

35P173- NV35 Short Form Engineering Board

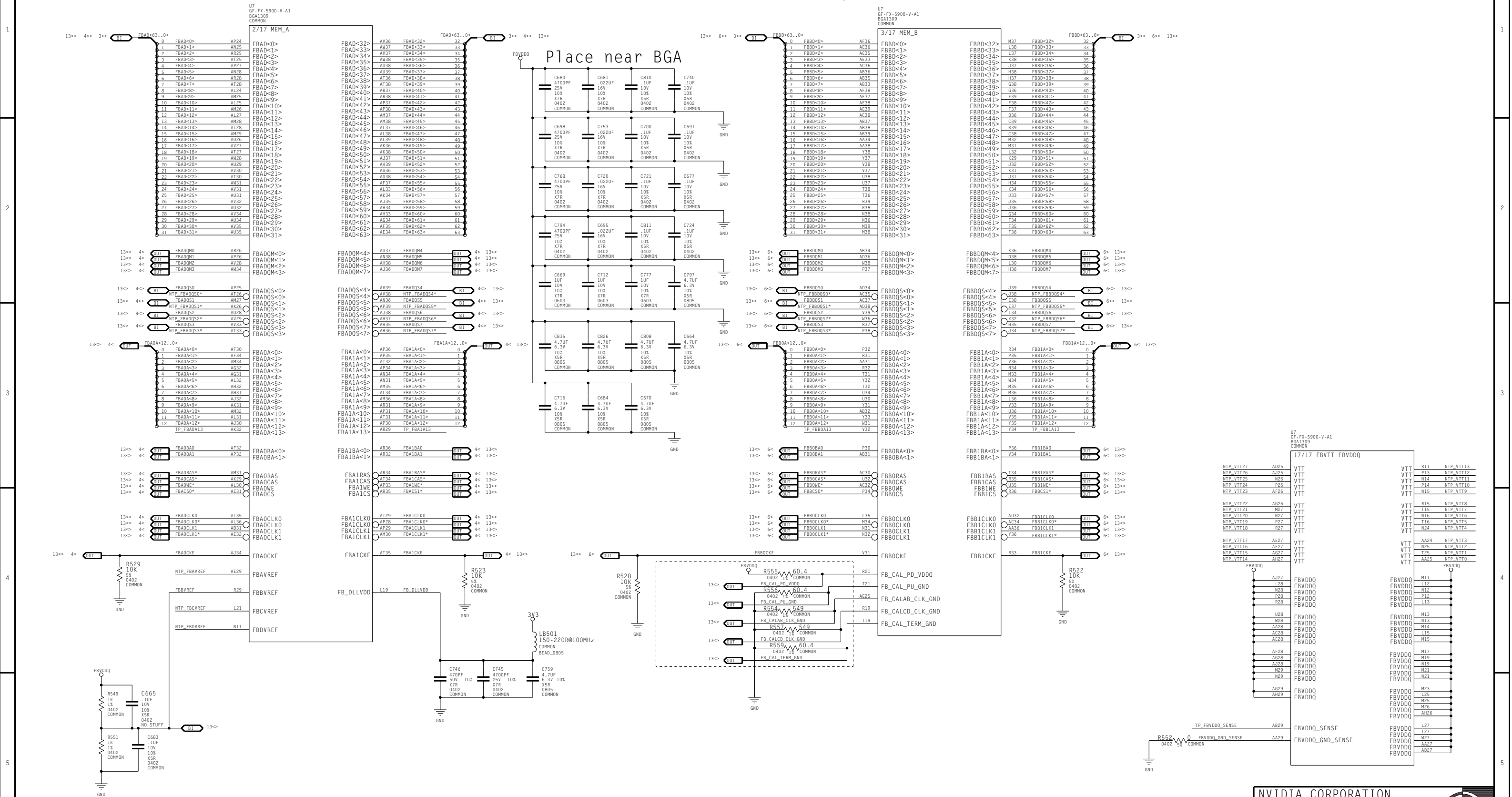
35P173_A01 - NV35 Flipchip BGA, 2 x 64MB DDR1 (8 x 4Mx32 = 128MB)
External TMD5 (SINGLE link), Internal TVout, Video Capture

Table of Contents:

- 1. Table of Contents .. this page
- 2. AGP 8X Interface
- 3. Memory: FB_A & FB_B Partitions, FBVDD/Q decoupling
- 4. Memory: FB_A
- 5. Memory: FB_B
- 6. Memory: FB_C & FB_D Partitions, FBVDD/Q decoupling
- 7. Memory: FB_C
- 8. Memory: FB_D
- 9. Memory: Decoupling
- 10. Memory Signal Constraints
- 11. BIOS, Strappings and Misc
- 12. DAC_A, DAC_B, PLL and SYNCbuffer
- 13. DVO/VIP Interface
- 14. DACA Filter and VGA connector
- 15. DACB VGA/TV Switch
- 16. DACB Filter and VGA connector
- 17. DVI Connector
- 18. TMD5 External with Silicon Image
- 19. Video Capture (SAA7114)
- 20. Video In/Out Connector External
Video In Connector Internal
- 21. GNDs, Thermal GNDs, Misc
- 22. GPIOs, NVVDD VID, TEMP and FAN Control
- 23. External Power Connection and Detection
- 24. Power Supply I: A3V3
- 25. Power Supply II: FBVDD/FBVDDQ/FBVTT
- 26. Power Supply III: NVVDD
- 27. Mechanical

SRO	VARIANT	NVPN	ASSEMBLY
8	BASE	600-10173-ssss-rrr	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	000	600-50173-0000-000	NV35 Value Board. 128 MB DVI-I, VGA)
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

3.Memory - FB_A & FB_B Partitions, FBVDD/Q decoupling



TO DO: RENAME TP_FBAA13 & TP_FBBA13 TO ABOVE NAMES

ASSEMBLY	NV35 Value Board. 128 MB DVI-I, VGA)
PAGE DETAIL	Memory: FBA & FBB Partitions, FBVDD/Q

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

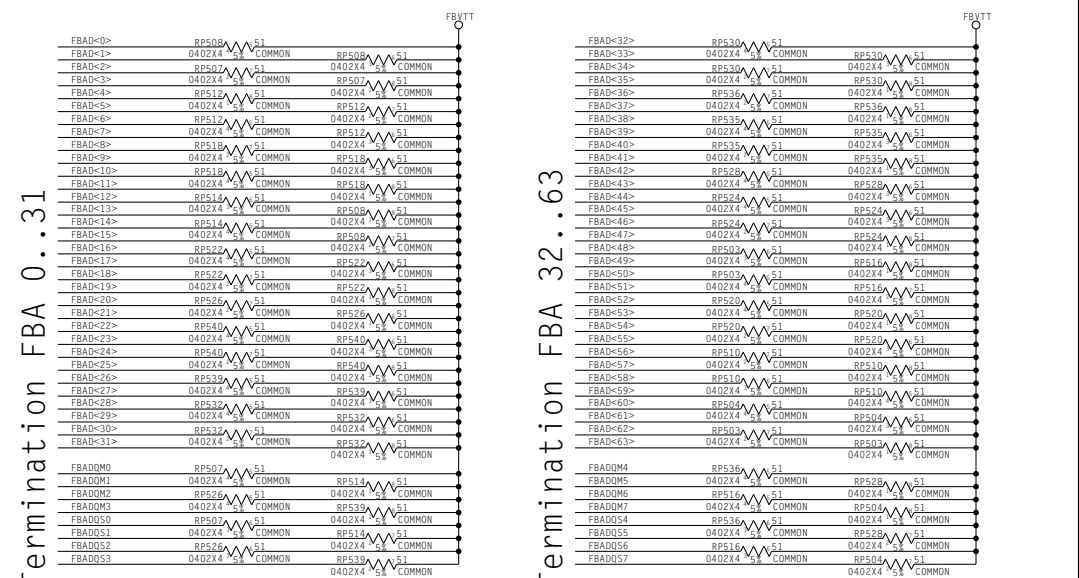
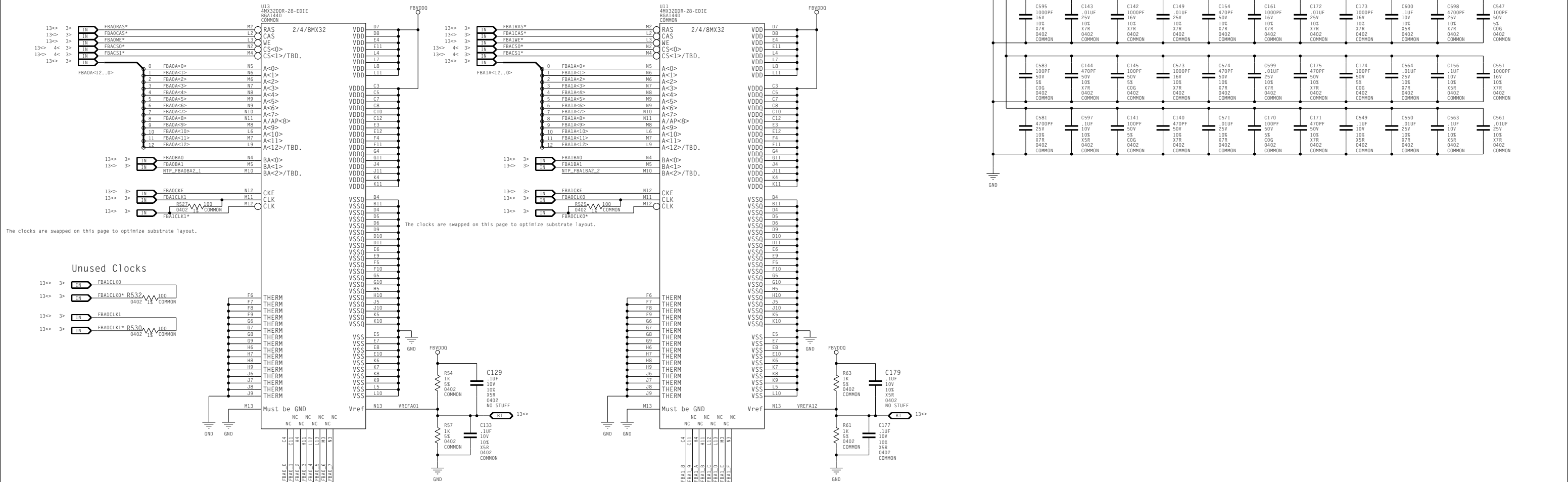
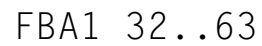
NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50173-0000-000
-------	--------------------

ID	design	PAGE	3 OF 27
NAME		DATE	19-JAN-2004

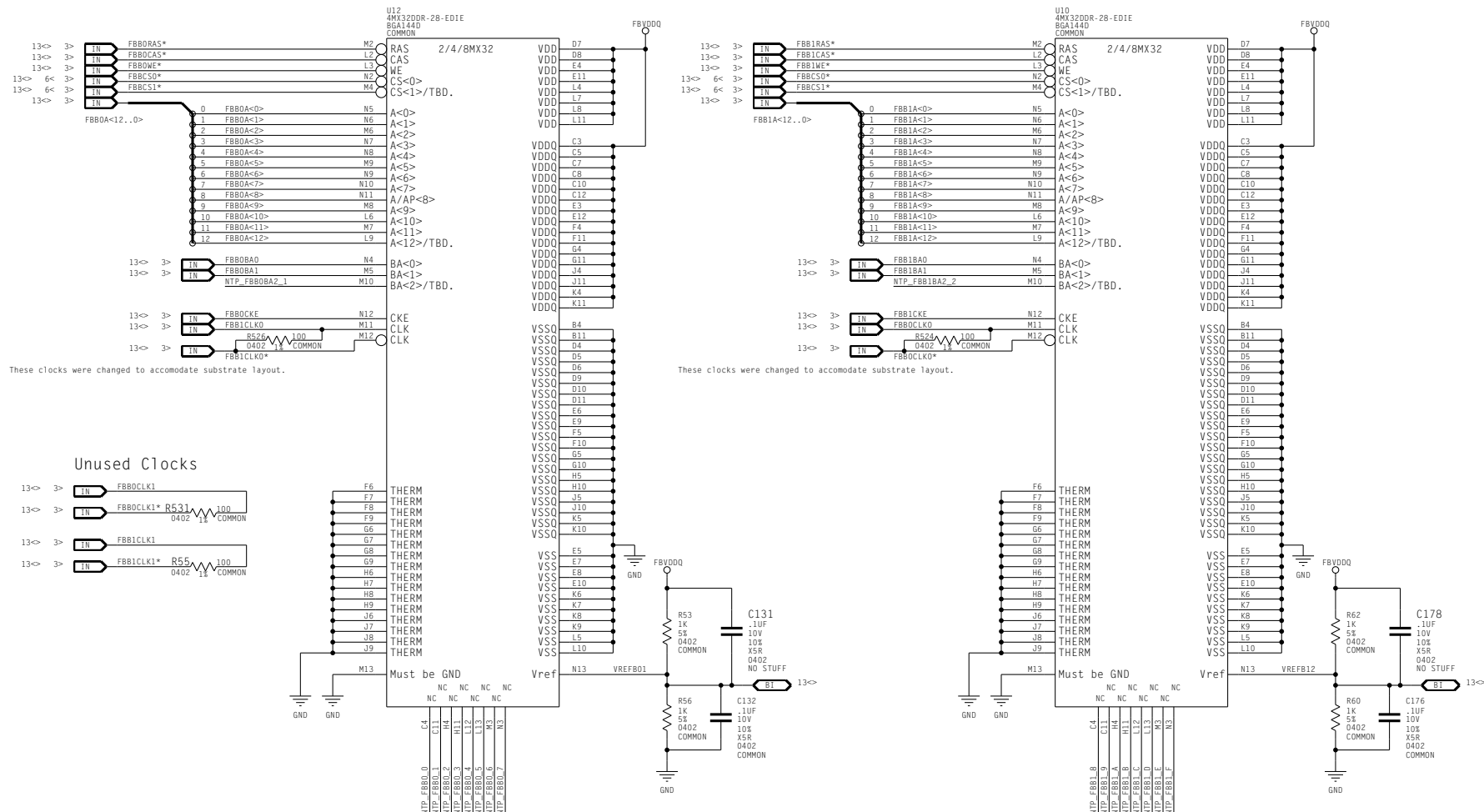
4. Memory Part. A - FBAD0..63



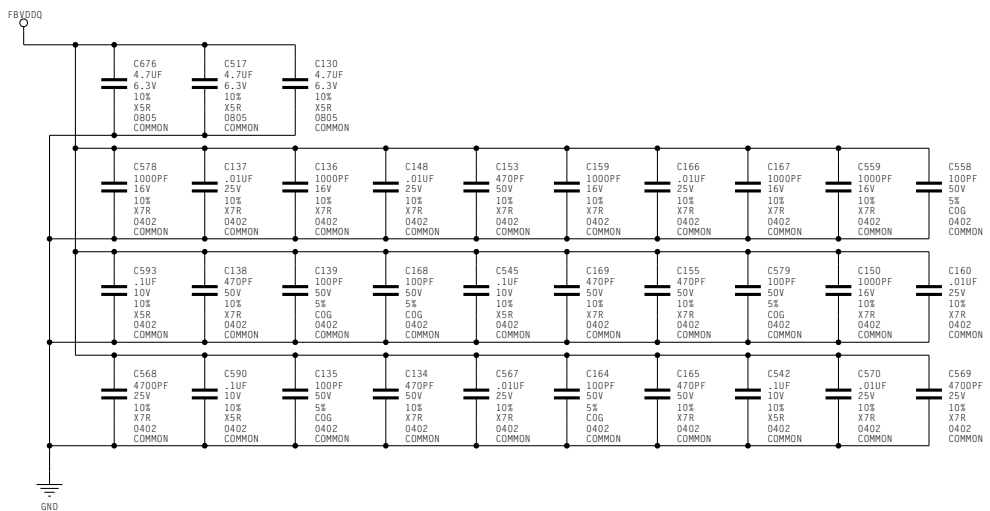
5. Memory Part. B - FBBD0..63

FBBD0 0..31

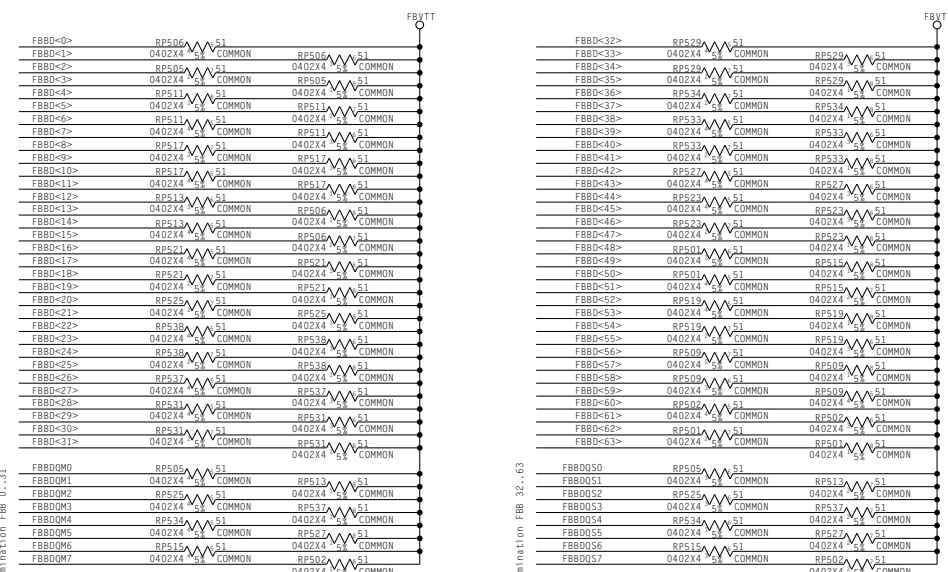
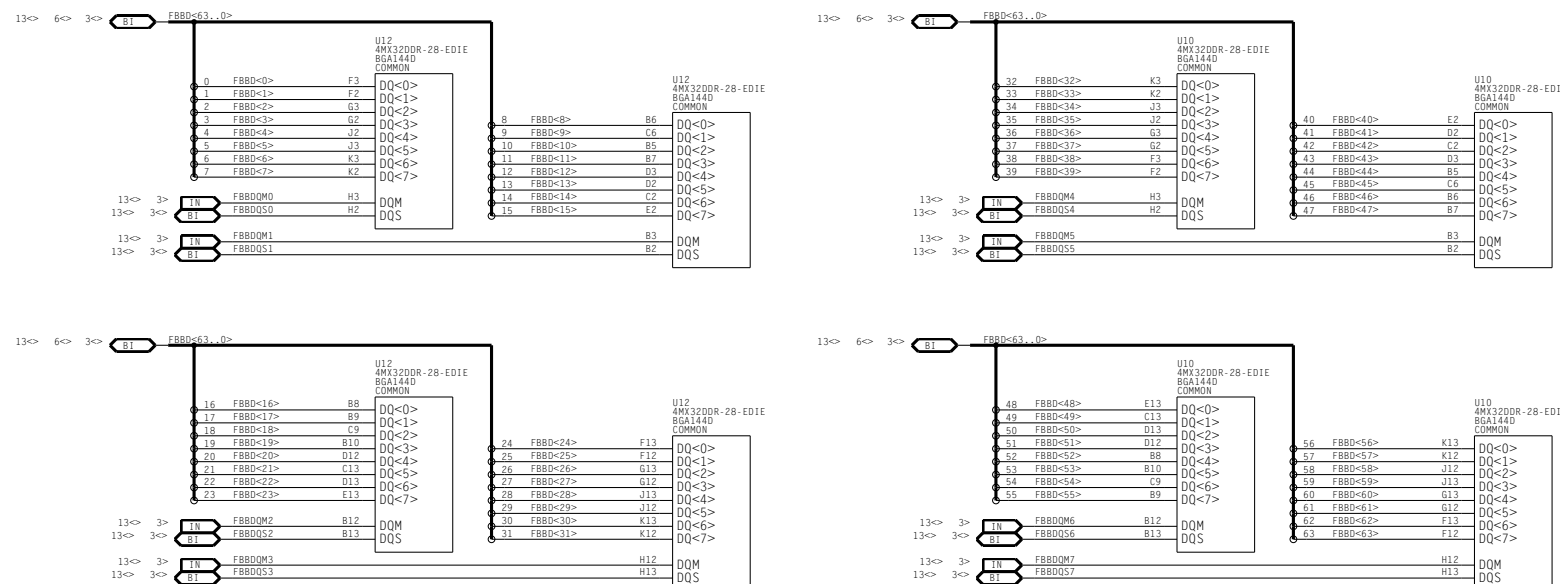
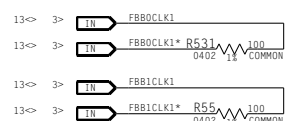
FBBD1 32..63



FBVDDQ Decoupling placement for whole Partition



Unused Clocks



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY NV35 Value Board, 128 MB DVI-I, VGA)
PAGE DETAIL Memory: FB_B

NVIDIA CORPORATION

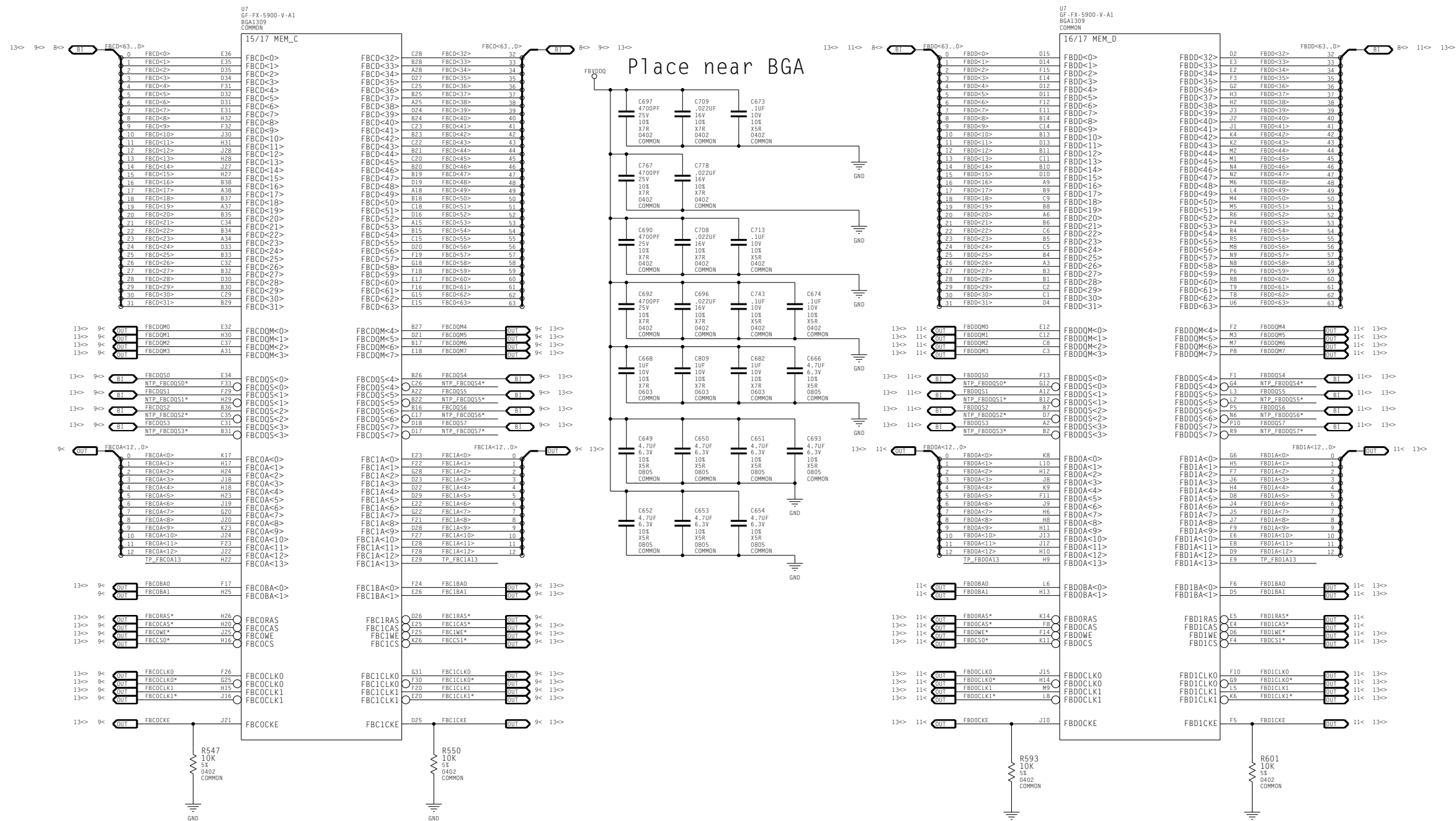
2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV_PN 600-50173-0000-000

ID design PAGE 5 OF 27
NAME DATE 19-JAN-2004

6. Memory FBC & FBD, FBVDD/Q decoupling

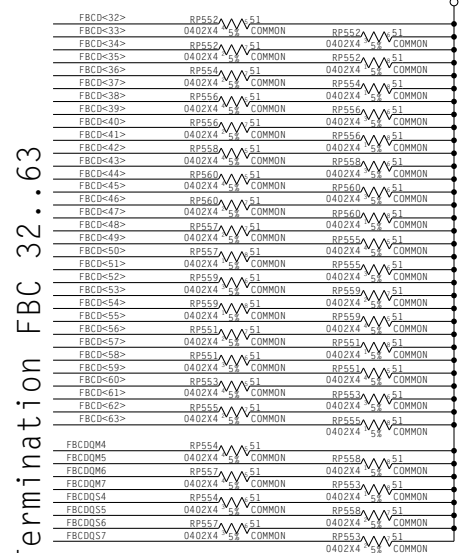
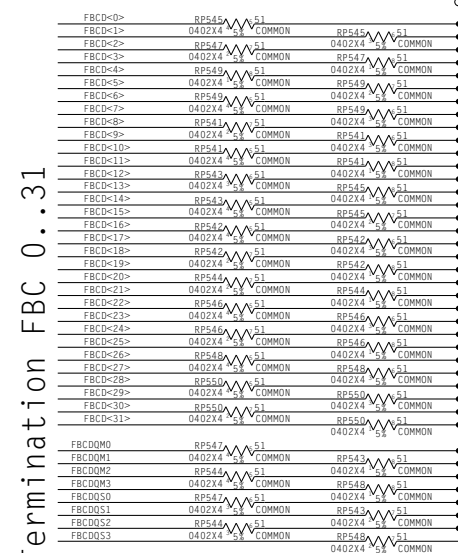
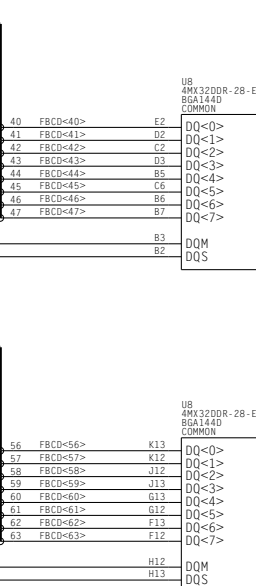
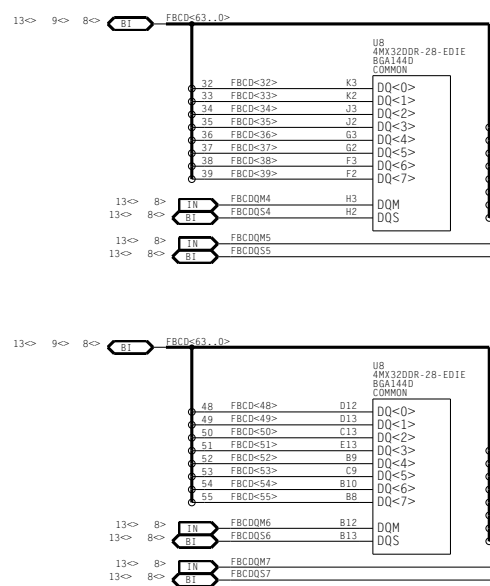
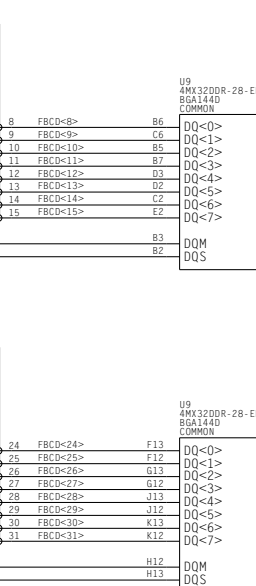
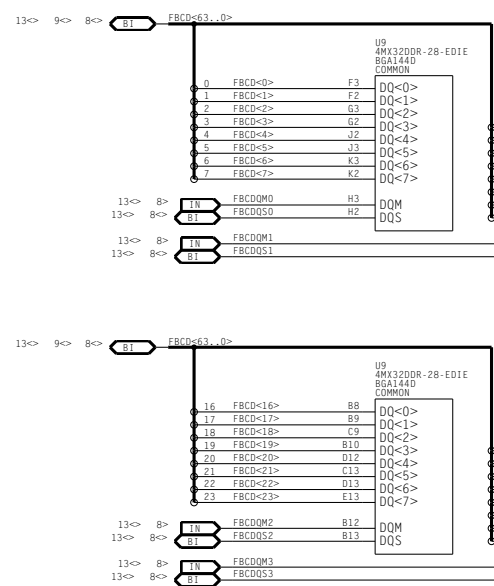
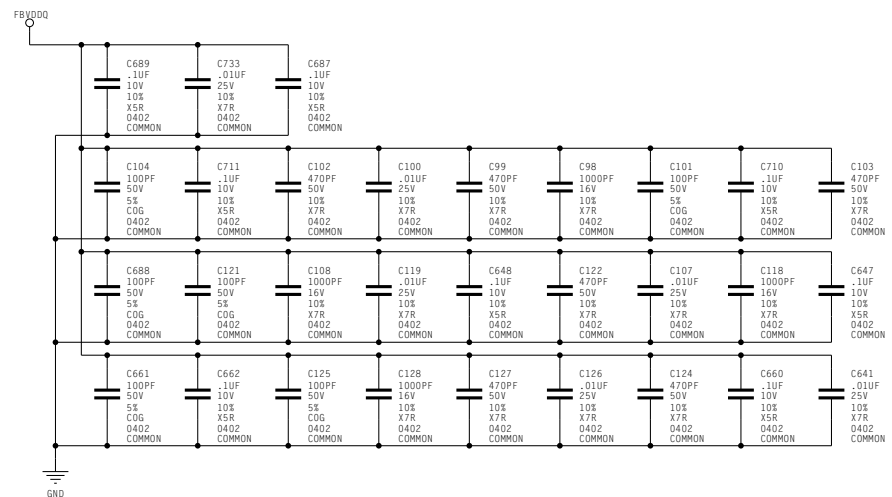
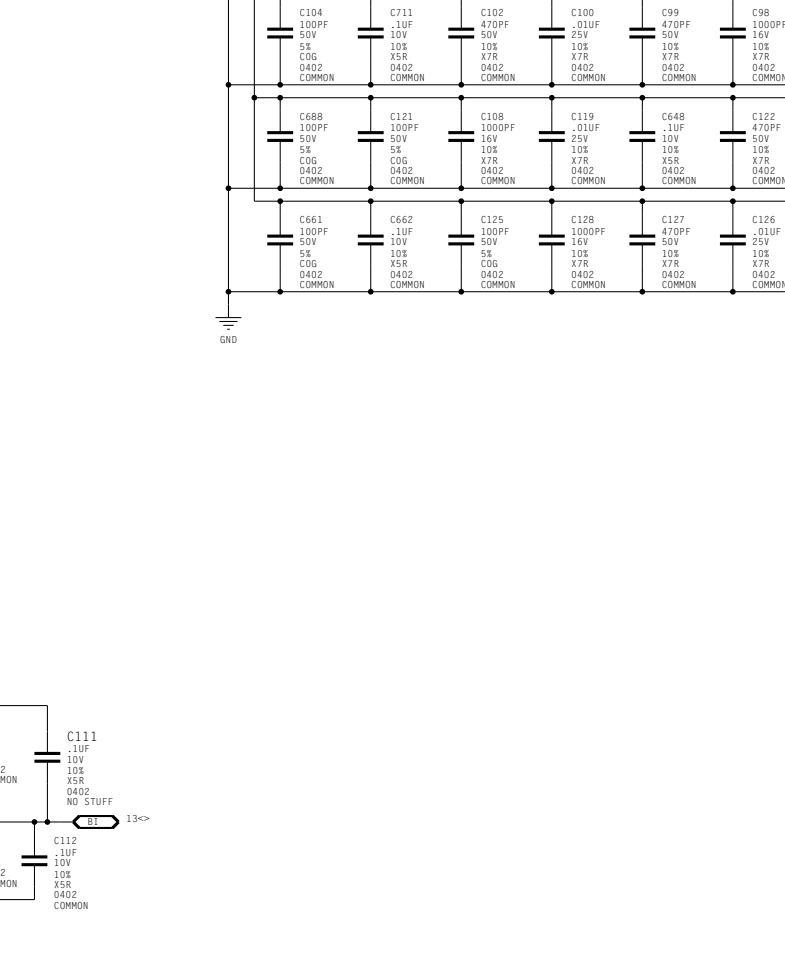
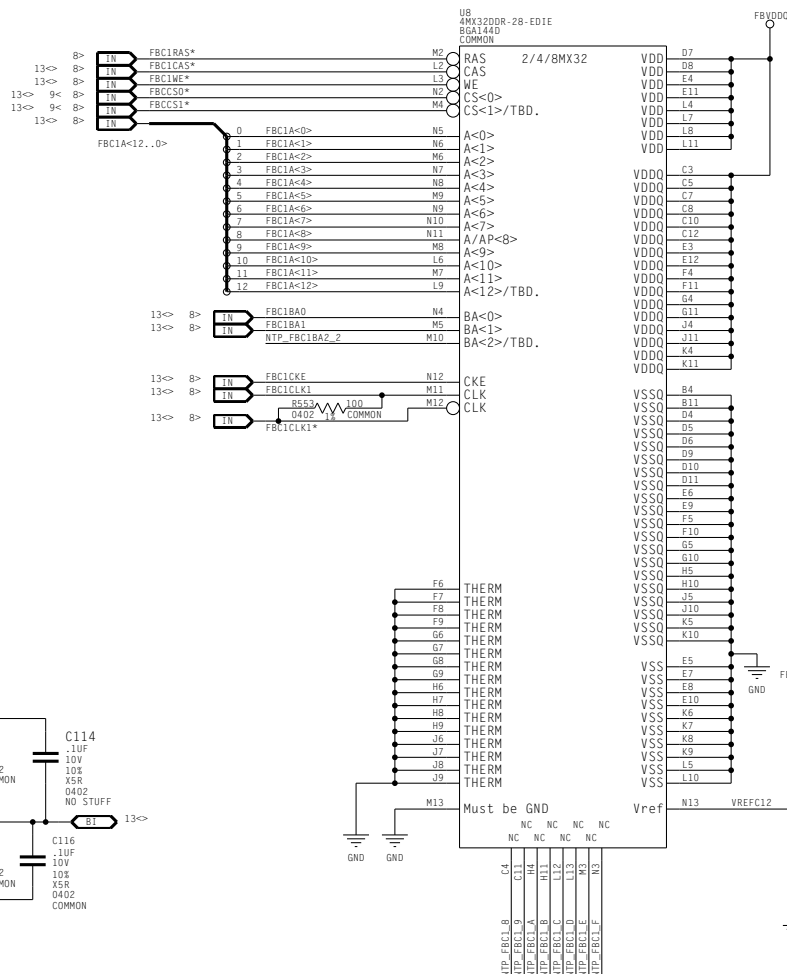
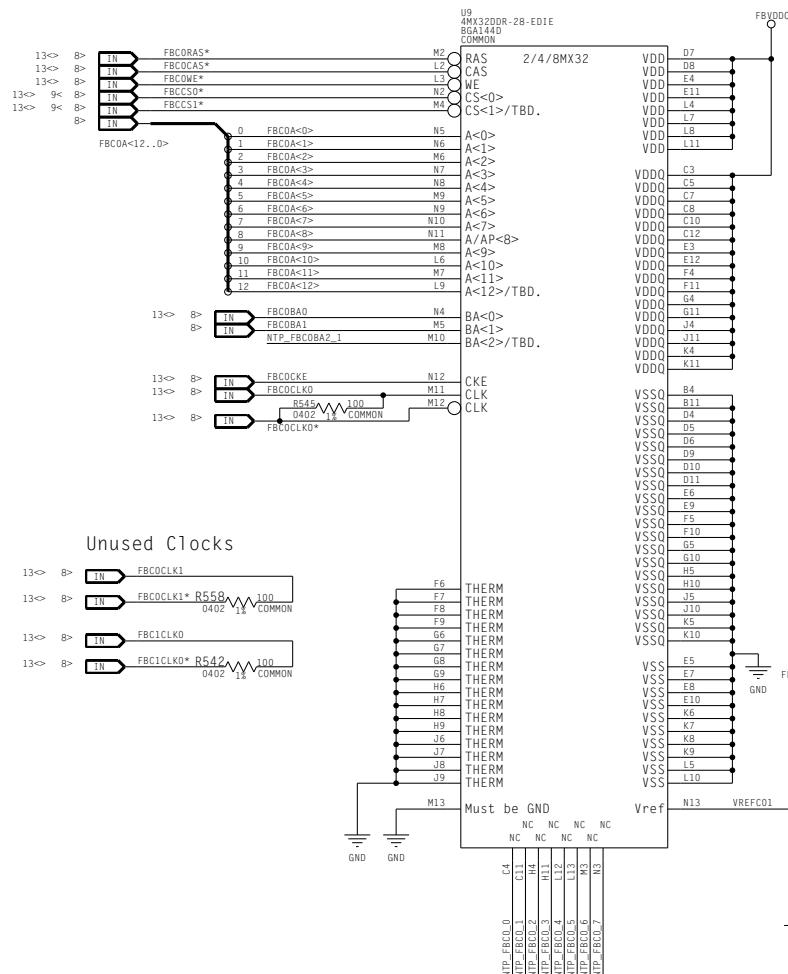
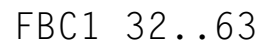


TO DO: RENAME TP_FBCx13 & TP_FBDx13 TO ABOVE NAMES

ASSEMBLY	NV35 Value Board. 128 MB DVI-I, VGA)
PAGE DETAIL	Memory: FBC & FBD Partitions, FBVDD/Q

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

7. Memory Part. C - FBCD0..63



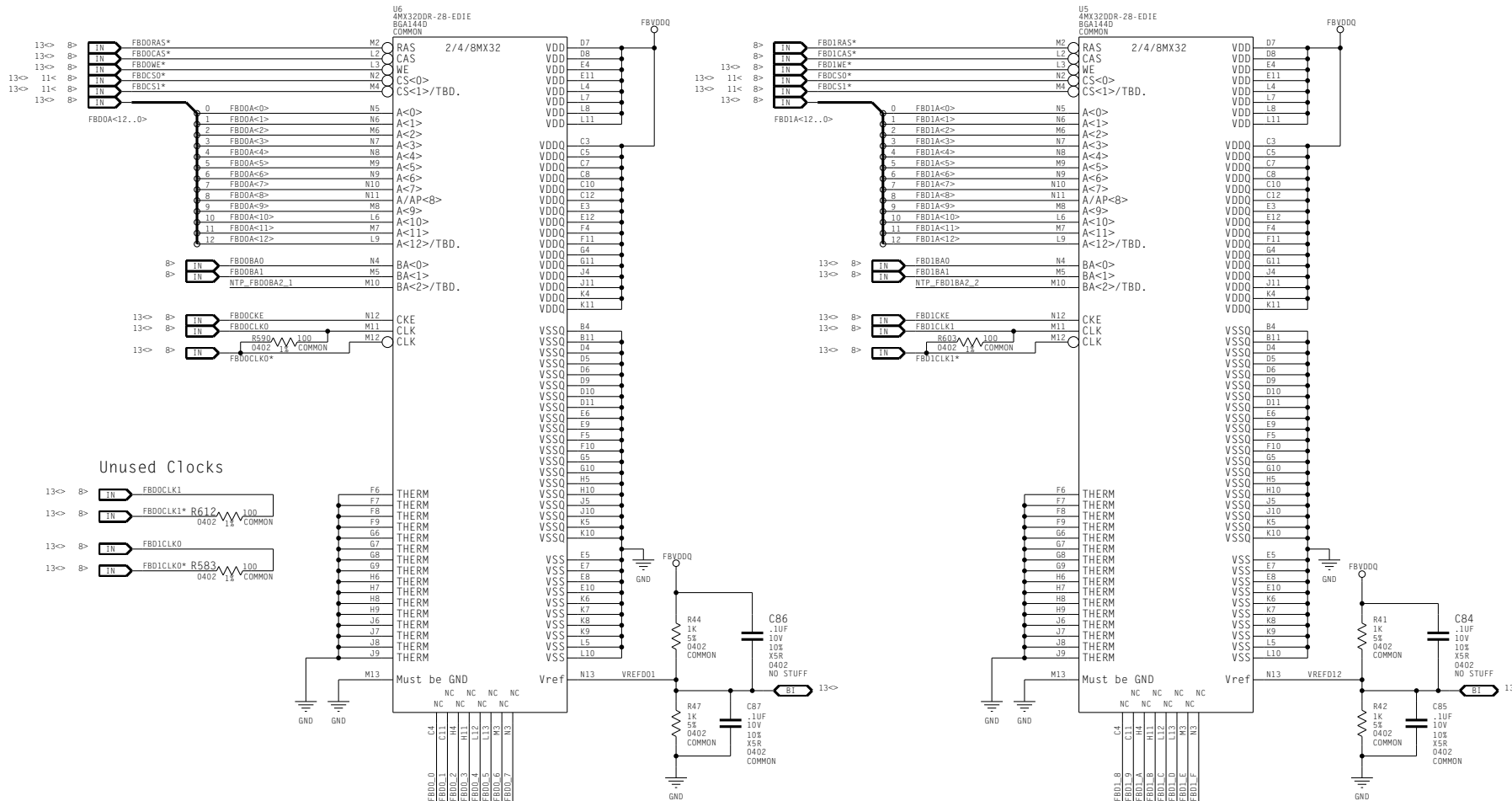
Termination FBC 0..31

Termination FBC 32..63

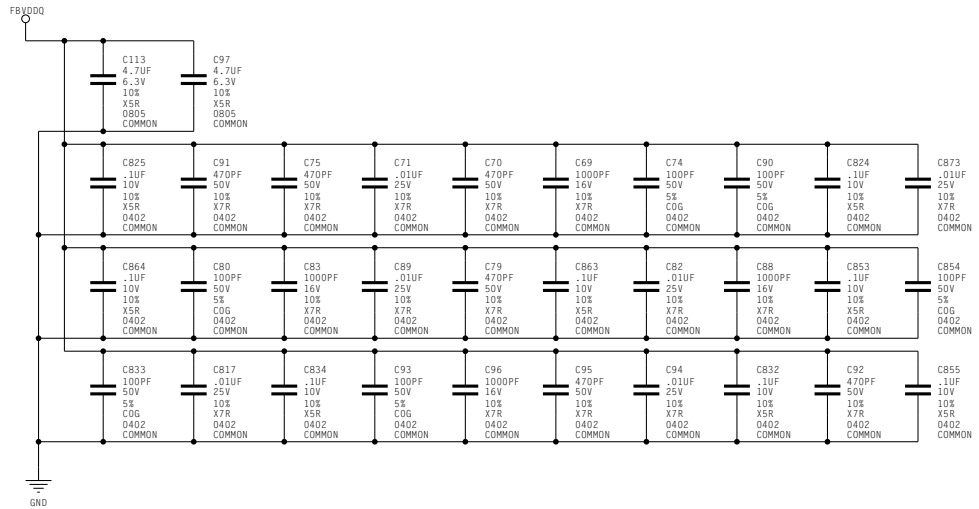
8. Memory Part. D - FBDD0..63

FBDD 0..31

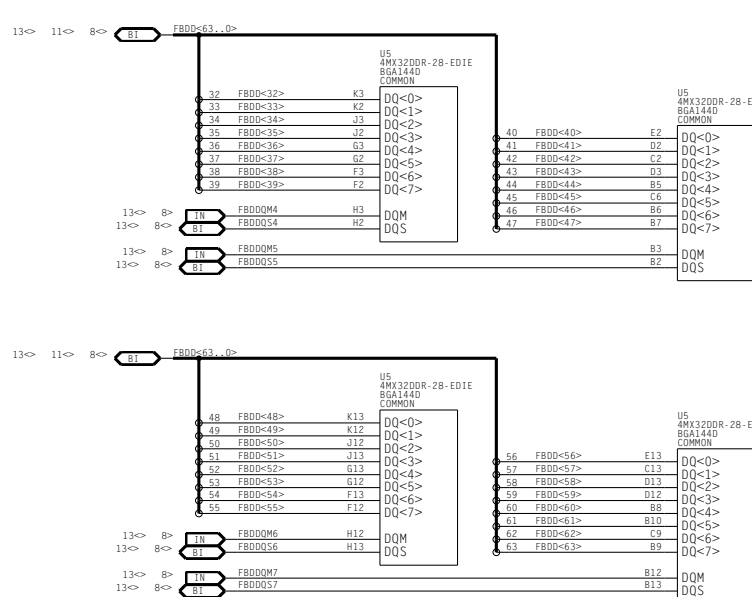
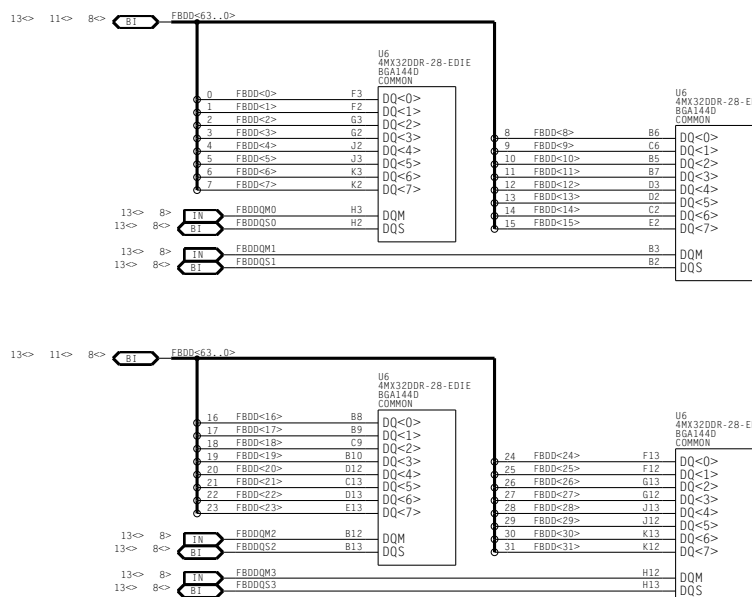
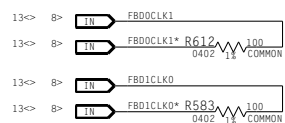
FBDD 32..63



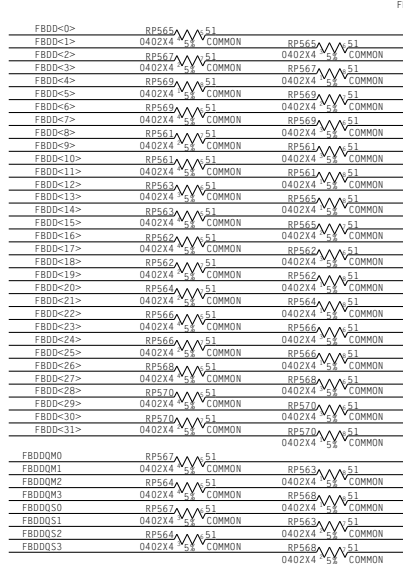
FBVDDQ Decoupling placement for whole Partition



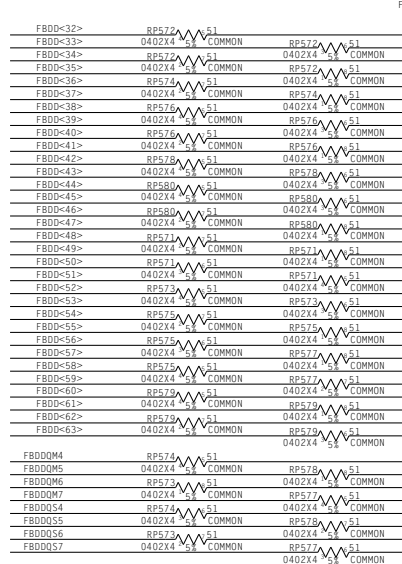
Unused Clocks



Termination FBD 0..31



Termination FBD 32..63



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY NV35 Value Board, 128 MB DVI-I, VGA)
PAGE DETAIL Memory: FB_D

NVIDIA CORPORATION

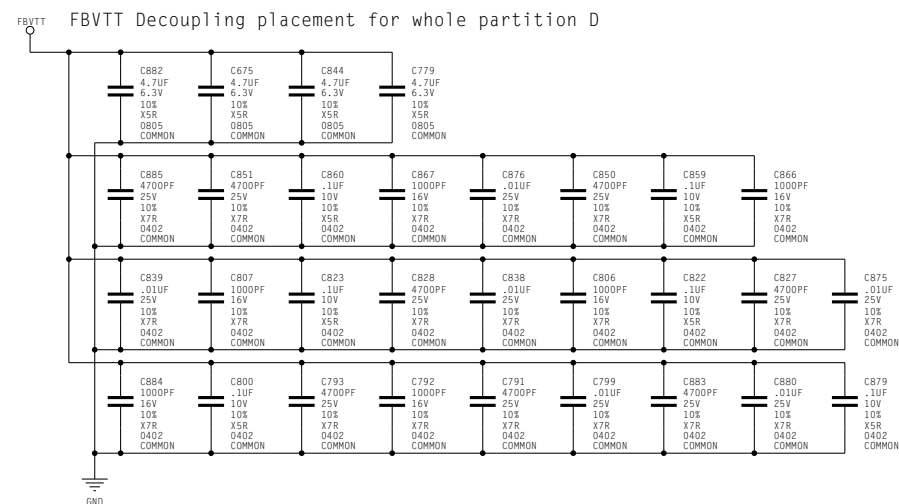
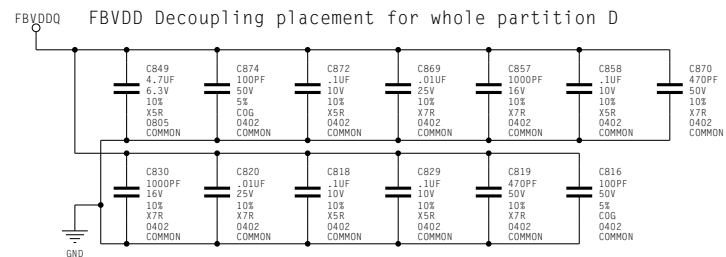
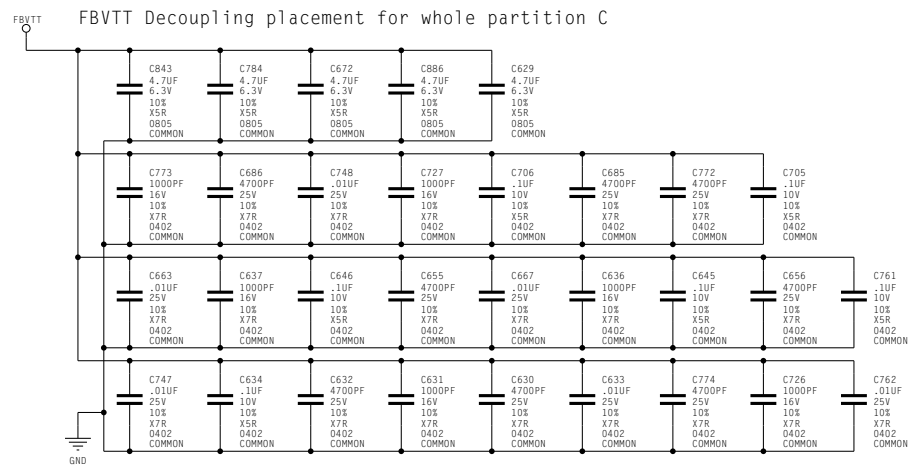
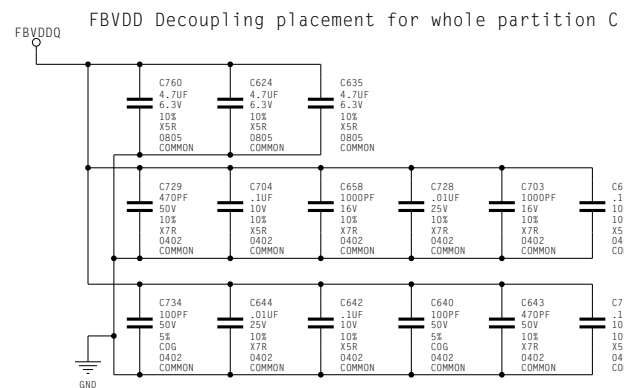
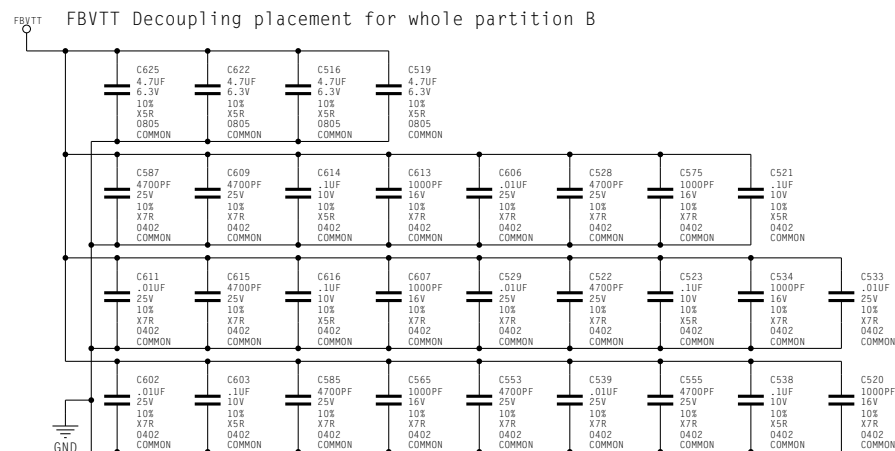
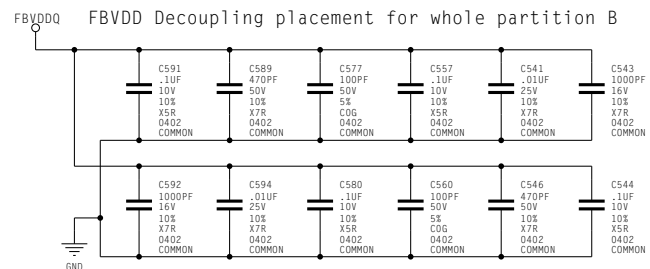
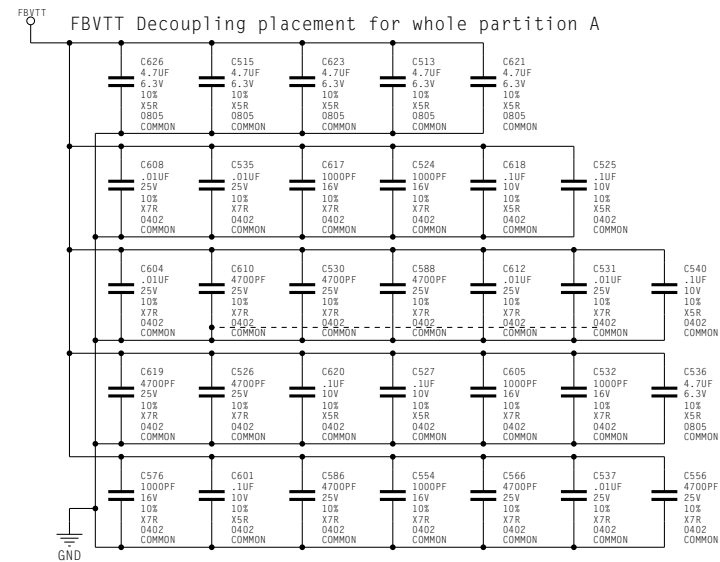
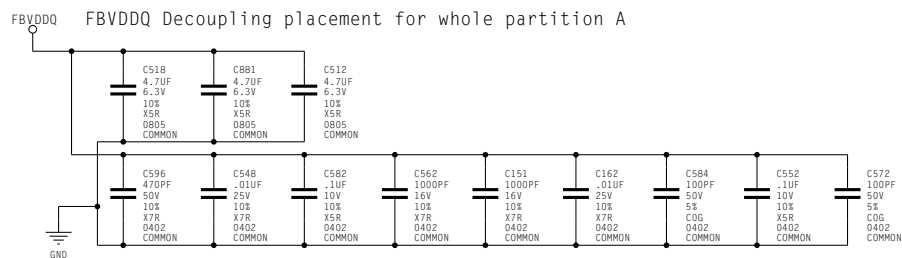
2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV_PN 600-50173-0000-000

ID desIgn PAGE 8 OF 27
NAME DATE 19-JAN-2004

9. Memory Decoupling



ASSEMBLY	NV35 Value Board. 128 MB DVI-I, VGA)
PAGE DETAIL	Memory: Decoupling

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

10. Memory NET SPACING RULES

Memory FBA FBB

NET Name	Diffpair	Spacing
FBA0CLK0	FBA0CLK0	18MIL_G2G_25MIL
FBA0CLK0*	FBA0CLK0	18MIL_G2G_25MIL
FBA0CLK1	FBA0CLK1	18MIL_G2G_25MIL
FBA0CLK1*	FBA0CLK1	18MIL_G2G_25MIL
FBA1CLK0	FBA1CLK0	18MIL_G2G_25MIL
FBA1CLK0*	FBA1CLK0	18MIL_G2G_25MIL
FBA1CLK1	FBA1CLK1	18MIL_G2G_25MIL
FBA1CLK1*	FBA1CLK1	18MIL_G2G_25MIL
FBB0CLK0	FBB0CLK0	18MIL_G2G_25MIL
FBB0CLK0*	FBB0CLK0	18MIL_G2G_25MIL
FBB0CLK1	FBB0CLK1	18MIL_G2G_25MIL
FBB0CLK1*	FBB0CLK1	18MIL_G2G_25MIL
FBB1CLK0	FBB1CLK0	18MIL_G2G_25MIL
FBB1CLK0*	FBB1CLK0	18MIL_G2G_25MIL
FBB1CLK1	FBB1CLK1	18MIL_G2G_25MIL
FBB1CLK1*	FBB1CLK1	18MIL_G2G_25MIL
FBA0<63..0>		15MIL
FBB0<63..0>		15MIL
FBA0QM0		15MIL
FBA0QM1		15MIL
FBA0QM2		15MIL
FBA0QM3		15MIL
FBA0QM4		15MIL
FBA0QM5		15MIL
FBA0QM6		15MIL
FBA0QM7		15MIL
FBB0QM0		15MIL
FBB0QM1		15MIL
FBB0QM2		15MIL
FBB0QM3		15MIL
FBB0QM4		15MIL
FBB0QM5		15MIL
FBB0QM6		15MIL
FBB0QM7		15MIL
FBA0QS0		20MIL
FBA0QS1		20MIL
FBA0QS2		20MIL
FBA0QS3		20MIL
FBA0QS4		20MIL
FBA0QS5		20MIL
FBA0QS6		20MIL
FBA0QS7		20MIL
FBB0QS0		20MIL
FBB0QS1		20MIL
FBB0QS2		20MIL
FBB0QS3		20MIL
FBB0QS4		20MIL
FBB0QS5		20MIL
FBB0QS6		20MIL
FBB0QS7		20MIL
FBA0A<13..0>		10MIL
FBA1A<13..0>		10MIL
FBB0A<13..0>		10MIL
FBB1A<13..0>		10MIL
FBA0RAS*		10MIL
FBA0CAS*		10MIL
FBA0WE*		10MIL
FBA0CKE		10MIL
FBA0BA0		10MIL
FBA0BA1		10MIL
FBA1RAS*		10MIL
FBA1CAS*		10MIL
FBA1WE*		10MIL
FBA1CKE		10MIL
FBA1BA0		10MIL
FBA1BA1		10MIL
FBB0RAS*		10MIL
FBB0CAS*		10MIL
FBB0WE*		10MIL
FBB0CKE		10MIL
FBB0BA0		10MIL
FBB0BA1		10MIL
FBB1RAS*		10MIL
FBB1CAS*		10MIL
FBB1WE*		10MIL
FBB1CKE		10MIL
FBB1BA0		10MIL
FBB1BA1		10MIL
FBA0CS0*		10MIL
FBA0CS1*		10MIL
FBB0CS0*		10MIL
FBB0CS1*		10MIL

FB_CAL...

FB_CAL_PD_VDDQ	20MIL_G2G_25MIL
FB_CAL_PU_GND	20MIL_G2G_25MIL
FB_CAL_CLK_GND	20MIL_G2G_25MIL
FB_CAL_TERM_GND	20MIL_G2G_25MIL
FB_CALAB_CLK_GND	20MIL_G2G_25MIL
FB_CALCD_CLK_GND	20MIL_G2G_25MIL

Memory FBC FBD

NET Name	Diffpair	Spacing
FBC0CLK0	FBC0CLK0	18MIL_G2G_25MIL
FBC0CLK0*	FBC0CLK0	18MIL_G2G_25MIL
FBC0CLK1	FBC0CLK1	18MIL_G2G_25MIL
FBC0CLK1*	FBC0CLK1	18MIL_G2G_25MIL
FBC1CLK0	FBC1CLK0	18MIL_G2G_25MIL
FBC1CLK0*	FBC1CLK0	18MIL_G2G_25MIL
FBC1CLK1	FBC1CLK1	18MIL_G2G_25MIL
FBC1CLK1*	FBC1CLK1	18MIL_G2G_25MIL
FBD0CLK0	FBD0CLK0	18MIL_G2G_25MIL
FBD0CLK0*	FBD0CLK0	18MIL_G2G_25MIL
FBD0CLK1	FBD0CLK1	18MIL_G2G_25MIL
FBD0CLK1*	FBD0CLK1	18MIL_G2G_25MIL
FBD1CLK0	FBD1CLK0	18MIL_G2G_25MIL
FBD1CLK0*	FBD1CLK0	18MIL_G2G_25MIL
FBD1CLK1	FBD1CLK1	18MIL_G2G_25MIL
FBD1CLK1*	FBD1CLK1	18MIL_G2G_25MIL
FBCD<63..0>		15MIL
FBD0<63..0>		15MIL
FBC0QM0		15MIL
FBC0QM1		15MIL
FBC0QM2		15MIL
FBC0QM3		15MIL
FBC0QM4		15MIL
FBC0QM5		15MIL
FBC0QM6		15MIL
FBC0QM7		15MIL
FBD0QM0		15MIL
FBD0QM1		15MIL
FBD0QM2		15MIL
FBD0QM3		15MIL
FBD0QM4		15MIL
FBD0QM5		15MIL
FBD0QM6		15MIL
FBD0QM7		15MIL
FBC0QS0		20MIL
FBC0QS1		20MIL
FBC0QS2		20MIL
FBC0QS3		20MIL
FBC0QS4		20MIL
FBC0QS5		20MIL
FBC0QS6		20MIL
FBC0QS7		20MIL
FBD0QS0		20MIL
FBD0QS1		20MIL
FBD0QS2		20MIL
FBD0QS3		20MIL
FBD0QS4		20MIL
FBD0QS5		20MIL
FBD0QS6		20MIL
FBD0QS7		20MIL
FBC0A<13..0>		10MIL
FBC1A<13..0>		10MIL
FBD0A<13..0>		10MIL
FBD1A<13..0>		10MIL
FBC0RAS*		10MIL
FBC0CAS*		10MIL
FBC0WE*		10MIL
FBC0CKE		10MIL
FBC0BA0		10MIL
FBC1BA1		10MIL
FBC0RAS*		10MIL
FBC1CAS*		10MIL
FBC1WE*		10MIL
FBC1CKE		10MIL
FBC1BA0		10MIL
FBC1BA1		10MIL
FBD0RAS*		10MIL
FBD0CAS*		10MIL
FBD0WE*		10MIL
FBD0CKE		10MIL
FBD1BA0		10MIL
FBD1BA1		10MIL
FBD0RAS*		10MIL
FBD0CAS*		10MIL
FBD1WE*		10MIL
FBD1CKE		10MIL
FBD1BA0		10MIL
FBD1BA1		10MIL
FBC0CS0*		10MIL
FBC0CS1*		10MIL
FBD0CS0*		10MIL
FBD0CS1*		10MIL

FBBVREF

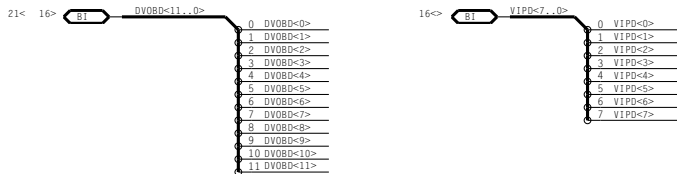
FBBVREF	12MIL_TRACE
VREFA01	12MIL_TRACE
VREFA02	12MIL_TRACE
VREFA11	12MIL_TRACE
VREFA12	12MIL_TRACE
VREFB01	12MIL_TRACE
VREFB02	12MIL_TRACE
VREFB11	12MIL_TRACE
VREFB12	12MIL_TRACE
VREFC01	12MIL_TRACE
VREFC02	12MIL_TRACE
VREFC11	12MIL_TRACE
VREFC12	12MIL_TRACE
VREFD01	12MIL_TRACE
VREFD02	12MIL_TRACE
VREFD11	12MIL_TRACE
VREFD12	12MIL_TRACE

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

11. BIOS, Straps, Misc

Straps

Assembly: BIOS



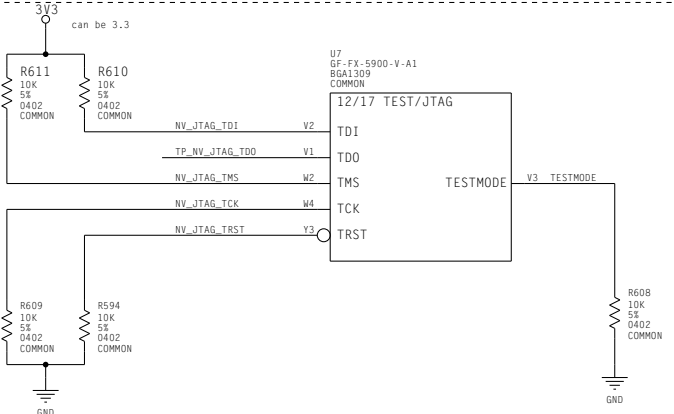
REG: NV_PEXTDEV_BOOT_0

Bit	Signal	VALUE_ID	VALUES
00:	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED 1 NORMAL
01:	SUB_VENDOR	SUB_VENDOR	0 NO_BIOS 1 read_from_BIOS
02:	RAM_CFG_0	RAM_CFG[3:0]	0000 RFU 0001 RFU 0010 RFU 0011 RFU 0100 RFU 0101 RFU 0110 RFU 0111 RFU
03:	RAM_CFG_1		
04:	RAM_CFG_2		
05:	RAM_CFG_3		
06:	CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz 01 14.31818 Mhz 10 27.000 Mhz 11 unknown
22:	CRYSTAL_1		
07:	TV_MODE_0	TV_MODE[1:0]	00 SECAM 01 NTSC 10 PAL 11 CRT
08:	TV_MODE_1		
09:	AGP8xEnable	AGP_30_8x	0 AGP8x enabled 1 AGP8x disabled
10:	AGP_SBA	AGP_SBA[0]	0 SBA enabled 1 SBA disabled
11:	AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled
12:	PCI_DEVIO_0	PCI_DEVIO[3:0]	0000 0x330 ... 1111 0x033F 0000 (default 0x330)
13:	PCI_DEVIO_1		
20:	PCI_DEVIO_2		
21:	PCI_DEVIO_3		
14:	BUS_TYPE	BUS_TYPE[0]	0 PCI 1 AGP
15:	FP_IFACE	FP_IFACE[0]	0 24bit 1 128bit
23:	FB_0	FB[1:0]	00 64M 01 128M 10 256M 11 512M
24:	FB_1		
25:	BR	BR[0]	0 BRIDGE disabled 1 BRIDGE enabled
26:	BR_128M	BR bits are ignored if BRIDGE is disabled	
27:	BR_AGP		
28:	BR_ID		
29:	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F 10 Serial_SST45VF 11 RFU
30:	ROM_TYPE_1		
16:	USER_0	STRAP_USER[3:0]	0000 (default)
17:	USER_1		
18:	USER_2		
19:	USER_3		

REG: NV_PEXTDEV_BOOT_3

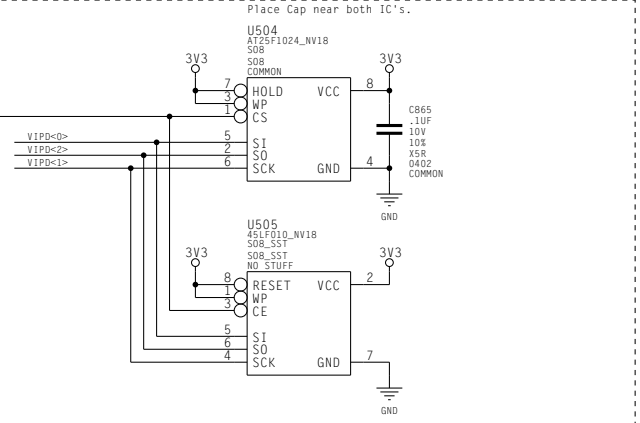
Bit	Signal	VALUE_ID	VALUES
00:	I394_EN_0	I394[0]	0 I394 disabled 1 I394 enabled
06:	BR_LAST_DEV		
07:	BR_BARI_BCASTONLY		
09:	BOARD		

Test/JTAG



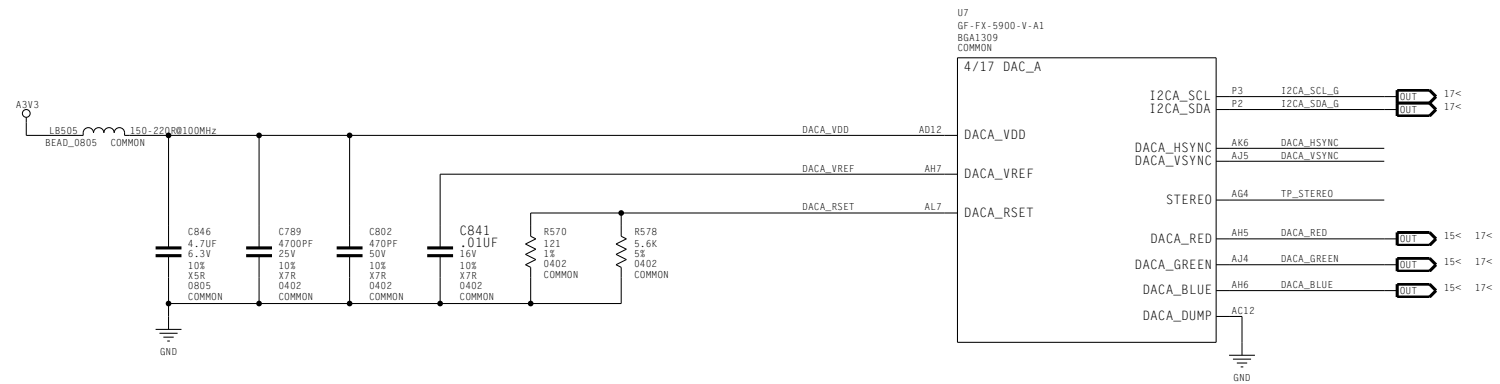
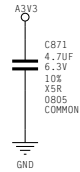
BIOS (serial)

Assembly: BIOS*

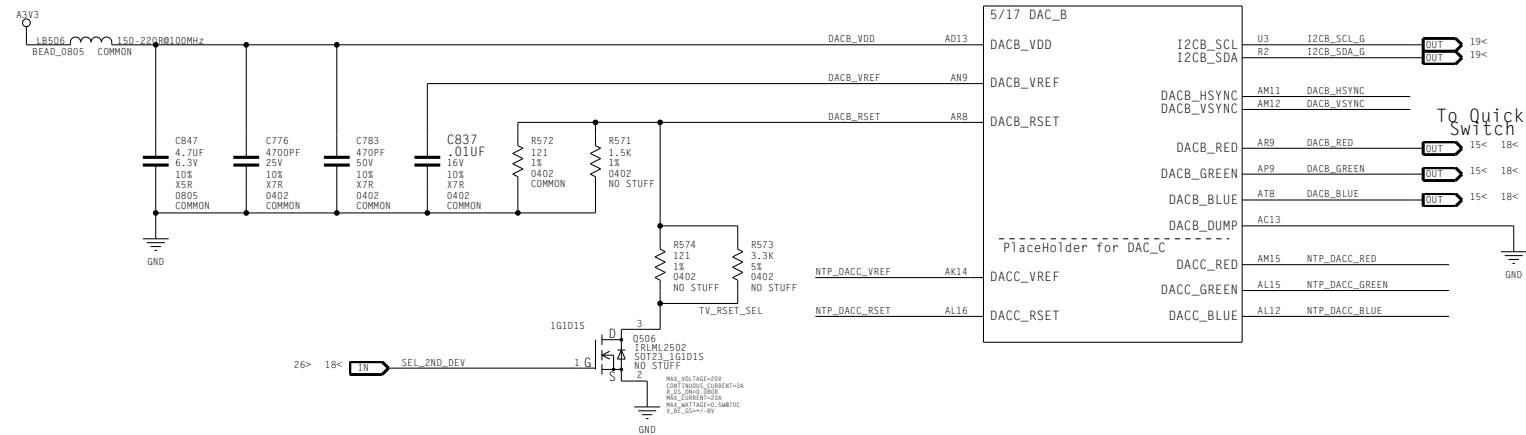


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

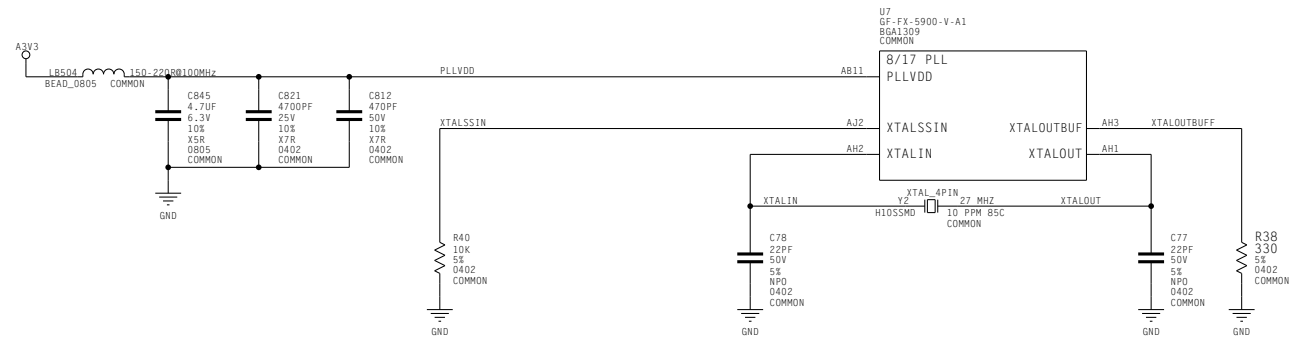
DACA



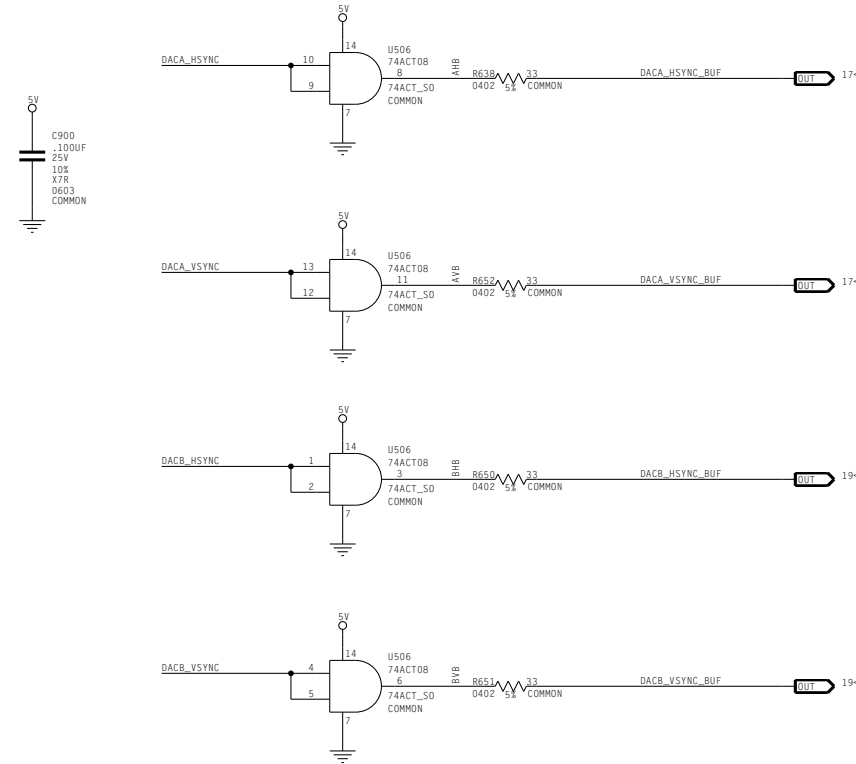
DACB



XTAL/PLLVD



DAC Sync Buffer



NET RULES

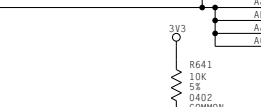
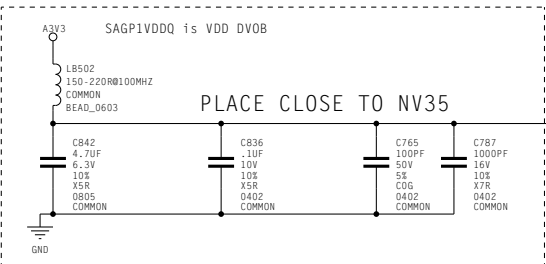
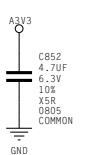
	NET	SPACING	PHYSICAL
	1N XTALIN	15MIL	5MIL TRACE
	1N XTALOUT	15MIL	5MIL TRACE
17< 15>	1N DACA_RED	20MIL G26_30MIL	
17< 15>	1N DACA_GREEN	20MIL G26_30MIL	
17< 15>	1N DACA_BLUE	20MIL G26_30MIL	
18< 15>	1N DACB_RED	20MIL G26_30MIL	
18< 15>	1N DACB_GREEN	20MIL G26_30MIL	
18< 15>	1N DACB_BLUE	20MIL G26_30MIL	
	1N DACA_VDD		16MIL TRACE
	1N DACA_RSET		16MIL TRACE
	1N DACA_VREF		16MIL TRACE
	1N DACA_VDD		16MIL TRACE
	1N DACA_RSET		16MIL TRACE
	1N DACA_VREF		16MIL TRACE
	1N PLLVDD		16MIL TRACE

13. DVO/VIP Interface

NET RULES

NET	PHYSICAL	SPACING
SAGPOCALPD_VDDQ	12MIL_TRACE	20MIL
SAGPICALPD_VDDQ	12MIL_TRACE	20MIL
SAGPOCALPU_GND	12MIL_TRACE	20MIL
SAGPICALPU_GND	12MIL_TRACE	20MIL
DVOA_VDD	16MIL_TRACE	
DVOB_VDD	16MIL_TRACE	
DVOAD<23..0>		10MIL
DVOAR<23..0>		10MIL

Place near
Power Filter



U7
GF-FX-5900-V-A1
86A1309
COMMON

7/17 DVOA DVOB VIP

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGPOVDDQ
SAGPOVDDQ
SAGPOVDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

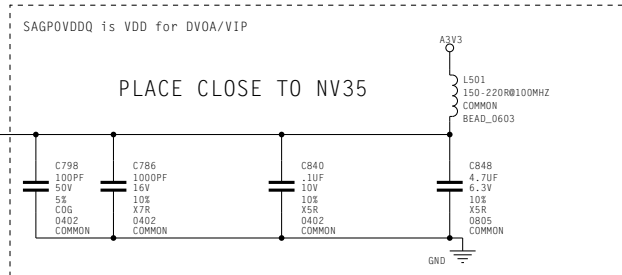
SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

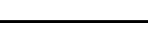
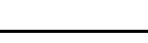
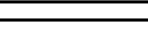
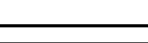
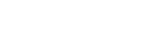
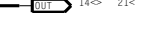
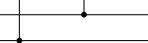
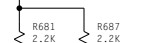
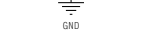
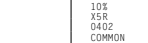
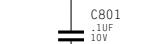
SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ

SAGP1VDDQ
SAGP1VDDQ
SAGP1VDDQ



Decoupling for VD50CLAMP1



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

ASSEMBLY

NV35 Value Board, 128 MB DVI-I, VGA)

PAGE DETAIL

DVO/VIP Interface

NV_PN

600-50173-0000-000

ID

des1gn

PAGE

13 OF 27

NAME

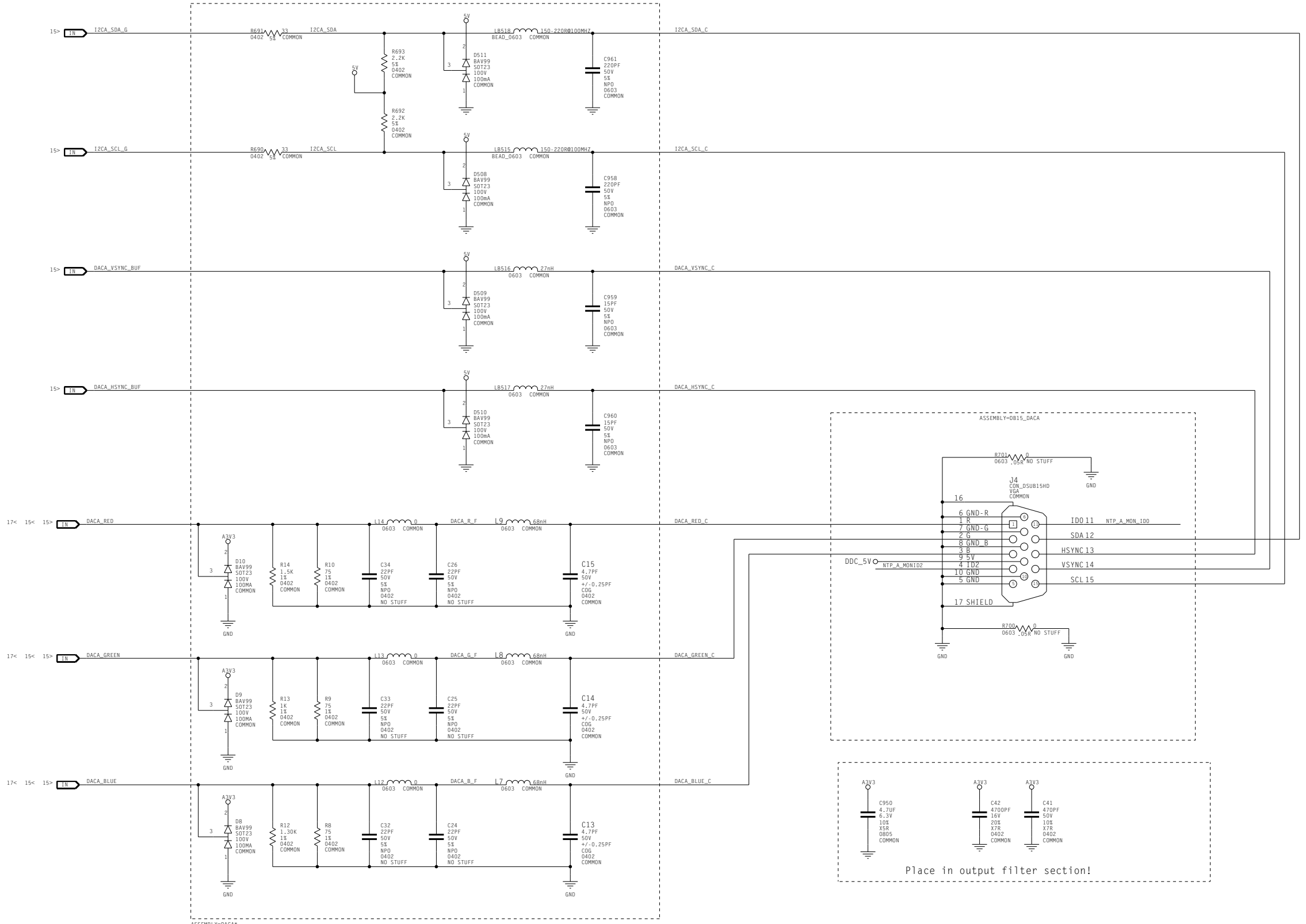
DATE

19-JAN-2004

14. DACA RGB filters, VGA connector Output (south)

DACA RGB-FILTER

DACA VGA connector



NET RULES		
NET	PHYSICAL	SPACING
DACA_RED	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACA_GREEN	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACA_BLUE	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACA_R_F	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACA_G_F	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACA_B_F	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACA_RED_C	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACA_GREEN_C	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACA_BLUE_C	NOTE:37.50hm Impedance	20MIL_G2G_30MIL

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

ASSEMBLY

NV35 Value Board, 128 MB DVI-I, VGA)

PAGE DETAIL

DACA Filter and VGA connector

NV_PN

600-50173-0000-000

ID

design

PAGE

14 OF 27

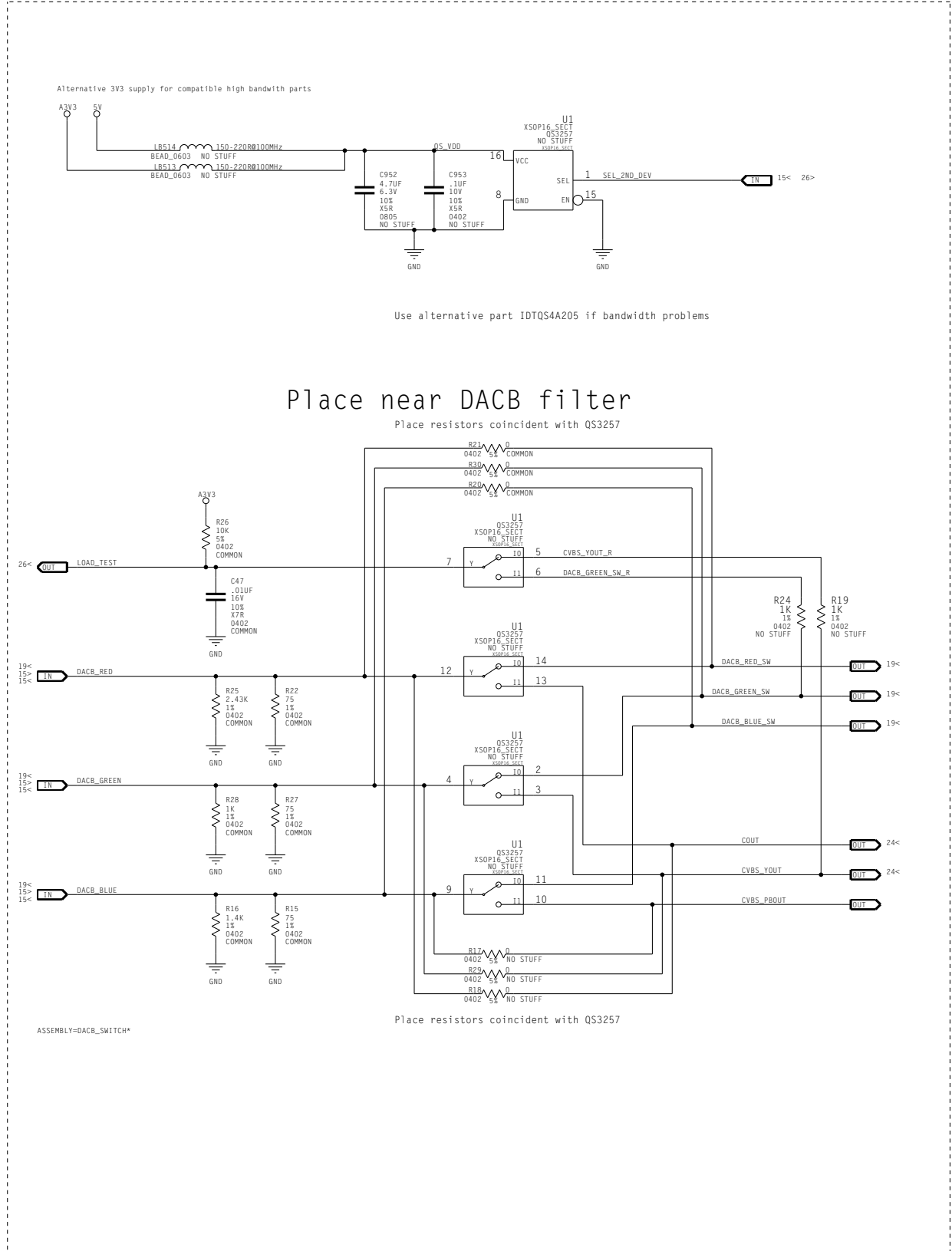
NAME

DATE

19-JAN-2004

15. DACB VGA/TV Switch

Quickswitch for DACB



ASSEMBLY		NV35 Value Board, 128 MB DVI-I, VGA)	
PAGE DETAIL		DACB VGA/TV Switch	

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN

600-50173-0000-000

ID

des1gn

PAGE

15 OF 27

NAME

DATE

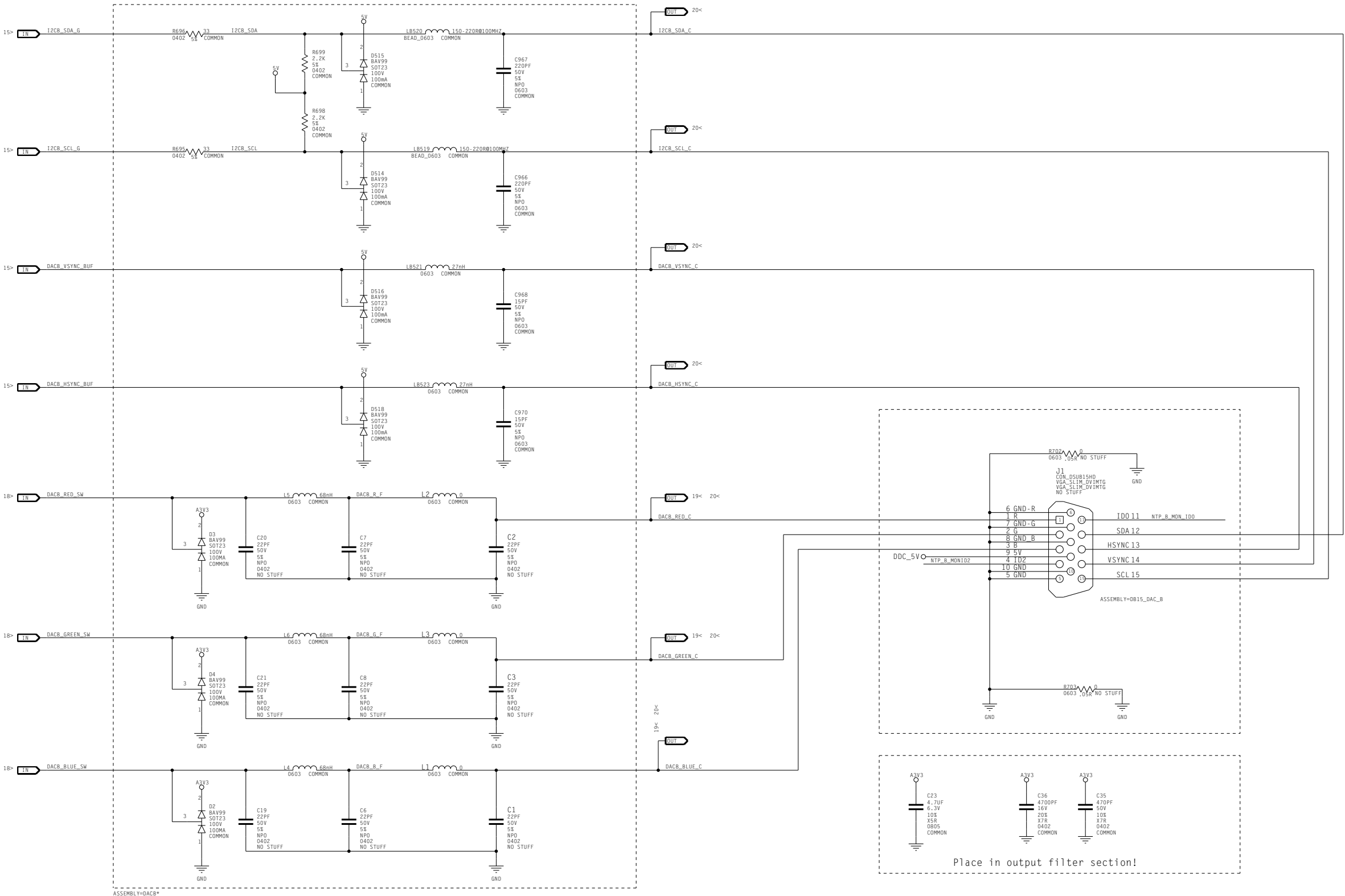
19-JAN-2004



16. DACB RGB filters, VGA connector (north)

DACB RGB-FILTER

DACB VGA connector



NET RULES		
NET	PHYSICAL	SPACING
DACB_RED	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACB_GREEN	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACB_BLUE	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACB_R_F	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACB_G_F	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACB_B_F	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACB_RED_C	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACB_GREEN_C	NOTE:37.50hm Impedance	20MIL_G2G_30MIL
DACB_BLUE_C	NOTE:37.50hm Impedance	20MIL_G2G_30MIL

1

15

5

1

12

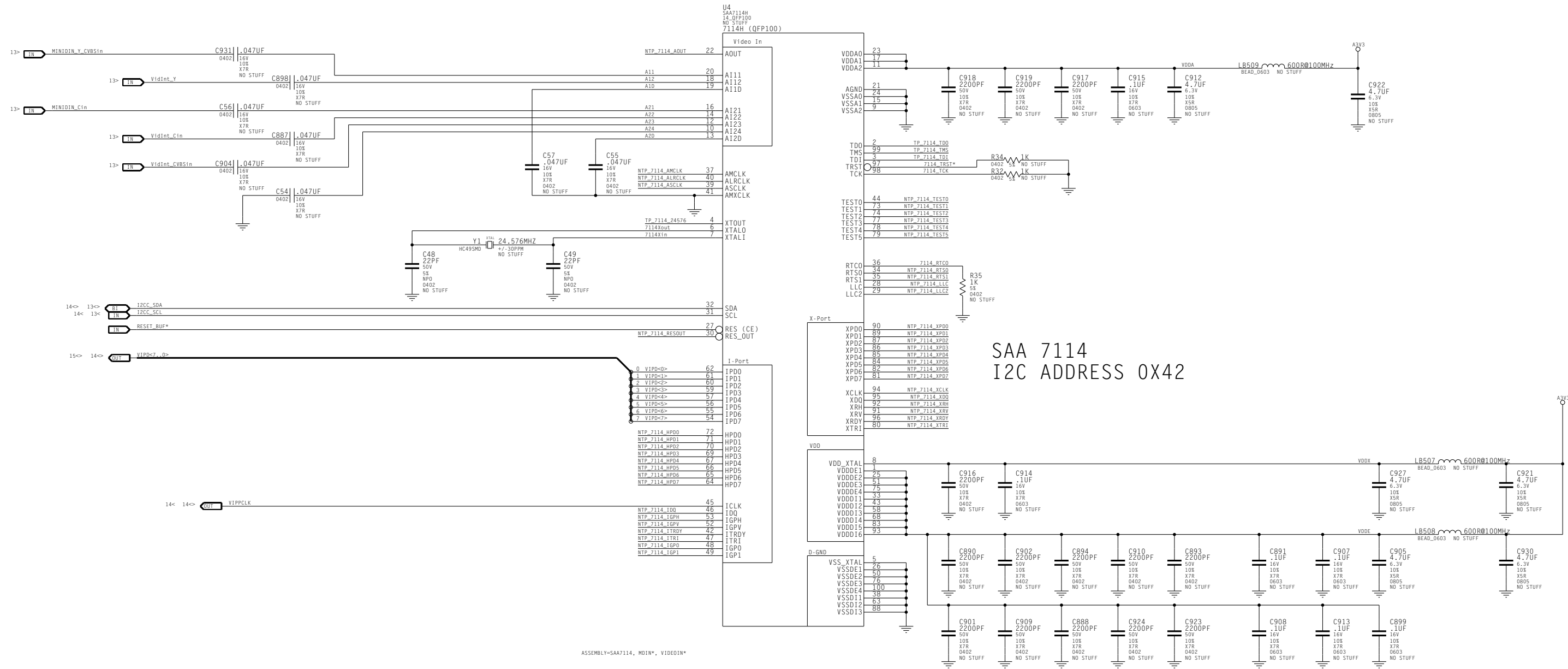
3

45

ID	design	PAGE	18 OF 27
NAME		DATE	19-JAN-2004

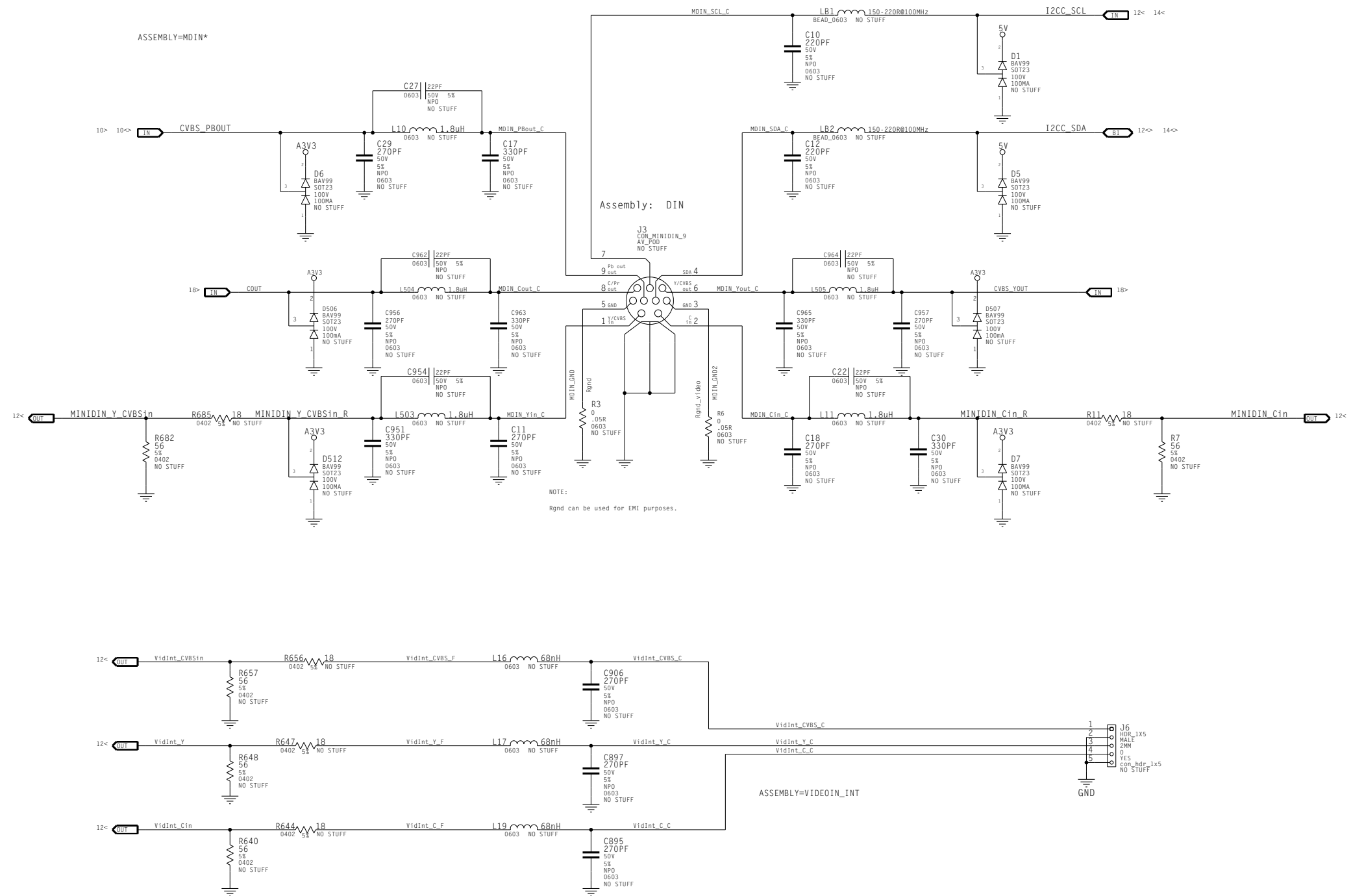
[illegible]

19. Video Capture



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

20. MiniDIN, 9 Pin, Video IN/OUT Connector



ASSEMBLY	NV35 Value Board. 128 MB DVI-I, VGA)
PAGE DETAIL	Video In/Out Connector External with Stereo Out (MiniDin)

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

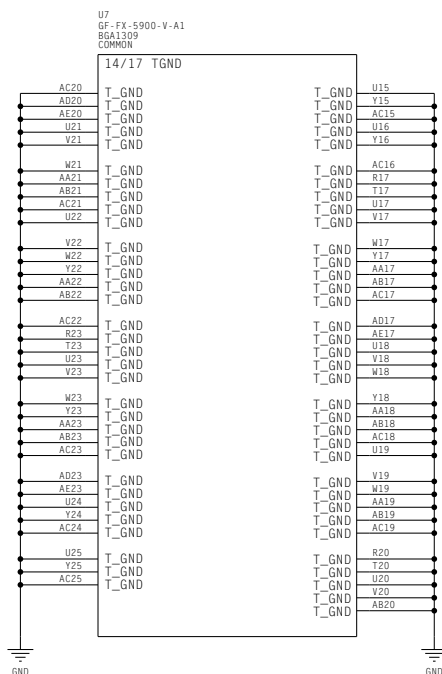
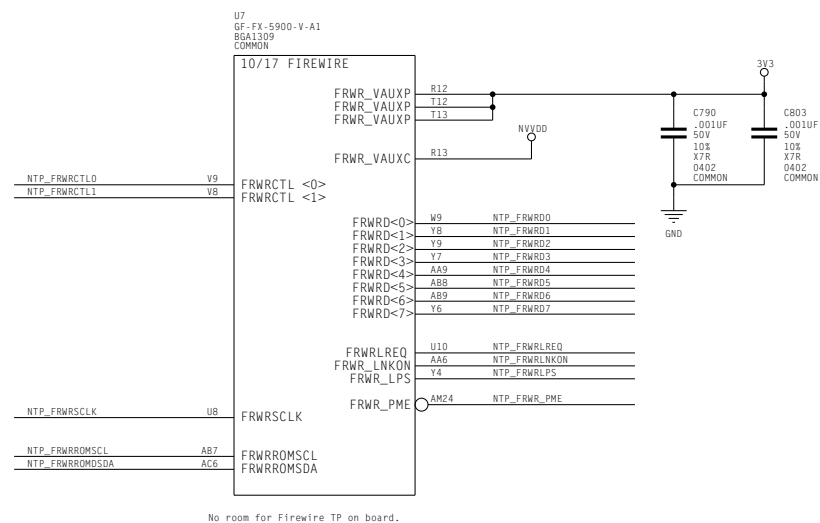
SANTA CLARA, CA 95050, USA

NV_PN	600-50173-0000-000
-------	--------------------

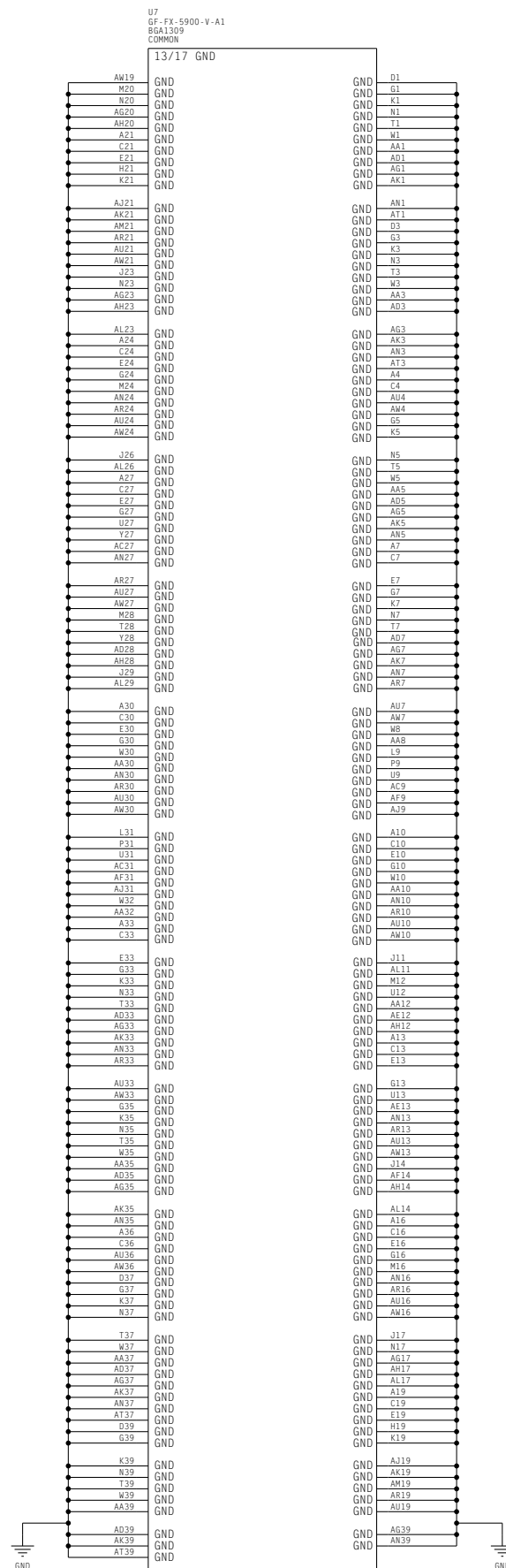
ID	design	PAGE	20 OF 27
NAME		DATE	19-JAN-2004




21. GND, Thermal GND and Misc...



U7		
GF-FX-5900-V-A1		
BGA1309		
COMMON		
		11/17 NC
NTP_NC_1	AV3	NC_01
NTP_NC_2	AM2	NC_02
NTP_NC_3	AV4	NC_03
NTP_NC_4	AU5	NC_04
NTP_NC_5	AV5	NC_05
NTP_NC_6	AD9	NC_06
NTP_NC_7	V11	NC_07
NTP_NC_8	AE11	NC_08
NTP_NC_9	AF12	NC_09
NTP_NC_10	AG13	NC_10
NTP_NC_11	AV13	NC_11
NTP_NC_12	AG14	NC_12
NTP_NC_13	AV14	NC_13
NTP_NC_14	AV15	NC_14
NTP_NC_15	AT16	NC_15
NTP_NC_16	AV17	NC_16
NTP_NC_17	AV17	NC_17
NTP_NC_18	AJ18	NC_18
NTP_NC_19	AJ22	NC_19



NET RULES		
	NET	PHYSICAL
IN	D102CALPD_VDDQ	12MIL_TRACE
IN	D102CALPU_GND	12MIL_TRACE

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-50173-0000-000		
ID	design	DATE	21 0F 27
NAME		DATE	19-JAN-2004

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

1

2

312345

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.



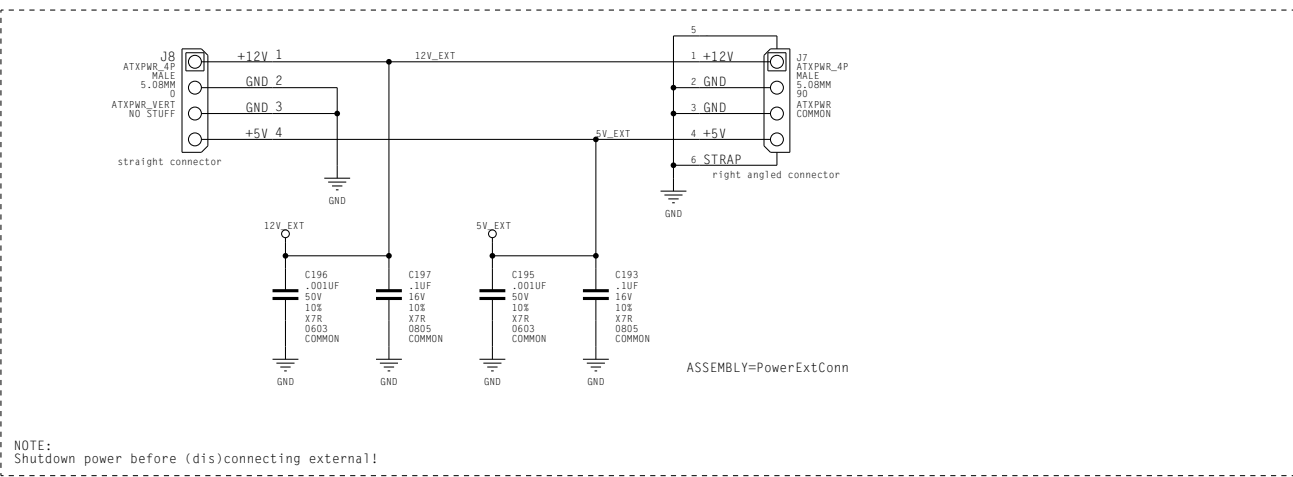
NV_PN	600-50173-0000-000
-------	--------------------

ID	design	PAGE	22 OF 27
NAME		DATE	19-JAN-2004

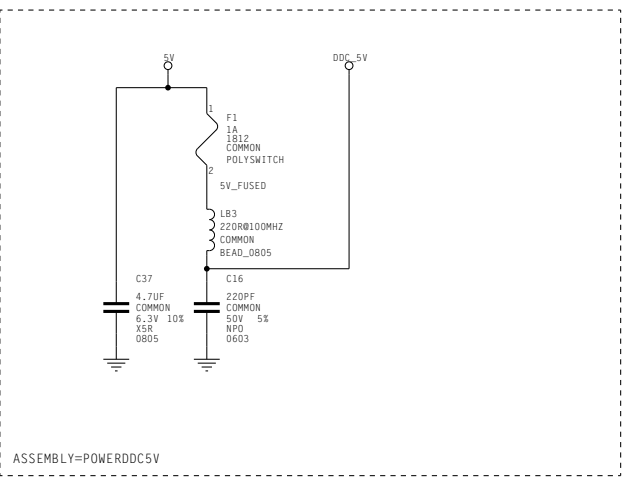
ID	design	PAGE	22 OF 27
NAME		DATE	19-JAN-2004

23. EXT POWER CONNECTION AND DETECTION

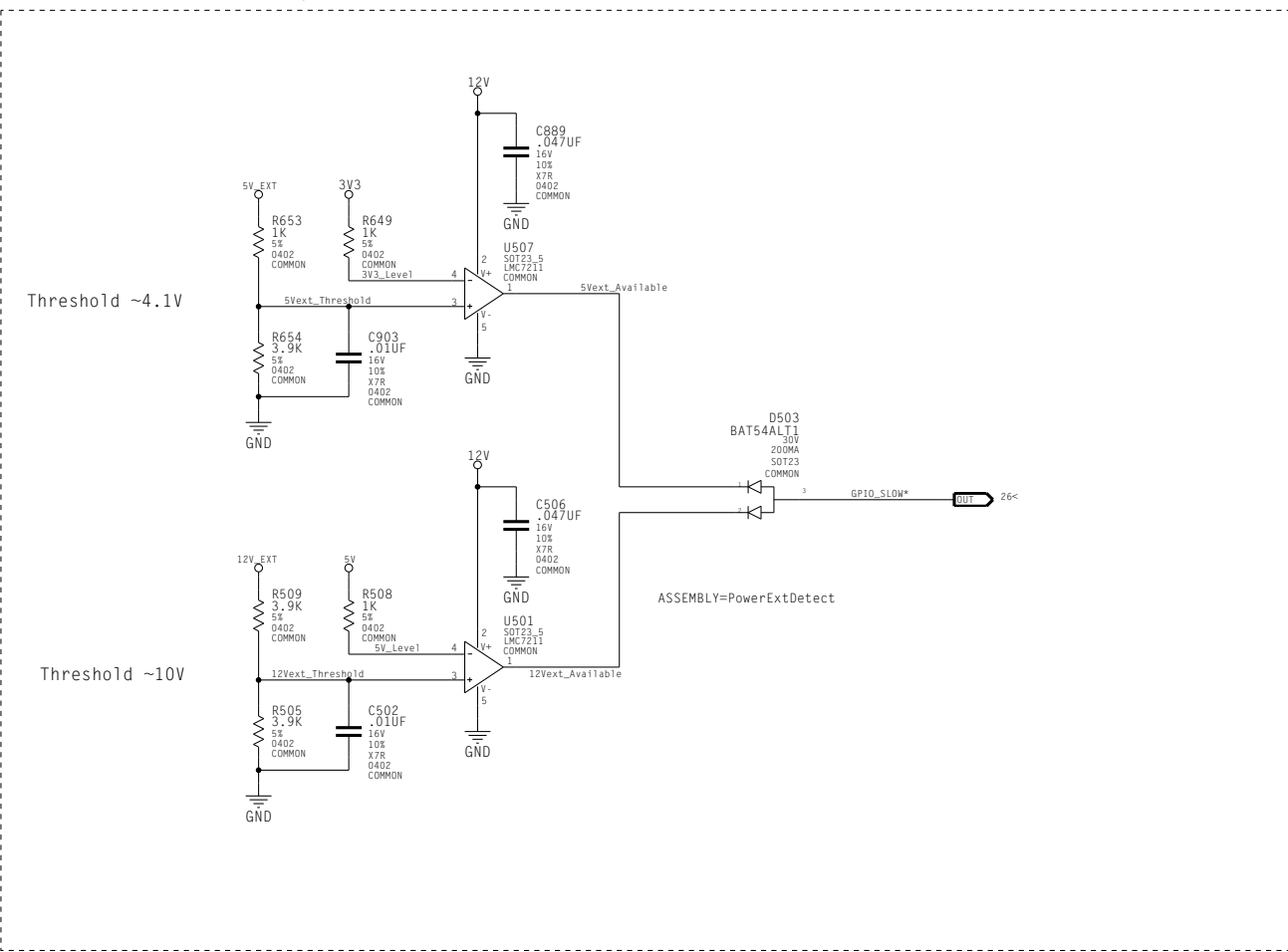
EXTERNAL 5.25 DEVICE CONNECTOR



DDC 5V



EXTERNAL Power detection signals



NET RULES

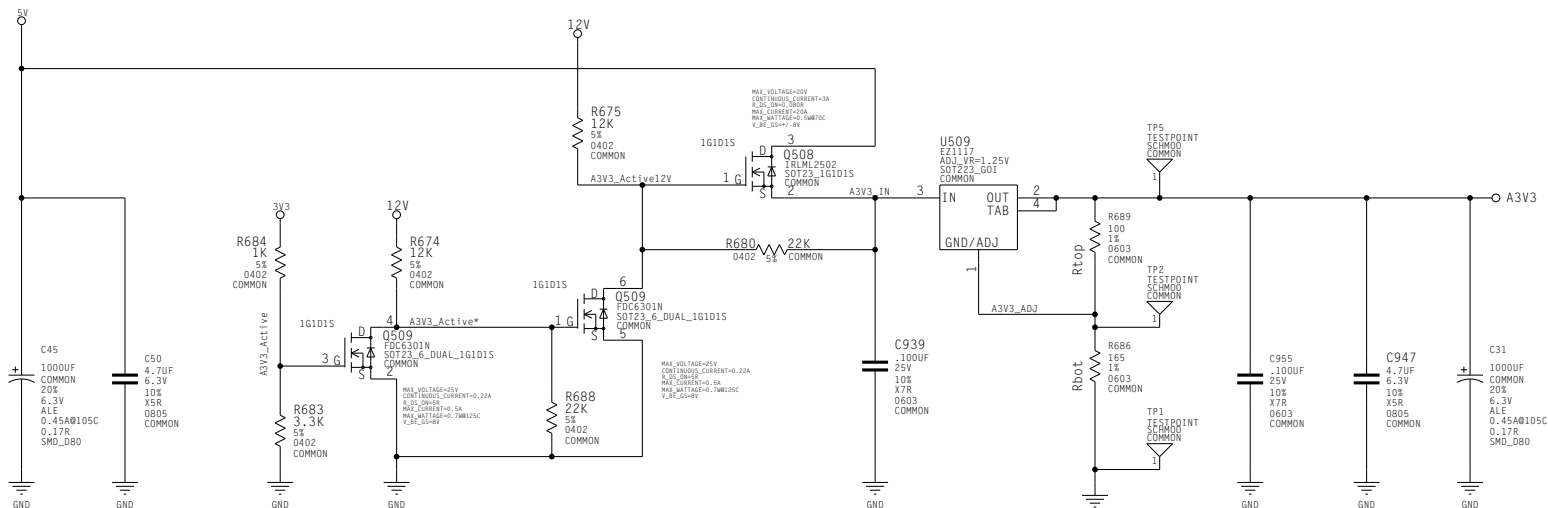
NET	PHYSICAL	VOLTAGE
5V_EXT	5V_EXT	5V
12V_EXT	12V_EXT	12V
5V_EXT and 12V_EXT need to be 220mil internal and 72 mil external		
B1	12V_EXT_D	12MIL_TRACE
B1	12V_EXT_R	12MIL_TRACE
B1	5V_EXT_R	12MIL_TRACE
B1	ENABLE_12V_EXT*	12MIL_TRACE 12V
B1	ENABLE_5V_EXT*	12MIL_TRACE 5V
B1	EXTSENSE	8MIL_TRACE
B1	DDC_5V	DDC_5V 12MIL_TRACE 5V
B1	5V_FUSED	5V_FUSED 12MIL_TRACE 5V

24. Power Supply I: Analog 3V3

NET RULES

	NET	PHYSICAL	VOLTAGE
A3V3	A3V3	12MIL_TRACE	3.3V
	5V10B5	12MIL_TRACE	5V
	10B5_ADJ	10MIL_TRACE	3.3V

A3V3 Supply



$$V_{out} = V_{Ref} * (1 + R_{bot}/R_{top})$$
$$3.31V = 1.25V * (1 + (165/100))$$

ASSEMBLY=A3V3_REG*

1



3




5

1

3



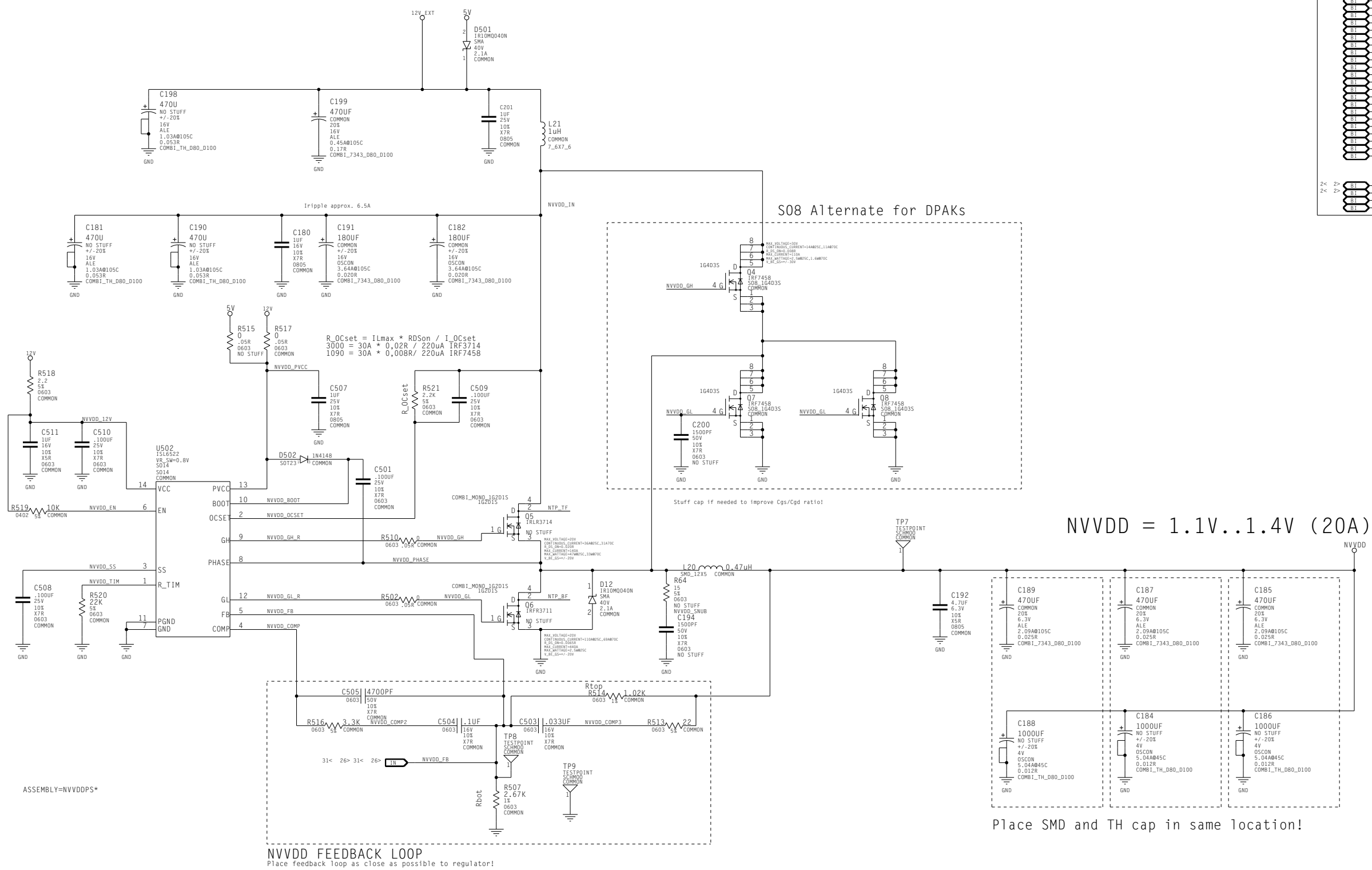
5

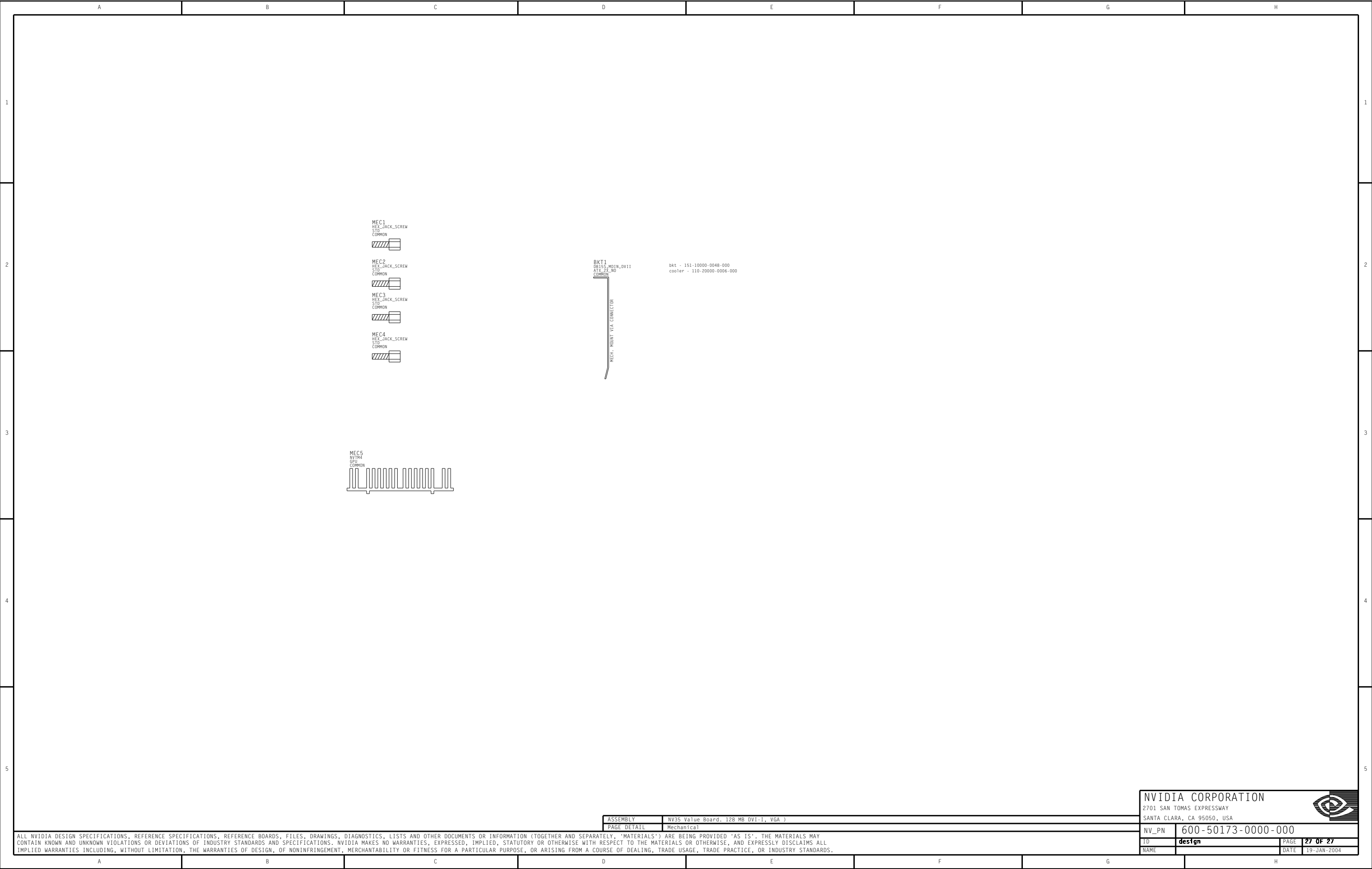
NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-50173-0000-000		
ID	design	PAGE	25 OF 27
NAME		DATE	19-JAN-2004

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

26. Power Supply IV: NVVDD

ISL 6522 S014 switching with 400kHz






ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA



NV_PN	600-50173-0000-000		
ID	design	PAGE	27 OF 27
NAME		DATE	19-JAN-2004