

PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI
Tall DVI-I + DP + DP + DP/HDMI + DP

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Note:

1	page:4-11 修改net name,加<>
2	page:8 增加跨頁符號
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4	page:16/17/19 修改DP footprint
5	page:18 修改HDMI footprint
6	page:26/27 修改output choke footprint



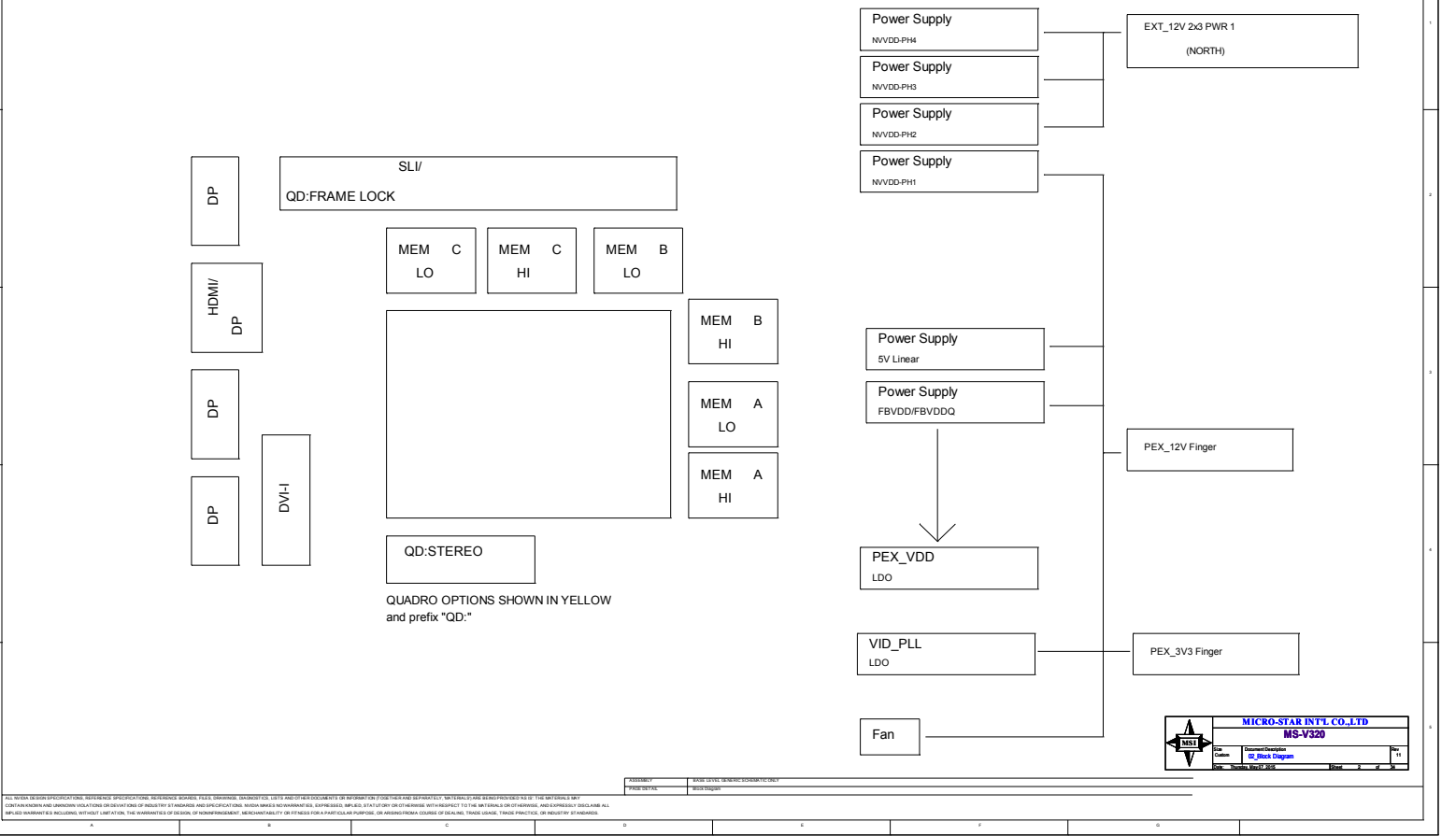
MICRO-STAR INT'L CO., LTD

MS-V320

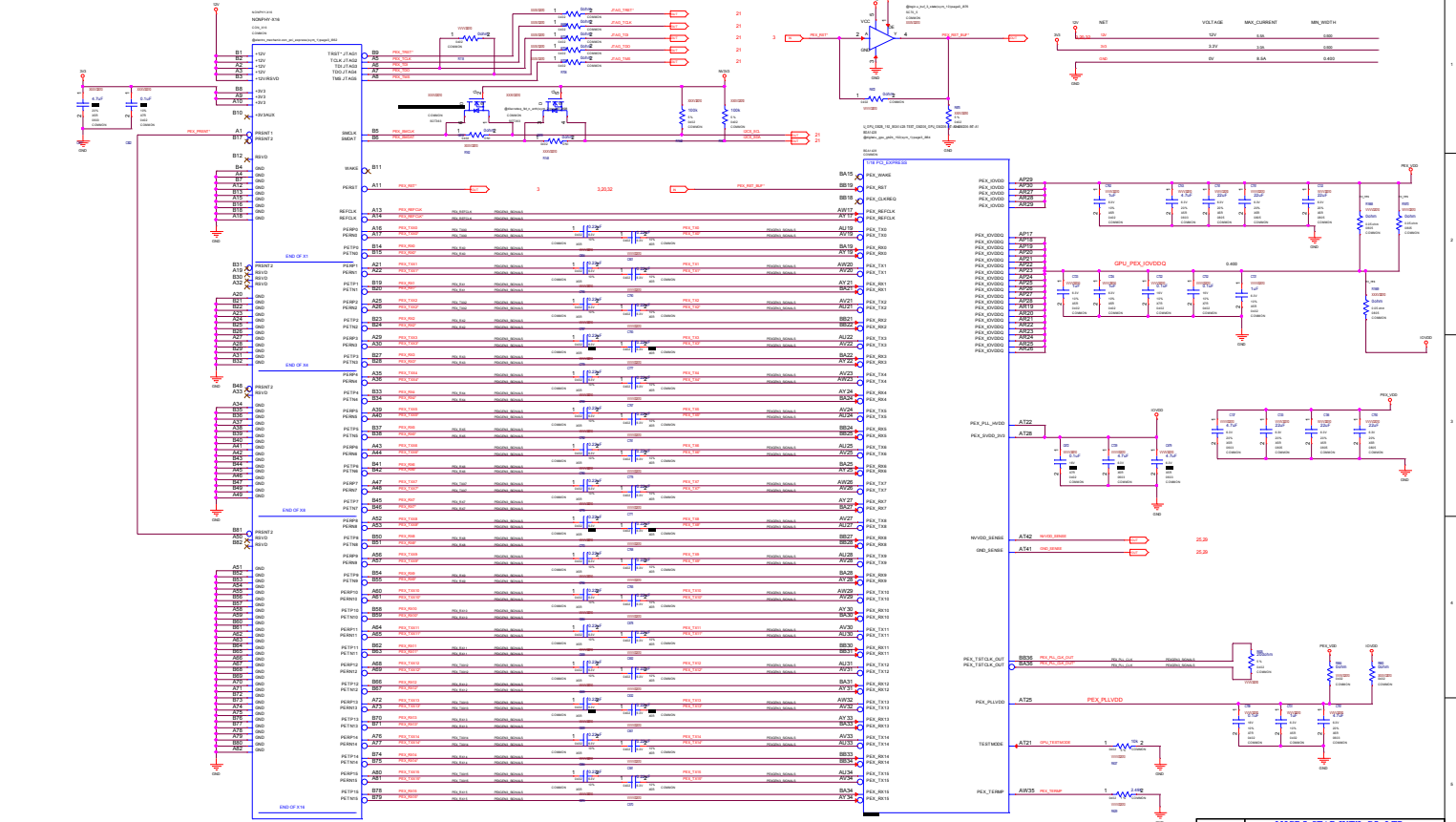
Doc Name	Micro-Star International	Doc No	
Doc Title	PG Table of Contents	Doc Rev	1.1
Doc Ver	Rev1.0, Rev1.1, Rev1.2, Rev1.3	Doc Date	2014.04.01

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Block Diagram




PCI Express



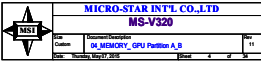
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ASSEMBLY
PCB DETAIL
PLOT SIGNATURE

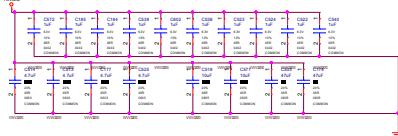
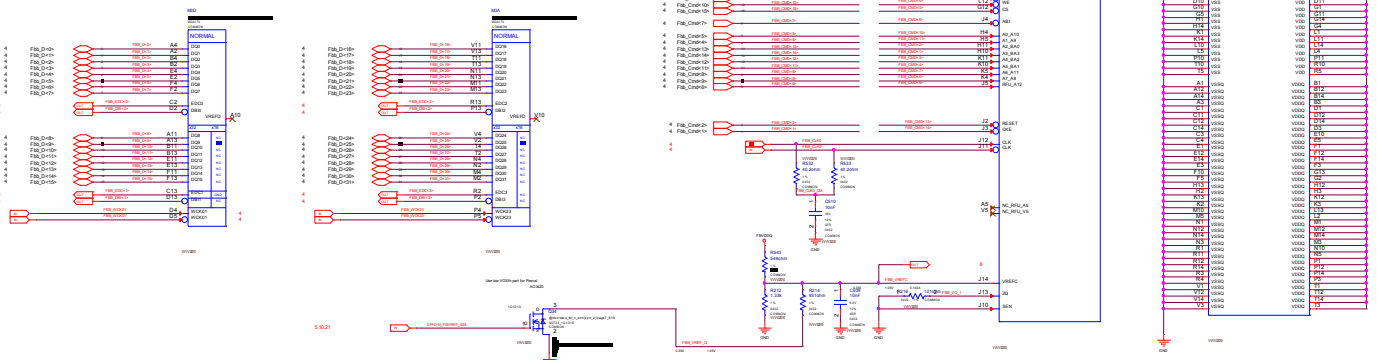


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Doc No.	MS-V320-001
Rev.	1.0
Date	2023/08/01
By	PCB Design
Check	PCB Design
Appr.	PCB Design



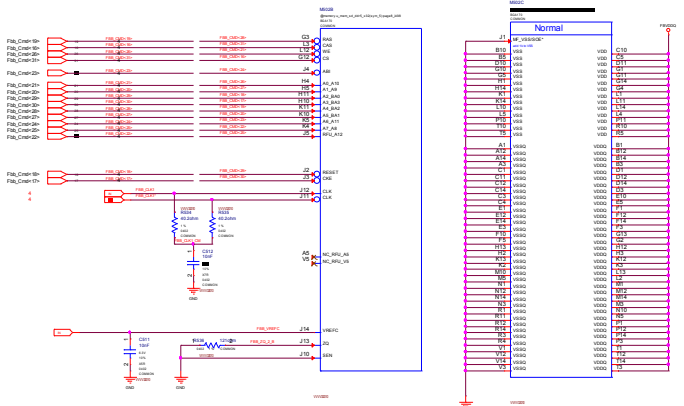
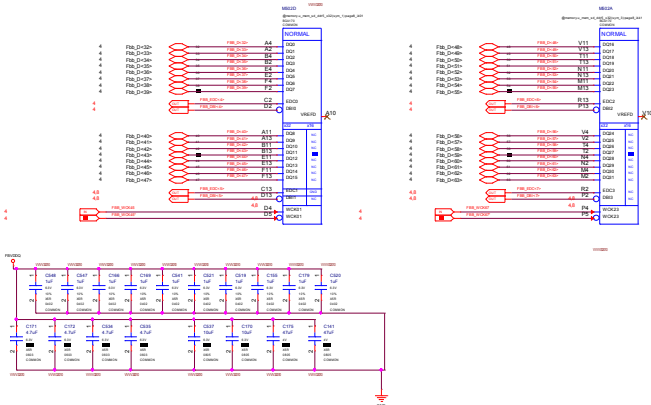




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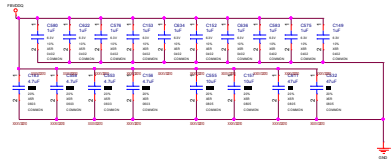
MICRO-STAR INT'L CO., LTD
MS-V320
Rev: 1.0
Date: 2023.10.20
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Check: 01_MEMORY_FBB_P_31
Draw: 01_MEMORY_FBB_P_31
Scale: 1:1

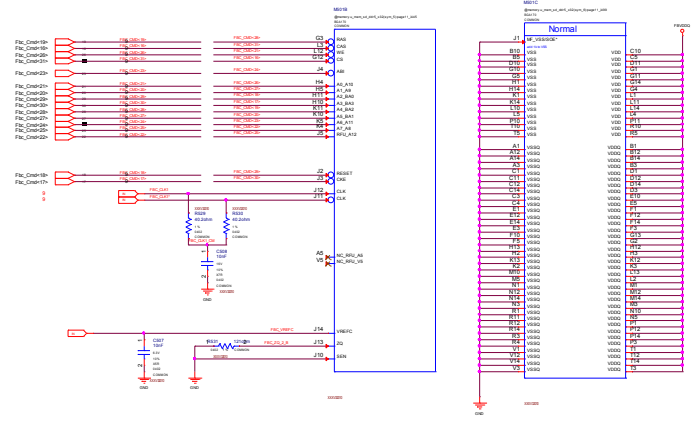
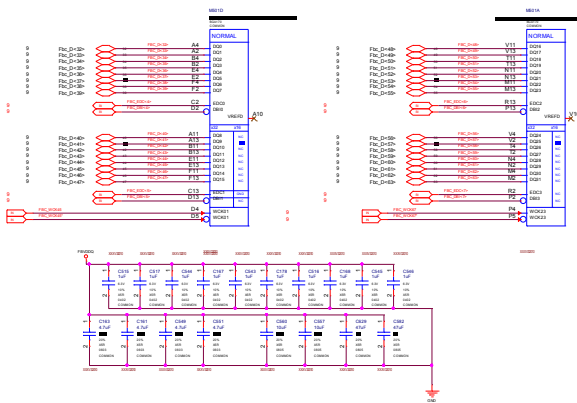


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MS-V320
Product Description
Memory Partition 63..32
Date: 2023-10-10
Ver: 1.0

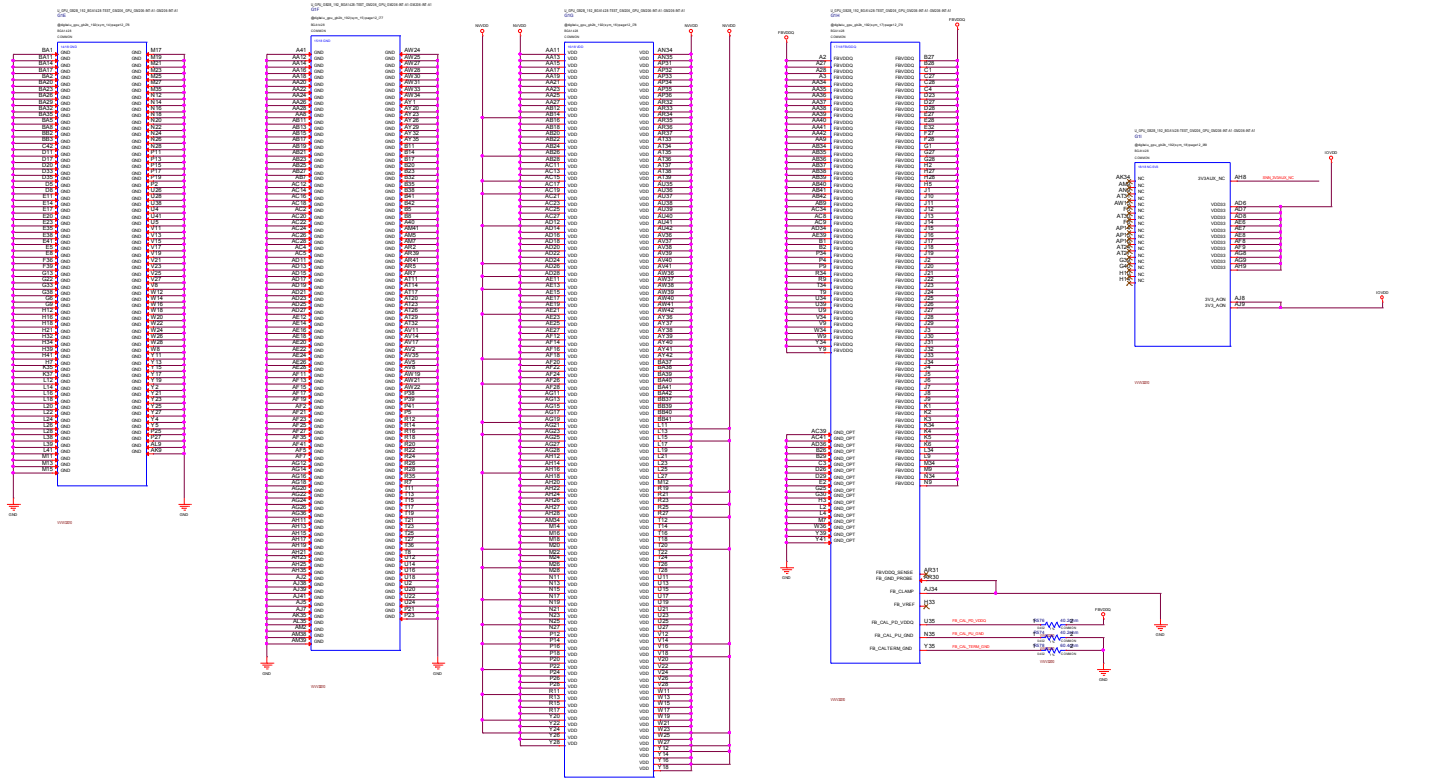




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GPU PWR and GND

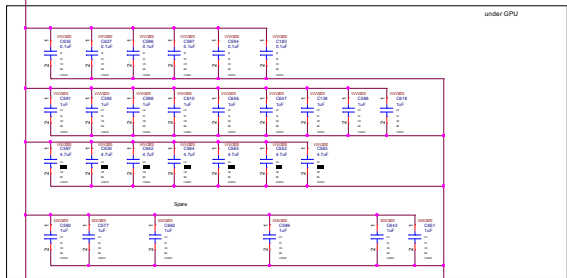


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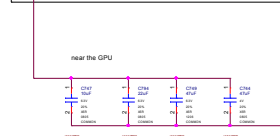
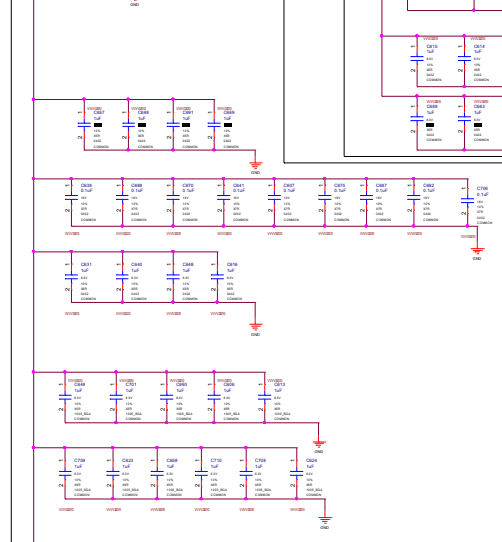
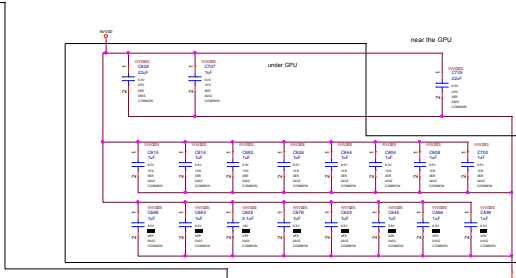
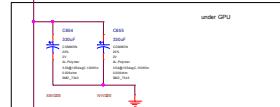
MICRO-STAR INT'L CO., LTD	
MS-V320	
Rev	Document Description
001	12 GPU PWR and GND
Rev	001

GPU Decoupling

FBVDDQ



NVDD



	Under GPU	Near GPU
NVDD	90uF + 1x 330uF	80uF
SVDD	33uF	22uF
Combined (Microell)	122uF + 1x 330uF	110uF

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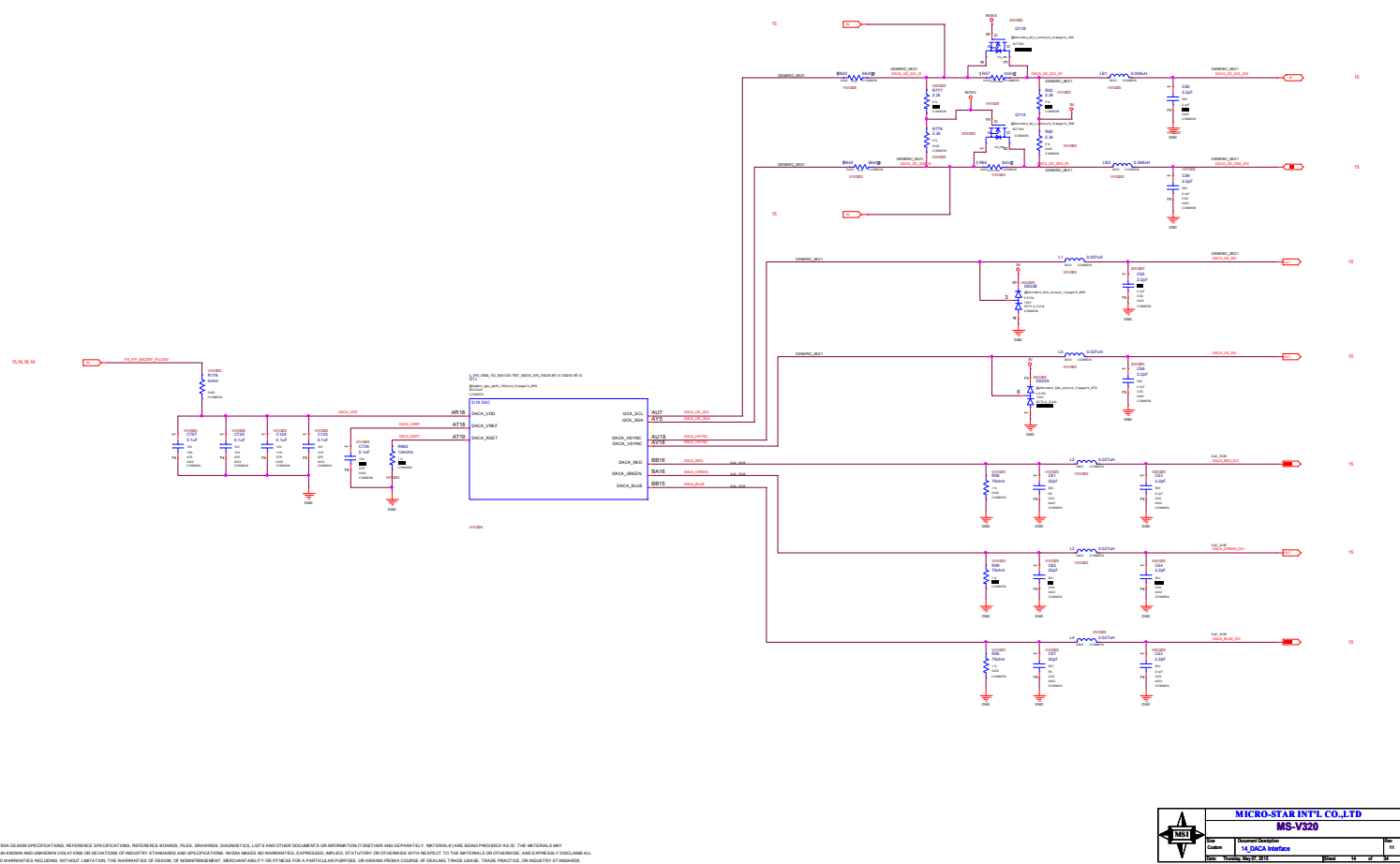
ASSEMBLY
PAGE 01/01

BASE LEVEL SCHEMATIC ONLY
GPU Decoupling



MICRO-STAR INT'L CO., LTD.	
MS-V320	
Doc. Name	Decoupling
Doc. Version	1.0 GPU Decoupling
Doc. Number	MS-V320-1.0

DACA Interface

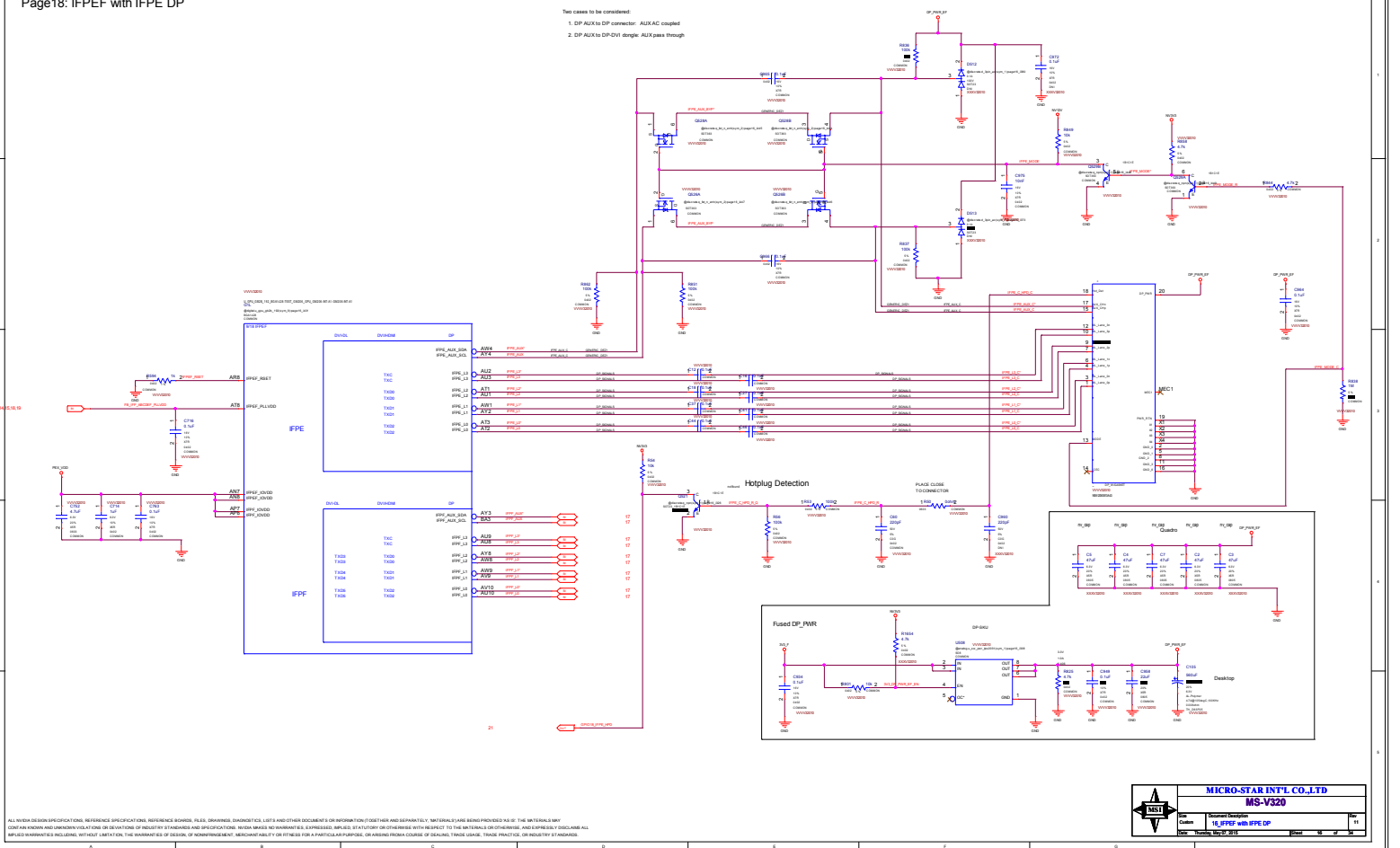


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	MICRO-STAR INT'L CO.,LTD		
	MS-V320		
	Item Custom	Description 14_DACA Interface	Qty 11
Date: Thursday, May 27, 2015			



Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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MICRO-STAR INT'L CO., LTD
MS-V320
Product Name: **IFPEF with IFPE DP**
Version: **1.0**
Date: **2023.07.18**





1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through





	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
1	WGA_VREF	3.3V		0.200
2	WGA_GN_PU_VREF	3.3V		0.200
3	WGA_GN_PU_VREF	3.3V		0.200

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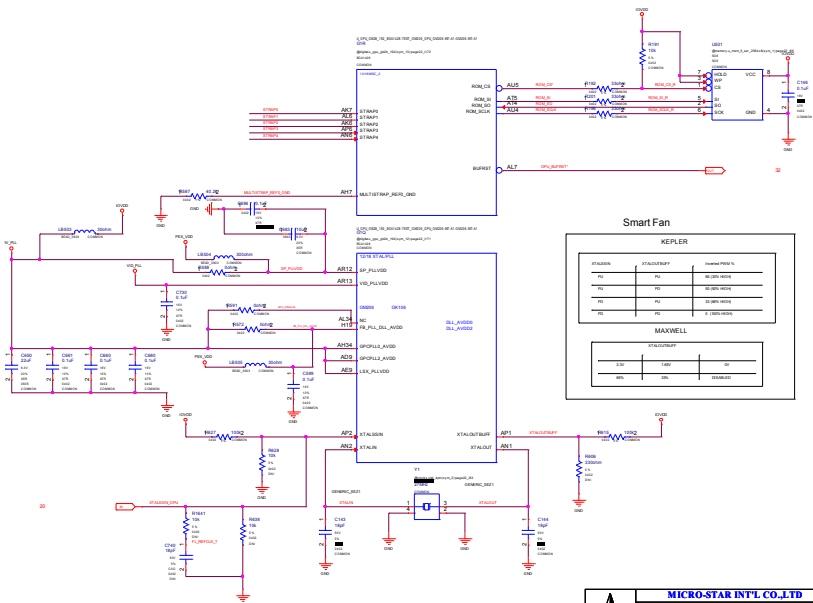
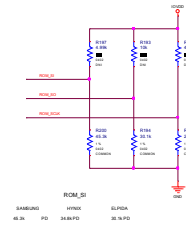
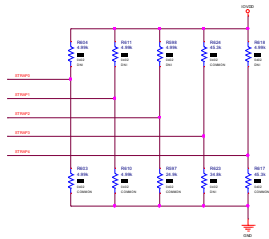


MISC2: ROM, XTAL, Straps

KEPLER		MAXWELL	
STRAP0	USER_BIT [3:0]'		
STRAP1	3G0_PRCFG3_LUT_ADDR'		
STRAP2	PC0_DEVID [3:0]'		
STRAP3	SOR0_EXPOSED [3:0]'		
STRAP4	DP_PLL_VCO_DIV'		
	PEX_MAX_SPEED'		
	PEX_SPD_CHANGE_GEN'		
	'		
ROM_S1	RAMCFG0[0]'	RAMCFG0[0]'	
	RAMCFG1[1]'	RAMCFG1[1]'	
	RAMCFG2[2]'	RAMCFG2[2]'	
ROM_S0	VGA_DEVICE'	VGA_DEVICE'	
	SMB_ALT_ADDR'	SMB_ALT_ADDR'	
	FB[0]_APERTURE_SIZE'	PC0_CFG'	
ROM_SCLK	FB[1]_APERTURE_SIZE'	DEV0_SEL'	
	PEX_PLL_PL_TERMIN02'	SOR0_EXPOSED'	
	PC0_DEVID_EXT[5]'	SOR1_EXPOSED'	
	SUB_VENDOR'	SOR2_EXPOSED'	
	PC0_DEVID_EXT[4]'	SOR3_EXPOSED'	

MULTI STRAP_0401_0402	
BOOT_PRESERVE	NO
BOOT_PRESERVE	NO
BOOT_PRESERVE	NO

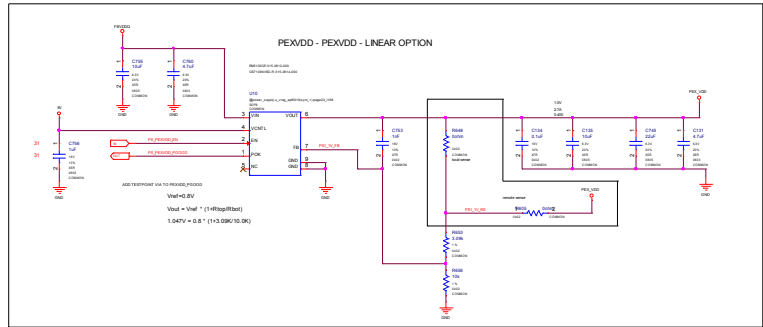
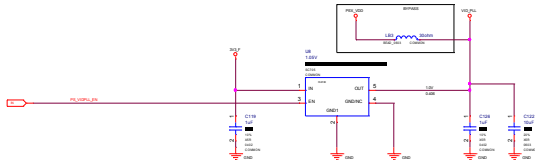
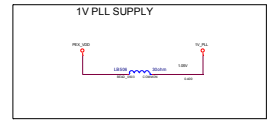
STRAP0	
0x00	0x00
0x01	0x01
0x02	0x02



Smart Fan	
KEPLER	MAXWELL
PC0	PC0
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PC2	PC2
PC3	PC3
PC4	PC4
PC5	PC5
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PC8	PC8
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MICRO-STAR INT'L CO., LTD	
MS-V320	
Model	MS-V320
Rev	1.0

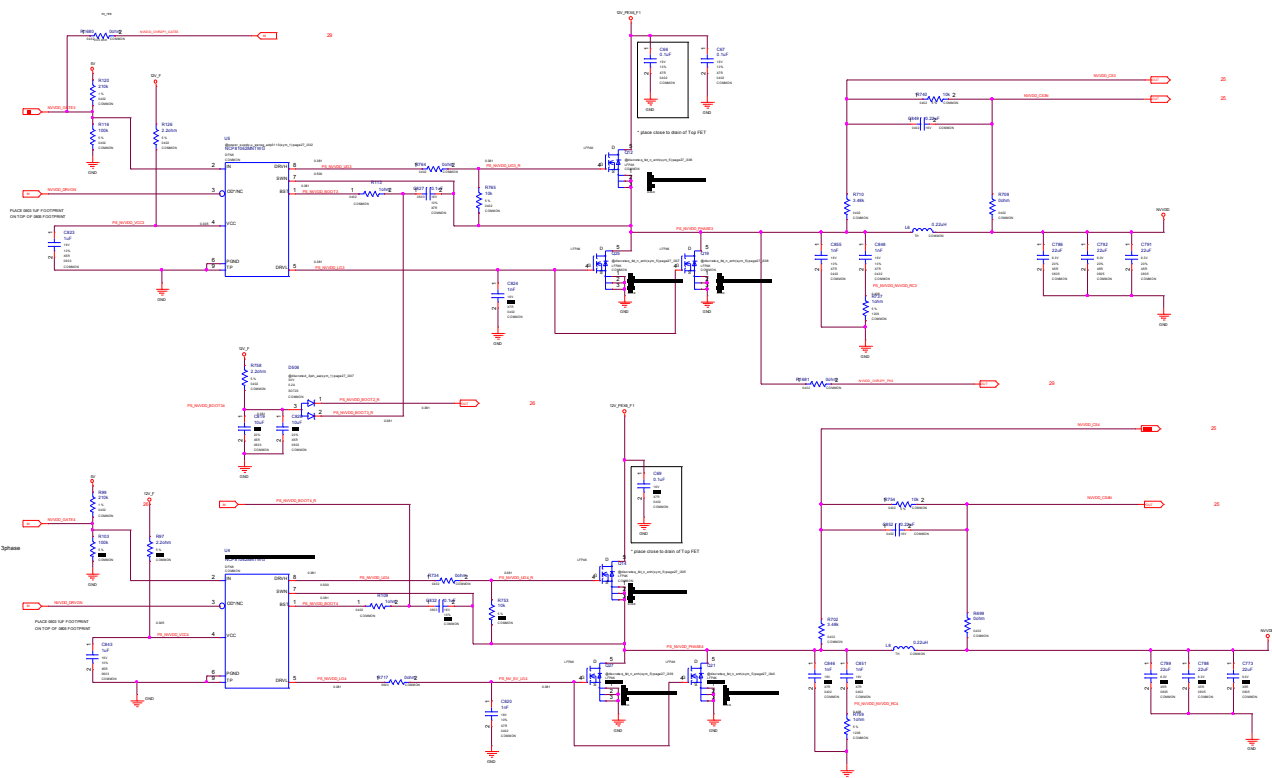
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MS-V320	
Doc	27_PS_NVVDD Phase 3,4
Rev	Rev. 01

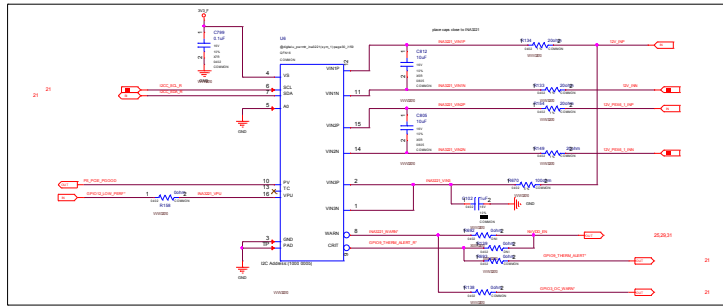
[RESERVED]

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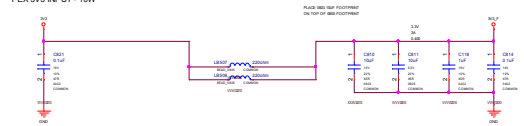
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MS-V320	
DATE	2024/08/01
BY	MS-V320
REV	01



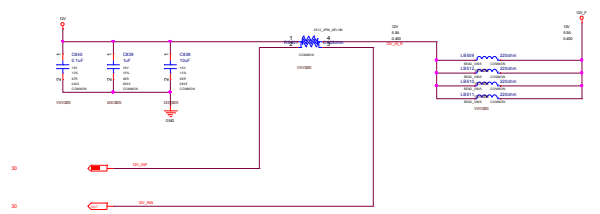
PS: Inputs, Filtering, and Monitoring



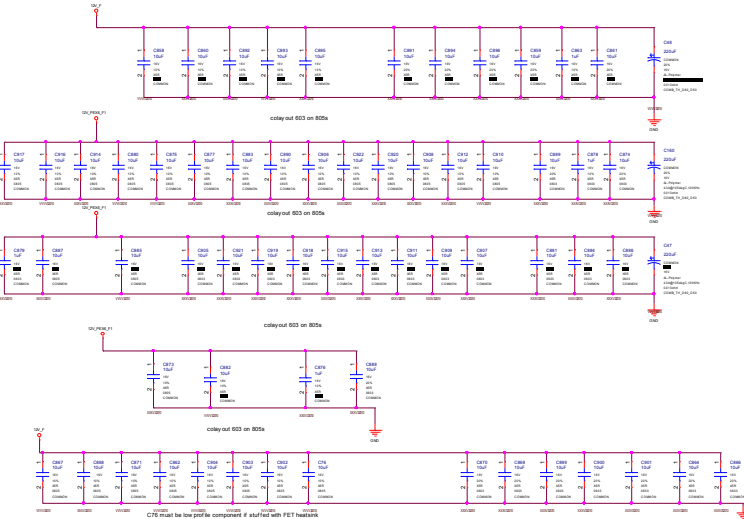
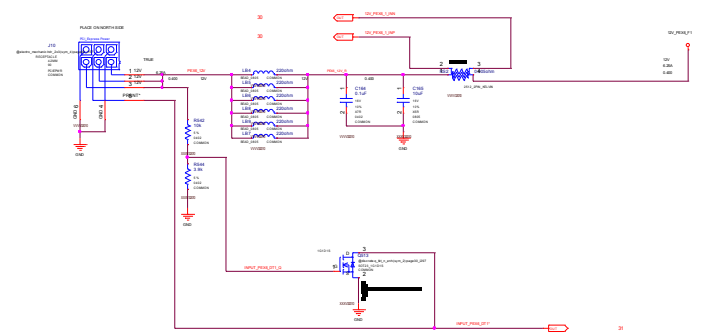
PEX.3V3 INPUT - 10W



PEX_12V INPUT - 66W

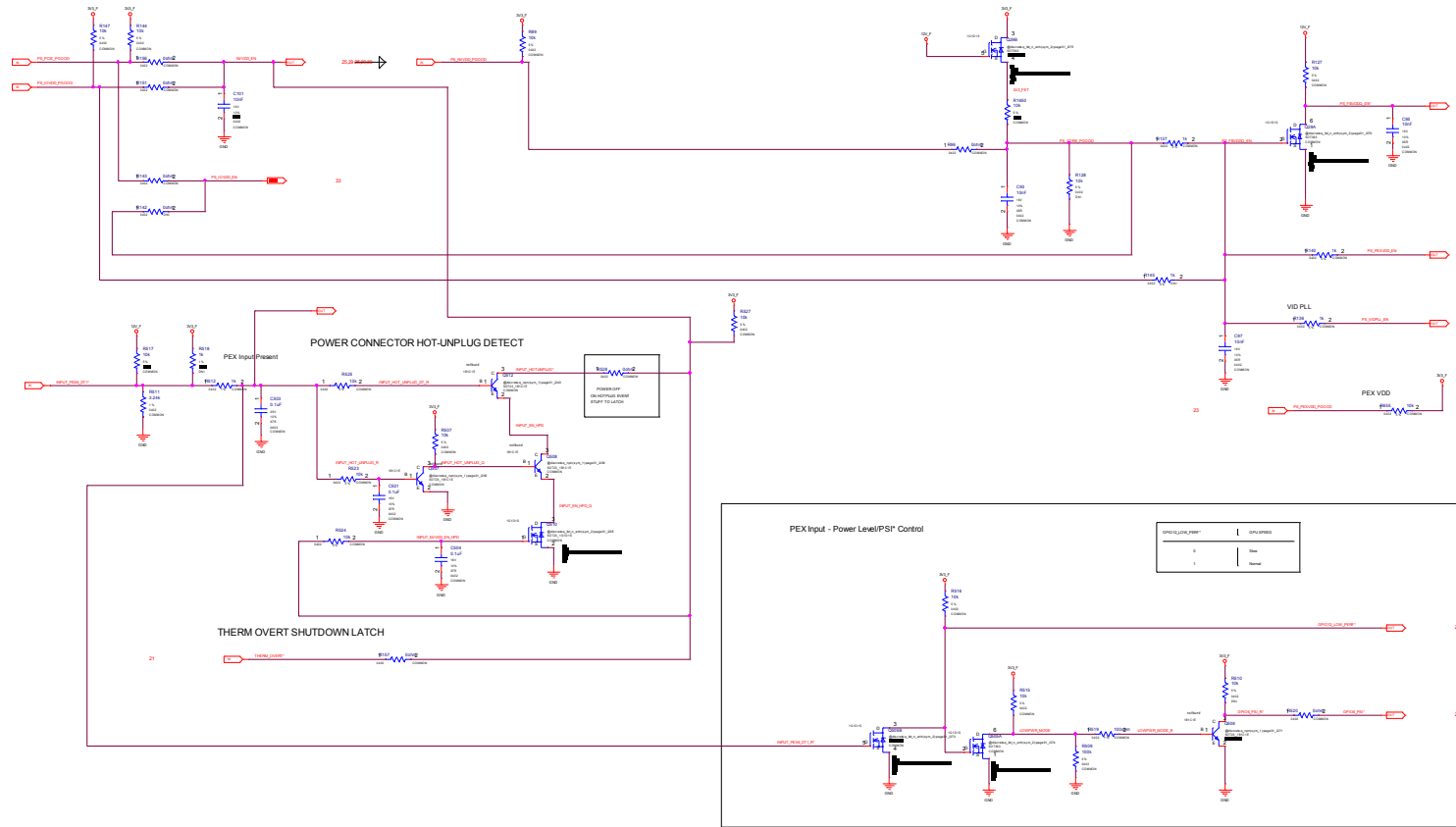


PEX6 INPUT - 2x3 PCIe CON 75W



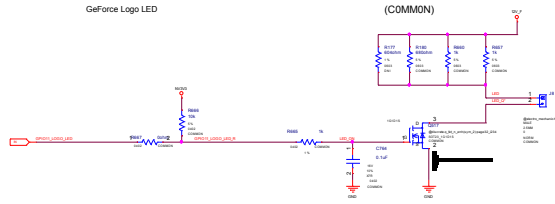
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PS: Sequence and Shutdown

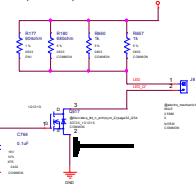


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GeForce Logo LED

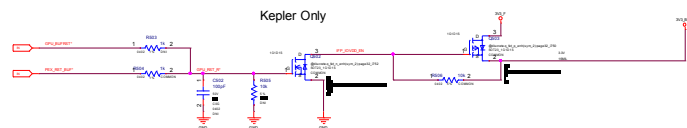


LED HEADER (COMMON)



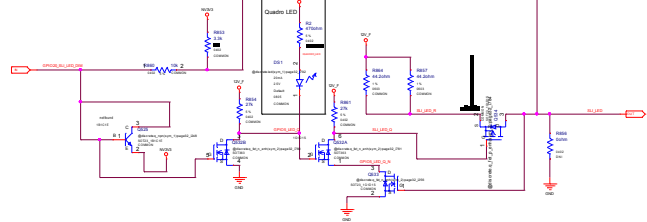
IFP_IOVDD (backdrive prevention)

Kepler Only

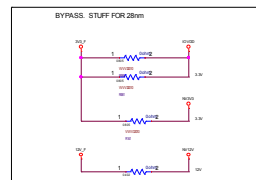
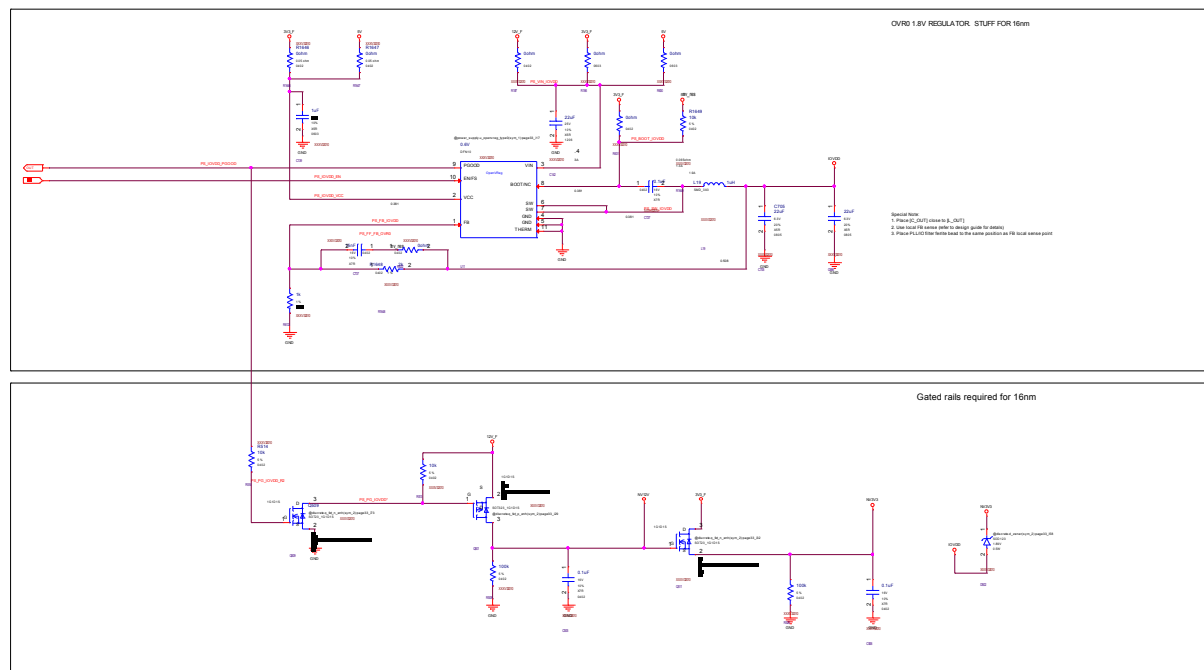


SLI LED

and Quadro LED



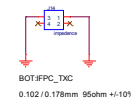
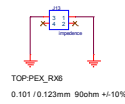
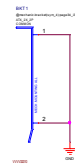
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