V064-0A G73 7600GS DDR2

base on 8988 modify, for G73 chip
remove DDR dram
add DDR2 dram
add RT9218 for FBVDDQ

PAGE SUMMARY:

8981 Ver : 00A modify P229-B01 Summary

Page 11. Add Video in connect to mini-din 10 pin & remove J5.

Page 12. Add DVI-I common choke.

Page 13. Connect net MIOBD 2 , MIOBD 6 & MIOBD 7 to BUS.

Page 15. Modify Power ,PWM change to ISL6549.

Page 16. Add Video function.

8988 Ver : 00A modify 8981-100 Summary

Page 02. Delete PCI-E connector

Page 15. Change 5V power supply to BR02VDD & Add sequence

Page 17,18,19,20. Add BR02 bradge circuit

8988 Ver : 00A BOM

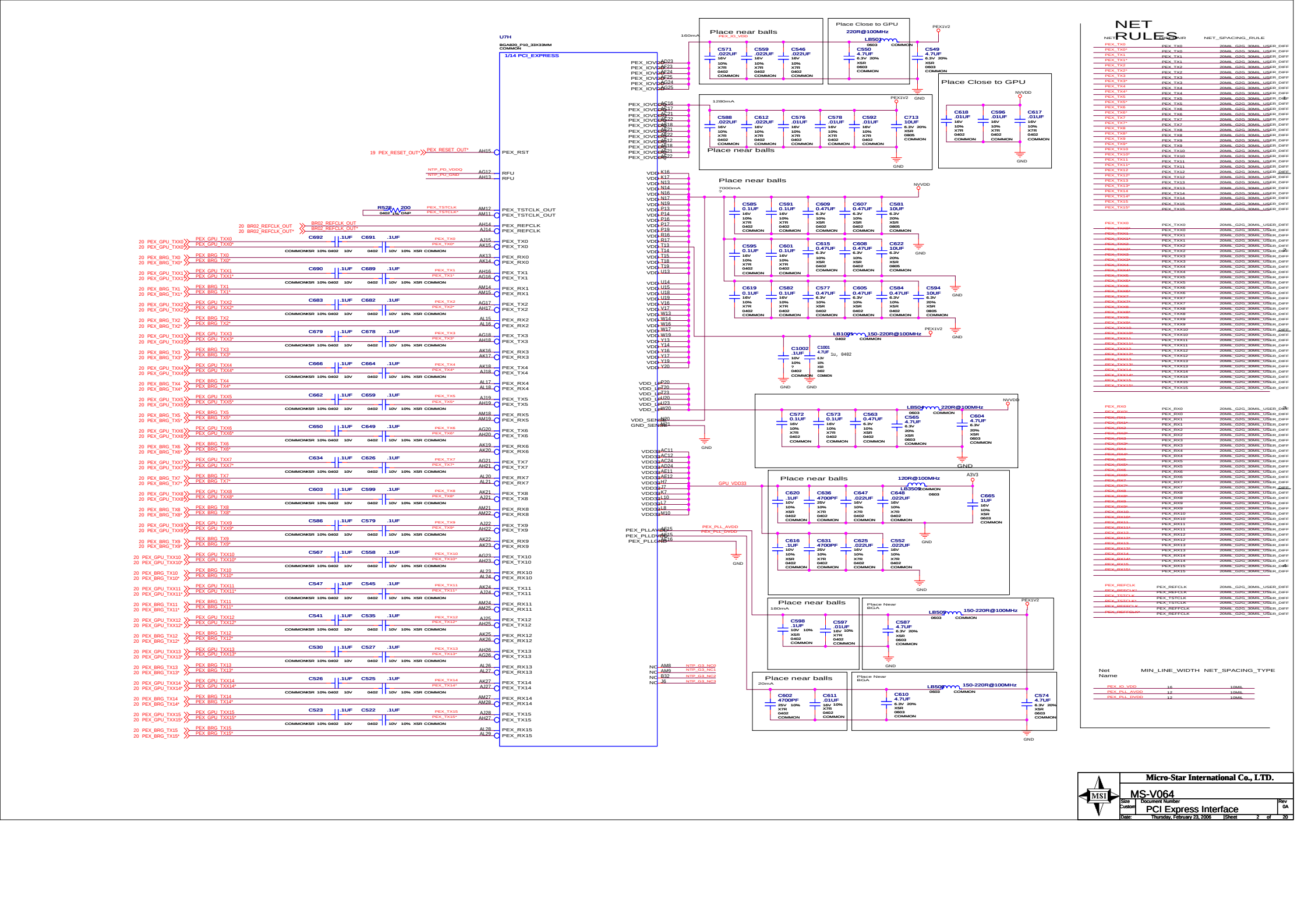
SKU000:MSI 602-8988-A10 MS-8988 00A NV43/VGA/DVI-I/VHT-10/256M DDR (Hynix 16*16-4)

SKU001:MSI 602-8988-A20 MS-8988 00A OPT:A NV43/VGA/DVI-I/VHT-10/128M DDR(Samsung 8*16-3.6)

REVISION HISTORY:

X1 Initial Release

sku	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10229-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
1	nv43dvivgatv128m16x	600-10229-0002-101	P229-B01 NV43 GEN DVI-I/VGA/S-VIDEO 128MB
2	nv43dvivgatv128m8x	600-10229-0003-101	P229-B01 NV43 GEN DVI-I/VGA/HDTV 128MB 8Mx16
3	43gldvivgatv128m8x	600-50229-0001-101	P229-B01 NV43-GL GEN DVI-I/VGA/HDTV 128MB
4	nv43dvivgatv256m16x	600-10229-0004-101	P229-B01 NV43 GEN DVI-I/VGA/HDTV 256MB 16Mx16
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>



NET RULES

NET	CLASS	NET_SPACING_RULE
PEX_TX0	PEX_TX0	20MIL_G2G_30MIL_USER_DIFF
PEX_TX0*	PEX_TX0	20MIL_G2G_30MIL_USER_DIFF
PEX_TX1	PEX_TX1	20MIL_G2G_30MIL_USER_DIFF
PEX_TX1*	PEX_TX1	20MIL_G2G_30MIL_USER_DIFF
PEX_TX2	PEX_TX2	20MIL_G2G_30MIL_USER_DIFF
PEX_TX2*	PEX_TX2	20MIL_G2G_30MIL_USER_DIFF
PEX_TX3	PEX_TX3	20MIL_G2G_30MIL_USER_DIFF
PEX_TX3*	PEX_TX3	20MIL_G2G_30MIL_USER_DIFF
PEX_TX4	PEX_TX4	20MIL_G2G_30MIL_USER_DIFF
PEX_TX4*	PEX_TX4	20MIL_G2G_30MIL_USER_DIFF
PEX_TX5	PEX_TX5	20MIL_G2G_30MIL_USER_DIFF
PEX_TX5*	PEX_TX5	20MIL_G2G_30MIL_USER_DIFF
PEX_TX6	PEX_TX6	20MIL_G2G_30MIL_USER_DIFF
PEX_TX6*	PEX_TX6	20MIL_G2G_30MIL_USER_DIFF
PEX_TX7	PEX_TX7	20MIL_G2G_30MIL_USER_DIFF
PEX_TX7*	PEX_TX7	20MIL_G2G_30MIL_USER_DIFF
PEX_TX8	PEX_TX8	20MIL_G2G_30MIL_USER_DIFF
PEX_TX8*	PEX_TX8	20MIL_G2G_30MIL_USER_DIFF
PEX_TX9	PEX_TX9	20MIL_G2G_30MIL_USER_DIFF
PEX_TX9*	PEX_TX9	20MIL_G2G_30MIL_USER_DIFF
PEX_TX10	PEX_TX10	20MIL_G2G_30MIL_USER_DIFF
PEX_TX10*	PEX_TX10	20MIL_G2G_30MIL_USER_DIFF
PEX_TX11	PEX_TX11	20MIL_G2G_30MIL_USER_DIFF
PEX_TX11*	PEX_TX11	20MIL_G2G_30MIL_USER_DIFF
PEX_TX12	PEX_TX12	20MIL_G2G_30MIL_USER_DIFF
PEX_TX12*	PEX_TX12	20MIL_G2G_30MIL_USER_DIFF
PEX_TX13	PEX_TX13	20MIL_G2G_30MIL_USER_DIFF
PEX_TX13*	PEX_TX13	20MIL_G2G_30MIL_USER_DIFF
PEX_TX14	PEX_TX14	20MIL_G2G_30MIL_USER_DIFF
PEX_TX14*	PEX_TX14	20MIL_G2G_30MIL_USER_DIFF
PEX_TX15	PEX_TX15	20MIL_G2G_30MIL_USER_DIFF
PEX_TX15*	PEX_TX15	20MIL_G2G_30MIL_USER_DIFF

NET	CLASS	NET_SPACING_RULE
PEX_TX0	PEX_TX0	20MIL_G2G_30MIL_USER_DIFF
PEX_TX0*	PEX_TX0	20MIL_G2G_30MIL_USER_DIFF
PEX_TX1	PEX_TX1	20MIL_G2G_30MIL_USER_DIFF
PEX_TX1*	PEX_TX1	20MIL_G2G_30MIL_USER_DIFF
PEX_TX2	PEX_TX2	20MIL_G2G_30MIL_USER_DIFF
PEX_TX2*	PEX_TX2	20MIL_G2G_30MIL_USER_DIFF
PEX_TX3	PEX_TX3	20MIL_G2G_30MIL_USER_DIFF
PEX_TX3*	PEX_TX3	20MIL_G2G_30MIL_USER_DIFF
PEX_TX4	PEX_TX4	20MIL_G2G_30MIL_USER_DIFF
PEX_TX4*	PEX_TX4	20MIL_G2G_30MIL_USER_DIFF
PEX_TX5	PEX_TX5	20MIL_G2G_30MIL_USER_DIFF
PEX_TX5*	PEX_TX5	20MIL_G2G_30MIL_USER_DIFF
PEX_TX6	PEX_TX6	20MIL_G2G_30MIL_USER_DIFF
PEX_TX6*	PEX_TX6	20MIL_G2G_30MIL_USER_DIFF
PEX_TX7	PEX_TX7	20MIL_G2G_30MIL_USER_DIFF
PEX_TX7*	PEX_TX7	20MIL_G2G_30MIL_USER_DIFF
PEX_TX8	PEX_TX8	20MIL_G2G_30MIL_USER_DIFF
PEX_TX8*	PEX_TX8	20MIL_G2G_30MIL_USER_DIFF
PEX_TX9	PEX_TX9	20MIL_G2G_30MIL_USER_DIFF
PEX_TX9*	PEX_TX9	20MIL_G2G_30MIL_USER_DIFF
PEX_TX10	PEX_TX10	20MIL_G2G_30MIL_USER_DIFF
PEX_TX10*	PEX_TX10	20MIL_G2G_30MIL_USER_DIFF
PEX_TX11	PEX_TX11	20MIL_G2G_30MIL_USER_DIFF
PEX_TX11*	PEX_TX11	20MIL_G2G_30MIL_USER_DIFF
PEX_TX12	PEX_TX12	20MIL_G2G_30MIL_USER_DIFF
PEX_TX12*	PEX_TX12	20MIL_G2G_30MIL_USER_DIFF
PEX_TX13	PEX_TX13	20MIL_G2G_30MIL_USER_DIFF
PEX_TX13*	PEX_TX13	20MIL_G2G_30MIL_USER_DIFF
PEX_TX14	PEX_TX14	20MIL_G2G_30MIL_USER_DIFF
PEX_TX14*	PEX_TX14	20MIL_G2G_30MIL_USER_DIFF
PEX_TX15	PEX_TX15	20MIL_G2G_30MIL_USER_DIFF
PEX_TX15*	PEX_TX15	20MIL_G2G_30MIL_USER_DIFF

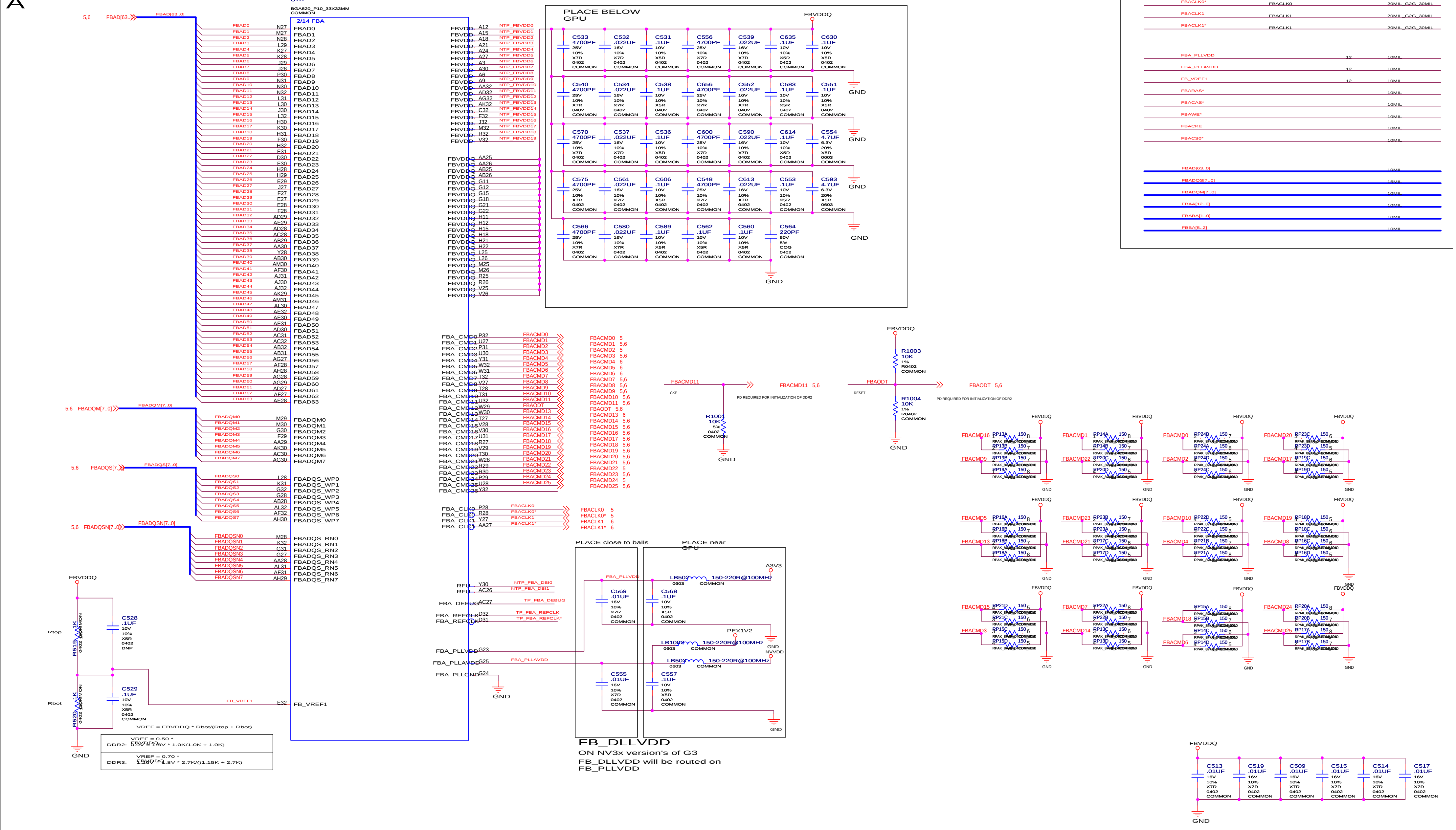
NET	CLASS	NET_SPACING_RULE
PEX_RX0	PEX_RX0	20MIL_G2G_30MIL_USER_DIFF
PEX_RX0*	PEX_RX0	20MIL_G2G_30MIL_USER_DIFF
PEX_RX1	PEX_RX1	20MIL_G2G_30MIL_USER_DIFF
PEX_RX1*	PEX_RX1	20MIL_G2G_30MIL_USER_DIFF
PEX_RX2	PEX_RX2	20MIL_G2G_30MIL_USER_DIFF
PEX_RX2*	PEX_RX2	20MIL_G2G_30MIL_USER_DIFF
PEX_RX3	PEX_RX3	20MIL_G2G_30MIL_USER_DIFF
PEX_RX3*	PEX_RX3	20MIL_G2G_30MIL_USER_DIFF
PEX_RX4	PEX_RX4	20MIL_G2G_30MIL_USER_DIFF
PEX_RX4*	PEX_RX4	20MIL_G2G_30MIL_USER_DIFF
PEX_RX5	PEX_RX5	20MIL_G2G_30MIL_USER_DIFF
PEX_RX5*	PEX_RX5	20MIL_G2G_30MIL_USER_DIFF
PEX_RX6	PEX_RX6	20MIL_G2G_30MIL_USER_DIFF
PEX_RX6*	PEX_RX6	20MIL_G2G_30MIL_USER_DIFF
PEX_RX7	PEX_RX7	20MIL_G2G_30MIL_USER_DIFF
PEX_RX7*	PEX_RX7	20MIL_G2G_30MIL_USER_DIFF
PEX_RX8	PEX_RX8	20MIL_G2G_30MIL_USER_DIFF
PEX_RX8*	PEX_RX8	20MIL_G2G_30MIL_USER_DIFF
PEX_RX9	PEX_RX9	20MIL_G2G_30MIL_USER_DIFF
PEX_RX9*	PEX_RX9	20MIL_G2G_30MIL_USER_DIFF
PEX_RX10	PEX_RX10	20MIL_G2G_30MIL_USER_DIFF
PEX_RX10*	PEX_RX10	20MIL_G2G_30MIL_USER_DIFF
PEX_RX11	PEX_RX11	20MIL_G2G_30MIL_USER_DIFF
PEX_RX11*	PEX_RX11	20MIL_G2G_30MIL_USER_DIFF
PEX_RX12	PEX_RX12	20MIL_G2G_30MIL_USER_DIFF
PEX_RX12*	PEX_RX12	20MIL_G2G_30MIL_USER_DIFF
PEX_RX13	PEX_RX13	20MIL_G2G_30MIL_USER_DIFF
PEX_RX13*	PEX_RX13	20MIL_G2G_30MIL_USER_DIFF
PEX_RX14	PEX_RX14	20MIL_G2G_30MIL_USER_DIFF
PEX_RX14*	PEX_RX14	20MIL_G2G_30MIL_USER_DIFF
PEX_RX15	PEX_RX15	20MIL_G2G_30MIL_USER_DIFF
PEX_RX15*	PEX_RX15	20MIL_G2G_30MIL_USER_DIFF

NET	CLASS	NET_SPACING_RULE
PEX_REFCLK	PEX_REFCLK	20MIL_G2G_30MIL_USER_DIFF
PEX_REFCLK*	PEX_REFCLK	20MIL_G2G_30MIL_USER_DIFF
PEX_TSTCLK	PEX_TSTCLK	20MIL_G2G_30MIL_USER_DIFF
PEX_TSTCLK*	PEX_TSTCLK	20MIL_G2G_30MIL_USER_DIFF
PEX_REFCLK	PEX_REFFCLK	20MIL_G2G_30MIL_USER_DIFF
PEX_REFCLK*	PEX_REFFCLK	20MIL_G2G_30MIL_USER_DIFF

Net Name	MIN_LINE_WIDTH	NET_SPACING_TYPE
PEX_IO_VDD	16	10MIL
PEX_PLL_AVDD	12	10MIL
PEX_PLL_DVDD	12	10MIL

Micro-Star International Co., LTD.		
MS-V064		
Size: Custom	Document Number: PCI Express Interface	Rev: 0A
Date: Thursday, February 23, 2006	Sheet 2 of 20	

FB BANK A



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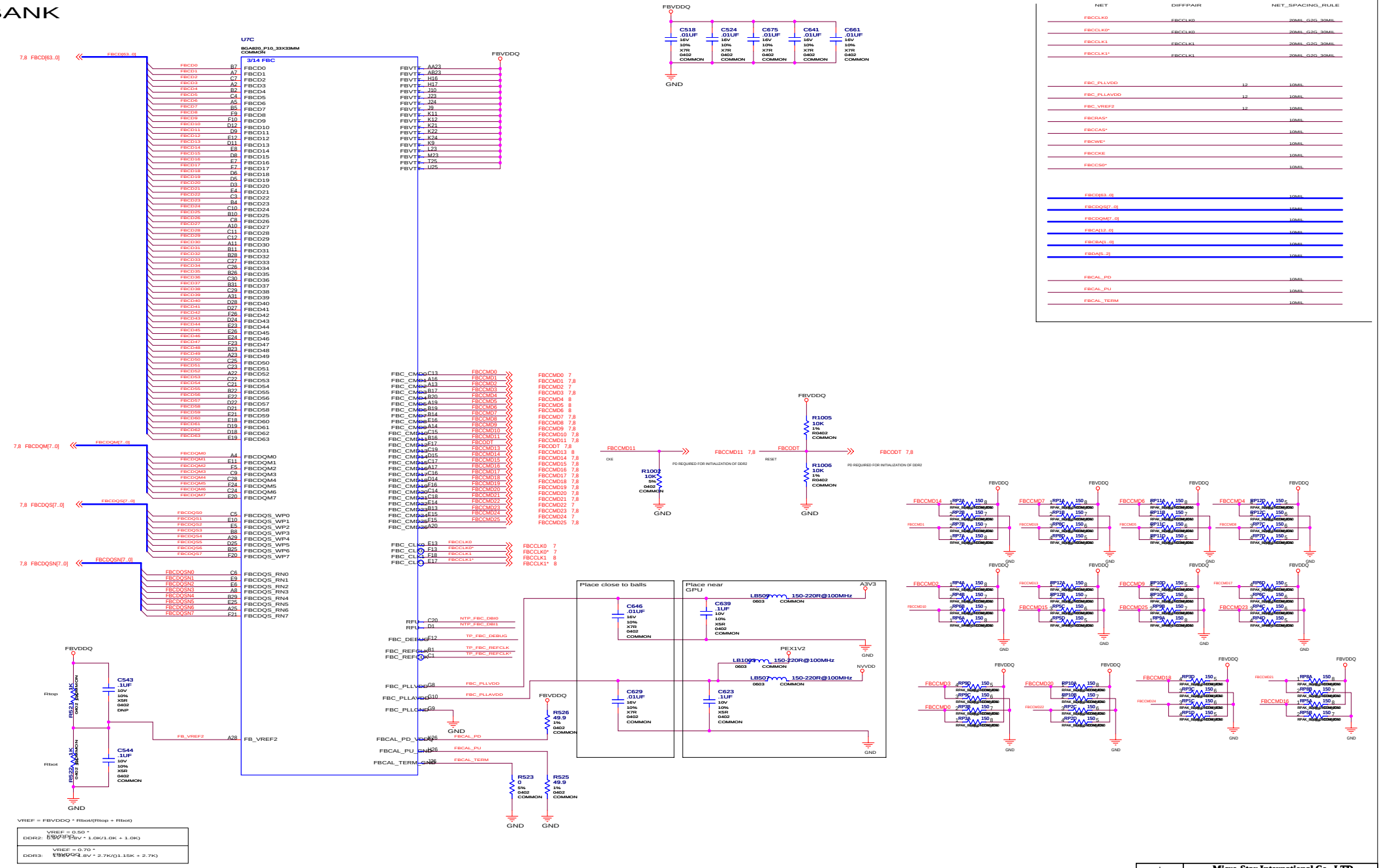
MS-V064			
Size: Custom	Document Number: FB BANK A		Rev: 0A
Date: Monday, March 06, 2006	Sheet 3 of 20		

FB BANK C



NET	DIFFPAIR	NET_SPACING_RULE
FBCCLK0	FBCCLK0	20MIL_G2G_30MIL
FBCCLK0*	FBCCLK0	20MIL_G2G_30MIL
FBCCLK1	FBCCLK1	20MIL_G2G_30MIL
FBCCLK1*	FBCCLK1	20MIL_G2G_30MIL
FBC_PLLVDD	12	10MIL
FBC_PLLAVDD	12	10MIL
FBC_VREF2	12	10MIL
FBCRAS*		10MIL
FBCCAS*		10MIL
FBCWE*		10MIL
FBCCKE		10MIL
FBCCS0*		10MIL
FBCD[63..0]		10MIL
FBCDQS[7..0]		10MIL
FBCDQM[7..0]		10MIL
FBCA[12..0]		10MIL
FBCBA[1..0]		10MIL
FBDA[5..2]		10MIL
FBCAL_PD		10MIL
FBCAL_PU		10MIL
FBCAL_TERM		10MIL

Micro-Star International Co., LTD.	
MS-V064	
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Rev: 0A	
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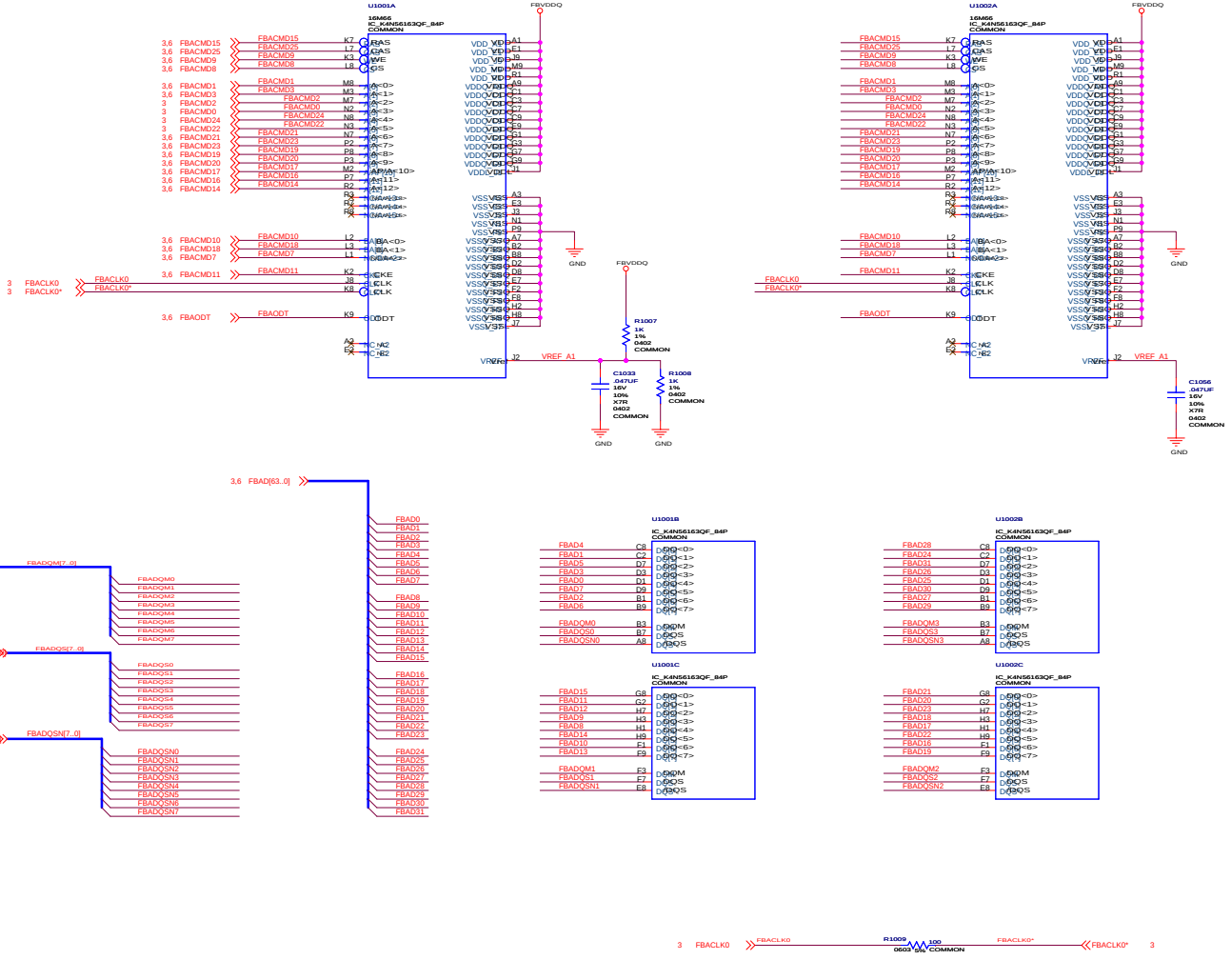
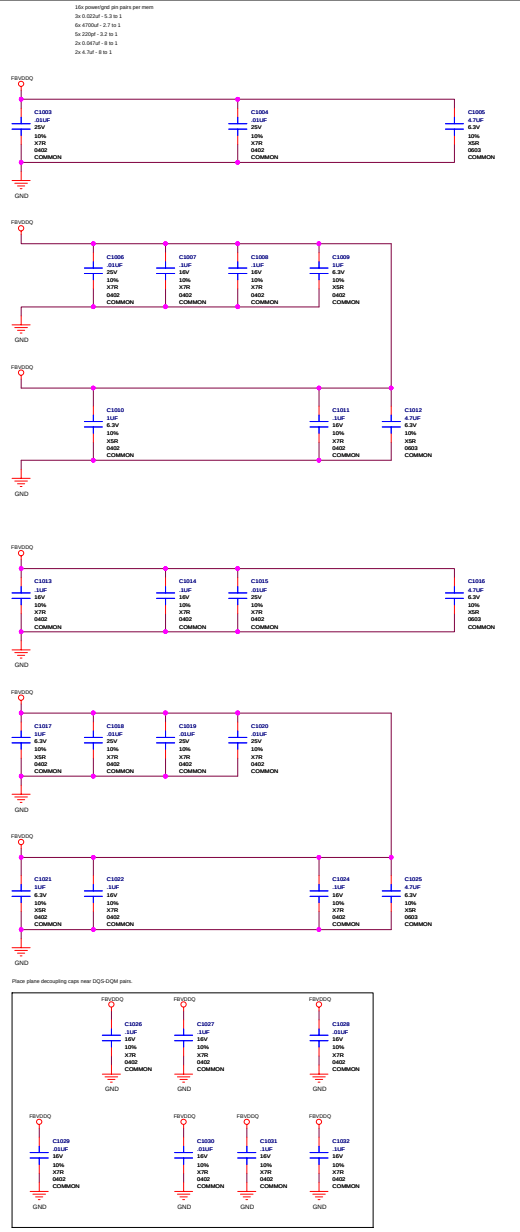
MEMORY 1st bank
0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY





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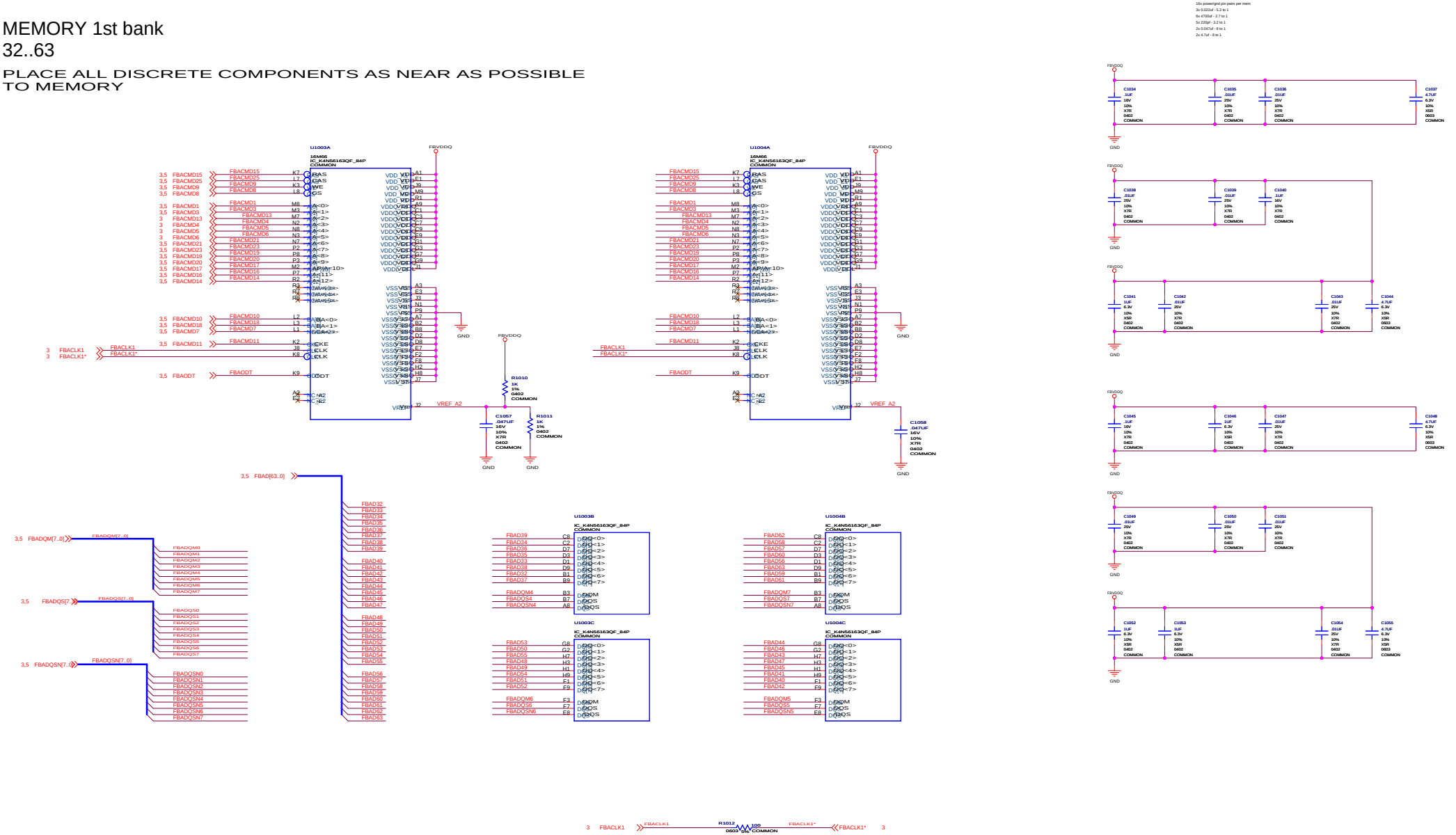
MS-V064		
Size: Custom	Document Number: Memory 1st bank 0..31	Rev: 0A
Date: Tuesday, February 28, 2006	Sheet 5 of 20	

MEMORY 1st bank
32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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MS-V064			
Size: Custom	Document Number: Memory 1st 32..63		Rev: 0A
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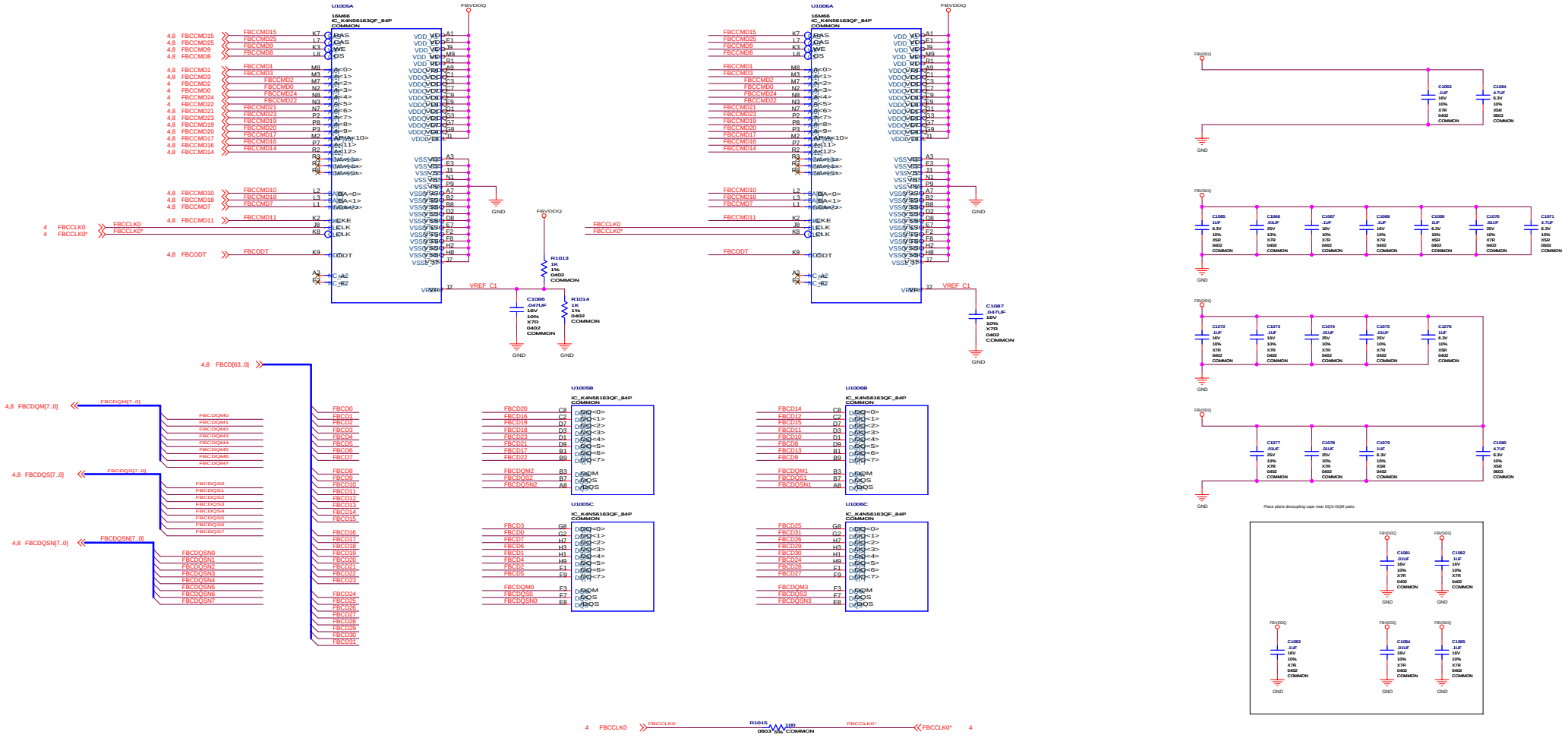
MEMORY 2nd bank
0..31

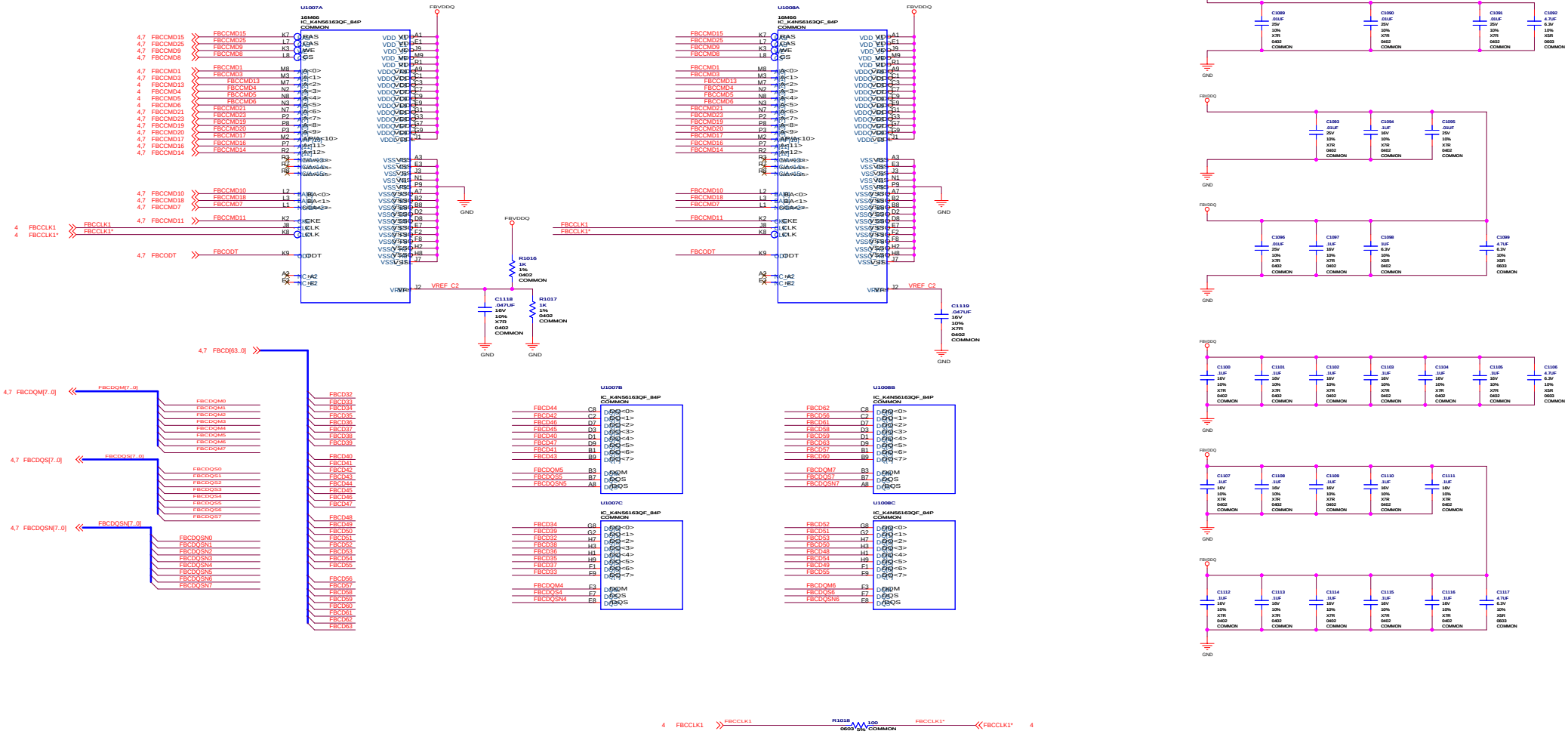
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



Micro-Star International Co., LTD.			
MS-V064			
Size: Custom	Document Number: Memory 2nd bank 0..31		Rev: 0A
Date: Tuesday, February 28, 2006		Sheet 7 of 20	

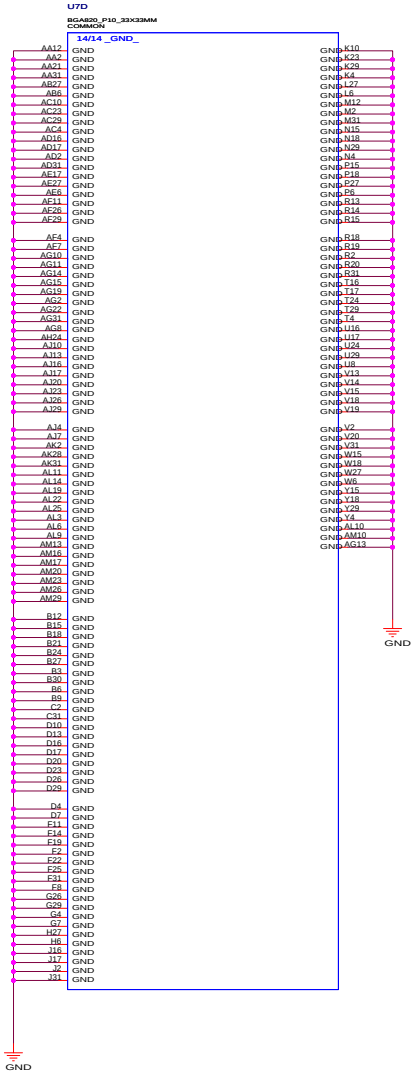
MEMORY 2nd bank
32..63

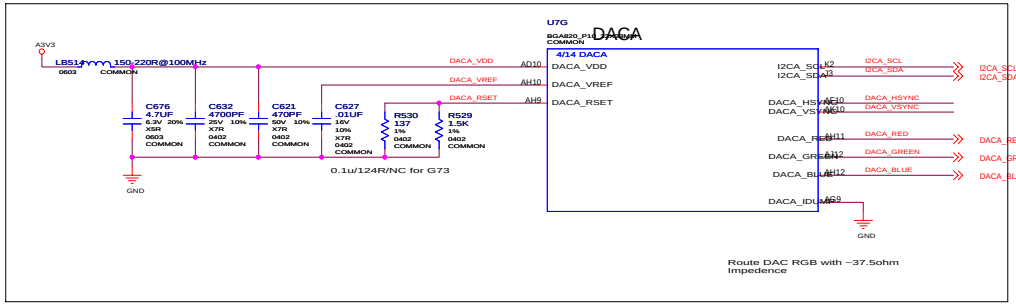
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE
TO MEMORY

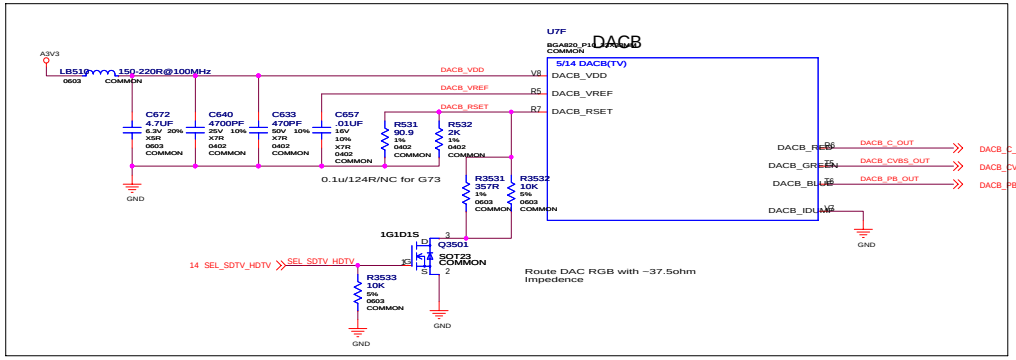


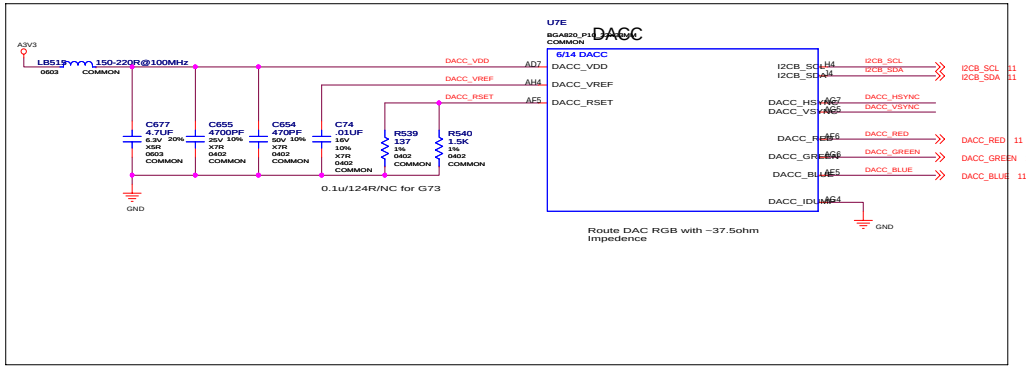
Micro-Star International Co., LTD.		
MS-V064		
Size: Custom	Document Number: Memory 2nd bank 32..63	Rev: 0A
Date: Tuesday, February 28, 2006	Sheet 8 of 20	

GND,DACA,DACB,DACC





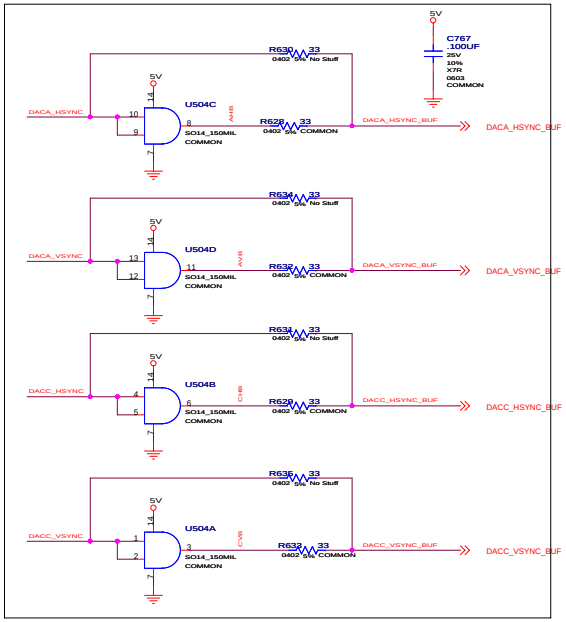




NET RULES

NET_NAME	MIN_LINE_WIDTH	NET_SPACING_RULE	IMPEDANCE
I2CA_SCL		10MIL	
I2CA_SDA		10MIL	
DACA_HSYNC		10MIL	
DACA_VSYNC		10MIL	
DACA_RED		20MIL	U6.AH11:R617.1:37.50 OHM:2%
DACA_GREEN		20MIL	U6.AJ12:R616.1:37.50 OHM:2%
DACA_BLUE		20MIL	U6.AH12:R615.1:37.50 OHM:2%
DACA_VDD	12	10MIL	
DACA_VREF	12	10MIL	
DACA_RSET	12	10MIL	
DACB_C_OUT		20MIL	U6.R6:R641.1:37.50 OHM:2%
DACB_CVBS_OUT		20MIL	U6.T5:R608.1:37.50 OHM:2%
DACB_PB_OUT		20MIL	U6.T6:R633.1:37.50 OHM:2%
DACB_VDD	12	10MIL	
DACB_VREF	12	10MIL	
DACB_RSET	12	10MIL	
DACC_HSYNC		10MIL	
DACC_VSYNC		10MIL	
DACC_RED		20MIL	U6.AF6:R623.1:37.50 OHM:2%
DACC_GREEN		20MIL	U6.AG6:R627.1:37.50 OHM:2%
DACC_BLUE		20MIL	U6.AE5:R620.1:37.50 OHM:2%
DACC_VDD	12	10MIL	
DACC_VREF	12	10MIL	
DACC_RSET	12	10MIL	
TV_RSET_SEL	12	10MIL	
I2CB_SDA		10MIL	
I2CB_SCL		10MIL	
SEL_2ND_DEV		10MIL	
AHB		10MIL	
AVB		10MIL	
DACA_HSYNC_BUF		10MIL	
DACA_VSYNC_BUF		10MIL	
CHB		10MIL	
CVB		10MIL	
DACC_HSYNC_BUF		10MIL	
DACC_VSYNC_BUF		10MIL	

DACA & DACC Sync Buffers



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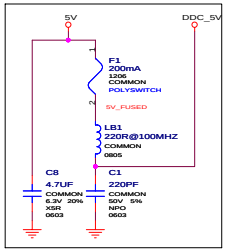
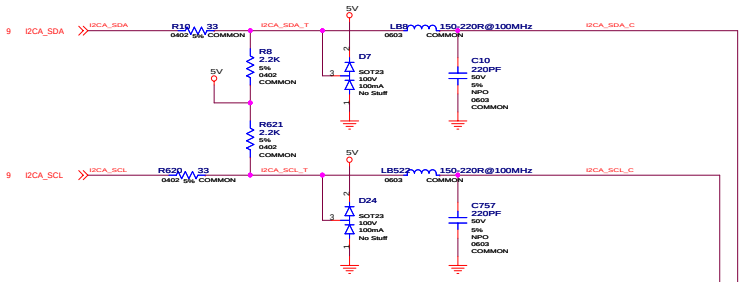
MS-V064
Size: Custom | Document Number: GND,DACA, DACB, DACC | Rev: 0A
Date: Thursday, February 23, 2006 | Sheet 9 of 20

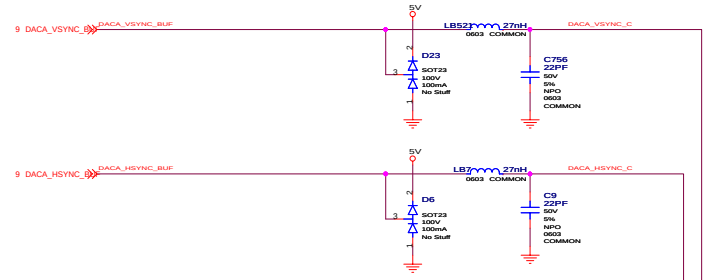
VGA
DACA

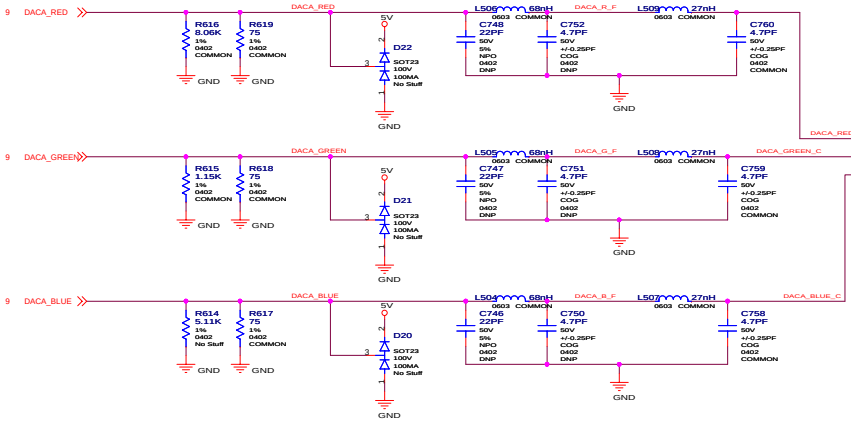
DDC
5V

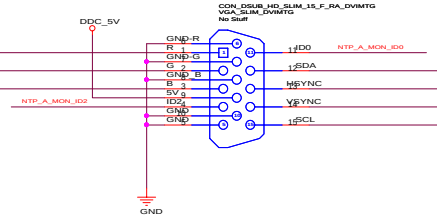


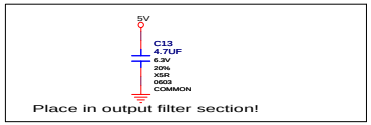
Changed the FUSE to 200mA



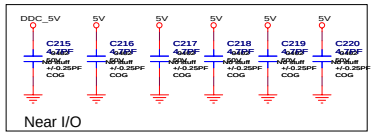


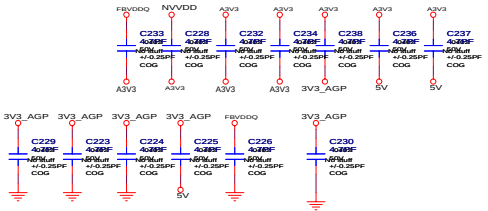






EMI Reserve Cap.





NET_NAME	NET_SPACING_RULE
DACA_R_F	20MIL
DACA_G_F	20MIL
DACA_B_F	20MIL
DACA_RED_C	20MIL
DACA_GREEN_C	20MIL
DACA_BLUE_C	20MIL
DACA_VSYNC_C	10MIL
DACA_HSYNC_C	10MIL

	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	16	5V
5V	16	5V
DDC_5V	16	5V
A3V3	16	3.3V
GND	16	0V

12 I2CA_SDA_C	I2CA_SDA_C	
12 I2CA_SCL_C	I2CA_SCL_C	
12 DACA_VSYNC_C	DACA_VSYNC_C	
12 DACA_HSYNC_C	DACA_HSYNC_C	
12 DACA_RED_C	DACA_RED_C	
12 DACA_GREEN_C	DACA_GREEN_C	
12 DACA_BLUE_C	DACA_BLUE_C	

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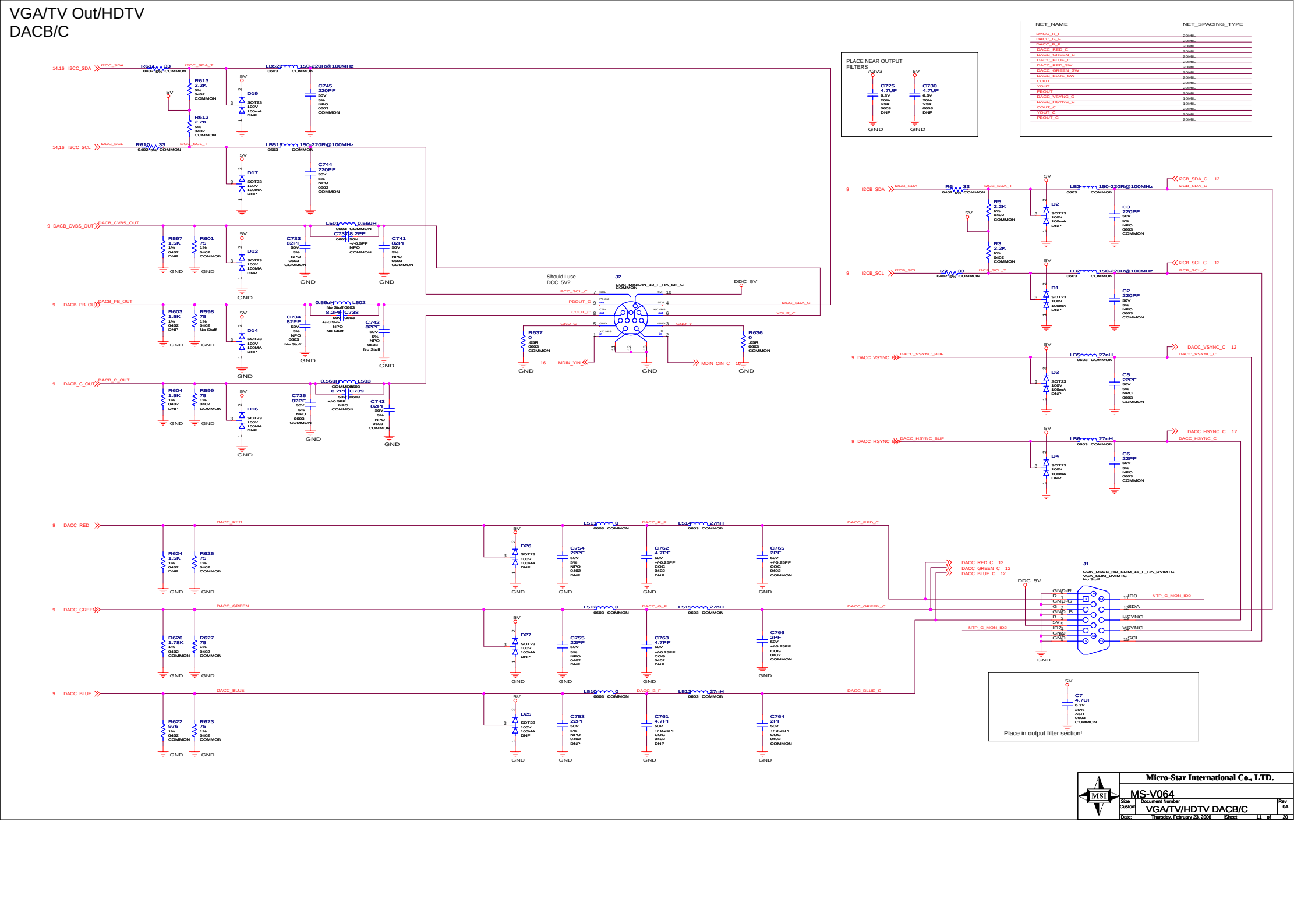
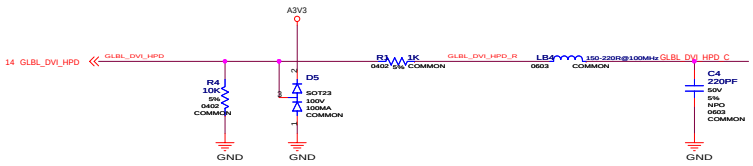
VGA/TV Out/HDTV
DACB/C



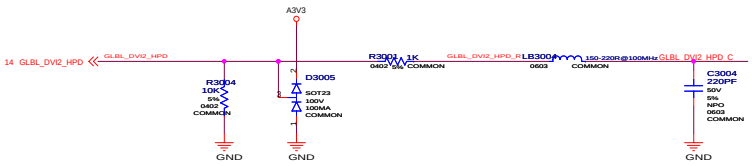
INTERNAL TMDS

Hotplug Detection



If no diodes stuffed shoud I stuff this?

Hotplug Detection2

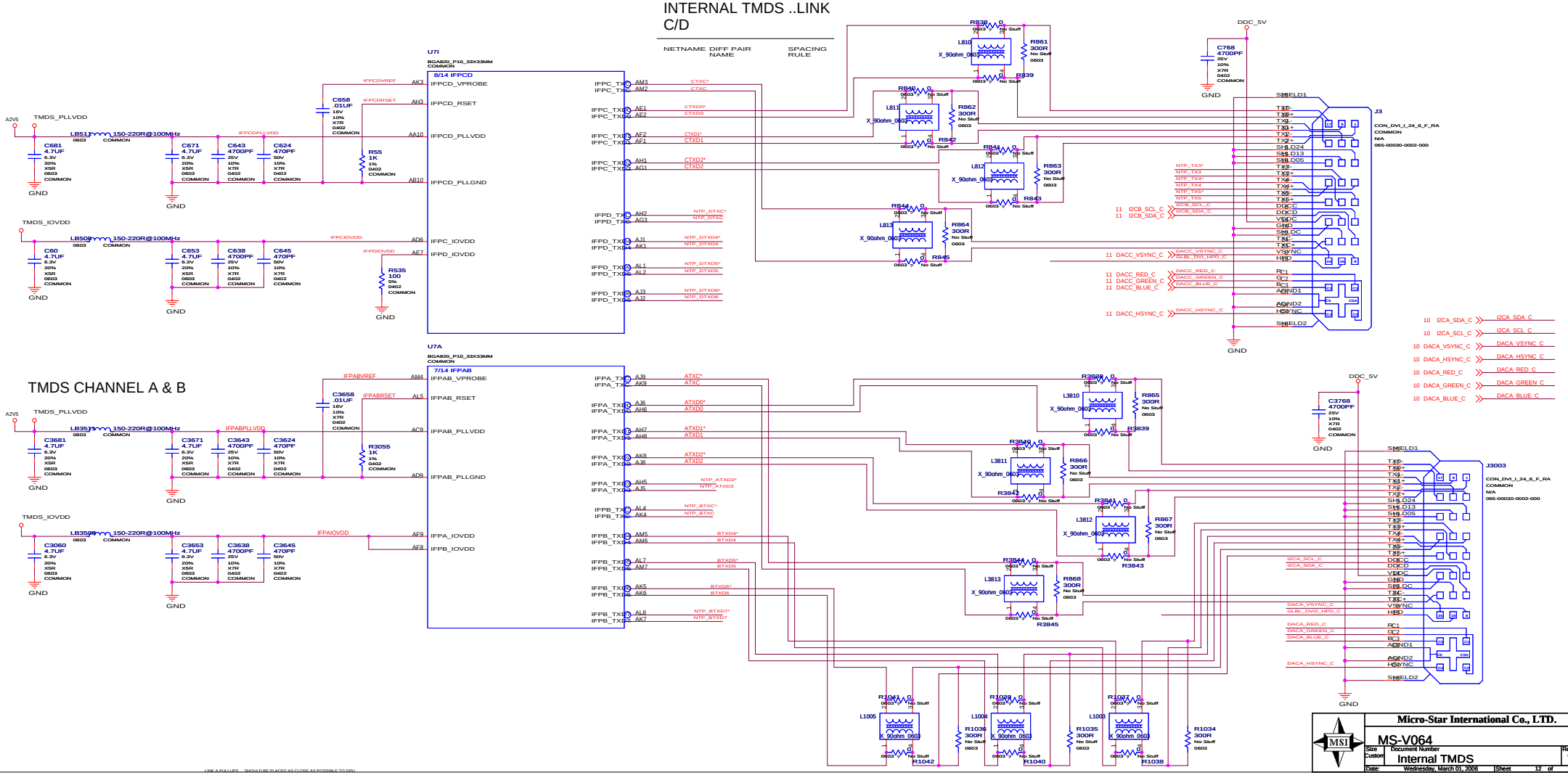


If no diodes stuffed shoud I stuff this?

INTERNAL TMDS ..LINK C/D

NETNAME	DIFF PAIR NAME	SPACING RULE

TMDS CHANNEL A & B



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Size: Custom	Document Number: Internal TMDS
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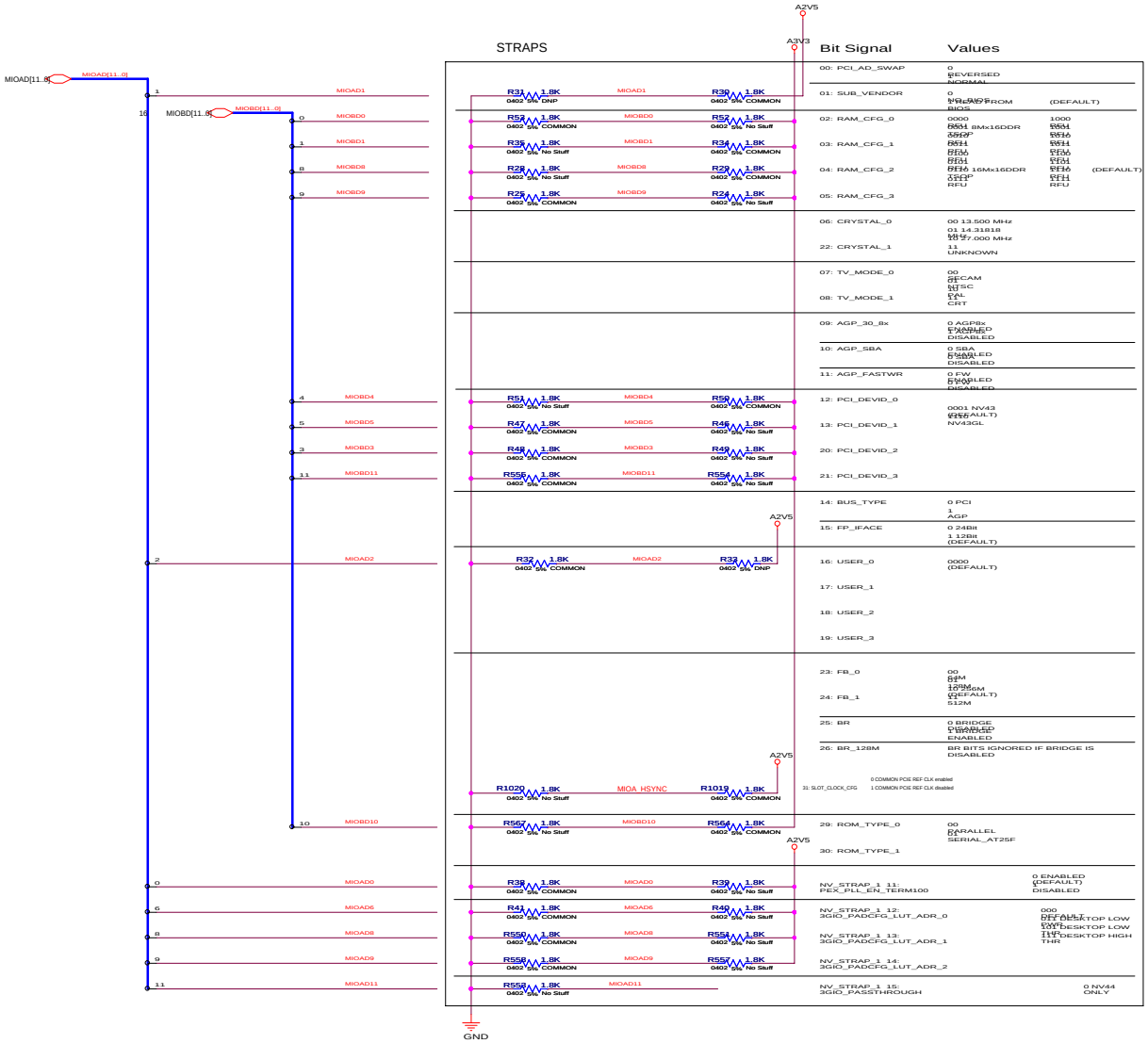
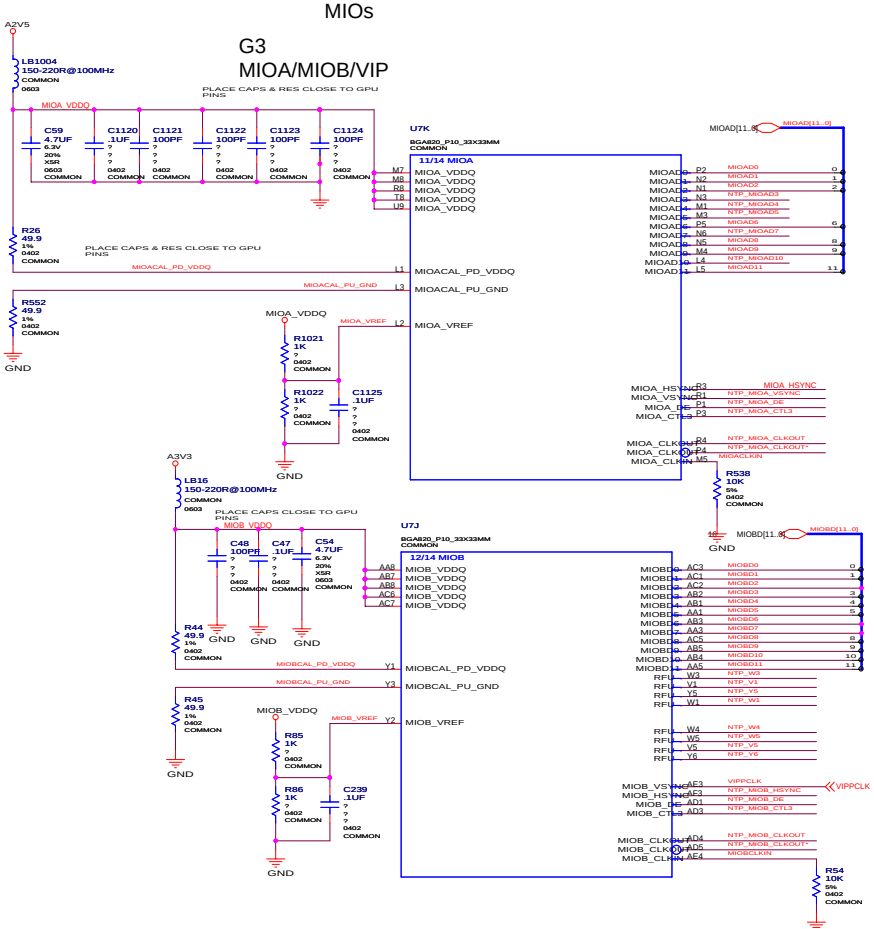
STRAPS, MIOA/MIOB

STRAPS



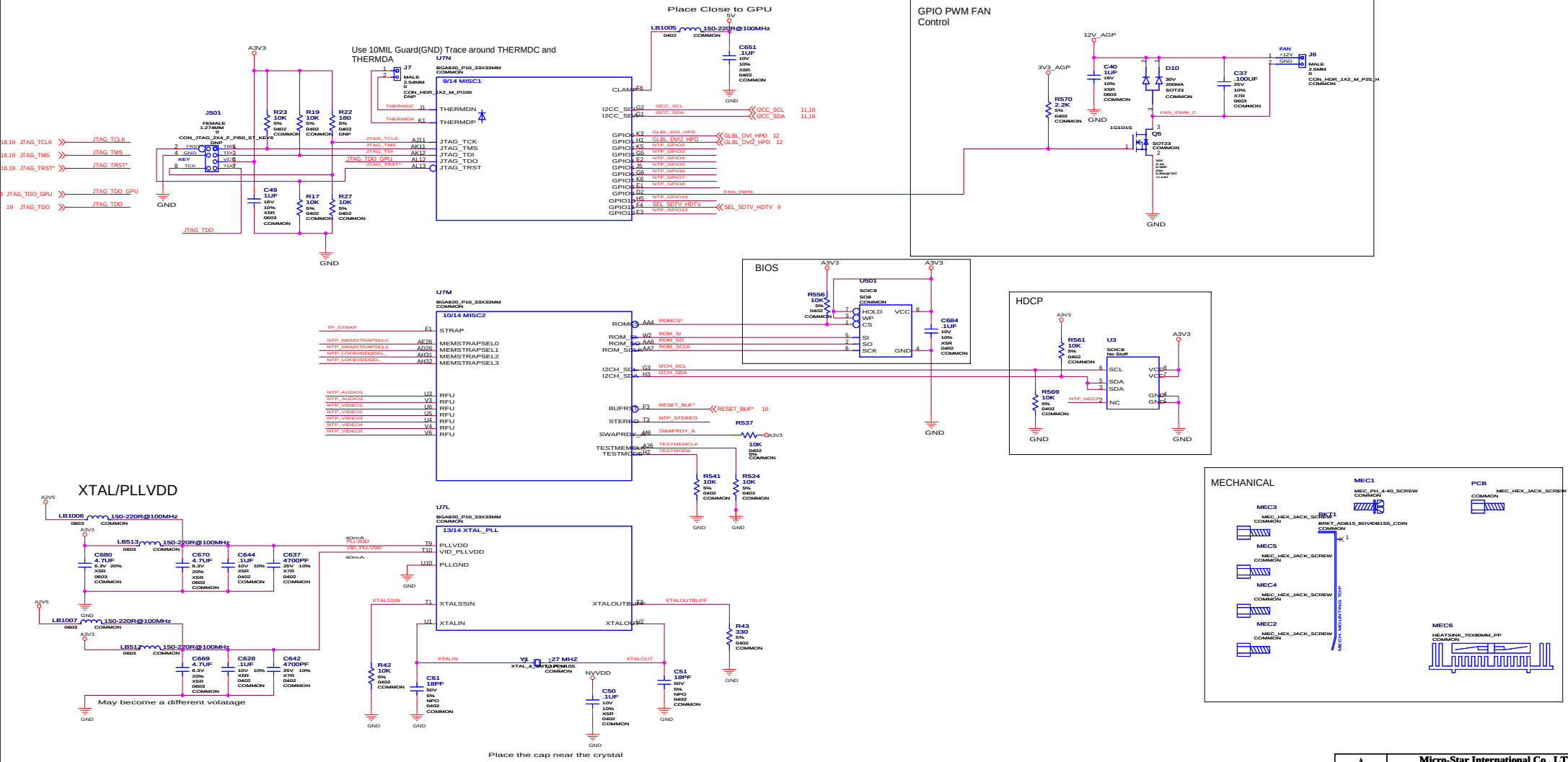
MIOs

G3 MIOA/MIOB/VIP



XTAL, GPIO, ROM

NET	MIN_LIN_WIDTH	NET_SPACING_RULE
XTALIN		20MIL
XTALOUT		20MIL
PLLVDD	12	10MIL
VID_PLLVDD	12	10MIL
FAN_PWM		20MIL
FAN_PWM_B		20MIL
FAN_PWM_C		20MIL
THERMDC	10	
THERMDA	10	



Micro-Star International Co., LTD.		
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Size: Custom	Document Number: XTAL,GPIO,ROM,FAN,MEC	Rev: 0A
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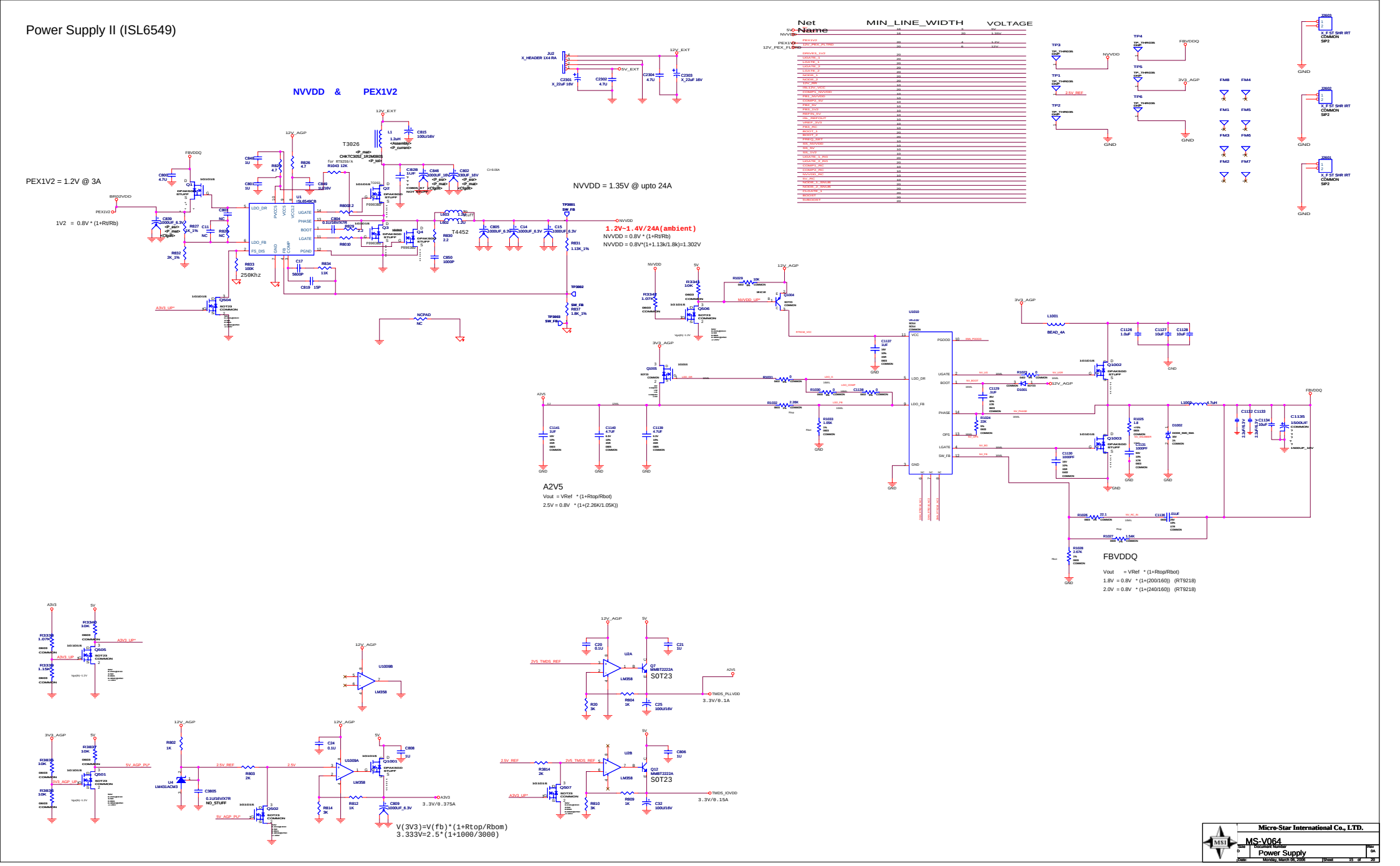
Power Supply II (ISL6549)



Net Name	MIN_LINE_WIDTH	VOLTAGE
5V_NVVDD	16	5V
PEX1V2	20	1.2V
12V_PEX_FLTRD	20	12V

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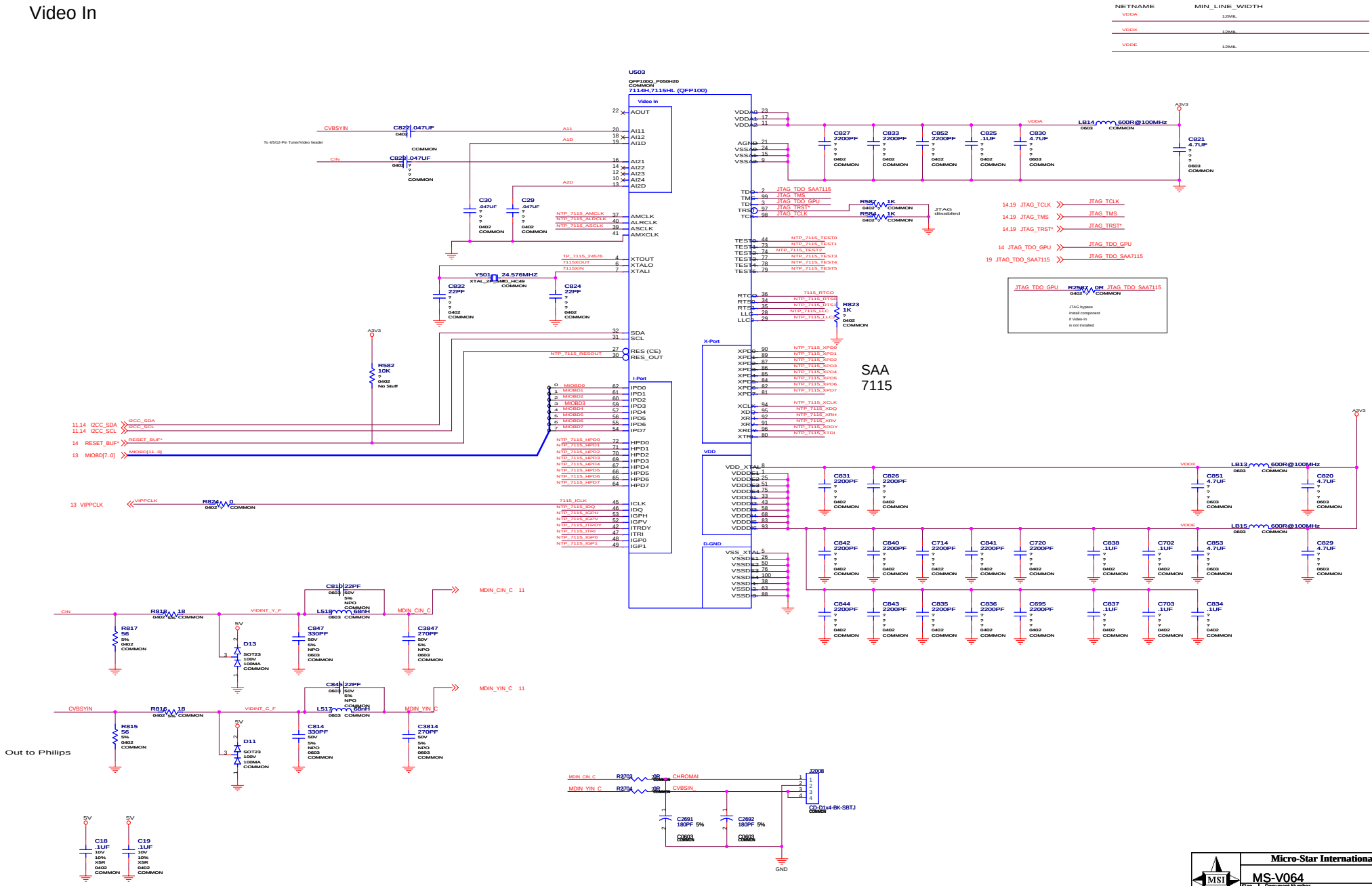
Power Supply

Video In


NETNAME MIN_LINE_WIDTH
VDDA 12MIL
VDDX 12MIL
VDDE 12MIL
U503
QFP100Q_P050H20
COMMON
7114H,7115HL (QFP100)
Video in
SAA
7115
X-Port
I-Port
VDD
D-GND
JTAG_TDO_GPU R2587 0R JTAG_TDO_SAA7115
JTAG bypass
Install component
if Video-In
is not installed
Out to Philips
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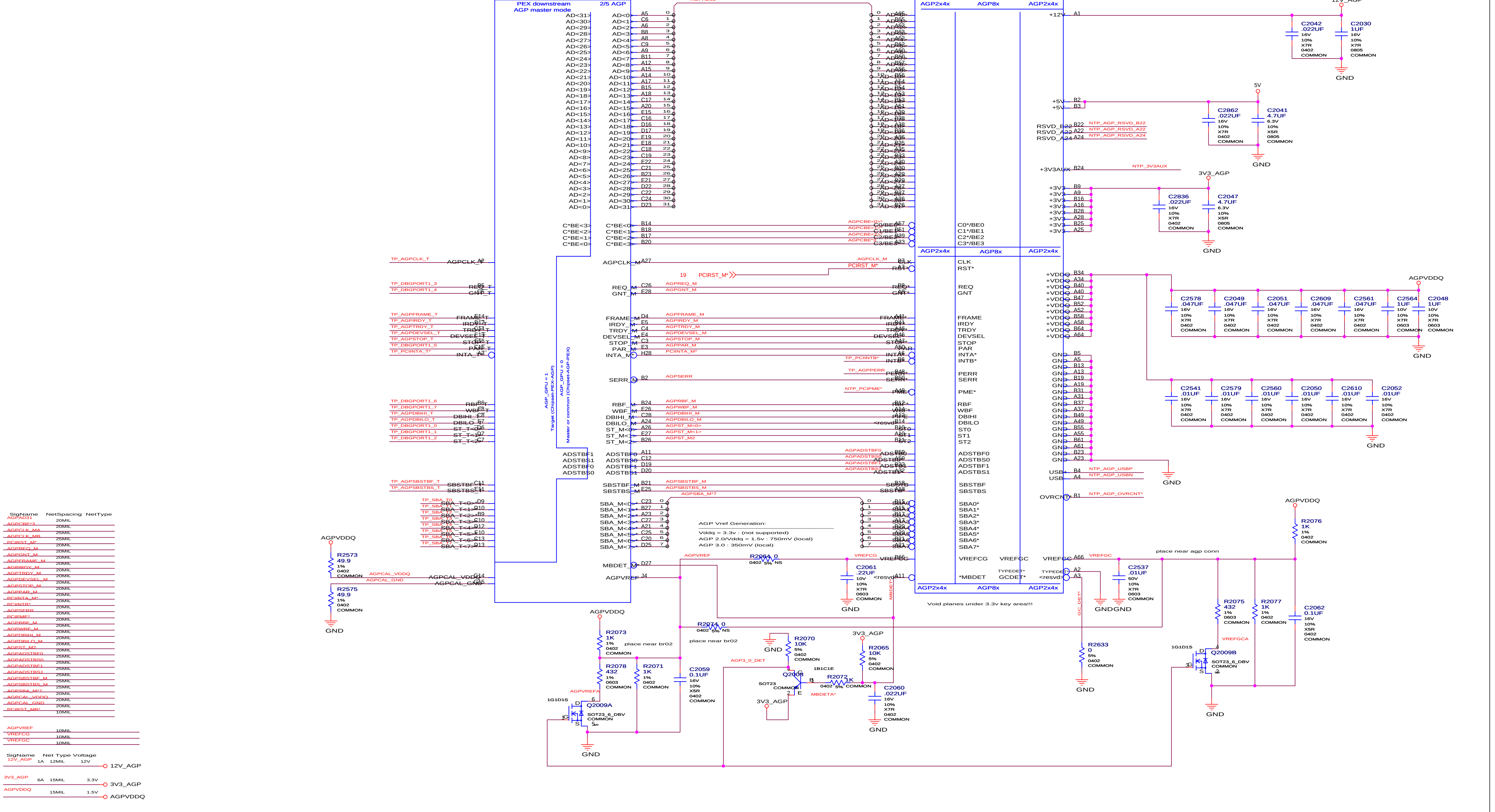
2. AGP to BR02 Interface

1



ASSEMBLY
PAGE
DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
AGP to BR02 Interface

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

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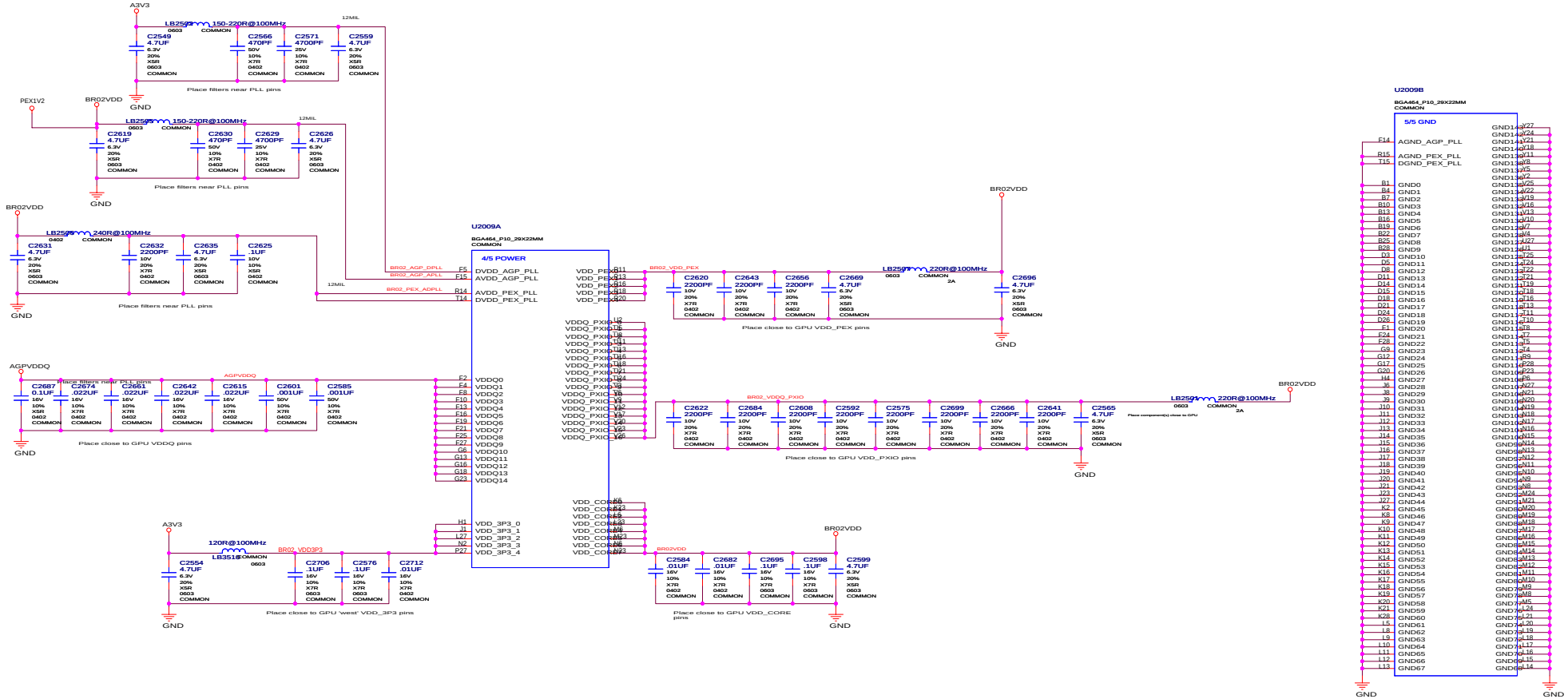
3. BR02
PWR/GND/De-Coupling



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	BR02
DETAIL	PWR/GND/De-Coupling

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Size: Custom	Document Number: BR02 PWR/GND/De-Coupling
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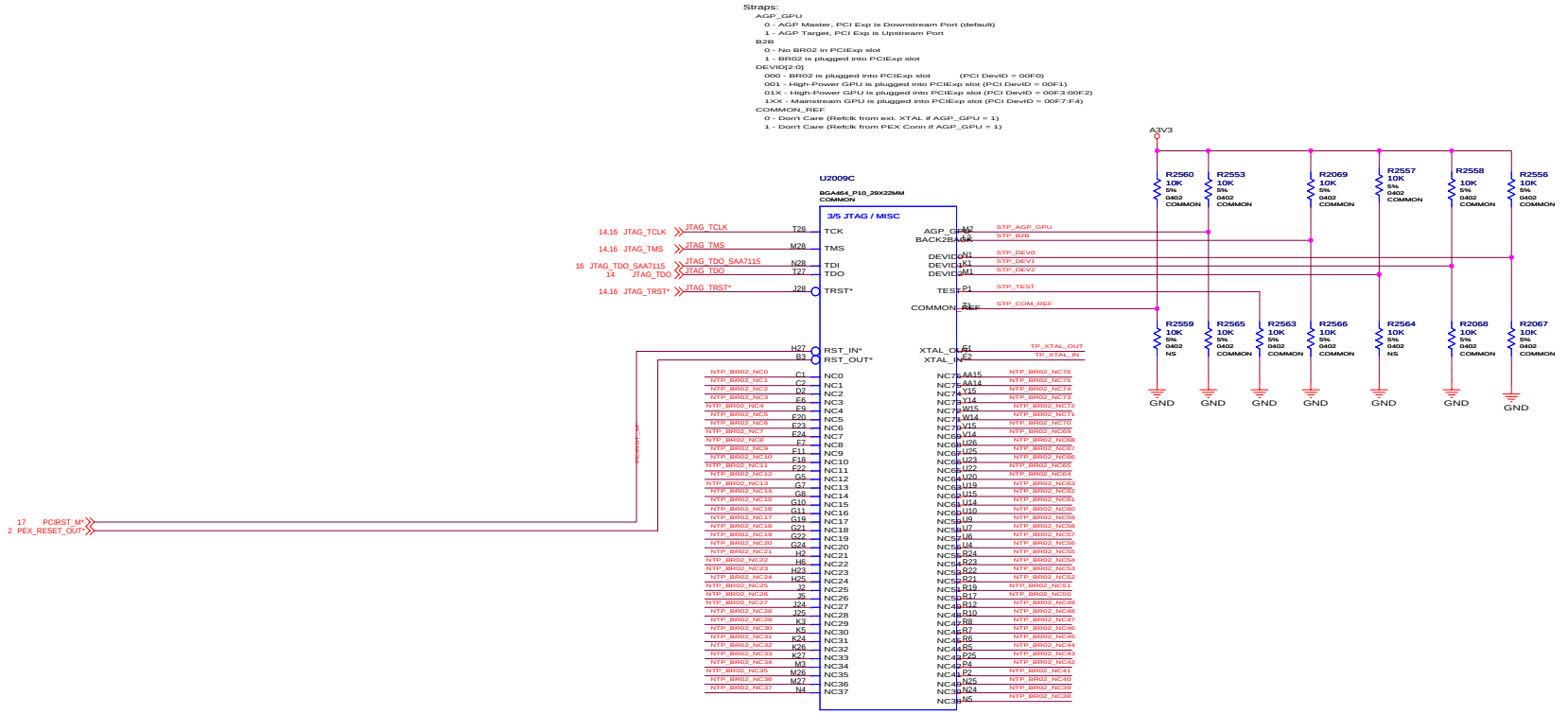
4. BR02 JTAG / Straps / Misc.



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BR02 STRAPS / MISC.

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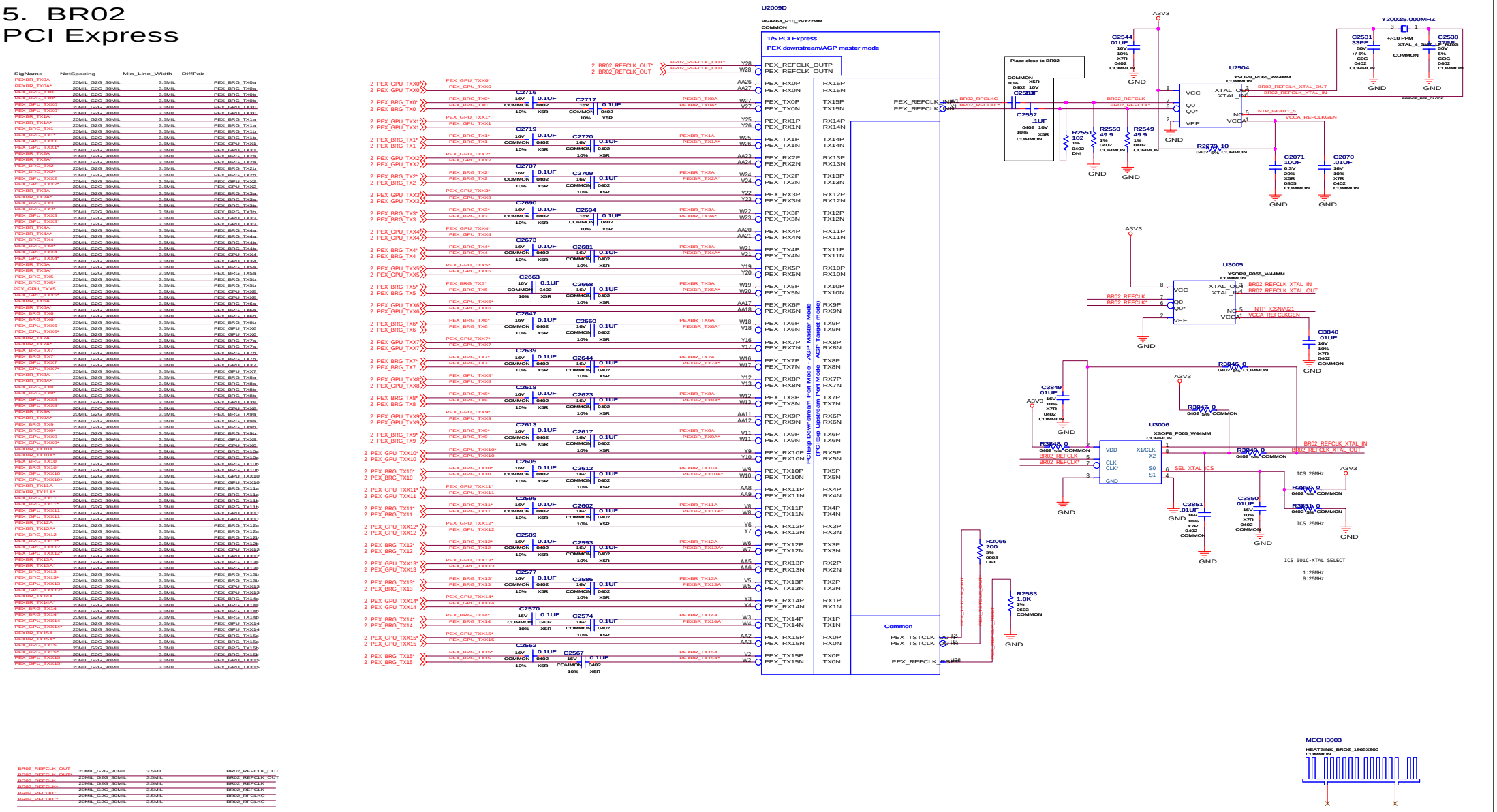
5. BR02
PCI Express



SigName	NetSpacing	Min_Line_Width	DiffPair
PEXBR_TX0A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX0a
PEXBR_TX0A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX0a
PEX_BRG_TX0	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX0b
PEX_BRG_TX0*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX0b
PEX_GPU_TX00	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX00
PEX_GPU_TX00*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX00
PEXBR_TX1A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX1a
PEXBR_TX1A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX1a
PEX_BRG_TX1	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX1b
PEX_BRG_TX1*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX1b
PEX_GPU_TX01	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX01
PEX_GPU_TX01*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX01
PEXBR_TX2A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX2a
PEXBR_TX2A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX2a
PEX_BRG_TX2	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX2b
PEX_BRG_TX2*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX2b
PEX_GPU_TX02	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX02
PEX_GPU_TX02*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX02
PEXBR_TX3A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX3a
PEXBR_TX3A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX3a
PEX_BRG_TX3	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX3b
PEX_BRG_TX3*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX3b
PEX_GPU_TX03	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX03
PEX_GPU_TX03*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX03
PEXBR_TX4A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX4a
PEXBR_TX4A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX4a
PEX_BRG_TX4	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX4b
PEX_BRG_TX4*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX4b
PEX_GPU_TX04	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX04
PEX_GPU_TX04*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX04
PEXBR_TX5A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX5a
PEXBR_TX5A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX5a
PEX_BRG_TX5	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX5b
PEX_BRG_TX5*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX5b
PEX_GPU_TX05	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX05
PEX_GPU_TX05*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX05
PEXBR_TX6A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX6a
PEXBR_TX6A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX6a
PEX_BRG_TX6	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX6b
PEX_BRG_TX6*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX6b
PEX_GPU_TX06	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX06
PEX_GPU_TX06*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX06
PEXBR_TX7A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX7a
PEXBR_TX7A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX7a
PEX_BRG_TX7	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX7b
PEX_BRG_TX7*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX7b
PEX_GPU_TX07	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX07
PEX_GPU_TX07*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX07
PEXBR_TX8A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX8a
PEXBR_TX8A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX8a
PEX_BRG_TX8	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX8b
PEX_BRG_TX8*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX8b
PEX_GPU_TX08	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX08
PEX_GPU_TX08*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX08
PEXBR_TX9A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX9a
PEXBR_TX9A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX9a
PEX_BRG_TX9	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX9b
PEX_BRG_TX9*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX9b
PEX_GPU_TX09	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX09
PEX_GPU_TX09*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX09
PEXBR_TX10A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX10a
PEXBR_TX10A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX10a
PEX_BRG_TX10	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX10b
PEX_BRG_TX10*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX10b
PEX_GPU_TX10	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX10
PEX_GPU_TX10*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX10
PEXBR_TX11A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX11a
PEXBR_TX11A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX11a
PEX_BRG_TX11	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX11b
PEX_BRG_TX11*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX11b
PEX_GPU_TX11	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX11
PEX_GPU_TX11*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX11
PEXBR_TX12A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX12a
PEXBR_TX12A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX12a
PEX_BRG_TX12	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX12b
PEX_BRG_TX12*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX12b
PEX_GPU_TX12	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX12
PEX_GPU_TX12*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX12
PEXBR_TX13A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX13a
PEXBR_TX13A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX13a
PEX_BRG_TX13	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX13b
PEX_BRG_TX13*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX13b
PEX_GPU_TX13	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX13
PEX_GPU_TX13*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX13
PEXBR_TX14A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX14a
PEXBR_TX14A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX14a
PEX_BRG_TX14	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX14b
PEX_BRG_TX14*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX14b
PEX_GPU_TX14	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX14
PEX_GPU_TX14*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX14
PEXBR_TX15A	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX15a
PEXBR_TX15A*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX15a
PEX_BRG_TX15	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX15b
PEX_BRG_TX15*	20MIL_G2G_30MIL	3.5MIL	PEX_BRG_TX15b
PEX_GPU_TX15	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX15
PEX_GPU_TX15*	20MIL_G2G_30MIL	3.5MIL	PEX_GPU_TX15

BR02_REFCLK_OUT	20MIL_G2G_30MIL	3.5MIL	BR02_REFCLK_OUT
BR02_REFCLK_OUT*	20MIL_G2G_30MIL	3.5MIL	BR02_REFCLK_OUT
BR02_REFCLK	20MIL_G2G_30MIL	3.5MIL	BR02_REFCLK
BR02_REFCLK*	20MIL_G2G_30MIL	3.5MIL	BR02_REFCLK
BR02_REFCLKC	20MIL_G2G_30MIL	3.5MIL	BR02_REFCLKC
BR02_REFCLKC*	20MIL_G2G_30MIL	3.5MIL	BR02_REFCLKC

PEX_REFCLK_RSET		3.5MIL	
PEX_TSTCLK_OUT	20MIL_G2G_30MIL	3.5MIL	PEX_TSTCLK_OUT
PEX_TSTCLK_OUT*	20MIL_G2G_30MIL	3.5MIL	PEX_TSTCLK_OUT
BR02_REFCLK_OUT	20MIL_G2G_30MIL	3.5MIL	BR02_REFCLK_OUT
BR02_REFCLK_OUT*	20MIL_G2G_30MIL	3.5MIL	BR02_REFCLK_OUT

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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