

P262: NV44/G3-64, TSOP MEMORY x16

REV HISTORY


A01

- 9/22/2004:
- Changed TMDS, PLLVDD to PLLVDD
 - Added bead option to PLLVDD rail of NV44
 - Changed RSET values for DACA and DACB
 - Changed DACB RSET FET to a dual package with GPIO11 control-Macrovision
 - Added F3V3 bypass to PLLVDD linear regulator
 - Changed location of R62

REV	VARIANT	M/P/N	ASSEMBLY
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ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P262 Overview



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V001

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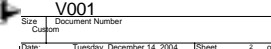
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Rev: A00

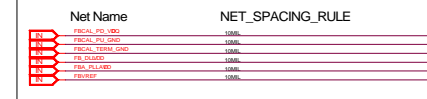
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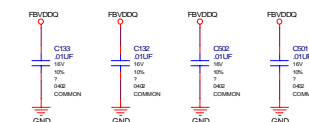
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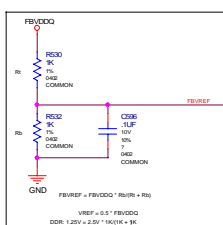
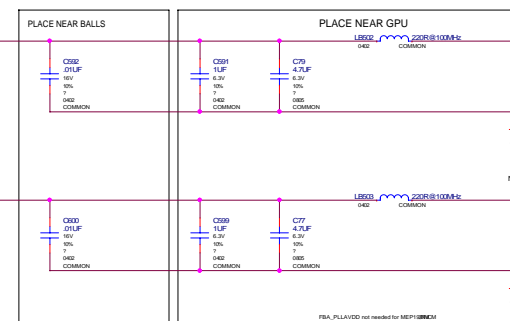
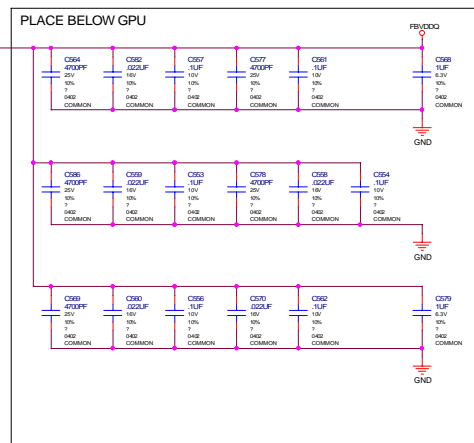
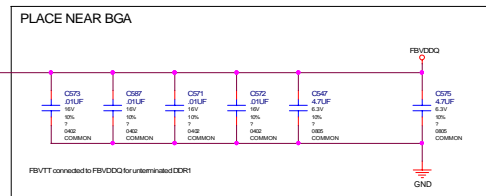
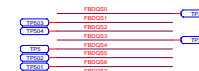
GPU: FB-Interface



X-Caps for FB_CMD BUS



LABTESTPOINTS



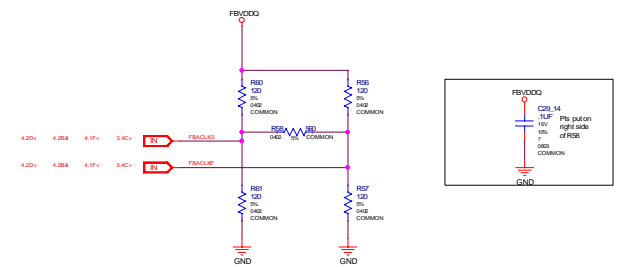
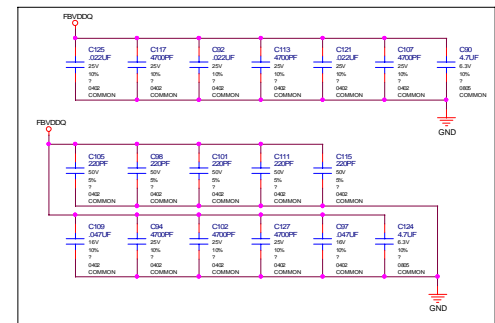
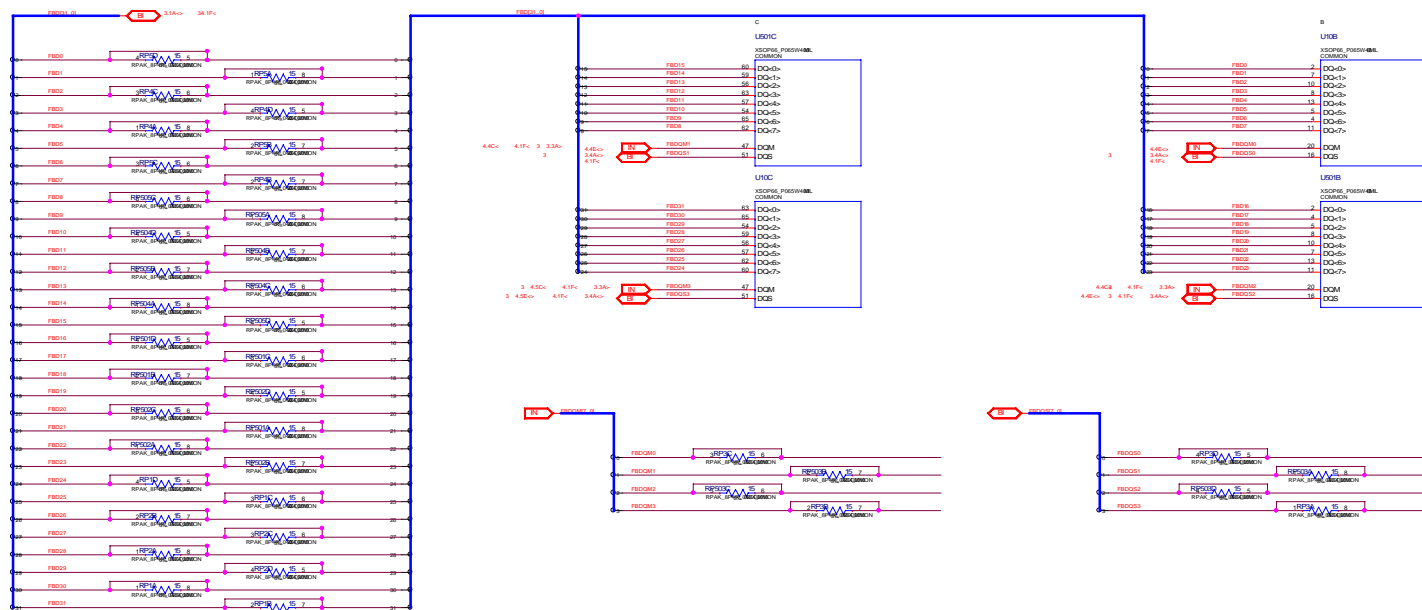
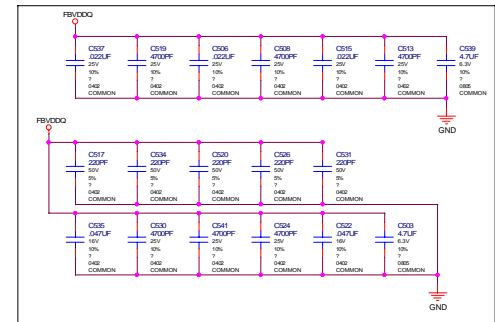
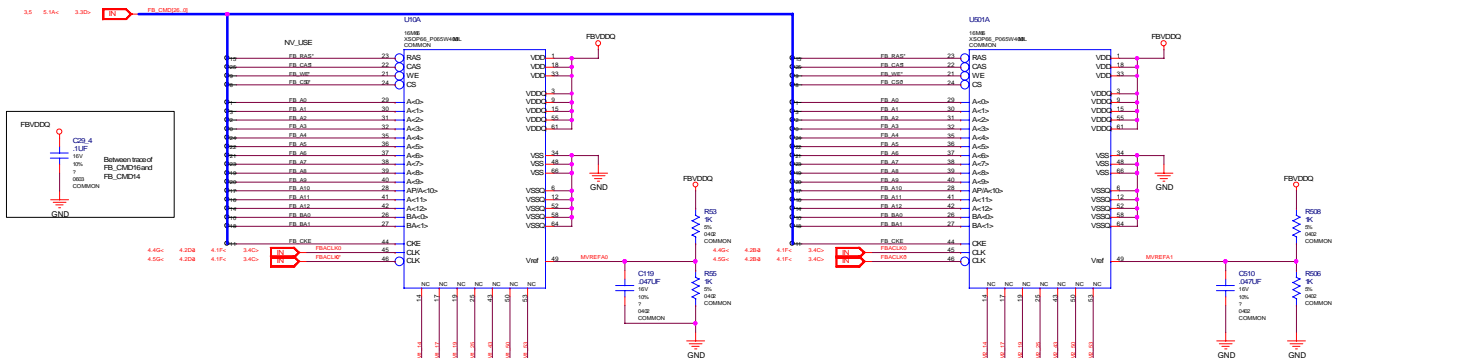
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ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FIN
PAGE DETAIL	Frame Buffer Interface

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V001		Revision
Document Number	Revision	
Custom	Alt	
Date	Tuesday, December 14, 2004	Sheet 3 of 13

Memory Bit
0..31



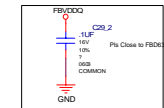
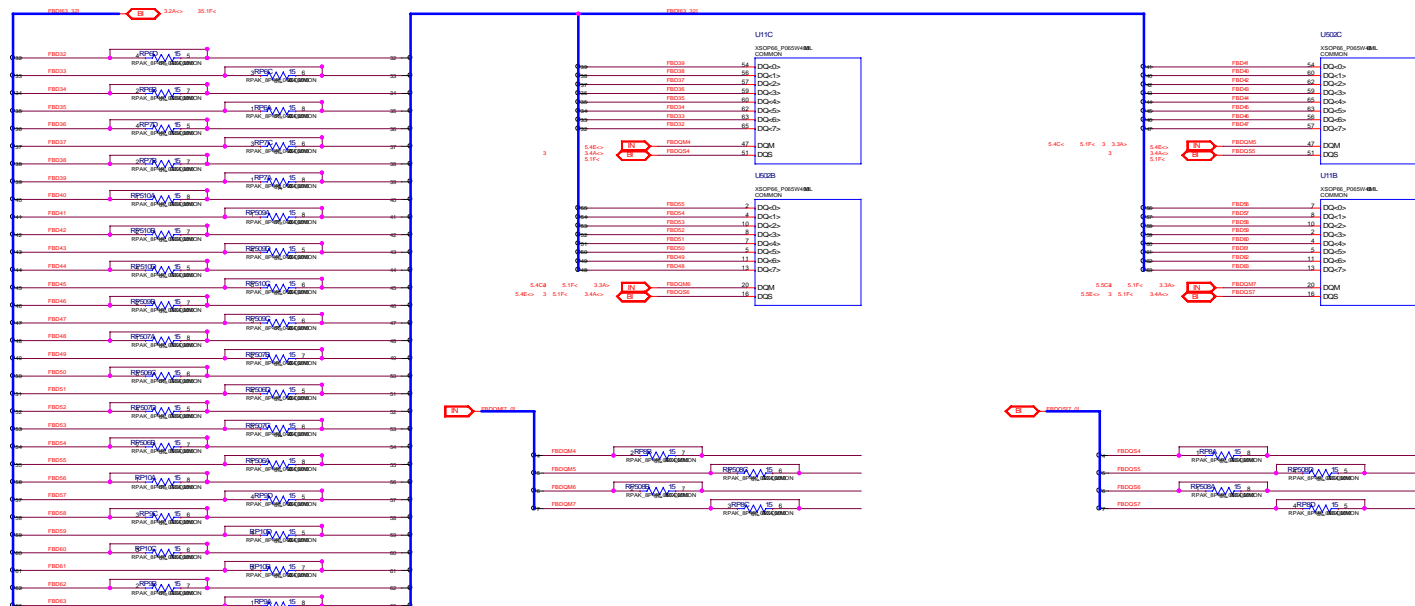
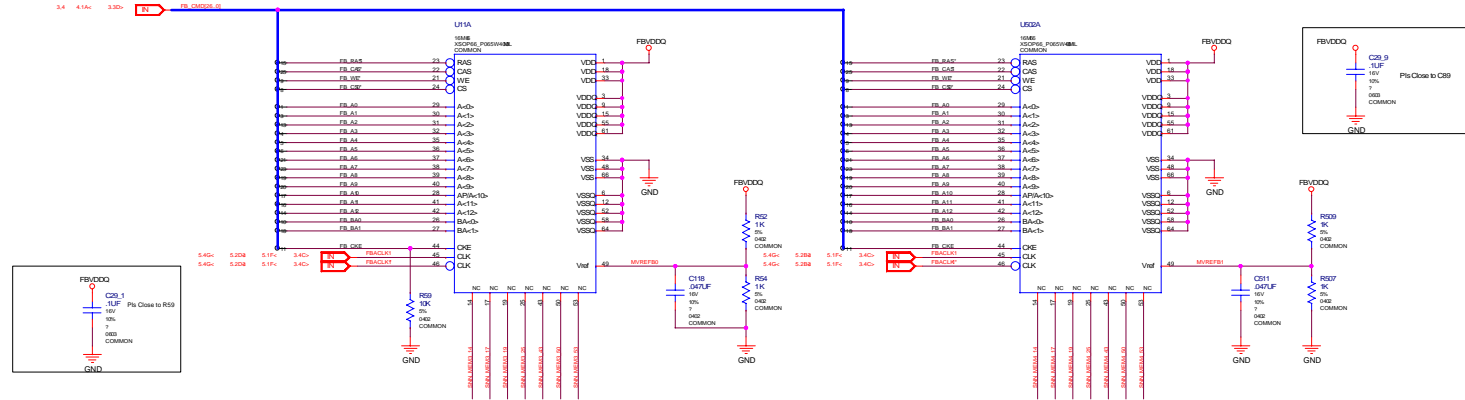
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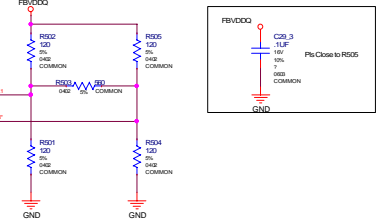
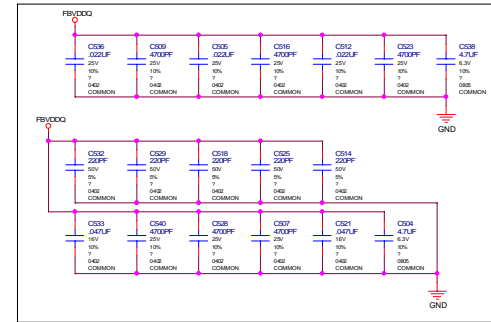
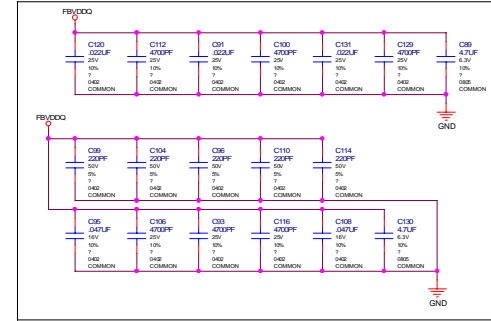
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Document Number			Rev A00
Tuesday, December 14, 2004		Sheet	4 of 13

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Memory Bit
32..63

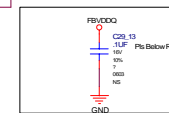
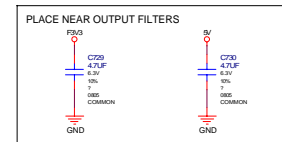
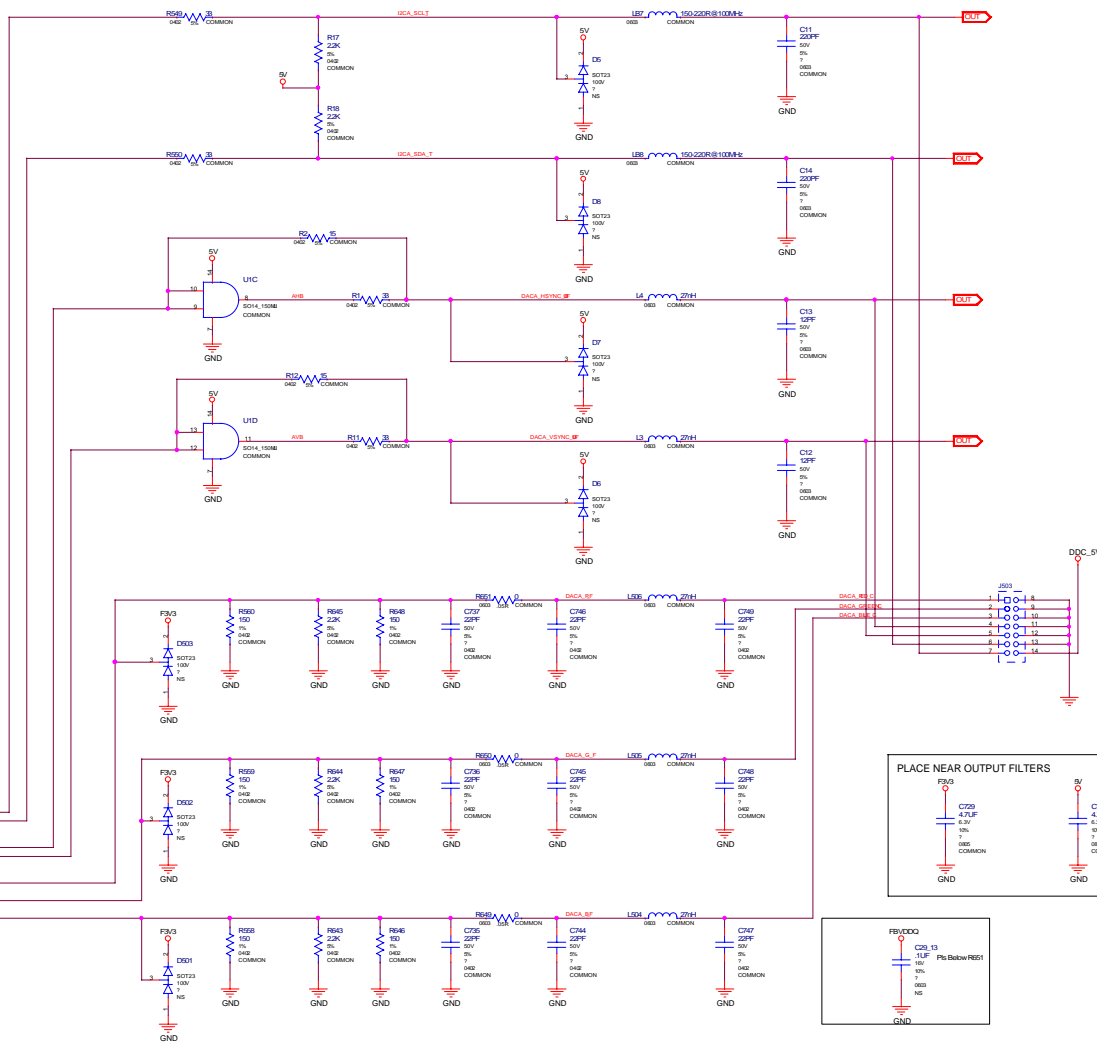
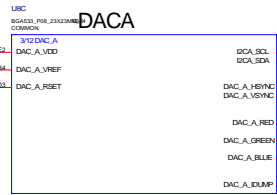
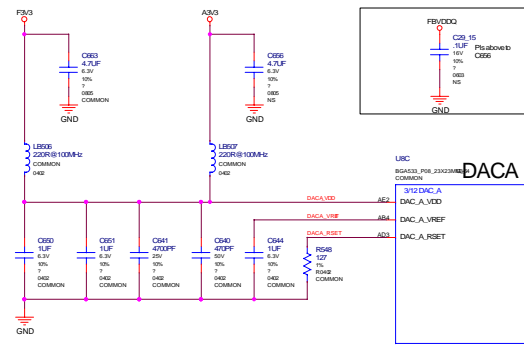
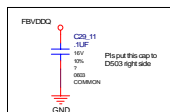
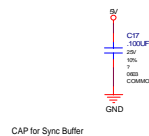


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FRAGLUT101	FRAGLUT1	250M
FRAGLUT102	FRAGLUT1	250M



DAC-A, DB15 Connector

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1003	DGCA_V001		100ML
1004	DGCA_V001		100ML
1005	DGCA_V001		100ML
1006	DGCA_V001		100ML
1007	DGCA_V001		100ML
1008	DGCA_V001	100ML	100ML
1009	DGCA_B01		200ML
1010	DGCA_B01		200ML
1011	DGCA_B01		200ML
1012	DGCA_B01		200ML
1013	DGCA_B01		200ML
1014	DGCA_B01		200ML
1015	DGCA_B01		200ML
1016	DGCA_B01		200ML
1017	DGCA_B01		200ML
1018	DGCA_B01		200ML
1019	DGCA_B01		200ML
1020	DGCA_B01		200ML
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1105	DGCA_B01		200ML
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PAGE DETAIL	DWGA, DWCB, DWCC, Sunc Butters



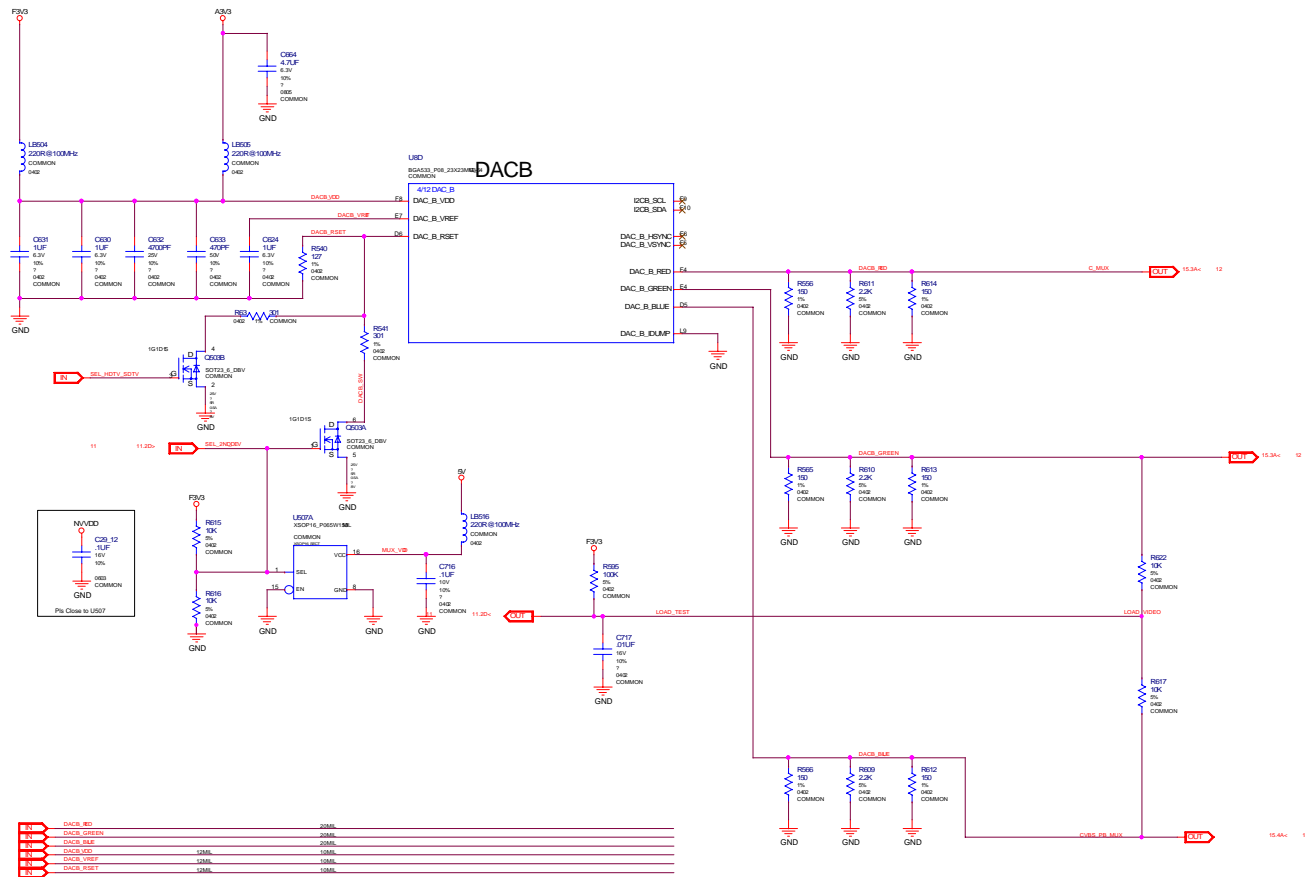
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V001

Size	Document Number
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Date:	Tuesday, Dec

Rev	13
AOC	13

DAC-B, MUX,
DB15



ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	VGA Output, TV Out

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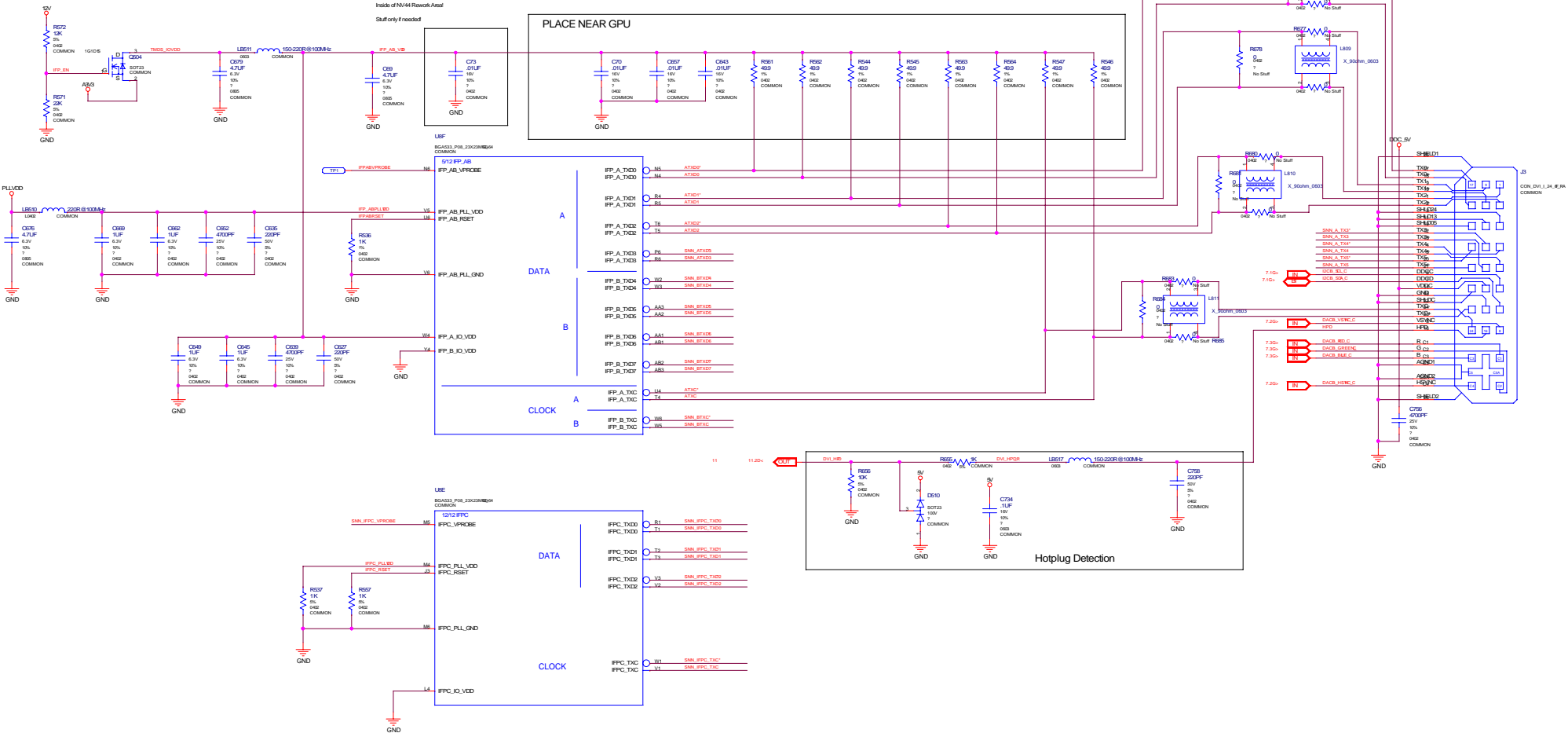
V001

Document Number

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Internal TMDS, DVI-Connector



Net Name	Diffpair	NET_SPACING_RULE	Voltage
REF_48VLS1B1			3.3V
REF_AB_VCB			3.3V
ATX0	ATX0C	200M	
ATX01	ATX0C	200M	
ATX02	ATX0C	200M	
ATX03	ATX0C	200M	
ATX04	ATX0C	200M	
ATX05	ATX0C	200M	
ATX06	ATX0C	200M	
ATX07	ATX0C	200M	
ATX08	ATX0C	200M	
ATX09	ATX0C	200M	
ATX10	ATX0C	200M	
ATX11	ATX0C	200M	
ATX12	ATX0C	200M	
ATX13	ATX0C	200M	
ATX14	ATX0C	200M	
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ATX16	ATX0C	200M	
ATX17	ATX0C	200M	
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ATX25	ATX0C	200M	
ATX26	ATX0C	200M	
ATX27	ATX0C	200M	
ATX28	ATX0C	200M	
ATX29	ATX0C	200M	
ATX30	ATX0C	200M	
ATX31	ATX0C	200M	
ATX32	ATX0C	200M	
ATX33	ATX0C	200M	
ATX34	ATX0C	200M	
ATX35	ATX0C	200M	
ATX36	ATX0C	200M	
ATX37	ATX0C	200M	
ATX38	ATX0C	200M	
ATX39	ATX0C	200M	
ATX40	ATX0C	200M	
ATX41	ATX0C	200M	
ATX42	ATX0C	200M	
ATX43	ATX0C	200M	
ATX44	ATX0C	200M	
ATX45	ATX0C	200M	
ATX46	ATX0C	200M	
ATX47	ATX0C	200M	
ATX48	ATX0C	200M	
ATX49	ATX0C	200M	
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ATX54	ATX0C	200M	
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ATX93	ATX0C	200M	
ATX94	ATX0C	200M	
ATX95	ATX0C	200M	
ATX96	ATX0C	200M	
ATX97	ATX0C	200M	
ATX98	ATX0C	200M	
ATX99	ATX0C	200M	
ATX100	ATX0C	200M	
ATX101	ATX0C	200M	
ATX102	ATX0C	200M	
ATX103	ATX0C	200M	
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ATX105	ATX0C	200M	
ATX106	ATX0C	200M	
ATX107	ATX0C	200M	

ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMD5 Interface



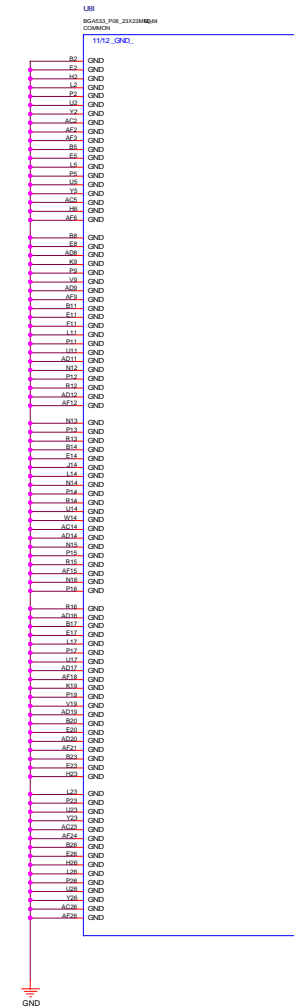
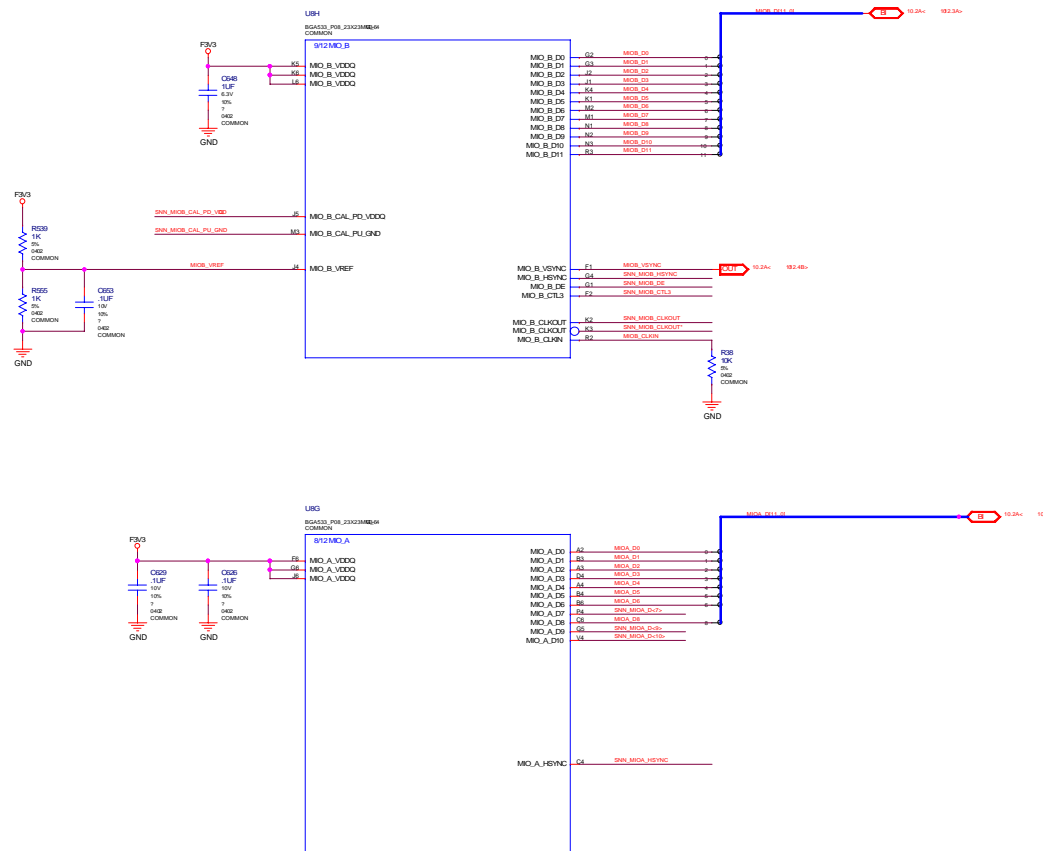
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MIOA, MIOB Interface, LPC-ROM



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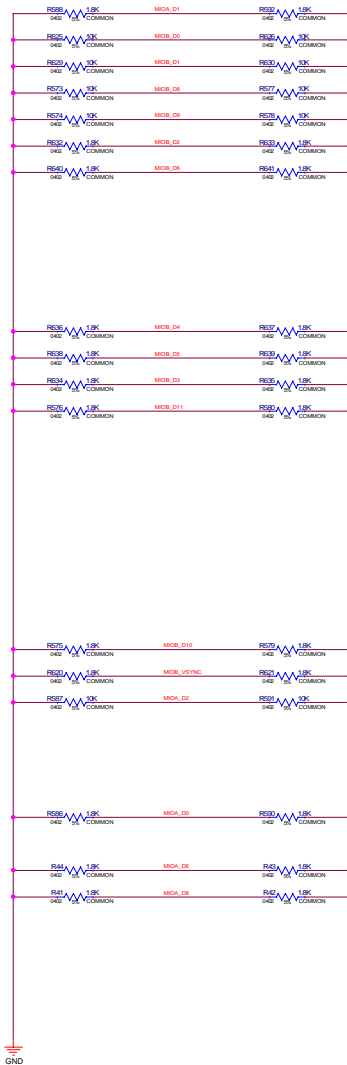
ASSEMBLY
PAGE DETAIL

LPC-ROM
MIOA/MIOB Interface,
LPC-ROM

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STRAPS, Mechanical Parts

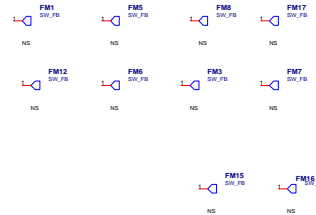
NV44 STRAPS



Bit Signal

Values

00:	PCI_AD_SWP	0 REVERSED	1 NORMAL
01:	SUB_VENDOR	0 NO_BIOS	1 READ FROM BIOS
02:	RAM_CFG_0	0000 RPU	1000 RPU
03:	RAM_CFG_1	0000 RPU	1000 RPU
04:	RAM_CFG_2	0100 RPU	1100 RPU
05:	RAM_CFG_3	0110 RPU	1110 RPU
06:	CRYSTAL_0	00 13.000 00M	01 13.333 00M
22:	CRYSTAL_1	00 27.000 00M	11 UNKNOWN
07:	TV_MODE_0	00 SECAM	01 NTSC
08:	TV_MODE_1	10 FIL	11 CRT
09:	AGP_3L_3s	0 AGP3n ENABLED	1 AGP3n DISABLED
10:	AGP_3BA	0 3BA ENABLED	0 3BA DISABLED
11:	AGP_FASTVTR	0 FV ENABLED	0 FV DISABLED
12:	PCI_DEV0_0	1100 (default 0000)	
13:	PCI_DEV0_1		
20:	PCI_DEV0_2		
21:	PCI_DEV0_3		
14:	BIU_TYPE	0 PCI	1 AGP
15:	FP_FACE	0 3BA	1 3BA (DEFAULT)
23:	FB_0	00 6M	01 10M
24:	FB_1	10 255M (DEFAULT)	11 512M
25:	BR	0 BRIDGE DISABLED	1 BRIDGE ENABLED
26:	BR_10M	BR BITS LOCKED IF BRIDGE IS DISABLED	
27:	BR_AGP		
28:	BR_IO		
29:	ROM_TYPE_0	00 PARALLEL	01 SERIAL_AT25P
30:	ROM_TYPE_1	10 SERIAL_SST49VF	11 UPC
16:	USER_0	0000 DEFAULT	
17:	USER_1		
18:	USER_2		
19:	USER_3		
PEX_PUL_EN_TERMS0			
32G0_PADCFS_LUT_ADDR0			
32G0_PADCFS_LUT_ADDR1			



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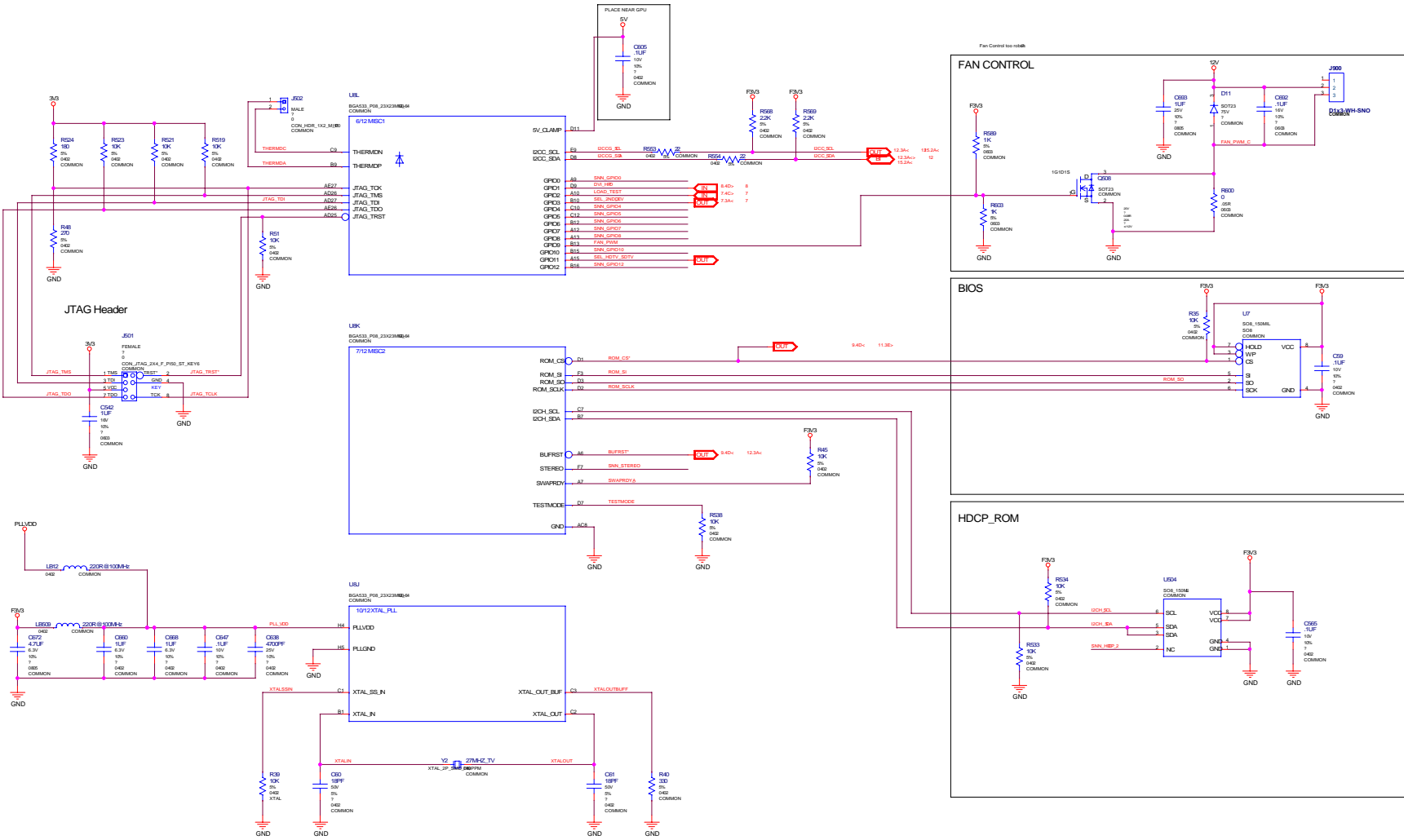
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ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	STRAPS, Mechanical Parts

XTAL, GPIO, BIOS, Fan Control, JTAG Headers

Net Name	NET_PHYSICAL_TYPE	NET_SPACING_RULE
XTALIN	0601_TRACE	0601
XTALOUT	0601_TRACE	0601
PLLED0	0601_TRACE	0601
PLLED1	0601_TRACE	0601
PLLED2	0601_TRACE	0601



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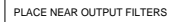
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PowerSupplyII: 5V, DDC5V, A3V3, F3V3, TMDS_PLLVDD

