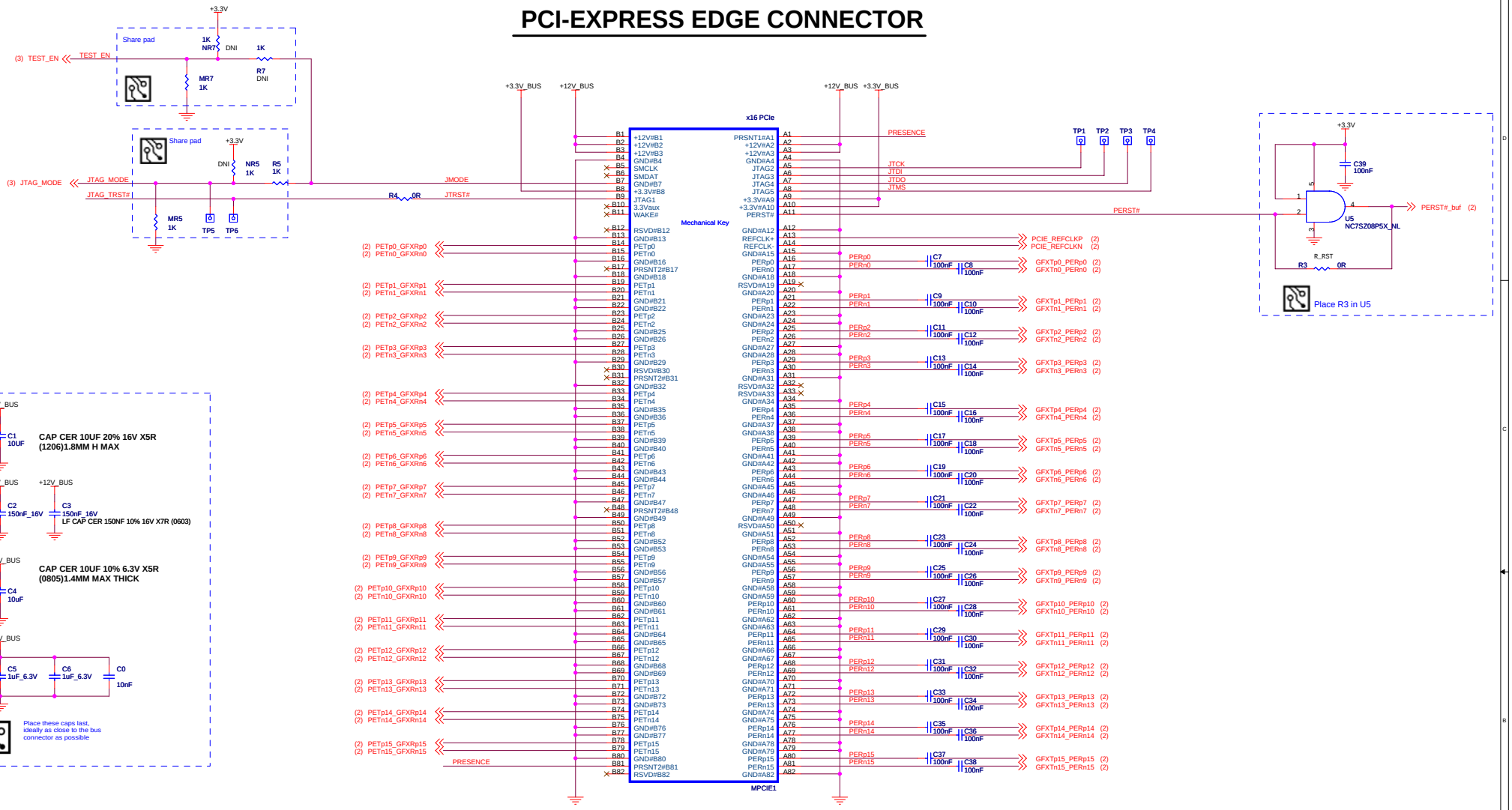
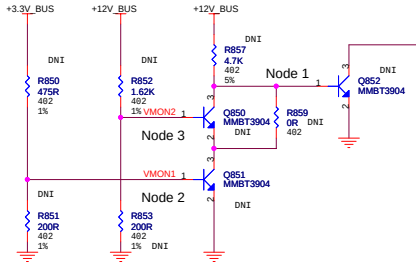
PCI-EXPRESS EDGE CONNECTOR





Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.

Node 1 When +12V_BUS ramps above min Vbe, SMPS_EN will be held low

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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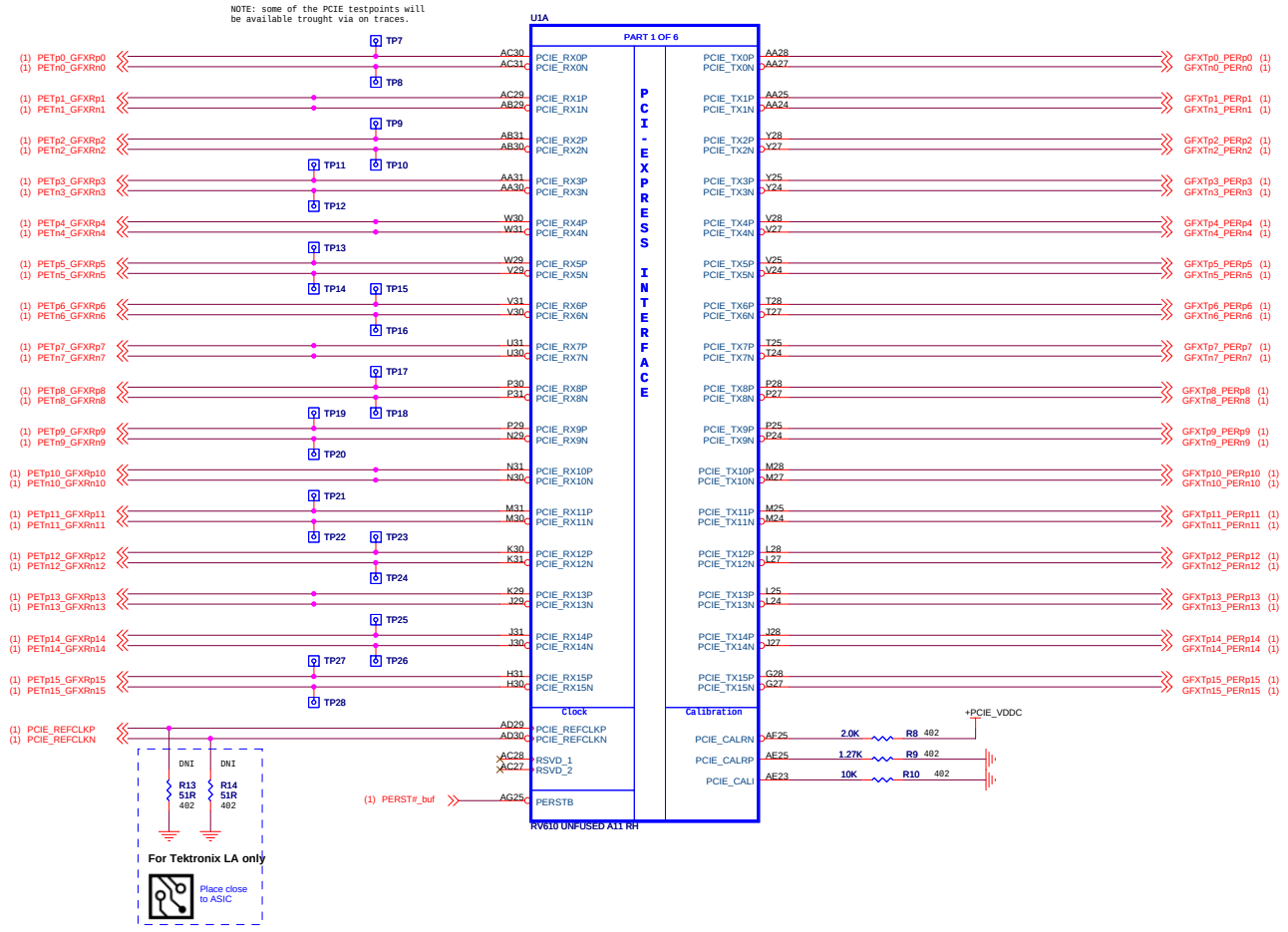

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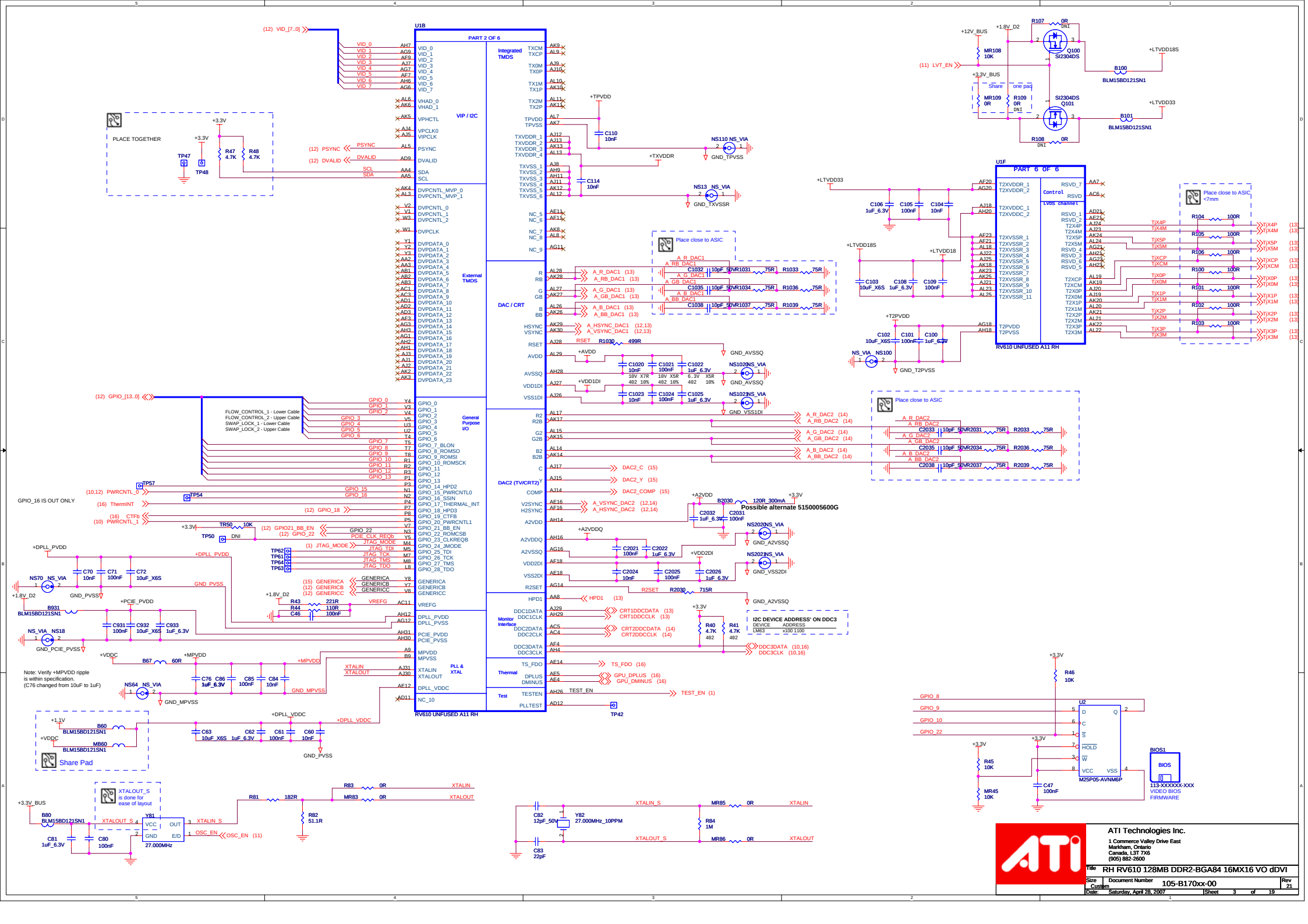
U1B
PART 2 OF 6
VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
VID_7
VIP / I2C
PSYNC
DVALID
SDA
SCL
DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
External TMDS
Integrated TMDS
DAC / CRT
DAC2 (TV/CRT2)
Monitor Interface
Thermal
Test
PLL & XTAL
General Purpose I/O
RV610 UNFUSED A11 RH
PLACE TOGETHER
TP47
TP48
R47 4.7K
R48 4.7K
Place close to ASIC
A_R_DAC1
A_RB_DAC1
A_G_DAC1
A_GB_DAC1
A_B_DAC1
A_BB_DAC1
C1032 10pF_50V
C1035 10pF_50V
C1038 10pF_50V
R1031 75R
R1034 75R
R1037 75R
R1033 75R
R1036 75R
R1039 75R
C110 10nF
C114 10nF
NS110 NS_VIA
NS13 NS_VIA
GND_TPVSS
GND_TXVSSR
+TXVDDR
+TPVDD
RSET R1030 499R
+AVDD
+VDD1DI
C1020 10nF
C1021 100nF
C1022 1uF_6.3V
C1023 10nF
C1024 100nF
C1025 1uF_6.3V
NS1020 NS_VIA
NS1021 NS_VIA
GND_AVSSQ
GND_VSS1DI
A_R_DAC2 (14)
A_RB_DAC2 (14)
A_G_DAC2 (14)
A_GB_DAC2 (14)
A_B_DAC2 (14)
A_BB_DAC2 (14)
C2033 10pF_50V
C2035 10pF_50V
C2038 10pF_50V
R2031 75R
R2034 75R
R2037 75R
R2033 75R
R2036 75R
R2039 75R
DAC2_C (15)
DAC2_Y (15)
DAC2_COMP (15)
A_VSYNC_DAC2 (12,14)
A_HSYNC_DAC2 (12,14)
+A2VDD
B2030 120R_300mA
Possible alternate 5150005600G
C2032 1uF_6.3V
C2031 100nF
NS2020 NS_VIA
GND_A2VSSQ
+A2VDDQ
C2021 100nF
C2022 1uF_6.3V
+VDD2DI
C2024 10nF
C2025 100nF
C2026 1uF_6.3V
NS2021 NS_VIA
GND_VSS2DI
R2SET R2030 715R
HPD1 (13)
CRT1DDCDATA (13)
CRT1DDCCLK (13)
CRT2DDCDATA (14)
CRT2DDCCLK (14)
DDC3DATA (10,16)
DDC3CLK (10,16)
R40 4.7K
R41 4.7K
I2C DEVICE ADDRESS' ON DDC3
DEVICE ADDRESS
LM63 x100 1100
TS_FDO (16)
GPU_DPLUS (16)
GPU_DMINUS (16)
TEST_EN
TEST_EN (1)
TP42
R107 0R DNI
Q100 SI2304DS
Q101 SI2304DS
R108 0R DNI
R109 0R DNI
MR108 10K
MR109 0R
+12V_BUS
+1.8V_D2
+3.3V_BUS
(11) LVT_EN
Share one pad
B100 BLM15BD121SN1
B101 BLM15BD121SN1
+LTVDD18S
+LTVDD33
U1F
PART 6 OF 6
Control
LVDS channel
T2VDDR_1
T2VDDR_2
T2VDDC_1
T2VDDC_2
T2VSSR_1
T2VSSR_2
T2VSSR_3
T2VSSR_4
T2VSSR_5
T2VSSR_6
T2VSSR_7
T2VSSR_8
T2VSSR_9
T2VSSR_10
T2VSSR_11
T2PVDD
T2PVSS
RSVD_7
RSVD
RSVD_1
RSVD_2
T2X4P
T2X4M
T2X5P
T2X5M
RSVD_4
RSVD_3
RSVD_6
RSVD_5
T2XCP
T2XCM
T2X0P
T2X0M
T2X1P
T2X1M
T2X2P
T2X2M
T2X3P
T2X3M
RV610 UNFUSED A11 RH
C106 1uF_6.3V
C105 100nF
C104 10nF
C103 10uF_X6S
C108 1uF_6.3V
C109 100nF
C102 10uF_X6S
C101 100nF
C100 1uF_6.3V
NS_VIA NS100
GND_T2PVSS
+T2PVDD
Place close to ASIC <7mm
TjX4P
TjX4M
TjX5P
TjX5M
TjXCP
TjXCM
TjX0P
TjX0M
TjX1P
TjX1M
TjX2P
TjX2M
TjX3P
TjX3M
R104 100R
R105 100R
R106 100R
R100 100R
R101 100R
R102 100R
R103 100R
(12) GPIO_[13..0]
FLOW_CONTROL_1 - Lower Cable
FLOW_CONTROL_2 - Upper Cable
SWAP_LOCK_1 - Lower Cable
SWAP_LOCK_2 - Upper Cable
GPIO_16 IS OUT ONLY
(10,12) PWRCNTL_0
(16) ThermINT
(16) CTFb
(10) PWRCNTL_1
(12) GPIO21_BB_EN
(12) GPIO_22
(1) JTAG_MODE
(15) GENERICA
(12) GENERICB
(12) GENERICC
TP57
TP54
TP50
TR50 10K
DNI
TP62
TP61
TP64
TP63
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
PCIE_CLK_REQb
JTAG_MODE
+DPLL_PVDD
+PCIE_PVDD
+VDDC
+MPVDD
+1.1V
+VDDC
GND_PVSS
GND_MPVSS
GND_PCIE_PVSS
B931 BLM15BD121SN1
B67 60R
B60 BLM15BD121SN1
MB60 BLM15BD121SN1
C70 10nF
C71 100nF
C72 10uF_X6S
C931 100nF
C932 10uF_X6S
C933 1uF_6.3V
C76 1uF_6.3V
C86
C85 100nF
C84 10nF
C63 10uF_X6S
C62 1uF_6.3V
C61 100nF
C60 10nF
NS70 NS_VIA
NS18
NS64 NS_VIA
R43 221R
R44 110R
C46 100nF
VREFG
Note: Verify +MPVDD ripple is within specification. (C76 changed from 10uF to 1uF)
Share Pad
XTALOUT_S is done for ease of layout
B80 BLM15BD121SN1
C81 1uF_6.3V
C80 100nF
Y81 27.000MHz
XTALIN_S
OSC_EN
OSC_EN (11)
R81 182R
R82 51.1R
R83 0R
MR83 0R
XTALIN
XTALOUT
C82 12pF_50V
C83 22pF
Y82 27.000MHz_10PPM
R84 1M
MR85 0R
MR86 0R
R46 10K
MR45 10K
R45 10K
U2
HOLD
VCC
VSS
M25P05-AVNM6P
C47 100nF
BIOS1
BIOS
113-XXXXXX-XXX
VIDEO BIOS FIRMWARE
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Title RH RV610 128MB DDR2-BGA84 16MX16 VO dDVI
Size Custom
Document Number 105-B170xx-00
Rev 21
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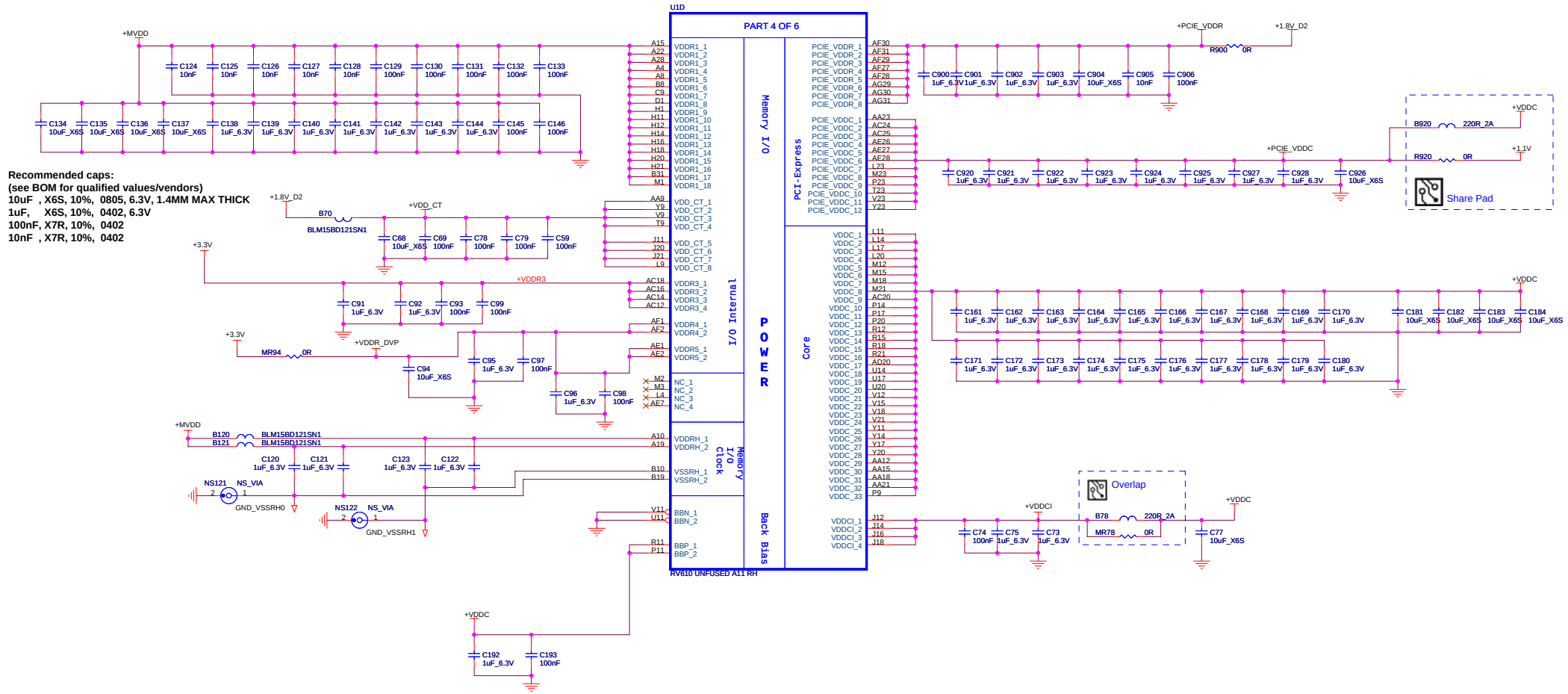

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Size: Custom	Document Number: 105-B170xx-00		Rev: 21
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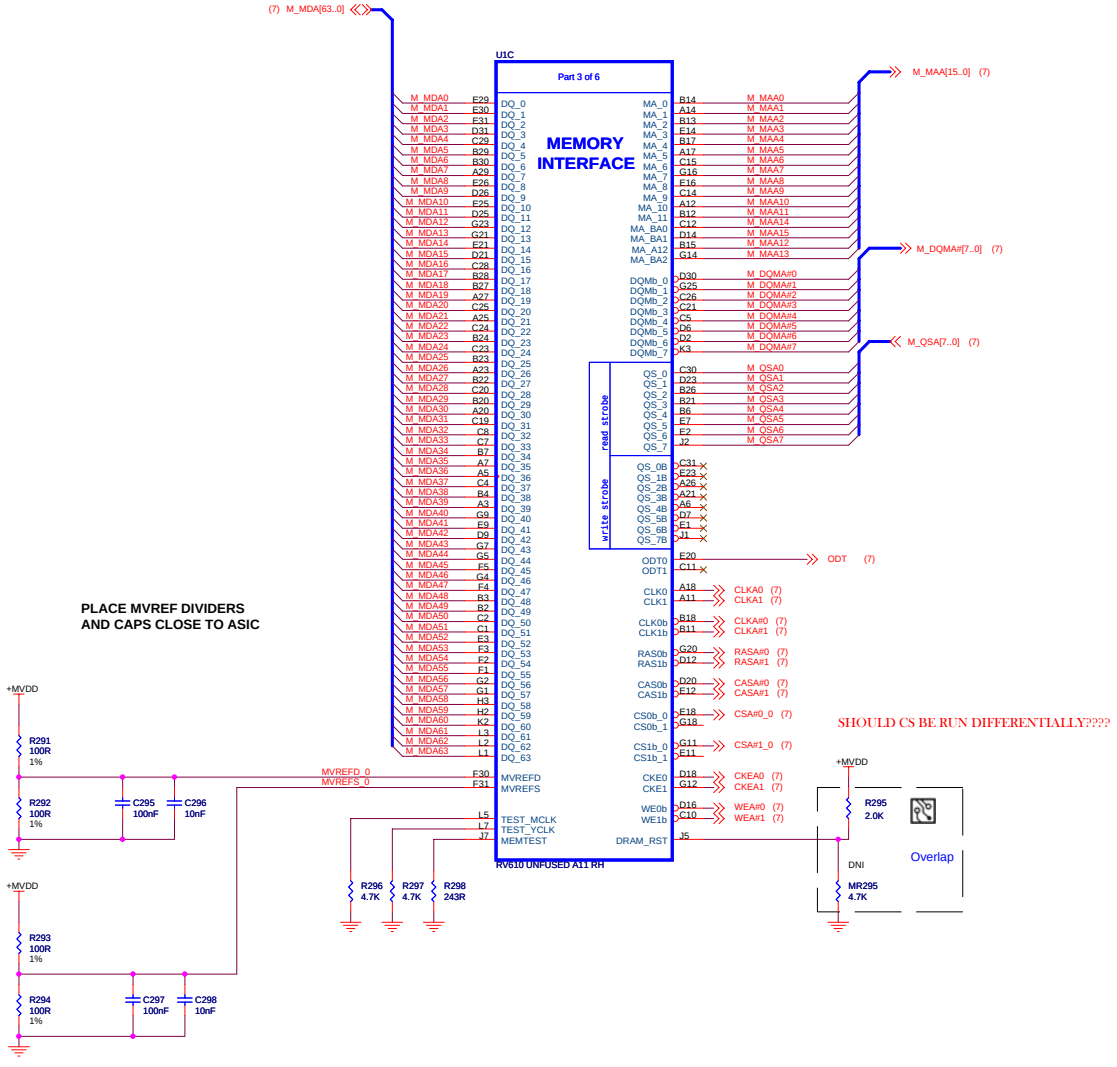

DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

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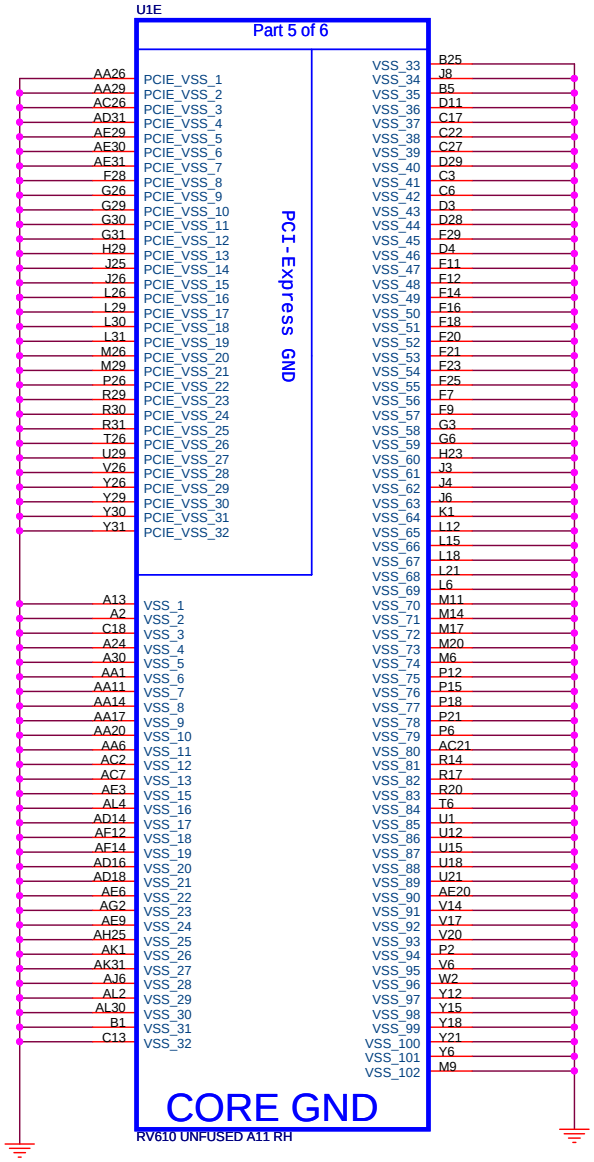

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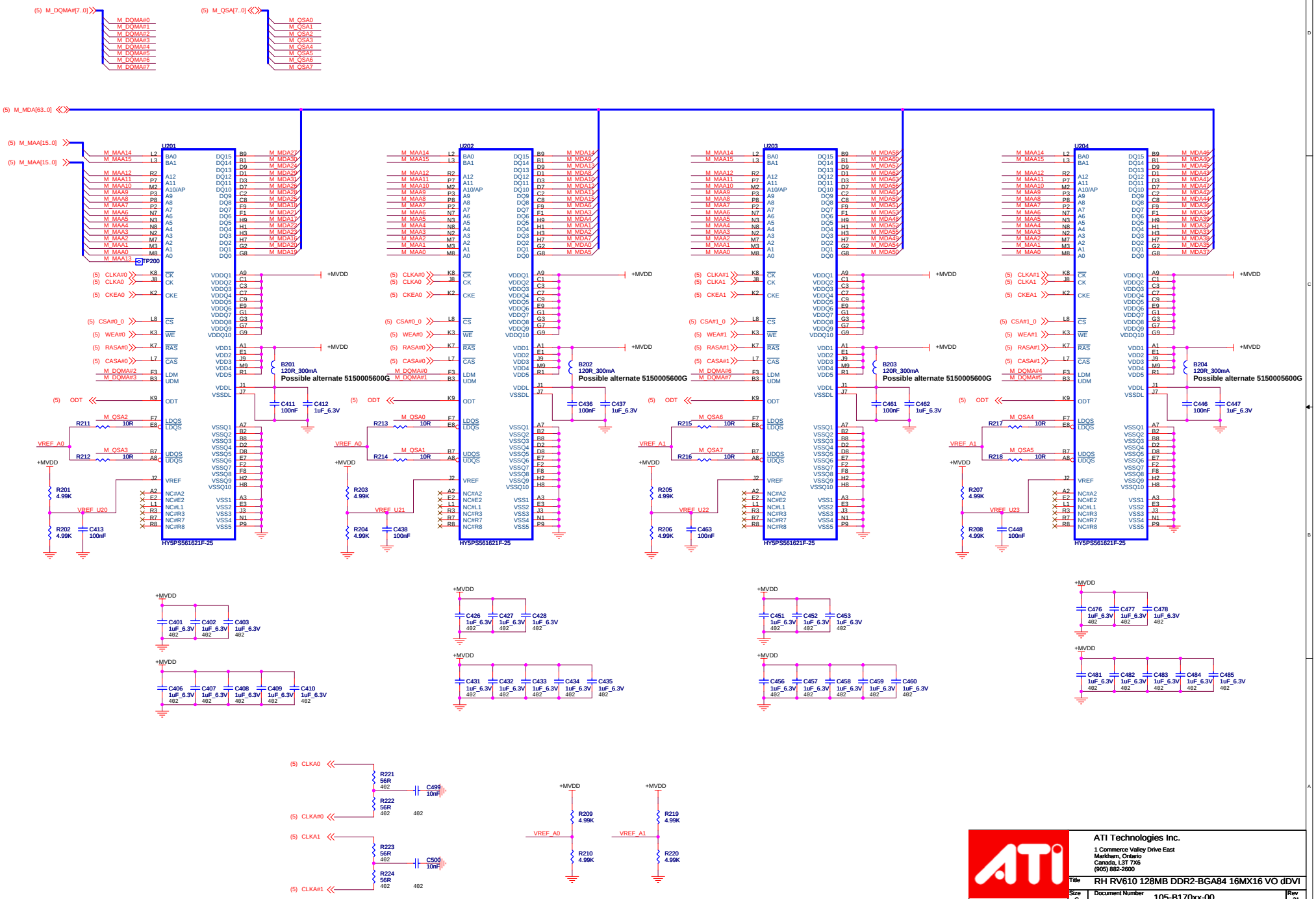
CHANNEL A: RANK 0 128MB DDR2



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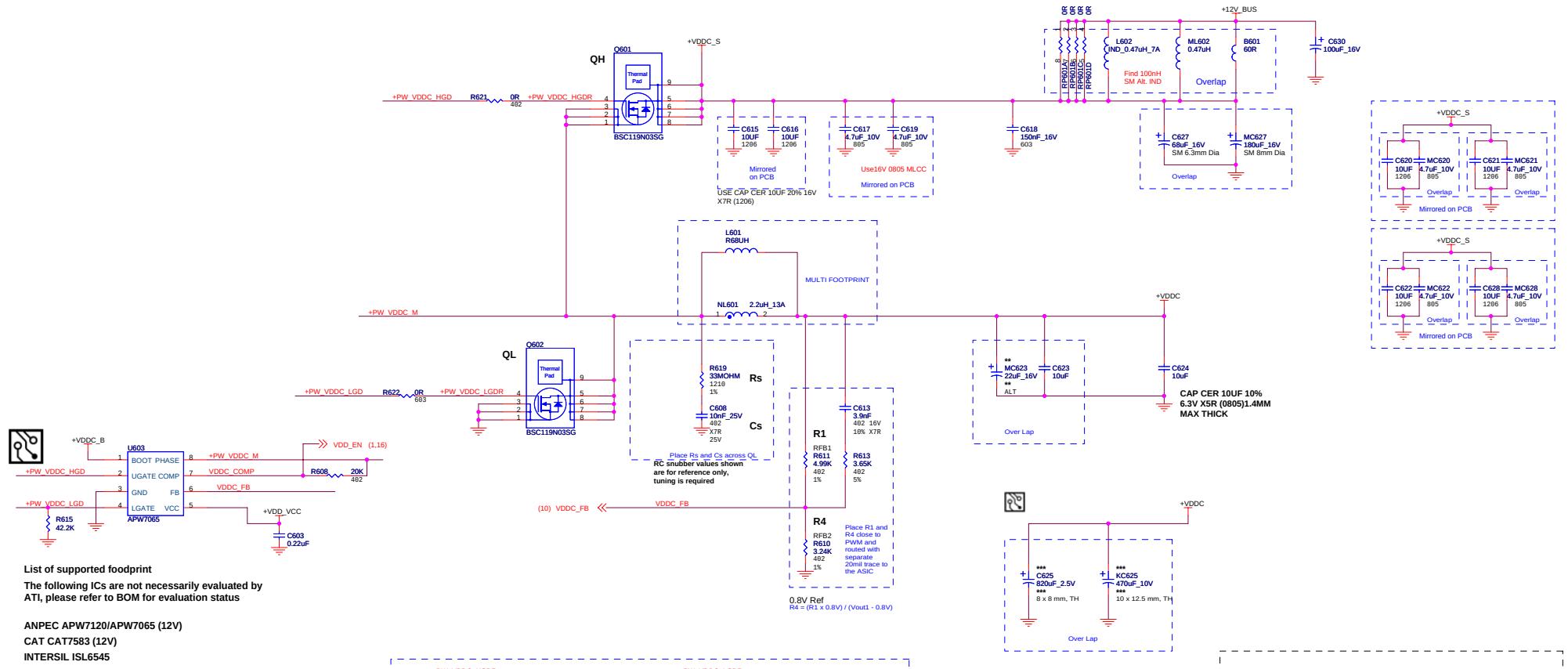
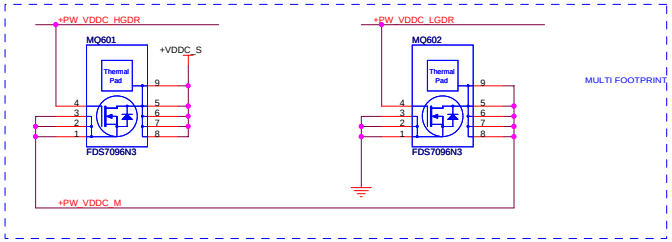


List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7120/APW7065 (12V)
CAT CAT7583 (12V)
INTERSIL ISL6545
NEXSEM NX2114/2307
RICHTEK RT9214/RT8101
OnSemi ON1582
uPI UP6101 (No Ext_Vref in)



Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

SMPS02- Regulator for VDDC

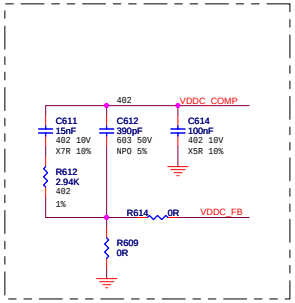
Vout = 0.9V ~ 1.1V

Part	Vout	RFB1	RFB2
0.8V Ref	1.1V (1.98V~2.08V)	200R p/n 3160200000G	511R p/n 3160511000G
	1.1V (1.10V~1.14V)	10K p/n 3160100200G	24.9K p/n 3160249200G

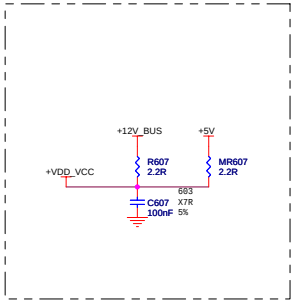
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

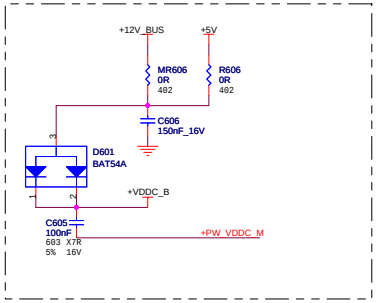
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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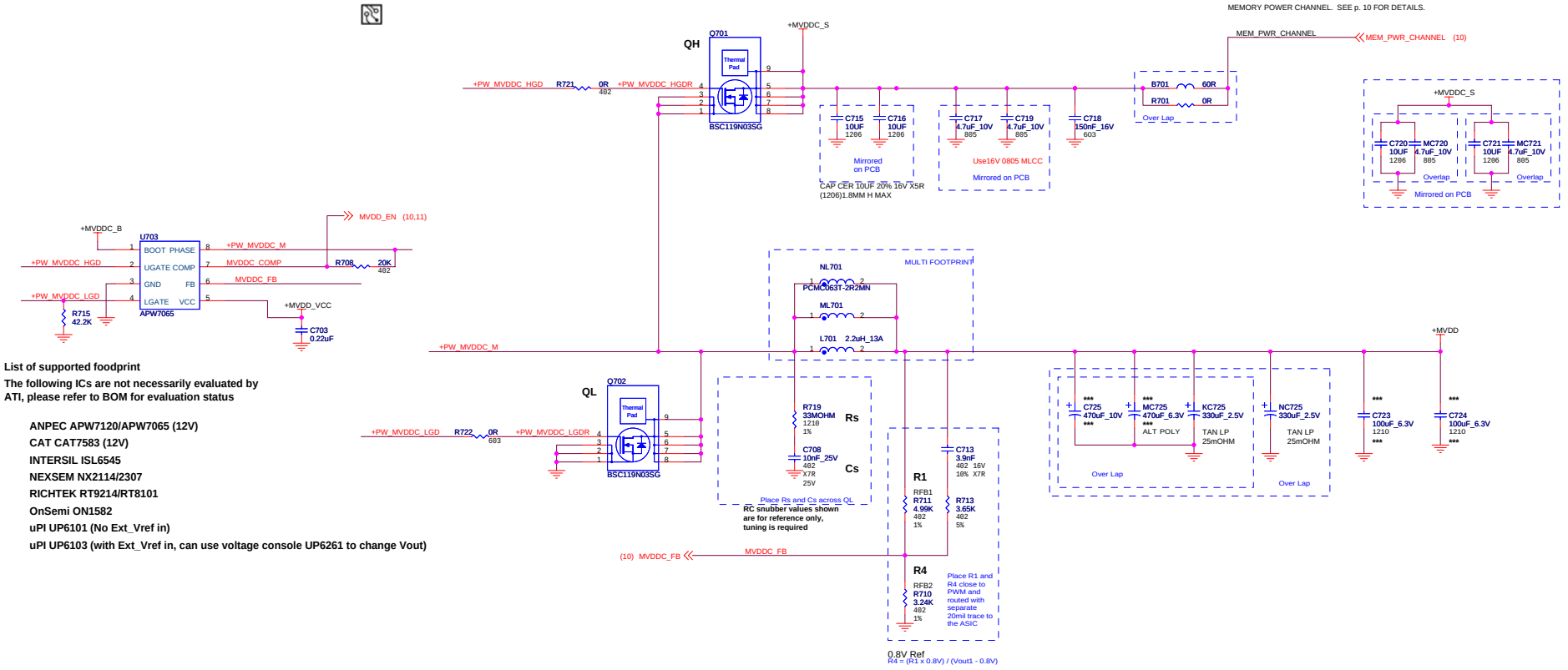

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- **CAT CAT7583 (12V)**
- **INTERSIL ISL6545**
- **NEXSEM NX2114/2307**
- **RICHTEK RT9214/RT8101**
- **OnSemi ON1582**
- **uPI UP6101 (No Ext_Vref in)**
- **uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**

SMPS02- Regulator for MVDD

Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G
	1.8V (1.78V~1.86V)	4.99K p/n 3160499100G	3.92K p/n 3160392100G

SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

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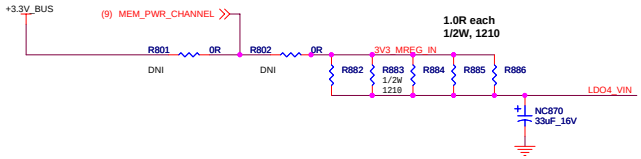
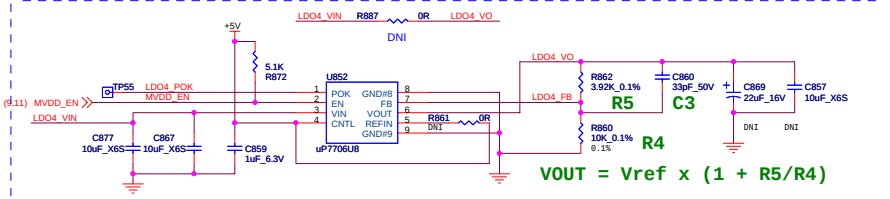
Linear Regulator for +MVDD
Vout = 1.8V ~ 2.1V
Iout = 2.75A MAX
P_REG = 1.35W
Tj(rise)max = 1.35Wx50C/W(50~70mm sq. Cu) = 67.5C

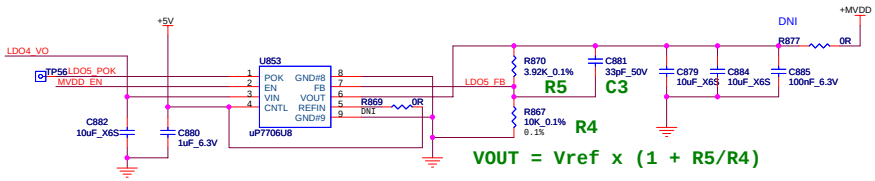
MEM PWR INPUT	INSTALL	DO NOT INSTALL
3.3V BUS (3V3_BUS_F)	R801 R802	R602 R701 or B701
12V (+VDDC_S)	R602 R701 or B701	R801 R802

Req = 1R/5 = 0.2R
P_Req = 0.2R * 2.75^2 = 1.5W
P_Reach = 1.5W/5 = 300mW < 500mW * 70%

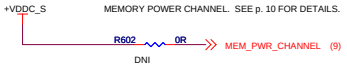
MEMORY POWER CHANNEL TO EASE LAYOUT CONGESTION OF LP BOARD. MEMORY POWER CHANNEL CAN BE USED TO DELIVER SOURCE VOLTAGE TO MVDD SMPS OR LINEAR REGULATORS (12V IN OR 3.3V IN)

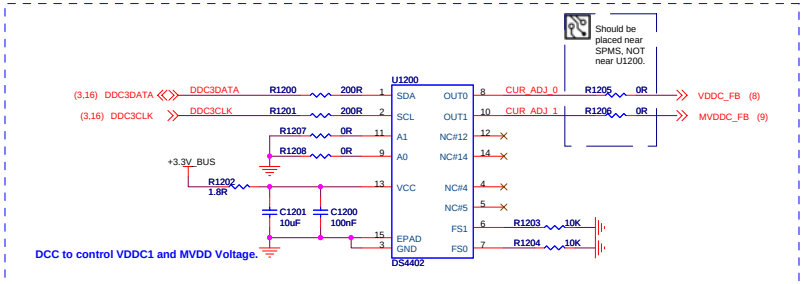






Memory Power Channel
Source Selection



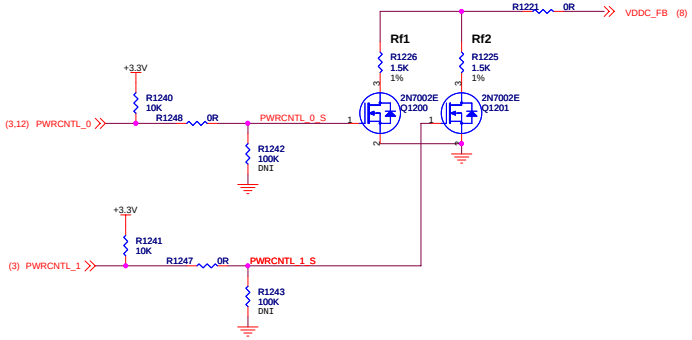


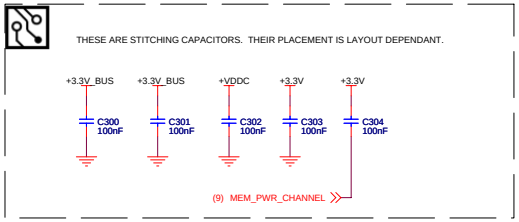
DCC to control VDDC1 and MVDD Voltage.

ASIC GPIO(x2) to control VDDC Voltage.

VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0	0				
0	1				
1	0				
1	1	1 0	1		Power-up Default





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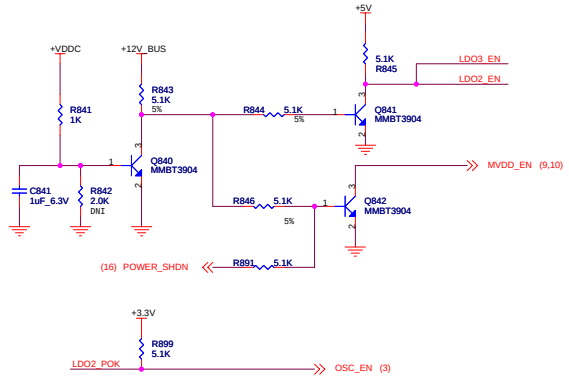
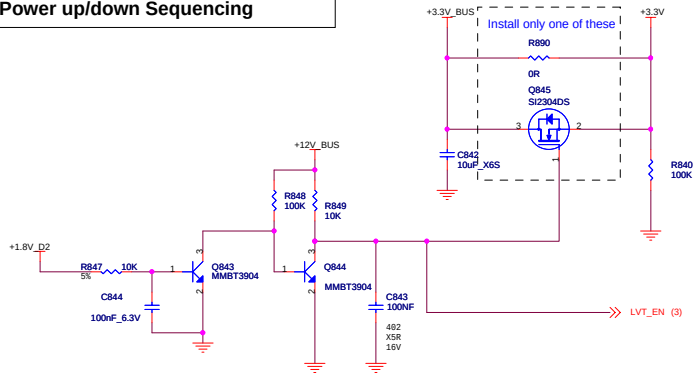
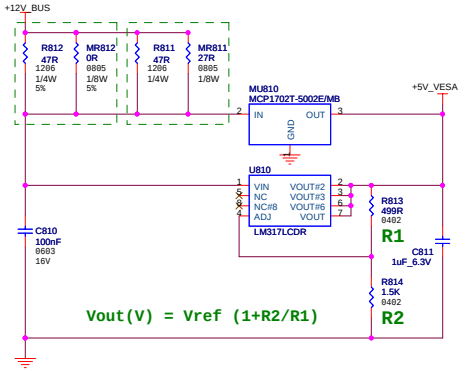
Power up/down Sequencing



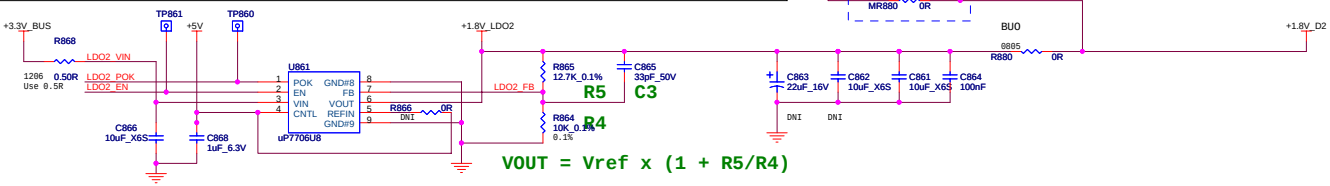


Regulators for +5V, +5V_VESA and +5V_VESA2

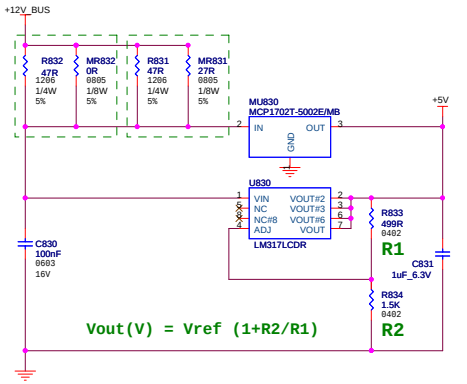


LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

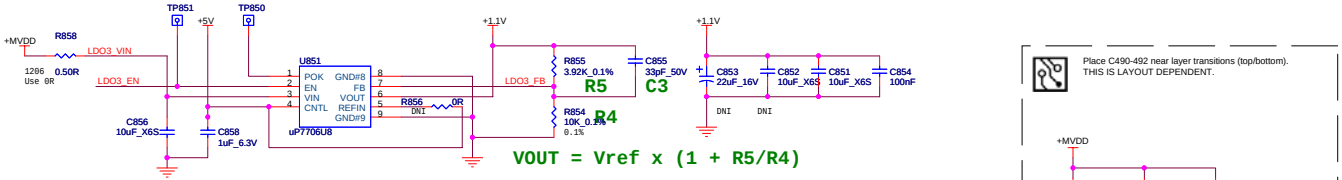


R868 (0.5R 1/2W or 0R 1206), R864, R865 & C865: To Be Verified



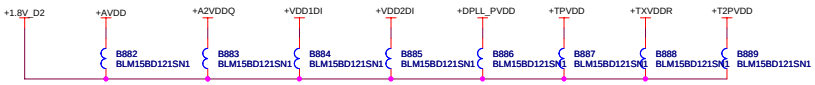
LDO #3: Vin = +1.45V to 2.1VMAX Vout = +1.1V +/- 2% Iout = 1.1A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



R854, R855 (3.92K) & C855: To Be Verified

Shared Power Rails



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PIN BASED STRAPS

+3.3V

DNI	MR50	10K	R50	10K	GPIO_0	GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
DNI	MR51	10K	R51	10K	GPIO_1	GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)
	MR52	10K	DNI R52	10K	GPIO_2	
	MR53	10K	DNI R53	10K	GPIO_3	GPIO(3:2) - ATI Internal Use Only - Reserved (Default: 00)
	MR54	10K	DNI R54	10K	GPIO_4	GPIO(4) - DEBUG_ACCESS ATI Internal Use Only - Reserved (Default: 0)
	MR55	10K	DNI R55	10K	GPIO_5	GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)
	MR56	10K	DNI R56	10K	GPIO_6	GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)
NTSC	MR57	10K	R57	10K	GPIO_7	GPIO(7) - TV OUT STANDARD (Jumper position overwrite resistor settings) 0 - PAL TVO (Jumper is closed) 1 - NTSC TVO (Jumper is open)
	MR58	10K	DNI R58	10K	GPIO_8	GPIO(8) - ATI Internal Use Only - Reserved (Default: 0)
	MR59	10K	R59	10K	GPIO_9	GPIO(9,13:11) - CONFIG[3..0] IF BIOS_ROM_EN=1 [default] (GPIO_22) tmel - AT25F512A (512 kbit)0010 AT25F1024A (1 Mbit)0011 ST Microelectronics- M25P05A (512 kbit) 0100 M25P10A (1 Mbit) 0101 M25P20 (2 Mbit) 0101 Chingis (formerly PMC) - Pm25LV512 (512 kbit) 0100 Pm25LV010 (1 Mbit) 0101 If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. (Config 3 = don care). x000 128MB x001 256MB x010 64MB x011 32MB x100 512MB x101 1GB x110 2GB x111 4GB
	MR63	10K	R63	10K	GPIO_13	
	MR62	10K	R62	10K	GPIO_12	
	MR61	10K	R61	10K	GPIO_11	
PSYNC						
DVALID						
	MR65	10K	DNI R65	10K	GENERICC → GENERICC (3)	GENERICC, GENERICB - ATI Internal Use Only - Reserved (Default: 0)
	MR64	10K	DNI R64	10K	GENERICB → GENERICB (3)	
	MR66	10K	R66	10K	A_VSYNC_DAC1 → A_VSYNC_DAC1 (3,13)	VSYNC - VIP_DEVICE_STRAP_EN 0: Slave VIP host port devices present (use if Theater is populated) 1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)
	MR67	10K	R67	10K	A_HSYNC_DAC1 → A_HSYNC_DAC1 (3,13)	HSYNC - ATI Internal Use Only - Reserved (Default 0)
	MR68	10K	DNI R68	10K	PSYNC	PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)
	MR69	10K	DNI R69	10K	GPIO21_BB_EN → GPIO21_BB_EN (3)	GPIO_21 - ATI Internal Use Only - Reserved (Default: 0)
	MR70	10K	DNI R70	10K	VID_0	VID_0 - ATI Internal Use Only - Reserved (Default: 0)
	MR71	10K	DNI R71	10K	VID_1	VID_1 - MSI_DIS (Default: 0)
	MR72	10K	DNI R72	10K	VID_2	VID_2 - ATI Internal Use Only - Reserved (Default: 0)
DNI	MR73	10K	R73	10K	VID_3	VID_3 - BIF_AUDIO_EN 0 - Disable HD Audio 1- Enable HD Audio
	MR74	10K	DNI R74	10K	VID_4	VID_4 - ATI Internal Use Only - Reserved (Default: 0)
	MR75	10K	DNI R75	10K	VID_5	VID_5 - 64BAR_EN_A (Default: 0) Enable 64-bit BARS
	MR76	10K	DNI R76	10K	VID_6	VID_6:7 - ATI Internal Use Only - Reserved (Default: 00)
	MR77	10K	DNI R77	10K	VID_7	
DNI	MR80	10K	R80	10K	A_VSYNC_DAC2 → A_VSYNC_DAC2 (3,14)	VSYNC - DDR2 VENDOR SELECT ATI Board Feature I (see GPIO_18)
	MR79	10K	DNI R79	10K	A_HSYNC_DAC2 → A_HSYNC_DAC2 (3,14)	HSYNC2 - ATI Internal Use Only - Reserved (Default: 0)
	MR60	10K	DNI R60	10K	DVALID	BIF_CLK_PM_EN 0 - Disable CLKREQ# power management capability 1 - Enable CLKREQ# power management capability
DNI	MR87	10K	DNI R87	10K	→ PWRCNTL_0 (3,10)	GPIO_15 - FOR FUTURE EXPANSION
DNI	MR46	10K	GPIO_22 → GPIO_22 (3)			GPIO_22_ROMCSb - Enable external BIOS ROM device (Default 1)
			R88	10K	→ GPIO_18 (3)	
DNI	MR88	10K				GPIO_18 - DDR2 MEM VENDOR [V2SYNC:GPIO_18] ATI Board Feature I QUIMONDA [0:0] HYNIX [0:1] SAMSUNG [1:0]

(3) VID_[7..0]

VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
VID_7

(3) GPIO_[13..0]

GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground — High logic voltage

Signal

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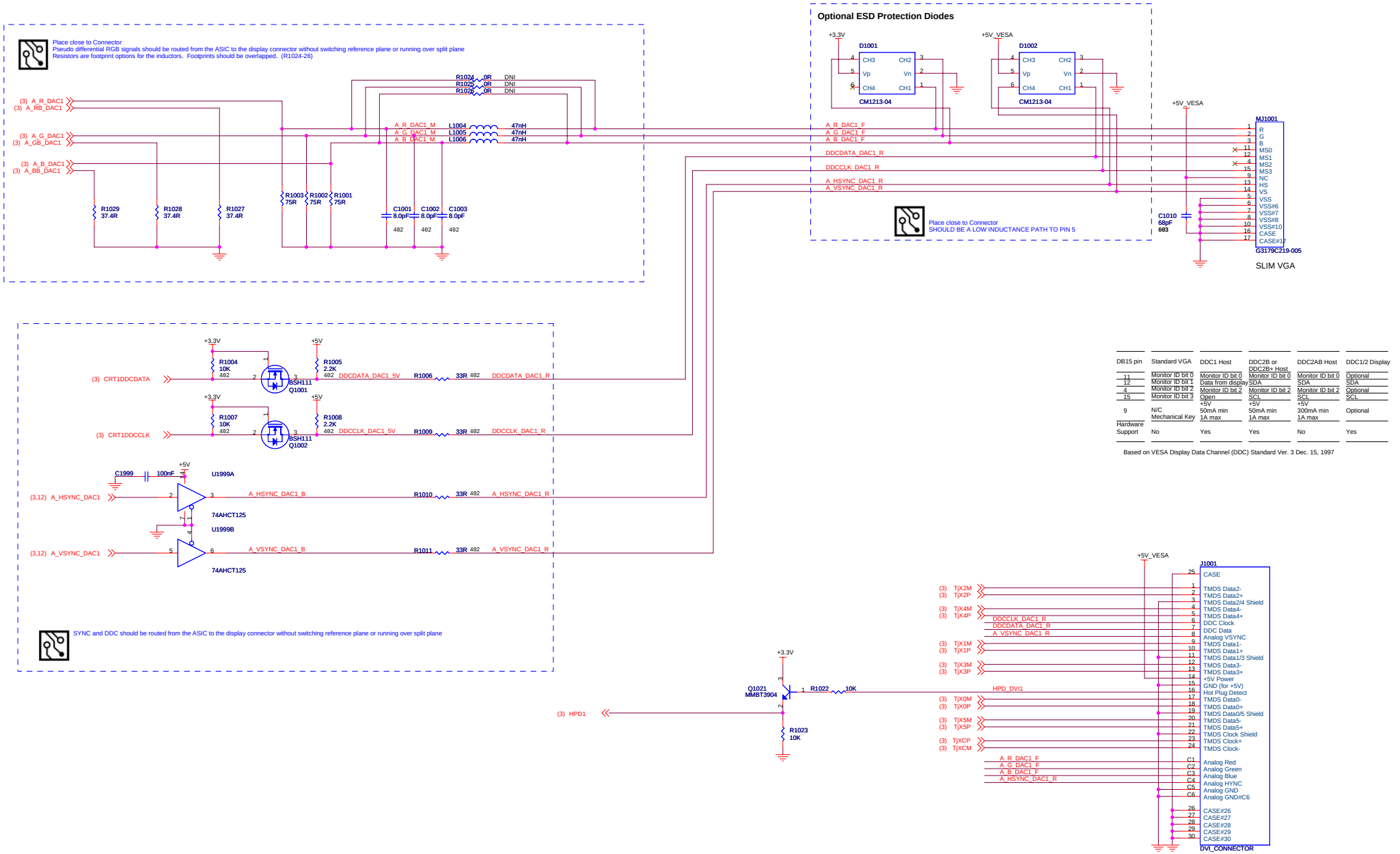

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

TMDS_2(Daul_Link) + DAC_1-CRT

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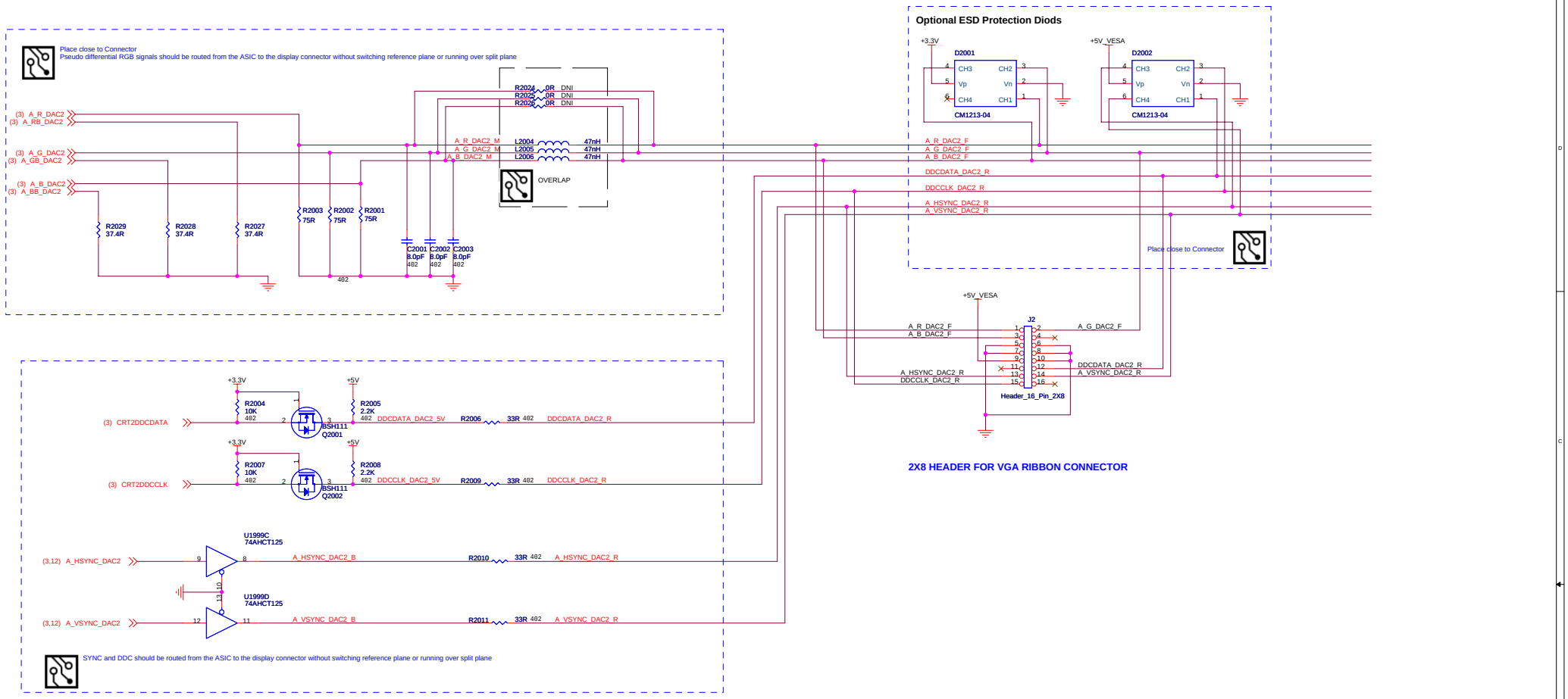

2X8 HEADER FOR VGA RIBBON CONNECTOR

TMDS_1(Single_Link) + DAC_2-CRT

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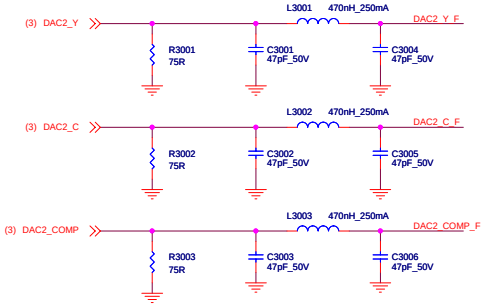

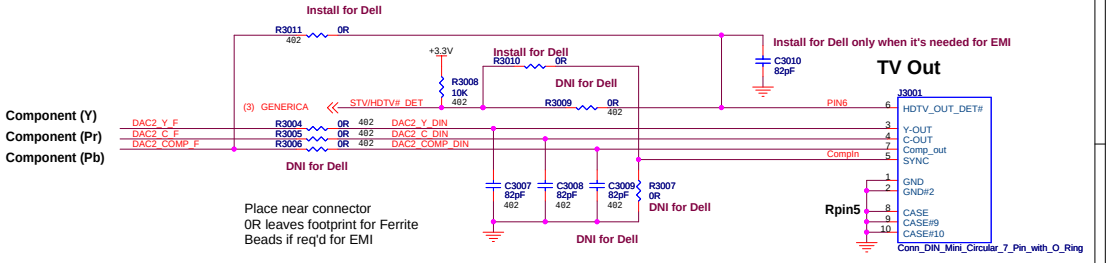

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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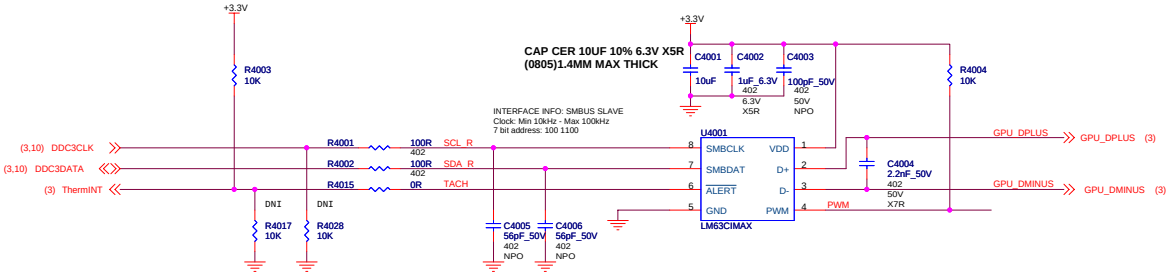
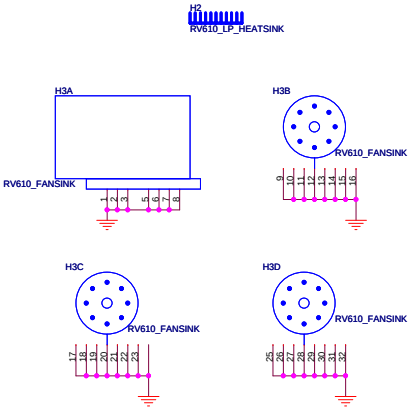
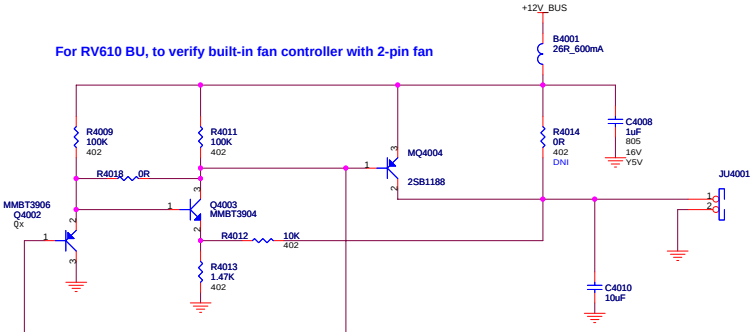
LM63 is for RV610 BU, until built-in fan controller is verified.

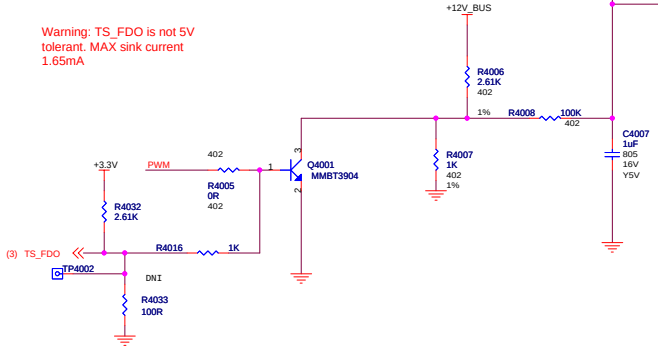




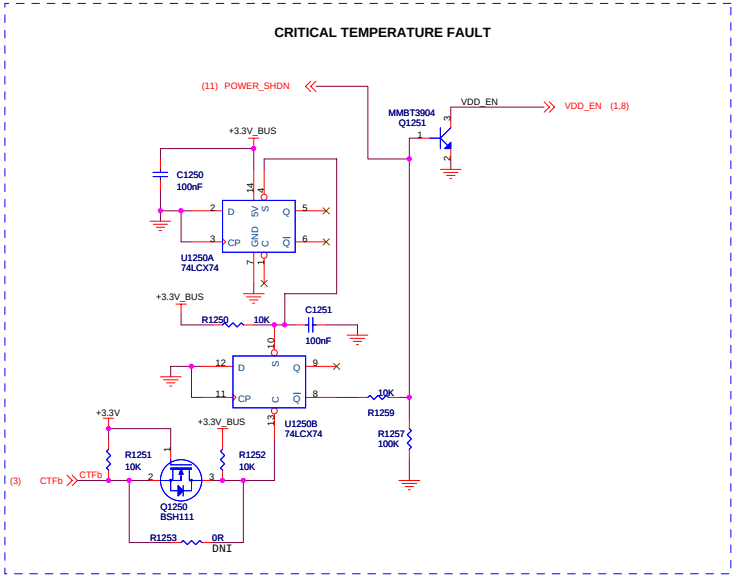
For RV610 BU, to verify built-in fan controller with 2-pin fan



Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA



CRITICAL TEMPERATURE FAULT



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DVI/VGA SCREWS

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

MT1
MT_Hole_0.136_in.
DNI

MT2
MT_Hole_0.136_in_6VIA
DNI

ASSY1
BRACKET
8020040100G

ASSY2
BRACKET
LP
8020040400G

<Variant Name>

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<variant Name>

Title

RH RV610 128MB DDR2-BGA84 16MX16 VO dDVI

Schematic No.

105-B170xx-00

Date:

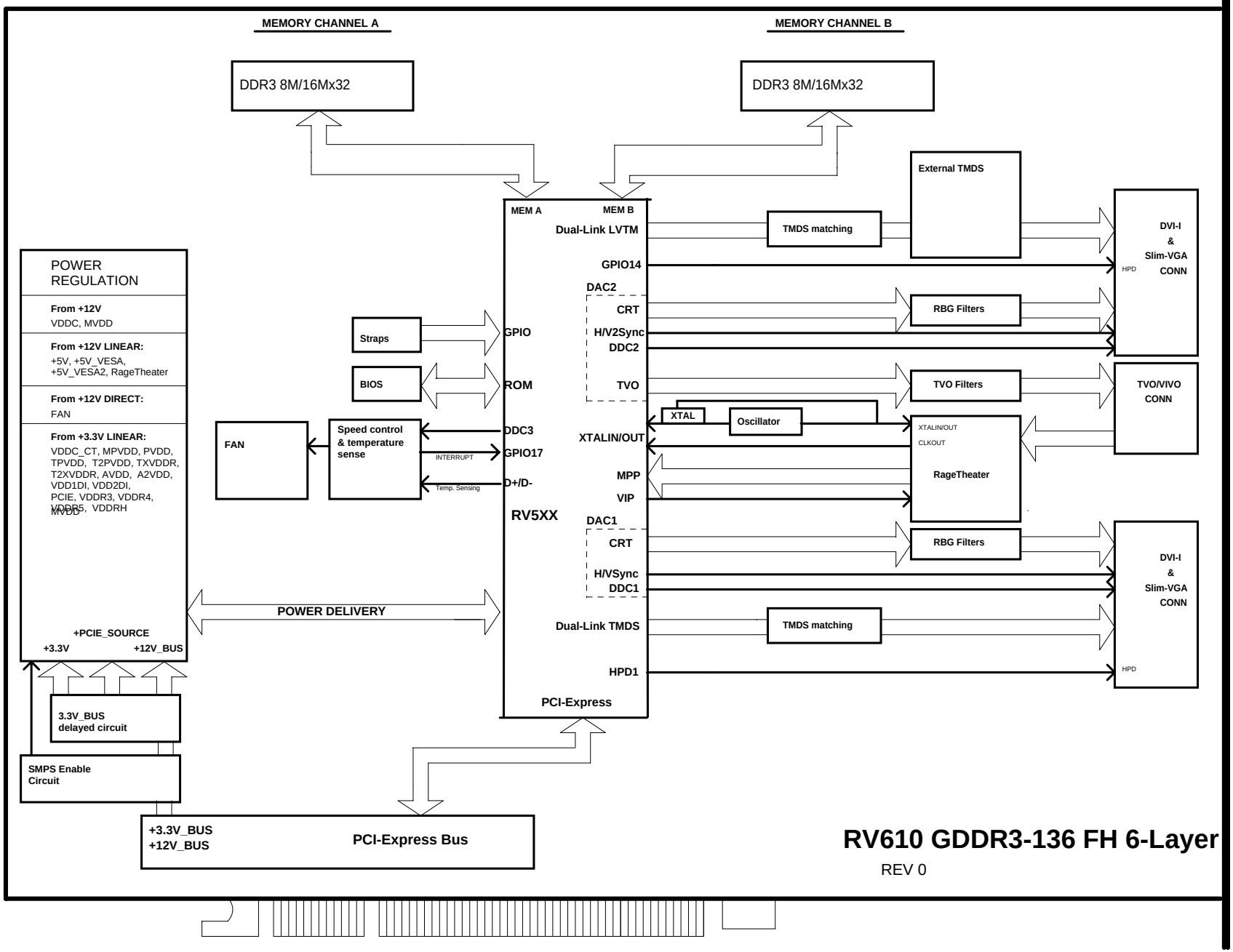
Saturday, April 28, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.

Rev 21

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
014	00B	2007.02.22	RM C890/MC890, RM B801/L801/ML801
015	00B	2007.02.27	ADD R4010 FOR FAN CIRCUIT. ADD STITCHING CAPS C300, C301, C302, C303
016	00B	2007.02.28	CORRECT "300" TO C300; ADD C304, CHNG C301;
017	00B	2007.03.06	POWER SUPPLY CHANGES: ADD MC627, R615, R609, R715, R709, R714, R614; REMOVE MC630, MC624;
018	00B	2007.03.06	DUE TO LAYOUT CONSTRAINTS: RM ML601. CHANGE C627, MC627.
019	00C	2007.04.17	REMOVE R90, Q90 (A12+ ASIC REMOVES NEED FOR THESE PARTS); REMOVE C850 (IS NOT POPULATED ON ANY BOM - WILL CAUSE VDDC TO BE UNSTABLE); ADD C4010 (FOR FAN SPIN UP);
020	00C	2007.04.19	ADD C490, C491, C492 FOR POSSIBLE MEMORY SIGNAL INTEGRITY/EMI IMPROVEMENTS (PER EMI TEAM);
021	00	2007.04.25	NO NETLIST/LAYOUT CHANGES. SCHEMATIC UPDATE NOTES p.12 (V2SYNC/GPIO_18 CLARIFICATION)



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