P654 - GT200/NVIO2

P654, GT200-100, 896MB/1792MB - GDDR3 BGA136 16M/32Mx32

DVI-I + DVI-I/DP + HD/SD/TVout, SPDIF, Dual SLI

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SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10654-BASE-A02	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10654-0000-000	DT, GT200-100, 550/1350/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I + HDTV
2	SKU0001	600-10654-0001-000	DT, GT200-100, 550/1350/1000, 896MB - 16Mx32 GDDR3, DVI-I + DP + HDTV
3	SKU0051	600-10654-0051-300	DT, GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	DT, GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Title Page

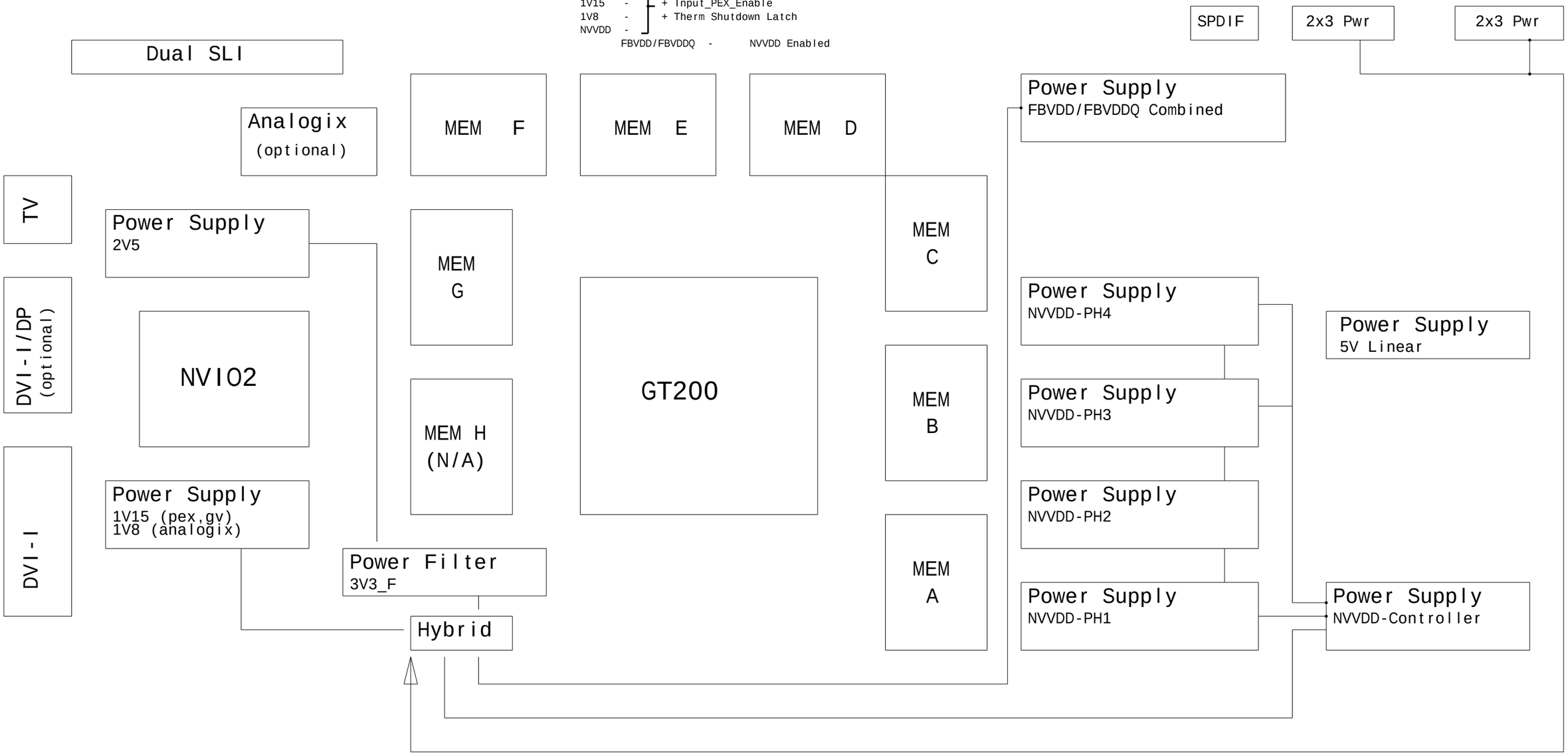
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	1 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Block Diagram

Power Sequence

5V	- Always On	
3V3	- Always On	
12V_F	- Always On	
12V_PEX6_F1	- Always On	
12V_PEX6_F2	- Always On	
3V3_DP	- Always On	
3V3_F	-	Hybrid Enable
2V5	-	+ Input_PEX_Enable
1V15	-	+ Therm Shutdown Latch
1V8	-	
NVVDD	-	
FBVDD/FBVDDQ	-	NVVDD Enabled



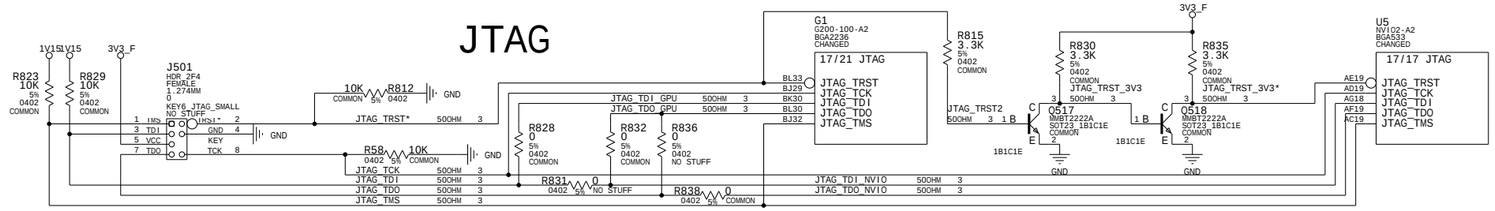
ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Block Diagram

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	2 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

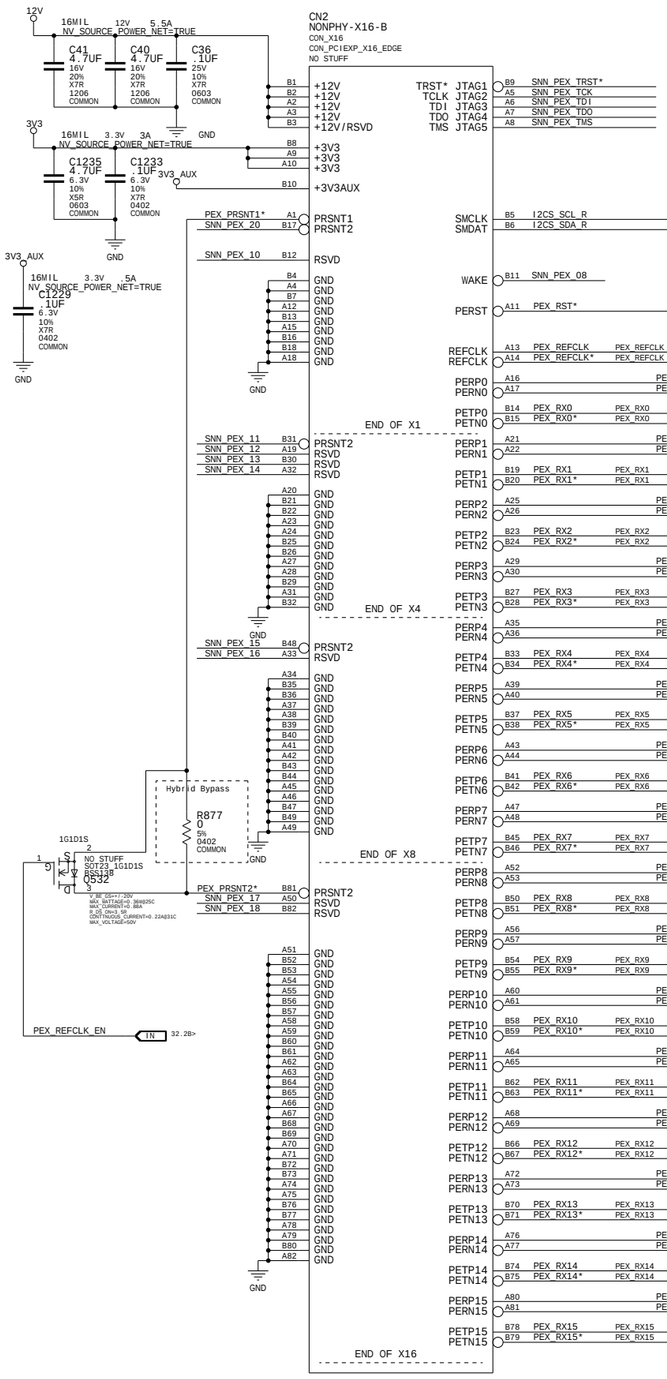
PCI Express / JTAG

JTAG

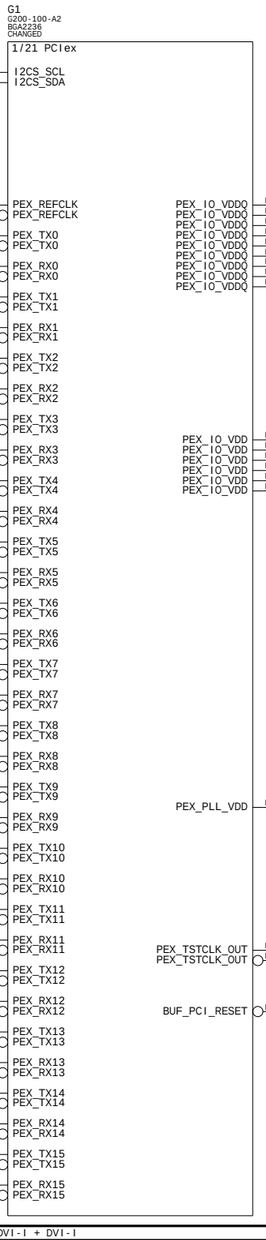


CN2 NONPHY-X16-B

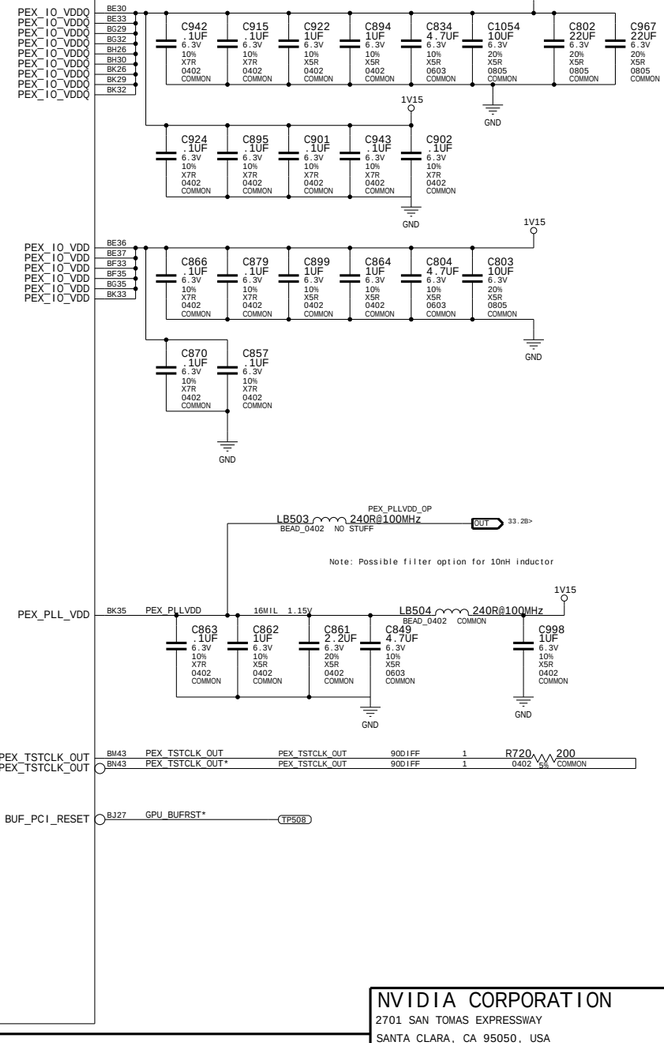
CON_X16
CON_PCIEXP_X16_EDGE
NO STUFF



G1 G200-100-A2 BGA2236 CHANGED — 1/21 PCIex



1V15 rails



PEX_PLL_VDD

PEX_TSTCLK_OUT — R720 200 0402 5% COMMON

BUF_PCI_RESET — GPU_BUFRST* — TP508

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	PCI Express / JTAG

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	3 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Framebuffer A,B: GPU Section + Calibration

G1
G200-100-A2
BGA2236
CHANGED

2/21 MEM_A

FBA_D<0>	BL39	FBA_D0	FBA_D32	BK50	FBA_D<32>
FBA_D<1>	BK38	FBA_D1	FBA_D33	BJ51	FBA_D<33>
FBA_D<2>	BK39	FBA_D2	FBA_D34	BH51	FBA_D<34>
FBA_D<3>	BJ39	FBA_D3	FBA_D35	BH50	FBA_D<35>
FBA_D<4>	BK42	FBA_D4	FBA_D36	BH49	FBA_D<36>
FBA_D<5>	BJ41	FBA_D5	FBA_D37	BG49	FBA_D<37>
FBA_D<6>	BJ42	FBA_D6	FBA_D38	BG50	FBA_D<38>
FBA_D<7>	BH42	FBA_D7	FBA_D39	BG52	FBA_D<39>
FBA_D<8>	BH44	FBA_D8	FBA_D40	BD49	FBA_D<40>
FBA_D<9>	BH45	FBA_D9	FBA_D41	BC48	FBA_D<41>
FBA_D<10>	BL43	FBA_D10	FBA_D42	BD47	FBA_D<42>
FBA_D<11>	BK44	FBA_D11	FBA_D43	BC47	FBA_D<43>
FBA_D<12>	BK45	FBA_D12	FBA_D44	BA47	FBA_D<44>
FBA_D<13>	BJ45	FBA_D13	FBA_D45	BA46	FBA_D<45>
FBA_D<14>	BJ44	FBA_D14	FBA_D46	AY47	FBA_D<46>
FBA_D<15>	BH46	FBA_D15	FBA_D47	AY48	FBA_D<47>
FBA_D<16>	BN46	FBA_D16	FBA_D48	BB52	FBA_D<48>
FBA_D<17>	BM46	FBA_D17	FBA_D49	BE50	FBA_D<49>
FBA_D<18>	BM47	FBA_D18	FBA_D50	BB51	FBA_D<50>
FBA_D<19>	BL48	FBA_D19	FBA_D51	BE51	FBA_D<51>
FBA_D<20>	BL49	FBA_D20	FBA_D52	BC52	FBA_D<52>
FBA_D<21>	BM51	FBA_D21	FBA_D53	BC51	FBA_D<53>
FBA_D<22>	BL51	FBA_D22	FBA_D54	BF52	FBA_D<54>
FBA_D<23>	BL52	FBA_D23	FBA_D55	BE52	FBA_D<55>
FBA_D<24>	BK47	FBA_D24	FBA_D56	BA52	FBA_D<56>
FBA_D<25>	BJ47	FBA_D25	FBA_D57	BA50	FBA_D<57>
FBA_D<26>	BH48	FBA_D26	FBA_D58	BA49	FBA_D<58>
FBA_D<27>	BG46	FBA_D27	FBA_D59	AW49	FBA_D<59>
FBA_D<28>	BG47	FBA_D28	FBA_D60	AW50	FBA_D<60>
FBA_D<29>	BH48	FBA_D29	FBA_D61	AW51	FBA_D<61>
FBA_D<30>	BF48	FBA_D30	FBA_D62	AV50	FBA_D<62>
FBA_D<31>	BE47	FBA_D31	FBA_D63	AV49	FBA_D<63>
FBA_DQM0	BH39	FBA_DQM0	FBA_DQM4	BH52	FBA_DQM4
FBA_DQM1	BM44	FBA_DQM1	FBA_DQM5	BB47	FBA_DQM5
FBA_DQM2	BM48	FBA_DQM2	FBA_DQM6	BD50	FBA_DQM6
FBA_DQM3	BF47	FBA_DQM3	FBA_DQM7	AW52	FBA_DQM7
FBA_DQS_RN0	BL42	FBA_DQS_RN0	FBA_DQS_RN4	BK52	FBA_DQS_RN4
FBA_DQS_RN1	BP45	FBA_DQS_RN1	FBA_DQS_RN5	BB49	FBA_DQS_RN5
FBA_DQS_RN2	BM50	FBA_DQS_RN2	FBA_DQS_RN6	BC53	FBA_DQS_RN6
FBA_DQS_RN3	BK48	FBA_DQS_RN3	FBA_DQS_RN7	AY53	FBA_DQS_RN7
FBA_DQS_WP0	BK41	FBA_DQS_WP0	FBA_DQS_WP4	BJ52	FBA_DQS_WP4
FBA_DQS_WP1	BN45	FBA_DQS_WP1	FBA_DQS_WP5	BB48	FBA_DQS_WP5
FBA_DQS_WP2	BM49	FBA_DQS_WP2	FBA_DQS_WP6	BD52	FBA_DQS_WP6
FBA_DQS_WP3	BJ48	FBA_DQS_WP3	FBA_DQS_WP7	AY52	FBA_DQS_WP7
FBA_CMD<0>	BR47	FBA_CMD0			
FBA_CMD<1>	BN47	FBA_CMD1			
FBA_CMD<2>	BR48	FBA_CMD2			
FBA_CMD<3>	BP48	FBA_CMD3			
FBA_CMD<4>	BN48	FBA_CMD4			
FBA_CMD<5>	BN49	FBA_CMD5			
FBA_CMD<6>	BR50	FBA_CMD6			
FBA_CMD<7>	BN50	FBA_CMD7			
FBA_CMD<8>	BR51	FBA_CMD8			
FBA_CMD<9>	BP51	FBA_CMD9			
FBA_CMD<10>	BN51	FBA_CMD10			
FBA_CMD<11>	BP53	FBA_CMD11			
FBA_CMD<12>	BN52	FBA_CMD12			
FBA_CMD<13>	BN54	FBA_CMD13			
FBA_CMD<14>	BM53	FBA_CMD14			
FBA_CMD<15>	BL55	FBA_CMD15			
FBA_CMD<16>	BL53	FBA_CMD16			
FBA_CMD<17>	BL54	FBA_CMD17			
FBA_CMD<18>	BK53	FBA_CMD18			
FBA_CMD<19>	BK55	FBA_CMD19			
FBA_CMD<20>	BJ53	FBA_CMD20			
FBA_CMD<21>	BH53	FBA_CMD21			
SNN_FBA_CMD<22>	BH54	FBA_CMD22			
FBA_CMD<23>	BH55	FBA_CMD23			
FBA_CMD<24>	BG53	FBA_CMD24			
FBA_CMD<25>	BG55	FBA_CMD25			
FBA_CMD<26>	BF53	FBA_CMD26			
FBA_CMD<27>	BE53	FBA_CMD27			
FBA_CMD<28>	BE54	FBA_CMD28			
SNN_FBA_CMD<29>	BE55	FBA_CMD29			
SNN_FBA_CMD<30>	BD53	FBA_CMD30			
SNN_FBA_CMD<31>	BD55	FBA_CMD31			
SNN_FBA_CMD<32>	BB53	FBA_CMD32			
FBA0_CLK0	BF45	FBA0_CLK0	FBA1_CLK0	BB45	FBA1_CLK0
FBA0_CLK0*	BF44	FBA0_CLK0	FBA1_CLK0*	BB46	FBA1_CLK0*
SNN_FBA0_CLK1	BF41	FBA0_CLK1	SNN_FBA1_CLK1	AW45	SNN_FBA1_CLK1
SNN_FBA0_CLK1*	BF42	FBA0_CLK1	SNN_FBA1_CLK1*	AY45	SNN_FBA1_CLK1*

FBA_DEBUG — BF39 FBAB_REFCLK (IN 19.5D>) / BE39 FBAB_REFCLK* (IN 19.5D>)

FBAB_MPLL_AVDD — BC45 FBABCD_MPLL_AVDD — 16MIL 1.15V 0.042A (OUT 5.4C<) — R502 10nH 0402 COMMON — 1V15

C826 1UF 6.3V 10% X7R 0402 COMMON
C810 2.2UF 6.3V 20% X5R 0402 COMMON
C816 4.7UF 6.3V 20% X5R 0603 COMMON
C847 1UF 6.3V 10% X5R 0402 COMMON
(GND)

FBVDDQ — R726 60.4 1% 0402 NO STUFF

G1
G200-100-A2
BGA2236
CHANGED

3/21 MEM_B

FBB_D<0>	AV52	FBB_D0	FBB_D32	AJ50	FBB_D<32>
FBB_D<1>	AU51	FBB_D1	FBB_D33	AJ52	FBB_D<33>
FBB_D<2>	AT52	FBB_D2	FBB_D34	AH52	FBB_D<34>
FBB_D<3>	AT50	FBB_D3	FBB_D35	AG52	FBB_D<35>
FBB_D<4>	AT49	FBB_D4	FBB_D36	AF52	FBB_D<36>
FBB_D<5>	AR49	FBB_D5	FBB_D37	AF51	FBB_D<37>
FBB_D<6>	AR50	FBB_D6	FBB_D38	AF50	FBB_D<38>
FBB_D<7>	AR52	FBB_D7	FBB_D39	AF49	FBB_D<39>
FBB_D<8>	AW48	FBB_D8	FBB_D40	AJ48	FBB_D<40>
FBB_D<9>	AV46	FBB_D9	FBB_D41	AJ47	FBB_D<41>
FBB_D<10>	AU47	FBB_D10	FBB_D42	AH47	FBB_D<42>
FBB_D<11>	AT47	FBB_D11	FBB_D43	AG47	FBB_D<43>
FBB_D<12>	AT46	FBB_D12	FBB_D44	AF48	FBB_D<44>
FBB_D<13>	AR46	FBB_D13	FBB_D45	AE48	FBB_D<45>
FBB_D<14>	AP47	FBB_D14	FBB_D46	AE47	FBB_D<46>
FBB_D<15>	AP48	FBB_D15	FBB_D47	AD47	FBB_D<47>
FBB_D<16>	AP52	FBB_D16	FBB_D48	AE53	FBB_D<48>
FBB_D<17>	AN52	FBB_D17	FBB_D49	AE52	FBB_D<49>
FBB_D<18>	AN51	FBB_D18	FBB_D50	AE51	FBB_D<50>
FBB_D<19>	AN50	FBB_D19	FBB_D51	AD52	FBB_D<51>
FBB_D<20>	AK49	FBB_D20	FBB_D52	AC52	FBB_D<52>
FBB_D<21>	AK50	FBB_D21	FBB_D53	AC51	FBB_D<53>
FBB_D<22>	AK51	FBB_D22	FBB_D54	AB52	FBB_D<54>
FBB_D<23>	AK52	FBB_D23	FBB_D55	AB51	FBB_D<55>
FBB_D<24>	AN49	FBB_D24	FBB_D56	AD46	FBB_D<56>
FBB_D<25>	AN49	FBB_D25	FBB_D57	AC46	FBB_D<57>
FBB_D<26>	AN48	FBB_D26	FBB_D58	AC48	FBB_D<58>
FBB_D<27>	AN47	FBB_D27	FBB_D59	AB48	FBB_D<59>
FBB_D<28>	AN46	FBB_D28	FBB_D60	Y48	FBB_D<60>
FBB_D<29>	AL47	FBB_D29	FBB_D61	W48	FBB_D<61>
FBB_D<30>	AK47	FBB_D30	FBB_D62	V46	FBB_D<62>
FBB_D<31>	AK48	FBB_D31	FBB_D63	V46	FBB_D<63>
FBB_DQM0	AT51	FBB_DQM0	FBB_DQM4	AG49	FBB_DQM4
FBB_DQM1	AV47	FBB_DQM1	FBB_DQM5	AH48	FBB_DQM5
FBB_DQM2	AL52	FBB_DQM2	FBB_DQM6	AC50	FBB_DQM6
FBB_DQM3	AW46	FBB_DQM3	FBB_DQM7	Y47	FBB_DQM7
FBB_DQS_RN0	AU53	FBB_DQS_RN0	FBB_DQS_RN4	AH51	FBB_DQS_RN4
FBB_DQS_RN1	AU48	FBB_DQS_RN1	FBB_DQS_RN5	AF47	FBB_DQS_RN5
FBB_DQS_RN2	AL51	FBB_DQS_RN2	FBB_DQS_RN6	AD50	FBB_DQS_RN6
FBB_DQS_RN3	AL48	FBB_DQS_RN3	FBB_DQS_RN7	AC47	FBB_DQS_RN7
FBB_DQS_WP0	AU52	FBB_DQS_WP0	FBB_DQS_WP4	AG50	FBB_DQS_WP4
FBB_DQS_WP1	AT48	FBB_DQS_WP1	FBB_DQS_WP5	AF46	FBB_DQS_WP5
FBB_DQS_WP2	AW50	FBB_DQS_WP2	FBB_DQS_WP6	AC49	FBB_DQS_WP6
FBB_DQS_WP3	AW47	FBB_DQS_WP3	FBB_DQS_WP7	AB47	FBB_DQS_WP7
FBB_CMD<0>	BB54	FBB_CMD0			
FBB_CMD<1>	BB55	FBB_CMD1			
FBB_CMD<2>	BA53	FBB_CMD2			
FBB_CMD<3>	BA55	FBB_CMD3			
FBB_CMD<4>	AY53	FBB_CMD4			
FBB_CMD<5>	AW54	FBB_CMD5			
FBB_CMD<6>	AW55	FBB_CMD6			
FBB_CMD<7>	AV53	FBB_CMD7			
FBB_CMD<8>	AV55	FBB_CMD8			
FBB_CMD<9>	AT53	FBB_CMD9			
FBB_CMD<10>	AT54	FBB_CMD10			
FBB_CMD<11>	AT55	FBB_CMD11			
FBB_CMD<12>	AR53	FBB_CMD12			
FBB_CMD<13>	AR55	FBB_CMD13			
FBB_CMD<14>	AP53	FBB_CMD14			
FBB_CMD<15>	AN55	FBB_CMD15			
FBB_CMD<16>	AN53	FBB_CMD16			
FBB_CMD<17>	AN54	FBB_CMD17			
FBB_CMD<18>	AM53	FBB_CMD18			
FBB_CMD<19>	AM55	FBB_CMD19			
FBB_CMD<20>	AL53	FBB_CMD20			
FBB_CMD<21>	AK53	FBB_CMD21			
SNN_FBB_CMD<22>	AK54	FBB_CMD22			
FBB_CMD<23>	AK55	FBB_CMD23			
FBB_CMD<24>	AJ53	FBB_CMD24			
FBB_CMD<25>	AJ55	FBB_CMD25			
FBB_CMD<26>	AH53	FBB_CMD26			
FBB_CMD<27>	AG55	FBB_CMD27			
FBB_CMD<28>	AG53	FBB_CMD28			
SNN_FBB_CMD<29>	AF55	FBB_CMD29			
SNN_FBB_CMD<30>	AF54	FBB_CMD30			
SNN_FBB_CMD<31>	AF53	FBB_CMD31			
SNN_FBB_CMD<32>	AD55	FBB_CMD32			
FBB0_CLK0	AW47	FBB0_CLK0	FBB1_CLK0	AK45	FBB1_CLK0
FBB0_CLK0*	AW46	FBB0_CLK0	FBB1_CLK0*	AK46	FBB1_CLK0
SNN_FBB0_CLK1	AT45	FBB0_CLK1	SNN_FBB1_CLK1	AP45	SNN_FBB1_CLK1
SNN_FBB0_CLK1*	AU45	FBB0_CLK1	SNN_FBB1_CLK1*	AN45	SNN_FBB1_CLK1

FBVDDQ — R721 60.4 1% 0402 NO STUFF

FBB_DEBUG — AU43 FBB_DEBUG

FBA_D<0>	40OHM	2 0	OUT 8.2A<>	FBA_D<0..63>	
FBA_D<1>	40OHM	2 1			
FBA_D<2>	40OHM	2 2			
FBA_D<3>	40OHM	2 3			
FBA_D<4>	40OHM	2 4			
FBA_D<5>	40OHM	2 5			
FBA_D<6>	40OHM	2 6			
FBA_D<7>	40OHM	2 7			
FBA_D<8>	40OHM	2 8			
FBA_D<9>	40OHM	2 9			
FBA_D<10>	40OHM	2 10			
FBA_D<11>	40OHM	2 11			
FBA_D<12>	40OHM	2 12			
FBA_D<13>	40OHM	2 13			
FBA_D<14>	40OHM	2 14			
FBA_D<15>	40OHM	2 15			
FBA_D<16>	40OHM	2 16			
FBA_D<17>	40OHM	2 17			
FBA_D<18>	40OHM	2 18			
FBA_D<19>	40OHM	2 19			
FBA_D<20>	40OHM	2 20			
FBA_D<21>	40OHM	2 21			
FBA_D<22>	40OHM	2 22			
FBA_D<23>	40OHM	2 23			
FBA_D<24>	40OHM	2 24			
FBA_D<25>	40OHM	2 25			
FBA_D<26>	40OHM	2 26			
FBA_D<27>	40OHM	2 27			
FBA_D<28>	40OHM	2 28			
FBA_D<29>	40OHM	2 29			
FBA_D<30>	40OHM	2 30			
FBA_D<31>	40OHM	2 31			
FBA_D<32>	40OHM	2 32			
FBA_D<33>	40OHM	2 33			
FBA_D<34>	40OHM	2 34			
FBA_D<35>	40OHM	2 35			
FBA_D<36>	40OHM	2 36			
FBA_D<37>	40OHM	2 37			
FBA_D<38>	40OHM	2 38			
FBA_D<39>	40OHM	2 39			
FBA_D<40>	40OHM	2 40			
FBA_D<41>	40OHM	2 41			
FBA_D<42>	40OHM	2 42			
FBA_D<43>	40OHM	2 43			
FBA_D<44>	40OHM	2 44			
FBA_D<45>	40OHM	2 45			
FBA_D<46>	40OHM	2 46			
FBA_D<47>	40OHM	2 47			
FBA_D<48>	40OHM	2 48			
FBA_D<49>	40OHM	2 49			
FBA_D<50>	40OHM	2 50			
FBA_D<51>	40OHM	2 51			
FBA_D<52>	40OHM	2 52			
FBA_D<53>	40OHM	2 53			
FBA_D<54>	40OHM	2 54			
FBA_D<55>	40OHM	2 55			
FBA_D<56>	40OHM	2 56			
FBA_D<57>	40OHM	2 57			
FBA_D<58>	40OHM	2 58			
FBA_D<59>	40OHM	2 59			
FBA_D<60>	40OHM	2 60			
FBA_D<61>	40OHM	2 61			
FBA_D<62>	40OHM	2 62			
FBA_D<63>	40OHM	2 63			
FBA_DQM0	40OHM	2	BI 8.4A<>		
FBA_DQM1	40OHM	2	BI 8.5A<>		
FBA_DQM2	40OHM	2	BI 8.5A<>		
FBA_DQM3	40OHM	2	BI 8.5A<>		
FBA_DQM4	40OHM	2	BI 8.5A<>		
FBA_DQM5	40OHM	2	BI 8.5A<>		
FBA_DQM6	40OHM	2	BI 8.5A<>		
FBA_DQM7	40OHM	2	BI 8.5A<>		
FBA_DQS_RN0	40OHM	1	IN 8.5A<		
FBA_DQS_RN1	40OHM	1	IN 8.5A<		
FBA_DQS_RN2	40OHM	1	IN 8.5A<		
FBA_DQS_RN3	40OHM	1	IN 8.5A<		
FBA_DQS_RN4	40OHM	1	IN 8.5A<		
FBA_DQS_RN5	40OHM	1	IN 8.5A<		
FBA_DQS_RN6	40OHM	1	IN 8.5A<		
FBA_DQS_RN7	40OHM	1	IN 8.5A<		
FBA_DQS_WP0	40OHM	1	OUT 8.5A>		
FBA_DQS_WP1	40OHM	1	OUT 8.5A>		
FBA_DQS_WP2	40OHM	1	OUT 8.5A>		
FBA_DQS_WP3	40OHM	1	OUT 8.5A>		
FBA_DQS_WP4	40OHM	1	OUT 8.5A>		
FBA_DQS_WP5	40OHM	1	OUT 8.5A>		
FBA_DQS_WP6	40OHM	1	OUT 8.5A>		
FBA_DQS_WP7	40OHM	1	OUT 8.5A>		
FBA_CMD<0>	40OHM	2 0	OUT 8.1A<	FBA_CMD<0..28>	
FBA_CMD<1>	40OHM	2 1			
FBA_CMD<2>	40OHM	2 2			
FBA_CMD<3>	40OHM	2 3			
FBA_CMD<4>	40OHM	2 4			
FBA_CMD<5>	40OHM	2 5			
FBA_CMD<6>	40OHM	2 6			
FBA_CMD<7>	40OHM	2 7			
FBA_CMD<8>	40OHM	2 8			
FBA_CMD<9>	40OHM	2 9			
FBA_CMD<10>	40OHM	2 10			
FBA_CMD<11>	40OHM	2 11			
FBA_CMD<12>	40OHM	2 12			
FBA_CMD<13>	40OHM	2 13			
FBA_CMD<14>	40OHM	2 14			
FBA_CMD<15>	40OHM	2 15			
FBA_CMD<16>	40OHM	2 16			
FBA_CMD<17>	40OHM	2 17			
FBA_CMD<18>	40OHM	2 18			
FBA_CMD<19>	40OHM	2 19			
FBA_CMD<20>	40OHM	2 20			
FBA_CMD<21>	40OHM	2 21			
FBA_CMD<23>	40OHM	2 23			
FBA_CMD<24>	40OHM	2 24			
FBA_CMD<25>	40OHM	2 25			
FBA_CMD<26>	40OHM	2 26			
FBA_CMD<27>	40OHM	2 27			
FBA_CMD<28>	40OHM	2 28			
FBA0_CLK0	80DIFF	1	OUT 8.2A<		
FBA0_CLK0*	80DIFF	1	OUT 8.2A<		
FBA1_CLK0	80DIFF	1	OUT 8.2A<		
FBA1_CLK0*	80DIFF	1	OUT 8.2A<		

FBB_D<0>	40OHM	2 0	OUT 9.2A<>	FBB_D<0..63>	
FBB_D<1>	40OHM	2 1			
FBB_D<2>	40OHM	2 2			
FBB_D<3>	40OHM	2 3			
FBB_D<4>	40OHM	2 4			
FBB_D<5>	40OHM	2 5			
FBB_D<6>	40OHM	2 6			
FBB_D<7>	40OHM	2 7			
FBB_D<8>	40OHM	2 8			
FBB_D<9>	40OHM	2 9			
FBB_D<10>	40OHM	2 10			
FBB_D<11>	40OHM	2 11			
FBB_D<12>	40OHM	2 12			
FBB_D<13>	40OHM	2 13			
FBB_D<14>	40OHM	2 14			
FBB_D<15>	40OHM	2 15			
FBB_D<16>	40OHM	2 16			
FBB_D<17>	40OHM	2 17			
FBB_D<18>	40OHM	2 18			
FBB_D<19>	40OHM	2 19			
FBB_D<20>	40OHM	2 20			
FBB_D<21>	40OHM	2 21			
FBB_D<22>	40OHM	2 22			
FBB_D<23>	40OHM	2 23			
FBB_D<24>	40OHM	2 24			
FBB_D<25>	40OHM	2 25			
FBB_D<26>	40OHM	2 26			
FBB_D<27>	40OHM	2 27			
FBB_D<28>	40OHM	2 28			
FBB_D<29>	40OHM	2 29			
FBB_D<30>	40OHM	2 30			
FBB_D<31>	40OHM	2 31			
FBB_D<32>	40OHM	2 32			
FBB_D<33>	40OHM	2 33			
FBB_D<34>	40OHM	2 34			
FBB_D<35>	40OHM	2 35			
FBB_D<36>	40OHM	2 36			
FBB_D<37>	40OHM	2 37			
FBB_D<38>	40OHM	2 38			
FBB_D<39>	40OHM	2 39			
FBB_D<40>	40OHM	2 40			
FBB_D<41>	40OHM	2 41			
FBB_D<42>	40OHM	2 42			
FBB_D<43>	40OHM	2 43			
FBB_D<44>	40OHM	2 44			
FBB_D<45>	40OHM	2 45			
FBB_D<46>	40OHM	2 46			
FBB_D<47>	40OHM	2 47			
FBB_D<48>	40OHM	2 48			
FBB_D<49>	40OHM	2 49			
FBB_D<50>	40OHM	2 50			
FBB_D<51>	40OHM	2 51			
FBB_D<52>	40OHM	2 52			
FBB_D<53>	40OHM	2 53			
FBB_D<54>	40OHM	2 54			
FBB_D<55>	40OHM	2 55			
FBB_D<56>	40OHM	2 56			
FBB_D<57>	40OHM	2 57			
FBB_D<58>	40OHM	2 58			
FBB_D<59>	40OHM	2 59			
FBB_D<60>	40OHM	2 60			
FBB_D<61>	40OHM	2 61			
FBB_D<62>	40OHM	2 62			
FBB_D<63>	40OHM	2 63			
FBB_DQM0	40OHM	2	BI 9.4A<>		
FBB_DQM1	40OHM	2	BI 9.5A<>		
FBB_DQM2	40OHM	2	BI 9.5A<>		
FBB_DQM3	40OHM	2	BI 9.5A<>		
FBB_DQM4	40OHM	2	BI 9.5A<>		
FBB_DQM5	40OHM	2	BI 9.5A<>		
FBB_DQM6	40OHM	2	BI 9.5A<>		
FBB_DQM7	40OHM	2	BI 9.5A<>		
FBB_DQS_RN0	40OHM	1	IN 9.5A<		
FBB_DQS_RN1	40OHM	1	IN 9.5A<		
FBB_DQS_RN2	40OHM	1	IN 9.5A<		
FBB_DQS_RN3	40OHM	1	IN 9.5A<		
FBB_DQS_RN4	40OHM	1	IN 9.5A<		
FBB_DQS_RN5	40OHM	1	IN 9.5A<		
FBB_DQS_RN6	40OHM	1	IN 9.5A<		
FBB_DQS_RN7	40OHM	1	IN 9.5A<		
FBB_DQS_WP0	40OHM	1	OUT 9.5A>		
FBB_DQS_WP1	40OHM	1	OUT 9.5A>		
FBB_DQS_WP2	40OHM	1	OUT 9.5A>		
FBB_DQS_WP3	40OHM	1	OUT 9.5A>		
FBB_DQS_WP4	40OHM	1	OUT 9.5A>		
FBB_DQS_WP5	40OHM	1	OUT 9.5A>		
FBB_DQS_WP6	40OHM	1	OUT 9.5A>		
FBB_DQS_WP7	40OHM	1	OUT 9.5A>		
FBB_CMD<0>	40OHM	2 0	OUT 9.1A<	FBB_CMD<0..28>	
FBB_CMD<1>	40OHM	2 1			
FBB_CMD<2>	40OHM	2 2			
FBB_CMD<3>	40OHM	2 3			
FBB_CMD<4>	40OHM	2 4			
FBB_CMD<5>	40OHM	2 5			
FBB_CMD<6>	40OHM	2 6			
FBB_CMD<7>	40OHM	2 7			
FBB_CMD<8>	40OHM	2 8			
FBB_CMD<9>	40OHM	2 9			
FBB_CMD<10>	40OHM	2 10			
FBB_CMD<11>	40OHM	2 11			
FBB_CMD<12>	40OHM	2 12			
FBB_CMD<13>	40OHM	2 13			
FBB_CMD<14>	40OHM	2 14			
FBB_CMD<15>	40OHM	2 15			
FBB_CMD<16>	40OHM	2 16			
FBB_CMD<17>	40OHM	2 17			
FBB_CMD<18>	40OHM	2 18			
FBB_CMD<19>	40OHM	2 19			
FBB_CMD<20>	40OHM	2 20			
FBB_CMD<21>	40OHM	2 21			
FBB_CMD<23>	40OHM	2 23			
FBB_CMD<24>	40OHM	2 24			
FBB_CMD<25>	40OHM	2 25			
FBB_CMD<26>	40OHM	2 26			
FBB_CMD<27>	40OHM	2 27			
FBB_CMD<28>	40OHM	2 28			
FBB0_CLK0	80DIFF	1	OUT 9.2A<		
FBB0_CLK0*	80DIFF	1	OUT 9.2A<		
FBB1_CLK0	80DIFF	1	OUT 9.2A<		
FBB1_CLK0*	80DIFF	1	OUT 9.2A<		

FB_CAL and Vref

FBVDDQ — R722 549 1% 0402 NO STUFF
R712 1.3K 1% 0402 NO STUFF — C798 .1UF 16V 10% X7R 0402 COMMON — GND
FBVDDQ — R760 549 1% 0402 NO STUFF
R767 1.3K 1% 0402 NO STUFF — C1052 .1UF 16V 10% X7R 0402 COMMON — GND

FBVDDQ — R736 48.7 1% 0402 COMMON — FB_CAL_PD_VDDQ L39
R731 40.2 1% 0402 COMMON — FB_CAL_PU_GND L40
R730 40.2 1% 0402 COMMON — FB_CAL_TERM_GND L42
FB_VREF0 AG46
FB_VREF1 AH11

G1
G200-100-A2
BGA2236
CHANGED

10/21 FBCAL

FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
FB_VREF0
FB_VREF1

VREF=FBVDDQ*Rtop/(Rtop+Rbot)
VREF=FBVDDQ*0.7

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer A,B: GPU Section + Calibration

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	4 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Framebuffer C,D: GPU Section

G1
G200-100-A2
BGA2236
CHANGED
4/21 MEM_C

FBC_D<0>	AB53	FBC_D0	FBC_D32	N51	FBC_D<32>
FBC_D<1>	W53	FBC_D1	FBC_D33	N52	FBC_D<33>
FBC_D<2>	W52	FBC_D2	FBC_D34	M52	FBC_D<34>
FBC_D<3>	Y52	FBC_D3	FBC_D35	L50	FBC_D<35>
FBC_D<4>	AA52	FBC_D4	FBC_D36	K51	FBC_D<36>
FBC_D<5>	Y51	FBC_D5	FBC_D37	K52	FBC_D<37>
FBC_D<6>	AA50	FBC_D6	FBC_D38	J52	FBC_D<38>
FBC_D<7>	AA49	FBC_D7	FBC_D39	J50	FBC_D<39>
FBC_D<8>	V49	FBC_D8	FBC_D40	L45	FBC_D<40>
FBC_D<9>	U48	FBC_D9	FBC_D41	L46	FBC_D<41>
FBC_D<10>	U47	FBC_D10	FBC_D42	L47	FBC_D<42>
FBC_D<11>	T47	FBC_D11	FBC_D43	K48	FBC_D<43>
FBC_D<12>	U46	FBC_D12	FBC_D44	H48	FBC_D<44>
FBC_D<13>	U45	FBC_D13	FBC_D45	H46	FBC_D<45>
FBC_D<14>	T45	FBC_D14	FBC_D46	G47	FBC_D<46>
FBC_D<15>	R46	FBC_D15	FBC_D47	J49	FBC_D<47>
FBC_D<16>	U52	FBC_D16	FBC_D48	H49	FBC_D<48>
FBC_D<17>	U51	FBC_D17	FBC_D49	H50	FBC_D<49>
FBC_D<18>	U50	FBC_D18	FBC_D50	F50	FBC_D<50>
FBC_D<19>	R50	FBC_D19	FBC_D51	H51	FBC_D<51>
FBC_D<20>	P50	FBC_D20	FBC_D52	H52	FBC_D<52>
FBC_D<21>	P51	FBC_D21	FBC_D53	F52	FBC_D<53>
FBC_D<22>	P52	FBC_D22	FBC_D54	E53	FBC_D<54>
FBC_D<23>	R52	FBC_D23	FBC_D55	D53	FBC_D<55>
FBC_D<24>	P45	FBC_D24	FBC_D56	C52	FBC_D<56>
FBC_D<25>	P46	FBC_D25	FBC_D57	D51	FBC_D<57>
FBC_D<26>	P47	FBC_D26	FBC_D58	E52	FBC_D<58>
FBC_D<27>	N47	FBC_D27	FBC_D59	E51	FBC_D<59>
FBC_D<28>	P48	FBC_D28	FBC_D60	D48	FBC_D<60>
FBC_D<29>	N48	FBC_D29	FBC_D61	D47	FBC_D<61>
FBC_D<30>	L48	FBC_D30	FBC_D62	E48	FBC_D<62>
FBC_D<31>	L49	FBC_D31	FBC_D63	F47	FBC_D<63>

FBC_DQM0	W51	FBC_DQM0	FBC_DQM4	K53	FBC_DQM4
FBC_DQM1	U49	FBC_DQM1	FBC_DQM5	G48	FBC_DQM5
FBC_DQM2	T51	FBC_DQM2	FBC_DQM6	G51	FBC_DQM6
FBC_DQM3	P49	FBC_DQM3	FBC_DQM7	C49	FBC_DQM7

FBC_DQS_RN0	Y49	FBC_DQS_RN0	FBC_DQS_RN4	L52	FBC_DQS_RN4
FBC_DQS_RN1	R47	FBC_DQS_RN1	FBC_DQS_RN5	K47	FBC_DQS_RN5
FBC_DQS_RN2	T52	FBC_DQS_RN2	FBC_DQS_RN6	G52	FBC_DQS_RN6
FBC_DQS_RN3	U50	FBC_DQS_RN3	FBC_DQS_RN7	E49	FBC_DQS_RN7
FBC_DQS_WP0	Y50	FBC_DQS_WP0	FBC_DQS_WP4	L51	FBC_DQS_WP4
FBC_DQS_WP1	T48	FBC_DQS_WP1	FBC_DQS_WP5	J47	FBC_DQS_WP5
FBC_DQS_WP2	T53	FBC_DQS_WP2	FBC_DQS_WP6	G53	FBC_DQS_WP6
FBC_DQS_WP3	M49	FBC_DQS_WP3	FBC_DQS_WP7	D49	FBC_DQS_WP7

FBC_CMD<0>	AD53	FBC_CMD0	FBC_CMD16		
FBC_CMD<1>	AC55	FBC_CMD1	FBC_CMD17		
FBC_CMD<2>	AC54	FBC_CMD2	FBC_CMD18		
FBC_CMD<3>	AC53	FBC_CMD3	FBC_CMD19		
FBC_CMD<4>	AA55	FBC_CMD4	FBC_CMD20		
FBC_CMD<5>	AA53	FBC_CMD5	FBC_CMD21		
FBC_CMD<6>	Y55	FBC_CMD6	FBC_CMD22	SNN_FBC_CMD<22>	L54
FBC_CMD<7>	Y54	FBC_CMD7	FBC_CMD23	FBC_CMD<23>	L53
FBC_CMD<8>	Y53	FBC_CMD8	FBC_CMD24	FBC_CMD<24>	J55
FBC_CMD<9>	V55	FBC_CMD9	FBC_CMD25	FBC_CMD<25>	J53
FBC_CMD<10>	V53	FBC_CMD10	FBC_CMD26	FBC_CMD<26>	H55
FBC_CMD<11>	U55	FBC_CMD11	FBC_CMD27	FBC_CMD<27>	H54
FBC_CMD<12>	U54	FBC_CMD12	FBC_CMD28	FBC_CMD<28>	H53
FBC_CMD<13>	U53	FBC_CMD13	FBC_CMD29	SNN_FBC_CMD<29>	F55
FBC_CMD<14>	R55	FBC_CMD14	FBC_CMD30	SNN_FBC_CMD<30>	F53
FBC_CMD<15>	R53	FBC_CMD15	FBC_CMD31	SNN_FBC_CMD<31>	E55
FBC_CMD<16>	P53	FBC_CMD16	FBC_CMD32	SNN_FBC_CMD<32>	E54
FBC_CMD<17>	P54	FBC_CMD17			
FBC_CMD<18>	P55	FBC_CMD18			
FBC_CMD<19>	M56	FBC_CMD19			
FBC_CMD<20>	M53	FBC_CMD20			
FBC_CMD<21>	L55	FBC_CMD21			
FBC_CMD<22>	L54	FBC_CMD22			
FBC_CMD<23>	L53	FBC_CMD23			
FBC_CMD<24>	J55	FBC_CMD24			
FBC_CMD<25>	J53	FBC_CMD25			
FBC_CMD<26>	H55	FBC_CMD26			
FBC_CMD<27>	H54	FBC_CMD27			
FBC_CMD<28>	H53	FBC_CMD28			
SNN_FBC_CMD<29>	F55	FBC_CMD29			
SNN_FBC_CMD<30>	F53	FBC_CMD30			
SNN_FBC_CMD<31>	E55	FBC_CMD31			
SNN_FBC_CMD<32>	E54	FBC_CMD32			

FBC0_CLK0	FBC0_CLK0	AA47	FBC0_CLK0	FBC1_CLK0	M46	FBC1_CLK0	FBC1_CLK0
FBC0_CLK0*	FBC0_CLK0	AA46	FBC0_CLK1	FBC1_CLK0*	M47	FBC1_CLK0*	FBC1_CLK0
SNN_FBC0_CLK1	FBC0_CLK1	AC45	FBC1_CLK1	SNN_FBC1_CLK1	Y45	SNN_FBC1_CLK1	FBC1_CLK1
SNN_FBC0_CLK1*	FBC0_CLK1	AB45	FBC1_CLK1	SNN_FBC1_CLK1*	W45	SNN_FBC1_CLK1*	FBC1_CLK1

FBVDDQ
R729
60.4
1%
0402
NO STUFF

FBC_DEBUG — P43 FBC_DEBUG

FBCD_REFCLK — AE45 FBCD_REFCLK — IN 19.5Ω>
FBCD_REFCLK — AF45 FBCD_REFCLK* — IN 19.5Ω>

FBCD_MPLL_AVDD — N45 FBABCD_MPLL_AVDD — IN 4.3C>

C813
.1UF
6.3V
10%
X7R
0402
COMMON
GND

C801
4.7UF
6.3V
20%
X5R
0603
COMMON
GND

G1
G200-100-A2
BGA2236
CHANGED
5/21 MEM_D

FBD_D<0>	E46	FBD_D0	FBD_D32	C37	FBD_D<32>
FBD_D<1>	E45	FBD_D1	FBD_D33	D38	FBD_D<33>
FBD_D<2>	F45	FBD_D2	FBD_D34	F38	FBD_D<34>
FBD_D<3>	H45	FBD_D3	FBD_D35	E37	FBD_D<35>
FBD_D<4>	G44	FBD_D4	FBD_D36	F36	FBD_D<36>
FBD_D<5>	F44	FBD_D5	FBD_D37	G35	FBD_D<37>
FBD_D<6>	D44	FBD_D6	FBD_D38	F35	FBD_D<38>
FBD_D<7>	E43	FBD_D7	FBD_D39	D35	FBD_D<39>
FBD_D<8>	L43	FBD_D8	FBD_D40	J34	FBD_D<40>
FBD_D<9>	K42	FBD_D9	FBD_D41	H33	FBD_D<41>
FBD_D<10>	J43	FBD_D10	FBD_D42	J33	FBD_D<42>
FBD_D<11>	J42	FBD_D11	FBD_D43	K33	FBD_D<43>
FBD_D<12>	G41	FBD_D12	FBD_D44	K32	FBD_D<44>
FBD_D<13>	H40	FBD_D13	FBD_D45	J32	FBD_D<45>
FBD_D<14>	G39	FBD_D14	FBD_D46	J31	FBD_D<46>
FBD_D<15>	F39	FBD_D15	FBD_D47	H31	FBD_D<47>
FBD_D<16>	C43	FBD_D16	FBD_D48	C31	FBD_D<48>
FBD_D<17>	D43	FBD_D17	FBD_D49	C34	FBD_D<49>
FBD_D<18>	D42	FBD_D18	FBD_D50	D30	FBD_D<50>
FBD_D<19>	E42	FBD_D19	FBD_D51	D32	FBD_D<51>
FBD_D<20>	D41	FBD_D20	FBD_D52	E34	FBD_D<52>
FBD_D<21>	D40	FBD_D21	FBD_D53	D34	FBD_D<53>
FBD_D<22>	D39	FBD_D22	FBD_D54	D31	FBD_D<54>
FBD_D<23>	E39	FBD_D23	FBD_D55	D33	FBD_D<55>
FBD_D<24>	J40	FBD_D24	FBD_D56	F29	FBD_D<56>
FBD_D<25>	K41	FBD_D25	FBD_D57	F30	FBD_D<57>
FBD_D<26>	J39	FBD_D26	FBD_D58	D26	FBD_D<58>
FBD_D<27>	H39	FBD_D27	FBD_D59	D27	FBD_D<59>
FBD_D<28>	G38	FBD_D28	FBD_D60	E28	FBD_D<60>
FBD_D<29>	H37	FBD_D29	FBD_D61	E30	FBD_D<61>
FBD_D<30>	H36	FBD_D30	FBD_D62	E26	FBD_D<62>
FBD_D<31>	K36	FBD_D31	FBD_D63		

FBD_DQM0	D45	FBD_DQM0	FBD_DQM4	E36	FBD_DQM4
FBD_DQM1	H43	FBD_DQM1	FBD_DQM5	J35	FBD_DQM5
FBD_DQM2	C40	FBD_DQM2	FBD_DQM6	F32	FBD_DQM6
FBD_DQM3	L37	FBD_DQM3	FBD_DQM7	C28	FBD_DQM7

FBD_DQS_RN0	D46	FBD_DQS_RN0	FBD_DQS_RN4	D36	FBD_DQS_RN4
FBD_DQS_RN1	G42	FBD_DQS_RN1	FBD_DQS_RN5	H34	FBD_DQS_RN5
FBD_DQS_RN2	E40	FBD_DQS_RN2	FBD_DQS_RN6	E33	FBD_DQS_RN6
FBD_DQS_RN3	J36	FBD_DQS_RN3	FBD_DQS_RN7	D29	FBD_DQS_RN7
FBD_DQS_WP0	C46	FBD_DQS_WP0	FBD_DQS_WP4	D37	FBD_DQS_WP4
FBD_DQS_WP1	H42	FBD_DQS_WP1	FBD_DQS_WP5	G33	FBD_DQS_WP5
FBD_DQS_WP2	F41	FBD_DQS_WP2	FBD_DQS_WP6	F33	FBD_DQS_WP6
FBD_DQS_WP3	J37	FBD_DQS_WP3	FBD_DQS_WP7	C29	FBD_DQS_WP7

FBD_CMD<0>	C54	FBD_CMD0	FBD_CMD16		
FBD_CMD<1>	B53	FBD_CMD1	FBD_CMD17		
FBD_CMD<2>	C51	FBD_CMD2	FBD_CMD18		
FBD_CMD<3>	C50	FBD_CMD3	FBD_CMD19		
FBD_CMD<4>	B51	FBD_CMD4	FBD_CMD20		
FBD_CMD<5>	A51	FBD_CMD5	FBD_CMD21		
FBD_CMD<6>	A50	FBD_CMD6	FBD_CMD22	SNN_FBD_CMD<22>	C39
FBD_CMD<7>	C48	FBD_CMD7	FBD_CMD23	FBD_CMD<23>	B39
FBD_CMD<8>	B48	FBD_CMD8	FBD_CMD24	FBD_CMD<24>	A39
FBD_CMD<9>	A48	FBD_CMD9	FBD_CMD25	FBD_CMD<25>	C38
FBD_CMD<10>	C47	FBD_CMD10	FBD_CMD26	FBD_CMD<26>	A38
FBD_CMD<11>	A47	FBD_CMD11	FBD_CMD27	FBD_CMD<27>	C36
FBD_CMD<12>	C45	FBD_CMD12	FBD_CMD28	FBD_CMD<28>	B36
FBD_CMD<13>	B45	FBD_CMD13	FBD_CMD29	SNN_FBD_CMD<29>	A36
FBD_CMD<14>	A45	FBD_CMD14	FBD_CMD30	SNN_FBD_CMD<30>	C35
FBD_CMD<15>	A44	FBD_CMD15	FBD_CMD31	SNN_FBD_CMD<31>	A35
FBD_CMD<16>	C44	FBD_CMD16	FBD_CMD32	SNN_FBD_CMD<32>	C33
FBD_CMD<17>	C42	FBD_CMD17			
FBD_CMD<18>	B42	FBD_CMD18			
FBD_CMD<19>	A42	FBD_CMD19			
FBD_CMD<20>	C41	FBD_CMD20			
FBD_CMD<21>	A41	FBD_CMD21			
FBD_CMD<22>	C39	FBD_CMD22			
FBD_CMD<23>	B39	FBD_CMD23			
FBD_CMD<24>	A39	FBD_CMD24			
FBD_CMD<25>	C38	FBD_CMD25			
FBD_CMD<26>	A38	FBD_CMD26			
FBD_CMD<27>	C36	FBD_CMD27			
FBD_CMD<28>	B36	FBD_CMD28			
SNN_FBD_CMD<29>	A36	FBD_CMD29			
SNN_FBD_CMD<30>	C35	FBD_CMD30			
SNN_FBD_CMD<31>	A35	FBD_CMD31			
SNN_FBD_CMD<32>	C33	FBD_CMD32			

FBD0_CLK0	FBD0_CLK0	K44	FBD0_CLK0	FBD1_CLK0	J38	FBD1_CLK0	FBD1_CLK0
FBD0_CLK0*	FBD0_CLK0	J44	FBD0_CLK1	FBD1_CLK0*	K38	FBD1_CLK0*	FBD1_CLK0
SNN_FBD0_CLK1	FBD0_CLK1	L34	FBD1_CLK1	SNN_FBD1_CLK1	L30	SNN_FBD1_CLK1	FBD1_CLK1
SNN_FBD0_CLK1*	FBD0_CLK1	L33	FBD1_CLK1	SNN_FBD1_CLK1*	L31	SNN_FBD1_CLK1*	FBD1_CLK1

FBVDDQ
R727
60.4
1%
0402
NO STUFF

FBD_DEBUG — N42 FBD_DEBUG

FBD_D<0..63> — OUT 10.2A<>

FBC_D<0>	400HM	2	0
FBC_D<1>	400HM	2	1
FBC_D<2>	400HM	2	2
FBC_D<3>	400HM	2	3
FBC_D<4>	400HM	2	4
FBC_D<5>	400HM	2	5
FBC_D<6>	400HM	2	6
FBC_D<7>	400HM	2	7
FBC_D<8>	400HM	2	8
FBC_D<9>	400HM	2	9
FBC_D<10>	400HM	2	10
FBC_D<11>	400HM	2	11
FBC_D<12>	400HM	2	12
FBC_D<13>	400HM	2	13
FBC_D<14>	400HM	2	14
FBC_D<15>	400HM	2	15
FBC_D<16>	400HM	2	16
FBC_D<17>	400HM	2	17
FBC_D<18>	400HM	2	18
FBC_D<19>	400HM	2	19
FBC_D<20>	400HM	2	20
FBC_D<21>	400HM	2	21
FBC_D<22>	400HM	2	22
FBC_D<23>	400HM	2	23
FBC_D<24>	400HM	2	24
FBC_D<25>	400HM	2	25
FBC_D<26>	400HM	2	26
FBC_D<27>	400HM	2	27
FBC_D<28>	400HM	2	28
FBC_D<29>	400HM	2	29
FBC_D<30>	400HM	2	30
FBC_D<31>	400HM	2	31
FBC_D<32>	400HM	2	32
FBC_D<33>	400HM	2	33
FBC_D<34>	400HM	2	34
FBC_D<35>	400HM	2	35
FBC_D<36>	400HM	2	36
FBC_D<37>	400HM	2	37
FBC_D<38>	400HM	2	38
FBC_D<39>	400HM	2	39
FBC_D<40>	400HM	2	40
FBC_D<41>	400HM	2	41
FBC_D<42>	400HM	2	42
FBC_D<43>	400HM	2	43
FBC_D<44>	400HM	2	44
FBC_D<45>	400HM	2	45
FBC_D<46>	400HM	2	46
FBC_D<47>	400HM	2	47
FBC_D<48>	400HM	2	48
FBC_D<49>	400HM	2	49
FBC_D<50>	400HM	2	50
FBC_D<51>	400HM	2	51
FBC_D<52>	400HM	2	52
FBC_D<53>	400HM	2	53
FBC_D<54>	400HM	2	54
FBC_D<55>	400HM	2	55
FBC_D<56>	400HM	2	56
FBC_D<57>	400HM	2	57
FBC_D<58>	400HM	2	58
FBC_D<59>	400HM	2	59
FBC_D<60>	400HM	2	60
FBC_D<61>	400HM	2	61
FBC_D<62>	400HM	2	62
FBC_D<63>	400HM	2	63

FBC_DQM0	400HM	2	BI 10.4A<>
FBC_DQM1	400HM	2	BI 10.5A<>
FBC_DQM2	400HM	2	BI 10.5A<>
FBC_DQM3	400HM	2	BI 10.5A<>
FBC_DQM4	400HM	2	BI 10.5A<>
FBC_DQM5	400HM	2	BI 10.5A<>
FBC_DQM6	400HM	2	BI 10.5A<>
FBC_DQM7	400HM	2	BI 10.5A<>

FBC_DQS_RN0	400HM	1	IN 10.5A<
FBC_DQS_RN1	400HM	1	IN 10.5A<
FBC_DQS_RN2	400HM	1	IN 10.5A<
FBC_DQS_RN3	400HM	1	IN 10.5A<
FBC_DQS_RN4	400HM	1	IN 10.5A<
FBC_DQS_RN5	400HM	1	IN 10.5A<
FBC_DQS_RN6	400HM	1	IN 10.5A<
FBC_DQS_RN7	400HM	1	IN 10.5A<

FBC_DQS_WP0	400HM	1	OUT 10.5A>
FBC_DQS_WP1	400HM	1	OUT 10.5A>
FBC_DQS_WP2	400HM	1	OUT 10.5A>
FBC_DQS_WP3	400HM	1	OUT 10.5A>
FBC_DQS_WP4	400HM	1	OUT 10.5A>
FBC_DQS_WP5	400HM	1	OUT 10.5A>
FBC_DQS_WP6	400HM	1	OUT 10.5A>
FBC_DQS_WP7	400HM	1	OUT 10.5A>

FBC_CMD<0..28> — OUT 10.1A<

FBC_CMD<0>	400HM	2	0
FBC_CMD<1>	400HM	2	1
FBC_CMD<2>	400HM	2	2
FBC_CMD<3>	400HM	2	3
FBC_CMD<4>	400HM	2	4
FBC_CMD<5>	400HM	2	5
FBC_CMD<6>	400HM	2	6
FBC_CMD<7>	400HM	2	7
FBC_CMD<8>	400HM	2	8
FBC_CMD<9>	400HM	2	9
FBC_CMD<10>	400HM	2	10
FBC_CMD<11>	400HM	2	11
FBC_CMD<12>	400HM	2	12
FBC_CMD<13>	400HM	2	13
FBC_CMD<14>	400HM	2	14
FBC_CMD<15>	400HM	2	15
FBC_CMD<16>	400HM	2	16
FBC_CMD<17>	400HM	2	17
FBC_CMD<18>	400HM	2	18
FBC_CMD<19>	400HM	2	19
FBC_CMD<20>	400HM	2	20
FBC_CMD<21>	400HM	2	21
FBC_CMD<23>	400HM	2	23
FBC_CMD<24>	400HM	2	24
FBC_CMD<25>	400HM	2	25
FBC_CMD<26>	400HM	2	26
FBC_CMD<27>	400HM	2	27
FBC_CMD<28>	400HM	2	28

FBC0_CLK0	80DIFF	1	OUT 10.2A<
FBC0_CLK0*	80DIFF	1	OUT 10.2A<
FBC1_CLK0	80DIFF	1	OUT 10.2A<
FBC1_CLK0*	80DIFF	1	OUT 10.2A<

FBD_D<0..63> — OUT 11.2A<>

FBD_D<0>	400HM	2	0
FBD_D<1>	400HM	2	1
FBD_D<2>	400HM	2	2
FBD_D<3>	400HM	2	3
FBD_D<4>	400HM	2	4
FBD_D<5>	400HM	2	5
FBD_D<6>	400HM	2	6
FBD_D<7>	400HM	2	7
FBD_D<8>	400HM	2	8
FBD_D<9>	400HM	2	9
FBD_D<10>	400HM	2	10
FBD_D<11>	400HM	2	11
FBD_D<12>	400HM	2	12
FBD_D<13>	400HM	2	13
FBD_D<14>	400HM	2	14
FBD_D<15>	400HM	2	15
FBD_D<16>	400HM	2	16
FBD_D<17>	400HM	2	17
FBD_D<18>	400HM	2	18
FBD_D<19>	400HM	2	19
FBD_D<20>	400HM	2	20
FBD_D<21>	400HM	2	21
FBD_D<22>	400HM	2	22
FBD_D<23>	400HM	2	23
FBD_D<24>	400HM	2	24
FBD_D<25>	400HM	2	25
FBD_D<26>	400HM	2	26
FBD_D<27>	400HM	2	27
FBD_D<28>	400HM	2	28
FBD_D<29>	400HM	2	29
FBD_D<30>	400HM	2	30
FBD_D<31>	400HM	2	31
FBD_D<32>	400HM	2	32
FBD_D<33>	400HM	2	33
FBD_D<34>	400HM	2	34
FBD_D<35>	400HM	2	35
FBD_D<36>	400HM	2	36
FBD_D<37>	400HM	2	37
FBD_D<38>	400HM	2	38
FBD_D<39>	400HM	2	39
FBD_D<40>	400HM	2	40
FBD_D<41>	400HM	2	41
FBD_D<42>	400HM	2	42
FBD_D<43>	400HM	2	43
FBD_D<44>	400HM	2	44
FBD_D<45>	400HM	2	45
FBD_D<46>	400HM	2	46
FBD_D<47>	400HM	2	47
FBD_D<48>	400HM	2	48
FBD_D<49>	400HM	2	49
FBD_D<50>	400HM	2	50
FBD_D<51>	400HM	2	51
FBD_D<52>	400HM	2	52
FBD_D<53>	400HM	2	53
FBD_D<54>	400HM	2	54
FBD_D<55>	400HM	2	55
FBD_D<56>	400HM	2	56
FBD_D<57>	400HM	2	57
FBD_D<58>	400HM	2	58
FBD_D<59>	400HM	2	59
FBD_D<60>	400HM	2	60
FBD_D<61>	400HM	2	61
FBD_D<62>	400HM	2	62
FBD_D<63>	400HM	2	63

FBD_DQM0	400HM	2	BI 11.4A<>
FBD_DQM1	400HM	2	BI 11.5A<>
FBD_DQM2	400HM	2	BI 11.5A<>
FBD_DQM3	400HM	2	BI 11.5A<>
FBD_DQM4	400HM	2	BI 11.5A<>
FBD_DQM5	400HM	2	BI 11.5A<>
FBD_DQM6	400HM	2	BI 11.5A<>
FBD_DQM7	400HM	2	BI 11.5A<>

FBD_DQS_RN0	400HM	1	IN 11.5A<
FBD_DQS_RN1	400HM	1	IN 11.5A<
FBD_DQS_RN2	400HM	1	IN 11.5A<
FBD_DQS_RN3	400HM	1	IN 11.5A<
FBD_DQS_RN4	400HM	1	IN 11.5A<
FBD_DQS_RN5	400HM	1	IN 11.5A<
FBD_DQS_RN6	400HM	1	IN 11.5A<
FBD_DQS_RN7	400HM	1	IN 11.5A<

FBD_DQS_WP0	400HM	1	OUT 11.5A>
FBD_DQS_WP1	400HM	1	OUT 11.5A>
FBD_DQS_WP2	400HM	1	OUT 11.5A>
FBD_DQS_WP3	400HM	1	OUT 11.5A>
FBD_DQS_WP4	400HM	1	OUT 11.5A>
FBD_DQS_WP5	400HM	1	OUT 11.5A>
FBD_DQS_WP6	400HM	1	OUT 11.5A>
FBD_DQS_WP7	400HM	1	OUT 11.5A>

FBD_CMD<0..28> — OUT 11.1A<

FBD_CMD<0>	400HM	2	0
FBD_CMD<1>	400HM	2	1
FBD_CMD<2>	400HM	2	2
FBD_CMD<3>	400HM	2	3
FBD_CMD<4>	400HM	2	4
FBD_CMD<5>	400HM	2	5
FBD_CMD<6>	400HM	2	6
FBD_CMD<7>	400HM	2	7
FBD_CMD<8>	400HM	2	8
FBD_CMD<9>	400HM	2	9
FBD_CMD<10>	400HM	2	10
FBD_CMD<11>	400HM	2	11
FBD_CMD<12>	400HM	2	12
FBD_CMD<13>	400HM	2	13
FBD_CMD<14>	400HM	2	14
FBD_CMD<15>	400HM	2	15
FBD_CMD<16>	400HM	2	16
FBD_CMD<17>	400HM	2	17
FBD_CMD<18>	400HM	2	18
FBD_CMD<19>	400HM	2	19
FBD_CMD<20>	400HM	2	20
FBD_CMD<21>	400HM	2	21
FBD_CMD<23>	400HM	2	23
FBD_CMD<24>	400HM	2	24
FBD_CMD<25>	400HM	2	25
FBD_CMD<26>	400HM	2	26
FBD_CMD<27>	400HM	2	27
FBD_CMD<28>	400HM	2	28

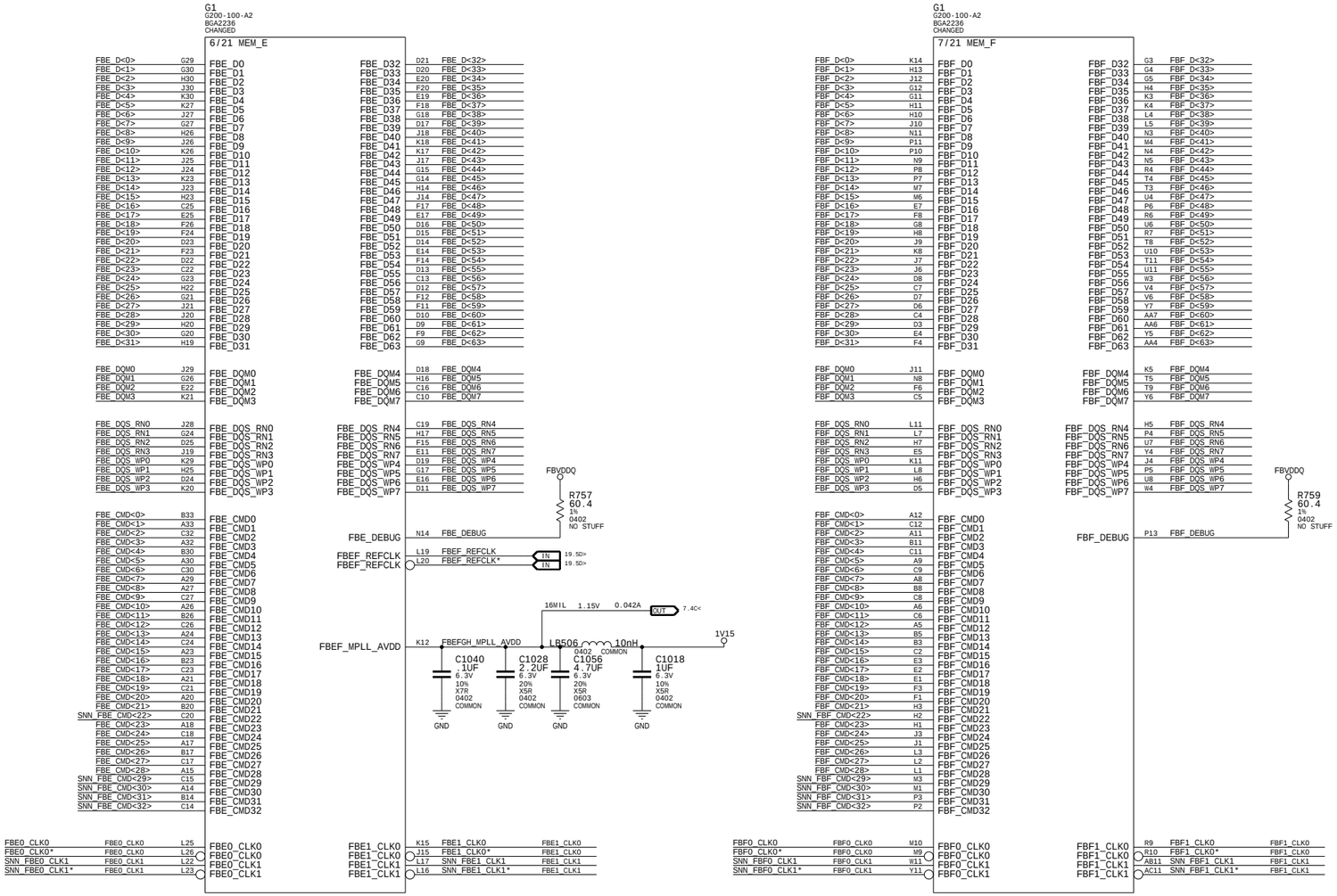
FBD0_CLK0	80DIFF	1	OUT 11.2A<
FBD0_CLK0*	80DIFF	1	OUT 11.2A<
FBD1_CLK0	80DIFF	1	OUT 11.2A<
FBD1_CLK0*	80DIFF	1	OUT 11.2A<

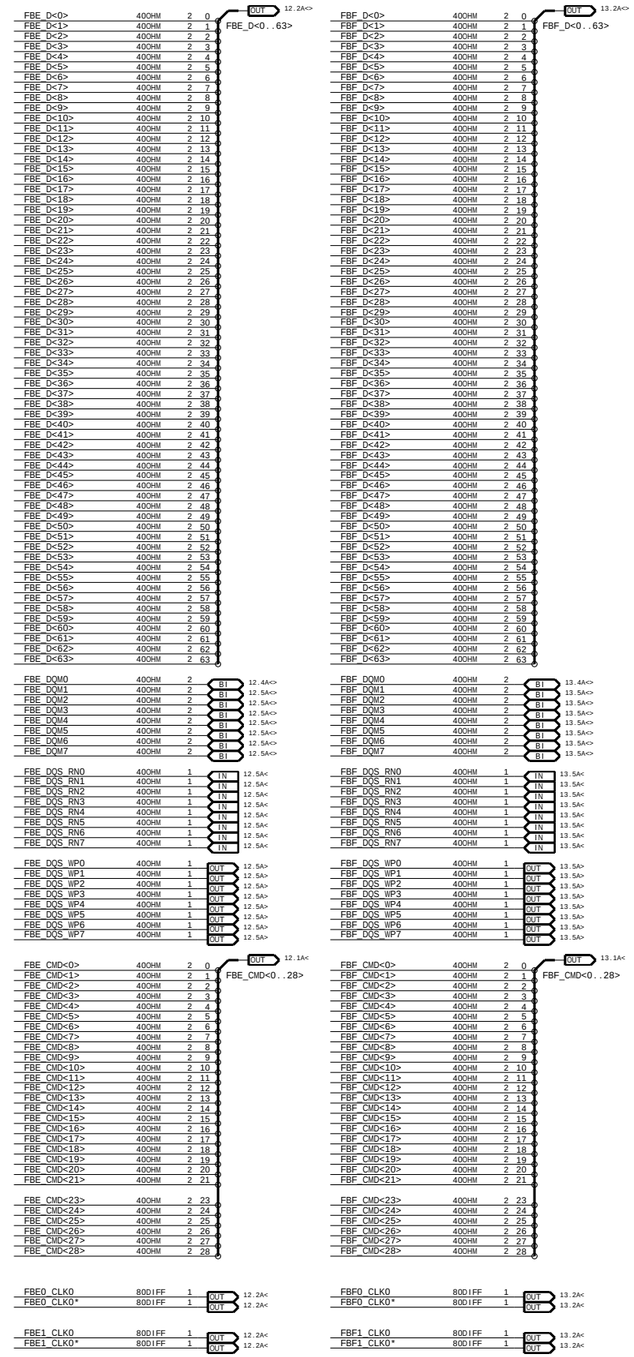
ASSEMBLY	DT, GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer C,D: GPU Section

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	5 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Framebuffer E,F: GPU Section



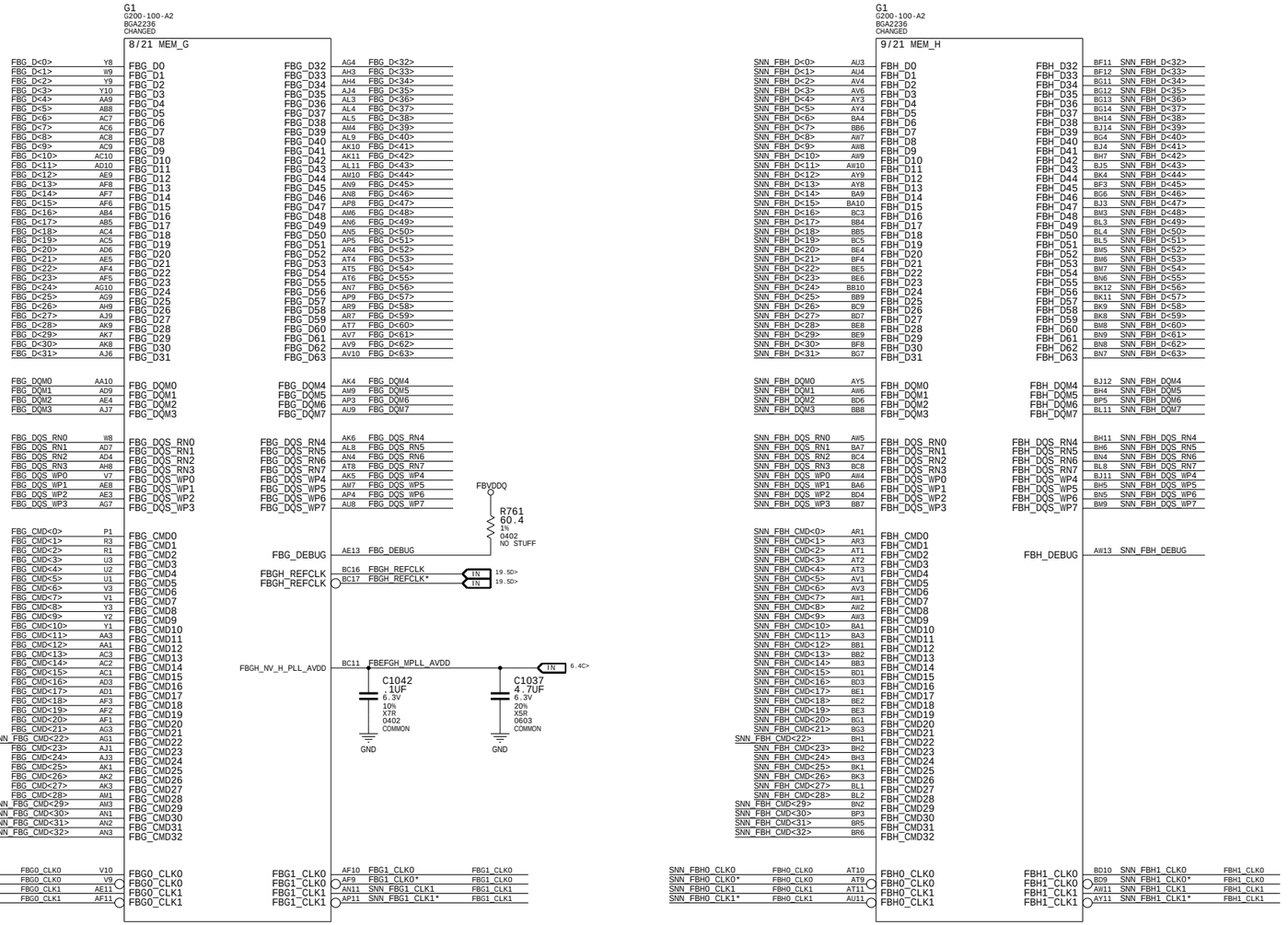


ASSEMBLY	DT, GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer E,F: GPU Section

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	6 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Framebuffer G,H: GPU Section



ASSEMBLY	DT, GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer G,H: GPU Section

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	7 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Framebuffer A: Memory Section

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer A: Memory Section

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	8 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Framebuffer B: Memory Section

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer B: Memory Section

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	9 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

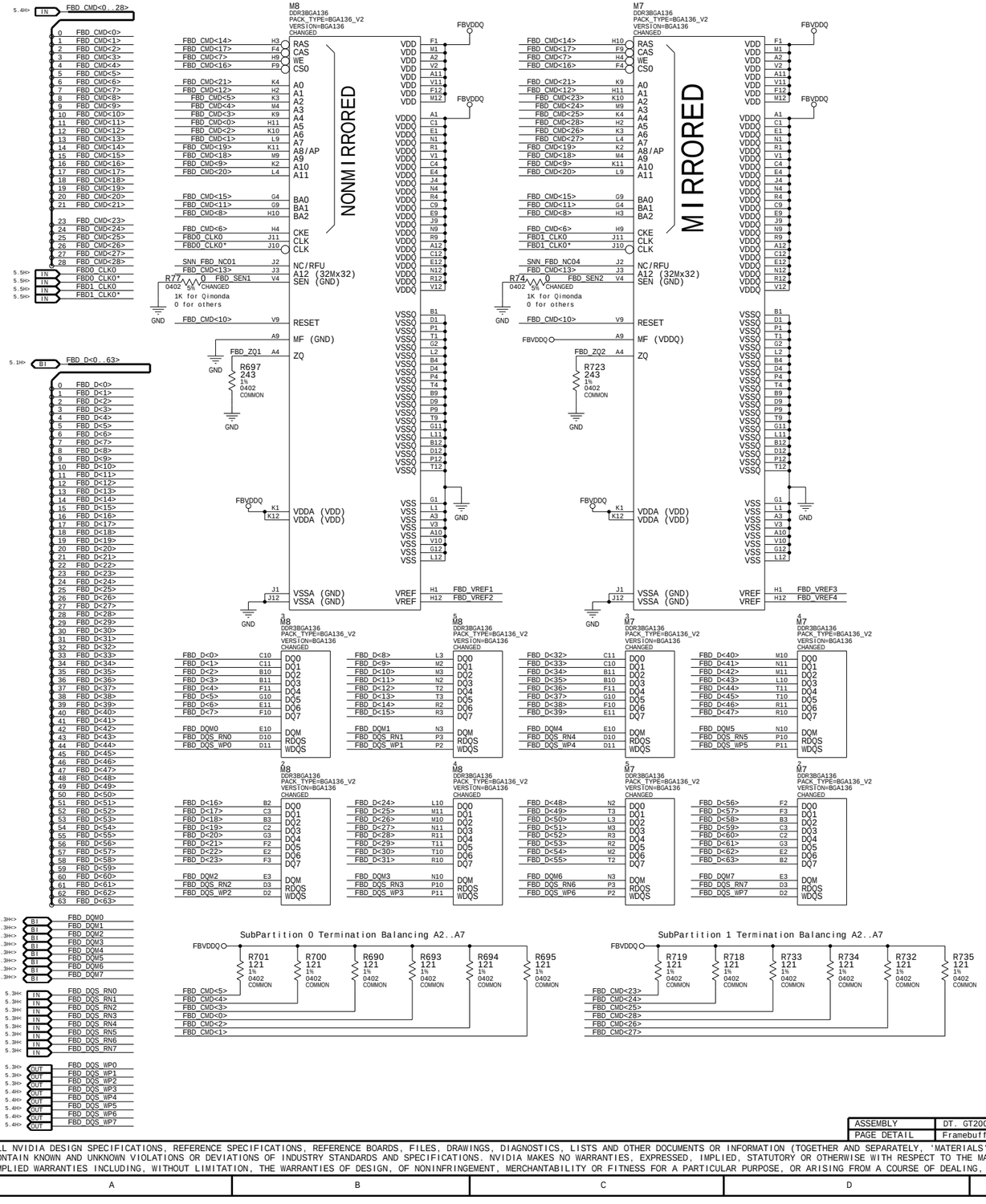
Framebuffer C: Memory Section

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer C: Memory Section

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	10 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Framebuffer D: Memory Section

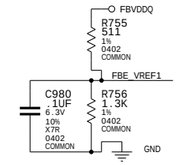


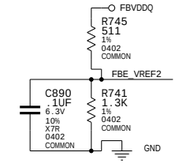
ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer D: Memory Section

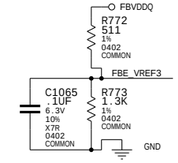
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

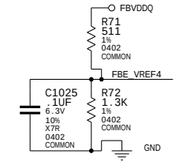
NV_PN	600-10654-0051-300 D		
ID	design	PAGE	11 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

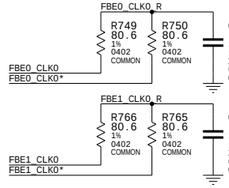
Framebuffer E: Memory Section

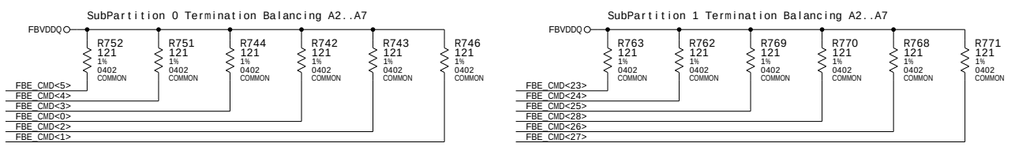


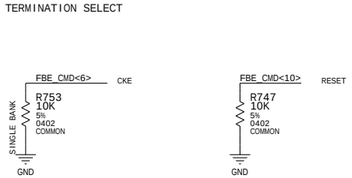












ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer E: Memory Section

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NV_PN	600-10654-0051-300 D		
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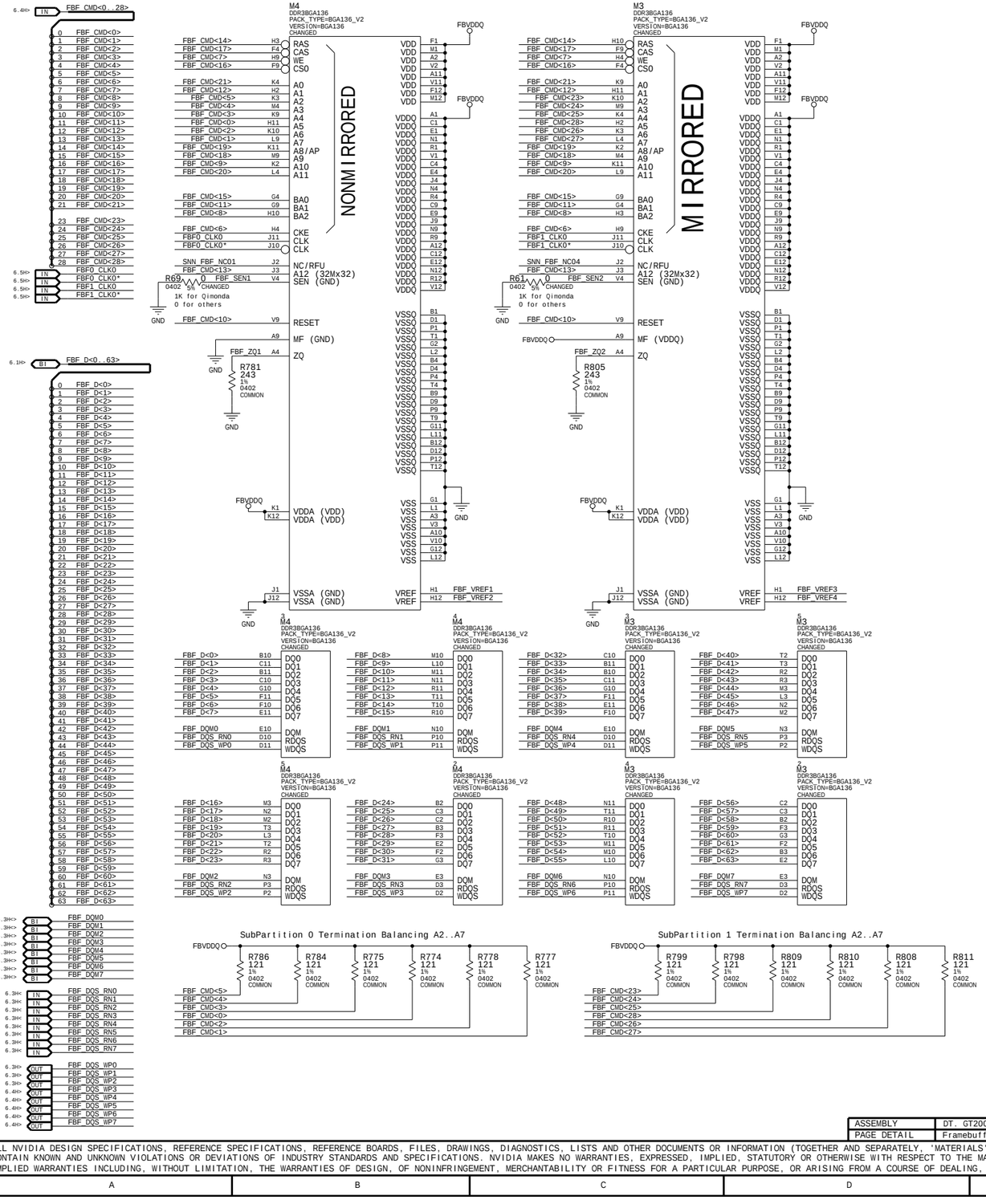
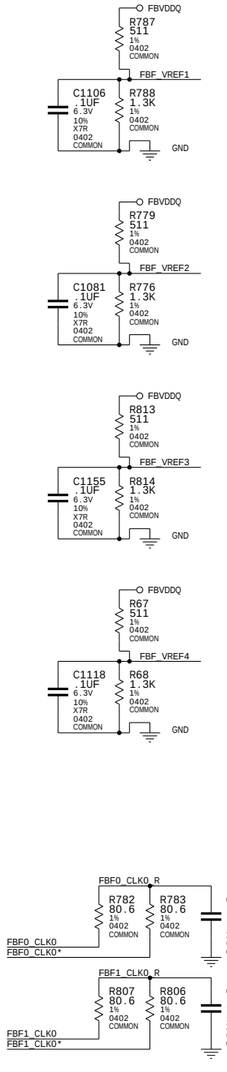
Framebuffer F: Memory Section





TERMINATION SELECT

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer F: Memory Section

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NV_PN	600-10654-0051-300 D		
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Framebuffer G: Memory Section

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer G: Memory Section

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NAME	Raite/Simon	DATE	22-OCT-2008

Framebuffer H: N/A

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer H: N/A

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NV_PN	600-10654-0051-300 D		
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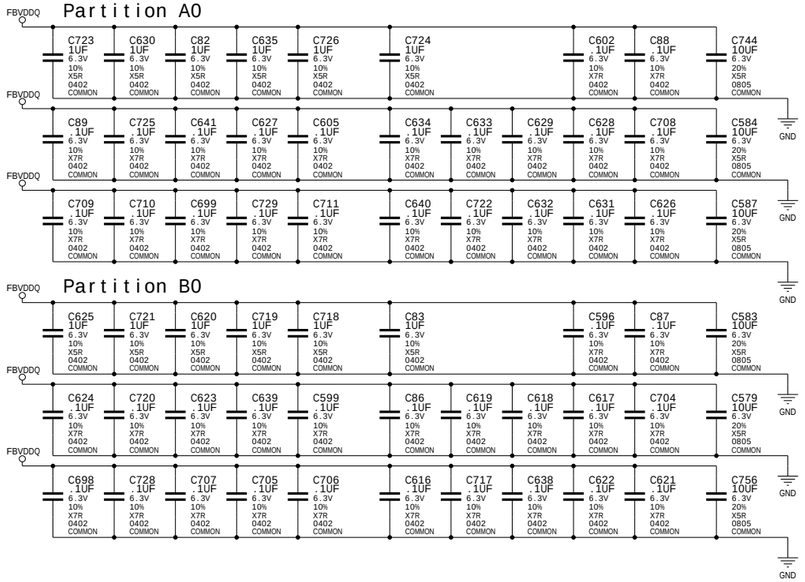
Decoupling: Memory Section A-D

Banks A-D FBVDD/Q
Combined Distributed Capacitance
280 uF

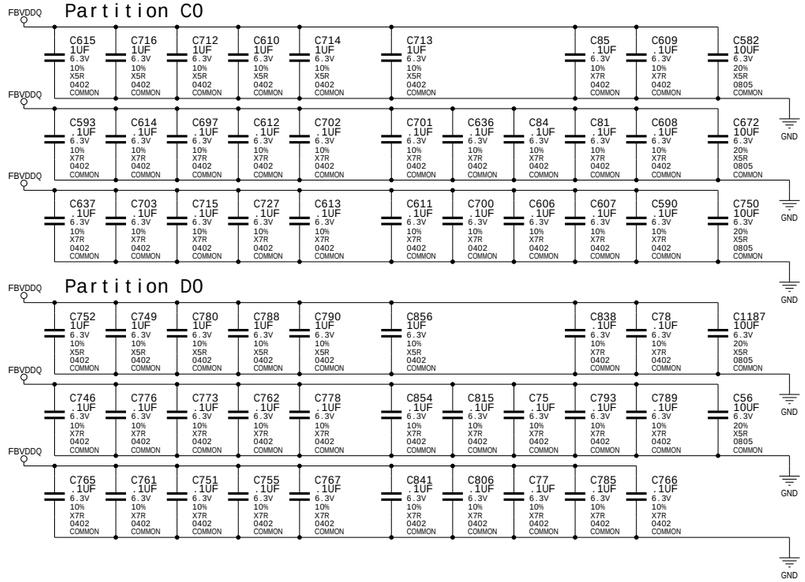
Decoupling for FBVDDQ

Partition A0



Partition B0

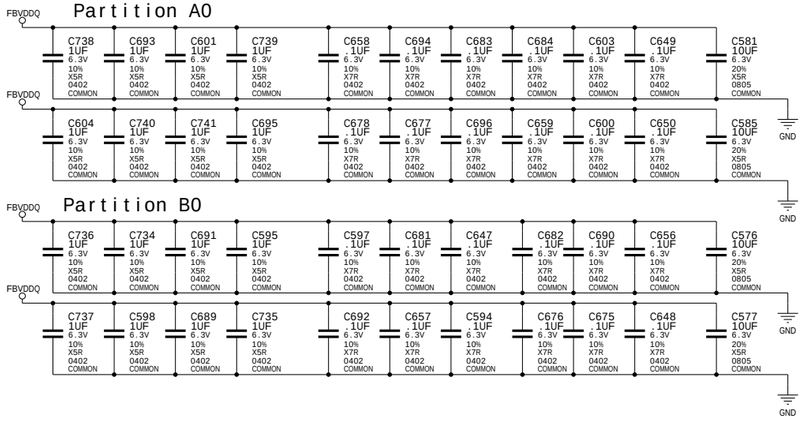
Partition C0



Partition D0

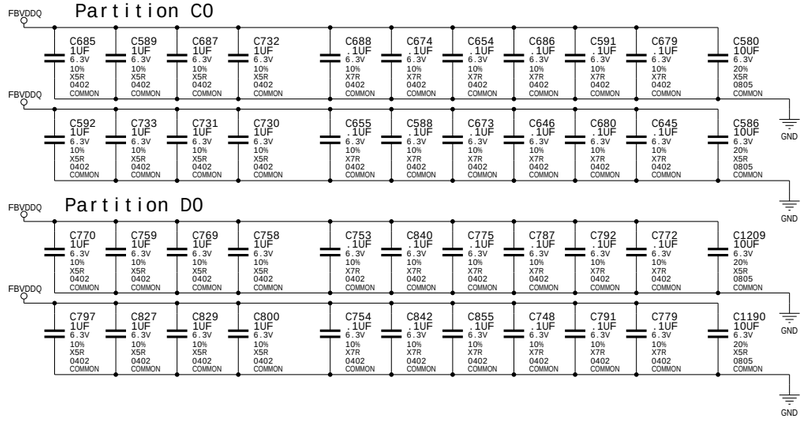
Decoupling for FBVDDQ

Partition A0



Partition B0

Partition C0



Partition D0

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Decoupling: Memory Section A-D

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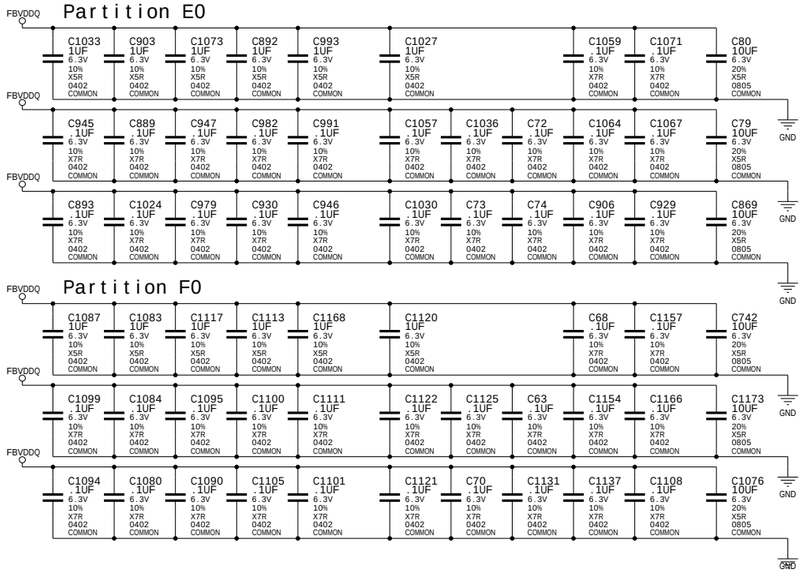
Decoupling: Memory Section E-G

Banks E-G FBVDD/Q
Combined Distributed Capacitance
210 uF

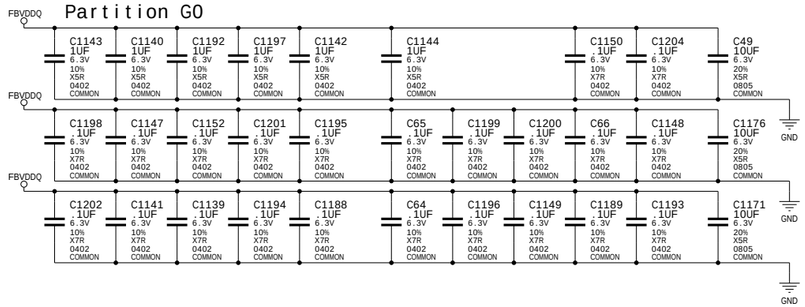
Decoupling for FBVDDQ

Partition E0



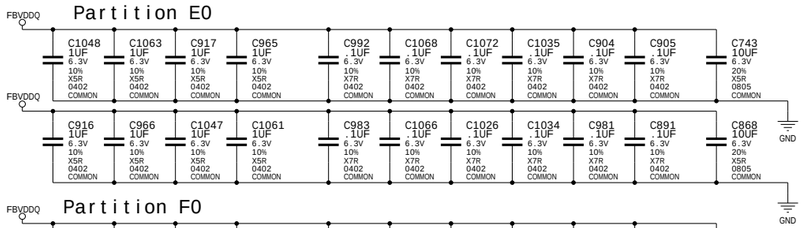
Partition F0

Partition G0

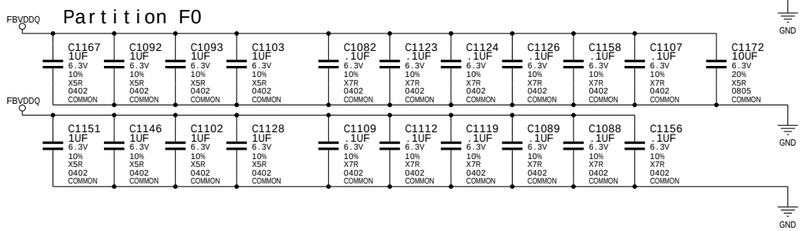


Decoupling for FBVDDQ

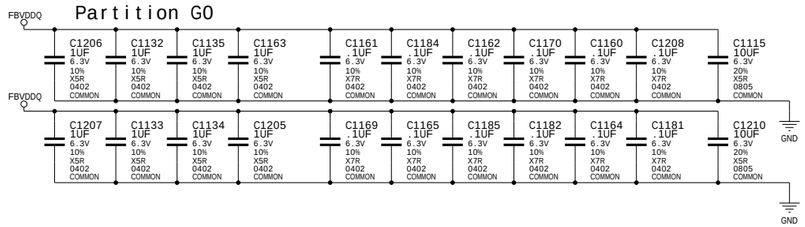
Partition E0



Partition F0



Partition G0



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Decoupling: Memory Section E-G

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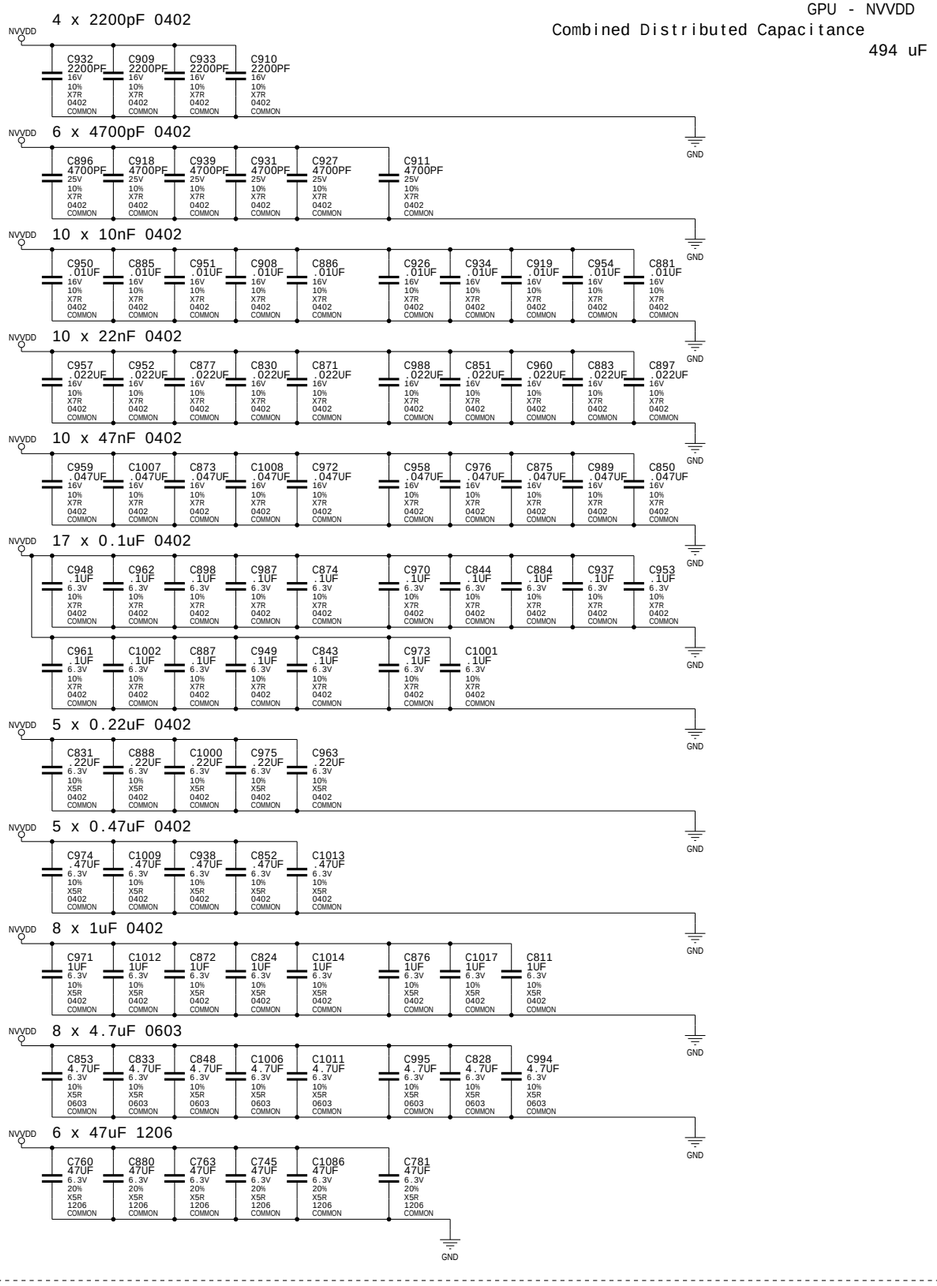
Decoupling: GPU (NVVDD, FBVDDQ)

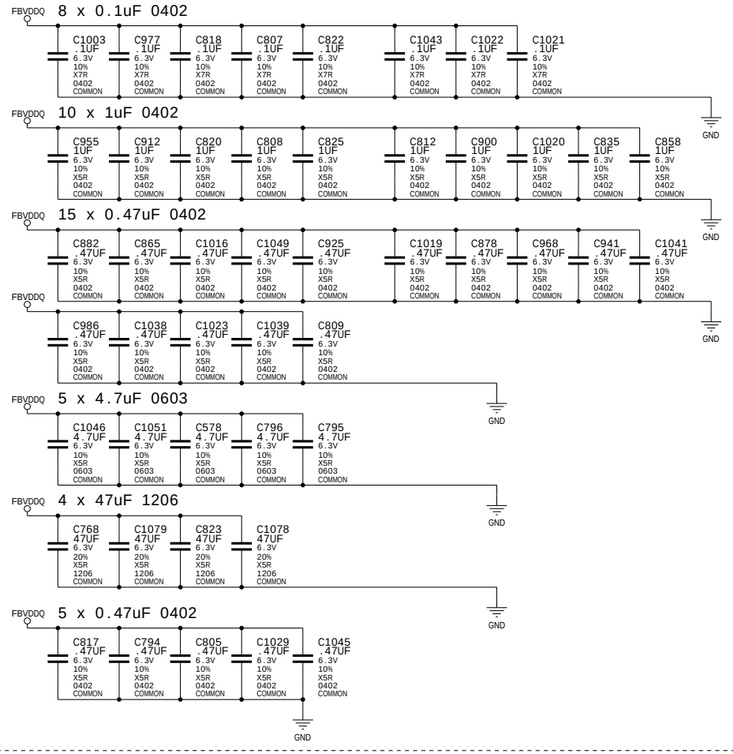
Decoupling for NVVDD (under GPU)

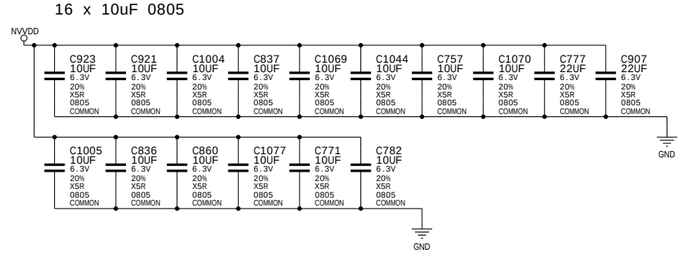
GPU - NVVDD
Combined Distributed Capacitance
494 uF



Decoupling for FBVDDQ (under GPU)

GPU - FBVDD/Q
Combined Distributed Capacitance
230 uF





ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Decoupling: GPU (NVVDD, FBVDDQ)

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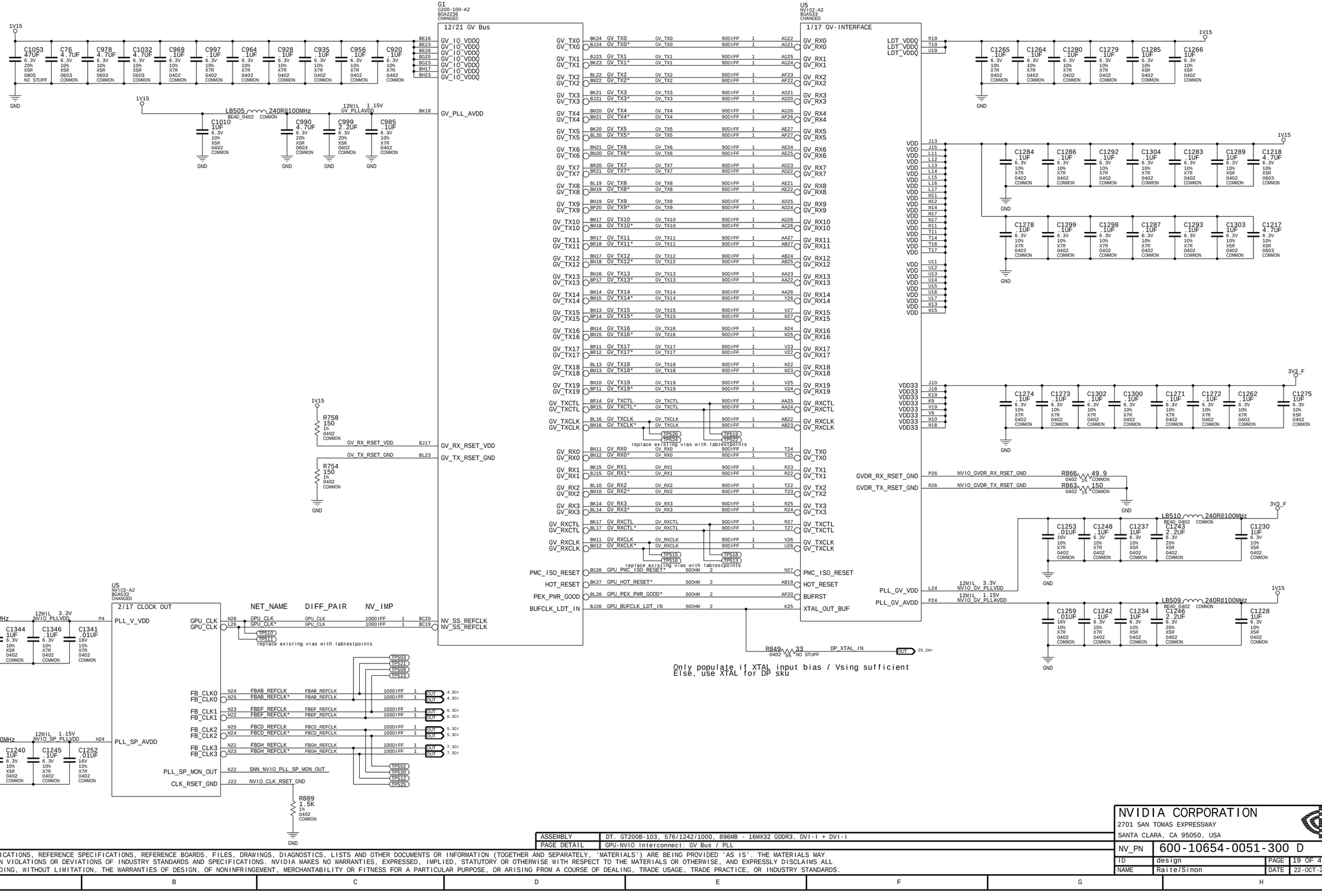
GPU-NVIO Interconnect: GV Bus / PLL



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	GPU-NVIO Interconnect: GV Bus / PLL

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NV_PN	600-10654-0051-300 D		
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Display: DACA (Middle DVI-I)

Desktop STEREO (option)

To support Desktop Card Stereo Out via DDC

28.3F> 21.2A< IN GPIO13_STEREO — R896 33 0402 5% NO STUFF — GPIO13_STEREO_DACA

R900 10K 5% 0402 NO STUFF NEAR MOSFET — GND

1G1D1S — Q533 BSS138 SOT23_1G1D1S NO STUFF

MAX_VOLTAGE=50V
MAX_CURRENT=0.22A@11C
0.2Ω_ON=1.5V
MAX_CURRENT=0.88A
MAX_WATTAGE=0.36W@25C
V_BE_GS=+/-20V

DDC isolation from GPU to Micro-Controller when in Hybrid Power mode

32.6F> 34.1D< 40.2E< 50.2J<

IN HYBRID_PWR_EN

U2 IDTQS3VH126 XSOP16_SECT NO STUFF

R933 33 0402 5% COMMON — I2C1_SCL_QS — A 11 / B 10 — I2C1_SCL_R

R940 0 0402 5% COMMON — BE 12

R932 33 0402 5% COMMON — I2C1_SDA_QS — A 14 / B 13 — I2C1_SDA_R

R941 0 0402 5% COMMON — BE 15

NEAR VAIO

U2 IDTQS3VH126 XSOP16_SECT NO STUFF

OUT 32.1F>

Note: May be possible to remove DDC clamp diodes

5V — R956 2.2K 5% 0402 COMMON — R957 2.2K 5% 0402 COMMON — BI 32.1G<>

I2C1_SCL_R — LB523 240R@100MHz BEAD_0402 COMMON — I2C1_SCL_CON — OUT 24.3G<

I2C1_SDA_R — LB524 240R@100MHz BEAD_0402 COMMON — I2C1_SDA_CON — BI 24.3G<

D526 BAV99 SOT23 100V 100MA COMMON — C1365 22PF 50V 5% C0G 0402 COMMON — GND

D527 BAV99 SOT23 100V 100MA COMMON — C1366 22PF 50V 5% C0G 0402 COMMON — GND

U5 NV102-A2 BGA533 CHANGED

3/17 DAC_A

3V3_F — LB515 240R@100MHz BEAD_0402 COMMON — 12MIL DACA_VDD 3.3V — DACA_VDD R9

C1317 1UF 6.3V 10% X5R 0402 COMMON — C1315 2.2UF 20% X5R 0402 COMMON — C1321 1UF 6.3V 10% X5R 0402 COMMON — C1319 1UF 6.3V 10% X7R 0402 COMMON — GND

I2C1_SCL — AD11 I2C1_SCL
I2C1_SDA — AD10 I2C1_SDA

DACA_HSYNC — U2 DACA_HSYNC
DACA_VSYNC — T2 DACA_VSYNC

DACA_RED — R1 DACA_RED
DACA_GREEN — T1 DACA_GREEN
DACA_BLUE — P2 DACA_BLUE

12MIL DACA_VREF — P6 DACA_VREF
12MIL DACA_RSET — R5 DACA_RSET
P9 DACA_AGND

DACA_IDUMP — T5

C1330 .01UF 16V 10% X7R 0402 COMMON — GND

R924 124 1% 0402 NO STUFF — GND
R925 124 1% 0402 COMMON — GND

Additional resistor for RSET trim
Both values must change if used

R948 150 1% 0402 COMMON — GND
R949 150 1% 0402 COMMON — GND
R950 150 1% 0402 COMMON — GND

NEAR NVIO

U3 74ACT08

NV_CRITICAL_NET=1 NV_IMPEDANCE=50OHM

4 / 5 / 6 / 7 — 14 — 74ACT_SO COMMON — GND

DACA_HSYNC_BUF_R

R946 33 0402 5% COMMON — DACA_HSYNC_BUF — L1 68nH 0603 COMMON — DACA_HSYNC_CON — OUT 24.4G<

R947 33 0402 5% NO STUFF

D1 BAV99 SOT23 100V 100MA COMMON — C5 8.2PF 50V +/-0.5PF C0G 0402 COMMON — GND

U3 74ACT08

NV_CRITICAL_NET=1 NV_IMPEDANCE=50OHM

10 / 9 / 8 / 7 — 14 — 74ACT_SO COMMON — GND

DACA_VSYNC_BUF_R

R955 33 0402 5% COMMON — DACA_VSYNC_BUF — L4 68nH 0603 COMMON — DACA_VSYNC_CON — OUT 24.3G<

R951 33 0402 5% NO STUFF

D7 BAV99 SOT23 100V 100MA COMMON — C12 8.2PF 50V +/-0.5PF C0G 0402 COMMON — GND

NV_CRITICAL_NET=1 NV_IMPEDANCE=75OHM

3V3 — D524 BAV99 SOT23 100V 100MA COMMON — GND

R967 150 1% 0402 COMMON — C1361 6.8PF 50V +/-0.5PF C0G 0402 COMMON — GND

L505 27nH 0603 COMMON

C1371 6.8PF 50V +/-0.5PF C0G 0402 COMMON — GND

DACA_RED_CON — OUT 24.3G<

NV_CRITICAL_NET=1 NV_IMPEDANCE=75OHM

3V3 — D525 BAV99 SOT23 100V 100MA COMMON — GND

R968 150 1% 0402 COMMON — C1362 6.8PF 50V +/-0.5PF C0G 0402 COMMON — GND

L509 27nH 0603 COMMON

C1375 6.8PF 50V +/-0.5PF C0G 0402 COMMON — GND

DACA_GREEN_CON — OUT 24.3G<

NV_CRITICAL_NET=1 NV_IMPEDANCE=75OHM

3V3 — D523 BAV99 SOT23 100V 100MA COMMON — GND

R966 150 1% 0402 COMMON — C1360 6.8PF 50V +/-0.5PF C0G 0402 COMMON — GND

L504 27nH 0603 COMMON

C1370 6.8PF 50V +/-0.5PF C0G 0402 COMMON — GND

DACA_BLUE_CON — OUT 24.3G<

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Display: DACA (Middle DVI-I)

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Display: DACC (South DVI-I)

Desktop STEREO (option)

To support Desktop Card Stereo Out via DDC

28.3F> 20.2A< IN GPIO13_STEREO — R959 33 0402 5% NO STUFF — GPIO13_STEREO_DACC

NEAR MOSFET

Q544 BSS138 SOT23_1G1D1S NO STUFF

GND

DDC isolation from GPU to Micro-Controller when in Hybrid Power mode

32.4F> 32.1C> 40.2E> 36.2A< IN HYBRID_PWR_EN

U2 IDTQS3VH126 XSOP16_SECT NO STUFF

R19 33 0402 5% COMMON — I2C2_SCL_QS

R11 0 0402 5% COMMON

R10 33 0402 5% COMMON — I2C2_SDA_QS

R9 0 0402 5% COMMON

NEAR VAIO

OUT 32.1G> — I2C2_SCL_R

BI 32.1G<> — I2C2_SDA_R

R8 2.2K 5% 0402 COMMON

R7 2.2K 5% 0402 COMMON

5V

LB2 240R@100MHz BEAD_0402 COMMON — I2C2_SCL_CON — OUT 23.3G<

LB1 240R@100MHz BEAD_0402 COMMON — I2C2_SDA_CON — BI 23.3G<

D4 D3 BAV99 SOT23 100V 100MA COMMON

C2 C3 22PF 50V 5% C0G 0402 COMMON

Note: May be possible to remove DDC clamp diodes

U3 74ACT08 74ACT_SO COMMON

R938 33 0402 5% COMMON — DACC_HSYNC_BUF_R — NV_CRITICAL_NET=1 NV_IMPEDANCE=50OHM — DACC_HSYNC_BUF

R939 33 0402 5% NO STUFF

L3 68nH 0603 COMMON — DACC_HSYNC_CON — OUT 23.4G<

D6 BAV99 SOT23 100V 100MA COMMON

C1 8.2PF 50V +/-0.5PF C0G 0402 COMMON

R952 33 0402 5% COMMON — DACC_VSYNC_BUF_R — DACC_VSYNC_BUF

R953 33 0402 5% NO STUFF

L2 68nH 0603 COMMON — DACC_VSYNC_CON — OUT 23.3G<

D5 BAV99 SOT23 100V 100MA COMMON

C4 8.2PF 50V +/-0.5PF C0G 0402 COMMON

U5 NV102-A2 BGA533 CHANGED

5/17 DAC_C

3V3_F

LB513 240R@100MHz BEAD_0402 COMMON

C1324 1UF 6.3V 10% X5R 0402 COMMON

C1310 2.2UF 6.3V 20% X5R 0402 COMMON

C1308 1UF 6.3V 10% X5R 0402 COMMON

C1307 .1UF 6.3V 10% X7R 0402 COMMON

12MIL 3.3V DACC_VDD — DACC_VDD — AC9

I2C2_SCL AG10 I2C2_SCL

I2C2_SDA AF10 I2C2_SDA

DACC_HSYNC AE9 DACC_HSYNC

DACC_VSYNC AD9 DACC_VSYNC

DACC_RED AF8 DACC_RED

DACC_GREEN AG9 DACC_GREEN

DACC_BLUE AG7 DACC_BLUE

12MIL DACC_VREF — AC13 — DACC_VREF

12MIL DACC_RSET — AB12 — DACC_RSET

AF7 — DACC_AGND

DACC_IDUMP AD8

C1297 .01UF 16V 10% X7R 0402 COMMON

R897 124 1% 0402 NO STUFF

R899 124 1% 0402 COMMON

R923 150 1% 0402 COMMON

R915 150 1% 0402 COMMON

R919 150 1% 0402 COMMON

NEAR NVIO

Additional resistor for RSET trim
Both values must change if used

3V3 — L507 33nH 0603 COMMON — DACC_RED_CON — OUT 23.3G<

R964 150 1% 0402 COMMON

C1358 6.8PF 50V +/-0.5PF C0G 0402 COMMON

C1373 6.8PF 50V +/-0.5PF C0G 0402 COMMON

D521 BAV99 SOT23 100V 100MA COMMON

L508 33nH 0603 COMMON — DACC_GREEN_CON — OUT 23.3G<

R965 150 1% 0402 COMMON

C1359 6.8PF 50V +/-0.5PF C0G 0402 COMMON

C1374 6.8PF 50V +/-0.5PF C0G 0402 COMMON

D522 BAV99 SOT23 100V 100MA COMMON

L506 33nH 0603 COMMON — DACC_BLUE_CON — OUT 23.3G<

R963 150 1% 0402 COMMON

C1357 6.8PF 50V +/-0.5PF C0G 0402 COMMON

C1372 6.8PF 50V +/-0.5PF C0G 0402 COMMON

D520 BAV99 SOT23 100V 100MA COMMON

NV_CRITICAL_NET=1 NV_IMPEDANCE=50OHM

NV_CRITICAL_NET=1 NV_IMPEDANCE=75OHM

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Display: DACC (South DVI-I)

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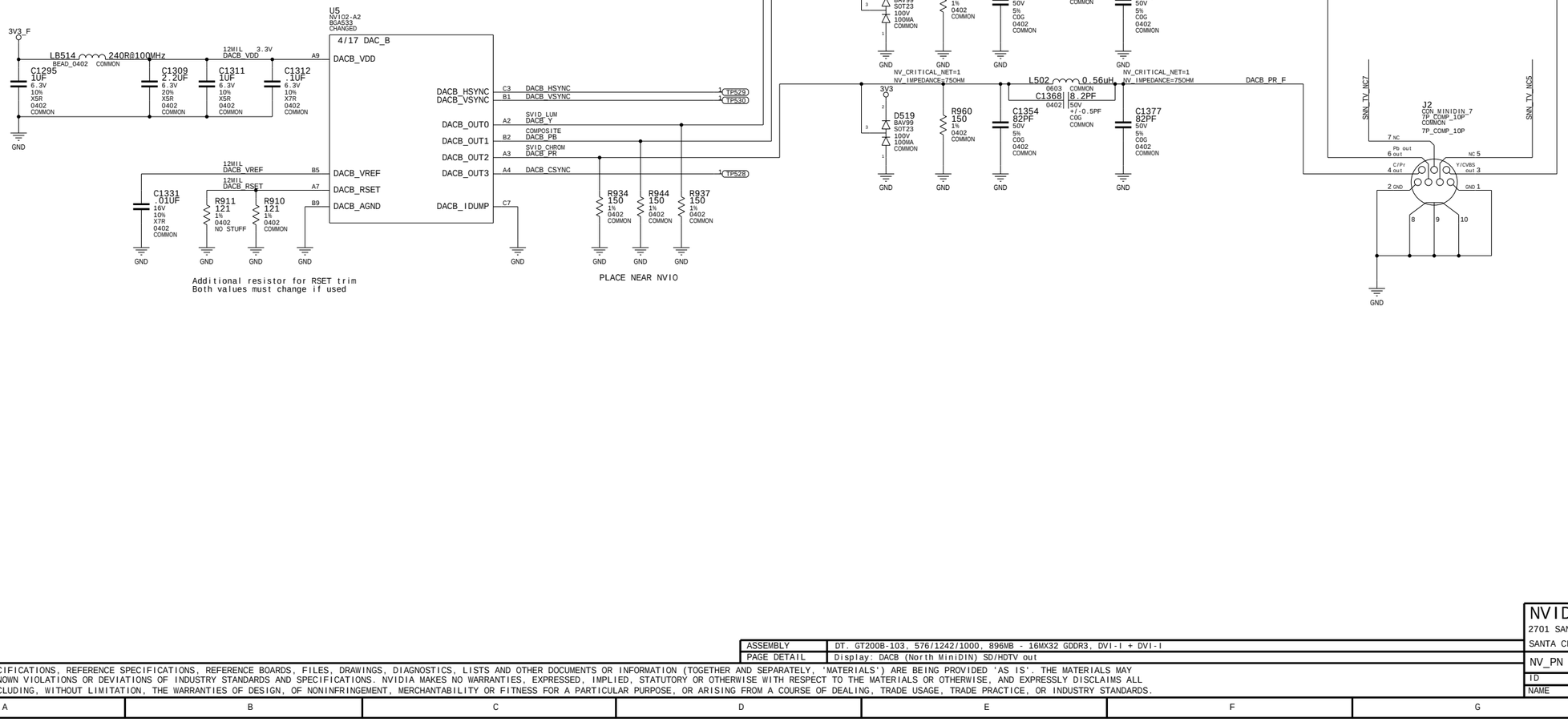
Display: DACB (North MiniDIN) SD/HDTV out



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Display: DACB (North MiniDIN) SD/HDTV out

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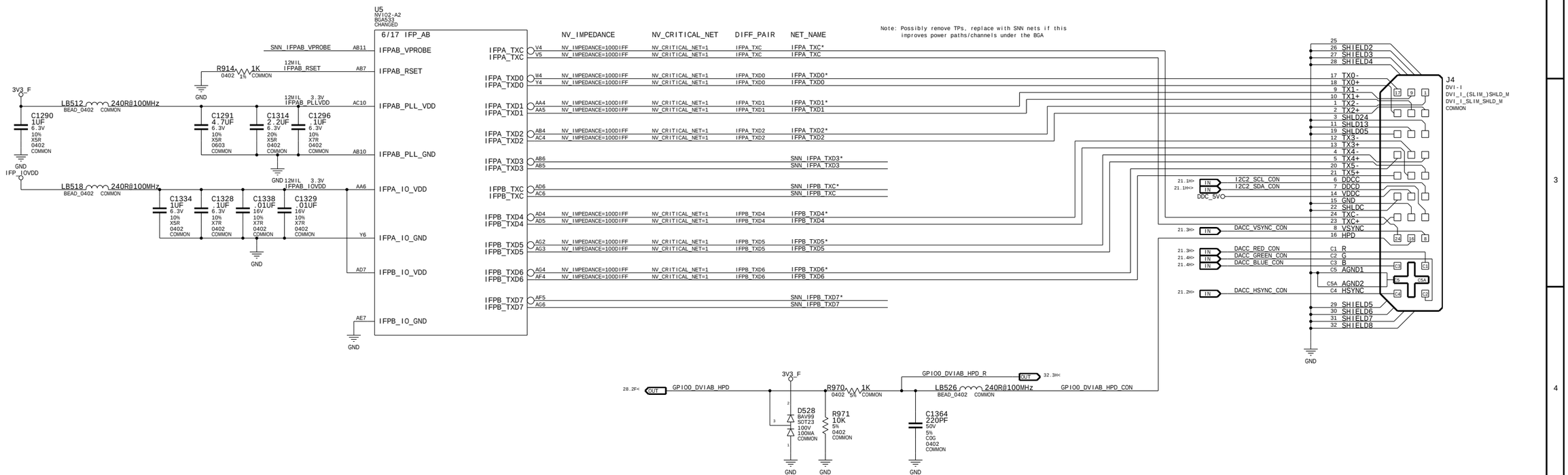
NAME	Raite/Simon	DATE	22-OCT-2008

Display: IFPAB for South DVI-I (with DACC)



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Display: IFPAB for south DVI-I (with DACC)

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2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
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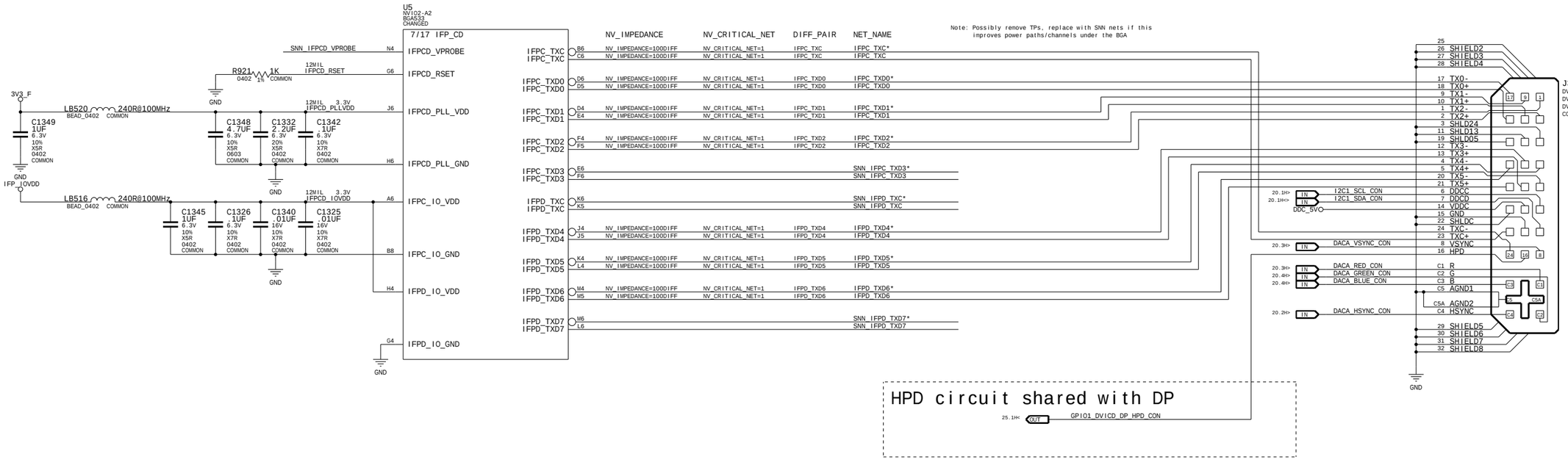
NAME	Raite/Simon	DATE	22-OCT-2008

Display: IFPCD for middle DVI-I (with DACA)



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Display: IFPCD for middle DVI-I (with DACA)

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NV_PN	600-10654-0051-300 D		
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NAME	Raite/Simon	DATE	22-OCT-2008

Display: DP - Analogix

* ANX9805 support

pin 76 - GPIO3 to DP mode, from pin 13, grounded on ANX9802
  - place GND resistor away from ANX device if needed

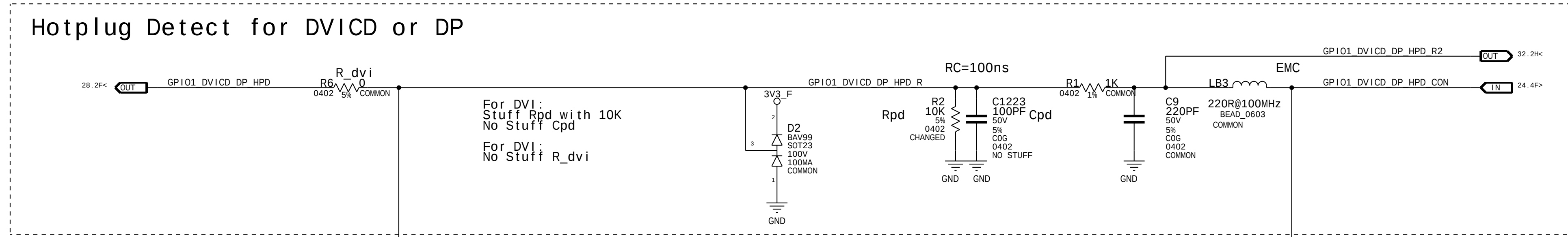
pin 74 - GPIO2, grounded on ANX9802
  - place GND resistor away from ANX device if needed

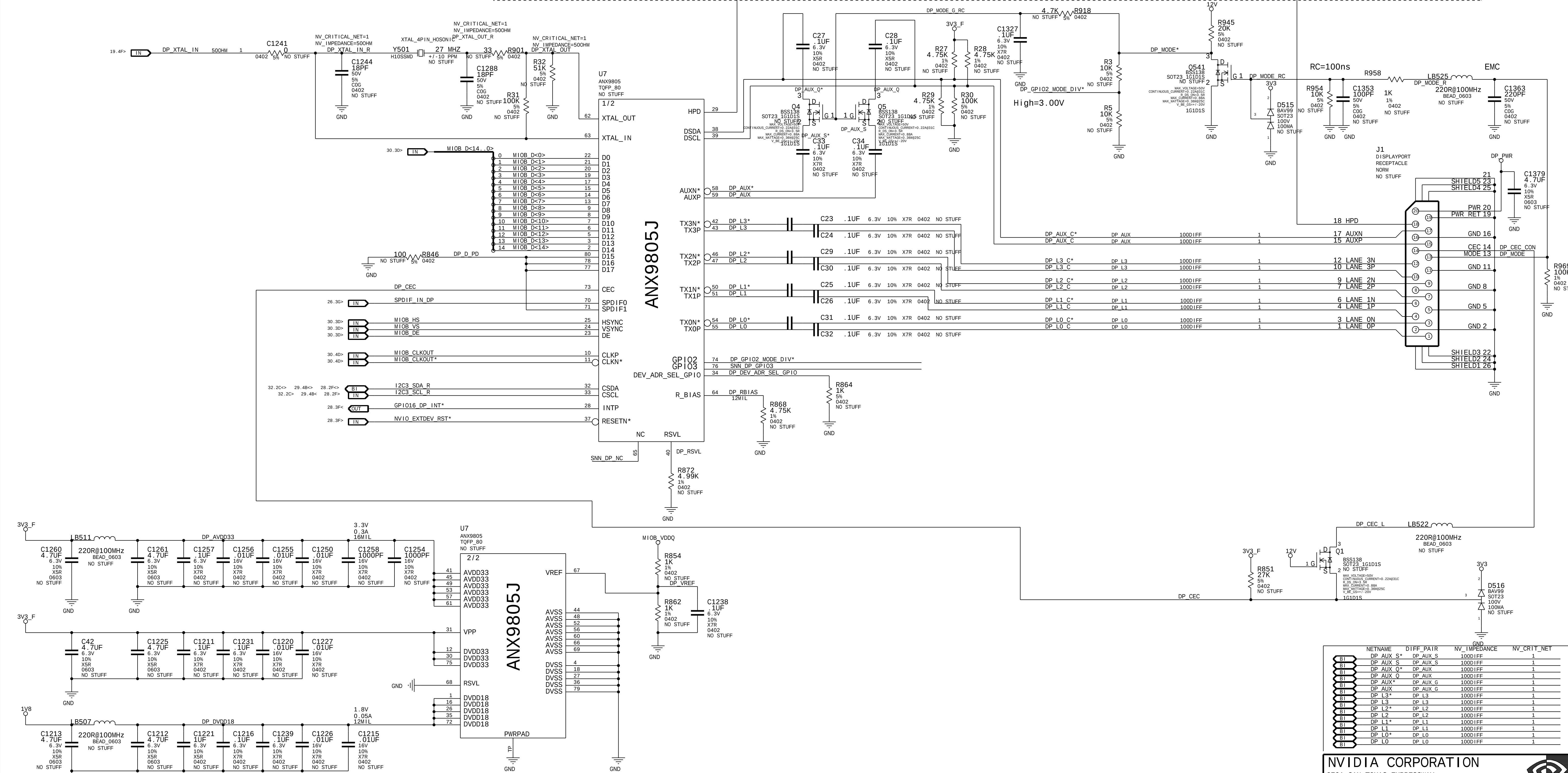
pin 73 - CEC support via FET and pull-up, grounded on ANX9802
  - place GND resistor away from ANX device if needed

pin 71 - SPDIF1 - tie to GND, input select 0/1 through internal register

pin 70 - SPDIF0 - support for Audio input, grounded on ANX9802
  - place GND resistor away from ANX device if needed

pin 68 - NC - tie to GND





	NETNAME	DIFF_PAIR	NV_IMPEDANCE	NV_CRIT_NET
BI	DP_AUX_S*	DP_AUX_S	100DIFF	1
BI	DP_AUX_S	DP_AUX_S	100DIFF	1
BI	DP_AUX_Q*	DP_AUX	100DIFF	1
BI	DP_AUX_Q	DP_AUX	100DIFF	1
BI	DP_AUX*	DP_AUX_G	100DIFF	1
BI	DP_AUX	DP_AUX_G	100DIFF	1
BI	DP_L3*	DP_L3	100DIFF	1
BI	DP_L3	DP_L3	100DIFF	1
BI	DP_L2*	DP_L2	100DIFF	1
BI	DP_L2	DP_L2	100DIFF	1
BI	DP_L1*	DP_L1	100DIFF	1
BI	DP_L1	DP_L1	100DIFF	1
BI	DP_L0*	DP_L0	100DIFF	1
BI	DP_L0	DP_L0	100DIFF	1

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ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Display: DP - Analogix

NV_PN	600-10654-0051-300 D		
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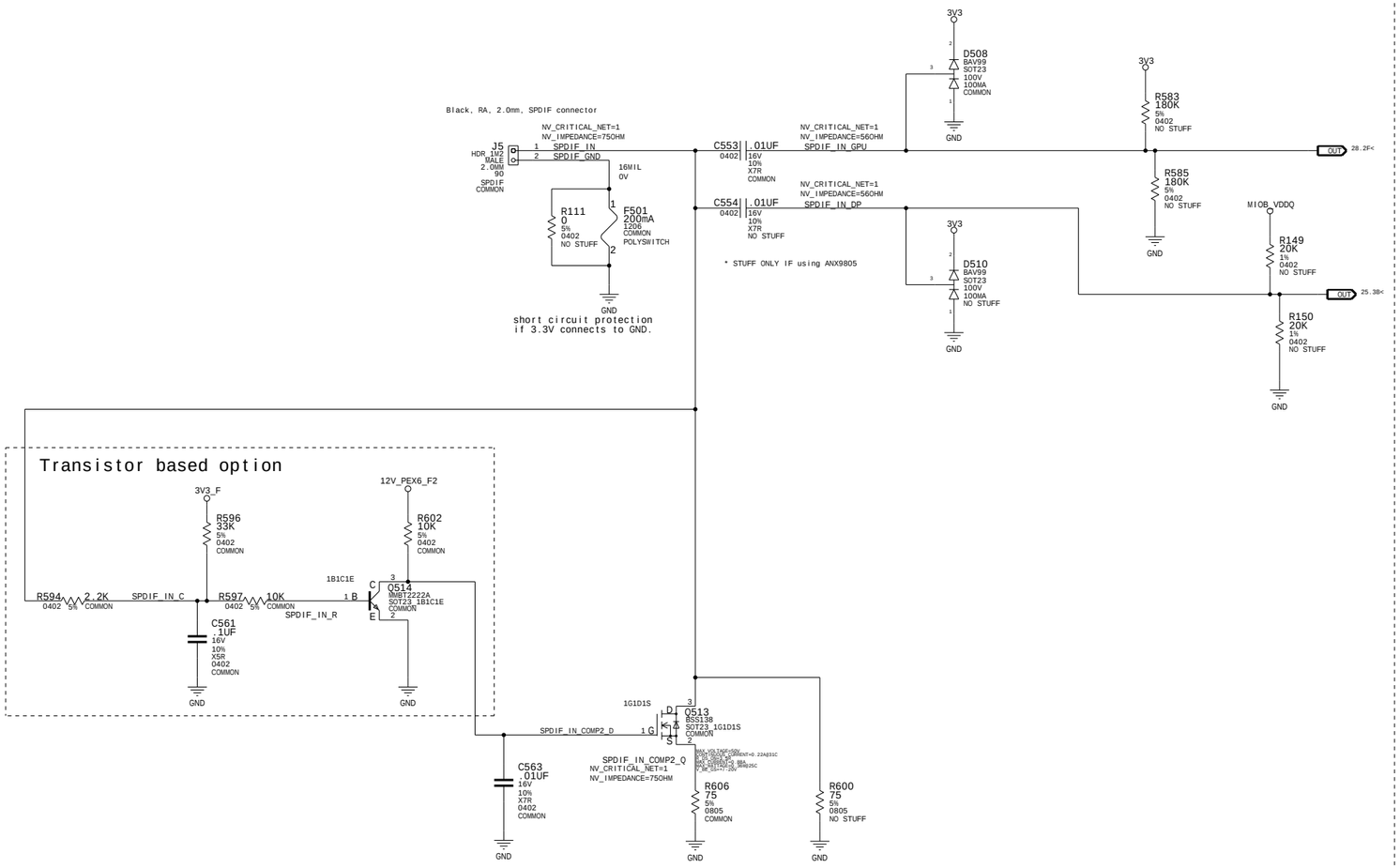
Connectors: SPDIF

SPDIF INPUT / Level Detection



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Connectors: SPDIF

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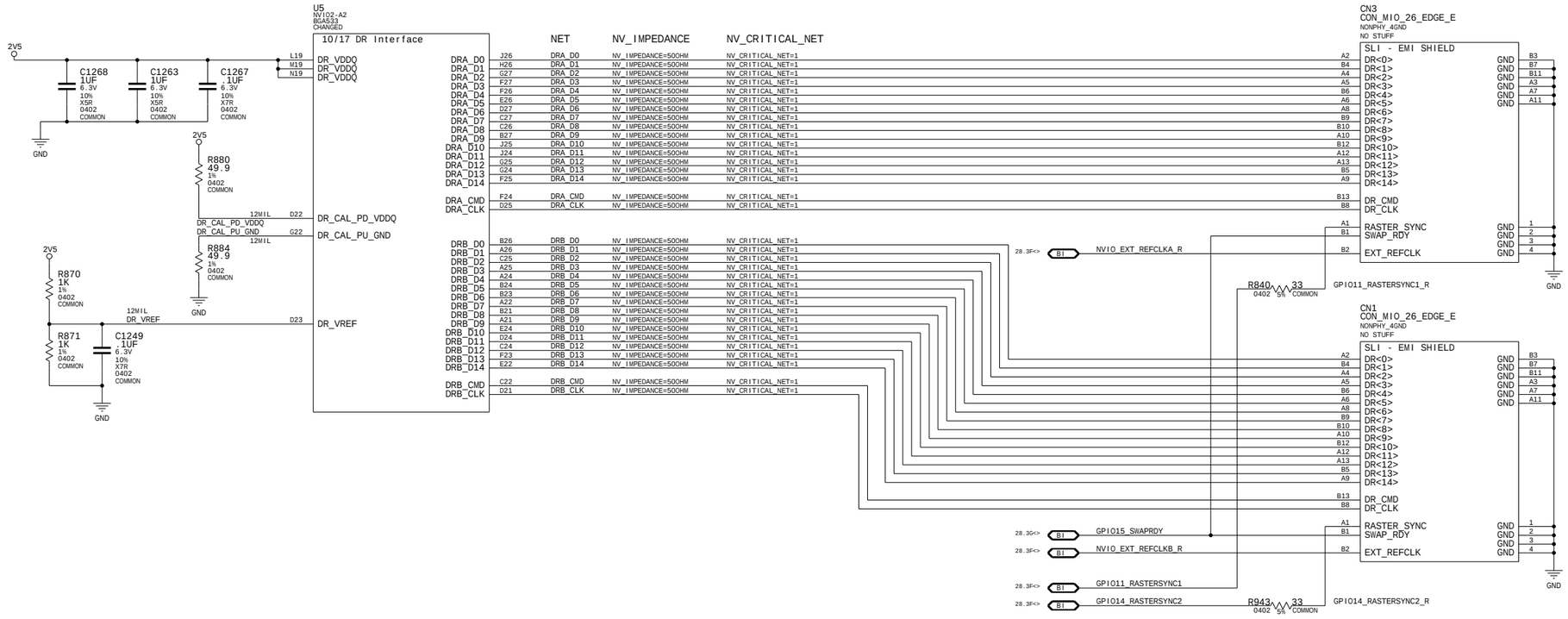
Connectors: DR Interface (Dual SLI)



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Connectors: DR Interface (Dual SLI)

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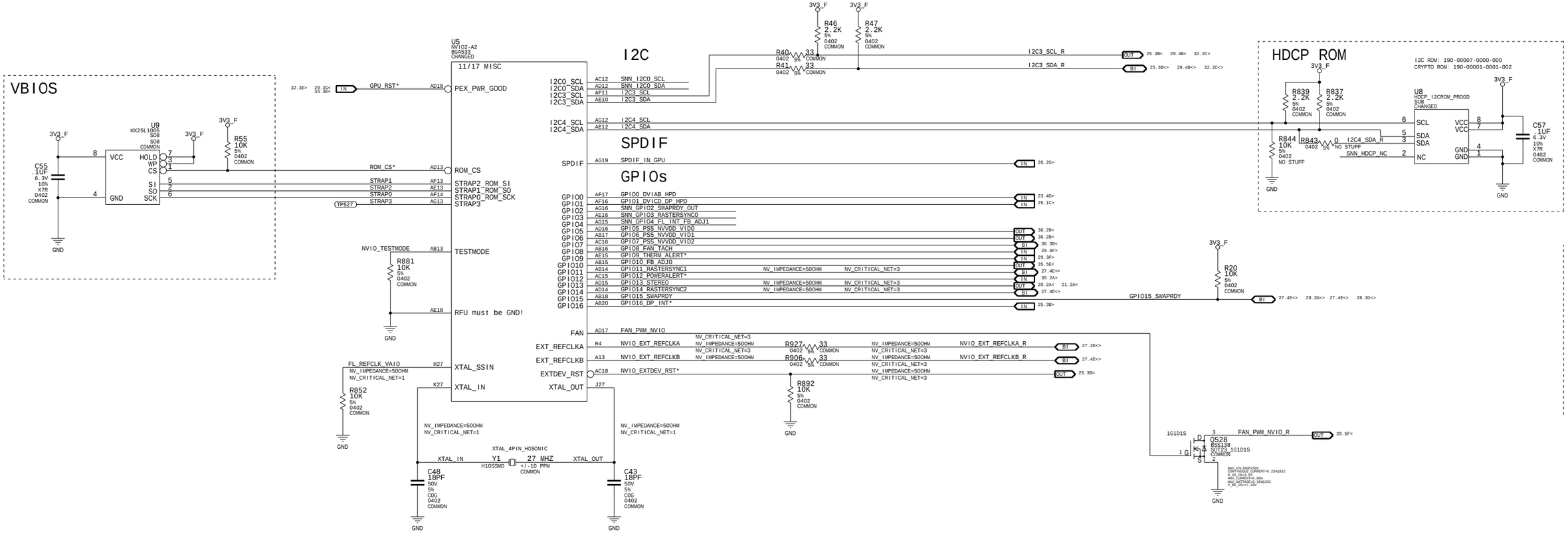
MISC: GPIO / XTAL / VBIOS / HDCP / I2C



ASSEMBLY	DT, GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	MISC: GPIO / XTAL / VBIOS / HDCP / I2C

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NV_PN	600-10654-0051-300 D		
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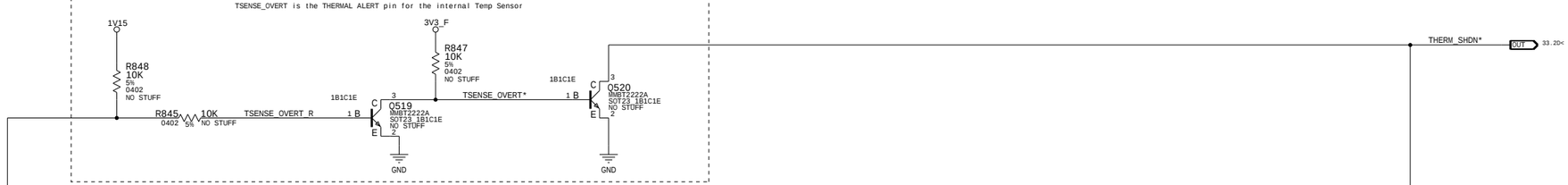
MISC: FAN / THERM

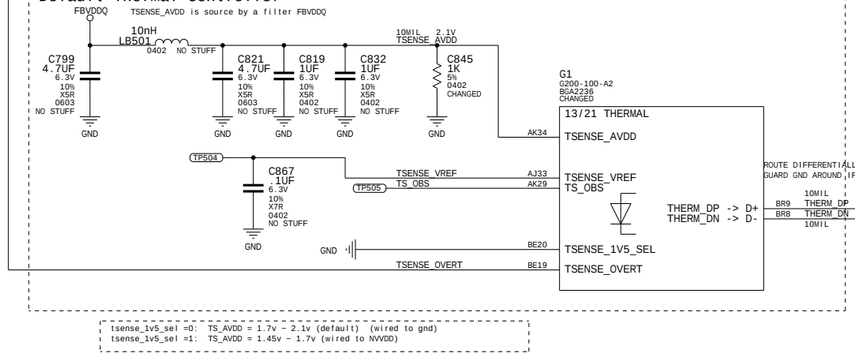
TSENSE_OVERT Level Shifter (1.15V to 3.3V)

TSENSE_OVERT is the THERMAL ALERT pin for the internal Temp Sensor



Internal GPU Thermal Sensor

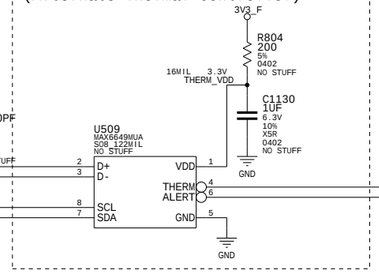
Default Thermal Controller



tsense_1v5_sel =0: TS_AVDD = 1.7v ~ 2.1v (default) (wired to gnd)
tsense_1v5_sel =1: TS_AVDD = 1.45v ~ 1.7v (wired to NVVDD)

LM99/MAX6649

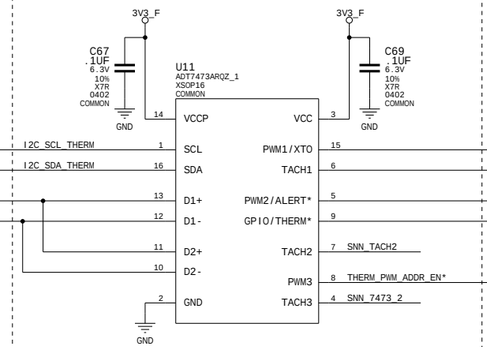
(Alternate Thermal Controller)

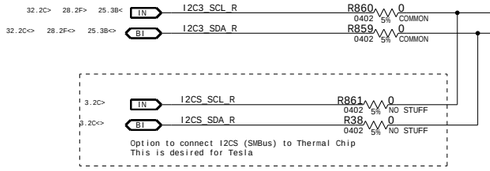


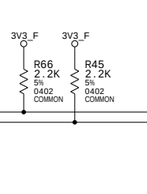
Note: POR internal thermal control
external controls will be DNI

ADT7473

(Secondary thermal controller choice)

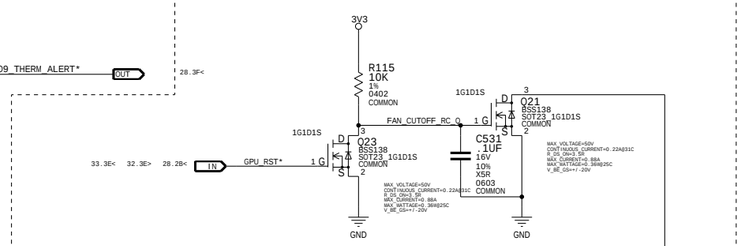




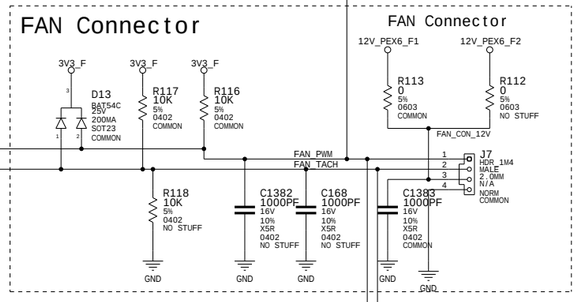


GPIO9_THERM_ALERT* OUT 28.3F<

FAN Connector



FAN Connector



GPU Driven Fan and Tach

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	MISC: FAN / THERM

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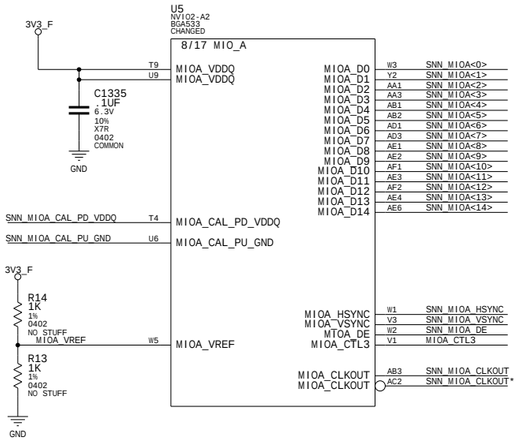
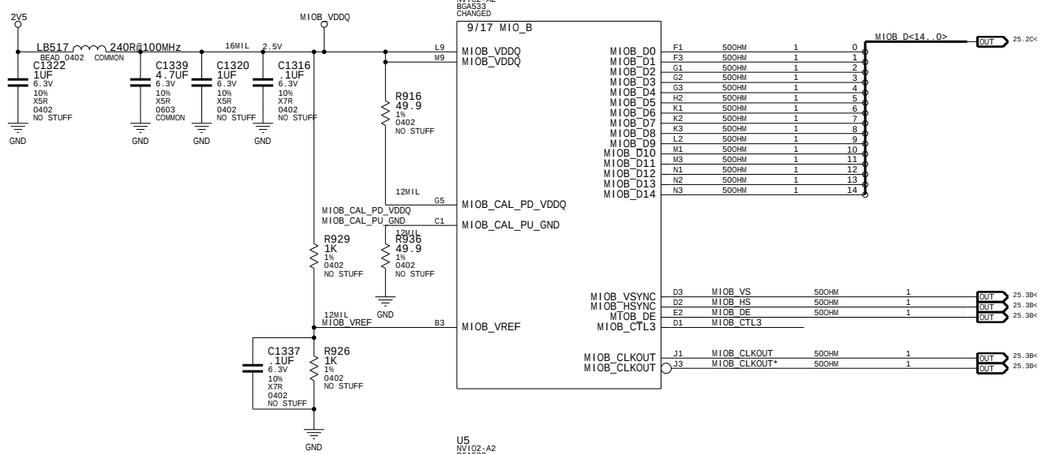
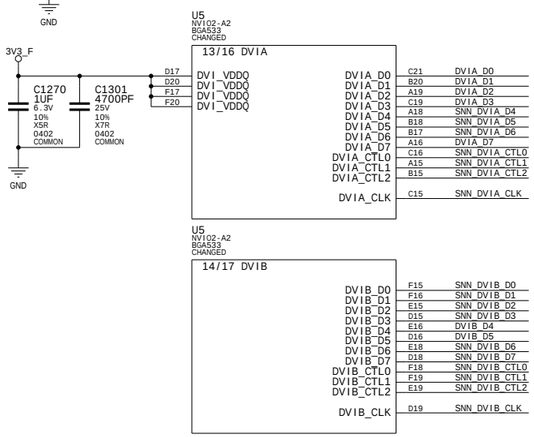
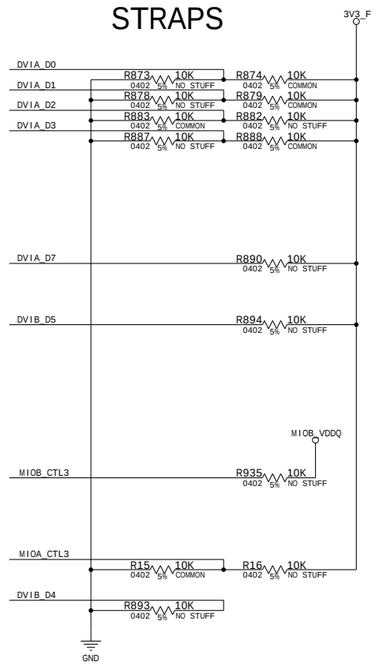
MISC: MIO / DVI / STRAPS









STRAP BITS BOOT0 = 0x101000

NR_:	USAGE	COMMENT
00 :	GV_WIDTH	DEFAULT=0x0 (WIDE)
01 :	SUB_VENDOR	DEFAULT=0x1 (FROM BIOS)
02 :	RAM_CFG[0]	
03 :	RAM_CFG[1]	
04 :	RAM_CFG[2]	
05 :	RAM_CFG[3]	
06 :	CRYSTAL	DEFAULT=0x0 (27MHz)
07 : 08 : 09 :	TV_MODE[0] TV_MODE[1] TV_MODE[2]	DEFAULT=0x1 (NTSC_J)
10 : 11 : 12 : 13 :	PCI_DEVID[0] PCI_DEVID[1] PCI_DEVID[2] PCI_DEVID[3]	SET BY BIOS DEFAULT=0x0
14 : 15 : 16 :	FB_SIZE[0] FB_SIZE[1] FB_SIZE[2]	DEFAULT=0x2 (256MB ??)
17 :	PEX_PLL_EN_TERM100	DEFAULT=0x0 (ENABLED)
18 : 19 : 20 : 21 :	3GIO_PAD_CFG_LUT_ADR[0] 3GIO_PAD_CFG_LUT_ADR[1] 3GIO_PAD_CFG_LUT_ADR[2] 3GIO_PAD_CFG_LUT_ADR[3]	DEFAULT=0x3 (DESKTOP_DEFAULT)
22 : 23 :	ROMTYPE[0] ROMTYPE[1]	DEFAULT=0x1 (AT25S)
24 : 25 : 26 : 27 :	USER[0] USER[1] USER[2] USER[3]	SET BY BIOS
28 :	PCI_DEVID_EXT	DEFAULT=0x0

STRAP BITS BOOT3 = 0x10100C

NR_:	USAGE	COMMENT
06 :	XCLK_555	DEFAULT=0x0
16 :	PCI_IOBAR	DEFAULT=0x1 0=DISABLE, 1=ENABLE

CFG	Config Width	Vendor
0000	Reserved	
0001	16Mx32 512-bit	Qimonda
0010	16Mx32 512-bit	Hynix*
0011	16Mx32 512-bit	Samsung*
0100	Reserved	
0101	32Mx32 512-bit	Qimonda
0110	32Mx32 512-bit	Hynix
0111	32Mx32 512-bit	Samsung
1000	Reserved	
1001	16Mx32 448-bit	Qimonda
1010	16Mx32 448-bit	Hynix
1011	16Mx32 448-bit	Samsung
1100	Reserved	
1101	32Mx32 448-bit	Qimonda
1110	32Mx32 448-bit	Hynix
1111	32Mx32 448-bit	Samsung

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	MISC: MIO / DVI / STRAPS

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Power and GND (GPU and NVIOx)

GPU SECTION GND

G1
G200-100-A2
BGA2236
CHANGED

19/21 GND1

AA11	GND	GND	AG17
AA13	GND	GND	AG18
AA15	GND	GND	AG19
AA16	GND	GND	AG2
AA17	GND	GND	AG20
AA18	GND	GND	AG21
AA19	GND	GND	AG22
AA2	GND	GND	AG23
AA20	GND	GND	AG24
AA21	GND	GND	AG25
AA22	GND	GND	AG26
AA23	GND	GND	AG27
AA24	GND	GND	AG28
AA25	GND	GND	AG29
AA26	GND	GND	AG30
AA27	GND	GND	AG31
AA28	GND	GND	AG32
AA29	GND	GND	AG33
AA30	GND	GND	AG34
AA31	GND	GND	AG35
AA32	GND	GND	AG36
AA33	GND	GND	AG43
AA34	GND	GND	AG45
AA35	GND	GND	AG48
AA36	GND	GND	AG5
AA43	GND	GND	AG51
AA45	GND	GND	AG54
AA48	GND	GND	AG8
AA5	GND	GND	AH15
AA51	GND	GND	AH16
AA54	GND	GND	AH17
AA8	GND	GND	AH18
AB15	GND	GND	AH19
AB16	GND	GND	AH20
AB17	GND	GND	AH21
AB18	GND	GND	AH22
AB19	GND	GND	AH24
AB20	GND	GND	AH25
AB21	GND	GND	AH26
AB22	GND	GND	AH27
AB23	GND	GND	AH28
AB24	GND	GND	AH29
AB25	GND	GND	AH30
AB26	GND	GND	AH31
AB27	GND	GND	AH32
AB28	GND	GND	AH36
AB29	GND	GND	AH33
AB30	GND	GND	AH34
AB31	GND	GND	AH35
AB32	GND	GND	AR2
AB33	GND	GND	AR43
AB34	GND	GND	AR45
AB35	GND	GND	AR48
AB36	GND	GND	AR5
AD11	GND	GND	AR51
AD13	GND	GND	AR54
AD2	GND	GND	AR8
AD28	GND	GND	AT15
AD29	GND	GND	AT17
AD43	GND	GND	AT19
AD45	GND	GND	AV54
AD48	GND	GND	AJ8
AD5	GND	GND	AM11
AD51	GND	GND	AM13
AD54	GND	GND	AM15
AD8	GND	GND	AM16
AF15	GND	GND	AM17
AF16	GND	GND	AM18
AF17	GND	GND	AM19
AF18	GND	GND	AM2
AF19	GND	GND	AM20
AF20	GND	GND	AM21
AF21	GND	GND	AM22
AF22	GND	GND	AM23
AF23	GND	GND	AM24
AF24	GND	GND	AM25
AF25	GND	GND	AM26
AF26	GND	GND	AM27
AF27	GND	GND	AM28
AF28	GND	GND	AM29
AF29	GND	GND	AM30
AF30	GND	GND	AM31
AF31	GND	GND	AM32
AF32	GND	GND	AM33
AF33	GND	GND	AM34
AF34	GND	GND	AM35
AF35	GND	GND	AM36
AF36	GND	GND	AM43
AG11	GND	GND	AM45
AG13	GND	GND	AM48
AG15	GND	GND	AM5
AG16	GND	GND	AM51

GND GND

G1
G200-100-A2
BGA2236
CHANGED

20/21 GND2

GND	B47	BP18	GND
GND	B50	BP21	GND
GND	B6	BP24	GND
GND	B9	BP27	GND
GND	BA11	BP29	GND
GND	BA13	BP32	GND
GND	BA2	BP35	GND
GND	BA43	BP38	GND
GND	BA45	BP41	GND
GND	BA48	BP44	GND
GND	BA5	BP47	GND
GND	BA51	BP50	GND
GND	BA54	BP6	GND
GND	BA8	BP9	GND
GND	BC15	C3	GND
GND	BC18	C53	GND
GND	BC21	D4	GND
GND	BC24	D52	GND
GND	BC27	E12	GND
GND	BC29	E15	GND
GND	BC32	E18	GND
GND	BC35	E21	GND
GND	BC38	E24	GND
GND	BC41	E27	GND
GND	BD11	E29	GND
GND	BD2	E32	GND
GND	BD45	E35	GND
GND	BD48	E38	GND
GND	BD5	E41	GND
GND	BD51	E44	GND
GND	BD54	E47	GND
GND	BD8	E50	GND
GND	BE12	E6	GND
GND	BE15	E9	GND
GND	BE18	F2	GND
GND	BE21	F5	GND
GND	BE24	F51	GND
GND	BE27	F54	GND
GND	BE29	H12	GND
GND	BE32	H15	GND
GND	BE35	H18	GND
GND	BE38	H21	GND
GND	BE41	H24	GND
GND	BE44	H27	GND
GND	BG2	H29	GND
GND	BG48	H32	GND
GND	BG5	H35	GND
GND	BG51	H38	GND
GND	BG54	H41	GND
GND	BG8	H44	GND
GND	BH12	H47	GND
GND	BH15	H9	GND
GND	BH18	J2	GND
GND	BH21	J48	GND
GND	BH24	J5	GND
GND	BH27	J51	GND
GND	BH29	J54	GND
GND	BH32	J8	GND
GND	BH35	L12	GND
GND	BH38	L15	GND
GND	BH41	L18	GND
GND	BH44	L21	GND
GND	BH47	L24	GND
GND	BH9	L27	GND
GND	BK2	L29	GND
GND	BK5	L32	GND
GND	BK51	L35	GND
GND	BK54	L38	GND
GND	BL12	L41	GND
GND	BL15	L44	GND
GND	BL18	M11	GND
GND	BL21	M2	GND
GND	BL24	M45	GND
GND	BL27	M48	GND
GND	BL29	M5	GND
GND	BL32	M51	GND
GND	BL35	M54	GND
GND	BL38	M8	GND
GND	BL41	N15	GND
GND	BL44	N18	GND
GND	BL47	N21	GND
GND	BL50	N24	GND
GND	BL6	N27	GND
GND	BL9	N29	GND
GND	BM4	N32	GND
GND	BM52	N35	GND
GND	BN3	N38	GND
GND	BN53	N41	GND
GND	BP12	R11	GND
GND	BP15	R13	GND

GND GND

G1
G200-100-A2
BGA2236
CHANGED

21/21 GND3

GND	R16
GND	R18
GND	R2
GND	R20
GND	R22
GND	R24
GND	R27
GND	R29
GND	R31
GND	R33
GND	R35
GND	R43
GND	R45
GND	R48
GND	R5
GND	R51
GND	R54
GND	R8
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T20
GND	T21
GND	T22
GND	T23
GND	T24
GND	T25
GND	T26
GND	T27
GND	T28
GND	T29
GND	T30
GND	T31
GND	T32
GND	T33
GND	T34
GND	T35
GND	T36
GND	V11
GND	V13
GND	V2
GND	V43
GND	V45
GND	V48
GND	V5
GND	V51
GND	V54
GND	V8
GND	Y15
GND	Y16
GND	Y17
GND	Y18
GND	Y19
GND	Y20
GND	Y21
GND	Y22
GND	Y23
GND	Y24
GND	Y25
GND	Y26
GND	Y27
GND	Y28
GND	Y29
GND	Y30
GND	Y31
GND	Y32
GND	Y33
GND	Y34
GND	Y35
GND	Y36

GND

GPU SECTION POWER

G1
G200-100-A2
BGA2236
CHANGED

14/21 NVVDD1

NVVDD	AC15	NVVDD	AJ21
NVVDD	AC16	NVVDD	AJ22
NVVDD	AC17	NVVDD	AJ23
NVVDD	AC18	NVVDD	AJ24
NVVDD	AC19	NVVDD	AJ27
NVVDD	AC20	NVVDD	AJ28
NVVDD	AC21	NVVDD	AJ29
NVVDD	AC22	NVVDD	AJ30
NVVDD	AC23	NVVDD	AJ31
NVVDD	AC24	NVVDD	AJ32
NVVDD	AC25	NVVDD	AJ34
NVVDD	AC26	NVVDD	AJ35
NVVDD	AC27	NVVDD	AJ36
NVVDD	AC28	NVVDD	AK15
NVVDD	AC29	NVVDD	AK16
NVVDD	AC30	NVVDD	AK17
NVVDD	AC31	NVVDD	AK18
NVVDD	AC32	NVVDD	AK19
NVVDD	AC33	NVVDD	AK20
NVVDD	AC34	NVVDD	AK21
NVVDD	AC35	NVVDD	AK22
NVVDD	AC36	NVVDD	AK23
NVVDD	AD15	NVVDD	AK24
NVVDD	AD16	NVVDD	AK25
NVVDD	AD17	NVVDD	AK26
NVVDD	AD18	NVVDD	AK27
NVVDD	AD19	NVVDD	AK28
NVVDD	AD20	NVVDD	AK30
NVVDD	AD21	NVVDD	AK31
NVVDD	AD22	NVVDD	AK32
NVVDD	AD23	NVVDD	AK33
NVVDD	AD24	NVVDD	AK35
NVVDD	AD25	NVVDD	AK36
NVVDD	AD26	NVVDD	AL15
NVVDD	AD27	NVVDD	AL16
NVVDD	AD28	NVVDD	AL17
NVVDD	AD29	NVVDD	AL18
NVVDD	AD30	NVVDD	AL19
NVVDD	AD31	NVVDD	AL20
NVVDD	AD32	NVVDD	AL21
NVVDD	AD33	NVVDD	AL22
NVVDD	AD34	NVVDD	AL23
NVVDD	AD35	NVVDD	AL24
NVVDD	AD36	NVVDD	AL25
NVVDD	AE15	NVVDD	AL26
NVVDD	AE16	NVVDD	AL27
NVVDD	AE17	NVVDD	AL28
NVVDD	AE18	NVVDD	AL29
NVVDD	AE19	NVVDD	AL30
NVVDD	AE20	NVVDD	AL31
NVVDD	AE21	NVVDD	AL32
NVVDD	AE22	NVVDD	AL33
NVVDD	AE23	NVVDD	AL34
NVVDD	AE24	NVVDD	AL35
NVVDD	AE27	NVVDD	AL36
NVVDD	AE28	NVVDD	AR15
NVVDD	AE29	NVVDD	AR16
NVVDD	AE30	NVVDD	AR17
NVVDD	AE31	NVVDD	AR18
NVVDD	AE32	NVVDD	AR19
NVVDD	AE33	NVVDD	AR20
NVVDD	AE34	NVVDD	AR21
NVVDD	AE35	NVVDD	AR22
NVVDD	AE36	NVVDD	AR23
NVVDD	AJ15	NVVDD	AR24
NVVDD	AJ16	NVVDD	AR25
NVVDD	AJ17	NVVDD	AR26
NVVDD	AJ18	NVVDD	AR27
NVVDD	AJ19	NVVDD	AR28
NVVDD	AJ20	NVVDD	AR29

NVVDD NVVDD

G1
G200-100-A2
BGA2236
CHANGED

15/21 NVVDD2

NVVDD	AR30	NVVDD	V17
NVVDD	AR31	NVVDD	V18
NVVDD	AR32	NVVDD	V19
NVVDD	AR33	NVVDD	V20
NVVDD	AR34	NVVDD	V21
NVVDD	AR35	NVVDD	V22
NVVDD	AR36	NVVDD	V23
NVVDD	AT16	NVVDD	V24
NVVDD	AT18	NVVDD	V25
NVVDD	AT20	NVVDD	V26
NVVDD	AT22	NVVDD	V27
NVVDD	AT24	NVVDD	V28
NVVDD	AT27	NVVDD	V29
NVVDD	AT29	NVVDD	V30
NVVDD	AT31	NVVDD	V31
NVVDD	AT33	NVVDD	V32
NVVDD	AT35	NVVDD	V33
NVVDD	BB43	NVVDD	V34
NVVDD	BC13	NVVDD	V35
NVVDD	BC14	NVVDD	V36
NVVDD	BC22	NVVDD	W15
NVVDD	BC23	NVVDD	W16
NVVDD	BC25	NVVDD	W17
NVVDD	BC26	NVVDD	W18
NVVDD	BC28	NVVDD	W19
NVVDD	BC30	NVVDD	W20
NVVDD	BC31	NVVDD	W21
NVVDD	BC33	NVVDD	W22
NVVDD	BC34	NVVDD	W23
NVVDD	BC36	NVVDD	W24
NVVDD	BC37	NVVDD	W25
NVVDD	BC39	NVVDD	W26
NVVDD	BC40	NVVDD	W27
NVVDD	BC42	NVVDD	W28
NVVDD	R15	NVVDD	W29
NVVDD	R17	NVVDD	W30
NVVDD	R19	NVVDD	W31
NVVDD	R21	NVVDD	W32
NVVDD	R23	NVVDD	W33
NVVDD	R25	NVVDD	W34
NVVDD	R26	NVVDD	W35
NVVDD	R28	NVVDD	W36
NVVDD	R30		
NVVDD	R32		
NVVDD	R34		
NVVDD	R36		
NVVDD	U15		
NVVDD	U16		
NVVDD	U17		
NVVDD	U18		
NVVDD	U19		
NVVDD	U20		
NVVDD	U21		
NVVDD	U22		
NVVDD	U23		
NVVDD	U24		
NVVDD	U25		
NVVDD	U26		
NVVDD	U27		
NVVDD	U28		
NVVDD	U29		
NVVDD	U30		
NVVDD	U31		
NVVDD	U32		
NVVDD	U33		
NVVDD	U34		
NVVDD	U35		
NVVDD	U36		
NVVDD	V15		
NVVDD	V16		

GPU SECTION MISC

G1
G200-100-A2
BGA2236
CHANGED

11/21 FBVDDQ/RFU

FBVDDQ	AB13	FBA_RFU0	BJ38 SNN_FBA_DBI0
FBVDDQ	AB43	FBA_RFU1	BG44 SNN_FBA_DBI1
FBVDDQ	AC13	FBA_RFU2	BL46 SNN_FBA_DBI2
FBVDDQ	AC43	FBA_RFU3	BG45 SNN_FBA_DBI3
FBVDDQ	AE43	FBA_RFU4	BF51 SNN_FBA_DBI4
FBVDDQ	AF13	FBA_RFU5	BE48 SNN_FBA_DBI5
FBVDDQ	AF43	FBA_RFU6	BE49 SNN_FBA_DBI6
FBVDDQ	AH13	FBA_RFU7	AY51 SNN_FBA_DBI7
FBVDDQ	AH43		
FBVDDQ	AK13	FBB_RFU0	AP51 SNN_FBB_DBI0
		FBB_RFU1	AR47 SNN_FBB_DBI1
FBVDDQ	AK43	FBB_RFU2	AM52 SNN_FBB_DBI2
FBVDDQ	AL13	FBB_RFU3	AL45 SNN_FBB_DBI3
FBVDDQ	AL43	FBB_RFU4	AJ49 SNN_FBB_DBI4
FBVDDQ	AT13	FBB_RFU5	AH45 SNN_FBB_DBI5
FBVDDQ	AT43	FBB_RFU6	AD49 SNN_FBB_DBI6
FBVDDQ	AU13	FBB_RFU7	W47 SNN_FBB_DBI7
FBVDDQ	AU43		
FBVDDQ	AY13	FBC_RFU0	V52 SNN_FBC_DBI0
FBVDDQ	L28	FBC_RFU1	V47 SNN_FBC_DBI1
FBVDDQ	N16	FBC_RFU2	V50 SNN_FBC_DBI2
		FBC_RFU3	R49 SNN_FBC_DBI3
FBVDDQ	N17	FBC_RFU4	N53 SNN_FBC_DBI4
FBVDDQ	N19	FBC_RFU5	J46 SNN_FBC_DBI5
FBVDDQ	N20	FBC_RFU6	F48 SNN_FBC_DBI6
FBVDDQ	N22	FBC_RFU7	D50 SNN_FBC_DBI7
FBVDDQ	N23		
FBVDDQ	N25	FBD_RFU0	G45 SNN_FBD_DBI0
FBVDDQ	N26	FBD_RFU1	J41 SNN_FBD_DBI1
FBVDDQ	N28	FBD_RFU2	F42 SNN_FBD_DBI2
FBVDDQ	N30	FBD_RFU3	K39 SNN_FBD_DBI3
FBVDDQ	N31	FBD_RFU4	G36 SNN_FBD_DBI4
		FBD_RFU5	G32 SNN_FBD_DBI5
FBVDDQ	N33	FBD_RFU6	E31 SNN_FBD_DBI6
FBVDDQ	N34	FBD_RFU7	F27 SNN_FBD_DBI7
FBVDDQ	N36		
FBVDDQ	N37	FBE_RFU0	H28 SNN_FBE_DBI0
FBVDDQ	N39	FBE_RFU1	K24 SNN_FBE_DBI1
FBVDDQ	N40	FBE_RFU2	E23 SNN_FBE_DBI2
FBVDDQ	T13	FBE_RFU3	J22 SNN_FBE_DBI3
FBVDDQ	T43	FBE_RFU4	F21 SNN_FBE_DBI4
FBVDDQ	U13	FBE_RFU5	J16 SNN_FBE_DBI5
FBVDDQ	U43	FBE_RFU6	E13 SNN_FBE_DBI6
		FBE_RFU7	E10 SNN_FBE_DBI7
FBVDDQ	W13		
FBVDDQ	W43	FBF_RFU0	J13 SNN_FBF_DBI0
FBVDDQ	Y13	FBF_RFU1	P9 SNN_FBF_DBI1
FBVDDQ	Y43	FBF_RFU2	K9 SNN_FBF_DBI2
		FBF_RFU3	E8 SNN_FBF_DBI3
		FBF_RFU4	L6 SNN_FBF_DBI4
		FBF_RFU5	U5 SNN_FBF_DBI5
		FBF_RFU6	U9 SNN_FBF_DBI6
		FBF_RFU7	W5 SNN_FBF_DBI7
		FBG_RFU0	AB9 SNN_FBG_DBI0
		FBG_RFU1	AG6 SNN_FBG_DBI1
		FBG_RFU2	AB3 SNN_FBG_DBI2
		FBG_RFU3	AJ10 SNN_FBG_DBI3
		FBG_RFU4	AH5 SNN_FBG_DBI4
		FBG_RFU5	AN10 SNN_FBG_DBI5
		FBG_RFU6	AR6 SNN_FBG_DBI6
		FBG_RFU7	AR10 SNN_FBG_DBI7
		FBH_RFU0	AU5 SNN_FBH_DBI0
		FBH_RFU1	BB11 SNN_FBH_DBI1
		FBH_RFU2	BF5 SNN_FBH_DBI2
		FBH_RFU3	BE7 SNN_FBH_DBI3
		FBH_RFU4	BJ8 SNN_FBH_DBI4
		FBH_RFU5	BK6 SNN_FBH_DBI5
		FBH_RFU6	BL7 SNN_FBH_DBI6
		FBH_RFU7	BP8 SNN_FBH_DBI7

G1
G200-100-A2
BGA2236
CHANGED

18/21 SPARE/MISC

SPARE	BB50	SNN_SPARE_01	NC
SPARE	BD46	SNN_SPARE_02	NC
SPARE	BE13	SNN_SPARE_03	NC
SPARE	BE14	SNN_SPARE_04	NC
SPARE	BE17	SNN_SPARE_05	NC
SPARE	BE22	SNN_SPARE_06	NC
SPARE	BE25	SNN_SPARE_07	NC
SPARE	BE28	SNN_SPARE_08	NC
SPARE	BE31	SNN_SPARE_09	NC
SPARE	BE34	SNN_SPARE_10	NC
SPARE	BF15	SNN_SPARE_11	NC
SPARE	BF17	SNN_SPARE_12	NC
SPARE	BF18	SNN_SPARE_13	NC
SPARE	BF20	SNN_SPARE_14	NC
SPARE	BF21	SNN_SPARE_15	NC
SPARE	BF23	SNN_SPARE_16	NC
SPARE	BF24	SNN_SPARE_17	NC
SPARE	BF26	SNN_SPARE_18	NC
SPARE	BF27	SNN_SPARE_19	NC
SPARE	BF29	SNN_SPARE_20	NC
SPARE	BF30	SNN_SPARE_21	NC
SPARE	BF32	SNN_SPARE_22	NC
SPARE	BF36	SNN_SPARE_23	NC
SPARE	BF38	SNN_SPARE_24	NC
SPARE	BF9	SNN_SPARE_25	NC
SPARE	BG10	SNN_SPARE_26	NC
SPARE	BG17	SNN_SPARE_27	NC
SPARE	BG18	SNN_SPARE_28	NC
SPARE	BG19	SNN_SPARE_29	NC
SPARE	BG21	SNN_SPARE_30	NC
SPARE	BG22	SNN_SPARE_31	NC
SPARE	BG24	SNN_SPARE_32	NC
SPARE	BG25	SNN_SPARE_33	NC
SPARE	BG27	SNN_SPARE_34	NC
SPARE	BG28	SNN_SPARE_35	NC
SPARE	BG30	SNN_SPARE_36	NC
SPARE	BG31	SNN_SPARE_37	NC
SPARE	BG33	SNN_SPARE_38	NC
SPARE	BG34	SNN_SPARE_39	NC
SPARE	BG36	SNN_SPARE_40	NC
SPARE	BG37	SNN_SPARE_41	
SPARE	BG38	SNN_SPARE_42	
SPARE	BG39	SNN_SPARE_43	
SPARE	BG40	SNN_SPARE_44	
SPARE	BG43	SNN_SPARE_45	
SPARE	BG9	SNN_SPARE_46	
SPARE	BH10	SNN_SPARE_47	
SPARE	BH16	SNN_SPARE_48	
SPARE	BH19	SNN_SPARE_49	
SPARE	BH20	SNN_SPARE_50	
SPARE	BH22	SNN_SPARE_51	
SPARE	BH25	SNN_SPARE_52	
SPARE	BH28	SNN_SPARE_53	
SPARE	BH31	SNN_SPARE_54	
SPARE	BH34	SNN_SPARE_55	
SPARE	BH36	SNN_SPARE_56	
SPARE	BH37	SNN_SPARE_57	
SPARE	BH40	SNN_SPARE_58	
SPARE	BH43	SNN_SPARE_59	
SPARE	BH8	SNN_SPARE_60	
SPARE	BJ18	SNN_SPARE_61	
SPARE	BJ20	SNN_SPARE_62	
SPARE	BJ30	SNN_SPARE_63	
SPARE	BJ35	SNN_SPARE_64	
SPARE	BJ36	SNN_SPARE_65	
SPARE	BJ9	SNN_SPARE_66	
SPARE	BK36	SNN_SPARE_67	
SPARE	BL36	SNN_SPARE_68	
SPARE	BL45	SNN_SPARE_69	
SPARE	BN22	SNN_SPARE_70	
SPARE	BN26	SNN_SPARE_71	
SPARE	BN29	SNN_SPARE_72	
SPARE	L13	SNN_SPARE_73	
SPARE	L14	SNN_SPARE_74	

TESTMODE BG42 GPU_TESTMODE

RFU (GND) BP26

R728
10K
5%
0402
COMMON

GND GND

NVIOx SECTION GND

U5
NV102-A2
BGA533
CHANGED

15/17 _GND

GND	AA2	GND	R2
GND	AB26	GND	T26
GND	AC11	GND	U23
GND	AC14	GND	U5
GND	AC17	GND	V2
GND	AC20	GND	W11
GND	AC23	GND	W12
GND	AC5	GND	W14
GND	AC8	GND	W16
GND	AD2	GND	W17
GND	AE26	GND	W19
GND	AF12	GND	W26
GND	AF15	GND	W9
GND	AF18	GND	Y23
GND	AF21	GND	Y5
GND	AF24	GND	M13
GND	AF3	GND	M15
GND	AF6	GND	M16
GND	AF9	GND	N11
GND	B10	GND	N12
GND	B13	GND	N13
GND	B16	GND	N14
GND	B19	GND	N15
GND	B22	GND	P11
GND	B25	GND	P12
GND	B4	GND	P13
GND	B7	GND	P14
GND	C2	GND	P15
GND	D12	GND	Y23
GND	D26	GND	P16
GND	D8	GND	P17
GND	E11	GND	R12
GND	E14	GND	R13
GND	E17	GND	R14
GND	E20	GND	R15
GND	E23	GND	R16
GND	E5	GND	R17
GND	E8	GND	T12
GND	E9	GND	T13
GND	F10	GND	T15
GND	F2		
GND	G26		
GND	H23		
GND	H5		
GND	J11		
GND	J12		
GND	J14		
GND	J16		
GND	J17		
GND	J19		
GND	J2		
GND	J9		
GND	K26		
GND	L23		
GND	L5		
GND	M2		
GND	N26		
GND	P19		
GND	P23		
GND	P5		

GND GND

U5
NV102-A2
BGA533
CHANGED

16/17 NC

SNN_NVIO_NC_01	A10	NC	E7 SNN_NVIO_NC_31
SNN_NVIO_NC_02	A12	NC	F11 SNN_NVIO_NC_32
SNN_NVIO_NC_03	AB21	NC	F12 SNN_NVIO_NC_33
SNN_NVIO_NC_04	AB8	NC	F13 SNN_NVIO_NC_34
SNN_NVIO_NC_05	AB9	NC	F14 SNN_NVIO_NC_35
SNN_NVIO_NC_06	AC21	NC	F21 SNN_NVIO_NC_36
SNN_NVIO_NC_07	AC22	NC	F22 SNN_NVIO_NC_37
SNN_NVIO_NC_08	AC24	NC	F7 SNN_NVIO_NC_38
SNN_NVIO_NC_09	AC7	NC	F8 SNN_NVIO_NC_39
SNN_NVIO_NC_10	AD27	NC	F9 SNN_NVIO_NC_40
SNN_NVIO_NC_11	AF25	NC	G23 SNN_NVIO_NC_41
SNN_NVIO_NC_12	B11	NC	H22 SNN_NVIO_NC_42
SNN_NVIO_NC_13	B12	NC	J23 SNN_NVIO_NC_43
SNN_NVIO_NC_14	B14	NC	K23 SNN_NVIO_NC_44
SNN_NVIO_NC_15	C10	NC	K24 SNN_NVIO_NC_45
SNN_NVIO_NC_16	C12	NC	L22 SNN_NVIO_NC_46
SNN_NVIO_NC_17	C13	NC	N5 SNN_NVIO_NC_47
SNN_NVIO_NC_18	C18	NC	N6 SNN_NVIO_NC_48
SNN_NVIO_NC_19	C4	NC	N9 SNN_NVIO_NC_49
SNN_NVIO_NC_20	C9	NC	P22 SNN_NVIO_NC_50
SNN_NVIO_NC_21	D10	NC	R3 SNN_NVIO_NC_51
SNN_NVIO_NC_22	D11	NC	R6 SNN_NVIO_NC_52
SNN_NVIO_NC_23	D13	NC	T3 SNN_NVIO_NC_53
SNN_NVIO_NC_24	D14	NC	T6 SNN_NVIO_NC_54
SNN_NVIO_NC_25	D7	NC	U22 SNN_NVIO_NC_55
SNN_NVIO_NC_26	D9	NC	U24 SNN_NVIO_NC_56
SNN_NVIO_NC_27	E10	NC	U4 SNN_NVIO_NC_57
SNN_NVIO_NC_28	E12	NC	V6 SNN_NVIO_NC_58
SNN_NVIO_NC_29	E13	NC	W6 SNN_NVIO_NC_59
SNN_NVIO_NC_30	E21	NC	Y22 SNN_NVIO_NC_60
		NC	Y24 SNN_NVIO_NC_61

GND GND 0V

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power and GND (GPU and NVIOx)

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	31 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Power: Hybrid Power

Per Datasheet:

Vf = 400mV at 10mA
Vf = 500mV at 30mA
* expected current < 2mA

3V3_AUX 3V3 D8 BAT54C 25V 200MA SOT23 NO STUFF R21 0 5% 0402 NO STUFF C20 1UF 6.3V 10% X5R 0402 NO STUFF C18 .1UF 6.3V 10% X7R 0402 NO STUFF HYBRID_3V3 3.0V 0.01A 10MIL GND

U6 HYBRID_PIC16F690_P XSOP20 NO STUFF

PIC16F690

VDD	1		
PEX_REF_CLK_ENABLE	2	I2CA_SCL	15
		I2CA_SDA	14
		I2CB_SCL	8
		I2CB_SDA	9
I2CC_SCL	3		
I2CC_SDA	17		
SMB_SCL	11	HOTPLUG_DETECT_C	12
SMB_SDA	13	HOTPLUG_DETECT_D	10
		HOTPLUG_DETECT_E	19
		HOTPLUG_DETECT_F	18
PCI_E_RESET*	7	GPU_RESET*	6
VPP	4	POWER_ENABLE	16
GND	20	FAN_ENABLE	5

HYBRID_3V3 R23 68K 5% 0402 NO STUFF — 3.4A< OUT — PEX_REFCLK_EN

Weak pull-ups needed for I2CS:
* if SMBus is isolated from the GPU
* if MB does not support SMBus
* if MB does not support 3V3AUX

HYBRID_3V3 R37 68K 5% 0402 NO STUFF; R35 68K 5% 0402 NO STUFF

29.4B< 28.2F> 25.3B< OUT I2C3_SCL_R
29.4B<> 28.2F<> 25.3B<> BI I2C3_SDA_R

32.5C< 29.4B< 3.2C> OUT I2CS_SCL_R
32.5C<> 29.4B<> 3.2C<> BI I2CS_SDA_R

HYBRID_3V3 R24 68K 5% 0402 NO STUFF — HYBRID_PRG_TP

3.2D> IN PEX_RST*

PEX_RST* R26 0 5% 0402 COMMON GPU_RST*

Stuff only to bypass the micro-controller

HYBRID_3V3 R876 68K 5% 0402 NO STUFF; R891 68K 5% 0402 NO STUFF; R922 68K 5% 0402 NO STUFF; R912 68K 5% 0402 NO STUFF

I2C1_SCL_UC — I2C1_SDA_UC — R885 10K 0402 5% NO STUFF GND

Stuff 10K pull-down for DP skus

I2C2_SCL_UC — I2C2_SDA_UC

HYBRID_3V3 R33 1.1M 0402 5% NO STUFF — HYBRID_HPD_E
HYBRID_3V3 R34 1.1M 0402 5% NO STUFF — HYBRID_HPD_F

HYBRID_HPD_DVICD_DP — HYBRID_HPD_DVIAB

GPU_RST* — R25 10K 0402 5% NO STUFF GND — 33.3E< 28.3B< 29.3C< OUT

3V3 R857 10K 5% 0402 COMMON

HYBRID_PWR_EN

FAN_PWM — 29.5H> OUT

40.3H> IN INPUT_PEX_PRSNT — R856 0 0402 5% COMMON
33.1G> IN THERM_SHDN_D* — R858 0 0402 5% COMMON

20.1D< 21.1D< 36.2A< 40.2E< OUT

I2C1_SCL_R — 20.1F> OUT
I2C1_SDA_R — 20.1F<> BI

Q531 BSS138 SOT23_1G1D1S NO STUFF; Q535 BSS138 SOT23_1G1D1S NO STUFF

I2C2_SCL_R — 21.1F> OUT
I2C2_SDA_R — 21.1F<> BI

Q537 BSS138 SOT23_1G1D1S NO STUFF; Q538 BSS138 SOT23_1G1D1S NO STUFF

Inverts HPD signal polarity

HYBRID_3V3 R36 68K 5% 0402 NO STUFF — GPIO1_DVICD_DP_HPD_R2_G

Q530 BSS138 SOT23_1G1D1S NO STUFF — R886 1K 0402 5% NO STUFF — GPIO1_DVICD_DP_HPD_R2 — 25.1H> IN
C1251 .1UF 16V 10% X7R 0402 NO STUFF — GND

Inverts HPD signal polarity

HYBRID_3V3 R22 68K 5% 0402 NO STUFF — GPIO0_DVIAB_HPD_R_G

Q540 BSS138 SOT23_1G1D1S NO STUFF — R4 1K 0402 5% NO STUFF — GPIO0_DVIAB_HPD_R — 23.4F> IN
C10 .1UF 16V 10% X7R 0402 NO STUFF — GND

Vcc section of I2C bus switch

U2 XSOP16_SECT IDTQS3VH126 NO STUFF

SNN_QS_NC1	1	NC	
SNN_QS_NC2	9	NC	
		VCC	16
		GND	8

HYBRID_3V3 — C16 .1UF 6.3V 10% X7R 0402 NO STUFF — GND

See DAC pages for switch sections

I2CS Isolation for Hybrid Power and Level Shifting(3.3V to 1.15V)

Isolates SMBus to the GPU when in Hybrid mode
GT200 I2CS lanes are 1.2V tolerant signals

Key property of AO3416 is low Vgs threshold (0.6V nom)

1V15 — Note: 1V15 rail is disabled while in Hybrid Mode

R43 10K 5% 0402 NO STUFF — GND

From Edge Connector — 32.2B> IN I2CS_SCL_R — Q7 AO3416 SOT23_1G1D1S NO STUFF — I2CS_SCL_Q — R39 33 0402 5% NO STUFF — R44 47K 5% 0402 COMMON — I2CS_SCL — To the GPU — OUT 3.2D<

From Edge Connector — 32.3B<> 29.4B<> 3.2C<> BI I2CS_SDA_R — Q6 AO3416 SOT23_1G1D1S NO STUFF — I2CS_SDA_Q — R42 33 0402 5% NO STUFF — R48 47K 5% 0402 COMMON — I2CS_SDA — To the GPU — BI 3.2D<>

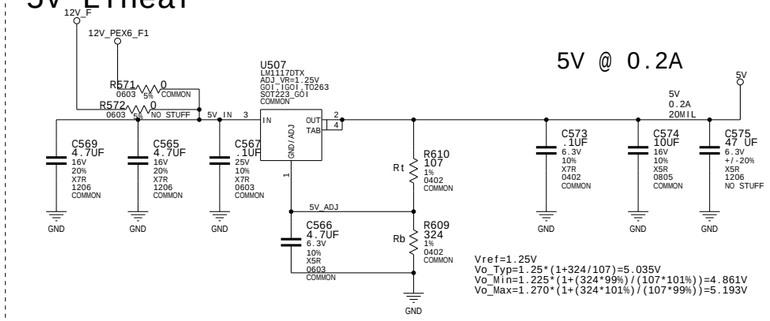
ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power: Hybrid Power

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

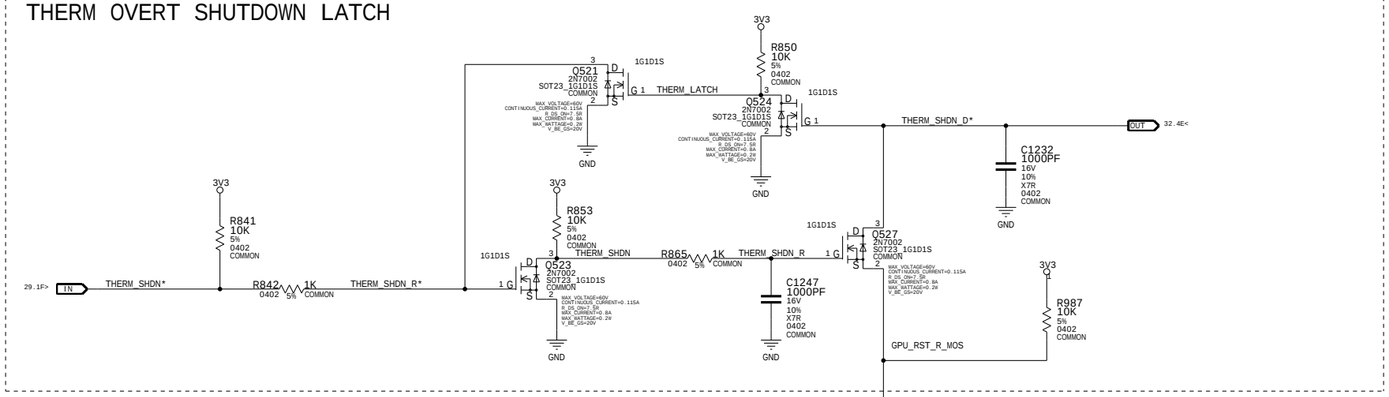
NV_PN	600-10654-0051-300 D		
ID	design	PAGE	32 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Power Supply: 5V LDO / 3V3_DP / THERM SHUTDOWN LATCH / IFP_IOVDD /PEX_PLVDD

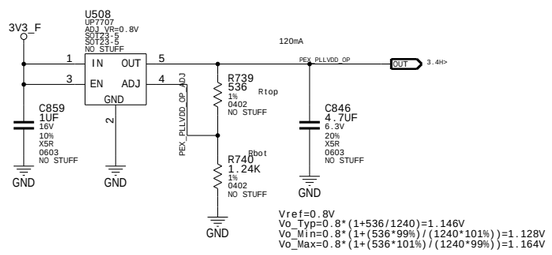
5V_Linear



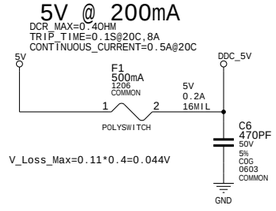
THERM OVERT SHUTDOWN LATCH



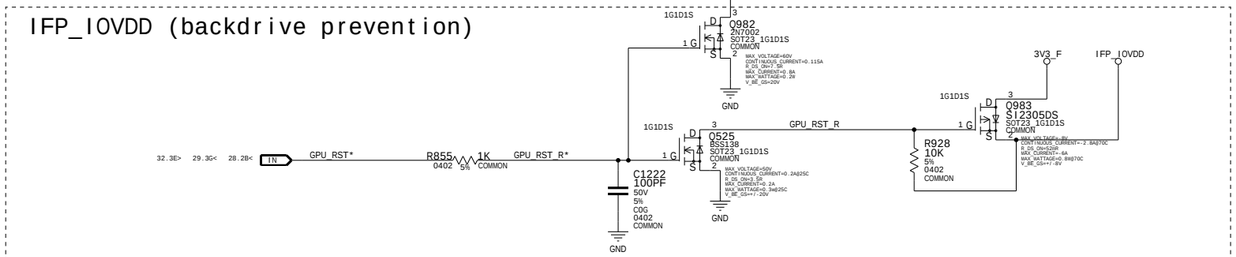
PEX PLLVDD optional Supply



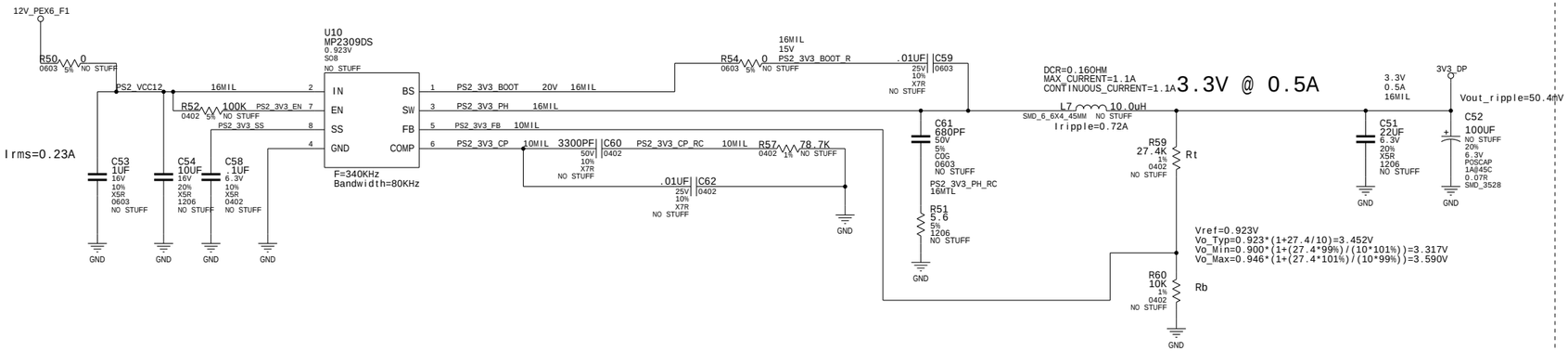
DDC_5V



IFP_IOVDD (backdrive prevention)



3V3_DP SWITCHER
(Only required for DisplayPort SKU)



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power Supply: 5V + 5V Alt / SHDN LATCH / IFP_IOVDD

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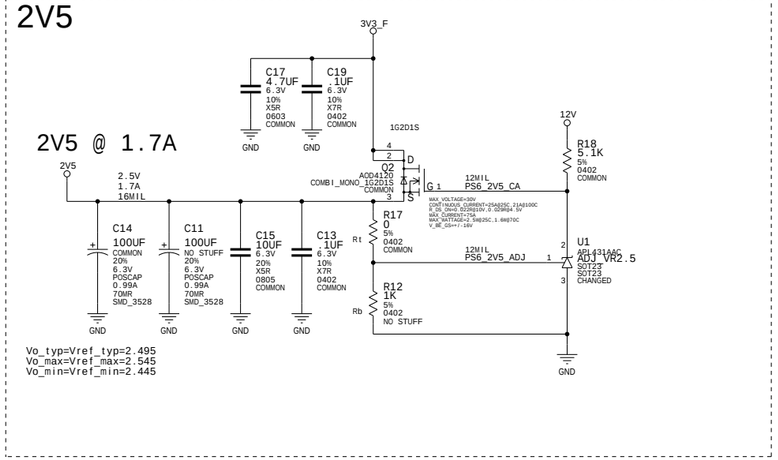
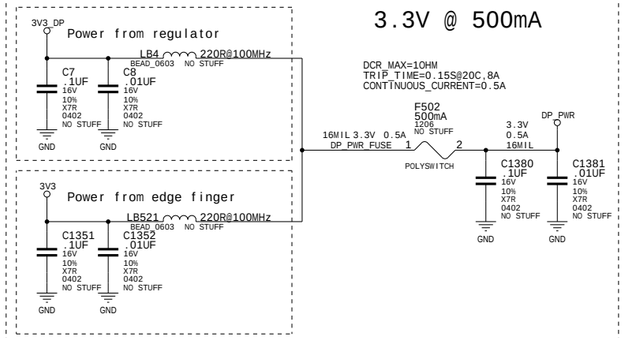
NV_PN	600-10654-0051-300 D		
ID	design	PAGE	33 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Power Supply: 2V5, DP_PWR, 8V5 1V15 (PEX_VDD, GV_VDD)

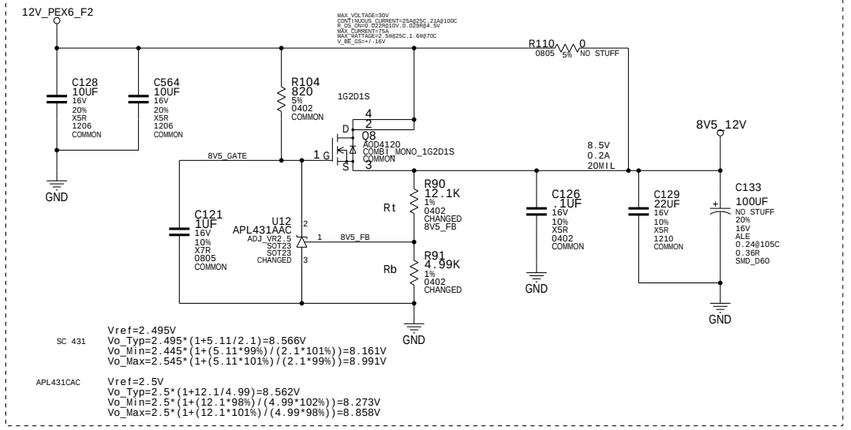
2V5



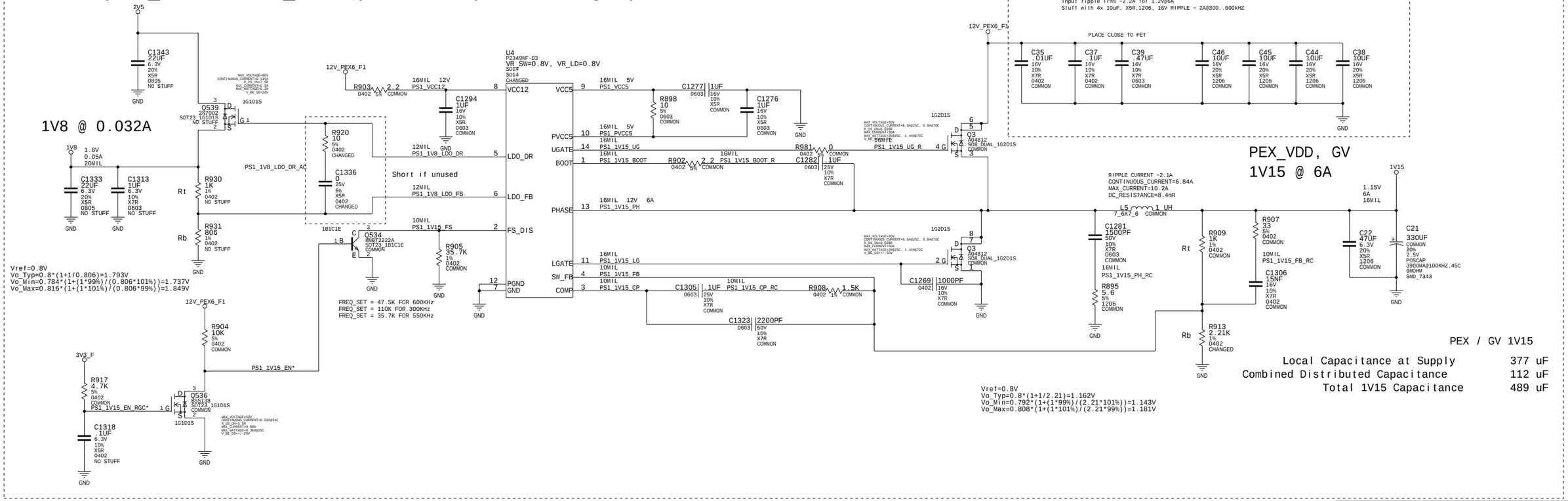
DP Dongle Supply



8V5



1V15 (PEX_VDD AND GV_VDD/Q) and 1V8(For Analogix)



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power Supply: 2V5, DP_PWR, 1V15 (PEX_VDD, GV_VDD)

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NV_PN	600-10654-0051-300 D		
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Power Supply: Combined FBVDD/Q

FBVDDQ Cin and PEX Cin filtering

* footprint supports multiple values and case sizes from 7473 Poscaps, 82uF low-profile SMD_D80, up to 180uF SMD_D80
* options providing for higher ripple current caps

Input ripple Irms ~7A@15A/phase (2 shared phases)
8x 10uF, X5R, 1206, 16V. I_RIPPLE ~2A@300..600kHZ

12V_PEX6_F1

Place 2 MLCCs exactly back-to-back to eliminate audible noise.

C521 10UF 16V 20% X5R 1206 COMMON
C523 10UF 16V 20% X5R 1206 COMMON
C160 10UF 16V 20% X5R 1206 COMMON
C505 10UF 16V 20% X5R 1206 COMMON
C149 10UF 16V 20% X5R 1206 COMMON
C522 10UF 16V 20% X5R 1206 COMMON
C504 10UF 16V 20% X5R 1206 NO STUFF
C506 10UF 16V 20% X5R 1206 NO STUFF
GND

12V_PEX6_F1
C146 180UF COMMON 20% 16V NPCAP 4.36A@105C 0.016R COMBI_7343_D80
C158 180UF NO STUFF 20% 16V NPCAP 4.36A@105C 0.016R COMBI_7343_D80
GND

U501
RT8805CQVA
VR=0.8V
QFN24
COMMON
2 PHASE PWM

12V 8MIL PS3_FBVDDQ_VCC12
C508 1UF 16V 10% X5R 0603 COMMON
GND
R523 2.2 0603 5% COMMON
12V_PEX6_F1

C515 3.3PF 10MIL 0402 50V NO STUFF +/-0.25PF C0G
C513 .022UF 0402 16V 10% X7R COMMON
R539 24.3K 0402 1% COMMON
PS3_FBVDDQ_CP_RC 10MIL
GND

PS3_FBVDDQ_CP
PS3_FBVDDQ_FB
28.3F< OUT GPIO12_POWERALERT* R548 0 0402 5% COMMON PS3_FBVDDQ_PGOOD
R511 33K 0402 5% COMMON PS3_FBVDDQ_FS
PS3_FBVDDQ_SS
C510 .1UF 0402 16V 10% X5R COMMON SNN_FBVDDQ_PI
GND

VCC12 21, 22
UGATE1 2 — PS3_FBVDDQ_UG1 — 16MIL
BOOT1 3 — PS3_FBVDDQ_BOOT1 — 16MIL
PHASE1 1 — PS3_FBVDDQ_PH1 — 16MIL
LGATE1 23 — PS3_FBVDDQ_LG1 — 16MIL
UGATE2 18 — PS3_FBVDDQ_UG2 — 16MIL
BOOT2 17 — PS3_FBVDDQ_BOOT2 — 16MIL
PHASE2 19 — PS3_FBVDDQ_PH2 — 16MIL
LGATE2 20 — PS3_FBVDDQ_LG2 — 16MIL
COMP 13
FB 14
PGOOD 16
RT 7
SS 12
PI 15
AGND 4
GND(PAD) 25
GND 11
IMAX 5 — PS3_FBVDDQ_IDES
R509 25.5K 1% 0402 COMMON
GND

SNN_FBVDDQ_NC1 24
SNN_FBVDDQ_NC2 6
SNN_FBVDDQ_NC3 8
SNN_FBVDDQ_NC4 9
SNN_FBVDDQ_NC5 10

FS=300KHZ

12V_PEX6_F1
R535 10K 5% 0402 COMMON
PS5_NVVDD_PGOOD*
1G1D1S Q507 BSS138 SOT23 1G1D1S COMMON
GND

1G1D1S Q506 BSS138 SOT23 1G1D1S COMMON
36.1G> IN PS5_NVVDD_PGOOD
GND

MAX_VOLTAGE=50V CONTINUOUS_CURRENT=0.22A@31C R_ON_ON=3.5R MAX_CURRENT=0.88A MAX_WATTAGE=0.36W@25C V_BE_GS=+/-20V

R508 2.2 0402 5% COMMON
16MIL PS3_FBVDDQ_UG1_R
LFPAK Q27 BSC119N03S LFPAK COMMON
MAX_VOLTAGE=30V CONTINUOUS_CURRENT=30A R_ON_ON=0.0028R-.5V MAX_CURRENT=120A MAX_WATTAGE=2.8W V_BE_GS=+/-20V

C502 .1UF 0603 25V 10% X7R COMMON
R510 0 0603 5% COMMON 16MIL PS3_FBVDDQ_LG1_G
LFPAK Q29 BSC059N03S LFPAK COMMON
MAX_VOLTAGE=30V CONTINUOUS_CURRENT=50A R_ON_ON=0.5mR MAX_CURRENT=200A MAX_WATTAGE=2.8W V_BE_GS=+/-20V
R506 0 0402 5% NO STUFF PS3_FBVDDQ_LG1_D 10MIL
D502 BAV99 SOT23 100V 100MA NO STUFF
R503 680PF 10% 0402 CHANGED
GND

C159 .47UF 0603 16V 10% X5R COMMON
12V_PEX6_F1
LFPAK Q24 BSC119N03S LFPAK COMMON
MAX_VOLTAGE=30V CONTINUOUS_CURRENT=30A R_ON_ON=0.0028R-.5V MAX_CURRENT=120A MAX_WATTAGE=2.8W V_BE_GS=+/-20V
R547 2.2 0402 5% COMMON 16MIL PS3_FBVDDQ_UG2_R
C518 .1UF 0603 25V 10% X7R COMMON
LFPAK Q22 BSC059N03S LFPAK COMMON
MAX_VOLTAGE=30V CONTINUOUS_CURRENT=50A R_ON_ON=0.5mR MAX_CURRENT=200A MAX_WATTAGE=2.8W V_BE_GS=+/-20V
R538 0 0603 5% COMMON 16MIL PS3_FBVDDQ_LG2_G
R531 0 0402 5% NO STUFF PS3_FBVDDQ_LG2_D 10MIL
D503 BAV99 SOT23 100V 100MA NO STUFF
R569 680PF 10% 0402 CHANGED
GND

DCR=2.9mOHM MAX_CURRENT=26A CONTINUOUS_CURRET=20A
12V
L16 1.0UH SMD_420X400 COMMON
D23 B340A SMA 40V 3A COMMON
C164 680PF 50V 5% C0G 0603 COMMON
PS3_FBVDDQ_PH1_RC 10MIL
R142 1.5 5% 1206 COMMON
GND

DCR=2.9mOHM MAX_CURRENT=26A CONTINUOUS_CURRET=20A
12V
L14 1.0UH SMD_420X400 COMMON
D16 B340A SMA 40V 3A COMMON
C144 680PF 50V 5% C0G 0603 COMMON
PS3_FBVDDQ_PH2_RC 10MIL
R114 1.5 5% 1206 COMMON
GND

optional type3 compensation

FBVDDQ = 1.9-2.0V @ 31A

V_ripple:28mV — 16MIL — 2.0V — 31A — FBVDDQ

C155 10UF 6.3V X5R 0805 COMMON
C161 10UF 6.3V 20% X5R 0805 COMMON
C153 10UF 6.3V 20% X5R 0805 COMMON
C156 470UF 6.3V 20% X5R 1206 COMMON
C154 470UF 6.3V 20% X5R 1206 COMMON
C148 470UF 6.3V 20% X5R 1206 COMMON
C145 220UF COMMON +/-20% 6.3V POSCAP 2.4A 0.025R SMD_7343
C162 220UF COMMON +/-20% 6.3V POSCAP 2.4A 0.025R SMD_7343
GND

FBVDD/Q	
Local Capacitance at Supply	630 uF
Combined Distributed Capacitance	490 uF
Total FBVDD/Q Capacitance	1120 uF

local sense feedback if GPU feedback is not there.
470R results in max. 2.25V

R560 470 0402 5% COMMON PS3_FBVDDQ_VSEN
R561 0 0402 5% COMMON FBVDDQ_SENSE IN 39.3B>
R552 33.2 0402 1% COMMON
PS3_FBVDDQ_FB_T3 Rt
R549 1.37K 1% 0402 COMMON
C517 .01UF 0402 25V 10% X7R COMMON
PS3_FBVDDQ_FB
Rb
R563 1K 1% 0402 NO STUFF
GND
Rb
R562 1K 1% 0402 CHANGED
FBVDDQ_SENSE_GND IN 39.3B>

Stuff for either:
1. Remote differential GND sense
2. Local GND sense

GPIO Controlled FBVDDQ Voltage Margining (OPTION)

Voltage Margining can be controlled via a divider across the Rbot resistor

NOTE - for this type of margining, the default must be with the FET ON, then to decrease the Vout, switch the FET OFF
IF USED - this requires the GPIO to be ON for the default mode

Vout = Vref*(Rtop*Rbot)/Rbot

EX: If desired Vnomimal = 2.0V, Vmargin = 1.9V
FET ON, Rbot = 1K*10K/(1K+10K), FBVDDQ = 2.0V
FET OFF, Rbot = 1K, FBVDDQ = 1.9V

3V3_F
R541 10K 5% 0402 NO STUFF
TP501
28.3F< IN GPIO10_FB_ADJ0
R540 0 0402 5% NO STUFF
PS3_FB_ADJ0_Q
C514 1000PF 16V 10% X5R 0402 NO STUFF
GND
R550 10K 1% 0402 NO STUFF
1G1D1S Q511 BSS138 SOT23 1G1D1S NO STUFF
PS3_FB_ADJ0_PD
GND

Vo_Typ=0.8*(1+1.37/1.10)=1.796V
Vo_Min=0.792*(1+(1.37*99%)/(1.10*101%))=1.759V
Vo_Max=0.808*(1+(1.37*101%)/(1.10*99%))=1.835V

Vo_Typ=0.8*(1+1.37/1.00)=1.896V
Vo_Min=0.792*(1+(1.37*99%)/(1.00*101%))=1.856V
Vo_Max=0.808*(1+(1.37*101%)/(1.00*99%))=1.937V

Vo_Typ=0.8*(1+1.37/0.909)=2.006V
Vo_Min=0.792*(1+(1.37*99%)/(0.909*101%))=1.962V
Vo_Max=0.808*(1+(1.37*101%)/(0.909*99%))=2.050V

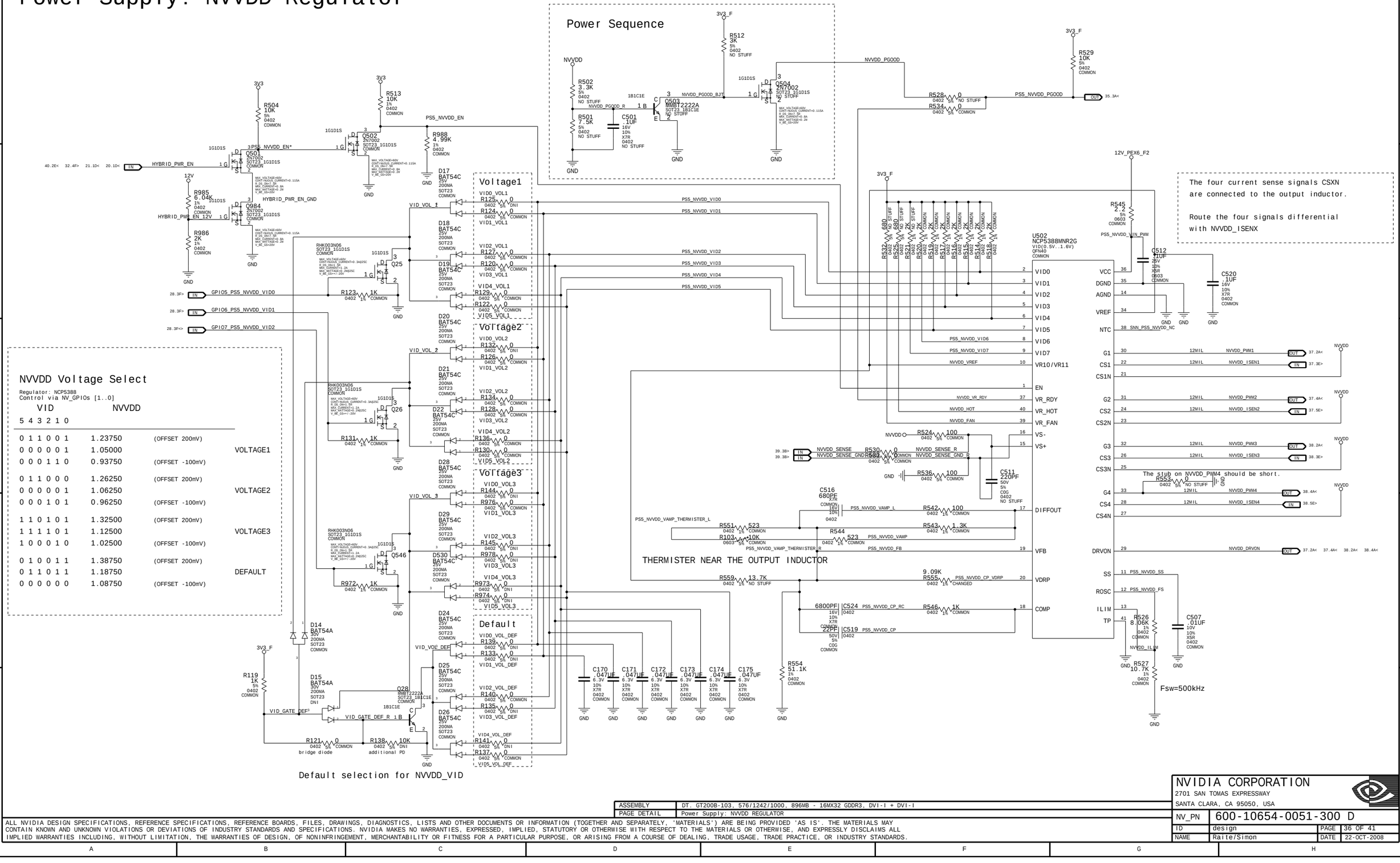
Vo_Typ=0.8*(1+1.37/0.845)=2.097V
Vo_Min=0.792*(1+(1.37*99%)/(0.845*101%))=2.144V
Vo_Max=0.808*(1+(1.37*101%)/(0.845*99%))=2.051V

ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power Supply: Combined FBVDD/Q

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	35 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Power Supply: NVVDD Regulator



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power Supply: NVVDD REGULATOR

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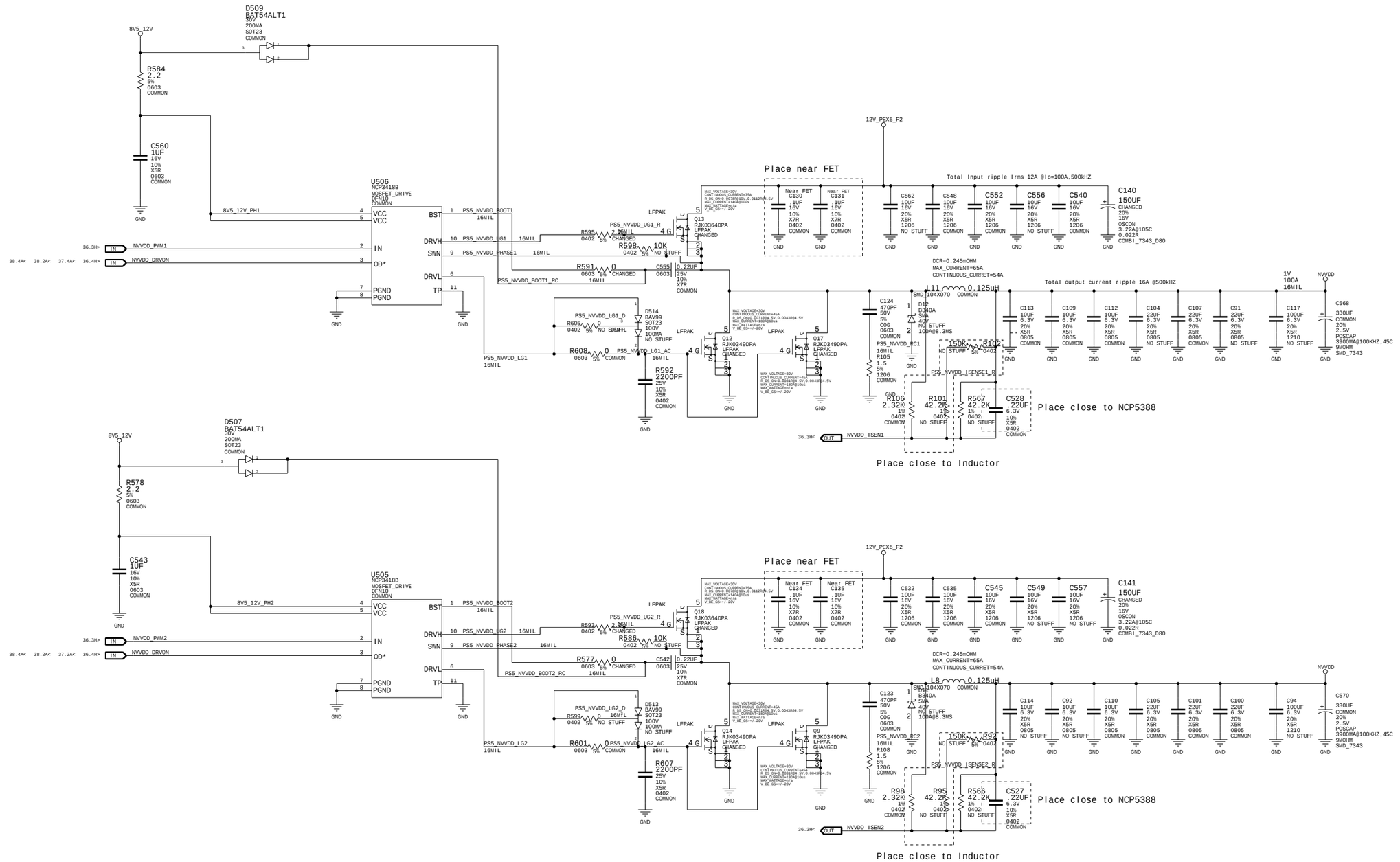
NV_PN	600-10654-0051-300 D		
ID	design	PAGE	36 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Power Supply: NVVDD Phase 1,2 powered from external PEX 6PIN



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power Supply: NVVDD Phase 1-2 of 4

NVIDIA CORPORATION
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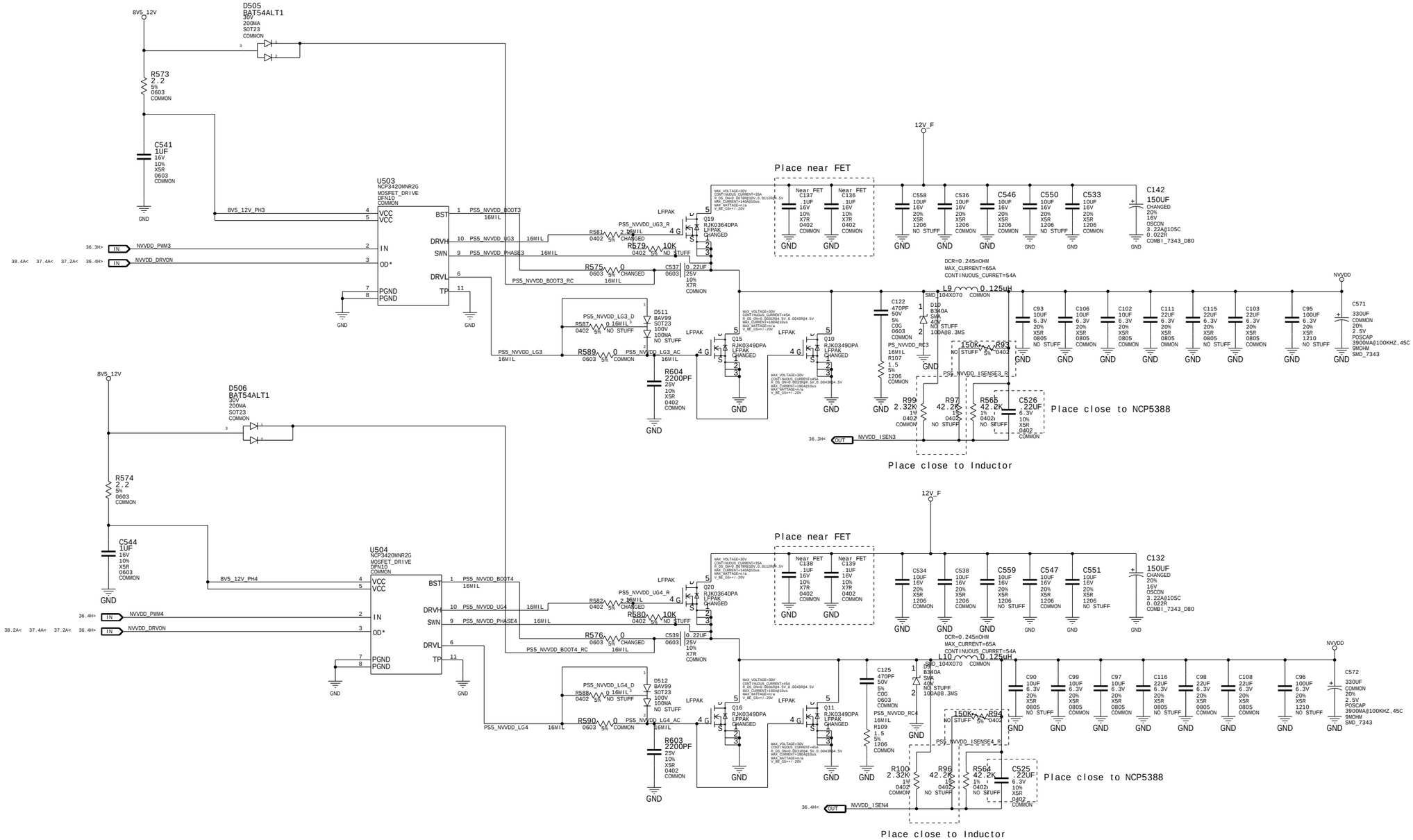
NV_PN	600-10654-0051-300 D		
ID	design	PAGE	37 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Power Supply: NVVDD Phase 3,4 powered from internal PEX edge connector



ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power Supply: NVVDD Phase 3-4 of 4

NVIDIA CORPORATION
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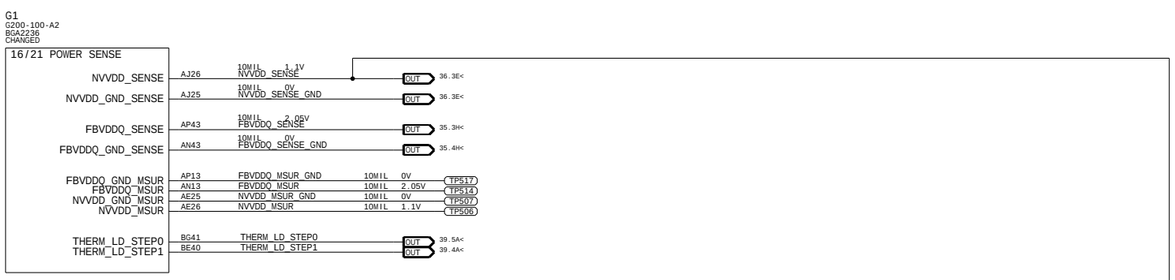
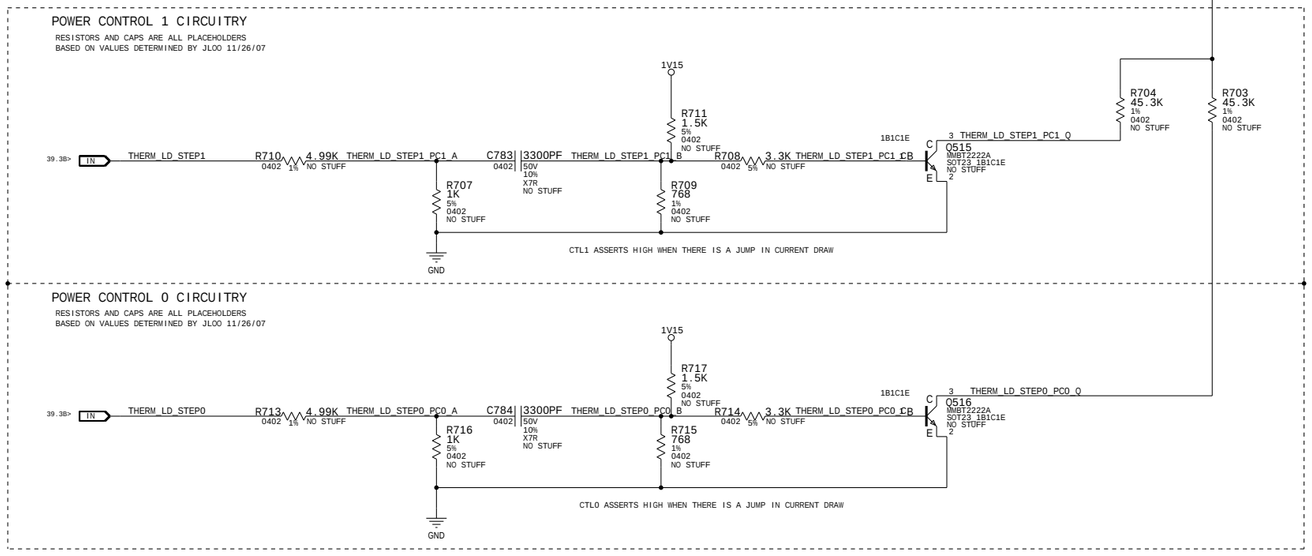
NV_PN	600-10654-0051-300 D		
ID	design	PAGE	38 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008

Power Supply: NVVDD power control

NVVDD & FBVDDQ SENSE/MSUR





ASSEMBLY	DT. GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	NVVDD & FBVDDQ SENSE/MSUR

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NV_PN	600-10654-0051-300 D		
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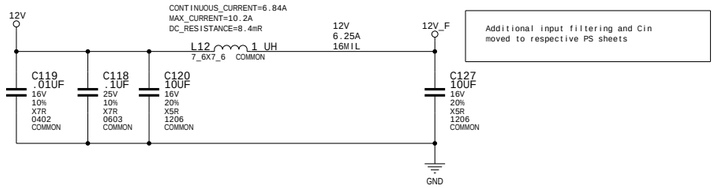
NAME	Raite/Simon	DATE	22-OCT-2008

Power: Input Rail Filter and Detection Logic

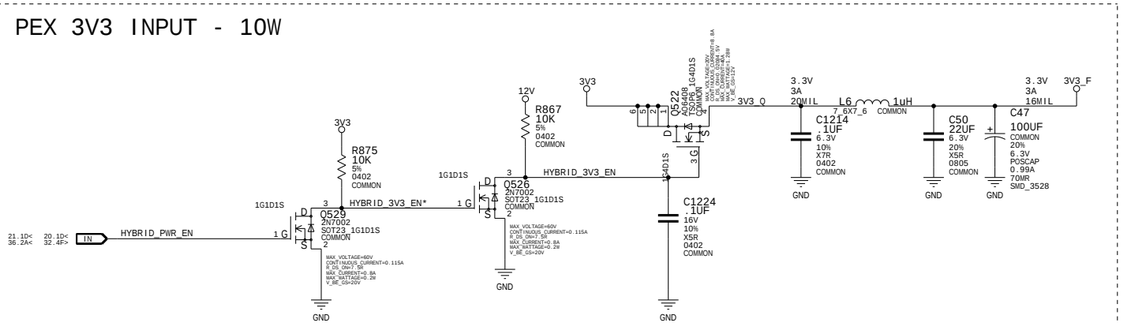
Connector Power State Table

2x3 Connector	2x3 Connector		Power	STATE
Connected	Connected		225W	Full Perf
Connected	Not Connected		150W	Board Off
Not Connected	Connected		150W	Board Off
Not Connected	Not Connected		75W	Board Off

PEX_12V INPUT - 66W

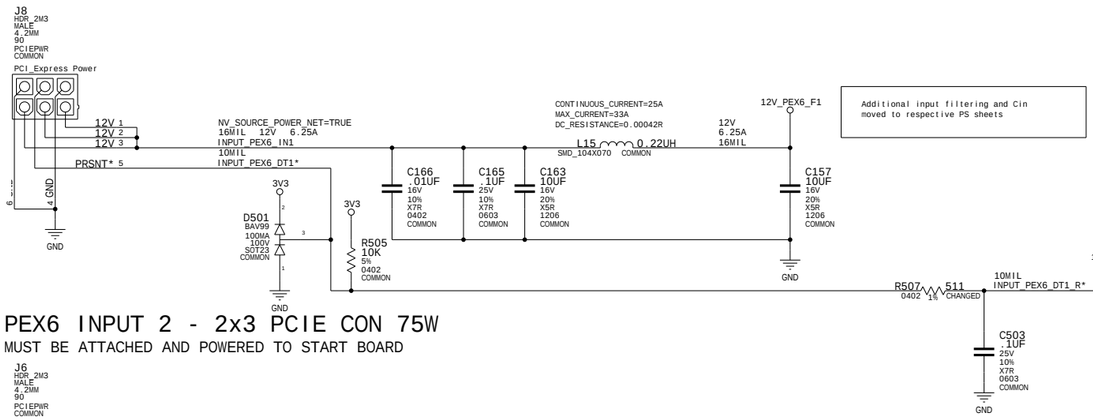


PEX 3V3 INPUT - 10W



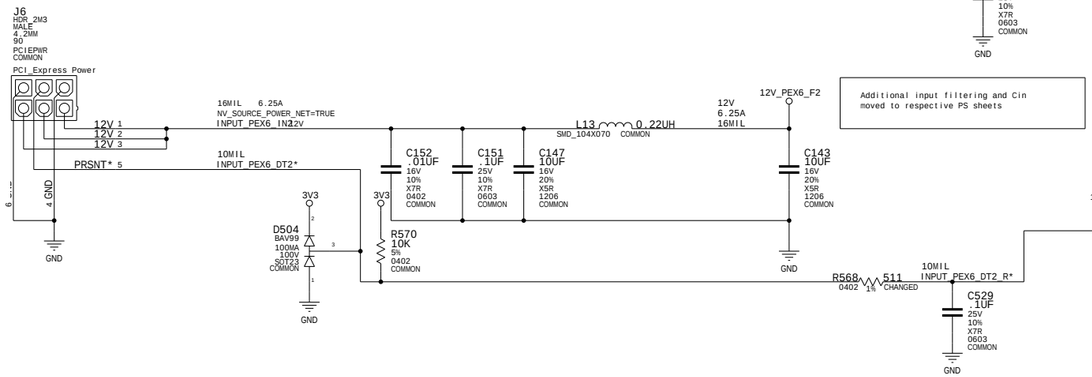
PEX6 INPUT 1 - 2x3 PCIE CON 75W

MUST BE ATTACHED AND POWERED TO START BOARD

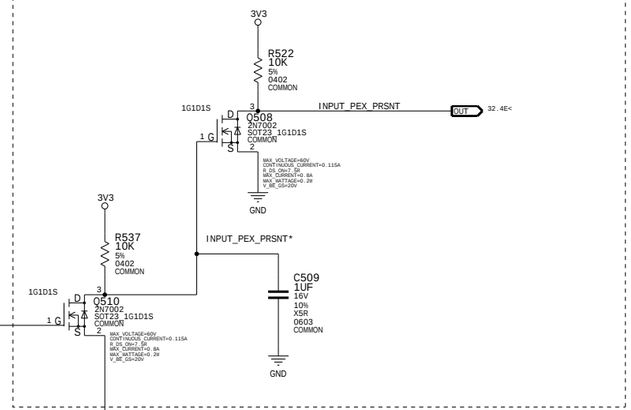


PEX6 INPUT 2 - 2x3 PCIE CON 75W

MUST BE ATTACHED AND POWERED TO START BOARD



Summary PEX input present



ASSEMBLY	DT, GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power: Input Rail Filter and Detection Logic

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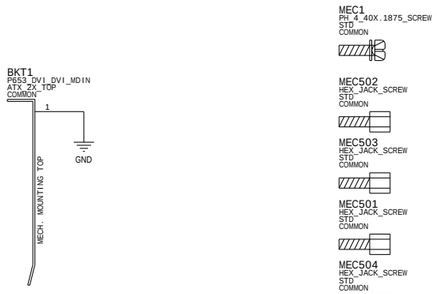
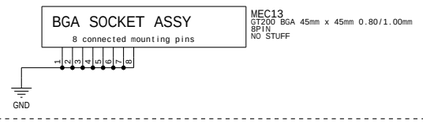
Thermal/Mechanical/ID

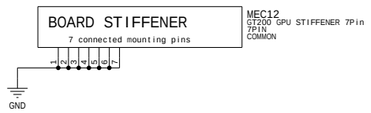
Bracket and Assembly



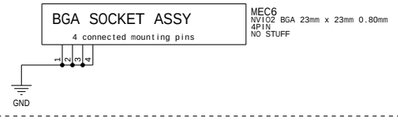
GPU Socket



GPU Stiffener



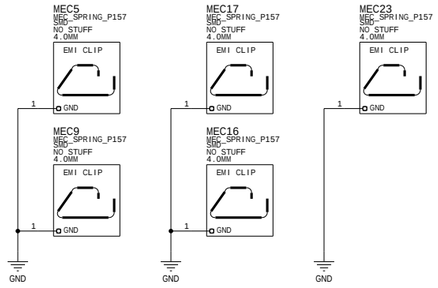
NVIOx Socket



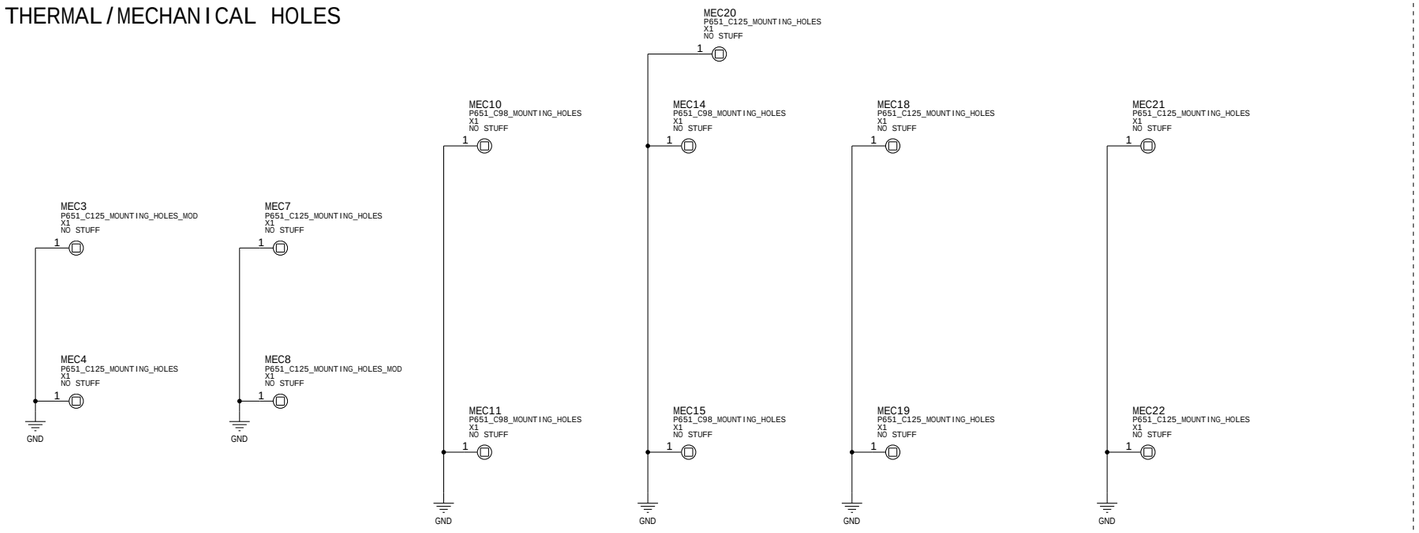
Hockey Stick Retention Mechanism

EMI Gnd Clips

Top Side Clips



THERMAL/MECHANICAL HOLES



ASSEMBLY	DT, GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Thermal/Mechanical

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10654-0051-300 D		
ID	design	PAGE	41 OF 41
NAME	Raite/Simon	DATE	22-OCT-2008