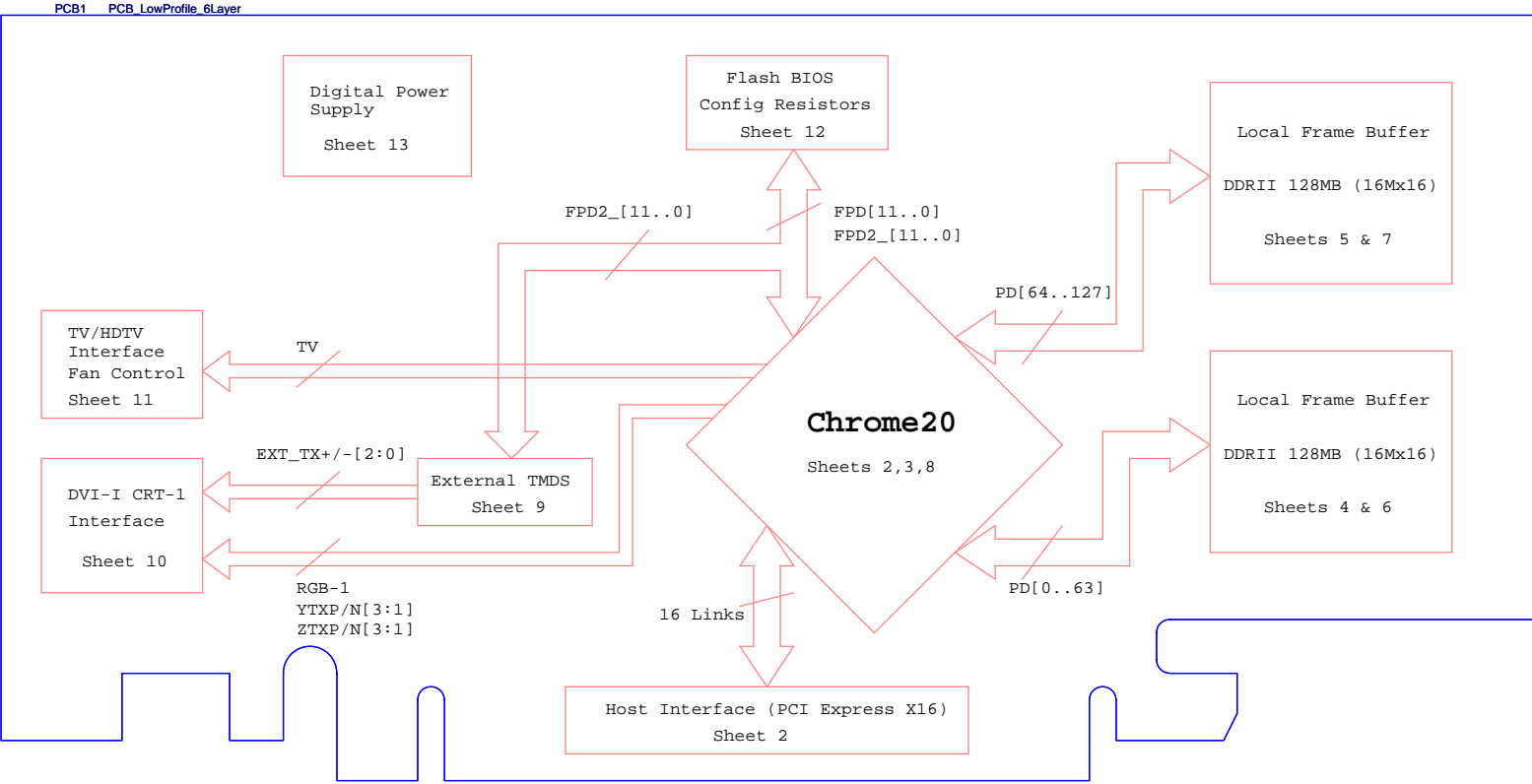



# Chrome20 "LOW PROFILE MONTEREY" DESKTOP

PCB No: VT6330A



DESCRIPTION OF CHANGE		DATE
A.01	Schematic created	01/16/06



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Title

Block Diagram

Size

B

Document Number

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Date

Thursday, February 16, 2006

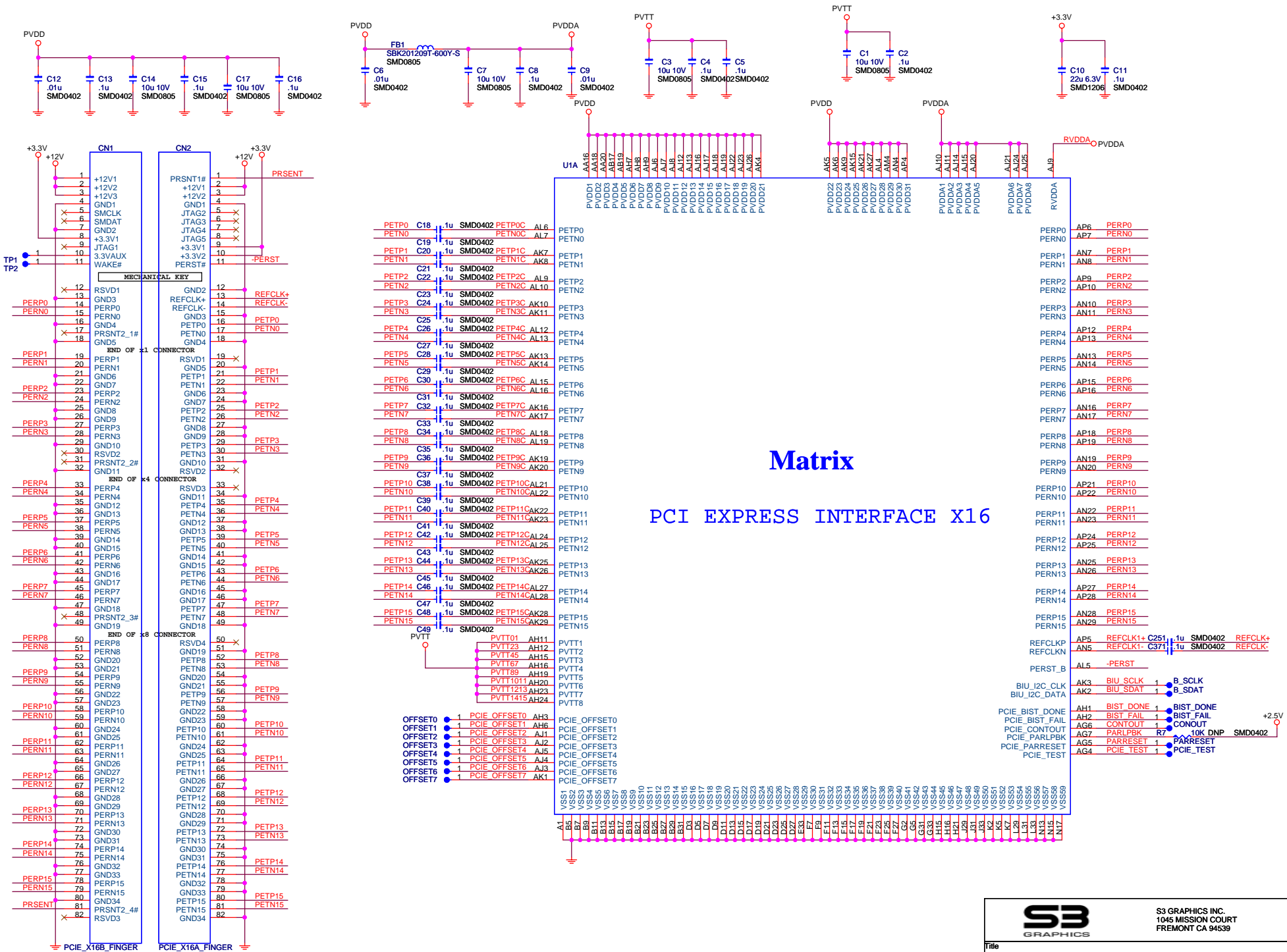
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THE INFORMATION CONTAINED IN THIS DOCUMENT IS PRELIMINARY AND SUBJECT TO CHANGE. S3 GRAPHICS BEARS NO RESPONSIBILITY FOR ANY ERRORS IN THESE DRAWINGS

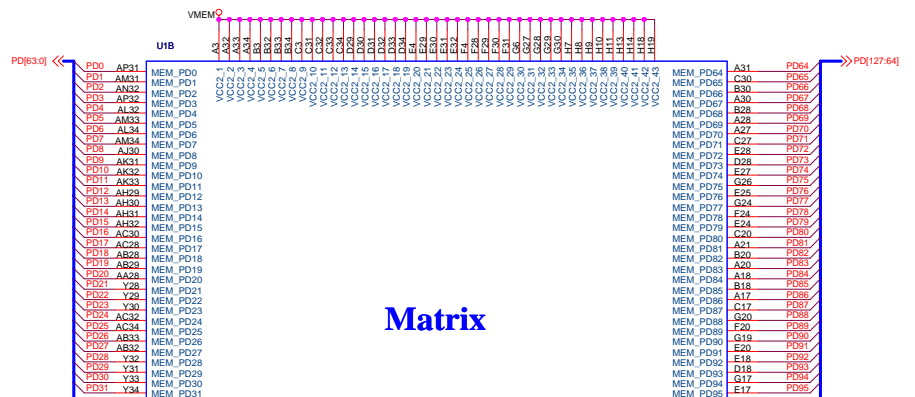
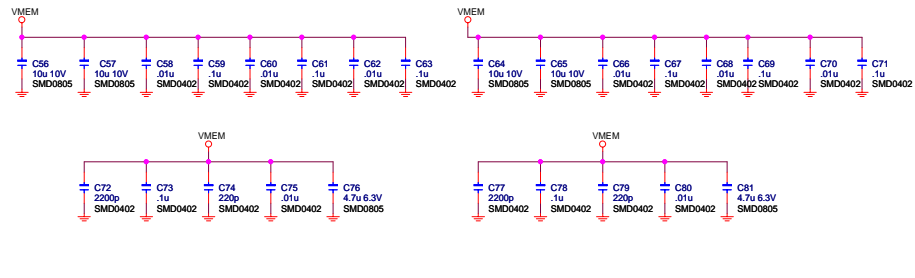


NOTES:  
1. "DNP" BY A COMPONENT MEANS "DO NOT POPULATE COMPONENT".

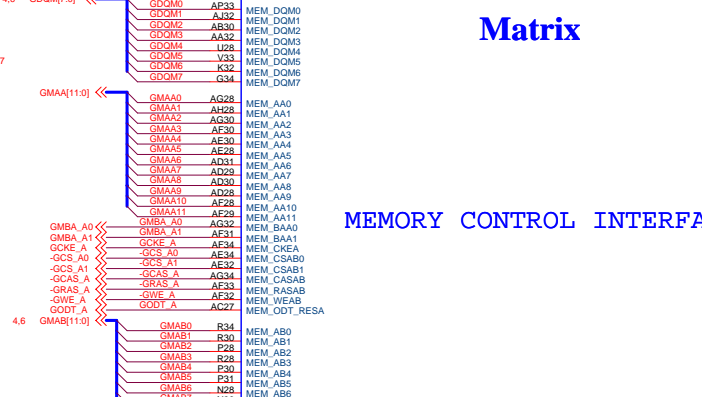
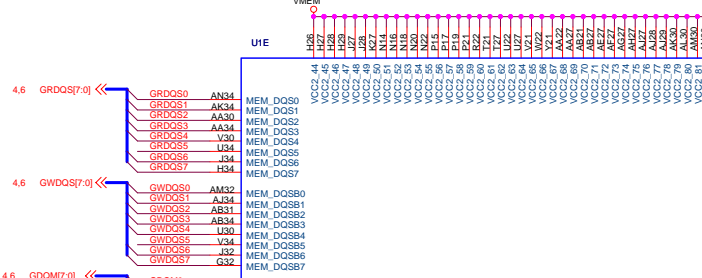
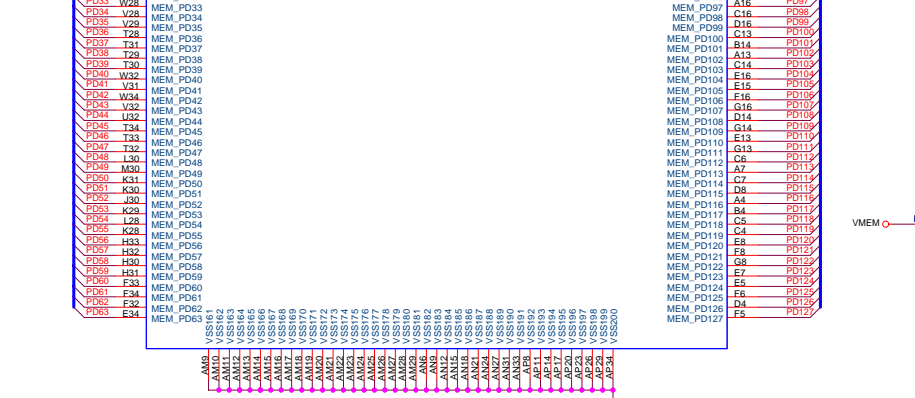


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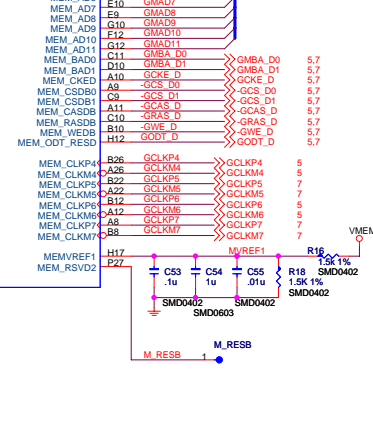
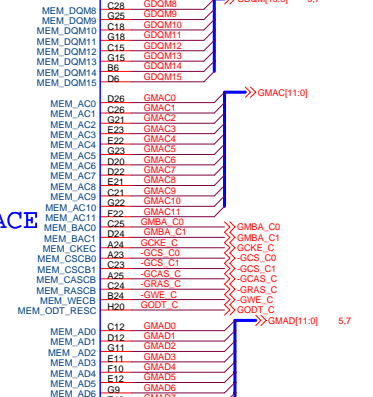
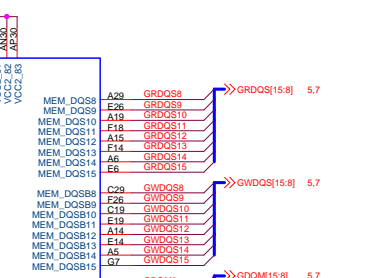
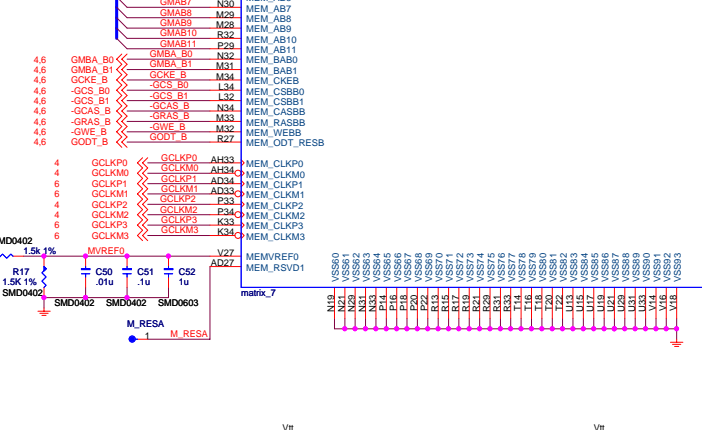
Title <b>PCIe Interface</b>		
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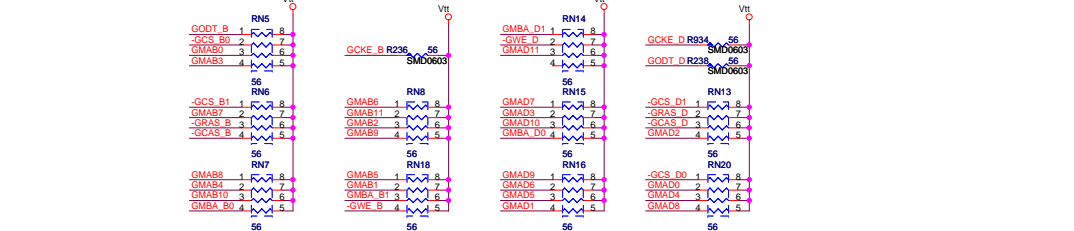
### MEMORY DATA INTERFACE

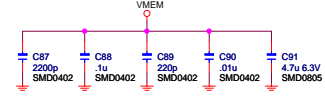
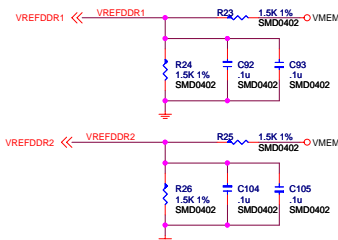
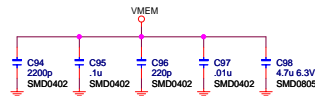
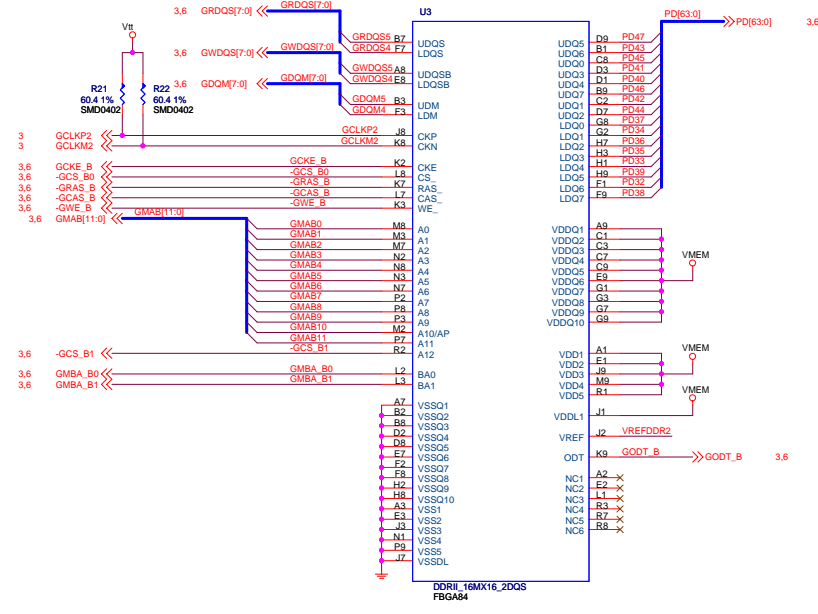
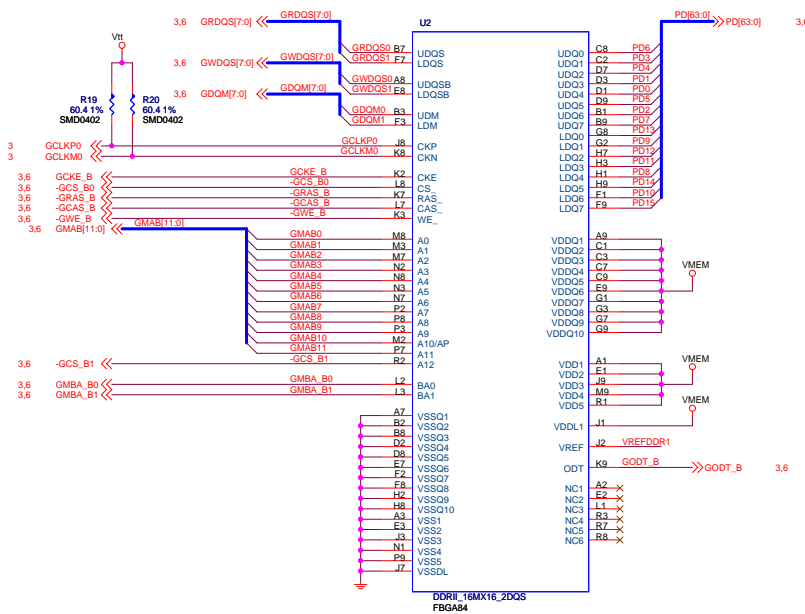


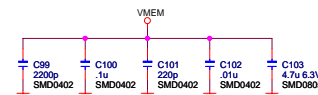
### Matrix

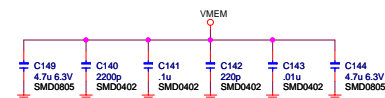


### MEMORY CONTROL INTERFACE











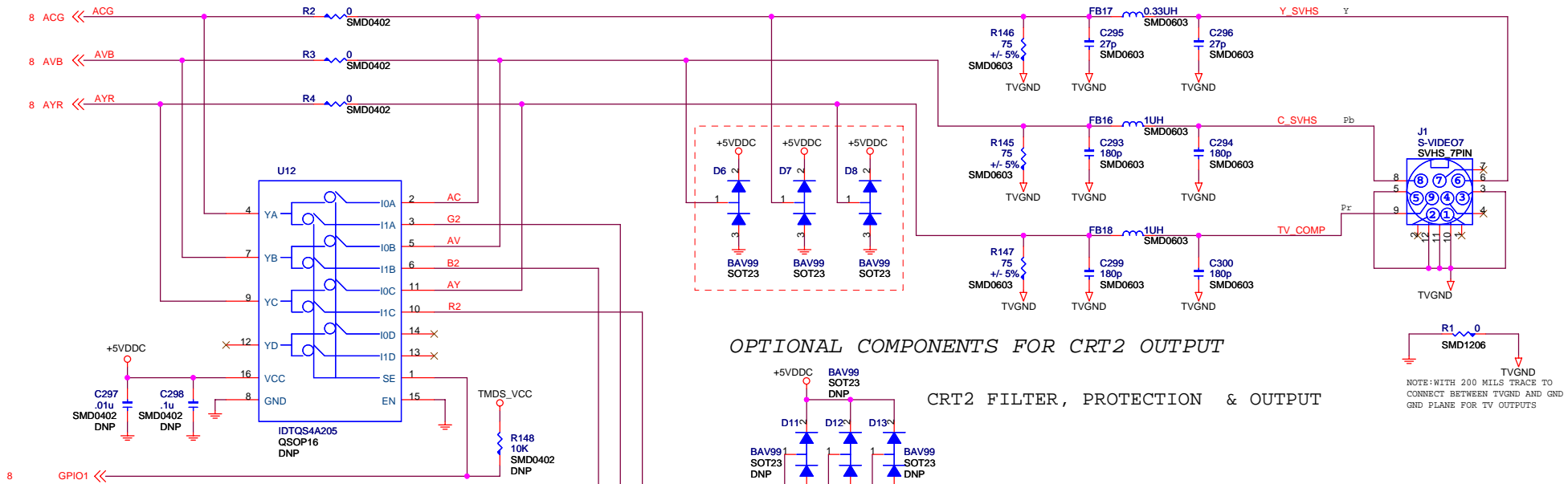




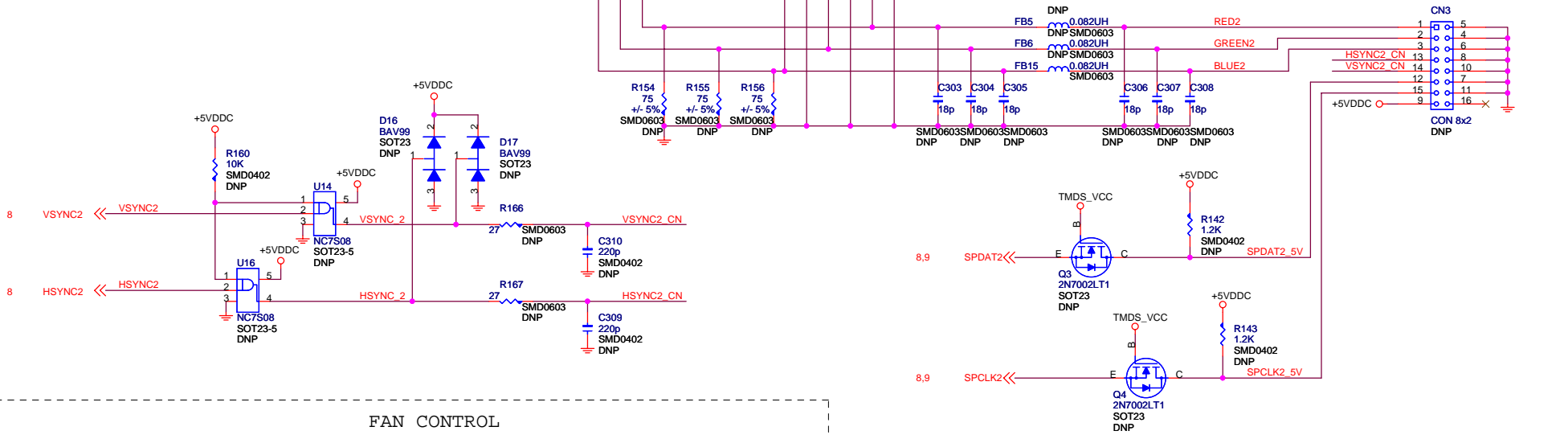




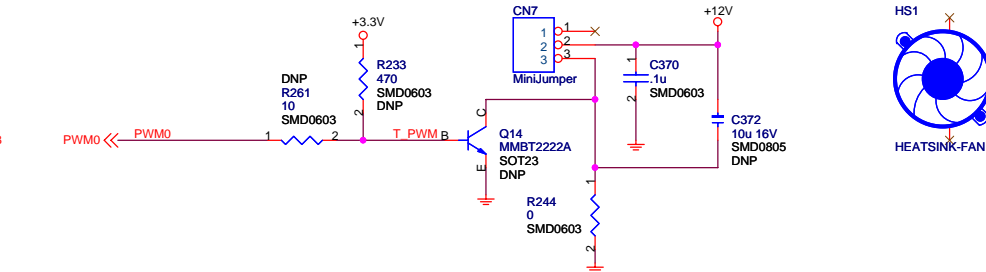
## TV FILTER, PROTECTION &amp; OUTPUT



## CRT2 FILTER, PROTECTION & OUTPUT



## FAN CONTROL



NOTES:

1. "DNP" BY A COMPONENT MEANS "DO NOT POPULATE COMPONENT".



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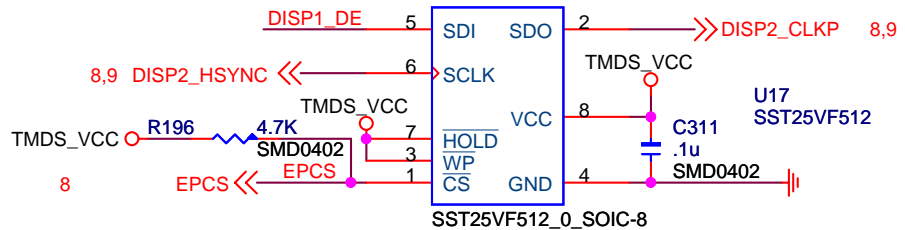
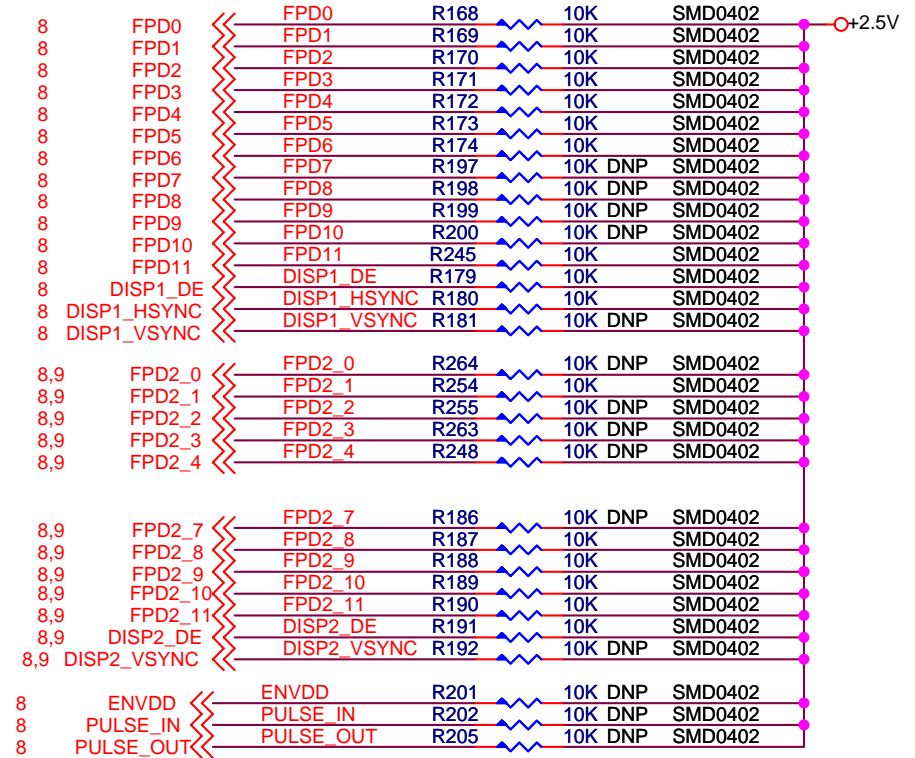
Title			
<b>TV / CRT2 / HDTV PORT &amp; FAN CONTROL</b>			
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# Strapping pins

REGISTER	SIGNAL	FUNCTION	VALUE	STUFF	RESISTOR
CR36_0	FPD0	PCIE LO NOT SUPPORTED	"0"	YES	
		PCIE LO SUPPORTED (DEFAULT)	"1"		R168
		PCIE L1 NOT SUPPORT	"0"	YES	
CR36_1	FPD1	PCIE L1 SUPPORTED (DEFAULT)	"1"		R169
		PCIE SCRAMBLE (DEFAULT)	"0"	YES	
		PCIE SCRAMBLE DISABLE	"1"		R170
CR36_2	FPD2	PCIE MSI_EN DISABLE (DEFAULT)	"0"	YES	
		PCIE MSI_EN ENABLE	"1"		R171
CR36_3	FPD3	PCIE NOT COMMON CLOCK	"0"	YES	
		PCIE COMMON CLOCK (DEFAULT)	"1"		R172
CR36_4	FPD4	USE PCIE INTERNAL PCLK (DEFAULT)	"0"	YES	
		USE PCIE EXTERNAL PCLK	"1"		R173
CR36_5	FPD5	PCIE 32-BIT ADDRESS MODE	"0"	YES	
		PCIE 64-BIT ADDRESS MODE	"1"		R174
CR36_6	FPD6	256K byte ROM size	"0"		
		64K byte ROM size	"1"	NO	R197
CR36_7	FPD7	ROM TYPE BIT-3..0] CR37[3..0]	"0"		
		000 SST SST39VF512 (PARALLEL 512kBIT)	"1"	NO	R198
		001 LPC ROM, SST49LF080A			
CR37_1	FPD9	100 ATMEL 25F1024 (SERIAL 1MBIT)	"0"		
		101 ST MICRO 25P10 (SERIAL 1MBIT)	"1"	NO	R199
		110 ST MICRO 25P05 (SERIAL 512kBIT)			
CR37_2	FPD10	111 SST SST25VF512 (SERIAL 512kBIT)	"0"		
		OTHERS RESERVED	"1"	NO	R200
CR37_3	FPD11	ROM CLK is PCLK/32	"0"	YES	
		ROM CLK is PCLK/16	"1"		R245
CR37_4	DISP1_DE	X16 PCI EXPRESS LINK WIDTH (DEFAULT)	"0"	YES	
		X8 PCI EXPRESS LINK WIDTH	"1"		R179
CR37_5	DISP1_HSYNC	MEMORY SPEED BITS[ 2..0] CR68[3]CR37[6..5]	"0"	YES	
		000 RESERVED 100 RESERVED	"1"		R180
		001 RESERVED 101 400MHz	"0"		
CR37_6	DISP1_VSYNC	010 300MHz	"1"	NO	R181
		011 350MHz	"0"		
		111 RESERVED	"0"		
CR68_3	FPD2_4		"1"	NO	R248
CR6F_7	ENVDD	HYNIX	"0"		
		SAMSUNG	"1"	NO	R201
CR37_7	FPD2_0	USE EXTERNAL MCLK/MCLK90 ON EXTCLK/SPDAT2	"0"		
		USE INTERNAL MCLK/MCLK90 (DEFAULT)	"1"	NO	R264
CR68_0	FPD2_1	USE EXTERNAL ECLK ON EXTECLK	"0"	YES	
		USE INTERNAL ECLK (DEFAULT)	"1"		R254
CR68_1	FPD2_2	USE EXTERNAL DCLK1 ON XIN	"0"		
		USE INTERNAL DCLK1 (DEFAULT)	"1"	NO	R255
CR68_2	FPD2_3	USE EXTERNAL DCLK2 ON SPDAT4	"0"		
		USE INTERNAL DCLK2 (DEFAULT)	"1"	NO	R263
CR68_7	FPD2_8	CRYSTAL CONNECTED TO XIN, XOUT (DEFAULT)	"0"	YES	
		OSCILLATOR CONNECTED TO XIN	"1"		R187
CR68_6	FPD2_7	1 RANK POPULATED	"0"		
		2 RANKS	"1"	NO	R186
CR6F_0	FPD2_9	POPULATED	"0"	YES	
		000 DDR2 16Mx16 100 DDR1 16Mx16	"1"		R188
		001 DDR3 8Mx32 101 DDR1 8Mx32	"0"	YES	R189
CR6F_1	FPD2_10	010 DDR2 32Mx16 110 DDR1 8Mx16	"1"		
		011 DDR3 16Mx32 111 DDR1 4Mx32	"0"	YES	R190
			"1"		
CR6F_3	DISP2_DE	00 0 FB	"0"	YES	
		01 32-BIT MEMORY BUS WIDTH	"1"		R191
		10 128-BIT MEMORY BUS WIDTH	"0"		
CR6F_5	DISP2_VSYNC	11 64-BIT MEMORY BUS WIDTH(DEFAULT)	"1"	NO	R192
			"0"		
CRCF1_6	PULSE_IN	FB MEMORY SIZE = 256M (DEFAULT)	"0"	NO	
		FB MEMORY SIZE = 512M	"1"		R202
CRCF1_7	PULSE_OUT	BIGENDIAN DISABLE (DEFAULT)	"0"	NO	
		BIGENDIAN ENABLE	"1"		R205

## NOTES:

1. "DNP" BY A COMPONENT MEANS "DO NOT POPULATE COMPONENT".



		S3 GRAPHICS INC. 1045 MISSION COURT FREMONT CA 94539	
		Title	
<h2>VGA BIOS EEPROM &amp; Config Setting</h2>			
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