

PG410 A01

GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI/DP + DP

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600-1G410-BASE-100

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A

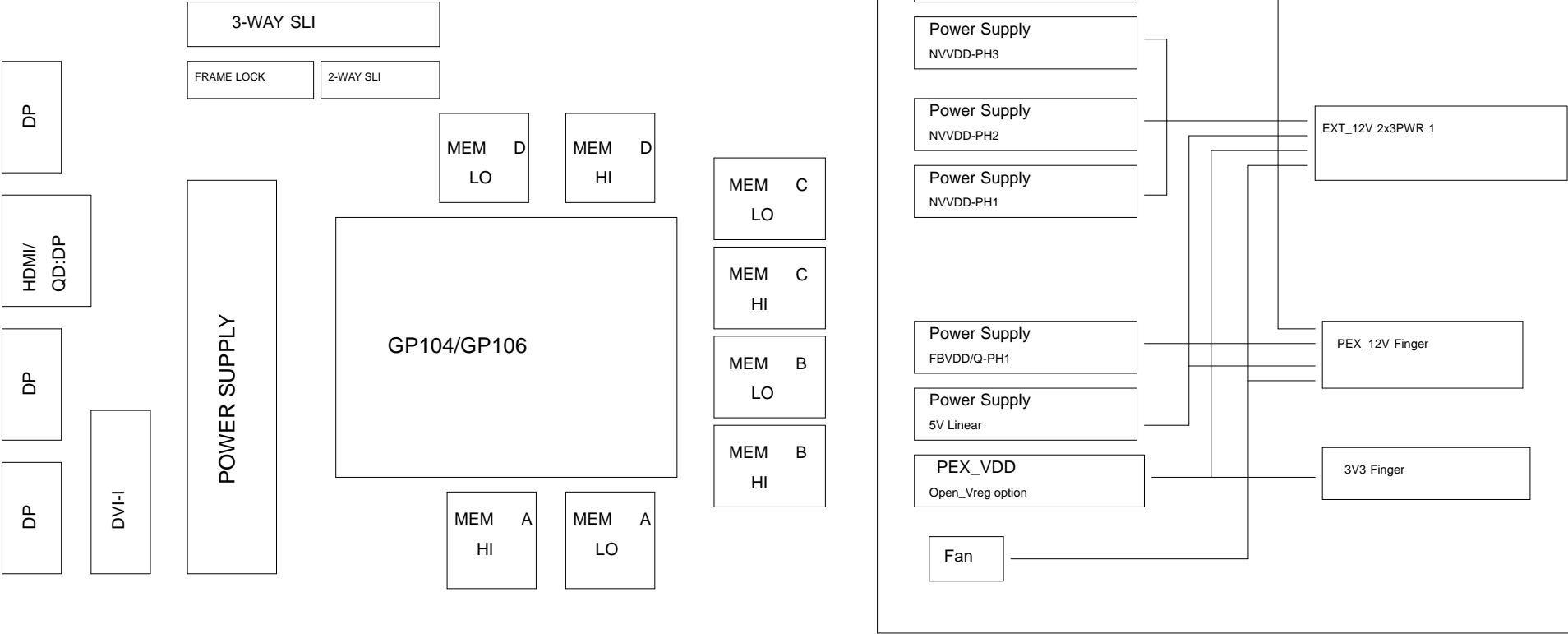
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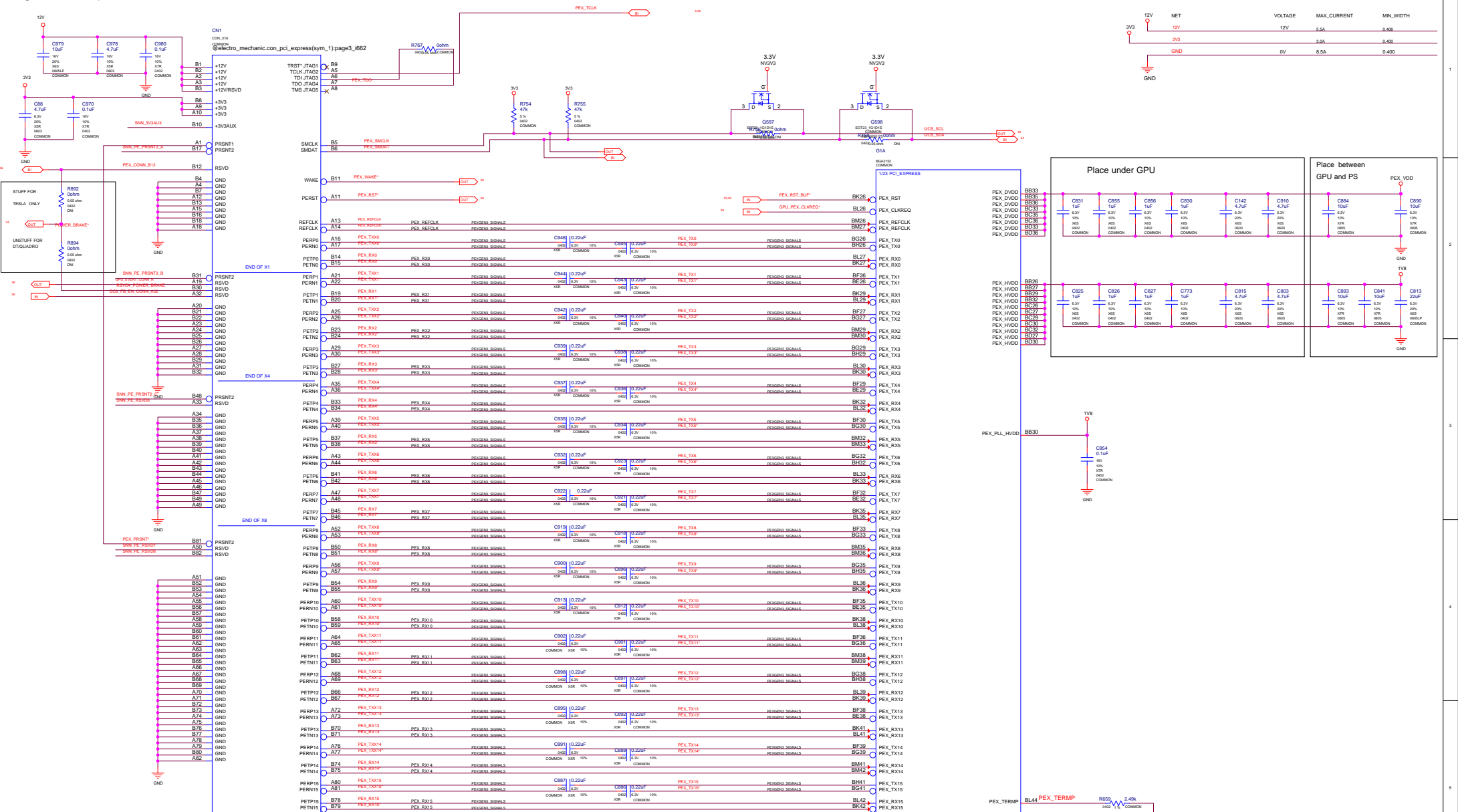




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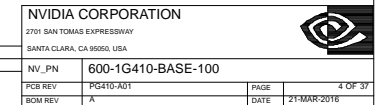
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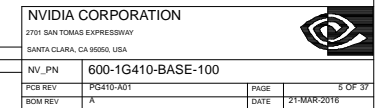


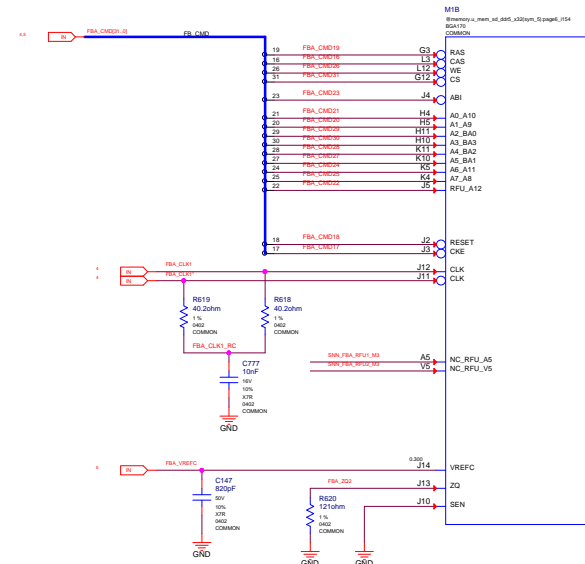
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PAGE DETAIL	PCI Express

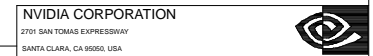
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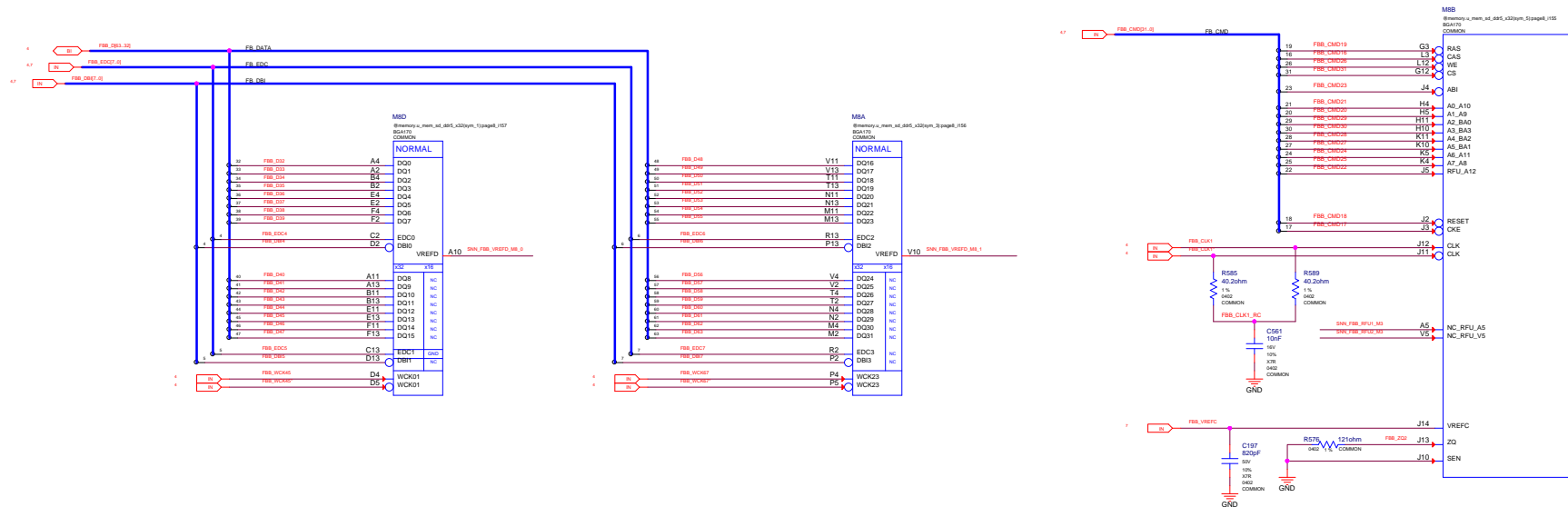








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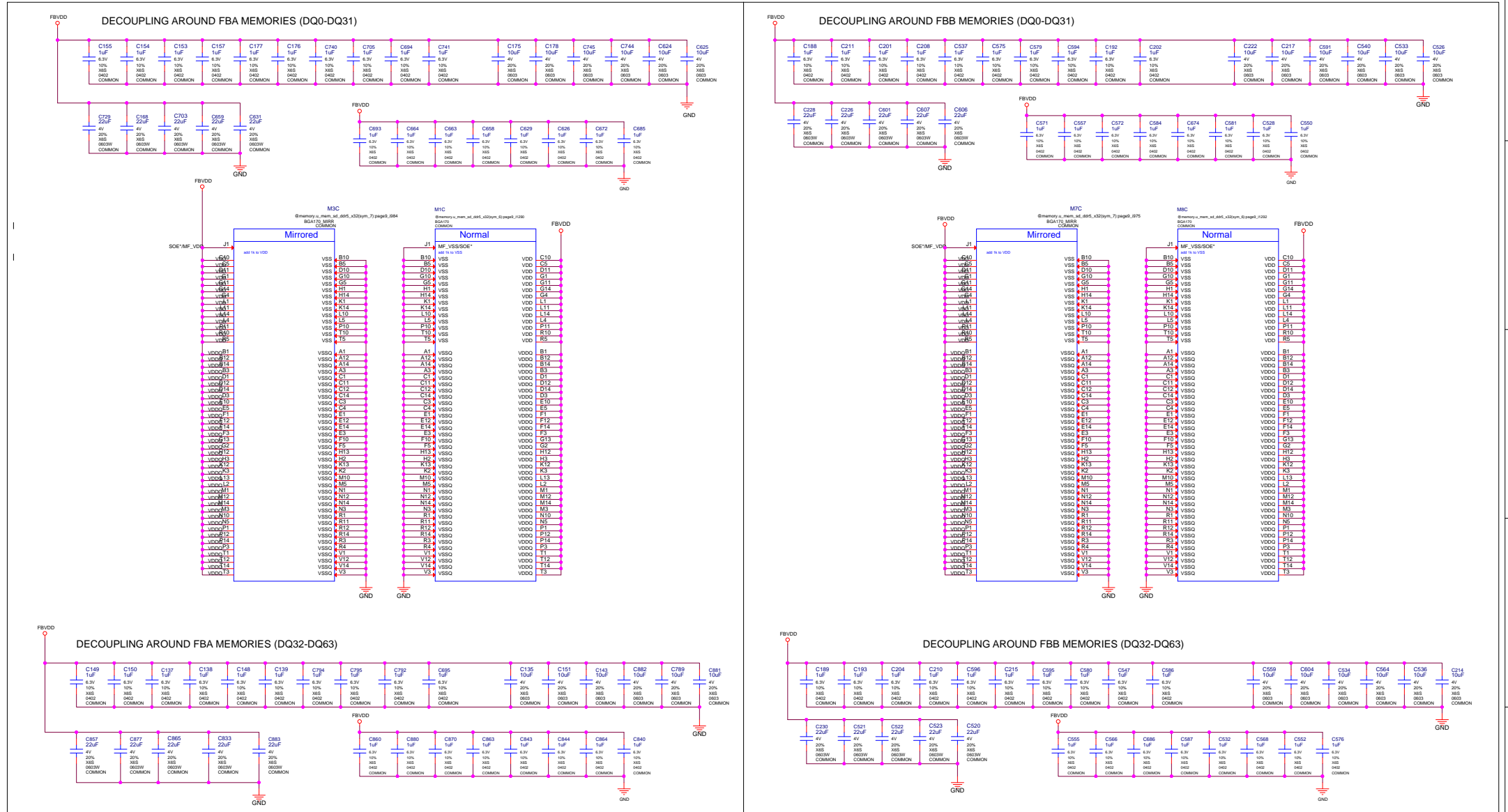


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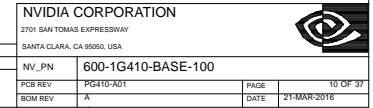
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>		
PAGE DETAIL	MEMORY: FB0[31:0]		

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PAGE DETAIL	MEMORY_FB0[63:32]		

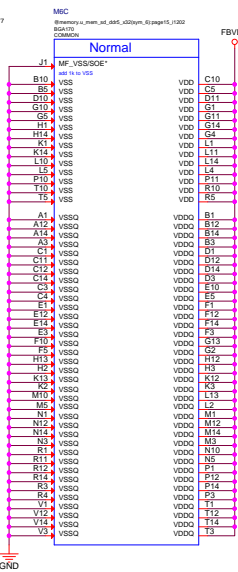
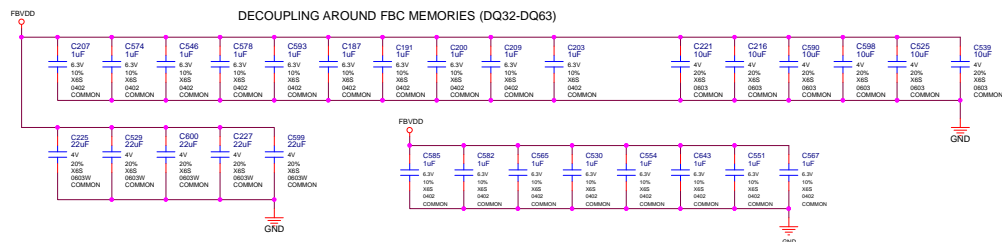
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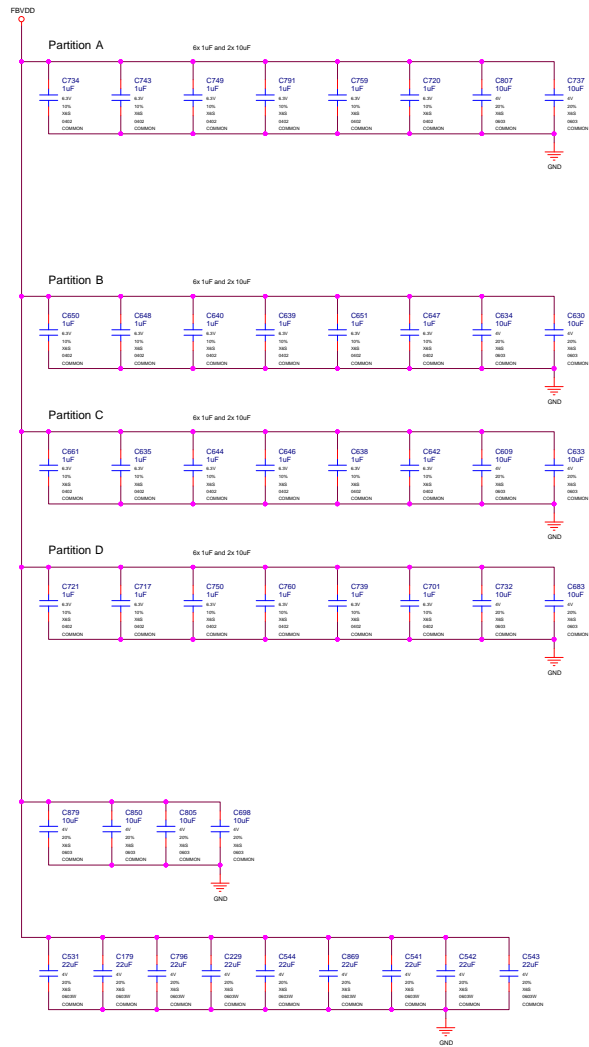


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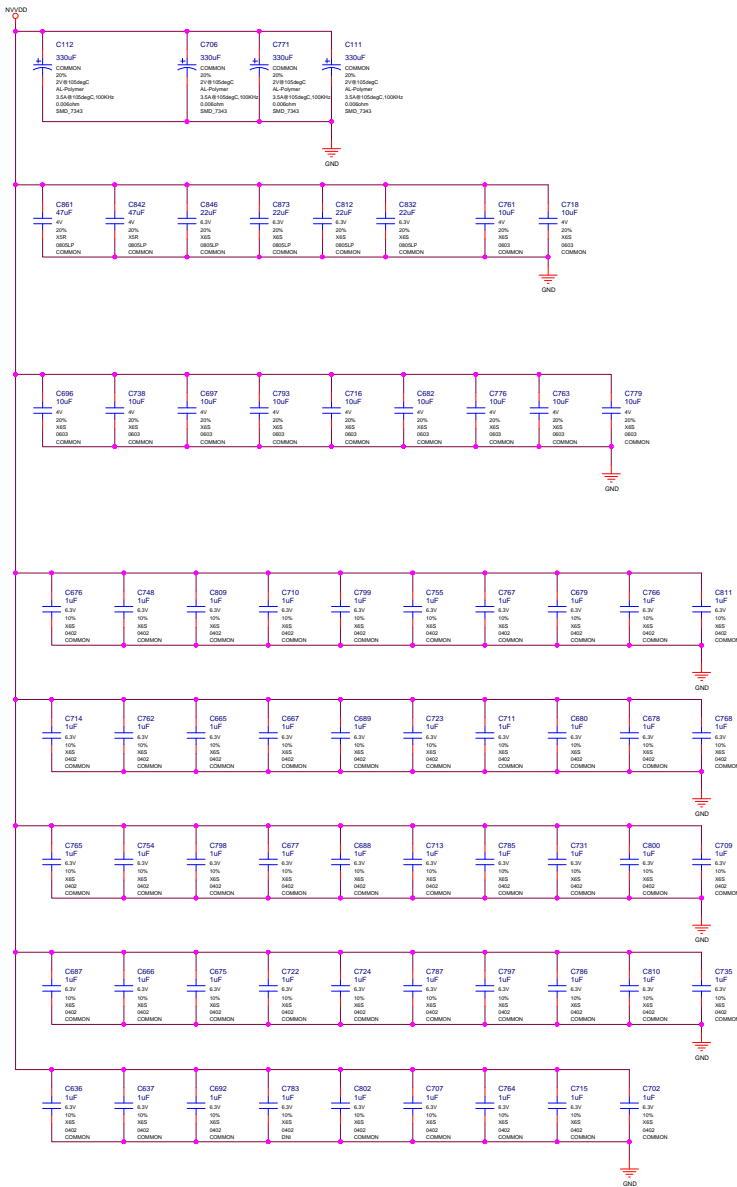


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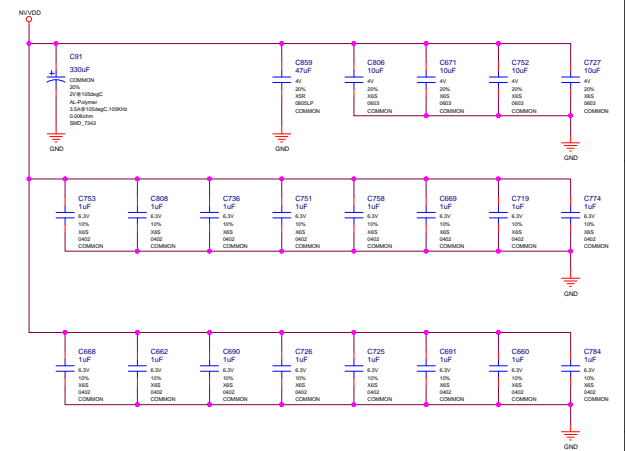
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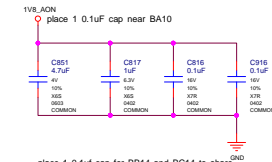
NVVDD



NVVDD

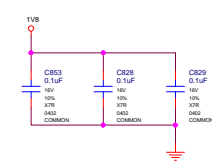


1V8_AON



place 1 0.1uF cap for BB14 and BC14 to share

1V8_MAIN



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	GPU Decoupling

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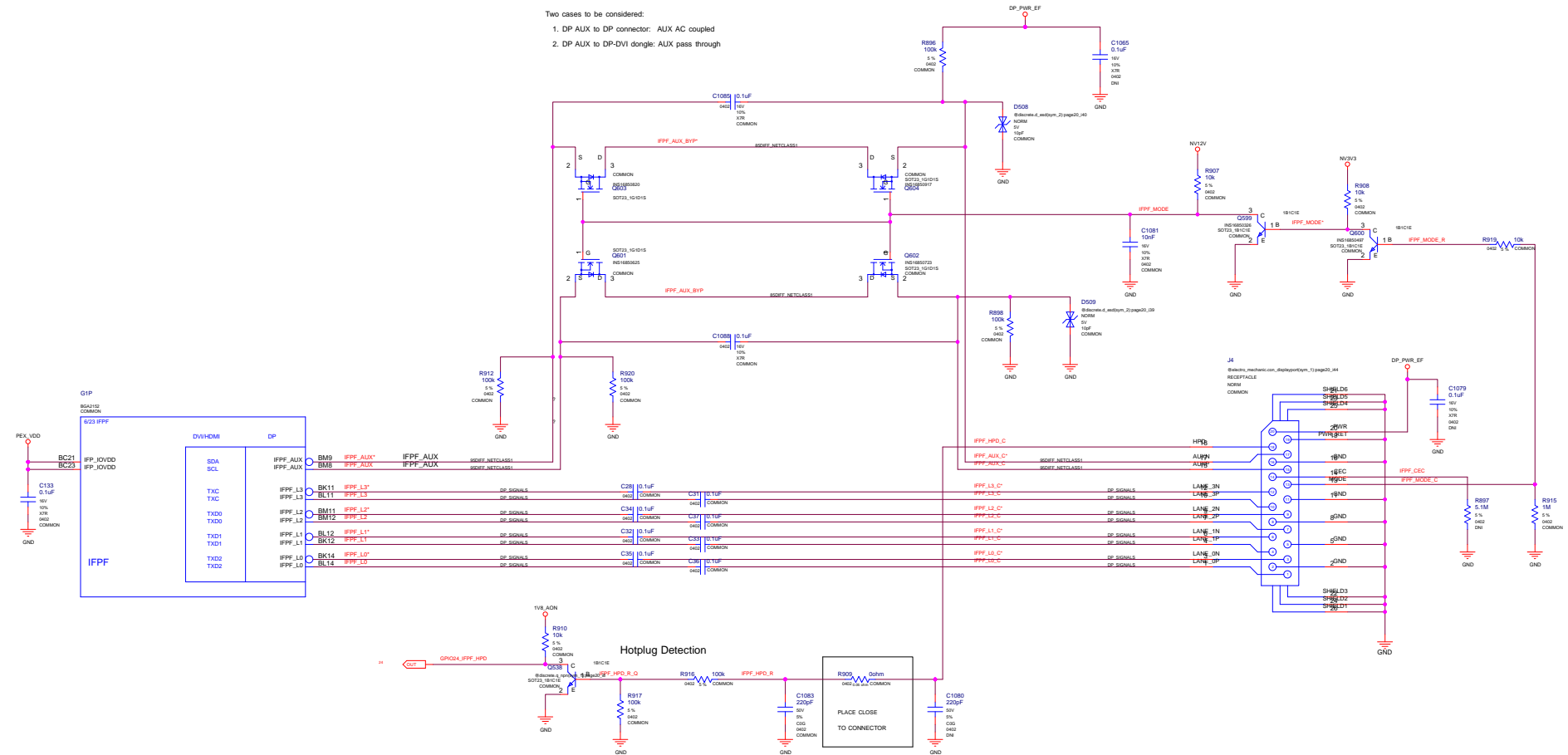
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1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPF DP

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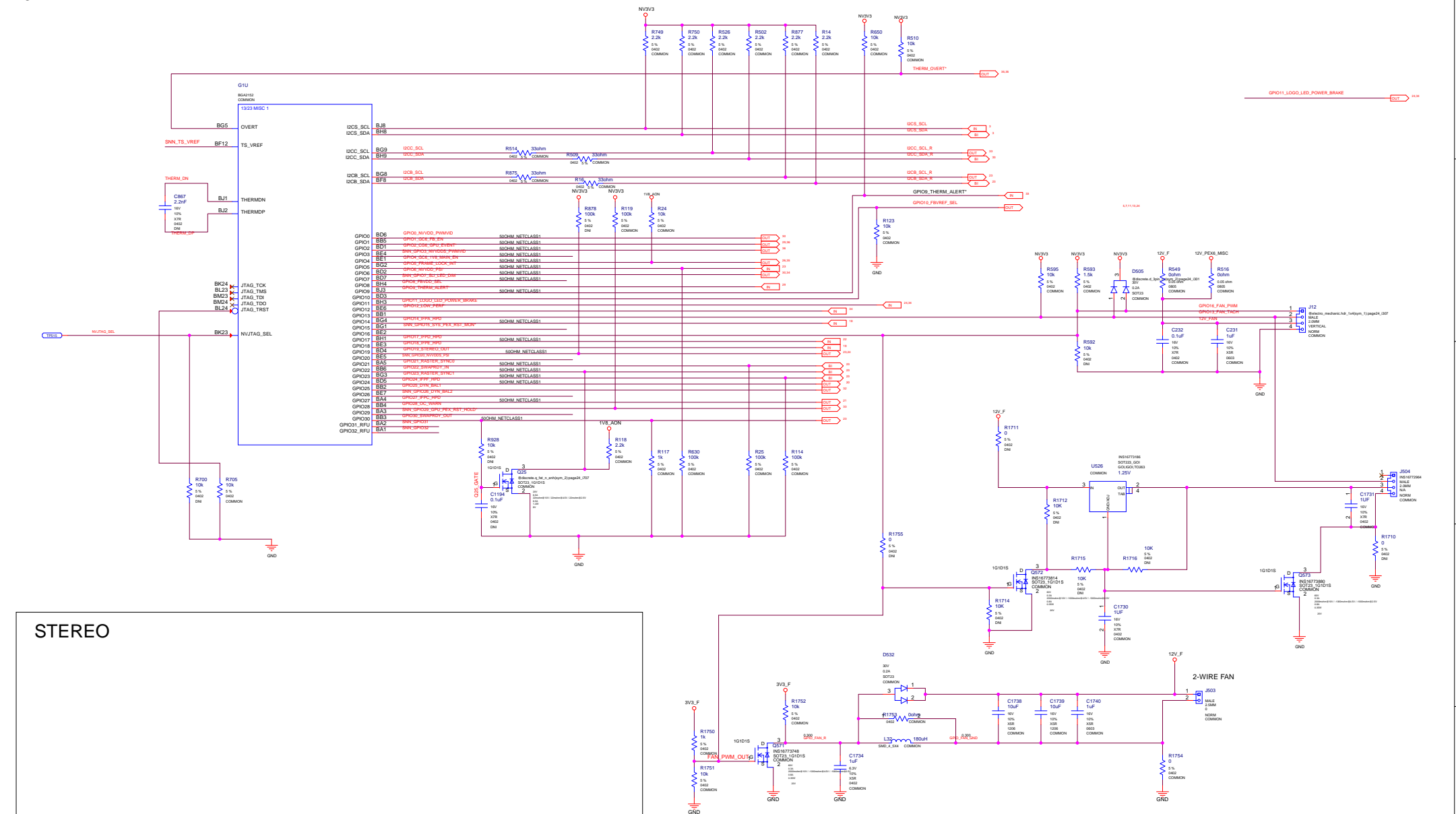


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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	0	0	0
L	H	M	1	0	1	1
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

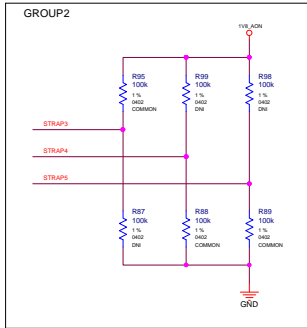
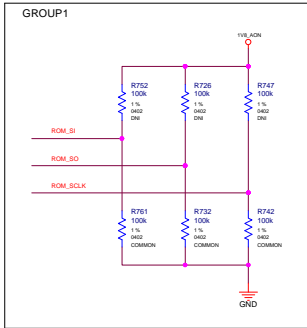
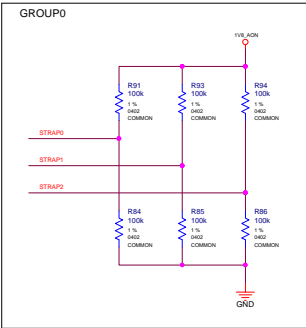
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

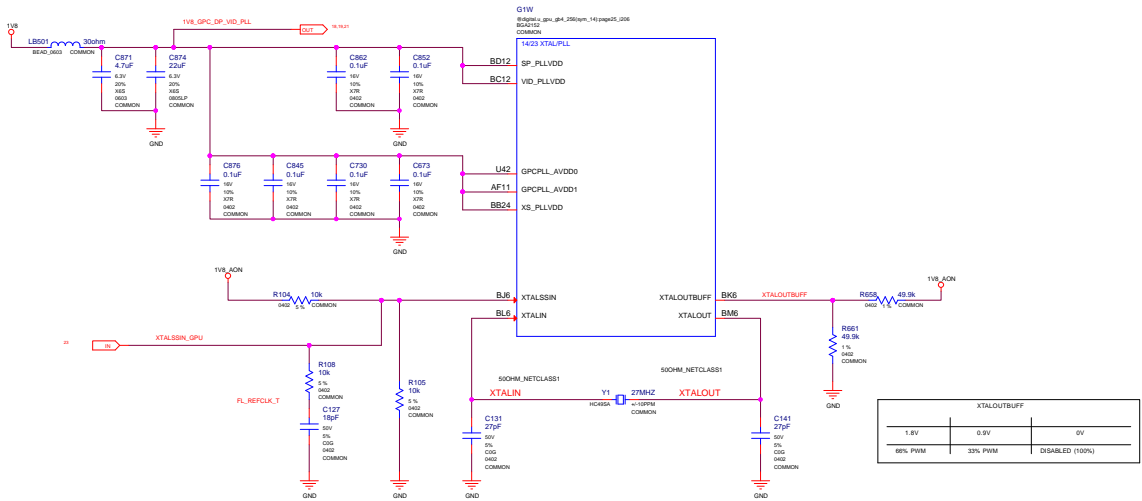
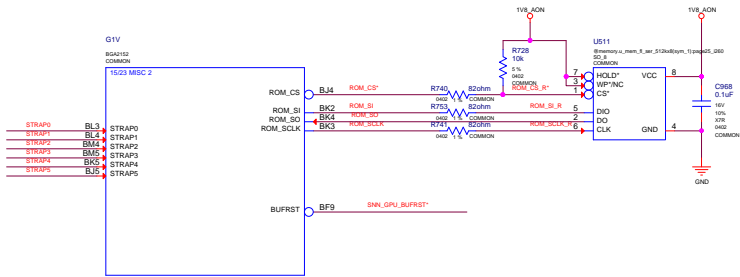
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL,STRAPS



CFG(3:0)	Config	Width	Vendor
0000	256Mx32 256-bit		Samsung
0001	256Mx32 256-bit		Micron
0010	256Mx32 256-bit		Hynix
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		



XTALOUTBUFF		
1.8V	0.9V	0V
80% PWM	33% PWM	DISABLED (100%)

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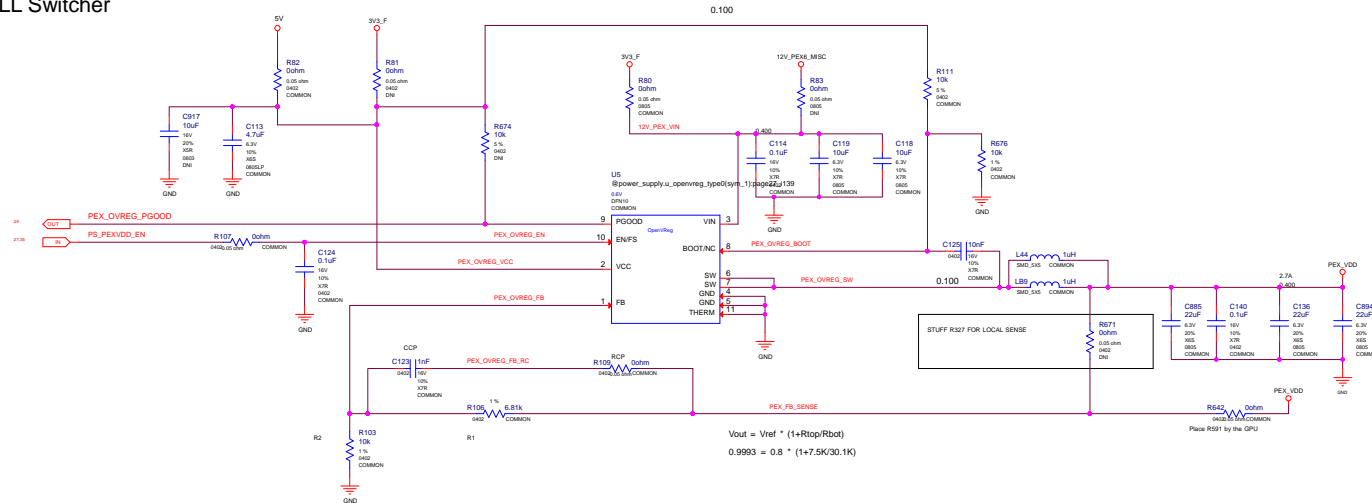


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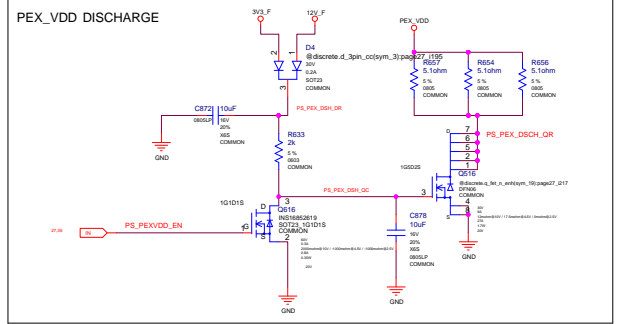
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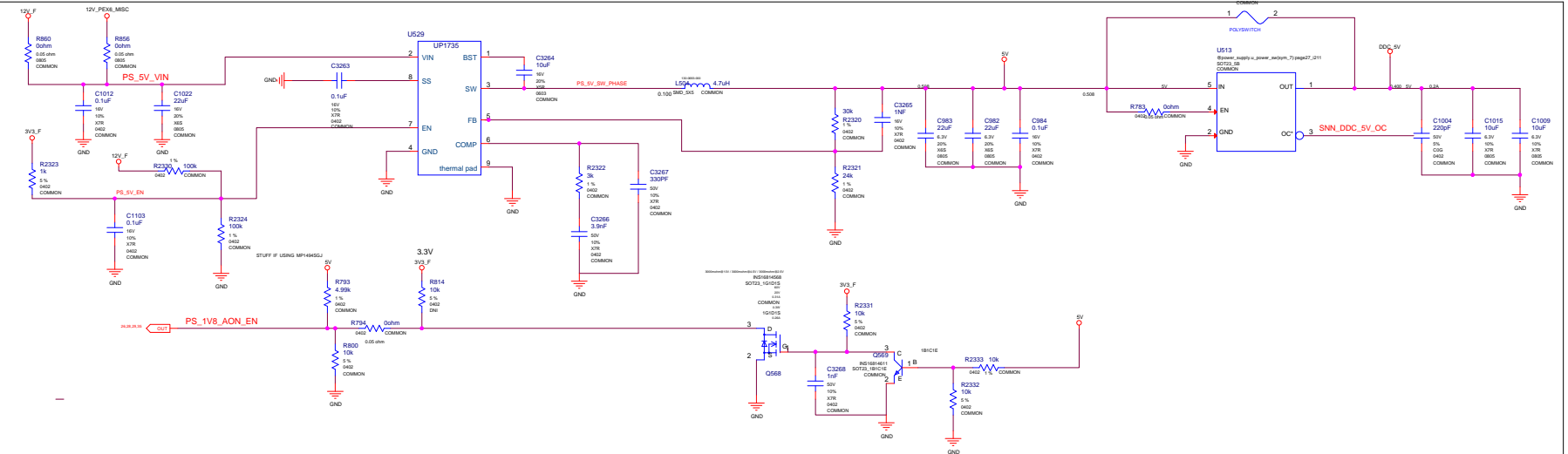
PEX PLL Switcher



PEX_VDD DISCHARGE



5V Switcher



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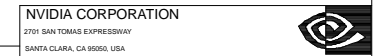
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PAGE DETAIL	PS_5V_PEX_VDD



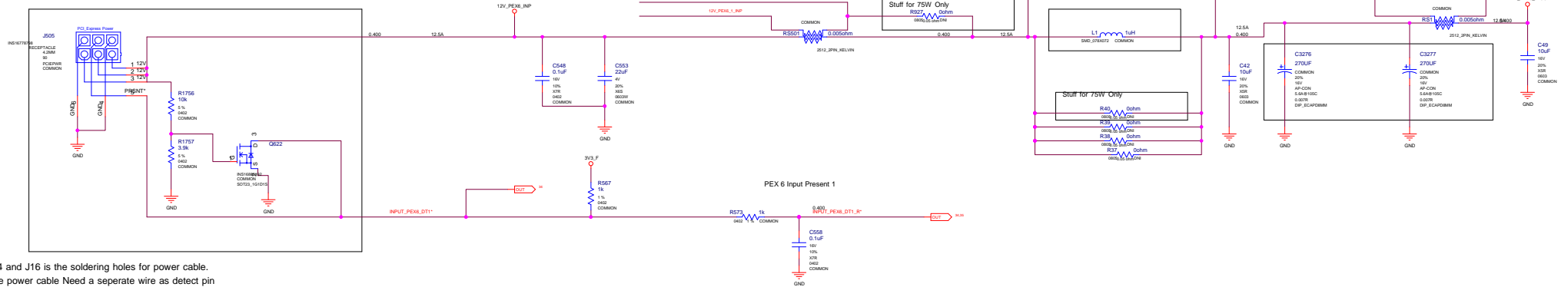
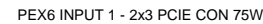
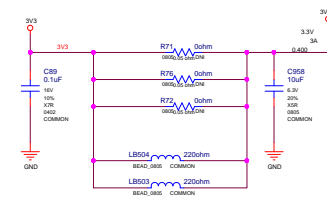
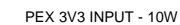
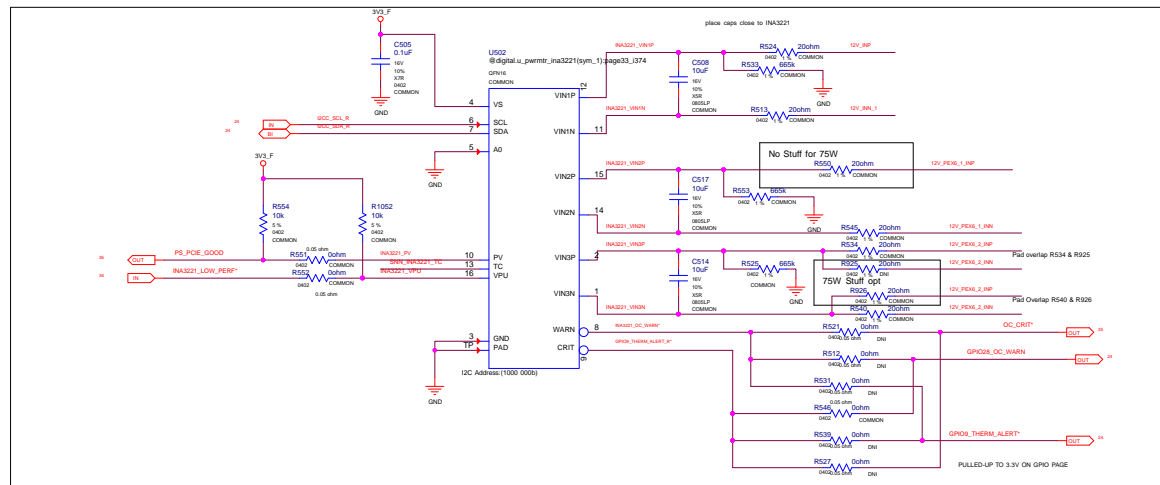
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MAY		DISCLAIMS ALL		PCB REV PG410-001	
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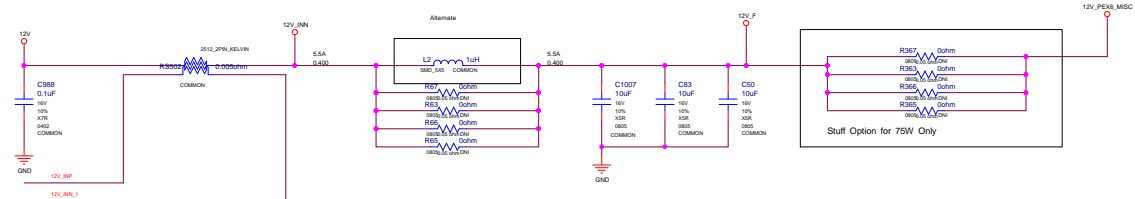
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>		
PAGE DETAIL	PS NVVDD Rail Balance Logic & Dynamic Phase		
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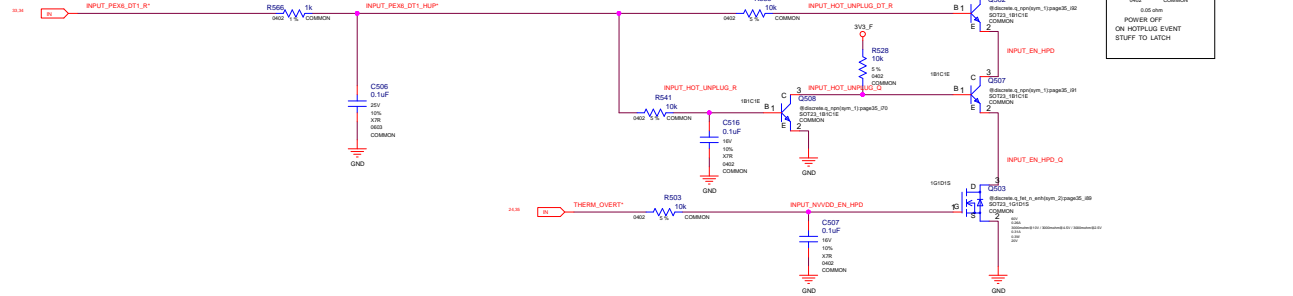


J14 and J16 is the soldering holes for power cable.
The power cable Need a seperate wire as detect pin
This detect wire need be soldered on J15

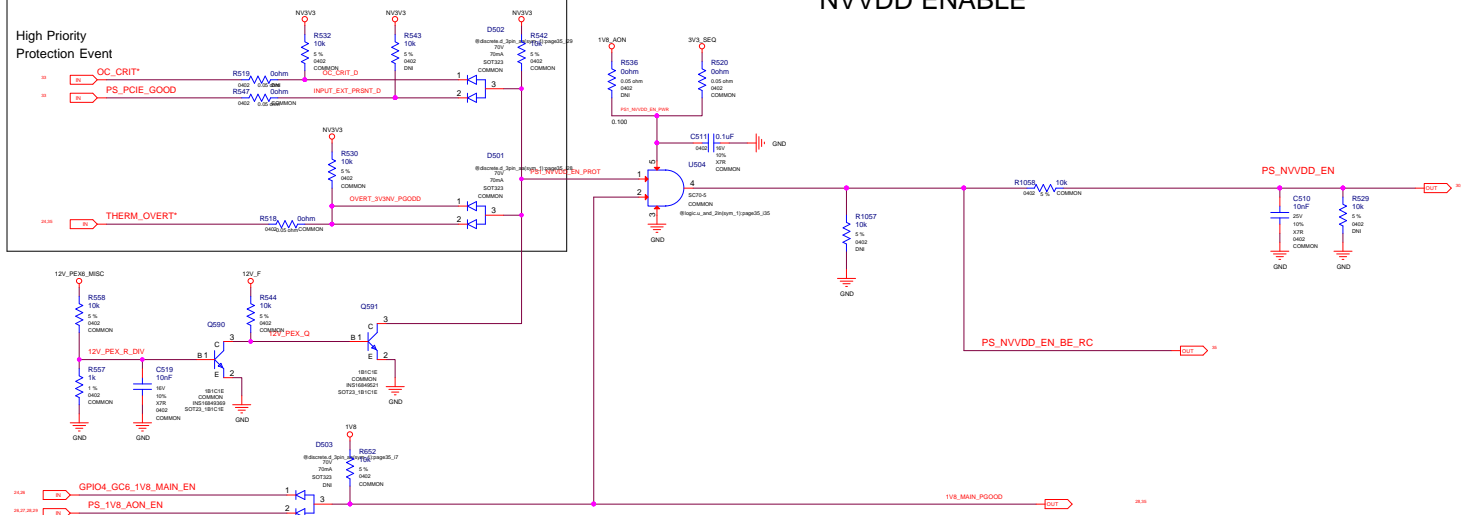


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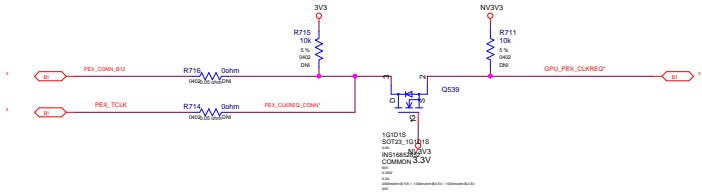
High Priority
Protection Event



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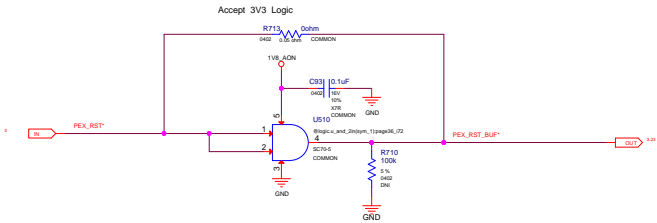
[illegible]

PEX_CLKREQ*



GPU_EVENT*

PEX_RST# LOGIC

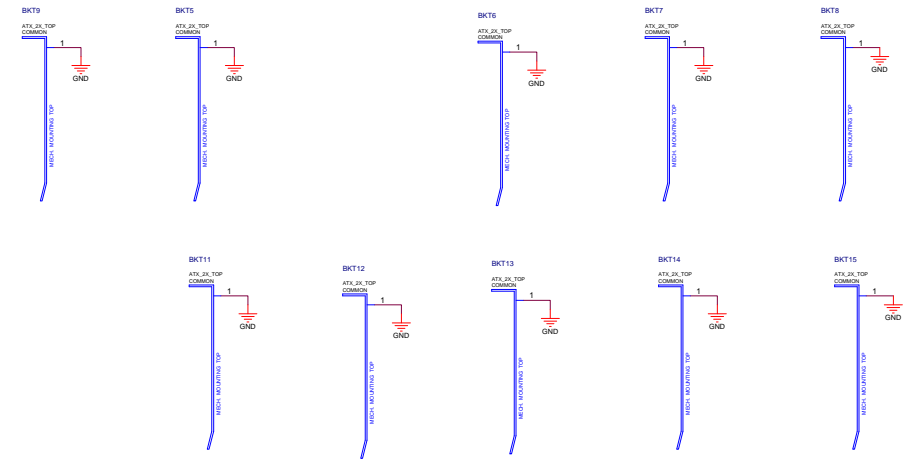


GC6 FB ENABLE

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GPU Stiffener:



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