

PG174-A01

TU117, 128b GDDR5 x32, 75W
DVI-D DL/DUAL DP + HDMI

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BCM REV

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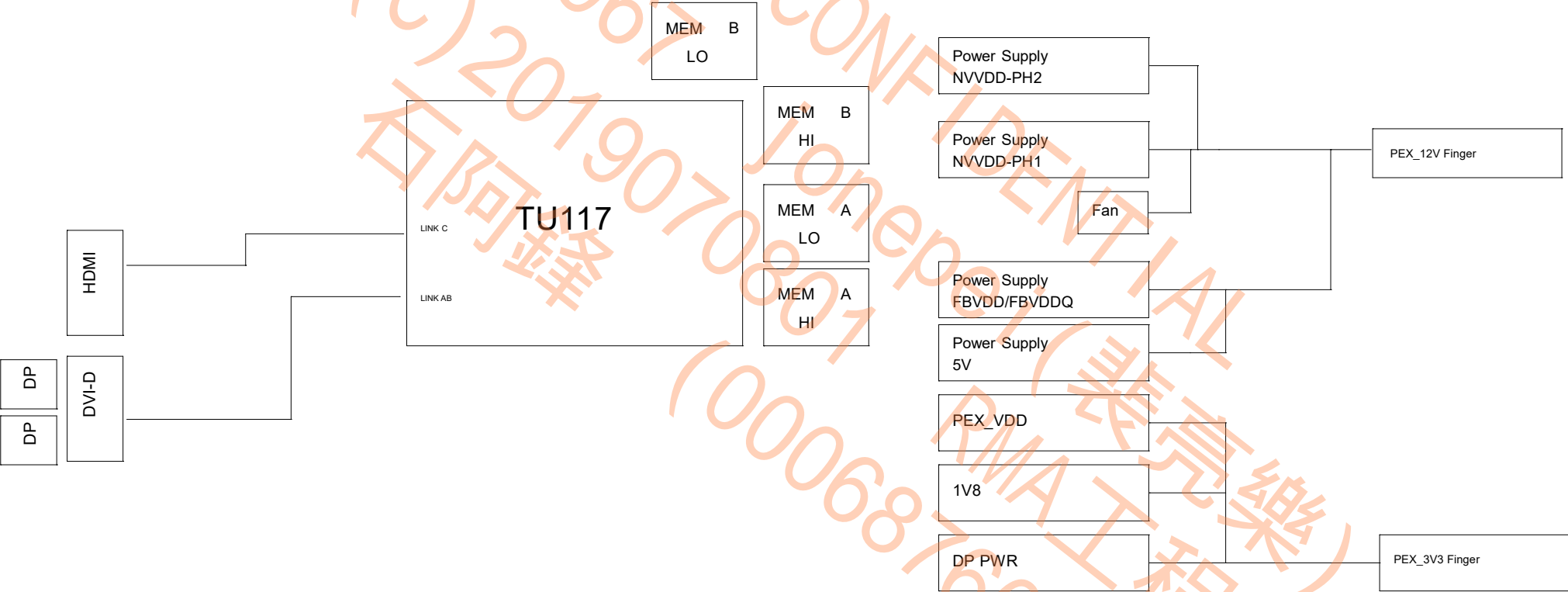
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DATE

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Block Diagram

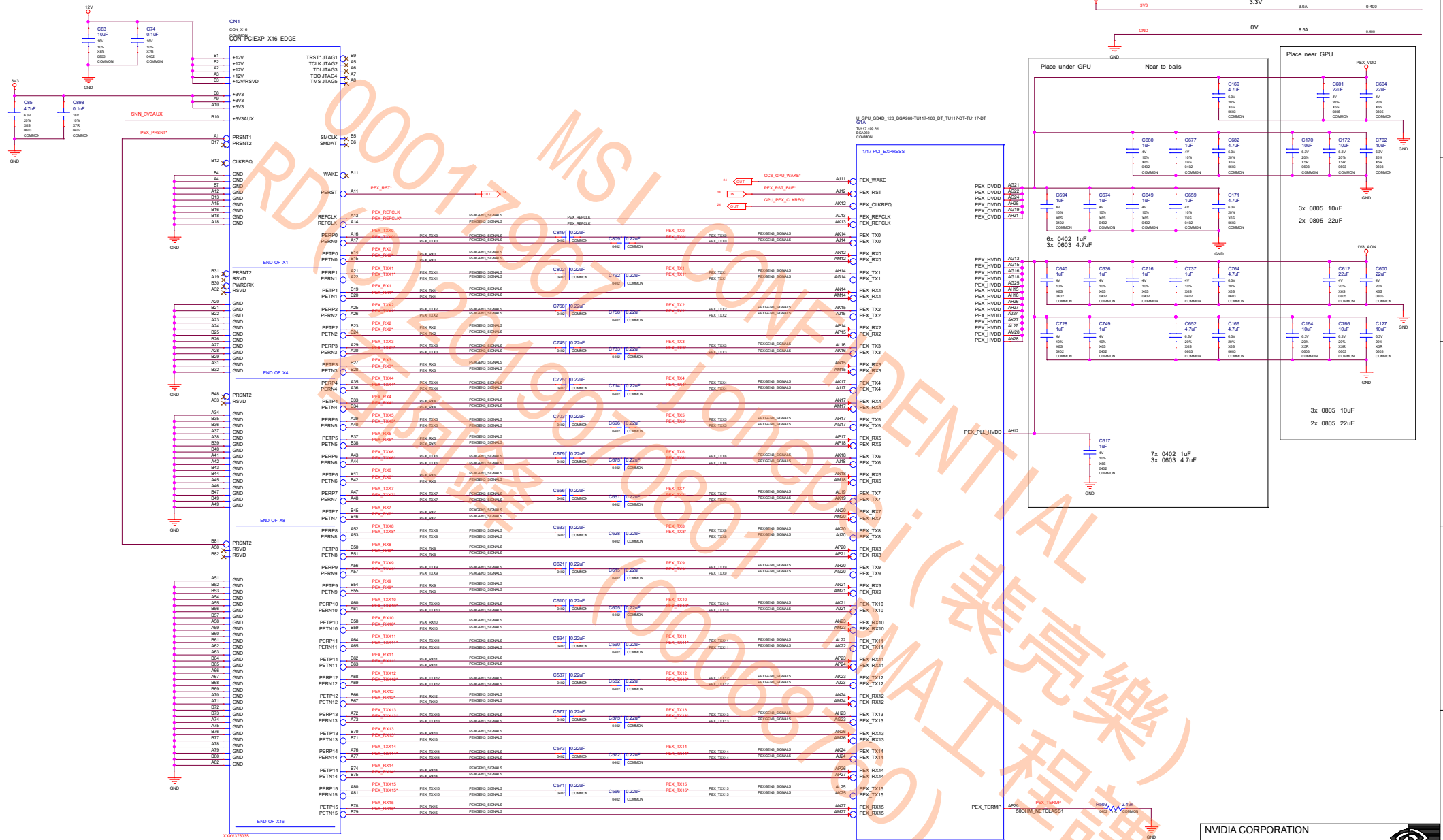


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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE: DETAIL	Block Diagram

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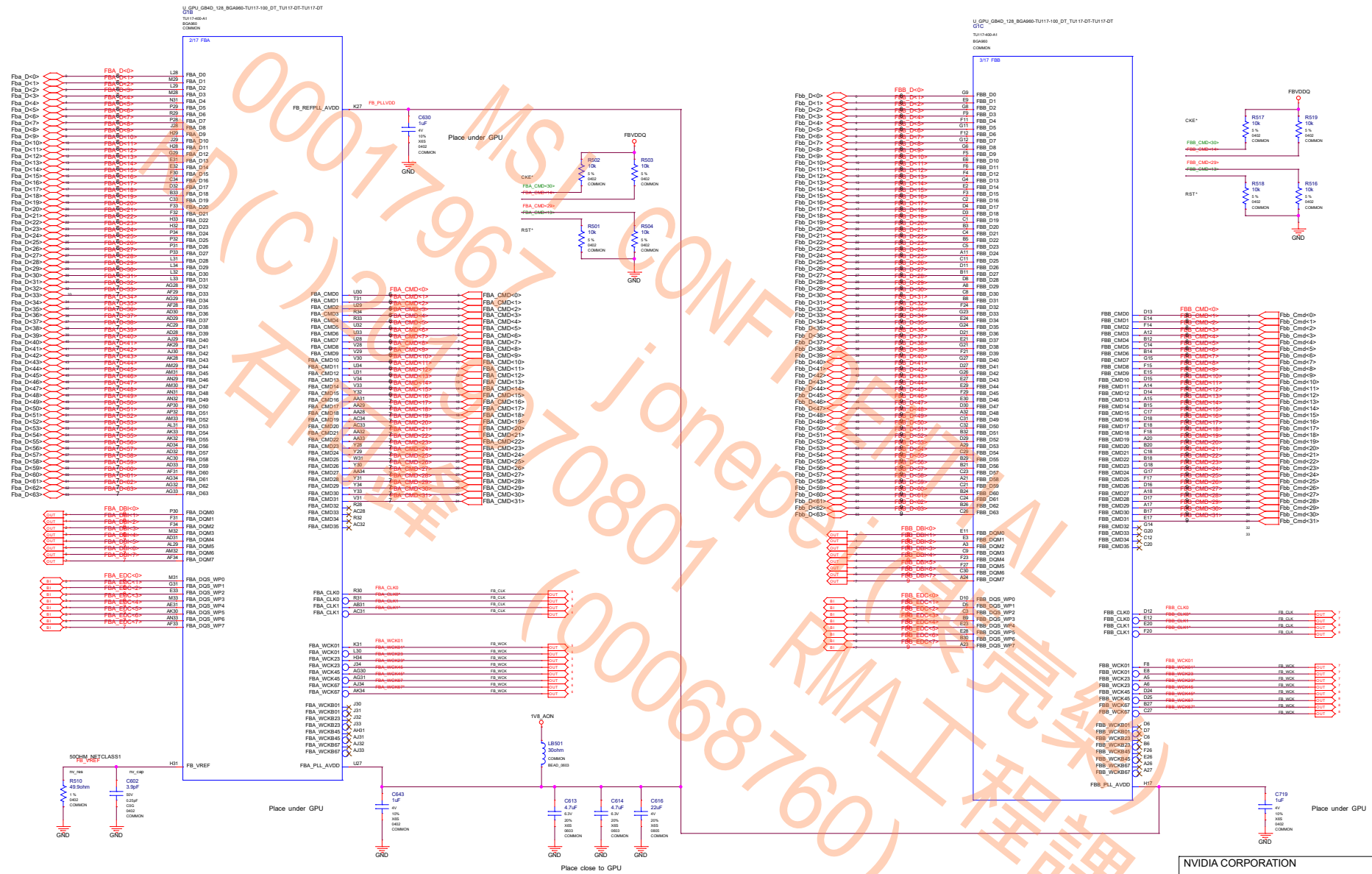
PCI Express



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MEMORY: GPU Partition A/B



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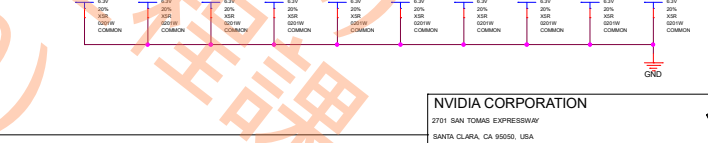
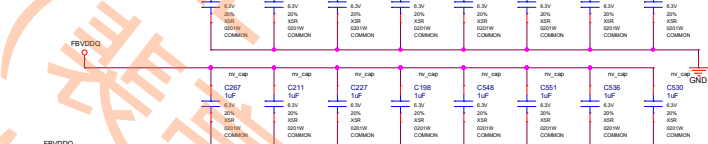
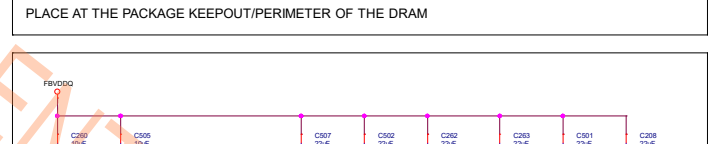
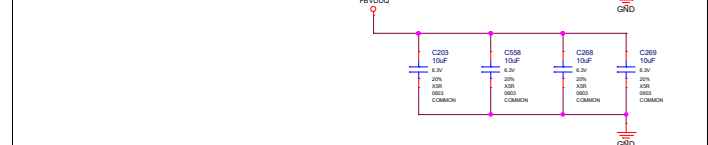
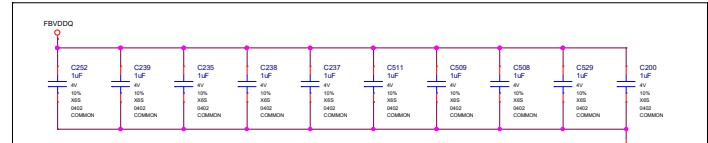
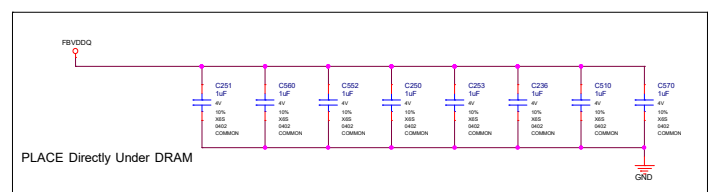
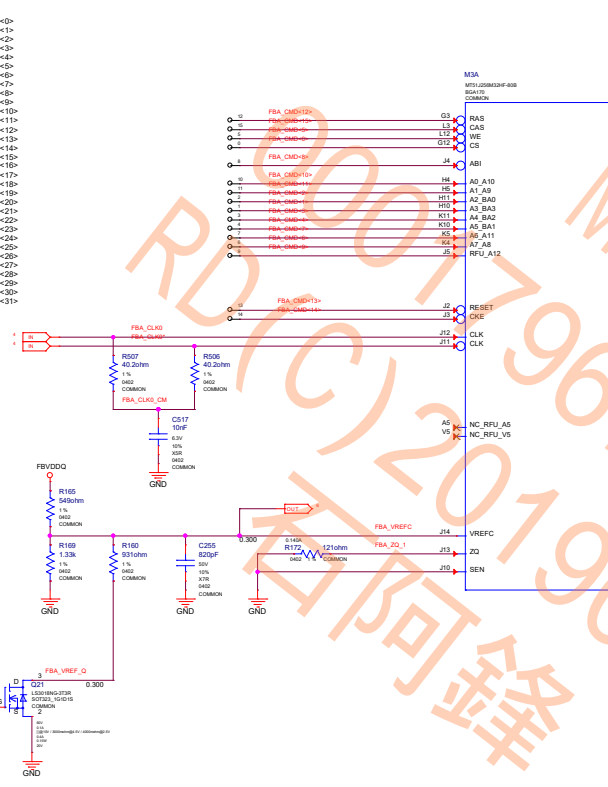
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FBA-CMD-0	FBA-CMD-0
R1: FBA-CMD-0	R1: FBA-CMD-0
R2: FBA-CMD-0	R2: FBA-CMD-0
R3: FBA-CMD-0	R3: FBA-CMD-0
R4: FBA-CMD-0	R4: FBA-CMD-0
R5: FBA-CMD-0	R5: FBA-CMD-0
R6: FBA-CMD-0	R6: FBA-CMD-0
R7: FBA-CMD-0	R7: FBA-CMD-0
R8: FBA-CMD-0	R8: FBA-CMD-0
R9: FBA-CMD-0	R9: FBA-CMD-0
R10: FBA-CMD-0	R10: FBA-CMD-0
R11: FBA-CMD-0	R11: FBA-CMD-0
R12: FBA-CMD-0	R12: FBA-CMD-0
R13: FBA-CMD-0	R13: FBA-CMD-0
R14: FBA-CMD-0	R14: FBA-CMD-0
R15: FBA-CMD-0	R15: FBA-CMD-0
R16: FBA-CMD-0	R16: FBA-CMD-0
R17: FBA-CMD-0	R17: FBA-CMD-0
R18: FBA-CMD-0	R18: FBA-CMD-0
R19: FBA-CMD-0	R19: FBA-CMD-0
R20: FBA-CMD-0	R20: FBA-CMD-0

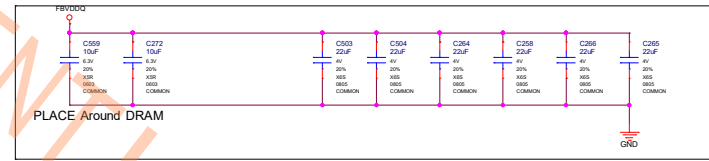
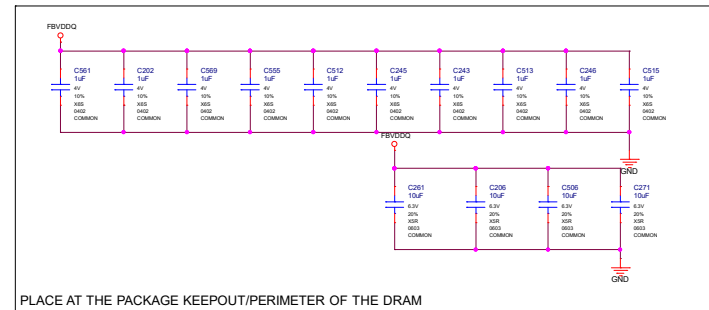
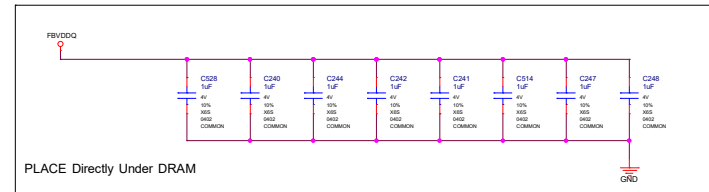
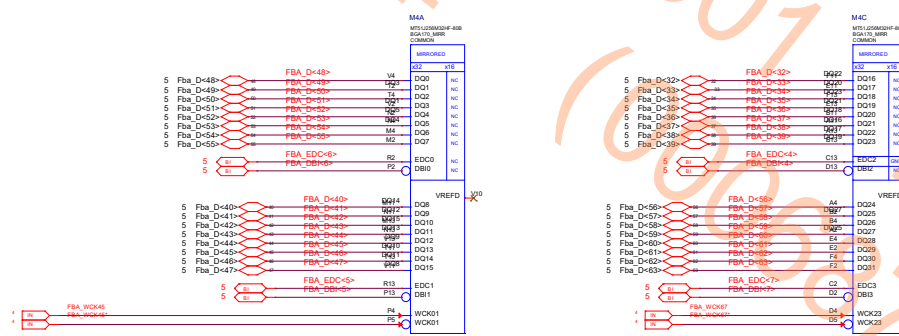
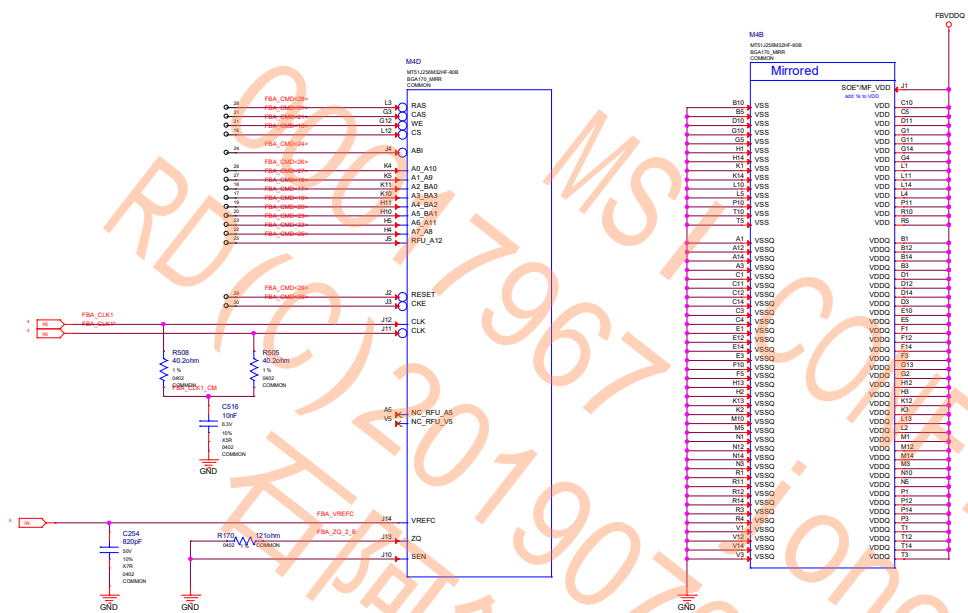
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CMD1	A3, BA3	
CMD2	A2, BA0	
CMD3	A4, BA2	
CMD4	A5, BA1	
CMD5	WE*	
CMD6	A7, AB	
CMD7	AE, A11	
CMD8	AB*	
CMD9	A12, RFU	
CMD10	AE, A10	
CMD11	A1, AB	
CMD12	RA5*	
CMD13	RS1*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3, BA3
CMD18		A2, BA0
CMD19		A4, BA2
CMD20		AE, BA1
CMD21		WE*
CMD22		A7, AB
CMD23		AE, A11
CMD24		A12, RFU
CMD25		AE, A10
CMD26		RA5*
CMD27		RS1*
CMD28		CKE*
CMD29		CAS*
CMD30		
CMD31		

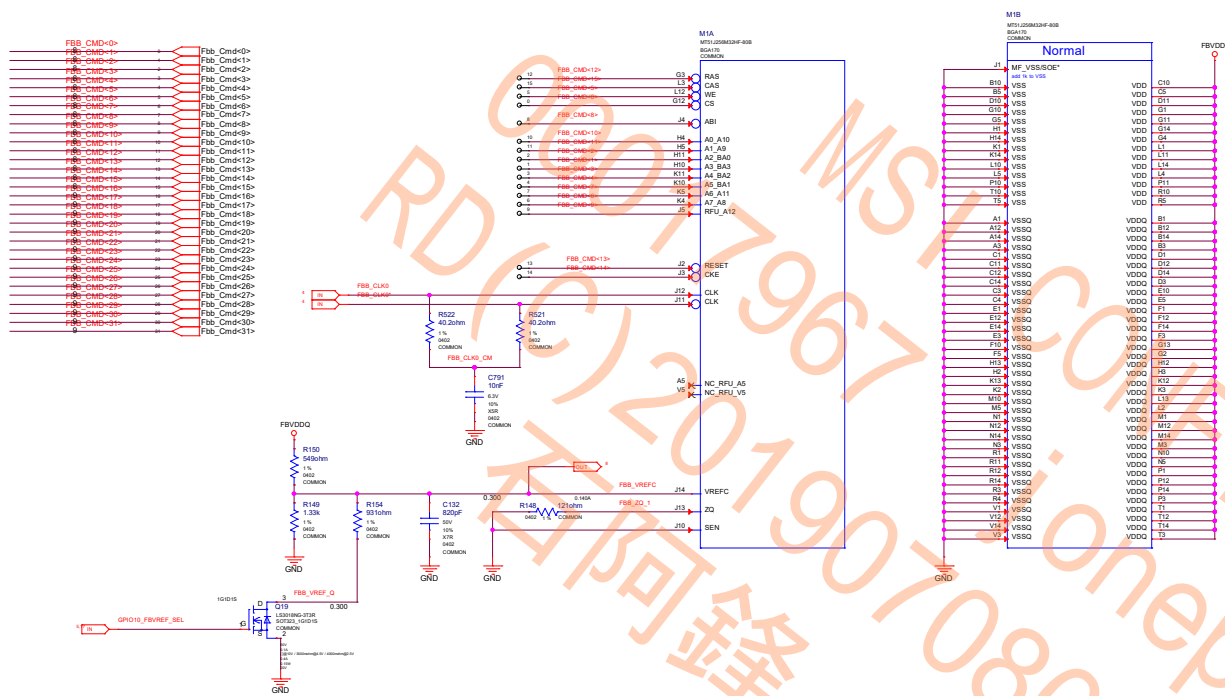


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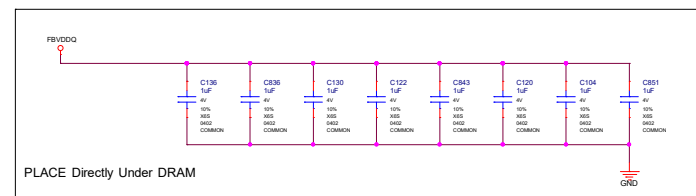
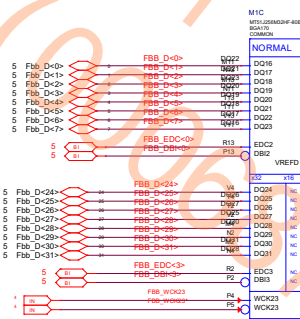
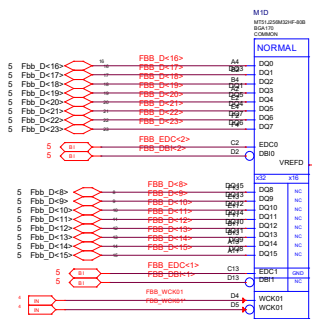
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CMD	0..31	32..63
CMD0	CS*	
CMD1	A3, BA3	
CMD2	A2, BA2	
CMD3	AE, BA1	
CMD4	WC5	
CMD5	AT, AB	
CMD7	AI, A11	
CMD8	AB*	
CMD9	AI2, RFU	
CMD10	AG, A10	
CMD11	A1, AB	
CMD12	RA5*	
CMD13	RB3*	
CMD14	OK*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3, BA3
CMD18		A2, BA2
CMD19		AE, BA1
CMD20		WC5
CMD21		AT, AB
CMD22		AI, A11
CMD23		AB*
CMD24		AI2, RFU
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CMD29		CAS*
CMD30		
CMD31		

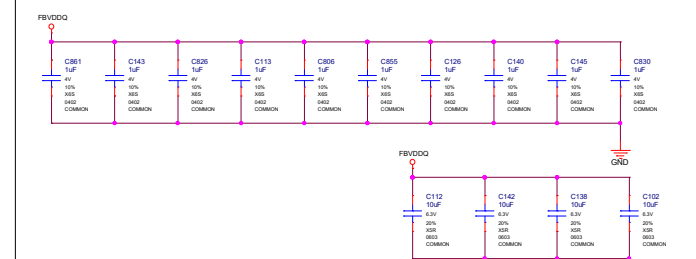




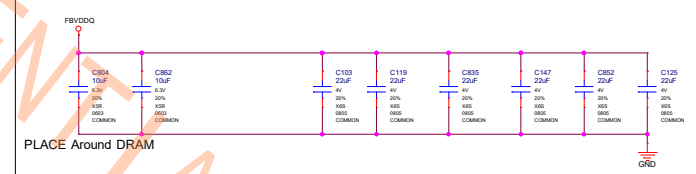
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CMD1	A3, BA0	
CMD2	A2, BA0	
CMD3	A4, BA2	
CMD4	A5, BA1	
CMD5	WE*	
CMD6	A7, A8	
CMD7	A6, A11	
CMD8	AB*	
CMD9	A10, RFU	
CMD10	A0, A10	
CMD11	A1, A9	
CMD12	RA*	
CMD13	RS*	
CMD14	CK*	
CMD15	CAS*	
CMD16		
CMD17		
CMD18	A3, BA3	
CMD19	A2, BA0	
CMD20	A4, BA2	
CMD21	A5, BA1	
CMD22	WE*	
CMD23	A7, A8	
CMD24	A6, A11	
CMD25	AB*	
CMD26	A10, RFU	
CMD27	A0, A10	
CMD28	A1, A9	
CMD29	RA*	
CMD30	RS*	
CMD31	CK*	



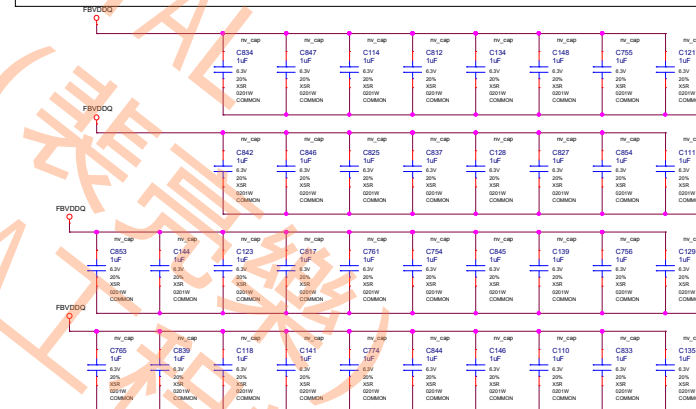
PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPUT/PERIMETER OF THE DRAM



PLACE Around DRAM



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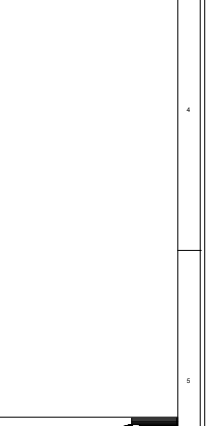
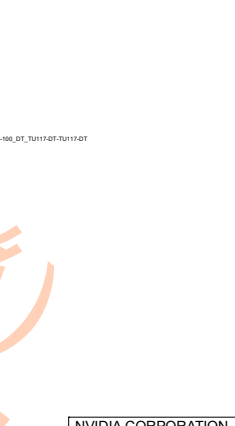
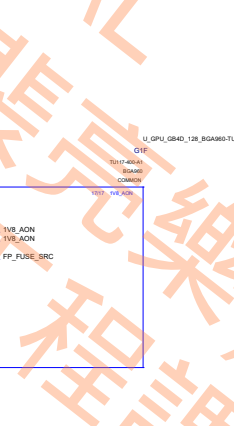
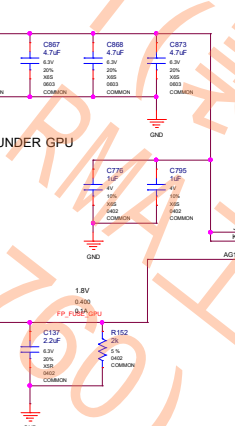
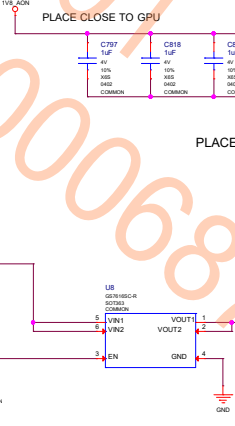
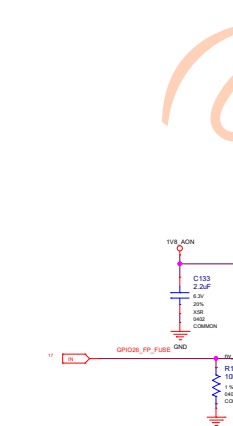
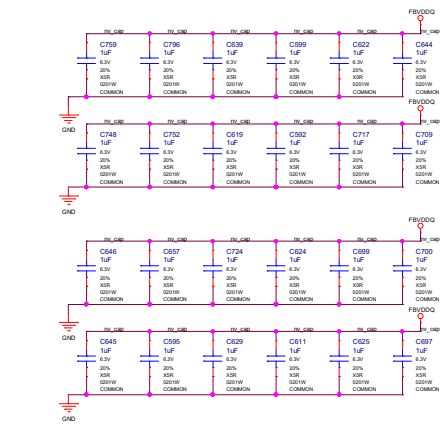
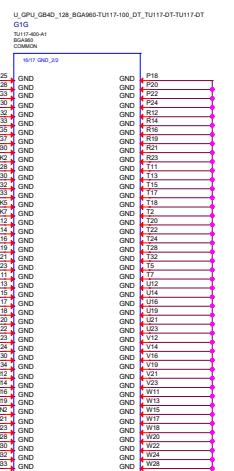
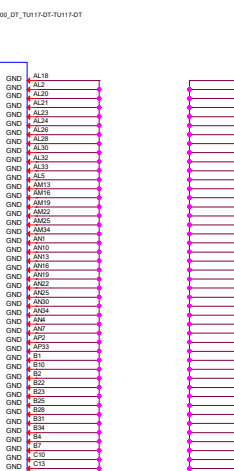
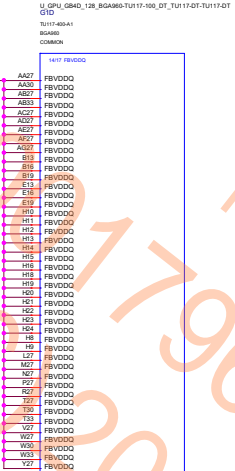
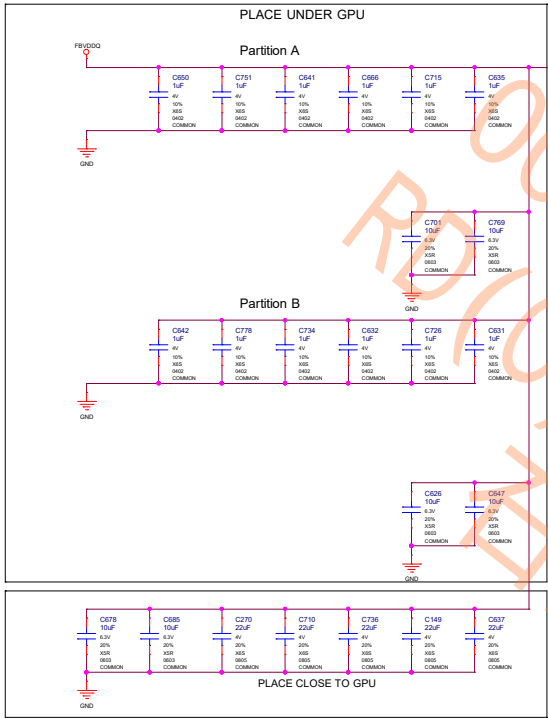


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GPU FBVDDQ & 1V8 Decoupling

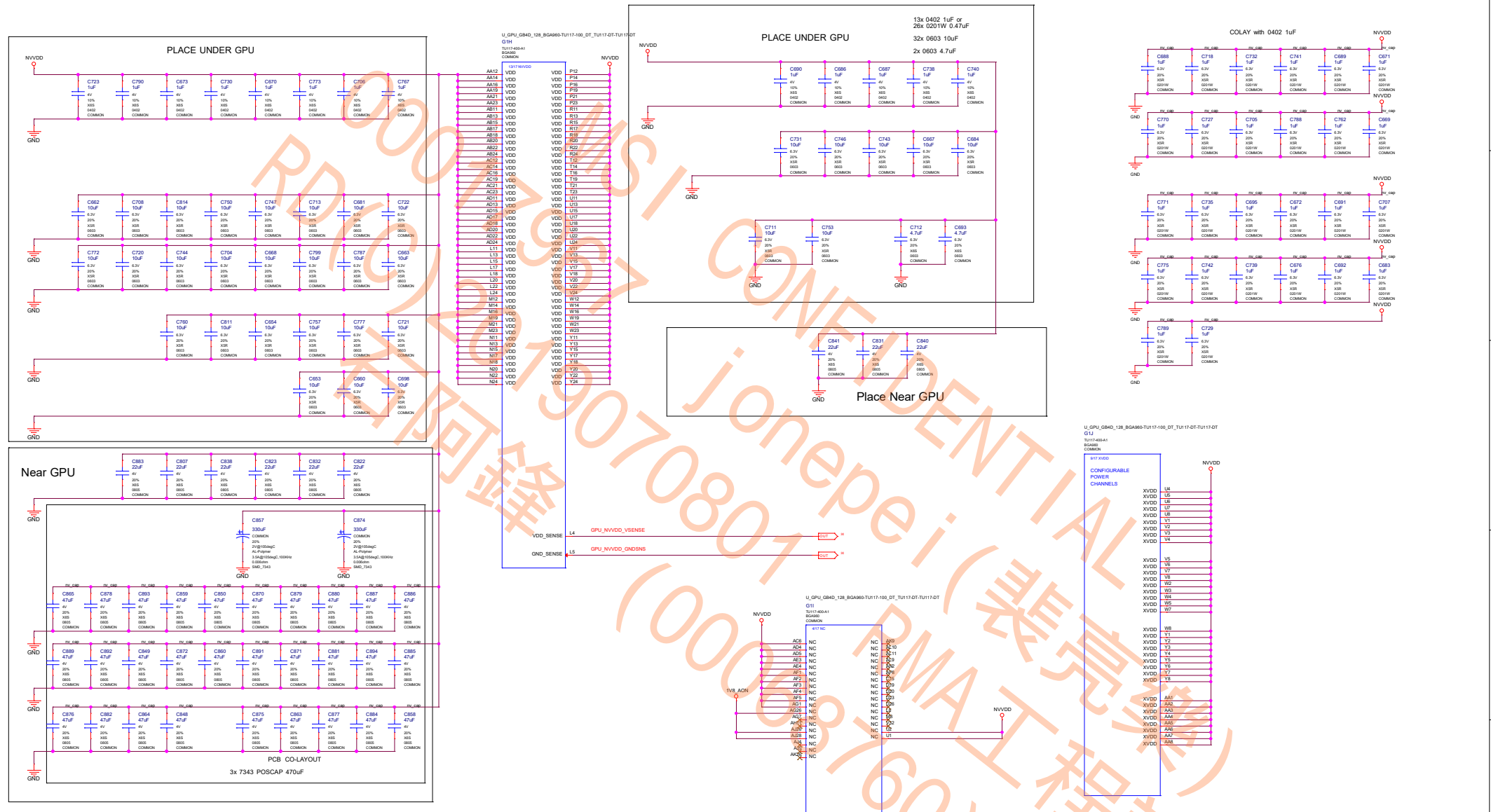


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GPU NVVDD Decoupling



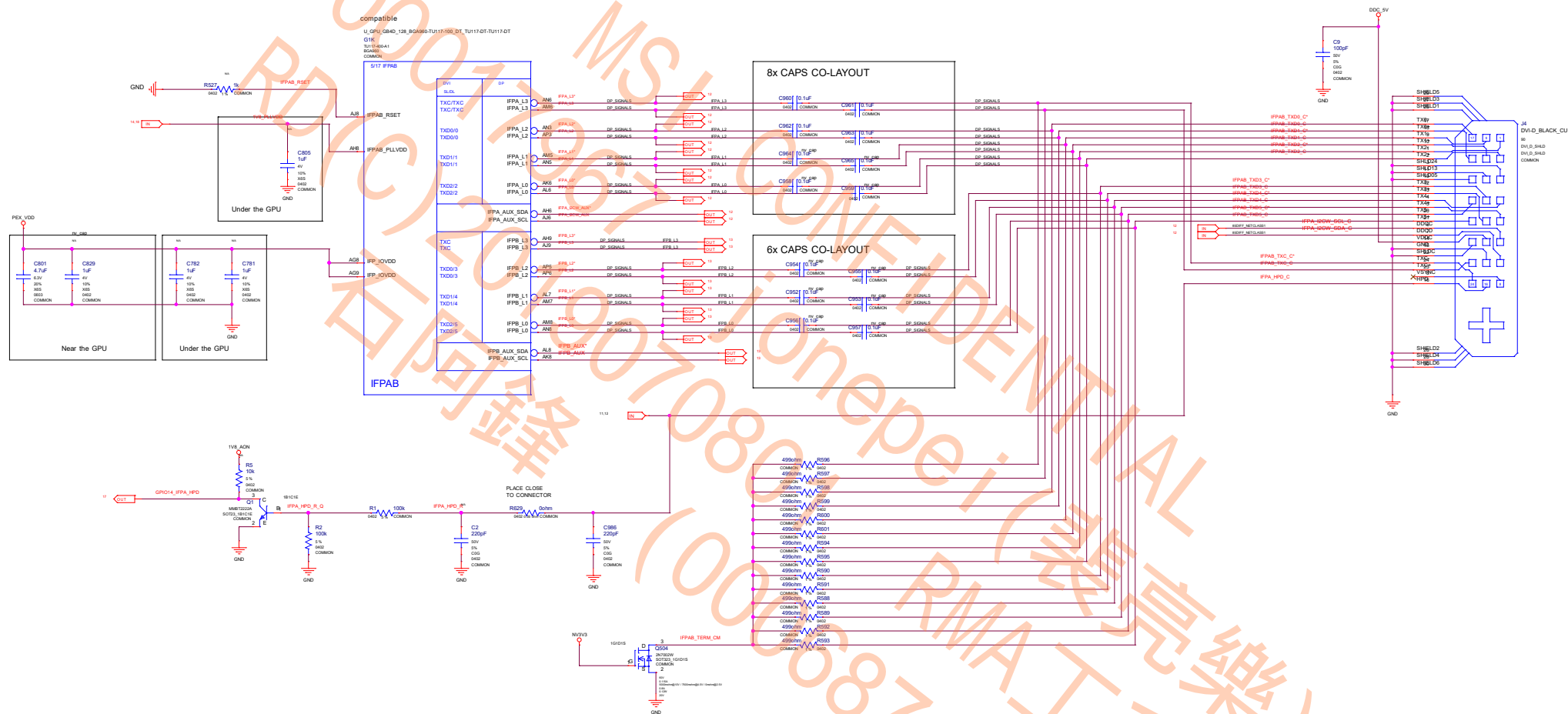
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IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPAB DVI-DL

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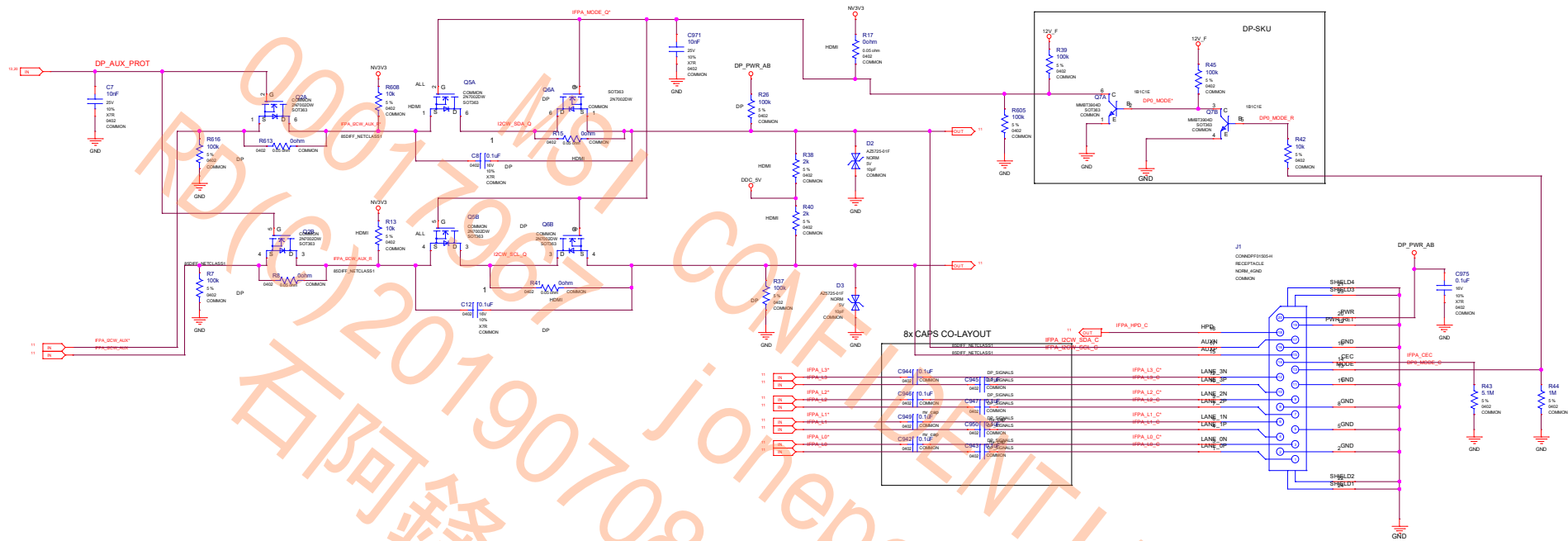
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BOM REV

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IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPA DP

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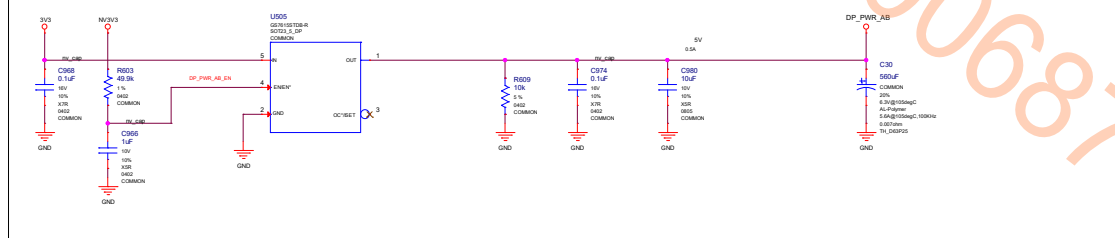
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Page13: IFPB DP



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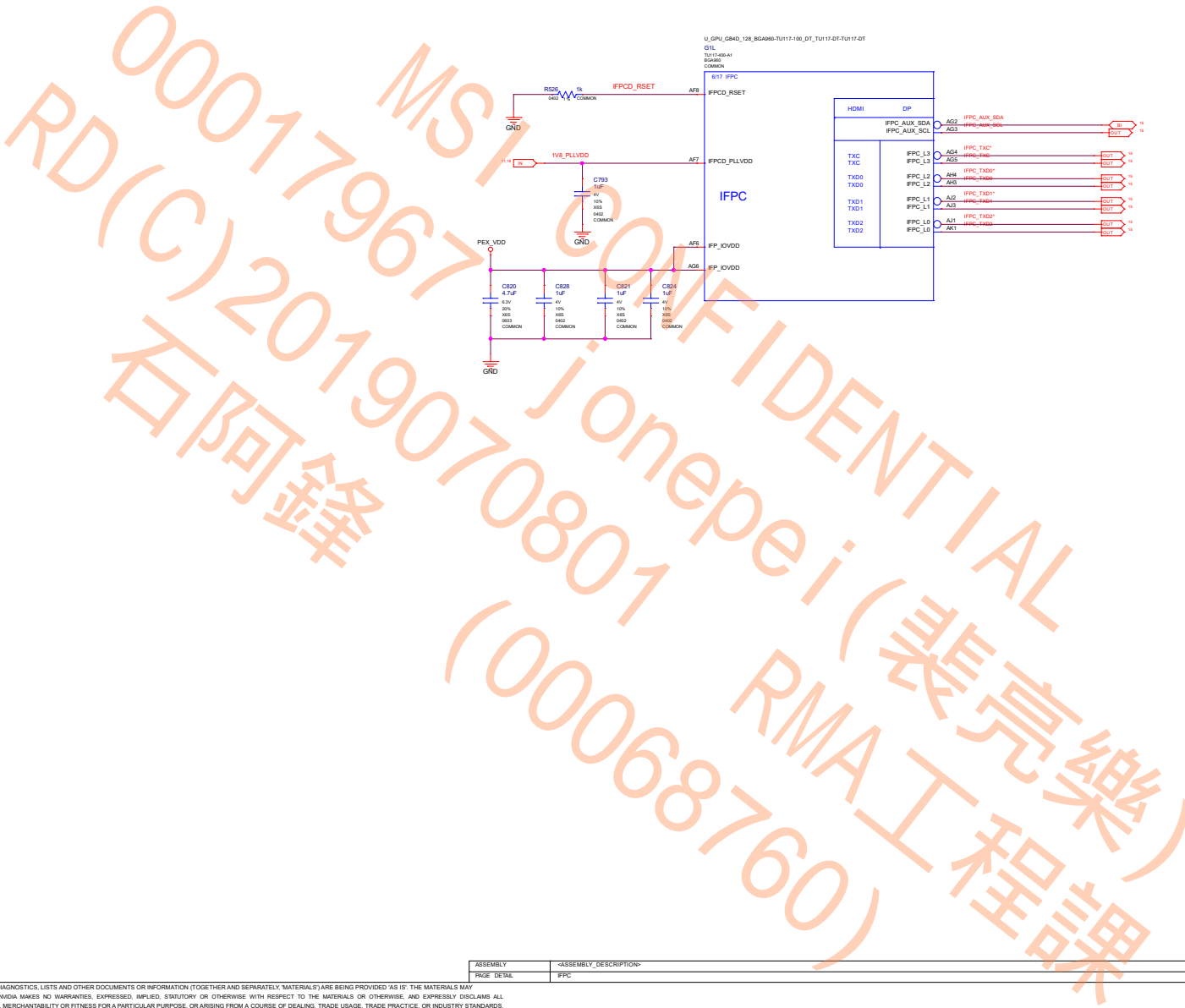
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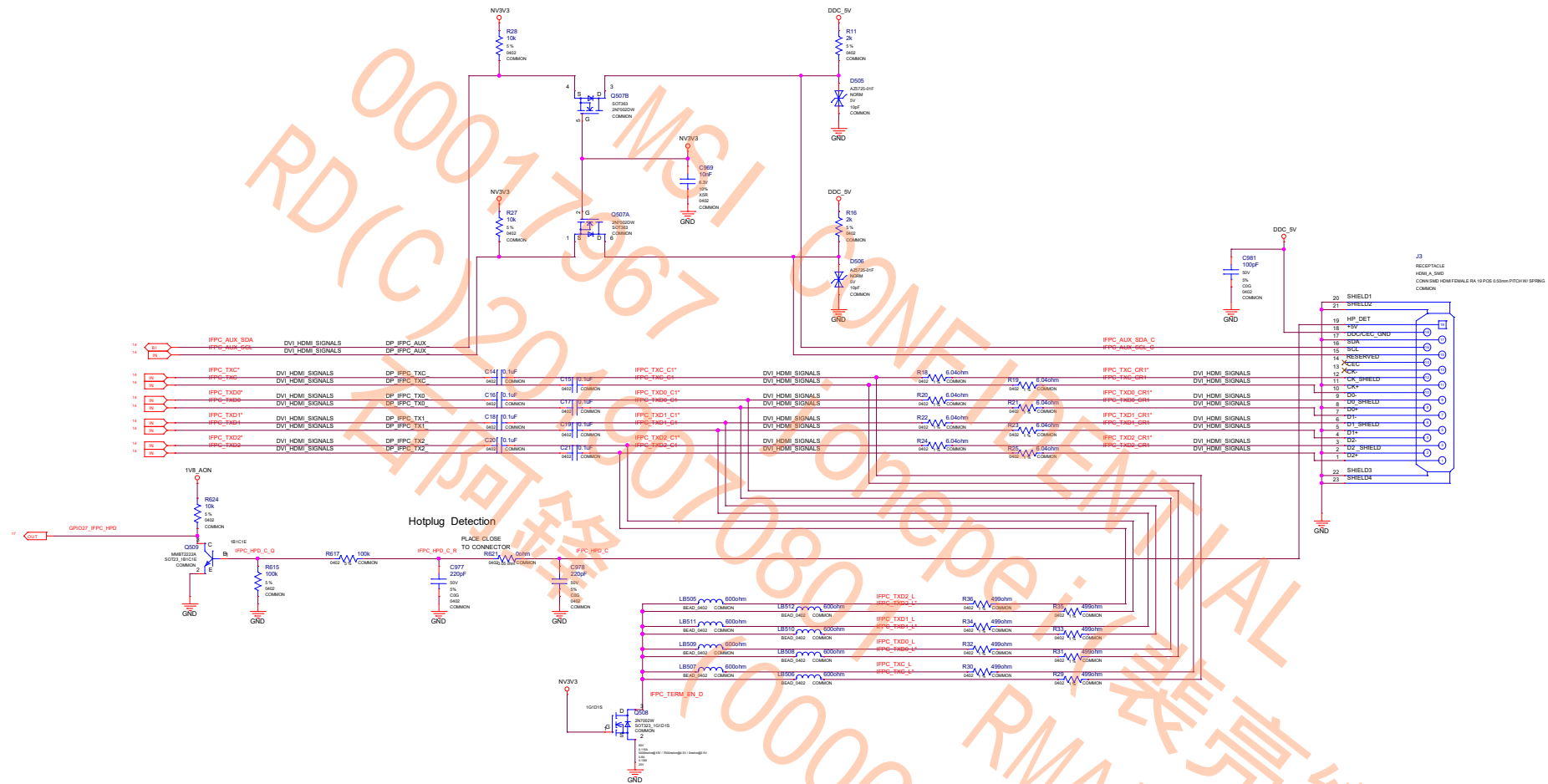
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IFPC HDMI



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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	IFPC HDMI

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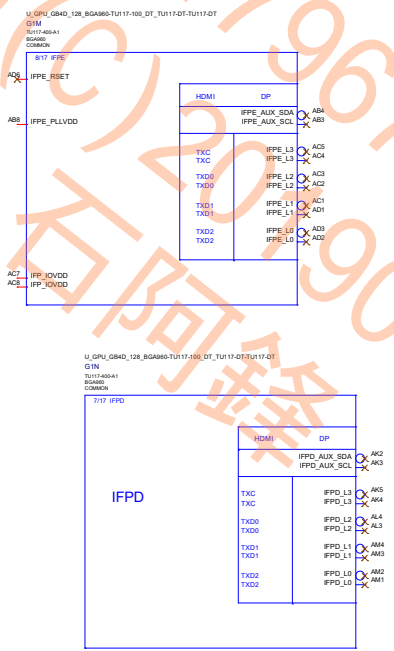


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IFPDEF UNUSED

00017967 MSI RD(C) 9070801 jonepei (00068760) CONFIDENTIAL RMA工程課 (裴亮樂)

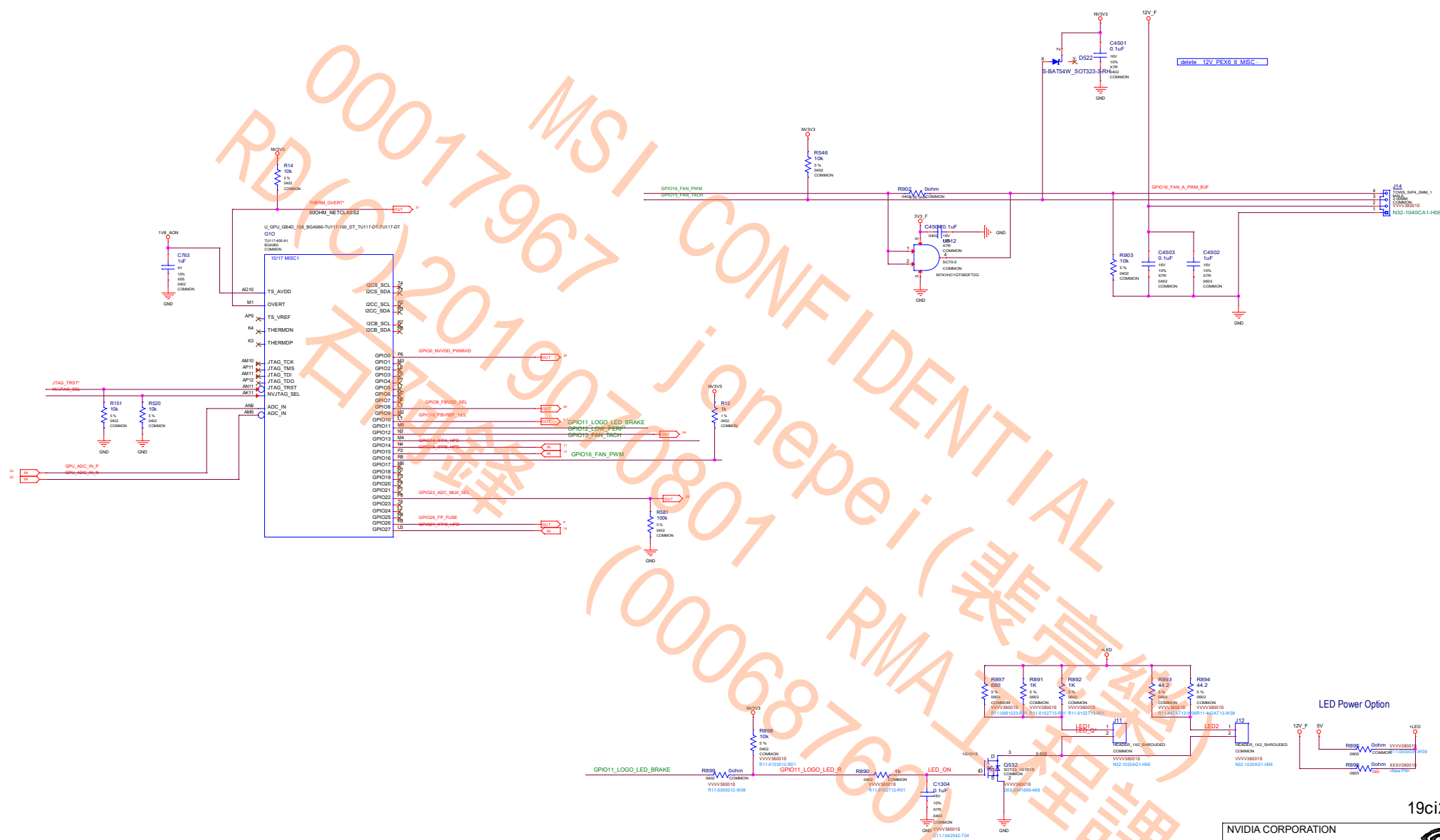


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MISC1: GPIO, Fan, Thermal, JTAG



19ci203



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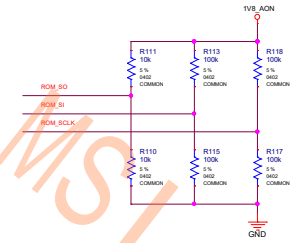
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PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GP

MISC2: ROM, XTAL, Straps

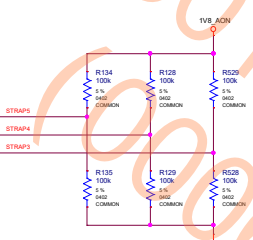
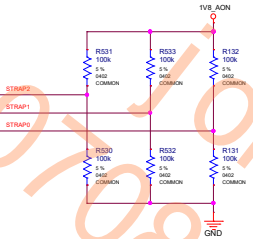
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	xxx1	FS_OVERT ENABLE	Default
L	L	M	xxx0	FS_OVERT DISABLE	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung 8Gb 256Mx32 K4G80325FC-HC25
L	L	H	0001	Micron 8Gb 256Mx32 MT51J256M32HF-80.B
L	H	L	0010	Hynix 8Gb 256Mx32 H5GC8H24AJR-R2C
L	H	H	0011	Hynix 8Gb 256Mx32 H5GQ8H24MJR-R4C
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

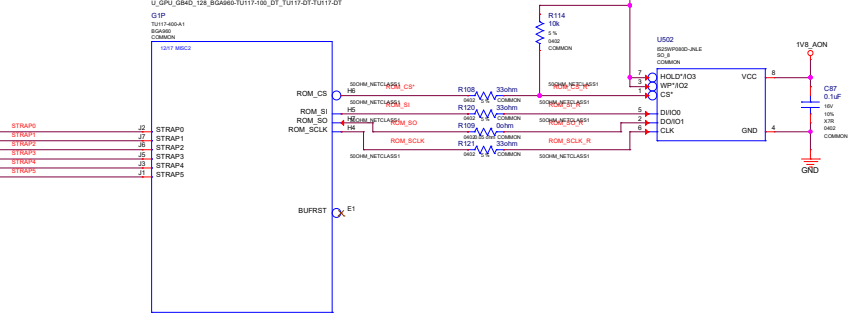


- 1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

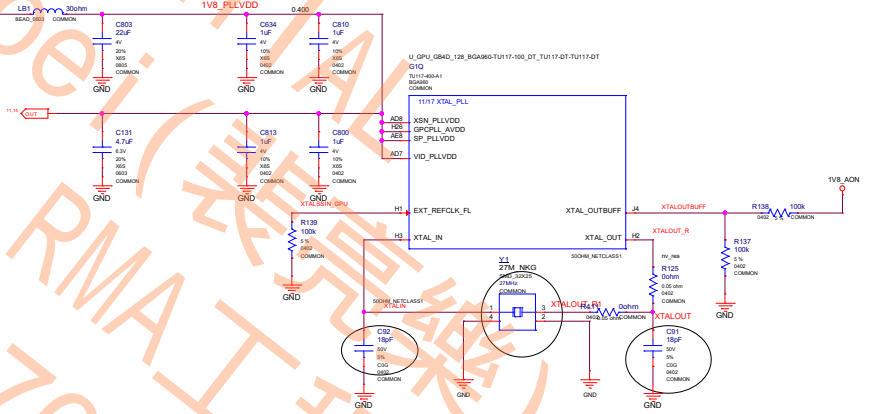
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



Smart Fan

XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



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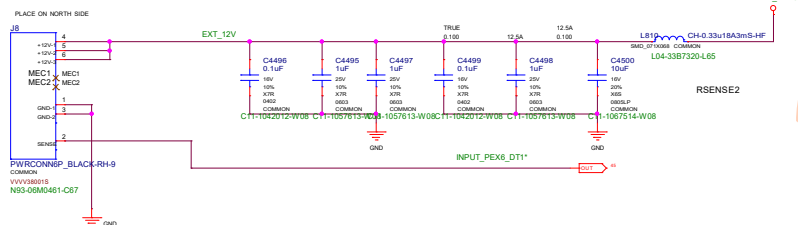
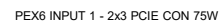
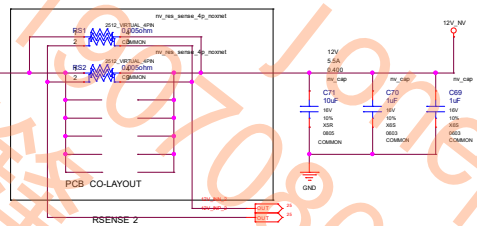
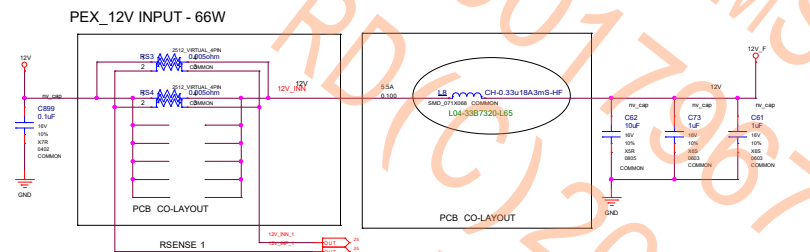
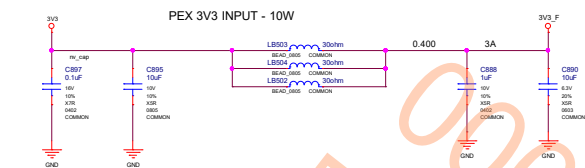
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE: DETAIL	MISC2: ROM, XTAL, Straps



Power Inputs and Filtering



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Power Inputs and Filtering

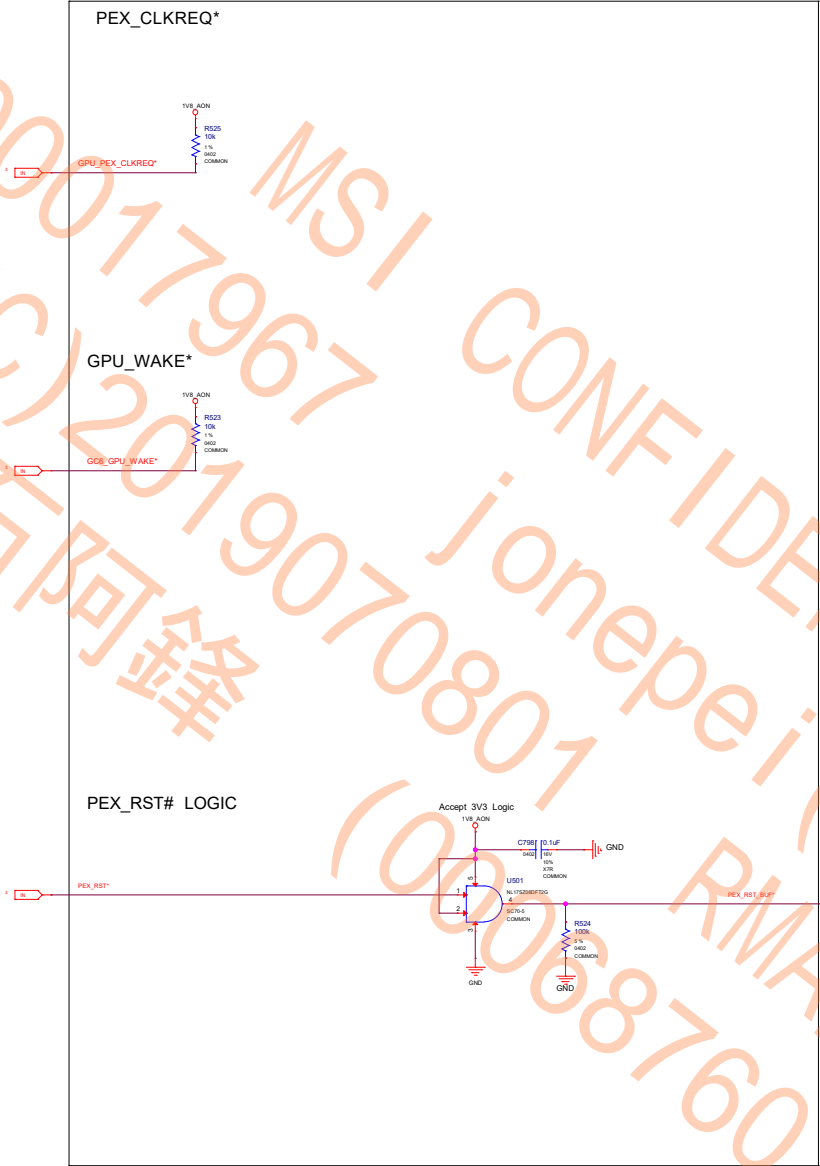
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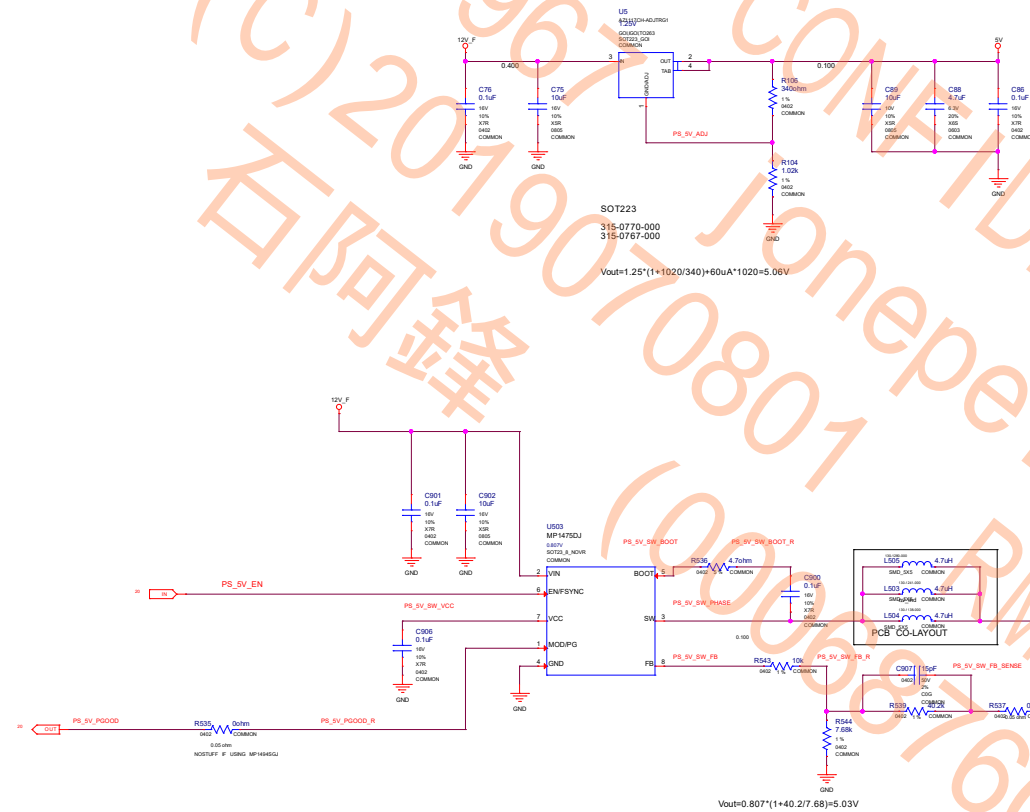


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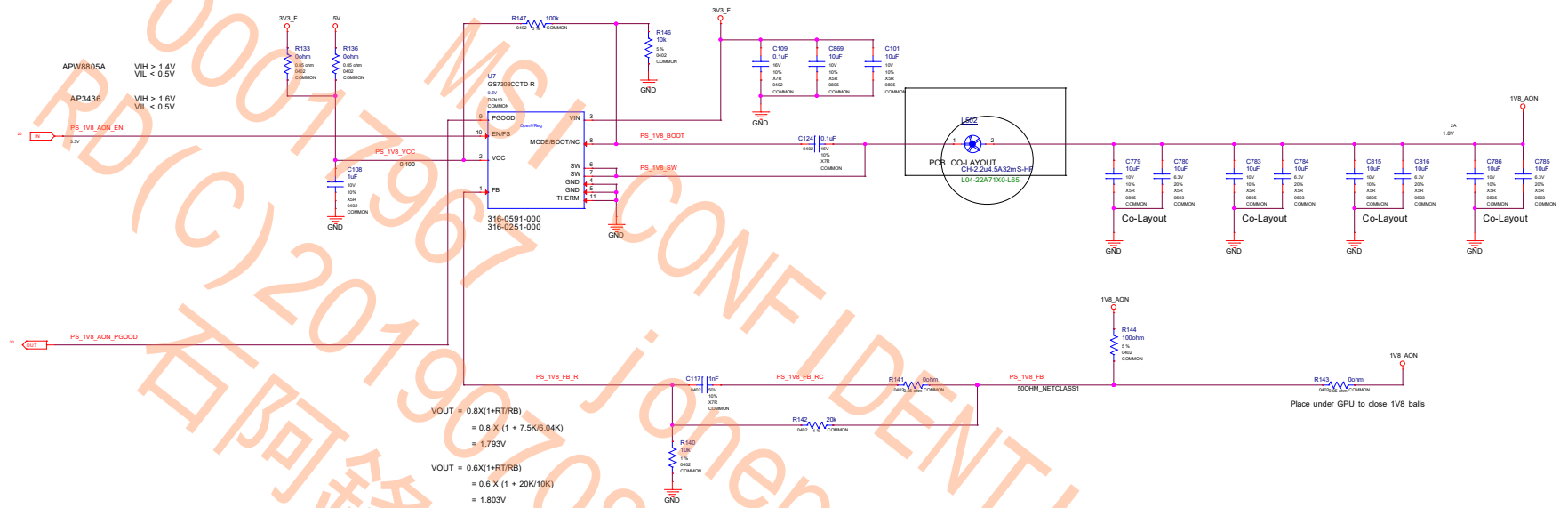


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PS: 1V8


$$\begin{aligned} V_{OUT} &= 0.8X(1+R_T/R_B) \\ &= 0.8 \times (1 + 7.5K/6.04K) \\ &= 1.793V \end{aligned}$$
$$\begin{aligned} V_{OUT} &= 0.6X(1+R_T/R_B) \\ &= 0.6 \times (1 + 20K/10K) \\ &= 1.803V \end{aligned}$$
$$\begin{aligned} V_{OUT} &= 0.6X(1+R_T/R_B) \\ &= 0.6 \times (1 + 20K/10K) \\ &= 1.803V \end{aligned}$$

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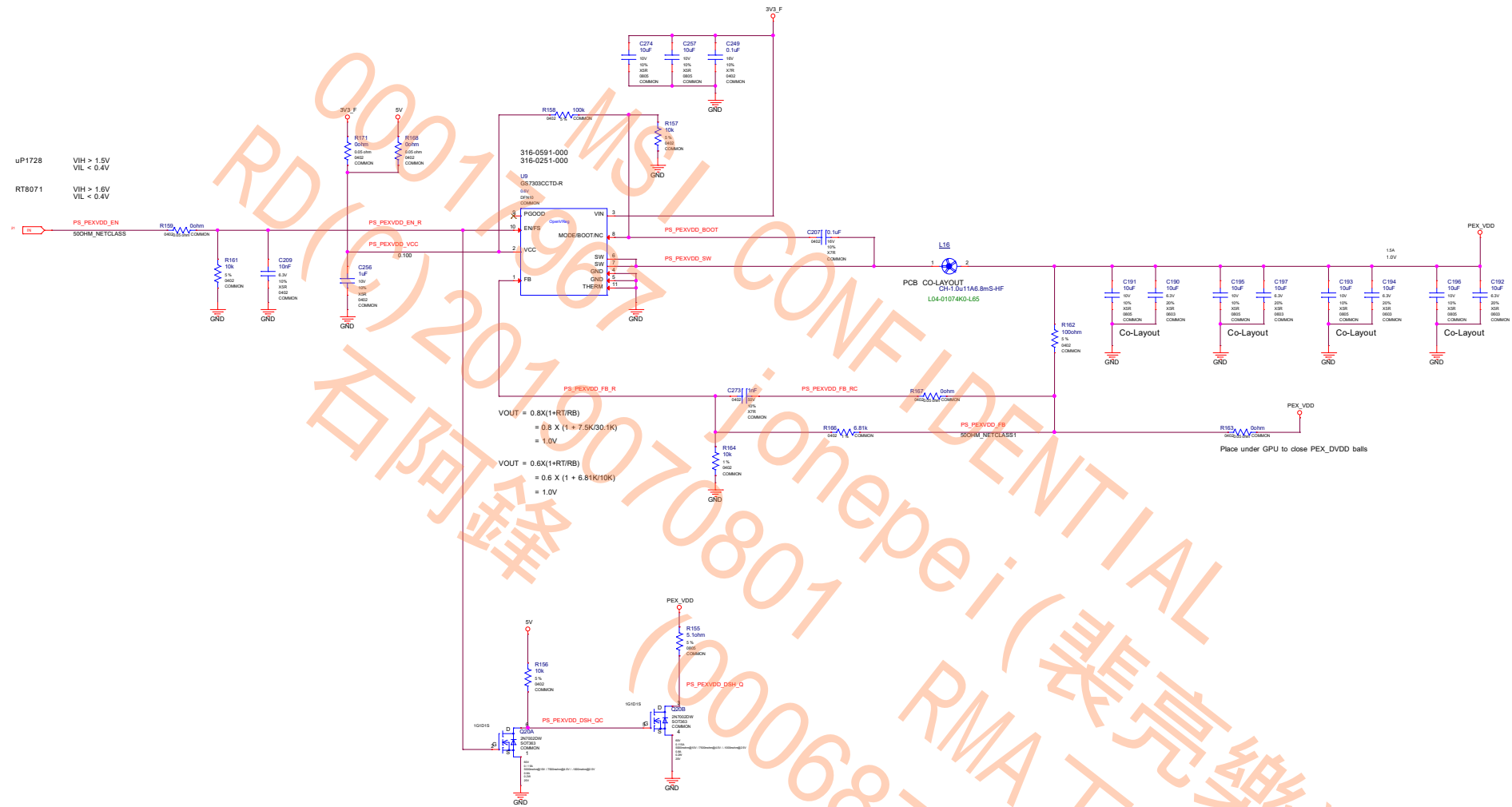
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PS: PEXVDD



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PAGE DETAIL	PS: PEXVDD

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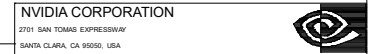
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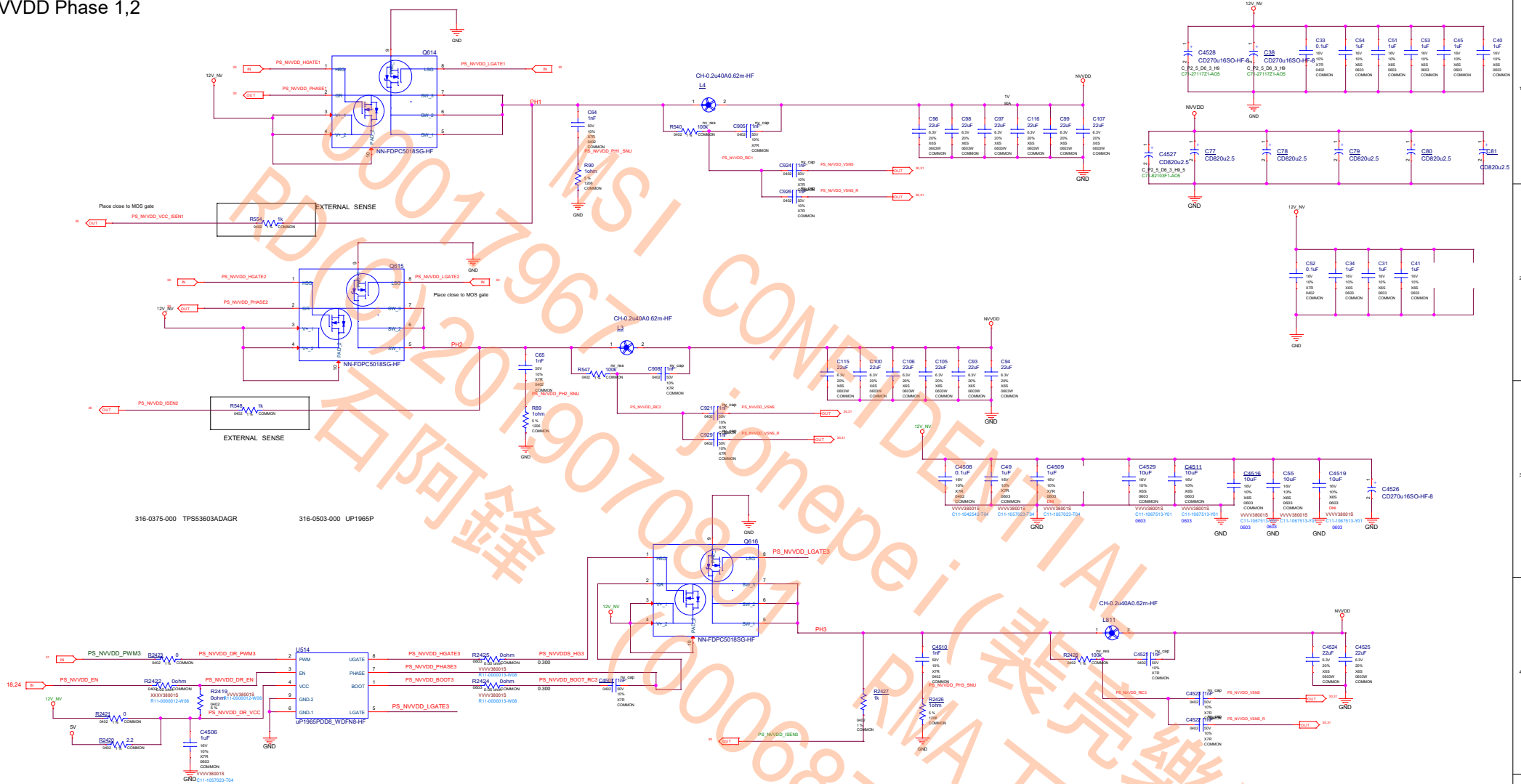
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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	PS: FBVDDQ

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PS: NVVDD Phase 1,2



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PAGE DETAIL	PS: NWC0 Phase 1,2

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Mechanical: Bracket/Thermal Solution

Brackets:

