

PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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Page	Description
51	SEQUENCE: MISC
52	LED & FAN HEADERS
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base on V372-02S change for D18 Z

1. P.23 remove SLI & BRIDGE_LED_VDD & SLI_BRG_PRST*

2. P.52 remove LED change FAN connector

3. P.53 remove LED

4. P.38&44 add FUSE

5. P.5~14 mem add <>

6. P.53 LED use V336-0D

7. P.32 remove

8. P.35~38 dual MOS

9. P.33 change dual MOS

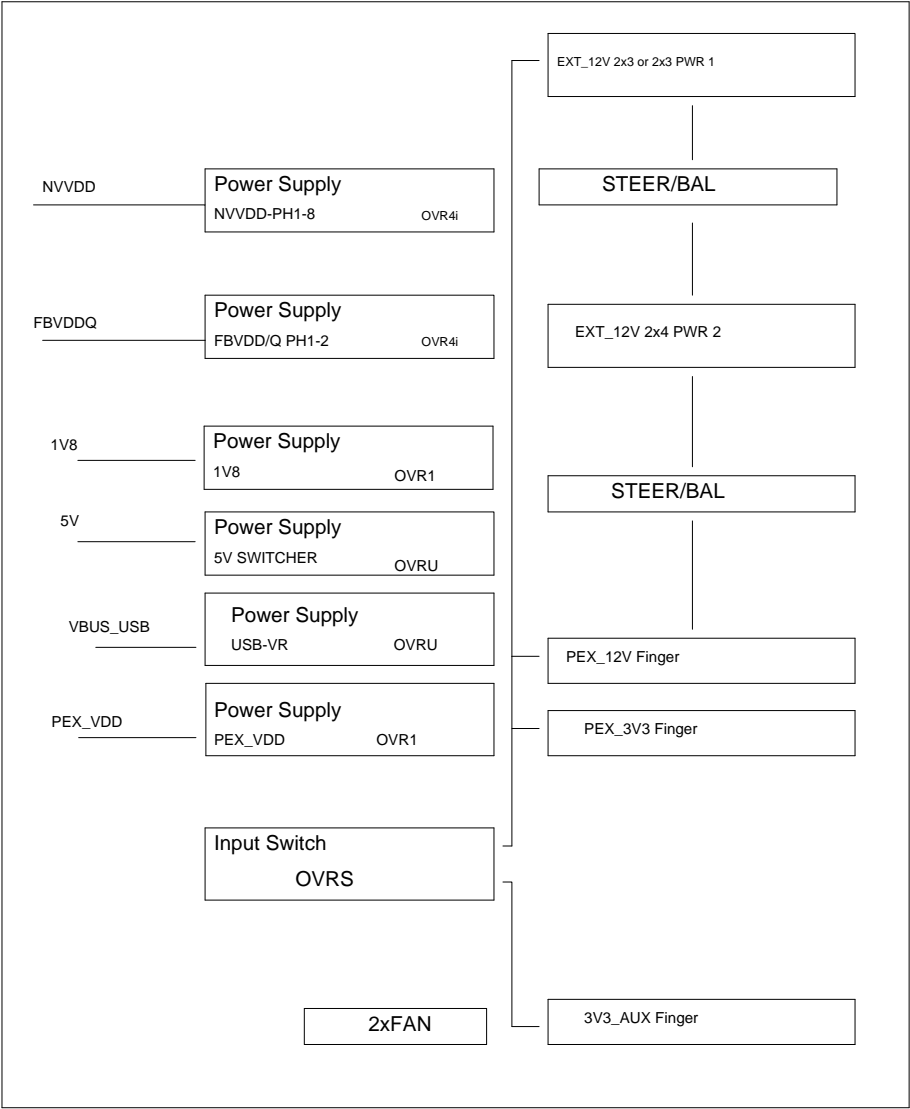
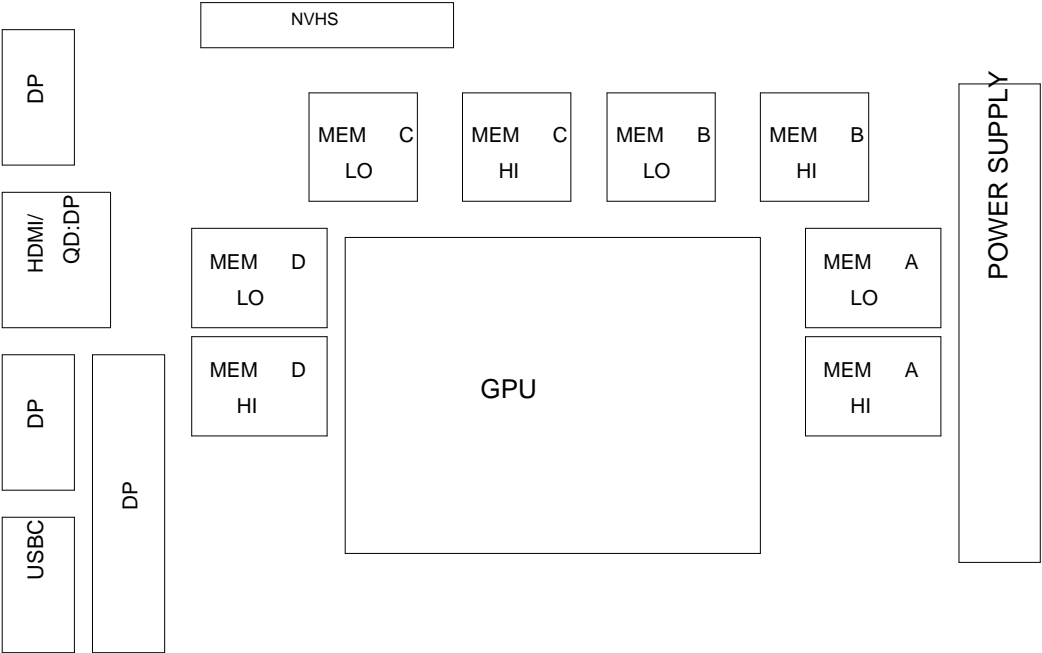
10. P.43 remove

11. P.31 change to UP1666

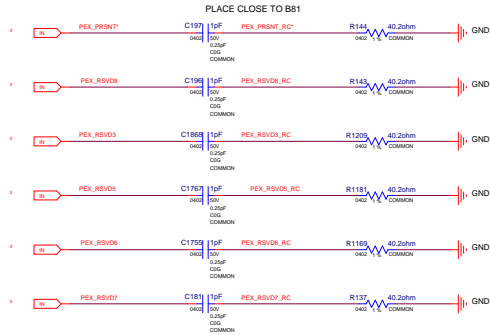
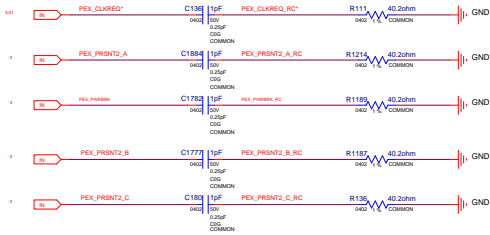
12. P.21 remove colay DP

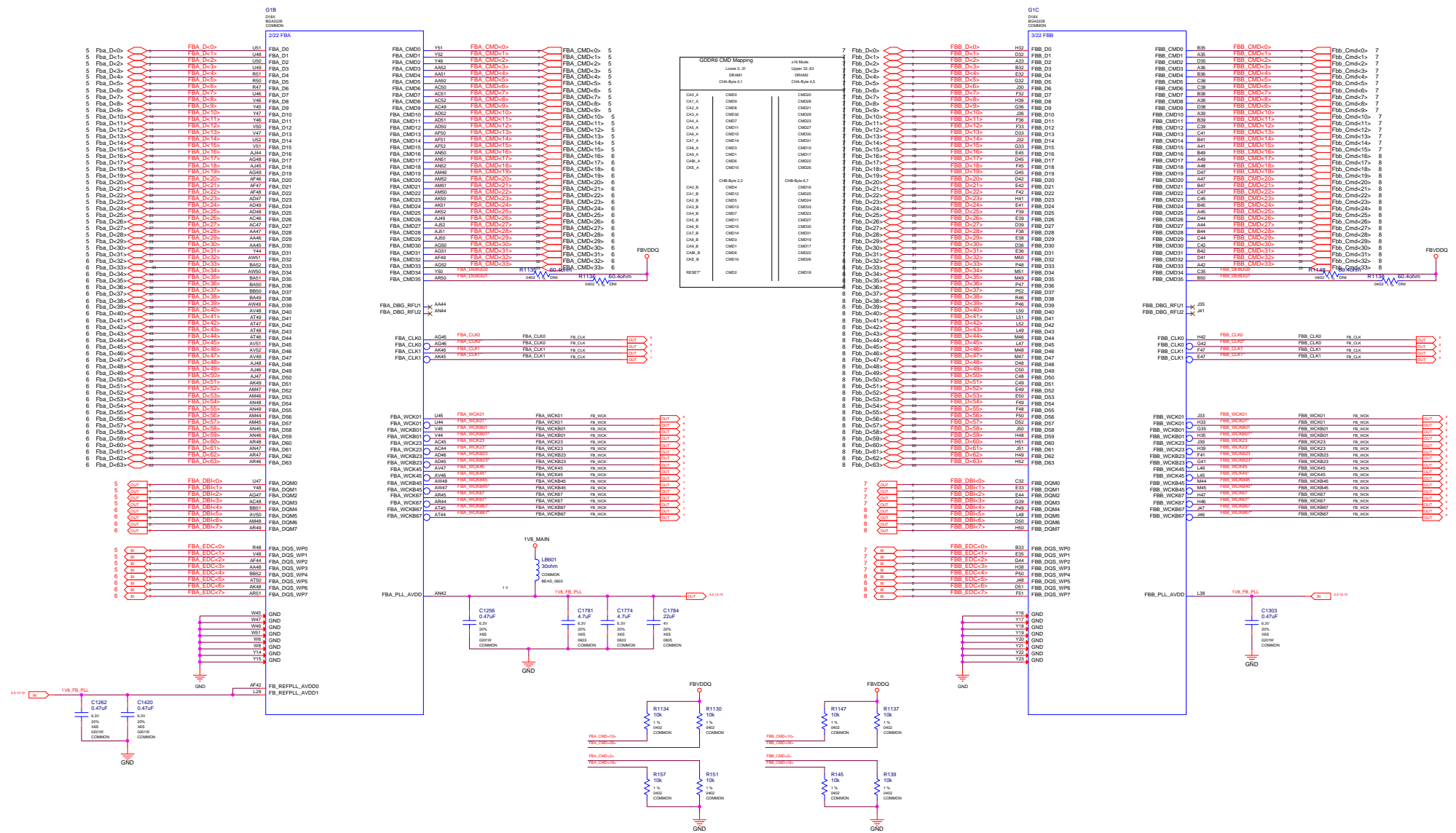
2019/06/17

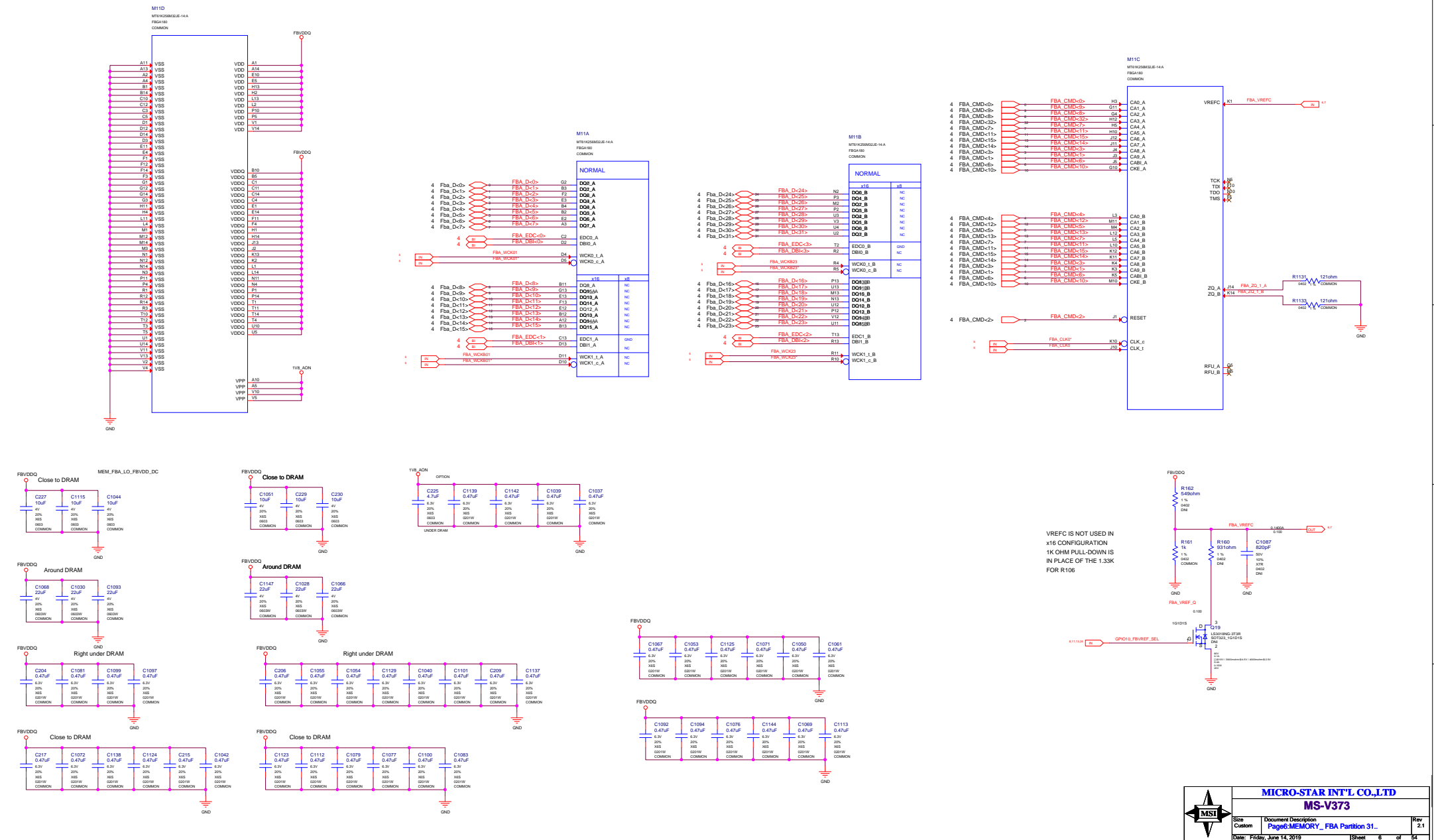
1.add NV link

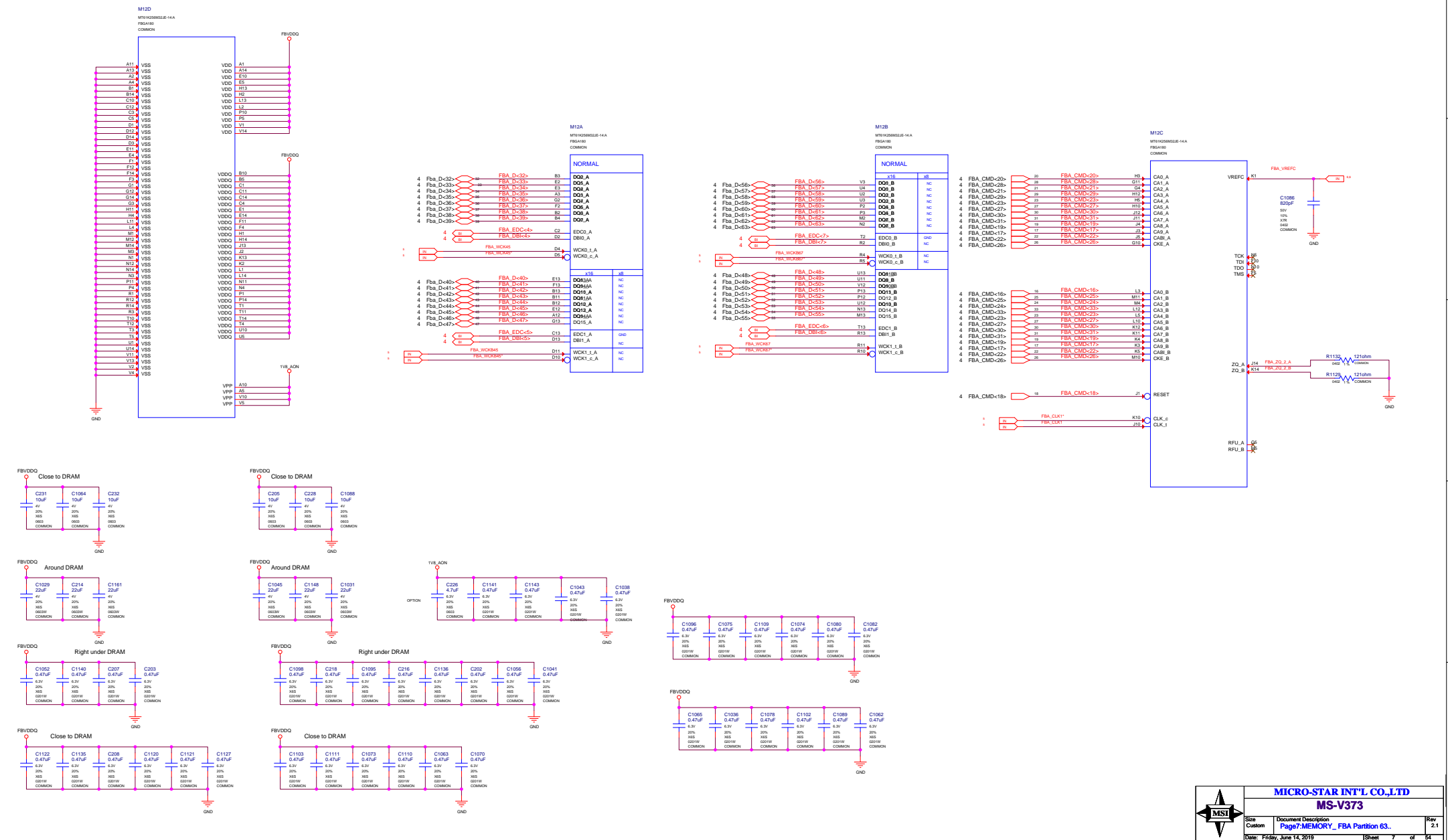


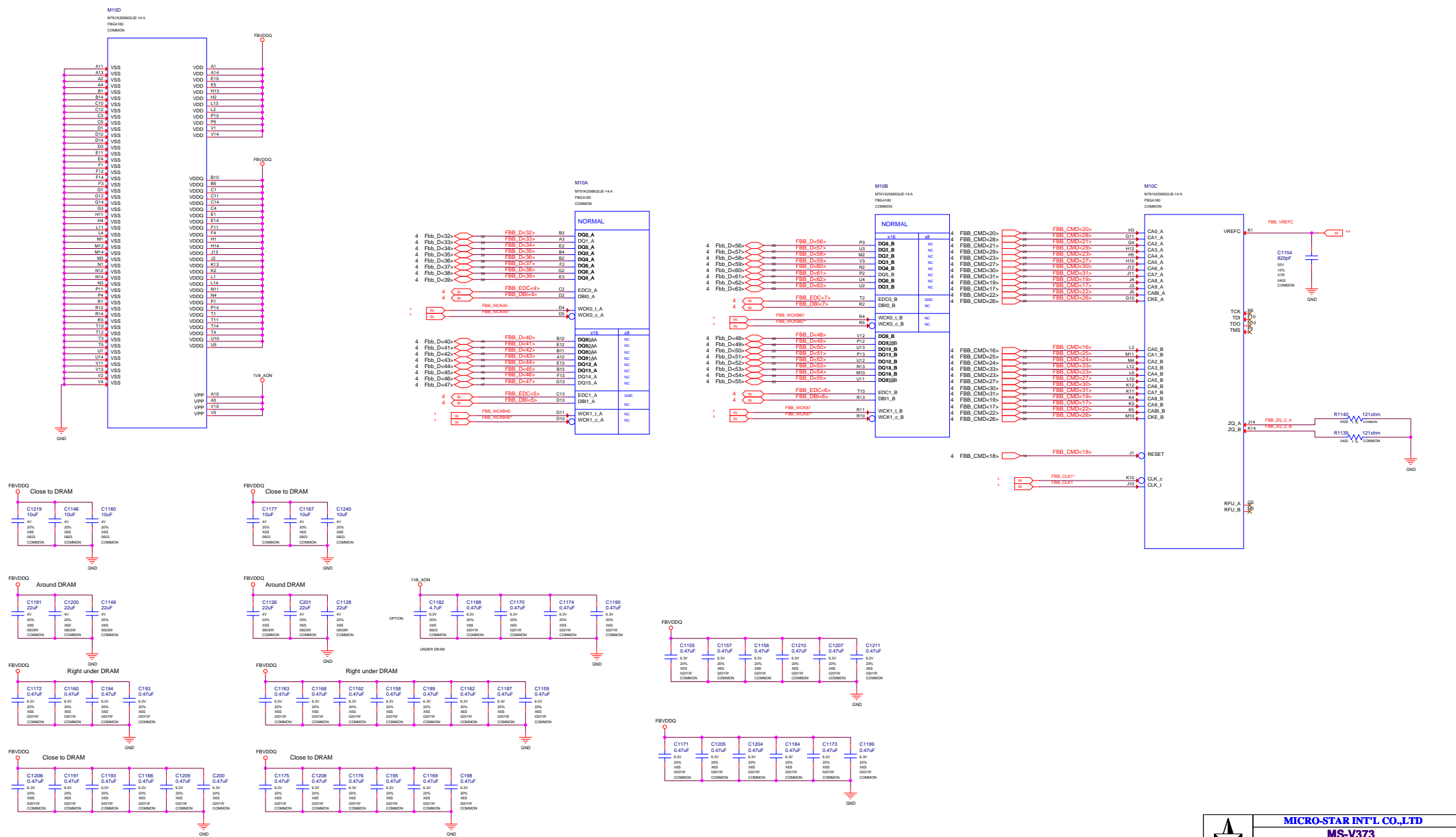


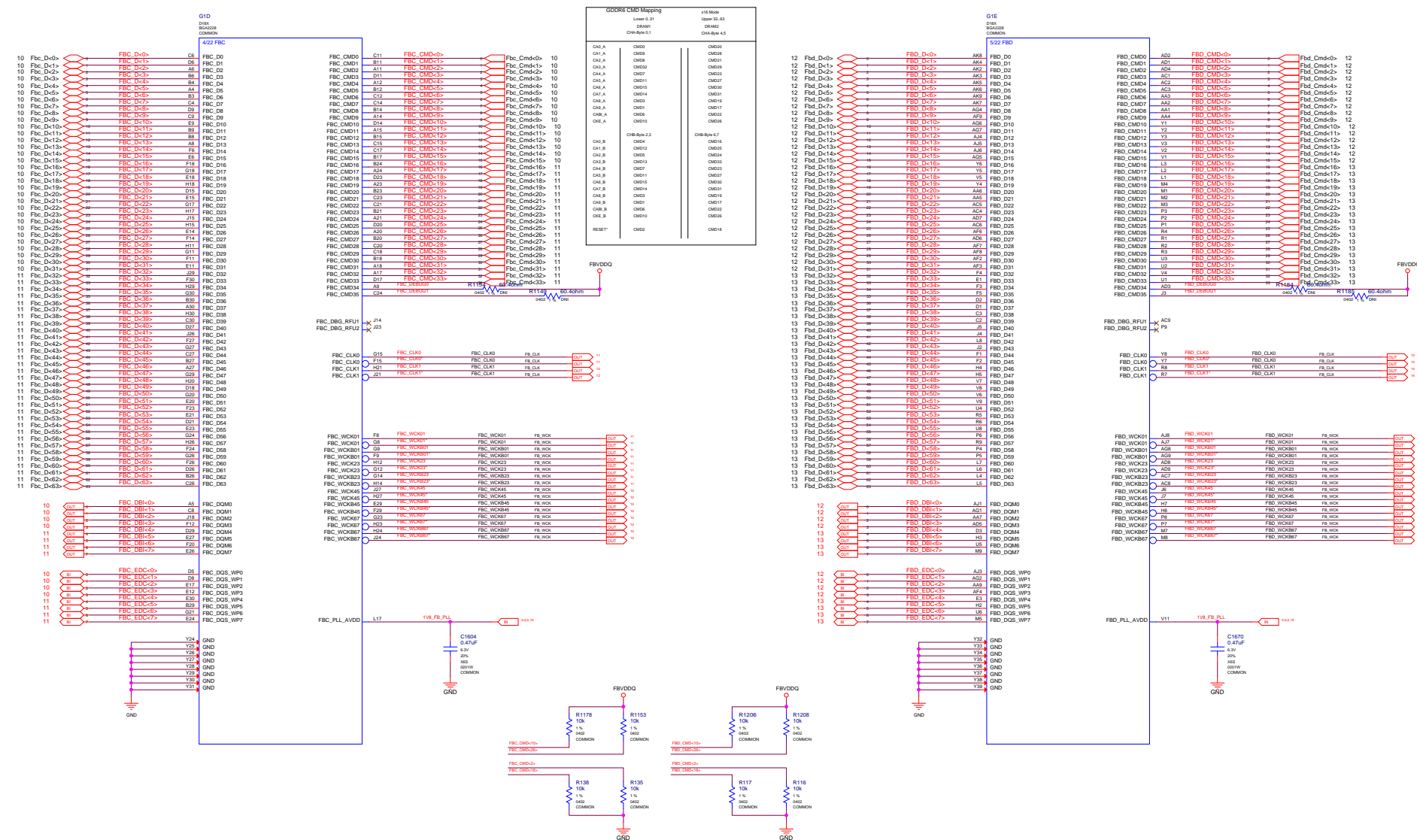


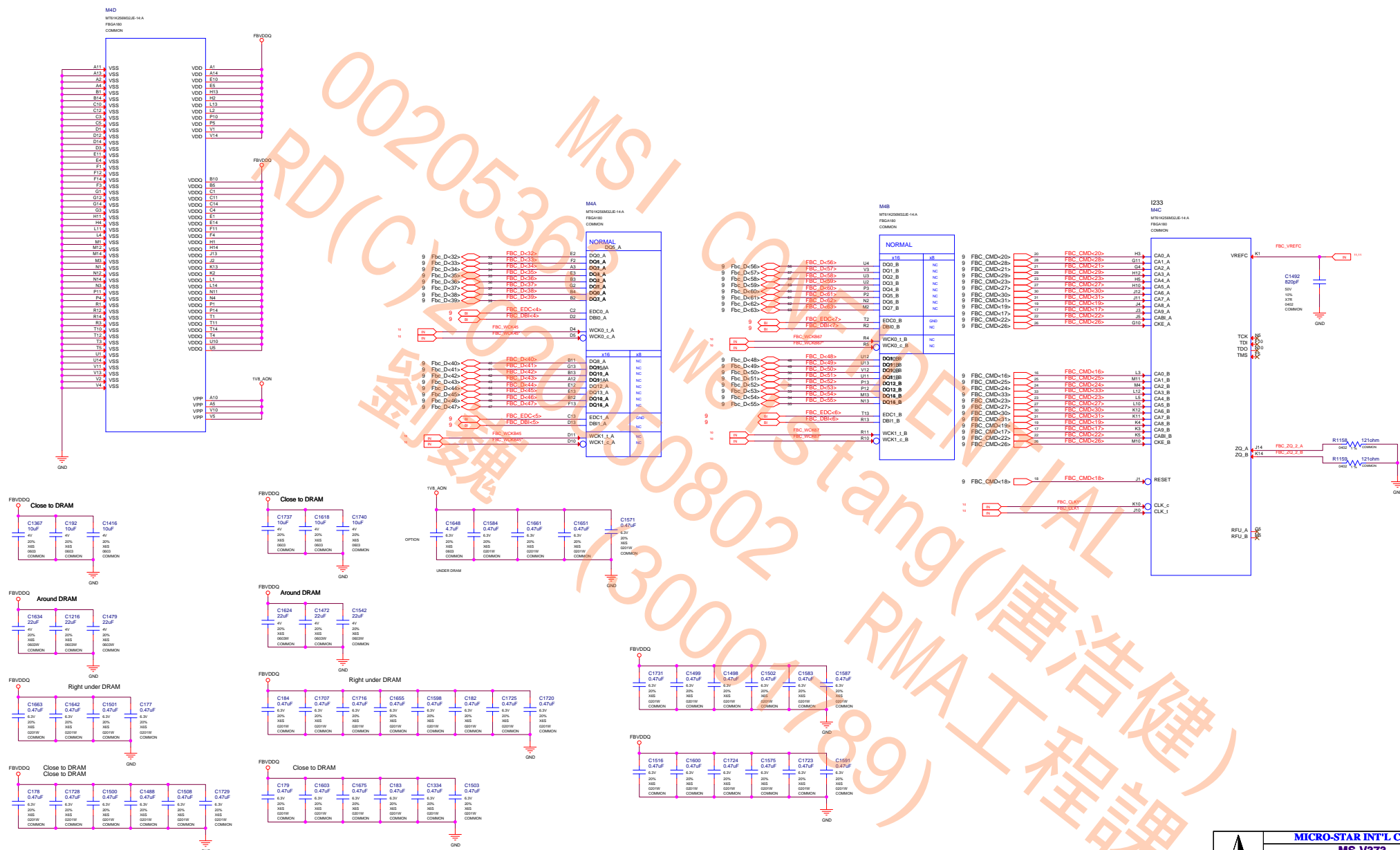


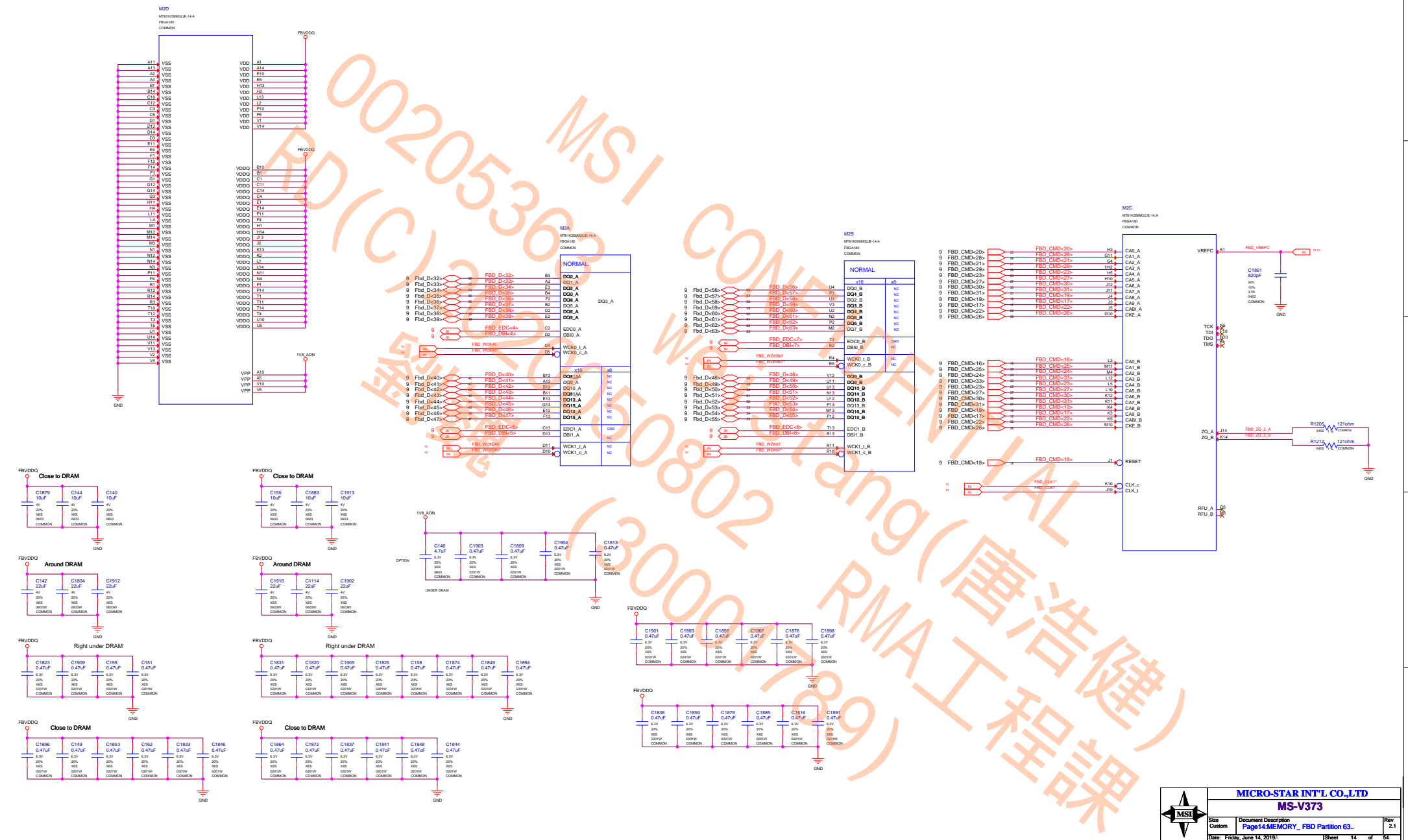


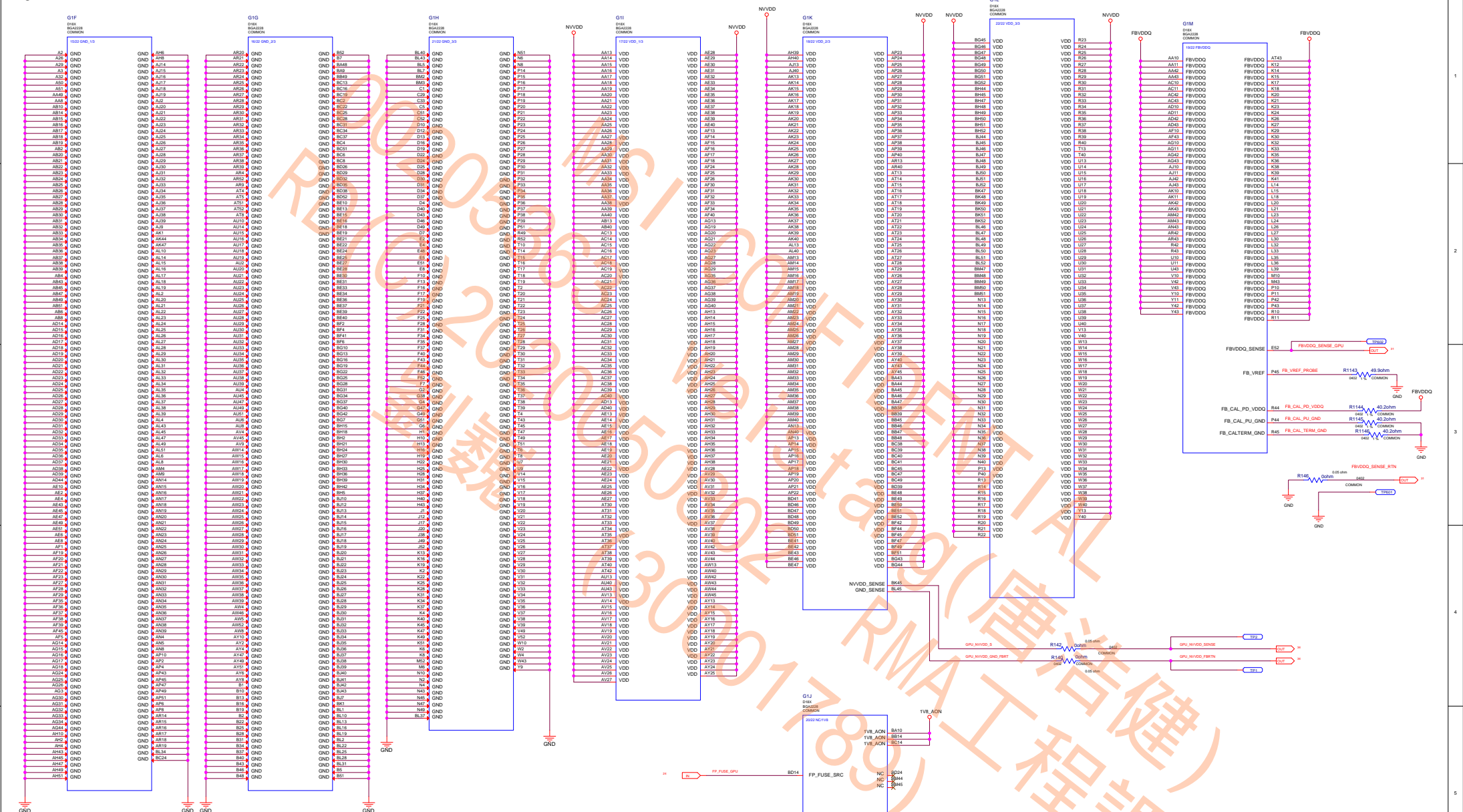








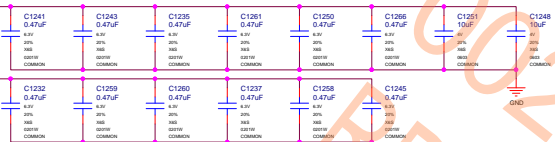




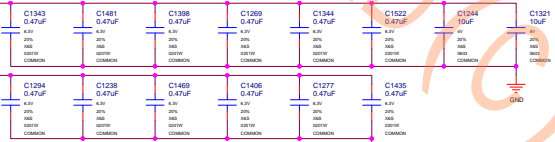
NVVDD

FBVDDQ

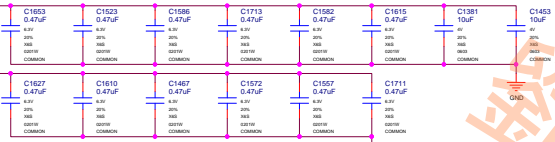
Partition A



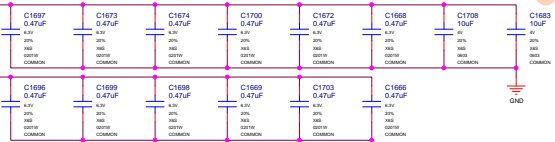
Partition B



Partition C



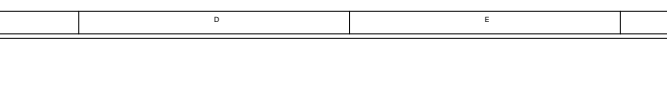
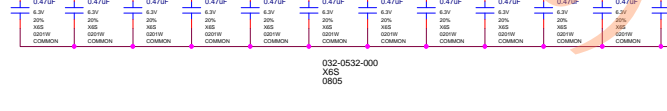
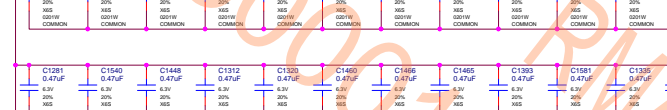
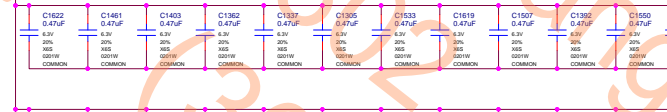
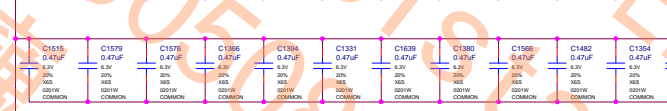
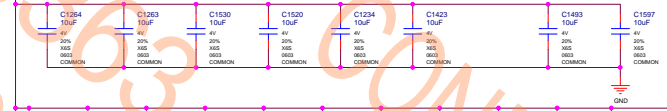
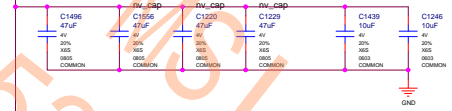
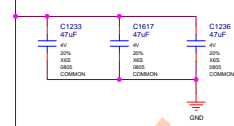
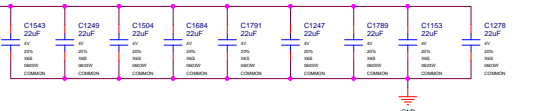
Partition D



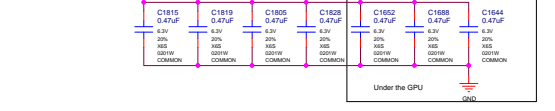
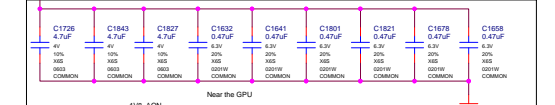
Place Close to GPU



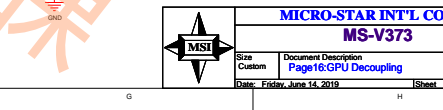
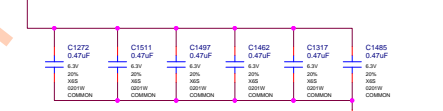
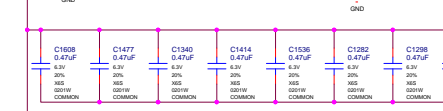
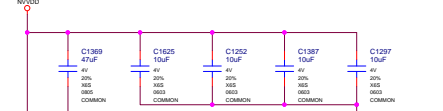
Place Close to GPU



1V8_AON

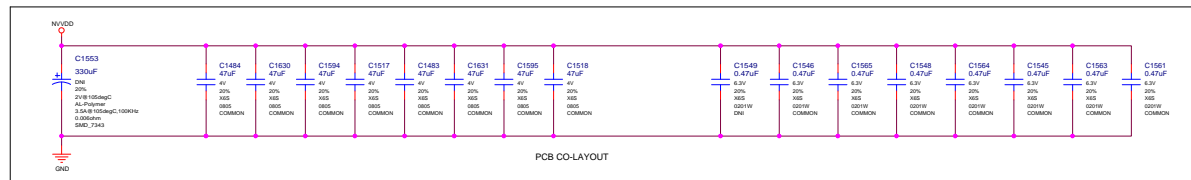
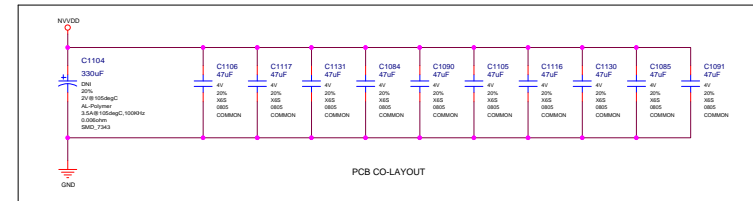
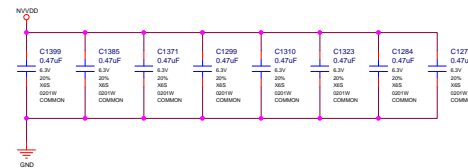
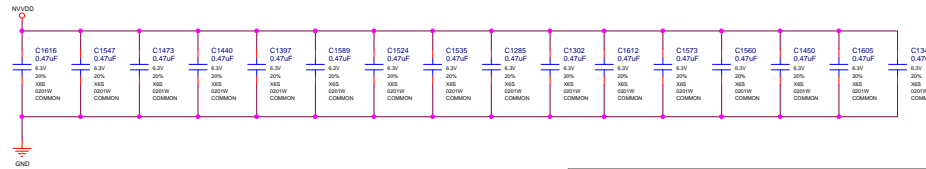
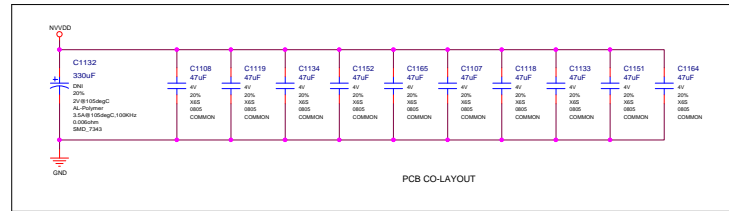
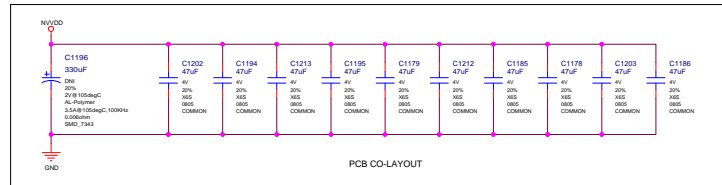
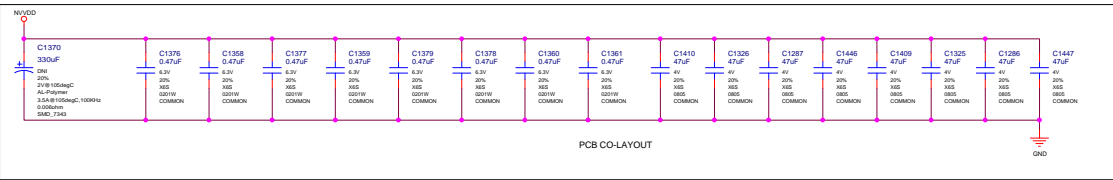


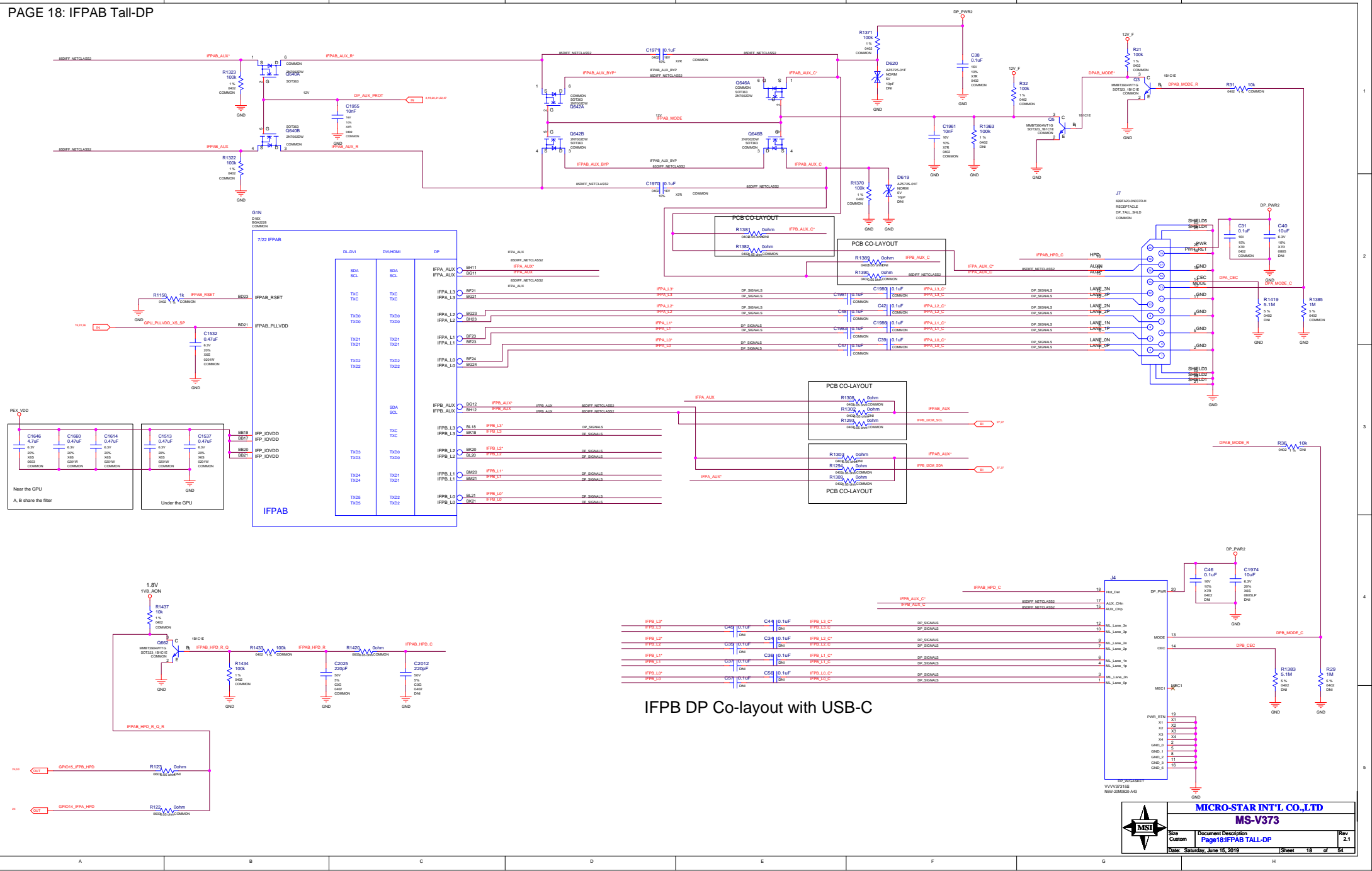
NVVDD



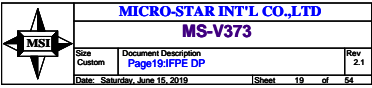
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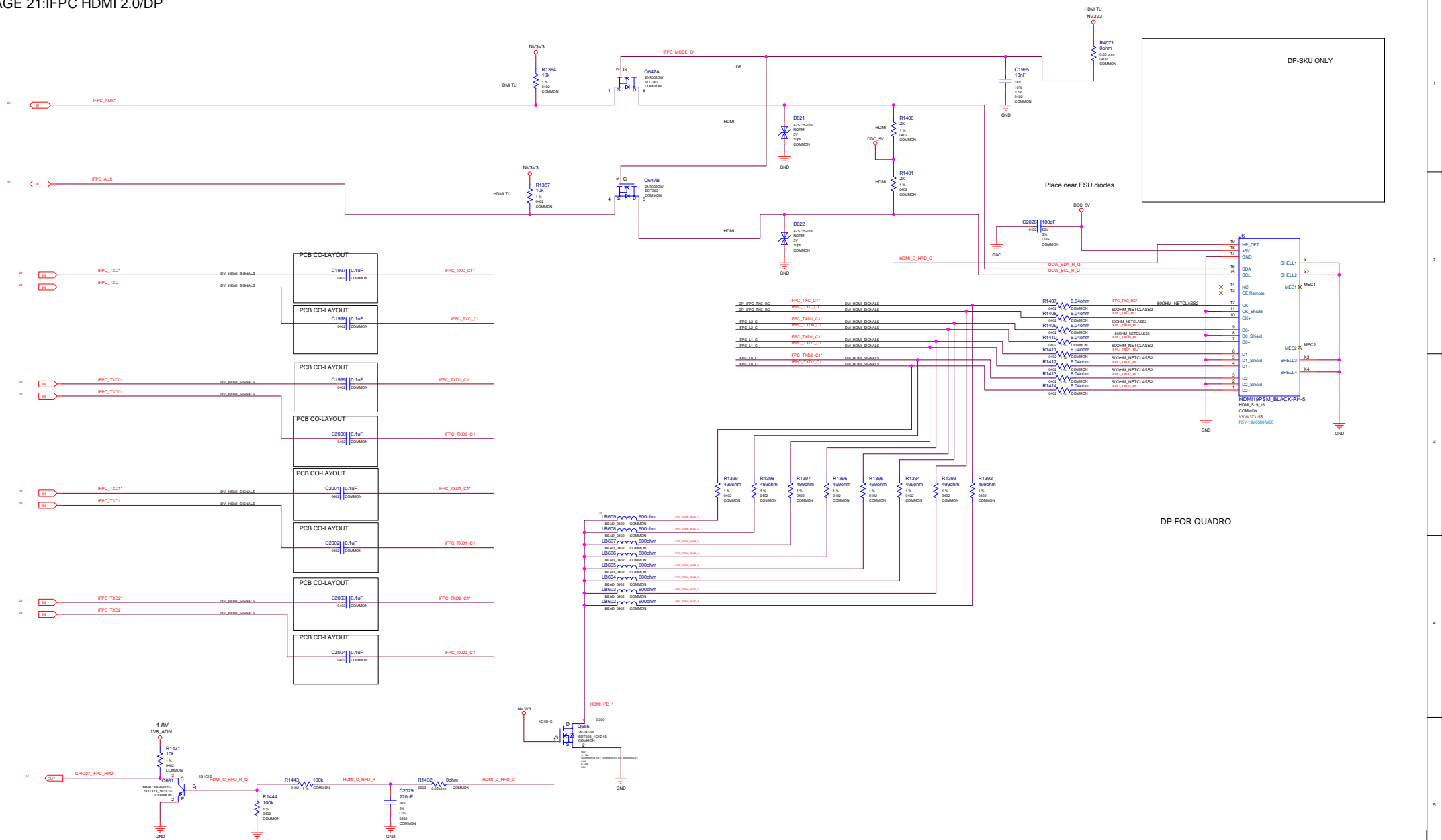
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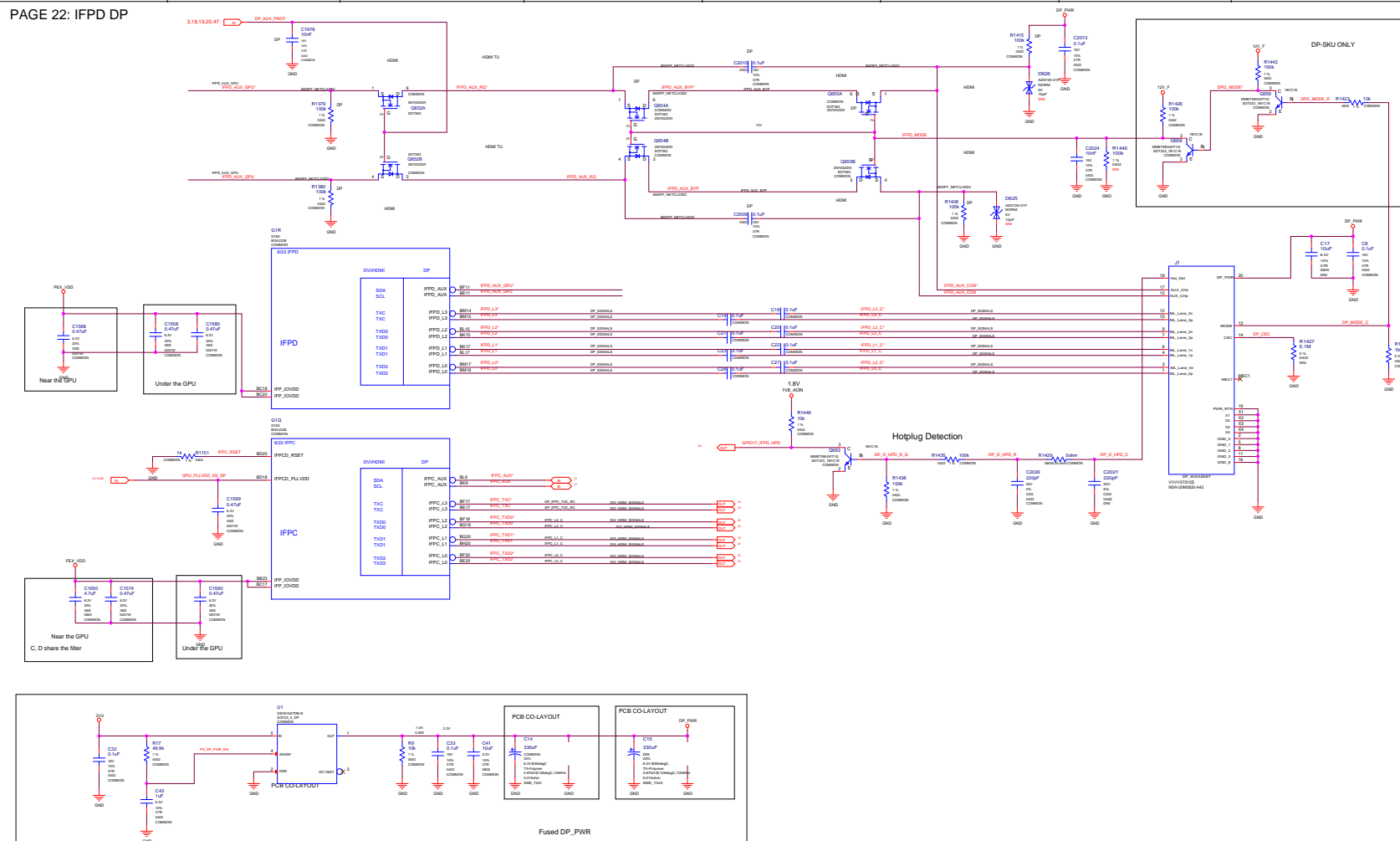


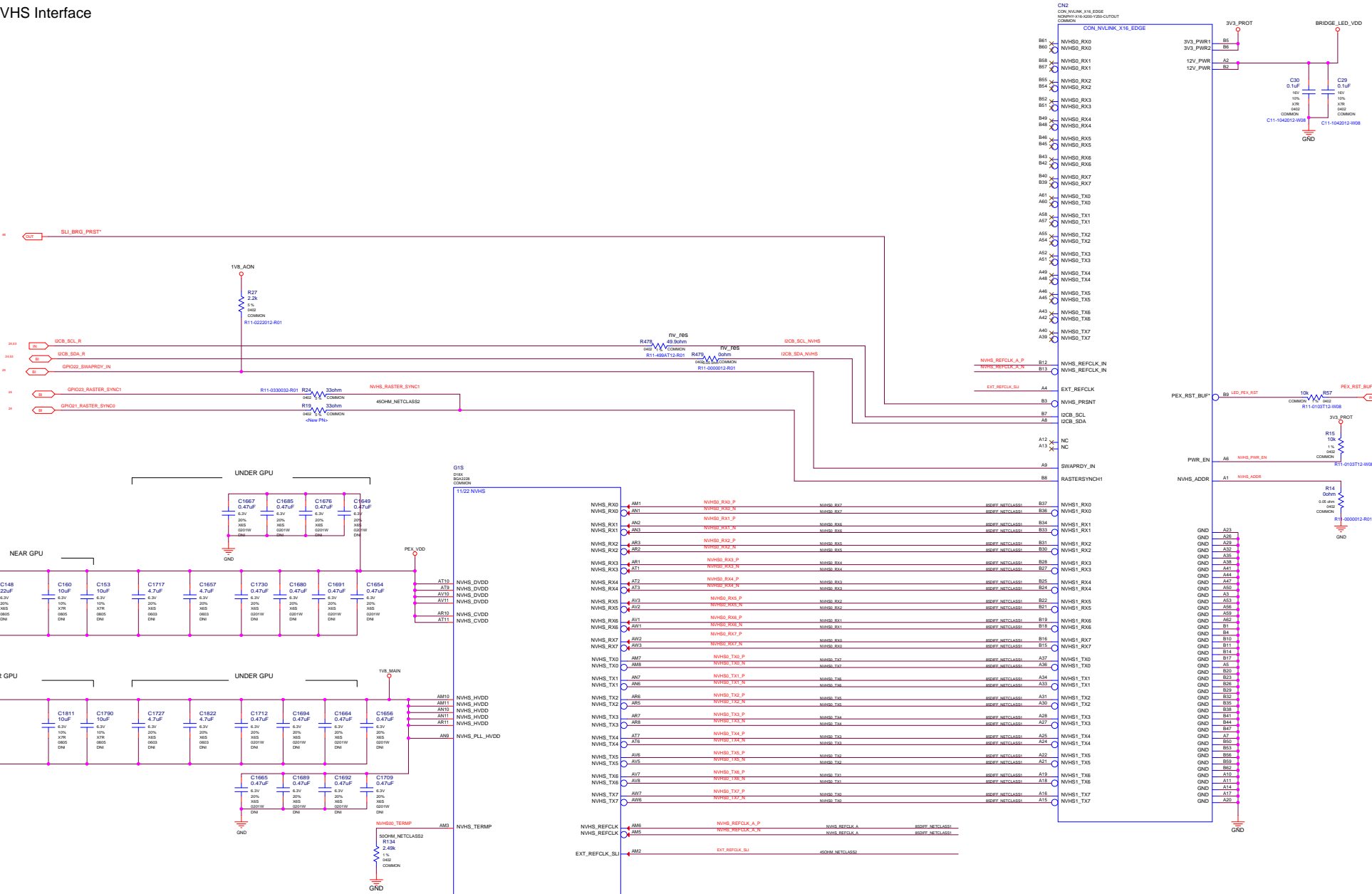


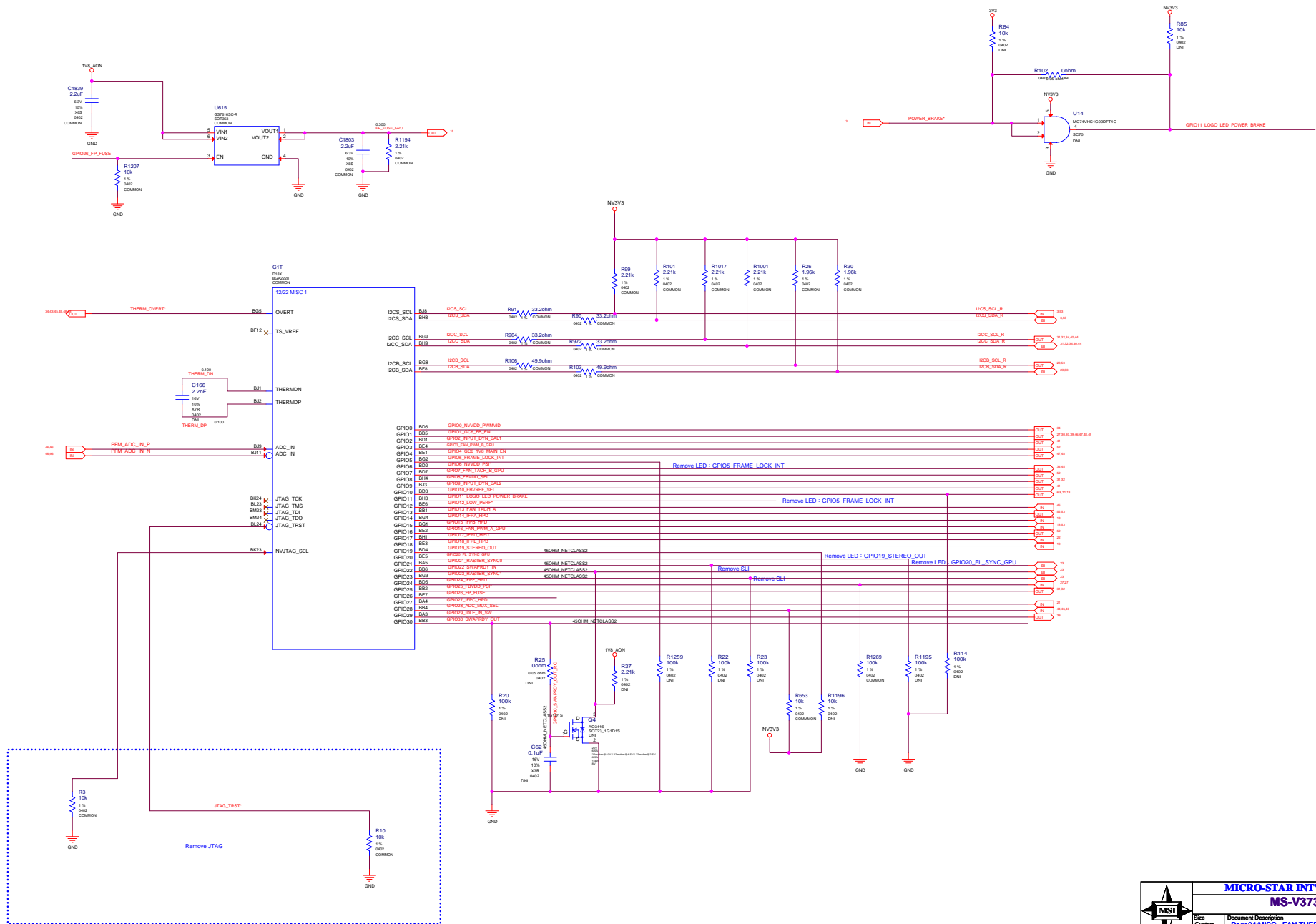
IFPAB DP Co-layout with USB-C











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H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

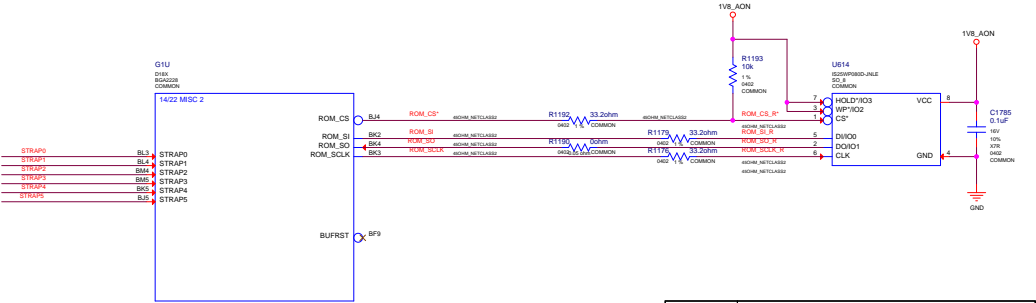
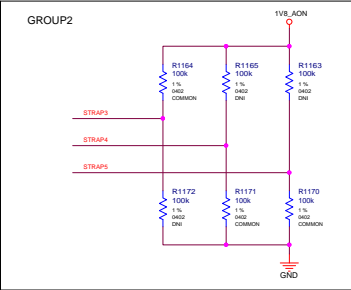
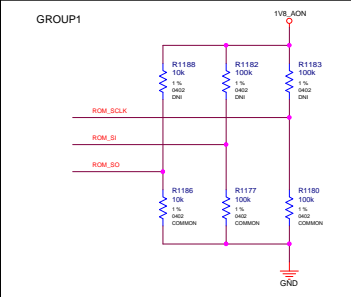
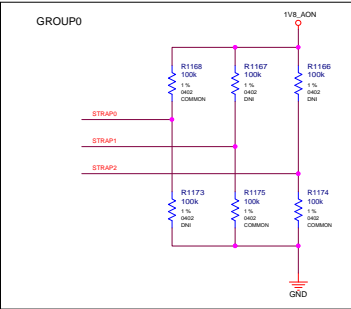
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

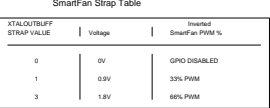
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

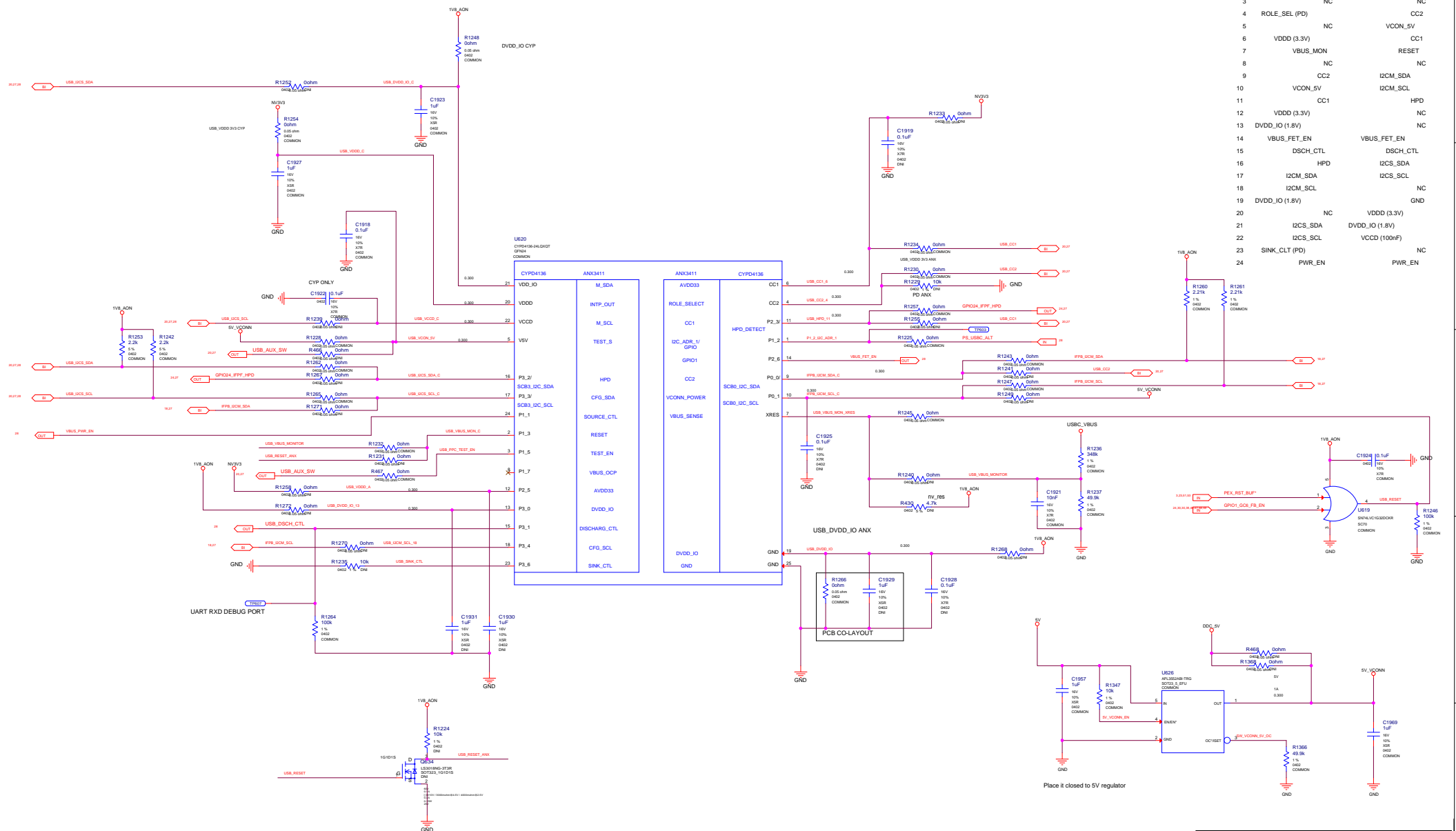
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default

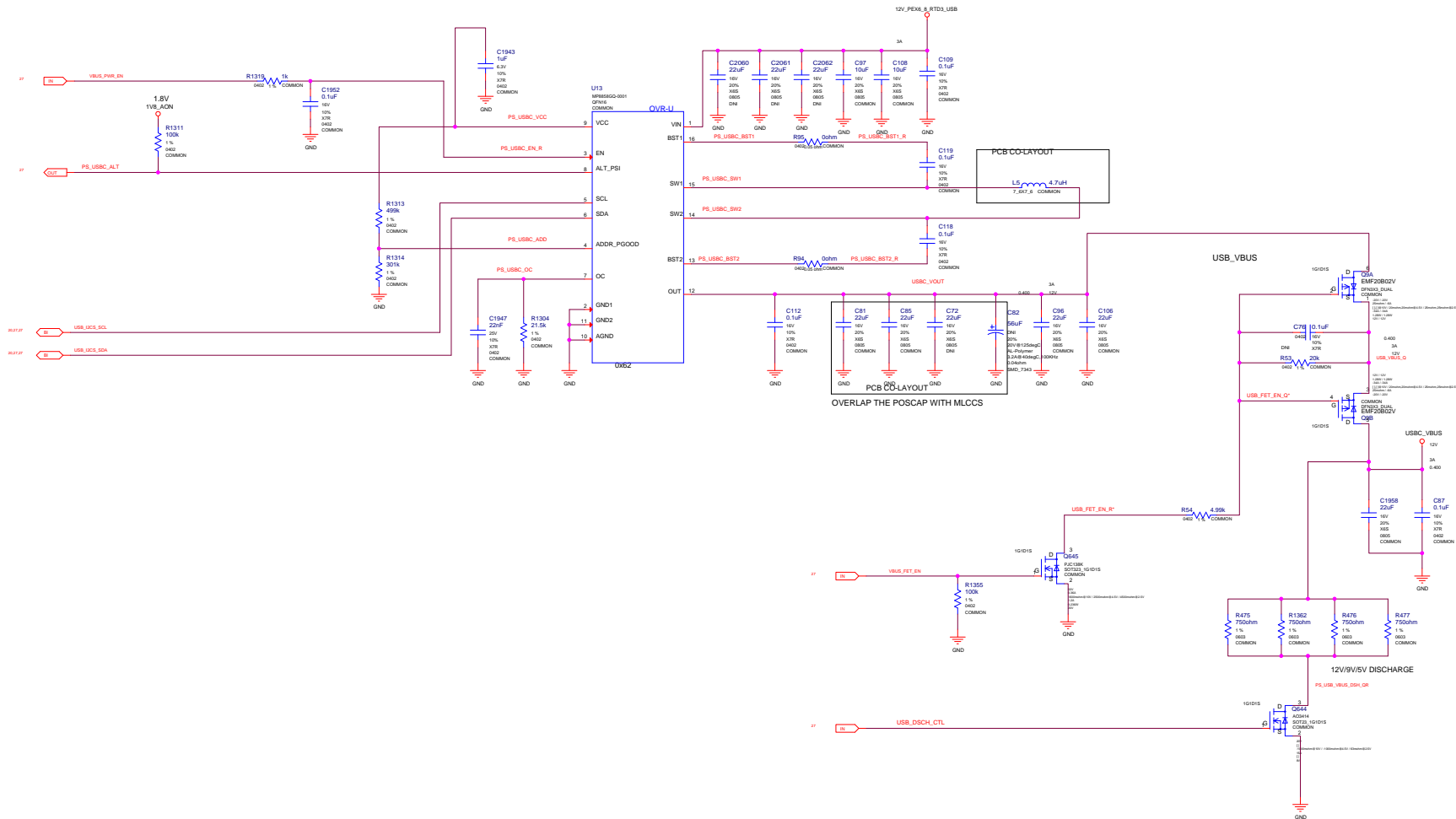
RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

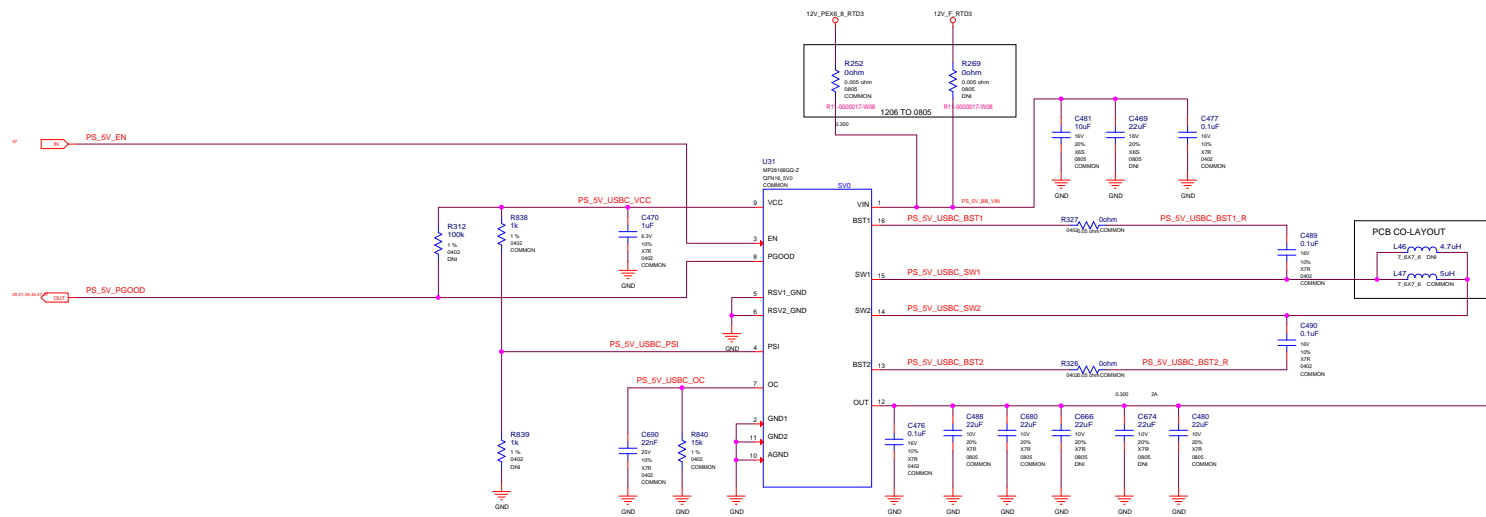






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	Size Custom	Document Description Page27:MISC_ USB PPC	Rev 2.1
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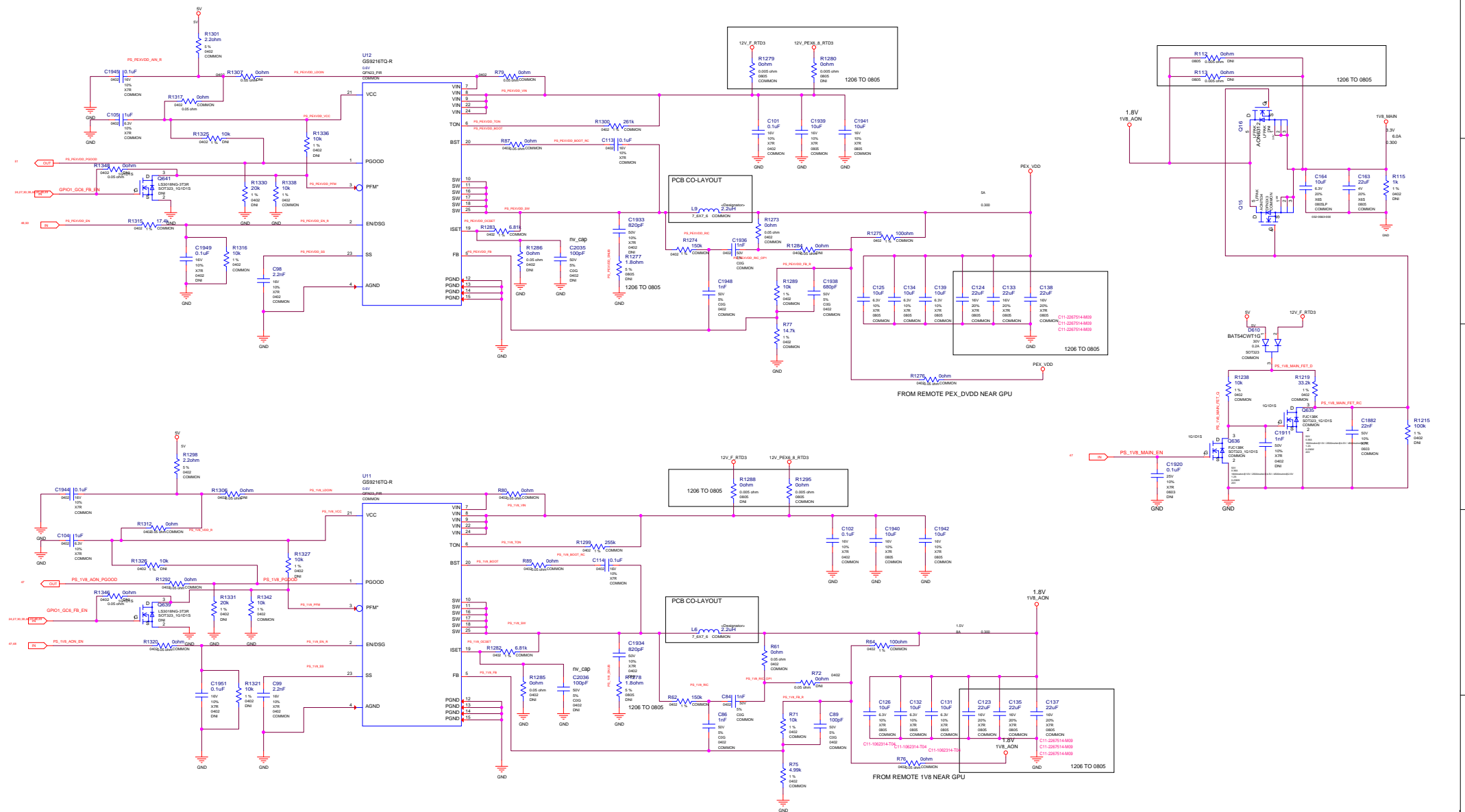
remove



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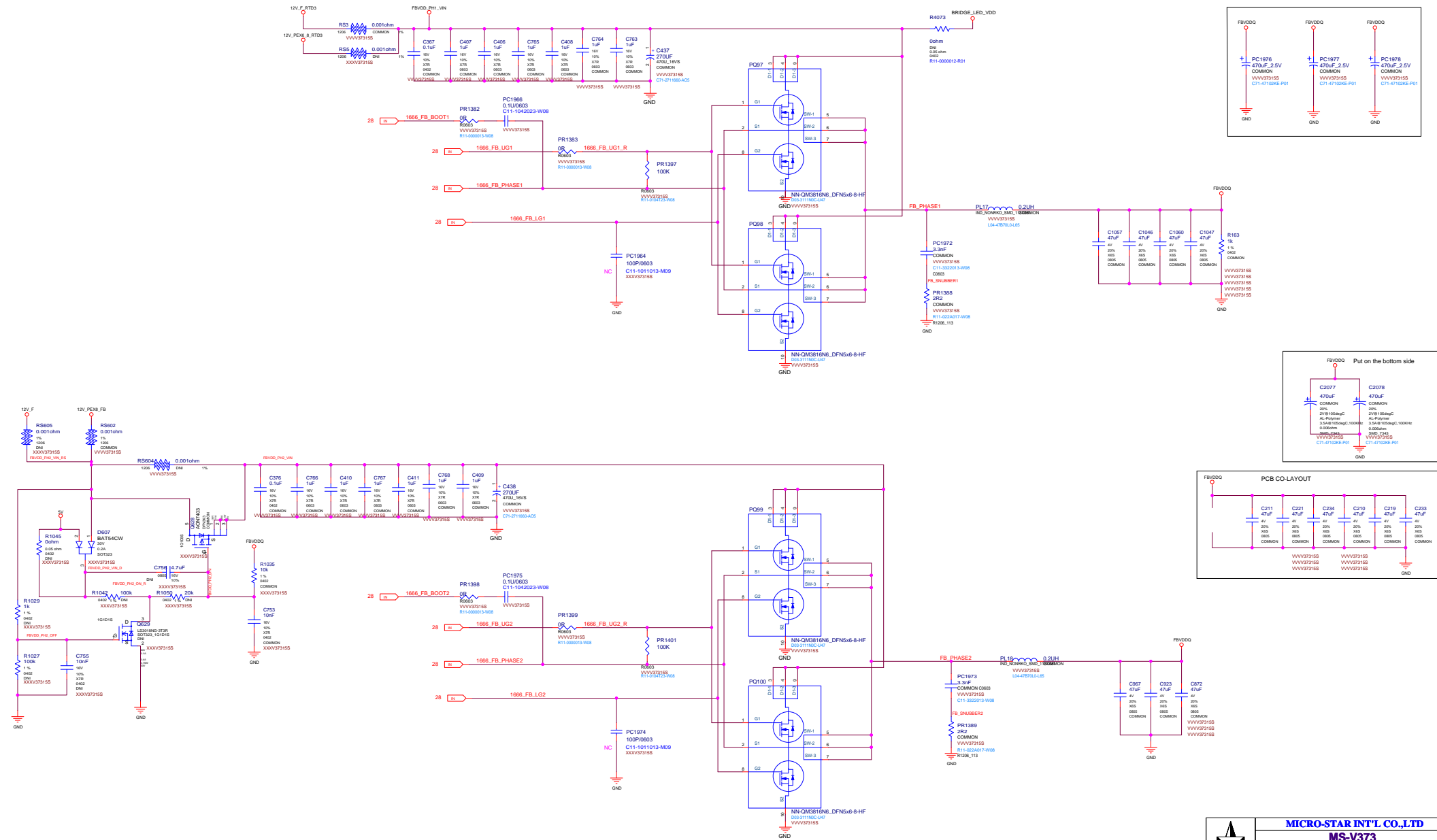


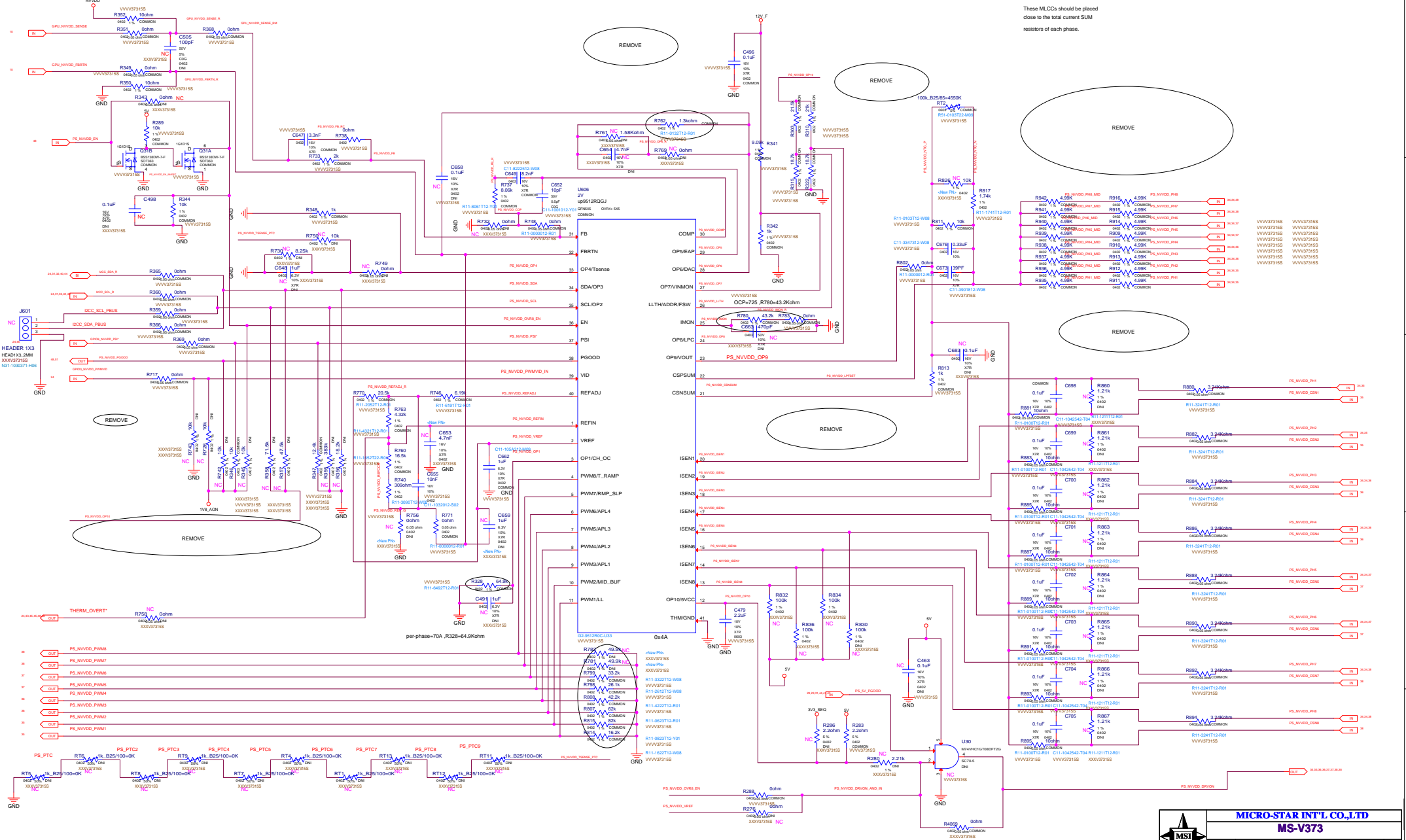
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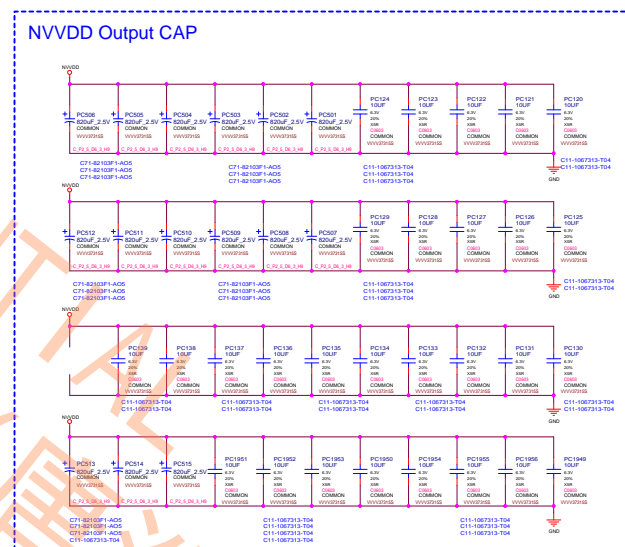
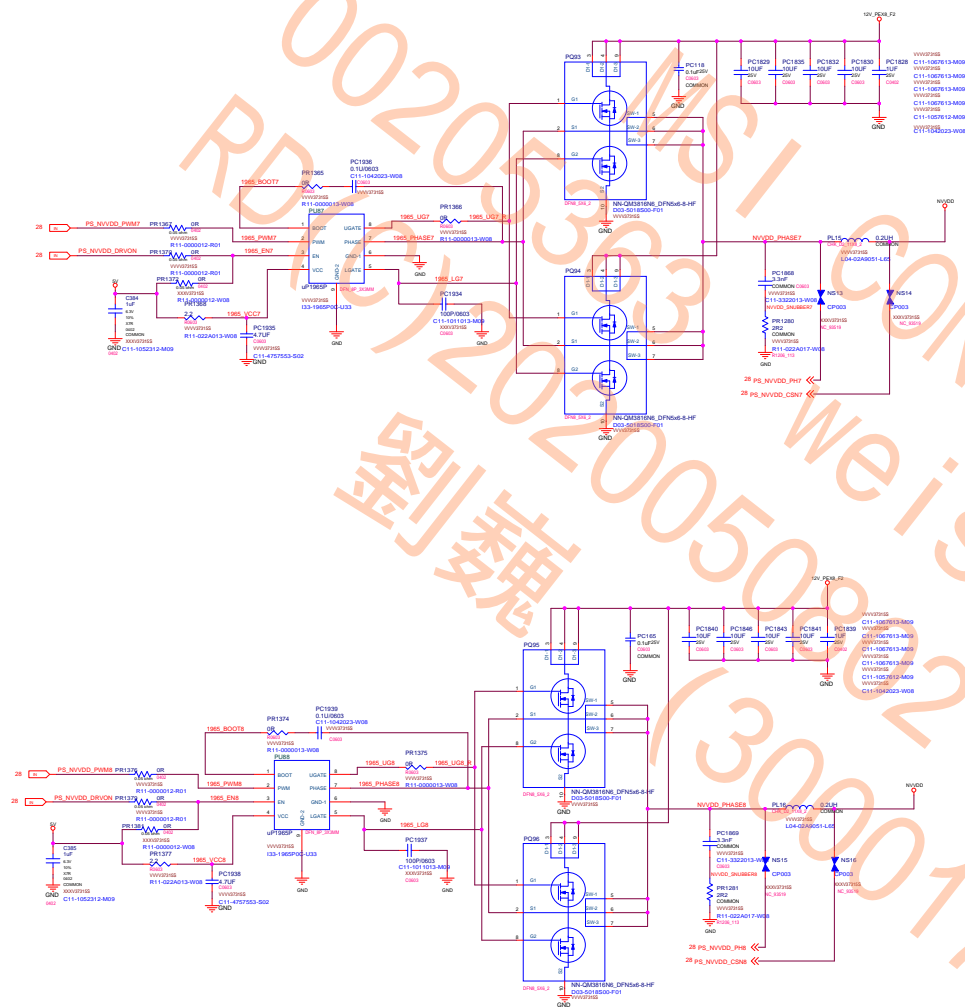
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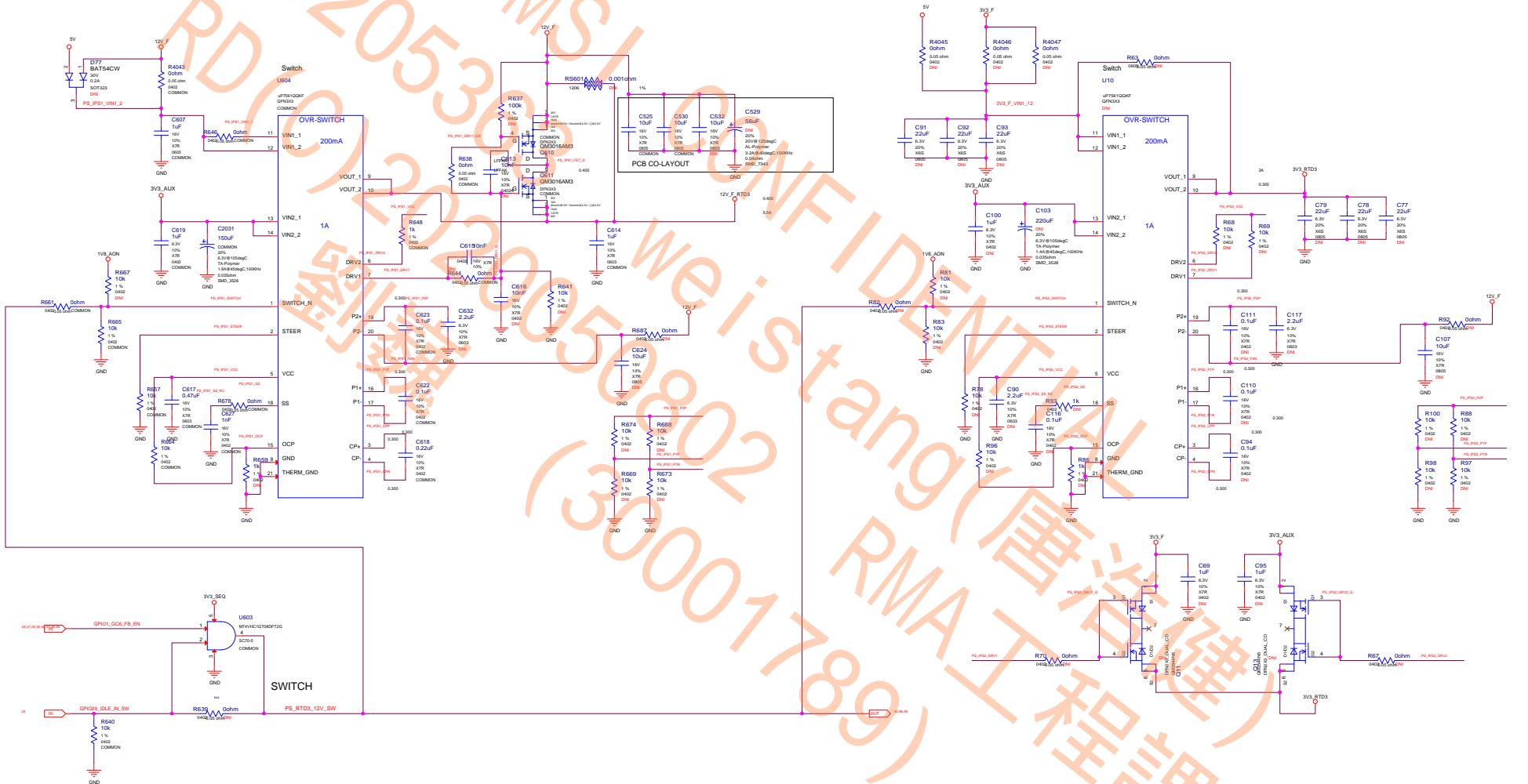


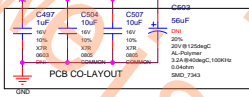
AND GATE LOGIC FOR P-BOARD

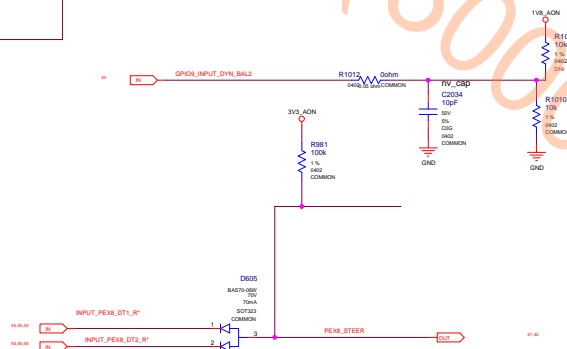
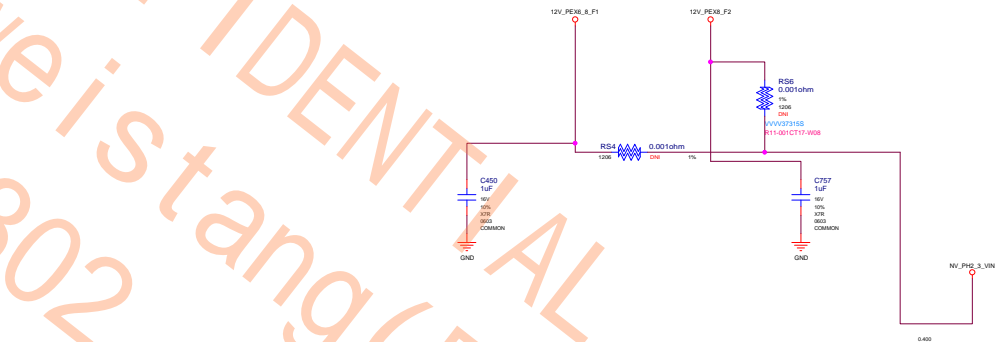
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

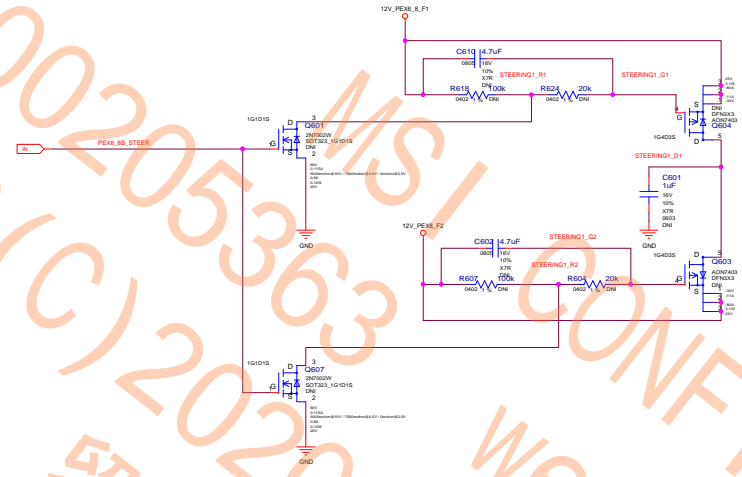
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



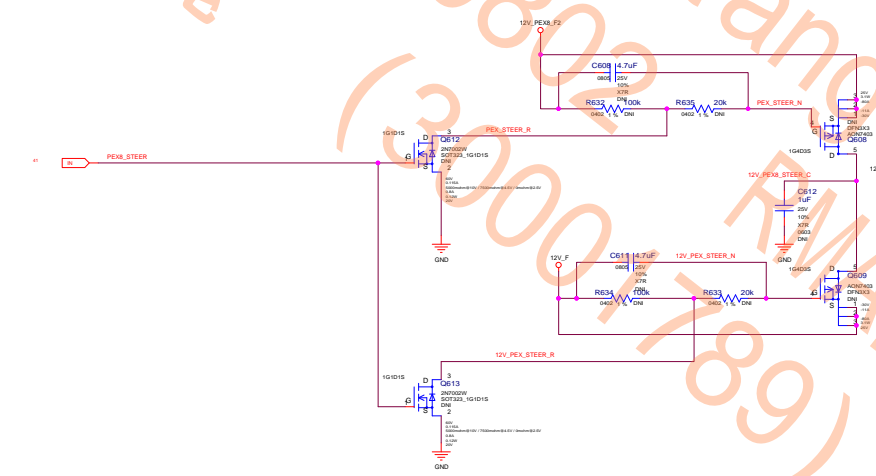




12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

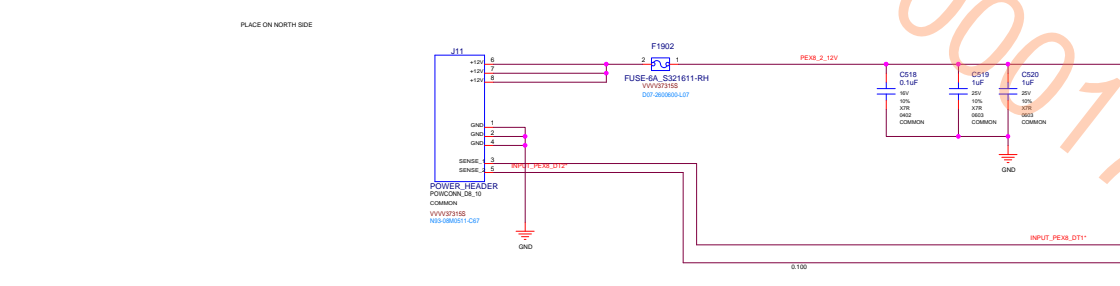
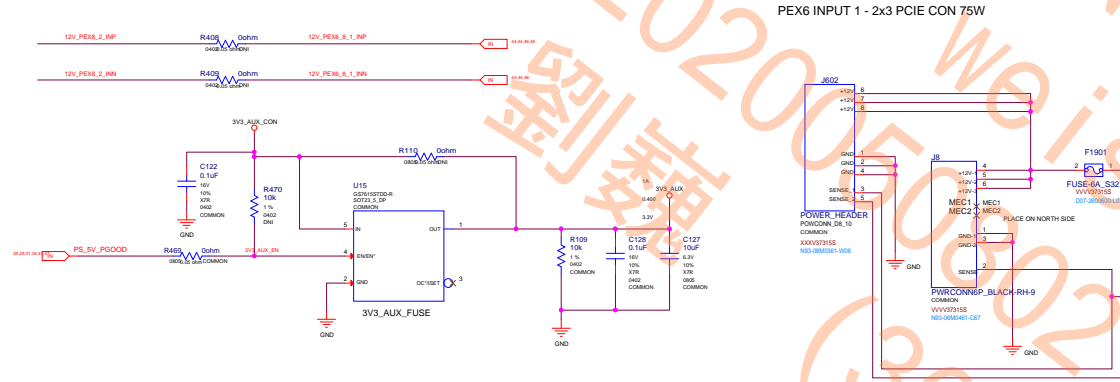
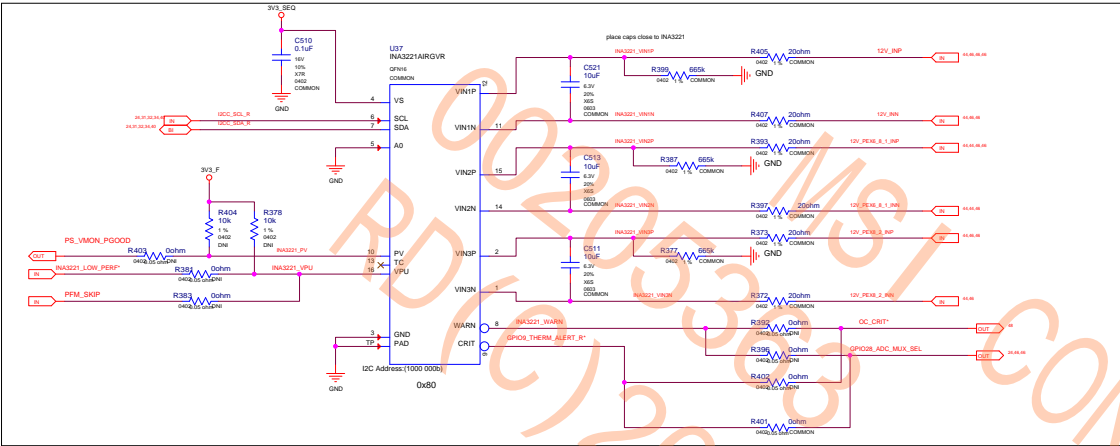


12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

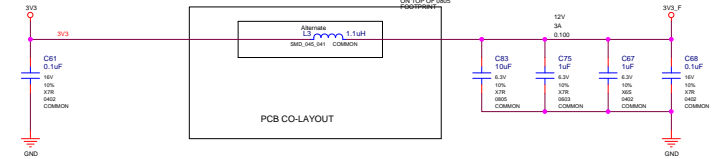


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00205363
RD(C)2020050802
劉魏
weistang(唐浩健)
(30001789)
RMA工程課

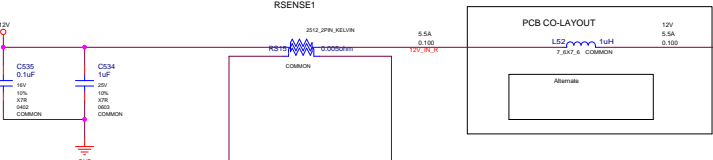
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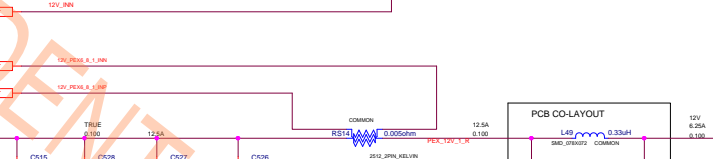
PEX 3V3 INPUT - 10W



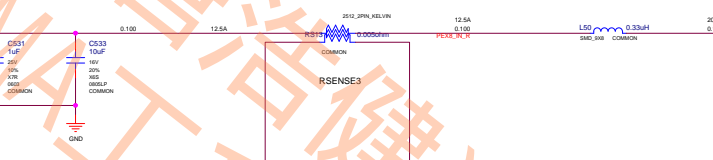
PEX_12V INPUT - 66W

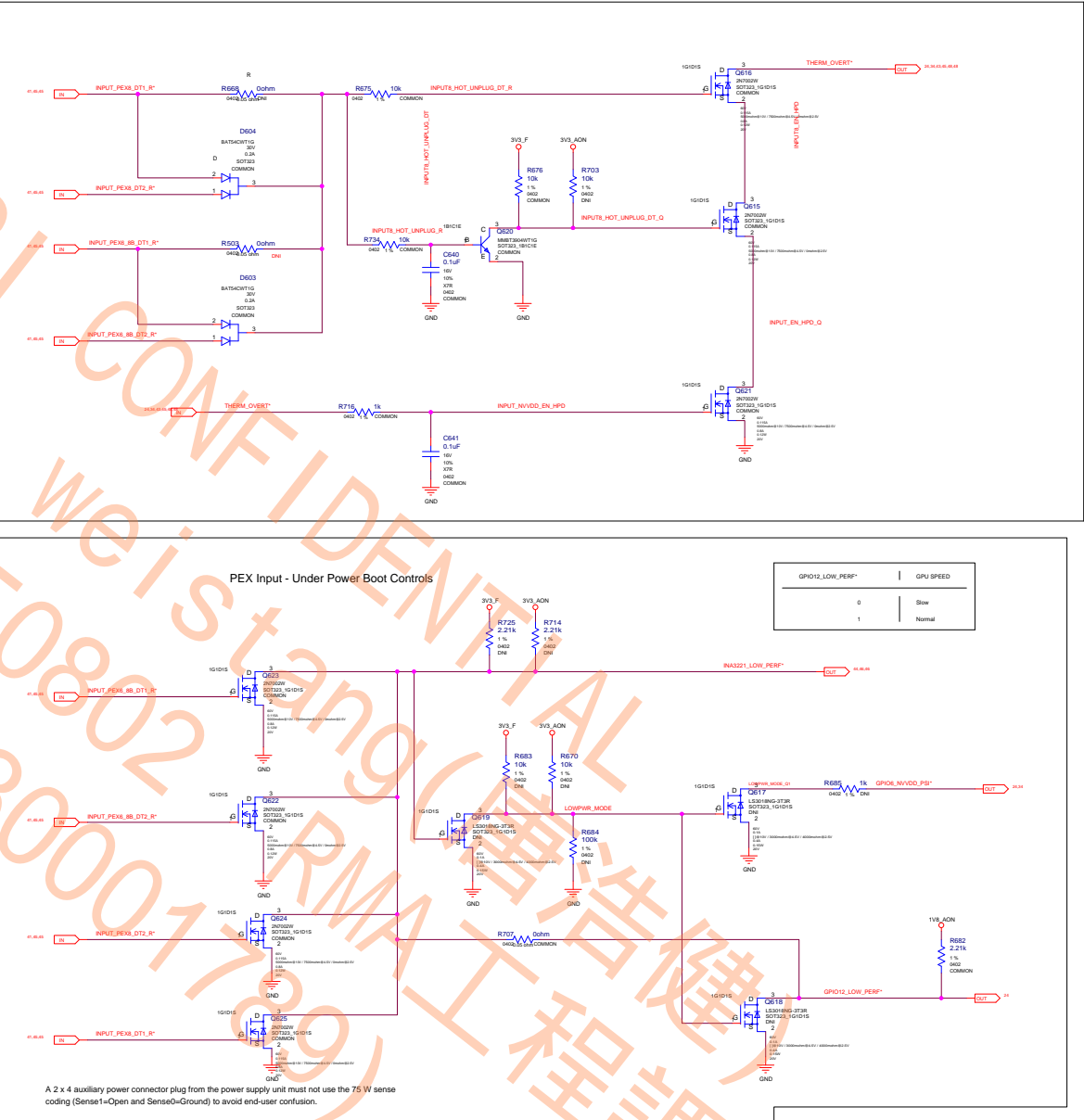
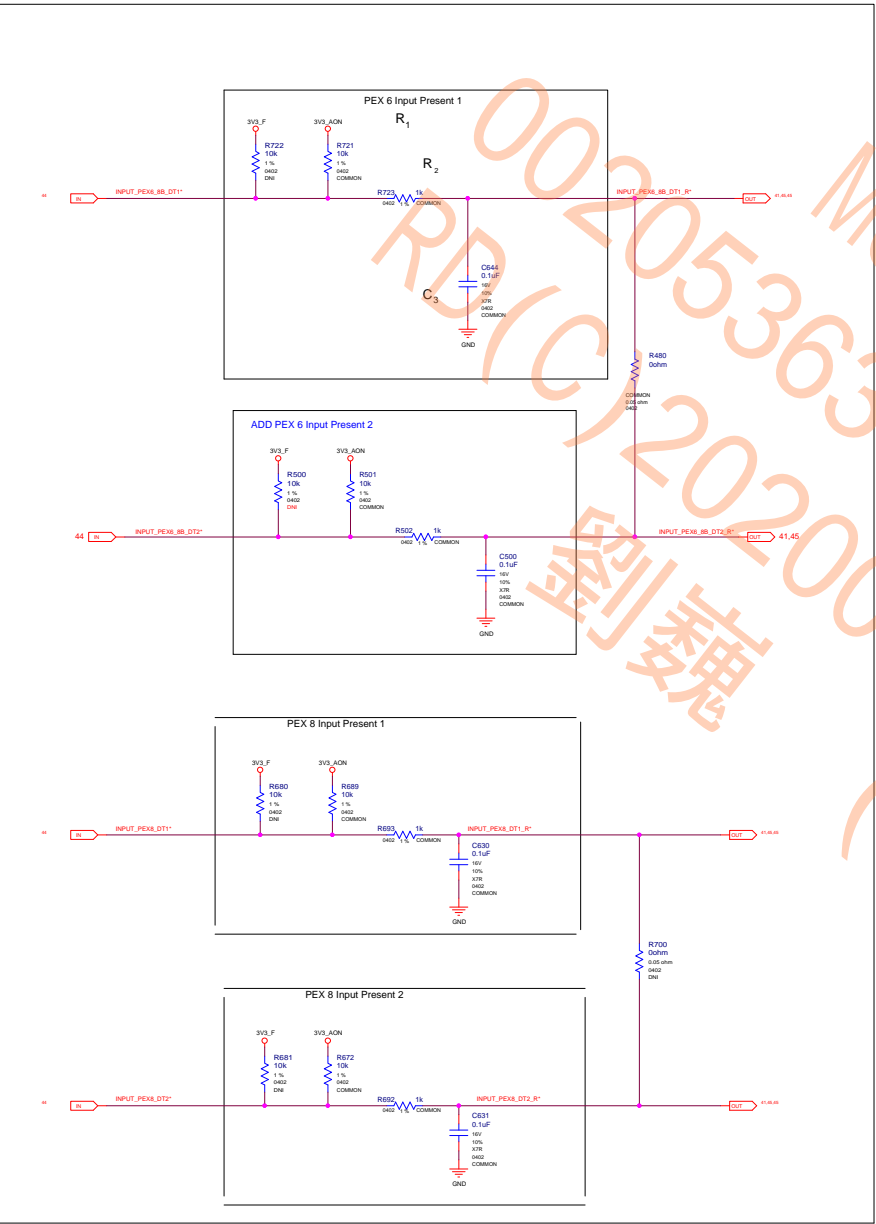


PEX6 INPUT 1 - 2x3 PCIe CON 75W

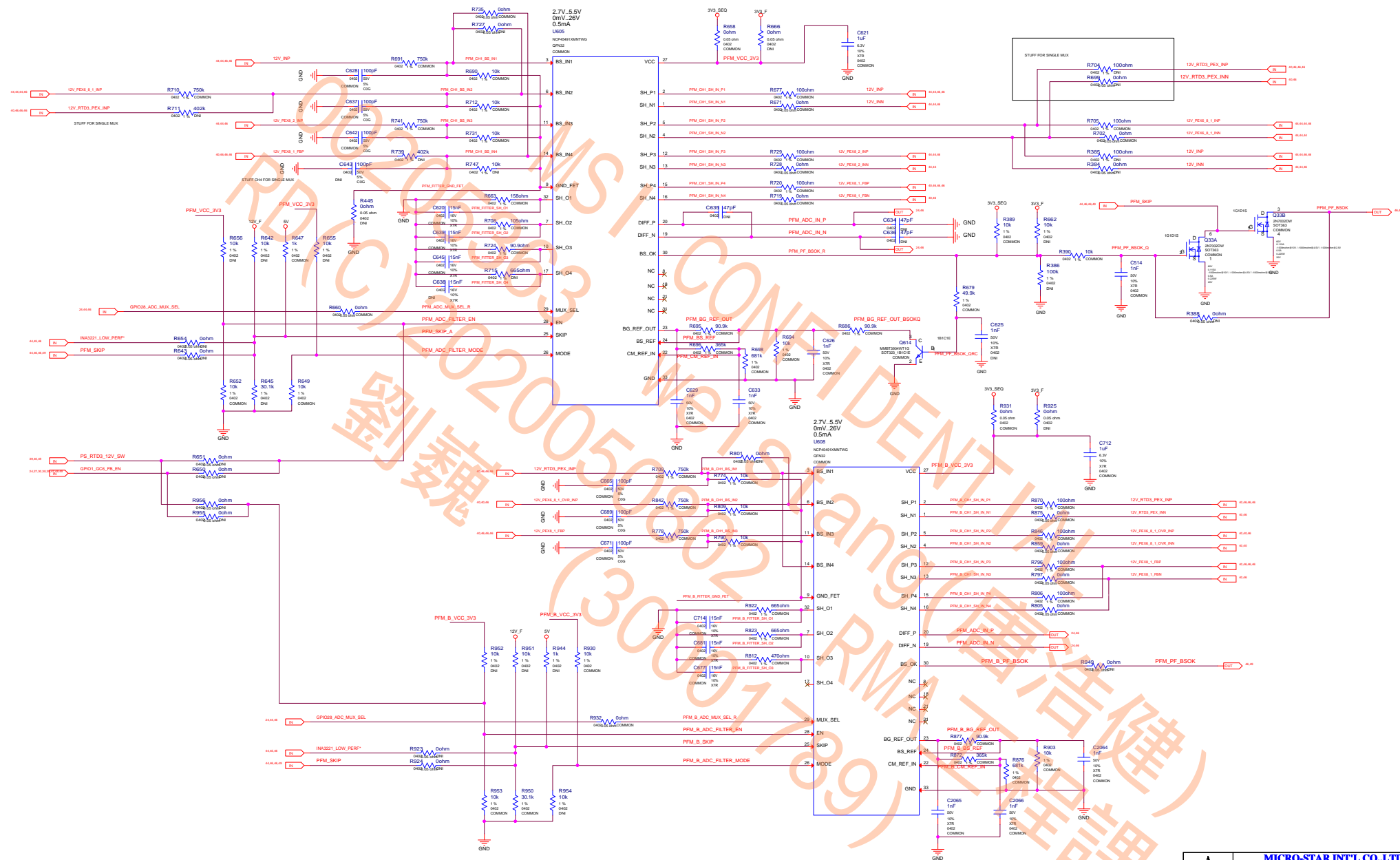


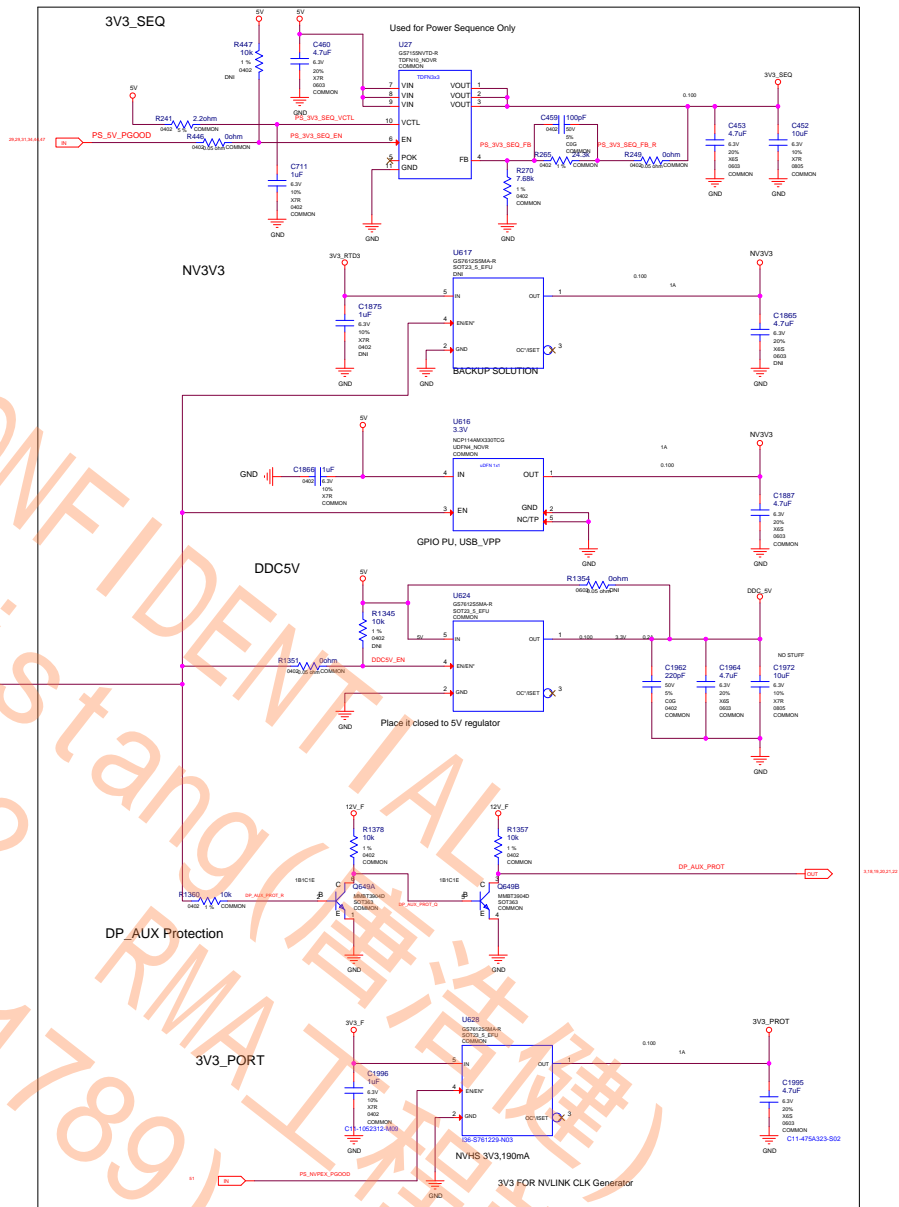
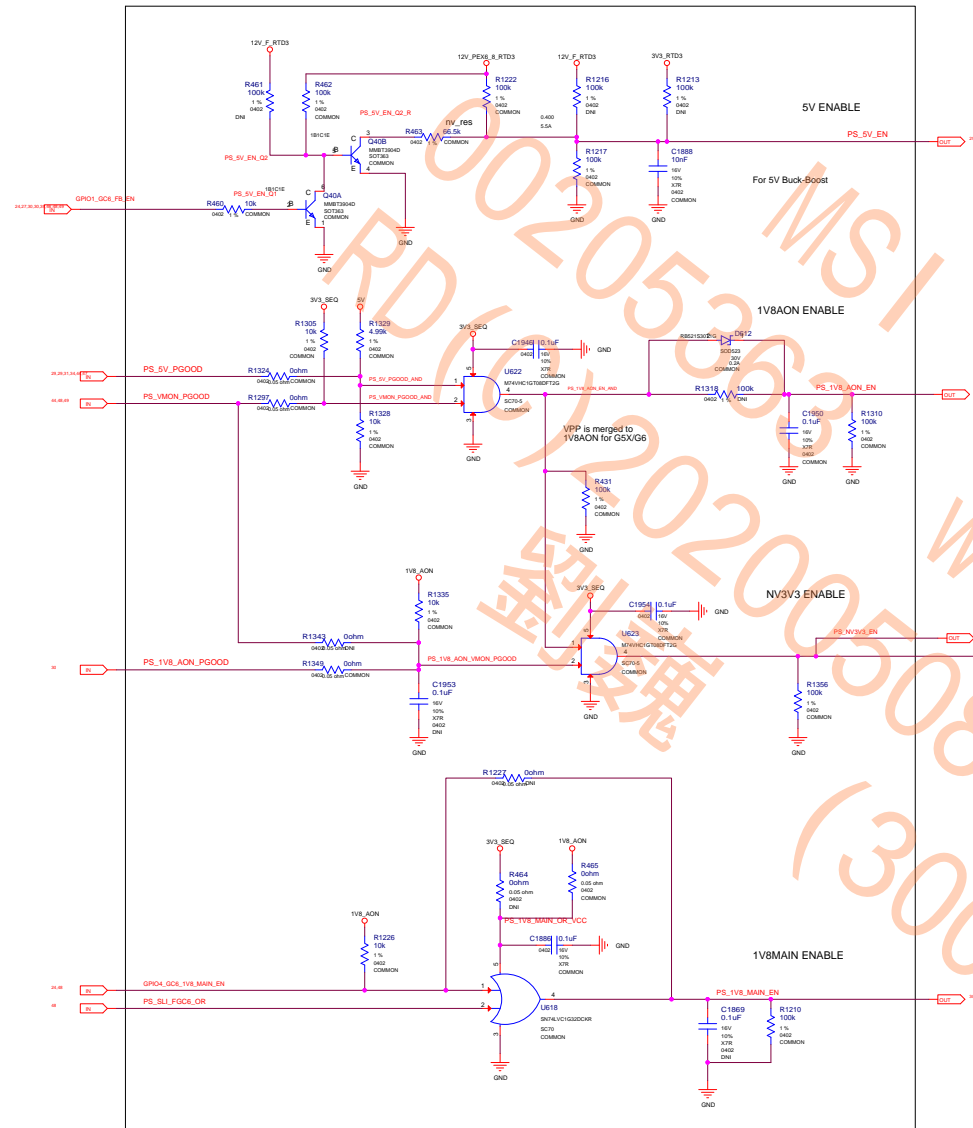
PEX8 INPUT 2 - 2x4 PCIe CON 150W





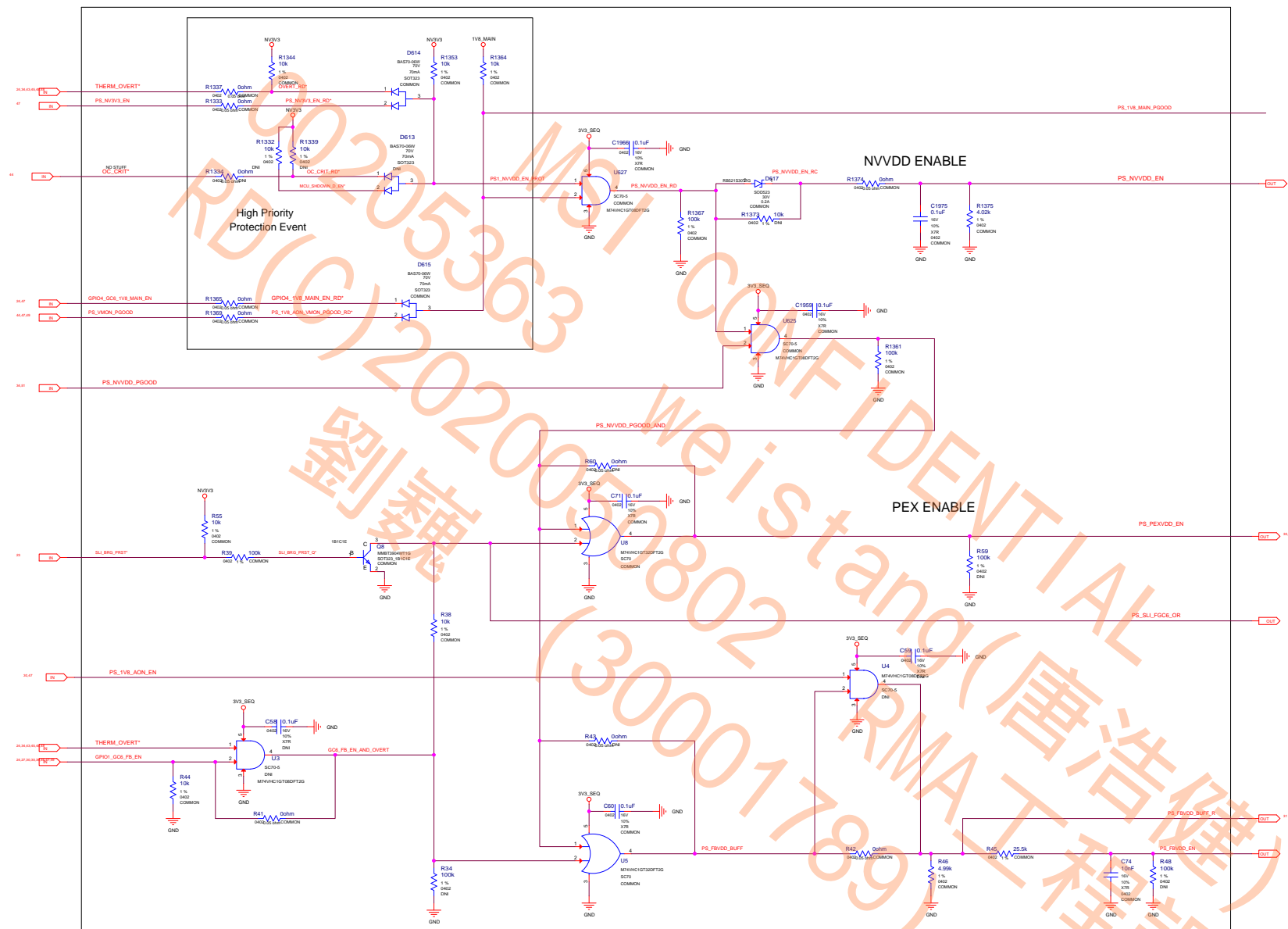
STUFF IF USING 2XMUX





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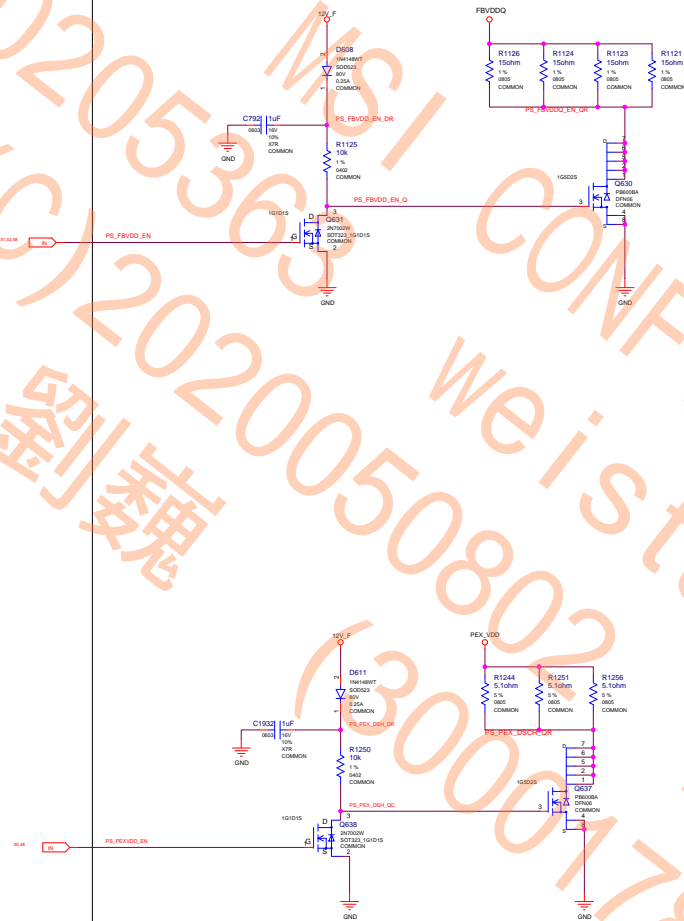
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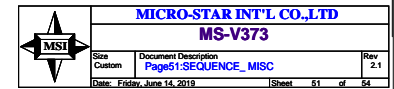


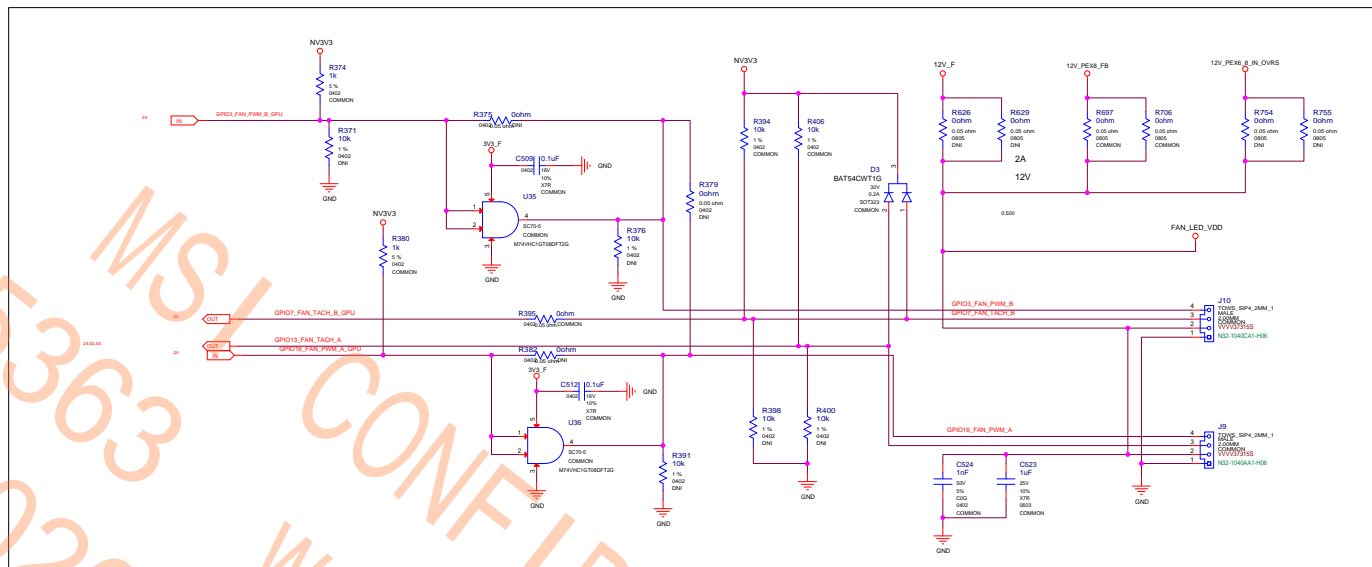
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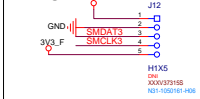


LED BOOST

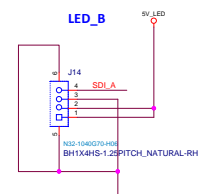
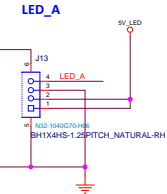
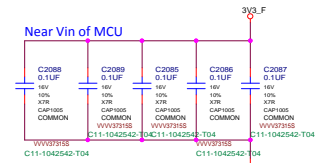
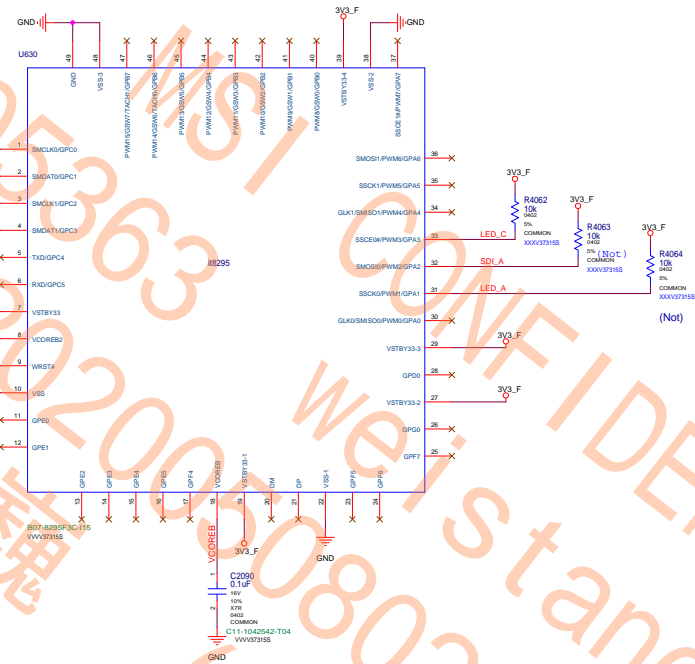
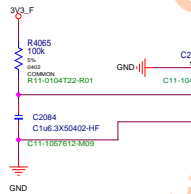
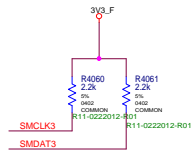
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Firmware Programming

Debug



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5V_LED

