

PG410 A01

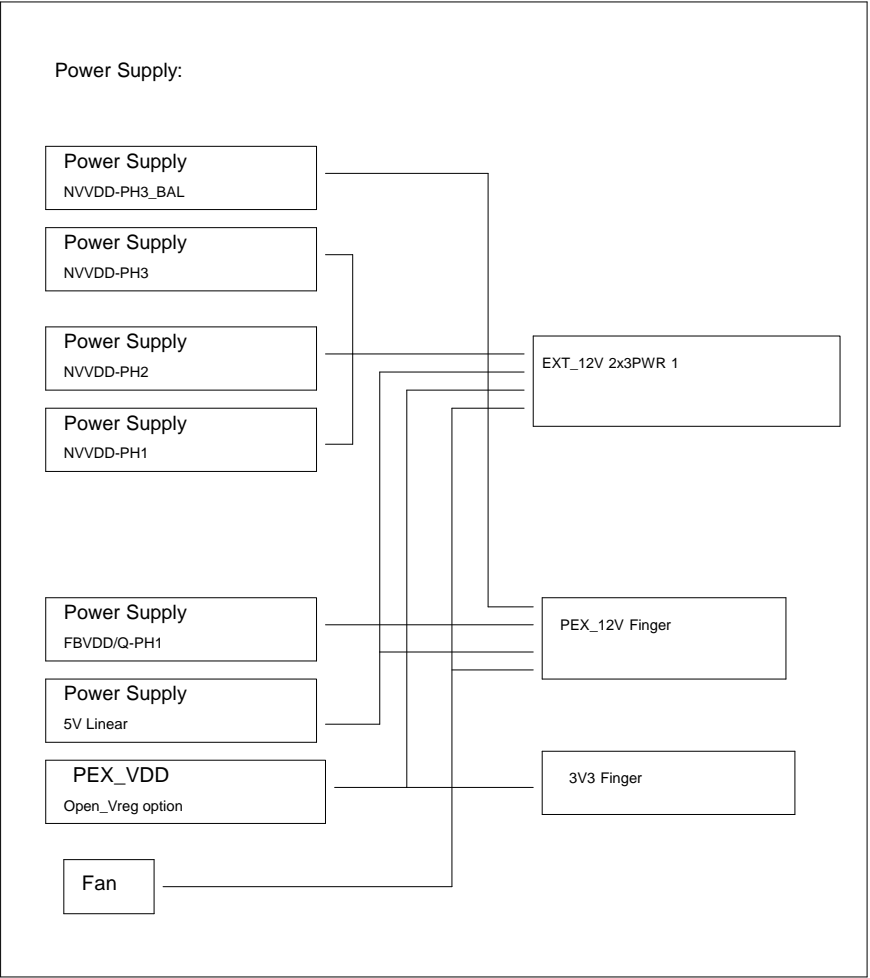
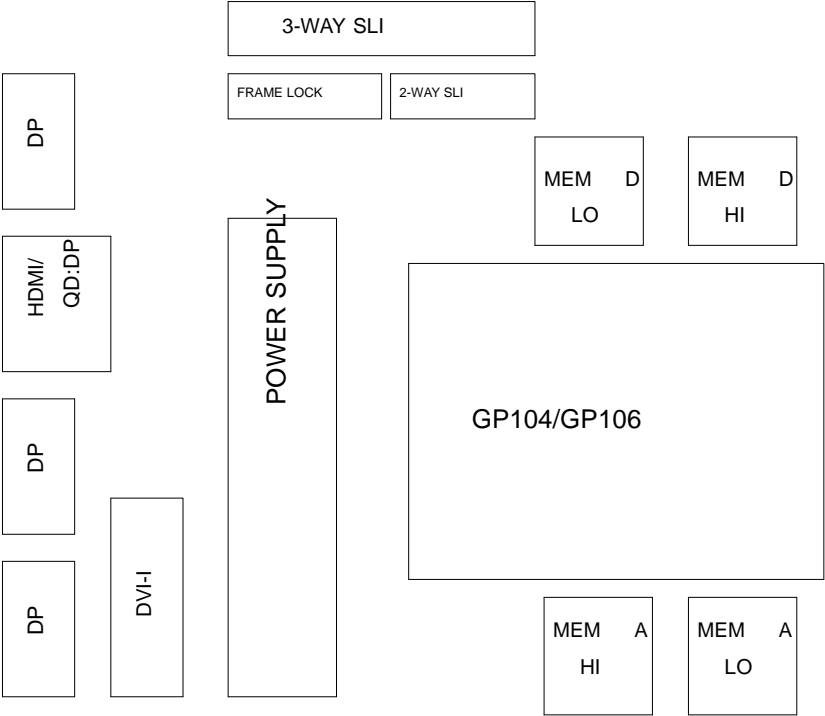
GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI/DP + DP

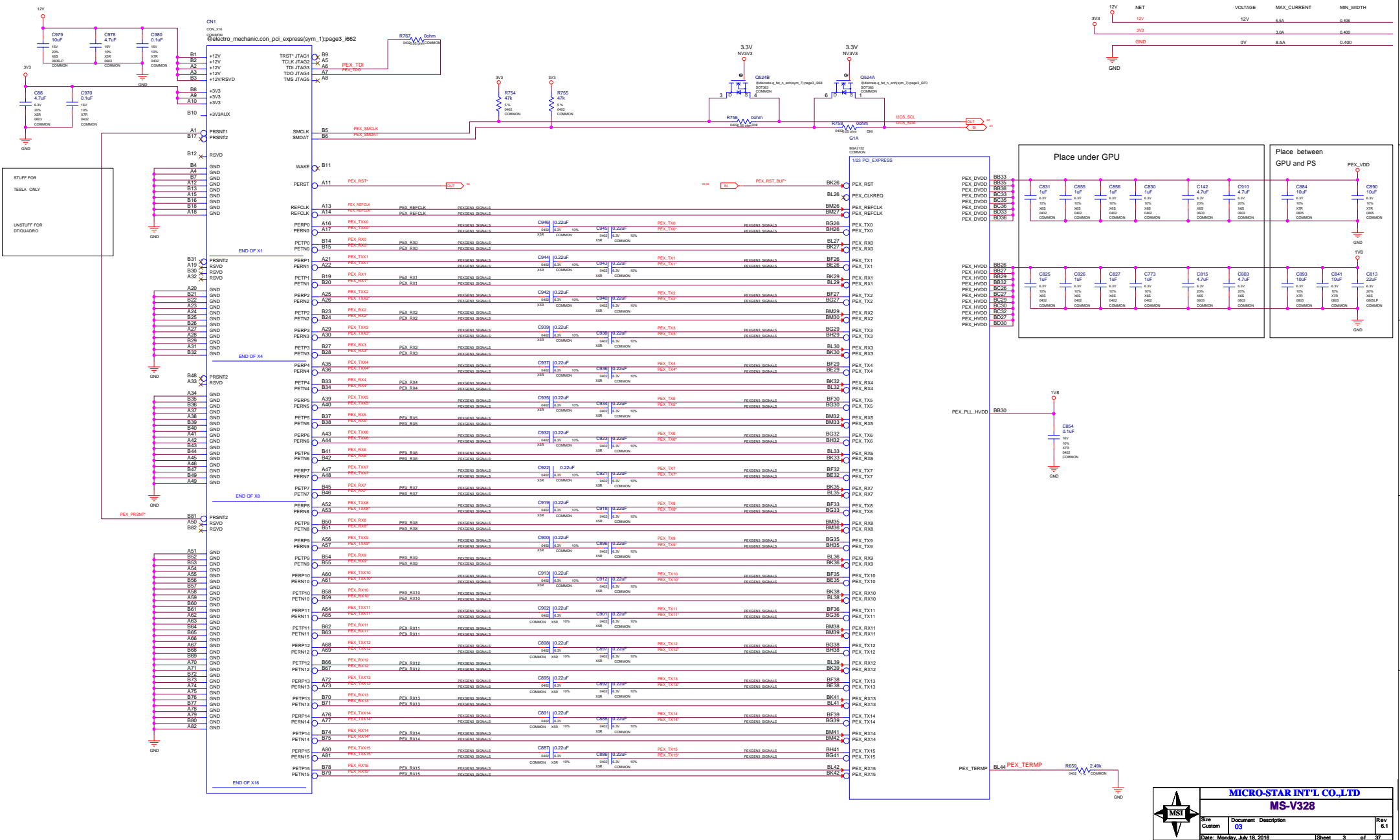
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6.1
1. 1V8_PLL, 1V8_AON
2. 5V, PEX_VDD
3. NV3V3, NV12V
4. FBVDD





GDDR5 CMD Mapping

CMD	9-31	32-63
CMD0	CAS*	
CMD1	CSE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A0	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	AB*	
CMD8	AE_A11	
CMD9	AF_A8	
CMD10	WE*	
CMD11	AE_BA1	
CMD12	AE_BA2	
CMD13	AE_BA3	
CMD14	AE_BA3	
CMD15	CS*	
CMD16	CAS*	
CMD17	RST*	
CMD18	RAS*	
CMD19	A1_A0	
CMD20	A0_A10	
CMD21	A12_RFU	
CMD22	AB*	
CMD23	AE_A11	
CMD24	AF_A8	
CMD25	WE*	
CMD26	AE_BA1	
CMD27	AE_BA2	
CMD28	AE_BA3	
CMD29	CS*	

G1B

8540102

COMMON

253 FBA

FBA_CMD0

FBA_CMD1

FBA_CMD2

FBA_CMD3

FBA_CMD4

FBA_CMD5

FBA_CMD6

FBA_CMD7

FBA_CMD8

FBA_CMD9

FBA_CMD10

FBA_CMD11

FBA_CMD12

FBA_CMD13

FBA_CMD14

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FBA_CMD299

FBA_CMD300

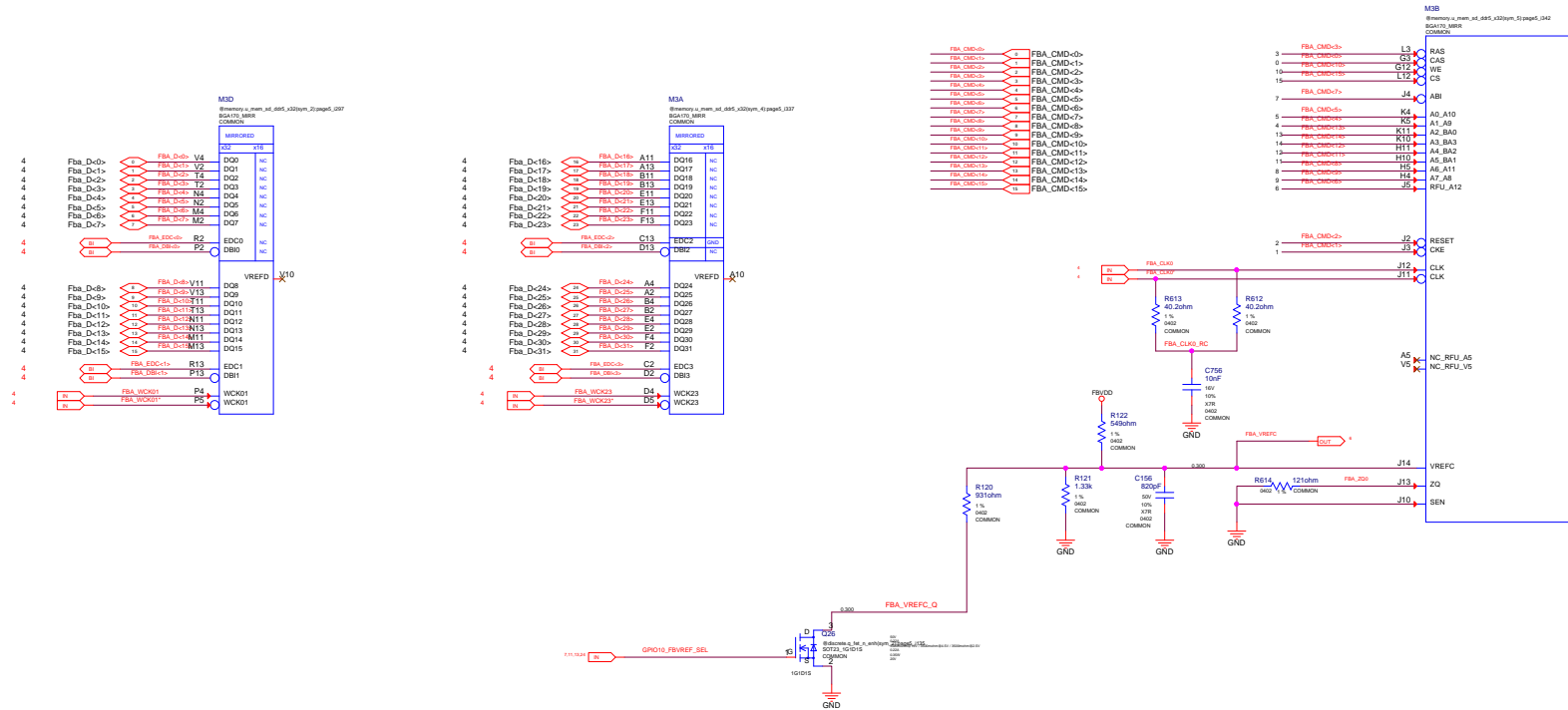
FBA_CMD301

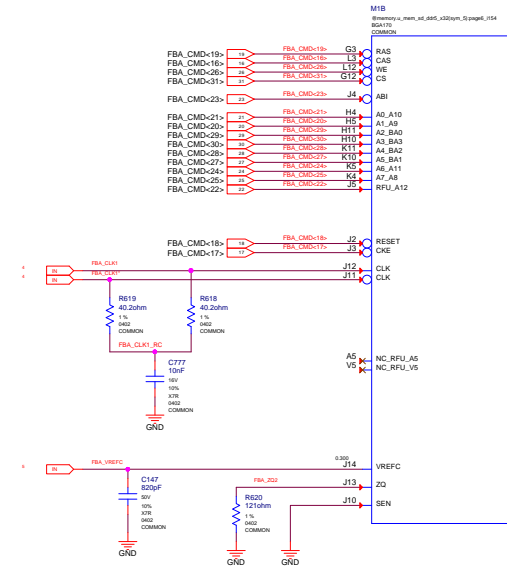
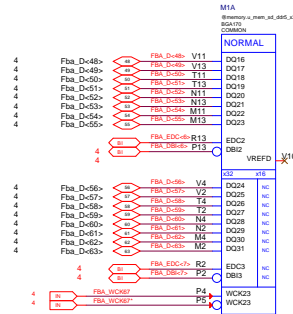
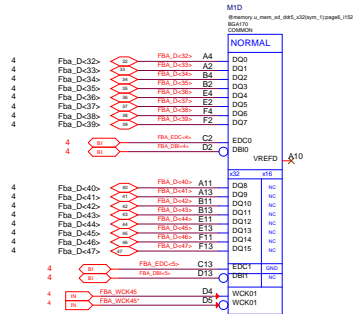
FBA_CMD302

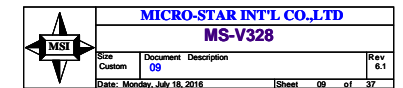
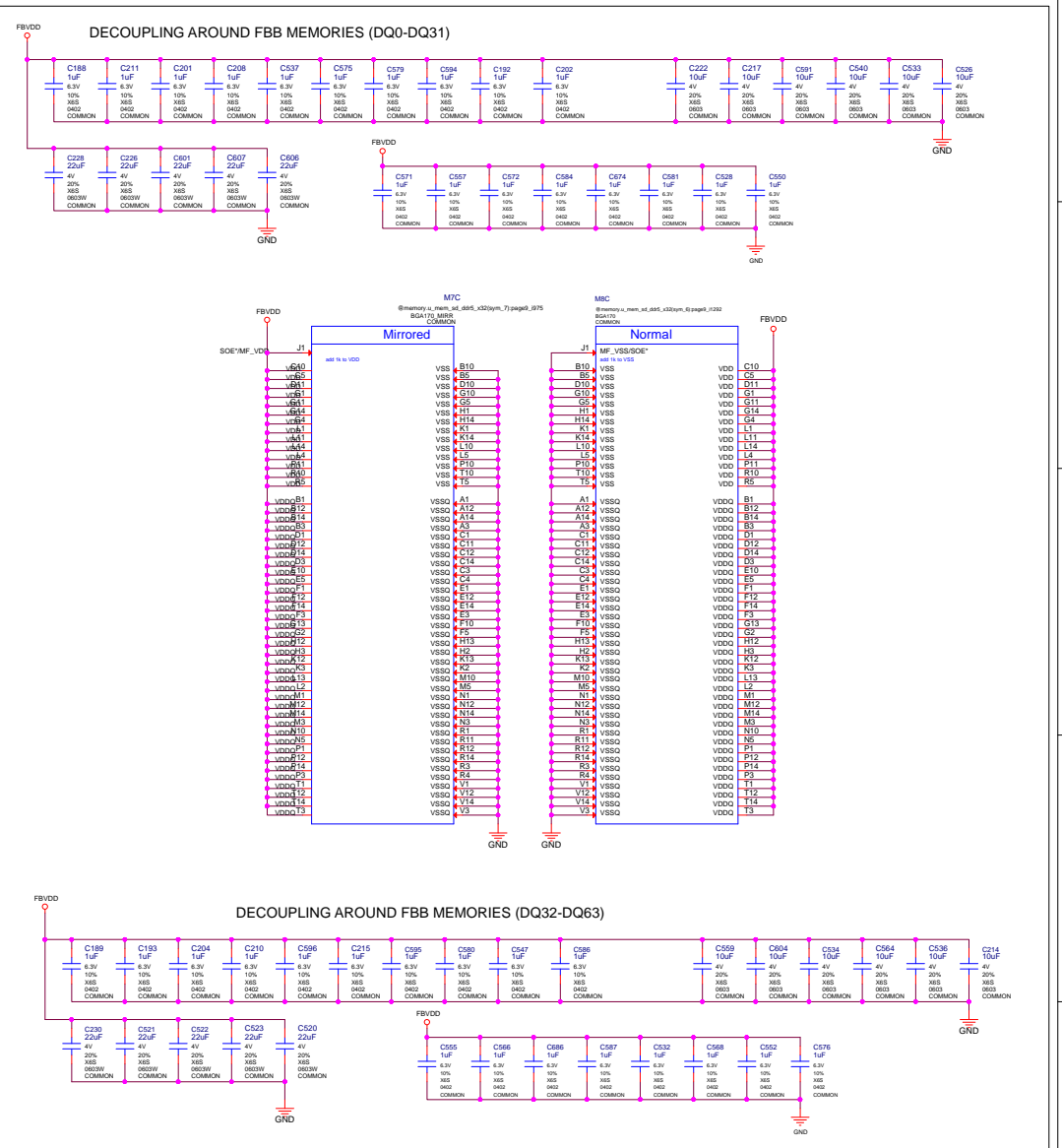
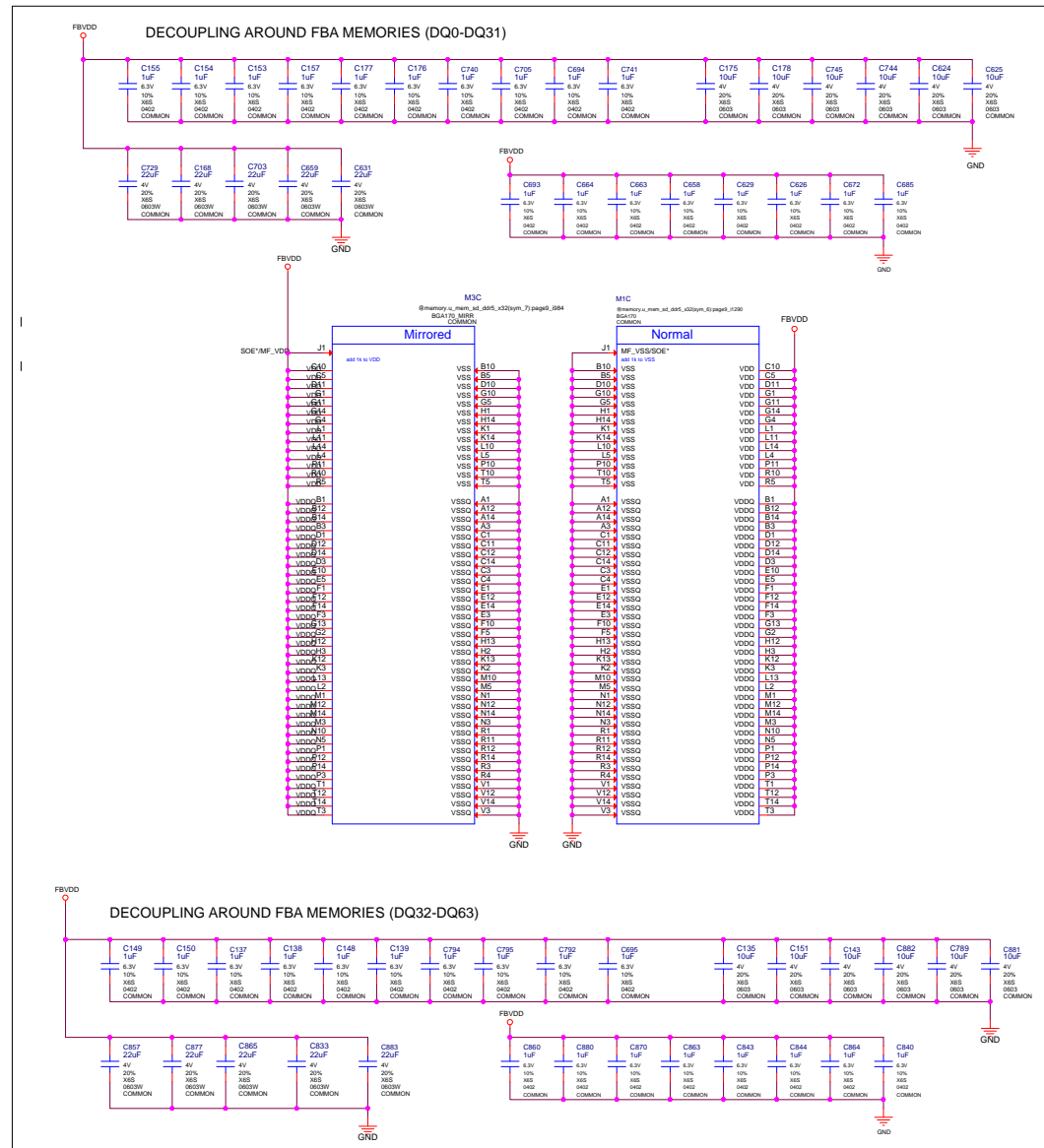
FBA_CMD303

FBA_CMD304

FBA_CMD305

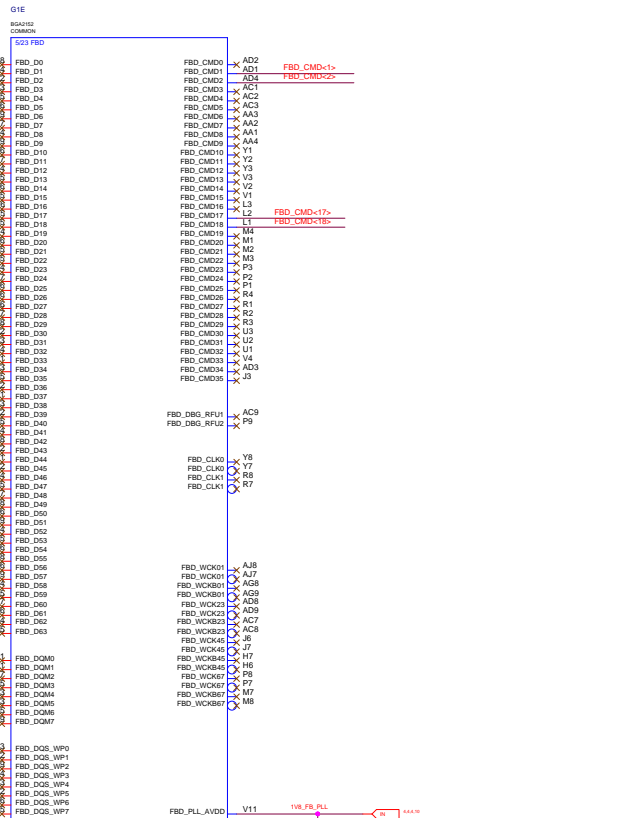
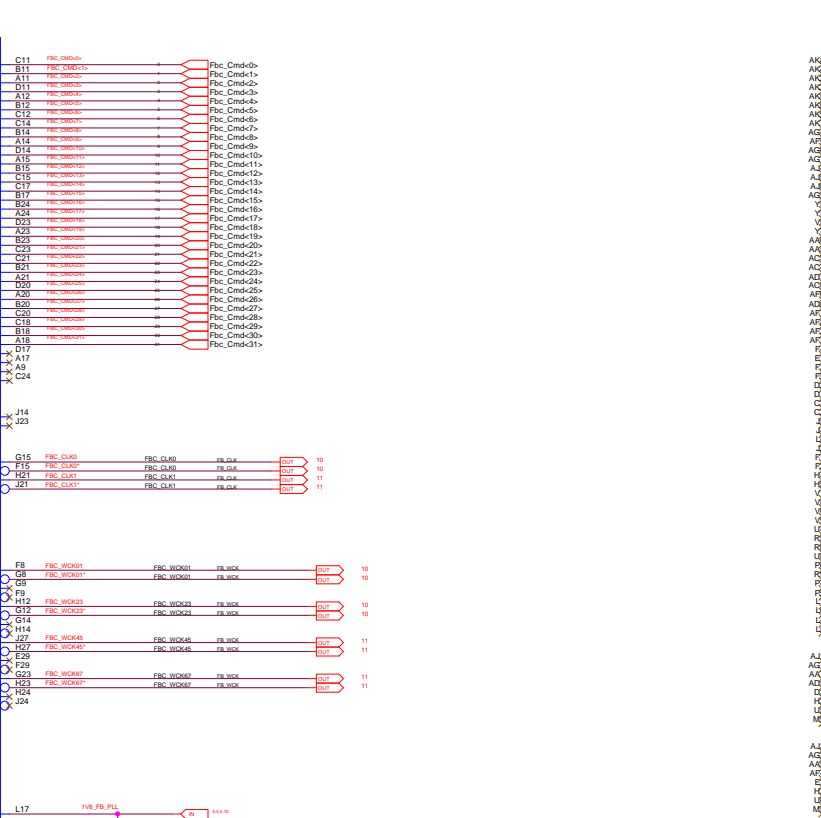
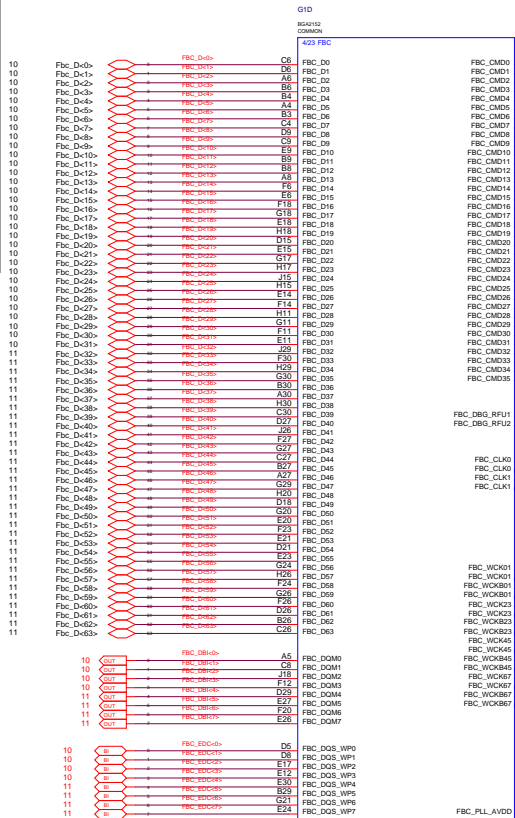


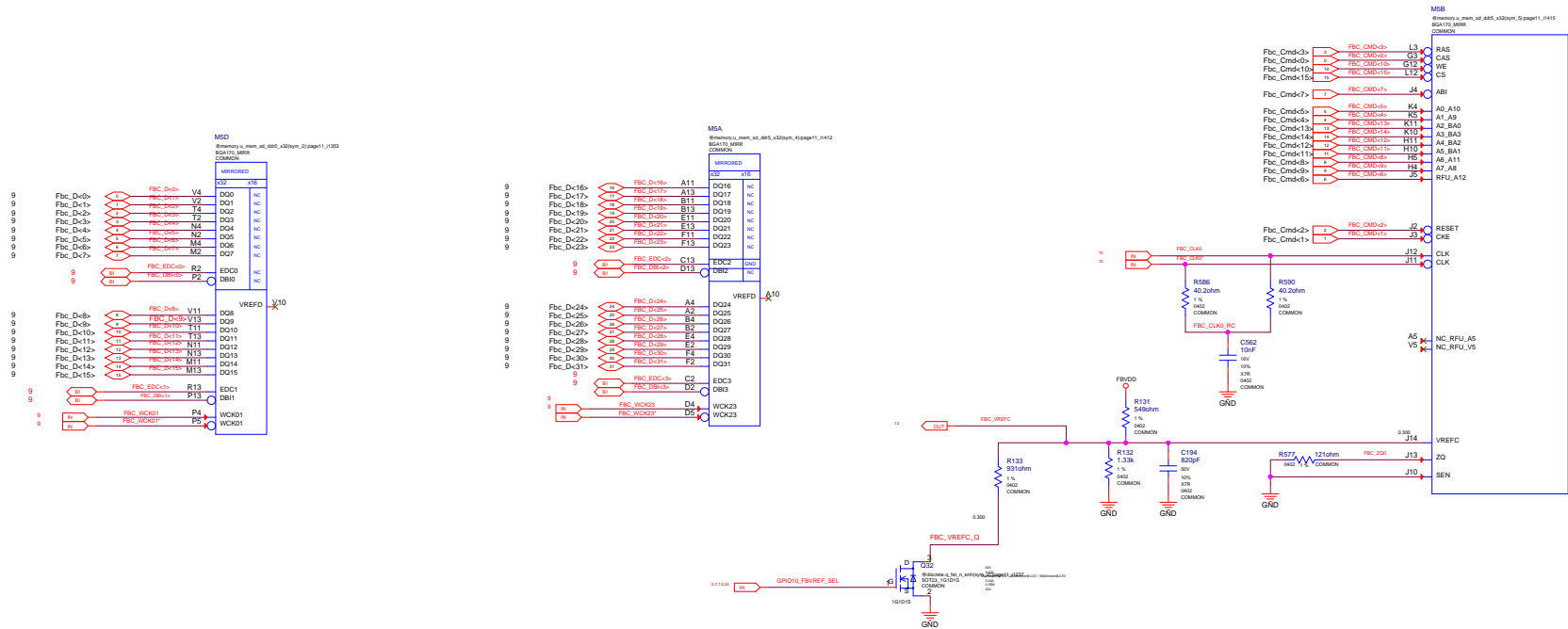





GDDR5 CMD Mapping

CMD	0-31	32-63
CM00	CAS*	
CM01	CKE*	
CM02	RST*	
CM03	RAS*	
CM04	A1_A0	
CM05	A0_A10	
CM06	A12_RFU	
CM07	AB*	
CM08	AB_A11	
CM09	A2_A0	
CM10	WE*	
CM11	A0_A11	
CM12	A0_A10	
CM13	A2_BA0	
CM14	A0_BA3	
CM15	CS*	
CM16		CAS*
CM17		CKE*
CM18		RST*
CM19		AB*
CM20	A1_A0	
CM21	A0_A10	
CM22	A12_RFU	
CM23	AB*	
CM24	AB_A11	
CM25	A2_A0	
CM26	WE*	
CM27	A0_A11	
CM28	A0_A10	
CM29	A2_BA0	
CM30	A0_BA3	
CM31	CS*	








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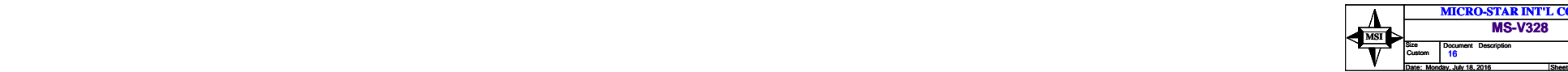
Size	Document	Description	Rev
Custom	13		6.0
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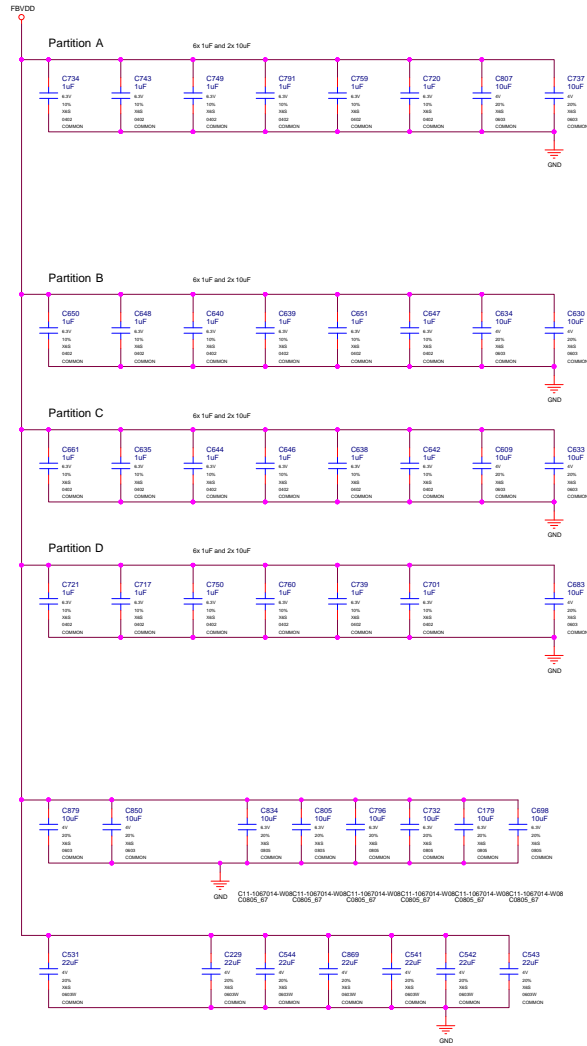
MICRO-STAR INT'L CO.,LTD

MS-V328

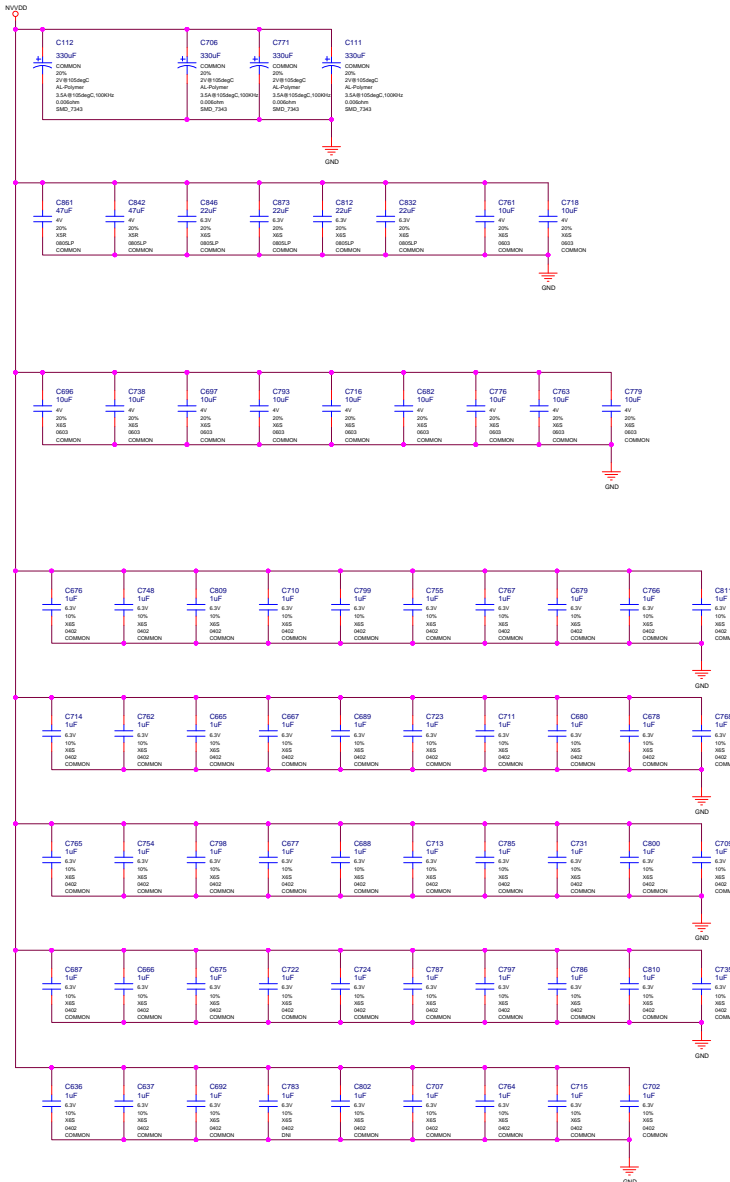
Size	Document	Description	Rev
Custom	14		6.0
Date: Monday, July 18, 2016			Sheet 14 of 37



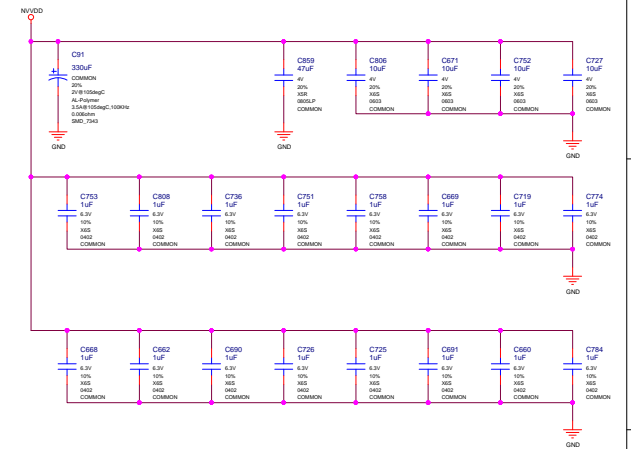
FBVDD



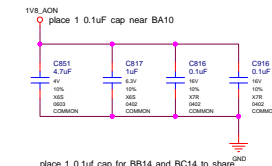
NVVDD



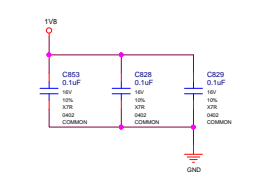
NVVDD

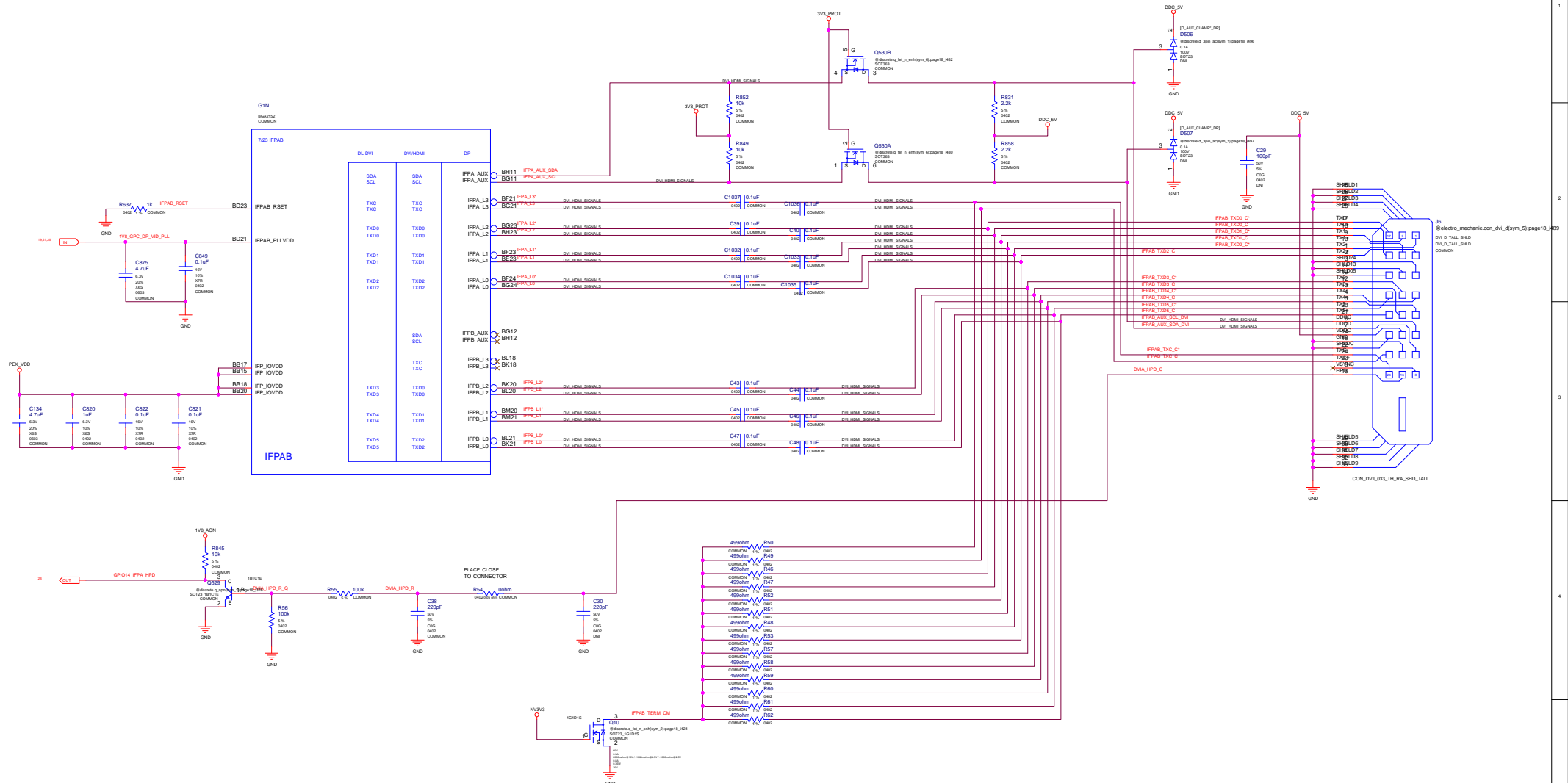


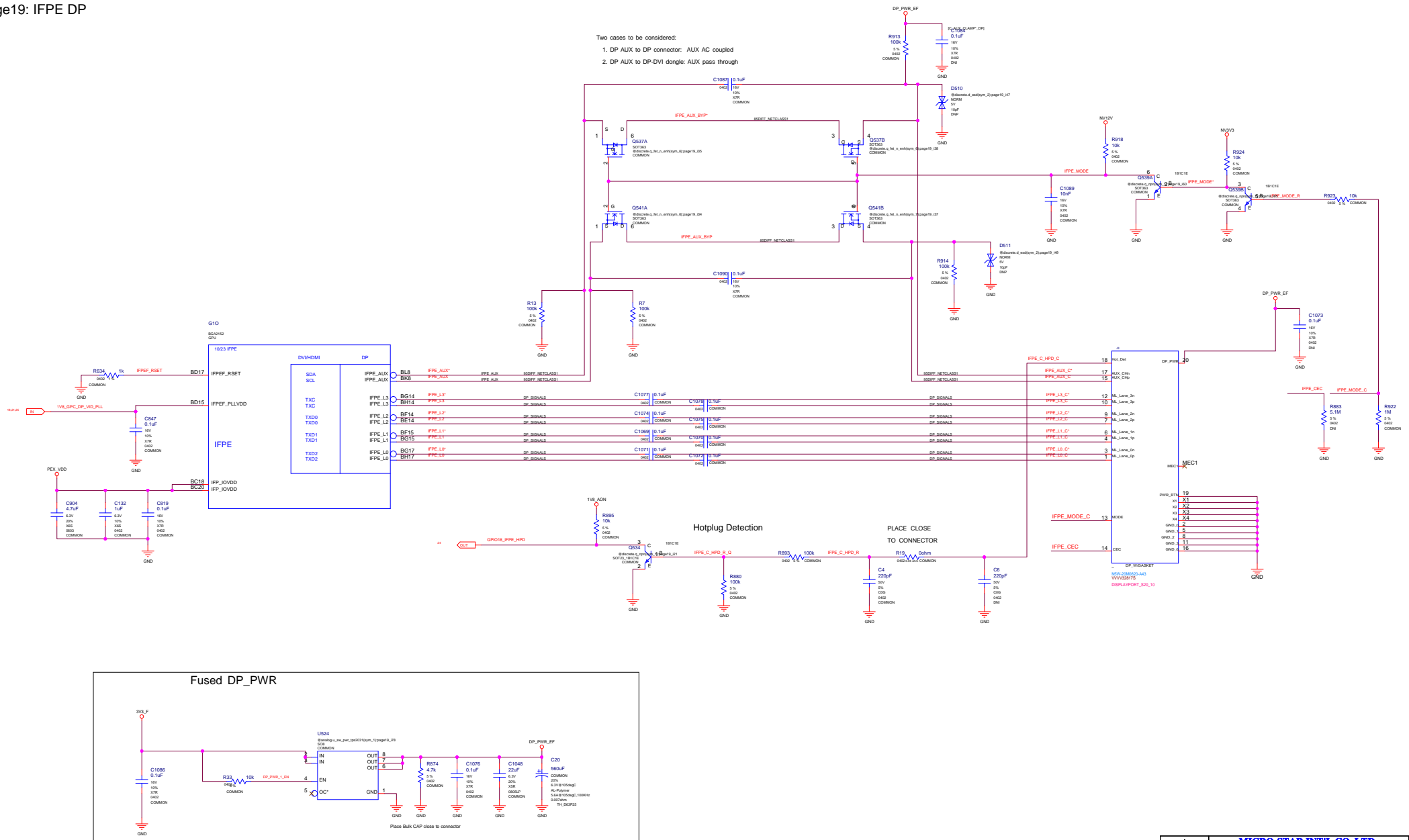
1V8_AON



1V8_MAIN

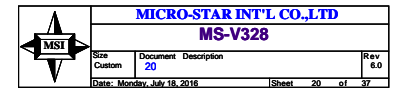
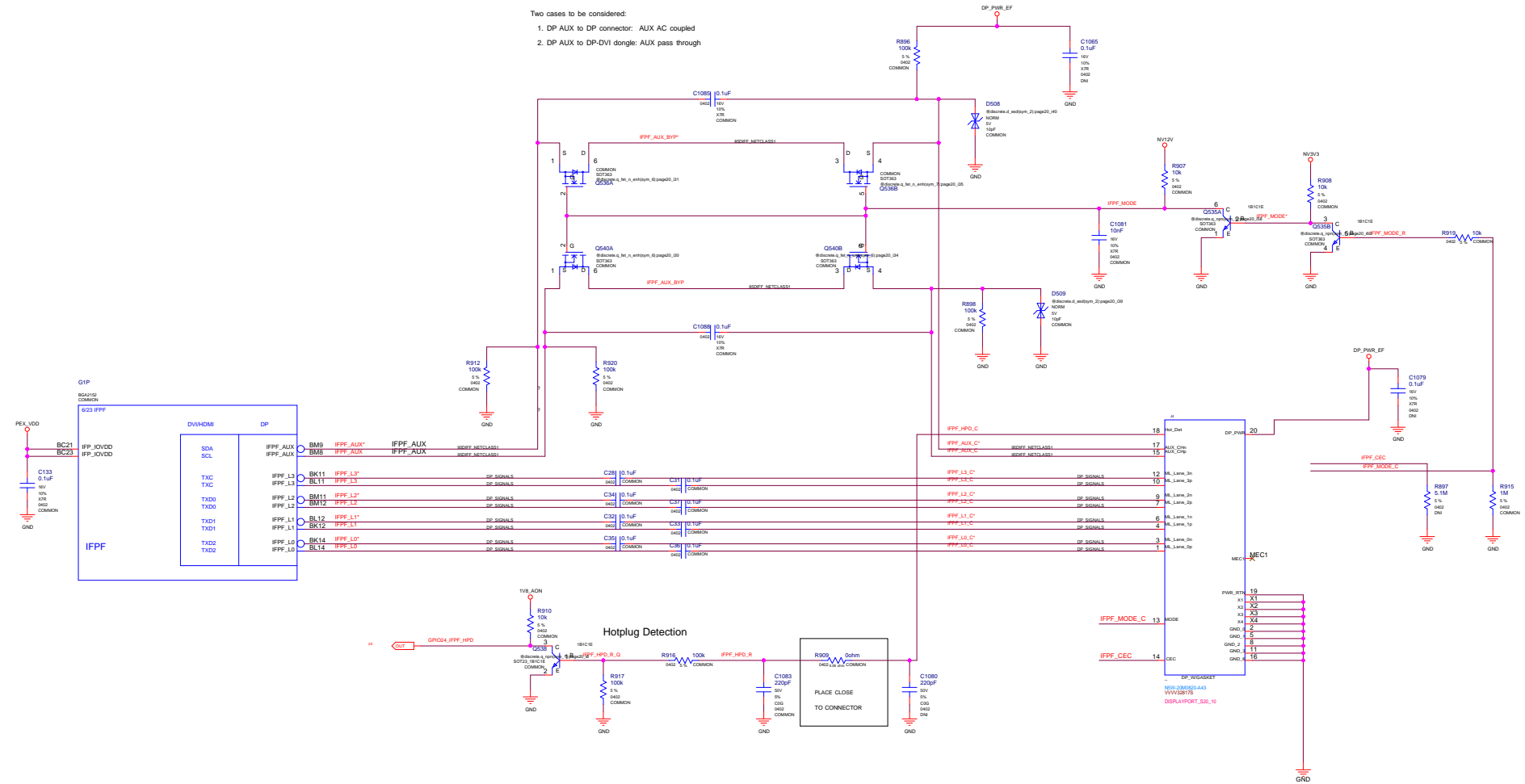


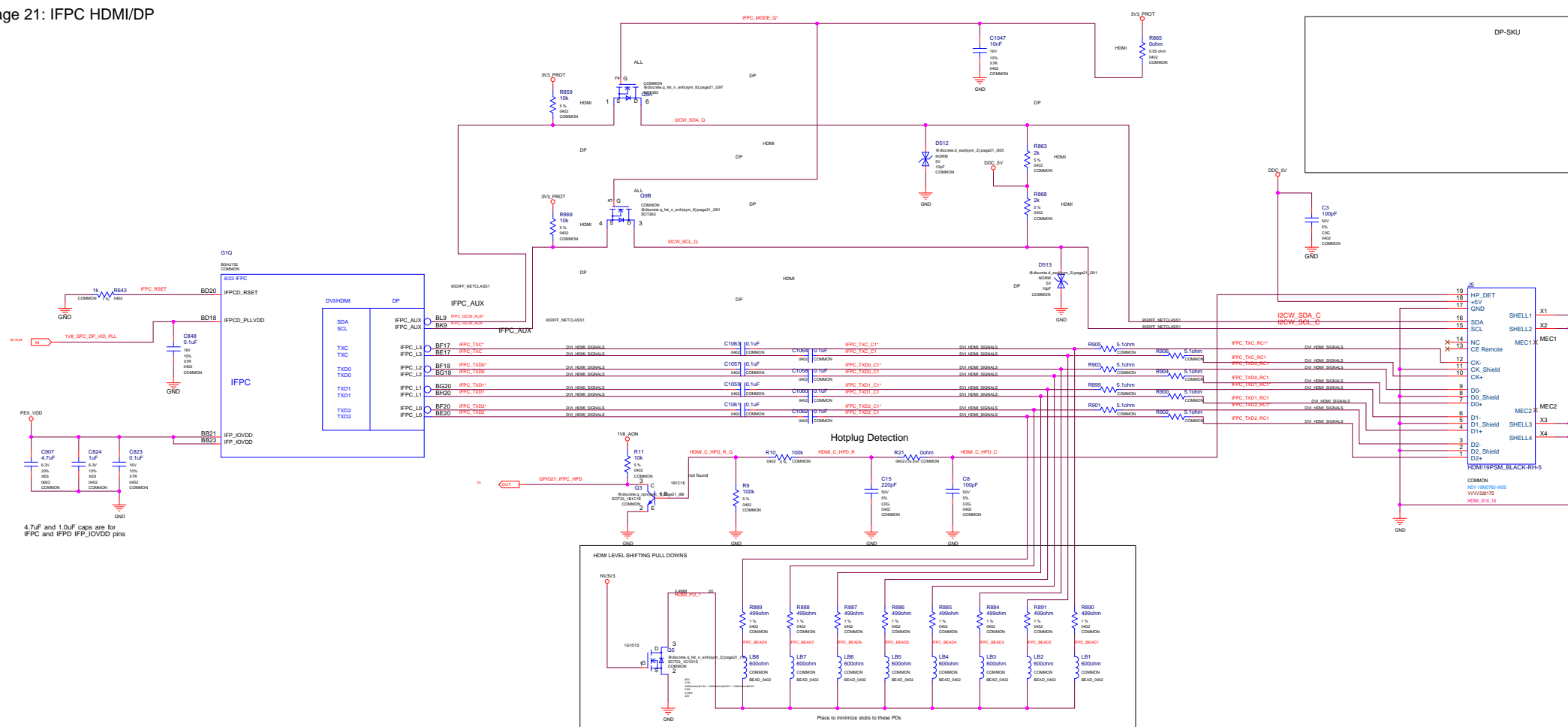




Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



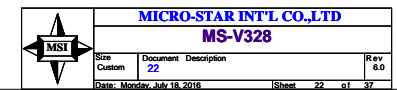
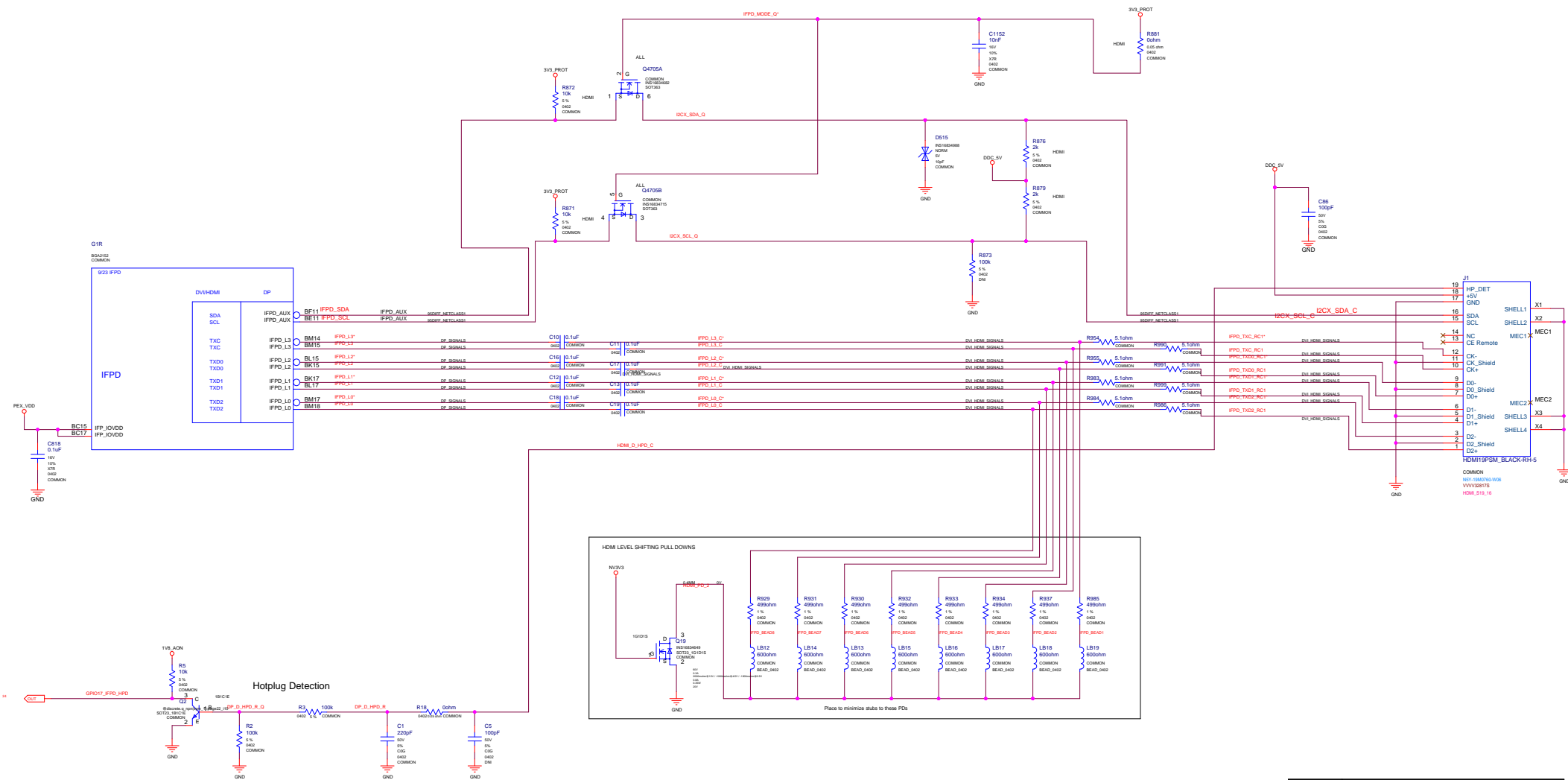


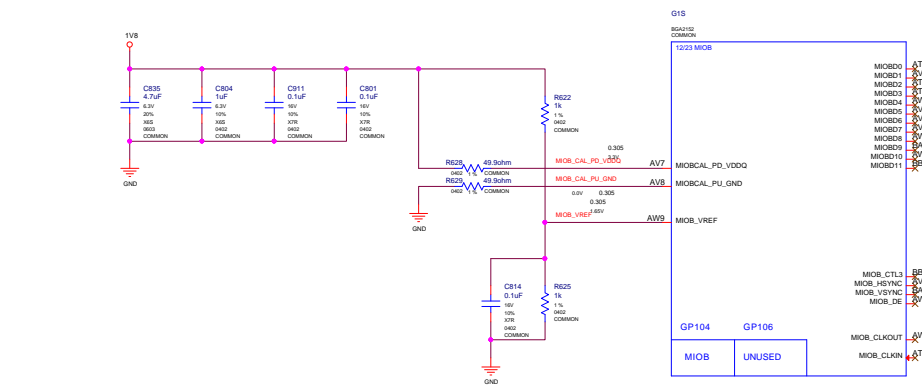
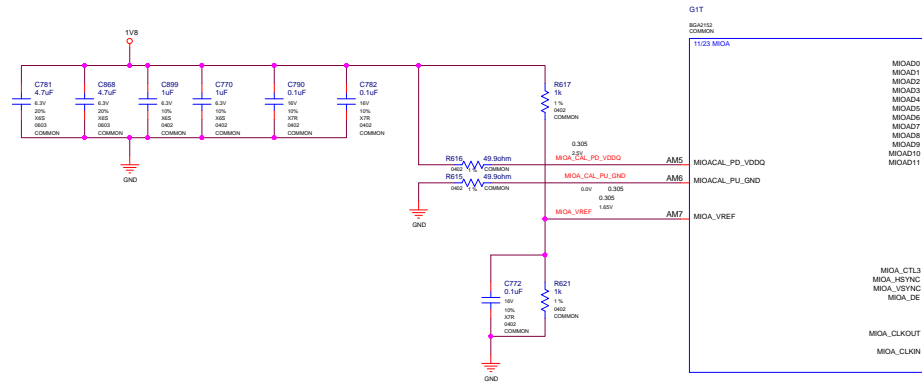
Fused DP_PWR

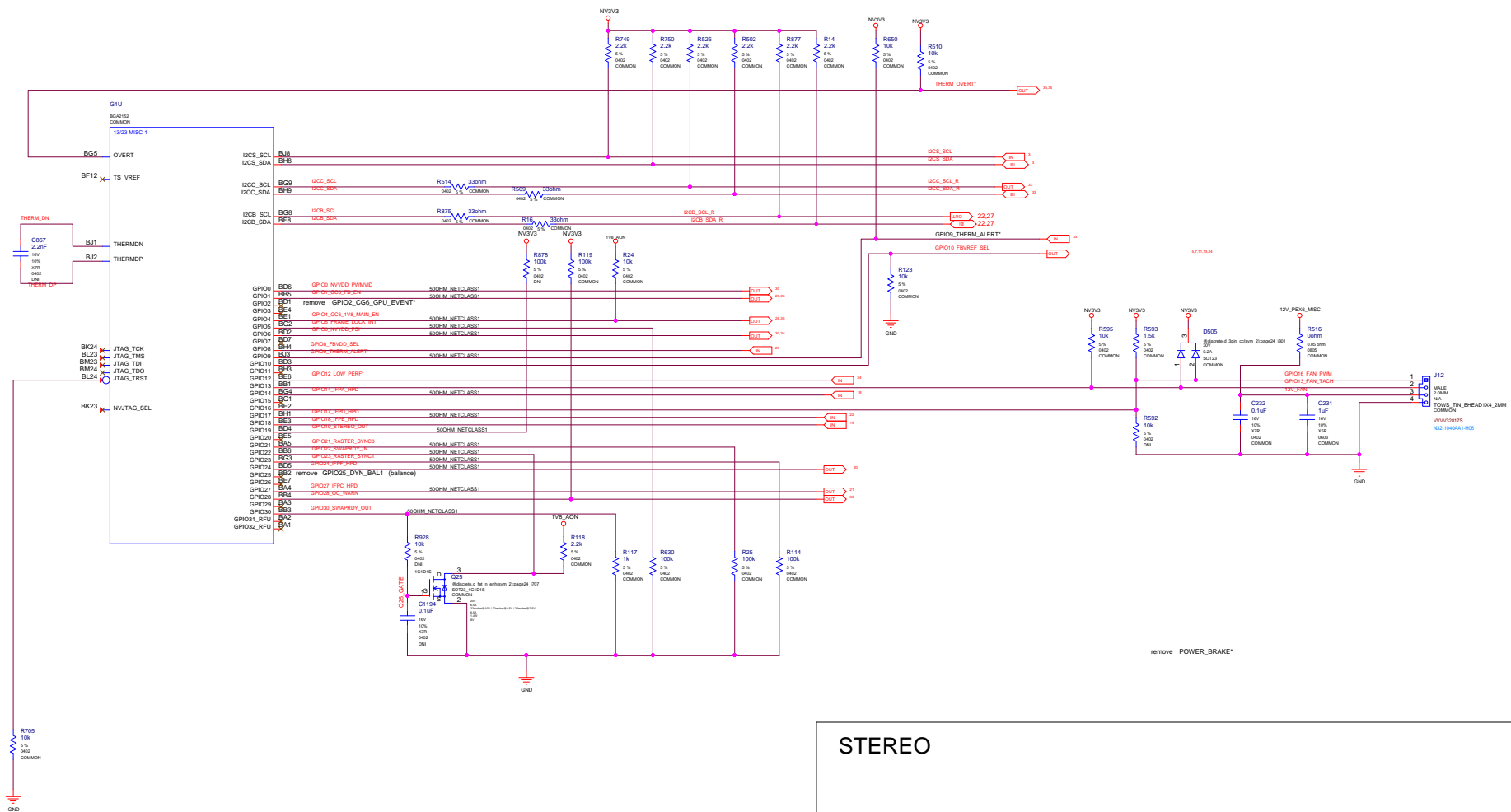


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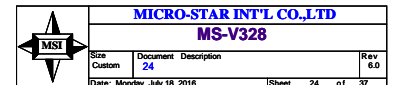
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STEREO



Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

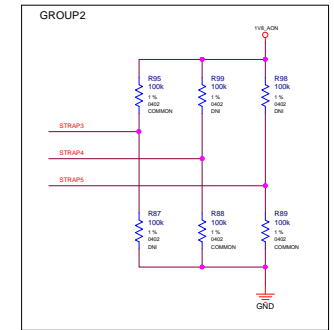
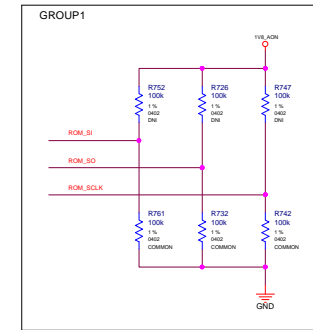
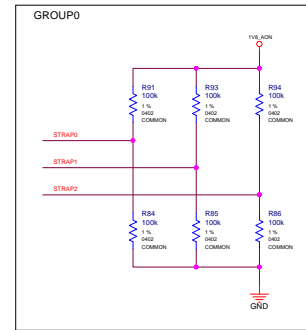
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	0	0	0
L	H	M	1	0	1	1
L	M	H	1	0	0	0
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

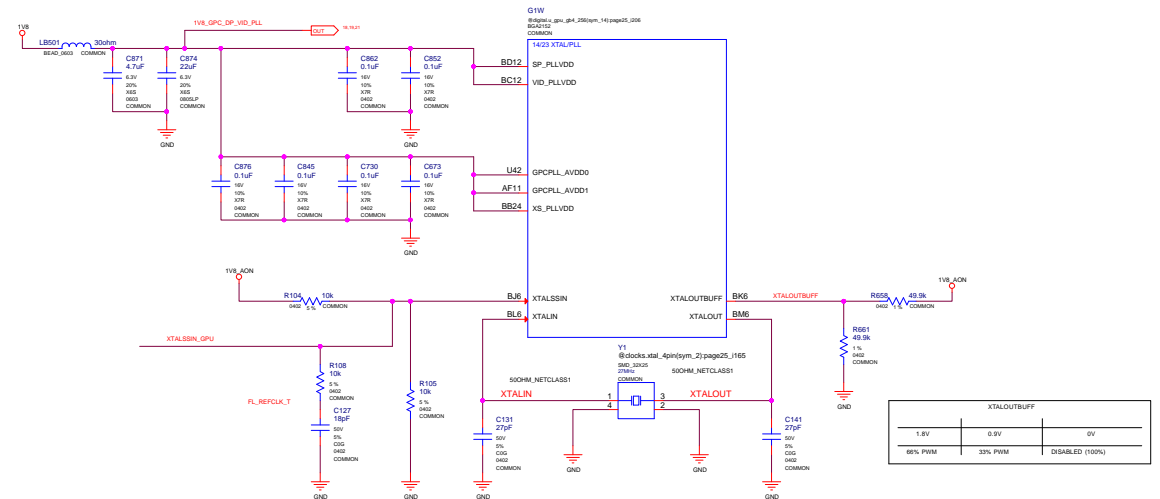
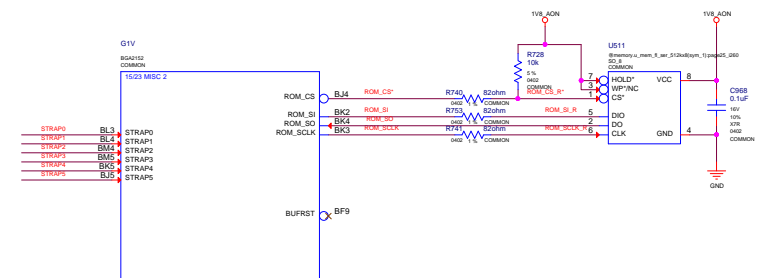
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

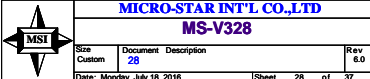
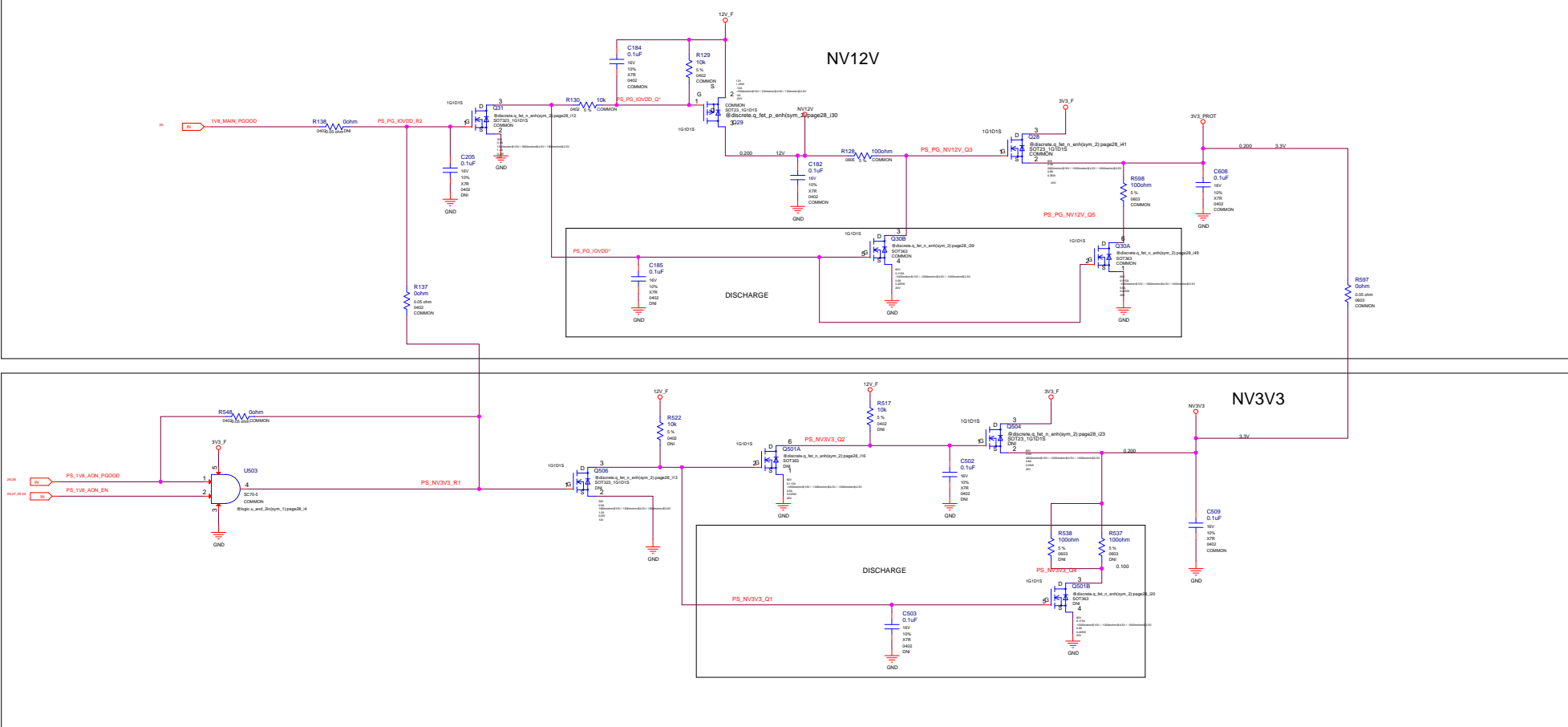


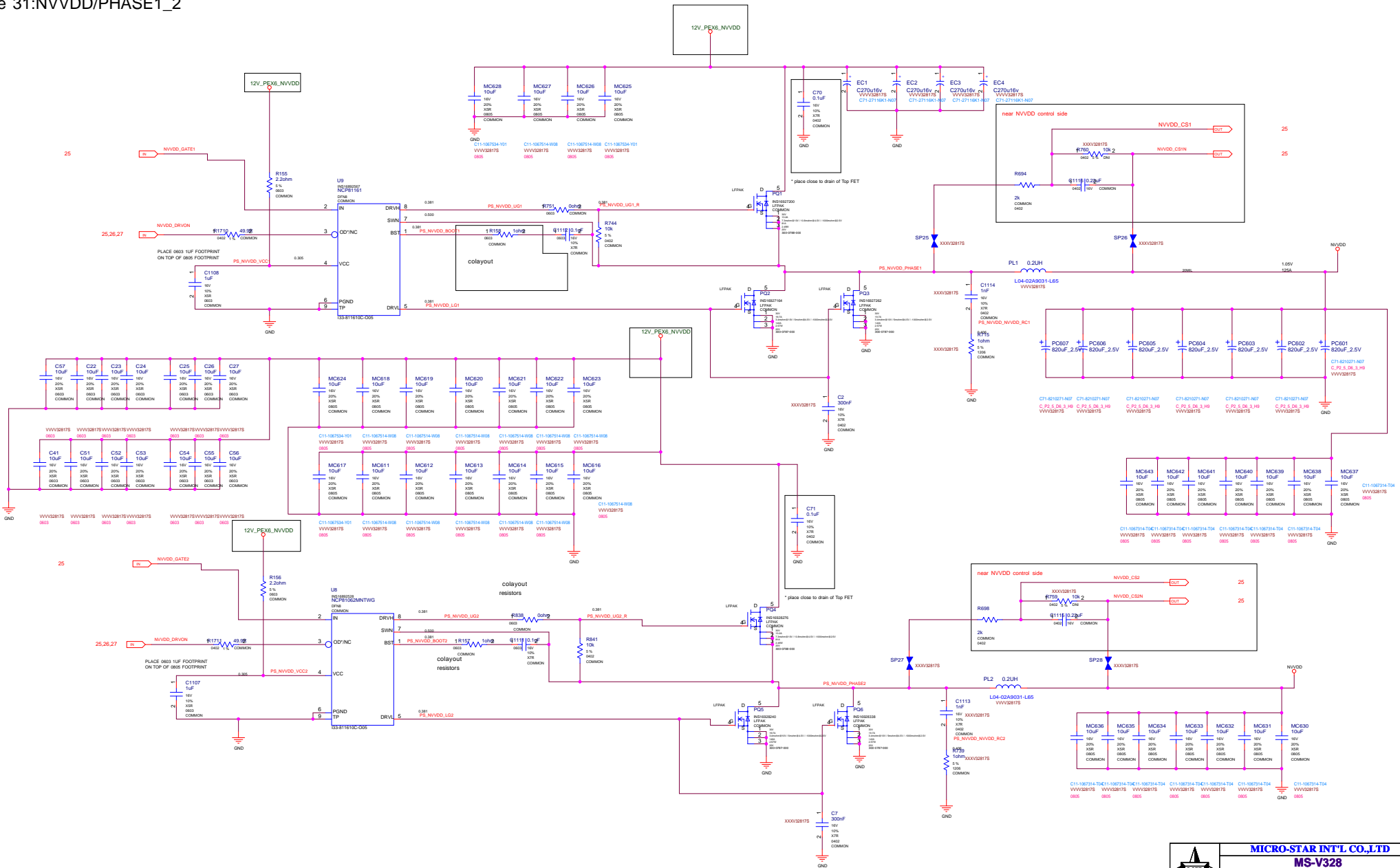
CFG(3:0)	Config	Width	Vendor
0000	256Mx32	256-bit	Samsung
0001	256Mx32	256-bit	Micron
0010	256Mx32	256-bit	Hynix
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		

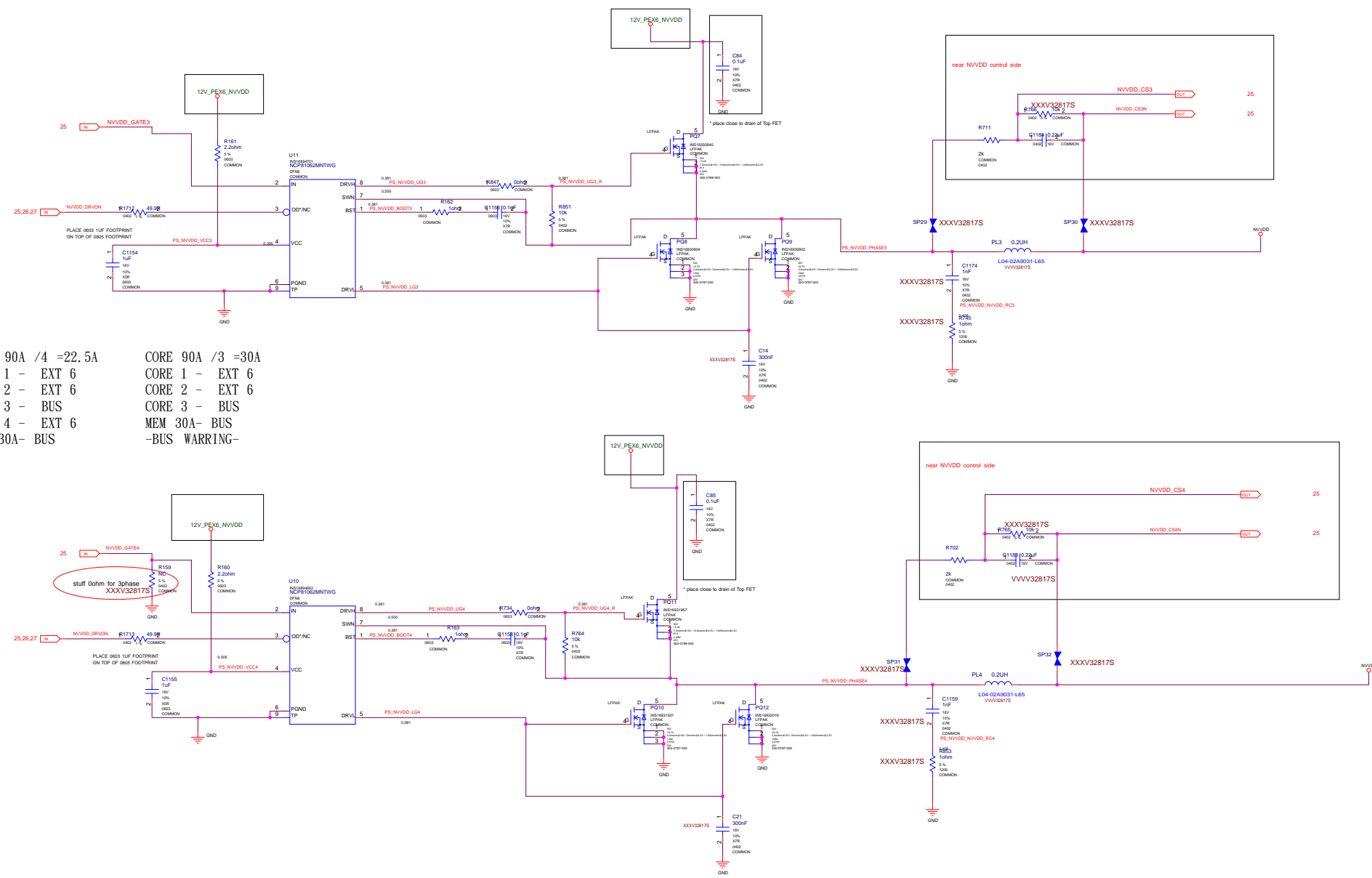


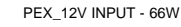
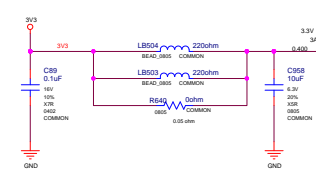
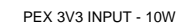
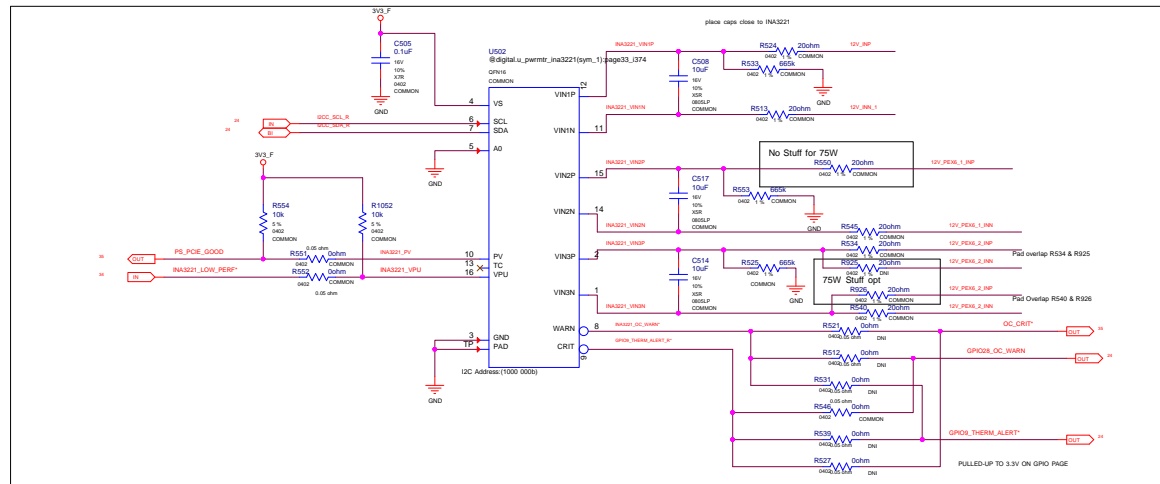
XTALOUTBUFF		
1.8V	0.9V	0V
80% PWM	33% PWM	DISABLED (100%)

MICRO-STAR INT'L CO.,LTD			
MS-V328			
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Custom	25		6.0
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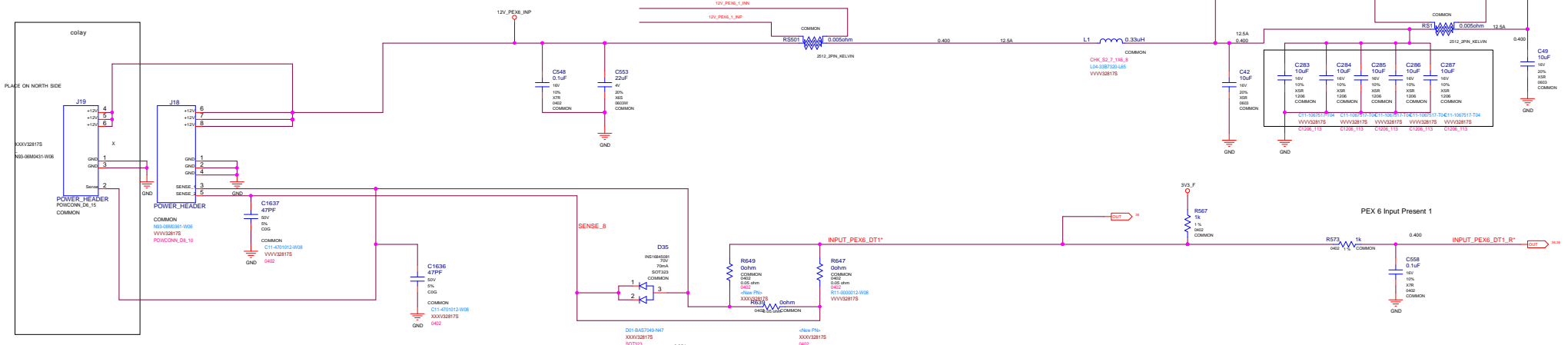








PEX6 INPUT 1 - 2x3 PCIE CON 75W

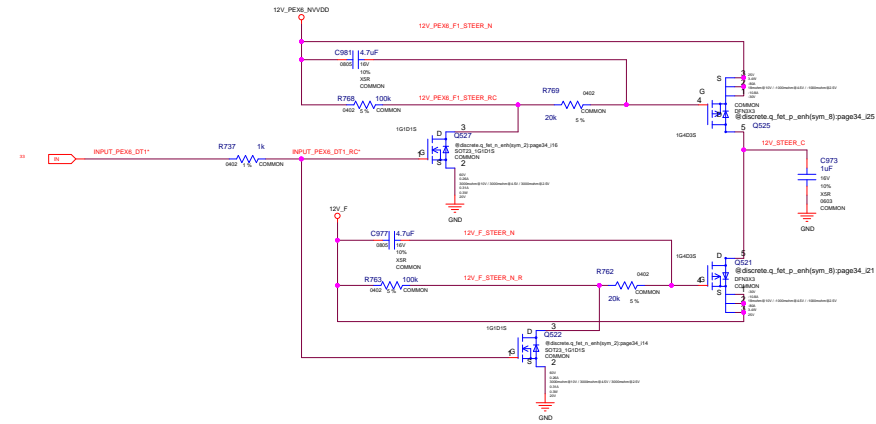


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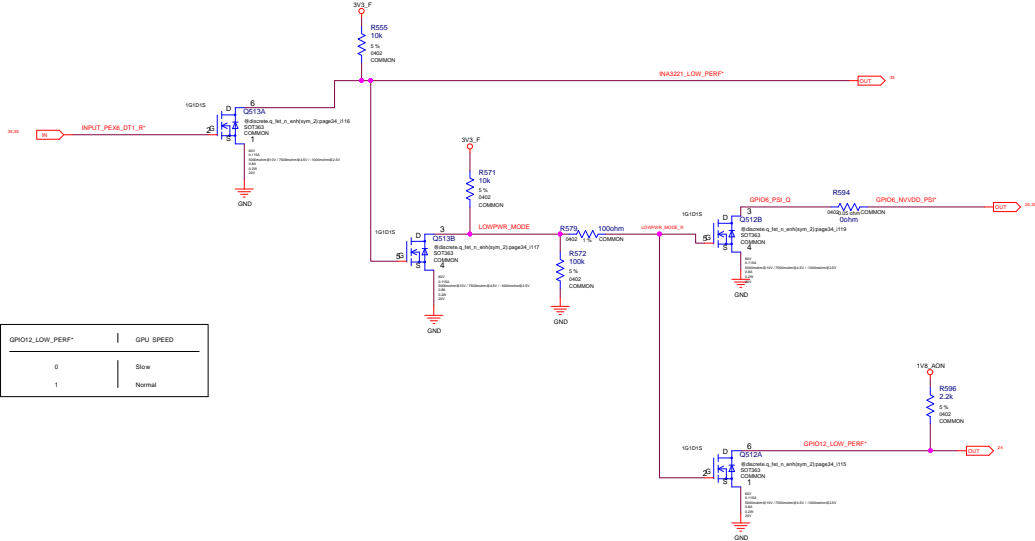
Size Custom	Document Description 33	Rev 6.
Date: Monday, July 18, 2016		Sheet 33 of 37

12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



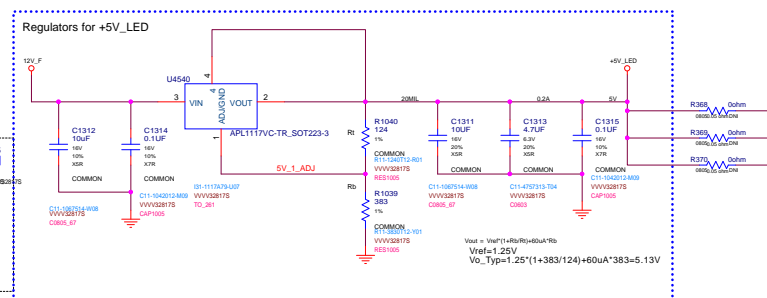
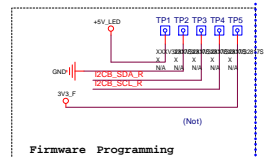
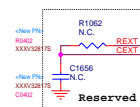
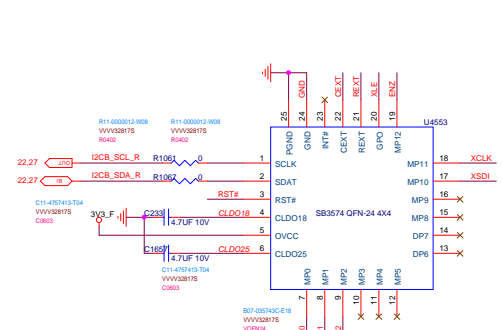
PEX Input - Power Level/PSI* Control



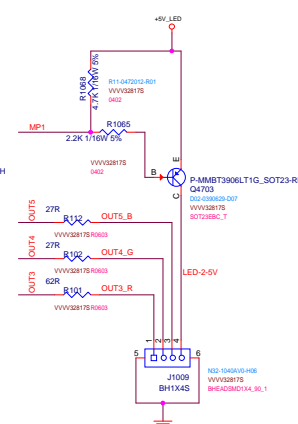
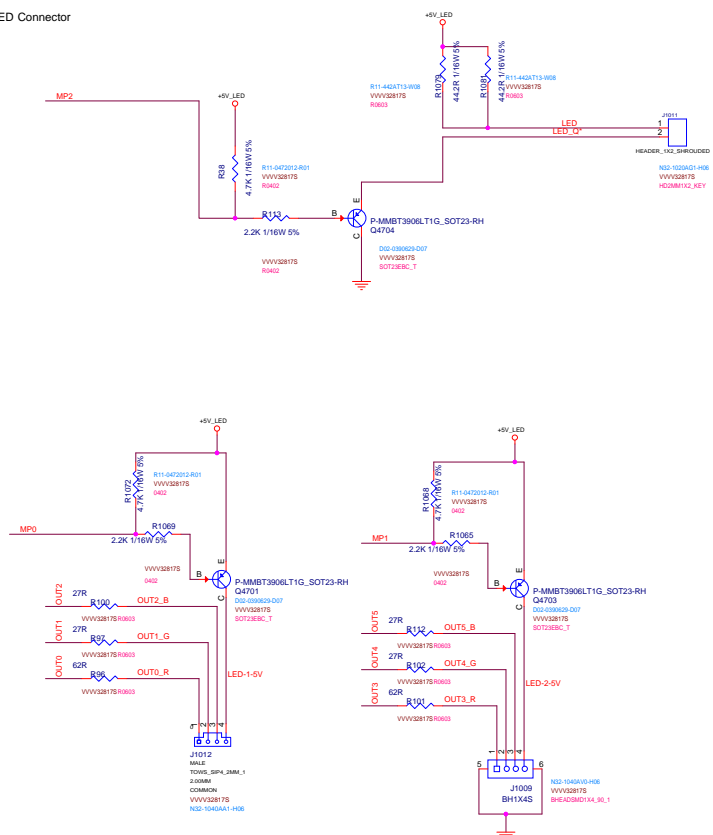
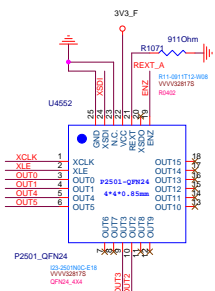
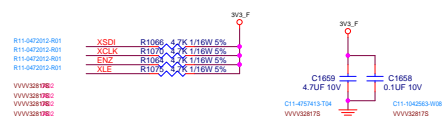
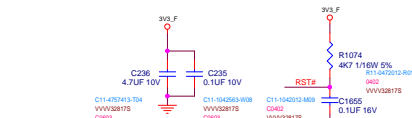
GPIO12_LOW_PERP*	GPU SPEED
0	Slow
1	Normal

GeForce Logo LED


```
remove GC6 FB ENABLE
remove GPU_EVENT*
remove PEX_CLKREQ*
PEX_RST# LOGIC
```

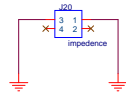
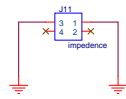
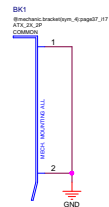


LED Connector

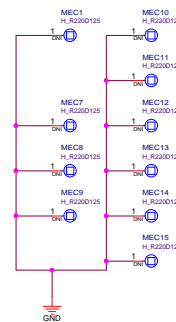


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Brackets:



Mechanical Holes Symbol



GPU Stiffner

