NAVI23 GDDR6 4PCS,8L DP/USB-C + DP + HDMI + DP

105-D532xx-00 Rev00B Desktop board(120W TGP)

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21	GFX & SOC CONTROLLER		
22	VDDCR_GFX PHASES 2 and 5		
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Size Custom
Document Description 0001 TOC
Rev 2.0
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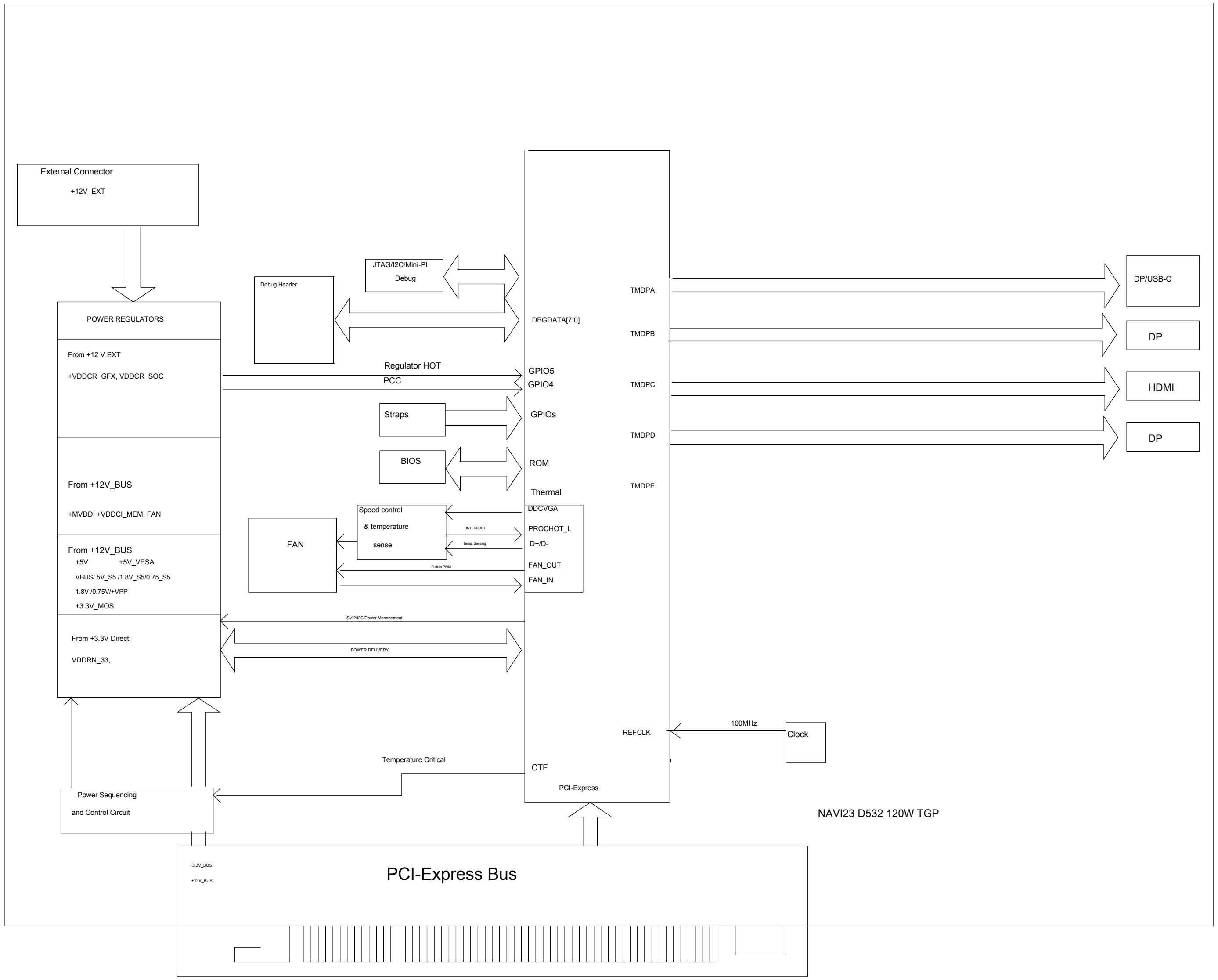
External Connector
+12V_EXT
POWER REGULATORS
From +12 V EXT
+VDDCR_GFX, VDDCR_SOC
From +12V_BUS
+MVDD, +VDDCI_MEM, FAN
From +12V_BUS
+5V
+5V_VESA
VBUS/ 5V_S5./1.8V_S5/0.75_S5
1.8V /0.75V/+VPP
+3.3V_MOS
From +3.3V Direct:
VDDRN_33,
Power Sequencing
and Control Circuit
Debug Header
JTAG/I2C/Mini-PI
Debug
Regulator HOT
PCC
Straps
BIOS
Speed control
& temperature
sense
FAN
INTERRUPT
Temp. Sensing
Built-in PWM
SVI2/I2C/Power Management
POWER DELIVERY
Temperature Critical
DBGDATA[7:0]
GPIO5
GPIO4
GPIOs
ROM
Thermal
DDCVGA
PROCHOT_L
D+/D-
FAN_OUT
FAN_IN
CTF
PCI-Express
TMDPA
TMDPB
TMDPC
TMDPD
TMDPE
REFCLK
100MHz
Clock
DP/USB-C
DP
HDMI
DP
NAVI23 D532 120W TGP
+3.3V_BUS
+12V_BUS
PCI-Express Bus

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Custom

Document Description
0002 BLOCK DIAGRAM

Rev
2.0

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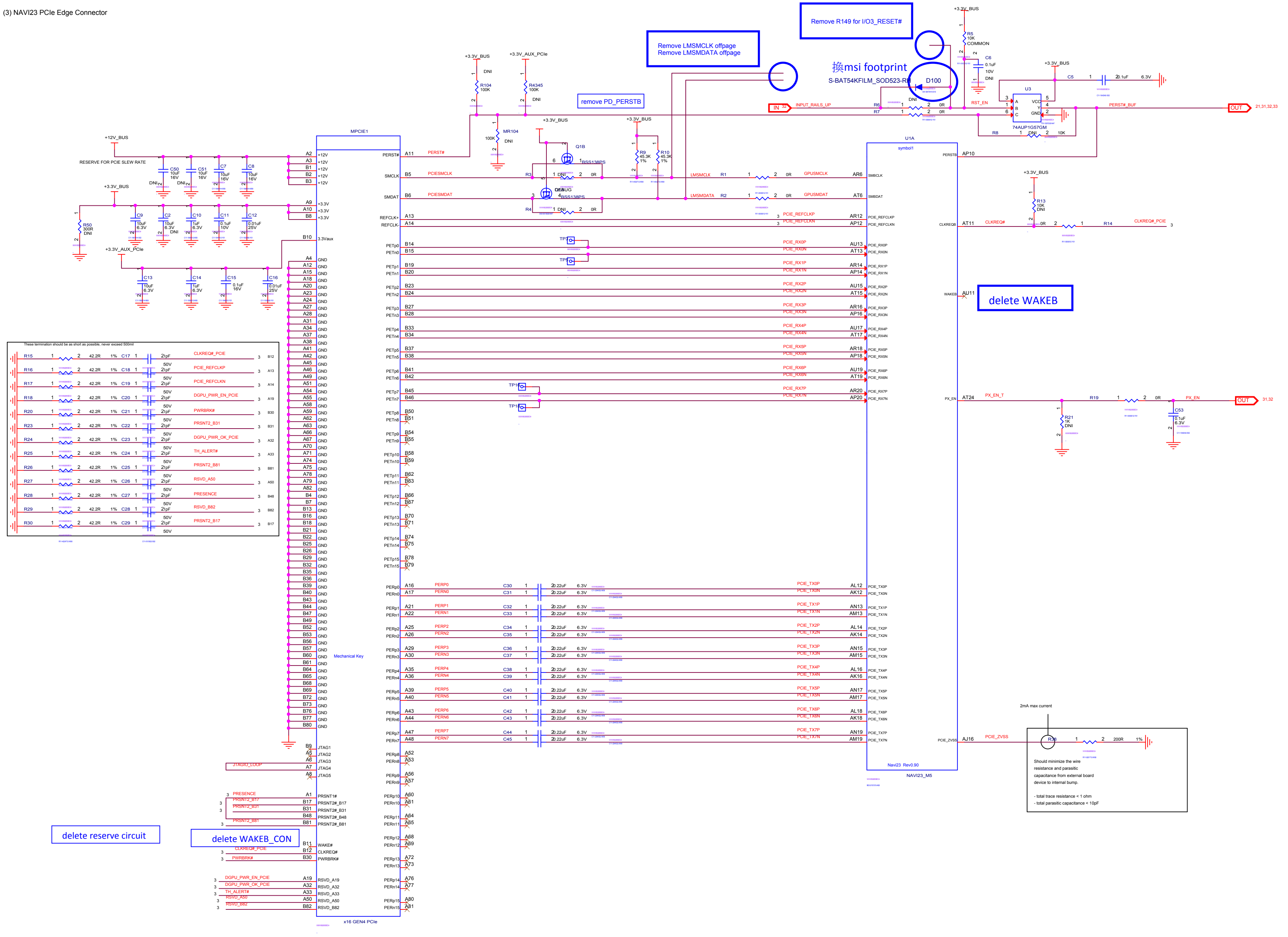
(3) NAVI23 PCIe Edge Connector


MPCIE1
x16 GEN4 PCIe
Mechanical Key
+12V_BUS
RESERVE FOR PCIE SLEW RATE
C50 10uF 16V DNI
C51 10uF 16V DNI
C7 10uF 16V
C8 10uF 16V
+3.3V_BUS
R50 300R DNI
C9 10uF 6.3V
C2 10uF 6.3V DNI
C10 1uF 6.3V
C11 0.1uF 10V
C12 0.01uF 25V
+3.3V_AUX_PCIe
C13 10uF 6.3V
C14 1uF 6.3V
C15 0.1uF 16V
C16 0.01uF 25V
These termination should be as short as possible, never exceed 500mil
R15 42.2R 1% C17 1pF 50V CLKREQ#_PCIE B12
R16 42.2R 1% C18 1pF 50V PCIE_REFCLKP A13
R17 42.2R 1% C19 1pF 50V PCIE_REFCLKN A14
R18 42.2R 1% C20 1pF 50V DGPU_PWR_EN_PCIE A19
R20 42.2R 1% C21 1pF 50V PWRBRK# B30
R23 42.2R 1% C22 1pF 50V PRSNT2_B31 B31
R24 42.2R 1% C23 1pF 50V DGPU_PWR_OK_PCIE A32
R25 42.2R 1% C24 1pF 50V TH_ALERT# A33
R26 42.2R 1% C25 1pF 50V PRSNT2_B81 B81
R27 42.2R 1% C26 1pF 50V RSVD_A50 A50
R28 42.2R 1% C27 1pF 50V PRESENCE B48
R29 42.2R 1% C28 1pF 50V RSVD_B82 B82
R30 42.2R 1% C29 1pF 50V PRSNT2_B17 B17
+12V A2 A3 B1 B2 B3
+3.3V A9 A10 B8
3.3Vaux B10
GND
JTAG1 B9, JTAG2 A5, JTAG3 A6, JTAG4 A7, JTAG5 A8
JTAGIO_LOOP
PRSNT1# A1 PRESENCE
PRSNT2#_B17 PRSNT2#_B31 PRSNT2#_B48 PRSNT2#_B81
WAKE# B11
CLKREQ# B12 CLKREQ#_PCIE
PWRBRK# B30 PWRBRK#
RSVD_A19 DGPU_PWR_EN_PCIE
RSVD_A32 DGPU_PWR_OK_PCIE
RSVD_A33 TH_ALERT#
RSVD_A50 RSVD_A50
RSVD_B82 RSVD_B82
PERST# A11 PERST#
SMCLK B5 PCIESMCLK
SMDAT B6 PCIESMDAT
REFCLK+ A13 REFCLK- A14
PETp0–PETn15
PERp0–PERn15
PERP0–PERP7 PERN0–PERN7
C30–C45 0.22uF 6.3V
+3.3V_BUS R104 100K DNI
+3.3V_AUX_PCIe R4345 100K DNI
MR104 100K DNI
Q1B BSS138PS
Q1A BSS138PS
DEBUG
R3 DNI 0R
R4 DNI 0R
R9 45.3K 1%
R10 45.3K 1%
LMSMCLK R1 0R GPUSMCLK
LMSMDATA R2 0R GPUSMDAT
TP3 TP5 TP16 TP18
IN 32 INPUT_RAILS_UP
R6 DNI 0R
R7 0R
D100
R5 10K COMMON
C6 0.1uF 10V DNI
RST_EN
U3 74AUP1G57GM
C5 0.1uF 6.3V
R8 DNI 10K
PERST#_BUF OUT 21,31,32,33
U1A symbol1
Navi23 Rev0.90
NAVI23_M5
PERSTB AP10
SMBCLK AR6
SMBDAT AT6
PCIE_REFCLKP AR12
PCIE_REFCLKN AP12
PCIE_RX0P–PCIE_RX7N
PCIE_TX0P–PCIE_TX7N
CLKREQB AT11 CLKREQ#
R13 10K DNI
R14 0R CLKREQ#_PCIE
WAKEB AU11
PX_EN AT24 PX_EN_T
R19 0R PX_EN OUT 31,32
R21 1K DNI
C53 0.1uF 6.3V
PCIE_ZVSS AJ16 PCIE_ZVSS
2mA max current
R38 200R 1%

Remove LMSMCLK offpage
Remove LMSMDATA offpage

Remove R149 for I/O3_RESET#

remove PD_PERSTB

換msi footprint

S-BAT54KFILM_SOD523-RH

delete WAKEB

delete reserve circuit

delete WAKEB_CON

Should minimize the wire resistance and parasitic capacitance from external board device to internal bump.

- total trace resistance < 1 ohm
- total parasitic capacitance < 10pF

SYMBOL LEGEND

DNI	DO NOT INSTALL
b or #	ACTIVE LOW
BUO	BRING UP ONLY
⏚	DIGITAL GROUND
▽	ANALOG GROUND

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Size Custom | Document Description 0003 NAVI23 - PCIe Interface | Rev 2.0

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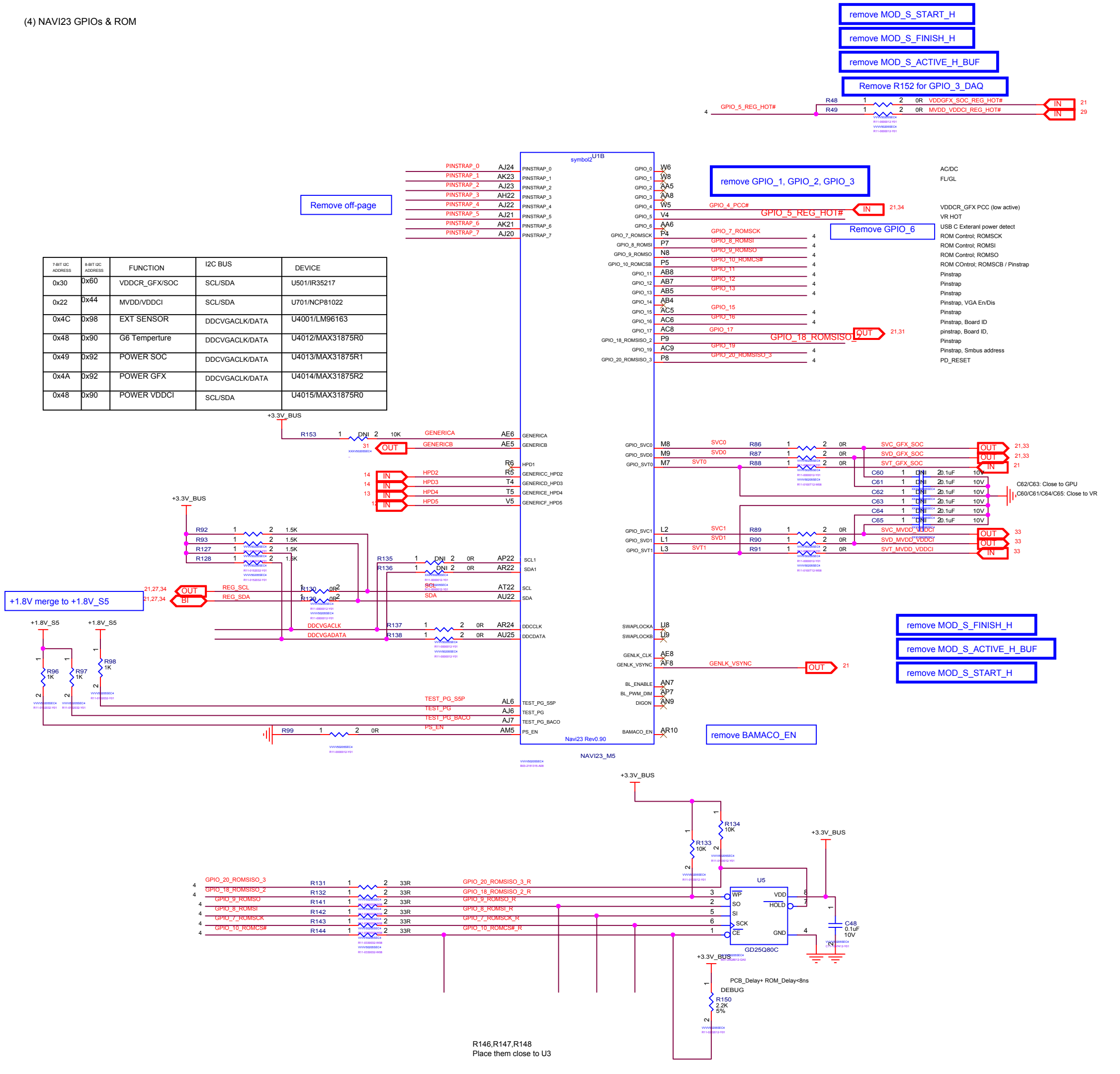
(4) NAVI23 GPIOs & ROM


remove MOD_S_START_H
remove MOD_S_FINISH_H
remove MOD_S_ACTIVE_H_BUF
Remove R152 for GPIO_3_DAQ
GPIO_5_REG_HOT#
R48 1 2 0R VDDGFX_SOC_REG_HOT# IN 21
R49 1 2 0R MVDD_VDDCI_REG_HOT# IN 29
U1B
symbol2
PINSTRAP_0 AJ24
PINSTRAP_1 AK23
PINSTRAP_2 AJ23
PINSTRAP_3 AH22
PINSTRAP_4 AJ22
PINSTRAP_5 AJ21
PINSTRAP_6 AK21
PINSTRAP_7 AJ20
Remove off-page
GPIO_0 W6
GPIO_1 W8
GPIO_2 AA5
GPIO_3 AA8
GPIO_4 W5
GPIO_5 V4
GPIO_6 AA6
GPIO_7_ROMSCK P4
GPIO_8_ROMSI P7
GPIO_9_ROMSO N8
GPIO_10_ROMCSB P5
GPIO_11 AB8
GPIO_12 AB7
GPIO_13 AB5
GPIO_14 AB4
GPIO_15 AC5
GPIO_16 AC6
GPIO_17 AC8
GPIO_18_ROMSISO_2 P9
GPIO_19 AC9
GPIO_20_ROMSISO_3 P8
remove GPIO_1, GPIO_2, GPIO_3
GPIO_4_PCC#
GPIO_5_REG_HOT# IN 21,34
Remove GPIO_6
GPIO_7_ROMSCK
GPIO_8_ROMSI
GPIO_9_ROMSO
GPIO_10_ROMCS#
GPIO_18_ROMSISO_2 OUT 21,31
GPIO_20_ROMSISO_3
AC/DC
FL/GL
VDDCR_GFX PCC (low active)
VR HOT
USB C Exteranl power detect
ROM Control; ROMSCK
ROM Control; ROMSI
ROM Control; ROMSO
ROM COntrol; ROMSCB / Pinstrap
Pinstrap
Pinstrap
Pinstrap
Pinstrap, VGA En/Dis
Pinstrap
Pinstrap, Board ID
pinstrap, Board ID,
Pinstrap
Pinstrap, Smbus address
PD_RESET
+3.3V_BUS
R153 1 DNI 2 10K
GENERICA AE6
GENERICB AE5 OUT 31
HPD1 R6
HPD2 R5 IN 14
HPD3 T4 IN 14
HPD4 T5 IN 13
HPD5 V5 IN 12
GENERICC_HPD2
GENERICD_HPD3
GENERICE_HPD4
GENERICF_HPD5
GPIO_SVC0 M8 SVC0 R86 1 2 0R SVC_GFX_SOC OUT 21,33
GPIO_SVD0 M9 SVD0 R87 1 2 0R SVD_GFX_SOC OUT 21,33
GPIO_SVT0 M7 SVT0 R88 1 2 0R SVT_GFX_SOC IN 21
C60 C61 C62 C63 C64 C65 DNI 0.1uF 10V
C62/C63: Close to GPU
C60/C61/C64/C65: Close to VR
GPIO_SVC1 L2 SVC1 R89 1 2 0R SVC_MVDD_VDDCI OUT 33
GPIO_SVD1 L1 SVD1 R90 1 2 0R SVD_MVDD_VDDCI OUT 33
GPIO_SVT1 L3 SVT1 R91 1 2 0R SVT_MVDD_VDDCI IN 33
+3.3V_BUS
R92 1 2 1.5K
R93 1 2 1.5K
R127 1 2 1.5K
R128 1 2 1.5K
R135 1 DNI 2 0R AP22 SCL1
R136 1 DNI 2 0R AR22 SDA1
+1.8V merge to +1.8V_S5
21,27,34 OUT REG_SCL
21,27,34 BI REG_SDA
R130 1 0R 2
R129 1 0R 2
SCL AT22
SDA AU22
DDCVGACLK R137 1 2 0R AR24 DDCCLK
DDCVGADATA R138 1 2 0R AU25 DDCDATA
SWAPLOCKA U8
SWAPLOCKB U9
GENLK_CLK AE8
GENLK_VSYNC AF8 GENLK_VSYNC OUT 21
BL_ENABLE AN7
BL_PWM_DIM AP7
DIGON AN9
remove MOD_S_FINISH_H
remove MOD_S_ACTIVE_H_BUF
remove MOD_S_START_H
+1.8V_S5
+1.8V_S5
R96 1K
R97 1K
R98 1K
TEST_PG_S5P AL6
TEST_PG AJ6
TEST_PG_BACO AJ7
PS_EN AM5
R99 1 2 0R
BAMACO_EN AR10
remove BAMACO_EN
Navi23 Rev0.90
NAVI23_M5
+3.3V_BUS
R134 10K
R133 10K
+3.3V_BUS
GPIO_20_ROMSISO_3 R131 1 2 33R GPIO_20_ROMSISO_3_R
GPIO_18_ROMSISO_2 R132 1 2 33R GPIO_18_ROMSISO_2_R
GPIO_9_ROMSO R141 1 2 33R GPIO_9_ROMSO_R
GPIO_8_ROMSI R142 1 2 33R GPIO_8_ROMSI_R
GPIO_7_ROMSCK R143 1 2 33R GPIO_7_ROMSCK_R
GPIO_10_ROMCS# R144 1 2 33R GPIO_10_ROMCS#_R
U5
WP SO SI SCK CE
VDD HOLD GND
GD25Q80C
C48 0.1uF 10V
+3.3V_BUS
PCB_Delay+ ROM_Delay<8ns
DEBUG
R150 2.2K 5%
R146,R147,R148
Place them close to U3

7-BIT I2C ADDRESS	8-BIT I2C ADDRESS	FUNCTION	I2C BUS	DEVICE
0x30	0x60	VDDCR_GFX/SOC	SCL/SDA	U501/IR35217
0x22	0x44	MVDD/VDDCI	SCL/SDA	U701/NCP81022
0x4C	0x98	EXT SENSOR	DDCVGACLK/DATA	U4001/LM96163
0x48	0x90	G6 Temperture	DDCVGACLK/DATA	U4012/MAX31875R0
0x49	0x92	POWER SOC	DDCVGACLK/DATA	U4013/MAX31875R1
0x4A	0x92	POWER GFX	DDCVGACLK/DATA	U4014/MAX31875R2
0x48	0x90	POWER VDDCI	SCL/SDA	U4015/MAX31875R0

Remove EXTERNAL SPI PROGRAMMER HEADER FOR VBIOS

EXTERNAL SPI PROGRAMMER HEADER FOR VBIOS

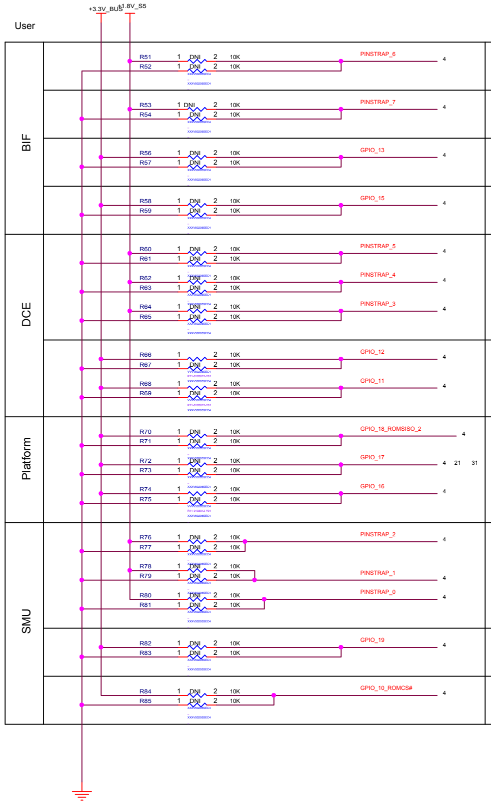
CS1
SO

VCC

CLK
SI

+1.8V merge to +1.8V_S5

Note: Internal PU/PD at GPIO pad is ~40k strength in 14nm design spec


+3.3V_BUS
+1.8V_S5
R51 1 DNI 2 10K
R52 1 DNI 2 10K
PINSTRAP_6 4
R53 1 DNI 2 10K
R54 1 DNI 2 10K
PINSTRAP_7 4
R56 1 DNI 2 10K
R57 1 DNI 2 10K
GPIO_13 4
R58 1 DNI 2 10K
R59 1 DNI 2 10K
GPIO_15 4
R60 1 DNI 2 10K
R61 1 DNI 2 10K
PINSTRAP_5 4
R62 1 DNI 2 10K
R63 1 DNI 2 10K
PINSTRAP_4 4
R64 1 DNI 2 10K
R65 1 DNI 2 10K
PINSTRAP_3 4
R66 1 2 10K
R67 1 DNI 2 10K
GPIO_12 4
R68 1 2 10K
R69 1 DNI 2 10K
GPIO_11 4
R70 1 DNI 2 10K
R71 1 DNI 2 10K
GPIO_18_ROMSISO_2 4
R72 1 DNI 2 10K
R73 1 DNI 2 10K
GPIO_17 4 21 31
R74 1 2 10K
R75 1 DNI 2 10K
GPIO_16 4
R76 1 DNI 2 10K
R77 1 DNI 2 10K
PINSTRAP_2 4
R78 1 DNI 2 10K
R79 1 DNI 2 10K
PINSTRAP_1 4
R80 1 DNI 2 10K
R81 1 DNI 2 10K
PINSTRAP_0 4
R82 1 DNI 2 10K
R83 1 DNI 2 10K
GPIO_19 4
R84 1 DNI 2 10K
R85 1 DNI 2 10K
GPIO_10_ROMCS# 4

User	Internal Default Value	Definition
BIF	0	STRAP_BIF_GEN4_DIS_A 0: PCIe GEN 4 supported 1: PCIe GEN 4 not supported
BIF	0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled
BIF	0	PINSTRAP_BIF_LC_TX_SWING 0: Full swing mode 1: Reduced swing mode(half swing)
BIF	0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognised as the system's VGA controller
DCE	0 0 0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected Deafault(PINSTRAP5,PINSTRAR4,PINSTRAR3) = 000
DCE	0 0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for both DisplayPort and HDMI Deafault(GPIO12,GPIO11) = 11
Platform	0 0 0	PINSTRAP_FIG[1:0] - No definition on NV PINSTRAP_MVDD_FB_DIVIDER_CONFIG 0: Divider does not exist 1: Divider exists
SMU	1 0 1	PINSTRAP_BFI_MEM_AP_SIZE[2:0] Or PINSTRAP_ROM_CONFIG[2:0] 100 - 512KBIT (ST) M25P05A 101 - 1MBIT (ST) (M25P10A) 101 - 2MBIT (ST) M25P20 101 - 4MBIT (ST) M25P40 101 - 8MBIT (ST) M25P80 100 - 512KBIT (CHINGIS) PM25LV512 101 - 1MBIT (CHINGIS) PM25LV010 Deafault(PINSTRAP2,PINSTRAR1,PINSTRAR0) = 101
SMU	0	PINSTRAP_SMBUS_ADDR 0: 0x41h 1: 0x40h
SMU	1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device

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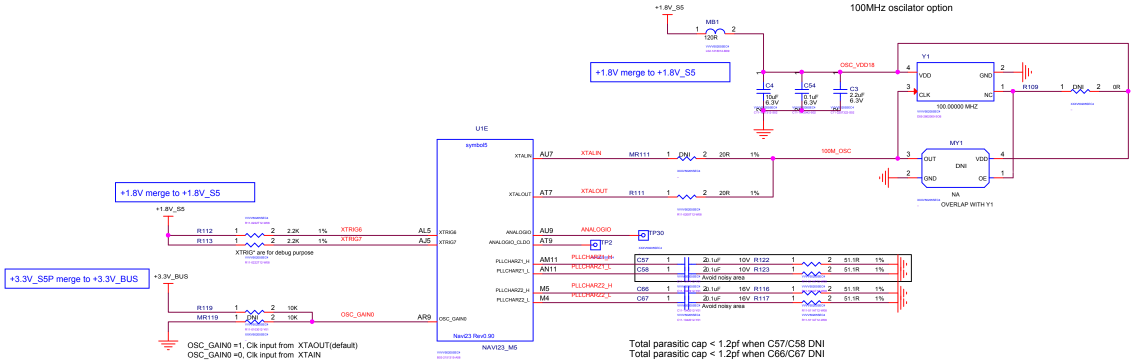
(5) NAVI23 XTAL


100MHz oscillator option
+1.8V_S5
MB1
1
2
120R
+1.8V merge to +1.8V_S5
OSC_VDD18
C4
10uF
6.3V
C54
0.1uF
6.3V
C3
2.2uF
6.3V
Y1
4
VDD
2
GND
3
CLK
1
NC
100.00000 MHZ
R109
1
DNI
2
0R
U1E
symbol5
XTALIN
AU7
XTALIN
MR111
1
DNI
2
20R
1%
100M_OSC
MY1
3
OUT
VDD
4
DNI
2
GND
OE
1
NA
OVERLAP WITH Y1
XTALOUT
AT7
XTALOUT
R111
1
2
20R
1%
+1.8V merge to +1.8V_S5
+1.8V_S5
R112
1
2
2.2K
1%
XTRIG6
AL5
XTRIG6
R113
1
2
2.2K
1%
XTRIG7
AJ5
XTRIG7
XTRIG* are for debug purpose
ANALOGIO
AU9
ANALOGIO
TP30
ANALOGIO_CLDO
AT9
TP2
PLLCHARZ1_H
AM11
PLLCHARZ1_H
C57
1
2
0.1uF
10V
R122
1
2
51.1R
1%
PLLCHARZ1_L
AN11
PLLCHARZ1_L
C58
1
2
0.1uF
10V
R123
1
2
51.1R
1%
Avoid noisy area
PLLCHARZ2_H
M5
PLLCHARZ2_H
C66
1
2
0.1uF
16V
R116
1
2
51.1R
1%
PLLCHARZ2_L
M4
PLLCHARZ2_L
C67
1
2
0.1uF
16V
R117
1
2
51.1R
1%
Avoid noisy area
+3.3V_S5P merge to +3.3V_BUS
+3.3V_BUS
R119
1
2
10K
MR119
1
DNI
2
10K
OSC_GAIN0
AR9
OSC_GAIN0
Navi23 Rev0.90
NAVI23_M5

OSC_GAIN0 =1, Clk input from XTAOUT(default)
OSC_GAIN0 =0, Clk input from XTAIN

Total parasitic cap < 1.2pf when C57/C58 DNI
Total parasitic cap < 1.2pf when C66/C67 DNI

MSI
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MS-V502
Size Custom
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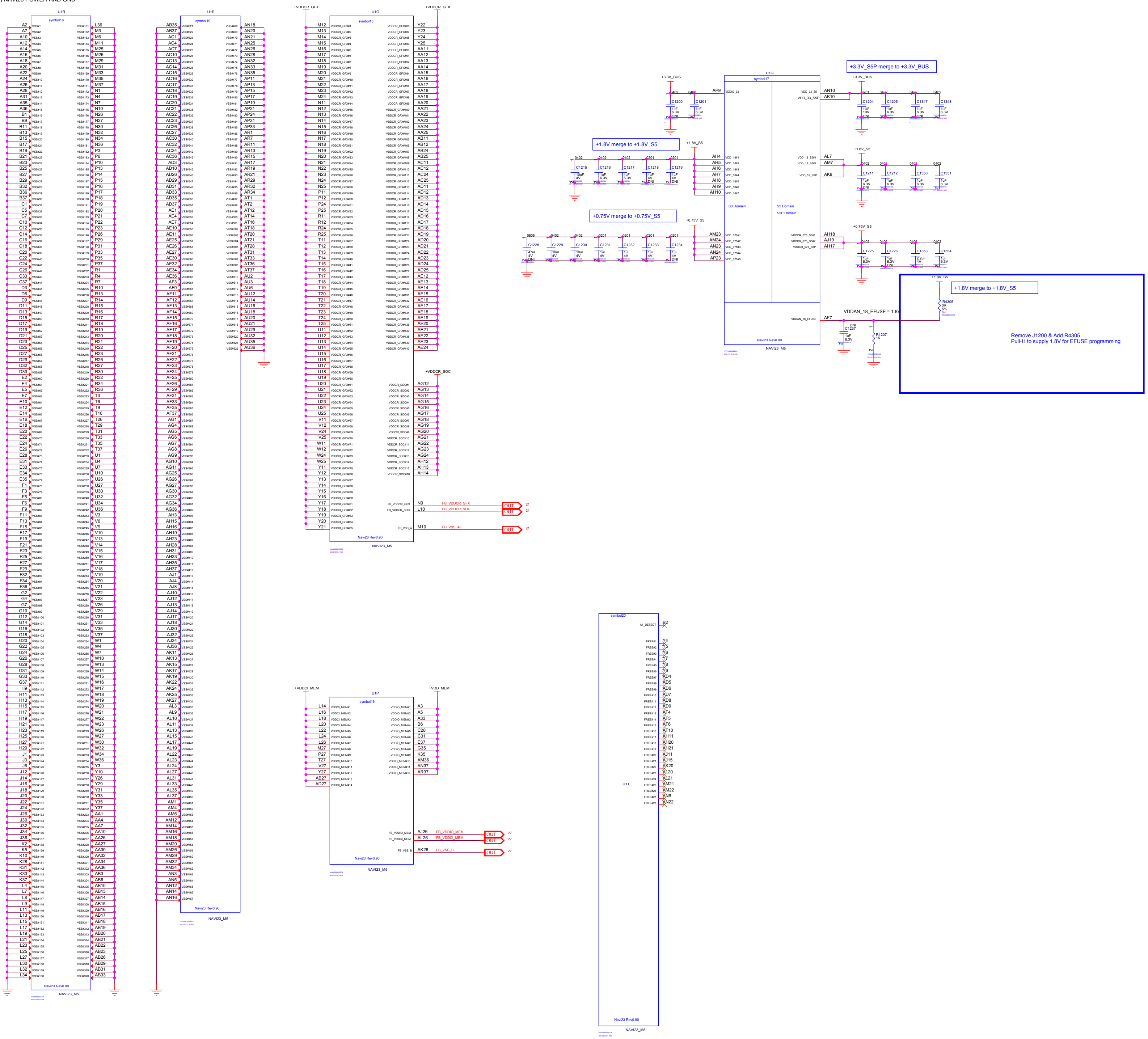
(6) NAVI23 POWER AND GND


U1R
symbol18
VSS#1 … VSS#320
Navi23 Rev0.90
NAVI23_M5
U1S
symbol19
VSS#321 … VSS#522
Navi23 Rev0.90
NAVI23_M5
+VDDCR_GFX
U1O
symbol15
VDDCR_GFX#1 … VDDCR_GFX#140
+VDDCR_SOC
VDDCR_SOC#1 … VDDCR_SOC#16
FB_VDDCR_GFX
FB_VDDCR_SOC
FB_VSS_A
N9
L10
M10
OUT
21
Navi23 Rev0.90
NAVI23_M5
+3.3V_BUS
U1Q
symbol17
VDDIO_33
AP9
C1200
C1201
1uF
6.3V
DNI
0402
VDD_33_S5
VDD_33_S5P
AN10
AK10
C1204
C1205
C1347
C1348
1UF
10V
0201
+1.8V_S5
VDD_18#1 … VDD_18#7
AH4
AH5
AH6
AH7
AH8
AH9
AH10
C1215
C1216
C1217
C1218
C1219
10uF
4V
VDD_18_S5#1
VDD_18_S5#2
VDD_18_S5P
AL7
AM7
AK9
C1211
C1212
C1350
C1351
S0 Domain
S5 Domain
S5P Domain
+0.75V_S5
VDD_075#1 … VDD_075#5
AM23
AM24
AN23
AN24
AP23
C1228
C1229
C1230
C1231
C1232
C1233
C1234
47uF
0805
VDDCR_075_S5#1
VDDCR_075_S5#2
VDDCR_075_S5P
AH18
AJ19
AH17
C1225
C1226
C1353
C1354
2.2uF
VDDAN_18_EFUSE
AF7
VDDAN_18_EFUSE = 1.8V
C1237
R1207
1K
R4305
0R
5%
Navi23 Rev0.90
NAVI23_M5
+VDDCI_MEM
+VDD_MEM
U1P
symbol16
VDDCI_MEM#1 … VDDCI_MEM#14
VDDIO_MEM#1 … VDDIO_MEM#12
FB_VDDIO_MEM
FB_VDDCI_MEM
FB_VSS_B
AJ26
AL26
AK26
27
Navi23 Rev0.90
NAVI23_M5
symbol20
A1_DETECT
B2
FREE#1 … FREE#28
U1T
Navi23 Rev0.90
NAVI23_M5

+3.3V_S5P merge to +3.3V_BUS

+1.8V merge to +1.8V_S5

+0.75V merge to +0.75V_S5

+1.8V merge to +1.8V_S5

Remove J1200 & Add R4305
Pull-H to supply 1.8V for EFUSE programming

+3.3V_AUX merge to +3.3V_BUS

+3.3V_S5P merge to +3.3V_BUS

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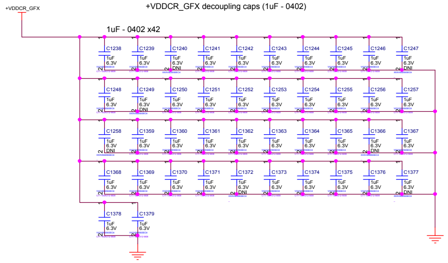
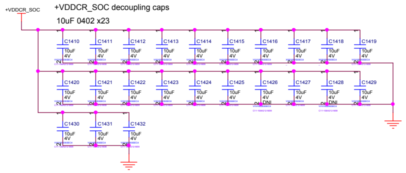
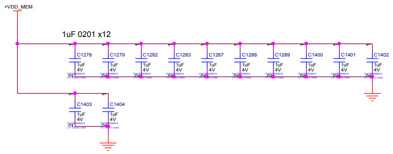
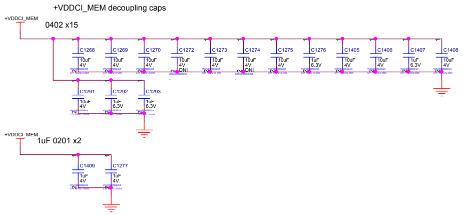
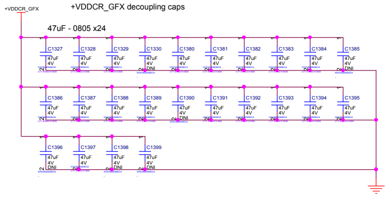
(7) NAVI23 Decaps


+VDDCR_GFX
+VDDCR_GFX decoupling caps (1uF - 0402)
1uF - 0402 x42
C1238 1uF 6.3V
C1239 1uF 6.3V
C1240 1uF 6.3V DNI
C1241 1uF 6.3V
C1242 1uF 6.3V
C1243 1uF 6.3V
C1244 1uF 6.3V
C1245 1uF 6.3V
C1246 1uF 6.3V
C1247 1uF 6.3V DNI
C1248 1uF 6.3V
C1249 1uF 6.3V DNI
C1250 1uF 6.3V
C1251 1uF 6.3V
C1252 1uF 6.3V
C1253 1uF 6.3V
C1254 1uF 6.3V
C1255 1uF 6.3V
C1256 1uF 6.3V
C1257 1uF 6.3V
C1258 1uF 6.3V DNI
C1359 1uF 6.3V
C1360 1uF 6.3V
C1361 1uF 6.3V
C1362 1uF 6.3V
C1363 1uF 6.3V
C1364 1uF 6.3V
C1365 1uF 6.3V
C1366 1uF 6.3V DNI
C1367 1uF 6.3V
C1368 1uF 6.3V
C1369 1uF 6.3V
C1370 1uF 6.3V
C1371 1uF 6.3V
C1372 1uF 6.3V DNI
C1373 1uF 6.3V
C1374 1uF 6.3V
C1375 1uF 6.3V
C1376 1uF 6.3V
C1377 1uF 6.3V DNI
C1378 1uF 6.3V
C1379 1uF 6.3V


+VDDCR_SOC
+VDDCR_SOC decoupling caps
10uF 0402 x23
C1410 10uF 4V
C1411 10uF 4V
C1412 10uF 4V
C1413 10uF 4V
C1414 10uF 4V
C1415 10uF 4V
C1416 10uF 4V
C1417 10uF 4V
C1418 10uF 4V
C1419 10uF 4V
C1420 10uF 4V
C1421 10uF 4V
C1422 10uF 4V
C1423 10uF 4V
C1424 10uF 4V
C1425 10uF 4V
C1426 10uF 4V DNI
C1427 10uF 4V
C1428 10uF 4V DNI
C1429 10uF 4V
C1430 10uF 4V
C1431 10uF 4V
C1432 10uF 4V


+VDD_MEM
1uF 0201 x12
C1278 1uF 4V
C1279 1uF 4V
C1282 1uF 4V
C1283 1uF 4V
C1287 1uF 4V
C1288 1uF 4V
C1289 1uF 4V
C1400 1uF 4V
C1401 1uF 4V
C1402 1uF 4V
C1403 1uF 4V
C1404 1uF 4V


+VDDCI_MEM decoupling caps
+VDDCI_MEM
0402 x15
C1268 10uF 4V
C1269 10uF 4V
C1270 10uF 4V
C1272 10uF 4V DNI
C1273 10uF 4V
C1274 10uF 4V DNI
C1275 10uF 4V
C1276 1uF 6.3V
C1405 10uF 4V
C1406 10uF 4V
C1407 1uF 6.3V
C1408 10uF 4V
C1291 10uF 4V
C1292 1uF 6.3V
C1293 1uF 6.3V
+VDDCI_MEM
1uF 0201 x2
C1409 1uF 4V
C1277 1uF 4V


+VDDCR_GFX
+VDDCR_GFX decoupling caps
47uF - 0805 x24
C1327 47uF 4V
C1328 47uF 4V
C1329 47uF 4V
C1330 47uF 4V DNI
C1380 47uF 4V
C1381 47uF 4V
C1382 47uF 4V
C1383 47uF 4V
C1384 47uF 4V
C1385 47uF 4V DNI
C1386 47uF 4V
C1387 47uF 4V
C1388 47uF 4V
C1389 47uF 4V
C1390 47uF 4V DNI
C1391 47uF 4V
C1392 47uF 4V
C1393 47uF 4V
C1394 47uF 4V
C1395 47uF 4V
C1396 47uF 4V DNI
C1397 47uF 4V
C1398 47uF 4V DNI
C1399 47uF 4V DNI

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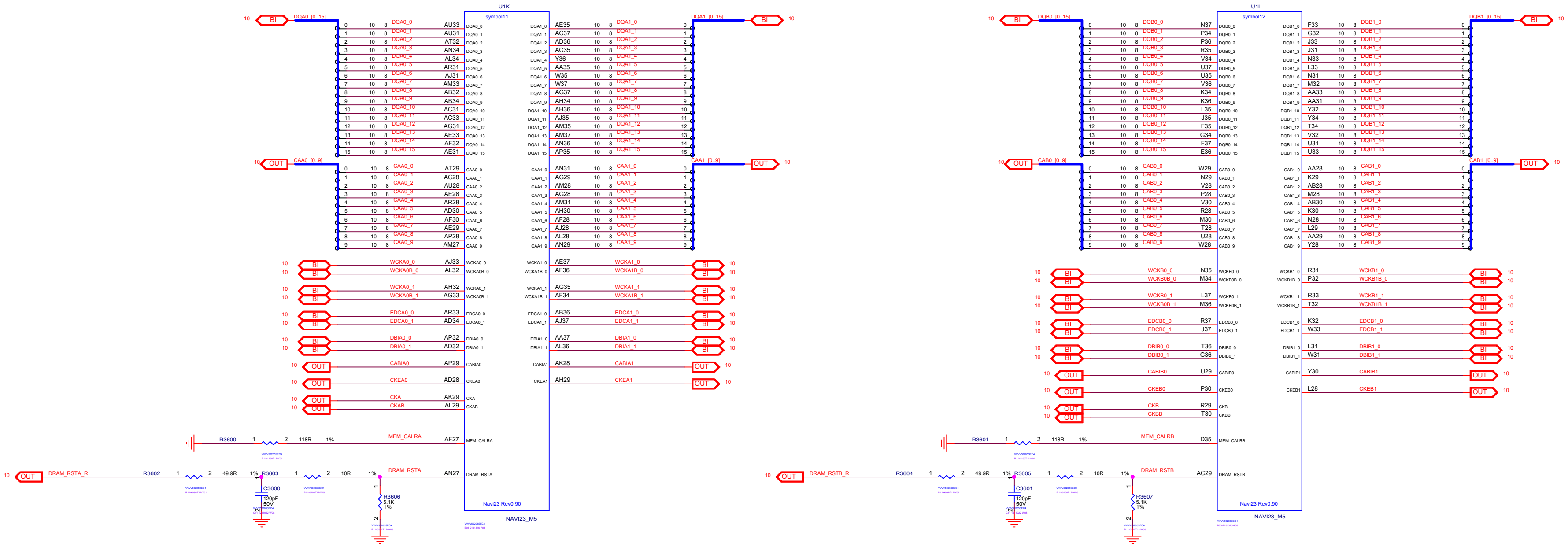
(8) NAVI23 MEM INTERFACE CH A/B


U1K
symbol11
DQA0_[0..15] BI 10
DQA0_0 AU33 · DQA0_1 AU31 · DQA0_2 AT32 · DQA0_3 AN34 · DQA0_4 AL34 · DQA0_5 AR31 · DQA0_6 AJ31 · DQA0_7 AM33 · DQA0_8 AB32 · DQA0_9 AB34 · DQA0_10 AC31 · DQA0_11 AC33 · DQA0_12 AG31 · DQA0_13 AE33 · DQA0_14 AF32 · DQA0_15 AE31
CAA0_[0..9] OUT 10
CAA0_0 AT29 · CAA0_1 AC28 · CAA0_2 AU28 · CAA0_3 AE28 · CAA0_4 AR28 · CAA0_5 AD30 · CAA0_6 AF30 · CAA0_7 AE29 · CAA0_8 AP28 · CAA0_9 AM27
WCKA0_0 AJ33 · WCKA0B_0 AL32 · WCKA0_1 AH32 · WCKA0B_1 AG33
EDCA0_0 AR33 · EDCA0_1 AD34 · DBIA0_0 AP32 · DBIA0_1 AD32
CABIA0 AP29 · CKEA0 AD28 · CKA AK29 · CKAB AL29
MEM_CALRA AF27 · R3600 1 2 118R 1%
DRAM_RSTA AN27 · DRAM_RSTA_R OUT 10 · R3602 1 2 49.9R 1% · R3603 1 2 10R 1% · C3600 120pF 50V · R3606 5.1K 1%
DQA1_0 AE35 · DQA1_1 AC37 · DQA1_2 AD36 · DQA1_3 AC35 · DQA1_4 Y36 · DQA1_5 AA35 · DQA1_6 W35 · DQA1_7 W37 · DQA1_8 AG37 · DQA1_9 AH34 · DQA1_10 AH36 · DQA1_11 AJ35 · DQA1_12 AM35 · DQA1_13 AM37 · DQA1_14 AN36 · DQA1_15 AP35
DQA1_[0..15] BI 10
CAA1_0 AN31 · CAA1_1 AG29 · CAA1_2 AM28 · CAA1_3 AG28 · CAA1_4 AM31 · CAA1_5 AH30 · CAA1_6 AF28 · CAA1_7 AJ28 · CAA1_8 AL28 · CAA1_9 AN29
CAA1_[0..9] OUT 10
WCKA1_0 AE37 · WCKA1B_0 AF36 · WCKA1_1 AG35 · WCKA1B_1 AF34
EDCA1_0 AB36 · EDCA1_1 AJ37 · DBIA1_0 AA37 · DBIA1_1 AL36
CABIA1 AK28 · CKEA1 AH29
Navi23 Rev0.90
NAVI23_M5
U1L
symbol12
DQB0_[0..15] BI 10
DQB0_0 N37 · DQB0_1 P34 · DQB0_2 P36 · DQB0_3 R35 · DQB0_4 V34 · DQB0_5 U37 · DQB0_6 U35 · DQB0_7 V36 · DQB0_8 K34 · DQB0_9 K36 · DQB0_10 L35 · DQB0_11 J35 · DQB0_12 F35 · DQB0_13 G34 · DQB0_14 F37 · DQB0_15 E36
CAB0_[0..9] OUT 10
CAB0_0 W29 · CAB0_1 N29 · CAB0_2 V28 · CAB0_3 P28 · CAB0_4 V30 · CAB0_5 R28 · CAB0_6 M30 · CAB0_7 T28 · CAB0_8 U28 · CAB0_9 W28
WCKB0_0 N35 · WCKB0B_0 M34 · WCKB0_1 L37 · WCKB0B_1 M36
EDCB0_0 R37 · EDCB0_1 J37 · DBIB0_0 T36 · DBIB0_1 G36
CABIB0 U29 · CKEB0 P30 · CKB R29 · CKBB T30
MEM_CALRB D35 · R3601 1 2 118R 1%
DRAM_RSTB AC29 · DRAM_RSTB_R OUT 10 · R3604 1 2 49.9R 1% · R3605 1 2 10R 1% · C3601 120pF 50V · R3607 5.1K 1%
DQB1_0 F33 · DQB1_1 G32 · DQB1_2 J33 · DQB1_3 J31 · DQB1_4 N33 · DQB1_5 L33 · DQB1_6 N31 · DQB1_7 M32 · DQB1_8 AA33 · DQB1_9 AA31 · DQB1_10 Y32 · DQB1_11 Y34 · DQB1_12 T34 · DQB1_13 V32 · DQB1_14 U31 · DQB1_15 U33
DQB1_[0..15] BI 10
CAB1_0 AA28 · CAB1_1 K29 · CAB1_2 AB28 · CAB1_3 M28 · CAB1_4 AB30 · CAB1_5 K30 · CAB1_6 N28 · CAB1_7 L29 · CAB1_8 AA29 · CAB1_9 Y28
CAB1_[0..9] OUT 10
WCKB1_0 R31 · WCKB1B_0 P32 · WCKB1_1 R33 · WCKB1B_1 T32
EDCB1_0 K32 · EDCB1_1 W33 · DBIB1_0 L31 · DBIB1_1 W31
CABIB1 Y30 · CKEB1 L28
Navi23 Rev0.90
NAVI23_M5

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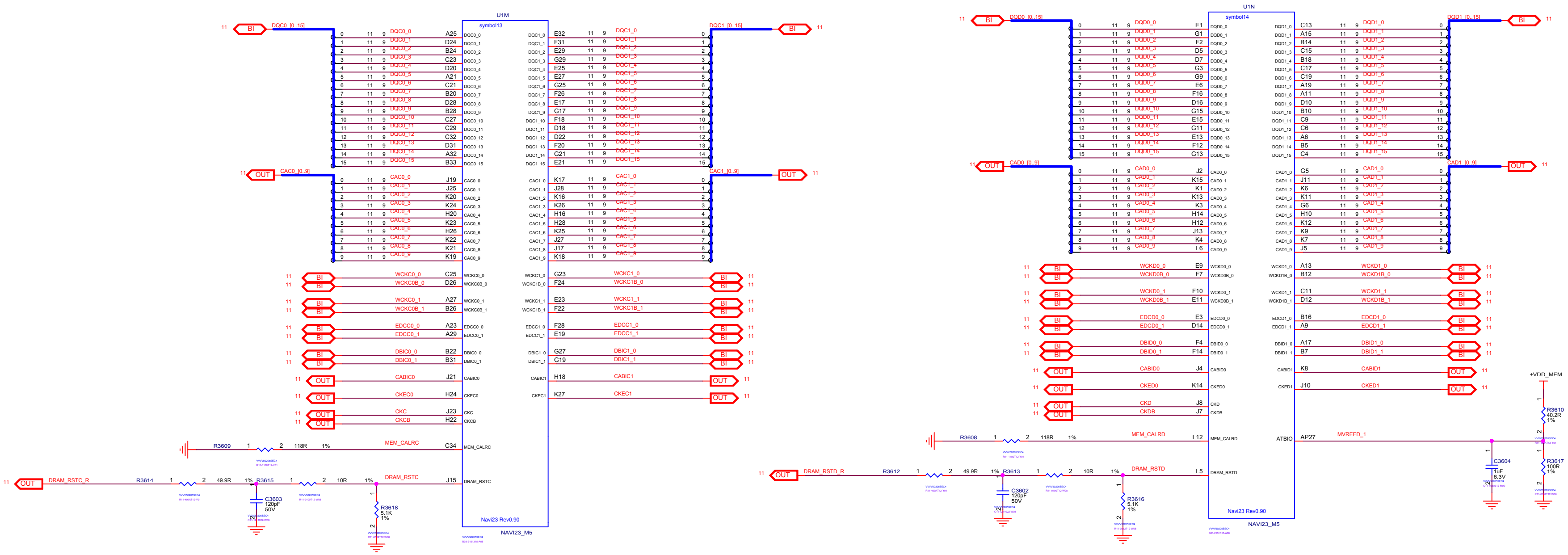
(9) NAVI23 MEM INTERFACE CH C/D


U1M
symbol13
Navi23 Rev0.90
NAVI23_M5
U1N
symbol14
Navi23 Rev0.90
NAVI23_M5
DQC0_[0..15]
DQC1_[0..15]
CAC0_[0..9]
CAC1_[0..9]
DQD0_[0..15]
DQD1_[0..15]
CAD0_[0..9]
CAD1_[0..9]
MEM_CALRC
MEM_CALRD
DRAM_RSTC
DRAM_RSTC_R
DRAM_RSTD
DRAM_RSTD_R
R3609 118R 1%
R3614 49.9R 1%
R3615 10R 1%
R3618 5.1K 1%
C3603 120pF 50V
R3608 118R 1%
R3612 49.9R 1%
R3613 10R 1%
R3616 5.1K 1%
C3602 120pF 50V
+VDD_MEM
R3610 40.2R 1%
R3617 100R 1%
C3604 1uF 6.3V
MVREFD_1
ATBIO
AP27

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Document Description: 0009 NAVI23 - MEM CH CD

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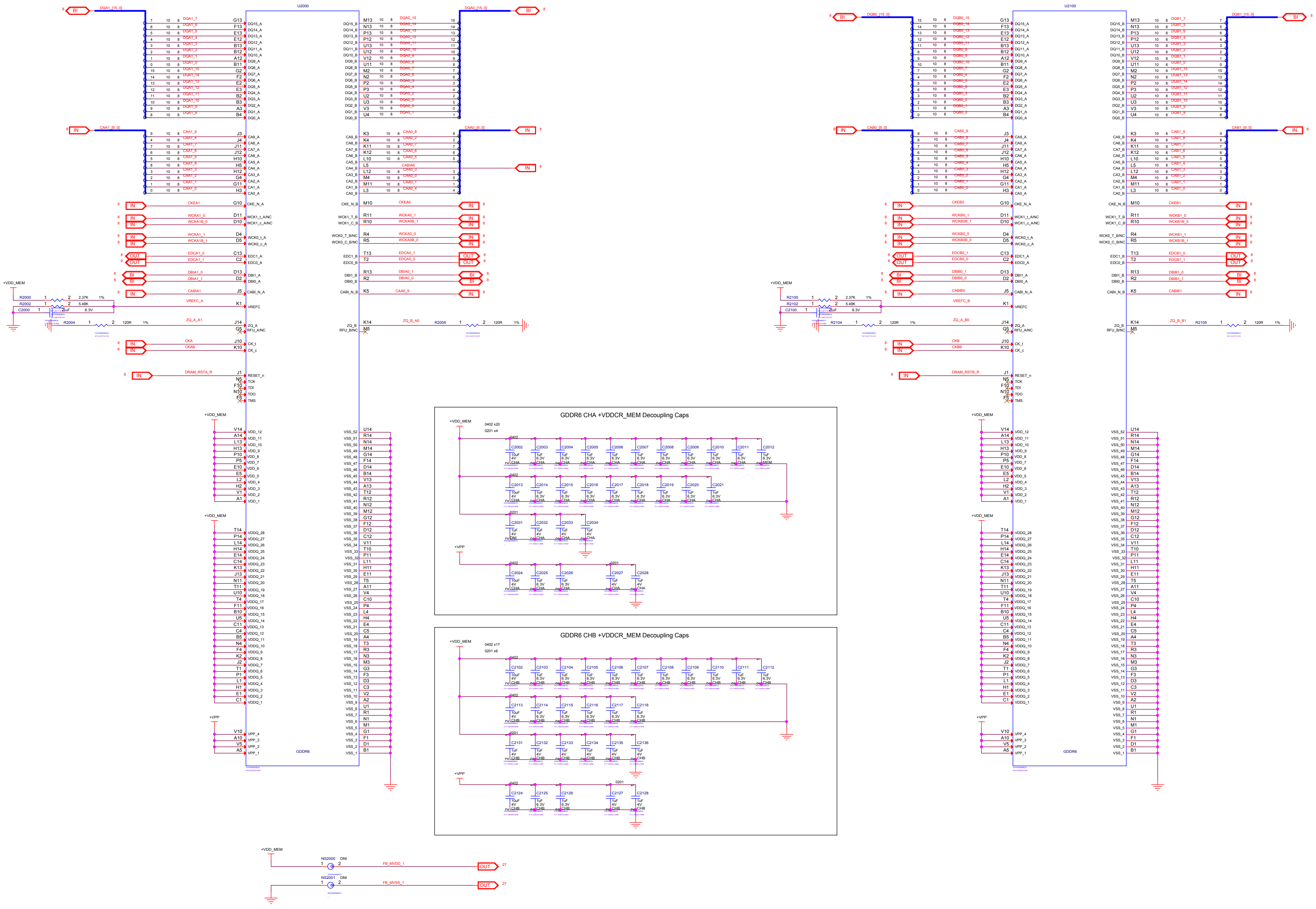
(10) GDDR6x16 CHAB Memory


U2000
U2100
GDDR6
DQA1_[15..0]
DQA0_[15..0]
DQB0_[15..0]
DQB1_[15..0]
CAA1_[9..0]
CAA0_[9..0]
CAB0_[9..0]
CAB1_[9..0]
CABIA0
CKEA1
CKEA0
CKEB0
CKEB1
WCKA1_0
WCKA1B_0
WCKA1_1
WCKA1B_1
WCKA0_1
WCKA0B_1
WCKA0_0
WCKA0B_0
WCKB0_1
WCKB0B_1
WCKB0_0
WCKB0B_0
WCKB1_0
WCKB1B_0
WCKB1_1
WCKB1B_1
EDCA1_0
EDCA1_1
EDCA0_1
EDCA0_0
EDCB0_1
EDCB0_0
EDCB1_0
EDCB1_1
DBIA1_0
DBIA1_1
DBIA0_1
DBIA0_0
DBIB0_1
DBIB0_0
DBIB1_0
DBIB1_1
CABIA1
CAA0_9
CABIB0
CABIB1
VREFC_A
VREFC_B
ZQ_A_A1
ZQ_B_A0
ZQ_A_B0
ZQ_B_B1
CKA
CKAB
CKB
CKBB
DRAM_RSTA_R
DRAM_RSTB_R
+VDD_MEM
+VPP
R2000 2.37K 1%
R2002 5.49K
C2000 1uF 6.3V
R2004 120R 1%
R2005 120R 1%
R2100 2.37K 1%
R2102 5.49K
C2100 1uF 6.3V
R2104 120R 1%
R2105 120R 1%
BI
IN
OUT
GDDR6 CHA +VDDCR_MEM Decoupling Caps
0402 x20
0201 x4
C2002 C2003 C2004 C2005 C2006 C2007 C2008 C2009 C2010 C2011 C2012
C2013 C2014 C2015 C2016 C2017 C2018 C2019 C2020 C2021
C2031 C2032 C2033 C2034
C2024 C2025 C2026 C2027 C2028
10uF 4V CHA
1uF 6.3V CHA
1uF 6.3V MEM
1uF 4V DNI
1uF 4V CHA
GDDR6 CHB +VDDCR_MEM Decoupling Caps
0402 x17
0201 x6
C2102 C2103 C2104 C2105 C2106 C2107 C2108 C2109 C2110 C2111 C2112
C2113 C2114 C2115 C2116 C2117 C2118
C2131 C2132 C2133 C2134 C2135 C2136
C2124 C2125 C2126 C2127 C2128
10uF 4V CHB
1uF 6.3V CHB
1uF 4V CHB
NS2000 DNI
NS2001 DNI
FB_MVDD_1
FB_MVSS_1
OUT 27

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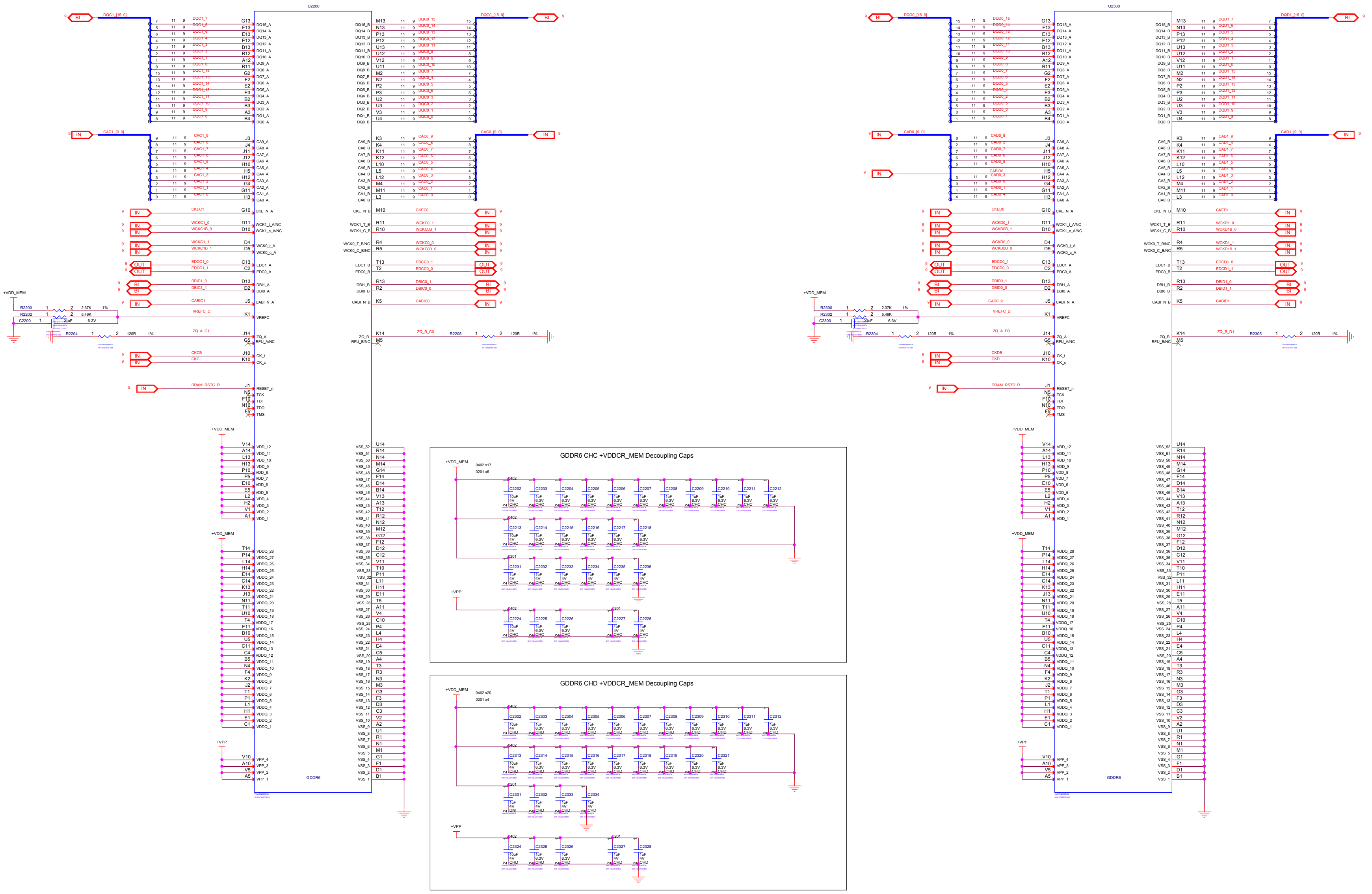
(11) GDDR6x16 CHCD Memory


U2200
U2300
GDDR6
+VDD_MEM
+VPP
GDDR6 CHC +VDDCR_MEM Decoupling Caps
GDDR6 CHD +VDDCR_MEM Decoupling Caps
0402 x17
0201 x6
0402 x20
0201 x4
BI
IN
OUT

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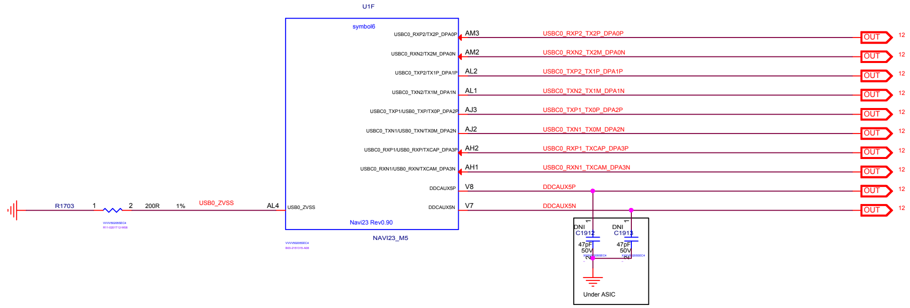
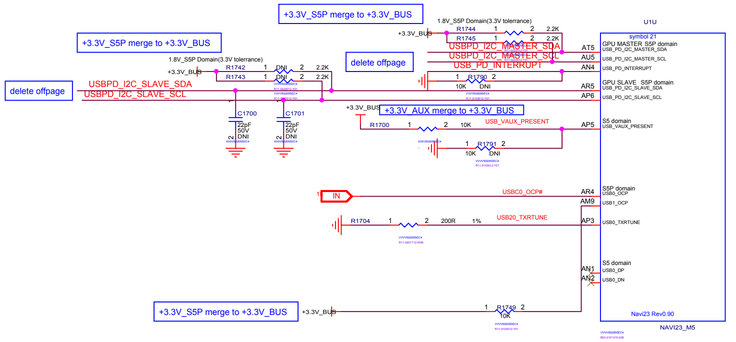
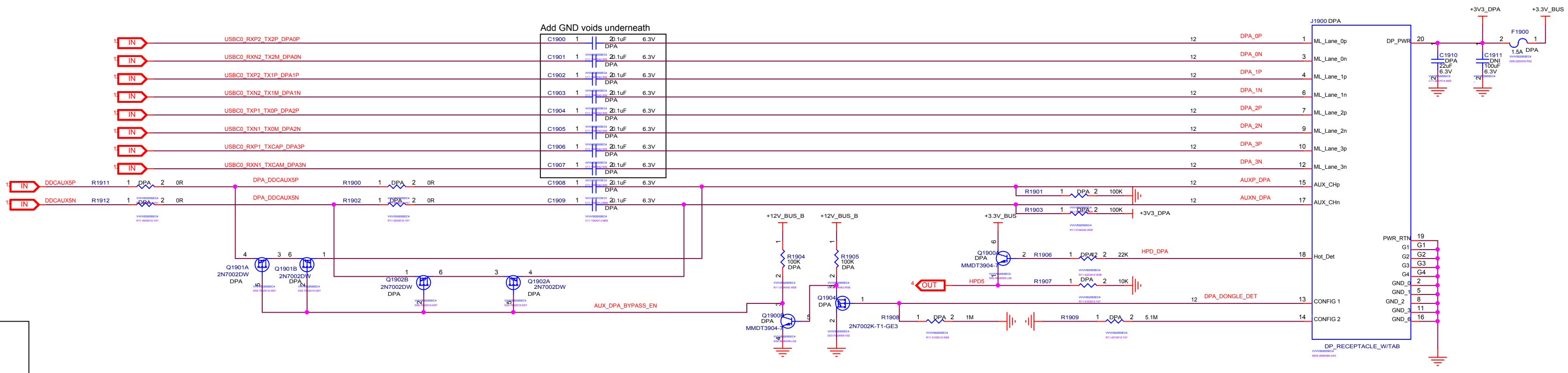
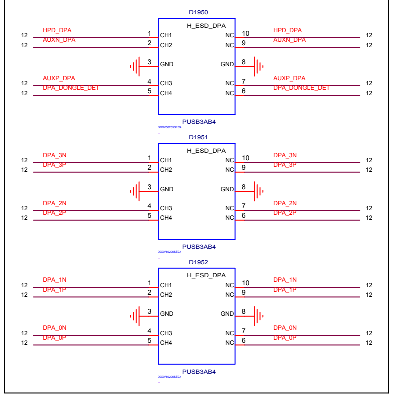
(12) TMDP AB


U1F
symbol6
USBC0_RXP2/TX2P_DPA0P AM3 USBC0_RXP2_TX2P_DPA0P OUT 12
USBC0_RXN2/TX2M_DPA0N AM2 USBC0_RXN2_TX2M_DPA0N OUT 12
USBC0_TXP2/TX1P_DPA1P AL2 USBC0_TXP2_TX1P_DPA1P OUT 12
USBC0_TXN2/TX1M_DPA1N AL1 USBC0_TXN2_TX1M_DPA1N OUT 12
USBC0_TXP1/USB0_TXP/TX0P_DPA2P AJ3 USBC0_TXP1_TX0P_DPA2P OUT 12
USBC0_TXN1/USB0_TXN/TX0M_DPA2N AJ2 USBC0_TXN1_TX0M_DPA2N OUT 12
USBC0_RXP1/USB0_RXP/TXCAP_DPA3P AH2 USBC0_RXP1_TXCAP_DPA3P OUT 12
USBC0_RXN1/USB0_RXN/TXCAM_DPA3N AH1 USBC0_RXN1_TXCAM_DPA3N OUT 12
DDCAUX5P V8 DDCAUX5P OUT 12
DDCAUX5N V7 DDCAUX5N OUT 12
R1703 1 2 200R 1% USB0_ZVSS AL4 USB0_ZVSS
Navi23 Rev0.90
NAVI23_M5
DNI C1912 47pF 50V
DNI C1913 47pF 50V
Under ASIC


+3.3V_S5P merge to +3.3V_BUS
1.8V_S5P Domain(3.3V tolerance)
+3.3V_BUS
R1744 1 2 2.2K
R1745 1 2 2.2K
U1U
symbol 21
+3.3V_S5P merge to +3.3V_BUS
1.8V_S5P Domain(3.3V tolerance)
+3.3V_BUS
R1742 1 DNI 2 2.2K
R1743 1 DNI 2 2.2K
delete offpage
USBPD_I2C_MASTER_SDA
USBPD_I2C_MASTER_SCL
USB_PD_INTERRUPT
delete offpage
USBPD_I2C_SLAVE_SDA
USBPD_I2C_SLAVE_SCL
R1790 1 2 10K DNI
AT5 GPU MASTER S5P domain USB_PD_I2C_MASTER_SDA
AU5 USB_PD_I2C_MASTER_SCL
AN4 USB_PD_INTERRUPT
AR5 GPU SLAVE S5P domain USB_PD_I2C_SLAVE_SDA
AP6 USB_PD_I2C_SLAVE_SCL
C1700 22pF 50V DNI
C1701 22pF 50V DNI
+3.3V_BUS
+3.3V_AUX merge to +3.3V_BUS
R1700 1 2 10K USB_VAUX_PRESENT
AP5 S5 domain USB_VAUX_PRESENT
R1791 1 2 10K DNI
IN USBC0_OCP#
AR4 S5P domain USB0_OCP
AM9 USB1_OCP
R1704 1 2 200R 1% USB20_TXRTUNE
AP3 USB0_TXRTUNE
S5 domain
AN1 USB0_DP
AN2 USB0_DN
+3.3V_S5P merge to +3.3V_BUS
+3.3V_BUS
R1749 1 2 10K
Navi23 Rev0.90
NAVI23_M5


Add GND voids underneath
IN USBC0_RXP2_TX2P_DPA0P C1900 1 2 0.1uF 6.3V DPA
IN USBC0_RXN2_TX2M_DPA0N C1901 1 2 0.1uF 6.3V DPA
IN USBC0_TXP2_TX1P_DPA1P C1902 1 2 0.1uF 6.3V DPA
IN USBC0_TXN2_TX1M_DPA1N C1903 1 2 0.1uF 6.3V DPA
IN USBC0_TXP1_TX0P_DPA2P C1904 1 2 0.1uF 6.3V DPA
IN USBC0_TXN1_TX0M_DPA2N C1905 1 2 0.1uF 6.3V DPA
IN USBC0_RXP1_TXCAP_DPA3P C1906 1 2 0.1uF 6.3V DPA
IN USBC0_RXN1_TXCAM_DPA3N C1907 1 2 0.1uF 6.3V DPA
IN DDCAUX5P R1911 1 DPA 2 0R DPA_DDCAUX5P R1900 1 DPA 2 0R C1908 1 2 0.1uF 6.3V DPA
IN DDCAUX5N R1912 1 DPA 2 0R DPA_DDCAUX5N R1902 1 DPA 2 0R C1909 1 2 0.1uF 6.3V DPA
Q1901A 2N7002DW DPA
Q1901B 2N7002DW DPA
Q1902B 2N7002DW DPA
Q1902A 2N7002DW DPA
AUX_DPA_BYPASS_EN
J1900 DPA
12 DPA_0P 1 ML_Lane_0p
12 DPA_0N 3 ML_Lane_0n
12 DPA_1P 4 ML_Lane_1p
12 DPA_1N 6 ML_Lane_1n
12 DPA_2P 7 ML_Lane_2p
12 DPA_2N 9 ML_Lane_2n
12 DPA_3P 10 ML_Lane_3p
12 DPA_3N 12 ML_Lane_3n
12 AUXP_DPA 15 AUX_CHp
12 AUXN_DPA 17 AUX_CHn
R1901 1 DPA 2 100K
R1903 1 DPA 2 100K +3V3_DPA
+12V_BUS_B R1904 100K DPA
+12V_BUS_B R1905 100K DPA
+3.3V_BUS
Q1900A DPA MMDT3904-7
R1906 1 DPA 2 22K HPD_DPA 18 Hot_Det
OUT HPD5 R1907 1 DPA 2 10K
Q1904 DPA 2N7002K-T1-GE3
12 DPA_DONGLE_DET 13 CONFIG 1
Q1900B DPA MMDT3904-7
R1908 1 DPA 2 1M
R1909 1 DPA 2 5.1M 14 CONFIG 2
DP_PWR 20
+3V3_DPA +3.3V_BUS
F1900 1.5A DPA
C1910 DPA 22uF 6.3V
C1911 DNI 100uF 6.3V
PWR_RTN 19
G1 G2 G3 G4
GND_0 2 GND_1 5 GND_2 8 GND_3 11 GND_6 16
DP_RECEPTACLE_W/TAB

OPTIONAL ESD PROTECTION DIODES


D1950 H_ESD_DPA
12 HPD_DPA 1 CH1 NC 10 HPD_DPA 12
12 AUXN_DPA 2 CH2 NC 9 AUXN_DPA 12
3 GND GND 8
12 AUXP_DPA 4 CH3 NC 7 AUXP_DPA 12
12 DPA_DONGLE_DET 5 CH4 NC 6 DPA_DONGLE_DET 12
PUSB3AB4
D1951 H_ESD_DPA
12 DPA_3N 1 CH1 NC 10 DPA_3N 12
12 DPA_3P 2 CH2 NC 9 DPA_3P 12
3 GND GND 8
12 DPA_2N 4 CH3 NC 7 DPA_2N 12
12 DPA_2P 5 CH4 NC 6 DPA_2P 12
PUSB3AB4
D1952 H_ESD_DPA
12 DPA_1N 1 CH1 NC 10 DPA_1N 12
12 DPA_1P 2 CH2 NC 9 DPA_1P 12
3 GND GND 8
12 DPA_0N 4 CH3 NC 7 DPA_0N 12
12 DPA_0P 5 CH4 NC 6 DPA_0P 12
PUSB3AB4

MICRO-STAR INT'L CO.,LTD

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Size: Custom
Document Description: 0012 NAVI23 - TMDPA - USB/DP
Rev: 2.0
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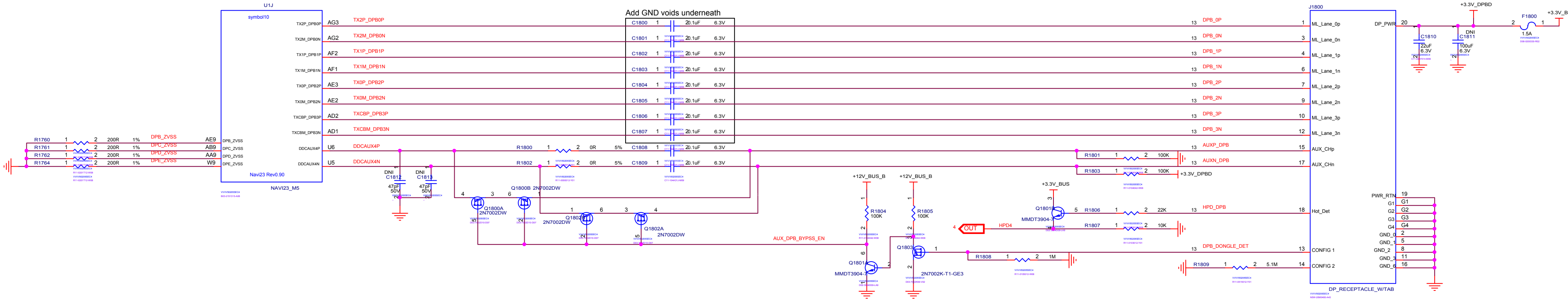
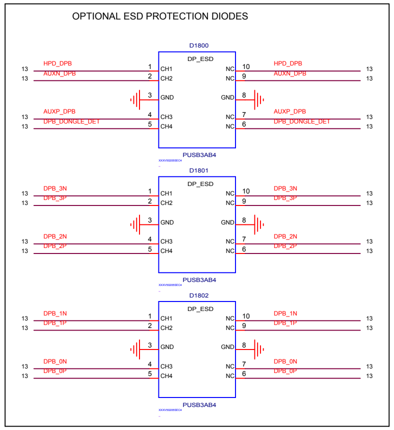
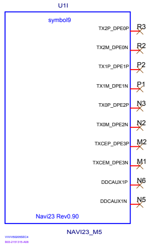
Sheet 12 of 37


U1J
symbol10
TX2P_DPB0P AG3
TX2M_DPB0N AG2
TX1P_DPB1P AF2
TX1M_DPB1N AF1
TX0P_DPB2P AE3
TX0M_DPB2N AE2
TXCBP_DPB3P AD2
TXCBM_DPB3N AD1
DPB_ZVSS AE9
DPC_ZVSS AB9
DPD_ZVSS AA9
DPE_ZVSS W9
DDCAUX4P U6
DDCAUX4N U5
Navi23 Rev0.90
NAVI23_M5
R1760 1 2 200R 1%
R1761 1 2 200R 1%
R1762 1 2 200R 1%
R1764 1 2 200R 1%
DPB_ZVSS
DPC_ZVSS
DPD_ZVSS
DPE_ZVSS
Add GND voids underneath
C1800 1 2 0.1uF 6.3V
C1801 1 2 0.1uF 6.3V
C1802 1 2 0.1uF 6.3V
C1803 1 2 0.1uF 6.3V
C1804 1 2 0.1uF 6.3V
C1805 1 2 0.1uF 6.3V
C1806 1 2 0.1uF 6.3V
C1807 1 2 0.1uF 6.3V
C1808 1 2 0.1uF 6.3V
C1809 1 2 0.1uF 6.3V
R1800 1 2 0R 5%
R1802 1 2 0R 5%
DDCAUX4P
DDCAUX4N
DNI C1812 47pF 50V
DNI C1813 47pF 50V
Q1800A 2N7002DW
Q1800B 2N7002DW
Q1802B 2N7002DW
Q1802A 2N7002DW
AUX_DPB_BYPSS_EN
13 DPB_0P 1 ML_Lane_0p
13 DPB_0N 3 ML_Lane_0n
13 DPB_1P 4 ML_Lane_1p
13 DPB_1N 6 ML_Lane_1n
13 DPB_2P 7 ML_Lane_2p
13 DPB_2N 9 ML_Lane_2n
13 DPB_3P 10 ML_Lane_3p
13 DPB_3N 12 ML_Lane_3n
13 AUXP_DPB 15 AUX_CHp
13 AUXN_DPB 17 AUX_CHn
R1801 1 2 100K
R1803 1 2 100K
+3.3V_DPBD
+12V_BUS_B
+12V_BUS_B
R1804 100K
R1805 100K
Q1801B MMDT3904-7
Q1801A MMDT3904-7
Q1803 2N7002K-T1-GE3
+3.3V_BUS
R1806 1 2 22K
13 HPD_DPB 18 Hot_Det
4 OUT HPD4
R1807 1 2 10K
R1808 1 2 1M
13 DPB_DONGLE_DET 13 CONFIG 1
R1809 1 2 5.1M 14 CONFIG 2
J1800
DP_PWR 20
PWR_RTN 19
G1 G2 G3 G4
GND_0 2
GND_1 5
GND_2 8
GND_3 11
GND_4 16
DP_RECEPTACLE_W/TAB
+3.3V_DPBD
+3.3V_BUS
F1800 2 1 1.5A
C1810 22uF 6.3V
DNI C1811 100uF 6.3V


OPTIONAL ESD PROTECTION DIODES
D1800
DP_ESD
13 HPD_DPB 1 CH1 NC 10 HPD_DPB 13
13 AUXN_DPB 2 CH2 NC 9 AUXN_DPB 13
3 GND GND 8
13 AUXP_DPB 4 CH3 NC 7 AUXP_DPB 13
13 DPB_DONGLE_DET 5 CH4 NC 6 DPB_DONGLE_DET 13
PUSB3AB4
D1801
DP_ESD
13 DPB_3N 1 CH1 NC 10 DPB_3N 13
13 DPB_3P 2 CH2 NC 9 DPB_3P 13
3 GND GND 8
13 DPB_2N 4 CH3 NC 7 DPB_2N 13
13 DPB_2P 5 CH4 NC 6 DPB_2P 13
PUSB3AB4
D1802
DP_ESD
13 DPB_1N 1 CH1 NC 10 DPB_1N 13
13 DPB_1P 2 CH2 NC 9 DPB_1P 13
3 GND GND 8
13 DPB_0N 4 CH3 NC 7 DPB_0N 13
13 DPB_0P 5 CH4 NC 6 DPB_0P 13
PUSB3AB4


U1I
symbol9
TX2P_DPE0P R3
TX2M_DPE0N R2
TX1P_DPE1P P2
TX1M_DPE1N P1
TX0P_DPE2P N3
TX0M_DPE2N N2
TXCEP_DPE3P M2
TXCEM_DPE3N M1
DDCAUX1P N6
DDCAUX1N N5
Navi23 Rev0.90
NAVI23_M5

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Size	Document Description	Rev
Custom	0013 NAVI23 - TMDPB - DP	2.0

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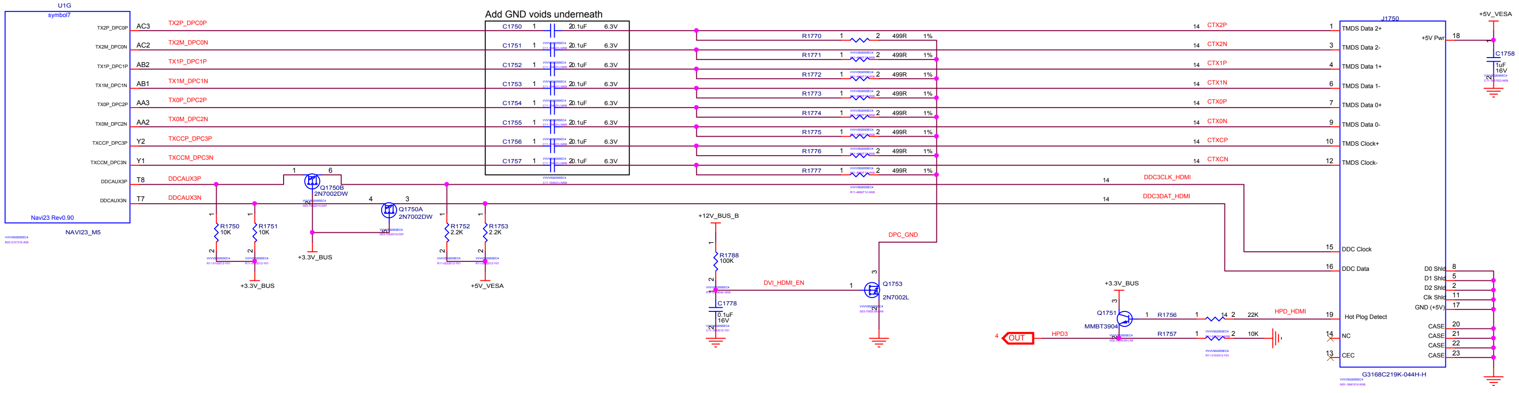
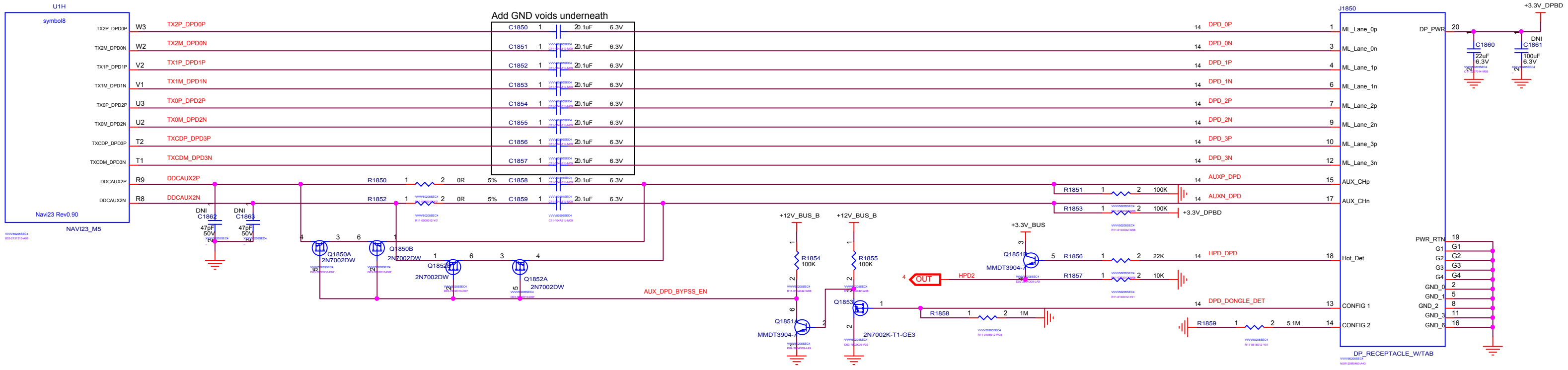
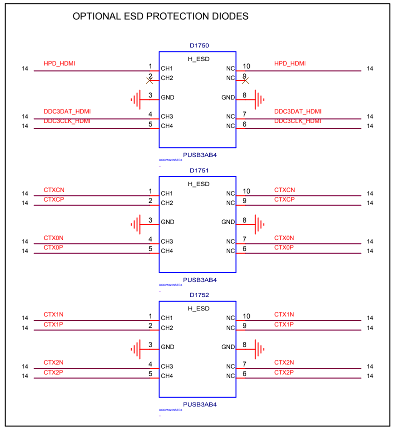


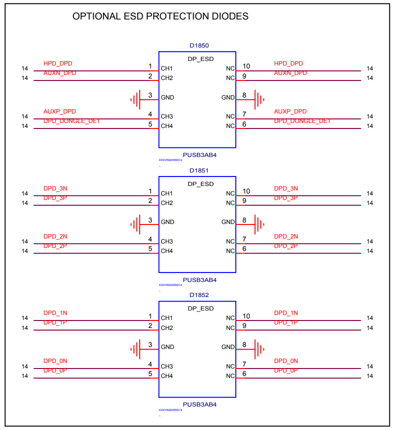
U1G
symbol7
TX2P_DPC0P AC3 TX2P_DPC0P
TX2M_DPC0N AC2 TX2M_DPC0N
TX1P_DPC1P AB2 TX1P_DPC1P
TX1M_DPC1N AB1 TX1M_DPC1N
TX0P_DPC2P AA3 TX0P_DPC2P
TX0M_DPC2N AA2 TX0M_DPC2N
TXCCP_DPC3P Y2 TXCCP_DPC3P
TXCCM_DPC3N Y1 TXCCM_DPC3N
DDCAUX3P T8 DDCAUX3P
DDCAUX3N T7 DDCAUX3N
Navi23 Rev0.90
NAVI23_M5
Add GND voids underneath
C1750 0.1uF 6.3V
C1751 0.1uF 6.3V
C1752 0.1uF 6.3V
C1753 0.1uF 6.3V
C1754 0.1uF 6.3V
C1755 0.1uF 6.3V
C1756 0.1uF 6.3V
C1757 0.1uF 6.3V
R1770 499R 1%
R1771 499R 1%
R1772 499R 1%
R1773 499R 1%
R1774 499R 1%
R1775 499R 1%
R1776 499R 1%
R1777 499R 1%
Q1750B 2N7002DW
Q1750A 2N7002DW
R1750 10K
R1751 10K
R1752 2.2K
R1753 2.2K
+3.3V_BUS
+5V_VESA
+12V_BUS_B
R1788 100K
C1778 0.1uF 16V
DVI_HDMI_EN
Q1753 2N7002L
DPC_GND
+3.3V_BUS
Q1751 MMBT3904
R1756 22K
R1757 10K
HPD_HDMI
OUT HPD3
DDC3CLK_HDMI
DDC3DAT_HDMI
CTX2P
CTX2N
CTX1P
CTX1N
CTX0P
CTX0N
CTXCP
CTXCN
J1750
TMDS Data 2+
TMDS Data 2-
TMDS Data 1+
TMDS Data 1-
TMDS Data 0+
TMDS Data 0-
TMDS Clock+
TMDS Clock-
DDC Clock
DDC Data
Hot Plug Detect
NC
CEC
+5V Pwr
D0 Shld
D1 Shld
D2 Shld
Clk Shld
GND (+5V)
CASE
CASE
CASE
CASE
C1758 1uF 16V
G3168C219K-044H-H



U1H
symbol8
TX2P_DPD0P W3 TX2P_DPD0P
TX2M_DPD0N W2 TX2M_DPD0N
TX1P_DPD1P V2 TX1P_DPD1P
TX1M_DPD1N V1 TX1M_DPD1N
TX0P_DPD2P U3 TX0P_DPD2P
TX0M_DPD2N U2 TX0M_DPD2N
TXCDP_DPD3P T2 TXCDP_DPD3P
TXCDM_DPD3N T1 TXCDM_DPD3N
DDCAUX2P R9 DDCAUX2P
DDCAUX2N R8 DDCAUX2N
Navi23 Rev0.90
NAVI23_M5
Add GND voids underneath
C1850 0.1uF 6.3V
C1851 0.1uF 6.3V
C1852 0.1uF 6.3V
C1853 0.1uF 6.3V
C1854 0.1uF 6.3V
C1855 0.1uF 6.3V
C1856 0.1uF 6.3V
C1857 0.1uF 6.3V
C1858 0.1uF 6.3V
C1859 0.1uF 6.3V
R1850 0R 5%
R1852 0R 5%
DNI C1862 47pF 50V
DNI C1863 47pF 50V
Q1850A 2N7002DW
Q1850B 2N7002DW
Q1852B 2N7002DW
Q1852A 2N7002DW
AUX_DPD_BYPSS_EN
+12V_BUS_B
R1854 100K
R1855 100K
Q1851 MMDT3904
Q1853 2N7002K-T1-GE3
+3.3V_BUS
Q1851 MMDT3904
R1856 22K
R1857 10K
OUT HPD2
R1851 100K
R1853 100K
+3.3V_DPBD
R1858 1M
R1859 5.1M
DPD_0P
DPD_0N
DPD_1P
DPD_1N
DPD_2P
DPD_2N
DPD_3P
DPD_3N
AUXP_DPD
AUXN_DPD
HPD_DPD
DPD_DONGLE_DET
J1850
ML_Lane_0p
ML_Lane_0n
ML_Lane_1p
ML_Lane_1n
ML_Lane_2p
ML_Lane_2n
ML_Lane_3p
ML_Lane_3n
AUX_CHp
AUX_CHn
Hot_Det
CONFIG 1
CONFIG 2
DP_PWR
PWR_RTN
G1
G2
G3
G4
GND_0
GND_1
GND_2
GND_5
GND_6
+3.3V_DPBD
C1860 22uF 6.3V
DNI C1861 100uF 6.3V
DP_RECEPTACLE_W/TAB



OPTIONAL ESD PROTECTION DIODES
D1750
H_ESD
HPD_HDMI
DDC3DAT_HDMI
DDC3CLK_HDMI
CH1
CH2
GND
CH3
CH4
NC
PUSB3AB4
D1751
H_ESD
CTXCN
CTXCP
CTX0N
CTX0P
PUSB3AB4
D1752
H_ESD
CTX1N
CTX1P
CTX2N
CTX2P
PUSB3AB4



OPTIONAL ESD PROTECTION DIODES
D1850
DP_ESD
HPD_DPD
AUXN_DPD
AUXP_DPD
DPD_DONGLE_DET
CH1
CH2
GND
CH3
CH4
NC
PUSB3AB4
D1851
DP_ESD
DPD_3N
DPD_3P
DPD_2N
DPD_2P
PUSB3AB4
D1852
DP_ESD
DPD_1N
DPD_1P
DPD_0N
DPD_0P
PUSB3AB4

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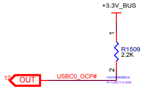
Size	Document Description	Rev
Custom	0014 NAVI23 - TMDPCD- HDMI,DP	2.0

Date: Wednesday, May 19, 2021 | Sheet 14 of 37

+3.3V_AUX merge to +3.3V_BUS


+3.3V_BUS
1
R1509
2.2K
2
12
OUT
USBC0_OCP#
R11-0201T12-W08

remove

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Size	Document Description	Rev
Custom	0015 PD CONTROLLER	2.0

Date: Wednesday, May 19, 2021 Sheet 15 of 37

remove

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Size	Document Description	Rev
Custom	0016 USB-C PORT 1& DP	2.0

Date: Wednesday, May 19, 2021 Sheet 16 of 37

remove

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	0017 3.3V_AUX	2.0

Date: Wednesday, May 19, 2021 Sheet 17 of 37

+3.3V_12V merge to +3.3V_BUS

remove

+0.75V merge to +0.75V_S5

+1.8V merge to +1.8V_S5

MICRO-STAR INT'L CO.,LTD		
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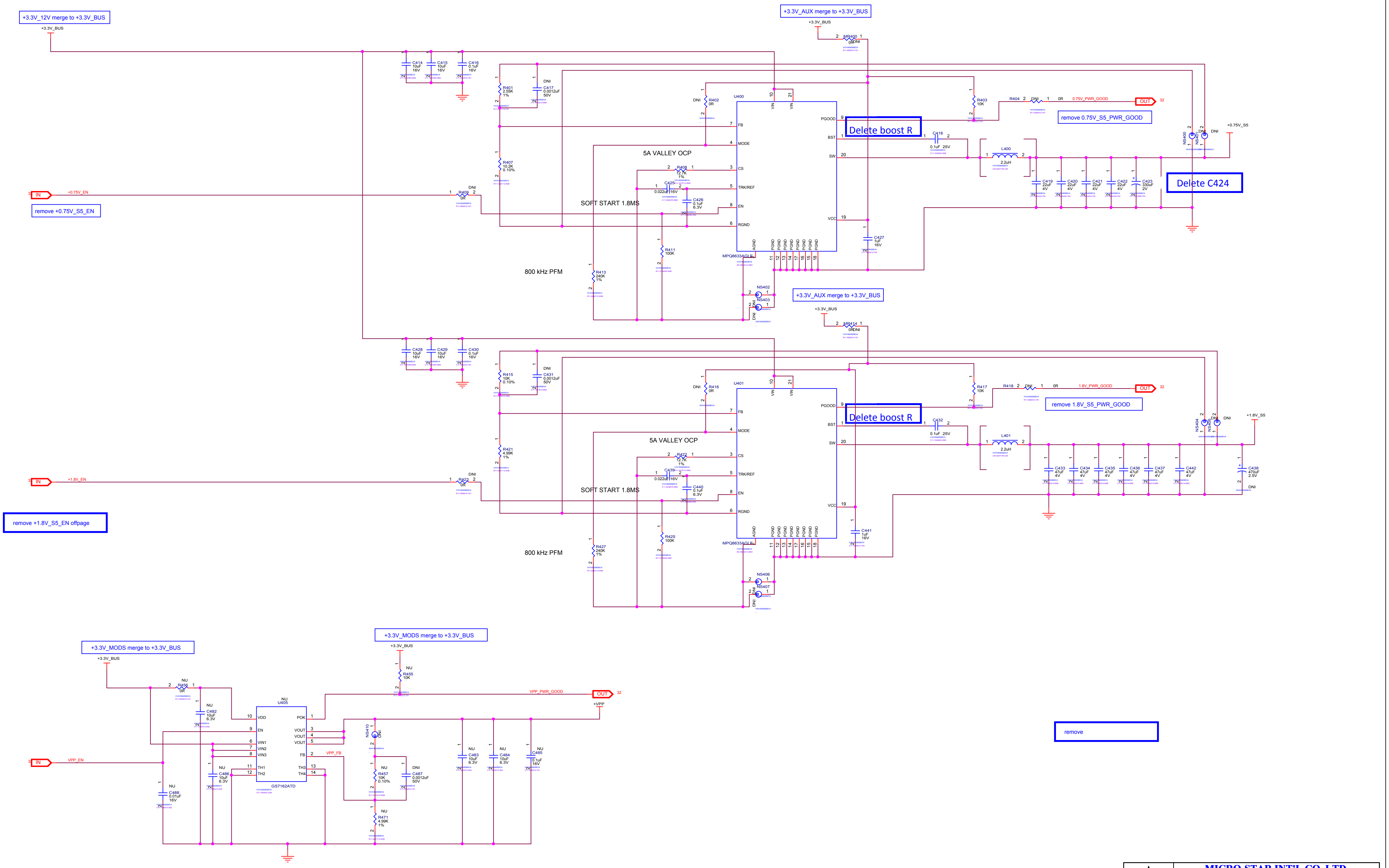
Size Custom	Document Description 0018 USB_VBUS 5V S5_Rails	Rev 2.0
Date: Wednesday, May 19, 2021	Sheet 18 of 37	


+3.3V_12V merge to +3.3V_BUS
+3.3V_BUS
+3.3V_AUX merge to +3.3V_BUS
MR400 0R DNI
C414 10uF 16V
C415 10uF 16V
C416 0.1uF 16V
R401 2.55K 1%
C417 0.0012uF 50V DNI
R402 0R DNI
U400
VIN
VIN
PGOOD
BST
SW
VCC
FB
MODE
CS
TRK/REF
EN
RGND
AGND
PGND
MPQ8633AGLE
Delete boost R
R403 10K
R404 DNI 0R
0.75V_PWR_GOOD
OUT
32
remove 0.75V_S5_PWR_GOOD
C418 0.1uF 25V
L400 2.2uH
C419 22uF 4V
C420 22uF 4V
C421 22uF 4V
C422 22uF 4V
C423 330uF 2V
Delete C424
NS400
NS401
DNI
+0.75V_S5
5A VALLEY OCP
R407 10.2K 0.10%
R408 12.7K 1%
C425 0.022uF 16V
C426 0.1uF 6.3V
SOFT START 1.8MS
IN
+0.75V_EN
R409 0R DNI
remove +0.75V_S5_EN
C427 1uF 16V
R411 100K
R413 240K 1%
800 kHz PFM
NS402
NS403
+3.3V_AUX merge to +3.3V_BUS
MR414 0R DNI
C428 10uF 16V
C429 10uF 16V
C430 0.1uF 16V
R415 10K 0.10%
C431 0.0012uF 50V DNI
R416 0R DNI
U401
R417 10K
R418 DNI 0R
1.8V_PWR_GOOD
remove 1.8V_S5_PWR_GOOD
C432 0.1uF 25V
L401 2.2uH
C433 47uF 4V
C434 47uF 4V
C435 47uF 4V
C436 47uF 4V
C437 47uF 4V
C442 47uF 4V
C438 470uF 2.5V DNI
NS404
NS405
+1.8V_S5
R421 4.99K 1%
R422 12.7K 1%
C439 0.022uF 16V
C440 0.1uF 6.3V
+1.8V_EN
R423 0R DNI
remove +1.8V_S5_EN offpage
C441 1uF 16V
R425 100K
R427 240K 1%
NS406
NS407
+3.3V_MODS merge to +3.3V_BUS
+3.3V_MODS merge to +3.3V_BUS
R456 0R NU
C482 10uF 6.3V NU
R455 10K NU
U405 NU
VDD
POK
EN
VOUT
VIN1
VIN2
VIN3
FB
TH1
TH2
TH3
TH4
GS7162ATD
VPP_PWR_GOOD
+VPP
VPP_EN
VPP_FB
NS410 DNI
R457 10K 0.10% NU
C487 0.0012uF 50V DNI
R471 4.99K 1% NU
C483 10uF 6.3V NU
C484 10uF 6.3V NU
C485 0.1uF 16V NU
C486 10uF 6.3V NU
C488 0.01uF 16V NU
remove

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Size: Custom
Document Description: 0019 REG 1.8V 0.75V VPP
Rev: 2.0
Date: Wednesday, May 19, 2021
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remove

remove +5V_S5 offpage

MVDD_PWR change to +12V_BUS_B

remove

remove

remove

MICRO-STAR INT'L CO.,LTD		
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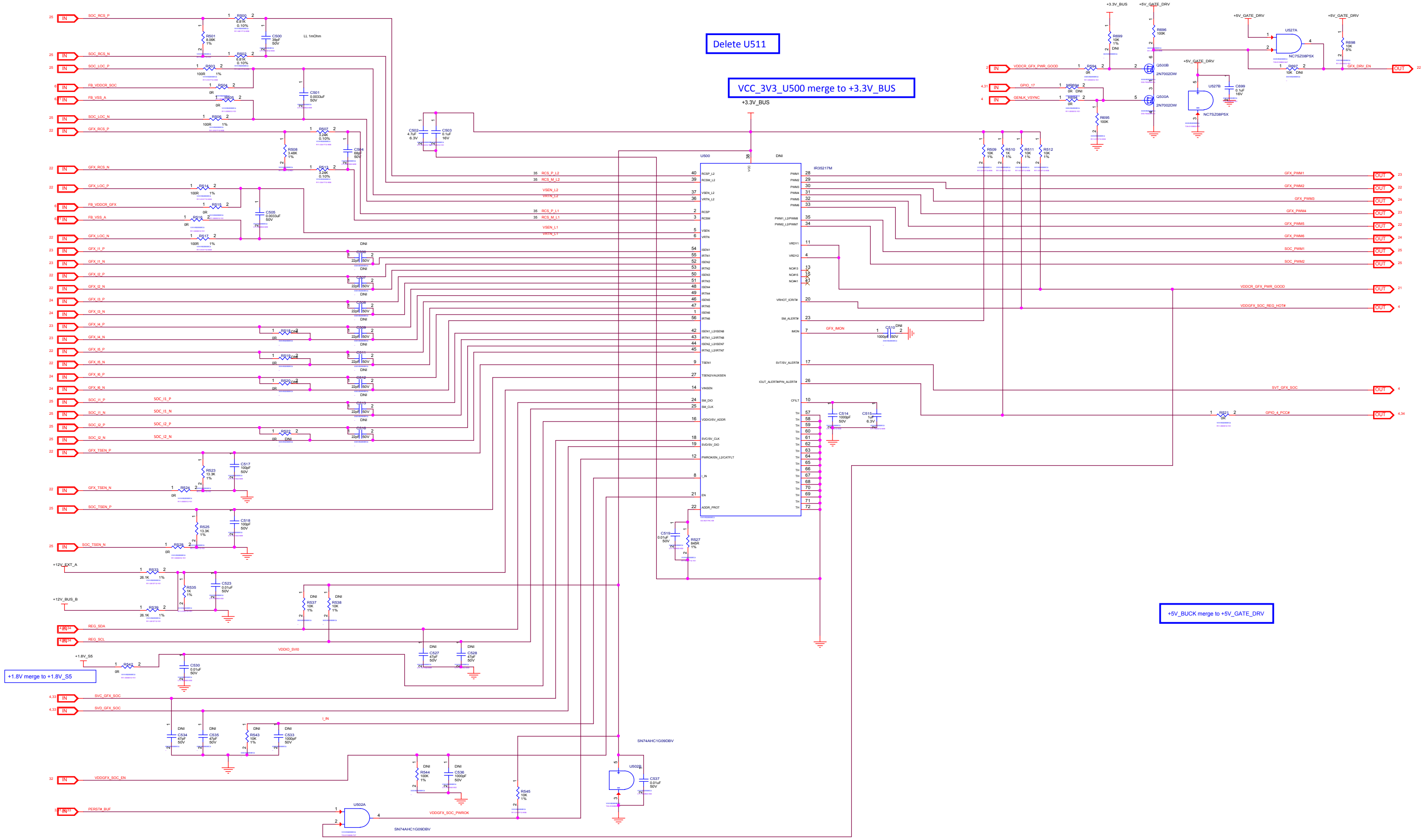
Size Custom	Document Description 0020 MODS CONTROL & POWER	Rev 2.0
Date: Wednesday, May 19, 2021	Sheet 20 of 37	


SOC_RCS_P
SOC_RCS_N
SOC_LOC_P
FB_VDDCR_SOC
FB_VSS_A
SOC_LOC_N
GFX_RCS_P
GFX_RCS_N
GFX_LOC_P
FB_VDDCR_GFX
GFX_LOC_N
GFX_I1_P
GFX_I1_N
GFX_I2_P
GFX_I2_N
GFX_I3_P
GFX_I3_N
GFX_I4_P
GFX_I4_N
GFX_I5_P
GFX_I5_N
GFX_I6_P
GFX_I6_N
SOC_I1_P
SOC_I1_N
SOC_I2_P
SOC_I2_N
GFX_TSEN_P
GFX_TSEN_N
SOC_TSEN_P
SOC_TSEN_N
+12V_EXT_A
+12V_BUS_B
REG_SDA
REG_SCL
+1.8V_S5
VDDIO_SVI0
SVC_GFX_SOC
SVD_GFX_SOC
I_IN
VDDGFX_SOC_EN
PERST#_BUF
IN
R500 6.81K 0.10%
R501 8.06K 1%
C500 39pF 50V
LL 1mOhm
R502 6.81K 0.10%
R503 100R 1%
R504 0R
R505 0R
C501 0.0033uF 50V
R506 100R 1%
R507 3.24K 0.10%
R508 3.48K 1%
C504 68pF 50V
R513 3.24K 0.10%
R514 100R 1%
R515 0R
R516 0R
C505 0.0033uF 50V
R517 100R 1%
C506 22pF 50V DNI
C507 22pF 50V DNI
C508 22pF 50V DNI
C509 22pF 50V DNI
C511 22pF 50V DNI
C512 22pF 50V DNI
C513 22pF 50V DNI
C516 22pF 50V DNI
R518 0R DNI
R519 0R DNI
R520 0R DNI
R522 0R DNI
R523 13.3K 1%
C517 100pF 50V
R524 0R
R525 13.3K 1%
C518 100pF 50V
R528 0R
R533 26.1K 1%
R535 1K 1%
C523 0.01uF 50V
R539 26.1K 1%
R537 10K 1% DNI
R538 10K 1% DNI
R542 0R
C530 0.01uF 50V
C527 47pF 50V DNI
C528 47pF 50V DNI
C534 47pF 50V DNI
C535 47pF 50V DNI
R543 10K 1% DNI
C533 1000pF 50V DNI
R544 100K 1% DNI
C536 1000pF 50V DNI
R545 10K 1%
U502A
U502B
SN74AHC1G09DBV
VDDGFX_SOC_PWROK
C537 0.01uF 50V
C502 4.7uF 6.3V
C503 0.1uF 16V
+3.3V_BUS
U500
DNI
IR35217M
VCC 38
RCS_P_L2
RCS_M_L2
VSEN_L2
VRTN_L2
RCS_P_L1
RCS_M_L1
VSEN_L1
VRTN_L1
40 RCSP_L2
39 RCSM_L2
37 VSEN_L2
36 VRTN_L2
2 RCSP
3 RCSM
5 VSEN
6 VRTN
54 ISEN1
55 IRTN1
52 ISEN2
53 IRTN2
50 ISEN3
51 IRTN3
48 ISEN4
49 IRTN4
46 ISEN5
47 IRTN5
1 ISEN6
56 IRTN6
42 ISEN1_L2/ISEN8
43 IRTN1_L2/IRTN8
44 ISEN2_L2/ISEN7
45 IRTN2_L2/IRTN7
9 TSEN1
27 TSEN2/VAUXSEN
14 VINSEN
24 SM_DIO
25 SM_CLK
16 VDDIO/SV_ADDR
18 SVC/SV_CLK
19 SVD/SV_DIO
12 PWROK/EN_L2/CATFLT
8 I_IN
21 EN
22 ADDR_PROT
PWM1 28
PWM2 29
PWM3 30
PWM4 31
PWM5 32
PWM6 33
PWM1_L2/PWM8 35
PWM2_L2/PWM7 34
VRDY1 11
VRDY2 4
NC#13 13
NC#15 15
NC#41 41
VRHOT_ICRIT# 20
SM_ALERT# 23
IMON 7
SVT/SV_ALERT# 17
IOUT_ALERT#/PIN_ALERT# 26
CFILT 10
TH 57 58 59 60 61 62 63 64 65 66 67 68 70 69 71 72
C519 0.01uF 50V
R527 845R 1%
GFX_IMON
C510 1000pF 50V DNI
C514 1000pF 50V
C515 1uF 6.3V
R509 10K 1%
R510 1K 1%
R511 10K 1%
R512 10K 1%
GFX_PWM1
GFX_PWM2
GFX_PWM3
GFX_PWM4
GFX_PWM5
GFX_PWM6
SOC_PWM1
SOC_PWM2
VDDCR_GFX_PWR_GOOD
VDDGFX_SOC_REG_HOT#
SVT_GFX_SOC
R521 0R
GPIO_4_PCC#
OUT
+5V_GATE_DRV
R699 10K 1% DNI
R696 100K
R594 0R
Q500B 2N7002DW
Q500A 2N7002DW
GPIO_17
GENLK_VSYNC
MR694 0R DNI
R694 0R
R695 100K
U527A NC7SZ08P5X
U527B NC7SZ08P5X
C699 0.1uF 16V
R697 10K DNI
R698 10K 5%
GFX_DRV_EN

Delete U511

VCC_3V3_U500 merge to +3.3V_BUS

+1.8V merge to +1.8V_S5

+5V_BUCK merge to +5V_GATE_DRV

6+2 PHASES：I32-35217HC-I08
5+1 PHASES：I32-35217JC-I08

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	MS-V502		
	Size D	Document Description 0021 GFX & SOC CONTROLLER	Rev 2.0
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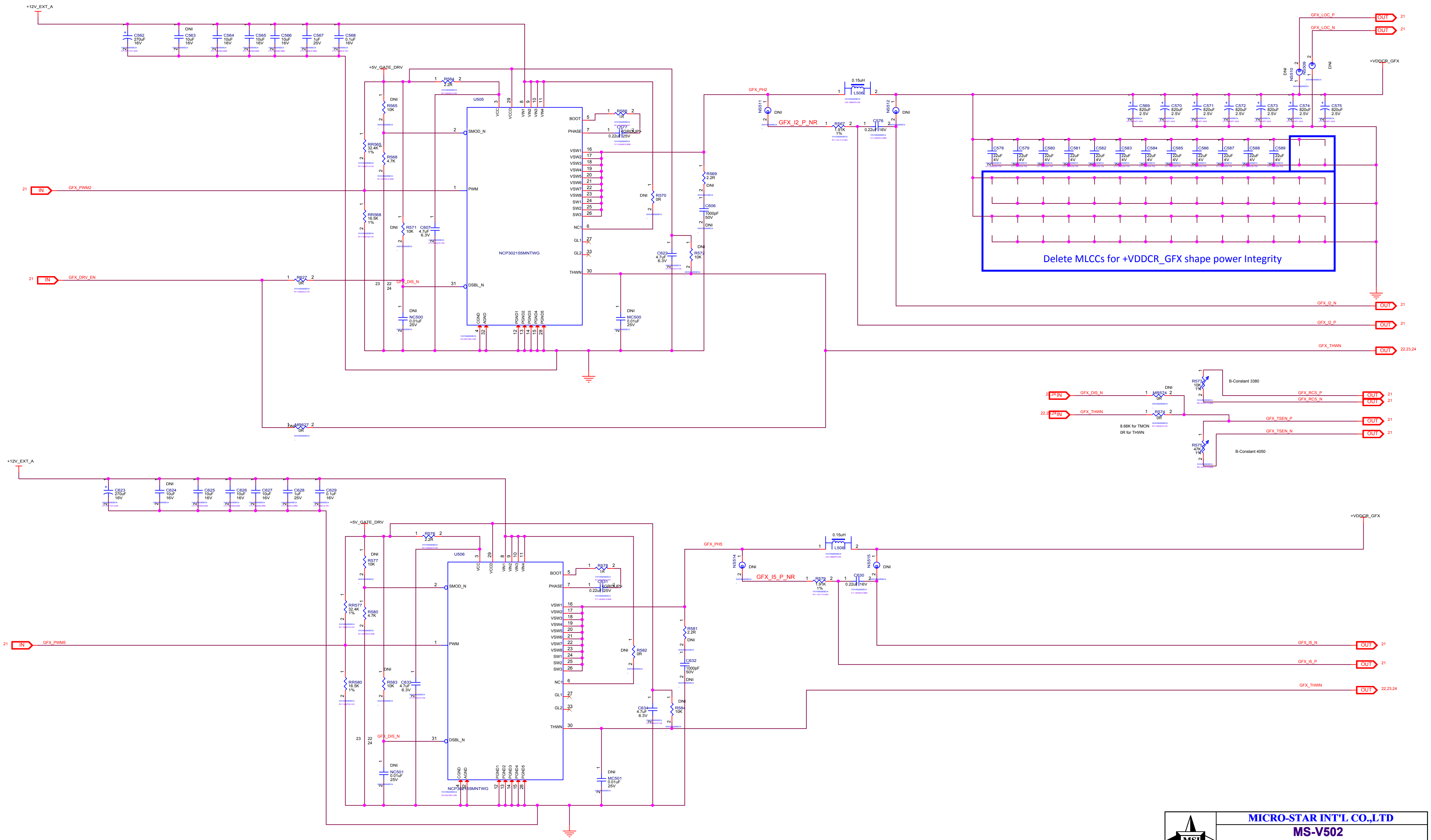
+12V_EXT_A
C562 270uF 16V
DNI C563 10uF 16V
C564 10uF 16V
C565 10uF 16V
C566 10uF 16V
C567 1uF 25V
C568 0.1uF 16V
+5V_GATE_DRV
R564 2.2R
U505
DNI R565 10K
RR565 32.4K 1%
R568 4.7K
RR568 16.5K 1%
DNI R571 10K
C607 4.7uF 6.3V
DNI NC500 0.01uF 25V
21 IN GFX_PWM2
21 IN GFX_DRV_EN
R627 0R
DNI MR627 0R
GFX_DIS_N
VCC VCCD VIN1 VIN2 VIN3 VIN4
SMOD_N
PWM
DSBL_N
CGND AGND
PGND1 PGND2 PGND3 PGND4 PGND5
BOOT PHASE
VSW1 VSW2 VSW3 VSW4 VSW5 VSW6 VSW7 VSW8 SW1 SW2 SW3
NC1 GL1 GL2 THWN
NCP302155MNTWG
R566 1R
C577 0.22uF 25V <GROUP>
DNI R570 0R
R569 2.2R DNI
C606 1000pF 50V DNI
C622 4.7uF 6.3V
DNI R572 10K
DNI MC500 0.01uF 25V
GFX_PH2
0.15uH L506
NS511 DNI
NS512 DNI
GFX_I2_P_NR
R567 1.91K 1%
C576 0.22uF 16V
GFX_LOC_P OUT 21
GFX_LOC_N OUT 21
DNI NS510
NS509 DNI
+VDDCR_GFX
C569 820uF 2.5V
C570 820uF 2.5V
C571 820uF 2.5V
C572 820uF 2.5V
C573 820uF 2.5V
C574 820uF 2.5V
C575 820uF 2.5V
C578 22uF 4V
C579 22uF 4V
C580 22uF 4V
C581 22uF 4V
C582 22uF 4V
C583 22uF 4V
C584 22uF 4V
C585 22uF 4V
C586 22uF 4V
C587 22uF 4V
C588 22uF 4V
C589 22uF 4V
GFX_I2_N OUT 21
GFX_I2_P OUT 21
GFX_THWN OUT 22,23,24
R573 10K 1%
B-Constant 3380
22,24 IN GFX_DIS_N
DNI MR574 0R
22,23,24 IN GFX_THWN
R574 0R
8.66K for TMON
0R for THWN
GFX_RCS_P OUT 21
GFX_RCS_N OUT 21
GFX_TSEN_P OUT 21
GFX_TSEN_N OUT 21
R575 47K 1%
B-Constant 4050
+12V_EXT_A
C623 270uF 16V
DNI C624 10uF 16V
C625 10uF 16V
C626 10uF 16V
C627 10uF 16V
C628 1uF 25V
C629 0.1uF 16V
+5V_GATE_DRV
R576 2.2R
U506
DNI R577 10K
RR577 32.4K 1%
R580 4.7K
21 IN GFX_PWM5
RR580 16.5K 1%
DNI R583 10K
C633 4.7uF 6.3V
GFX_DIS_N
DNI NC501 0.01uF 25V
NCP302155MNTWG
R578 1R
C631 0.22uF 25V <GROUP>
DNI R582 0R
R581 2.2R DNI
C632 1000pF 50V DNI
C634 4.7uF 6.3V
DNI R584 10K
DNI MC501 0.01uF 25V
GFX_PH5
0.15uH L508
NS514 DNI
NS515 DNI
GFX_I5_P_NR
R579 1.91K 1%
C630 0.22uF 16V
+VDDCR_GFX
GFX_I5_N OUT 21
GFX_I5_P OUT 21
GFX_THWN OUT 22,23,24

Delete MLCCs for +VDDCR_GFX shape power Integrity

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Custom	0022 VDDCR_GFX PHASES 2 and 5	2.0

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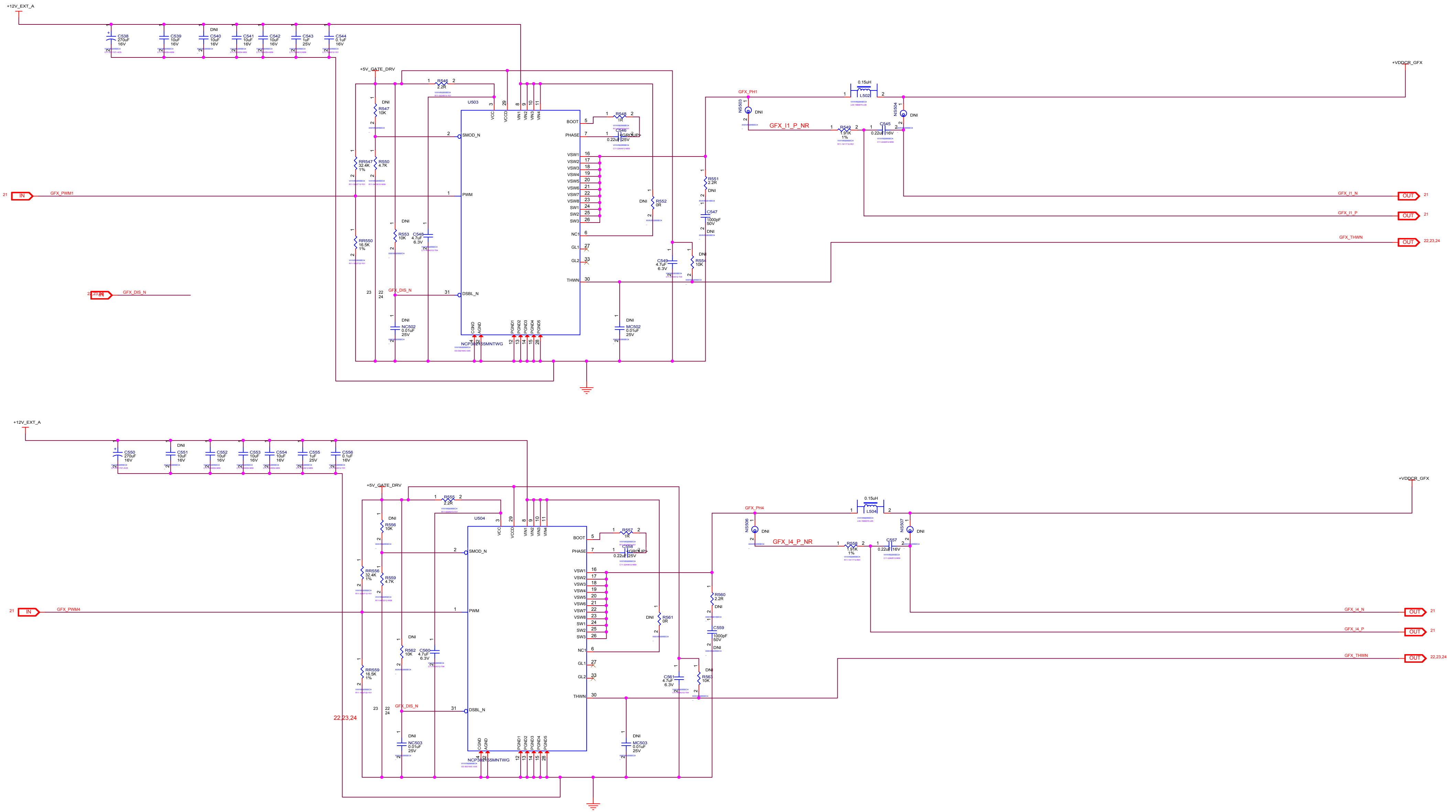
+12V_EXT_A
C538 270uF 16V
C539 10uF 16V
DNI C540 10uF 16V
C541 10uF 16V
C542 10uF 16V
C543 1uF 25V
C544 0.1uF 16V
+5V_GATE_DRV
R546 2.2R
U503
DNI R547 10K
RR547 32.4K 1%
R550 4.7K
21 IN GFX_PWM1
DNI R553 10K
C548 4.7uF 6.3V
RR550 16.5K 1%
22,23,24 IN GFX_DIS_N
23 22 24 GFX_DIS_N
DNI NC502 0.01uF 25V
VCC VCCD VIN1 VIN2 VIN3 VIN4
SMOD_N PWM DSBL_N
BOOT PHASE
VSW1 VSW2 VSW3 VSW4 VSW5 VSW6 VSW7 VSW8 SW1 SW2 SW3
NC1 GL1 GL2 THWN
CGND AGND PGND1 PGND2 PGND3 PGND4 PGND5
NCP302155MNTWG
R548 1R
C546 0.22uF 25V <GROUP>
DNI R552 0R
R551 2.2R DNI
C547 1000pF 50V DNI
C549 4.7uF 6.3V
DNI R554 10K
DNI MC502 0.01uF 25V
GFX_PH1
0.15uH L502
NS503 DNI
NS504 DNI
GFX_I1_P_NR
R549 1.91K 1%
C545 0.22uF 16V
+VDDCR_GFX
GFX_I1_N OUT 21
GFX_I1_P OUT 21
GFX_THWN OUT 22,23,24
+12V_EXT_A
C550 270uF 16V
DNI C551 10uF 16V
C552 10uF 16V
C553 10uF 16V
C554 10uF 16V
C555 1uF 25V
C556 0.1uF 16V
+5V_GATE_DRV
R555 2.2R
U504
DNI R556 10K
RR556 32.4K 1%
R559 4.7K
21 IN GFX_PWM4
DNI R562 10K
C560 4.7uF 6.3V
RR559 16.5K 1%
22,23,24
23 22 24 GFX_DIS_N
DNI NC503 0.01uF 25V
NCP302155MNTWG
R557 1R
C558 0.22uF 25V <GROUP>
DNI R561 0R
R560 2.2R DNI
C559 1000pF 50V DNI
C561 4.7uF 6.3V
DNI R563 10K
DNI MC503 0.01uF 25V
GFX_PH4
0.15uH L504
NS506 DNI
NS507 DNI
GFX_I4_P_NR
R558 1.91K 1%
C557 0.22uF 16V
+VDDCR_GFX
GFX_I4_N OUT 21
GFX_I4_P OUT 21
GFX_THWN OUT 22,23,24

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Size
Custom

Document Description
0023 VDDCR_GFX PHASES 1 and 4

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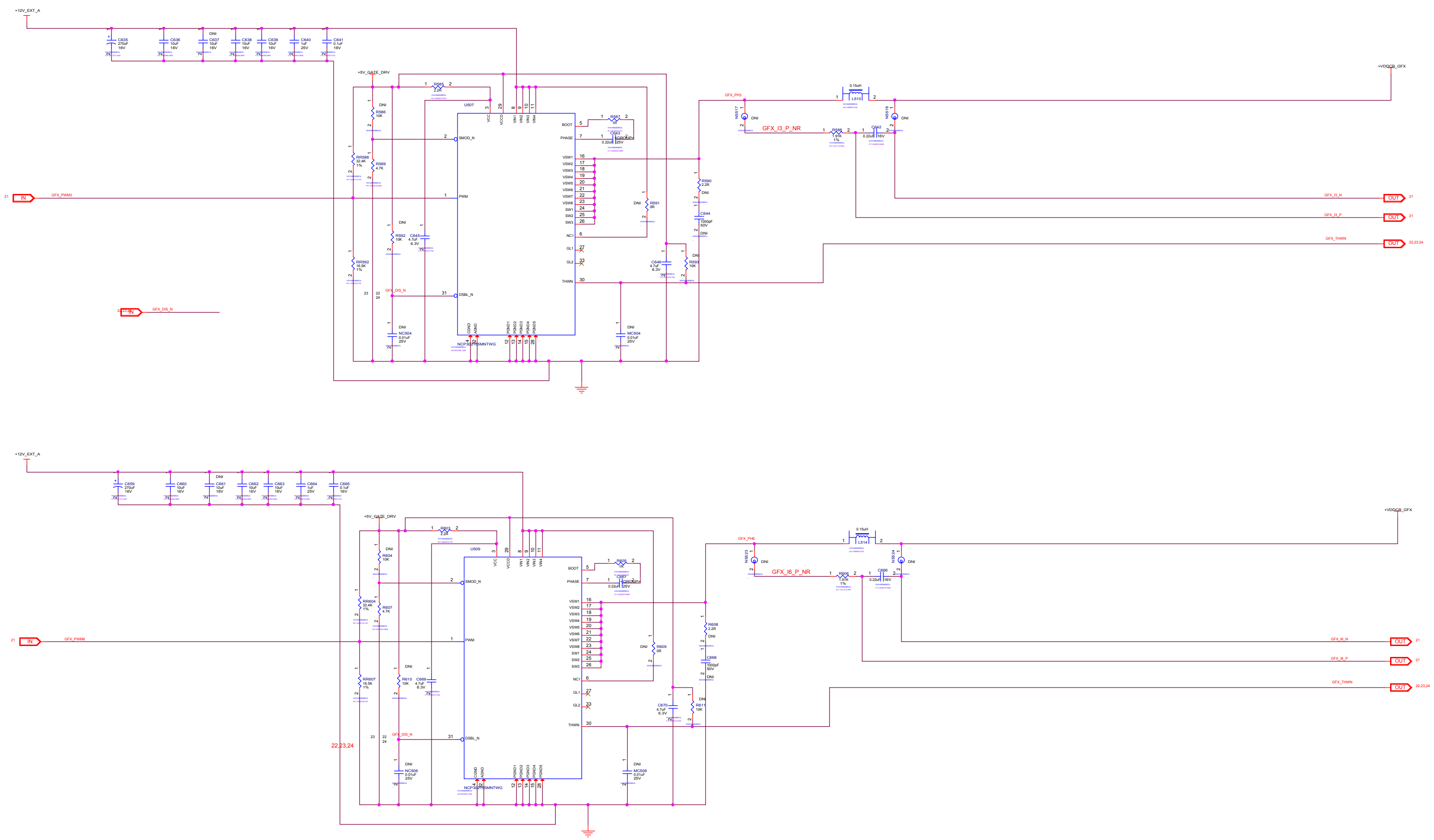
+12V_EXT_A
C635 270uF 16V
C636 10uF 16V
DNI C637 10uF 16V
C638 10uF 16V
C639 10uF 16V
C640 1uF 25V
C641 0.1uF 16V
+5V_GATE_DRV
R585 2.2R
U507
VCC
VCCD
VIN1
VIN2
VIN3
VIN4
DNI R586 10K
RR586 32.4K 1%
R589 4.7K
SMOD_N
21 IN GFX_PWM3
PWM
DNI R592 10K
C645 4.7uF 6.3V
RR592 16.5K 1%
GFX_DIS_N
DSBL_N
22,23,24 IN GFX_DIS_N
DNI NC504 0.01uF 25V
CGND
AGND
PGND1
PGND2
PGND3
PGND4
PGND5
NCP302155MNTWG
BOOT
PHASE
R587 1R
C643 0.22uF 25V
<GROUP>
VSW1
VSW2
VSW3
VSW4
VSW5
VSW6
VSW7
VSW8
SW1
SW2
SW3
NC1
GL1
GL2
THWN
DNI R591 0R
DNI MC504 0.01uF 25V
C646 4.7uF 6.3V
DNI R593 10K
R590 2.2R DNI
C644 1000pF 50V DNI
GFX_PH3
0.15uH L510
NS517 DNI
NS518 DNI
GFX_I3_P_NR
R588 1.91K 1%
C642 0.22uF 16V
+VDDCR_GFX
GFX_I3_N OUT 21
GFX_I3_P OUT 21
GFX_THWN OUT 22,23,24
+12V_EXT_A
C659 270uF 16V
C660 10uF 16V
DNI C661 10uF 16V
C662 10uF 16V
C663 10uF 16V
C664 1uF 25V
C665 0.1uF 16V
+5V_GATE_DRV
R603 2.2R
U509
DNI R604 10K
RR604 32.4K 1%
R607 4.7K
21 IN GFX_PWM6
DNI R610 10K
C669 4.7uF 6.3V
RR607 16.5K 1%
GFX_DIS_N
22,23,24
DNI NC506 0.01uF 25V
NCP302155MNTWG
R605 1R
C667 0.22uF 25V
<GROUP>
DNI R609 0R
DNI MC506 0.01uF 25V
C670 4.7uF 6.3V
DNI R611 10K
R608 2.2R DNI
C668 1000pF 50V DNI
GFX_PH6
0.15uH L514
NS523 DNI
NS524 DNI
GFX_I6_P_NR
R606 1.91K 1%
C666 0.22uF 16V
+VDDCR_GFX
GFX_I6_N OUT 21
GFX_I6_P OUT 21
GFX_THWN OUT 22,23,24

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Size	Document Description	Rev
D	0024 VDDCR_GFX PHASES 3 and 6	2.0

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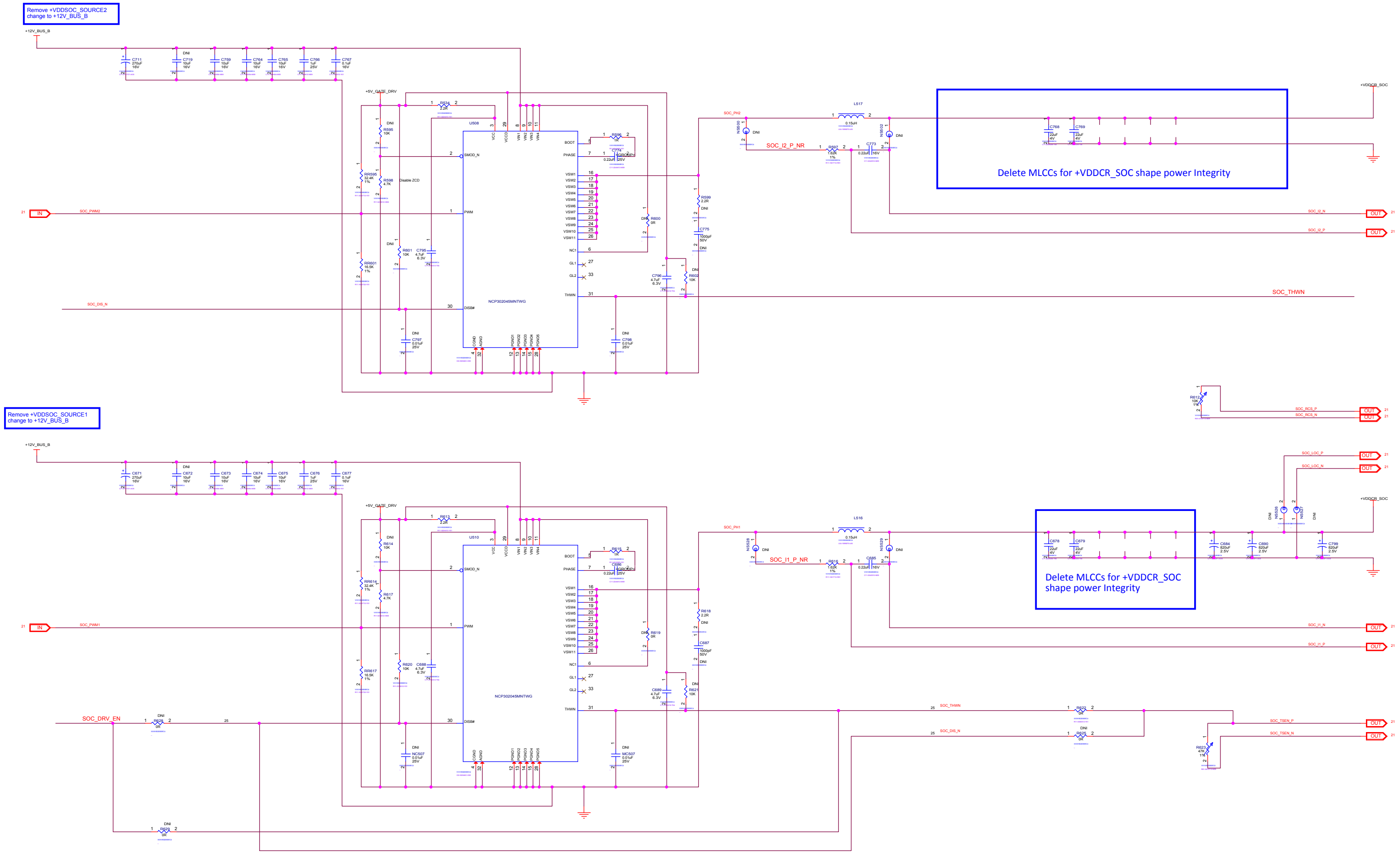
+12V_BUS_B
C711 270uF 16V
DNI C719 10uF 16V
C759 10uF 16V
C764 10uF 16V
C765 10uF 16V
C766 1uF 25V
C767 0.1uF 16V
+5V_GATE_DRV
R534 2.2R
U508
DNI R595 10K
RR595 32.4K 1%
R598 4.7K
Disable ZCD
VCC VCCD VIN1 VIN2 VIN3 VIN4
BOOT
PHASE
SMOD_N
PWM
DISB#
VSW1 VSW2 VSW3 VSW4 VSW5 VSW6 VSW7 VSW8 VSW9 VSW10 VSW11
NC1
GL1
GL2
THWN
CGND AGND PGND1 PGND2 PGND3 PGND4 PGND5
NCP302045MNTWG
R596 1R
C774 0.22uF 25V
<GROUP>
DNI R600 0R
DNI R601 10K
C795 4.7uF 6.3V
RR601 16.5K 1%
DNI C797 0.01uF 25V
DNI C798 0.01uF 25V
C796 4.7uF 6.3V
DNI R602 10K
R599 2.2R DNI
C775 1000pF 50V DNI
21 IN SOC_PWM2
SOC_DIS_N
SOC_PH2
L517 0.15uH
NS500 DNI
NS502 DNI
SOC_I2_P_NR
R597 1.62K 1%
C773 0.22uF 16V
C768 22uF 4V
C769 22uF 4V
+VDDCR_SOC
SOC_I2_N OUT 21
SOC_I2_P OUT 21
SOC_THWN
R612 10K 1%
SOC_RCS_P OUT 21
SOC_RCS_N OUT 21
C671 270uF 16V
DNI C672 10uF 16V
C673 10uF 16V
C674 10uF 16V
C675 10uF 16V
C676 1uF 25V
C677 0.1uF 16V
R613 2.2R
U510
DNI R614 10K
RR614 32.4K 1%
R617 4.7K
21 IN SOC_PWM1
R615 1R
C686 0.22uF 25V
DNI R619 0R
R620 10K
C688 4.7uF 6.3V
RR617 16.5K 1%
DNI NC507 0.01uF 25V
DNI MC507 0.01uF 25V
C689 4.7uF 6.3V
DNI R621 10K
R618 2.2R DNI
C687 1000pF 50V DNI
SOC_DRV_EN
DNI R628 0R
DNI R629 0R
SOC_PH1
L516 0.15uH
NS528 DNI
NS529 DNI
SOC_I1_P_NR
R616 1.62K 1%
C685 0.22uF 16V
C678 22uF 4V
C679 22uF 4V
C684 820uF 2.5V
C690 820uF 2.5V
C799 820uF 2.5V
NS526 DNI
NS527 DNI
SOC_LOC_P OUT 21
SOC_LOC_N OUT 21
SOC_I1_N OUT 21
SOC_I1_P OUT 21
25 SOC_THWN
25 SOC_DIS_N
R622 0R
DNI R625 0R
R623 47K 1%
SOC_TSEN_P OUT 21
SOC_TSEN_N OUT 21

Remove +VDDSOC_SOURCE2
change to +12V_BUS_B

Delete MLCCs for +VDDCR_SOC shape power Integrity

Remove +VDDSOC_SOURCE1
change to +12V_BUS_B

Delete MLCCs for +VDDCR_SOC
shape power Integrity

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Size D

Document Description 0025 VDDCR_SOC

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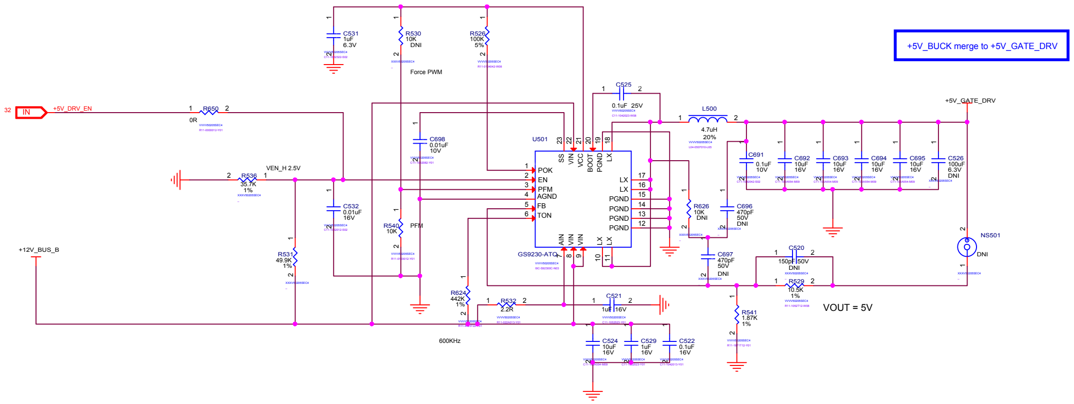
+5V_BUCK merge to +5V_GATE_DRV
32
IN
+5V_DRV_EN
R650
0R
VEN_H 2.5V
R536
35.7K
1%
+12V_BUS_B
C531
1uF
6.3V
R530
10K
DNI
R526
100K
5%
Force PWM
C698
0.01uF
10V
C532
0.01uF
16V
R531
49.9K
1%
R540
10K
PFM
U501
SS
VIN
VCC
BOOT
PGND
LX
POK
EN
PFM
AGND
FB
TON
LX
LX
PGND
PGND
PGND
PGND
AIN
VIN
VIN
LX
LX
GS9230-ATQ
R624
442K
1%
R532
2.2R
C521
1uF 16V
600KHz
C524
10uF
16V
C529
1uF
16V
C522
0.1uF
16V
C525
0.1uF 25V
L500
4.7uH
20%
R626
10K
DNI
C696
470pF
50V
DNI
C697
470pF
50V
DNI
C691
0.1uF
10V
C692
10uF
16V
C693
10uF
16V
C694
10uF
16V
C695
10uF
16V
C526
100uF
6.3V
DNI
+5V_GATE_DRV
NS501
DNI
C520
150pF 50V
DNI
R529
10.5K
1%
R541
1.87K
1%
VOUT = 5V

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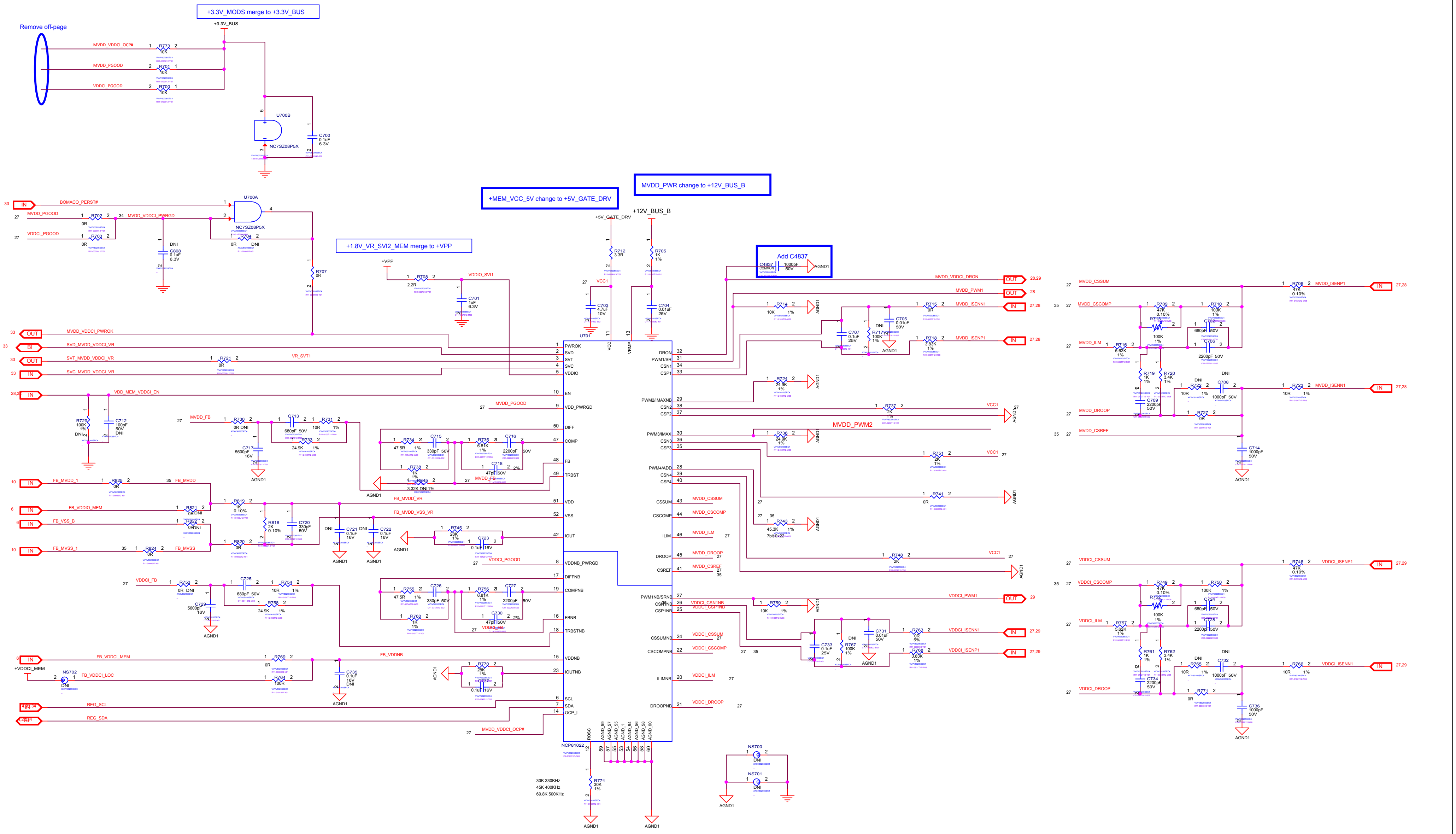
+3.3V_MODS merge to +3.3V_BUS

Remove off-page

+MEM_VCC_5V change to +5V_GATE_DRV

MVDD_PWR change to +12V_BUS_B

+1.8V_VR_SVI2_MEM merge to +VPP

Add C4837

30K 330KHz
45K 400KHz
69.8K 500KHz

+3.3V_BUS
MVDD_VDDCI_OCP#
MVDD_PGOOD
VDDCI_PGOOD
R773 10K
R701 10K
R700 10K
U700B
NC7SZ08P5X
C700 0.1uF 6.3V
U700A
BOMACO_PERST#
MVDD_VDDCI_PWRGD
R702 0R
R703 0R
R704 0R DNI
C808 0.1uF 6.3V DNI
R707 0R
MVDD_VDDCI_PWROK
SVD_MVDD_VDDCI_VR
SVT_MVDD_VDDCI_VR
SVC_MVDD_VDDCI_VR
R721 0R
VR_SVT1
VDD_MEM_VDDCI_EN
R729 100K 1% DNI
C712 100pF 50V DNI
+VPP
R708 2.2R
VDDIO_SVI1
C701 1uF 6.3V
+5V_GATE_DRV
+12V_BUS_B
R712 3.3R
R705 1K 1%
VCC1
C703 4.7uF 10V
C704 0.01uF 25V
C4837 1000pF 50V
AGND1
U701
NCP81022
PWROK
SVD
SVT
SVC
VDDIO
EN
VDD_PWRGD
DIFF
COMP
FB
TRBST
VDD
VSS
IOUT
VDDNB_PWRGD
DIFFNB
COMPNB
FBNB
TRBSTNB
VDDNB
IOUTNB
SCL
SDA
OCP_L
ROSC
VCC
VRMP
DRON
PWM1/SR
CSN1
CSP1
PWM2/IMAXNB
CSN2
CSP2
PWM3/IMAX
CSN3
CSP3
PWM4/ADD
CSN4
CSP4
CSSUM
CSCOMP
ILIM
DROOP
CSREF
PWM1NB/SRNB
CSN1NB
CSP1NB
CSSUMNB
CSCOMPNB
ILIMNB
DROOPNB
AGND_59
AGND_57
AGND_55
AGND_1
AGND_54
AGND_56
AGND_58
AGND_60
MVDD_VDDCI_DRON
MVDD_PWM1
MVDD_ISENN1
MVDD_ISENP1
MVDD_PWM2
R714 10K 1%
R715 0R
R718 3.83K 1%
C705 0.01uF 50V
C707 0.1uF 25V
R717 100K 1% DNI
R724 24.9K 1%
R737 2K 1%
R736 24.9K 1%
R751 2K 1%
R741 0R
R743 45.3K 1%
7bit 0x22
R748 2K
MVDD_CSSUM
MVDD_CSCOMP
MVDD_ILM
MVDD_DROOP
MVDD_CSREF
MVDD_FB
R730 0R DNI
C713 680pF 50V
R731 10R 1%
R733 24.9K 1%
C717 5600pF 16V
R734 47.5R 1%
C715 330pF 50V
R735 6.81K 1%
C716 2200pF 50V
R738 1K 1%
C718 47pF 50V 2%
R845 3.32K DNI 1%
MVDD_FB
FB_MVDD_1
FB_MVDD
FB_VDDIO_MEM
FB_VSS_B
FB_MVSS_1
FB_MVSS
R825 0R
R821 0R DNI
R822 0R DNI
R824 0R
R819 1K 0.10%
R818 2K 0.10%
R820 0R
C720 330pF 50V
C721 0.1uF 16V DNI
C722 0.1uF 16V DNI
FB_MVDD_VR
FB_MVDD_VSS_VR
R745 28K 1%
C723 0.1uF 16V
VDDCI_PGOOD
VDDCI_FB
R753 0R DNI
C729 5600pF 16V
C725 680pF 50V
R754 10R 1%
R758 24.9K 1%
R755 47.5R 1%
C726 330pF 50V
R756 6.81K 1%
C727 2200pF 50V
R760 1K 1%
C730 47pF 50V 2%
VDDCI_FB
FB_VDDCI_MEM
+VDDCI_MEM
NS702 DNI
FB_VDDCI_LOC
R769 0R
R764 100R
FB_VDDNB
C735 0.1uF 16V DNI
R770 28K 1%
C737 0.1uF 16V
REG_SCL
REG_SDA
MVDD_VDDCI_OCP#
R774 30K 1%
VDDCI_CSN1NB
VDDCI_CSP1NB
VDDCI_PWM1
R759 10K 1%
C733 0.1uF 25V
R767 100K 1% DNI
C731 0.01uF 50V
R763 0R 5%
R768 3.83K 1%
VDDCI_ISENN1
VDDCI_ISENP1
VDDCI_CSSUM
VDDCI_CSCOMP
VDDCI_ILM
VDDCI_DROOP
NS700 DNI
NS701 DNI
R706 47K 0.10%
R709 47K 0.10%
R710 100K 1%
R713 100K 1%
C702 680pF 50V
C706 2200pF 50V
R716 5.62K 1%
R719 1K 1%
R720 3.4K 1%
C709 2200pF 50V
R722 10R 1% DNI
C708 1000pF 50V DNI
R723 10R 1%
R727 0R
C714 1000pF 50V
R746 47K 0.10%
R749 47K 0.10%
R750 100K 1%
R752 100K 1%
C724 680pF 50V
C728 2200pF 50V
R757 5.62K 1%
R761 1K 1%
R762 3.4K 1%
C734 2200pF 50V
R765 10R 1% DNI
C732 1000pF 50V DNI
R766 10R 1%
R771 0R
C736 1000pF 50V
IN
OUT
BI

MICRO-STAR INT'L CO.,LTD

MS-V502

Size	Document Description	Rev
Custom	0027 MVDD_VDDCI CONTROLLER	2.0

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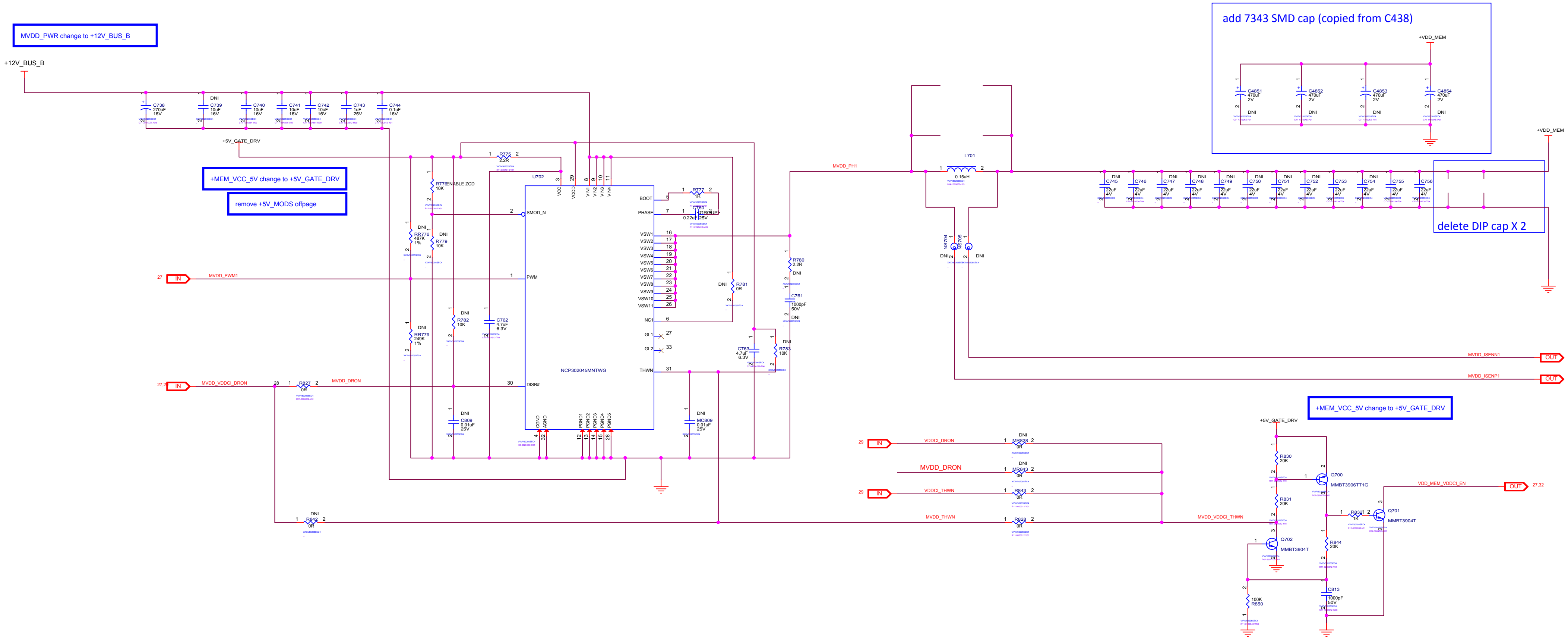

+12V_BUS_B
C738 270uF 16V
DNI C739 10uF 16V
C740 10uF 16V
C741 10uF 16V
C742 10uF 16V
C743 1uF 25V
C744 0.1uF 16V
+5V_GATE_DRV
R775 2.2R
U702
VCC 3
VCCD 29
VIN1 8
VIN2 9
VIN3 10
VIN4 11
R776 10K
ENABLE ZCD
SMOD_N 2
DNI RR776 487K 1%
DNI R779 10K
27 IN MVDD_PWM1
PWM 1
DNI R782 10K
C762 4.7uF 6.3V
DNI RR779 249K 1%
27,2 IN MVDD_VDDCI_DRON
28
R827 0R
MVDD_DRON
DISB# 30
DNI C809 0.01uF 25V
CGND 4
AGND 32
PGND1 12
PGND2 13
PGND3 14
PGND4 15
PGND5 28
NCP302045MNTWG
BOOT 5
R777 1R
PHASE 7
C760 0.22uF 25V
<GROUP>
VSW1 16
VSW2 17
VSW3 18
VSW4 19
VSW5 20
VSW6 21
VSW7 22
VSW8 23
VSW9 24
VSW10 25
VSW11 26
NC1 6
GL1 27
GL2 33
THWN 31
DNI R781 0R
DNI MC809 0.01uF 25V
C763 4.7uF 6.3V
DNI R783 10K
R780 2.2R DNI
C761 1000pF 50V DNI
DNI R842 0R
MVDD_PH1
L701 0.15uH
NS704 DNI
NS705 DNI
MVDD_ISENN1 OUT 27
MVDD_ISENP1 OUT 27
+VDD_MEM
C4851 470uF 2V DNI
C4852 470uF 2V DNI
C4853 470uF 2V DNI
C4854 470uF 2V DNI
DNI C745 22uF 4V
C746 22uF 4V
DNI C747 22uF 4V
DNI C748 22uF 4V
DNI C749 22uF 4V
DNI C750 22uF 4V
DNI C751 22uF 4V
DNI C752 22uF 4V
C753 22uF 4V
DNI C754 22uF 4V
C755 22uF 4V
C756 22uF 4V
+VDD_MEM
29 IN VDDCI_DRON
DNI MR828 0R
MVDD_DRON
DNI MR843 0R
29 IN VDDCI_THWN
R843 0R
MVDD_THWN
R828 0R
MVDD_VDDCI_THWN
+5V_GATE_DRV
R830 20K
Q700 MMBT3906TT1G
R831 20K
R832 1K
Q701 MMBT3904T
VDD_MEM_VDDCI_EN OUT 27,32
Q702 MMBT3904T
R844 20K
C813 1000pF 50V
100K R850

MVDD_PWR change to +12V_BUS_B

+MEM_VCC_5V change to +5V_GATE_DRV

remove +5V_MODS offpage

add 7343 SMD cap (copied from C438)

delete DIP cap X 2

+MEM_VCC_5V change to +5V_GATE_DRV

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Custom	0028 REG MVDD	2.0

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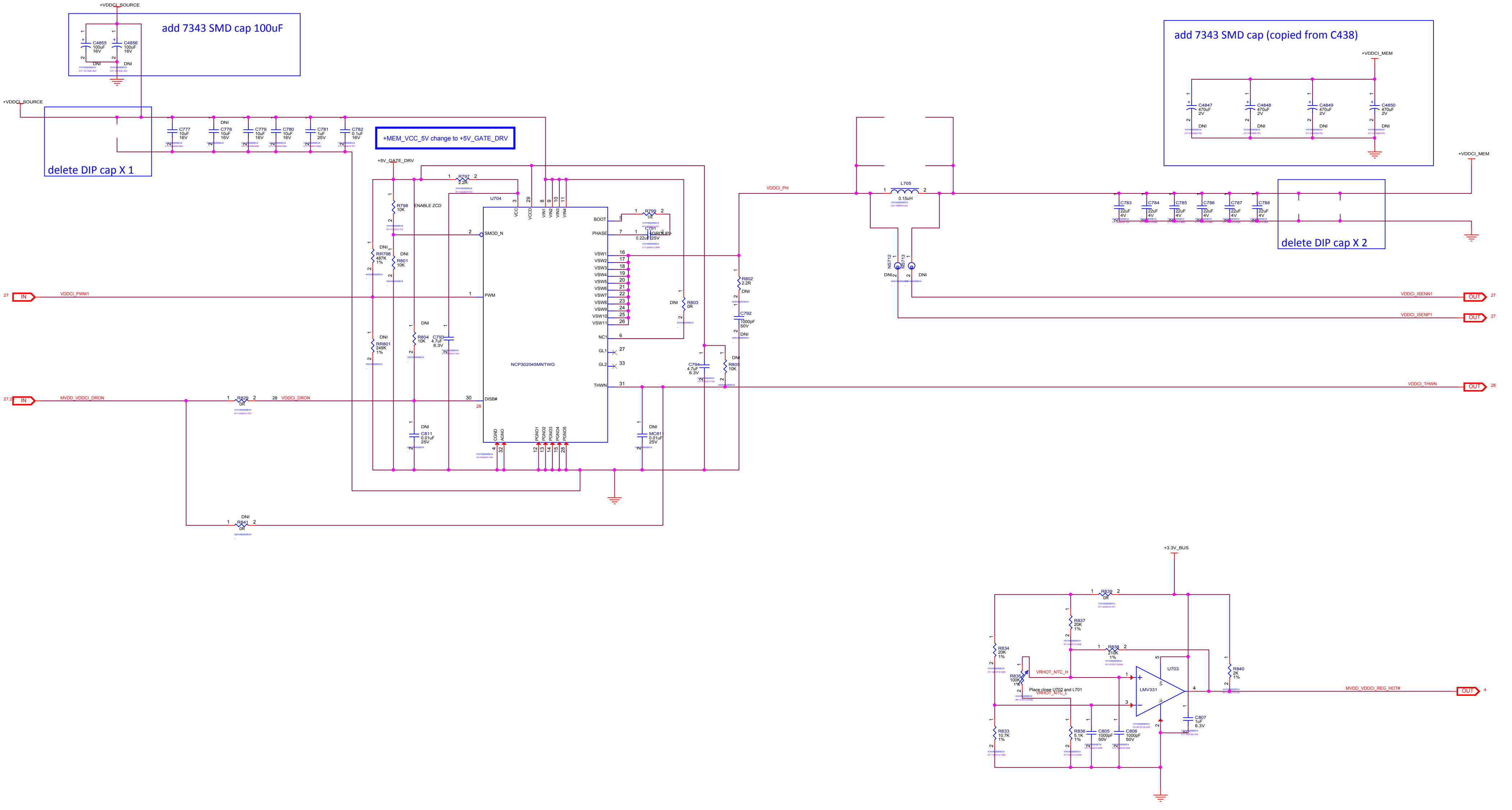
+VDDCI_SOURCE
add 7343 SMD cap 100uF
C4855 100uF 16V DNI
C4856 100uF 16V DNI
+VDDCI_SOURCE
delete DIP cap X 1
C777 10uF 16V
C778 10uF 16V DNI
C779 10uF 16V
C780 10uF 16V
C781 1uF 25V
C782 0.1uF 16V
+MEM_VCC_5V change to +5V_GATE_DRV
+5V_GATE_DRV
R797 2.2R
U704
R798 10K
ENABLE ZCD
RR798 487K 1% DNI
R801 10K DNI
RR801 249K 1% DNI
R804 10K DNI
C793 4.7uF 6.3V
C811 0.01uF 25V DNI
27
IN
VDDCI_PWM1
27,28
IN
MVDD_VDDCI_DRON
R829 0R
28 VDDCI_DRON
R841 0R DNI
VCC
VCCD
VIN1
VIN2
VIN3
VIN4
SMOD_N
PWM
DISB#
BOOT
PHASE
VSW1
VSW2
VSW3
VSW4
VSW5
VSW6
VSW7
VSW8
VSW9
VSW10
VSW11
NC1
GL1
GL2
THWN
CGND
AGND
PGND1
PGND2
PGND3
PGND4
PGND5
NCP302045MNTWG
R799 1R
C791 0.22uF 25V
<GROUP>
R803 0R DNI
MC811 0.01uF 25V DNI
C794 4.7uF 6.3V
R805 10K DNI
R802 2.2R DNI
C792 1000pF 50V DNI
VDDCI_PH
L705 0.15uH
NS712 DNI
NS713 DNI
add 7343 SMD cap (copied from C438)
+VDDCI_MEM
C4847 470uF 2V DNI
C4848 470uF 2V DNI
C4849 470uF 2V DNI
C4850 470uF 2V DNI
+VDDCI_MEM
C783 22uF 4V
C784 22uF 4V
C785 22uF 4V
C786 22uF 4V
C787 22uF 4V
C788 22uF 4V
delete DIP cap X 2
VDDCI_ISENN1
OUT
27
VDDCI_ISENP1
OUT
27
VDDCI_THWN
OUT
28
+3.3V_BUS
R839 0R
R837 20K 1%
R838 210K 1%
R834 20K 1%
R835 100K 1%
VRHOT_NTC_H
Place close U702 and L701
VRHOT_NTC_L
U703
LMV331
R840 2K 1%
MVDD_VDDCI_REG_HOT#
OUT
4
C807 1uF 6.3V
R833 10.7K 1%
R836 5.1K 1%
C805 1000pF 50V
C806 1000pF 50V

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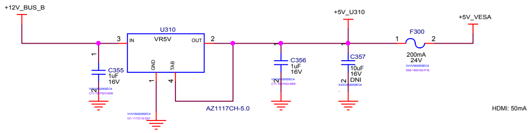
+1.8V FOR BOMACO

remove

+5V_VESA FOR HDMI


+12V_BUS_B
U310
VR5V
IN
OUT
GND
TAB
3
2
1
4
AZ1117CH-5.0
VVVV50205SEC4
I31-1117C19-D07
C355
1uF
16V
VVVV50205SEC4
C11-1057523-M09
C356
1uF
16V
VVVV50205SEC4
C11-1057523-M09
+5V_U310
C357
10uF
16V
DNI
XXXV50205SEC4
F300
200mA
24V
VVVV50205SEC4
D08-1400100-P16
+5V_VESA
HDMI: 50mA

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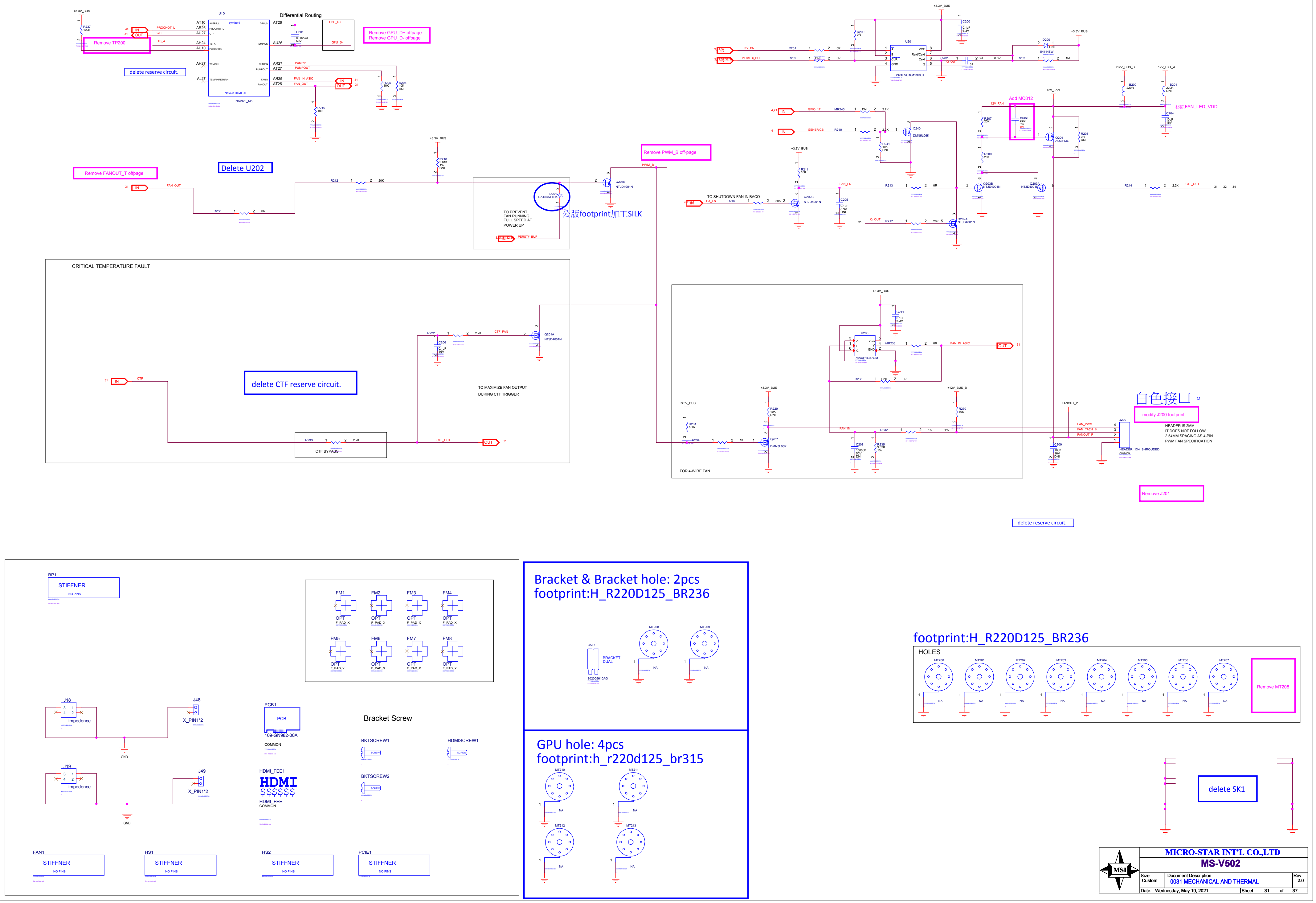
(27) MECH AND THERM MANAGEMENT


+3.3V_BUS
R237 100K
IN 34 PROCHOT_L
OUT 31 CTF
TS_A
Remove TP200
delete reserve circuit.
U1D symbol4
AT10 ALERT_L
AR26 PROCHOT_L
AU27 CTF
AH24 TS_A
AU10 PWRBRKB
AH27 TEMPIN
AJ27 TEMPINRETURN
DPLUS AT26
DMINUS AU26
PUMPIN AR27
PUMPOUT AT27
FANIN AR25
FANOUT AT25
Navi23 Rev0.90
NAVI23_M5
Differential Routing
C201 0.0022uF 50V
GPU_D+
GPU_D-
Remove GPU_D+ offpage
Remove GPU_D- offpage
PUMPIN
PUMPOUT
FAN_IN_ASIC IN 31
FAN_OUT OUT 31
R205 10K
R206 10K DNI
R215 10K
Remove FANOUT_T offpage
Delete U202
31 IN FAN_OUT
R258 0R
R212 20K
R210 2.61K 1% DNI
D201 BAT54KFILM
TO PREVENT FAN RUNNING FULL SPEED AT POWER UP
IN PERST#_BUF
公版footprint加工SILK
Q201B NTJD4001N
Remove PWM_B off-page
PWM_B
U201 SN74LVC1G123DCT
A B CLR GND VCC Rext/Cext Cext Q
PX_EN R201 0R
PERST#_BUF R202 DNI 0R
R200 0R
C200 0.1uF 6.3V
C202 10uF 6.3V
Q_OUT 31
R203 1M
D200 DNI 1N4148W
+12V_BUS_B
+12V_EXT_A
B200 220R
B201 220R DNI
移除FAN_LED_VDD
C204 10uF 16V
12V_FAN
Add MC812
MC812 2.2uF 16V DNI
R207 20K
R209 20K
Q204 AO3413L
R208 0R DNI
4,21 IN GPIO_17 MR240 DNI 2.2K
4 IN GENERICB R240 2.2K
R241 10K DNI
Q240 DMN5L06K
R211 10K
FAN_EN
C205 0.1uF 6.3V DNI
TO SHUTDOWN FAN IN BACO
IN PX_EN R216 20K
Q202B NTJD4001N
R213 0R
Q203B NTJD4001N
Q203A NTJD4001N
R214 2.2K CTF_OUT 31 32 34
31 Q_OUT R217 20K
Q202A NTJD4001N
CRITICAL TEMPERATURE FAULT
R222 2.2K CTF_FAN
C206 0.1uF 16V
Q201A NTJD4001N
31 IN CTF
delete CTF reserve circuit.
TO MAXIMIZE FAN OUTPUT DURING CTF TRIGGER
R233 2.2K
CTF BYPASS
CTF_OUT OUT 32
U200 74AUP1G57GM
C211 0.1uF 6.3V
MR236 0R FAN_IN_ASIC OUT 31
R236 DNI 0R
R231 5.1K
R234 1K
R229 10K DNI
Q207 DMN5L06K
FAN_IN
C208 1000pF 50V DNI
R235 3.83K 1%
R232 1K 1%
R230 10K
FOR 4-WIRE FAN
FANOUT_P
C209 10uF 16V DNI
FAN_PWM
FAN_TACH_B
FANOUT_P
J200 HEADER_1X4_SHROUDED COMMON
白色接口。
modify J200 footprint
HEADER IS 2MM
IT DOES NOT FOLLOW
2.54MM SPACING AS 4-PIN
PWM FAN SPECIFICATION
Remove J201
delete reserve circuit.
BP1 STIFFNER NO PINS
FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8 OPT F_PAD_X
J18 impedence
J48 X_PIN1*2
J19 impedence
J49 X_PIN1*2
GND
PCB1 PCB 109-GN982-00A COMMON
HDMI_FEE1 HDMI HDMI_FEE COMMON
Bracket Screw
BKTSCREW1 SCREW
BKTSCREW2 SCREW
HDMISCREW1 SCREW
FAN1 STIFFNER NO PINS
HS1 STIFFNER NO PINS
HS2 STIFFNER NO PINS
PCIE1 STIFFNER NO PINS
Bracket & Bracket hole: 2pcs
footprint:H_R220D125_BR236
BKT1 BRACKET DUAL 802005610AG
MT208 MT209 NA
GPU hole: 4pcs
footprint:h_r220d125_br315
MT210 MT211 MT212 MT213 NA
footprint:H_R220D125_BR236
HOLES
MT200 MT201 MT202 MT203 MT204 MT205 MT206 MT207 NA
Remove MT208
delete SK1

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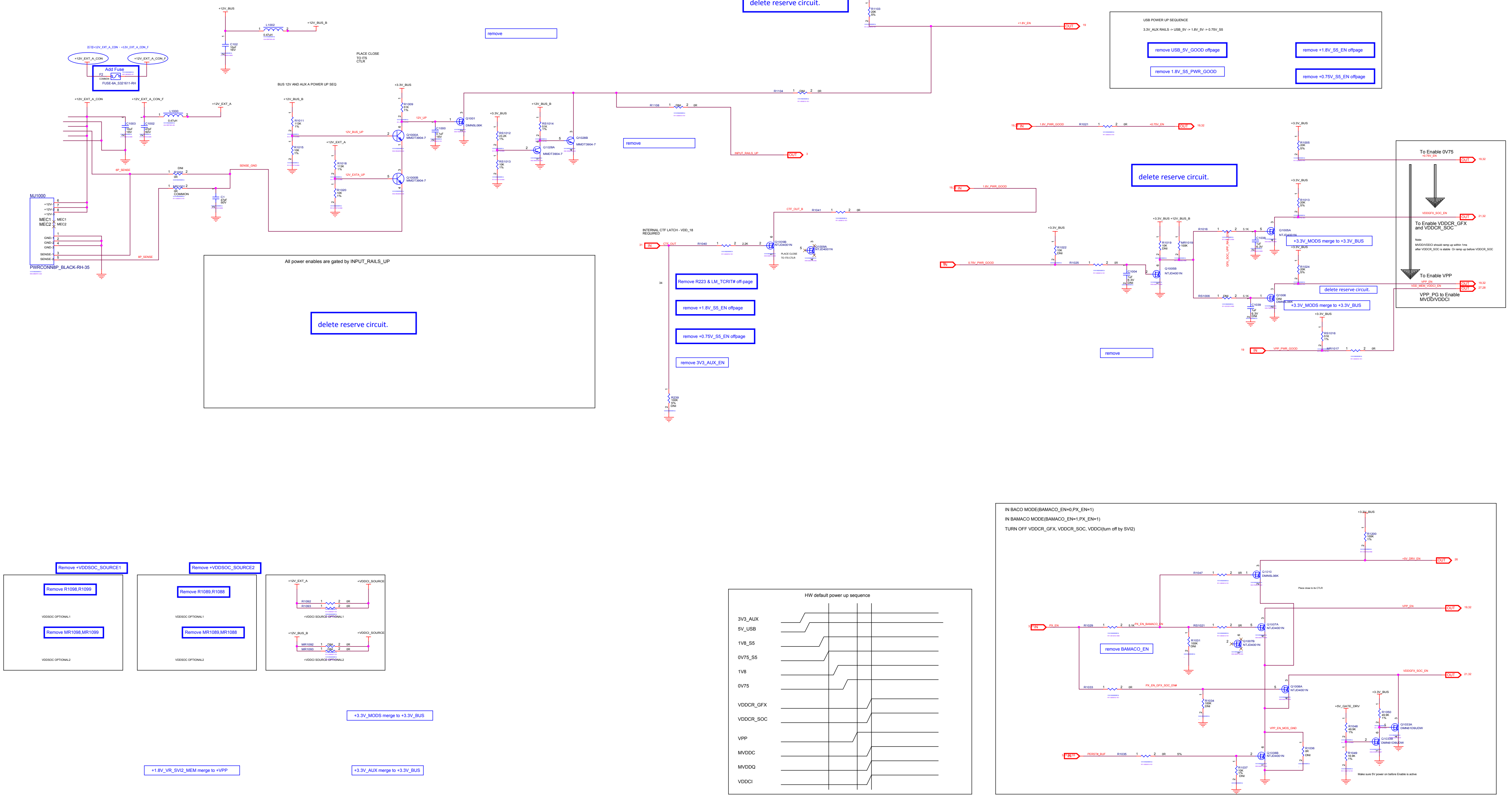
(27) POWER MANAGEMENT


+12V_BUS
L1002
0.47uH
+12V_BUS_B
C102
10uF
16V
新增+12V_EXT_A_CON、+12V_EXT_A_CON_F
+12V_EXT_A_CON
+12V_EXT_A_CON_F
F2
COMMON
FUSE-6A_S321611-RH
PLACE CLOSE
TO ITS
CTLR
BUS 12V AND AUX A POWER UP SEQ
+12V_EXT_A
L1000
0.47uH
C1003
10uF
16V
C1002
47pF
50V
6P_SENSE
R1001
DNI
0R
MR1001
0R
COMMON
SENSE_GND
C1
47pF
50V
MJ1000
+12V-1
+12V-2
+12V-3
MEC1
MEC2
GND-1
GND-2
GND-3
SENSE-1
SENSE-2
8P_SENSE
PWRCONN8P_BLACK-RH-35
R1011
113K
1%
R1015
10K
1%
12V_BUS_UP
R1018
113K
1%
R1020
10K
1%
12V_EXTA_UP
+3.3V_BUS
R1009
51K
1%
12V_UP
Q1000A
MMDT3904-7
Q1000B
MMDT3904-7
C1000
0.1uF
16V
Q1001
DMN5L06K
RS1012
23.2K
1%
RS1013
10K
1%
RS1014
51K
1%
Q1028A
MMDT3904-7
Q1028B
MMDT3904-7
R1108
DNI
0R
INPUT_RAILS_UP
OUT
R1104
DNI
0R
R1103
20K
5%
+1.8V_EN
OUT
USB POWER UP SEQUENCE
3.3V_AUX RAILS -> USB_5V -> 1.8V_5V -> 0.75V_S5
IN
1.8V_PWR_GOOD
R1021
0R
+0.75V_EN
CTF_OUT_B
R1041
0R
INTERNAL CTF LATCH - VDD_18
REQUIRED
CTF_OUT
R1040
2.2K
Q1009B
NTJD4001N
Q1009A
NTJD4001N
PLACE CLOSE
TO ITS CTLR
R239
100K
5%
DNI
0.75V_PWR_GOOD
R1022
10K
DNI
R1025
0R
C1004
1uF
6.3V
DNI
Q1005B
NTJD4001N
+3.3V_BUS +12V_BUS_B
R1019
10K
DNI
MR1019
100K
R1016
5.1K
GFX_SOC_VPP_RAIL_EN
C1038
1uF
6.3V
Q1005A
NTJD4001N
RS1006
DNI
5.1K
C1039
1uF
6.3V
DNI
Q1006
DNI
DMN5L06K
R1005
20K
5%
R1013
20K
5%
R1024
20K
5%
RS1016
51K
1%
VPP_PWR_GOOD
MR1017
0R
To Enable 0V75
+0.75V_EN
VDDGFX_SOC_EN
To Enable VDDCR_GFX
and VDDCR_SOC
Note:
MVDD/VDDCI should ramp up within 1ms
after VDDCR_SOC is stable Or ramp up before VDDCR_SOC
To Enable VPP
VPP_EN
VDD_MEM_VDDCI_EN
VPP_PG to Enable
MVDD/VDDCI
VDDSOC OPTIONAL1
VDDSOC OPTIONAL2
+12V_EXT_A
+VDDCI_SOURCE
R1092
R1093
0R
+VDDCI SOURCE OPTIONAL1
+12V_BUS_B
MR1092
MR1093
DNI
+VDDCI SOURCE OPTIONAL2
HW default power up sequence
3V3_AUX
5V_USB
1V8_S5
0V75_S5
1V8
0V75
VDDCR_GFX
VDDCR_SOC
VPP
MVDDC
MVDDQ
VDDCI
IN BACO MODE(BAMACO_EN=0,PX_EN=1)
IN BAMACO MODE(BAMACO_EN=1,PX_EN=1)
TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI(turn off by SVI2)
R1200
100K
1%
+5V_DRV_EN
R1047
0R
Q1010
DMN5L06K
Place close to its CTLR
PX_EN
R1029
5.1K
PX_EN_BAMACO_EN
RS1021
0R
Q1007A
NTJD4001N
Q1007B
NTJD4001N
R1031
100K
DNI
R1033
0R
PX_EN_GFX_SOC_EN#
R1034
100K
DNI
Q1008A
NTJD4001N
VPP_EN_MOS_GND
PERST#_BUF
R1035
0R
5%
R1037
10K
1%
DNI
Q1008B
NTJD4001N
R1036
0R
DNI
+5V_GATE_DRV
R1048
49.9K
1%
R1049
16.9K
1%
R1050
49.9K
1%
Q1033A
DMN61D9UDW
Q1033B
DMN61D9UDW
Make sure 5V power on before Enable is active

Add Fuse

remove

delete reserve circuit.

All power enables are gated by INPUT_RAILS_UP

delete reserve circuit.

remove

Remove R223 & LM_TCRIT# off-page

remove +1.8V_S5_EN offpage

remove +0.75V_S5_EN offpage

remove 3V3_AUX_EN

remove USB_5V_GOOD offpage

remove 1.8V_S5_PWR_GOOD

remove +1.8V_S5_EN offpage

remove +0.75V_S5_EN offpage

delete reserve circuit.

+3.3V_MODS merge to +3.3V_BUS

delete reserve circuit.

+3.3V_MODS merge to +3.3V_BUS

remove

remove BAMACO_EN

Remove +VDDSOC_SOURCE1

Remove R1098,R1099

Remove MR1098,MR1099

Remove +VDDSOC_SOURCE2

Remove R1089,R1088

Remove MR1089,MR1088

+3.3V_MODS merge to +3.3V_BUS

+1.8V_VR_SVI2_MEM merge to +VPP

+3.3V_AUX merge to +3.3V_BUS

MSI
MICRO-STAR INT'L CO.,LTD
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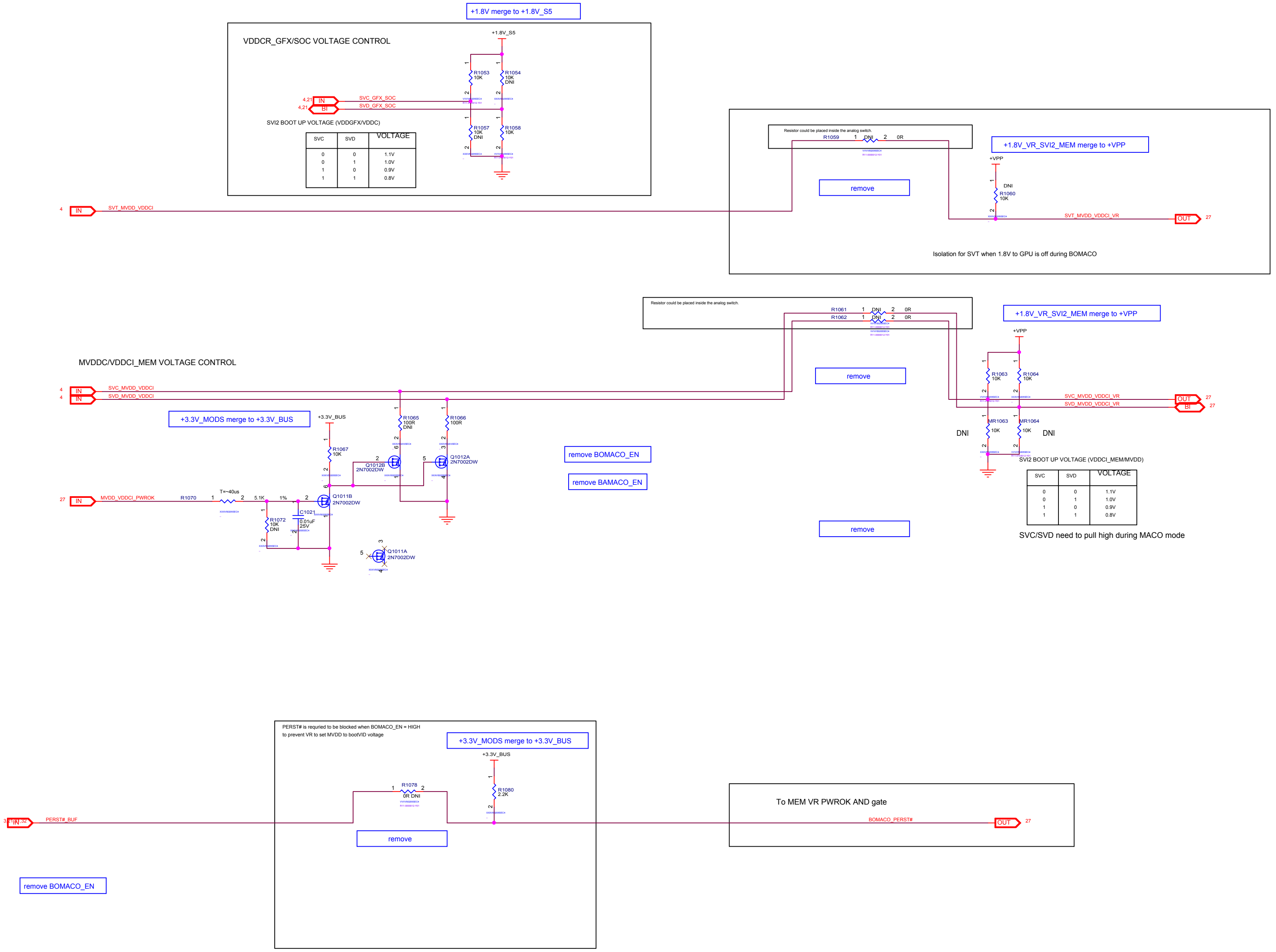
(28) SVI2


+1.8V merge to +1.8V_S5
VDDCR_GFX/SOC VOLTAGE CONTROL
+1.8V_S5
R1053
10K
R1054
10K
DNI
R1057
10K
DNI
R1058
10K
4,21
IN
SVC_GFX_SOC
4,21
BI
SVD_GFX_SOC
4
IN
SVT_MVDD_VDDCI
Resistor could be placed inside the analog switch.
R1059
DNI
0R
remove
+1.8V_VR_SVI2_MEM merge to +VPP
+VPP
DNI
R1060
10K
SVT_MVDD_VDDCI_VR
OUT
27
Resistor could be placed inside the analog switch.
R1061
DNI
0R
R1062
DNI
0R
remove
+1.8V_VR_SVI2_MEM merge to +VPP
+VPP
R1063
10K
R1064
10K
SVC_MVDD_VDDCI_VR
OUT
27
SVD_MVDD_VDDCI_VR
BI
27
MR1063
10K
DNI
MR1064
10K
DNI
remove
MVDDC/VDDCI_MEM VOLTAGE CONTROL
4
IN
SVC_MVDD_VDDCI
4
IN
SVD_MVDD_VDDCI
+3.3V_MODS merge to +3.3V_BUS
+3.3V_BUS
R1067
10K
R1065
100R
DNI
R1066
100R
Q1012B
2N7002DW
Q1012A
2N7002DW
remove BOMACO_EN
remove BAMACO_EN
27
IN
MVDD_VDDCI_PWROK
R1070
T=~40us
5.1K
1%
Q1011B
2N7002DW
R1072
10K
DNI
C1021
0.01uF
25V
Q1011A
2N7002DW
+3.3V_MODS merge to +3.3V_BUS
+3.3V_BUS
R1078
0R DNI
R1080
2.2K
remove
IN
PERST#_BUF
BOMACO_PERST#
OUT
27
remove BOMACO_EN

SVI2 BOOT UP VOLTAGE (VDDGFX/VDDC)

SVC	SVD	VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

Isolation for SVT when 1.8V to GPU is off during BOMACO

SVI2 BOOT UP VOLTAGE (VDDCI_MEM/MVDD)

SVC	SVD	VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

SVC/SVD need to pull high during MACO mode

PERST# is requried to be blocked when BOMACO_EN = HIGH
to prevent VR to set MVDD to bootVID voltage

To MEM VR PWROK AND gate

MICRO-STAR INT'L CO.,LTD
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Custom	0033 SVI2	2.0

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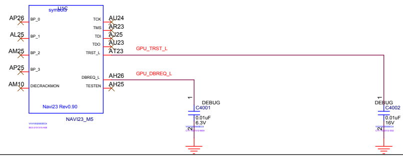
(29) DEBUG CIRCUIT

Delete JTAG

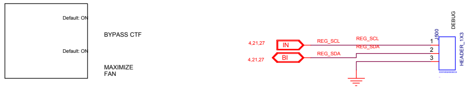
+1.8V merge to +1.8V_S5

JTAG


U1C
symbols
AP26
AL25
AM25
AP25
AM10
BP_0
BP_1
BP_2
BP_3
DIECRACKMON
TCK
TMS
TDI
TDO
TRST_L
DBREQ_L
TESTEN
AU24
AR23
AJ25
AU23
AT23
AH26
AH25
GPU_TRST_L
GPU_DBREQ_L
Navi23 Rev0.90
NAVI23_M5
DEBUG
C4001
0.01uF
6.3V
DEBUG
C4002
0.01uF
16V

SWITCHES

Remove


Default: ON
Default: ON
BYPASS CTF
MAXIMIZE FAN
4,21,27
IN
4,21,27
BI
REG_SCL
REG_SDA
REG_SCL
REG_SDA
1
2
3
J500
DEBUG
HEADER_1X3

POWERGOOD STATUS

MXM POWERGOOD GENERATION

SS LABELS

VDDGFX_VDDCR

MVDD_VDDCI

SS LABEL

PG

Vih=2.1v

SS LABELS

0.75

0.75_S5

2530004900G

Remove

S0 POWER GOOD

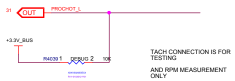
THERMAL SENSOR FOR GDDR6

THERMAL SENSOR FOR SOC

Remove

THERMAL SENSOR FOR GFX

THERMAL SENSOR FOR VDDCI


31
OUT
PROCHOT_L
+3.3V_BUS
R4039
1
DEBUG
2
10K

TACH CONNECTION IS FOR TESTING

AND RPM MEASUREMENT ONLY

Remove

LM96163 FOR BACKUP THERMAL CONTROL

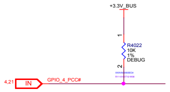
LED LIGHTS

LED RED "ON" INDICATES CTF FAULT

LED YELLOW "ON" INDICATES FANOFF (BACO) MODE

Remove

LED YELLOW "ON" INDICATES BAMACO STATE


+3.3V_BUS
1
R4022
10K
1%
DEBUG
2
4,21
IN
GPIO_4_PCC#

LED RED "ON" INDICATES PCC triggerred

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Remove PI Debug

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AMD

TITLE: NAVI23 DT XT GDDR6 x16 BOARD

DOCUMENT NUMBER: 105-D532xx-00

DATE: Tue Jul 07 03:31:54 2020

SHEET NUMBER: 36 OF 36

REV: 00B

REVISION HISTORY

ENGINEER: Yahyazadeh, Danial

NOTES: NOTE

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SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
00A	00A	05/18/2020	Initial schematic
00B	00B	06/30/2020	Change all ESD based on EMI's new requirement Add Q1033 related circuit for VDDGFX_SOC_EN control to resolve the potential risk on BACO exit(P32)
		07/06/2020	Change +3.3V_MODS, +5V_MODS, +5V_GATE_DRV circuit(P20,P21)

MSI

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Custom	0036 REVISION HISTORY	2.0

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Remove LED_CONTROLLER_IT8295