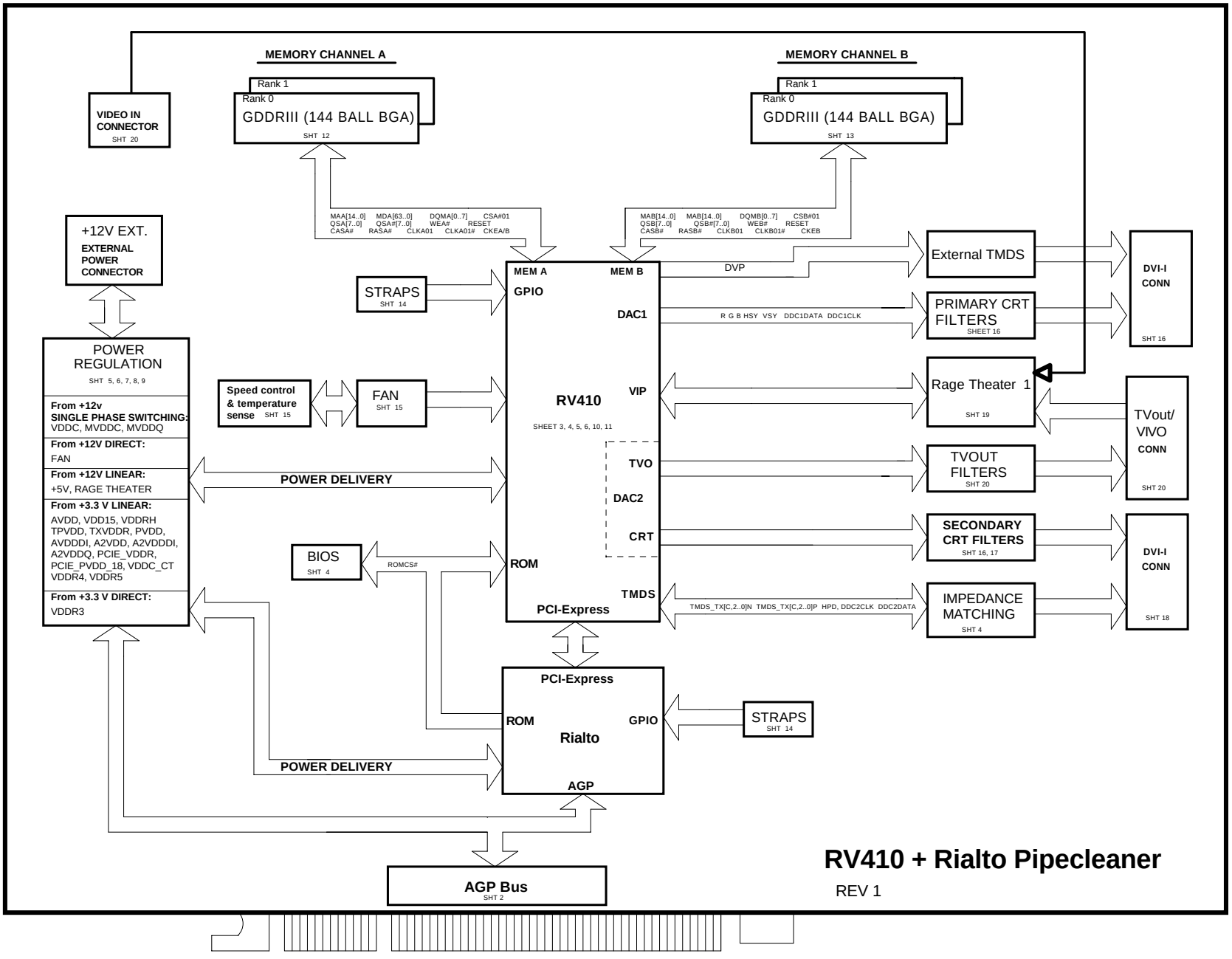
Title	Schematic No.	Date:
AGP RV410 DV VG VIVO 256MB DDR3	105-A41800-00	**Thursday, December 23, 2004**

REVISION HISTORY

Rev 3

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/08/04	Initial release, based on A379 RV410 Pipecleaner.
1	00B	08/10/04	Unify Chassis and Digital Gnd. Update ASIC memory VREF divider to 70%. Change R138, R149, R151, R159 to 3160100000 Update ASIC memory voltages from 1.9V to 2.1V, change R256 and R311 to 3240124100, change R253 and R310 to 3240200100 Added option for new Capacitors to input of +VDDC Regulator C1705 and alternate MC1705. Add option for different bulk capcitors on the ouptupt of +VDDC, +MVDDC, +MVDDQ regulators. These alternates are for Polymer Caps and Throughhole LOW ESR electrolytic caps. Add Option three resistor packs (RP207, RP208, RP210) to give option to short +MVDDC and +MVDDQ. Power bufget must be verified before implementing.
2	00C	25/10/04	Change +PCIE_VDDR Regulator REG7 to RT9194 with MTD3055.
3	00	5/12/04	Add B2 to share +B_VDDC with +PCIE_VDDR_12.



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1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

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LAYOUT NOTE: SOME OF THE CAPS BELOW MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

+12V_BUS — C12 10uF_20V

+5V_BUS — C5 47uF_6.3V

+3.3V_BUS — C10 47uF_6.3V

+VDDQ_BUS — C4 100uF_6.3V >= 6.3V

Use 47uF Tant. 16V 20% D size (P/N 4230047600), 800mR Max. ESR and Max. ripple 430mA @ 100kHz
or
100uF, Alum. 6.3V 20% 6.3mm dia (P/N 4261010700), 440mR Max. ESR and Max. ripple 230mA @ 100kHz
or
47uF, Alum. 6.3V 20% 5mm dia (P/N 4262047600), 760mR Max. ESR and Max. ripple 150mA @ 100kHz

Place C2 on left side of AGP connector

4X/8X AGP BUS

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

MAGP1

A1	12V	B1	OVRCNT#
A2	TYPEDET#	B2	5.0V
A3	GC_DET#/RESERVED	B3	5.0V#B3
A4	USB-	B4	USB+
A5	GND	B5	GND#B5
A6	INTA#	B6	INTB#
A7	RST#	B7	CLK
A8	GNT#	B8	REQ#
A9	VCC3.3	B9	VCC3.3#B9
A10	ST1	B10	ST0
A11	MB_DET#/RESERVED	B11	ST2
A12	DBI_HI/PIPE#	B12	RBF#
A13	GND#A13	B13	GND#B13
A14	WBF#	B14	DBI_LO/RESERVED
A15	SBA1	B15	SBA0
A16	VCC3.3#A16	B16	VCC3.3#B16
A17	SBA3	B17	SBA2
A18	SB_STB#	B18	SB_STB
A19	GND#A19	B19	GND#B19
A20	SBA5	B20	SBA4
A21	SBA7	B21	SBA6
A22	RESERVED	B22	RESERVED#B22
A23	GND#A23	B23	GND#B23
A24	RESERVED#A24	B24	3.3VAUX
A25	VCC3.3#A25	B25	VCC3.3#B25
A26	AD30	B26	AD31
A27	AD28	B27	AD29
A28	VCC3.3#A28	B28	VCC3.3#B28
A29	AD26	B29	AD27
A30	AD24	B30	AD25
A31	GND#A31	B31	GND#B31
A32	AD_STB1#	B32	AD_STB1
A33	C/BE3#	B33	AD23
A34	VDDQ1.5	B34	VDDQ1.5#B34
A35	AD22	B35	AD21
A36	AD20	B36	AD19
A37	GND#A37	B37	GND#B37
A38	AD18	B38	AD17
A39	AD16	B39	C/BE2#
A40	VDDQ1.5#A40	B40	VDDQ1.5#B40
A41	FRAME#	B41	IRDY#
A42	KEY	B42	KEY#B42
A43	KEY#A43	B43	KEY#B43
A44	KEY#A44	B44	KEY#B44
A45	KEY#A45	B45	KEY#B45
A46	TRDY#	B46	DEVSEL#
A47	STOP#	B47	VDDQ1.5#B47
A48	PME#	B48	PERR#
A49	GND#A49	B49	GND#B49
A50	PAR	B50	SERR#
A51	AD15	B51	C/BE1#
A52	VDDQ1.5#A52	B52	VDDQ1.5#B52
A53	AD13	B53	AD14
A54	AD11	B54	AD12
A55	GND#A55	B55	GND#B55
A56	AD9	B56	AD10
A57	C/BE0#	B57	AD8
A58	VDDQ1.5#A58	B58	VDDQ1.5#B58
A59	AD_STB0#	B59	AD_STB0
A60	AD6	B60	AD7
A61	GND#A61	B61	GND#B61
A62	AD4	B62	AD5
A63	AD2	B63	AD3
A64	VDDQ1.5#A64	B64	VDDQ1.5#B64
A65	AD0	B65	AD1
A66	VREFGC	B66	VREFCG

1.5V_AGP_BUS

AGP_C/BE#[3..0] — AGP_C/BE#[3..0] (21)
AGP_AD[31..0] — AGP_AD[31..0] (21)
AGP_SBA[7..0] — AGP_SBA[7..0] (21)
AGP_ST[2..0] — AGP_ST[2..0] (21)

AGP_TYPEDET#
AGP_GC_8X_DET#
(21) AGP_INTR#
AGP_CON_RESET#
(21) AGP_GNT#
(21) AGP_MB_8X_DET# — R7 0R 402
(21) AGP_DBI_HI — R9 0R 402
(21) AGP_WBF#
(21) AGP_SBSTB# — R1 0R 402
(21) AGP_ADSTB1# — R5 0R 402
(21) AGP_FRAME#
(21) AGP_TRDY#
(21) AGP_STOP#
(21) AGP_PAR
(21) AGP_ADSTB0# — R12 0R 402
AGP_VREFGC

AGP_MB_8X_DET#_R
AGP_DBI_HI_R
AGP_ST1
AGP_SBA1
AGP_SBA3
AGP_SBA5
AGP_SBA7
AGP_AD30
AGP_AD28
AGP_AD26
AGP_AD24
AGP_C/BE#3
AGP_AD22
AGP_AD20
AGP_AD18
AGP_AD16
AGP_PAR_R
AGP_AD15
AGP_AD13
AGP_AD11
AGP_AD9
AGP_C/BE#0
AGP_AD6
AGP_AD4
AGP_AD2
AGP_AD0

AGP_ST0
AGP_ST2
AGP_SBA0
AGP_SBA2
AGP_SBA4
AGP_SBA6
AGP_AD31
AGP_AD29
AGP_AD27
AGP_AD25
AGP_AD23
AGP_AD21
AGP_AD19
AGP_AD17
AGP_C/BE#2
AGP_C/BE#1
AGP_AD14
AGP_AD12
AGP_AD10
AGP_AD8
AGP_AD7
AGP_AD5
AGP_AD3
AGP_AD1

AGP_AGPCLK (21) — AGP_REQ# (21)
AGP_RBF# (21) — AGP_DBI_LO (21)
AGP_SBSTB (21)
AGP_ADSTB1 (21)
AGP_IRDY# (21)
AGP_DEVSEL# (21)
AGP_ADSTB0 (21)
AGP_AGPREF

AGP_DBI_LO_R — R8 0R 402
AGP_SBSTB_R — R2 0R 402
AGP_ADSTB1_R — R10 0R 402
AGP_ADSTB0_R — R13 0R 402

+5V_BUS — 74ACT08MTC U2B
AGP_CON_RESET# — R3 100R — AGP_RESET# (16,18,21)
R4 180R 402

Spare gate

+5V_BUS — U2A 74ACT08MTC — C1 100nF

Caps for EMI - install close to AGP connector

+12V_BUS — C22 100nF 402
+5V_BUS — C25 100nF 402
+3.3V_BUS — C24 100nF 402

AGP_TYPEDET# — R19 5.1R
+12V, TYPEDET# short protection for OEM (5.1R)

AGP_GC_8X_DET# — R63 0R 402

UNIVERSAL VREFGC CIRCUIT (4X, 8X)

(21) AGP_MB_8X_DET# — AGP_MB_8X_DET# — R17 47K 402 — Q20 BSN20 — R6 20K 402 — TEST

+VDDQ_BUS — Q1 2N7002E — R20 324R 402 — AGP_VREFGC
R21 147R
R24 100R 402
C6 10nF 402
Close to ASIC

+5V_BUS — C3 100nF 402 — U4 TC7SZ08FU — R23 1K 402

May be placed far from connector -- place C3 FAR from connector, on left side!!

UNIVERSAL VREFCG CIRCUIT (4X, 8X)

AGP_AGPREF
+VDDQ_BUS
TEST — Q77 2N7002E — R72 147R
R75 324R 402
DNI
R73 0R 402
AGP_AGPREFCG — AGP_AGPREFCG (21)
R74 100R 402
C11 10nF 402
Close to ASIC

ATI Technologies Inc.
1 Commerce Valley Drive East
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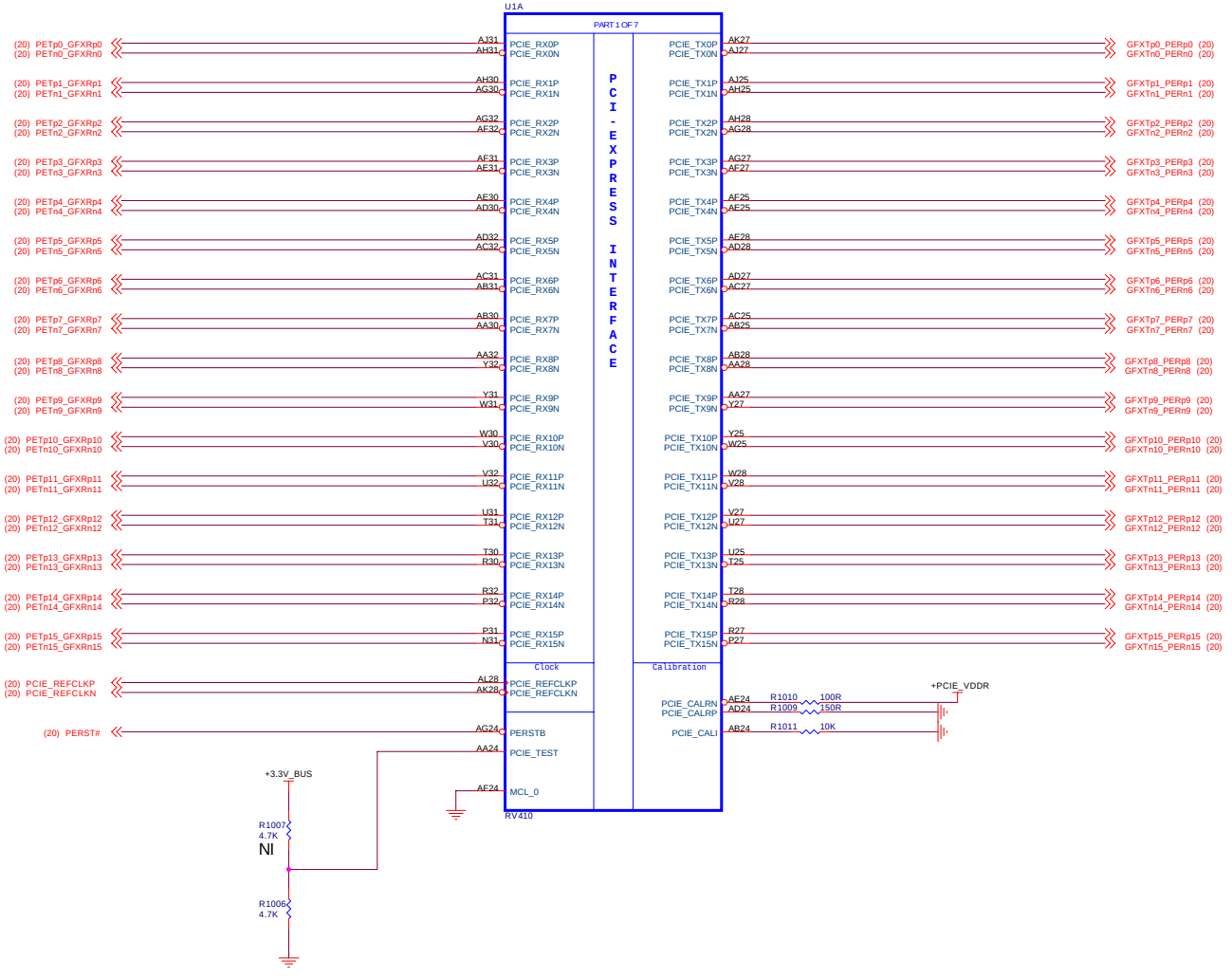
NOTE: some of the PCIE testpoints will
be available trought via on traces.



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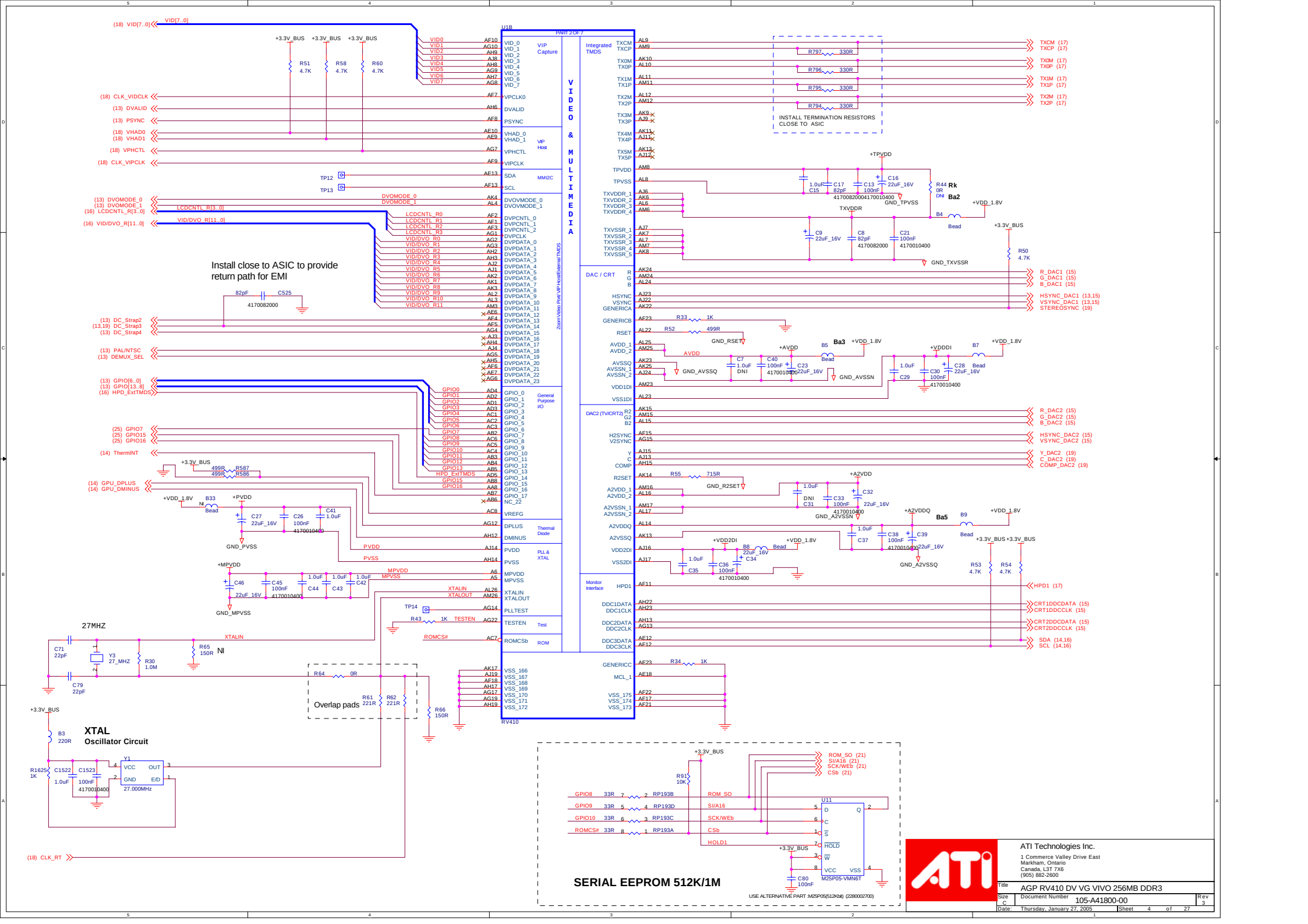
U1B
PART 2 OF 7
VIDEO & MULTIMEDIA
VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
VID_7
VIP Capture
VPCLK0
DVALID
PSYNC
VHAD_0
VHAD_1
VIP Host
VPHCTL
VIPCLK
SDA
SCL
MMI2C
DVOVMODE_0
DVOVMODE_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
Zoom/Video Port/ VIP Host/External TMDS
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_15
GPIO_16
GPIO_17
NC_22
General Purpose I/O
VREFG
DPLUS
DMINUS
Thermal Diode
PVDD
PVSS
PLL & XTAL
MPVDD
MPVSS
XTALIN
XTALOUT
PLLTEST
TESTEN
Test
ROMCSb
ROM
VSS_166
VSS_167
VSS_168
VSS_169
VSS_170
VSS_171
VSS_172
RV410
Integrated TMDS
TXCM
TXCP
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TX3M
TX3P
TX4M
TX4P
TX5M
TX5P
INSTALL TERMINATION RESISTORS CLOSE TO ASIC
TPVDD
TPVSS
TXVDDR_1
TXVDDR_2
TXVDDR_3
TXVDDR_4
TXVSSR_1
TXVSSR_2
TXVSSR_3
TXVSSR_4
TXVSSR_5
DAC / CRT
R
G
B
HSYNC
VSYNC
GENERICA
GENERICB
RSET
AVDD_1
AVDD_2
AVSSQ
AVSSN_1
AVSSN_2
VDD1DI
VSS1DI
DAC2 (TV/CRT2)
R2
G2
B2
H2SYNC
V2SYNC
Y
C
COMP
R2SET
A2VDD_1
A2VDD_2
A2VSSN_1
A2VSSN_2
A2VDDQ
A2VSSQ
VDD2DI
VSS2DI
Monitor Interface
HPD1
DDC1DATA
DDC1CLK
DDC2DATA
DDC2CLK
DDC3DATA
DDC3CLK
GENERICC
MCL_1
VSS_175
VSS_174
VSS_173
+TPVDD
GND_TPVSS
GND_TXVSSR
+VDD_1.8V
+3.3V_BUS
GND_RSET
+AVDD
GND_AVSSQ
GND_AVSSN
+VDDI
GND_R2SET
+A2VDD
GND_A2VSSN
+A2VDDQ
GND_A2VSSQ
+VDD2DI
GND_PVSS
GND_MPVSS
Install close to ASIC to provide return path for EMI
27MHZ
XTAL
Oscillator Circuit
Overlap pads
SERIAL EEPROM 512K/1M
USE ALTERNATIVE PART :M25P05(512Kbit) (2280002700)
M25P05-VMN6T
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600
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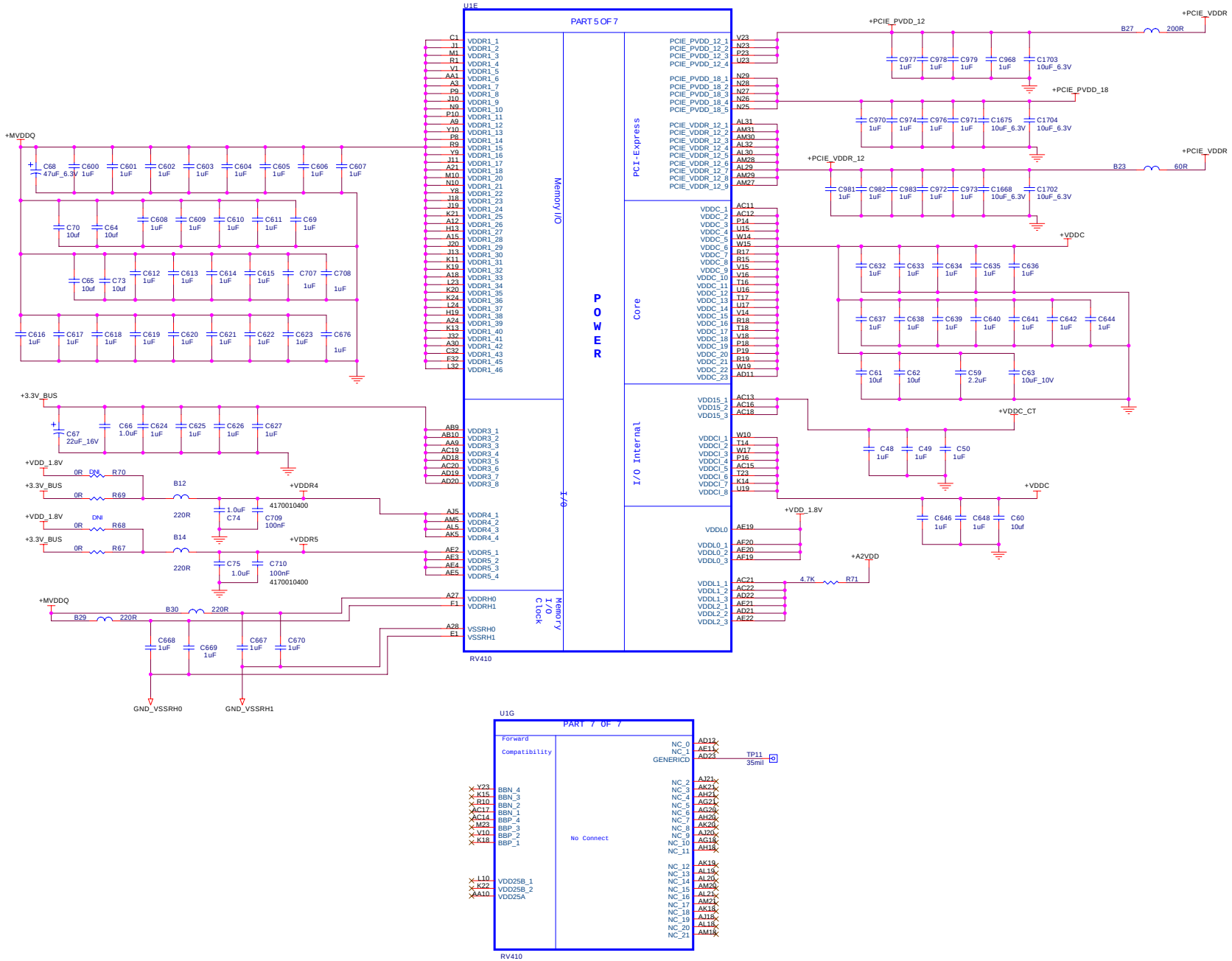

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1 Commerce Valley Drive East
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GND_AVSSN GND_MPVSS GND_PVSS GND_TPVSS GND_TXVSSR GND_A2VSSN GND_A2VSSQ GND_AVSSQ GND_R2SET GND_RSET GND_VSSRH0 GND_VSSRH1 GND_RT GND_VIN GND_TVVSSN

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

U1F

Part 6 of 7

PCI-Express GND

AH27	PCIE_VSS_1		VSS_45	AD16	
AC23	PCIE_VSS_2		VSS_44	AA6	
AL27	PCIE_VSS_3		VSS_43	P7	
R23	PCIE_VSS_4		VSS_42	P5	
P25	PCIE_VSS_5		VSS_41	M3	
R25	PCIE_VSS_6		VSS_40	M9	
T26	PCIE_VSS_7		VSS_39	L7	
U26	PCIE_VSS_8		VSS_38	M7	
W26	PCIE_VSS_9		VSS_47	AD17	
Y26	PCIE_VSS_10		VSS_48	AH11	
AB26	PCIE_VSS_11		VSS_49	A8	
AC26	PCIE_VSS_12		VSS_50	U7	
AD25	PCIE_VSS_13		VSS_51	C10	
AE26	PCIE_VSS_14		VSS_52	E9	
AF26	PCIE_VSS_15		VSS_53	F3	
AD26	PCIE_VSS_16		VSS_54	J9	
AC25	PCIE_VSS_17		VSS_55	N7	
AH26	PCIE_VSS_18		VSS_56	N3	
AC28	PCIE_VSS_19		VSS_57	Y5	
Y28	PCIE_VSS_20		VSS_58	AM13	
U28	PCIE_VSS_21		VSS_59	AC10	
P28	PCIE_VSS_22		VSS_60	Y6	
AH29	PCIE_VSS_23		VSS_61	U6	
AF28	PCIE_VSS_24		VSS_62	E5	
V29	PCIE_VSS_25		VSS_63	AL13	
AC29	PCIE_VSS_26		VSS_64	A11	
W27	PCIE_VSS_27		VSS_65	U8	
AB27	PCIE_VSS_28		VSS_66	U9	
V26	PCIE_VSS_29		VSS_67	U10	
AJ26	PCIE_VSS_30		VSS_68	R6	
AJ32	PCIE_VSS_31		VSS_69	AD6	
AK29	PCIE_VSS_32		VSS_70	V6	
P26	PCIE_VSS_33		VSS_71	AD14	
P29	PCIE_VSS_34		VSS_72	AD13	
R29	PCIE_VSS_35		VSS_73	D11	
T29	PCIE_VSS_36		VSS_74	J12	
U29	PCIE_VSS_37		VSS_75	K12	
W29	PCIE_VSS_38		VSS_77	A13	
Y29	PCIE_VSS_39		VSS_78	F13	
AA29	PCIE_VSS_40		VSS_79	E13	
AB29	PCIE_VSS_41		VSS_80	F15	
AD29	PCIE_VSS_42		VSS_81	K16	
AE29	PCIE_VSS_43		VSS_82	J21	
AF29	PCIE_VSS_44		VSS_83	H16	
AG29	PCIE_VSS_45		VSS_84	T15	
AJ29	PCIE_VSS_46		VSS_85	V17	
AK26	PCIE_VSS_47		VSS_86	C15	
AK30	PCIE_VSS_48		VSS_87	C4	
AG26	PCIE_VSS_49		VSS_88	U14	
N30	PCIE_VSS_50		VSS_89	P15	
R31	PCIE_VSS_51		VSS_90	A16	
AF30	PCIE_VSS_52		VSS_91	E16	
AC30	PCIE_VSS_53		VSS_92	G13	
V31	PCIE_VSS_54		VSS_93	G16	
P30	PCIE_VSS_55		VSS_94	P17	
AA31	PCIE_VSS_56		VSS_95	R16	
U30	PCIE_VSS_57		VSS_97	R14	
AD31	PCIE_VSS_58		VSS_98	W16	
AK32	PCIE_VSS_59		VSS_99	C18	
AJ28	PCIE_VSS_60		VSS_100	F16	
Y30	PCIE_VSS_61		VSS_101	W18	
AJ30	PCIE_VSS_62		VSS_102	U18	
AK31	PCIE_VSS_63		VSS_103	AE16	
AA23	PCIE_VSS_64		VSS_104	AE17	
AG31	PCIE_VSS_65		VSS_105	A19	
N24	PCIE_VSS_66		VSS_106	H32	
W23	PCIE_VSS_67		VSS_107	E19	
AB23	PCIE_VSS_69		VSS_108	G19	
P24	PCIE_VSS_70		VSS_109	N8	
R24	PCIE_VSS_71		VSS_110	Y7	
T24	PCIE_VSS_72		VSS_112	T19	
U24	PCIE_VSS_73		VSS_113	V19	
V24	PCIE_VSS_74		VSS_114	G21	
W24	PCIE_VSS_75		VSS_115	C21	
Y24	PCIE_VSS_76		VSS_116	F21	
AC24	PCIE_VSS_77		VSS_117	AE14	
AH24	PCIE_VSS_78		VSS_118	AK16	
V25	PCIE_VSS_79		VSS_119	U5	
AA25	PCIE_VSS_80		VSS_120	F22	
R26	PCIE_VSS_81		VSS_121	F18	
AA26	PCIE_VSS_82		VSS_122	K30	
T27	PCIE_VSS_83		VSS_124	C24	
AE27	PCIE_VSS_84		VSS_125	F24	
			VSS_126	M24	
B1	VSS_1		VSS_127	A25	
H1	VSS_2		VSS_128	D30	
L1	VSS_3		VSS_129	E25	
P1	VSS_4		VSS_130	G25	
U1	VSS_5		VSS_131	G20	
Y1	VSS_6		VSS_132	G22	
AD7	VSS_7		VSS_133	F27	
AE8	VSS_8		VSS_134	E28	
AL1	VSS_9		VSS_135	H21	
A2	VSS_10		VSS_136	C27	
AM2	VSS_11		VSS_137	E32	
AD10	VSS_12		VSS_138	H28	
E8	VSS_13		VSS_139	J30	
H5	VSS_14		VSS_140	K17	
K10	VSS_15		VSS_141	K27	
M8	VSS_16		VSS_142	M32	
T10	VSS_17		VSS_143	A22	
E12	VSS_18		VSS_144	C20	
AC9	VSS_19		VSS_145	E19	
AF14	VSS_20		VSS_146	H20	
AD8	VSS_21		VSS_147	J24	
C5	VSS_22		VSS_148	M28	
F10	VSS_23		VSS_149	J28	
J3	VSS_24		VSS_150	J16	
L6	VSS_25		VSS_151	F30	
M6	VSS_26		VSS_152	K23	
P6	VSS_27		VSS_153	L29	
AA4	VSS_28		VSS_154	A31	
AG11	VSS_29		VSS_155	B32	
V3	VSS_30		VSS_156	E30	
AG16	VSS_31		VSS_157	AE15	
R3	VSS_32		VSS_158	AG23	
C6	VSS_33		VSS_159	AD9	
C9	VSS_34		VSS_160	AF16	
F6	VSS_35		VSS_161	AH10	
H7	VSS_36		VSS_163	AJ10	
J6	VSS_37		VSS_164	AD15	
			VSS_165	AH16	

CORE GND

RV410

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title: AGP RV410 DV VG VIVO 256MB DDR3

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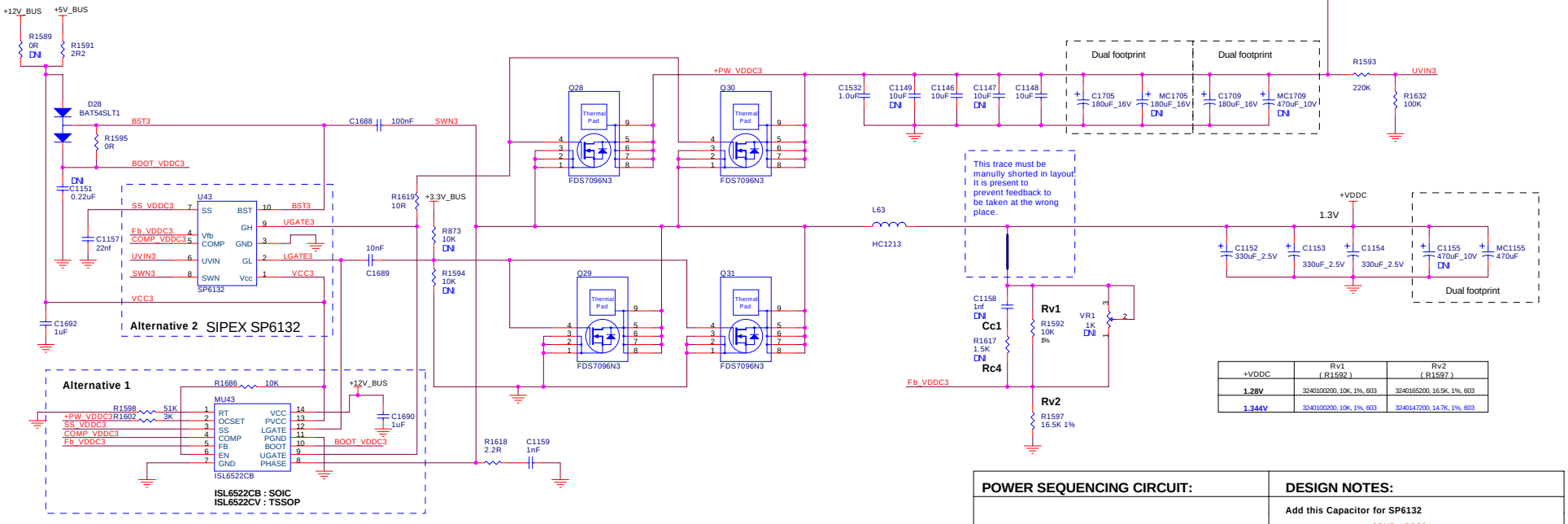
CORE REGULATOR VDDC



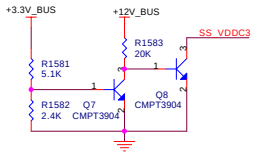
+VDDC	Rv1 (R1592)	Rv2 (R1597)
1.28V	3240100200, 10K, 1%, 603	3240165200, 16.5K, 1%, 603
1.344V	3240100200, 10K, 1%, 603	3240147200, 14.7K, 1%, 603

TP1
TP2
I_VDDC_LOOP

Current loop to measure VDDC output current.

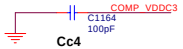
Lower MOSFET should be surrounded by a lot of copper for heat dissipation

POWER SEQUENCING CIRCUIT:

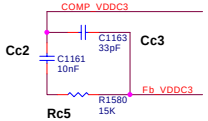


DESIGN NOTES:

Add this Capacitor for SP6132



Compensation Circuit



FOR ALTERNATE #1

Remove R374, R375, R371, C168 and U32

Install R370, R112, R954, R305-R308, C160 C159 and MU32

FOR ALTERNATE #2

Change C157 for 10 uF and C121 for 1 uF
Replace C764 by 0 Ohm resistor
Replace R314 with a bead
Remove R954, R370, R305-R308, C159, R112, C160 and MU32
Install R374, R375, R371, C168 and U32

Compensation circuit

Rc1 = 10K, Rc2 = 8.06K
R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF

<Variant Name>
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1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
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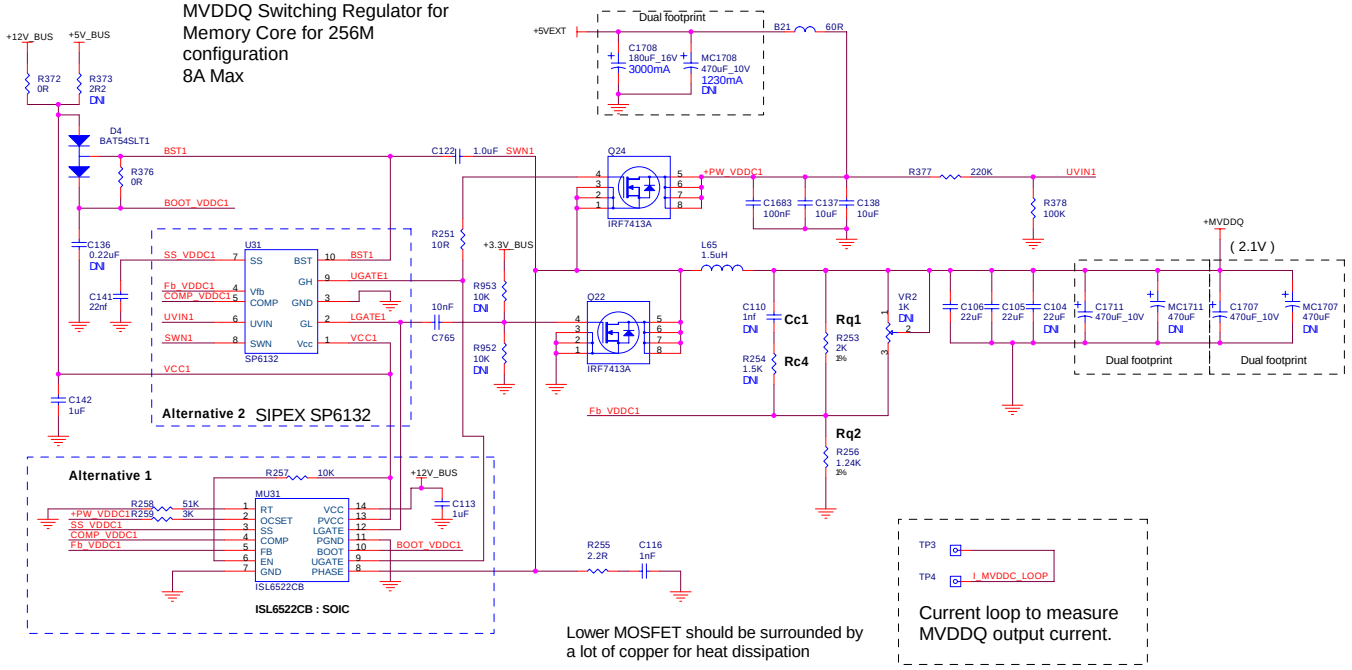
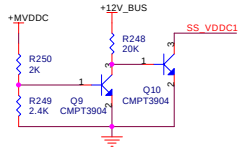
MVDDQ Switching Regulator for Memory Core for 256M configuration
8A Max



Lower MOSFET should be surrounded by a lot of copper for heat dissipation

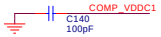
Current loop to measure MVDDQ output current.

POWER SEQUENCING CIRCUIT:

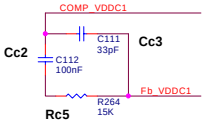


DESIGN NOTES:

Add this Capacitor for ALTERNATE #2



Compensation Circuit



FOR ALTERNATE #1

Install R372, D4, R376, C113, R257, R258, R259, MU31, R255 and C116

Remove R373, R377, R378, C122, C140 and U31

FOR ALTERNATE #2

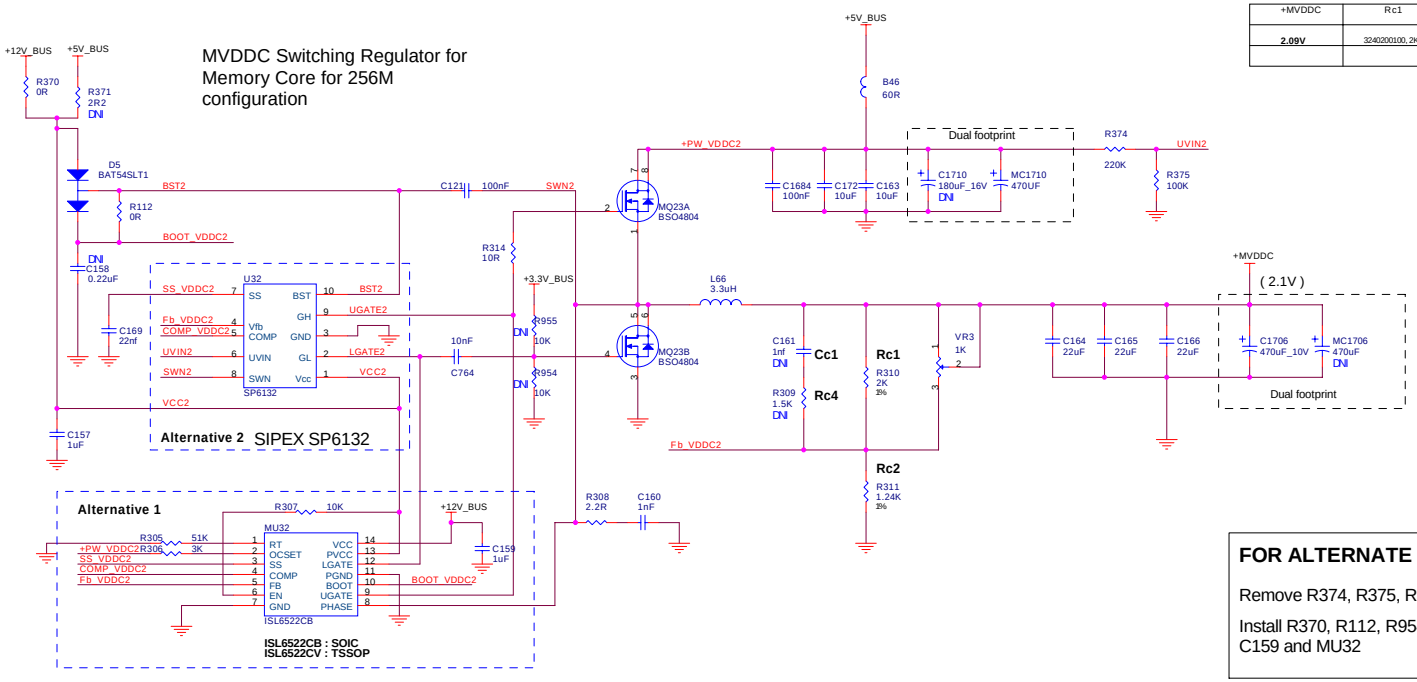
Change C142 for 10uF
Install R377, R378, R373, C122, C140 and U31
Remove R255, C116, R372, R376, D4, MU31, R257, R258, R259 and C113

Compensation circuit

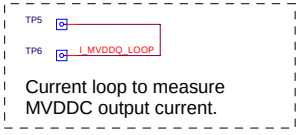
Rc1 = 10K, Rc2 = 8.06K
R264 = 41.2K, C111 = 27 pF

+MVDDQ	Rq1	Rq2
2.09V	3240200100, 2K, 1%	3240124100, 1.24K, 1%

MVDDC Switching Regulator for Memory Core for 256M configuration



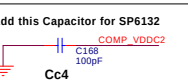
+MVDDC	Rc1	Rc2
2.09V	3240200100, 2K, 1%	3240124100, 1.24K, 1%



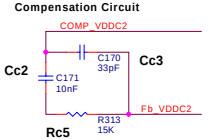
Current loop to measure MVDDC output current.

DESIGN NOTES:

Add this Capacitor for SP6132



Compensation Circuit



FOR ALTERNATE #1

Remove R374, R375, R371, C168 and U32

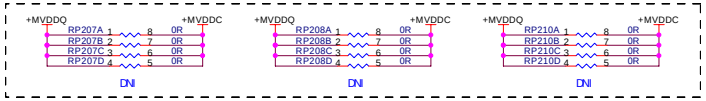
Install R370, R112, R954, R305-R308, C160 C159 and MU32

FOR ALTERNATE #2

Change C157 for 10 uF and C121 for 1 uF
Replace C764 by 0 Ohm resistor
Replace R314 with a bead
Remove R954, R370, R305-R308, C159, R112, C160 and MU32
Install R374, R375, R371, C168 and U32

Compensation circuit

Rc1 = 10K, Rc2 = 8.06K
R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF



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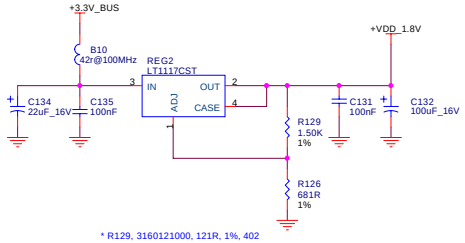
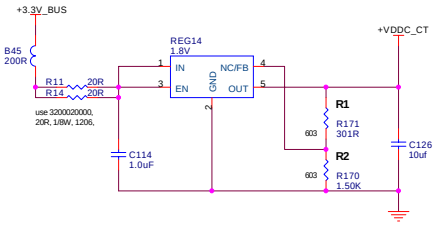
+1.8V Regulator



* R129, 3160121000, 121R, 1%, 402
R126, 316053R600, 53.6R, 1%, 402

VDDC_CT

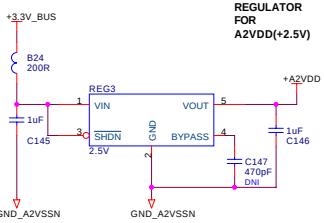
+1.5V Regulator for VDDC_CT (VDD15)
Vin=+3.3V
Vout=+1.5V(100mA)



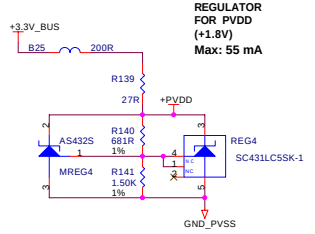
Use SP6201EM5-ADJ, 200mA, SOT23-5, DO<500mV (2480041200) $0.11
Alt. TI TPS76301, ADJ, 150mA, SOT23, DO<300mV (2480040800)
Alt. SP6201EM5-1.5, 200mA, SOT23-5, DO<500mV (2480041300) $0.11
Alt. AP131, 1.5V, 300mA, SOT23-5L, DO<400mV,

	SP6201EM5-ADJ Vo=1.25 (1+R1/R2)	TPS76301, ADJ Vo=1.186 (1+R1/R2)
R1	3240301000, 301R, 1%	3240402000, 402R, 1%
R2	3240150100, 1.50K, 1%	3240150100, 1.50K, 1%

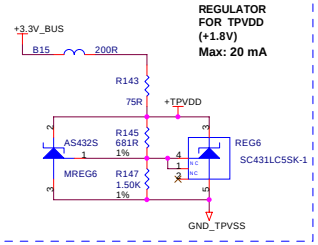
REGULATOR FOR A2VDD(+2.5V)



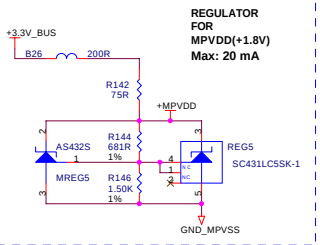
REGULATOR FOR PVDD (+1.8V) Max: 55 mA



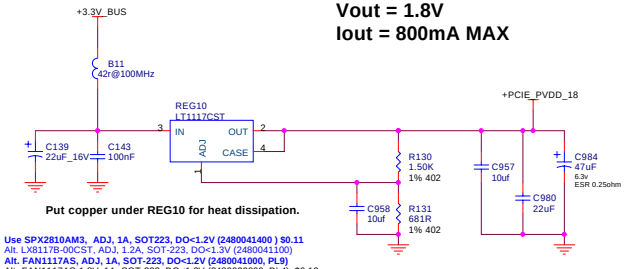
REGULATOR FOR TPVDD (+1.8V) Max: 20 mA



REGULATOR FOR MPVDD(+1.8V) Max: 20 mA



Regulator for PCIE_PVDD_18
Vout = 1.8V
Iout = 800mA MAX

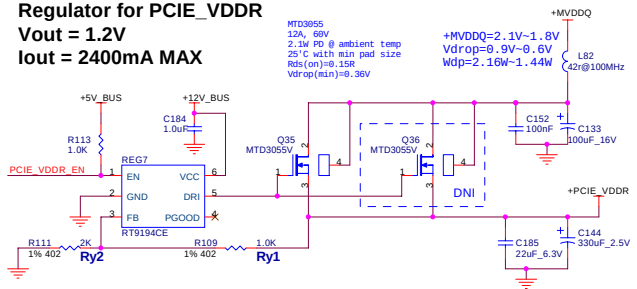


Put copper under REG10 for heat dissipation.

Use SPX2810AM3, ADJ, 1A, SOT223, DO<1.2V (2480041400) $0.11
Alt. LX8117B-00CST, ADJ, 1.2A, SOT-223, DO<1.3V (2480041100)
Alt. FAN1117AS, ADJ, 1A, SOT-223, DO<1.2V (2480041000, PL9)
Alt. FAN1117AS-1.8V, 1A, SOT-223, DO<1.2V (2480020000, PL4), $0.13
Alt. LX8117A-00CST, ADJ, 1A, SOT-223, DO<1.3V (2480002100, PL1), $0.25
Alt. AP1117, ADJ, 1A, SOT-223, DO<1.4V, Use +5V_BUS input Only, $0.10

* R130, 3160121000, 121R, 1%, 402
R131, 316053R600, 53.6R, 1%, 402

Regulator for PCIE_VDDR
Vout = 1.2V
Iout = 2400mA MAX

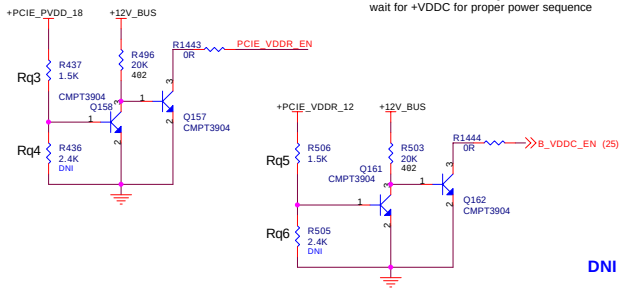


Note:
Place 1sq. In Copper Area under Q35, Q36 for heat dissipation.

+PCIE_VDDR	Ry1	Ry2
1.2V	3160100100, 1.0K, 1%	3160200100, 2.0K, 1%

PCIE PWR SEQUENCE

Circuit to hold PCI-E voltage low
wait for +VDDC for proper power sequence



DNI

PCIE Power

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1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
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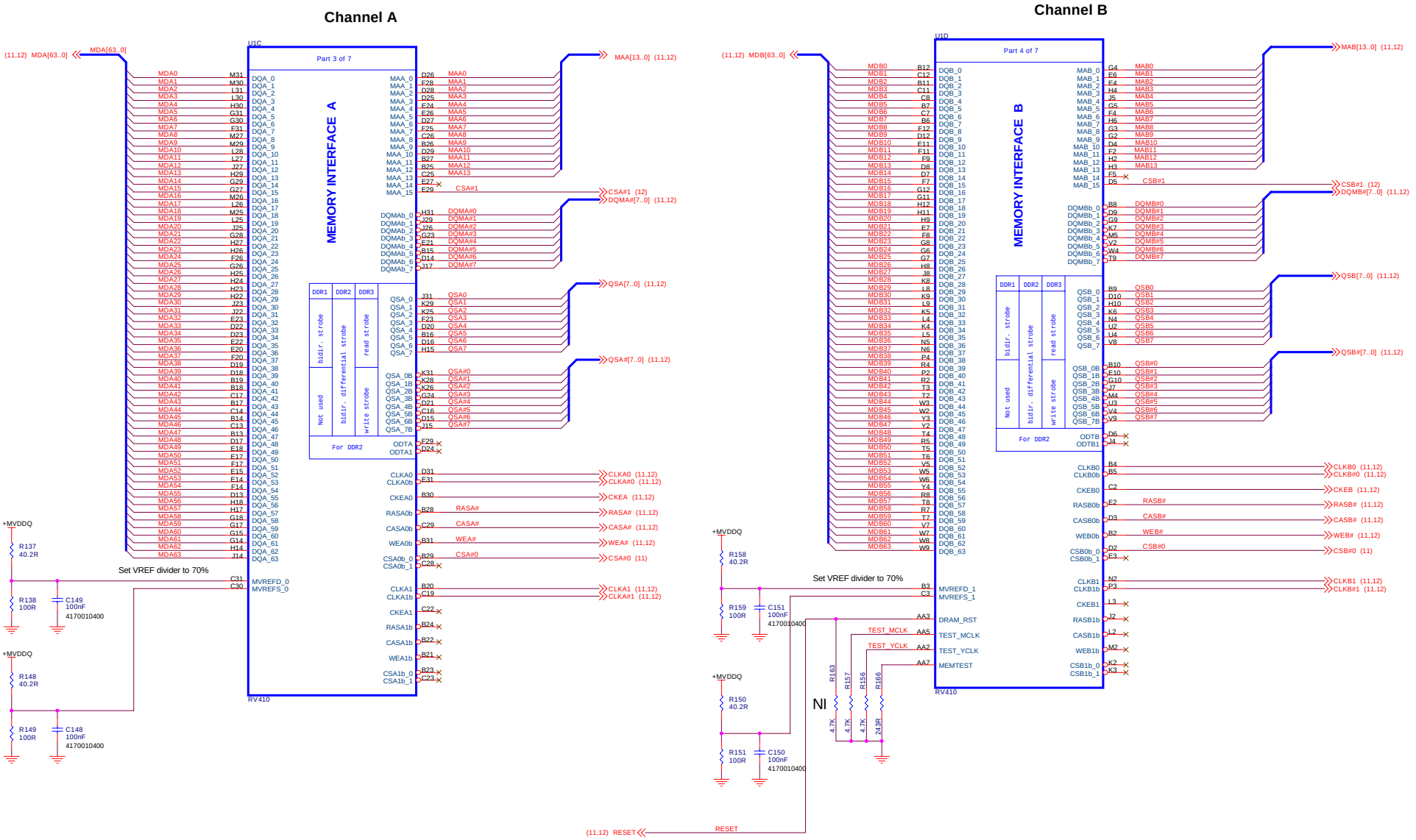
RV410 MEMORY CHANNELS A and B



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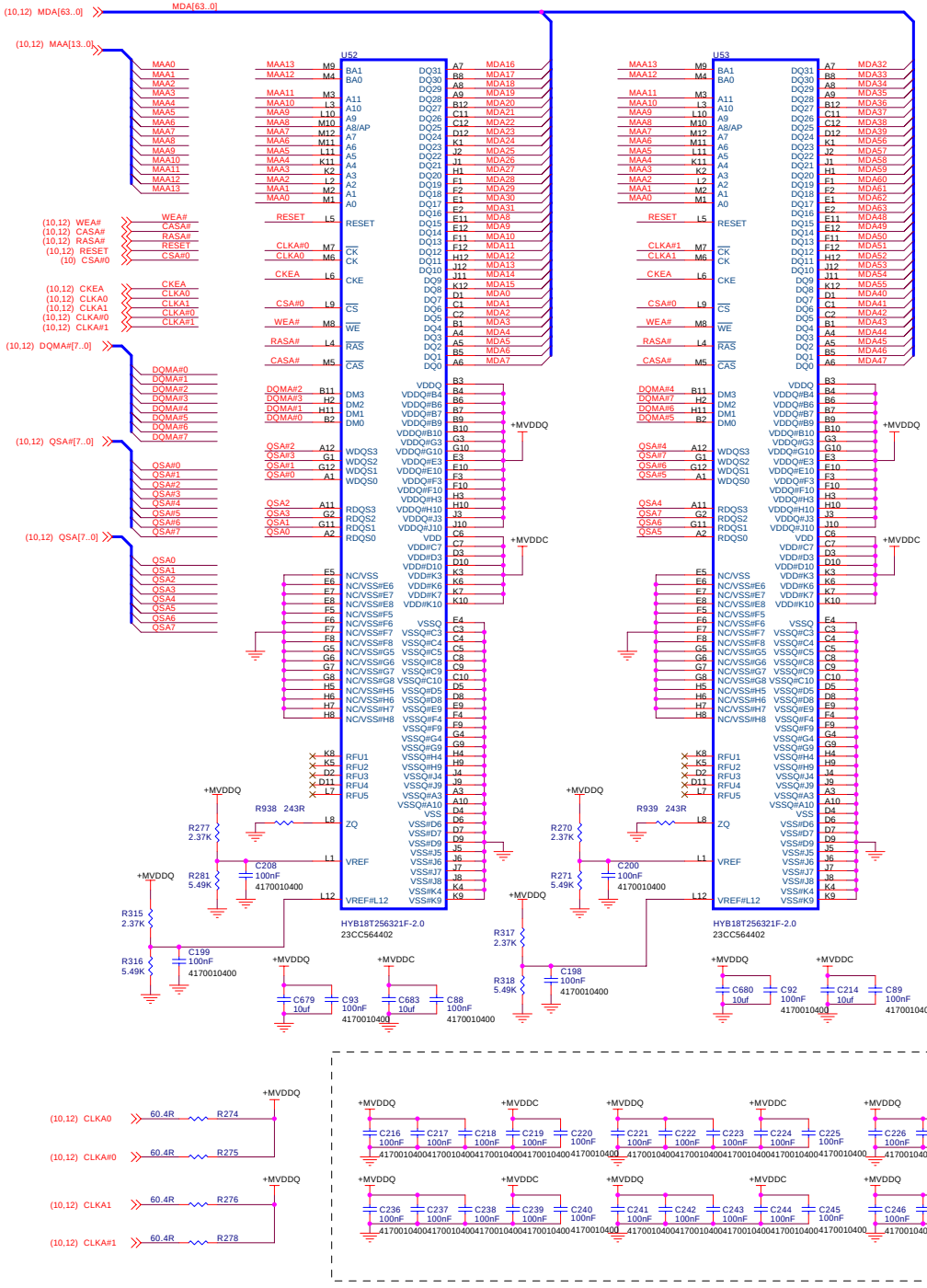
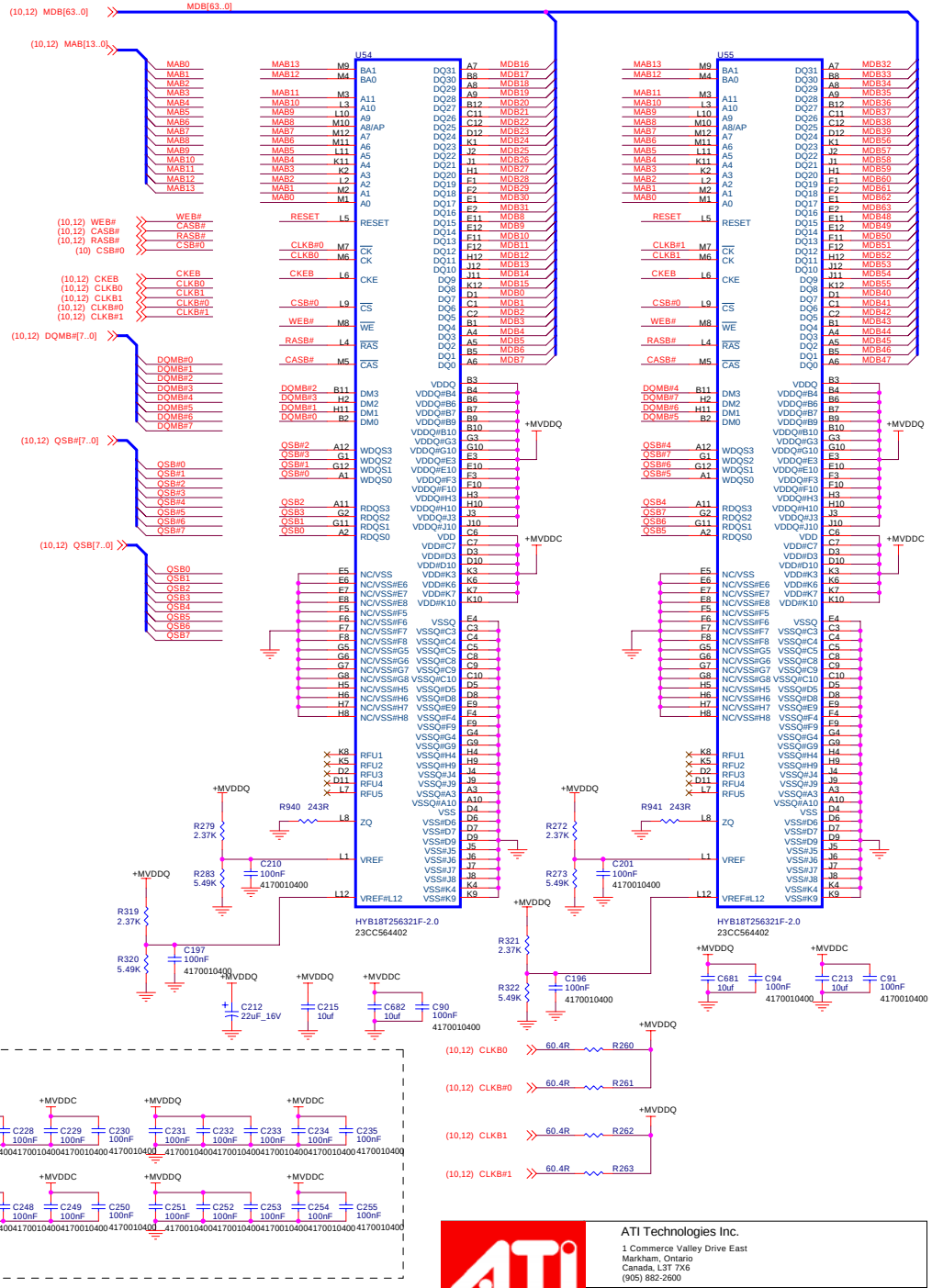
256 Mbit GDDRIII Channels A and B Rank 1

Channel A



Channel B



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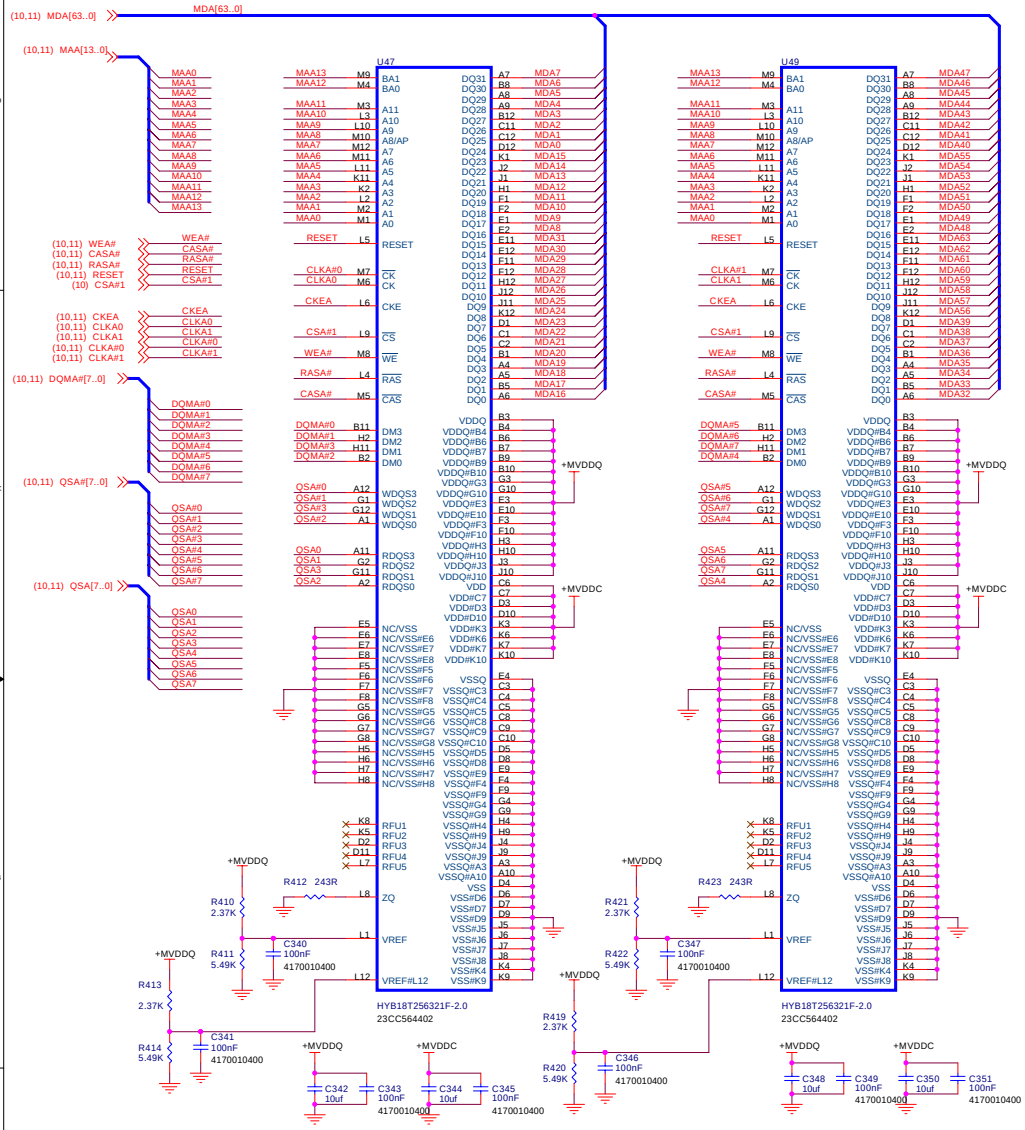
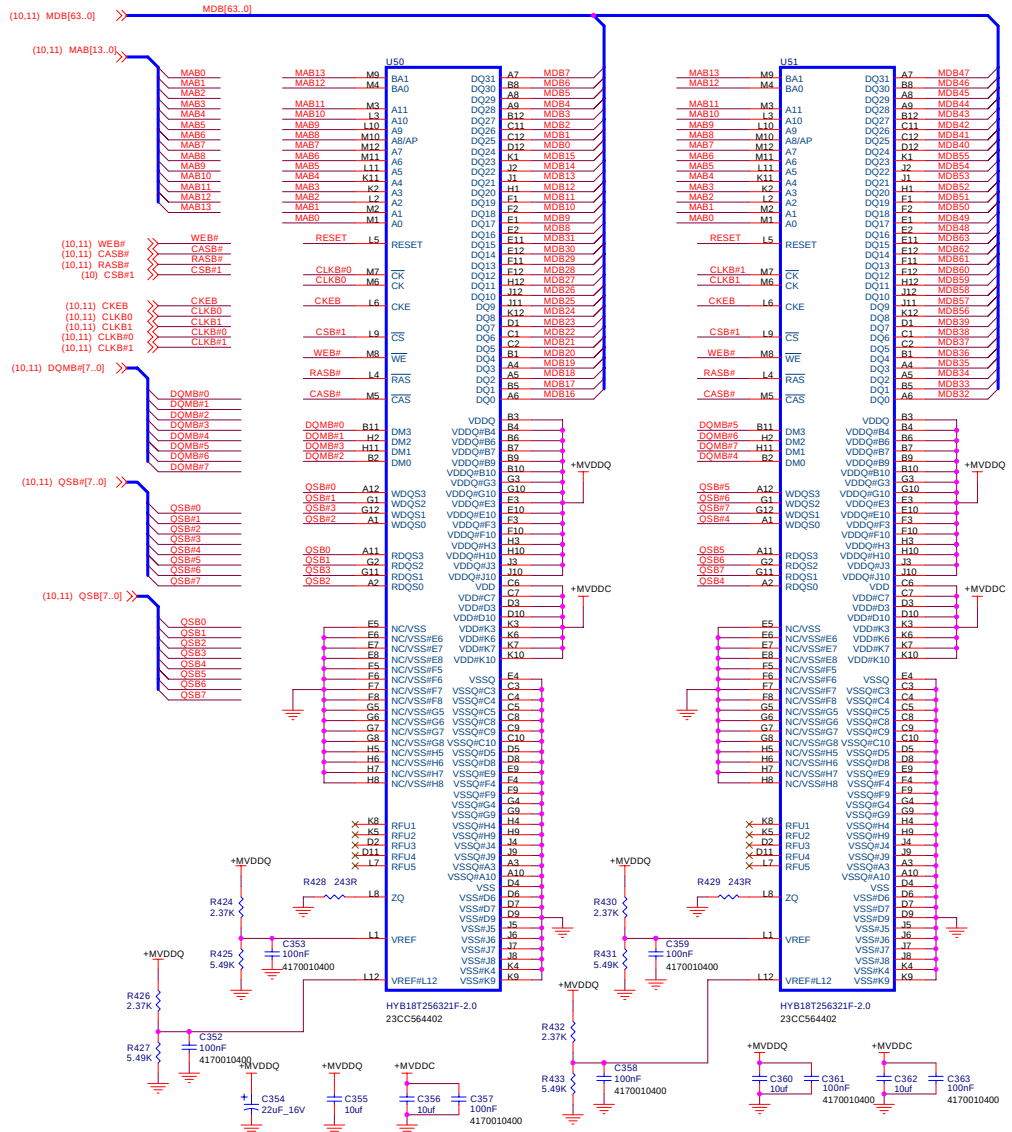
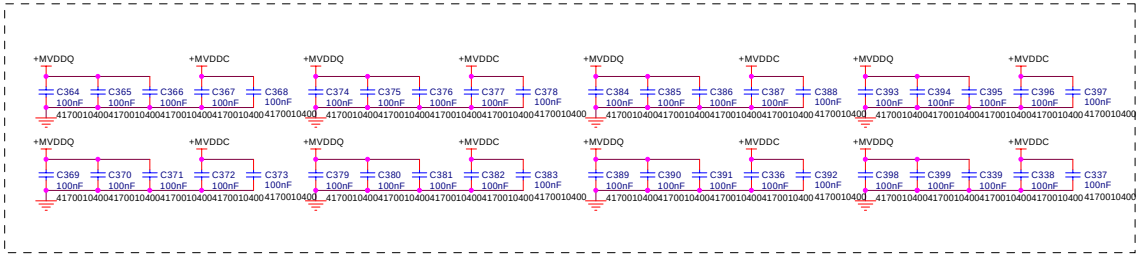
256 Mbit GDDRIII Channels A and B Rank 1

Channel A



Channel B





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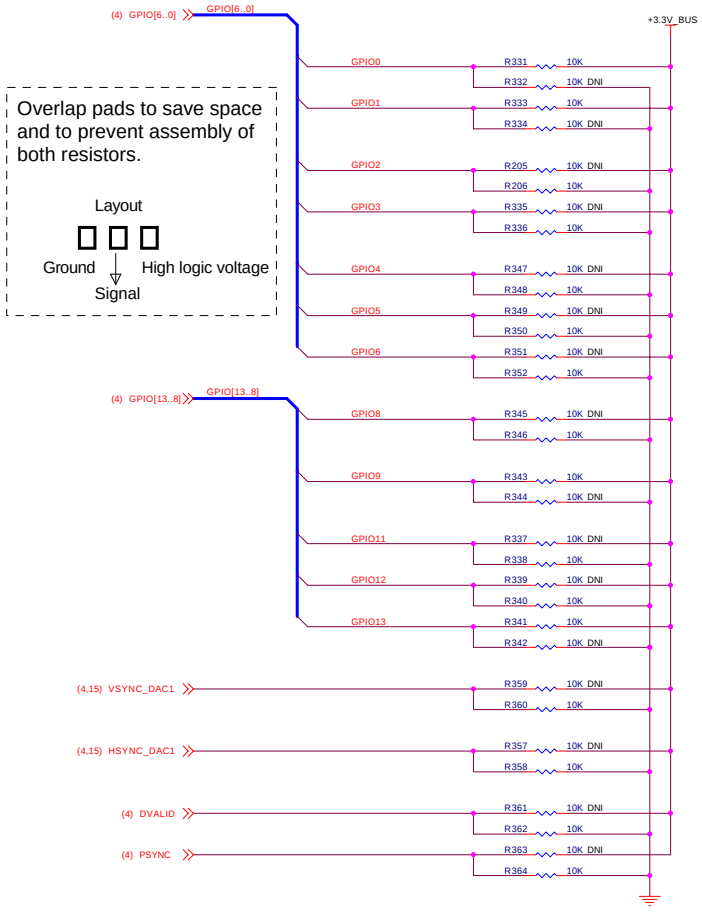
OPTION STRAPS

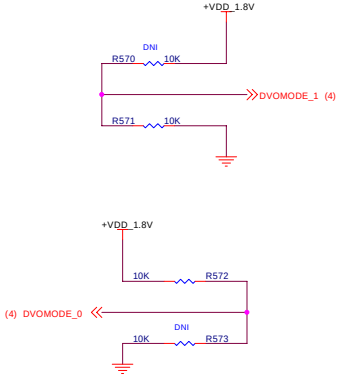


Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground — High logic voltage

Signal



RV410 Shared Straps — REV. 0.5

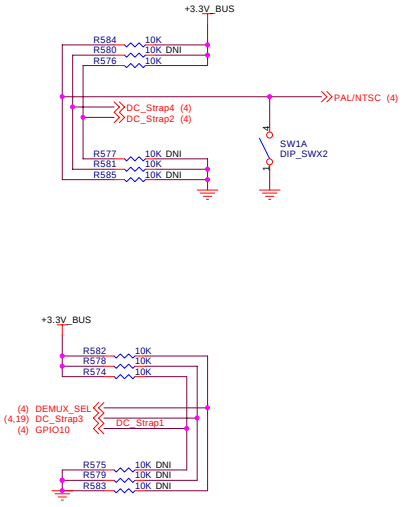
STRAPS	PIN	DESCRIPTION	VALUE
PCIE_SWING	GPIO(0)	Transmitter Swing Control 0: 50% Tx output swing mode 1: full Tx output swing	1
TRANSMIT_DE-EMPHASIS	GPIO(1)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	1
PCIE_MODE (ATI Internal)	GPIO(3:2)	PCIE mode: 00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: RESERVED	00
TX_IEXT	GPIO(4)	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage	0
FORCE _COMPLIANCE	GPIO(5)	Force chip to get to compliance state quickly for Tester purposes 0: Normal operation 1: Force to compliance state	0
PLL_BW (ATI Internal)	GPIO(6)	0: Full PLL Bandwidth 1: Reduced PLL bandwidth	0
DEBUG_ACCESS	GPIO(8)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible 0: Disable debug access 1: Enable debug access	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type. GPIO[9,13,12,11] 000x - No ROM,CHG_ID=00 001x - No ROM, CHG_ID=01 010x - No ROM, CHG_ID=10 011x - No ROM, CHG_ID=11 1001 - 1M Serial AT25F1024 ROM (Atmel) 1010 - 1M Serial AT45DB011 ROM (Atmel) 1011 - 1M Serial M25P10 ROM (ST) 1100 - 512K Serial M25P05 ROM (ST) 1101 - 1M Serial SST45LF010 ROM (SST) 1M Serial W45B512 ROM (WinBond) 512K Serial W45B012 ROM (WinBond) 1110 - 1M Serial SST25VF010 ROM (SST) 512K Serial SST25VF512 ROM (SST) 1111 - 1M NX25F011B ROM (NexFlash) **Chip IDs:** Chip ID is based on substrate fuses and CHG_ID strap (which comes from ROM if used, or pin straps if no ROM is connected): CHG_ID = ROMIDCFG[2:1] = GPIO[13:12]	1100
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this in low during reset. **0 - Slave VIP host port devices present** **1 - No slave VIP host port devices reporting presence during reset**	1
RFU	HSYNC	RFU **0 - Normal** 1 - Not used	0

RV410 Dedicated Straps — REV. 0.2

ZV_VOLTAGE_SEL0	DVOVMODE_0	DVOVMODE_0 is for ZV_LCDCNTL and ZV_LCDDATA(11:0). **0 - 3.3 V signaling** 1 - 1.8 V signaling	0
ZV_VOLTAGE_SEL1	DVOVMODE_1	DVOVMODE_1 is for ZV_LCDDATA(23:12) **0 - 3.3 V signaling** 1 - 1.8 V signaling	0

Board Straps — REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	DVALID, PSYNC.	Memory connected to R420 identification for BIOS **00 - Samsung GDDR 3 memory 144 Ball BGA package** 01 - TBD 10 - TBD 11 - TBD	000
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Not detected	0
DC_Strap3	LCDDATA(14)	HDTV out detect **0 - Detected** 1 - Enabled	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off **01 - DAC2 On as CRT** 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1



WARNING

Some of those straps must be connected to +VDD_1.8V if ZV_LCDATA bus is set to 1.8 V.

<Variant Name>

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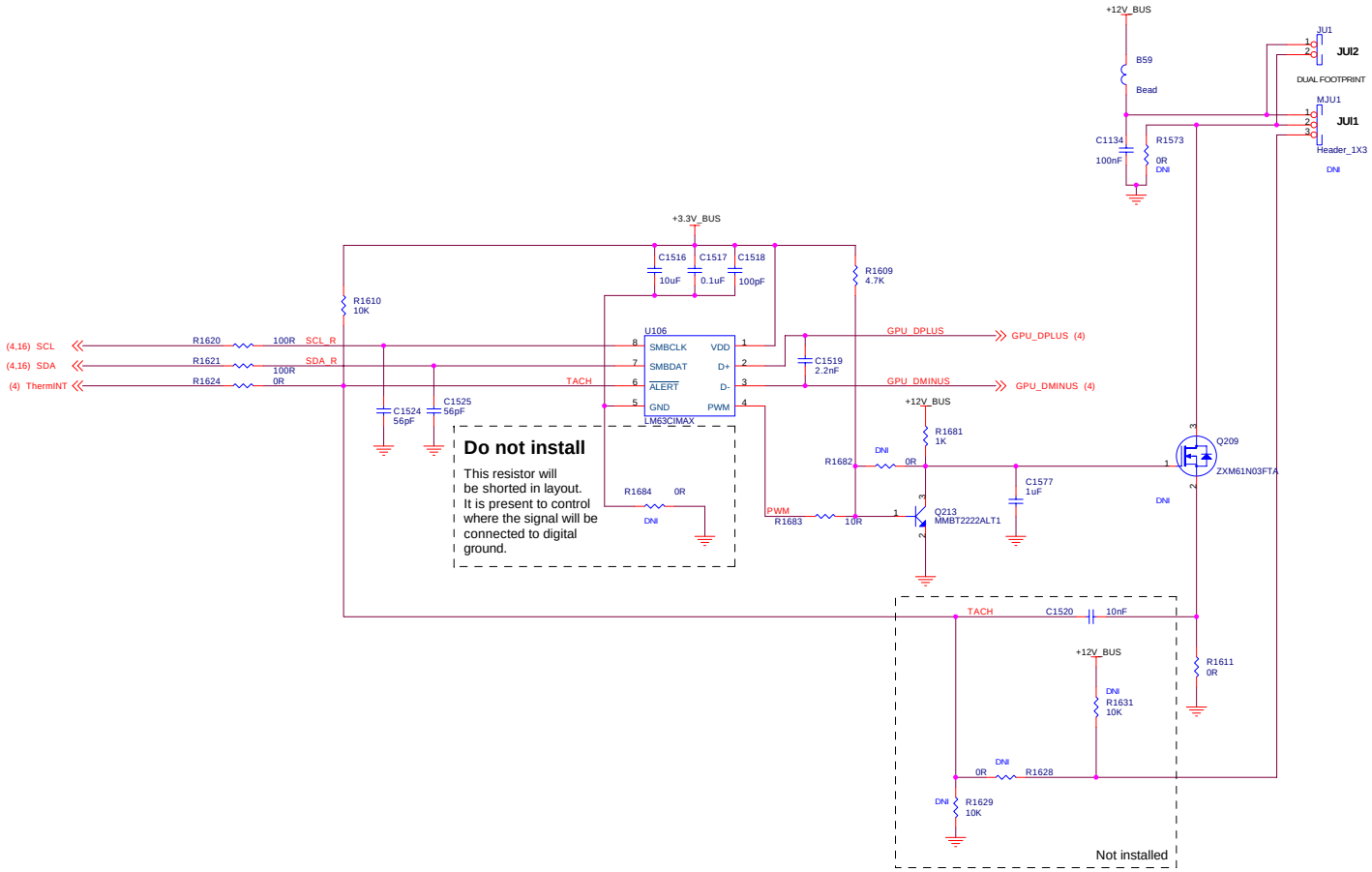
TEMPERATURE SENSE AND SPEED CONTROLLED FAN



ATI Technologies Inc.	
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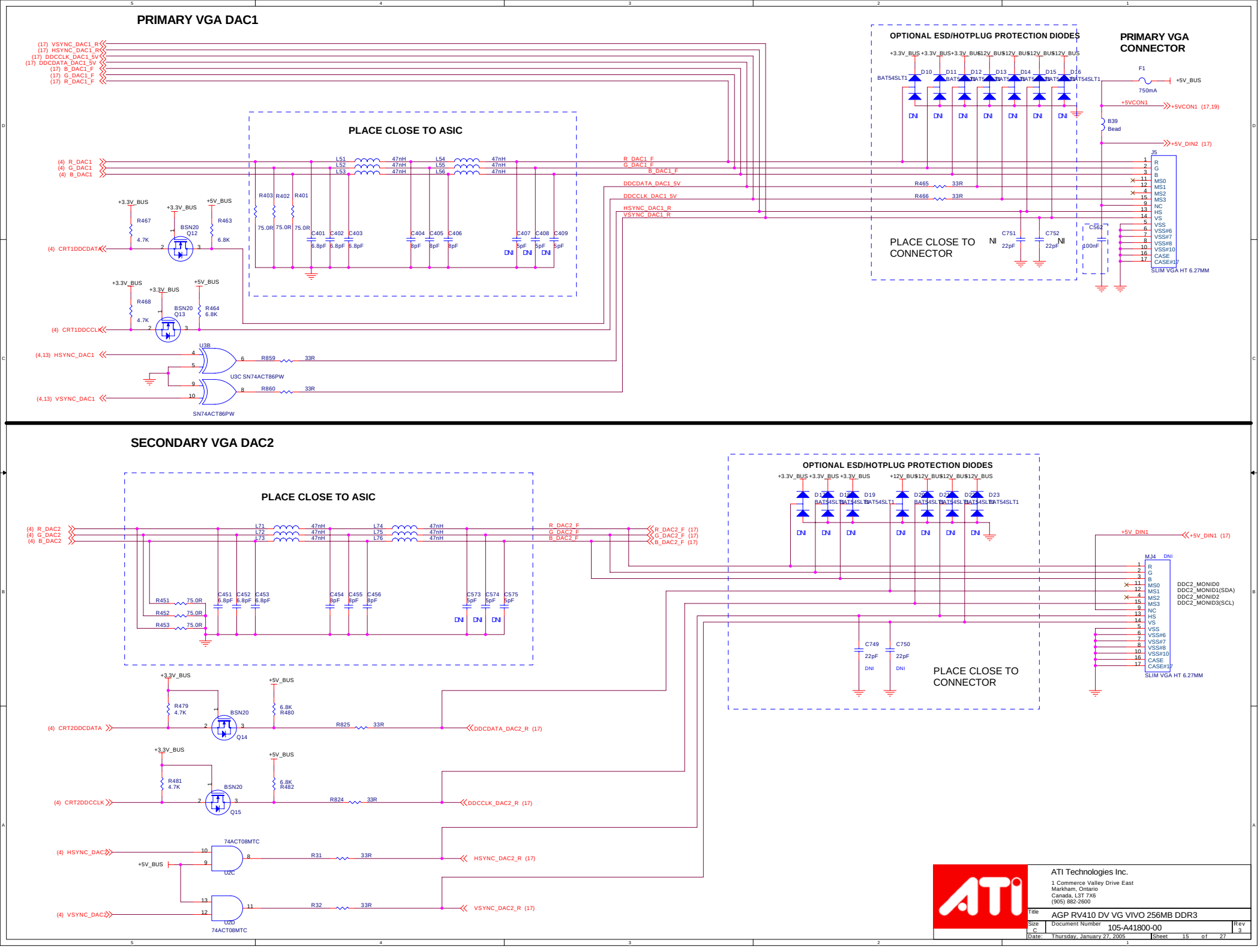
PRIMARY VGA DAC1
(17) VSYNC_DAC1_R
(17) HSYNC_DAC1_R
(17) DDCCLK_DAC1_5V
(17) DDCDATA_DAC1_5V
(17) B_DAC1_F
(17) G_DAC1_F
(17) R_DAC1_F
PLACE CLOSE TO ASIC
(4) R_DAC1
(4) G_DAC1
(4) B_DAC1
L51 47nH
L52 47nH
L53 47nH
L54 47nH
L55 47nH
L56 47nH
R403 75.0R
R402 75.0R
R401 75.0R
C401 6.8pF
C402 6.8pF
C403 6.8pF
C404 8pF
C405 8pF
C406 8pF
C407 5pF
C408 5pF
C409 5pF
DNI
R_DAC1_F
G_DAC1_F
B_DAC1_F
DDCDATA_DAC1_5V
DDCCLK_DAC1_5V
HSYNC_DAC1_R
VSYNC_DAC1_R
+3.3V_BUS
+5V_BUS
R467 4.7K
BSN20 Q12
R463 6.8K
(4) CRT1DDCDAT
R468 4.7K
BSN20 Q13
R464 6.8K
(4) CRT1DDCCLK
U3B
(4,13) HSYNC_DAC1
R859 33R
U3C SN74ACT86PW
(4,13) VSYNC_DAC1
R860 33R
SN74ACT86PW
OPTIONAL ESD/HOTPLUG PROTECTION DIODES
+12V_BUS
D10 BAT54SLT1
D11 BAT54SLT1
D12 BAT54SLT1
D13 BAT54SLT1
D14 BAT54SLT1
D15 BAT54SLT1
D16 BAT54SLT1
R465 33R
R466 33R
PLACE CLOSE TO CONNECTOR
C751 22pF
C752 22pF
NI
PRIMARY VGA CONNECTOR
F1
750mA
+5V_BUS
+5VCON1
+5VCON1 (17,19)
B39 Bead
+5V_DIN2 (17)
C562 100nF
J5
R
G
B
MS0
MS1
MS2
MS3
NC
HS
VS
VSS
VSS#6
VSS#7
VSS#8
VSS#10
CASE
CASE#17
SLIM VGA HT 6.27MM
SECONDARY VGA DAC2
PLACE CLOSE TO ASIC
(4) R_DAC2
(4) G_DAC2
(4) B_DAC2
L71 47nH
L72 47nH
L73 47nH
L74 47nH
L75 47nH
L76 47nH
R451 75.0R
R452 75.0R
R453 75.0R
C451 6.8pF
C452 6.8pF
C453 6.8pF
C454 8pF
C455 8pF
C456 8pF
C573 5pF
C574 5pF
C575 5pF
R_DAC2_F
G_DAC2_F
B_DAC2_F
R_DAC2_F (17)
G_DAC2_F (17)
B_DAC2_F (17)
R479 4.7K
BSN20 Q14
R480 6.8K
(4) CRT2DDCDATA
R825 33R
DDCDATA_DAC2_R (17)
R481 4.7K
BSN20 Q15
R482 6.8K
(4) CRT2DDCCLK
R824 33R
DDCCLK_DAC2_R (17)
74ACT08MTC
U2C
(4) HSYNC_DAC2
R31 33R
HSYNC_DAC2_R (17)
U2D
(4) VSYNC_DAC2
R32 33R
VSYNC_DAC2_R (17)
OPTIONAL ESD/HOTPLUG PROTECTION DIODES
D17 BAT54SLT1
D18 BAT54SLT1
D19 BAT54SLT1
D22 BAT54SLT1
D23 BAT54SLT1
PLACE CLOSE TO CONNECTOR
C749 22pF
C750 22pF
+5V_DIN1
+5V_DIN1 (17)
MJ4
DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)
SLIM VGA HT 6.27MM
ATI Technologies Inc.
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MUST BE INSTALLED IF NO
TMDS IS INSTALLED

LCDCNTL_R[3..0]

+3.3V_BUS

LCDCNTL_R0 RP600A 1 8 10K
LCDCNTL_R1 RP600B 2 7 10K
LCDCNTL_R2 RP600C 3 6 10K
LCDCNTL_R3 RP600D 4 5 10K

Place close to TMDS

(4) VID/DVO_R[11..0]

VID/DVO_R[11..0]

U37

VID/DVO_R0 18 D0
VID/DVO_R1 17 D1
VID/DVO_R2 16 D2
VID/DVO_R3 15 D3
VID/DVO_R4 14 D4
VID/DVO_R5 13 D5
VID/DVO_R6 10 D6
VID/DVO_R7 9 D7
VID/DVO_R8 8 D8
VID/DVO_R9 7 D9
VID/DVO_R10 6 D10
VID/DVO_R11 5 D11

TX0- 35 TX0M_EXT
TX0+ 36 TX0P_EXT
TX1- 38 TX1M_EXT
TX1+ 39 TX1P_EXT
TX2- 41 TX2M_EXT
TX2+ 42 TX2P_EXT
TXC- 32 TXCM_EXT
TXC+ 33 TXCP_EXT

TXCP_EXT (17)
TXCM_EXT (17)
TX2P_EXT (17)
TX2M_EXT (17)
TX1P_EXT (17)
TX1M_EXT (17)
TX0P_EXT (17)
TX0M_EXT (17)

R1240 330R C481 100nF
R1241 330R C482 100nF
R1242 330R C483 100nF
R1243 330R C484 100nF

+AVCC_TMDS

+3.3V_BUS

B31 200R

AVCC 34
AVCC#40 40
AGND 37
AGND#43 43

C460 100pF
C461 2.2nF
C462 100nF
C463 100pF
C464 2.2nF
C465 100nF
C466 47uF

+3.3V_BUS
R625 1K
R620 1K
I2C_ADDR 24 CTL3/A2

(4) LCDCNTL_R[3..0]

LCDCNTL_R[3..0]

LCDCNTL_R1 20 HSYNC
LCDCNTL_R0 21 VSYNC
LCDCNTL_R2 19 DE
LCDCNTL_R3

+VREF_TMDS
12 IDICK+
11 IDCK-

+3.3V_BUS
R483 5.1K
MSEN_TMDS 48 MSEN

R1103 33K
R1104 0R
HPD_ExtTMDS 44
I2C_RST 25 EDGE/HTPLG ISEL/RST#

(2,18,21) AGP_RESET#

INSTALL FOR Si164
HI = I2C SELECT,LO = I2C CTRL RESET

(4,14) SDA 26 SDA
(4,14) SCL 27 SCL

+3.3V_BUS
Do not install
R484 0R
R492 0R

1 GND#1
31 AGND#31
47 PD#
Sil1162

+VREF_TMDS
VREF 2
EXT_SWING 30
EXT_SWING R485 680R

+PVCC_TMDS
PVCC1 28
PVCC2 46
PGND 29
PGND#45 45
VCC#22 22
VCC 3

C469 100pF
C470 100nF
C479 100pF
C480 100nF
C471 22uF_10V

+3.3V_BUS
GND 4
GND#23 23
TH_GND 49

C472 100pF
C473 100nF
C474 2.2nF
C475 100nF
C476 100pF
C477 2.2nF

+3.3V_BUS
B32 200R
22uF_10V C1236

Max 25 mA

+12V_BUS
R301 360R
R304 680R
R491 2K

REG9 TL431CDBVR

(4) HPD_ExtTMDS

HPD_ExtTMDS

+3.3V_BUS
R486 20K
R487 20K
402
402

D35 MMBZ5222BLT1
R490 100K
Q32 CMPT3904
Q33 CMPT3904

R488 20K 402
R489 20K 402

HPD_ExtTMDS_DVI (17)

SELECT VREF ACCORDING
TO SWING ON D[23:0]

+VDDR4
C478 100nF X7R
R302 1.0K
+VREF_TMDS
C467 100nF X7R
R303 1.0K

SELECT VREF ACCORDING
TO SWING ON D[23:0]

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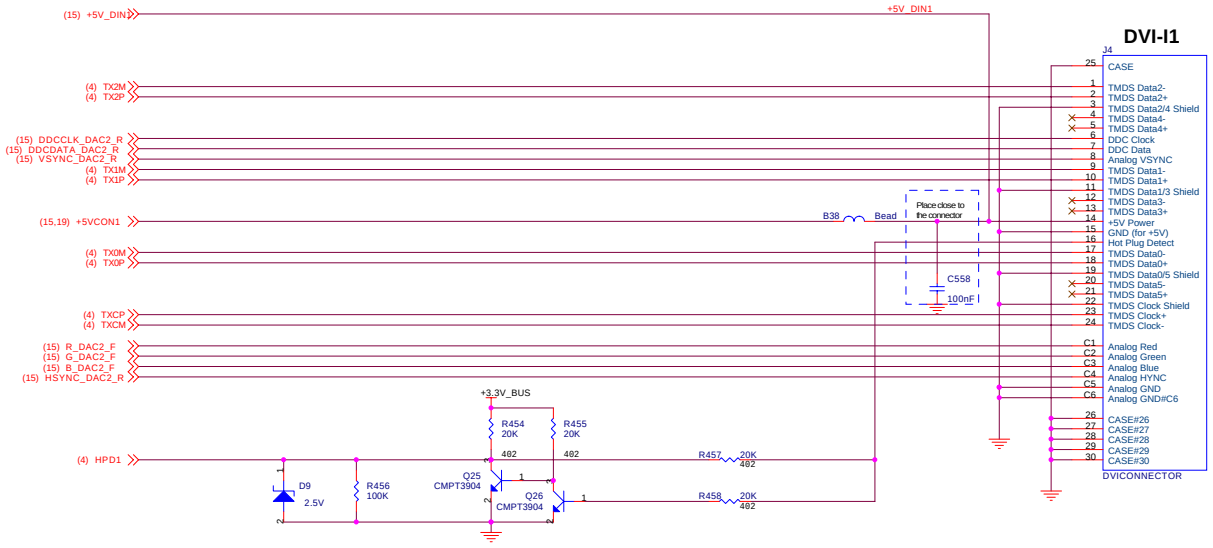
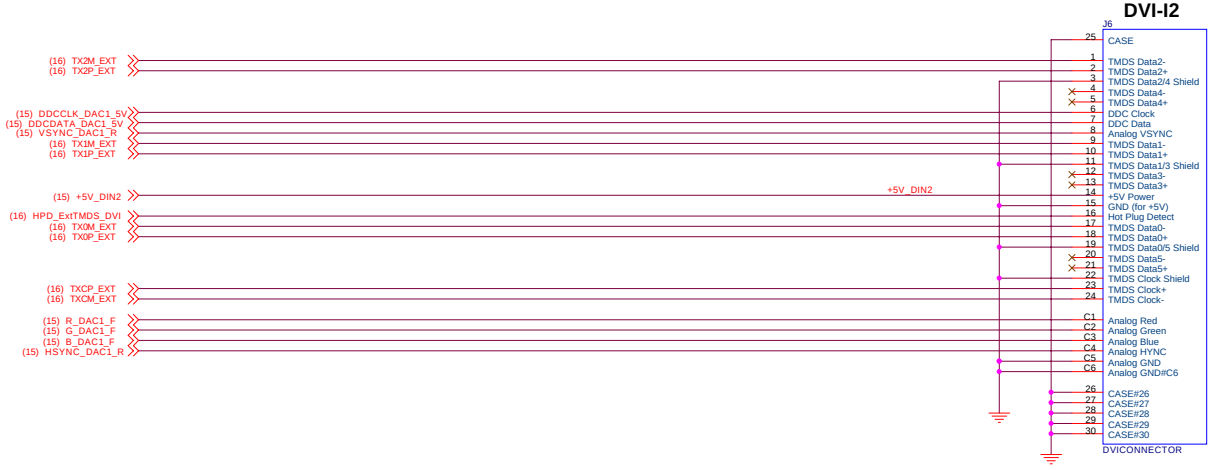
PRIMARY DVI-I CONNECTOR (DVI-I1)
(Internal TMDS + DAC2 VGA)



SECONDARY DVI-I CONNECTOR (DVI-I2)
(Ext TMDS + DAC1 VGA)



<Variant Name>

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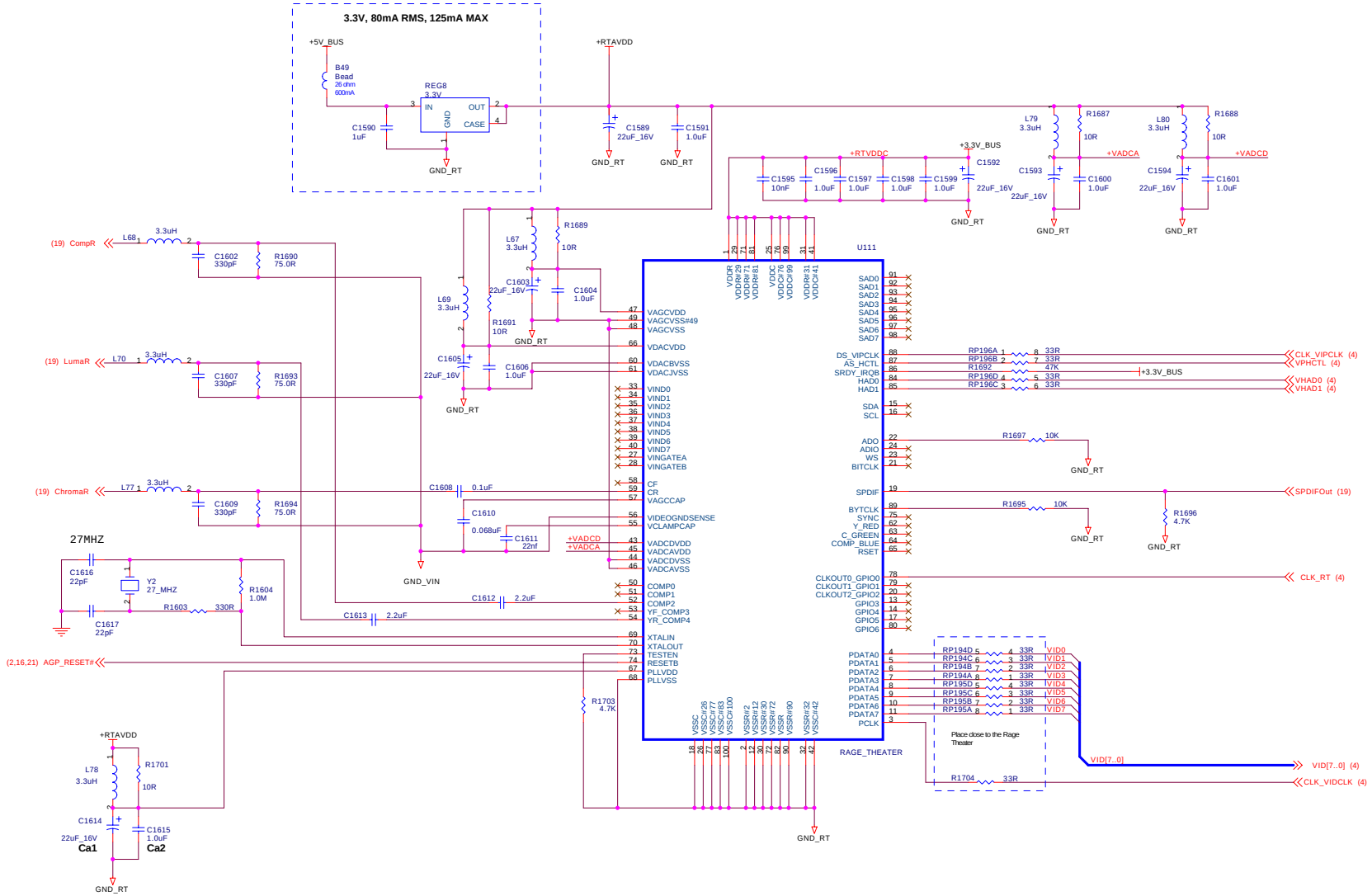

IMPORTANT

Layout Guide line of THEATER

#1 : Ca1 and Ca2 have to be placed as close as possible to the respective pins of Rage THEATER

#2 : GND_VIN should be seperated from Digital or Chassis Ground and have no loops

#3 : GND_VIN should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

Put 2D line as close as possible to pin 56 of Rage Theater

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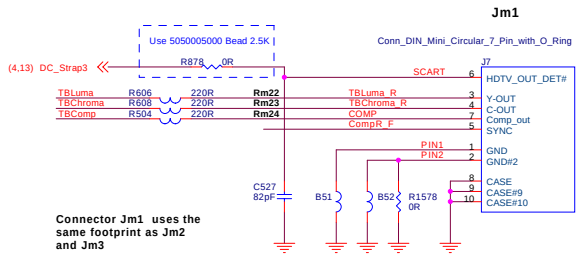
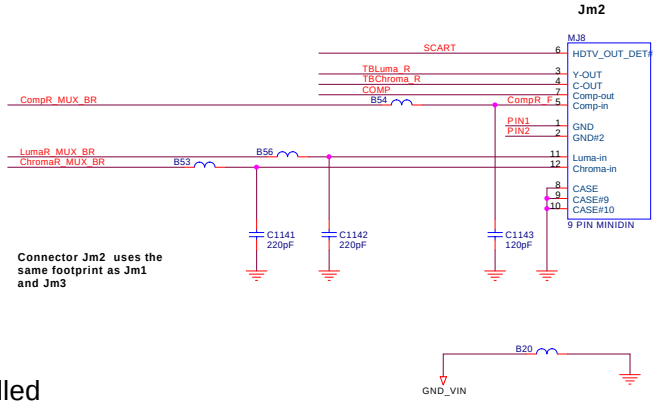
TV Out (SVHS) MiniDIN 7-pin

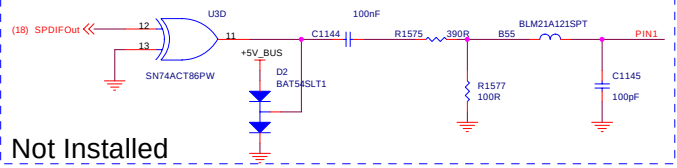


ViVO connector (Installed only if Rage Theater is installed)



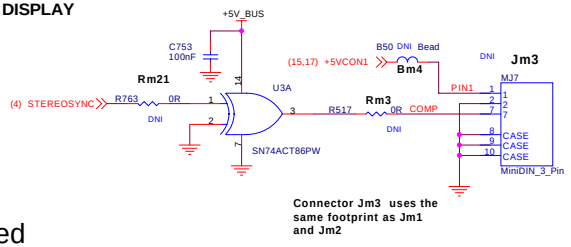
Not Installed

SPDIF - OUT



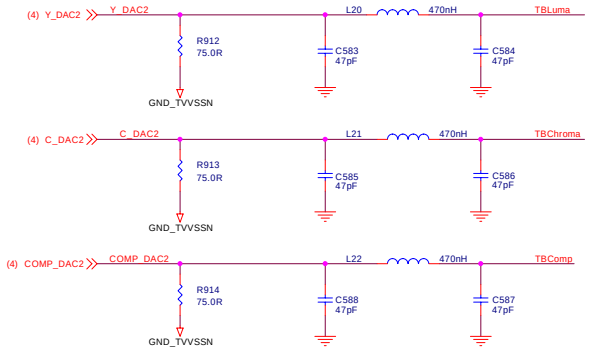
Not Installed

STEREOSCOPIC DISPLAY CONNECTOR

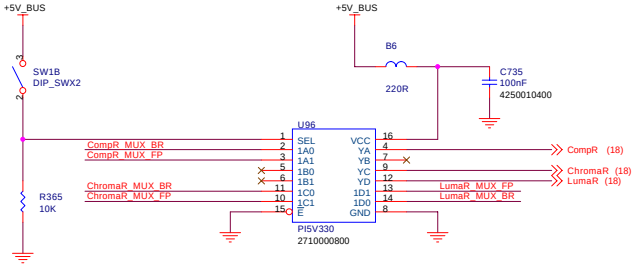


Not Installed

TV-OUT

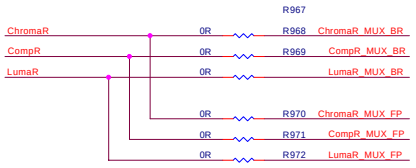


Video In Mux when Bracket and Front panel connector are installed



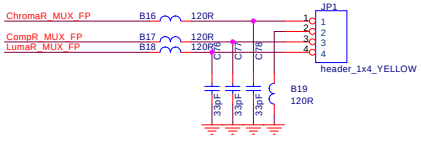
Not Installed

MUX BYPASS



Not Installed

Video In Front panel connector



Not Installed

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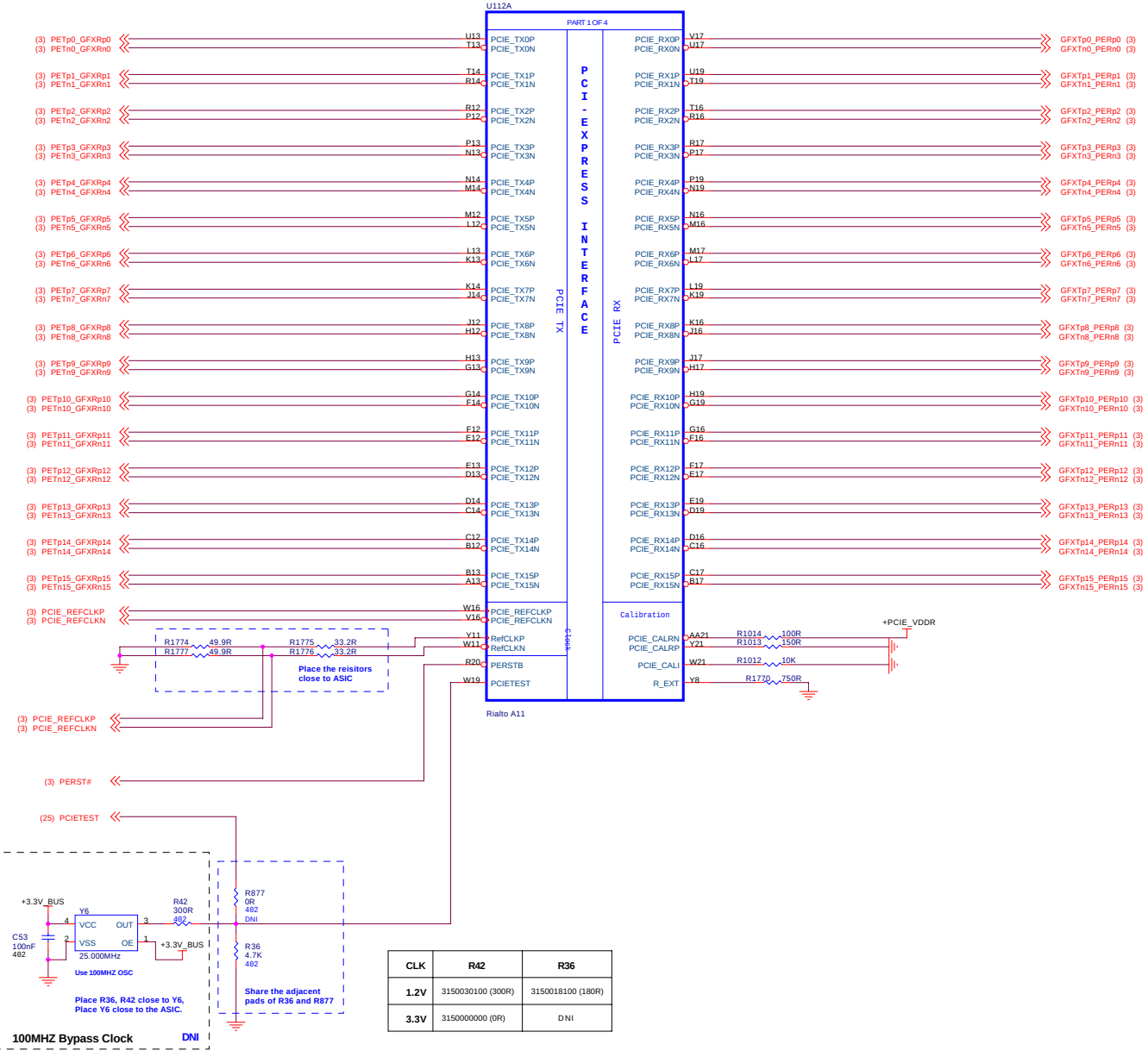
Rialto ASIC p/n is: 218BAPAGA11F



CLK	R42	R36
1.2V	3150030100 (300R)	3150018100 (180R)
3.3V	3150000000 (0R)	DNI

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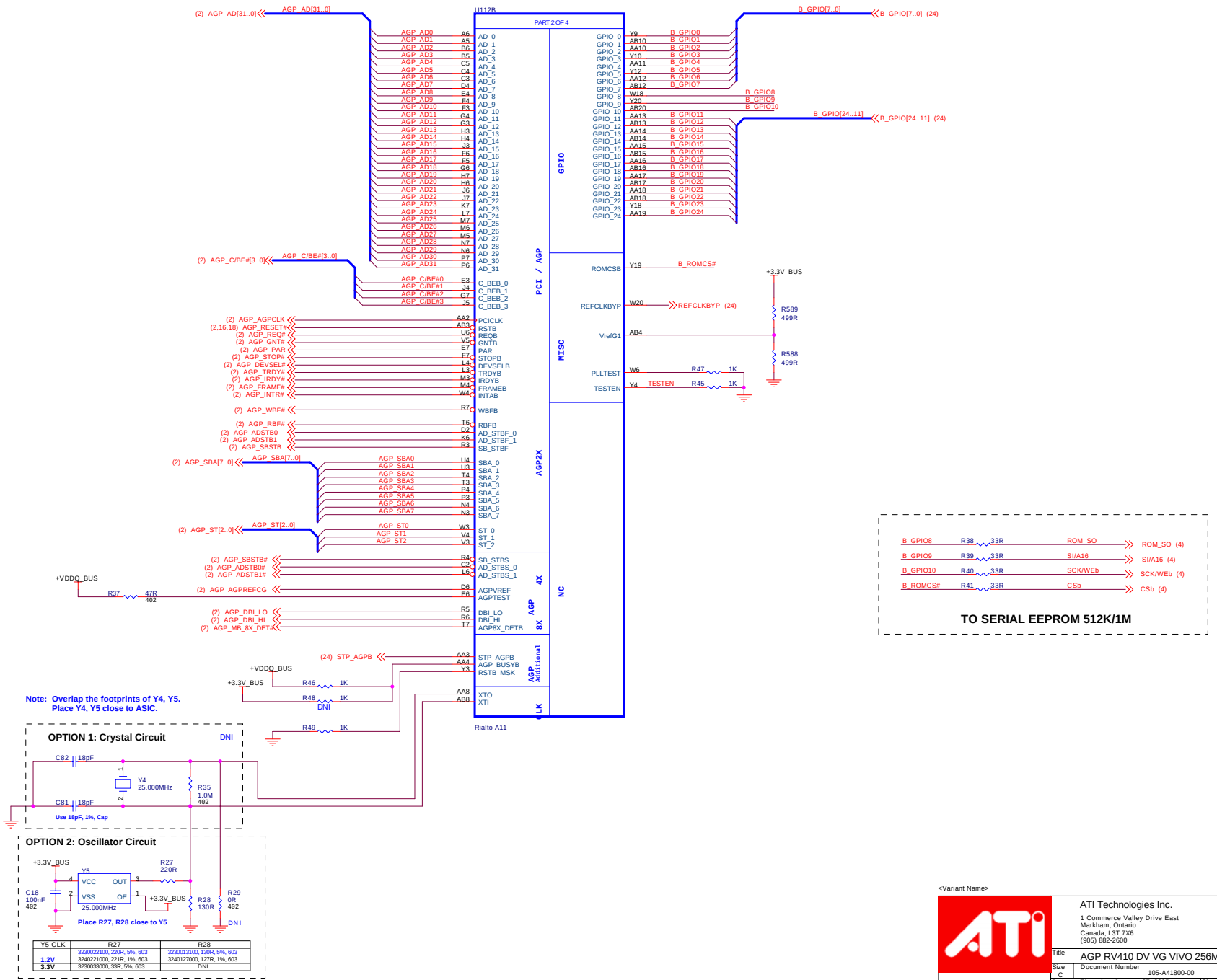

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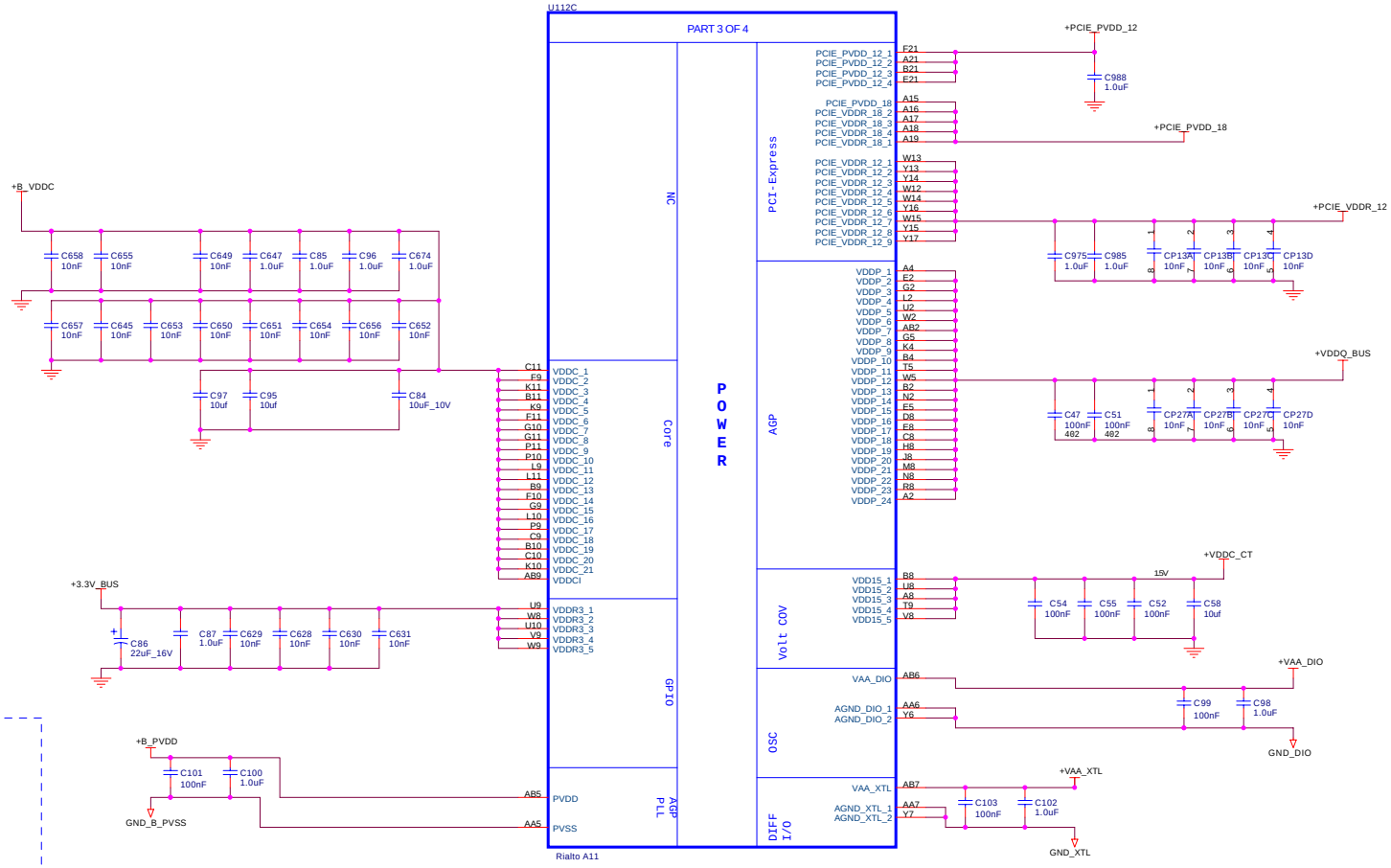
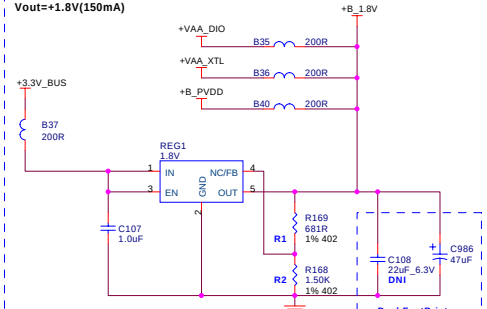


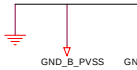
NOTE: Place REG1 close to ASIC.

REGULATOR FOR B_1.8V
Vin=+3.3V
Vout=+1.8V(150mA)



Use SP6201EM5-ADJ, 200mA, SOT23-5, DO<500mV (2480041200) $0.11
Alt. TI TPS76301, ADJ, 150mA, DO<300mV, SOT23 (2480040800)
Alt. TI TPS76318, 1.8V, 150MA, DO<300mV, SOT23 (2480003900)

	SP6201EM5-ADJ Vo=1.25 (1+R1/R2)	TPS76301, ADJ Vo=1.186 (1+R1/R2)
R1	3160681000, 681R, 1%	
R2	3160150100, 1.50K, 1%	



NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

<Variant Name>

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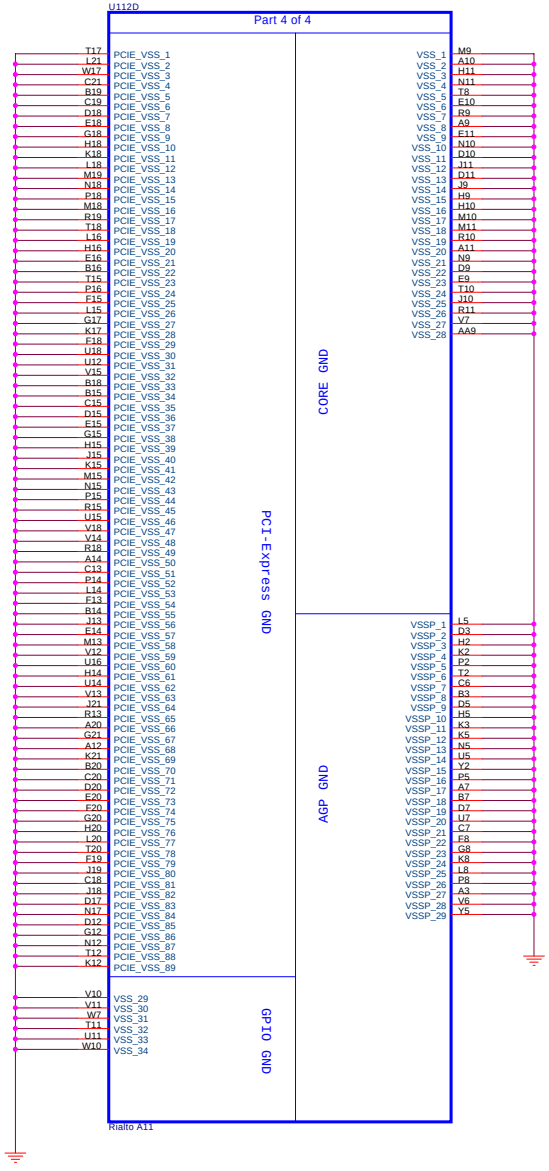

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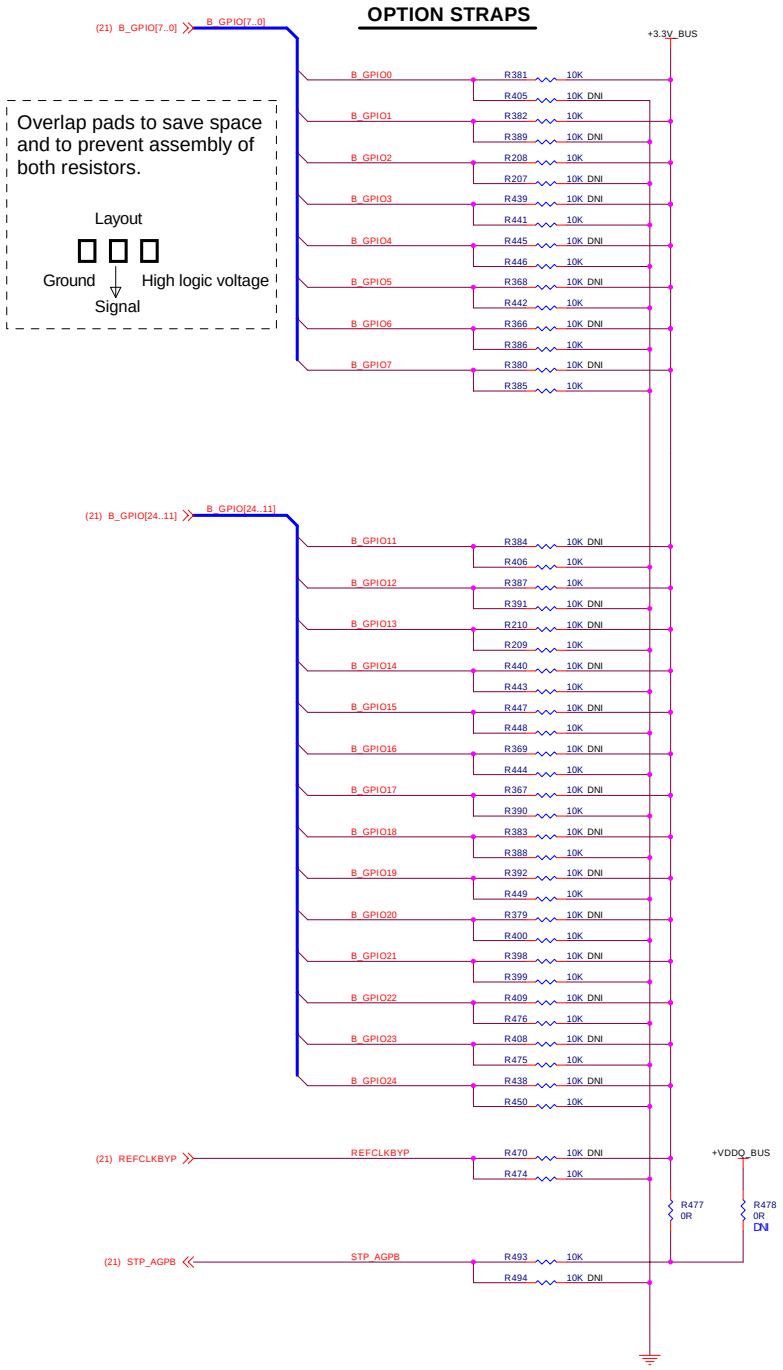

PCIE_AGP_Bridge Shared Straps

STRAPS	PIN	DESCRIPTION	DEFAULT
PCIE_PTX_PWRS_ENB	GPIO(0)	PCI Express transmitter power-saving enable bar 0 - 50% Tx output swing for mobile applications 1 - Full output swing	1
PCIE_PTX_DEEMPH_EN	GPIO(1)	PCI Express transmitter de-emphasis enable 0 - de-emphasis disenable 1 - de-emphasis enable	1
PCIE_ICP (1:0)	GPIO(3:2)	Charge pump current setting 00 - 5.0uA 01 - 10.0uA **10 - 15.0uA** 11 - 20.0uA	01
PCIE_PTX_IEXT	GPIO(4)	PCI Express transmitter extra ouptput current 0 - no extra current 1 - extra current in output stage	0
DEBUG_ACCESS	GPIO(5)	1 - Set the debug bus muxes to bring out debug signals even if registers are inaccessable	0
PCIE_PPLL_BW	GPIO(6)	PCI Express PLL bandwidth setting 0 - Full PLL bandwidth 1 - Reduces PLL bandwidth	0
PCIE_REVERSE_ALL	GPIO(7)	0 - Don't reverse physical PCIE lanes 1 - Reverse physical PCIE lanes	0
ROMIDCFG(1:0)	GPIO(12:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 00 - No ROM, CHG_ID=0 01 - 512Kb Serial AT25F512 ROM (Atmel) or AT24F1024 ROM (Atmel) **10 - 512K Serial M25P05A ROM (ST) or PM25LV512 (PMC)** 11 - 1M Serial M25P10A ROM (ST) or PM25LV010 (PMC)	10
PCI_RETRY_ENb	GPIO(13)	0 - Enable all PCI read/write retry, retry cycle 0x3 1 - Disable PCI read/write retry	0
VGA_MONO_MODE(1:0)	GPIO(24, 14)	00 - only VGA controller 01 - only MONO controller 10 - neither VGA/MONO controller 11 - both VGA/MONO controller	00
REFCLK_LINK_CONFIG	GPIO(15)	One of the strap bit to encode the combination of: SEND_LINK_TRAINING_IMMEDIATELY MOBILE_EN AGP_ONLY .... etc,	0
MULTIFUNC	GPIO(16)	For MULTIFUNC, when TESTEN(pin)=0, 0 = 00 - Single function device 1 = 01 - Two function device. No AGP in either function	0
PCIE_FORCE_COMPLIANCE		For PCIE_FORCE_COMPLIANCE, when TESTEN(pin)=1, 0 - Normal operation 1 - Force LC into compliance mode	0
AGPFBSKEW(1:0)	GPIO(18:17)	AGP 1xclock feedback phase adjustment wrt refclk(cpuclk) 00 - refclk slightly earlier than feedback 01 - refclk 1 tap later than feedback 10 - refclk 1 tap earlier than feedback 11 - refclk 2 tap earlier than feedback clock	00 internal pulldown
X1CLK_SKEW(1:0)	GPIO(20:19)	Clock phase adjustment between x1clk and x2clk 00 - 0 tap delay 01 - 1 tap delay 10 - 2 tap delay 11 - 3 tap delay	00 internal pulldown
BUSCFG	GPIO(21)	Control BUS type, CLK PLL select	0 internal pulldown
AGP_ONLY	GPIO(22)	0 - normal operation, assume VPU is working 1 - for debugging, shut off VPU so the bridge is working in AGP only mode	0
PCIE_LINK_TIMEOUT_OVERRIDE	GPIO(23)	0 - Timeout is active 1 - Timeout is disabled	0
MOBILE_EN	REFCLKBYP		0
BUS_PCI_CFG_RETRY_Enb	STP_AGPB	when internal MOBILE_EN=0 STRAP_BUS_PCI_CFG_RETRY_Enb	1

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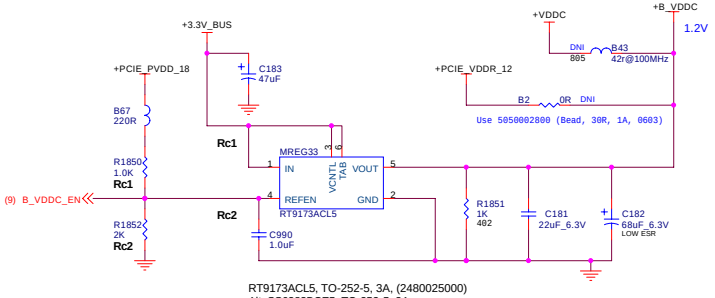
Regulator for B_VDDC
Vout = 1.2V
Iout = 1000mA MAX

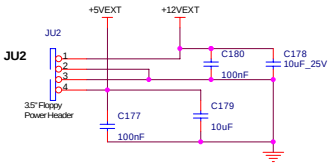


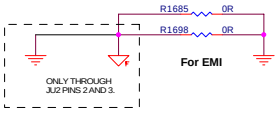
RT9173ACL5, TO-252-5, 3A, (2480025000)
Alt. SS6383BCE5, TO-252-5, 3A

Put copper under MREG33 for heat dissipation.

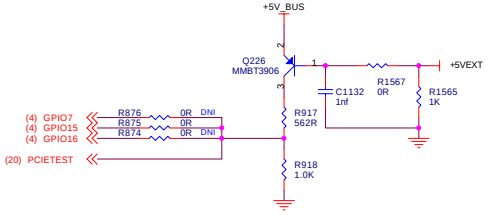
+B_VDDC	Rc1	Rc2
1.2V	3240215100, 2.15K, 1%	3240124100, 1.24K, 1%
1.26V	3240200100, 2K, 1%	3240124100, 1.24K, 1%
1.31V	3240187100, 1.87K, 1%	3240124100, 1.24K, 1%

External Power & Controls





EXTERNAL POWER DETECT



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

CRT
SCREWS

ASSY1
SCREW
JACKSCREW
ASSY

ASSY4
SCREW
JACKSCREW
ASSY

ASSY6
SCREW
PAN_HEAD

ASSY8
BRACKET
DVI, TV Out, DVI

ASSY9
BRACKET
VGA, VID OUT, DVI

ASSY10
BRACKET
VGA, DVI

DVI SCREWS

ASSY2
SCREW
JACKSCREW
ASSY

ASSY5
SCREW
JACKSCREW
ASSY

MISC. BOARD PARTS

ASSY3
BLANK
LABEL
1.50W_X_0.50H
ASSY

ASSY7
ANTISTATIC
BAG
6_X_11
ASSY

MT1
MT_Hole_0.136_in.
620NOPN004

H103
HEATSINK

REF2
PCB
109-A37900-00A

REF3
ATI LOGO
LABEL
ATI_LOGO_LABEL

H104
NA

Check if need to Add Rialto Hintsink?

<Variant Name>

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