

P2002

2GB GDDR5, 256b, 64Mx32

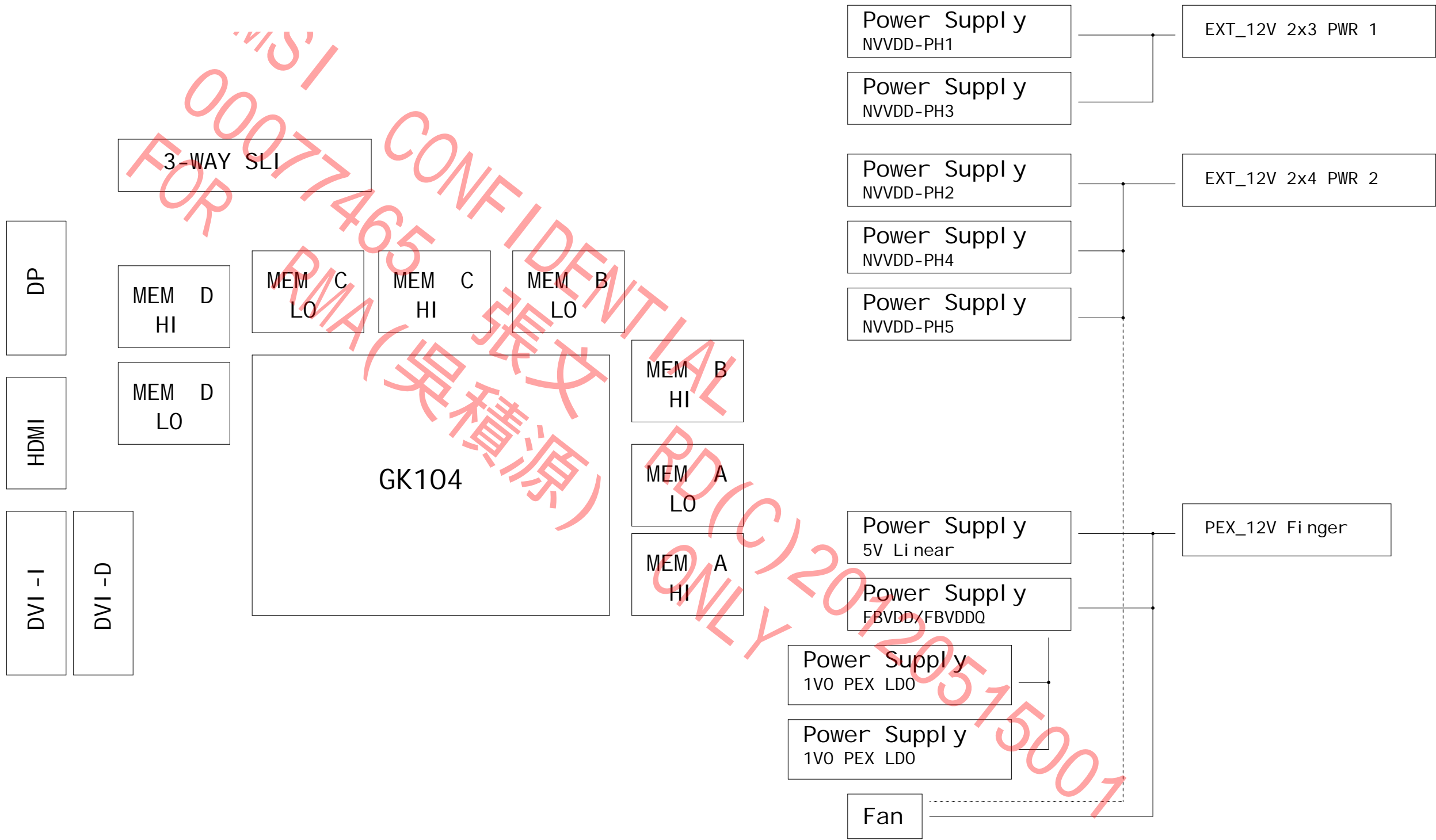
Stacked DVI -I /DVI -D + HDMI + DP

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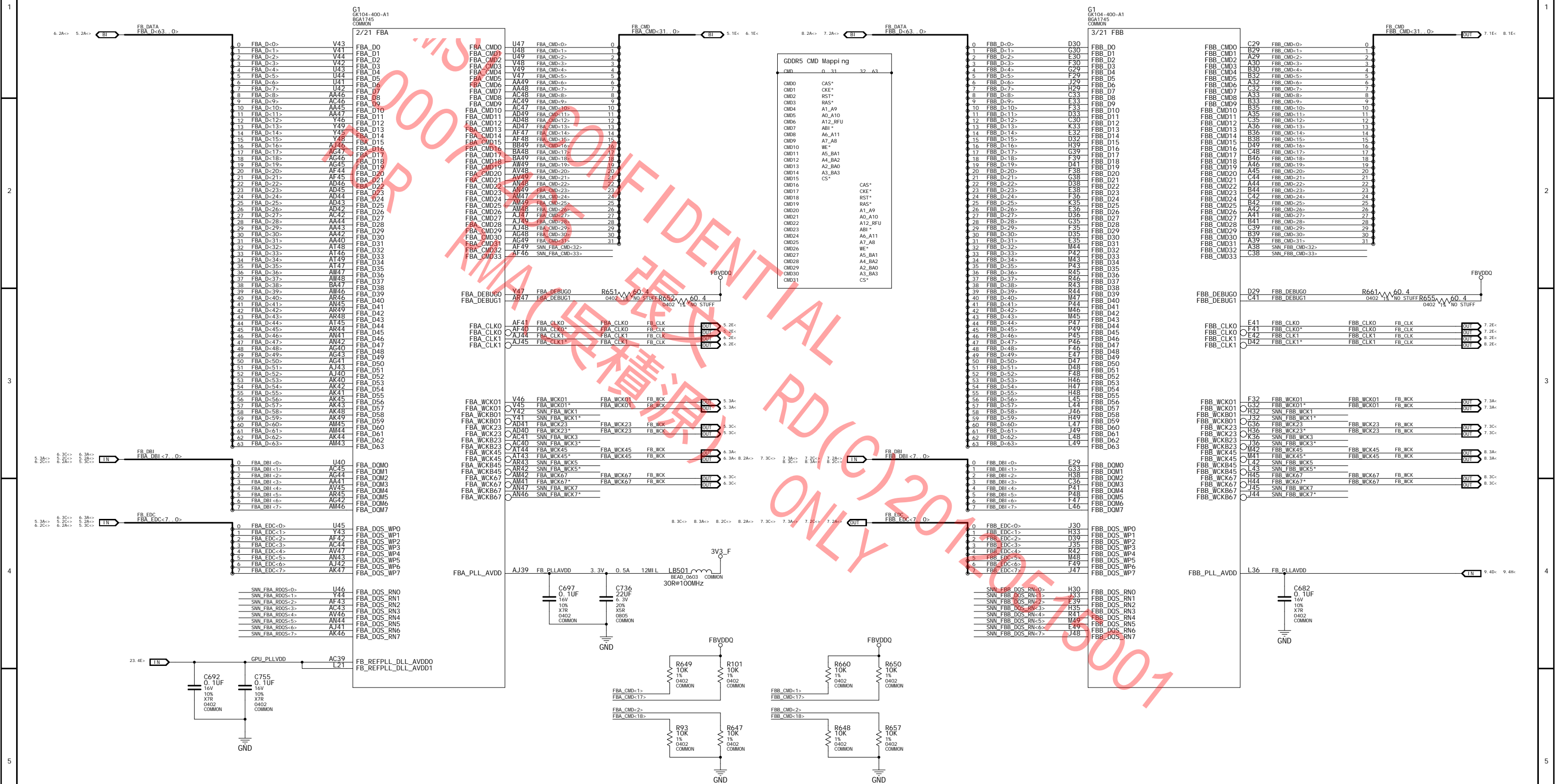


Page3: PCI Express

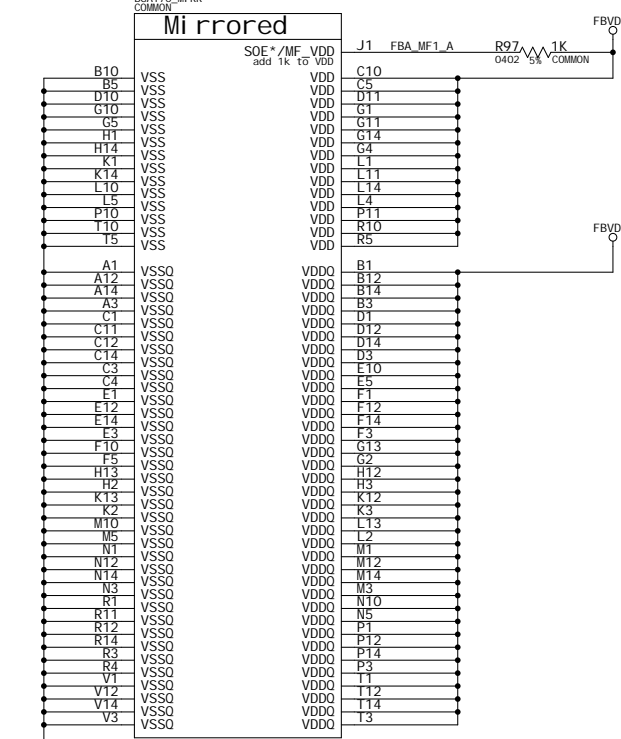


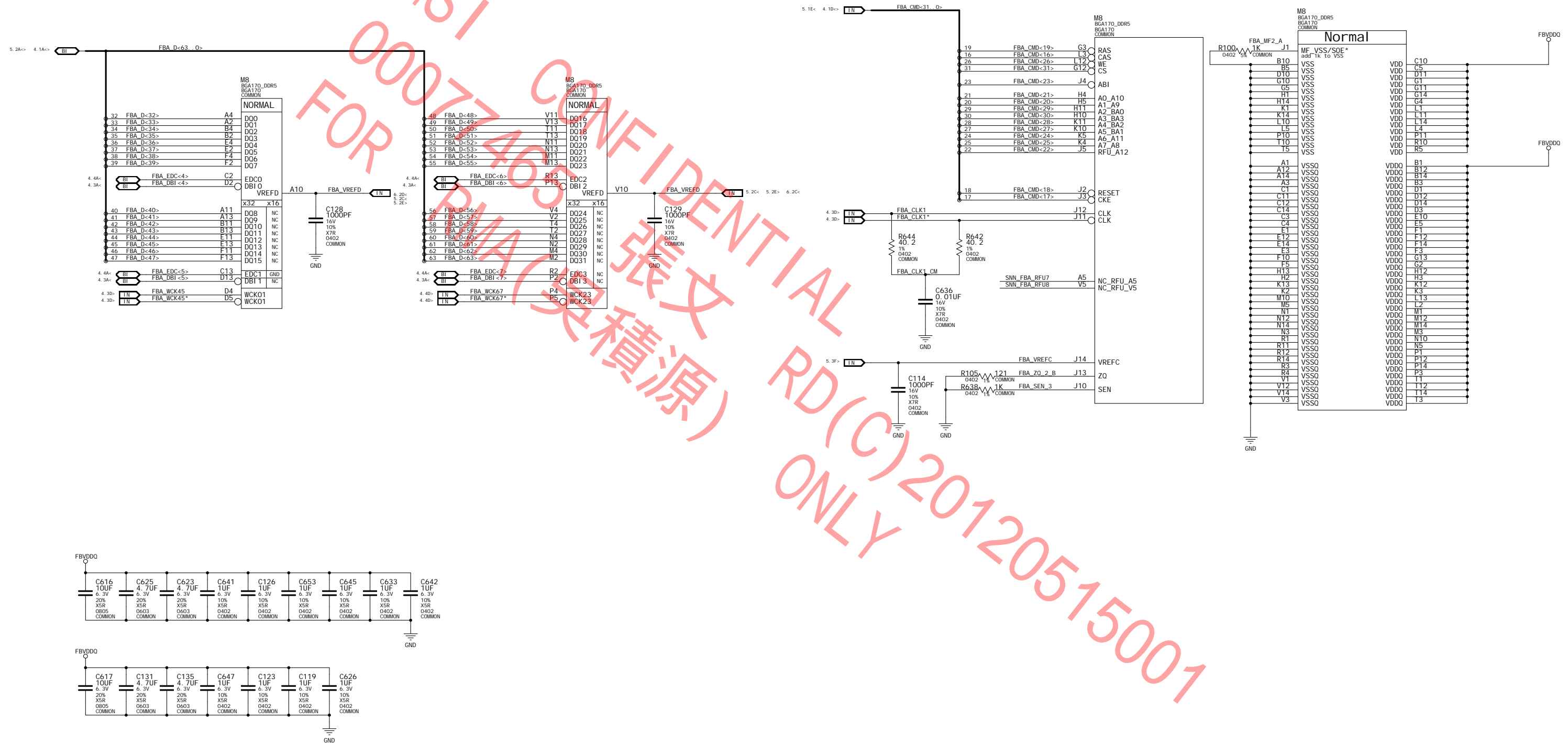
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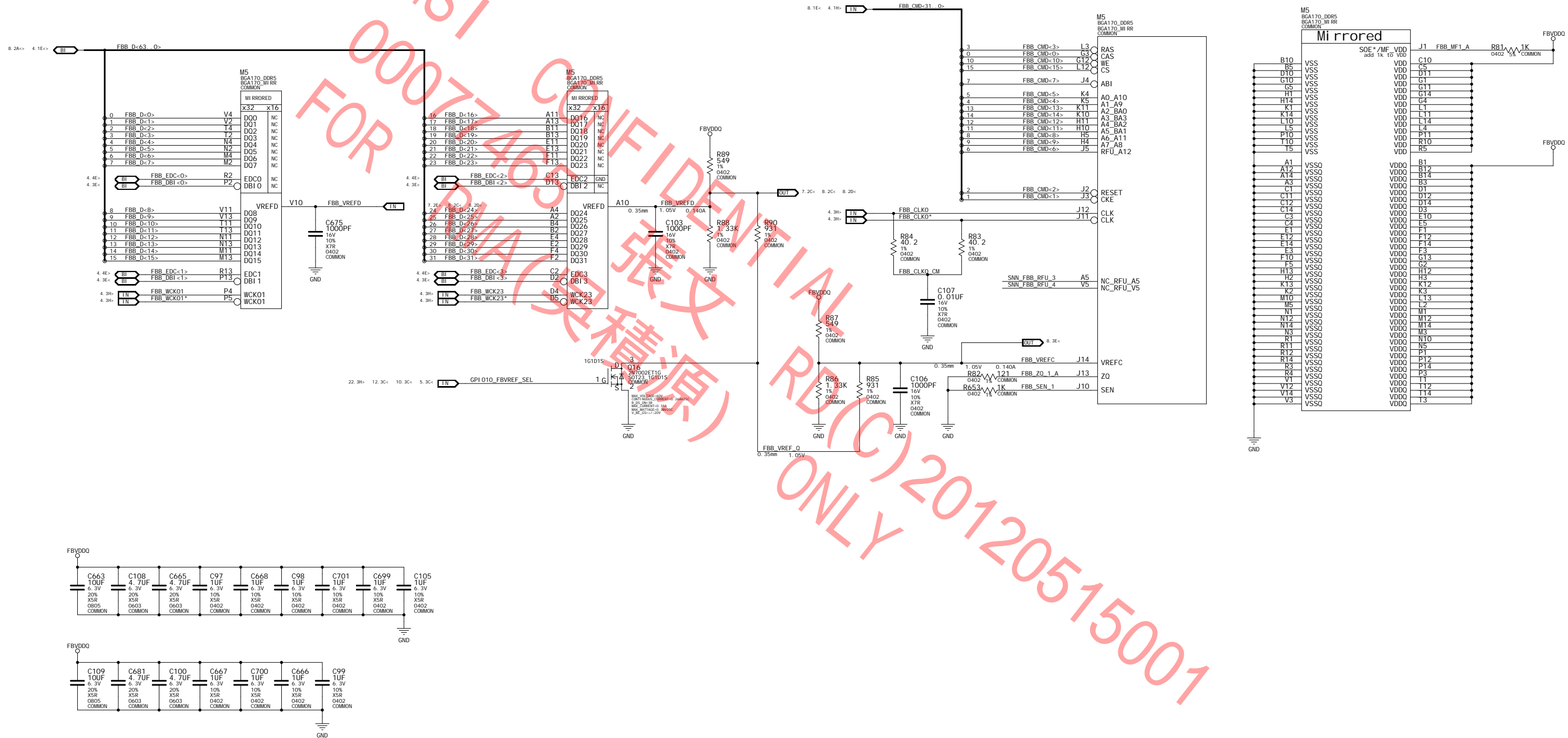
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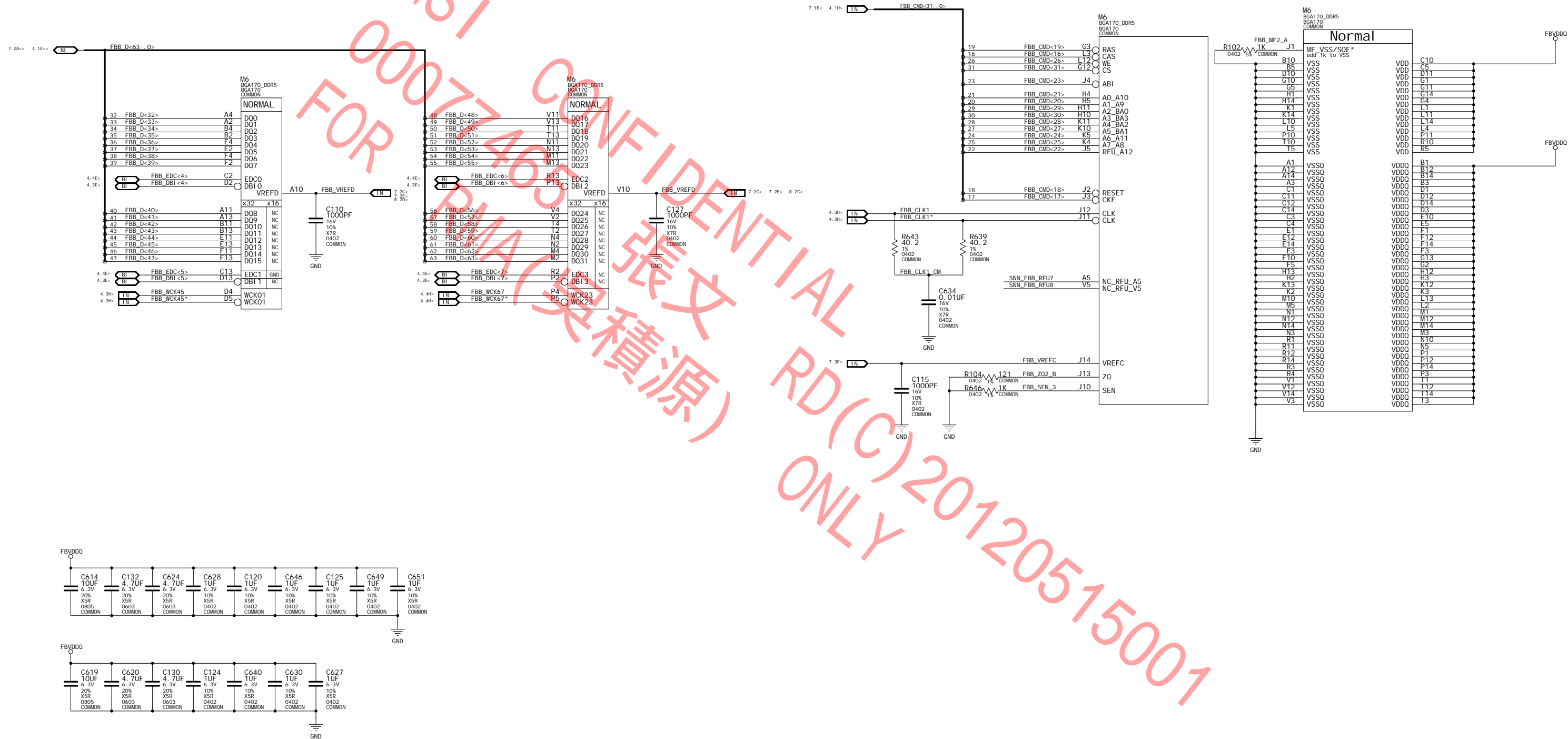




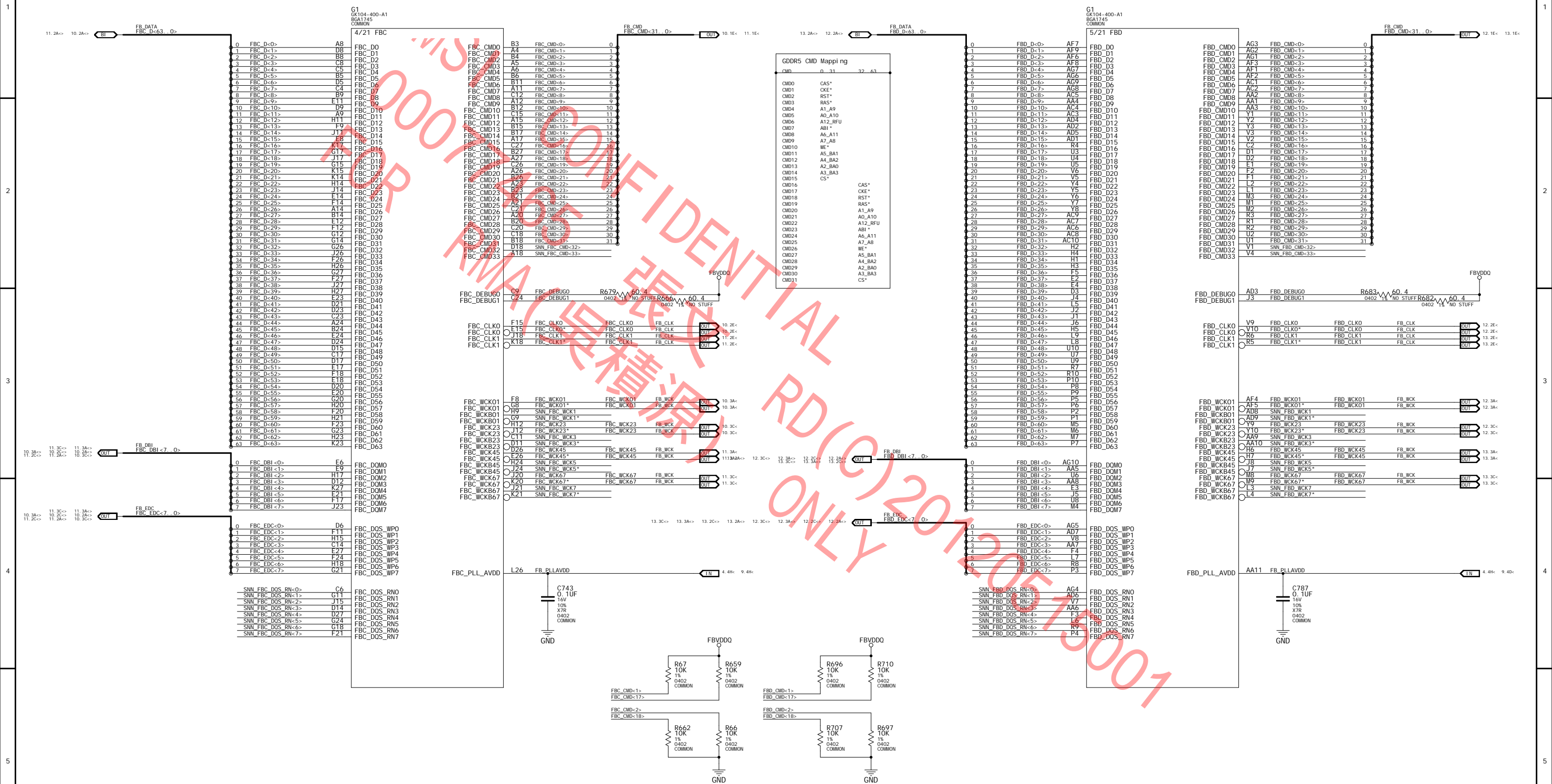


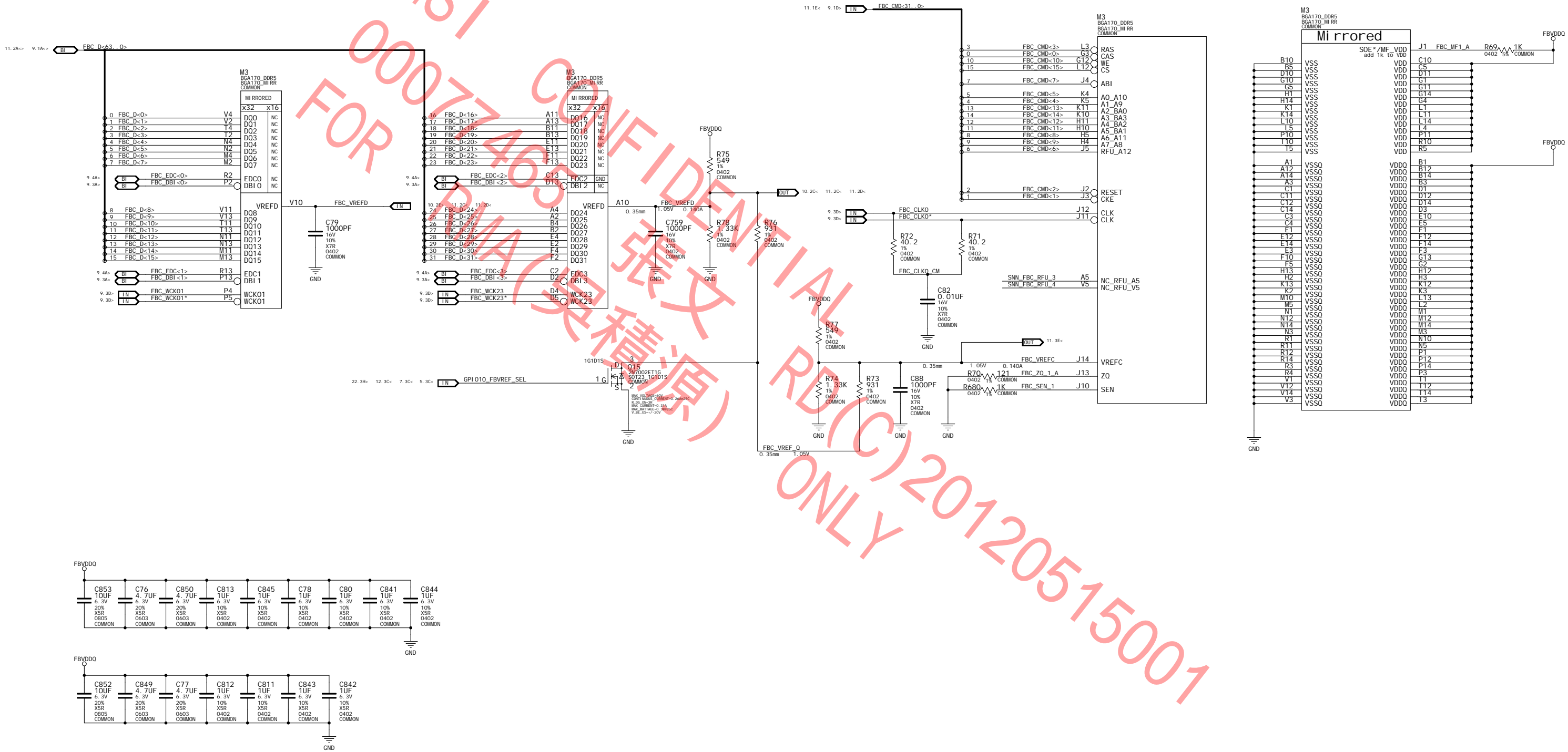
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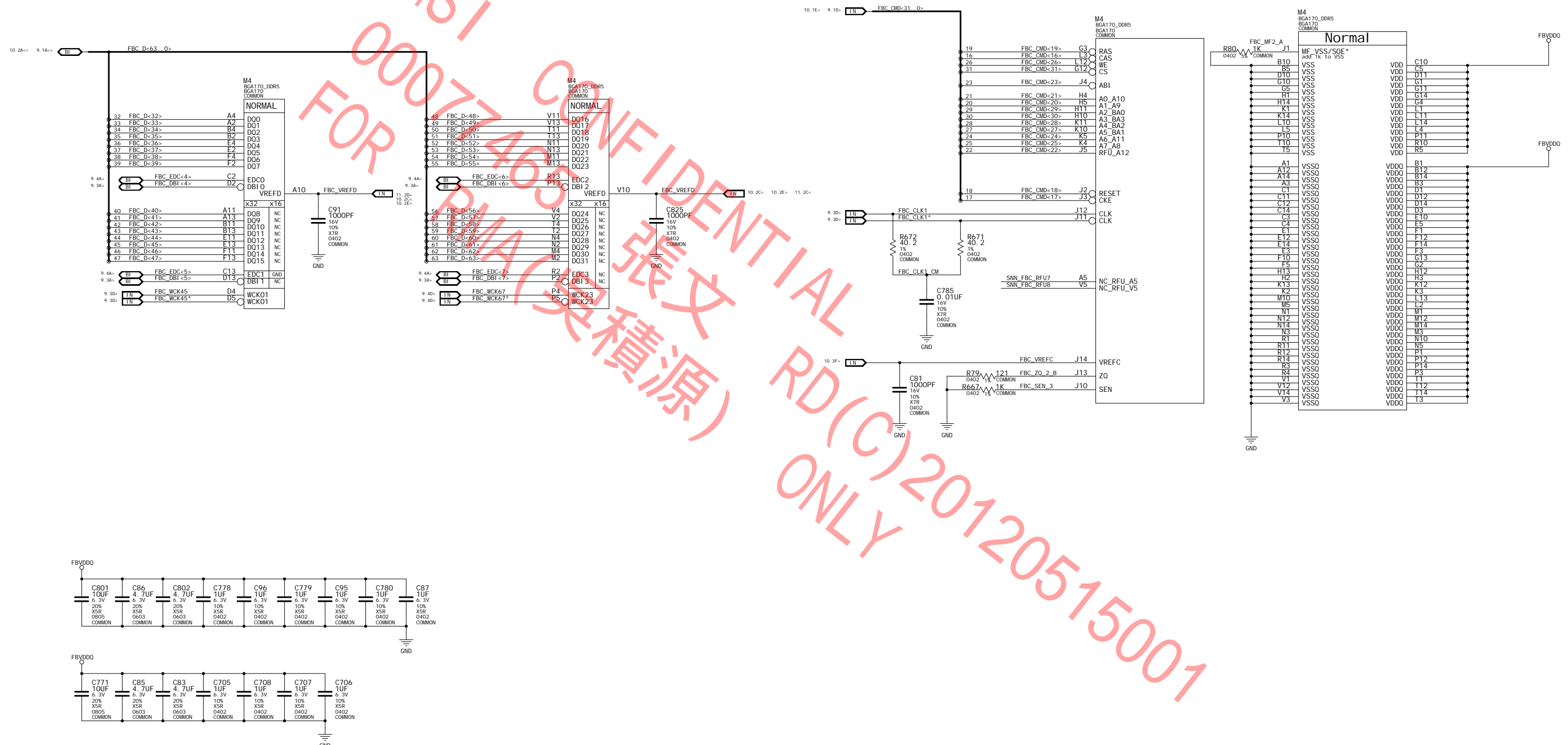






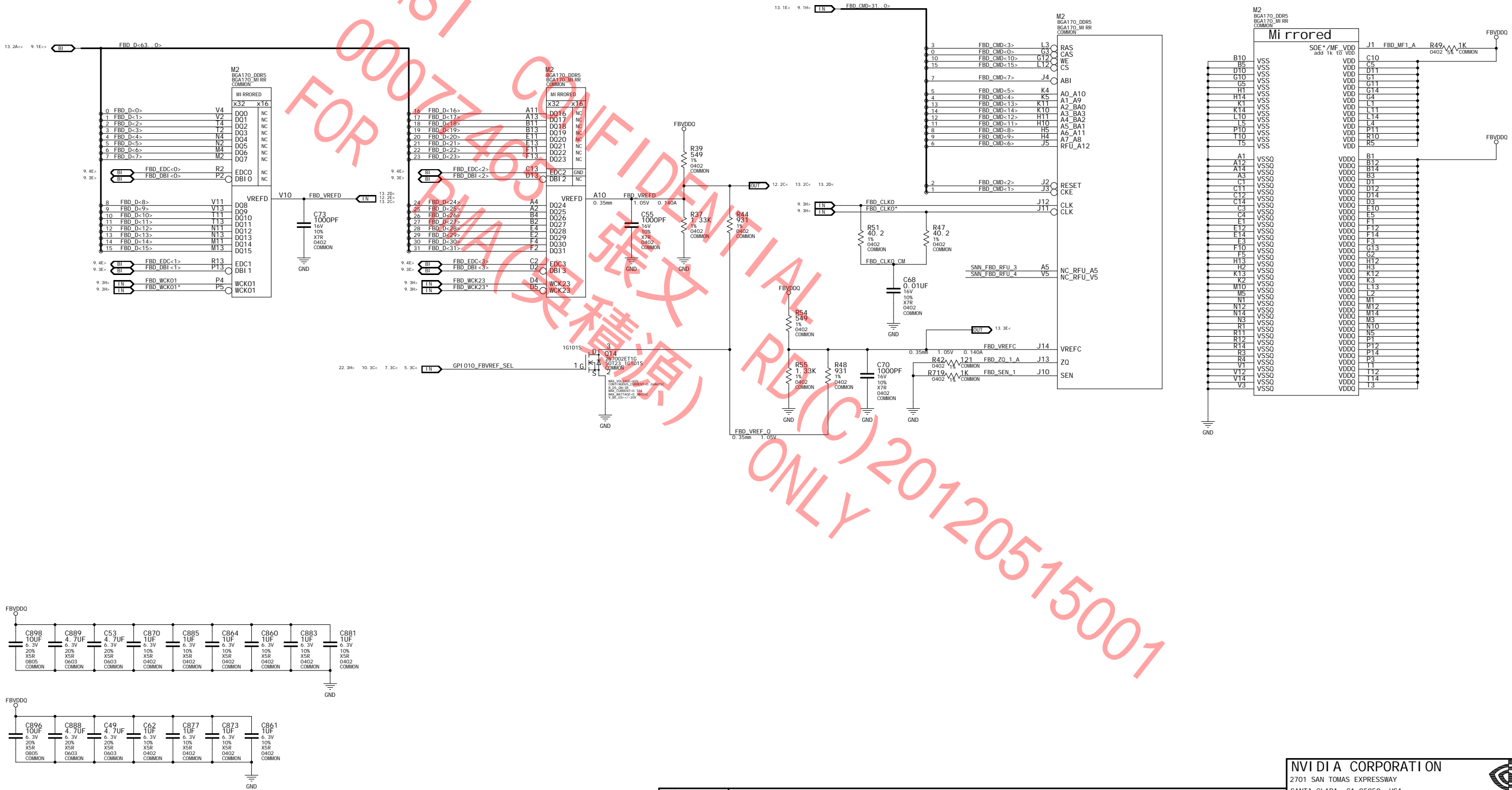


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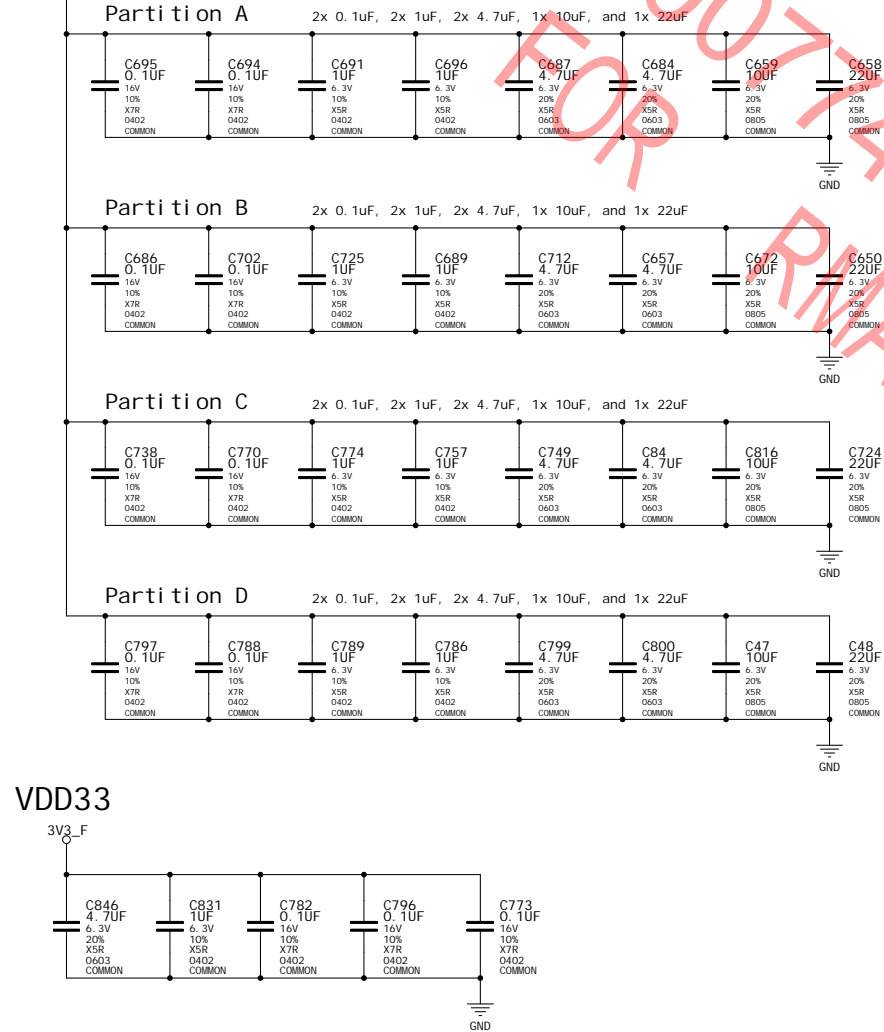




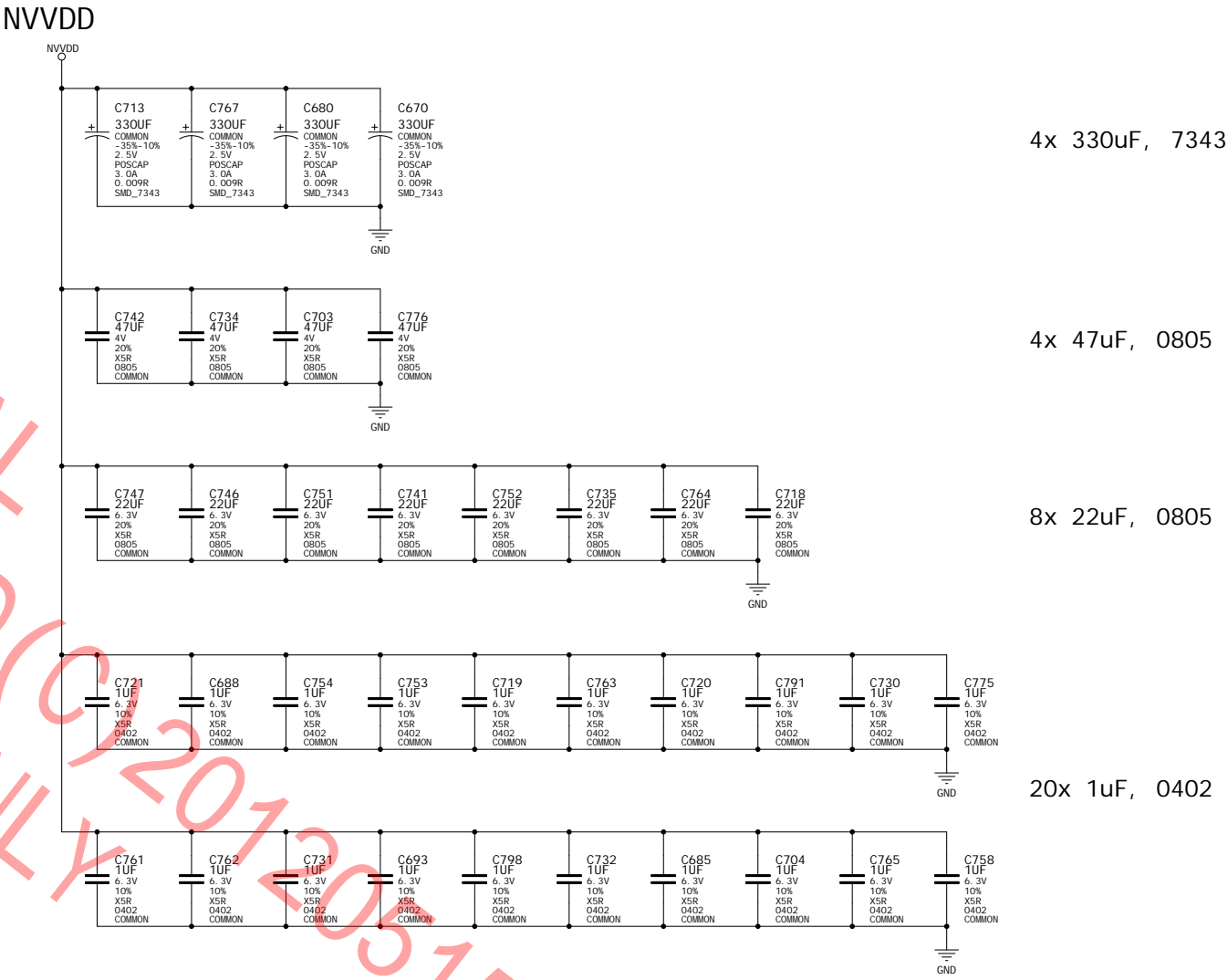


Based on GB2-X GDDR5 FBVDDQ Decap Guidel ine

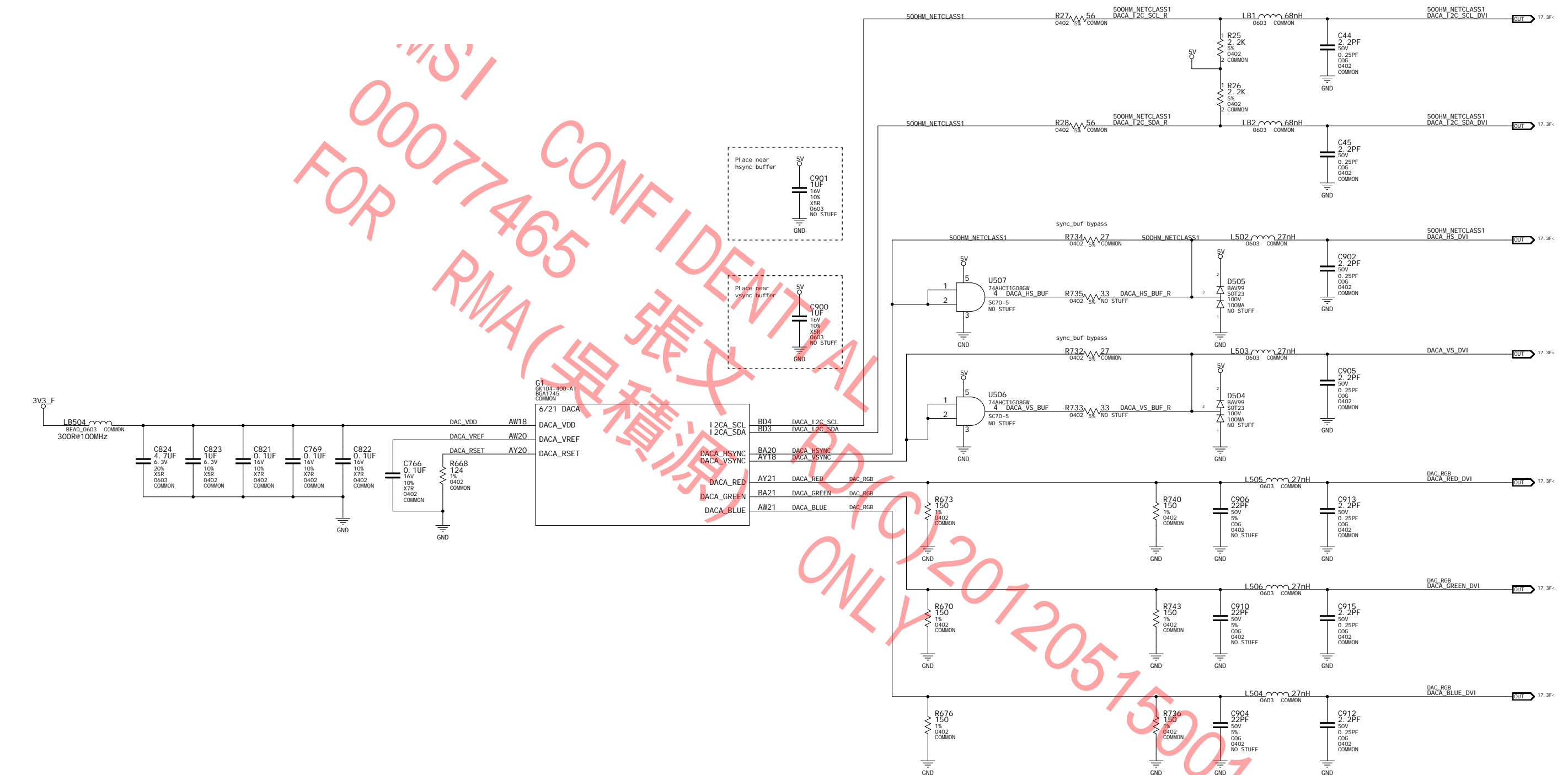
FBVDDQ 0.1uF, 0.47uF & 1uF, 0402 (Pl ace Under GPU)  
4.7uF, 0603 (Pl ace Near GPU)  
10uF, 0805 (Pl ace Near GPU)  
22uF, 0805 (Pl ace Near GPU)



NVVDD Decoupl ing caps. Pl ace under GPU.




## Page16: DACA Interface



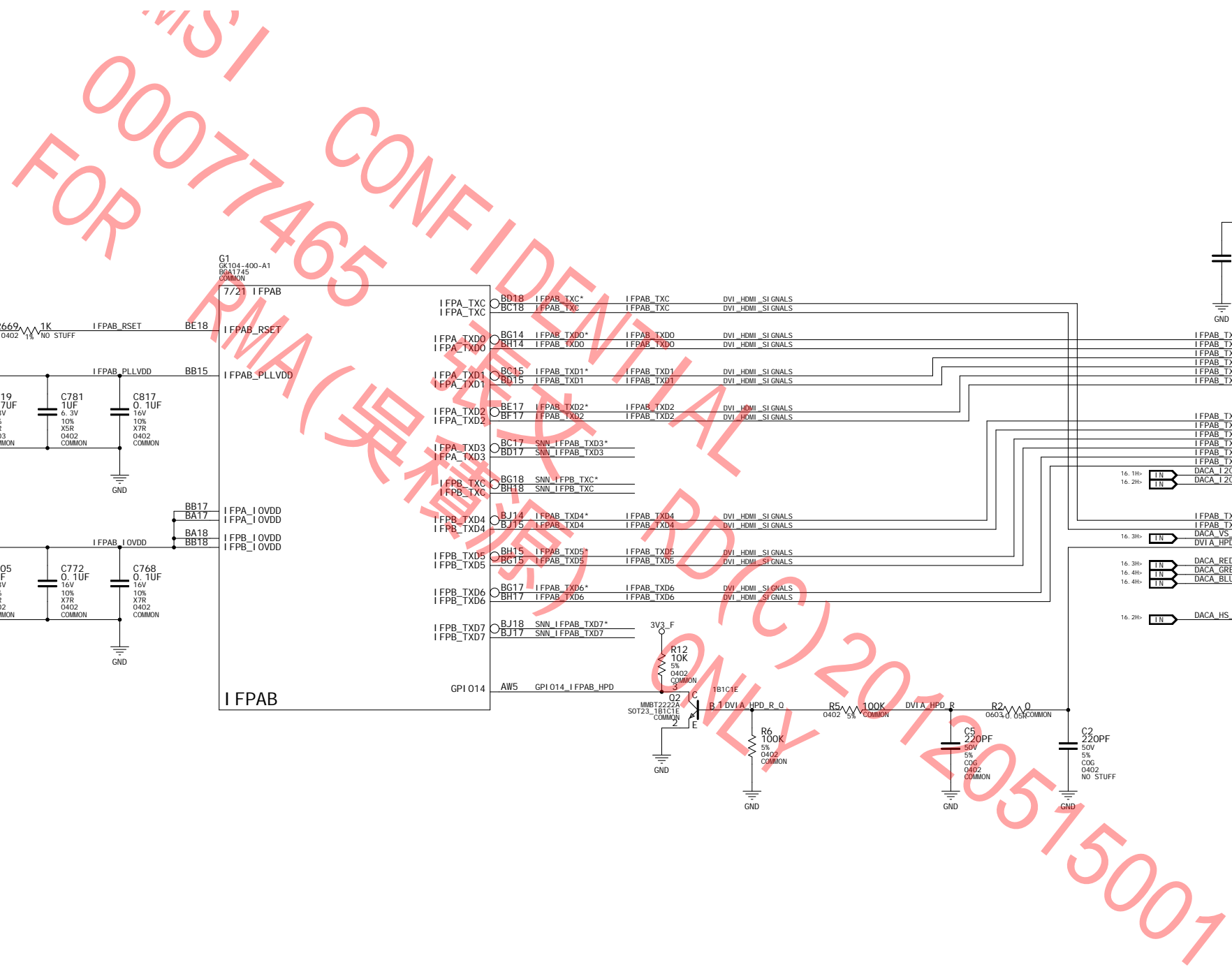
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DAC_VDD	3.3V	0.25A	16MIL

ASSEMBLY	SKU0000 GK104 256b 64Mx32 2GB
PAGE DETAIL	DACA Interface

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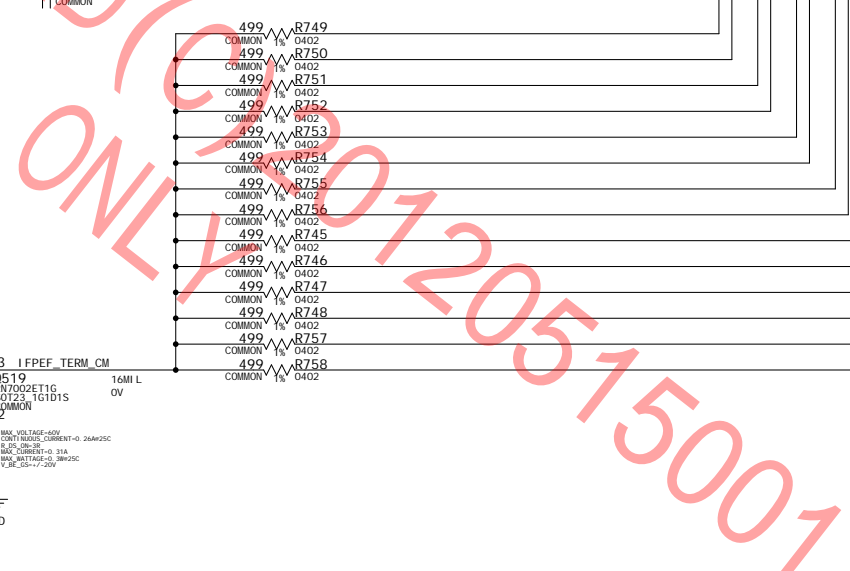
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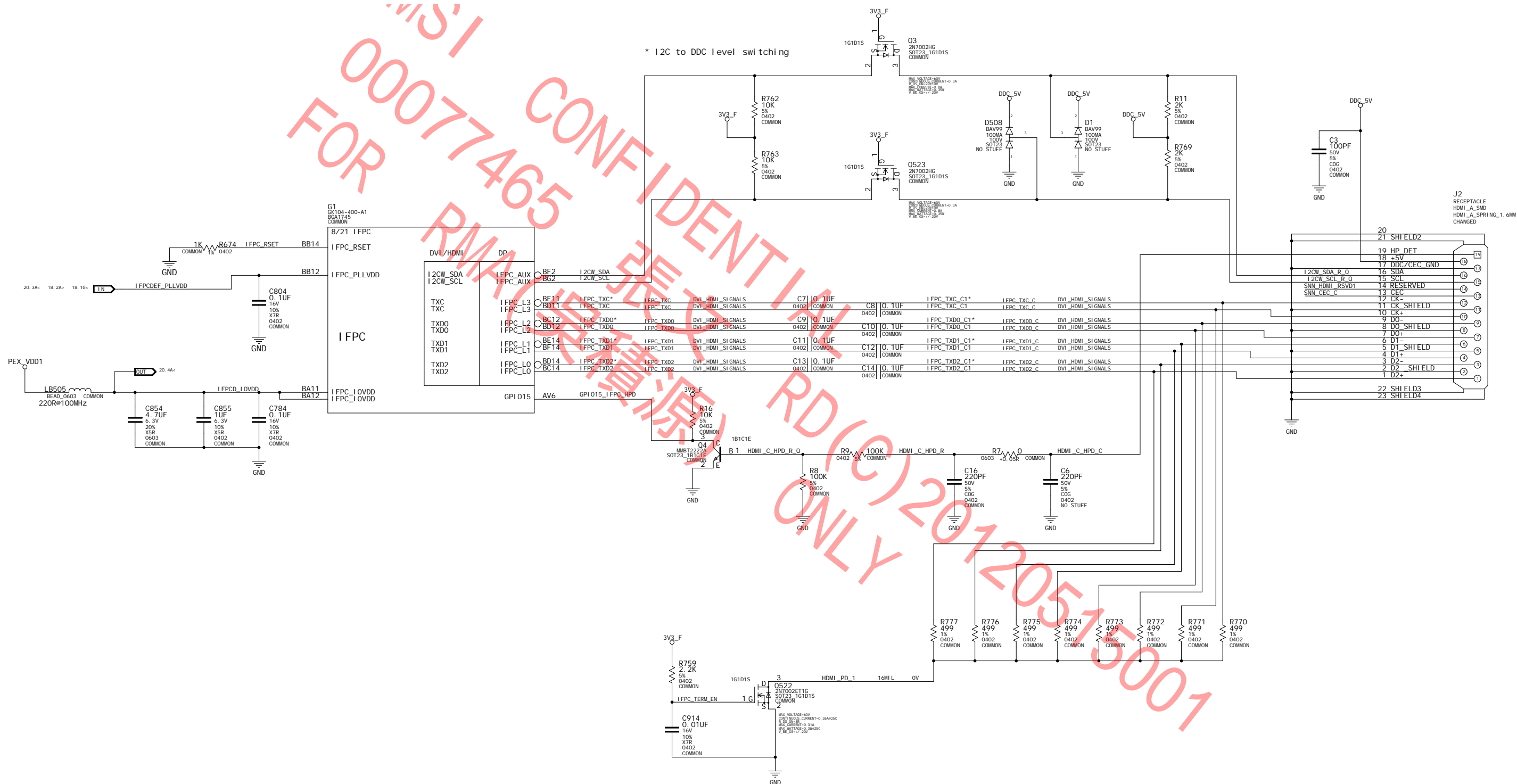




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ASSEMBLY	SKU0000 GK104 256b 64Mx32 2GB
PAGE DETAIL L	1FPC HDMI

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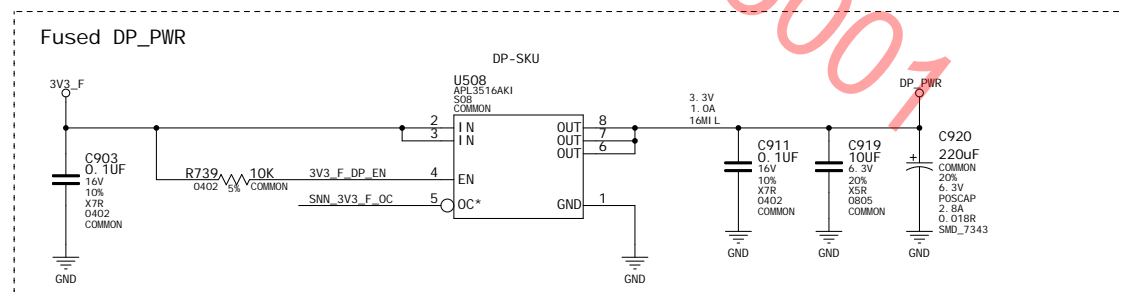
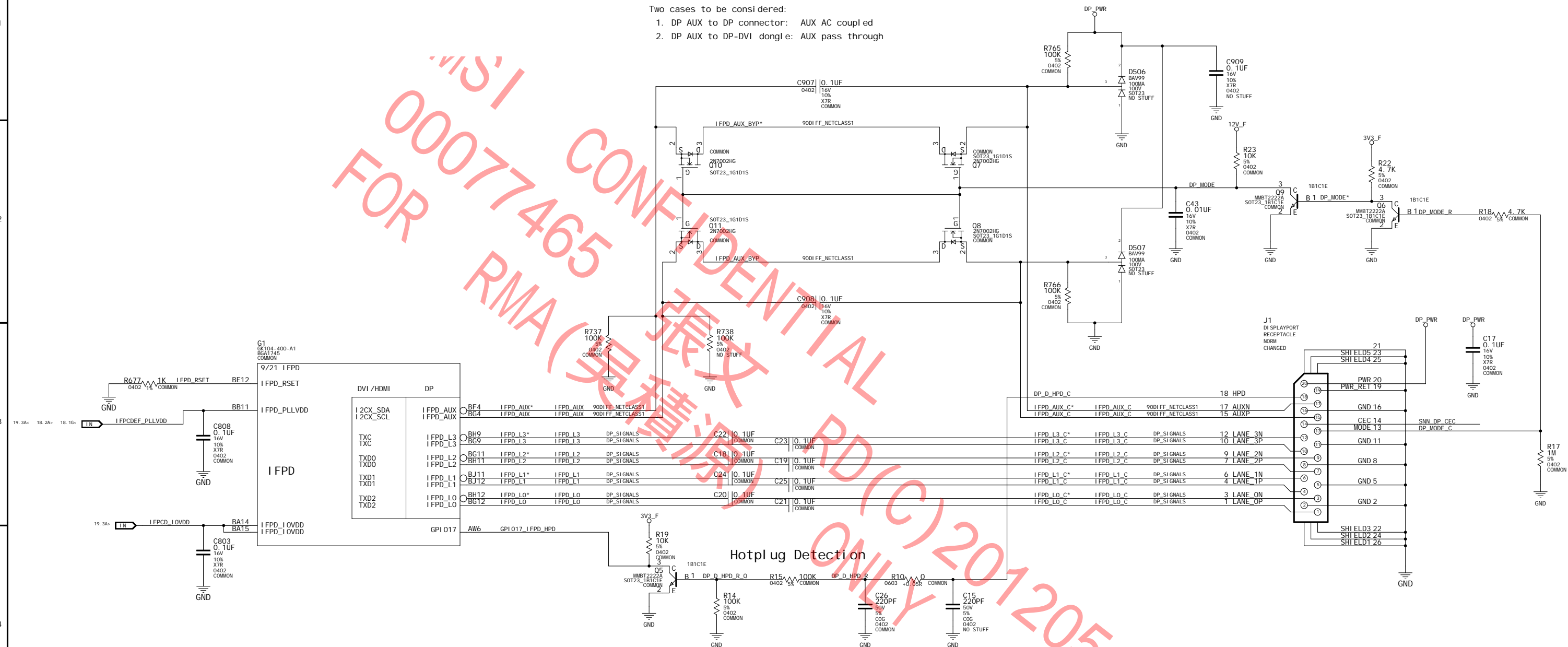



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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

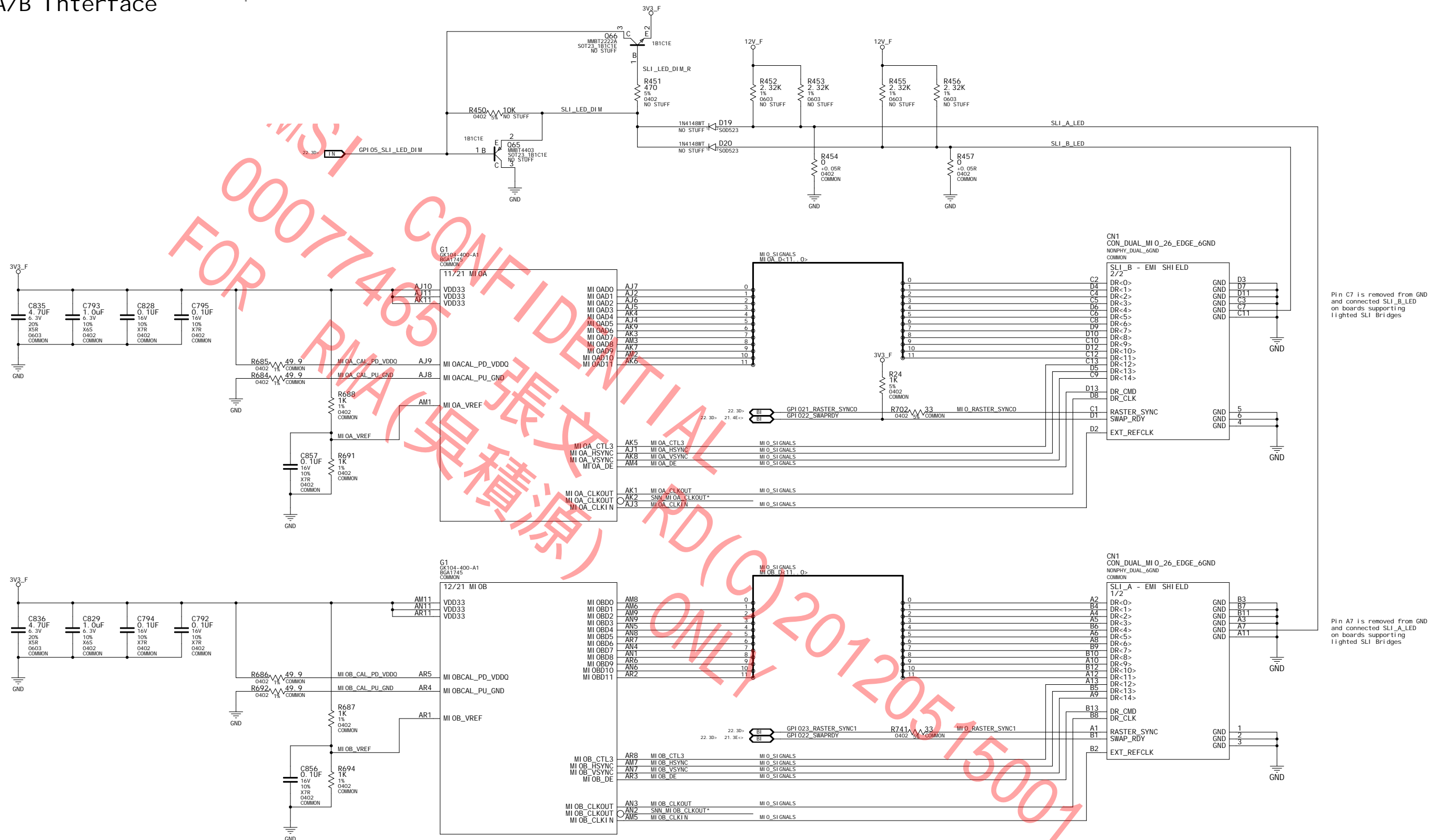


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## Page21: MI 0A/B Interface



	NET	VOLTAGE	MAX_CURRENT	MIN_WI_DTH
J1N	MI_O_VDDO	2.5V	0.80A	16MIL
J1N	MI_OA_VREF	1.65V		12MIL
J1N	MI_OA_CAL_PD_VDDQ	2.5V		12MIL
J1N	MI_OA_CAL_PU_GND	0.0V		12MIL

1N	MI OB_VREF	1.65V	12MI L
1N	MI OB_CAL_PD_VDDQ	3.3V	12MI L
1N	MI OB_CAL_PU_GND	0.0V	12MI L

ASSEMBLY	SKU0000 GK104 256b 64Mx32 2GB
PAGE DETAIL	MI0A/B Interface

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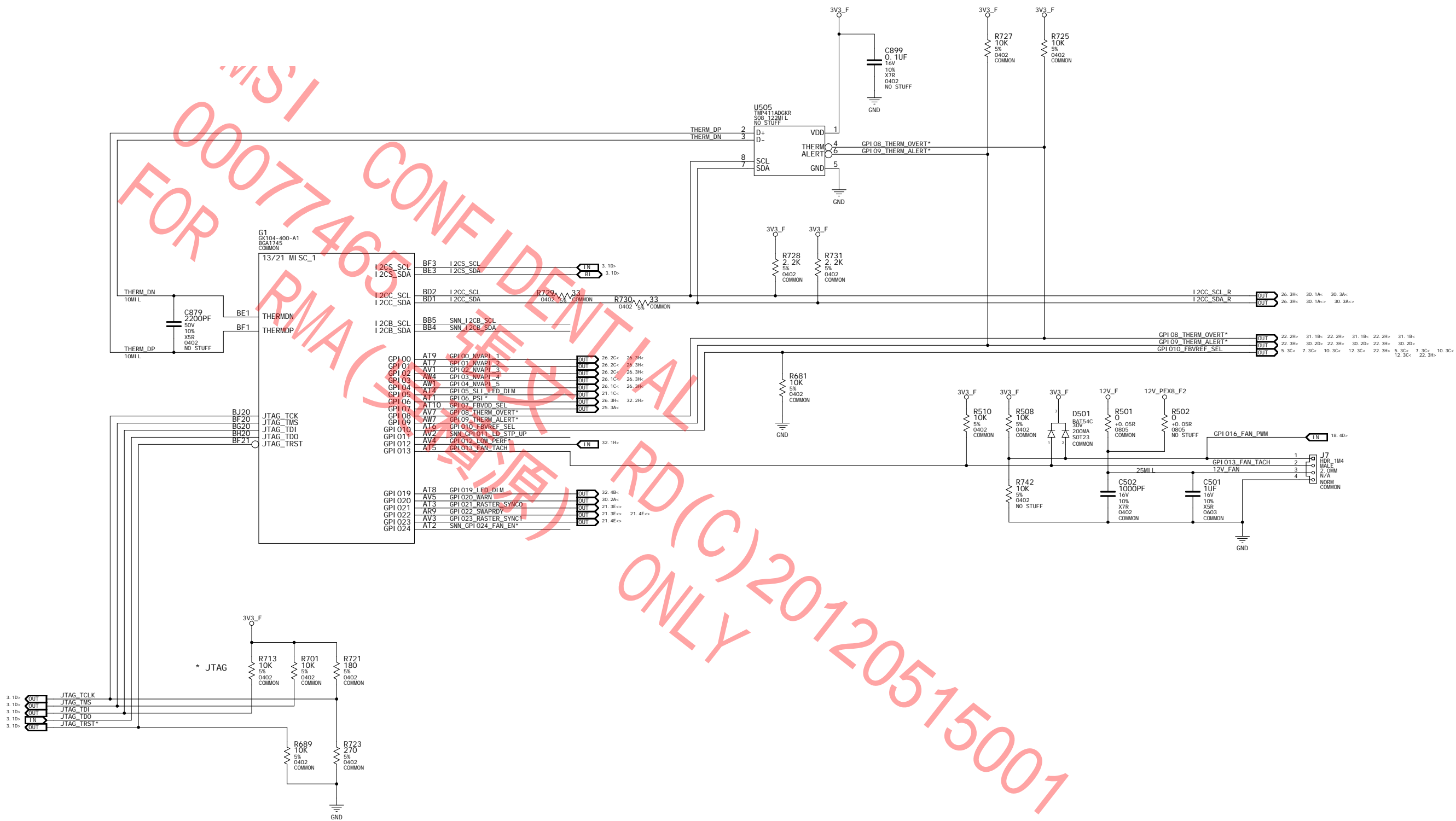
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Page23: MI SC2: ROM, XTAL, Straps

STRAPO	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0000 - (0x1180)*	5K PD -400 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		
ROM_SI	RAMCFG[0]*	0*	
	RAMCFG[1]*	1*	35K PD* 0110 for 64Mx32 256-bit Hynix for SKU 0 primary memory
	RAMCFG[2]*	1*	
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	10K PU*
	FB[0]_APERTURE_SIZE*	0* For 256MB*	
	FB[1]_APERTURE_SIZE*	1* For 256MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0* DISABLED*	
	PCI_DEVID_EXT[5]*	0* For 0x1180*	25K PD*
	SUB_VENDOR*	1* Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0* For 0x1180*	

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit Elpi da	
0010	32Mx32 256-bit Hyni x	
0011	32Mx32 256-bit Samsung	
0100	Reserved	
0101	64Mx32 256-bit Elpi da	
0110	64Mx32 256-bit Hyni x	
0111	64Mx32 256-bit Samsung	
1000	Reserved	
1001	32Mx32 192-bit Elpi da	
1010	32Mx32 192-bit Hyni x	
1011	32Mx32 192-bit Samsung	
1100	Reserved	
1101	64Mx32 192-bit Elpi da	
1110	64Mx32 192-bit Hyni x	
1111	64Mx32 192-bit Samsung	

	MULTI_STRAP_REFO_GND
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2K 1% TO GND

Smart Fan		
XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

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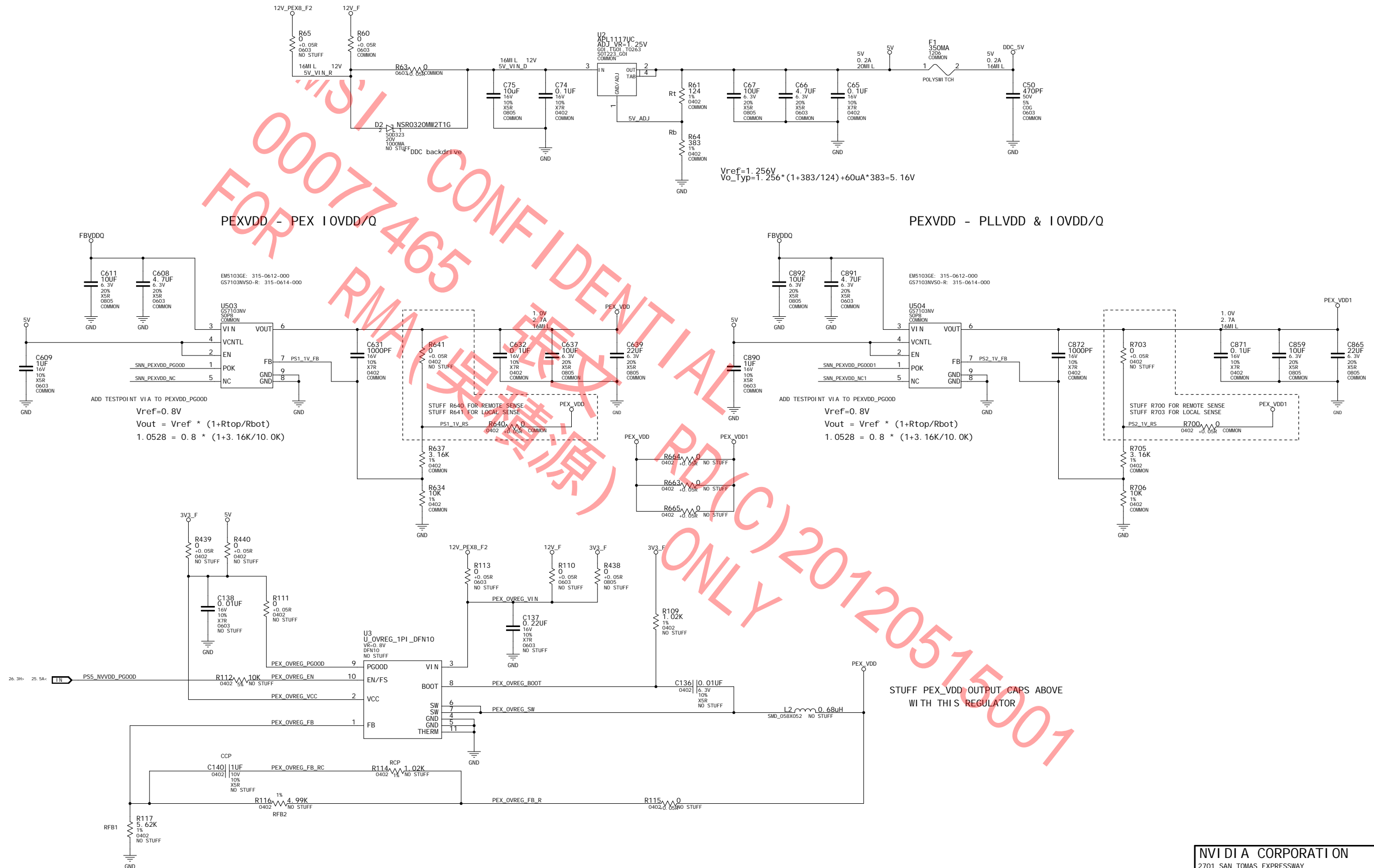
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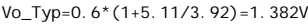
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PAGE DETAIL	PS: FBVDD/Q

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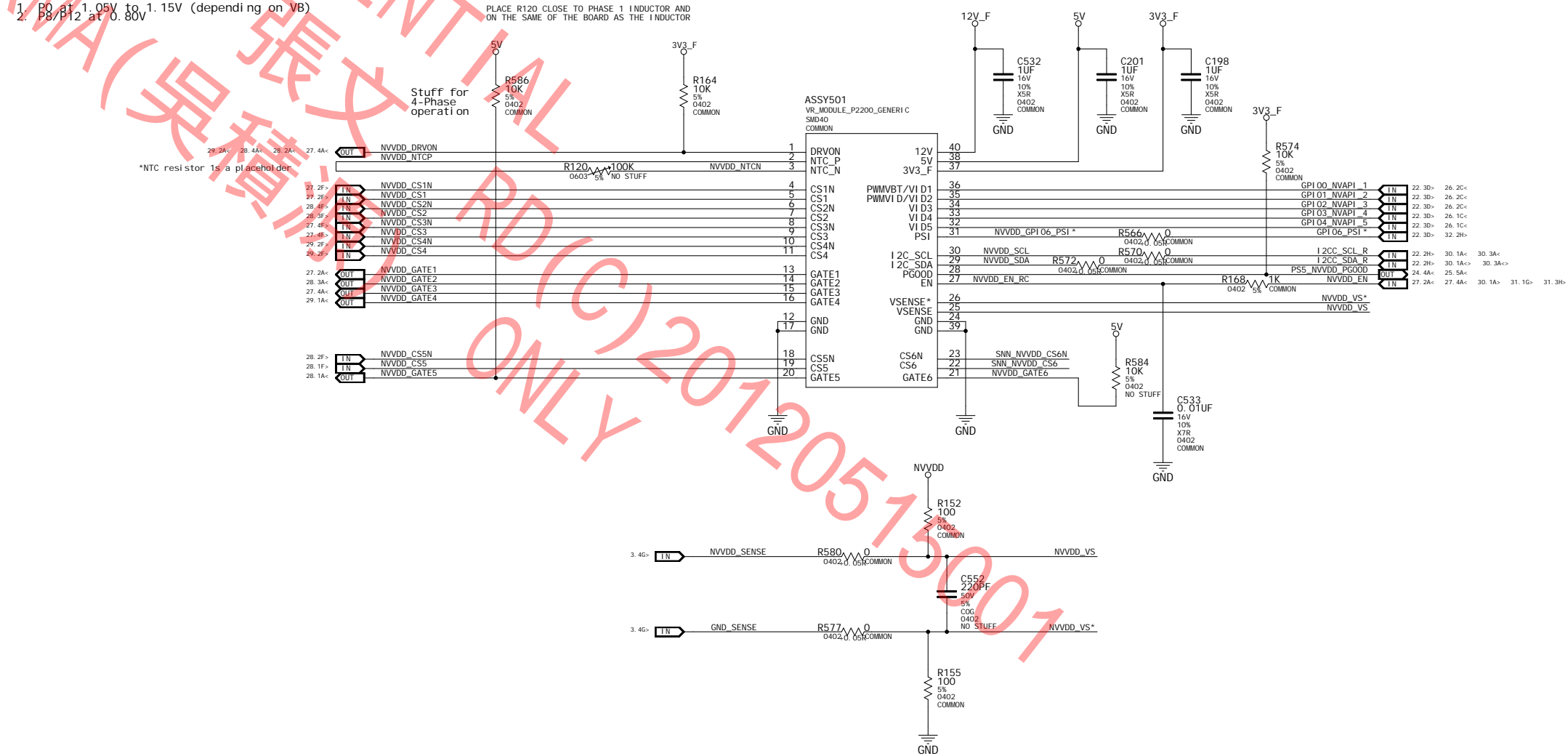
VID Table						
GPI 07	GPI 06	GPI 05	GPI 02	GPI 017	VOUT	
VID_5	VID_4	VID_3	VID_2	VID_1		
0	0	0	0	0	1.2125V	
0	0	0	0	1	1.2000V	
0	0	0	1	0	1.1875V	
0	0	0	1	1	1.1750V	
0	0	1	0	0	1.1625V	
0	0	1	0	1	1.1500V	
0	0	1	1	0	1.1375V	
0	0	1	1	1	1.1250V	
0	1	0	0	0	1.1125V	
0	1	0	0	1	1.1000V	
0	1	0	1	0	1.0875V	
0	1	0	1	1	1.0750V	
0	1	1	0	0	1.0625V	
0	1	1	0	1	1.0500V	
0	1	1	1	0	1.0375V	
0	1	1	1	1	1.0250V	
1	0	0	0	0	1.0125V	
1	0	0	0	1	1.0000V	
1	0	0	1	0	0.9875V	
1	0	0	1	1	0.9750V	
1	0	1	0	0	0.9625V	
1	0	1	0	1	0.9500V	
1	0	1	1	0	0.9375V	
1	0	1	1	1	0.9250V	
1	1	0	0	0	0.9125V	
1	1	0	0	1	0.9000V	
1	1	0	1	0	0.8875V	
1	1	0	1	1	0.8750V	
1	1	1	0	0	0.8625V	
1	1	1	0	1	0.8500V	
1	1	1	1	0	0.8375V	
1	1	1	1	1	0.8250V	

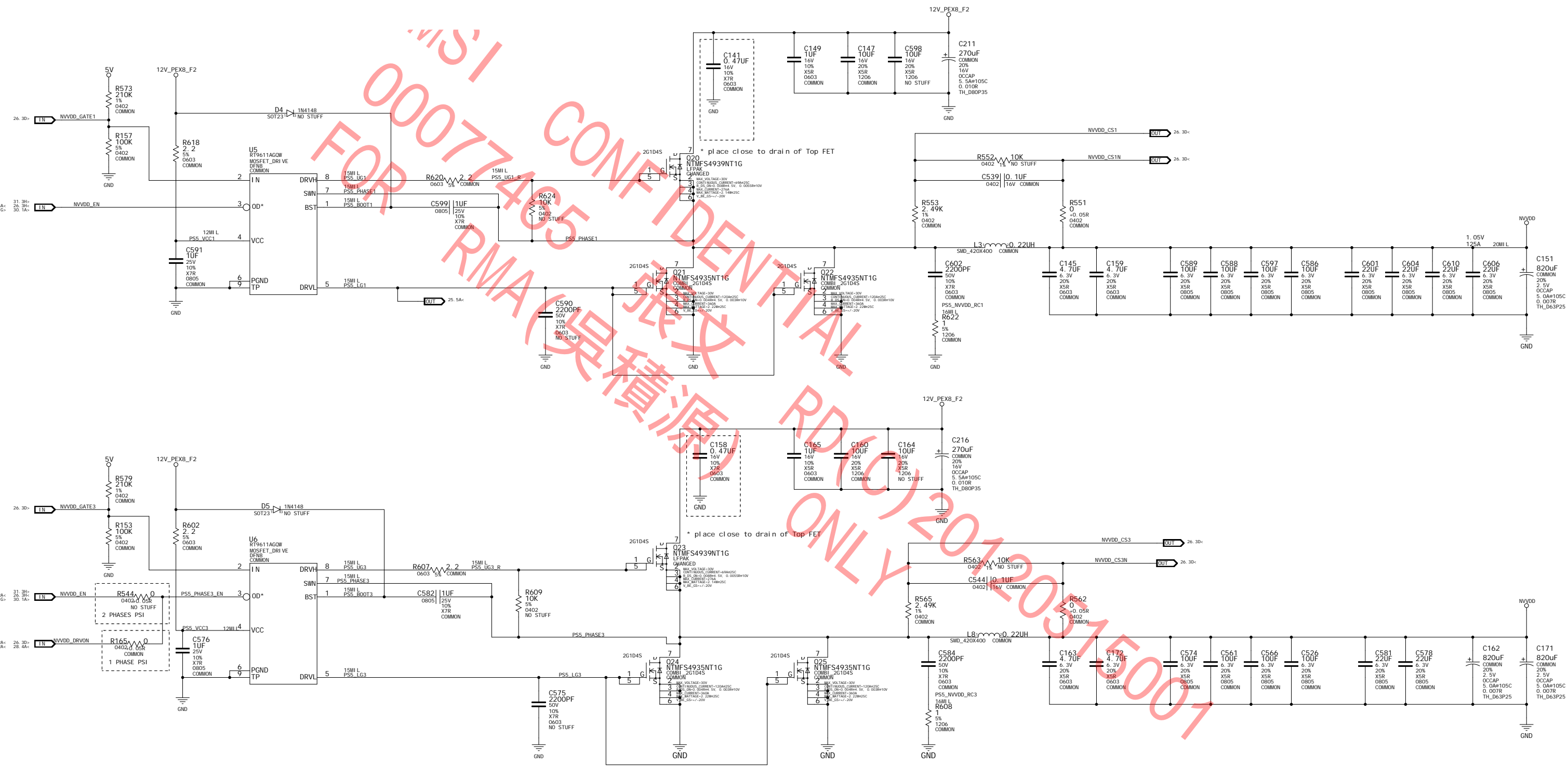
SOFT START (VR11)

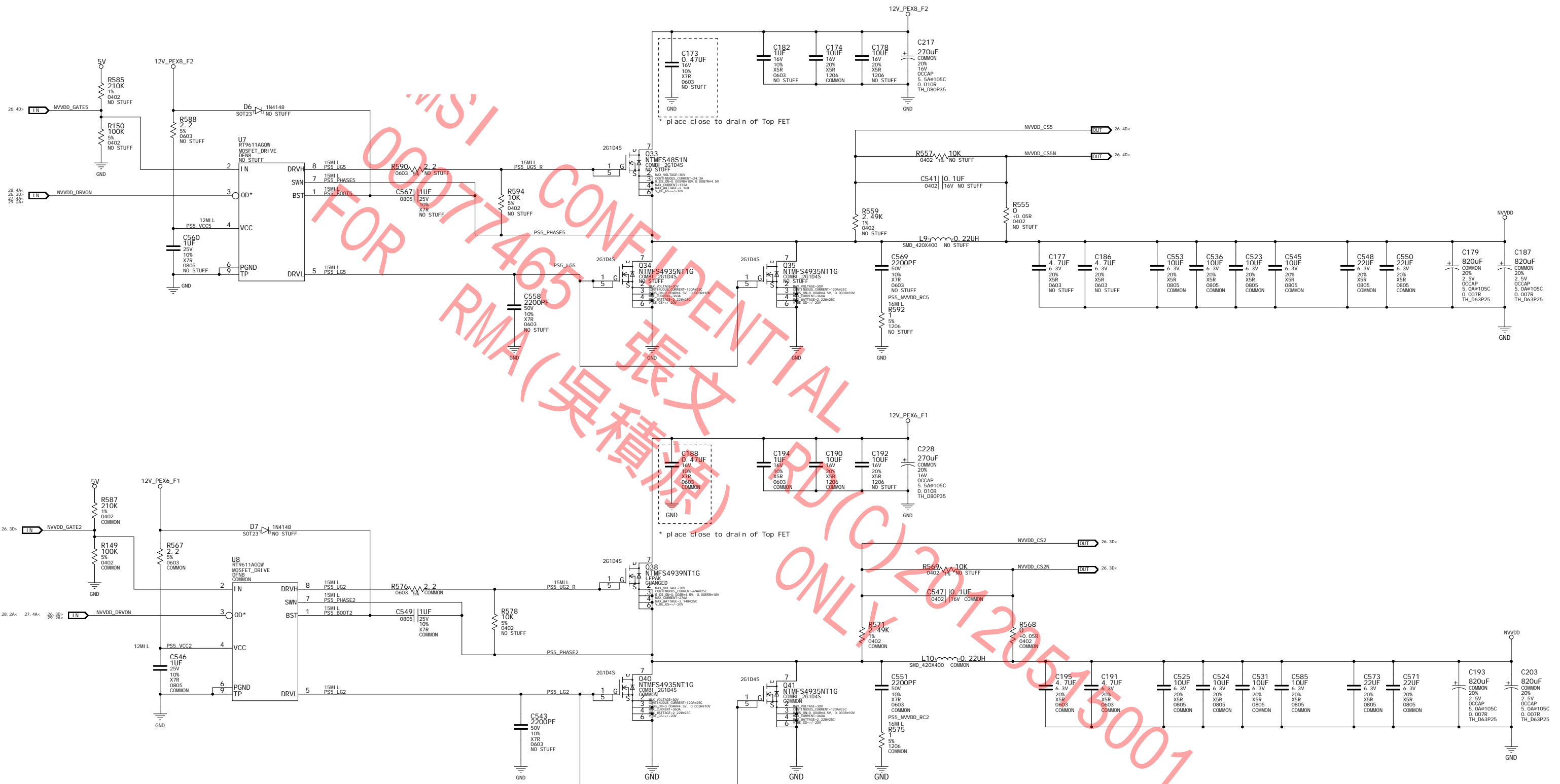
1. Ramp 0V to 1.10V in ~2ms
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPI0 tri-state  
VID[5:1]=11000 to set 0.9125V

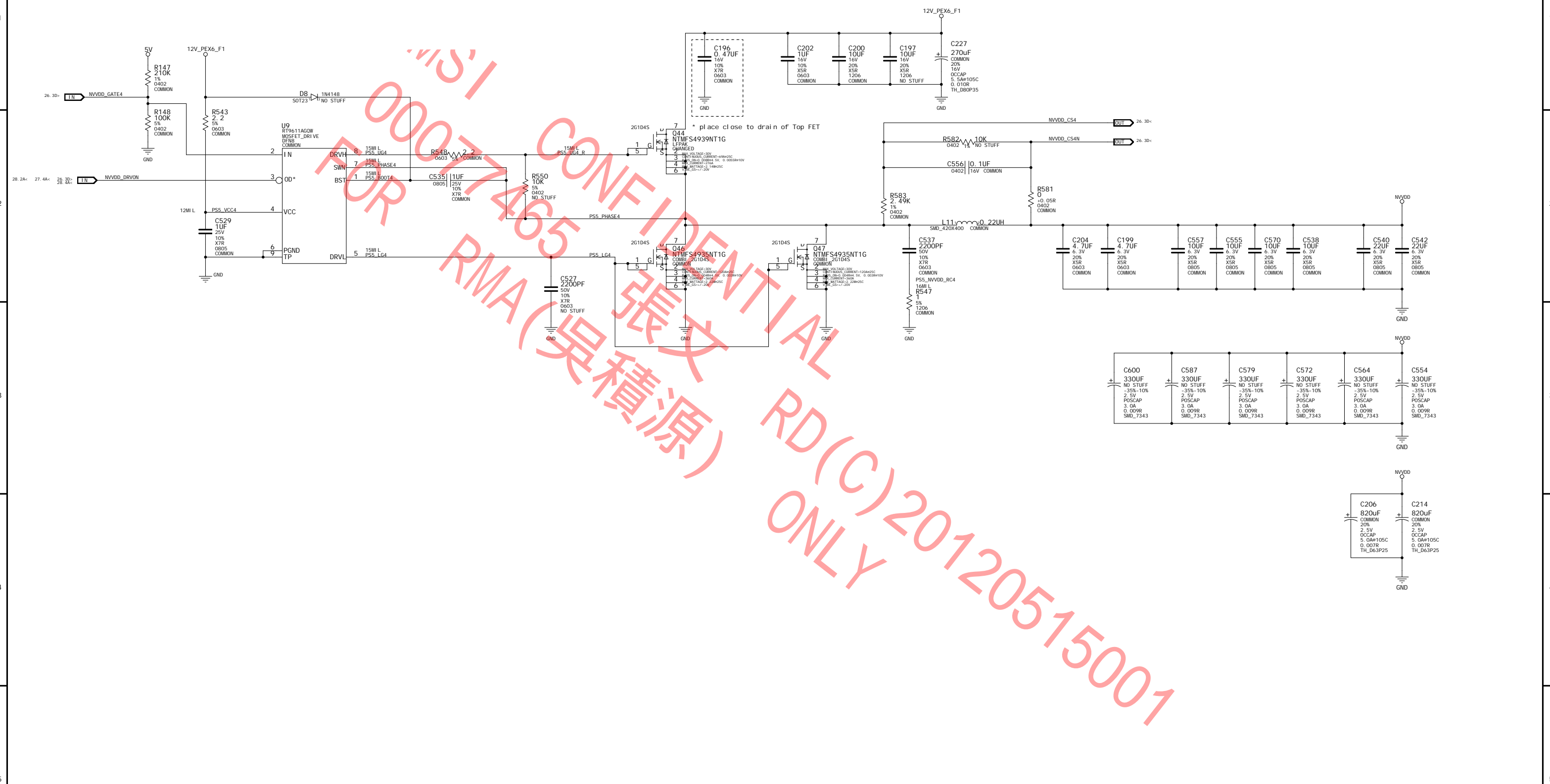
P-STATE VOLTAGES

1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V



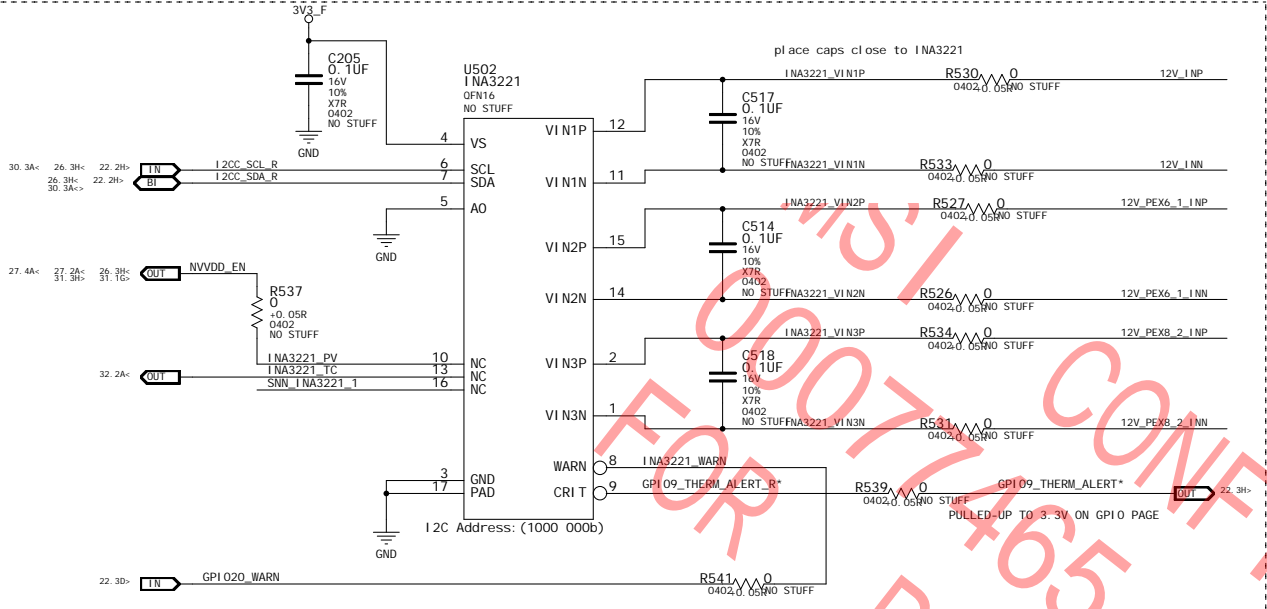




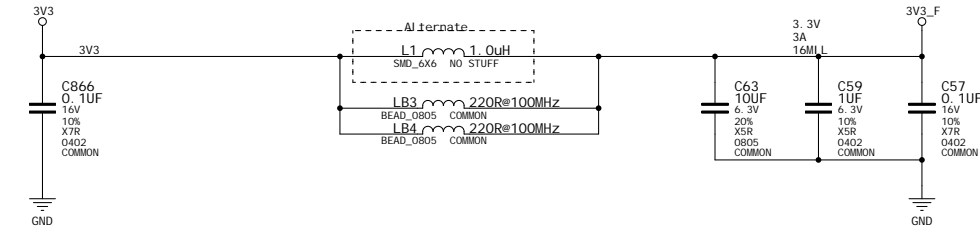




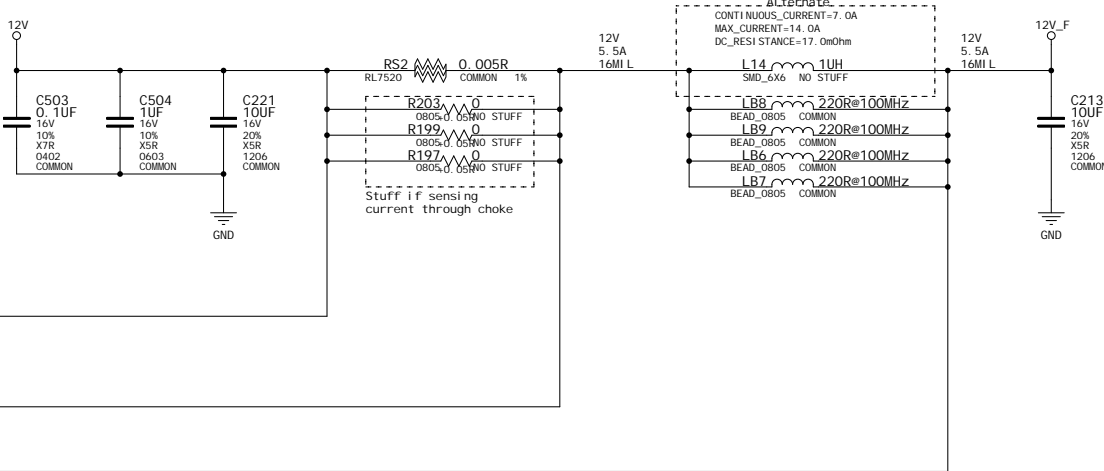
Page30: PS: Inputs, Filtering, and Monitoring



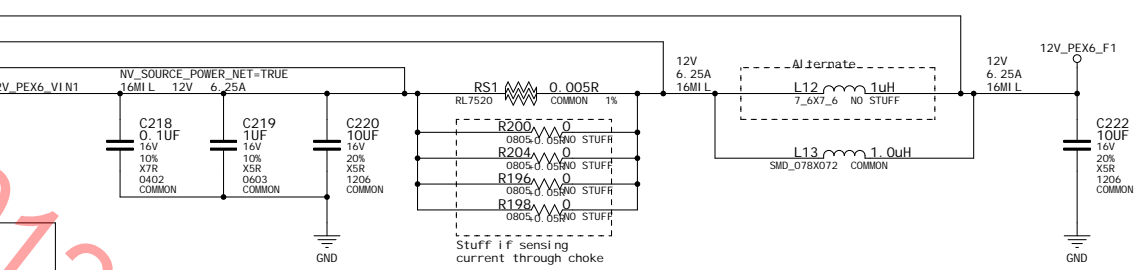
PEX 3V3 INPUT - 10W



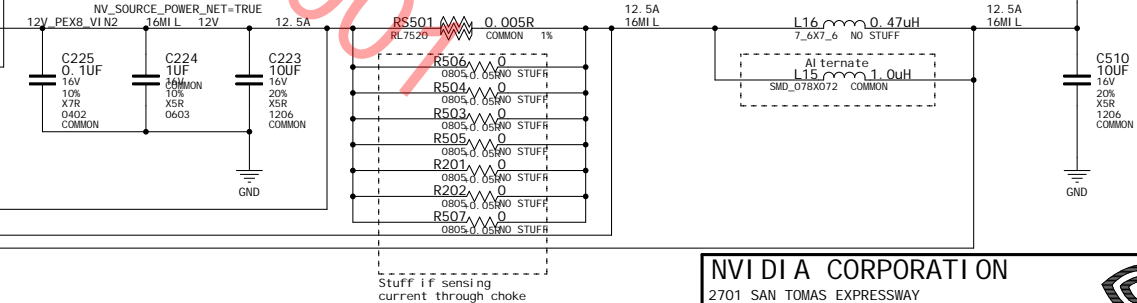
PEX\_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



Stacked Connector

J6  
6-pin PEX/8-pin PEX  
6-pin PEX/6-pin PEX

See BOM to determine which connector is stuffed

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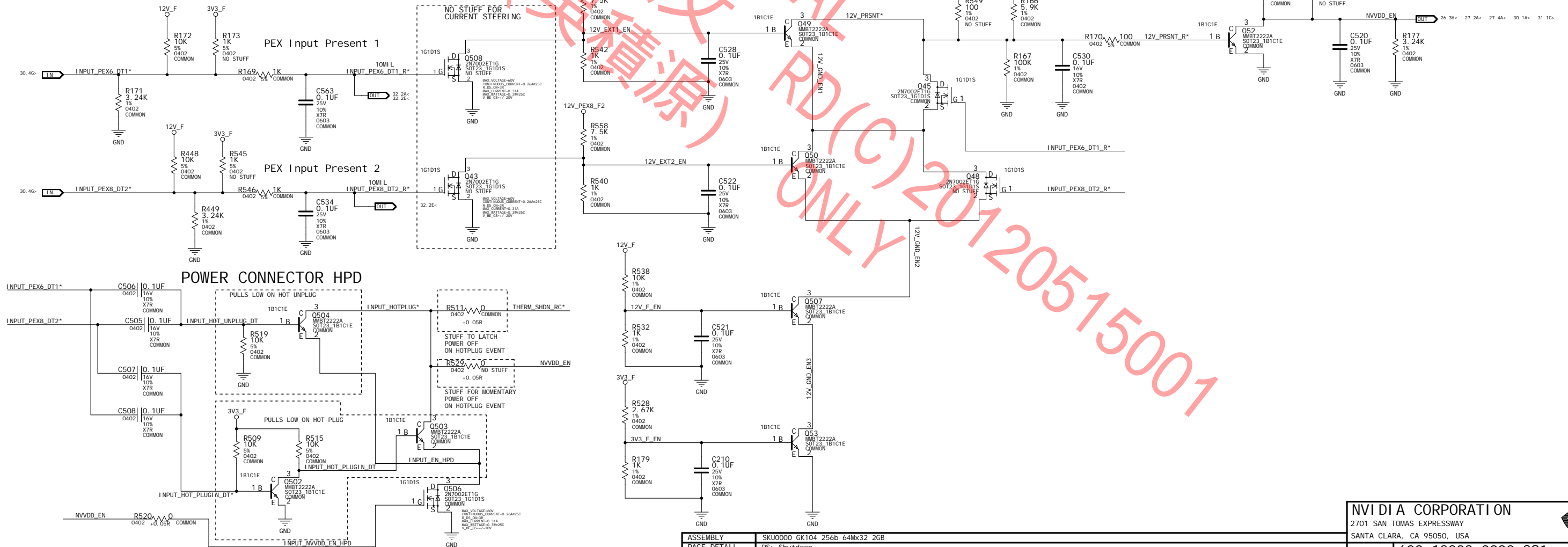
NV\_PN 600-12002-0000-QS1

PCB REV	P2002-A03	PAGE	30 OF 33
BOM REV	A	DATE	07-FEB-2012

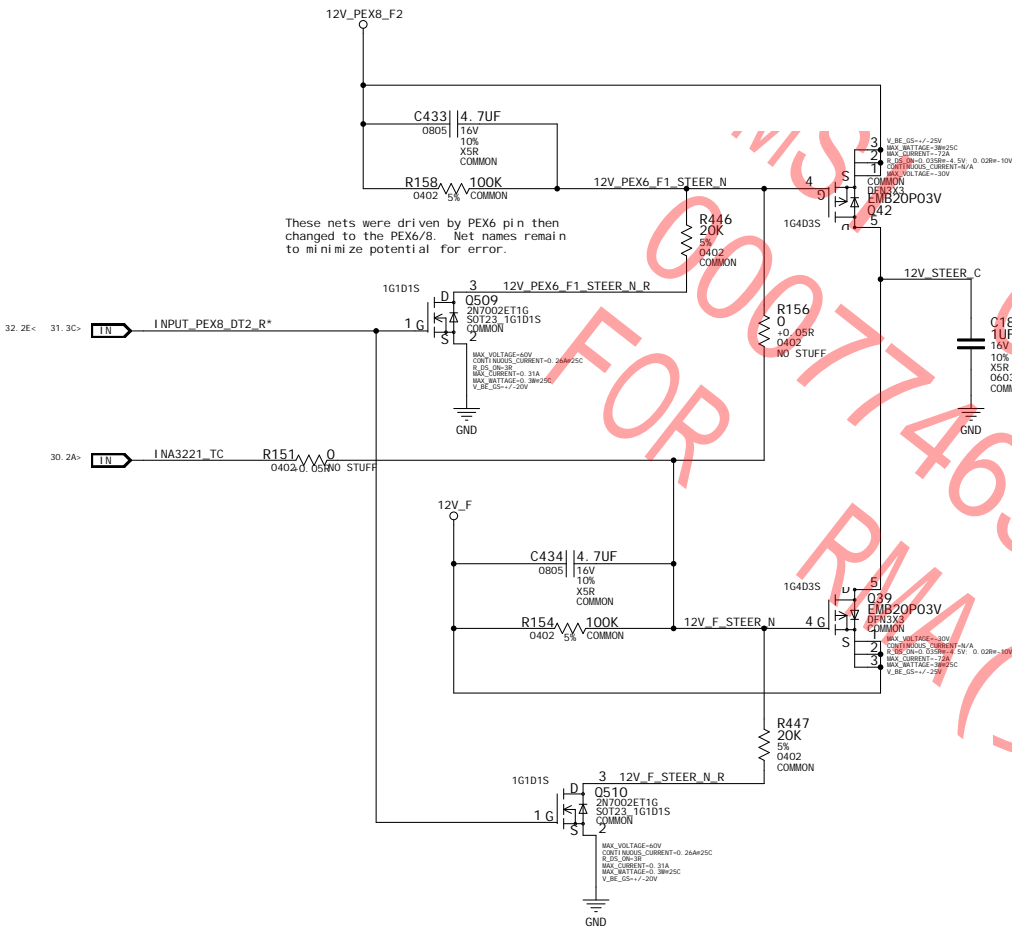
THERM OVERT SHUTDOWN LATCH

IFP\_I0VDD (backdrive prevention)

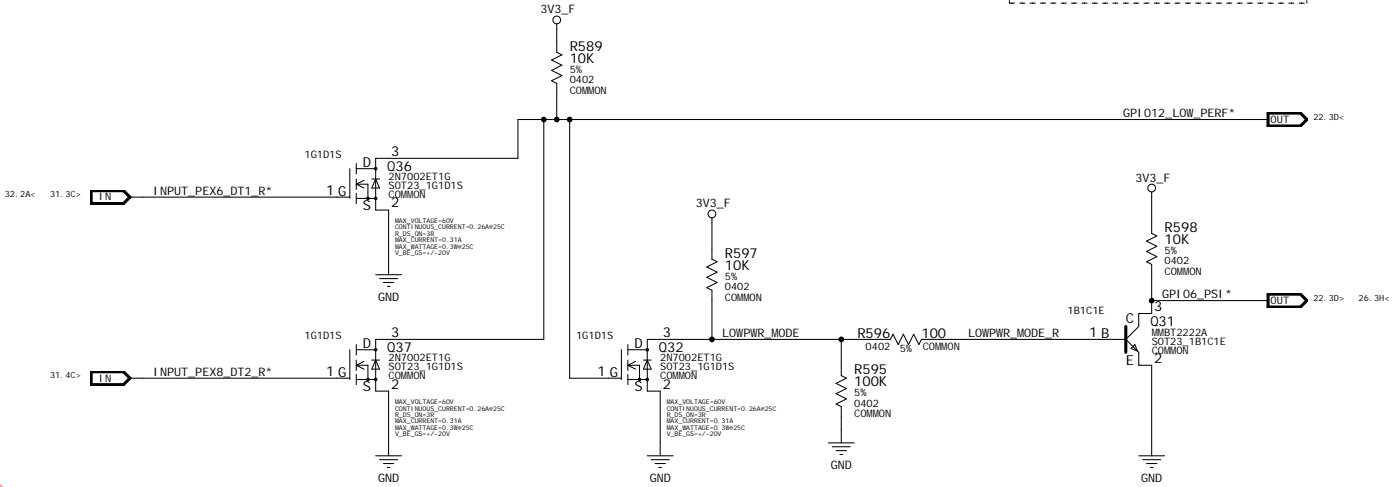
## PEX Input - NVVDD Power Sequence



PEX Input - 12V Current Steering FETs



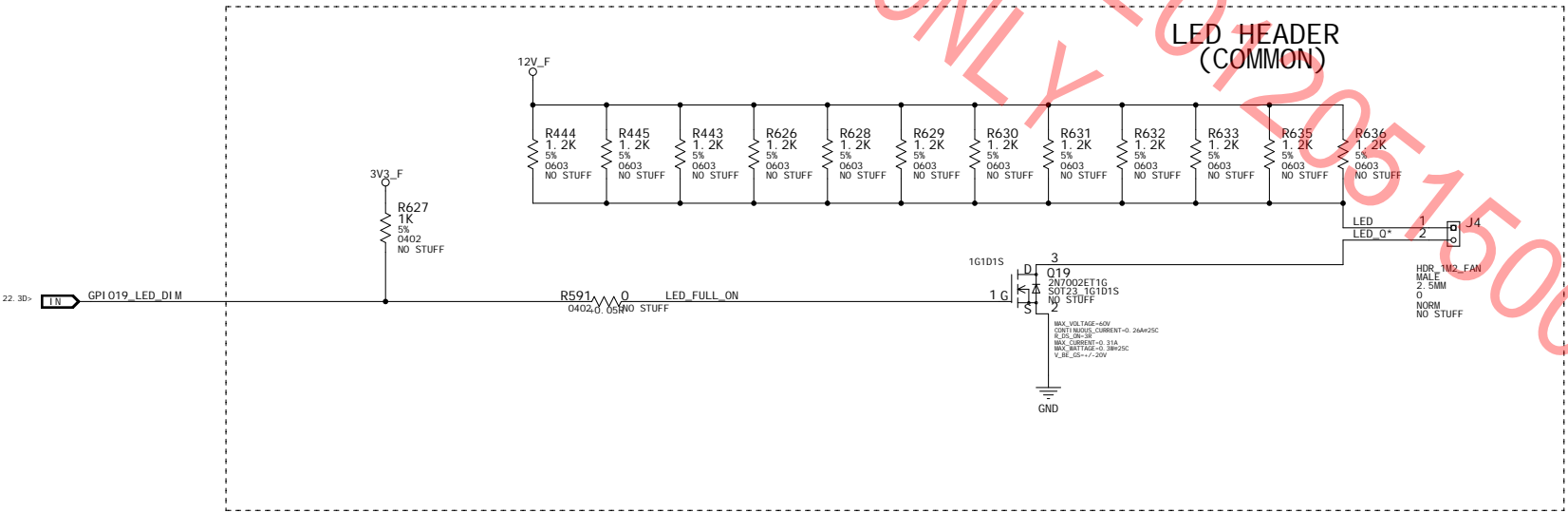
PEX Input - Power Level /PSI \* Control



GPI012_LOW_PERF*	GPU_SPEED
0	Slow
1	Normal

GeForce Logo LED

LED HEADER (COMMON)



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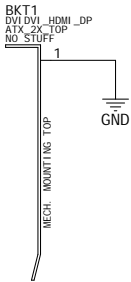
BOM REV A

PAGE 32 OF 33

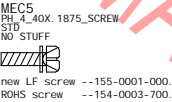
DATE 07-FEB-2012

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Brackets:



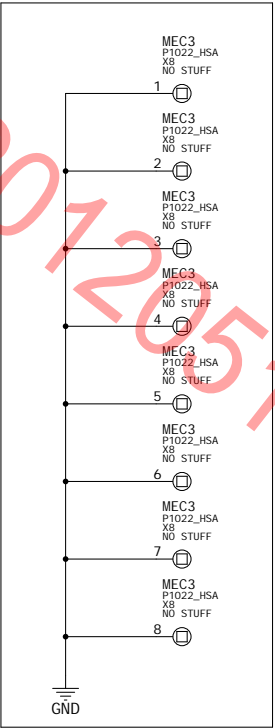
Bracket Screw



Hockey Stick



GPU Sti ffner



Mechani cal Hol es Symbol



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BOM REV A DATE 07-FEB-2012

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