

PG142-B00

DP + DP + DP + HDMI/DP

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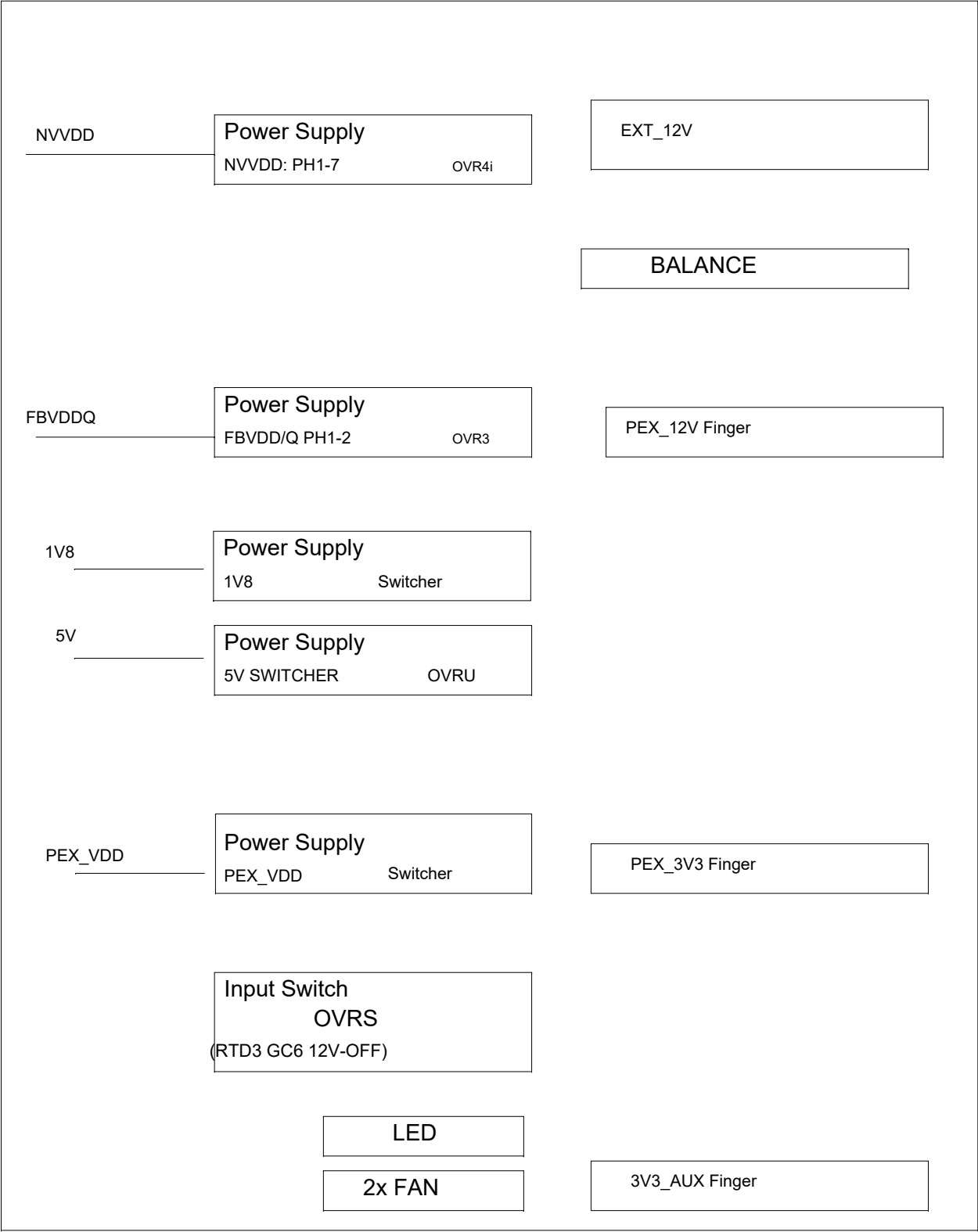
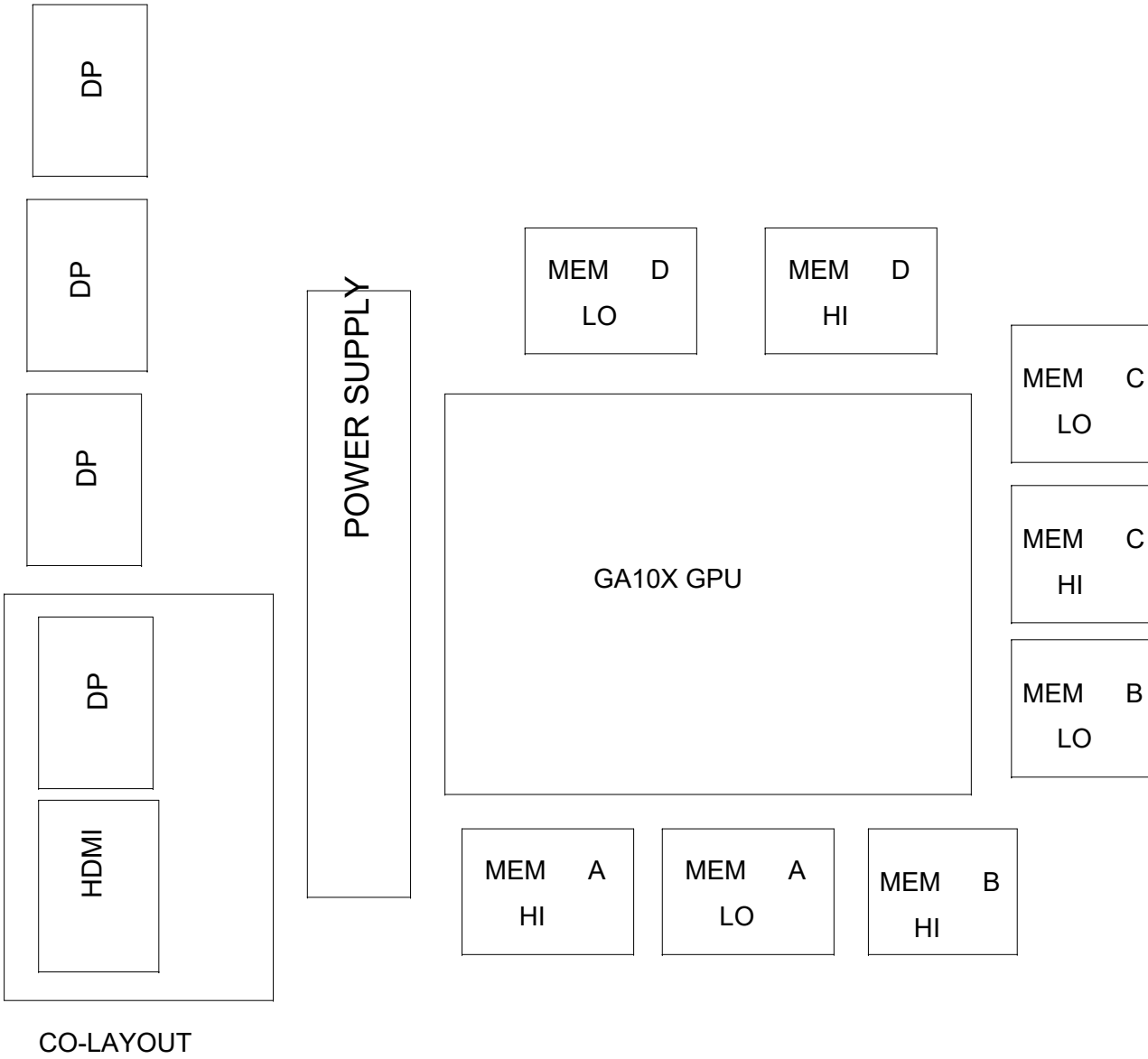
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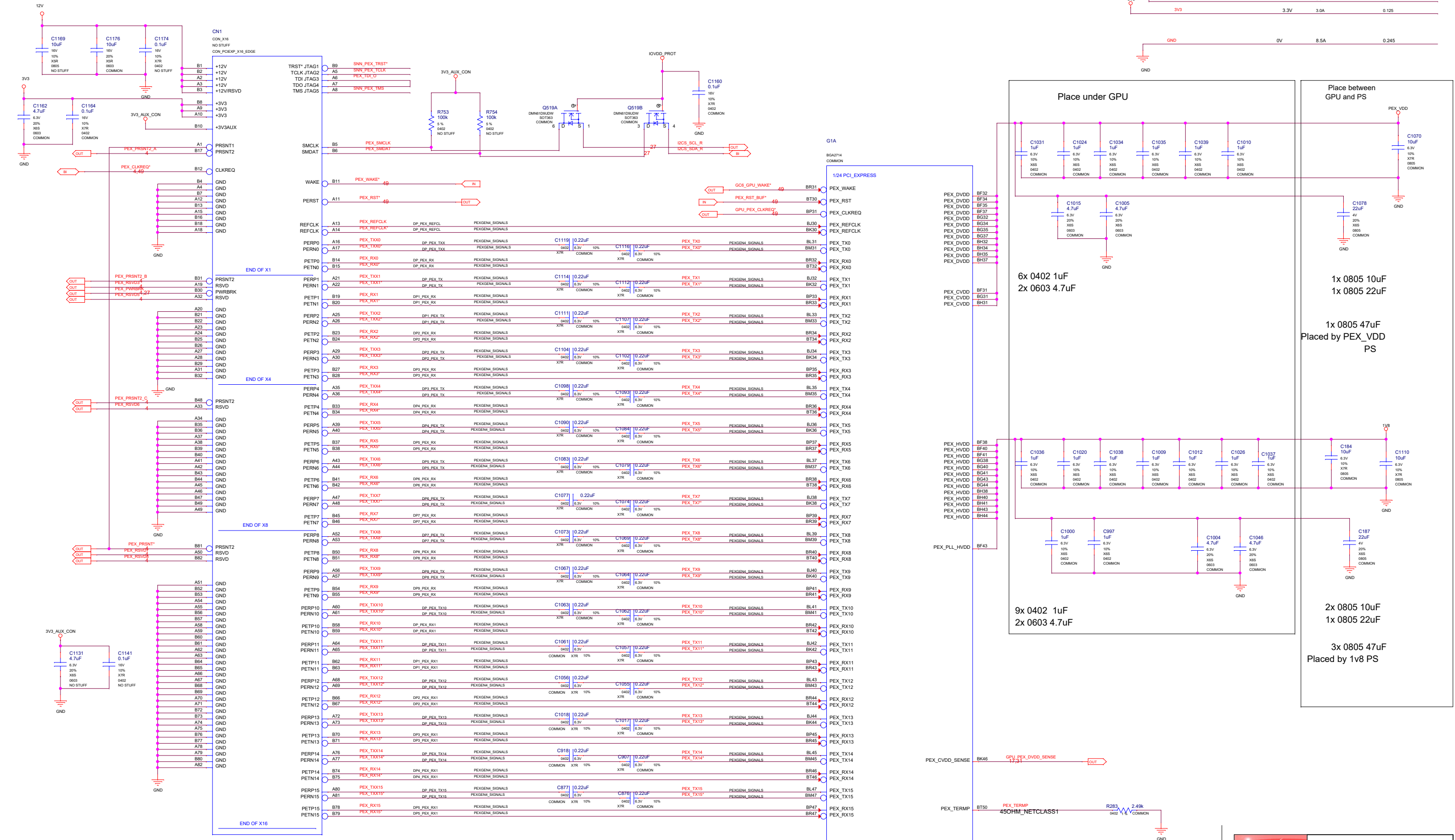
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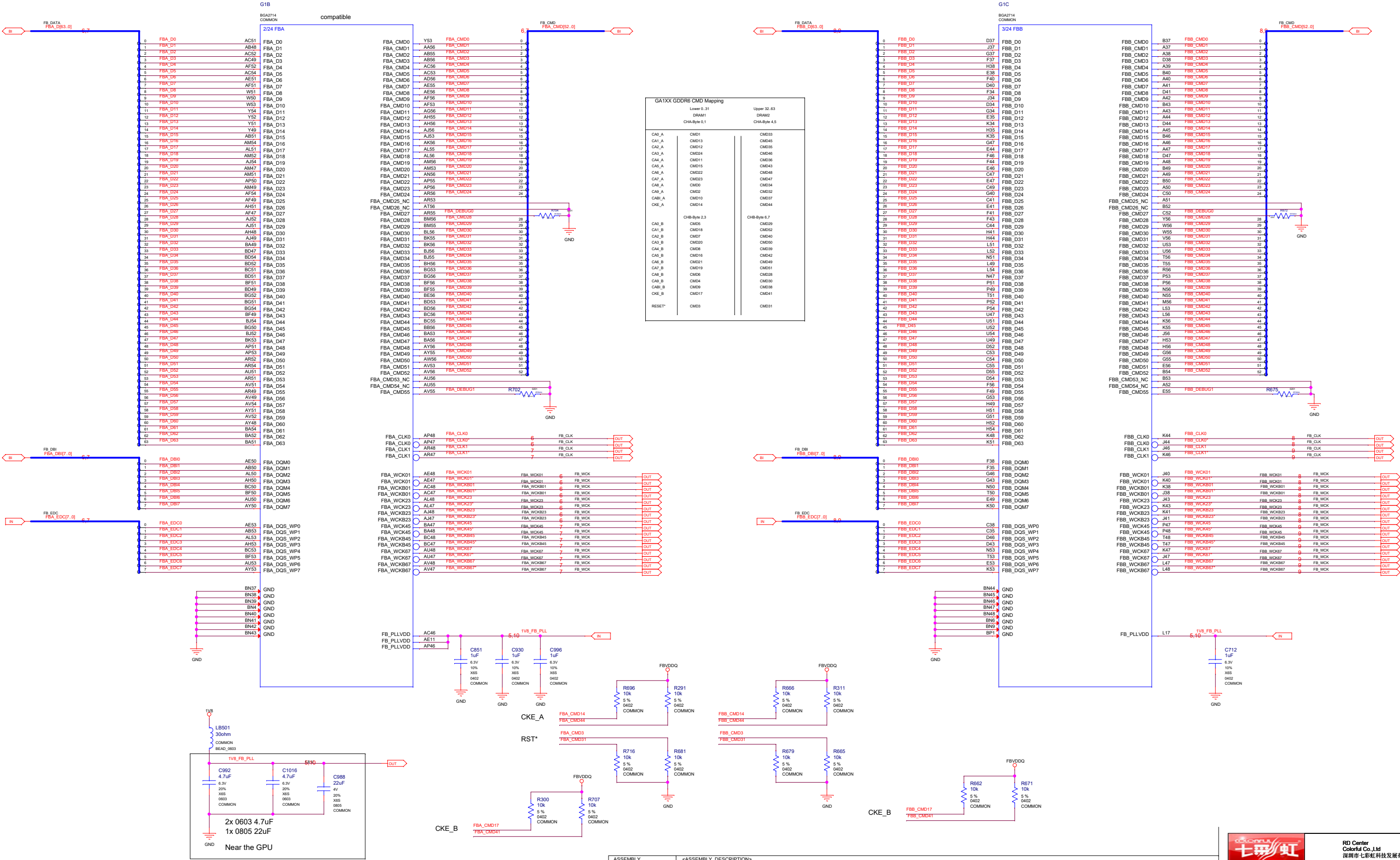
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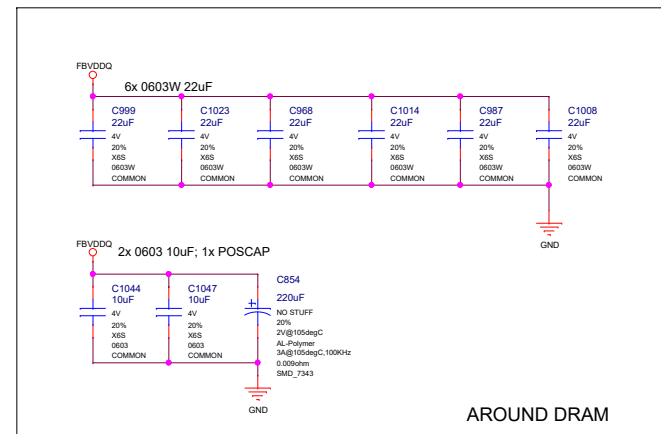
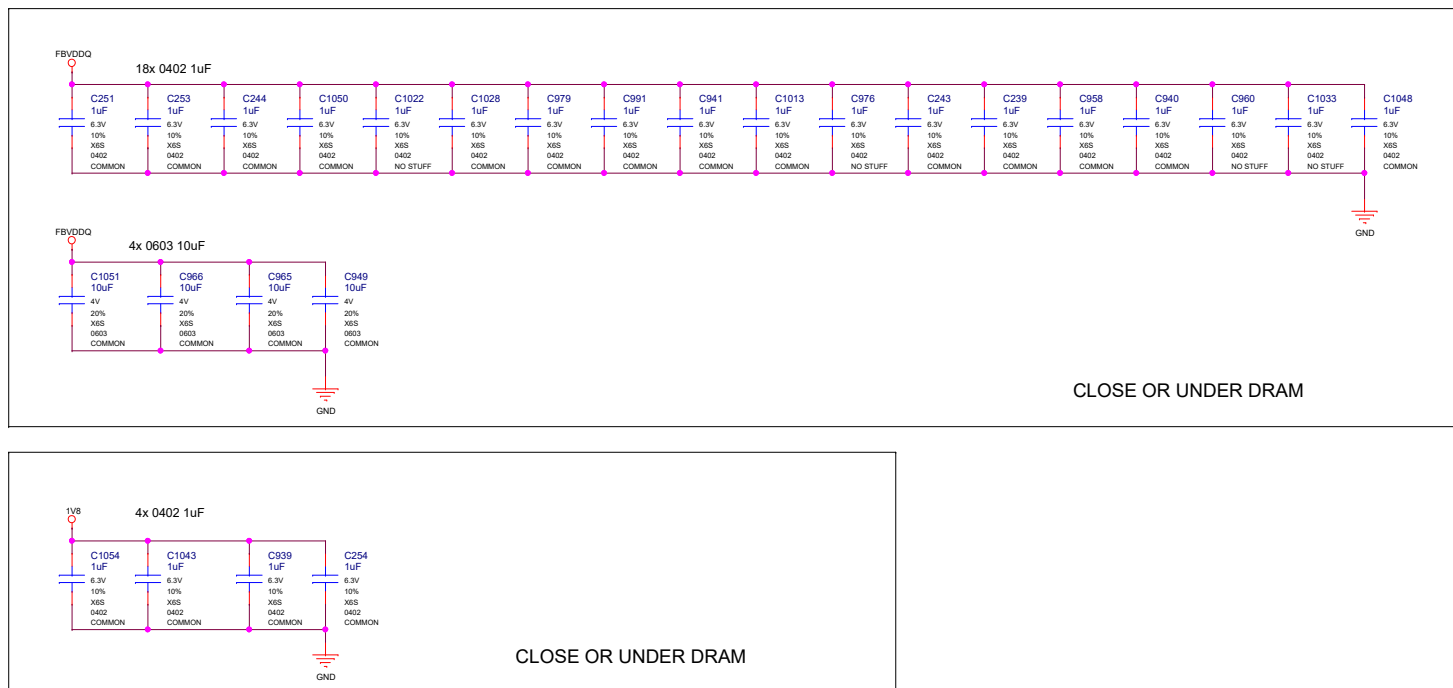
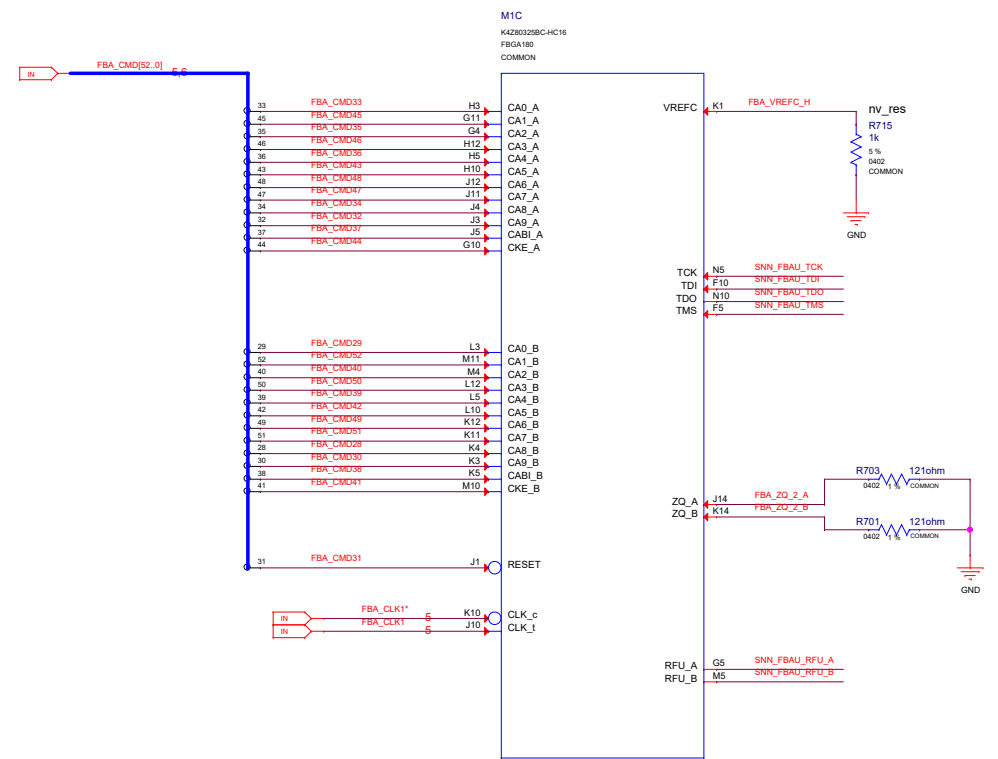
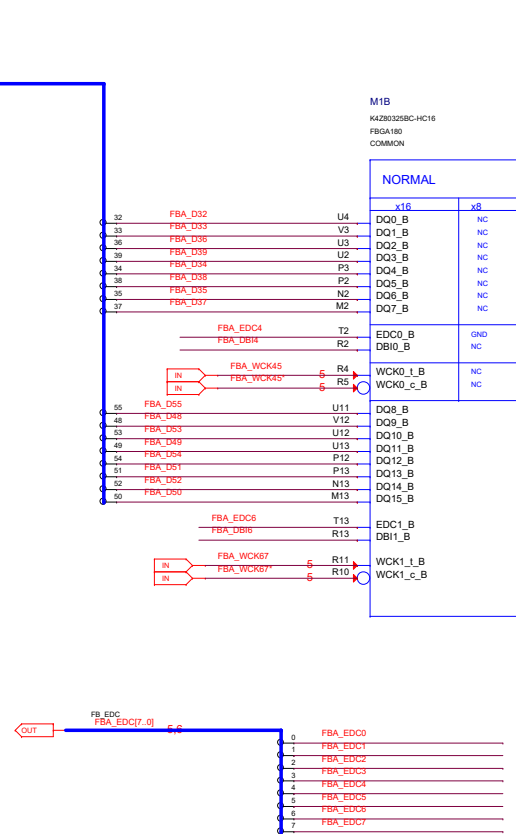
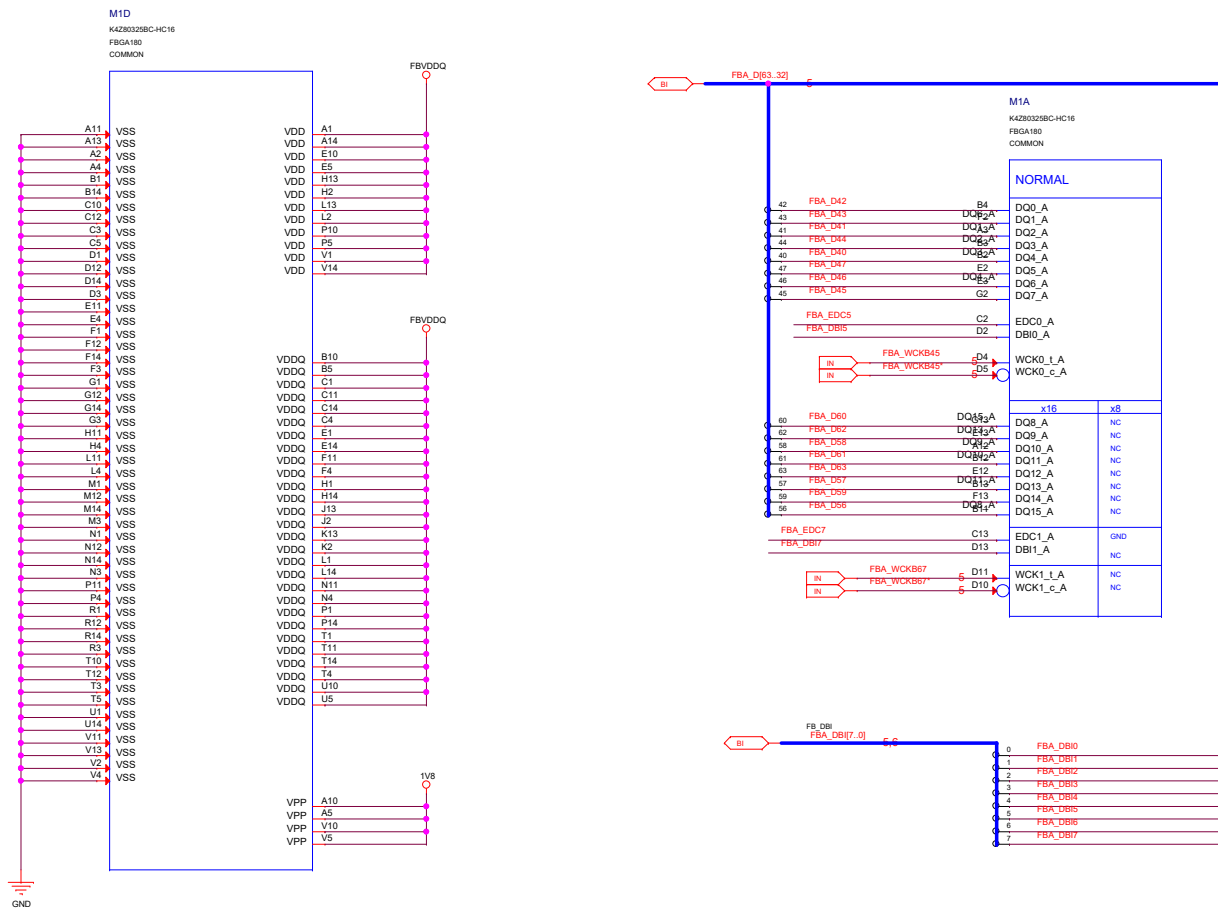
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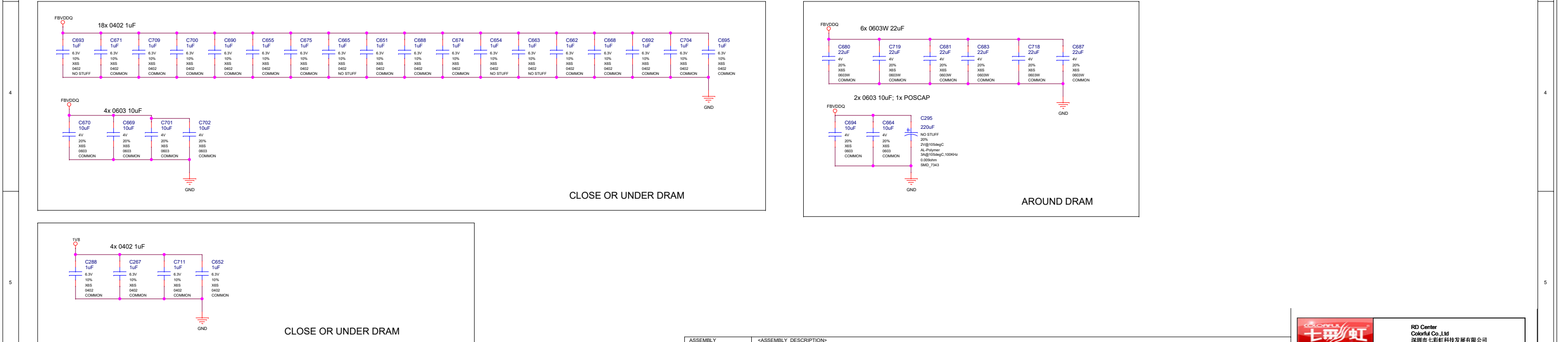
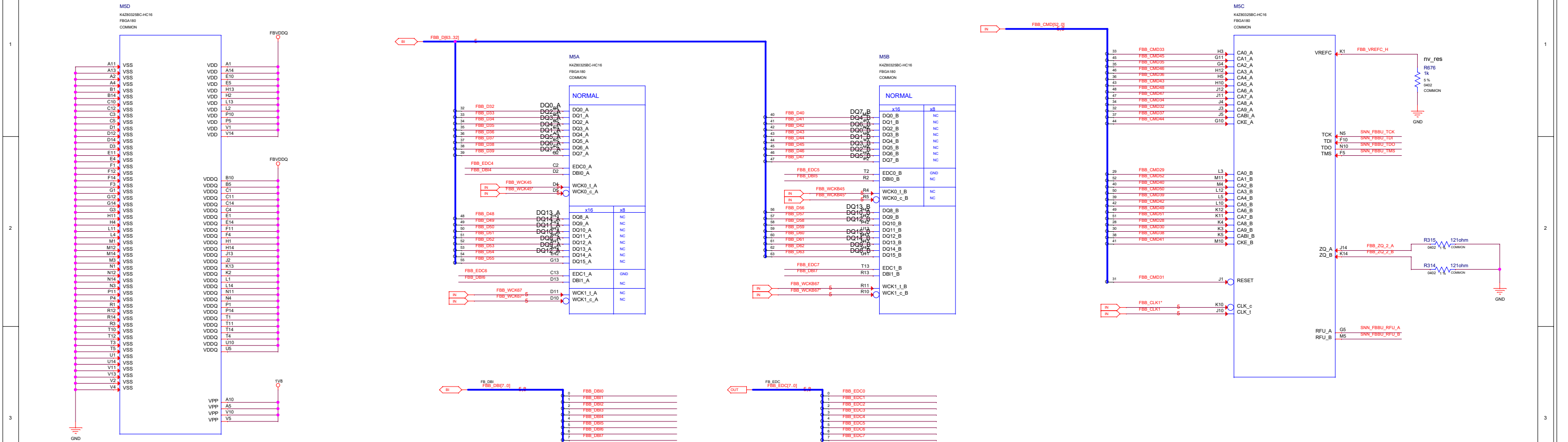
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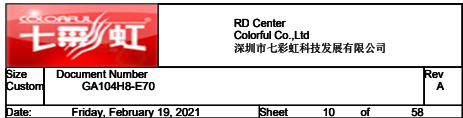
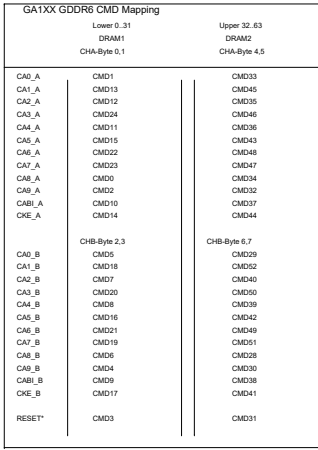
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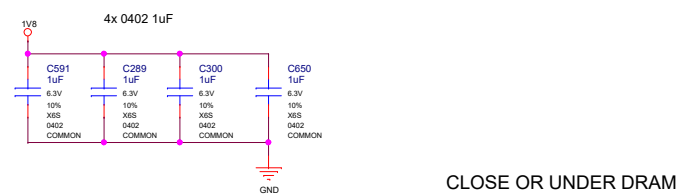
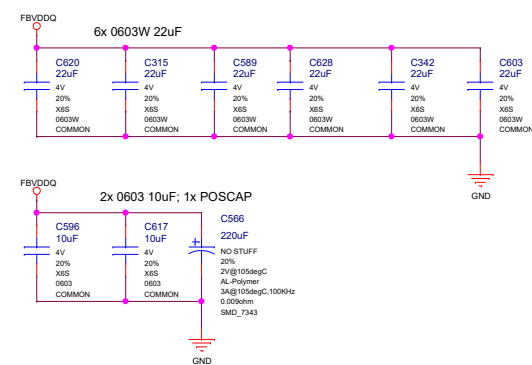
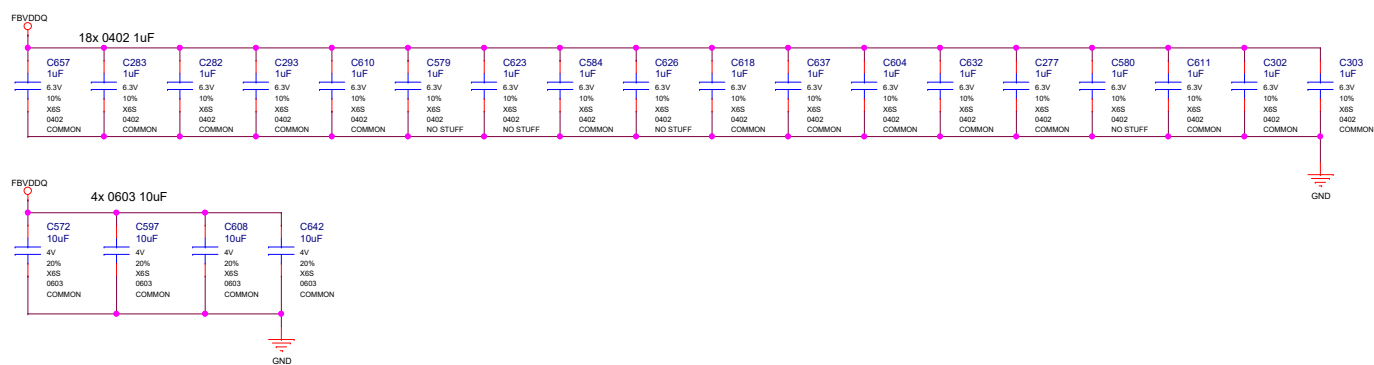
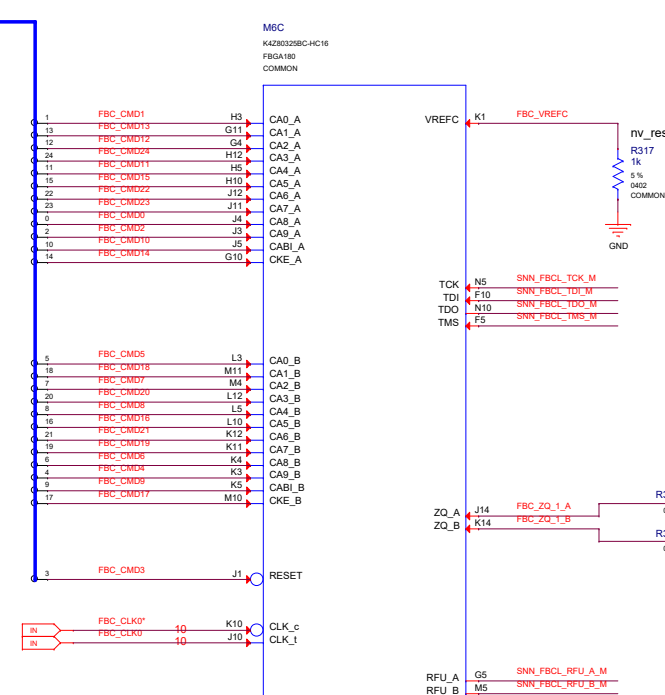
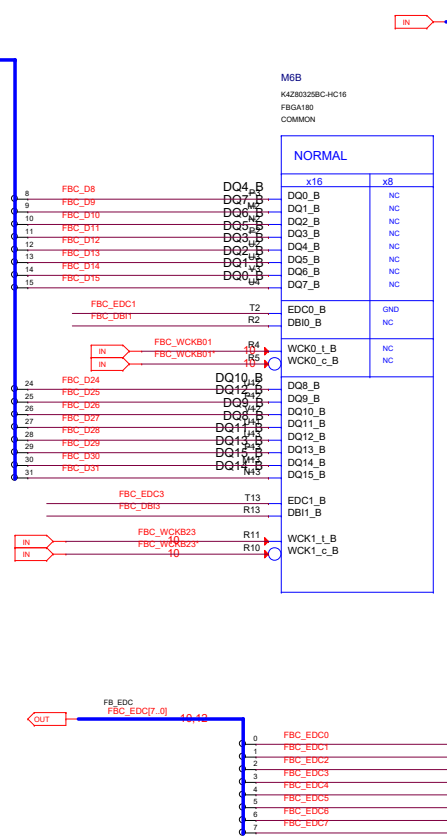
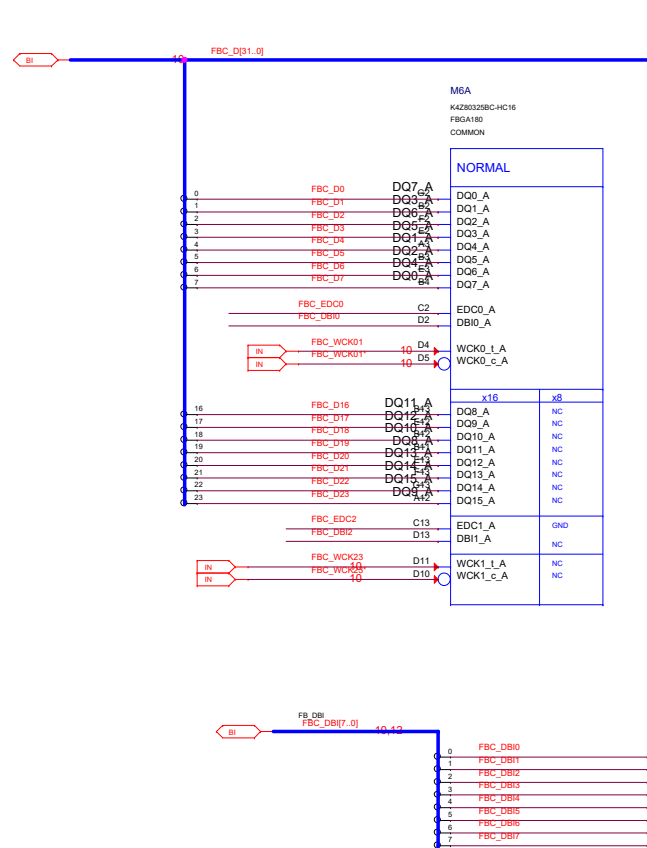
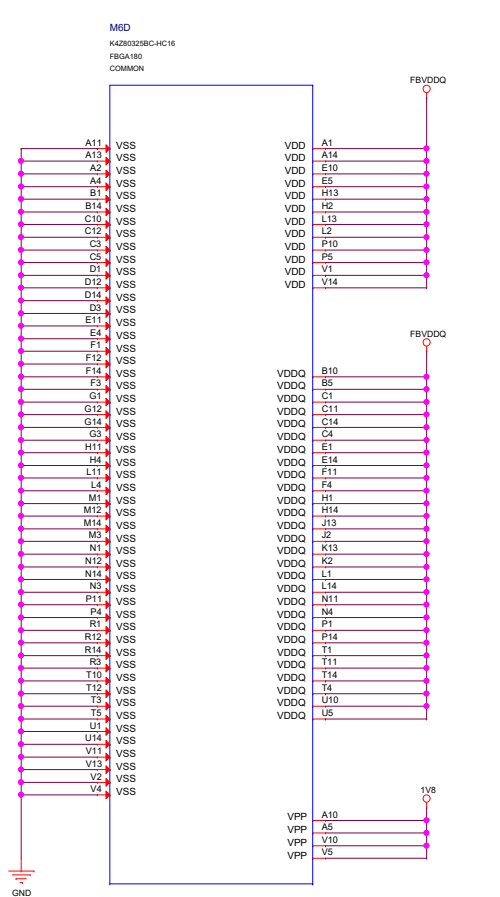


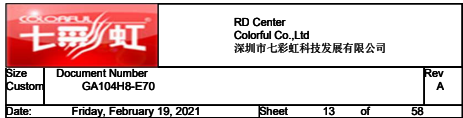
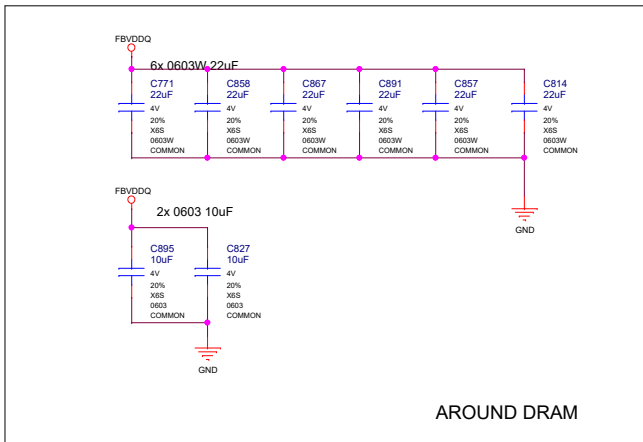
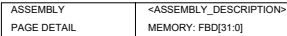


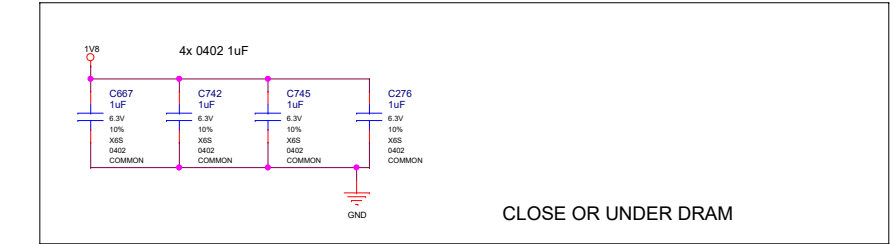
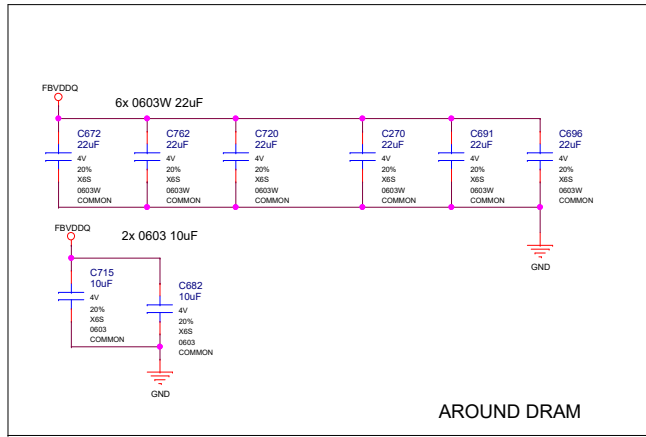
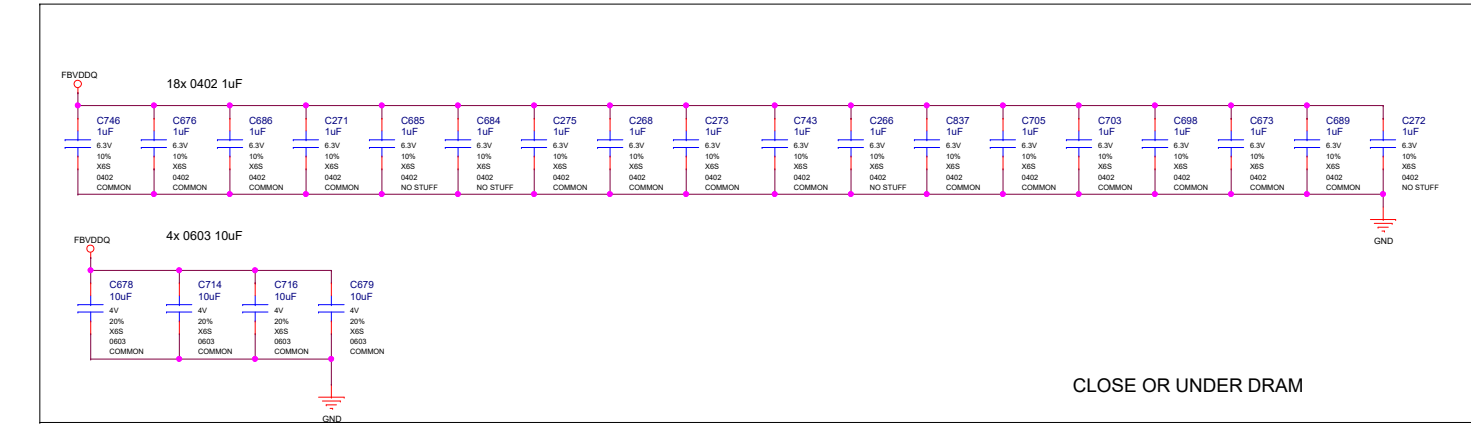
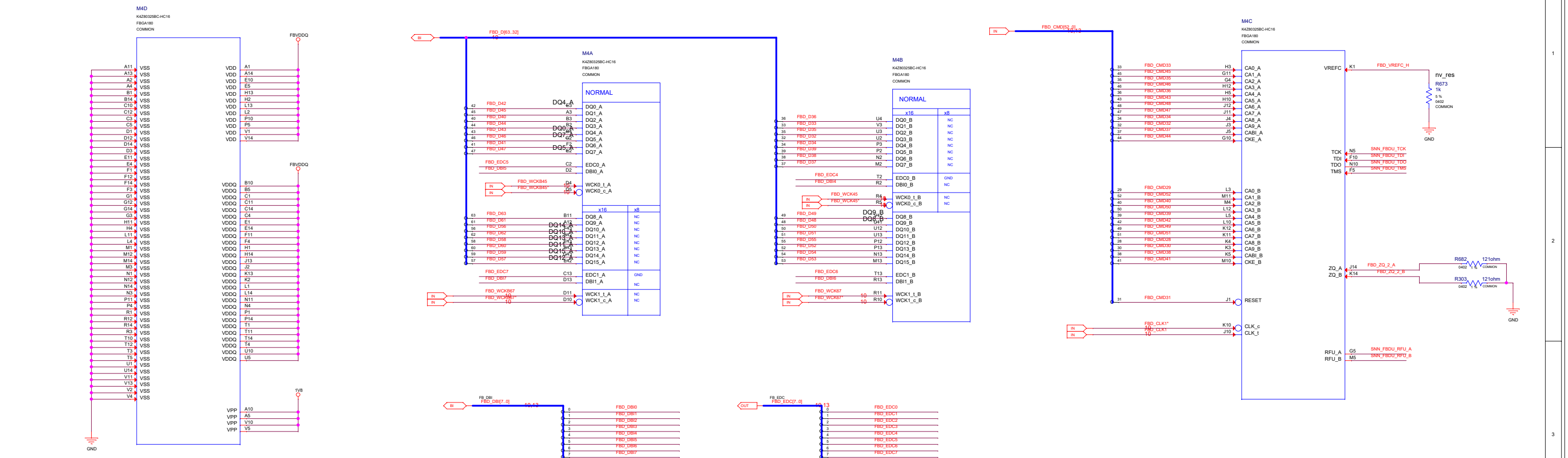
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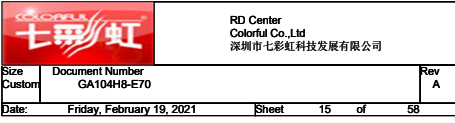
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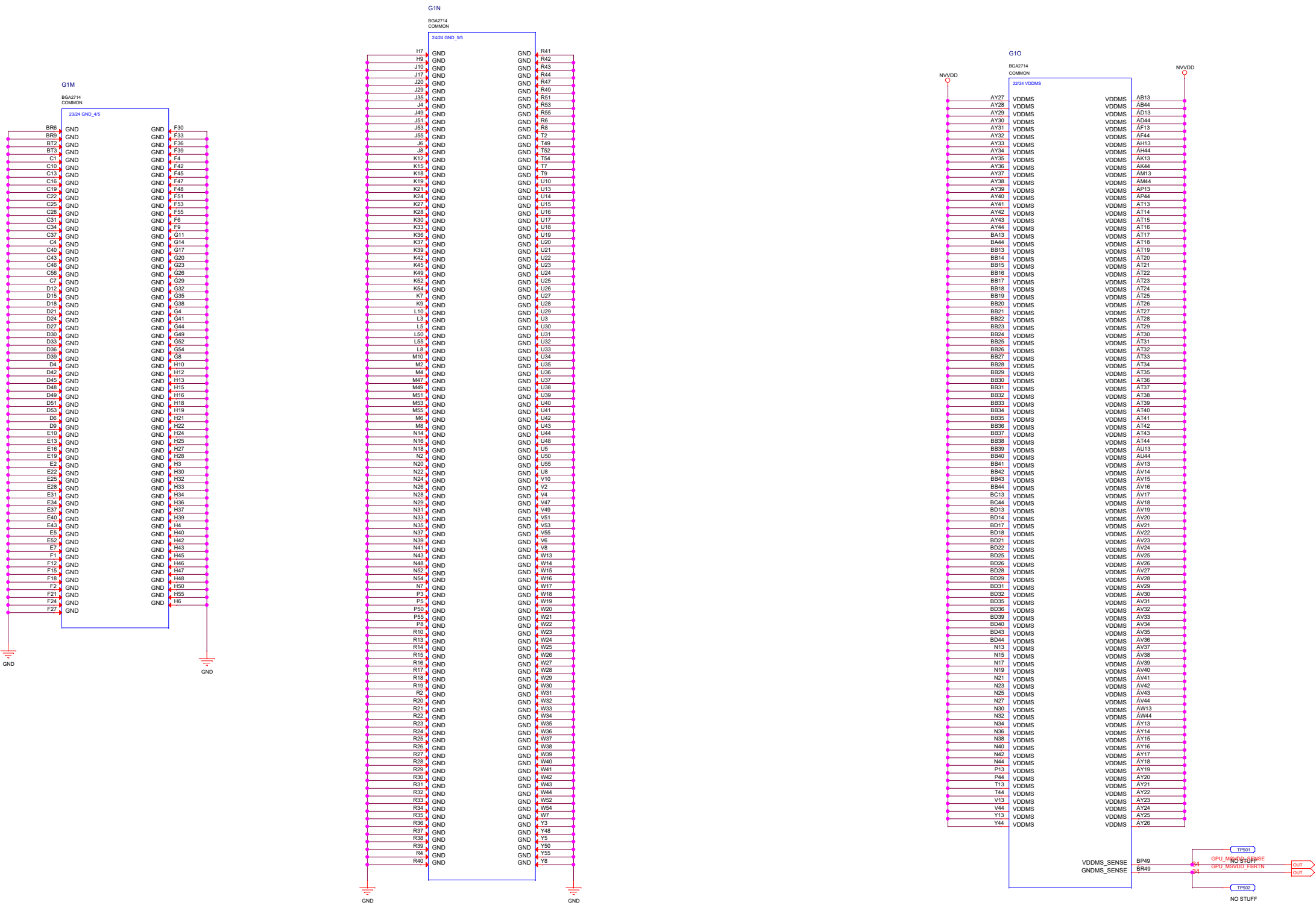
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GPU PWR & GND

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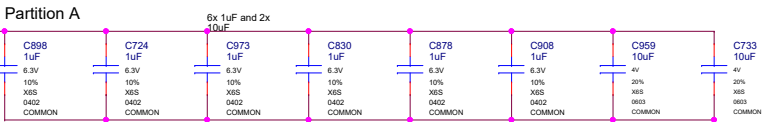
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FBVDDQ

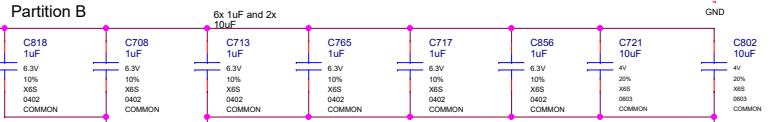
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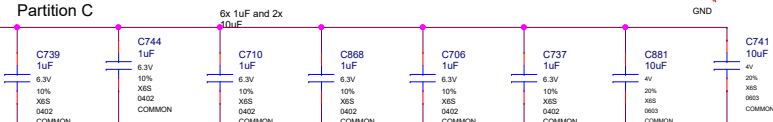
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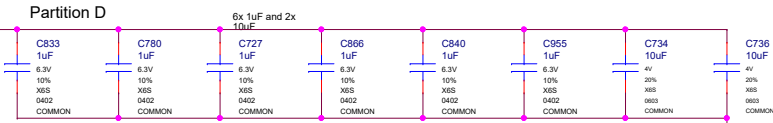
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Partition C



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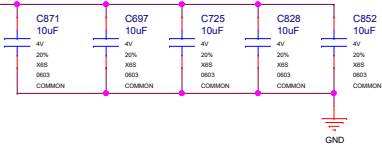


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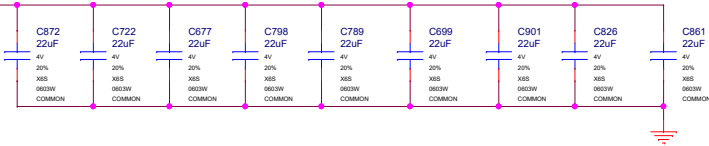
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9x 22uF




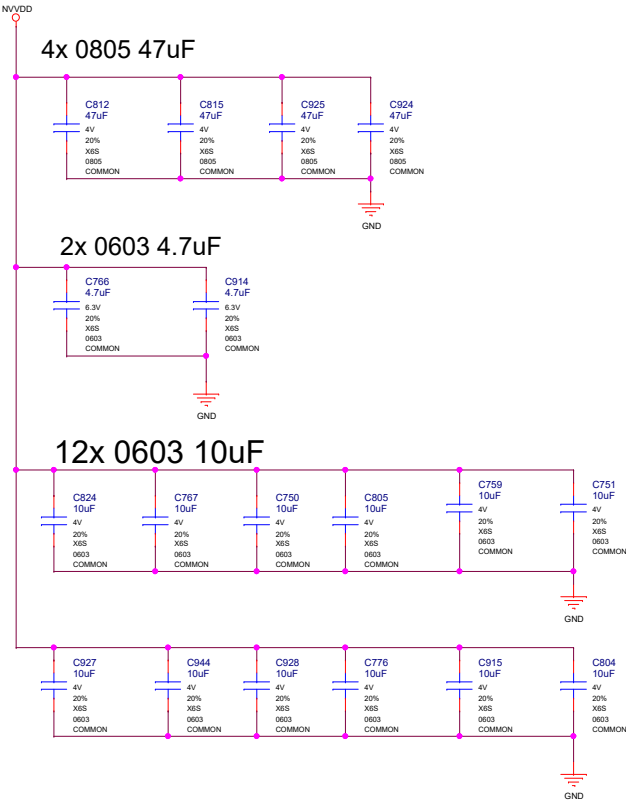
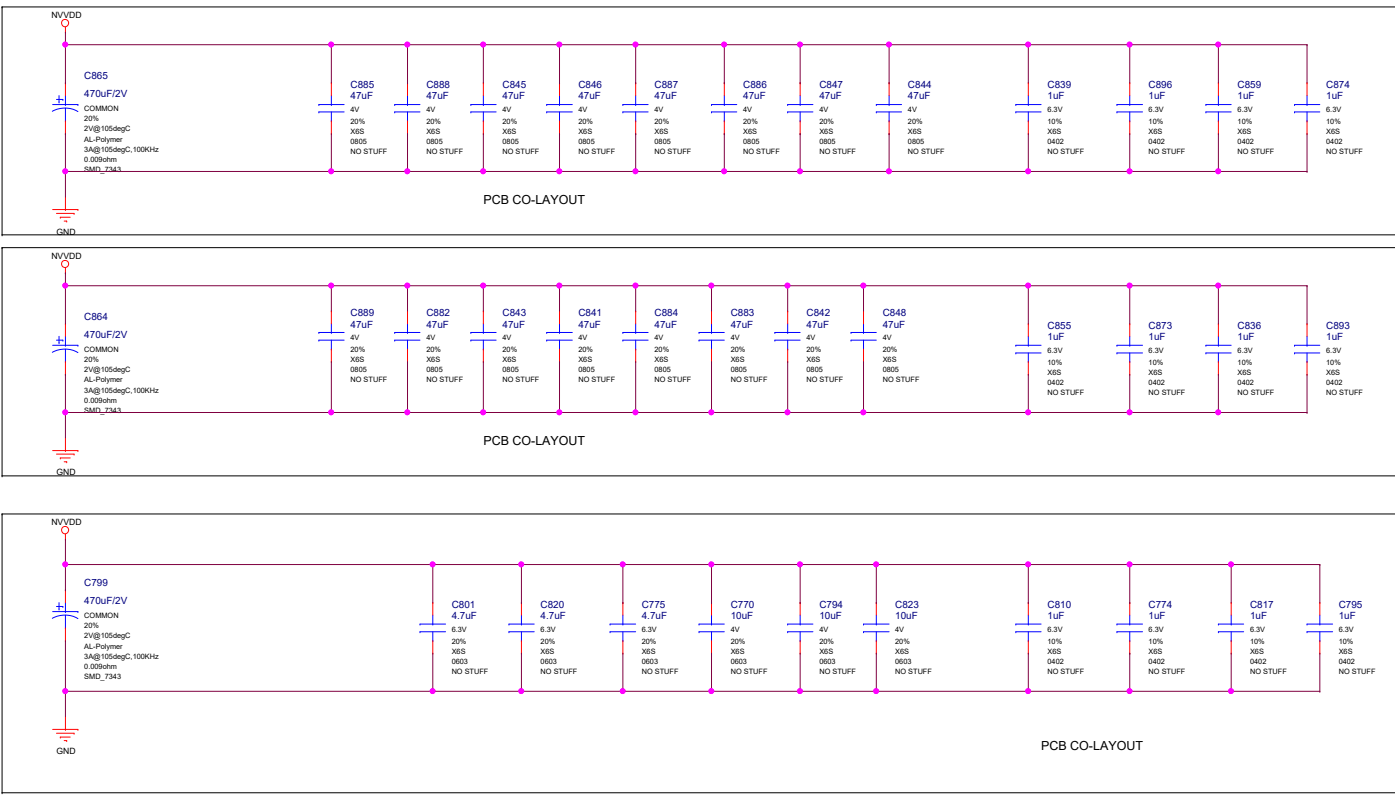
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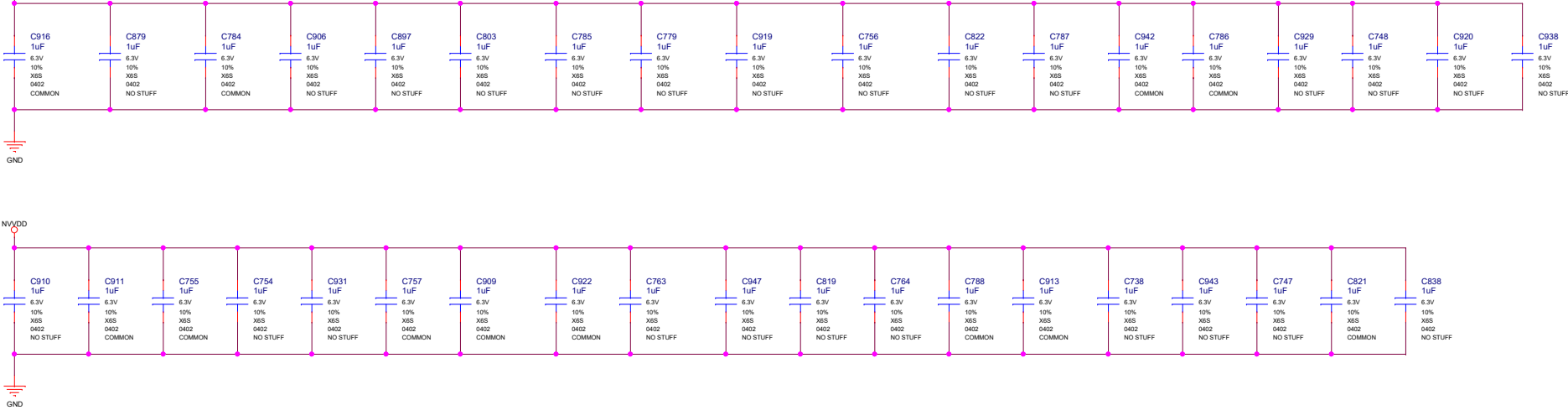
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37 x 0402 1uF




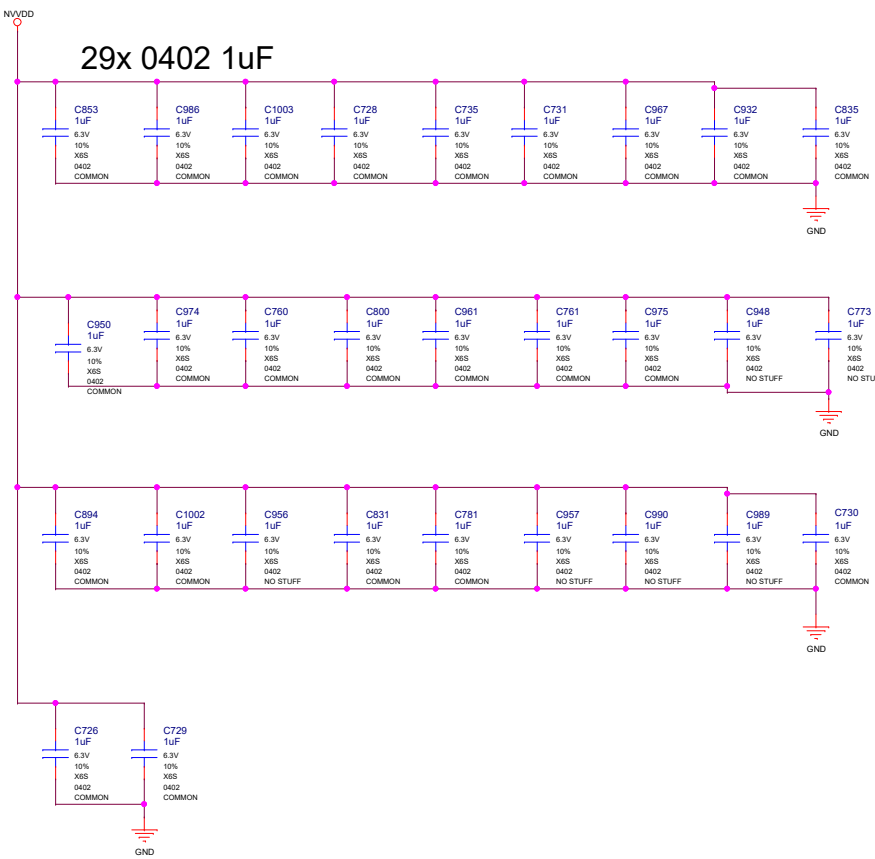
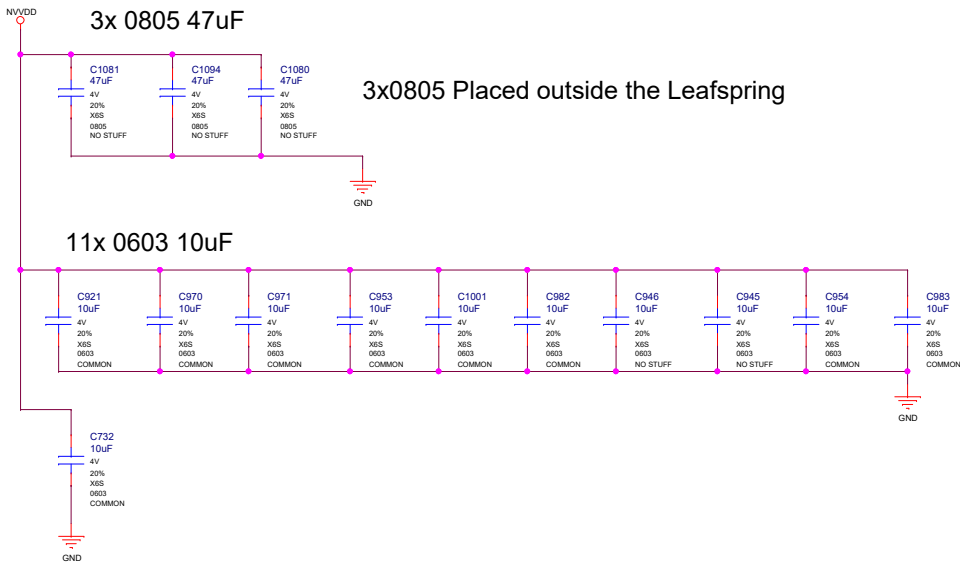
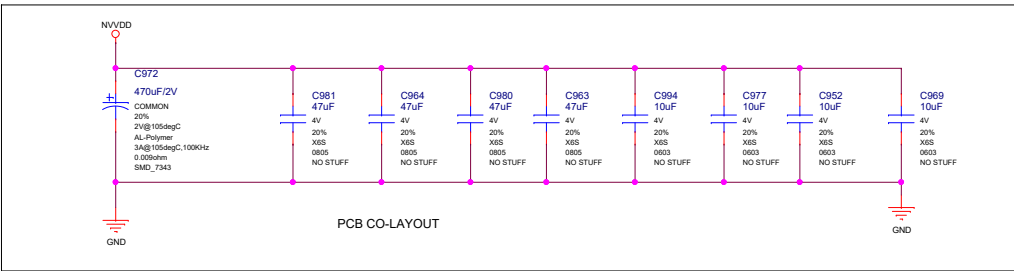
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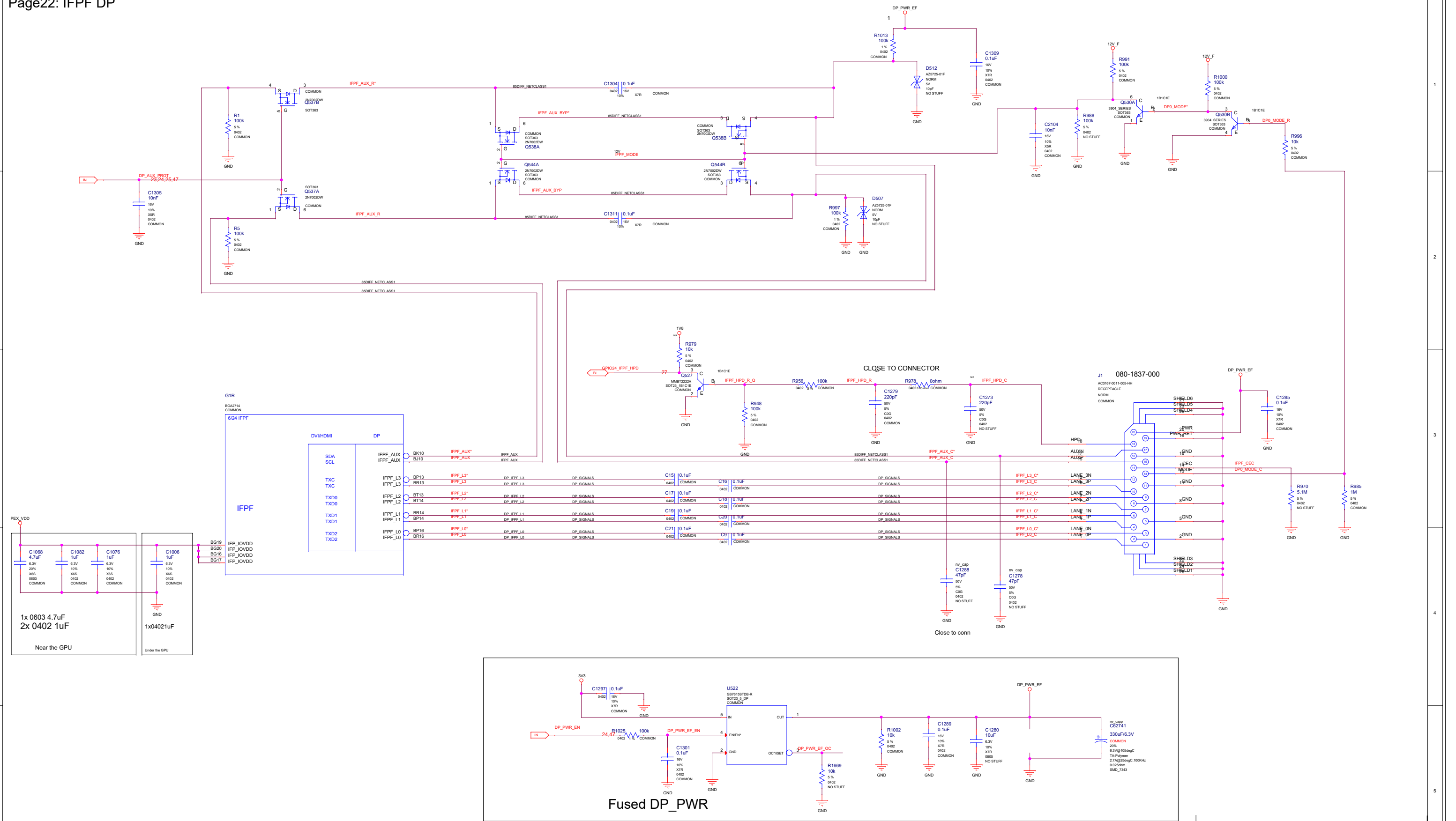
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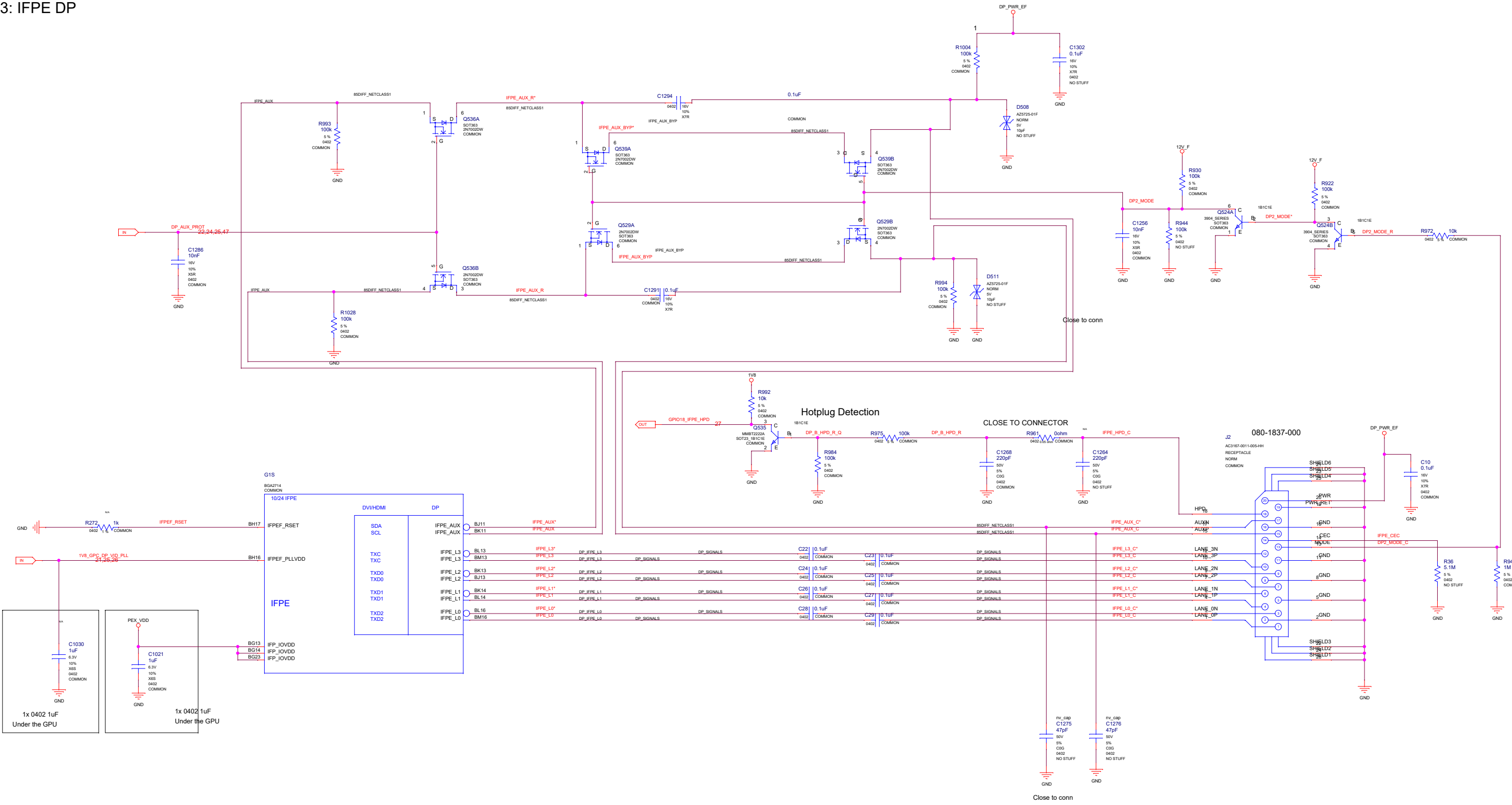
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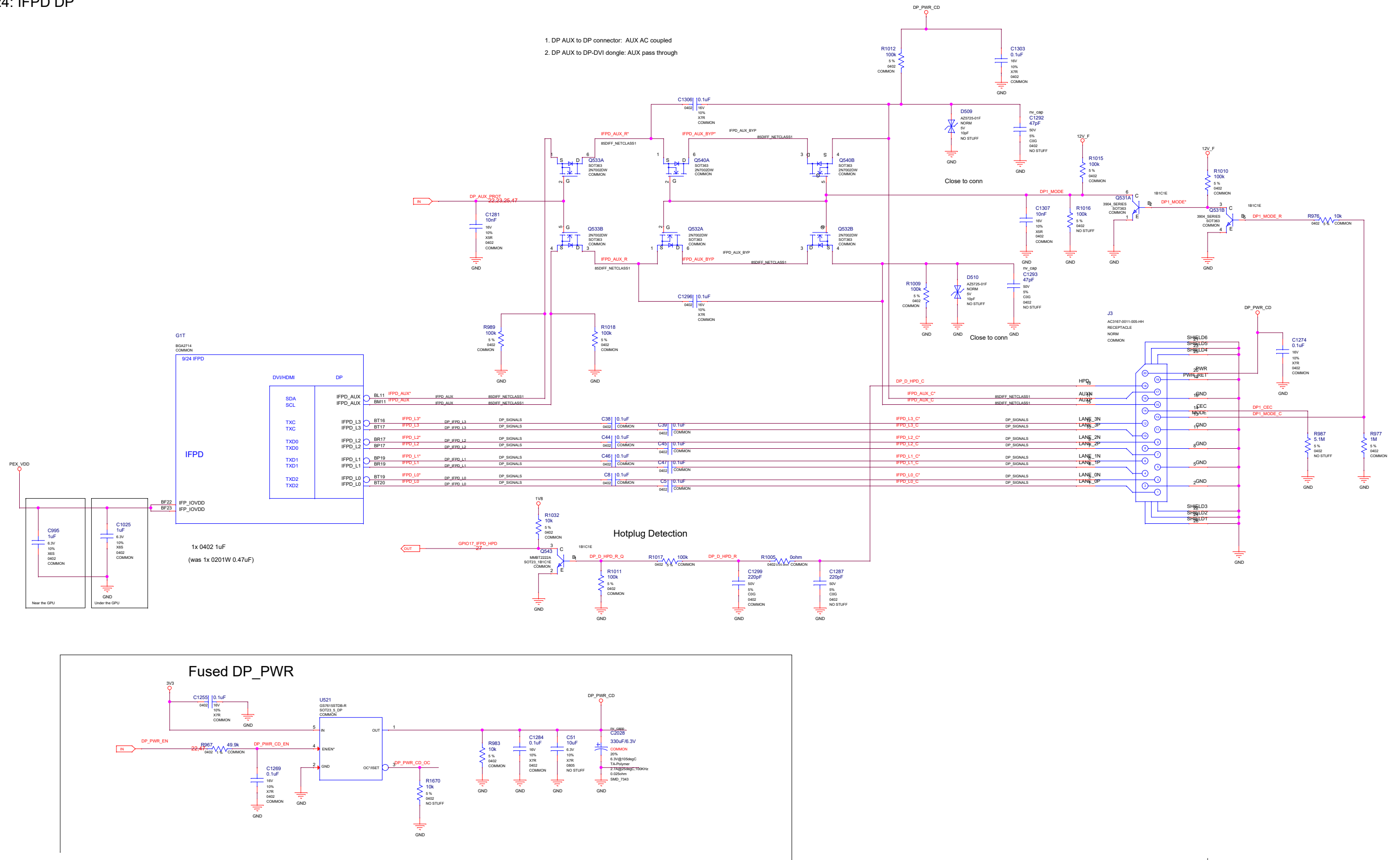
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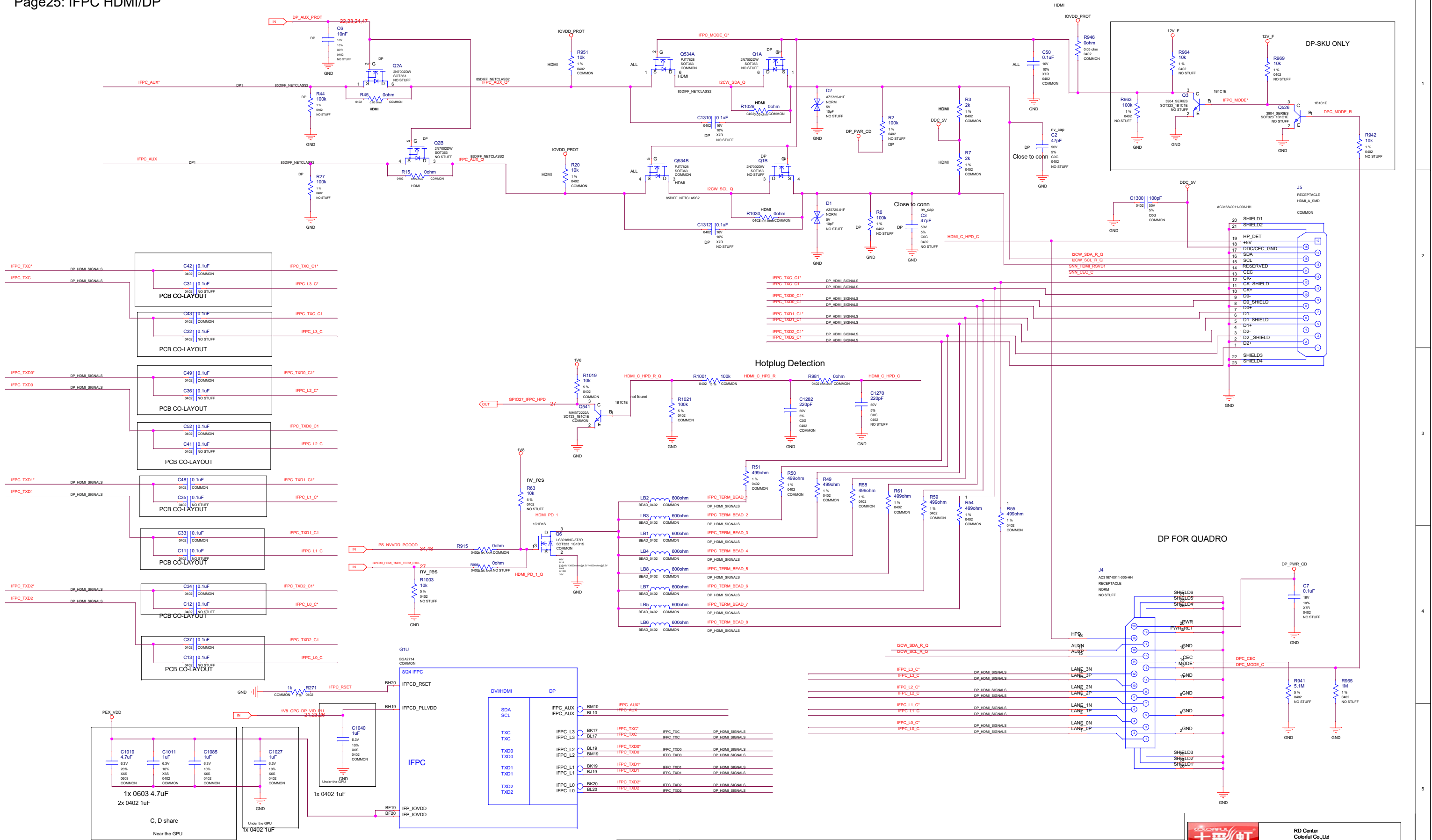
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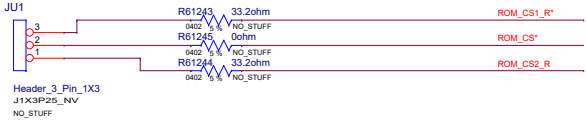
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Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
TBD				

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

JU1按下高频 Pin(1,2) 相连 BIOS2(U16)
JU1弹起 低频Pin(2,3) 相连 BIOS1(U10828)

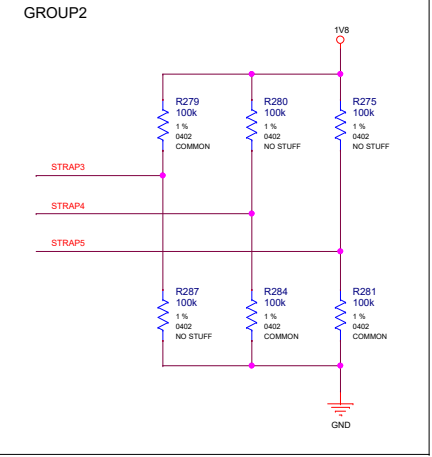
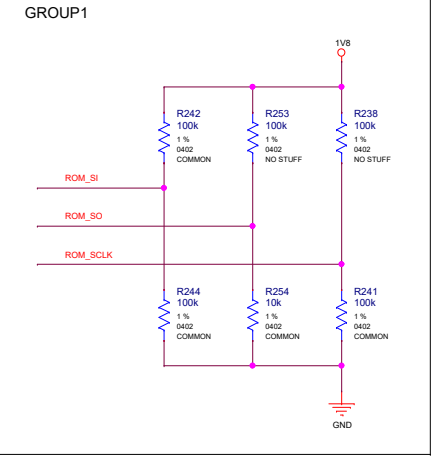
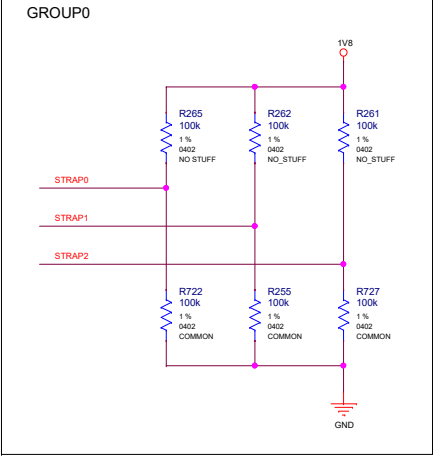


ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE		
H	H	H	0111	FS_OVERT ENABLE		
H	H	M	0000	FS_OVERT DISABLE		
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

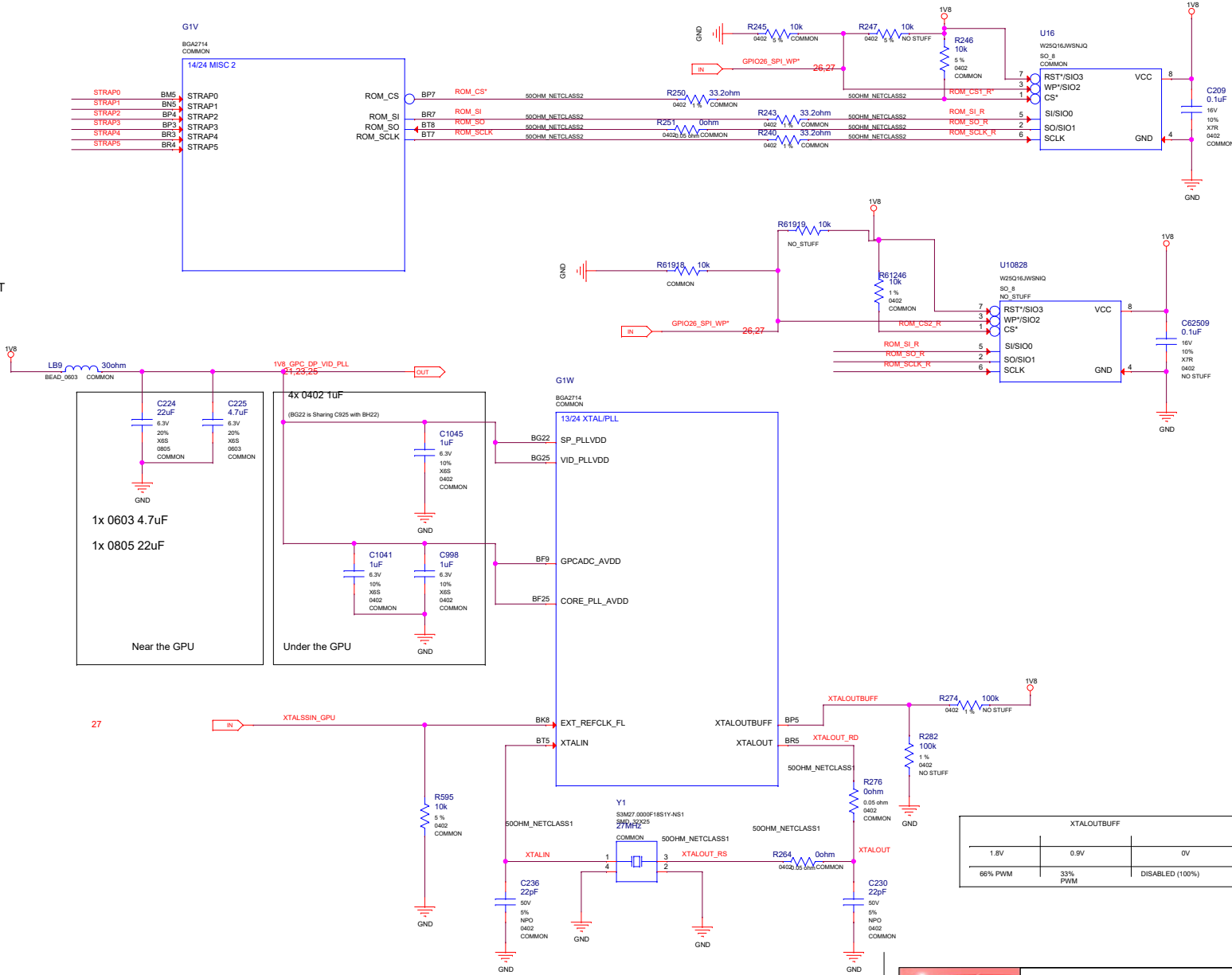
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M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



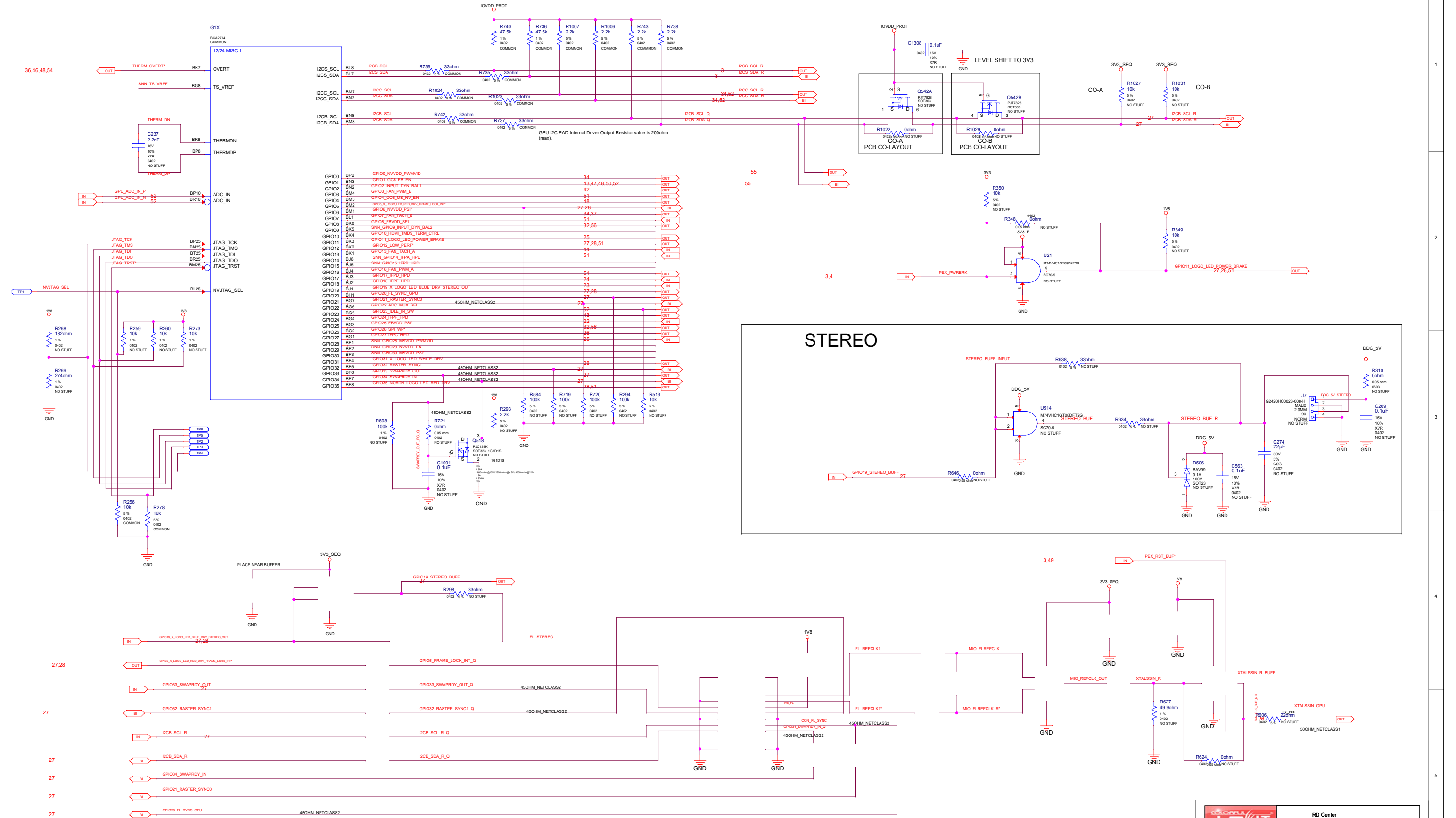
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: ROM, XTAL,STRAPS

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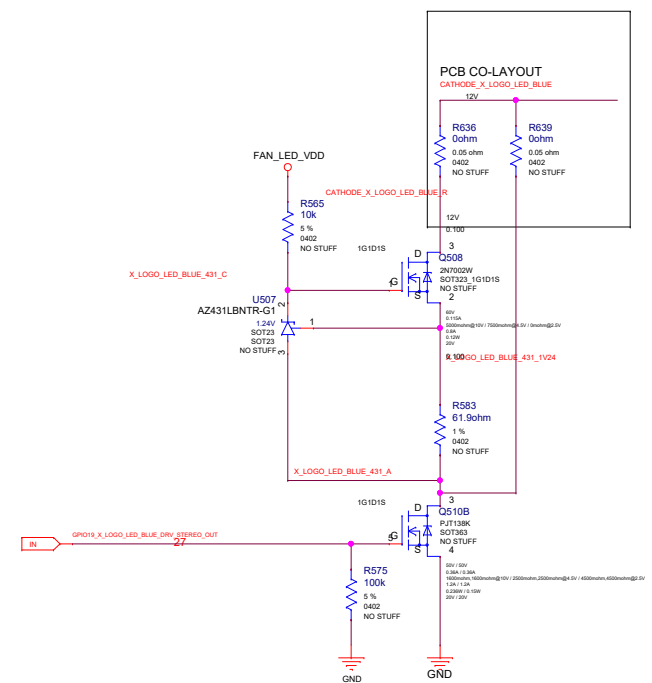
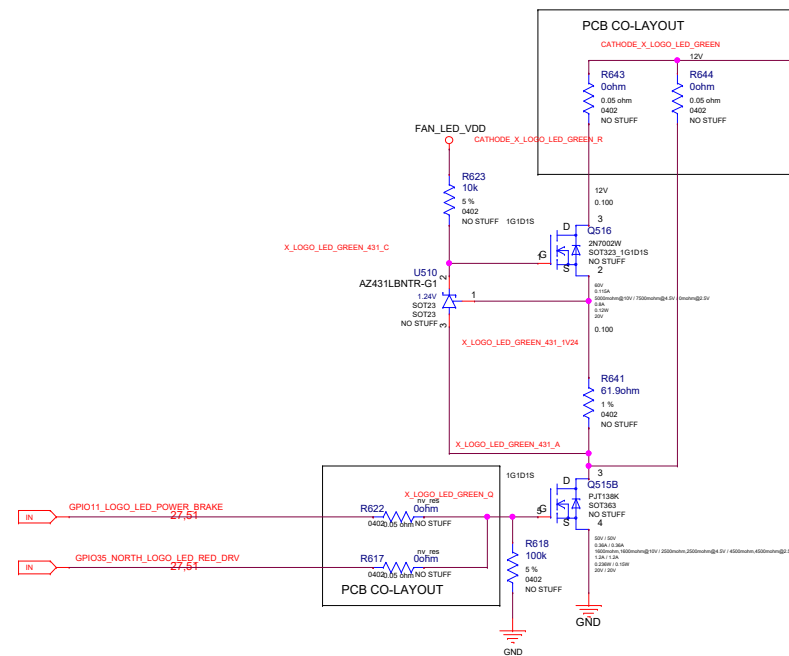
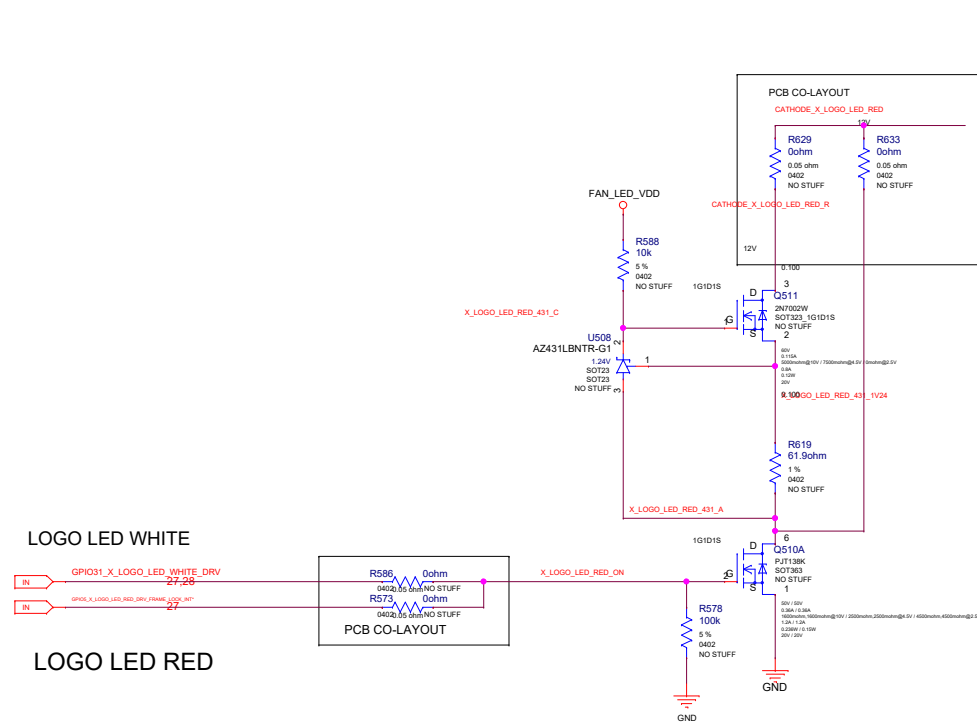
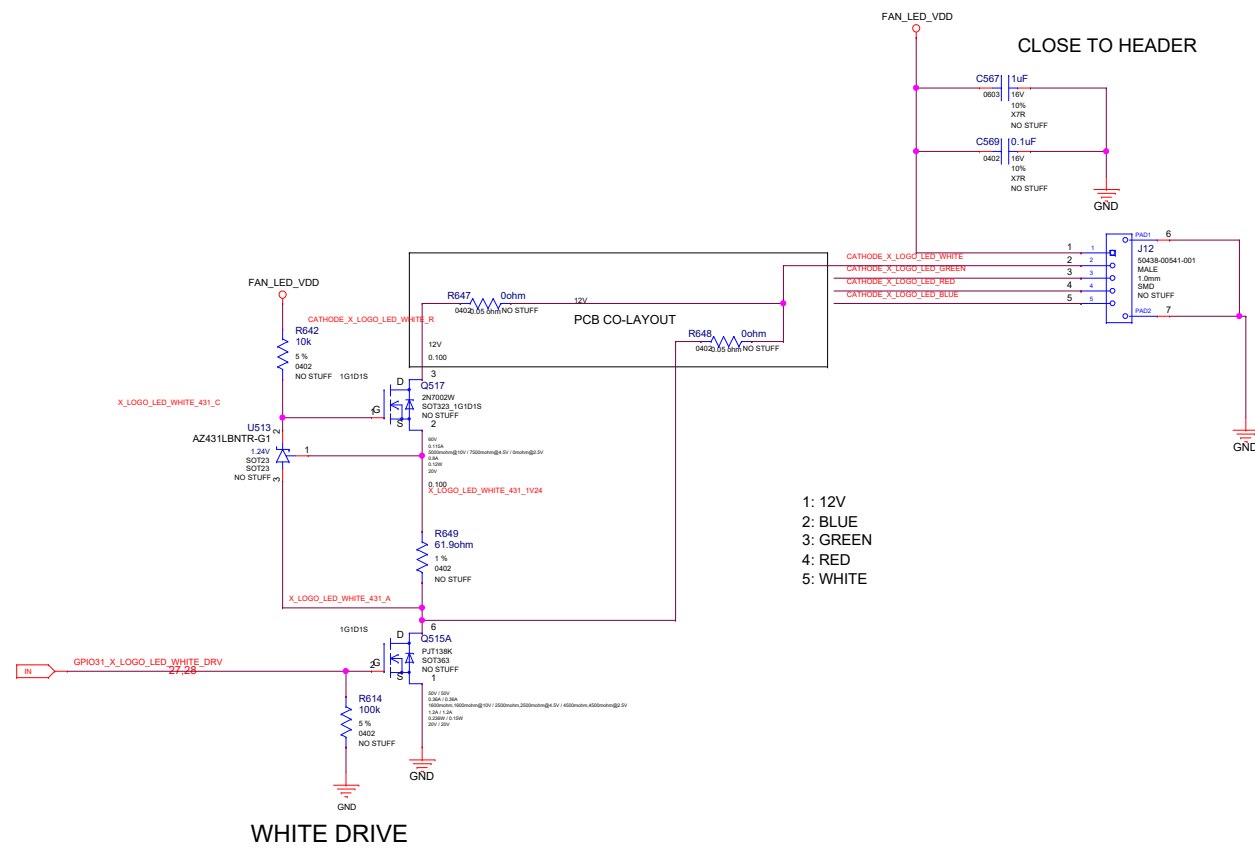


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ASSEMBLY
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MISC2: JTAG,GPIO,ADC,I2C,FL,STEREO

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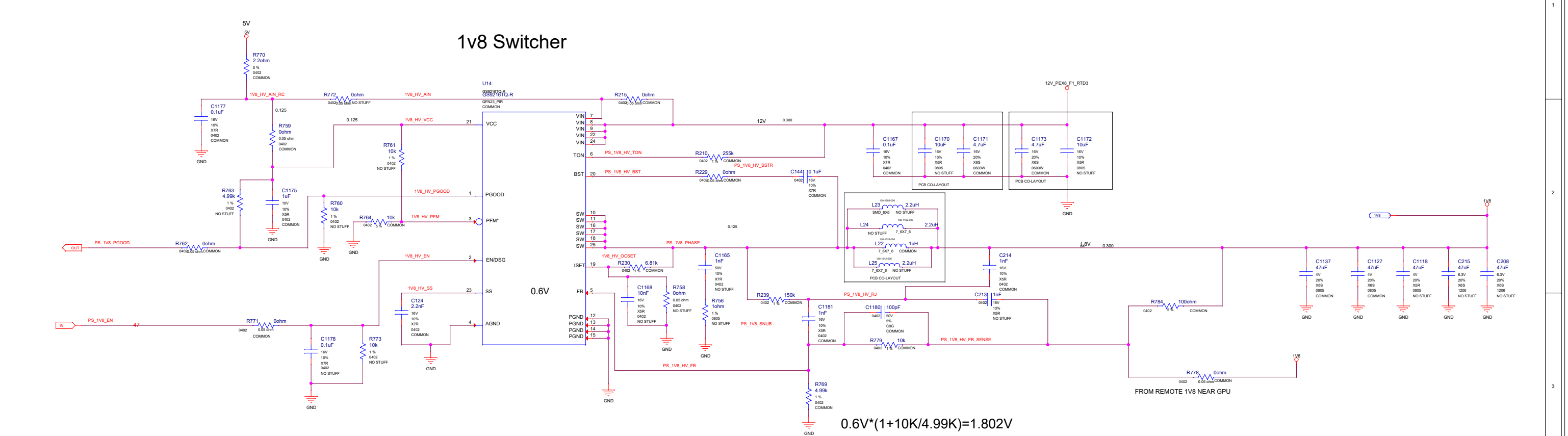
GREEN DRIVE

BLUE DRIVE

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC3: RGB


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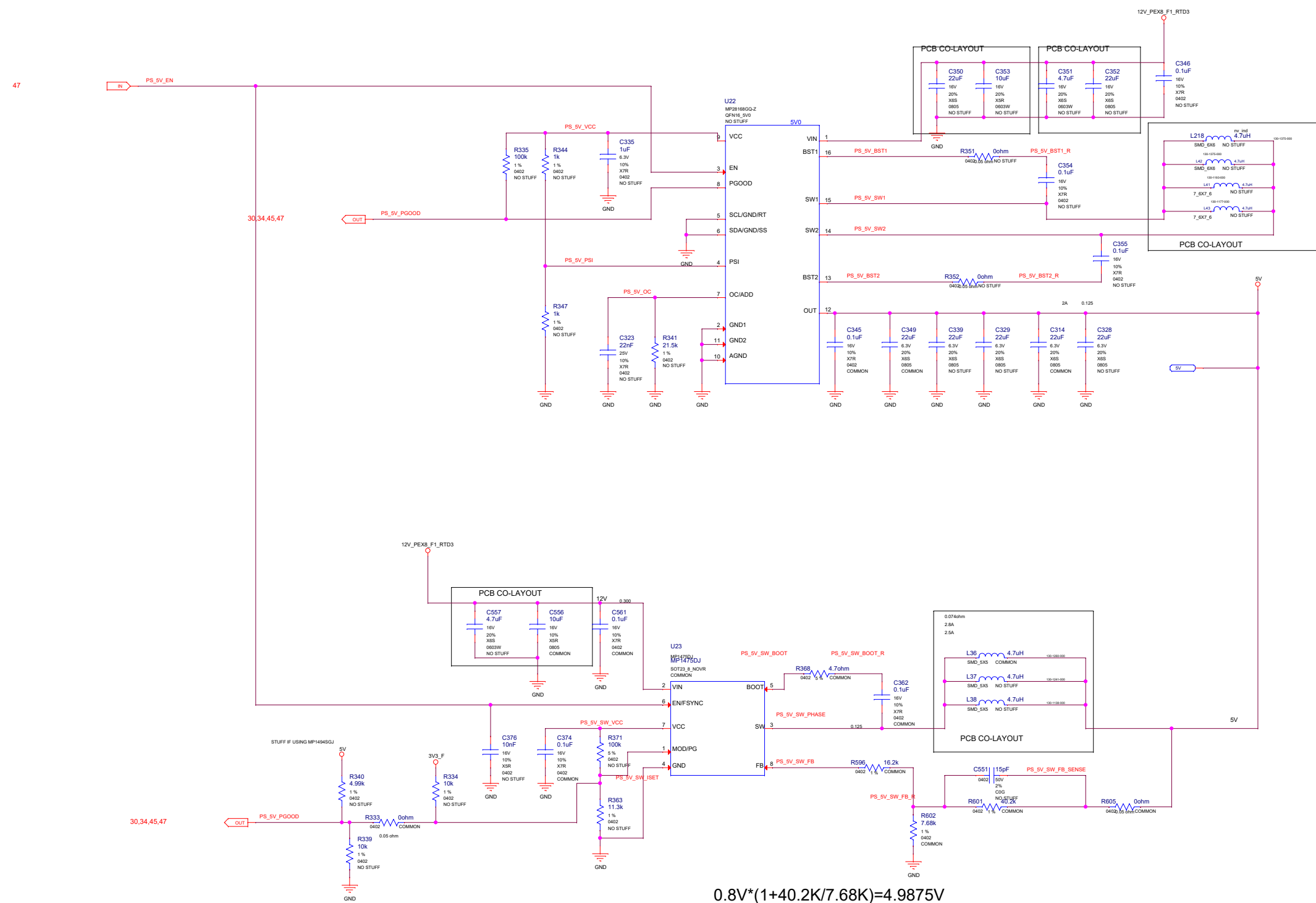
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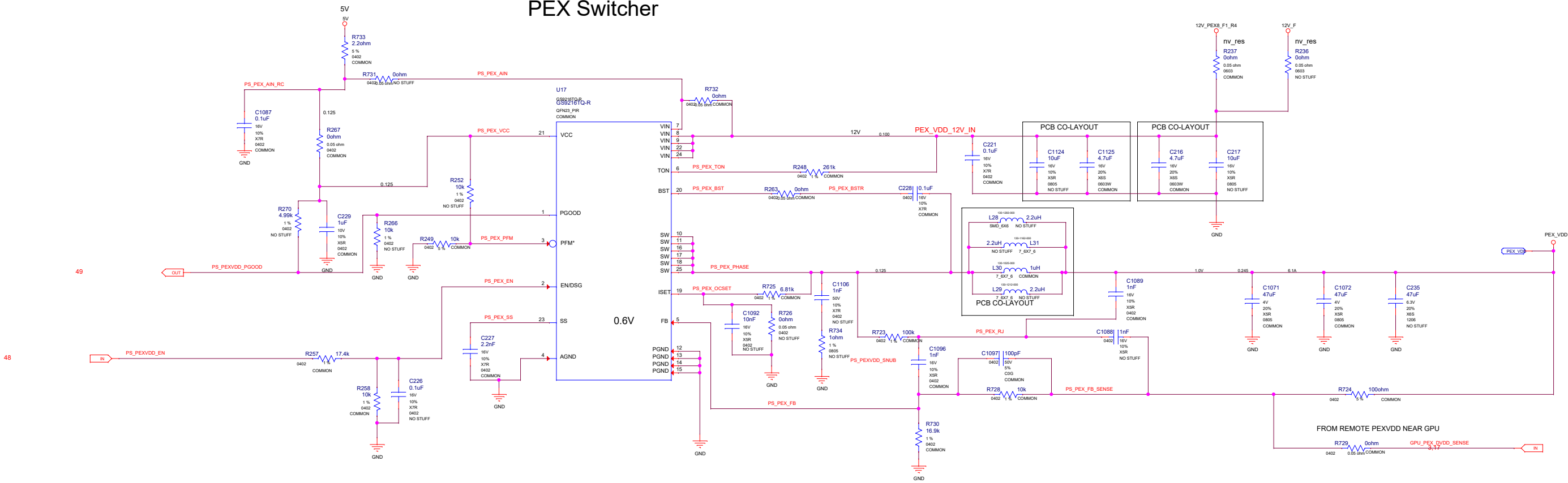
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PEX Switcher

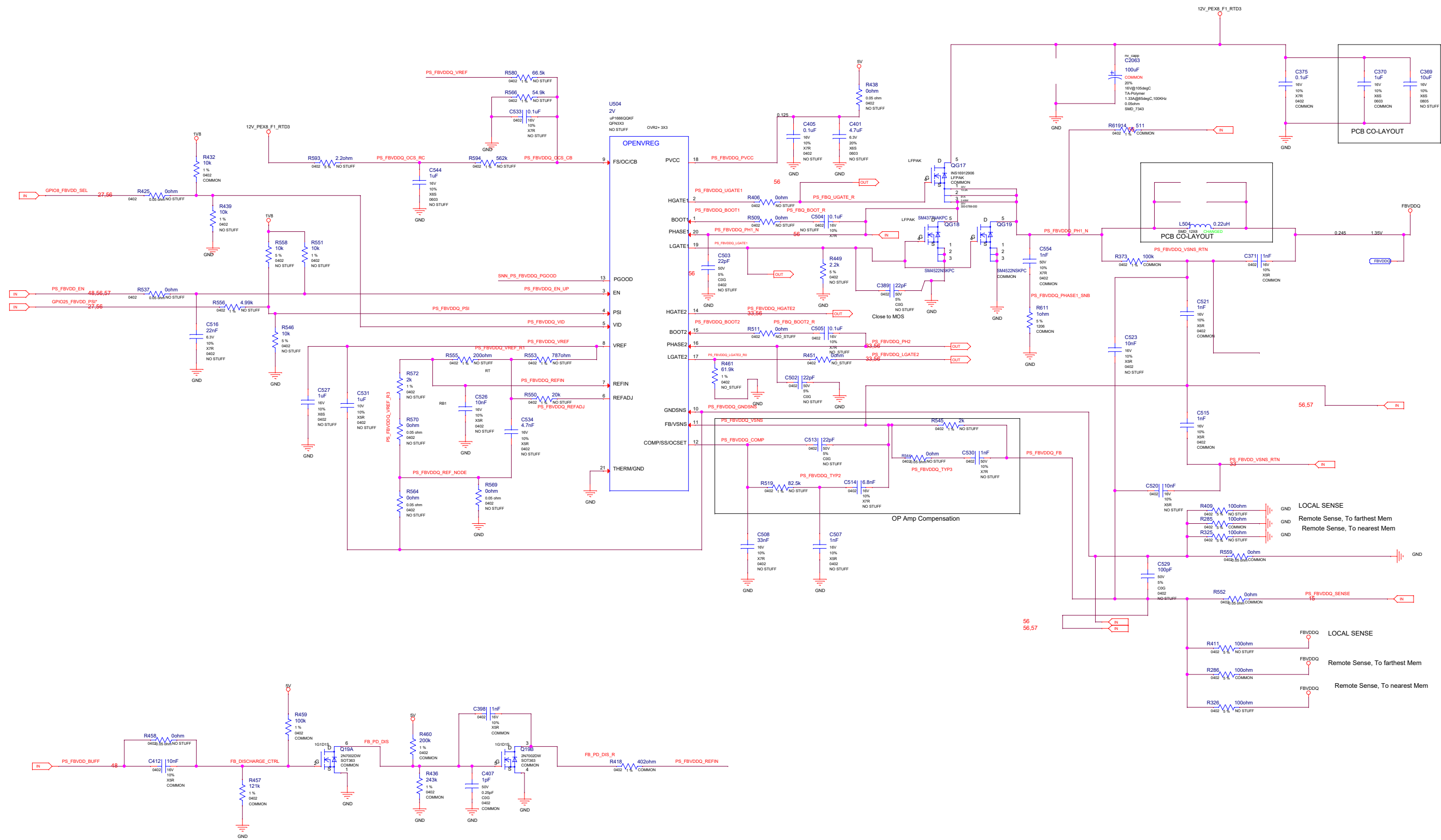


$0.6V \cdot (1 + 10K / 16.9K) = 0.955V$

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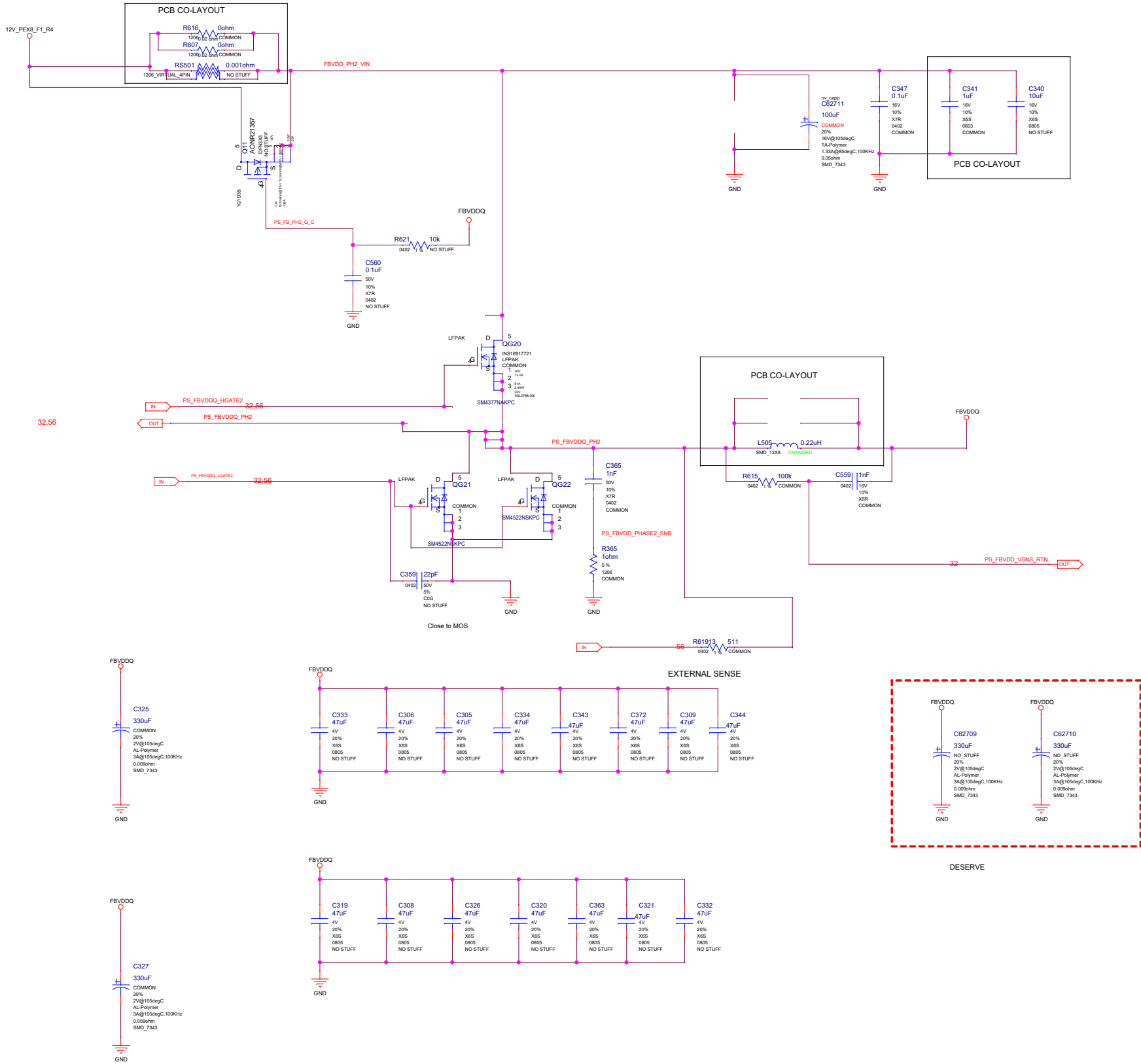


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FBVDD PH2 INPUT ANTI-BACKDRIVE



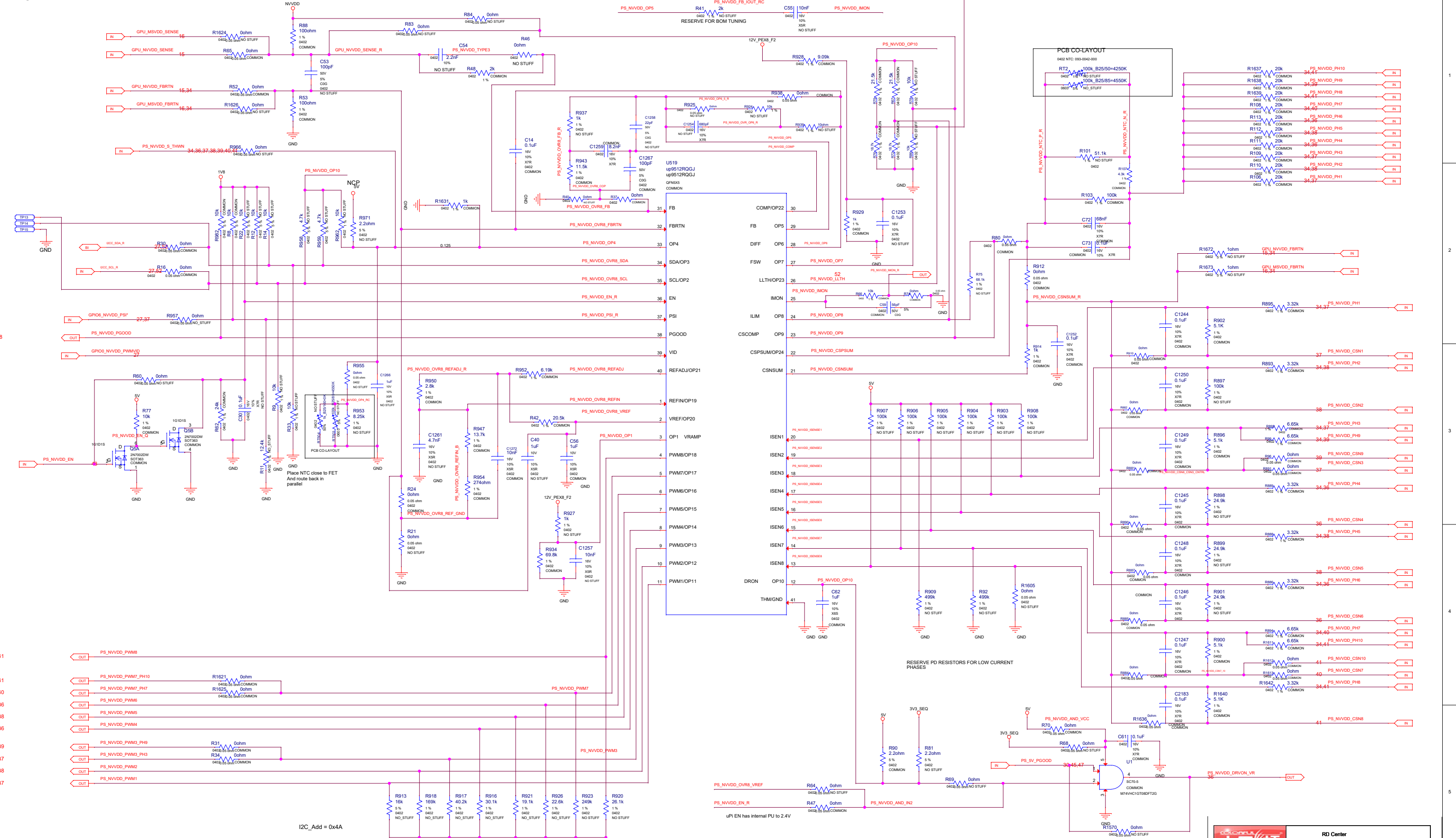
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PAGE DETAIL	PS: NVVDD Controller

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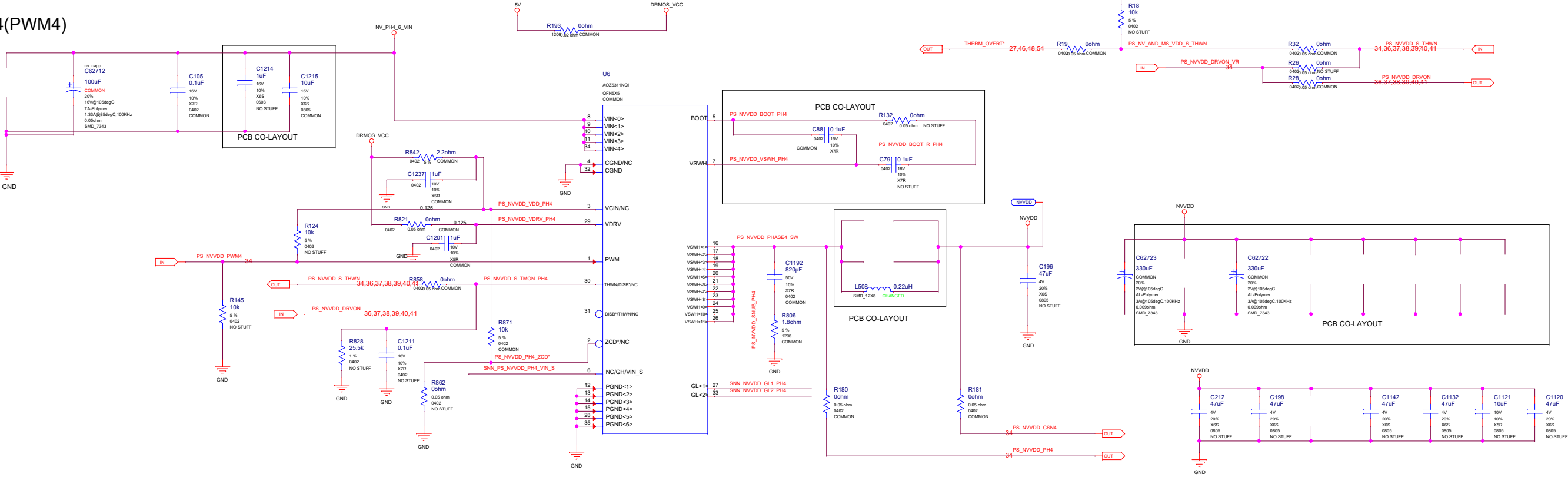
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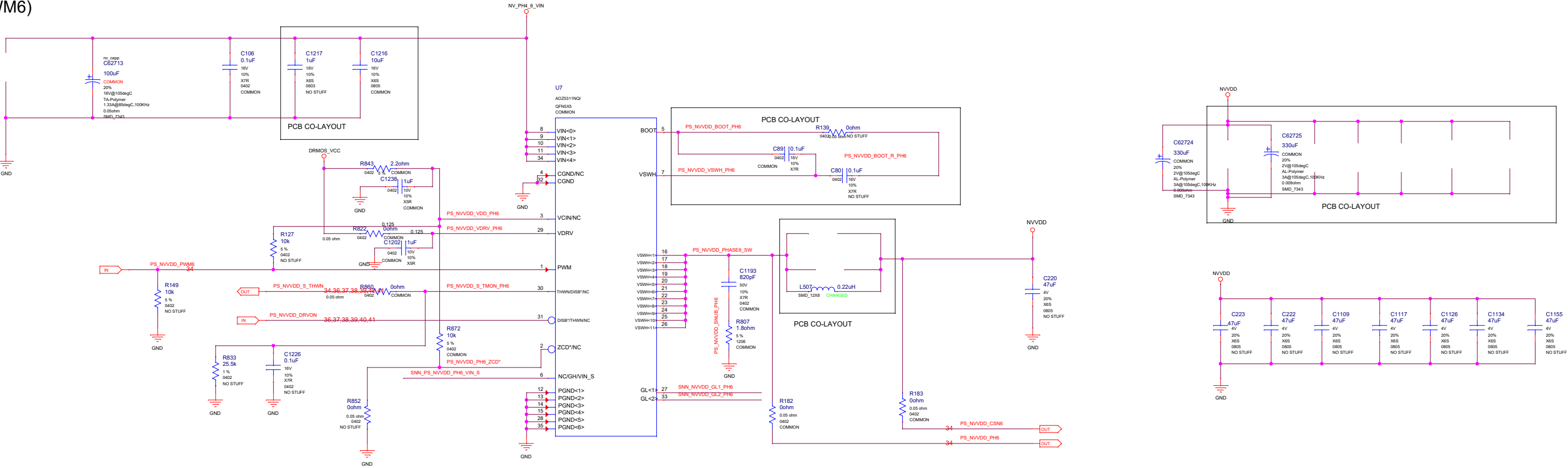
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NVVDD PH4(PWM4)



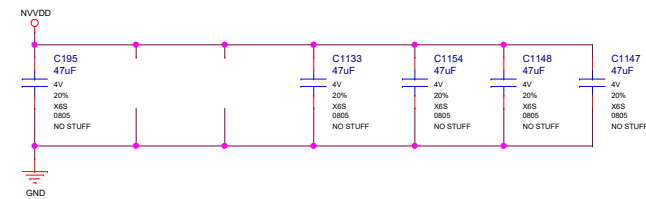
NVVDD PH6(PWM6)




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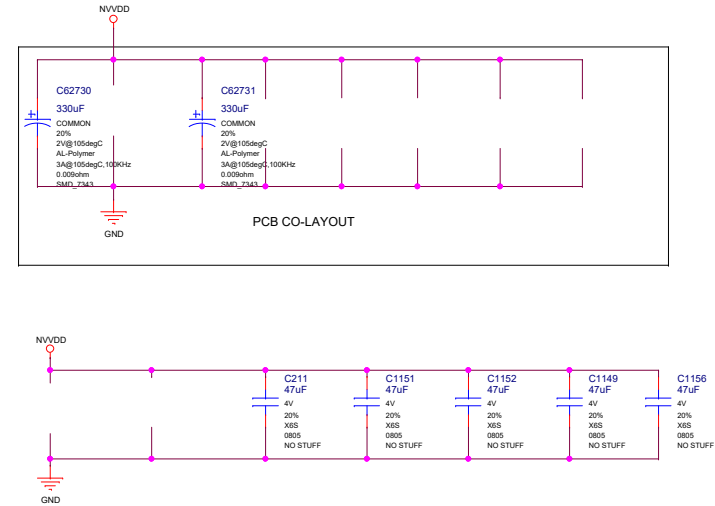
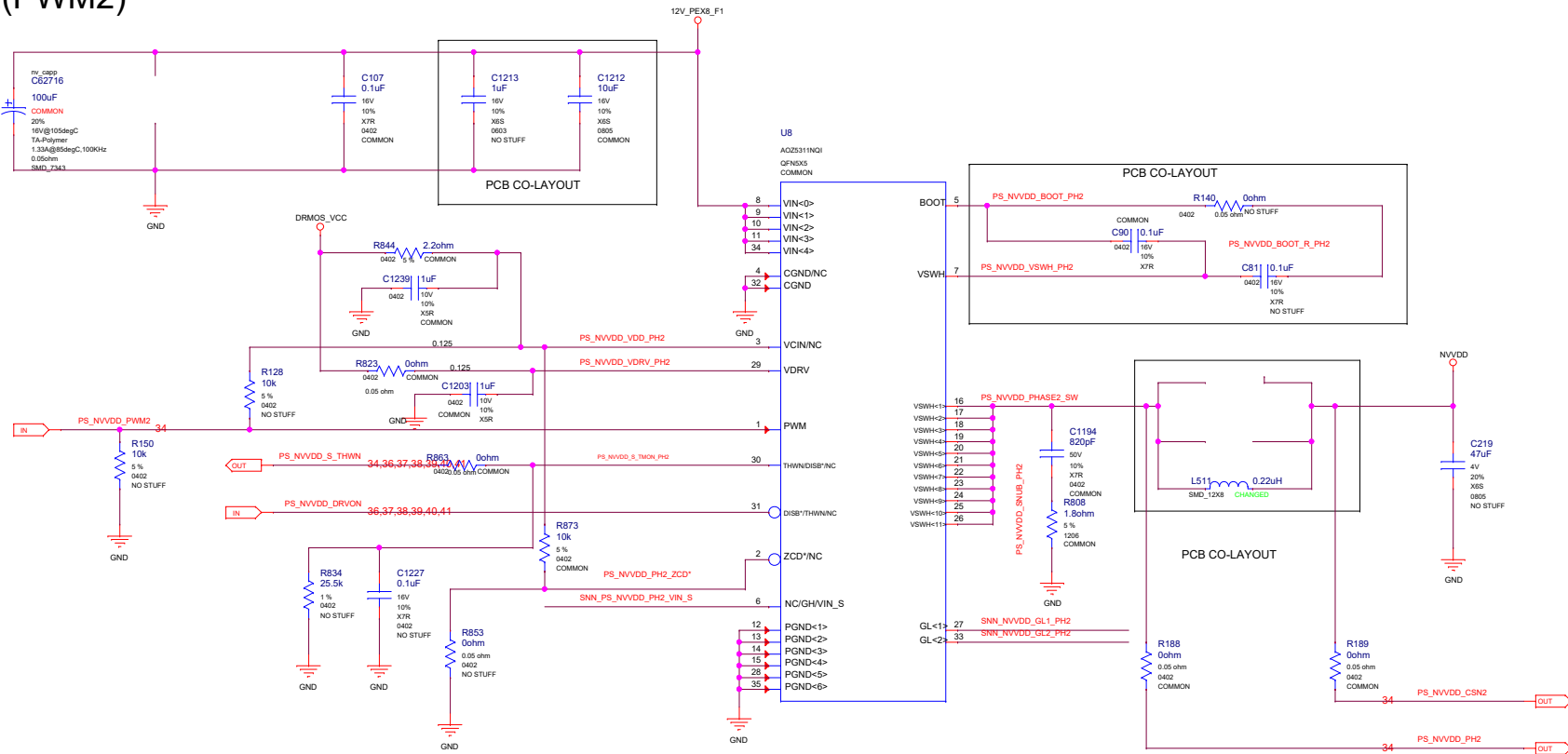


PCB CO-LAYOUT

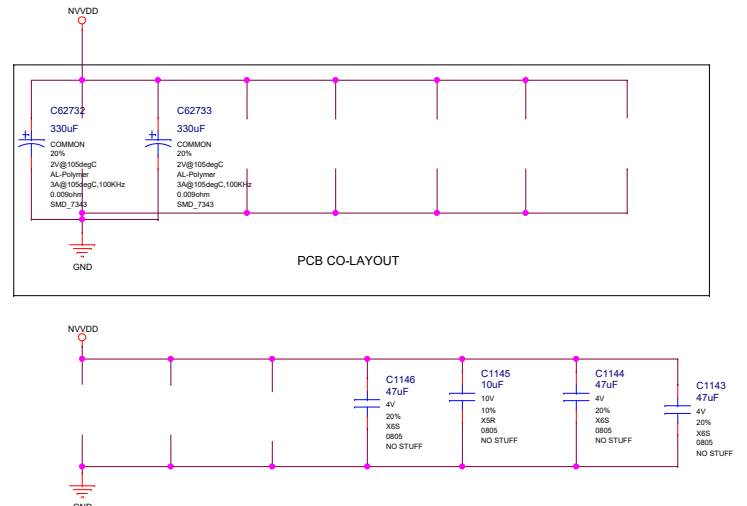
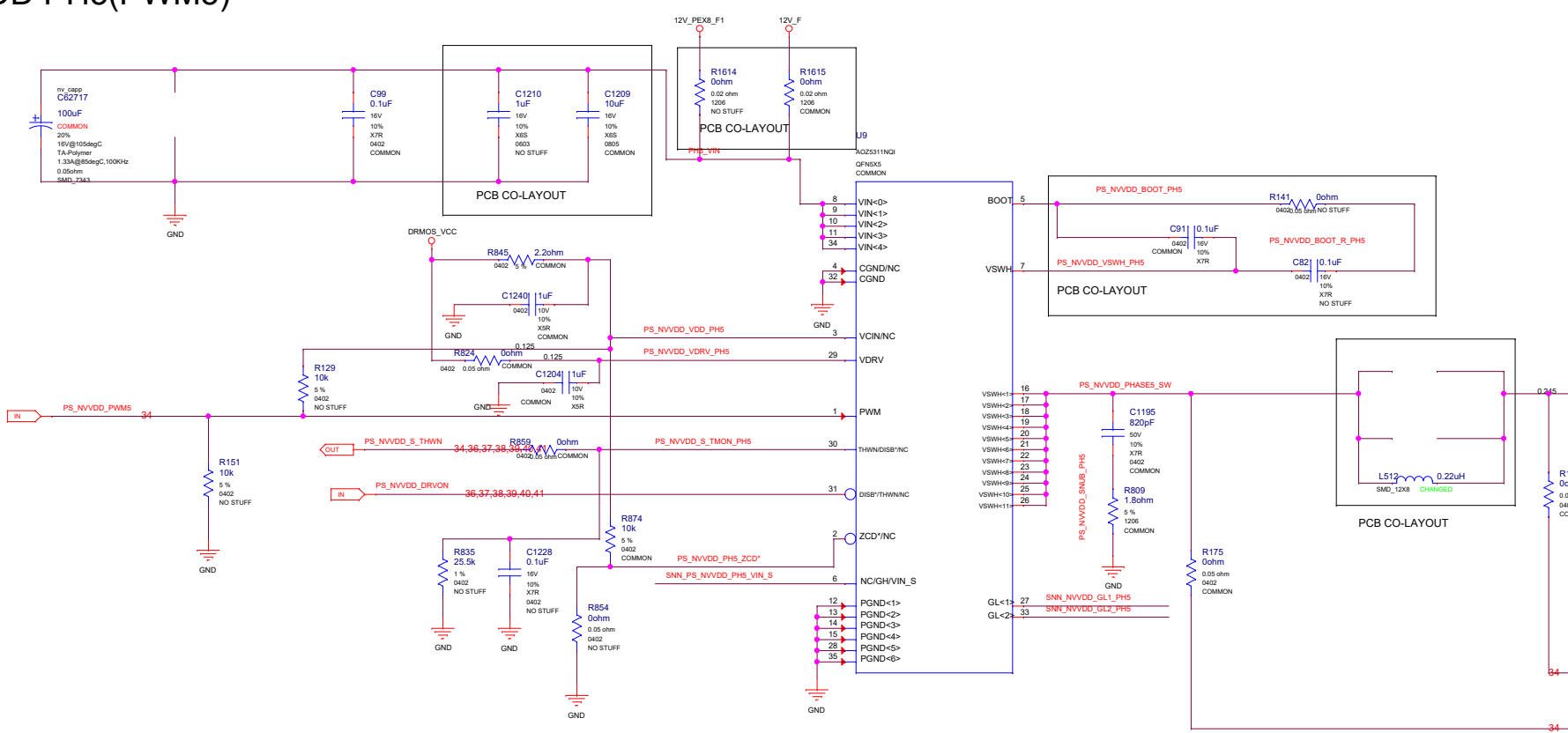
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NVVDD PH2(PWM2)



NVVDD PH5(PWM5)

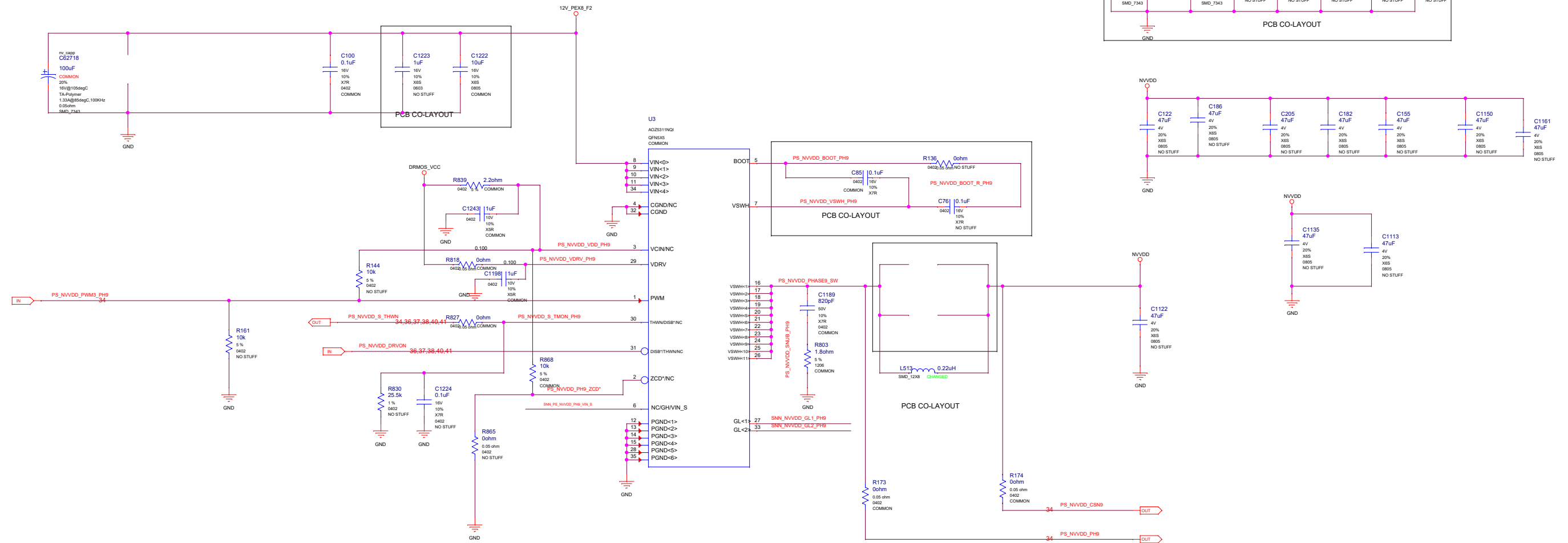


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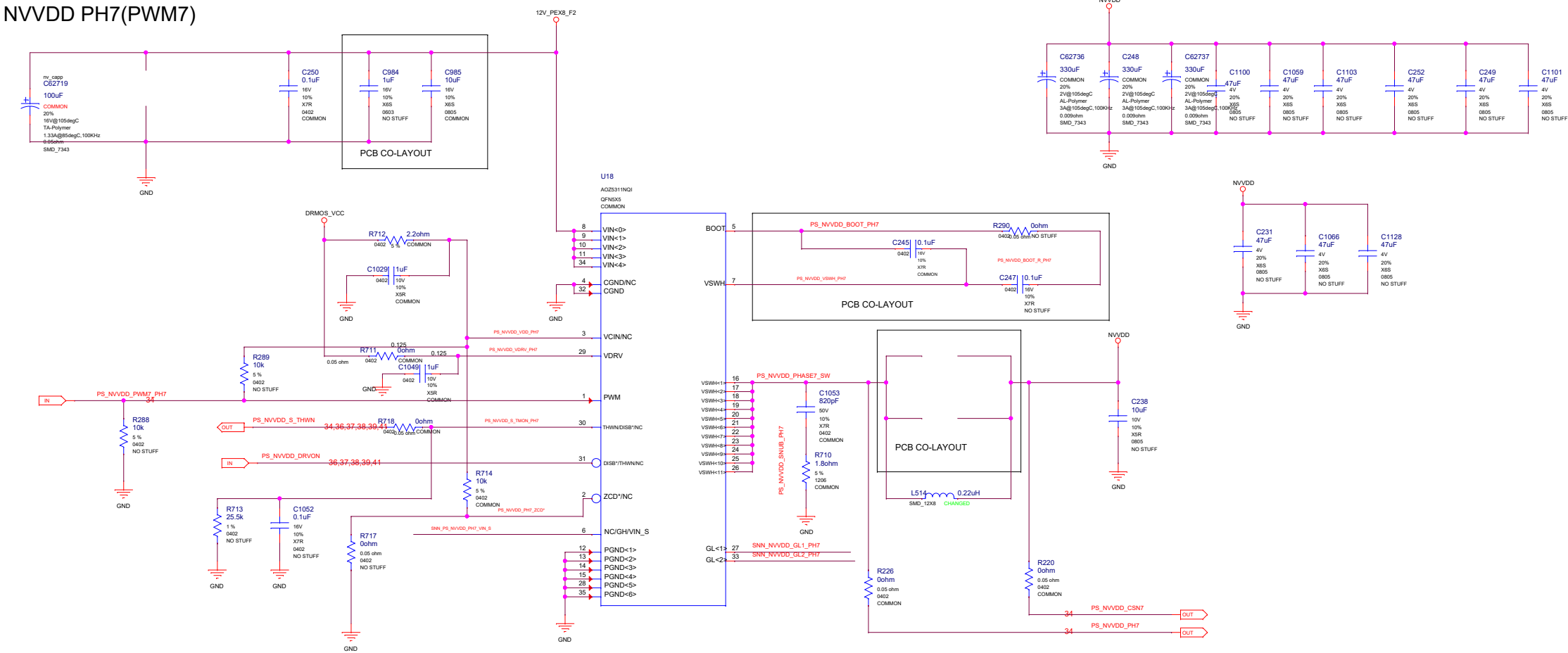
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PAGE DETAIL		PS: NVDD P#9		Size Custom Document Number GA104H8-E70 Rev A	
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NVVDD PH7(PWM7)



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ASSEMBLY
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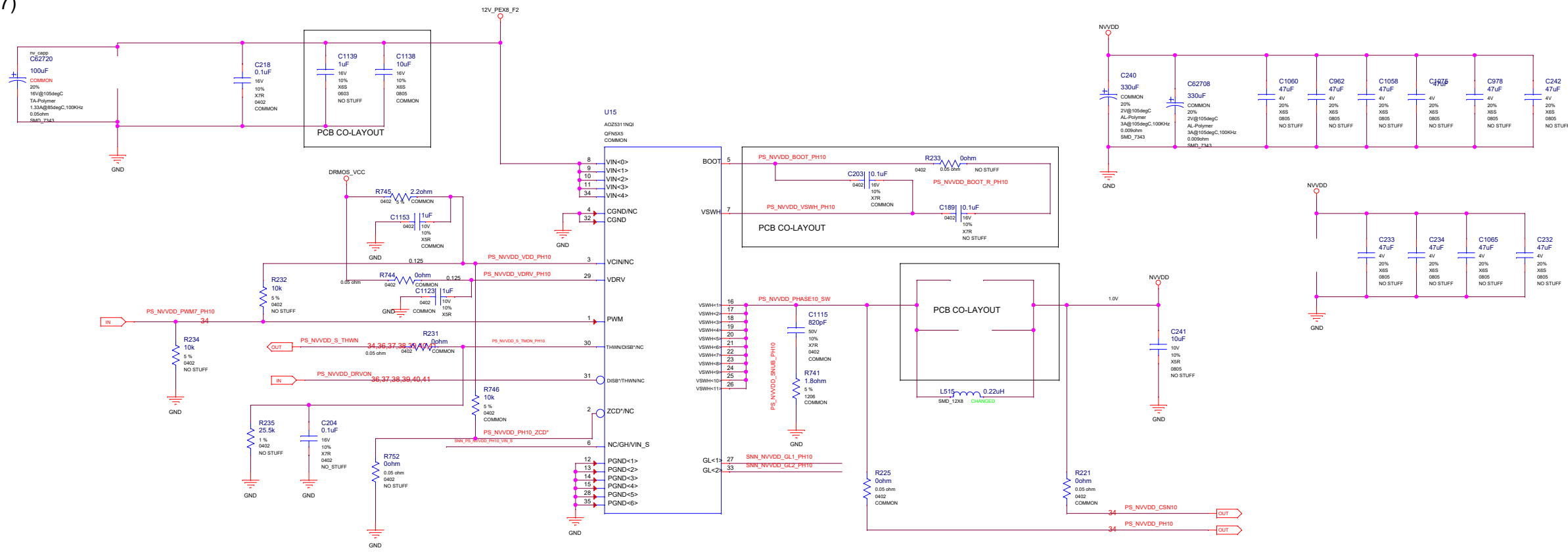
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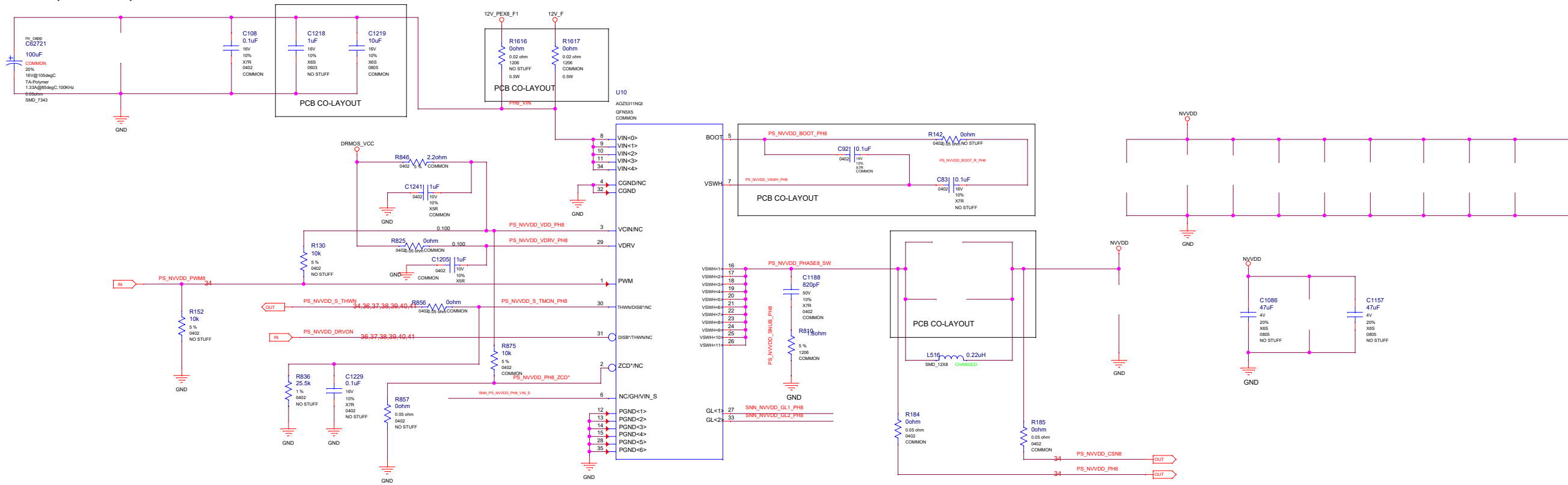
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Page41: NVVDD PH10 & 8
NVVDD PH10(PWM7)



NVVDD PH8(PWM8)

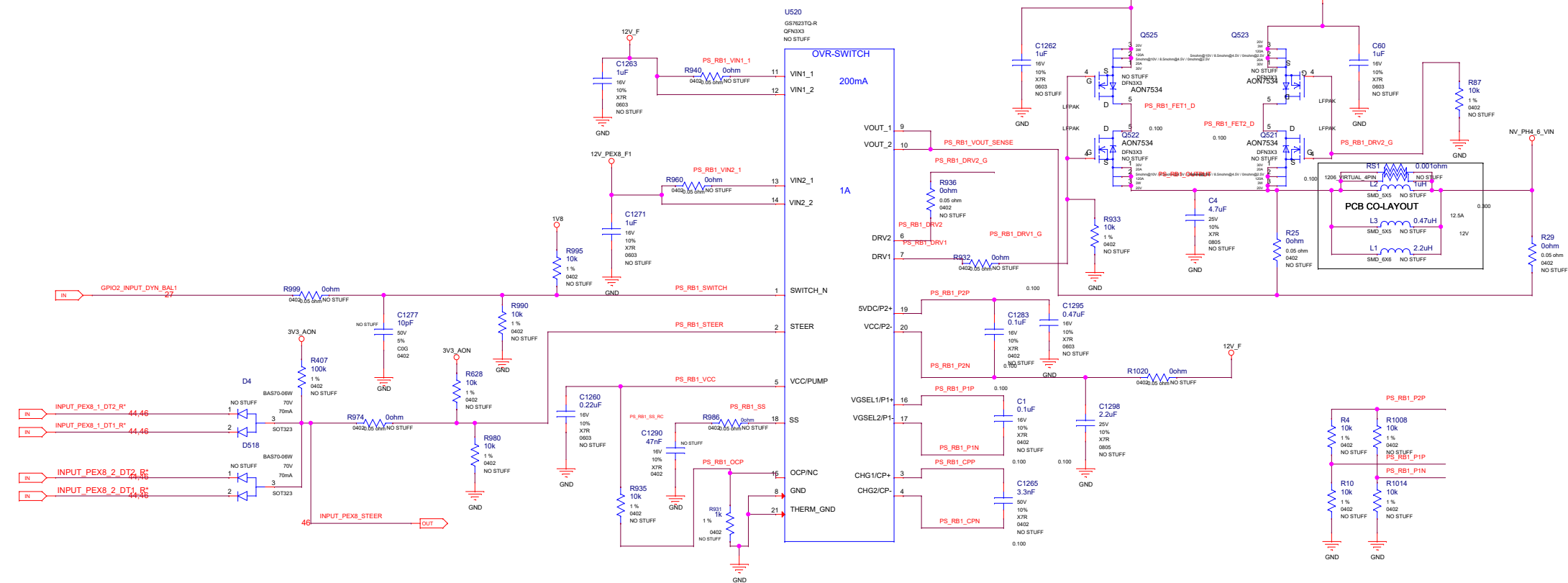
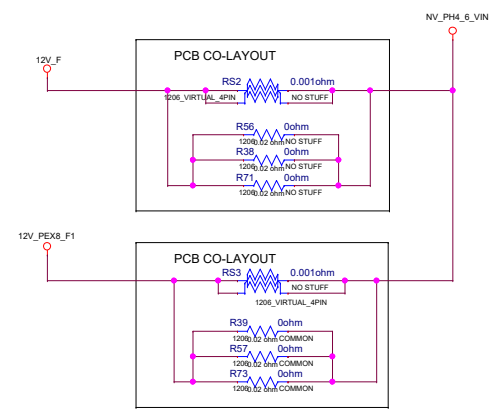
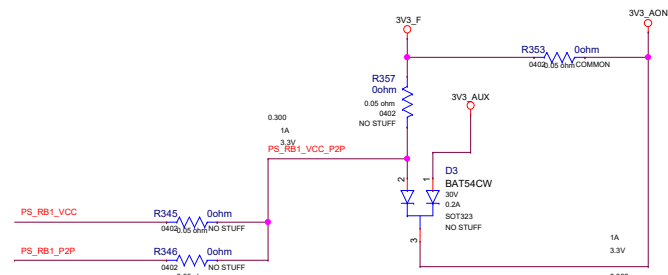


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Page42: Input Power Balancing Switcher

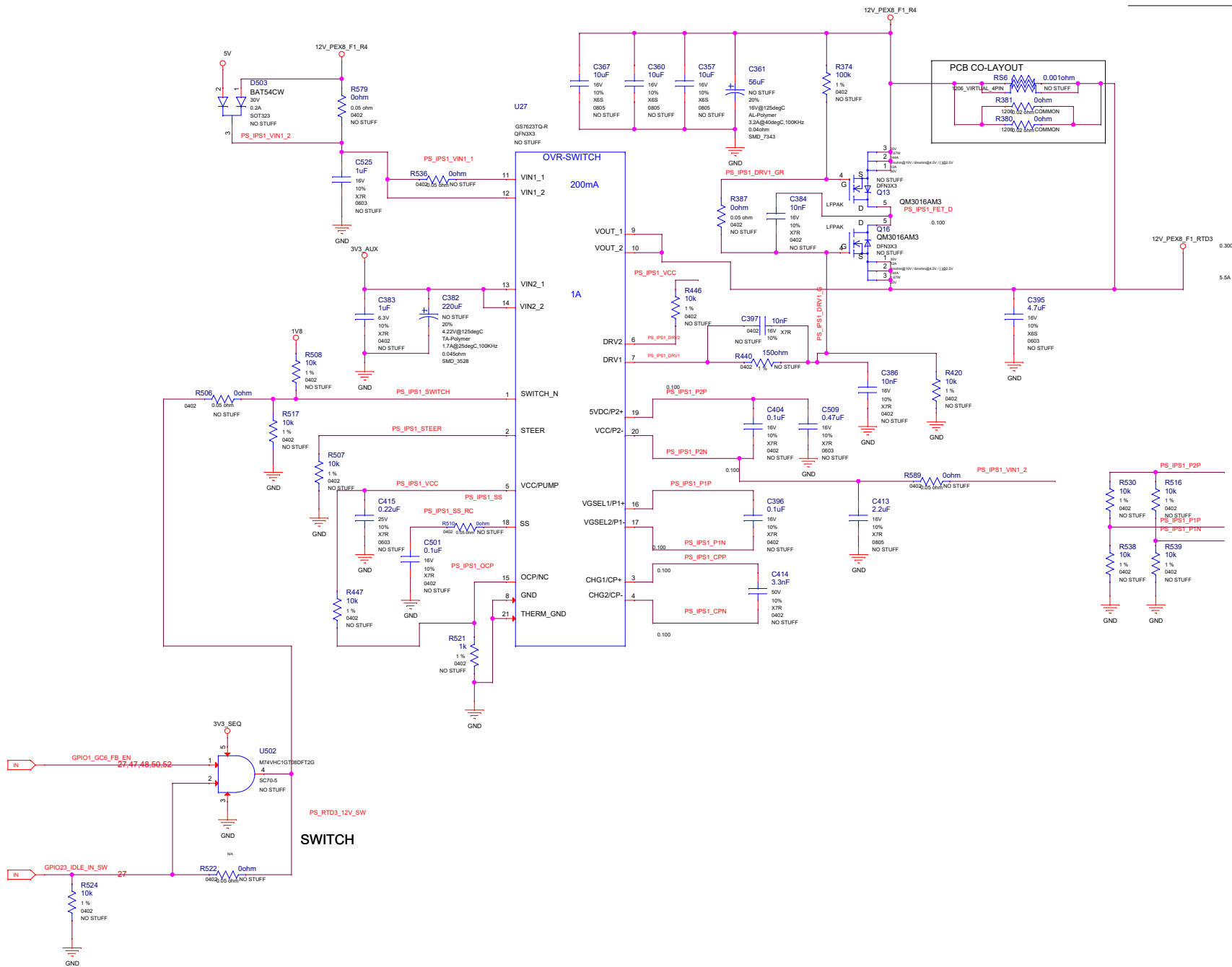


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PAGE DETAIL	PS: OVRS_INPUT POWER BALANCE

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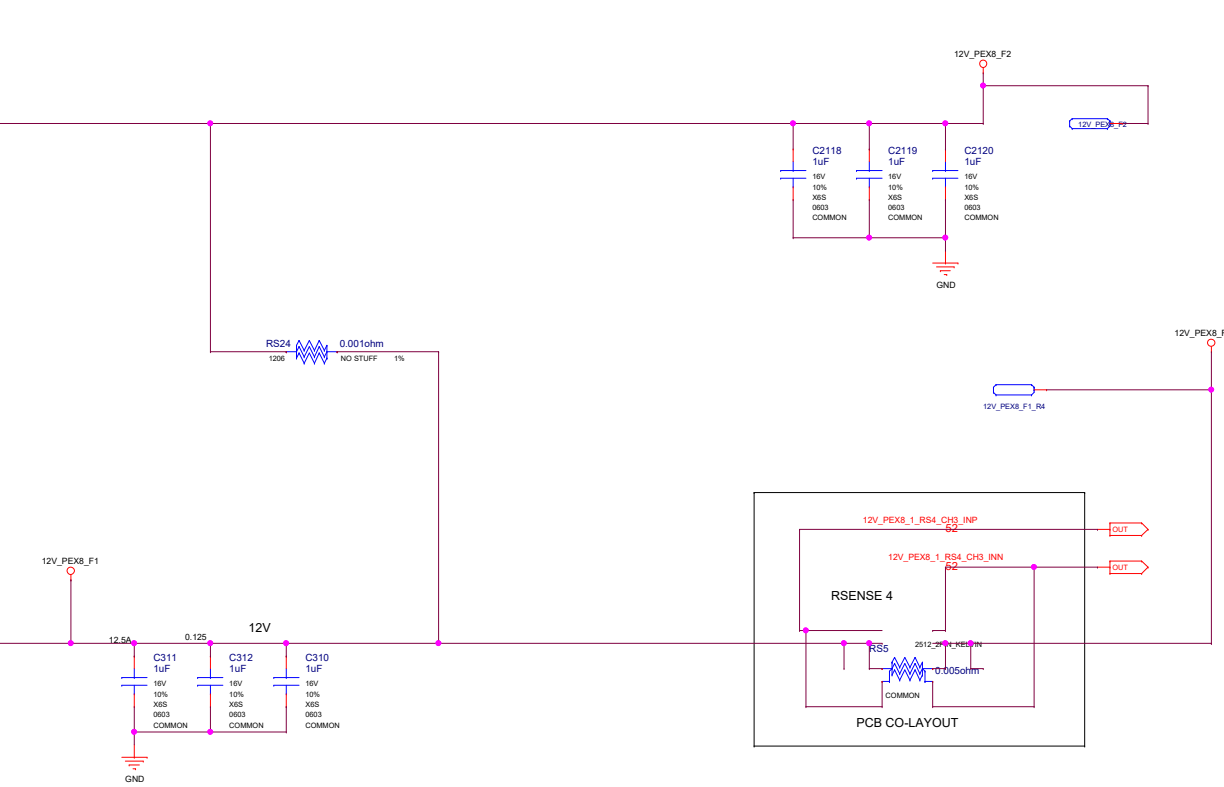
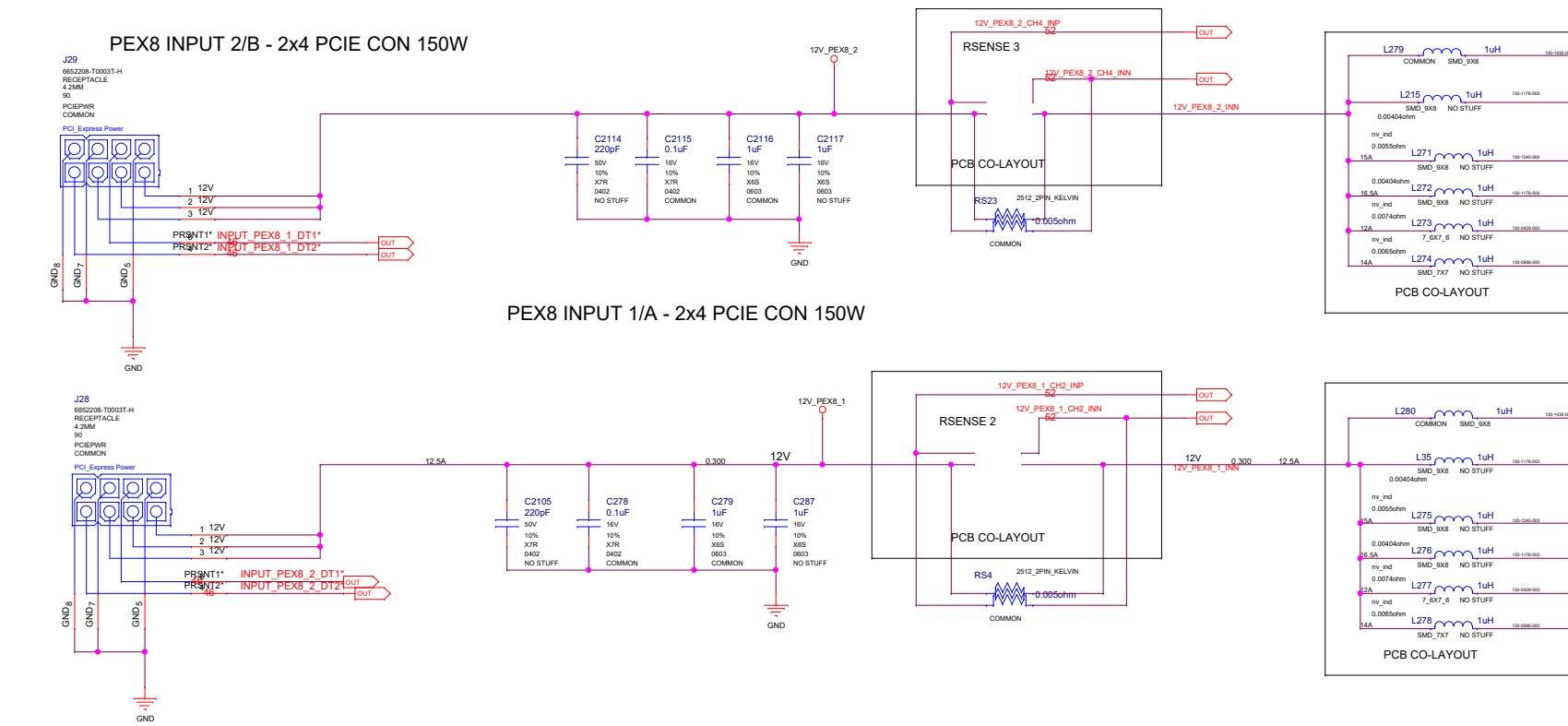
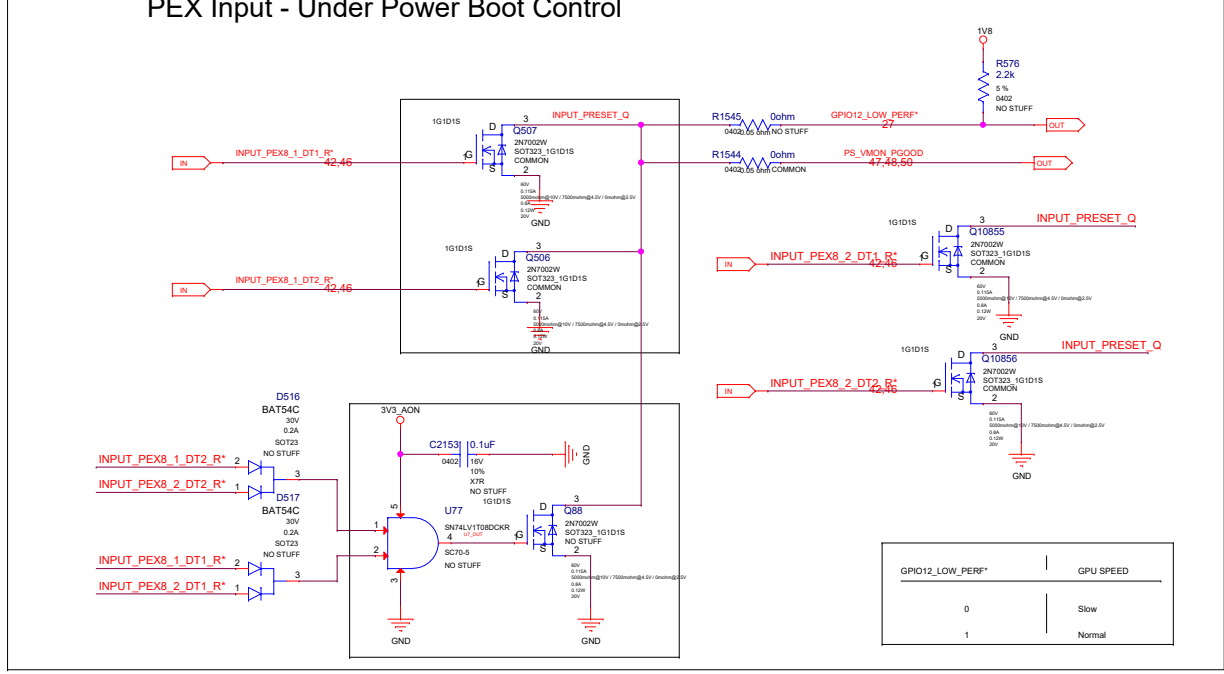
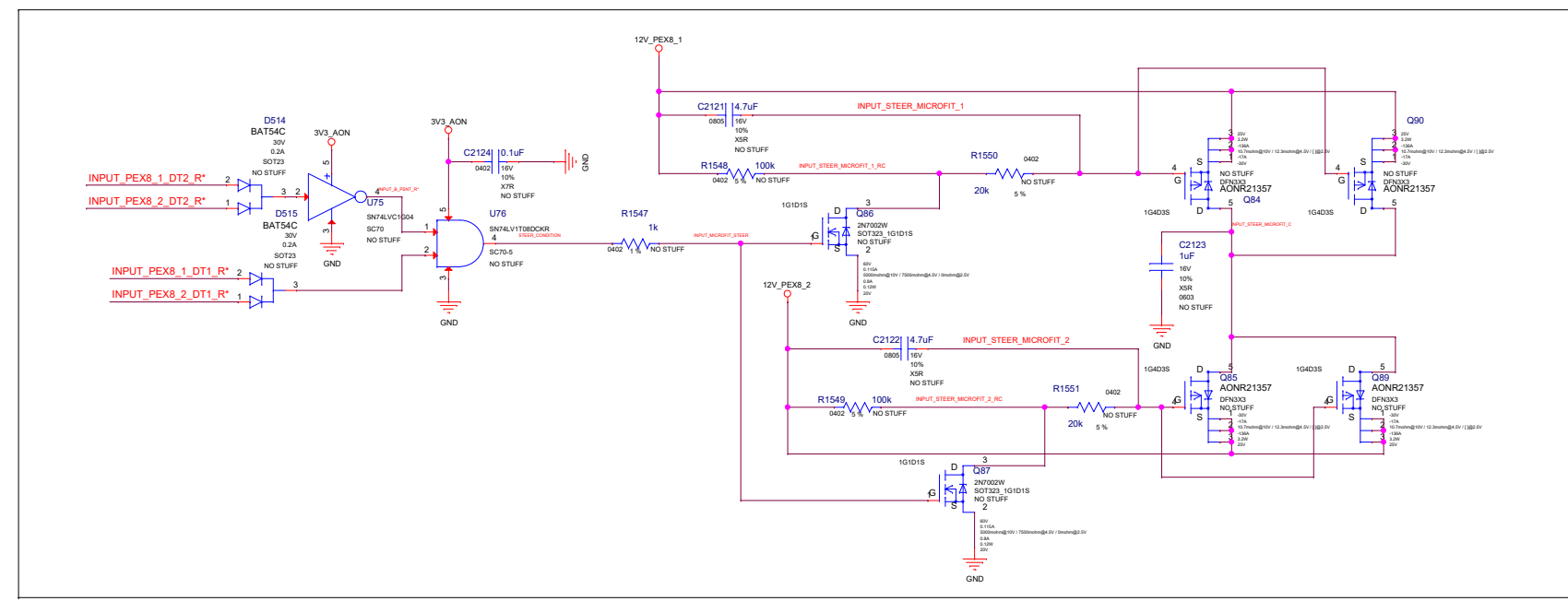
GPIO1	GPIO29	SWITCH	VOUT	SWITCH	VOUT
0	0	0	12V	0	VOUT = VIN1
0	1	0	12V	1	VOUT = VIN2
1	0	0	12V		
1	1	1	3V3A		



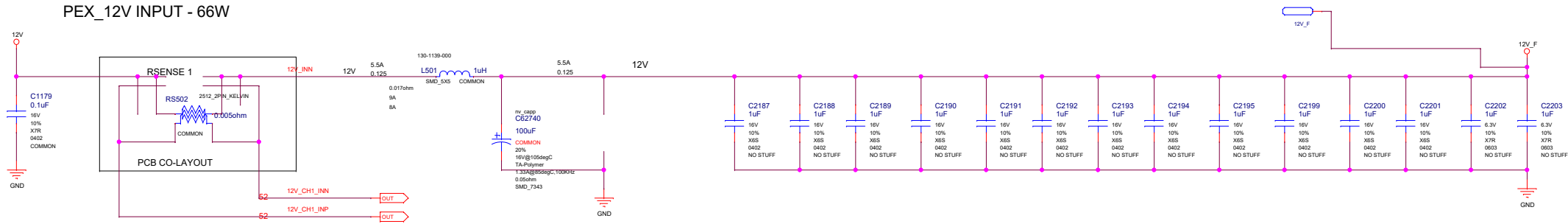
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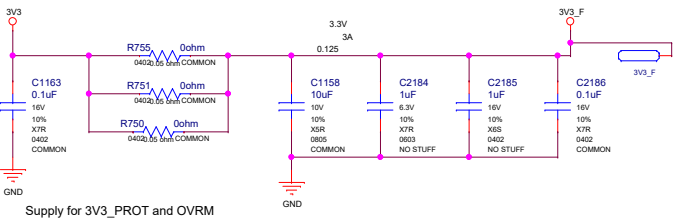
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PEX_12V INPUT - 66W

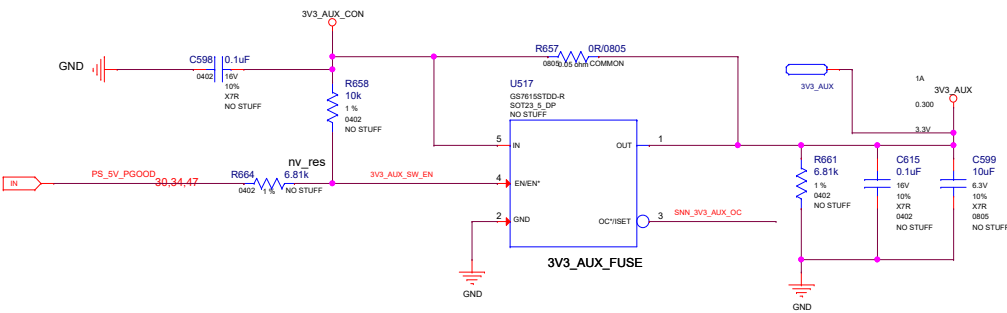


PEX 3V3 INPUT - 10W



Supply for 3V3_PROT and OVRM

3V3_AUX




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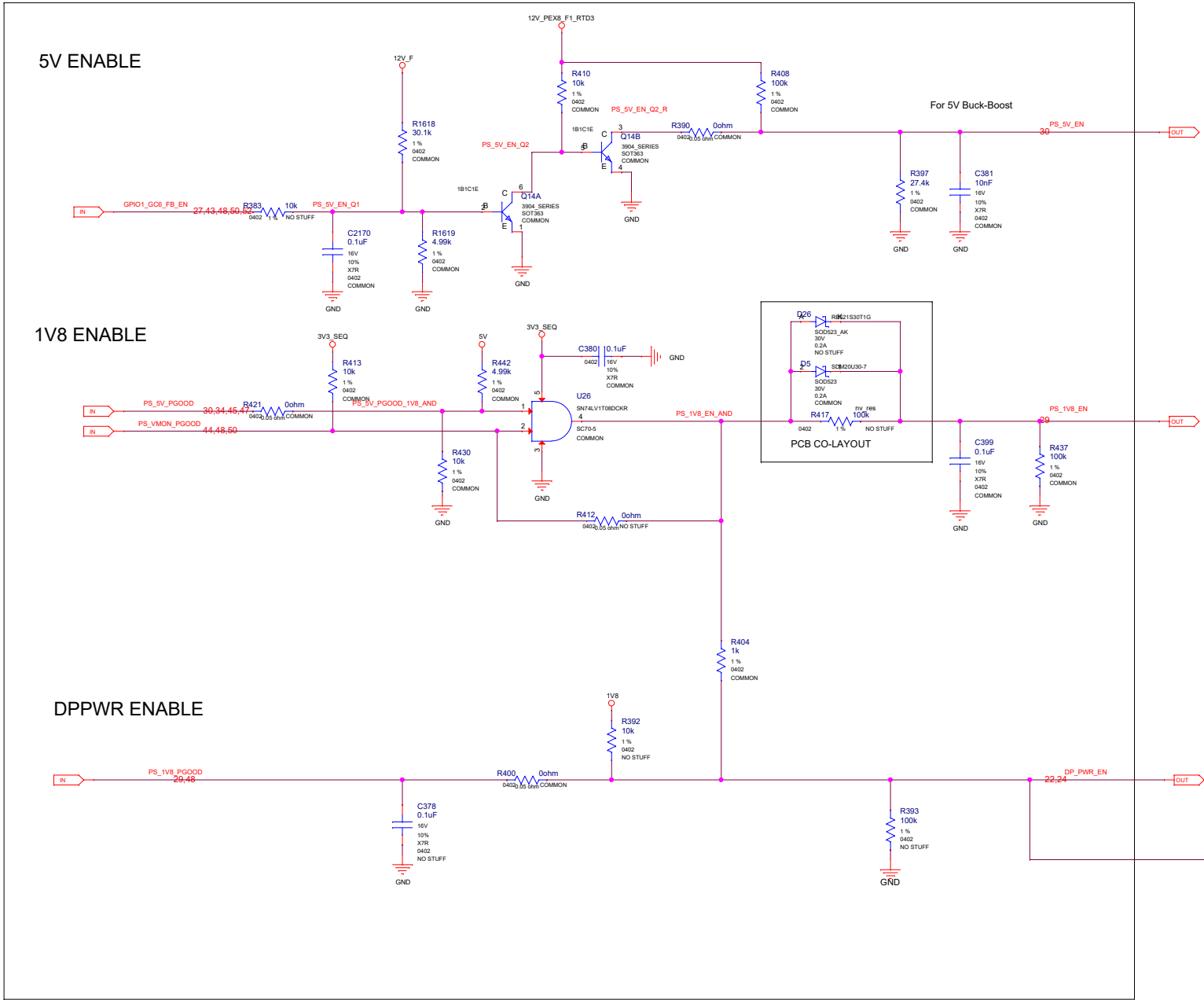
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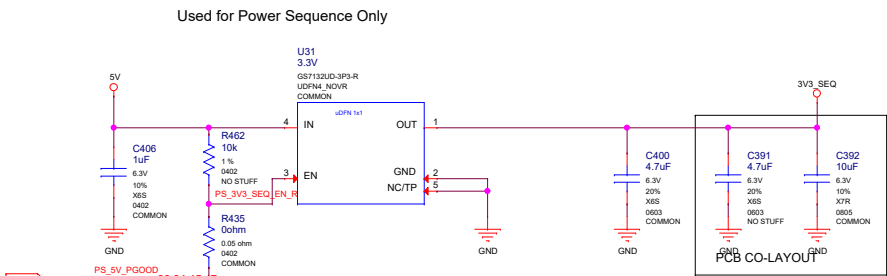


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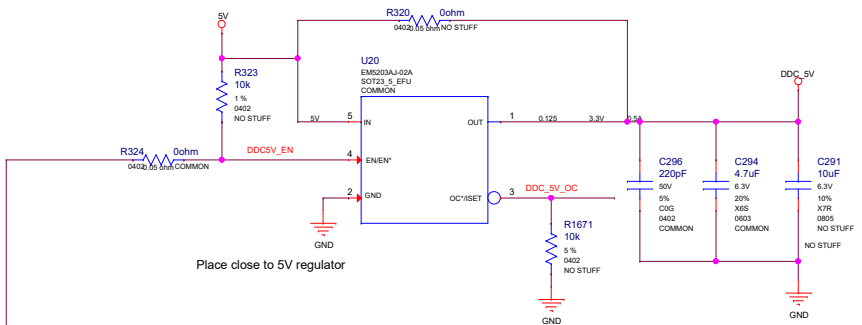
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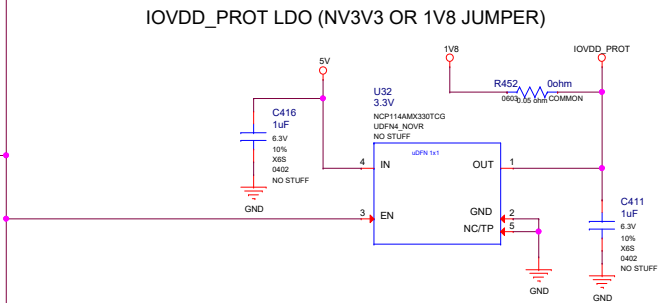
3V3_SEQ



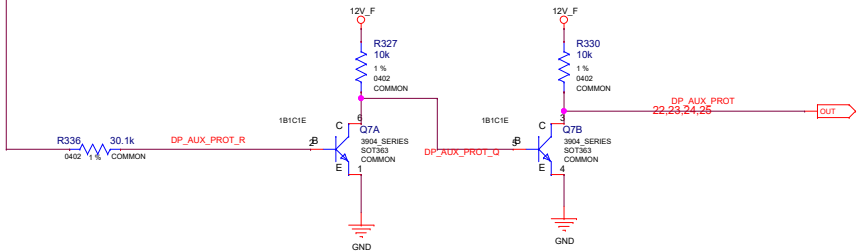
DDC_5V



IOVDD_PROT



DP_AUX PROTECTION



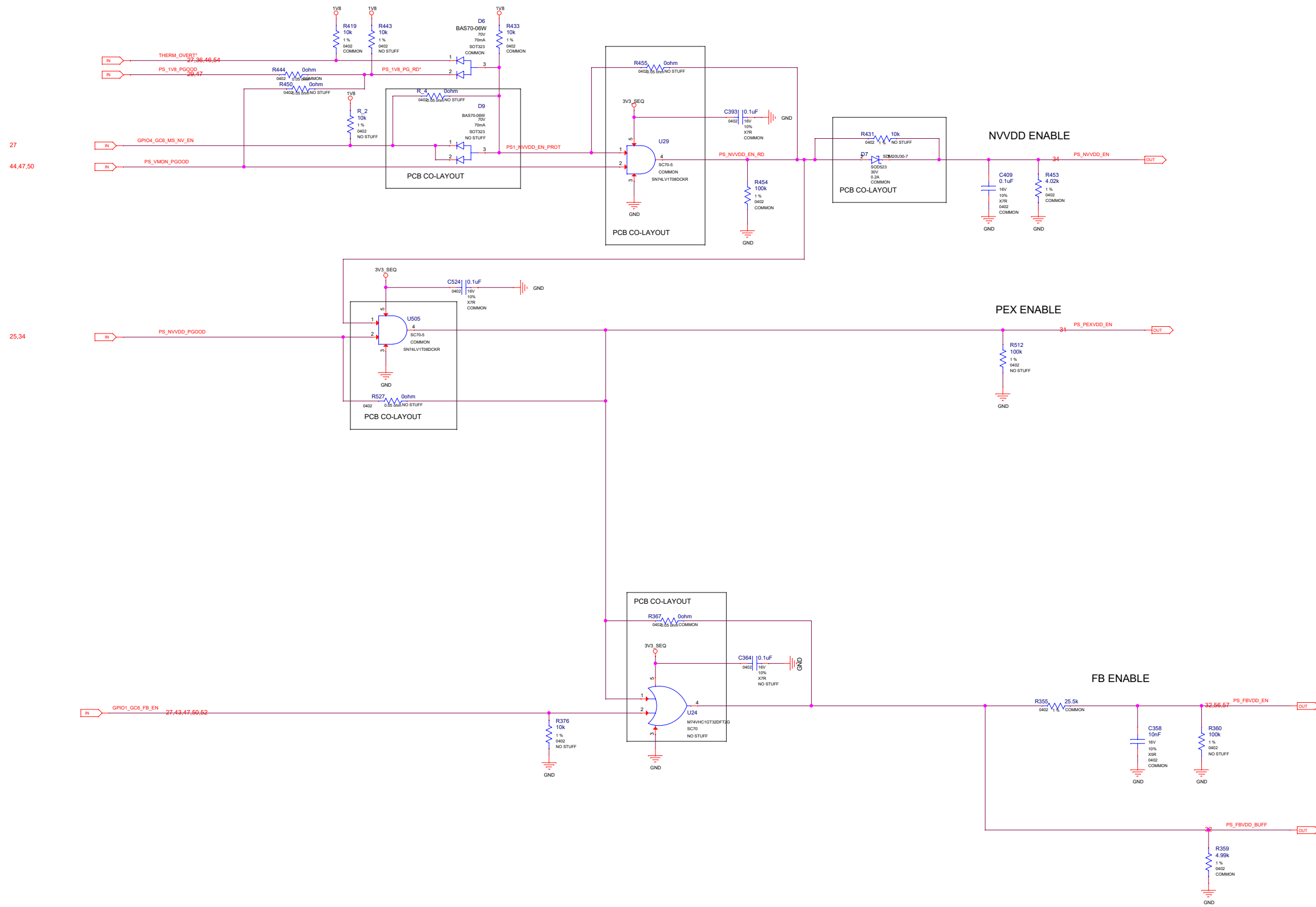
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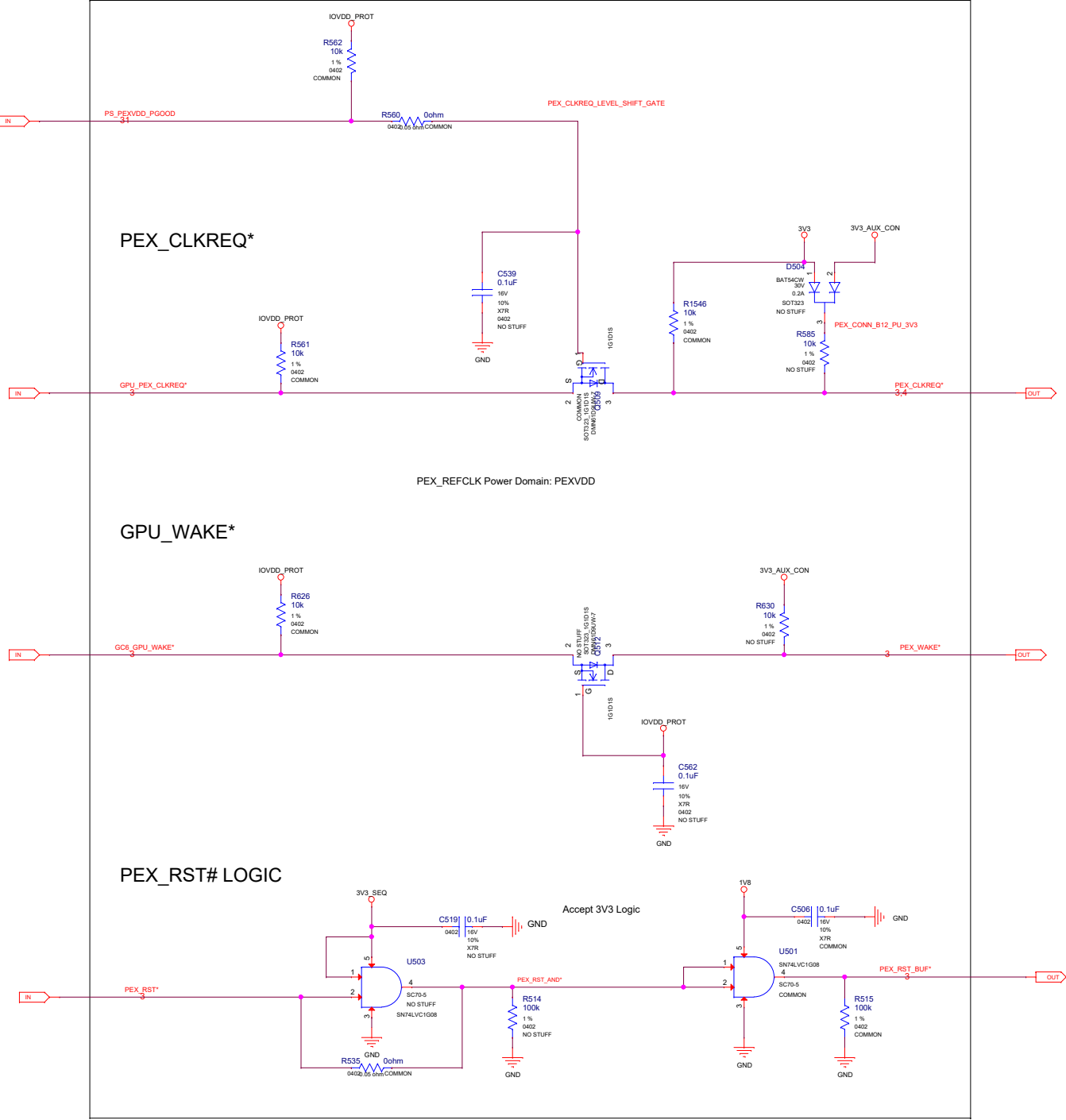
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NVVDD, PEX, FBVDDQ ENABLE

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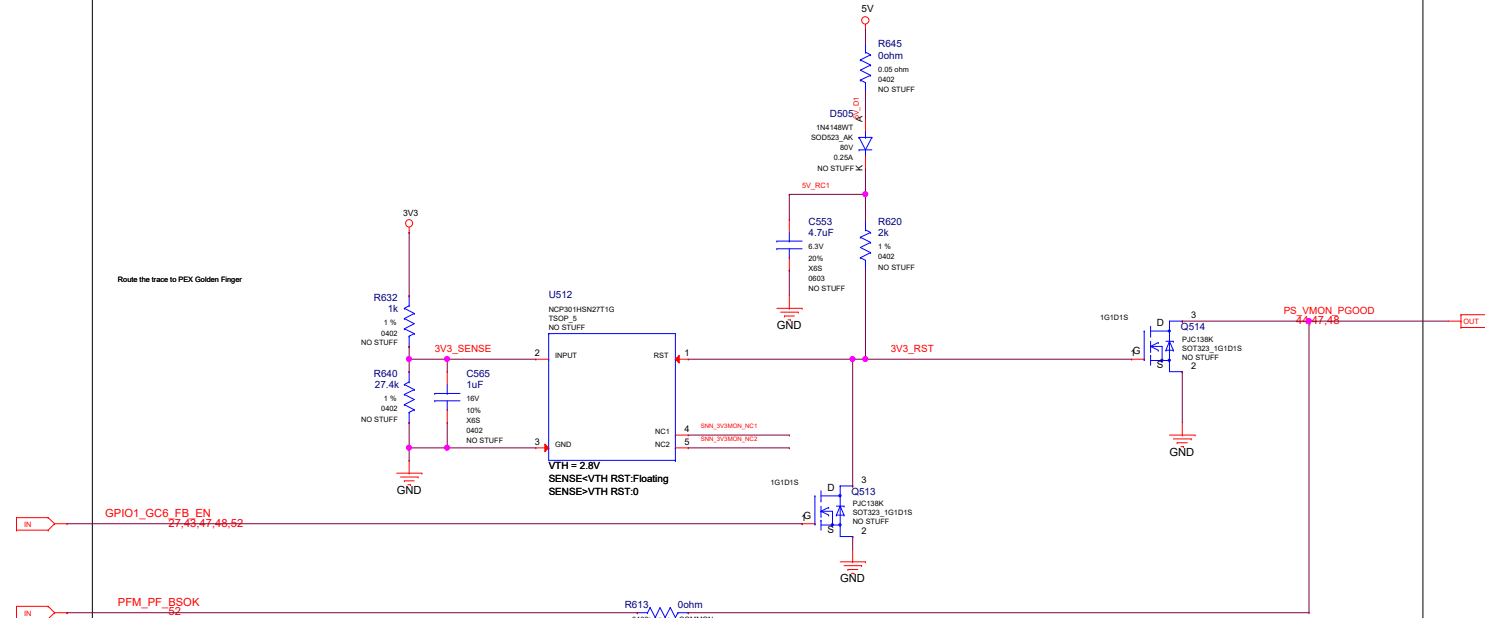
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3V3PEX Voltage Monitor

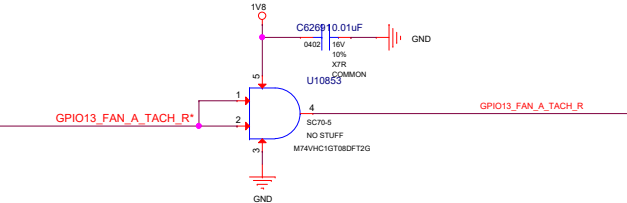
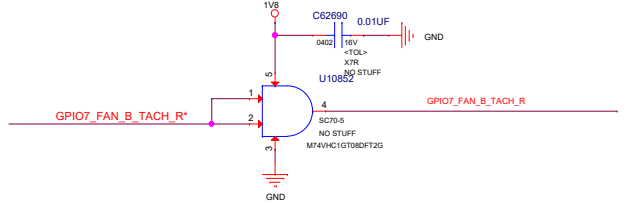
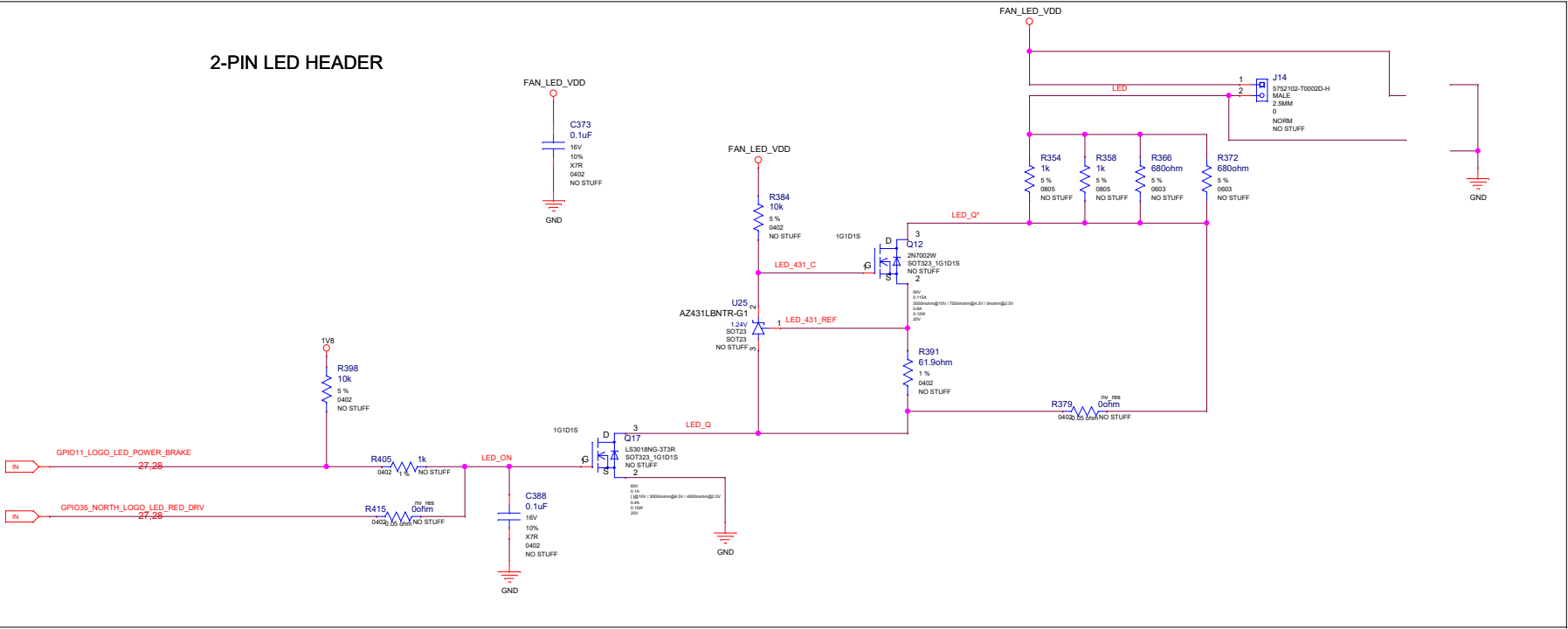


BOM Configuration

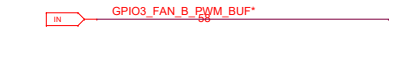
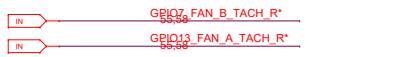
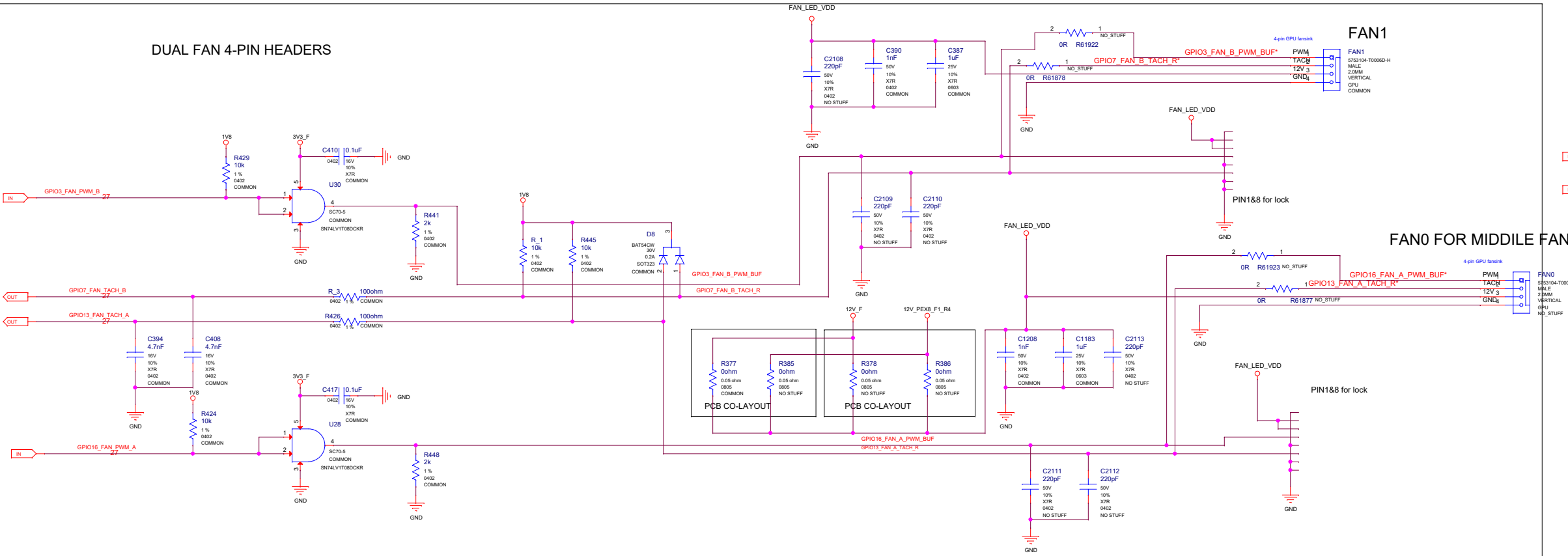
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NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vih
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence, Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)


2-PIN LED HEADER



DUAL FAN 4-PIN HEADERS



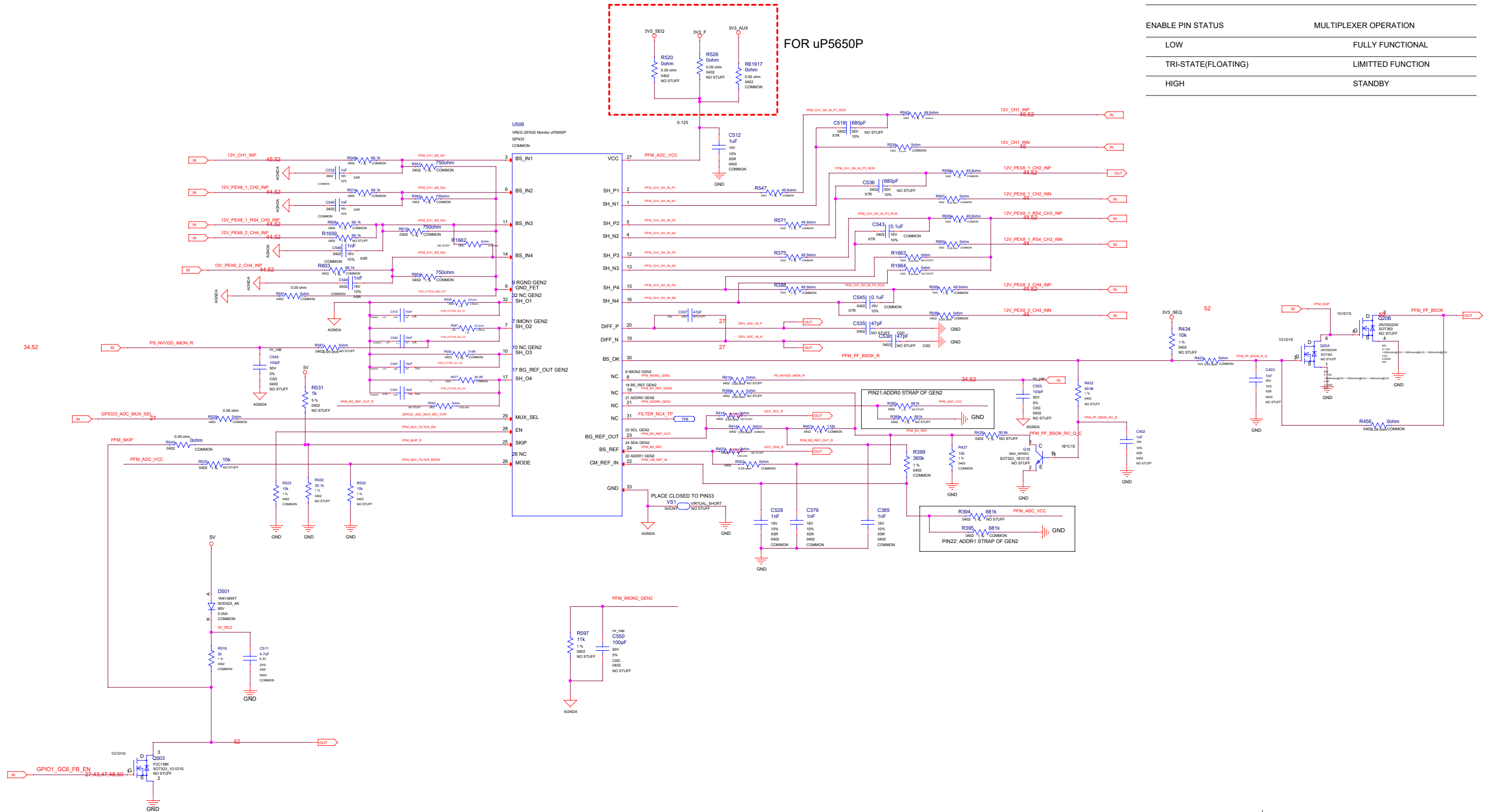
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Page52: OVRM_PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

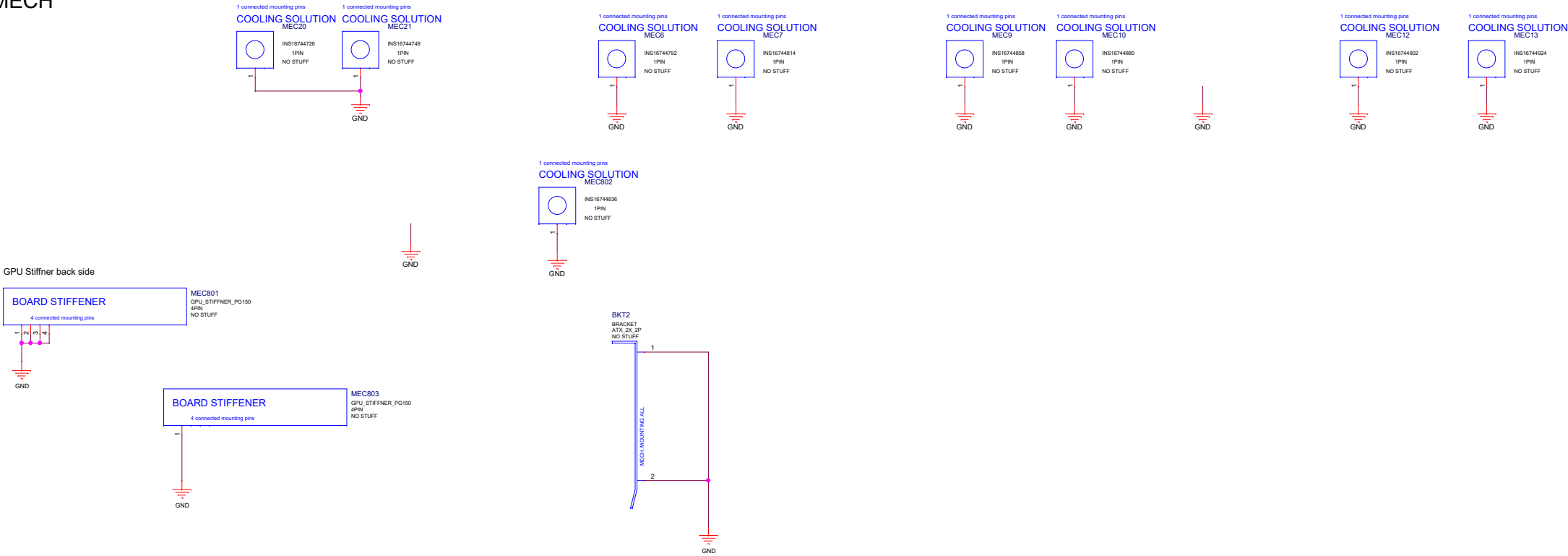
ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS:OVRM PWR SENSE


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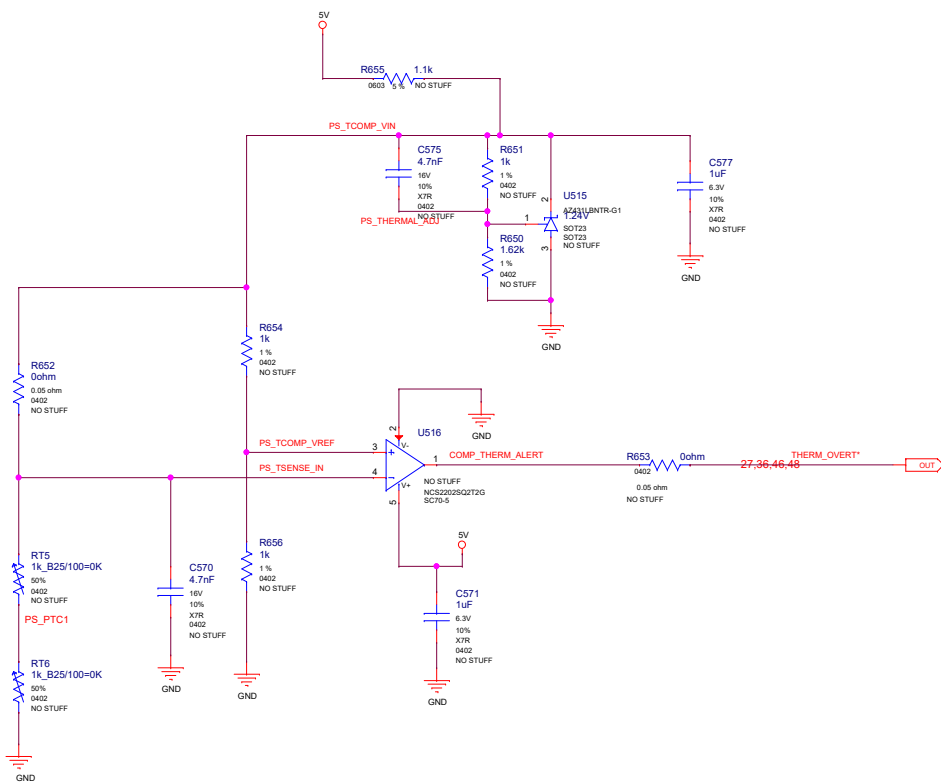
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
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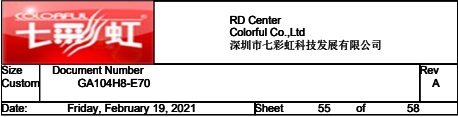
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NCP81273 EN VIH >1.5V, VIL < 0.7V
UP9509/10 EN VIH >1.2V, VIL < 0.6V
RT8817A EN VIH >1.2V, VIL < 0.6V



