P78, NV17, 4Mx32 DDR, 64MB, RGB, TV-out, ~~video capture~~, AGP4X

PCI DEVICE ID = 0X171 FOR NV17-128D.

PRIMARY ** VGA1 DAC A ** LFH1 TMDS A I2C1.
SECONDARY ** S-VIDEO/TV-OUT DAC B ** LFH2 VGA2 TMDS B I2C0
VIDCAP ** VIP 7113 I2C2.
9pin DIN ** RGB2 I2C2.

X01: P78-A00
New file Created P71-X39+memory of P75 and new Mem PS

X02: P78-A00
Memory Address bus termination removed

X03: P78-A00
Cleanup- Design Review updates

X04: P78-A00
Mem Data/DQM bus Swapped on 11/14/01

X05: P78-A00
IFP PLLVDD REGULATOR ADDED
FBBCLK0 and 1 interchanged

X06: P78-A00
to memory U201/U203
Mem clock Pullups not required-R243 to R250 removed.
MVREF res package changed from 0603 to 0402 for
R219,R220 to R222, R239 to R242
U201- nets FBD19,20,21 swapped

X07: P78-A00
For I2C-2 Pull up/Protection
R1033 to 1036(4 pcs), 0603 addeded
L602, L603 (2pcs), 0805 added.
C883,C884 (2pcs), 0603 added
D505, D506 (2pcs), sot23 added.

X08: P78-A00
Changed the power for GPU Frame buffer decaps. Should be
FBVDDQ/FBVDD.
Deleted C868, C846 - TH part no space.
L602, L603- Package changed from 0805 to 0603.
GPU VDDDVO, C529, C530 AND DVOVREF TO 3.3V instead of
A3.3V

X09: P78-A00
ADDED ONE MORE REGULATOR FOR IFP PLLVDD
C885, C886 -0805 ADDED
R1038,R1039-0402 ADDED
U825 ADDED
R1028, R1029, R1031, R1032 PACKAGE
CHANGED TO 0402.

X10: P78-A00-Final Review
C419, C886 removed.-Not required

X11: P78-A00
R1040 Pull Down for Hotswap input added

X12: P78-A00
R616 added in series to Core switcher
12V input

X13: P78-A00
R201 AND C293 to be on FBVDD/Q instead of 3.3V

X14: P78-A00-PCB X-Released
Moved C618 CAP from 12V to 12V_IN

X15: P78-A00 -SCH X-Released
Memory Power R69 to support 2.8V or 2.5V Sku.
R69 CHANGED TO 154R FROM 150R FOR 2.8V
Bracket component added to SCH

NVVDD more comments added in PS sheet
Mem Pscomments edited in PS sheet

X17: P78-A00
Y300 Should be 18pF XTAL
C320,C321- New tuned values are 18pF
New Discrete VGA filter component values
changed to 10pF-68nH-No cap- 68nH-10pF.
NO_STUFF Integrated filter components.

U511 memory regulator o/p current spec lowerd to 2.0A
and Added new NVPN for 2.5V.
C145 No_stuff
U701-More substitute added
P300-DB15 and Bracket replaced with new PN.

X18: P78-A00
VGA Filter 10pF to be stuffed, missed in X17

X19: P78-A00
Add note in SCH that SAA7113 is not
supported in this design
Heat sink M2 changed from 45x45mm to 53x64mm

Stuff Option	Meaning
COMMON	Common to all assemblies
NO STUFF	Not present in any assembly
VIDCAP	Video In - Video Out, or Video Capture
LFH	LFH BOTH CHANNELS, NO TV, NO VIDCAP
TV	Second DAC channel goes to Svideo connector as TV Out
TVO	4pin DIN for TV Only
1117	Fixed 1117 linear regulator for A3.3V
1117_ADJ	Adjustable 1117 linear regulator for A3.3V
NO_1117	Connect A3.3V to 3.3V. No 1117 regulator.
IFPREG0	2.8V FOR IFP0PLLVD FOR LFH
IFPREG1	2.8V FOR IFP1PLLVD FOR LFH
IFPREG3V	IFP PLLVDD REGULATORS INPUT 3.3V
IFPREG5V	IFP PLLVDD REGULATORS INPUT 5V
ONE_IFPREG	COMMON 2.8V REGULATOR FOR IFP0PLLVD AND IFP1PLLVDD
IFP03V	A3.3V FOR IFP0PLLVD, DON'T USE IFPREG0, FOR TV
IFP13V	A3.3V FOR IFP1PLLVD, DON'T USE IFPREG1, FOR TV
NV17-128D	STRAP OPTION 0X171
CLAMP1	VGA1 Sync/I2C Clamping diodes
RGB_PROT	RGB Protection diodes on primary DAC outputs
CLAMP2	VGA2 Sync/I2C Clamping diodes
RGB2_PROT	RGB Protection diodes on secondary DAC outputs
CLAMP3	VIDCAP I2C/Video In Clamping diodes
TVCLAMP	TV Red/Green Clamping diodes
GPU	GPU ONLY
NV17-128D	IDSTRAP OPTION-171H
MEMORY	Memory only
M2-8V	Memory & PS output 2.8V
M2-5V	Memory & PS output 2.5V

PAGE OVERVIEW

1 top (this) page
2 1. AGP interface, core decoupling
3 2.a NV17 Frame Buffer
4 2.b Frame Buffer 0..63
5 2.c Frame Buffer 64...127
6 3.a Dual DAC, 1st VGA
7 3.b Dual DAC, 2nd LFH
8 4. LFH/Panel
9 5. TV-out, video capture, stereo
10 6. Power supply
11 6a. Memory Linear Regulator
12 7. BIOS, Strapping

140-10078-0000-A00
602-10078-0000-A00

NVIDIA Corporation
3535 Monroe St
Santa Clara, CA 95051, USA

P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X

Size	CAGE Code	DWG NO	Rev
Custom			17

Monday, January 14, 2002 — Scale — Sheet 1 of 12

{Item}\t{Quantity}\t{Reference}\t{Value}\t{Assembly}\t{MAIN}\t{NVPN}\t{Source Package}\t{AVL1}\t{AVL2}\t{AVL3}\t{AVL4}\t{AVL5}
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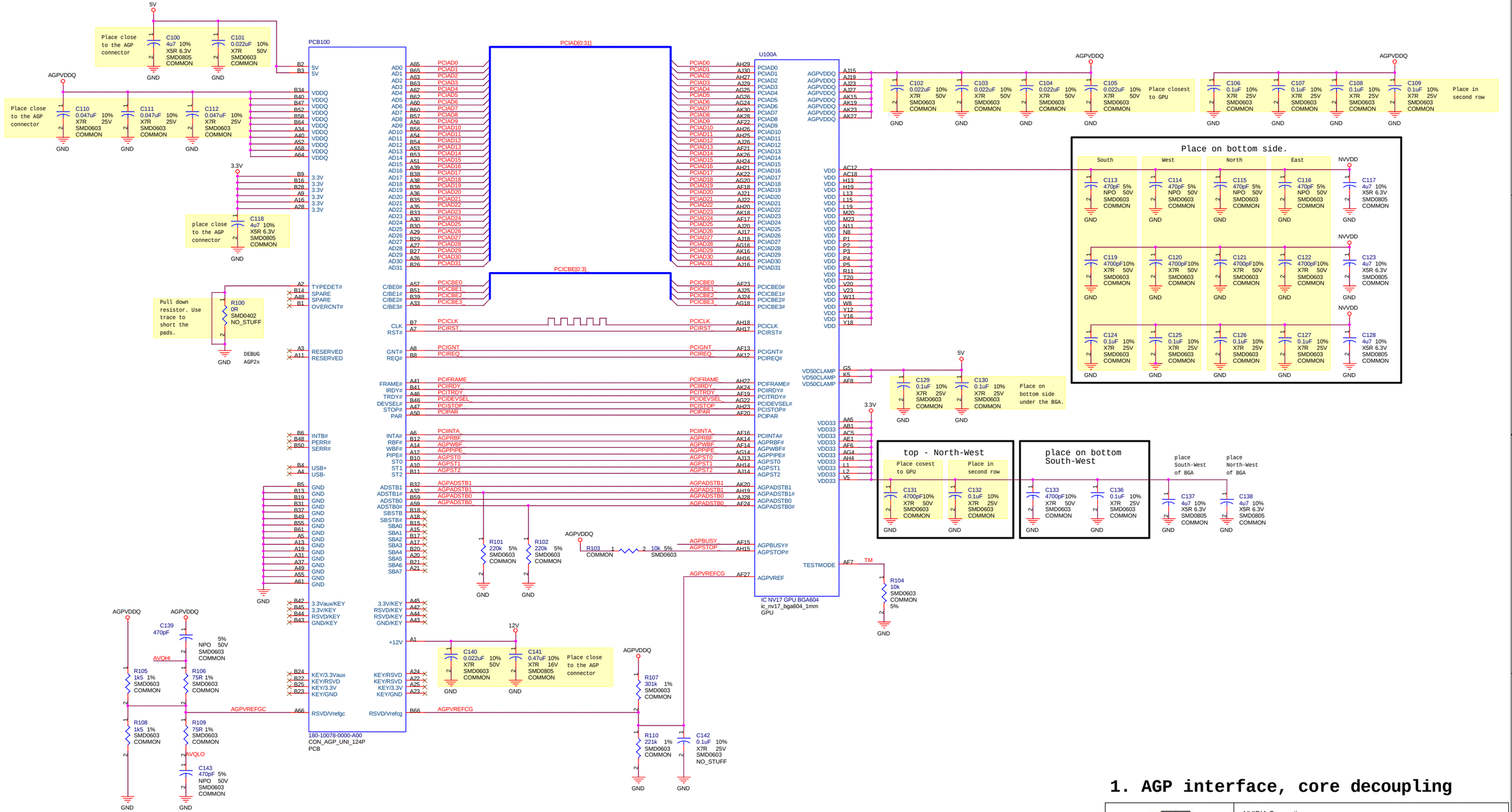
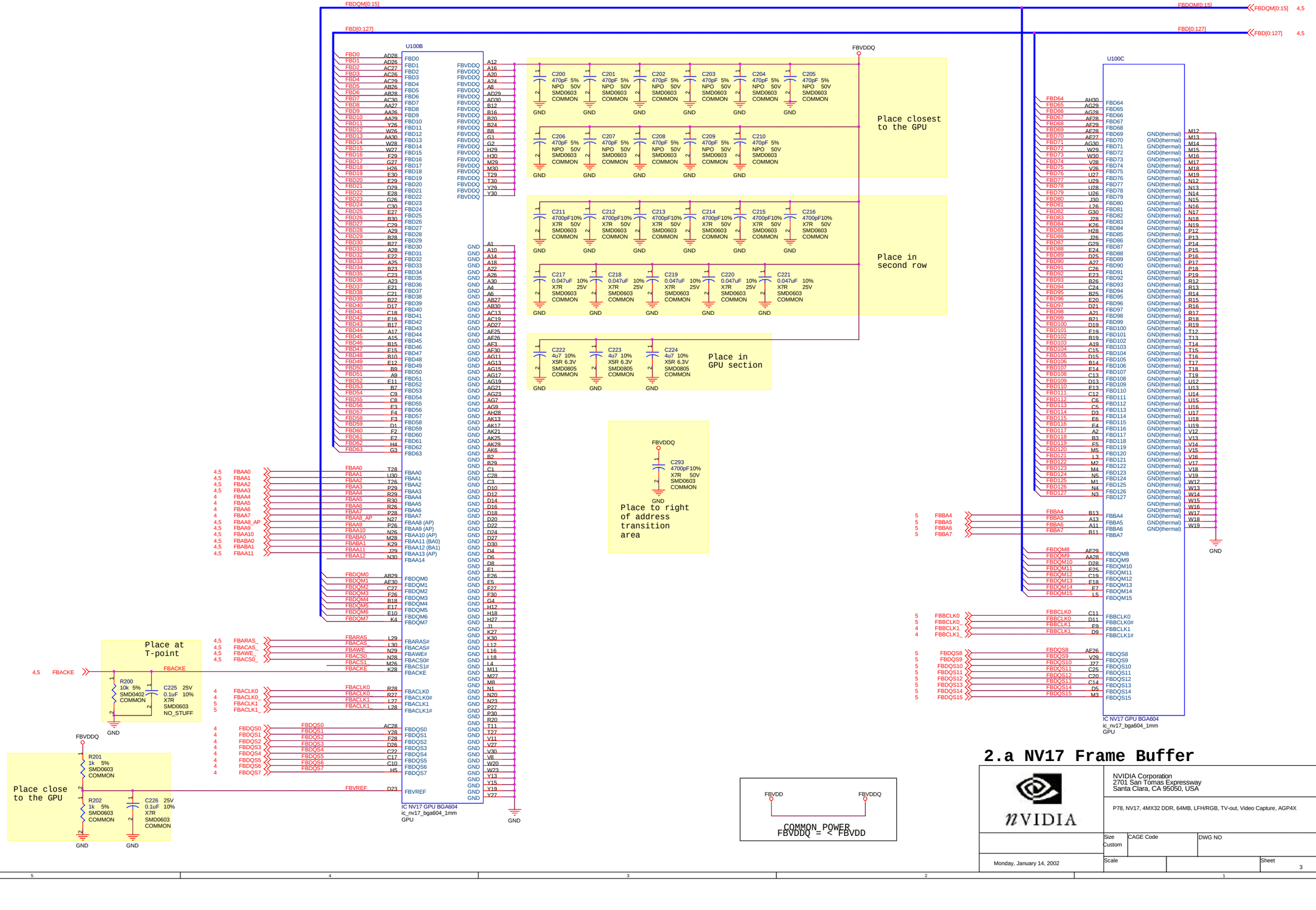
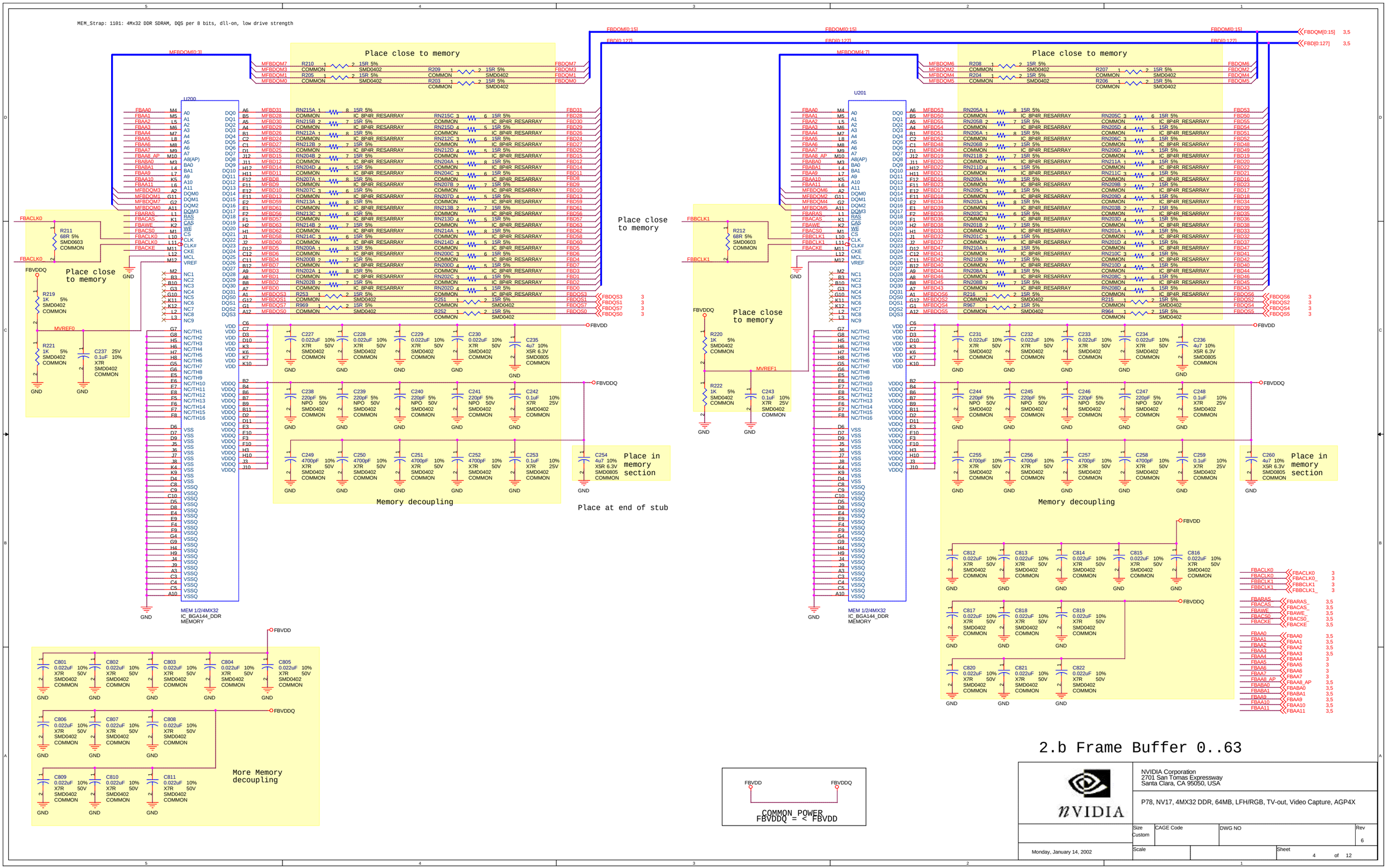

PCB100
180-10078-0000-A00
CON_AGP_UNI_124P
PCB
U100A
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
GPU
PCIAD[0:31]
PCICBE[0:3]
Place close to the AGP connector
Pull down resistor. Use trace to short the pads.
DEBUG AGP2x
Place on bottom side.
Place on bottom side under the BGA.
top - North-West
place on bottom South-West
1. AGP interface, core decoupling
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X
Monday, January 14, 2002
Sheet 2 of 12


FBDQM[0:15]
FBD[0:127]
U100B
FBVDDQ
C200 470pF 5% NPO 50V SMD0603 COMMON
C201 470pF 5% NPO 50V SMD0603 COMMON
C202 470pF 5% NPO 50V SMD0603 COMMON
C203 470pF 5% NPO 50V SMD0603 COMMON
C204 470pF 5% NPO 50V SMD0603 COMMON
C205 470pF 5% NPO 50V SMD0603 COMMON
C206 470pF 5% NPO 50V SMD0603 COMMON
C207 470pF 5% NPO 50V SMD0603 COMMON
C208 470pF 5% NPO 50V SMD0603 COMMON
C209 470pF 5% NPO 50V SMD0603 COMMON
C210 470pF 5% NPO 50V SMD0603 COMMON
Place closest to the GPU
C211 4700pF10% X7R 50V SMD0603 COMMON
C212 4700pF10% X7R 50V SMD0603 COMMON
C213 4700pF10% X7R 50V SMD0603 COMMON
C214 4700pF10% X7R 50V SMD0603 COMMON
C215 4700pF10% X7R 50V SMD0603 COMMON
C216 4700pF10% X7R 50V SMD0603 COMMON
C217 0.047uF 10% X7R 25V SMD0603 COMMON
C218 0.047uF 10% X7R 25V SMD0603 COMMON
C219 0.047uF 10% X7R 25V SMD0603 COMMON
C220 0.047uF 10% X7R 25V SMD0603 COMMON
C221 0.047uF 10% X7R 25V SMD0603 COMMON
Place in second row
C222 4u7 10% X5R 6.3V SMD0805 COMMON
C223 4u7 10% X5R 6.3V SMD0805 COMMON
C224 4u7 10% X5R 6.3V SMD0805 COMMON
Place in GPU section
C293 4700pF10% X7R 50V SMD0603 COMMON
Place to right of address transition area
Place at T-point
R200 10k 5% SMD0402 COMMON
C225 25V 0.1uF 10% X7R SMD0603 NO_STUFF
R201 1k 5% SMD0603 COMMON
R202 1k 5% SMD0603 COMMON
C226 25V 0.1uF 10% X7R SMD0603 COMMON
Place close to the GPU
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
GPU
U100C
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
GPU
FBVDD
FBVDDQ
COMMON_POWER
FBVDDQ = < FBVDD
2.a NV17 Frame Buffer
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X
Size Custom
CAGE Code
DWG NO
Rev 01
Monday, January 14, 2002
Scale
Sheet 3 of 12



2.b Frame Buffer 0..63

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2701 San Tomas Expressway
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P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X

Size	CAGE Code	DWG NO	Rev
Custom			6

Monday, January 14, 2002

Scale

Sheet 4 of 12

MEM_Strap: 1101: 4Mx32 DDR SDRAM, DQS per 8 bits, dll-on, low drive strength

FBDQM[0:15]
FBD[0:127]
MFBDQM[8:11]

Place close to memory

MFBDQM8 R223 15R 5% FBDQM8
MFBDQM9 COMMON SMD0402 R225 15R 5% FBDQM9
MFBDQM10 R227 15R 5% COMMON SMD0402 FBDQM10
MFBDQM11 COMMON SMD0402 R229 15R 5% FBDQM11
COMMON SMD0402

U202

FBACLK1 R231 68R 5% SMD0603 COMMON FBACLK1
FBACLK0 FBACLK0

FBVDDQ Place close to memory
R239 1K 5% SMD0402 COMMON
MVREF2
R241 1K 5% SMD0402 COMMON
C273 0.1uF 10% X7R 25V SMD0402 COMMON

MEM 1/2/4MX32 IC_BGA144_DDR MEMORY

FBVDD
C263 0.022uF 10% X7R 50V SMD0402 COMMON
C264 0.022uF 10% X7R 50V SMD0402 COMMON
C265 0.022uF 10% X7R 50V SMD0402 COMMON
C266 0.022uF 10% X7R 50V SMD0402 COMMON
C271 4u7 10% X5R 6.3V SMD0805 COMMON
FBVDDQ
C274 220pF 5% NPO 50V SMD0402 COMMON
C275 220pF 5% NPO 50V SMD0402 COMMON
C276 220pF 5% NPO 50V SMD0402 COMMON
C277 220pF 5% NPO 50V SMD0402 COMMON
C278 0.1uF 10% X7R 25V SMD0402 COMMON
C285 4700pF 10% X7R 50V SMD0402 COMMON
C286 4700pF 10% X7R 50V SMD0402 COMMON
C287 4700pF 10% X7R 50V SMD0402 COMMON
C288 4700pF 10% X7R 50V SMD0402 COMMON
C289 0.1uF 10% X7R 25V SMD0402 COMMON
C290 4u7 10% X5R 6.3V SMD0805 COMMON
Place in memory section
Memory decoupling

FBVDD
C823 0.022uF 10% X7R 50V SMD0402 COMMON
C824 0.022uF 10% X7R 50V SMD0402 COMMON
C825 0.022uF 10% X7R 50V SMD0402 COMMON
C826 0.022uF 10% X7R 50V SMD0402 COMMON
C827 0.022uF 10% X7R 50V SMD0402 COMMON
FBVDDQ
C828 0.022uF 10% X7R 50V SMD0402 COMMON
C829 0.022uF 10% X7R 50V SMD0402 COMMON
C830 0.022uF 10% X7R 50V SMD0402 COMMON
C831 0.022uF 10% X7R 50V SMD0402 COMMON
C832 0.022uF 10% X7R 50V SMD0402 COMMON
C833 0.022uF 10% X7R 50V SMD0402 COMMON
More Memory decoupling

FBDQM[0:15]
FBD[0:127]
MFBDQM[12:15]

Place close to memory

MFBDQM12 R224 15R 5% FBDQM12
MFBDQM13 COMMON SMD0402 R226 15R 5% FBDQM13
MFBDQM14 R228 15R 5% COMMON SMD0402 FBDQM14
MFBDQM15 COMMON SMD0402 R230 15R 5% FBDQM15
COMMON SMD0402

U203

FBBCLK0 R232 68R 5% SMD0603 COMMON FBBCLK0
FBBCLK0 FBBCLK0

FBVDDQ Place close to memory
R240 1K 5% SMD0402 COMMON
MVREF3
R242 1K 5% SMD0402 COMMON
C279 0.1uF 10% X7R 25V SMD0402 COMMON

MEM 1/2/4MX32 IC_BGA144_DDR MEMORY

FBVDD
C267 0.022uF 10% X7R 50V SMD0402 COMMON
C268 0.022uF 10% X7R 50V SMD0402 COMMON
C269 0.022uF 10% X7R 50V SMD0402 COMMON
C270 0.022uF 10% X7R 50V SMD0402 COMMON
C272 4u7 10% X5R 6.3V SMD0805 COMMON
FBVDDQ
C280 220pF 5% NPO 50V SMD0402 COMMON
C281 220pF 5% NPO 50V SMD0402 COMMON
C282 220pF 5% NPO 50V SMD0402 COMMON
C283 220pF 5% NPO 50V SMD0402 COMMON
C284 0.1uF 10% X7R 25V SMD0402 COMMON
C291 4700pF 10% X7R 50V SMD0402 COMMON
C292 4700pF 10% X7R 50V SMD0402 COMMON
C299 4700pF 10% X7R 50V SMD0402 COMMON
C294 4700pF 10% X7R 50V SMD0402 COMMON
C295 0.1uF 10% X7R 25V SMD0402 COMMON
C296 4u7 10% X5R 6.3V SMD0805 COMMON
Place in memory section
Memory decoupling

C293->C299

FBVDD
C834 0.022uF 10% X7R 50V SMD0402 COMMON
C835 0.022uF 10% X7R 50V SMD0402 COMMON
C836 0.022uF 10% X7R 50V SMD0402 COMMON
C837 0.022uF 10% X7R 50V SMD0402 COMMON
C838 0.022uF 10% X7R 50V SMD0402 COMMON
FBVDDQ
C839 0.022uF 10% X7R 50V SMD0402 COMMON
C840 0.022uF 10% X7R 50V SMD0402 COMMON
C841 0.022uF 10% X7R 50V SMD0402 COMMON
C842 0.022uF 10% X7R 50V SMD0402 COMMON
C843 0.022uF 10% X7R 50V SMD0402 COMMON
C844 0.022uF 10% X7R 50V SMD0402 COMMON

FBACLK1 FBACLK1 3
FBACLK1_ FBACLK1_ 3
FBBCLK0 FBBCLK0 3
FBBCLK0_ FBBCLK0_ 3

FBARAS_ FBARAS_ 3,4
FBACAS_ FBACAS_ 3,4
FBAWE_ FBAWE_ 3,4
FBACS0_ FBACS0_ 3,4
FBACKE FBACKE 3,4

FBAA0 FBAA0 3,4
FBAA1 FBAA1 3,4
FBAA2 FBAA2 3,4
FBAA3 FBAA3 3,4
FBAA4 FBAA4 3
FBAA5 FBAA5 3
FBAA6 FBAA6 3
FBAA7 FBAA7 3
FBAA8_AP FBAA8_AP 3,4
FBABA0 FBABA0 3,4
FBABA1 FBABA1 3,4
FBAA9 FBAA9 3,4
FBAA10 FBAA10 3,4
FBAA11 FBAA11 3,4

FBDQM[0:15] FBDQM[0:15] 3,4
FBD[0:127] FBD[0:127] 3,4

2.c Frame Buffer 64...127

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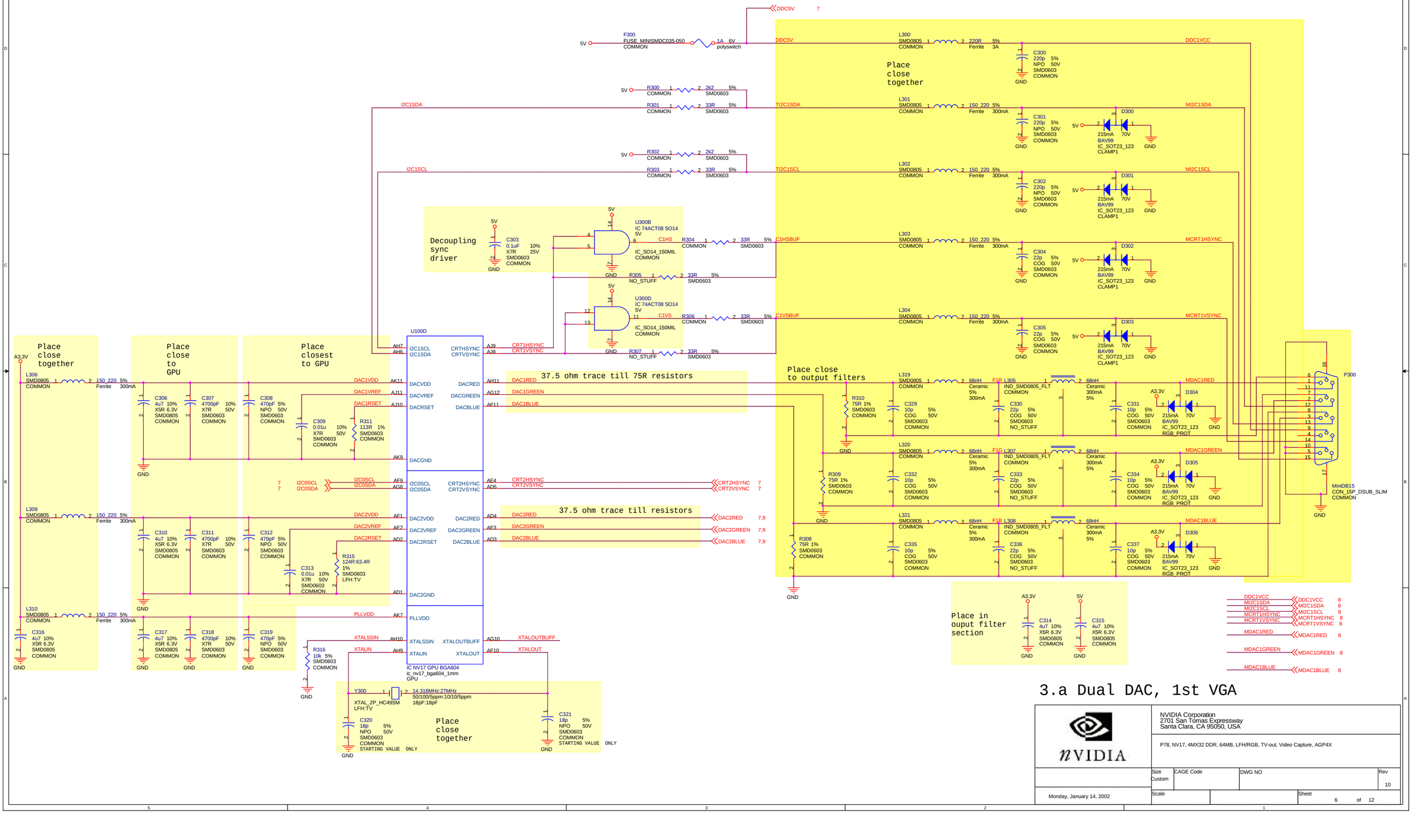
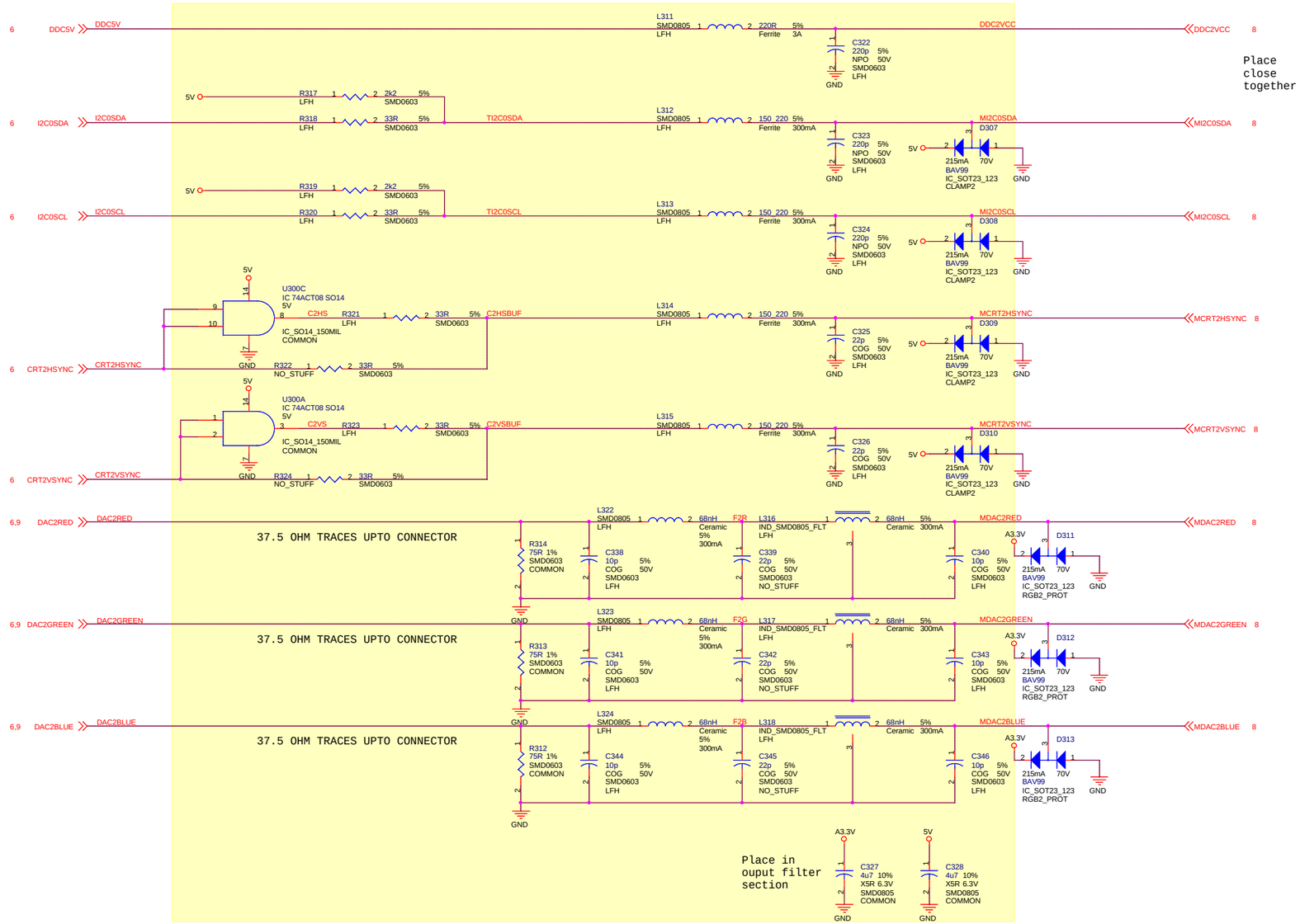
P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X

Size	CAGE Code	DWG NO	Rev
Custom			6

Monday, January 14, 2002 — Scale — Sheet 5 of 12


DDC5V
F300
FUSE_MINISMDC035-050
COMMON
1A 6V
polyswitch
L300
SMD0805
COMMON
220R 5%
Ferrite 3A
DDC1VCC
C300
220p 5%
NPO 50V
SMD0603
COMMON
Place close together
R300 2k2 5%
R301 33R 5%
I2C1SDA
Ti2C1SDA
L301
150_220 5%
Ferrite 300mA
MI2C1SDA
C301
D300
215mA 70V
BAV99
IC_SOT23_123
CLAMP1
R302 2k2 5%
R303 33R 5%
I2C1SCL
Ti2C1SCL
L302
MI2C1SCL
C302
D301
Decoupling sync driver
C303
0.1uF 10%
X7R 25V
SMD0603
U300B
IC 74ACT08 SO14
C1HS
R304 33R 5%
C1HSBUF
L303
MCRT1HSYNC
C304
22p 5%
COG 50V
D302
R305 33R 5%
NO_STUFF
U300D
C1VS
R306 33R 5%
C1VSBUF
L304
MCRT1VSYNC
C305
D303
IC_SO14_150MIL
R307 33R 5%
U100D
AH7 I2C1SCL
AH6 I2C1SDA
AJ9 CRTHSYNC
AJ8 CRTVSYNC
CRT1HSYNC
CRT1VSYNC
Place close to output filters
L319
68nH
Ceramic 5% 300mA
F1R L305
IND_SMD0805_FLT
C329 10p 5% COG 50V
C330 22p 5% COG 50V
C331 10p 5% COG 50V
D304
MDAC1RED
R310 75R 1% SMD0603 COMMON
L320
F1G L307
C332 10p 5% COG 50V
C333 22p 5% COG 50V
C334 10p 5% COG 50V
D305
MDAC1GREEN
R309 75R 1% SMD0603 COMMON
L321
F1B L308
C335 10p 5% COG 50V
C336 22p 5% COG 50V
C337 10p 5% COG 50V
D306
MDAC1BLUE
R308 75R 1% SMD0603 COMMON
P300
MiniDB15
CON_15P_DSUB_SLIM
COMMON
Place in ouput filter section
C314 4u7 10% X5R 6.3V SMD0805 COMMON
C315 4u7 10% X5R 6.3V SMD0805 COMMON
DDC1VCC 8
MI2C1SDA 8
MI2C1SCL 8
MCRT1HSYNC 8
MCRT1VSYNC 8
MDAC1RED 8
MDAC1GREEN 8
MDAC1BLUE 8
Place close together
L306
150_220 5%
Ferrite 300mA
C306 4u7 10% X5R 6.3V SMD0805 COMMON
C307 4700pF 10% X7R 50V SMD0603 COMMON
C308 470pF 5% NPO 50V SMD0603 COMMON
C309 0.01u 10% X7R 50V SMD0603 COMMON
R311 113R 1% SMD0603 COMMON
DAC1VDD
DAC1VREF
DAC1RSET
DACGND
DACVDD
DACVREF
DACRSET
DACRED
DACGREEN
DACBLUE
AK11
AJ11
AJ10
AK9
AH11
AG12
AE11
DAC1RED
DAC1GREEN
DAC1BLUE
37.5 ohm trace till 75R resistors
I2C0SCL
I2C0SDA
CRT2HSYNC
CRT2VSYNC
AF9
AG8
AE4
AD5
37.5 ohm trace till resistors
L309
C310 4u7 10% X5R 6.3V SMD0805 COMMON
C311 4700pF 10% X7R 50V SMD0603 COMMON
C312 470pF 5% NPO 50V SMD0603 COMMON
C313 0.01u 10% X7R 50V SMD0603 COMMON
R315 124R:63.4R 1% SMD0603 LFH:TV
DAC2VDD
DAC2VREF
DAC2RSET
DAC2GND
AF1
AE2
AD2
AD1
AD4
AE3
AD3
DAC2RED
DAC2GREEN
DAC2BLUE
L310
C316 4u7 10% X5R 6.3V SMD0805 COMMON
C317 4u7 10% X5R 6.3V SMD0805 COMMON
C318 4700pF 10% X7R 50V SMD0603 COMMON
C319 470pF 5% NPO 50V SMD0603 COMMON
PLLVDD
AK7
R316 10k 5% SMD0603 COMMON
XTALSSIN
XTALIN
AH10
AH9
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
AG10
AF10
iC NV17 GPU BGA604
ic_nv17_bga604_1mm
GPU
Y300 14.318MHz:27MHz
XTAL_2P_HC49SM
LFH:TV
50/100/5ppm:10/10/5ppm
18pF:18pF
C320 18p 5% NPO 50V SMD0603 COMMON STARTING VALUE ONLY
C321 18p 5% NPO 50V SMD0603 COMMON STARTING VALUE ONLY
Place close together
Place close to GPU
Place closest to GPU
A3.3V
5V
GND
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X
3.a Dual DAC, 1st VGA
Size Custom
CAGE Code
DWG NO
Rev 10
Monday, January 14, 2002
Scale
Sheet 6 of 12



VERIFY SKU FOR PROTECTION DIODES

3.b Dual DAC, 2nd LFH

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

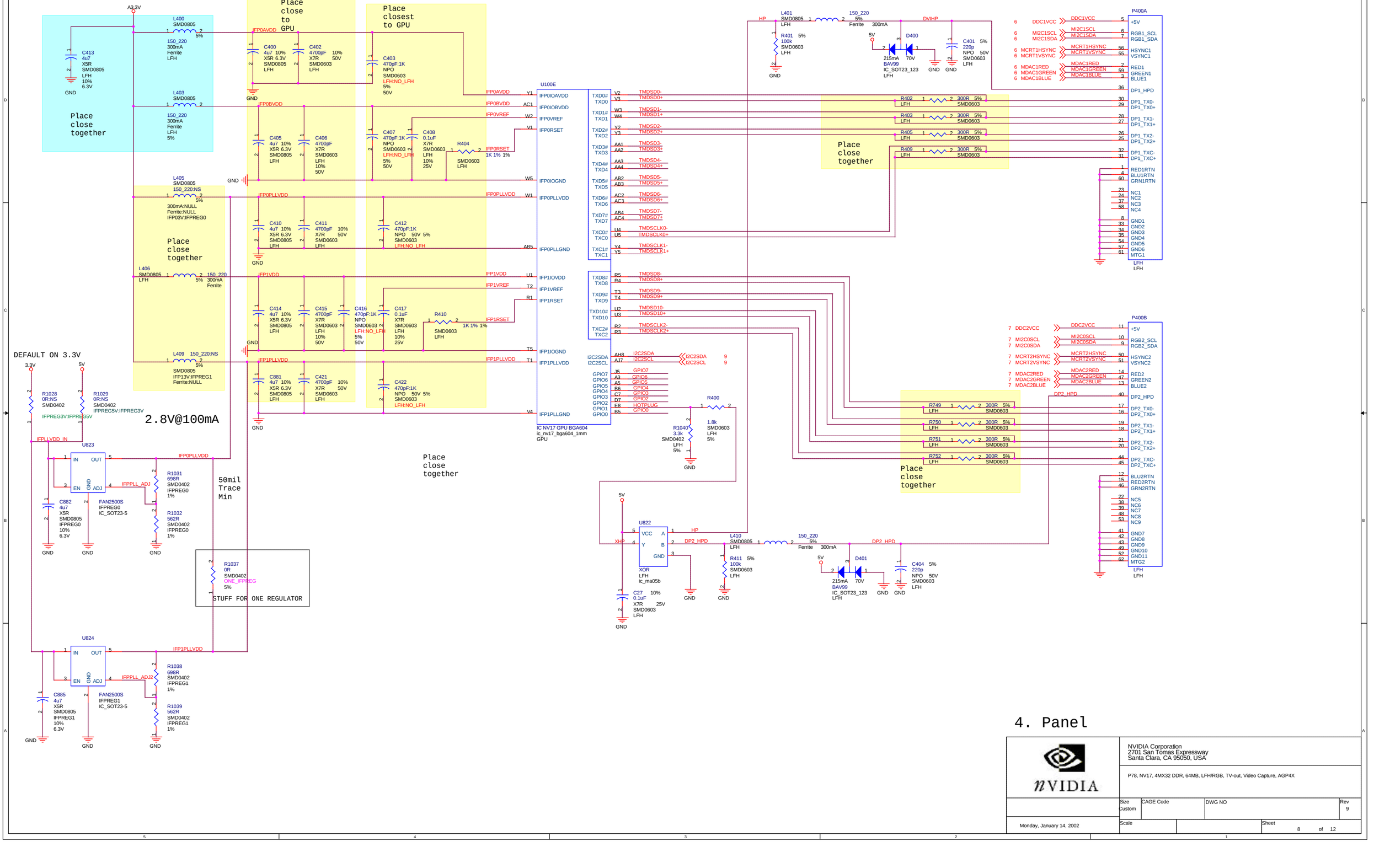
P71, NV17, 4MX16 SDR, 64MB, LFH/RGB, TV-out, video capture, AGP4x

Size	CAGE Code	DWG NO	Rev
Custom			10

Monday, January 14, 2002

Scale

Sheet 7 of 12



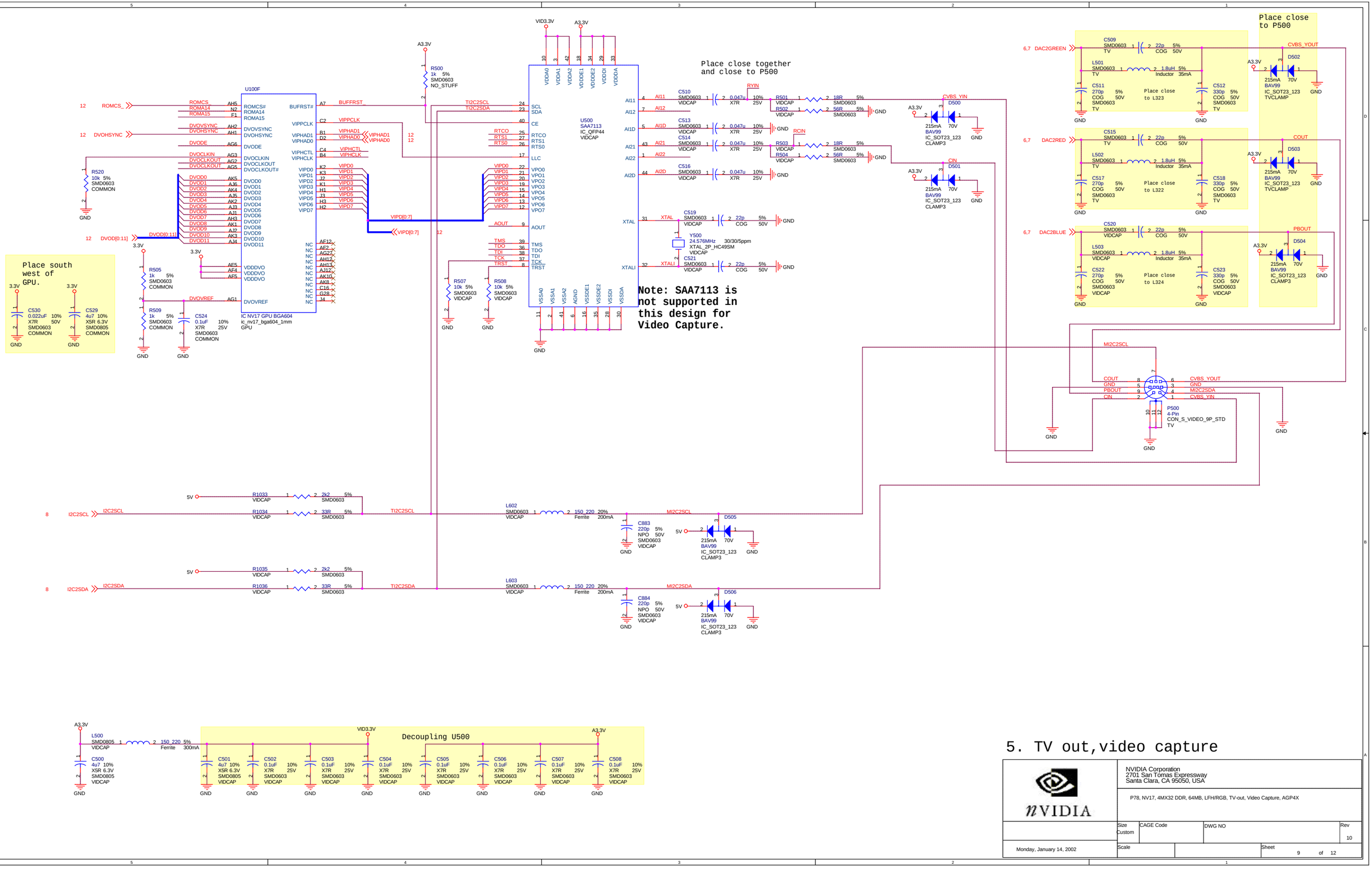
4. Panel

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X

Size	CAGE Code	DWG NO	Rev
Custom			9

Monday, January 14, 2002 | Scale | | Sheet 8 of 12


U100F
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
GPU
U500
SAA7113
IC_QFP44
VIDCAP
Place close together
and close to P500
Note: SAA7113 is
not supported in
this design for
Video Capture.
Place south
west of
GPU.
Place close
to P500
P500
4-Pin
CON_S_VIDEO_9P_STD
TV
Decoupling U500
5. TV out,video capture
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X
Monday, January 14, 2002
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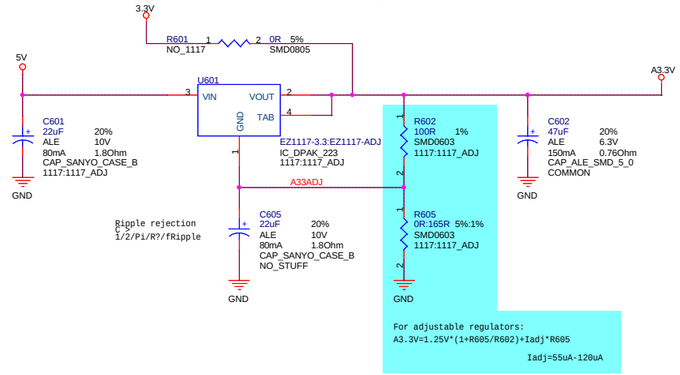
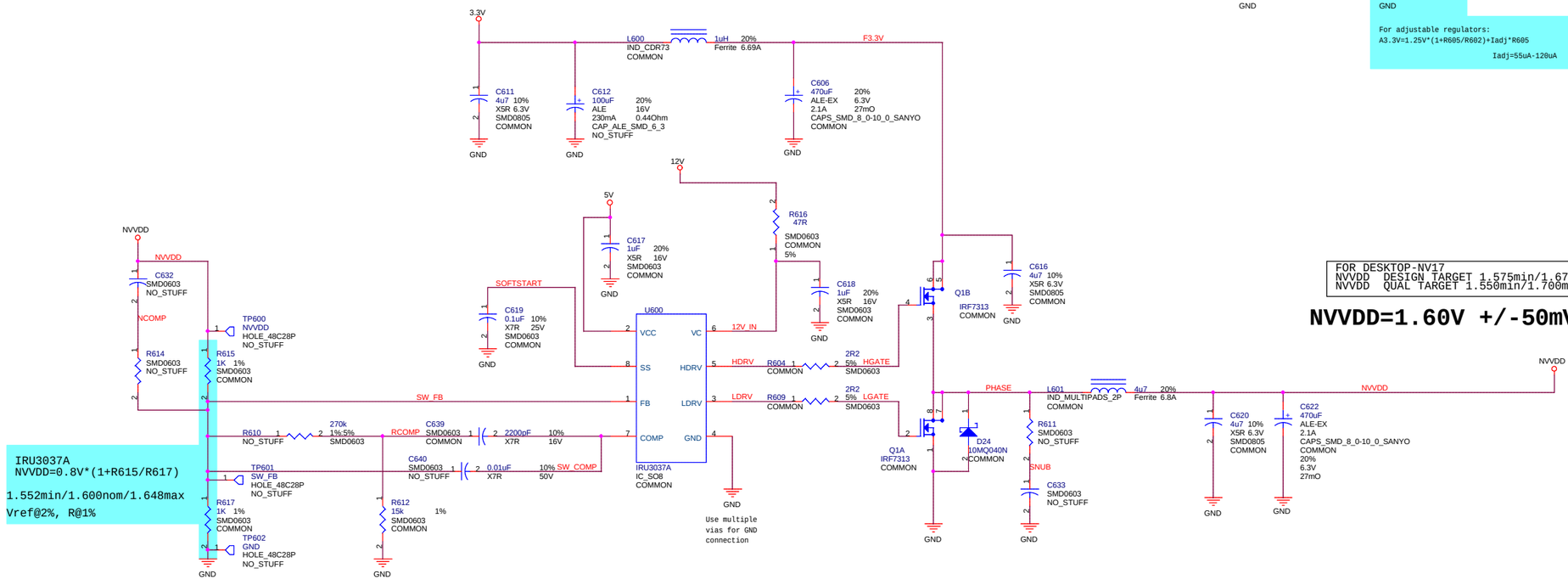
Analog 3.3V



FOR DESKTOP-NV17
NVVDD DESIGN TARGET 1.575min/1.675max
NVVDD QUAL TARGET 1.550min/1.700max

NVVDD=1.60V +/-50mV /4A



6. Power supply

NVIDIA	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA		
	P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X		
	Size: Custom	CAGE Code	DWG NO / Rev: 16
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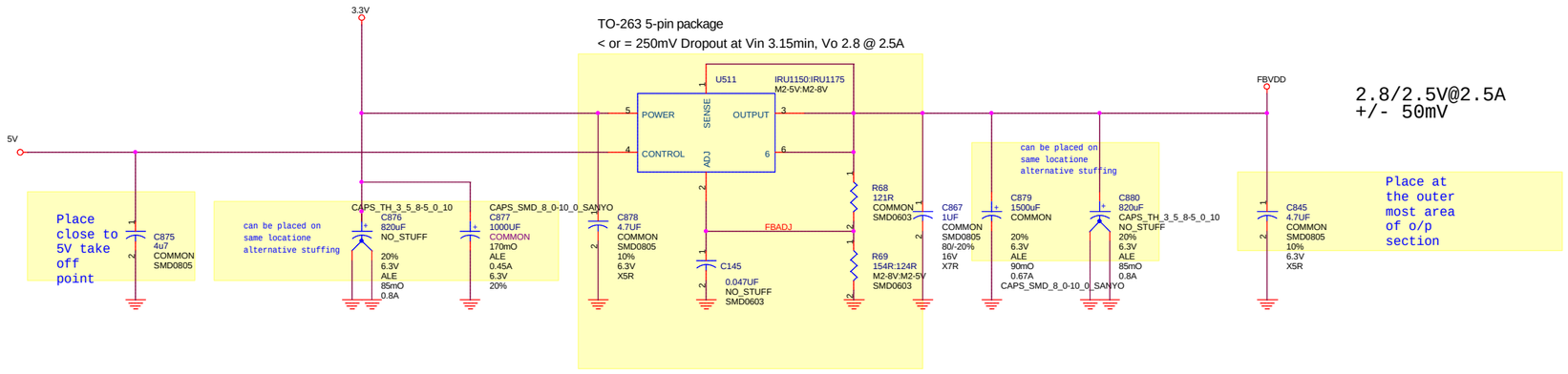
Note: Repeated on memory sheets also

FBVDD FBVDDQ

COMMON POWER
FBVDDQ = < FBVDD



Vo = 1.25 * (1+ R69/R68) + Iadj * R69

Iadj = 50uA

M2-8V = 2.512/2.54/2.563- Mem Limit 2.66 to 2.94

M2-5V = 2.817/2.85/2.881- Mem Limit 2.375 to 2.625

6.a MEMORY power supply

NVIDIA Corporation
3535 Monroe St
Santa Clara, CA 95051, USA

P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X

Size	CAGE Code	DWG NO	Rev
C			16

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PORC_REG[30:0]			
Bit_0	R701 1 NO_STUFF 2 10k 5% SMD0402	DVOD0	R701 1 COMMON 2 10k 5% SMD0402 — 3.3V — PCI_AD_SWAP
Bit_1	R702 1 NO_STUFF 2 10k 5% SMD0402	DVOD1	R703 1 COMMON 2 10k 5% SMD0402 — SUB_VENDOR
Bit_2	R704 1 NO_STUFF 2 10k 5% SMD0402	DVOD2	R705 1 COMMON 2 10k 5% SMD0402 — RAM_CFG0
Bit_3	R706 1 COMMON 2 10k 5% SMD0402	DVOD3	R707 1 NO_STUFF 2 10k 5% SMD0402 — RAM_CFG1
Bit_4	R708 1 NO_STUFF 2 10k 5% SMD0402	DVOD4	R709 1 COMMON 2 10k 5% SMD0402 — RAM_CFG2
Bit_5	R710 1 NO_STUFF 2 10k 5% SMD0402	DVOD5	R711 1 COMMON 2 10k 5% SMD0402 — RAM_CFG3
Bit_6	R712 1 LFH:TV 2 NS:10k 5% SMD0402	DVOD6	R713 1 LFH:TV 2 10k:NS 5% SMD0402 — CRYSTAL0
Bit_22	R714 1 LFH:TV 2 10k:NS 5% SMD0402	VIPD6	R715 1 LFH:TV 2 NS:10k 5% SMD0402 — CRYSTAL1
Bit_7	R716 1 NO_STUFF 2 10k 5% SMD0402	DVOD7	R717 1 COMMON 2 10k 5% SMD0402 — TVMODE0
Bit_8	R718 1 LFH:TV 2 NS:10k 5% SMD0402	DVOD8	R719 1 LFH:TV 2 10k:NS 5% SMD0402 — TVMODE1
Bit_9	R722 1 COMMON 2 10k 5% SMD0402	DVOD9	R723 1 NO_STUFF 2 10k 5% SMD0402 — AGP4x
Bit_11	R724 1 COMMON 2 10k 5% SMD0402	VIPD7	R725 1 NO_STUFF 2 10k 5% SMD0402 — AGP_FW
Bit_12	R726 1 NO_STUFF 2 10k 5% SMD0402	VIPD4	R727 1 NV17-128D 2 10k 5% SMD0402 — PCI_DEVID3
Bit_13	R728 1 NV17-128D 2 10k 5% SMD0402	VIPD5	R729 1 NO_STUFF 2 10k 5% SMD0402 — PCI_DEVID2
Bit_20	R730 1 NV17-128D 2 10k 5% SMD0402	VIPD3	R731 1 NO_STUFF 2 10k 5% SMD0402 — PCI_DEVID1
Bit_21	R732 1 NV17-128D 2 10k 5% SMD0402	DVOHSYNC	R733 1 NO_STUFF 2 10k 5% SMD0402 — PCI_DEVID0
Bit_14	R734 1 NO_STUFF 2 10k 5% SMD0402	DVOD11	R735 1 COMMON 2 10k 5% SMD0402 — BUS_TYPE
Bit_16	R736 1 COMMON 2 10k 5% SMD0402	VIPD0	R737 1 NO_STUFF 2 10k 5% SMD0402 — USER0
Bit_17	R738 1 COMMON 2 10k 5% SMD0402	VIPD1	R739 1 NO_STUFF 2 10k 5% SMD0402 — USER1
Bit_18	R740 1 COMMON 2 10k 5% SMD0402	VIPHAD0	R741 1 NO_STUFF 2 10k 5% SMD0402 — USER2
Bit_19	R742 1 COMMON 2 10k 5% SMD0402	VIPHAD1	R743 1 NO_STUFF 2 10k 5% SMD0402 — USER3
Bit_29	R744 1 NO_STUFF 2 10k 5% SMD0402	DVOD10	R745 1 COMMON 2 10k 5% SMD0402 — ROMTYPE0
Bit_30	R746 1 COMMON 2 10k 5% SMD0402	VIPD2	R747 1 NO_STUFF 2 10k 5% SMD0402 — ROMTYPE1

GND

PCI_AD_SWAP
0: REVERSED-Not supported
1: NORMAL Default

SUB_VENDOR
0: system BIOS
1: adapter BIOS Default

RAM_CFG[3:0]
1111: 4Mx32 DDR SDRAM, DQS per 32 bits, dll-on, low drive strength-Not supported inP78
1101: 4Mx32 DDR SDRAM, DQS per 8 bits, dll-on, low drive strength

CRYSTAL[1:0]
00: 13.5MHz-Not Supported
01: 14.318MHz- LFH
10: 27MHz - TV
11: Reserved

TVMODE[1:0]
00: SECAM
01: NTSC - Default
10: PAL
11: DAC2-VGA-LFH

AGP4x
0: enabled - Default
1: disabled

AGP_FW
0: enabled - Default
1: disabled

PCI_DEVID[3:0]
0001: NV17-128D
0010: NV17-S-XX
1000: NV17-GL-XX

0x171

BUS_TYPE
0: PCI
1: AGP- Default

USER[3:0]
USER[0]=0: PC
USER[0]=1: MAC- NOT SUPPORTED

ROMTYPE[1:0]
00: Parallel
01: Serial AT25F Default
10: Notused
11: Reserved

M2
Passive
COMMON
110-00018-0000-000
HEATSINK, PASSIVE, MECH HOLD DOWN, 53mm X 64mm

3.3V
C700 0.1u 10% X7R 25V SMD0603 COMMON
GND

9 DVOD[0:11] DVOD[0:11]
9 VIPD[0:7] VIPD[0:7]

U701 AT25F1024 COMMON IC_SO8 COMMON
R748 10k SMD0603 NO_STUFF 5%
DVOD0 DVOD1 VIPD0 ROMCS_
SI SCK SO CS VDD HOLD WP GND

9 ROMCS_ ROMCS_

9 DVOHSYNC DVOHSYNC
9 VIPHAD0 VIPHAD0
9 VIPHAD1 VIPHAD1

M401
BRACKET
VGA_DIN_STD:VGA_DIN_LP:VGA_STD:VGA_LP

7. BIOS, Strapping

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X

Size	CAGE Code	DWG NO	Rev
Custom			17

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