

(9) PCIE_REFCLKP >>> PCIE_REFCLKP
(9) PCIE_REFCLKN >>> PCIE_REFCLKN
(9) PCIE_RST# >>> PCIE_RST#
(9) PCIE_RXP[15..0] >>> PCIE_RXP[15..0]
(9) PCIE_RXN[15..0] >>> PCIE_RXN[15..0]
(9) PCIE_TXP[15..0] <<< PCIE_TXP[15..0]
(9) PCIE_TXN[15..0] <<< PCIE_TXN[15..0]

<Variant Name>

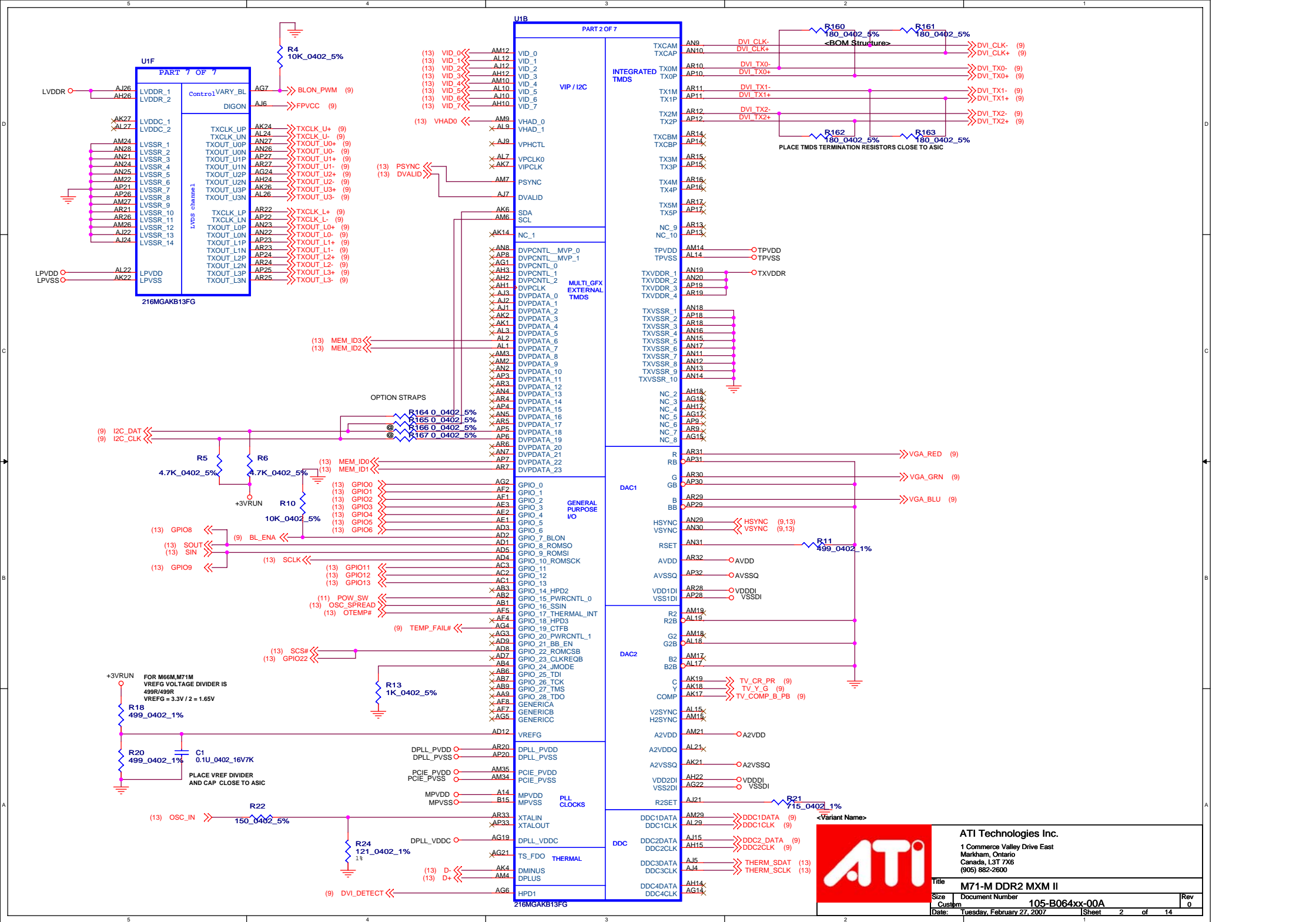


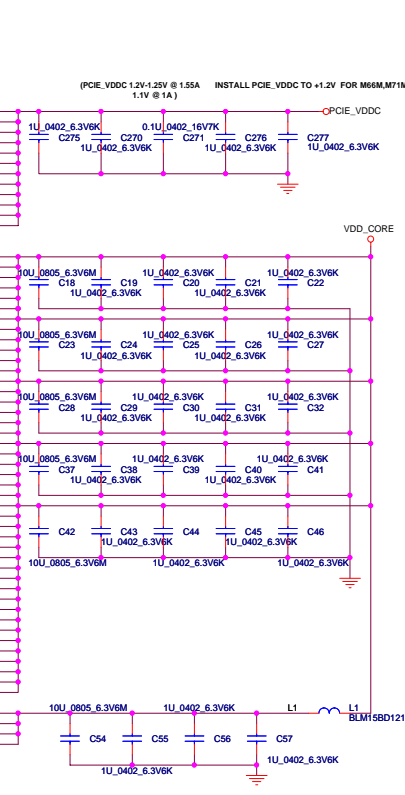
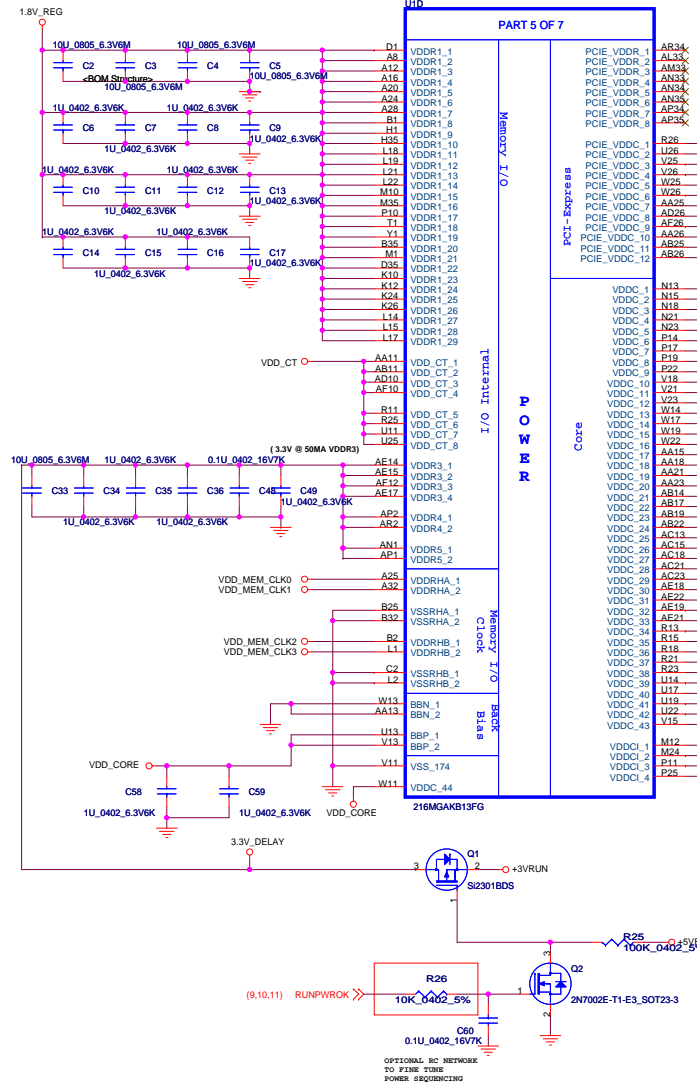
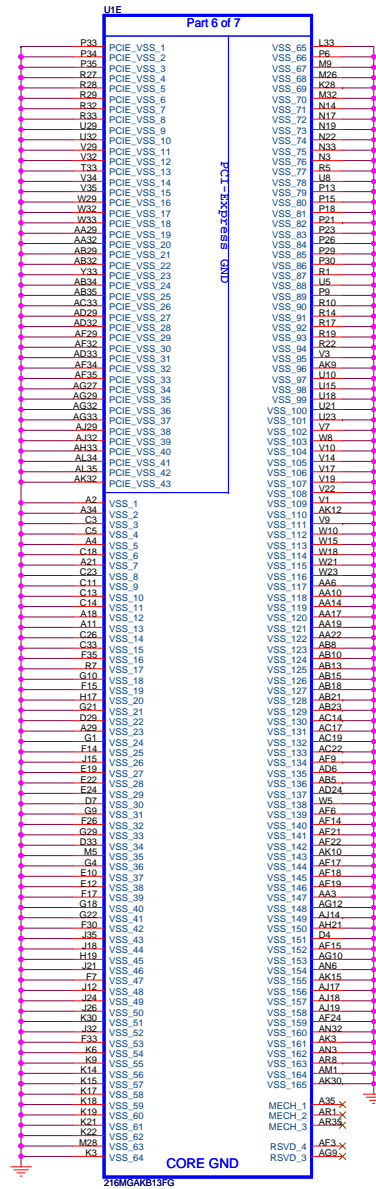
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Size	Document Number	105-B064xx-00A	Rev 0
Date:	Monday, December 04, 2006	Sheet 1 of 14	

FOR PCIE_CALI
INSTALL 10K TO PCIE_VSS FOR M72M,M76M
INSTALL 1.47K TO PCIE_VSS FOR M66M,M71M



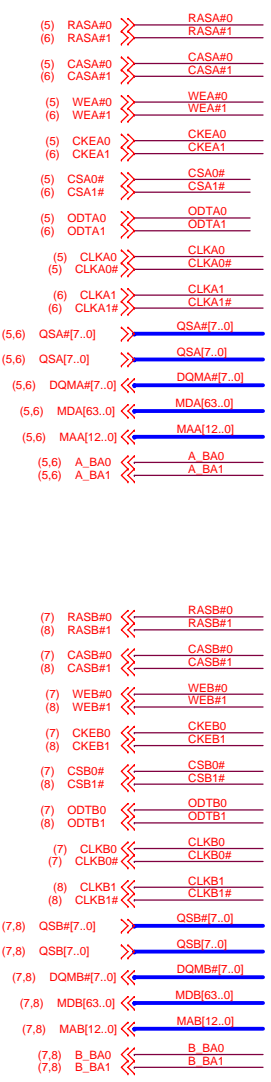
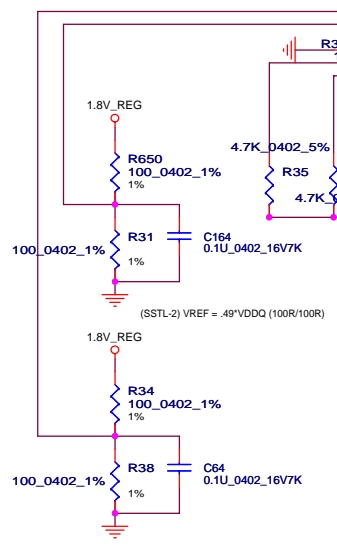
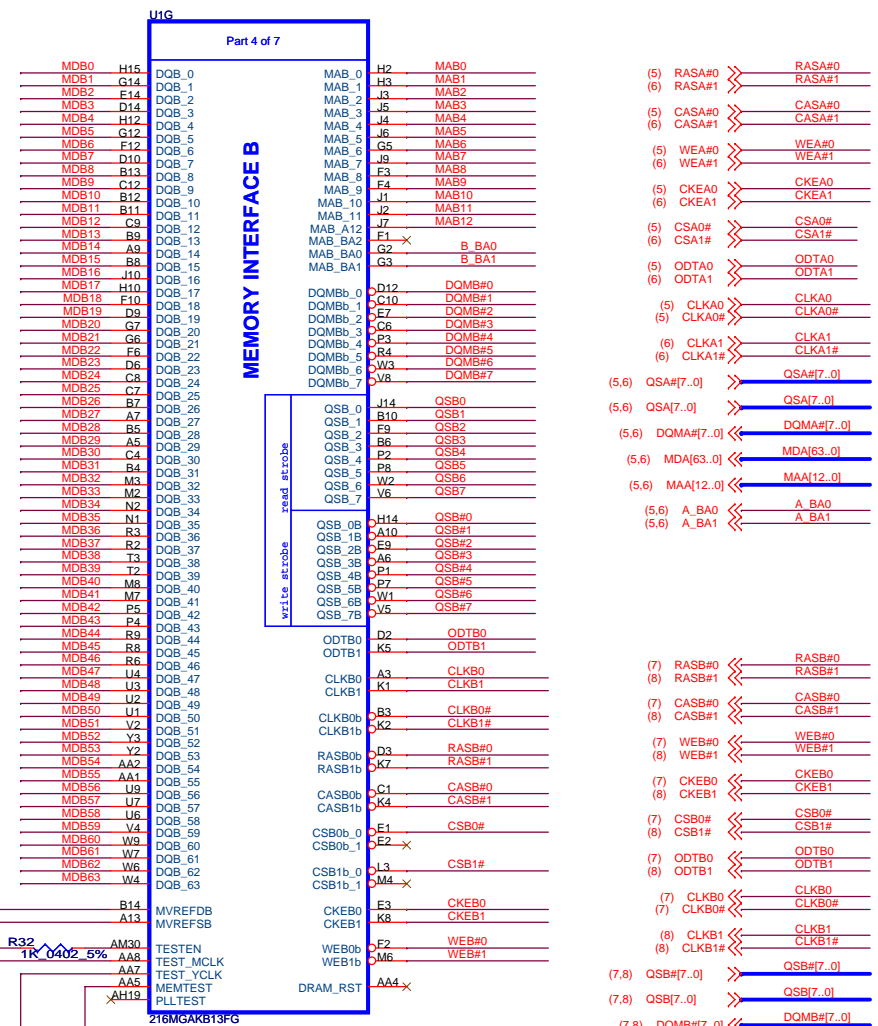
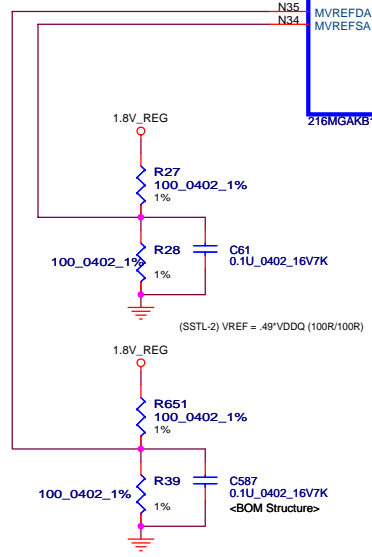
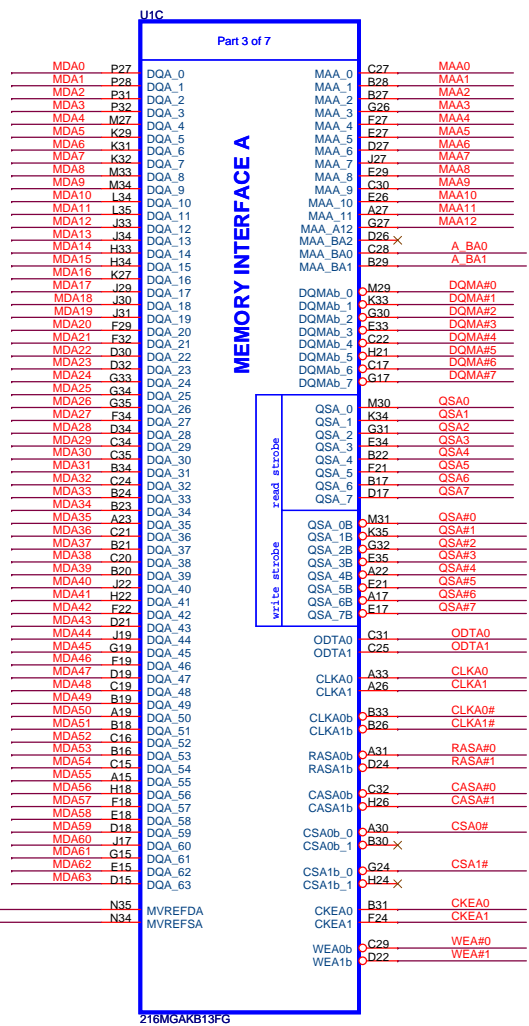


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Title	M71-M DDR2 MXM II
Document Number	105-B064xx-00A
Size	C
Date	Monday, December 04, 2006
Sheet	3 of 14
Rev	0



<Variant Name>

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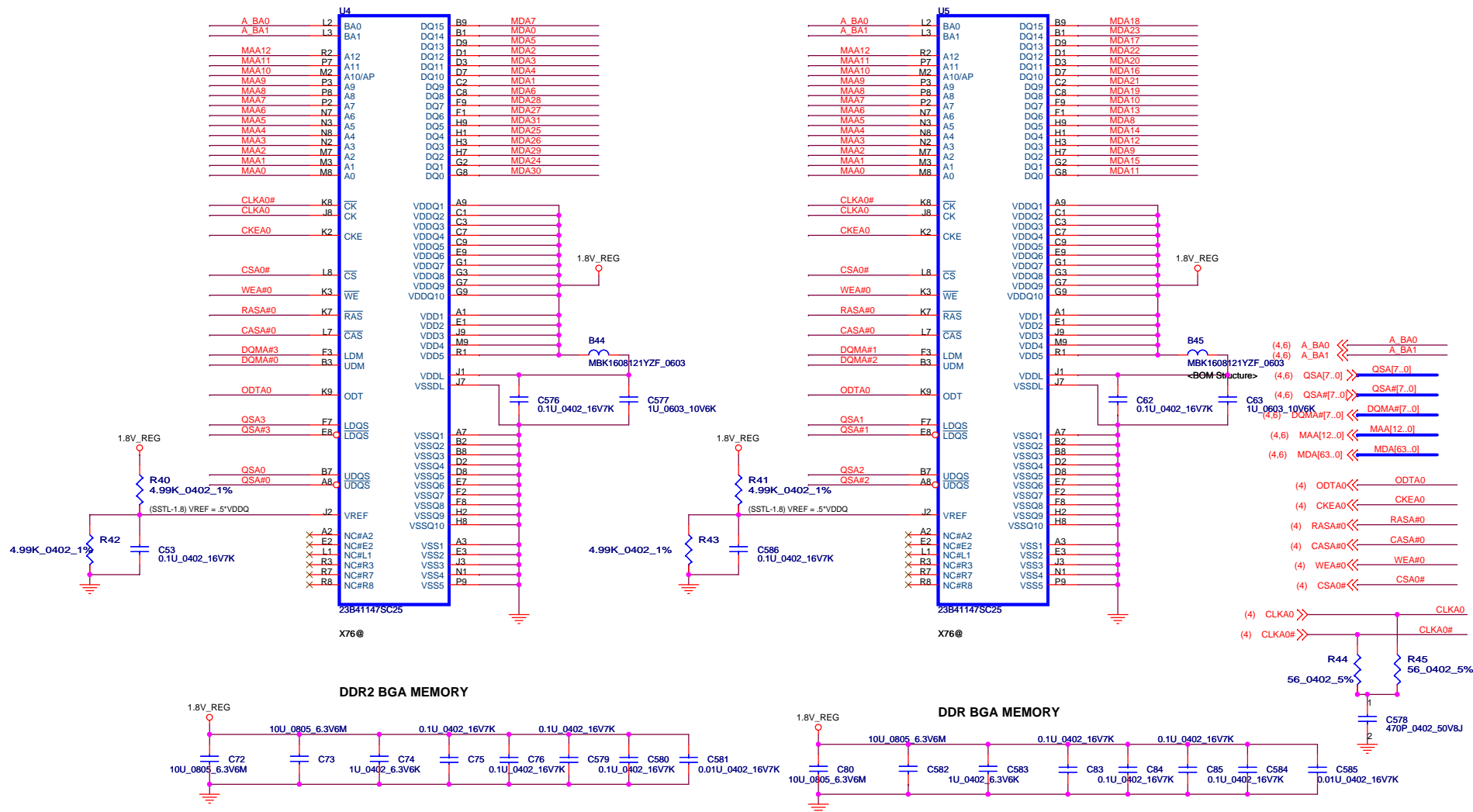
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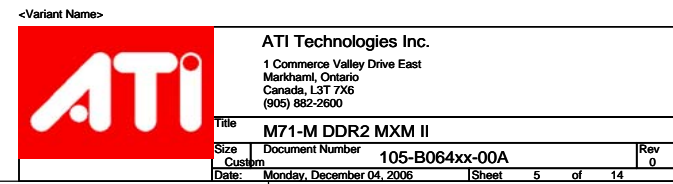
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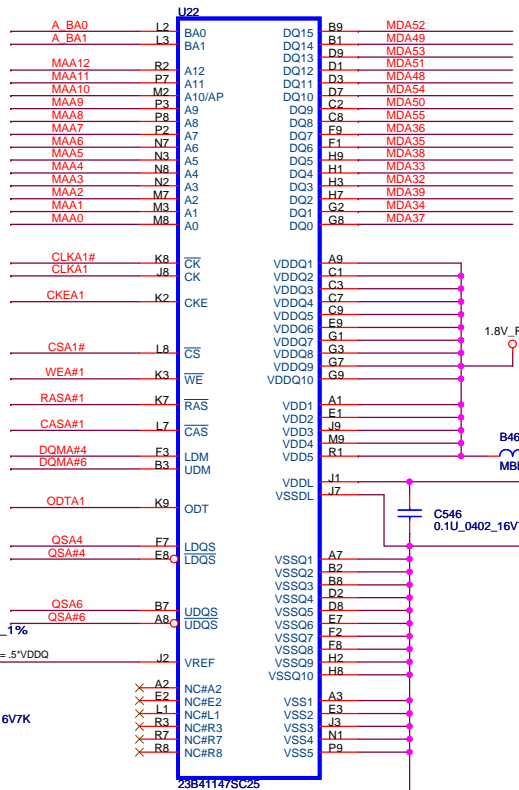
Date: Monday, December 04, 2006 Sheet 4 of 14

Rev 0

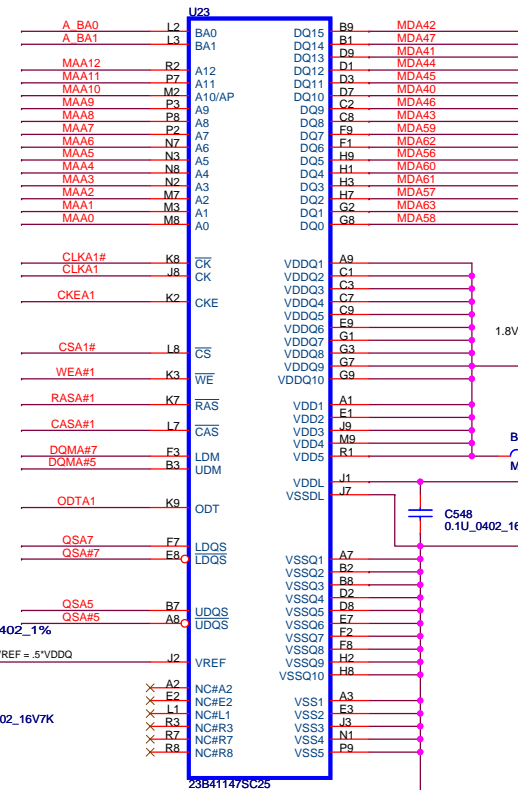
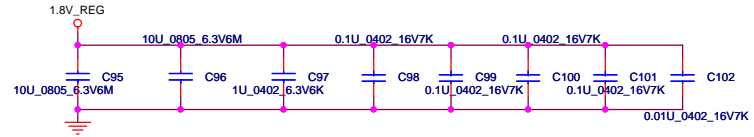


CHAN A RANK 0 DDR2 BGA MEMORY

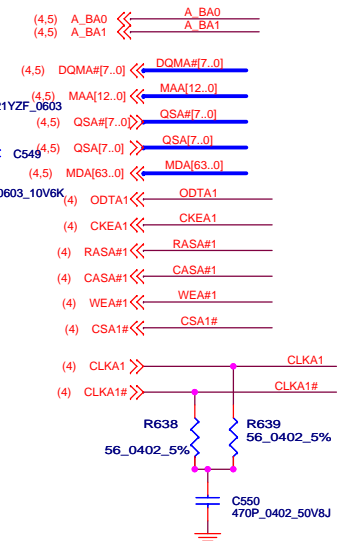
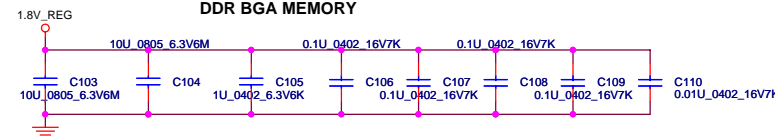




DDR2 BGA MEMORY

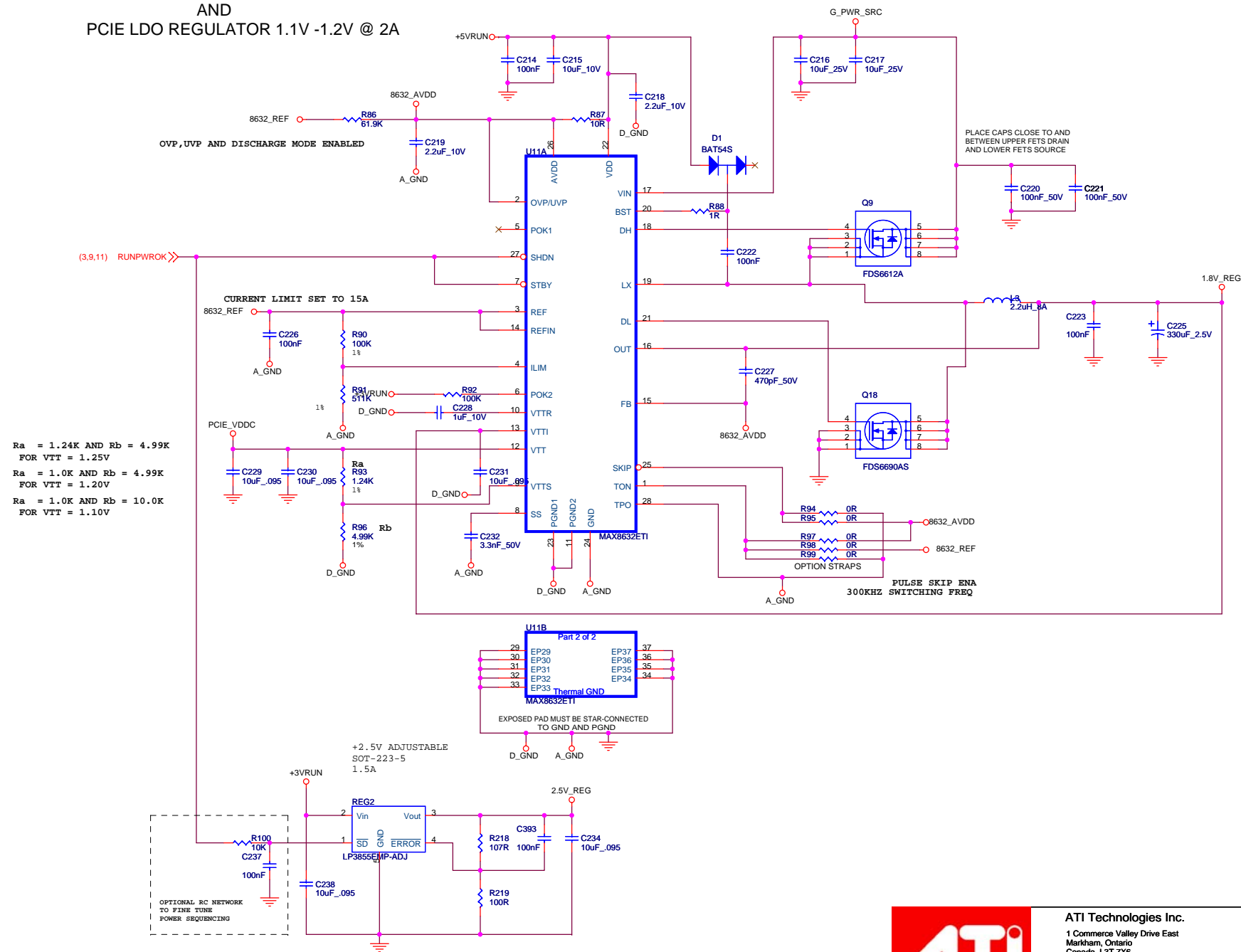


DDR2 BGA MEMORY



CHAN B RANK 0 DDR2 BGA MEMORY

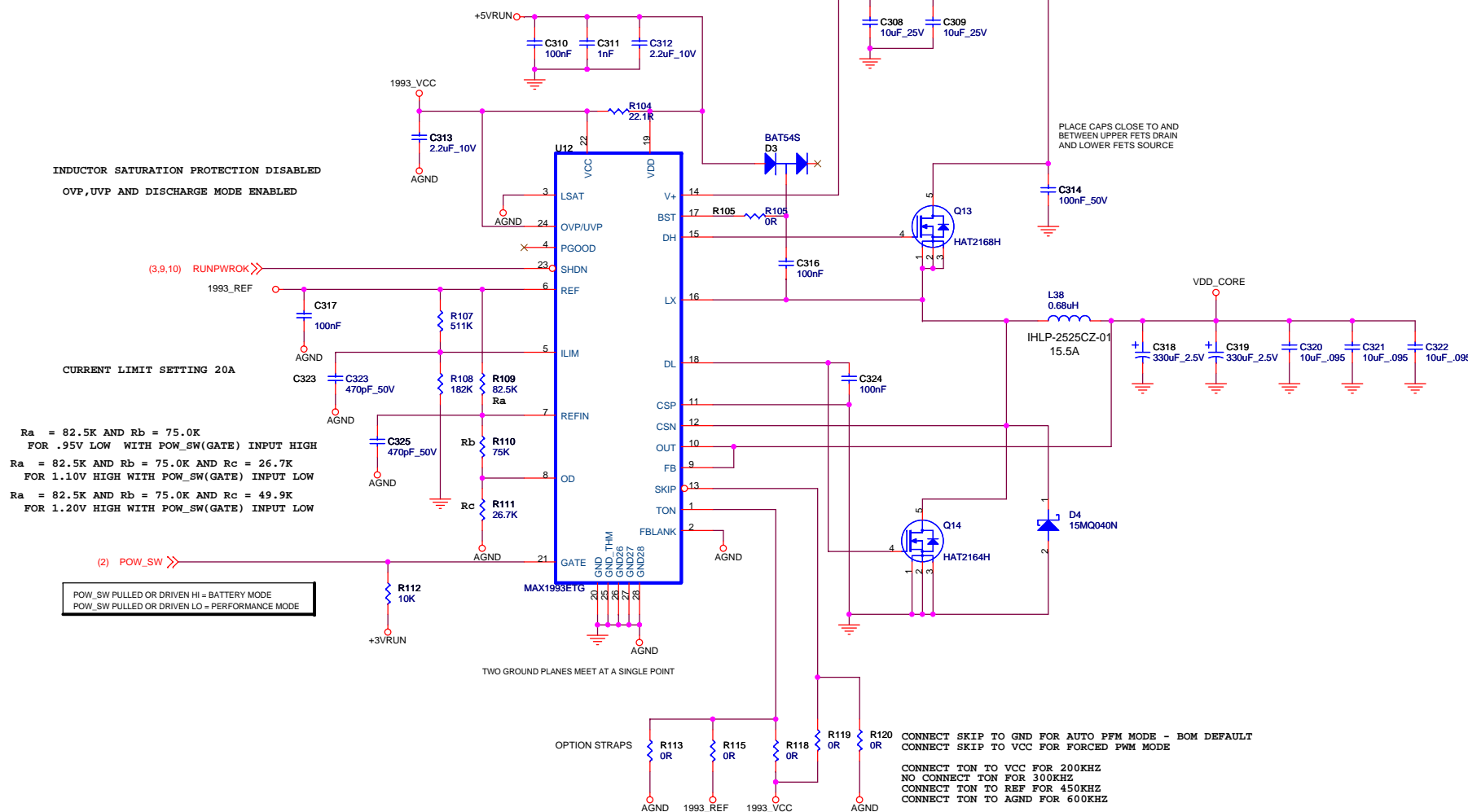
I/O PWM REGULATOR 1.8V @ 8A
AND
PCIE LDO REGULATOR 1.1V -1.2V @ 2A



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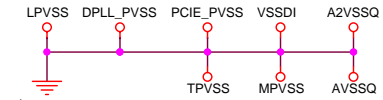
Title		M71-M DDR2 MXM II	
Size B	Document Number	105-B064xx-00A	Rev 0
Date:	Saturday, August 19, 2006	Sheet	10 of 14

CORE PWM REGULATOR .95V - 1.0V - 1.2V @ 15A




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Size	Custom	Document Number	105-B064xx-00A
Date	Saturday, August 19, 2006	Sheet	11 of 14



* PLACE ALL DECOUPLING CAPS CLOSE TO THE ASIC AND RUN DEDICATED TRACES FROM ASIC PINS TO JOIN THE GROUND PLANE WITH ONE VIA AT THE CAP

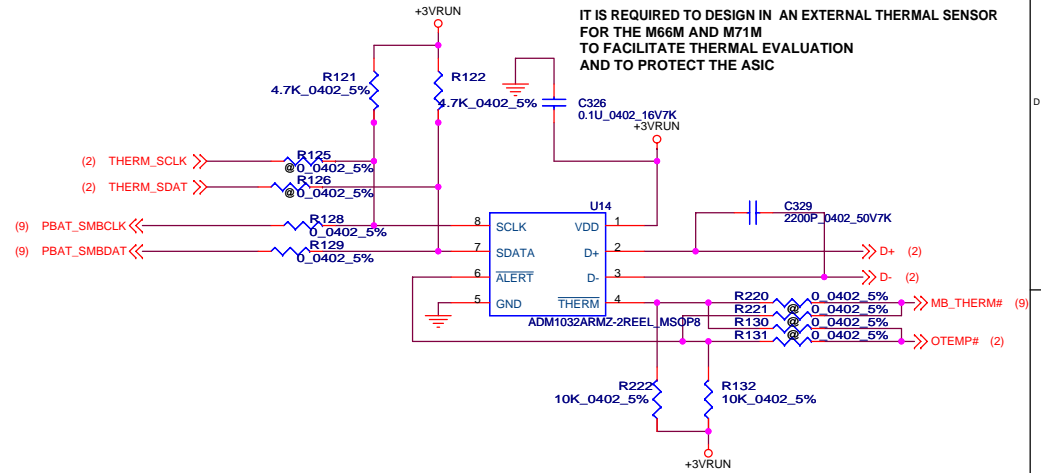
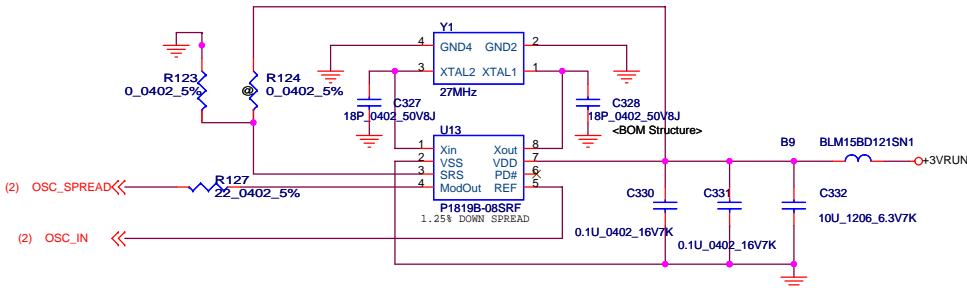
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Title		M71-M DDR2 MXM II	
Size	Document Number	105-B064xx-00A	
B			Rev 0
Date:	Monday, December 04, 2006	Sheet	12 of 14

MEMORY CLOCK SPREAD SPECTRUM

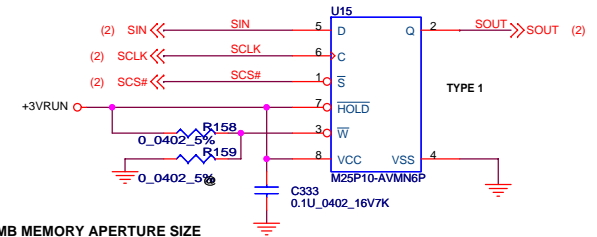


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS	
			M66M,M71M	M72M,M76M
BIF_MSI_DIS	VID1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_64BAR_EN_A	VID5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MUXED OUT	0	0
PLL_IBIAS_RD_1	GPIO6	(M66/71)BIAS CURRENT FOR PCIE PHY PLL MSBIT (M72/76)RSVD	0	0
PLL_IBIAS_RD_0	GPIO5	(M66/71)BIAS CURRENT FOR PCIE PHY PLL LSBIT (M72/76)RSVD	1	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1	1
ROMIDCFG(3:0)	GPIO[9,13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYN	IGNORE VIP DEVICE STRAPS	X	X
BIF_VGA_DIS	PSYN	VGA ENABLED	NA	0
MEM_TYPE	UNUSED GPIO	MEMORY TYPE,MAKE AND SIZE INFO	X X X	X X X

FLASH ROM



ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

VID0	VID2	VID3	VID4	VID6	VID7	HSYN	DVALID	GPIO2	GPIO3	GPIO5	GPIO6	GPIO8	VHAD0
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET													
GPIO_28_TDO	GENERICC	GPIO21_BB_EN	GPIO_23_CLKREQB (DRIVES LOW DURING RESET)	H2SYN	V2SYN								

<Variant Name>



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Title	M71-M DDR2 MXM II
Size	Document Number
Custom	105-B064xx-00A
Date:	Tuesday, February 27, 2007
Sheet	13 of 14
Rev	0

Vedio Memory Config. (VGA Internal PD) 1.8V only					Size	Vendor	Chips
MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0				
0	0	0	0		64MB	16Mx16	Samsung x2
0	0	0	1		128MB	16Mx16	Samsung x4
0	0	1	0		Default	256MB	16Mx16 Samsung x8
0	0	1	1		64MB	16Mx16	Hynix x2
0	1	0	0		128MB	16Mx16	Hynix x4
0	1	0	1		256MB	16Mx16	Hynix x8
0	1	1	0		64MB	16Mx16	Infineon x2
0	1	1	1		128MB	16Mx16	Infineon x4
1	0	0	0		256MB	16Mx16	Infineon x8



Schematic No.
105-B064xx-00A

Date: **Monday, December 04, 2006**

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.

Rev 0

[illegible]