P1041-B02

GF114, 768/1024MB 1536MB/2048MB, GDDR5 192b/256b 32M/64Mx32
DVI-I-DL, DVI-I-DL/DP, mHDMI

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SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11041-BASE-400	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0050	600-11041-0050-400	GF114-325, 1024MB, GDDR5 256b 32Mx32, DVI-I-DL, DVI-I-DL, mHDMI
2	SKU0060	600-11041-0060-400	GF114-300-KB, 1024MB, GDDR5 192b 64Mx32 & 32Mx32, DVI-I-DL, DVI-I-DL, mHDMI
3	SKU0061	600-11041-0061-400	GF114-300-KA, 768MB, GDDR5 192b 32Mx32, DVI-I-DL, DVI-I-DL, mHDMI
4	SKU0070	600-11041-0070-400	GF114-225, 1024MB, GDDR5 256b 32Mx32, DVI-I-DL, DVI-I-DL, mHDMI
5	SKU0075	600-11041-0075-400	GF114-200-KB, 1024MB, GDDR5 192b 64Mx32, & 32Mx32, DVI-IDL, DVI-I-DL, mHDMI
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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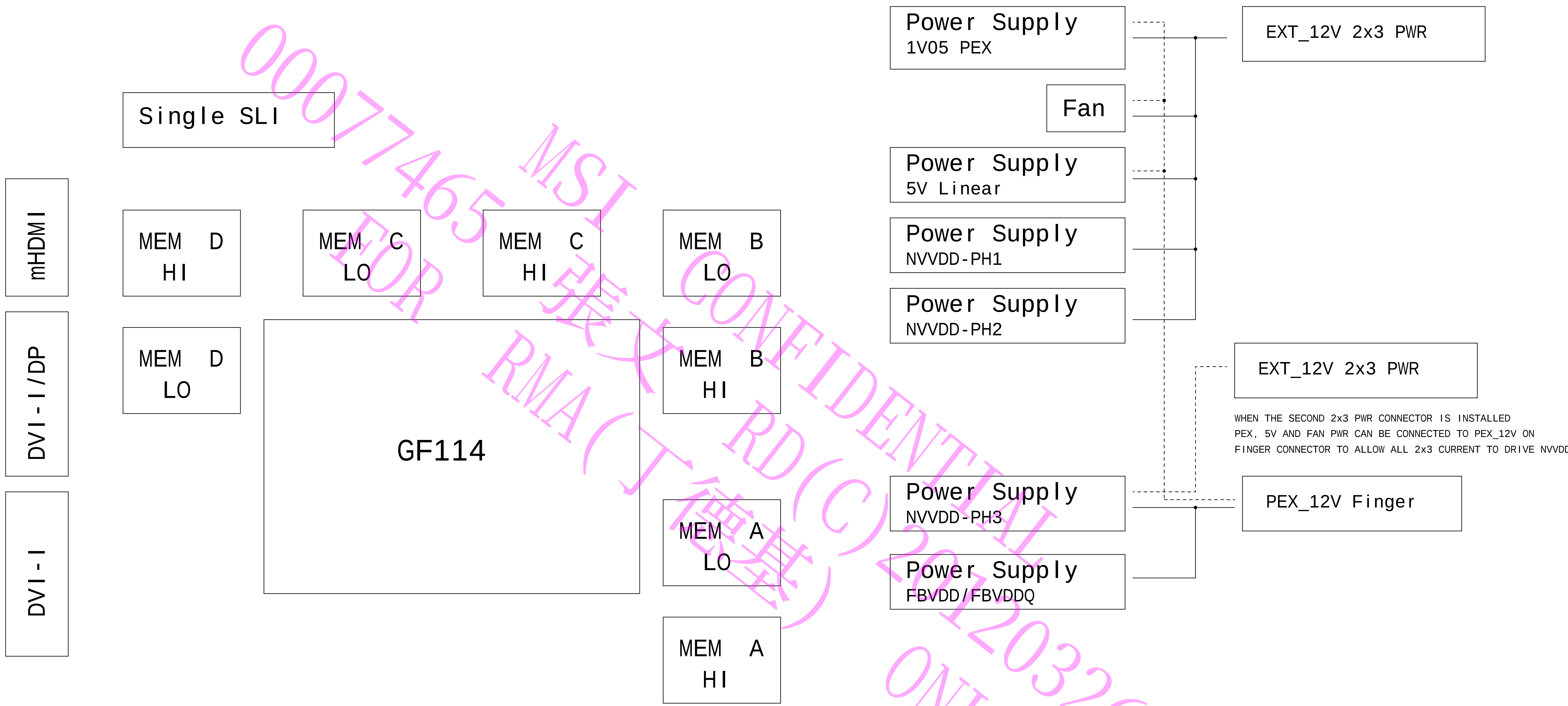
Page2: Block Diagram



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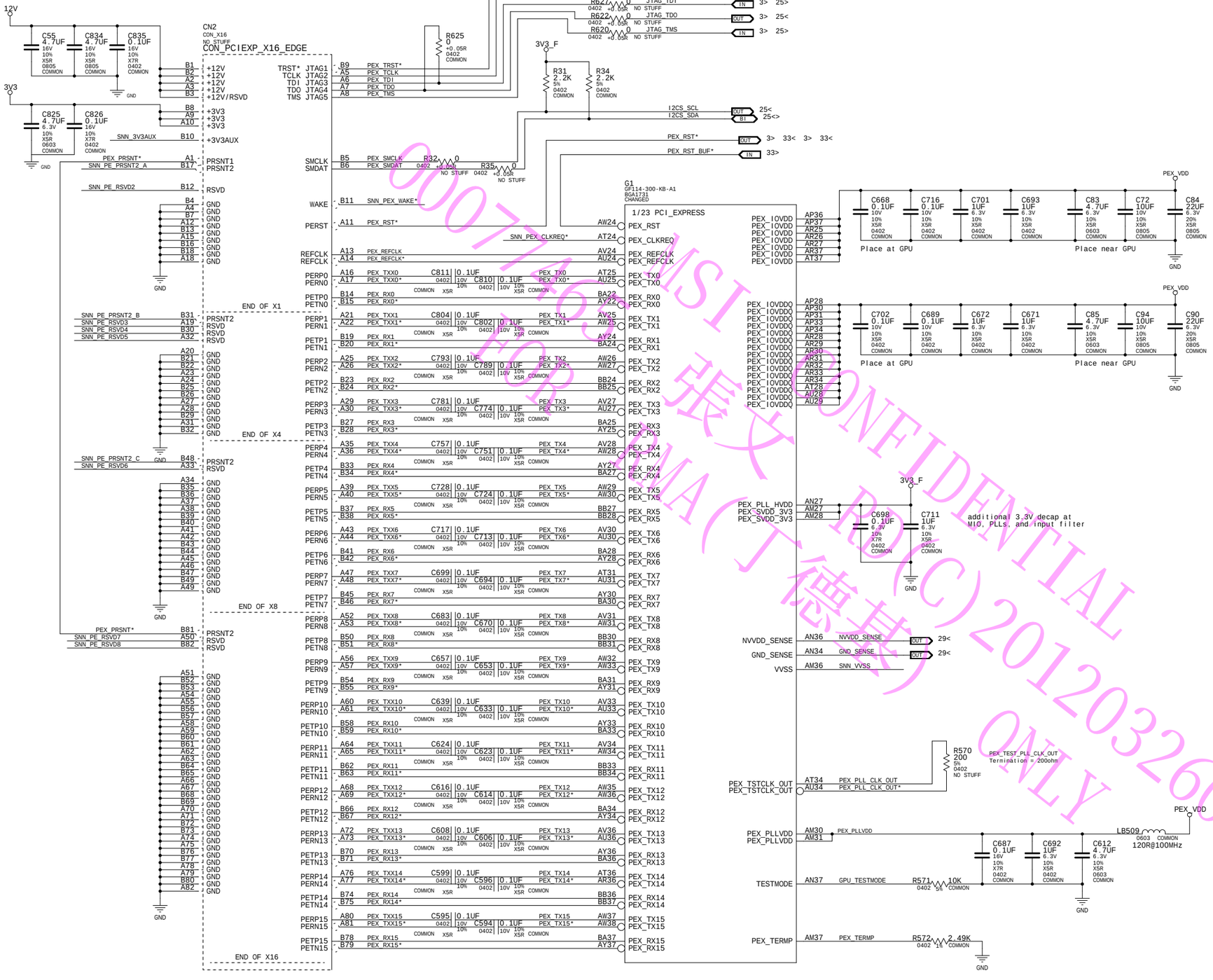
Page3: PCI Express



PEX NET RULES

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PEX_REFCLK*	1	90DIFF	PEX_REFCLK
PEX_TXX0	1	90DIFF	PEX_TXX0
PEX_TXX0*	1	90DIFF	PEX_TXX0
PEX_TXX1	1	90DIFF	PEX_TXX1
PEX_TXX1*	1	90DIFF	PEX_TXX1
PEX_TXX2	1	90DIFF	PEX_TXX2
PEX_TXX2*	1	90DIFF	PEX_TXX2
PEX_TXX3	1	90DIFF	PEX_TXX3
PEX_TXX3*	1	90DIFF	PEX_TXX3
PEX_TXX4	1	90DIFF	PEX_TXX4
PEX_TXX4*	1	90DIFF	PEX_TXX4
PEX_TXX5	1	90DIFF	PEX_TXX5
PEX_TXX5*	1	90DIFF	PEX_TXX5
PEX_TXX6	1	90DIFF	PEX_TXX6
PEX_TXX6*	1	90DIFF	PEX_TXX6
PEX_TXX7	1	90DIFF	PEX_TXX7
PEX_TXX7*	1	90DIFF	PEX_TXX7
PEX_TXX8	1	90DIFF	PEX_TXX8
PEX_TXX8*	1	90DIFF	PEX_TXX8
PEX_TXX9	1	90DIFF	PEX_TXX9
PEX_TXX9*	1	90DIFF	PEX_TXX9
PEX_TXX10	1	90DIFF	PEX_TXX10
PEX_TXX10*	1	90DIFF	PEX_TXX10
PEX_TXX11	1	90DIFF	PEX_TXX11
PEX_TXX11*	1	90DIFF	PEX_TXX11
PEX_TXX12	1	90DIFF	PEX_TXX12
PEX_TXX12*	1	90DIFF	PEX_TXX12
PEX_TXX13	1	90DIFF	PEX_TXX13
PEX_TXX13*	1	90DIFF	PEX_TXX13
PEX_TXX14	1	90DIFF	PEX_TXX14
PEX_TXX14*	1	90DIFF	PEX_TXX14
PEX_TXX15	1	90DIFF	PEX_TXX15
PEX_TXX15*	1	90DIFF	PEX_TXX15
PEX_RX0	1	90DIFF	PEX_RX0
PEX_RX0*	1	90DIFF	PEX_RX0
PEX_RX1	1	90DIFF	PEX_RX1
PEX_RX1*	1	90DIFF	PEX_RX1
PEX_RX2	1	90DIFF	PEX_RX2
PEX_RX2*	1	90DIFF	PEX_RX2
PEX_RX3	1	90DIFF	PEX_RX3
PEX_RX3*	1	90DIFF	PEX_RX3
PEX_RX4	1	90DIFF	PEX_RX4
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PEX_RX5*	1	90DIFF	PEX_RX5
PEX_RX6	1	90DIFF	PEX_RX6
PEX_RX6*	1	90DIFF	PEX_RX6
PEX_RX7	1	90DIFF	PEX_RX7
PEX_RX7*	1	90DIFF	PEX_RX7
PEX_RX8	1	90DIFF	PEX_RX8
PEX_RX8*	1	90DIFF	PEX_RX8
PEX_RX9	1	90DIFF	PEX_RX9
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PEX_RX10	1	90DIFF	PEX_RX10
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PEX_RX14*	1	90DIFF	PEX_RX14
PEX_RX15	1	90DIFF	PEX_RX15
PEX_RX15*	1	90DIFF	PEX_RX15
PEX_TX0	1	90DIFF	PEX_TX0
PEX_TX0*	1	90DIFF	PEX_TX0
PEX_TX1	1	90DIFF	PEX_TX1
PEX_TX1*	1	90DIFF	PEX_TX1
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PEX_TX2*	1	90DIFF	PEX_TX2
PEX_TX3	1	90DIFF	PEX_TX3
PEX_TX3*	1	90DIFF	PEX_TX3
PEX_TX4	1	90DIFF	PEX_TX4
PEX_TX4*	1	90DIFF	PEX_TX4
PEX_TX5	1	90DIFF	PEX_TX5
PEX_TX5*	1	90DIFF	PEX_TX5
PEX_TX6	1	90DIFF	PEX_TX6
PEX_TX6*	1	90DIFF	PEX_TX6
PEX_TX7	1	90DIFF	PEX_TX7
PEX_TX7*	1	90DIFF	PEX_TX7
PEX_TX8	1	90DIFF	PEX_TX8
PEX_TX8*	1	90DIFF	PEX_TX8
PEX_TX9	1	90DIFF	PEX_TX9
PEX_TX9*	1	90DIFF	PEX_TX9
PEX_TX10	1	90DIFF	PEX_TX10
PEX_TX10*	1	90DIFF	PEX_TX10
PEX_TX11	1	90DIFF	PEX_TX11
PEX_TX11*	1	90DIFF	PEX_TX11
PEX_TX12	1	90DIFF	PEX_TX12
PEX_TX12*	1	90DIFF	PEX_TX12
PEX_TX13	1	90DIFF	PEX_TX13
PEX_TX13*	1	90DIFF	PEX_TX13
PEX_TX14	1	90DIFF	PEX_TX14
PEX_TX14*	1	90DIFF	PEX_TX14
PEX_TX15	1	90DIFF	PEX_TX15
PEX_TX15*	1	90DIFF	PEX_TX15
PEX_PLL_CLK_OUT	1	90DIFF	PEX_PLL_CLK_OUT
PEX_PLL_CLK_OUT*	1	90DIFF	PEX_PLL_CLK_OUT
PEX_RST*	1	50OHM	
PRSNT*			
PEX_TRST*			
PEX_TCLK			
PEX_TDI			
PEX_TDO			
PEX_TMS			
JTAG_TCLK			
JTAG_TMS			
JTAG_TDI			
JTAG_TDO			
JTAG_TRST*			

NET		VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	NV_SOURCE_POWER_NET	12V	5.5A	24MIL
3V3	NV_SOURCE_POWER_NET	3.3V	3.0A	20MIL
GND	NV_SOURCE_POWER_NET	0V	8.5A	16MIL
PEX_PLLVDD		1.05V	0.16A	12MIL

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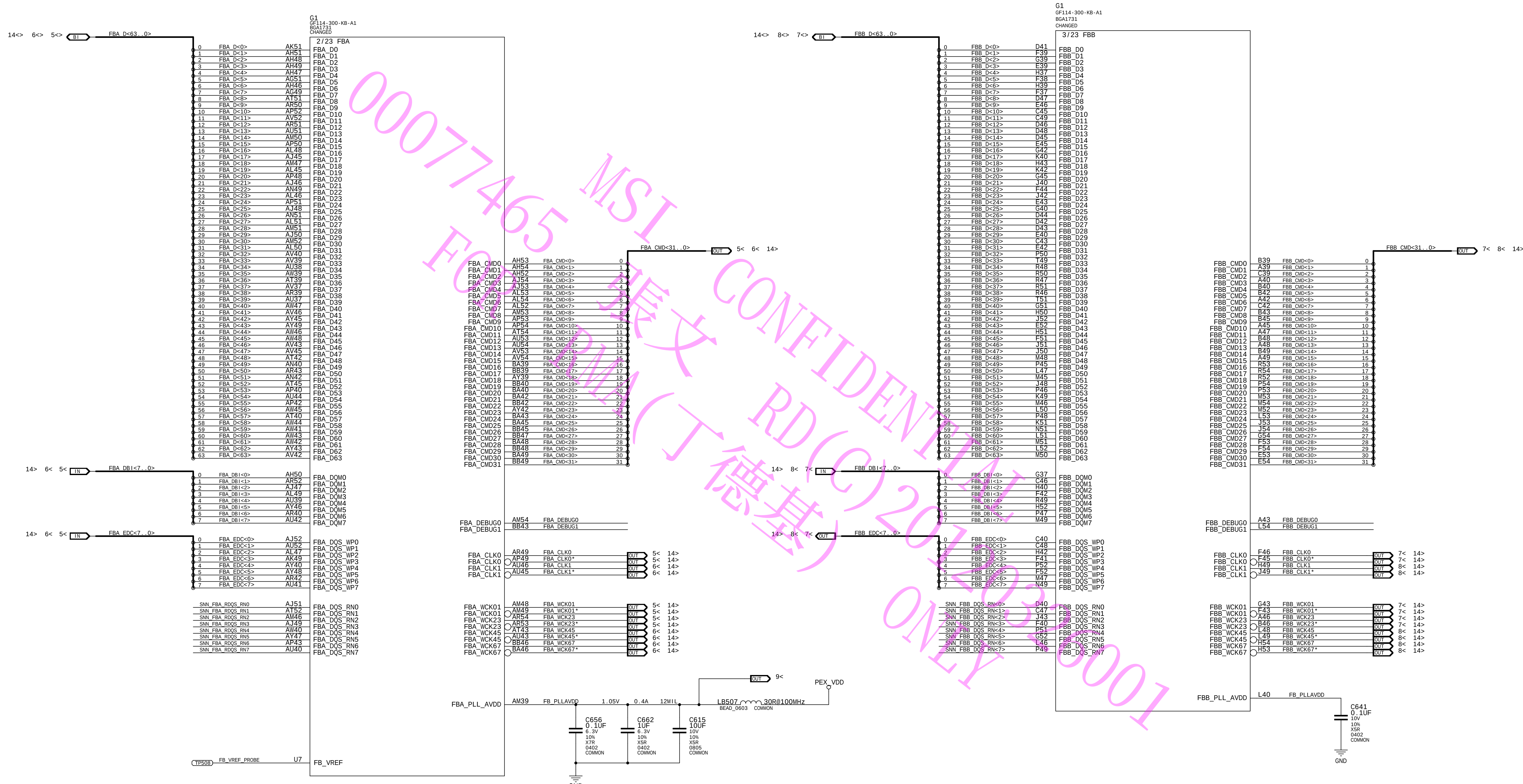

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU Partition A/B

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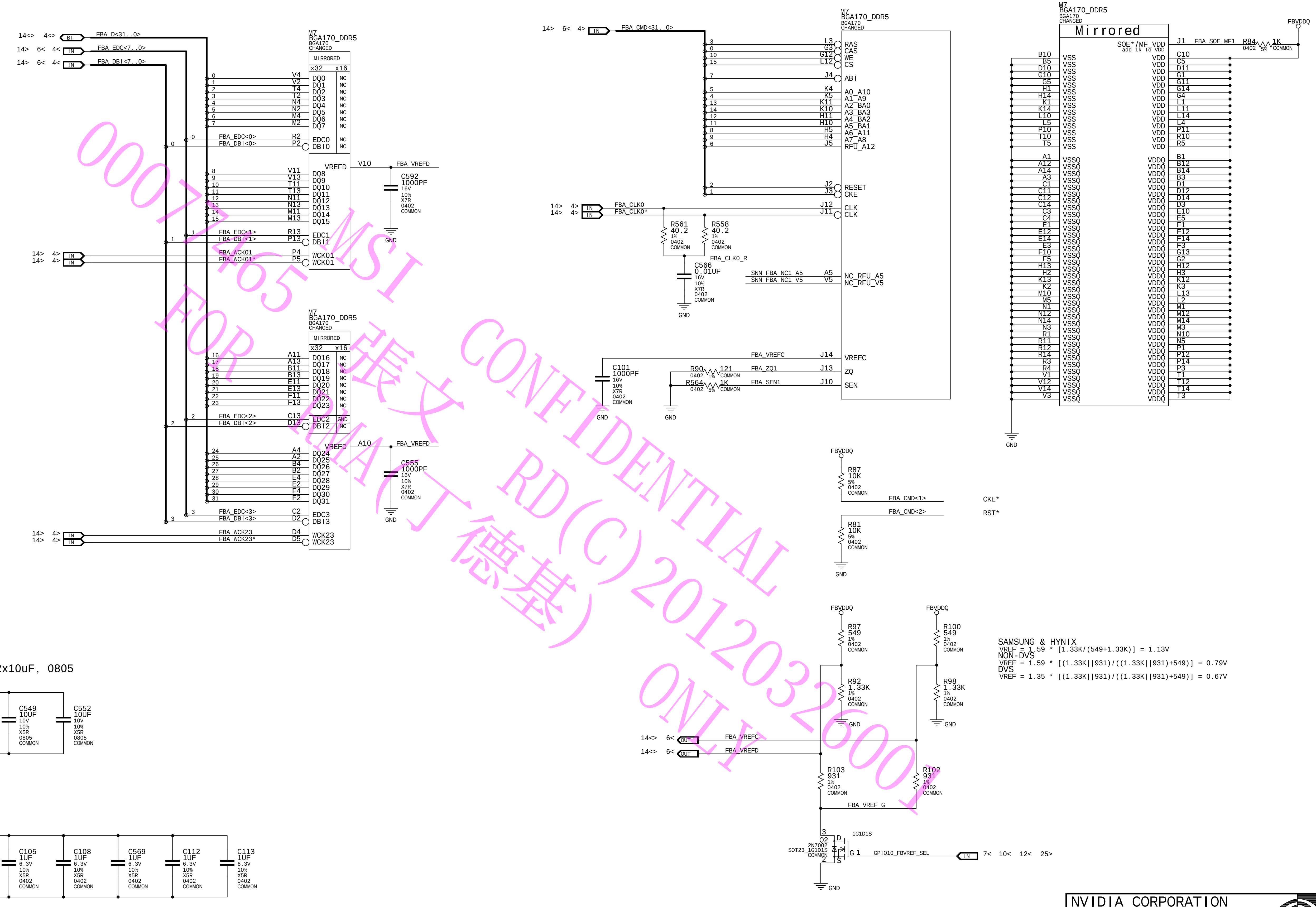
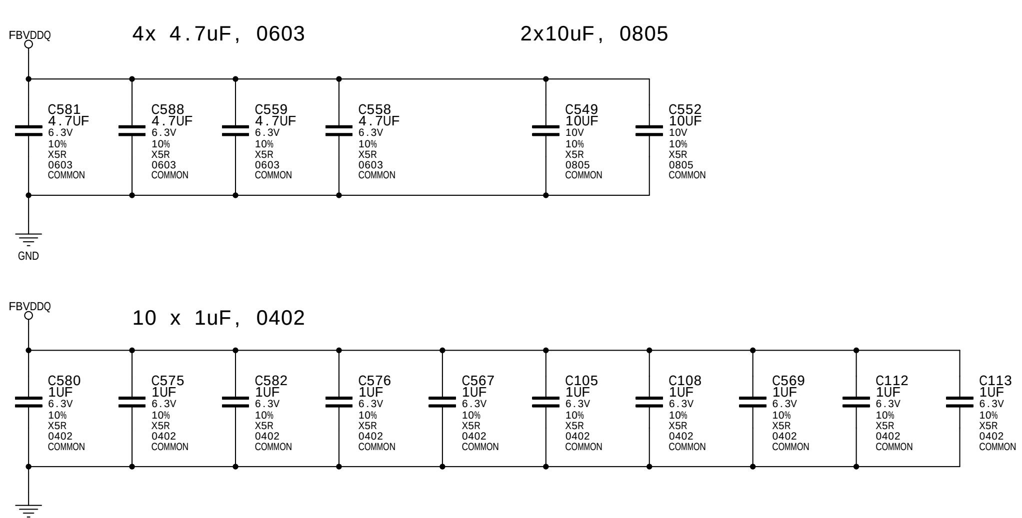
GDDR5 CMD Mapping

CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

** Vref switching options:
- internal Vref should be POR for VrefD





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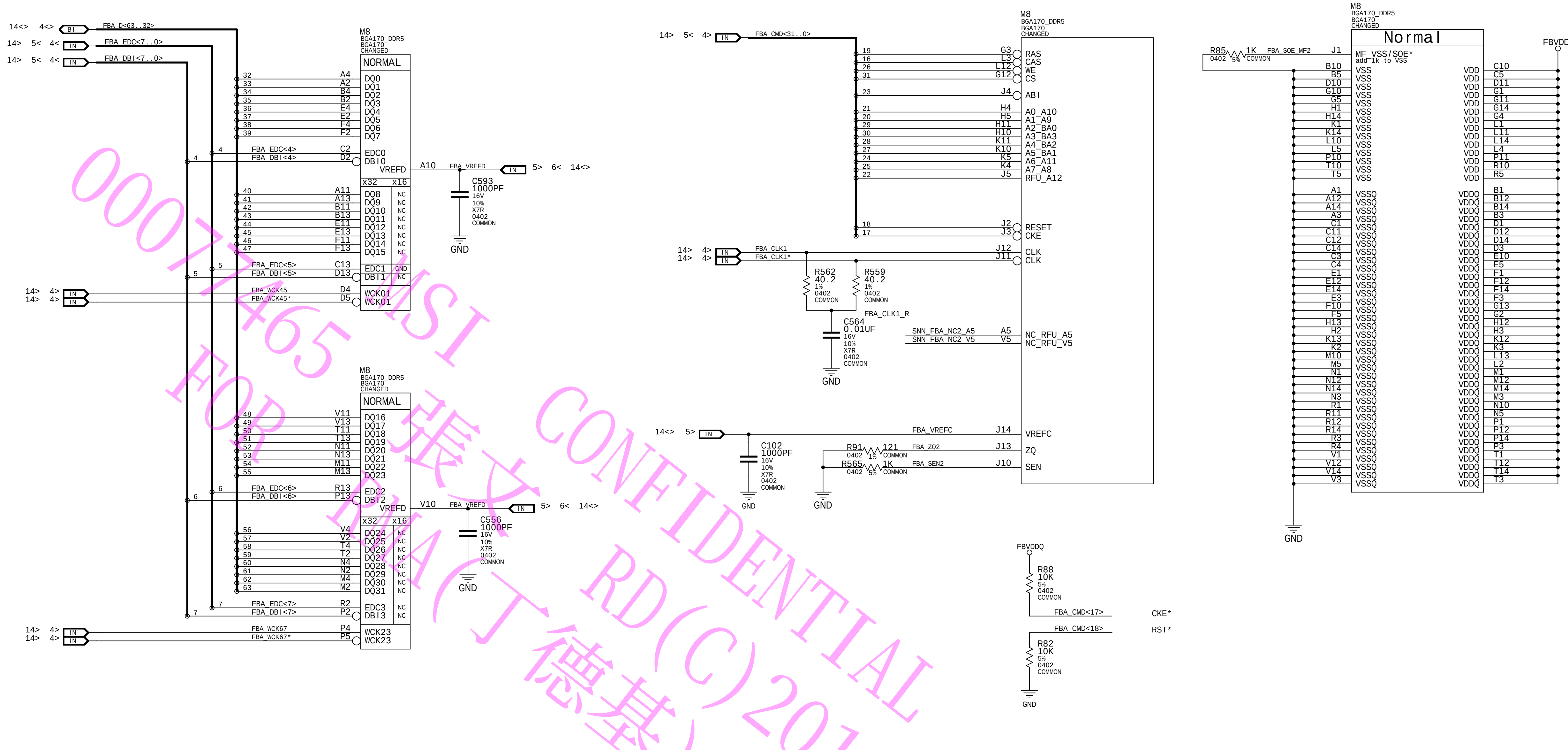
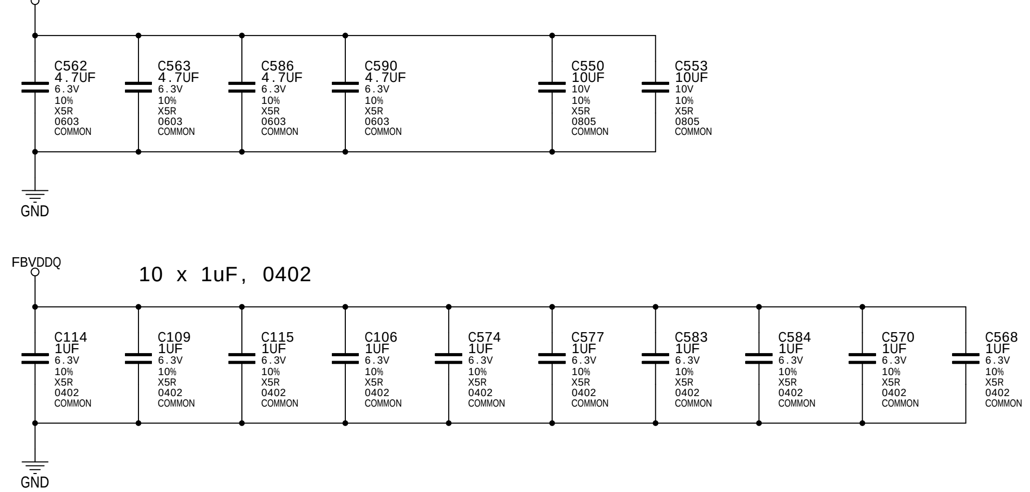
GDDR5 CMD Mapping

CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

** Vref switching options:
- internal Vref should be POR for VrefD





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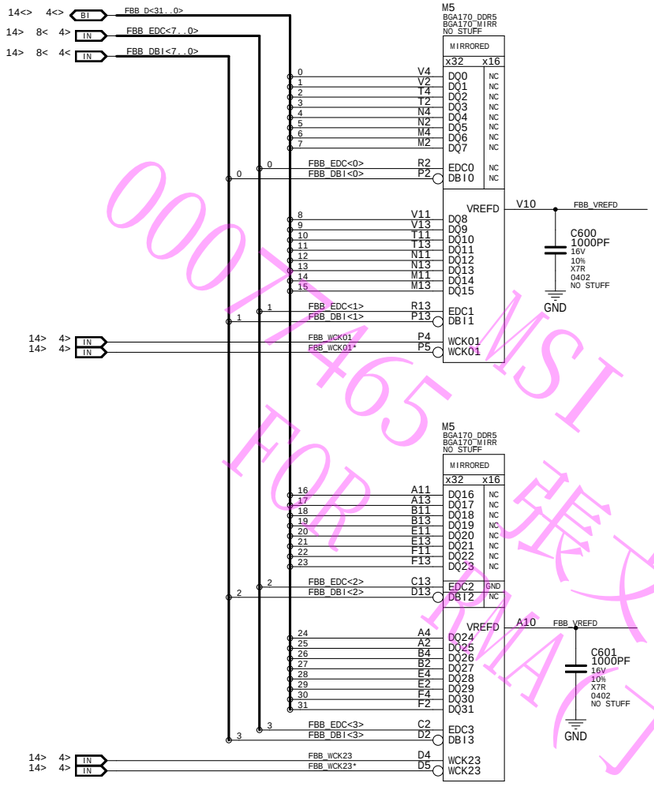
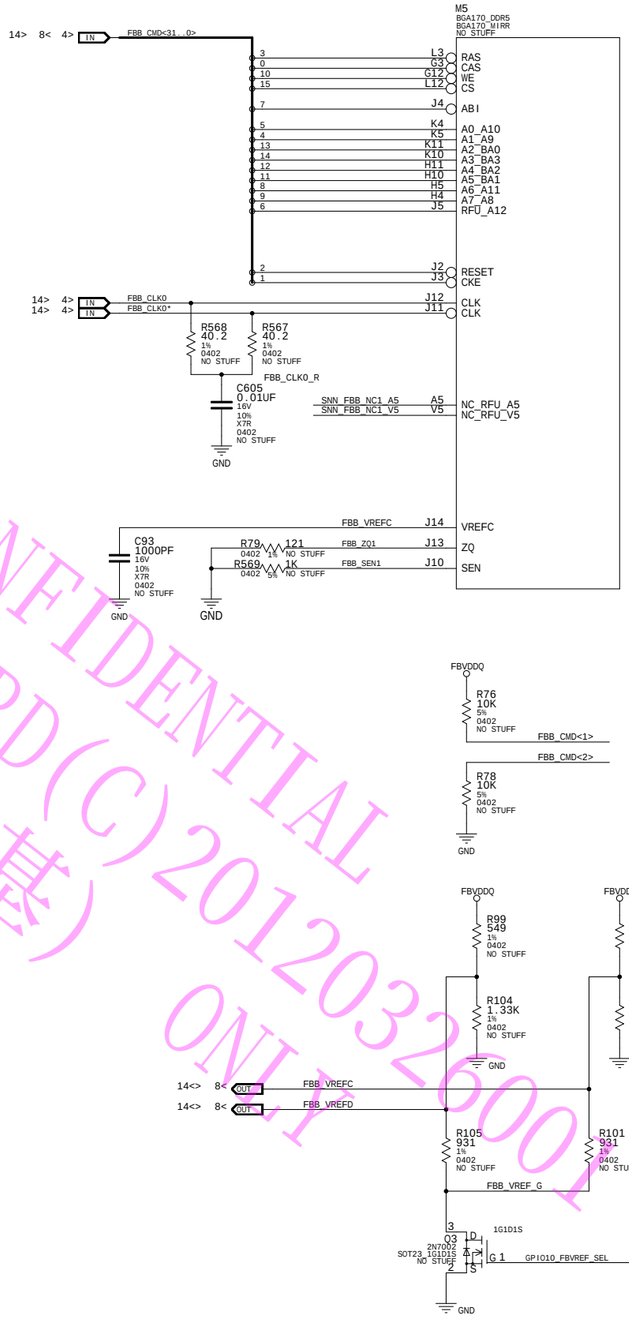
Page7: FBB Partition 31..0

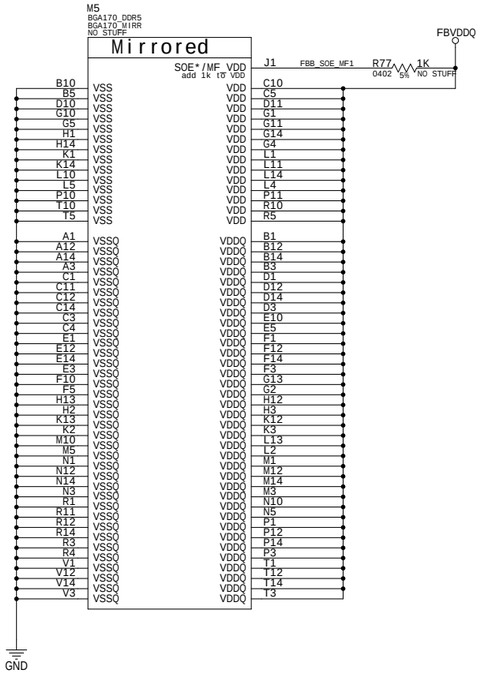
GDDR5 CMD Mapping

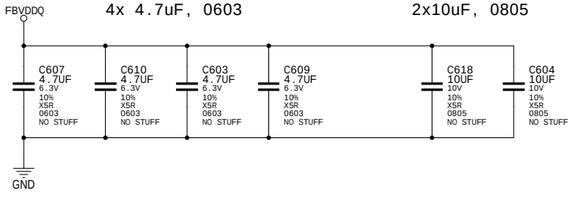
CMD	0..31	32..63
CMD0	CA5*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CA5*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

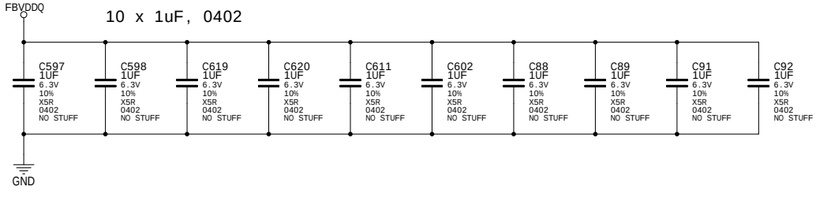
** Vref switching options:
- internal Vref should be POR for VrefD











SAMSUNG & HYNIX
VREF = 1.59 * [1.33K/(549+1.33K)] = 1.13V
NON-DVS
VREF = 1.59 * [(1.33K||931)/((1.33K||931)+549)] = 0.79V
DVS
VREF = 1.35 * [(1.33K||931)/((1.33K||931)+549)] = 0.67V

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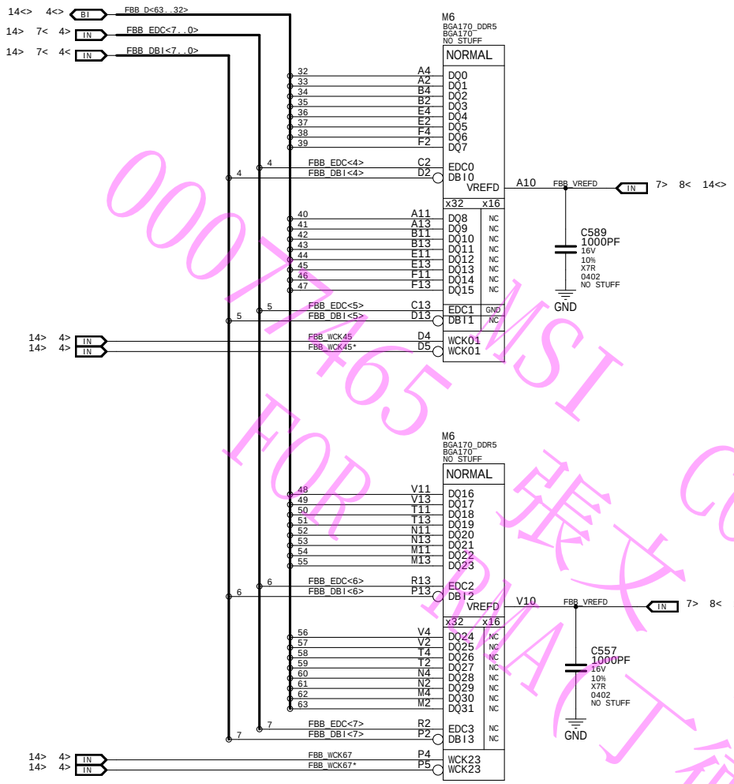
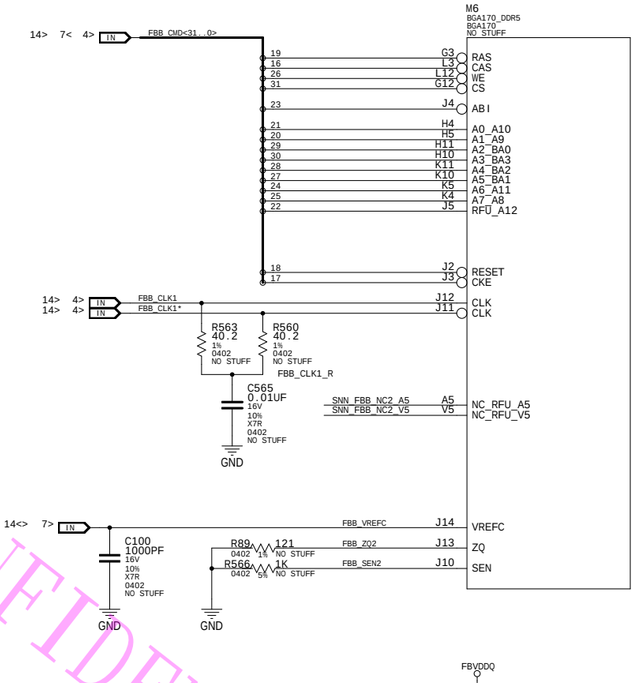
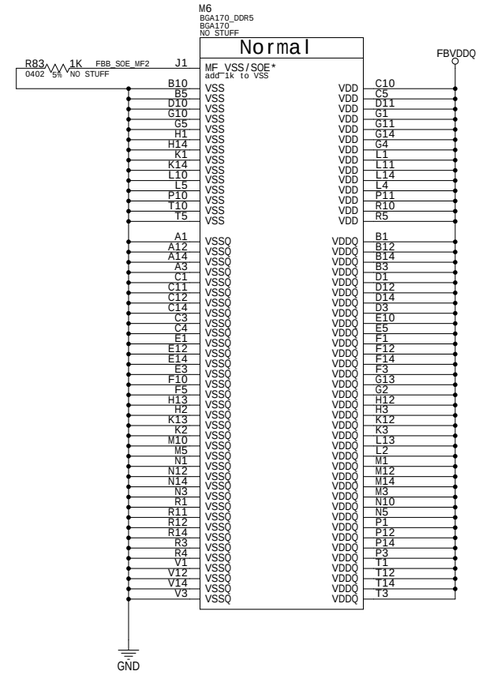
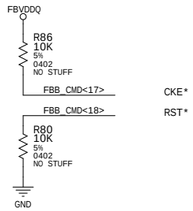
GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

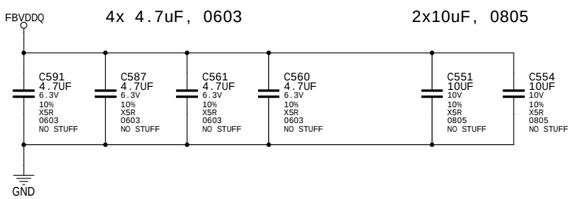
** Vref switching options:
- internal Vref should be POR for VrefD

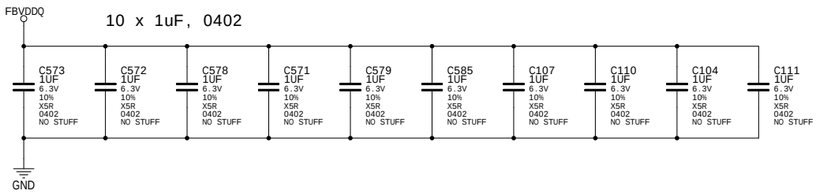












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PAGE DETAIL	FBB Partition 63..32

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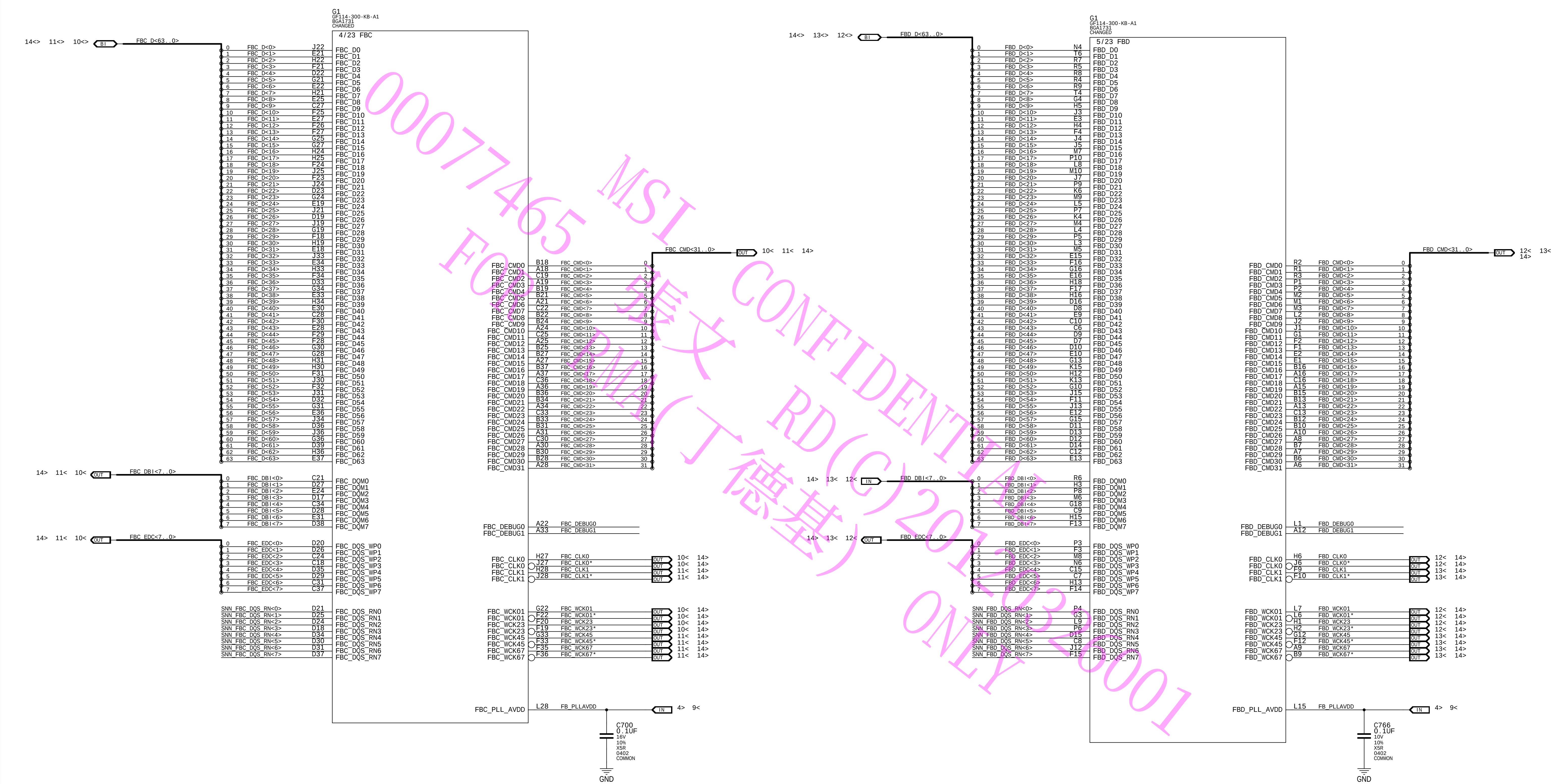
Page9: GPU Partition C/D



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PAGE DETAIL	GPU Partition C/D

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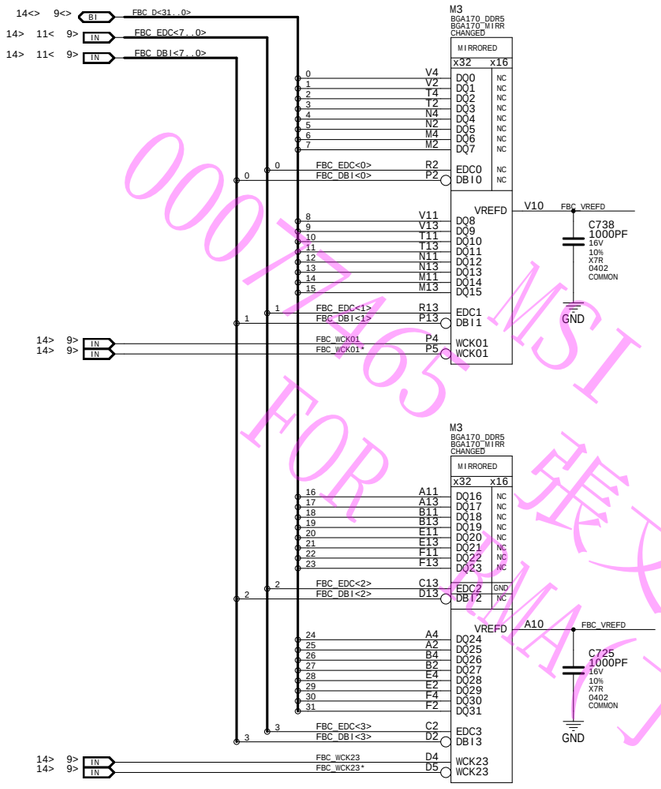
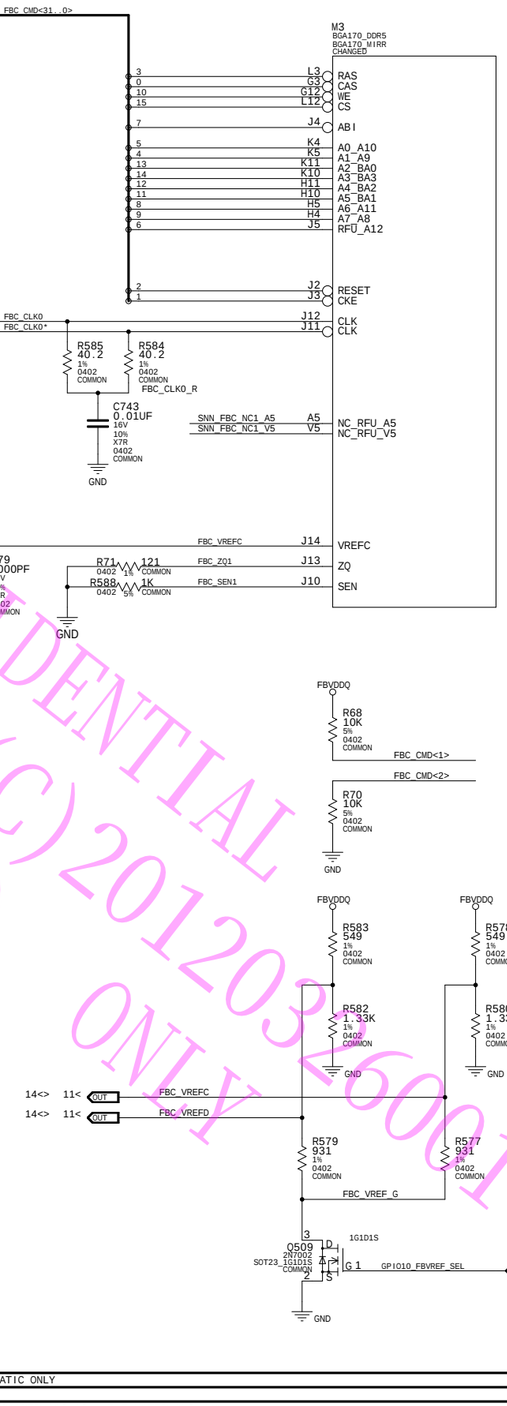
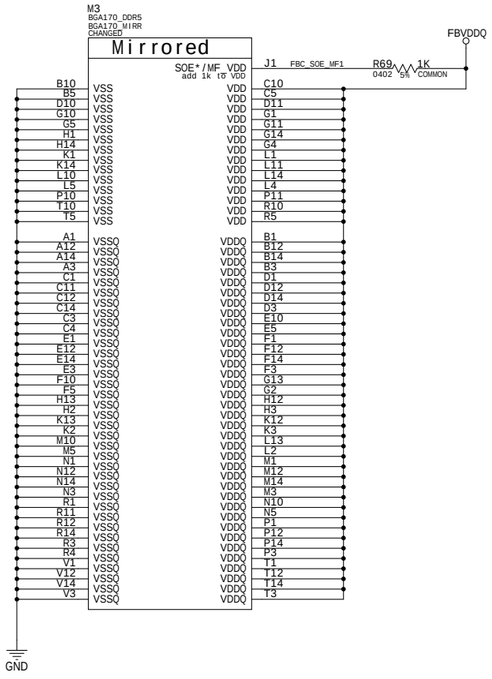
Page10: FBC Partition 31..0

GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A3_BA3	
CMD14	A2_BA0	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

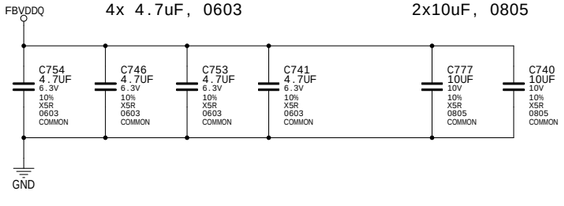
** Vref switching options:
- internal Vref should be POR for VrefD

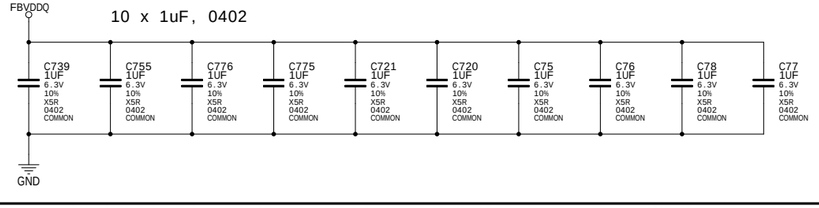






SAMSUNG & HYNIX
VREF = 1.59 * [1.33K/(549+1.33K)] = 1.13V
NON-DVS
VREF = 1.59 * [(1.33K||931)/((1.33K||931)+549)] = 0.79V
DVS
VREF = 1.35 * [(1.33K||931)/((1.33K||931)+549)] = 0.67V





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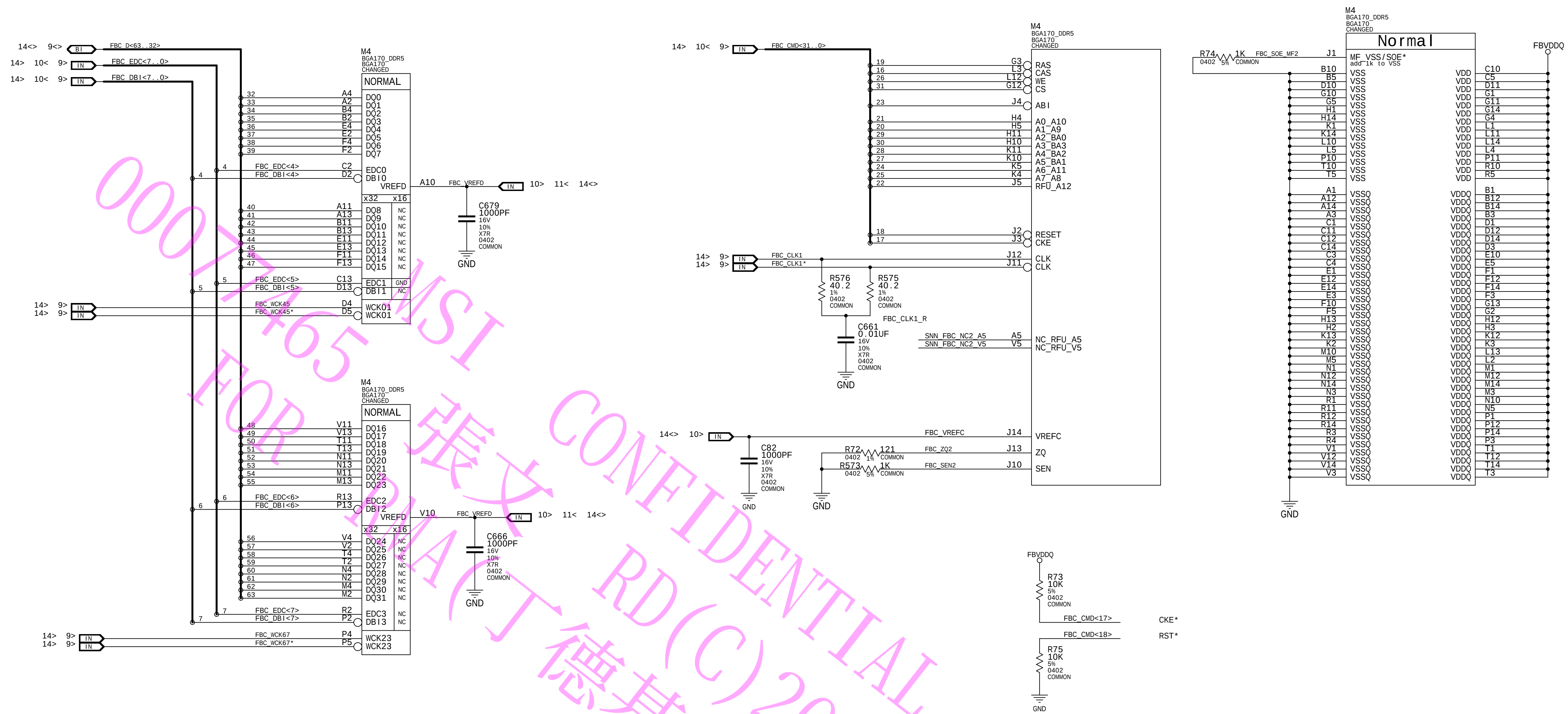
Page11: FBC Partition 63..32

GDDR5 CMD Mapping

CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

** Vref switching options:
- internal Vref should be POR for VrefD

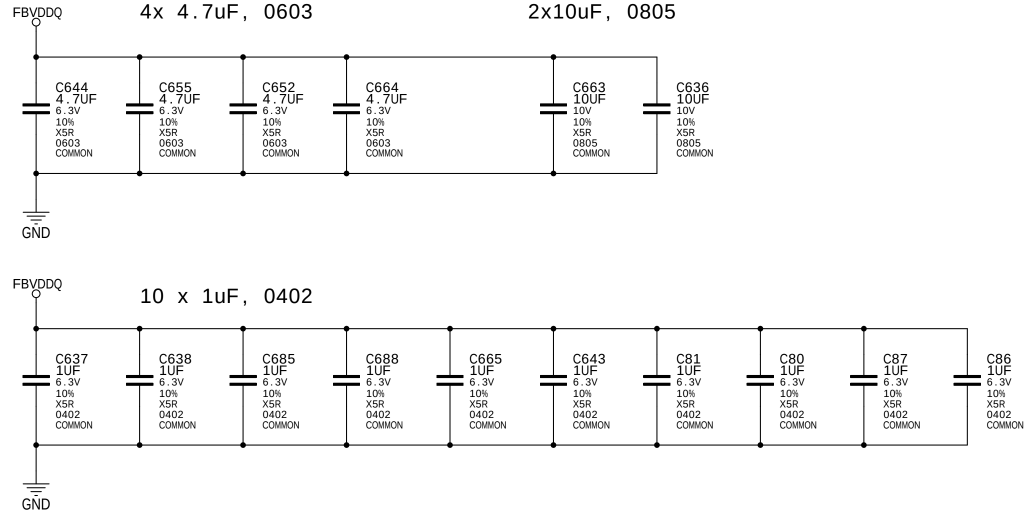


FBVDDQ

4x 4.7uF, 0603

2x10uF, 0805

10 x 1uF, 0402



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PAGE DETAIL	FBC Partition 63..32

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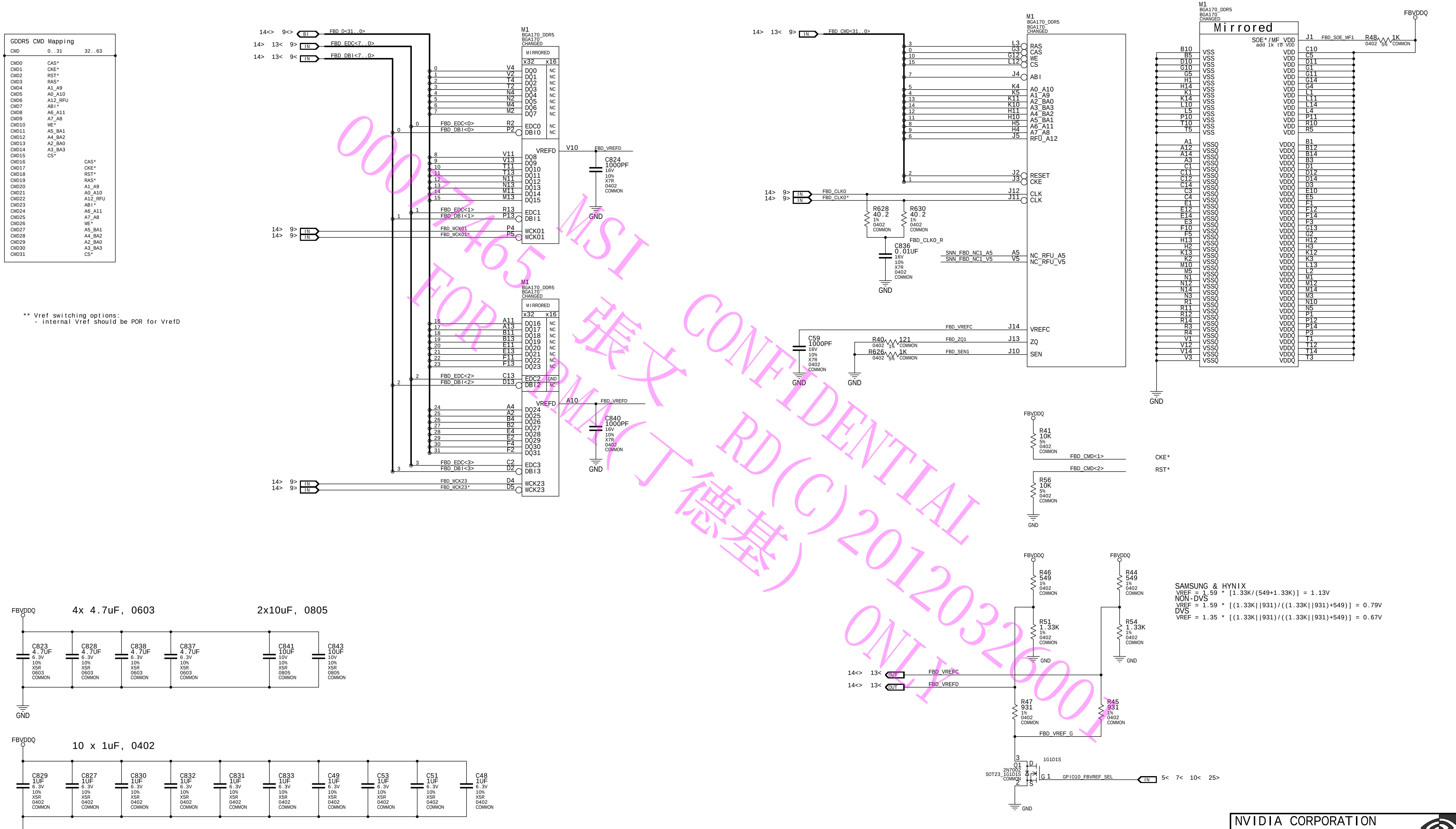
Page12: FBD Partition 31..0

GDDR5 CMD Mapping

CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

** Vref switching options:
- internal Vref should be POR for VrefD



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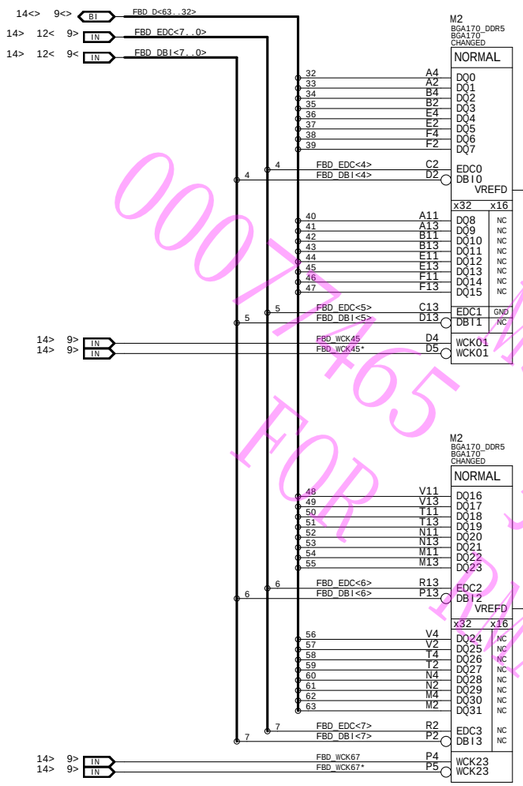
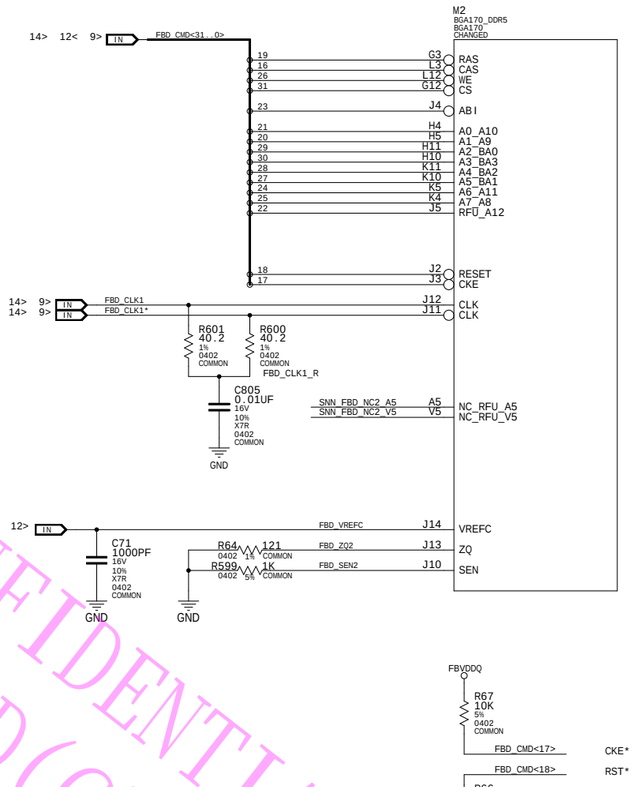
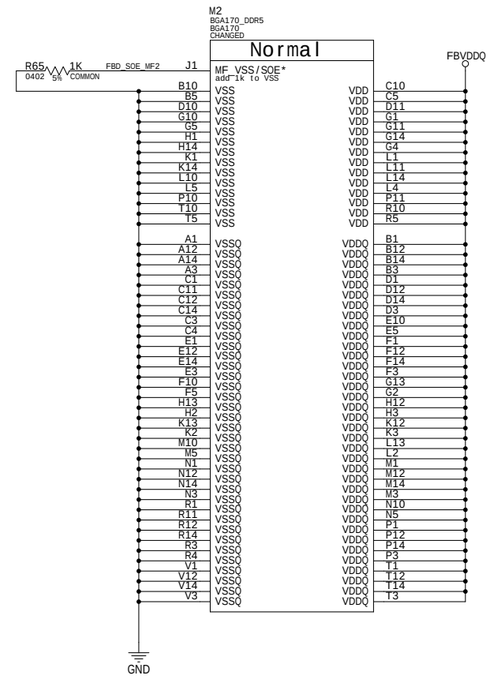
Page13: FBD Partition 63..32

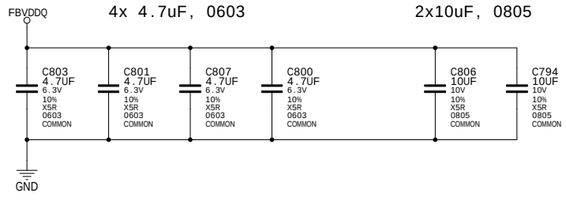
GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CA5*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CA5*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

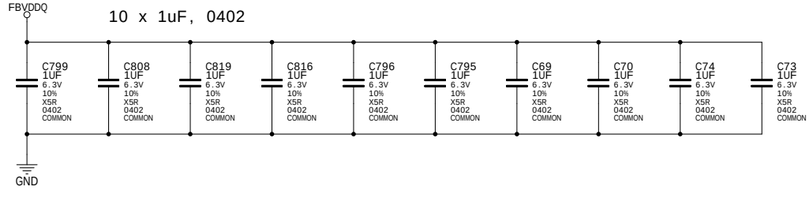
** Vref switching options:
- internal Vref should be POR for VrefD











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Page14: FB Net Properties

NET RULES for FrameBuffer A/B

Pages	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
5< 4>	OUT	FBA_CLK0	1	80DIFF	FBA_CLK0
5< 4>	OUT	FBA_CLK0*	1	80DIFF	FBA_CLK0
6< 4>	OUT	FBA_CLK1	1	80DIFF	FBA_CLK1
6< 4>	OUT	FBA_CLK1*	1	80DIFF	FBA_CLK1
7< 4>	OUT	FBB_WCK01	1	80DIFF	FBB_WCK01
7< 4>	OUT	FBB_WCK01*	1	80DIFF	FBB_WCK01
7< 4>	OUT	FBB_WCK23	1	80DIFF	FBB_WCK23
7< 4>	OUT	FBB_WCK23*	1	80DIFF	FBB_WCK23
8< 4>	OUT	FBB_WCK45	1	80DIFF	FBB_WCK45
8< 4>	OUT	FBB_WCK45*	1	80DIFF	FBB_WCK45
8< 4>	OUT	FBB_WCK67	1	80DIFF	FBB_WCK67
8< 4>	OUT	FBB_WCK67*	1	80DIFF	FBB_WCK67
6< 5< 4>	OUT	FBA_CMD<31..0>	1	45OHM	
6< 5< 4<	OUT	FBA_EDC<7..0>	1	45OHM	
6< 5< 4<	OUT	FBA_DBI<7..0>	1	45OHM	
6<> 5<> 4<>	BI	FBA_D<63..0>	1	45OHM	

Pages	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
7< 4>	OUT	FBB_CLK0	1	80DIFF	FBB_CLK0
7< 4>	OUT	FBB_CLK0*	1	80DIFF	FBB_CLK0
8< 4>	OUT	FBB_CLK1	1	80DIFF	FBB_CLK1
8< 4>	OUT	FBB_CLK1*	1	80DIFF	FBB_CLK1
5< 4>	OUT	FBA_WCK01	1	80DIFF	FBA_WCK01
5< 4>	OUT	FBA_WCK01*	1	80DIFF	FBA_WCK01
5< 4>	OUT	FBA_WCK23	1	80DIFF	FBA_WCK23
5< 4>	OUT	FBA_WCK23*	1	80DIFF	FBA_WCK23
6< 4>	OUT	FBA_WCK45	1	80DIFF	FBA_WCK45
6< 4>	OUT	FBA_WCK45*	1	80DIFF	FBA_WCK45
6< 4>	OUT	FBA_WCK67	1	80DIFF	FBA_WCK67
6< 4>	OUT	FBA_WCK67*	1	80DIFF	FBA_WCK67
8< 7< 4>	OUT	FBB_CMD<31..0>	1	45OHM	
8< 7< 4>	OUT	FBB_EDC<7..0>	1	45OHM	
8< 7< 4<	OUT	FBB_DBI<7..0>	1	45OHM	
8<> 7<> 4<>	BI	FBB_D<63..0>	1	45OHM	

Pages	Port	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
6< 5>	BI	FBA_VREFD	1.00V	0.02A	8MIL
6< 5>	BI	FBA_VREFC	1.00V	0.02A	8MIL
8< 7>	BI	FBB_VREFD	1.00V	0.02A	8MIL
8< 7>	BI	FBB_VREFC	1.00V	0.02A	8MIL

NET RULES for FrameBuffer C/D

Pages	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
10< 9>	OUT	FBC_CLK0	1	80DIFF	FBC_CLK0
10< 9>	OUT	FBC_CLK0*	1	80DIFF	FBC_CLK0
11< 9>	OUT	FBC_CLK1	1	80DIFF	FBC_CLK1
11< 9>	OUT	FBC_CLK1*	1	80DIFF	FBC_CLK1
10< 9>	OUT	FBC_WCK01	1	80DIFF	FBC_WCK01
10< 9>	OUT	FBC_WCK01*	1	80DIFF	FBC_WCK01
10< 9>	OUT	FBC_WCK23	1	80DIFF	FBC_WCK23
10< 9>	OUT	FBC_WCK23*	1	80DIFF	FBC_WCK23
11< 9>	OUT	FBC_WCK45	1	80DIFF	FBC_WCK45
11< 9>	OUT	FBC_WCK45*	1	80DIFF	FBC_WCK45
11< 9>	OUT	FBC_WCK67	1	80DIFF	FBC_WCK67
11< 9>	OUT	FBC_WCK67*	1	80DIFF	FBC_WCK67
11< 10< 9>	OUT	FBC_CMD<31..0>	1	45OHM	
11< 10< 9>	OUT	FBC_EDC<7..0>	1	45OHM	
11< 10< 9>	OUT	FBC_DBI<7..0>	1	45OHM	
10<> 9<> 11<>	BI	FBC_D<63..0>	1	45OHM	

Pages	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
12< 9>	OUT	FBD_CLK0	1	80DIFF	FBD_CLK0
12< 9>	OUT	FBD_CLK0*	1	80DIFF	FBD_CLK0
13< 9>	OUT	FBD_CLK1	1	80DIFF	FBD_CLK1
13< 9>	OUT	FBD_CLK1*	1	80DIFF	FBD_CLK1
12< 9>	OUT	FBD_WCK01	1	80DIFF	FBD_WCK01
12< 9>	OUT	FBD_WCK01*	1	80DIFF	FBD_WCK01
12< 9>	OUT	FBD_WCK23	1	80DIFF	FBD_WCK23
12< 9>	OUT	FBD_WCK23*	1	80DIFF	FBD_WCK23
13< 9>	OUT	FBD_WCK45	1	80DIFF	FBD_WCK45
13< 9>	OUT	FBD_WCK45*	1	80DIFF	FBD_WCK45
13< 9>	OUT	FBD_WCK67	1	80DIFF	FBD_WCK67
13< 9>	OUT	FBD_WCK67*	1	80DIFF	FBD_WCK67
13< 12< 9>	OUT	FBD_CMD<31..0>	1	45OHM	
13< 12< 9>	OUT	FBD_EDC<7..0>	1	45OHM	
13< 12< 9<	OUT	FBD_DBI<7..0>	1	45OHM	
12<> 9<> 13<>	BI	FBD_D<63..0>	1	45OHM	

Pages	Port	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
11< 10>	BI	FBC_VREFD	1.00V	0.02A	8MIL
11< 10>	BI	FBC_VREFC	1.00V	0.02A	8MIL
13< 12>	BI	FBD_VREFD	1.00V	0.02A	8MIL
13< 12>	BI	FBD_VREFC	1.00V	0.02A	8MIL

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	FB Net Properties

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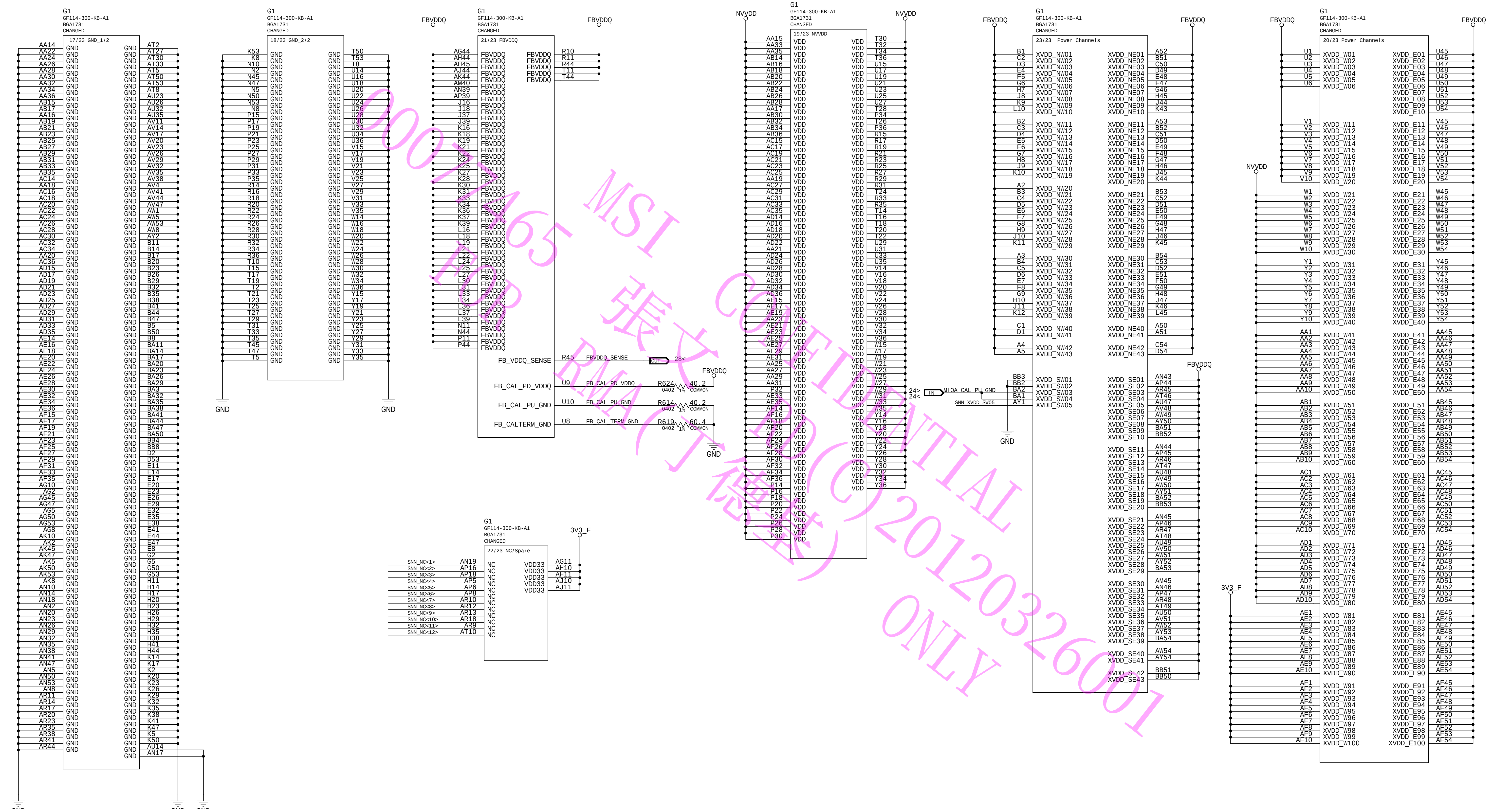
Page15: GPU PWR and GND

** Power channels are configurable.
XVDD_* pins are not connected on the substrate.
Therefore, XVDD_* pins can be assigned as needed.



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PAGE DETAIL	GPU PWR and GND

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Page16: GPU Decoupling

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU Decoupling

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Page17: Blank

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	Blank

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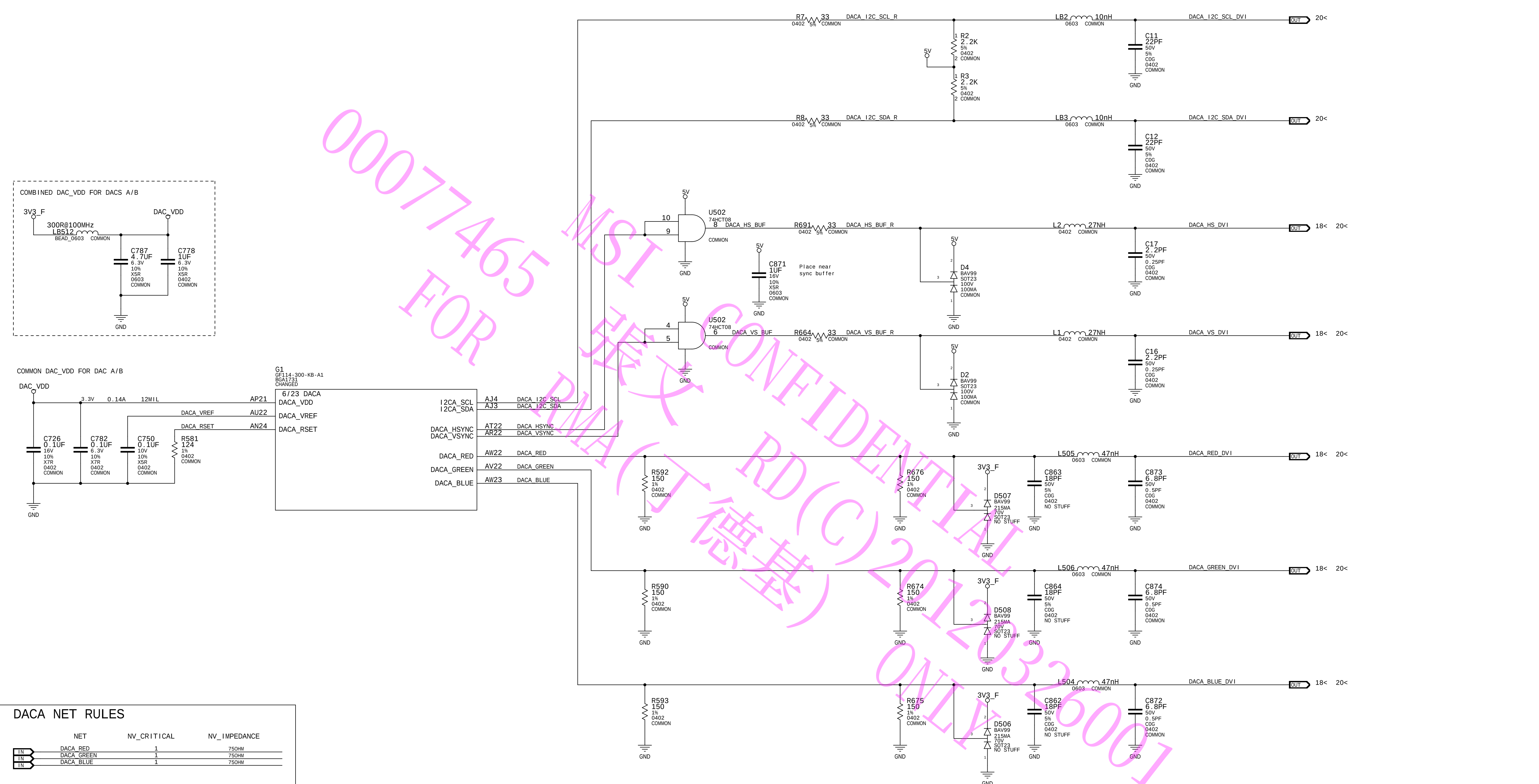
Page18: DACA (South)



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DACA NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE
IN	DACA_RED	1	75OHM
IN	DACA_GREEN	1	75OHM
IN	DACA_BLUE	1	75OHM
20< 18> IN	DACA_RED_DVI	1	75OHM
20< 18> IN	DACA_GREEN_DVI	1	75OHM
20< 18> IN	DACA_BLUE_DVI	1	75OHM
IN	DACA_HSYNC	2	50OHM
IN	DACA_VSYNC	2	50OHM
IN	DACA_HS_BUF	2	50OHM
IN	DACA_VS_BUF	2	50OHM
IN	DACA_HS_BUF_R	2	50OHM
IN	DACA_VS_BUF_R	2	50OHM
20< 18> IN	DACA_HS_DVI	2	50OHM
20< 18> IN	DACA_VS_DVI	2	50OHM

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DACA (South)

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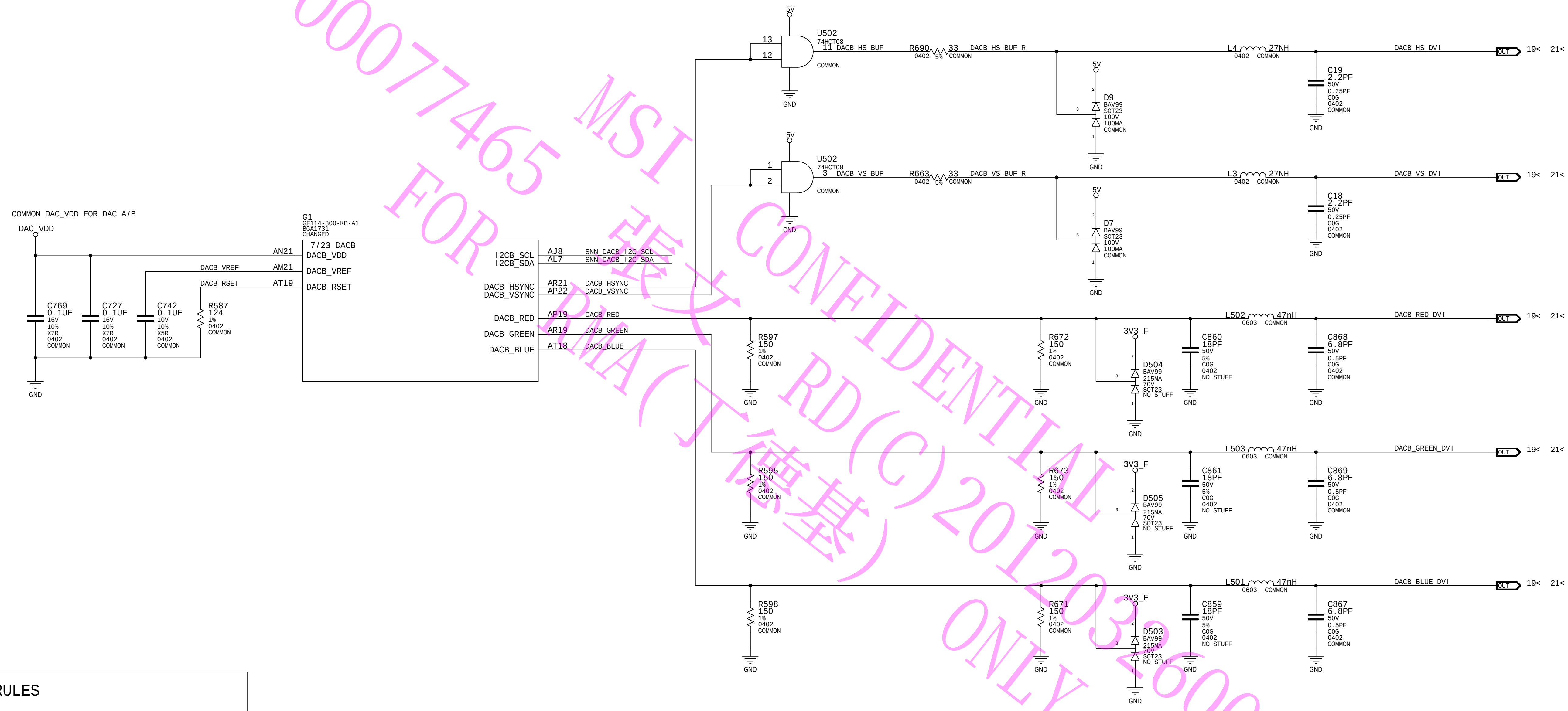
Page19: DACB (Mid)



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DACB NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE
IN	DACB_RED	1	75OHM
IN	DACB_GREEN	1	75OHM
IN	DACB_BLUE	1	75OHM
21< 19> IN	DACB_RED_DVI	1	75OHM
21< 19> IN	DACB_GREEN_DVI	1	75OHM
21< 19> IN	DACB_BLUE_DVI	1	75OHM
IN	DACB_HSYNC	2	50OHM
IN	DACB_VSYNC	2	50OHM
IN	DACB_HS_BUF	2	50OHM
IN	DACB_VS_BUF	2	50OHM
IN	DACB_HS_BUF_R	2	50OHM
IN	DACB_VS_BUF_R	2	50OHM
21< 19> IN	DACB_HS_DVI	2	50OHM
21< 19> IN	DACB_VS_DVI	2	50OHM

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DACB (Mid)

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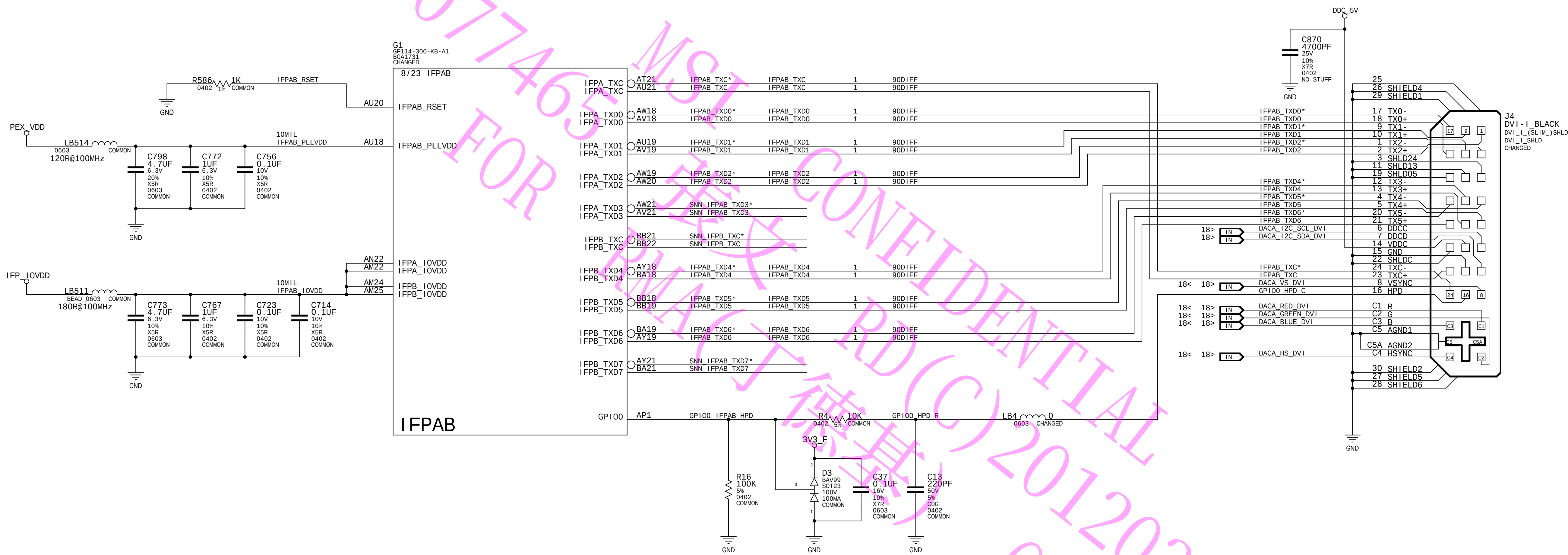
Page20: IFPAB DVI-I-DL (South)



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PAGE DETAIL	IFPAB DVI-DL (South)

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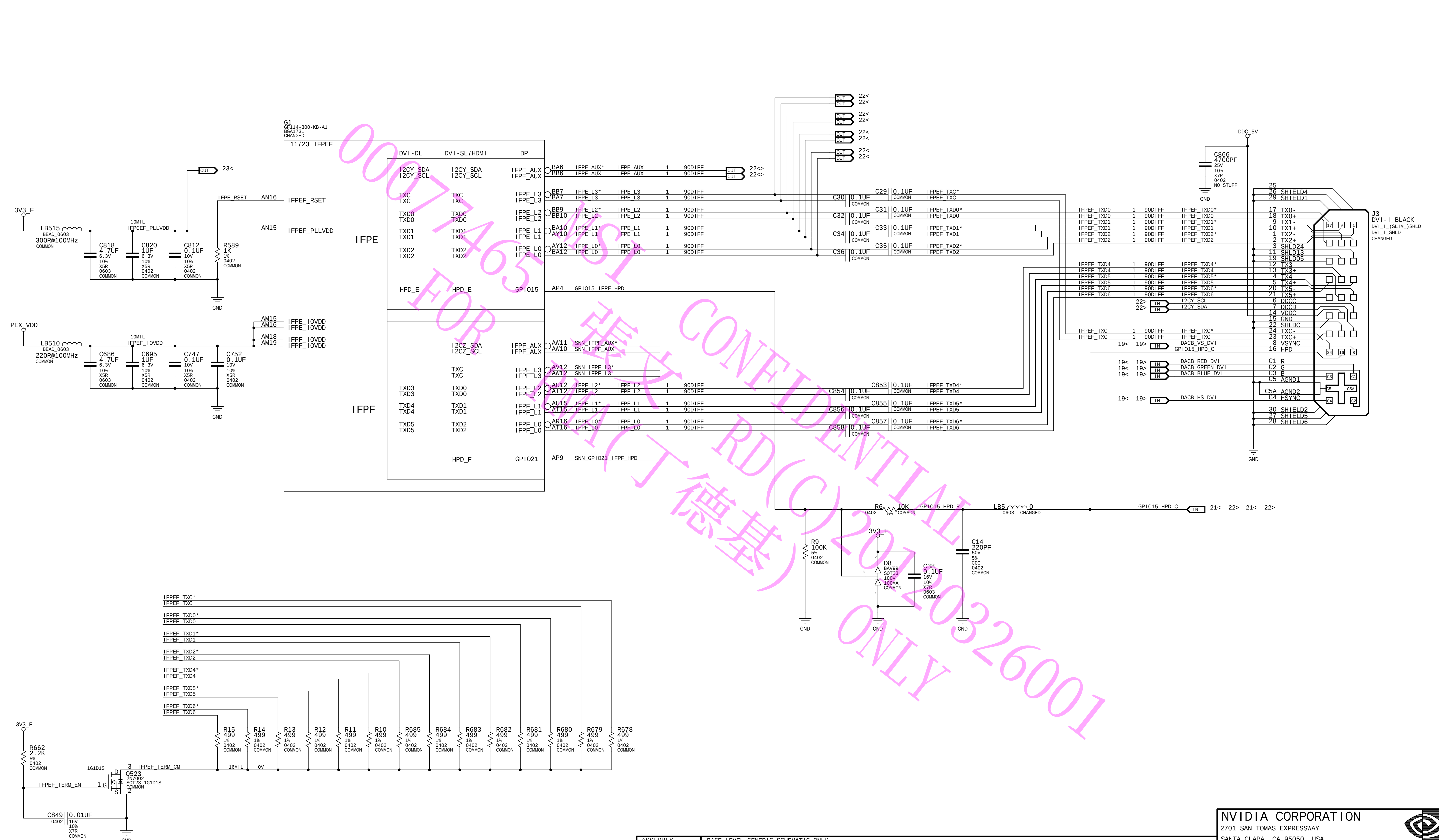
Page21: IFPEF DVI-I-DL (Mid)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPEF DVI-DL (Mid)

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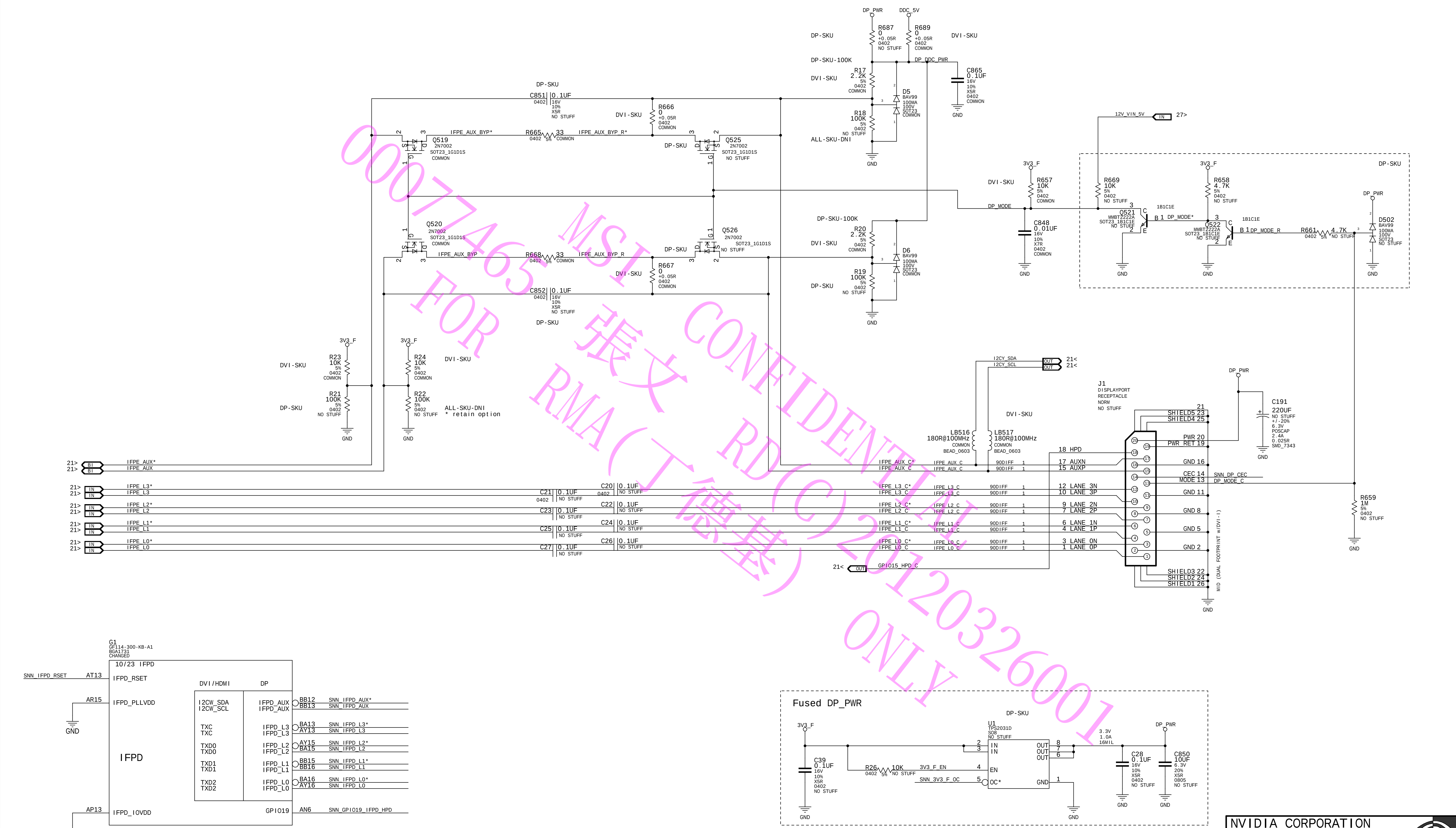
Page22: IFPEF DP (Mid)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPEF DP (Mid)

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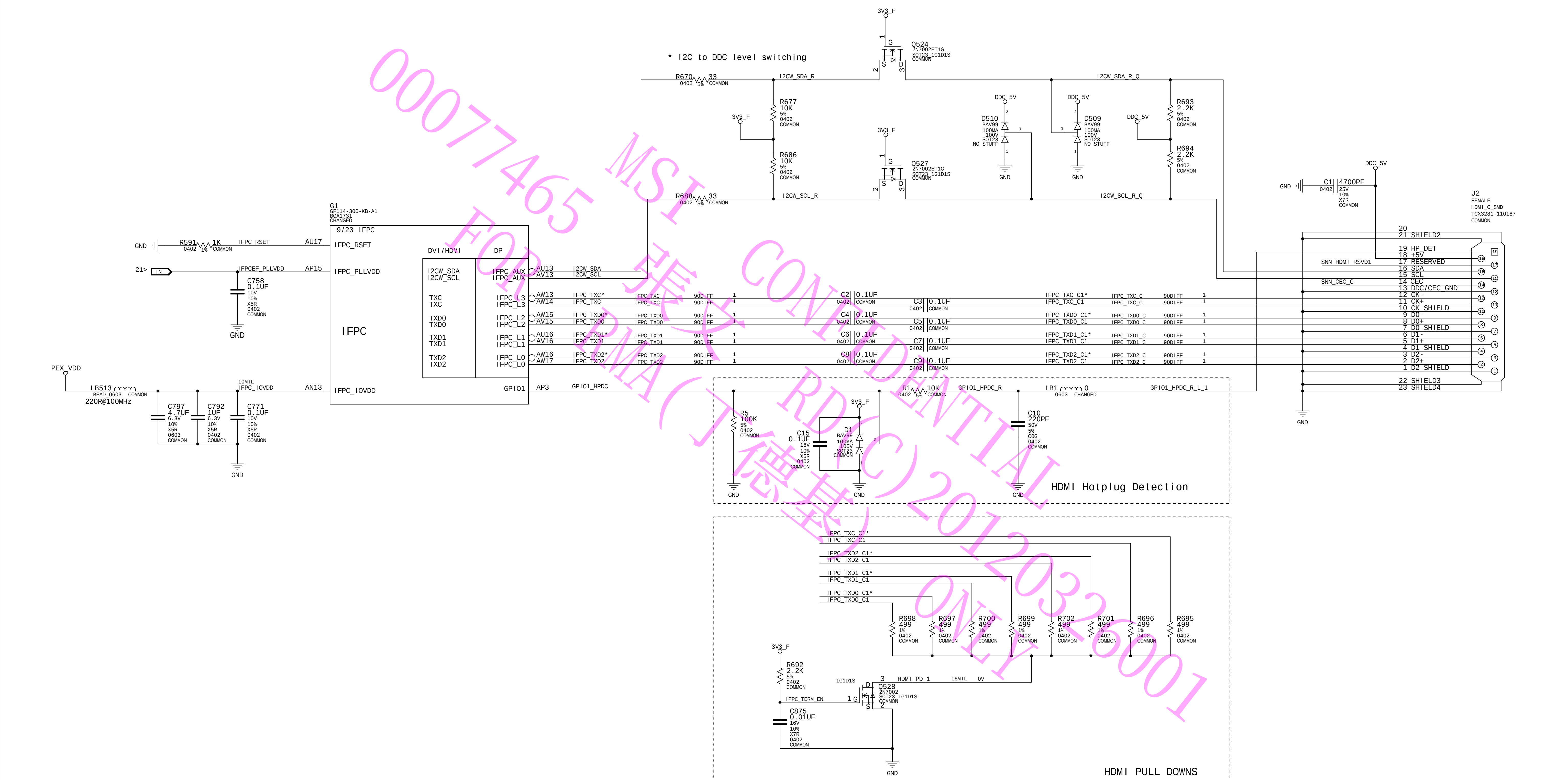
Page23: IFPC mHDMI (North)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPC mHDMI (North)

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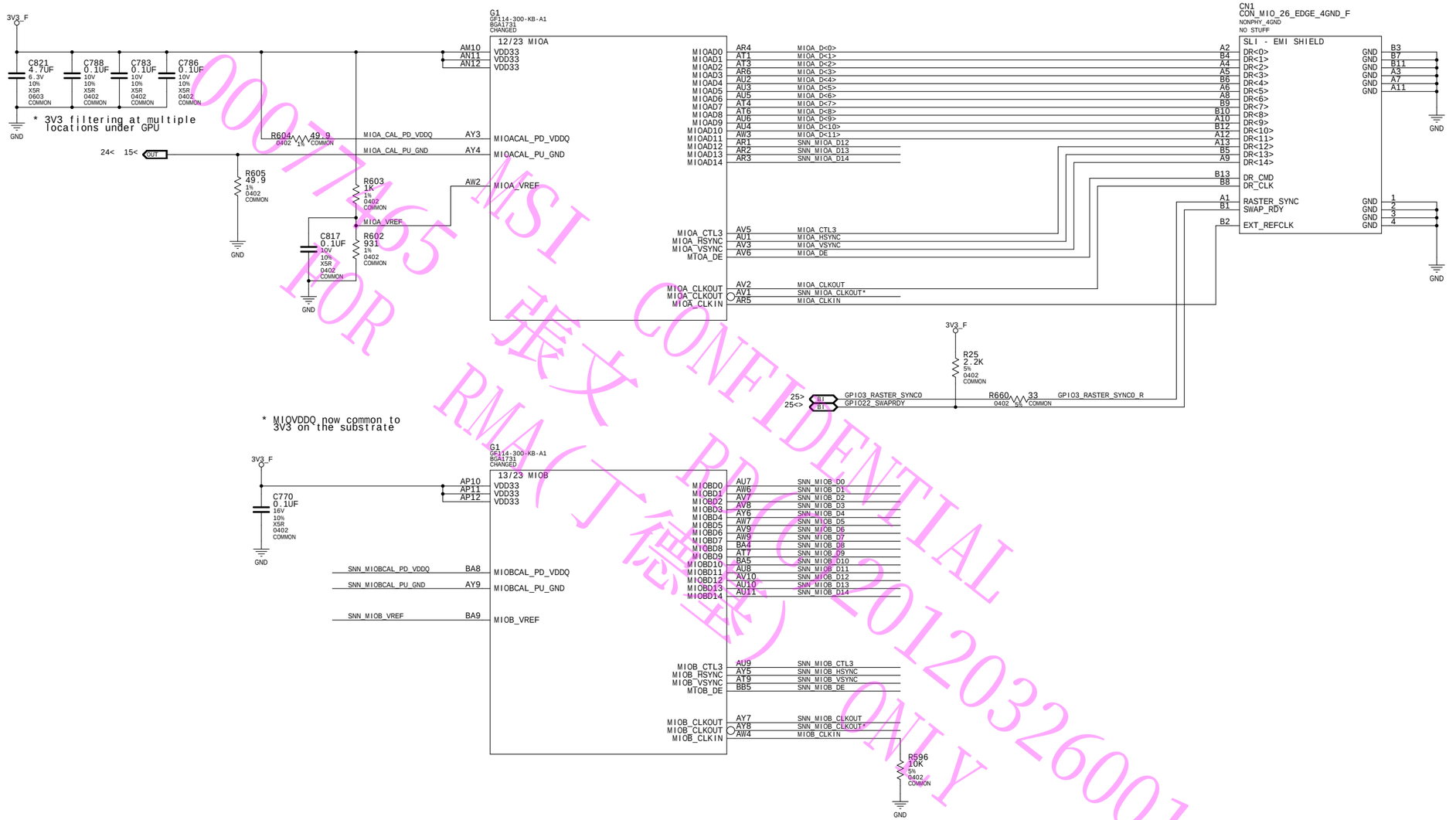
Page24: Multi-use IO (MIO) Interface



MIO NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	MIOA_D<11..0>	1	50OHM	
IN	MIOA_HSYNC	1	50OHM	
IN	MIOA_VSYNC	1	50OHM	
IN	MIOA_CTL3	1	50OHM	
IN	MIOA_DE	1	50OHM	
IN	MIOA_CLKOUT	1	50OHM	
IN	MIOA_CLKIN	1	50OHM	

	NET	VOLTAGE	MIN_WIDTH
IN	MIOA_VREF	1.65V	6MIL
IN	MIOA_CAL_PD_VDDQ	3.3V	6MIL
24> 15< IN	MIOA_CAL_PU_GND	0.0V	6MIL

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	Multi-use IO (MIO) Interface

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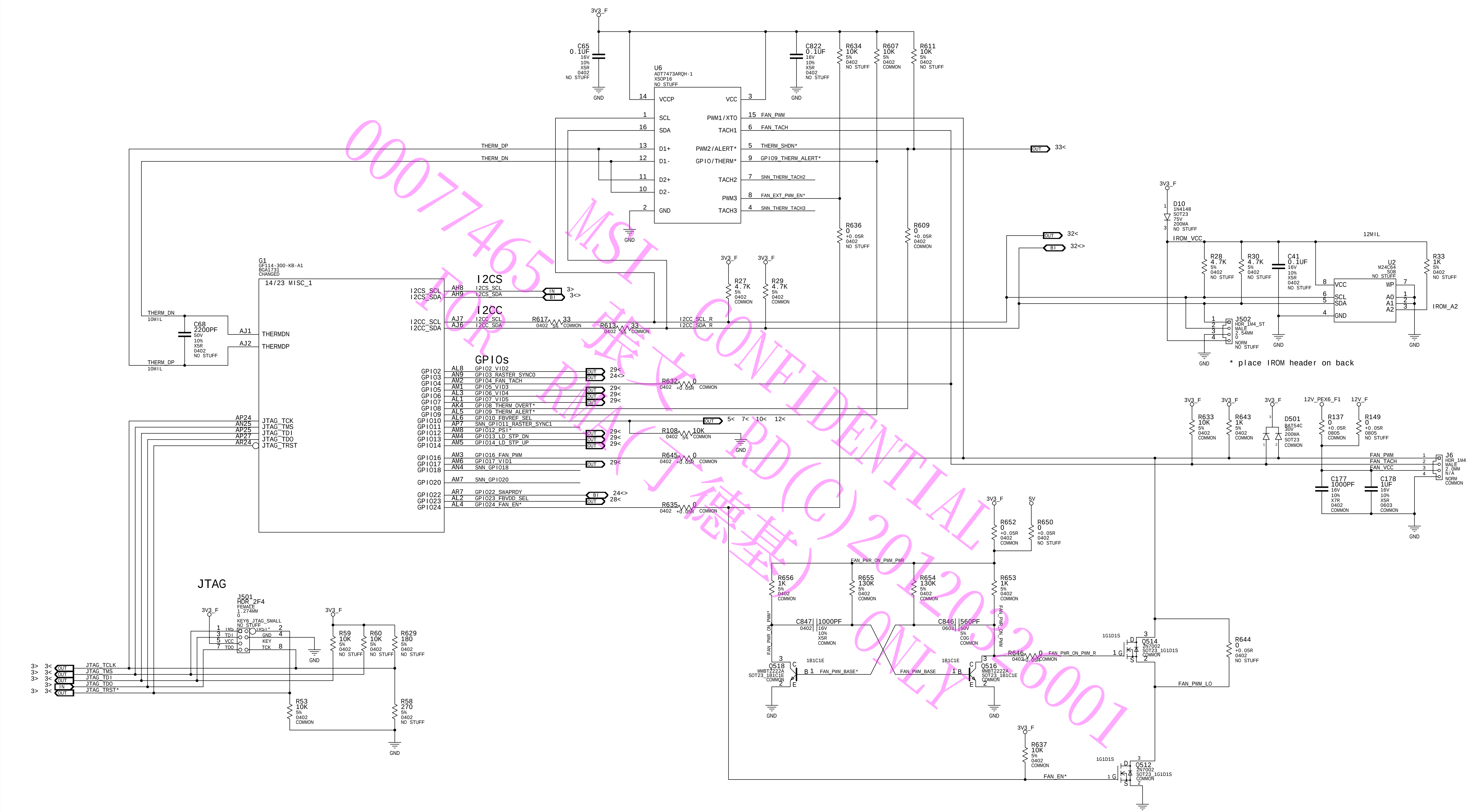
Page25: Misc: Fan, Thermal, JTAG, GPIO



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	Misc: Fan, Thermal, JTAG, GPIO

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Page26: Misc: ROM, HDCP, XTAL, Straps

STRAP0	USER_BIT [3..0]	0000:=> 5K PD
STRAP1	3GIO_PADCFG_LUT_ADR	0000 :=>5K PD 0000 Desktop
STRAP2	PCI_DEVID [3:0]	0001 For 0x1201 (SKU0050) :=> 10K PD 0101 For 0x1205 (SKU0060 & SKU0061) :=> 30K PD 0011 For 0x1203 (SKU0070) :=> 20K PD

ROM_SI	RAMCFG[0]		32Mx32 256 bit Samsung for SKU0050 & SKU0070 0011: PD 20K 32Mx32 256 bit Hynix for SKU0050 & SKU0070 0010: PD 15K 32Mx32 192 bit Samsung for SKU0061 1011: PU 20K 32Mx32 192 bit Hynix for SKU0061 1011: PU 15K 64Mx32 192 bit Samsung for SKU0060 1011: PU 20K 64Mx32 192 bit Hynix for SKU0060 1010: PU 15K
	RAMCFG[1]		
	RAMCFG[2]		
	RAMCFG[3]		
ROM_SO	VGA_DEVICE	1	10k PD
	SMB_ALT_ADDR	0	
	FB[0]_BAR_SIZE	0	
	XCLK_417	0	
ROM_SCLK	PEX_PLL_EN_TERM100	1 ENABLED	45K PD
	SLOT_CLK_CFG	1 ENABLE	
	SUB_VENDOR	1 Dedicated BIOS	
	PCI_DEVID_EXT	0 0xC	

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

NON MIXED DENSITY STRAP DEFINITION

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit	Elpida
0010	32Mx32 256-bit	Hynix
0011	32Mx32 256-bit	Samsung
0100	Reserved	
0101	64Mx32 256-bit	Elpida
0110	64Mx32 256-bit	Hynix
0111	64Mx32 256-bit	Samsung
1000	Reserved	
1001	32Mx32 192-bit	Elpida
1010	32Mx32 192-bit	Hynix
1011	32Mx32 192-bit	Samsung
1100	Reserved	
1101	64Mx32 192-bit	Elpida
1110	64Mx32 192-bit	Hynix
1111	64Mx32 192-bit	Samsung

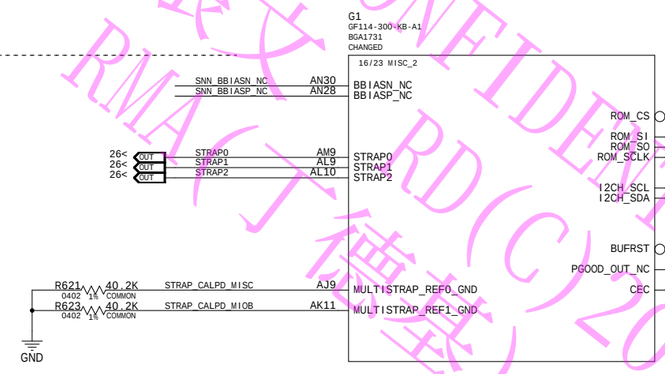
MIXED DENSITY STRAP DEFINITION

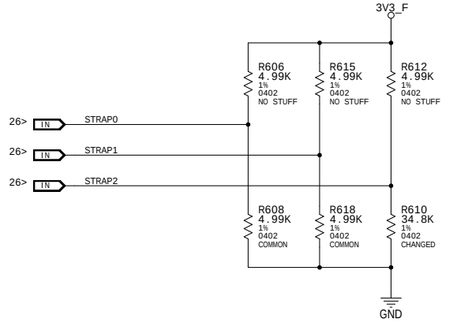
MIXED DENSITY = PARTITION A 64Mx32
PARTITION B NO STUFF
PARTITION C 32Mx32
PARTITION D 32Mx32

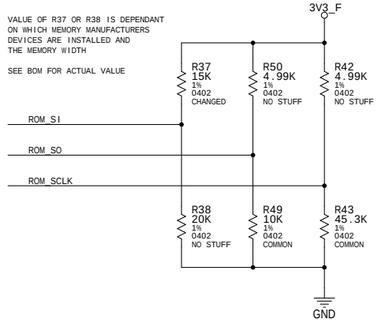
CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	64Mx32/32Mx32 256-bit	Elpida
0010	64Mx32/32Mx32 256-bit	Hynix
0011	64Mx32/32Mx32 256-bit	Samsung
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	
1000	Reserved	
1001	64Mx32/32Mx32 192-bit	Elpida
1010	64Mx32/32Mx32 192-bit	Hynix
1011	64Mx32/32Mx32 192-bit	Samsung
1100	Reserved	
1101	Reserved	
1110	Reserved	
1111	Reserved	

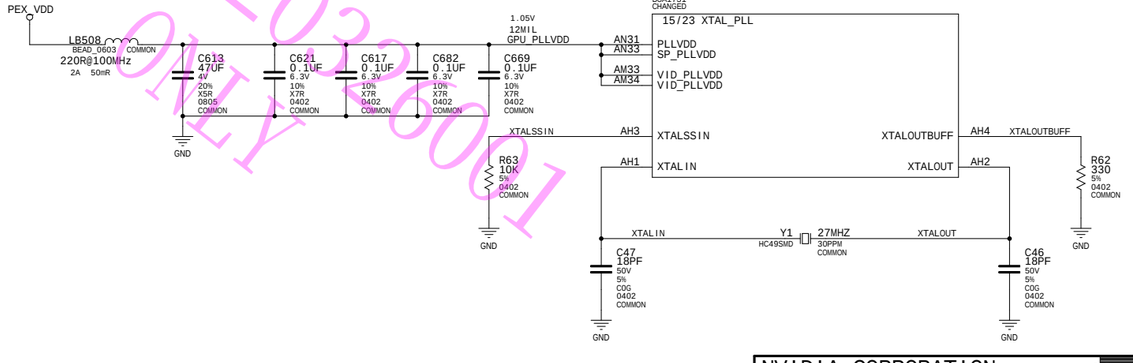
MISC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE
XTALSSIN	1	50OHM
XTALIN	1	50OHM
XTALOUT	1	50OHM









ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	Misc: ROM, HDCP, XTAL, Straps

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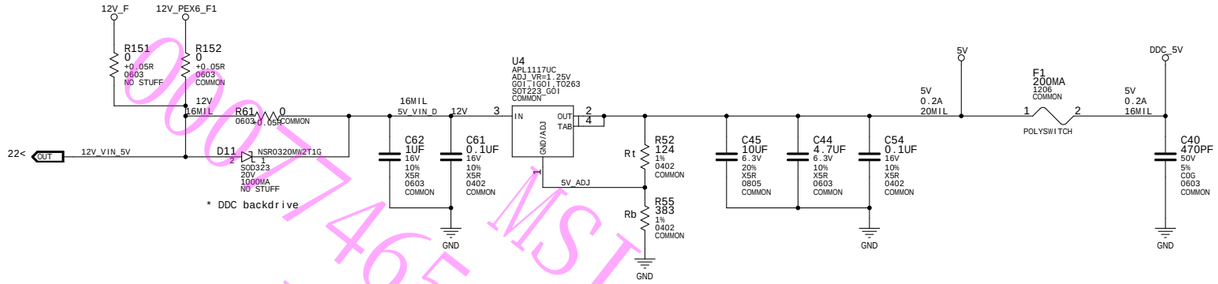
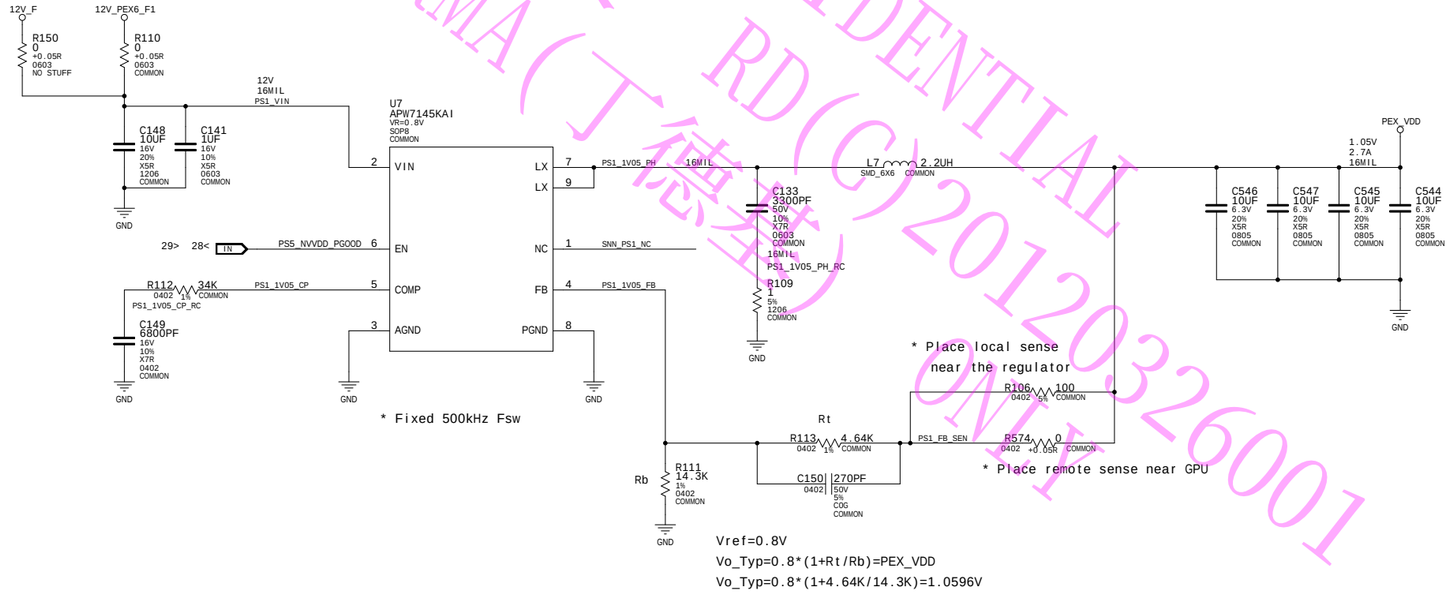
Page27: PS: 5V, PEX_VDD



Vref=1.256V
Vo_Typ=1.256*(1+383/124)+60uA*383=5.16V

Input ripple (Irms) = ~0.9A @ 2.7A



Vref=0.8V
Vo_Typ=0.8*(1+Rt/Rb)=PEX_VDD
Vo_Typ=0.8*(1+4.64K/14.3K)=1.0596V

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PAGE DETAIL	PS: 5V, PEX_VDD

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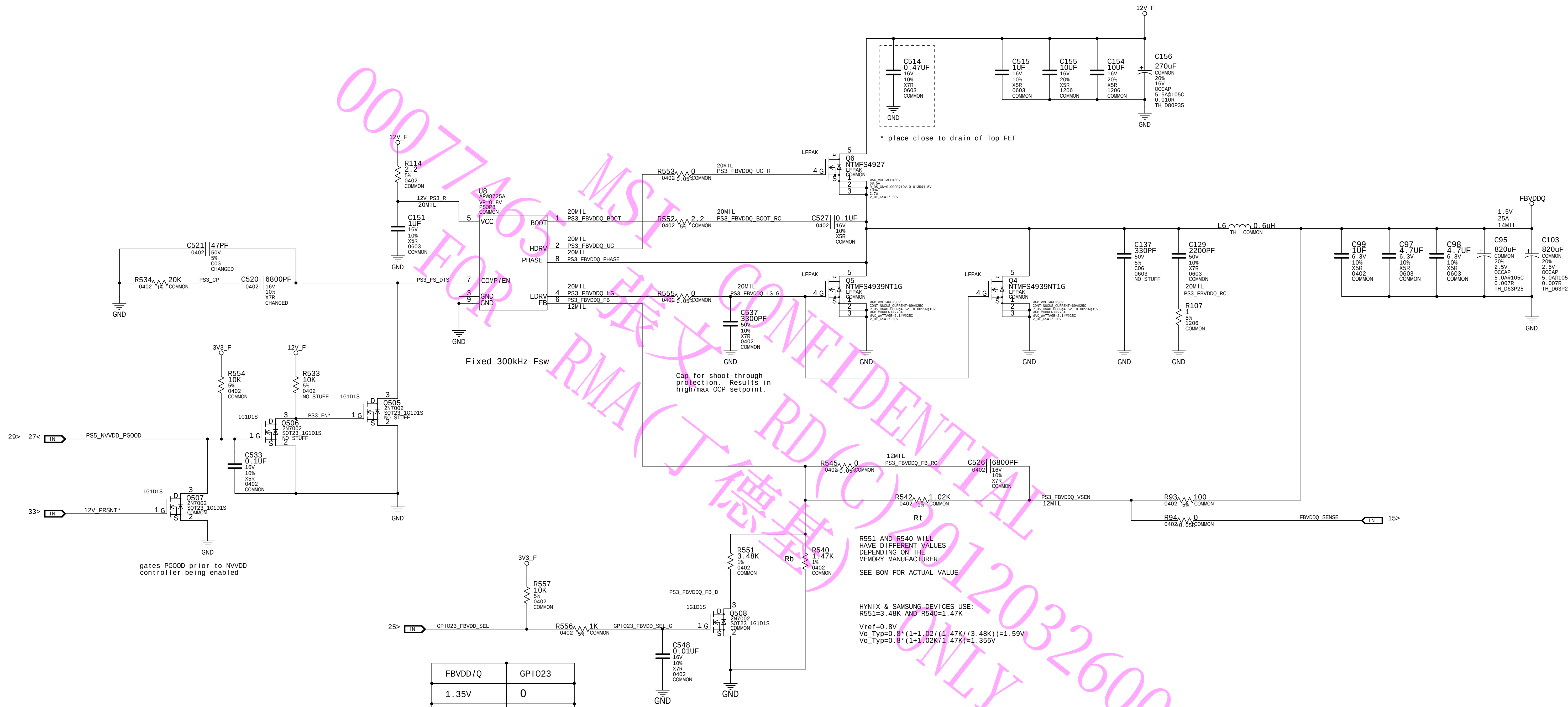
Page28: PS: FBVDD/Q



FBVDD/Q	GPIO23
1.35V	0
1.5V	1

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PAGE DETAIL	PS: FBVDD/Q

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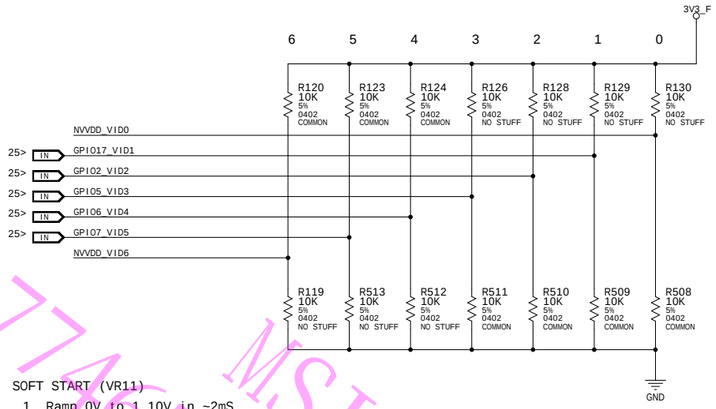
Page29: PS: NVVDD Controller

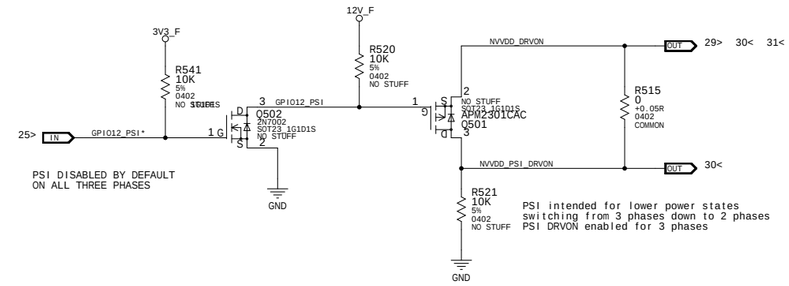
VID Table

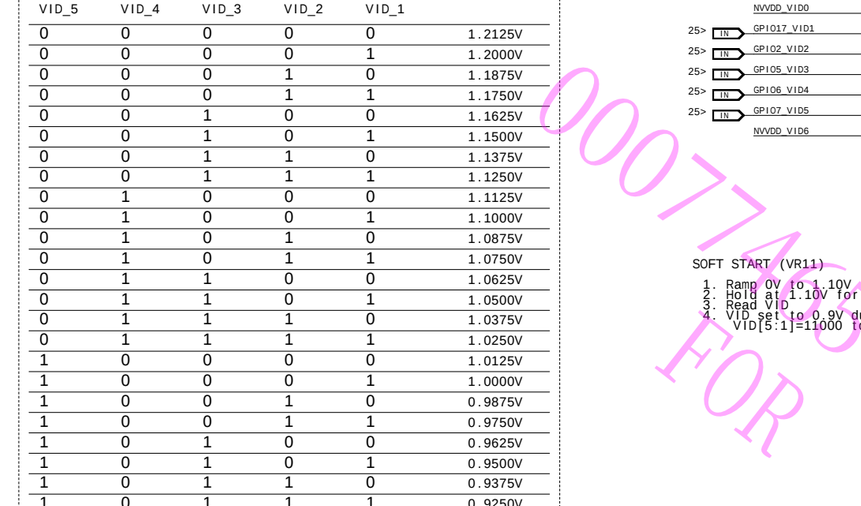
GPIO7	GPIO6	GPIO5	GPIO2	GPIO17	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V



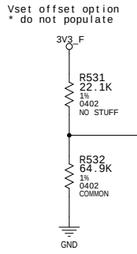
SOFT START (VR11)

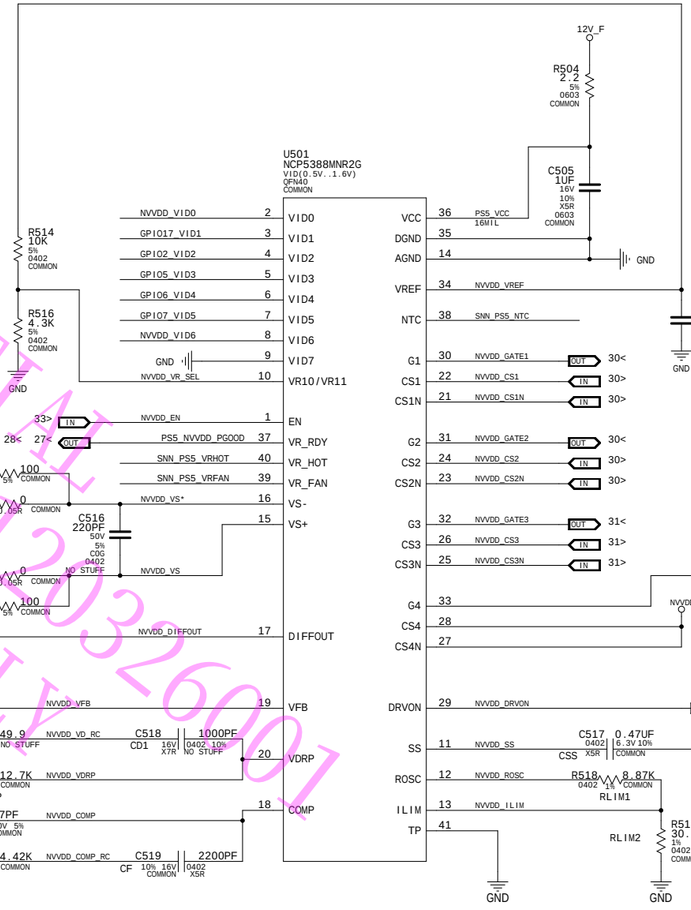
1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPIO_tri-state
   VID[5:1]=11000 to set 0.9125V





THERM LOAD STEP OPTION
* minimize stubs on NVVDD_VS





Updated compensation 07/14
RFB1 to 511 ohm
CFB1 to 2200 pF
RF to 4.42K ohm
CF to 2200 pF
CH to 47 pF

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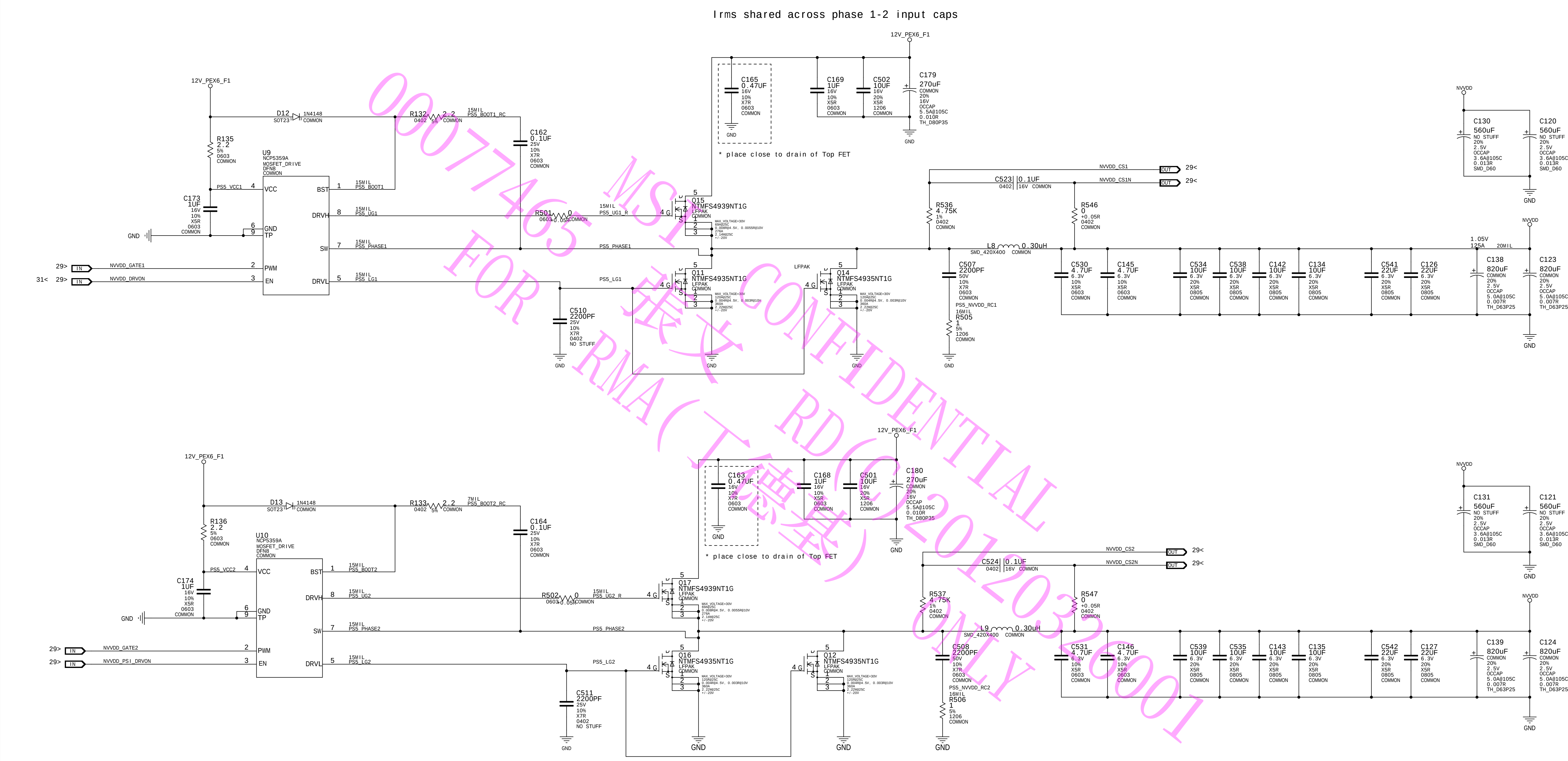
Page30: PS: NVVDD Phase 1-2



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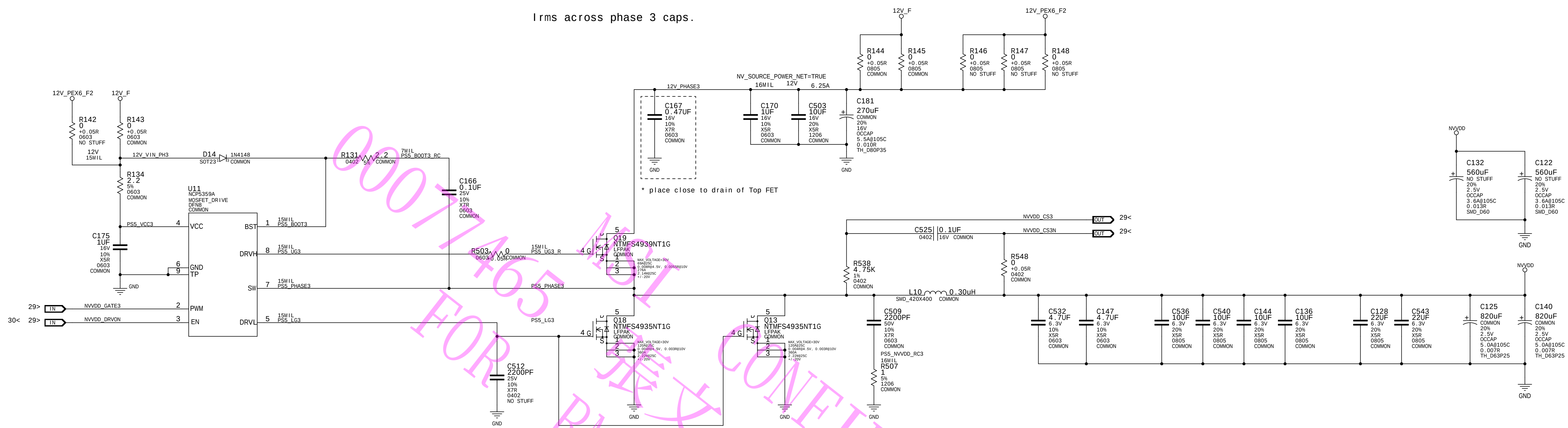
Page31: PS: NVVDD Phase 3



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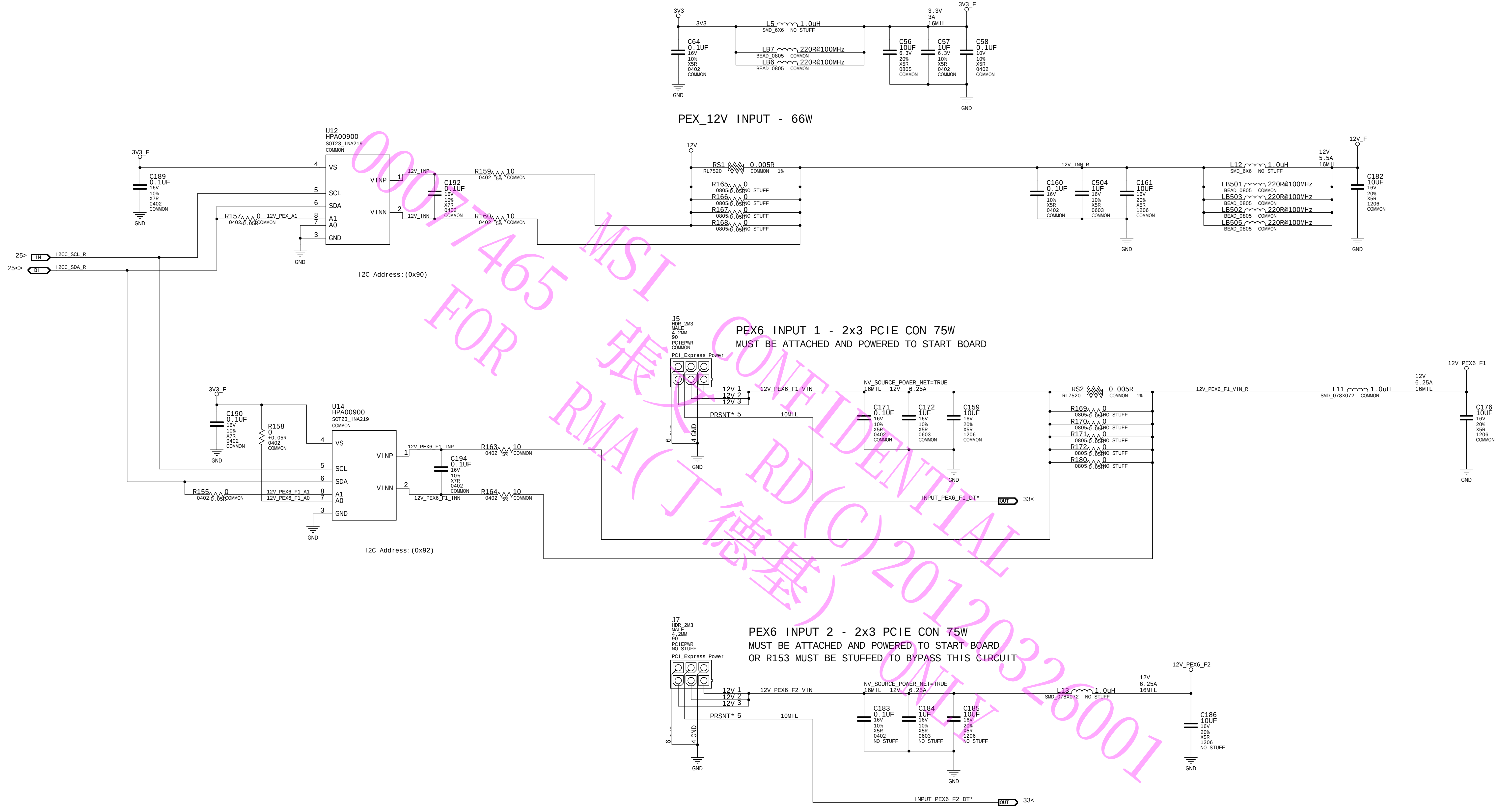
Page32: PS: Inputs, Shutdown



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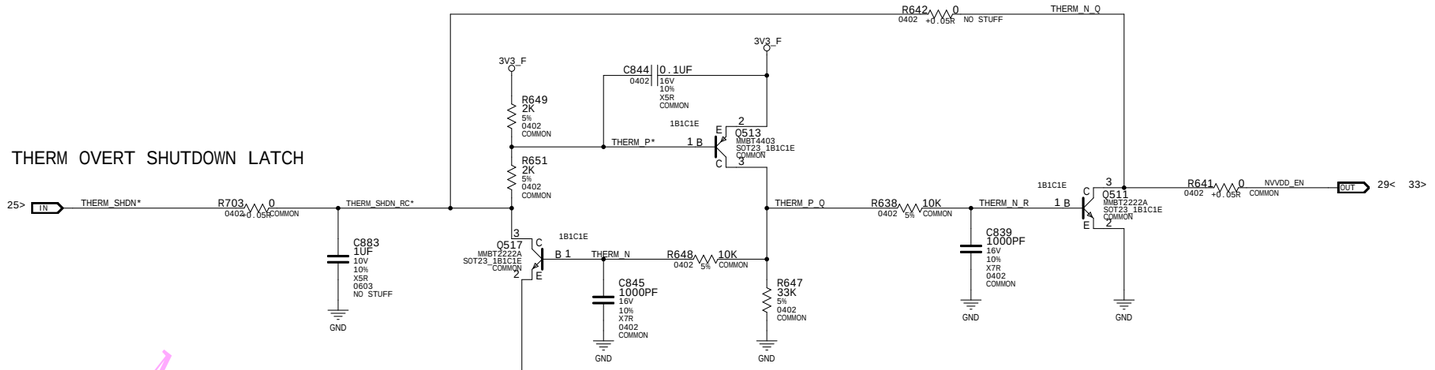
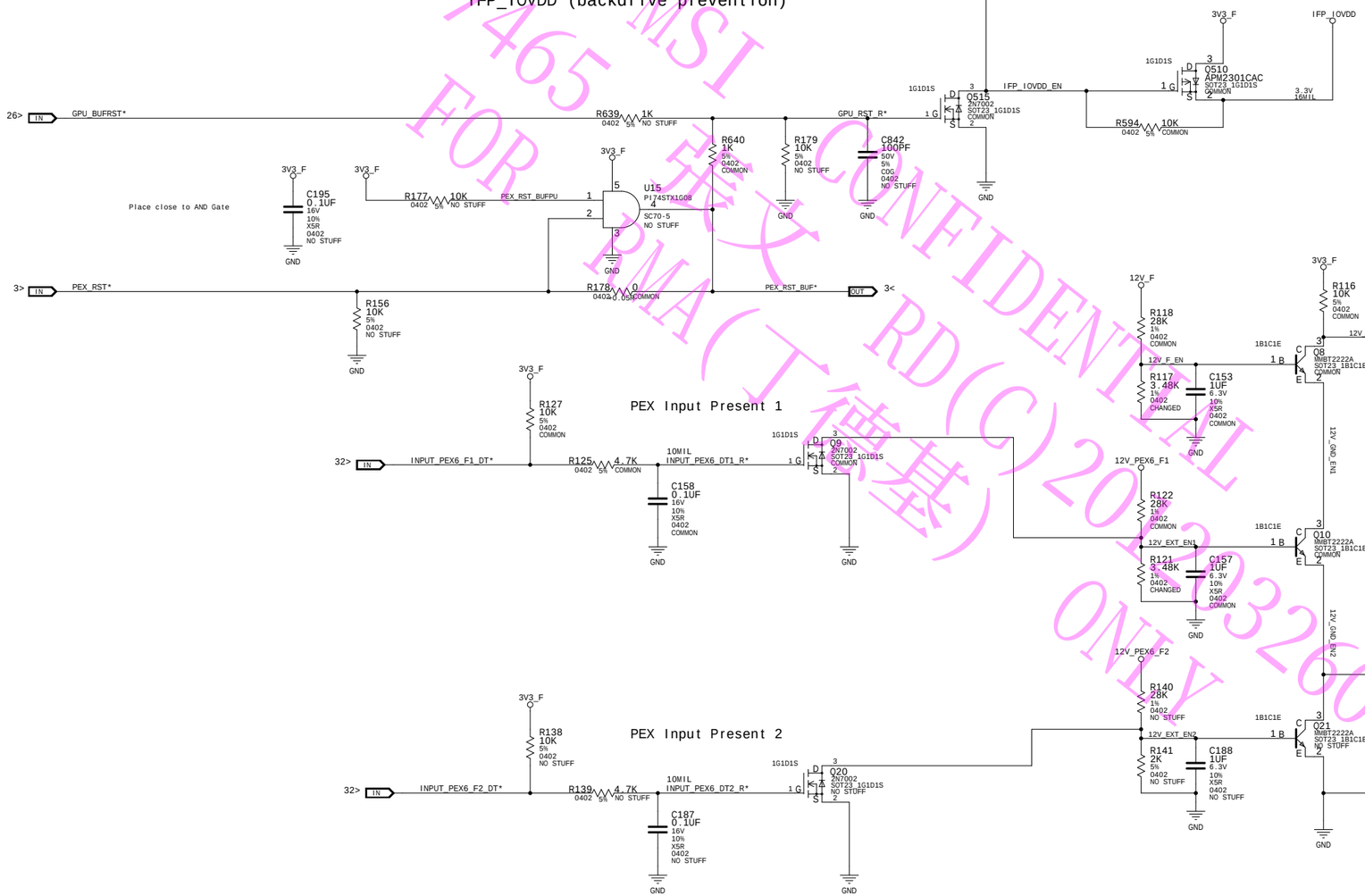
Page33: PS: IFP, Shutdown

THERM OVERT SHUTDOWN LATCH



IFP_IOVDD (backdrive prevention)



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Page34: Mechanical: Bracket/Thermal Solution

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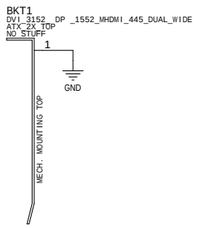
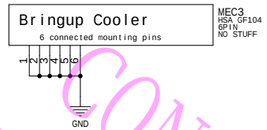
Brackets:

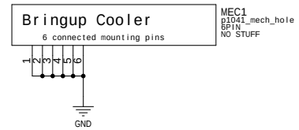


Cooler/GPU Stiffener

* when available



P1041 MOUNTING HOLE LOCATIONS



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