NV28M-P138, DAC, TMDS, LVDS, TVout, 32/64MB 4MX32 BGA DDR, AGP4X, Dell Mobile

X00
1. Schematics taken from E153-A00.

X17
1. Use RUNPWRGD for all PS enabling.

A01:

X40
1. Corrected serial ROM hookup.

A02:

X42
1. Corrected I2C2 hookup at U9 (CH7009).
2. Changed R254 to 1.5K 1%. This raises NVVDD to 1.25V.
3. Connect GPIO1 to 90C387 PD, and disconnect SUS_STAT- from motherboard.
4. Change Q2 to FDS6982.

X44
5. Change R287 to 2.67K and R254 to 1.1K when NVVDDSW stuff option is employed, with R254 = 1.5K when no NVVDDSW is used (NOSW stuff option).
6. Removed TP606 to allow better guard trace on thermal sensor D+ and D- lines.
7. Connected CH_GPIO0 to NSM_DUAL to select single or dual link panels.

A03:

X00

1. Add r989, r990, r991, r992 to pull up I2C bus.

2. Change c82 and c84 into small package to fit into new mechanical requirement.

3. Change r44 from pull-up to pull-up to ground.

4. Chang c60 and c61 to 47pF fot TVout issue.

X01

1. Change r287 to 4.02k; r254 to 1.21k.

A04:

X00

1. Change Mem vendor strapping option

X01

1. In P.13, rework to prevent LCDVCC backdrive. Connect L12.2 directly to C32.1 instead of 3.3NSM.

2. In P.14, rework to prevent LCDVCC glich. Use resistive load n-fet as an inverter driven by 3VRUN instead of 5VRUN.

3. Change CH7009 to CH7009B and connect U9.9 (HPDET) to J10.36 (DVI_DET)

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1.1 TOP PAGE

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602-10138-0000-004

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2.0 NV DECOUPLING

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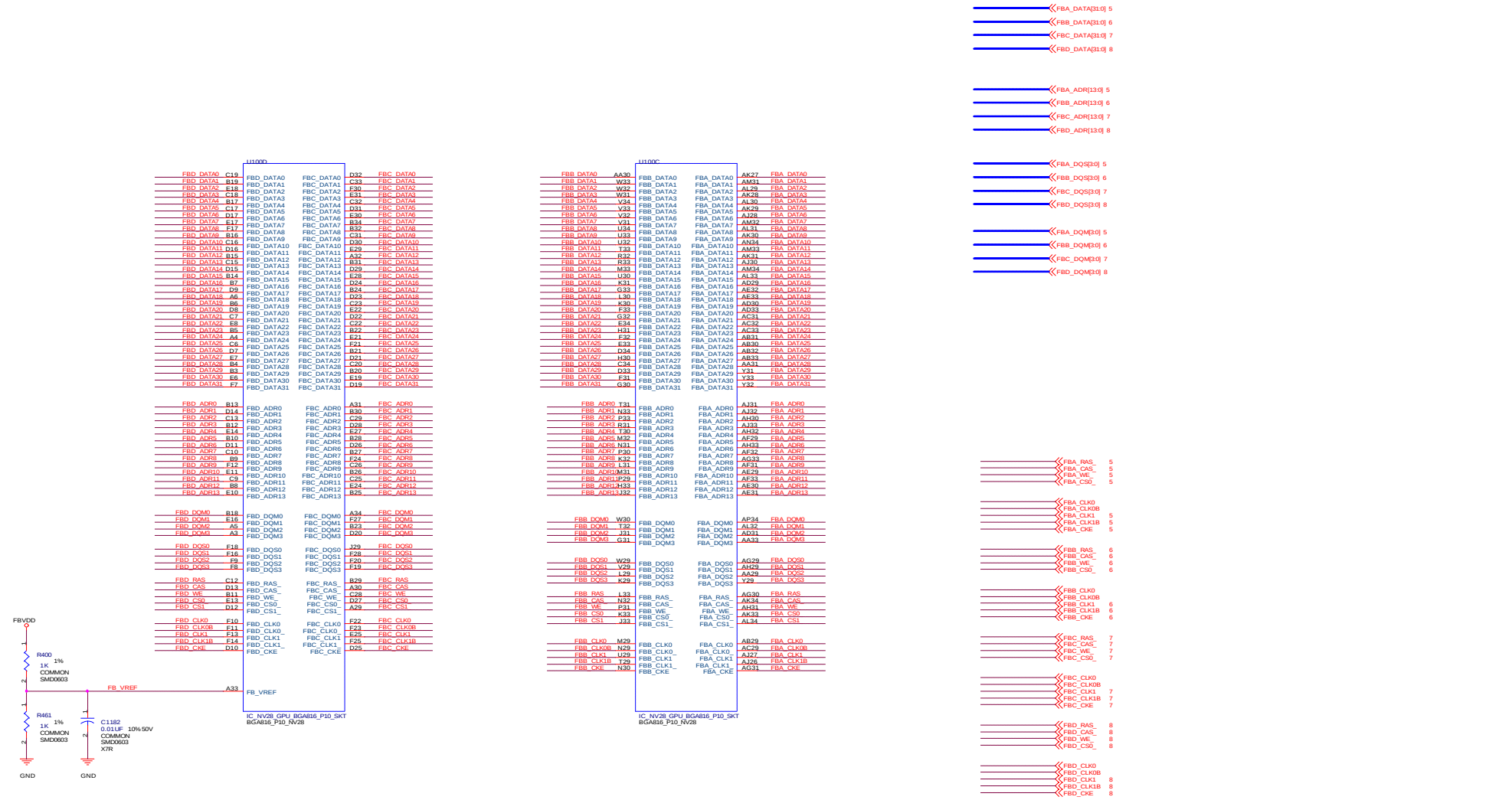

2.1 NV FBA/B/C/D

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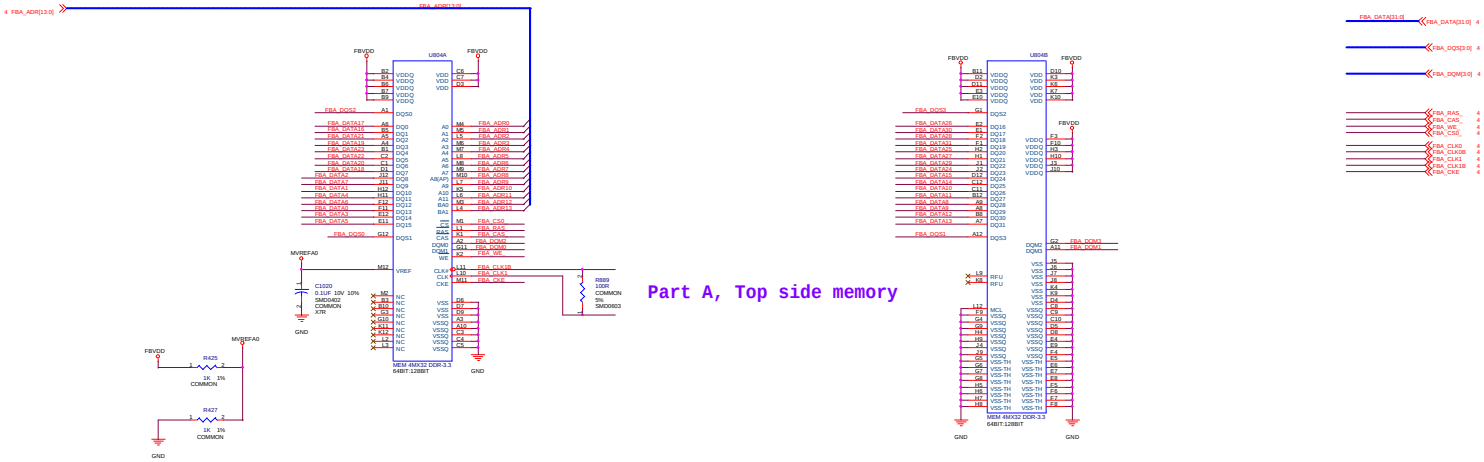

2.2 FBA DDR 4MX32 SDRAM

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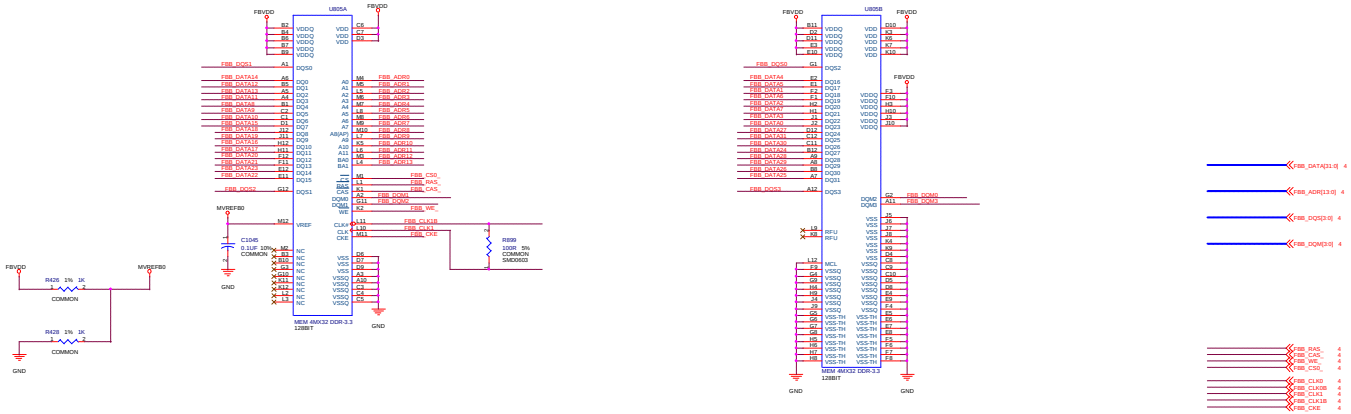

2.3 FBB DDR 4MX32 SDRAM

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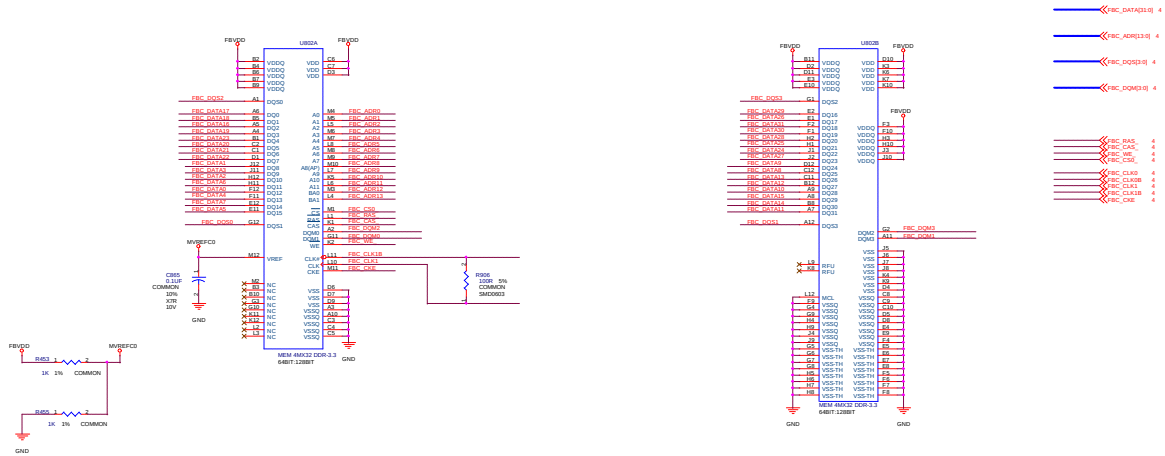

2.4 FBC DDR 4MX32 SDRAM

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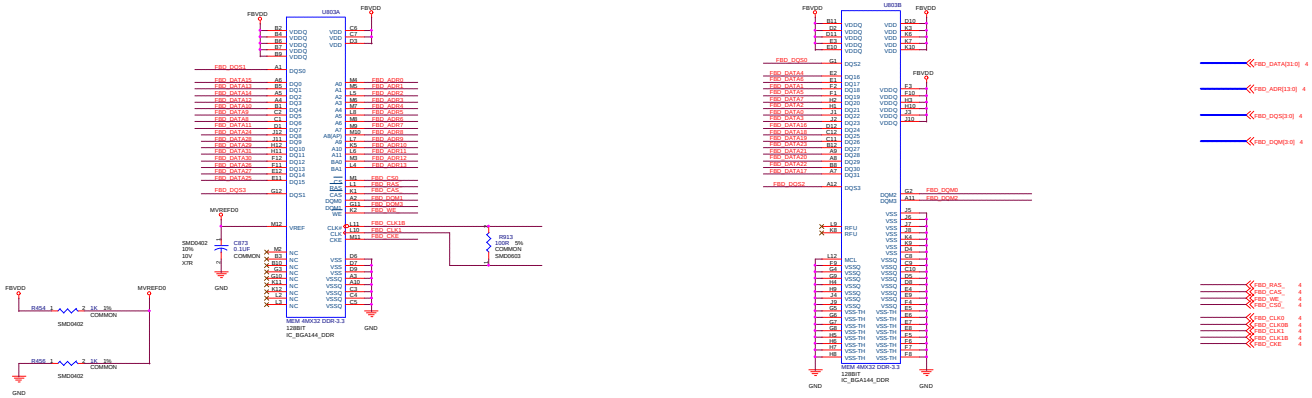

2.5 FBD DDR 4MX32 SDRAM

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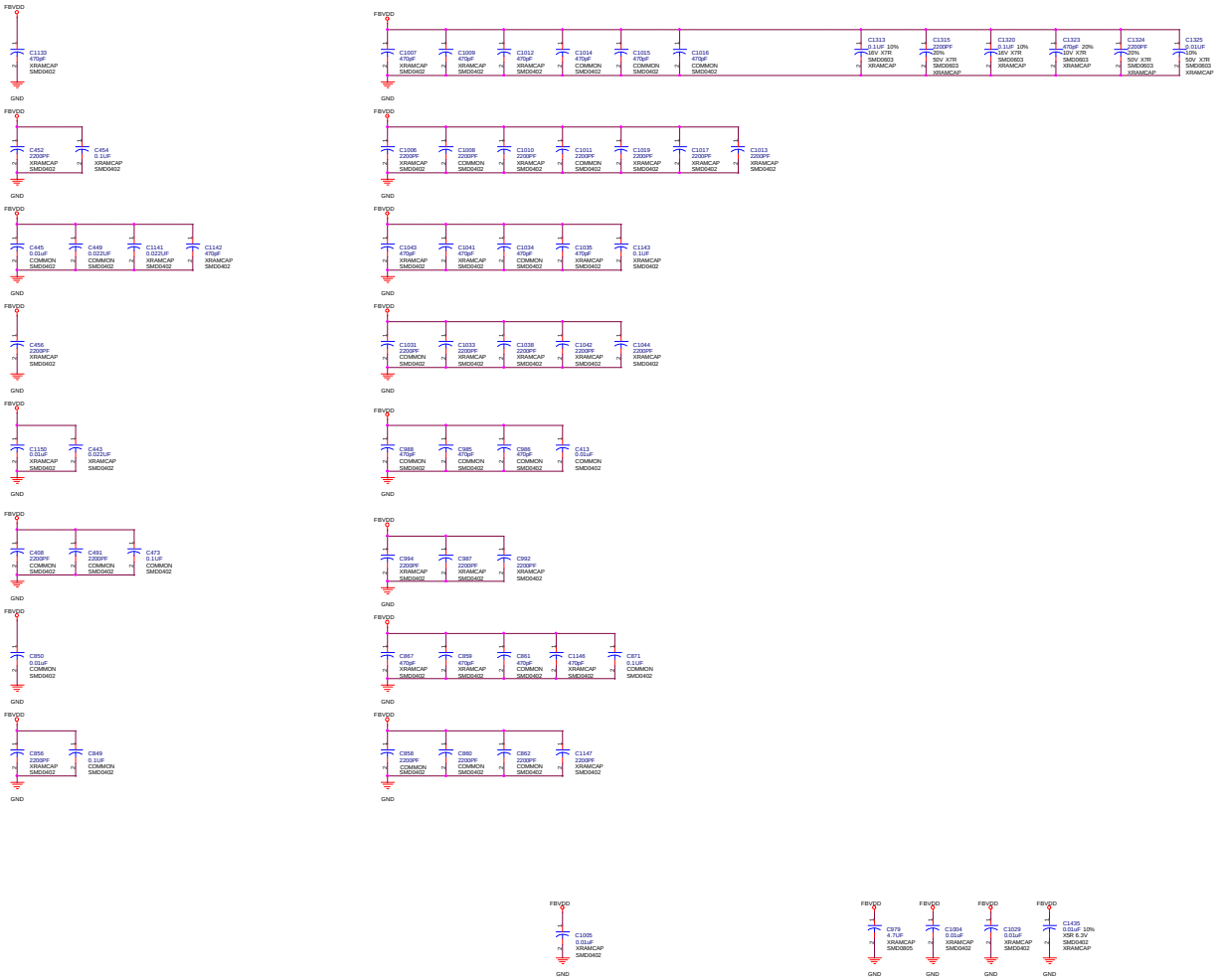

2.6 BGA MEMORY DECOUPLING

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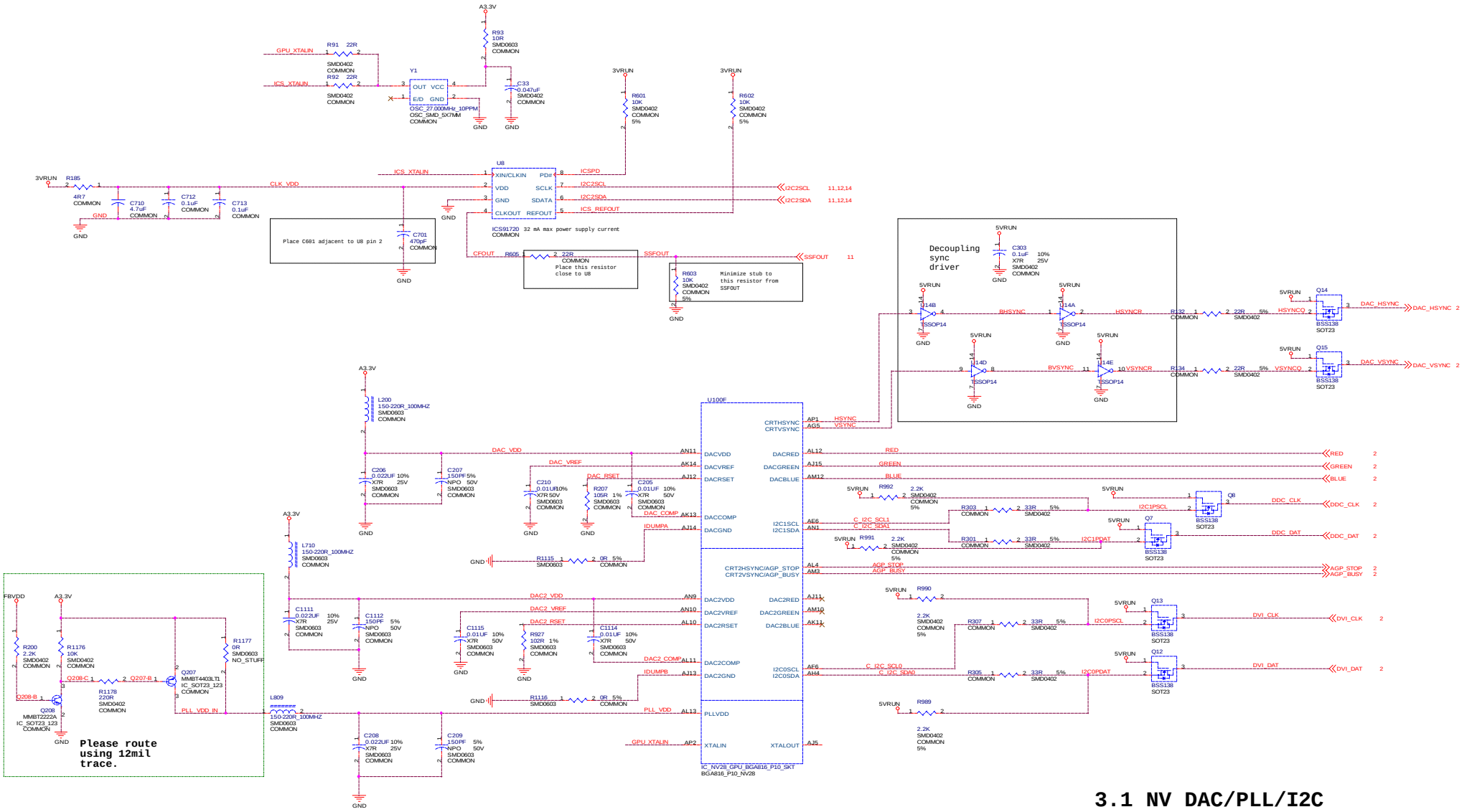

3.1 NV DAC/PLL/I2C

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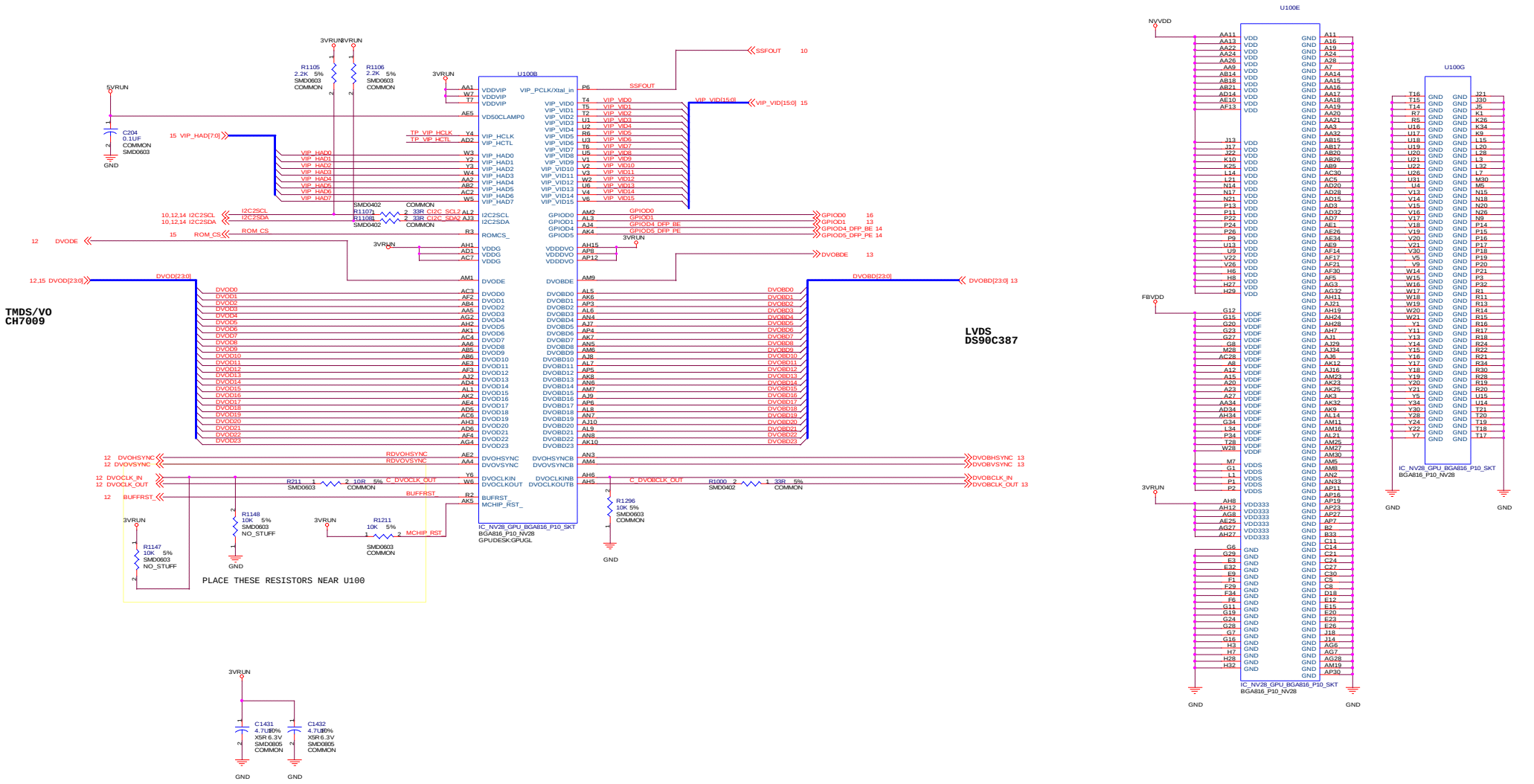

3.2 DVOA/B

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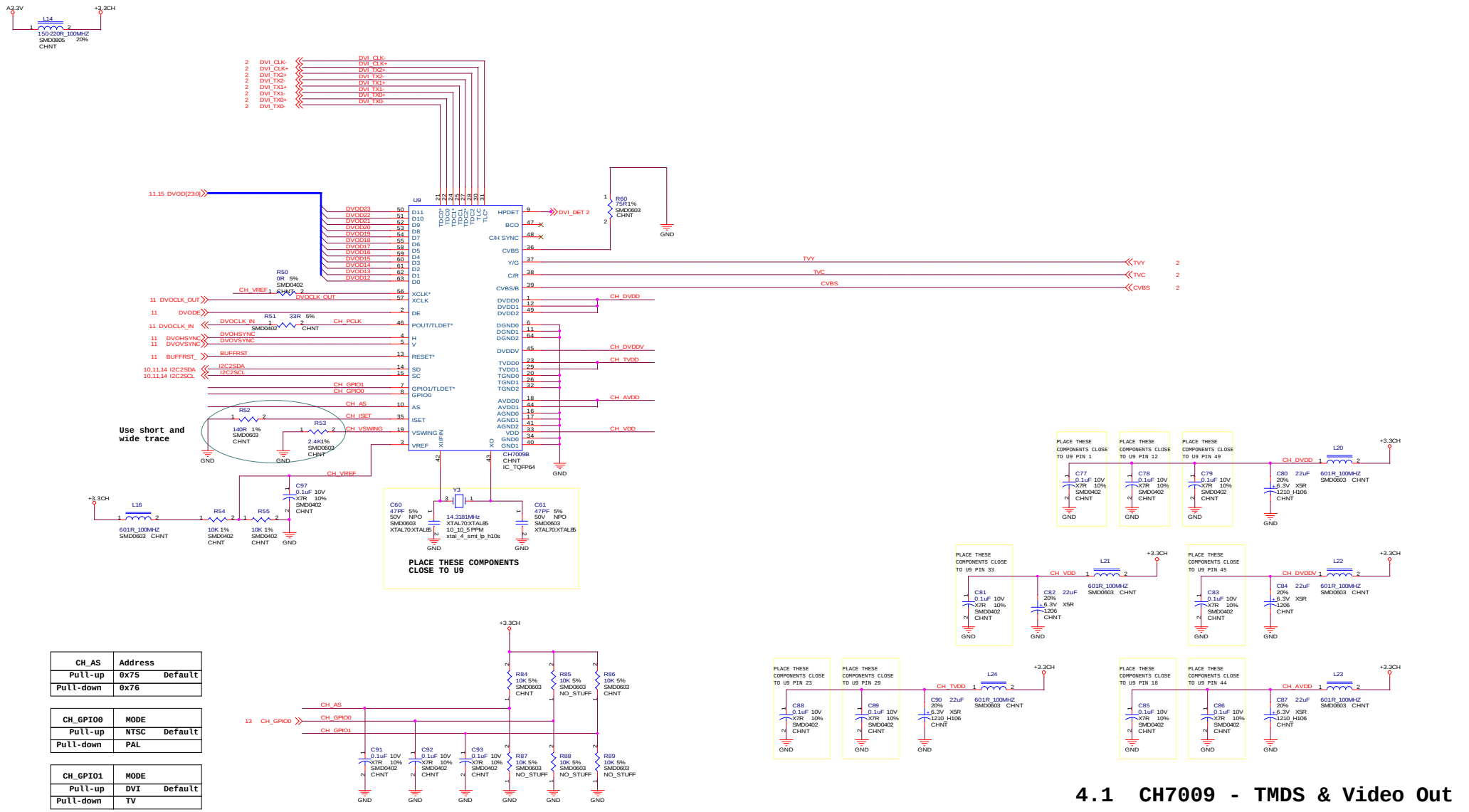

CH_AS	Address
Pull-up	0x75 Default
Pull-down	0x76

CH_GPIO0	MODE
Pull-up	NTSC Default
Pull-down	PAL

CH_GPIO1	MODE
Pull-up	DVI Default
Pull-down	TV

4.1 CH7009 - TMDS & Video Out

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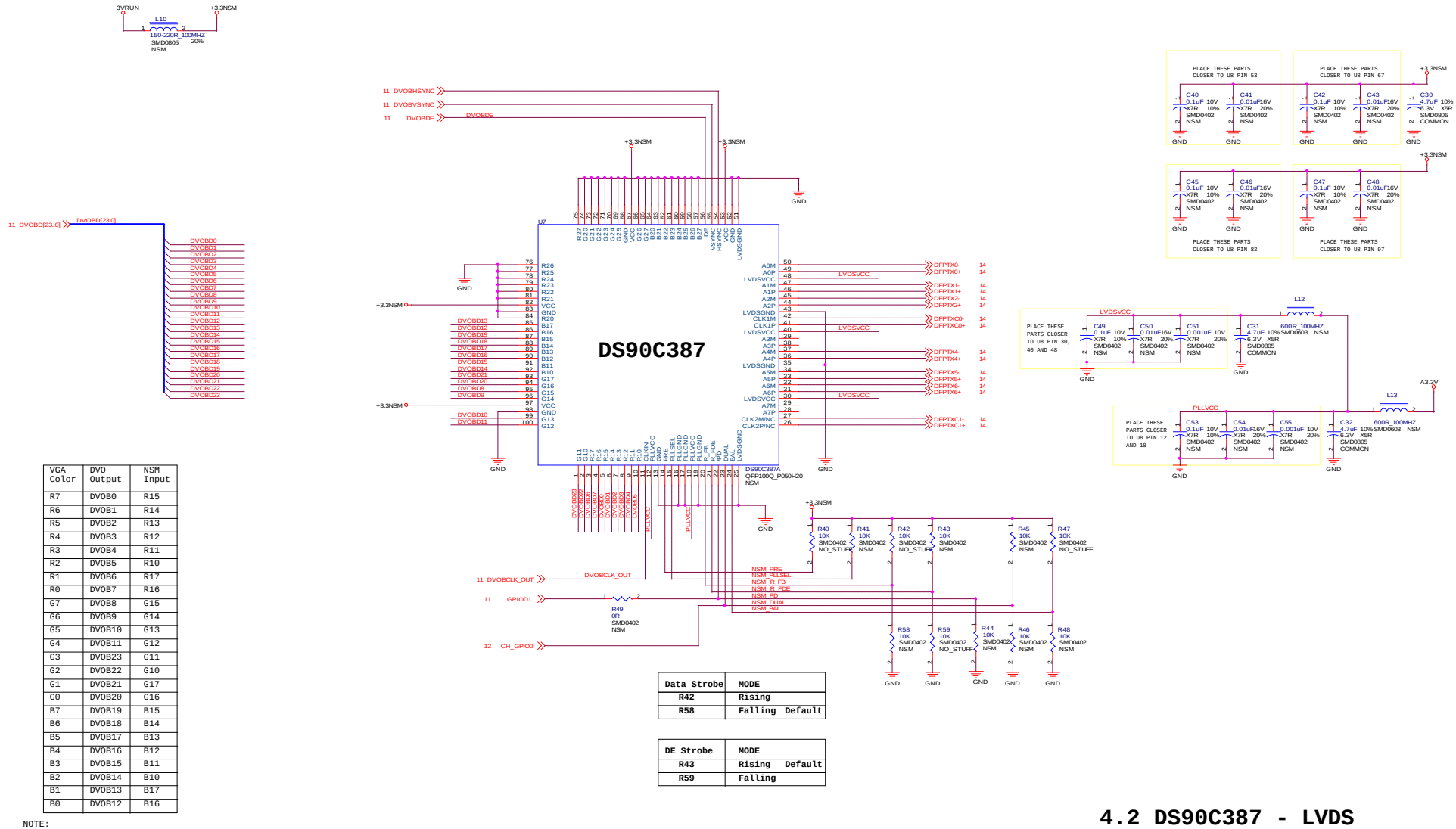

VGA Color	DVO Output	NSM Input
R7	DVOB0	R15
R6	DVOB1	R14
R5	DVOB2	R13
R4	DVOB3	R12
R3	DVOB4	R11
R2	DVOB5	R10
R1	DVOB6	R17
R0	DVOB7	R16
G7	DVOB8	G15
G6	DVOB9	G14
G5	DVOB10	G13
G4	DVOB11	G12
G3	DVOB23	G11
G2	DVOB22	G10
G1	DVOB21	G17
G0	DVOB20	G16
B7	DVOB19	B15
B6	DVOB18	B14
B5	DVOB17	B13
B4	DVOB16	B12
B3	DVOB15	B11
B2	DVOB14	B10
B1	DVOB13	B17
B0	DVOB12	B16

NOTE:

This is for single pixel per clock input mapping ONLY.

Data Strobe	MODE
R42	Rising
R58	Falling Default

DE Strobe	MODE
R43	Rising Default
R59	Falling

4.2 DS90C387 - LVDS

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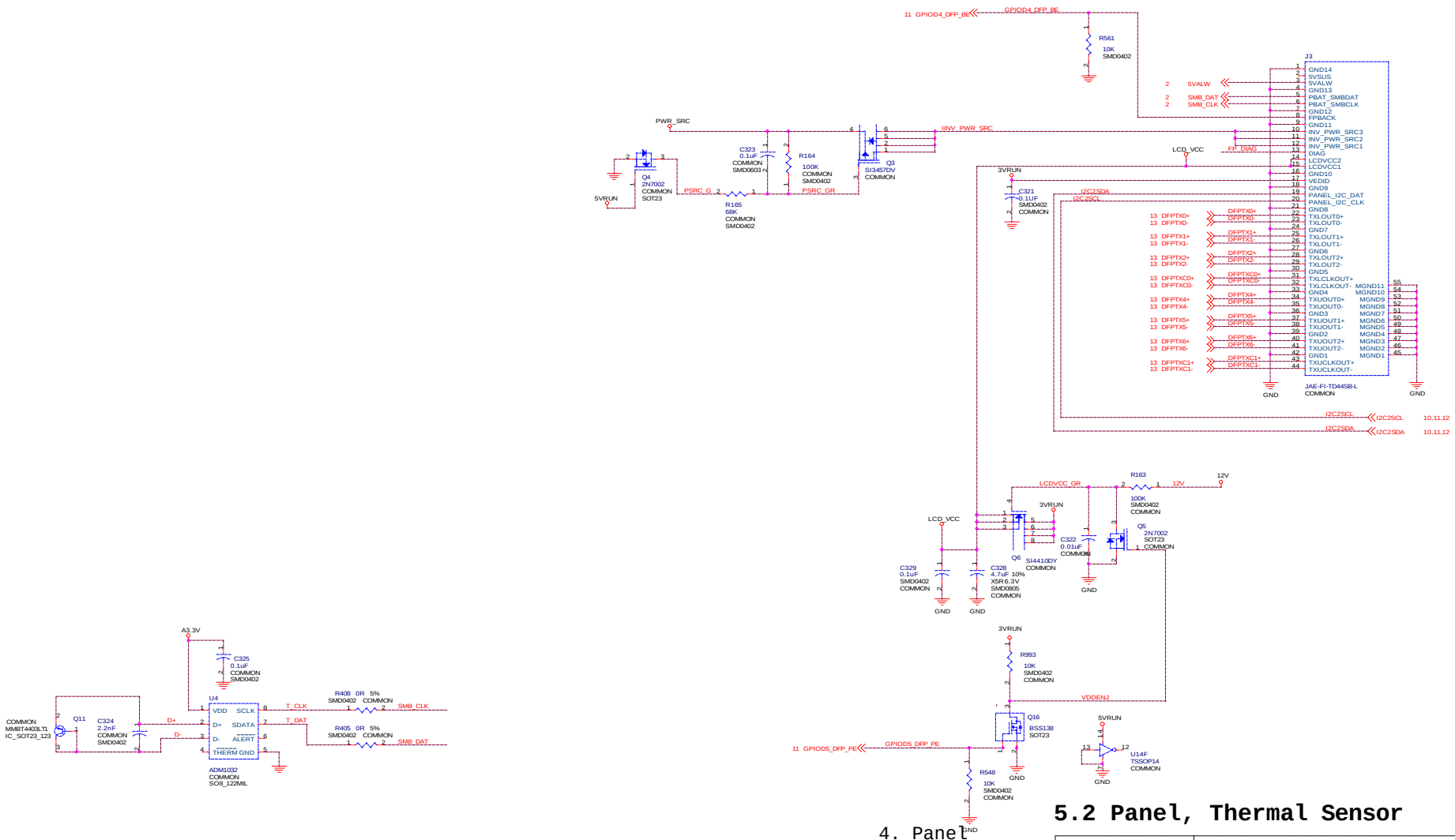

4. Panel

5.2 Panel, Thermal Sensor

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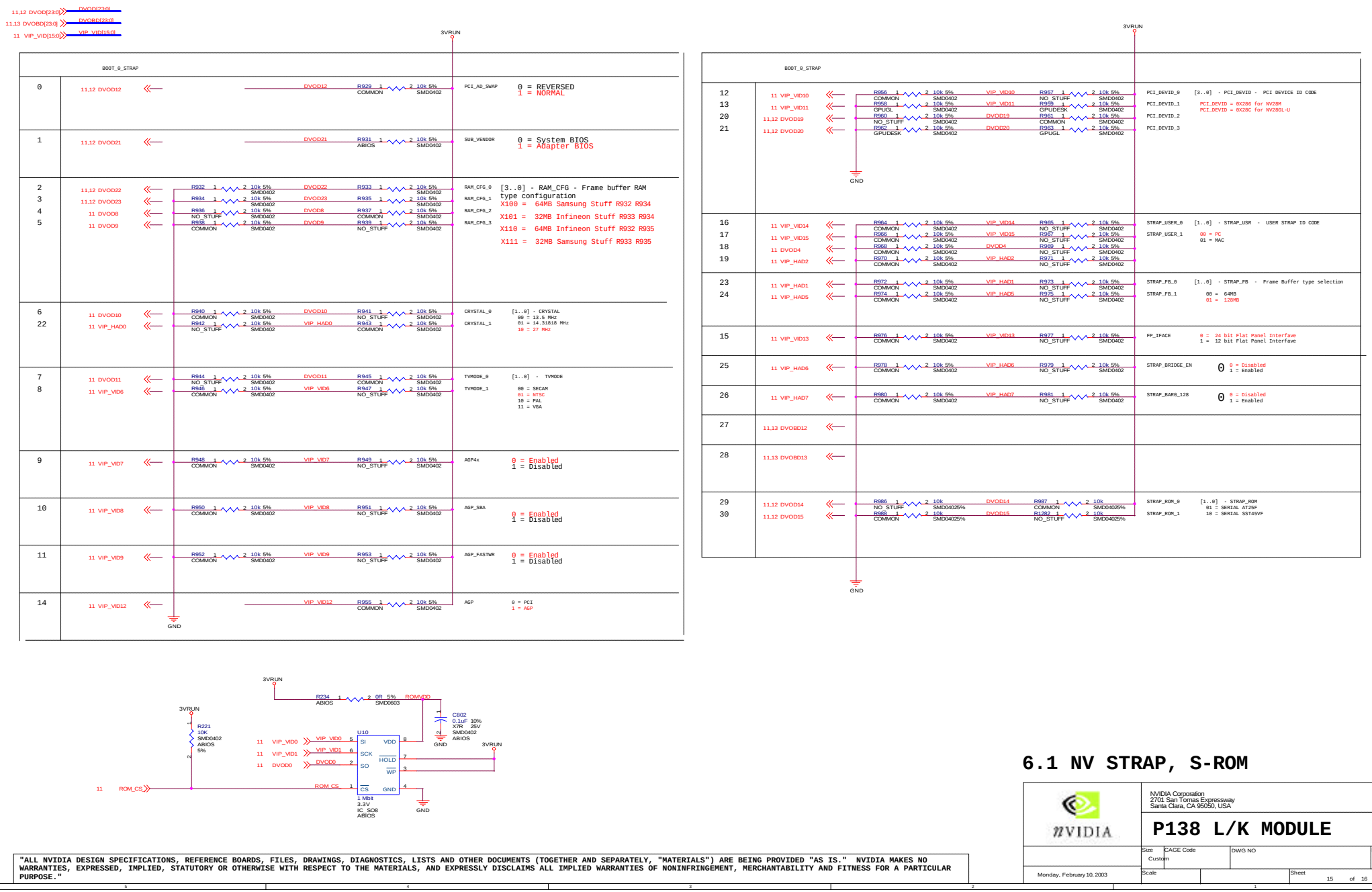

6.1 NV STRAP, S-ROM

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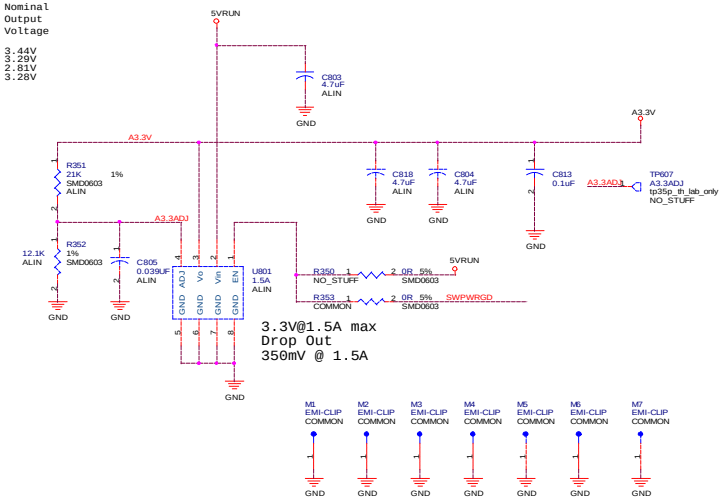
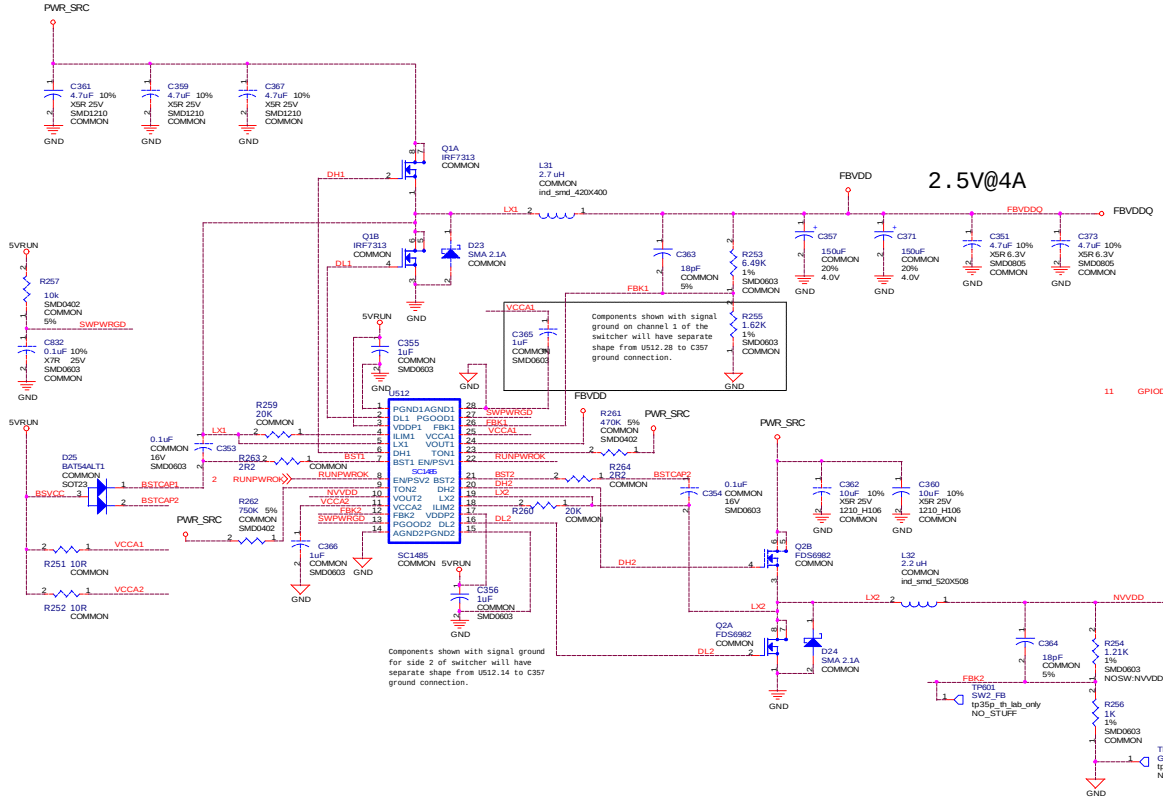
Vo=(1.20 * (R248 + R250)) / R250

R351	R352	Nominal Output Voltage
215R	115R	3.44V
200R	115R	3.29V
154R	115R	2.81V
21K	12.1K	3.28V

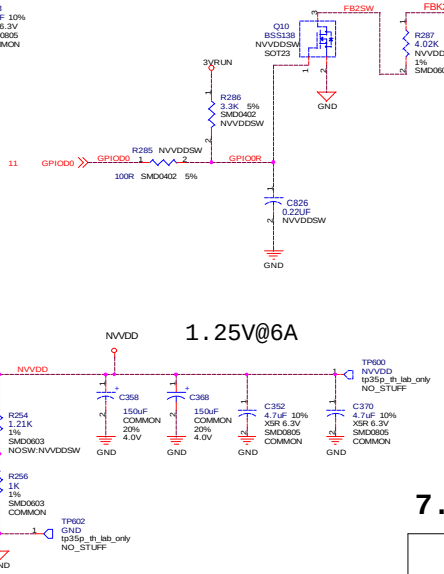
Analog 3.3V



2.5V@4A



1.25V@6A



NVVDD Switching	
GPIOD0 = 0	NVVDD = 1.10V
GPIOD0 = 1 or not driven	NVVDD = 1.25V

7.2 NVVDD/FBVDD POWER SUPPLIES

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