MS-V088 VER 0A

NV43-PCIE NV43 256MB/128bit, BGA 16MX16 DDR2,VGA,DVI-I,TV-OUT(HT-10)

P295-A00 DESIGN NV43 300/267MHZ 128MB/256MB/512MB DDR2 84-FBGA

PAGE SUMMARY:

DDR2 84-FBGA Clock setting 350MHZ

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	602-10295-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	602-10295-0000-000	GF-6600-A04 GEN 300/267MHZ 256MB 84-FBGA DDR2 16MX16 VGA+DVI-I+HDTV
2	SKU001	602-10295-0001-000	GF-6600-A04 GEN 300/267MHZ 128MB 84-FBGA DDR2 8MX16 VGA+DVI-I+HDTV
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

REV HISTORY

A00
-08/04/2005:

1.Page18: change power solution to RT9218 for NVVDD & FBVDDQ

10S
-08/04/2005:

1.Page18: Move C913~C916 out form C910,C911 & Move C930,C931 out form C929

2.Page19: Add C940 near C36

3.Page19: Remove C16, C35, C55

B00
-12/06/2005:

1.ADD G73 circuit

C00
-04/26/2006:

1.Remove NV43 reserve circuit

2.Page14: Add SPDIF circuit

3.Page15: Add TMDS Dual_Link A/B

4.Page17: Add MIOA Feature SLI CON

5.Page18,19: Modify Power solution same as P345

C01
-06/26/2006:

1.Page18:Add MIOA SLI referenc power

2.Page18:Add R0805 NVVDD to PEX1V2

3.Page18:Add NVVDD Choke Footprint

4.Page15/16:Add Bridge R for EMI

AOO
-11/10/2006:V041-3.1 change model name to V088-0A

1.Page17:MIOA/B SLI signals resverve

2.Page13:Straps reserve for G84

3.Page10/11/12:Reserve DAC_VREF for G84 DAC

4.Page3/4:Reserve FBIO ODT for G84 DDR2

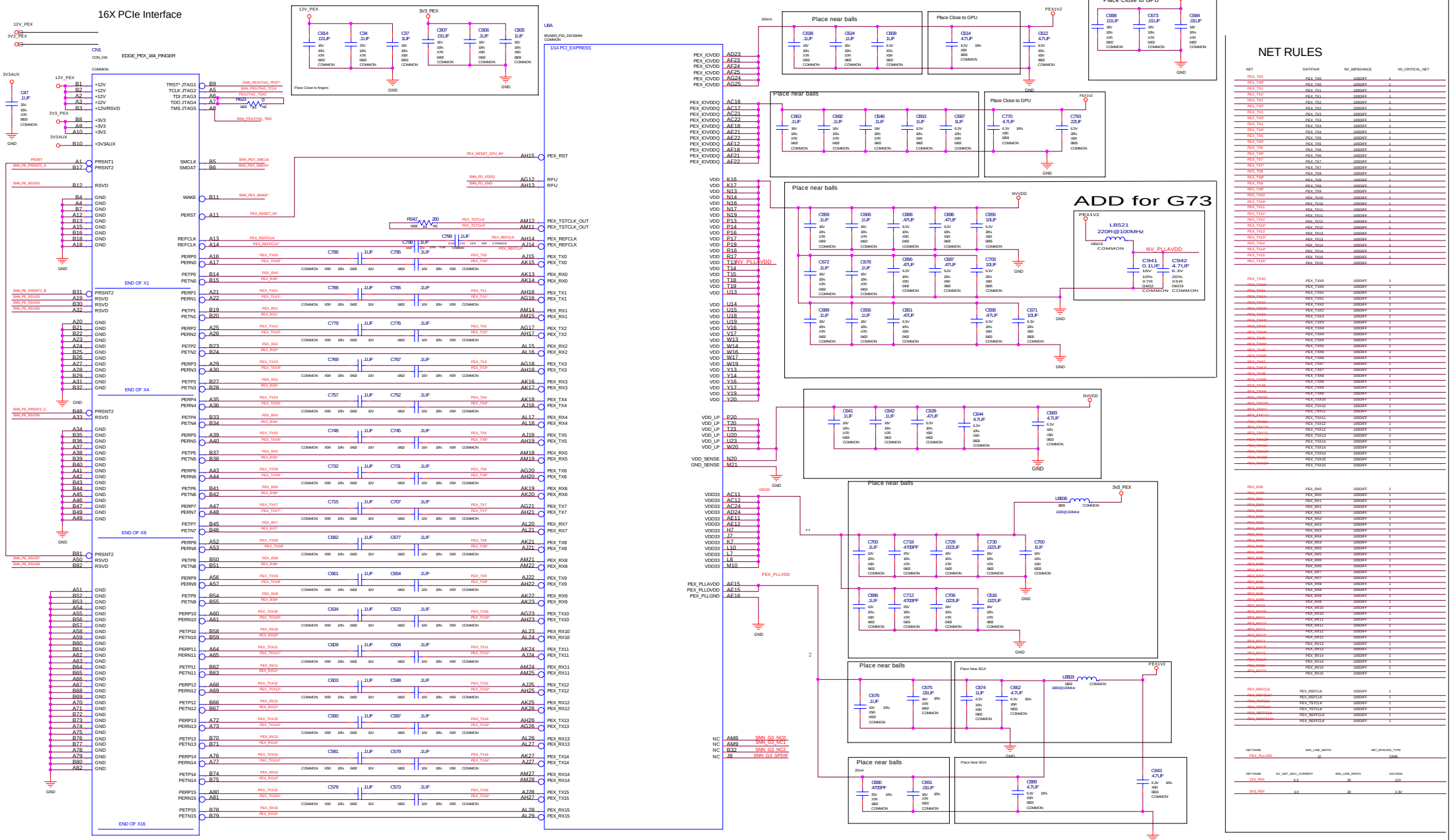
5.Page3/4:Reserve FBIO External VREF for G84

6.Page3/4/5/6/7/8:Reserve FBIO Dual Rank Inplementation for G84

7.Page3/4/14:Reserve I/O changes for G84

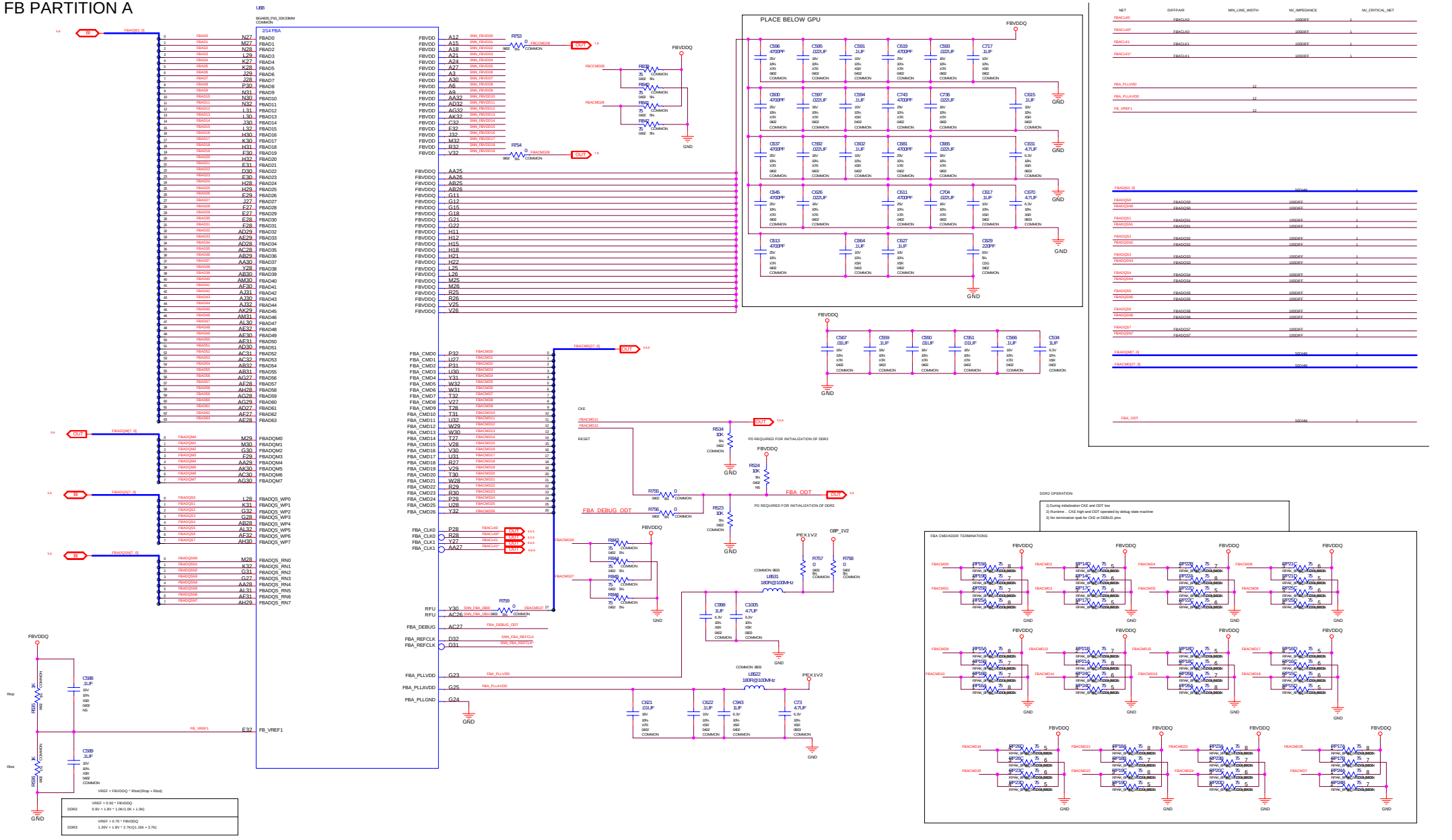
8.Page3/9/15/16/19:Reserve Power rail for G84

02 PCI EXPRESS, NVVDD, VDD33



03 FB BANK A, FBVDDQ DECOUPLING

FB PARTITION A



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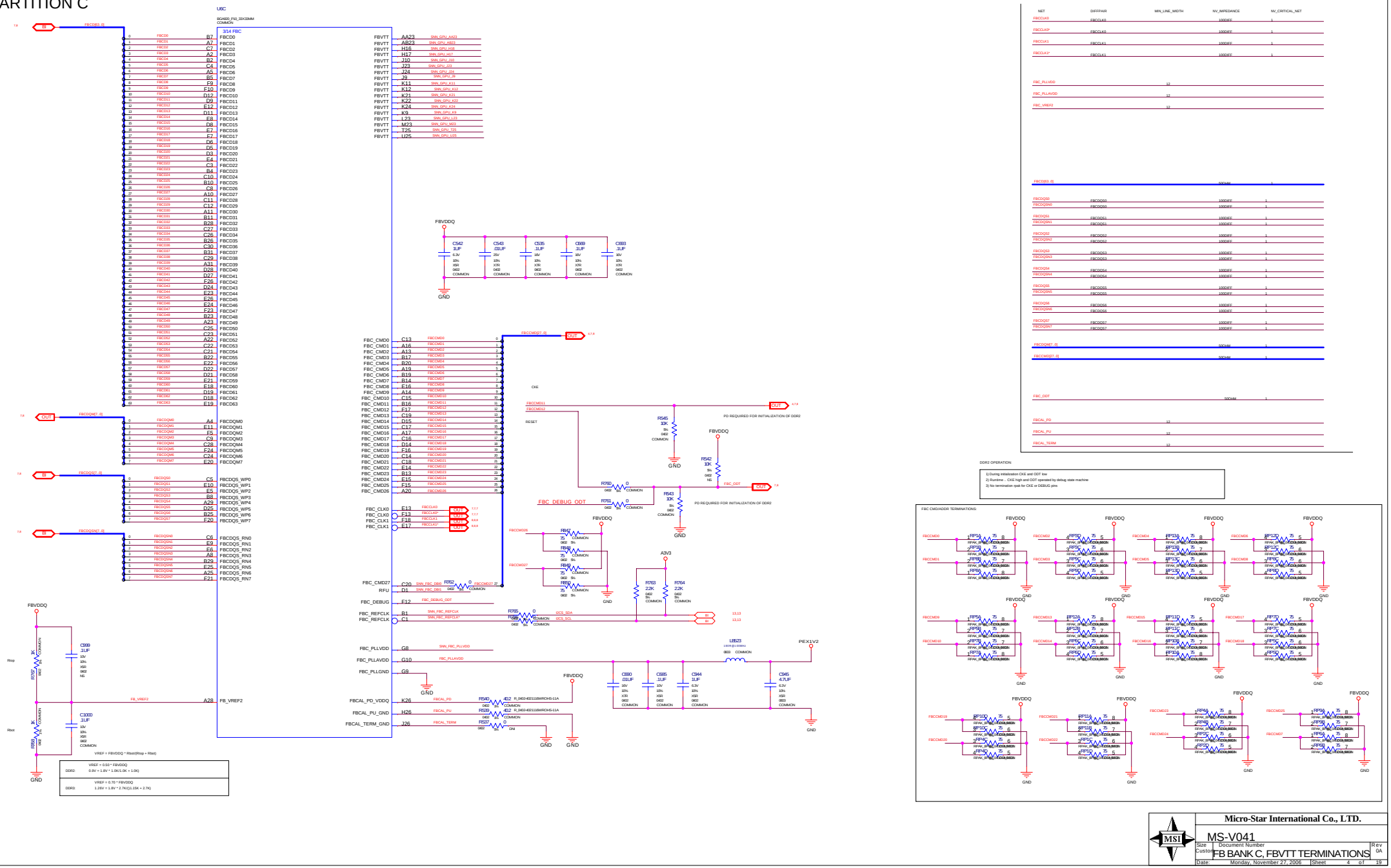
Size: Custom	Document Number: FB BANK A,FBVDDQ DECOUPLING		Rev: 0A
Date: Monday, November 27, 2006	Sheet 3 of 19		

04 FB BANK C, FBVTT TERMINATIONS

FB PARTITION C



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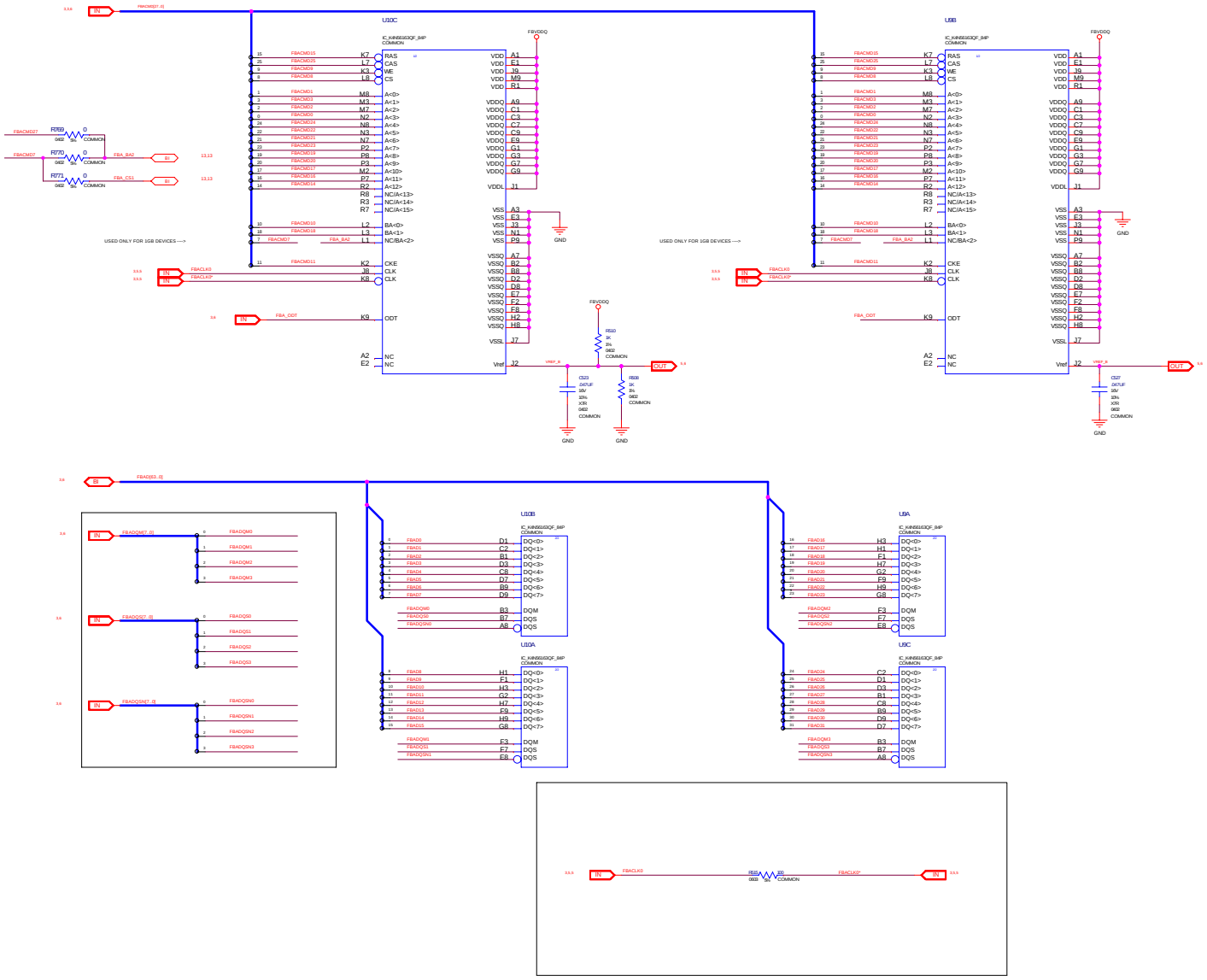
Size: Custom	Document Number: FB BANK C, FBVTT TERMINATIONS		Rev: 0A
Date: Monday, November 27, 2006	Sheet 4 of 19		

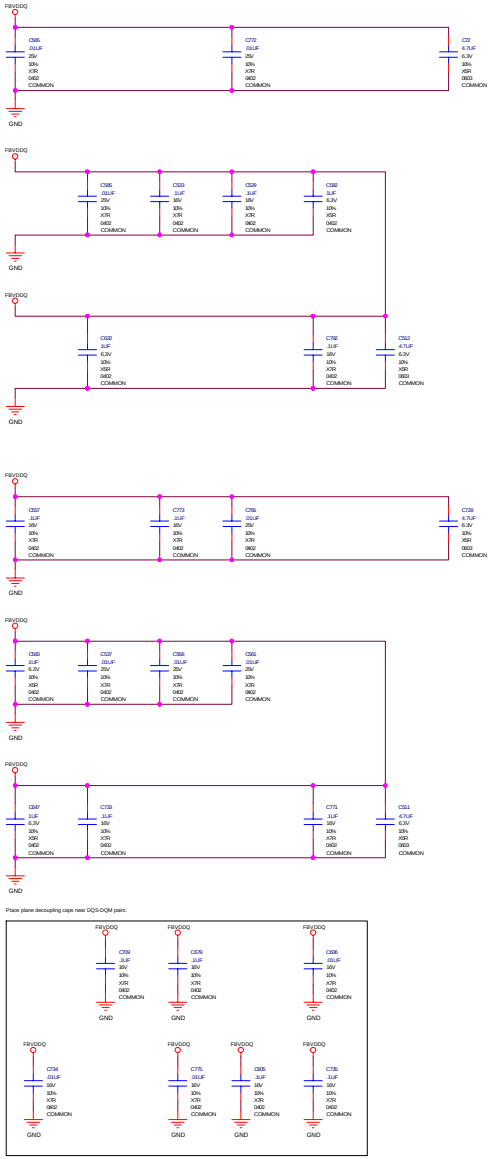
05 MEMORY PARTITION A 0..31

FBA MEMORY 1st bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



16x power/gnd pin pairs per mem
3x 0.022uF - 5.3 to 1
6x 4700uF - 2.7 to 1
5x 220pF - 3.2 to 1
2x 0.047uF - 8 to 1
2x 4.7uF - 8 to 1



Place plane decoupling caps near DQS-DQM pairs.

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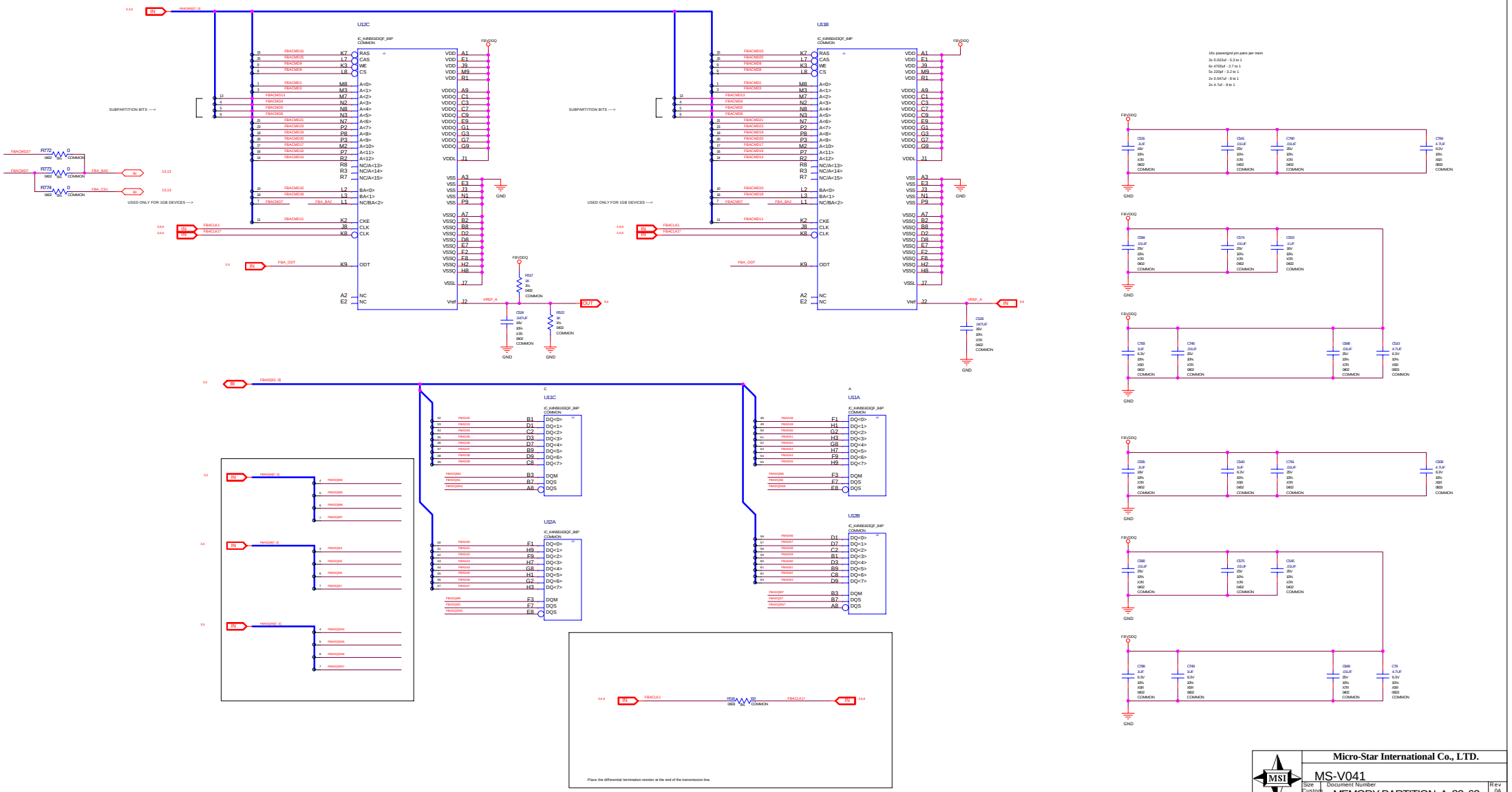
Size: Custom	Document Number: MEMORY PARTITION A 0..31	Rev: 0A
Date: Tuesday, November 28, 2006	Sheet 5 of 19	

06 MEMORY PARTITION A 32..63

FBA MEMORY 1st bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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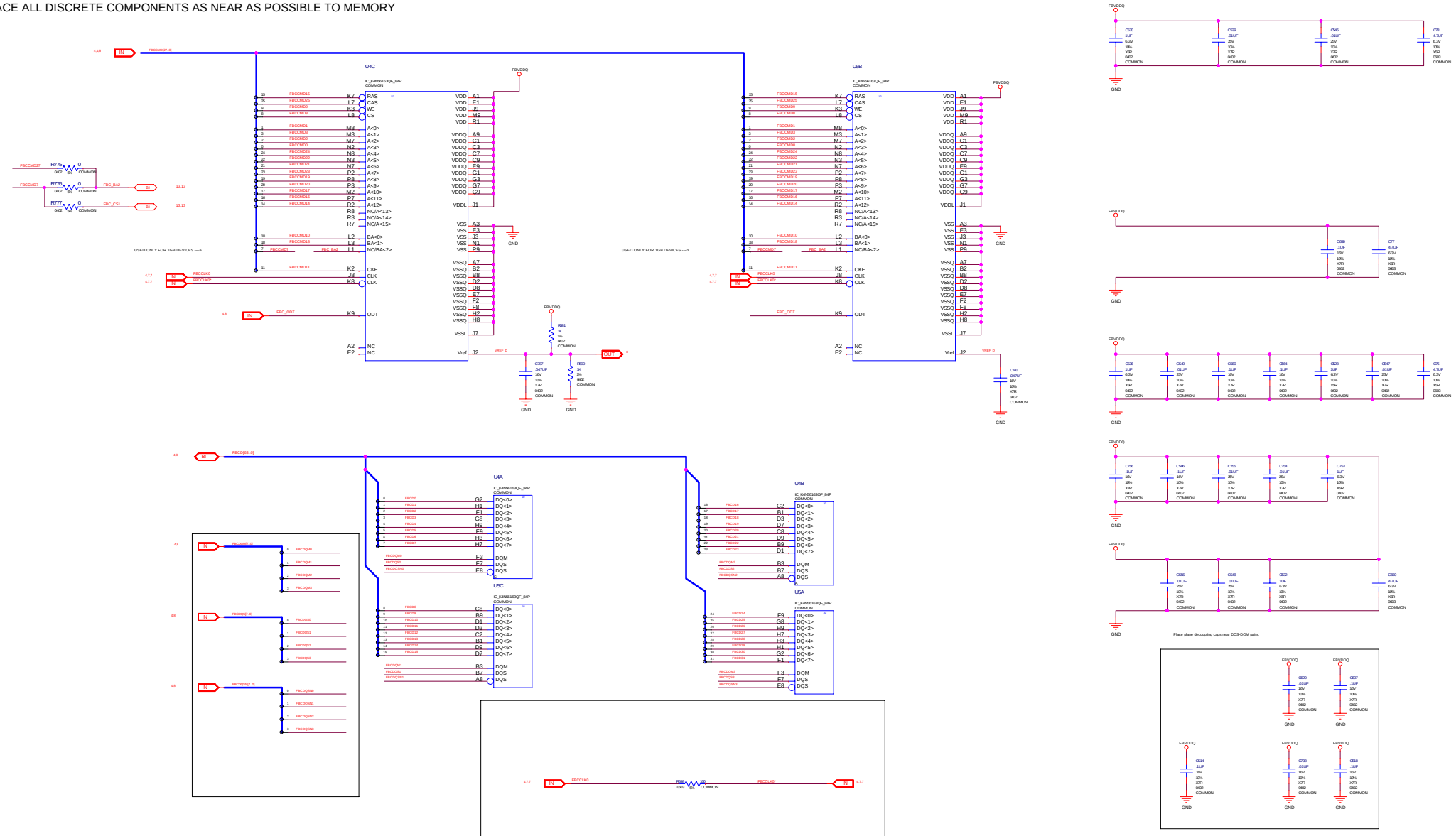
Size: Custom	Document Number: MEMORY PARTITION A 32..63		Rev: 0A
Date: Tuesday, November 28, 2006	Sheet 6 of 19		

07 MEMORY PARTITION C 0..31

FBC MEMORY 2nd bank 0..31

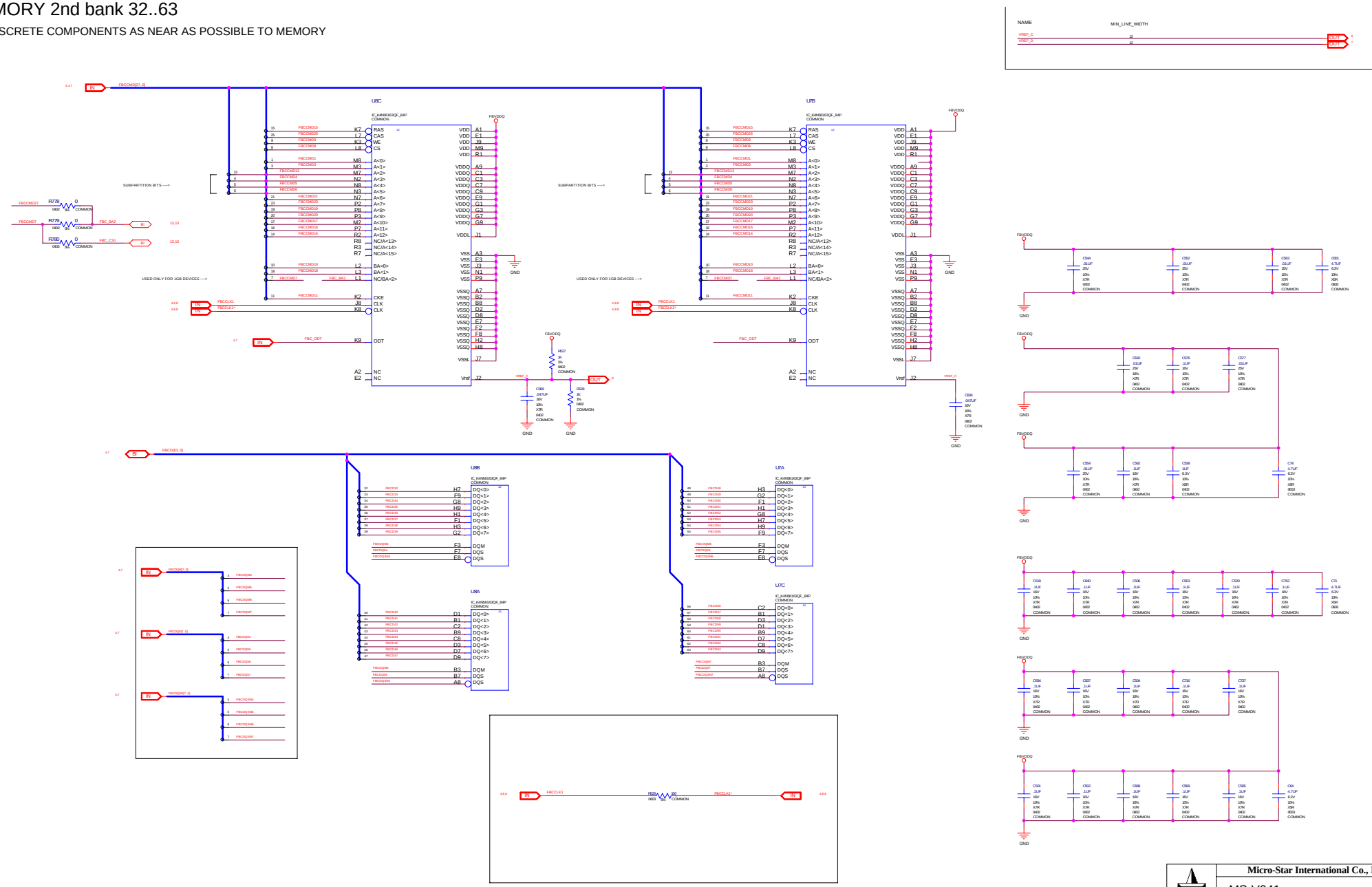
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



08 MEMORY PARTITION C 32..63

FBC MEMORY 2nd bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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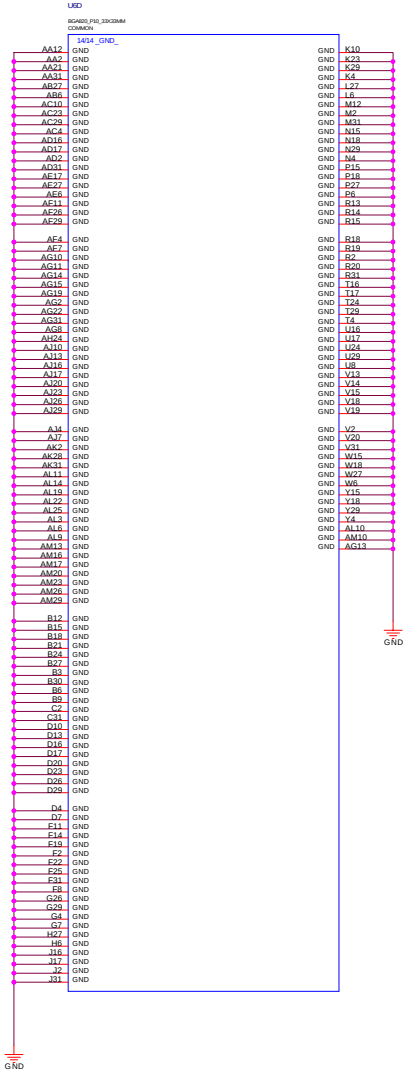
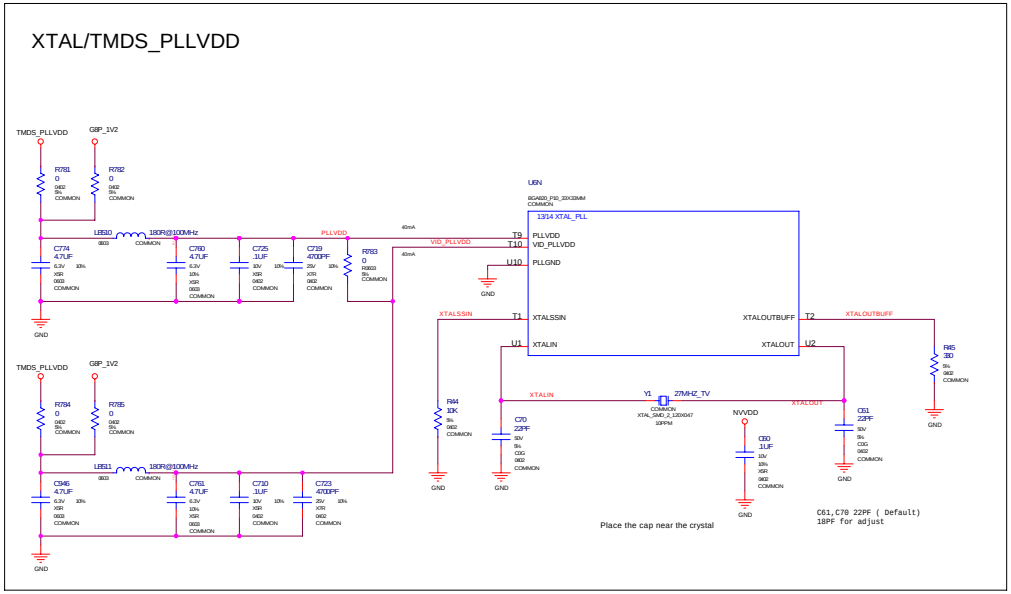
MS-V041	
Size: Custom	Document Number: MEMORY PARTITION C 32..63
Rev: 0A	
Date: Tuesday, November 28, 2006	Sheet 8 of 19

09 GPU GND / TMDS_PLLVDD





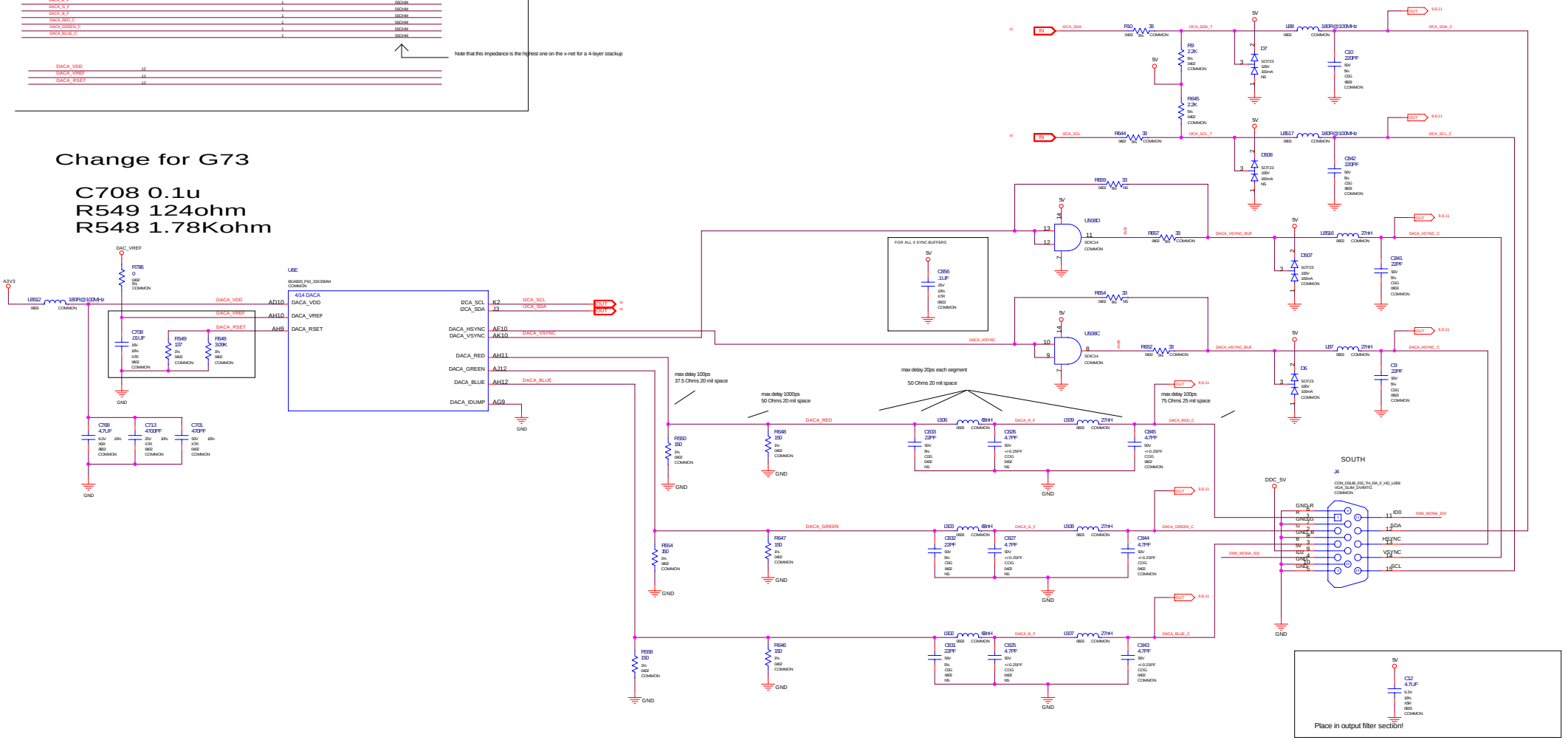
10 DACA - VGA

NET_NAME	MIN_LINE_WIDTH	NV_CRITICAL_NET	NV_IMPEDANCE
I2CA_SCL			
I2CA_SDA			
DACA_HSYNC		2	50OHM
DACA_VSYNC		2	50OHM
DACA_HSYNC_BUF		2	50OHM
DACA_VSYNC_BUF		2	50OHM
DACA_VSYNC_C		2	50OHM
DACA_HSYNC_C		2	50OHM
AVIB		2	50OHM
A VIB		2	50OHM
DACA_RED		1	50OHM
DACA_GREEN		1	50OHM
DACA_BLUE		1	50OHM
DACA_G_F		1	50OHM
DACA_R_F		1	50OHM
DACA_RED_C		1	50OHM
DACA_GREEN_C		1	50OHM
DACA_BLUE_C		1	50OHM
DACA_VDD	12		
DACA_VREF	12		
DACA_RSET	12		

Note that this impedance is the highest one on the x-net for a 4-layer stackup

Change for G73

C708 0.1u
R549 124ohm
R548 1.78Kohm



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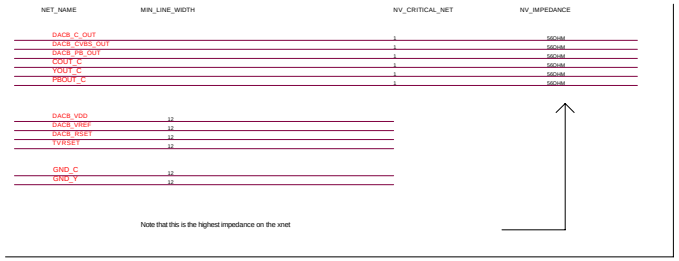
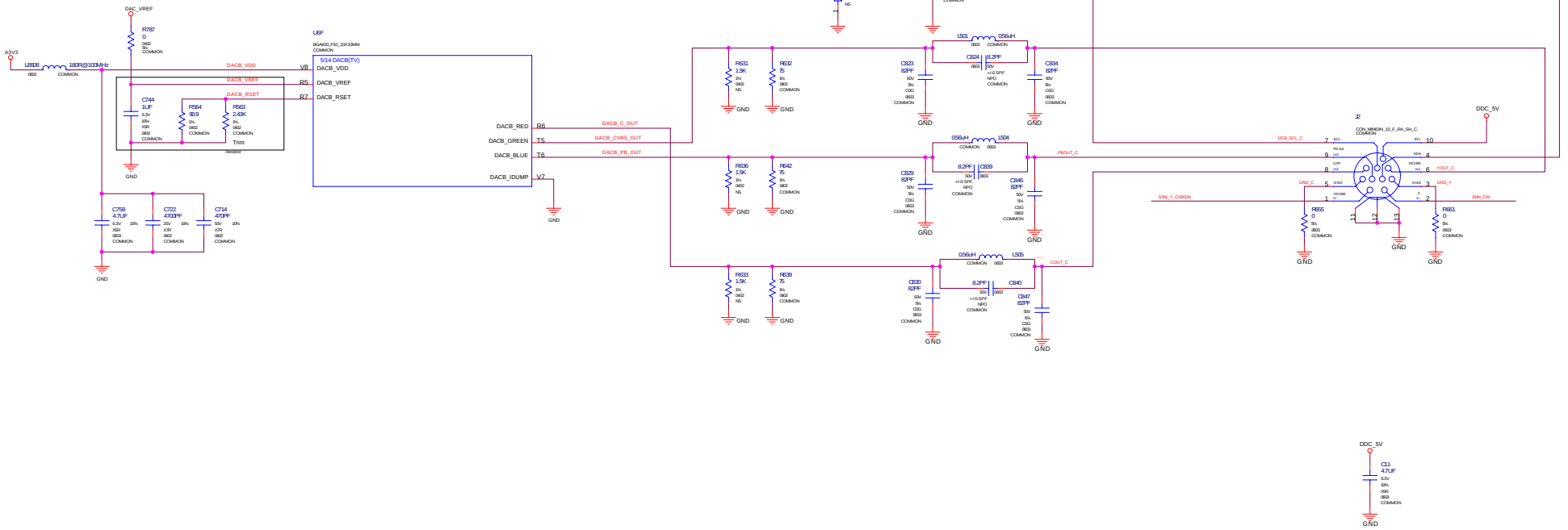
MS-V041
Size: Custom | Document Number: DACA - VGA | Rev: 0A
Date: Monday, November 13, 2006 | Sheet 10 of 19

11 DACB - TVOUT, VIDEO IN



Change for G73

C744 0.1u
R564 124ohm
R563 1.78Kohm



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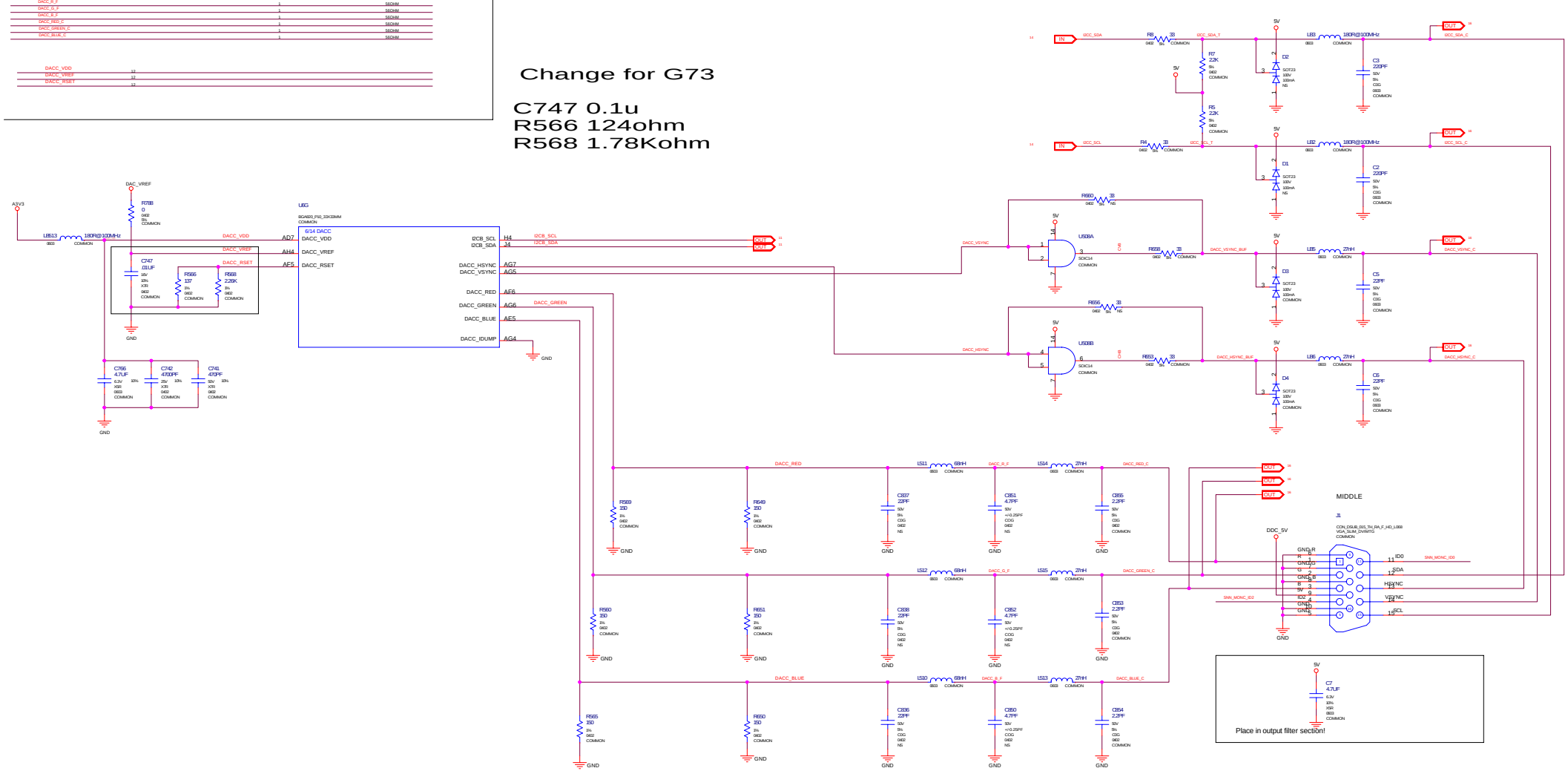
MS-V041		
Size: Custom	Document Number: DACB - TVOUT, VIDEO IN	Rev: 0A
Date: Monday, November 13, 2006	Sheet 11 of 19	

12 DACC - VGA

NET_NAME	MIN_LINE_WIDTH	NET_SPACING_RULE	NV_CRITICAL_NET	NV_IMPEDANCE
I2CB_SCL				
I2CB_SDA				
DACC_HSYNC		2		50OHM
DACC_VSYNC		2		50OHM
DACC_HSYNC_BUF		2		50OHM
DACC_VSYNC_BUF		2		50OHM
DACC_VSYNC_C		2		50OHM
DACC_HSYNC_C		2		50OHM
CHB		2		50OHM
CVB		2		50OHM
DACC_RED		1		50OHM
DACC_GREEN		1		50OHM
DACC_BLUE		1		50OHM
DACC_R_F		1		50OHM
DACC_G_F		1		50OHM
DACC_B_F		1		50OHM
DACC_RED_C		1		50OHM
DACC_GREEN_C		1		50OHM
DACC_BLUE_C		1		50OHM
DACC_VDD		12		
DACC_VREF		12		
DACC_RSET		12		

Change for G73

C747 0.1u
R566 124ohm
R568 1.78Kohm



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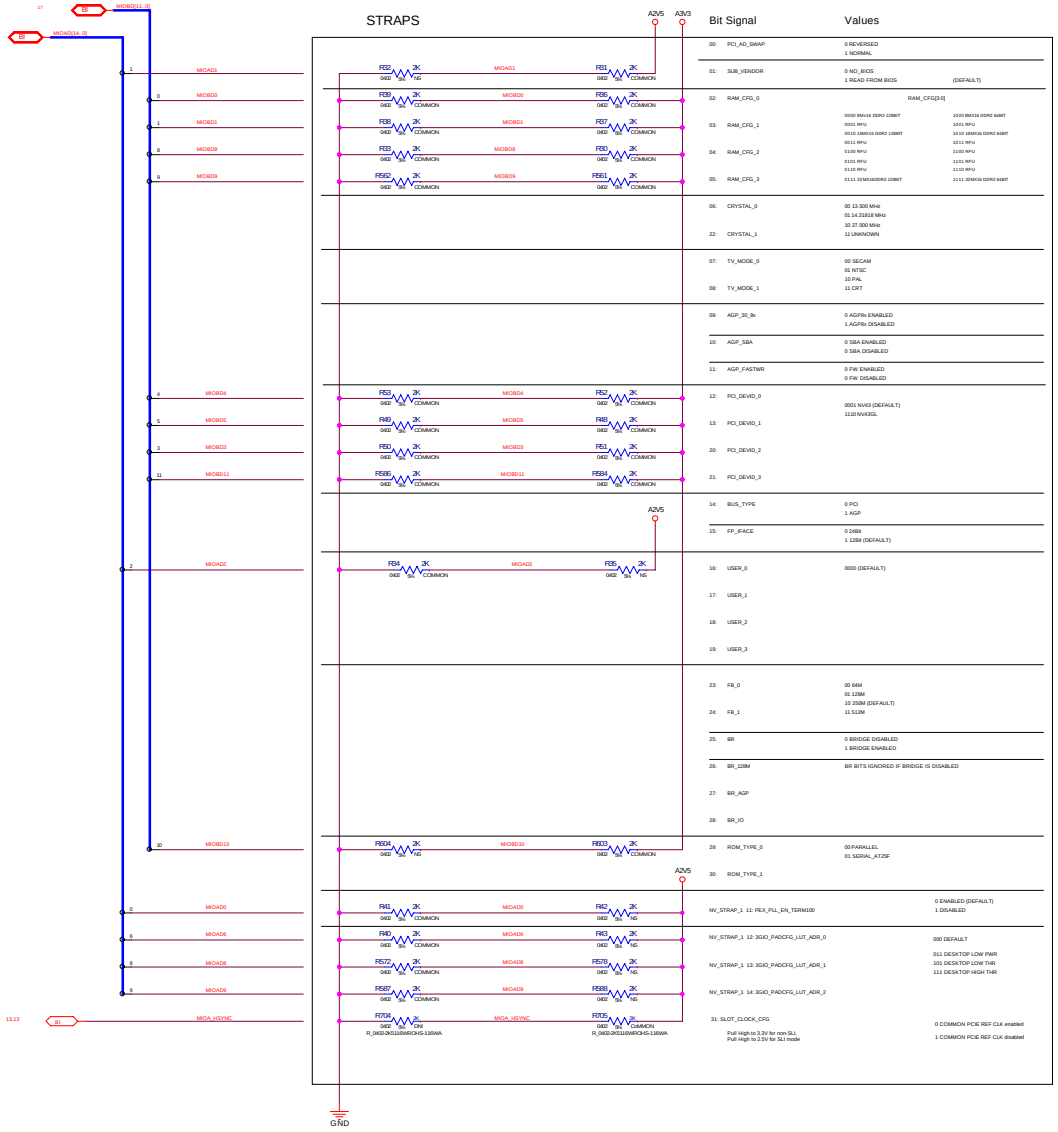
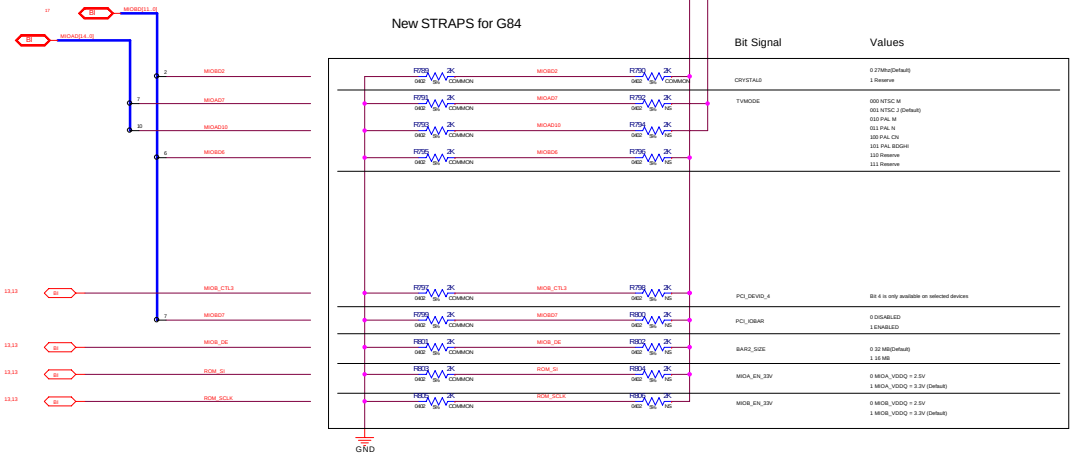
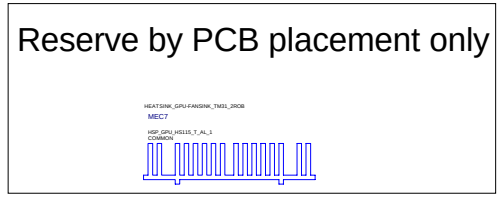
MS-V041	
Size: Custom	Document Number: DACC - VGA
Rev: 0A	
Date: Monday, November 13, 2006	Sheet 12 of 19

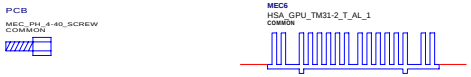
13 STRAPS, FANSINK, MECHANICALS (Strap R using 2K if no specail requred)

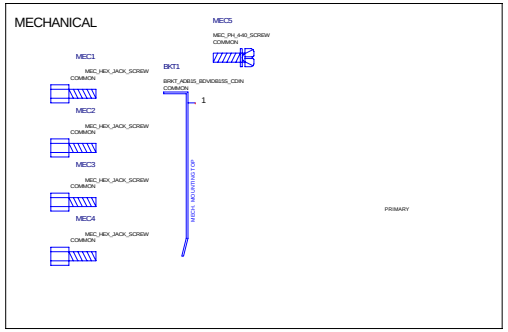


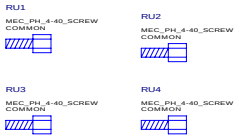


Reserve by PCB placement only









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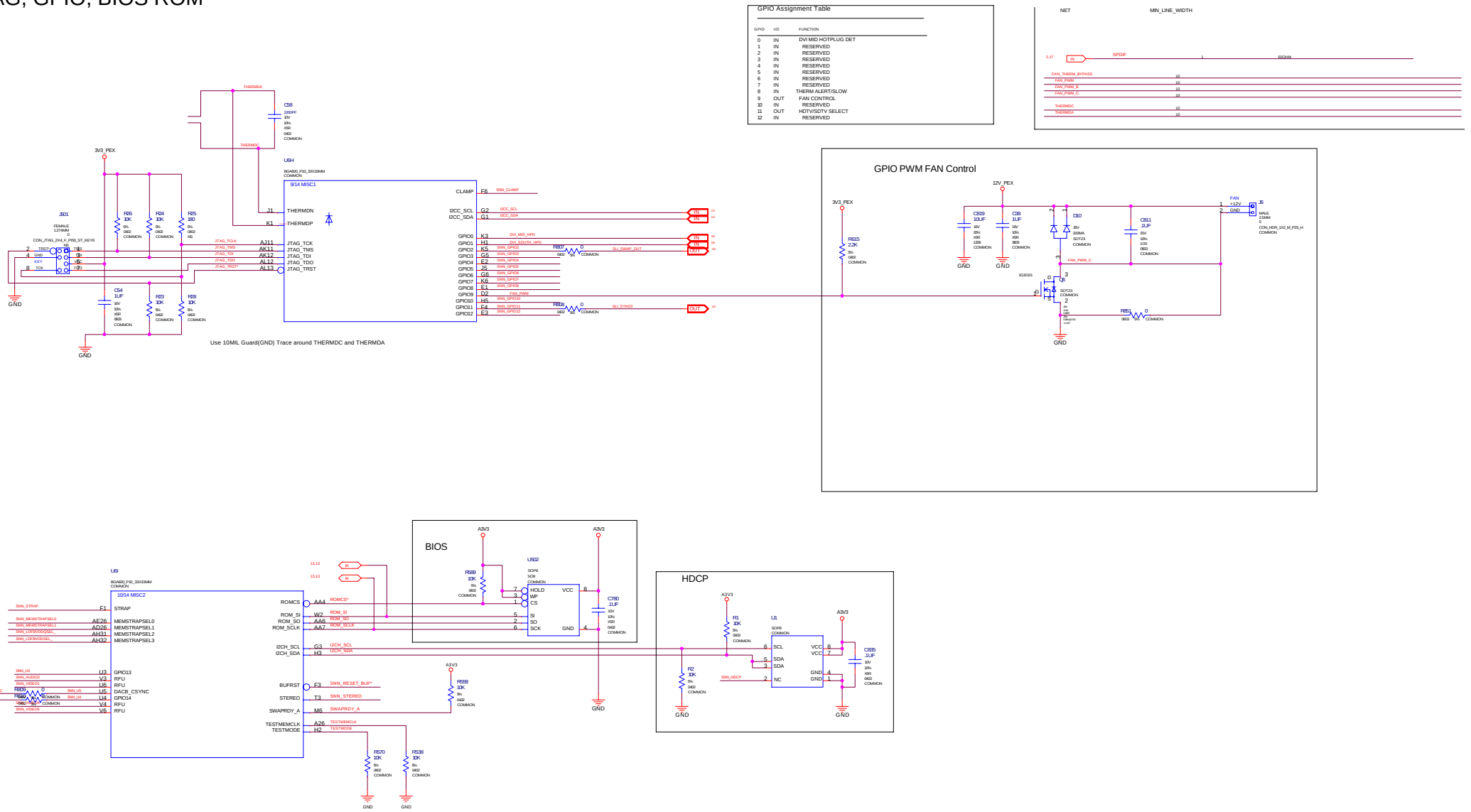
MS-V041		
Size: Custom	Document Number: STRAPS, FANSINK, MECHANICALS	Rev: 0A
Date: Monday, December 04, 2006	Sheet 13 of 19	

14 GPIO, HDCP, VBIOS, FAN CON

JTAG, GPIO, BIOS ROM



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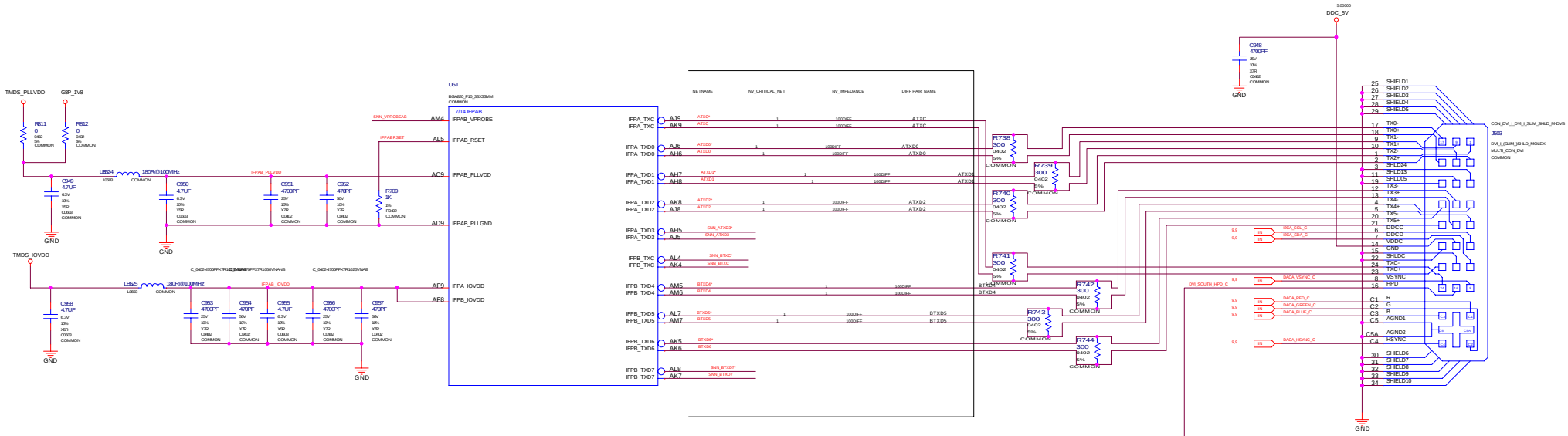
MS-V041	
Size: Custom	Document Number: GPIO, HDCP, VBIOS, FAN CON
Rev: 0A	
Date: Thursday, November 30, 2006	Sheet 14 of 19

15 INTERNAL TMDS LINK A/B

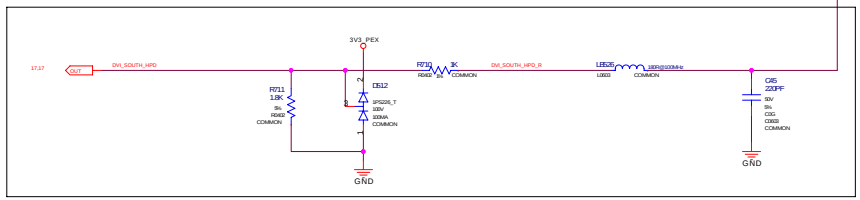
IFPAB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RSET	1	50OHM	
DVI_SOUTH_HPD_C	1	50OHM	
DVI_SOUTH_HPD_R	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLLVDD	2.20000	0.04	16.0
IFPAB_IOVDD	2.20000	0.24	16.0



Hotplug Detection



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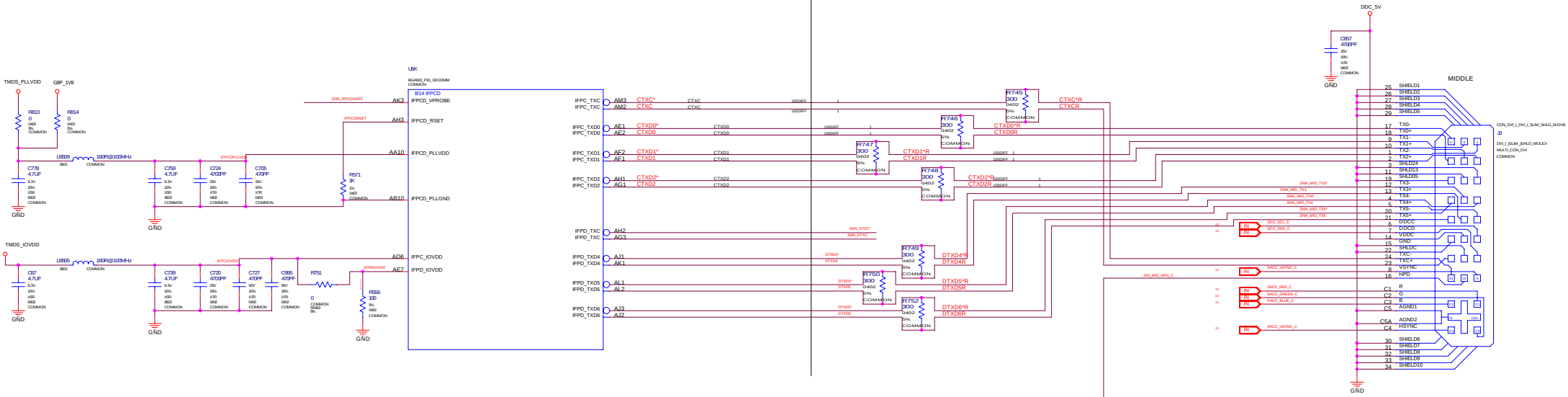
MS-V041		
Size: Custom	Document Number: INTERNAL TMDS LINK A/B	Rev: 0A
Date: Monday, November 13, 2006	Sheet: 15 of 19	

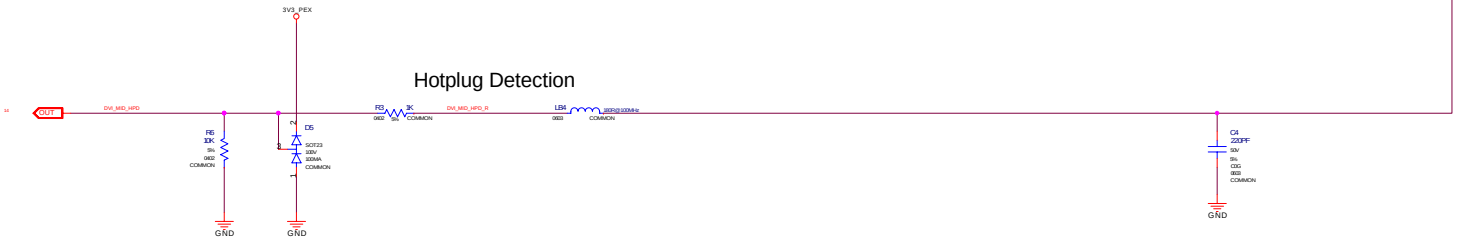
16 INTERNAL TMDS LINK C/D

NET	MIN_LINE_WIDTH	VOLTAGE
IFPCDVREF	12	3.3V
IFPCDPLLVDD	12	3.3V
IFPCIOVDD	12	3.3V
IFPIOVDD	12	3.3V
IFPCDRSET	12	

INTERNAL TMDS ..LINK C



Hotplug Detection



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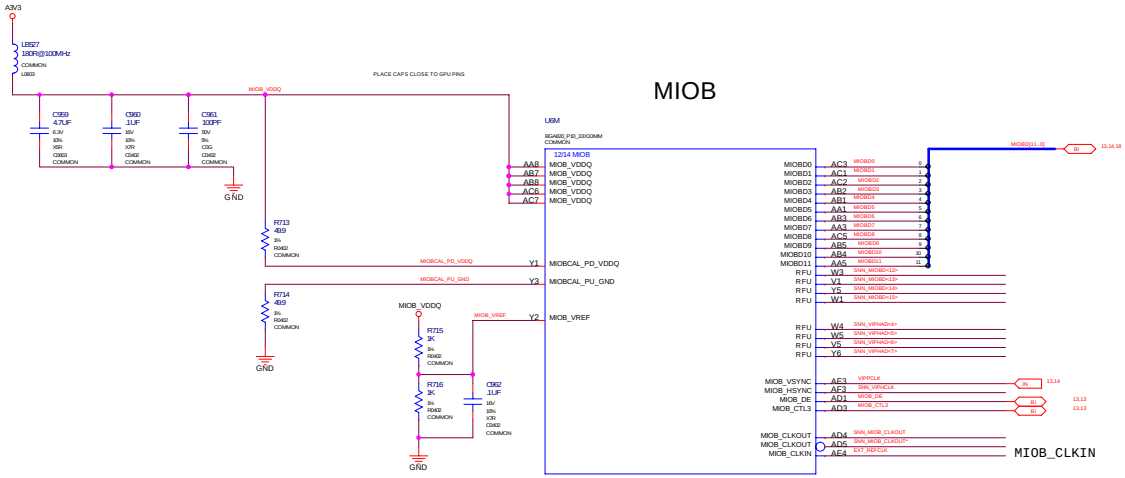
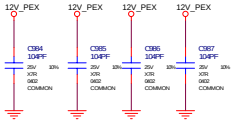
MS-V041		
Size: Custom	Document Number: INTERNAL TMDS LINK C/D	Rev: 0A
Date: Monday, November 13, 2006	Sheet 16 of 19	

17 MIOA, MIOB, NVPLL

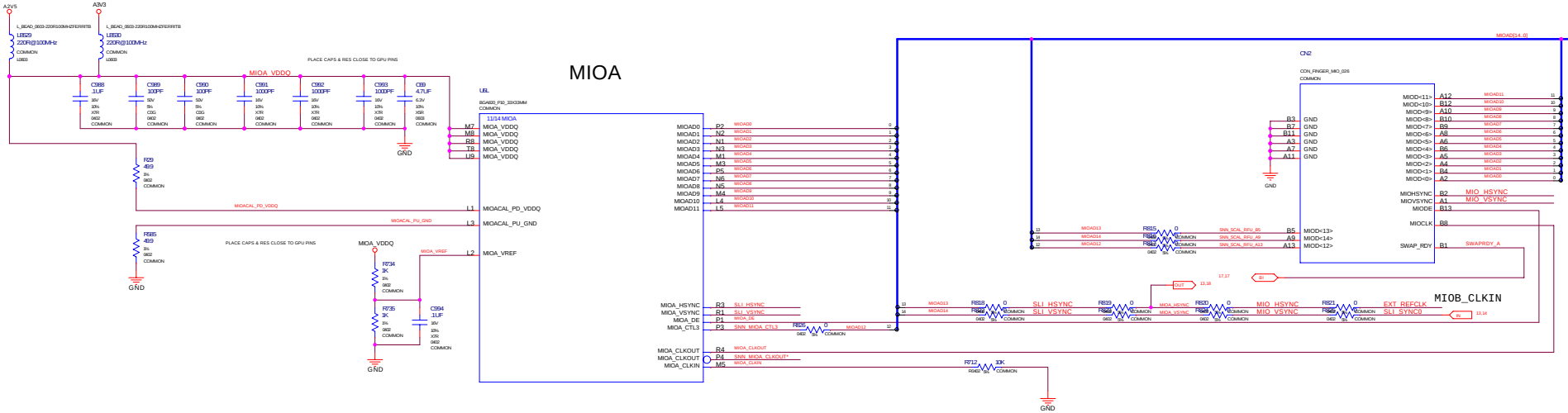
MIO NET RULES

MIOB





MIOA



Feature Connector

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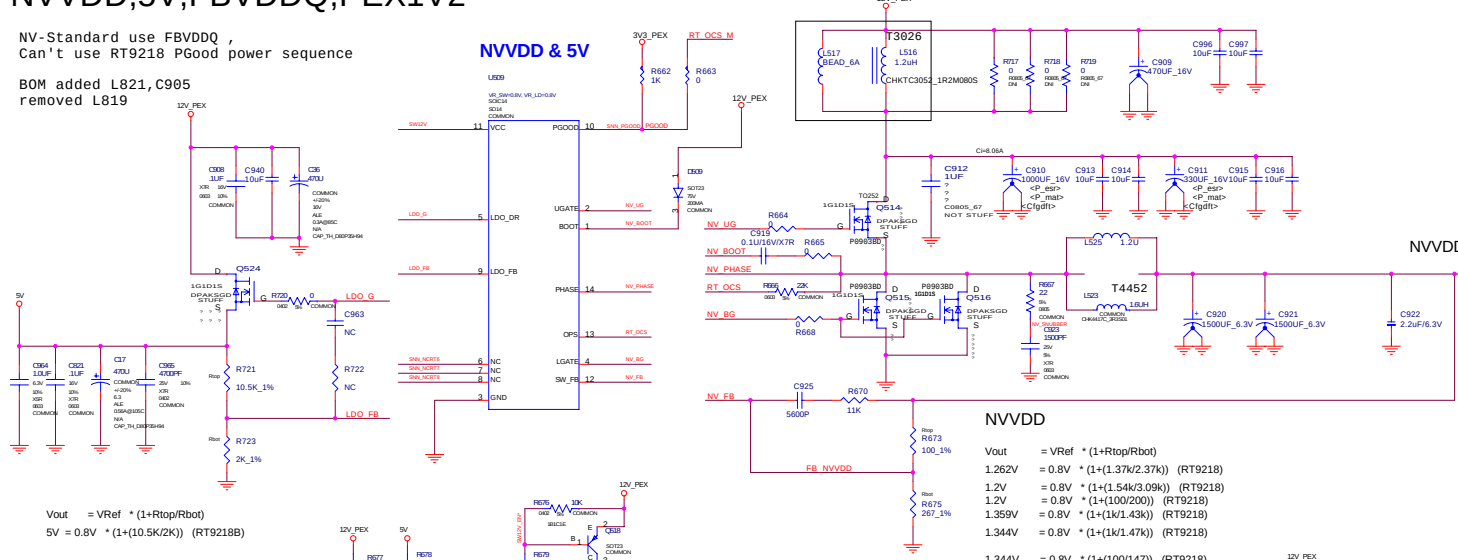
Size: Custom | Document Number: MIOA, MIOB, NVPLL | Rev: 0A
Date: Tuesday, November 28, 2006 | Sheet 17 of 19

18 Power Supply (RT9218)
NVVDD,5V,FBVDDQ,PEX1V2

NV-Standard use FBVDDQ ,
Can't use RT9218 PGood power sequence

BOM added L821,C905
removed L819

NVVDD & 5V



NVVDD = 1.35V @ upto 18A

1.2V~1.4V/24A(ambient)

NVVDD = 0.8V * (1+Rt/Rb)

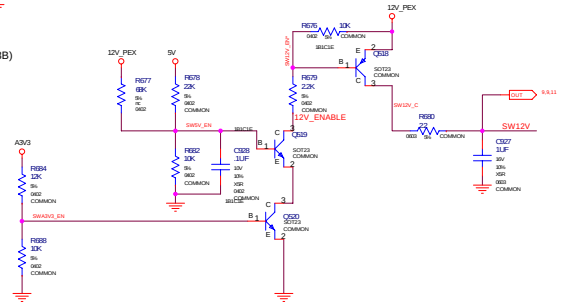
NVVDD

Vout = VRef * (1+Rtop/Rbot)

1.262V	= 0.8V * (1+(1.37k/2.37k))	(RT9218)
1.2V	= 0.8V * (1+(1.54k/3.09k))	(RT9218)
1.2V	= 0.8V * (1+(100/200))	(RT9218)
1.359V	= 0.8V * (1+(1k/1.43k))	(RT9218)
1.344V	= 0.8V * (1+(1k/1.47k))	(RT9218)
1.344V	= 0.8V * (1+(100/147))	(RT9218)
1.3V	= 0.8V * (1+(100/160))	(RT9218) default
1.099V	= 0.8V * (1+(100/267))	(RT9218) default

Vout = VRef * (1+Rtop/Rbot)

5V = 0.8V * (1+(10.5K/2K)) (RT9218B)

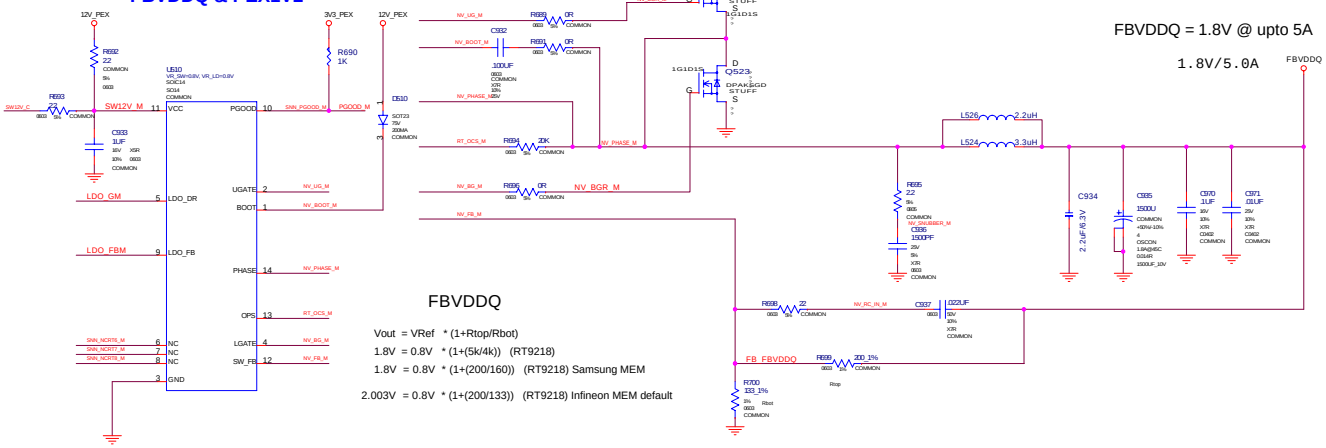


FBVDDQ & PEX1V2

Choose RT9218 PGood power sequence

Added BOM R883,R904

Removed R905



FBVDDQ = 1.8V @ upto 5A

1.8V/5.0A

FBVDDQ

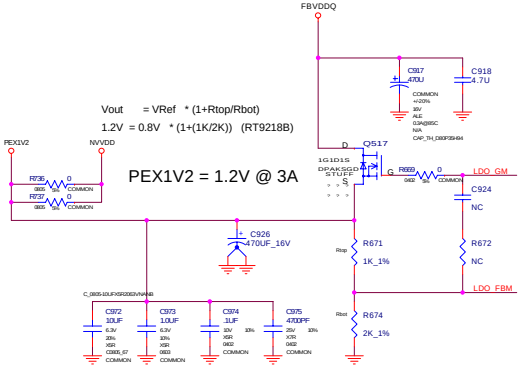
Vout = VRef * (1+Rtop/Rbot)

1.8V	= 0.8V * (1+(5k/4k))	(RT9218)
1.8V	= 0.8V * (1+(200/160))	(RT9218) Samsung MEM
2.003V	= 0.8V * (1+(200/133))	(RT9218) Infineon MEM default

Vout = VRef * (1+Rtop/Rbot)

1.2V = 0.8V * (1+(1K/2K)) (RT9218B)

PEX1V2 = 1.2V @ 3A

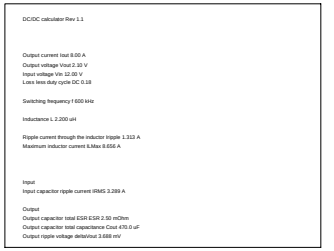


Net Name / MIN_LINE_WIDTH / VOLTAGE

Net Name	MIN_LINE_WIDTH		VOLTAGE
5V	16	3	5V
NVVDD	16	20	1.35V
12V_PEX	20	6	12V
PEX1V2	20	4	1.2V
12V_PEX_FLTRD	20	6	12V
FBVTT	20	1.5	FBVTT/2 V

DRIVE3_1V2	20	
UGATE_1	20	
LGATE_1	20	
UGATE_2	20	
LGATE_2	20	
NODE_1	20	
NODE_2	20	
12V_RR	10	
ISL12V_VCC	20	
COMP1_NVVDD	10	
FB1_NVVDD	10	
COMP2_5V	10	
FB2_5V	10	
FB3_1V2	10	
REFIN_5V	10	
ISL_REFOUT	10	
VREF_3V3	10	
FB3_RC	10	
BOOT_1	20	
BOOT_2	20	
FREQ_SET	10	
SS_NVVDD	10	
SS_5V	10	
SS_1V2	10	
UGATE_1_RG	20	
UGATE_2_RG	20	
COMP1_RC	10	
COMP2_RC	10	
NVVDD_RC	10	
5V_RC	10	
NODE_1_SNUB	20	
NODE_2_SNUB	20	
CLGATE_1	20	
BOOST	20	
5VBOOST	20	

FM1 FM2 FM3 FM4 FM5 FM6



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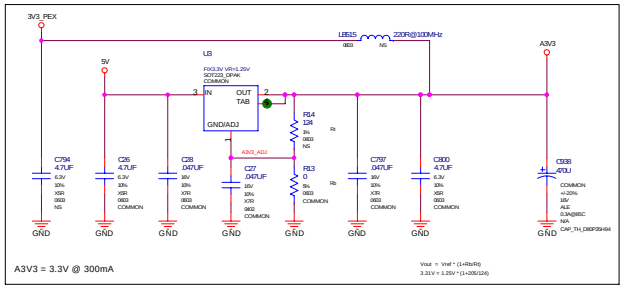
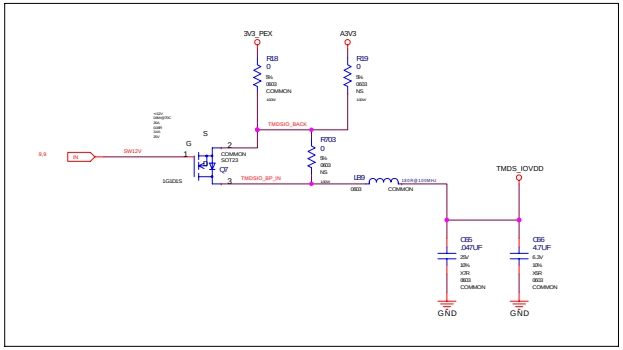
MS-V041			
Size: Custom	Document Number: NVVDD,PEX1V2,FBVDDQ		Rev: 0A
Date: Wednesday, November 29, 2006	Sheet 18 of 19		

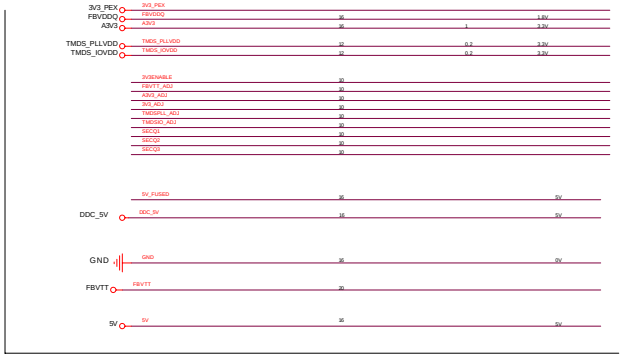
19 Others Power Supply (Linears)
A3V3,A2V5,TMDS_PLLVDD,TMDS_IOVDD

A3V3

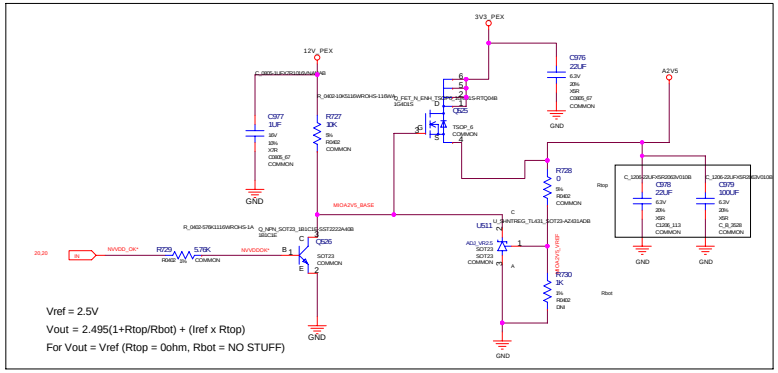


TMDS IO SUPPLY WITH BACKDRIVE PROTECTION

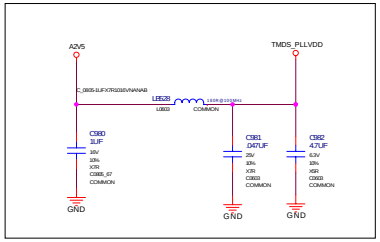




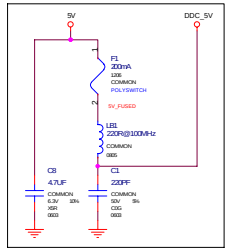
A2V5



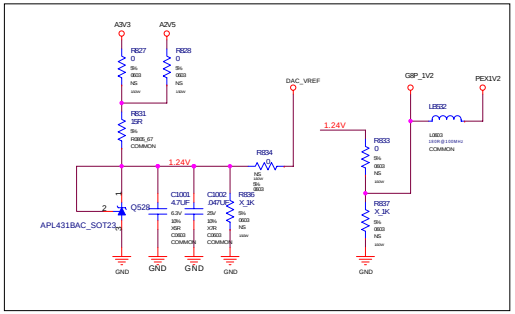
TMDS PLL Supply



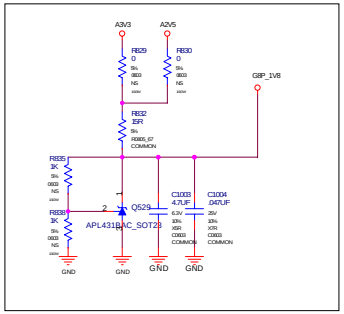
DDC 5V



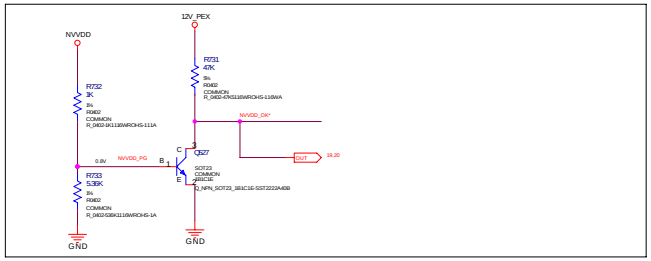
DAC_VREF & 1V2



1V8



Power Sequencing for FBVDDQ & A2V5



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MS-V041		
Size: Custom	Document Number: Others Power Supply (Linears)	Rev: 0A
Date: Thursday, November 30, 2006	Sheet 19 of 19	