電子類元件 零件承認書文件 CHECK LIST

零件廠商：UPI **品名規格：5V/12V Synchronous-Rectified Buck Controller**

技嘉料號：10TA1-601542-01R (uP1542SSU8)

項次	文件項目
Data Sheet 檢核項目	
1	DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2**
8	零件樣品 20PCS(Chipset 等高單價，至少 1PCS)
9	**主動電子零件承認基本調查表。註 3**
10	以上資料電子檔爲 PDF 檔，且是同 1 個 File
GPMS 綠色產品管理系統-物料管制文件檢核清單	
物料管制文件 1	GPMS 綠色產品管理系統：零件照片
物料管制文件 2	GPMS 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4**
物料管制文件 3	GPMS 綠色產品管理系統：Data Sheet
GPMS 綠色產品管理系統-MCD 表格	
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
其他文件 (僅適用電阻、電容類之系列元件)	
附件 1	危害物質測試報告 Test Report of Hazardous Substances。**註 5**
附件 2	元件調查表 Component Composition Table

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷爲雷射或油墨等
※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)
※ **3. 主動電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G***
※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”
※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指爲具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

主動電子零件承認基本調查表

一、原物料規格/來源			
項次	部位名稱/規格	材質	原物料來源產地
1	CHIP	Silicon	Taiwan
2	DIE ATTACH	Adhesives	Hong Kong
3	LEAD FRAME	Metal	Japan
4	BONDING WIRE	Metal	Singapore
5	MOLDING COMPOUND	Resin	Japan
6	Plating	Metal	Taiwan

二、晶圓廠					
項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	**Maxchip**	**Taiwan**	**8**	**100**	外包
2					

三、封裝廠				
項次	工廠名稱	生產產地	投產比率(%)	自有/外包
1	**GTK**	**Taiwan**	**100**	外包
2				

四、產能	
總產能(月/PCS)	可供技嘉產能(月/PCS)
2M	400K

※ 1. 晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉研發管理與 CE 單位，並更新文件

※ 2. 以上資訊欄位若有不足，可自行增加行數

5V/12V Synchronous-Rectified Buck Controller

General Description

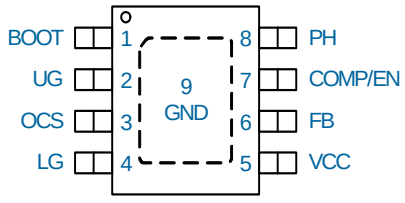
The uP1542 is a compact synchronous-rectified buck controller specifically designed to operate from 5V or 12V supply voltage and to deliver high quality output voltage as low as 0.6V for uP1542S/U (linear OCP).

The uP1542 adopts constant frequency, voltage mode control scheme, featuring easy-to-use, low external component count, and fast transient response. Fixed 300kHz operation provides an optimal level of integration to reduce size and cost of the power supply.

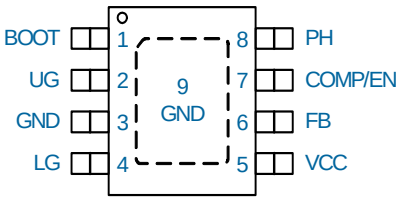
This controller integrates internal MOSFET drivers that support 12V+12V bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count.

Other features include internal soft start, over/under voltage protection, over current protection and shutdown function. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part is available in PSOP-8L and WDFN2x2-8L package.

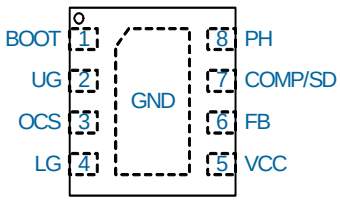
Pin Configuration



PSOP-8L (uP1542S)



PSOP-8L (uP1542Q/T/V)



WDFN2x2-8L (uP1542U)

Features

- **Operates from 5V or 12V Supply Voltage**
  - **3.3V to 12V V_{IN} Input Range**
  - **V_{REF} with 1.0% Accuracy:**
    uP1542S/U: 0.6V V_{REF}
    uP1542T/Q/V: 0.8V V_{REF}
- **Stand Alone Mode Operation**
- **Simple Single-Loop Control Design**
  - **Voltage-Mode PWM Control**
  - **Fast Transient Response**
  - **Fixed 300kHz Switching Frequency**
- **High-Bandwidth Error Amplifier**
  - **0% to 90% Duty Cycle**
- **Lossless, Adjuatable Over Current Protection**
  - **Uses Lower MOSFET $R_{DS(ON)}$**
  - **uP1542S/U: Linear OCP**
  - **uP1542T/Q/V: Fixed OCP**
- **Internal Soft Start**
- **Integrated Boot Diode**
- **PSOP-8L and WDFN2x2-8L Package**
- **RoHS Compliant and Halogen Free**

Applications

- **Power Supplies for Microprocessors or Subsystem Power Supplies**
- **Cable Modems, Set Top Boxes, and DSL Modems**
- **Industrial Power Supplies; General Purpose Supplies**
- **5V or 12V Input DC-DC Regulators**
- **Low-Voltage Distributed Power Supplies**

Ordering Information

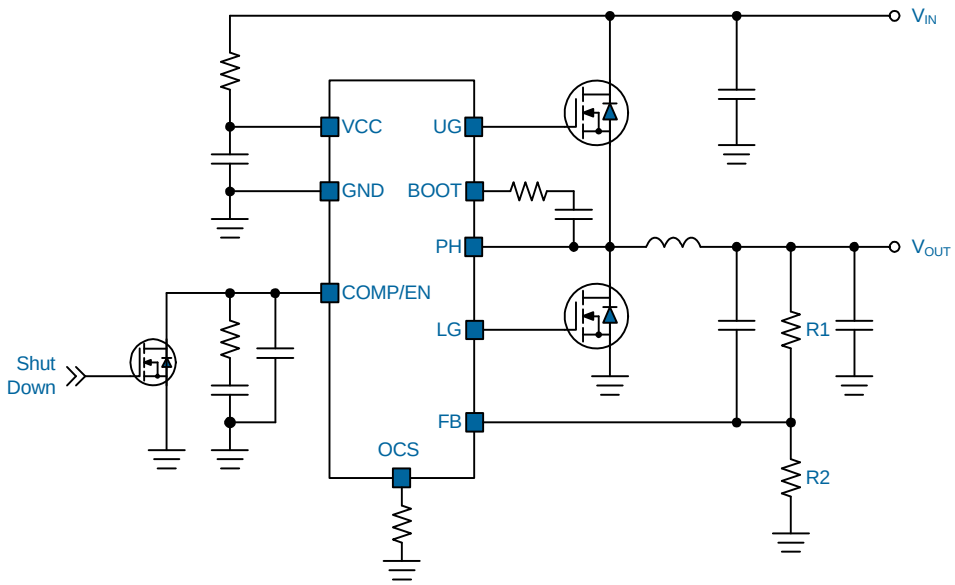
Order Number	Package Type	V_{REF}	Remark	Top Marking
uP1542SSU8	PSOP-8L	0.6V	linear OCP	uP1542S
uP1542TSU8		0.8V	fixed OCP@225mV	uP1542T
uP1542QSU8		0.8V	fixed OCP@300mV	uP1542Q
uP1542VSU8		0.8V	fixed OCP@375mV	uP1542V
uP1542UDD8	WDFN2x2-8L	0.6V	linear OCP	DJ

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

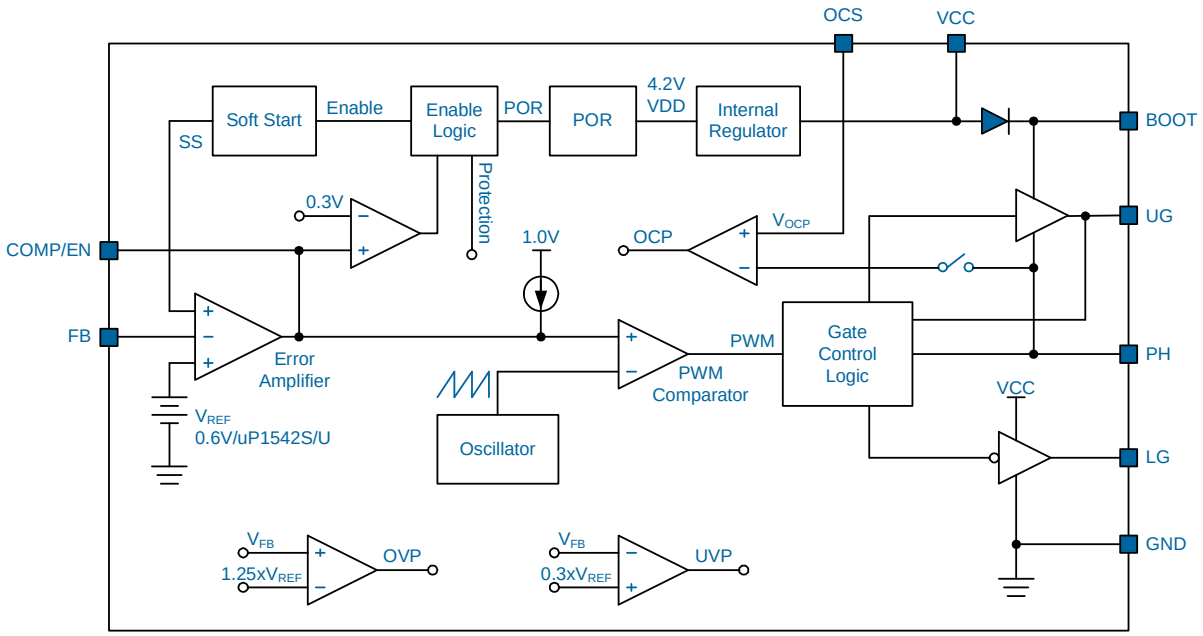
Functional Pin Description

Pin Name	Pin Function
BOOT	**Bootstrap Supply** for the floating upper gate driver. Connect the bootstrap capacitor between BOOT pin and the PH pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
UG	**Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
GND	**Ground.**
OCS	**Over Current Protection Setting.** Connect a resistor from this pin to GND to set the OCP level.
LG	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
VCC	**Supply Voltage.** This pin provides the bias supply for the uP1542 and the lower gate driver. Connect a well-decoupled 4.5V to 13.2V supply voltage to this pin. Ensure that a decoupling capacitor is placed near the IC.
FB	**Feedback Voltage.** This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage. Use this pin in combination with the COMP/EN pin to compensate the voltage control feedback loop of the converter.
COMP/EN	**Error Amplifier Output.** This is the output of the error amplifier and the non-inverting input of the PWM comparator. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter. Pulling COMP/EN to a level below 0.3V disables the controller and causes the oscillator to stop, the UG and LG outputs to be held low.
PH	**PHASE Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UG driver, and to monitor the voltage drop across the lower MOSFET for over current protection. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
Exposed Pad	**Ground.** The exposed pad is the dominate heat conducting path and should be well soldered to the PCB with multiple vias for optimal thermal performance.

Typical Application Circuit



Functional Block Diagram



Functional Description

The uP1542 is a compact synchronous-rectified buck controller specifically designed to operate from 5V or 12V supply voltage and to deliver high quality output voltage as low as 0.6V.

Supply Voltage

The VCC pin receives a well-decoupled 4.5V to 13.2V supply voltage to power the control circuit, the lower gate driver and the bootstrap circuit for the higher gate driver. A minimum 1uF ceramic capacitor is recommended to bypass the supply voltage. Place the bypassing capacitor physically near the IC.

An internal linear regulator regulates the supply voltage into a 4.2V voltage VDD for internal control logic circuit. No external bypass capacitor is required for filtering the VDD voltage.

The uP1542 integrates MOSFET gate drives that are powered from the VCC pin and support 12V+12V driving capability. A bootstrap diode is embedded to facilitate PCB design and reduce the total BOM cost. No external Schottky diode is required. Converters that consist of uP1542 feature high efficiency without special consideration on the selection of MOSFETs.

Note: The embedded bootstrap diode is not a Schottky diode having a 0.8V forward voltage. External Schottky diode is highly recommended if the VCC voltage is expected to be lower than 5.0V. Otherwise the bootstrap diode may be too low for the device to work normally.

Power On Reset and Chip Enable

A power on reset (POR) circuitry continuously monitors the supply voltage at VCC pin. Once the rising POR threshold is exceeded, the uP1542 sets itself to active state and is ready to accept chip enable command. The rising POR threshold is typically 4.2V at VCC rising.

The COMP/EN is a multifunctional pin: control loop compensation and chip enable as shown in Figure 1. An Enable Comparator monitors the COMP/EN pin voltage for chip enable. A signal level transistor is adequate to pull this pin down to ground and shut down the uP1542. An 80uA current source charges the external compensation network with 1.0V ceiling when this pin is released. If the voltage at COMP/EN pin exceeds 0.3V, the uP1542 initiates its softstart cycle.

The 80uA current source keeps charging the COMP pin to its ceiling until the feedback loop boosts the COMP pin higher than 0.8V according to the feedback signal. The current source is cut off when V_{COMP} is higher than 1.0V during normal operation.

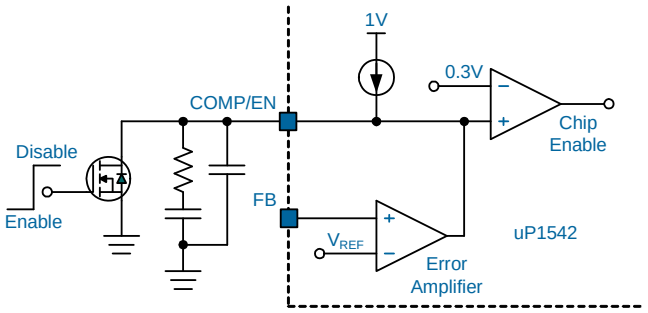


Figure 1. Chip Enable Function

Soft Start

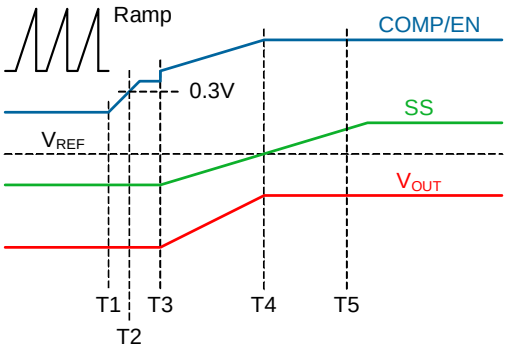
A built-in Soft Start is used to prevent surge current from power supply input during turn on (referring to the Functional Block Diagram). The error amplifier is a three-input device. Reference voltage V_{REF} or the internal soft start voltage SS whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. SS internally ramps up to VCC and the output voltage will follow the SS signal and ramp up smoothly to its target level.

The SS signal keeps ramping up after it exceeds the reference voltage V_{REF}. However, the reference voltage V_{REF} takes over the behavior of error amplifier after SS > V_{REF}. When the SS signal climb to 1.3 x V_{REF}, the uP1542 claims the end of softstart cycle and enables the over and under voltage protection of the output voltage.

Figure 2 shows a typical start up interval for uP1542 where the COMP/SD pin has been released from a grounded (system shutdown) state.

The internal 80uA current source starts to charge the compensation network after the COMP/SD pin is released from grounded at T1. The COMP/SD exceeds 0.3V and enables the uP1542 at T2. The COMP/SD continues ramping up and stays at 1V before the SS starts ramping up at T3. The uP1542 initializes itself such as current limit level setting (see the relative section) during the time interval between T2 and T3. The output voltage follows the internal SS and ramps up to its final level during T3 and T4. At T4, the reference voltage V_{REF} takes over the behavior of the error amplifier as the internal SS crosses V_{REF}. The internal SS keeps ramping up and reaches 1.3 x V_{REF} at T5, where the uP1542 asserts the end of softstart cycle.

Functional Description



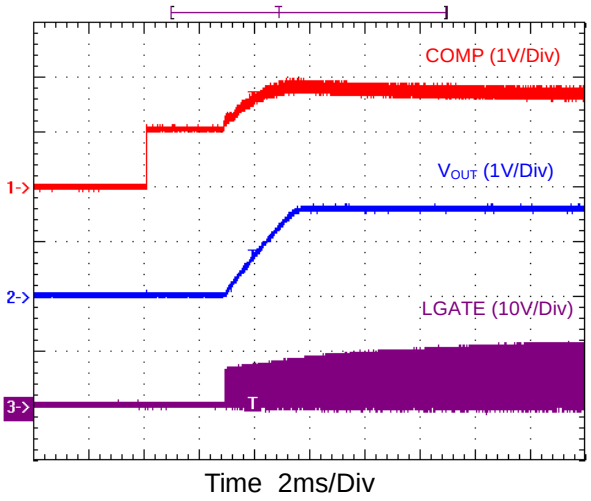


Figure 2. Softstart Behavior of uP1542.

Power Input Detection

The uP1542 detects PH voltage for the present of power input when the UG turns on the first time. If the PH voltage does not exceed 1.0V when the UG turns on, the uP1542 asserts that power input in not ready and stops the softstart cycle. Another softstart cycle is initiate after a 6ms time delay. Figure 4 shows the start up interval where V_{IN} does not present initially.

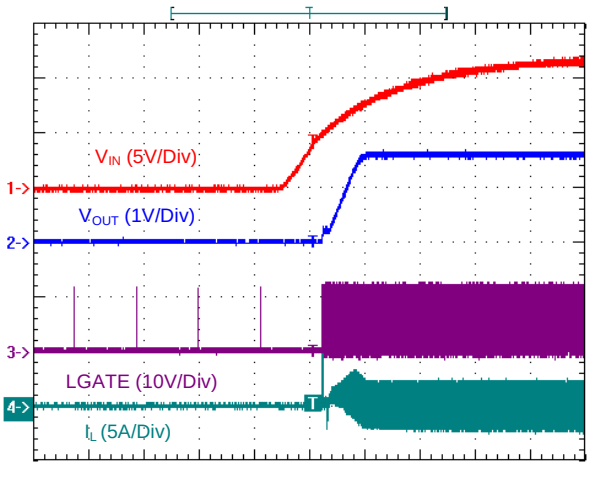


Figure 3. Softstart where V_{IN} does not Present Initially.

Output Voltage Selection

The output voltage can be programmed to any level between the reference voltage V_{REF} up to the 90% of V_{IN} supply. The lower limitation of output voltage is caused by the internal reference. The upper limitation of the output voltage is caused by the maximum available duty cycle (90% typical). This is to leave enough time for over current detection. Output voltage out of this range is not allowed.

An voltage divider sets the output voltage (refer to the Typical Application Circuit on page 3 for detail). In real applications, choose R1 in 1kΩ ~ 10kΩ range and choose appropriate R2 according to the desired output voltage.

$$V_{OUT} = V_{REF} \times \frac{R1+R2}{R2}$$

Over Current Protection (OCP)

The uP1542 detects voltage drop across the lower MOSFET (V_{PHASE}) for over current protection when it is turned on. If V_{PHASE} is lower than the user-programmable voltage V_{OCP}, the uP1542 asserts OCP and shuts down the converter. The OCP level can be programmed by OCS pin (uP1542S/U) or fixed at 300mV (uP1542Q).

The uP1542 sources a 20uA current source out of OCS pin. Connect resistor R_{OCS} at OCS pin to create voltage level V_{OCS} for OCP setting. The maximum of V_{OCP} should not be larger than 375mV.

$$V_{OCS} = \frac{20uA \times R_{OCS}}{4}$$

$$V_{OCP} = V_{OCS}$$

$$I_{OCP} = \frac{V_{OCP}}{R_{DS(ON)}} \quad (A)$$

For example:

If V_{OCP} = 375mV, and $R_{DS(ON)}$ = 10mΩ, the I_{OCP} will be 37.5A.

If V_{OCP} = 225mV, and $R_{DS(ON)}$ = 10mΩ, the I_{OCP} will be 22.5A.

Over Voltage and Under Voltage Protection

The uP1542 asserts over voltage protection if the feedback voltage V_{FB} is higher than 125% of reference voltage V_{REF}. The uP1542 asserts under voltage protection if the feedback voltage V_{FB} is lower than 30% of reference voltage V_{REF} after soft start end. The uP1542 turns off both higher and lower gate drivers upon UVP and turns on lower gate driver upon OVP. Both UVP and OVP are latch-off type and can be reset by POR or toggling the COMP/EN pin.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC ---------- -0.3V to +15V
BOOT to PH ---------- -0.3V to +15V
PH to GND
- DC ---------- -0.7V to 15V
- < 200ns ---------- -8V to 30V

BOOT to GND
- DC ---------- -0.3V to VCC + 15V
- < 200ns ---------- -0.3V to 42V

UG to PH
- DC---------- -0.3V to (BOOT - PH +0.3V)
- <200ns ---------- -5V to (BOOT - PH + 0.3V)

LG to GND
- DC ---------- -0.3V to + (VCC + 0.3V)
- <200ns ---------- -5V to VCC + 0.3V

Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- PSOP-8L θ_{JA} ---------- 47°C/W
- WDFN2x2-8L θ_{JA} ---------- 155°C/W
- PSOP-8L θ_{JC} ---------- 17.9°C/W
- WDFN2x2-8L θ_{JC} ---------- 20°C/W

Power Dissipation, P_D @ T_A = 25°C
- PSOP-8L ---------- 2.13W
- WDFN2x2-8L ---------- 0.65W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- +4.5V to 13.2V

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Voltage	V_{CC}		4.5	--	13.2	V
Supply Current	I_{CC}	UG and LG Open, V_{CC} = 12V, Switching	--	3	--	mA
Quiescent Supply Current	I_{CC_Q}	V_{FB} = V_{REF} + 0.1V, No Switching	--	1.3	--	mA
Power Input Voltage	V_{IN}		3.0	--	13.2	V
Power On Reset						
POR Threshold	V_{CCRTH}	V_{CC} rising	4.0	4.2	4.4	V
POR Hysteresis	V_{CCHYS}		--	0.5	--	V
Switching Frequency						
Free Running Frequency	f_{OSC}		270	300	330	kHz
Ramp Amplitude	ΔV_{OSC}	V_{CC} = 12V	--	3	--	V_{P-P}
Reference Voltage						
Internal Reference Voltage Accuracy	V_{FB}	uP1542S/U	0.594	0.60	0.606	V
		uP1542T/Q/V	0.792	0.800	0.808	V
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	55	70	--	dB
Gain-Bandwidth Product	GBW	Guaranteed by Design	--	10	--	MHz
Slew Rate	SR	Guaranteed by Design	3	6	--	V/us
Transconductance			600	800	1000	uA/V
Output Source Current		V_{FB} < V_{REF}	80	120	--	uA
Output Sink Current		V_{FB} > V_{REF}	80	120	--	uA
Input Offset Voltage			-1.0	0	1.0	mV
Input Leakage Current			--	0.1	1.0	nA
PWM Controller Gate Drivers						
Upper Gate Source	R_{UG_SRC}	I_{UG} = 100mA Source	--	3	5	Ω
Upper Gate Sink	R_{UG_SNK}	I_{UG} = 100mA Sink	--	1.5	3	Ω
Lower Gate Source	R_{LG_SRC}	I_{UG} = 100mA Source	--	3	5	Ω
Lower Gate Sink	R_{LG_SNK}	I_{UG} = 100mA Sink	--	1	2	Ω

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM Controller Gate Drivers						
PH Falling to LG Rising Delay		V_{PH} < 1.2V to V_{LG} > 1.2V	--	30	--	ns
LG Falling to UG Rising Delay		V_{LG} < 1.2V to (V_{UG} - V_{PH}) > 1.2V	--	30	--	ns
Minimum Duty Cycle			--	0	--	%
Maximum Duty Cycle			85	90	95	%
Soft Start						
Soft Start Time		from COMP/EN released to V_{OUT} in regulation	--	2.5	--	ms
Protection						
Under Voltage Protection	V_{FB_UVP}	Percentage of V_{REF}	--	30	--	%
Over Voltage Protection	V_{FB_OVP}	Percentage of V_{REF}	--	125	--	%
Over Voltage Protection Delay			--	20	--	us
Over Current Threshold	V_{PH}	uP1542T	--	-225	--	mV
		uP1542Q	--	-300	--	
		uP1542V	--	-375	--	
OCP Programmable Range	V_{OCP}	uP1542S/U	-375	--	-100	mV
OCS Source Current for OCP Setting	I_{OCS}		--	20	--	uA
OCP Delay Time			--	3.33	--	us
Disable Threshold	$V_{COMP/EN}$		0.25	0.3	0.35	V
Over Temperature Protection			--	150	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Application Information

Component Selection Guidelines

The selection of external component is primarily determined by the maximum load current and begins with the selection of power MOSFET switches. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its capability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specification.

Power MOSFET Selection

The uP1542 requires two external N-channel power MOSFETs for upper (controlled) and lower (synchronous) switches. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, maximum current $I_{DS(MAX)}$, gate supply requirements, and thermal management requirements.

The gate drive voltage is supplied by VCC pin that receives 4.5V~13.2V supply voltage. When operating with a 7~13.2V power supply for VCC, a wide variety of NMOSFETs can be used. Logic-level threshold MOSFET should be used if the input voltage is expected to drop below 7V. Caution should be exercised with devices exhibiting very low $V_{GS(ON)}$ characteristics. The shoot-through protection present aboard the uP1542 may be circumvented by these MOSFETs if they have large parasitic impedances and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on. Also avoid MOSFETs with excessive switching times; the circuitry is expecting transitions to occur in under 30ns or so.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components: conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty cycle. Since the uP1542 is operating in continuous conduction mode, the duty cycles for the MOSFETs are:

$$D_{UP} = \frac{V_{OUT}}{V_{IN}};\ D_{LOW} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{UP} = I_{OUT}^2 \times R_{DS(ON)} \times D_{UP} + 0.5 \times I_{OUT} \times V_{IN} \times T_{SW} \times f_{OSC}$$

$$P_{LOW} = I_{OUT}^2 \times R_{DS(ON)} \times D_{LOW}$$

where T_{SW} is the combined switch ON and OFF time.

Both MOSFETs have I^2R losses and the upper MOSFET includes an additional term for switching losses, which are largest at high input voltages. The lower MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short-circuit or at high input voltage. These equations assume linear voltage current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode.

Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

The gate-charge losses are mainly dissipated by the uP1542 and don't heat the MOSFETs. However, large gate charge increases the switching interval, T_{SW} that increases the MOSFET switching losses. The gate-charge losses are calculated as:

$$P_{G\_C} = V_{CC} \times (V_{CC} \times (C_{ISS\_UP} + C_{ISS\_LO}) + V_{IN} \times C_{RSS\_UP}) \times f_{OSC}$$

where C_{ISS_UP} is the input capacitance of the upper MOSFET, C_{ISS_LOW} is the input capacitance of the lower MOSFET, and C_{RSS_UP} is the reverse transfer capacitance of the upper MOSFET. Make sure that the gate-charge loss will not cause over temperature at uP1542, especially with large gate capacitance and high supply voltage.

Output Inductor Selection

Output inductor selection usually is based on the considerations of inductance, rated current, size requirements and DC resistance (DCR).

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 20% of $I_{OUT(MAX)}$.

There is another tradeoff between output ripple current/ voltage and response time to a transient load. Increasing the value of inductance reduces the output ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

Application Information

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Input Capacitor Selection

The synchronous-rectified Buck converter draws pulsed current with sharp edges from the input capacitor, resulting in ripples and spikes at the input supply voltage. Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs to avoid the stray inductance along the connection trace.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck converter is calculated as:

$$I_{IN(RMS)} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{IN(REMS)} = I_{OUT(RMS)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can also be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Output Capacitor Selection

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The equivalent ripple current into the output capacitor is half of the inductor ripple current while the equivalent frequency is double of phase operation frequency due to two phase operation The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} = \frac{\Delta I_L}{2}\left(ESR + \frac{1}{16 \times f_{OSC} \times C_{OUT}}\right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes.

Bootstrap Capacitor Selection

An external bootstrap capacitor C_{BOOT} connected to the BOOT pin supplies the gate drive voltage for the upper MOSFET. This capacitor is charged through the internal

diode when the PH node is low. When the upper MOSFET turns on, the PH node rises to V_{IN} and the BOOT pin rises to approximately V_{IN} + V_{CC}. The boot capacitor needs to store about 100 times the gate charge required by the upper MOSFET. In most applications 0.47µF to 1µF, X5R or X7R dielectric capacitor is adequate.

Feedback Loop Compensation

Figure 5 highlights the voltage-mode control loop for a synchronous-rectified buck converter consisting of uP1542. The control loop includes a compensator and a modulator, where the modulator consists of the PWM comparator, the power stage amplifier and the output filter; the compensator consists of the error amplifier and compensating network. A well-designed feedback loop tightly regulates the output voltage (V_{OUT}) to the reference voltage V_{REF} with fast response to load/line transient and good stability. The goal of the compensation network is to provide and the highest 0dB crossing frequency and adequate phase margin (greater than 45 degrees). It is also recommended to manipulate loop frequency response that its gain crosses over 0dB at a slope of -20dB/dec.

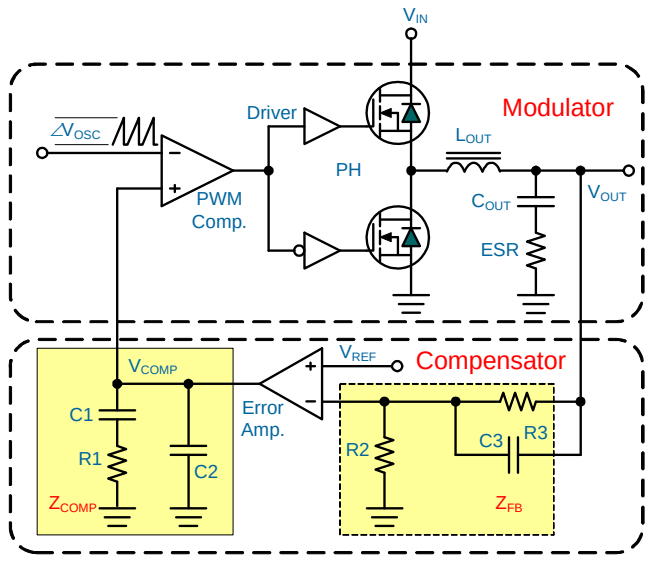


Figure 5. Voltage Control Loop Using uP1542.

Modulator Break Frequency Equations

The error amplifier output (V_{COMP}) is compared with the oscillator (OSC) sawtooth waveform to provide a pulse-width modulated (PWM) waveform with an amplitude of V_{IN} at the PH node. The PWM waveform is smoothed by the output filter (L_{OUT} and C_{OUT}). The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC Gain and the output filter (L_{OUT} and C_{OUT}), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter expressed as:

$$F_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitor. Note that this requires that the output capacitor should have enough ESR to satisfy stability requirements as described in the later sections. The ESR zero of the output capacitor expressed as:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

Figure 6 illustrates frequency response of a typical modulator using uP1542.

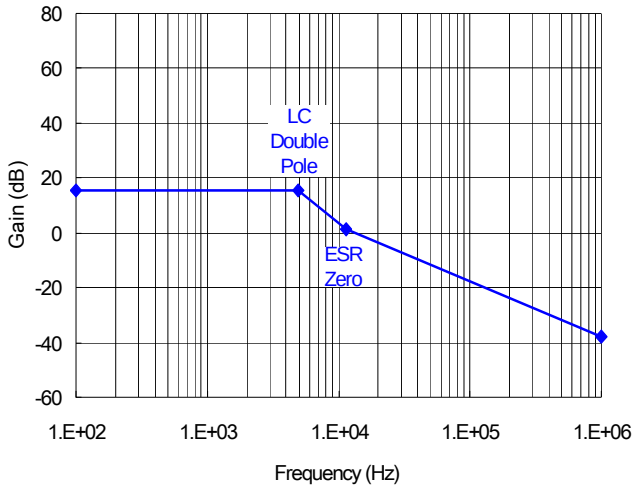


Figure 6. Frequency Response of Modulator.

2) Compensator Frequency Equations

The uP1542 adopts an operational transconductance amplifier (OTA) as the error amplifier as shown in Figure 7.

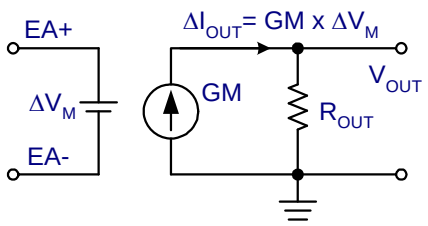


Figure 7. Operational Transconductance Amplifier.

The ***transconductance*** is defined as:

$$GM = \frac{\Delta I_{OUT}}{\Delta V_M}$$

where ΔV_M = (EA+) - (EA-); ΔI_{OUT} = E/A output current.

Figure 8 illustrates a type II compensation network using OTA. The compensation network consists of the error amplifier and the impedance networks Z_{FB} and Z_{COMP}.

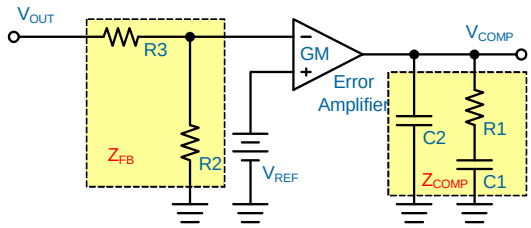


Figure 8. Type II Compensation Network Using OTA.

The compensator transfer function is the small-signal transfer function of V_{COMP}/V_{OUT}. This function is dominated by a Mid-Band Gain and compensation network Z_{COMP}, with a pole at F_{P1} and a zero at F_{Z1}. The Mid-Band Gain of the compensation is expressed as:

$$Mid\_Band\_Gain = \frac{R2}{R2 \times R3} \times R1 \times GM$$

The equations below relate the compensation network's pole and zero to the components (R1, C1, and C2) in Figure 9.

$$F_{P1} = \frac{1}{2\pi \times R1 \times (\frac{C1 \times C2}{C1 + C2})}; \quad F_{Z1} = \frac{1}{2\pi \times R1 \times C1}$$

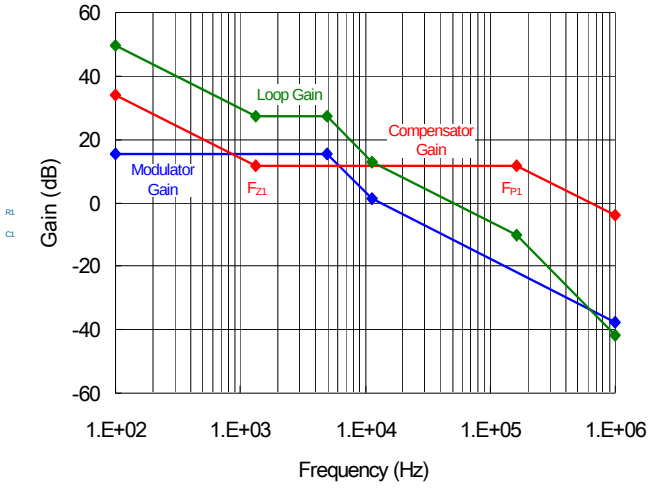


Figure 9. Frequency Response of Type II Compensation.

Figure 10 shows the DC-DC converter's gain vs. frequency. Careful design of Z_{COMP} and Z_{FB} provides tight regulation and fast response to load/line transient with good stability. Follow the guidelines for locating the poles and zeros of the compensation network.

1. Pick Mid-Band Gain (R1) for desired converter bandwidth.
2. Place Zero (C1) below LC double pole (~25% F_{LC}).
3. Place Pole (C2) at half the switching frequency.
4. Check gain against error amplifier open loop gain.
5. Estimate phase margin - repeat if necessary.

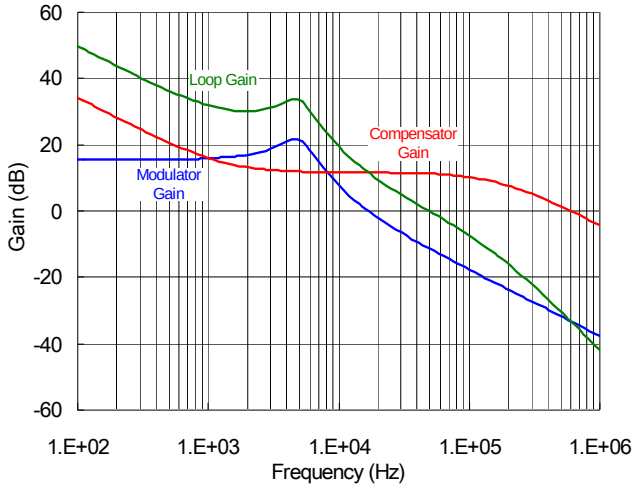


Figure 10. Frequency Response of Type II Compensation.

Design Example

As a design example, take a power supply with the following specifications:

V_{IN} = 10.8V to 13.2V (12V nominal), V_{OUT} = 1.2V ±5%, $I_{OUT(MAX)}$ = 20A, f_{OSC} = 300kHz/200kHz, ΔV_{OUT} = 20mV, bandwidth = 50kHz.

1.) Power Component Selection

First, choose the inductor for about 20% ripple current at the maximum V_{IN}:

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

$$\Delta I_L = 20A \times 20\% = \frac{1}{300kHz \times L_{OUT}} \times 1.2V \times (1 - \frac{1.2V}{13.2V})$$

$$L_{OUT} = 0.9\ uH$$

Selecting a standard value of 1.0uH results in a maximum ripple current of 3.6A.

Choose two 1000uF capacitors with 10mΩ ESR in parallel to yield equivalent ESR = 5mΩ. The output ripple voltage is about 18mV accordingly. An optional 22uF ceramic output capacitor is recommended to minimize the effect of ESL in the output ripple.

The modulator DC gain and break frequencies are calculated as:

$$DC\ Gain = 20 \times \log(\frac{V_{IN}}{\Delta V_{OSC}}) = 20 \times \log(\frac{12}{1.8}) = 16.5dB$$

$$F_{LC} = \frac{1}{2\pi\sqrt{1\times10^{-6} \times 2000 \times 10^{-6}}} = 3.56kHz$$

$$F_{ESR} = \frac{1}{2\pi \times 5 \times 10^{-3} \times 2000 \times 10^{-6}} = 16kHz$$

2.) Compensation

Select R2 = 10kΩ and R3 = 5kΩ to set output voltage as 1.2V. R2 and R3 do not affect the compensation, 1kΩ ~ 10kΩ is adequate for the application.

The modulator gain at zero-crossing frequency (50kHz) is calculated as -19.5dB. This demands a compensator with mid-band gain as 19.5dB. Select R1 as:

$$R1 = \frac{10^{(19.5/20)} \times V_{OUT}}{GM \times V_{REF}} = 17.7k\Omega$$

Select C1 = 10nF to place F_{Z1} = 0.9kHz, about one forth of the LC double pole.

Select C2 = 68pF to place F_{P1} = 133kHz, about half of the switching frequency.

Figure 11 shows the result loop gain vs. frequency relation.

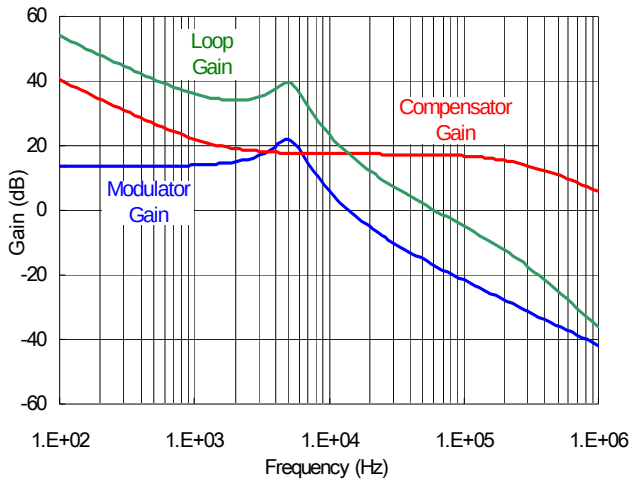


Figure 11. Gain vs. Frequency for the Design Example.

Type III Compensation

The ESR zero plays an important role in type II compensation. Output capacitors with low ESR and small capacitance push the ESR zero to high frequency band. If the ESR zero is ten times higher than the LC double pole, the double pole may cause the loop phase close to 180° and make the control loop unstable. A type II compensation cannot stabilize the loop since it has only one zero.

A type III compensation network as shown in Figure 12 that features 2 poles and 2 zeros is necessary for such applications where ESR zero is far away from the LC double pole. Adding a feedforward capacitor C3 on original type II compensation network introduces an additional pole-zero pair (Z2 and P2) as illustrated in Figure 13. The new pole-zero pair are expressed as:

$$Z2 = \frac{1}{2\pi \times R3 \times C3};\ P2 = \frac{1}{2\pi \times C3 \times (R2 \times R3)/(R2 + R3)}$$

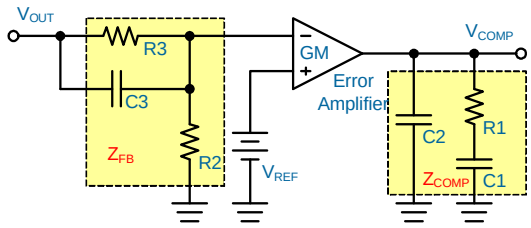


Figure 12. Type III Compensation Network.

While the Mid-Band Gain remains unchanged, the additional pole-zero pair causes a gain boost at the flat gain region. The gain-boost is limited by the ratio (R1 +R2)/ R2. Figures 14 shows the DC-DC converter's gain vs. frequency.

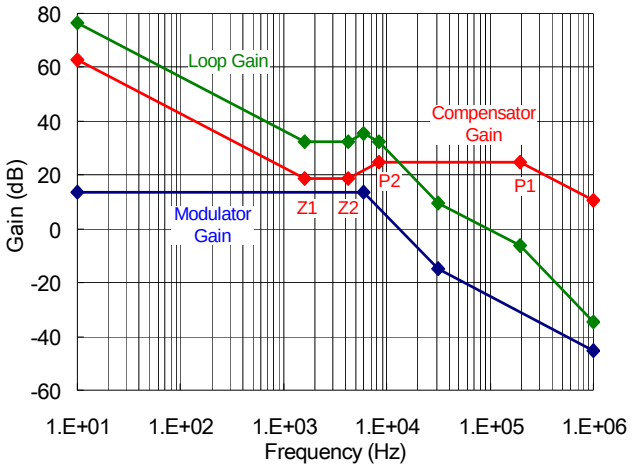


Figure 13. Loop Gain of Type III Compensation Network.

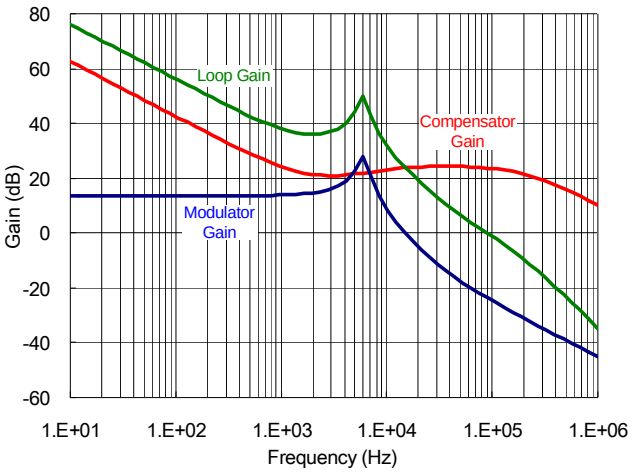


Figure 14. Frequency Response of Type III Compensation.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD}x(ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value.

During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

PCB Layout Considerations

High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another in a synchronous-rectified buck converter causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement layout and printed circuit board design minimizes the voltage spikes induced in the converter.

Follow the layout guidelines for optimal performance of uP1542.

1 The upper and lower MOSFETs turn on/off and conduct pulsed current alternatively with high slew rate transition. Any inductance in the switched current path generates a large voltage spike during the switching. The interconnecting wires indicated by red heavy lines conduct pulsed current with sharp transient and should be part of a ground or power plane in a printed circuit board to minimize the voltage spike. Make all the connection the top layer with wide, copper filled areas.

2 Place the power components as physically close as possible.

2.1 Place the input capacitors, especially the high frequency ceramic decoupling capacitors, directly to the drain of upper MOSFET ad the source of the lower MOSFET. To reduce the ESR replace the single input capacitor with two parallel units

2.2 Place the output capacitor between the converter and load.

3 Place the uP1542 near the upper and lower MOSFETs with UG and LG facing the power components. Keep the components connected to noise sensitive pins near the uP1542 and away from the inductor and other noise sources.

4 Use a dedicated grounding plane and use vias to ground all critical components to this layer. The ground plane layer should not have any traces and should be as close as possible to the layer with power MOSFETs. Use an immediate via to connect the components to ground plane including GND of uP1542. Use several bigger vias for power components.

5 Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes to maintain good voltage filtering and to keep power losses low. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

6 The PH node is subject to very high dV/dt voltages. Stray capacitance between this island and the surrounding circuitry tend to induce current spike and capacitive noise coupling. Keep the sensitive circuit away from the PH node and keep the PCB area small to limit the capacitive coupling. However, the PCB area should be kept moderate since it also acts as main heat convection path of the lower MOSFET.

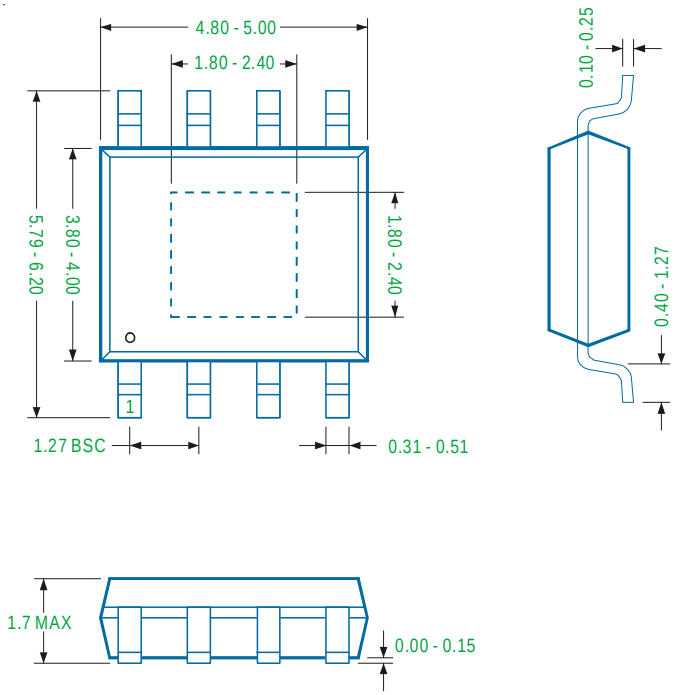
7 The uP1542 sources/sinks impulse current with 2A peak to turn on/off the upper and lower MOSFETs. The connecting trance between the controller and gate/source of the MOSFET should be wide and short to minimize the parasitic inductance along the traces.

8 Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component.

9 Provide local VCC decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as possible to the BOOT and PH pins.

Package Information

PSOP - 8L

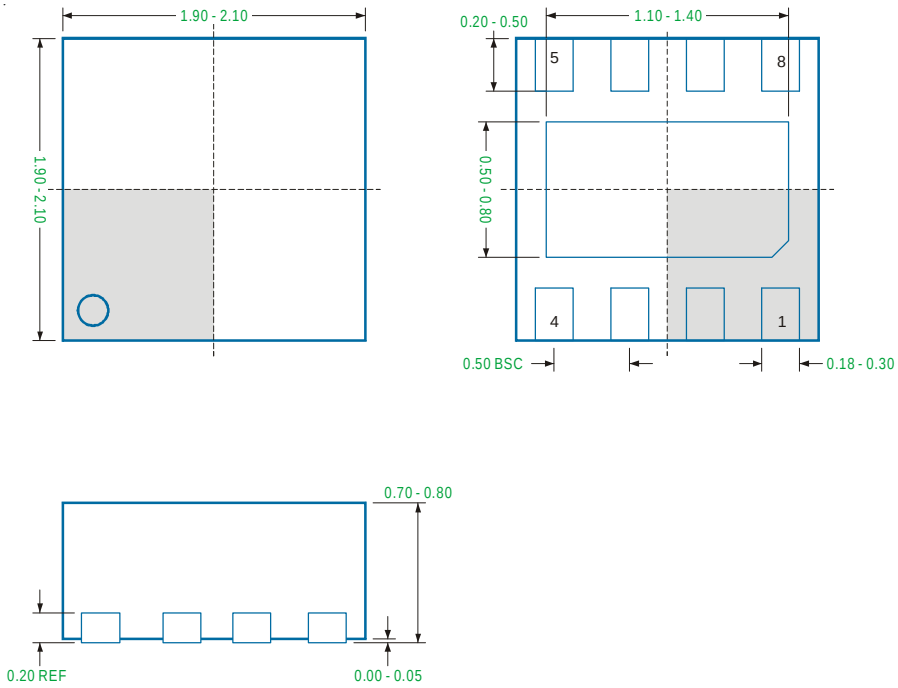


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

WDFN2x2 - 8L



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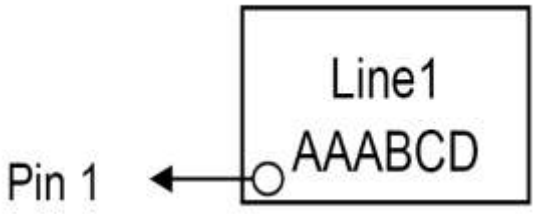
物質組成成份表
Materials Composition Declaration(MCD) Form

Part Number	uP1542SSU8
PKG Type	SOP-8L

Materials Composition Spreadsheet

Material	Weight(%)	Composition	CAS No.	Ratio(%)	Weight(mg)	PPM
Die	1.86%	Si	7440-21-3	99.6416%	1.334400307	18533
		W	7440-33-7	0.041%	0.000549072	8
		Al	7429-90-5	0.2825%	0.00378324	53
		Ti	7440-32-6	0.0349%	0.000467381	6
Lead frame	28.50%	Copper	7440-50-8	94.8875%	19.470915	270429
		Iron	7439-89-6	2.35%	0.48222	6698
		Lead	7439-92-1	0.005%	0.001026	14
		Phosphorus	7723-14-0	0.0825%	0.016929	235
		Zinc	7440-66-6	0.175%	0.03591	499
		Silver	7440-22-4	2.5%	0.513	7125
Epoxy	0.84%	Silver	7440-22-4	74.75%	0.452088	6279
		Epoxy Resin A	9003-36-5	4%	0.024192	336
		Epoxy Resin B	Trade secret	6%	0.036288	504
		Diluent A	Trade secret	4%	0.024192	336
		Diluent B	Trade secret	5%	0.03024	420
		Diluent C	3101-60-8	1%	0.006048	84
		Hardener	Trade secret	5%	0.03024	420
		Dicyandiamide	461-58-5	0.25%	0.001512	21
Bonding Wire	0.22%	Copper	7440-50-8	100%	0.1584	2200
Molding Compound	66.18%	Silica Fused	60676-86-0	81%	38.596176	536058
		Epoxy Resin	Trade secret	8%	3.811968	52944
		Epoxy, Cresol Novolac	29690-82-2	2.5%	1.19124	16545
		Phenol Resin	Trade secret	8%	3.811968	52944
		Carbon Black	1333-86-4	0.5%	0.238248	3309
Plating	2.40%	Pure tin	7440-31-5	100%	1.728	24000
Total package weight(mg)					72	

Top Marking Rule



Line 1 : Product Code

Part No.	Product Code
uP1542SSU8	**uP1542S**

Line 2 :

AAA - uPI internal trace code

BCD - Date Code, rules as below:

B：Last one of western calendar year (0~9), ex. 2007=7, 2008=8

C：Month

Month	Code	Month	Code	Month	Code	Month	Code
Jan	1	Apr	4	Jul	7	Oct	A
Feb	2	May	5	Aug	8	Nov	B
Mar	3	Jun	6	Sep	9	Dec	C

D：Date

Date	Code	Date	Code	Date	Code	Date	Code
1	1	9	9	17	H	25	S
2	2	10	A	18	J	26	T
3	3	11	B	19	K	27	U
4	4	12	C	20	L	28	V
5	5	13	D	21	M	29	W
6	6	14	E	22	N	30	X
7	7	15	F	23	P	31	Y
8	8	16	G	24	R		

產品可靠度驗證報告

Product Reliability Qualification Report

Product: uP1542

Approved by Date:	Terry Hung 2012/08/28	Apply by Date:	B.Y. Hsieh 2012/08/28

1. Purpose:

1.1 The reliability summary report is included the ESD, Latch up, product qualification and package qualification test.

1.2 To ensure the product meets uPI's quality specification.

1.3 To establish a test schedule for quality control and evaluate the reliability performance.

2. Product Information:

2.1 Part No.: uP1542

2.2 Wafer Manufacture: MAX

2.3 Package type: PSOP-8

3. Operation Life Test (OLT)

3.1 Test information

- Test condition : **T_A=125℃, V_{DD}=15 V**
- Readout time : **168 / 1000 hours**
- Sample size : **77 ea**

3.2 Test results

Test Item	Test Time	S/S	Fail	Failure Rate (λ)
OLT	168	77	0	FIT= 77 , MTTF=13,025,802 (Confidence Level 90%) FIT = 31 , MTTF=32,733,078 (Confidence Level 60%)
OLT	1000	77	0	FIT= 13 , MTTF=77,534,533 (Confidence Level 90%) FIT = 5 , MTTF=194,839,751 (Confidence Level 60%)

3.3 Reference Documents:

3.3.1 MIL-STD-19500E (LTPD Sampling Plans)

3.3.2 MIL-STD-883D 1005.8 (OLT)

4. ESD and Latch-up Test

4.1 ESD Test item and result

Test Item	ESD HBM	ESD MM
Test Condition	HBM: +- 2000 V	MM : +- 200V
Sample Size	3 units	3 units
Test Reference Standard	JEDEC STD JESD22-A114	JEDEC EIA/ JESD22-A115
Test Result	**Pass**	**Pass**

4.2 Latch-up Test item and result

Test Item	Latch-up Vcc	Latch-up I/O
Test Condition	Vstress (Latch-Up Vcc)	Istress (Latch-Up I/O)
Sample Size	3 units	3 units.
Test Reference Standard	JEDEC JESD78A	JEDEC JESD78A
Test Result	**Pass**	**Pass**

4.3 Reference Documents:

4.3.1 JEDEC EIA/JESD22-A114-B (Human Body Model,HBM)

4.3.2 JEDEC EIA/JESD22-A115-A (Machine Model, MM)

4.3.3 JEDEC EIA/JESD78 A(Latch-up)

5. Package Qualification Test

5.1 Test items and condition:

a. Moisture soak: MSL=3, 30°C, 60% RH, 192 hrs
b. IR reflow: 260°C ,3 cycles
c. PCT: 121°C,100%RH,19.7 psia,168 hrs
d. HAST:130°C, 85%RH,33.5 psia, 96 hrs
e. HTST: 150°C, 1000 hrs
f. THT: 85°C, 85%RH, 1000 hrs
g. TCT: -65°C ~150°C, 500 cycles

5.2 Test Results:

Test Procedure	Sample Size	Visual Insp. rej/s.s	Function Test rej/s.s	Judgment
Before Precondition	390EA	0/390	0/390	PASS
After Precondition	390EA	0/390	0/390	PASS
PCT 168hrs	77EA	0/77	0/77	PASS
TCT 500cycles	77EA	0/77	0/77	PASS
HAST 96hrs	77EA	0/77	0/77	PASS
HTST 1000hrs	77EA	0/77	0/77	PASS
THT 1000hrs	77EA	0/77	0/77	PASS

5.3 Reference Documents:

5.3.1 IPC JEDEC J-STD-020C Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

5.3.2 IPC JEDEC J-STD-033B Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

5.3.3 JESD22-A104C Temperature Cycling

5.3.4 EIA JESD22-A101-B Steady State Temperature Humidity Bias Life Test

5.3.5 JESD22-A110-B Highly-Accelerated Temperature and Humidity Stress Test

(HAST)

5.3.6 JESD22-A103C High Temperature Storage Life

5.3.7 JESD22-A113C Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

5.3.8 JESD22-A102-C Accelerated Moisture Resistance-Unbias

SOP/MSOP & SOT Package Series

Definition:

TSSOP/SOP: Thin-Shrink/Small Outline Package

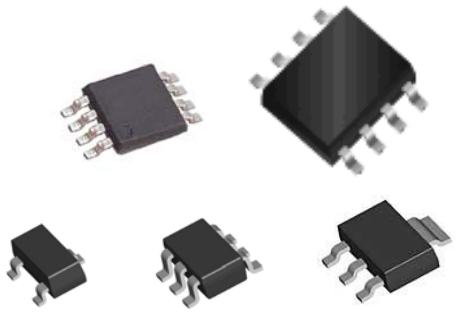
MSOP : Miniature Small Outline Package

SOT: Small Outline Transistor

P Type = With Exposed Bottom Pad

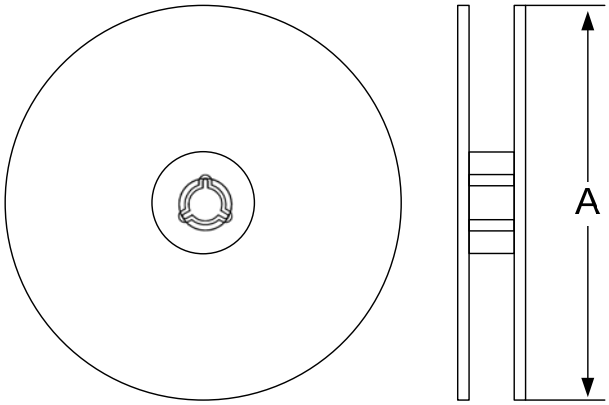
F Type = With Fused Lead

T Type(for SOT) = Thin package(Thickness = 0.85 ± 0.05mm)

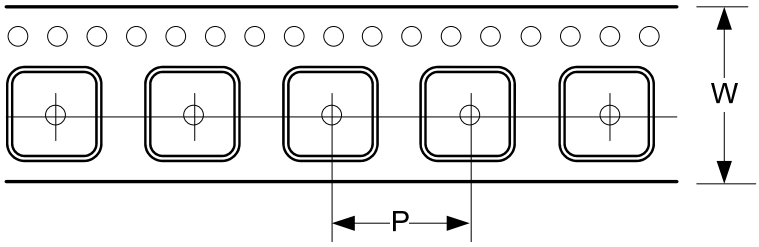


Tape & Reel Drawing

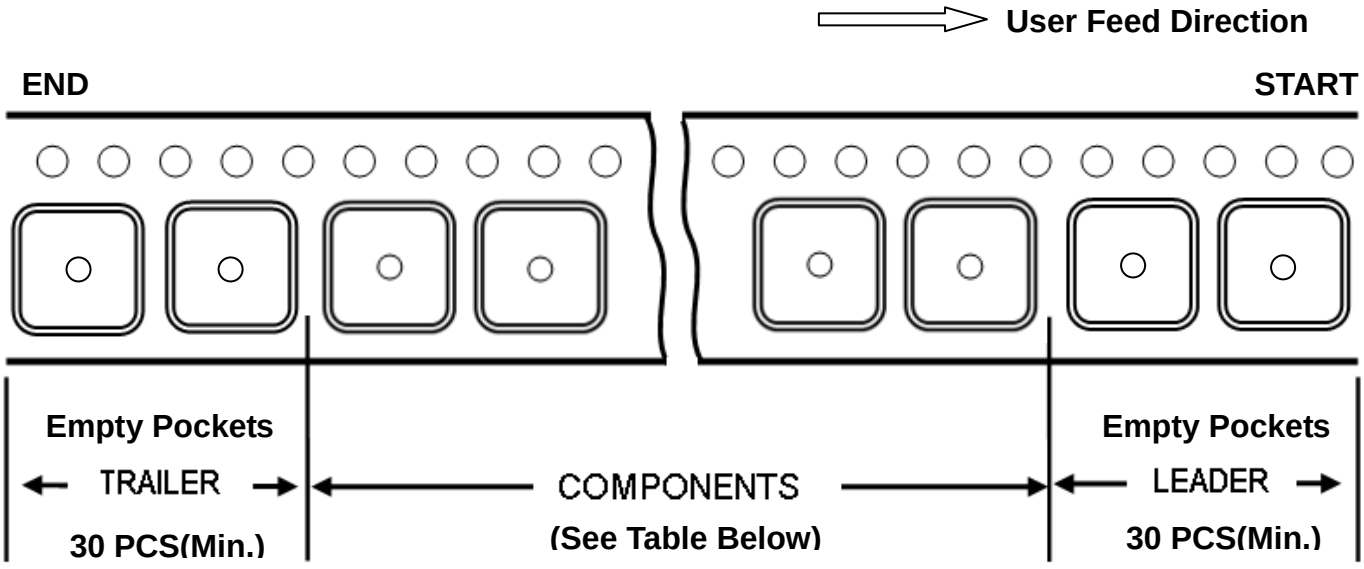
Lock Reel



Carrier Tape

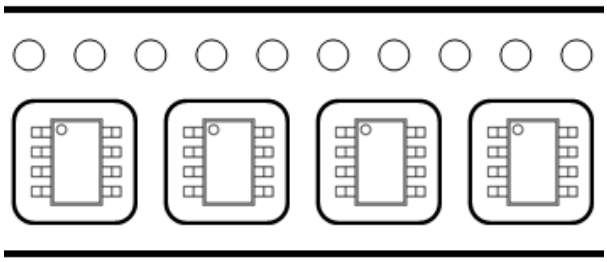


Packing Illustration

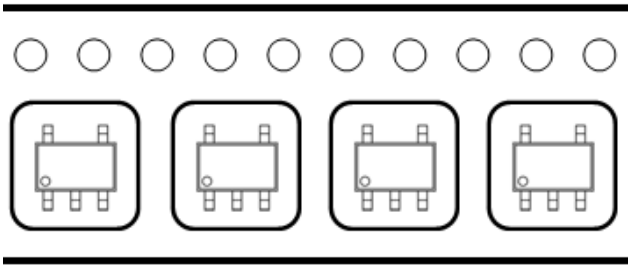


Pin1 Orientation

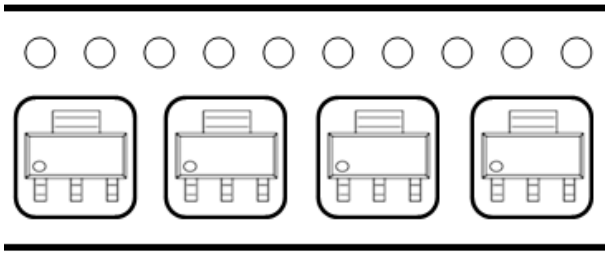
TSSOP/SOP/MSOP Series



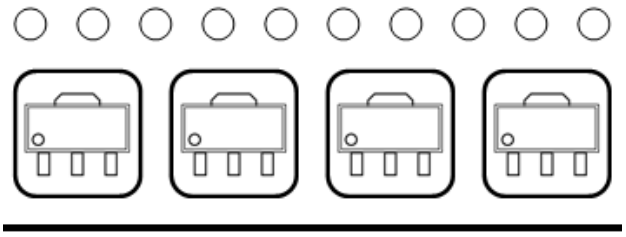
SOT23/353 Series



SOT223 Series



SOT89 Series



Packing Quantity List

PKG Type Body Size	Reel Diameter(A) (inch/mm)	Carrier Width(W) (mm)	Carrier Pitch(P) (mm)	Reel Quantity (pcs)	Remark
(P/F)SOP 8L	13 / 330	12	8	2500	
(P)SOP 14/16L	13 / 330	16	8	2500	
TSSOP 14	13 / 330	12	8	2500	
TSSOP 20	13 / 330	16	8	2500	
(T)SOT23 3/5/6/8 L	7 / 180	8	4	3000	
SOT89	7 / 180	12	8	1000	
MSOP 8L	13 / 330	12	8	2500	
(T)SOT223	13 / 330	12	8	2500	
SOT353 (SC 70 5L)	7 / 180	8	4	3000	

Packaging Drawing

Barcode Label – Apply for Reel/Al Bag/Inner Box and Outer Carton

P/N：uPI Part Number

LOT：Wafer Lot Number

QTY：Packing Quantity

D/C：Manufacturing Date Code

DATE：Packing Date

Note：For Internal Use Only

Inner Box

Box A(7” Reel)

183*183*80mm

Box B(13” Reel)

355*338*50mm

Outer Carton

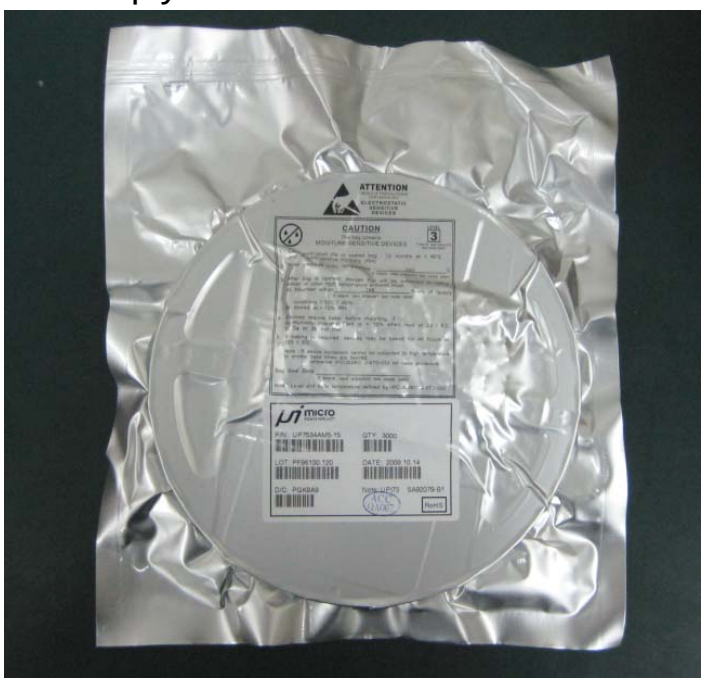
Carton A
382*283*390mm

Carton B
550*385*375mm

Carton C
645*365*250mm

Package Storage Condition:

- Vacuum Sealed into Moisture Barrier Bag and Meet MSL Level 3 requests.
- Comply with J-STD-033 standard.



- Storage Condition

  Vacuum Sealed : 12 months at <40℃ and 90%RH

  Bag Opened : Within 168 hrs at < 30℃ / 60%RH

- Baking Condition

  Re-Backing @ 125℃ +/- 5 ℃, 9hrs for IC only;

  Floor life begins counting at time =0 after Re-Backing.

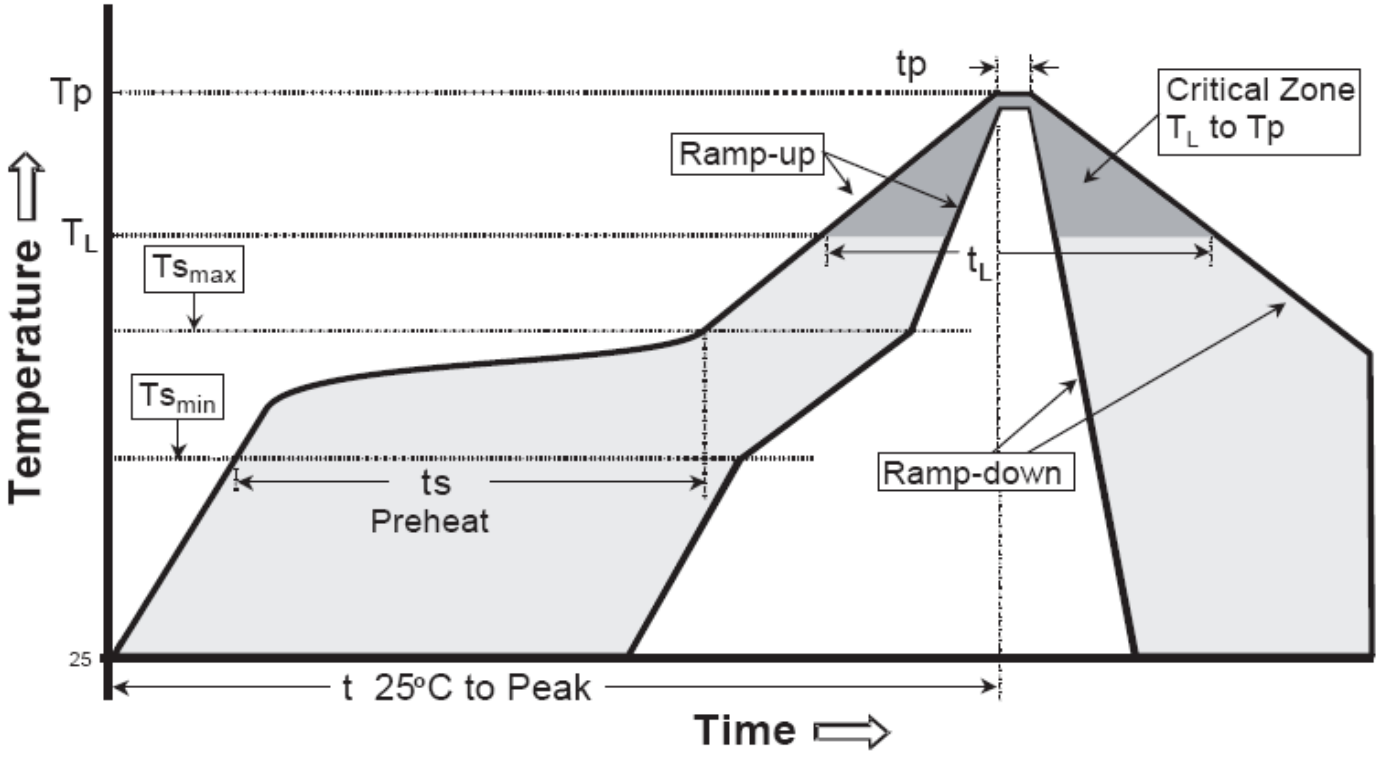
  The times of Re-Backing: 2 times, Max.

Halogen-Free Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 -2000	Volume mm^3 > 2000
< 1.6 mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6 mm - 2.5 mm	260 +0 °C	250 +0 °C	245 +0 °C
≧ 2.5 mm	250 +0 °C	245 +0 °C	245 +0 °C

IR Reflow Profile

Profile Feature	Halogen-Free Assembly
Average Ramp-uP Rate (TS_{max} to Tp)	3 °C/second max.
Preheat - Temperature Min (TS_{min}) - Temperature Max (TS_{max}) - Time (TS_{min} to TS_{max})	 150 °C 200 °C 60-180 Seconds
Time Maintained above - Temperature (TL) - Time (tL)	 217 °C 60-150 Seconds
Peak/Classification Temperature (Tp)	<=260 °C
Time Within 5 °C of actual Peak Temperature (tp)	20-40 seconds
Ramp-Down Rate	6 °C/second max.
Time 25 °C to Peak Temperature	8 minutes max.



Part No Naming Rule