# PG161-A00

# TU106 6GB GDDR6, 192b, X16
# DVI-D/DP + DP + HDMI

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V375-20
1. 移除 CO-LAY
2. Core Power: uP9512SQKI (QFN 4x4) + (NCP302045 x 4)
   Memory Power: I32-S725602-N03 + (UBIQ 3103+3107*2)
3. P.34 add R779
4. P.30 & 44 移除PS_FBVDD_BUFF換頁符號
   換 FBVDD controller，換成1PHASE 上1下2
5. P.52 add HDMI & DVI 螺絲
6. IO 換常用料，footprint 不變


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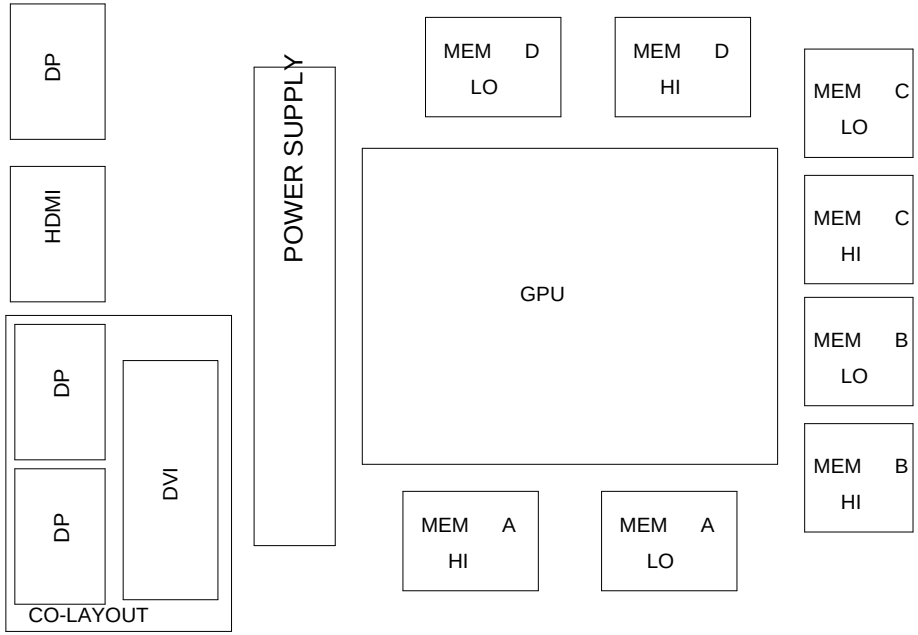
Page2: Block Diagram




Power Supply:

- Power Supply NVVDD-PH6
- Power Supply NVVDD-PH5
- Power Supply NVVDD-PH4
- Power Supply NVVDD-PH3
- Power Supply NVVDD-PH2
- Power Supply NVVDD-PH1
- Power Supply FBVDDQ-PH2
- Power Supply FBVDDQ-PH1
- Power Supply 5V
- PEX_VDD
- 1V8
- Fan
- DP_PWR

EXT_12V 2x4 PWR

PEX_12V Finger

3V3 Finger

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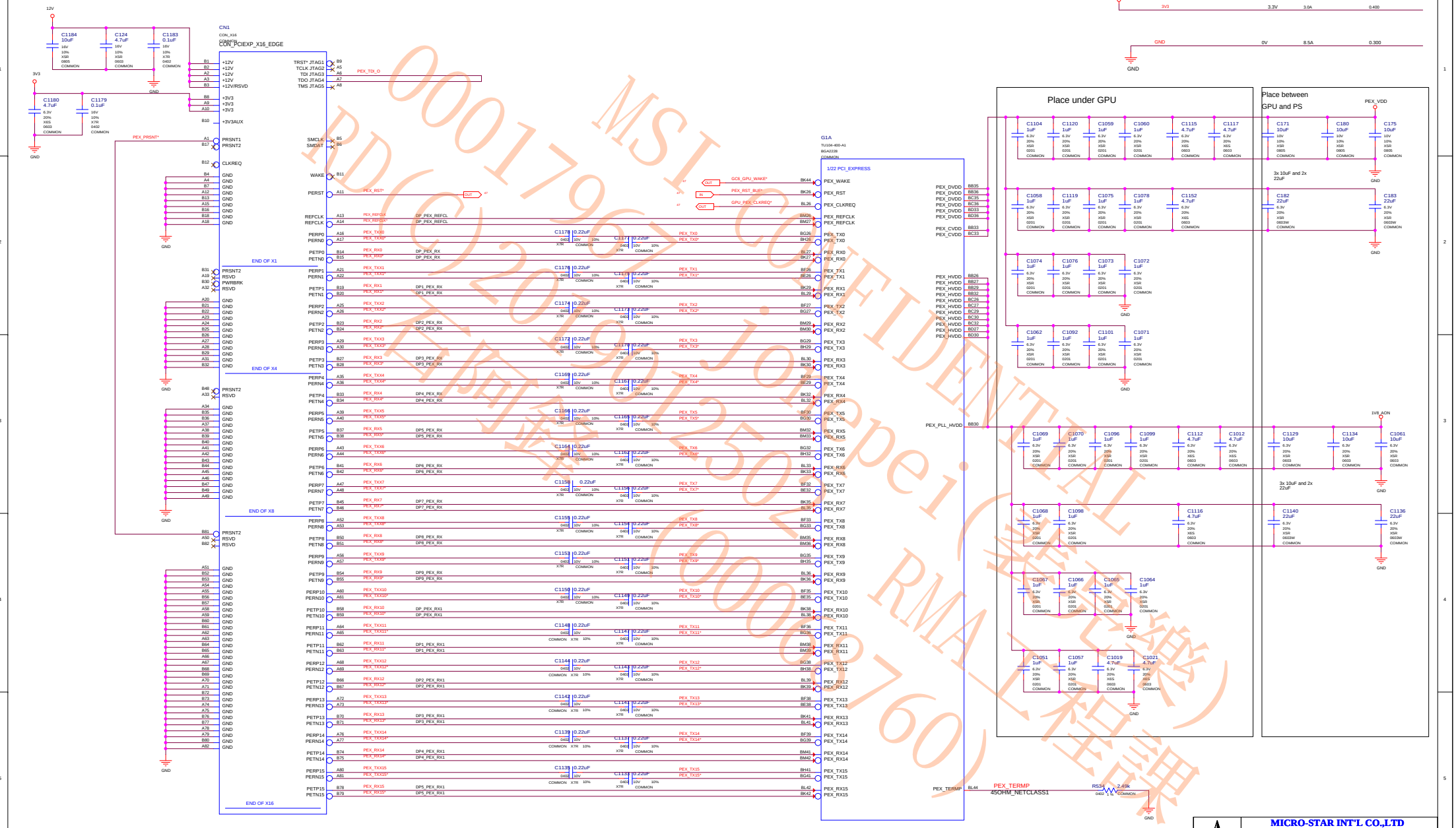
Page3: PCI Express

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# NO PEX GEN4 SUPPORT

# DELETE RC TERMINATIONS

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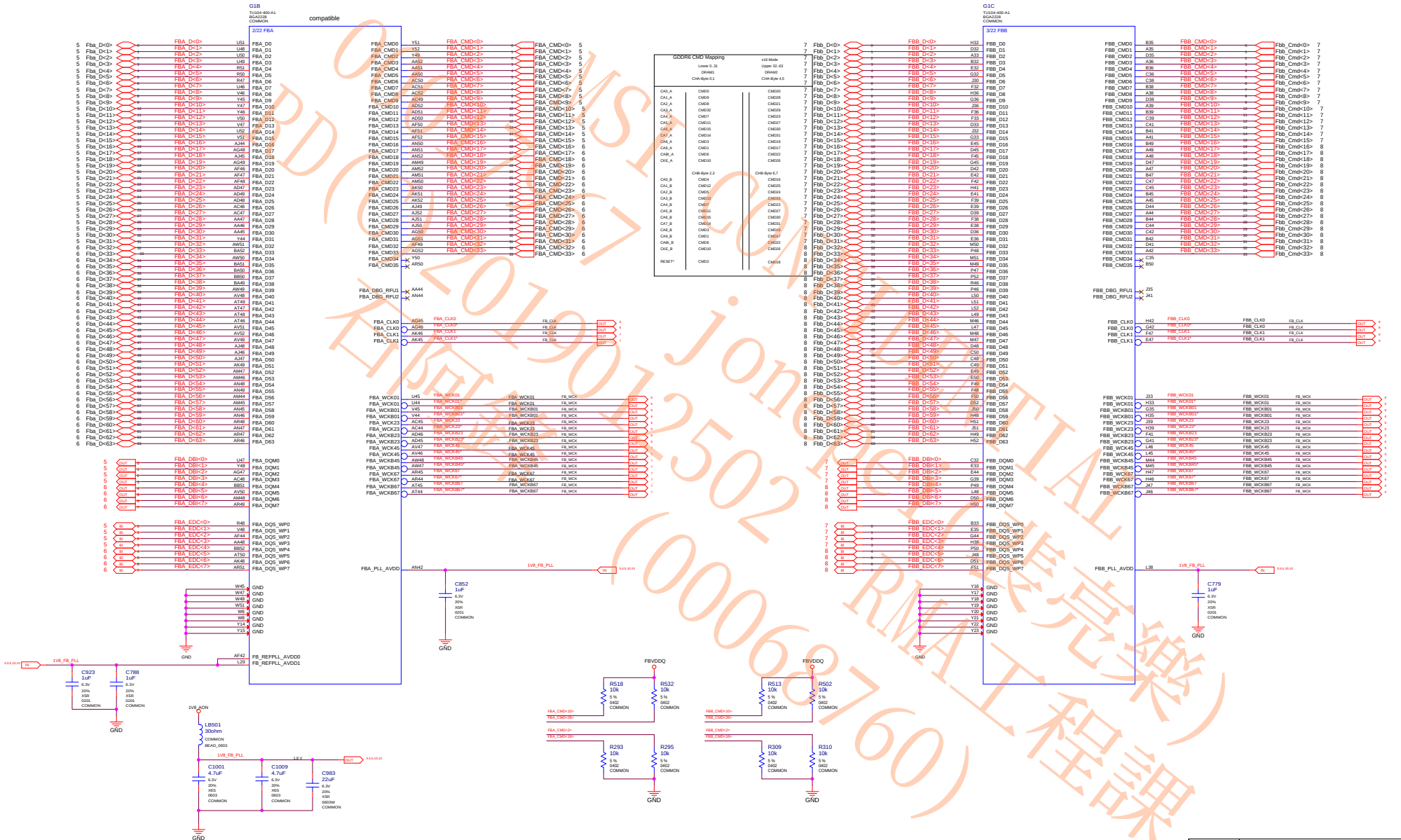
# Page5: MEMORY: GPU Partition A/B





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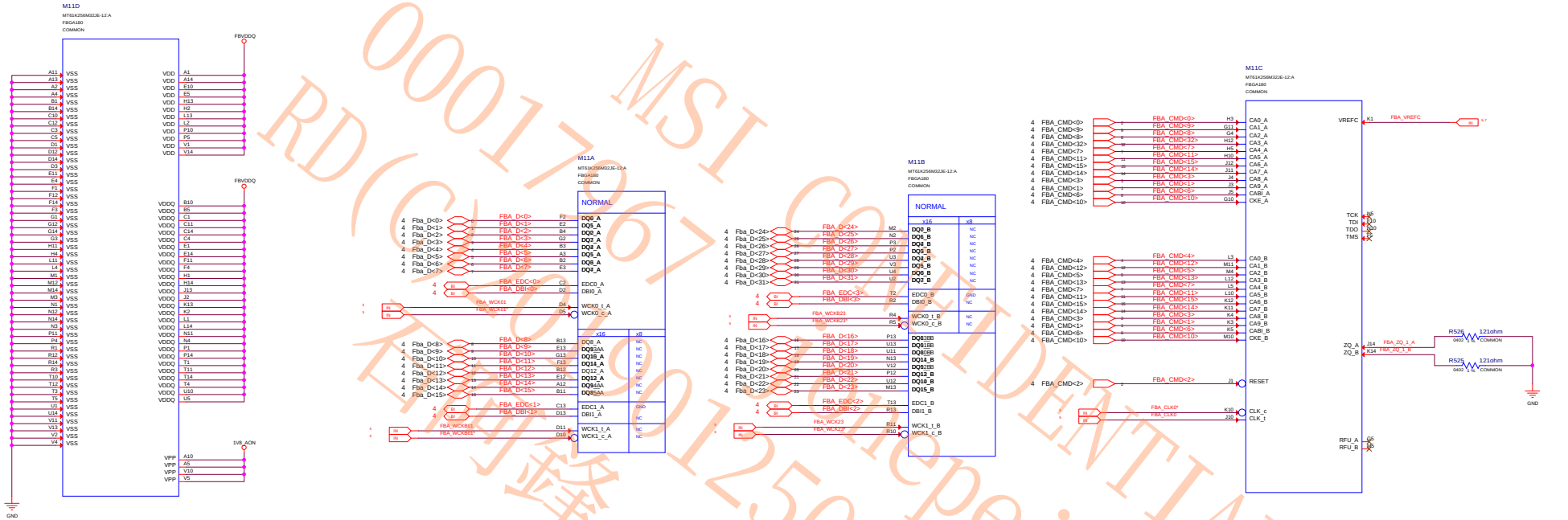
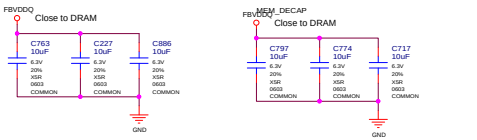
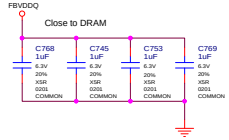
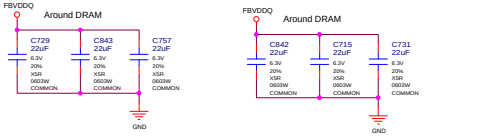


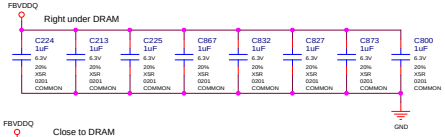



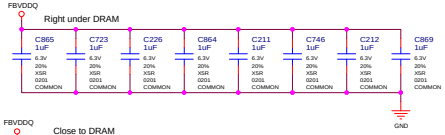



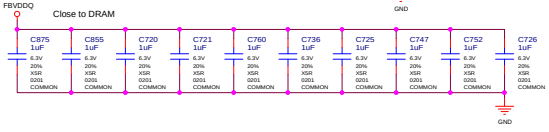



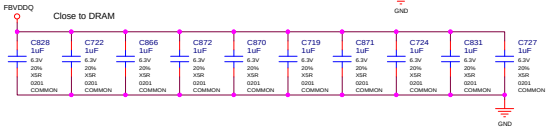




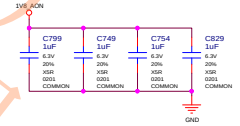



VREFC IS NOT USED IN x16 CONFIGURATION. 1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R106

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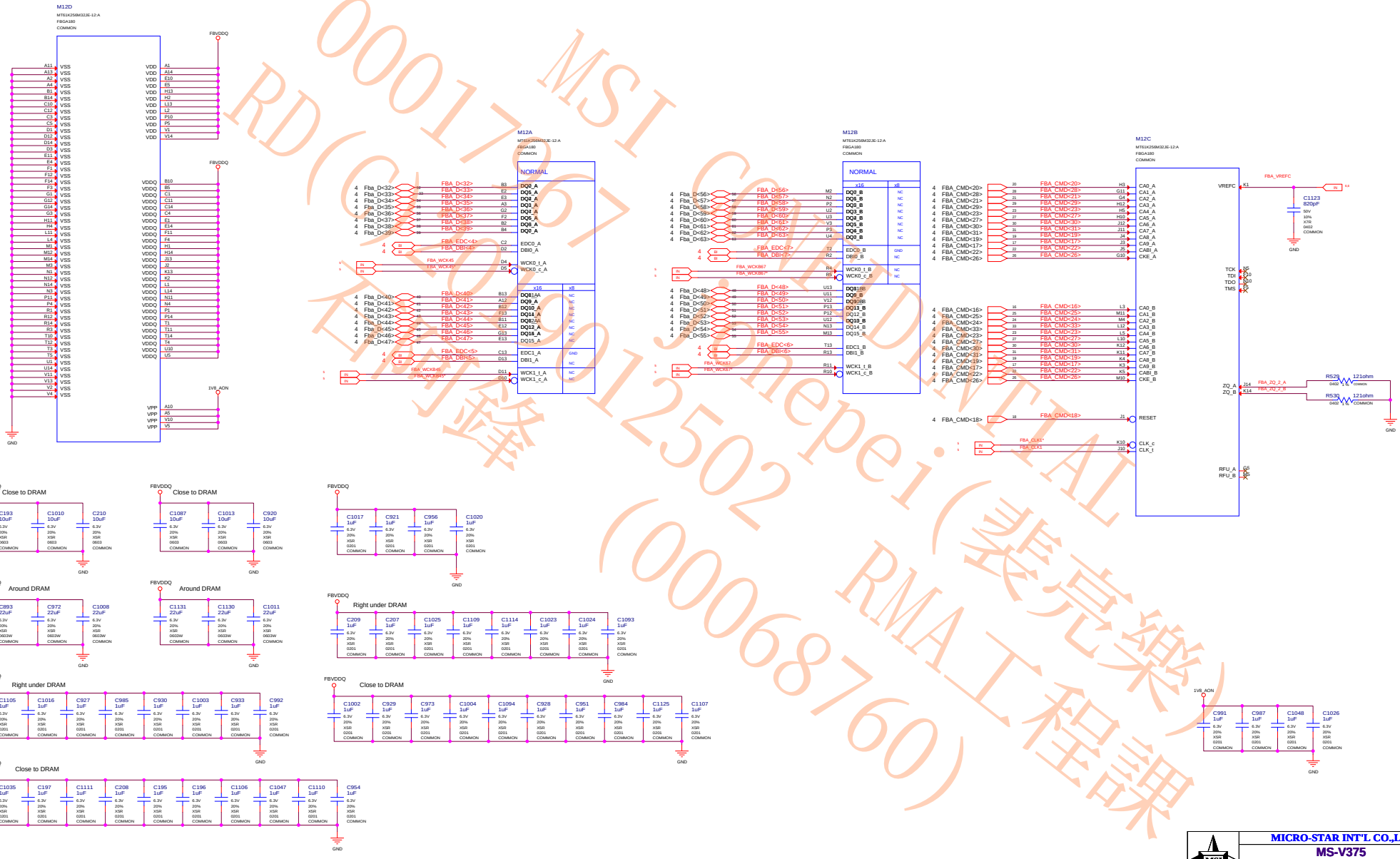


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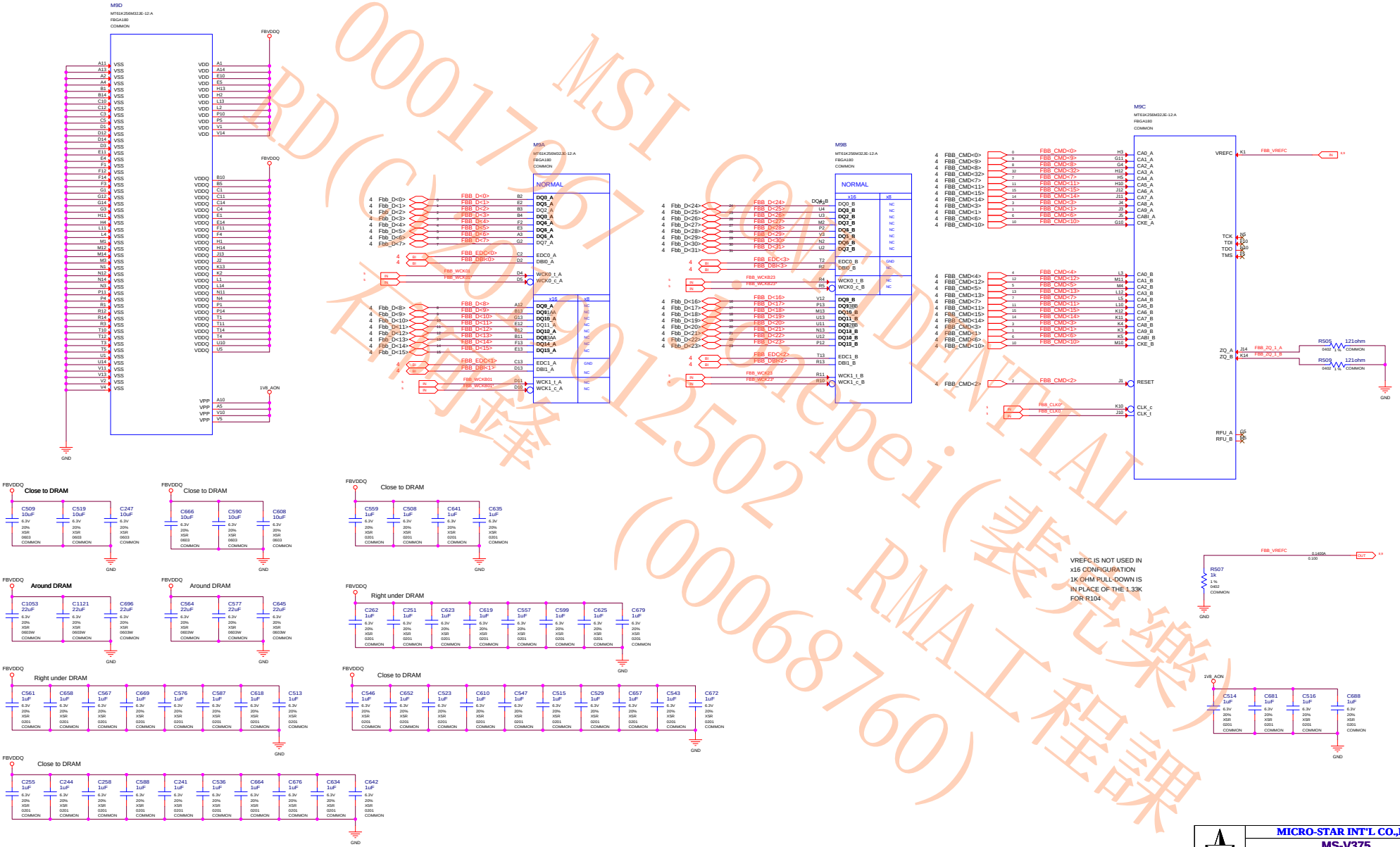


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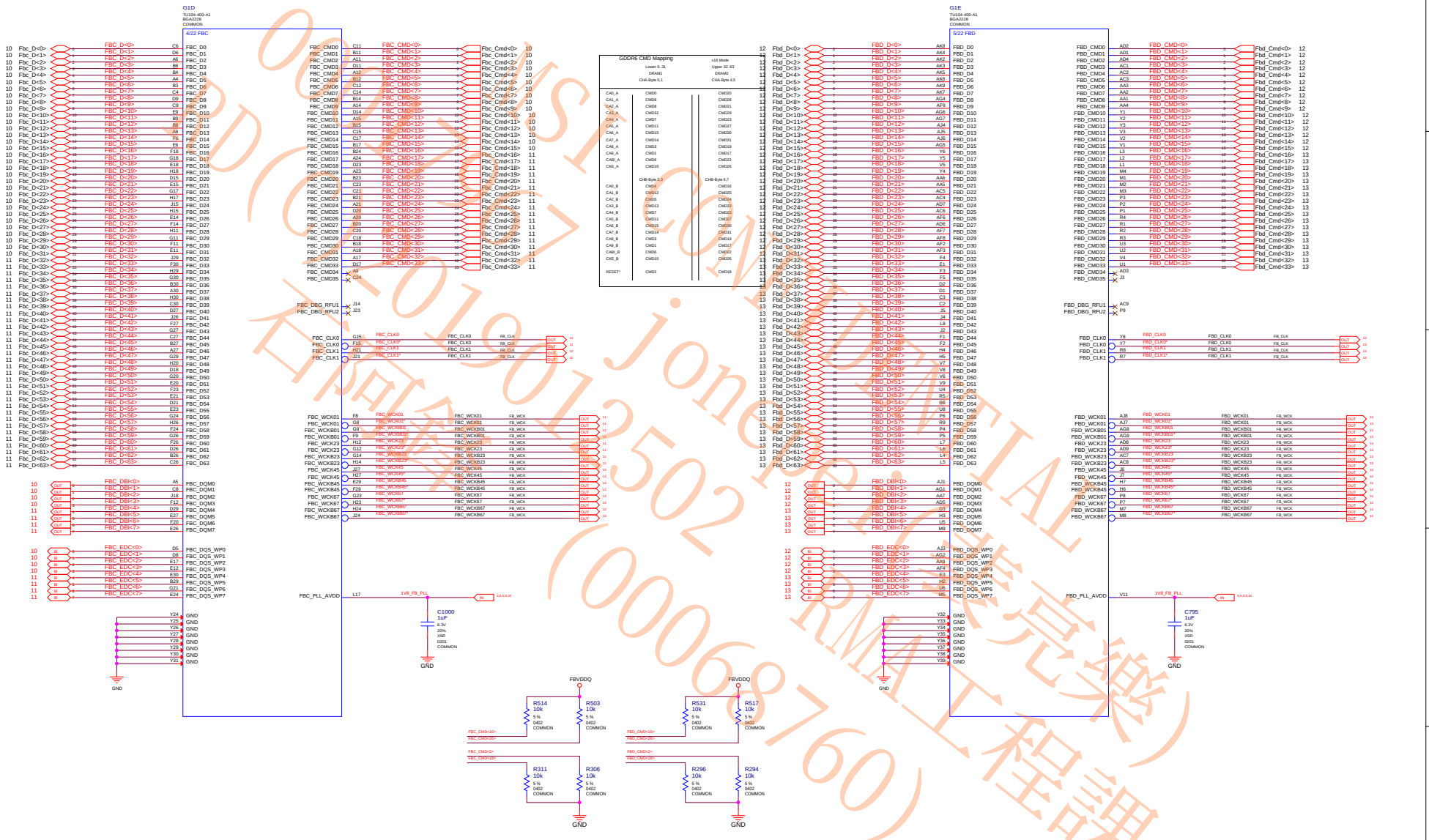
# Page10: MEMORY: GPU Partition C/D





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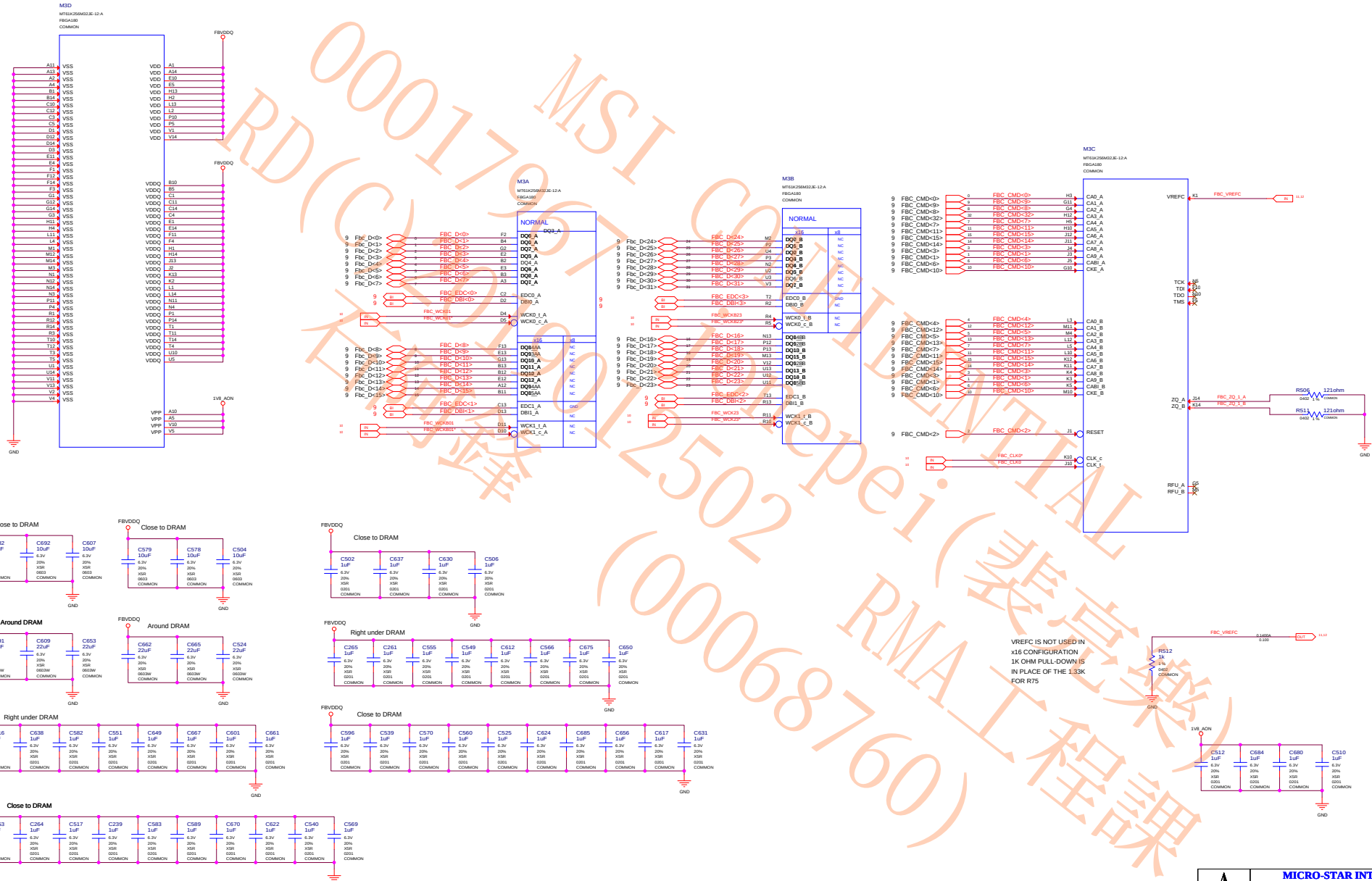



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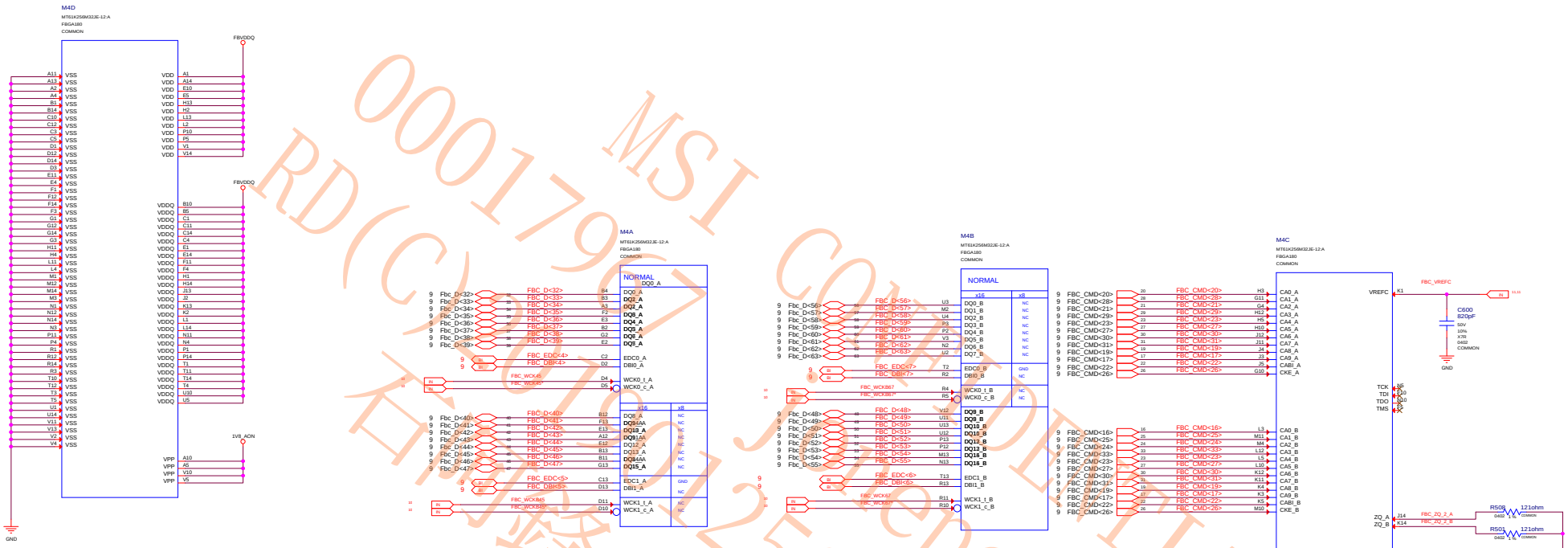



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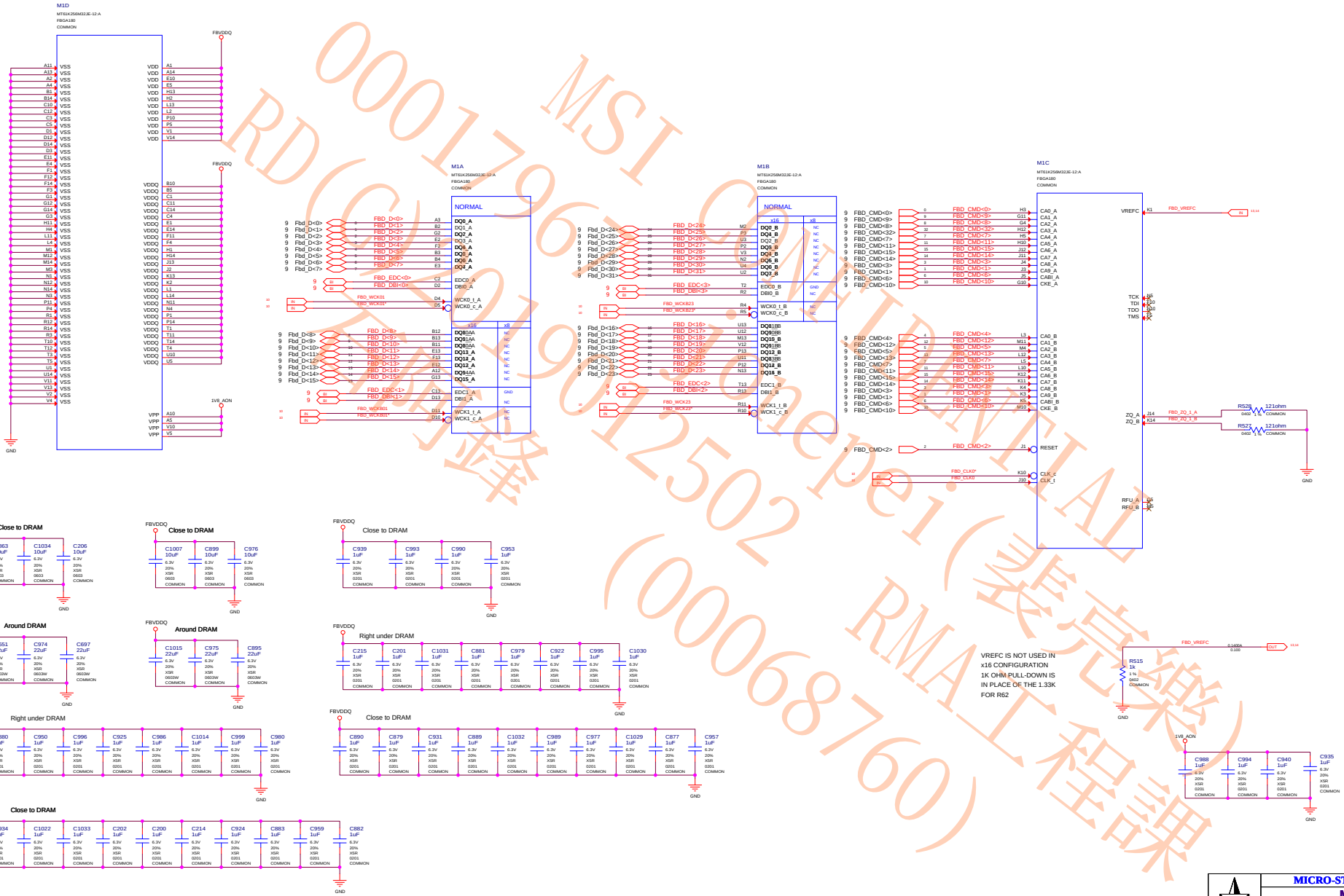


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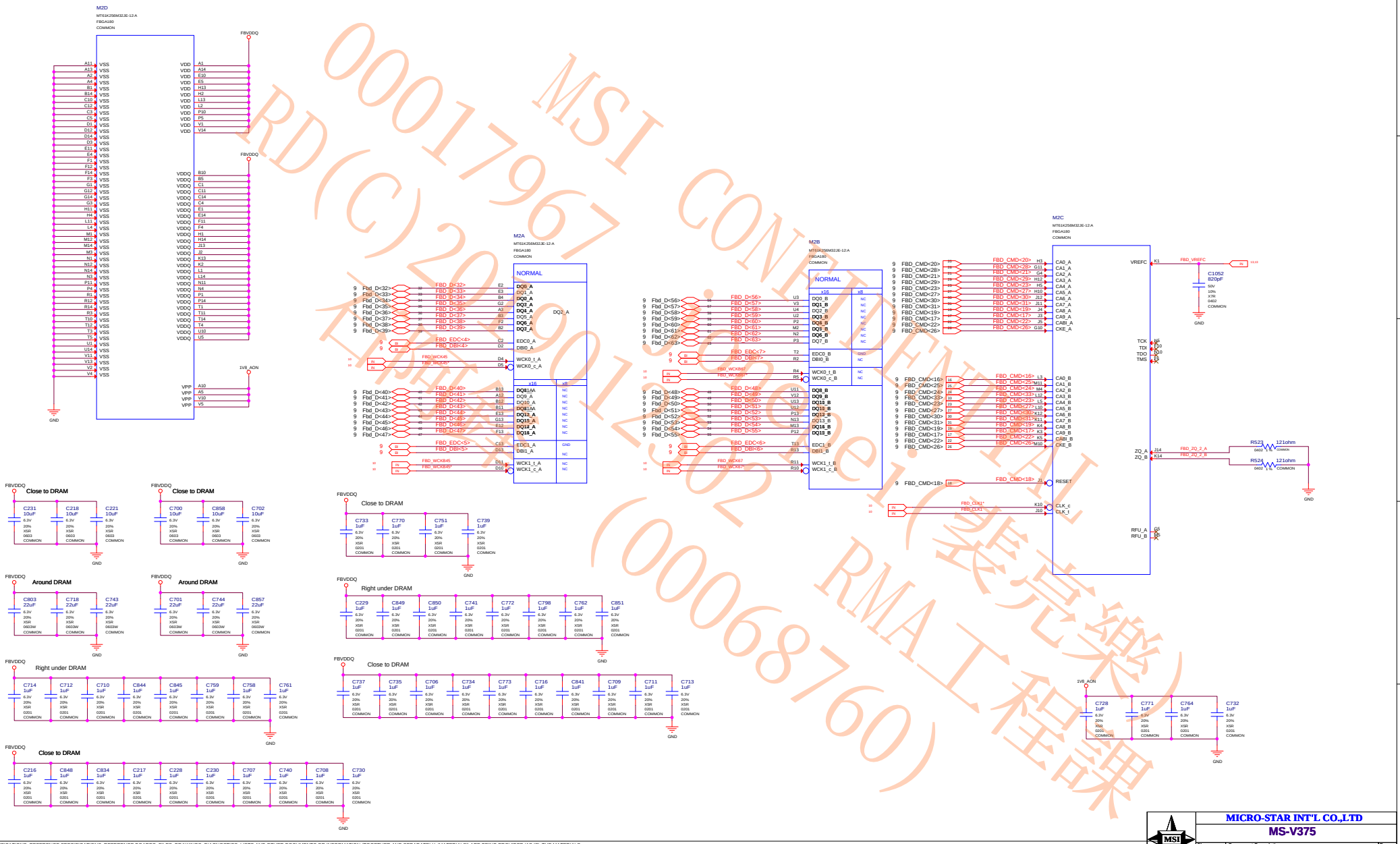


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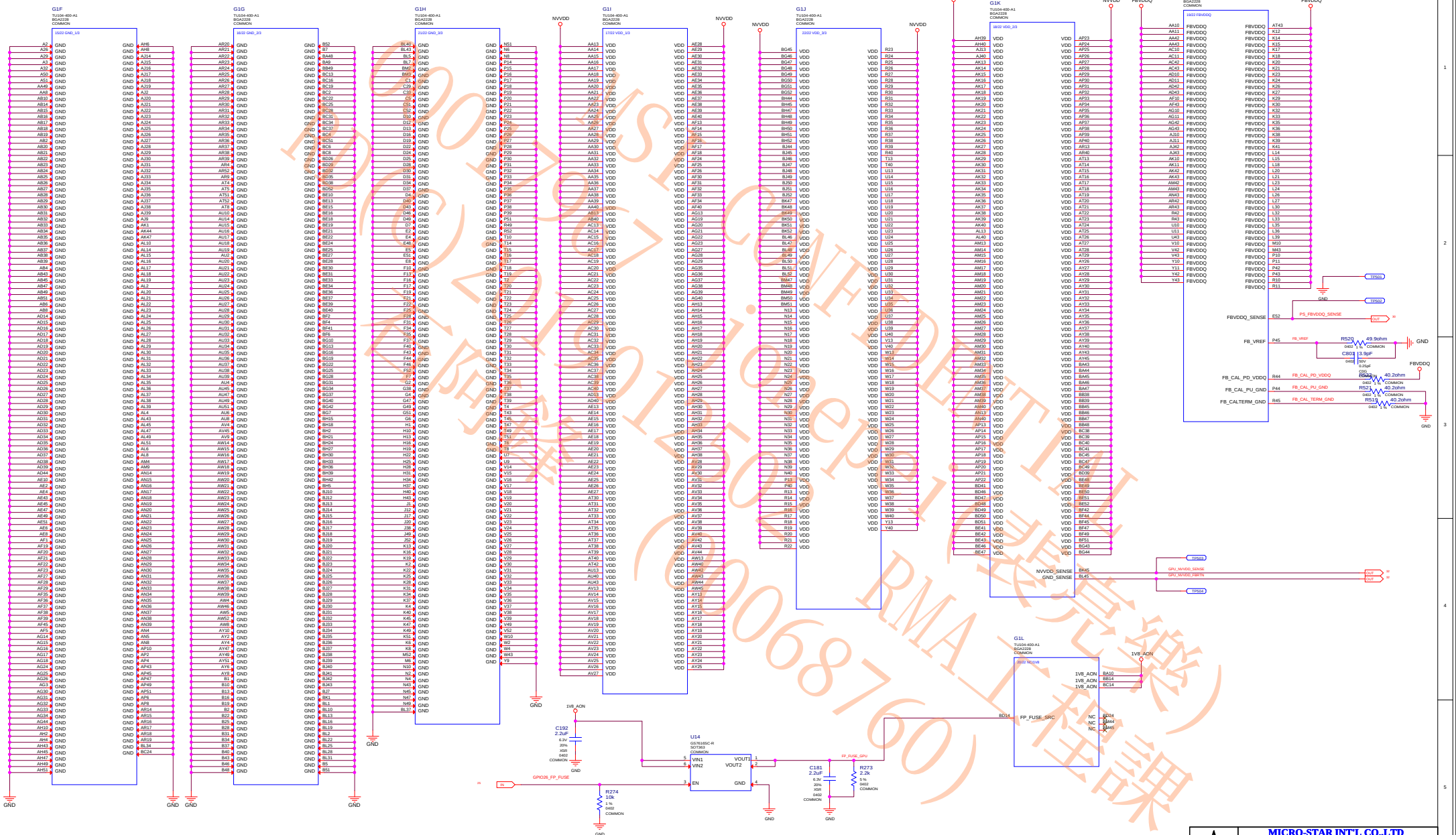
# Page15: GPU PWR and GND





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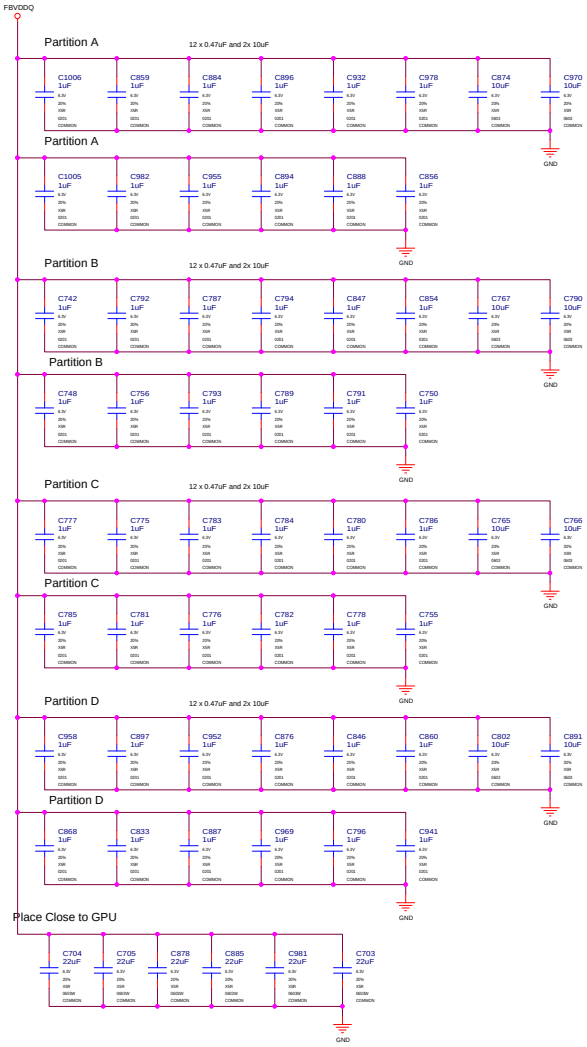
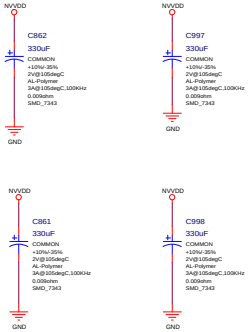
# Page16: GPU Decoupling 1

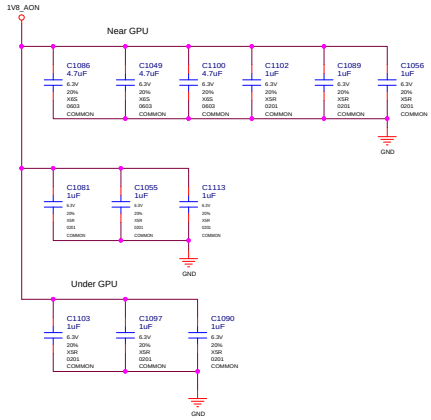
## FBVDDQ




## NVVDD




## 1V8_AON

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| Custom | Page16: GPU Decoupling 1 | 1.0 |

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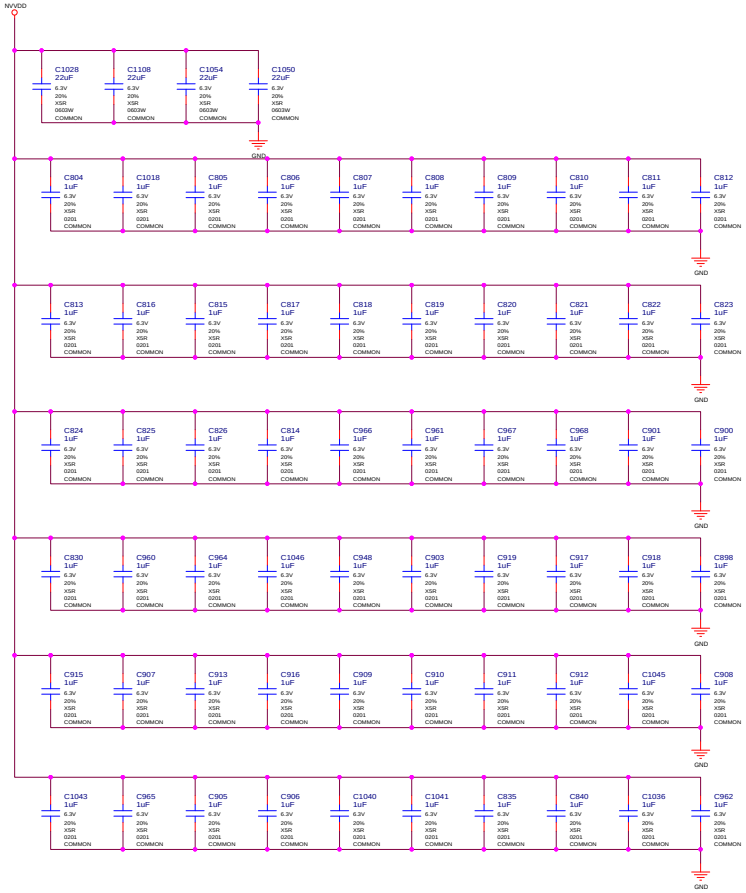
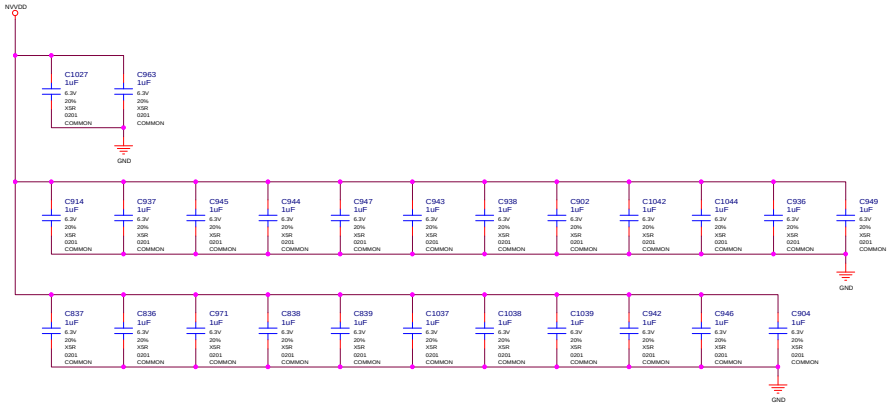
# Page17: GPU Decoupling 2

## NVVDD

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| Custom | Page17: GPU Decoupling 2 | 1.0 |

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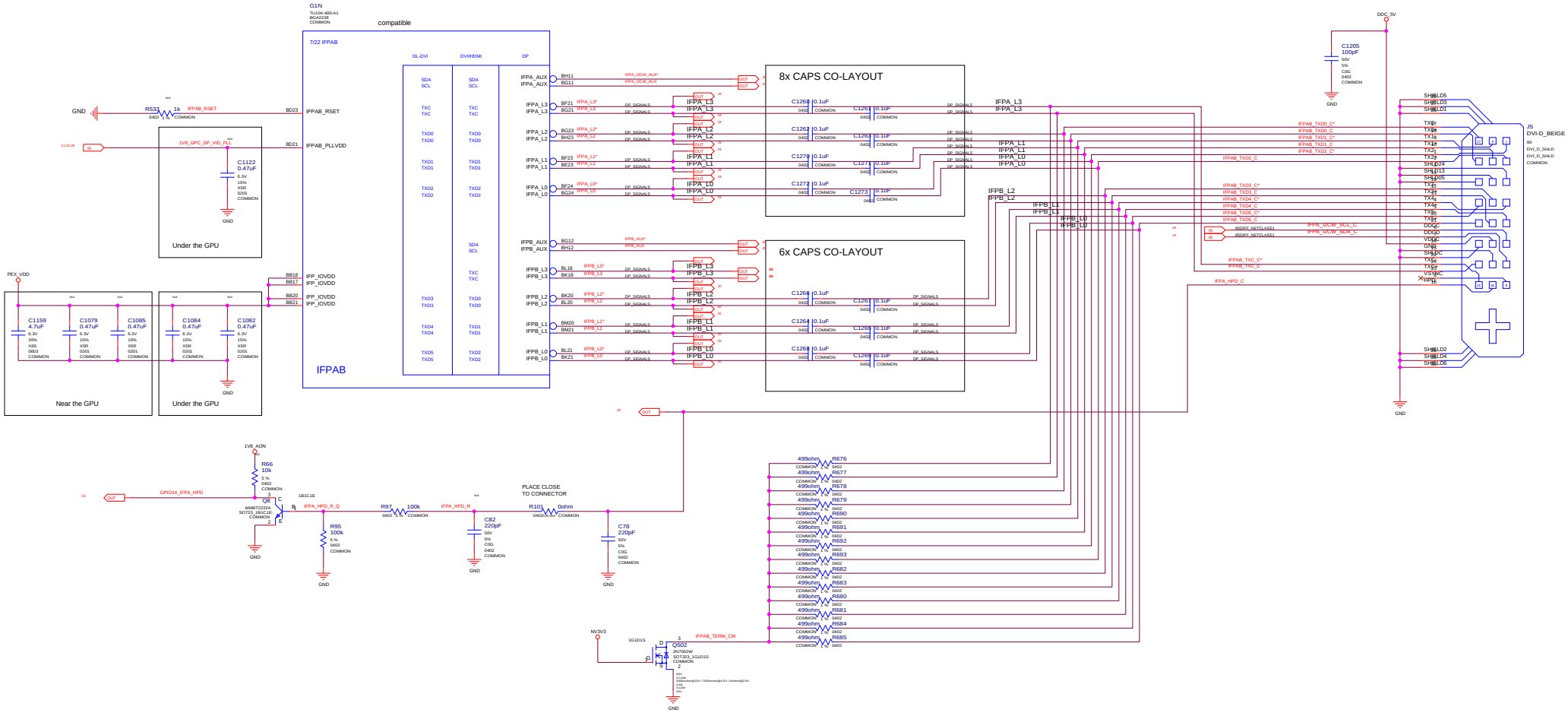
# IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP

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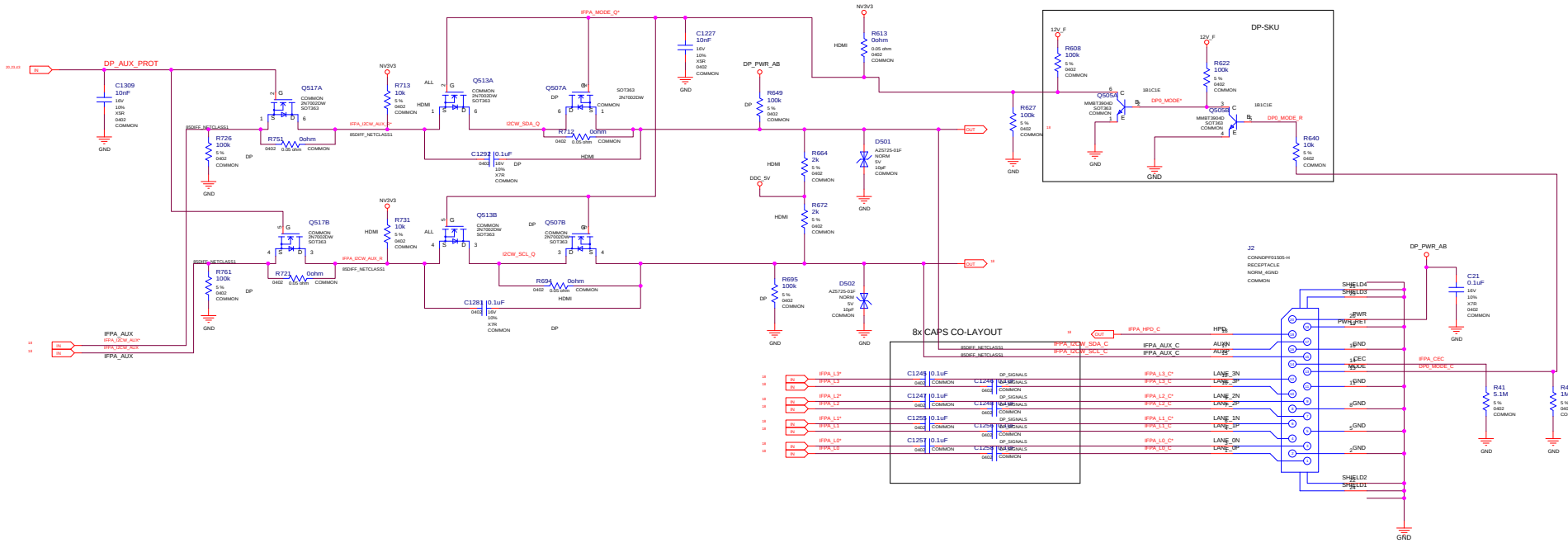


# IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

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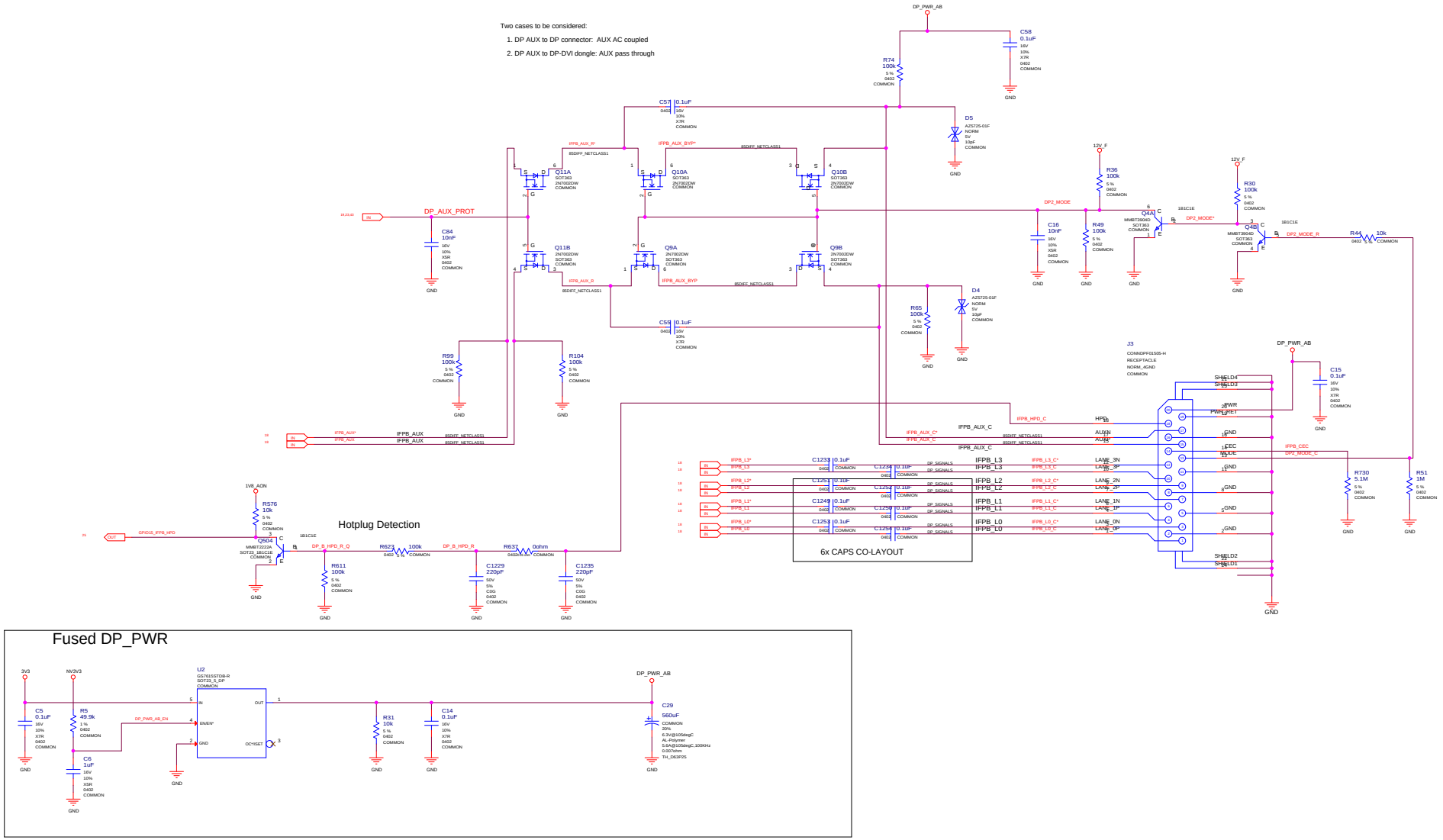
# IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

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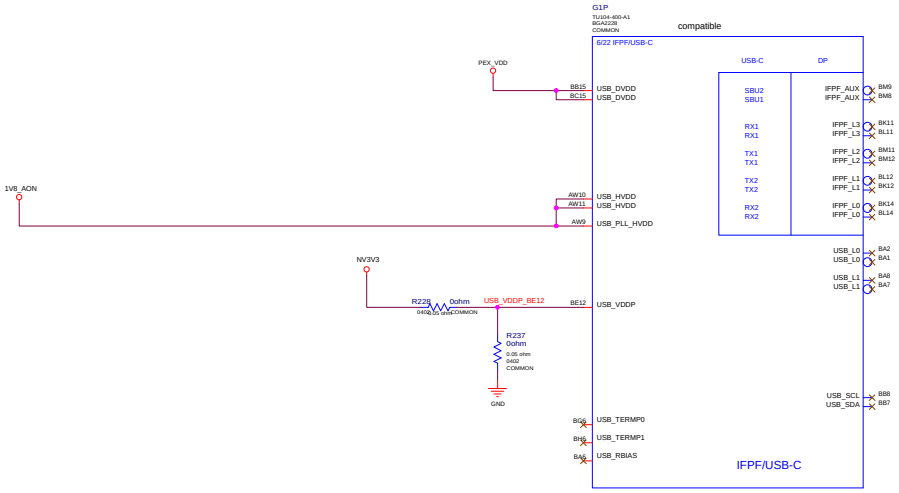
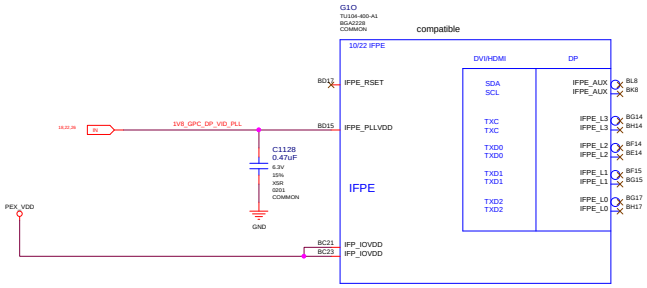
Page21: IFPE & IFPF USB-C NC




IFPF NC




IFPE NC

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IO: IFPE & IFPF USBC NC

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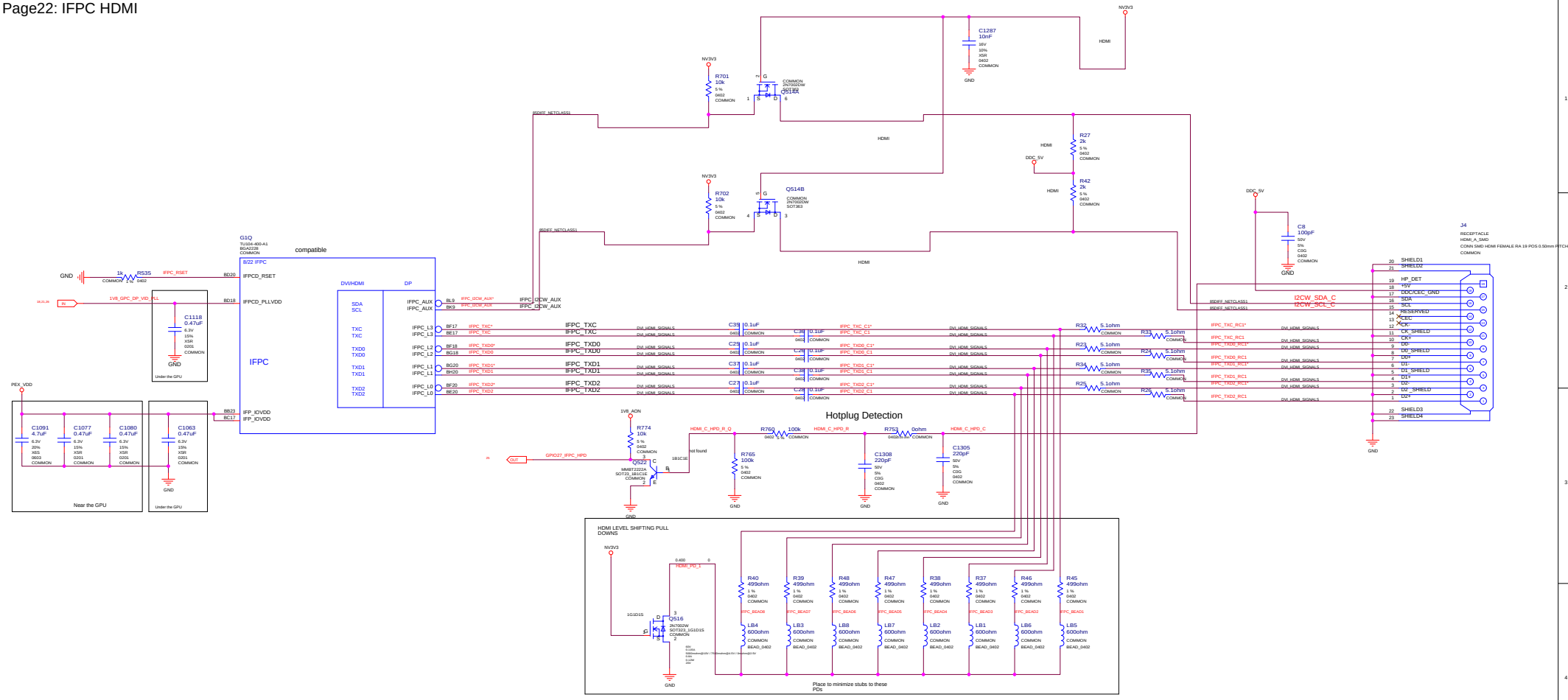
# Page22: IFPC HDMI





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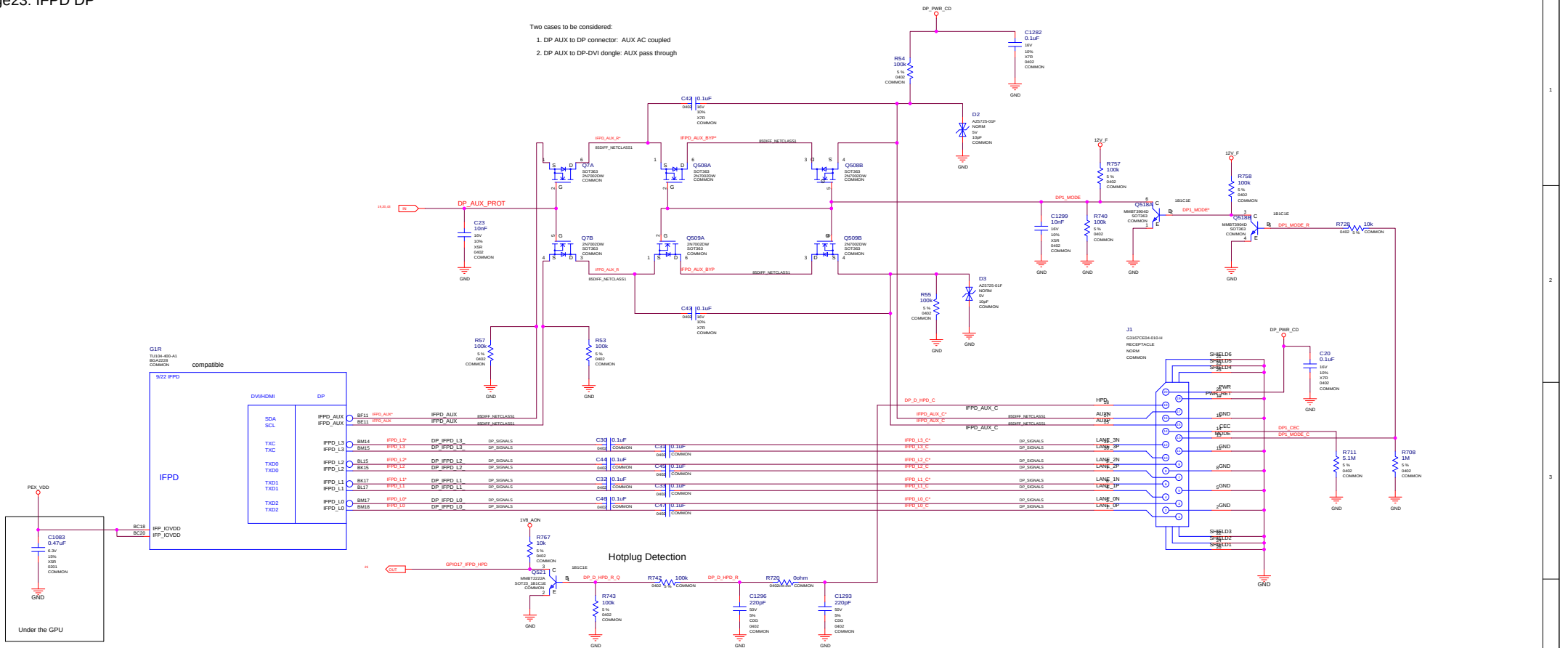
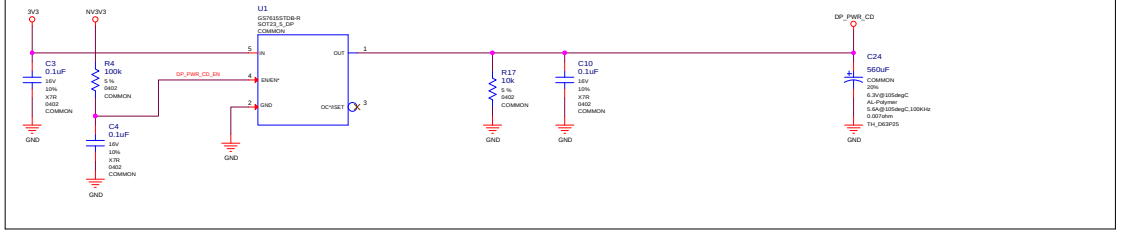
# Page23: IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through




## Fused DP_PWR

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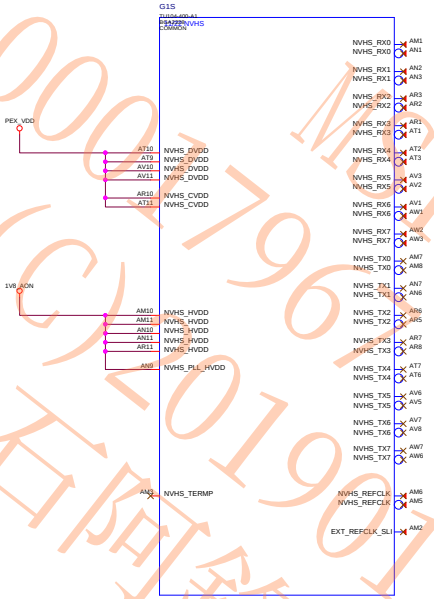
Page24: NVHS Interface and Frame Lock

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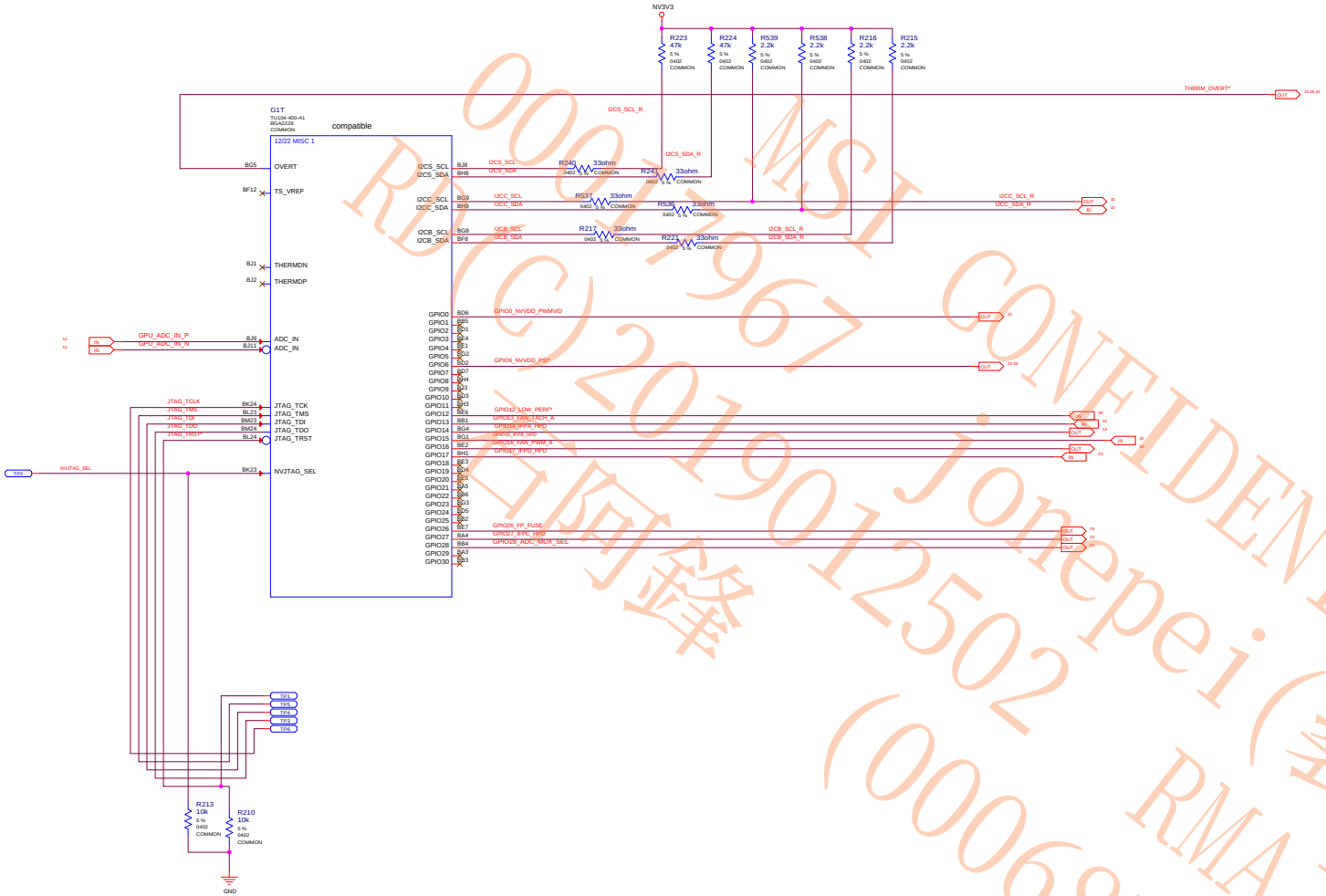
Page25: MISC1: Fan, Thermal, JTAG, GPIO





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# Page26: MISC2: ROM, XTAL, Straps

| STRAP2 | STRAP1 | STRAP0 | RAMCFG[4:0] |
|---|---|---|---|
| L | L | L | 00000 |
| L | L | H | 00001 |
| L | H | L | 00010 |
| L | H | H | 00011 |
| H | H | L | 00110 |
| H | H | H | 00111 |
| L | L | M | 01000 |

| RAMCFG[4:0] | DENSITY | WIDTH | VENDOR | DIE |
|---|---|---|---|---|
| 00000 | 8Gb | 256-bit | Samsung | C |
| 00001 | 8Gb | 256-bit | Micron | A |
| 00010 | 8Gb | 256-bit | Hynix | M |
| 00011 | 8Gb | 256-bit | Samsung | C |
| 00100 | 8Gb | 256-bit | Micron | A |
| 00101 | 8Gb | 256-bit | Hynix | M |
| 00110 | 16Gb | 256-bit | Samsung | M |
| 00111 | | | | |

| ROM_SO | ROM_SI | ROM_SCLK | DUMMY[2:0],FS_OVERT | | |
|---|---|---|---|---|---|
| L | L | L | XXX1 | 1:ENABLE 0:DISABLE<br>FS_OVERT ENABLE | DEFAULT |
| L | L | M | XXX0 | FS_OVERT DISABLE | |

| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |
|---|---|---|---|---|---|---|
| M | H | H | 1 | 1 | 1 | 1 |
| M | H | L | 1 | 1 | 1 | 0 |
| M | L | H | 1 | 1 | 0 | 1 |
| M | L | L | 1 | 1 | 0 | 0 |
| L | H | M | 1 | 0 | 1 | 1 |
| L | M | H | 1 | 0 | 1 | 0 |
| L | M | L | 1 | 0 | 0 | 1 |
| L | L | M | 1 | 0 | 0 | 0 |
| H | H | H | 0 | 1 | 1 | 1 |
| H | H | L | 0 | 1 | 1 | 0 |
| H | L | H | 0 | 1 | 0 | 1 |
| H | L | L | 0 | 1 | 0 | 0 |
| L | H | H | 0 | 0 | 1 | 1 |
| L | H | L | 0 | 0 | 1 | 0 |
| L | L | H | 0 | 0 | 0 | 1 DEFAULT |
| L | L | L | 0 | 0 | 0 | 0 |

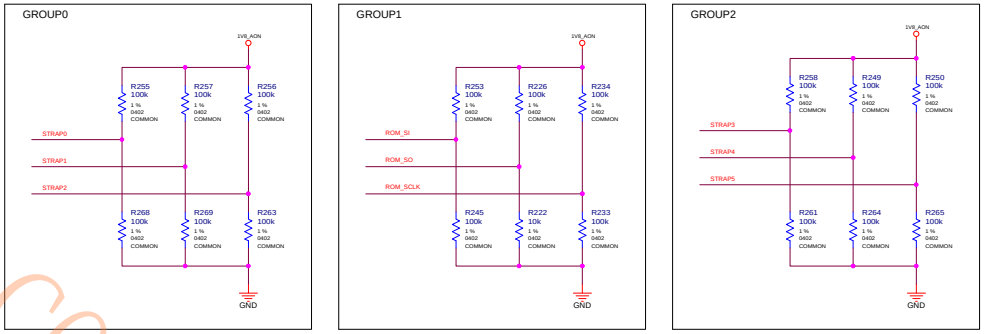
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

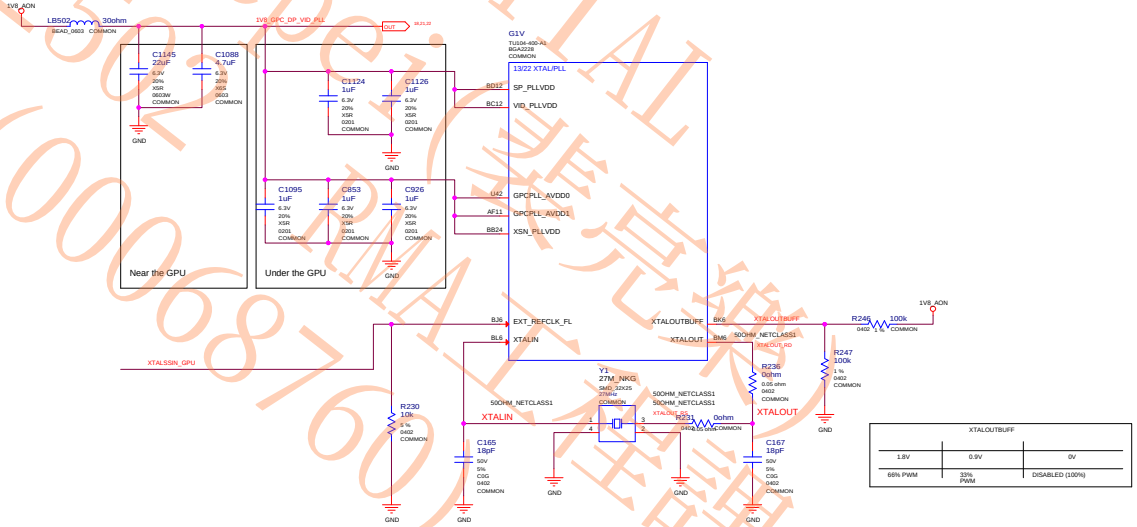
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







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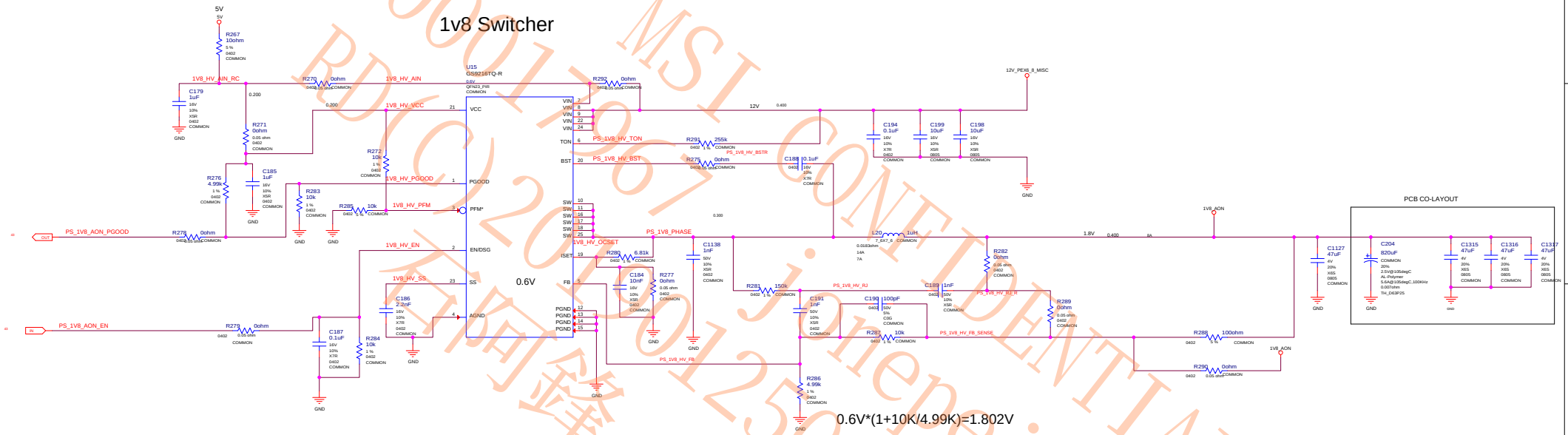


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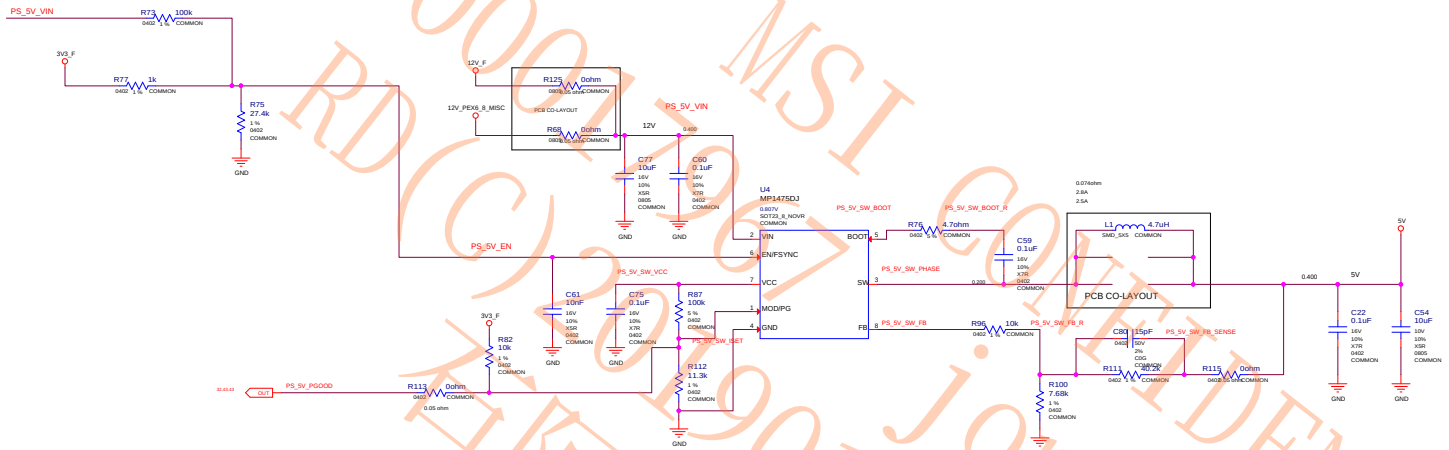
Page28: PS: 5V




0.8V*(1+40.2K/7.68K)=4.9875V

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| Size: Custom | Document Description: Page28: PS: 5V | | Rev: 1.0 |
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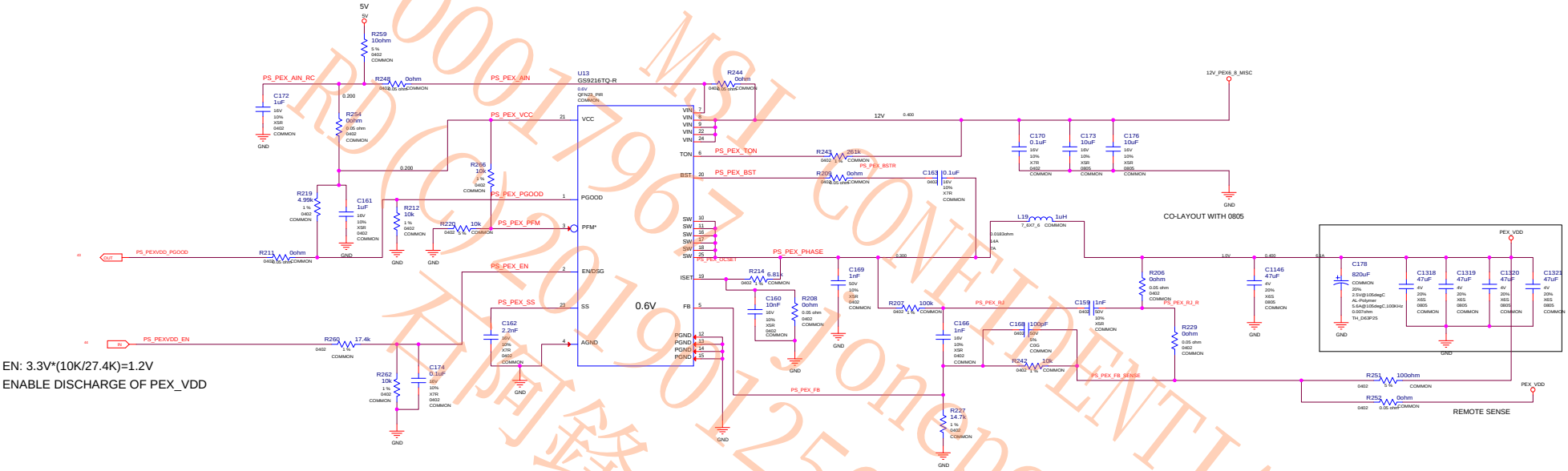
## PEX Switcher




EN: 3.3V*(10K/27.4K)=1.2V

ENABLE DISCHARGE OF PEX_VDD

0.6V*(1+10K/14.7K)=1.008V

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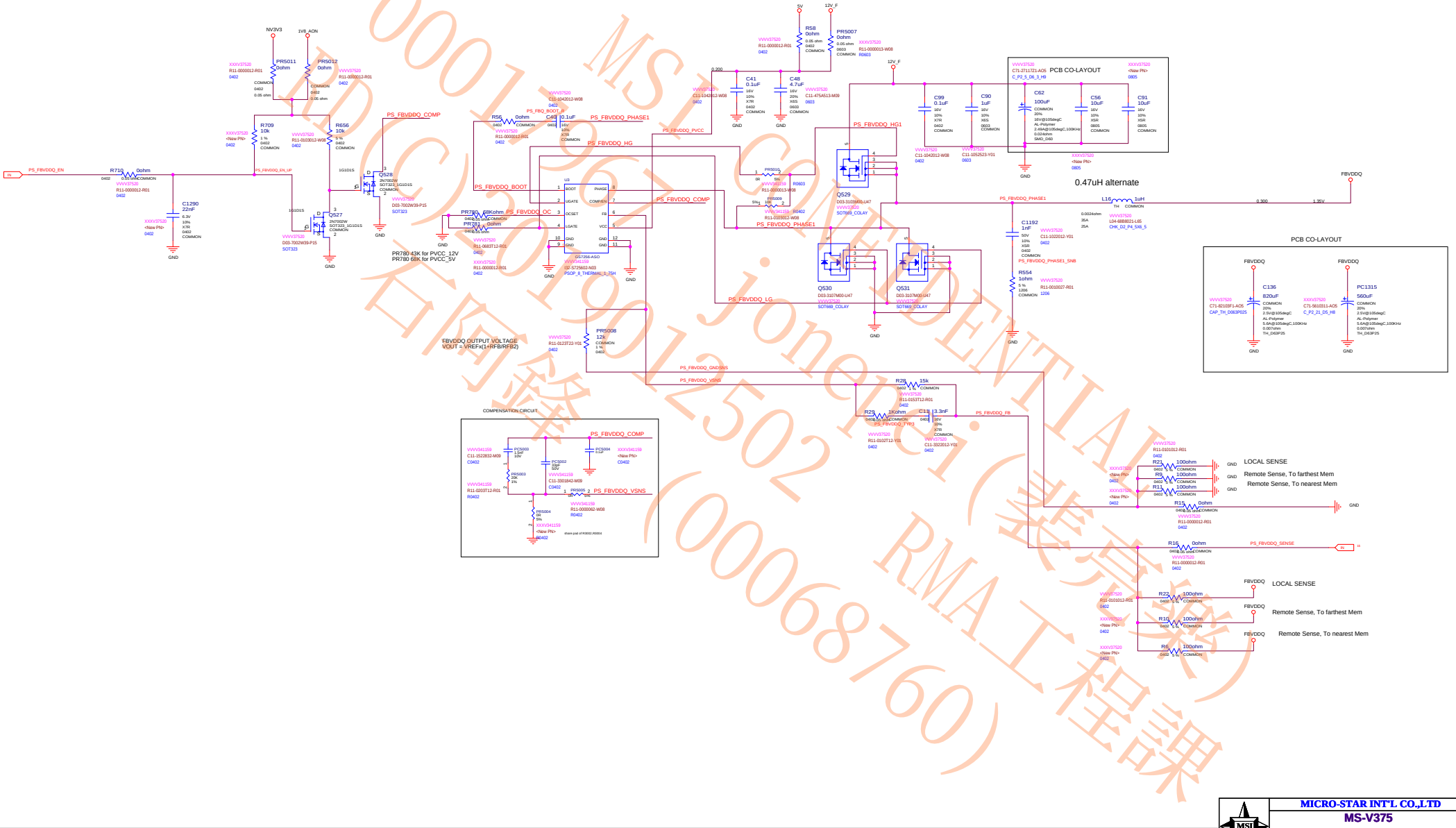
# Page30: PS: FBVDDQ





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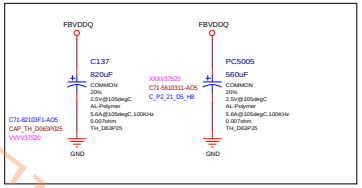
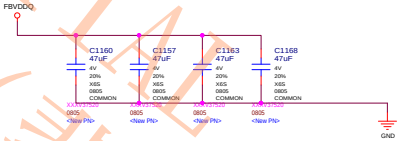
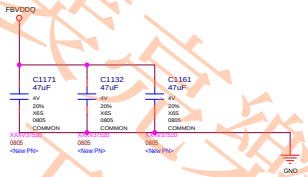
Page31: PS: FBVDDQ PH2


PCB CO-LAYOUT



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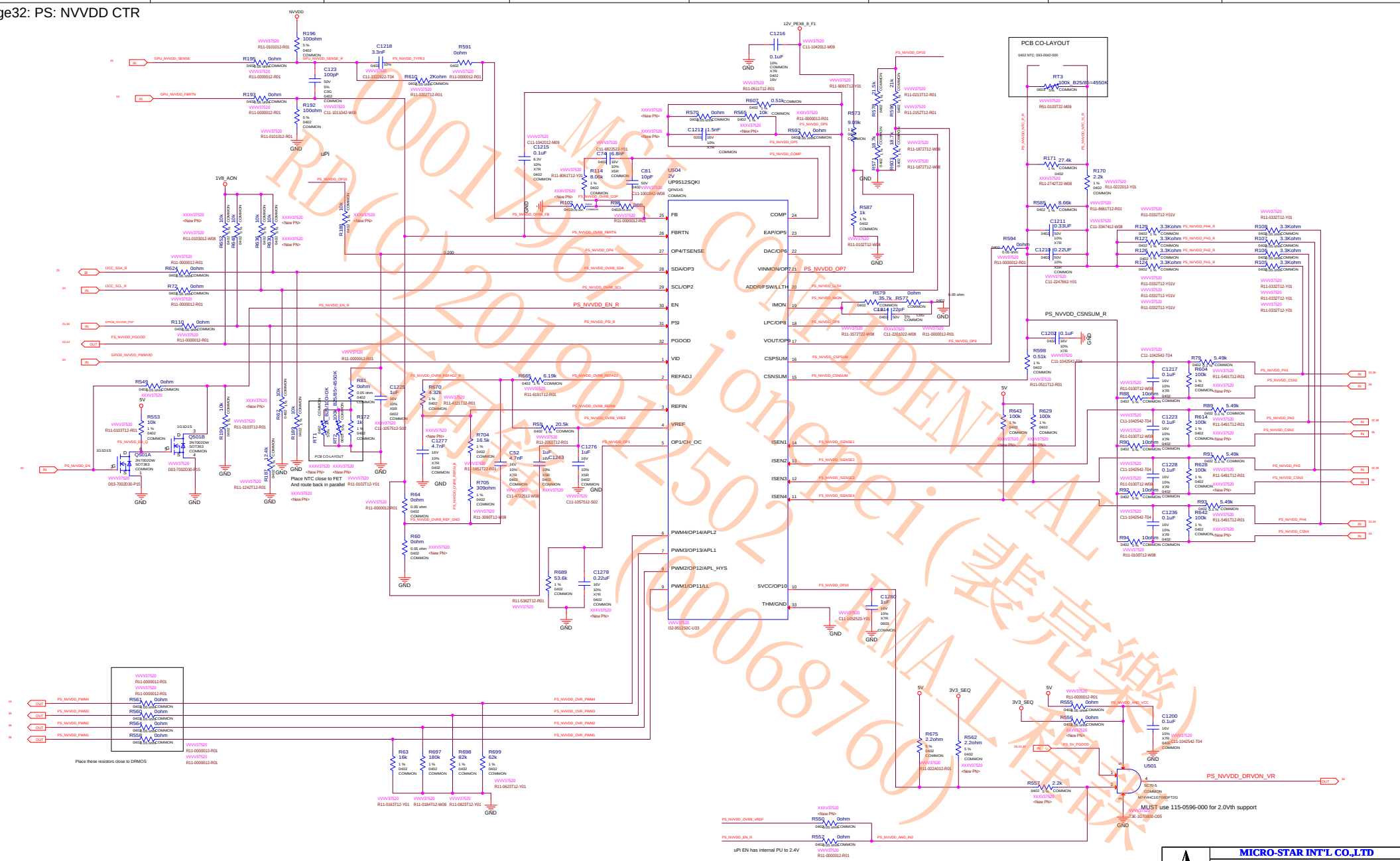


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| Size | Custom |
| Document Description | Page32: PS: NVVDD CTR |
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# DROP OVR3i SOLUTION

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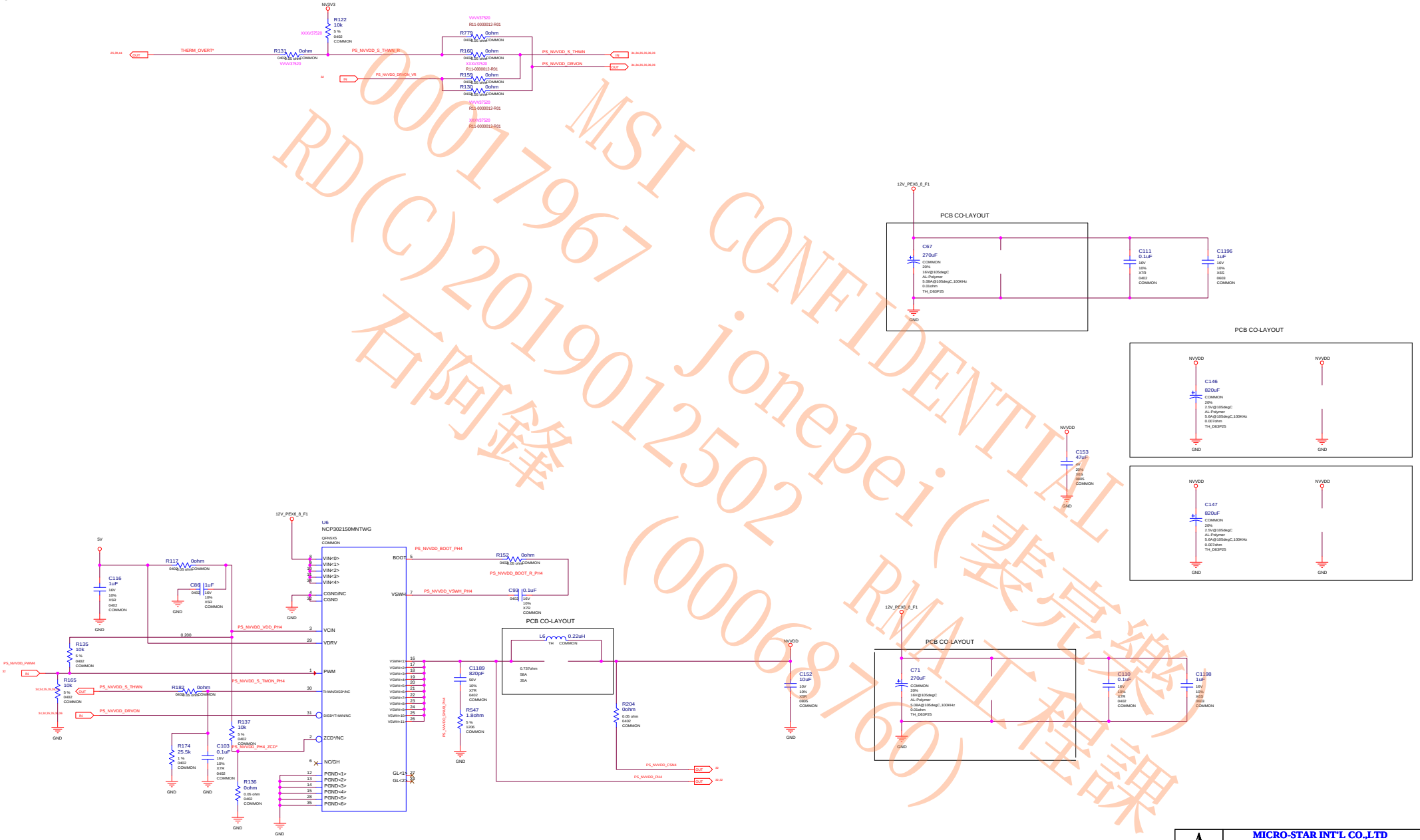
Page34: PS: NVVDD PH6&4

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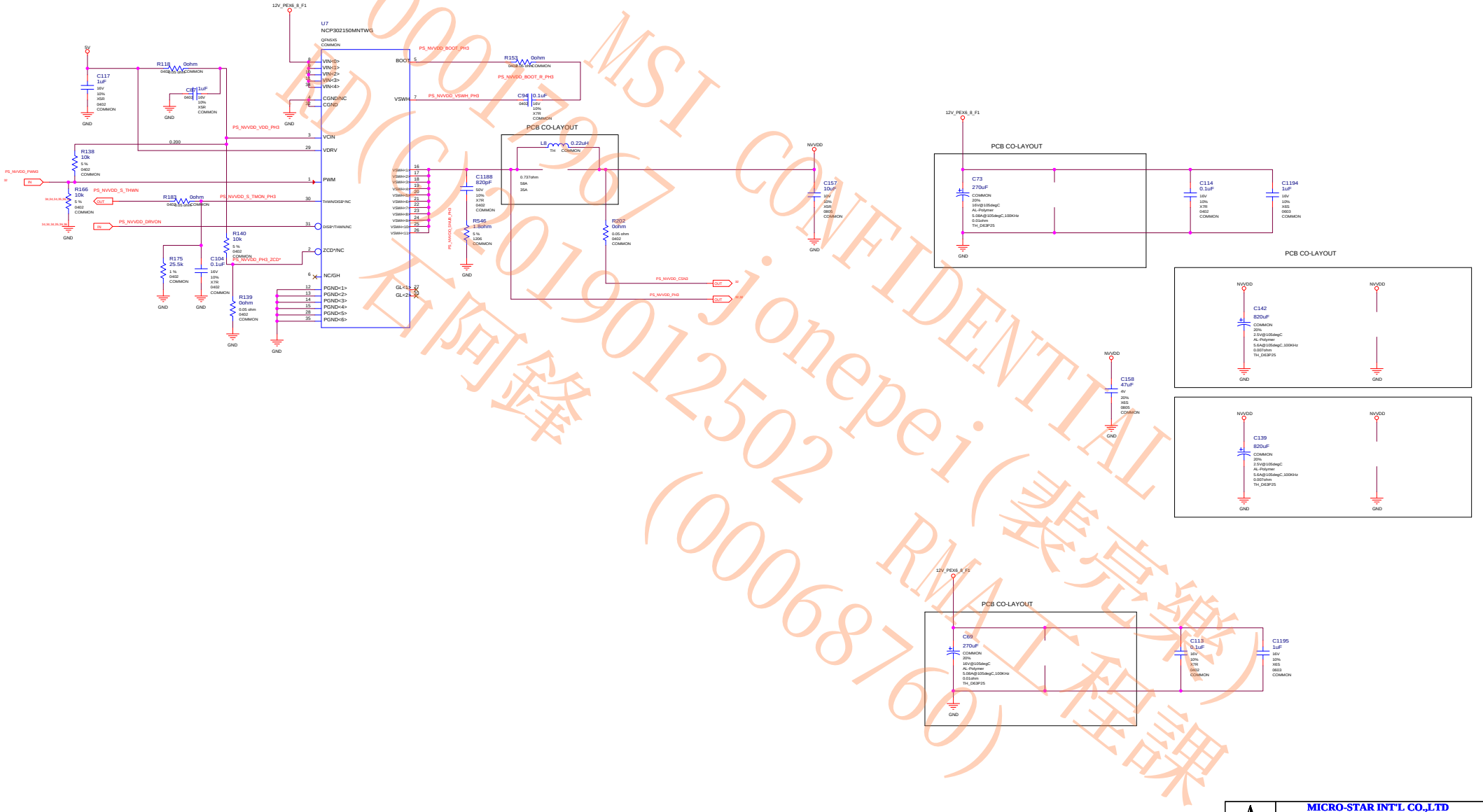
# Page35: PS: NVVDD PH3&5











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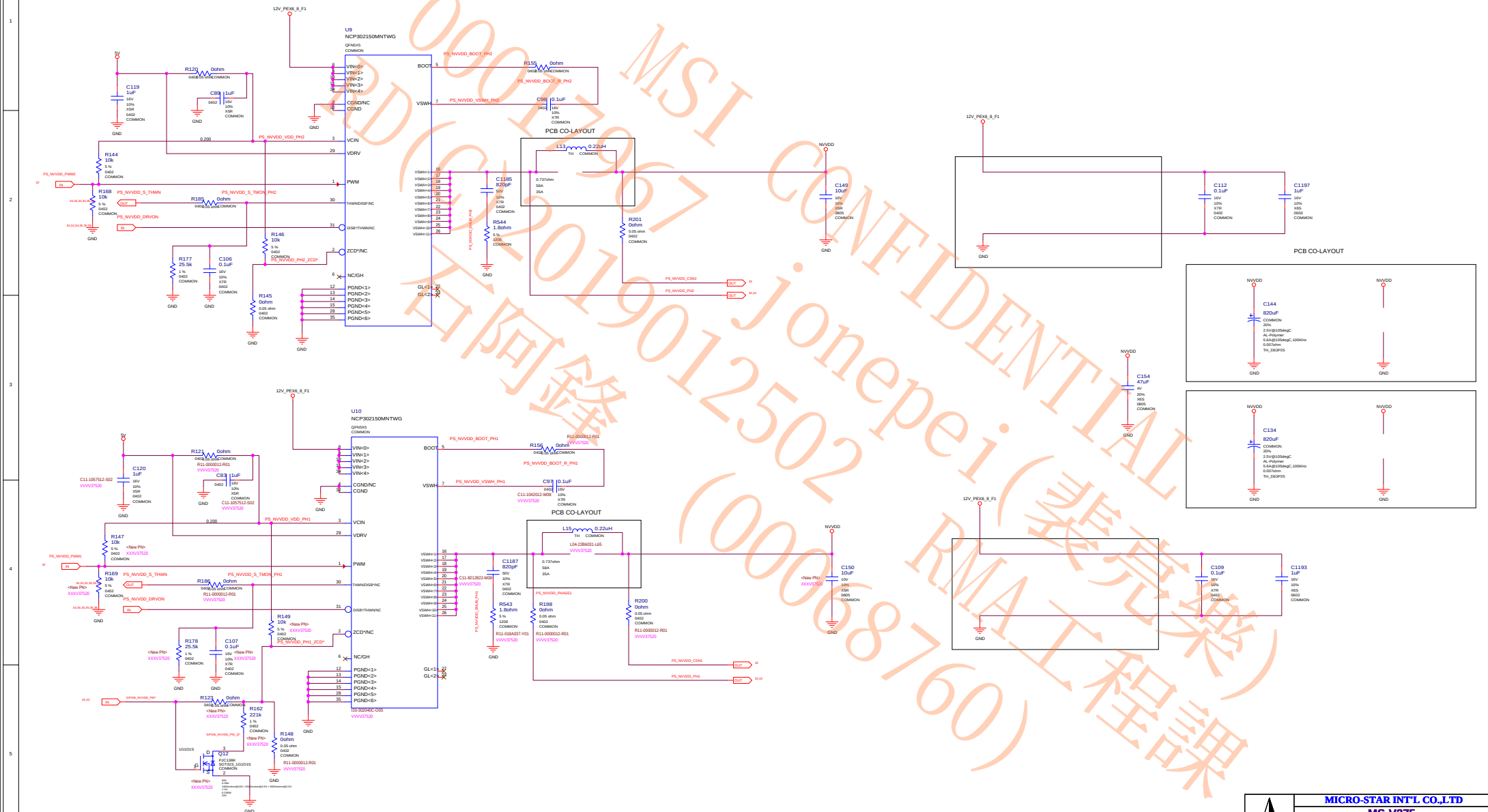
Page36: PS: NVVDD PH2&1





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# DELETE RAIL BALANCE CIRCUIT

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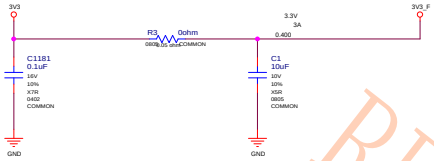
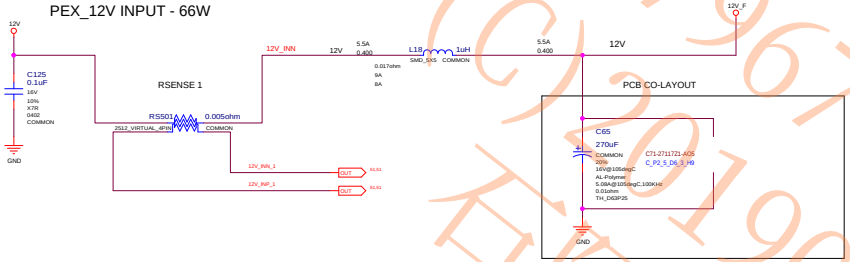
# Page38: PS: Inputs, Filtering, and Monitoring

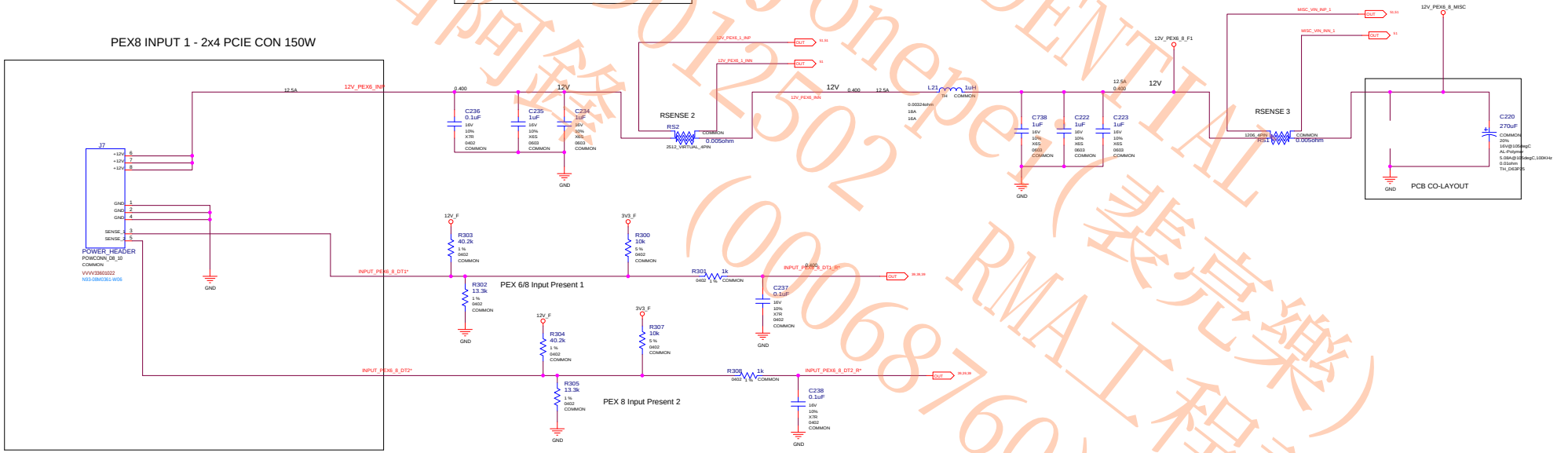
## PEX 3V3 INPUT - 10W




## PEX_12V INPUT - 66W




## PEX8 INPUT 1 - 2x4 PCIE CON 150W





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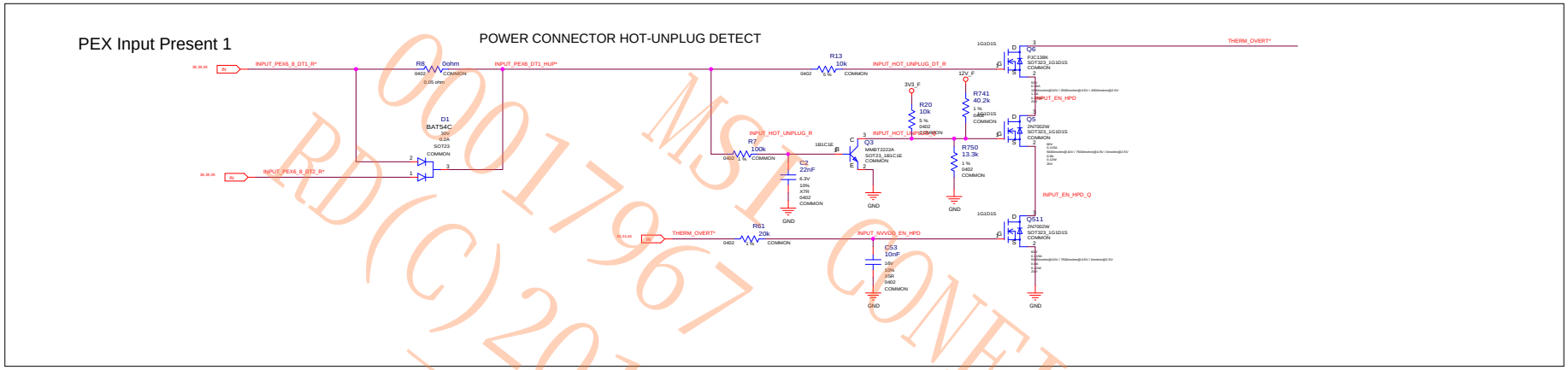
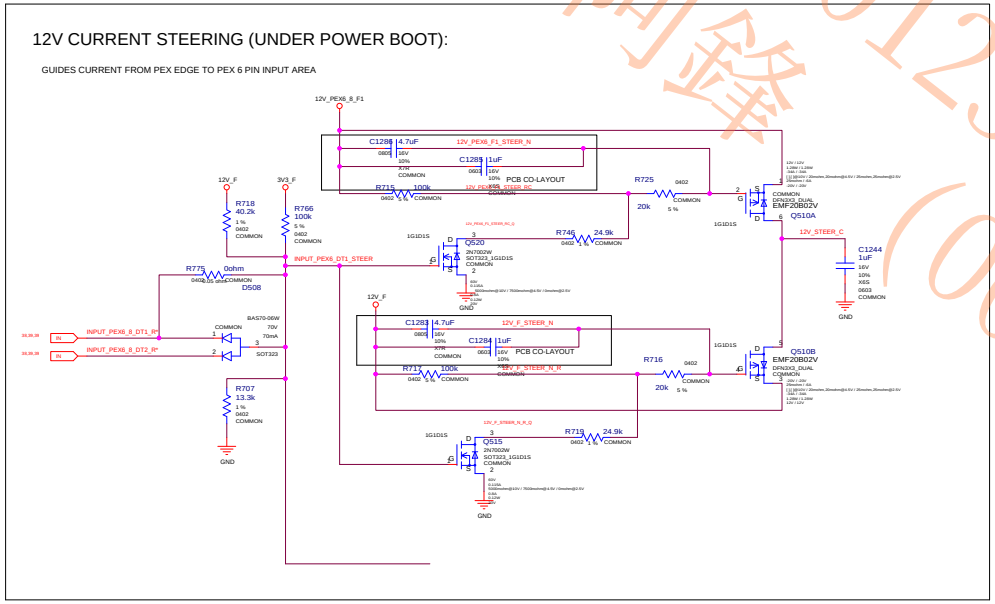
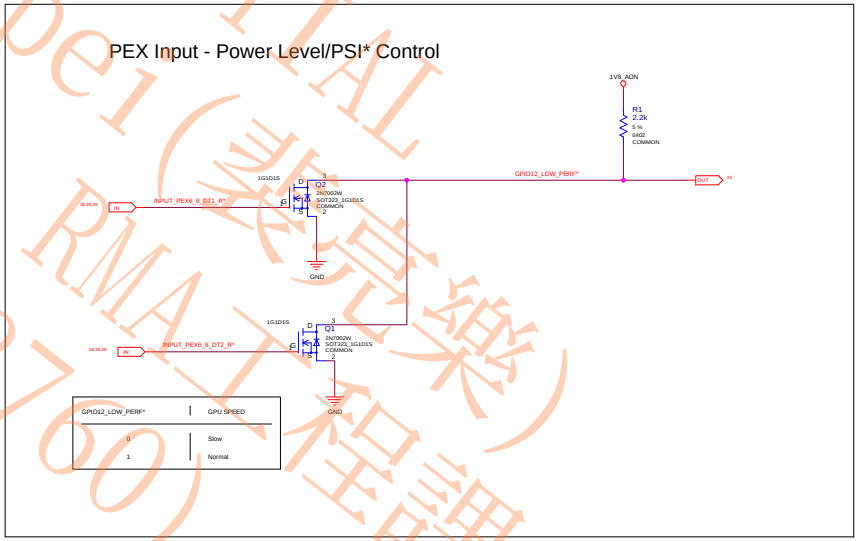
Page39: PS: HOT-UNPLUG, UNDER POWER BOOT, CURRENT STEERING

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| Size: Custom | Document Description: Page39: HOT-UNPLUG, CURRENT STEERING | Rev: 1.0 |
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Page40: BUCKBOOST

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Page41: PPC

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Page42: 12V & 3V3_A SWITCHER

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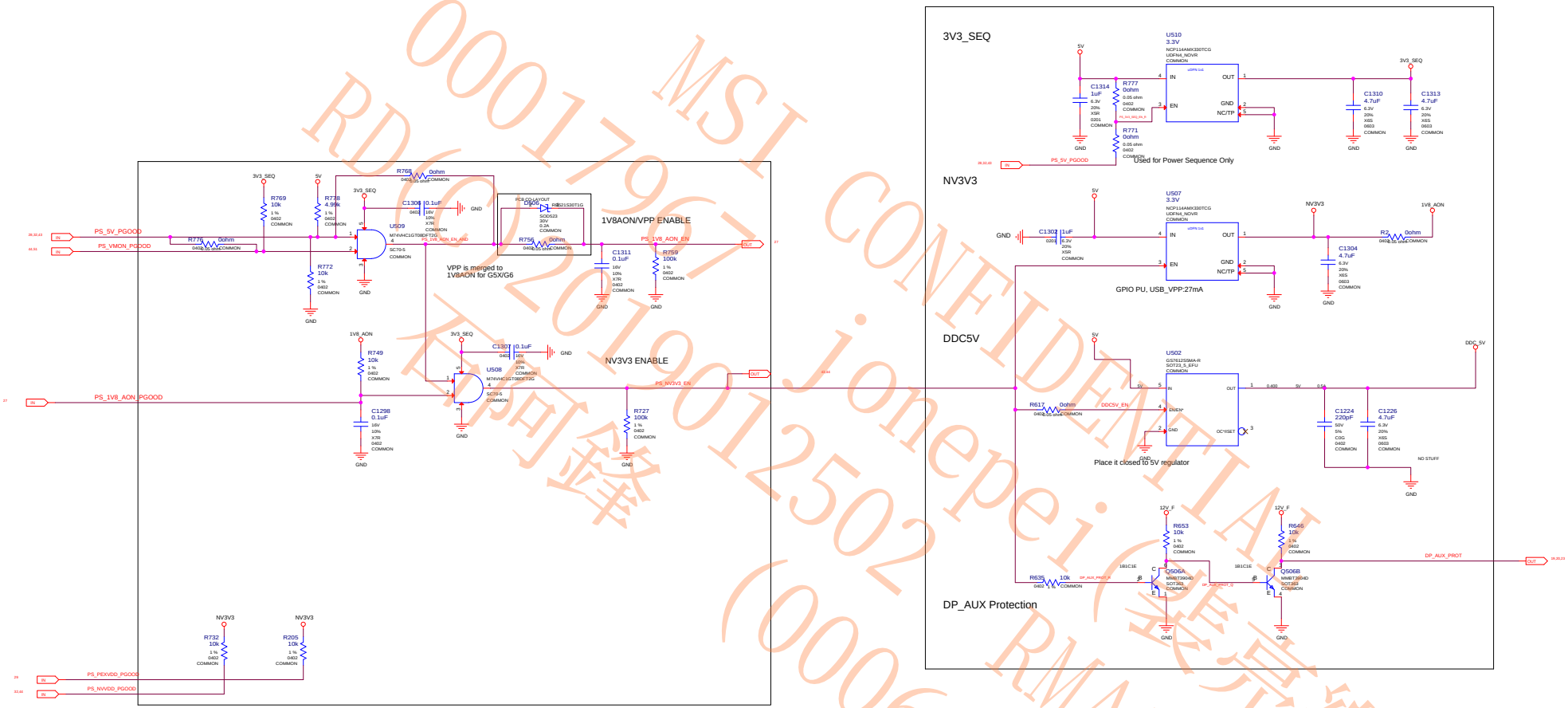
Page43: SEQ:5V,1V8,NV3V3 ENABLE





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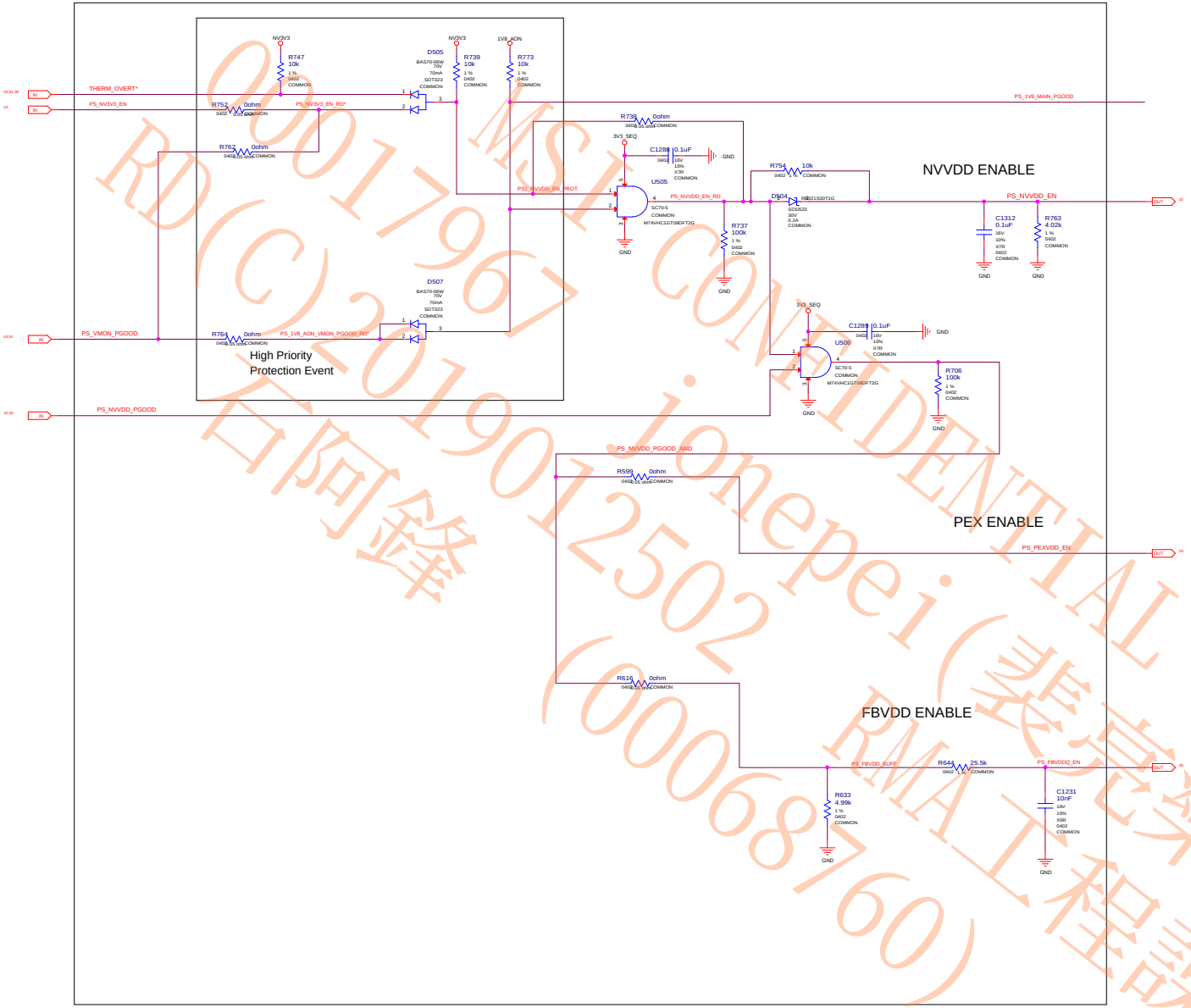
Page44: SEQ:NV,PEX,FB ENABLE

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Page45: SEQUENCE:Voltage Monitor

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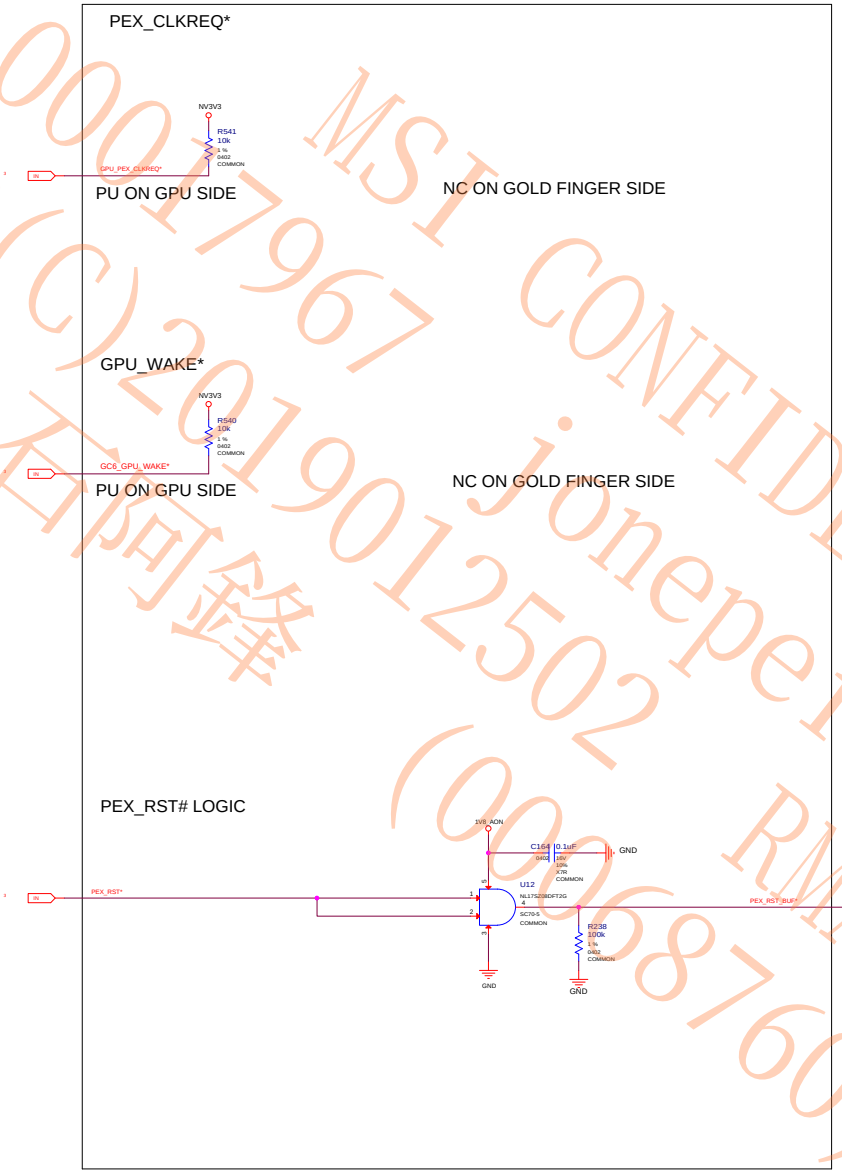
Page47: SEQUENCE:MISC





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Page48: LOGO LED

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Page49: LED DRIVER & Boost

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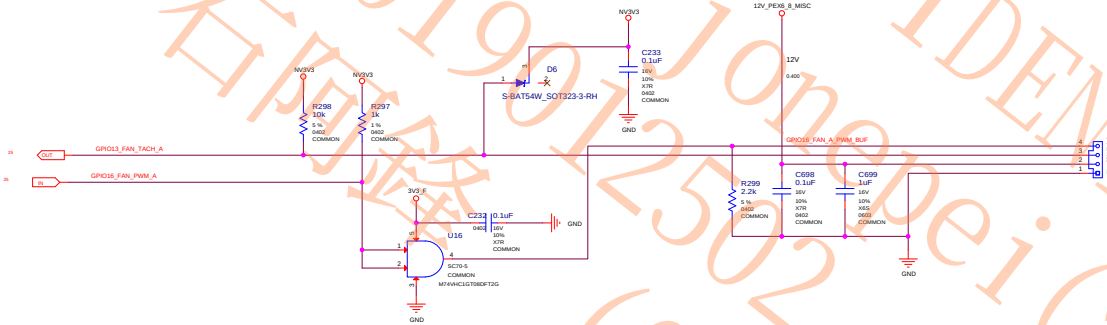
Page50: FAN

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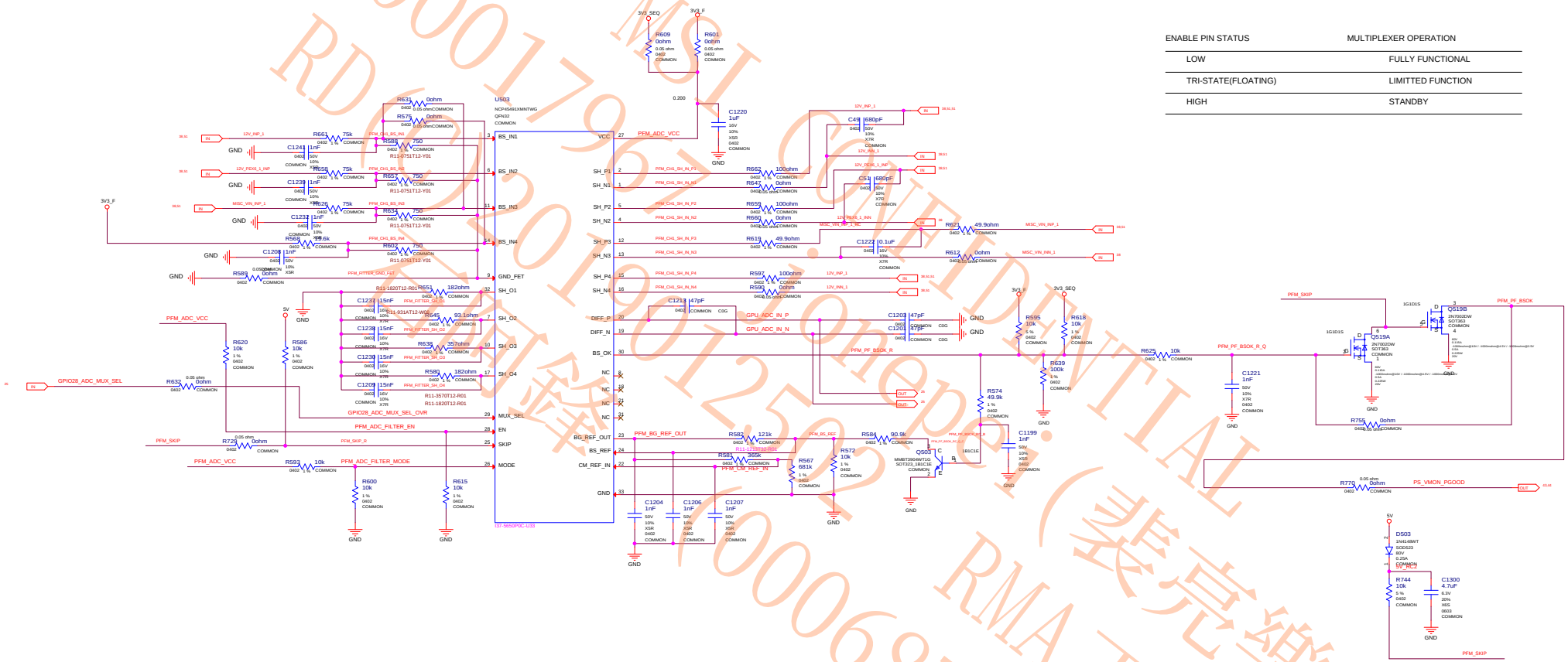
Page51: PWR SENSE

| MODE PIN STATUS | MULTIPLEXER OPERATION |
|---|---|
| LOW | DEVICE A |
| TRI-STATE(FLOATING) | STAND-ALONE |
| HIGH | DEVICE B |

| ENABLE PIN STATUS | MULTIPLEXER OPERATION |
|---|---|
| LOW | FULLY FUNCTIONAL |
| TRI-STATE(FLOATING) | LIMITTED FUNCTION |
| HIGH | STANDBY |





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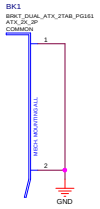
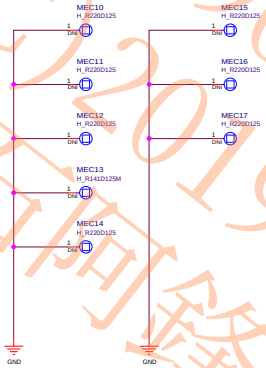
# Page52: MECH

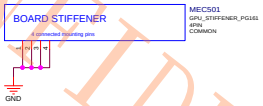
Bracket:

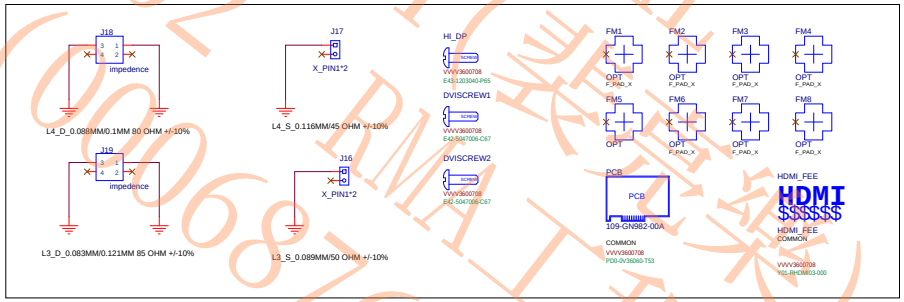



Mechanical Holes Symbol




BACK STIFFENER:





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Page53: PTC

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