<variant Name>

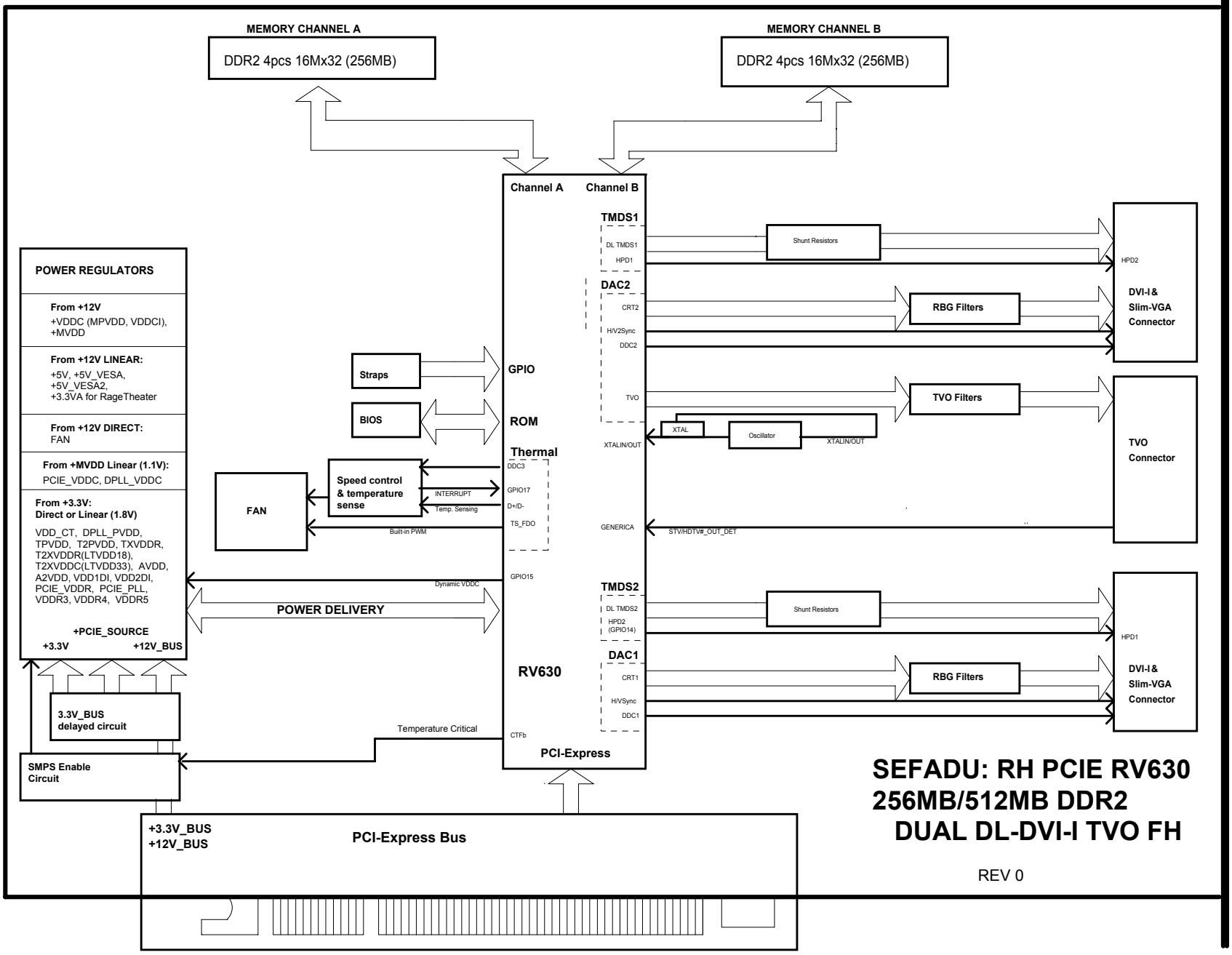
| Title | Schematic No. | Date: |
|---|---|---|
| RV630 DDR2-REVISION HISTORY | 105-B149xx-00 | Friday, April 13, 2007 |

# REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact ATI representative to obtain latest BOM closest to the application desired.**

Rev 4

| Sch Rev | PCB Rev | Date | REVISION DESCRIPTION |
|---|---|---|---|
| 0 | 00A | 06/11/17 | Initial design for RV630 DDR2 |
| 1 | 00B | 07/01/26 | THIS IS A TEST BOARD, WE WILL BASE ON THIS ONE TO DECIDE WHICH WAY WE SHOULD GO<br>1) CHANGING RGB CONFIGURATION FOR BOTH DAC1 AND DAC2 (PAGE 3, 14 AND 15)<br>2) ADD-IN Q102 AND R49 FOR VDDR3 POWER SEQUENCE CONTROL<br>3) CONNECT R847 TO +1.8V_D1 INSTEAD OF +1.8V_LDO2 (PAGE 13)<br>4) LVTM LAYOUT CHANGES TO IMPROVE SI |
| 2 | 00C | 07/02/08 | 1) COME BACK AND START AS REV. A SINCE REV. B DOES NOT WORK ON CRT SIGNALS, EXCEPT THE LAYOUT ON LVTM TO IMPROVE SI<br>2) ADD-IN Q102 AND R49 FOR VDDR3 POWER SEQUENCE CONTROL<br>3) CONNECT R847 TO +1.8V_D1 INSTEAD OF +1.8V_LDO2 (PAGE 14)<br>4) ADD-IN SINGLE PHASE POWER SUPPLY DUE TO POWER MEASUREMENT IS LOWER THAN ESTIMATE (PAGE 10)<br>5) REMOVE JU57 AND ADD-IN SW1 TO SUPPORT JTAG CONNECTOR TJ47 (GPIO5) (PAGE 7) |
| 3 | 00D | 07/03/12 | 1) REMOVE RP702 AND RP703. REPLACE BY R724 (PAGE12). IT'S FOR DFM RECOMMENDATION (NO TECHNICAL REASON)<br>2) ADD-IN R4010 AND C4010 FOR 2-PIN CONTROLLER TO USE INTERNAL PWM (PAGE 18) |
| 4 | 00 | 07/04/02 | 1) NO SCHEMATIC CHANGE. ONLY MOVE R1206 CLOSE TO U703 TO IMPROVE THE FB LINE (TOO LONG). R1206 IS NOT POPULATED ON BOM |




# SEFADU: RH PCIE RV630 256MB/512MB DDR2 DUAL DL-DVI-I TVO FH

REV 0

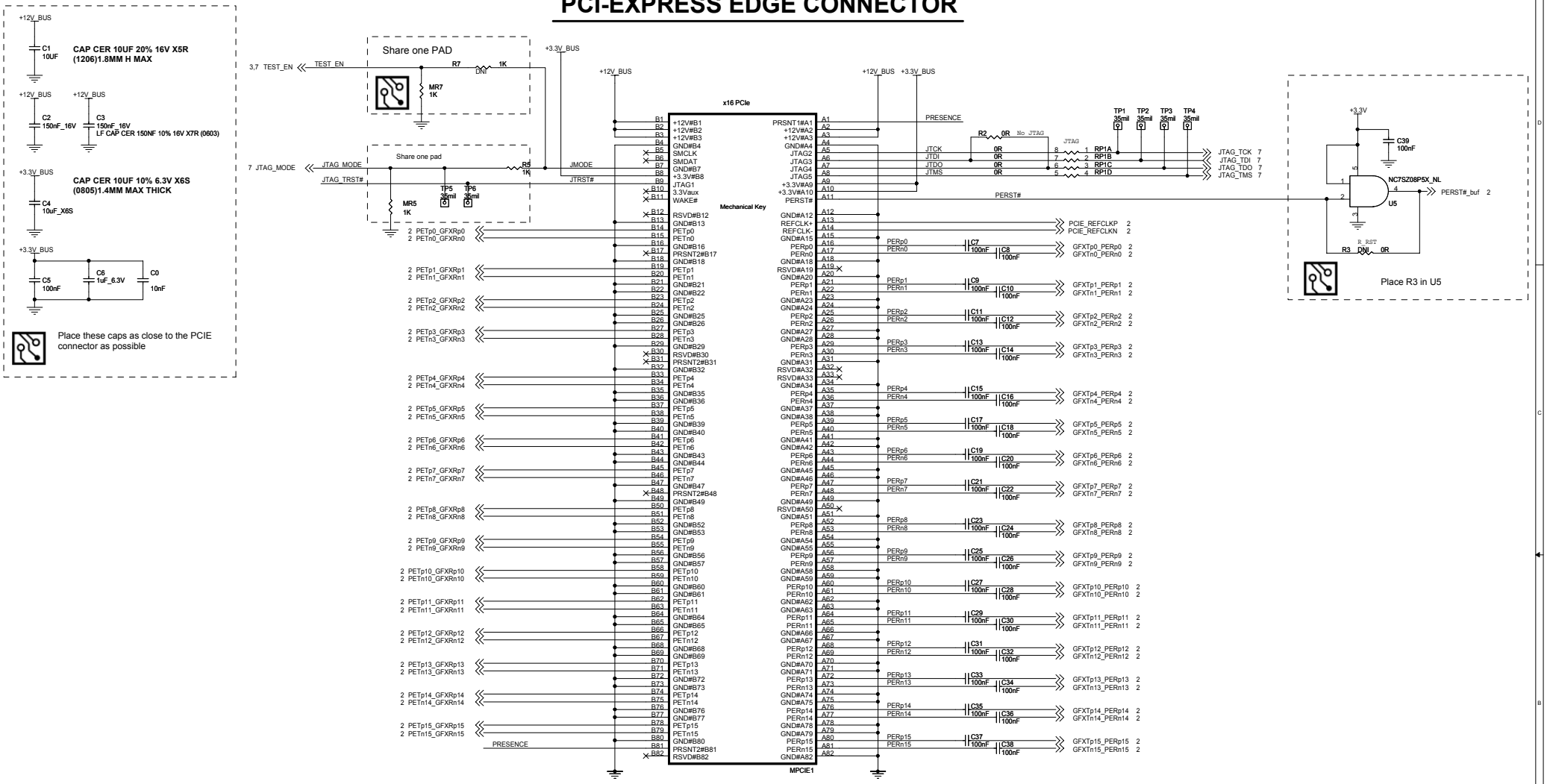
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title: RV630 DDR2-BLOCK DIAGRAM

| Size | Document Number | Rev |
|---|---|---|
| C | 105-B149xx-00 | 4 |

Date: Friday, April 13, 2007 Sheet 21 of 21

# PCI-EXPRESS EDGE CONNECTOR




SYMBOL LEGEND

| | |
|---|---|
| DNI | DO NOT INSTALL |
| # | ACTIVE LOW |
| | DIGITAL GROUND |
| | ANALOG GROUND |
| BUO | BRING UP ONLY |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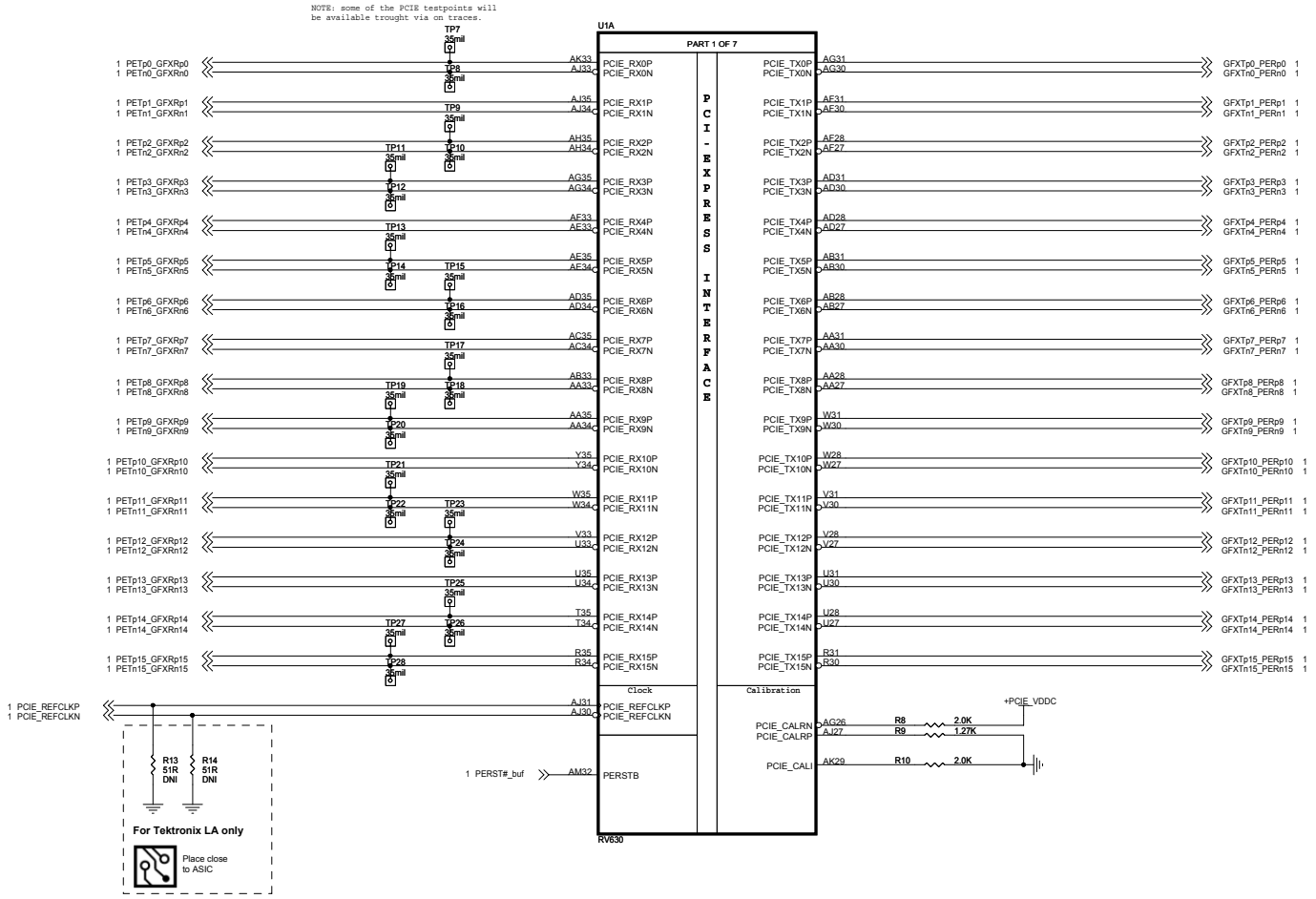
| | | | |
|---|---|---|---|
| Title | RH PCIE RV630 DDR2- PCIE CONNECTOR | | |
| Size C | Document Number 105-B149xx-00 | | Rev 4 |
| Date: Friday, April 13, 2007 | Sheet 1 of 21 | | |




| | |
|---|---|
| Company | ATI Technologies Inc. |
| Address | 1 Commerce Valley Drive East<br>Markham, Ontario<br>Canada, L3T 7X6<br>(905) 882-2600 |
| Title | RV630 DDR2- ASIC PCIE I/F |
| Size | C |
| Document Number | 105-B149xx-00 |
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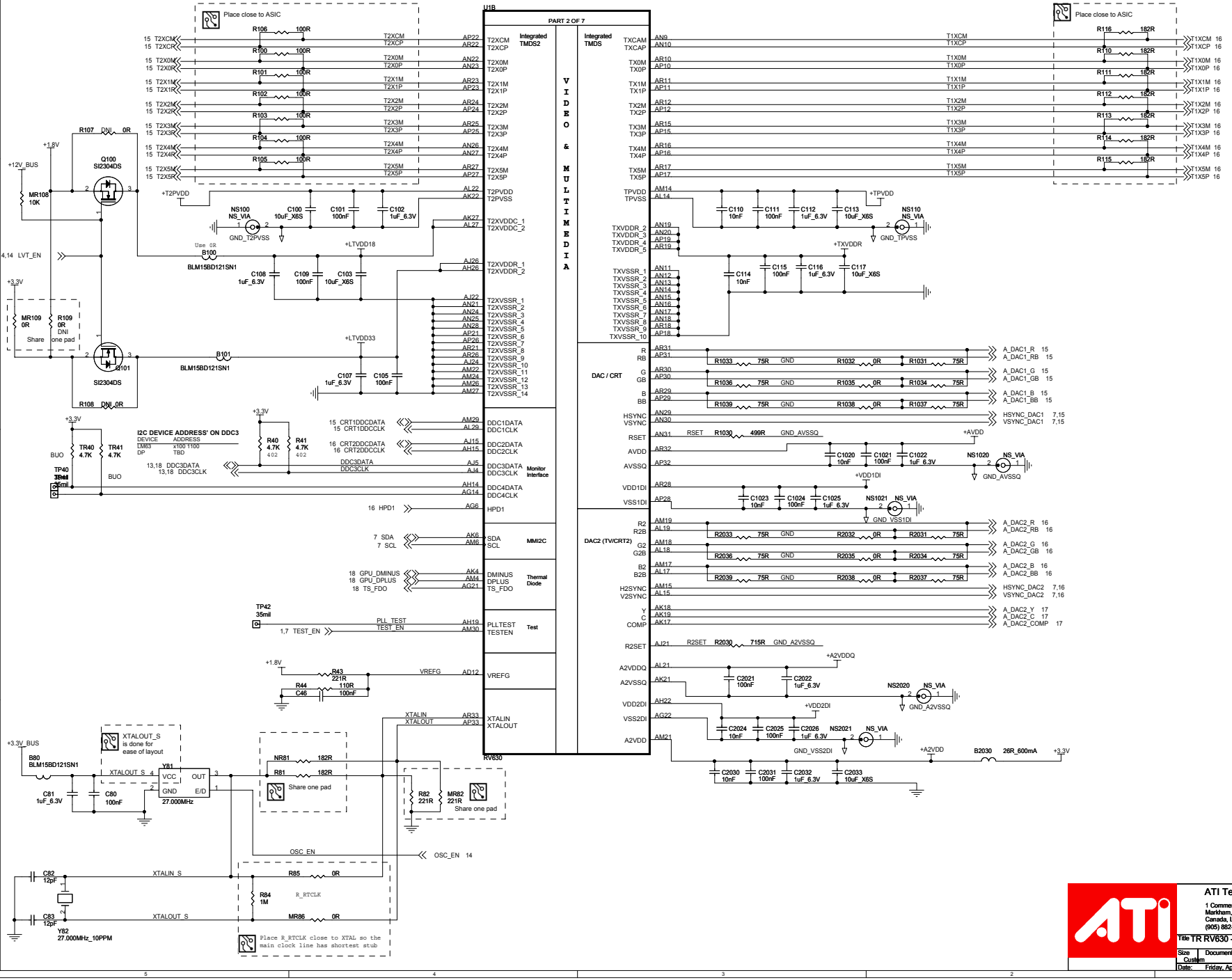
| Date: | Friday, April 13, 2007 |
| Sheet | 2 of 21 |

**Recommended caps:**
**(see BOM for qualified values/vendors)**
**10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK**
**1uF, X6S, 10%, 0402, 6.3V**
**100nF, X7R, 10%, 0402**
**10nF , X7R, 10%, 0402**



**Recommended caps:**
**(see BOM for qualified values/vendors)**
**10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK**
**1uF, X6S, 10%, 0402, 6.3V**
**100nF, X7R, 10%, 0402**
**10nF , X7R, 10%, 0402**

U1E

PART 5 OF 7

Memory I/O

POWER

PCI-Express

Core

Selected PLL's

Mechanical Pins

RV630

+MVDD
C150 10nF, C151 10nF, C152 10nF, C154 10nF, C155 10nF, C157 10nF, C158 10nF, C159 10nF
C156 100nF, C130 100nF, C131 100nF, C132 100nF, C133 100nF, C134 100nF, C135 100nF, C136 100nF, C137 100nF, C138 100nF, C139 100nF
C153 1uF_6.3V, C140 1uF_6.3V, C141 1uF_6.3V, C142 1uF_6.3V, C143 1uF_6.3V, C144 1uF_6.3V, C145 1uF_6.3V, C146 1uF_6.3V, C147 1uF_6.3V, C148 1uF_6.3V, C149 1uF_6.3V
C124 10uF_X6S, C125 10uF_X6S, C126 10uF_X6S, C127 10uF_X6S, C128 10uF_X6S, C129 10uF_X6S

A8 VDDR1_1, H35 VDDR1_2, L22 VDDR1_3, M1 VDDR1_4, M10 VDDR1_5, M35 VDDR1_6, P10 VDDR1_7, T1 VDDR1_8, Y1 VDDR1_9, A12 VDDR1_10, A16 VDDR1_11, A20 VDDR1_12, A24 VDDR1_13, A28 VDDR1_14, B1 VDDR1_15, B35 VDDR1_16, D1 VDDR1_17, D35 VDDR1_18, H1 VDDR1_19, K10 VDDR1_20, K12 VDDR1_21, K24 VDDR1_22, K26 VDDR1_23, L14 VDDR1_24, L15 VDDR1_25, L17 VDDR1_26, L18 VDDR1_27, L19 VDDR1_28, L21 VDDR1_29

+MVDD, B120 BLM15BD121SN1, C120 1uF_6.3V, NS120 NS_VIA, GND_VSSRHA, B123 BLM15BD121SN1, C123 1uF_6.3V, NS123 NS_VIA, GND_VSSRHB

A25 VDDRHA_1, A32 VDDRHA_2
B2 VDDRHB_1, L1 VDDRHB_2
B25 VSSRHA_1, B32 VSSRHA_2
C2 VSSRHB_1, L2 VSSRHB_2

+3.3V, R90 0R, Q90 SI2304DS, 3,14 LVT_EN

+VDDR_3
C90 1uF_6.3V, C91 100nF, C92 1uF_6.3V, C93 100nF
AE14 VDDR3_1, AE15 VDDR3_2, AE17 VDDR3_3, AE12 VDDR3_4

+3.3V
C94 10uF_X6S, C95 1uF_6.3V, C97 100nF, C96 1uF_6.3V, C98 100nF
AP2 VDDR4_1, AR2 VDDR4_2
AN1 VDDR5_1, AP1 VDDR5_2

+DPLL_PVDD
C70 1uF_6.3V, C71 100nF, C72 10uF_X6S
NS70 NS_VIA, GND_PVSS
AR20 DPLL_PVDD, AP20 DPLL_PVSS

A35 MECH_1, AR1 MECH_2, AR35 MECH_3

+PCIE_PVDD, B930 BLM15BD121SN1, +1.8V
C930 1uF_6.3V, C931 100nF, C932 10uF_X6S
NS18 NS_VIA, GND_PCIE_PVSS
AM35 PCIE_PVDD, AM34 PCIE_PVSS

R26 PCIE_VDDC_1, W25 PCIE_VDDC_2, W26 PCIE_VDDC_3, AA25 PCIE_VDDC_4, AA26 PCIE_VDDC_5, AB25 PCIE_VDDC_6, AB26 PCIE_VDDC_7, AD26 PCIE_VDDC_8, AF26 PCIE_VDDC_9, U26 PCIE_VDDC_10, V25 PCIE_VDDC_11, V26 PCIE_VDDC_12

+PCIE_VDDC
C920 1uF_6.3V, C921 1uF_6.3V, C922 1uF_6.3V, C923 1uF_6.3V, C924 1uF_6.3V, C925 1uF_6.3V, C926 10uF_X6S

+VDDC, B920 220R_2A, Install only one of these two, R920 0R, +1.1V

AL33 PCIE_VDDR_1, AM33 PCIE_VDDR_2, AN33 PCIE_VDDR_3, AN34 PCIE_VDDR_4, AN35 PCIE_VDDR_5, AP34 PCIE_VDDR_6, AP35 PCIE_VDDR_7, AR34 PCIE_VDDR_8

+PCIE_VDDR, +1.8V, R900 0R
C900 10nF, C901 100nF, C902 1uF_6.3V, C903 10nF, C904 100nF, C905 1uF_6.3V, C906 1uF_6.3V, C907 1uF_6.3V

N13 VDDC_1, R18 VDDC_2, W11 VDDC_3, AB19 VDDC_4, AC23 VDDC_5, AE18 VDDC_6, AE19 VDDC_7, AE21 VDDC_8, AE22 VDDC_9, N15 VDDC_10, N18 VDDC_11, N21 VDDC_12, N23 VDDC_13, P14 VDDC_14, P17 VDDC_15, P19 VDDC_16, P22 VDDC_17, R13 VDDC_18, R15 VDDC_19, R21 VDDC_20, R23 VDDC_21, U14 VDDC_22, U17 VDDC_23, U19 VDDC_24, U22 VDDC_25, V15 VDDC_26, V18 VDDC_27, V21 VDDC_28, V23 VDDC_29, W14 VDDC_30, W17 VDDC_31, W19 VDDC_32, W22 VDDC_33, AA15 VDDC_34, AA18 VDDC_35, AA21 VDDC_36, AA23 VDDC_37, AB14 VDDC_38, AB17 VDDC_39, AB22 VDDC_40, AC13 VDDC_41, AC15 VDDC_42, AC18 VDDC_43, AC21 VDDC_44

+VDDC
C161 1uF_6.3V, C162 1uF_6.3V, C163 1uF_6.3V, C164 1uF_6.3V, C165 1uF_6.3V, C166 1uF_6.3V, C167 1uF_6.3V, C168 1uF_6.3V, C169 1uF_6.3V, C170 1uF_6.3V, C181 10uF_X6S, C182 10uF_X6S, C183 10uF_X6S
C171 1uF_6.3V, C172 1uF_6.3V, C173 1uF_6.3V, C174 1uF_6.3V, C175 1uF_6.3V, C176 1uF_6.3V, C177 1uF_6.3V, C178 1uF_6.3V, C179 1uF_6.3V, C180 1uF_6.3V
C160 1uF_6.3V, C184 1uF_6.3V, C185 1uF_6.3V, C186 1uF_6.3V, C187 10uF_X6S, C188 10uF_X6S, C189 10uF_X6S

+VDDC
U13 BBP_1, V13 BBP_2

M12 VDDCI_1, M24 VDDCI_2, P11 VDDCI_3, P25 VDDCI_4

+VDDCI, B77 220R_2A, +VDDC
C73 100nF, C76 1uF_6.3V, C74 100nF, C75 1uF_6.3V, C77 10uF_X6S

R11 VDD_CT_1, R25 VDD_CT_2, U11 VDD_CT_3, U25 VDD_CT_4, AA11 VDD_CT_5, AB11 VDD_CT_6, AD10 VDD_CT_7, AF10 VDD_CT_8

+1.8V
C78 100nF, C79 100nF, C68 100nF, C69 100nF

A14 MPVDD, B15 MPVSS, AG19 DPLL_VDDC

+MPVDD, B67 26R 600mA, +VDDC
C64 10nF, C65 100nF, C66 1uF_6.3V, C67 10uF_X6S
NS_VIA NS64, GND_MPVSS

+DPLL_VDDC
C60 1uF_6.3V, C61 100nF, C62 10uF_X6S
GND_PVSS

Install only one of these two
B60 BLM15BD121SN1, +1.1V
MB60 BLM15BD121SN1, +VDDC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Title: RV630 DDR2- ASIC POWERS

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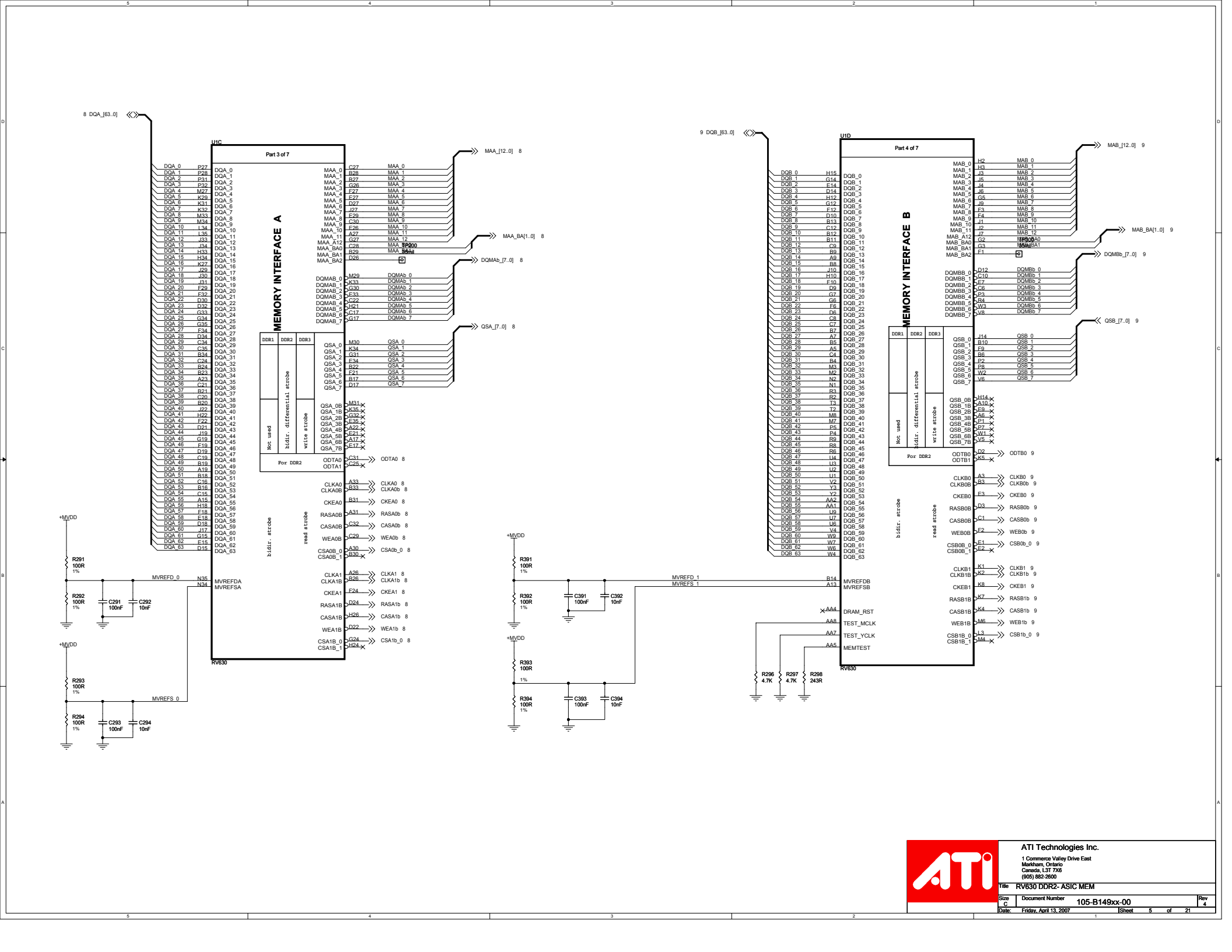



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Title: RV630 DDR2- ASIC MEM

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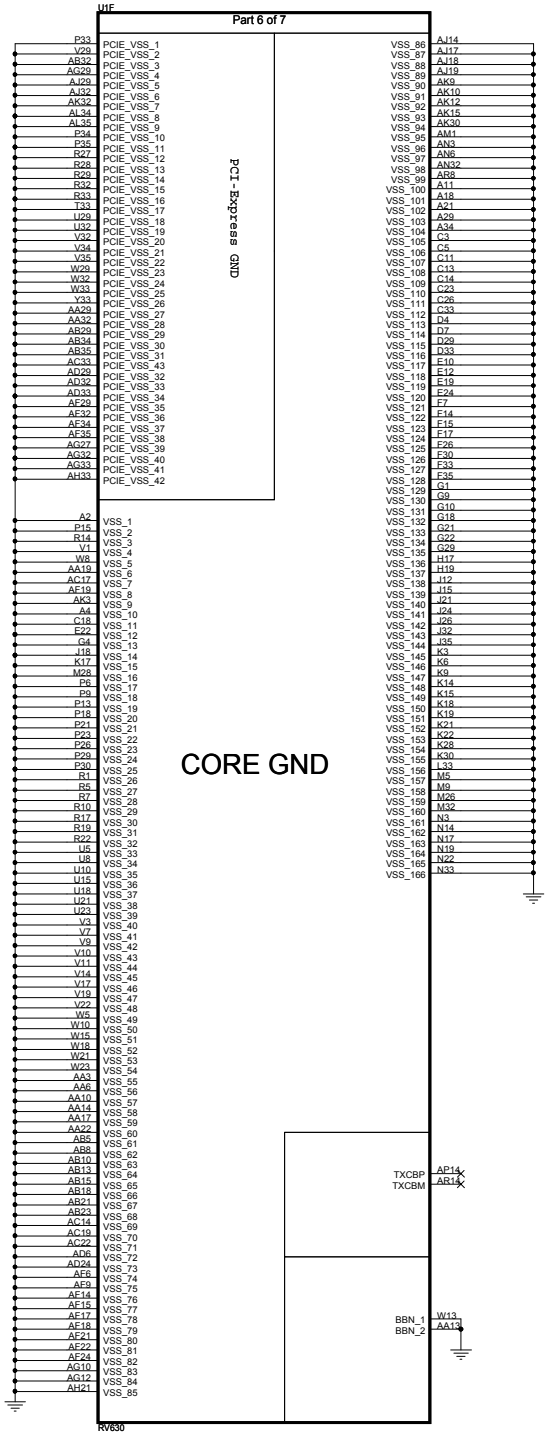


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Title: RV630 DDR2- ASIC GROUNDS

| Size | Document Number | Rev |
|---|---|---|
| C | 105-B149xx-00 | 4 |

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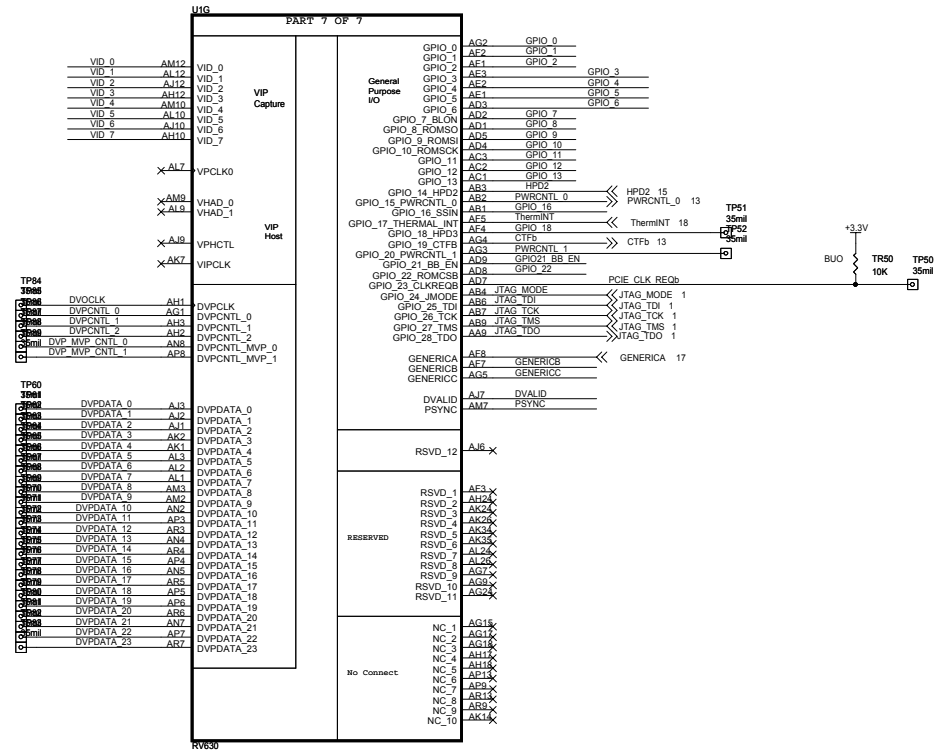
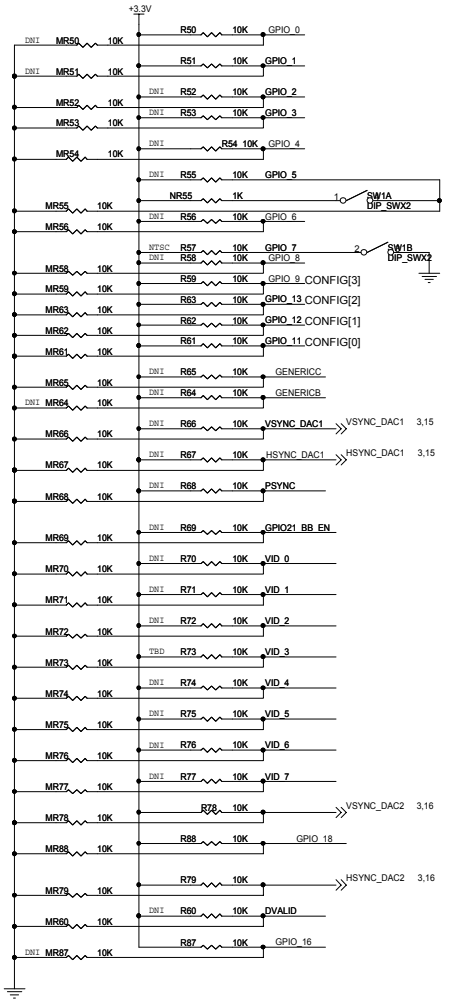



## PIN BASED STRAPS




GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

ATI Internal Use Only - Reserved (Default: 00)

DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

ATI Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0]
0010 - 512Kbit AT25F512A (Atmel)
0011 - 1Mbit AT25F1024A (Atmel)
0100 - 512Kbit M25P05A (ST)
0101 - 1Mbit M25P10A (ST)
0101 - 2Mbit M25P20 (ST)
0100 - 512Kbit Pm25LV512 (Chingis)
0101 - 1Mbit Pm25LV010 (Chingis)

ATI Internal Use Only - Reserved (Default: 0)

VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

ATI Internal Use Only - Reserved

VGA DISABLE : 1 for disable (set to 0 for normal operation)

ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

MSI_DIS (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

BIF_AUDIO_EN
0 - Disable HD Audio 1- Enable HD Audio

ATI Internal Use Only - Reserved (Default: 0)

64BAR_EN_A (Default: 0)

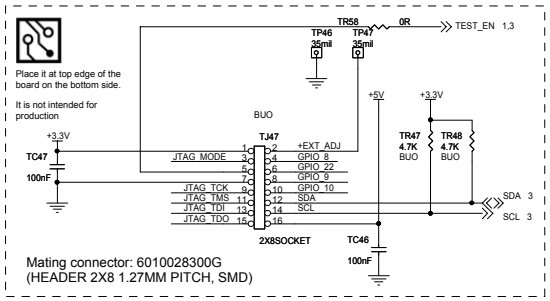
ATI Internal Use Only - Reserved (Default: 0)

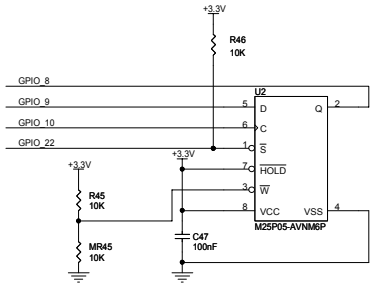
ATI Internal Use Only - Reserved (Default: 0)

MEMORY CONFIG ATI Board Feature I
VSYNC_DAC2 CHECK ATI MEMORY
GPIO18 TUNING DOCUMENT

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

Pull-Down Resistors are for BU until built-in pull-downs are verified.





113-B149XX-XXX
VIDEO BIOS FIRMWARE

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| | | | |
|---|---|---|---|
| Title | RV630 DDR2- ASIC DVO-BOOT SRAPS | | |
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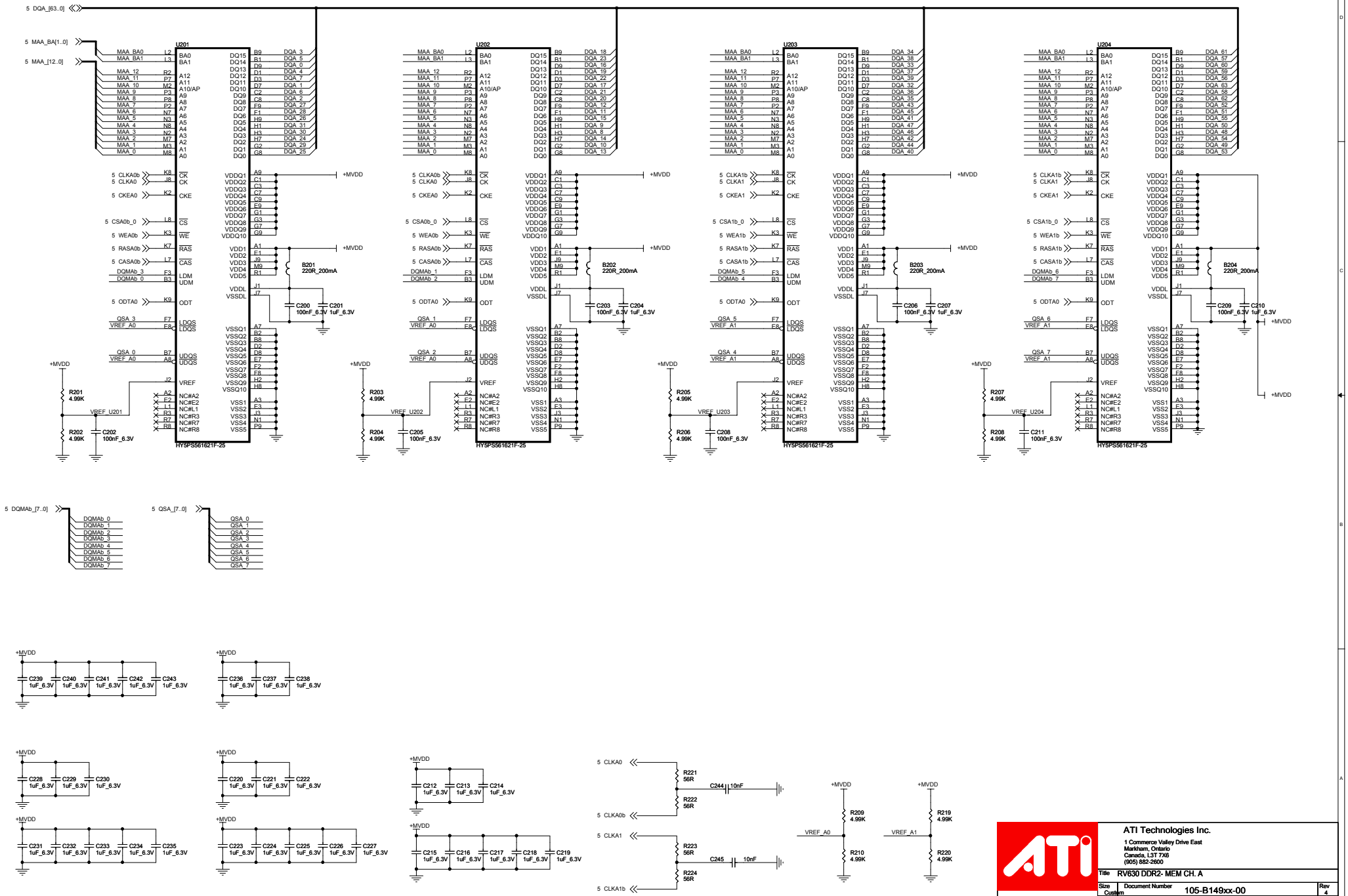
# CHANNEL A: 128MB/256MB DDR2

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| | | |
|---|---|---|
| Title | RV630 DDR2- MEM CH. A | |
| Size: Custom | Document Number: 105-B149xx-00 | Rev: 4 |
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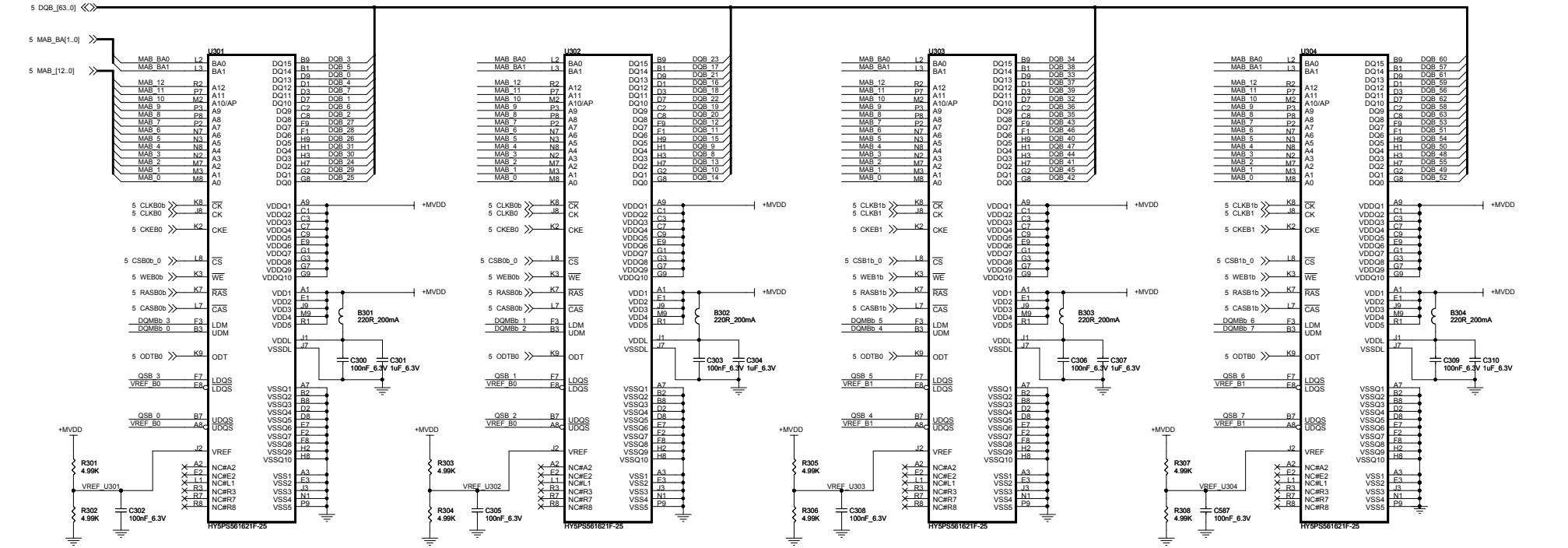
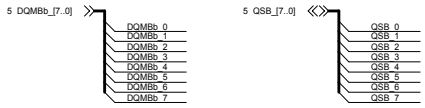
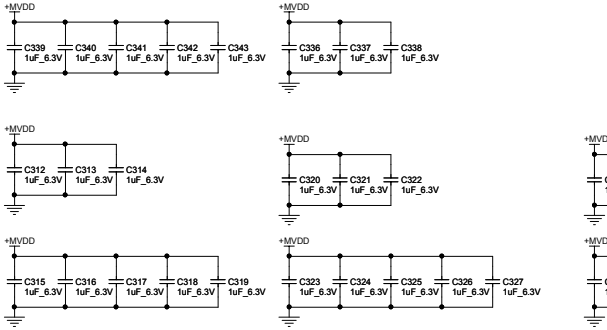
# CHANNEL B: 128MB/256MB DDR2

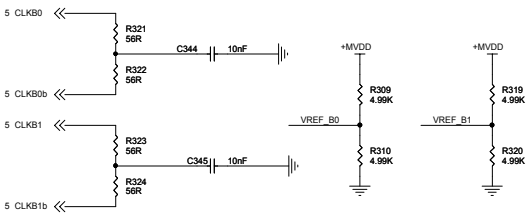










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| | | |
|---|---|---|
| Title | RV630 DDR2- MEM CH. B | |
| Size: C | Document Number: 105-B149xx-00 | Rev: 4 |
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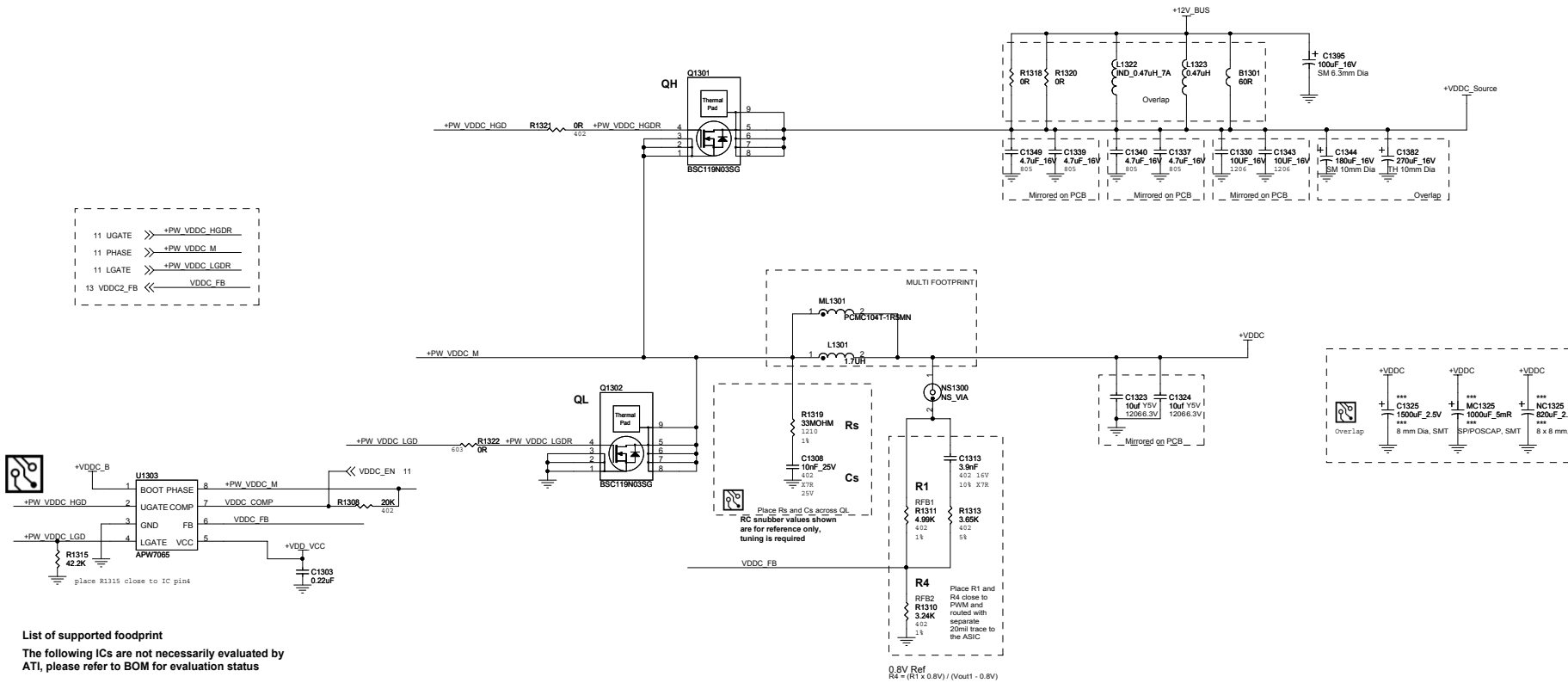


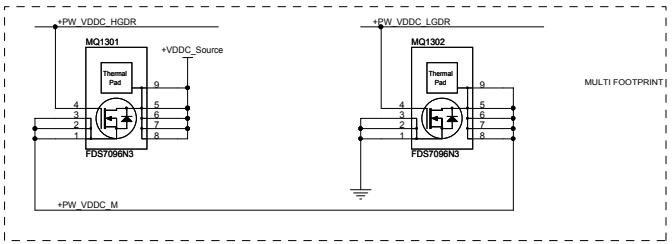

**List of supported foodprint**

**The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status**

**ANPEC APW7120/APW7065 (12V)**
**CAT CAT7583 (12V)**
**INTERSIL ISL6545**
**NEXSEM NX2114/2307**
**RICHTEK RT9214/RT8101**
**OnSemi ON1582**
**uPI UP6101 (No Ext_Vref in)**

Layout guideline for Nexsem NX2114/2307

1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW_MVDDC_LGD and PW_MVDDC_HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



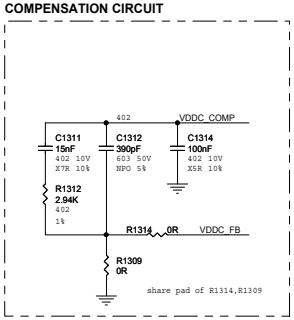

**SMPS02- Regulator for VDDC**
**Vout = 0.9V ~ 1.1V**

| Part | Vout | RFB1 | RFB2 |
|---|---|---|---|
| 0.8V Ref | 2.03V (1.98V~2.08V) | 4.99K p/n 3160499100G | 3.24K p/n 3160324100G |
| | | | |
| | | | |

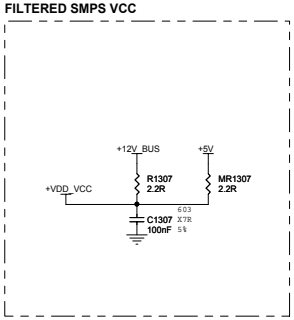
## SMPS02 Specifications

| | Nominal Value ; Tolerance | Adjustable range / Notes |
|---|---|---|
| Vin (power stage) | 12V ; +/-8% PCIe | ATX12V ver. 2.2 +/-5% |
| Vout | 2V ; +2%/-2% | 1.8V ~ 2.85V |
| Vout ripple (DC) | 50mVpp | |
| Iout | 6Aavg, 8Adc max | |
| Step load | 3Amax | |
| Vout ripple (AC) | +/-10% or 200mVpp @ 3A step load | |
| Switching Freq. | ~300kHz | TBD |
| Protections | | |

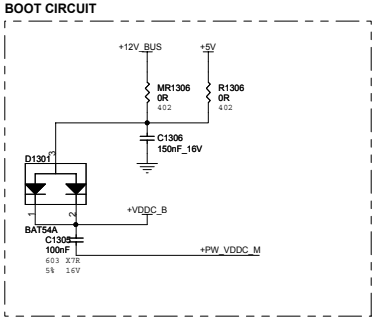
**COMPENSATION CIRCUIT**




**FILTERED SMPS VCC**




**BOOT CIRCUIT**

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## Information on Compatable Controller Parts

| | PWM IC #1 | PWM IC #2 | PWM IC #3 | PWM IC #4 | |
|---|---|---|---|---|---|
| Gate drive voltage | 5V, 8V, 12V | 5V, 8V, 12V | 5V only | 12V only | |
| Vref | 0.6V | 0.6V | 0.6V | 0.6V | |
| Bootstrap diodes | Internal (DNP D601, D611) | Internal (DNP D601, D611) | External (Populate D601, D611) | Internal (DNP D601, D611) | |
| Phase current adjustable (unbalanced between phases) | Yes | Yes | Yes | TBD | |
| Option Pin Selection | | | | | |
| Pin 10 (IOUT/IMAX/DROOP) | IOUT/DROOP (R662) | IOUT/IMAX | IOUT | IOUT/IMAX | |
| Pin 11 (RT) | R_RT -= 10,000,000/Fsw | TBD | R_RT -= 18,600,000/Fsw | TBD | |
| Pin 12 (COMP/DROOP) | COMP | DROOP (R663) | COMP | COMP | |
| Pin 14 (SS/ICOMP) | SS/EN | GND (SS fixed internally) | ICOMP (SS dependent on Fsw) | SS | |
| Pin 16 (REFOUT/POK) | POK (Open drain) | IREFOUT/POK POK voltage = 1.2V | INREFOUT/POK PGood voltage = 1.25V | INREFOUT/PGOOD Vrefout = 0.6V | |
| Pin 21 (VCCDRV/DROOP) | VCCDRV | VCCDRV | DROOP (R664) | DROOP (R664) | |

## Choosing Different Gate Drive

| Gate Drive | Populate | Do Not Populate |
|---|---|---|
| 5V Gate Drive | R631, R632 | R630, R670, C660, R661, Q661 |
| 8V Gate Drive | R630, C660, R661, Q661 | R631, R632, R670 |
| 12V Gate Drive | R630, C660, R670 | R631, R632, R661, Q661 |

## External Detection Circuit and Indication

| Cases | Behaviour | Notifications |
|---|---|---|
| External cable not plugged in +12V_BUS not in regulation | 12V_EXT_DETb = X<br>EN1 -> "0" (by R12)<br>ENb1 -> 3.3V<br>ENBUS = "0" | VDDC disabled |
| External cable not plugged in +12V_BUS in regulation | 12V_EXT_DETb = "1"<br>EN1 -> 3V (by R11 and R12)<br>ENb1 = 0V<br>ENBUS = "1" | VDDC enabled<br>External Power Missing |
| External cable plugged in +12V_XXX not in regulation | 12V_EXT_DETb = "0"<br>EN1 < 3V (due to low 12V)<br>ENb1 = 3.3V<br>ENBUS = "0" | VDDC disabled |
| External cable plugged in +12V_XXX in regulation | 12V_EXT_DETb = "0"<br>EN1 -> 3V<br>ENb1 = 0V<br>ENBUS = "1" | VDDC enabled<br>Normal Operation |

## SMPS03 Specifications

| | Nominal Value | Tolerance | Adjustable range / Notes |
|---|---|---|---|
| Vin (power stage) | 12V | +/-8% PCIe | ATX12V ver. 2.2 +/-5% |
| Vout | 1.2V | +2.5%/-2.5% | 0.8V - 1.5V |
| Vout ripple (DC) | TBD | | |
| Iout | TBD | | 55A (target 60A) max |
| Step load | TBD | | |
| Vout ripple (AC) | TBD | | |
| Switching Freq. | TBD | | 50kHz - 1MHz |
| Protections | | | |


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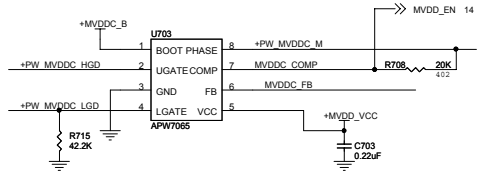
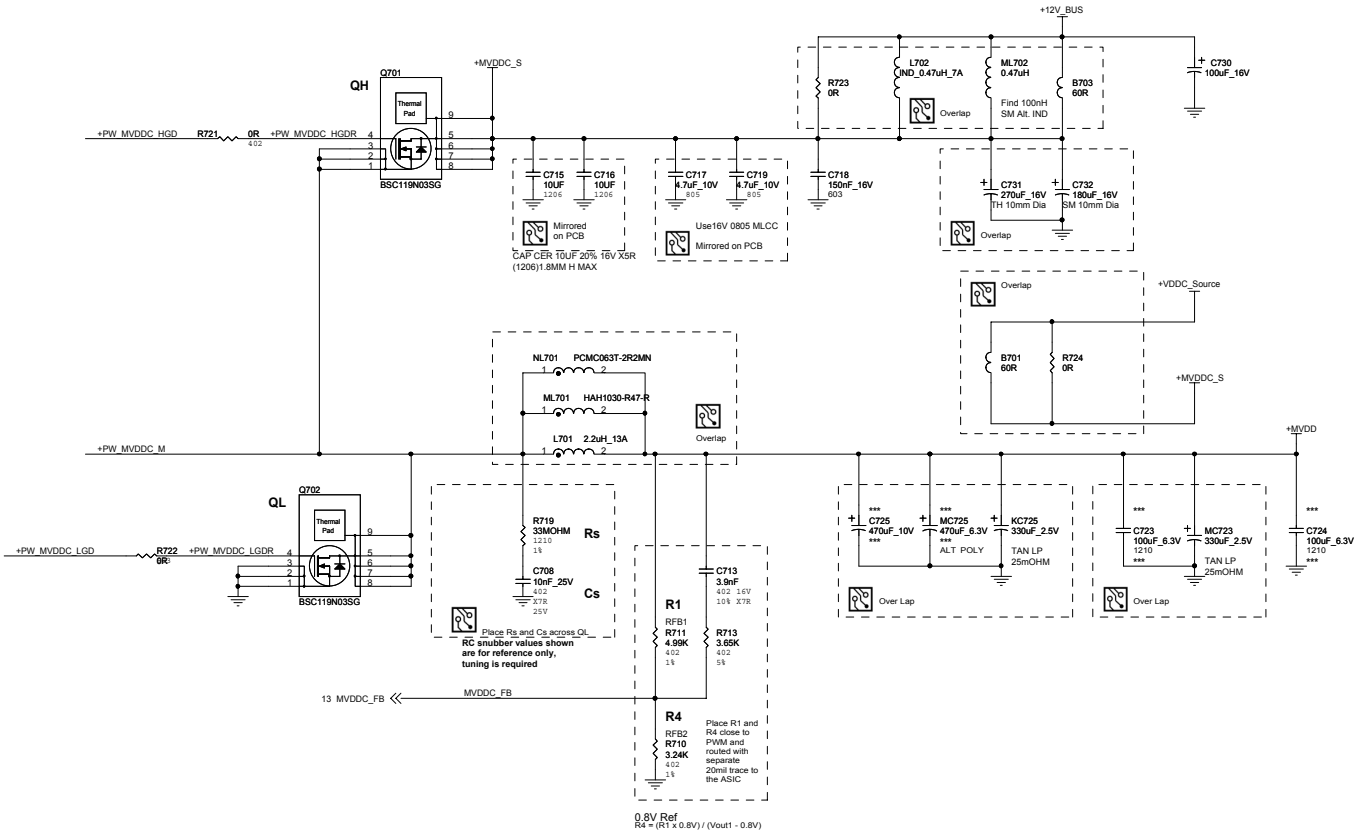
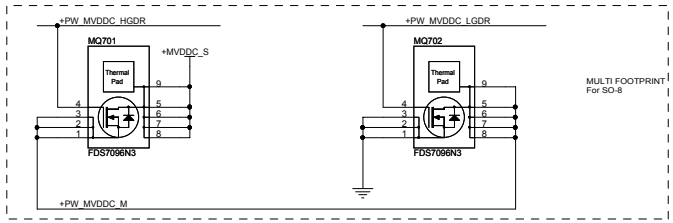



**List of supported foodprint**

**The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status**

**ANPEC APW7120/APW7065 (12V)**
**CAT CAT7583 (12V)**
**INTERSIL ISL6545**
**NEXSEM NX2114/2307**
**RICHTEK RT9214/RT8101**
**OnSemi ON1582**
**uPI UP6101 (No Ext_Vref in)**
**uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**




**SMPS02- Regulator for MVDD**

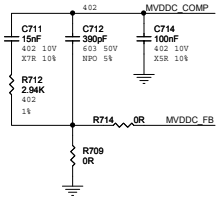
**Vout = 1.8V ~ 2.85V**

| Part | Vout | RFB1 | RFB2 |
|---|---|---|---|
| 0.8V Ref | 2.03V (1.98V~2.08V) | 4.99K p/n 3160499100G | 3.24K p/n 3160324100G |
| | | | |
| | | | |

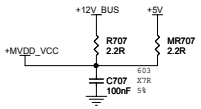
## SMPS02 Specifications

| | Nominal Value ; Tolerance | Adjustable range / Notes |
|---|---|---|
| Vin (power stage) | 12V ; +/-8% PCIe | ATX12V ver. 2.2 +/-5% |
| Vout | 2V ; +2%/-2% | 1.8V ~ 2.85V |
| Vout ripple (DC) | 50mVpp | |
| Iout | 6Aavg, 8Adc max | |
| Step load | 3Amax | |
| Vout ripple (AC) | +/-10% or 200mVpp @ 3A step load | |
| Switching Freq. | ~300kHz | TBD |
| Protections | | |

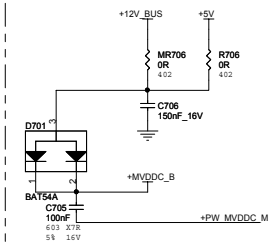
**COMPENSATION CIRCUIT**




**FILTERED SMPS VCC**




**BOOT CIRCUIT**




Layout guideline for Nexsem NX2114/2307

1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.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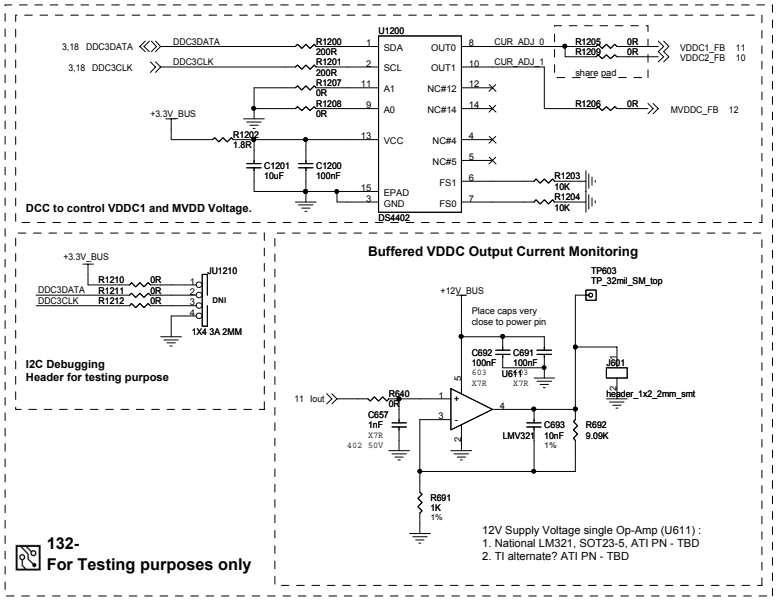
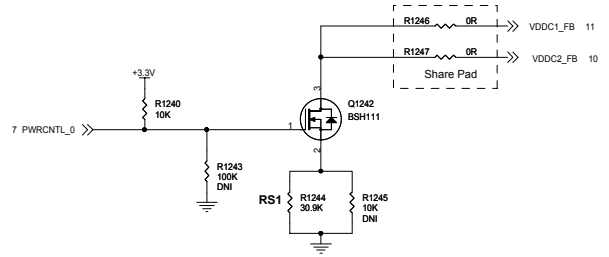
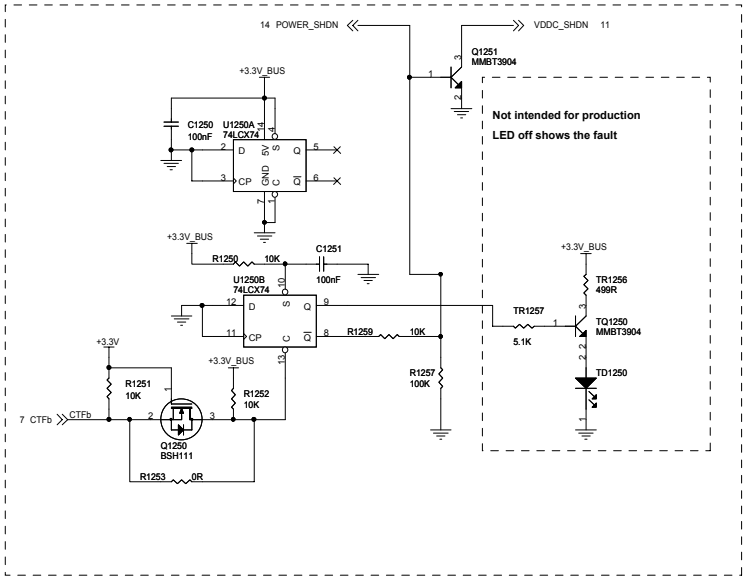



**SMPS03- Regulator for VDDC**

**Vout = .9V ~ 1.2V**

| | VDDC | RS1 | PWRCNTL_0 |
|---|---|---|---|
| *0.6V Ref* | .9V | N/A | LOW |
| | 1.0V | 59.0K 1%<br>ATI # 3160590200G | HIGH |
| | 1.1V | 30.9K 1%<br>ATI # 3160309200G | HIGH |
| | 1.2V | 20.0K 1%<br>ATI # 3160200200G | HIGH |

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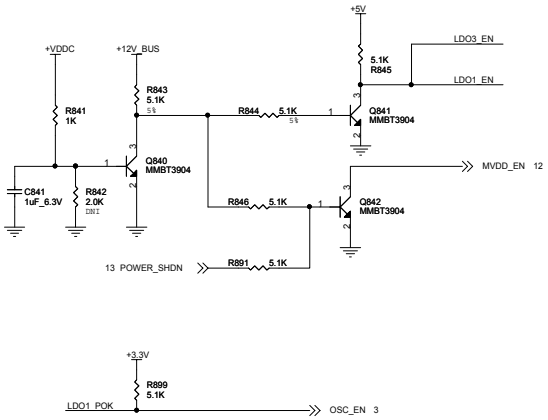
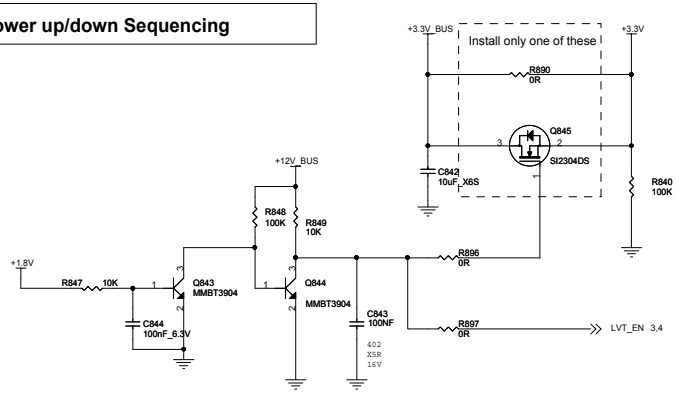
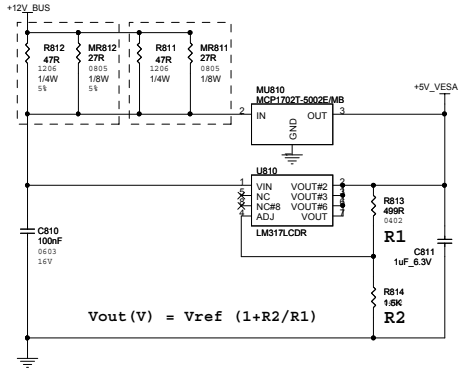
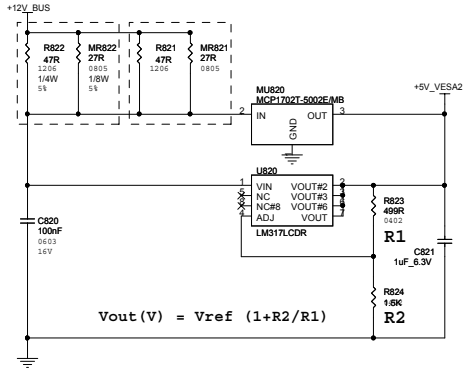
## Power up/down Sequencing

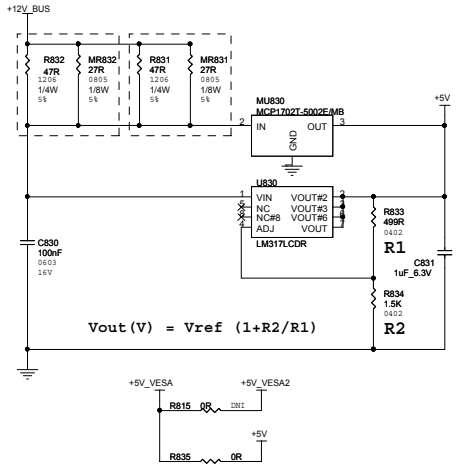



## Regulators for +5V, +5V_VESA and +5V_VESA2

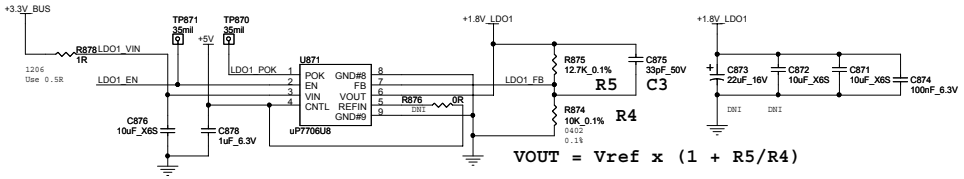


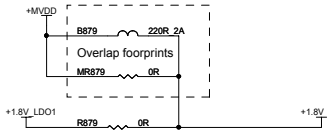




**LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX**

**PCB: 50 to 70mm sq. copper area for cooling**

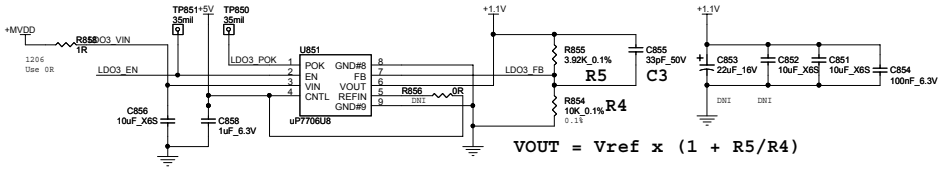


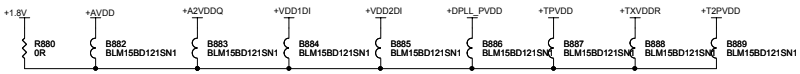

**DELETE LDO2**

**LDO #3: Vin = +1.45V to 2.1VMAX Vout = +1.1V +/- 2% Iout = 1.1A (TBV) RMS MAX**

**PCB: 50 to 70mm sq. copper area for cooling**




## Shared Power Rails





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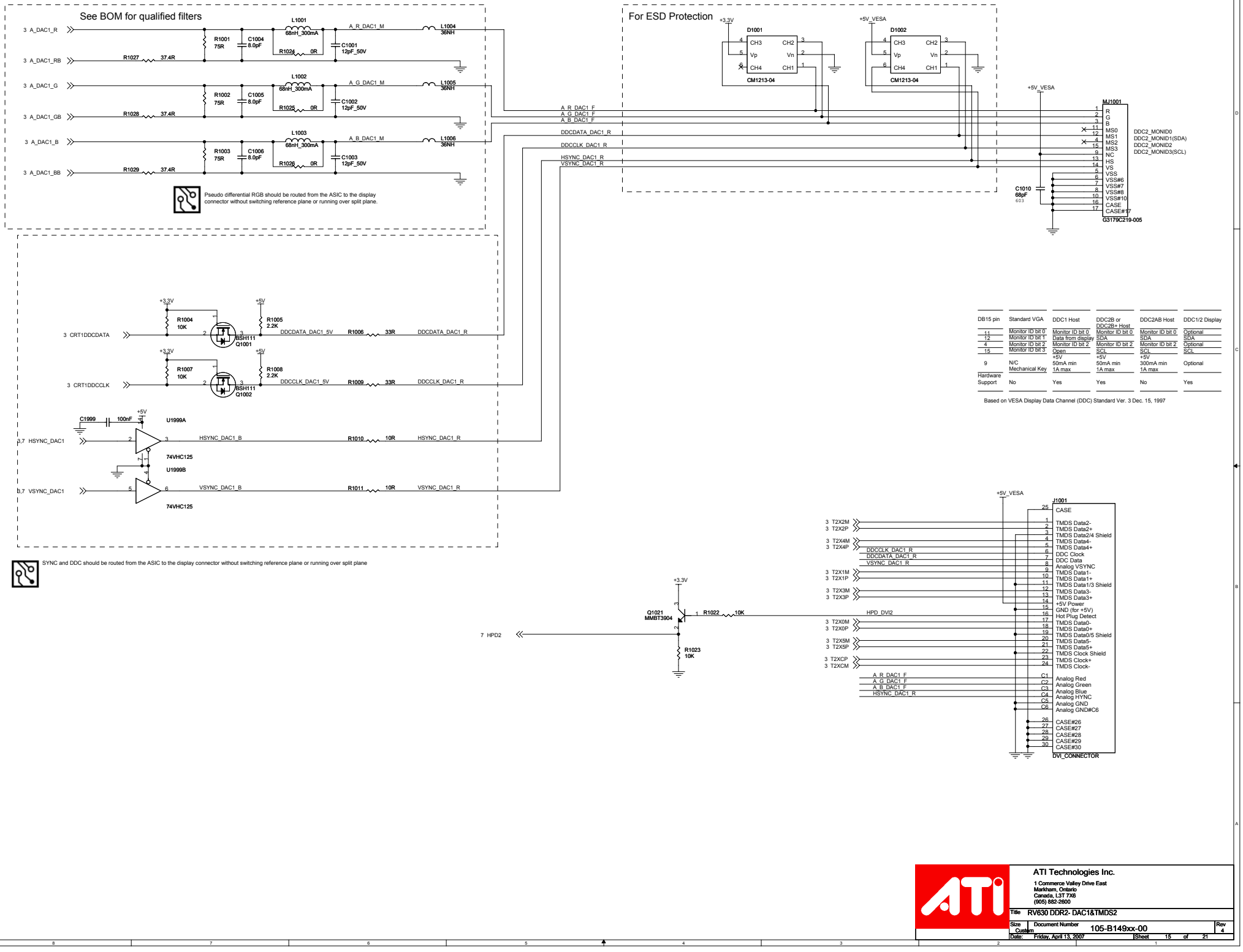


| DB15 pin | Standard VGA | DDC1 Host | DDC2B or DDC2B+ Host | DDC2AB Host | DDC1/2 Display |
|---|---|---|---|---|---|
| 11 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Optional |
| 12 | Monitor ID bit 1 | Data from display | SDA | SDA | SDA |
| 4 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Optional |
| 15 | Monitor ID bit 3 | Open | SCL | SCL | SCL |
| | | +5V | +5V | +5V | |
| 9 | N/C | 50mA min | 50mA min | 300mA min | Optional |
| | Mechanical Key | 1A max | 1A max | 1A max | |
| Hardware Support | No | Yes | Yes | No | Yes |

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997


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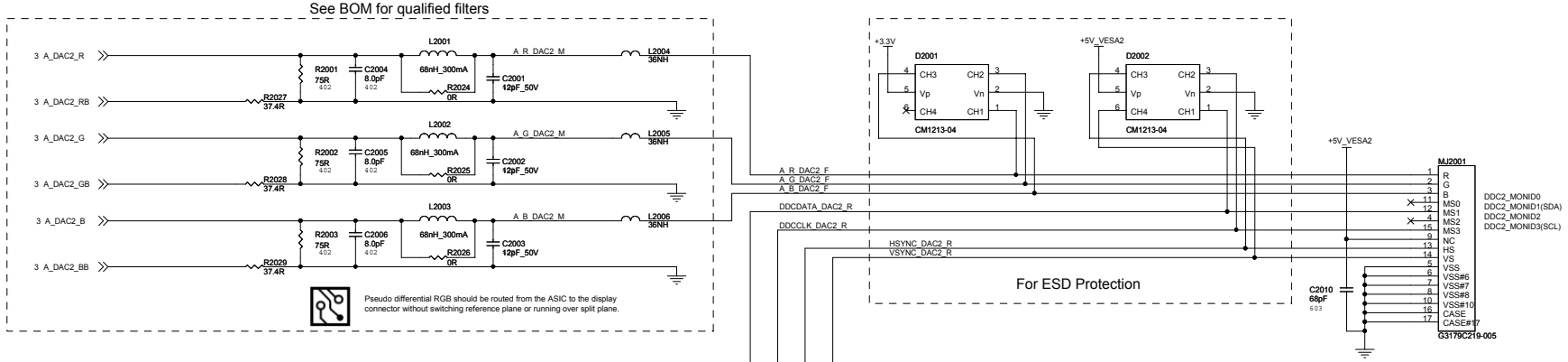
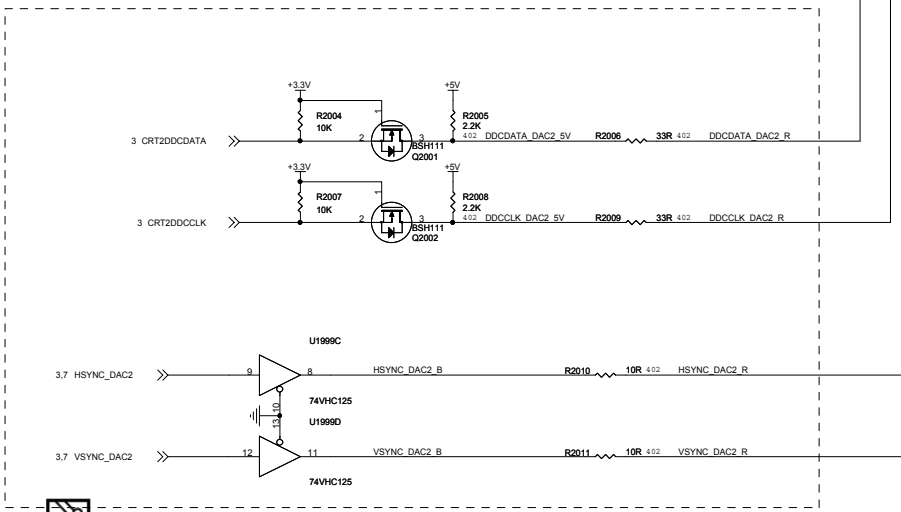
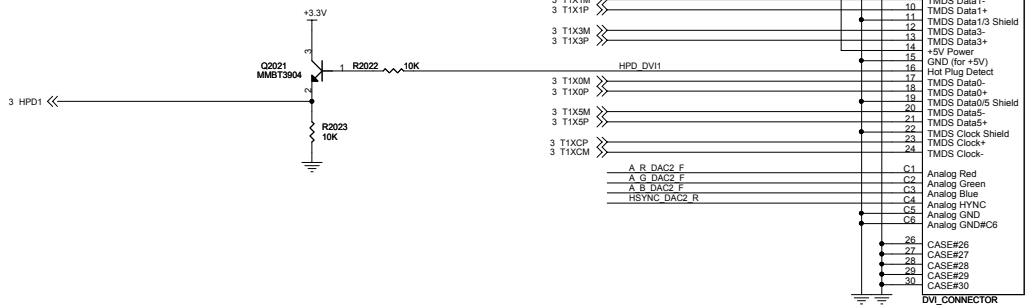
See BOM for qualified filters




| DB15 pin | Standard VGA | DDC1 Host | DDC2B or DDC2B+ Host | DDC2AB Host | DDC1/2 Display |
|---|---|---|---|---|---|
| 11 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Optional |
| 12 | Monitor ID bit 1 | Data from display | SDA | SDA | SDA |
| 4 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Optional |
| 15 | Monitor ID bit 3 | Open | SCL | SCL | SCL |
| 9 | N/C | +5V 50mA min | +5V 50mA min | +5V 300mA min | Optional |
| Hardware Support | Mechanical Key | 1A max | 1A max | 1A max | |
| | No | Yes | Yes | No | Yes |

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





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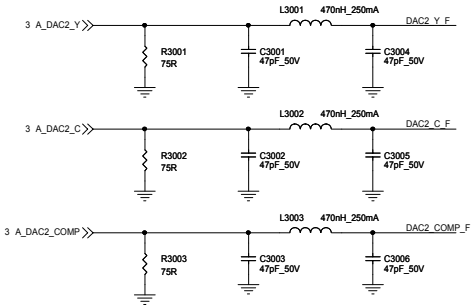


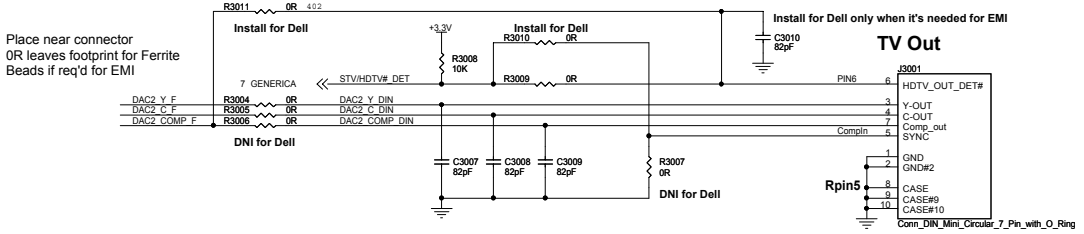


The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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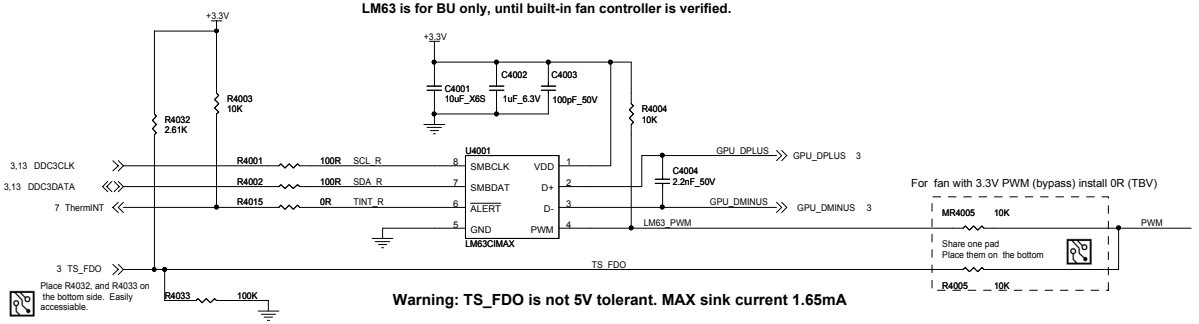
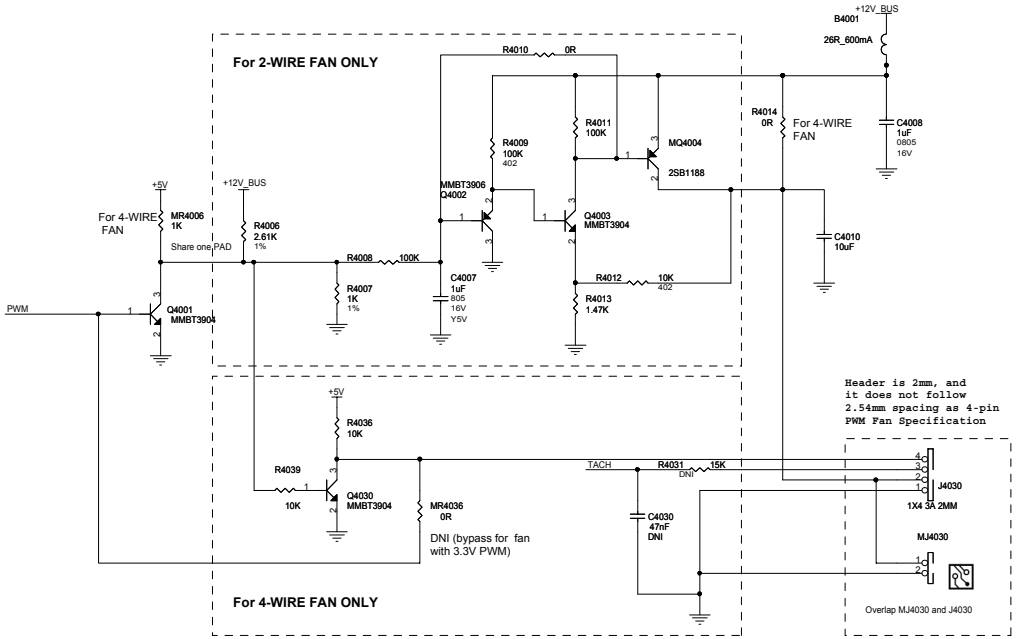
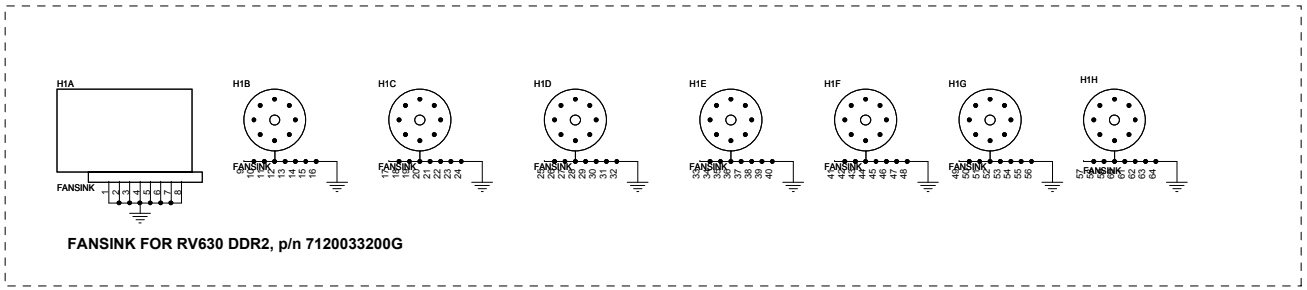
**LM63 is for BU only, until built-in fan controller is verified.**




**Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA**




**FANSINK FOR RV630 DDR2, p/n 7120033200G**

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DVI/DVI SCREWS with top tab

ASSY-SCREW1

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT

ASSY-SCREW2

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT

ASSY-SCREW3

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT

ASSY-SCREW4

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY-SCREW

ASSY1

ANTISTATIC
BAG

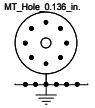
6_X_11

ASSY2

BRACKET

802038600G

MT1
MT_Hole_0.136_in.



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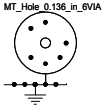
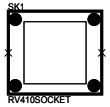


PCB1

PCB

109-B14931-00C

SK1



RV410SOCKET

<Variant Name>

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

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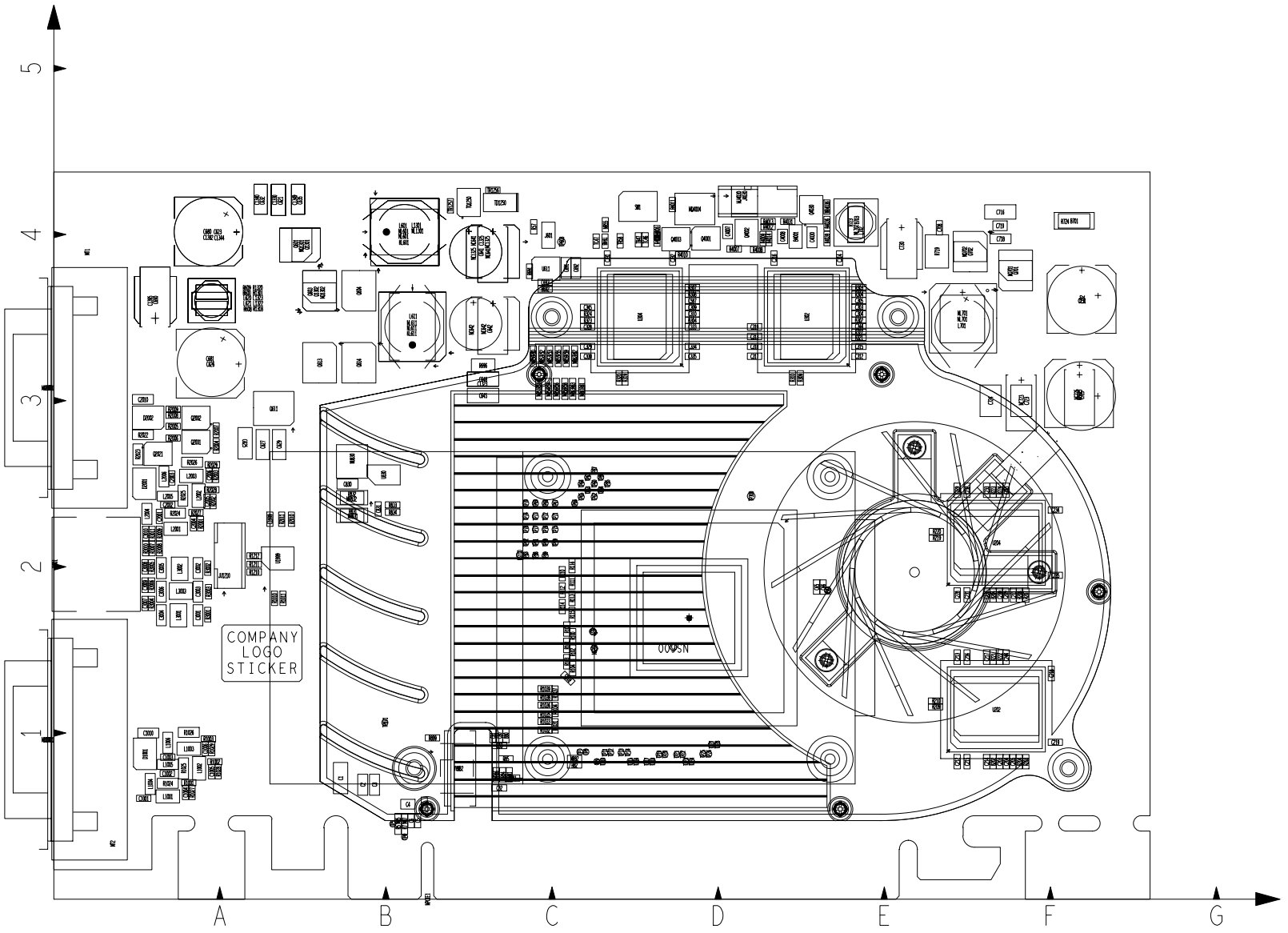
|---|---|---|
| Title | RV630 DDR2-MECHANICAL | |
| Size C | Document Number 105-B149xx-00 | Rev 4 |
| Date: Friday, April 13, 2007 | Sheet 19 of 21 | |

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| AMD<br>ADVANCED MICRO DEVICES<br>PCBCAD GROUP | RH PCIE RV630 512MB DDR2 DUAL DL-DVI-I VIVO FH<br><br>P/N 109-B14931-00<br>APR 5, 2007 ASSEMBLY TOP<br>Jasmine Lin/Svetlana Ostrovsky SHEET 1 OF 2 |

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APR 5, 2007
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