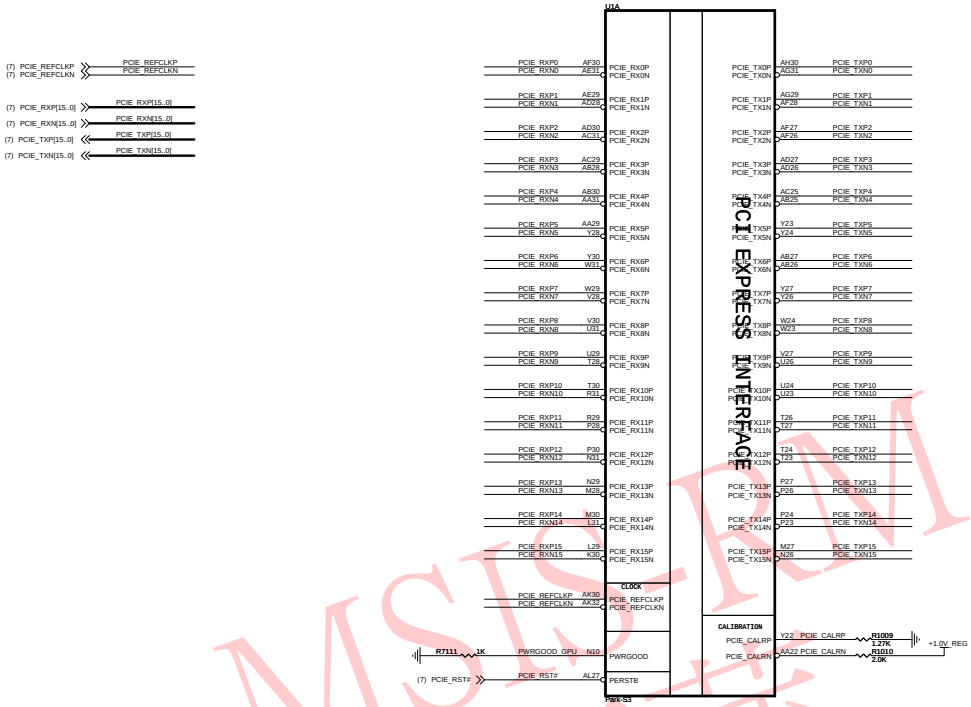

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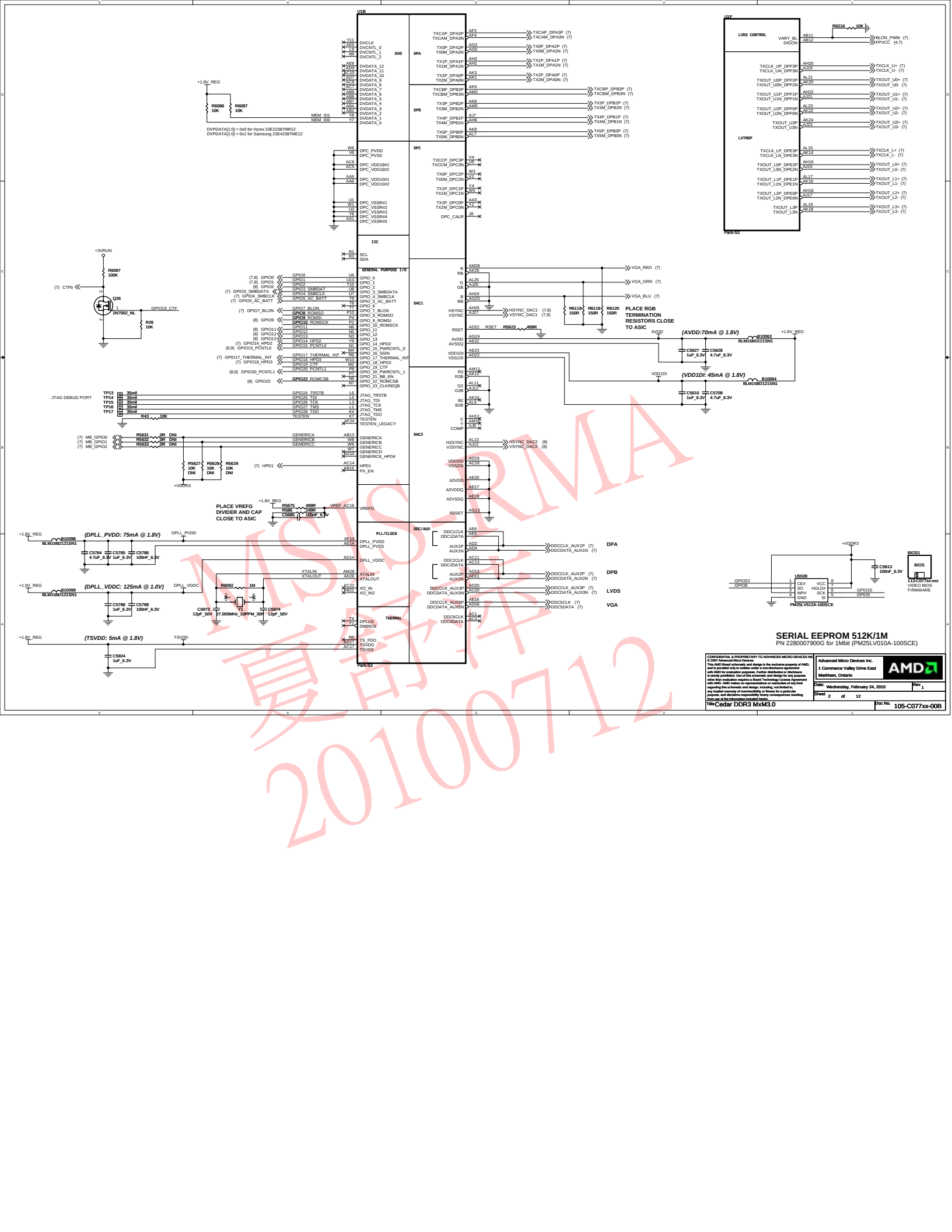

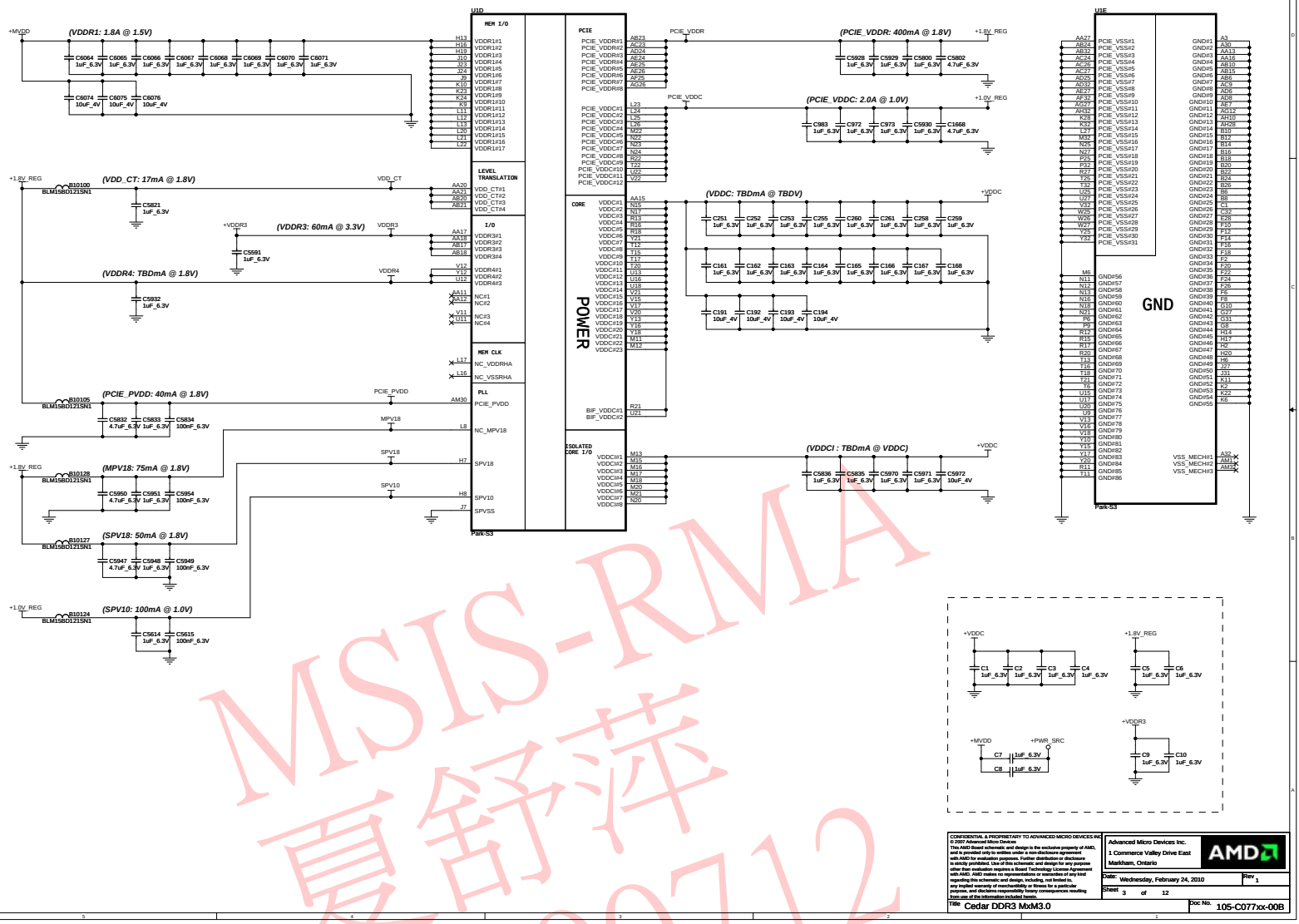

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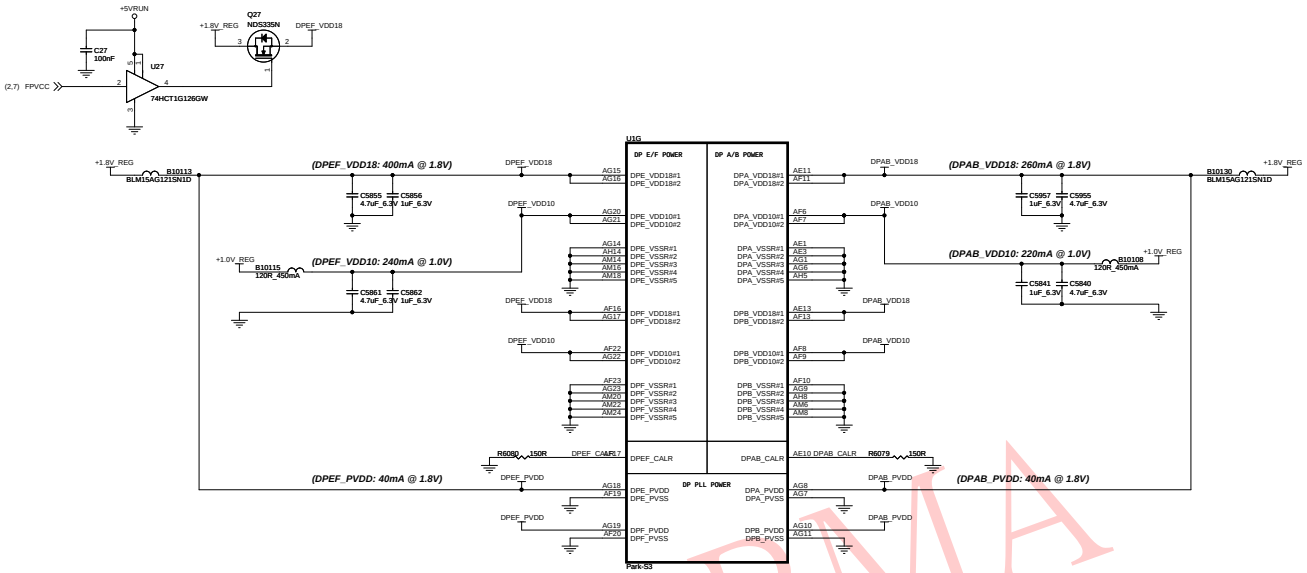

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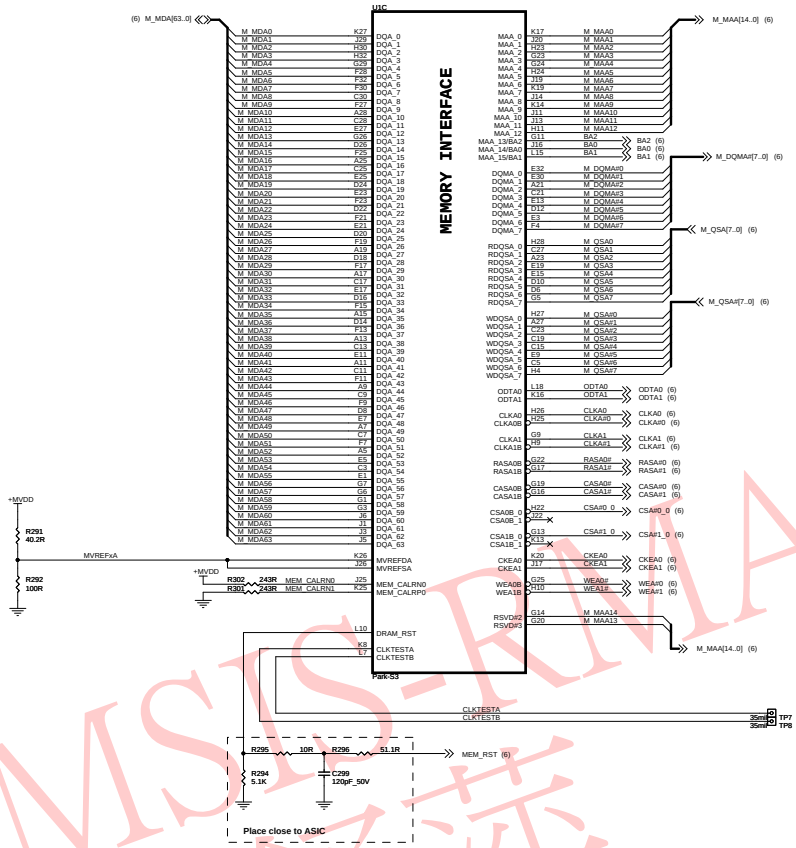

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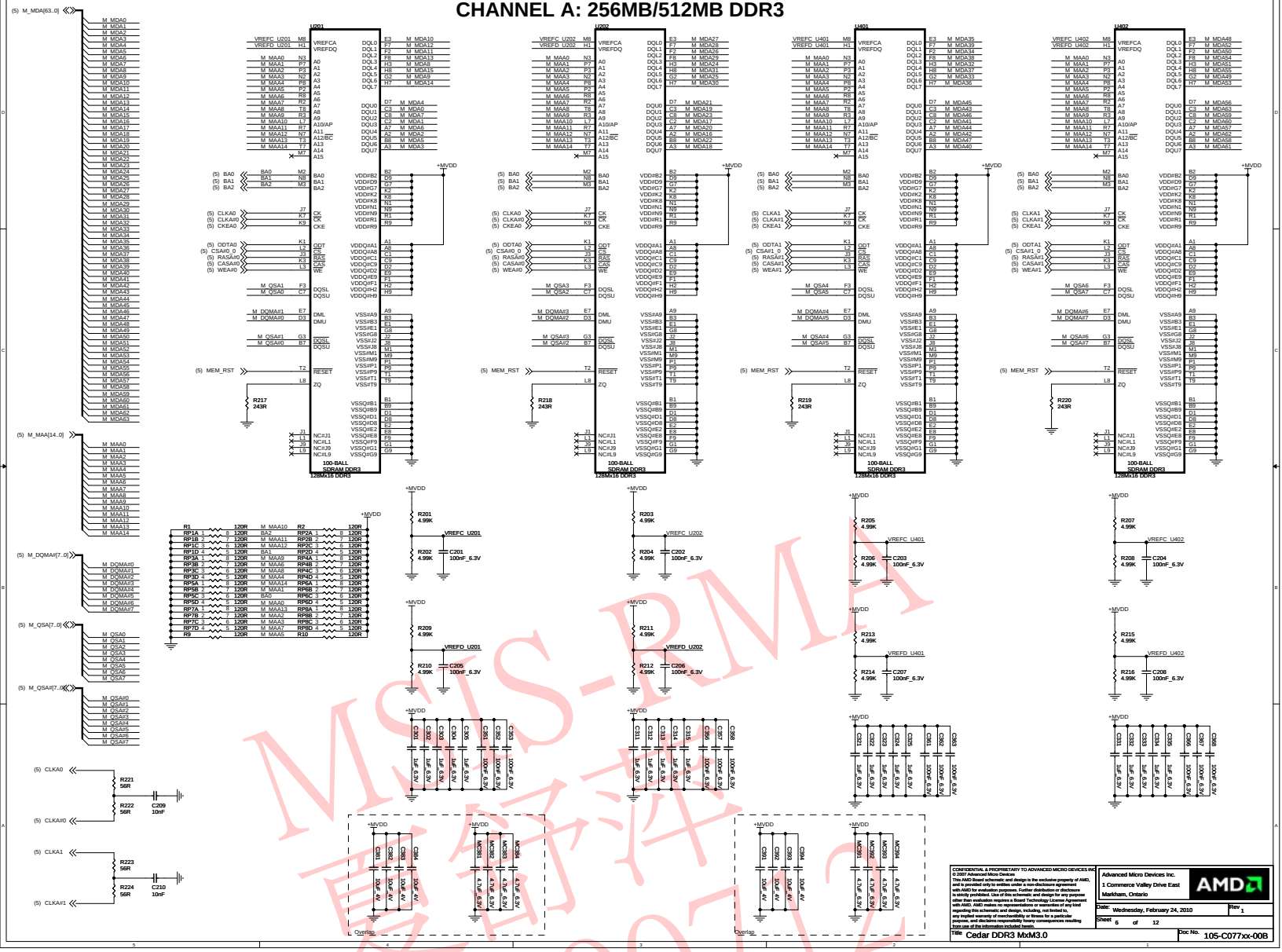
CHANNEL A: 256MB/512MB DDR3



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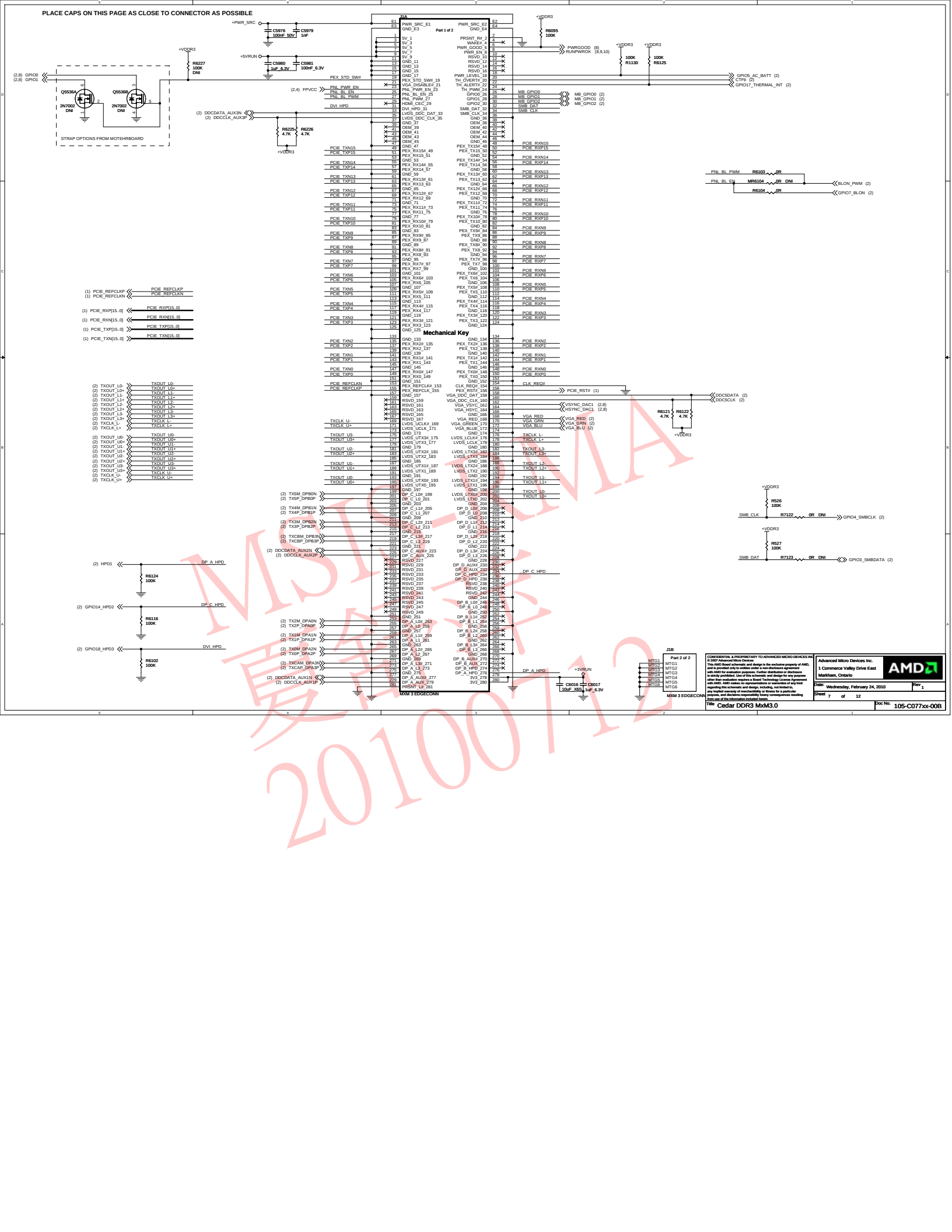
PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE



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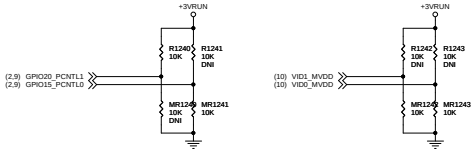
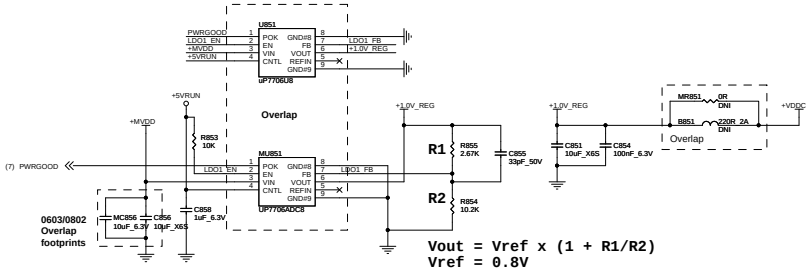
Voltage Settings and Power Play

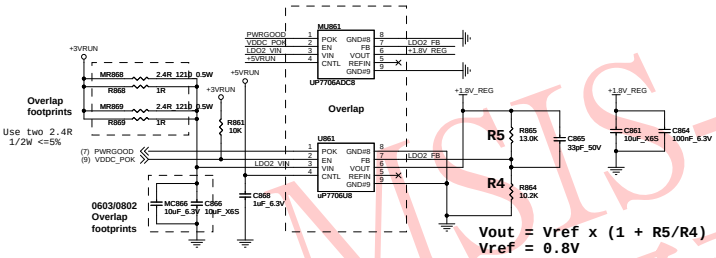


LDO1 Vin = +1.5V +/-2% Vout = +1.0V +/- 2% Iout = 1.5A RMS MAX (TBV)
PCB: 50 to 70mm sq. copper area for cooling



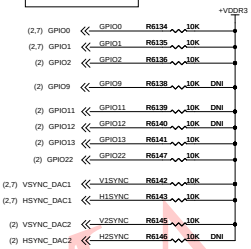
Vout = Vref x (1 + R1/R2)
Vref = 0.8V

LDO2 Vin = +3.3V +/-6% Vout = +1.8V +/- 2% Iout = 0.8A RMS MAX (TBV)
PCB: 50 to 70mm sq. copper area for cooling

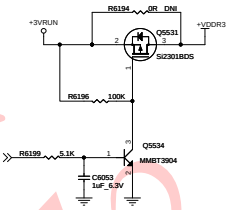


Vout = Vref x (1 + R5/R4)
Vref = 0.8V

PIN STRAPS



VDDR3 GATING



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing GPIO0 and GPIO1 pull ups need to be stuffed with Q5536 if system board is controlling the PCIE swing.	1
TX_DEEMPH_EN	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE Gen2 Enable 0: Advertises the PCIE device as 2.5GT/s capable at power-on 1: Advertises the PCIE device as 5.0GT/s capable at power-on	1
BIF_VGA DIS	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU) GPIO9 pull up needs to be stuffed with Q5537 if system board is controlling the VGA capacity	0
ROMIDCFG[2:0]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	1
AUD[1] AUD[0]	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
VIP_DEVICE_STRAP_DIS	V2SYNC	VIP Device Strap Disable 0: Slave VIP host port devices present 1: No slave VIP host port devices reporting presence	1
SMS_EN_HARD	H2SYNC	Reserved	0

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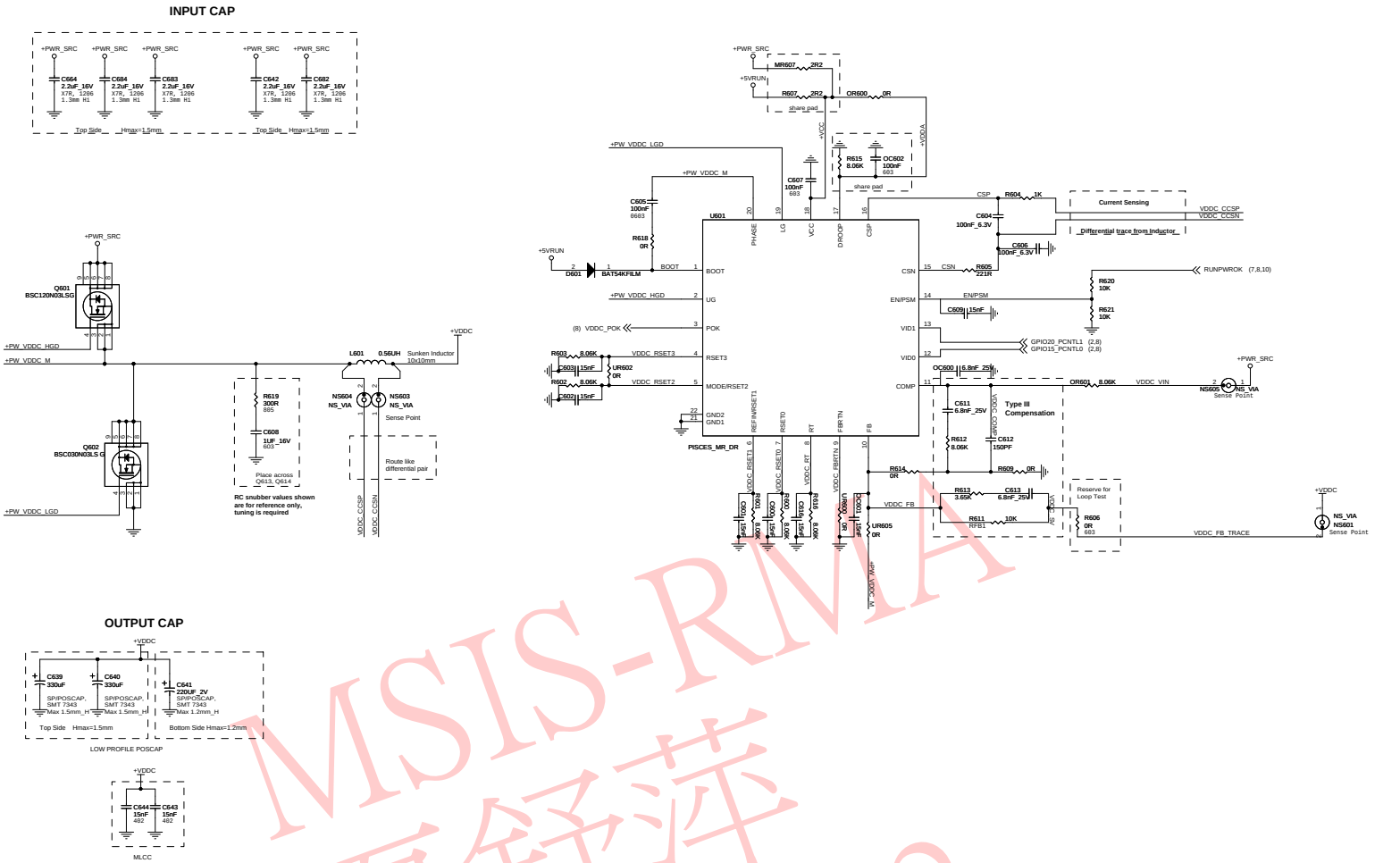

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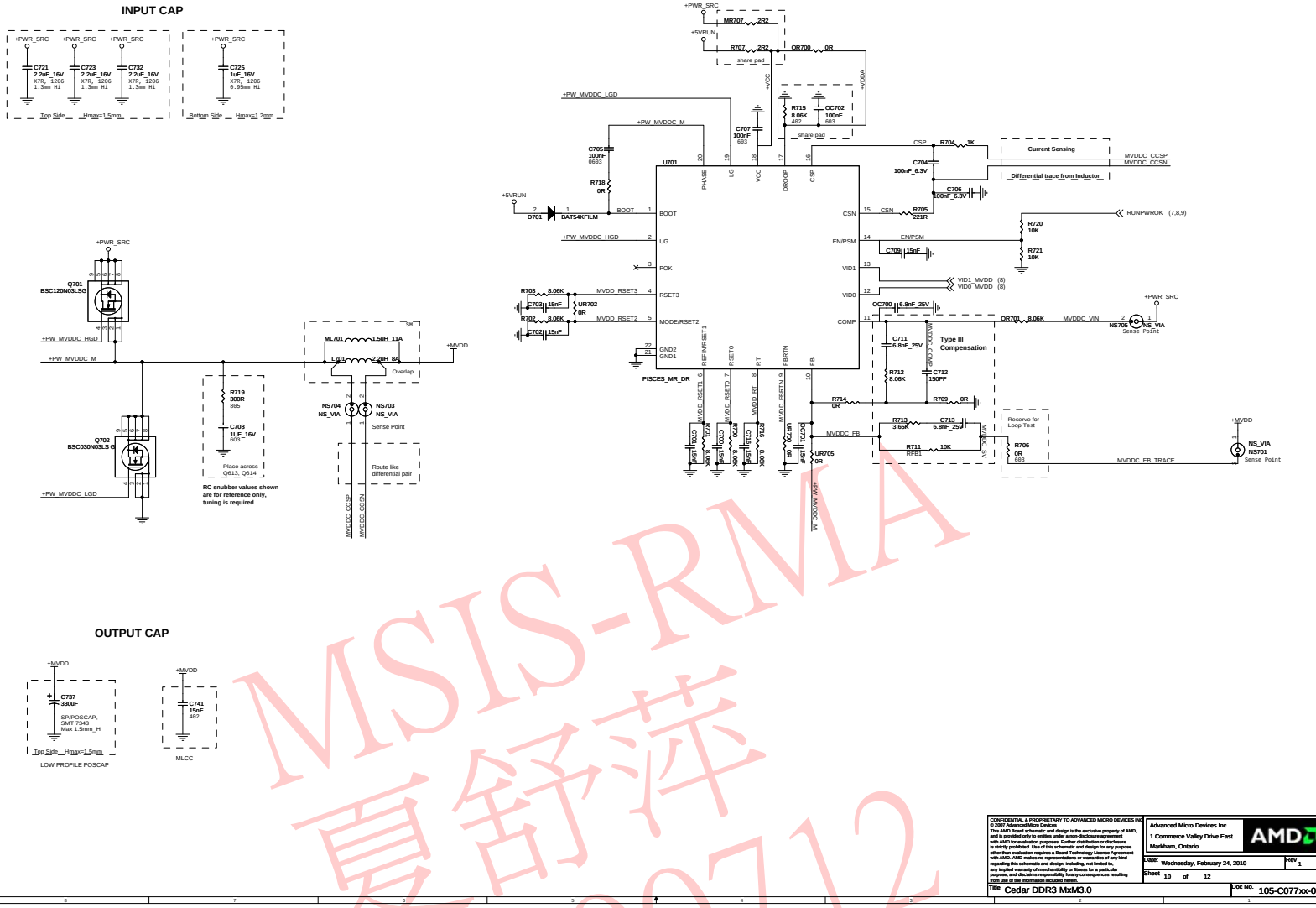

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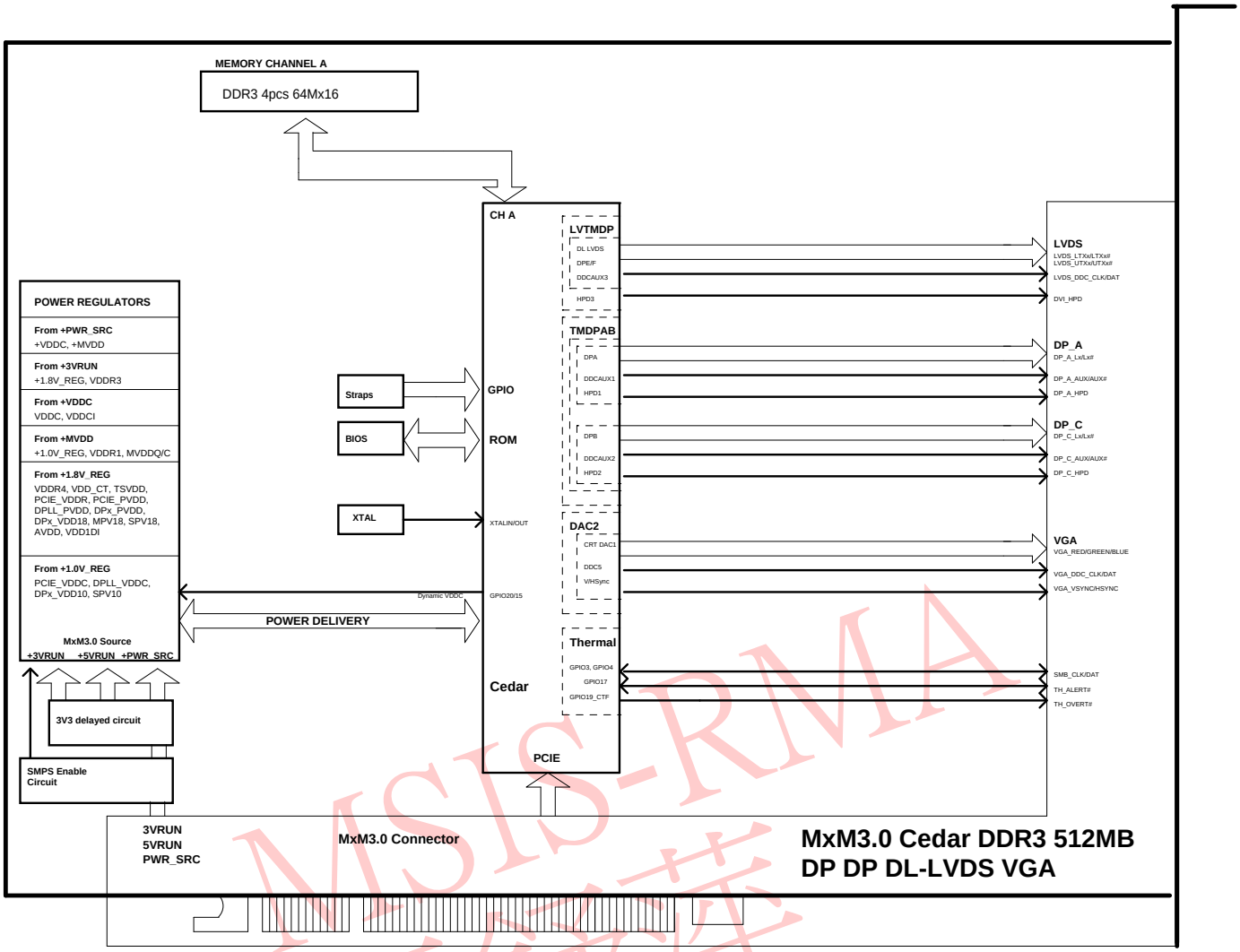

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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	09/10/06	Initial design for Cedar DDR3 MxM3.0 Type A-4L
1	00B	10/02/24	Layout change only (Move GPIO4_SMBCLK to the bottom layer)