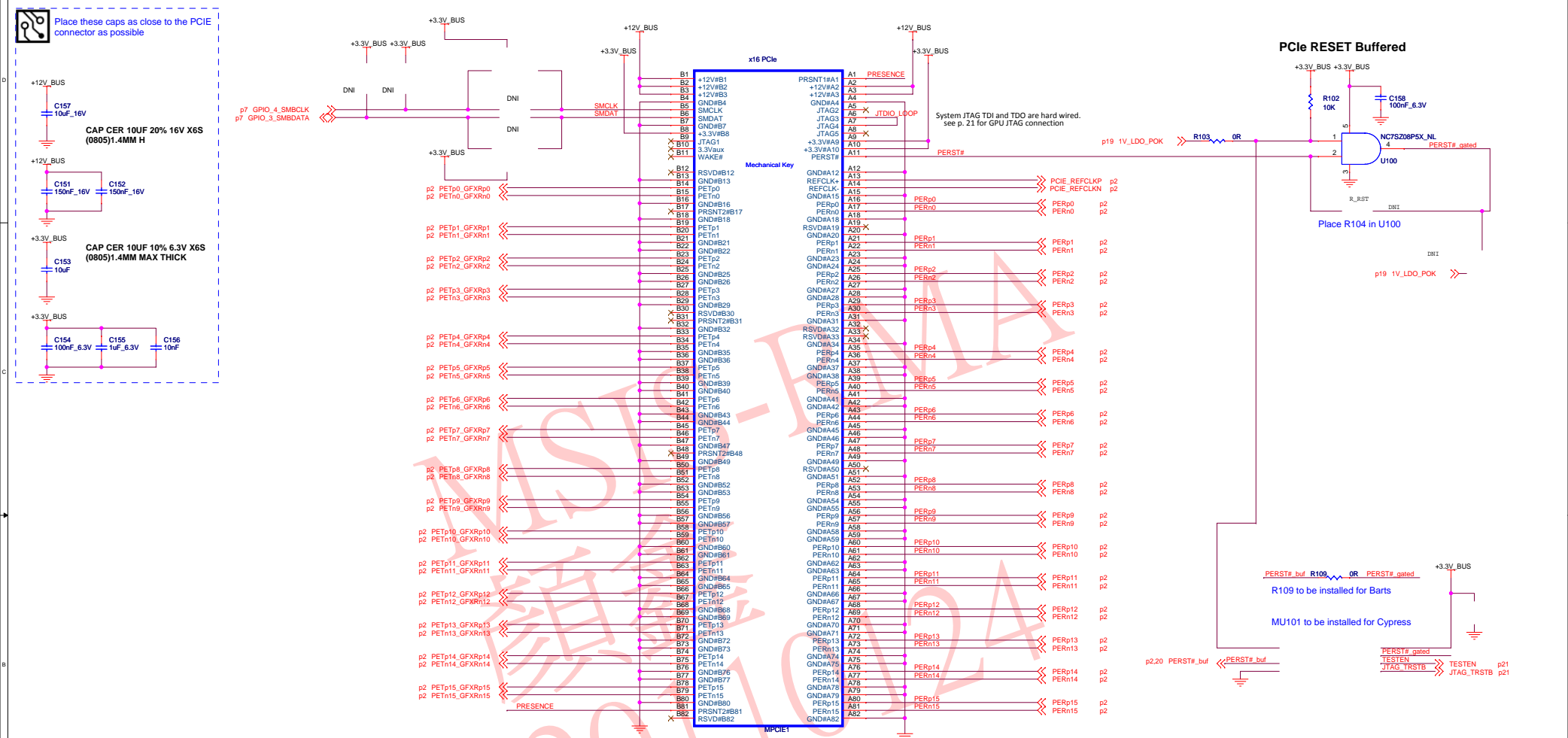
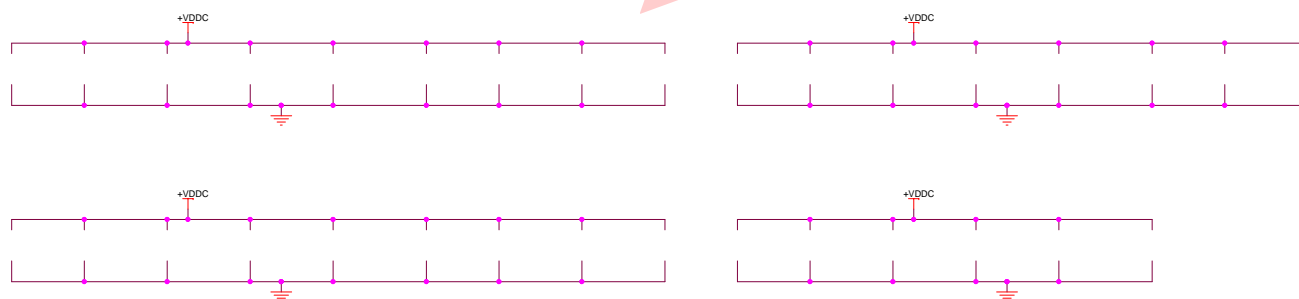




## PCI-EXPRESS EDGE CONNECTOR



PCIe stitching caps: To be placed close to the PCIe diff pair routed on Layer 6 at the PCIe slot



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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Markham, Ontario

Date: Friday, October 29, 2010

Sheet 1 of 23



Rev 62

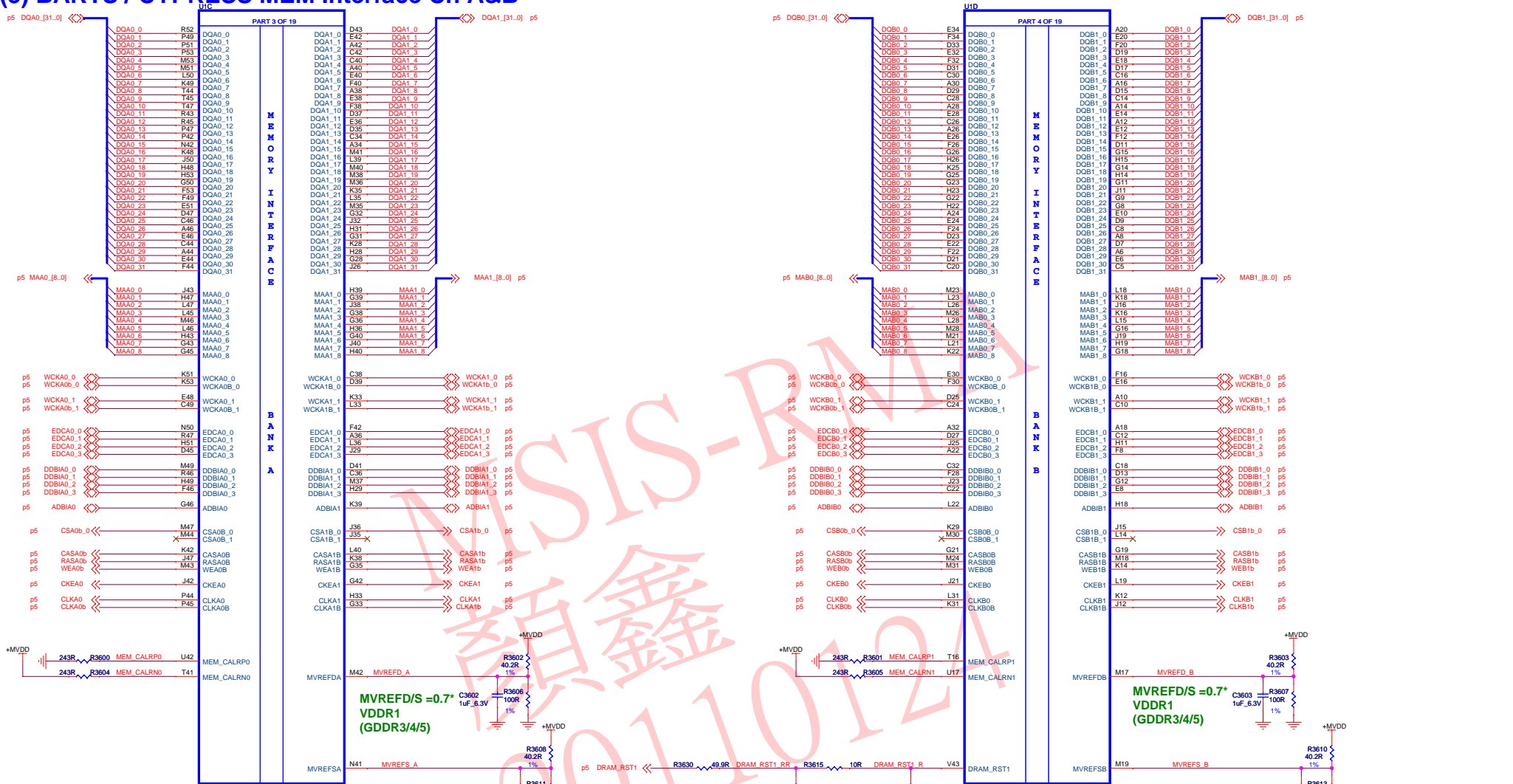
Title **PCIE EDGE CONNECTOR**

Doc No.	102-C22201-01
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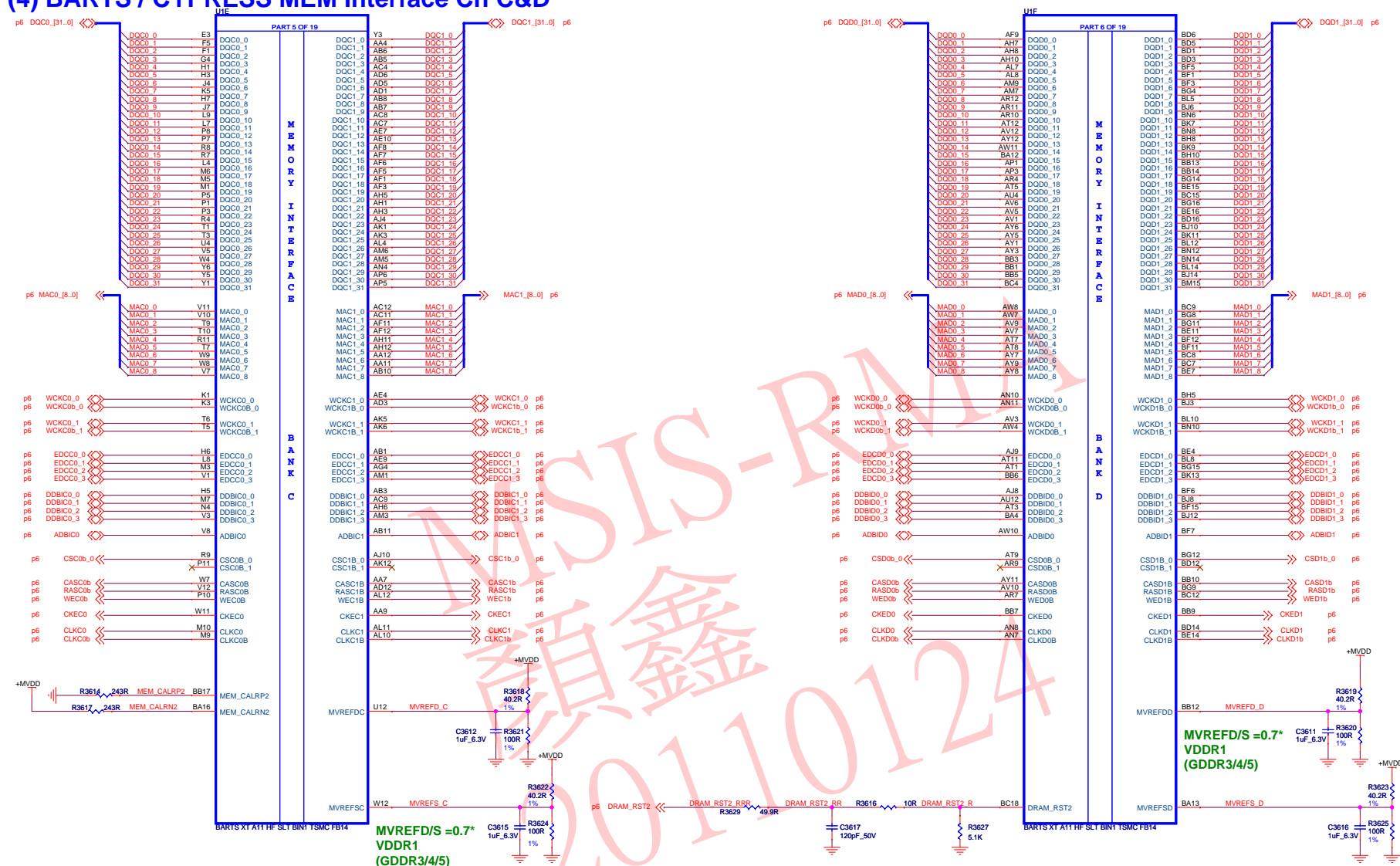


Doc No. 102-C22201-01

### (3) BARTS / CYPRESS MEM Interface Ch A&B



#### (4) BARTS / CYPRESS MEM Interface Ch C&D



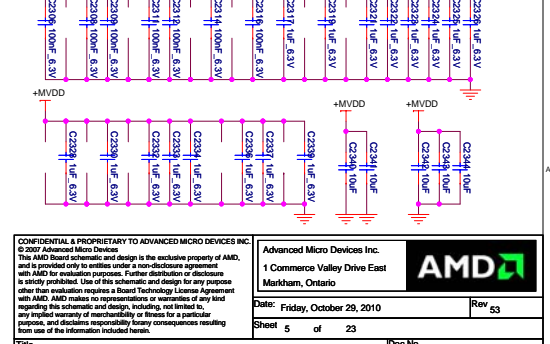
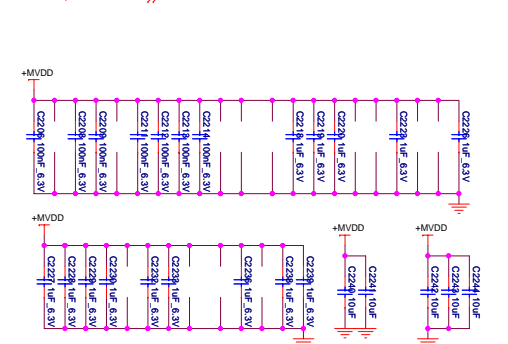
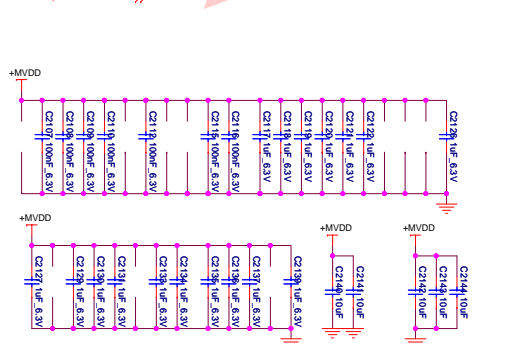
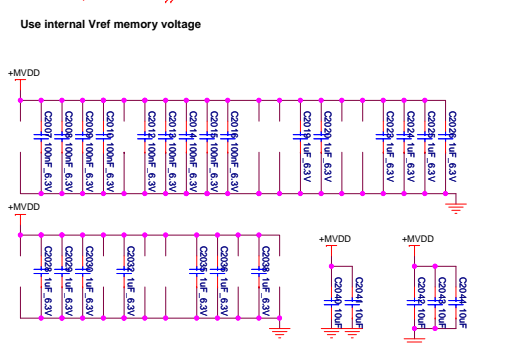
**GDDR5**


**+MVD0**

**p3 DQA1[31:0]**

Address	Data
DQAO-14	M0
DQAO-15	M1
DQAO-13	N2
DQAO-12	N4
DQAO-10	Y2
DQAO-9	T4
DQAO-11	Y2
DQAO-8	V4
DQAO-7	M3
DQAO-6	M1
DQAO-4	N13
DQAO-5	N11
DQAO-0	Y13
DQAO-2	T11
DQAO-1	Y13
DQAO-3	V11
DQAO-6	F13
DQAO-20	F11
DQAO-22	E13
DQAO-21	E11
DQAO-19	B13
DQAO-18	B11
DQAO-17	A13
DQAO-16	A11
DQAO-26	F4
DQAO-25	F2
DQAO-24	E2
DQAO-23	E0
DQAO-28	B2
DQAO-30	B4
DQAO-29	A2
DQAO-31	A4

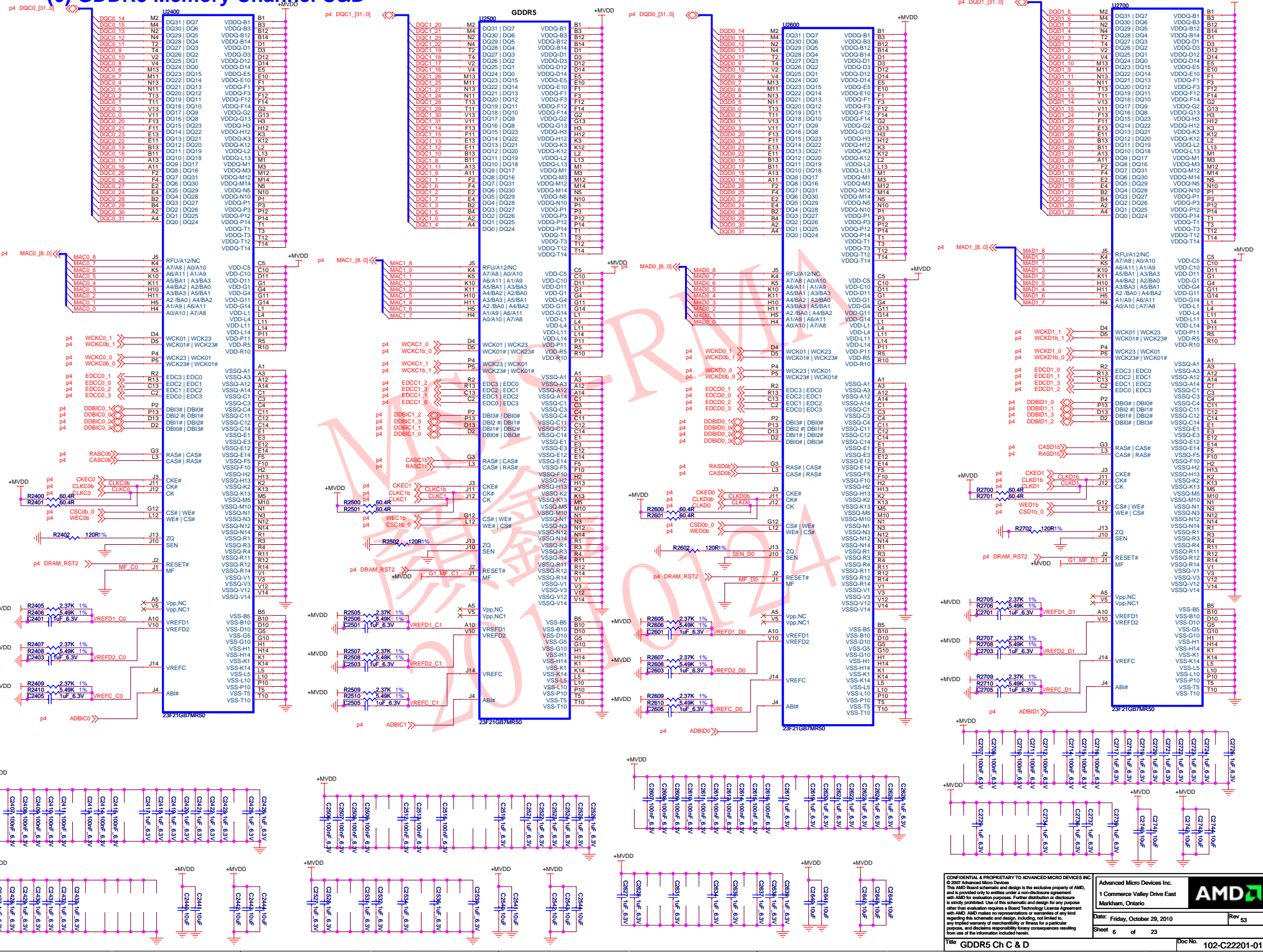
Address	Data
VDDQ-B1	B1
VDDQ-B3	B3
VDDQ-B7	B7
VDDQ-B14	B14
VDDQ-D1	D1
VDDQ-D3	D3
VDDQ-D12	D12
VDDQ-D14	D14
VDDQ-D15	D15
VDDQ-E5	E5
VDDQ-E10	E10
VDDQ-F11	F11
VDDQ-F12	F12
VDDQ-F14	F14
VDDQ-G12	G12
VDDQ-G13	G13
VDDQ-G19	G19
VDDQ-H4	H4
VDDQ-H12	H12
VDDQ-K3	K3
VDDQ-K12	K12
VDDQ-L13	L13
VDDQ-L14	L14
VDDQ-M1	M1
VDDQ-M3	M3
VDDQ-M12	M12
VDDQ-M14	M14
VDDQ-N5	N5
VDDQ-N10	N10
VDDQ-N11	N11
VDDQ-P1	P1
VDDQ-P12	P12
VDDQ-P13	P13
VDDQ-P14	P14



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<p>Title <b>GDDR5 Ch A &amp; B</b></p>	<p>Date: Friday, October 29, 2010          Sheet 5 of 23          Rev 33</p>
<p>Doc No. <b>102-C2201-01</b></p>	



## (6) GDDR5 Memory Channel C&D



# (07) BARTS / Cypress GPIOs Strap CF XTAL OSC

PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

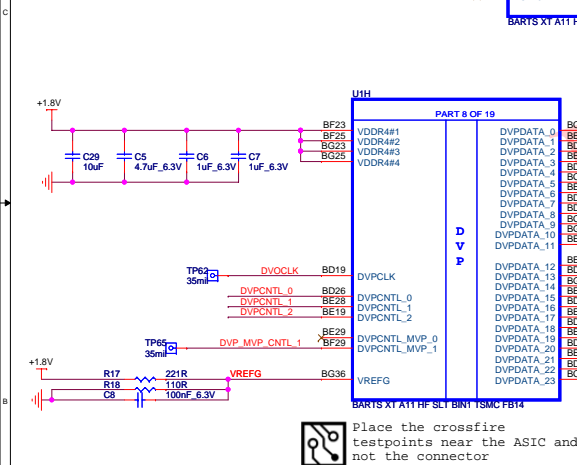
SCL / SDA BUS:

IC Address	Function	Device
0x50	Oni VDDC REGS	

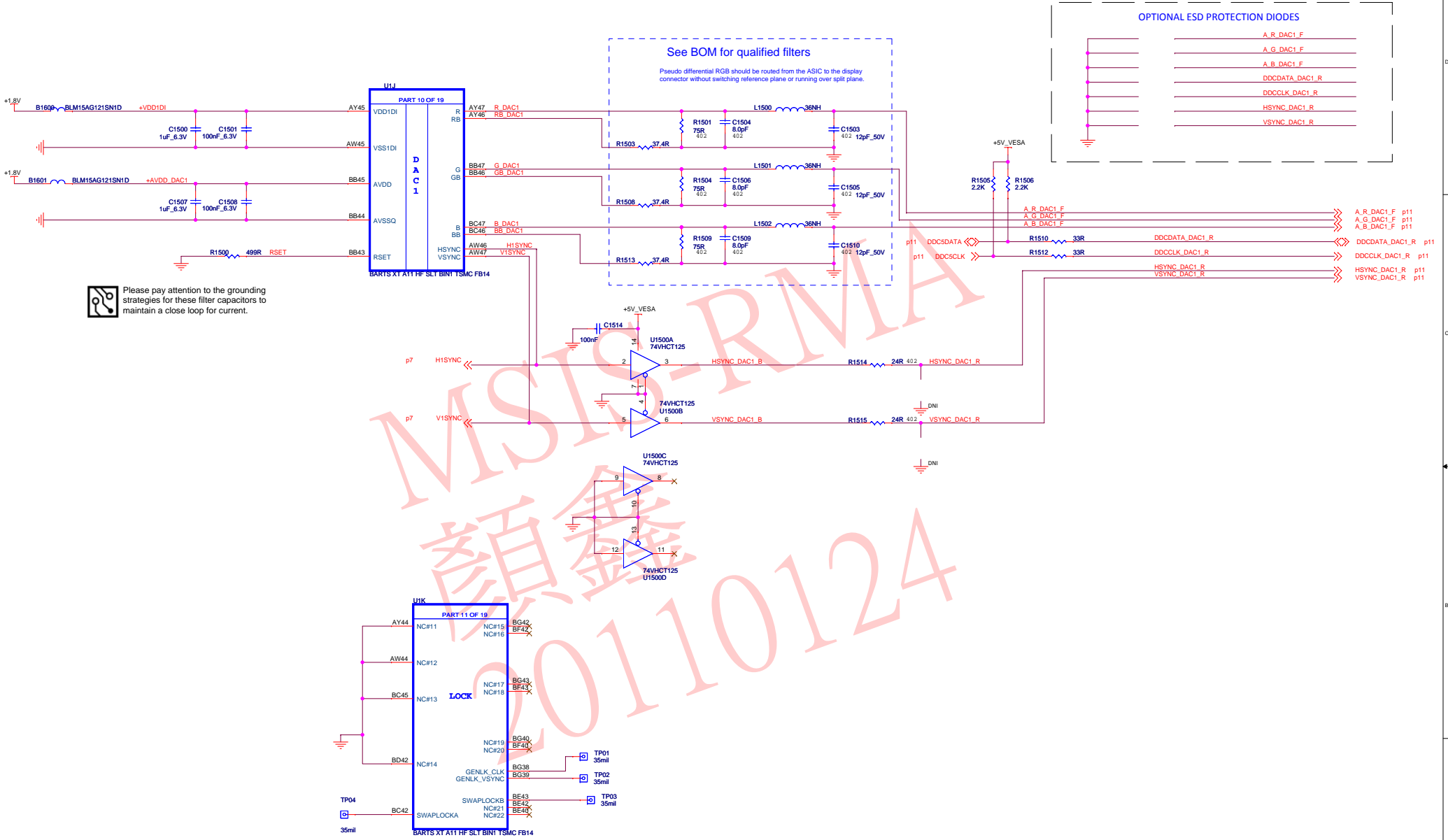
DDC6 BUS:

IC Address	Function	Device
0x98	LM90163 External Temperature Sensor	LM90163

PWRGOOD must be connected to GND for normal operation



(08) BARTS / CYPRESS DAC1





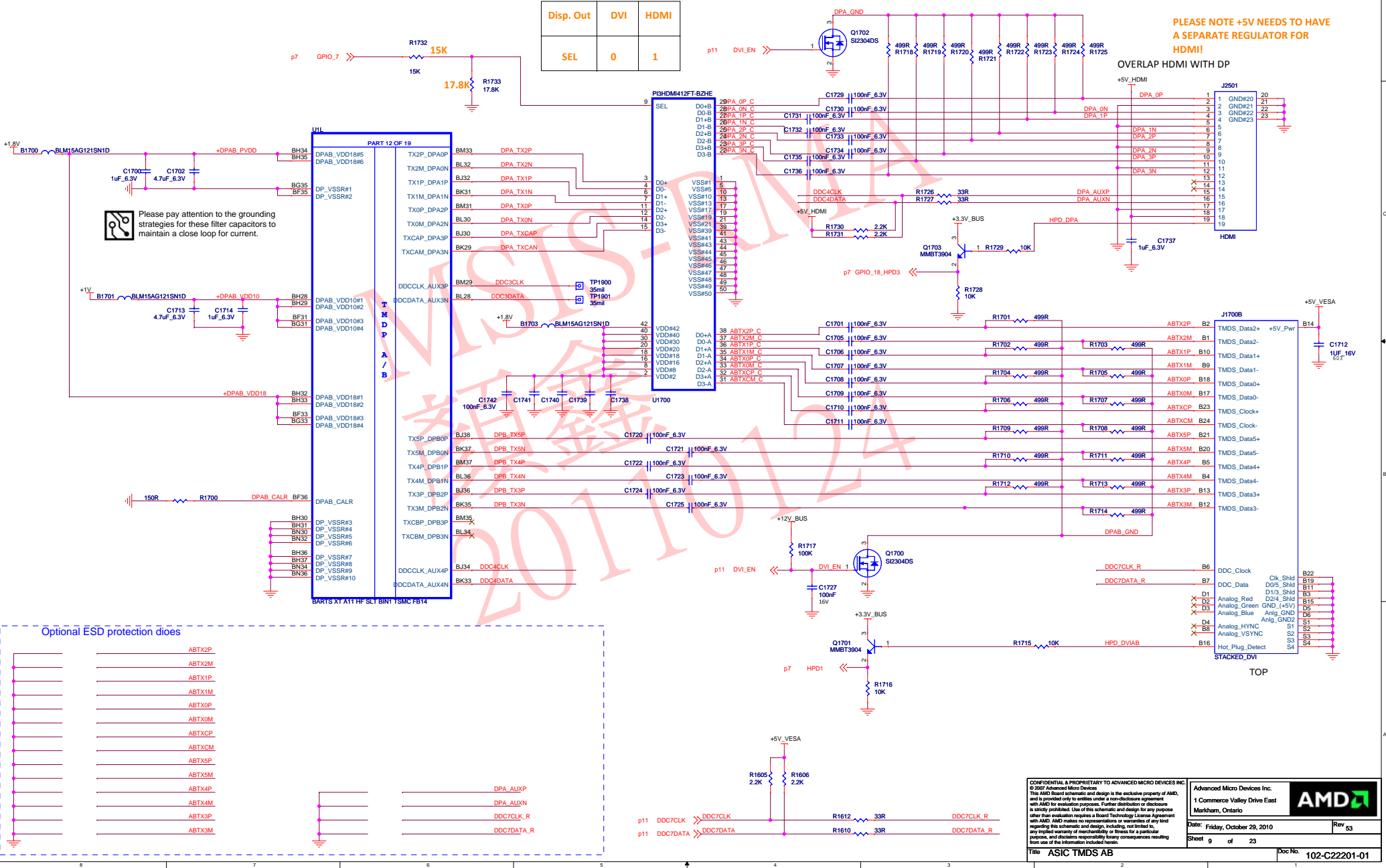
(09) BARTS / CYPRESS TMDS A&B



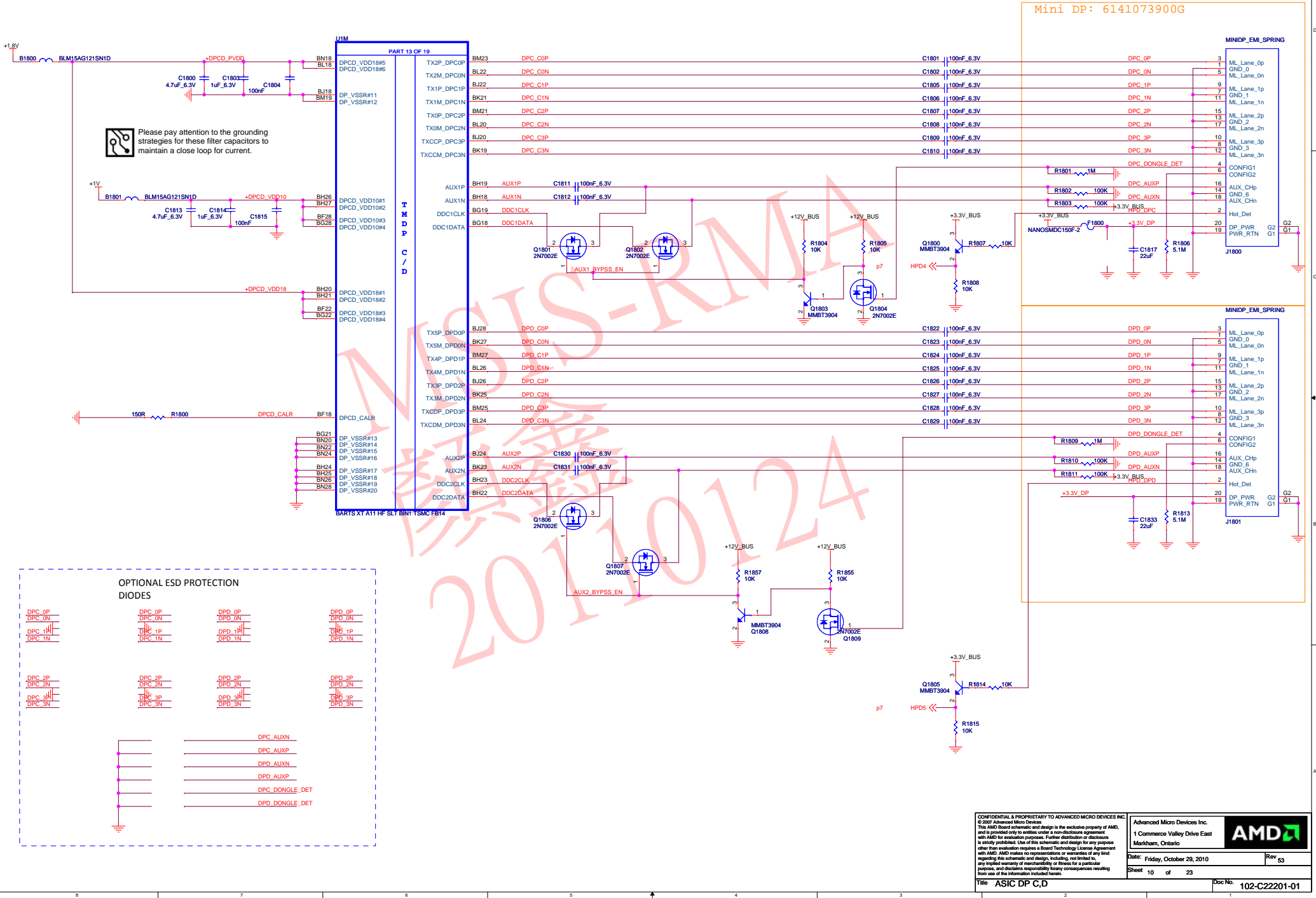
HDMI/DVI MUX:  
0.1uF cap to be used, placed close to VDD power pins  
Place 1x to top and 1x to bottom of the package  
Use 5 ground vias for the ground pad: 1 via at each corner of the ground pad and 1 in the center of the ground pad  
TDFN package to be used: 2600009800G  
SEL is 1.8V only

Disp. Out	DVI	HDMI
SEL	0	1

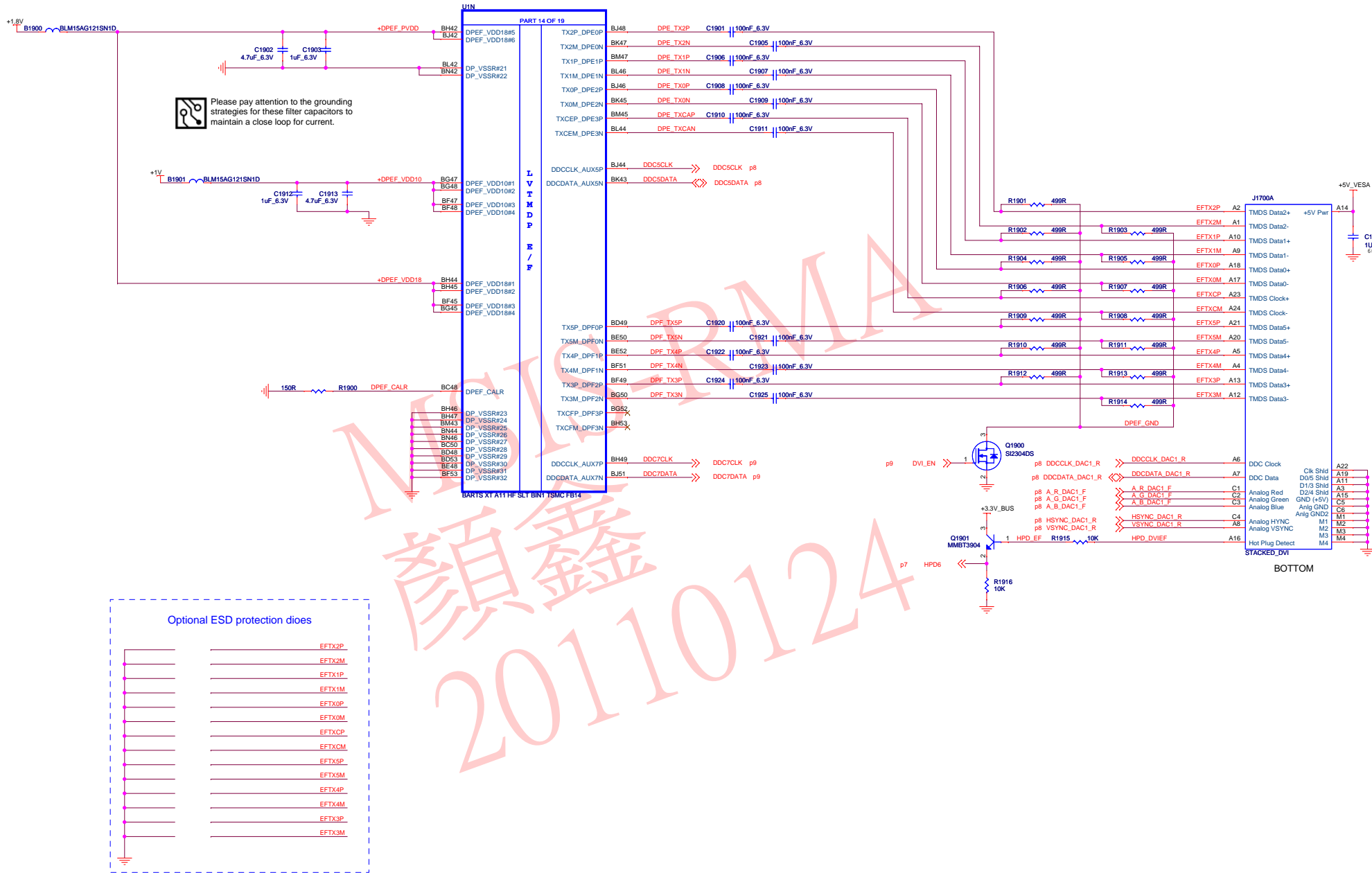
PLEASE NOTE +5V NEEDS TO HAVE A SEPARATE REGULATOR FOR HDMI!!



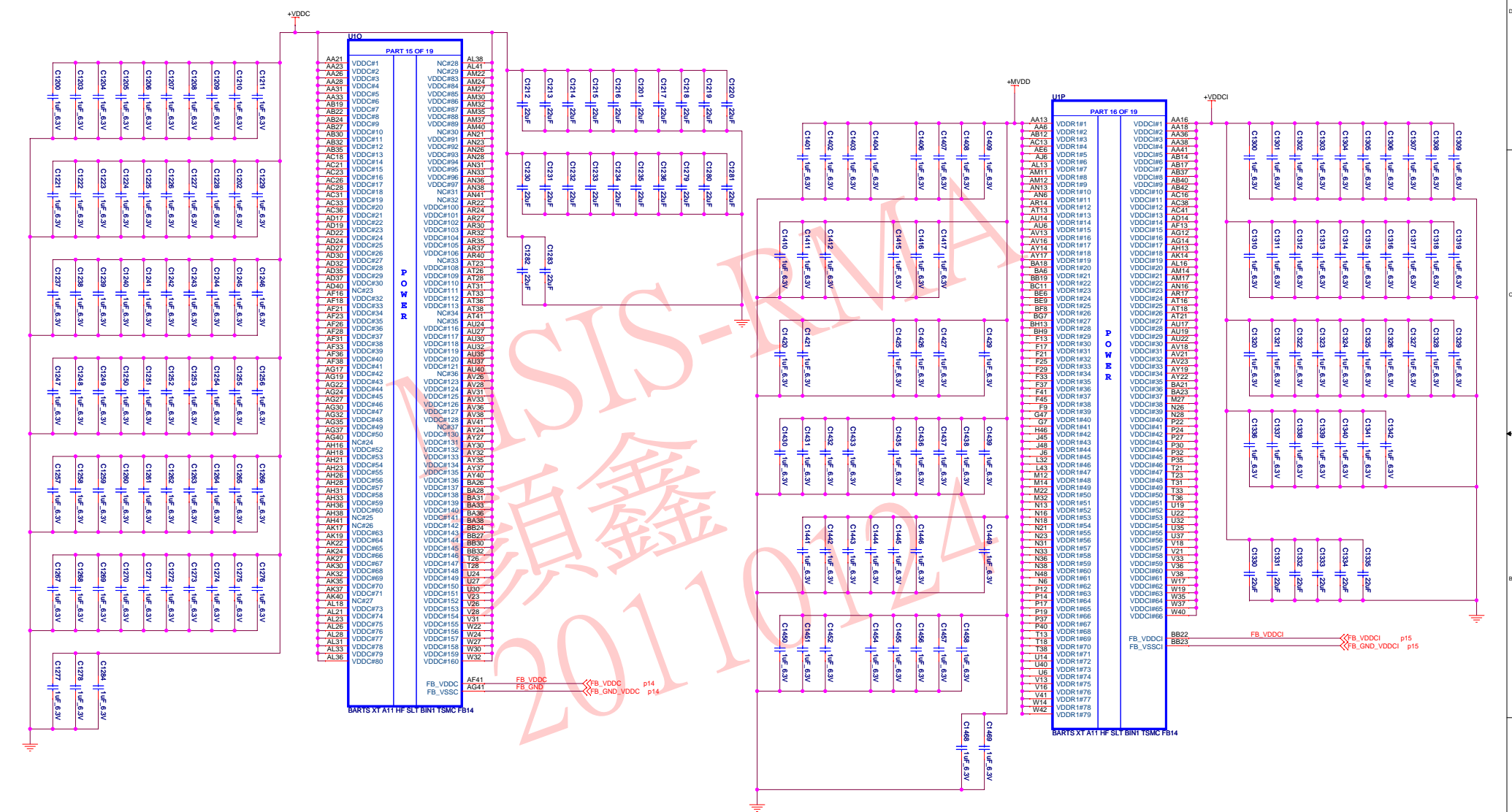
(10) BARTS / CYPRESS Display Port/HDMI C&D



(11) BARTS / CYPRESS LVTMDP E&F



## (12) BARTS / CYPRESS Power



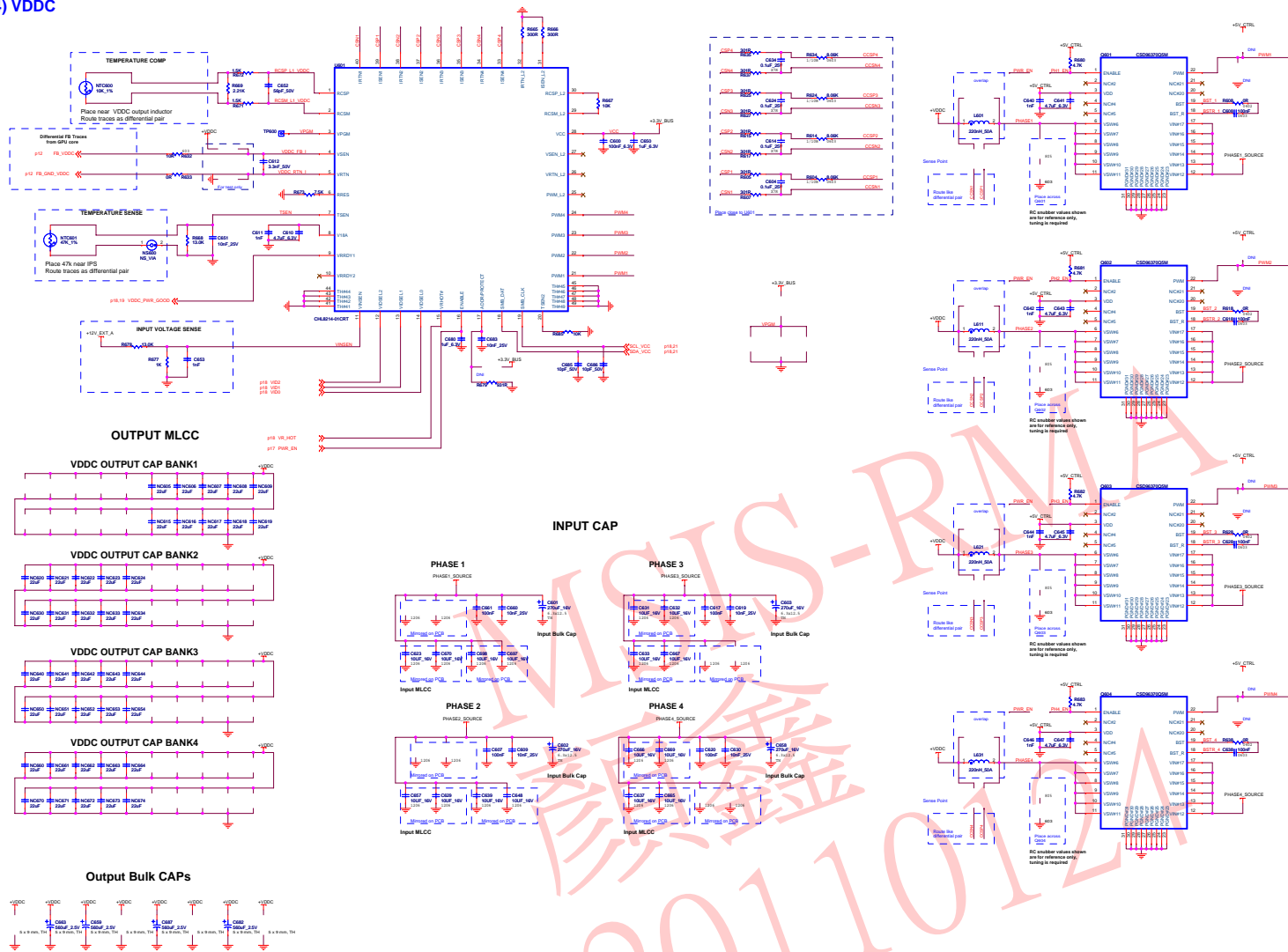
(13) BARTS / CYPRESS GND

UHQ			UR		
PART 17 OF 19			PART 18 OF 19		
AA0	VSS#1	AM10	BA17	VSS#251	L42
AA10	VSS#126	AM13	BA19	VSS#252	L48
AA14	VSS#127	AM16	BA2	VSS#253	L52
AA17	VSS#128	AM18	BA21	VSS#254	L6
AA19	VSS#129	AM23	BA24	VSS#255	M11
AA2	VSS#130	AM26	BA27	VSS#256	M13
AA22	VSS#131	AM28	BA30	VSS#257	M16
AA24	VSS#132	AM31	BA32	VSS#258	M33
AA27	VSS#133	AM33	BA35	VSS#259	M45
AA30	VSS#134	AM36	BA37	VSS#260	M48
AA32	VSS#135	AM38	BA40	VSS#261	M8
AA35	VSS#136	AM41	BA41	VSS#262	N12
AA37	VSS#137	AM48	BB11	VSS#263	N14
AA40	VSS#138	AN12	BB16	VSS#264	N17
AA42	VSS#139	AN14	BB18	VSS#265	N19
AA5	VSS#140	AN17	BB21	VSS#266	N22
AB13	VSS#141	AN2	BB26	VSS#267	N24
AB16	VSS#142	AN22	BB28	VSS#268	N27
AB18	VSS#143	AN24	BB31	VSS#269	N30
AB21	VSS#144	AN27	BB33	VSS#270	N32
AB23	VSS#145	AN30	BB40	VSS#271	N35
AB24	VSS#146	AN32	BB41	VSS#272	N37
AB26	VSS#147	AN35	BB51	VSS#273	N40
AB31	VSS#148	AN37	BB53	VSS#274	N42
AB33	VSS#149	AN40	BB8	VSS#275	N48
AB36	VSS#150	AN8	BC14	VSS#276	P13
AB38	VSS#151	AR13	BC15	VSS#277	P16
AB41	VSS#152	AR16	BC19	VSS#278	P18
AB9	VSS#153	AR2	BC2	VSS#279	P21
AC10	VSS#154	AR21	BC23	VSS#280	P23
AC14	VSS#155	AR23	BC33	VSS#281	P26
AC17	VSS#156	AR26	BC40	VSS#282	P28
AC19	VSS#157	AR28	CC6	VSS#283	P31
AC2	VSS#158	AR31	DD15	VSS#284	P33
AC22	VSS#159	AR33	DD18	VSS#285	P36
AC24	VSS#160	AR36	DD20	VSS#286	P38
AC27	VSS#161	AR38	DD38	VSS#287	P41
AC30	VSS#162	AR41	BE12	VSS#288	P43
AC33	VSS#163	AR6	BE16	VSS#289	P46
AC35	VSS#164	AR8	BE2	VSS#290	P48
AC37	VSS#165	AT10	BE40	VSS#291	P5
AC40	VSS#166	AT14	BE8	VSS#292	R10
AC42	VSS#167	AT17	BF14	VSS#293	R12
AC5	VSS#168	AT19	BF19	VSS#294	R44
AD13	VSS#169	AT22	BF19	VSS#295	R48
AD16	VSS#170	AT24	BF21	VSS#296	R50
AD18	VSS#171	AT27	BF26	VSS#297	R6
AD21	VSS#172	AT30	BF32	VSS#298	T11
AD23	VSS#173	AT32	BF9	VSS#299	T12
AD26	VSS#174	AT35	CC2	VSS#300	T14
AD28	VSS#175	AT37	GG6	VSS#301	T19
AD31	VSS#176	AT40	BH1	VSS#302	T22
AD33	VSS#177	AT6	BH11	VSS#303	T24
AD36	VSS#178	AU13	BH12	VSS#304	T27
AD38	VSS#179	AU16	BH14	VSS#305	T30
AD41	VSS#180	AU18	BH15	VSS#306	T32
AE11	VSS#181	AU2	BH38	VSS#307	T35
AE2	VSS#182	AU22	CH21	VSS#308	T37
AE8	VSS#183	AU23	BH40	VSS#309	T40
AF10	VSS#184	AU26	BH7	VSS#310	T43
AF14	VSS#185	AU28	BL15	VSS#311	T46
AF17	VSS#186	AU31	BL16	VSS#312	T51
AF19	VSS#187	AU33	BL38	VSS#313	T53
AF22	VSS#188	AU36	BM11	VSS#314	T58
AF24	VSS#189	AU38	BM13	VSS#315	T61
AF27	VSS#190	AU41	BM7	VSS#316	T63
AF30	VSS#191	AU40	BM9	VSS#317	T68
AF32	VSS#192	AU52	BN16	VSS#318	T72
AF35	VSS#193	AV11	BN38	VSS#319	T75
AF37	VSS#194	AV14	F10	VSS#320	T78
AF40	VSS#195	AV17	F11	VSS#321	T81
AG13	VSS#196	AV19	F14	VSS#322	T83
AG16	VSS#197	AV22	F18	VSS#323	T86
AG18	VSS#198	AV24	F19	VSS#324	T88
AG2	VSS#199	AV27	F23	VSS#325	T91
AG21	VSS#200	AV30	F27	VSS#326	T93
AG23	VSS#201	AV32	F33	VSS#327	T96
AG26	VSS#202	AV35	F36	VSS#328	T98
AG28	VSS#203	AV37	F38	VSS#329	T101
AG31	VSS#204	AV40	F43	VSS#330	T103
AG33	VSS#205	AV43	F45	VSS#331	T106
AG36	VSS#206	AV46	F47	VSS#332	T108
AG38	VSS#207	AV8	F7	VSS#333	T11
AG5	VSS#208	AW2	G2	VSS#334	T12
AH14	VSS#209	AW50	G29	VSS#335	T14
AH17	VSS#210	AW52	G48	VSS#336	T17
AH19	VSS#211	AW8	G52	VSS#337	T20
AH22	VSS#212	AW9	G6	VSS#338	T23
AH24	VSS#213	AY10	H12	VSS#339	T26
AH26	VSS#214	AY13	H16	VSS#340	T28
AH30	VSS#215	AY16	H21	VSS#341	T31
AH32	VSS#216	AY18	H25	VSS#342	T33
AH35	VSS#217	AY21	H32	VSS#343	T36
AH37	VSS#218	AY23	H35	VSS#344	T39
AH40	VSS#219	AY26	H38	VSS#345	T42
AH9	VSS#220	AY28	H42	VSS#346	T45
AJ2	VSS#221	AY31	H45	VSS#347	T48
AJ7	VSS#222	AY33	H9	VSS#348	T51
AK13	VSS#223	AY36	J2	VSS#349	T53
AK15	VSS#224	AY38	J22	VSS#350	T56
AK18	VSS#225	AY41	J26	VSS#351	T58
AK21	VSS#226	AY48	J31	VSS#352	T61
AK26	VSS#227	AY49	J33	VSS#353	T63
AK28	VSS#228	B11	J35	VSS#354	T66
AK31	VSS#229	B13	J46	VSS#355	T68
AK33	VSS#230	B15	J52	VSS#356	T71
AK36	VSS#231	B19	J58	VSS#357	T73
AK38	VSS#232	B21	K15	VSS#358	T76
AK41	VSS#233	B23	K16	VSS#359	T78
AL14	VSS#234	B25	K19	VSS#360	T81
AL17	VSS#235	B27	K21	VSS#361	T83
AL19	VSS#236	B29	K23	VSS#362	T86
AL2	VSS#237	B31	K26	VSS#363	T88
AL22	VSS#238	B33	K32	VSS#364	T91
AL24	VSS#239	B35	K36	VSS#365	T93
AL30	VSS#240	B37	K40	VSS#366	T96
AL32	VSS#241	B39	K6	VSS#367	T98
AL35	VSS#242	B41	L12	VSS#368	T101
AL37	VSS#243	B43	L16	VSS#369	T103
AL40	VSS#244	B45	L3	VSS#370	T106
AL5	VSS#245	B47	L5	VSS#371	T108
AL9	VSS#246	B49	L25	VSS#372	T11
ALB	VSS#247	B5	L38	VSS#373	T12
ALB	VSS#248	BA14	VSS#374	VSS#375	T14
ALB	VSS#249				
ALB	VSS#250				

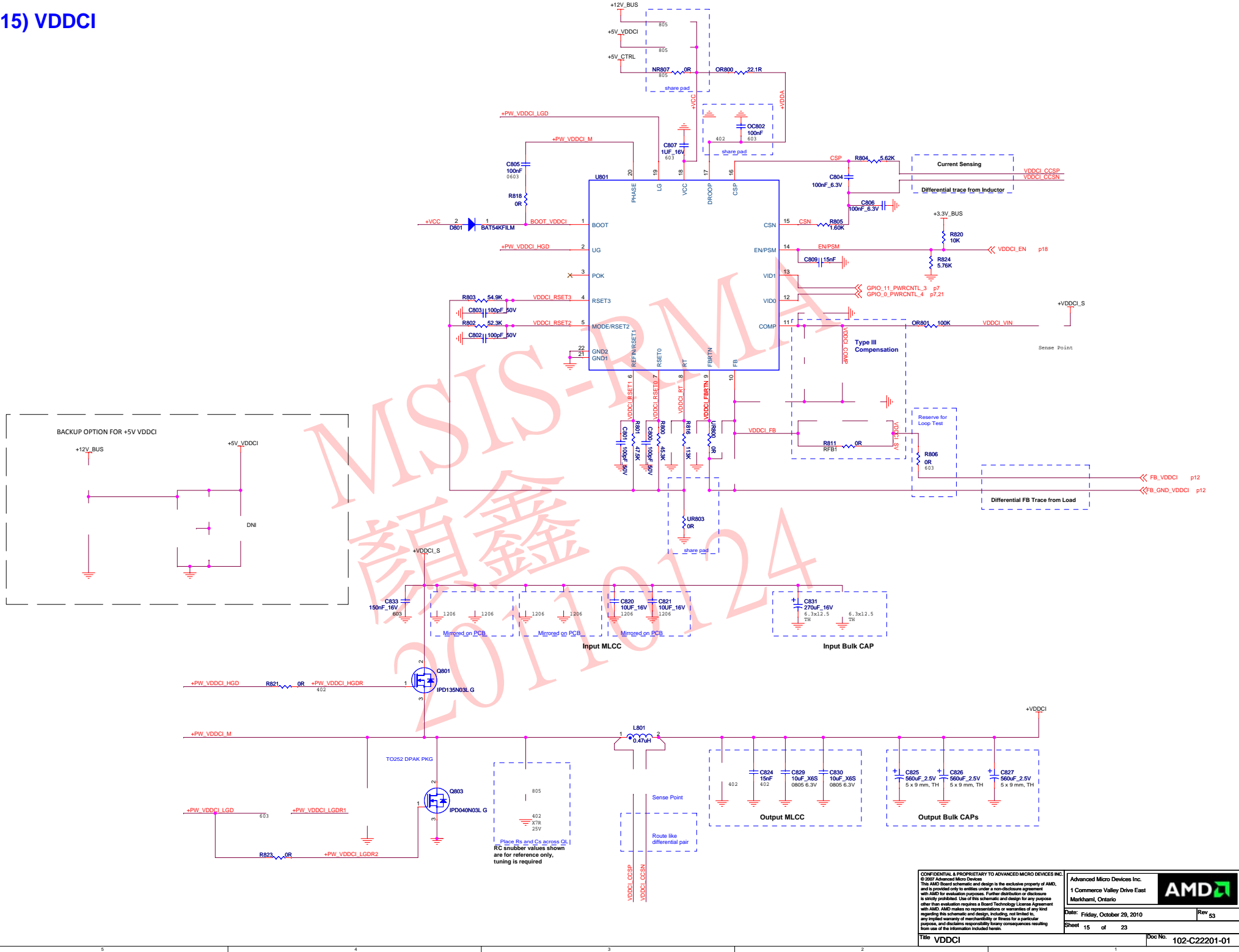
BARTS XT AT1 HF SLY BIN1 TSMC FB14

UR		PART 18 OF 19	
BA17	VSS#251	VSS#376	L42
BA19	VSS#252	VSS#377	L48
BA2	VSS#253	VSS#378	L6
BA21	VSS#254	VSS#379	M11
BA24	VSS#255	VSS#380	M13
BA27	VSS#256	VSS#381	M16
BA30	VSS#257	VSS#382	M33
BA32	VSS#258	VSS#383	M45
BA35	VSS#259	VSS#384	M48
BA37	VSS#260	VSS#385	M8
BA40	VSS#261	VSS#386	N12
BA41	VSS#262	VSS#387	N14
BB11	VSS#263	VSS#388	N17
BB16	VSS#264	VSS#389	N19
BB18	VSS#265	VSS#390	N22
BB21	VSS#266	VSS#391	N24
BB26	VSS#267	VSS#392	N27
BB28	VSS#268	VSS#393	N30
BB31	VSS#269	VSS#394	N32
BB33	VSS#270	VSS#395	N35
BB40	VSS#271	VSS#396	N37
BB41	VSS#272	VSS#397	N40
BB51	VSS#273	VSS#398	N42
BB53	VSS#274	VSS#399	N48
BB8	VSS#275	VSS#400	P13
BC14	VSS#276	VSS#401	P16
BC15	VSS#277	VSS#402	P18
BC2	VSS#279	VSS#403	P21
BC23	VSS#280	VSS#404	P23
BC33	VSS#281	VSS#405	P26
BC40	VSS#282	VSS#406	P28
CC6	VSS#283	VSS#407	P31
DD15	VSS#284	VSS#408	P33
DD18	VSS#285	VSS#409	P36
DD20	VSS#286	VSS#410	P38
DD38	VSS#287	VSS#411	P41
BE12	VSS#288	VSS#412	P43
BE16	VSS#289	VSS#413	P46
BE2	VSS#290	VSS#414	P48
BE40	VSS#291	VSS#415	P5
BF14	VSS#292	VSS#416	P6
BF16	VSS#293	VSS#417	R10
BF19	VSS#294	VSS#418	R12
BF21	VSS#295	VSS#419	R2
BF26	VSS#296	VSS#420	R44
BF32	VSS#297	VSS#421	R48
BF9	VSS#298	VSS#422	R50
CC2	VSS#299	VSS#423	T11
GG6	VSS#300	VSS#424	T12
BH1	VSS#301	VSS#425	T14
BH11	VSS#302	VSS#426	T19
BH12	VSS#303	VSS#427	T22
BH14	VSS#304	VSS#428	T24
BH15	VSS#305	VSS#429	T27
BH38	VSS#306	VSS#430	T30
BH39	VSS#307	VSS#431	T32
BH40	VSS#308	VSS#432	T35
BH7	VSS#309	VSS#433	T38
BL15	VSS#310	VSS#434	T39
BL16	VSS#311	VSS#435	T40
BL38	VSS#312	VSS#436	T42
BM11	VSS#313	VSS#437	T43
BM13	VSS#314	VSS#438	T46
BM7	VSS#315	VSS#439	T51
BM9	VSS#316	VSS#440	T53
BN16	VSS#317	VSS#441	T58
BN38	VSS#318	VSS#442	T61
F10	VSS#319	VSS#443	T63
F11	VSS#320	VSS#444	T68
F14	VSS#321	VSS#445	T72
F18	VSS#322	VSS#446	T75
F19	VSS#323	VSS#447	T78
F23	VSS#324	VSS#448	T81
F27	VSS#325	VSS#449	T83
F33	VSS#326	VSS#450	T86
F36	VSS#327	VSS#451	T88
F38	VSS#328	VSS#452	T91
F43	VSS#329	VSS#453	T93
F45	VSS#330	VSS#454	T96
F47	VSS#331	VSS#455	T98
F7	VSS#332	VSS#456	T101
G2	VSS#333	VSS#457	T103
G29	VSS#334	VSS#458	T106
G48	VSS#335	VSS#459	T108
G52	VSS#336	VSS#460	T11
G6	VSS#337	VSS#461	T12
H12	VSS#338	VSS#462	T14
H16	VSS#339	VSS#463	T17
H21	VSS#340	VSS#464	T20
H25	VSS#341	VSS#465	T23
H32	VSS#342	VSS#466	T26
H35	VSS#343	VSS#467	T28
H38	VSS#344	VSS#468	T31
H42	VSS#345	VSS#469	T33
H45	VSS#346	VSS#470	T36
H9	VSS#347	VSS#471	T39
J2	VSS	VSS#472	T42
J22	VSS#350	VSS#473	T45
J28	VSS#352	VSS#474	T48
J31	VSS#353	VSS#475	T51
J33	VSS#354	VSS#476	T52
J38	VSS#355	VSS#477	T53
J46	VSS#356	VSS#478	T56
J48	VSS#357	VSS#479	T58
J8	VSS#359	VSS#480	T61
K15	VSS#360	VSS#481	T63
K19	VSS#361	VSS#482	T68
K21	VSS#362	VSS#483	T72
K23	VSS#363	VSS#484	T75
K26	VSS#364	VSS#485	T78
K32	VSS#365	VSS#486	T81
K36	VSS#366	VSS#487	T83
K6	VSS#368	VSS#488	T86
K8	VSS#369	VSS#489	T88
L12	VSS#370	VSS#490	T91
L16	VSS#371	VSS#491	T93
L18	VSS#372	VSS#492	T96
L29	VSS#373	VSS#493	T98
L37	VSS#374	VSS#494	T101
L38	VSS#375	VSS#495	T103



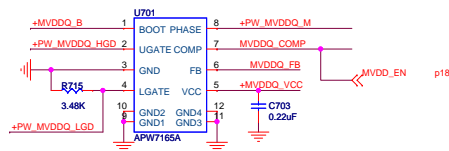


# (15) VDDCI



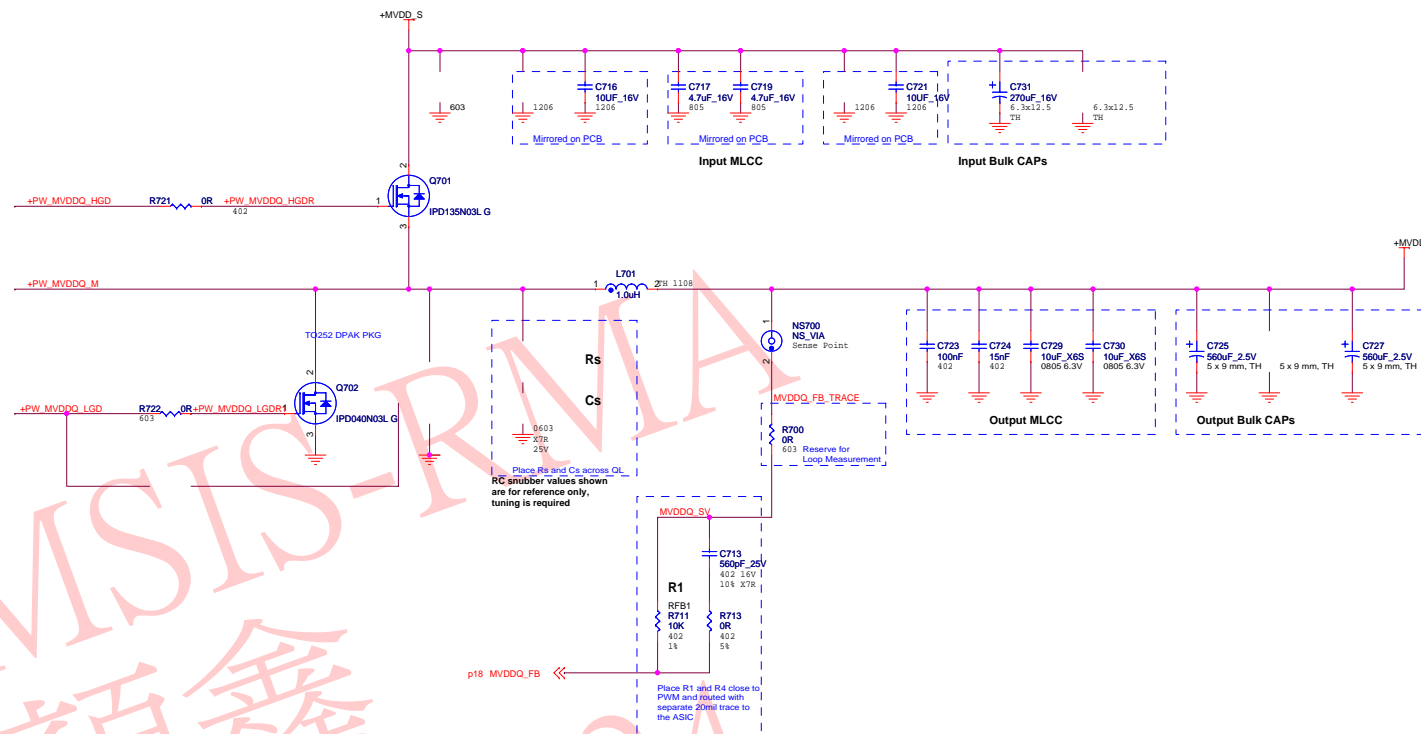


# (16) MVDD

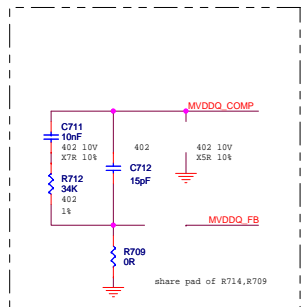


## Layout guideline

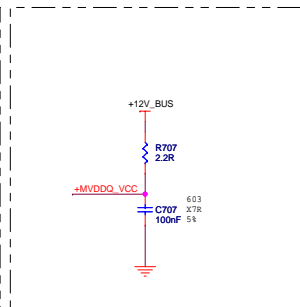
- 1-Position the controller (U701) such that LGate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces (+PW\_MVDDQ\_LGD and +PW\_MVDDQ\_HGD) as short and as wide as possible to reduce the trace inductance.
- 2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows:  
Vcc bypass cap is C703, and Boost cap is C705.
- 3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



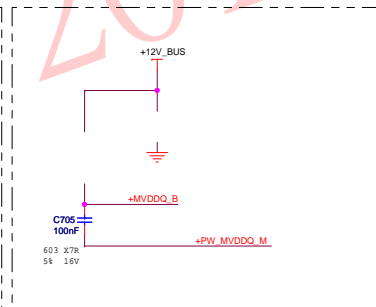
## COMPENSATION CIRCUIT




## FILTERED SMPS VCC



## BOOT CIRCUIT

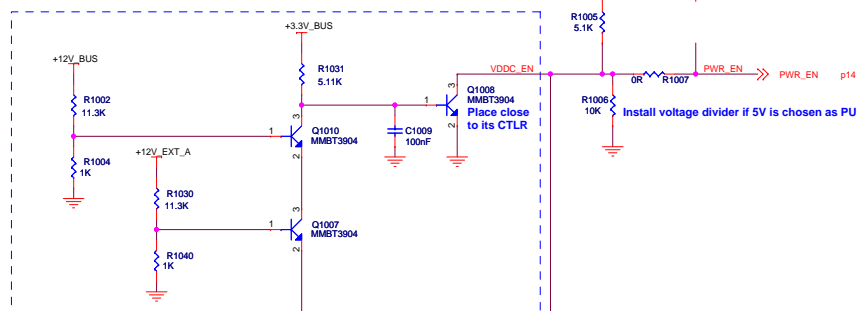
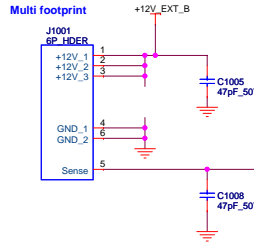
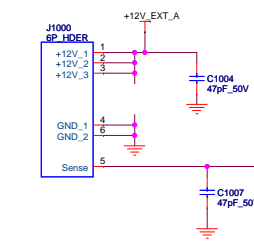


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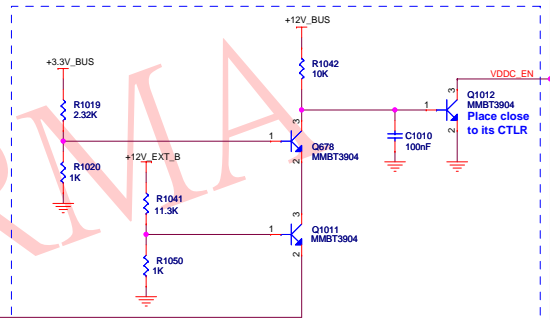
Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario			
Date: Friday, October 29, 2010			Rev 53
Sheet 16 of 23			

Title: MVDD

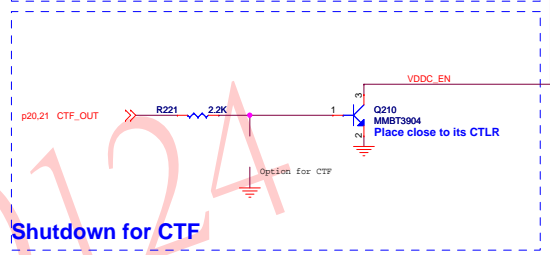
(19) BARTS / CYPRESS POWER MGMNT



BUS 12V and AUX A Power up Seq

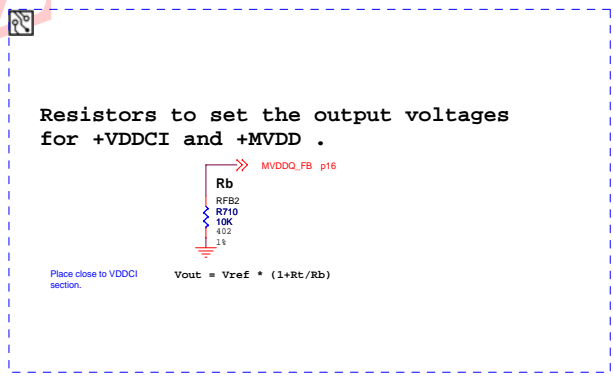
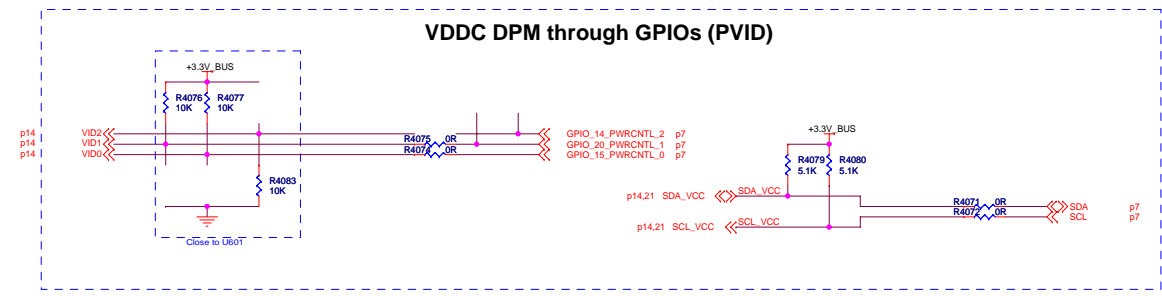
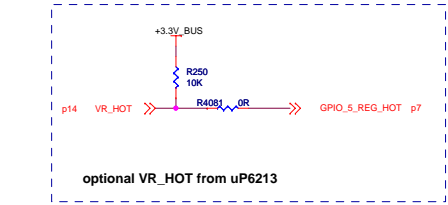
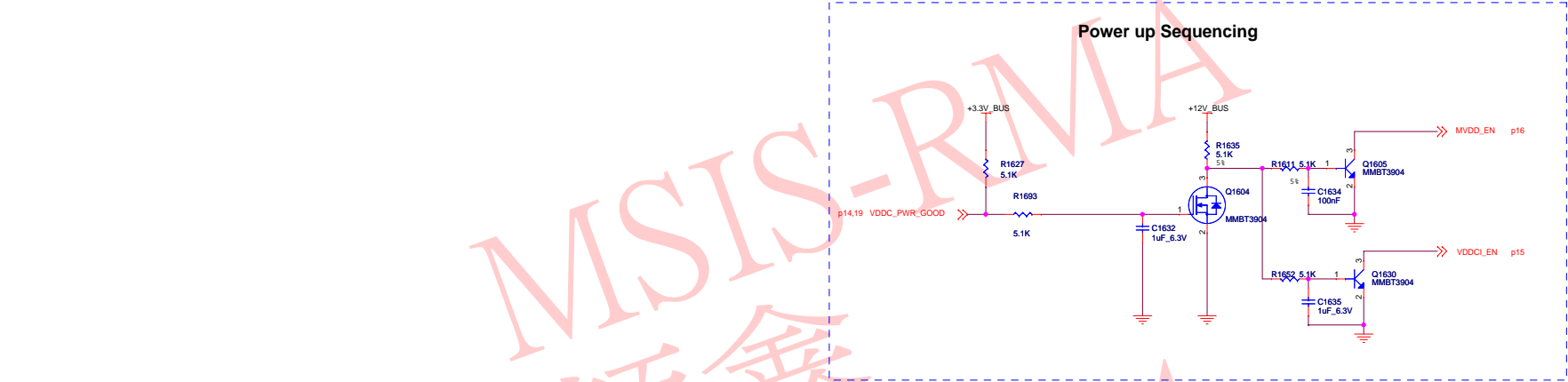
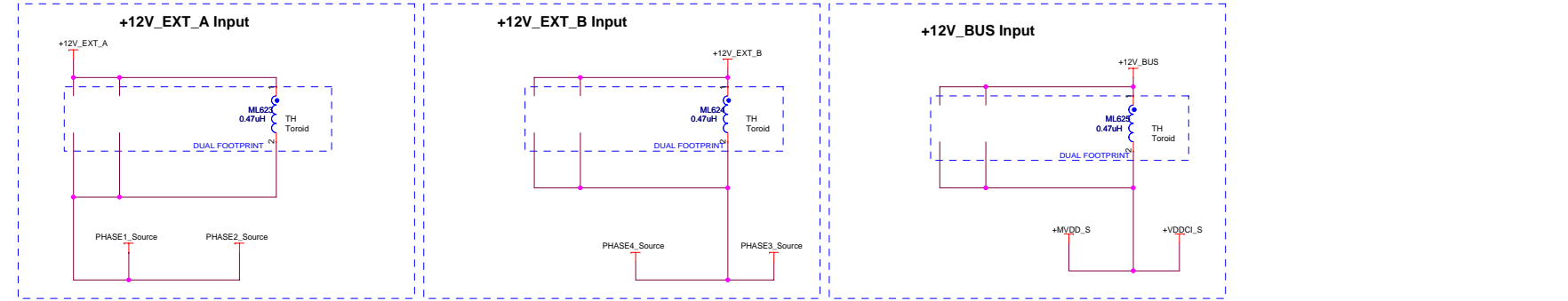


BUS 3.3V and AUX B Power up Seq



Shutdown for CTF

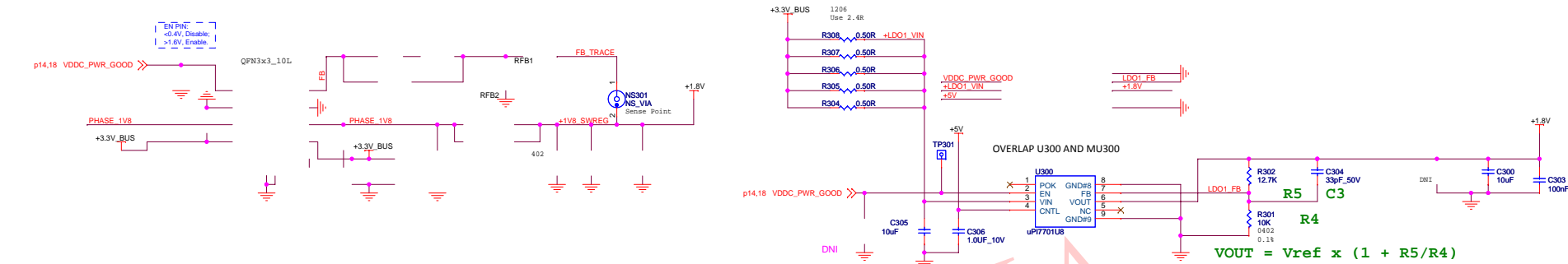
(17) BARTS / CYPRESS VDDCI POWER PLAY



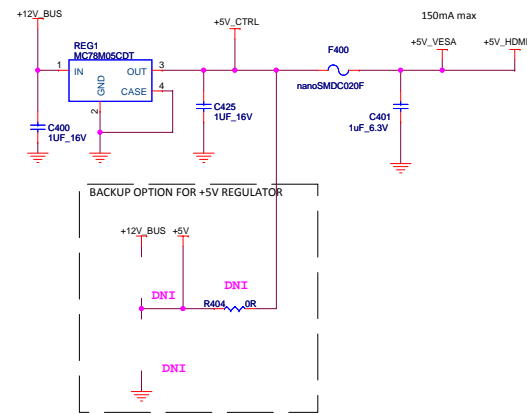


(18) BARTS / CYPRESS Small Rail Regulators

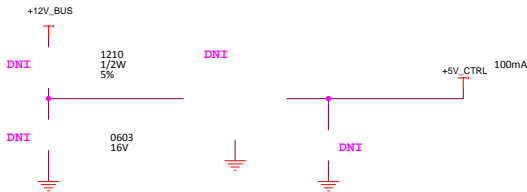
LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling



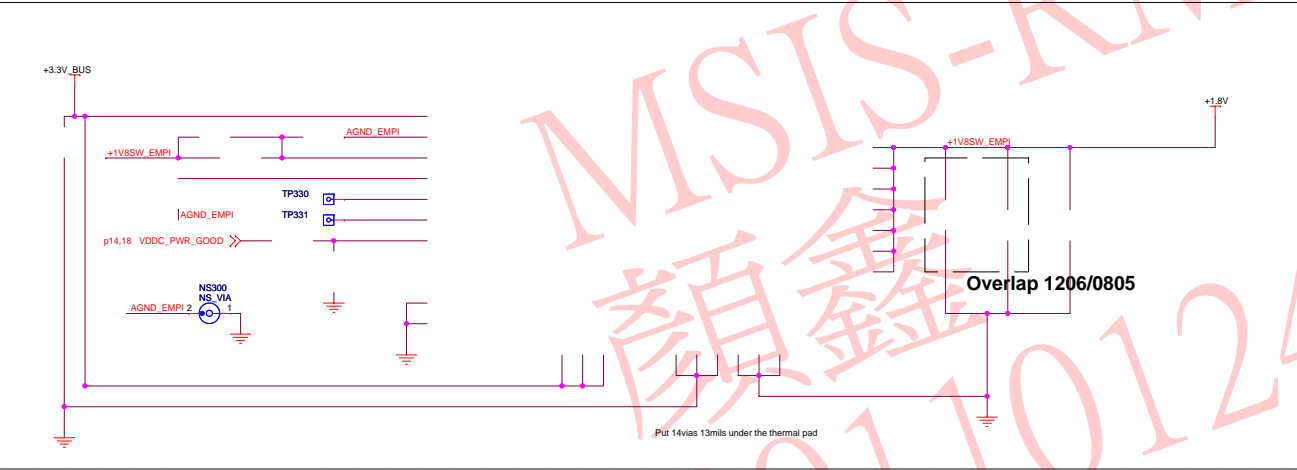
Regulators for +5V, +5V\_VESA and +5V\_HDMI  
Iout max = 150mA (DVI+HDMI)



optional 5V power for VDDC regulator;

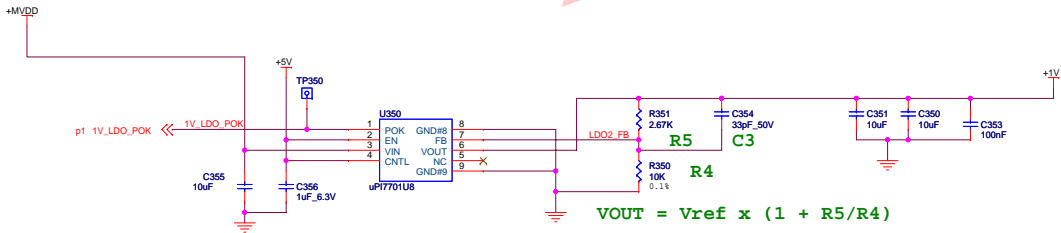


Other cheaper solution at 5MHz switching for 1.8V

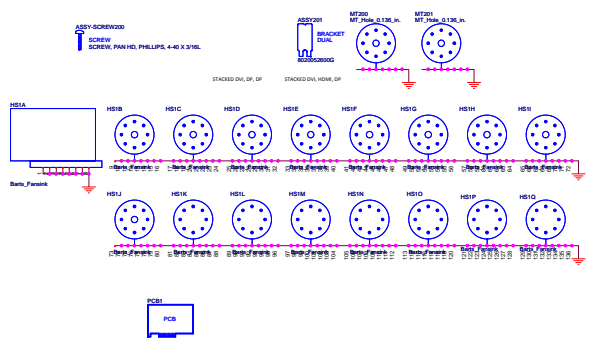
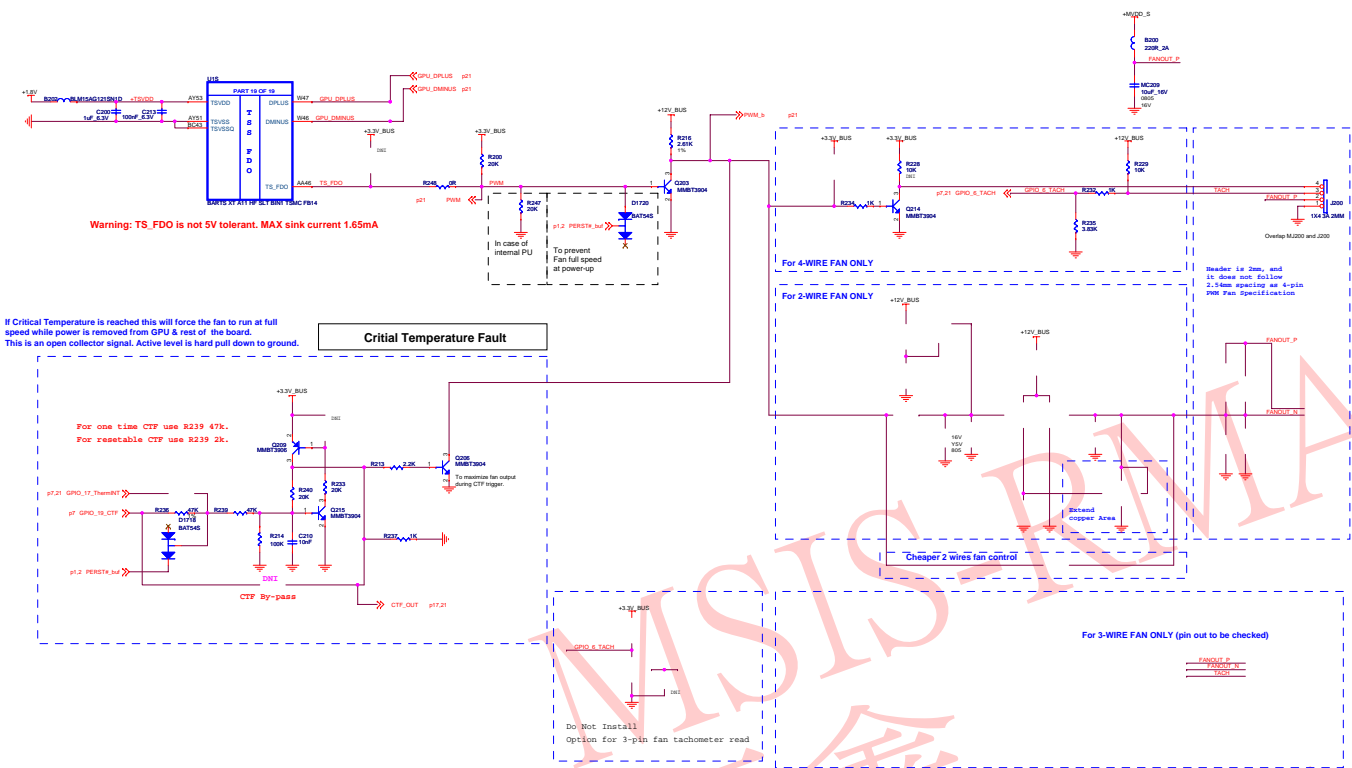


LDO #2: Vin = +1.35V to 1.8V MAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling

OVERLAP ALTERNATE CAP FOOTPRINTS

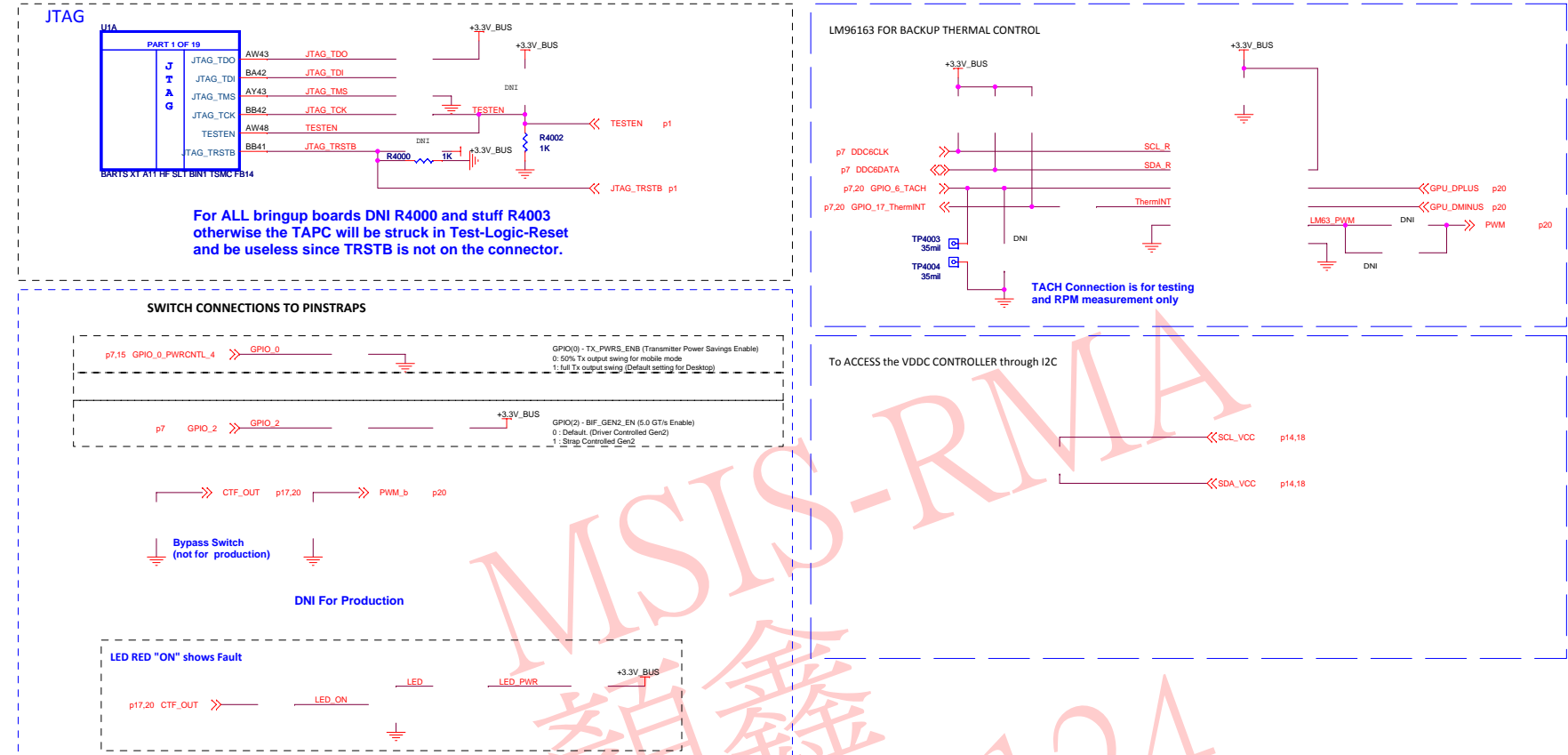


## (20) BARTS / CYPRESS Mechanical and Thermal Management



- FANSINK solutions
1. XT HS P/N - 7121294000G
  2. PRO HS P/N - TBD
- MOSFET Heatsink MT
1. Passive HS 7120194000G
- BRACKET solutions
1. DS mDP, mDP, HDMI, Stacked DVI 8020052600G
  2. SS mDP, mDP, DVI

(21) CYPRESS Debug Circuits







Title  
RH BARTS CYPRESS GDDR5 mDP-mDP-HDMI-DVII-DVII

Schematic No.  
102-C22201-01

Date:  
Friday, October 29, 2010

## REVISION HISTORY

**NOTE:** This schematic represents the PCB, it does not represent any specific SKU.  
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.  
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev	53
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Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	19/04/2010	Initial release. Based on C220
1	00B	09/08/2010	Page01: Added direct connection from Pull-Up for MUI01 for Cypress Page09: remove the inductor for top DVI line Page14: update Q601,Q602,Q603,Q604 symbol Page17: add C211 Page20: add R201, R237, R241. Page18: add optional 3-pin fan tach circuitry/ Page50: update block diagram