P73, NV17, 4/8Mx16 DDR, 32/64MB, Dual RGB, TV-out, Video Capture, AGP4X

PCI DEVICE ID = 0X172 FOR GF4-MX420-XX.

PRIMARY ** VGA1 DAC_A ** I2C1.
SECONDARY ** VGA2 DAC_B ** I2C0.
VIDCAP ** VIP 7114 I2C2.
9pin DIN ** RGB2 I2C2. See PDS for Hookup

P73-A00-X01

Created SCH from P78-X16 for I/O Netlist only

P73-A00-X02

CREATED NX16 MEMORY, DECOUPLING FROM P78

P73-A00-X03

ADDED MEM & CORE FROM P70 PS FOR ISL6529

SAA7114 DECAPS ADDED AND CHANGED TO 0402

P73-A00-X04

PCB Footprint for RAM added

P73-A00-X05

C620, C621 Removed
Extra Mem Decaps removed

P73-A00-X06

PCB Footprint for Inductor, Stacked DB15, ISL6529 added

PCB Footprint for L305, L307, L308, L316-L324 changed to 0603 from 0805.
Added X-Comp R750, R751.

P73-A00-X07

TV-XTAL should be 18pf CL.
Each memory with separate clock

P73-A00-X08

U700-Parallel ROM and C700 decap Removed for space

P73-A00-X09

0603 to 0402 Package Changes for 49 components

P73-A00-X10

Design Review Updates

0603 to 0402 Package Changes for 33 components

0805 to 0603 Package Changes for 17 components

0402 to 0603 Package Changes for 10 components

Removed 25 components

P73-A00-X11

Swaps in Memory termination RN201, RN203, RN205, RN207

P73-A00-X12

C606, C615 TH replacements, Removed for want of space.

P73-A00-X13

Memory bus swaps on 1/11/02-Swap 2

P73-A00-X14

Memory bus swaps on 1/12/02-Swap 3

P73-A00-X15

Memory bus byte swaps as per NV17-Ball arrangement

P73-A00-X16

Memory bus byte and bit swaps as per layout

TV Filter moved to VGA2 page with more routing notes

P73-A00-X17

The C397, C311, C318 changed to 0603 from 0402 for two trace routing near GPU break out.
P300-2 Mounting pins removed from CGND

P73-A00-X18

Added X Components C824 to C830 to FBVDDQ

P73-A00-X19

Added X Components C831 to C832 to FBVDDQ

R610, R612 for FBVDDQ re-fixed to have <5K for Rfb

P73-A00-X20- X-Rel Candidate

Clean-up for Agile upload
Memory de-coupling values modified as per layout.

P73-A00-X21- ECO-3893

Q600 Should be FET istead of BJT Transistor.

P73-A00-X22-

Corrected NV17-S sku in the table in this page

P73-A01-X01

The RED and GREEN signal to TV filter interchanged. Corrected by swapping CVBS_YOUT and COUT.

P73-A01-X02

Corrected by swapping CVBS_YOUT and COUT at DIN

Type 3 Compensation Values for ISL6529 changed
C616---NS---47nF
R614---NS---8.06K
C618---33nF---70nF
R611---16.2K---6.65K
C619---33nF----1.8nF

AGPSTOP to 3.3V
R616 -47R inseries to 12V for ISL6529 is too high, changed to 4.7R

P73-A01-X03-Final Netlist

R616 -4.7R inseries to 12V for ISL6529 is changed to 0R

R624 - Added 2.2R inseries to 5V for ISL6529.

ISL6529 Compensation Res to be Type 2 with Snubber coponents stuffed. Values under test.

P73-A01-X04-For X-Rel

The Type 2 Compensation works better than Type 3 Compensation.
C616. R614 No Stuff, R614 Nostuff, C618 3300pf, R611 16.2K, C619 33pF, R616 0R
Snubber values are
R626 2.2R, C617 2200PF

P73-A01-X05-ECO4193

The Type 3 Compensation works better than Type 2 Compensation in the new layout with new values tried at Intersil.
C616-47nF. R614-10R, C618 1000pf, R611-10K, C619 1500pF.

Stuff Option	Meaning
COMMON	Common to all assemblies and 1st VGA comps
NO STUFF	Not present in any assembly
VIDCAP	Video In or Video Capture
VGA2	2nd VGA Components and Conenctor
DSUB	Standard single VGA Connector
TV	Second DAC channel goes to Svideo connector as TV Out
TVO	4pin DIN for TV Only
1117	Fixed 1117 linear regulator for A3.3V
1117_ADJ	Adjustable 1117 linear regulator for A3.3V
NO_1117	Connect A3.3V to 3.3V. No 1117 regulator.
CLAMP1	VGA1 Sync/I2C Clamping diodes
RGB_PROT	RGB Protection diodes on primary DAC outputs
CLAMP2	VGA2 Sync/I2C Clamping diodes
RGB2_PROT	RGB Protection diodes on secondary DAC outputs
CLAMP3	VIDCAP I2C/Video In Clamping diodes
TVCLAMP	TV Red/Green Clamping diodes
GPU	GPU ONLY
NV17-S	IDSTRAP OPTION-172H
MEMORY	Memory only
M2-8V	Memory PS output 2.8V
M2-5V	Memory PS output 2.5V

PAGE OVERVIEW

1 top (this) page
2 1. AGP interface, core decoupling
3 2.a NV17 Frame Buffer
4 3.a Dual DAC, 1st VGA
5 3.b Dual DAC, 2nd VGA
6. 3.c TMDS NV17
7 4.a Frame Buffer 0..31
8 4.b Frame Buffer 32...63
9 5. TV-out, video capture, stereo
10 6. Power supply
11 7. BIOS, Strapping

140-10073-0000-A01
602-10073-0000-A01

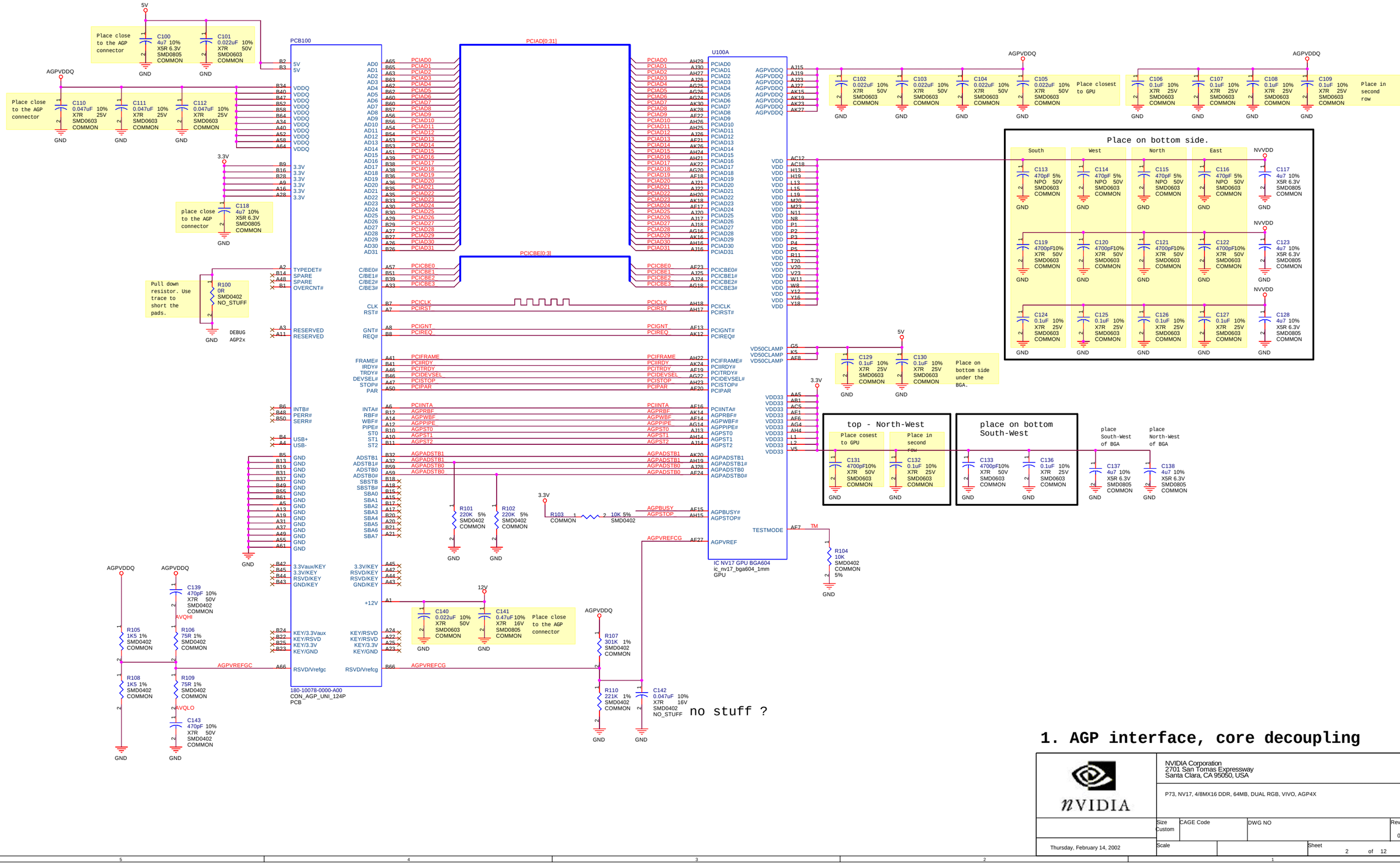
NVIDIA Corporation
3535 Monroe St
Santa Clara, CA 95051, USA

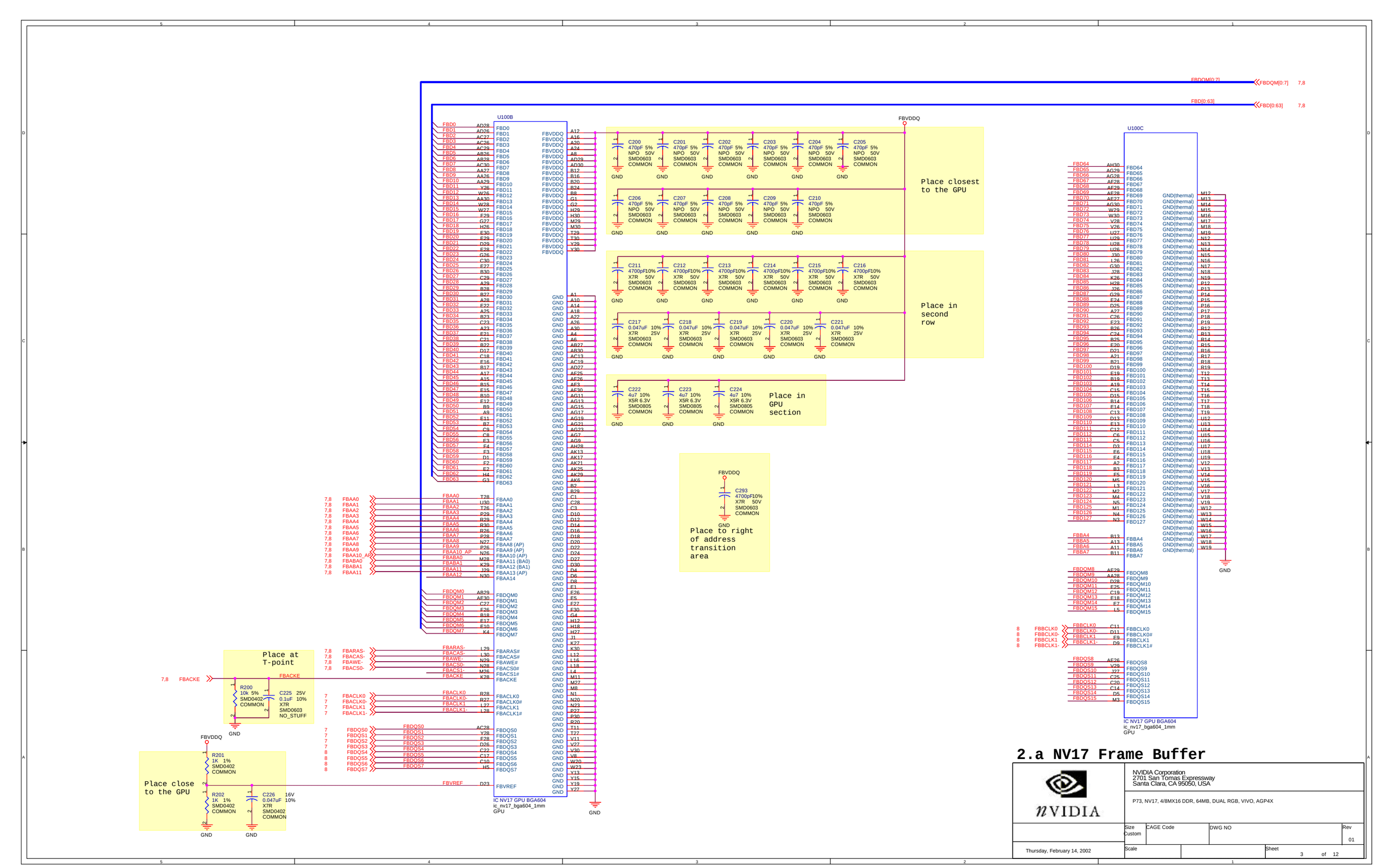
P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X

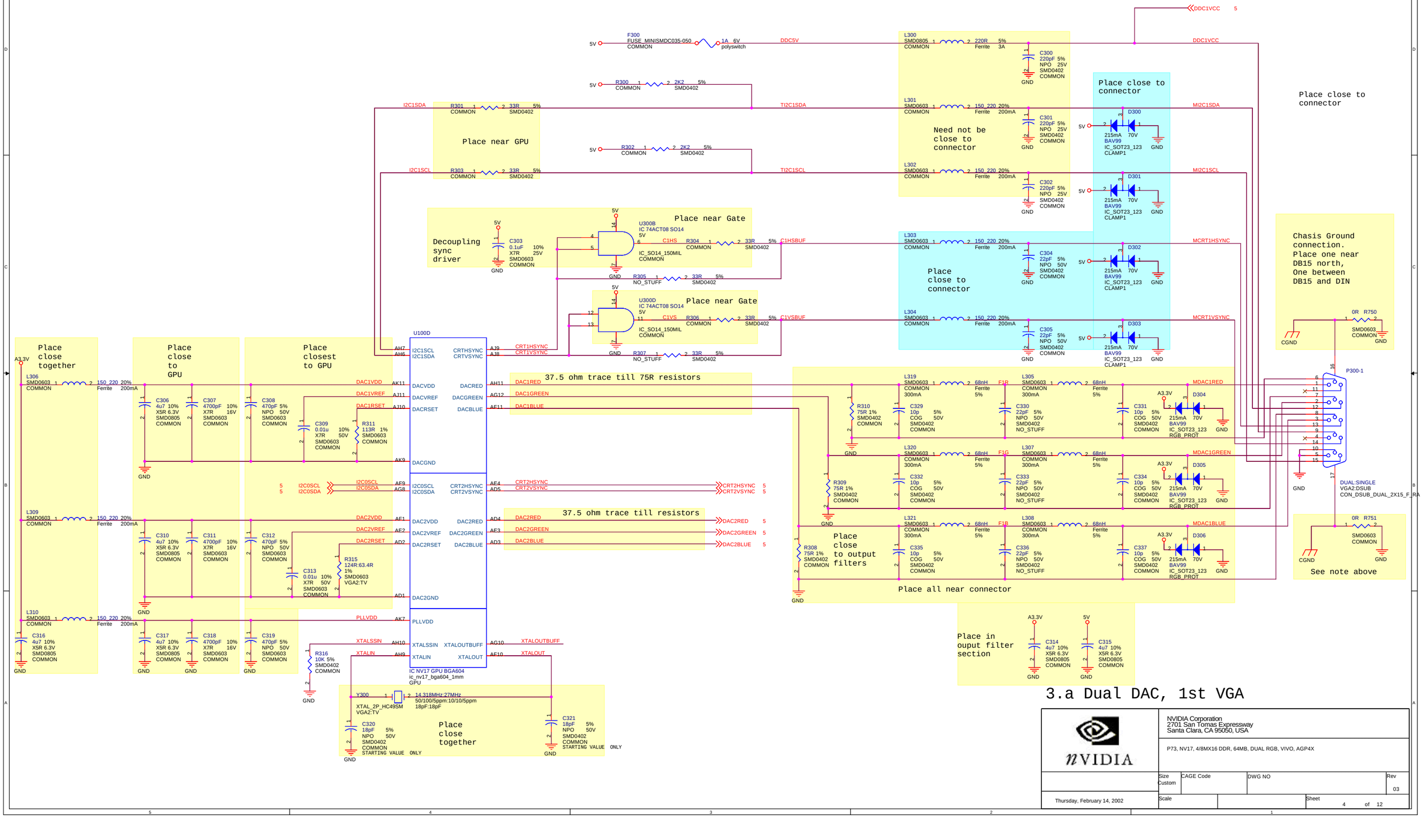
Size	CAGE Code	DWG NO	Rev
Custom			05

Thursday, February 14, 2002 | Scale | Sheet 1 of 11

{Item}\t{Quantity}\t{Reference}\t{Value}\t{Assembly}\t{MAIN}\t{NVPN}\t{Source Package}\t{AVL1}\t{AVL2}\t{AVL3}\t{AVL4}\t{AVL5}
Item\tQuantity\tReference\tValue\tAssembly\tMAIN\tNVPN\tSource Package\tAVL1\tAVL2\tAVL3\tAVL4\tAVL5


PCB100
U100A
PCIAD[0:31]
PCICBE[0:3]
Place close to the AGP connector
C100 4u7 10% X5R 6.3V SMD0805 COMMON
C101 0.022uF 10% X7R 50V SMD0603 COMMON
C110 0.047uF 10% X7R 25V SMD0603 COMMON
C111 0.047uF 10% X7R 25V SMD0603 COMMON
C112 0.047uF 10% X7R 25V SMD0603 COMMON
C118 4u7 10% X5R 6.3V SMD0805 COMMON
Pull down resistor. Use trace to short the pads.
R100 0R SMD0402 NO_STUFF
DEBUG AGP2x
R101 220K 5% SMD0402 COMMON
R102 220K 5% SMD0402 COMMON
R103 10K 5% SMD0402 COMMON
R104 10K SMD0402 COMMON 5%
C102 0.022uF 10% X7R 50V SMD0603 COMMON
C103 0.022uF 10% X7R 50V SMD0603 COMMON
C104 0.022uF 10% X7R 50V SMD0603 COMMON
C105 0.022uF 10% X7R 50V SMD0603 COMMON
Place closest to GPU
C106 0.1uF 10% X7R 25V SMD0603 COMMON
C107 0.1uF 10% X7R 25V SMD0603 COMMON
C108 0.1uF 10% X7R 25V SMD0603 COMMON
C109 0.1uF 10% X7R 25V SMD0603 COMMON
Place in second row
Place on bottom side.
South
West
North
East
C113 470pF 5% NPO 50V SMD0603 COMMON
C114 470pF 5% NPO 50V SMD0603 COMMON
C115 470pF 5% NPO 50V SMD0603 COMMON
C116 470pF 5% NPO 50V SMD0603 COMMON
C117 4u7 10% X5R 6.3V SMD0805 COMMON
C119 4700pF10% X7R 50V SMD0603 COMMON
C120 4700pF10% X7R 50V SMD0603 COMMON
C121 4700pF10% X7R 50V SMD0603 COMMON
C122 4700pF10% X7R 50V SMD0603 COMMON
C123 4u7 10% X5R 6.3V SMD0805 COMMON
C124 0.1uF 10% X7R 25V SMD0603 COMMON
C125 0.1uF 10% X7R 25V SMD0603 COMMON
C126 0.1uF 10% X7R 25V SMD0603 COMMON
C127 0.1uF 10% X7R 25V SMD0603 COMMON
C128 4u7 10% X5R 6.3V SMD0805 COMMON
C129 0.1uF 10% X7R 25V SMD0603 COMMON
C130 0.1uF 10% X7R 25V SMD0603 COMMON
Place on bottom side under the BGA.
top - North-West
Place cosest to GPU
Place in second row
C131 4700pF10% X7R 50V SMD0603 COMMON
C132 0.1uF 10% X7R 25V SMD0603 COMMON
place on bottom South-West
C133 4700pF10% X7R 50V SMD0603 COMMON
C136 0.1uF 10% X7R 25V SMD0603 COMMON
place South-West of BGA
place North-West of BGA
C137 4u7 10% X5R 6.3V SMD0805 COMMON
C138 4u7 10% X5R 6.3V SMD0805 COMMON
C139 470pF 10% X7R 50V SMD0402 COMMON
C140 0.022uF 10% X7R 50V SMD0603 COMMON
C141 0.47uF 10% X7R 16V SMD0805 COMMON
Place close to the AGP connector
C142 0.047uF 10% X7R 16V SMD0402 NO_STUFF
R105 1K5 1% SMD0402 COMMON
R106 75R 1% SMD0402 COMMON
R107 301K 1% SMD0402 COMMON
R108 1K5 1% SMD0402 COMMON
R109 75R 1% SMD0402 COMMON
R110 221K 1% SMD0402 COMMON
C143 470pF 10% X7R 50V SMD0402 COMMON
180-10078-0000-A00 CON_AGP_UNI_124P PCB
IC NV17 GPU BGA604 ic_nv17_bga604_1mm GPU
no stuff ?
1. AGP interface, core decoupling
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X
Thursday, February 14, 2002
Size Custom
CAGE Code
DWG NO
Rev 02
Scale
Sheet 2 of 12


FBDQM[0:7]
FBDQM[0:7] 7,8
FBD[0:63]
FBD[0:63] 7,8
U100B
FBVDDQ
C200 470pF 5% NPO 50V SMD0603 COMMON
C201 470pF 5% NPO 50V SMD0603 COMMON
C202 470pF 5% NPO 50V SMD0603 COMMON
C203 470pF 5% NPO 50V SMD0603 COMMON
C204 470pF 5% NPO 50V SMD0603 COMMON
C205 470pF 5% NPO 50V SMD0603 COMMON
C206 470pF 5% NPO 50V SMD0603 COMMON
C207 470pF 5% NPO 50V SMD0603 COMMON
C208 470pF 5% NPO 50V SMD0603 COMMON
C209 470pF 5% NPO 50V SMD0603 COMMON
C210 470pF 5% NPO 50V SMD0603 COMMON
Place closest to the GPU
C211 4700pF 10% X7R 50V SMD0603 COMMON
C212 4700pF 10% X7R 50V SMD0603 COMMON
C213 4700pF 10% X7R 50V SMD0603 COMMON
C214 4700pF 10% X7R 50V SMD0603 COMMON
C215 4700pF 10% X7R 50V SMD0603 COMMON
C216 4700pF 10% X7R 50V SMD0603 COMMON
C217 0.047uF 10% X7R 25V SMD0603 COMMON
C218 0.047uF 10% X7R 25V SMD0603 COMMON
C219 0.047uF 10% X7R 25V SMD0603 COMMON
C220 0.047uF 10% X7R 25V SMD0603 COMMON
C221 0.047uF 10% X7R 25V SMD0603 COMMON
Place in second row
C222 4u7 10% X5R 6.3V SMD0805 COMMON
C223 4u7 10% X5R 6.3V SMD0805 COMMON
C224 4u7 10% X5R 6.3V SMD0805 COMMON
Place in GPU section
FBVDDQ
C293 4700pF 10% X7R 50V SMD0603 COMMON
Place to right of address transition area
U100C
Place at T-point
R200 10k 5% SMD0402 COMMON
C225 25V 0.1uF 10% X7R SMD0603 NO_STUFF
FBACKE
FBVDDQ
R201 1K 1% SMD0402 COMMON
R202 1K 1% SMD0402 COMMON
C226 16V 0.047uF 10% X7R SMD0402 COMMON
Place close to the GPU
FBVREF
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
GPU
GND
2.a NV17 Frame Buffer
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X
Thursday, February 14, 2002
Size Custom
CAGE Code
DWG NO
Rev 01
Scale
Sheet 3 of 12



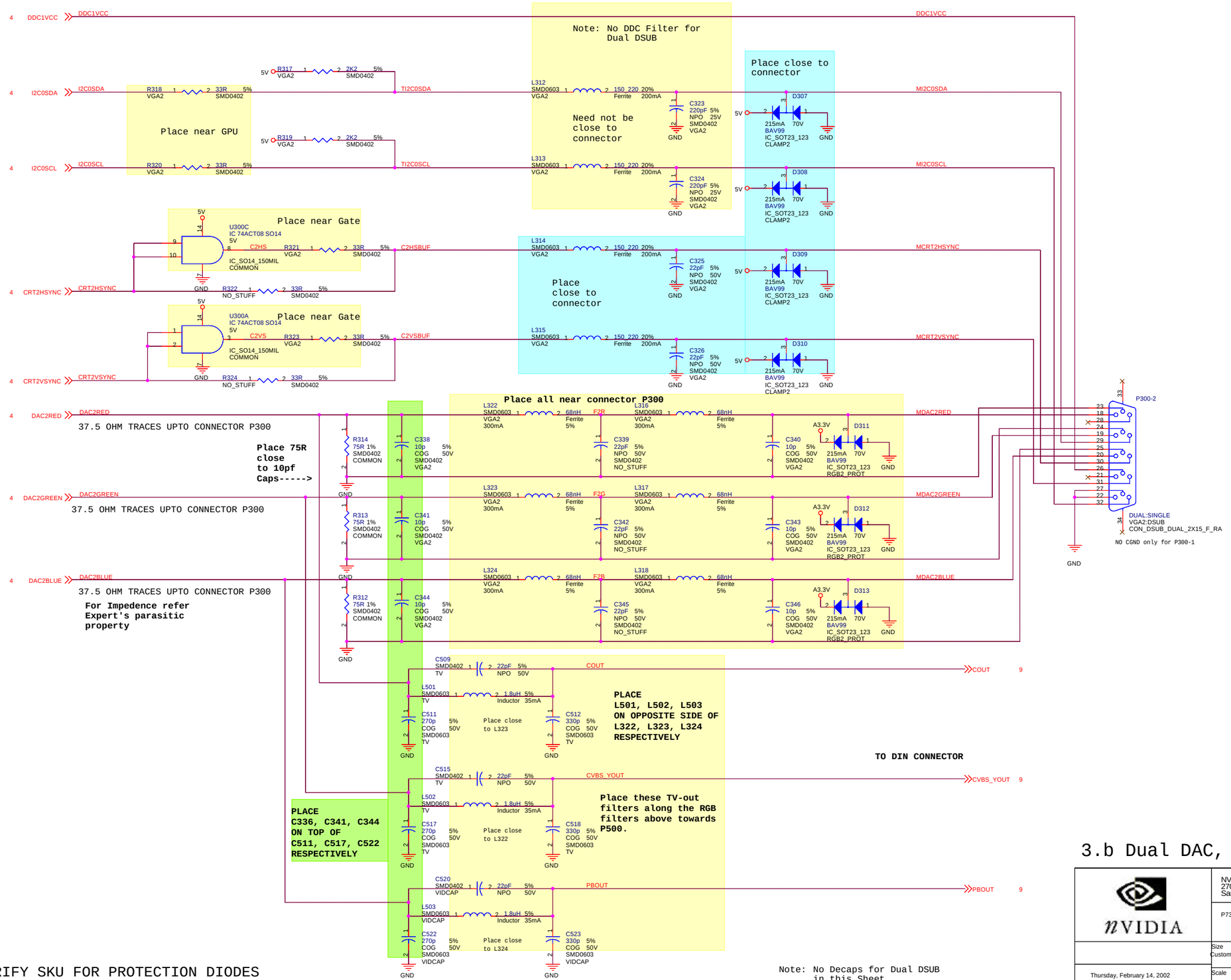
3.a Dual DAC, 1st VGA

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X

Size	CAGE Code	DWG NO	Rev
Custom			03

Thursday, February 14, 2002 | Scale | Sheet 4 of 12

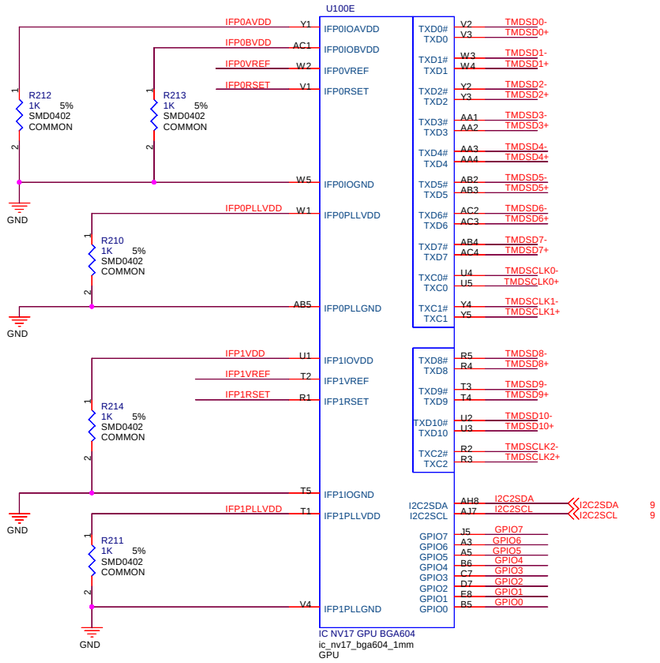


3.b Dual DAC, 2nd VGA

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X

Size	CAGE Code	DWG NO	Rev
Custom			03
Thursday, February 14, 2002	Scale		Sheet 5 of 11



Place
close
together

3.c TMDS_NV17

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Santa Clara, CA 95050, USA

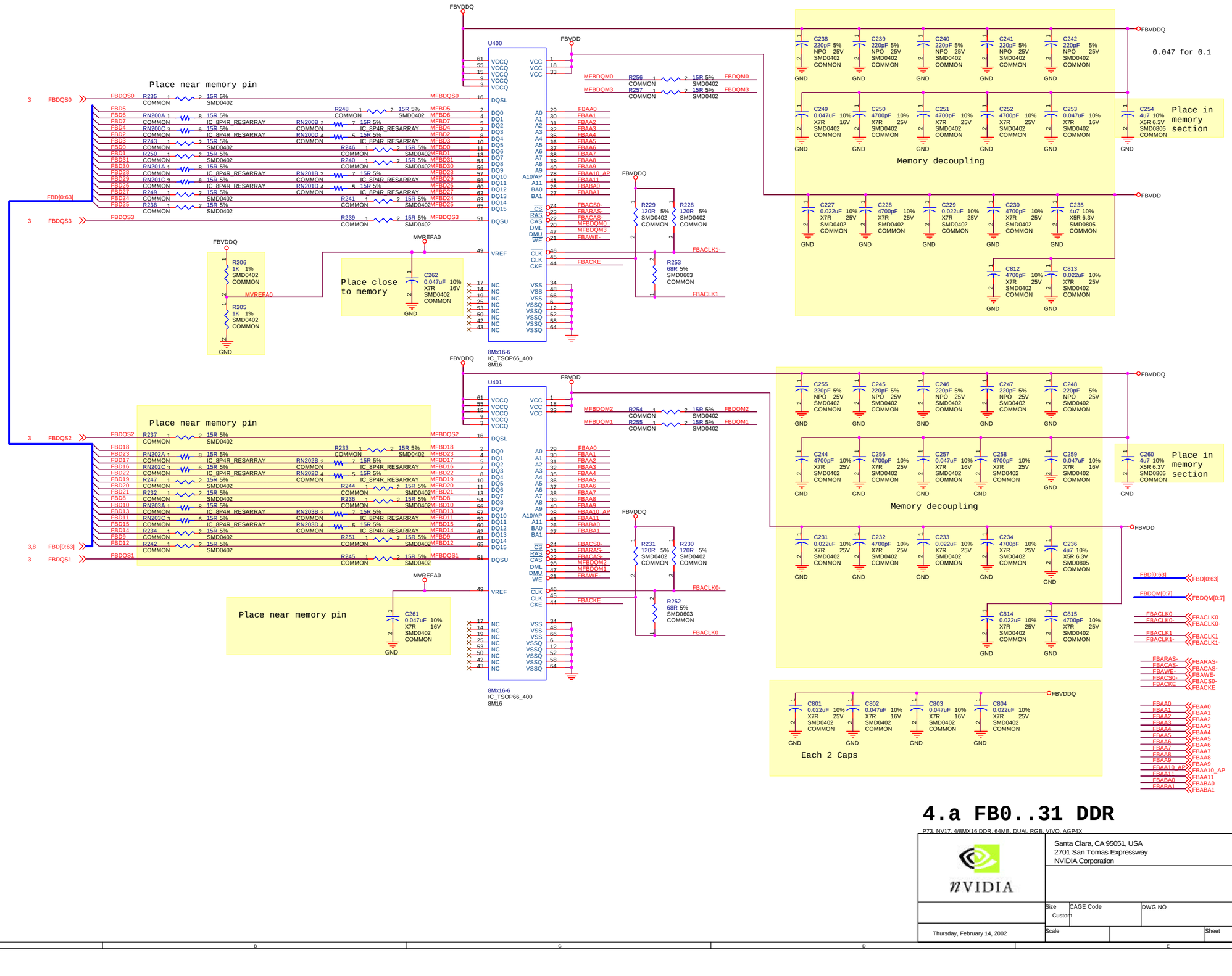
P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X

Size	CAGE Code	DWG NO	Rev
Custom			5

Thursday, February 14, 2002

Scale

Sheet 6 of 12



4.a FB0..31 DDR

P73_NV17_4/8MX16_DDR_64MB_DUAL_RGB_VIVO_AGP4X

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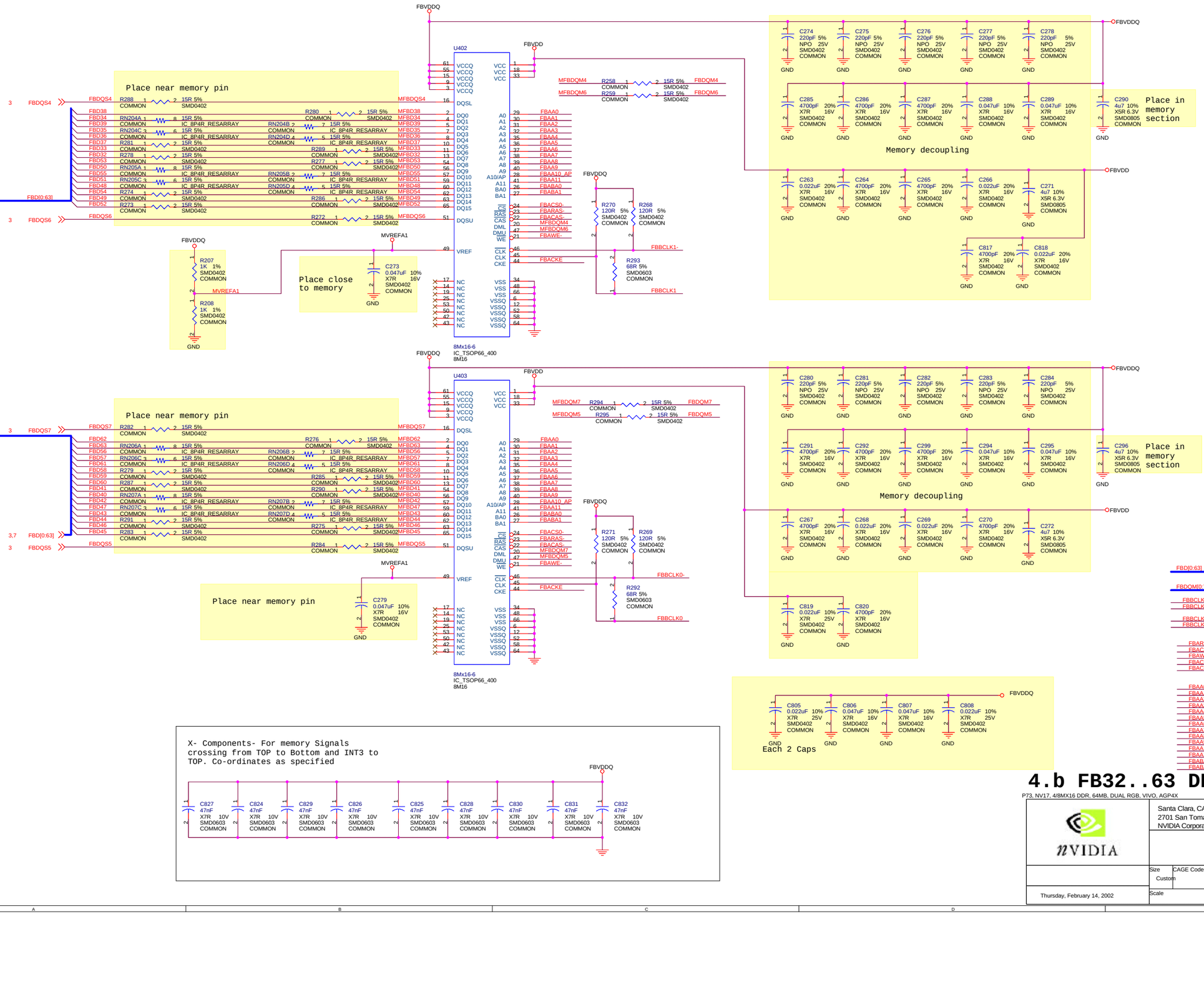
NVIDIA Corporation

Size	CAGE Code	DWG NO	Rev
Custom			A
Thursday, February 14, 2002	Scale	Sheet 7 of 12	



X- Components- For memory Signals crossing from TOP to Bottom and INT3 to TOP. Co-ordinates as specified

4.b FB32..63 DDR

P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X

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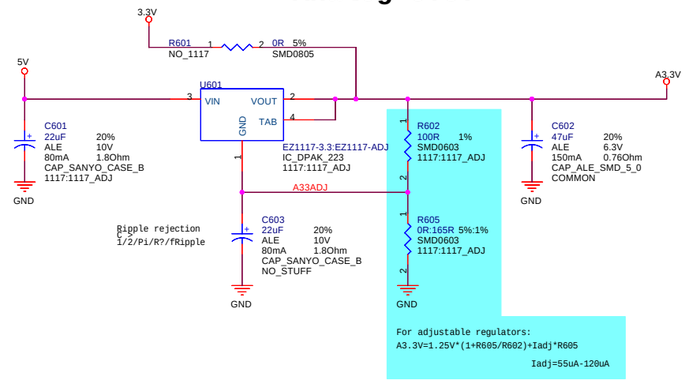
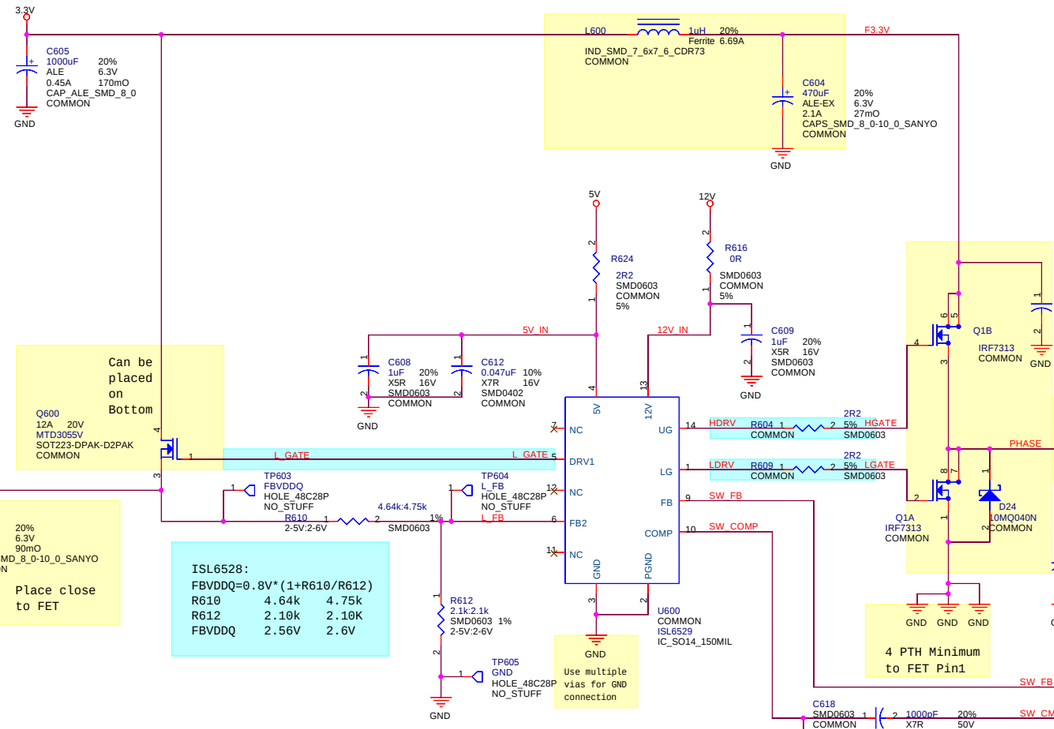
Size	CAGE Code	DWG NO	Rev
Custom			A
Thursday, February 14, 2002	Scale		Sheet 8 of 12

5. TV out,video capture

NVIDIA	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA	
	P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X	
Thursday, February 14, 2002	Size: Custom / CAGE Code / DWG NO / Rev: 08 Scale / Sheet: 9 of 12	

Analog 3.3V



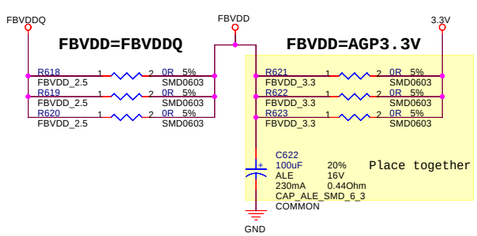


FOR DESKTOP-NV17
NVVDD DESIGN TARGET 1.584min/1.616max
NVVDD QUAL TARGET 1.550min/1.700max

NVVDD=1.60V +/-50mV /4A

FBVDDQ=2.53V +/-30mV

USE MAX WIDTH OF TRACES AS POSSIBLE



FBVDD

The FBVDD can take either FBVDDQ or AGP3.3V. Place the resistors accordingly for plane split.

6. Power supply

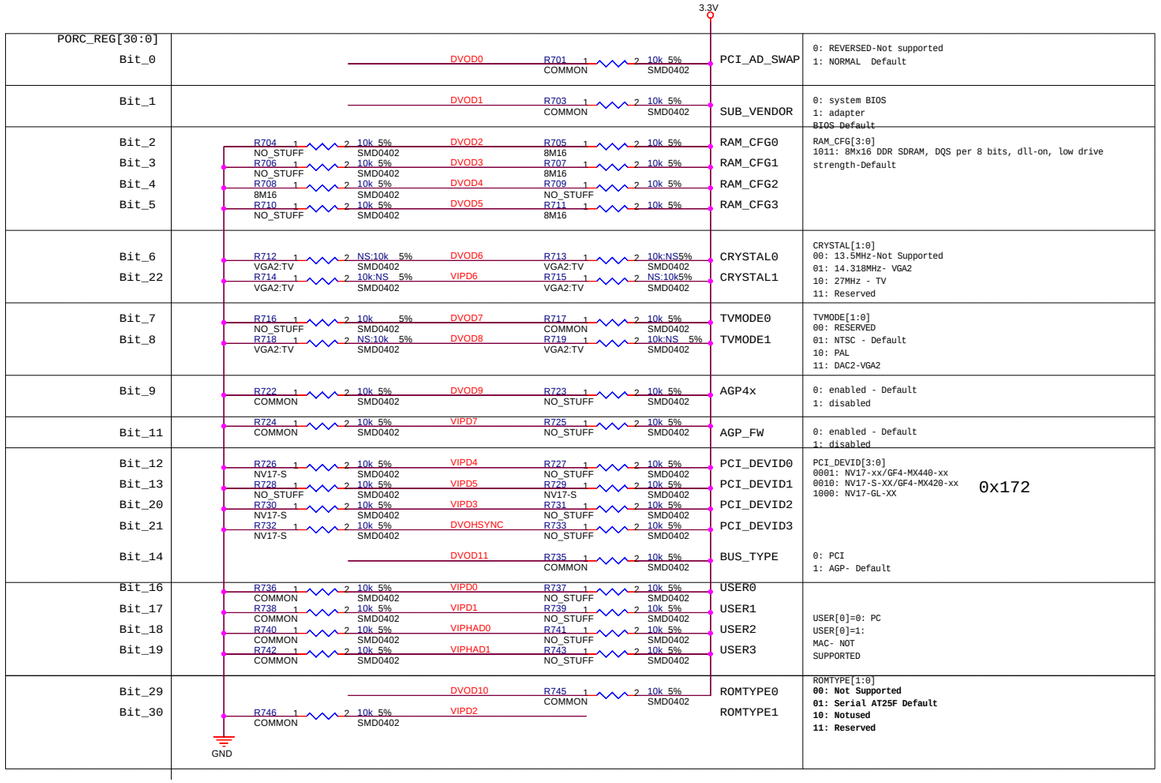
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

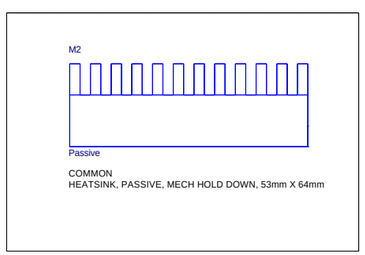
P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X

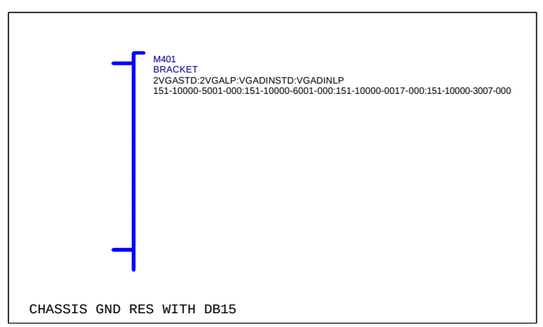
Size	CAGE Code	DWG NO	Rev
Custom			5

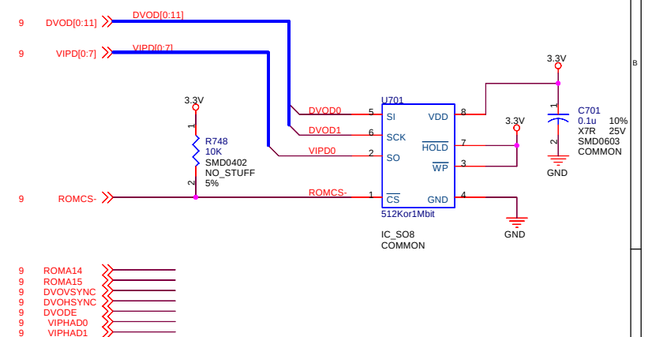
Thursday, February 14, 2002

Scale









7. BIOS, Strapping, Mech

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X

Size	CAGE Code	DWG NO	Rev
Custom			08

Thursday, February 14, 2002

Scale

Sheet 12 of 12