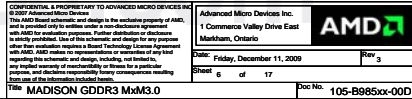
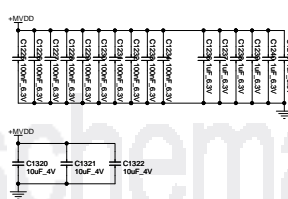
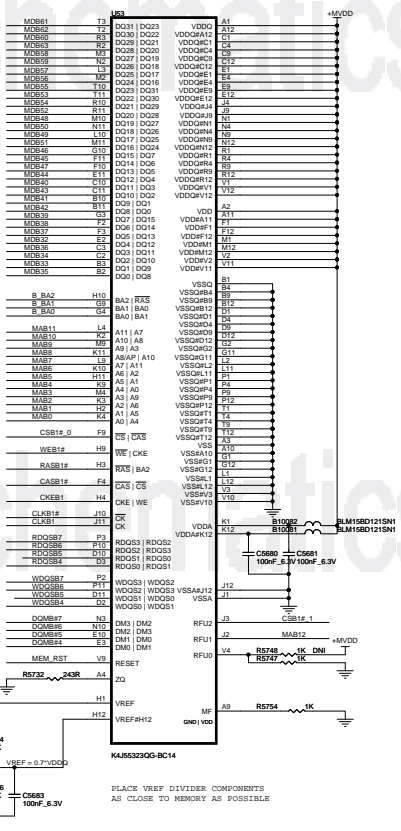
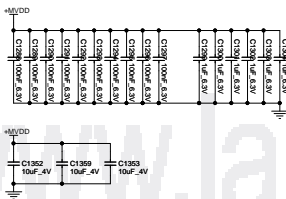
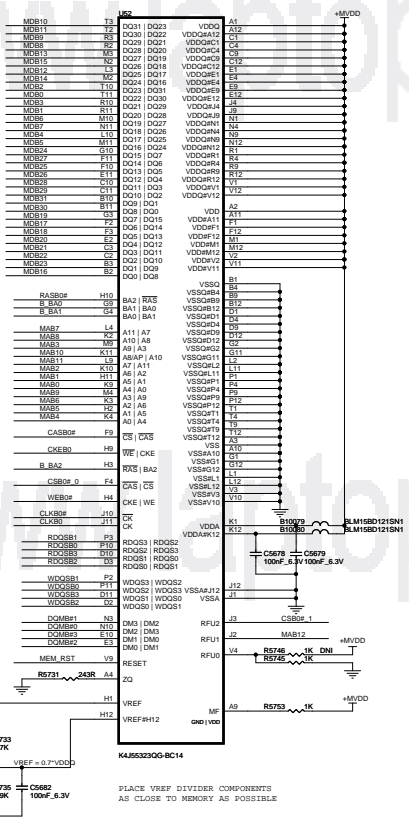


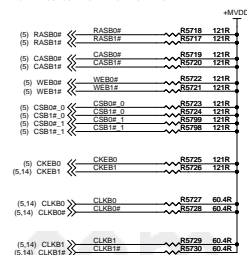
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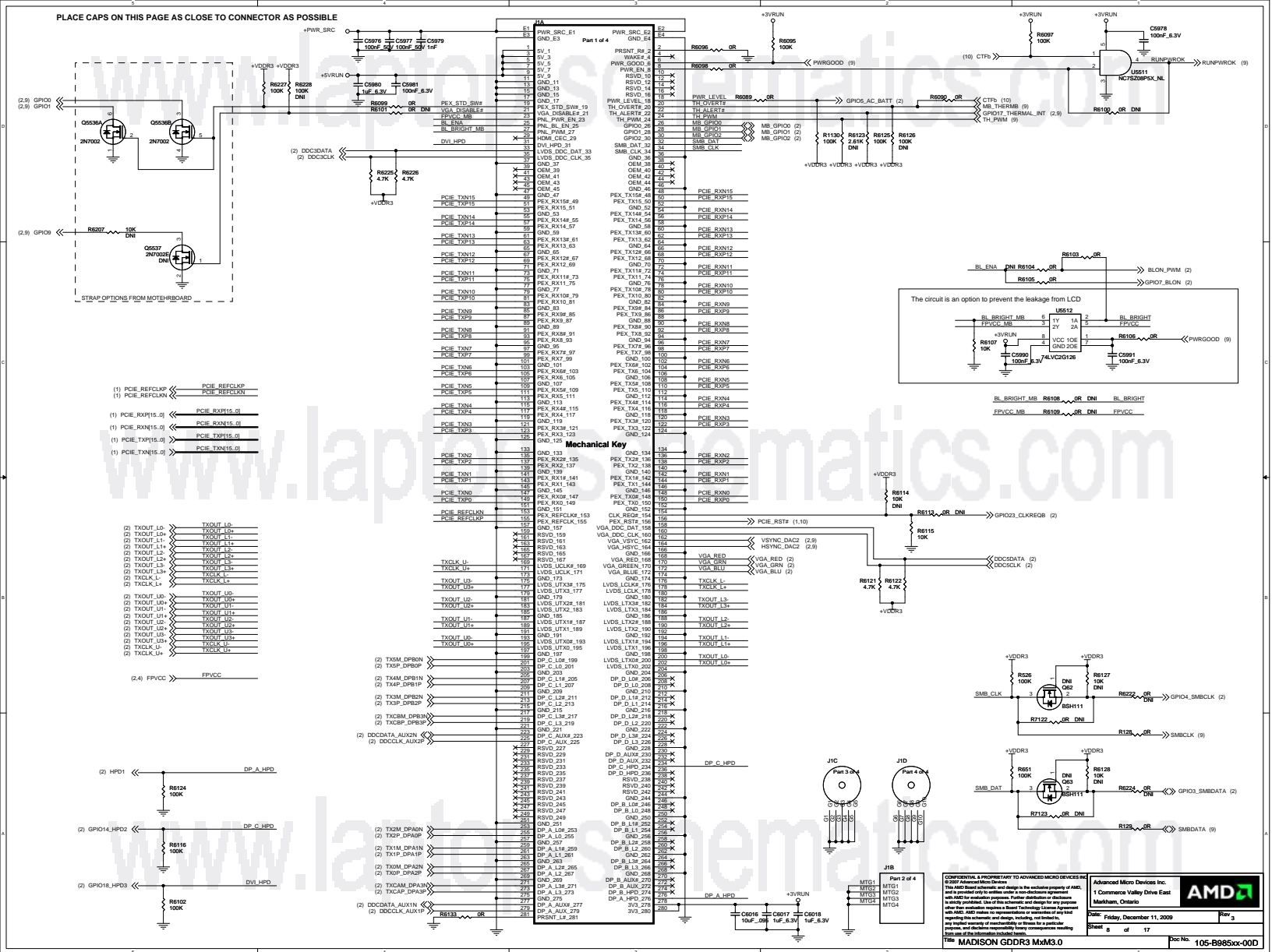
**GDDR3 32MX32 MEMORY**



QDDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES MAY CHANGE  
SEE LAYOUT GUIDE FOR LATEST INFORMATION



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Title <b>MADISON GDDR3 Mx3.0</b>		Date: Friday, December 11, 2009 Sheet 7 of 17	
Doc No:		Rev 3 106-B885xx-00D	





[illegible]

(2,8) GPIO0	GPIO0	R5134	10K
(2,8) GPIO1	GPIO1	R5135	10K
(2) GPIO2	GPIO2	R5136	10K
(2,8) GPIO9	GPIO9	R5138	10K DNI
(2) GPIO11	GPIO11	R5138	10K
(2) GPIO12	GPIO12	R5140	10K DNI
(2) GPIO13	GPIO13	R5141	10K
(2) GPIO22	GPIO22	R5147	10K
(2) HSYNC_DAC1	V11SYNC	R5142	10K
(2) HSYNC_DAC1	H11SYNC	R5143	10K
(2,8) HSYNC_DAC2	V21SYNC	R5146	10K
(2,8) HSYNC_DAC2	H21SYNC	R5146	10K DNI
(2,10) GPIO21_BB_EN	GPIO21_BBEN	R5146	10K
(2) GPIO28	GPIO28	R5137	10K

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	GPIOD	Transmitter Power Savings Enable 0: Slew Tx output enable 1: Full Tx output enable	1
TX_DEEMPH_EN	GPIOD1	PCIe Transmitter De-emphasis Enable 0: Tx de-empirsis disabled 1: Tx de-empirsis enabled	1
BIF_GEN2_EN_A	GPIQ2	PCIe Gen2 Enable 0: Advertises the PCIe device as 2.5GT/s capable at power-on 1: Advertises the PCIe device as 5.0GT/s capable at power-on	1
BIF_VGA_DIS	GPIQ9	VGA Control 0: VGA controller capacity disabled 1: VGA controller capacity enabled (for multi-GPU)	0
ROMIDCFG[2:0]	GPIQC[13:11]	Serial ROM type or Memory Aperture Size Selected If GPIQCD = 0, defines memory aperture size If GPIQCD = 1, defines ROM type 0: 16-bit Serial ROM (SR)      101: mbea: M2PROM (ST) 1: 16-bit Serial ROM (SR)      102: mbea: M2PROM (ST) 2: 16-bit Serial ROM (SR)      103: mbea: M2PROM (ST) 3: 16-bit Serial ROM (SR)      104: mbea: M2PROM (ST) 4: 16-bit Parallel ROM (DPRG) 105: mbea: M2PROM (ST) 5: 16-bit Parallel ROM (DPRG) 106: mbea: M2PROM (ST) 6: 16-bit Parallel ROM (DPRG) 107: mbea: M2PROM (ST) 7: 16-bit Parallel ROM (DPRG) 108: mbea: M2PROM (ST) 8: 16-bit Parallel ROM (DPRG) 109: mbea: M2PROM (ST) 9: 16-bit Parallel ROM (DPRG) 110: mbea: M2PROM (ST) 10: 16-bit Parallel ROM (DPRG) 111: mbea: M2PROM (ST) 11: 16-bit Parallel ROM (DPRG) 112: mbea: M2PROM (ST) 12: 16-bit Parallel ROM (DPRG) 113: mbea: M2PROM (ST) 13: 16-bit Parallel ROM (DPRG) 114: mbea: M2PROM (ST) 14: 16-bit Parallel ROM (DPRG) 115: mbea: M2PROM (ST) 15: 16-bit Parallel ROM (DPRG) 116: mbea: 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Figure 10: PWRVREG circuit diagram. The circuit shows a PWRVREG block connected to a +5V/SLN input and a +1.5V\_REG output. The PWRVREG block includes a feedback network with resistors R585 (1R, 1210), R586 (1R, 1210), and R587 (0.50R). The output is connected to a load network with resistors R1 (2.67K), R2 (10.2K), and capacitors C855 (30uF, 50V), C852 (10uF), and C851 (10uF). The circuit is powered by a +1.5V\_REG supply.

Overlap footprints  
Use = 0.5R  
1/2W <=5%

(B) PWRVREG

CS56  
10uF\_X85

CS54  
1uF\_8.3V

U861  
PWRVREG

CS55  
30uF\_50V

CS52  
10uF

CS51  
10uF

R585  
1R, 1210

R586  
1R, 1210

R587  
0.50R

R1  
2.67K

R2  
10.2K

R588  
1R, 1210

R589  
1R, 1210

R590  
0.50R

R591  
0.50R

R592  
0.50R

R593  
0.50R

R594  
0.50R

R595  
0.50R

R596  
0.50R

R597  
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R598  
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R599  
0.50R

R600  
0.50R

R601  
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R602  
0.50R

R603  
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R604  
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R605  
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R608  
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R613  
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R615  
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R616  
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R617  
0.50R

R618  
0.50R

R619  
0.50R

R620  
0.50R

R621  
0.50R

R622  
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R623  
0.50R

R624  
0.50R

R625  
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R626  
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R627  
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R628  
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R629  
0.50R

R630  
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R631  
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R632  
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R731  
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R736  
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R737  
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R738  
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R739  
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R740  
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R741  
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R754  
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R798  
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R799  
0.50R

R800  
0.50R

R801  
0.50R

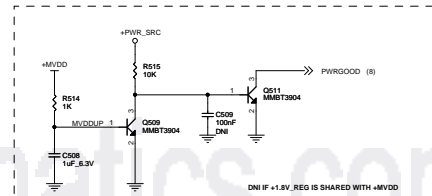
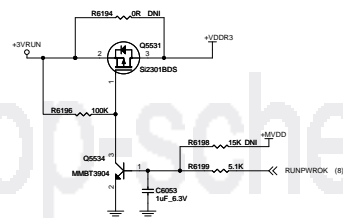
R802  
0.50R

R803  
0.50R

R804  
0.50R

R805  
0.50R

R806  
0.50R

[illegible]

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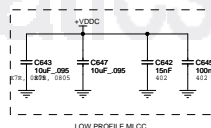
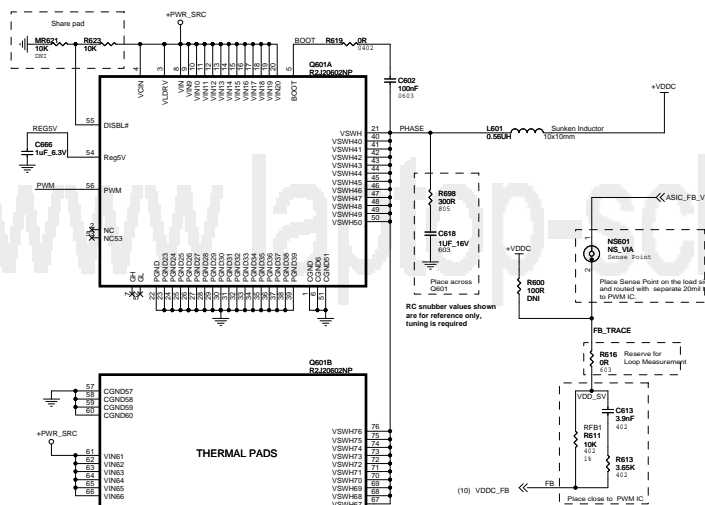
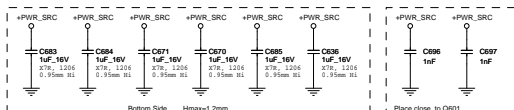
**AMD**

Date: Friday, December 11, 2009 Rev 3  
Sheet 9 of 17

Title: **MADISON GDDR3 MxM3.0** Doc No: 105-B985x-00D



Figure 1: Schematic diagram of the power plane layout. It shows four identical power source symbols connected to a common ground. Each symbol consists of a capacitor labeled C657, C669, C638, and C665 respectively, with a value of 2.2uF, 16V, and a 1.3mm HI dimension. The symbols are connected to a PWR\_SRC net. The layout is labeled 'Top Side' and 'Hmax=1.5mm'.



COMP

C611  
6.8uF .25V  
402

R612  
8.06K  
402

C612  
150PF  
402

R614  
0R

FB

R609  
0R

Place close to U601

REGSV

share piad

R607 2.2R

+5VRLIN

Q

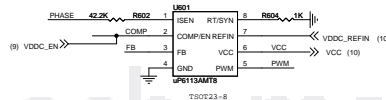
MR607 2.2R

VCC

603  
x7R  
5k

C607  
100nF

Place close to U601



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Title: **MADISON\_GDDR3\_M2\_M3\_2**

Advanced Micro Devices Inc.  
1 Commerce Valley Drive East  
Markham, Ontario

Date: Friday, December 11, 2015  
Sheet: 1 of 1

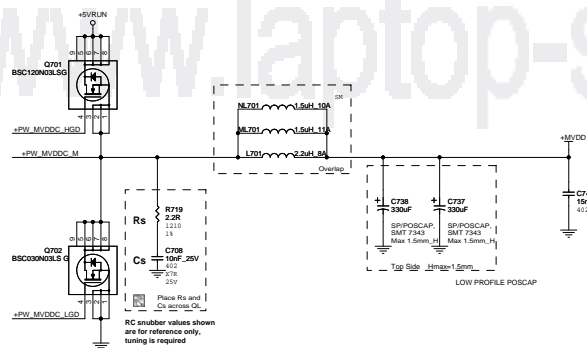
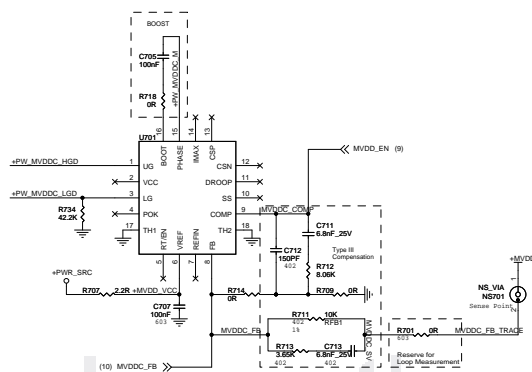
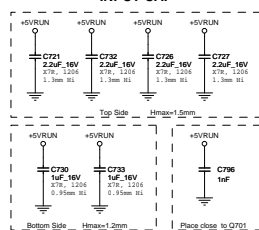
11 of 17

Doc No. 105 B08Eym 00

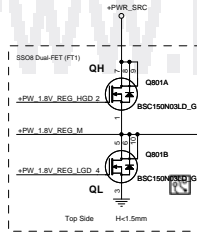
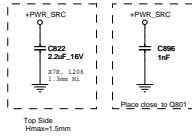
Title **MADISON GDDR3 MxM3 C**

Doc No. 105 B08Eym 00

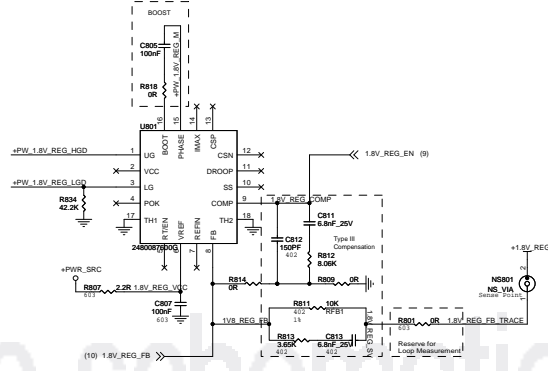
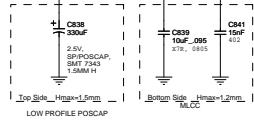
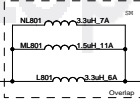
## INPUT CAP



INPUT CAP

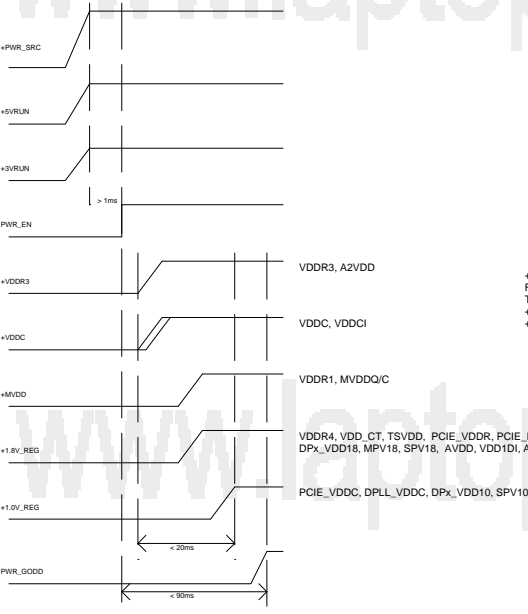


Place R324 and C822 as close as possible to the MOSFET. TC stubs shown are for reference only, tuning is required.

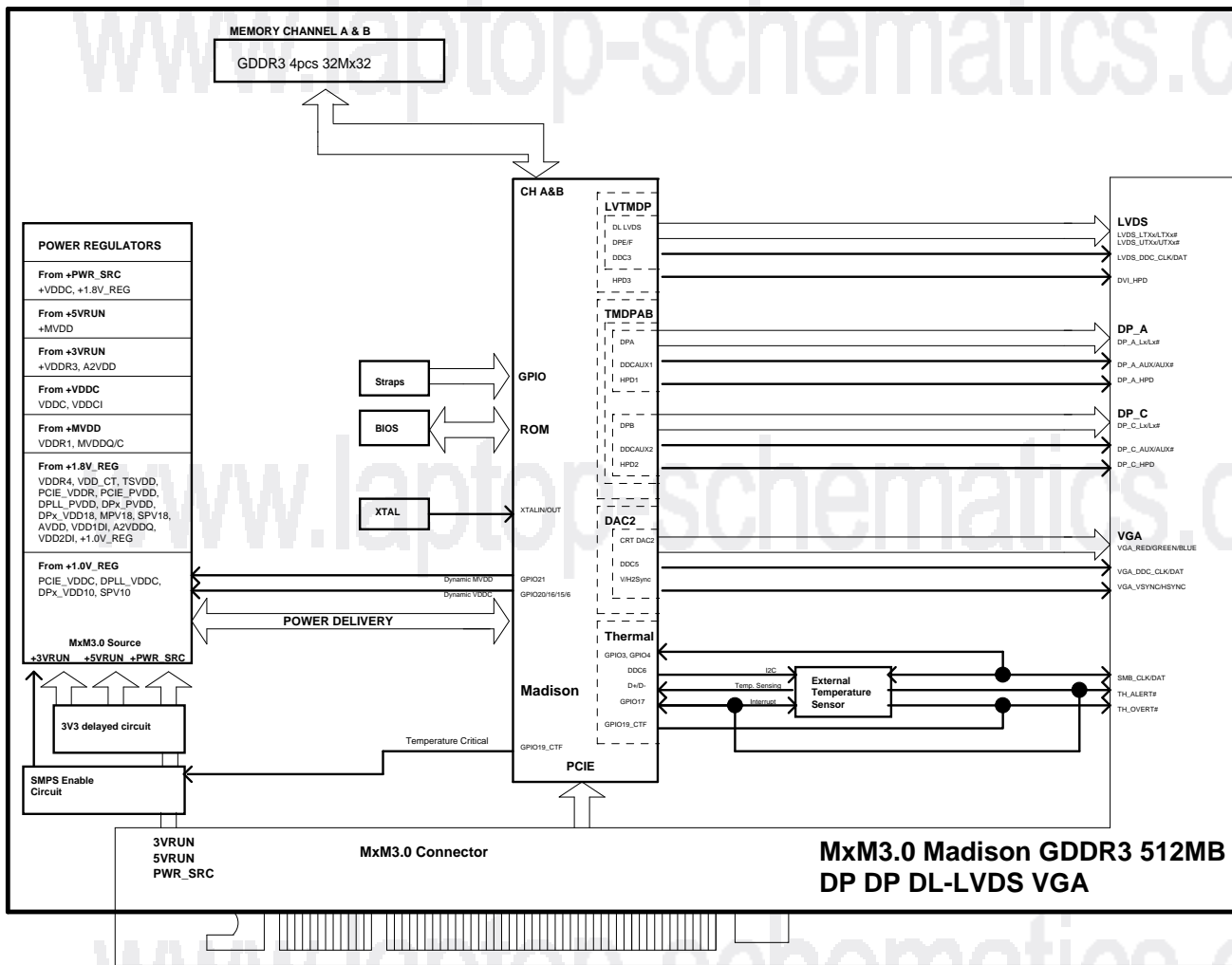




POWER UP SEQUENCE (not to scale)



+VDDR3 should ramp before or simultaneously with +VDDC.  
For LVDS, DPx\_VDD10 should ramp-up before DPx\_VDD18 and PCIe Reference clock should begin before DPx\_VDD18.  
The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both +VDDC and +1.8V\_REG have ramped up.  
+VDDC and +1.8V\_REG should not ramp-up simultaneously.  
+VDDC should ramp before +1.8V\_REG and +1.0V\_REG.





<div>AMD</div>			Title		Schematic No.		Date:	
			MADISON GDDR3 MxM3.0		105-B985xx-00D		Friday, December 11, 2009	
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.					Rev 3
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION					
0	00A	09/06/02	Initial design for Madison GDDR3 MxM3.0 based on M96 B803					
1	00B	09/08/27	Add U27, Q27, C27 - Gating circuit to delay DPEF_VDD18 Add R1677, R1678, R1679, R1680 - Pull downs for VID circuit Add R600 for debug Increase TP coverage					
2	00C	09/10/30	Add C696, C697, C796, C896 (0402 input caps for power supplies) Add R1001 (DRAM_RST topology change) Change J1 symbol (includes non-plated tooling holes) Move JTAG TPs out of the back plate area					
3	00D	09/12/11	Pull back power planes					
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