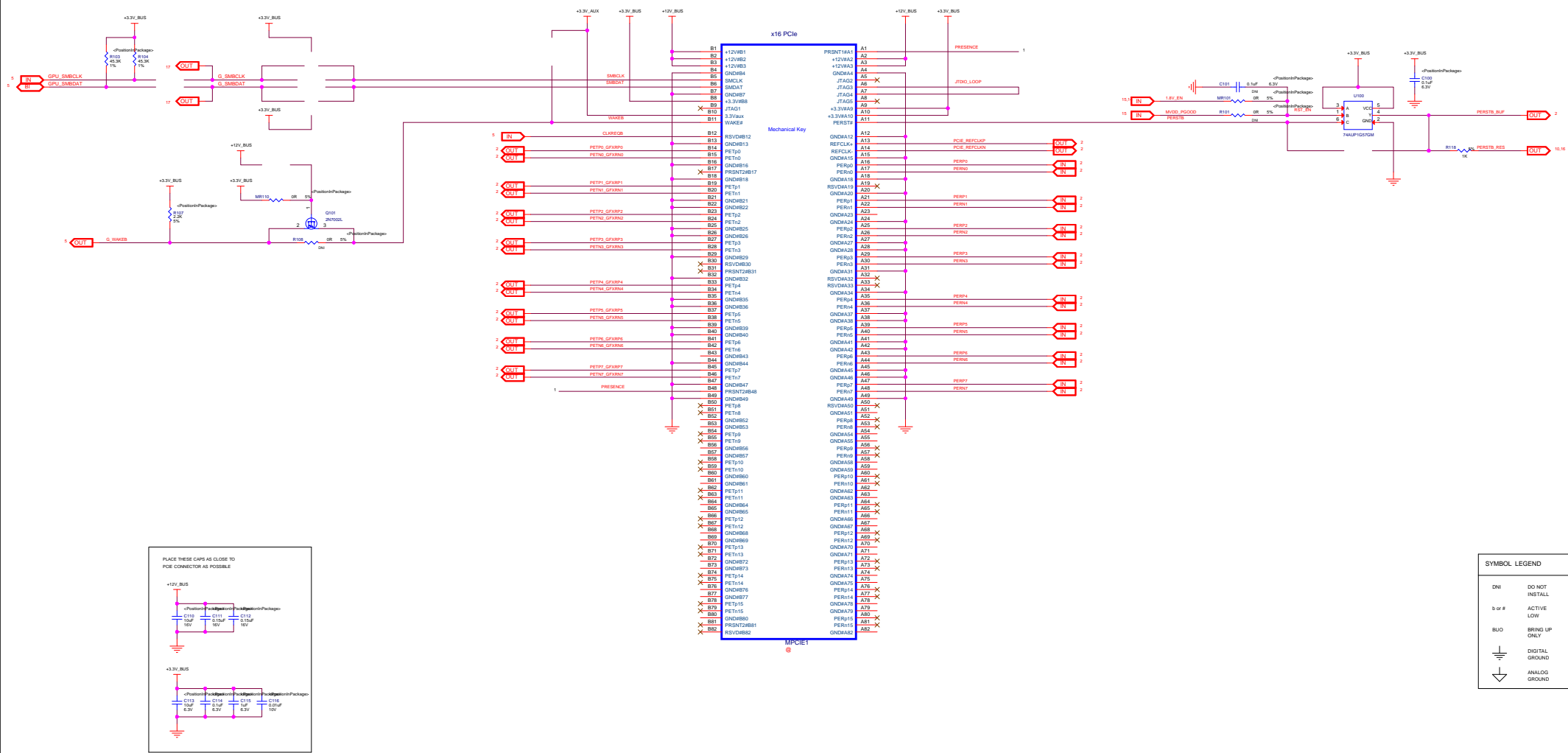
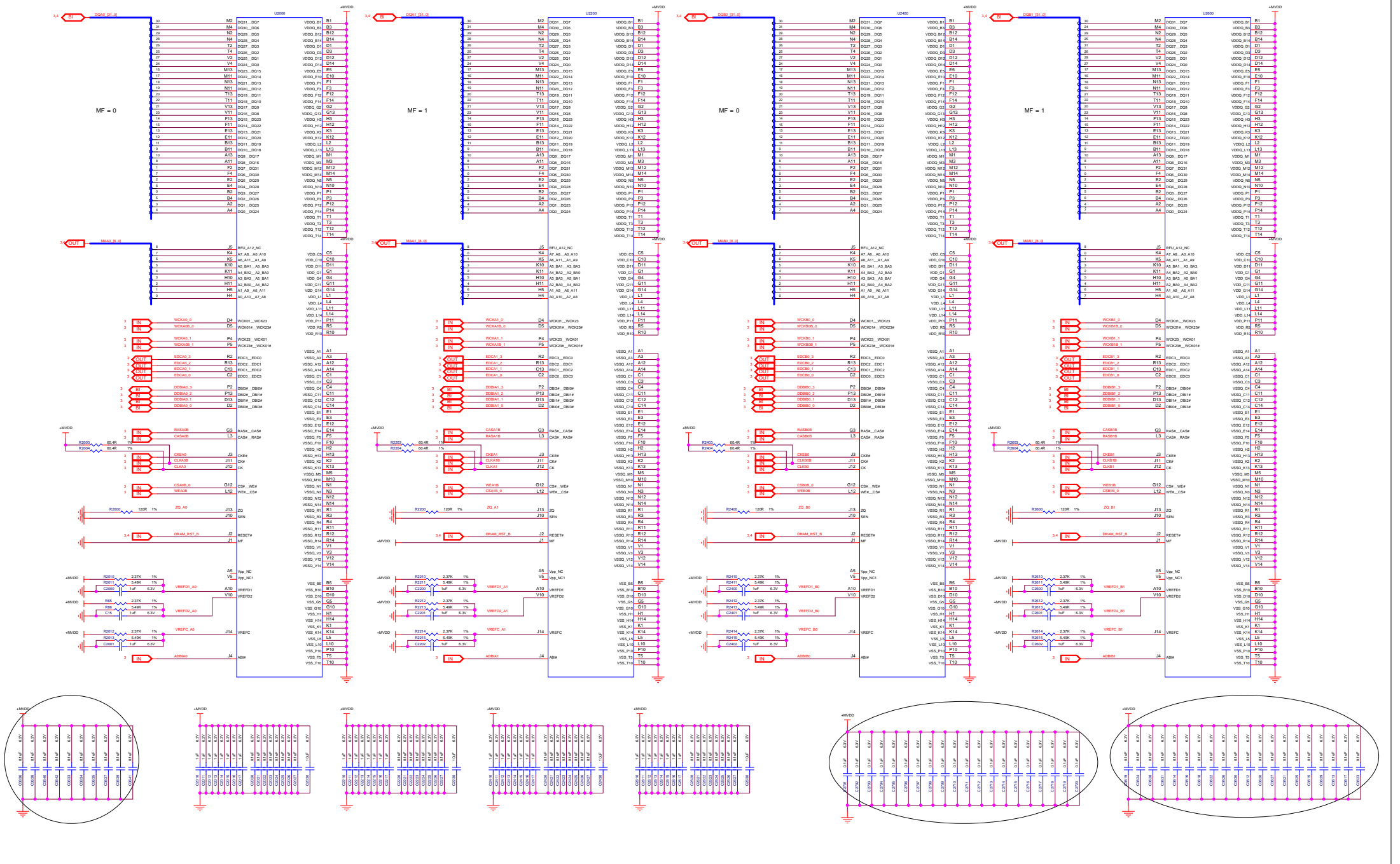


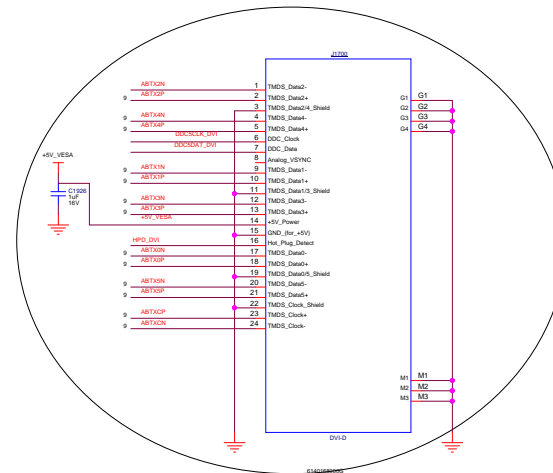
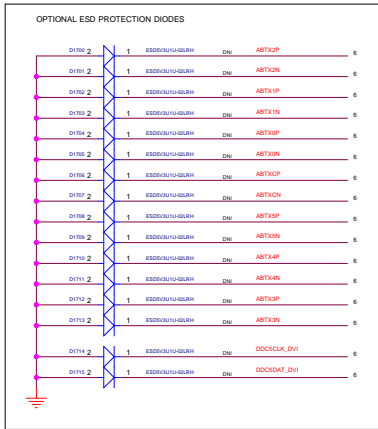
(1) PCIe EDGE CONNECTOR



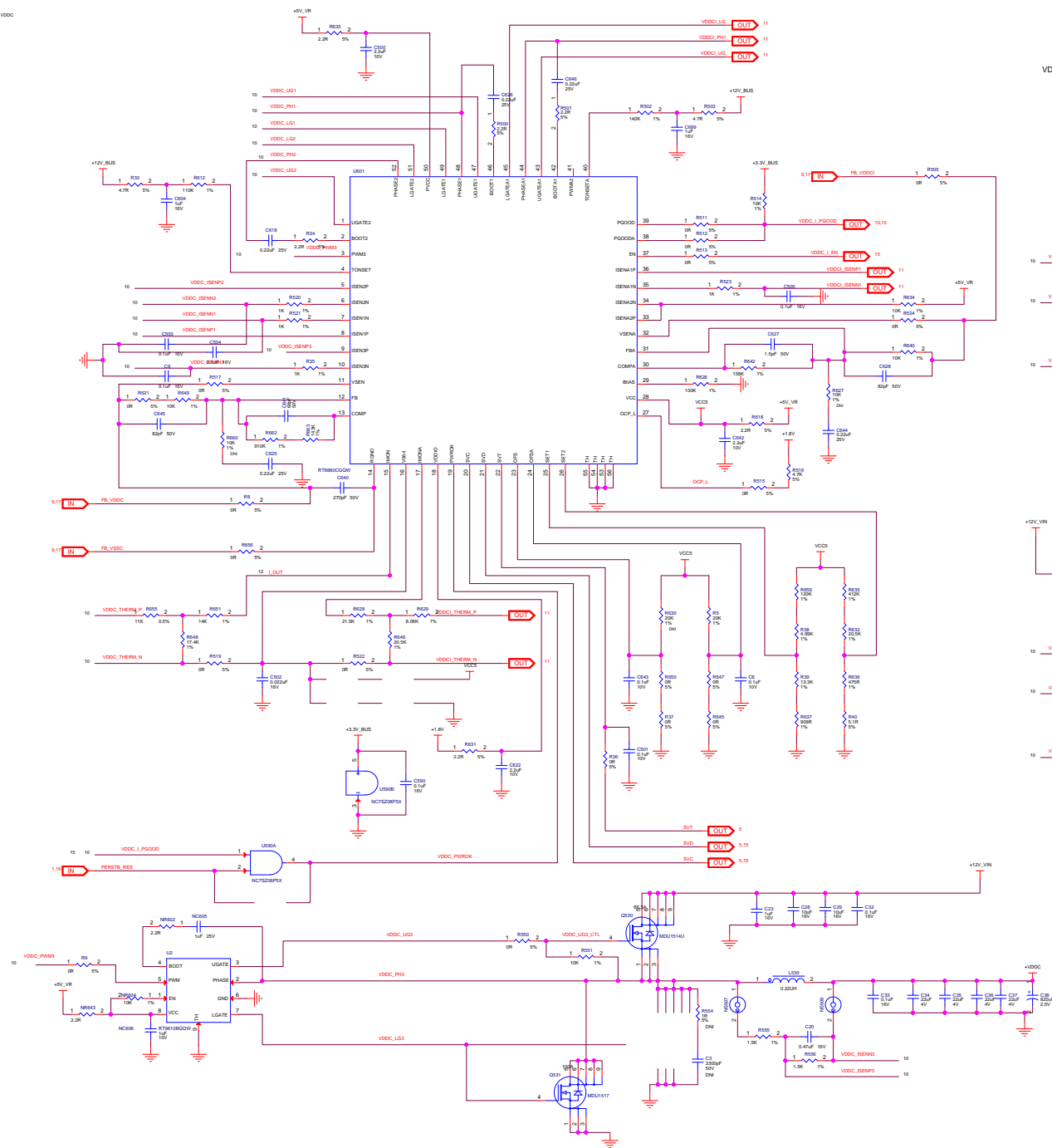
(4) GDDR5 CHAB x32



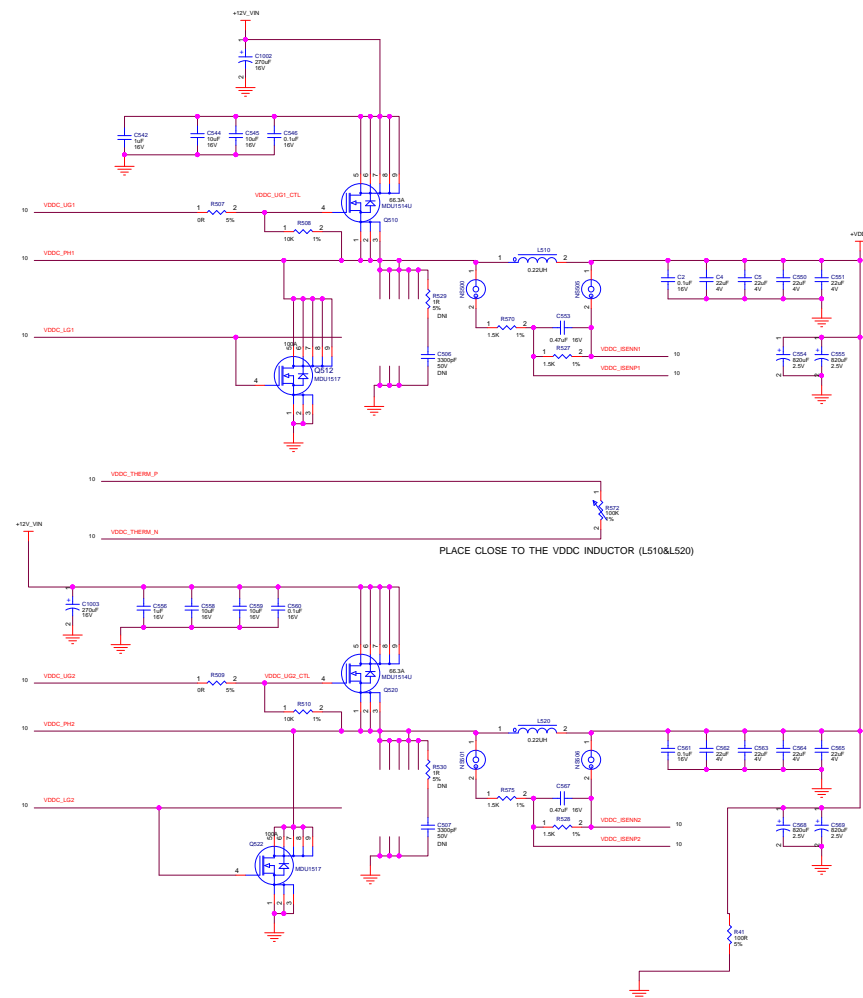
(6) BAFFIN TMDPAB - dDVI



(7) BAFFIN TMDPCD - HDMI DP

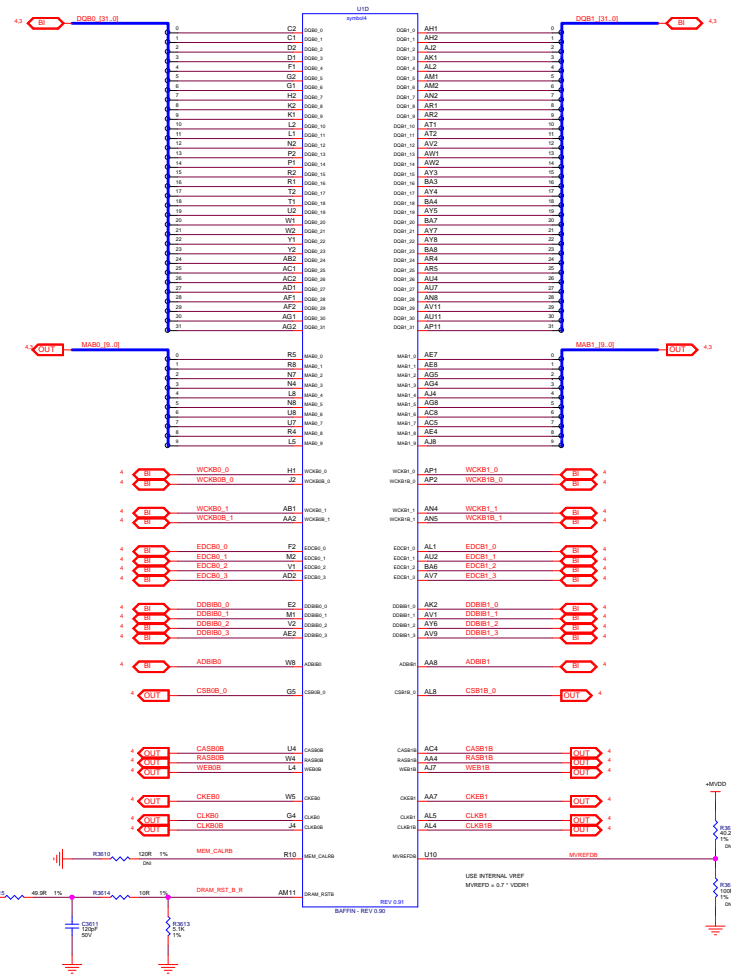
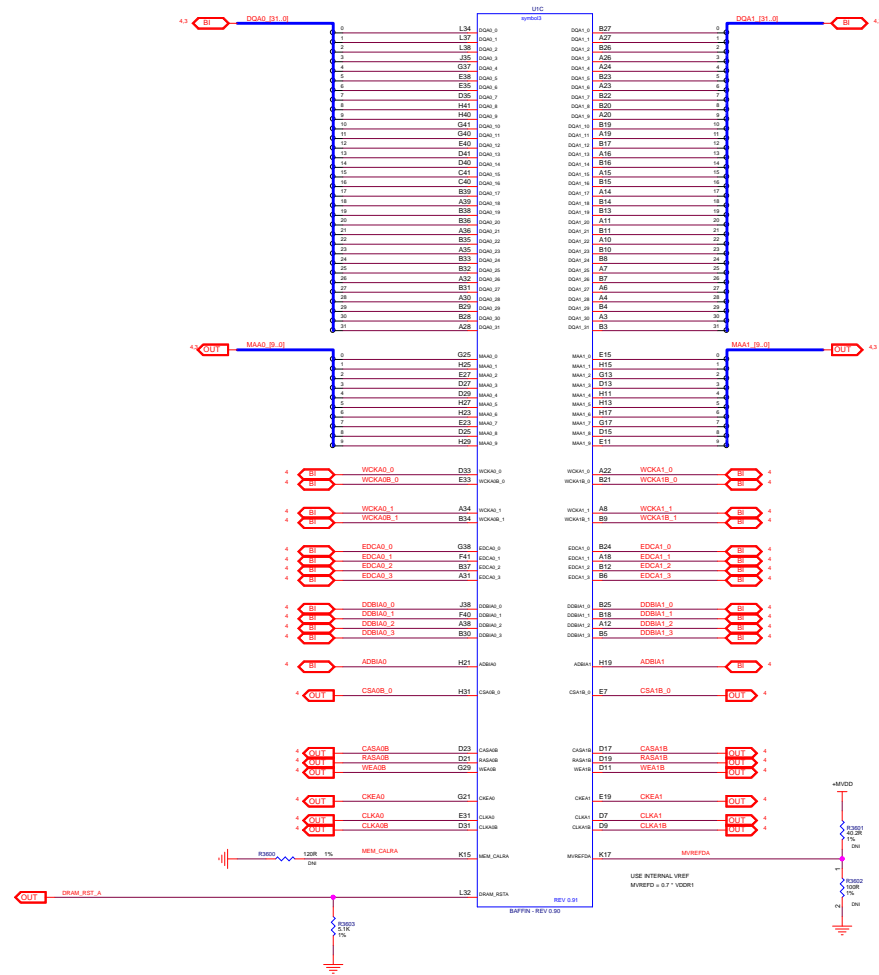


VDDC INPUT



PLACE CLOSE TO THE VDDC INDUCTOR (L510&L520)

(3) RACERX MEMORY INTERFACE



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SHEET: BAFFIN MEMORY

DATE: Wed Jun 01 06:00:28 2016

REV: 1.0

SHEET NUMBER: 3 OF 11

TITLE:	TITLE
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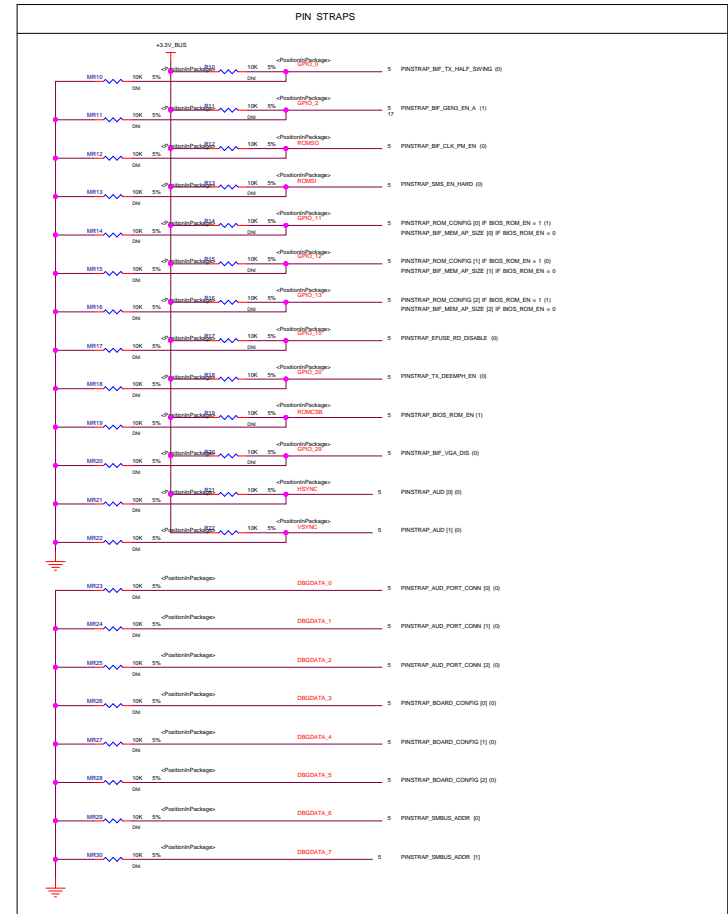
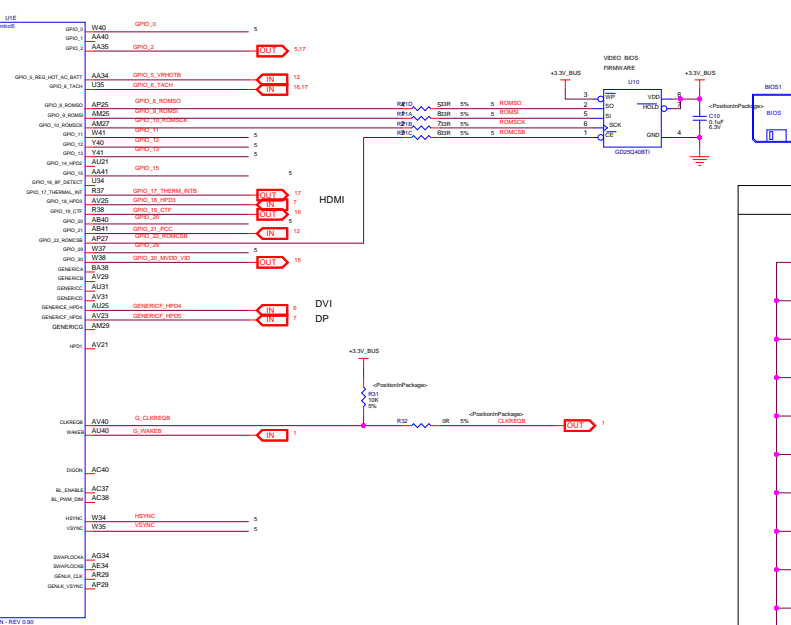
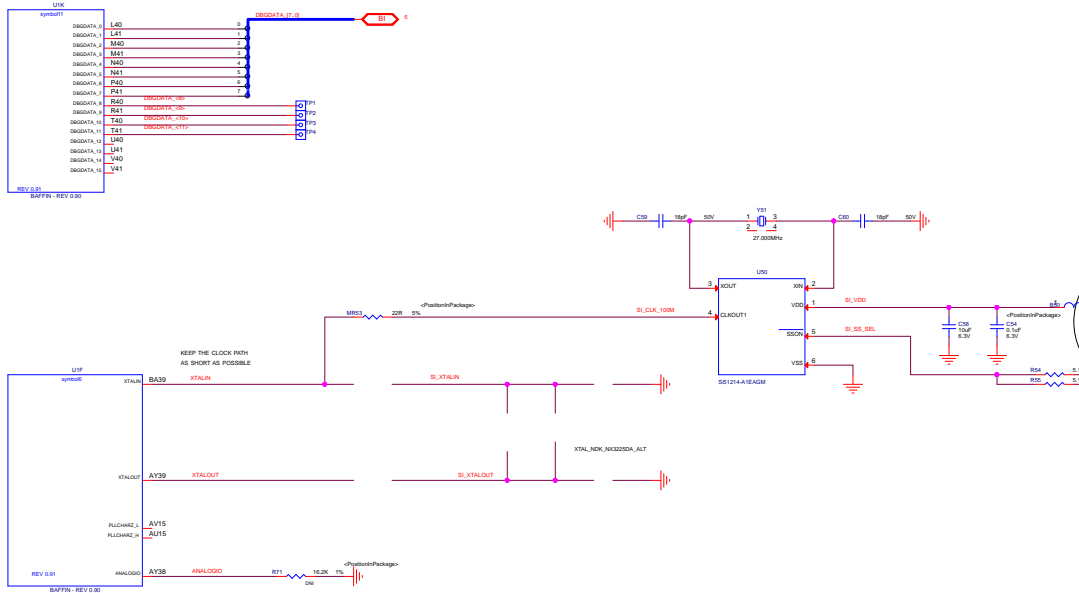
3

1

(5) BAFFIN GPIO STRAPS CLK

DEVICE	ADDRESS
AD5274	0x5C
RT9433	0x52
VTMM II	

DEVICE	ADDRESS
LM9003	0x98



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SHEET: BAFFIN GPIO STRAPS CLK

DATE: Wed Jun 01 06:00:29 2016

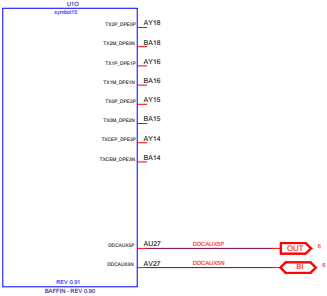
REV: 1.0


SHEET NUMBER: 5 OF 11

TITLE:	TITLE
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TITLE

(8) BAFFIN TMDPE

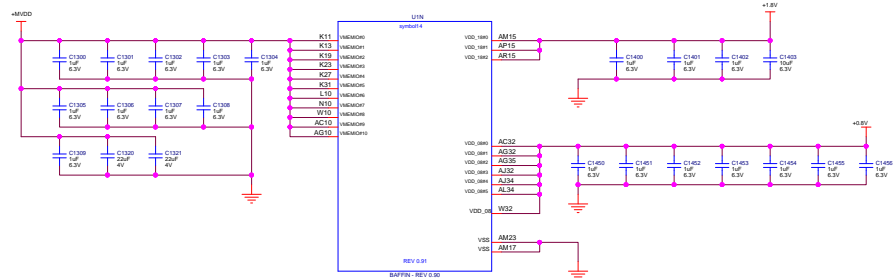
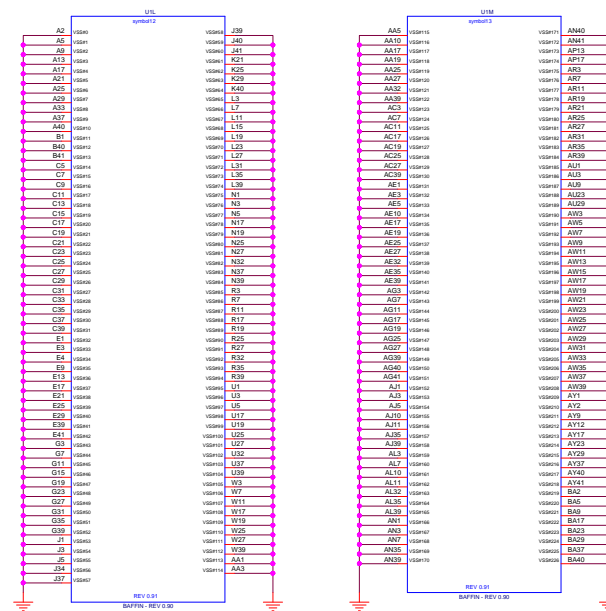
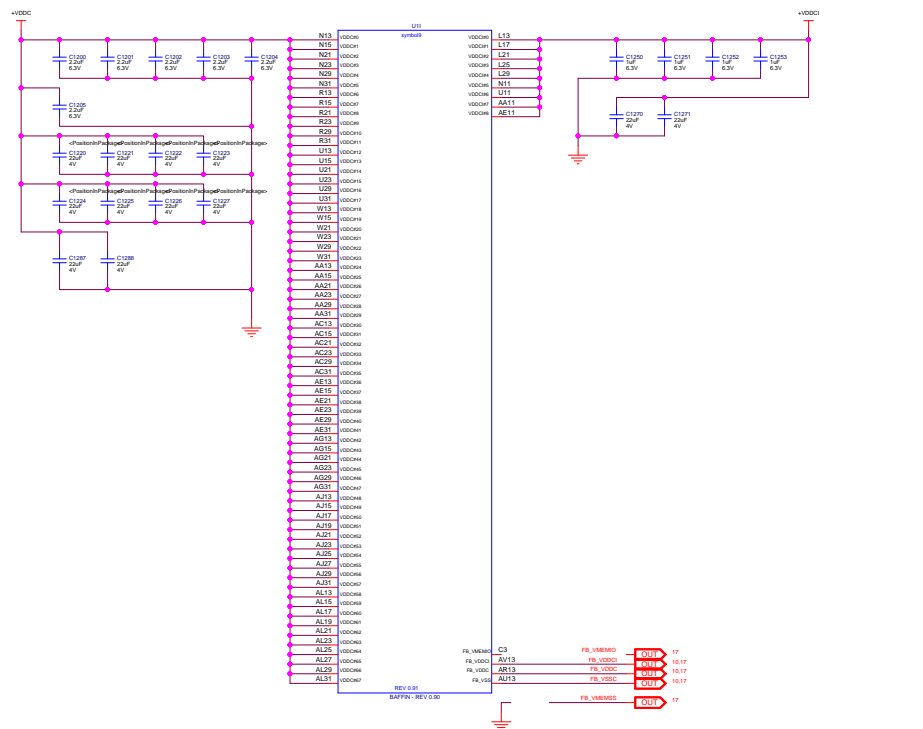


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SHEET: BAFFIN TMDPE - NC		
DATE: Wed Jun 01 08:00:29 2016	REV: 1.0	
SHEET NUMBER: 8 OF 19		
DOCUMENT NUMBER: 105_CXXX00_00A		

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TITLE

(9) BAFFIN POWER GND



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SHEET: BAFFIN POWER GND

DATE: Wed Jun 01 06:00:30 2016

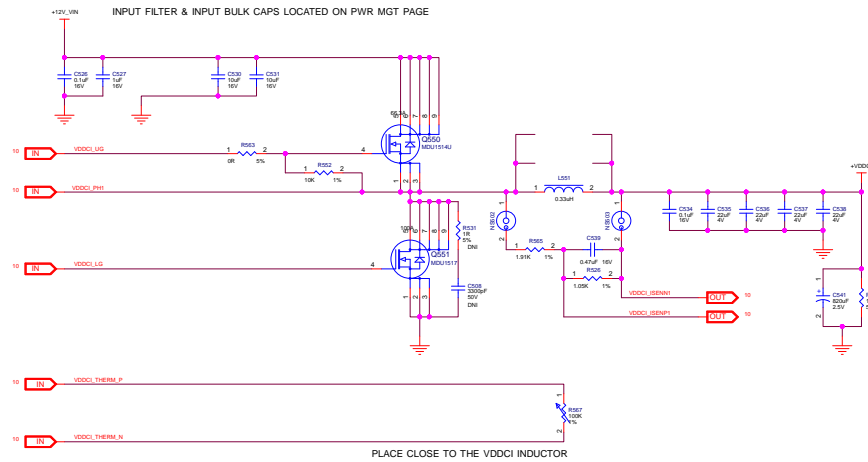
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SHEET NUMBER: 9 OF 19

TITLE: _____

DOCUMENT NUMBER: 105_CXXX00_00A

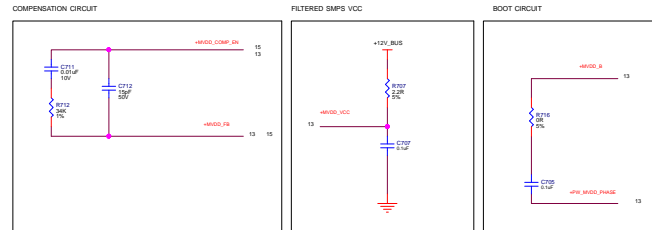
(11) VDDCI



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SHEET: VDDCI	
DATE: Wed Jun 01 08:00:30 2016	REV: 1.0
SHEET NUMBER: 11 OF 19	
DOCUMENT NUMBER: 106_CXXX00_00A	

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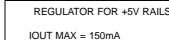
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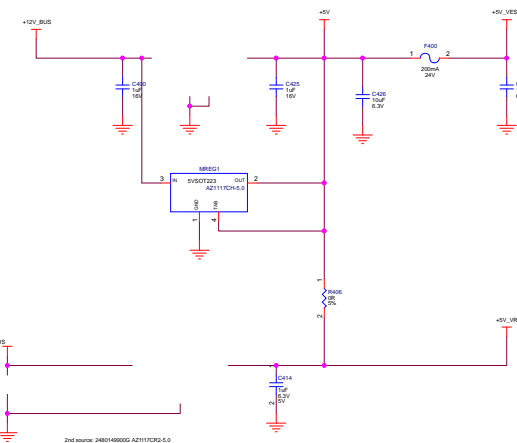
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TITLE:	TITLE
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(19) 0.8V

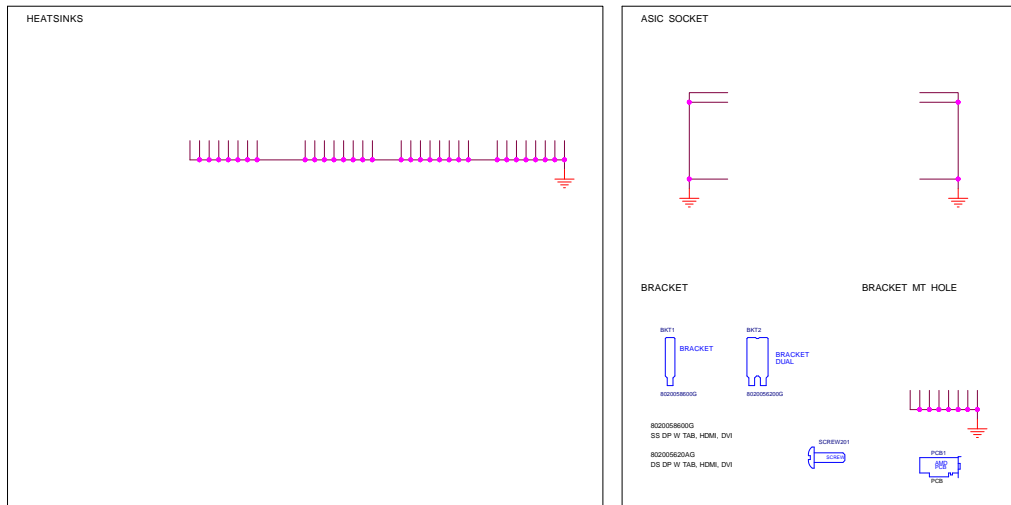
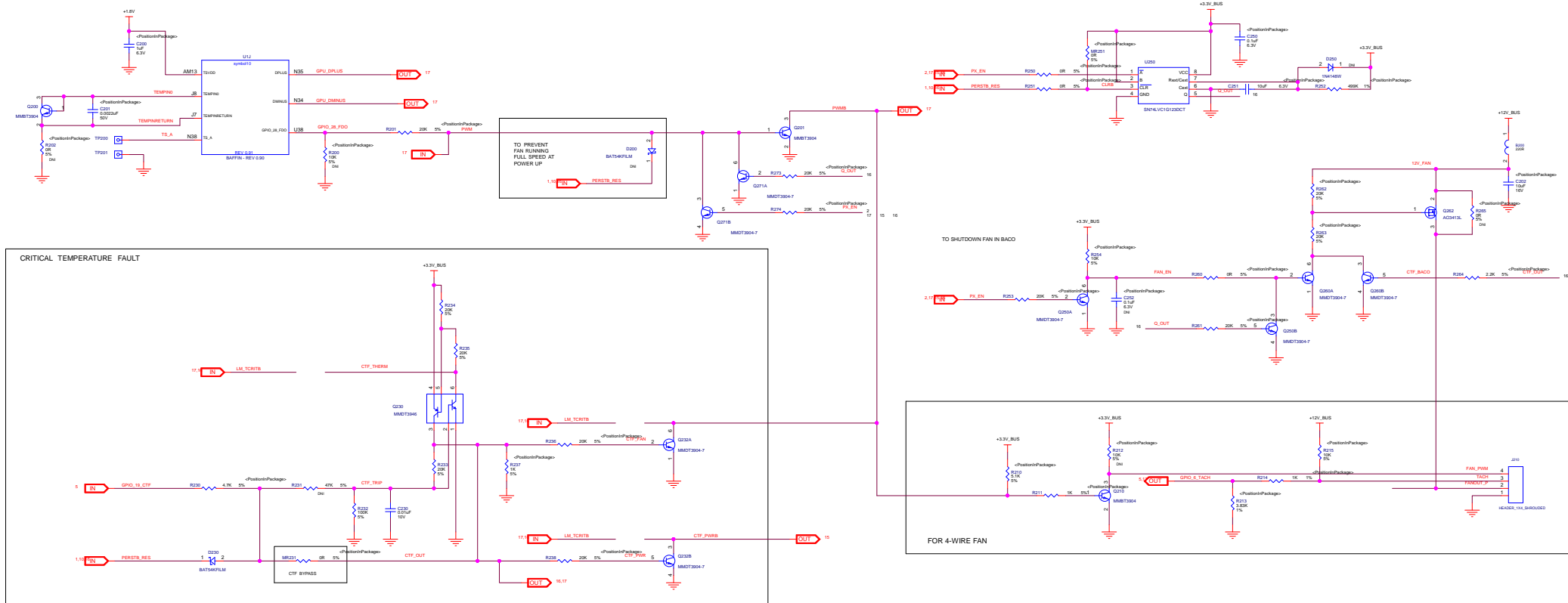



LDO #1: VIN = 3.0V TO 3.6V MAX VOUT = +1.8V +/- 2% IOUT = 1.3A RMS MAX
PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING

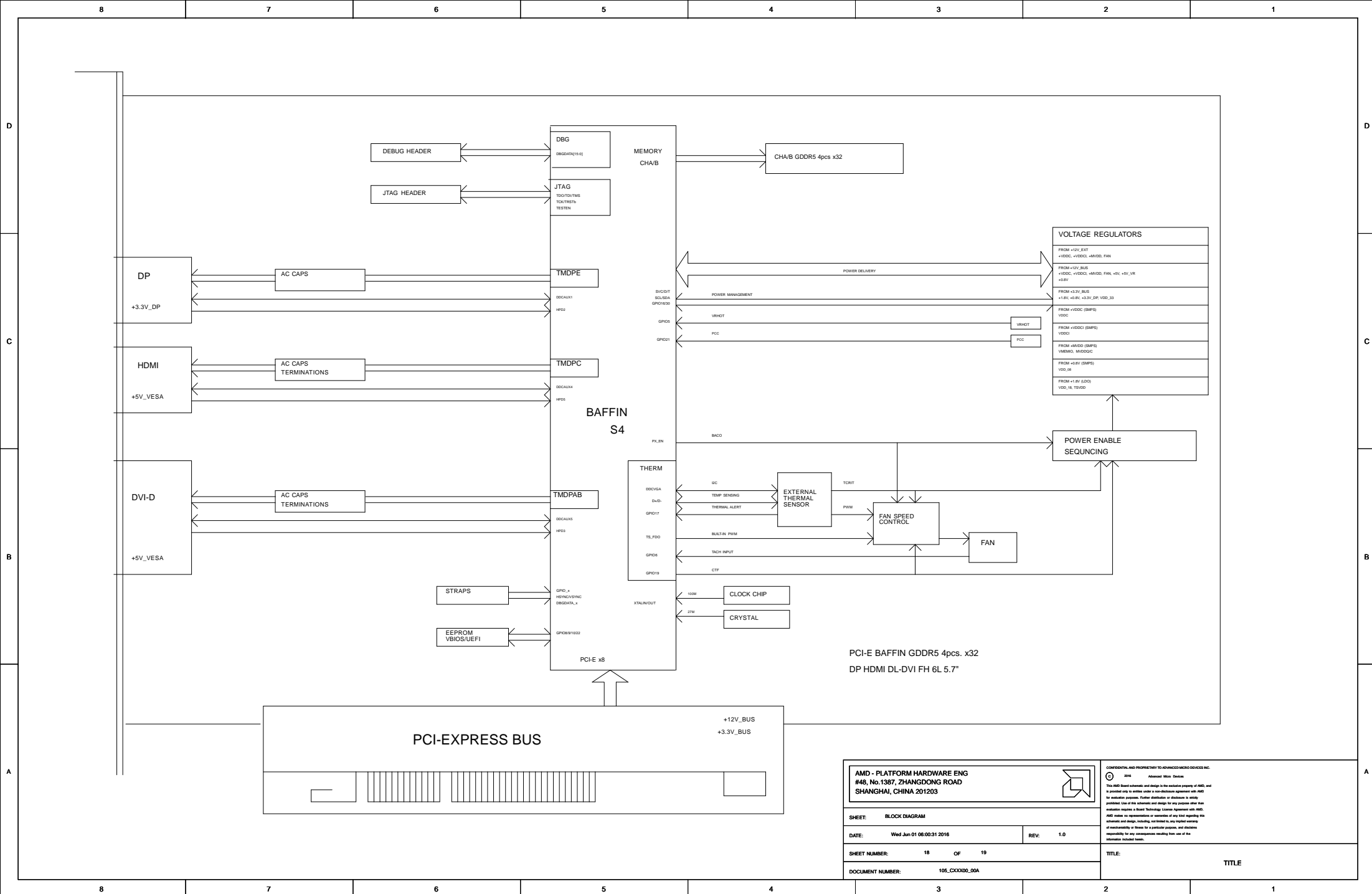


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SHEET: 0.8V REG					
DATE: Wed Jun 01 06:00:30 2016		REV: 1.0			
SHEET NUMBER: 14 OF 19				TITLE:	
DOCUMENT NUMBER: 105_C00000_00A				TITLE	
NOTES: NOTE					

(17) THERMAL MANAGEMENT



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SHEET:	THERMAL MANAGEMENT		REV:	1.0
DATE:	Wed Jun 01 06:00:31 2016			
SHEET NUMBER:	16	OF	19	TITLE:
DOCUMENT NUMBER:	106_CXX000_00A			TITLE



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AMD 		TITLE:				DOCUMENT NUMBER: 106_C00000_00A				DATE: Wed Jun 01 06:00:31 2016				SHEET NUMBER: 19 OF 19		REV: 1.0	
REVISION HISTORY						ENGINEER: XXXX		NOTES: NOTE		<div>CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding this schematic and design, including, not limited to, any explicit warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.</div> <div>C 2016 Advanced Micro Devices</div> <div>AMD - PLATFORM HARDWARE ENG #48, No.1367, ZHANGDONG ROAD SHANGHAI, CHINA 201203</div>							
SCH Rev		PCB Rev		Date		REVISION DESCRIPTION											
0		00A		1610202015		INITIAL RELEASE											
1		00B		1622202015		AMD 1.0V1.0202015 CLK 0200 AMD 100MHz CLOCK speed Change 0.02 power good pin up											

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