

PG410 A01

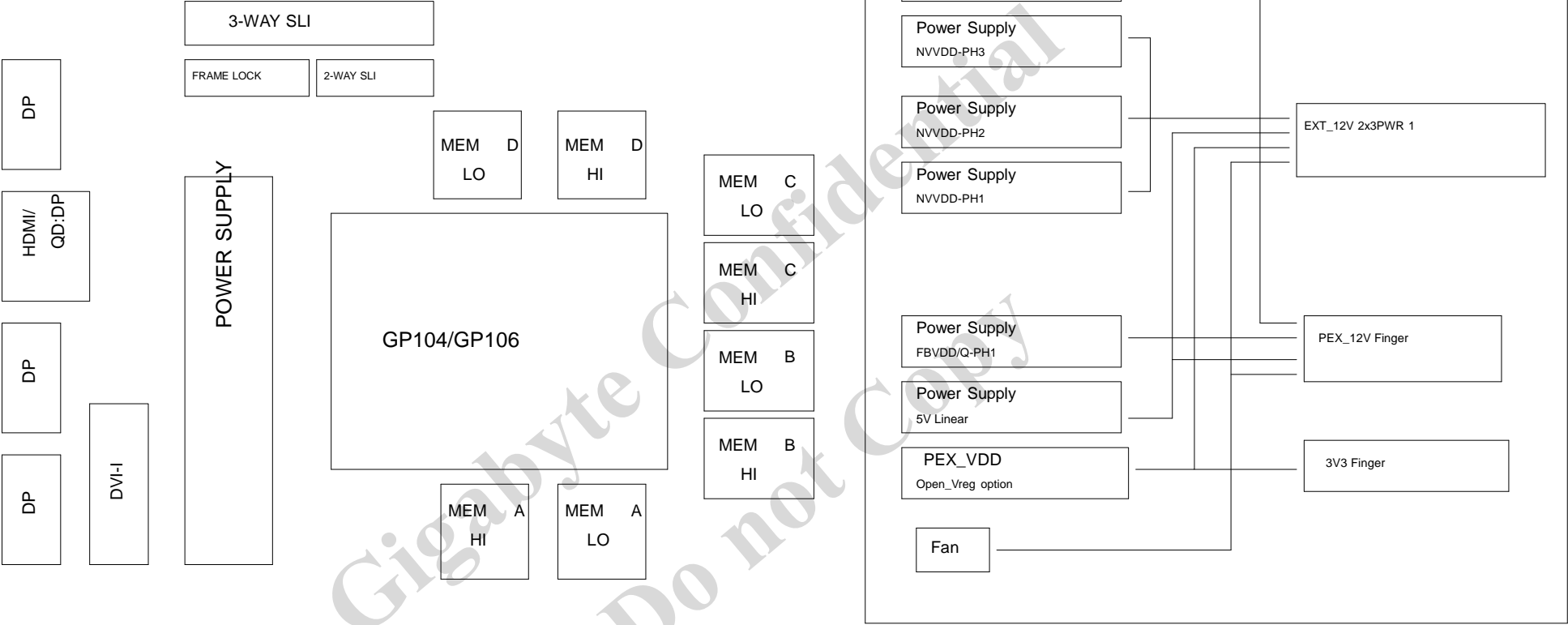
GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32  
Tall DVI-D + DP + DP + HDMI/DP + DP

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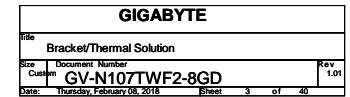
GIGABYTE			
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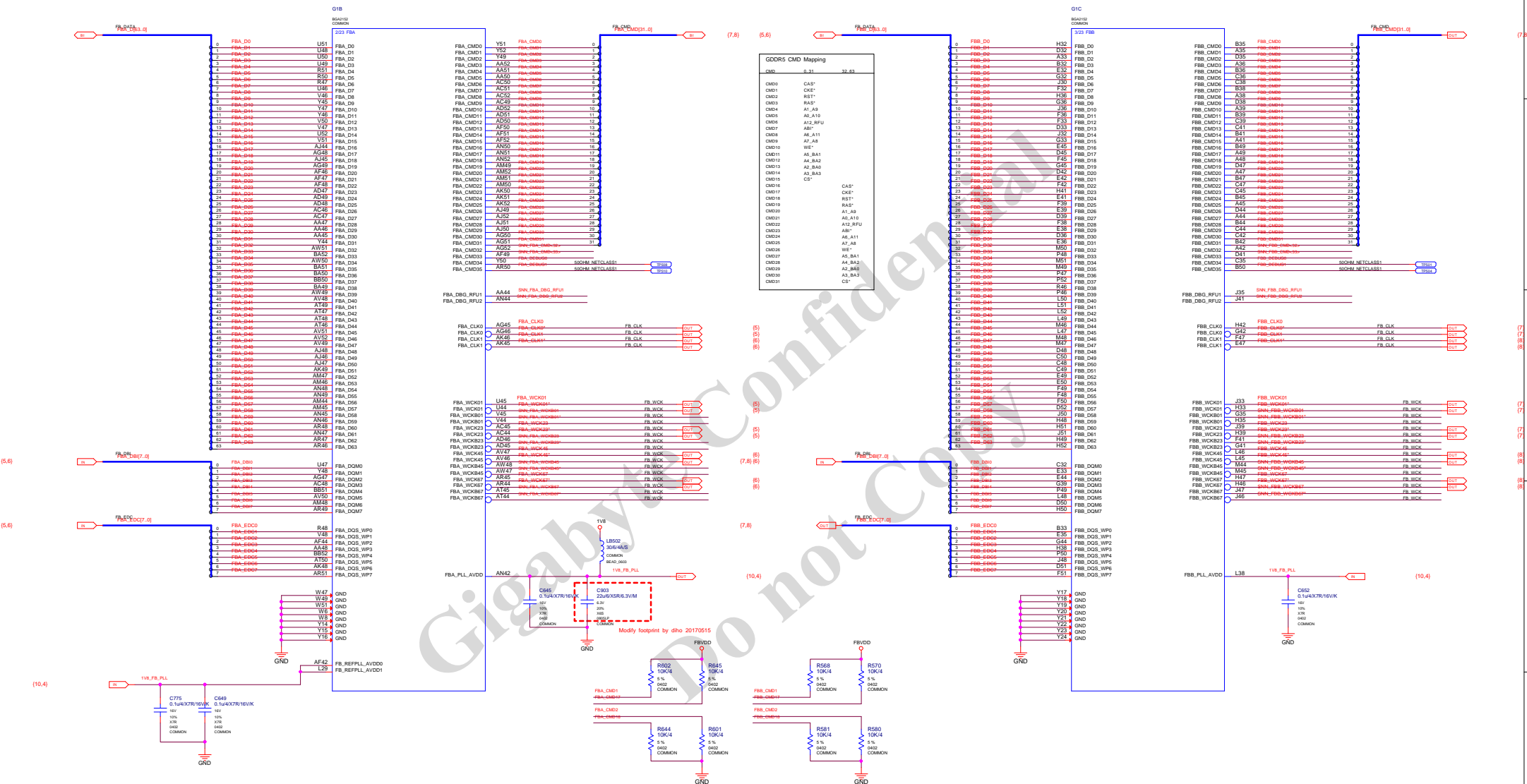


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ASSEMBLY PAGE: DETAIL  
-<ASSEMBLY\_DESCRIPTION> Block Diagram

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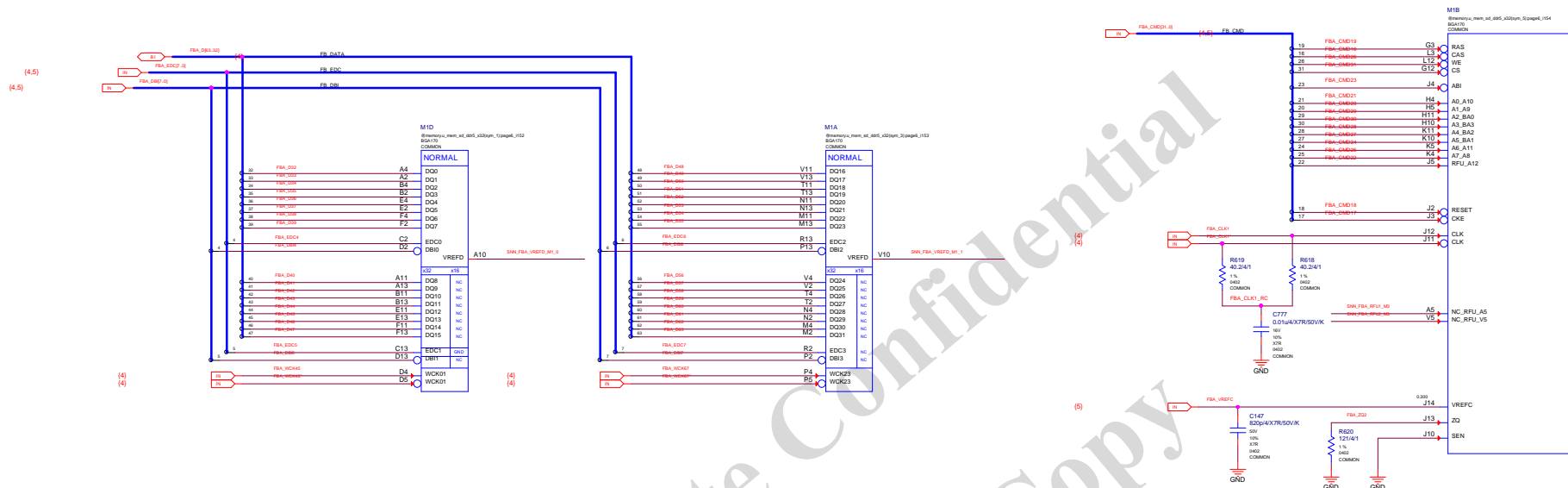
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ASSEMBLY  
PAGE DETAIL

ASSEMBLY DESCRIPTION:  
GPU FB\_AB

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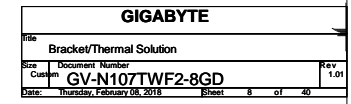
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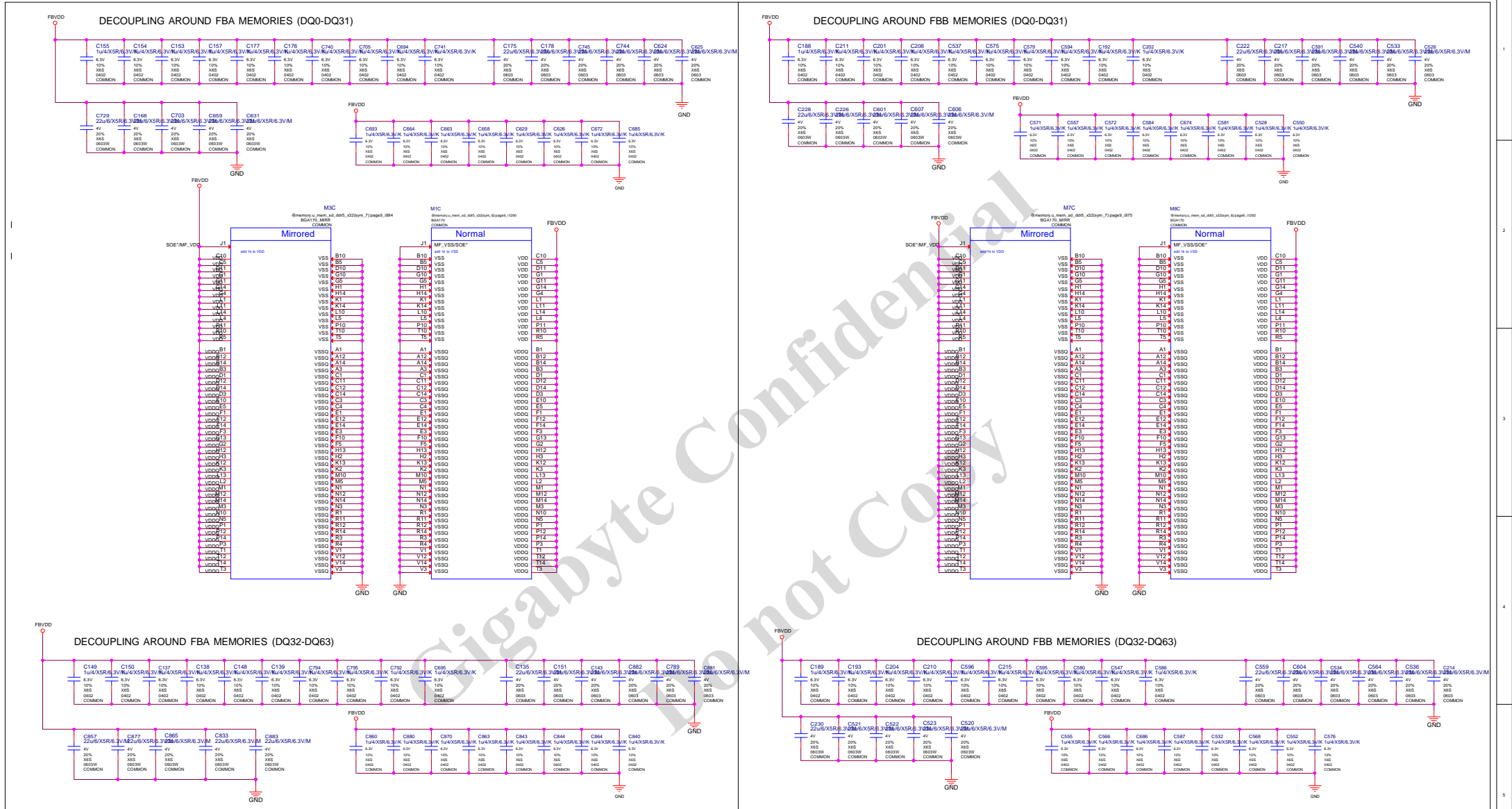
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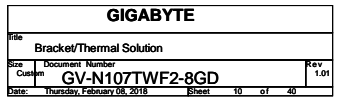
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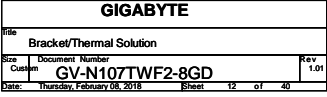
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MEM FB AB PWR

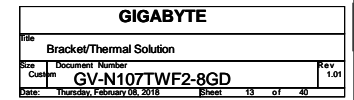
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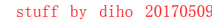
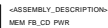








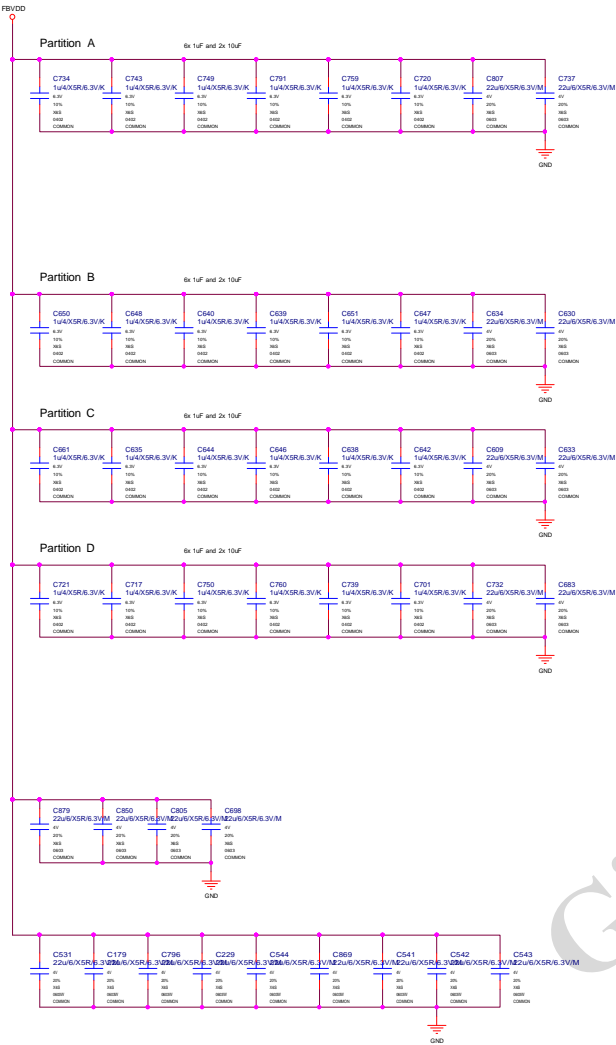




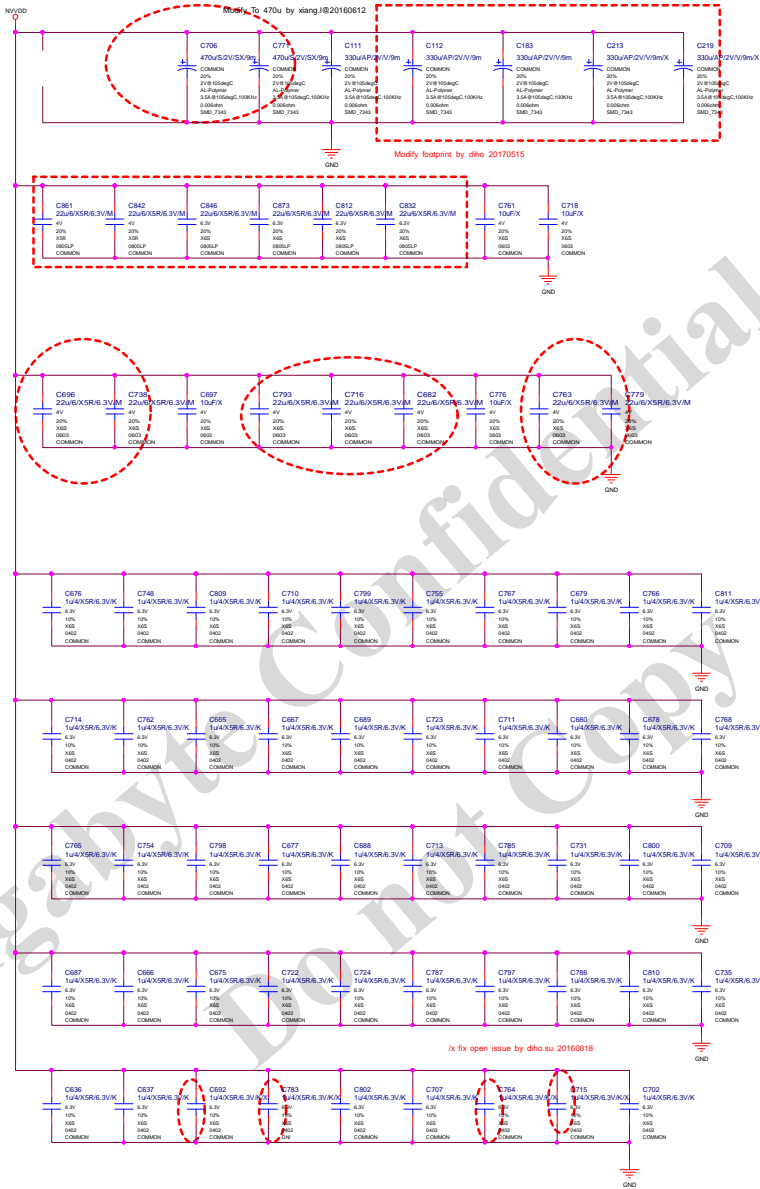




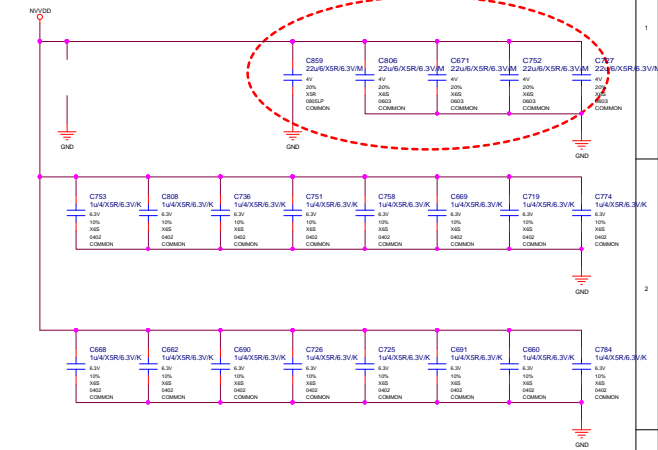
## FBVDD



## NVVDD

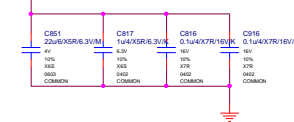


## NVVDD



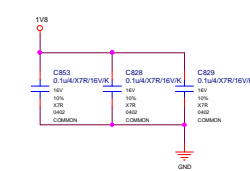
## 1V8\_AON

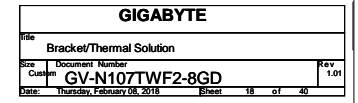
Place 1.0uF cap near BA10



place 1.0uF cap for BB14 and BC14 to share

## 1V8\_MAIN

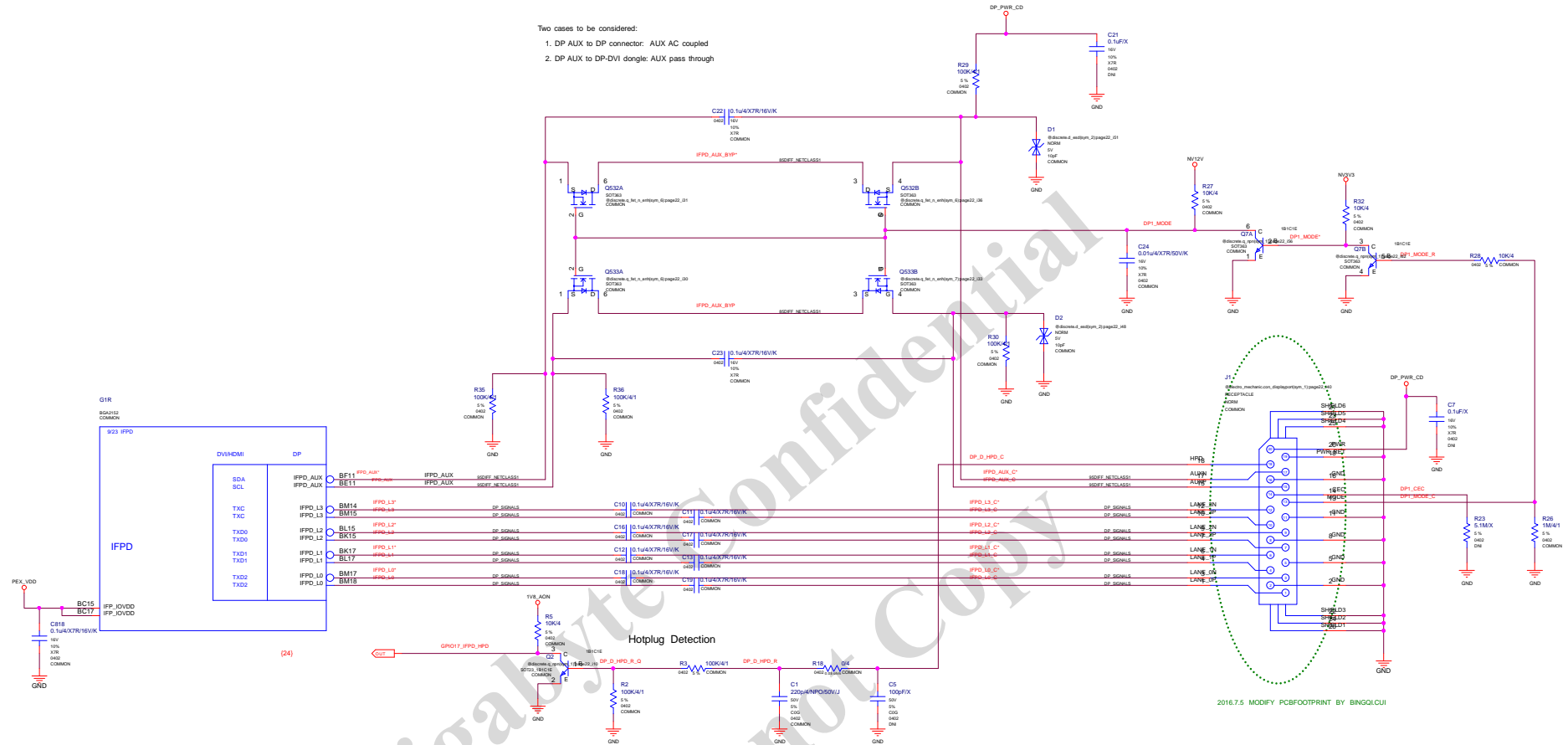












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IFPD DP

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MIOA/B Interface and FRAME LOCK

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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	SOR0/1/2/3 ENABLE
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE

1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

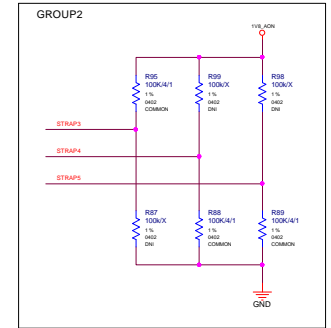
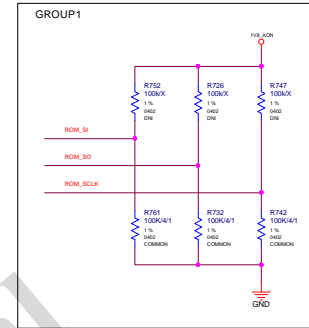
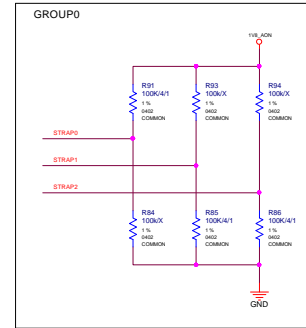
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER

1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

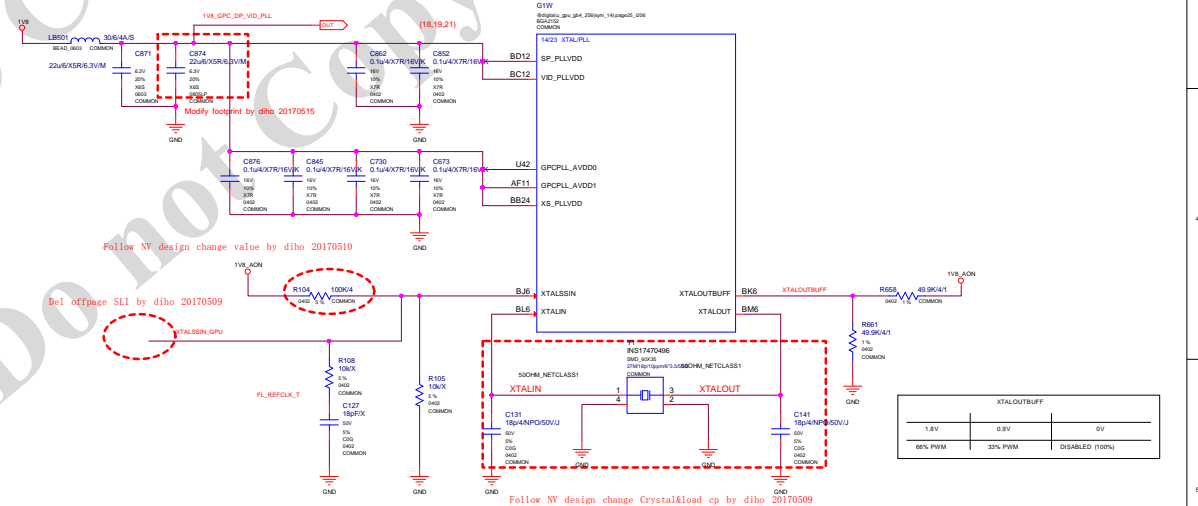
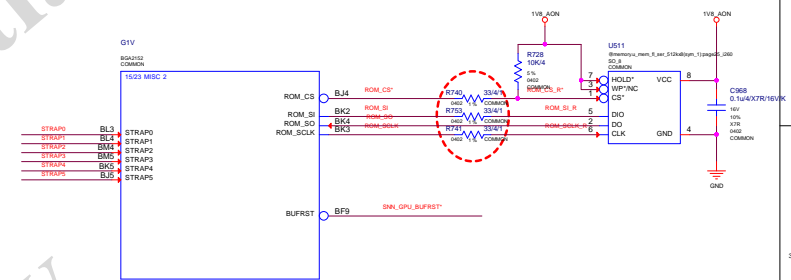
ASSEMBLY  
PAGE DETAIL

ASSEMBLY\_DESCRIPTION  
MISC: ROM, XTAL, STRAPS

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CFG(3:0)	Config	Width	Vendor
0000	256Mx32	256-bit	Samsung
0001	256Mx32	256-bit	Micron
0010	256Mx32	256-bit	Hynix
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		

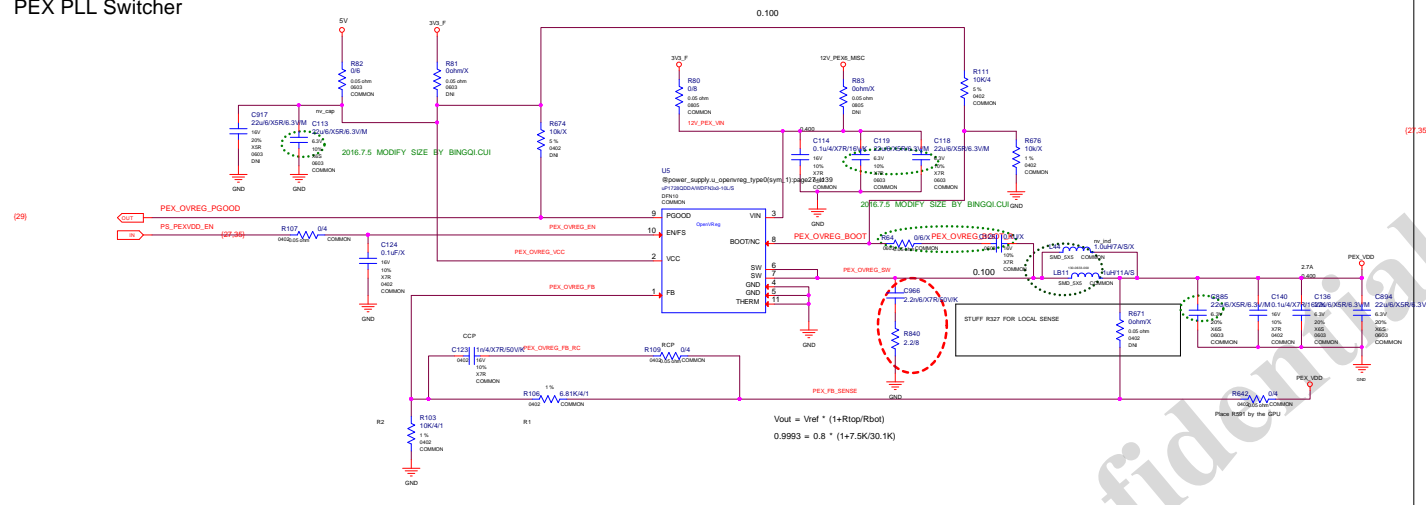


XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

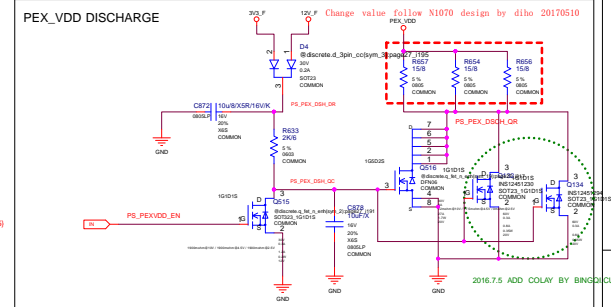
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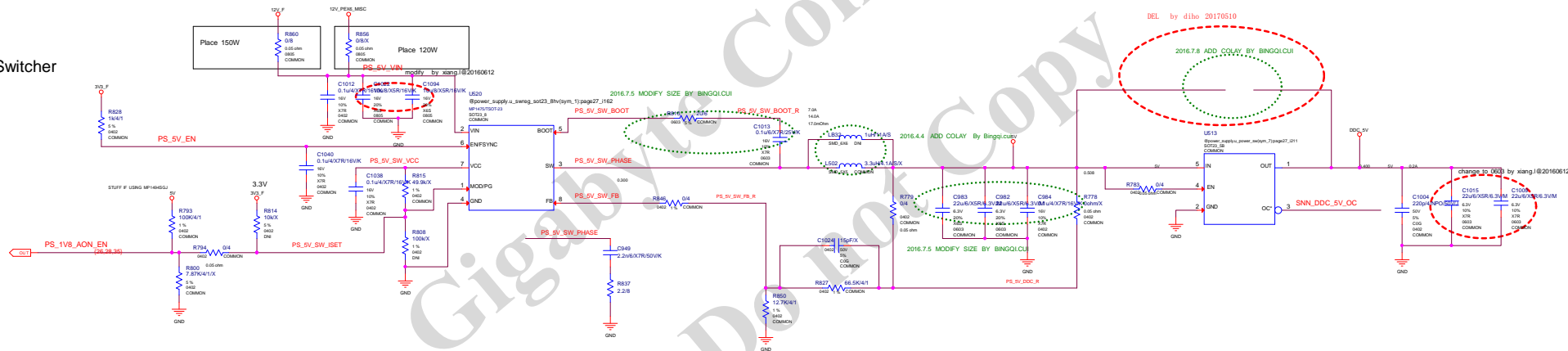
## PEX PLL Switcher



## PEX\_VDD DISCHARGE



## 5V Switcher

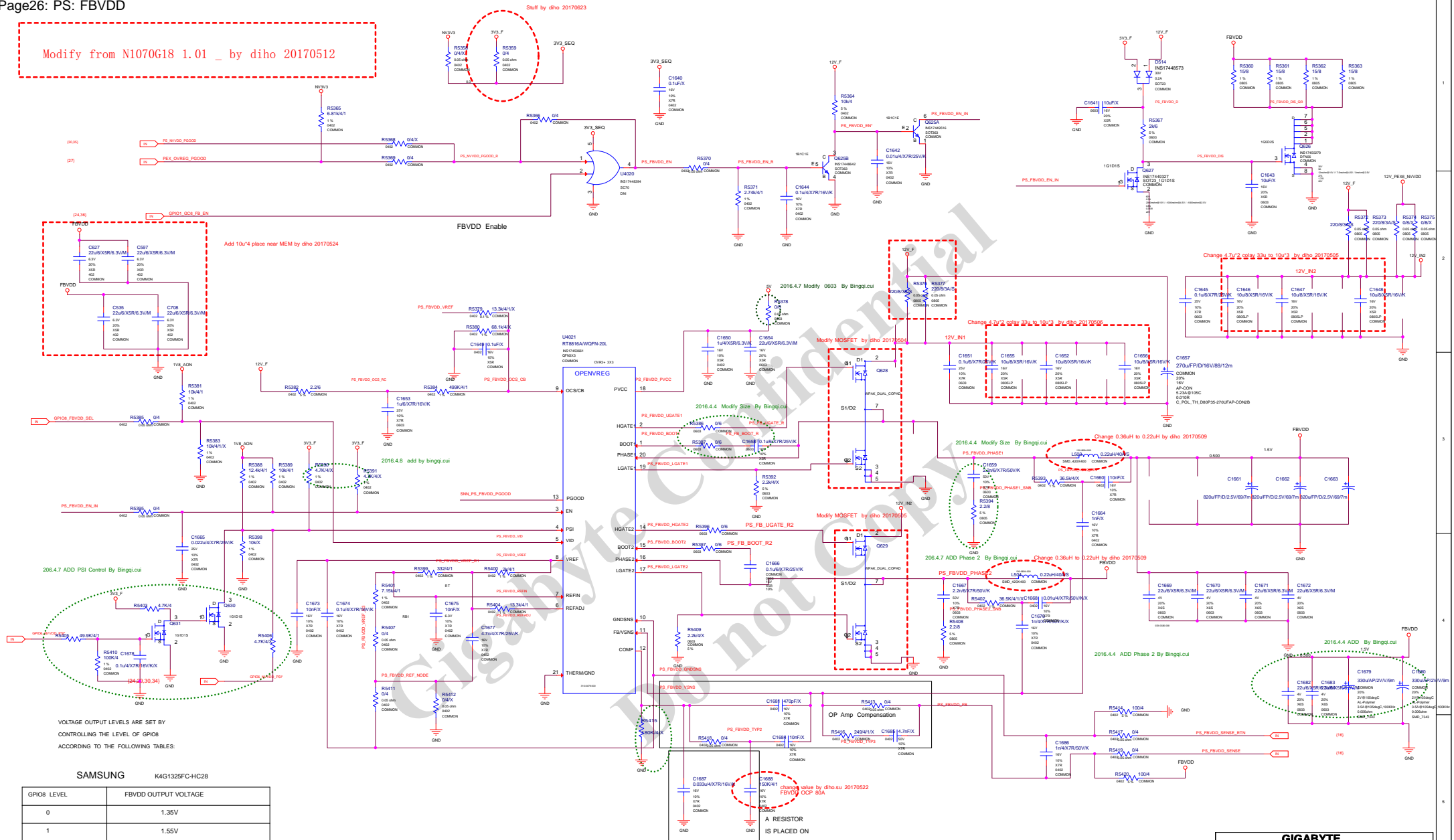


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GPIO8 LEVEL	FBVDD OUTPUT VOLTAGE
0	1.35V
1	1.55V

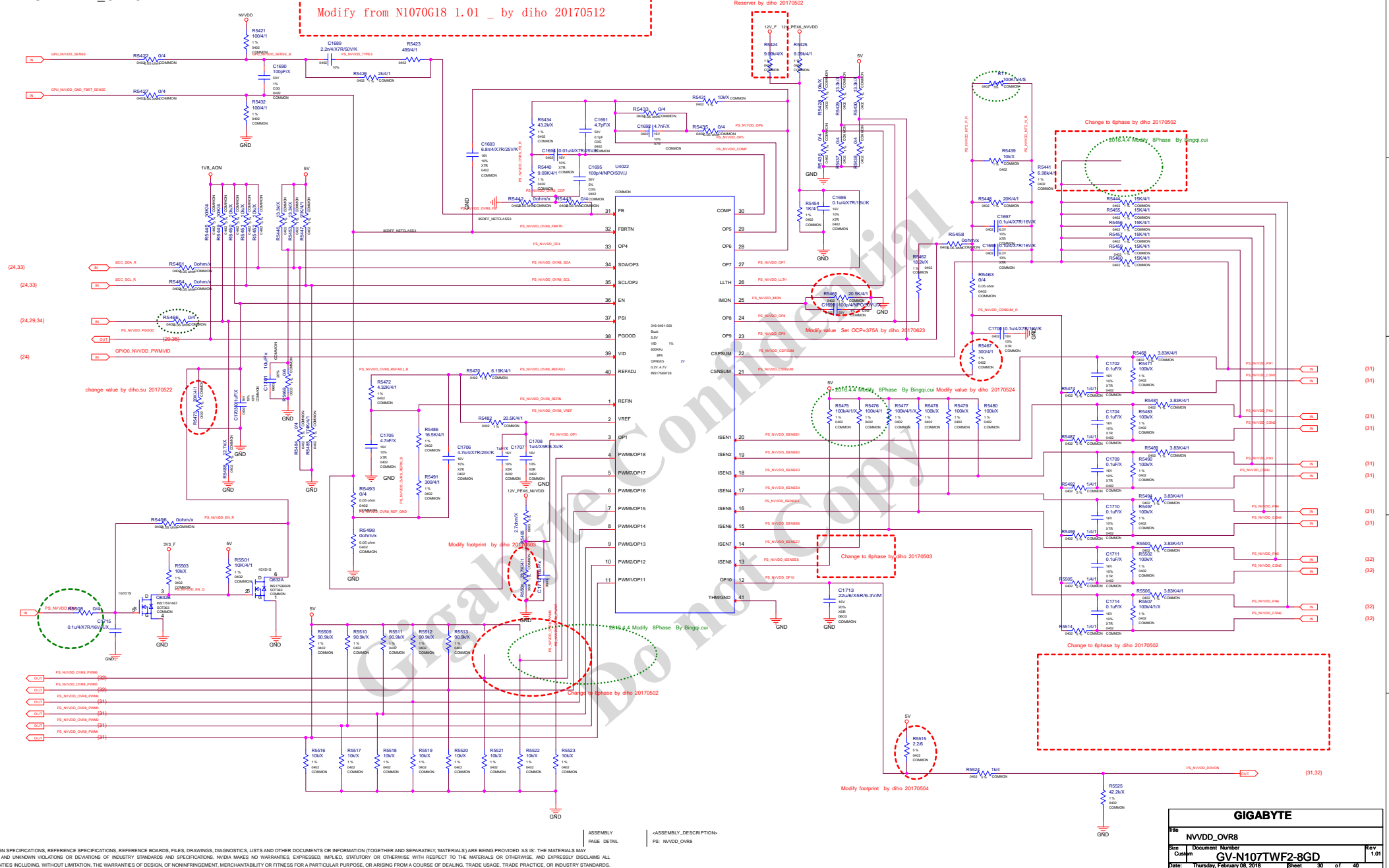
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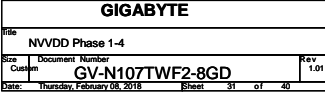
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDD

GM Amp Compensation C206 FOOTPRINT

## GIGABYTE

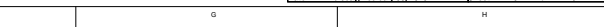
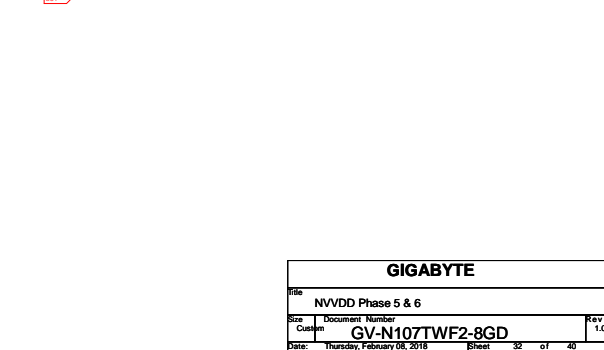
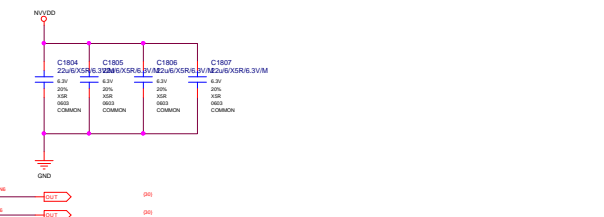
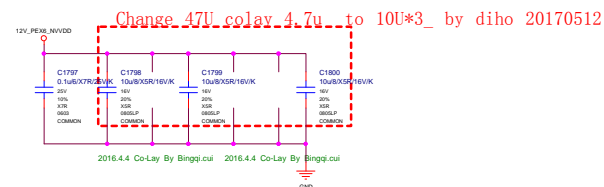
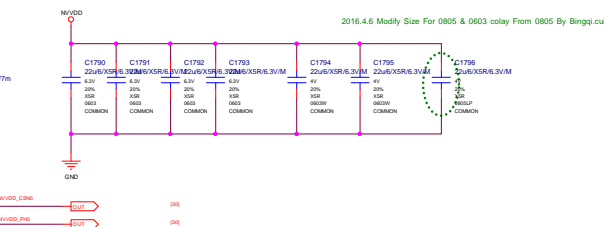
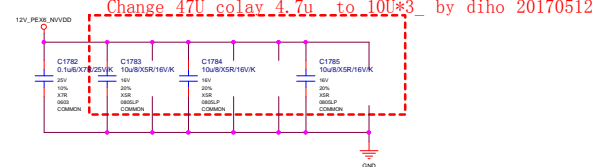
<b>GIGABYTE</b>			
Title: FBVDD			
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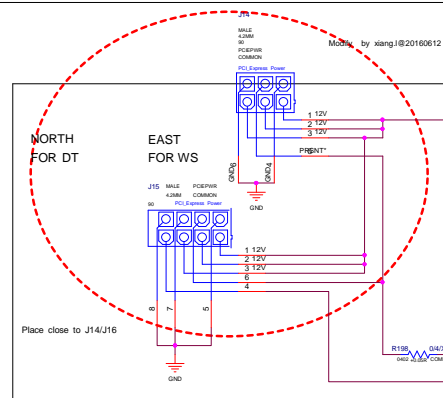
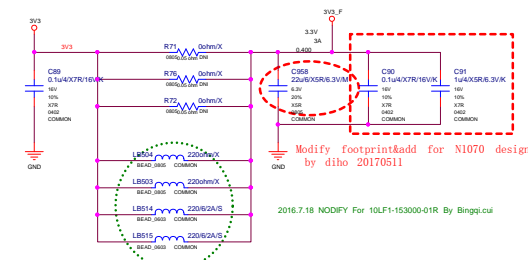
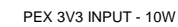
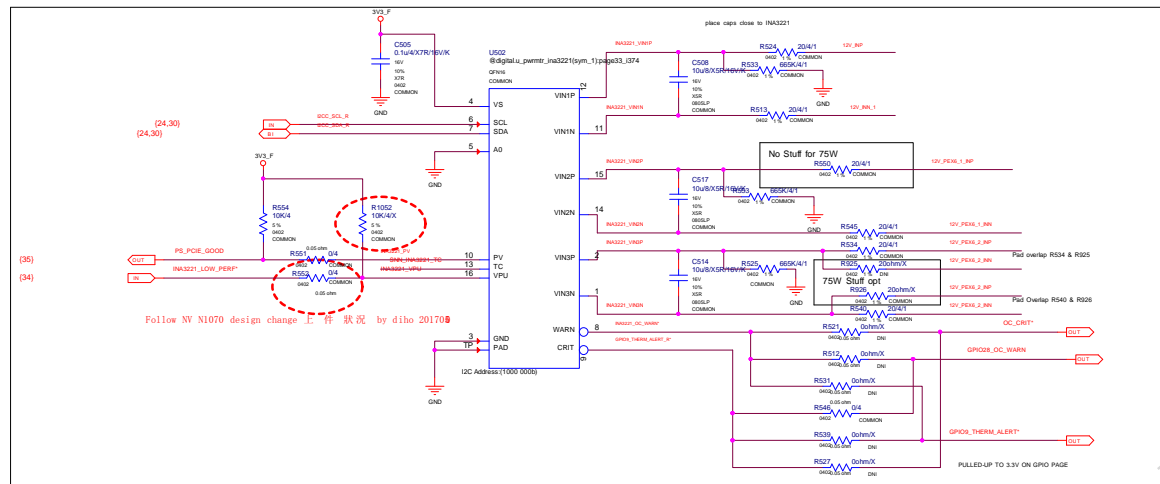


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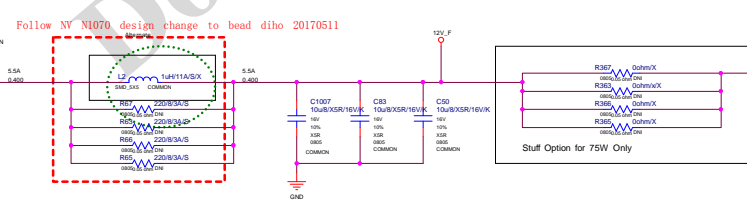
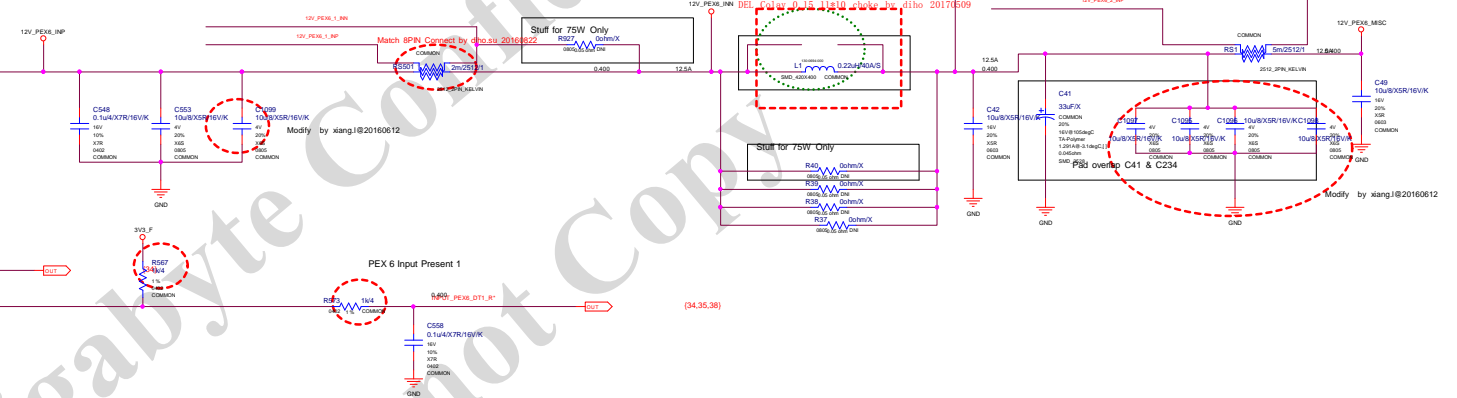
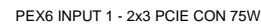
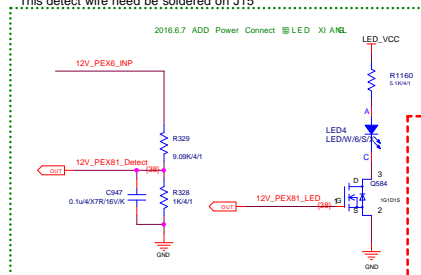
Change 47U colay 4.7u\_ to 10U\*3\_ by diho 20170512





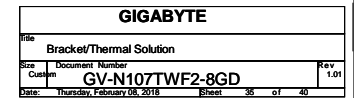
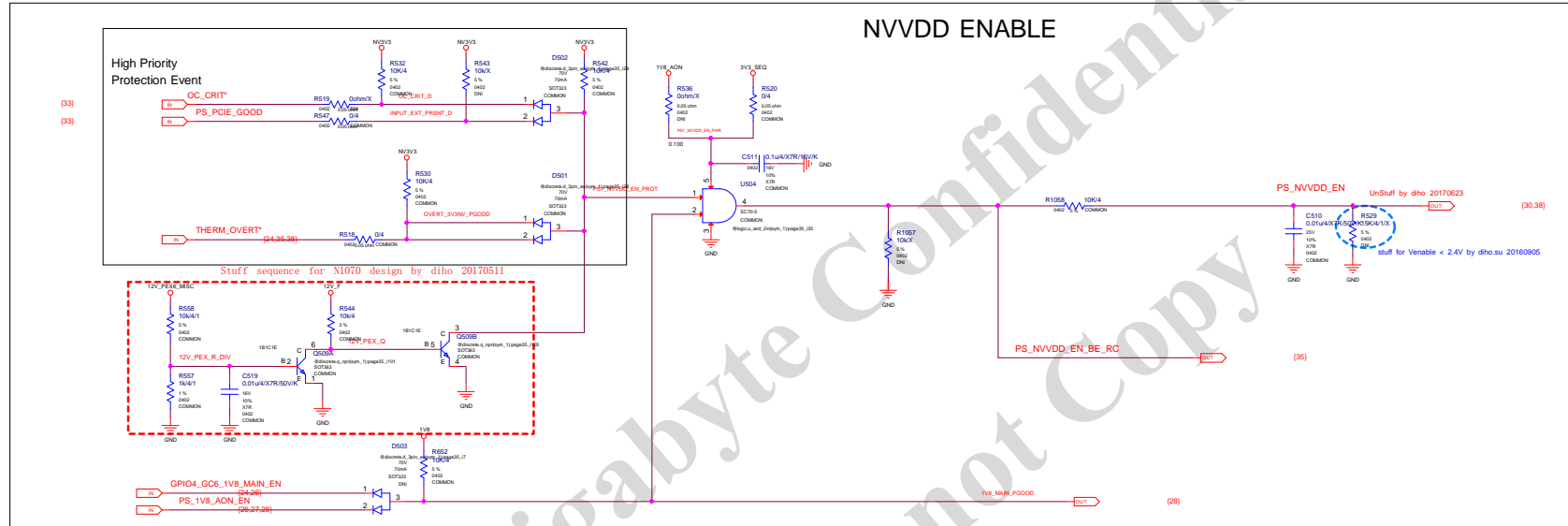


J14 and J16 is the soldering holes for power cable.  
The power cable Need a seperate wire as detect pin  
This detect wire need be soldered on J15

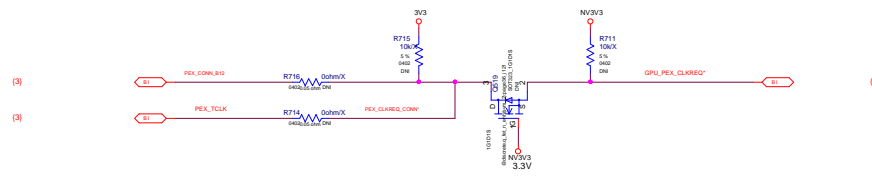


<b>GIGABYTE</b>			
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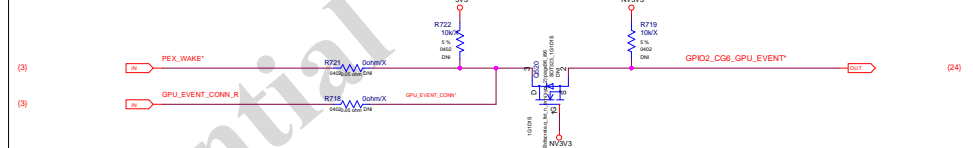




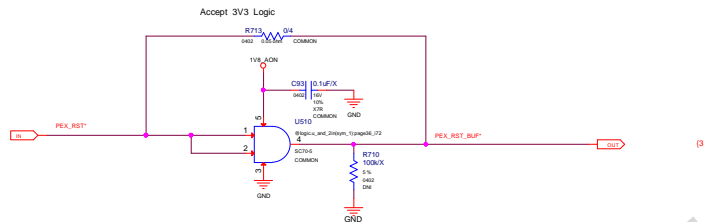
### PEX\_CLKREQ\*



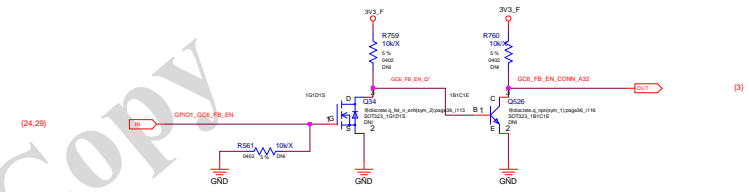
### GPU\_EVENT\*



### PEX\_RST# LOGIC



### GC6 FB ENABLE

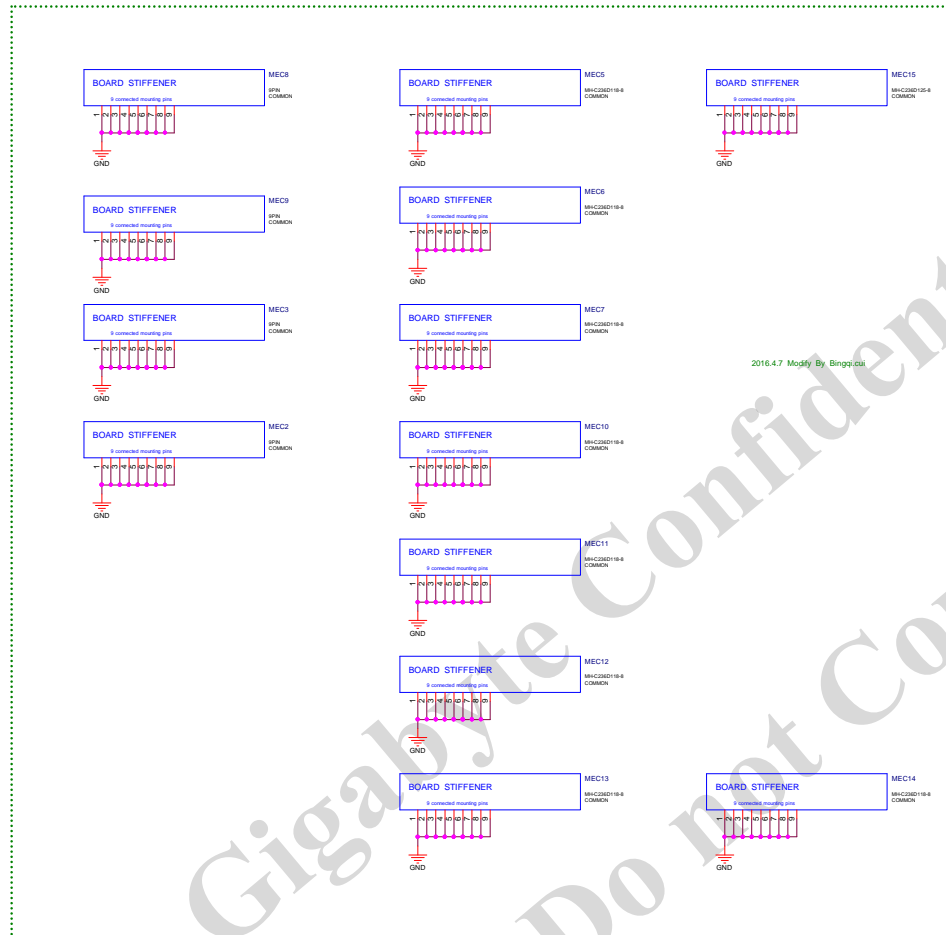


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PS: GC6 MISC

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ASSEMBLY  
PAGE DETAIL

<ASSEMBLY\_DESCRIPTION>  
MECH

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/X by diho 20170510

MCU\_R  
MCU\_G  
MCU\_B

X1\_LED

X2\_LED

FAN Stop LED

Windforce\_LED

/X &amp; Del Colay 2pin connect by diho 20170510

J513, J512  
Co-Lay

GIGABYTE

LED			
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PAGE DETAIL

ASSEMBLY DESCRIPTION  
MECH

History									
Data		Modify							
2016.04.04		First version							
2017.05.10		Modify PCB Layers							