40P201- NV40 HIGH END BOARD

NV 40 E201_A02 - NV40 Flipchip BGA, 4 x 64MB DDR3 (8 x 8Mx32 = 256MB) Internal TMDS (dual link) and External TMDS (dual link). Internal TVout. TV Capture 7114/5

Table of Contents:

- 1. Table of Contents .. this page
- 2. AGP 8X Interface
- 3. Memory: FB_A & FB_B Partitions
- 4. Memory: FB_A BankO
- 5. Memory: FB_B BankO
- 6. Memory: FB_C & FB_D Partitions
- 7. Memory: FB_C BankO
- 8. Memory: FB_D BankO
- 9. Memory Signal Constraints, FB Cal, Vref
- 10. External Clock Generators
- 11. BIOS, Strappings, PLL Filters
- 12. DAC_A, DAC_B, PLL and SYNCbuffer
- 13. DVO A & B Interface
- 14. DACA Filter and VGA connector
- 15. DACB VGA/TV Switch, misc GPU connections
- 16. DACB Filter and VGA connector
- 17. DVI Connectors South and Mid, Internal TMDS
- 18. DUAL TMDS External with Silicon Image
- 19. Video Capture (SAA7114)
- 20. Video In/Out Connector External/Internal (MiniDin) Video In Connector Internal, STEREO
- 21. GNDs, Thermal GNDs, FBVDDQ and FBVTT decoup caps
- 22. 3.3V and NVVDD decoup caps
- 23. GPIOs, NVVDD VID, Thermal and FAN Control
- 24. External Power Connection and Detection
- 25. Power Supply I: A3V3, TMDS POWER
- 26. Power Supply III: FBVDD, FBVDDQ, & FBVTT
- 27. Power Supply IV: NVVDD
- 28. Mechanical

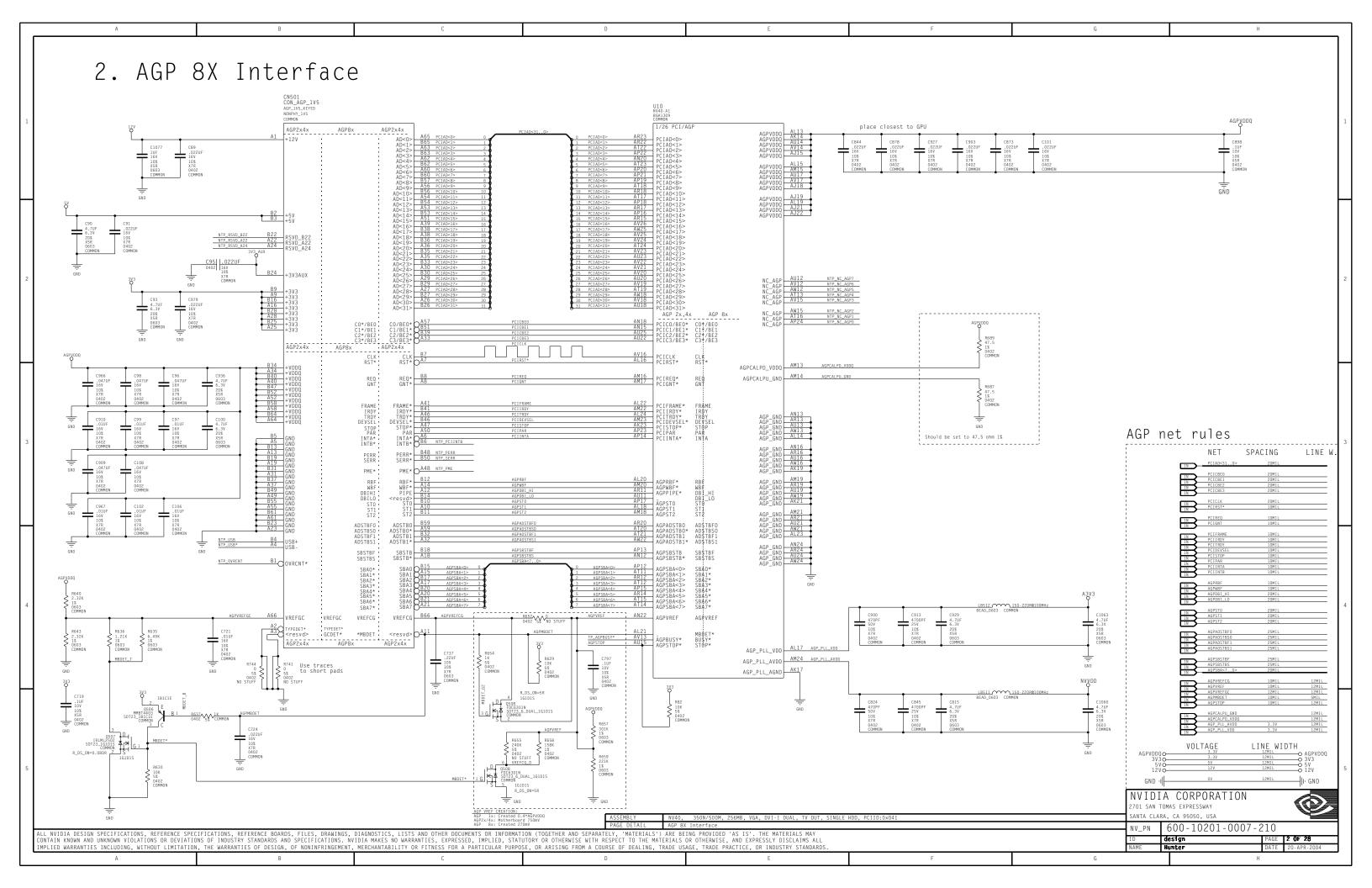
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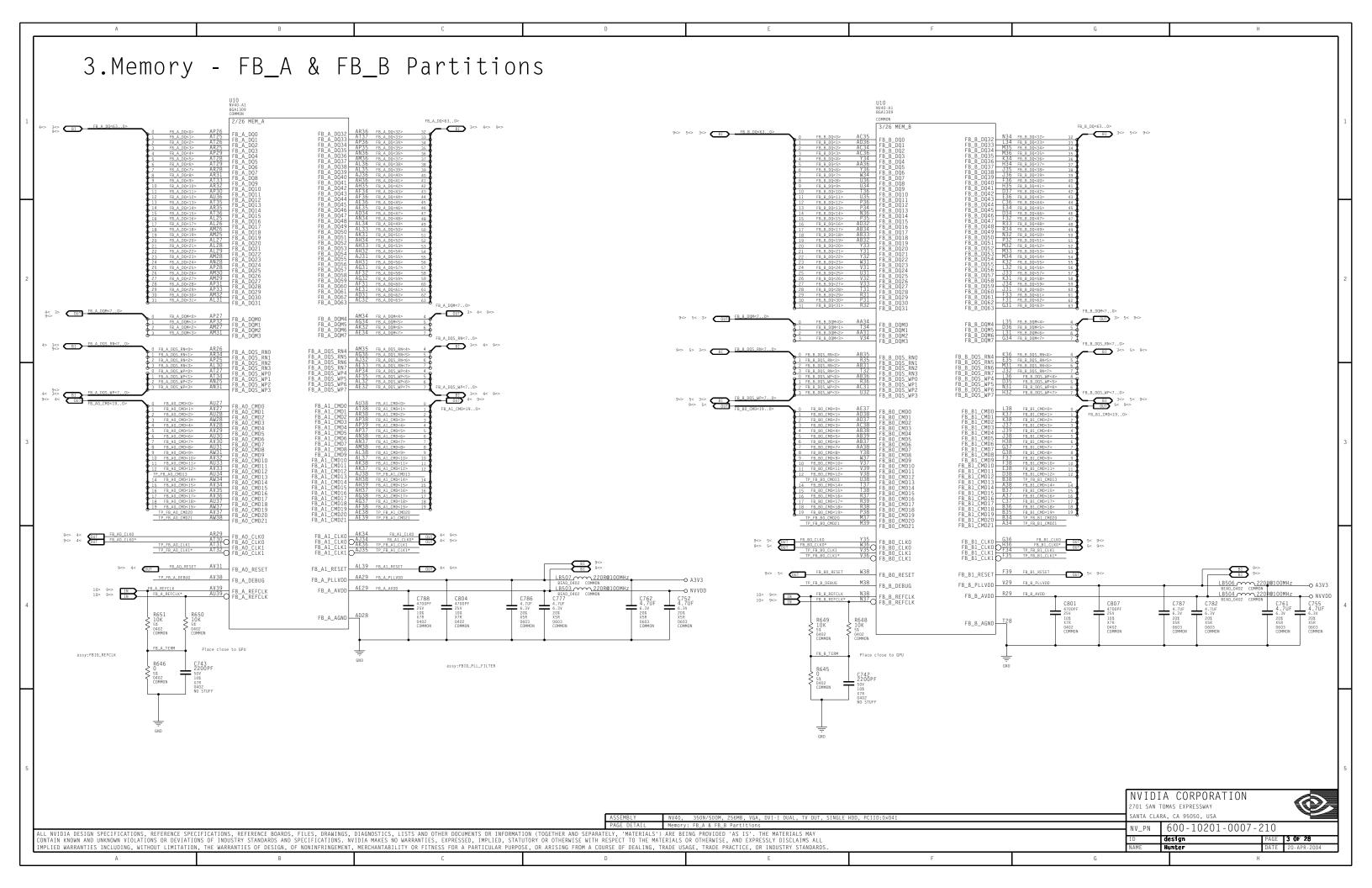
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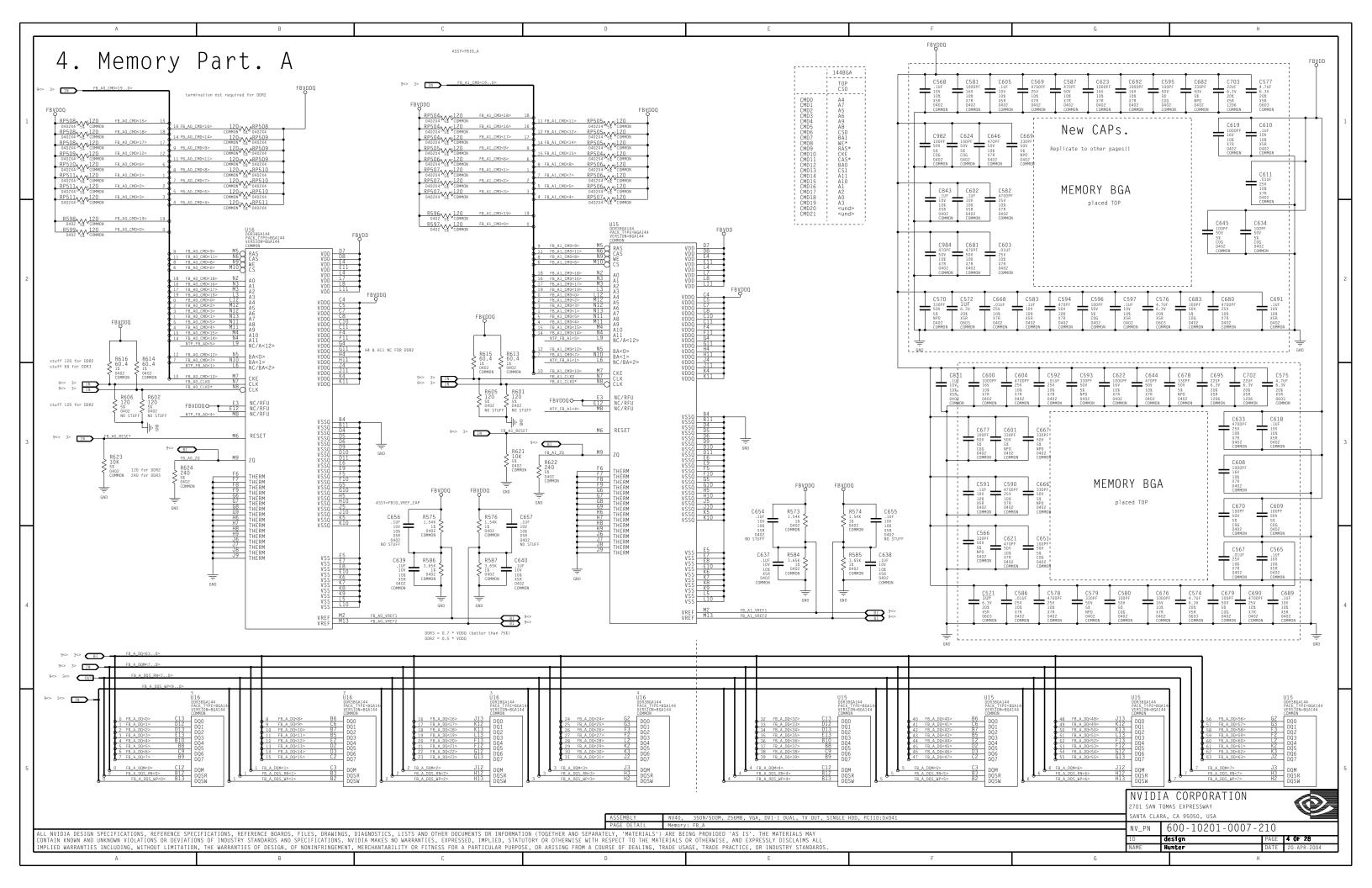
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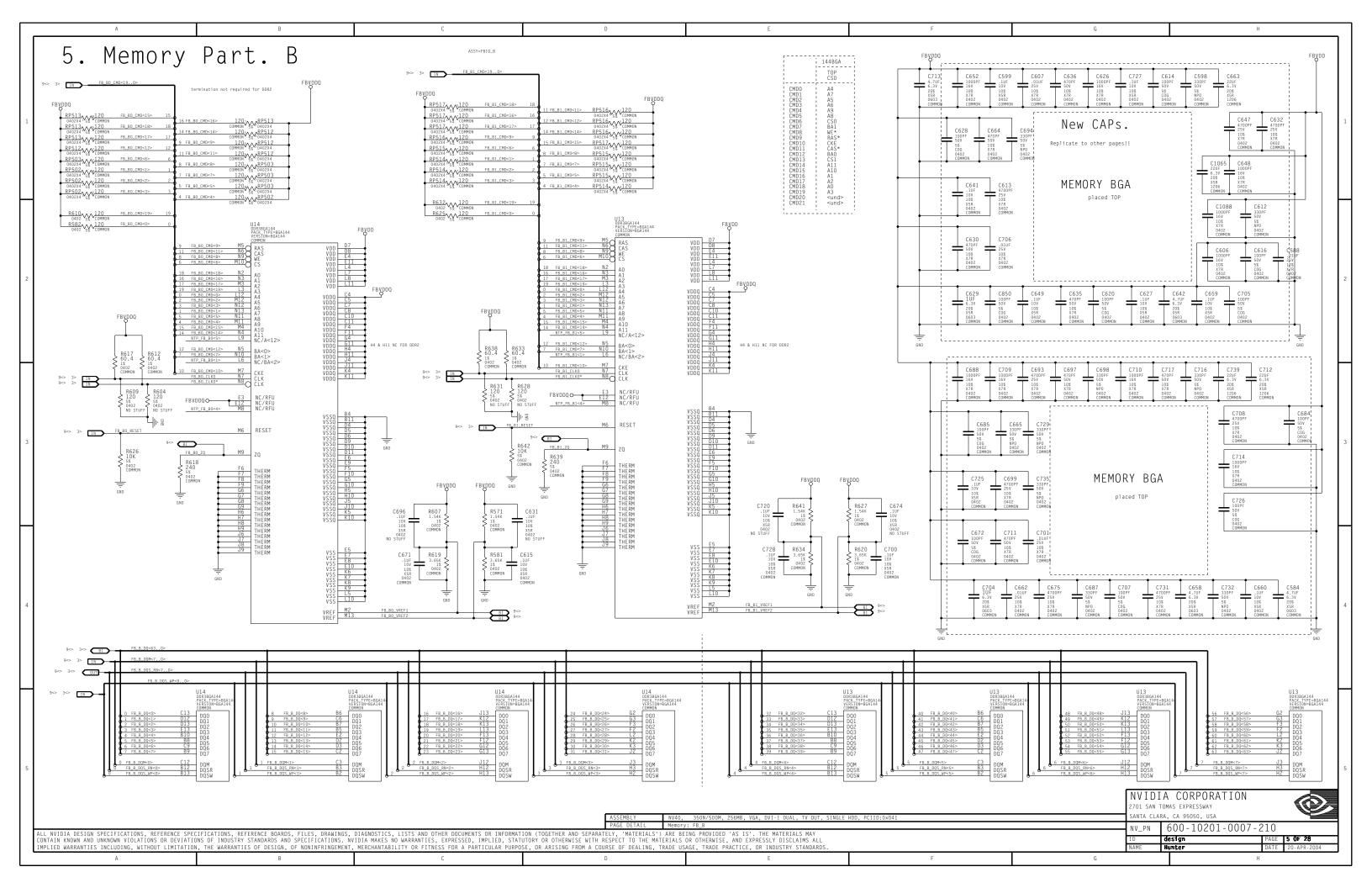
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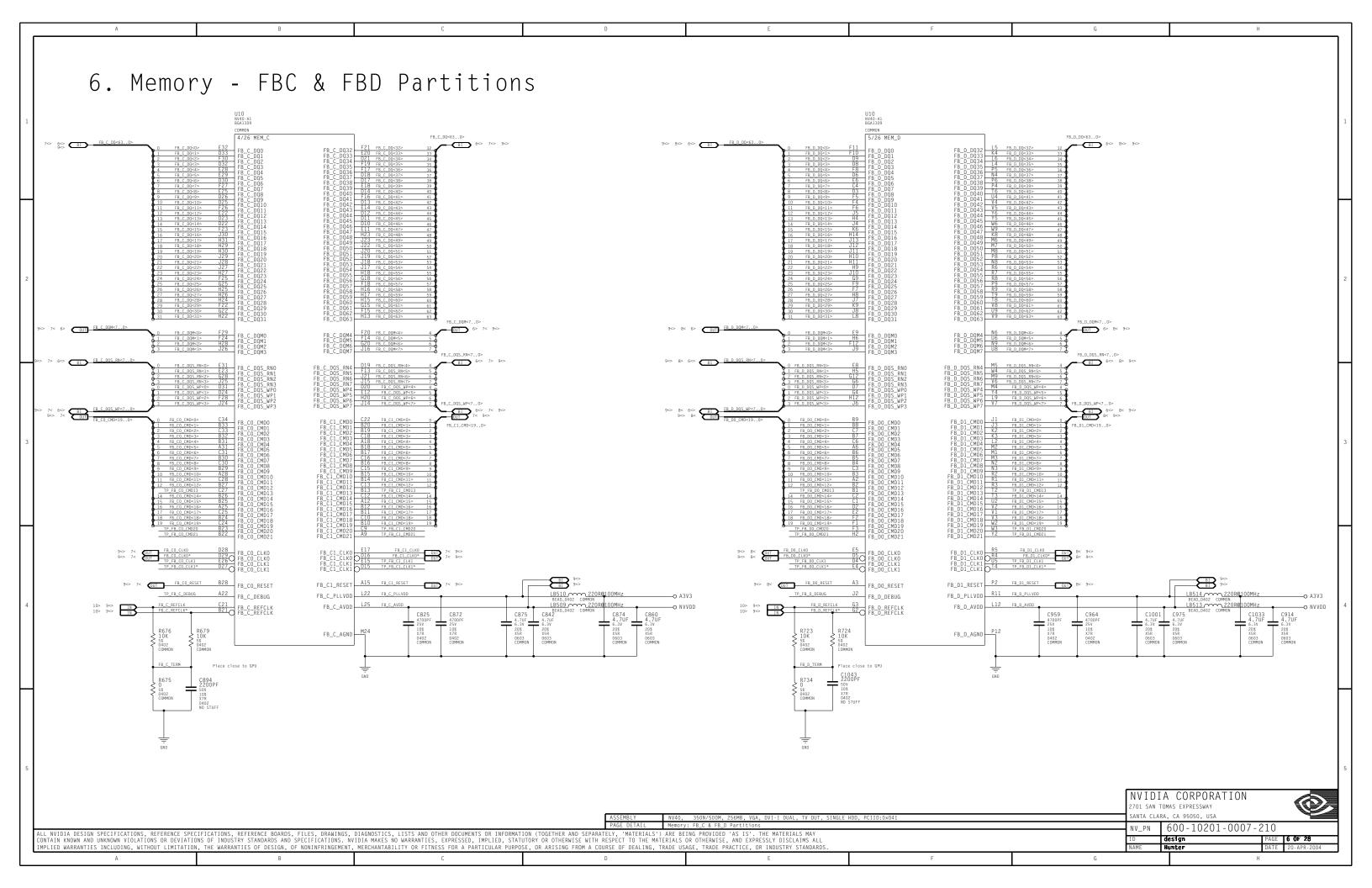
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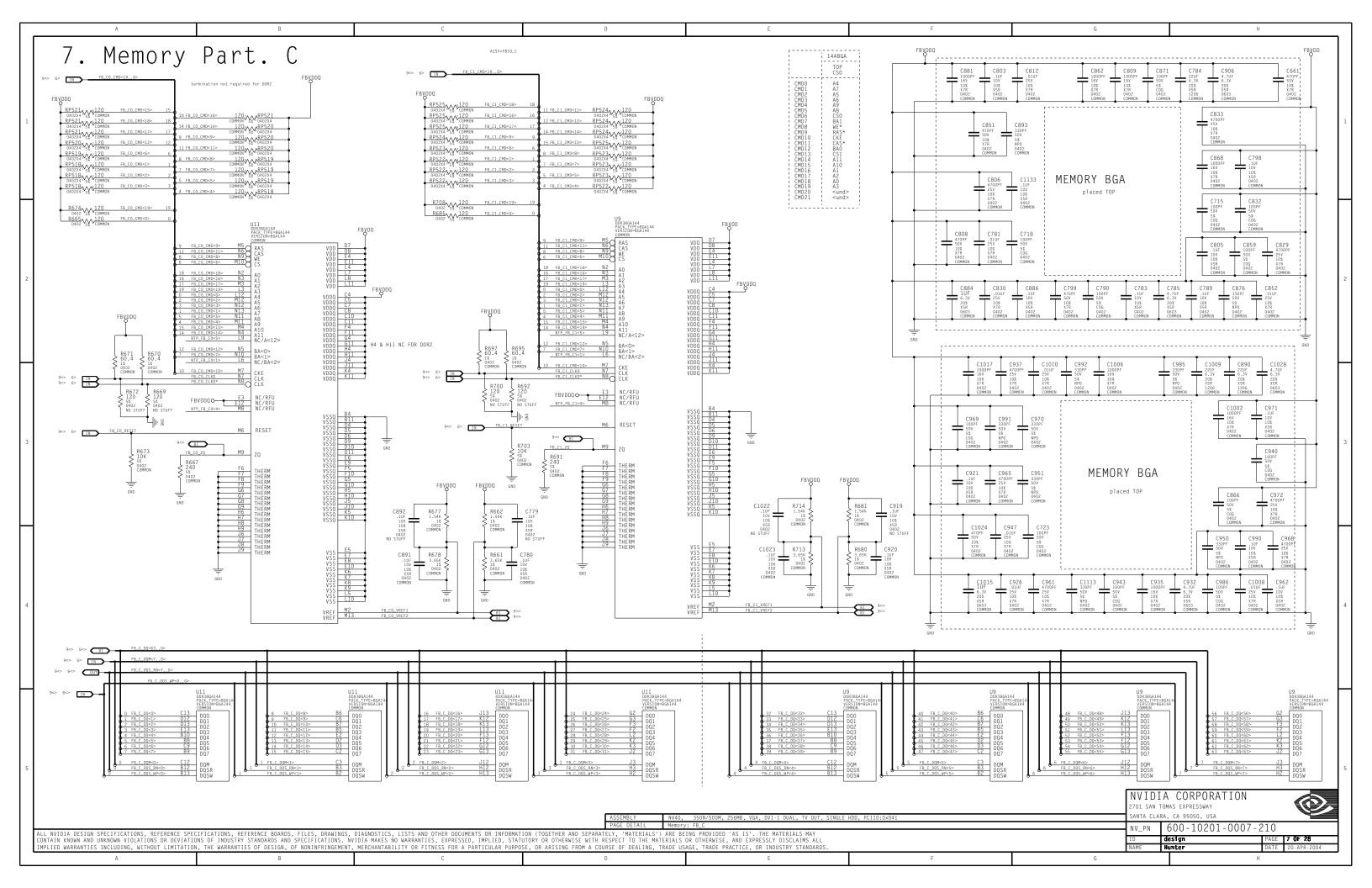


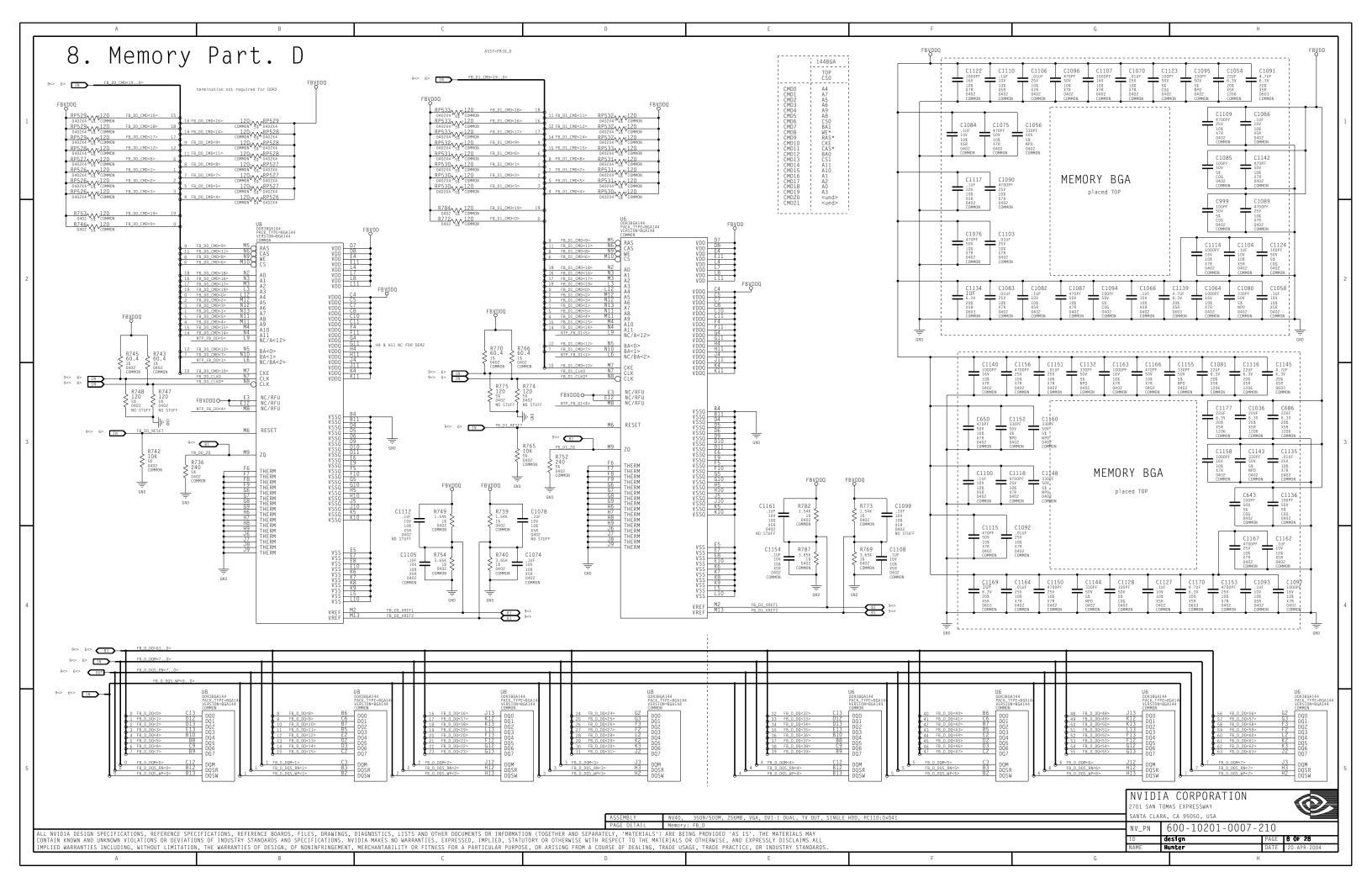






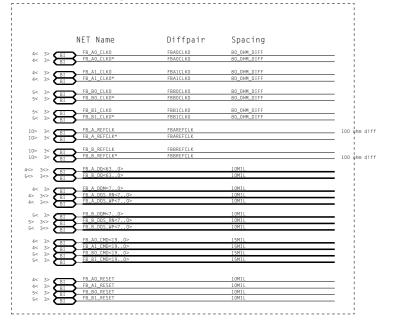






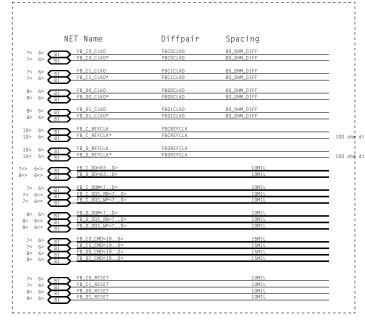
9. Memory NET SPACING RULES, FB CAL & VREF

Memory FBA FBB

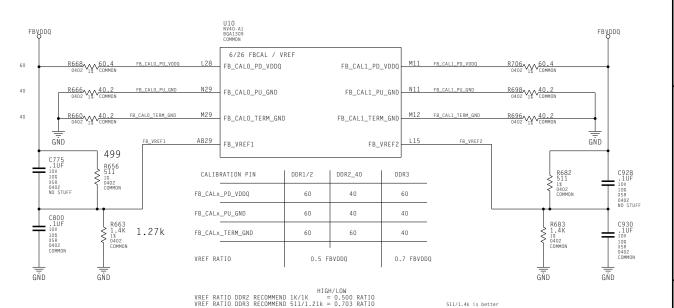


	NET Name	MIN_LINE_WIDTH	VOLTAGE
3<> BI	FB_A_AVDD	12MIL	3.
3 BI	FB_A_PLLVDD	12MIL	3.
3<> BI	FB_B_AVDD	12MIL	3.
3 BI	FB_B_PLLVDD	12MIL	3.
4<> BI	FB_AO_ZQ	12MIL	0.
4<> BI	FB_A1_ZQ	12MIL	0.
5<> BI	FB_B0_ZQ	12MIL	0.
50 BI	FB_B1_ZQ	12MIL	0.
4<> BI	FB_AO_VREF1	12MIL	0.
4<> BI	FB_A0_VREF2	12MIL	0.
4<> BI	FB_A1_VREF1	12MIL	0.
4<> BI	FB_A1_VREF2	12MIL	0.
5<> BI	FB_B0_VREF1	12MIL	0.
5<> BI	FB_B0_VREF2	12MIL	0.
5<> BI	FB_B1_VREF1	12MIL	0.
5<> BI	FB B1 VREF2	12MIL	0.

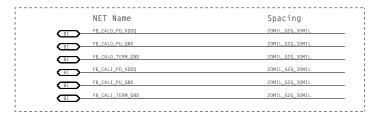
Memory FBC FBD



	NET Name	MIN_LINE_WIDTH	VOLTAGE
6<> BI	FB_C_AVDD	12MIL	3.3
60 BI	FB_C_PLLVDD	12MIL	3.3
6<	FB_D_AVDD	12MIL	3.3
60 BI	FB_D_PLLVDD	12MIL	3.3
7< nt	FB_CO_ZQ	12MIL	0.9
7 BI	FB_C1_ZQ	12MIL	0.9
80 BI	FB_D0_ZQ	12MIL	0.9
8 BI	FB_D1_ZQ	12MIL	0.9
7<> BI	FB_CO_VREF1	12MIL	0.9
7 BI	FB_CO_VREF2	12MIL	0.9
7 BI	FB_C1_VREF1	12MIL	0.9
7 BI	FB_C1_VREF2	12MIL	0.9
80 BI	FB_DO_VREF1	12MIL	0.9
80 BI	FB_DO_VREF2	12MIL	0.9
80 BI	FB_D1_VREF1	12MIL	0.9
80 BI	FB D1 VREF2	12MIL	0.9



DEFAULT BASE SCHEMATICS ARE SETUP FOR DDR3



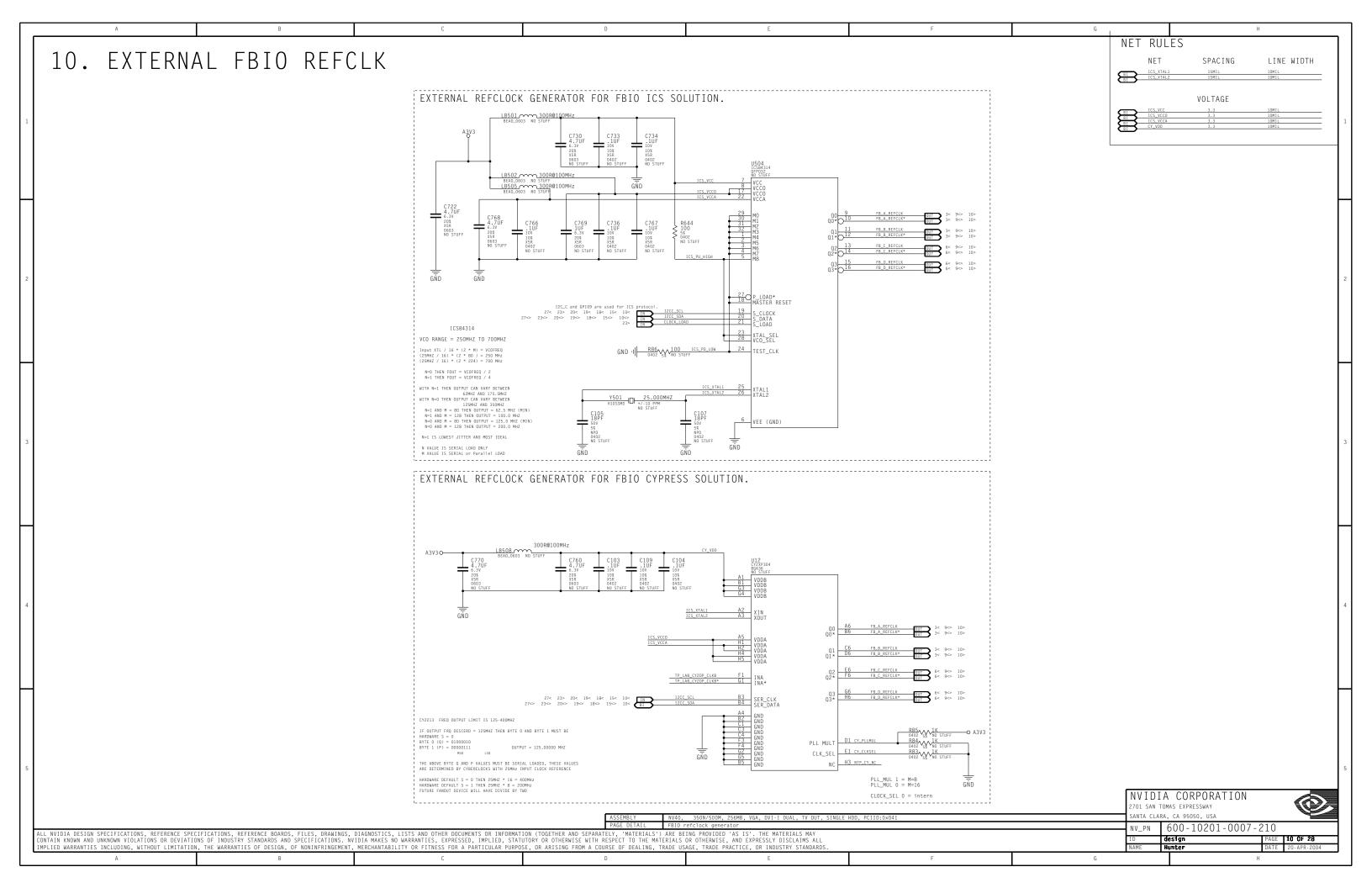
		NET Name	MIN_LINE_WIDTH	VOLTAGE
- 1	₽	FB_VREF1	12MIL	3.3V
i	}	FB_VREF2	12MIL	3.3V
1				
1				

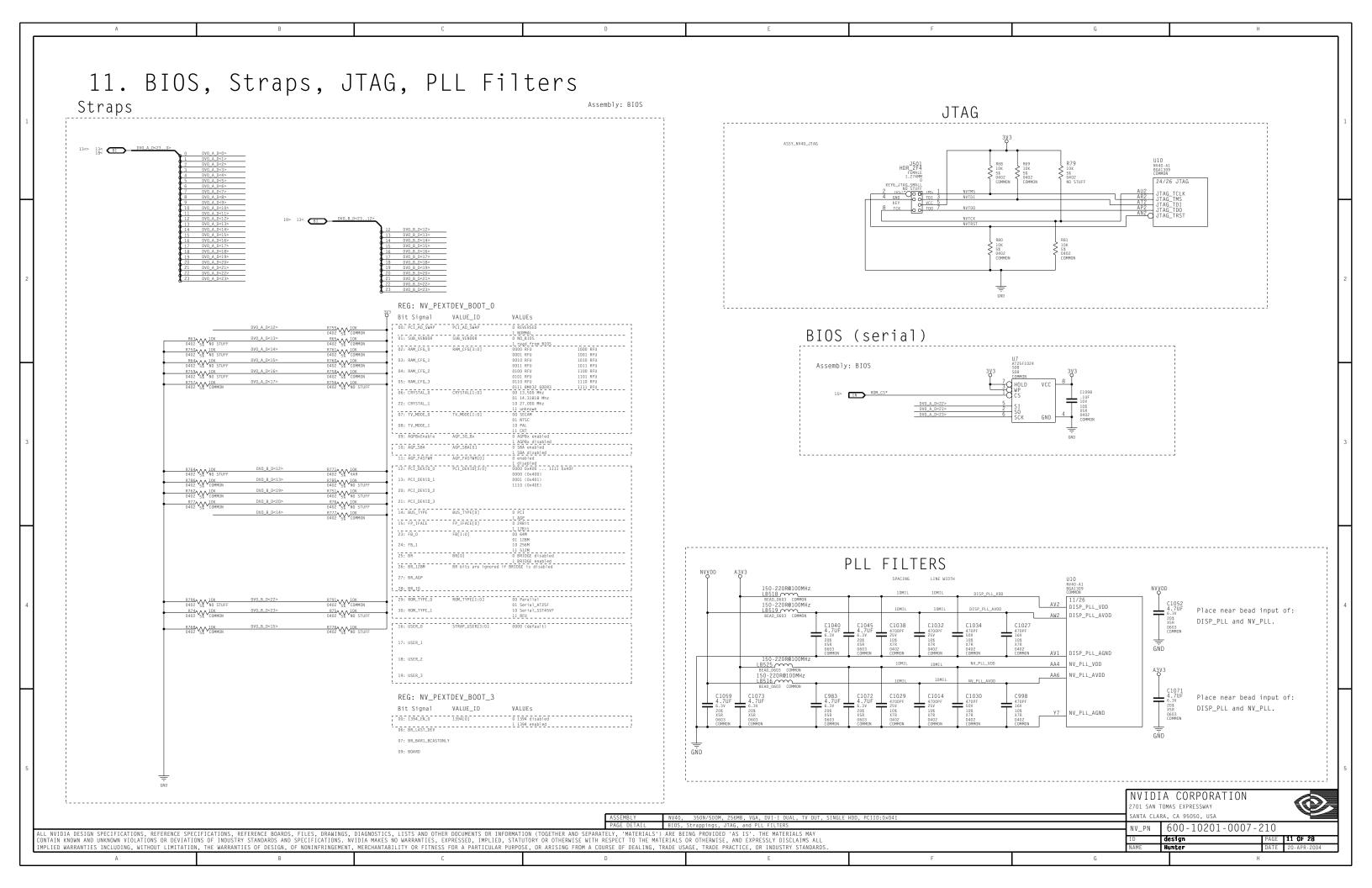
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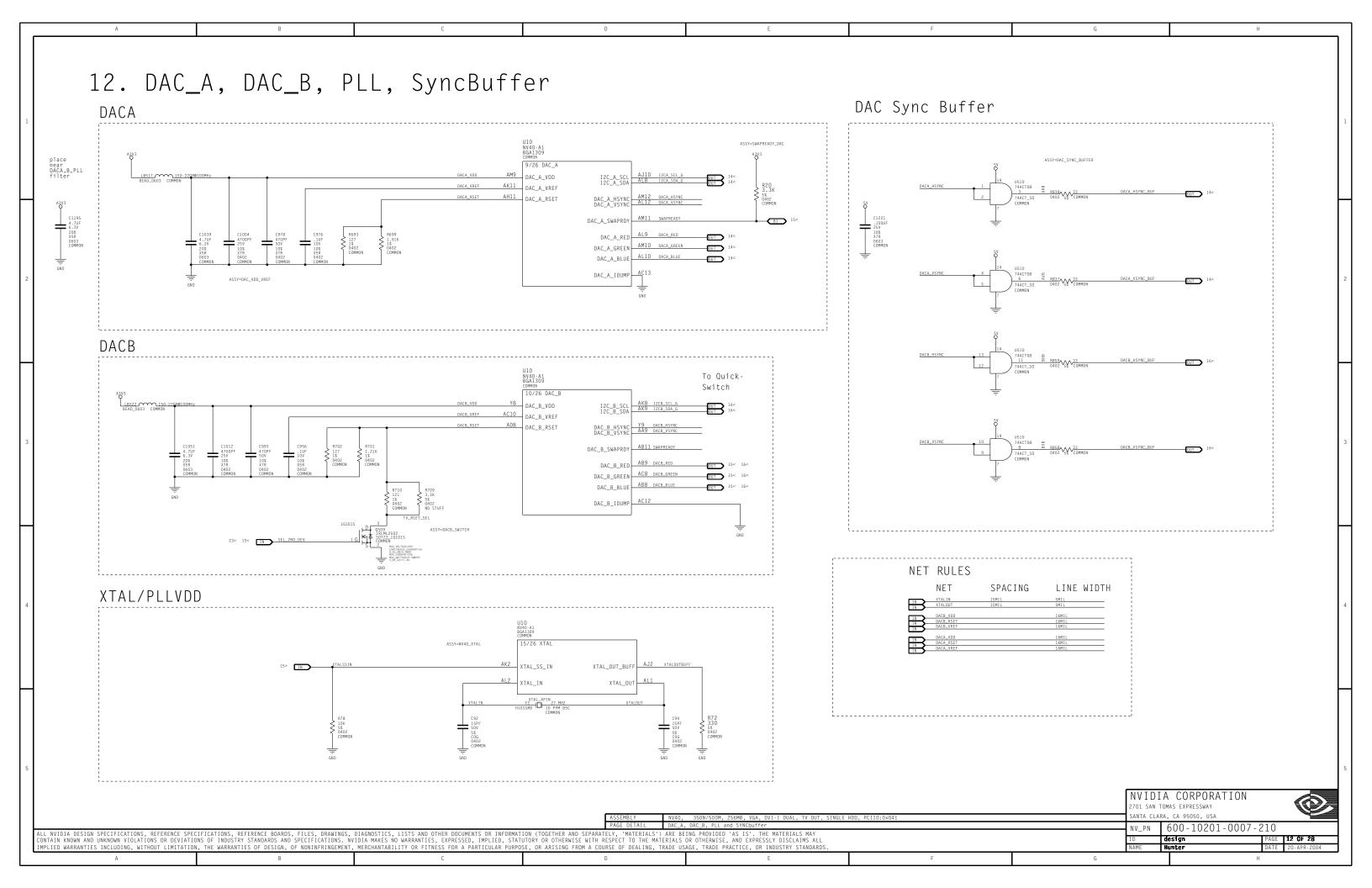
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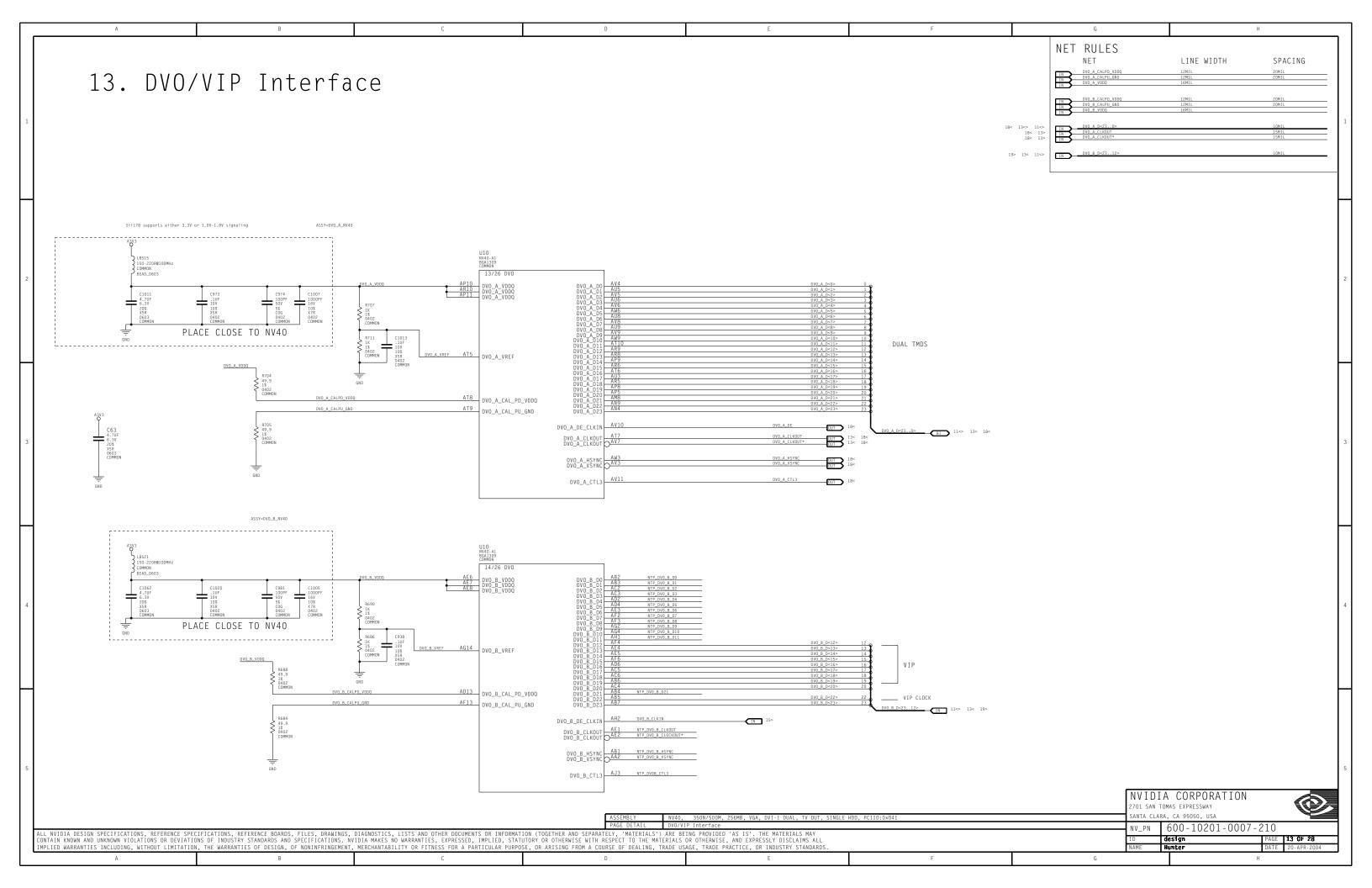
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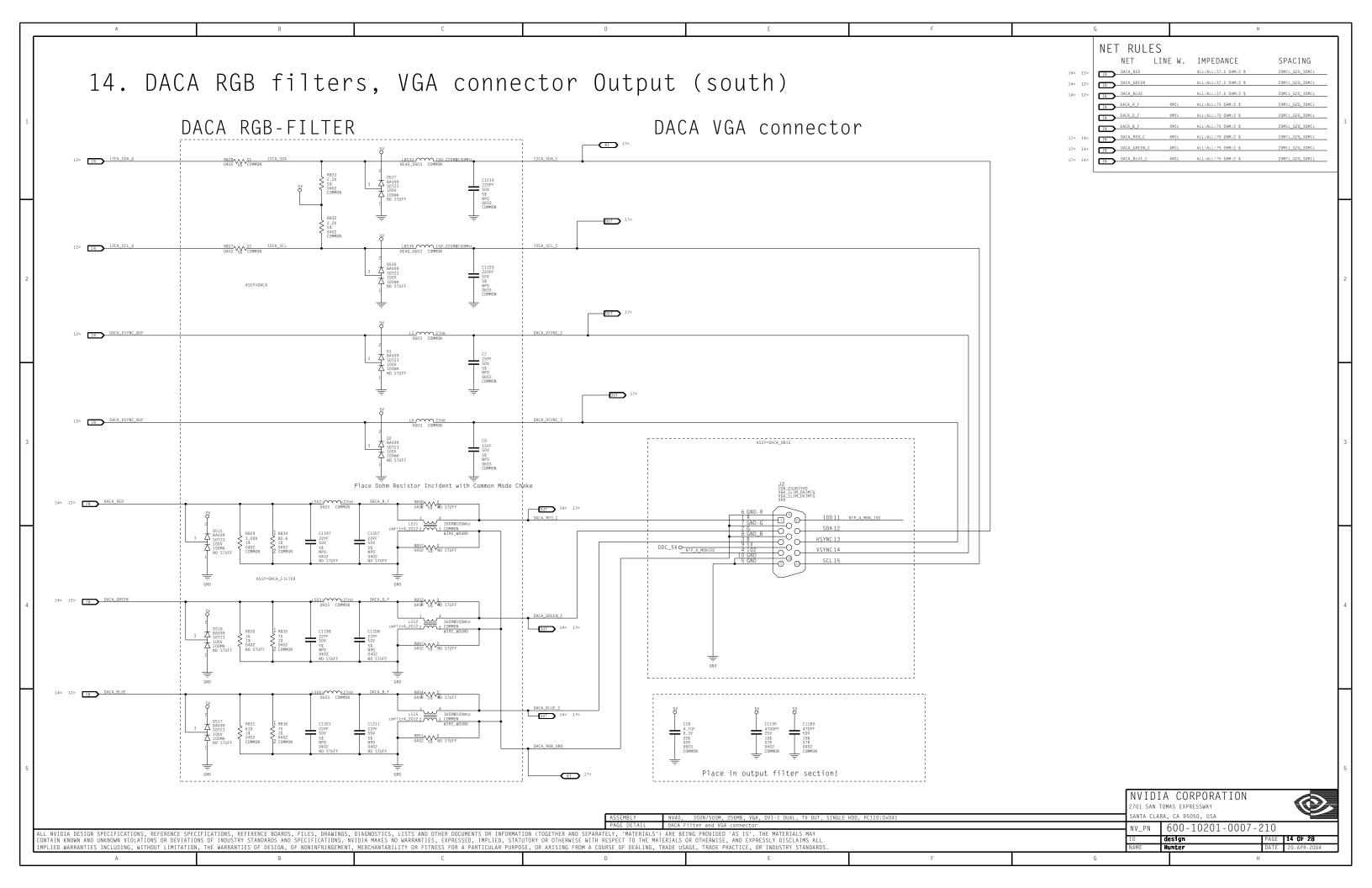
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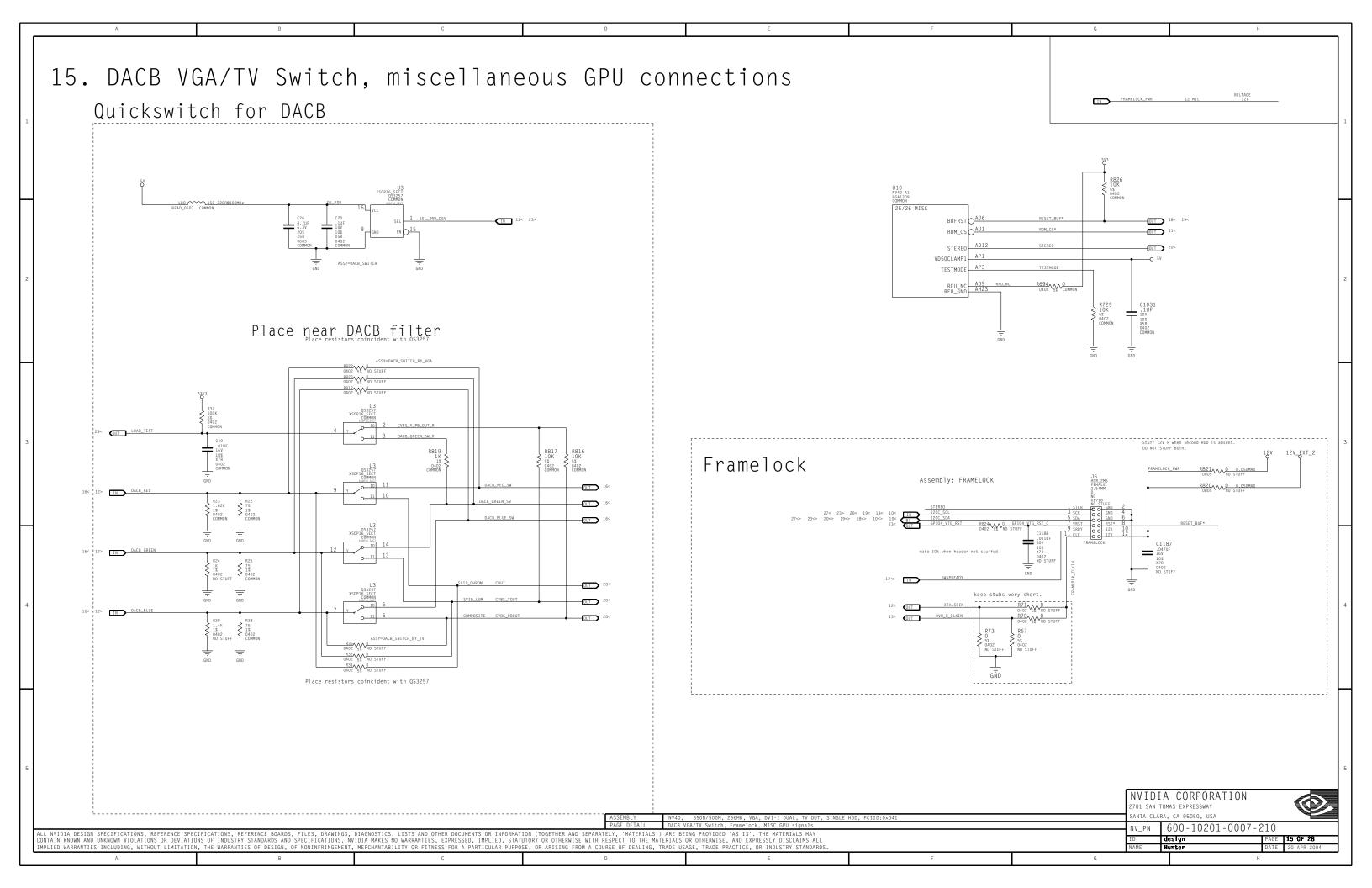


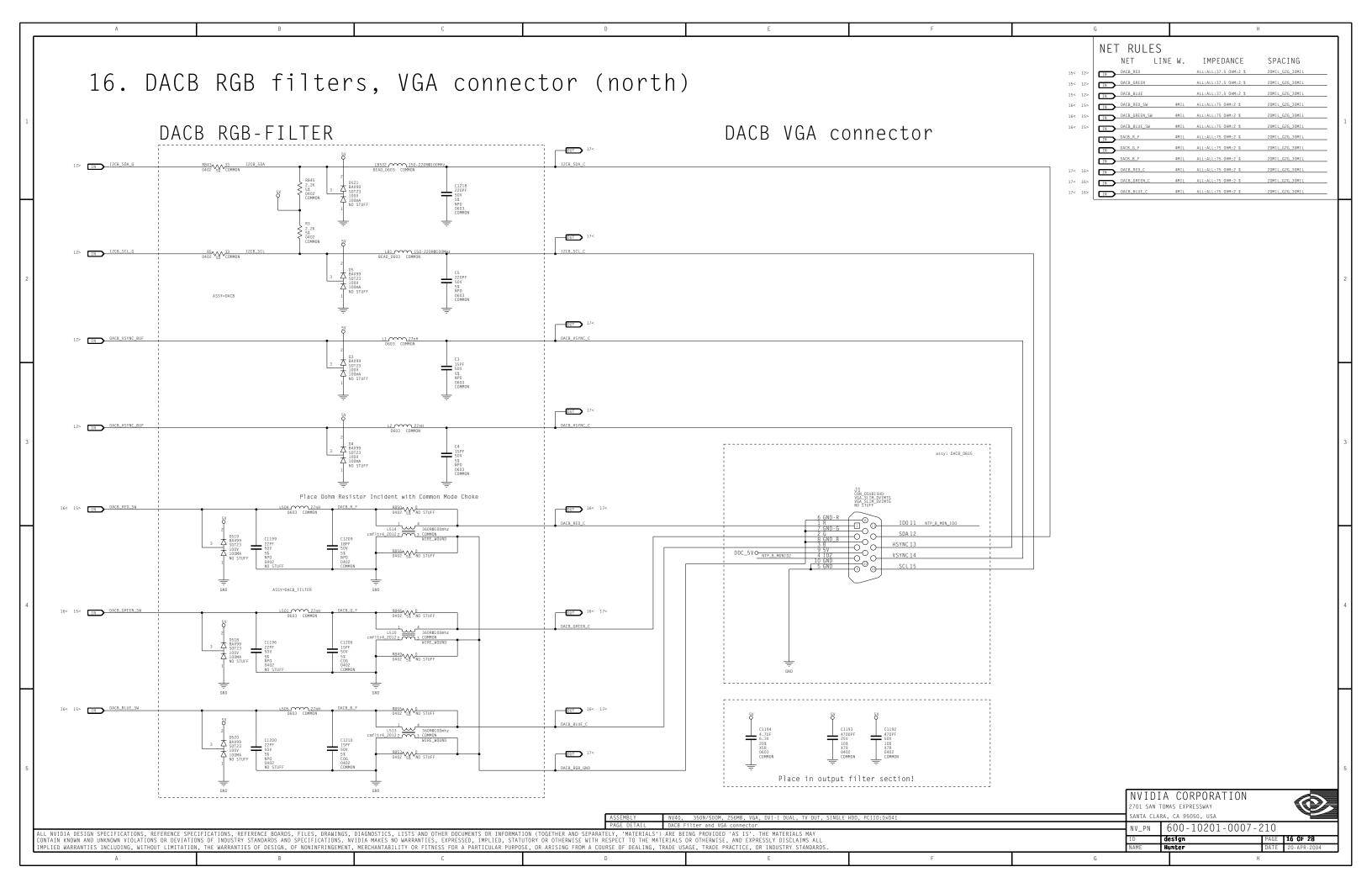


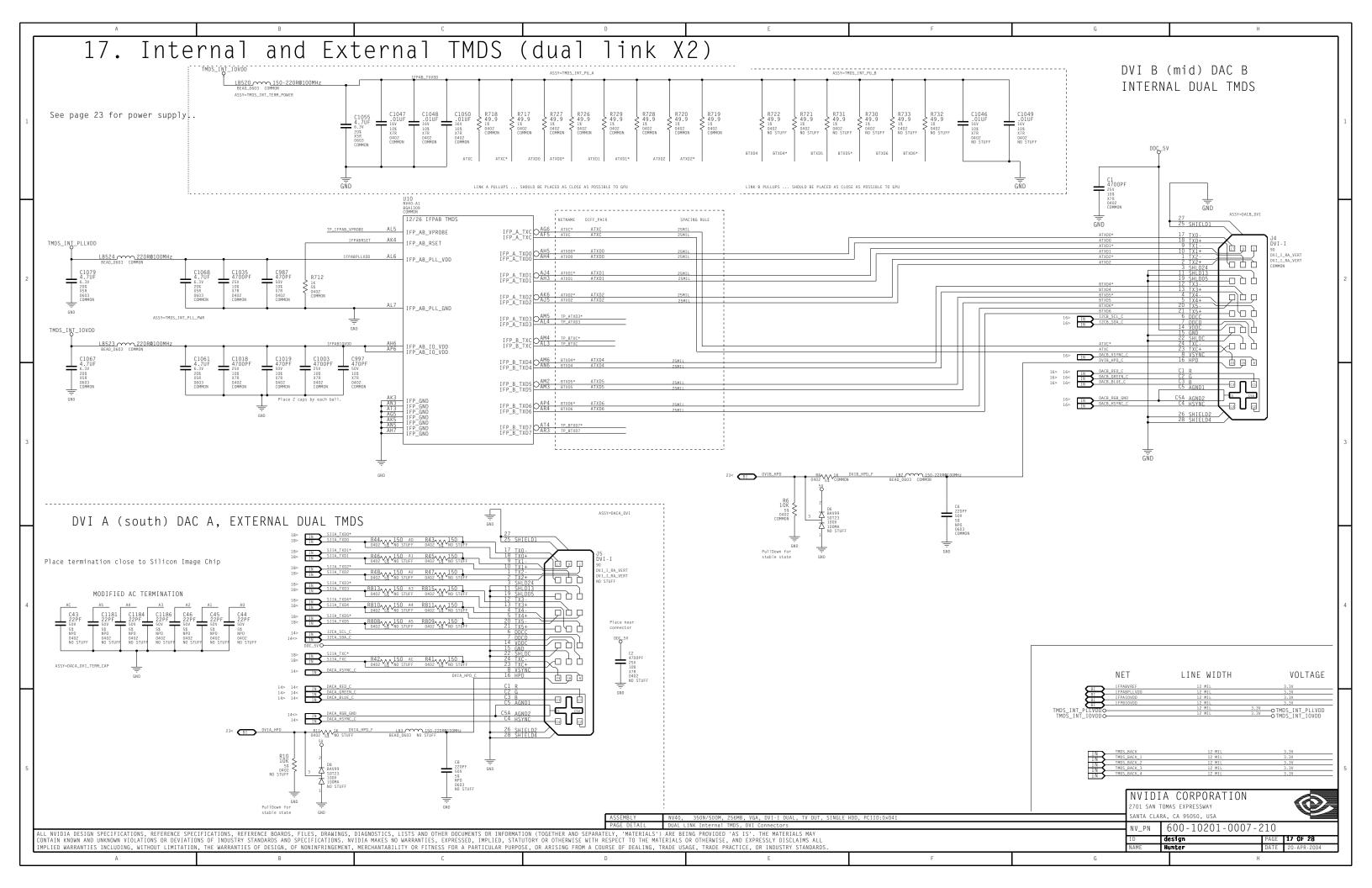


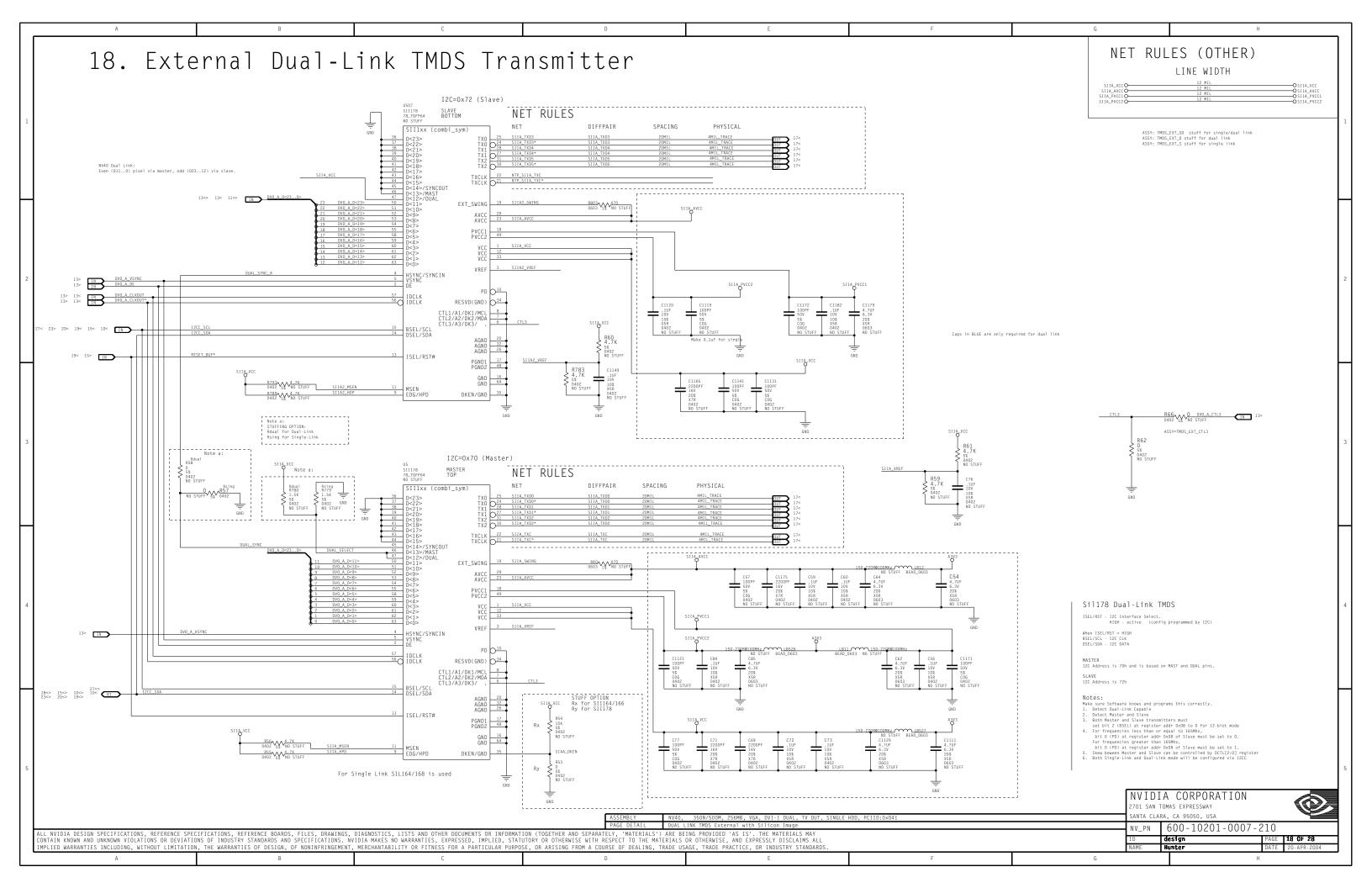


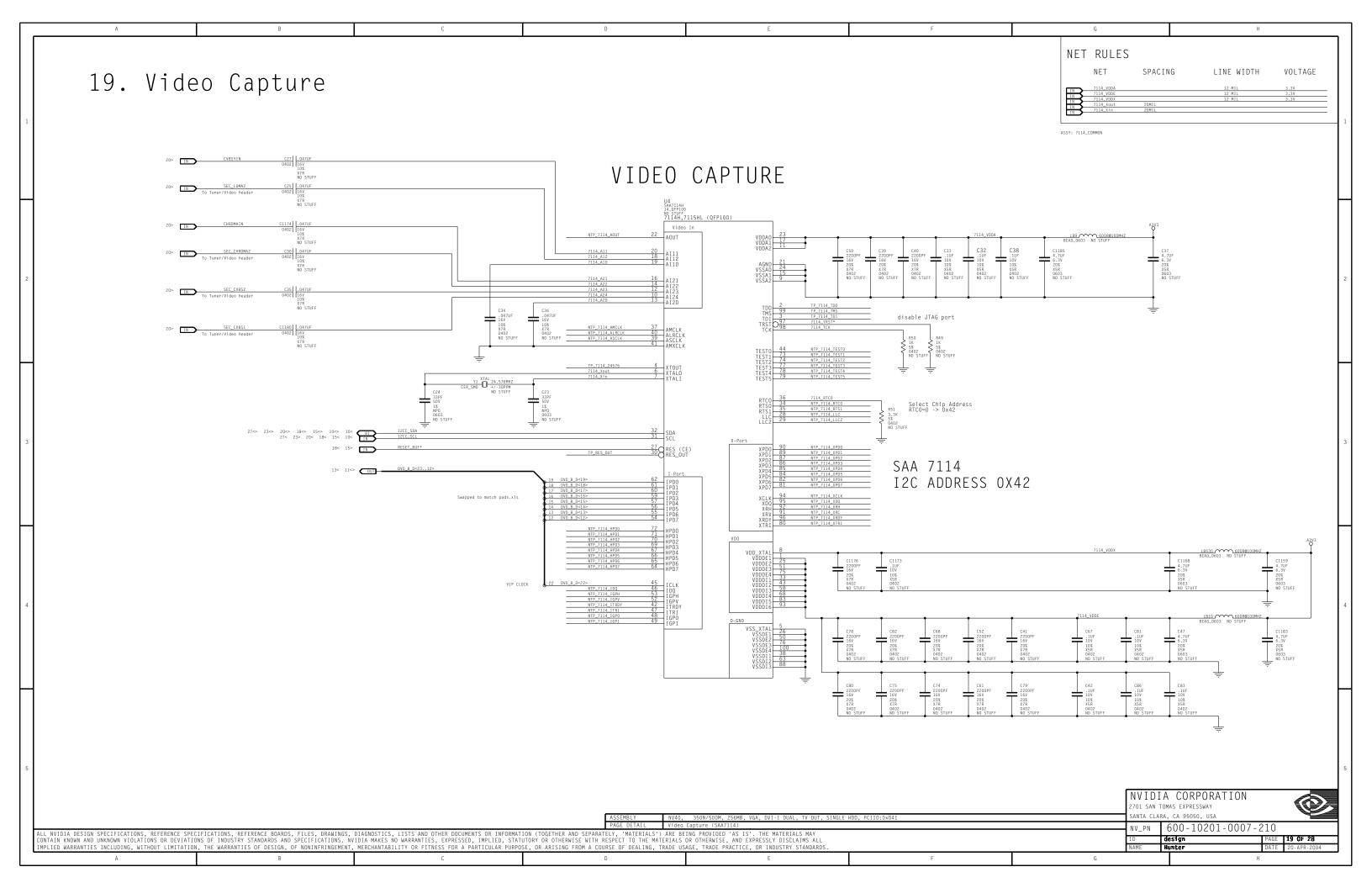


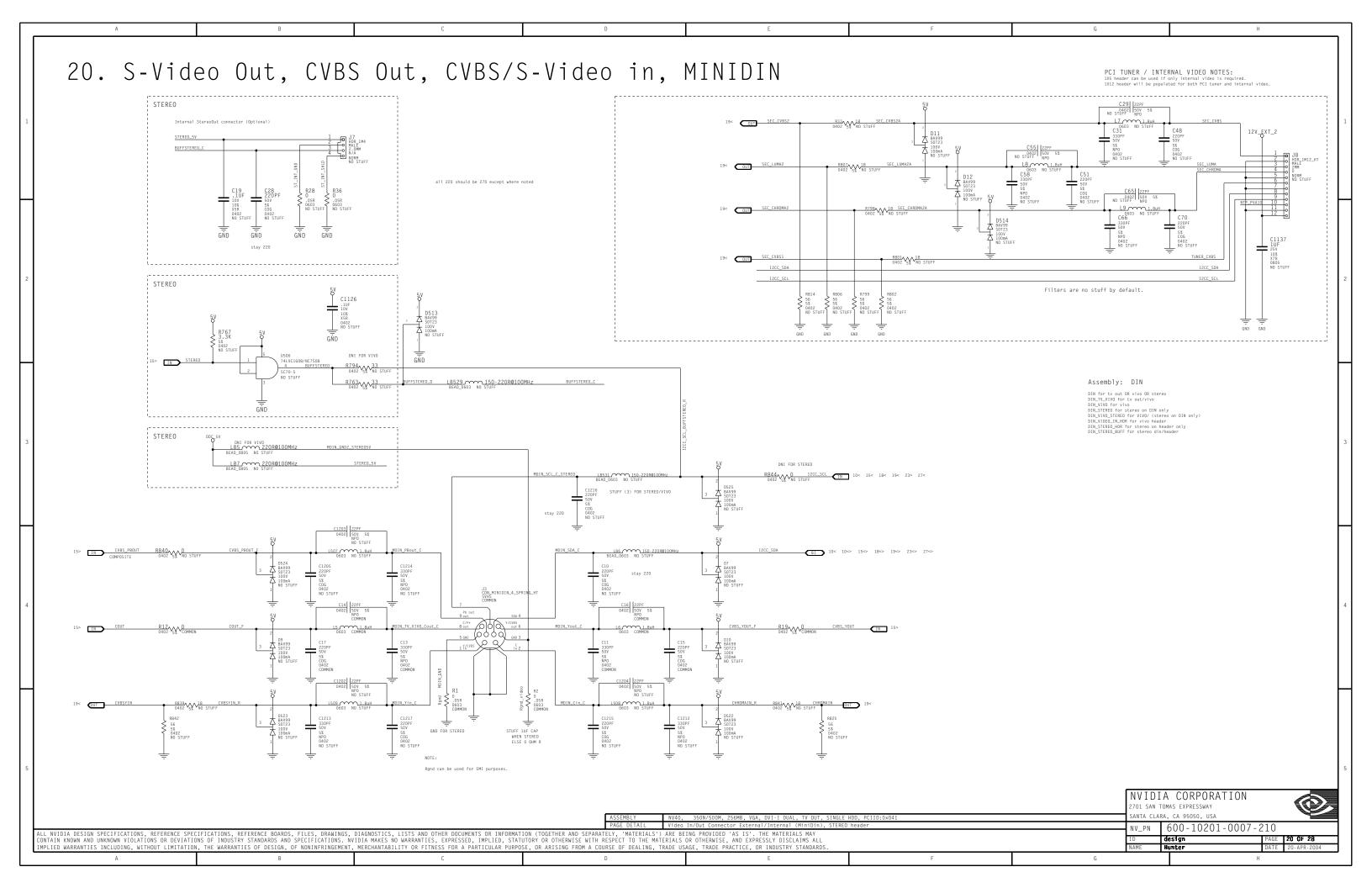




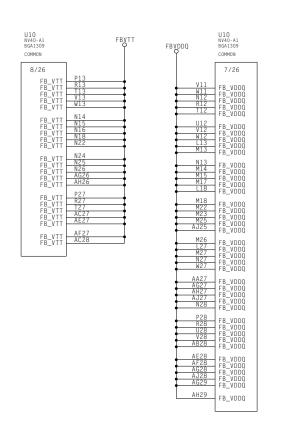


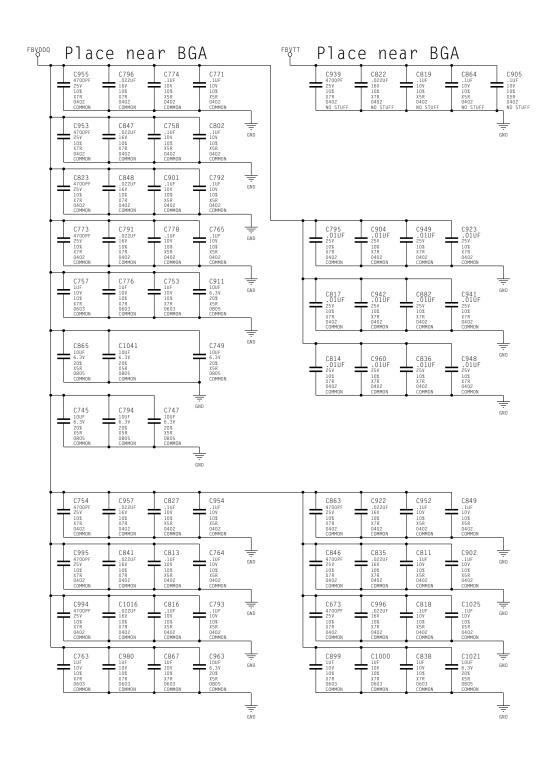


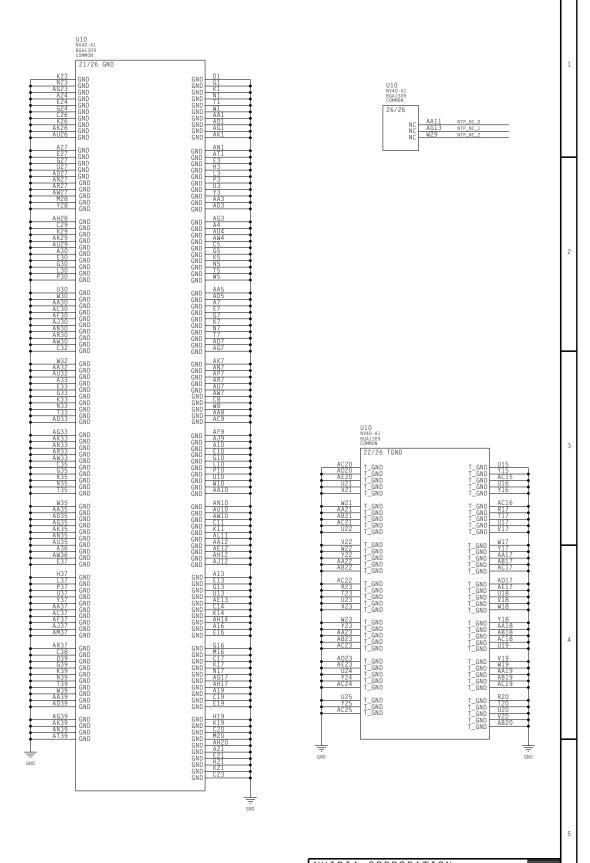




21. FBVTT AND FBVDDQ DECOUPLING, AND Misc...





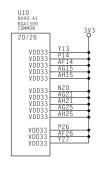


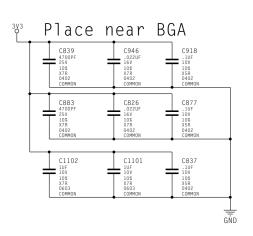
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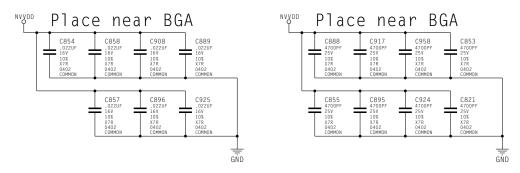
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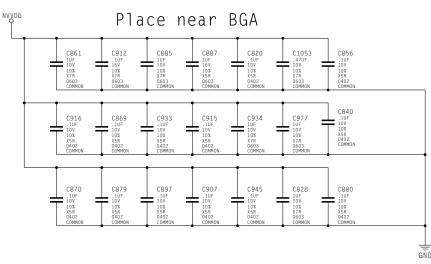
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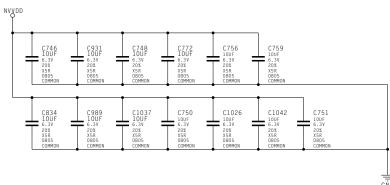
22. VDD AND NVVDD DECOUPLING

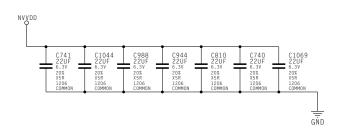












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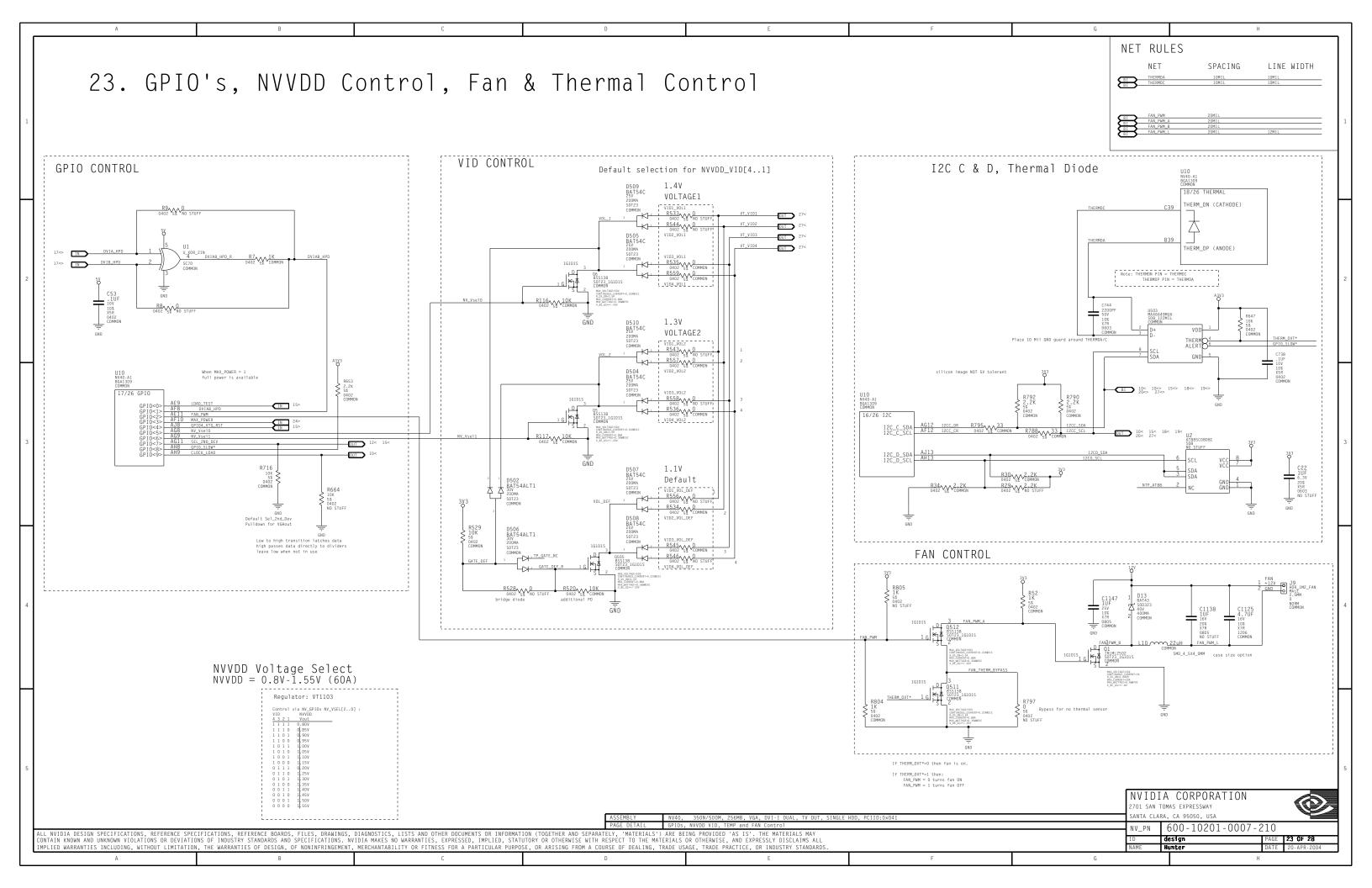
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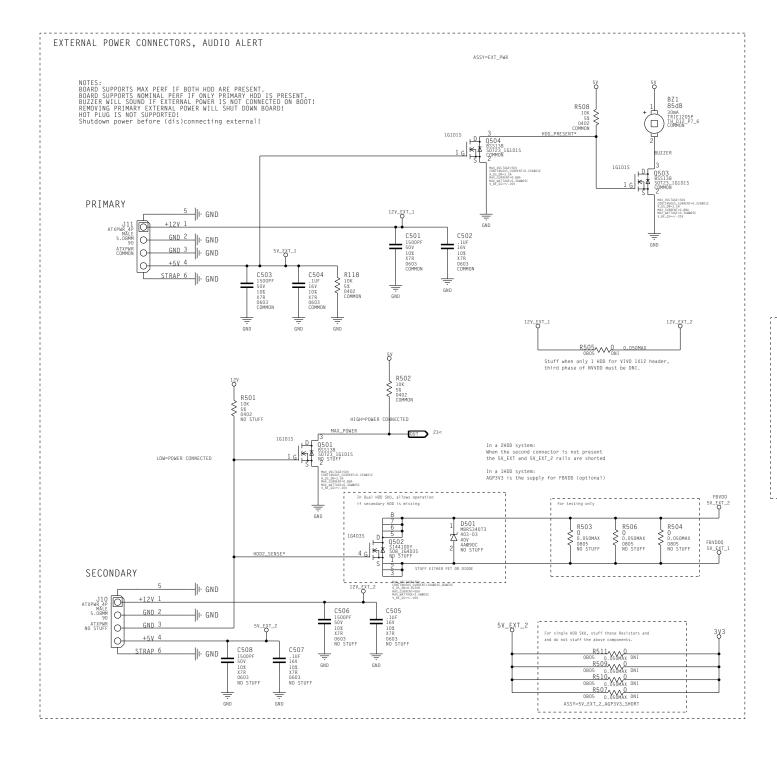
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PAGE | 22 OF 28

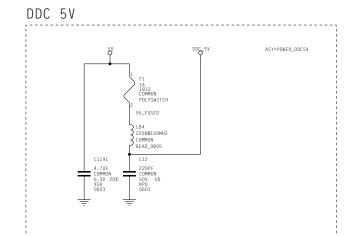


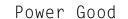




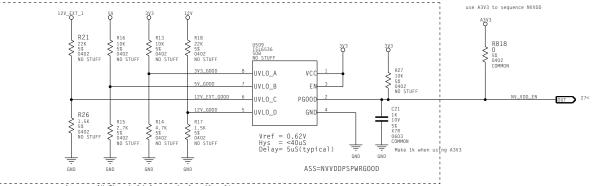


LINE WIDTH NET VOLTAGE





POWER_DDC5V



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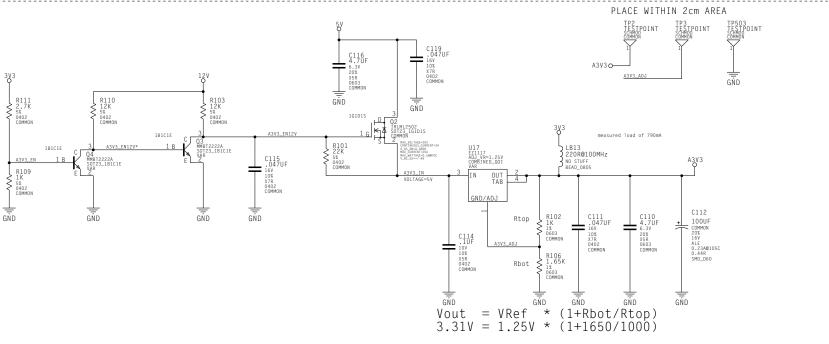
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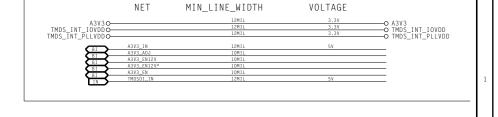
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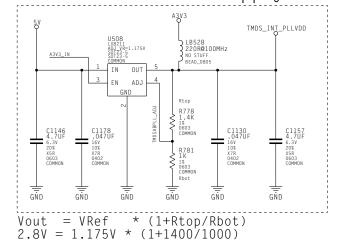




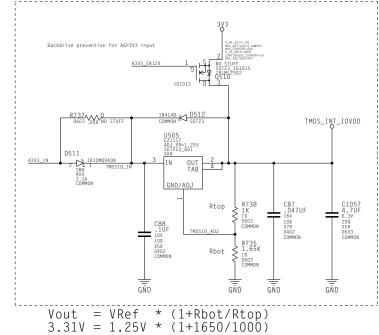




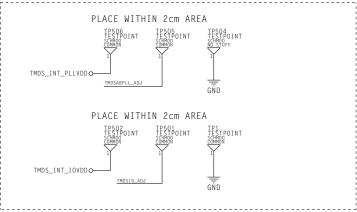
TMDS Internal PLL Supply



TMDS Internal IO Supply



SHM00 Testpoints TMDS



TMDS power sequencing done by using A3V3_IN.

	ASSEMBLY	NV40, 350N/500M, 256MB, VGA, DVI-I DUAL, TV OUT, SINGLE HDD, PCIID:0x041	_
	PAGE DETAIL	A3V3, TMDS IO POWER SUPPLIES	Ξ
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