P897 - GT200/NVIO2

P897, GT200-100, 896MB/1792MB - GDDR3 BGA136 16M/32Mx32

DVI-I + DVI-I + HD/SD/TVout, SPDIF, Dual SLI

Table of Contents

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10897-BASE-B01	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0053	600-10897-0053-300	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
2	SKU0054	600-10897-0054-300	DT, GT200-103-B3, 640/1440/1200, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
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4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Title Page

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Block Diagram

Power Sequence

5V	- Always On	
3V3	- Always On	
12V_F	- Always On	
12V_PEX6_F1	- Always On	
12V_PEX6_F2	- Always On	
FBVDD/FBVDDQ	- NVVDD Enabled	
NVVDD	- Input_PEX_Enable	+ Therm Shutdown Latch
2V5	-	
1V15	-	

SPDIF

2x3 Pwr

2x3 Pwr

Dual SLI

Power Supply
FBVDD/FBVDDQ Combined

Power Supply
5V Linear

TV

DVI-I

NVIO2

DVI-I

Power Supply
1V15 (pex,gv)

Power Supply
2V5

MEM F

MEM G

MEM H (N/A)

MEM E

MEM D

MEM C

MEM B

MEM A

GT200

Hybrid

Power Filter
12V_F

Power Supply
NVVDD-PH1

Power Supply
NVVDD-PH2

Power Supply
NVVDD-PH3

Power Supply
NVVDD-PH4

Power Supply
NVVDD-PH5

Power Supply
NVVDD-PH6

Power Supply
NVVDD-Controller

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Block Diagram

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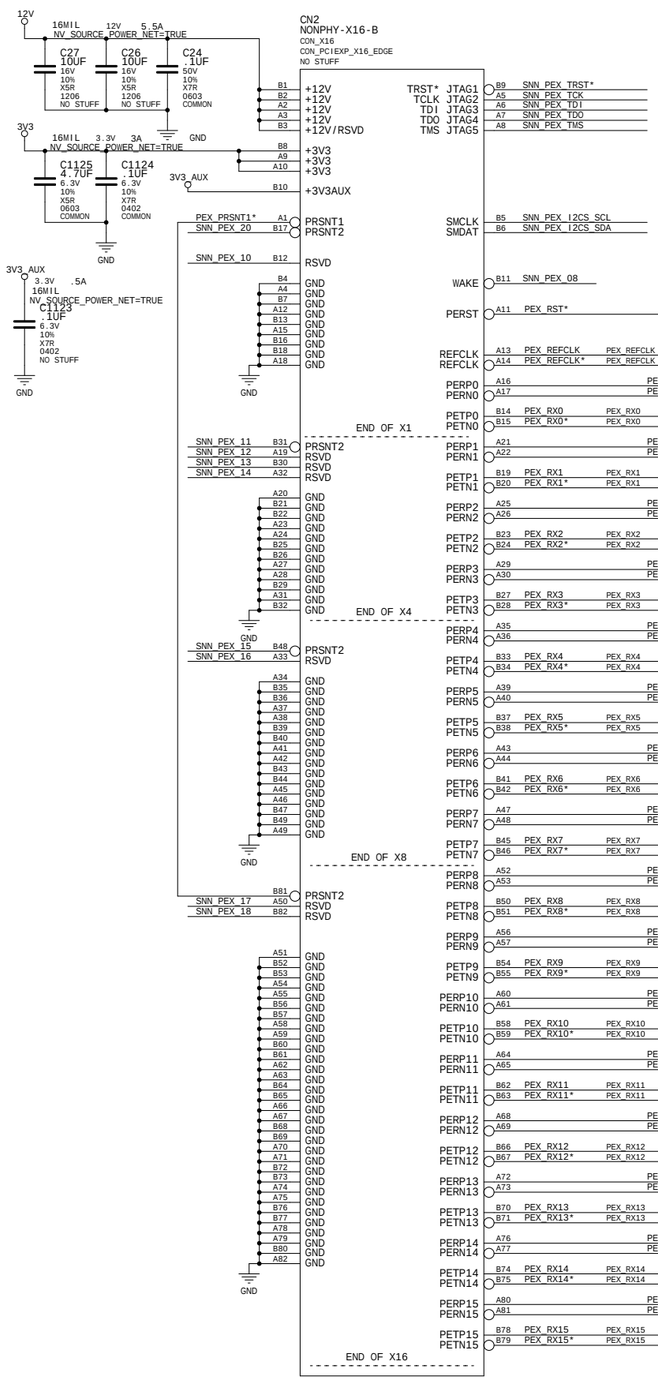
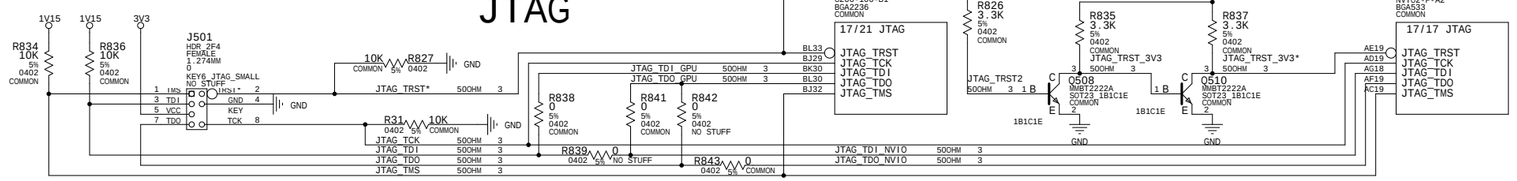
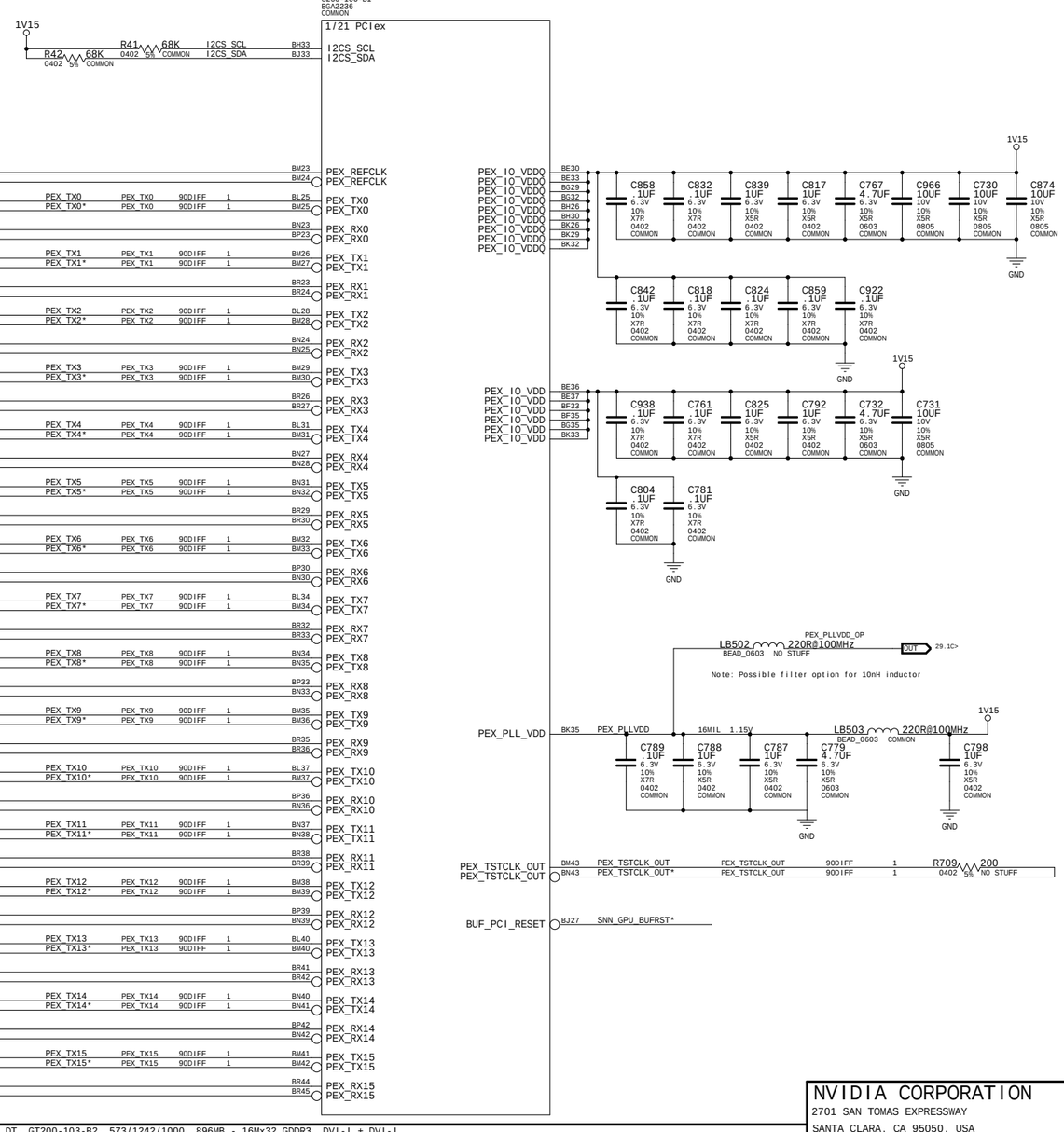
PCI Express / JTAG



JTAG





ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	PCI Express / JTAG

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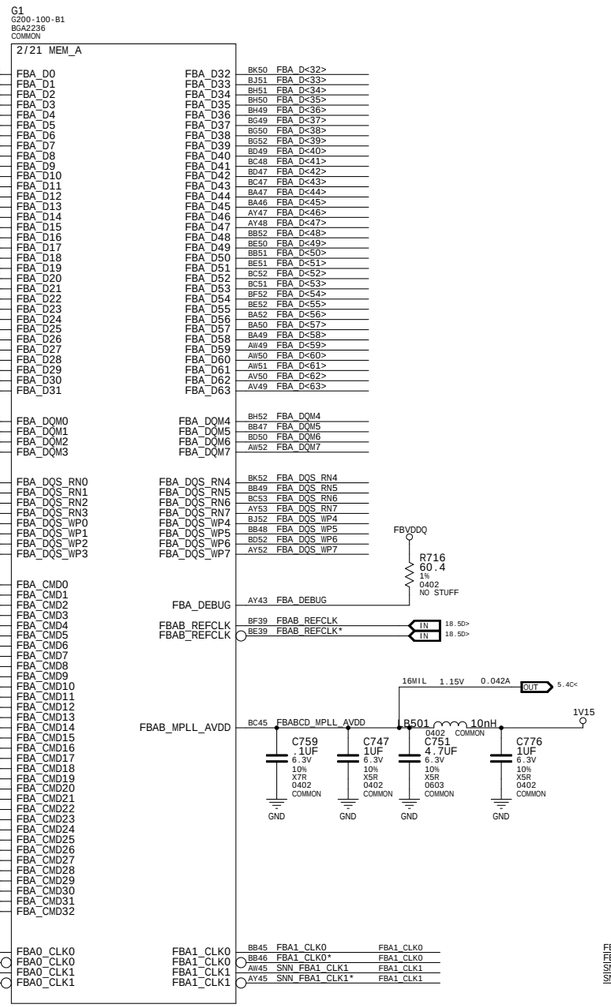
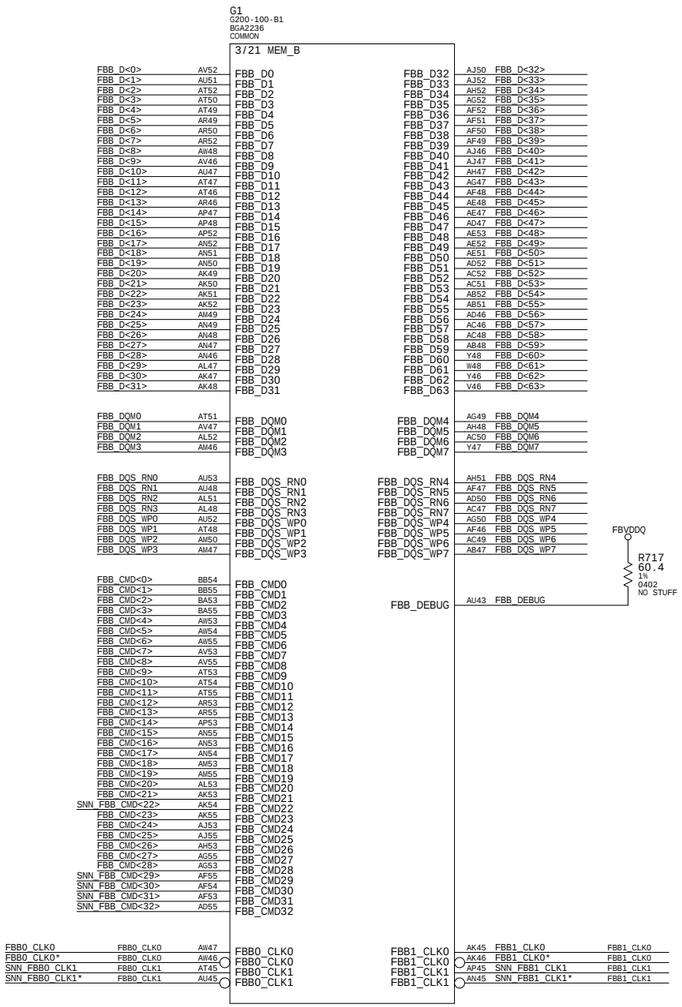
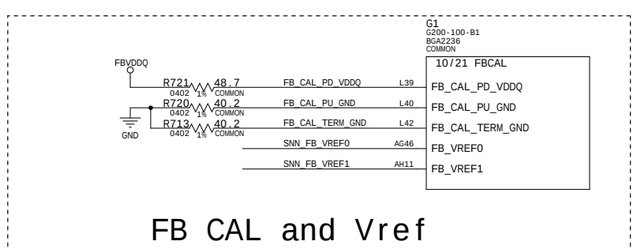
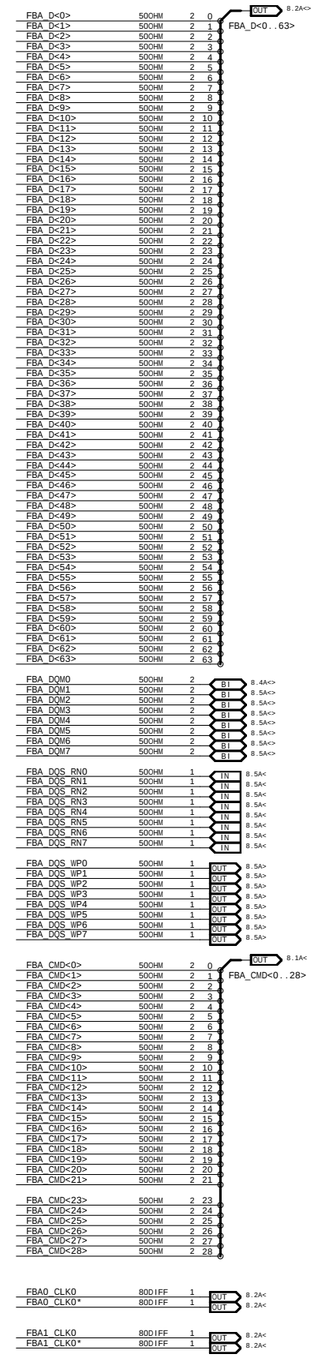
Framebuffer A,B: GPU Section + Calibration

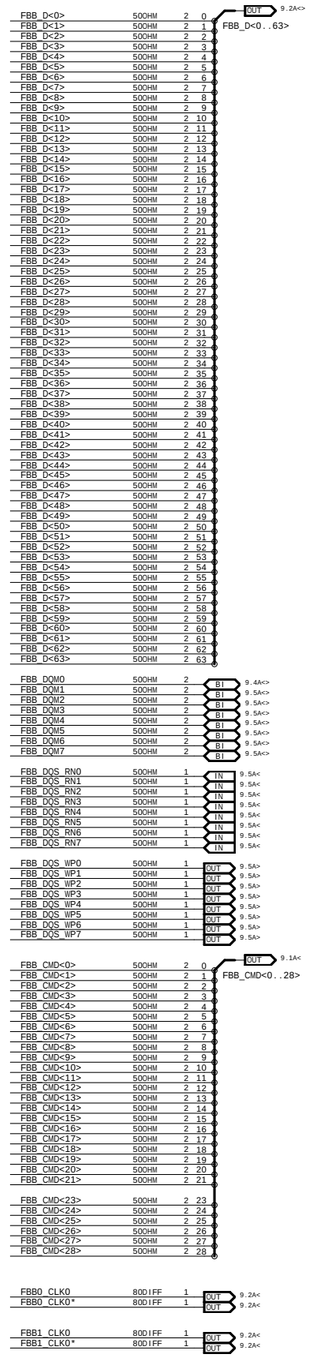






FB CAL and Vref





ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer A,B: GPU Section + Calibration

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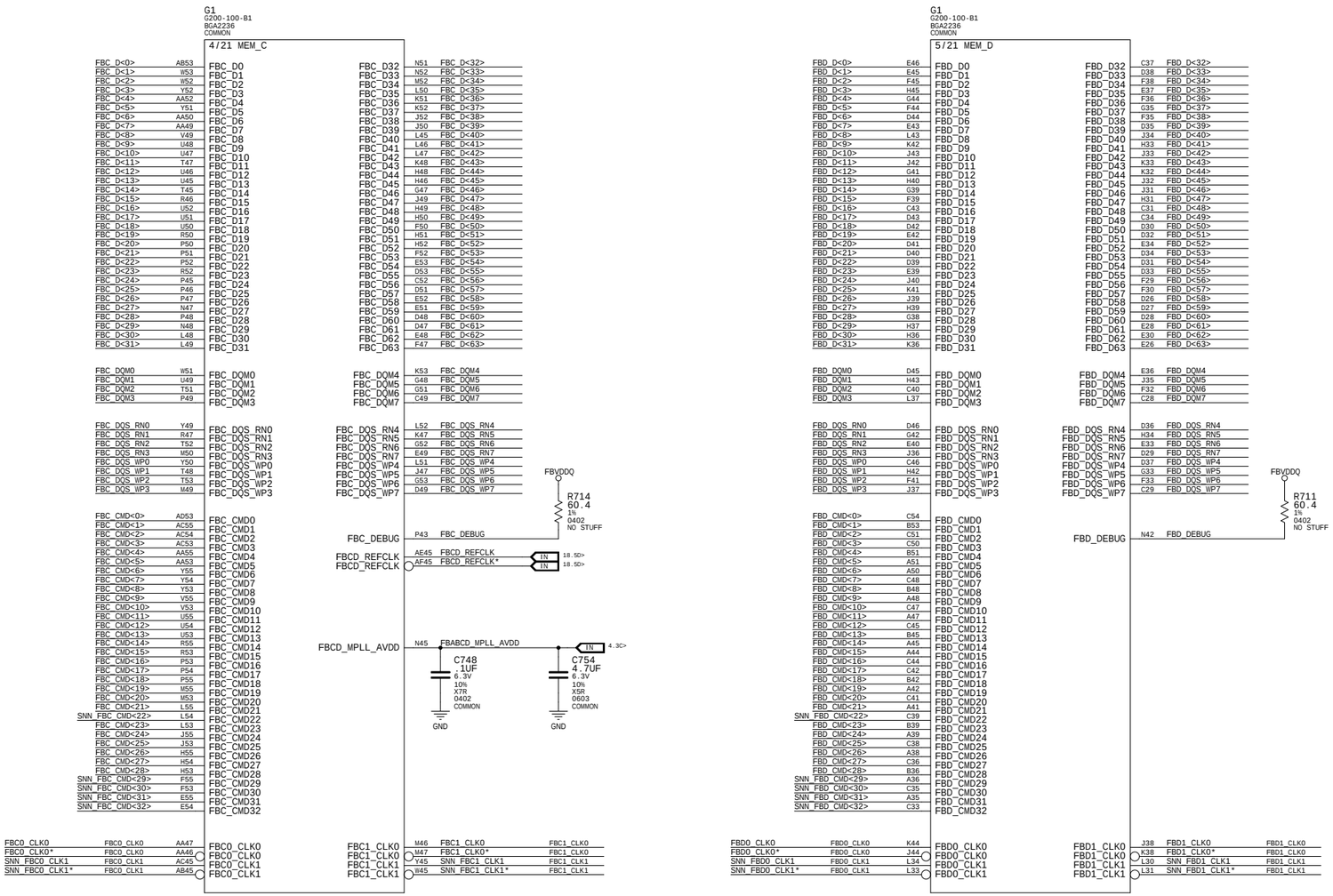
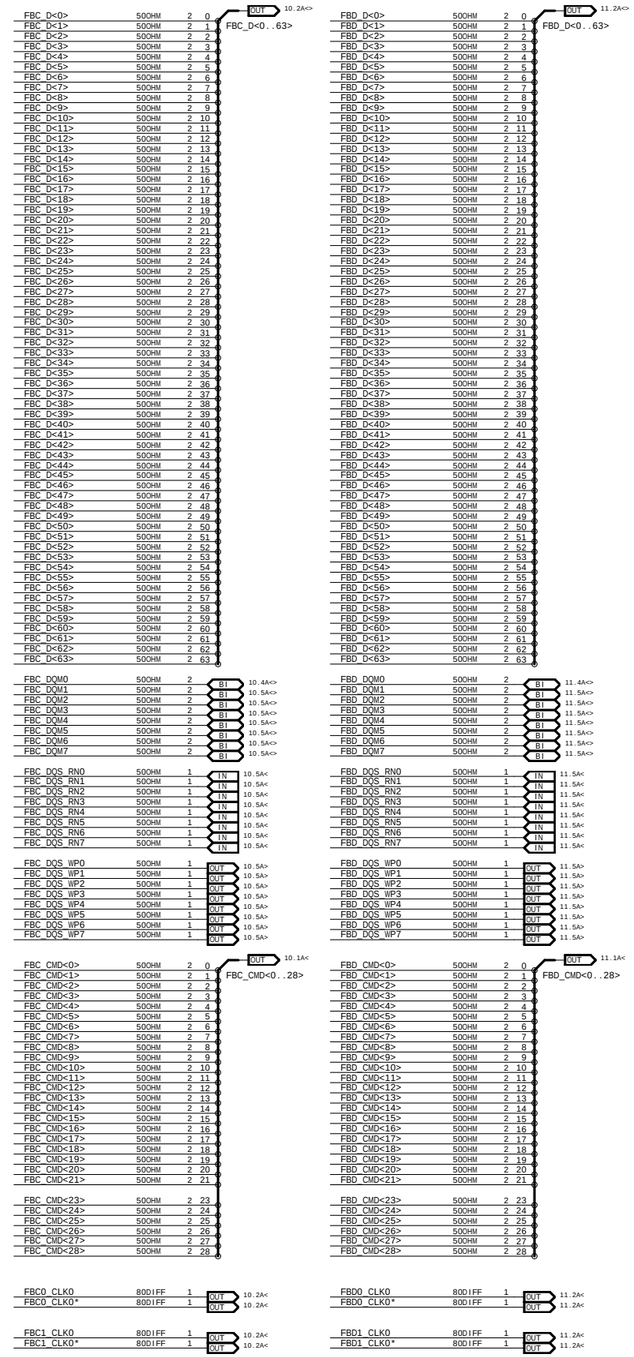
Framebuffer C,D: GPU Section





ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer C,D: GPU Section

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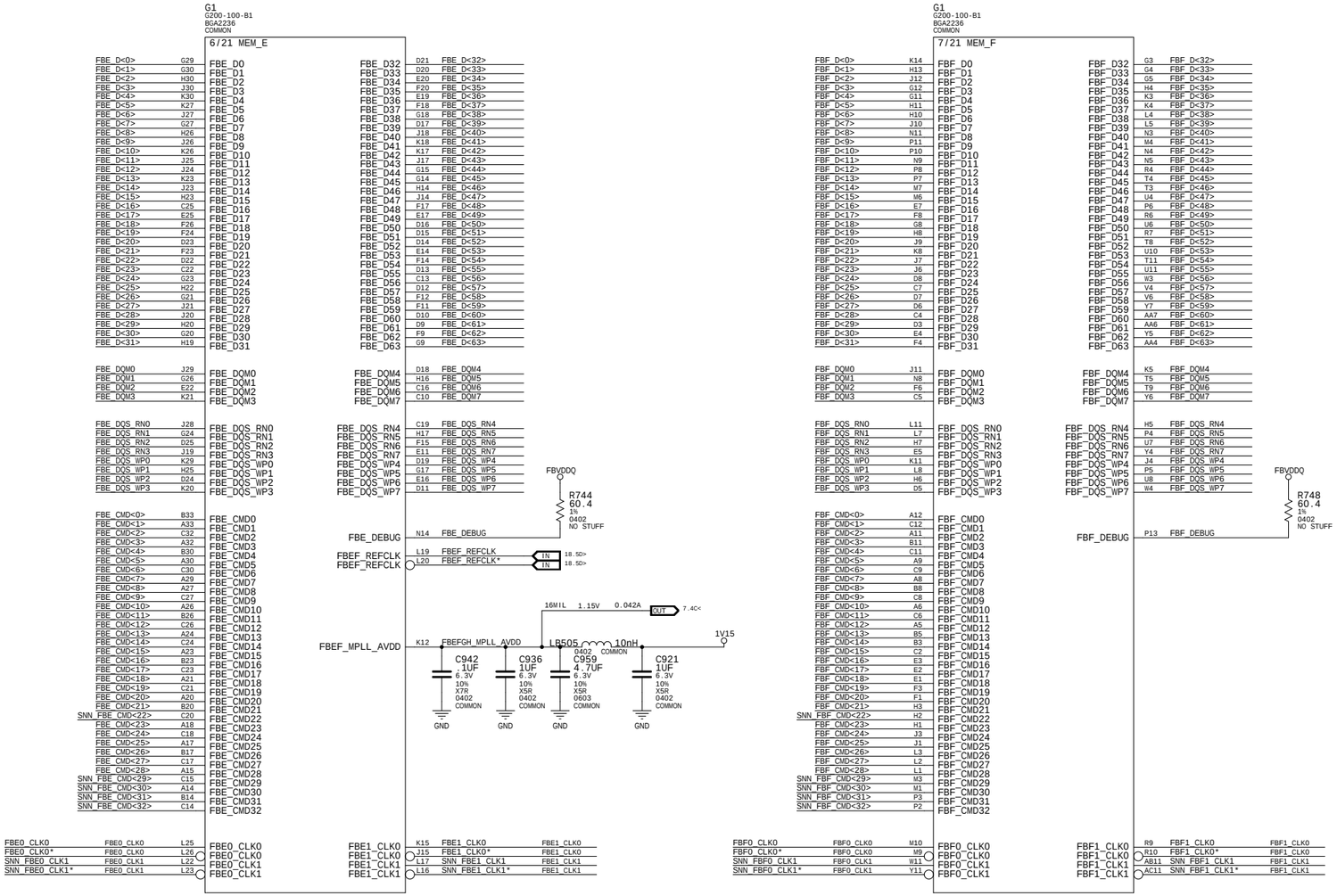
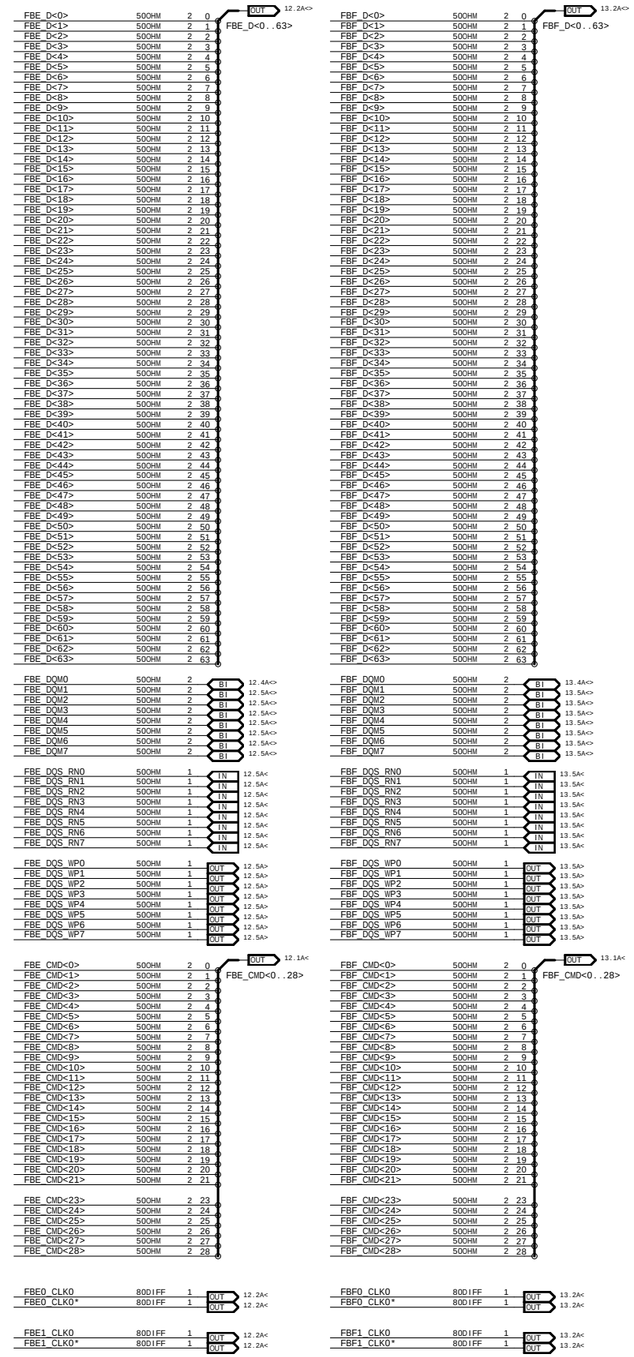
Framebuffer E,F: GPU Section





ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer E,F: GPU Section

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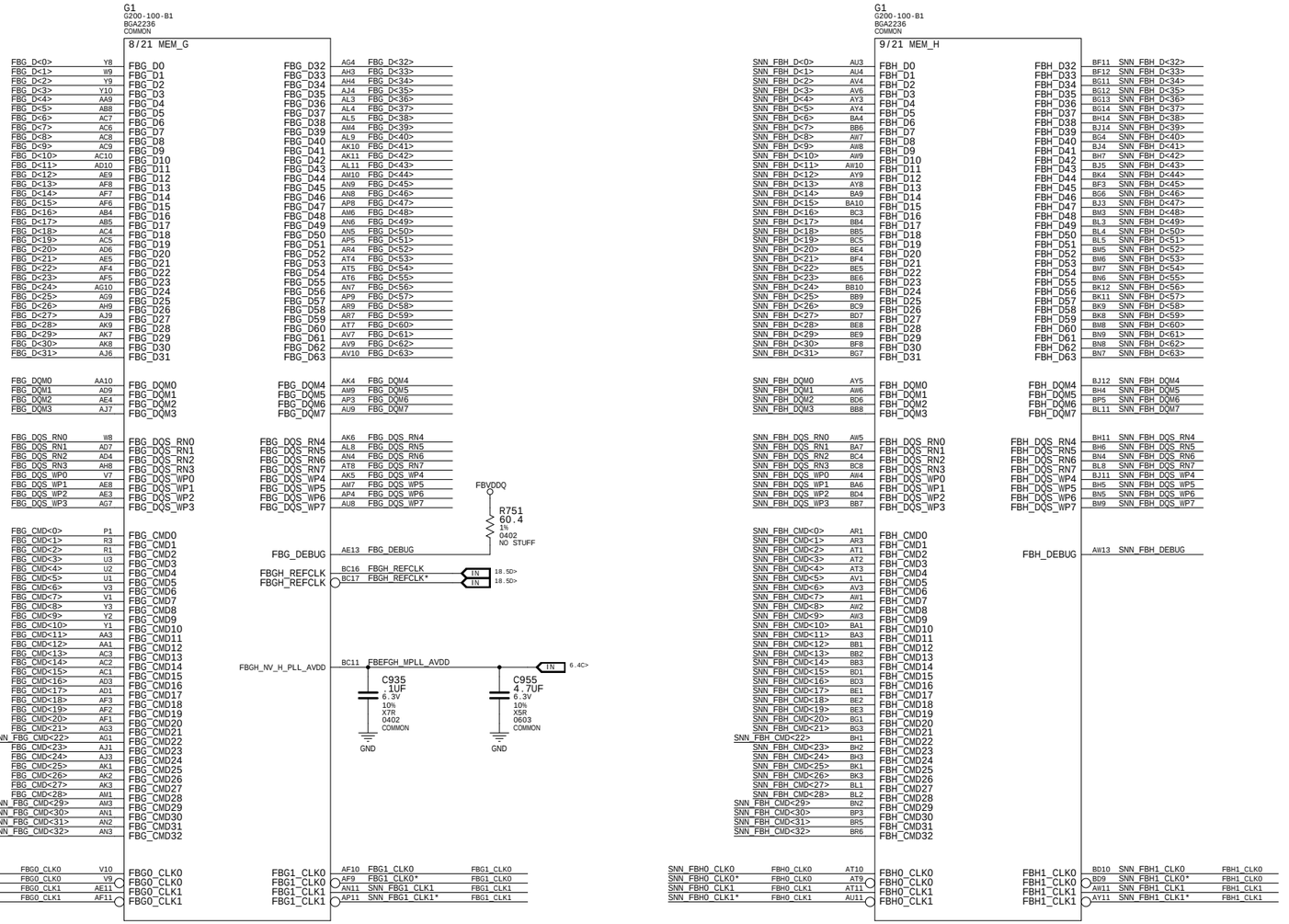
Framebuffer G,H: GPU Section



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer G,H: GPU Section

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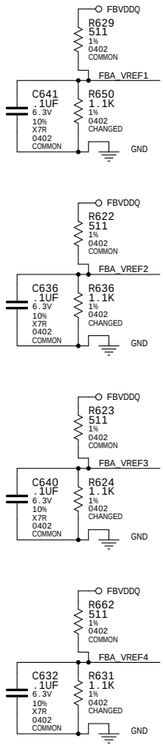
Framebuffer A: Memory Section

VREF = 68% FBVDDQ for Samsung memoey

VREF = 72% FBVDDQ for Hynix memoey



TERMINATION SELECT

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer A: Memory Section

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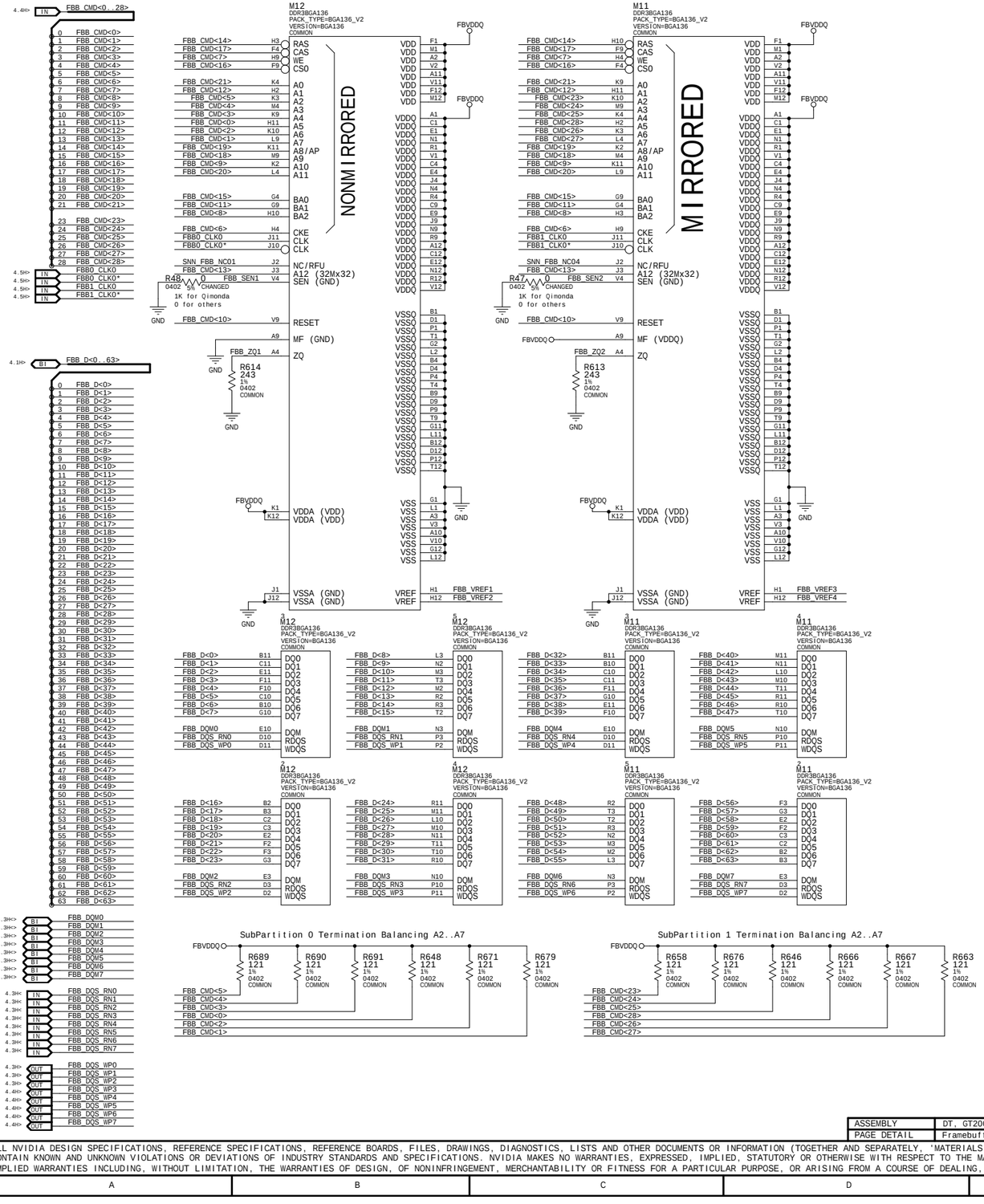
Framebuffer B: Memory Section



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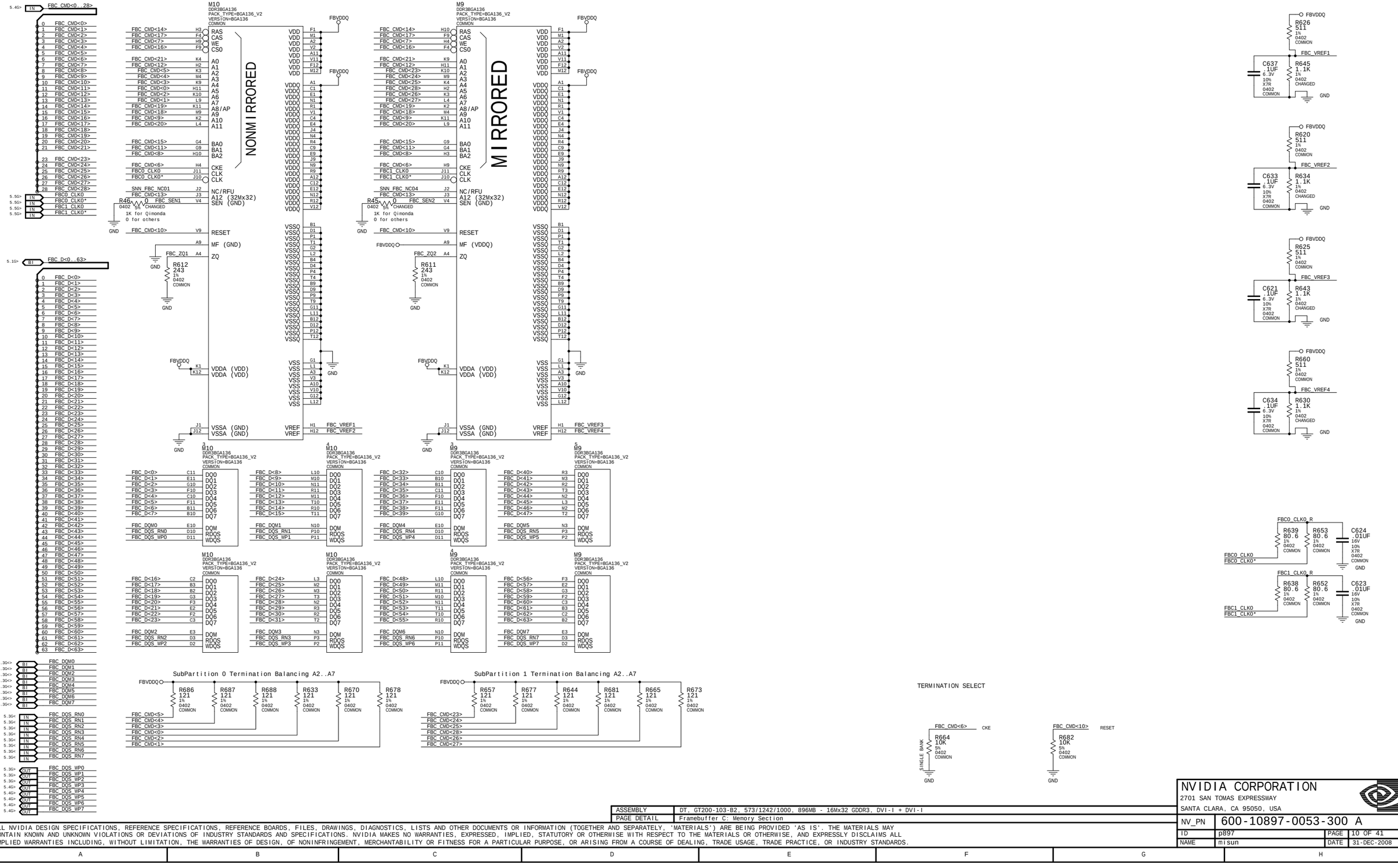
Framebuffer C: Memory Section



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer C: Memory Section

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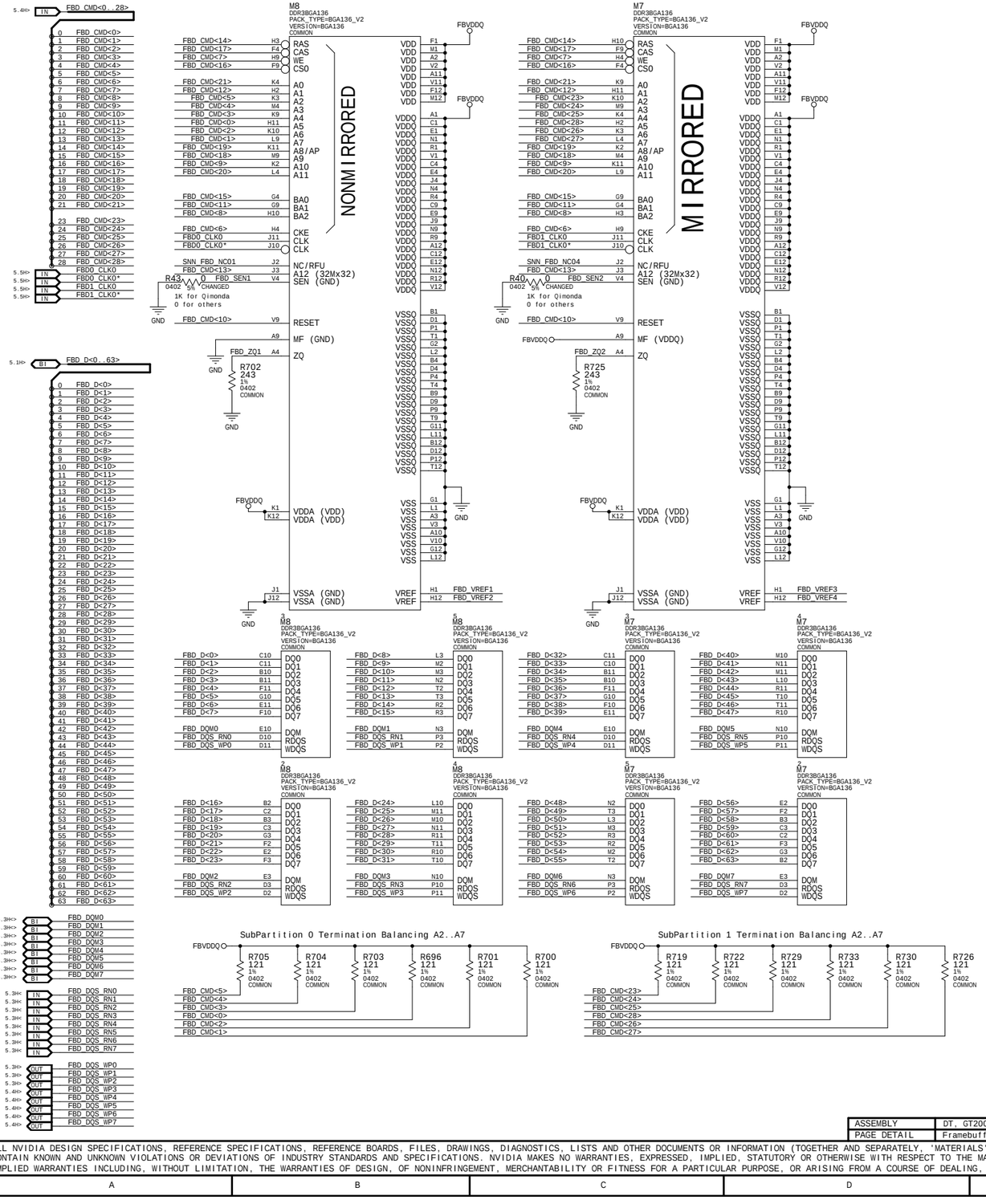
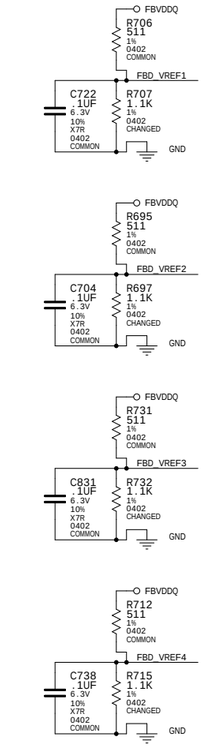
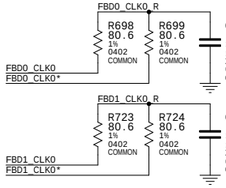
Framebuffer D: Memory Section







ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer D: Memory Section

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Framebuffer E: Memory Section

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer E: Memory Section

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Framebuffer F: Memory Section

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer F: Memory Section

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Framebuffer G: Memory Section

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Framebuffer G: Memory Section

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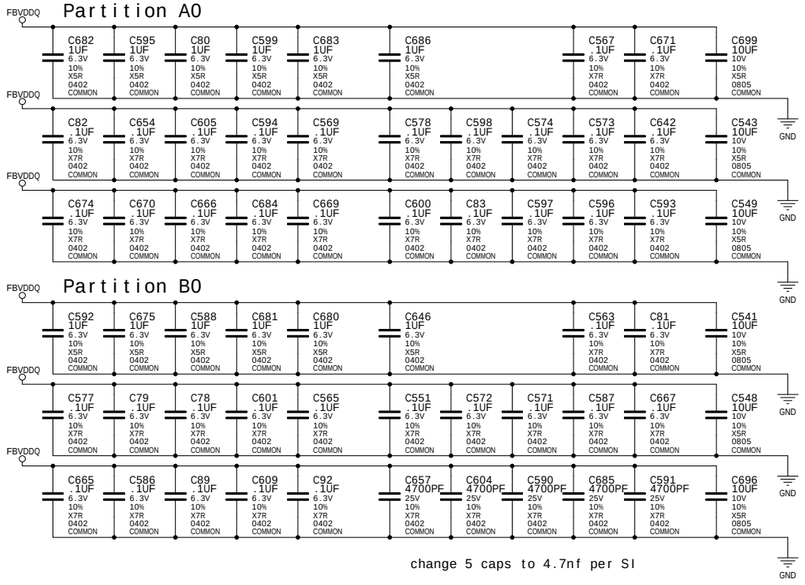
Decoupling: Memory Section A-D

Banks A-D FBVDD/Q
Combined Distributed Capacitance
280 uF

Decoupling for FBVDDQ

Partition A0

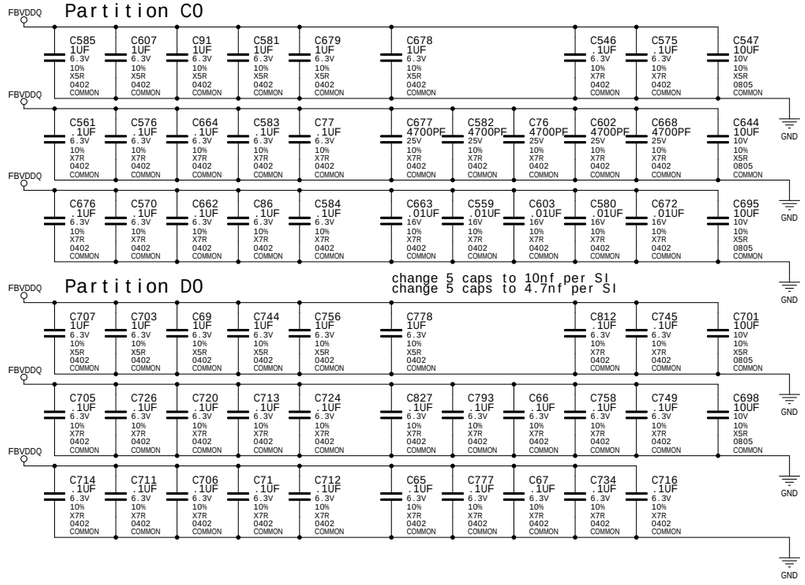


Partition B0

change 5 caps to 4.7nf per SI

GND

Partition C0

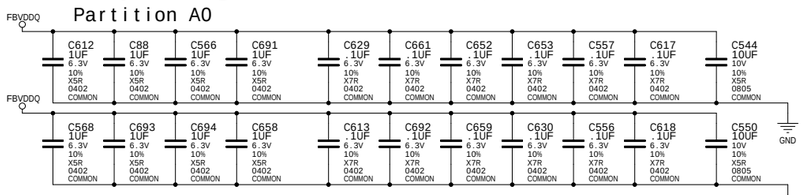


Partition D0

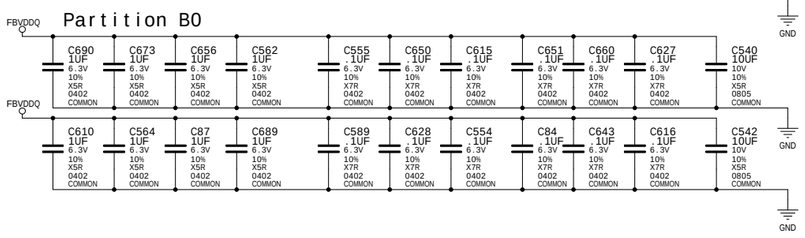
change 5 caps to 10nf per SI
change 5 caps to 4.7nf per SI

Decoupling for FBVDDQ

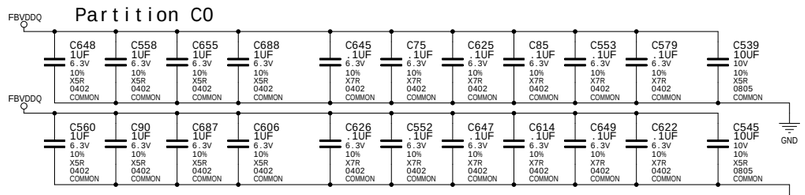
Partition A0



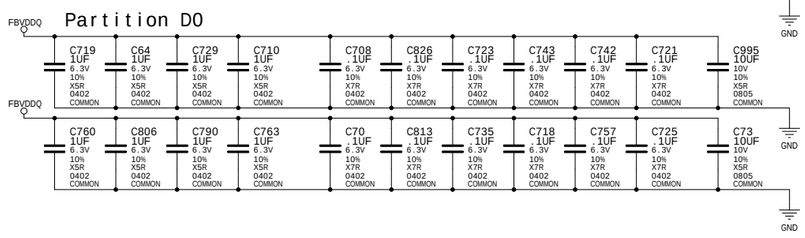
Partition B0



Partition C0



Partition D0



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Decoupling: Memory Section A-D

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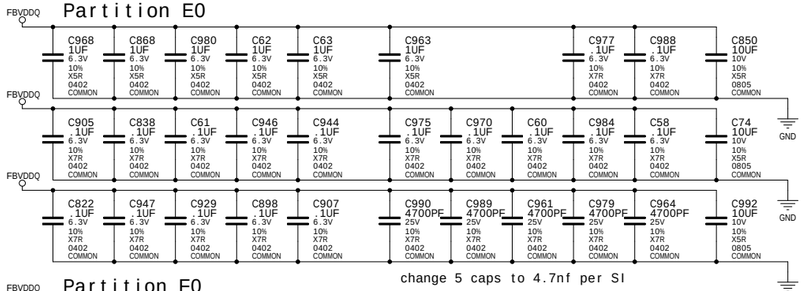
Decoupling: Memory Section E-G

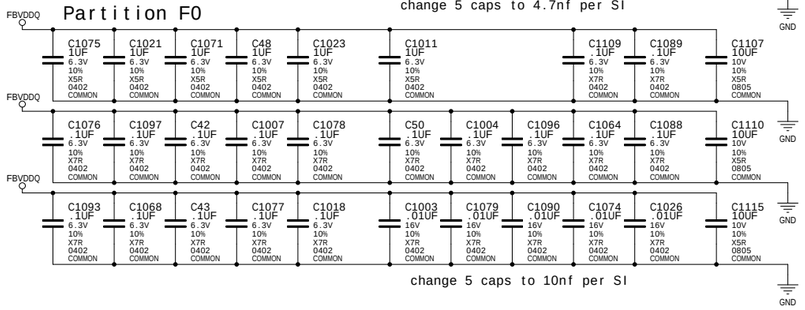
Banks E-G FBVDD/Q
Combined Distributed Capacitance
210 uF

Decoupling for FBVDDQ

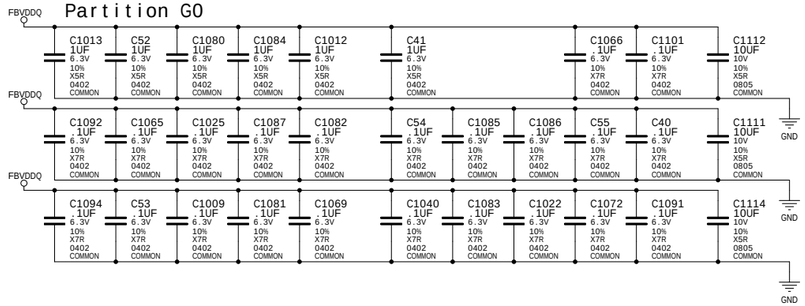
Partition E0



Partition F0

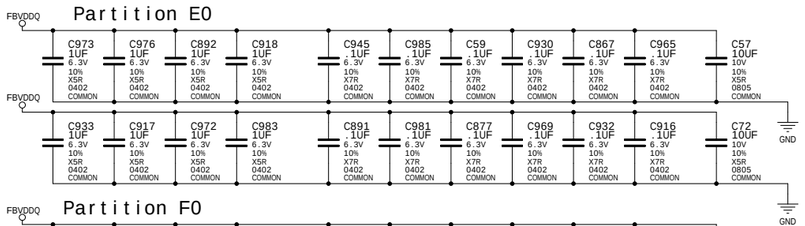


Partition G0

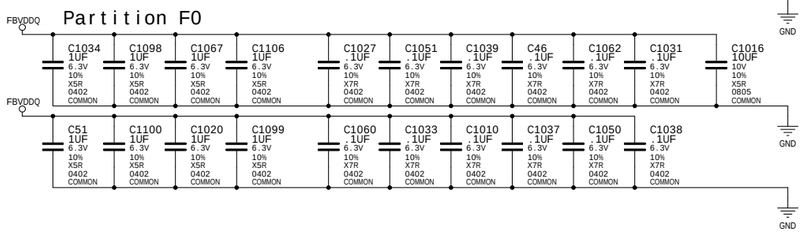


Decoupling for FBVDDQ

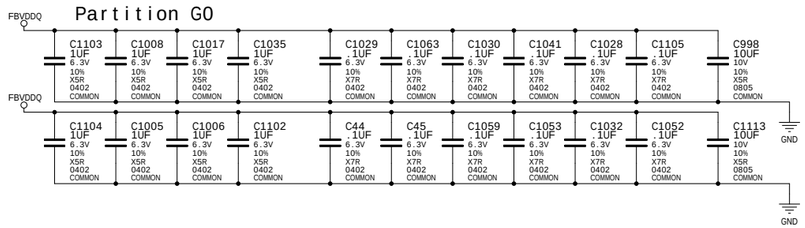
Partition E0



Partition F0



Partition G0



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Decoupling: Memory Section E-G

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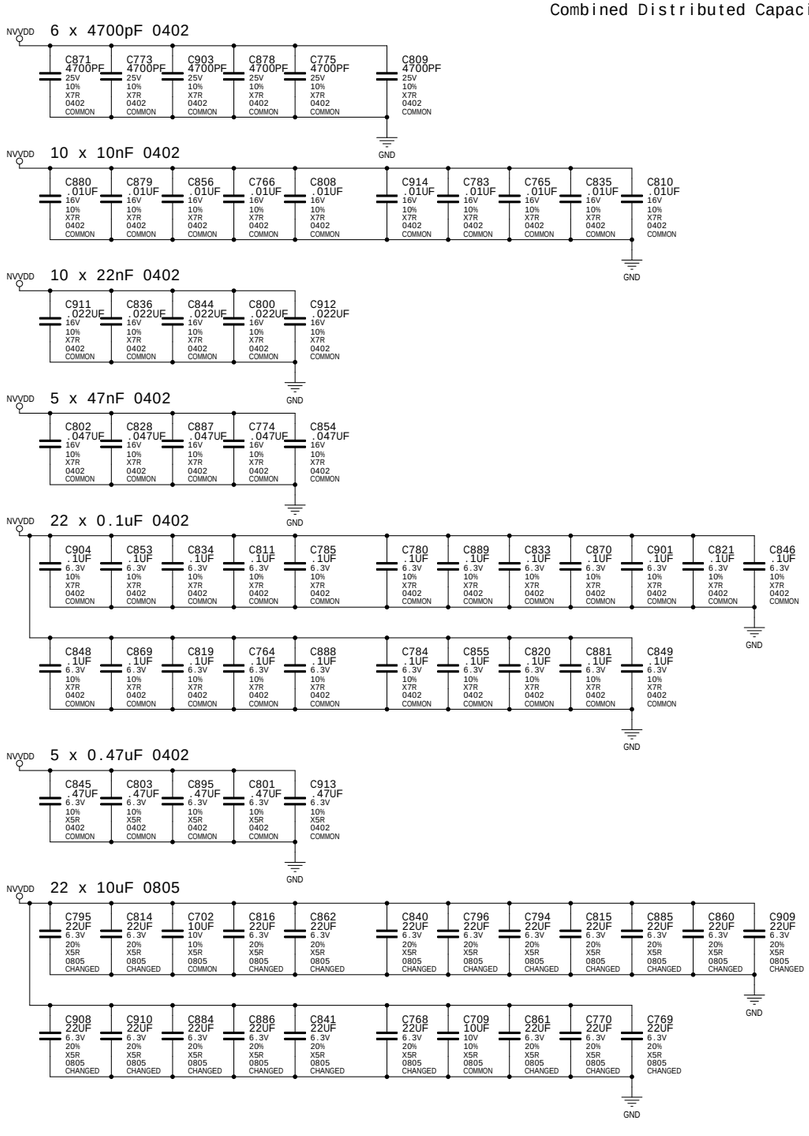
Decoupling: GPU (NVVDD, FBVDDQ)

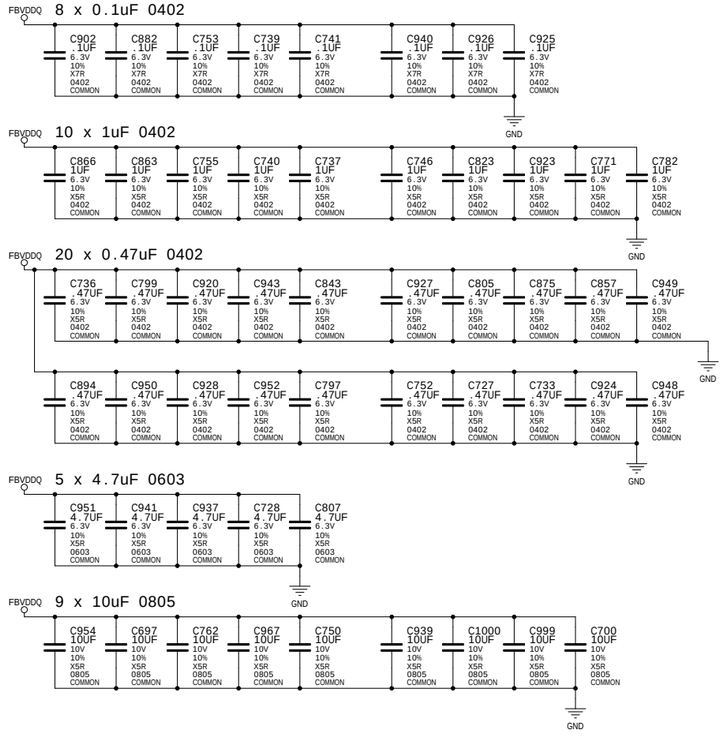
Decoupling for NVVDD (under GPU)

GPU - NVVDD
Combined Distributed Capacitance



Decoupling for FBVDDQ (under GPU)

GPU - FBVDD/Q
Combined Distributed Capacitance
230 uF



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Decoupling: GPU (NVVDD, FBVDDQ)

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10897-0053-300 A		
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GPU-NVIO Interconnect: GV Bus / PLL

G1
G200-100-B1
BGA2236
COMMON

12/21 GV Bus

U2
NV102-P-A2
BGA533
COMMON

1/17 GV-INTERFACE

GV_TX0	BK24	GV_TX0	GV_TX0	90DIFF	1	AG22	GV_RX0
GV_TX0	BJ24	GV_TX0*	GV_TX0	90DIFF	1	AG21	GV_RX0
GV_TX1	BJ23	GV_TX1	GV_TX1	90DIFF	1	AG25	GV_RX1
GV_TX1	BK23	GV_TX1*	GV_TX1	90DIFF	1	AG24	GV_RX1
GV_TX2	BL22	GV_TX2	GV_TX2	90DIFF	1	AF23	GV_RX2
GV_TX2	BM22	GV_TX2*	GV_TX2	90DIFF	1	AF22	GV_RX2
GV_TX3	BK21	GV_TX3	GV_TX3	90DIFF	1	AD21	GV_RX3
GV_TX3	BJ21	GV_TX3*	GV_TX3	90DIFF	1	AD20	GV_RX3
GV_TX4	BM20	GV_TX4	GV_TX4	90DIFF	1	AG26	GV_RX4
GV_TX4	BN21	GV_TX4*	GV_TX4	90DIFF	1	AF26	GV_RX4
GV_TX5	BK20	GV_TX5	GV_TX5	90DIFF	1	AE27	GV_RX5
GV_TX5	BL20	GV_TX5*	GV_TX5	90DIFF	1	AF27	GV_RX5
GV_TX6	BN21	GV_TX6	GV_TX6	90DIFF	1	AE24	GV_RX6
GV_TX6	BN20	GV_TX6*	GV_TX6	90DIFF	1	AE25	GV_RX6
GV_TX7	BR20	GV_TX7	GV_TX7	90DIFF	1	AD23	GV_RX7
GV_TX7	BR21	GV_TX7*	GV_TX7	90DIFF	1	AD22	GV_RX7
GV_TX8	BL19	GV_TX8	GV_TX8	90DIFF	1	AE21	GV_RX8
GV_TX8	BM19	GV_TX8*	GV_TX8	90DIFF	1	AE22	GV_RX8
GV_TX9	BN19	GV_TX9	GV_TX9	90DIFF	1	AD25	GV_RX9
GV_TX9	BP20	GV_TX9*	GV_TX9	90DIFF	1	AD24	GV_RX9
GV_TX10	BM17	GV_TX10	GV_TX10	90DIFF	1	AD26	GV_RX10
GV_TX10	BM18	GV_TX10*	GV_TX10	90DIFF	1	AC26	GV_RX10
GV_TX11	BR17	GV_TX11	GV_TX11	90DIFF	1	AA27	GV_RX11
GV_TX11	BR18	GV_TX11*	GV_TX11	90DIFF	1	AB27	GV_RX11
GV_TX12	BN17	GV_TX12	GV_TX12	90DIFF	1	AB24	GV_RX12
GV_TX12	BN18	GV_TX12*	GV_TX12	90DIFF	1	AB25	GV_RX12
GV_TX13	BN16	GV_TX13	GV_TX13	90DIFF	1	AA23	GV_RX13
GV_TX13	BP17	GV_TX13*	GV_TX13	90DIFF	1	AA22	GV_RX13
GV_TX14	BM14	GV_TX14	GV_TX14	90DIFF	1	AA26	GV_RX14
GV_TX14	BM15	GV_TX14*	GV_TX14	90DIFF	1	Y26	GV_RX14
GV_TX15	BN13	GV_TX15	GV_TX15	90DIFF	1	V27	GV_RX15
GV_TX15	BP14	GV_TX15*	GV_TX15	90DIFF	1	W27	GV_RX15
GV_TX16	BN14	GV_TX16	GV_TX16	90DIFF	1	W24	GV_RX16
GV_TX16	BN15	GV_TX16*	GV_TX16	90DIFF	1	W25	GV_RX16
GV_TX17	BR11	GV_TX17	GV_TX17	90DIFF	1	V23	GV_RX17
GV_TX17	BR12	GV_TX17*	GV_TX17	90DIFF	1	V22	GV_RX17
GV_TX18	BL13	GV_TX18	GV_TX18	90DIFF	1	W22	GV_RX18
GV_TX18	BM13	GV_TX18*	GV_TX18	90DIFF	1	W23	GV_RX18
GV_TX19	BN10	GV_TX19	GV_TX19	90DIFF	1	V25	GV_RX19
GV_TX19	BP11	GV_TX19*	GV_TX19	90DIFF	1	V24	GV_RX19
GV_TXCTL	BR14	GV_TXCTL	GV_TXCTL	90DIFF	1	AA25	GV_RXCTL
GV_TXCTL	BR15	GV_TXCTL*	GV_TXCTL	90DIFF	1	AA24	GV_RXCTL
GV_TXCLK	BL16	GV_TXCLK	GV_TXCLK	90DIFF	1	AB22	GV_RXCLK
GV_TXCLK	BM16	GV_TXCLK*	GV_TXCLK	90DIFF	1	AB23	GV_RXCLK

replace existing vias with labtestpoints

GV_RX0	BN11	GV_RX0	GV_RX0	90DIFF	1	T24	GV_TX0
GV_RX0	BN12	GV_RX0*	GV_RX0	90DIFF	1	T25	GV_TX0
GV_RX1	BK15	GV_RX1	GV_RX1	90DIFF	1	R23	GV_TX1
GV_RX1	BJ15	GV_RX1*	GV_RX1	90DIFF	1	R22	GV_TX1
GV_RX2	BL10	GV_RX2	GV_RX2	90DIFF	1	T22	GV_TX2
GV_RX2	BM10	GV_RX2*	GV_RX2	90DIFF	1	T23	GV_TX2
GV_RX3	BK14	GV_RX3	GV_RX3	90DIFF	1	R25	GV_TX3
GV_RX3	BL14	GV_RX3*	GV_RX3	90DIFF	1	R24	GV_TX3
GV_RXCTL	BK17	GV_RXCTL	GV_RXCTL	90DIFF	1	R27	GV_TXCTL
GV_RXCTL	BL17	GV_RXCTL*	GV_RXCTL	90DIFF	1	T27	GV_TXCTL
GV_RXCLK	BM11	GV_RXCLK	GV_RXCLK	90DIFF	1	V26	GV_TXCLK
GV_RXCLK	BM12	GV_RXCLK*	GV_RXCLK	90DIFF	1	U26	GV_TXCLK

replace existing vias with labtestpoints

PMC_ISO_RESET	BG26	GPU_PMC_ISO_RESET*	50OHM	1	N27	PMC_ISO_RESET
HOT_RESET	BK27	GPU_HOT_RESET*	50OHM	1	AB19	HOT_RESET
PEX_PWR_GOOD	BL26	GPU_PEX_PWR_GOOD*	50OHM	1	AF20	BUFRST
BUFCLK_LDT_IN	BJ26	GPU_BUFCLK_LDT_IN	50OHM	1	K25	XTAL_OUT_BUF

GPU_CLK	M26	GPU_CLK	GPU_CLK	90DIFF	1	BC20	NV_SS_REFCLK
GPU_CLK	L26	GPU_CLK*	GPU_CLK	90DIFF	1	BC19	NV_SS_REFCLK
FB_CLK0	N24	FBAB_REFCLK	FBAB_REFCLK	90DIFF	1	OUT	4.3<
FB_CLK0	N25	FBAB_REFCLK*	FBAB_REFCLK	90DIFF	1	OUT	4.3<
FB_CLK1	W23	FBEF_REFCLK	FBEF_REFCLK	90DIFF	1	OUT	6.3<
FB_CLK1	W22	FBEF_REFCLK*	FBEF_REFCLK	90DIFF	1	OUT	6.3<
FB_CLK2	M25	FBCD_REFCLK	FBCD_REFCLK	90DIFF	1	OUT	5.3<
FB_CLK2	M24	FBCD_REFCLK*	FBCD_REFCLK	90DIFF	1	OUT	5.3<
FB_CLK3	N22	FBGH_REFCLK	FBGH_REFCLK	90DIFF	1	OUT	7.3<
FB_CLK3	N23	FBGH_REFCLK*	FBGH_REFCLK	90DIFF	1	OUT	7.3<

U2
NV102-P-A2
BGA533
COMMON

2/17 CLOCK OUT

NET_NAME		DIFF_PAIR	NV_IMP
PLL_V_VDD	P4		
PLL_SP_AVDD	H24		
PLL_SP_MON_OUT	K22	SNN_NVIO_PLL_SP_MON_OUT	
CLK_RSET_GND	J22	NVIO_CLK_RSET_GND	

GV_RX_RSET_VDD	BJ17	GV_RX_RSET_VDD							
GV_TX_RSET_GND	BL23	GV_TX_RSET_GND							
NVIO_GVDR_RX_RSET_GND	P26	NVIO_GVDR_RX_RSET_GND							
NVIO_GVDR_TX_RSET_GND	R26	NVIO_GVDR_TX_RSET_GND							

LDT_VDDQ R19, T19, U19

VDD J13, J15, L11, L12, L13, L14, L15, L16, L17, M11, M12, M14, M17, N17, R11, T11, T14, T16, T17, U11, U12, U13, U14, U15, U16, U17, W13, W15

VDD33 J10, J18, K19, K9, V19, V9, W10, W18

PLL_GV_VDD L24 NVIO_GV_PLLVDD 12MIL 3.3V

PLL_GV_AVDD P24 NVIO_GV_PLLAVDD 12MIL 1.15V

GV_PLL_AVDD BK18 LB504 240R@100MHz BEAD_0402 COMMON 12MIL 1.15V GV_PLLAVDD

1V15 R745 150 1% 0402 COMMON

1V15 R737 150 1% 0402 COMMON

R849 49.9 1% 0402 COMMON

R846 150 1% 0402 COMMON

R864 1.5K 1% 0402 COMMON

LB515 240R@100MHz BEAD_0402 COMMON 12MIL 3.3V NVIO_PLLVDD

LB506 240R@100MHz BEAD_0402 COMMON 12MIL 1.15V NVIO_SP_PLLVDD

LB508 240R@100MHz BEAD_0402 COMMON

LB507 240R@100MHz BEAD_0402 COMMON

1V15	C957	10UF	10V	10%	X5R	0805	COMMON
	C953	10UF	10V	10%	X5R	0805	COMMON
	C883	4.7UF	6.3V	10%	X5R	0603	COMMON
	C68	4.7UF	6.3V	10%	X5R	0603	COMMON
	C876	.1UF	6.3V	10%	X7R	0402	COMMON
	C899	.1UF	6.3V	10%	X7R	0402	COMMON
	C873	.1UF	6.3V	10%	X7R	0402	COMMON
	C847	.1UF	6.3V	10%	X7R	0402	COMMON
	C851	.1UF	6.3V	10%	X7R	0402	COMMON
	C872	.1UF	6.3V	10%	X7R	0402	COMMON
	C837	.1UF	6.3V	10%	X7R	0402	COMMON
	C915	1UF	6.3V	10%	X5R	0402	COMMON
	C896	4.7UF	6.3V	10%	X5R	0603	COMMON
	C900	1UF	6.3V	10%	X5R	0402	COMMON
	C893	.1UF	6.3V	10%	X7R	0402	COMMON
1V15	C1148	.1UF	6.3V	10%	X7R	0402	COMMON
	C1147	.1UF	6.3V	10%	X7R	0402	COMMON
	C1162	.1UF	6.3V	10%	X7R	0402	COMMON
	C1161	.1UF	6.3V	10%	X7R	0402	COMMON
	C1165	1UF	6.3V	10%	X5R	0402	COMMON
	C1149	1UF	6.3V	10%	X5R	0402	COMMON
1V15	C1164	.1UF	6.3V	10%	X7R	0402	COMMON
	C1167	.1UF	6.3V	10%	X7R	0402	COMMON
	C1175	.1UF	6.3V	10%	X7R	0402	COMMON
	C1192	.1UF	6.3V	10%	X7R	0402	COMMON
	C1163	.1UF	6.3V	10%	X7R	0402	COMMON
	C1169	1UF	6.3V	10%	X5R	0402	COMMON
	C1122	4.7UF	6.3V	10%	X5R	0603	COMMON
1V15	C1160	.1UF	6.3V	10%	X7R	0402	COMMON
	C1183	.1UF	6.3V	10%	X7R	0402	COMMON
	C1182	.1UF	6.3V	10%	X7R	0402	COMMON
	C1168	.1UF	6.3V	10%	X7R	0402	COMMON
	C1176	.1UF	6.3V	10%	X7R	0402	COMMON
	C1191	1UF	6.3V	10%	X5R	0402	COMMON
	C1138	4.7UF	6.3V	10%	X5R	0603	COMMON
3V3	C1158	.1UF	6.3V	10%	X7R	0402	COMMON
	C1157	.1UF	6.3V	10%	X7R	0402	COMMON
	C1190	.1UF	6.3V	10%	X7R	0402	COMMON
	C1188	.1UF	6.3V	10%	X7R	0402	COMMON
	C1155	.1UF	6.3V	10%	X7R	0402	COMMON
	C1156	.1UF	6.3V	10%	X7R	0402	COMMON
	C1145	.1UF	6.3V	10%	X7R	0402	COMMON
	C1159	1UF	6.3V	10%	X5R	0402	COMMON
3V3	C1140	.01UF	16V	10%	X7R	0402	COMMON
	C1136	1UF	6.3V	10%	X7R	0402	COMMON
	C1130	1UF	6.3V	10%	X5R	0402	COMMON
	C1133	1UF	6.3V	10%	X5R	0402	COMMON
	C1127	1UF	6.3V	10%	X5R	0402	COMMON
1V15	C1142	.01UF	16V	10%	X7R	0402	COMMON
	C1135	.1UF	6.3V	10%	X7R	0402	COMMON
	C1128	1UF	6.3V	10%	X5R	0402	COMMON
	C1132	1UF	6.3V	10%	X5R	0402	COMMON
	C1126	1UF	6.3V	10%	X5R	0402	COMMON
3V3	C1230	1UF	6.3V	10%	X5R	0402	COMMON
	C1225	1UF	6.3V	10%	X5R	0402	COMMON
	C1221	1UF	6.3V	10%	X5R	0402	COMMON
	C1223	.1UF	6.3V	10%	X7R	0402	COMMON
	C1219	.01UF	16V	10%	X7R	0402	COMMON
1V15	C1121	1UF	6.3V	10%	X5R	0402	COMMON
	C1129	1UF	6.3V	10%	X5R	0402	COMMON
	C1131	1UF	6.3V	10%	X5R	0402	COMMON
	C1134	.1UF	6.3V	10%	X7R	0402	COMMON
	C1141	.01UF	16V	10%	X7R	0402	COMMON

GND

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	GPU-NVIO Interconnect: GV Bus / PLL

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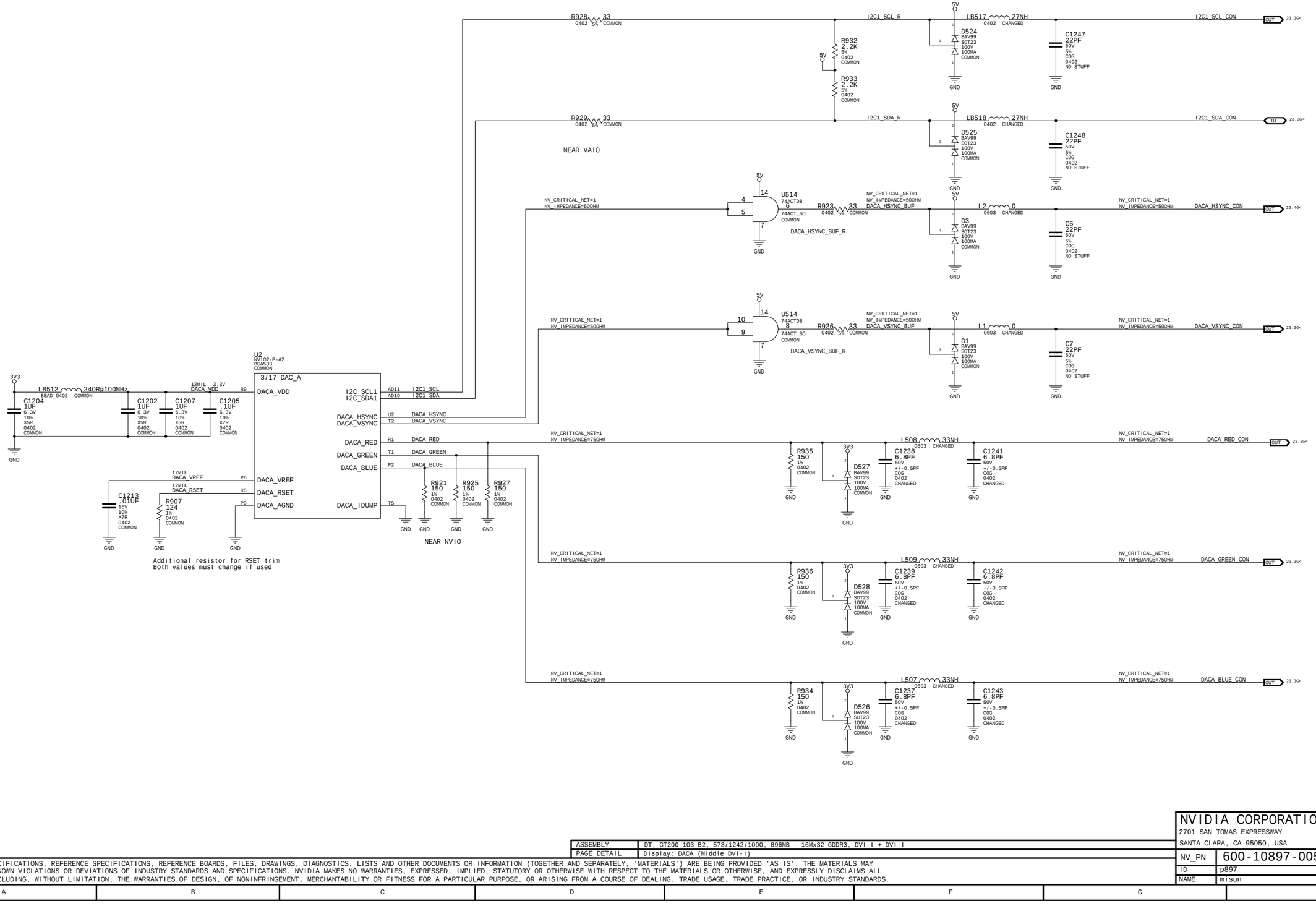
Display: DACA (Middle DVI-I)



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Display: DACA (Middle DVI-I)

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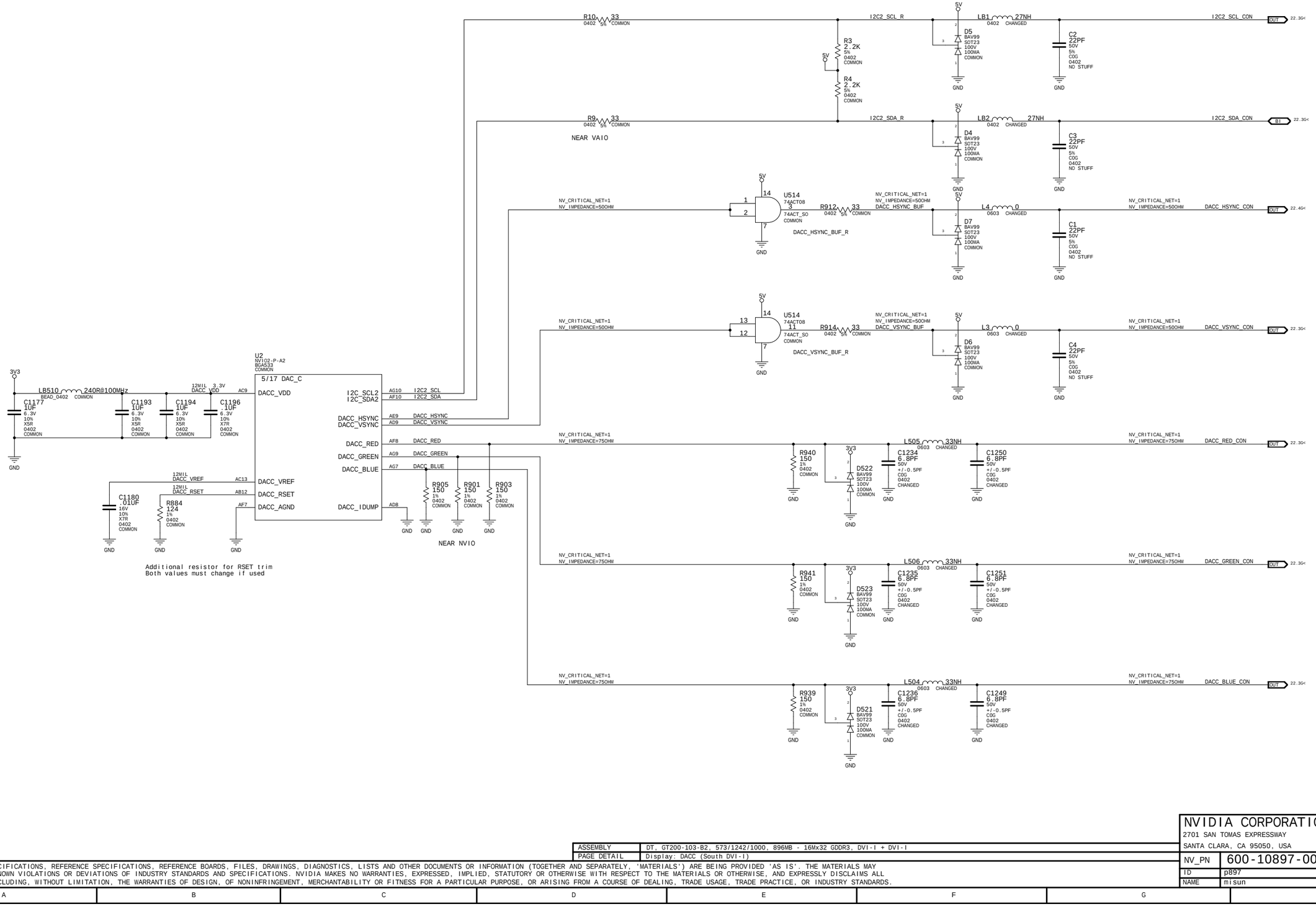
Display: DACC (South DVI-I)



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Display: DACC (South DVI-I)

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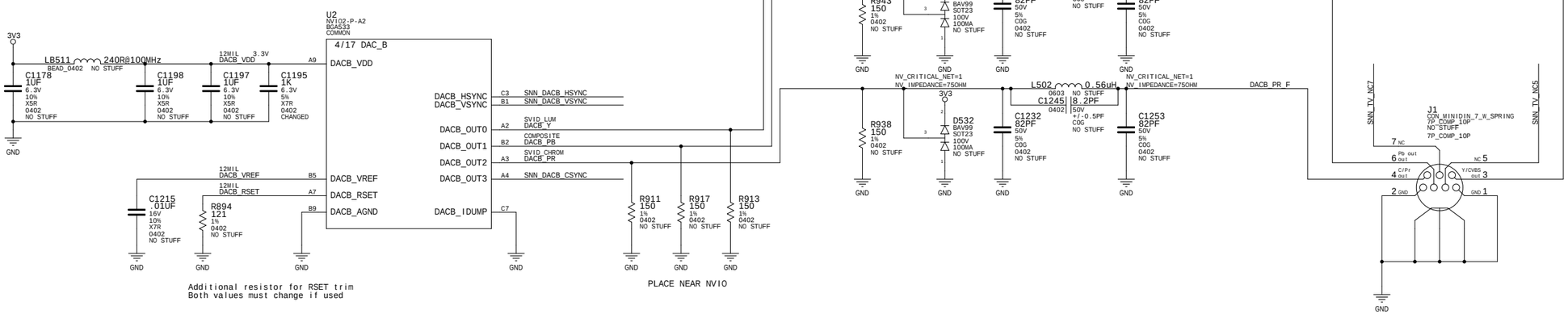
Display: DACB (North MiniDIN) SD/HDTV out



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Display: DACB (North MiniDIN) SD/HDTV out

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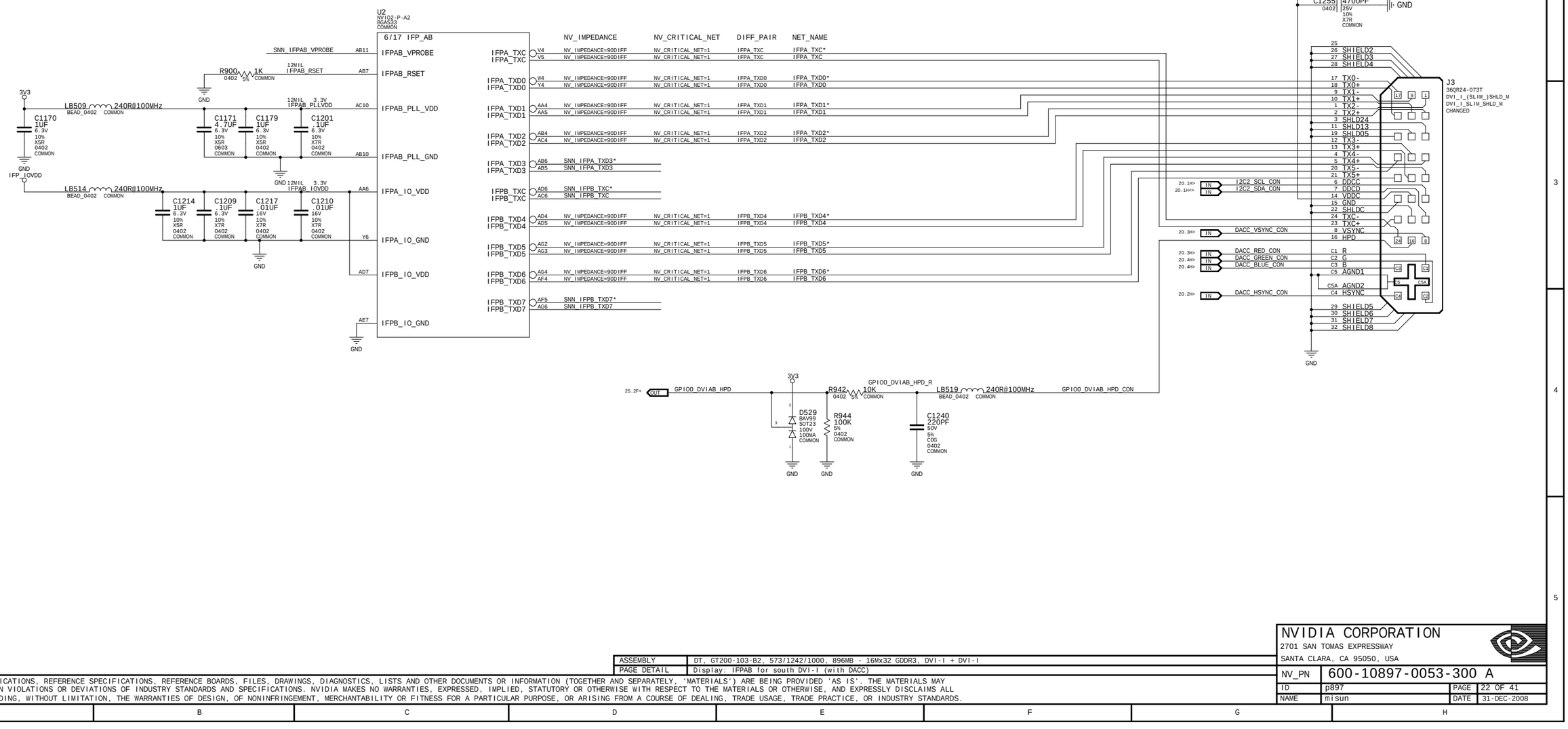
Display: IFPAB for South DVI-I (with DACC)



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Display: IFPAB for south DVI-I (with DACC)

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Display: IFPCD for middle DVI-I (with DACA)

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Display: IFPCD for middle DVI-I (with DACA)

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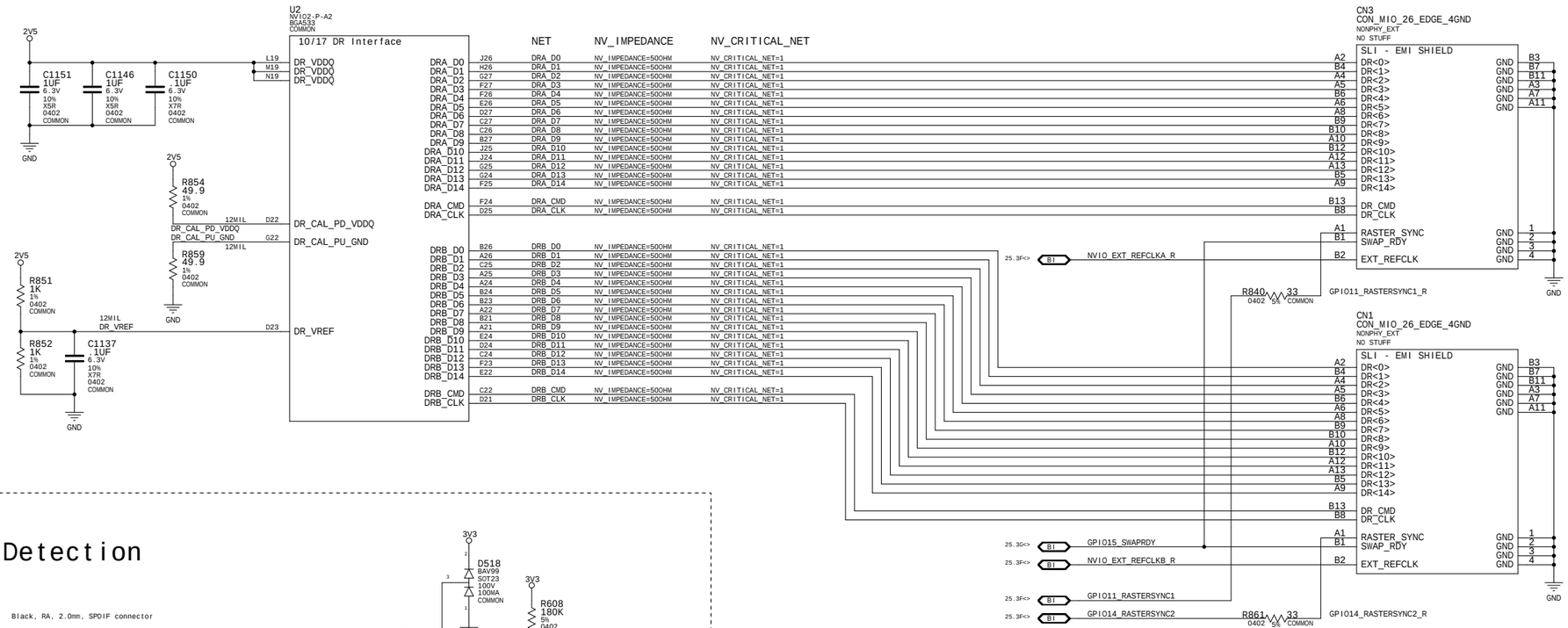
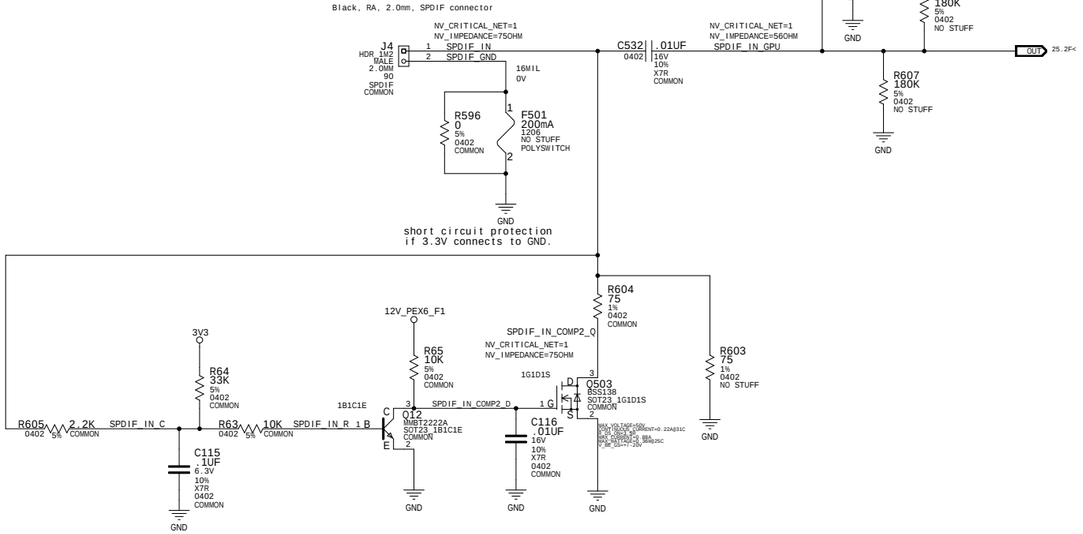
Connectors: DR Interface (Dual SLI) / SPDIF



SPDIF INPUT / Level Detection



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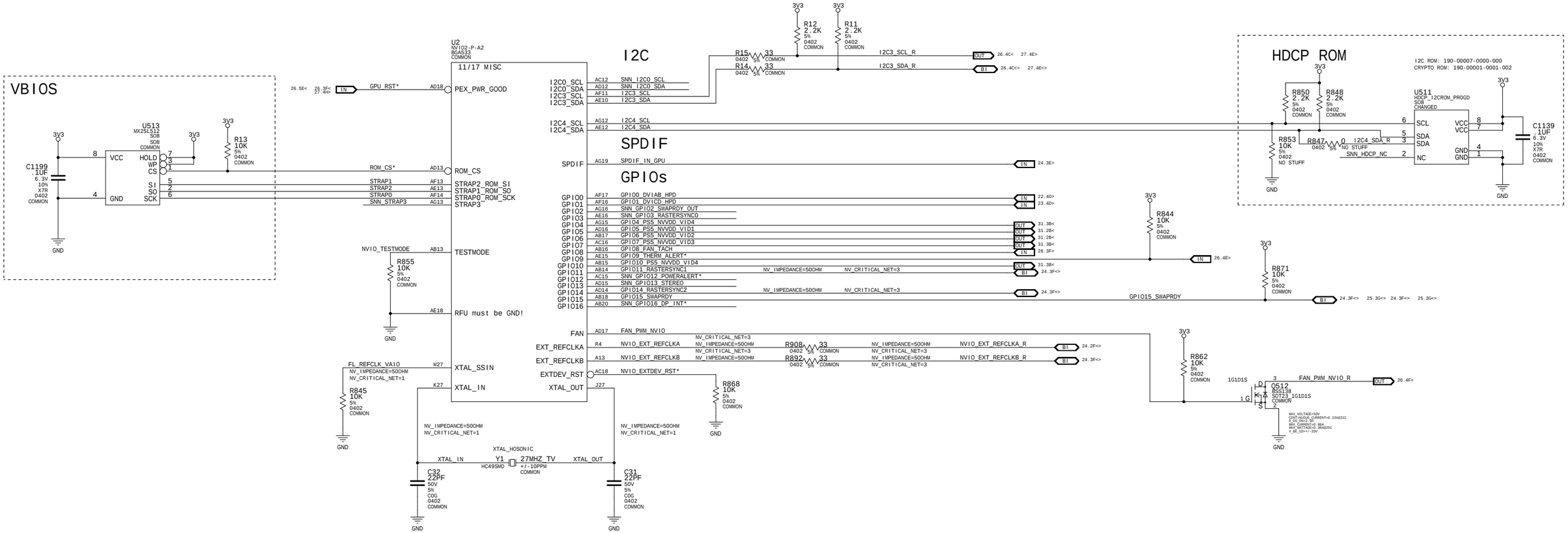
MISC: GPIO / XTAL / VBIOS / HDCP / I2C



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	MISC: GPIO / XTAL / VBIOS / HDCP / I2C

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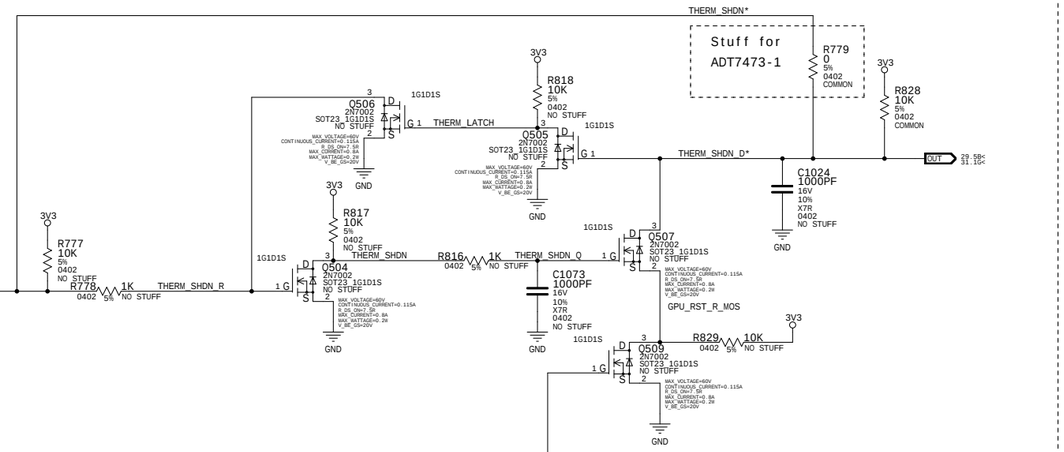
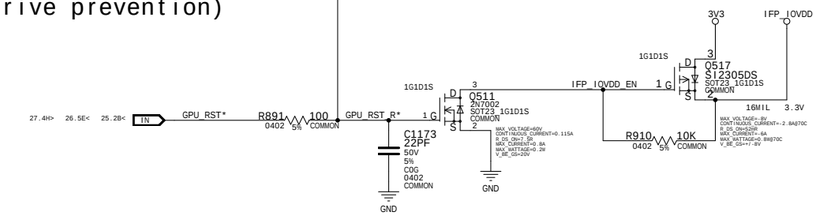
MISC: FAN / THERM / IFP_IOVDD

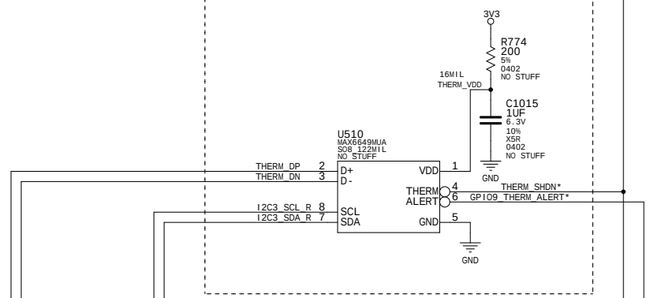
THERM OVERT SHUTDOWN LATCH



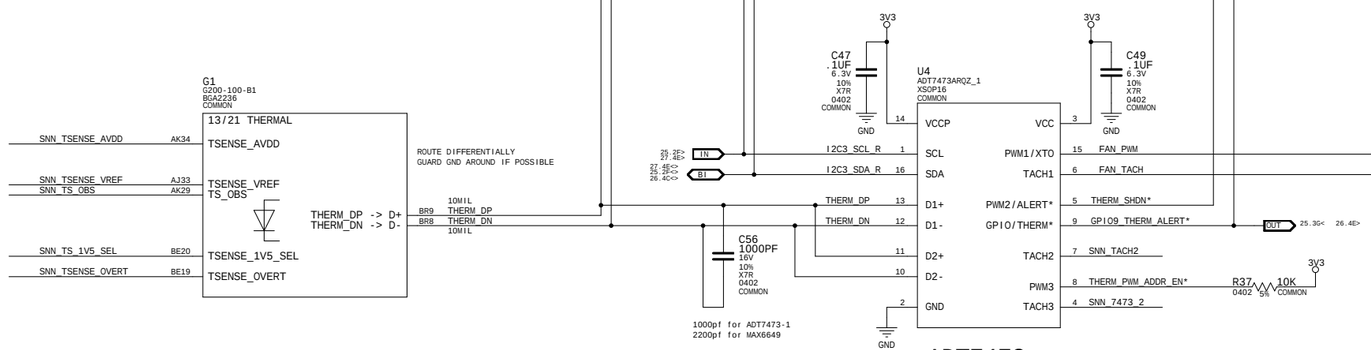
IFP_IOVDD (backdrive prevention)



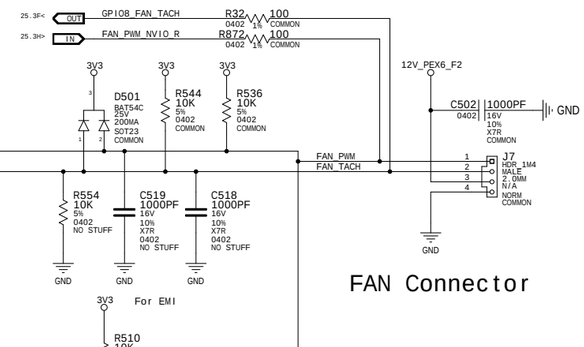
MAX6649 option



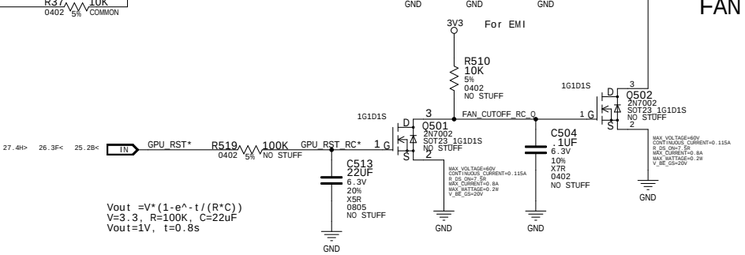
ADT7473



GPU Driven Fan and Tach



FAN Connector



At power on (not warm boot) stops fan for ~0.8sec

ASSEMBLY	
PAGE DETAIL	MISC: FAN / THERM / IFP_IOVDD

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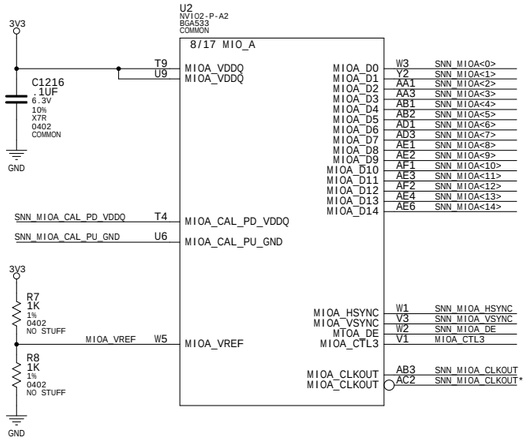
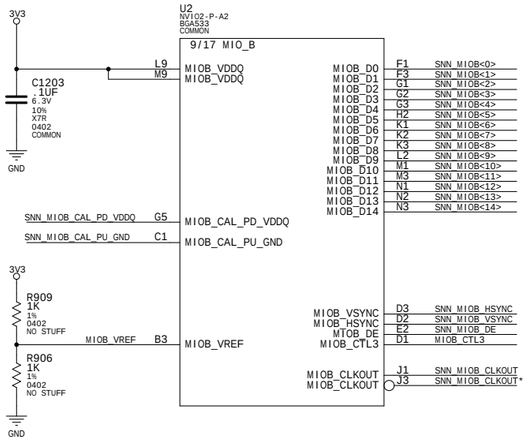
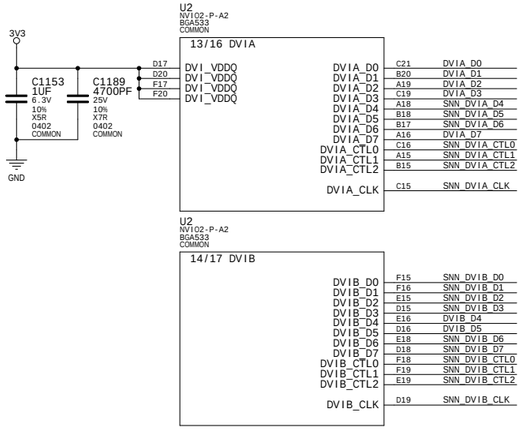
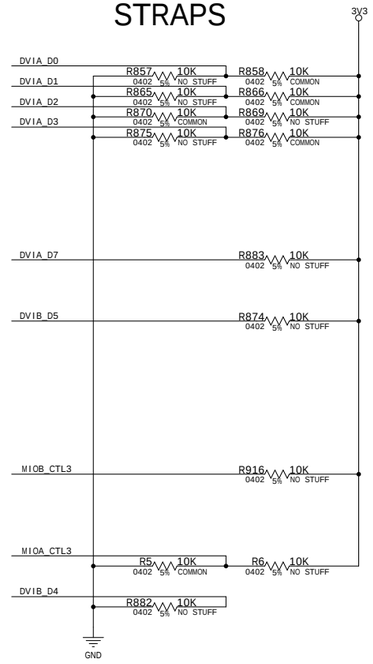
MISC: MIO / DVI / STRAPS / Hybrid







STRAPS



STRAP BITS BOOT0 = 0x101000

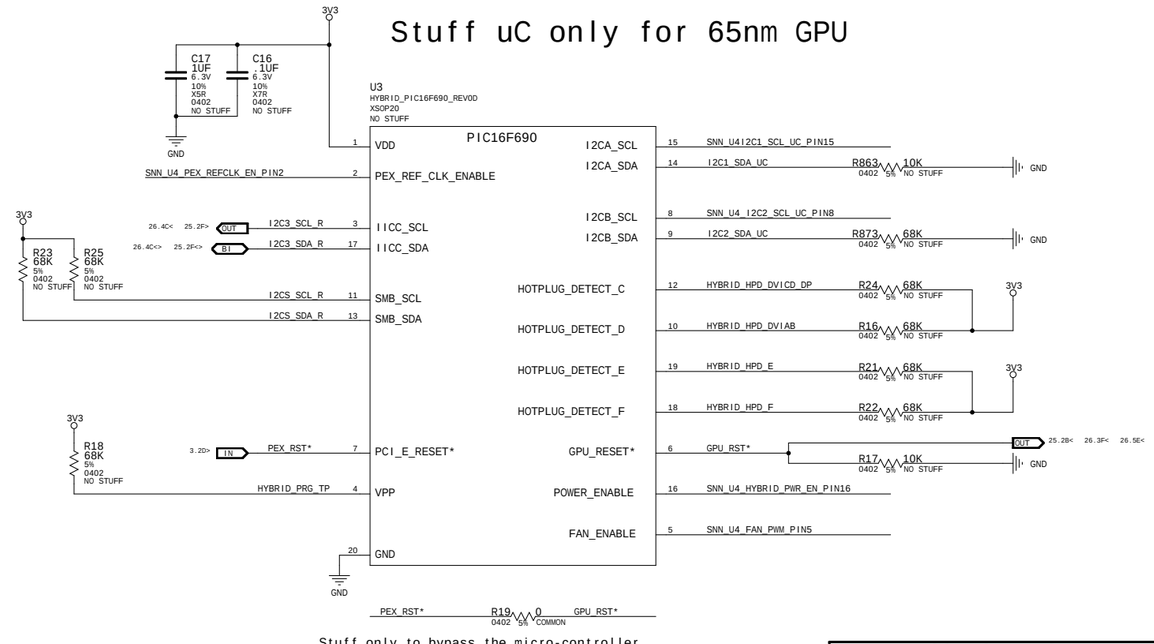
NR_:_USAGE	COMMENT
00 : GV_WIDTH	DEFAULT=0x0 (WIDE)
01 : SUB_VENDOR	DEFAULT=0x1 (FROM BIOS)
02 : RAM_CFG[0]	
03 : RAM_CFG[1]	
04 : RAM_CFG[2]	
05 : RAM_CFG[3]	
06 : CRYSTAL	DEFAULT=0x0 (27MHz)
07 : TV_MODE[0]	DEFAULT=0x1 (NTSC_J)
08 : TV_MODE[1]	
09 : TV_MODE[2]	
10 : PCI_DEVID[0]	SET BY BIOS
11 : PCI_DEVID[1]	
12 : PCI_DEVID[2]	
13 : PCI_DEVID[3]	DEFAULT=0x0
14 : FB_SIZE[0]	DEFAULT=0x2 (256MB ??)
15 : FB_SIZE[1]	
16 : FB_SIZE[2]	
17 : PEX_PLL_EN_TERM100	DEFAULT=0x0 (ENABLED)
18 : 3GIO_PAD_CFG_LUT_ADR[0]	DEFAULT=0x3 (DESKTOP_DEFAULT)
19 : 3GIO_PAD_CFG_LUT_ADR[1]	
20 : 3GIO_PAD_CFG_LUT_ADR[2]	
21 : 3GIO_PAD_CFG_LUT_ADR[3]	
22 : ROMTYPE[0]	DEFAULT=0x1 (AT25S)
23 : ROMTYPE[1]	
24 : USER[0]	SET BY BIOS
25 : USER[1]	
26 : USER[2]	
27 : USER[3]	
28 : PCI_DEVID_EXT	DEFAULT=0x0

STRAP BITS BOOT3 = 0x10100C

NR_:_USAGE	COMMENT
06 : XCLK_555	DEFAULT=0x0
16 : PCI_IOBAR	DEFAULT=0x1 0=DISABLE, 1=ENABLE

CFG	Config Width	Vendor
0000	Reserved	
0001	16Mx32	512-bit Qimonda
0010	16Mx32	512-bit Hynix*
0011	16Mx32	512-bit Samsung*
0100	Reserved	
0101	32Mx32	512-bit Qimonda
0110	32Mx32	512-bit Hynix
0111	32Mx32	512-bit Samsung
1000	Reserved	
1001	16Mx32	448-bit Qimonda
1010	16Mx32	448-bit Hynix
1011	16Mx32	448-bit Samsung
1100	Reserved	
1101	32Mx32	448-bit Qimonda
1110	32Mx32	448-bit Hynix
1111	32Mx32	448-bit Samsung

Stuff uC only for 65nm GPU



Stuff only to bypass the micro-controller

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	MISC: MIO / DVI / STRAPS / Hybrid

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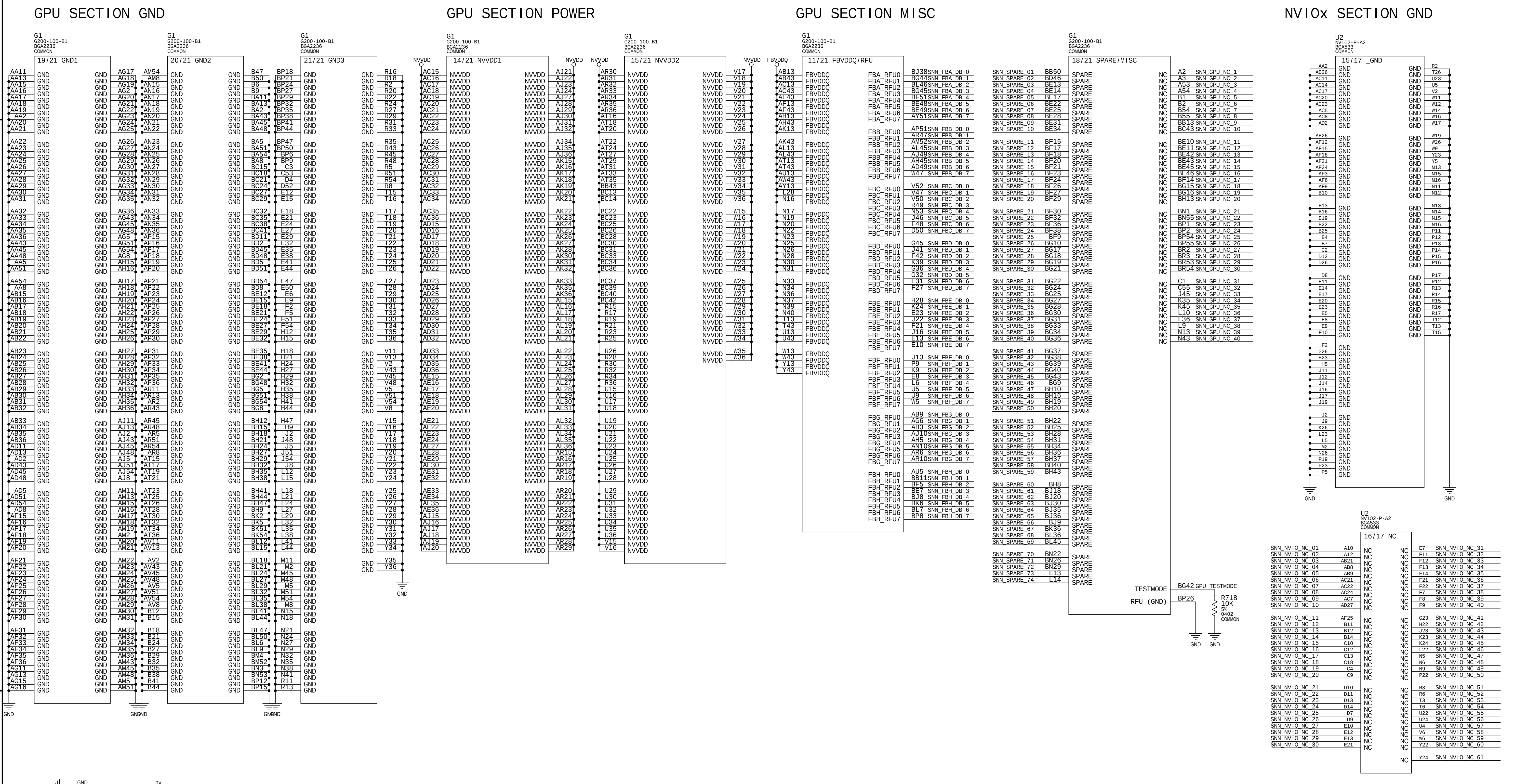
Power and GND (GPU and NVIOx)



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power and GND (GPU and NVIOx)

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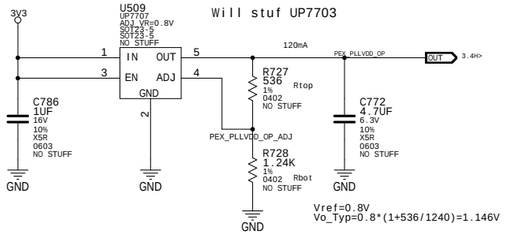
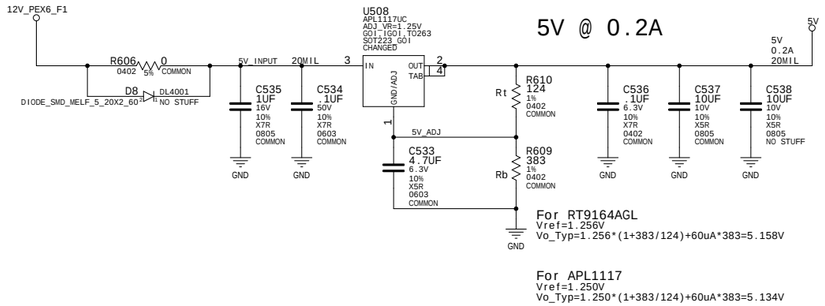
Power Supply: 2V5 / PEX_PLLVDD / 1V15 (PEX_VDD, GV_VDD)

PEX PLLVDD optional Supply

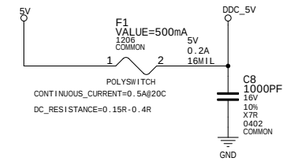


5V Linear



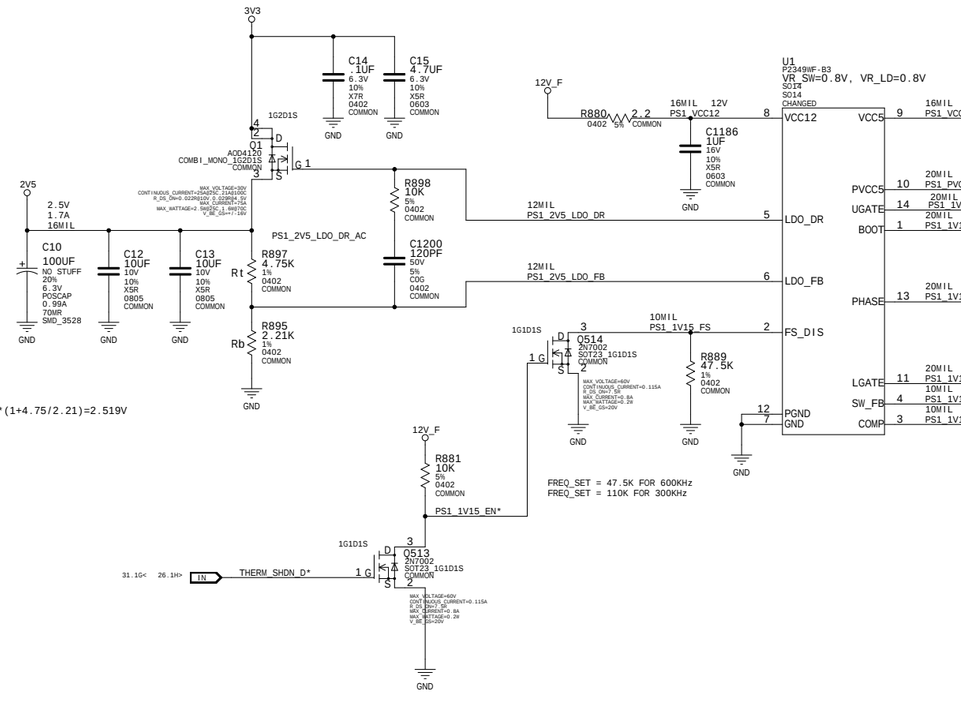
DDC_5V

5V @ 200mA



1V15 (PEX_VDD AND GV_VDD/Q) and 2V5

2V5 @ 1.7A



ASSEMBLY	
PAGE DETAIL	Power Supply: 2V5 / PEX_PLLVDD / 1V15 (PEX_VDD, GV_VDD)

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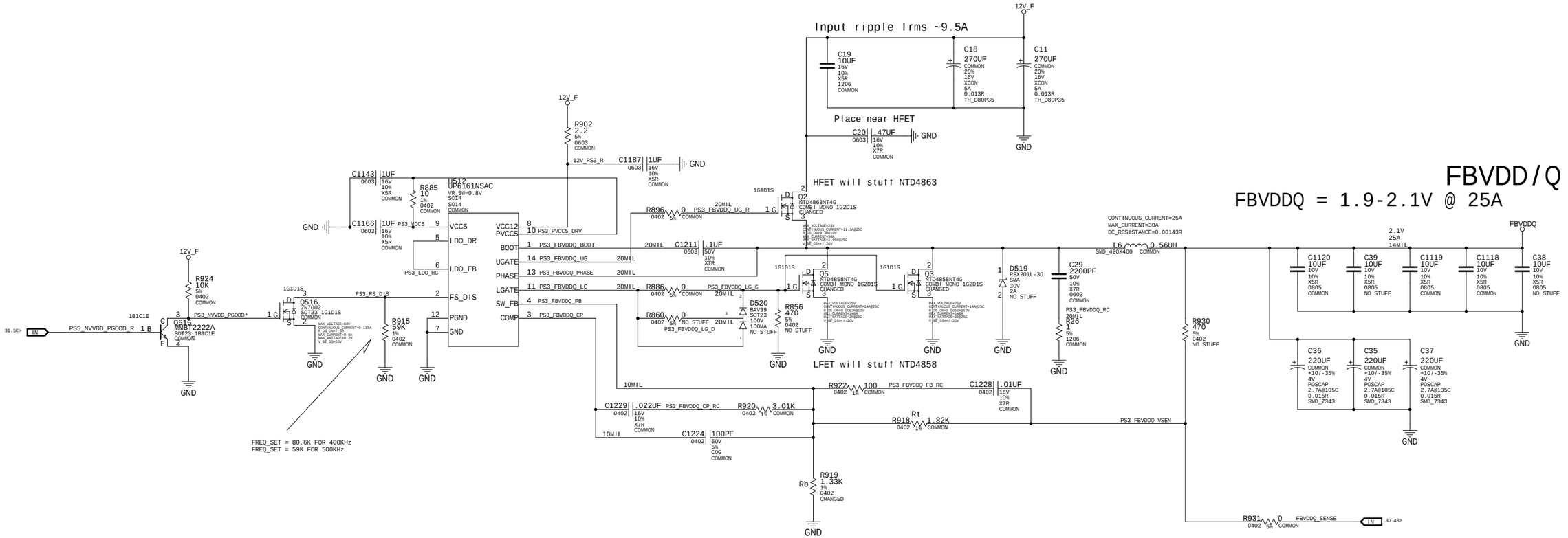
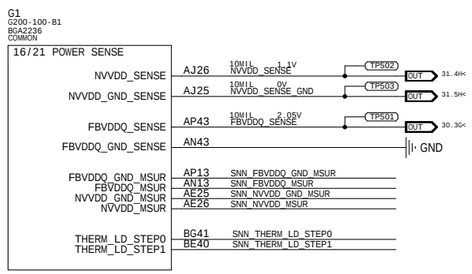
Power Supply: Combined FBVDD/Q



NVVDD & FBVDDQ SENSE/MSUR



Vref=0.8V
Vo_Typ=0.8*(1+1.82/1.15)=2.066V for Hynix memory
Vo_Typ=0.8*(1+1.82/1.33)=1.895V for Samsung memory

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power Supply: Combined FBVDD/Q

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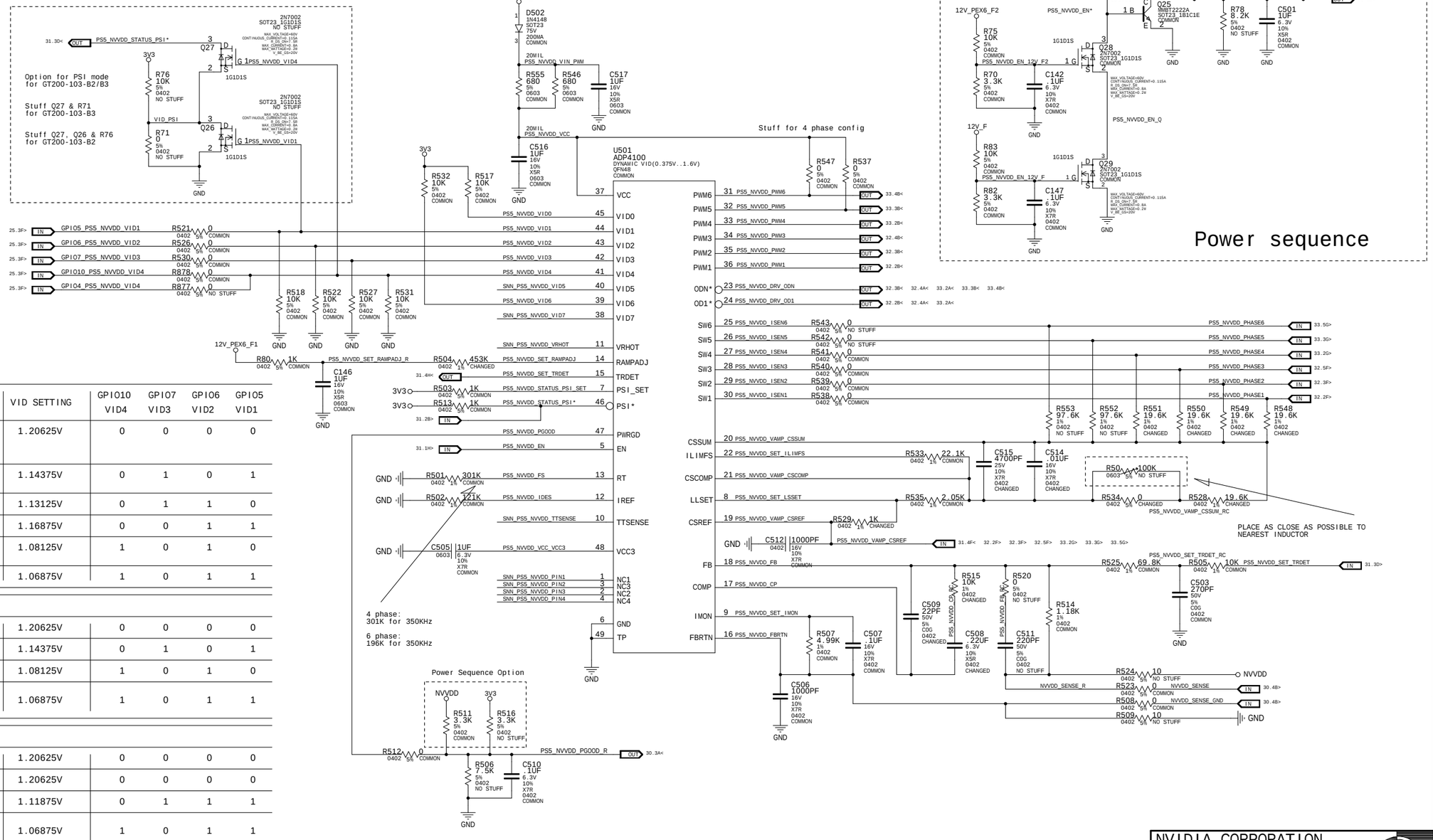
Power Supply: NVVDD Regulator

GPIO10 VID4	GPIO7 VID3	GPIO6 VID2	GPIO5 VID1	VID0	VOLTAGE	
0	0	0	0	1	1.20625	--Default
0	0	0	1	0	1.20000	
0	0	0	1	1	1.19375	
0	0	1	0	0	1.18750	
0	0	1	0	1	1.18125	
0	0	1	1	0	1.17500	
0	0	1	1	1	1.16875	
0	1	0	0	0	1.16250	
0	1	0	0	1	1.15625	
0	1	0	1	0	1.15000	
0	1	0	1	1	1.14375	
0	1	1	0	0	1.13750	
0	1	1	0	1	1.13125	
0	1	1	1	0	1.12500	
0	1	1	1	1	1.11875	
1	0	0	0	0	1.11250	
1	0	0	0	1	1.10625	
1	0	0	1	0	1.10000	
1	0	0	1	1	1.09375	
1	0	1	0	0	1.08750	
1	0	1	0	1	1.08125	
1	0	1	1	0	1.07500	
1	0	1	1	1	1.06875	
1	1	0	0	0	1.06250	
1	1	0	0	1	1.05625	
1	1	0	1	0	1.05000	

NVVDD Voltage Select

ADP4100 has VID offset controlled by Rb
Here VID code can set higher to counteract this offset voltage.

		VOLTAGE	VID SETTING	GPIO10 VID4	GPIO7 VID3	GPIO6 VID2	GPIO5 VID1
GT200-103-A2							
	BOOT VOLTAGE	1.1875V	1.20625V	0	0	0	0
VB0	2D MODE, DOS;						
	3D MODE, P0 MODE; 2D MODE, P8 MODE;	1.1250V	1.14375V	0	1	0	1
	2D MODE, P12 MODE;	1.1125V	1.13125V	0	1	1	0
VB1	2D MODE, DOS;	1.1500V	1.16875V	0	0	1	1
	3D MODE, P0 MODE; 2D MODE, P8 MODE;	1.0625V	1.08125V	1	0	1	0
	2D MODE, P12 MODE;	1.0500V	1.06875V	1	0	1	0
GT200-103-B2							
	BOOT VOLTAGE	1.1875V	1.20625V	0	0	0	0
VB0	3D MODE, P0 MODE;	1.1250V	1.14375V	0	1	0	1
VB1	3D MODE, P0 MODE;	1.0625V	1.08125V	1	0	1	0
VB0/VB1	2D MODE, P8 MODE; 2D MODE, P12 MODE; 2D MODE, DOS;	1.0500V	1.06875V	1	0	1	1
GT200-103-B3							
	BOOT VOLTAGE	1.1875V	1.20625V	0	0	0	0
VB0	3D MODE, P0 MODE;	1.1875V	1.20625V	0	0	0	0
VB1	3D MODE, P0 MODE;	1.1000V	1.11875V	0	1	1	1
VB0/VB1	2D MODE, P8 MODE; 2D MODE, P12 MODE; 2D MODE, DOS;	1.0500V	1.06875V	1	0	1	1



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	NVVDD Regulator

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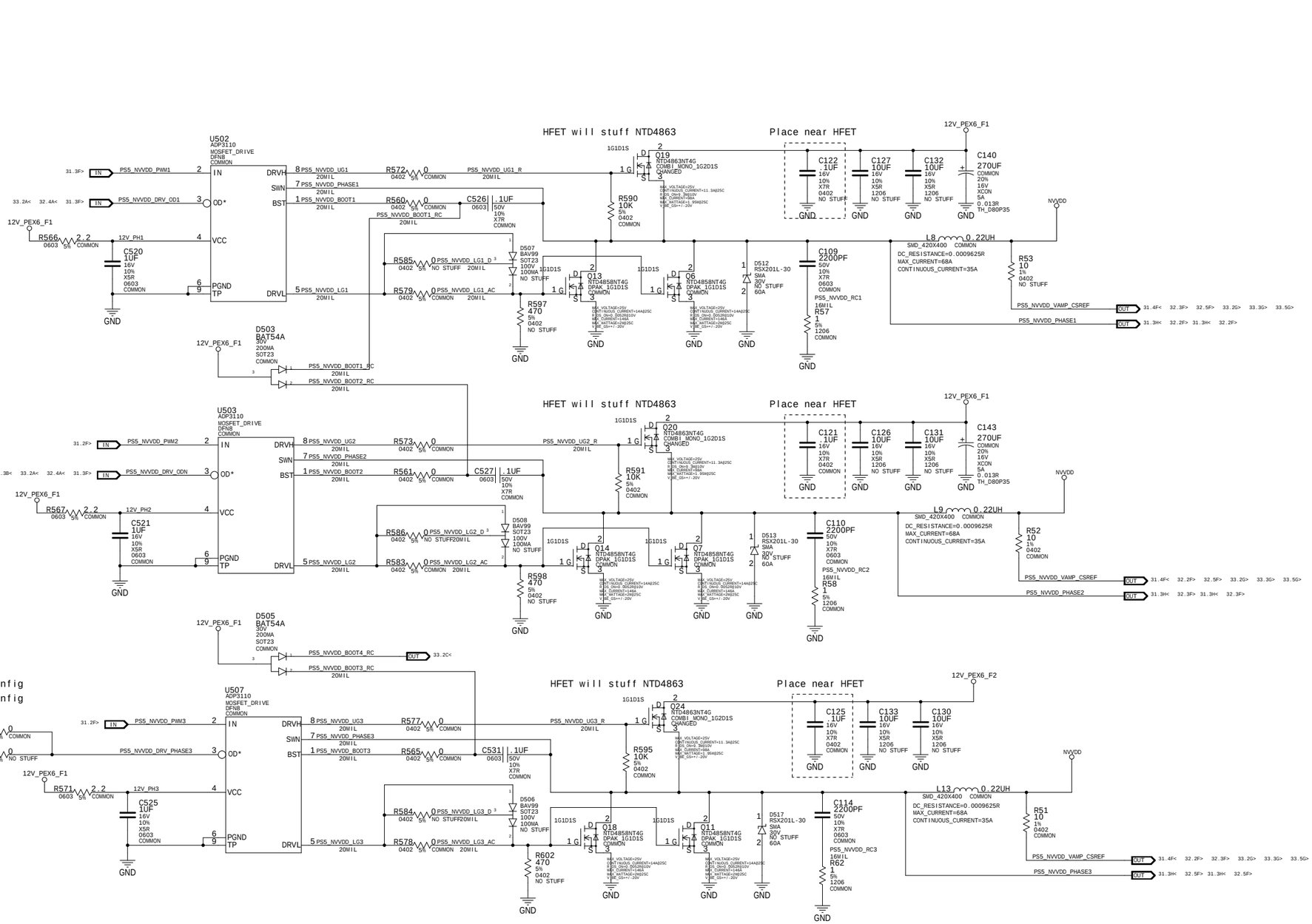
Power Supply: NVVDD Phase 1,2,3 powered from external PEX 6PIN



ASSEMBLY	
PAGE DETAIL	Power Supply: NVVDD Phase 1-3 of 6

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NV_PN	600-10897-0053-300 A		
ID	p897	PAGE	32 OF 41
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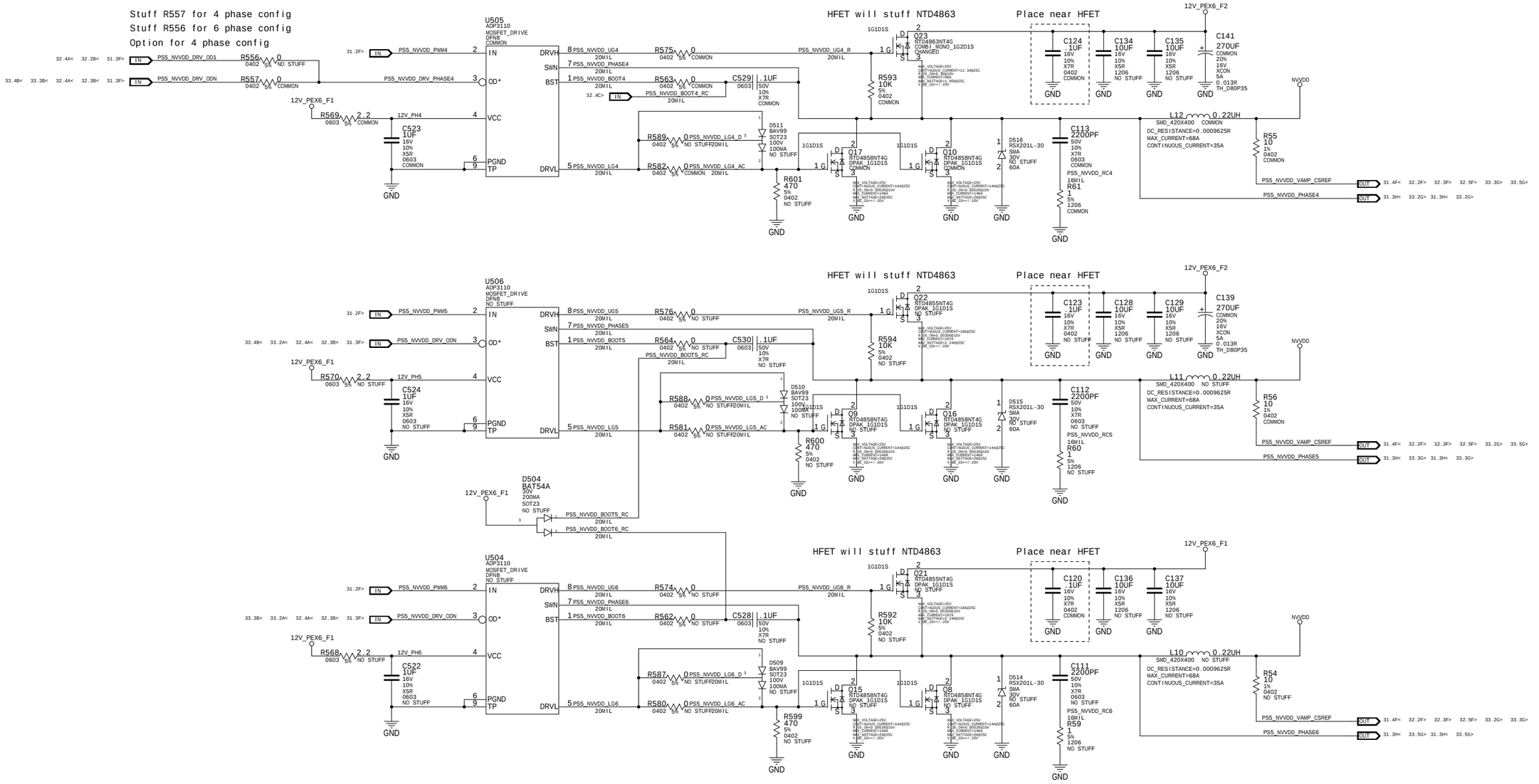
Power Supply: NVVDD Phase 4,5,6 powered from external PEX 6PIN



ASSEMBLY	
PAGE DETAIL	Power Supply: NVVDD Phase 4-6 of 6

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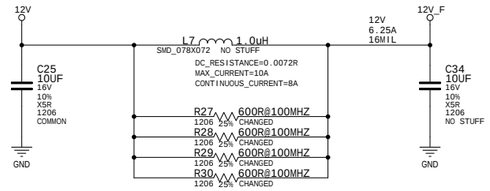
Power: Input Rail Filter

Connector Power State Table

2x3 Connector	2x3 Connector	Power	STATE
Connected	Connected	225W	Full Perf
Connected	Not Connected	150W	Board Off
Not Connected	Connected	150W	Board Off
Not Connected	Not Connected	75W	Board Off

PEX_12V INPUT - 66W

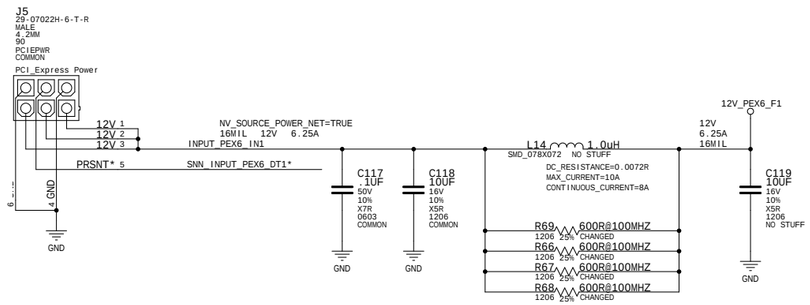


ALTERNATIVE

Additional input filtering and Cin moved to respective PS sheets

PEX6 INPUT 1 - 2x3 PCIE CON 75W

MUST BE ATTACHED AND POWERED TO START BOARD

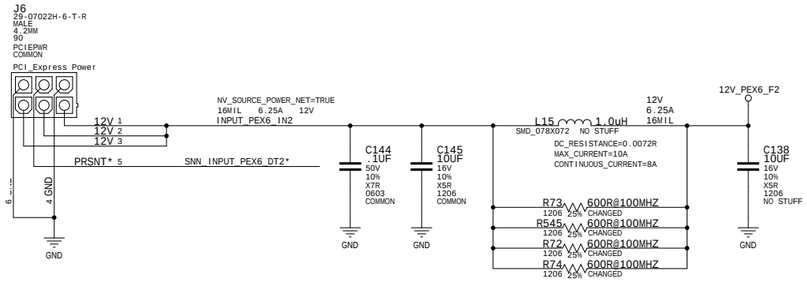


ALTERNATIVE

Additional input filtering and Cin moved to respective PS sheets

PEX6 INPUT 2 - 2x3 PCIE CON 75W

MUST BE ATTACHED AND POWERED TO START BOARD



ALTERNATIVE

Additional input filtering and Cin moved to respective PS sheets

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Power: Input Rail Filter

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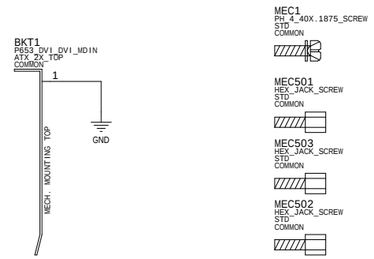
Thermal/Mechanical/ID

Bracket and Assembly



MEC1
PH_4.40X.1875_SCREW
STD
COMMON

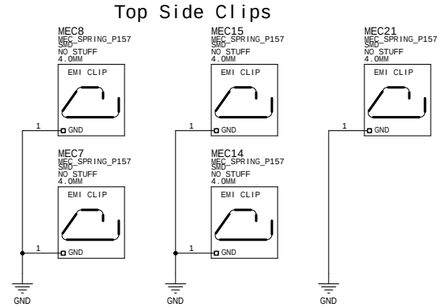
MEC501
HEX_JACK_SCREW
STD
COMMON

MEC503
HEX_JACK_SCREW
STD
COMMON

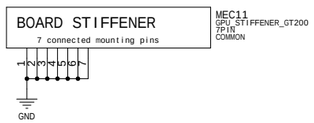
MEC502
HEX_JACK_SCREW
STD
COMMON

MEC504
HEX_JACK_SCREW
STD
COMMON

EMI Gnd Clips



GPU Stiffener

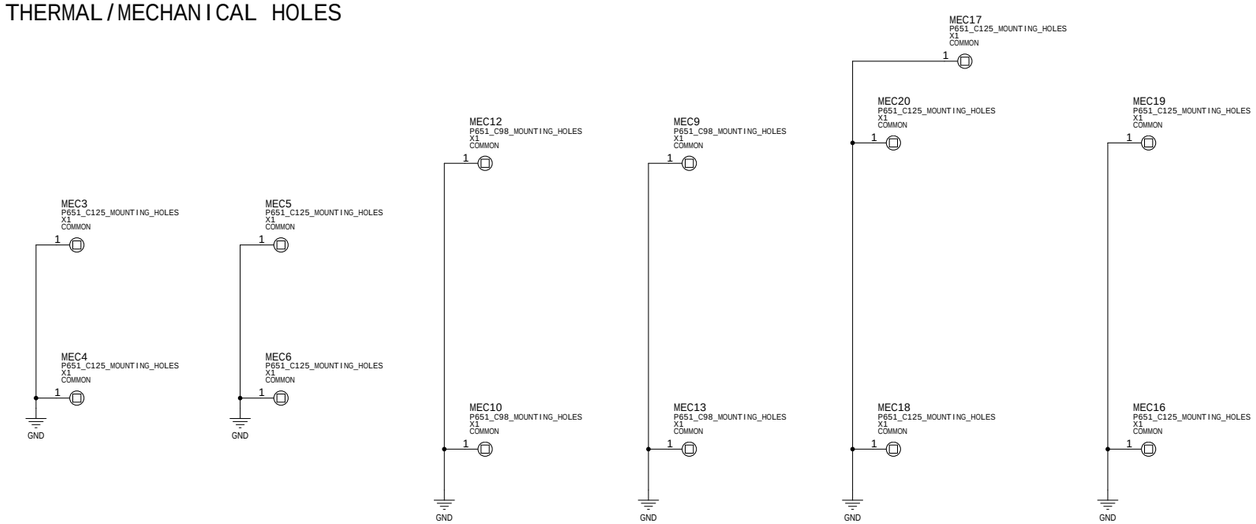


MEC11
GPU_STIFFENER_GT200
7PIN
COMMON

Hockey Stick Retention Mechanism

MEC2
PEX_RET_BRKOFF_P651
NOPTN
COMMON

THERMAL/MECHANICAL HOLES



ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
PAGE DETAIL	Thermal/Mechanical

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Title: Basenet Report
Design: p897
Date: Dec 2 14:57:45 2008

Base nets and synonyms for
p897_b00_lib.P897(@p897_b00_lib.p897(sch
_1))

Base Signal	Location([Zone][dir])
5V_ADJ	29.2E
5V_INPUT	29.1D
12V_PH1	32.2B
12V_PH2	32.3B
12V_PH3	32.4B
12V_PH4	33.2B
12V_PH5	33.3B
12V_PH6	33.4B
12V_PS3_R	30.2C
DACA_BLUE	19.3C
DACA_BLUE_CON	19.4H> 23.3G<
DACA_GREEN	19.3C
DACA_GREEN_CON	19.4H> 23.3G<
DACA_HSYNC	19.3C
DACA_HSYNC_BUF	19.2F
DACA_HSYNC_BUF_R	19.2E
DACA_HSYNC_CON	19.2H> 23.4G<
DACA_RED	19.3C
DACA_RED_CON	19.3H> 23.3G<
DACA_RSET	19.3B
DACA_VDD	19.3B
DACA_VREF	19.3B
DACA_VSYNC	19.3C
DACA_VSYNC_BUF	19.3F
DACA_VSYNC_BUF_R	19.3E
DACA_VSYNC_CON	19.3H> 23.3G<
DACB_PB	21.3C
DACB_PB_F	21.2F
DACB_PR	21.3C
DACB_PR_F	21.3F
DACB_RSET	21.3B
DACB_VDD	21.3B
DACB_VREF	21.3B
DACB_Y	21.3C
DACB_Y_F	21.2F
DACC_BLUE	20.3C
DACC_BLUE_CON	20.4H> 22.3G<
DACC_GREEN	20.3C
DACC_GREEN_CON	20.4H> 22.3G<
DACC_HSYNC	20.3C
DACC_HSYNC_BUF	20.2F
DACC_HSYNC_BUF_R	20.2E
DACC_HSYNC_CON	20.2H> 22.4G<
DACC_RED	20.3C
DACC_RED_CON	20.3H> 22.3G<
DACC_RSET	20.3B
DACC_VDD	20.3B
DACC_VREF	20.3B
DACC_VSYNC	20.3C
DACC_VSYNC_BUF	20.3F
DACC_VSYNC_BUF_R	20.3E
DACC_VSYNC_CON	20.3H> 22.3G<
DRA_CLK	24.2D
DRA_CMD	24.2D
DRA_D0	24.1D
DRA_D1	24.1D
DRA_D2	24.1D
DRA_D3	24.1D
DRA_D4	24.1D
DRA_D5	24.1D
DRA_D6	24.1D
DRA_D7	24.1D
DRA_D8	24.1D
DRA_D9	24.1D
DRA_D10	24.1D
DRA_D11	24.2D
DRA_D12	24.2D
DRA_D13	24.2D
DRA_D14	24.2D
DRB_CLK	24.2D
DRB_CMD	24.2D
DRB_D0	24.2D
DRB_D1	24.2D
DRB_D2	24.2D
DRB_D3	24.2D
DRB_D4	24.2D
DRB_D5	24.2D
DRB_D6	24.2D
DRB_D7	24.2D
DRB_D8	24.2D
DRB_D9	24.2D
DRB_D10	24.2D
DRB_D11	24.2D
DRB_D12	24.2D
DRB_D13	24.2D
DRB_D14	24.2D
DR_CAL_PD_VDDQ	24.2C

DR_CAL_PU_GND	24.2C
DR_VREF	24.2C
DVIA_D0	27.1E 27.4C
DVIA_D1	27.1E 27.4C
DVIA_D2	27.1E 27.4C
DVIA_D3	27.1E 27.4C
DVIA_D7	27.2E 27.4C
DVIB_D4	27.3E 27.5C
DVIB_D5	27.2E 27.5C
FAN_CUTOFF_RC_Q	26.5F
FAN_PWM	26.4D 26.4G
FAN_PWM_NVIO	25.3D
FAN_PWM_NVIO_R	25.3H> 26.4F<
FAN_TACH	26.4D 26.4G
FBA0_CLK0	4.4A 4.5G> 8.2A< 8.2A
	8.4G
FBA0_CLK0*	4.4A 4.5G> 8.2A< 8.2A
	8.4G
FBA0_CLK0_R	8.4H
FBA1_CLK0	4.4B 4.5G> 8.2A< 8.2C
	8.4G
FBA1_CLK0*	4.4B 4.5G> 8.2A< 8.2C
	8.4G
FBA1_CLK0_R	8.4H
FBABCD_MPLL_AVDD	4.3C> 5.4C<
FBAB_REFCLK	4.3C< 18.5D>
FBAB_REFCLK*	4.3C< 18.5D>
FBA_CMD<0>	4.3A 4.4F 8.1A 8.1A
	8.5A
FBA_CMD<0..28>	4.4G> 8.1A<
FBA_CMD<1>	4.3A 4.4F 8.1A 8.1A
	8.5A
FBA_CMD<2>	4.3A 4.4F 8.1A 8.1A
	8.5A
FBA_CMD<3>	4.3A 4.4F 8.1A 8.1A
	8.5A
FBA_CMD<4>	4.3A 4.4F 8.1A 8.1A
	8.5A
FBA_CMD<5>	4.3A 4.4F 8.1A 8.1A
	8.5A
FBA_CMD<6>	4.3A 4.4F 8.1A 8.2A
	8.2C 8.5F
FBA_CMD<7>	4.3A 4.4F 8.1A 8.1A
	8.1C
FBA_CMD<8>	4.3A 4.4F 8.1A 8.2A
	8.2C
FBA_CMD<9>	4.3A 4.4F 8.1A 8.1A
	8.1C
FBA_CMD<10>	4.3A 4.4F 8.1A 8.2A
	8.2C 8.5F
FBA_CMD<11>	4.3A 4.4F 8.1A 8.2A
	8.2C
FBA_CMD<12>	4.3A 4.4F 8.1A 8.1A
	8.1C
FBA_CMD<13>	4.3A 4.4F 8.1A 8.2A
	8.2C
FBA_CMD<14>	4.3A 4.4F 8.1A 8.1A
	8.1C
FBA_CMD<15>	4.3A 4.4F 8.1A 8.2A
	8.2C
FBA_CMD<16>	4.3A 4.4F 8.1A 8.1A
	8.1C
FBA_CMD<17>	4.3A 4.4F 8.1A 8.1A
	8.1C
FBA_CMD<18>	4.3A 4.4F 8.1A 8.1A
	8.1C
FBA_CMD<19>	4.3A 4.4F 8.1A 8.1A
	8.1C
FBA_CMD<20>	4.3A 4.4F 8.1A 8.1C
	8.2A
FBA_CMD<21>	4.3A 4.4F 8.1A 8.1C
	8.2A
FBA_CMD<23>	4.3A 4.4F 8.1C 8.2A
	8.5C
FBA_CMD<24>	4.3A 4.5F 8.1C 8.2A
	8.5C
FBA_CMD<25>	4.4A 4.5F 8.1C 8.2A
	8.5C
FBA_CMD<26>	4.4A 4.5F 8.1C 8.2A
	8.5C
FBA_CMD<27>	4.4A 4.5F 8.1C 8.2A
	8.5C
FBA_CMD<28>	4.4A 4.5F 8.1C 8.2A
	8.5C
FBA_D<0>	4.1A 4.1F 8.2A 8.3A
FBA_D<0..63>	4.1G> 8.2A<>
FBA_D<1>	4.1A 4.1F 8.2A 8.3A
FBA_D<2>	4.1A 4.1F 8.2A 8.3A
FBA_D<3>	4.1A 4.1F 8.2A 8.3A
FBA_D<4>	4.1A 4.1F 8.2A 8.4A
FBA_D<5>	4.1A 4.1F 8.2A 8.4A
FBA_D<6>	4.1A 4.1F 8.2A 8.4A
FBA_D<7>	4.1A 4.1F 8.3A 8.4A
FBA_D<8>	4.1A 4.1F 8.3A 8.3B
FBA_D<9>	4.1A 4.1F 8.3A 8.3B
FBA_D<10>	4.1A 4.1F 8.3A 8.3B

FBA_D<11>	4.1A 4.1F 8.3A 8.3B
FBA_D<12>	4.1A 4.1F 8.3A 8.4B
FBA_D<13>	4.1A 4.1F 8.3A 8.4B
FBA_D<14>	4.1A 4.1F 8.3A 8.4B
FBA_D<15>	4.1F 4.2A 8.3A 8.4B
FBA_D<16>	4.1F 4.2A 8.3A 8.4A
FBA_D<17>	4.1F 4.2A 8.3A 8.4A
FBA_D<18>	4.1F 4.2A 8.3A 8.4A
FBA_D<19>	4.1F 4.2A 8.3A 8.4A
FBA_D<20>	4.1F 4.2A 8.3A 8.4A
FBA_D<21>	4.1F 4.2A 8.3A 8.4A
FBA_D<22>	4.1F 4.2A 8.3A 8.4A
FBA_D<23>	4.1F 4.2A 8.3A 8.4A
FBA_D<24>	4.1F 4.2A 8.3A 8.4B
FBA_D<25>	4.1F 4.2A 8.3A 8.4B
FBA_D<26>	4.1F 4.2A 8.3A 8.4B
FBA_D<27>	4.2A 4.2F 8.3A 8.4B
FBA_D<28>	4.2A 4.2F 8.3A 8.4B
FBA_D<29>	4.2A 4.2F 8.3A 8.4B
FBA_D<30>	4.2A 4.2F 8.3A 8.4B
FBA_D<31>	4.2A 4.2F 8.3A 8.4B
FBA_D<32>	4.1B 4.2F 8.3A 8.3C
FBA_D<33>	4.1B 4.2F 8.3A 8.3C
FBA_D<34>	4.1B 4.2F 8.3A 8.3C
FBA_D<35>	4.1B 4.2F 8.3A 8.3C
FBA_D<36>	4.1B 4.2F 8.3A 8.4C
FBA_D<37>	4.1B 4.2F 8.4A 8.4C
FBA_D<38>	4.1B 4.2F 8.4A 8.4C
FBA_D<39>	4.1B 4.2F 8.4A 8.4C
FBA_D<40>	4.1B 4.2F 8.3C 8.4A
FBA_D<41>	4.1B 4.2F 8.3C 8.4A
FBA_D<42>	4.1B 4.2F 8.3C 8.4A
FBA_D<43>	4.1B 4.2F 8.3C 8.4A
FBA_D<44>	4.1B 4.2F 8.4A 8.4C
FBA_D<45>	4.1B 4.2F 8.4A 8.4C
FBA_D<46>	4.1B 4.2F 8.4A 8.4C
FBA_D<47>	4.2B 4.2F 8.4A 8.4C
FBA_D<48>	4.2B 4.2F 8.4A 8.4C
FBA_D<49>	4.2B 4.2F 8.4A 8.4C
FBA_D<50>	4.2B 4.2F 8.4A 8.4C
FBA_D<51>	4.2B 4.2F 8.4A 8.4C
FBA_D<52>	4.2B 4.2F 8.4A 8.4C
FBA_D<53>	4.2B 4.2F 8.4A 8.4C
FBA_D<54>	4.2B 4.2F 8.4A 8.4C
FBA_D<55>	4.2B 4.2F 8.4A 8.4C
FBA_D<56>	4.2B 4.2F 8.4A 8.4C
FBA_D<57>	4.2B 4.3F 8.4A 8.4C
FBA_D<58>	4.2B 4.3F 8.4A 8.4C
FBA_D<59>	4.2B 4.3F 8.4A 8.4C
FBA_D<60>	4.2B 4.3F 8.4A 8.4C
FBA_D<61>	4.2B 4.3F 8.4A 8.4C
FBA_D<62>	4.2B 4.3F 8.4A 8.4C
FBA_D<63>	4.2B 4.3F 8.4A 8.4C
FBA_DEBUG	4.3B
FBA_DQM0	4.2A 4.3G<> 8.4A<>
	8.4A
FBA_DQM1	4.2A 4.3G<> 8.4B
	8.5A<>
FBA_DQM2	4.2A 4.3G<> 8.4A
	8.5A<>
FBA_DQM3	4.2A 4.3G<> 8.4B
	8.5A<>
FBA_DQM4	4.2B 4.3G<> 8.4C
	8.5A<>
FBA_DQM5	4.2B 4.3G<> 8.4C
	8.5A<>
FBA_DQM6	4.2B 4.3G<> 8.4C
	8.5A<>
FBA_DQM7	4.2B 4.3G<> 8.4C
	8.5A<>
FBA_DQS_RN0	4.2A 4.3G< 8.4A 8.5A<
FBA_DQS_RN1	4.2A 4.3G< 8.4B 8.5A<
FBA_DQS_RN2	4.2A 4.3G< 8.4A 8.5A<
FBA_DQS_RN3	4.2A 4.3G< 8.4B 8.5A<
FBA_DQS_RN4	4.2B 4.3G< 8.4C 8.5A<
FBA_DQS_RN5	4.2B 4.3G< 8.4C 8.5A<
FBA_DQS_RN6	4.2B 4.3G< 8.4C 8.5A<
FBA_DQS_RN7	4.2B 4.3G< 8.4C 8.5A<
FBA_DQS_WP0	4.2A 4.3G> 8.4A 8.5A>
FBA_DQS_WP1	4.3A 4.3G> 8.4B 8.5A>
FBA_DQS_WP2	4.3A 4.3G> 8.4A 8.5A>
FBA_DQS_WP3	4.3A 4.4G> 8.4B 8.5A>
FBA_DQS_WP4	4.2B 4.4G> 8.4C 8.5A>
FBA_DQS_WP5	4.3B 4.4G> 8.4C 8.5A>
FBA_DQS_WP6	4.3B 4.4G> 8.4C 8.5A>
FBA_DQS_WP7	4.3B 4.4G> 8.4C 8.5A>
FBA_SEN1	8.2A
FBA_SEN2	8.2C
FBA_VREF1	8.1H 8.3B
FBA_VREF2	8.2H 8.3B
FBA_VREF3	8.2H 8.3D
FBA_VREF4	8.3D 8.3H
FBA_ZQ1	8.2A
FBA_ZQ2	8.2C
FBB0_CLK0	4.4C 4.5H> 9.2A< 9.2A
	9.4G

FBB0_CLK0*	4.4C 4.5H> 9.2A< 9.2A
	9.4G
FBB0_CLK0_R	9.4H
FBB1_CLK0	4.4E 4.5H> 9.2A< 9.2C
	9.4G
FBB1_CLK0*	4.4E 4.5H> 9.2A< 9.2C
	9.4G
FBB1_CLK0_R	9.4H
FBB_CMD<0>	4.3D 4.4G 9.1A 9.1A
	9.5A
FBB_CMD<0..28>	4.4H> 9.1A<
FBB_CMD<1>	4.3D 4.4G 9.1A 9.1A
	9.5A
FBB_CMD<2>	4.3D 4.4G 9.1A 9.1A
	9.5A
FBB_CMD<3>	4.3D 4.4G 9.1A 9.1A
	9.5A
FBB_CMD<4>	4.3D 4.4G 9.1A 9.1A
	9.5A
FBB_CMD<5>	4.3D 4.4G 9.1A 9.1A
	9.5A
FBB_CMD<6>	4.3D 4.4G 9.1A 9.2A
	9.2C 9.5F
FBB_CMD<7>	4.3D 4.4G 9.1A 9.1A
	9.1C
FBB_CMD<8>	4.3D 4.4G 9.1A 9.2A
	9.2C
FBB_CMD<9>	4.3D 4.4G 9.1A 9.1A
	9.1C
FBB_CMD<10>	4.3D 4.4G 9.1A 9.2A
	9.2C 9.5F
FBB_CMD<11>	4.3D 4.4G 9.1A 9.2A
	9.2C
FBB_CMD<12>	4.3D 4.4G 9.1A 9.1A
	9.1C
FBB_CMD<13>	4.3D 4.4G 9.1A 9.2A
	9.2C
FBB_CMD<14>	4.3D 4.4G 9.1A 9.1A
	9.1C
FBB_CMD<15>	4.3D 4.4G 9.1A 9.2A
	9.2C
FBB_CMD<16>	4.3D 4.4G 9.1A 9.1A
	9.1C
FBB_CMD<17>	4.3D 4.4G 9.1A 9.1A
	9.1C
FBB_CMD<18>	4.3D 4.4G 9.1A 9.1A
	9.1C
FBB_CMD<19>	4.3D 4.4G 9.1A 9.1A
	9.1C
FBB_CMD<20>	4.3D 4.4G 9.1A 9.1C
	9.2A
FBB_CMD<21>	4.3D 4.4G 9.1A 9.1C
	9.2A
FBB_CMD<23>	4.3D 4.4G 9.1C 9.2A
	9.5C
FBB_CMD<24>	4.3D 4.5G 9.1C 9.2A
	9.5C
FBB_CMD<25>	4.4D 4.5G 9.1C 9.2A
	9.5C
FBB_CMD<26>	4.4D 4.5G 9.1C 9.2A
	9.5C
FBB_CMD<27>	4.4D 4.5G 9.1C 9.2A
	9.5C
FBB_CMD<28>	4.4D 4.5G 9.1C 9.2A
	9.5C
FBB_D<0>	4.1D 4.1G 9.2A 9.3A
FBB_D<0..63>	4.1H> 9.2A<>
FBB_D<1>	4.1D 4.1G 9.2A 9.3A
FBB_D<2>	4.1D 4.1G 9.2A 9.3A
FBB_D<3>	4.1D 4.1G 9.2A 9.3A
FBB_D<4>	4.1D 4.1G 9.2A 9.4A
FBB_D<5>	4.1D 4.1G 9.2A 9.4A
FBB_D<6>	4.1D 4.1G 9.2A 9.4A
FBB_D<7>	4.1D 4.1G 9.3A 9.4A
FBB_D<8>	4.1D 4.1G 9.3A 9.3B
FBB_D<9>	4.1D 4.1G 9.3A 9.3B
FBB_D<10>	4.1D 4.1G 9.3A 9.3B
FBB_D<11>	4.1D 4.1G 9.3A 9.3B
FBB_D<12>	4.1D 4.1G 9.3A 9.4B
FBB_D<13>	4.1D 4.1G 9.3A 9.4B
FBB_D<14>	4.1D 4.1G 9.3A 9.4B
FBB_D<15>	4.1G 4.2D 9.3A 9.4B
FBB_D<16>	4.1G 4.2D 9.3A 9.4A
FBB_D<17>	4.1G 4.2D 9.3A 9.4A
FBB_D<18>	4.1G 4.2D 9.3A 9.4A
FBB_D<19>	4.1G 4.2D 9.3A 9.4A
FBB_D<20>	4.1G 4.2D 9.3A 9.4A
FBB_D<21>	4.1G 4.2D 9.3A 9.4A
FBB_D<22>	4.1G 4.2D 9.3A 9.4A
FBB_D<23>	4.1G 4.2D 9.3A 9.4A
FBB_D<24>	4.1G 4.2D 9.3A 9.4B
FBB_D<25>	4.1G 4.2D 9.3A 9.4B
FBB_D<26>	4.1G 4.2D 9.3A 9.4B
FBB_D<27>	4.2D 4.2G 9.3A 9.4B
FBB_D<28>	4.2D 4.2G 9.3A 9.4B
FBB_D<29>	4.2D 4.2G 9.3A 9.4B

FBB_D<30>	4.2D 4.2G 9.3A 9.4B
FBB_D<31>	4.2D 4.2G 9.3A 9.4B
FBB_D<32>	4.1E 4.2G 9.3A 9.3C
FBB_D<33>	4.1E 4.2G 9.3A 9.3C
FBB_D<34>	4.1E 4.2G 9.3A 9.3C
FBB_D<35>	4.1E 4.2G 9.3A 9.3C
FBB_D<36>	4.1E 4.2G 9.3A 9.4C
FBB_D<37>	4.1E 4.2G 9.4A 9.4C
FBB_D<38>	4.1E 4.2G 9.4A 9.4C
FBB_D<39>	4.1E 4.2G 9.4A 9.4C
FBB_D<40>	4.1E 4.2G 9.3C 9.4A
FBB_D<41>	4.1E 4.2G 9.3C 9.4A
FBB_D<42>	4.1E 4.2G 9.3C 9.4A
FBB_D<43>	4.1E 4.2G 9.3C 9.4A
FBB_D<44>	4.1E 4.2G 9.4A 9.4C
FBB_D<45>	4.1E 4.2G 9.4A 9.4C
FBB_D<46>	4.1E 4.2G 9.4A 9.4C
FBB_D<47>	4.2E 4.2G 9.4A 9.4C
FBB_D<48>	4.2E 4.2G 9.4A 9.4C
FBB_D<49>	4.2E 4.2G 9.4A 9.4C
FBB_D<50>	4.2E 4.2G 9.4A 9.4C
FBB_D<51>	4.2E 4.2G 9.4A 9.4C
FBB_D<52>	4.2E 4.2G 9.4A 9.4C
FBB_D<53>	4.2E 4.2G 9.4A 9.4C
FBB_D<54>	4.2E 4.2G 9.4A 9.4C
FBB_D<55>	4.2E 4.2G 9.4A 9.4C
FBB_D<56>	4.2E 4.2G 9.4A 9.4C
FBB_D<57>	4.2E 4.3G 9.4A 9.4C
FBB_D<58>	4.2E 4.3G 9.4A 9.4C
FBB_D<59>	4.2E 4.3G 9.4A 9.4C
FBB_D<60>	4.2E 4.3G 9.4A 9.4C
FBB_D<61>	4.2E 4.3G 9.4A 9.4C
FBB_D<62>	4.2E 4.3G 9.4A 9.4C
FBB_D<63>	4.2E 4.3G 9.4A 9.4C
FBB_DEBUG	4.3E
FBB_DQM0	4.2D 4.3H<> 9.4A<>
	9.4A
FBB_DQM1	4.2D 4.3H<> 9.4B
	9.5A<>
FBB_DQM2	4.2D 4.3H<> 9.4A
	9.5A<>
FBB_DQM3	4.2D 4.3H<> 9.4B
	9.5A<>
FBB_DQM4	4.2E 4.3H<> 9.4C
	9.5A<>
FBB_DQM5	4.2E 4.3H<> 9.4C
	9.5A<>
FBB_DQM6	4.2E 4.3H<> 9.4C
	9.5A<>
FBB_DQM7	4.2E 4.3H<> 9.4C
	9.5A<>
FBB_DQS_RN0	4.2D 4.3H< 9.4A 9.5A<
FBB_DQS_RN1	4.2D 4.3H< 9.4B 9.5A<
FBB_DQS_RN2	4.2D 4.3H< 9.4A 9.5A<
FBB_DQS_RN3	4.2D 4.3H< 9.4B 9.5A<
FBB_DQS_RN4	4.2E 4.3H< 9.4C 9.5A<
FBB_DQS_RN5	4.2E 4.3H< 9.4C 9.5A<
FBB_DQS_RN6	4.2E 4.3H< 9.4C 9.5A<
FBB_DQS_RN7	4.2E 4.3H< 9.4C 9.5A<
FBB_DQS_WP0	4.2D 4.3H> 9.4A 9.5A>
FBB_DQS_WP1	4.3D 4.3H> 9.4B 9.5A>
FBB_DQS_WP2	4.3D 4.3H> 9.4A 9.5A>
FBB_DQS_WP3	4.3D 4.4H> 9.4B 9.5A>
FBB_DQS_WP4	4.2E 4.4H> 9.4C 9.5A>
FBB_DQS_WP5	4.3E 4.4H> 9.4C 9.5A>
FBB_DQS_WP6	4.3E 4.4H> 9.4C 9.5A>
FBB_DQS_WP7	4.3E 4.4H> 9.4C 9.5A>
FBB_SEN1	9.2A
FBB_SEN2	9.2C
FBB_VREF1	9.1H 9.3B
FBB_VREF2	9.2H 9.3B
FBB_VREF3	9.2H 9.3D
FBB_VREF4	9.3D 9.3H
FBB_ZQ1	9.2A
FBB_ZQ2	9.2C
FBC0_CLK0	5.4A 5.5G> 10.2A<
	10.2A 10.4G
FBC0_CLK0*	5.4A 5.5G> 10.2A<
	10.2A 10.4G
FBC0_CLK0_R	10.4H
FBC1_CLK0	5.4B 5.5G> 10.2A<
	10.2C 10.4G
FBC1_CLK0*	5.4B 5.5G> 10.2A<
	10.2C 10.4G
FBC1_CLK0_R	10.4H
FBCD_REFCLK	5.3C< 18.5D>
FBCD_REFCLK*	5.3C< 18.5D>
FBC_CMD<0>	5.3A 5.4F 10.1A 10.1A
	10.5A
FBC_CMD<0..28>	5.4G> 10.1A<
FBC_CMD<1>	5.3A 5.4F 10.1A 10.1A
	10.5A
FBC_CMD<2>	5.3A 5.4F 10.1A 10.1A
	10.5A
FBC_CMD<3>	5.3A 5.4F 10.1A 10.1A
	10.5A

FBC_CMD<4>	5.3A 5.4F 10.1A 10.1A
	10.5A
FBC_CMD<5>	5.3A 5.4F 10.1A 10.1A
	10.5A
FBC_CMD<6>	5.3A 5.4F 10.1A 10.2A
	10.2C 10.5F
FBC_CMD<7>	5.3A 5.4F 10.1A 10.1A
	10.1C
FBC_CMD<8>	5.3A 5.4F 10.1A 10.2A
	10.2C
FBC_CMD<9>	5.3A 5.4F 10.1A 10.1A
	10.1C
FBC_CMD<10>	5.3A 5.4F 10.1A 10.2A
	10.2C 10.5F
FBC_CMD<11>	5.4A 5.4F 10.1A 10.2A
	10.2C
FBC_CMD<12>	5.4A 5.4F 10.1A 10.1A
	10.1C
FBC_CMD<13>	5.4A 5.4F 10.1A 10.2A
	10.2C
FBC_CMD<14>	5.4A 5.4F 10.1A 10.1A
	10.1C
FBC_CMD<15>	5.4A 5.4F 10.1A 10.2A
	10.2C
FBC_CMD<16>	5.4A 5.4F 10.1A 10.1A
	10.1C
FBC_CMD<17>	5.4A 5.4F 10.1A 10.1A
	10.1C
FBC_CMD<18>	5.4A 5.4F 10.1A 10.1A
	10.1C
FBC_CMD<19>	5.4A 5.4F 10.1A 10.1A
	10.1C
FBC_CMD<20>	5.4A 5.4F 10.1A 10.1C
	10.2A
FBC_CMD<21>	5.4A 5.4F 10.1A 10.1C
	10.2A
FBC_CMD<23>	5.4A 5.4F 10.1C 10.2A
	10.5C
FBC_CMD<24>	5.4A 5.5F 10.1C 10.2A
	10.5C
FBC_CMD<25>	5.4A 5.5F 10.1C 10.2A
	10.5C
FBC_CMD<26>	5.4A 5.5F 10.1C 10.2A
	10.5C
FBC_CMD<27>	5.4A 5.5F 10.1C 10.2A
	10.5C
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FBC_D<3>	5.1F 5.2A 10.2A 10.3A
FBC_D<4>	5.1F 5.2A 10.2A 10.4A
FBC_D<5>	5.1F 5.2A 10.2A 10.4A
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FBC_D<7>	5.1F 5.2A 10.3A 10.4A
FBC_D<8>	5.1F 5.2A 10.3A 10.3B
FBC_D<9>	5.1F 5.2A 10.3A 10.3B
FBC_D<10>	5.1F 5.2A 10.3A 10.3B
FBC_D<11>	5.1F 5.2A 10.3A 10.3B
FBC_D<12>	5.1F 5.2A 10.3A 10.4B
FBC_D<13>	5.1F 5.2A 10.3A 10.4B
FBC_D<14>	5.1F 5.2A 10.3A 10.4B
FBC_D<15>	5.1F 5.2A 10.3A 10.4B
FBC_D<16>	5.1F 5.2A 10.3A 10.4A
FBC_D<17>	5.1F 5.2A 10.3A 10.4A
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FBC_D<19>	5.1F 5.2A 10.3A 10.4A
FBC_D<20>	5.1F 5.2A 10.3A 10.4A
FBC_D<21>	5.1F 5.2A 10.3A 10.4A
FBC_D<22>	5.1F 5.2A 10.3A 10.4A
FBC_D<23>	5.1F 5.2A 10.3A 10.4A
FBC_D<24>	5.1F 5.2A 10.3A 10.4B
FBC_D<25>	5.1F 5.2A 10.3A 10.4B
FBC_D<26>	5.1F 5.2A 10.3A 10.4B
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FBC_D<28>	5.2A 5.2F 10.3A 10.4B
FBC_D<29>	5.2A 5.2F 10.3A 10.4B
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FBC_D<31>	5.2F 5.3A 10.3A 10.4B
FBC_D<32>	5.1B 5.2F 10.3A 10.3C
FBC_D<33>	5.2B 5.2F 10.3A 10.3C
FBC_D<34>	5.2B 5.2F 10.3A 10.3C
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FBC_D<46>	5.2B 5.2F 10.4A 10.4C

FBC_D<47>	5.2B 5.2F 10.4A 10.4C
FBC_D<48>	5.2B 5.2F 10.4A 10.4C
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FBC_D<50>	5.2B 5.2F 10.4A 10.4C
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FBC_D<53>	5.2B 5.2F 10.4A 10.4C
FBC_D<54>	5.2B 5.2F 10.4A 10.4C
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FBC_D<58>	5.2B 5.3F 10.4A 10.4C
FBC_D<59>	5.2B 5.3F 10.4A 10.4C
FBC_D<60>	5.2B 5.3F 10.4A 10.4C
FBC_D<61>	5.2B 5.3F 10.4A 10.4C
FBC_D<62>	5.2B 5.3F 10.4A 10.4C
FBC_D<63>	5.3B 5.3F 10.4A 10.4C
FBC_DEBUG	5.3B
FBC_DQM0	5.3A 5.3G<> 10.4A<>
	10.4A
FBC_DQM1	5.3A 5.3G<> 10.4B
	10.5A<>
FBC_DQM2	5.3A 5.3G<> 10.4A
	10.5A<>
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	10.5A<>
FBC_DQM4	5.3B 5.3G<> 10.4C
	10.5A<>
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	10.5A<>
FBC_DQM7	5.3B 5.3G<> 10.4C
	10.5A<>
FBC_DQS_RN0	5.3A 5.3G< 10.4A
	10.5A<
FBC_DQS_RN1	5.3A 5.3G< 10.4B
	10.5A<
FBC_DQS_RN2	5.3A 5.3G< 10.4A
	10.5A<
FBC_DQS_RN3	5.3A 5.3G< 10.4B
	10.5A<
FBC_DQS_RN4	5.3B 5.3G< 10.4C
	10.5A<
FBC_DQS_RN5	5.3B 5.3G< 10.4C
	10.5A<
FBC_DQS_RN6	5.3B 5.3G< 10.4C
	10.5A<
FBC_DQS_RN7	5.3B 5.3G< 10.4C
	10.5A<
FBC_DQS_WP0	5.3A 5.3G> 10.4A
	10.5A>
FBC_DQS_WP1	5.3A 5.3G> 10.4B
	10.5A>
FBC_DQS_WP2	5.3A 5.3G> 10.4A
	10.5A>
FBC_DQS_WP3	5.3A 5.4G> 10.4B
	10.5A>
FBC_DQS_WP4	5.3B 5.4G> 10.4C
	10.5A>
FBC_DQS_WP5	5.3B 5.4G> 10.4C
	10.5A>
FBC_DQS_WP6	5.3B 5.4G> 10.4C
	10.5A>
FBC_DQS_WP7	5.3B 5.4G> 10.4C
	10.5A>
FBC_SEN1	10.2A
FBC_SEN2	10.2C
FBC_VREF1	10.1H 10.3B
FBC_VREF2	10.2H 10.3B
FBC_VREF3	10.2H 10.3D
FBC_VREF4	10.3D 10.3H
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FBC_ZQ2	10.2C
FBD0_CLK0	5.4C 5.5H> 11.2A<
	11.2A 11.4G
FBD0_CLK0*	5.4C 5.5H> 11.2A<
	11.2A 11.4G
FBD0_CLK0_R	11.4H
FBD1_CLK0	5.4E 5.5H> 11.2A<
	11.2C 11.4G
FBD1_CLK0*	5.4E 5.5H> 11.2A<
	11.2C 11.4G
FBD1_CLK0_R	11.4H
FBD_CMD<0>	5.3D 5.4G 11.1A 11.1A
	11.5A
FBD_CMD<0..28>	5.4H> 11.1A<
FBD_CMD<1>	5.3D 5.4G 11.1A 11.1A
	11.5A
FBD_CMD<2>	5.3D 5.4G 11.1A 11.1A
	11.5A
FBD_CMD<3>	5.3D 5.4G 11.1A 11.1A
	11.5A
FBD_CMD<4>	5.3D 5.4G 11.1A 11.1A
	11.5A
FBD_CMD<5>	5.3D 5.4G 11.1A 11.1A

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
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2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10897-0053-300 A		
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NAME	misun	DATE	31-DEC-2008

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	11.2C 11.5F
FBD_CMD<7>	5.3D 5.4G 11.1A 11.1A
	11.1C
FBD_CMD<8>	5.3D 5.4G 11.1A 11.2A
	11.2C
FBD_CMD<9>	5.3D 5.4G 11.1A 11.1A
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	11.2C 11.5F
FBD_CMD<11>	5.4D 5.4G 11.1A 11.2A
	11.2C
FBD_CMD<12>	5.4D 5.4G 11.1A 11.1A
	11.1C
FBD_CMD<13>	5.4D 5.4G 11.1A 11.2A
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FBD_CMD<14>	5.4D 5.4G 11.1A 11.1A
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FBD_CMD<15>	5.4D 5.4G 11.1A 11.2A
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FBD_CMD<16>	5.4D 5.4G 11.1A 11.1A
	11.1C
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FBD_CMD<18>	5.4D 5.4G 11.1A 11.1A
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FBD_CMD<19>	5.4D 5.4G 11.1A 11.1A
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FBD_CMD<20>	5.4D 5.4G 11.1A 11.1C
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FBD_CMD<21>	5.4D 5.4G 11.1A 11.1C
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FBD_CMD<23>	5.4D 5.4G 11.1C 11.2A
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FBD_CMD<25>	5.4D 5.5G 11.1C 11.2A
	11.5C
FBD_CMD<26>	5.4D 5.5G 11.1C 11.2A
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FBD_CMD<27>	5.4D 5.5G 11.1C 11.2A
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FBD_CMD<28>	5.4D 5.5G 11.1C 11.2A
	11.5C
FBD_D<0>	5.1D 5.1G 11.2A 11.3A
FBD_D<0..63>	5.1H> 11.2A<>
FBD_D<1>	5.1G 5.2D 11.2A 11.3A
FBD_D<2>	5.1G 5.2D 11.2A 11.3A
FBD_D<3>	5.1G 5.2D 11.2A 11.3A
FBD_D<4>	5.1G 5.2D 11.2A 11.4A
FBD_D<5>	5.1G 5.2D 11.2A 11.4A
FBD_D<6>	5.1G 5.2D 11.2A 11.4A
FBD_D<7>	5.1G 5.2D 11.3A 11.4A
FBD_D<8>	5.1G 5.2D 11.3A 11.3B
FBD_D<9>	5.1G 5.2D 11.3A 11.3B
FBD_D<10>	5.1G 5.2D 11.3A 11.3B
FBD_D<11>	5.1G 5.2D 11.3A 11.3B
FBD_D<12>	5.1G 5.2D 11.3A 11.4B
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FBD_D<34>	5.2E 5.2G 11.3A 11.3C
FBD_D<35>	5.2E 5.2G 11.3A 11.3C
FBD_D<36>	5.2E 5.2G 11.3A 11.4C
FBD_D<37>	5.2E 5.2G 11.4A 11.4C
FBD_D<38>	5.2E 5.2G 11.4A 11.4C
FBD_D<39>	5.2E 5.2G 11.4A 11.4C
FBD_D<40>	5.2E 5.2G 11.3C 11.4A
FBD_D<41>	5.2E 5.2G 11.3C 11.4A
FBD_D<42>	5.2E 5.2G 11.3C 11.4A
FBD_D<43>	5.2E 5.2G 11.3C 11.4A
FBD_D<44>	5.2E 5.2G 11.4A 11.4C
FBD_D<45>	5.2E 5.2G 11.4A 11.4C
FBD_D<46>	5.2E 5.2G 11.4A 11.4C
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FBD_D<54>	5.2E 5.2G 11.4A 11.4C
FBD_D<55>	5.2E 5.2G 11.4A 11.4C
FBD_D<56>	5.2E 5.2G 11.4A 11.4C
FBD_D<57>	5.2E 5.3G 11.4A 11.4C
FBD_D<58>	5.2E 5.3G 11.4A 11.4C
FBD_D<59>	5.2E 5.3G 11.4A 11.4C
FBD_D<60>	5.2E 5.3G 11.4A 11.4C
FBD_D<61>	5.2E 5.3G 11.4A 11.4C
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	11.4A
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	11.5A<>
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	11.5A<>
FBD_DQM7	5.3E 5.3H<> 11.4C
	11.5A<>
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	11.5A<
FBD_DQS_RN1	5.3D 5.3H< 11.4B
	11.5A<
FBD_DQS_RN2	5.3D 5.3H< 11.4A
	11.5A<
FBD_DQS_RN3	5.3D 5.3H< 11.4B
	11.5A<
FBD_DQS_RN4	5.3E 5.3H< 11.4C
	11.5A<
FBD_DQS_RN5	5.3E 5.3H< 11.4C
	11.5A<
FBD_DQS_RN6	5.3E 5.3H< 11.4C
	11.5A<
FBD_DQS_RN7	5.3E 5.3H< 11.4C
	11.5A<
FBD_DQS_WP0	5.3D 5.3H> 11.4A
	11.5A>
FBD_DQS_WP1	5.3D 5.3H> 11.4B
	11.5A>
FBD_DQS_WP2	5.3D 5.3H> 11.4A
	11.5A>
FBD_DQS_WP3	5.3D 5.4H> 11.4B
	11.5A>
FBD_DQS_WP4	5.3E 5.4H> 11.4C
	11.5A>
FBD_DQS_WP5	5.3E 5.4H> 11.4C
	11.5A>
FBD_DQS_WP6	5.3E 5.4H> 11.4C
	11.5A>
FBD_DQS_WP7	5.3E 5.4H> 11.4C
	11.5A>
FBD_SEN1	11.2A
FBD_SEN2	11.2C
FBD_VREF1	11.1H 11.3B
FBD_VREF2	11.2H 11.3B
FBD_VREF3	11.2H 11.3D
FBD_VREF4	11.3D 11.3H
FBD_ZQ1	11.2A
FBD_ZQ2	11.2C
FBE0_CLK0	6.4A 6.5G> 12.2A<
	12.2A 12.4G
FBE0_CLK0*	6.4A 6.5G> 12.2A<
	12.2A 12.4G
FBE0_CLK0_R	12.4H
FBE1_CLK0	6.4B 6.5G> 12.2A<
	12.2C 12.4G
FBE1_CLK0*	6.4B 6.5G> 12.2A<
	12.2C 12.4G
FBE1_CLK0_R	12.4H
FBEFGH_MPLL_AVDD	6.4C> 7.4C<
FBEF_REFCLK	6.3C< 18.5D>
FBEF_REFCLK*	6.3C< 18.5D>
FBE_CMD<0>	6.3A 6.4F 12.1A 12.1A
	12.5A
FBE_CMD<0..28>	6.4G> 12.1A<
FBE_CMD<1>	6.3A 6.4F 12.1A 12.1A
	12.5A
FBE_CMD<2>	6.3A 6.4F 12.1A 12.1A
	12.5A
FBE_CMD<3>	6.3A 6.4F 12.1A 12.1A
	12.5A
FBE_CMD<4>	6.3A 6.4F 12.1A 12.1A
	12.5A
FBE_CMD<5>	6.3A 6.4F 12.1A 12.1A

	12.5A
FBE_CMD<6>	6.3A 6.4F 12.1A 12.2A
	12.2C 12.5F
FBE_CMD<7>	6.3A 6.4F 12.1A 12.1A
	12.1C
FBE_CMD<8>	6.3A 6.4F 12.1A 12.2A
	12.2C
FBE_CMD<9>	6.3A 6.4F 12.1A 12.1A
	12.1C
FBE_CMD<10>	6.3A 6.4F 12.1A 12.2A
	12.2C 12.5F
FBE_CMD<11>	6.4A 6.4F 12.1A 12.2A
	12.2C
FBE_CMD<12>	6.4A 6.4F 12.1A 12.1A
	12.1C
FBE_CMD<13>	6.4A 6.4F 12.1A 12.2A
	12.2C
FBE_CMD<14>	6.4A 6.4F 12.1A 12.1A
	12.1C
FBE_CMD<15>	6.4A 6.4F 12.1A 12.2A
	12.2C
FBE_CMD<16>	6.4A 6.4F 12.1A 12.1A
	12.1C
FBE_CMD<17>	6.4A 6.4F 12.1A 12.1A
	12.1C
FBE_CMD<18>	6.4A 6.4F 12.1A 12.1A
	12.1C
FBE_CMD<19>	6.4A 6.4F 12.1A 12.1A
	12.1C
FBE_CMD<20>	6.4A 6.4F 12.1A 12.1C
	12.2A
FBE_CMD<21>	6.4A 6.4F 12.1A 12.1C
	12.2A
FBE_CMD<23>	6.4A 6.4F 12.1C 12.2A
	12.5C
FBE_CMD<24>	6.4A 6.5F 12.1C 12.2A
	12.5C
FBE_CMD<25>	6.4A 6.5F 12.1C 12.2A
	12.5C
FBE_CMD<26>	6.4A 6.5F 12.1C 12.2A
	12.5C
FBE_CMD<27>	6.4A 6.5F 12.1C 12.2A
	12.5C
FBE_CMD<28>	6.4A 6.5F 12.1C 12.2A
	12.5C
FBE_D<0>	6.1A 6.1F 12.2A 12.3A
FBE_D<0..63>	6.1G> 12.2A<>
FBE_D<1>	6.1F 6.2A 12.2A 12.3A
FBE_D<2>	6.1F 6.2A 12.2A 12.3A
FBE_D<3>	6.1F 6.2A 12.2A 12.3A
FBE_D<4>	6.1F 6.2A 12.2A 12.4A
FBE_D<5>	6.1F 6.2A 12.2A 12.4A
FBE_D<6>	6.1F 6.2A 12.2A 12.4A
FBE_D<7>	6.1F 6.2A 12.3A 12.4A
FBE_D<8>	6.1F 6.2A 12.3A 12.3B
FBE_D<9>	6.1F 6.2A 12.3A 12.3B
FBE_D<10>	6.1F 6.2A 12.3A 12.3B
FBE_D<11>	6.1F 6.2A 12.3A 12.3B
FBE_D<12>	6.1F 6.2A 12.3A 12.4B
FBE_D<13>	6.1F 6.2A 12.3A 12.4B
FBE_D<14>	6.1F 6.2A 12.3A 12.4B
FBE_D<15>	6.1F 6.2A 12.3A 12.4B
FBE_D<16>	6.1F 6.2A 12.3A 12.4A
FBE_D<17>	6.1F 6.2A 12.3A 12.4A
FBE_D<18>	6.1F 6.2A 12.3A 12.4A
FBE_D<19>	6.1F 6.2A 12.3A 12.4A
FBE_D<20>	6.1F 6.2A 12.3A 12.4A
FBE_D<21>	6.1F 6.2A 12.3A 12.4A
FBE_D<22>	6.1F 6.2A 12.3A 12.4A
FBE_D<23>	6.1F 6.2A 12.3A 12.4A
FBE_D<24>	6.1F 6.2A 12.3A 12.4B
FBE_D<25>	6.1F 6.2A 12.3A 12.4B
FBE_D<26>	6.1F 6.2A 12.3A 12.4B
FBE_D<27>	6.2A 6.2F 12.3A 12.4B
FBE_D<28>	6.2A 6.2F 12.3A 12.4B
FBE_D<29>	6.2A 6.2F 12.3A 12.4B
FBE_D<30>	6.2A 6.2F 12.3A 12.4B
FBE_D<31>	6.2F 6.3A 12.3A 12.4B
FBE_D<32>	6.1B 6.2F 12.3A 12.3C
FBE_D<33>	6.2B 6.2F 12.3A 12.3C
FBE_D<34>	6.2B 6.2F 12.3A 12.3C
FBE_D<35>	6.2B 6.2F 12.3A 12.3C
FBE_D<36>	6.2B 6.2F 12.3A 12.4C
FBE_D<37>	6.2B 6.2F 12.4A 12.4C
FBE_D<38>	6.2B 6.2F 12.4A 12.4C
FBE_D<39>	6.2B 6.2F 12.4A 12.4C
FBE_D<40>	6.2B 6.2F 12.3C 12.4A
FBE_D<41>	6.2B 6.2F 12.3C 12.4A
FBE_D<42>	6.2B 6.2F 12.3C 12.4A
FBE_D<43>	6.2B 6.2F 12.3C 12.4A
FBE_D<44>	6.2B 6.2F 12.4A 12.4C
FBE_D<45>	6.2B 6.2F 12.4A 12.4C
FBE_D<46>	6.2B 6.2F 12.4A 12.4C
FBE_D<47>	6.2B 6.2F 12.4A 12.4C
FBE_D<48>	6.2B 6.2F 12.4A 12.4C
FBE_D<49>	6.2B 6.2F 12.4A 12.4C

FBE_D<50>	6.2B 6.2F 12.4A 12.4C
FBE_D<51>	6.2B 6.2F 12.4A 12.4C
FBE_D<52>	6.2B 6.2F 12.4A 12.4C
FBE_D<53>	6.2B 6.2F 12.4A 12.4C
FBE_D<54>	6.2B 6.2F 12.4A 12.4C
FBE_D<55>	6.2B 6.2F 12.4A 12.4C
FBE_D<56>	6.2B 6.2F 12.4A 12.4C
FBE_D<57>	6.2B 6.3F 12.4A 12.4C
FBE_D<58>	6.2B 6.3F 12.4A 12.4C
FBE_D<59>	6.2B 6.3F 12.4A 12.4C
FBE_D<60>	6.2B 6.3F 12.4A 12.4C
FBE_D<61>	6.2B 6.3F 12.4A 12.4C
FBE_D<62>	6.2B 6.3F 12.4A 12.4C
FBE_D<63>	6.3B 6.3F 12.4A 12.4C
FBE_DEBUG	6.3B
FBE_DQM0	6.3A 6.3G<> 12.4A<>
	12.4A
FBE_DQM1	6.3A 6.3G<> 12.4B
	12.5A<>
FBE_DQM2	6.3A 6.3G<> 12.4A
	12.5A<>
FBE_DQM3	6.3A 6.3G<> 12.4B
	12.5A<>
FBE_DQM4	6.3B 6.3G<> 12.4C
	12.5A<>
FBE_DQM5	6.3B 6.3G<> 12.4C
	12.5A<>
FBE_DQM6	6.3B 6.3G<> 12.4C
	12.5A<>
FBE_DQM7	6.3B 6.3G<> 12.4C
	12.5A<>
FBE_DQS_RN0	6.3A 6.3G< 12.4A
	12.5A<
FBE_DQS_RN1	6.3A 6.3G< 12.4B
	12.5A<
FBE_DQS_RN2	6.3A 6.3G< 12.4A
	12.5A<
FBE_DQS_RN3	6.3A 6.3G< 12.4B
	12.5A<
FBE_DQS_RN4	6.3B 6.3G< 12.4C
	12.5A<
FBE_DQS_RN5	6.3B 6.3G< 12.4C
	12.5A<
FBE_DQS_RN6	6.3B 6.3G< 12.4C
	12.5A<
FBE_DQS_RN7	6.3B 6.3G< 12.4C
	12.5A<
FBE_DQS_WP0	6.3A 6.3G> 12.4A
	12.5A>
FBE_DQS_WP1	6.3A 6.3G> 12.4B
	12.5A>
FBE_DQS_WP2	6.3A 6.3G> 12.4A
	12.5A>
FBE_DQS_WP3	6.3A 6.4G> 12.4B
	12.5A>
FBE_DQS_WP4	6.3B 6.4G> 12.4C
	12.5A>
FBE_DQS_WP5	6.3B 6.4G> 12.4C
	12.5A>
FBE_DQS_WP6	6.3B 6.4G> 12.4C
	12.5A>
FBE_DQS_WP7	6.3B 6.4G> 12.4C
	12.5A>
FBE_SEN1	12.2A
FBE_SEN2	12.2C
FBE_VREF1	12.1H 12.3B
FBE_VREF2	12.2H 12.3B
FBE_VREF3	12.2H 12.3D
FBE_VREF4	12.3D 12.3H
FBE_ZQ1	12.2A
FBE_ZQ2	12.2C
FBF0_CLK0	6.4C 6.5H> 13.2A<
	13.2A 13.4G
FBF0_CLK0*	6.4C 6.5H> 13.2A<
	13.2A 13.4G
FBF0_CLK0_R	13.4H
FBF1_CLK0	6.4E 6.5H> 13.2A<
	13.2C 13.4G
FBF1_CLK0*	6.4E 6.5H> 13.2A<
	13.2C 13.4G
FBF1_CLK0_R	13.4H
FBF_CMD<0>	6.3D 6.4G 13.1A 13.1A
	13.5A
FBF_CMD<0..28>	6.4H> 13.1A<
FBF_CMD<1>	6.3D 6.4G 13.1A 13.1A
	13.5A
FBF_CMD<2>	6.3D 6.4G 13.1A 13.1A
	13.5A
FBF_CMD<3>	6.3D 6.4G 13.1A 13.1A
	13.5A
FBF_CMD<4>	6.3D 6.4G 13.1A 13.1A
	13.5A
FBF_CMD<5>	6.3D 6.4G 13.1A 13.1A
	13.5A
FBF_CMD<6>	6.3D 6.4G 13.1A 13.2A
	13.2C 13.5F

FBF_CMD<7>	6.3D 6.4G 13.1A 13.1A
	13.1C
FBF_CMD<8>	6.3D 6.4G 13.1A 13.2A
	13.2C
FBF_CMD<9>	6.3D 6.4G 13.1A 13.1A
	13.1C
FBF_CMD<10>	6.3D 6.4G 13.1A 13.2A
	13.2C 13.5F
FBF_CMD<11>	6.4D 6.4G 13.1A 13.2A
	13.2C
FBF_CMD<12>	6.4D 6.4G 13.1A 13.1A
	13.1C
FBF_CMD<13>	6.4D 6.4G 13.1A 13.2A
	13.2C
FBF_CMD<14>	6.4D 6.4G 13.1A 13.1A
	13.1C
FBF_CMD<15>	6.4D 6.4G 13.1A 13.2A
	13.2C
FBF_CMD<16>	6.4D 6.4G 13.1A 13.1A
	13.1C
FBF_CMD<17>	6.4D 6.4G 13.1A 13.1A
	13.1C
FBF_CMD<18>	6.4D 6.4G 13.1A 13.1A
	13.1C
FBF_CMD<19>	6.4D 6.4G 13.1A 13.1A
	13.1C
FBF_CMD<20>	6.4D 6.4G 13.1A 13.1C
	13.2A
FBF_CMD<21>	6.4D 6.4G 13.1A 13.1C
	13.2A
FBF_CMD<23>	6.4D 6.4G 13.1C 13.2A
	13.5C
FBF_CMD<24>	6.4D 6.5G 13.1C 13.2A
	13.5C
FBF_CMD<25>	6.4D 6.5G 13.1C 13.2A
	13.5C
FBF_CMD<26>	6.4D 6.5G 13.1C 13.2A
	13.5C
FBF_CMD<27>	6.4D 6.5G 13.1C 13.2A
	13.5C
FBF_CMD<28>	6.4D 6.5G 13.1C 13.2A
	13.5C
FBF_D<0>	6.1D 6.1G 13.2A 13.3A
FBF_D<0..63>	6.1H> 13.2A<>
FBF_D<1>	6.1G 6.2D 13.2A 13.3A
FBF_D<2>	6.1G 6.2D 13.2A 13.3A
FBF_D<3>	6.1G 6.2D 13.2A 13.3A
FBF_D<4>	6.1G 6.2D 13.2A 13.4A
FBF_D<5>	6.1G 6.2D 13.2A 13.4A
FBF_D<6>	6.1G 6.2D 13.2A 13.4A
FBF_D<7>	6.1G 6.2D 13.3A 13.4A
FBF_D<8>	6.1G 6.2D 13.3A 13.3B
FBF_D<9>	6.1G 6.2D 13.3A 13.3B
FBF_D<10>	6.1G 6.2D 13.3A 13.3B
FBF_D<11>	6.1G 6.2D 13.3A 13.3B
FBF_D<12>	6.1G 6.2D 13.3A 13.4B
FBF_D<13>	6.1G 6.2D 13.3A 13.4B
FBF_D<14>	6.1G 6.2D 13.3A 13.4B
FBF_D<15>	6.1G 6.2D 13.3A 13.4B
FBF_D<16>	6.1G 6.2D 13.3A 13.4A
FBF_D<17>	6.1G 6.2D 13.3A 13.4A
FBF_D<18>	6.1G 6.2D 13.3A 13.4A
FBF_D<19>	6.1G 6.2D 13.3A 13.4A
FBF_D<20>	6.1G 6.2D 13.3A 13.4A
FBF_D<21>	6.1G 6.2D 13.3A 13.4A
FBF_D<22>	6.1G 6.2D 13.3A 13.4A
FBF_D<23>	6.1G 6.2D 13.3A 13.4A
FBF_D<24>	6.1G 6.2D 13.3A 13.4B
FBF_D<25>	6.1G 6.2D 13.3A 13.4B
FBF_D<26>	6.1G 6.2D 13.3A 13.4B
FBF_D<27>	6.2D 6.2G 13.3A 13.4B
FBF_D<28>	6.2D 6.2G 13.3A 13.4B
FBF_D<29>	6.2D 6.2G 13.3A 13.4B
FBF_D<30>	6.2D 6.2G 13.3A 13.4B
FBF_D<31>	6.2G 6.3D 13.3A 13.4B
FBF_D<32>	6.1E 6.2G 13.3A 13.3C
FBF_D<33>	6.2E 6.2G 13.3A 13.3C
FBF_D<34>	6.2E 6.2G 13.3A 13.3C
FBF_D<35>	6.2E 6.2G 13.3A 13.3C
FBF_D<36>	6.2E 6.2G 13.3A 13.4C
FBF_D<37>	6.2E 6.2G 13.4A 13.4C
FBF_D<38>	6.2E 6.2G 13.4A 13.4C
FBF_D<39>	6.2E 6.2G 13.4A 13.4C
FBF_D<40>	6.2E 6.2G 13.3C 13.4A
FBF_D<41>	6.2E 6.2G 13.3C 13.4A
FBF_D<42>	6.2E 6.2G 13.3C 13.4A
FBF_D<43>	6.2E 6.2G 13.3C 13.4A
FBF_D<44>	6.2E 6.2G 13.4A 13.4C
FBF_D<45>	6.2E 6.2G 13.4A 13.4C
FBF_D<46>	6.2E 6.2G 13.4A 13.4C
FBF_D<47>	6.2E 6.2G 13.4A 13.4C
FBF_D<48>	6.2E 6.2G 13.4A 13.4C
FBF_D<49>	6.2E 6.2G 13.4A 13.4C
FBF_D<50>	6.2E 6.2G 13.4A 13.4C
FBF_D<51>	6.2E 6.2G 13.4A 13.4C
FBF_D<52>	6.2E 6.2G 13.4A 13.4C

FBF_D<53>	6.2E 6.2G 13.4A 13.4C
FBF_D<54>	6.2E 6.2G 13.4A 13.4C
FBF_D<55>	6.2E 6.2G 13.4A 13.4C
FBF_D<56>	6.2E 6.2G 13.4A 13.4C
FBF_D<57>	6.2E 6.3G 13.4A 13.4C
FBF_D<58>	6.2E 6.3G 13.4A 13.4C
FBF_D<59>	6.2E 6.3G 13.4A 13.4C
FBF_D<60>	6.2E 6.3G 13.4A 13.4C
FBF_D<61>	6.2E 6.3G 13.4A 13.4C
FBF_D<62>	6.2E 6.3G 13.4A 13.4C
FBF_D<63>	6.3E 6.3G 13.4A 13.4C
FBF_DEBUG	6.3E
FBF_DQM0	6.3D 6.3H<> 13.4A<>
	13.4A
FBF_DQM1	6.3D 6.3H<> 13.4B
	13.5A<>
FBF_DQM2	6.3D 6.3H<> 13.4A
	13.5A<>
FBF_DQM3	6.3D 6.3H<> 13.4B
	13.5A<>
FBF_DQM4	6.3E 6.3H<> 13.4C
	13.5A<>
FBF_DQM5	6.3E 6.3H<> 13.4C
	13.5A<>
FBF_DQM6	6.3E 6.3H<> 13.4C
	13.5A<>
FBF_DQM7	6.3E 6.3H<> 13.4C
	13.5A<>
FBF_DQS_RN0	6.3D 6.3H< 13.4A
	13.5A<
FBF_DQS_RN1	6.3D 6.3H< 13.4B
	13.5A<
FBF_DQS_RN2	6.3D 6.3H< 13.4A
	13.5A<
FBF_DQS_RN3	6.3D 6.3H< 13.4B
	13.5A<
FBF_DQS_RN4	6.3E 6.3H< 13.4C
	13.5A<
FBF_DQS_RN5	6.3E 6.3H< 13.4C
	13.5A<
FBF_DQS_RN6	6.3E 6.3H< 13.4C
	13.5A<
FBF_DQS_RN7	6.3E 6.3H< 13.4C
	13.5A<
FBF_DQS_WP0	6.3D 6.3H> 13.4A
	13.5A>
FBF_DQS_WP1	6.3D 6.3H> 13.4B
	13.5A>
FBF_DQS_WP2	6.3D 6.3H> 13.4A
	13.5A>
FBF_DQS_WP3	6.3D 6.4H> 13.4B
	13.5A>
FBF_DQS_WP4	6.3E 6.4H> 13.4C
	13.5A>
FBF_DQS_WP5	6.3E 6.4H> 13.4C
	13.5A>
FBF_DQS_WP6	6.3E 6.4H> 13.4C
	13.5A>
FBF_DQS_WP7	6.3E 6.4H> 13.4C
	13.5A>
FBF_SEN1	13.2A
FBF_SEN2	13.2C
FBF_VREF1	13.1H 13.3B
FBF_VREF2	13.2H 13.3B
FBF_VREF3	13.2H 13.3D
FBF_VREF4	13.3D 13.3H
FBF_ZQ1	13.2A
FBF_ZQ2	13.2C
FBG0_CLK0	7.4A 7.5G> 14.2A<
	14.2A 14.4G
FBG0_CLK0*	7.4A 7.5G> 14.2A<
	14.2A 14.4G
FBG0_CLK0_R	14.4H
FBG1_CLK0	7.4B 7.5G> 14.2A<
	14.2C 14.4G
FBG1_CLK0*	7.4B 7.5G> 14.2A<
	14.2C 14.4G
FBG1_CLK0_R	14.4H
FBGH_REFCLK	7.3C< 18.5D>
FBGH_REFCLK*	7.3C< 18.5D>
FBG_CMD<0>	7.3A 7.4F 14.1A 14.1A
	14.5A
FBG_CMD<0..28>	7.4G> 14.1A<
FBG_CMD<1>	7.3A 7.4F 14.1A 14.1A
	14.5A
FBG_CMD<2>	7.3A 7.4F 14.1A 14.1A
	14.5A
FBG_CMD<3>	7.3A 7.4F 14.1A 14.1A
	14.5A
FBG_CMD<4>	7.3A 7.4F 14.1A 14.1A
	14.5A
FBG_CMD<5>	7.3A 7.4F 14.1A 14.1A
	14.5A
FBG_CMD<6>	7.3A 7.4F 14.1A 14.2A
	14.2C 14.5F
FBG_CMD<7>	7.3A 7.4F 14.1A 14.1A

	14.1C
FBG_CMD<8>	7.3A 7.4F 14.1A 14.2A
	14.2C
FBG_CMD<9>	7.3A 7.4F 14.1A 14.1A
	14.1C
FBG_CMD<10>	7.3A 7.4F 14.1A 14.2A
	14.2C 14.5F
FBG_CMD<11>	7.4A 7.4F 14.1A 14.2A
	14.2C
FBG_CMD<12>	7.4A 7.4F 14.1A 14.1A
	14.1C
FBG_CMD<13>	7.4A 7.4F 14.1A 14.2A
	14.2C
FBG_CMD<14>	7.4A 7.4F 14.1A 14.1A
	14.1C
FBG_CMD<15>	7.4A 7.4F 14.1A 14.2A
	14.2C
FBG_CMD<16>	7.4A 7.4F 14.1A 14.1A
	14.1C
FBG_CMD<17>	7.4A 7.4F 14.1A 14.1A
	14.1C
FBG_CMD<18>	7.4A 7.4F 14.1A 14.1A
	14.1C
FBG_CMD<19>	7.4A 7.4F 14.1A 14.1A
	14.1C
FBG_CMD<20>	7.4A 7.4F 14.1A 14.1C
	14.2A
FBG_CMD<21>	7.4A 7.4F 14.1A 14.1C
	14.2A
FBG_CMD<23>	7.4A 7.4F 14.1C 14.2A
	14.5C
FBG_CMD<24>	7.4A 7.5F 14.1C 14.2A
	14.5C
FBG_CMD<25>	7.4A 7.5F 14.1C 14.2A
	14.5C
FBG_CMD<26>	7.4A 7.5F 14.1C 14.2A
	14.5C
FBG_CMD<27>	7.4A 7.5F 14.1C 14.2A
	14.5C
FBG_CMD<28>	7.4A 7.5F 14.1C 14.2A
	14.5C
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FBG_D<0..63>	7.1G> 14.2A<>
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FBG_D<2>	7.1F 7.2A 14.2A 14.3A
FBG_D<3>	7.1F 7.2A 14.2A 14.3A
FBG_D<4>	7.1F 7.2A 14.2A 14.4A
FBG_D<5>	7.1F 7.2A 14.2A 14.4A
FBG_D<6>	7.1F 7.2A 14.2A 14.4A
FBG_D<7>	7.1F 7.2A 14.3A 14.4A
FBG_D<8>	7.1F 7.2A 14.3A 14.3B
FBG_D<9>	7.1F 7.2A 14.3A 14.3B
FBG_D<10>	7.1F 7.2A 14.3A 14.3B
FBG_D<11>	7.1F 7.2A 14.3A 14.3B
FBG_D<12>	7.1F 7.2A 14.3A 14.4B
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FBG_D<14>	7.1F 7.2A 14.3A 14.4B
FBG_D<15>	7.1F 7.2A 14.3A 14.4B
FBG_D<16>	7.1F 7.2A 14.3A 14.4A
FBG_D<17>	7.1F 7.2A 14.3A 14.4A
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FBG_D<19>	7.1F 7.2A 14.3A 14.4A
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FBG_D<22>	7.1F 7.2A 14.3A 14.4A
FBG_D<23>	7.1F 7.2A 14.3A 14.4A
FBG_D<24>	7.1F 7.2A 14.3A 14.4B
FBG_D<25>	7.1F 7.2A 14.3A 14.4B
FBG_D<26>	7.1F 7.2A 14.3A 14.4B
FBG_D<27>	7.2A 7.2F 14.3A 14.4B
FBG_D<28>	7.2A 7.2F 14.3A 14.4B
FBG_D<29>	7.2A 7.2F 14.3A 14.4B
FBG_D<30>	7.2A 7.2F 14.3A 14.4B
FBG_D<31>	7.2F 7.3A 14.3A 14.4B
FBG_D<32>	7.1B 7.2F 14.3A 14.3C
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FBG_D<35>	7.2B 7.2F 14.3A 14.3C
FBG_D<36>	7.2B 7.2F 14.3A 14.4C
FBG_D<37>	7.2B 7.2F 14.4A 14.4C
FBG_D<38>	7.2B 7.2F 14.4A 14.4C
FBG_D<39>	7.2B 7.2F 14.4A 14.4C
FBG_D<40>	7.2B 7.2F 14.3C 14.4A
FBG_D<41>	7.2B 7.2F 14.3C 14.4A
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FBG_D<43>	7.2B 7.2F 14.3C 14.4A
FBG_D<44>	7.2B 7.2F 14.4A 14.4C
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FBG_D<46>	7.2B 7.2F 14.4A 14.4C
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FBG_D<48>	7.2B 7.2F 14.4A 14.4C
FBG_D<49>	7.2B 7.2F 14.4A 14.4C
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FBG_D<52>	7.2B 7.2F 14.4A 14.4C
FBG_D<53>	7.2B 7.2F 14.4A 14.4C

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
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FBG_D<54>	7.2B 7.2F 14.4A 14.4C
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FBG_D<56>	7.2B 7.2F 14.4A 14.4C
FBG_D<57>	7.2B 7.3F 14.4A 14.4C
FBG_D<58>	7.2B 7.3F 14.4A 14.4C
FBG_D<59>	7.2B 7.3F 14.4A 14.4C
FBG_D<60>	7.2B 7.3F 14.4A 14.4C
FBG_D<61>	7.2B 7.3F 14.4A 14.4C
FBG_D<62>	7.2B 7.3F 14.4A 14.4C
FBG_D<63>	7.3B 7.3F 14.4A 14.4C
FBG_DEBUG	7.3B
FBG_DQM0	7.3A 7.3G<> 14.4A<> 14.4A
FBG_DQM1	7.3A 7.3G<> 14.4B 14.5A<>
FBG_DQM2	7.3A 7.3G<> 14.4A 14.5A<>
FBG_DQM3	7.3A 7.3G<> 14.4B 14.5A<>
FBG_DQM4	7.3B 7.3G<> 14.4C 14.5A<>
FBG_DQM5	7.3B 7.3G<> 14.4C 14.5A<>
FBG_DQM6	7.3B 7.3G<> 14.4C 14.5A<>
FBG_DQM7	7.3B 7.3G<> 14.4C 14.5A<>
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FBG_DQS_RN1	7.3A 7.3G< 14.4B 14.5A<
FBG_DQS_RN2	7.3A 7.3G< 14.4A 14.5A<
FBG_DQS_RN3	7.3A 7.3G< 14.4B 14.5A<
FBG_DQS_RN4	7.3B 7.3G< 14.4C 14.5A<
FBG_DQS_RN5	7.3B 7.3G< 14.4C 14.5A<
FBG_DQS_RN6	7.3B 7.3G< 14.4C 14.5A<
FBG_DQS_RN7	7.3B 7.3G< 14.4C 14.5A<
FBG_DQS_WP0	7.3A 7.3G> 14.4A 14.5A>
FBG_DQS_WP1	7.3A 7.3G> 14.4B 14.5A>
FBG_DQS_WP2	7.3A 7.3G> 14.4A 14.5A>
FBG_DQS_WP3	7.3A 7.4G> 14.4B 14.5A>
FBG_DQS_WP4	7.3B 7.4G> 14.4C 14.5A>
FBG_DQS_WP5	7.3B 7.4G> 14.4C 14.5A>
FBG_DQS_WP6	7.3B 7.4G> 14.4C 14.5A>
FBG_DQS_WP7	7.3B 7.4G> 14.4C 14.5A>
FBG_SEN1	14.2A
FBG_SEN2	14.2C
FBG_VREF1	14.1H 14.3B
FBG_VREF2	14.2H 14.3B
FBG_VREF3	14.2H 14.3D
FBG_VREF4	14.3D 14.3H
FBG_ZQ1	14.2A
FBG_ZQ2	14.2C
FBVDDQ_SENSE	30.3G< 30.4B>
FB_CAL_PD_VDDQ	4.5B
FB_CAL_PU_GND	4.5B
FB_CAL_TERM_GND	4.5B
FL_REFCLK_VAIO	25.3B
GPIO0_DVIAB_HPD	22.4D> 25.2F<
GPIO0_DVIAB_HPD_CON	22.4F
GPIO0_DVIAB_HPD_R	22.4E
GPIO1_DVICD_HPD	23.4D> 25.2F<
GPIO1_DVICD_HPD_CON	23.3G 23.4F
GPIO1_DVICD_HPD_R	23.4E
GPIO4_PS5_NVVDD_VID	25.3F> 31.3B<
GPIO5_PS5_NVVDD_VID	25.3F> 31.2B<
GPIO6_PS5_NVVDD_VID	25.3F> 31.2B<
GPIO7_PS5_NVVDD_VID	25.3F> 31.3B<
GPIO8_FAN_TACH	25.3F< 26.3F>
GPIO9_THERM_ALERT*	25.3G< 26.4E> 26.4E>
GPIO10_PS5_NVVDD_VID	25.3F> 31.3B<
GPIO11_RASTERSYNC1_R	24.3F<> 25.3F<>
GPIO11_RASTERSYNC1_R	24.2G
GPIO14_RASTERSYNC2_R	24.3F<> 25.3F<>
GPIO14_RASTERSYNC2_R	24.3G
GPIO15_SWAPRDY	24.3F<> 25.3G<> 25.3G<>
GPU_BUFCLK_LDT_IN	18.4E
GPU_CLK	18.4C
GPU_CLK*	18.4C
GPU_HOT_RESET*	18.4E
GPU_PEX_PWR_GOOD*	18.4E
GPU_PMC_ISO_RESET*	18.4E
GPU_RST*	25.2B< 26.3F< 26.5E< 27.4H> 27.5F
GPU_RST_R*	26.3G
GPU_RST_RC*	26.5F
GPU_RST_R_MOS	26.2G
GPU_TESTMODE	28.4G
GV_PLLAVDD	18.1C
GV_RX0	18.3E
GV_RX0*	18.3E
GV_RX1	18.3E
GV_RX1*	18.3E
GV_RX2	18.3E
GV_RX2*	18.3E
GV_RX3	18.3E
GV_RX3*	18.3E
GV_RXCLK	18.4E
GV_RXCLK*	18.4E
GV_RXCTL	18.4E
GV_RXCTL*	18.4E
GV_RX_RSET_VDD	18.3C
GV_TX0	18.1E
GV_TX0*	18.1E
GV_TX1	18.1E
GV_TX1*	18.1E
GV_TX2	18.1E
GV_TX2*	18.1E
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GV_TX19	18.3E
GV_TX19*	18.3E
GV_TXCLK	18.3E
GV_TXCLK*	18.3E
GV_TXCTL	18.3E
GV_TXCTL*	18.3E
GV_TX_RSET_GND	18.3C
HYBRID_HPD_DVIAB	27.4G
HYBRID_HPD_DVICD_DP	27.4G
HYBRID_HPD_E	27.4G
HYBRID_HPD_F	27.4G
HYBRID_PRG_TP	27.5E
I2C1_SCL	19.3C
I2C1_SCL_CON	19.1H> 23.3G<
I2C1_SCL_R	19.1F
I2C1_SDA	19.3C
I2C1_SDA_CON	19.1H<> 23.3G<
I2C1_SDA_R	19.1F
I2C1_SDA_UC	27.4G
I2C2_SCL	20.3C
I2C2_SCL_CON	20.1H> 22.3G<
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I2C2_SDA	20.3C
I2C2_SDA_CON	20.1H<> 22.3G<
I2C2_SDA_R	20.1F
I2C2_SDA_UC	27.4G
I2C3_SCL	25.2D
I2C3_SCL_R	25.2F> 26.4C< 26.4C< 27.4E>
I2C3_SDA	25.2D
I2C3_SDA_R	25.2F<> 26.4C<> 26.4C<> 27.4E<>
I2C4_SCL	25.2D
I2C4_SDA	25.2D
I2C4_SDA_R	25.2G
I2CS_SCL	3.1E
I2CS_SCL_R	27.4E
I2CS_SDA	3.2E
I2CS_SDA_R	27.4E
IFPAB_IOVDD	22.3B
IFPAB_PLLVDD	22.3B
IFPAB_RSET	22.2B
IFPA_TXC	22.2E
IFPA_TXC*	22.2E
IFPA_TXD0	22.3E
IFPA_TXD0*	22.2E
IFPA_TXD1	22.3E
IFPA_TXD1*	22.3E
IFPA_TXD2	22.3E
IFPA_TXD2*	22.3E
IFPB_TXD4	22.3E
IFPB_TXD4*	22.3E
IFPB_TXD5	22.3E
IFPB_TXD5*	22.3E
IFPB_TXD6	22.3E
IFPB_TXD6*	22.3E
IFPCD_IOVDD	23.3B
IFPCD_PLLVDD	23.3B
IFPCD_RSET	23.2B
IFPC_TXC	23.2E
IFPC_TXC*	23.2E
IFPC_TXD0	23.3E
IFPC_TXD0*	23.2E
IFPC_TXD1	23.3E
IFPC_TXD1*	23.3E
IFPC_TXD2	23.3E
IFPC_TXD2*	23.3E
IFPD_TXD4	23.3E
IFPD_TXD4*	23.3E
IFPD_TXD5	23.3E
IFPD_TXD5*	23.3E
IFPD_TXD6	23.3E
IFPD_TXD6*	23.3E
IFP_IOVDD_EN	26.3H
INPUT_PEX6_IN1	34.3A
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JTAG_TCK	3.1E
JTAG_TDI	3.1E
JTAG_TDI_GPU	3.1E
JTAG_TDI_NVIO	3.1F
JTAG_TDO	3.1E
JTAG_TDO_GPU	3.1E
JTAG_TDO_NVIO	3.1F
JTAG_TNS	3.1E
JTAG_TRST*	3.1E
JTAG_TRST2	3.1G
JTAG_TRST_3V3	3.1G
JTAG_TRST_3V3*	3.1G
MIOA_CTL3	27.2C 27.3E
MIOA_VREF	27.2B
MIOB_CTL3	27.2E 27.3C
MIOB_VREF	27.3B
NVIO_CLK_RSET_GND	18.5C
NVIO_EXTDEV_RST*	25.3D
NVIO_EXT_REFCLKA	25.3D
NVIO_EXT_REFCLKA_R	24.2F<> 25.3F<>
NVIO_EXT_REFCLKB	25.3D
NVIO_EXT_REFCLKB_R	24.3F<> 25.3F<>
NVIO_GVDR_RX_RSET_GND	18.3F
NVIO_GVDR_TX_RSET_GND	18.3F
NVIO_GV_PLLAVDD	18.4F
NVIO_GV_PLLVDD	18.4F
NVIO_PLLVDD	18.4A
NVIO_SP_PLLVDD	18.5A
NVIO_TESTMODE	25.3B
NVVDD_SENSE	30.4B> 31.4H<
NVVDD_SENSE_GND	30.4B> 31.5H<
NVVDD_SENSE_R	31.4G
PEX_PLLVDD	3.4F
PEX_PLLVDD_OP	3.4H> 29.1C>
PEX_PLLVDD_OP_ADJ	29.2B
PEX_PRSNT1*	3.1A
PEX_REFCLK	3.2B
PEX_REFCLK*	3.2B
PEX_RST*	3.2D> 27.5E< 27.5F
PEX_RX0	3.2B
PEX_RX0*	3.2B
PEX_RX1	3.2B
PEX_RX1*	3.2B
PEX_RX2	3.3B
PEX_RX2*	3.3B
PEX_RX3	3.3B
PEX_RX3*	3.3B
PEX_RX4	3.3B
PEX_RX4*	3.3B
PEX_RX5	3.3B
PEX_RX5*	3.3B
PEX_RX6	3.3B
PEX_RX6*	3.3B
PEX_RX7	3.4B
PEX_RX7*	3.4B
PEX_RX8	3.4B
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PEX_RX9	3.4B
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PEX_RX13*	3.5B
PEX_RX14	3.5B
PEX_RX14*	3.5B
PEX_RX15	3.5B
PEX_RX15*	3.5B
PEX_TSTCLK_OUT	3.4F
PEX_TSTCLK_OUT*	3.4F
PEX_TX0	3.2E
PEX_TX0*	3.2E
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PEX_TX11	3.4E
PEX_TX11*	3.4E
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PEX_TX12*	3.4E
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PEX_TX13*	3.5E
PEX_TX14	3.5E
PEX_TX14*	3.5E
PEX_TX15	3.5E
PEX_TX15*	3.5E
PEX_TX_C0	3.2C
PEX_TX_C0*	3.2C
PEX_TX_C1	3.2C
PEX_TX_C1*	3.2C
PEX_TX_C2	3.2C
PEX_TX_C2*	3.2C
PEX_TX_C3	3.3C
PEX_TX_C3*	3.3C
PEX_TX_C4	3.3C
PEX_TX_C4*	3.3C
PEX_TX_C5	3.3C
PEX_TX_C5*	3.3C
PEX_TX_C6	3.3C
PEX_TX_C6*	3.3C
PEX_TX_C7	3.3C
PEX_TX_C7*	3.3C
PEX_TX_C8	3.4C
PEX_TX_C8*	3.4C
PEX_TX_C9	3.4C
PEX_TX_C9*	3.4C
PEX_TX_C10	3.4C
PEX_TX_C10*	3.4C
PEX_TX_C11	3.4C
PEX_TX_C11*	3.4C
PEX_TX_C12	3.4C
PEX_TX_C12*	3.4C
PEX_TX_C13	3.5C
PEX_TX_C13*	3.5C
PEX_TX_C14	3.5C
PEX_TX_C14*	3.5C
PEX_TX_C15	3.5C
PEX_TX_C15*	3.5C
PS1_1V15_BOOT	29.3D
PS1_1V15_CP	29.4D
PS1_1V15_CP_RC	29.4E
PS1_1V15_EN*	29.4C
PS1_1V15_FB	29.4D
PS1_1V15_FB_RC	29.5F
PS1_1V15_FB_SEN	29.4G
PS1_1V15_FS	29.4C
PS1_1V15_LG	29.4D
PS1_1V15_PH	29.4D
PS1_1V15_PH_RC	29.4F
PS1_1V15_UG	29.3D
PS1_1V15_UG_R	29.3E
PS1_2V5_LDO_DR	29.3C
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PS1_2V5_LDO_FB	29.4C
PS1_PVCC5	29.3D
PS1_VCC5	29.3D
PS1_VCC12	29.3C
PS3_FBVDDQ_BOOT	30.2C
PS3_FBVDDQ_CP	30.2C
PS3_FBVDDQ_CP_RC	30.3D
PS3_FBVDDQ_FB	30.2C
PS3_FBVDDQ_FB_RC	30.3E
PS3_FBVDDQ_LG	30.2C
PS3_FBVDDQ_LG_D	30.2D
PS3_FBVDDQ_LG_G	30.2D
PS3_FBVDDQ_PHASE	30.2C
PS3_FBVDDQ_RC	30.2F
PS3_FBVDDQ_UG	30.2C
PS3_FBVDDQ_UG_R	30.2D
PS3_FBVDDQ_VSEN	30.3F
PS3_FS_DIS	30.2B
PS3_LDO_RC	30.2C
PS3_NVVDD_PGOOD*	30.2B
PS3_PVCC5_DRV	30.2C
PS3_VCC5	30.2C
PS5_NVVDD_BOOT1	32.2C
PS5_NVVDD_BOOT1_RC	32.2C 32.2C
PS5_NVVDD_BOOT2	32.3C
PS5_NVVDD_BOOT2_RC	32.3C
PS5_NVVDD_BOOT3	32.4C
PS5_NVVDD_BOOT3_RC	32.4C
PS5_NVVDD_BOOT4	33.2C
PS5_NVVDD_BOOT4_RC	32.4C> 33.2C<
PS5_NVVDD_BOOT5	33.3C
PS5_NVVDD_BOOT5_RC	33.3C 33.4C
PS5_NVVDD_BOOT6	33.4C
PS5_NVVDD_BOOT6_RC	33.4C
PS5_NVVDD_CP	31.4E
PS5_NVVDD_CP_RC	31.4F
PS5_NVVDD_DRV_OD1	31.3F> 32.2B< 32.4A< 33.2A<
PS5_NVVDD_DRV_ODN	31.3F> 32.3B< 32.4A< 33.2A< 33.3B< 33.4B<
PS5_NVVDD_DRV_PHASE3	32.4B
PS5_NVVDD_DRV_PHASE4	33.2B
PS5_NVVDD_EN	31.1H> 31.3D<
PS5_NVVDD_EN*	31.1G
PS5_NVVDD_EN_12V_FB2	31.2F
PS5_NVVDD_EN_12V_FB2	31.2F
PS5_NVVDD_EN_Q	31.2G
PS5_NVVDD_FB	31.4E
PS5_NVVDD_FBRTN	31.4E
PS5_NVVDD_FB_RC	31.4G
PS5_NVVDD_FS	31.3D
PS5_NVVDD_IDES	31.4D
PS5_NVVDD_ISEN1	31.3E
PS5_NVVDD_ISEN2	31.3E
PS5_NVVDD_ISEN3	31.3E
PS5_NVVDD_ISEN4	31.3E
PS5_NVVDD_ISEN5	31.3E
PS5_NVVDD_ISEN6	31.3E
PS5_NVVDD_LG1	32.2C
PS5_NVVDD_LG1_AC	32.2C
PS5_NVVDD_LG1_D	32.2C
PS5_NVVDD_LG2	32.3C
PS5_NVVDD_LG2_AC	32.3C
PS5_NVVDD_LG2_D	32.3C
PS5_NVVDD_LG3	32.5C
PS5_NVVDD_LG3_AC	32.5C
PS5_NVVDD_LG3_D	32.4C
PS5_NVVDD_LG4	33.2C
PS5_NVVDD_LG4_AC	33.2D
PS5_NVVDD_LG4_D	33.2D
PS5_NVVDD_LG5	33.3C
PS5_NVVDD_LG5_AC	33.3D
PS5_NVVDD_LG5_D	33.3D
PS5_NVVDD_LG6	33.5C
PS5_NVVDD_LG6_AC	33.5D
PS5_NVVDD_LG6_D	33.4D
PS5_NVVDD_PGOOD	31.3D
PS5_NVVDD_PGOOD_R	30.3A< 31.5E>
PS5_NVVDD_PHASE1	31.3H< 32.2F> 32.2F>
PS5_NVVDD_PHASE2	31.3H< 32.3F> 32.3F>
PS5_NVVDD_PHASE3	31.3H< 32.5F> 32.5F>
PS5_NVVDD_PHASE4	31.3H< 33.2G> 33.2G>
PS5_NVVDD_PHASE5	31.3H< 33.3G> 33.3G>
PS5_NVVDD_PHASE6	31.3H< 33.5G> 33.5G>
PS5_NVVDD_PWM1	31.3F> 32.2B<
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PS5_NVVDD_PWM3	31.2F> 32.4B<
PS5_NVVDD_PWM4	31.2F> 33.2B<
PS5_NVVDD_PWM5	31.2F> 33.3B<
PS5_NVVDD_PWM6	31.2F> 33.4B<
PS5_NVVDD_RC1	32.2E
PS5_NVVDD_RC2	32.3E
PS5_NVVDD_RC3	32.5E
PS5_NVVDD_RC4	33.2E
PS5_NVVDD_RC5	33.3E
PS5_NVVDD_RC6	33.5E
PS5_NVVDD_SET_ILIM_FS	31.3E
PS5_NVVDD_SET_IMON	31.4E
PS5_NVVDD_SET_LSSET	31.4E
PS5_NVVDD_SET_RAMP_ADJ	31.3D
PS5_NVVDD_SET_RAMP_ADJ_R	31.3C
PS5_NVVDD_SET_TRDET	31.3D> 31.4H<
PS5_NVVDD_SET_TRDET_RC	31.4G
PS5_NVVDD_STATUS_P	31.2B> 31.3D<
PS5_NVVDD_STATUS_P_SET	31.3D
PS5_NVVDD_UG1	32.2C
PS5_NVVDD_UG1_R	32.2C
PS5_NVVDD_UG2	32.3C
PS5_NVVDD_UG2_R	32.3D
PS5_NVVDD_UG3	32.4C
PS5_NVVDD_UG3_R	32.4D
PS5_NVVDD_UG4	33.2C
PS5_NVVDD_UG4_R	33.2D
PS5_NVVDD_UG5	33.3C
PS5_NVVDD_UG5_R	33.3D
PS5_NVVDD_UG6	33.4C
PS5_NVVDD_UG6_R	33.4D
PS5_NVVDD_VAMP_CSOMP	31.3E
PS5_NVVDD_VAMP_CSREF	31.4F< 31.4F< 32.2F> 32.3F> 32.5F> 33.2G> 33.3G> 33.5G>
PS5_NVVDD_VAMP_CSUM	31.3E
PS5_NVVDD_VAMP_CSUM_RC	31.4G
PS5_NVVDD_VCC	31.2D
PS5_NVVDD_VCC_VCC3	31.4D
PS5_NVVDD_VID0	31.2D
PS5_NVVDD_VID1	31.2C 31.2D
PS5_NVVDD_VID2	31.2D
PS5_NVVDD_VID3	31.2D
PS5_NVVDD_VID4	31.2C 31.3D
PS5_NVVDD_VID6	31.3D
PS5_NVVDD_VIN_PWM_ROM_CS*	31.2D 25.2B
SNN_7473_2	26.4D
SNN_DACB_CSYNC	21.3C
SNN_DACB_HSYNC	21.3C
SNN_DACB_VSYNC	21.3C
SNN_DVIA_CLK	27.4C
SNN_DVIA_CTL0	27.4C
SNN_DVIA_CTL1	27.4C
SNN_DVIA_CTL2	27.4C
SNN_DVIA_D4	27.4C
SNN_DVIA_D5	27.4C
SNN_DVIA_D6	27.4C
SNN_DVIB_CLK	27.5C
SNN_DVIB_CTL0	27.5C
SNN_DVIB_CTL1	27.5C
SNN_DVIB_CTL2	27.5C
SNN_DVIB_D0	27.5C
SNN_DVIB_D1	27.5C
SNN_DVIB_D2	27.5C
SNN_DVIB_D3	27.5C
SNN_DVIB_D6	27.5C
SNN_DVIB_D7	27.5C
SNN_FBAO_CLK1	4.4A
SNN_FBAO_CLK1*	4.4A
SNN_FBA1_CLK1	4.4B
SNN_FBA1_CLK1*	4.4B
SNN_FBA_CMD<22>	4.3A
SNN_FBA_CMD<29>	4.4A
SNN_FBA_CMD<30>	4.4A
SNN_FBA_CMD<31>	4.4A
SNN_FBA_CMD<32>	4.4A
SNN_FBA_DBI0	28.1E
SNN_FBA_DBI1	28.1E
SNN_FBA_DBI2	28.1E
SNN_FBA_DBI3	28.1E
SNN_FBA_DBI4	28.1E
SNN_FBA_DBI5	28.1E
SNN_FBA_DBI6	28.1E
SNN_FBA_DBI7	28.1E
SNN_FBA_NC01	8.2A
SNN_FBA_NC04	8.2C
SNN_FBB0_CLK1	4.4C
SNN_FBB0_CLK1*	4.4C
SNN_FBB1_CLK1	4.4E
SNN_FBB1_CLK1*	4.4E
SNN_FBB_CMD<22>	4.3D
SNN_FBB_CMD<29>	4.4D
SNN_FBB_CMD<30>	4.4D
SNN_FBB_CMD<31>	4.4D
SNN_FBB_CMD<32>	4.4D
SNN_FBB_DBI0	28.2E
SNN_FBB_DBI1	28.2E
SNN_FBB_DBI2	28.2E
SNN_FBB_DBI3	28.2E
SNN_FBB_DBI4	28.2E
SNN_FBB_DBI5	28.2E
SNN_FBB_DBI6	28.2E
SNN_FBB_DBI7	28.2E
SNN_FBB_NC01	9.2A
SNN_FBB_NC04	9.2C
SNN_FBC0_CLK1	5.4A
SNN_FBC0_CLK1*	5.4A
SNN_FBC1_CLK1	5.4B
SNN_FBC1_CLK1*	5.4B
SNN_FBC_CMD<22>	5.4A
SNN_FBC_CMD<29>	5.4A
SNN_FBC_CMD<30>	5.4A
SNN_FBC_CMD<31>	5.4A
SNN_FBC_CMD<32>	5.4A
SNN_FBC_DBI0	28.2E
SNN_FBC_DBI1	28.2E
SNN_FBC_DBI2	28.2E
SNN_FBC_DBI3	28.2E
SNN_FBC_DBI4	28.2E
SNN_FBC_DBI5	28.2E
SNN_FBC_DBI6	28.2E
SNN_FBC_DBI7	28.2E
SNN_FBC_NC01	10.2A
SNN_FBC_NC04	10.2C
SNN_FBD0_CLK1	5.4C
SNN_FBD0_CLK1*	5.4C
SNN_FBD1_CLK1	5.4E
SNN_FBD1_CLK1*	5.4E
SNN_FBD_CMD<22>	5.4D
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SNN_FBD_DBI0	28.2E
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SNN_FBD_DBI2	28.2E
SNN_FBD_DBI3	28.2E
SNN_FBD_DBI4	28.2E
SNN_FBD_DBI5	28.2E
SNN_FBD_DBI6	28.2E
SNN_FBD_DBI7	28.2E
SNN_FBD_NC01	11.2A
SNN_FBD_NC04	11.2C
SNN_FBE0_CLK1	6.4A
SNN_FBE0_CLK1*	6.4A
SNN_FBE1_CLK1	6.4B
SNN_FBE1_CLK1*	6.4B
SNN_FBE_CMD<22>	6.4A
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SNN_FBE_DBI0	28.2E
SNN_FBE_DBI1	28.2E
SNN_FBE_DBI2	28.3E
SNN_FBE_DBI3	28.3E
SNN_FBE_DBI4	28.3E
SNN_FBE_DBI5	28.3E
SNN_FBE_DBI6	28.3E
SNN_FBE_DBI7	28.3E
SNN_FBE_NC01	12.2A
SNN_FBE_NC04	12.2C
SNN_FBF0_CLK1	6.4C
SNN_FBF0_CLK1*	6.4C
SNN_FBF1_CLK1	6.4E
SNN_FBF1_CLK1*	6.4E
SNN_FBF_CMD<22>	6.4D
SNN_FBF_CMD<29>	6.4D
SNN_FBF_CMD<30>	6.4D
SNN_FBF_CMD<31>	6.4D
SNN_FBF_CMD<32>	6.4D
SNN_FBF_DBI0	28.3E
SNN_FBF_DBI1	28.3E
SNN_FBF_DBI2	28.3E
SNN_FBF_DBI3	28.3E
SNN_FBF_DBI4	28.3E

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SNN_FBF_DBI5	28.3E
SNN_FBF_DBI6	28.3E
SNN_FBF_DBI7	28.3E
SNN_FBF_NC01	13.2A
SNN_FBF_NC04	13.2C
SNN_FBGO_CLK1	7.4A
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SNN_FBG_DBI4	28.3E
SNN_FBG_DBI5	28.3E
SNN_FBG_DBI6	28.3E
SNN_FBG_DBI7	28.3E
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SNN_FBG_NC04	14.2C
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SNN_FBH0_CLK0*	7.4C
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SNN_FBH0_CLK1*	7.4C
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SNN_FBH1_CLK0*	7.4E
SNN_FBH1_CLK1	7.4E
SNN_FBH1_CLK1*	7.4E
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SNN_FBH_DBI5	28.4E
SNN_FBH_DBI6	28.4E
SNN_FBH_DBI7	28.4E
SNN_FBH_DEBUG	7.3E
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SNN_FBH_DQS_RN1	7.3D
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SNN_FBH_DQS_RN7	7.3E
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SNN_FBH_DQS_WP7	7.3E
SNN_FBVDDQ_GND_MSUR	30.4B
SNN_FBVDDQ_MSUR	30.5B
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SNN_FB_VREF1	4.5B
SNN_GPIO2_SWAPRDY_OUT	25.2D
SNN_GPIO3_RASTERSYNC0	25.3D
SNN_GPIO12_POWERALERT*	25.3D
SNN_GPIO13_STEREO	25.3D
SNN_GPIO16_DP_INT*	25.3D
SNN_GPU_BUFRST*	3.5F
SNN_GPU_NC_1	28.1G
SNN_GPU_NC_2	28.1G
SNN_GPU_NC_3	28.1G
SNN_GPU_NC_4	28.1G
SNN_GPU_NC_5	28.1G
SNN_GPU_NC_6	28.1G
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SNN_GPU_NC_8	28.1G
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SNN_GPU_NC_32	28.2G
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SNN_GPU_NC_40	28.3G
SNN_HDCP_NC	25.2G
SNN_I2C0_SCL	25.2D
SNN_I2C0_SDA	25.2D
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SNN_IFPA_TXD3	22.3D
SNN_IFPA_TXD3*	22.3D
SNN_IFPB_TXC	22.3D
SNN_IFPB_TXC*	22.3D
SNN_IFPB_TXD7	22.4D
SNN_IFPB_TXD7*	22.4D
SNN_IFPCD_VPROBE	23.2B
SNN_IFPC_TXD3	23.3D
SNN_IFPC_TXD3*	23.3D
SNN_IFPD_TXC	23.3D
SNN_IFPD_TXC*	23.3D
SNN_IFPD_TXD7	23.4D
SNN_IFPD_TXD7*	23.4D
SNN_INPUT_PEX6_DT1*	34.3A
SNN_INPUT_PEX6_DT2*	34.4A
SNN_MIOA<0>	27.1C
SNN_MIOA<1>	27.1C
SNN_MIOA<2>	27.1C
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SNN_MIOA<4>	27.1C
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SNN_MIOA_CAL_PD_VDD	27.2B
SNN_MIOA_CAL_PU_GND	27.2B
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SNN_MIOA_CLKOUT*	27.2C
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SNN_MIOB<14>	27.3C
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SNN_MIOB_CAL_PU_GND	27.3B
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SNN_MIOB_CLKOUT*	27.4C
SNN_MIOB_DE	27.3C
SNN_MIOB_HSYNC	27.3C
SNN_MIOB_VSYNC	27.3C
SNN_NVIO_NC_01	28.4G
SNN_NVIO_NC_02	28.4G
SNN_NVIO_NC_03	28.4G

SNN_NVIO_NC_04	28.4G
SNN_NVIO_NC_05	28.4G
SNN_NVIO_NC_06	28.4G
SNN_NVIO_NC_07	28.4G
SNN_NVIO_NC_08	28.4G
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SNN_NVIO_PLL_SP_NOUT	18.5C
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SNN_PEX_TDO	3.1B
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SNN_PEX_TRST*	3.1B
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SNN_PS5_NVVDD_PIN3	31.4D
SNN_PS5_NVVDD_PIN4	31.4D
SNN_PS5_NVVDD_TTSENSE	31.4D
SNN_PS5_NVVDD_VID5	31.3D
SNN_PS5_NVVDD_VID7	31.3D
SNN_PS5_NVVDD_VRHOT	31.3D
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SNN_SPARE_74	28.4F
SNN_STRAP3	25.2B
SNN_TACH2	26.4D
SNN_THERM_LD_STEP0	30.5B
SNN_THERM_LD_STEP1	30.5B
SNN_TSENSE_AVDD	26.4A
SNN_TSENSE_OVERT	26.4A
SNN_TSENSE_VREF	26.4A
SNN_TS_1V5_SEL	26.4A
SNN_TS_OBS	26.4A
SNN_TV_NC5	21.3G
SNN_TV_NC7	21.3G
SNN_U4I2C1_SCL_UC_PIN15	27.3G
SNN_U4_FAN_PWM_PIN5	27.5G
SNN_U4_HYBRID_PWR_EN_PIN16	27.5G
SNN_U4_I2C2_SCL_UC_PIN8	27.4G
SNN_U4_PEX_REFCLK_EN_PIN2	27.4E
SPDIF_GND	24.3C
SPDIF_IN	24.3C
SPDIF_IN_C	24.5A
SPDIF_IN_COMP2_D	24.5C
SPDIF_IN_COMP2_Q	24.4C
SPDIF_IN_GPU	24.3E> 25.2F<
SPDIF_IN_R	24.5B

STRAP0	25.2B
STRAP1	25.2B
STRAP2	25.2B
THERM_DN	26.3C 26.4B 26.4C
THERM_DP	26.3C 26.4B 26.4C
THERM_LATCH	26.1F
THERM_PWM_ADDR_EN*	26.4D
THERM_SHDN	26.2F
THERM_SHDN*	26.1G 26.2E 26.3D 26.4D
THERM_SHDN_D*	26.1H> 29.5B< 31.1G<
THERM_SHDN_Q	26.2G
THERM_SHDN_R	26.2E
THERM_VDD	26.3D
VID_PSI	31.2C
XTAL_IN	25.4C
XTAL_OUT	25.4C

ASSEMBLY	DT, GT200-103-B2, 573/1242/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
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