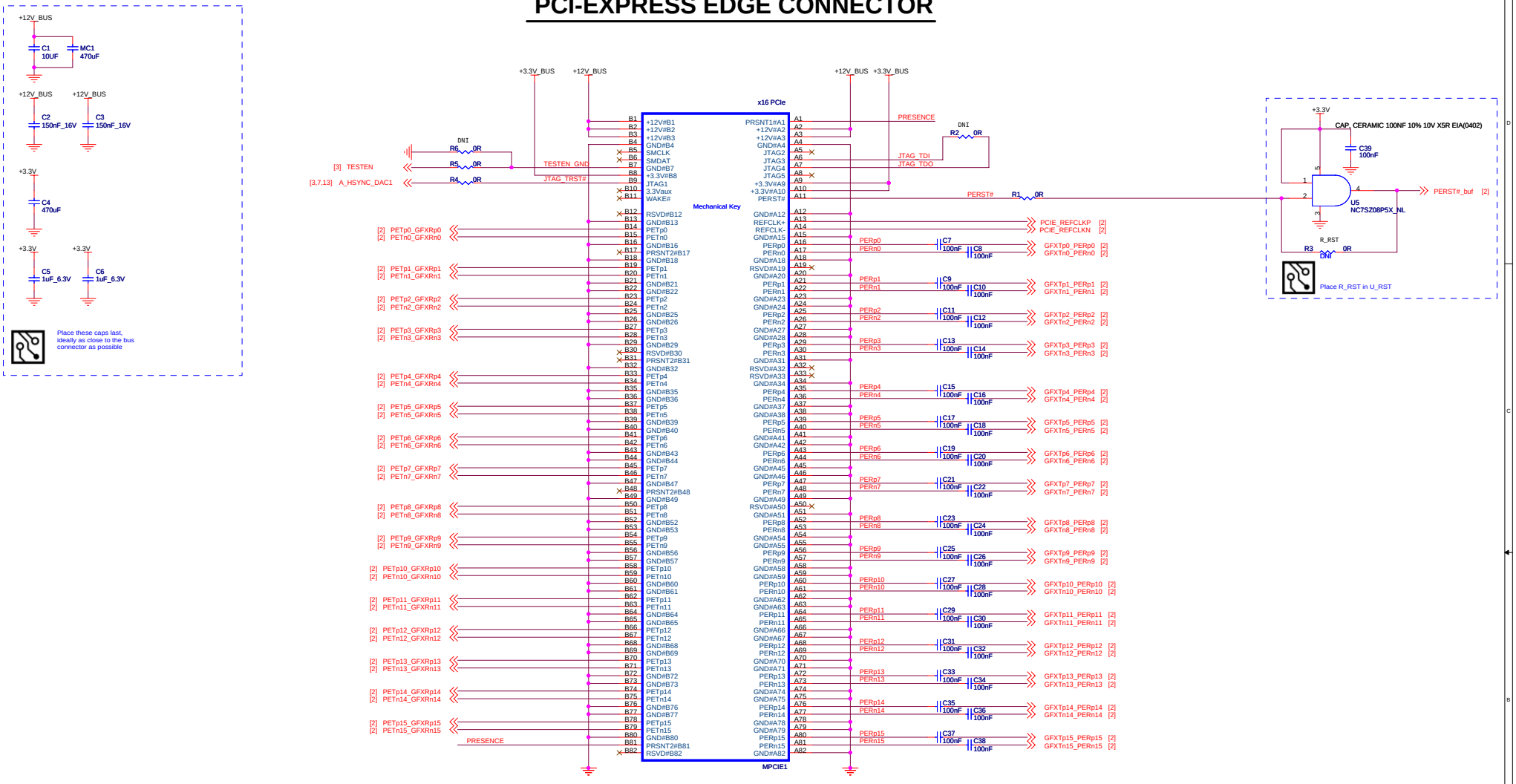
PCI-EXPRESS EDGE CONNECTOR



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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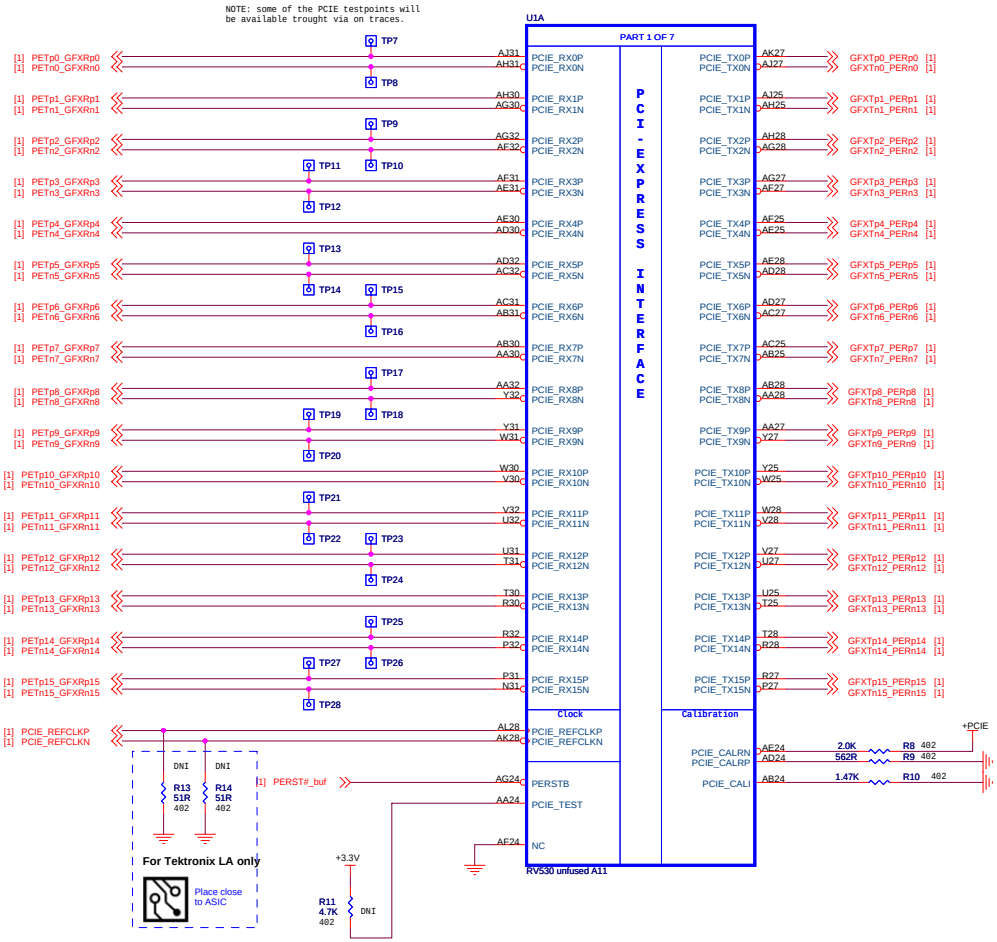
Size C	Document Number 105-A67700-00A	Rev 1
Date: Tuesday, December 20, 2005	Sheet 1 of 19	



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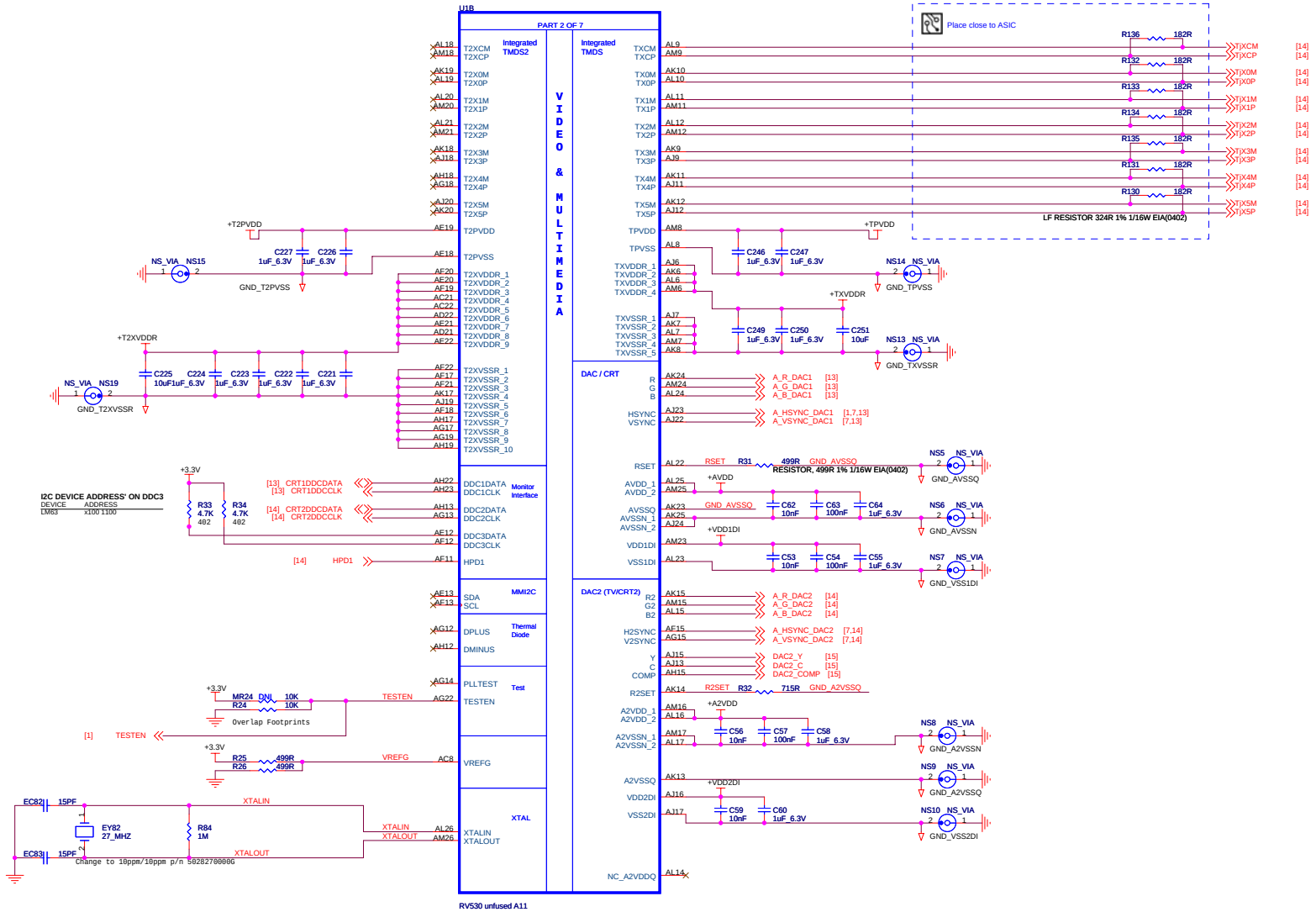
Size: C	Document Number: 105-A67700-00A	Rev: 1
Date: Friday, December 16, 2005	Sheet 2 of 19	



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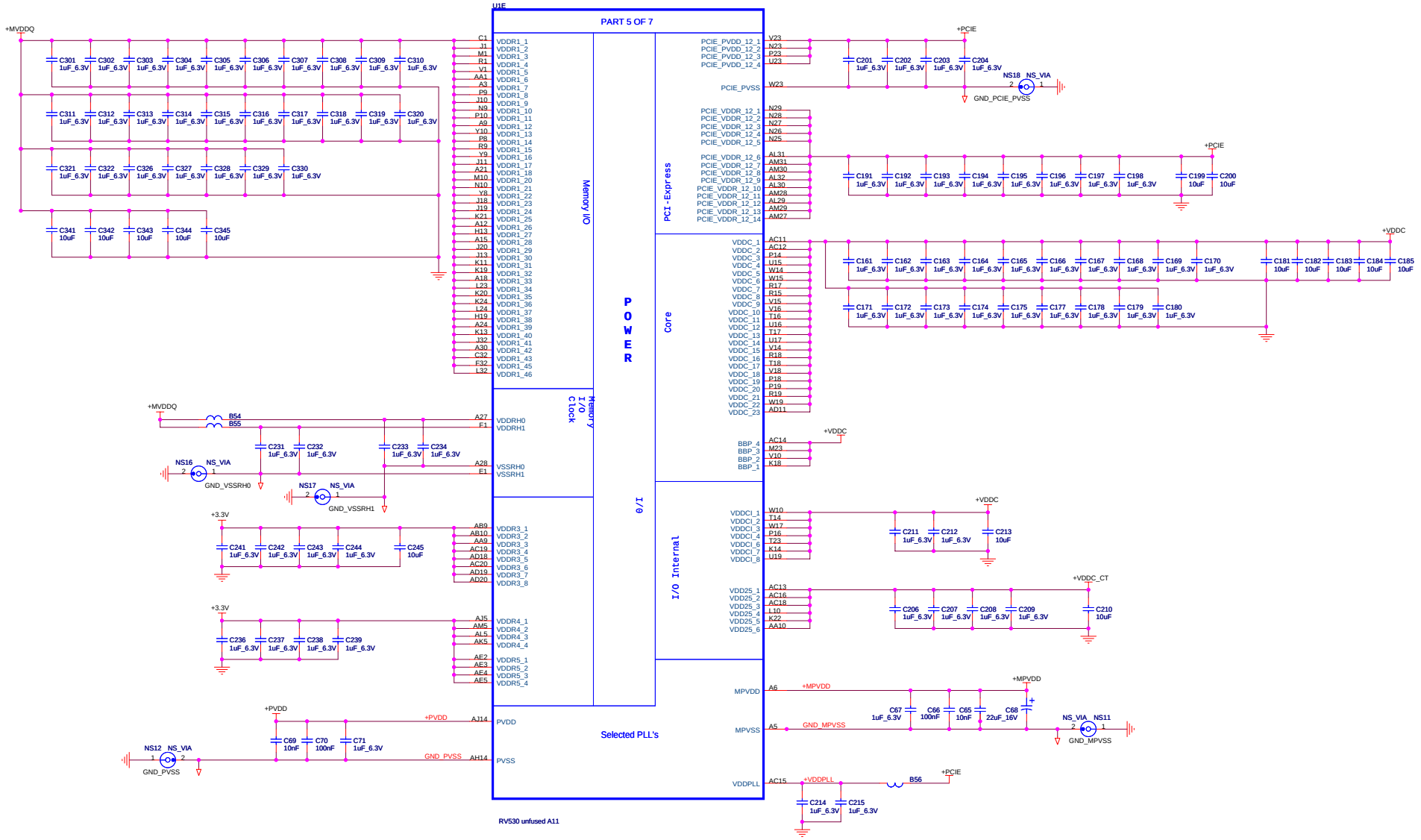
Title	MS-V050 RV515 TSOP
Size	Custom
Document Number	105-A67700-00A
Rev	1
Date:	Monday, December 19, 2005
Sheet	3 of 19



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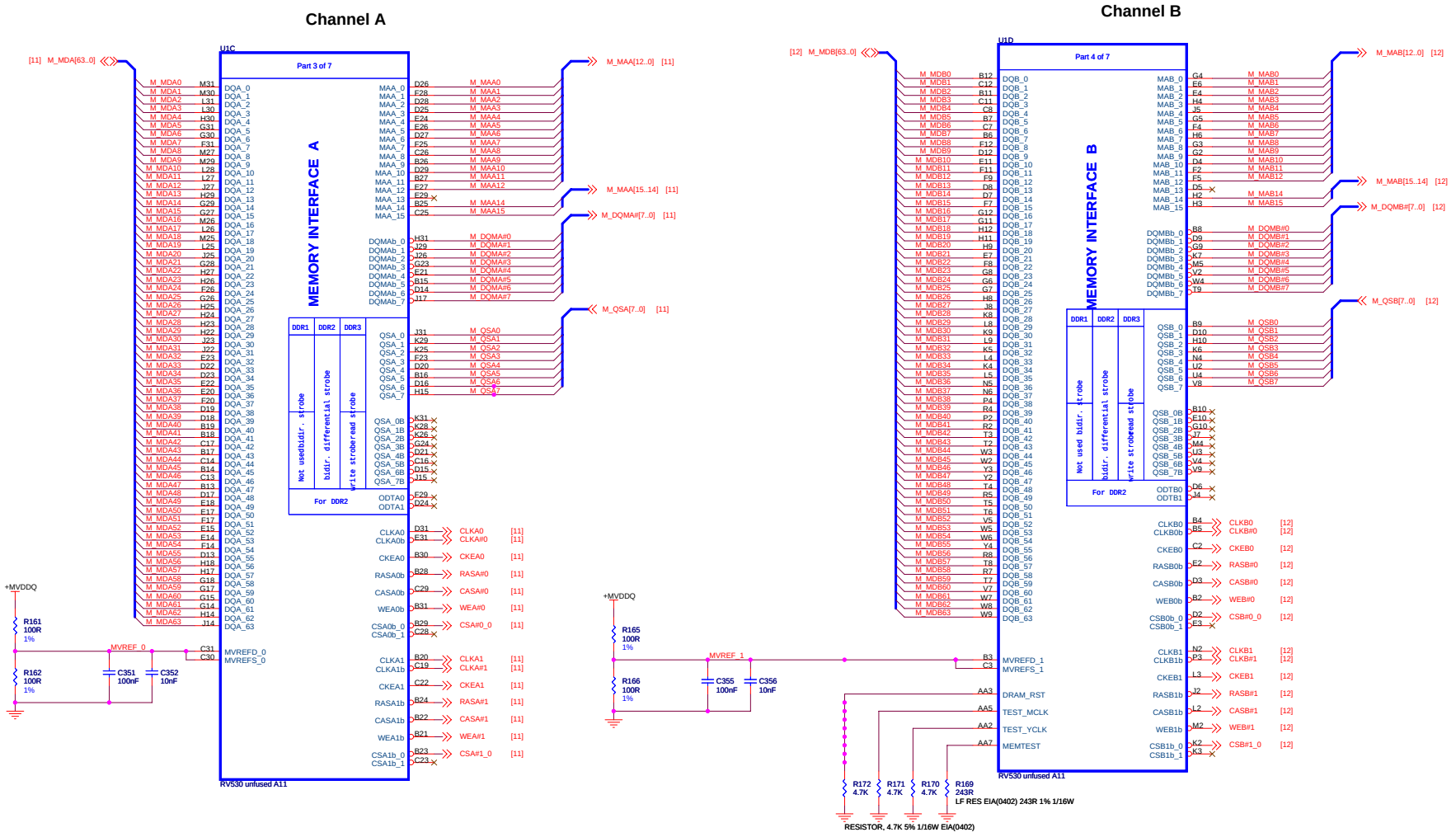
Size C	Document Number 105-A67700-00A	Rev 1
Date: Thursday, October 13, 2005	Sheet 4 of 19	

RV530 MEMORY CHANNELS A and B



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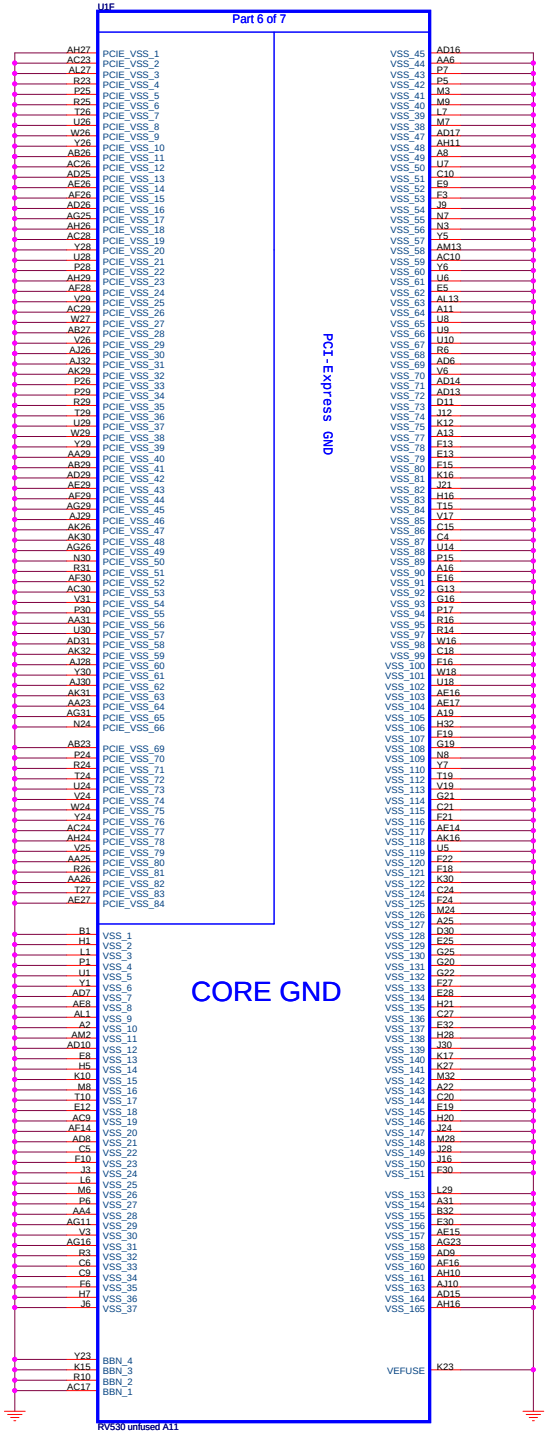
Size C	Document Number 105-A67700-00A		Rev 1
Date: Friday, December 16, 2005	Sheet 5 of 19		



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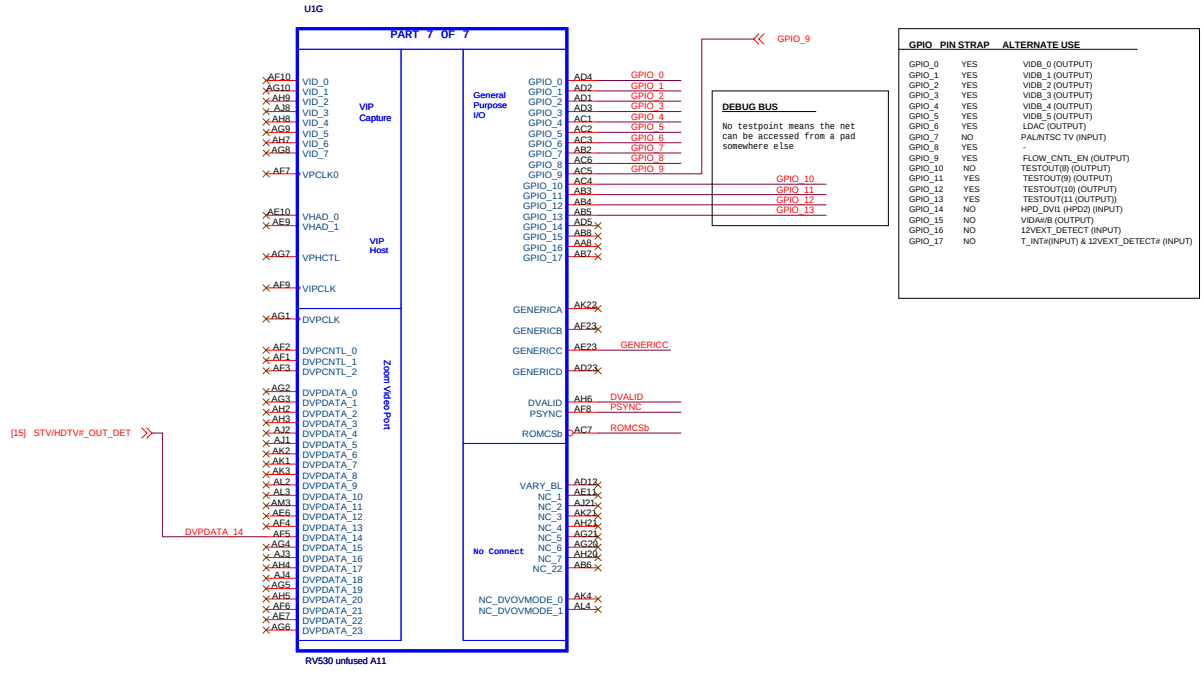
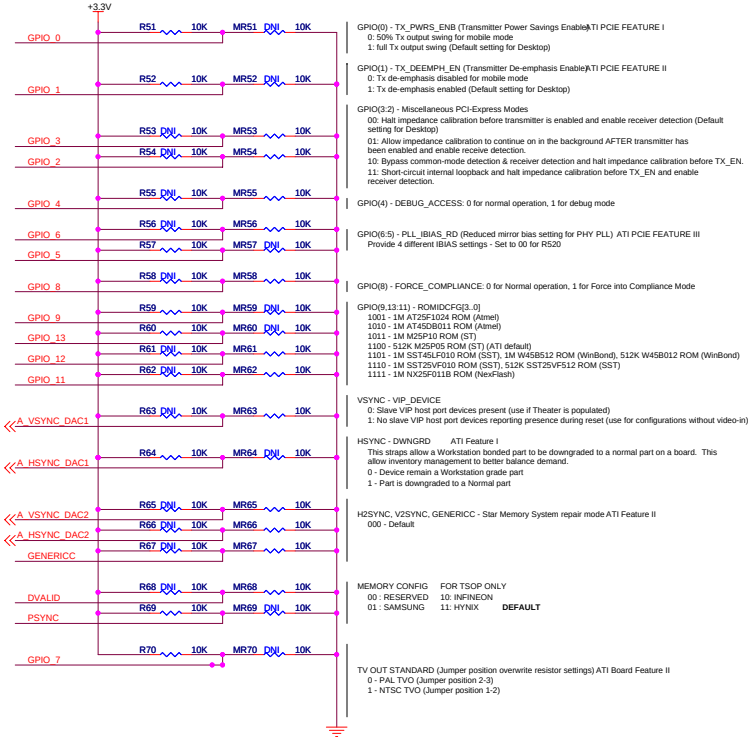
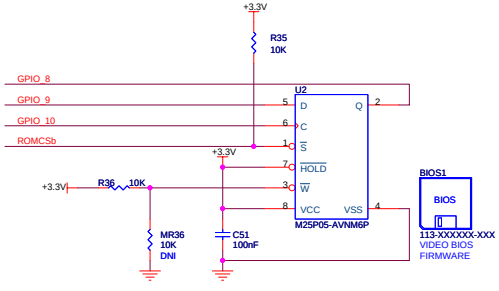
Size: C	Document Number: 105-A67700-00A	Rev: 1
Date: Thursday, October 13, 2005	Sheet 6 of 19	



GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDAWB (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

PIN BASED STRAPS





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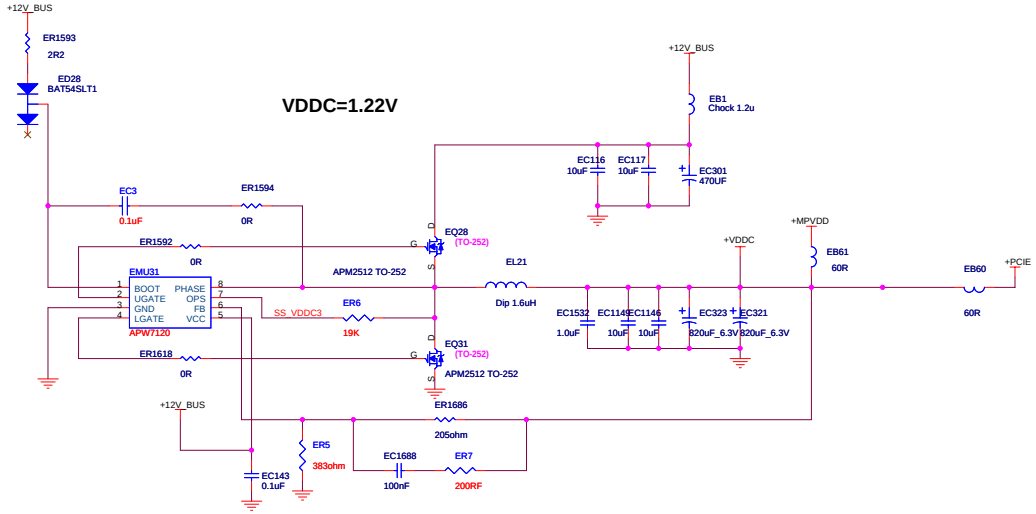
Title	MS-V050 RV515 TSOP		
Size C	Document Number 105-A67700-00A		Rev 1
Date: Friday, December 16, 2005		Sheet 7 of 19	

CORE REGULATOR +VDDC



VDDC=0.8 * [1 + (ER1686 / ER5)]

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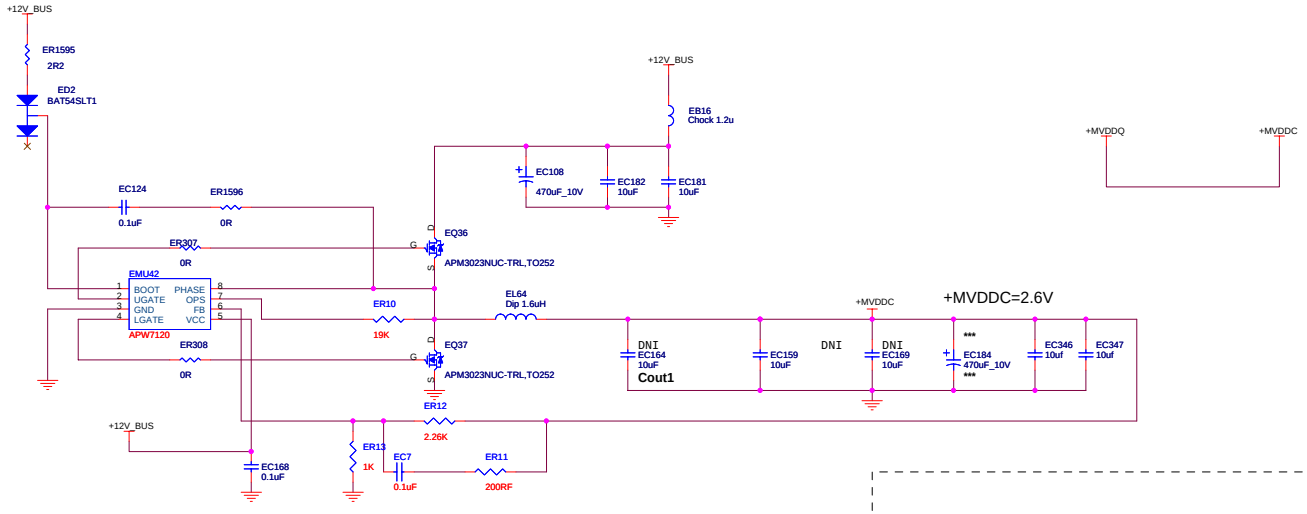
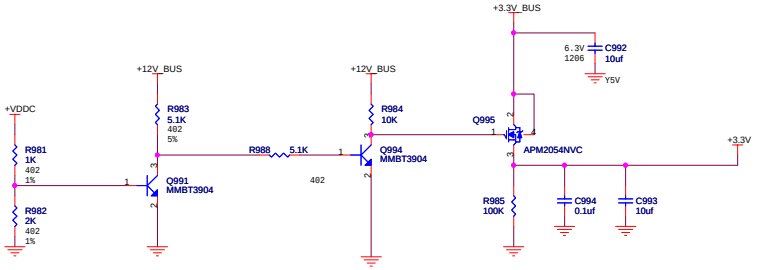
Title	MS-V050 RV515 TSOP	
Size: Custom	Document Number: 105-A67700-00A	Rev: 1
Date: Tuesday, December 20, 2005	Sheet 8 of 19	



MVDDC=0.8 * [1 + (ER12 / ER13)]

	ER12	ER13
2.6V	R11-2261T13-W08	R11-0102T23-R01



Power Sequencing

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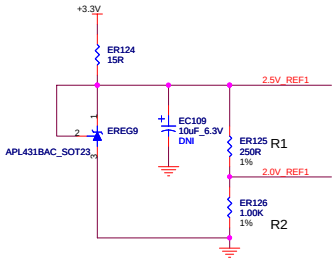
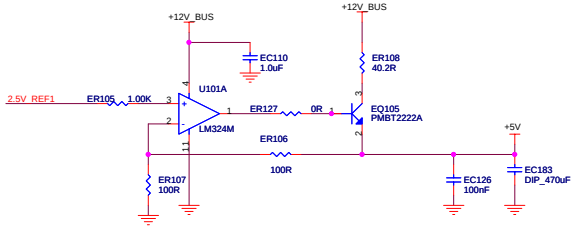
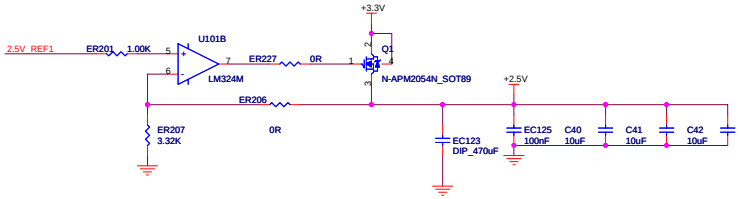
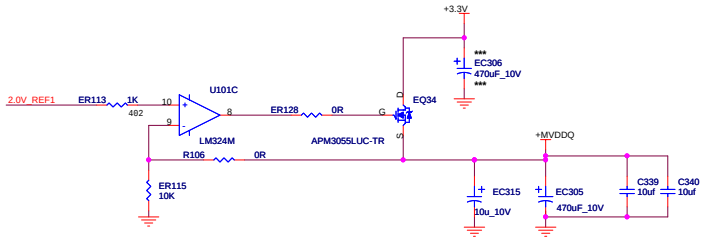
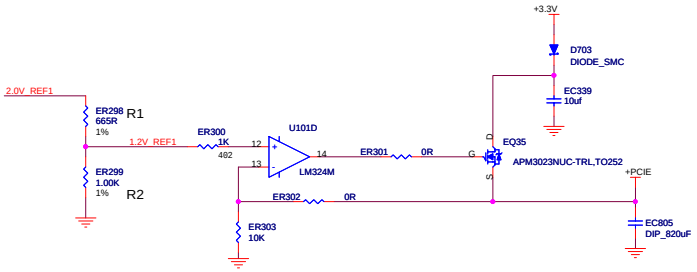
Size: Custom	Document Number: 105-A67700-00A	Rev: 1
Date: Tuesday, December 27, 2005	Sheet 9 of 19	

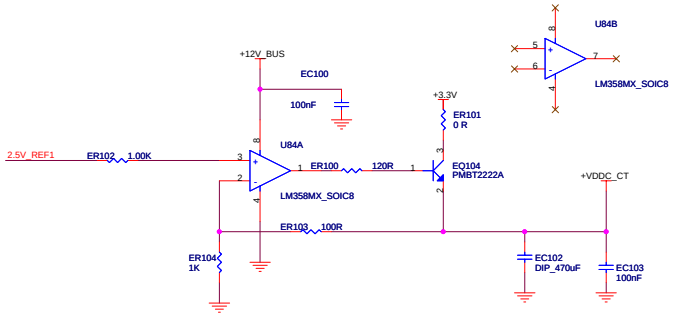












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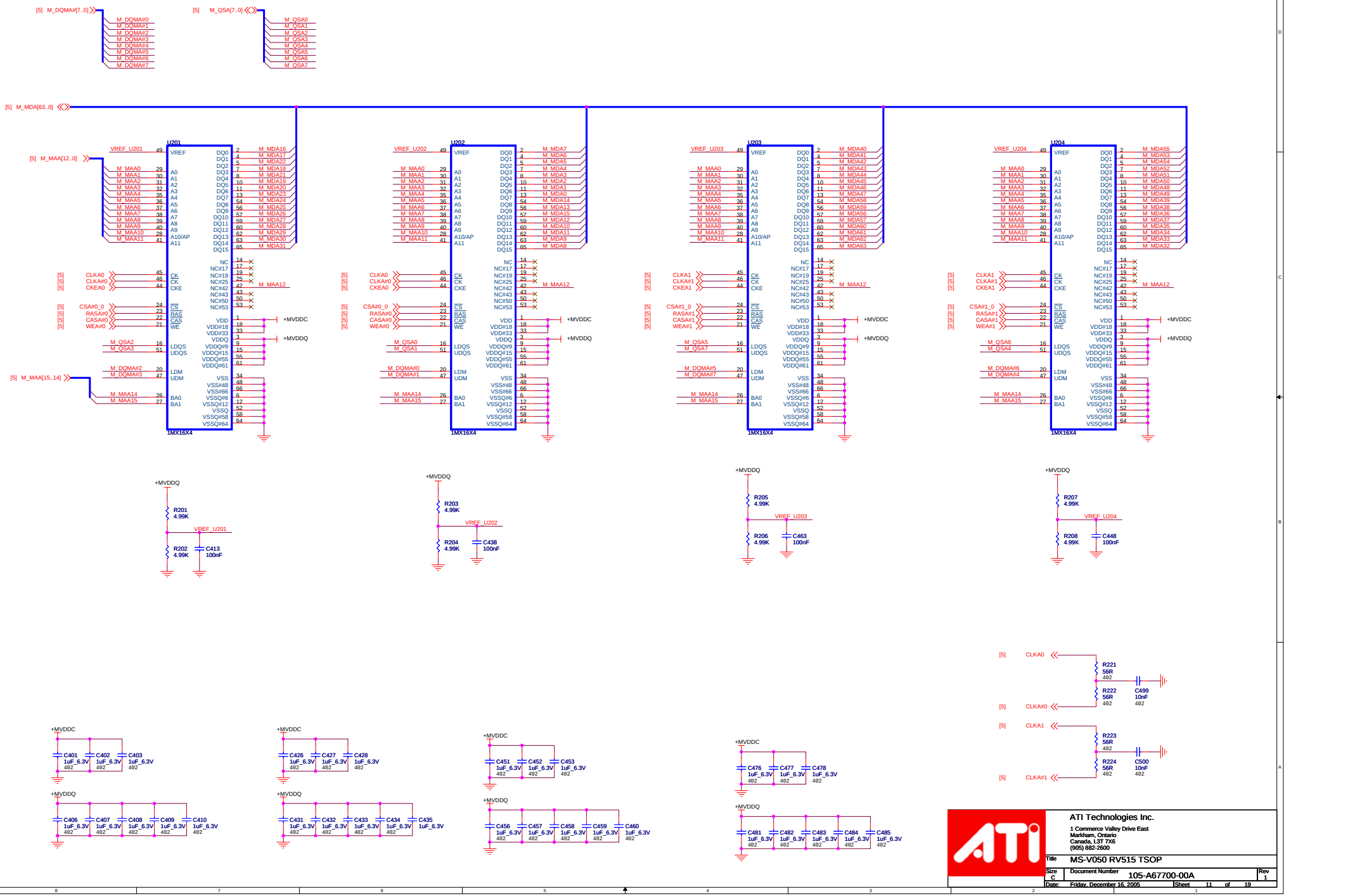
Title	MS-V050 RV515 TSOP	
Size C	Document Number 105-A67700-00A	Rev 1
Date: Tuesday, December 27, 2005	Sheet 10 of 19	

CHANNEL A: RANK 0 128/256MB DDR1



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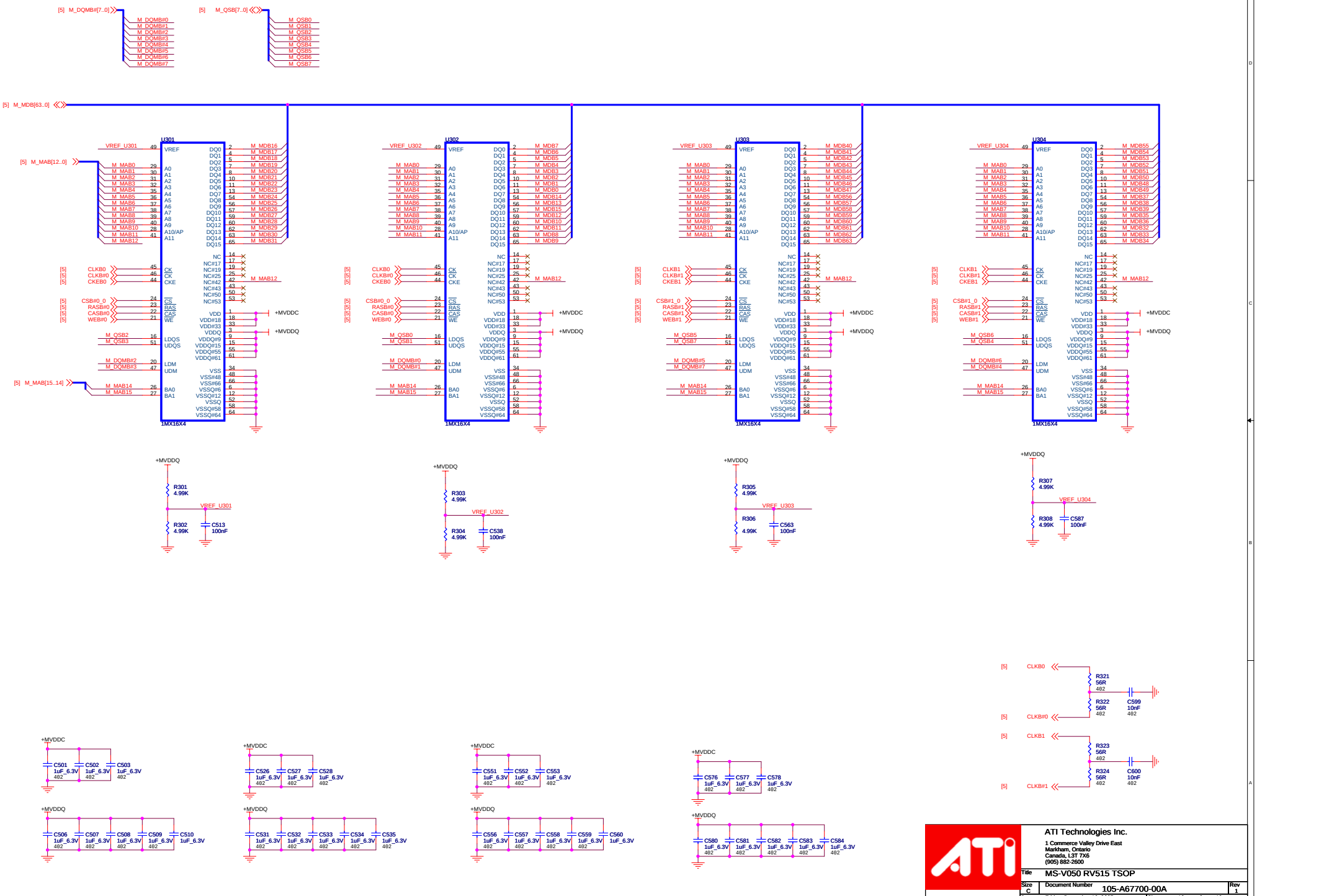
Title	MS-V050 RV515 TSOP	
Size C	Document Number 105-A67700-00A	Rev 1
Date: Friday, December 16, 2005	Sheet 11 of 19	

CHANNEL B: RANK 0 128/256MB DDR1



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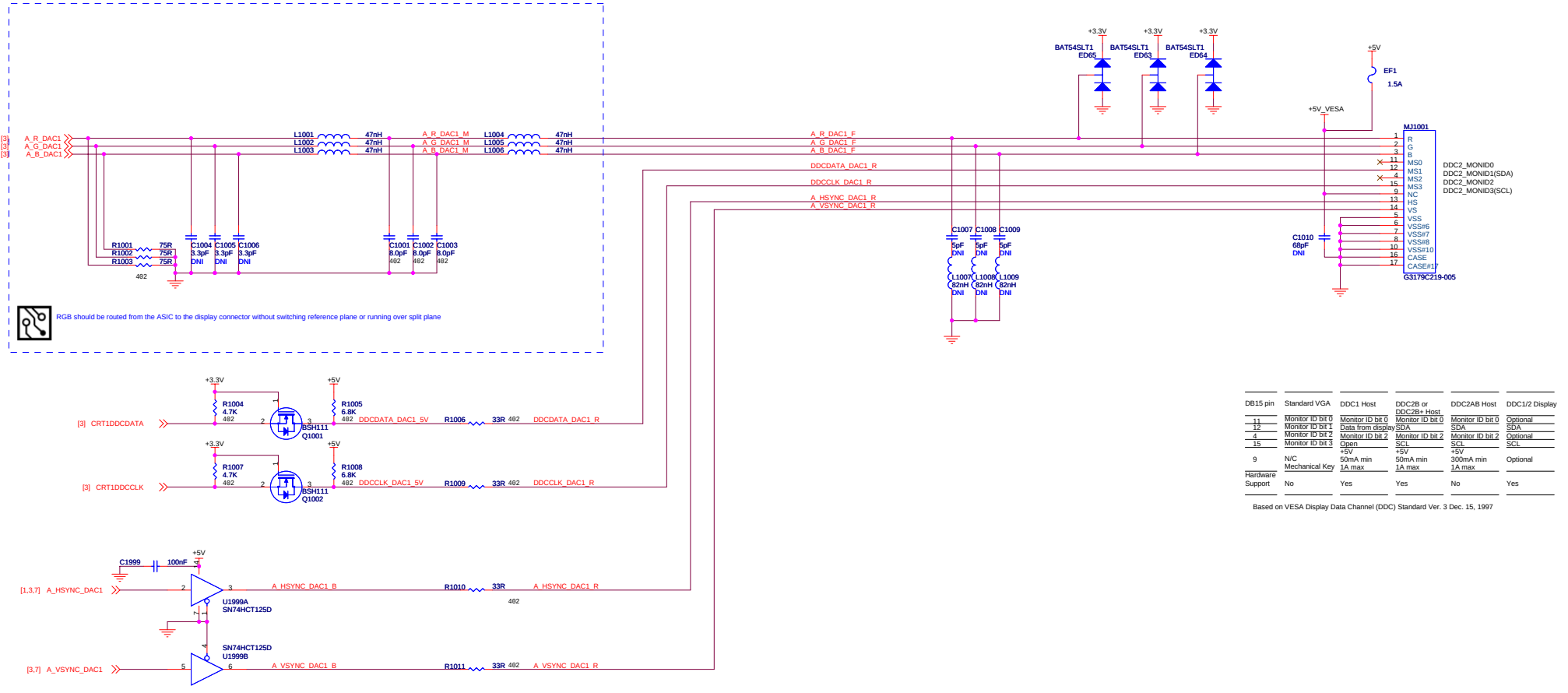
Size C	Document Number 105-A67700-00A	Rev 1
Date: Friday, December 16, 2005	Sheet 12 of 19	



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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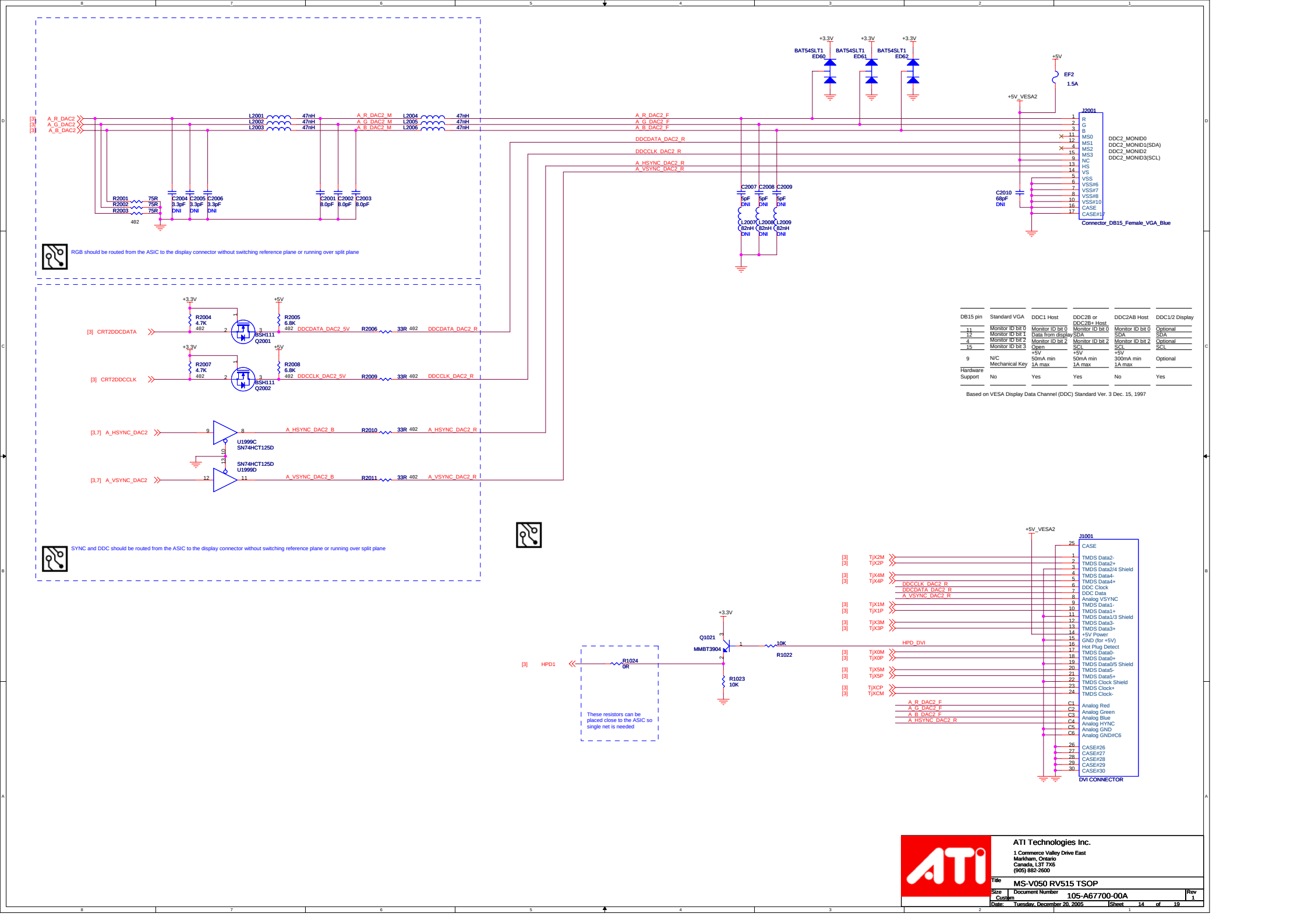
Title	MS-V050 RV515 TSOP	
Size: Custom	Document Number: 105-A67700-00A	Rev: 1
Date: Tuesday, December 20, 2005	Sheet 13 of 19	



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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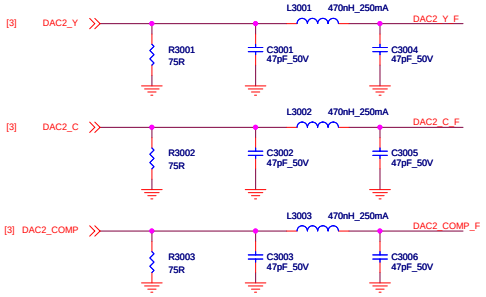
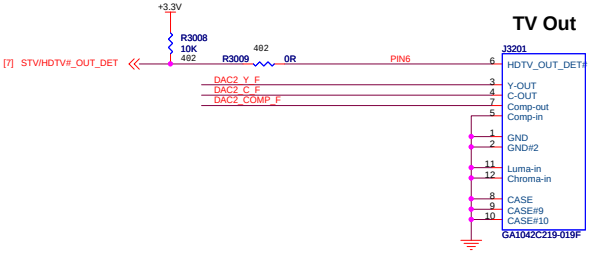
Size: Custom	Document Number: 105-A67700-00A	Rev: 1
Date: Tuesday, December 20, 2005	Sheet 14 of 19	



Place near connector
0R leaves footprint for Ferrite Beads if req'd for EMI



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

7 pin N56-07F0021-F02

9 pin N56-09F0031-F02

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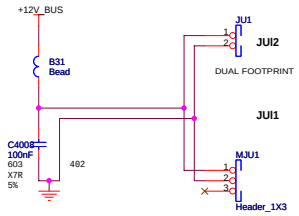
Size C	Document Number 105-A67700-00A	Rev 1
Date: Friday, December 16, 2005	Sheet 15 of 19	



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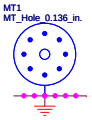
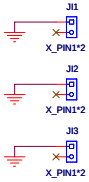
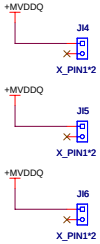
Size: C	Document Number: 105-A67700-00A	Rev: 1
Date: Friday, December 23, 2005	Sheet 16 of 19	







<Variant Name>

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Size: C	Document Number: 105-A67700-00A	Rev: 1
Date: Friday, December 23, 2005	Sheet 17 of 19	

<variant Name>

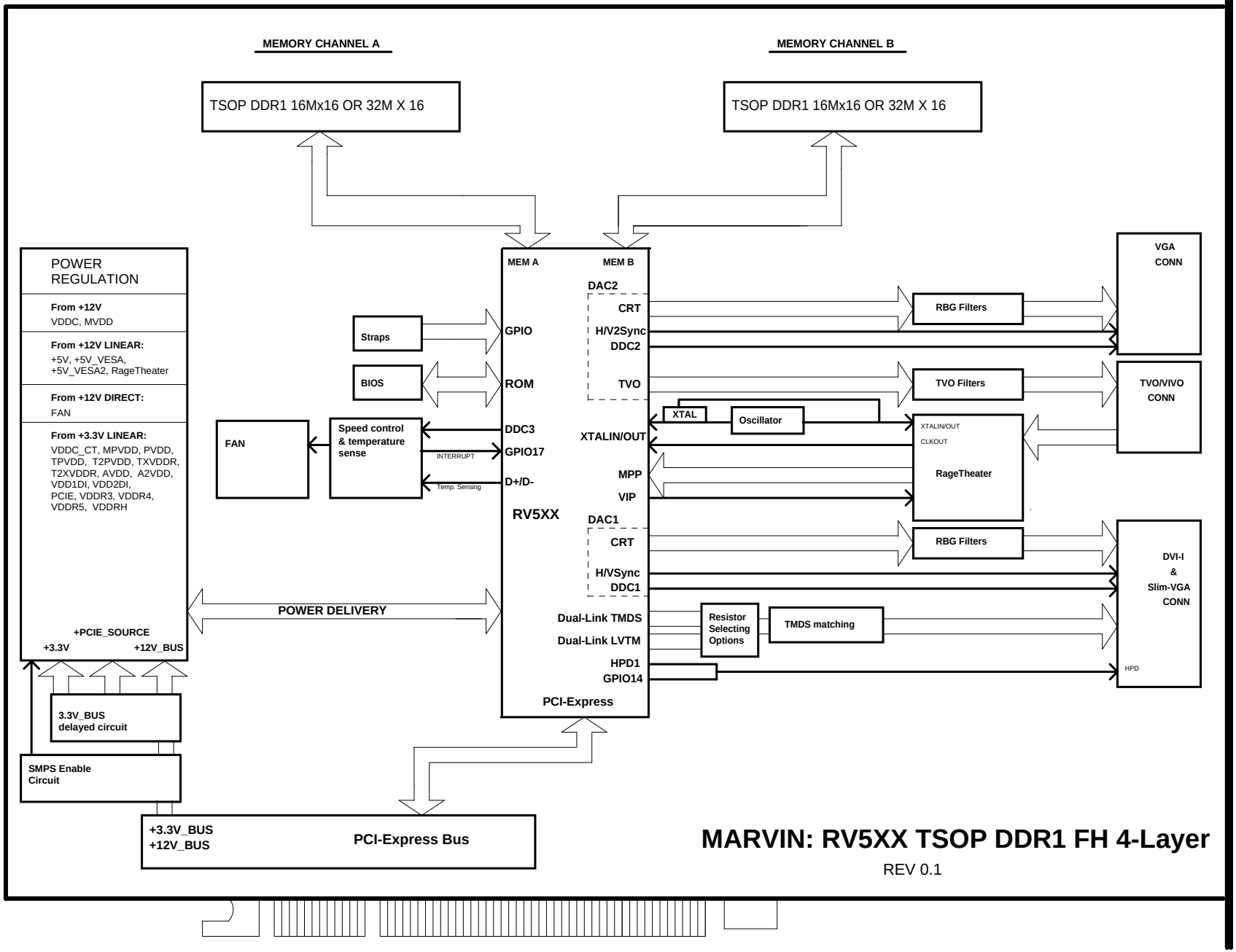
Title	Schematic No.	Date:
RV515/530 ATX VGA DVI VIVO 256/512MB TSOP	105-A67700-00A	**Thursday, October 13, 2005**

REVISION HISTORY

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
		06/29/05	DERIVE FROM A666
0	00A	07/27/05	(pg 01) Correct clock circuitry to support RT (pg 08) Swap R603 and R604 to match layout for documentation purposes (pg 09) Swap R703 and R704 to match layout for documentation purposes (pg 10) Add MVDD linear regulator option (pg 11) Add R986, R987, R988; replace redundant power sequence circuit with +5V_EN and MVDD_EN (pg 11) Add MR911, R918 for +MPVDD for no-tracking option (pg 16) Change C3103 to 603 footprint, change RT to power from 3.3V_BUS to avoid leakage, remove redundant RT clock resistors

V050-10



MARVIN: RV5XX TSOP DDR1 FH 4-Layer

REV 0.1

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Size C	Document Number 105-A67700-00A	Rev 1
Date: Tuesday, December 13, 2005	Sheet 19 of 19	