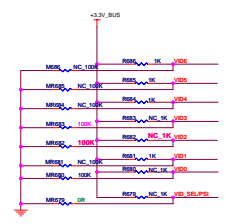


U1J		
XB49	SP_RX0P	SP_TX0P
XB41	SP_RX0N	SP_TX0N
XB50	SP_RX1P	SP_TX1P
XB52	SP_RX1N	SP_TX1N
XB48	SP_RX3P	SP_TX3P
XB49	SP_RX2N	SP_TX2N
XB51	SP_RX3P	SP_TX3P
XB52	SP_RX3N	SP_TX3N
XB48	SP_RX4P	SP_TX4P
XB49	SP_RX4N	SP_TX4N
XB51	SP_RX5P	SP_TX5P
XB52	SP_RX5N	SP_TX5N
XB48	SP_RX6P	SP_TX6P
XB49	SP_RX6N	SP_TX6N
XB51	SP_RX7P	SP_TX7P
XB52	SP_RX7N	SP_TX7N
XB48	SP_RX8P	SP_TX8P
XB49	SP_RX8N	SP_TX8N
XB51	SP_RX9P	SP_TX9P
XB52	SP_RX9N	SP_TX9N
XB48	SP_RX10P	SP_TX10P
XB49	SP_RX10N	SP_TX10N
XB51	SP_RX11P	SP_TX11P
XB52	SP_RX11N	SP_TX11N
XB48	SP_RX12P	SP_TX12P
XB49	SP_RX12N	SP_TX12N
XB51	SP_RX13P	SP_TX13P
XB52	SP_RX13N	SP_TX13N
XB48	SP_RX14P	SP_TX14P
XB49	SP_RX14N	SP_TX14N
XB51	SP_RX15P	SP_TX15P
XB52	SP_RX15N	SP_TX15N
XB47	SP_REFCLKP	SP_CALRP
XB48	SP_REFCLKN	SP_CALRN

RV770 GLA11

Output Voltage Program (VBD10.x +VID6)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output Voltage
1	1	0	1	1	0	0	1.5500
1	1	0	1	1	0	1	1.5250
1	1	0	1	1	1	0	1.5000
1	1	0	1	1	1	1	1.4750
1	1	1	0	0	0	0	1.4500
1	1	1	0	0	0	1	1.4250
1	1	1	0	0	1	0	1.4000
1	1	1	0	0	1	1	1.3750
1	1	1	0	1	0	0	1.3500
1	1	1	0	1	0	1	1.3250
1	1	1	0	1	1	0	1.3000
1	1	1	0	1	1	1	1.2750
1	1	1	1	0	0	0	1.2500
1	1	1	1	0	0	1	1.2250
1	1	1	1	0	1	0	1.2000
1	1	1	1	0	1	1	1.1750
1	1	1	1	1	0	0	1.1500
1	1	1	1	1	0	1	1.1250
1	1	1	1	1	1	0	1.1000

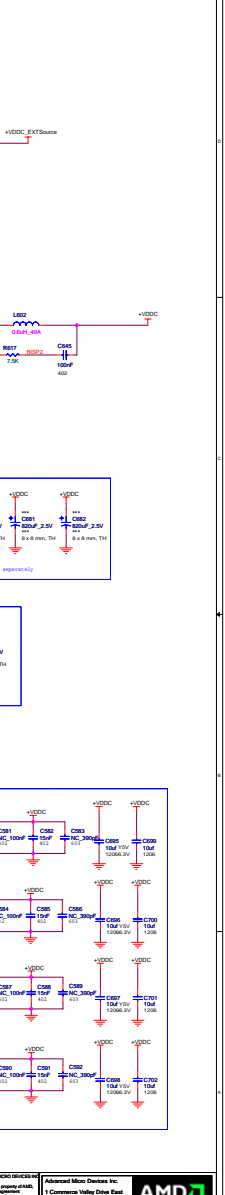
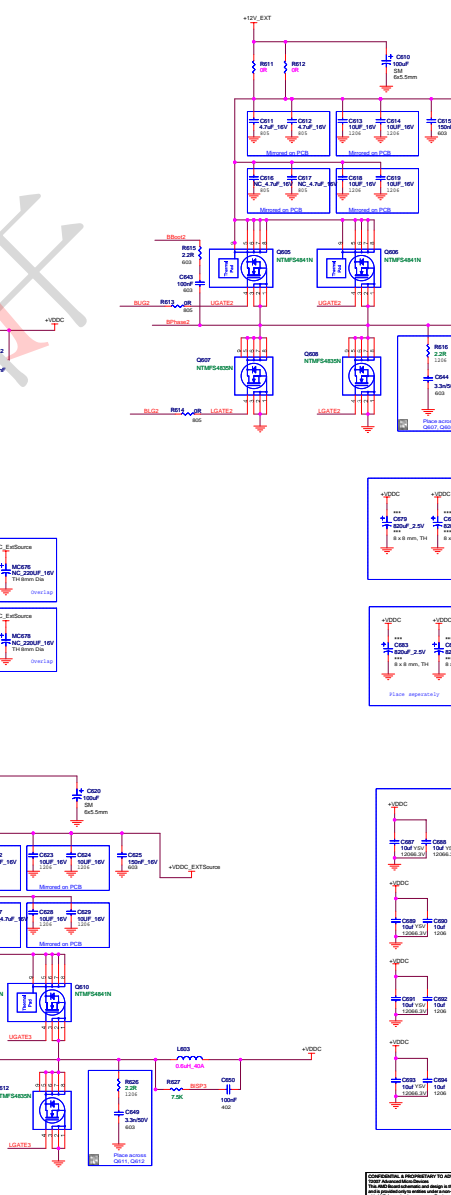
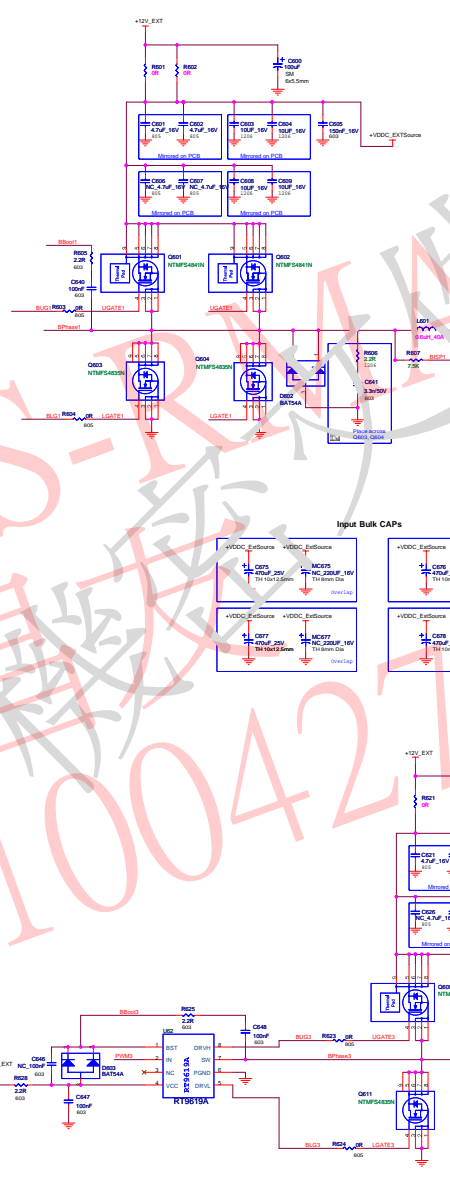
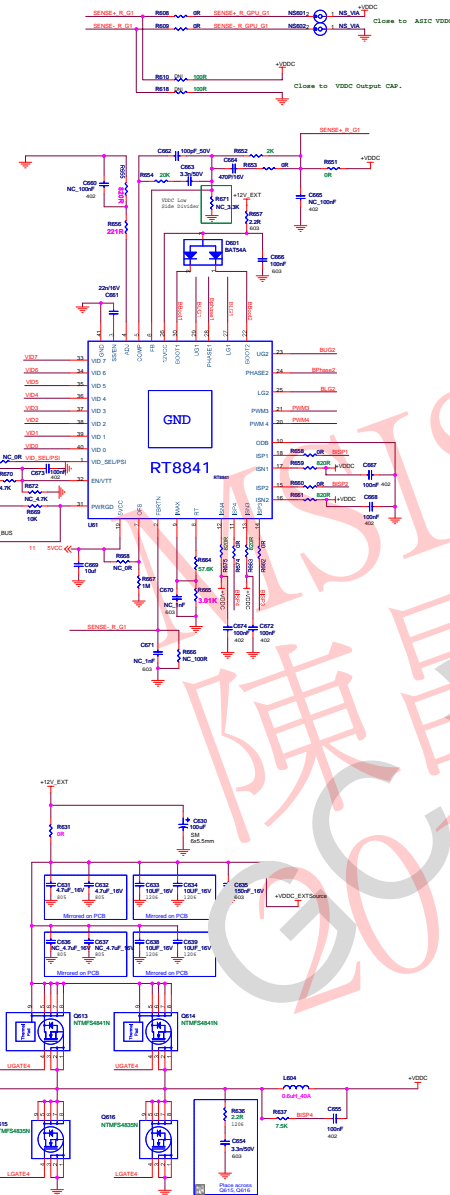


SVID Setting


VID3[5] = 11, VDDCmax = 1.10V
 VID3[2] = 10, VDDCmax = 1.20V
 VID3[2] = 01, VDDCmax = 1.30V
 VID3[2] = 00, VDDCmax = 1.40V

SVID VDDC Programming

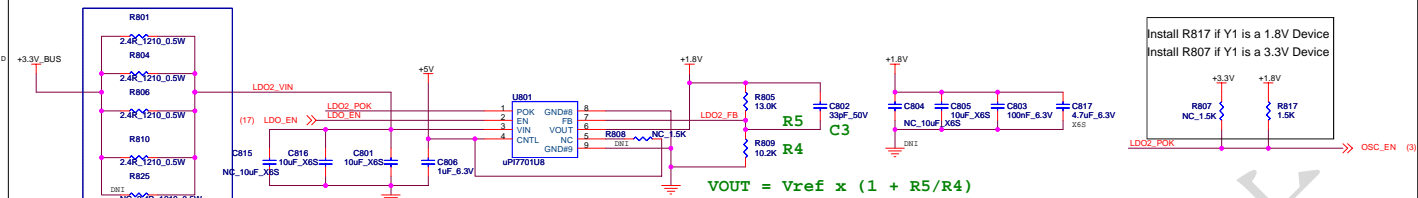
VID[4:1]	VDDC
00	SWRUS Voltage 1: 30
01	SWRUS Voltage 2: 30
10	SWRUS Voltage 3: 30
11	SWRUS Voltage 4: Reserved



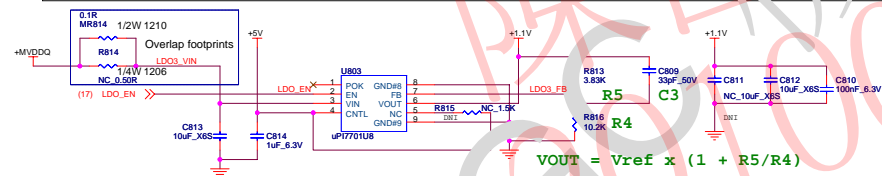
MSIS-RMA#
陳昌友
20100427

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<small>Date: Thursday, October 09, 2008</small>		<small>Rev 1</small>			
<small>Sheet 13 of 22</small>					
<small>Title RH RV770 GDDR5 DV-H VO DV-H FH</small>		<small>Doc No:</small>		<small>105-B507xx-10</small>	

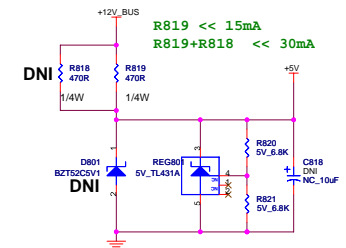
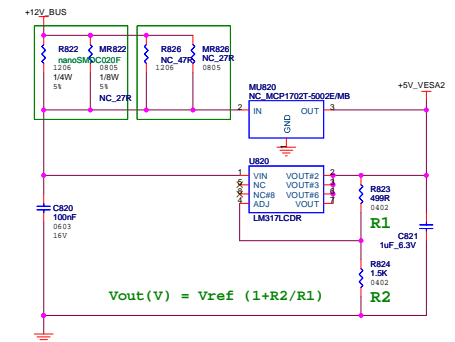
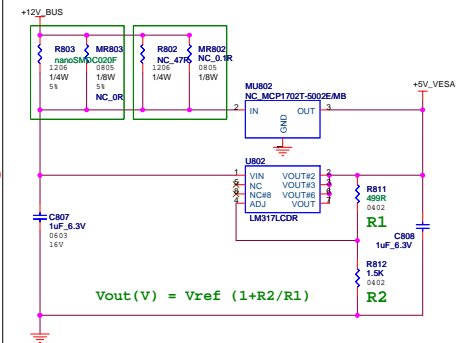
LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 1.7A (TBV) RMS MAX
PCB: Min 70mm sq. copper area for cooling




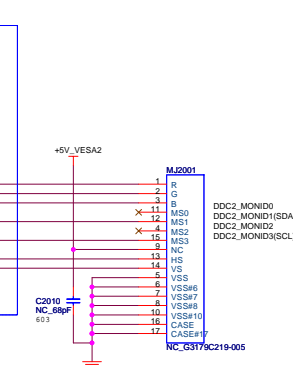
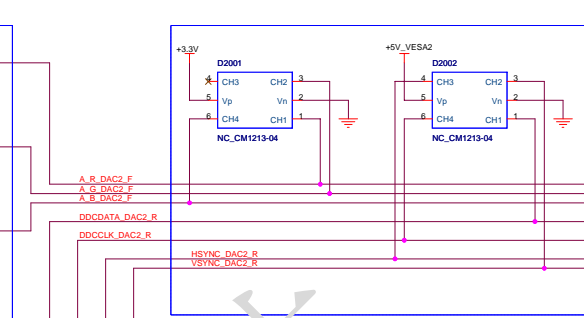
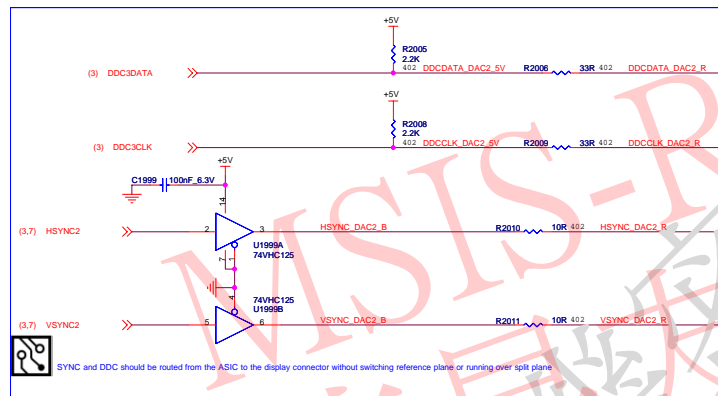
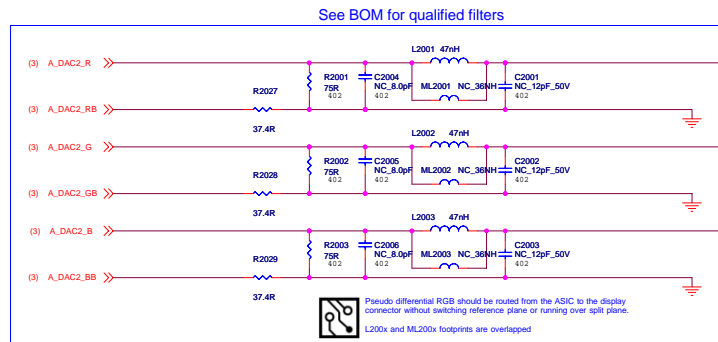
LDO #3: Vin = +1.50V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX
PCB: Min 70mm sq. copper area for cooling



Regulators for +5V, +5V_VESA and +5V_VESA2



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Date: Thursday, October 09, 2008		Rev:	
Sheet 14 of 22			
Title: RH RV770 GDDR5 DVI-I VO DVI-H		Doc No: 105-B507xx-10	



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC3AB Host	DDC1/2 Display
1	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional
2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
3	Monitor ID bit 3	Monitor ID bit 3	Monitor ID bit 3	Monitor ID bit 3	Optional
4	Monitor ID bit 4	Monitor ID bit 4	Monitor ID bit 4	Monitor ID bit 4	Optional
5	Monitor ID bit 5	Monitor ID bit 5	Monitor ID bit 5	Monitor ID bit 5	Optional
6	Open	Open	Open	Open	Optional
7	NC	NC	NC	NC	Optional
8	NC	NC	NC	NC	Optional
9	NC	NC	NC	NC	Optional
10	NC	NC	NC	NC	Optional
11	NC	NC	NC	NC	Optional
12	NC	NC	NC	NC	Optional
13	NC	NC	NC	NC	Optional
14	NC	NC	NC	NC	Optional
15	NC	NC	NC	NC	Optional

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

