Revision History

Schematics taken from P151-A00-X24

MS-8889 00A

00A-0621
1)Page 10,13,18 of the original design (P151) has been delete.
2)Page 10,12 U816,U817,U818,U811(single gate) share one ACT08/SO8.
3.Page 13 a.P300 change reference to P600.
b.Add P300 (long D-sub)for SEC D-sub.
4.Page 14 a.Remove P602.
b.Add S_OUT1,S_IN1,AV_OUT1,AV_IN1,J1,J2 connector.
5.Page 16,17 Modify power supply solution.
a.PWM from SC1102A,SC1541-3.3V,SC1565 share one ISL6529.
b.FBVDDQ is transfered from Q800,U4 by 5V.
c.SC2610 change to HIP6012.

00A-0624
1)Page 16 a.Remove C1250,C1251,R1076,R1071,Q10,U4,Q800.
b.FBVDDQ Remove Q800 and U4 ,Add U812/NIKO-108SS/TO-263.
c.Q905 and Q201 from 45N02LD change to 55N02LD for low Rdson.
2)page 17 Remove Q9,R2086,Q8,R2087.
3)page 11 Add R2217/33ohm and C2495 for "DVOCLK_IN".
4)page 15 change Text Note "PCI_DEVID =253" to "PCI_DEVID =283".
5)page 17 a.R2085 change value to 4.7K.
b.U3 change refernce to U813.

00A-0625
1)Page 16 ADD C1250,C1251,R1076,C1071.
2)page 9 a.ADD RP16/47ohm for "DVOBD12" and "DVOBD13".
b.Add solder side heat sink "K201"
3)page 11 Add SAA7104/5.

00A-0626
1)Page 9 - Change the 47ohm RPack to 33ohm RPack.
2)Page 2 - a.ADD C106/4.7U for "12V to gnd".
b.R80,R81,R82,and R83 from 5% change to 1%.
3)Page 16 - U812 from L1085/3A change to L1084/5A for FBVDDQ.
4)Page 14 - S_OUT1 & S_IN1 chage to P500 & P501.

00A-0701
1)Page 2 - a.ADD thermal sensor RT1 (in GPU solder side).
b.ADD C113/220PF "AGPVREFCG" pull down.
2)Page 14 - Remove J1.
4)Page 16 - a.Remove C1406.
b.ADD CE1,CE2,CE3,CE4 for EMI (FBVDD bypass).
c.ADD R617/1K,R618/6.8K,C1406/470PF for U814.
5)Page 17 - ADD C2307,C2308 for "FBVDDQ".

00A-0702
1)Page 2 - a.Make R80 = 49.9 ohms 1%, Make R81 =
NO_STUFF, Make R82 = 56.2 ohms 1%, and
Make R83 = NO_STUFF.
b.C110 from 0.1uF change to 0.01uF
C113 from 220PF change to 0.22uF
2)Page 16/17 - R617, R618, R624, R616, R1080, R1082,
R1210, R1104, R2085, R2083, R2082 all be 1%.

00A-0703
1)Page 2 - Add R111,R112 0ohm for thermal sensor.
2)Page 11 - Remove U1 7104H/QFP64.

00A-0704
1)Page 11 - Remove R2218.
2)Add 8.a H/W MONITOR for channel only, Medion NO_STUFF.
3)Page 17 - Add C2235 for 12V to GND.

00A-0708
1)Page 2 - RT1 footprint from SMD change to DIP.

00A-0709
1)Page 16 - Remove C1276,C1264,C1366,C1267,C1301,C1379,C1304.
2)Page 5,6,7,8 - Add C550-C565 / 10PF / 0402 from
"FB(A/B/C/D)CLK(0/0-/1/1-) total 16pcs for
EMI engineer.

00A-0712
1)Need to change Power net on R2088 sheet 17 to "12V".
Need to change Power Net on D658 sheet 17 to "12V".

00A-0716
1)Page 2 - a.R80 and R81 needs to be tied to "GND". right now it is tied to VDDQ.
b.R82 and R83 needs to be tied to "VDDQ".
Pin 'R82.2' moved to net 'VDDQ'.
Pin 'R83.2' moved to net 'VDDQ'.
Pin 'R81.1' moved to net 'GND'.
2)Page 2 - Pin 'Q901.3' moved to net 'AGP_MDT2'. This is the collector.
Pin 'Q901.1' moved to net 'AGP_MDT4'. This is the BASE.
Pin 'Q901.2' moved to net '3.3V'. This is the Emitter.
3)Page 2 - Component value changes:
a.R98 please change from 5.76K to 6.49K 1%.
b.R110 and R105 change from 1.5K to 2.32K 1%.
c.Q613 - Changed from 2N7002 to IRLML2502 (N-ch 20V 3A 0.08 on resistence).
d.Q901A - change to MMBT4403LT1.

Sub Assemblies	Description
COMMON	Components are stuffed for all SKUs
NO_STUFF	Components are not stuffed
PRI_DVI_I	Components stuffed for Primary VGA
PRI_PROT	Components stuffed for Primary Protection
SEC_DVI_I	Components stuffed for Secondary DVI
SEC_PROT	Components stuffed for Secondary Protection
AGP3VFBDQ	Components stuffed for AGP 3.3V to FBVDD
FBVDD-FBDQ	Components stuffed for FBVDDQ 2.5V to FBVDD
PLL-SEQ	Components stuffed for PLL Sequence
PWR-SEQ	Components stuffed for Power Sequence
PWR-SEQ-BP	Components stuffed for Power Sequence By-PASS
NVDD-2602	Components stuffed for NVVDD Power
FB_2610_SWT	Components stuffed for FBVDD Power
SC1541	Components stuffed for 3.3VL Fixed
SC1565	Components stuffed for SC1565 - 3.3VL Adj.
FB64LO	Components stuffed for FBA_DATA and FBD_DATA
FB64UP	Components stuffed for FBC_DATA and FBD_DATA
SER-PROM	Components stuffed for Serial PROM
PAR-PROM	Components stuffed for Parallel PROM
FAN_HS-LFT	Components stuffed for Fan / Blower left of the GPU
FAN_SNK	Fan Sink Component
HEAT_SNK	Heat Sink Component
VIVO	Components stuffed for Video IN/OUT
VIDO-7104	SAA7104 Video Out
CX-ENC-TVOUT	Components stuffed for CX25871 - TV-OUT
SOCKET	Components stuffed for Socket
64MB-4MX16	Components stuffed for Mem-CFG: 64MB (4Mx16) memory
BRACKET	IO Bracket / VGA-DIN-DVI-I
BRACKET-VGA	IO Bracket / VGA- -DVI-I
FB_2610_LDO	Components stuffed for FBVDDQ Power
FBVDD_ADJ	Components to adjust FBVVD out voltage.
FBVDQ_ADJ	Components to adjust FBVVDQ out voltage.

Table of Contents

Legend:

TPNC = Test Point - Not Connected

602-10085-0000-A03
140-10085-0000-A03

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Santa Clara, CA 95050 USA

Top Page .. P151

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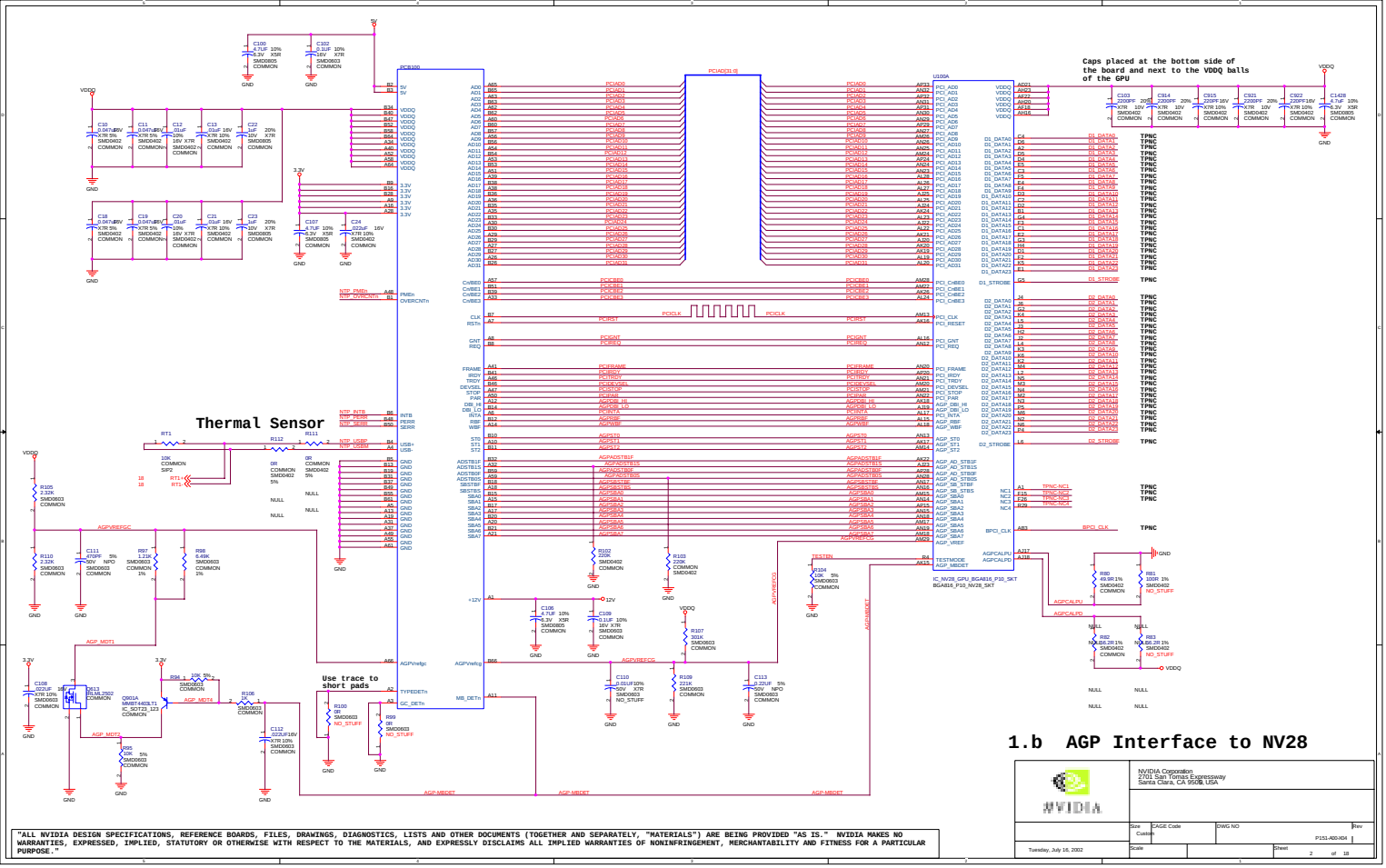

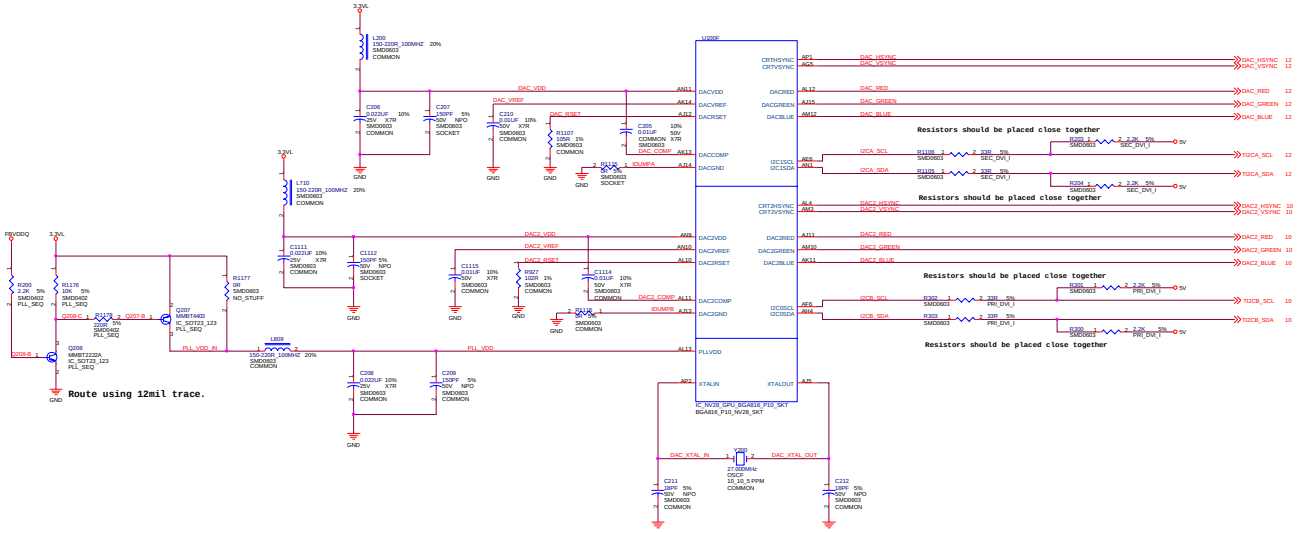

1.c NV28 .. PLL / DAC / I2C

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NV28_PL / DAC / I2C

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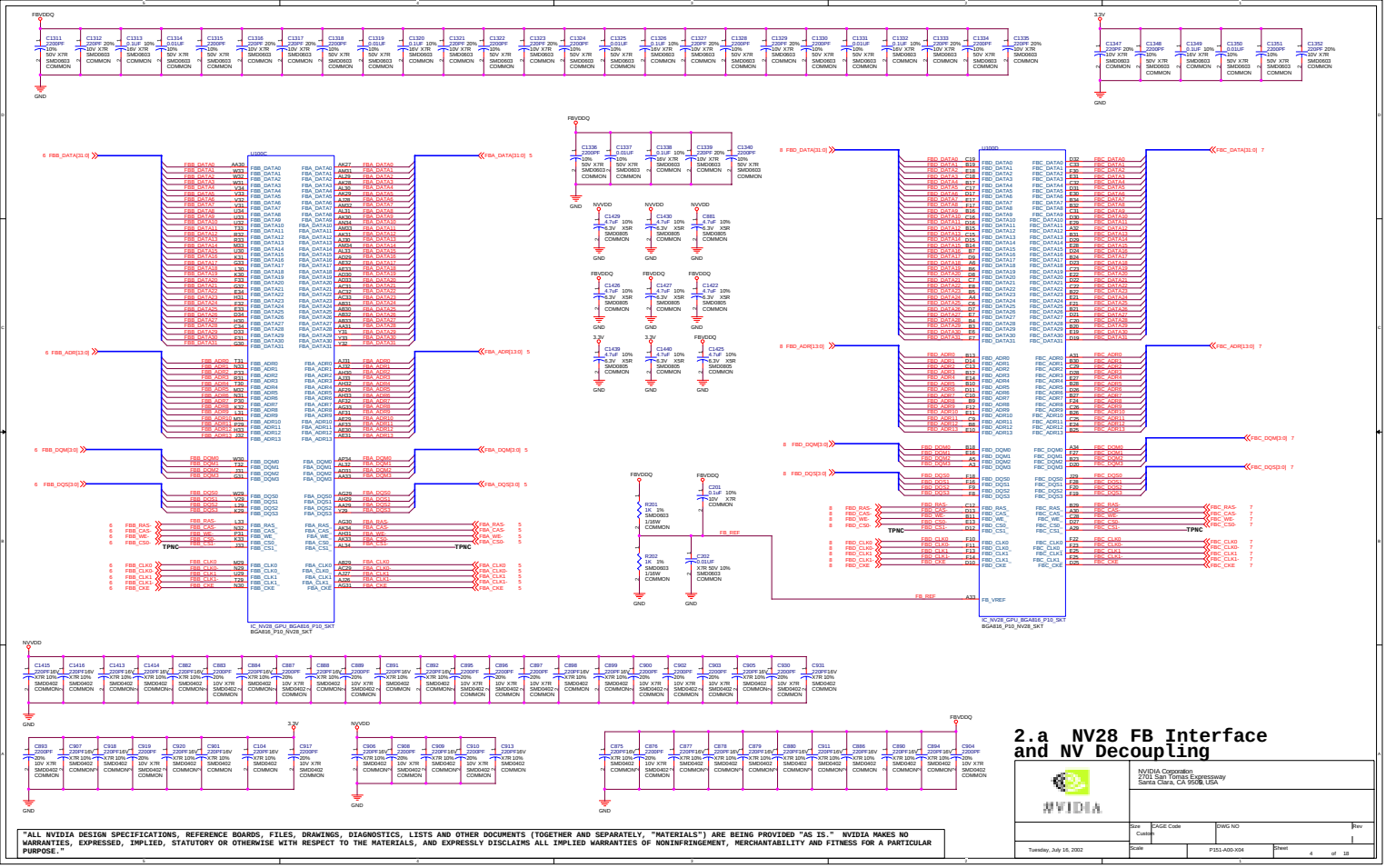

2.a NV28 FB Interface and NV Decoupling

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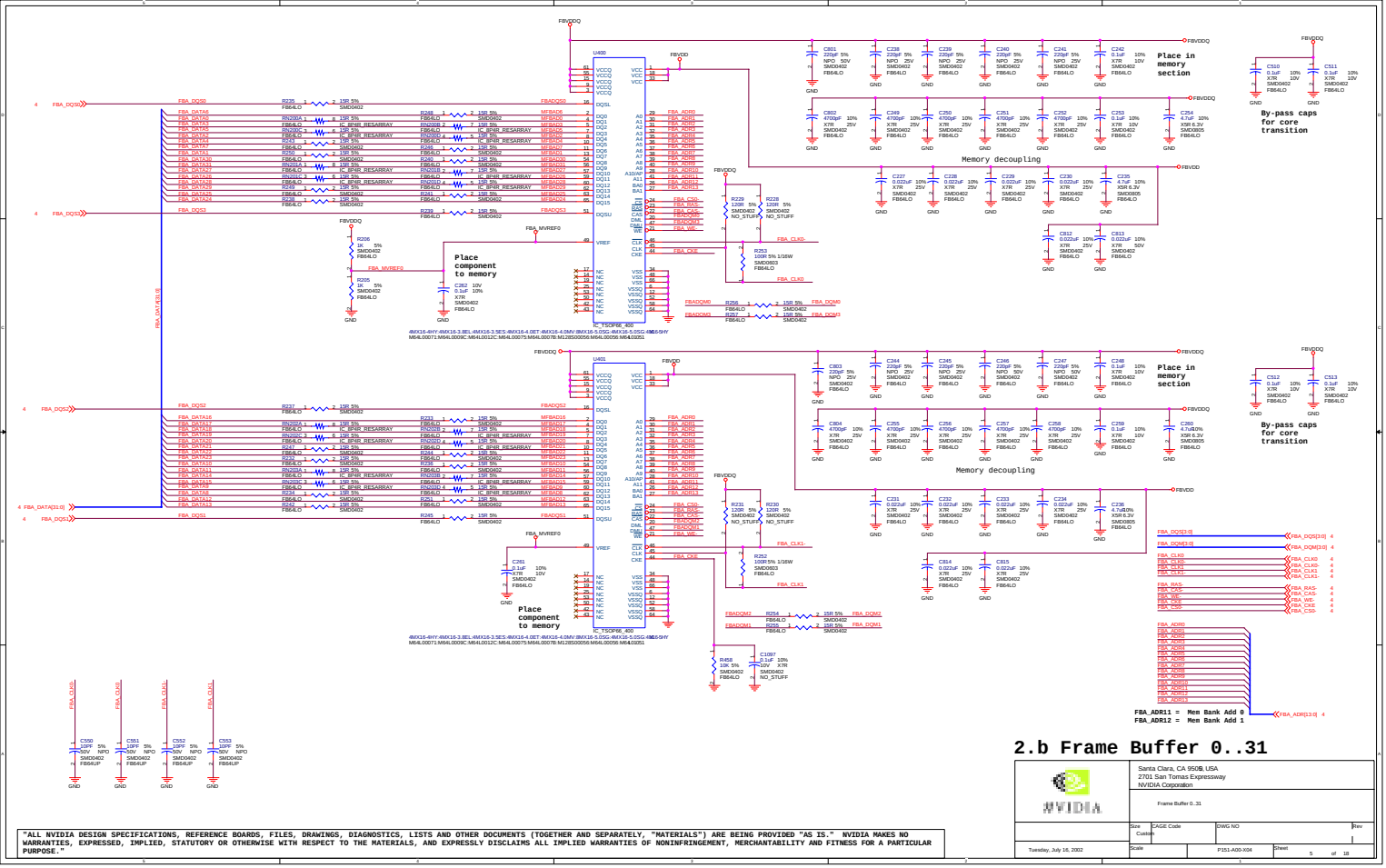

2.b Frame Buffer 0..31

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Frame Buffer 0..31

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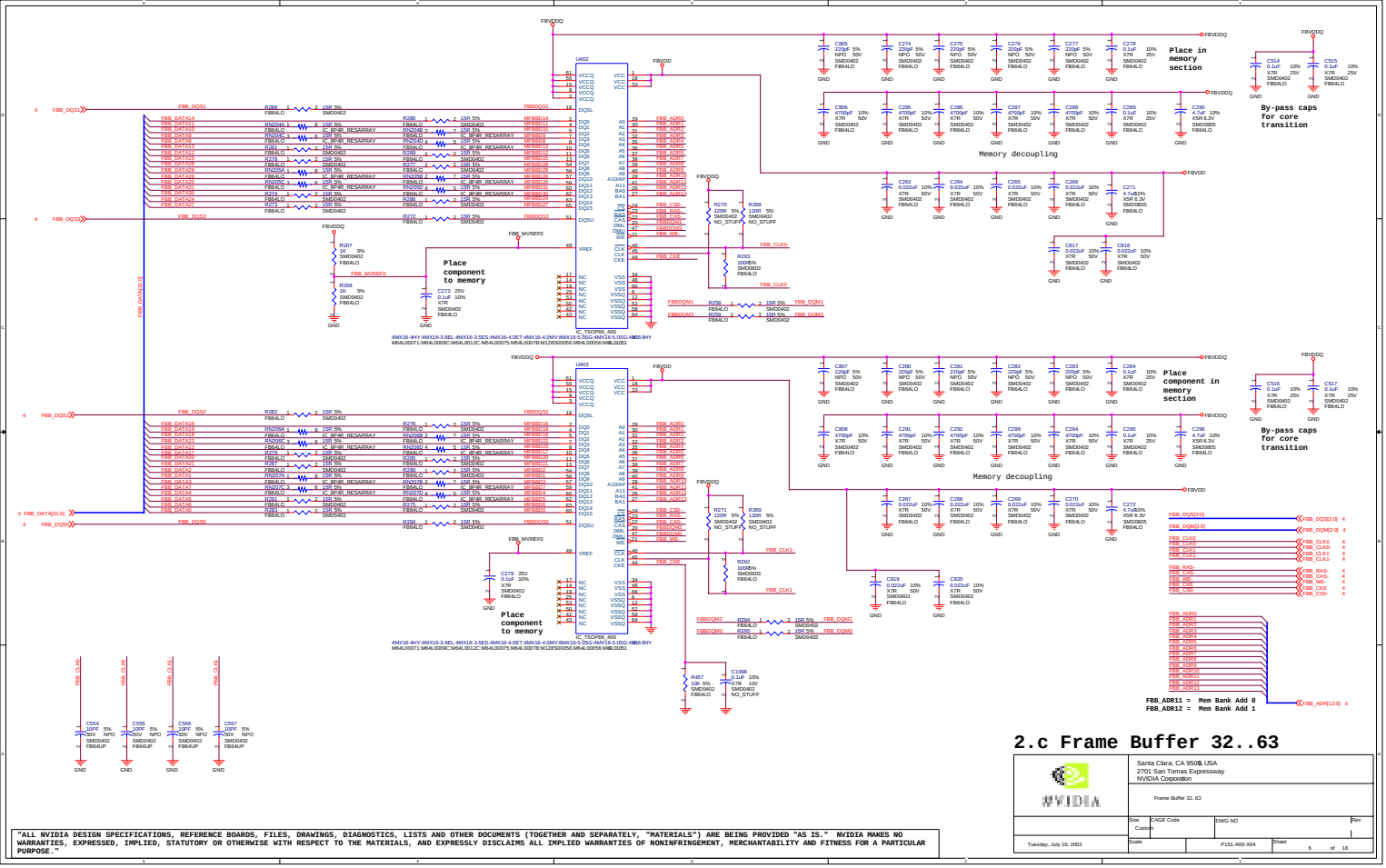

2.c Frame Buffer 32..63

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Frame Buffer 32..63

Tuesday, July 16, 2002

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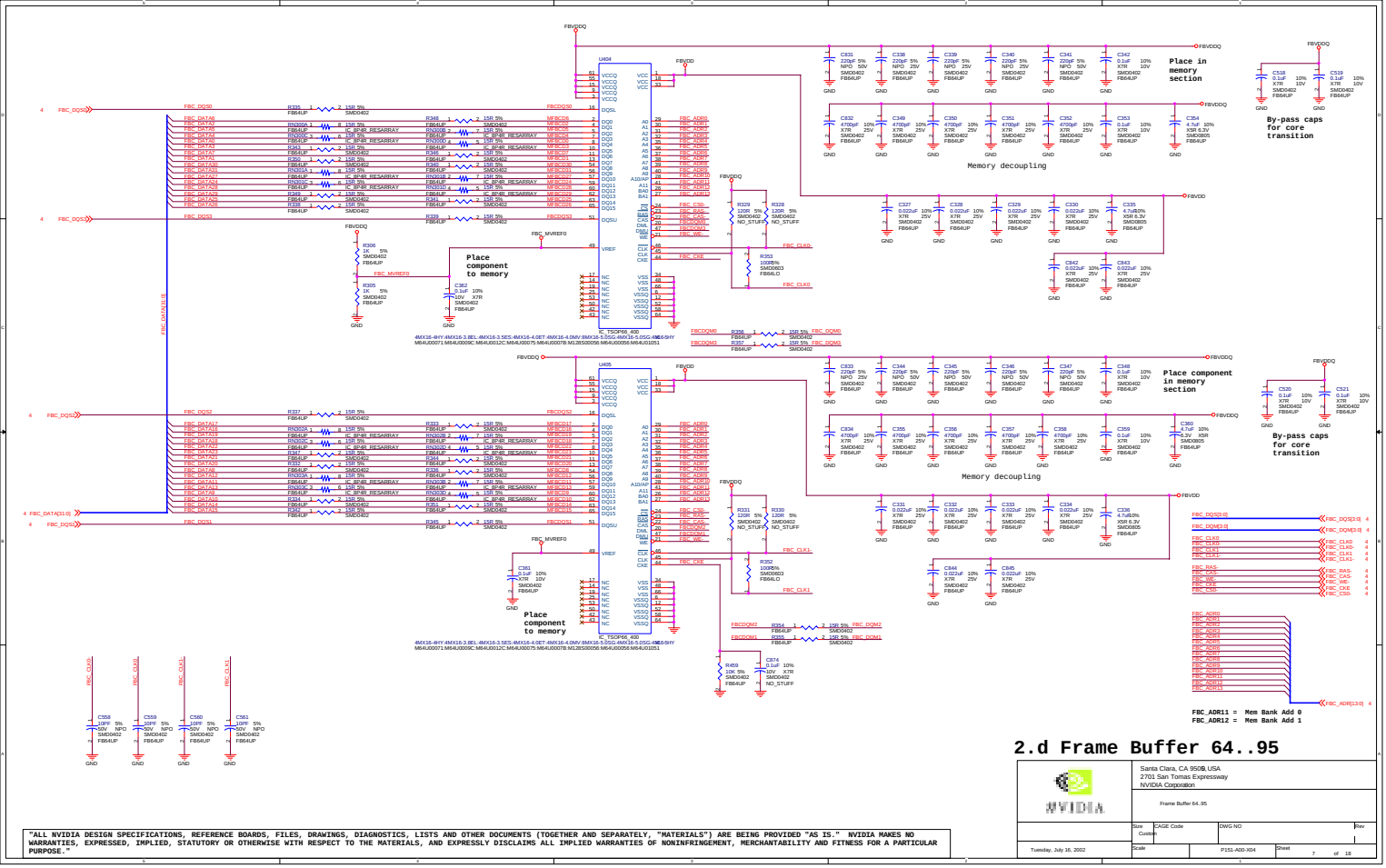

2.d Frame Buffer 64..95

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Frame Buffer 64..95

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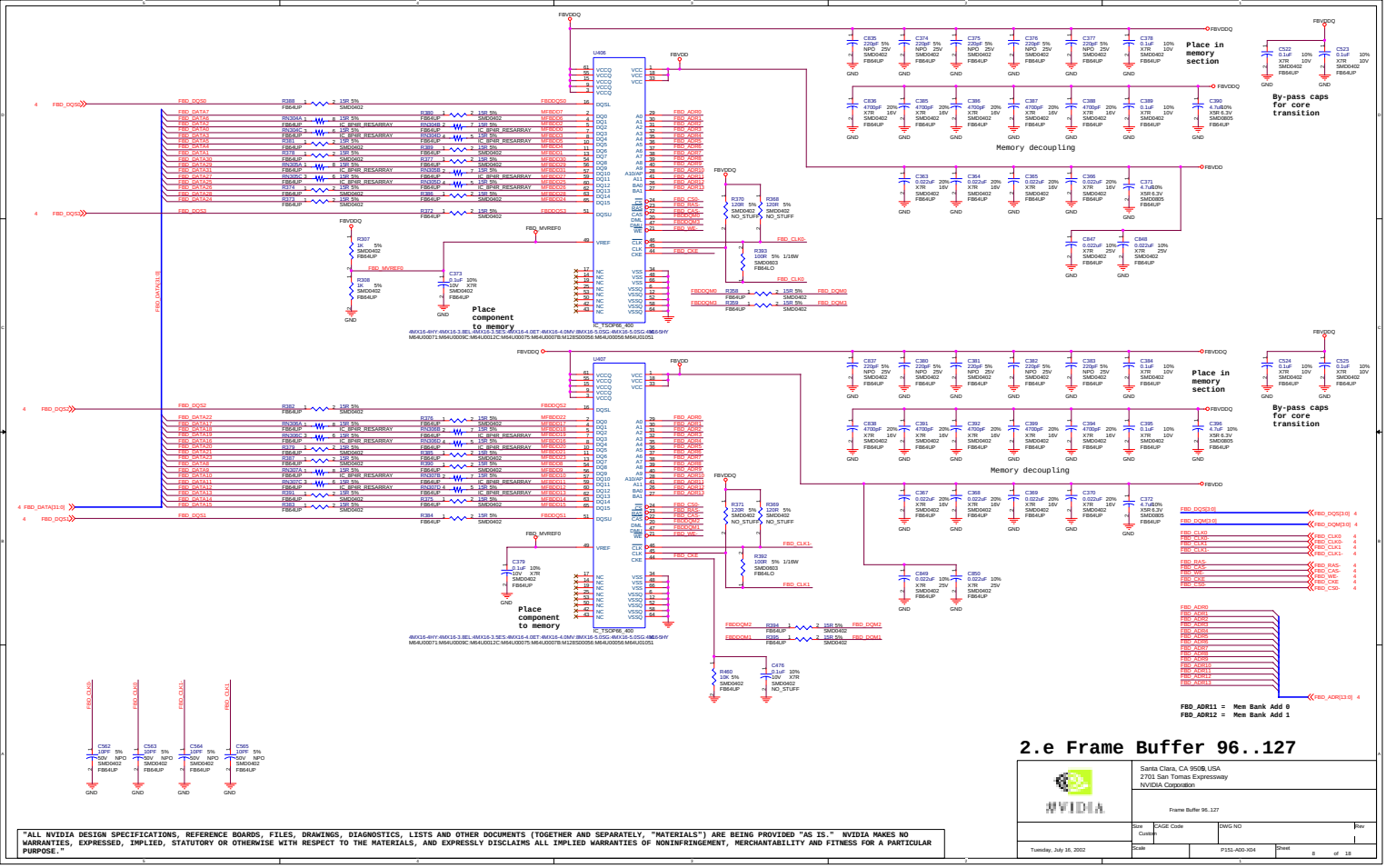

2.e Frame Buffer 96..127

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Frame Buffer 96..127

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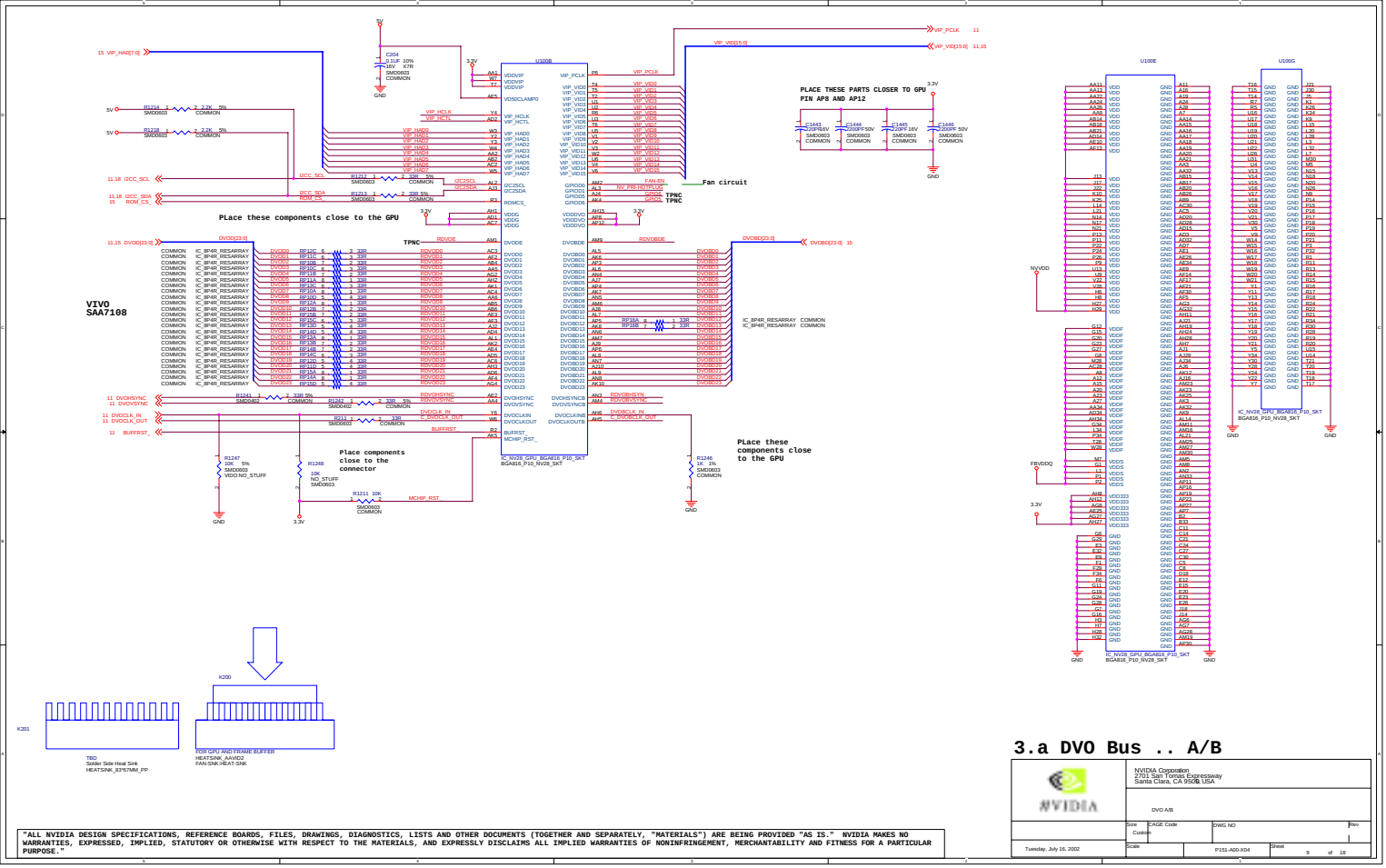

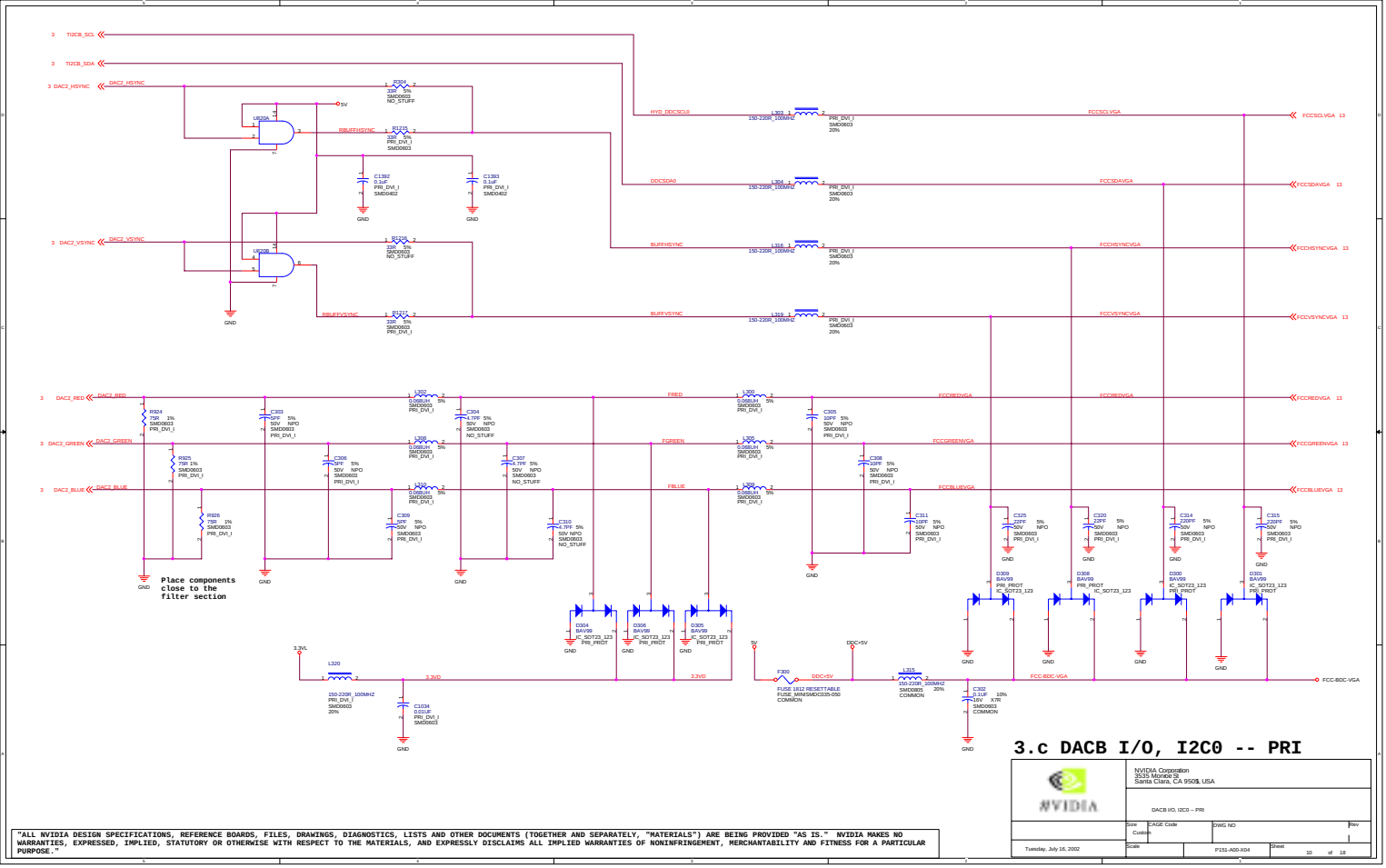

3.c DACB I/O, I2C0 -- PRI

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Santa Clara, CA 95051 USA

DACB I/O, I2C0 – PRI

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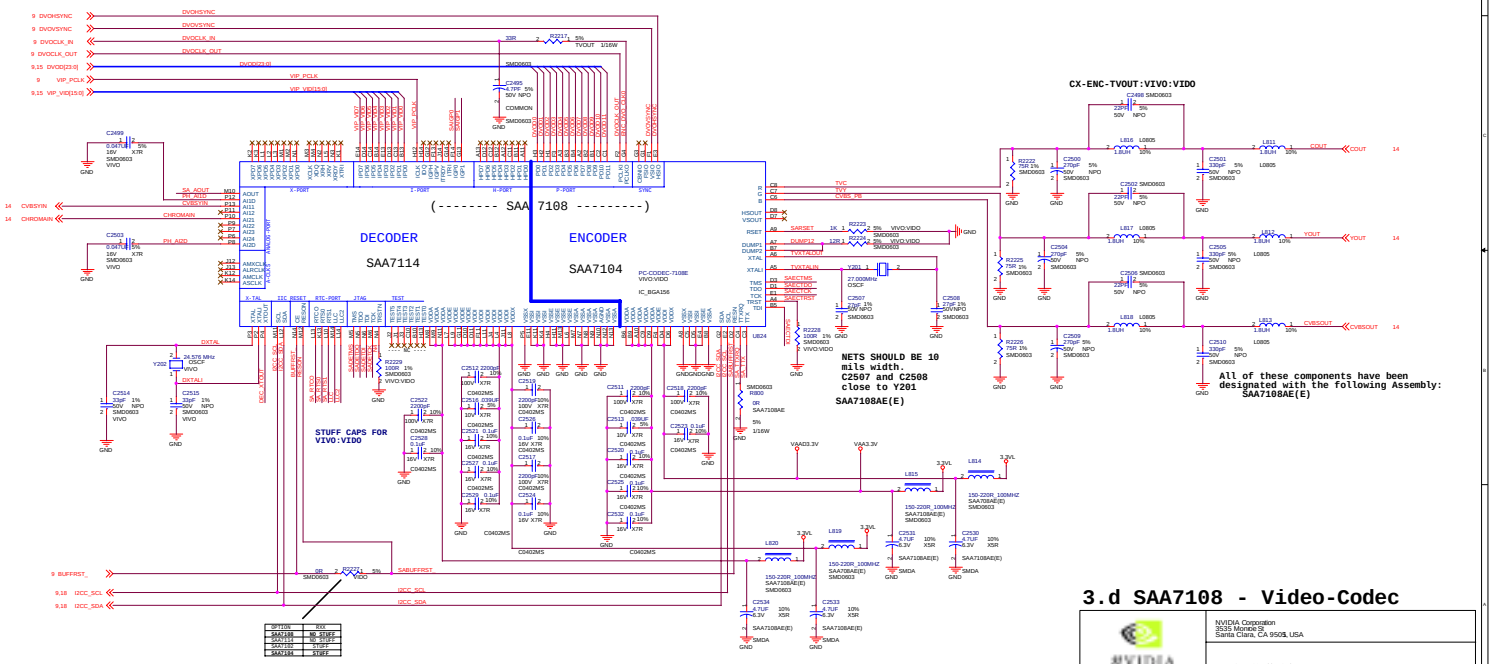

3.d SAA7108 - Video-Codec

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SAA7108 - Video-Codec			
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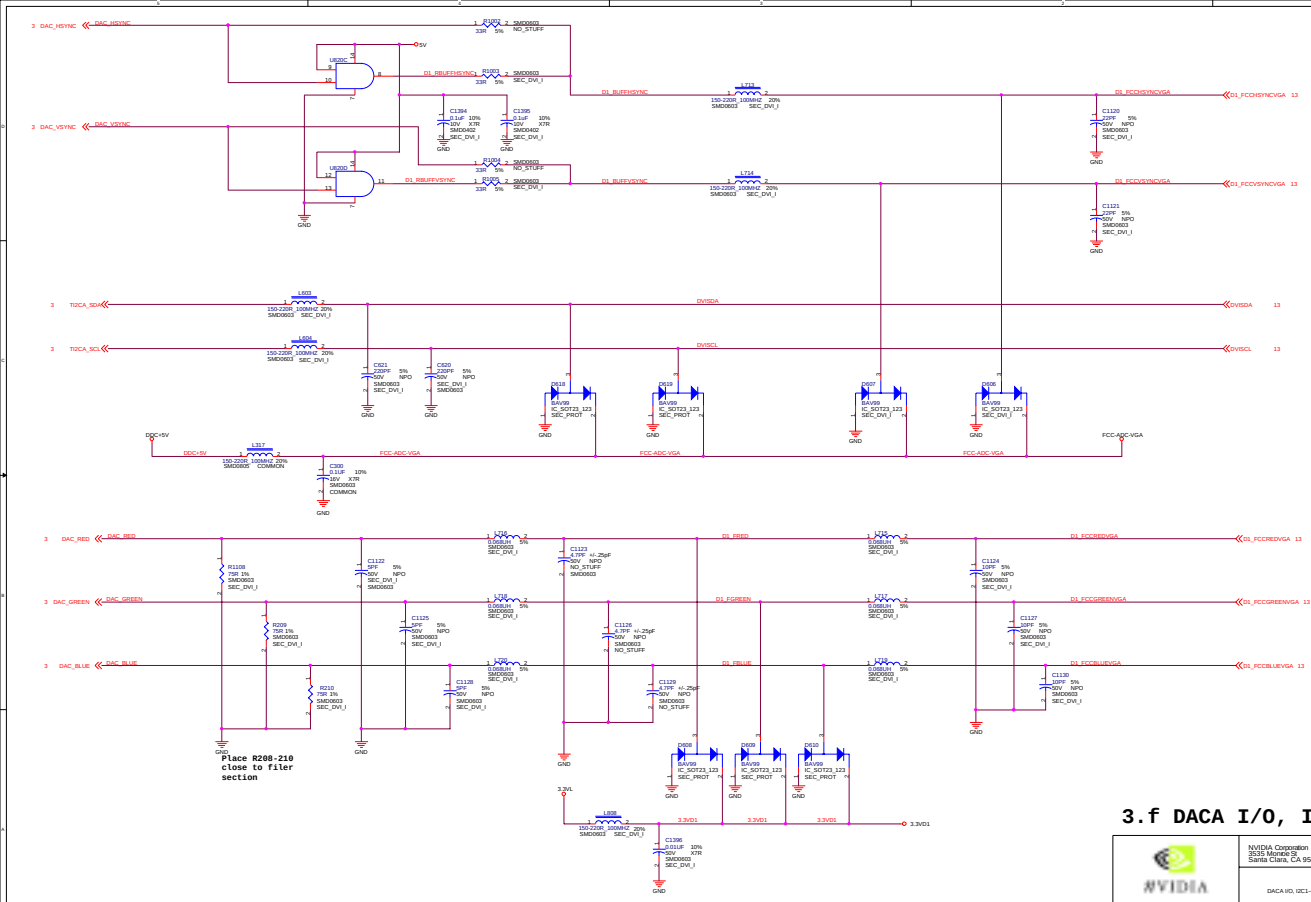

3.f DACA I/O, I2C1-- SEC

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DACA I/O, I2C1-- SEC

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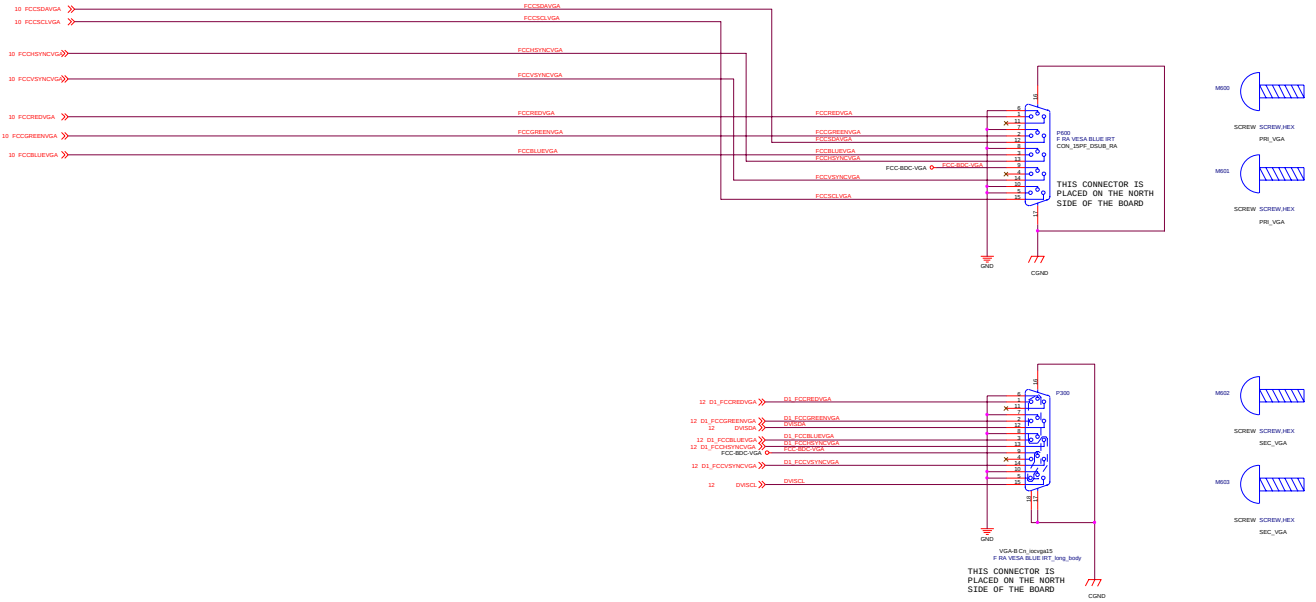

3.g DACB(A)/VGA-DB15 Connectors

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DACB(A)/VGA-DB15 Connectors

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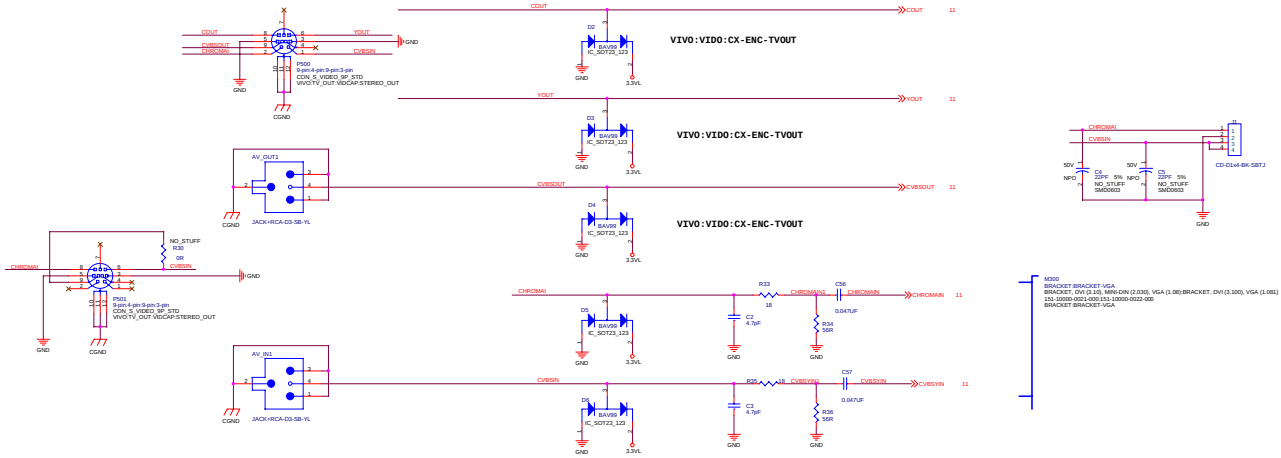
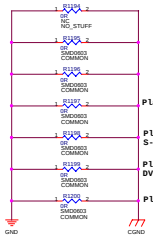


X-Components

All of these components have been designated with the following Assembly: VIVO

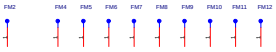


Place resistor above VGA connector

Place resistor between the DVI and S-Video connectors

Place resistor below S-Video and DVIconnectors

Place resistor below the DVIconnector



3.h Connector - S-Video-Vidcap.

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Connector - S-Video-Vidcap.

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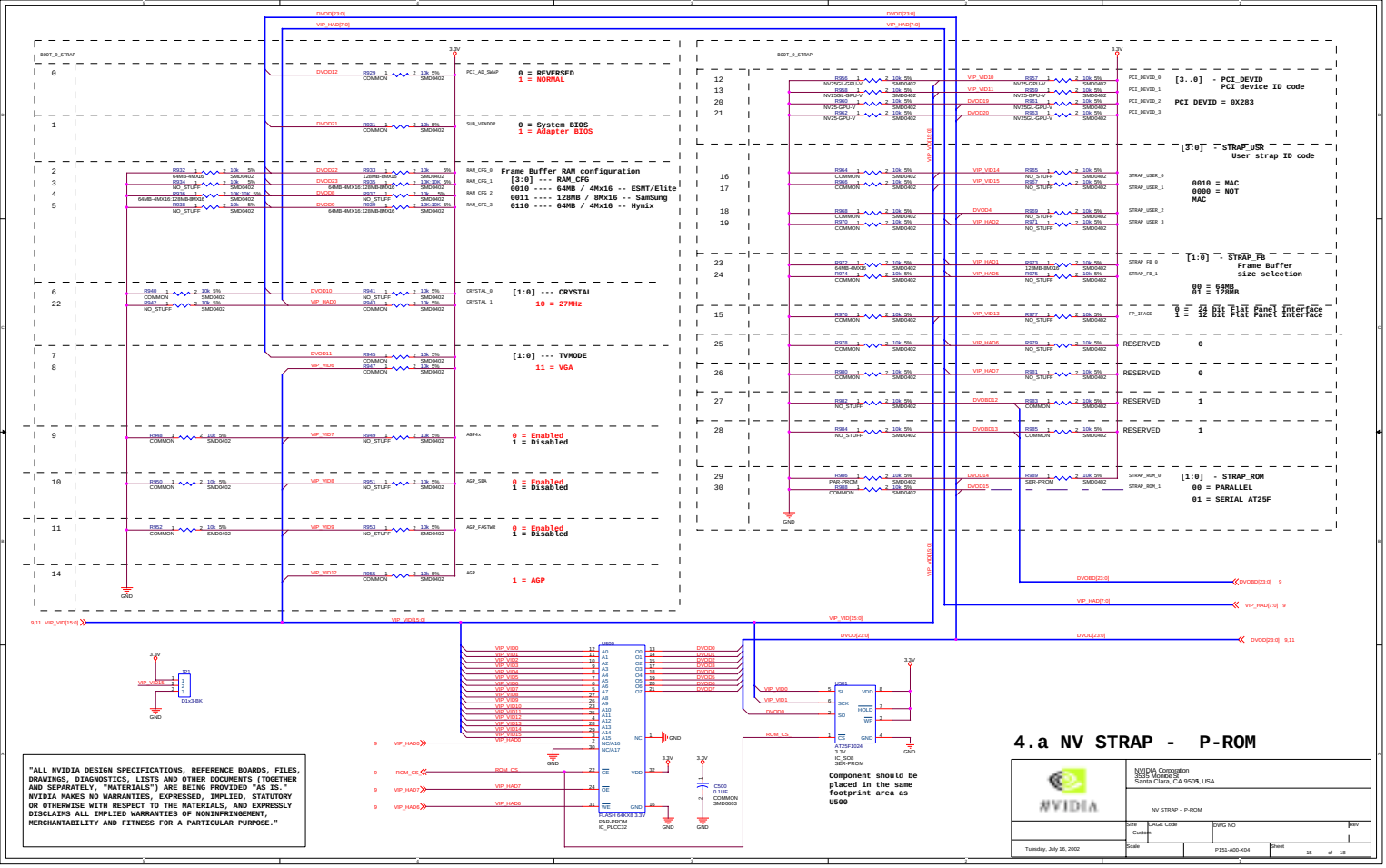
BOOT_0_STRAP
PCI_AD_SWAP
0 = REVERSED
1 = NORMAL
SUB_VENDOR
0 = System BIOS
1 = Amapter BIOS
RAM_CFG_0
RAM_CFG_1
RAM_CFG_2
RAM_CFG_3
Frame Buffer RAM configuration
[3:0] --- RAM_CFG
0010 ---- 64MB / 4Mx16 -- ESMT/Elite
0011 ---- 128MB / 8Mx16 -- SamSung
0110 ---- 64MB / 4Mx16 -- Hynix
CRYSTAL_0
CRYSTAL_1
[1:0] --- CRYSTAL
10 = 27MHz
[1:0] --- TVMODE
11 = VGA
AGPEx
0 = Enabled
1 = Disabled
AGP_SBA
0 = Enabled
1 = Disabled
AGP_FASTWR
0 = Enabled
1 = Disabled
AGP
1 = AGP
PCI_DEVID_0
PCI_DEVID_1
PCI_DEVID_2
PCI_DEVID_3
[3..0] - PCI_DEVID
PCI device ID code
PCI_DEVID = 0X283
[3:0] - sTRAP_uSR
User strap ID code
STRAP_USER_0
STRAP_USER_1
STRAP_USER_2
STRAP_USER_3
0010 = MAC
0000 = NOT
MAC
STRAP_FB_0
STRAP_FB_1
[1:0] - STRAP_FB
Frame Buffer
size selection
00 = 64MB
01 = 128MB
FP_IFACE
0 = 24 bit Flat Panel Interface
1 = 12 bit Flat Panel Interface
RESERVED
0
RESERVED
0
RESERVED
1
RESERVED
1
STRAP_ROM_0
STRAP_ROM_1
[1:0] - STRAP_ROM
00 = PARALLEL
01 = SERIAL AT25F
"ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE."
Component should be placed in the same footprint area as U500
4.a NV STRAP - P-ROM
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Santa Clara, CA 95051 USA
NV STRAP - P-ROM
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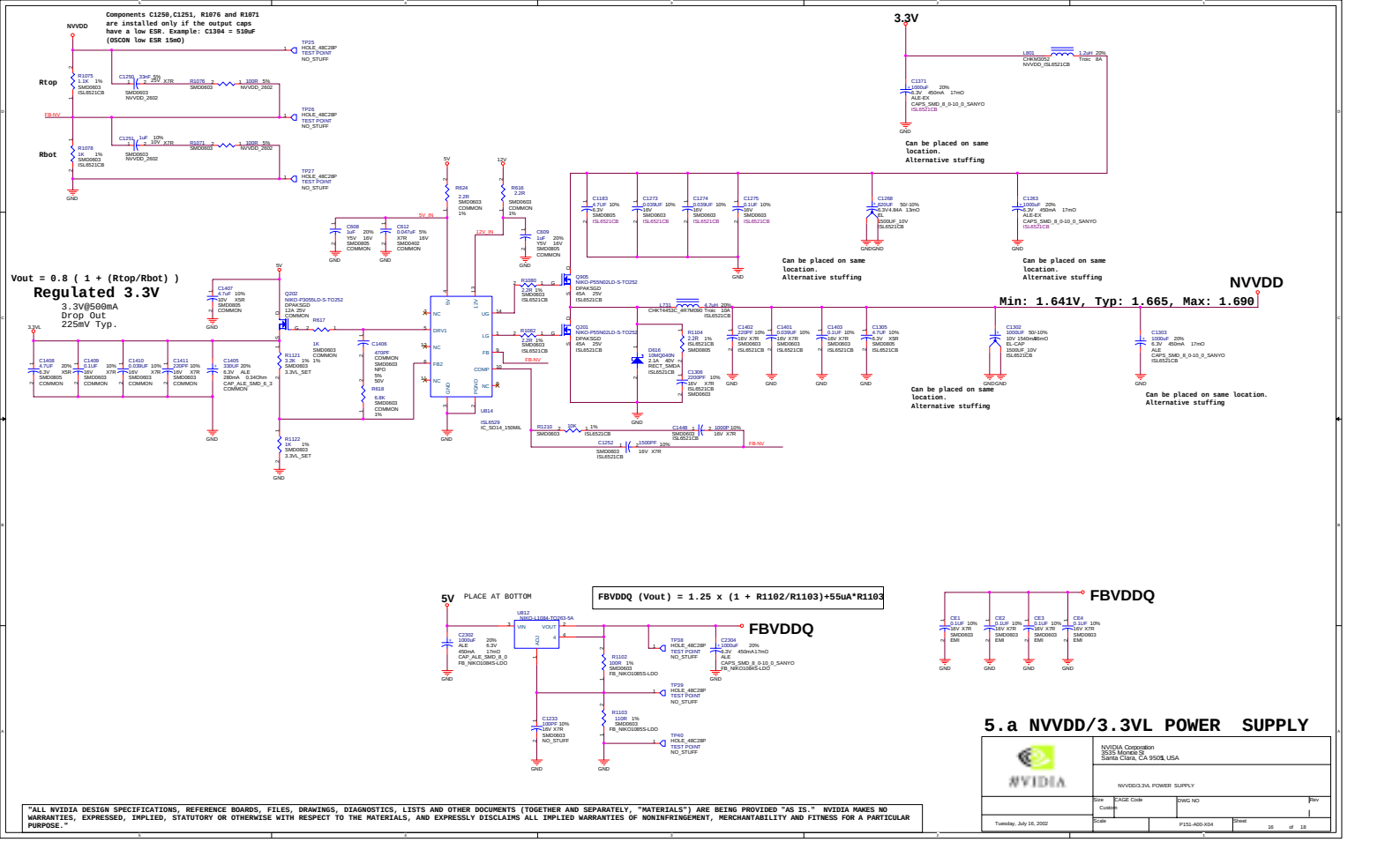

5.a NVVDD/3.3VL POWER SUPPLY

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NVVDD/3.3VL POWER SUPPLY

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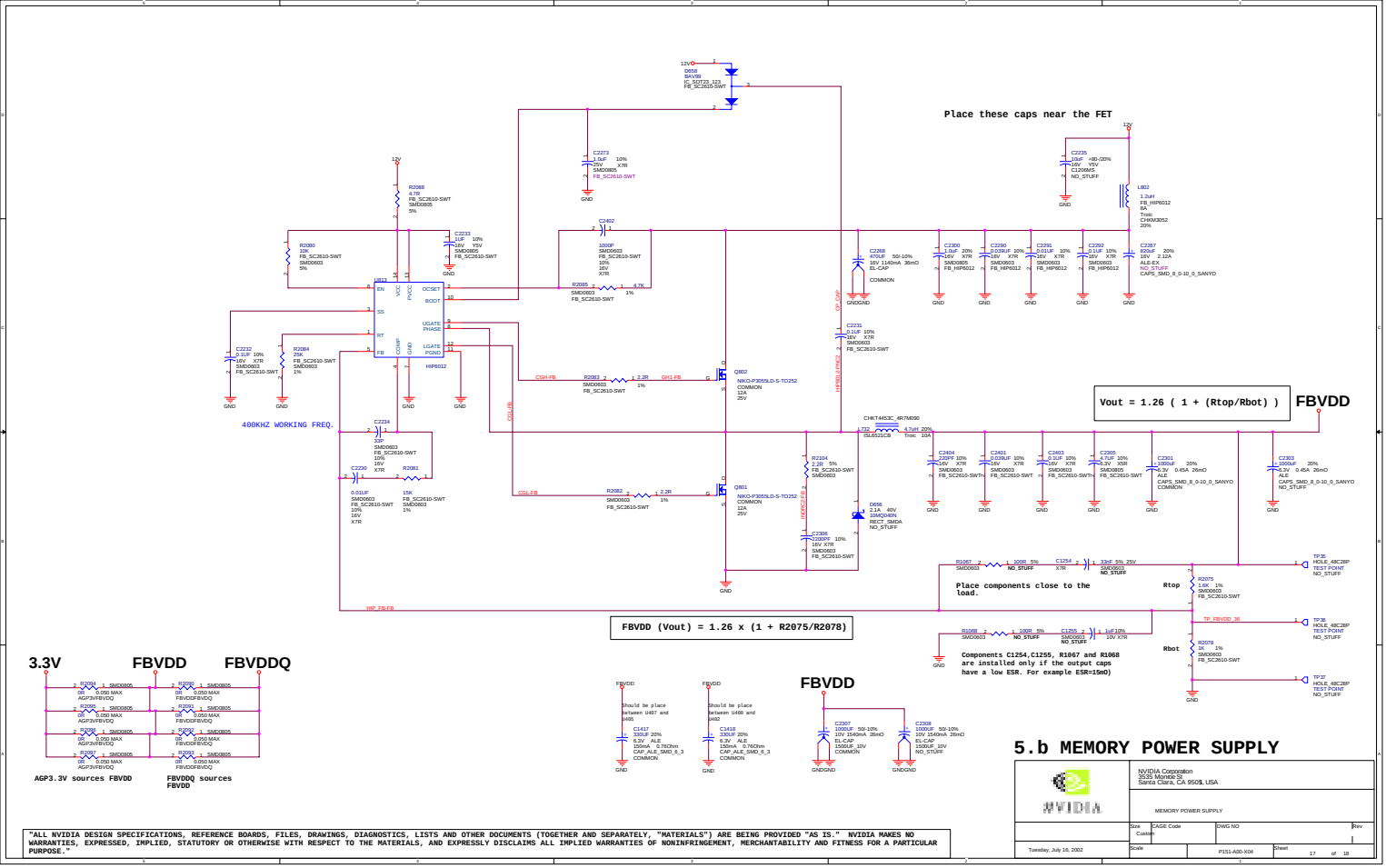

5.b MEMORY POWER SUPPLY

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MEMORY POWER SUPPLY

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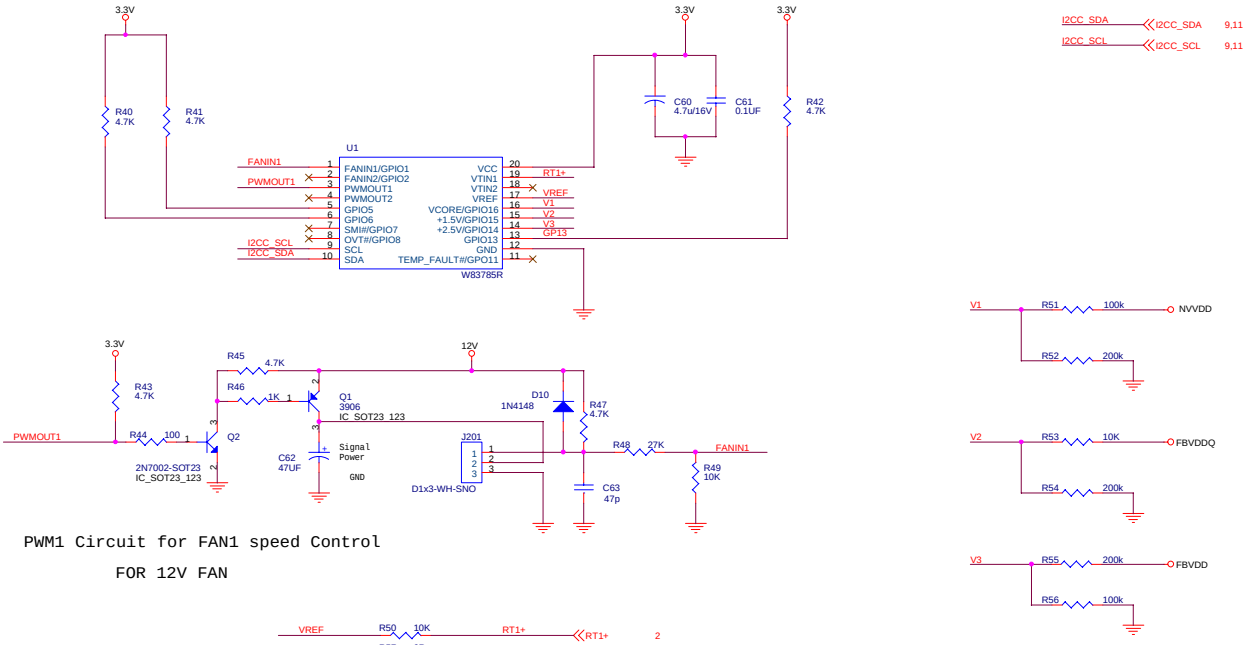

NVIDIA Corporation 3535 Monroe St Santa Clara, CA 95051, USA			
H/W MONITOR			
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