P1070-A01

GF108, 512MB 32Mx32 GDDR5
Desktop, 75W TGP, DL-DVI/VGA/HDMI

TABLE OF CONTENTS

Page	Description
01	Table of Contents
02	Block Diagram
03	PCI Express
04	Framebuffer A,B: GPU Section
05	Memory A Bank 0..31
06	Memory A Bank 32..63
07	Memory Decoupling, Net Rules
08	GPU Power and GND, NVVDD Decoupling, THERMAL/MECHANICAL
09	Display: DACA (South DVI-I)
10	Display: DACB (Middle DSUB)
11	Display: LFPAB (South DVI-I)
12	Display: LFPC (North HDMI)
13	Unused: LFPD/EF, MIOA/B
14	MISC: VBIOS, XTAL, STRAPS
15	MISC:GPIO, JTAG, INFO ROM, THERMAL LATCH, FAN CONTROL
16	Power Supply: 12V INPUT, DDC_5V, PEXVDD
17	Power Supply: FBVDDQ
18	Power Supply: NVVDD

2010/11/30 MS-V258-1.0 changed list

Page	Description
08	add a SP-CAP near GPU bottom
	add screw & HDMI fee & PCB & cross point & Fan
	changed BKT1 PCB footprint to shorter name
15	deleted 12V BOOST circuit & removed net 12V_FAN &
	12V_F contact FAN 12V input directly & add R688 &
	modified fan control circuit & Fan housing changed to 4 pin &
	delete INFO ROM circuit & I2CC link to VDD adjust circuit &
	delete JTAG circuit & delete D501
16	removed net 12V_FAN & delete LDO Option & delete Switcher Option
	changed 12V Input choke footprint & delete co-lay resistor
17	changed FBVDDQ Output choke footprint & delete co-lay choke
18	changed NVVDD Output choke footprint & delete co-lay choke
17,18	changed Q2 Q3 Q4 Q5 Q6 Q8 Q9 Q10 PCB footprint to shorter name &
	remove co-lay SMD OS-CON CAP
19	add a new page for VDD adjust circuit

2011/8/23 MS-V269-2.0 changed list

Page	Description
04	Remove FBB and add TERMINATION OPTION FOR 8 LOAD CMD LINE
05	Change to Memory 1st Bank 0..31
06	Change to Memory 1st Bank 32..63
07	Del some Memory Decoupling
08	Change THERMAL/MECHANICAL HOLES
15	Change Fan control circuit
16	Add 12V by-pass resistance & remove PEX_VDD control for 6262

2012/4/16 MS-V269-3.0 changed list

Page	Description
04~07	Copy all the memory component from V230-6.0(128M*16bit*8pcs/128bit DDR3)
15	Del 4pin Fan control circuit, Add 2pin fan control circuit

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11070-BASE-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-11070-0000-100	GF108-400, 512MB 32Mx32 GDDR5, DVI, VGA, HDMI
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Date: Friday, April 20, 2012 | Sheet 1 of 19

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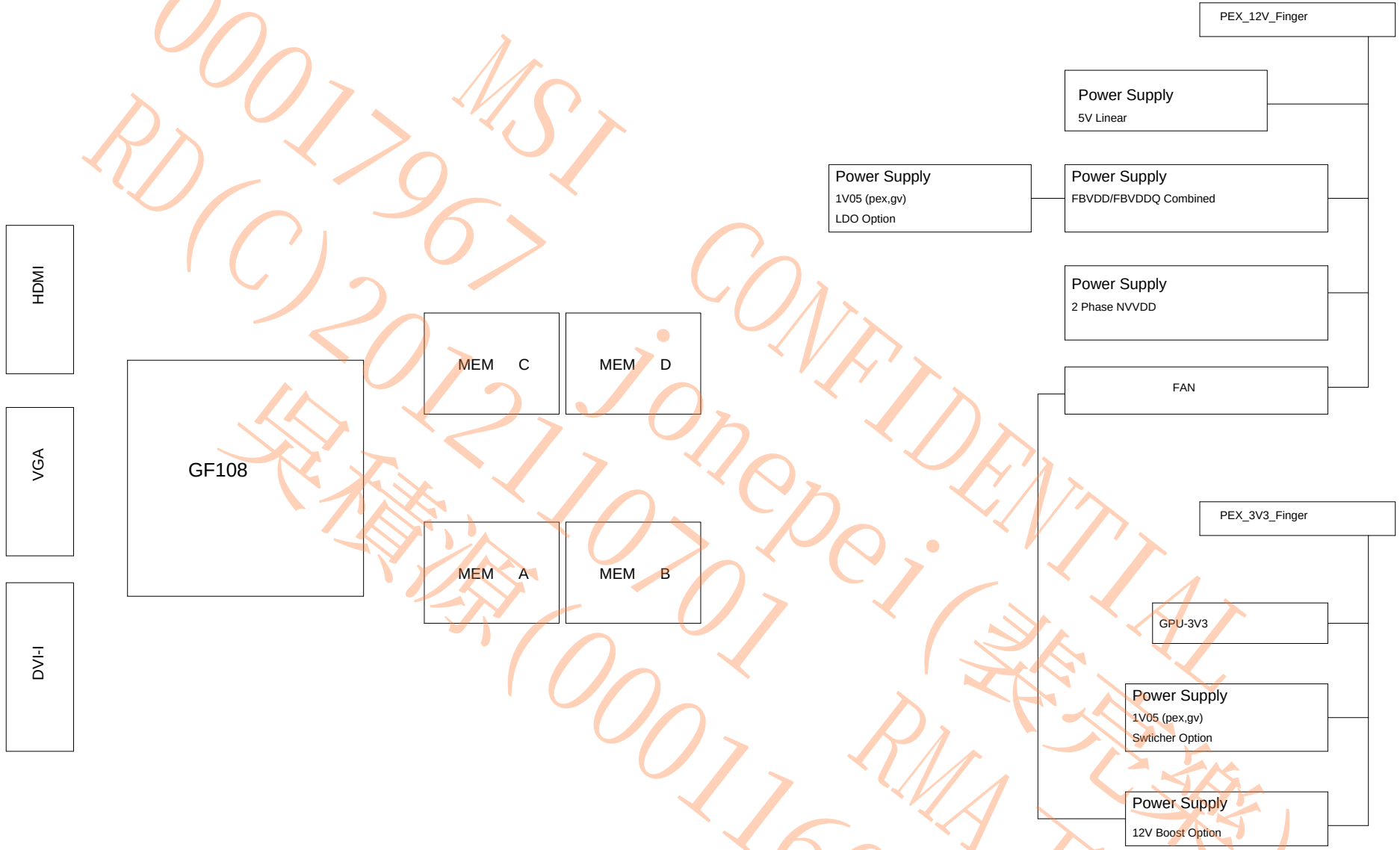
Block Diagram



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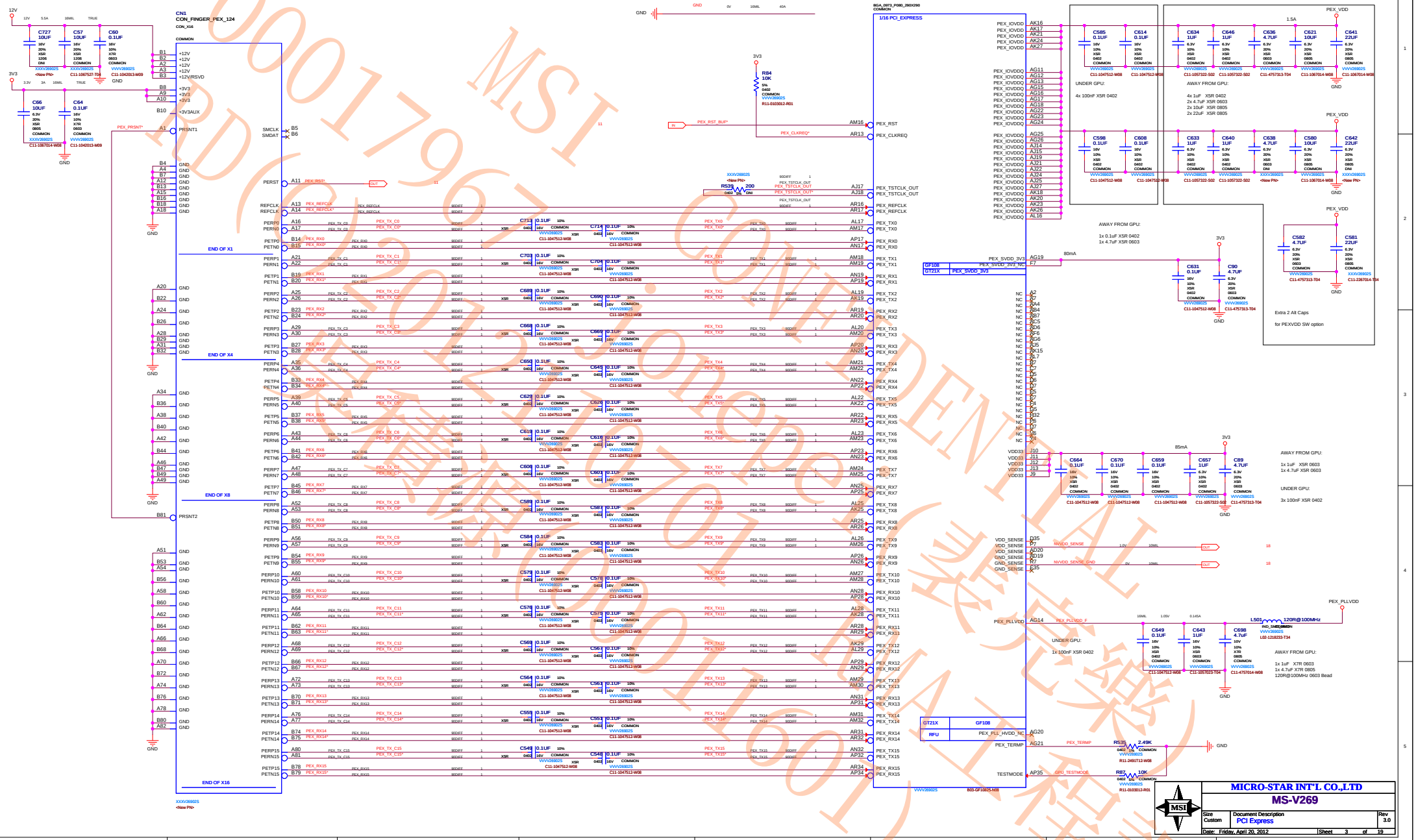
Date: Friday, April 20, 2012	Sheet 2 of 19	

PCI Express



CN1
CON_FINGER_PEX_124
G1A
1/16 PCI_EXPRESS
END OF X1
END OF X4
END OF X8
END OF X16
UNDER GPU:
4x 100nF X5R 0402
AWAY FROM GPU:
4x 1uF X5R 0402
2x 4.7uF X5R 0603
2x 10uF X5R 0805
2x 22uF X5R 0805
AWAY FROM GPU:
1x 0.1uF X5R 0402
1x 4.7uF X5R 0603
Extra 2 Alt Caps
for PEXVDD SW option
AWAY FROM GPU:
1x 1uF X5R 0603
1x 4.7uF X5R 0603
UNDER GPU:
3x 100nF X5R 0402
UNDER GPU:
1x 100nF X5R 0402
AWAY FROM GPU:
1x 1uF X7R 0603
1x 4.7uF X7R 0805
120R@100MHz 0603 Bead
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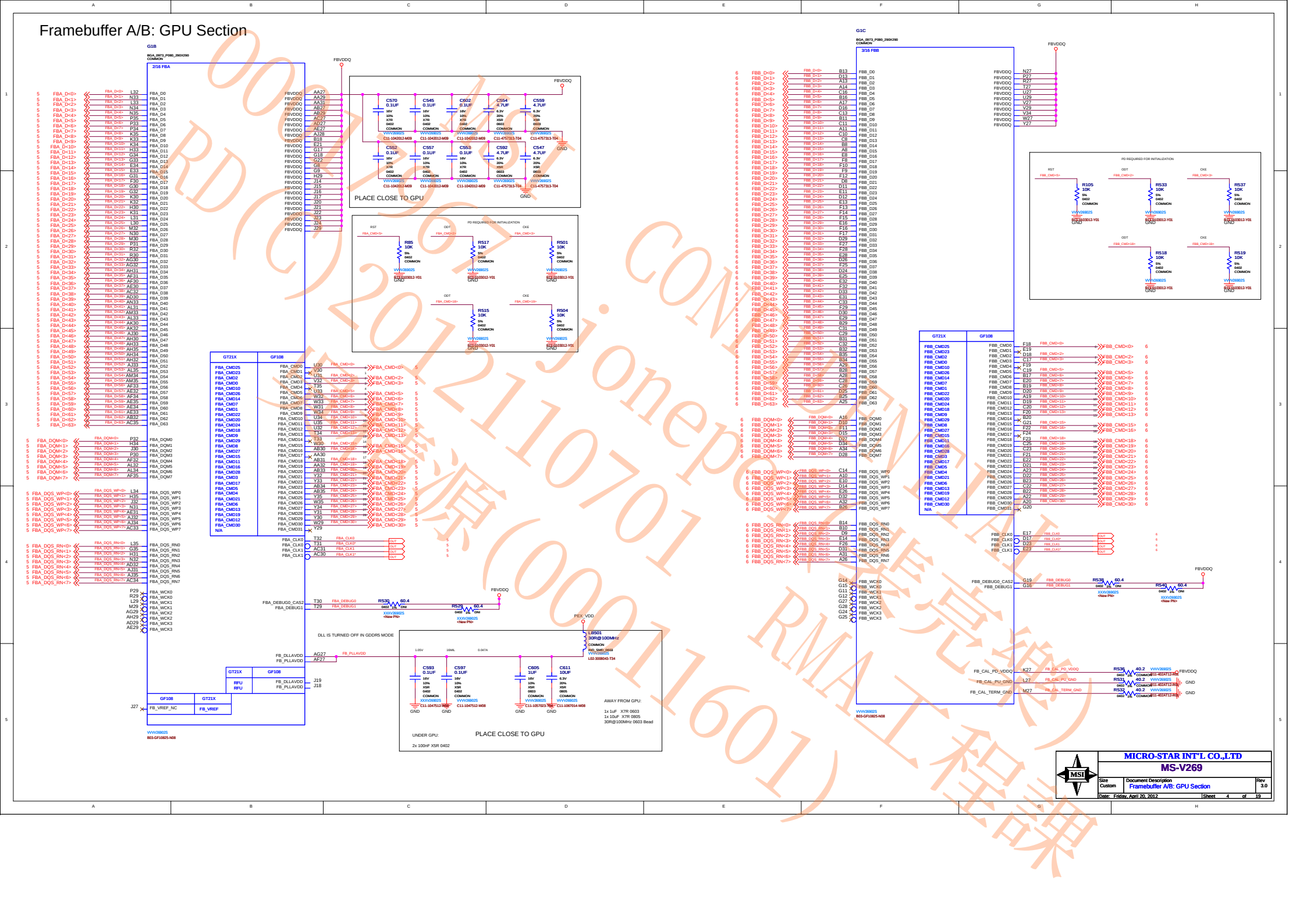
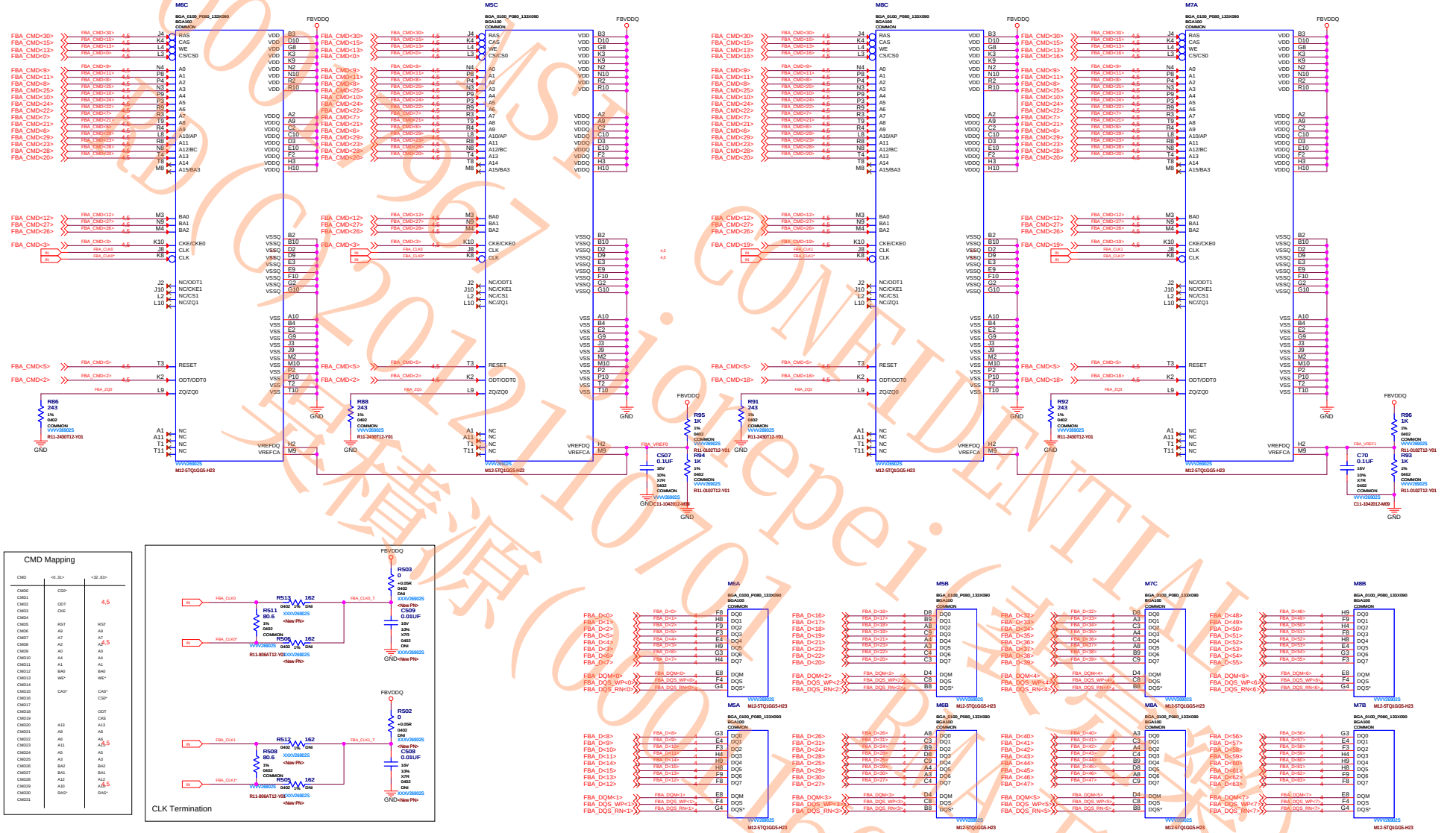
Size Custom
Document Description PCI Express
Rev 3.0
Date: Friday, April 20, 2012
Sheet 3 of 19

Framebuffer A/B: GPU Section



FBA Partition



CMD Mapping

CMD	<0..31>	<32..63>
CMD0	CS0*	
CMD1		
CMD2	ODT	4,5
CMD3	CKE	
CMD4		
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2 4,5
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14		
CMD15	CAS*	CAS*
CMD16		CS0*
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11 4,5
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10 4,5
CMD30	RAS*	RAS*
CMD31		

CLK Termination

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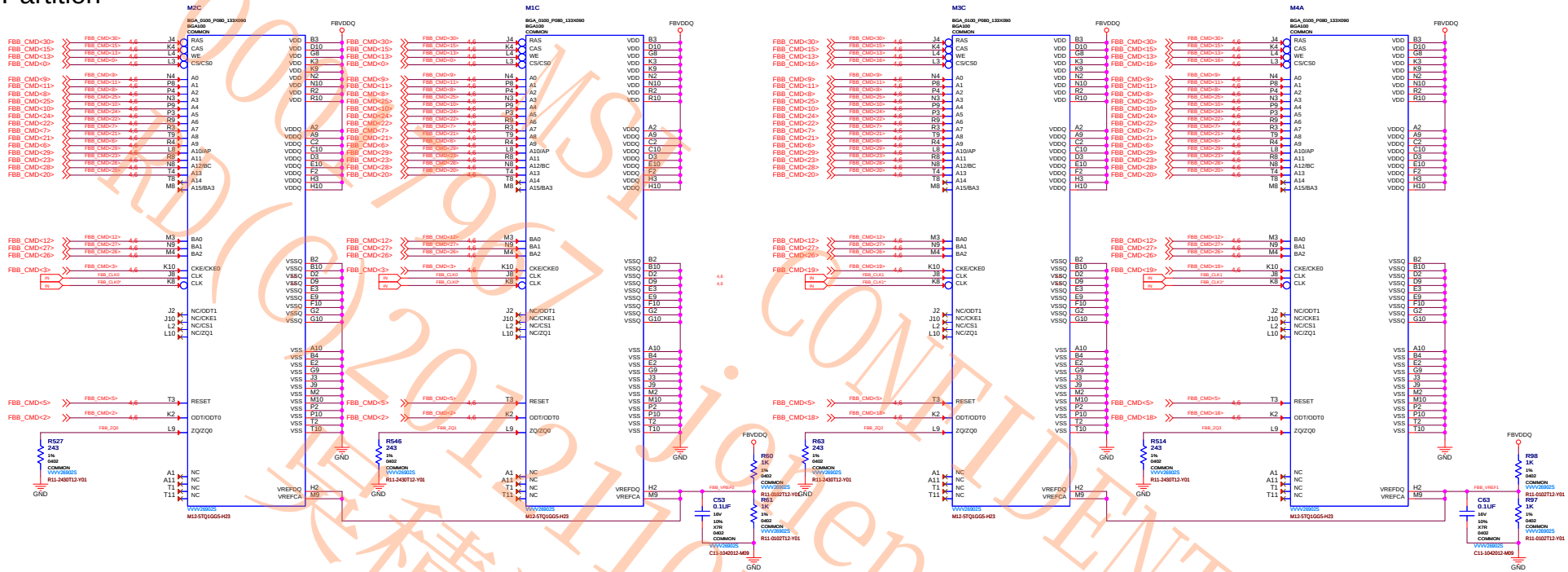
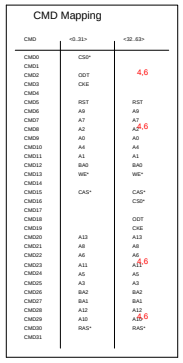
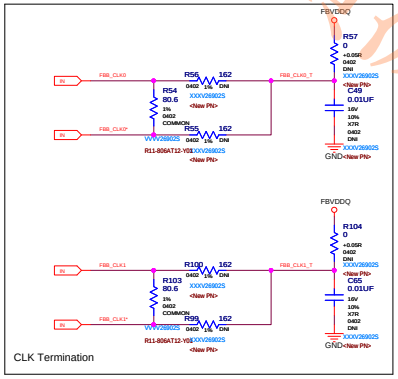
Size	Document Description	Rev
Custom	FBA	3.0

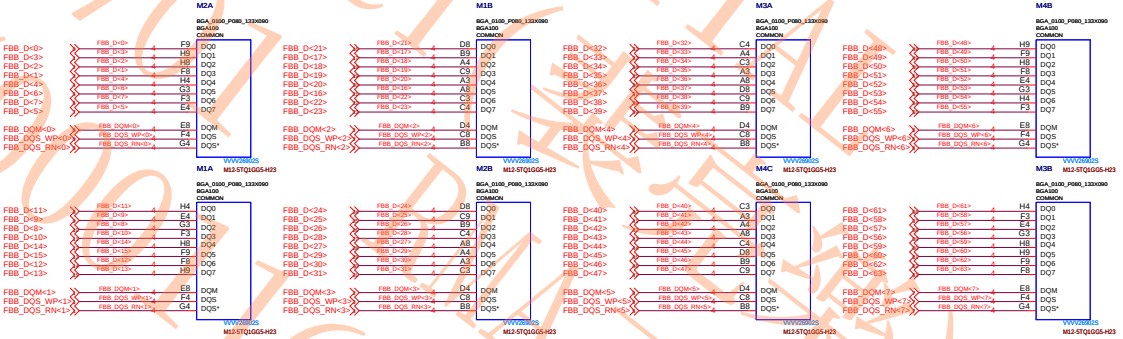
Date: Friday, April 20, 2012 Sheet 5 of 19

FBB Partition









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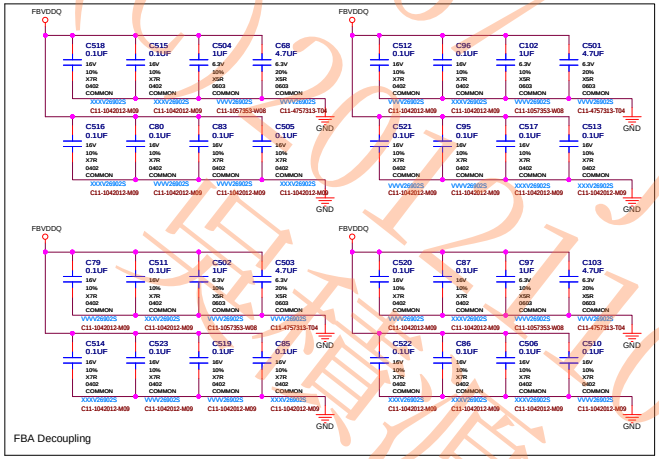
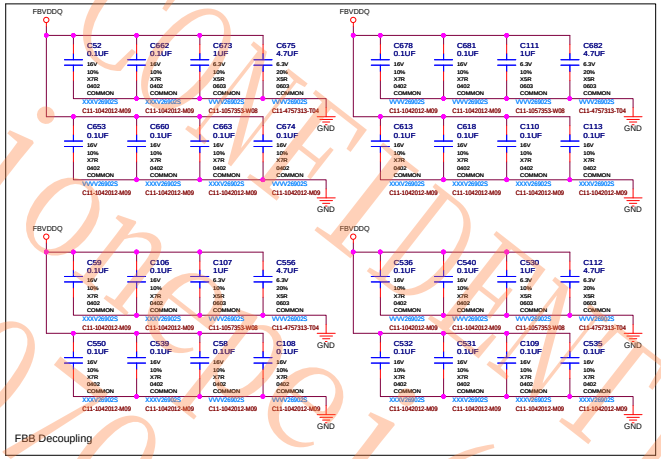
Rev: 3.0	
Date: Friday, April 20, 2012	Sheet 6 of 19

Memory Decoupling





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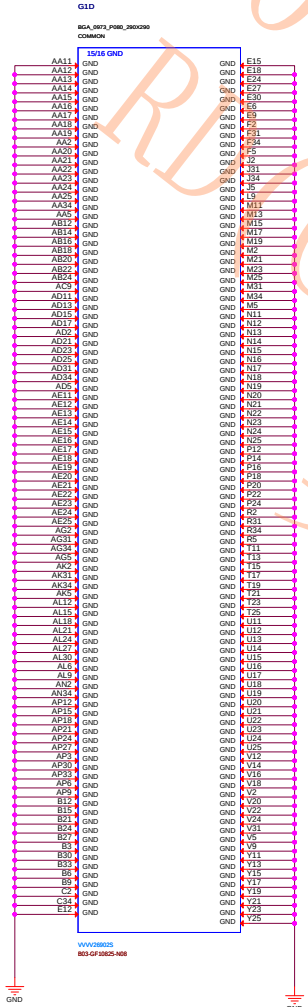
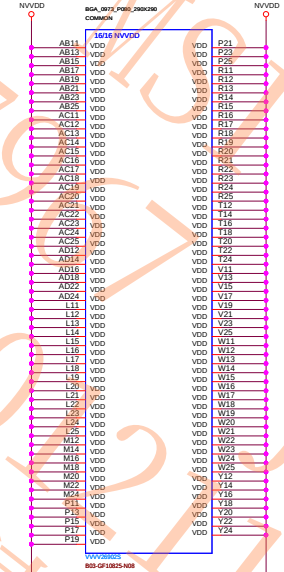
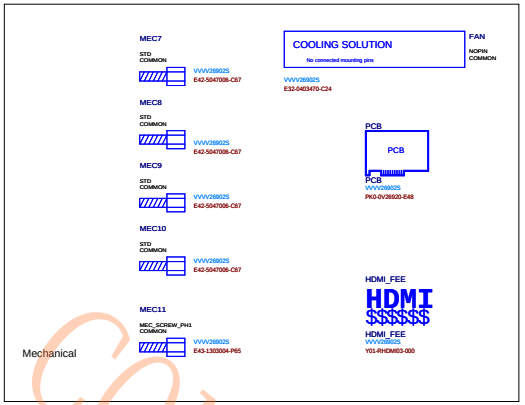
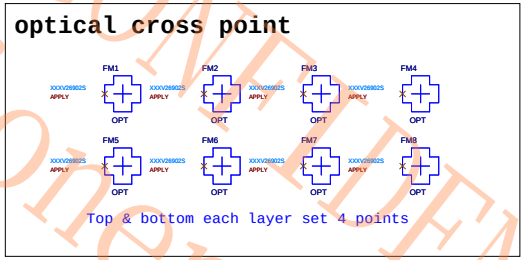
Date: Friday, April 20, 2012	Sheet 7 of 19	

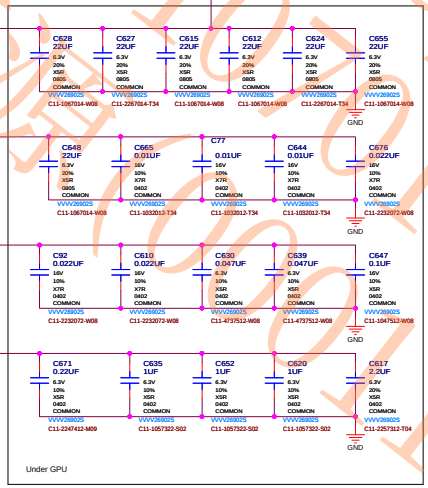
GPU Power and GND, NVVDD Decoupling, THERMAL/MECHANICAL

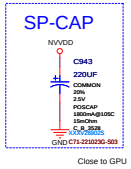


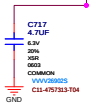












GF108 NVVDD Decoupling

UNDER GPU:

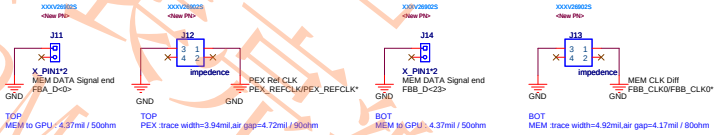
4x 0402 x7R 10nF
4x 0402 x7R 22nF
2x 0402 x7R 47nF
2x 0402 x5R 100nF
1x 0402 x5R 220nF
3x 0402 x5R 1UF
1x 0402 x5R 2.2UF

AWAY FROM GPU:

1x 0603 x5R 4.7UF

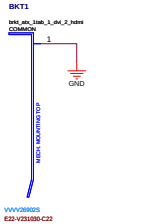
AFTER VRM:

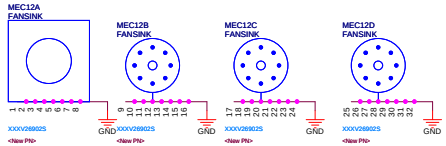
10x 0805 x5R 10UF



Bracket and Assembly

No more Screw symbol in schematic!





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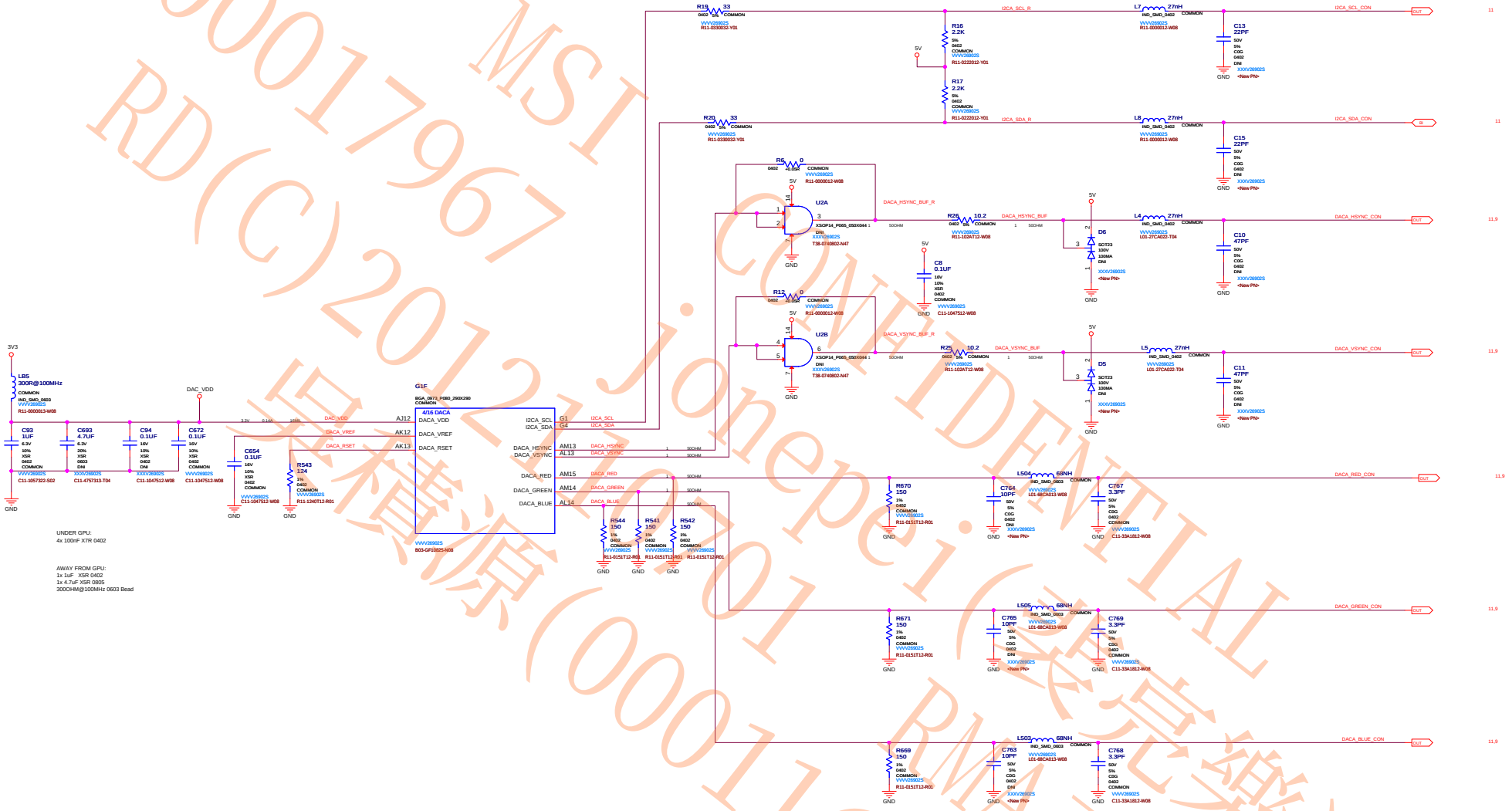
Date: Friday, April 20, 2012	Sheet 8 of 19	

0001791 Rev1.0 2012/04/20 RD(C)2012 CONFIDENTIAL 完稿版(禁止外流) RMA工程用

Display: DACA (South DVI-I)



NET		NV_CRITICAL	NV_IMPEDANCE
DACA_HSYNC_CON	11.9	1	50OHM
DACA_VSYNC_CON	11.9	1	50OHM
DACA_RED_CON	11.9	1	50OHM
DACA_GREEN_CON	11.9	1	50OHM
DACA_BLUE_CON	11.9	1	50OHM

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Size	Document Description	Rev
Custom	Display: DACA (South DVI-I)	3.0

Date: Friday, April 20, 2012 Sheet 9 of 19

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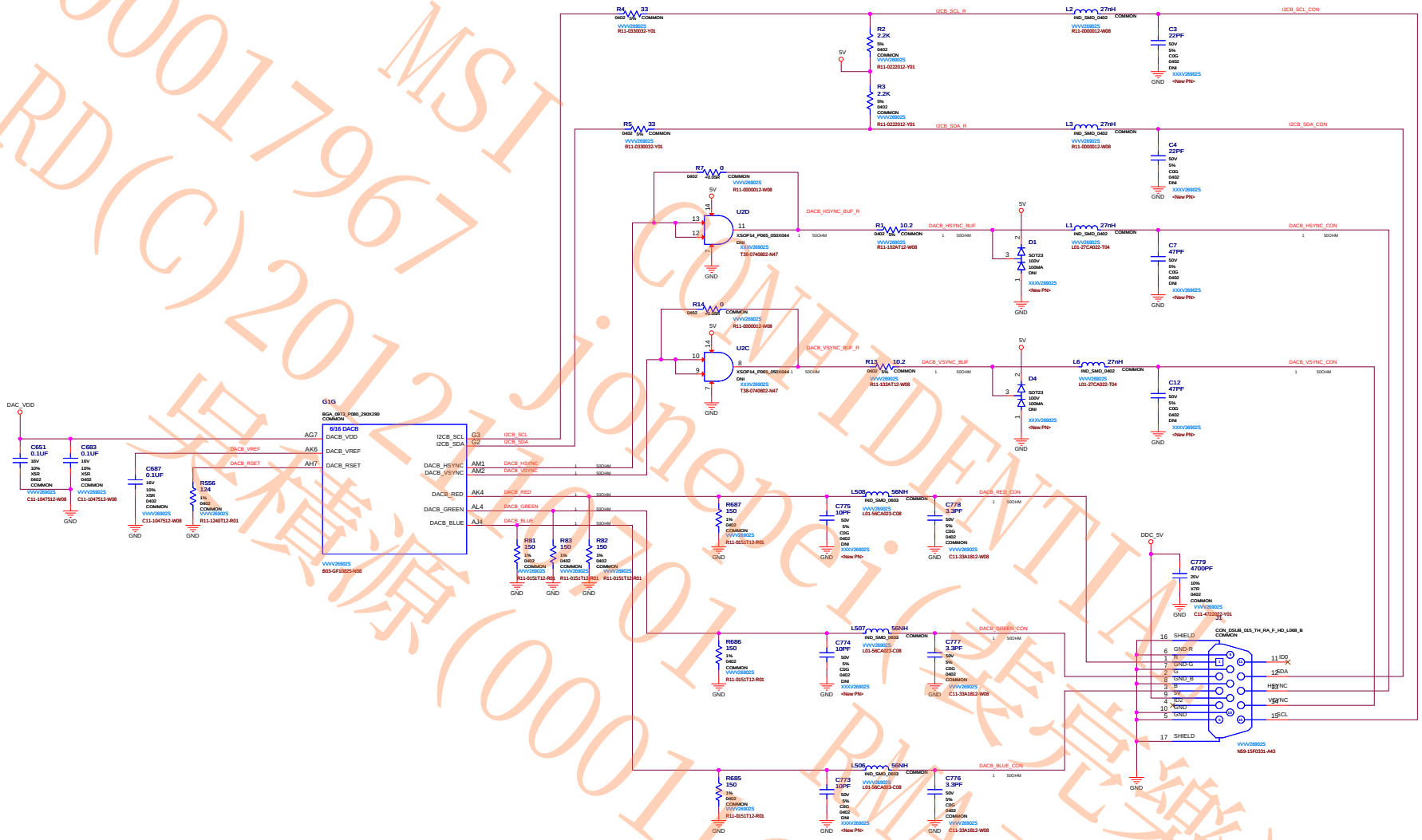
Display: DACB (Middle DSUB)



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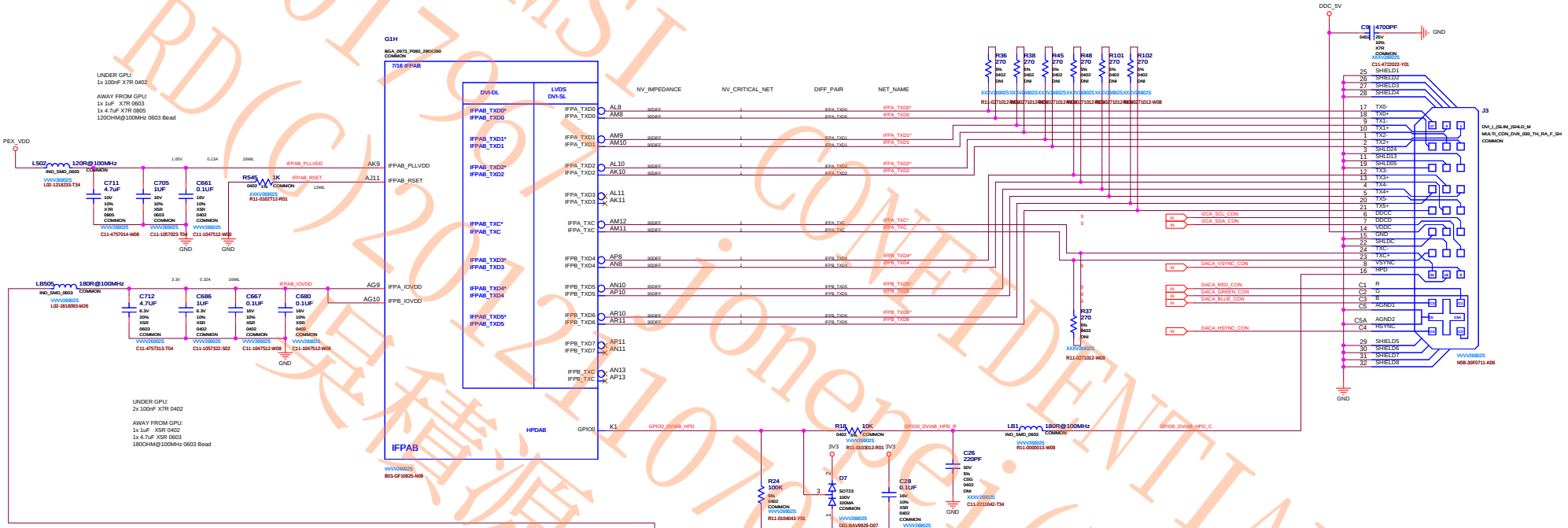
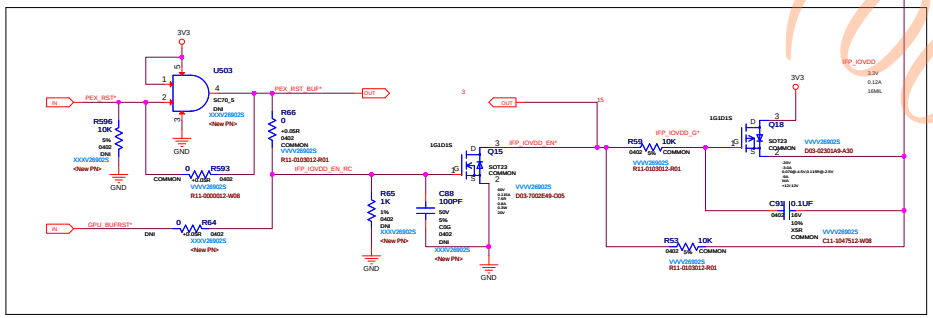
Date: Friday, April 20, 2012	Sheet 10 of 19	

Display: LFPAB (South DVI-I)



IFP_IOVDD BACKDRIVE PREVENTION



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Date: Friday, April 20, 2012	Sheet 11 of 19	

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00017957

Display: LFPC (North HDMI)

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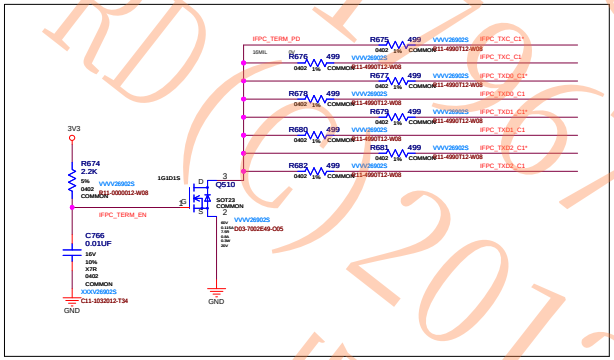
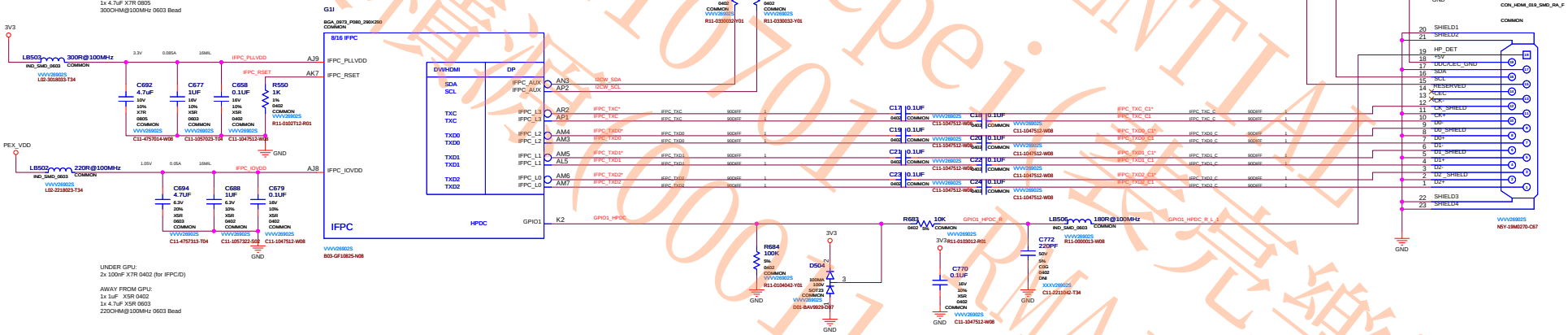
RDC(2012110701)
(2012110701)

HDMI PULL DOWNS





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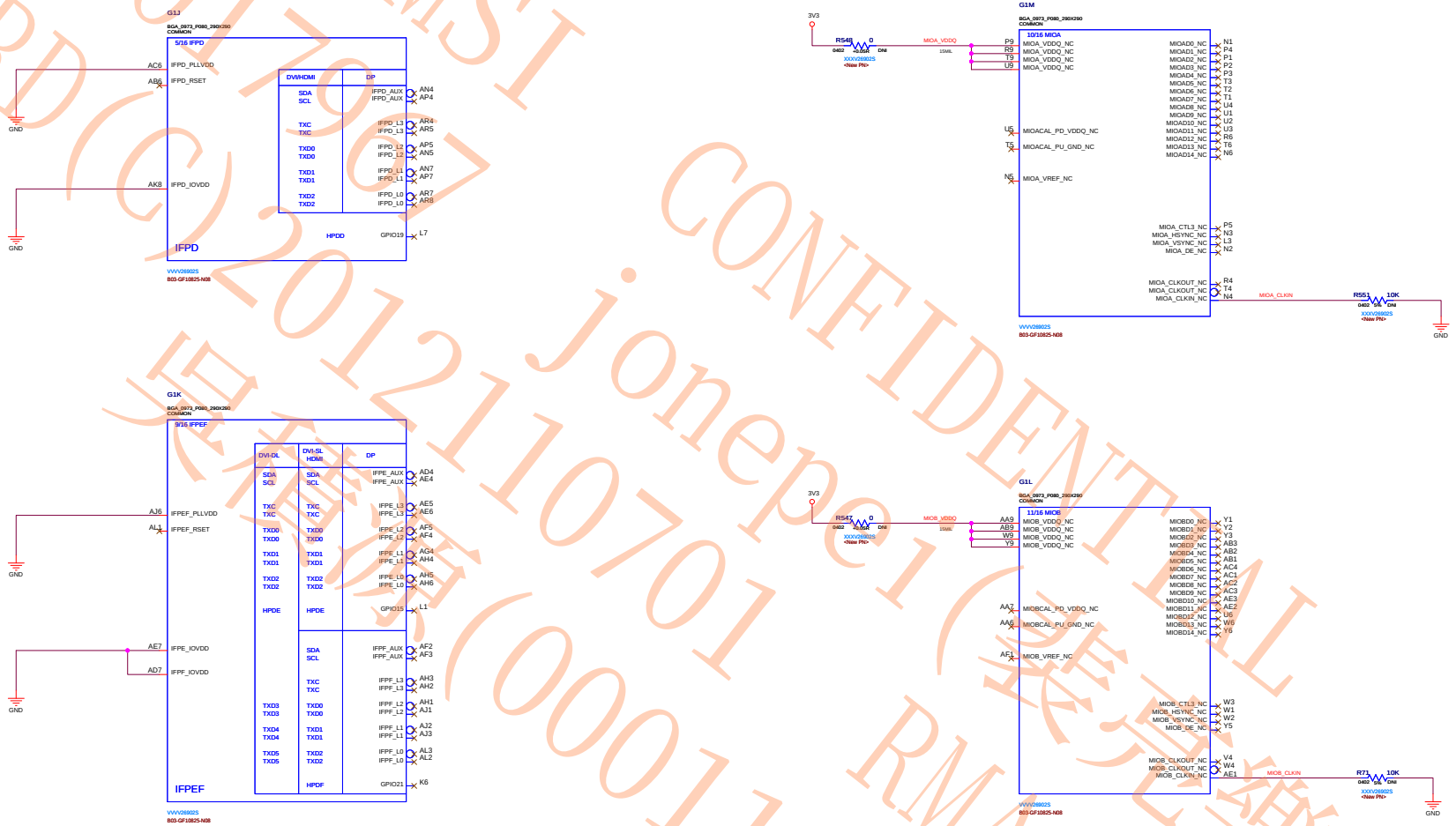
Date: Friday, April 20, 2012	Sheet 12 of 19	

Unused: LFPD/EF, MIOA/B



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Date: Friday, April 20, 2012	Sheet 13 of 19	

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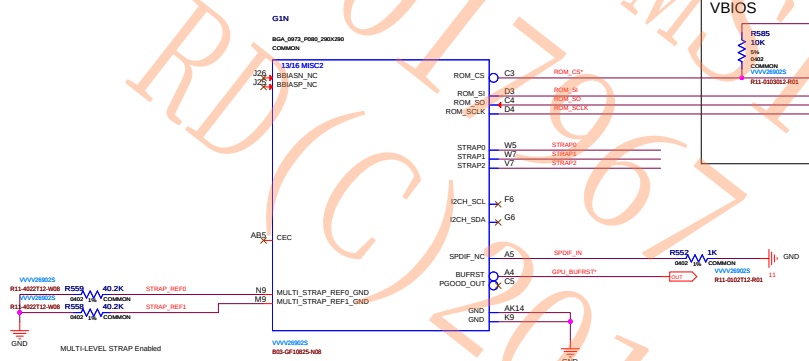
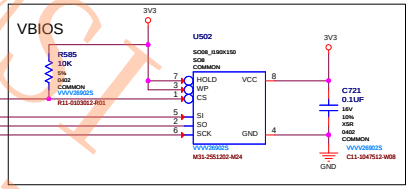
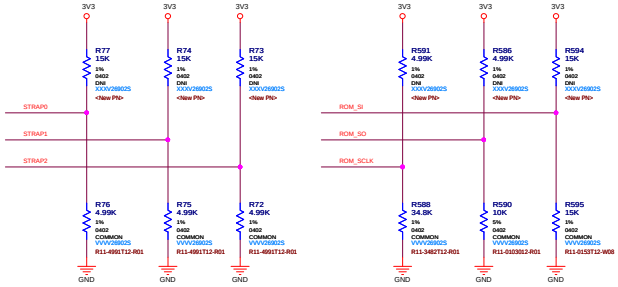
宣稿資(00011601)

MISC: VBIOS, XTAL, STRAPS

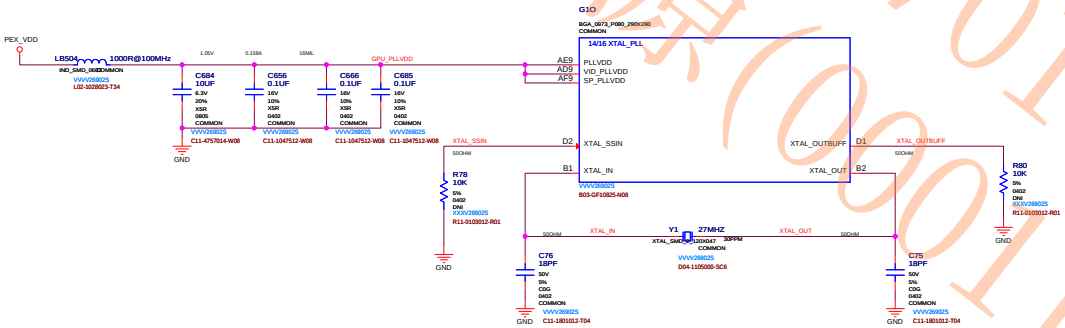






	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

ROM_SI	RAMCFG[3]	0001 32Mx32 128-bit Qimonda	
		0010 32Mx32 128-bit Hynix	=> 15K PD
	RAMCFG[2]	0011 32Mx32 128-bit Samsung	=> 20K PD
	RAMCFG[1]	0101 64Mx32 128-bit Qimonda	
		0110 64Mx32 128-bit Hynix	
	RAMCFG[0]	0111 64Mx32 128-bit Samsung	
ROM_SO	XCLK_417	0 277MHz (Default)	
	FB[0]_BAR_SIZE	0 256MB (Default)	10K PD
	SMB_ALT_ADDR	0 0x9E (Default)	
	VGA_DEVICE	1 VGA Device (Default)	
ROM_SCLK	PCI_DEVID_EXT	0 DID<4>=0	
	SUB_VENDOR	1 BIOS ROM Present	45K PD
	SLOT_CLK_CFG	1 Share Ref CLK	
	PEX_PLL_EN_TERM100	1 Enable	
STRAP0	USER_BIT [3..0]	0000 Default	5K PD
STRAP1	3GIO_PADCFG_LUT_ADR [3..0]	0000 Desktop	5K PD
STRAP2	PCI_DEVID [3:0]	0000 DID: 0x0DE0	5K PD



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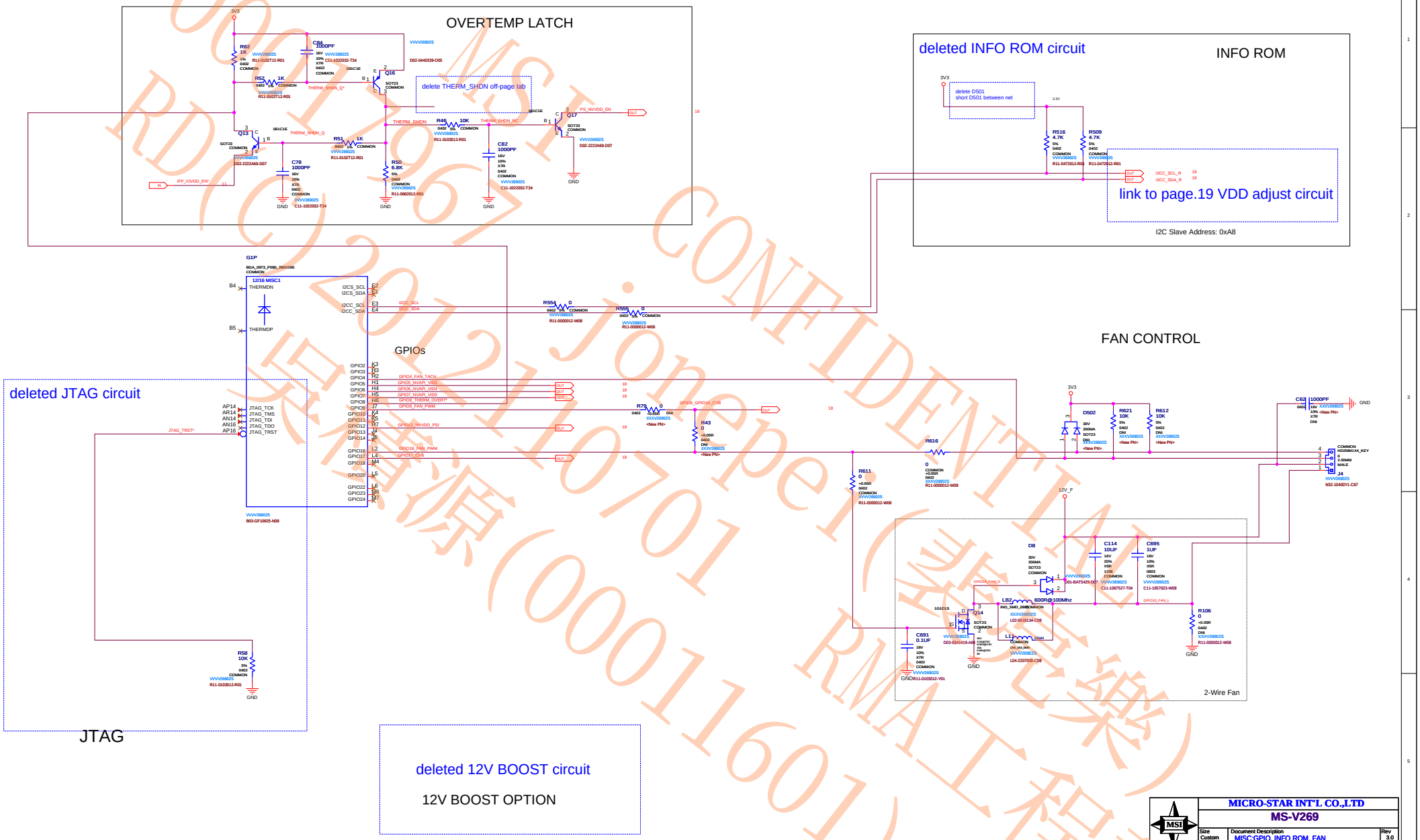
Rev: 3.0	
Date: Friday, April 20, 2012	Sheet 14 of 19

MISC:GPIO, JTAG, INFO ROM, THERMAL LATCH, FAN CONTROL



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Size: Custom	Document Description: MISC:GPIO, INFO ROM, FAN	Rev: 3.0
Date: Friday, April 20, 2012	Sheet 15 of 19	

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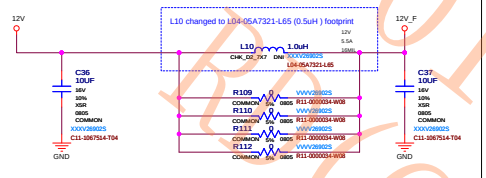
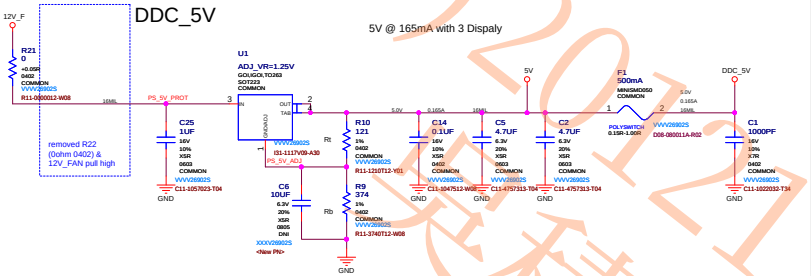
(00011601)

Power Supply: 12V INPUT, DDC_5V, PEXVDD

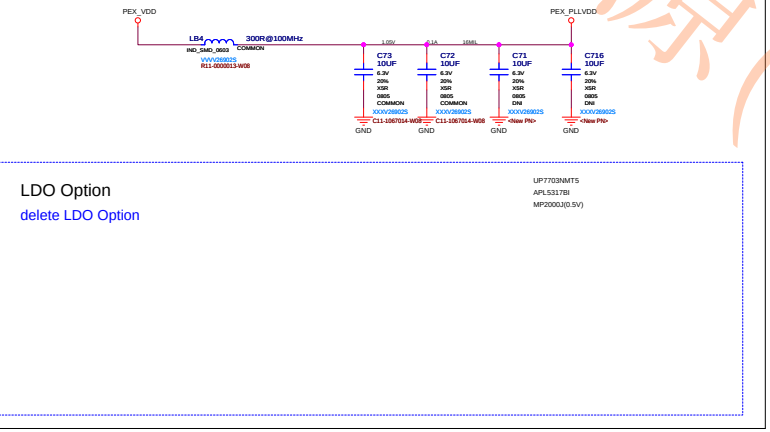
PEX_12V INPUT - 66W



DDC_5V



PEX_PLLVDD

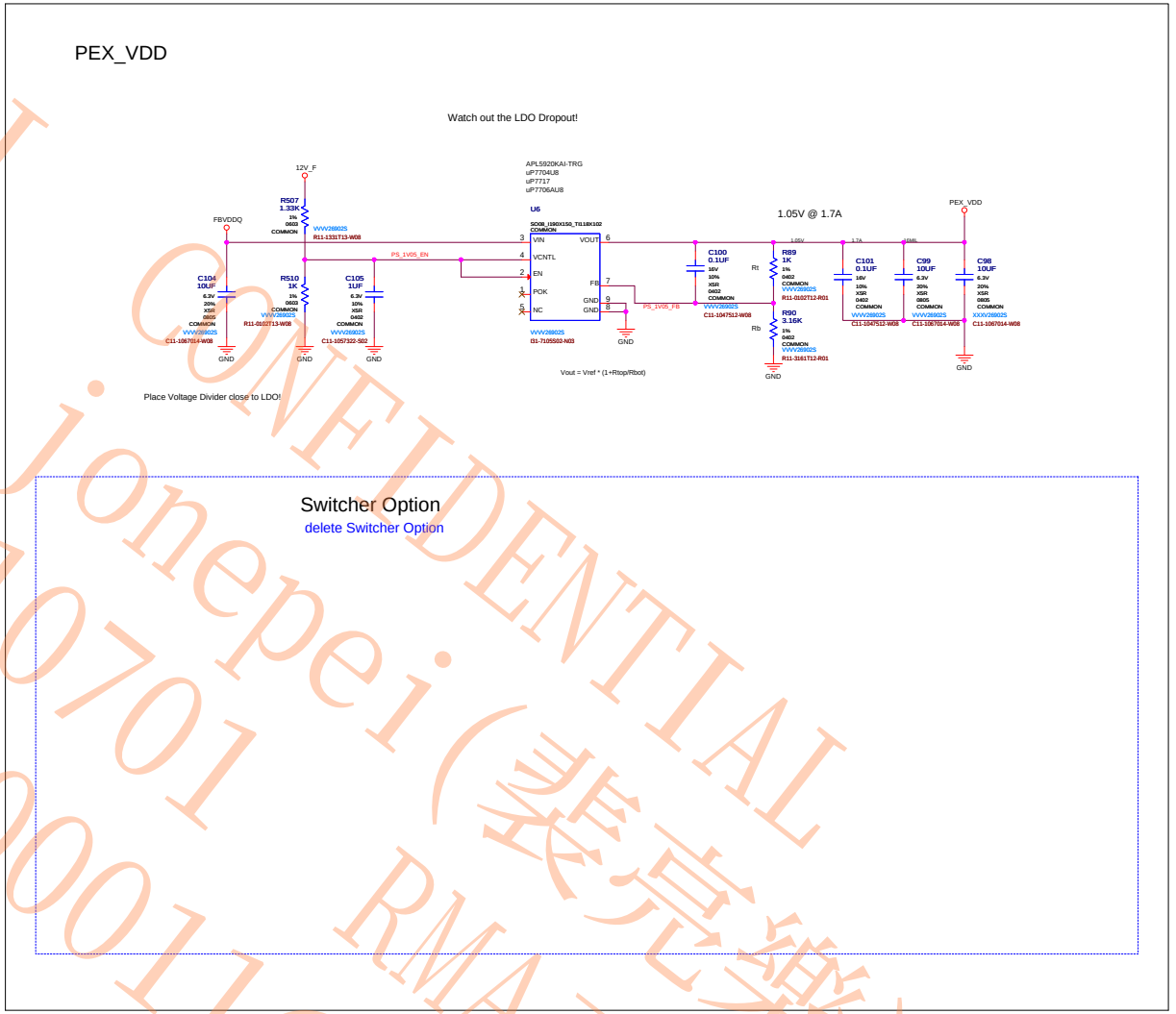


LDO Option

delete LDO Option

UP7703NMT5
APL5317BI
MP2000J(0.5V)

PEX_VDD



Switcher Option

delete Switcher Option

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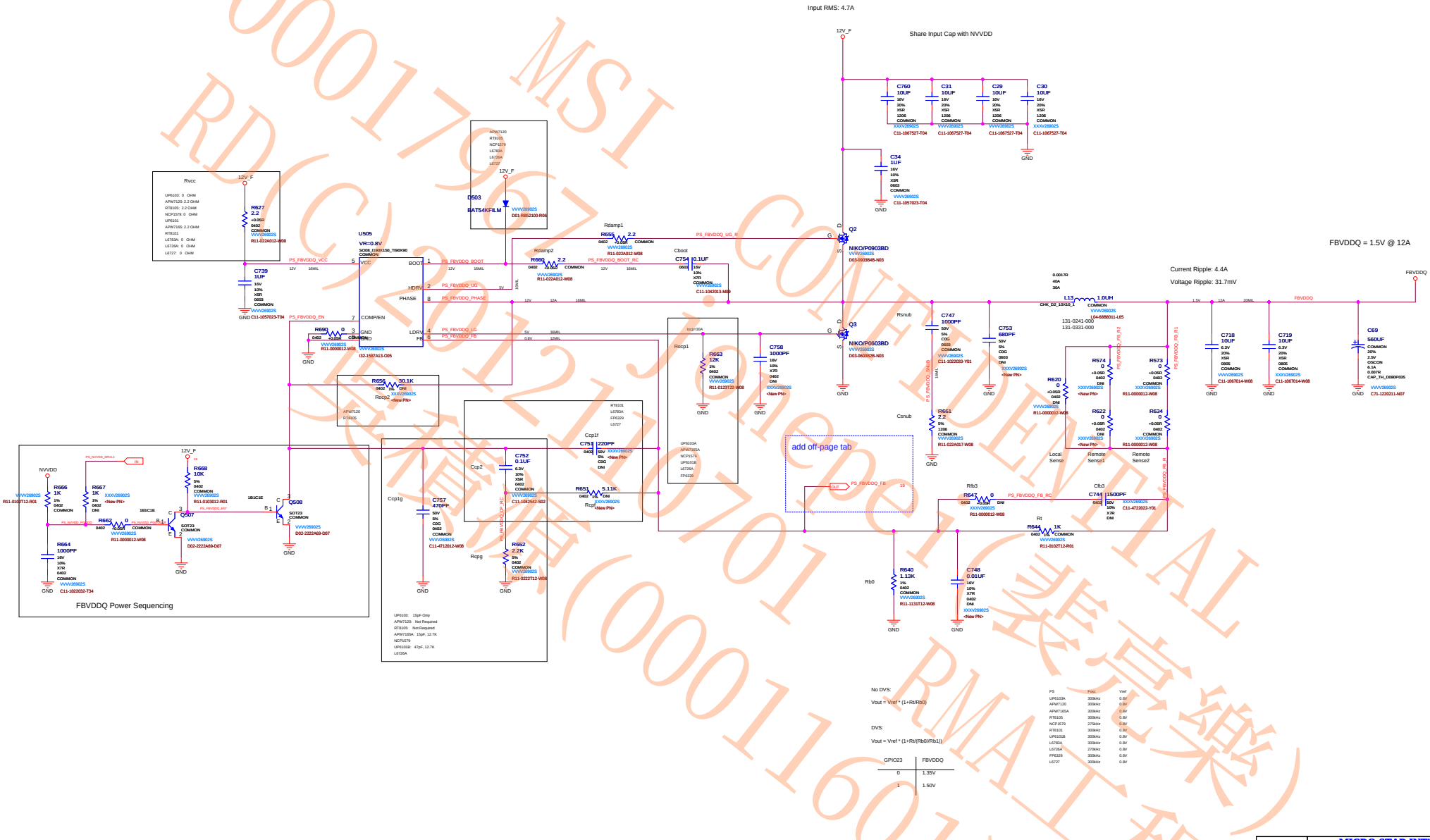
Size: Custom	Document Description: Power Supply: 12V INPUT, DDC	Rev: 3.0
Date: Friday, April 20, 2012	Sheet 16 of 19	

Power Supply: FBVDDQ



No DVS:

Vout = Vref * (1+Rt/Rb0)

DVS:

Vout = Vref * (1+Rt/(Rb0//Rb1))

GPIO23	FBVDDQ
0	1.35V
1	1.50V

PS	Fosc	Vref
UP6103A	300kHz	0.6V
APW7120	300kHz	0.8V
APW7165A	300kHz	0.8V
RT8105	300kHz	0.8V
NCP1579	275kHz	0.8V
RT8101	300kHz	0.8V
UP6101B	300kHz	0.8V
L6783A	300kHz	0.8V
L6726A	270kHz	0.8V
FP6329	300kHz	0.6V
L6727	300kHz	0.8V

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Size: Custom	Document Description: Power Supply: FBVDDQ	Rev: 3.0
Date: Friday, April 20, 2012	Sheet 17 of 19	

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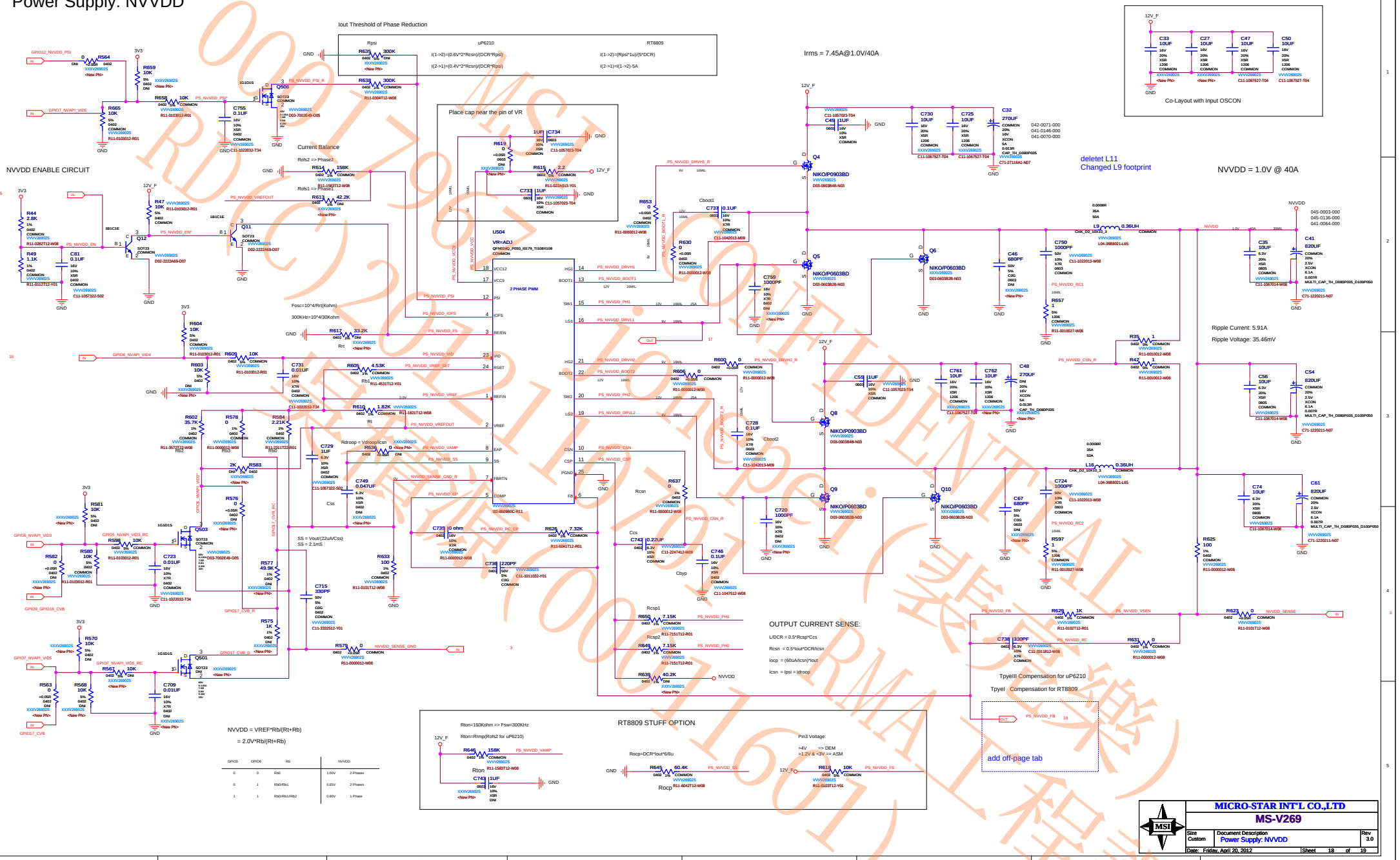
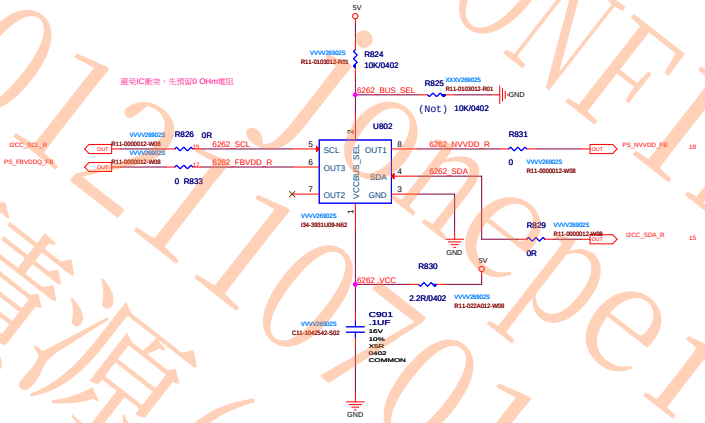
RMA工程課
(00011601)

Power Supply: NVVDD



VDD adjust circuit



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Size: Custom	Document Description: VDD adjust circuit
Rev: 3.0	
Date: Friday, April 20, 2012	Sheet 19 of 19

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