PG190-A02

GA104/GA106 GB5256
DP + DP + DP + HDMI/DP

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Page2: Block Diagram

DP

DP

DP

HDMI

DP

CO-LAYOUT

POWER SUPPLY

MEM D LO

MEM D HI

GA10X GPU
GB5-256

MEM C LO

MEM C HI

MEM B LO

MEM B HI

MEM A HI

MEM A LO

Power Supply:

NVVDD-PH8

NVVDD-PH7

NVVDD-PH6

NVVDD-PH5

NVVDD-PH4

NVVDD-PH3

NVVDD-PH2

NVVDD-PH1

FBVDDQ-PH2

FBVDDQ-PH1

5V

PEX_VDD

1V8

Fan

DP_PWR_CD/EF

EXT_12V 8PIN PWR

PEX_12V Finger

PEX_3V3 FINGER

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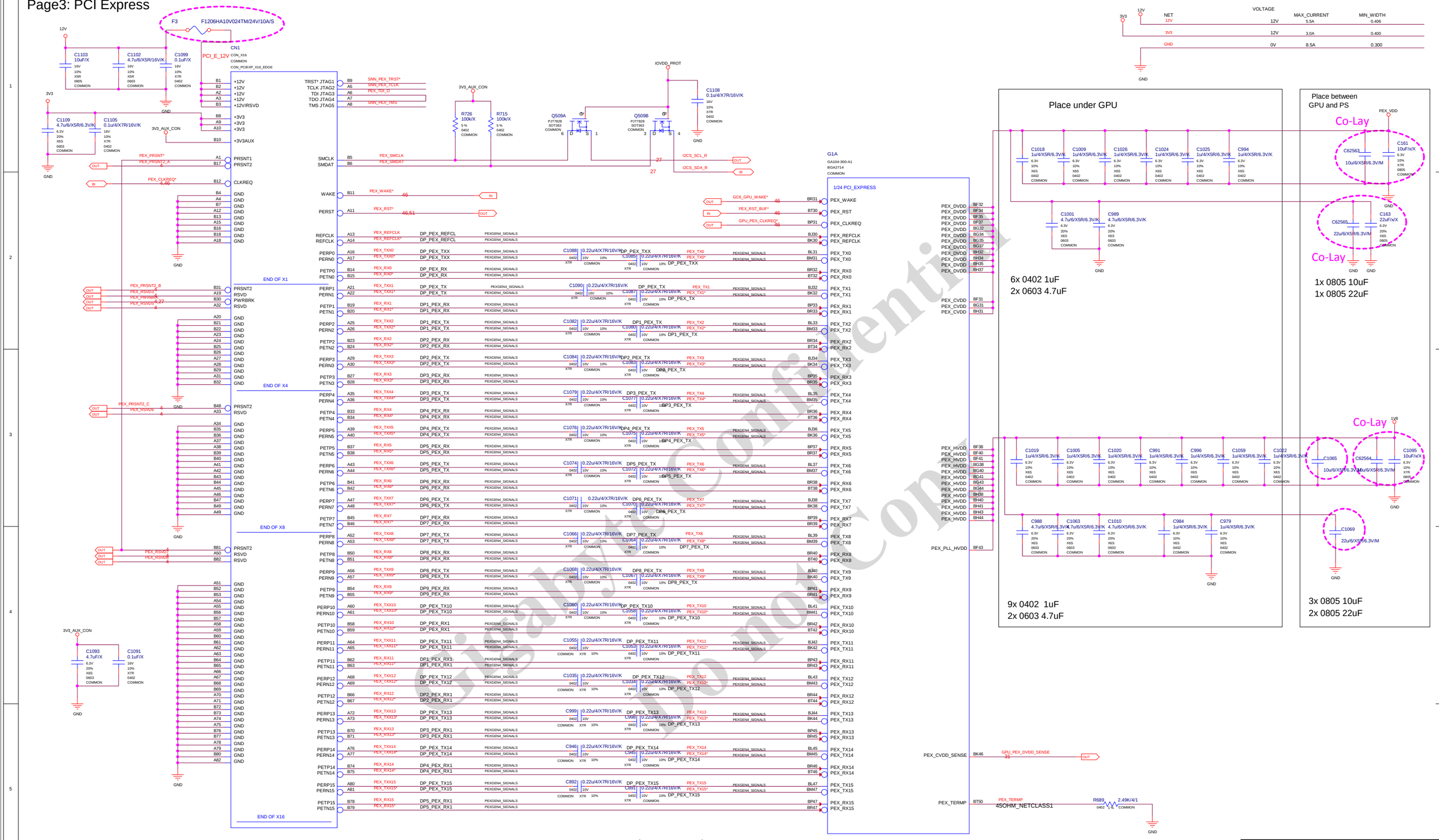
Page3: PCI Express



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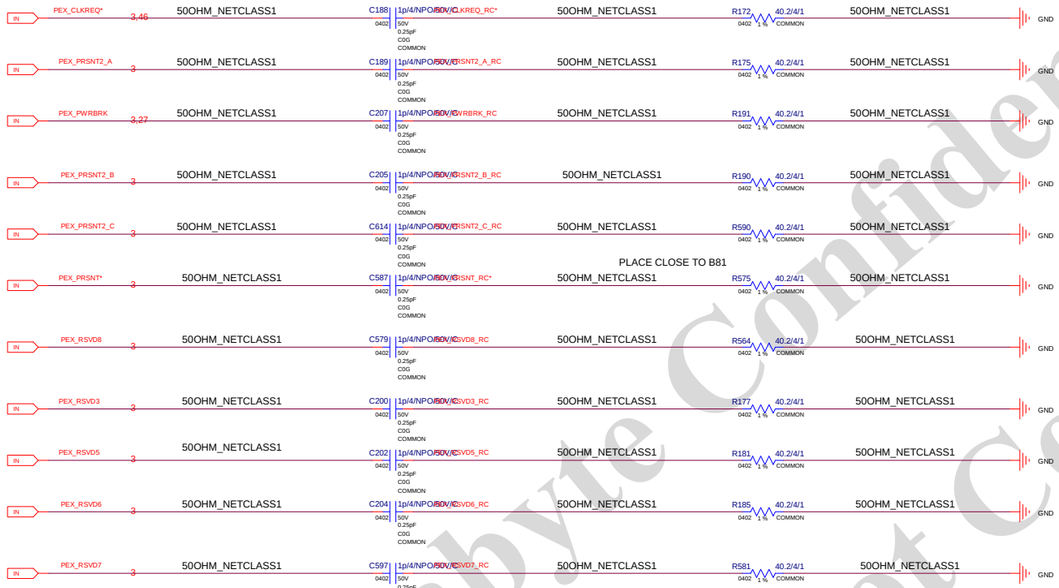

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//syseng/Projects/GA1xx/GA1XX_CMD-Mapping.xlsx

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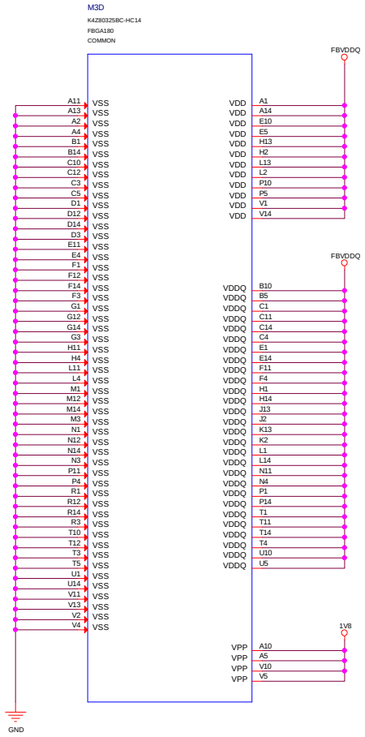
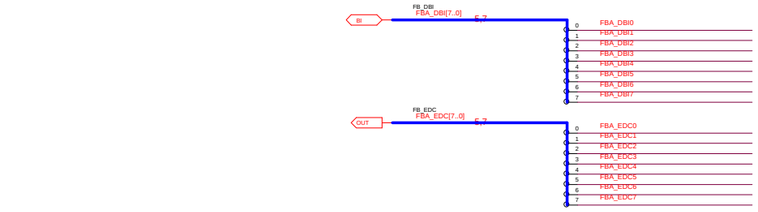
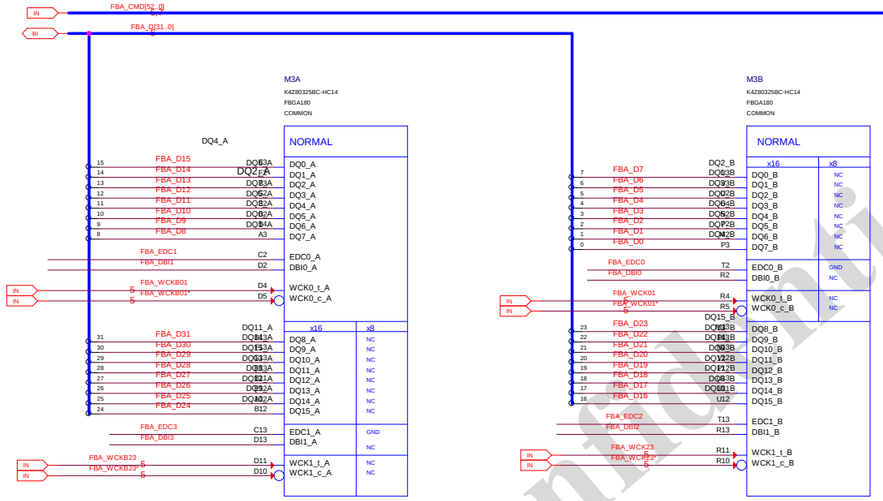
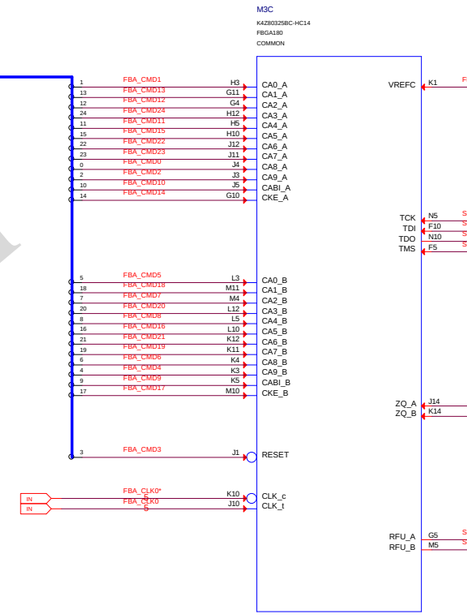
Page6: MEMORY: FBA Partition 31..0

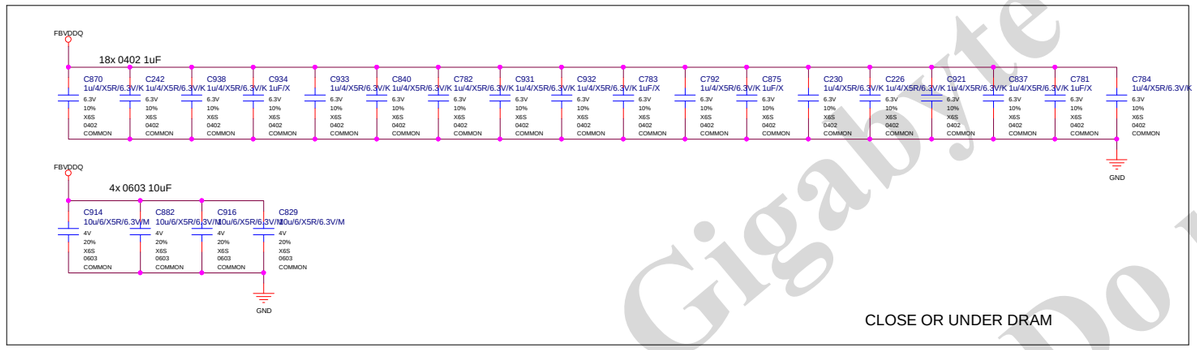


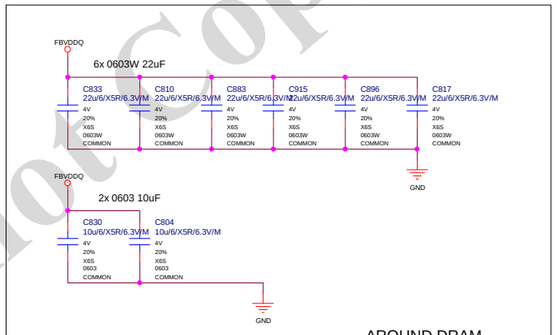
decap via : at least 2 gnd vias and 2 power vias for each cap

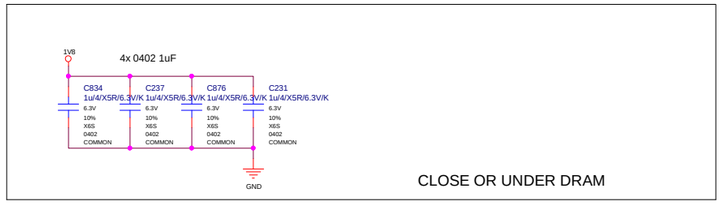












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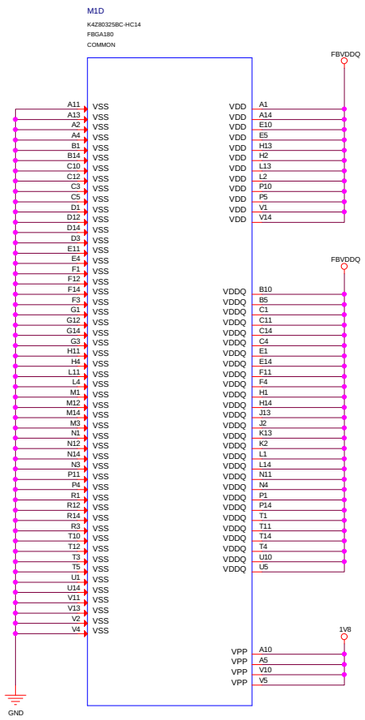

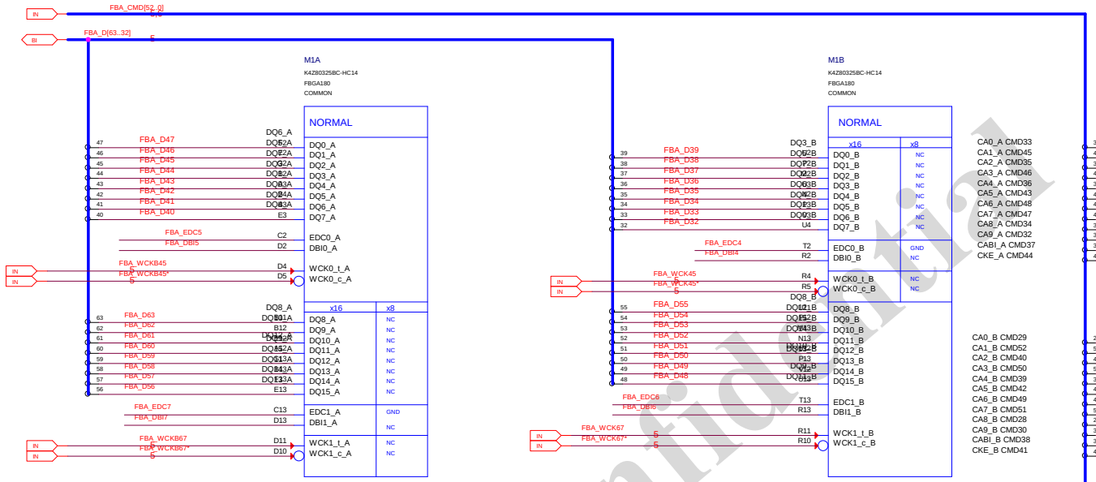

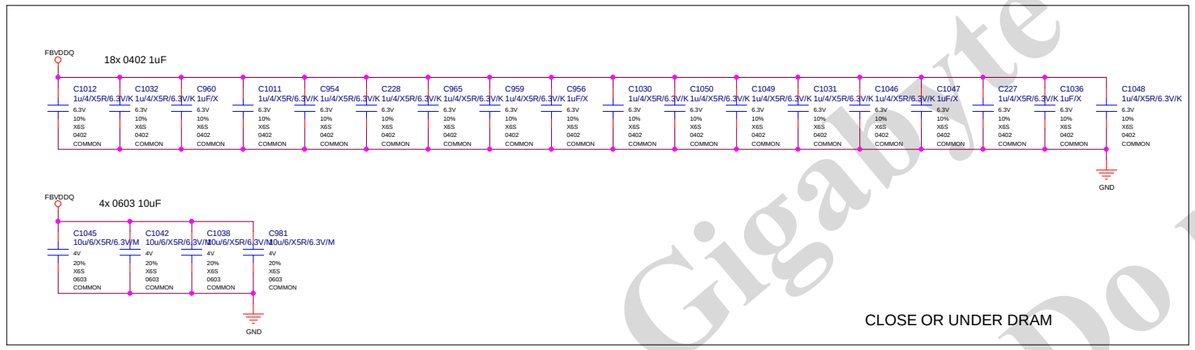

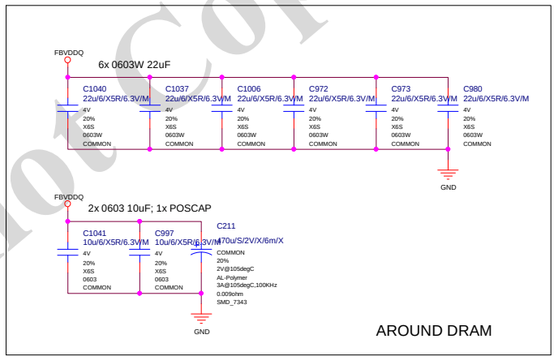

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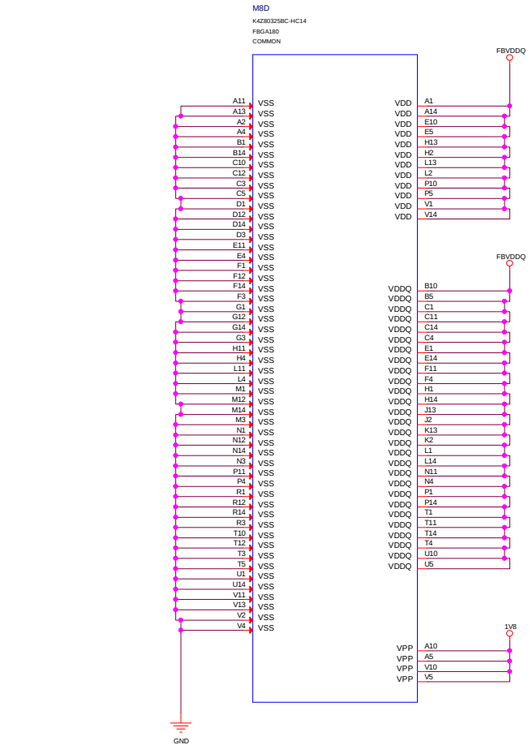

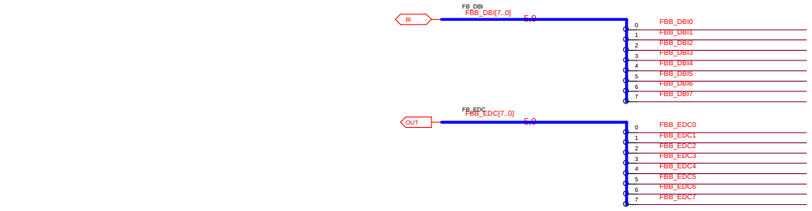

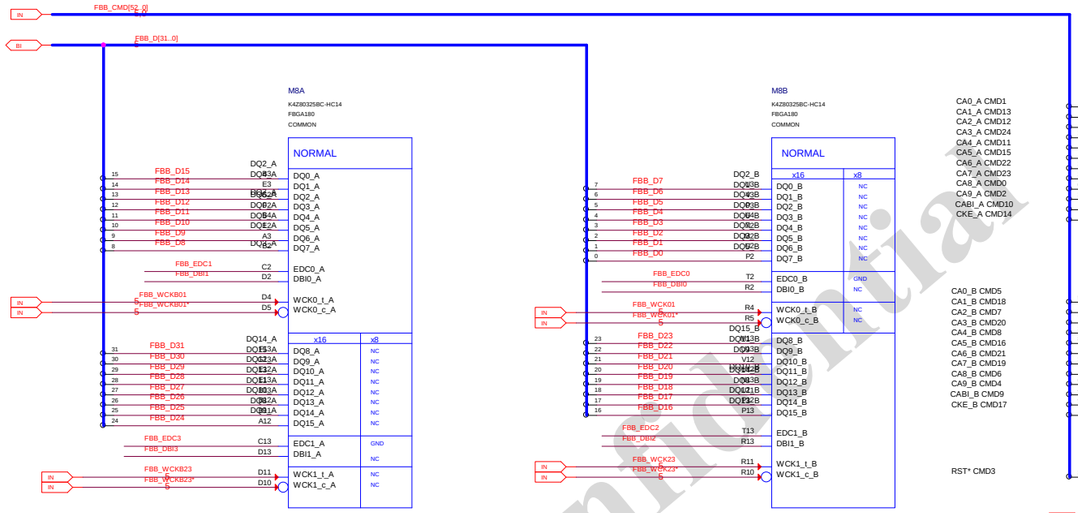

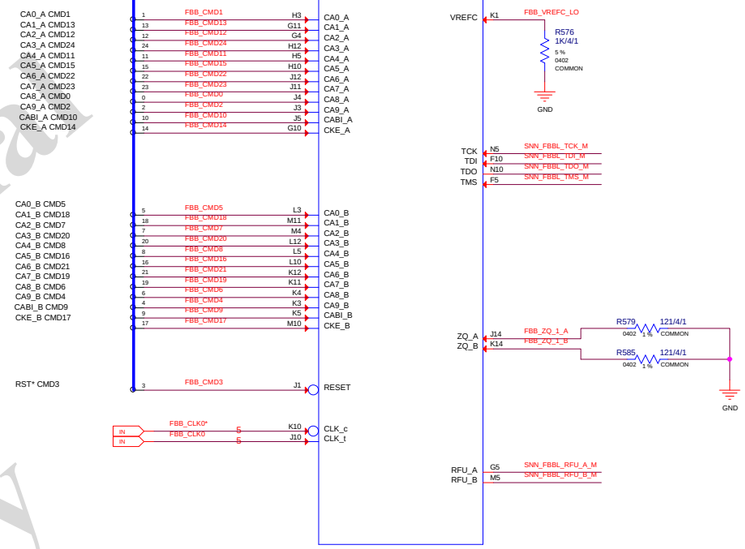

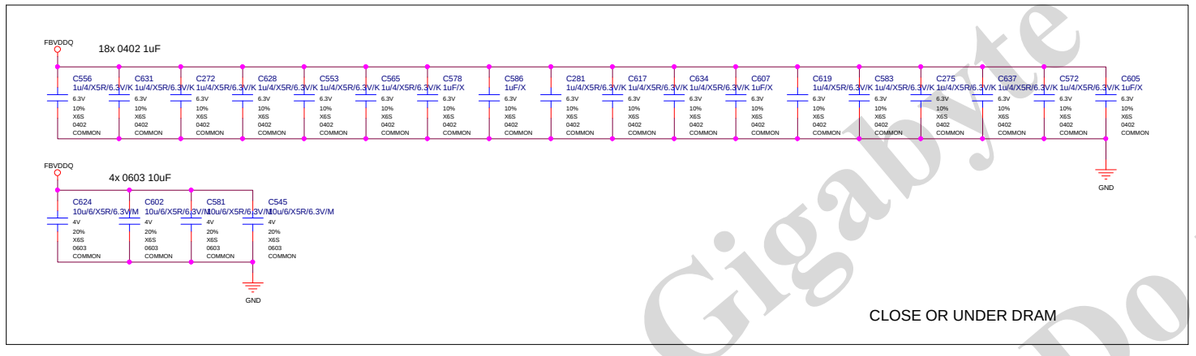

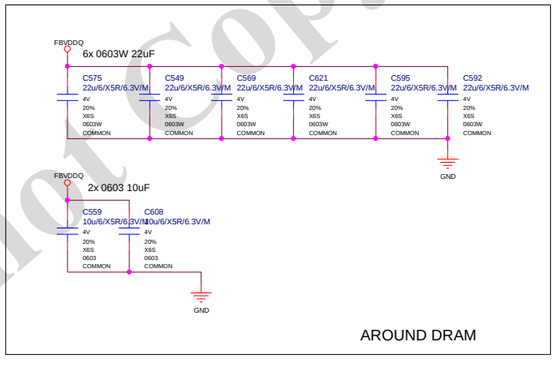

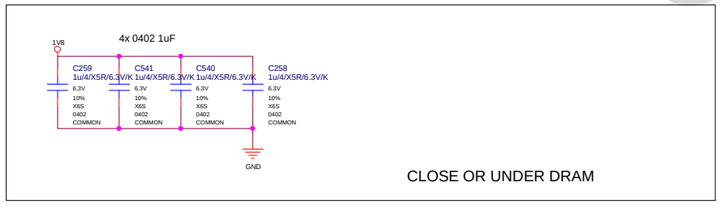

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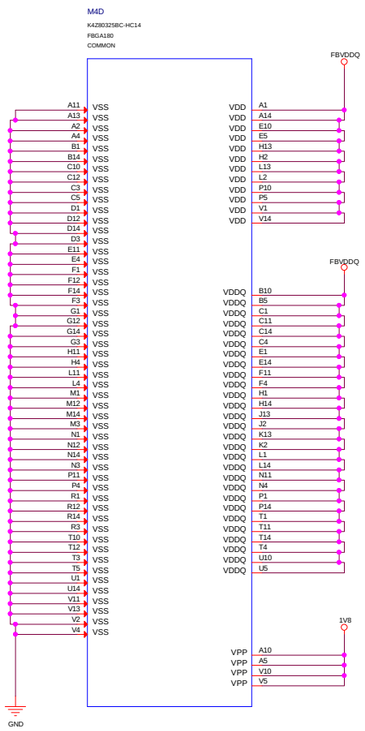

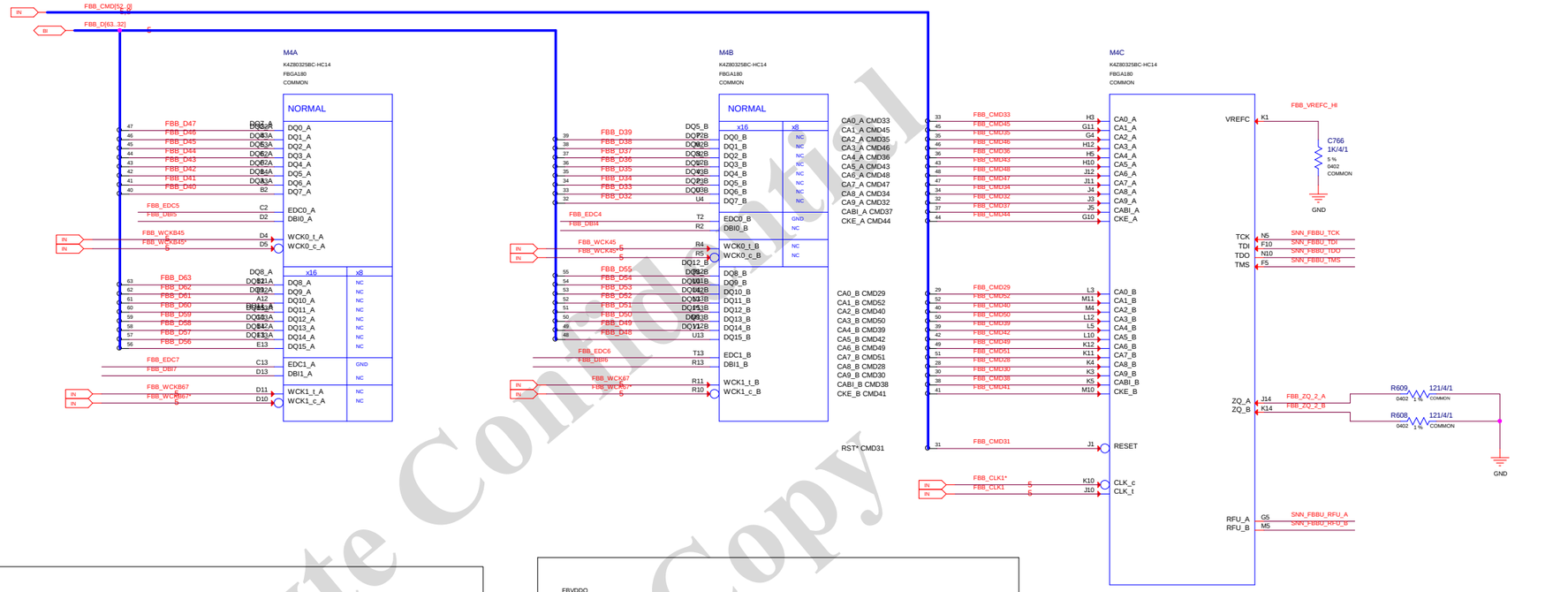

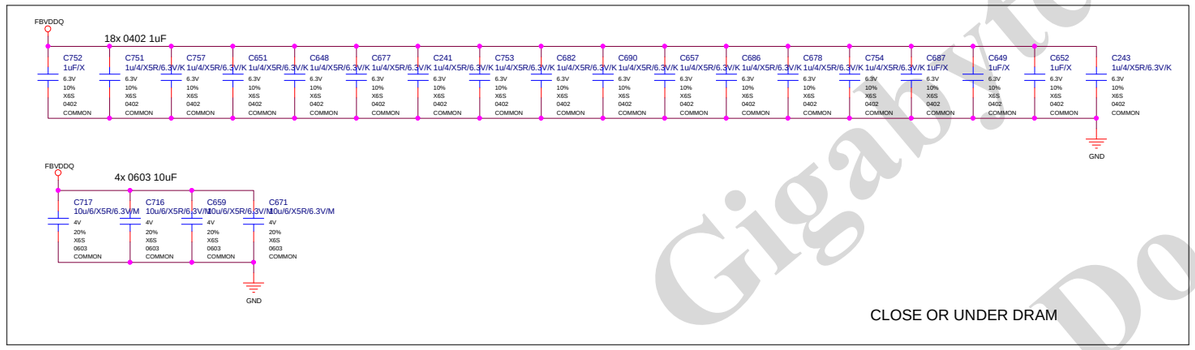

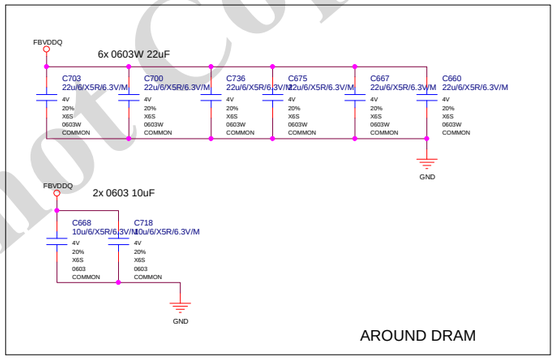

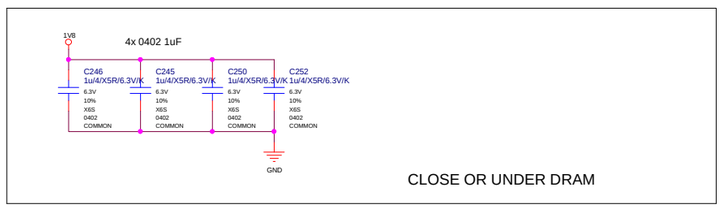

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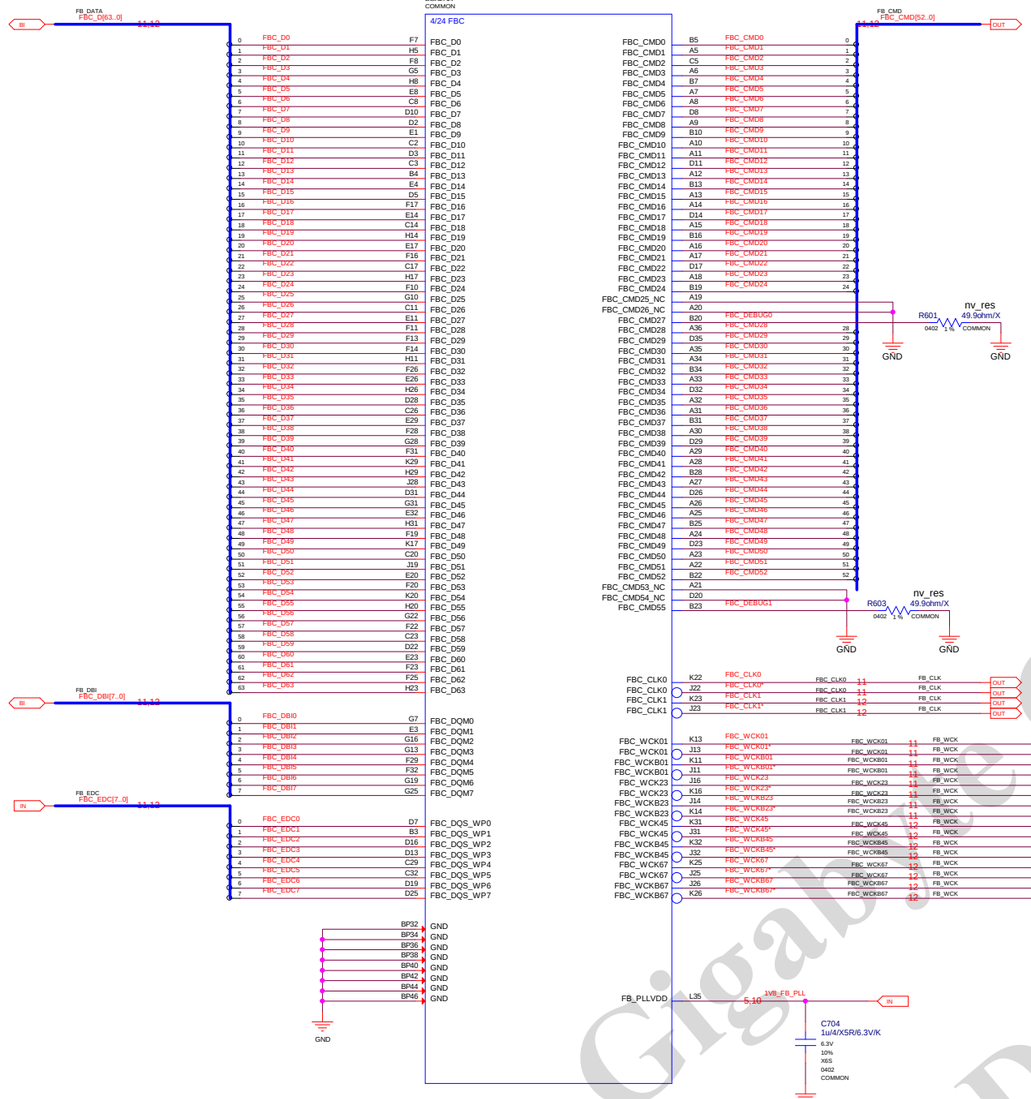

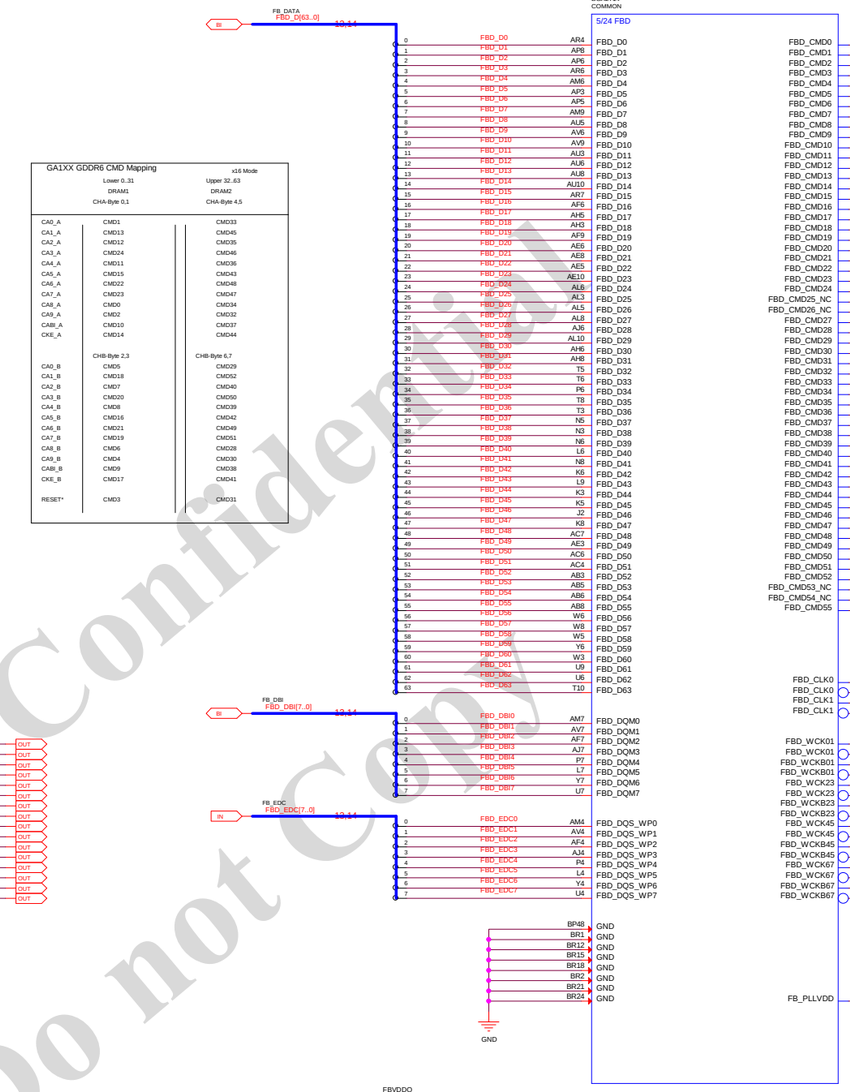

GA1XX GDDR6 CMD Mapping

	Lower 0..31 / DRAM1 / CHA-Byte 0,1	x16 Mode: Upper 32..63 / DRAM2 / CHA-Byte 4,5
CA0_A	CMD1	CMD33
CA1_A	CMD13	CMD45
CA2_A	CMD12	CMD35
CA3_A	CMD24	CMD46
CA4_A	CMD11	CMD36
CA5_A	CMD15	CMD43
CA6_A	CMD22	CMD48
CA7_A	CMD23	CMD47
CA8_A	CMD0	CMD34
CA9_A	CMD2	CMD32
CABI_A	CMD10	CMD37
CKE_A	CMD14	CMD44
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD5	CMD29
CA1_B	CMD18	CMD52
CA2_B	CMD7	CMD40
CA3_B	CMD20	CMD50
CA4_B	CMD8	CMD39
CA5_B	CMD16	CMD42
CA6_B	CMD21	CMD49
CA7_B	CMD19	CMD51
CA8_B	CMD6	CMD28
CA9_B	CMD4	CMD30
CABI_B	CMD9	CMD38
CKE_B	CMD17	CMD41
RESET*	CMD3	CMD31

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: GPU Partition C/D

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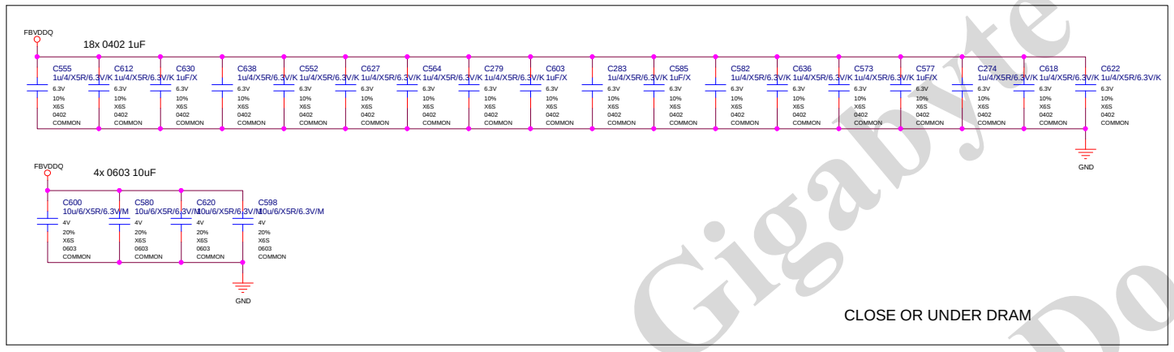
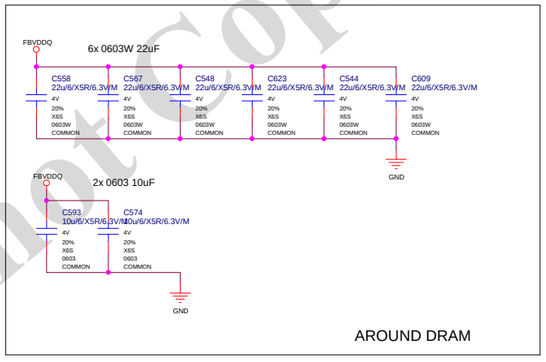
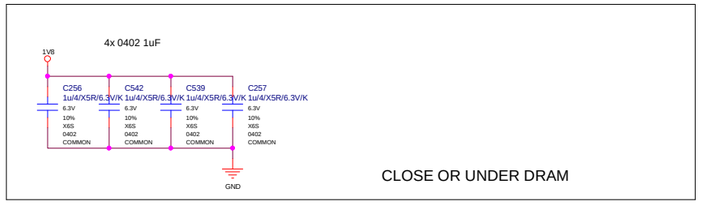
Page11: MEMORY: FBC Partition 31..0







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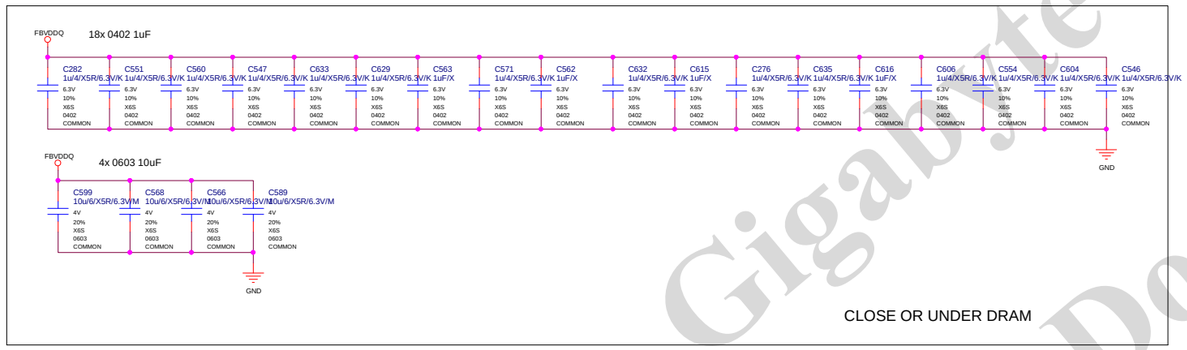
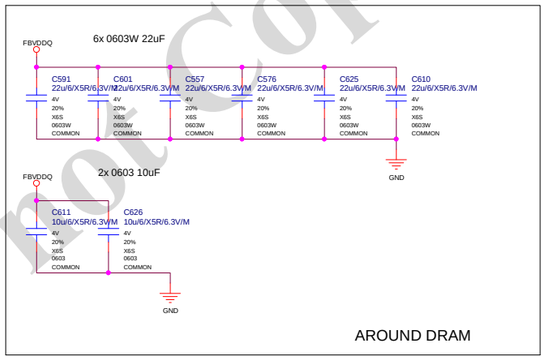
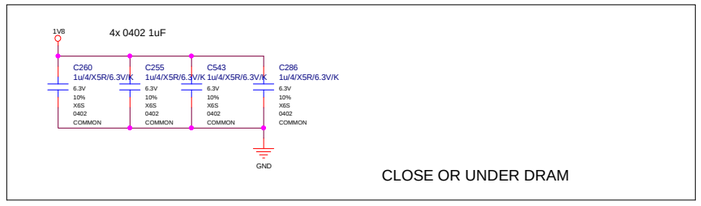
Page12: MEMORY: FBC Partition 63..32







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PAGE DETAIL	MEMORY: FBC Partition 63..32

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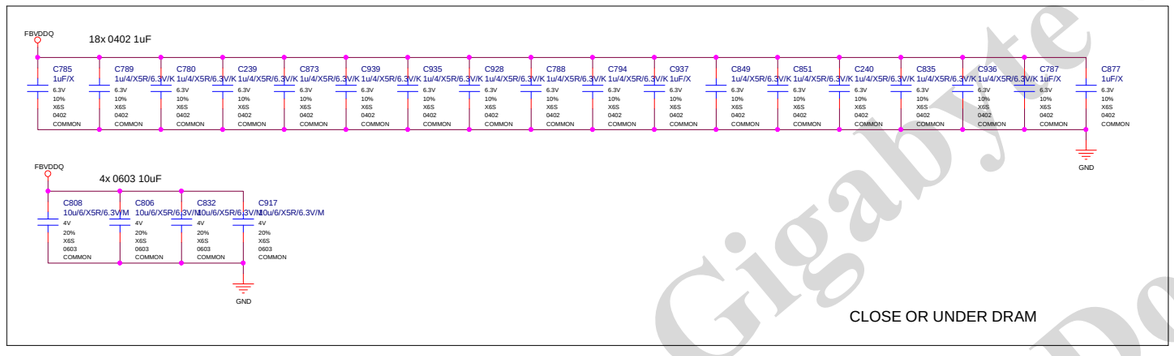
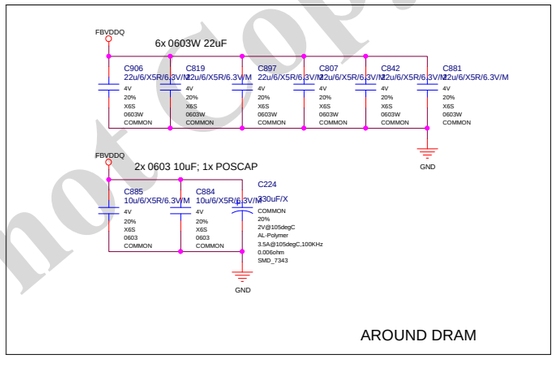
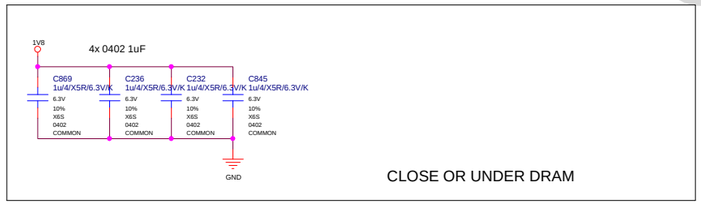
Page13: MEMORY: FBD Partition 31..0







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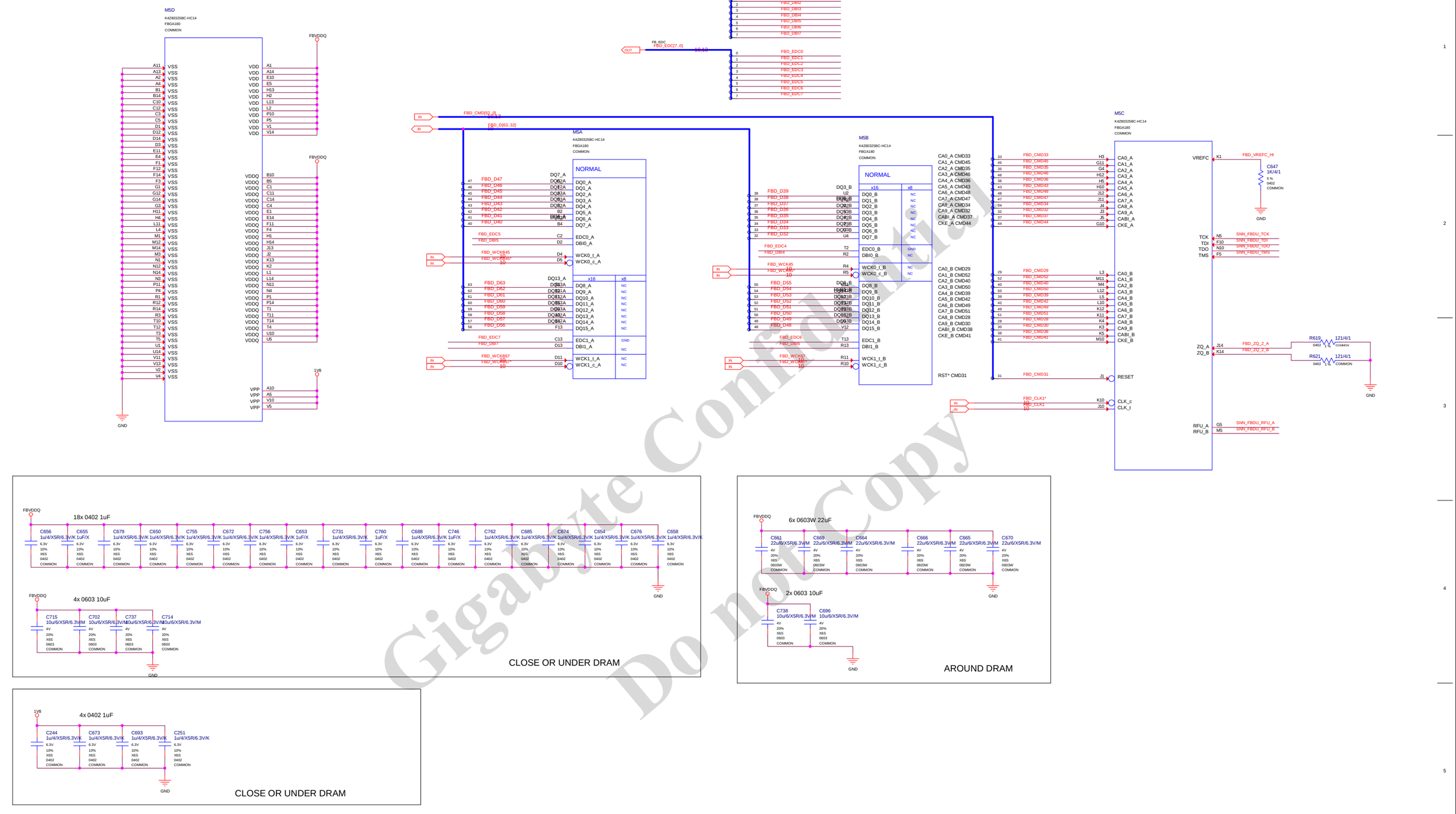
Page14: MEMORY: FBD Partition 63..32



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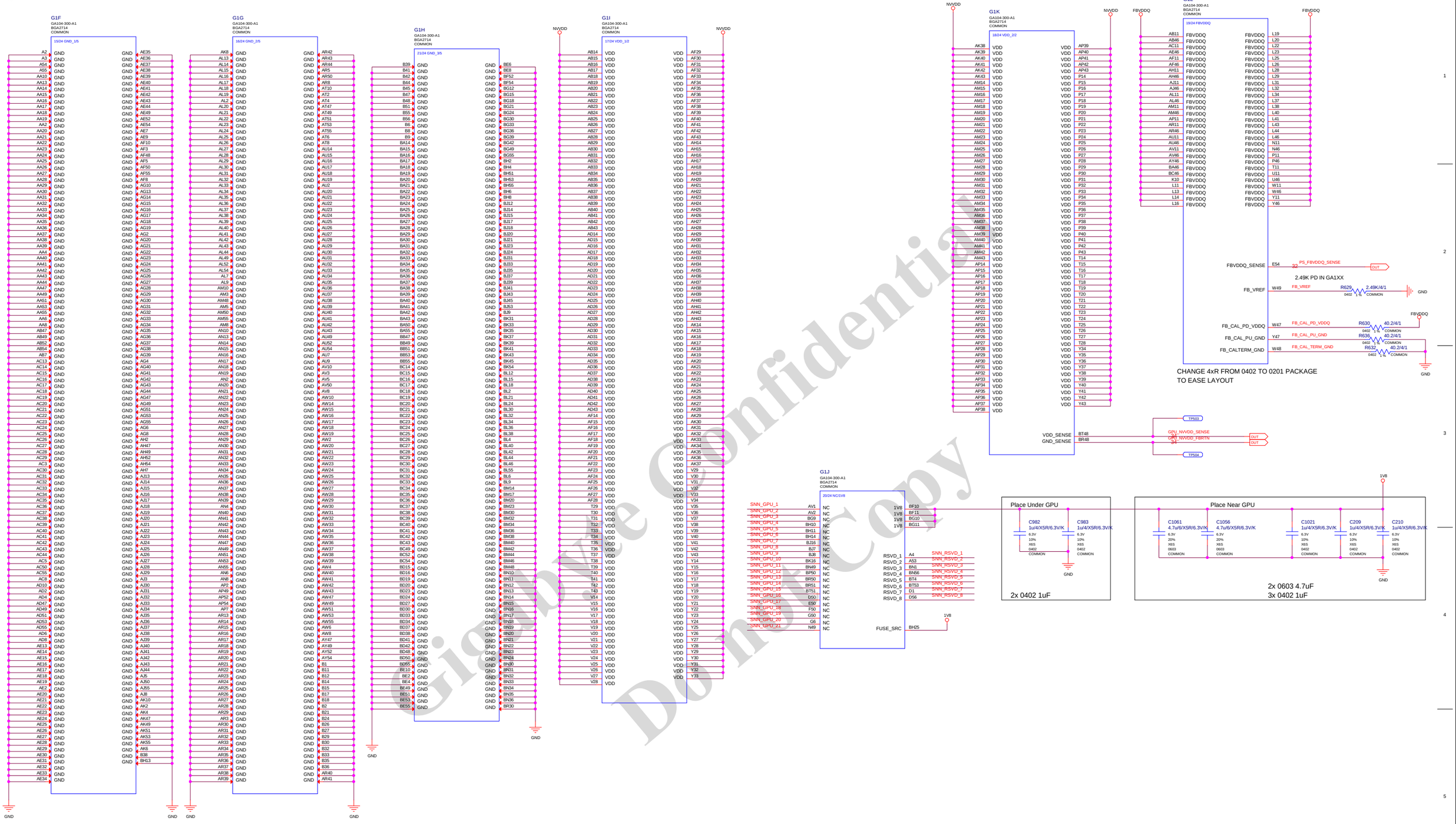
Page15: GPU PWR and GND



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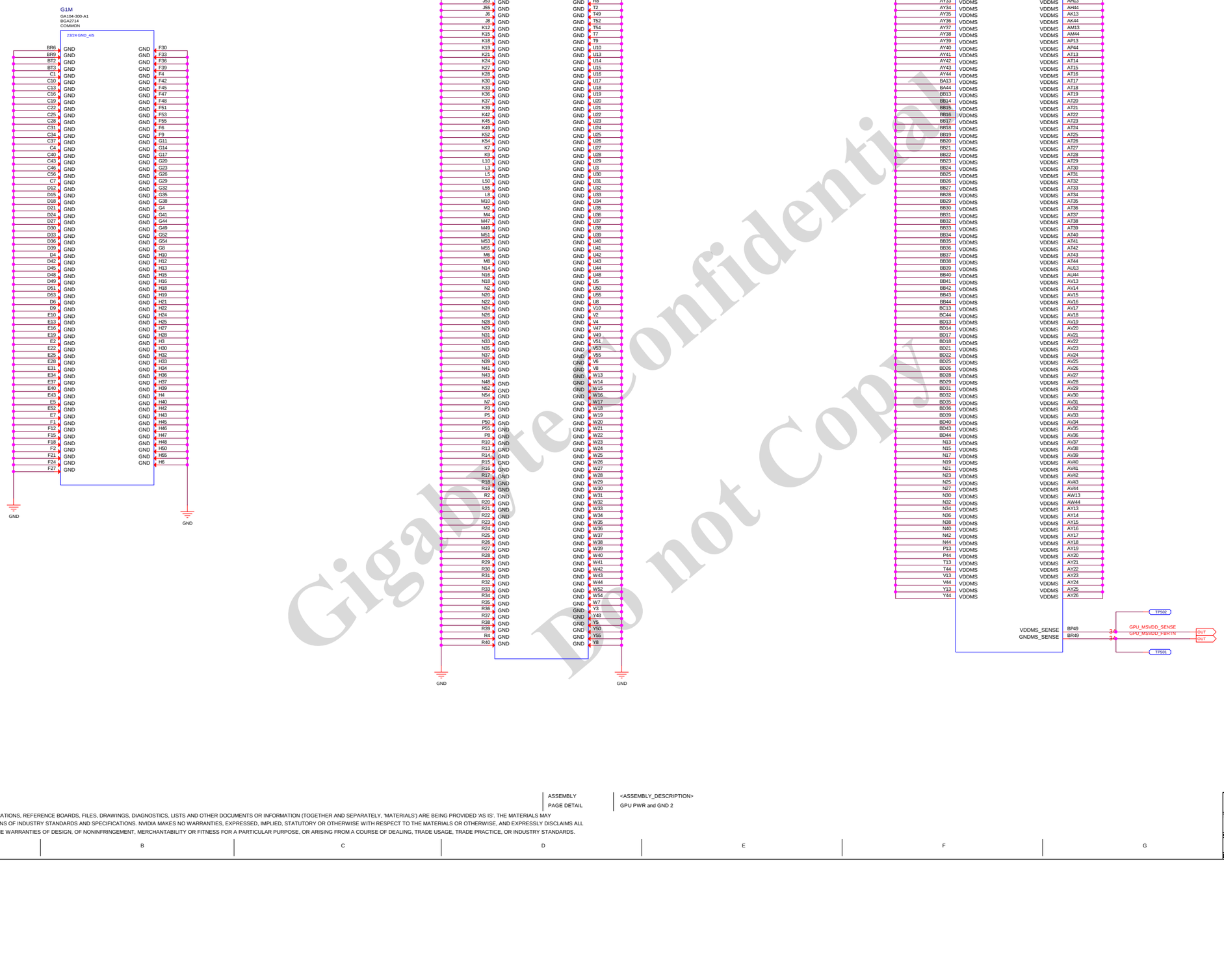
Page16: GPU PWR and GND 2



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PAGE DETAIL GPU PWR and GND 2

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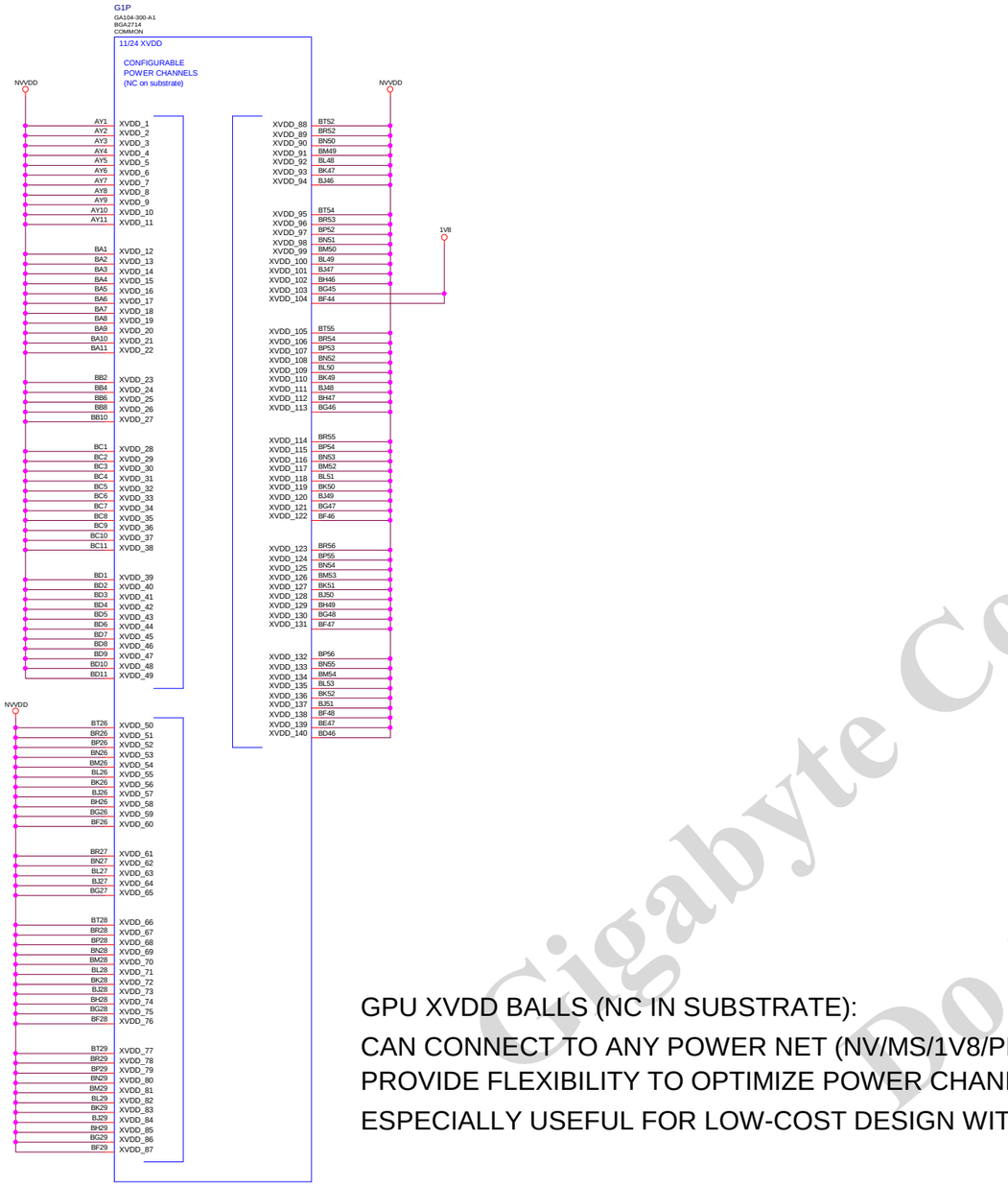
Page17: GPU XVDD



GPU XVDD BALLS (NC IN SUBSTRATE):

CAN CONNECT TO ANY POWER NET (NV/MS/1V8/PEX, etc.) ON SYSTEM BOARD,
PROVIDE FLEXIBILITY TO OPTIMIZE POWER CHANNELS ON SYSTEM BOARD,
ESPECIALLY USEFUL FOR LOW-COST DESIGN WITH REDUCED PCB LAYERS.

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL GPU XVDD

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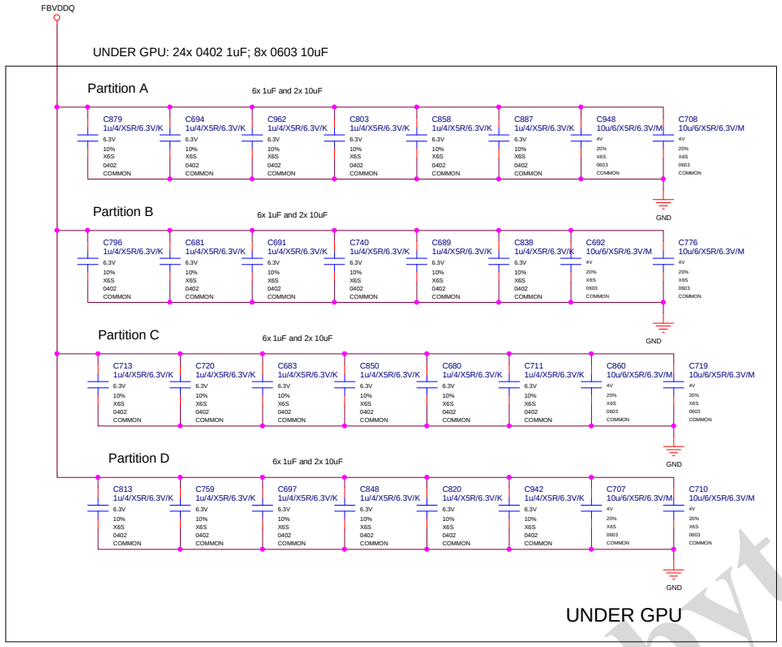
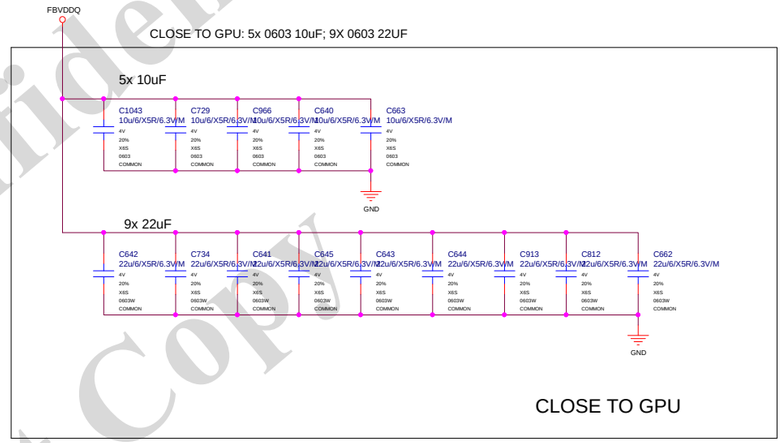
Page18: GPU DECOUPLING FBVDDQ

FBVDDQ



FBVDDQ



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING FBVDDQ

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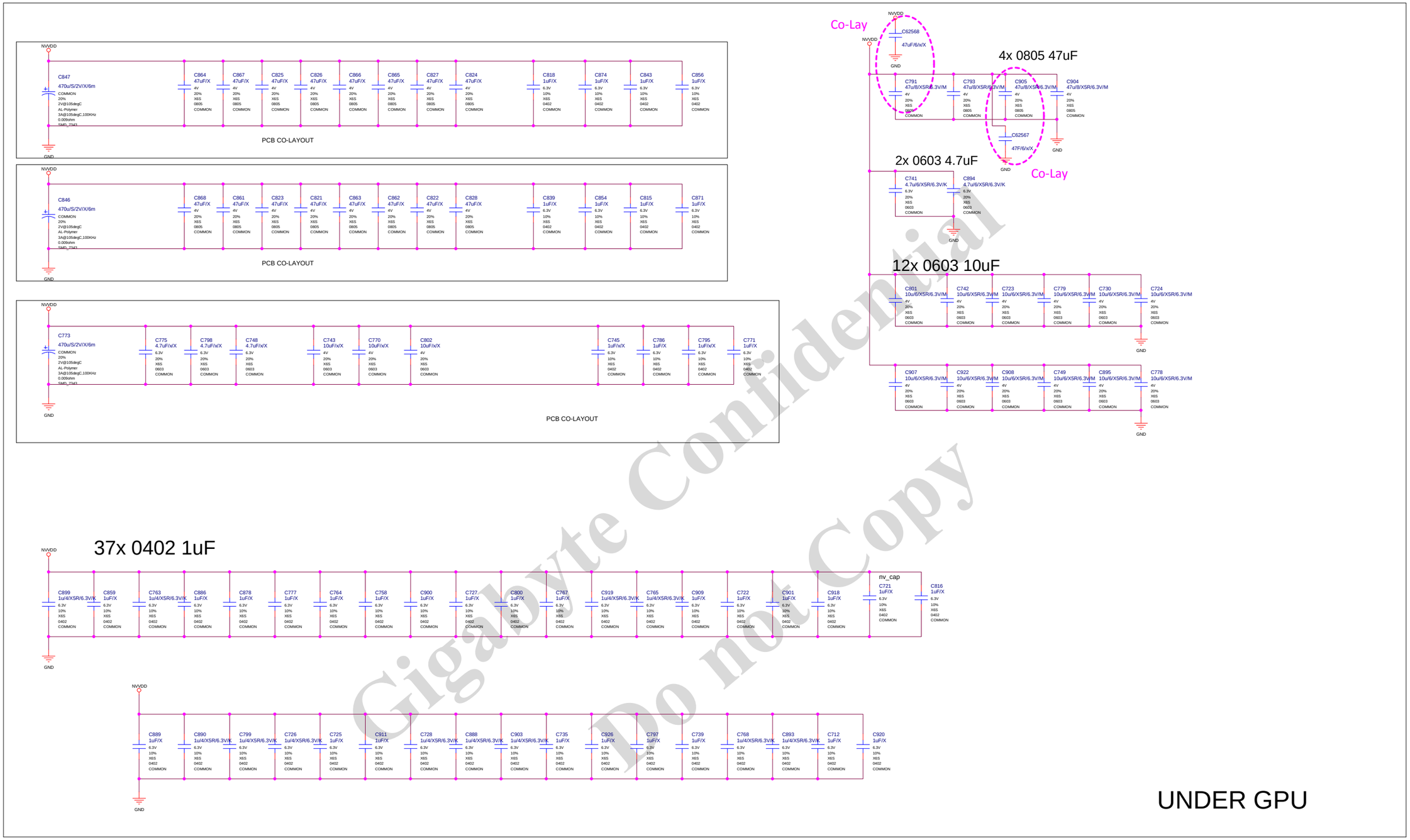
Page19: GPU DECOUPLING NVVDD



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING NVVDD

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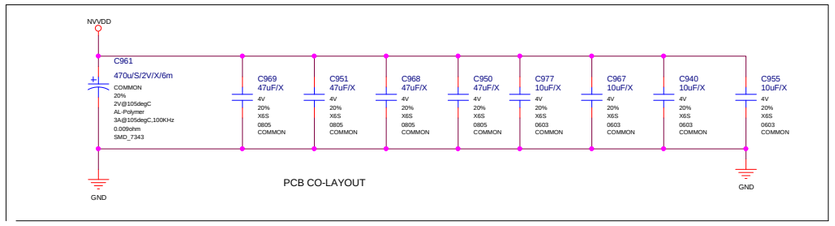
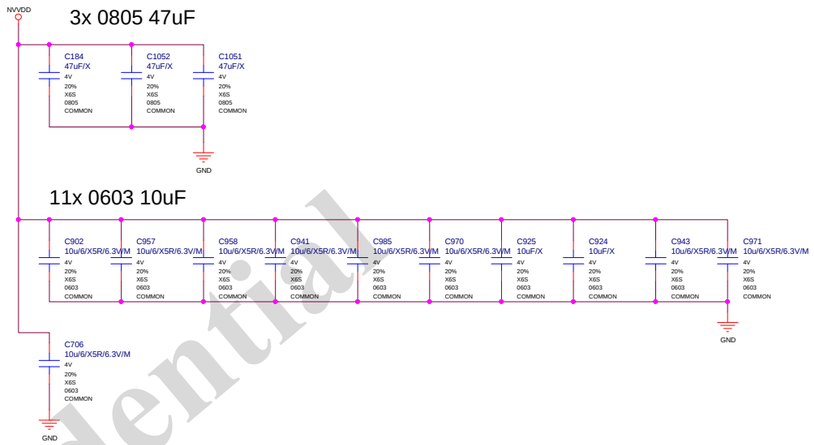
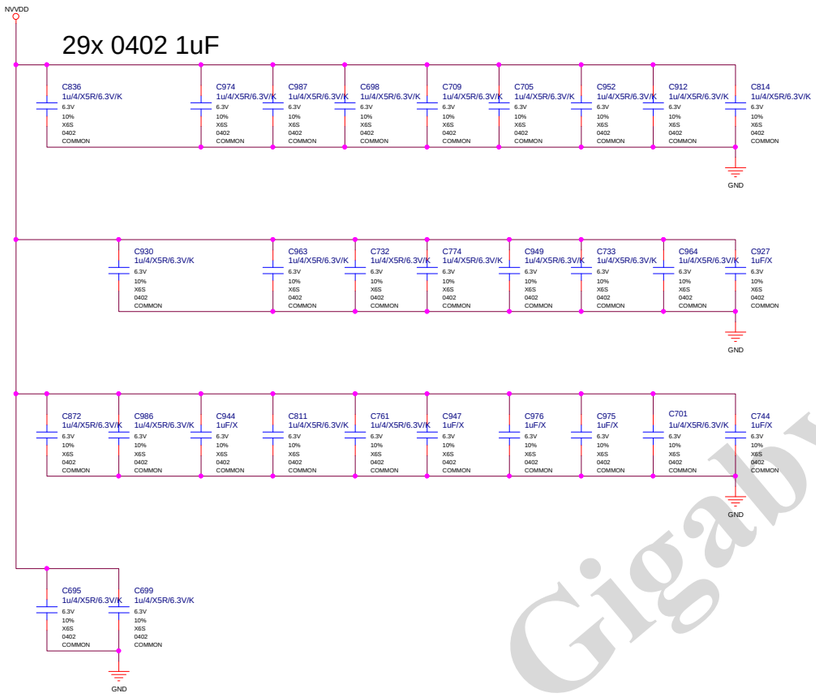
Page20: GPU DECOUPLING NVVDD 2







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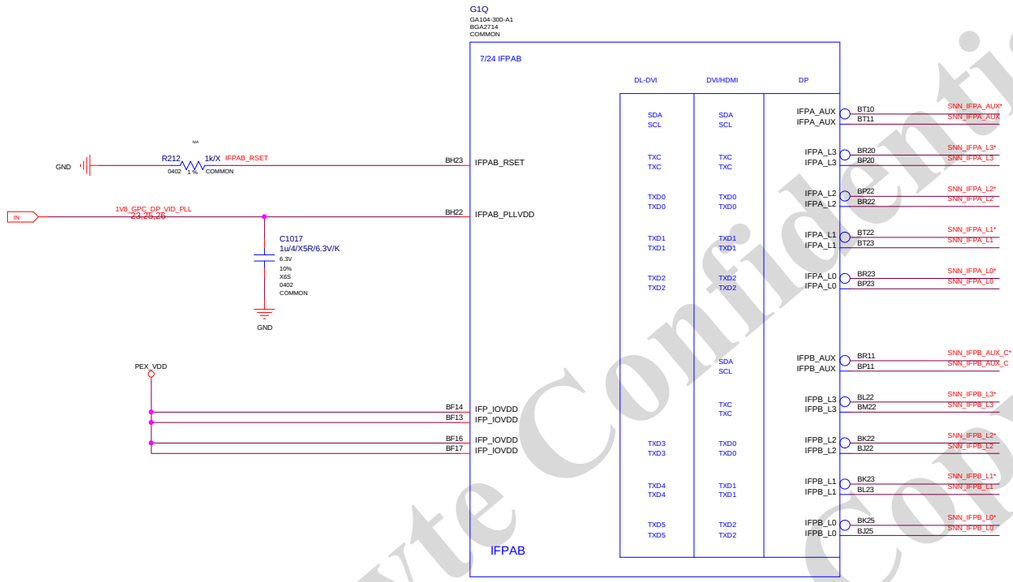
Page21: IFPAB DVI-D-DL



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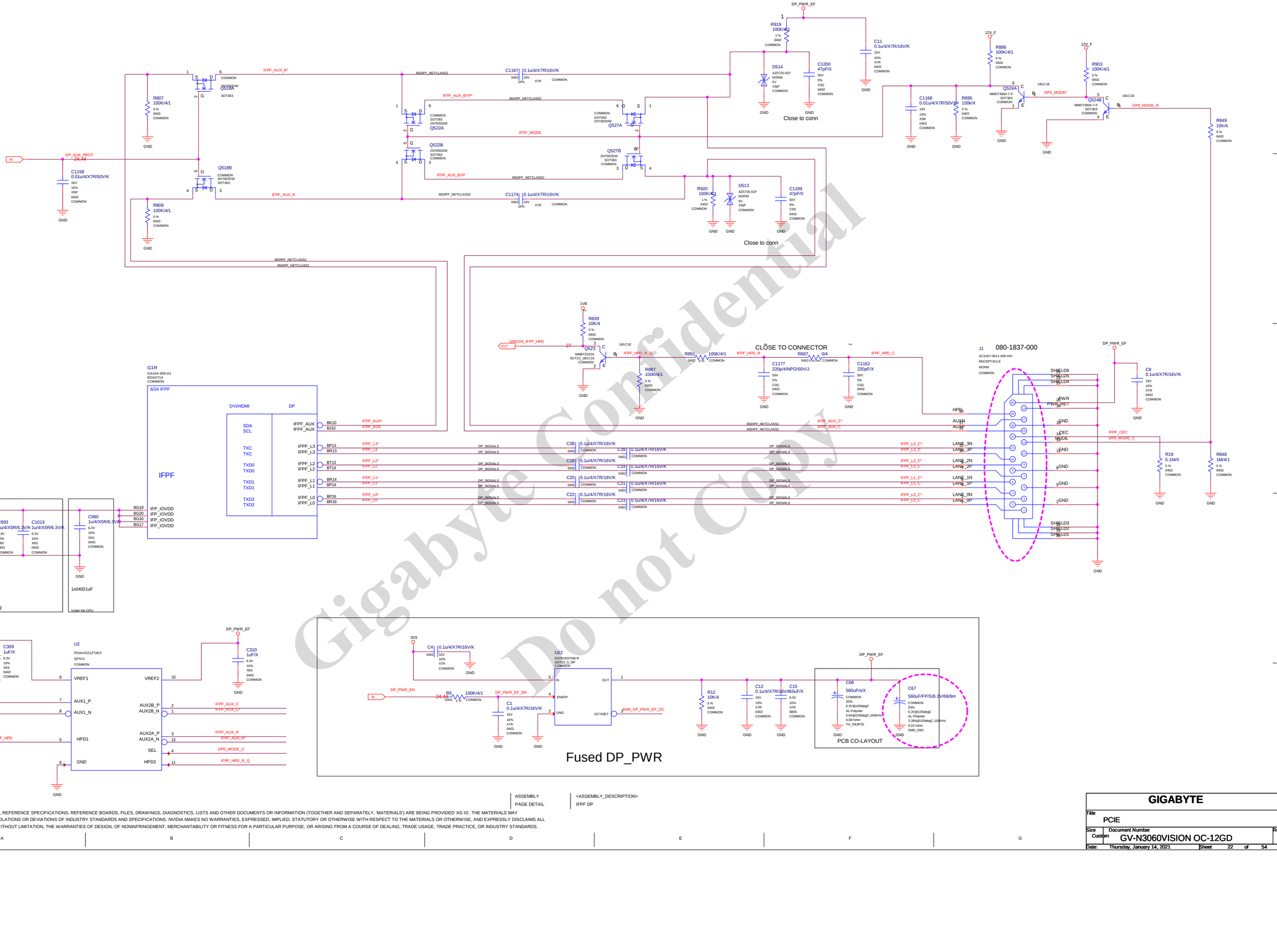
Page22: IFPF DP



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PAGE DETAIL	IFPF DP

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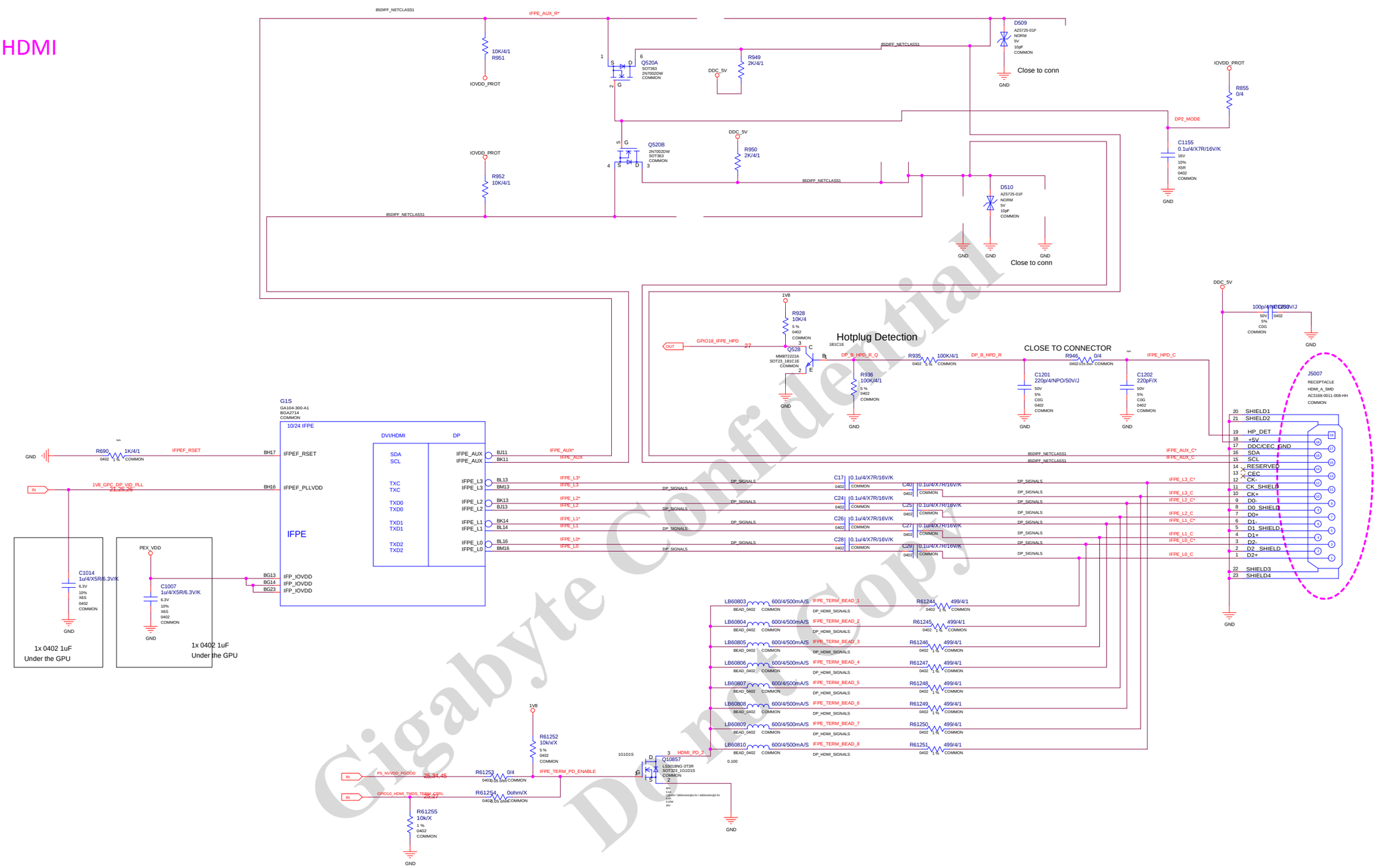
Page23: IFPE DP

Change to HDMI



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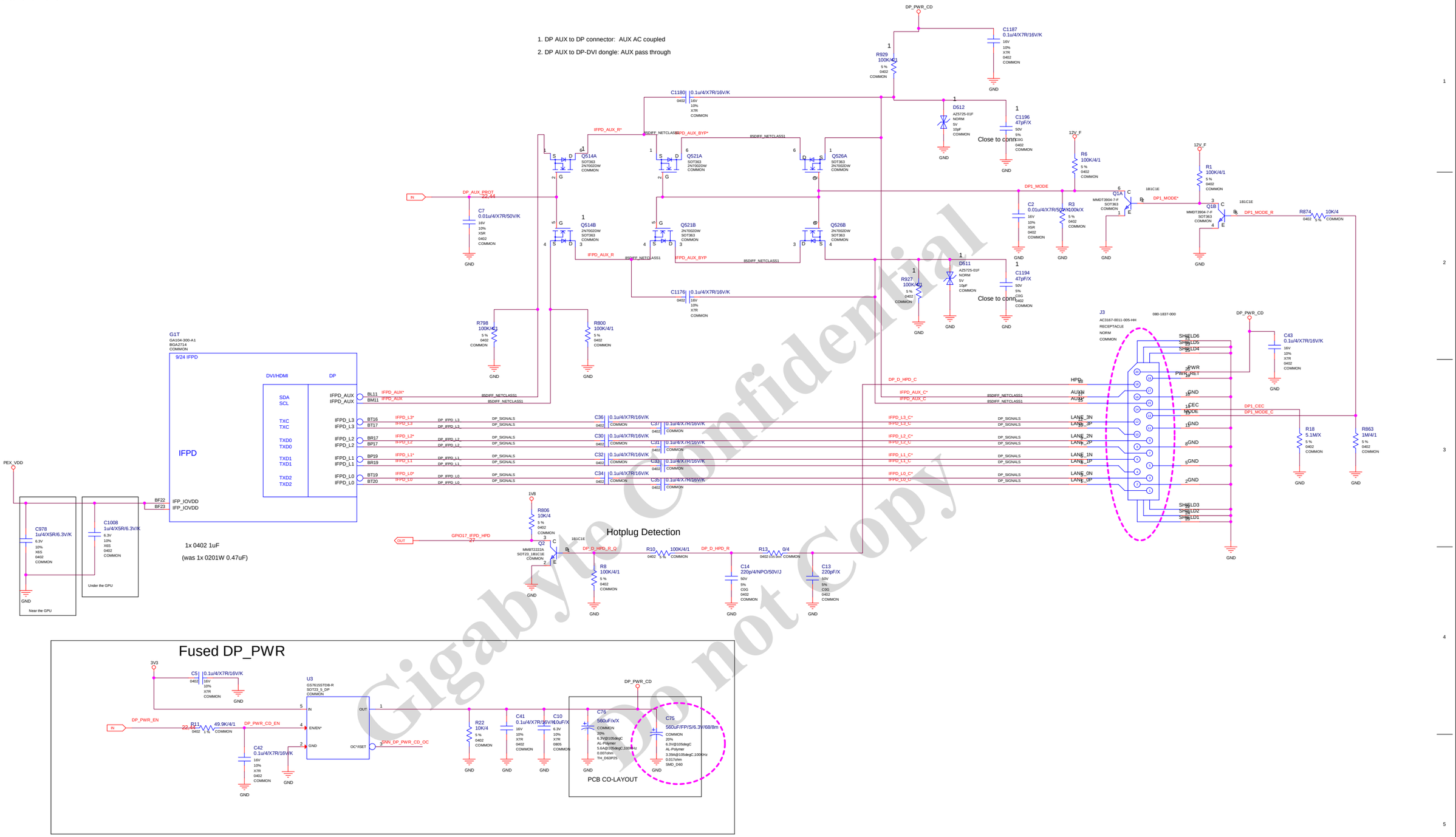
Page24: IFPD DP



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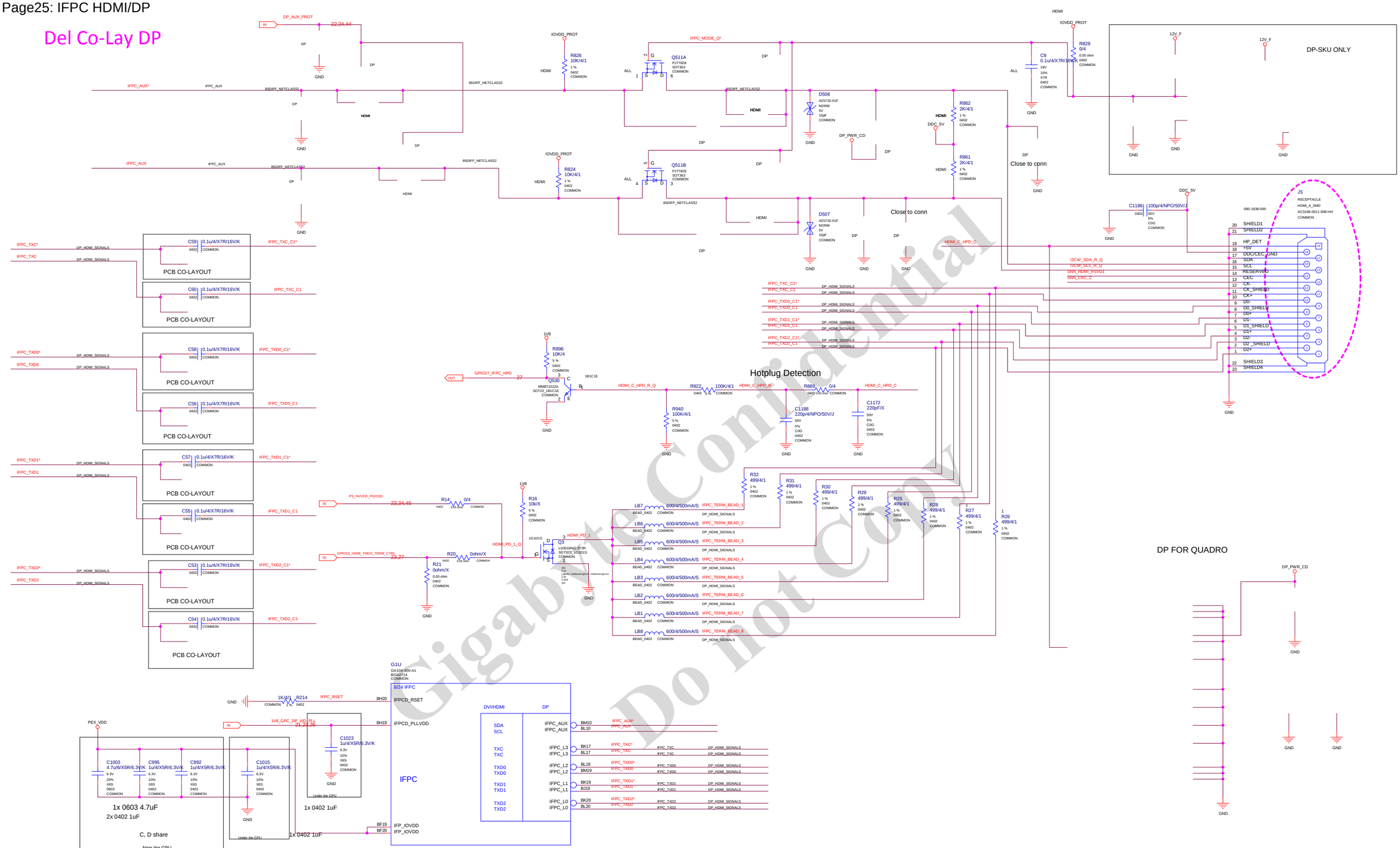
Page25: IFPC HDMI/DP

Del Co-Lay DP



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPC HDMI/DP

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Page26: MISC: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	4'd7	FS_OVERT ENABLE
L	M	L	4'd9	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

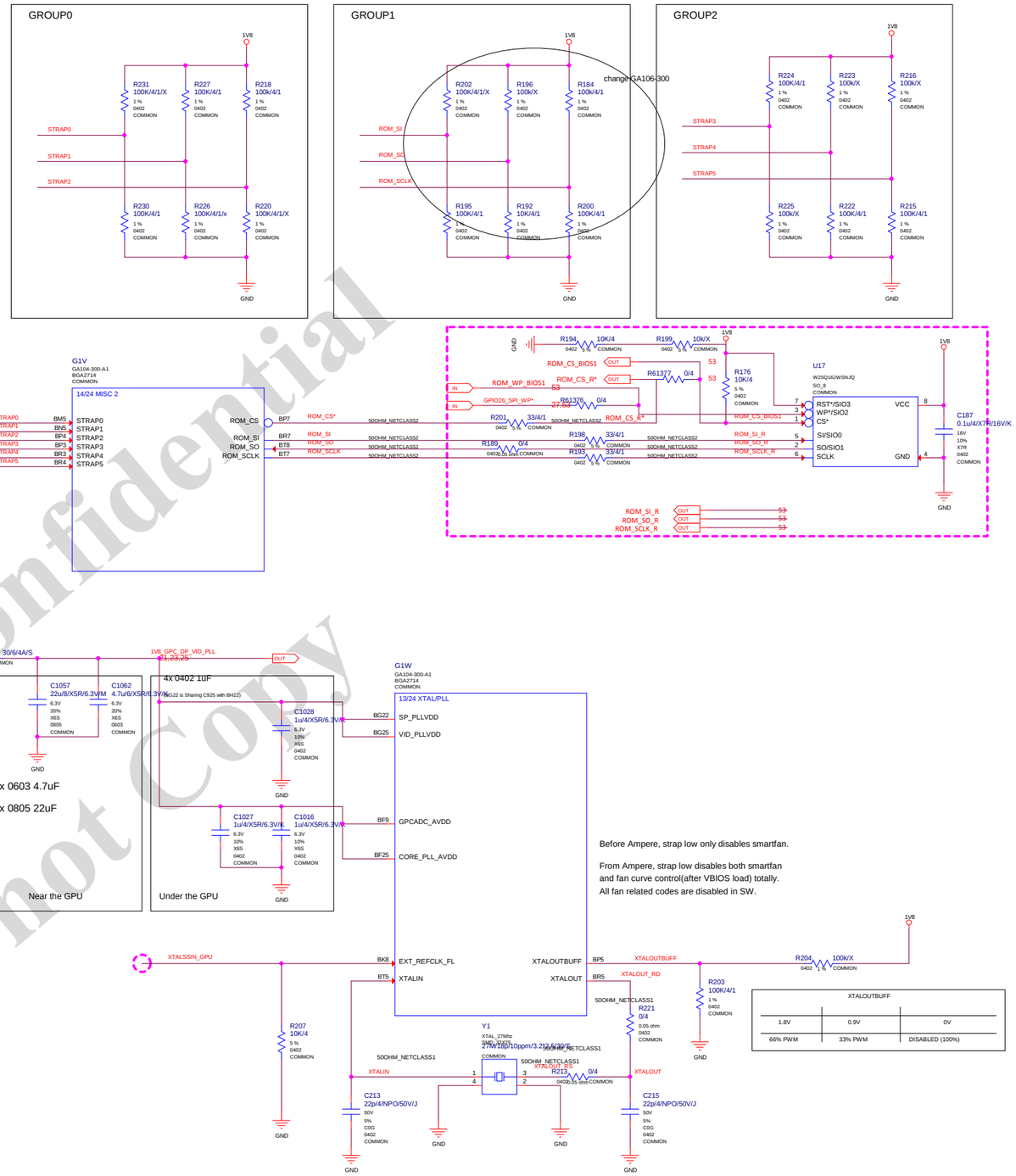
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL MISC: ROM, XTAL, STRAPS

GIGABYTE

Title: PCIE

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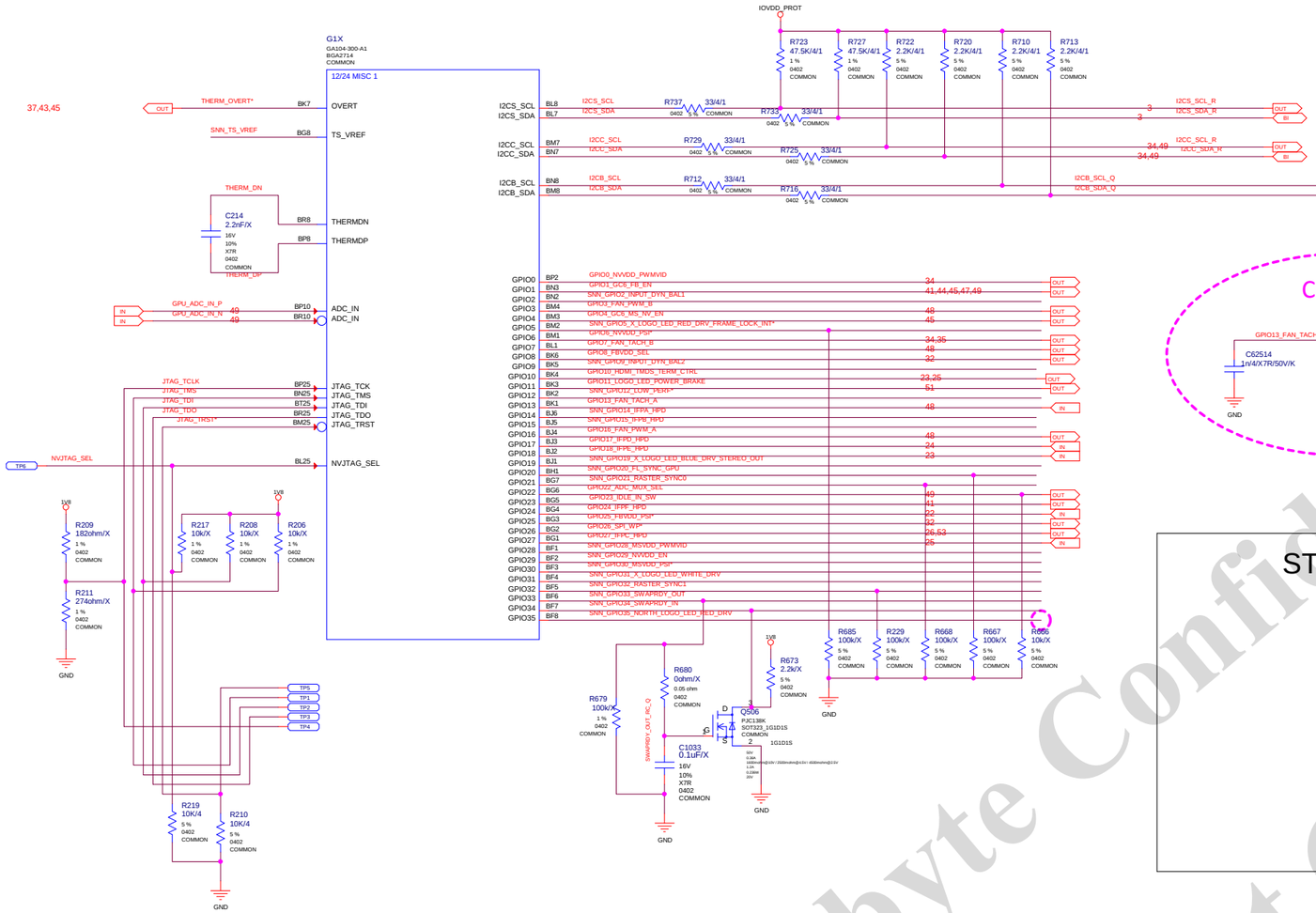
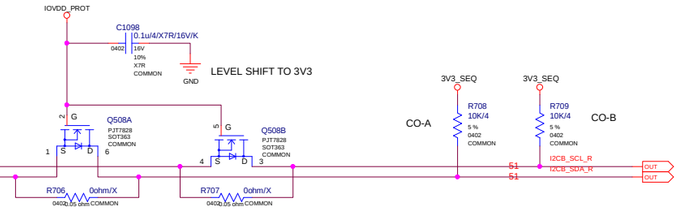
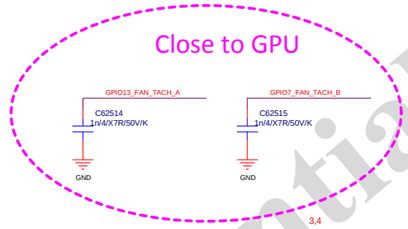
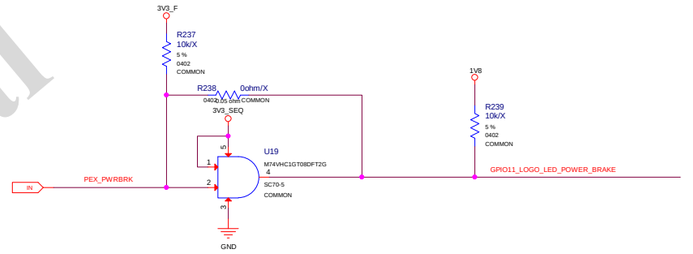
Page27: MISC2: JTAG, GPIO, ADC, I2C, OVERT









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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL MISC2: JTAG,GPIO,ADC.12C,OVERT

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	GIGABYTE
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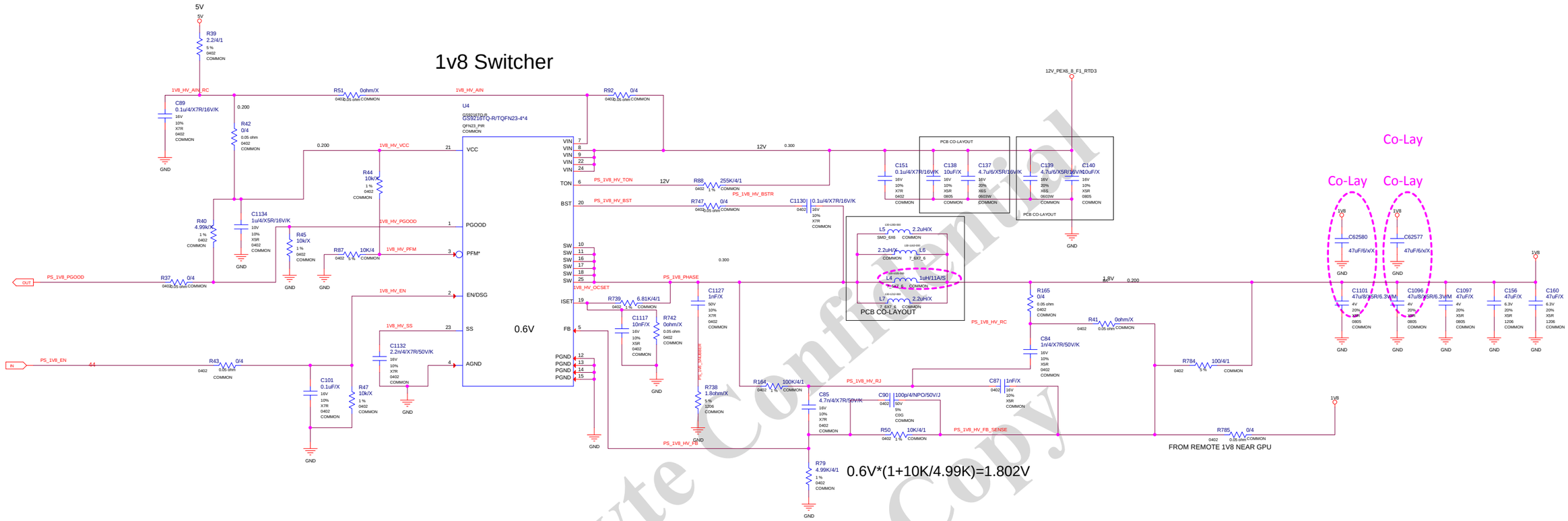
1v8 Switcher



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PAGE DETAIL P:S: 1V8

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Title: PCIE

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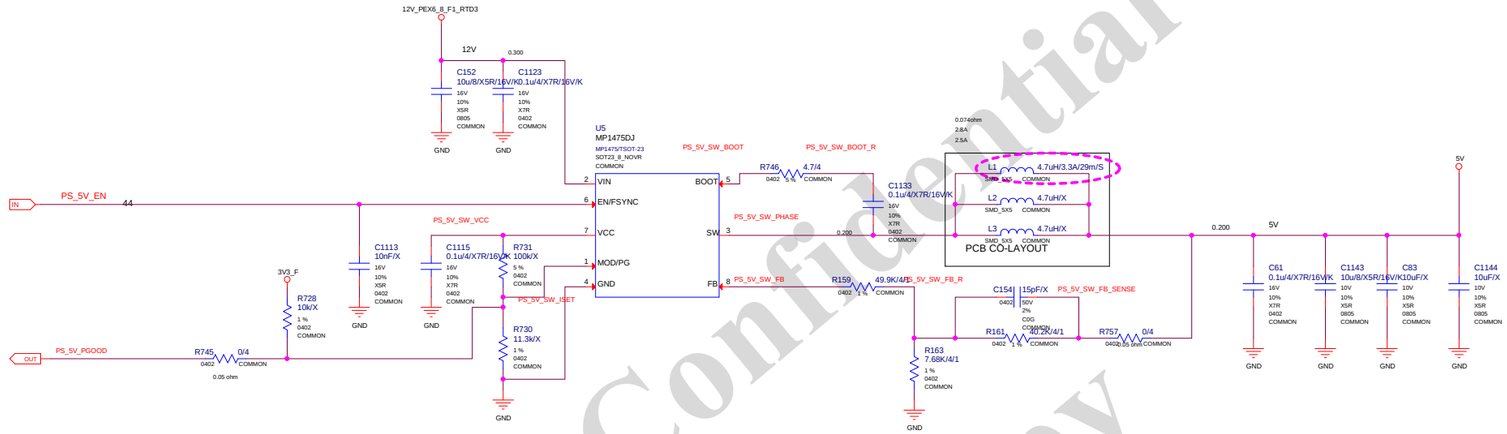
Page30: PS: 5V



0.8V*(1+40.2K/7.68K)=4.9875V

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: 5V

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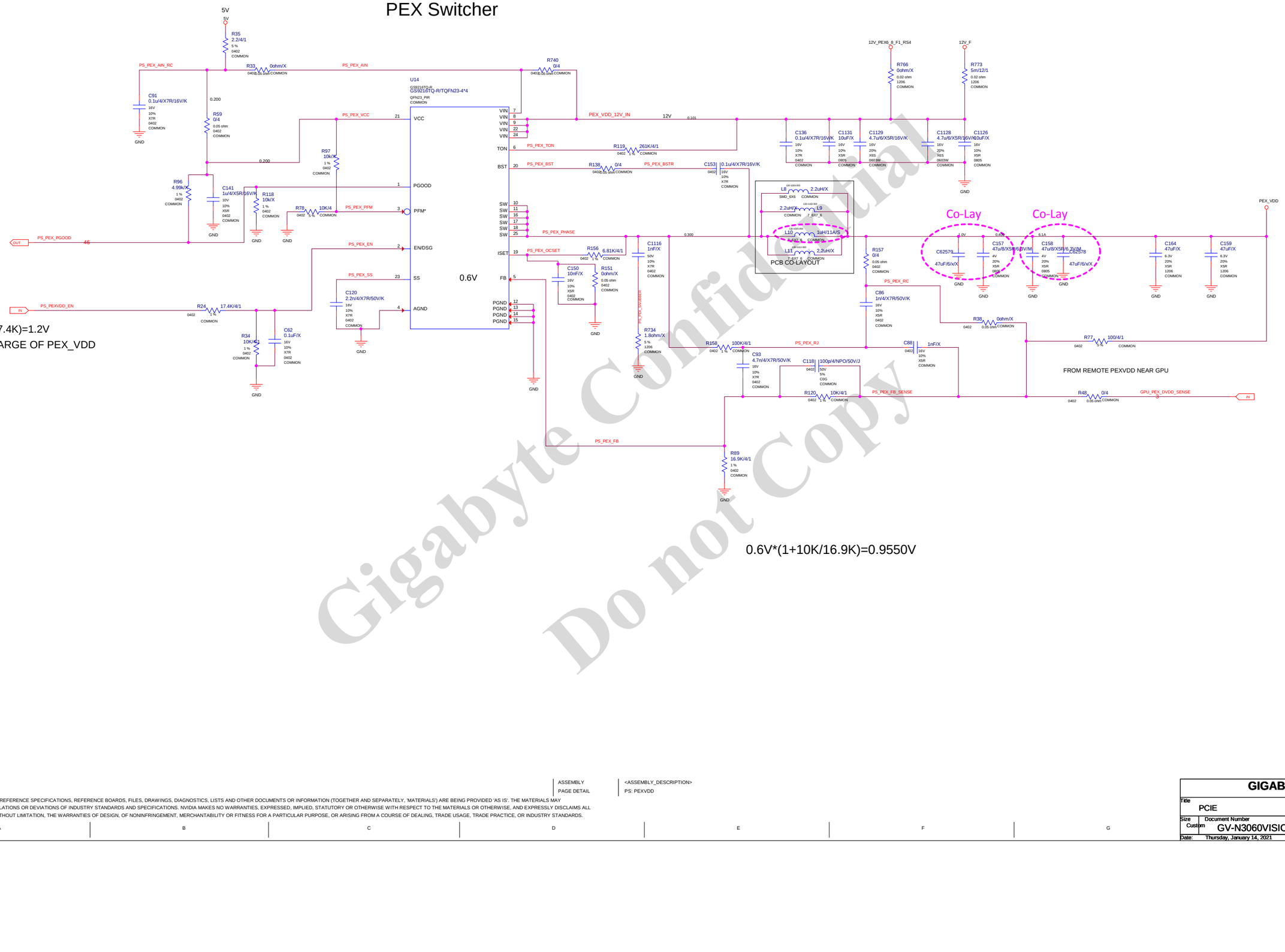
PEX Switcher



EN: 3.3V*(10K/27.4K)=1.2V

ENABLE DISCHARGE OF PEX_VDD

0.6V*(1+10K/16.9K)=0.9550V

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PAGE DETAIL PS: PEXVDD

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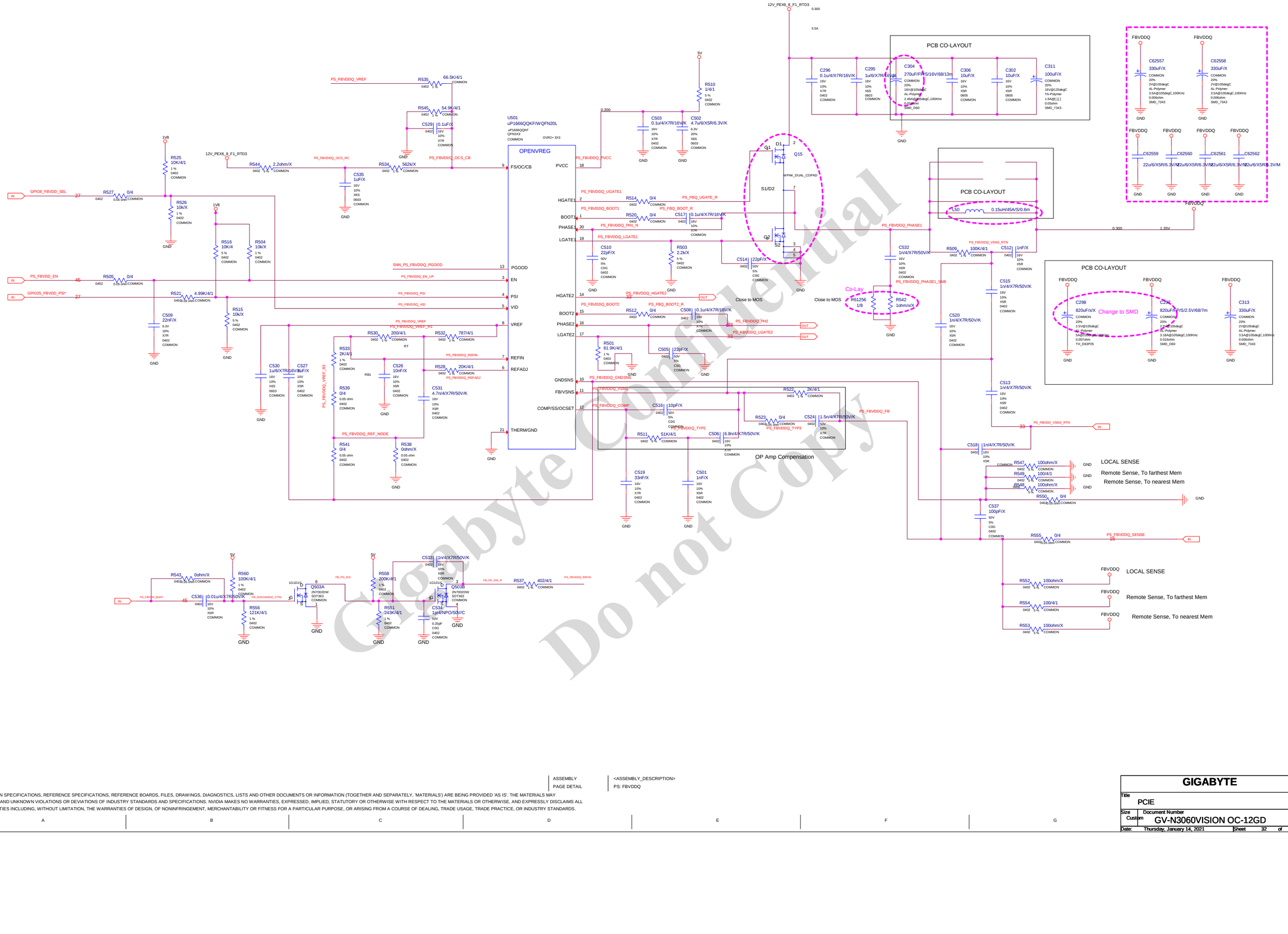
Page32: PS: FBVDDQ



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: FBVDDQ

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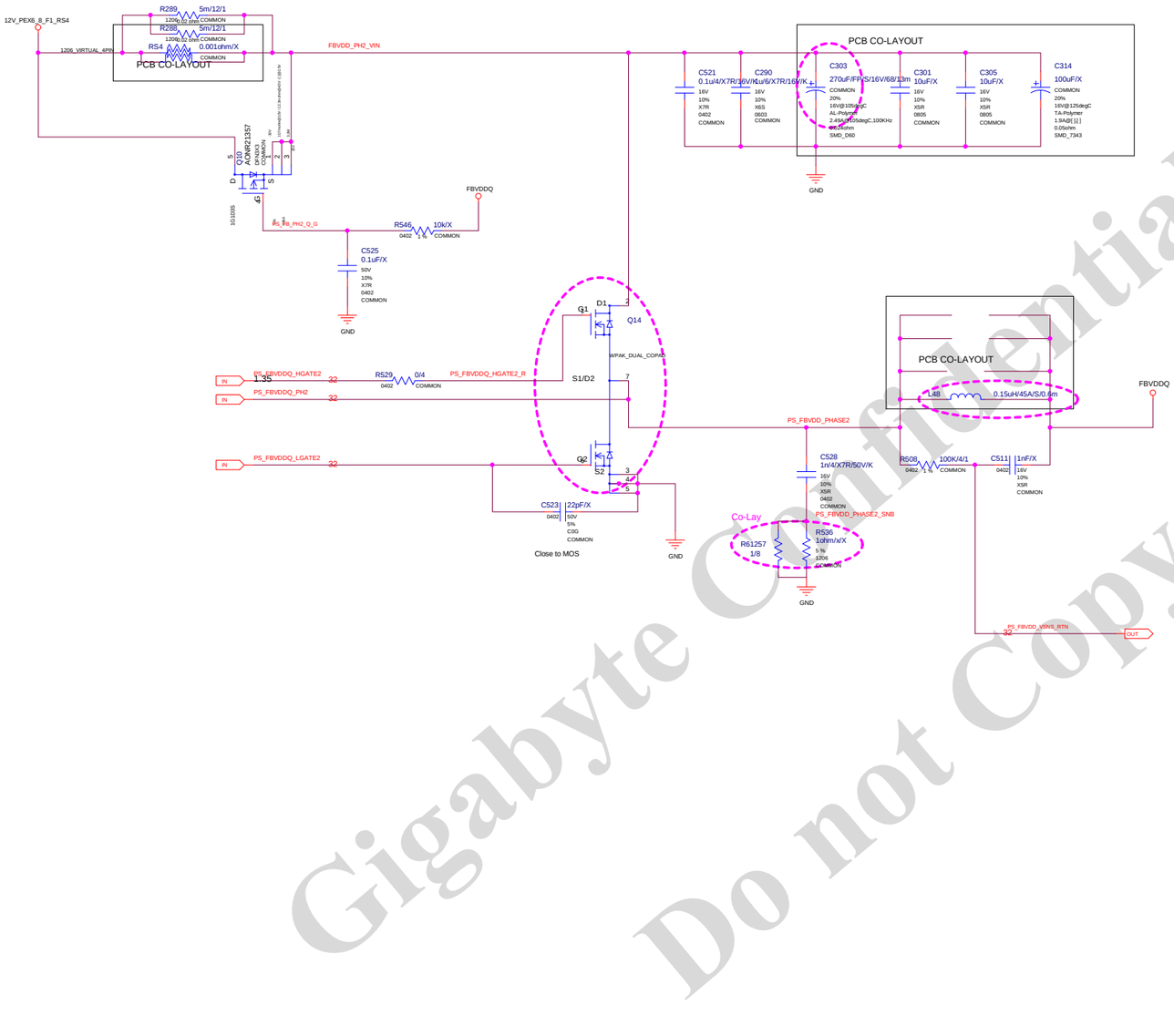
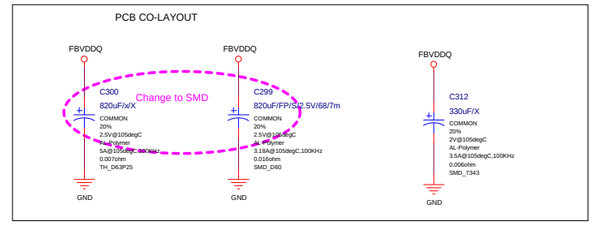
Page33: PS: FBVDDQ PH2

FBVDD PH2 INPUT ANTI-BACKDRIVE





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PAGE DETAIL P5: FBVDDQ PH2

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Page34: PS: NVVDD CTR

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD CNTL

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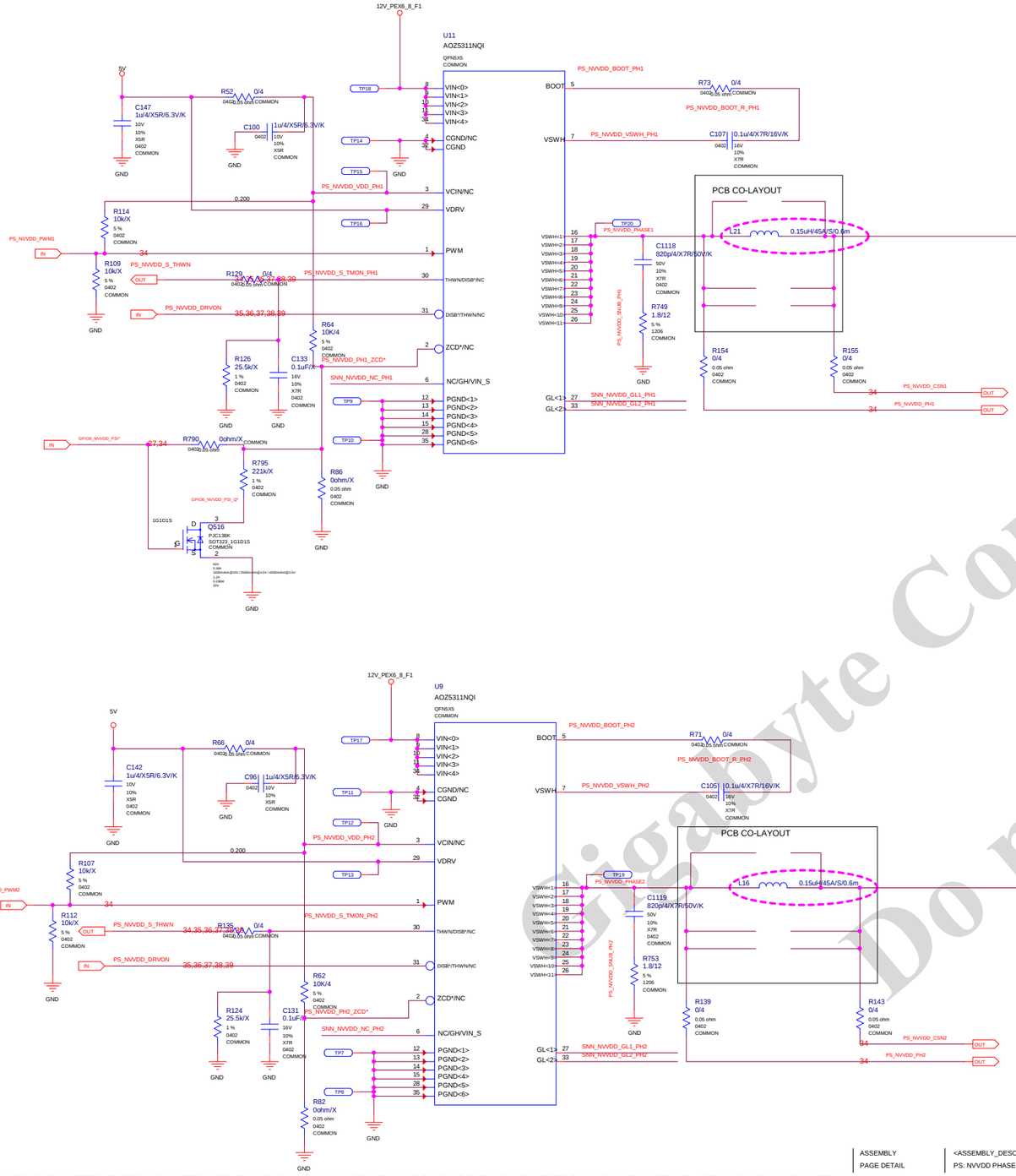
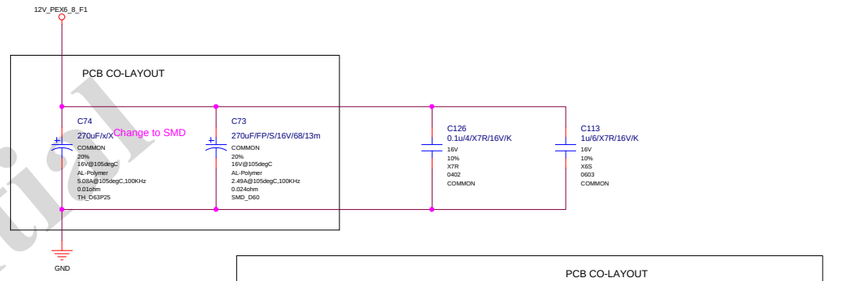
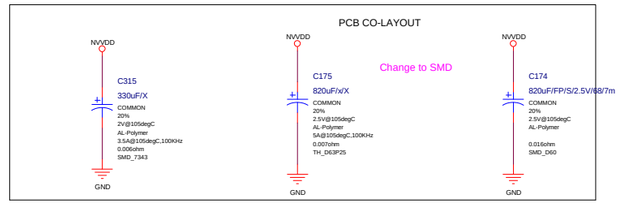
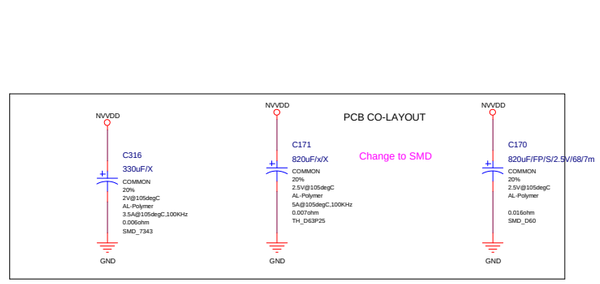
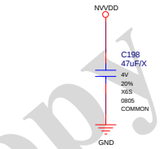
Page35: PS: NVVDD PH1 & 2

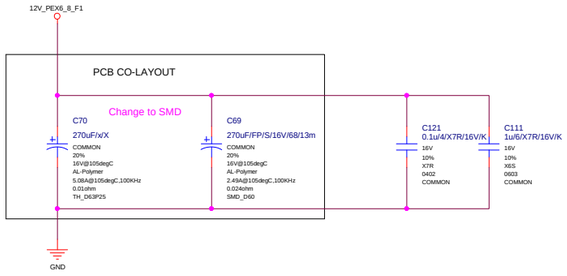












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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD PHASE 1 & 2

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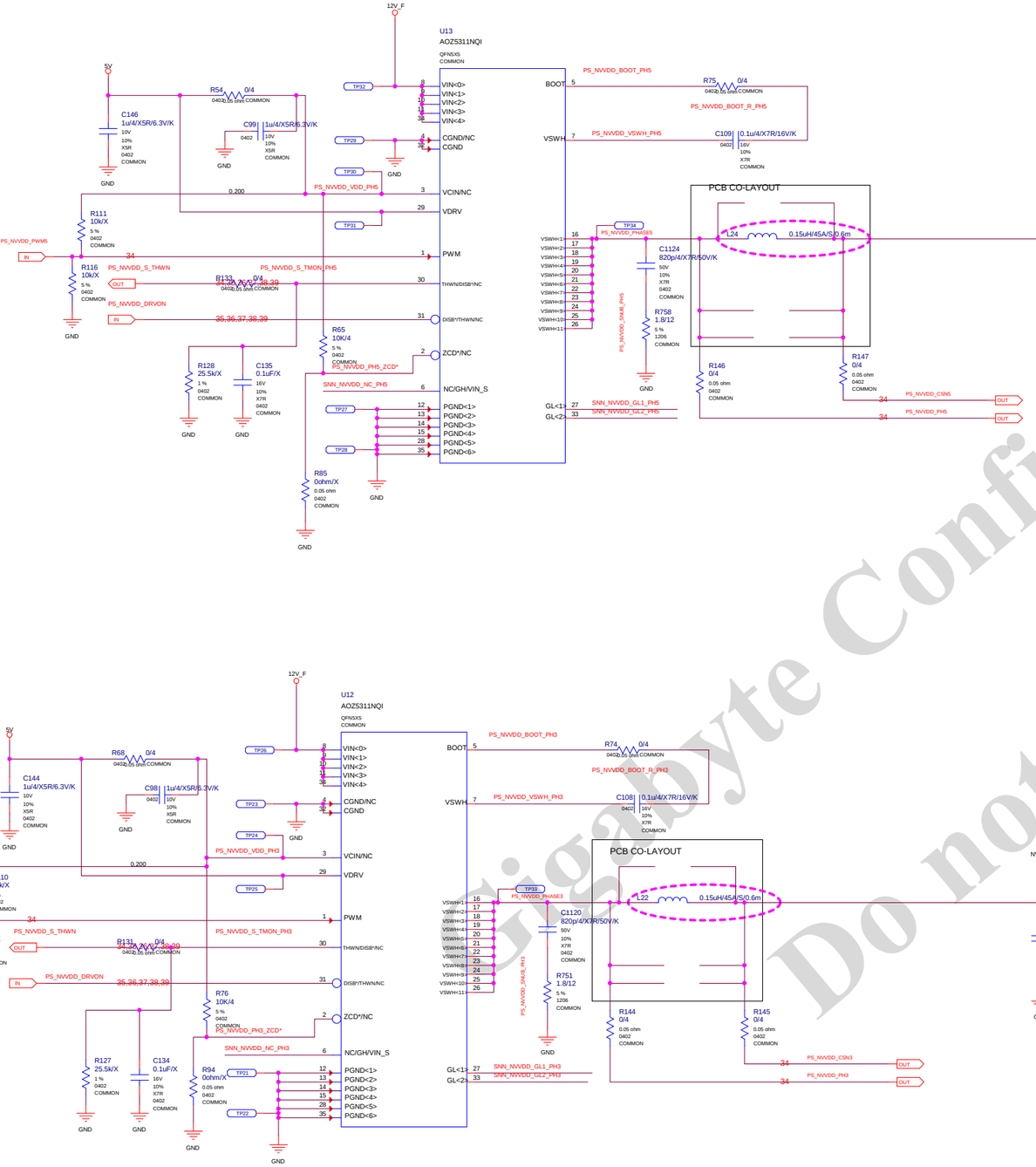
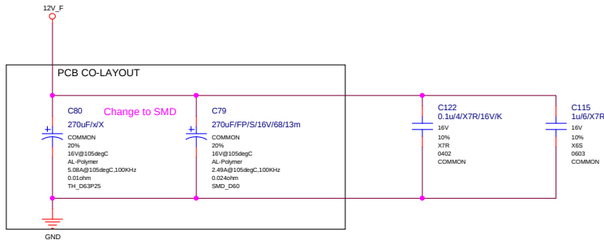
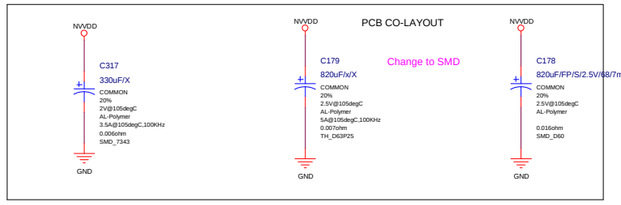
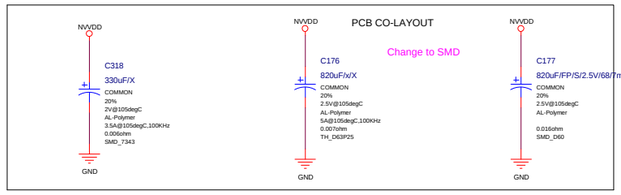
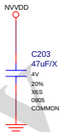
Page36: PS: NVVDD PH3 & 5

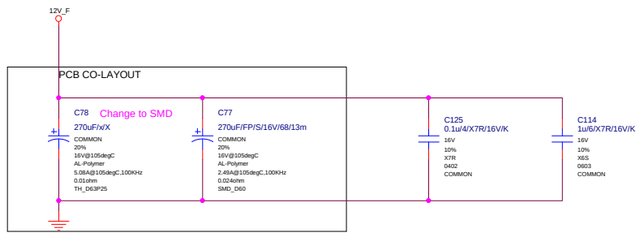












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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD PHASE 3 & 5

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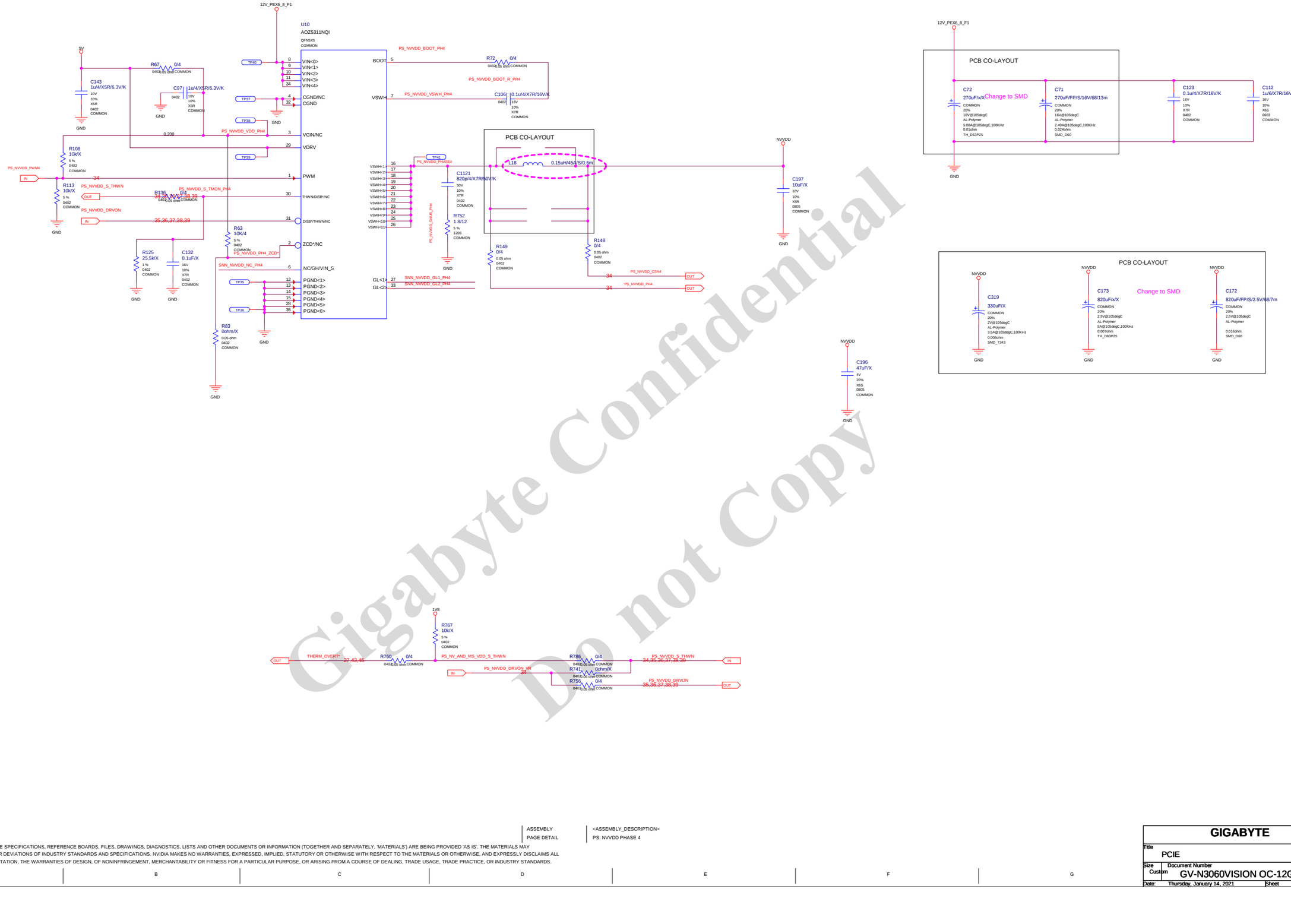
Page37: PS: NVVDD PH4



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: NVVDD PHASE 4

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Title: PCIE			
Size: Custom	Document Number: GV-N3060VISION OC-12GD		Rev: 1.01
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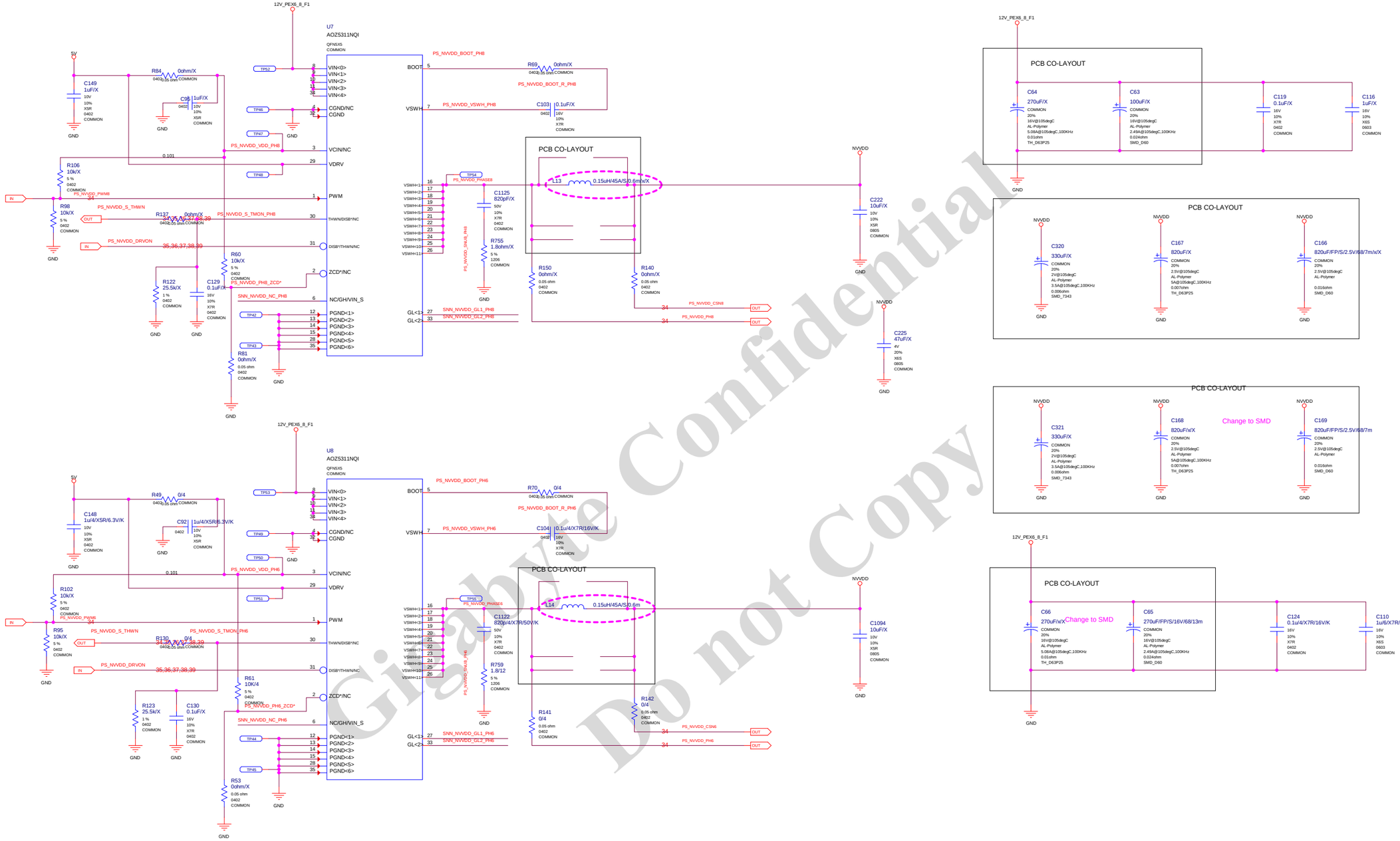
Page38: PS: NVVDD PH6 & 8



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD PHASE 6 & 8

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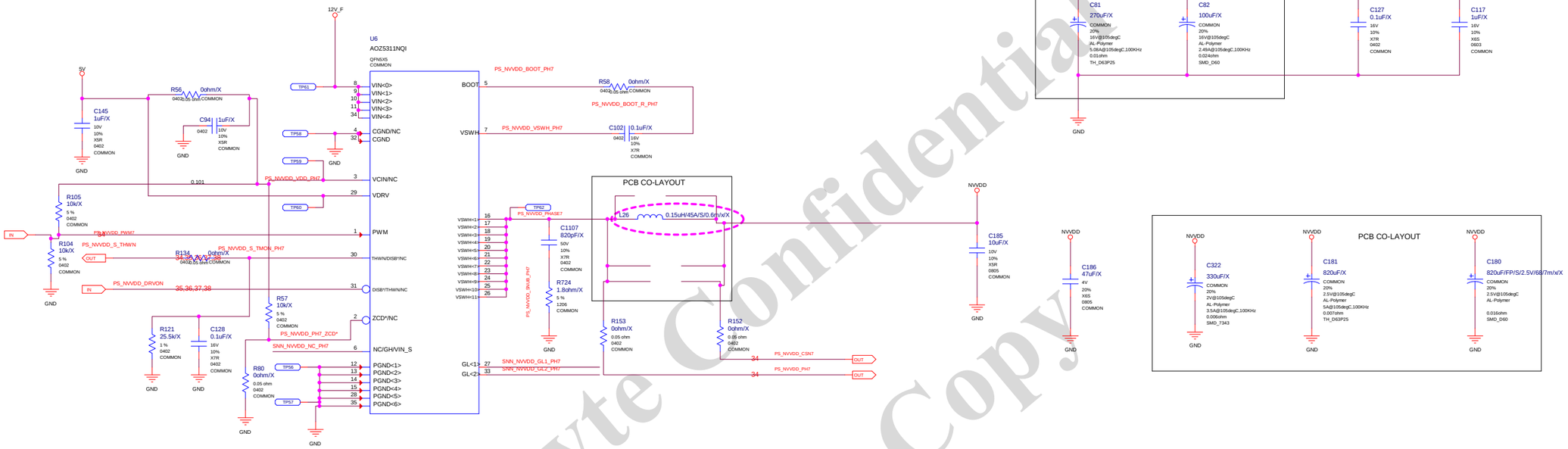
Page39: PS: NVVDD PH7



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PAGE DETAIL	PS: NVVDD PHASE 7

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GIGABYTE

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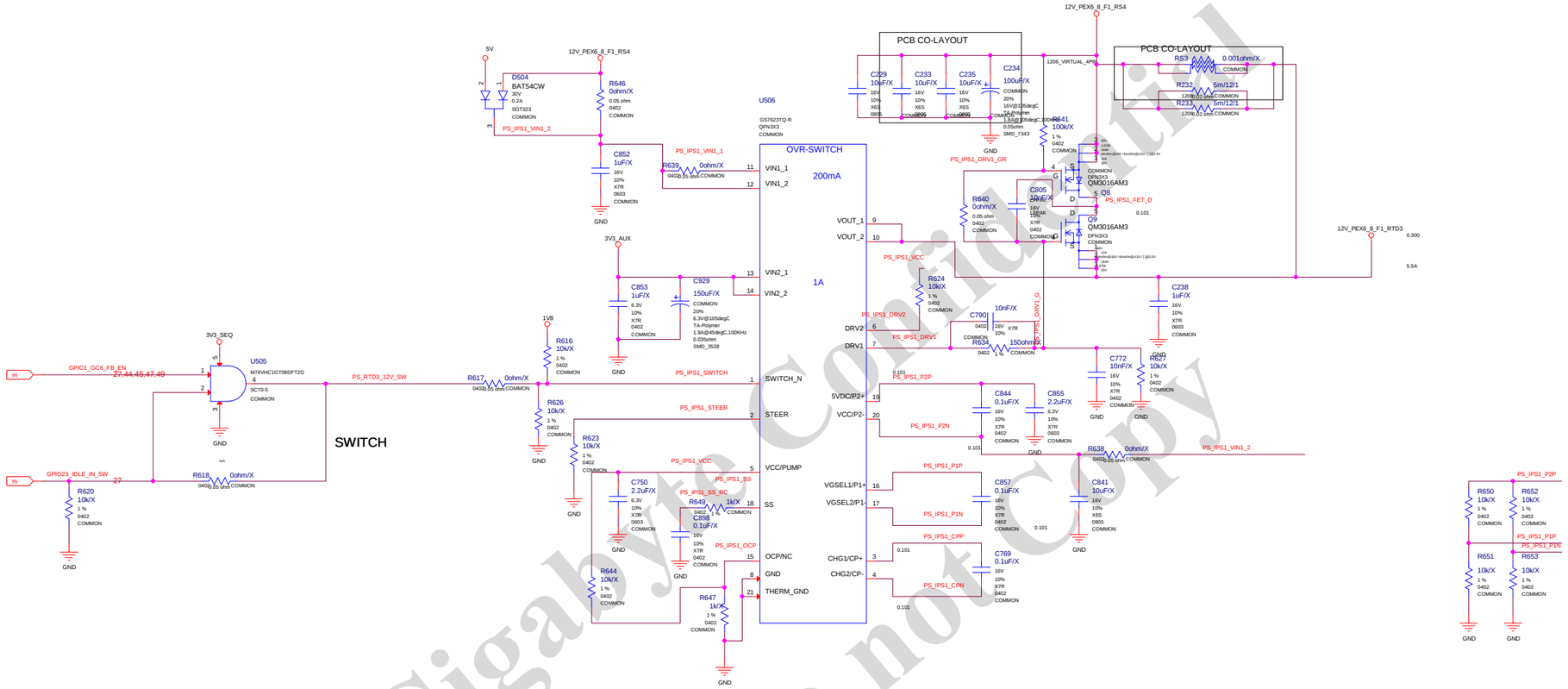
Page41: INPUT SWITCH RTD3 (12V & 3V3_A SWITCHER)

AND GATE LOGIC

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V
0	1	0	12V
1	0	0	12V
1	1	1	3V3A

SWITCH	VOUT
0	VOUT = VIN1
1	VOUT = VIN2



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL INPUT SWITCH RTD3

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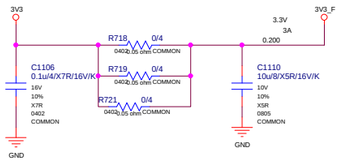
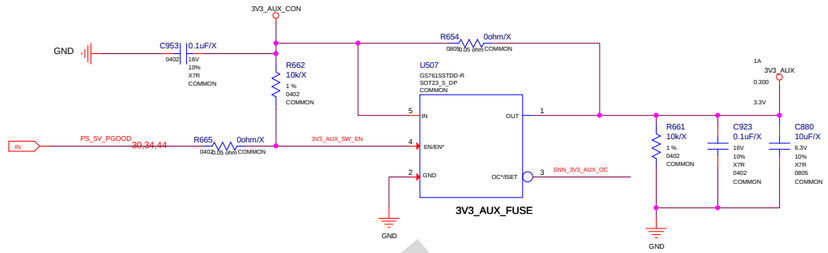
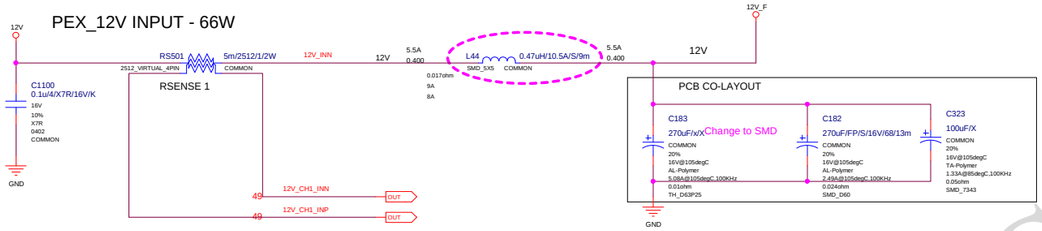
Page42: PEX_INPUT, 12V_EXT_INPUT, FILTERING

PEX 3V3 INPUT - 10W

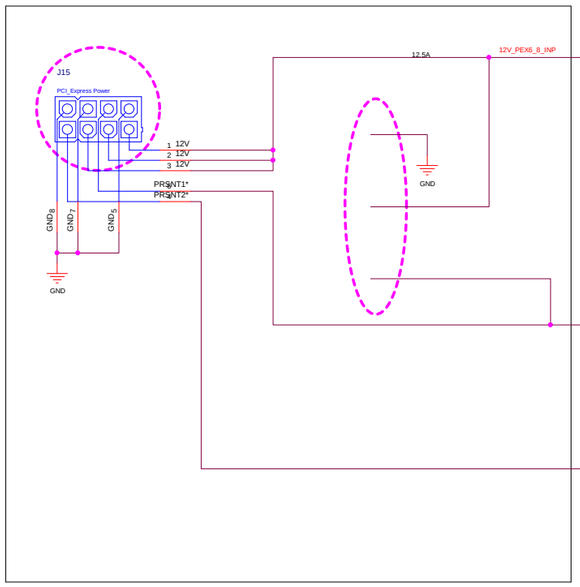


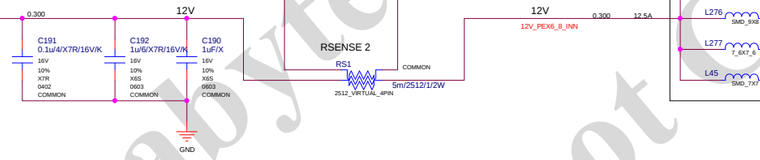


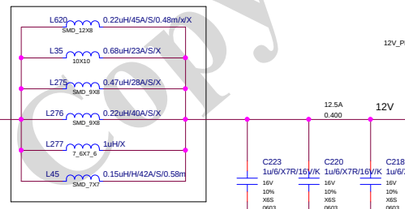
PEX_12V INPUT - 66W

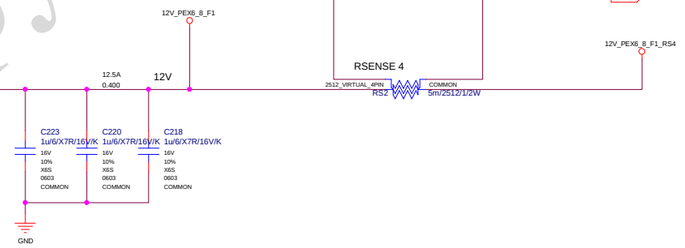


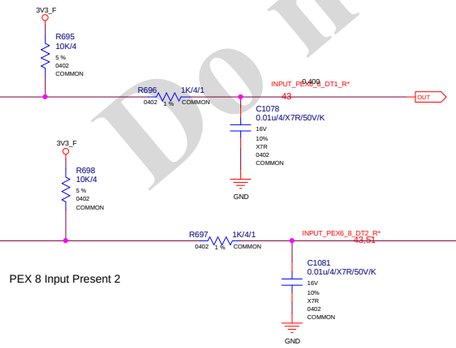
PEX8 INPUT 1 - 2x4 PCIE CON 150W

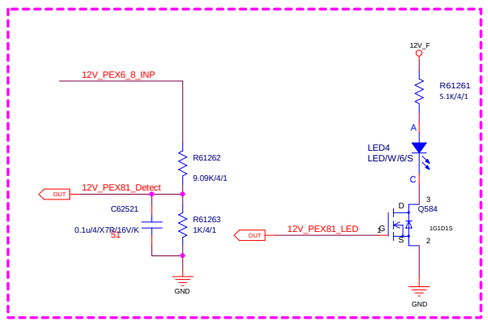












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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	INPUT POWER, FILTERING

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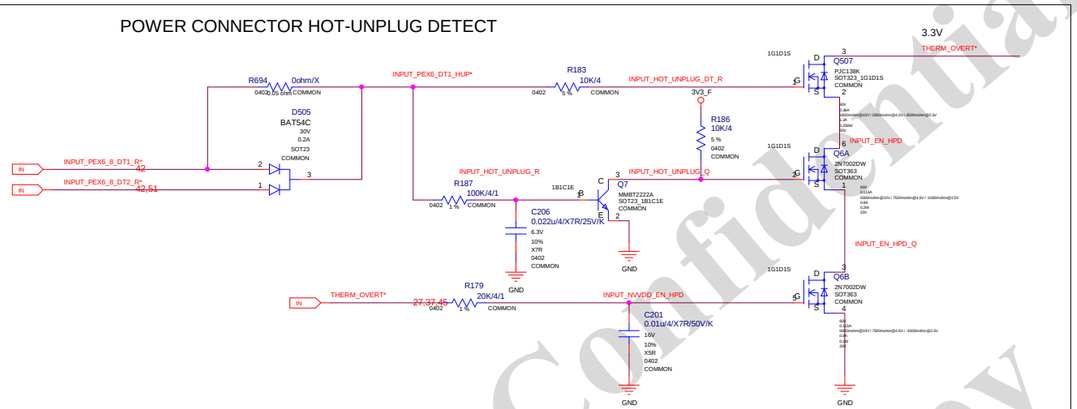
Page43: MISC: HOT UNPLUG

POWER CONNECTOR HOT-UNPLUG DETECT



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL MISC: Hot Unplug

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Title: PCIE

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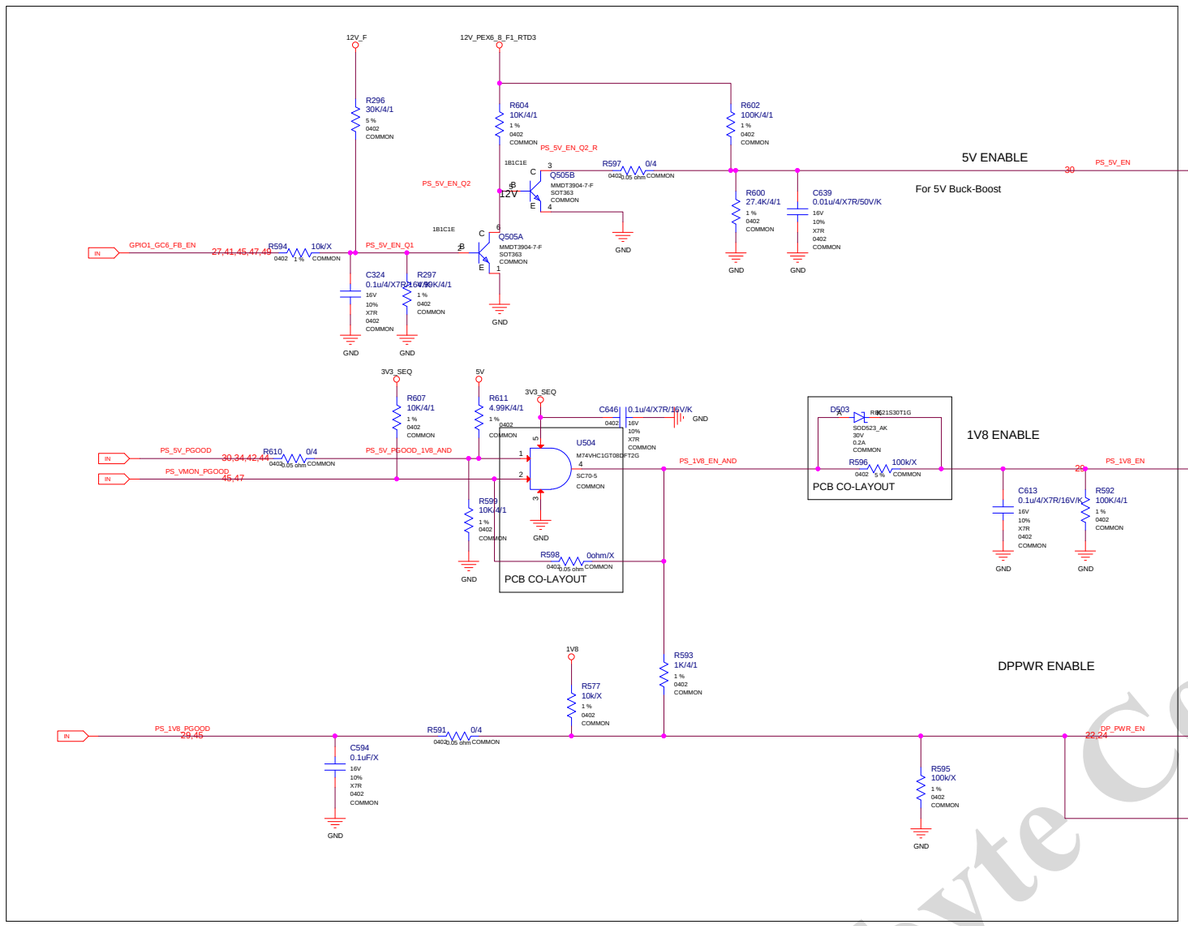
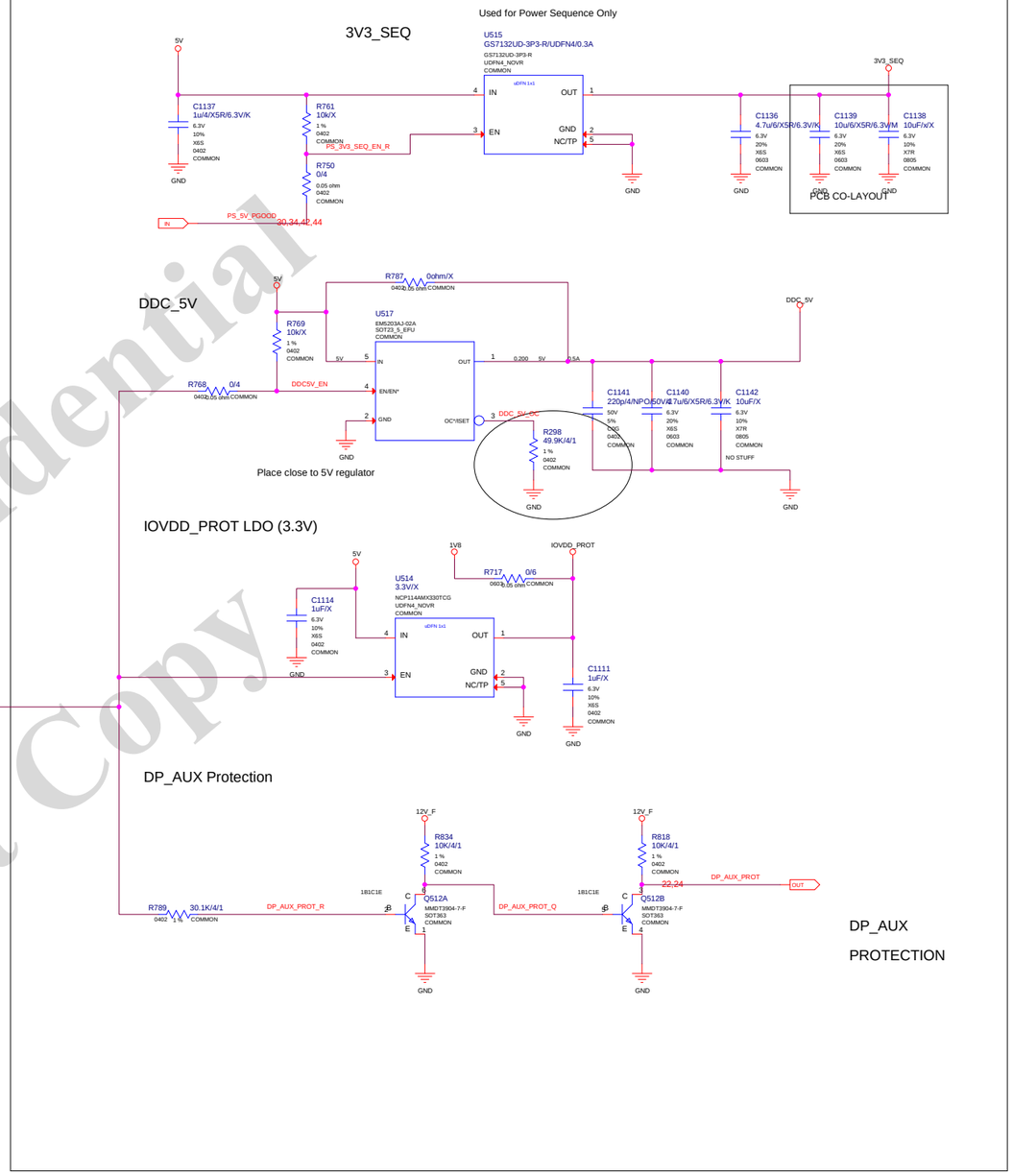
Page44: SEQ: 3V3_SEQ, DDC_5V, DP_AUX_PROT





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ASSEMBLY | <ASSEMBLY_DESCRIPTION>
PAGE DETAIL | SEQ: 3V3_SEQ,DDC_5V,DP_AUX_PROT

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Page45: SEQ:NVVDD, PEX, FBVDDQ ENABLE

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL SEQ: NVVDD, PEXVDD AND FBVDDQ ENABLE

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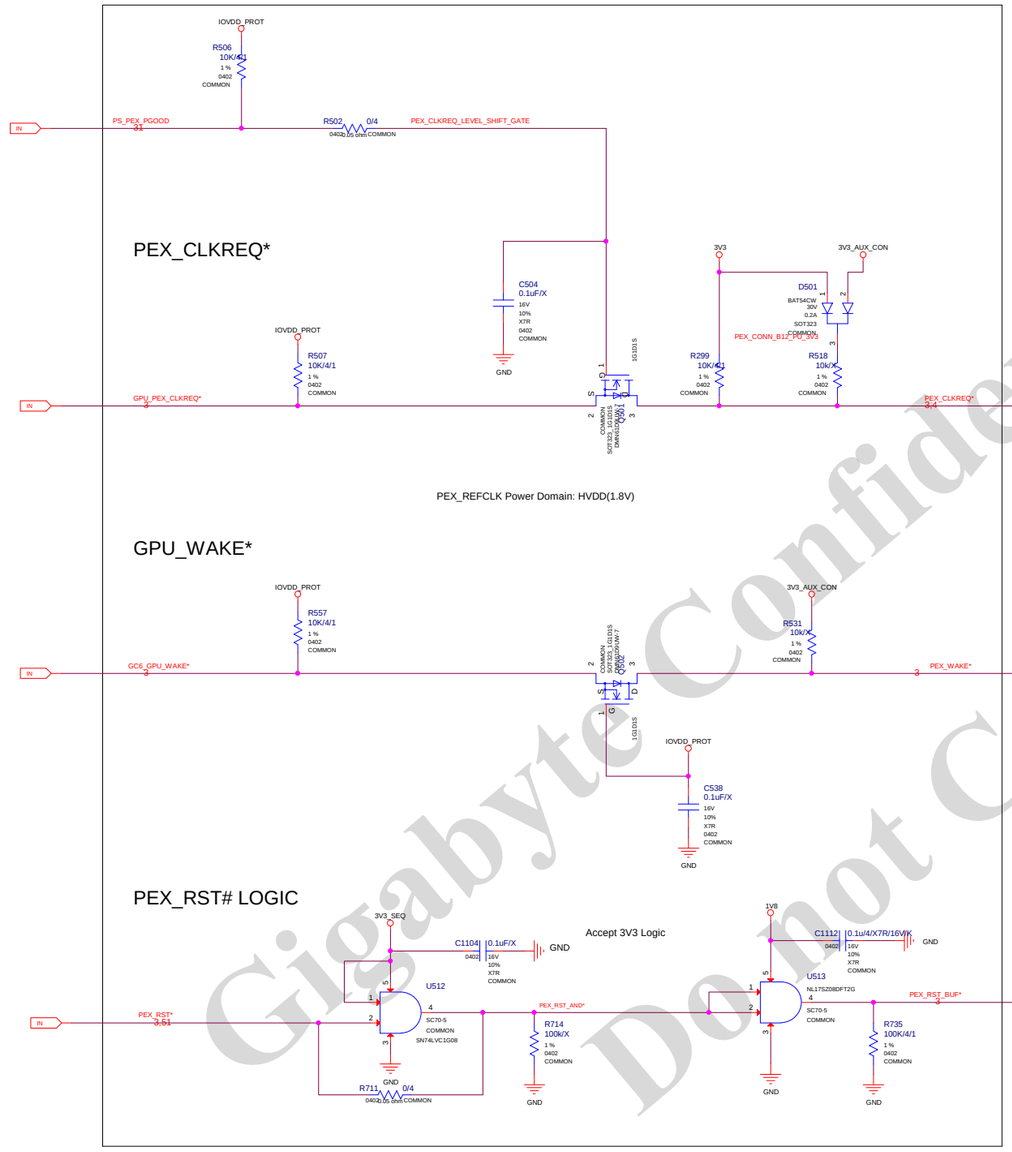
Page46: SEQ:MISC



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PAGE DETAIL | SEQ: MISC

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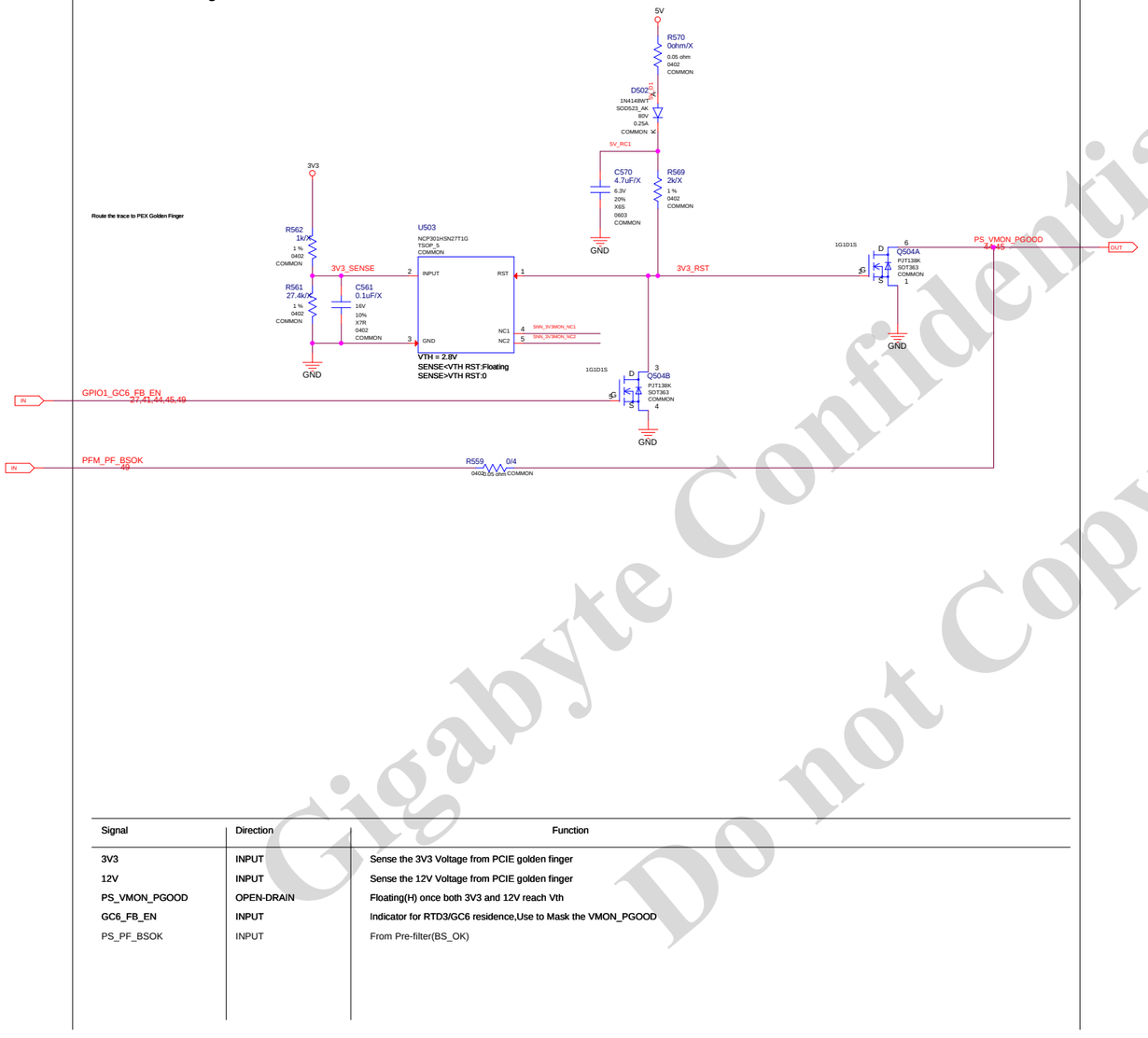
3V3PEX Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_BSOK	INPUT	From Pre-filter(BS_OK)

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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL SEQUENCE: VOLTAGE MONITOR

GIGABYTE

Title: PCIE

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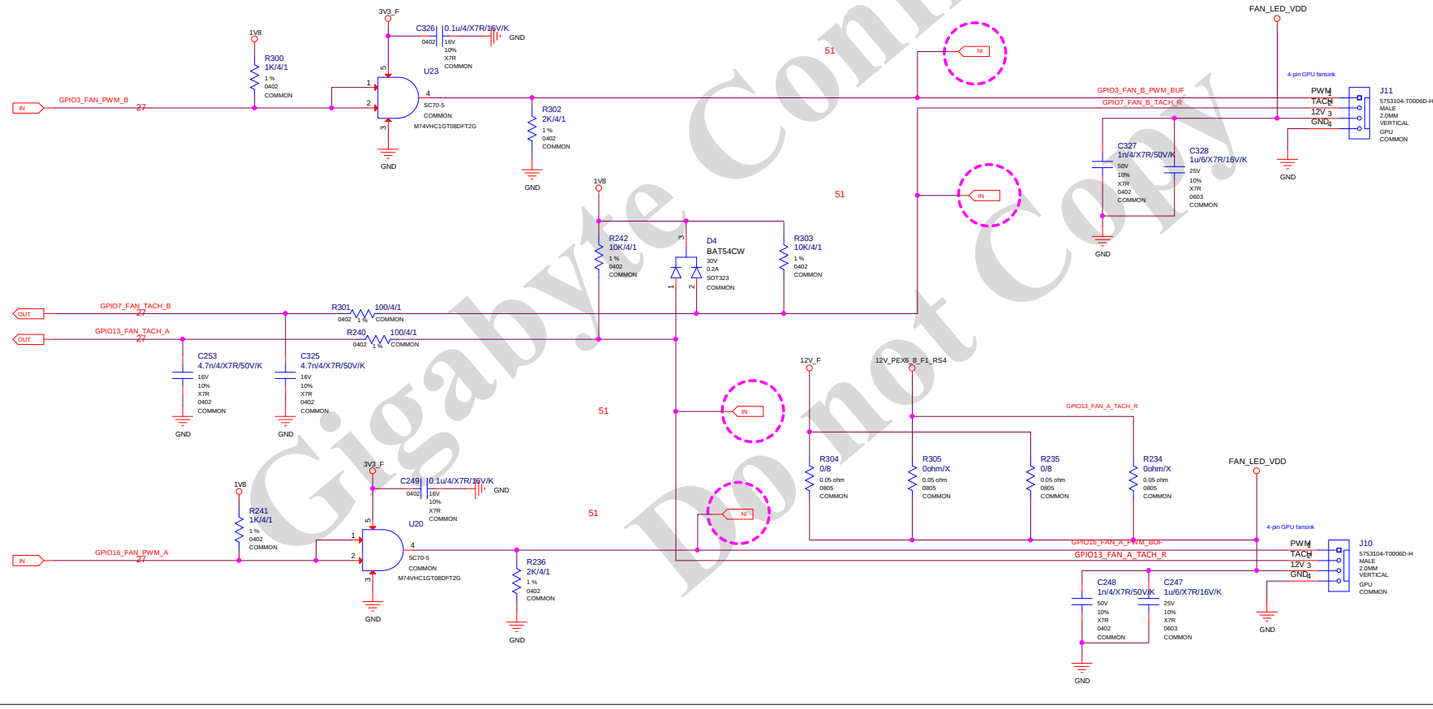
Page48: FAN & LED

2-PIN LED HEADER

Del 2 Pin LED

DUAL FAN 4-PIN HEADERS



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PAGE DETAIL	FAN & LED

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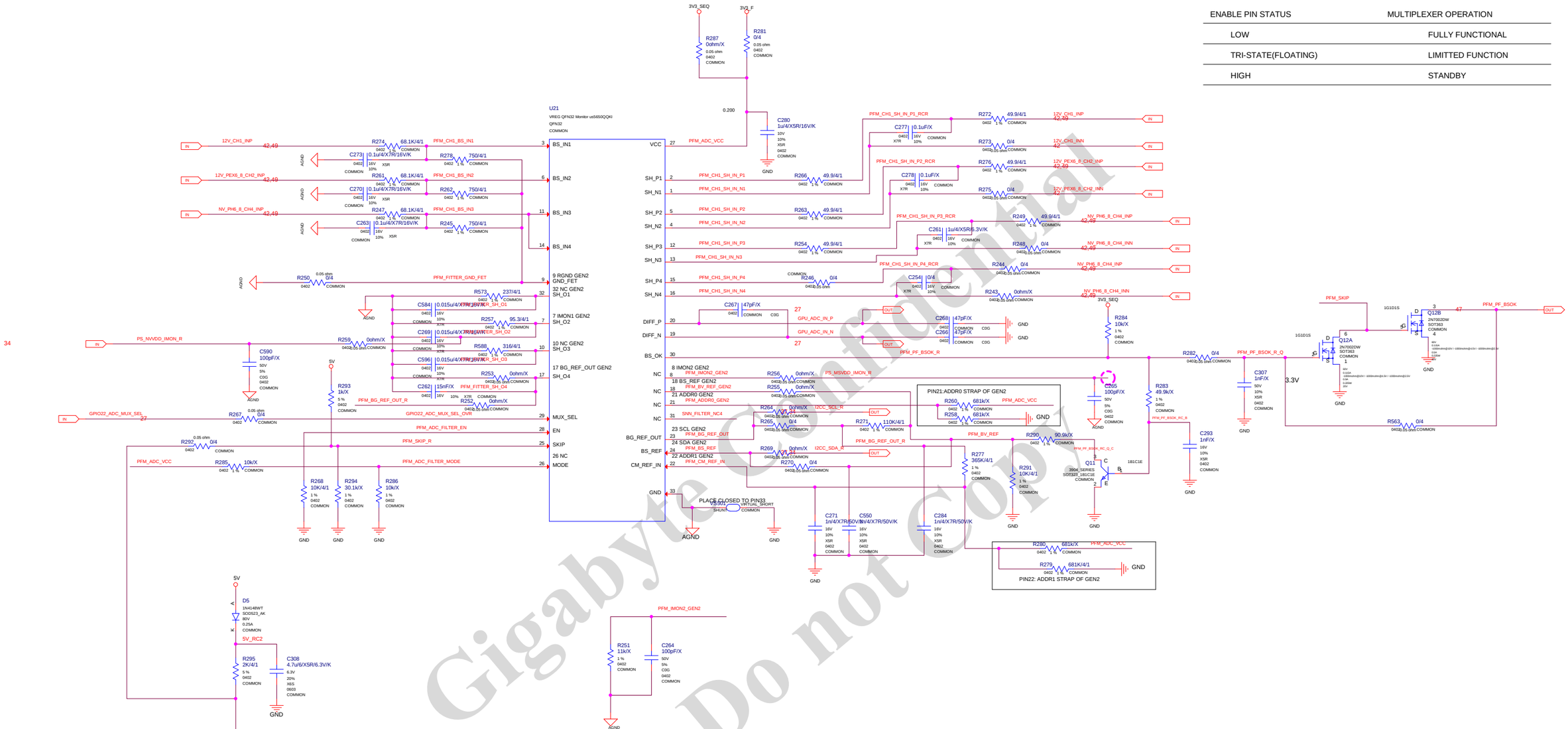
Page49: OVRM_PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	OVRM POWER SENSE

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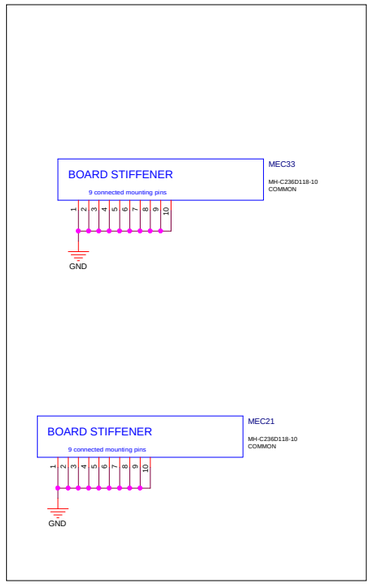
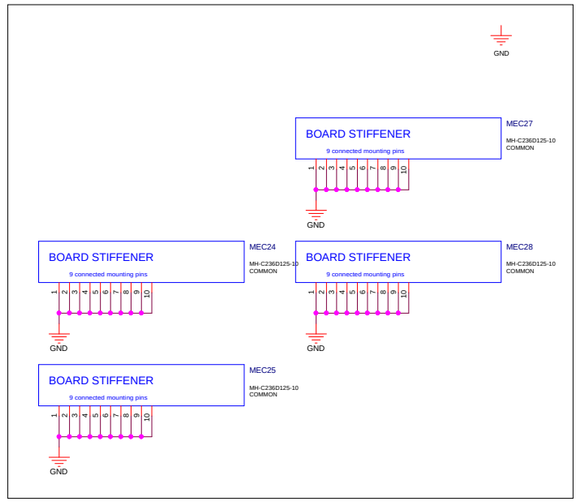
GIGABYTE

Page50: MECH

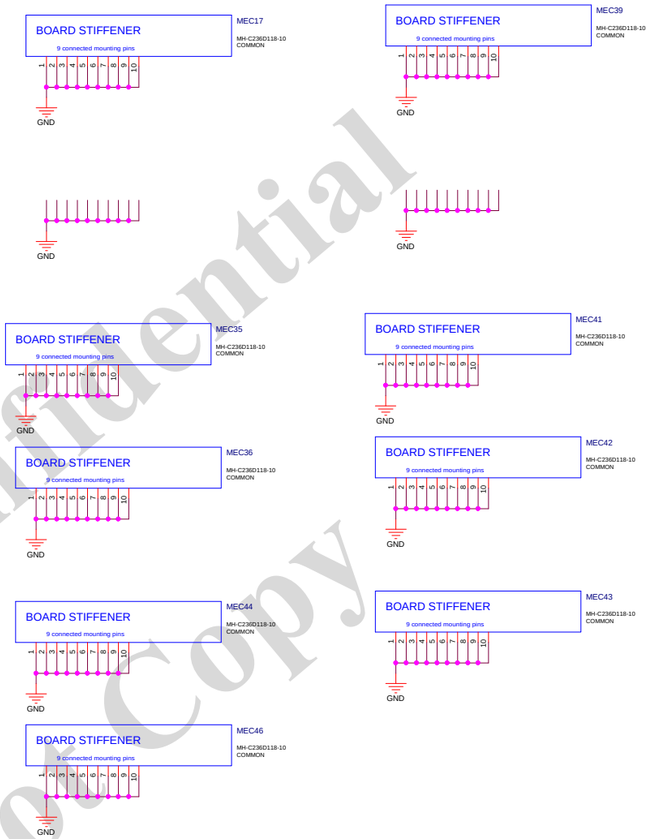
BKT SINK



GPU SINK



MOS
螺絲孔



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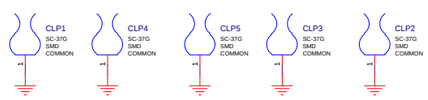

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH

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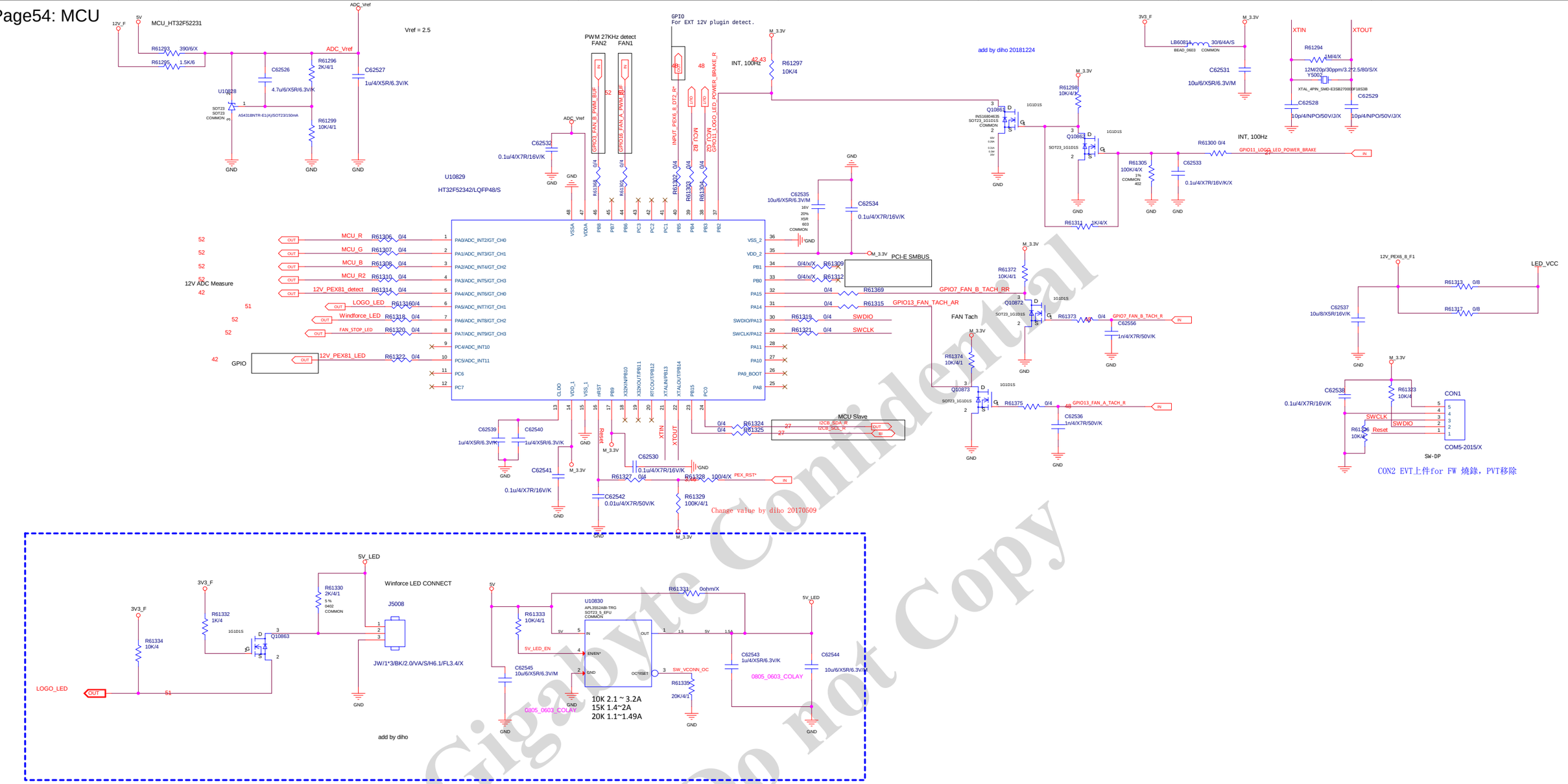
Page54: MCU



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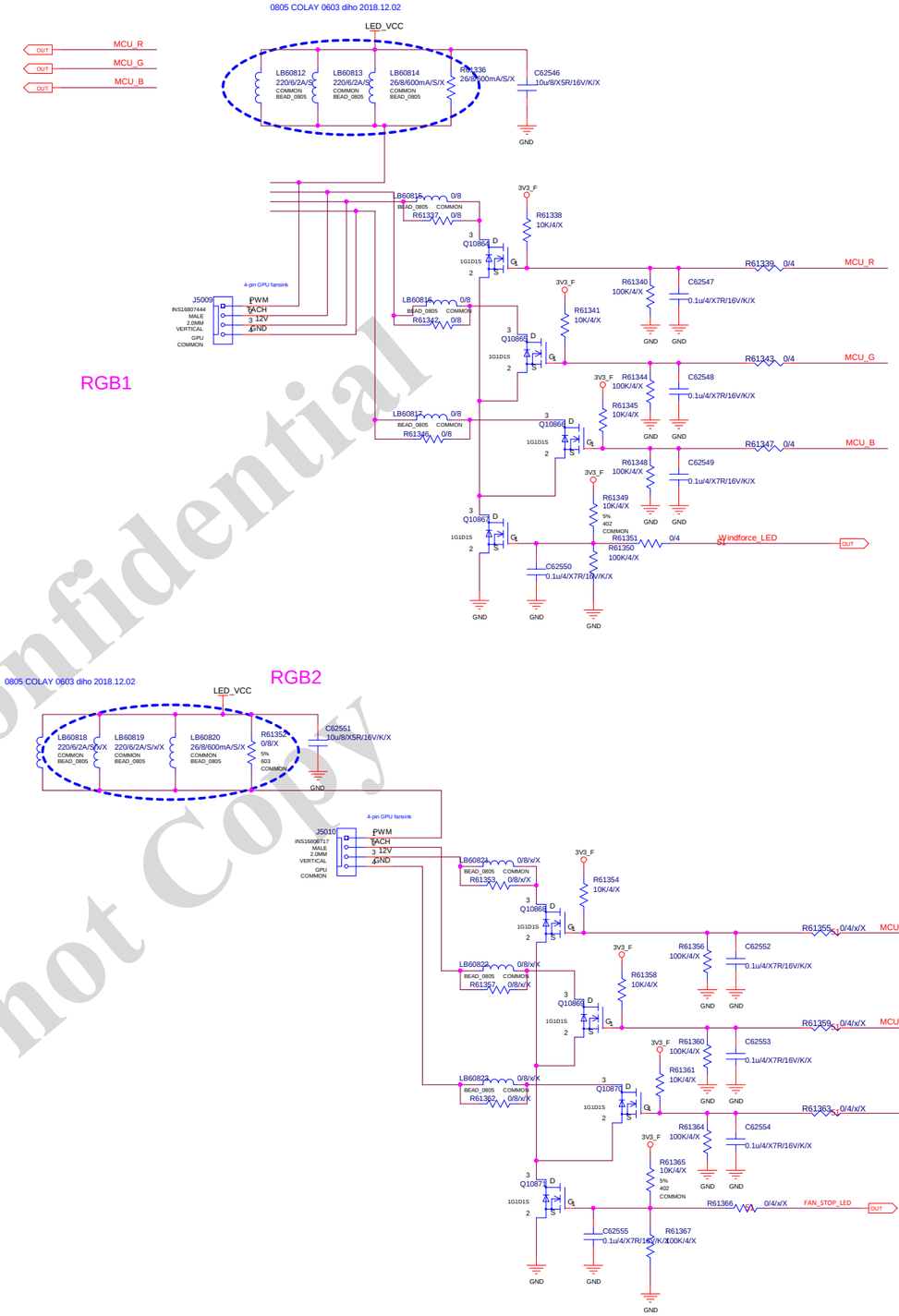

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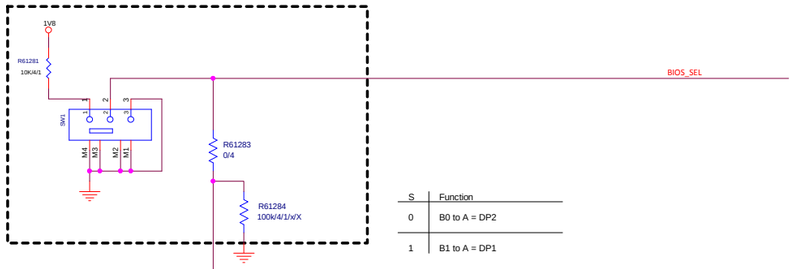
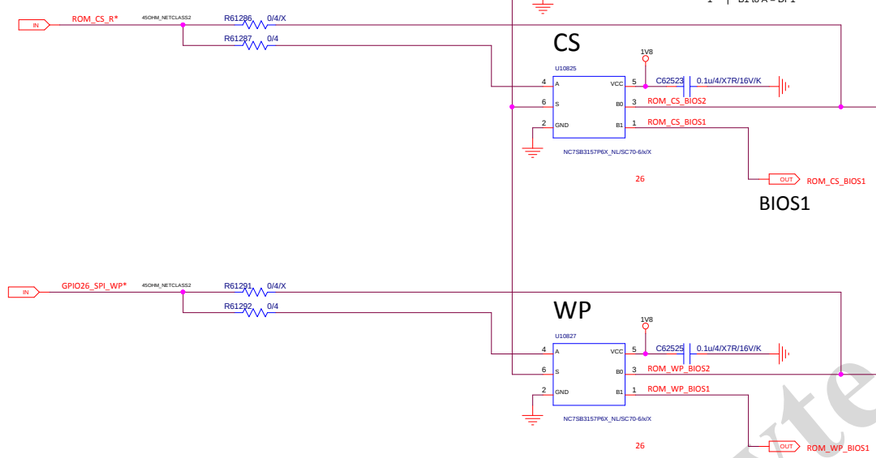
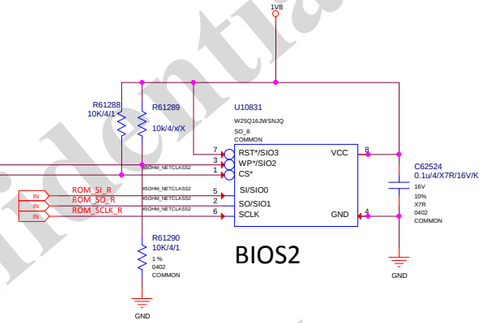
BIOS Switch

For Dual BIOS switch



S	Function
0	B0 to A = DP2
1	B1 to A = DP1





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History

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2020.08.06	First version

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