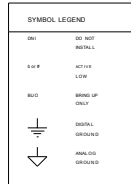
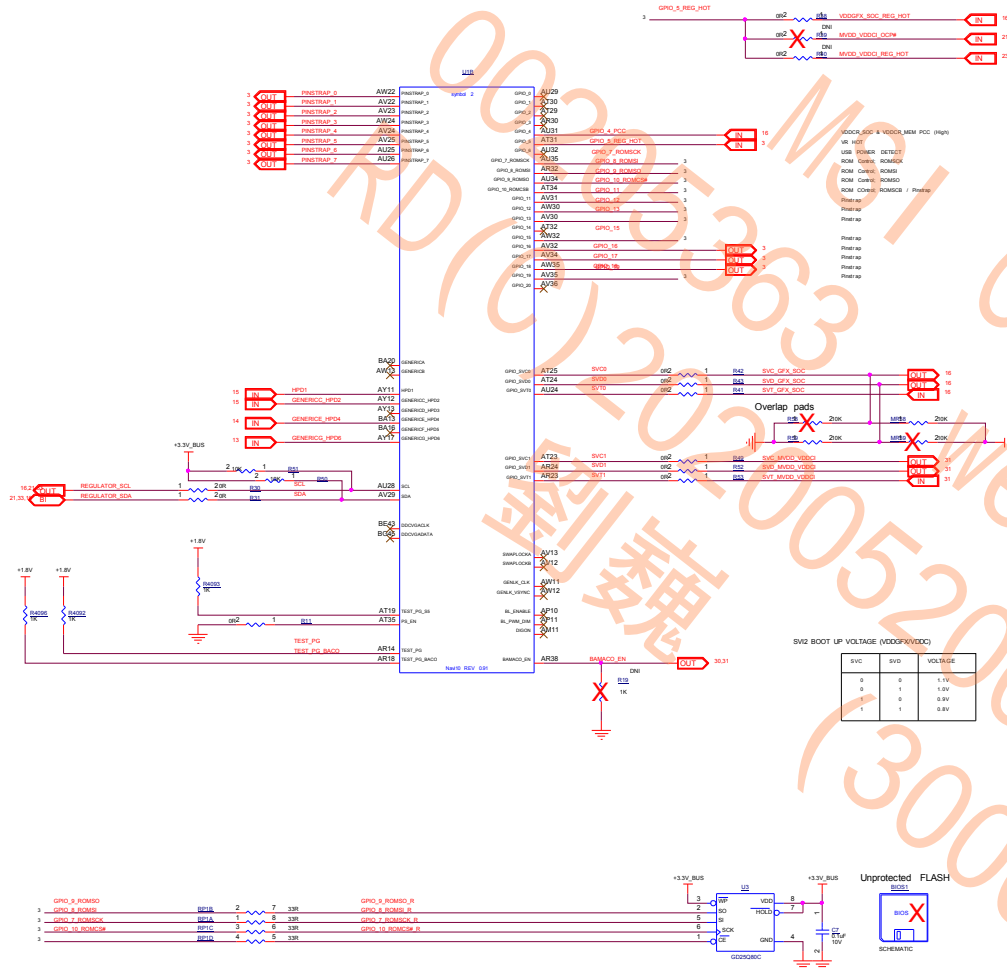


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SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
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4	NAV110 XTAL	29	NAV110 GND
5	NAV110 MEM CHAB	30	POWER MANAGEMENT
6	NAV110 MEM CHCD	31	SVR2 & BAMACO
7	NAV110 MEM CHEF	32	MECHANICAL & THERMAL
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21	MVDD_VDDCI CONTROLLER		
22	REG MVDD		
23	REG VDDCI		
24	REG 0.75V		
25	REG 1.8V		

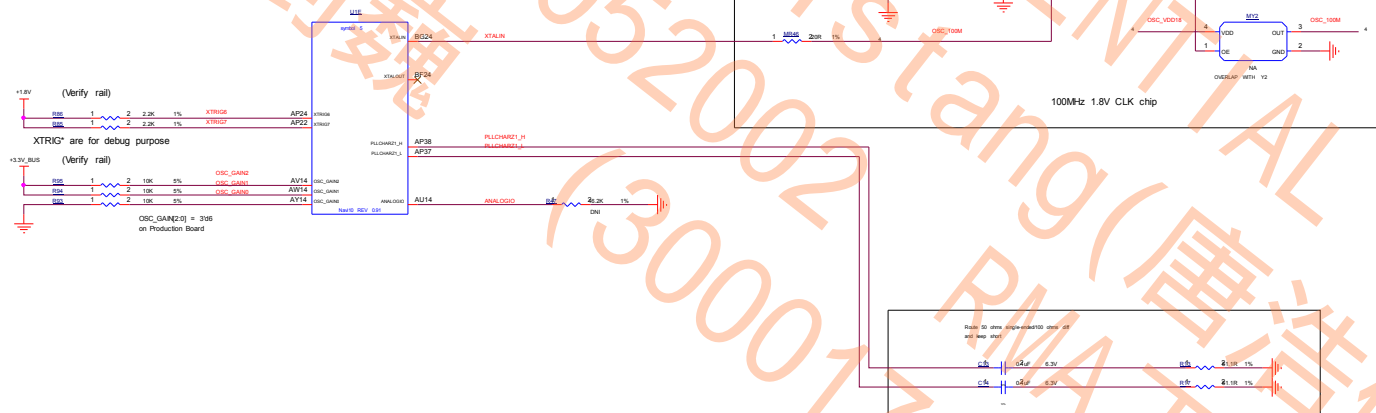
PLACE THESE CAPS AS CLOSE TO
THE COLLARED END AS POSSIBLE.

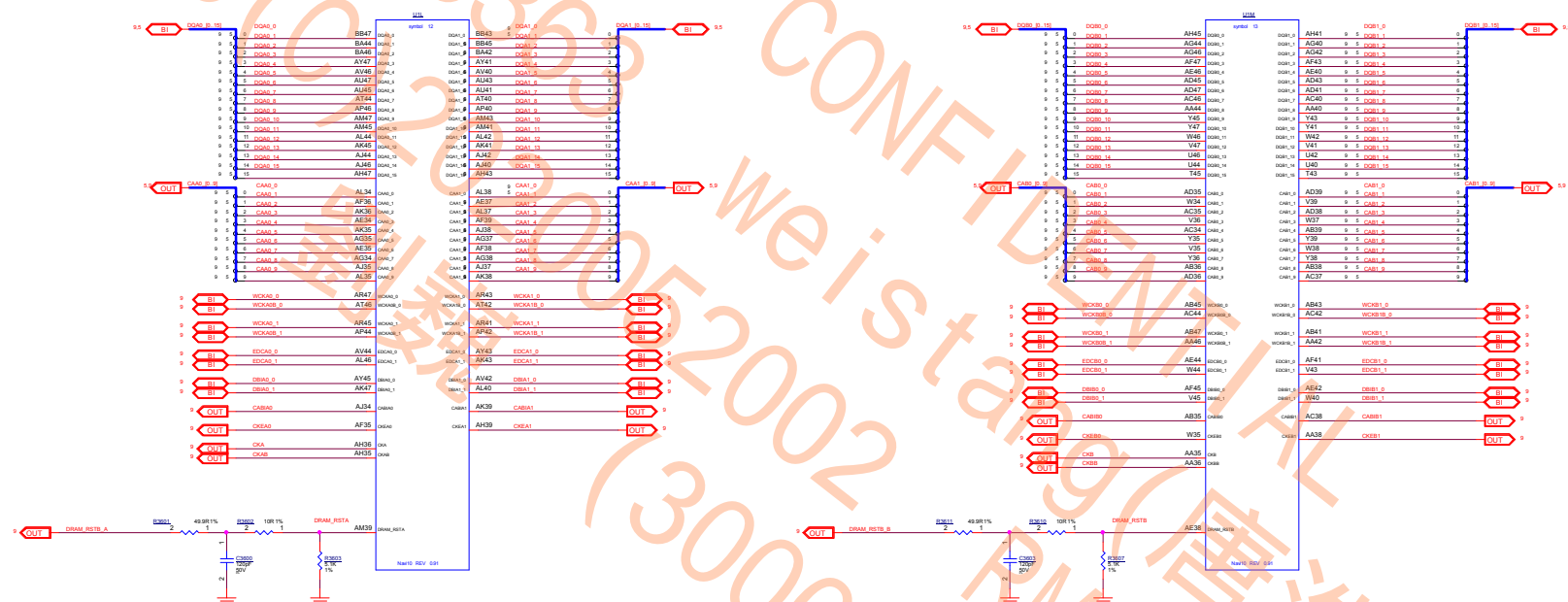


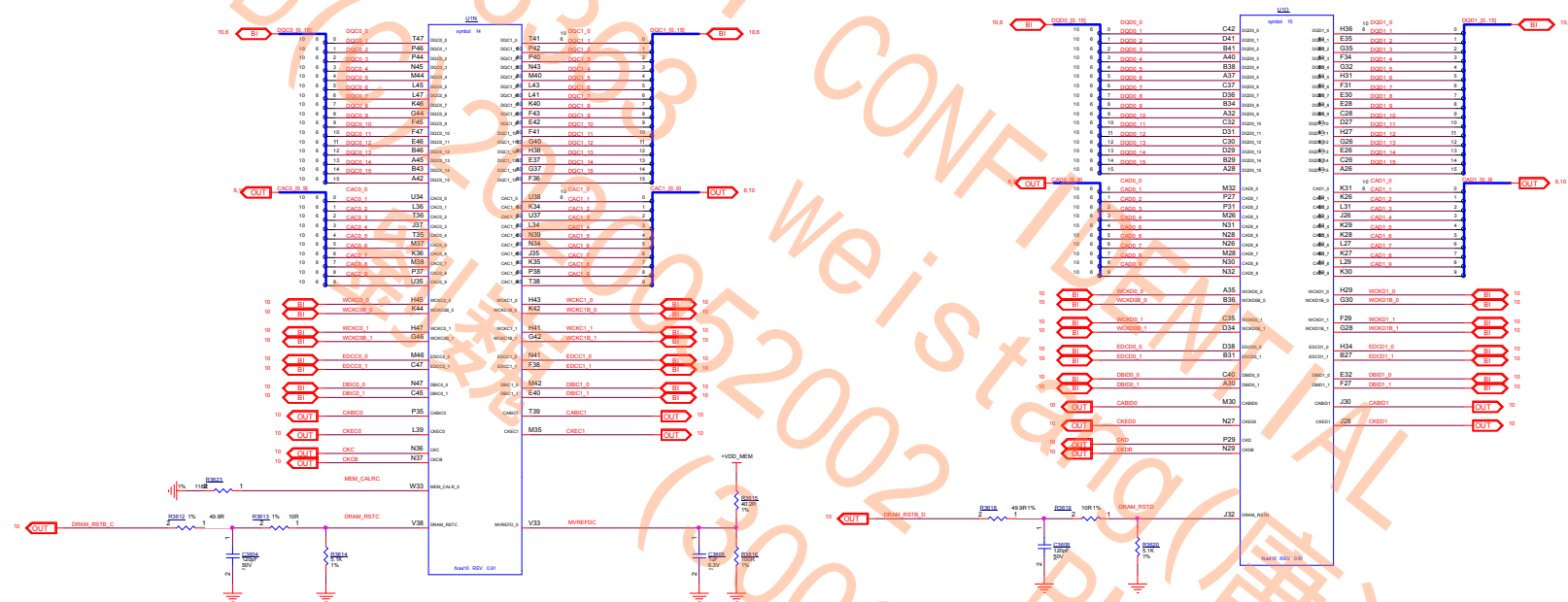


Note: Internal PUPD at GPIO pad is ~40k strength in 14nm design spec

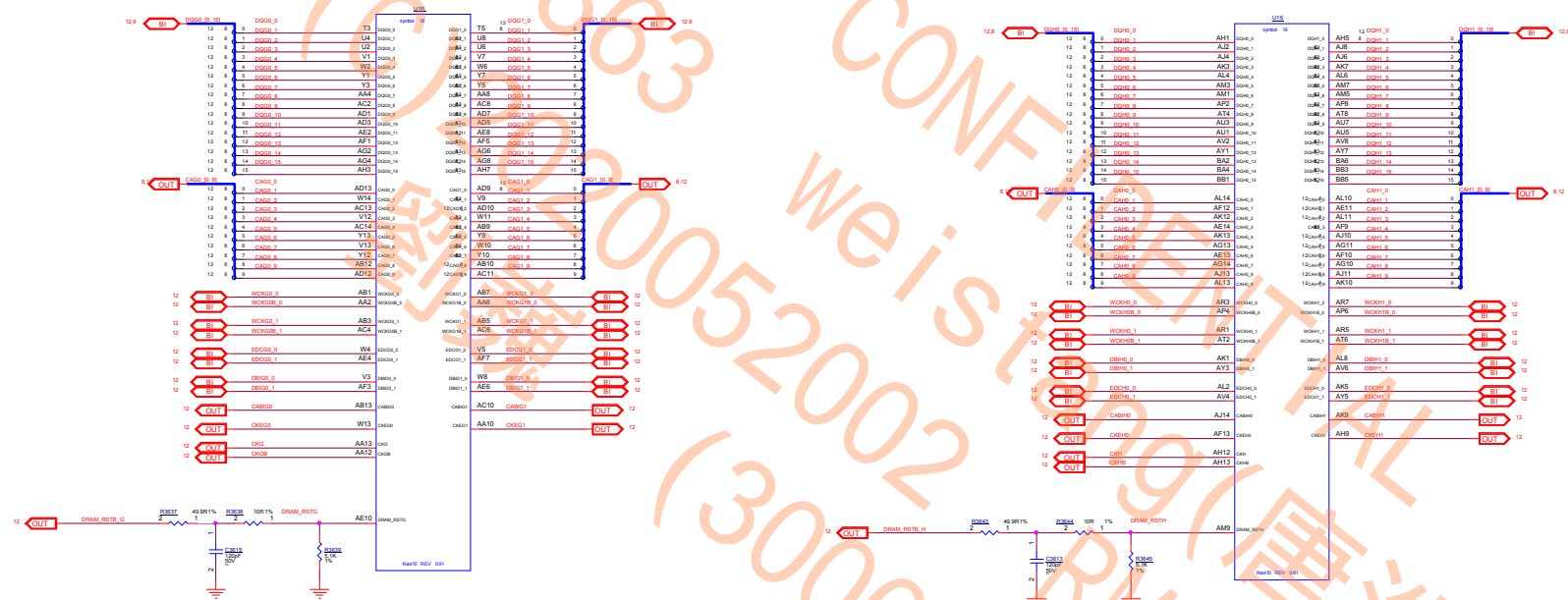
User	Internal Default Value	Definition
BIF	0	STRAP_BIF_GEN4_DIS_A 0: PCIe Gen4 supported 1: PCIe Gen4 not supported
	0	PINSTRAP_BIF_CLK_PM_EN 0: CLKSTOP power management capability is disabled 1: CLKSTOP power management capability is enabled
	0	PINSTRAP_BIF_IC_TX_SWING 0: VIOA receiver capability is enabled 1: The device will be equipped on the system's VGA controller
DCE	0	PINSTRAP_BIF_VGA_DIS 0: VGA receiver capability is enabled 1: The device will be equipped on the system's VGA controller
	0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected 4: 4 endpoints connected
	0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if design is selected 3: Audio for DisplayPort and native HDMI
Platform	0	GPIO_16
	0	GPIO_17
	0	GPIO_18
SMU	1	PINSTRAP_2
	0	PINSTRAP_1
	1	PINSTRAP_0
SMU	0	GPIO_16
	0	GPIO_17
	1	GPIO_18
SMU	0	PINSTRAP_SMBUS_ADDR 0: 0x40 1: 0x41
	1	PINSTRAP_BIOS_ROM_EN 0: Enable the external BIOS ROM device 1: Enable the internal BIOS ROM device

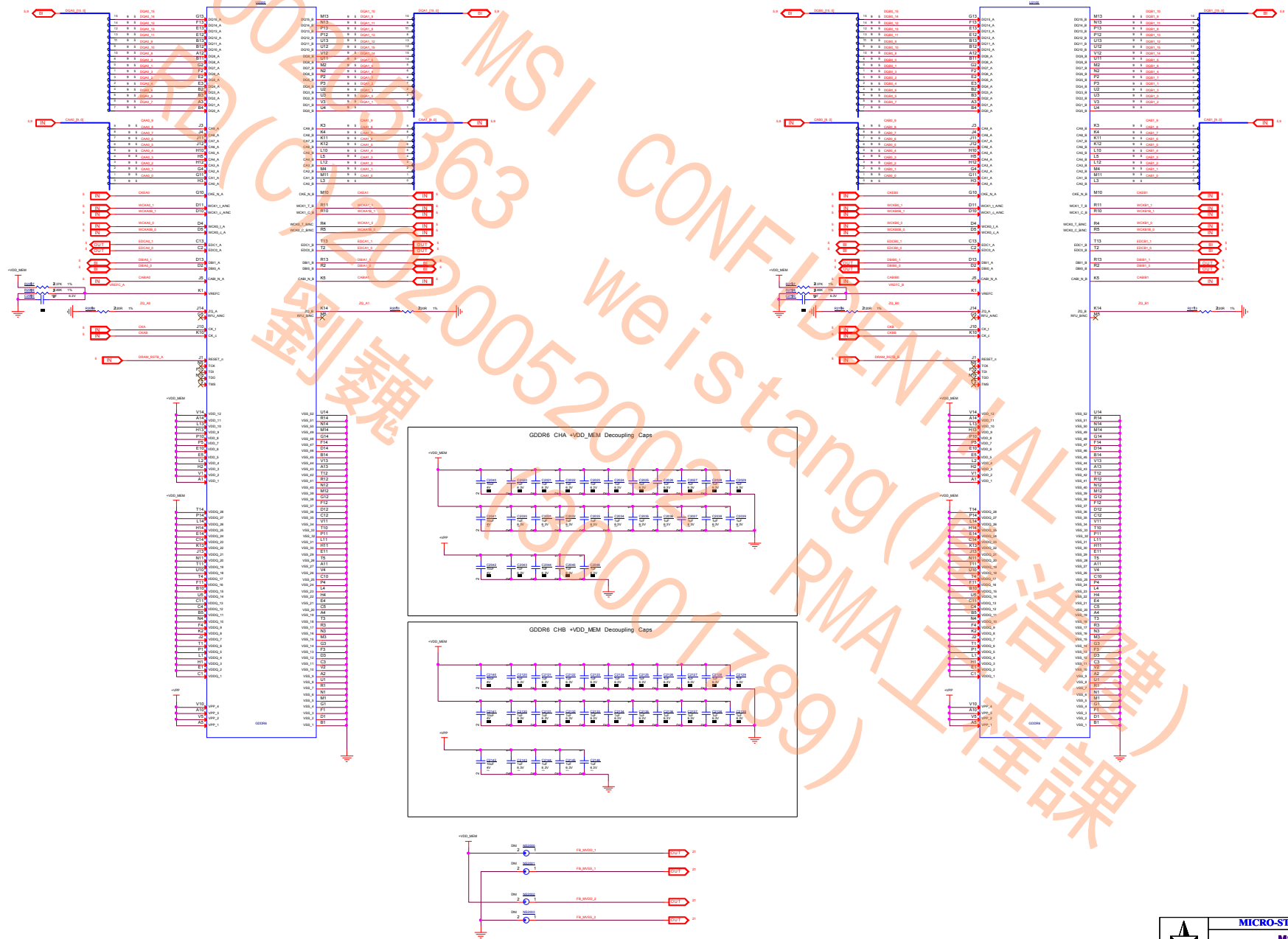


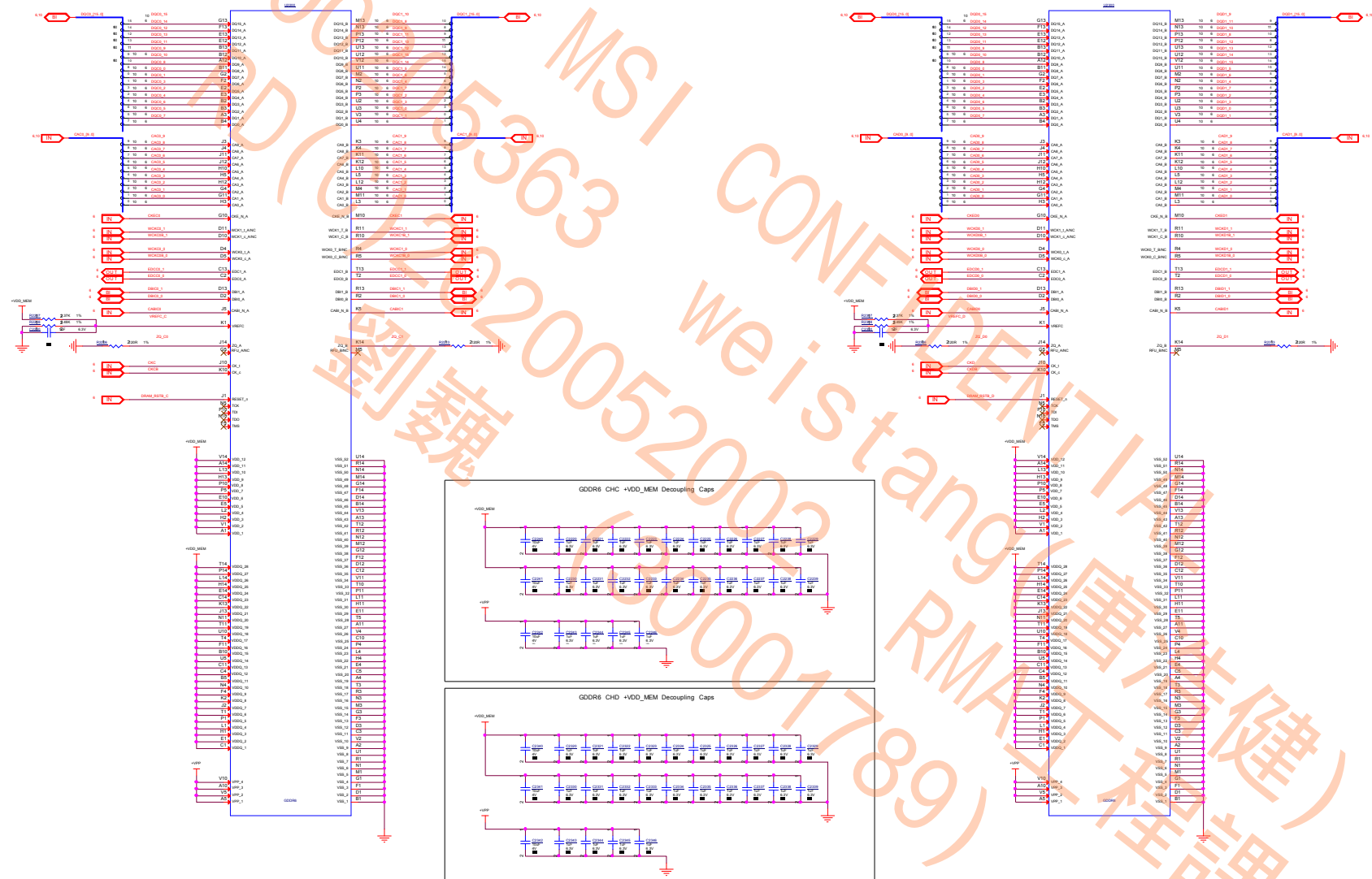


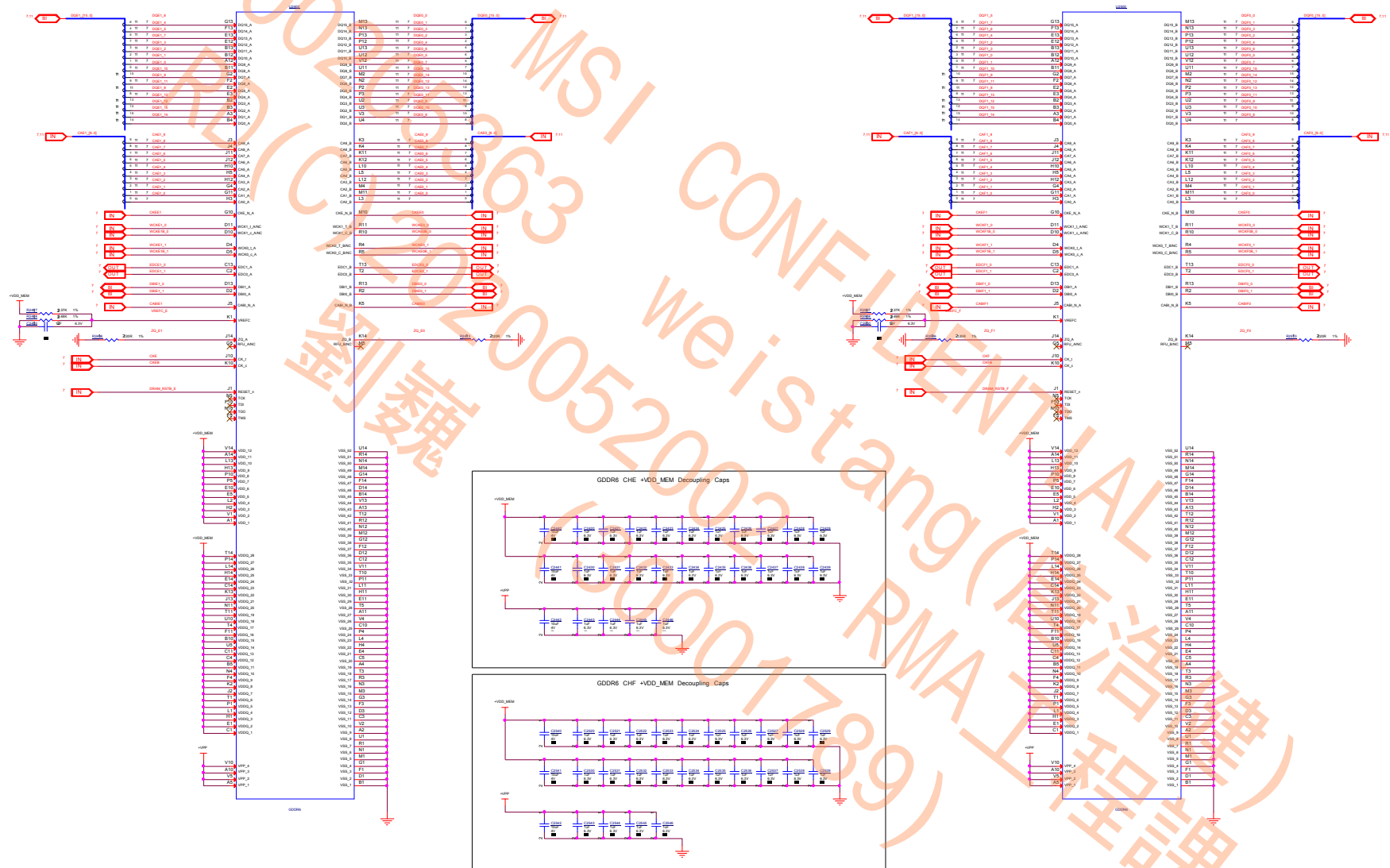


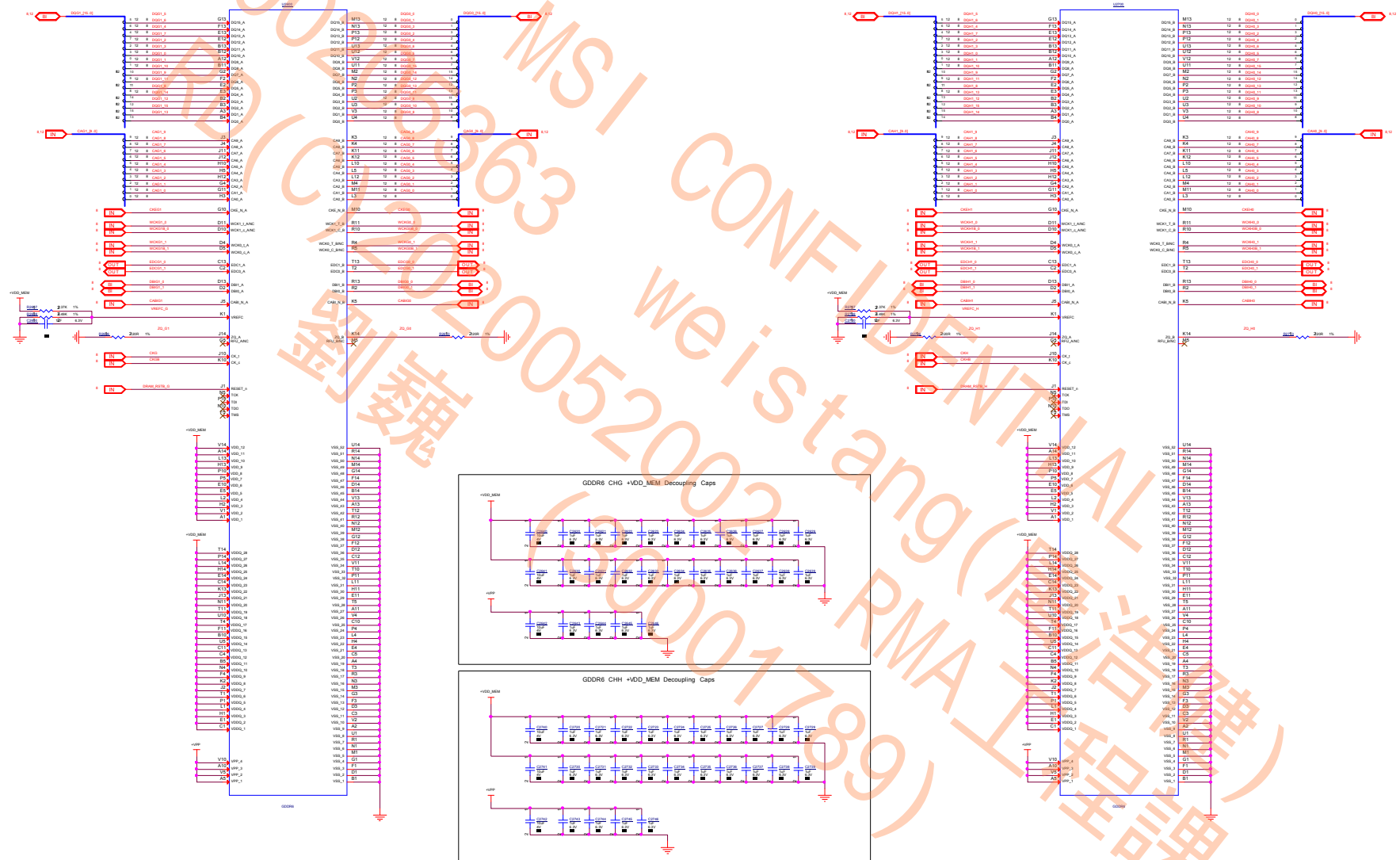


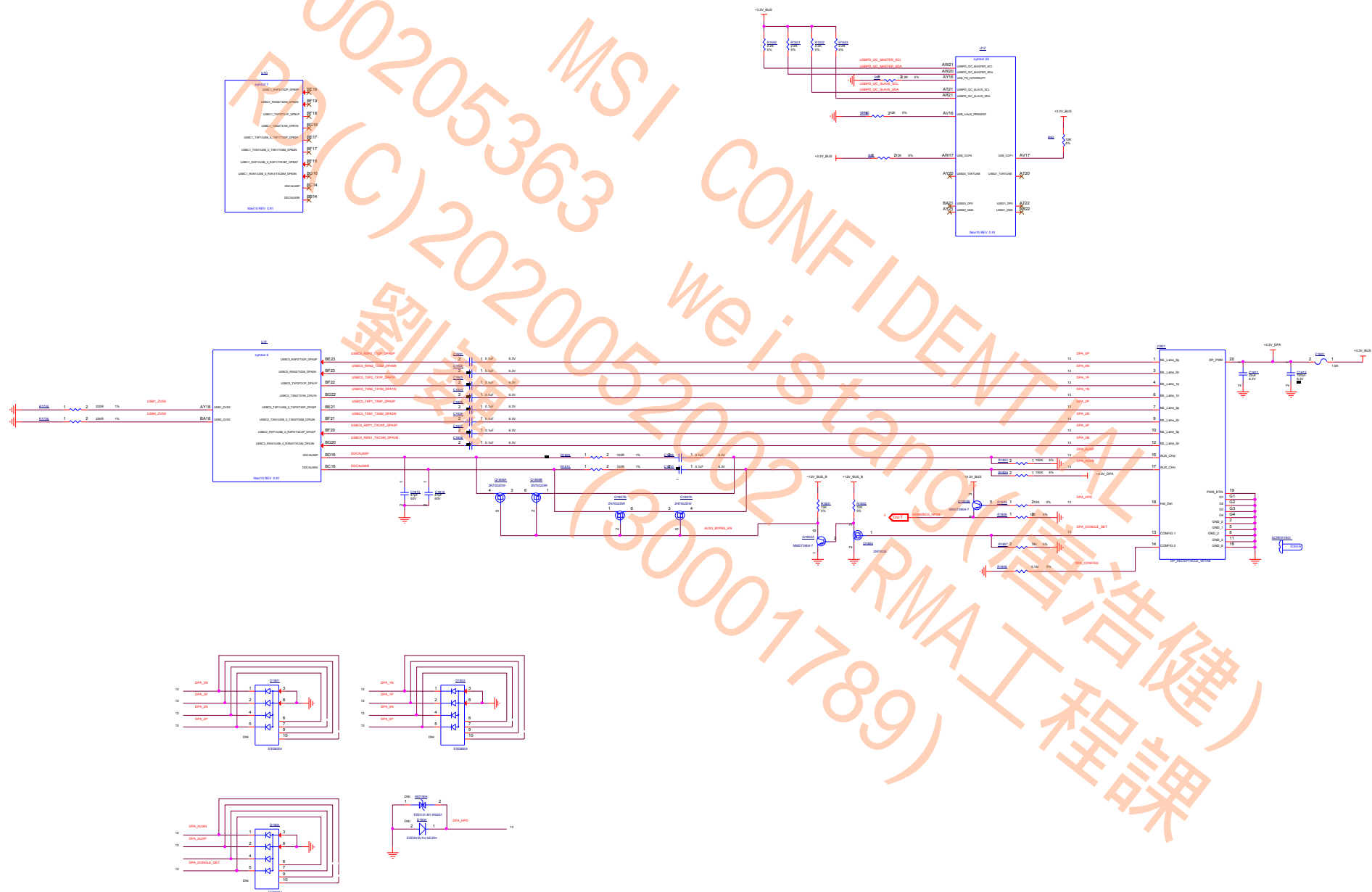


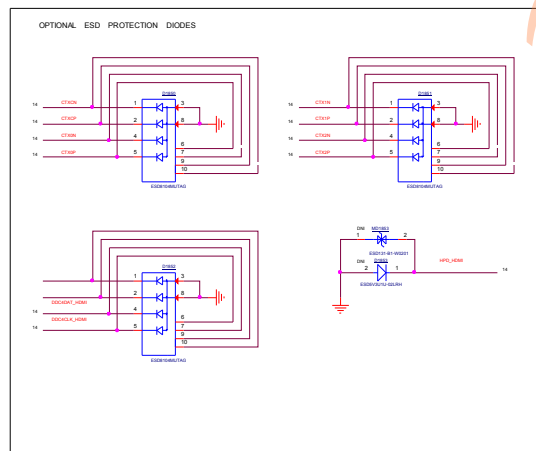
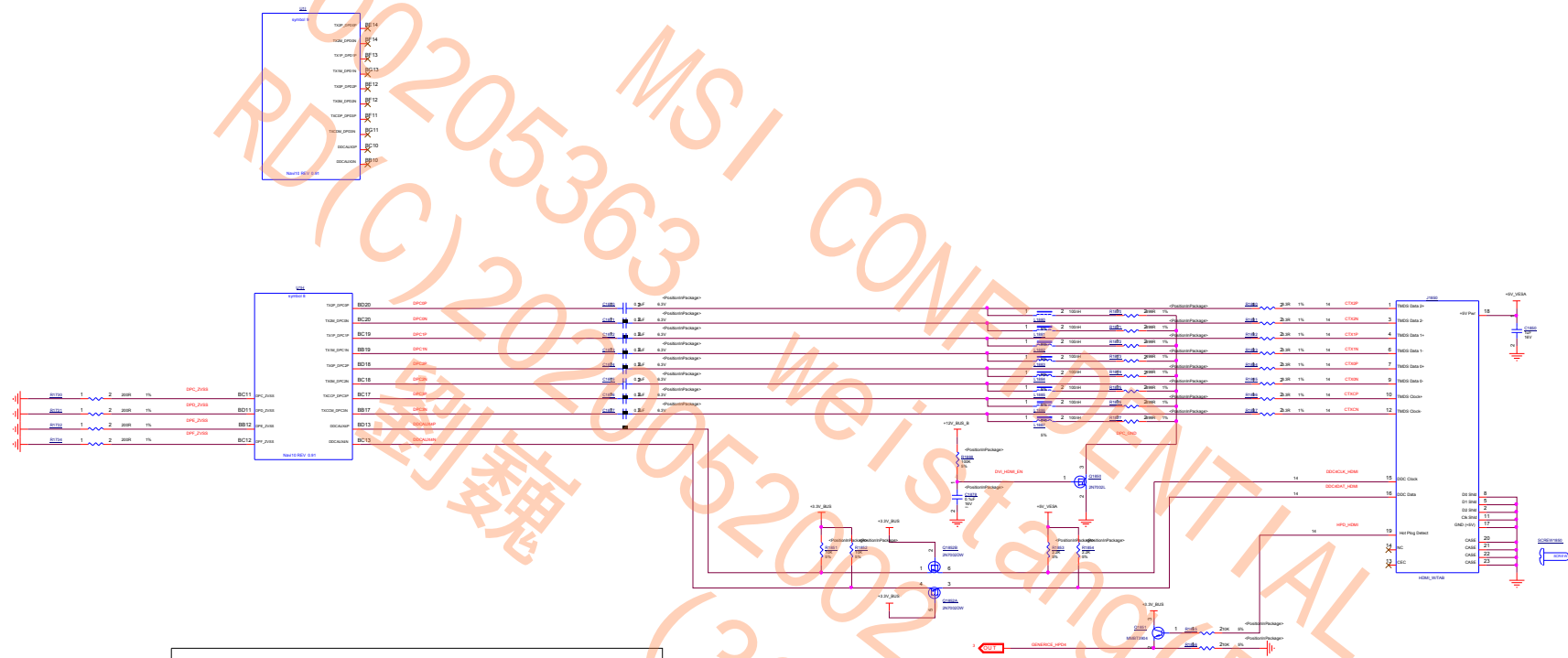




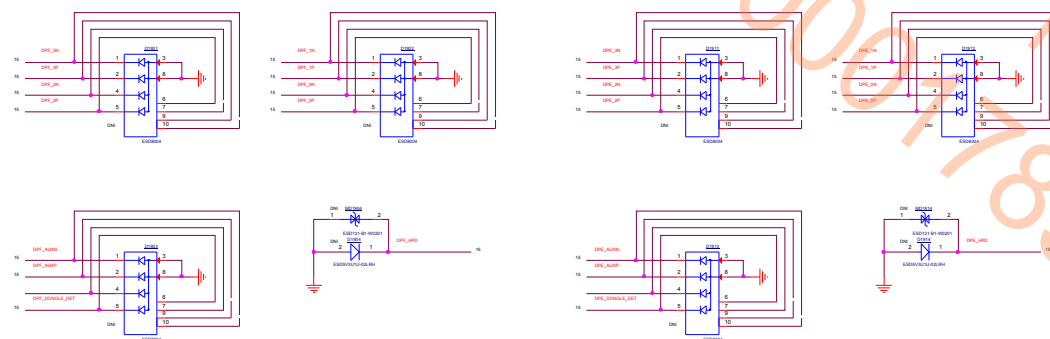
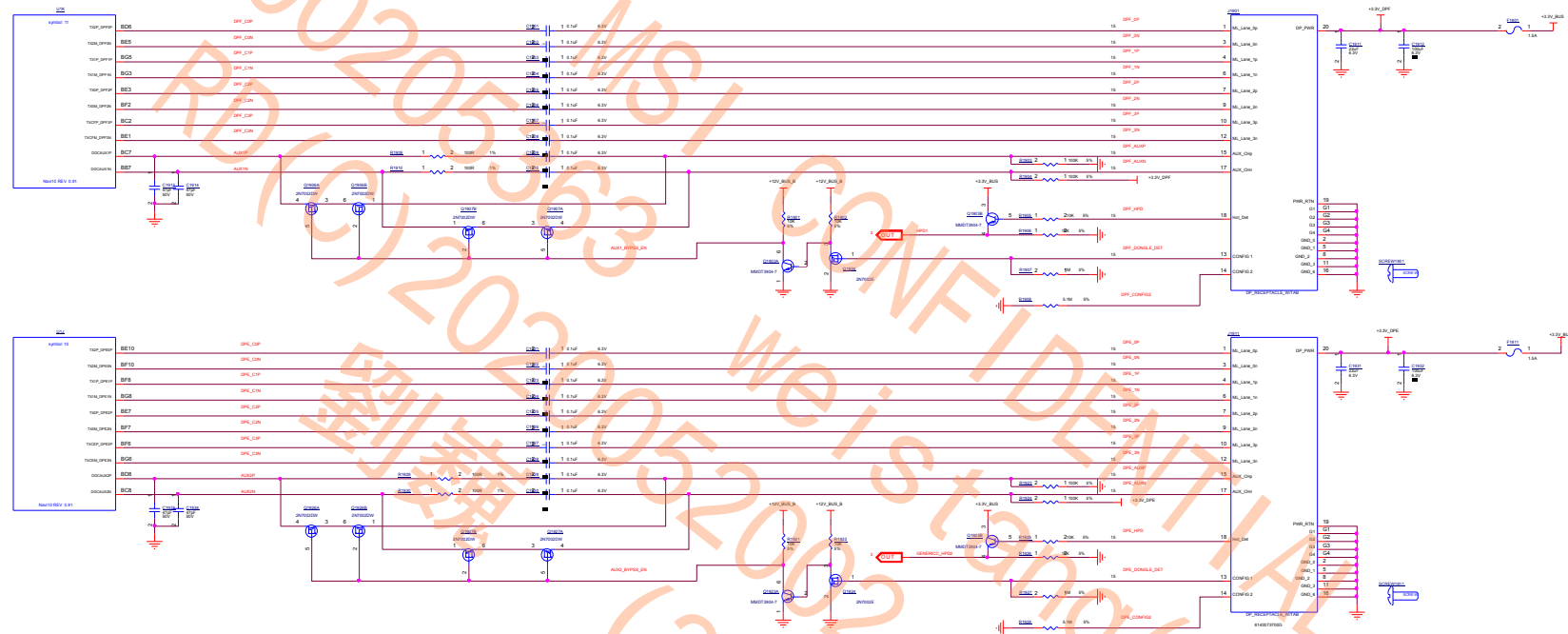


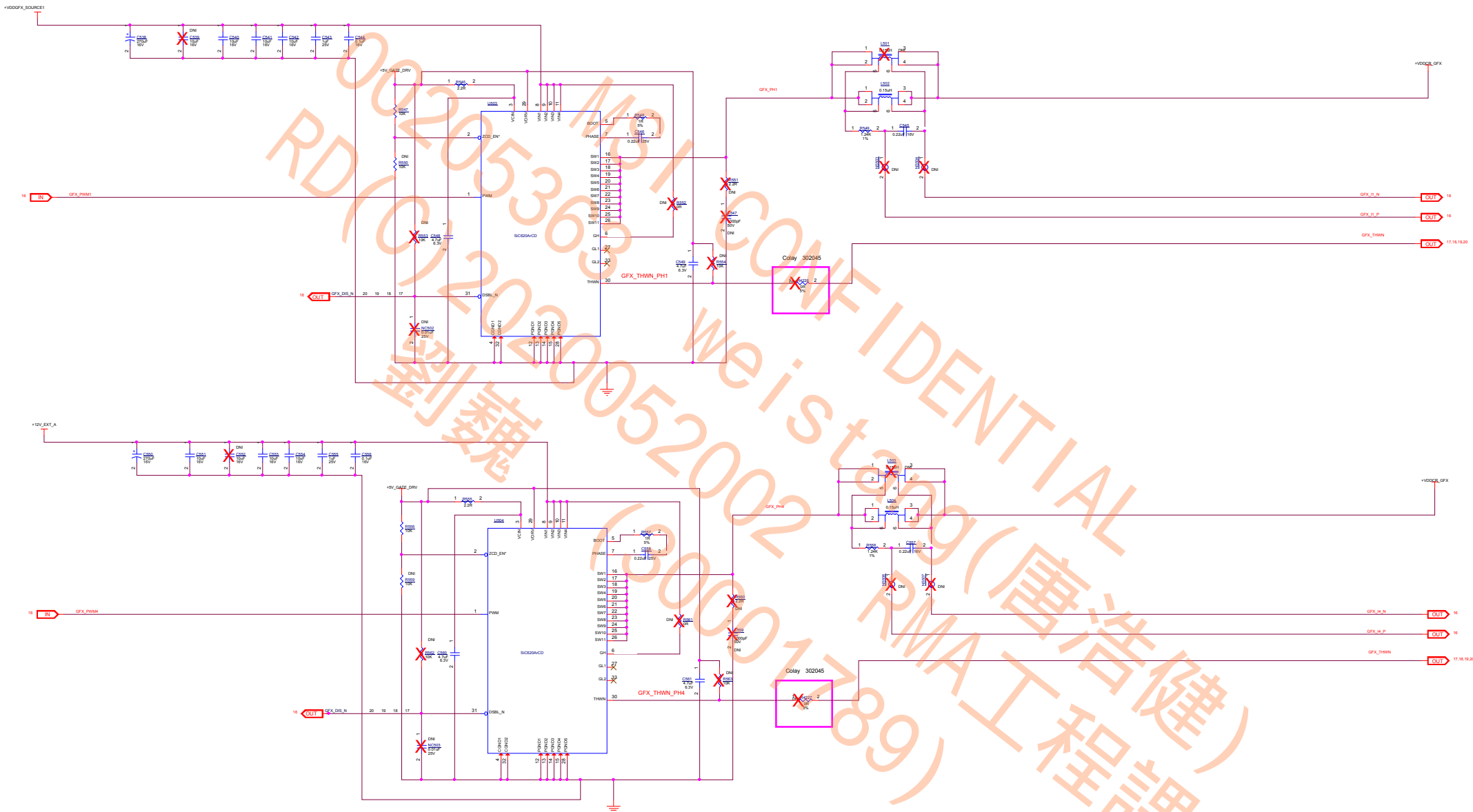


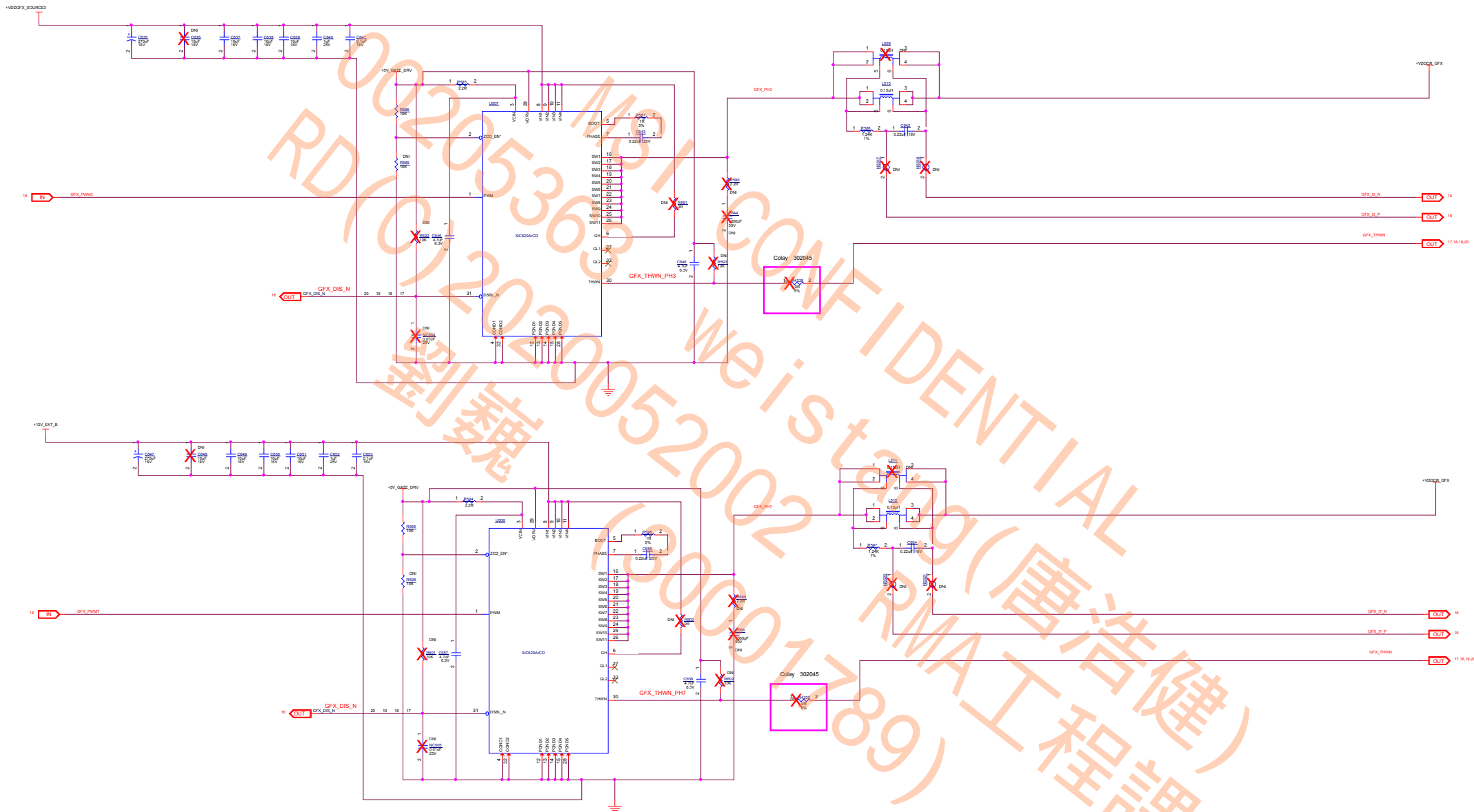


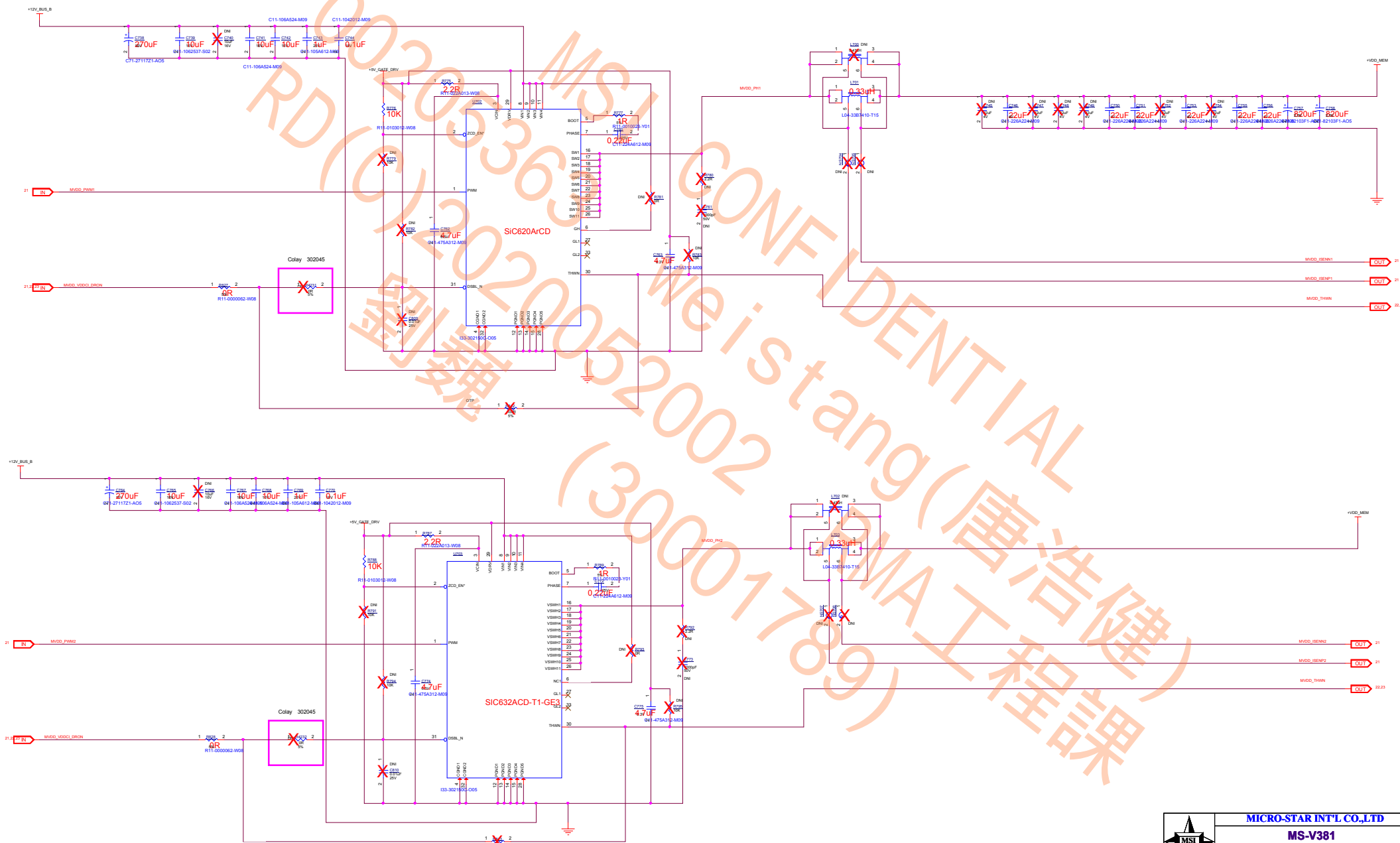


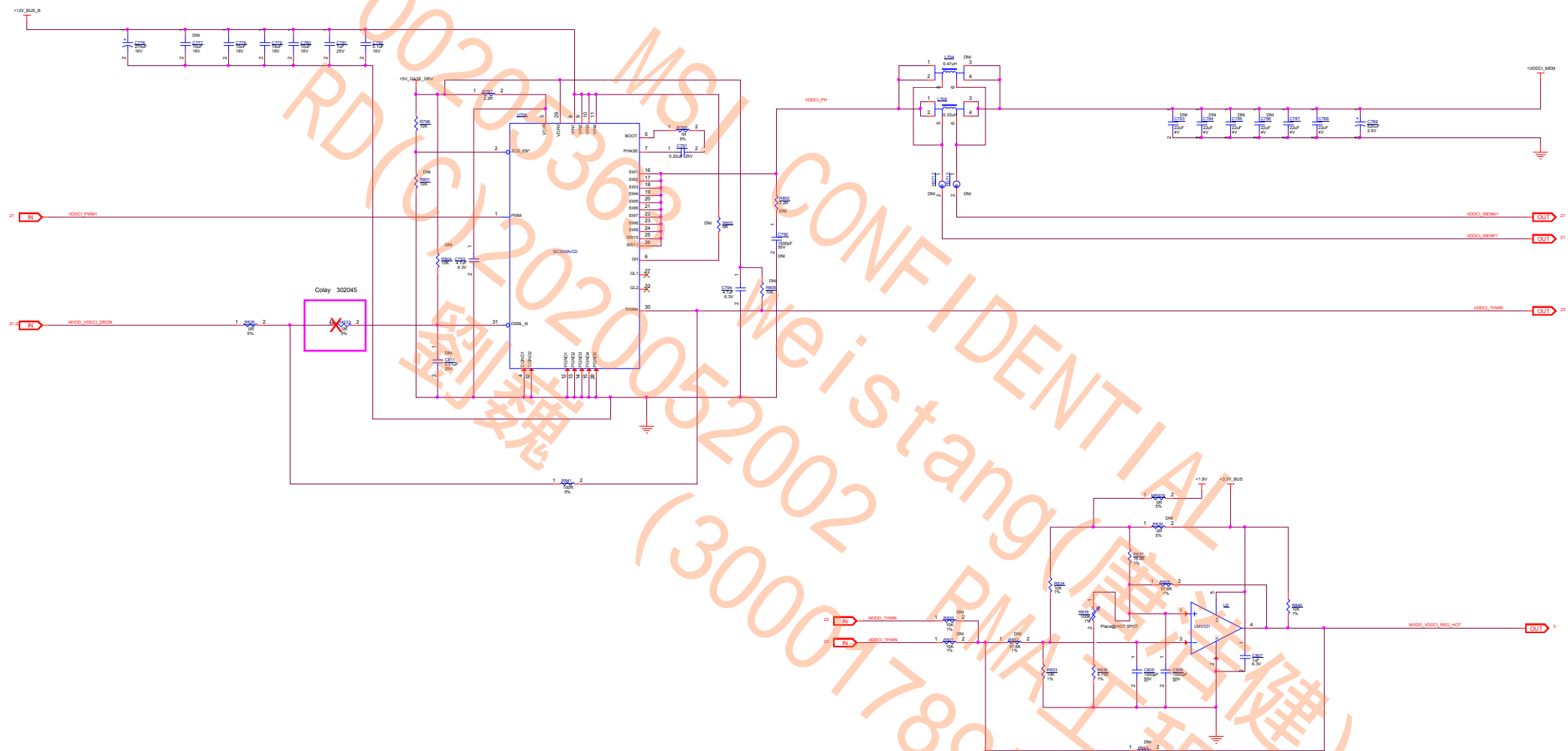
(9) NAVI10 TMDP E/F

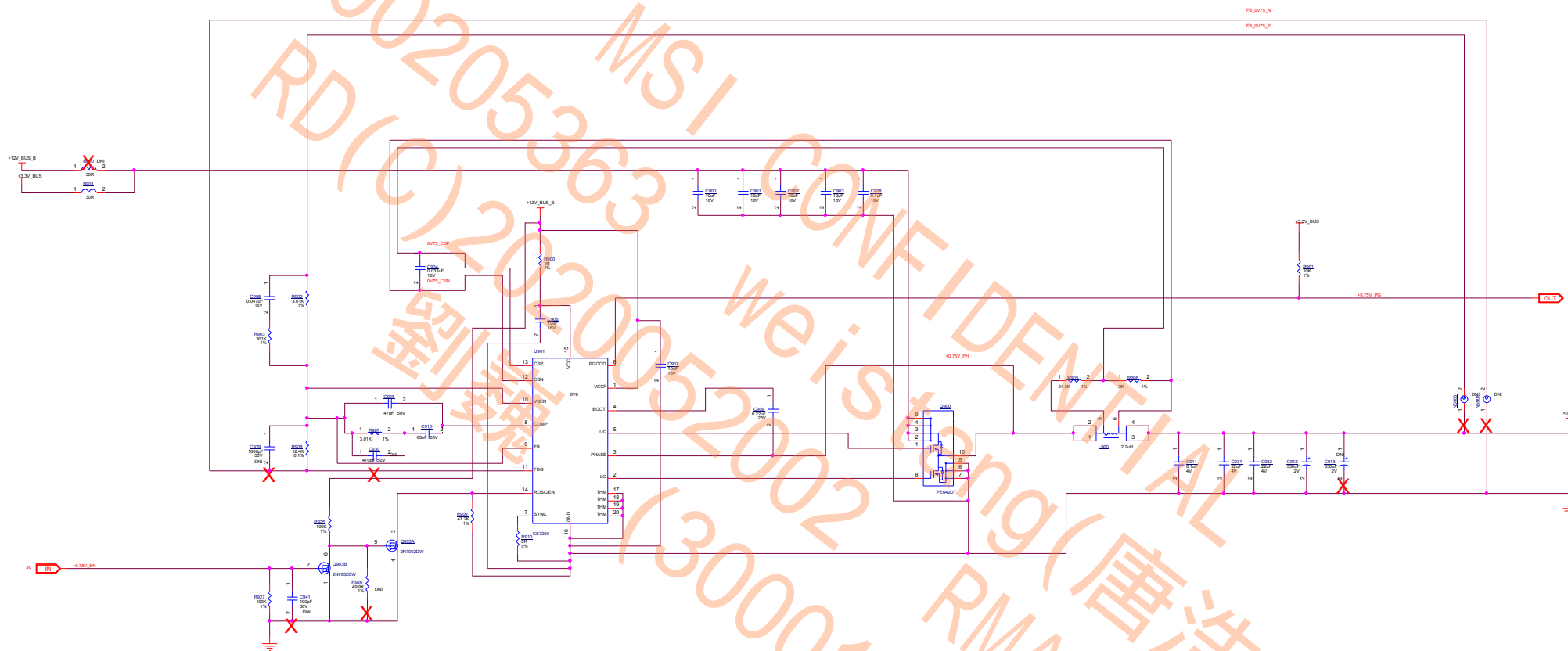


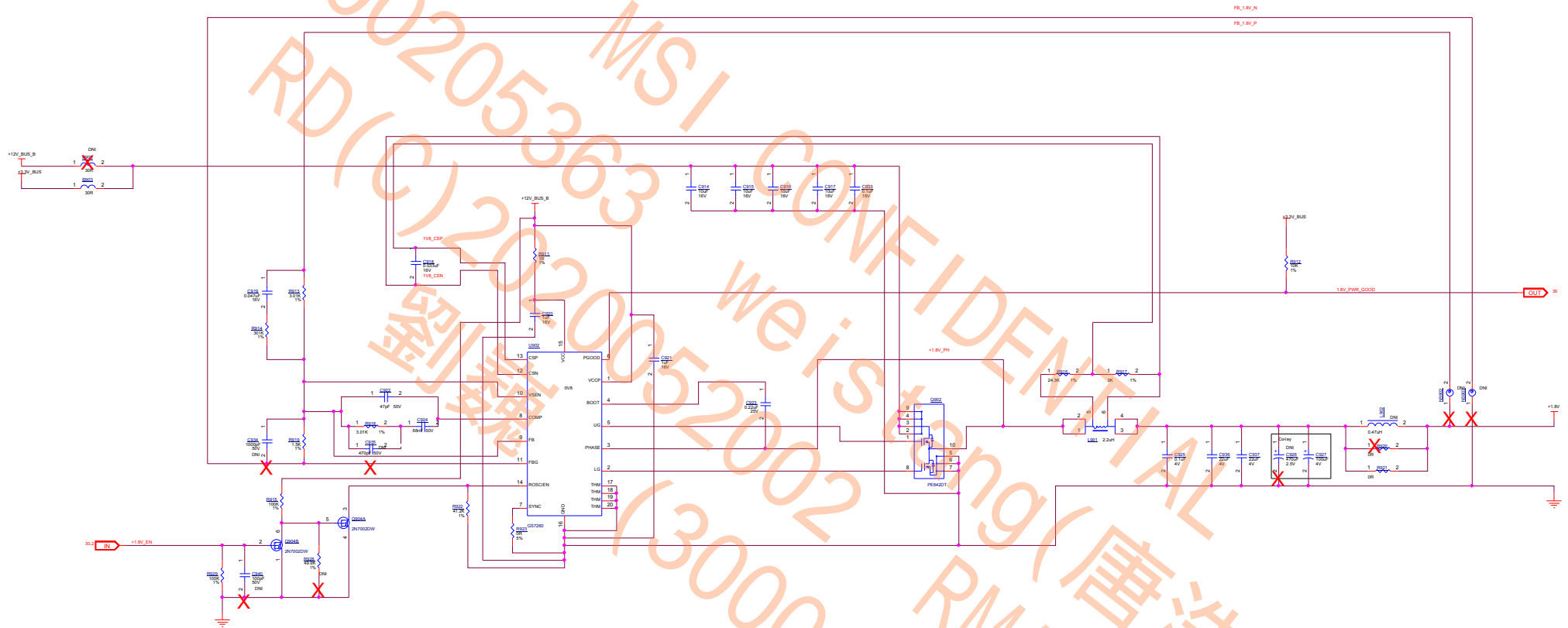


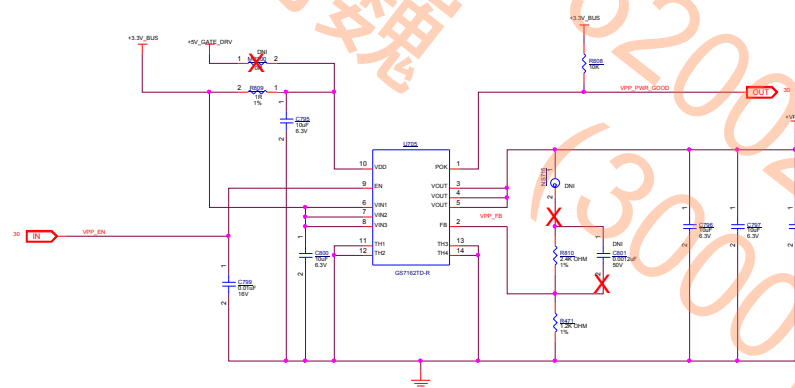


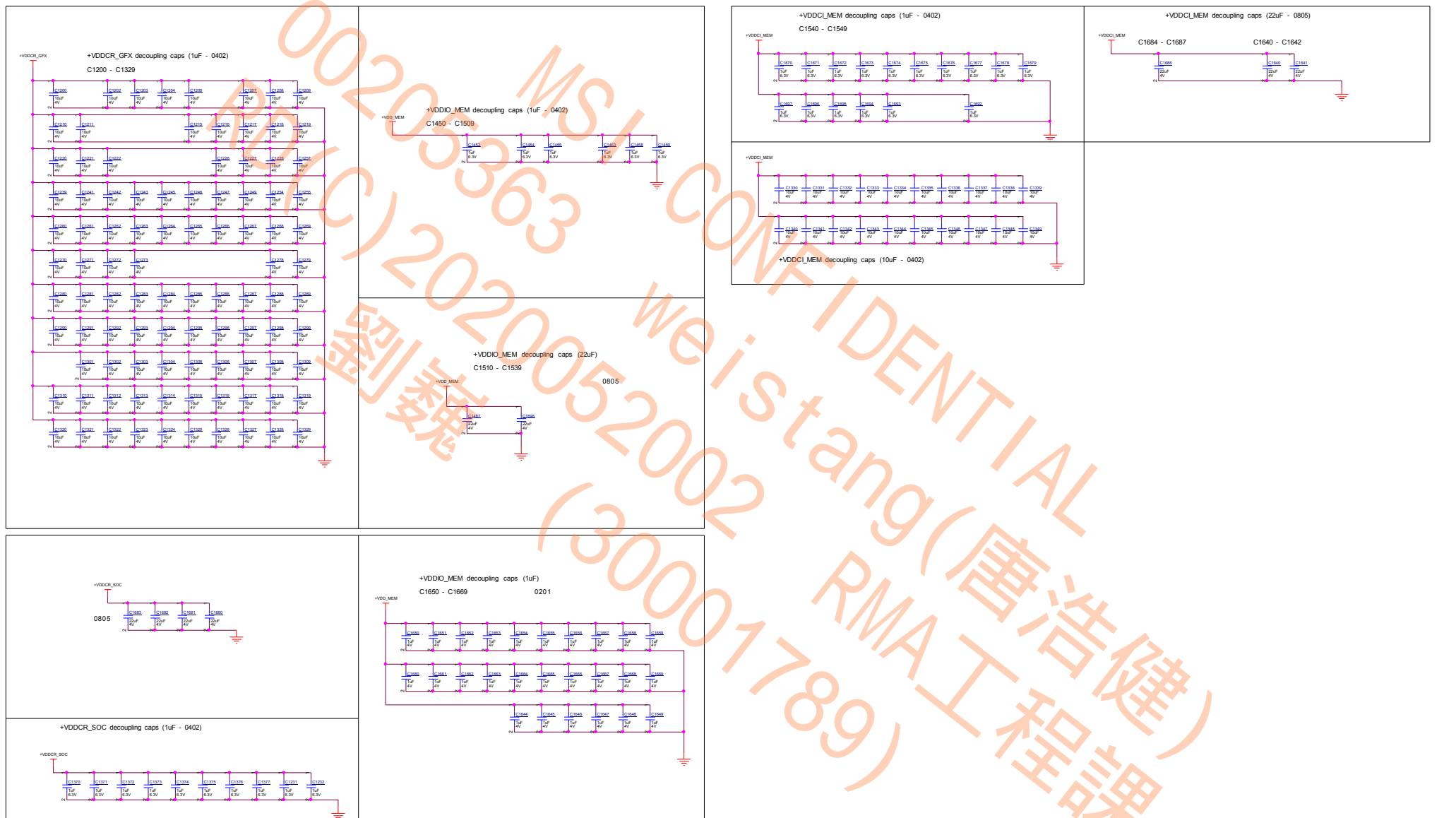


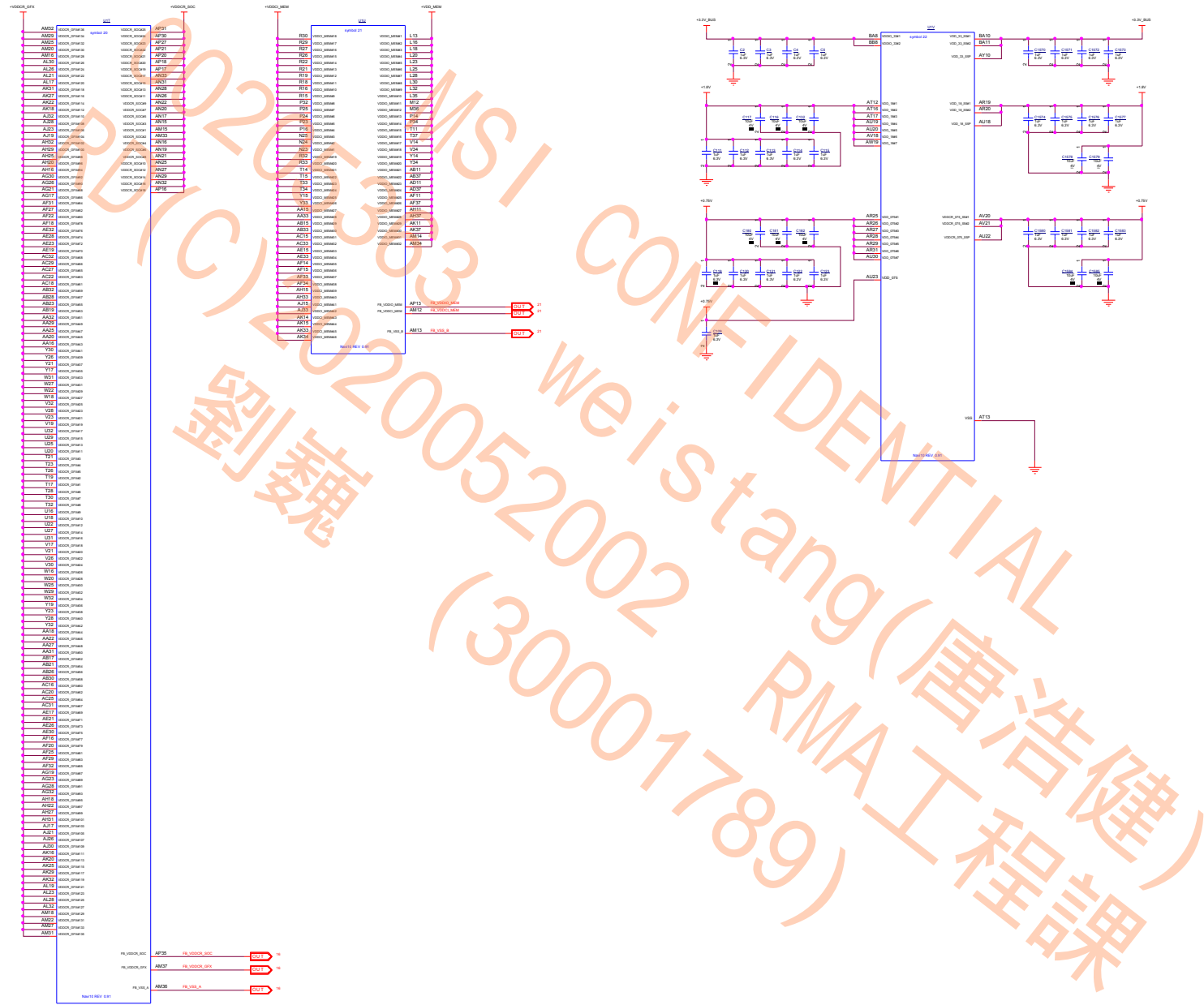


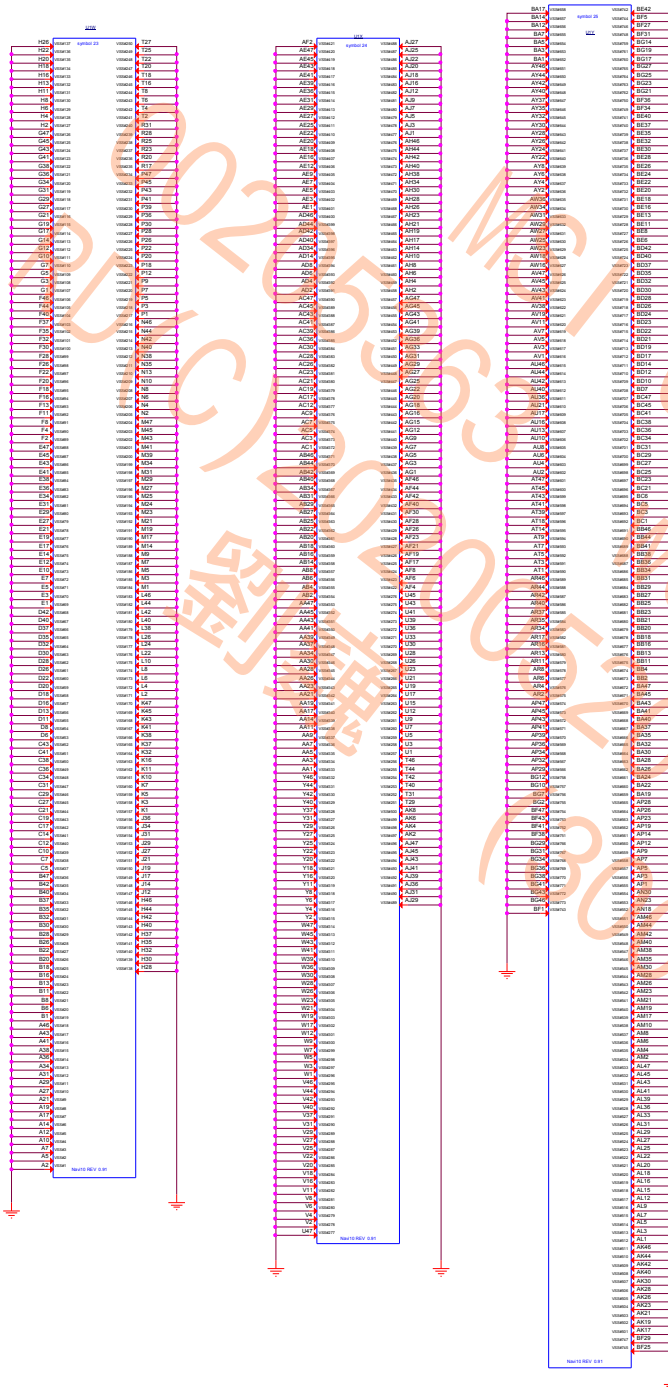


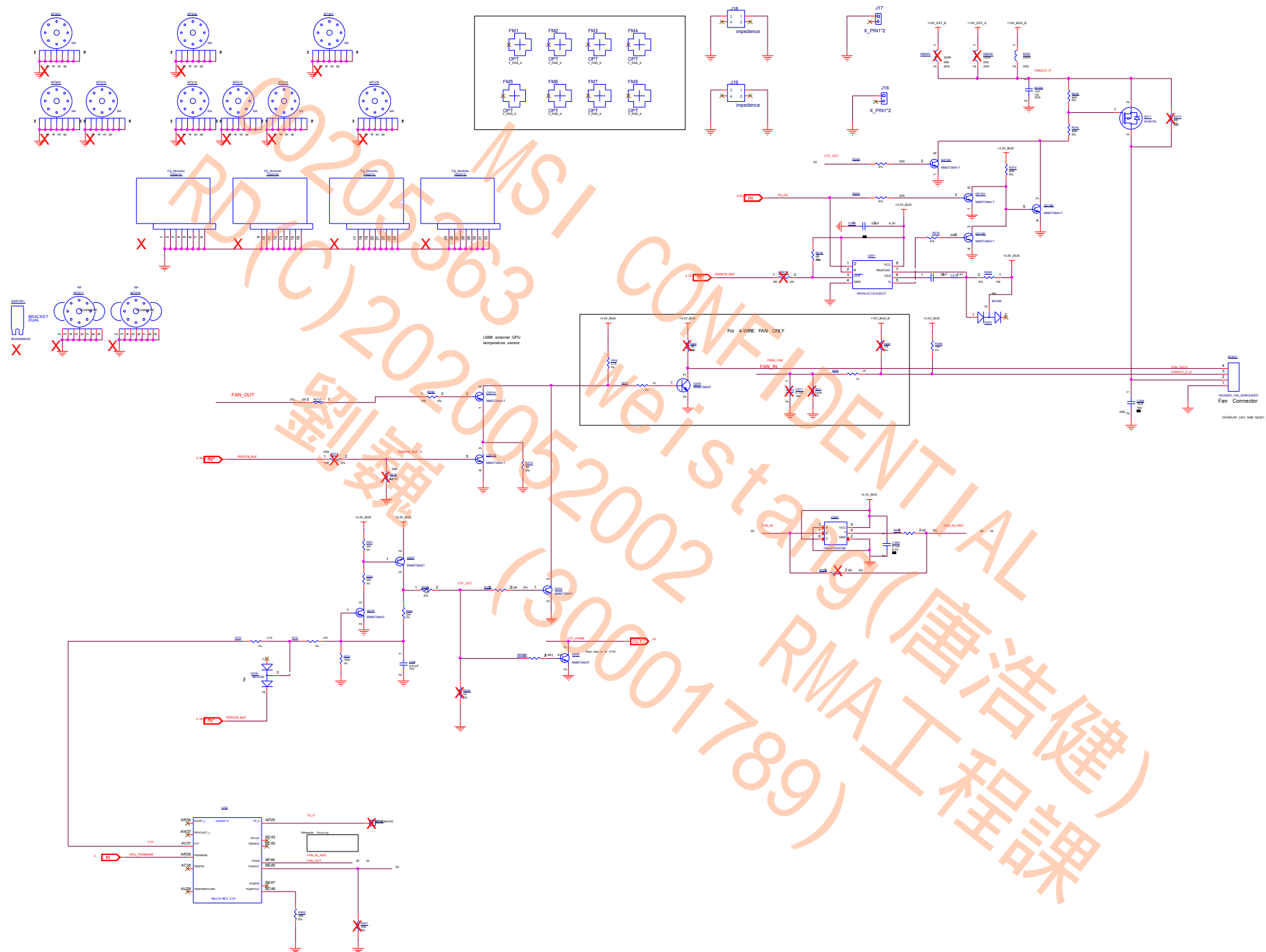


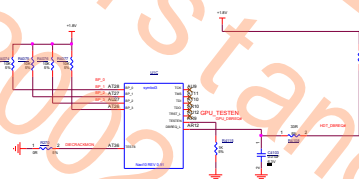
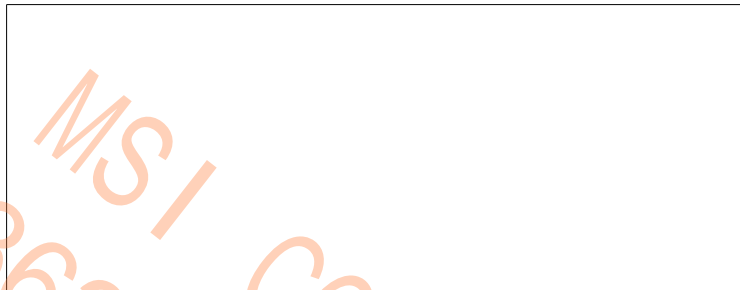
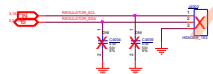




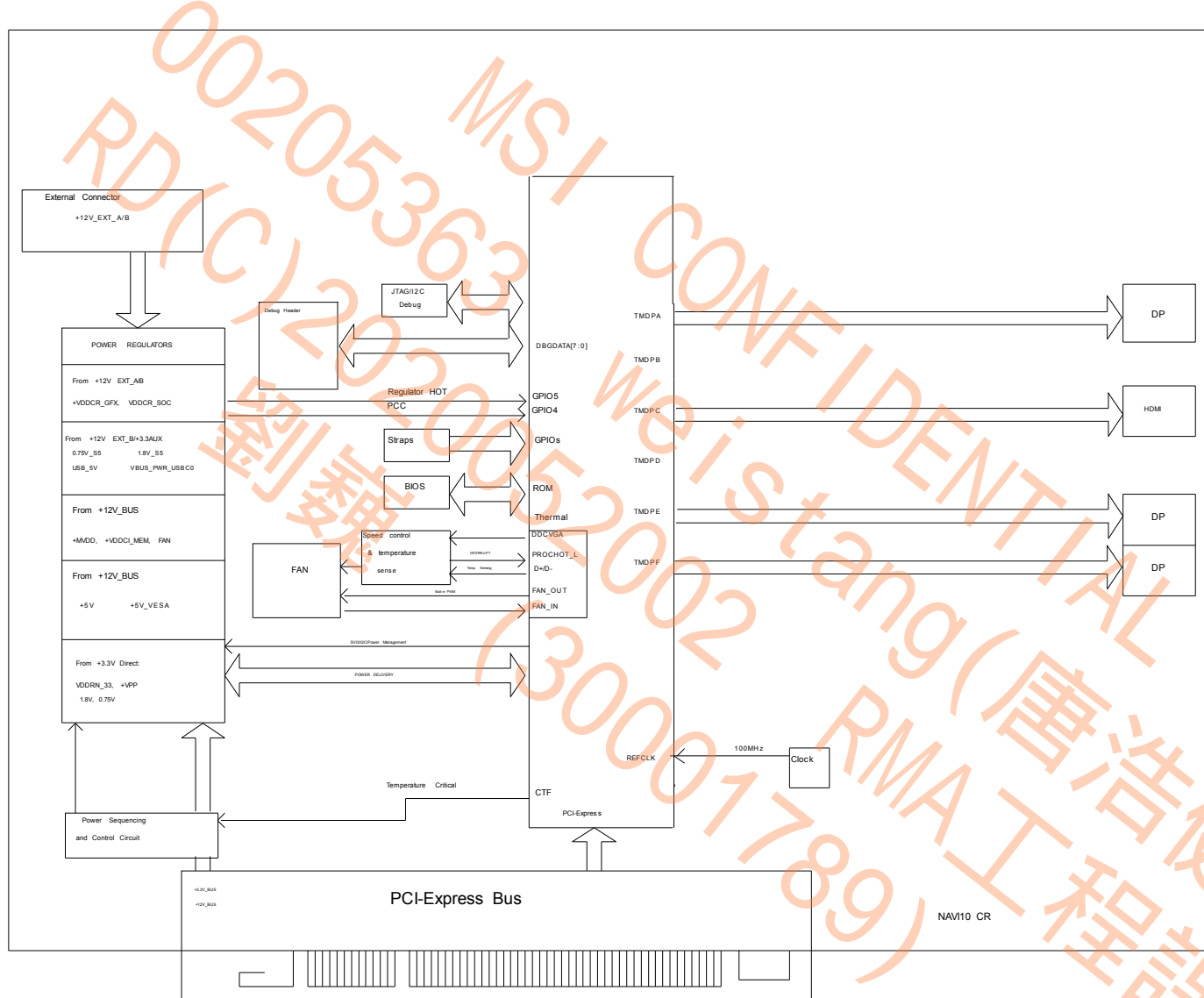








RADEON Lightbar header



**TITLE:**

NAVI10 G6X16mode DP DP HDMI DP

DOCUMENT NUMBER:

105_D199xxx_008

DATE:

Fri Jun 21 03:44:58 2019

SHEET NUMBER:

35

OF

35

REV: 1.00

REVISION HISTORY

ENGINEER:

Peak, Dong

NOTES :

NOTE

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Advanced Micro Device

AMD - PLATFORM HARDWARE ENG
No.669, HUANKE ROAD
SHANGHAI, CHINA 201203

SCH Rev	PCB Rev	Date	REVISION DESCRIPTION
1	-00A	FEB 11 2019	.ODA schematics
2	-00B	JUN 27 2019	ADD PULL HIGH ON THE PWRRPG
			2019_11_07 GFX_MEM_SOC_VDDCI Co-Lay 302045 and Power PIN fix to 8+6 reverse type Only 2019_11_11 Add Fan_IN output back Page 32, Change Footprint con_dp_astron_r6890020_tab > con_tab , edgecon_pci_express_gen4_16 > edgecon_16 , Remove MT203, MT 211, MT208 Screw Hole 2019_11_14 add Cross Light point , Remove Page 2 TP detect point, Remove lightbar header, Remove CTF & J4100 debug Pin