

P393-A01 Base Design

P393-A01, G92, 8Mx32/16Mx32 GDDR3 (800/1000 MHz),
DVI-I-DL, DVI-I-DL/DisplayPort, HDTVout/Stereo

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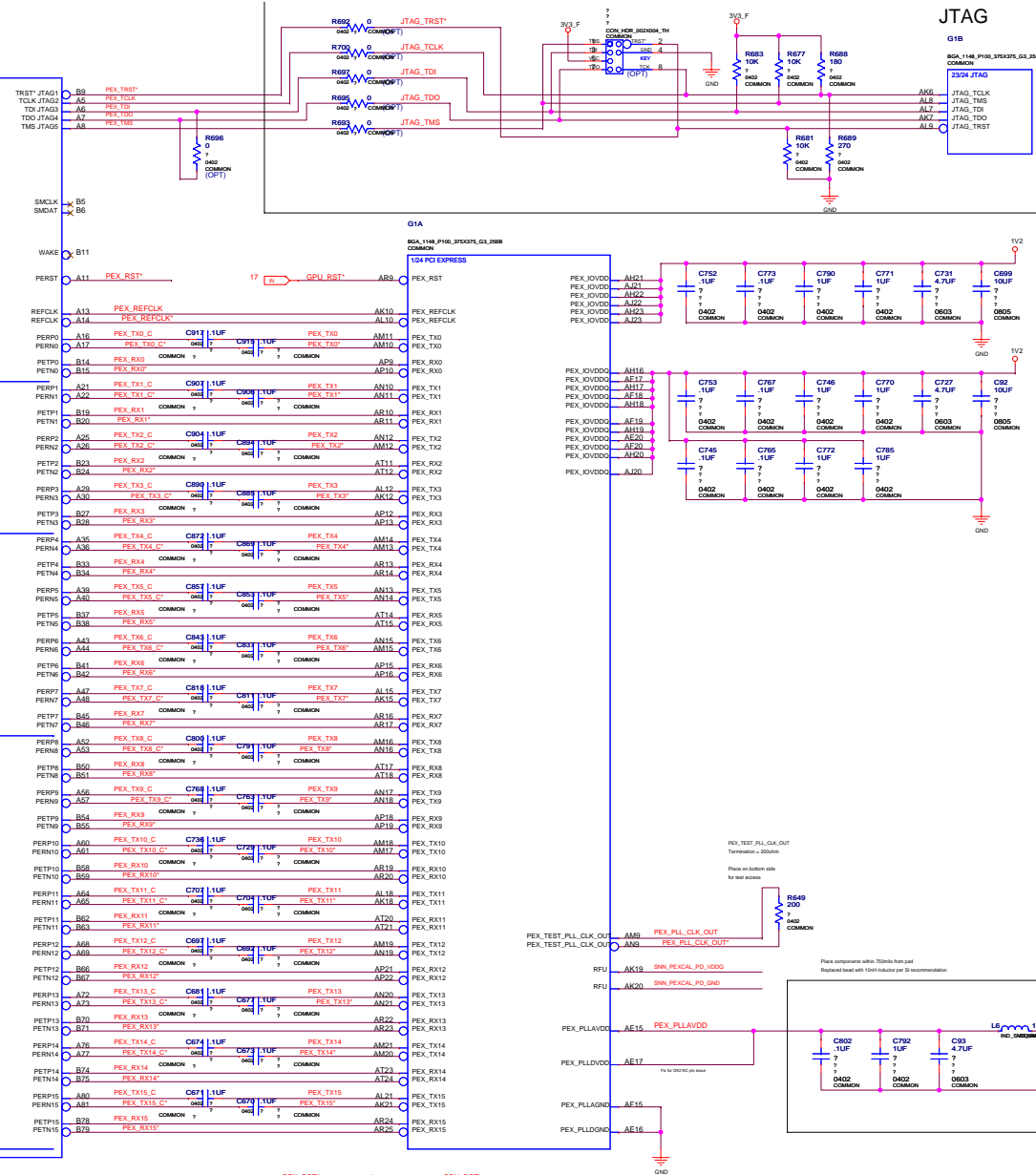
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REV	VARIANT	NPVN	ASSEMBLY
00	BASE	800-10393-0000-100	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU_DT_0000	800-10393-0000-100	P393 G92-300 512MB GDDR3 16Mx32 DVI-I+HDTV
2	SKU_DT_0002	800-10393-0002-100	P393 G92-200 512MB GDDR3 16Mx32 DVI-I+HDTV
3	SKU_W6_0501	800-10393-0500-100	P393 G92-475 512MB GDDR3 16Mx32 DVI-I+H+P+STEREO
4	SKU_W6_0501	800-10393-0501-100	P393 G92-850 512MB GDDR3 16Mx32 DVI-I+HDTV
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ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview

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SUMMARY			
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Stuff only to bypass the micro-controller

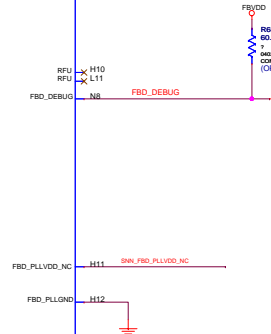
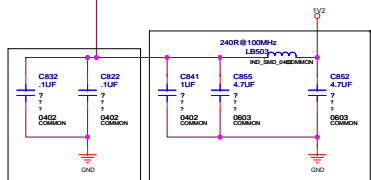
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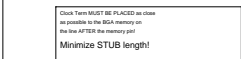


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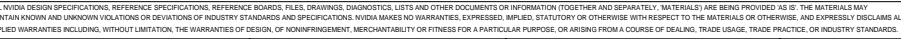


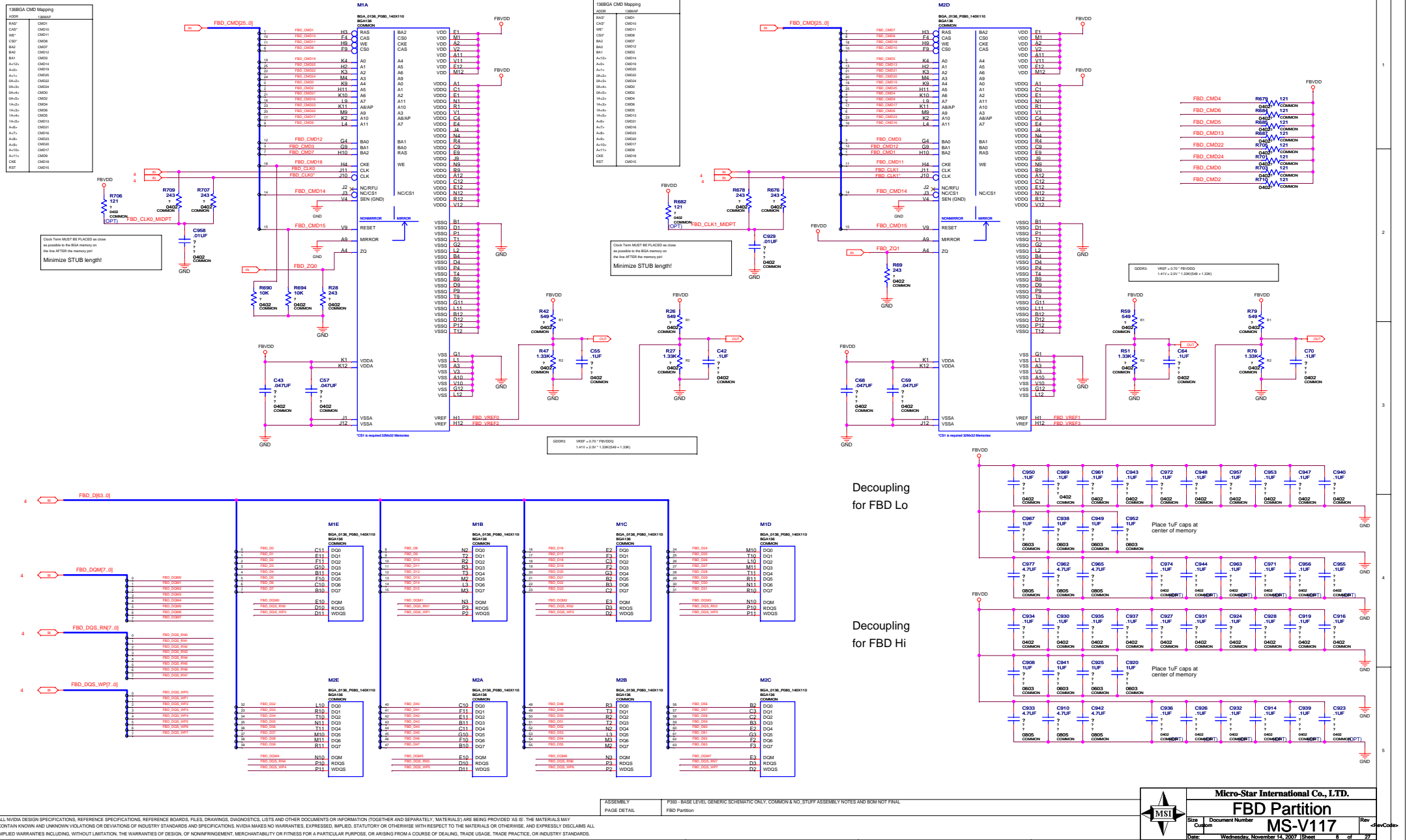




Decoupling for FBA Hi

1386GA CMD Mapping	
RAS	CM01
CAS	CM02
WE	CM03
CS0	CM04
BA2	CM07
BA0	CM08
BA1	CM09
A0	CM10
A1	CM11
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NET RULES for FrameBuffer A/B

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
CLUT	FBA_CLK0 3.5	1	NOFF
CLUT	FBA_CLK0P 3.5	1	FBA_CLK0
CLUT	FBA_CLK1 3.5	1	NOFF
CLUT	FBA_CLK1P 3.5	1	FBA_CLK1

CLUT	FBA_CMDS0 3.5	1	NOFF
CLUT	FBA_CMDS0P 3.5	1	NOFF
CLUT	FBA_CMDS1 3.5	1	NOFF
CLUT	FBA_CMDS1P 3.5	1	NOFF
B	FBA_VIO 3.5	1	NOFF

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
CLUT	FBB_CLK0 3.5	1	NOFF
CLUT	FBB_CLK0P 3.5	1	FBB_CLK0
CLUT	FBB_CLK1 3.5	1	NOFF
CLUT	FBB_CLK1P 3.5	1	FBB_CLK1

CLUT	FBB_CMDS0 3.5	1	NOFF
CLUT	FBB_CMDS0P 3.5	1	NOFF
CLUT	FBB_CMDS1 3.5	1	NOFF
CLUT	FBB_CMDS1P 3.5	1	NOFF
B	FBB_VIO 3.5	1	NOFF

B	FBA_DEB0 3	1	NOFF
B	FBB_DEB0 3	1	NOFF

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
B	FBA0_PLAVDD 3	1.2V	0.02A
B	FBA_VREF0 5	1.40V	0.02A
B	FBA_VREF1 5	1.40V	0.02A
B	FBA_VREF2 5	1.40V	0.02A
B	FBA_VREF3 5	1.40V	0.02A
B	FBA_Z00 5	2.0V	0.02A
B	FBA_Z01 5	2.0V	0.02A

B	FBB_VREF0 5	1.40V	0.02A
B	FBB_VREF1 5	1.40V	0.02A
B	FBB_VREF2 5	1.40V	0.02A
B	FBB_VREF3 5	1.40V	0.02A
B	FBB_Z00 5	2.0V	0.02A
B	FBB_Z01 5	2.0V	0.02A

B	FBA_VREF1 3	1.40V	0.02A
B	FBA_VREF2 3	1.40V	0.02A

NET RULES for FrameBuffer C/D

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
CLUT	FBC_CLK0 4.7	1	NOFF
CLUT	FBC_CLK0P 4.7	1	FBC_CLK0
CLUT	FBC_CLK1 4.7	1	NOFF
CLUT	FBC_CLK1P 4.7	1	FBC_CLK1

CLUT	FBC_CMDS0 4.7	1	NOFF
CLUT	FBC_CMDS0P 4.7	1	NOFF
CLUT	FBC_CMDS1 4.7	1	NOFF
CLUT	FBC_CMDS1P 4.7	1	NOFF
B	FBC_VIO 4.7	1	NOFF

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
CLUT	FBD_CLK0 4.8	1	NOFF
CLUT	FBD_CLK0P 4.8	1	FBD_CLK0
CLUT	FBD_CLK1 4.8	1	NOFF
CLUT	FBD_CLK1P 4.8	1	FBD_CLK1

CLUT	FBD_CMDS0 4.8	1	NOFF
CLUT	FBD_CMDS0P 4.8	1	NOFF
CLUT	FBD_CMDS1 4.8	1	NOFF
CLUT	FBD_CMDS1P 4.8	1	NOFF
B	FBD_VIO 4.8	1	NOFF

B	FBD_DEB0 4	1	NOFF
B	FBD_DEB0 4	1	NOFF

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
B	FBC0_PLAVDD 4	1.2V	0.02A
B	FBC_VREF0 7	1.40V	0.02A
B	FBC_VREF1 7	1.40V	0.02A
B	FBC_VREF2 7	1.40V	0.02A
B	FBC_VREF3 7	1.40V	0.02A
B	FBC_Z00 7	2.0V	0.02A
B	FBC_Z01 7	2.0V	0.02A

B	FBD_VREF0 8	1.40V	0.02A
B	FBD_VREF1 8	1.40V	0.02A
B	FBD_VREF2 8	1.40V	0.02A
B	FBD_VREF3 8	1.40V	0.02A
B	FBD_Z00 8	2.0V	0.02A
B	FBD_Z01 8	2.0V	0.02A

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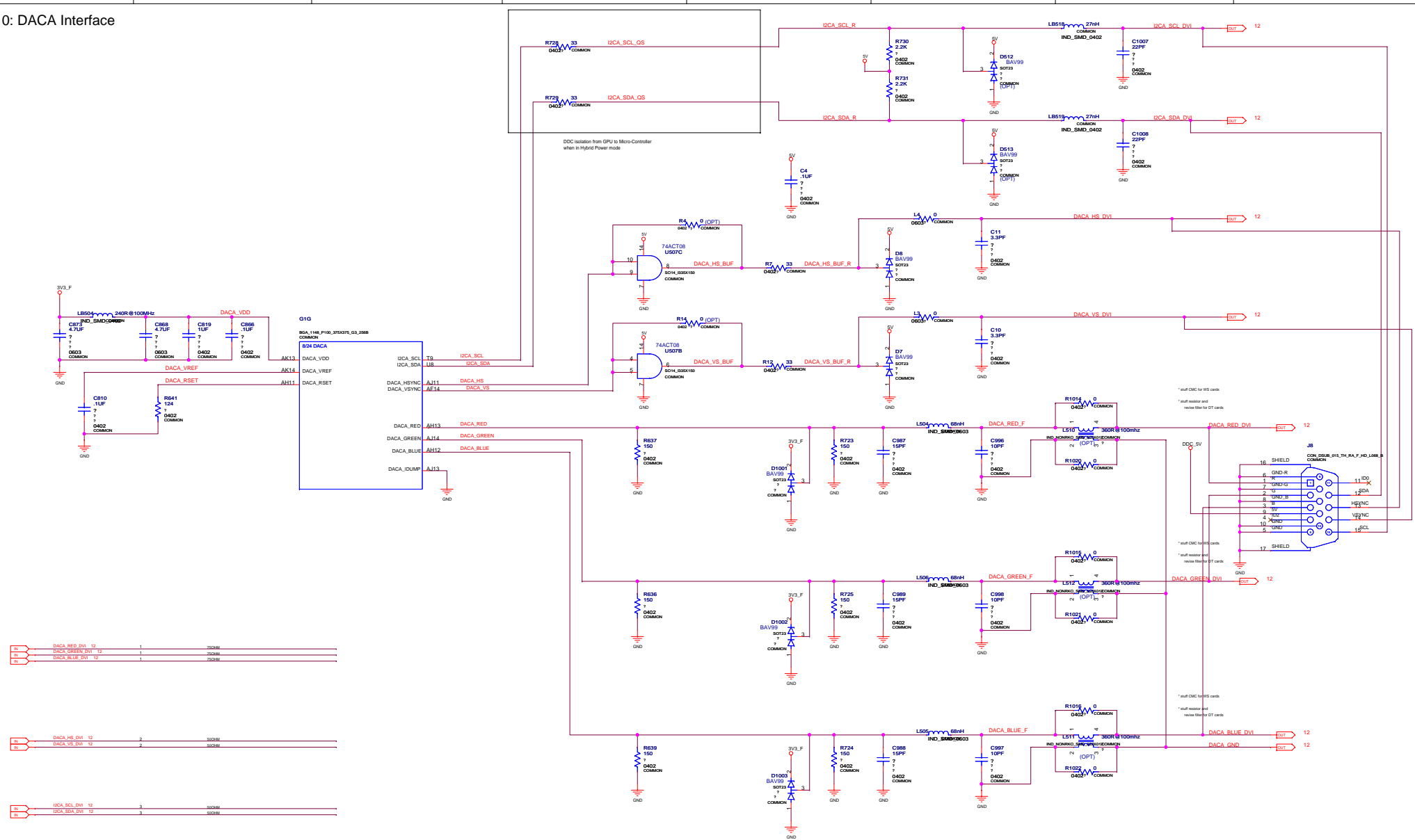
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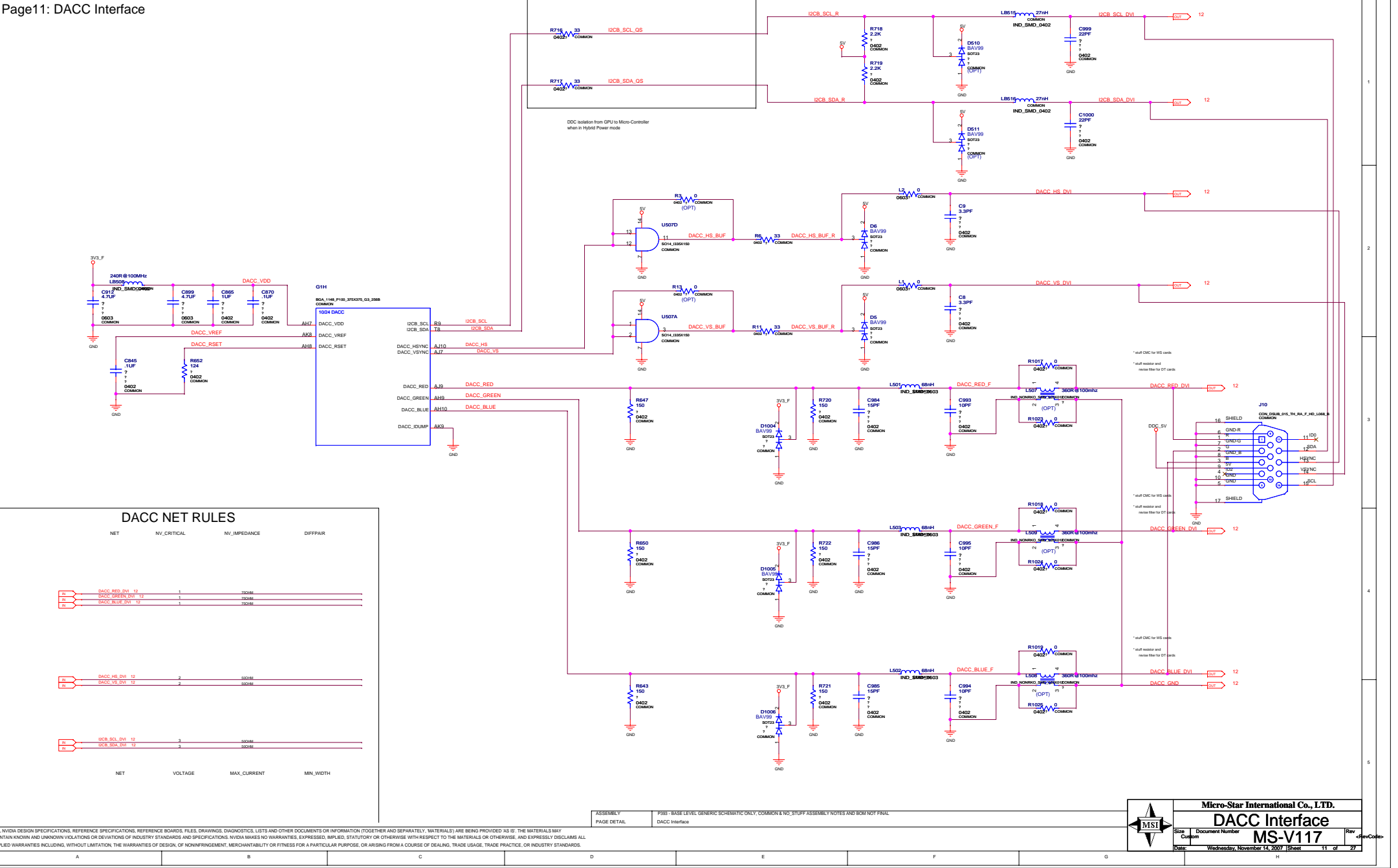
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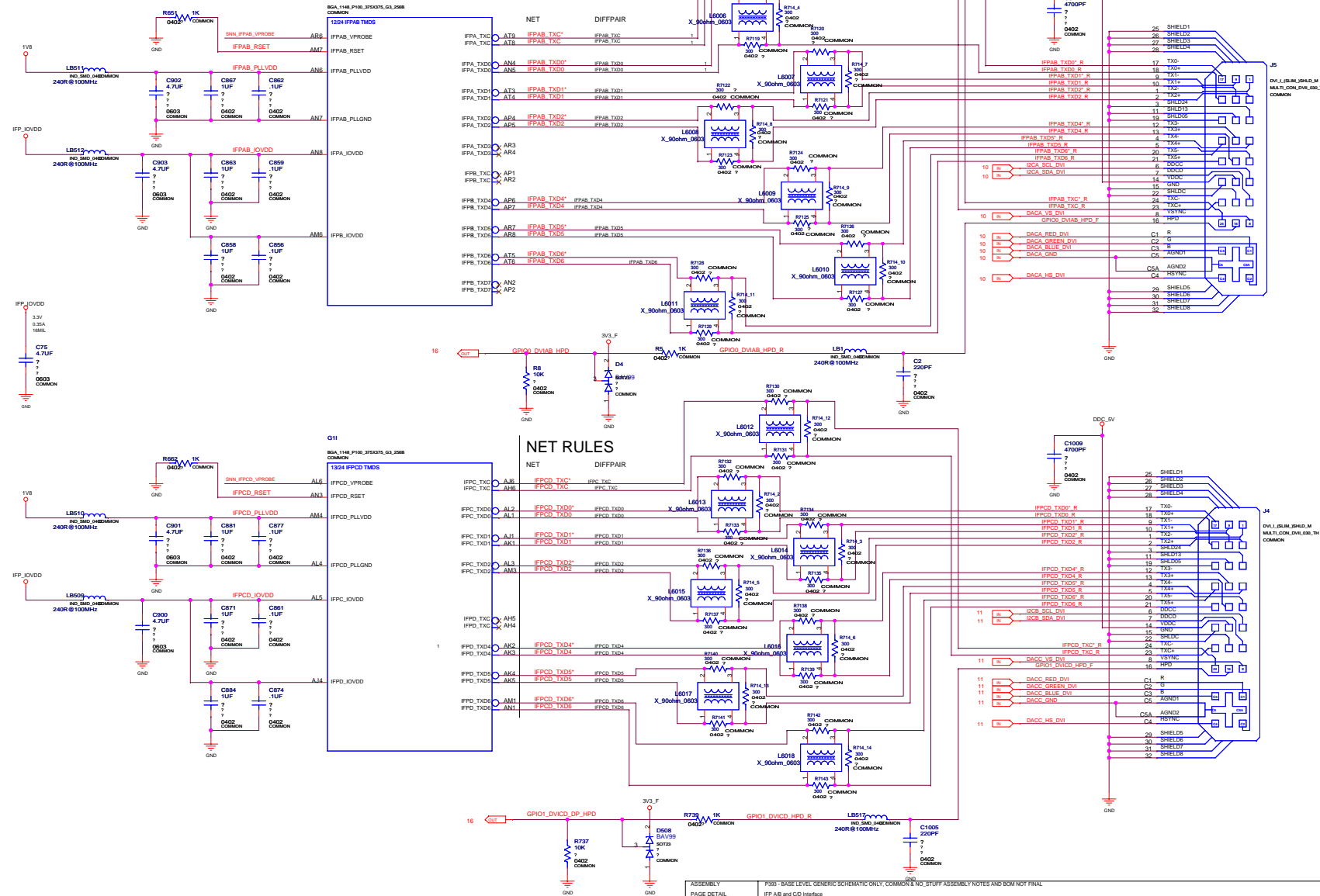
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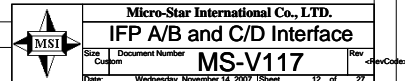
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ASSEMBLY PAGE DETAIL
F001: BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON'S NO STOPF ASSEMBLY NOTES AND NON NOT PRINT
DACC Interface

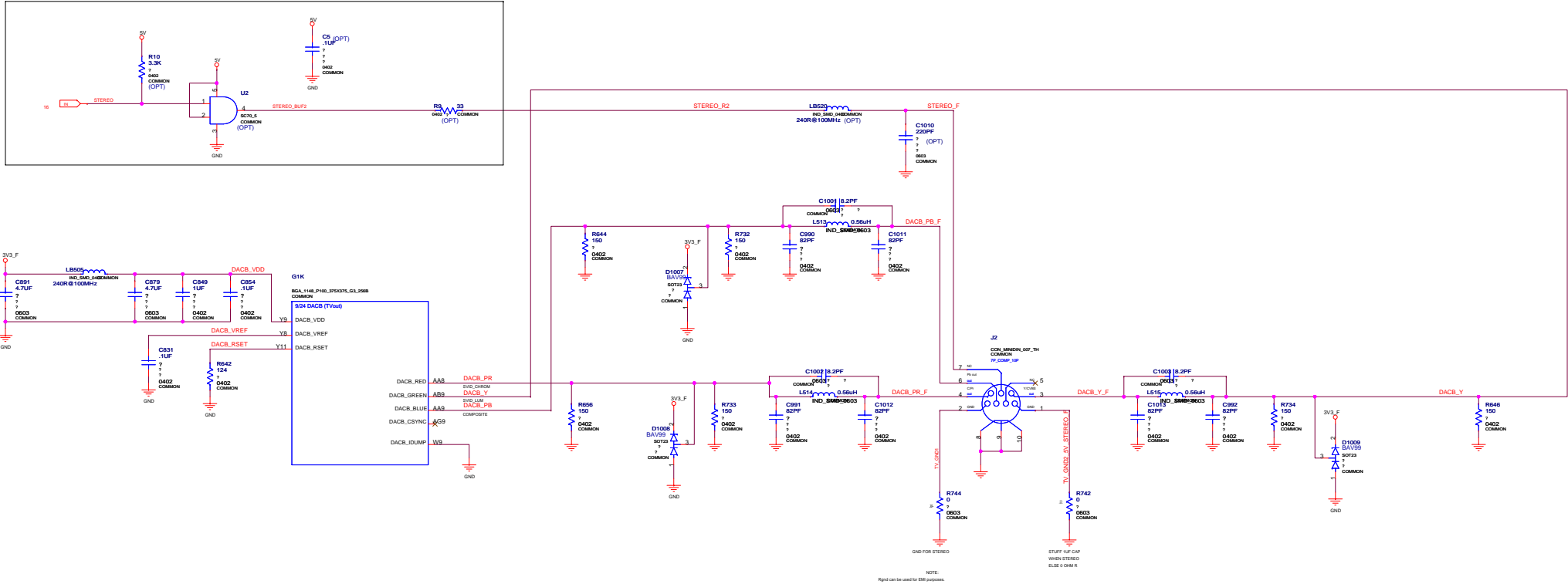


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ASSEMBLY	P300 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP A/B and C/D Interface



Stereo



NOTE:
Rgnd can be used for EMI purposes.

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ASSEMBLY	P300 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB and Stereo Interface

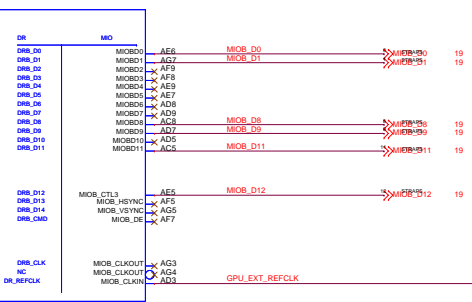
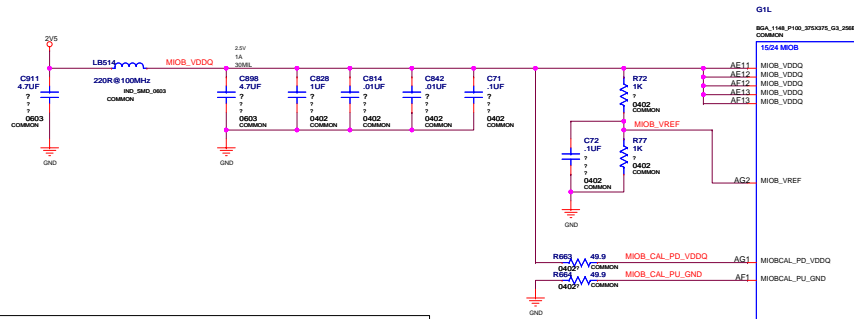
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DACB and Stereo Interface


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	Multi-use IO(MIO) Interface		
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Page15: Display Port (Analogix ANX9802/ANX9805)

* IEC keeper circuit removed

* ANX9805 support

pin 76 - GPIO3 to DP mode, from pin 13, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 74 - GPIO2, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 73 - CSC support via I2C and pull-up, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 71 - SPDR1 - tie to GND, input select 01 through internal register

pin 70 - SPDR0 - support for Audio input, grounded on ANX9802
- place GND resistor away from ANX device if needed

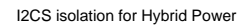
pin 68 - NC - tie to GND

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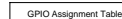
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PAGE DETAIL	Display Port



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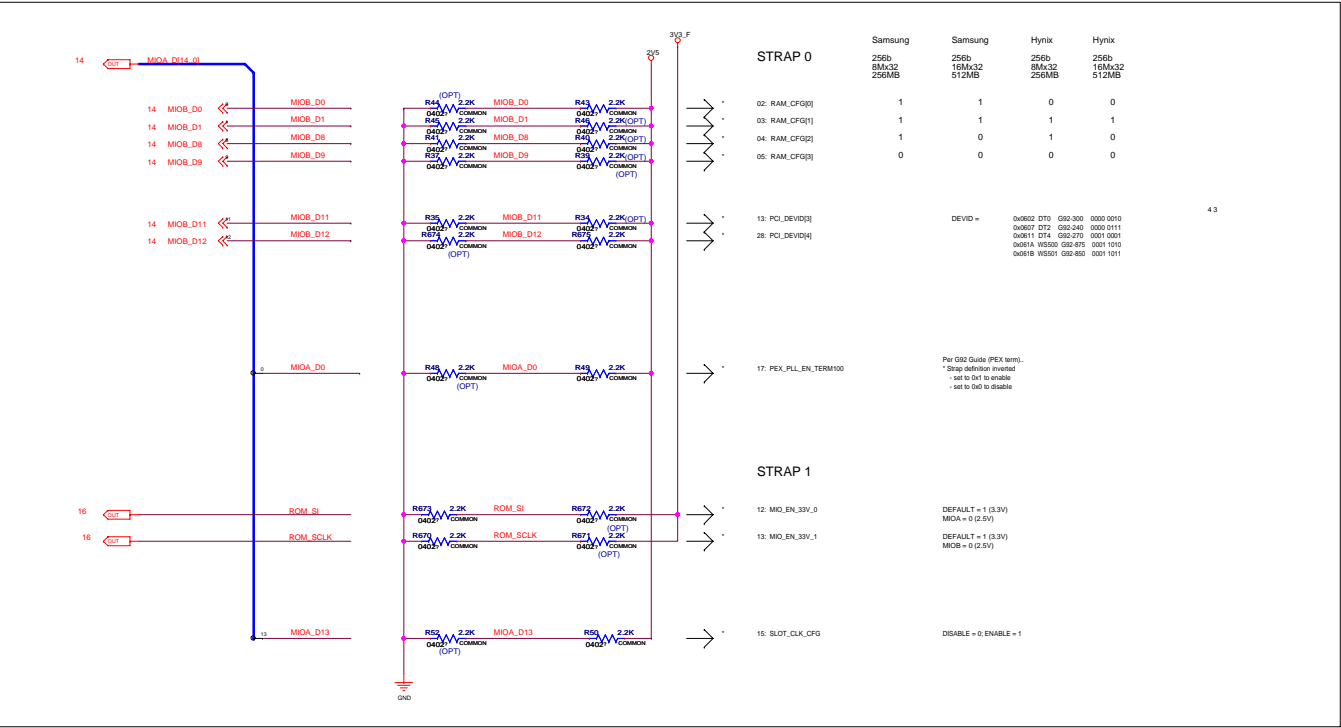


(BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)

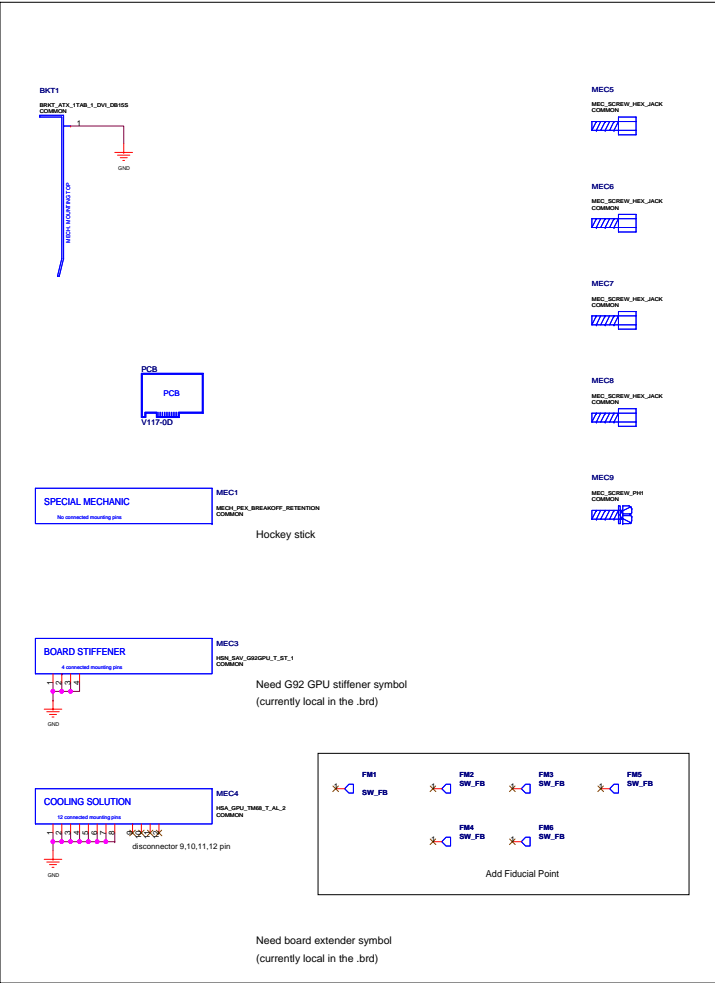


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STRAPS



MECHANICAL



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ASSEMBLY
PAGE DETAIL
F011 - BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO STRAP ASSEMBLY NOTES AND BOM NOT FINAL
Configuration Straps and Mechanical

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Straps and Mechanical

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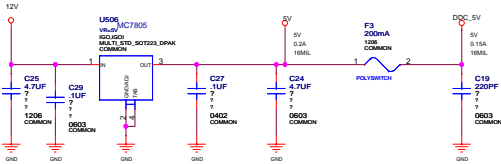
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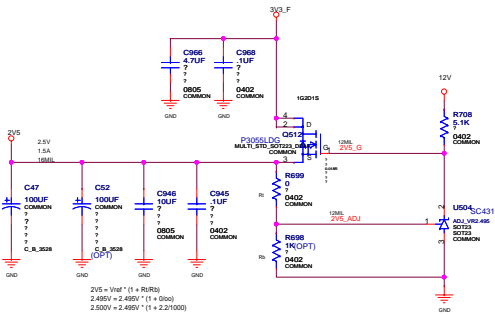
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5V and DDC5V Supply



2V5 Supply

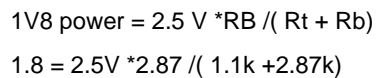


DEL 5V STEREO Supply

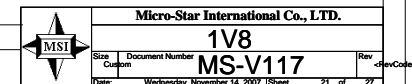
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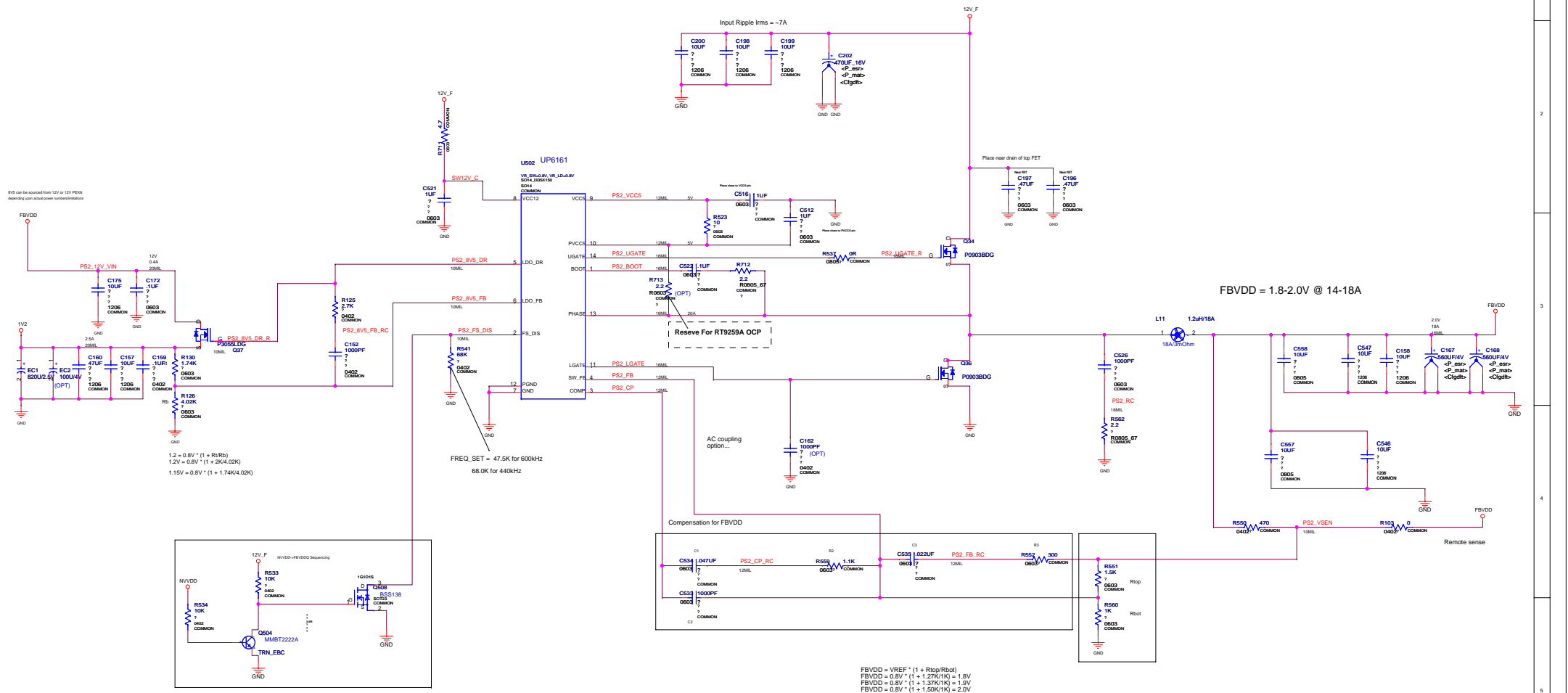
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PAGE DETAIL	Power Supply 5V, STEREO_5V, 2V5, DP_PWR

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5V, 2V5,			
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ASSEMBLY	P303 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 1V2, 1V8



[illegible]

ASSEMBLY	PJ93 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: FBVDDIQ, 8V5

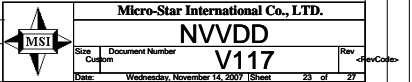


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FBVDD/VDDQ, 1V2

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ASSEMBLY	POWER - BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO-STEP ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply NVVDD Phase 1 & 2



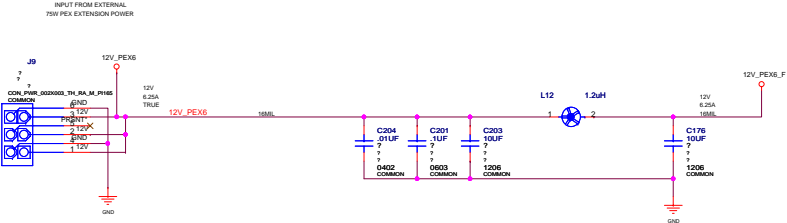
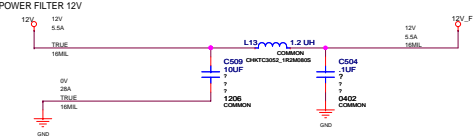
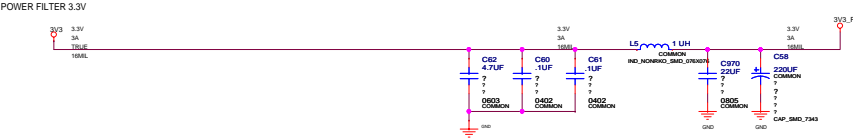
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ASSEMBLY	POWER - BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO-STEP ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply NVVDD Phase 1



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ASSEMBLY PAGE DETAIL P381-6A3E LEVEL 0 GENERIC SCHEMATIC ONLY COMMON & NO STUFF ASSEMBLY NOTES AND/NOT FINAL Power Supply: Filter/Detection of 3V3, 12V, 12V_PEX



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3V3,12V,12V_PEX
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Weak pull-ups needed for DCS:
* If SMBus is isolated from the GPU
* If MB does not support SMBus
* If MB does not support 3V3ALX

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ASSEMBLY	POWER - BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO-STEP ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply Hybrid Power



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