

C116-B, NV18B/NV31/NV34, 8MX16DDR, 128MB, Video IN/OUT, DVI-I, VGA

Page Overview

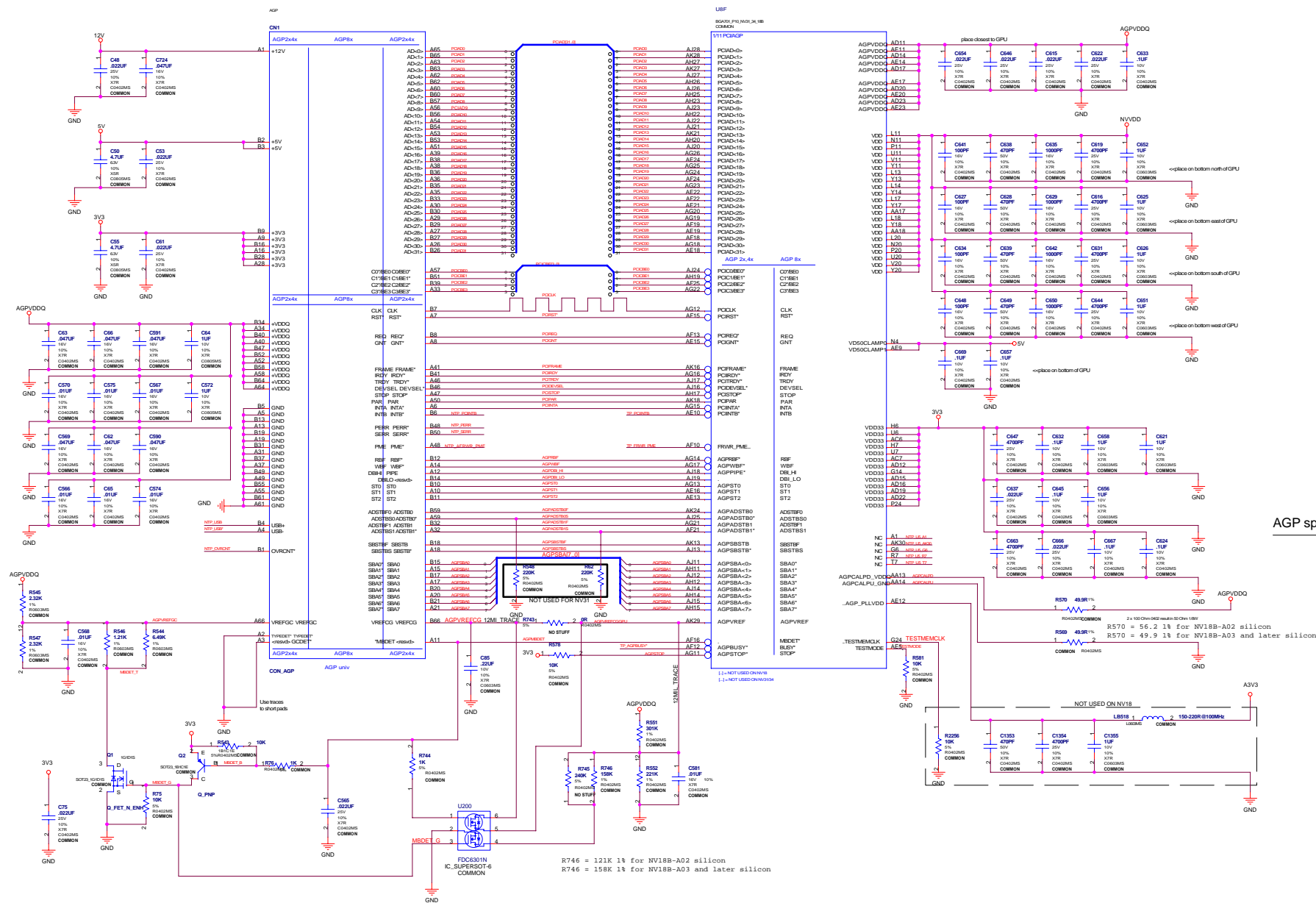
- 1 C116B PAGE OVERVIEW
- 2 NV18 AGP Section and AGP connector
- 3 NV18 FRAMEBUFFER Interface
- 4 MEMORY 128MB, 8Mx16DDR Bits 0..31
- 5 MEMORY 128MB, 8Mx16DDR Bits 32..63
- 6 MEMORY 128MB, 8Mx16DDR Bits 64..95
- 7 MEMORY 128MB, 8Mx16DDR Bits 96..127
- 8 NV18 STRAPPING, I/O Interface
- BIOS, FAN CONTROL, THERMAL SENSOR
- 9 NV18 DACA, DACB output, SYNC amplifier
- PLL Section
- 10 DACB MULTIPLEXER
- 11 PRIMARY DISPLAY Filter and Connector
- 12 SECONDARY DISPLAY Filter and Connector
- 13 NV18 INTERNAL TMDS Power and Output
- TMDS Backdrive circuit
- 14 PRIMARY DISPLAY DVI-I option
- Hotplug detection and Connector
- 15 VIDEO CAPTURE Philips 7114 I/O
- 16 VIDEO IN/OUT, Filter and Connector
- 17 VIDEO INTERNAL Input
- Filter and Connector
- 18 1394 TEXAS TSB41AB2, PowerRails,
- I/O, Internal and external connector
- 19 POWER SUPPLY
- NVVD, MEM_VDD, A3V3, TMDS3V3, TMDSP
- 20 MECHANICS, and FBVD

HISTORY:

- 00A: INITIAL VERSION
- ADD A.T.E. TEST POINTS
- ADD CIRCUIT TO SUPPORT NV34
- CONNECT W83785(U900) TO VGA THERMDA/C
- 00B: ADD FOUR COMMON CHOKES FOR EMI SOLUTION. PAGE 14.
- ADD FBVD SOURCE OPTION FROM FBVDQ. PAGE 18
- CHANGED FBVDQ FROM 2.6V TO 2.52V FOR NV34/P162. PAGE 17.
- 200: ADD SMART FAN CONTROL AND H/W MONITOR OPTION. PAGE 18.
- ADD IR CONTROLLER AND MODIFIED MINIDIN_9 CIRCUIT TO
- SUPPORT IR/TWIN BIOS SELECTION. PAGE 16
- CHANGED FBVDQ FROM 2.6V TO 2.52V. PAGE 17.

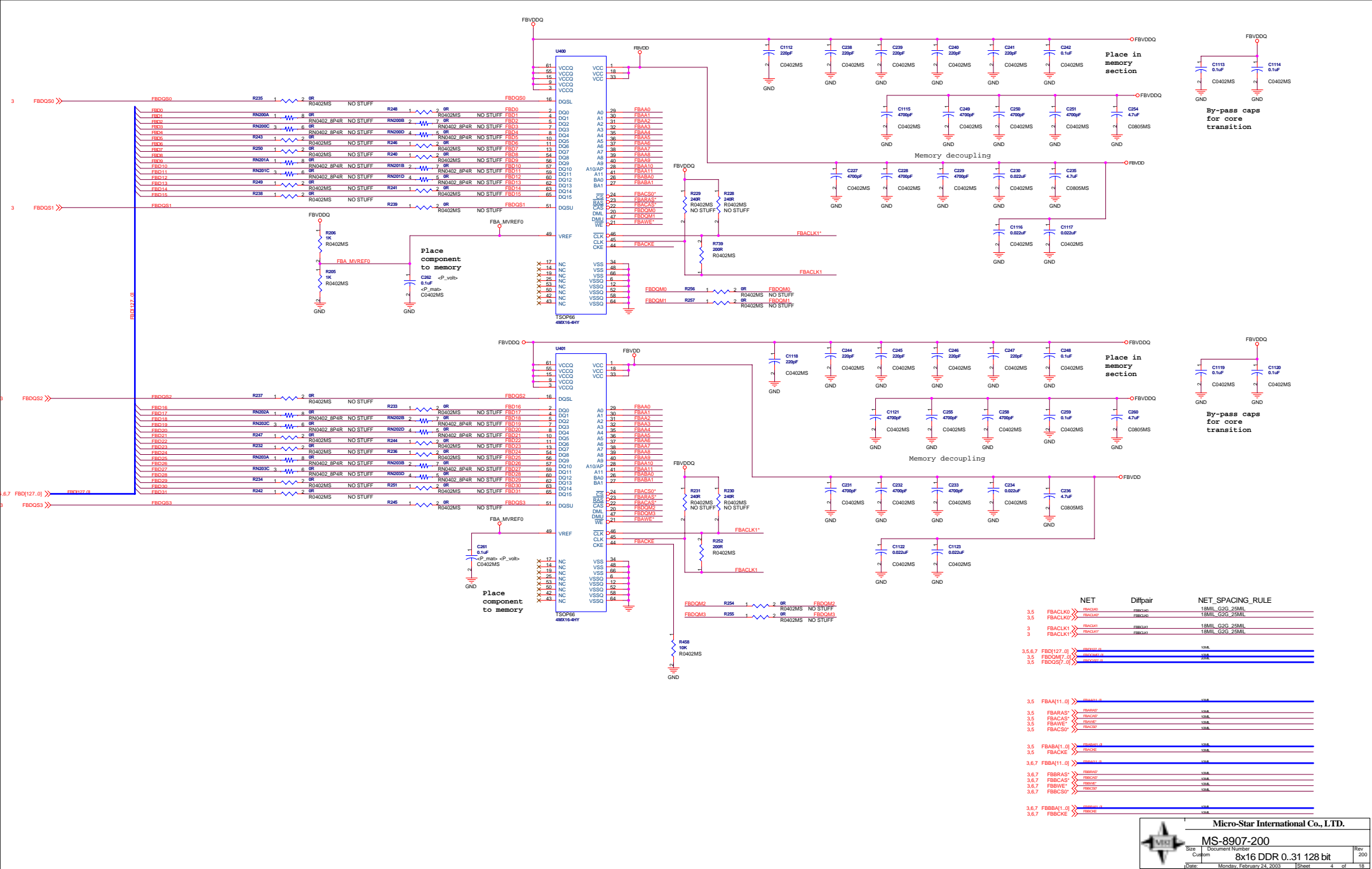
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS:
NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

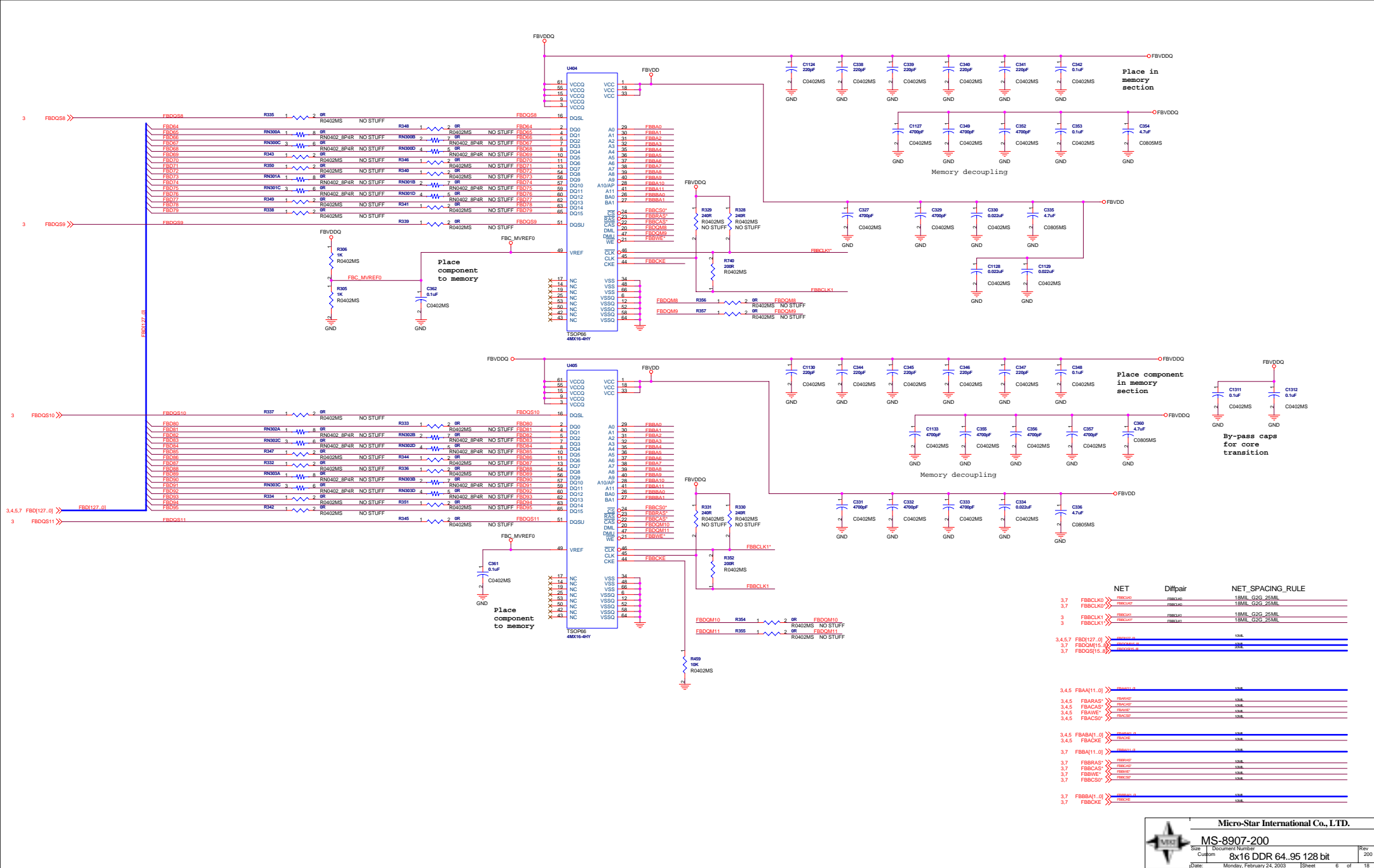
NV18 AGP SECTION AND AGP CONNECTOR



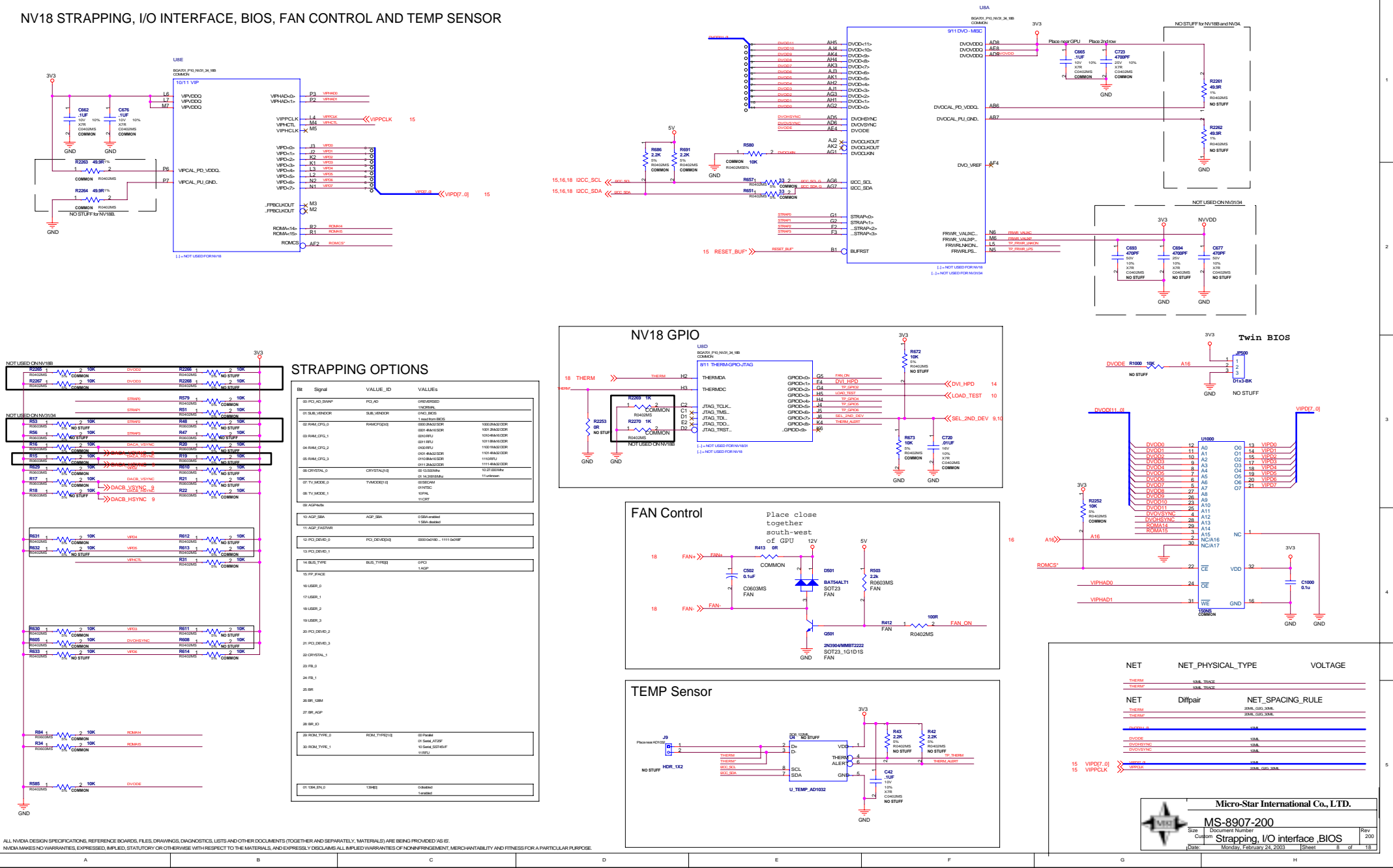
AGP spacing rules

AD9833-2	20.0
AD9833-4	20.0
AD9833-5	20.0
AD9833-6	20.0
AD9833-7	20.0
AD9833-8	20.0
AD9833-9	20.0
AD9833-10	20.0
AD9833-11	20.0
AD9833-12	20.0
AD9833-13	20.0
AD9833-14	20.0
AD9833-15	20.0
AD9833-16	20.0
AD9833-17	20.0
AD9833-18	20.0
AD9833-19	20.0
AD9833-20	20.0
AD9833-21	20.0
AD9833-22	20.0
AD9833-23	20.0
AD9833-24	20.0
AD9833-25	20.0
AD9833-26	20.0
AD9833-27	20.0
AD9833-28	20.0
AD9833-29	20.0
AD9833-30	20.0
AD9833-31	20.0
AD9833-32	20.0
AD9833-33	20.0
AD9833-34	20.0
AD9833-35	20.0
AD9833-36	20.0
AD9833-37	20.0
AD9833-38	20.0
AD9833-39	20.0
AD9833-40	20.0
AD9833-41	20.0
AD9833-42	20.0
AD9833-43	20.0
AD9833-44	20.0
AD9833-45	20.0
AD9833-46	20.0
AD9833-47	20.0
AD9833-48	20.0
AD9833-49	20.0
AD9833-50	20.0
AD9833-51	20.0
AD9833-52	20.0
AD9833-53	20.0
AD9833-54	20.0
AD9833-55	20.0
AD9833-56	20.0
AD9833-57	20.0
AD9833-58	20.0
AD9833-59	20.0
AD9833-60	20.0
AD9833-61	20.0
AD9833-62	20.0
AD9833-63	20.0
AD9833-64	20.0
AD9833-65	20.0
AD9833-66	20.0
AD9833-67	20.0
AD9833-68	20.0
AD9833-69	20.0
AD9833-70	20.0
AD9833-71	20.0
AD9833-72	20.0
AD9833-73	20.0
AD9833-74	20.0
AD9833-75	20.0
AD9833-76	20.0
AD9833-77	20.0
AD9833-78	20.0
AD9833-79	20.0
AD9833-80	20.0
AD9833-81	20.0
AD9833-82	20.0
AD9833-83	20.0
AD9833-84	20.0
AD9833-85	20.0
AD9833-86	20.0
AD9833-87	20.0
AD9833-88	20.0
AD9833-89	20.0
AD9833-90	20.0
AD9833-91	20.0
AD9833-92	20.0
AD9833-93	20.0
AD9833-94	20.0
AD9833-95	20.0
AD9833-96	20.0
AD9833-97	20.0
AD9833-98	20.0
AD9833-99	20.0
AD9833-100	20.0
AD9833-101	20.0
AD9833-102	20.0
AD9833-103	20.0
AD9833-104	20.0
AD9833-105	20.0
AD9833-106	20.0
AD9833-107	20.0
AD9833-108	20.0
AD9833-109	20.0
AD9833-110	20.0
AD9833-111	20.0
AD9833-112	20.0
AD9833-113	20.0
AD9833-114	20.0
AD9833-115	20.0
AD9833-116	20.0
AD9833-117	20.0
AD9833-118	20.0
AD9833-119	20.0
AD9833-120	20.0
AD9833-121	20.0
AD9833-122	20.0
AD9833-123	20.0
AD9833-124	20.0
AD9833-125	20.0
AD9833-126	20.0
AD9833-127	20.0
AD9833-128	20.0
AD9833-129	20.0
AD9833-130	20.0
AD9833-131	20.0
AD9833-132	20.0
AD9833-133	20.0
AD9833-134	20.0
AD9833-135	20.0
AD9833-136	20.0
AD9833-137	20.0
AD9833-138	20.0
AD9833-139	20.0
AD9833-140	20.0
AD9833-141	20.0
AD9833-142	20.0
AD9833-143	20.0
AD9833-144	20.0
AD9833-145	20.0
AD9833-146	20.0
AD9833-147	20.0
AD9833-148	20.0
AD9833-149	20.0
AD9833-150	20.0
AD9833-151	20.0
AD9833-152	20.0
AD9833-153	20.0
AD9833-154	20.0
AD9833-155	20.0
AD9833-156	20.0
AD9833-157	20.0
AD9833-158	20.0
AD9833-159	20.0
AD9833-160	20.0
AD9833-161	20.0
AD9833-162	20.0
AD9833-163	20.0
AD9833-164	20.0
AD9833-165	20.0
AD9833-166	20.0
AD9833-167	20.0
AD9833-168	20.0
AD9833-169	20.0
AD9833-170	20.0
AD9833-171	20.0
AD9833-172	20.0
AD9833-173	20.0
AD9833-174	20.0
AD9833-175	20.0
AD9833-176	20.0
AD9833-177	20.0
AD9833-178	20.0
AD9833-179	20.0
AD9833-180	20.0
AD9833-181	20.0
AD9833-182	20.0
AD9833-183	20.0
AD9833-184	20.0
AD9833-185	20.0
AD9833-186	20.0
AD9833-187	20.0
AD9833-188	20.0
AD9833-189	20.0
AD9833-190	20.0
AD9833-191	20.0
AD9833-192	20.0
AD9833-193	20.0
AD9833-194	20.0
AD9833-195	20.0
AD9833-196	20.0
AD9833-197	20.0
AD9833-198	20.0
AD9833-199	20.0
AD9833-200	20.0
AD9833-201	20.0
AD9833-202	20.0
AD9833-203	20.0
AD9833-204	20.0
AD9833-205	20.0
AD9833-206	20.0
AD9833-207	20.0
AD9833-208	20.0
AD9833-209	20.0
AD9833-210	20.0
AD9833-211	20.0
AD9833-212	20.0
AD9833-213	20.0
AD9833-214	20.0
AD9833-215	20.0
AD9833-216	20.0
AD9833-217	20.0
AD9833-218	20.0
AD9833-219	20.0
AD9833-220	20.0
AD9833-221	20.0
AD9833-222	20.0
AD9833-223	20.0
AD9833-224	20.0
AD9833-225	20.0
AD9833-226	20.0
AD9833-227	20.0
AD9833-228	20.0
AD9833-229	20.0
AD9833-230	20.0
AD9833-231	20.0
AD9833-232	20.0
AD9833-233	20.0
AD9833-234	20.0
AD9833-235	20.0
AD9833-236	20.0
AD9833-237	20.0
AD9833-238	20.0
AD9833-239	20.0
AD9833-240	20.0
AD9833-241	20.0
AD9833-242	20.0
AD9833-243	20.0
AD9833-244	20.0
AD9833-245	20.0
AD9833-246	20.0
AD9833-247	20.0
AD9833-248	20.0
AD9833-249	20.0
AD9833-250	20.0
AD9833-251	20.0
AD9833-252	20.0
AD9833-253	20.0
AD9833-254	20.0
AD9833-255	20.0
AD9833-256	20.0
AD9833-257	20.0
AD9833-258	20.0
AD9833-259	20.0
AD9833-260	20.0
AD9833-261	20.0
AD9833-262	20.0
AD9833-263	20.0
AD9833-264	20.0
AD9833-265	20.0
AD9833-266	20.0
AD9833-267	20.0
AD9833-268	20.0
AD9833-269	20.0
AD9833-270	20.0
AD9833-271	20.0
AD9833-272	20.0
AD9833-273	20.0
AD9833-274	20.0
AD9833-275	20.0
AD9833-276	20.0
AD9833-277	20.0
AD9833-278	20.0
AD9833-279	20.0
AD9833-280	20.0
AD9833-281	20.0
AD9833-282	20.0
AD9833-283	20.0
AD9833-284	20.0
AD9833-285	20.0
AD9833-286	20.0
AD9833-287	20.0
AD9833-288	20.0
AD9833-289	20.0
AD9833-290	20.0
AD9833-291	20.0
AD9833-292	20.0
AD9833-293	20.0
AD9833-294	20.0
AD9833-295	20.0
AD9833-296	20.0
AD9833-297	20.0
AD9833-298	20.0
AD9833-299	20.0
AD9833-300	20.0
AD9833-301	20.0
AD9833-302	20.0
AD9833-303	20.0
AD9833-304	20.0
AD9833-305	20.0
AD9833-306	20.0
AD9833-307	20.0
AD9833-308	20.0
AD9833-309	20.0
AD9833-310	20.0
AD9833-311	20.0
AD9833-312	20.0
AD9833-313	20.0
AD9833-314	20.0
AD9833-315	20.0
AD9833-316	20.0
AD9833-317	20.0
AD9833-318	20.0
AD9833-319	20.0
AD9833-320	20.0
AD9833-321	20.0
AD9833-322	20.0
AD9833-323	20.0
AD9833-324	20.0
AD9833-325	20.0
AD9833-326	20.0
AD9833-327	20.0
AD9833-328	20.0
AD9833-329	20.0
AD9833-330	20.0
AD9833-331	20.0
AD9833-332	20.0
AD9833-333	20.0
AD9833-334	20.0
AD9833-335	20.0
AD9833-336	20.0
AD9833-337	20.0
AD9833-338	20.0
AD9833-339	20.0
AD9833-340	20.0
AD9833-341	20.0
AD9833-342	20.0
AD9833-343	20.0
AD9833-344	20.0
AD9833-345	20.0
AD9833-346	20.0
AD9833-347	20.0
AD9833-348	20.0
AD9833-349	20.0
AD9833-350	20.0
AD9833-351	20.0
AD9833-352	20.0
AD9833-353	20.0
AD9833-354	20.0
AD9833-355	20.0
AD9833-356	20.0
AD9833-357	20.0
AD9833-358	20.0
AD9833-359	20.0
AD9833-360	20.0
AD9833-361	20.0
AD9833-362	20.0
AD9833-363	20.0
AD9833-364	20.0
AD9833-365	20.0
AD9833-366	20.0
AD9833-367	20.0
AD9833-368	20.0
AD9833-369	20.0
AD9833-370	20.0
AD9833-371	20.0
AD9833-372	20.0
AD9833-373	20.0
AD9833-374	20.0
AD9833-375	20.0
AD9833-376	20.0
AD9833-377	20.0
AD9833-378	20.0
AD9833-379	20.0
AD9833-380	20.0
AD9833-381	20.0
AD9833-382	20.0
AD9833-383	20.0
AD9833-384	20.0
AD9833-385	20.0
AD9833-386	20.0
AD9833-387	20.0
AD9833-388	20.0
AD9833-389	20.0
AD9833-390	20.0
AD9833-391	20.0
AD9833-392	20.0
AD9833-393	20.0
AD9833-394	20.0
AD9833-395	20.0
AD9833-396	20.0
AD9833-397	20.0
AD9833-398	20.0
AD9833-399	20.0
AD9833-400	20.0
AD9833-401	20.0
AD9833-402	20.0
AD9833-403	20.0
AD9833-404	20.0
AD9833-405	20.0
AD9833-406	20.0
AD9833-407	20.0
AD9833-408	20.0
AD9833-409	20.0
AD9833-410	20.0
AD9833-411	20.0
AD9833-412	20.0
AD9833-413	20.0
AD9833-414	20.0
AD9833-415	20.0
AD9833-416	20.0
AD9833-417	20.0
AD9833-418	20.0
AD9833-419	20.0
AD9833-420	20.0
AD9833-421	20.0
AD9833-422	20.0
AD9833-423	20.0
AD9833-424	20.0
AD9833-425	20.0
AD9833-426	20.0
AD9833-427	20.0
AD9833-428	20.0
AD9833-429	20.0
AD9833-430	20.0
AD9833-431	20.0
AD9833-432	20.0
AD9833-433	20.0
AD9833-434	20.0
AD9833-435	20.0
AD9833-436	20.0
AD9833-437	20.0
AD9833-438	20.0
AD9833-439	20.0
AD9833-440	20.0
AD9833-441	20.0
AD9833-442	20.0
AD9833-443	20.0
AD9833-444	20.0
AD9833-445	20.0
AD9833-446	20.0
AD9833-447	20.0
AD9833-448	20.0
AD9833-449	20.0
AD9833-450	20.0
AD9833-451	20.0
AD9833-452	20.0
AD9833-453	20.0
AD9833-454	20.0
AD9833-455	20.0
AD9833-456	20.0
AD9833-457	20.0
AD9833-458	20.0
AD9833-459	20.0
AD9833-460	20.0
AD9833-461	20.0
AD9833-462	20.0
AD9833-463	20.0
AD9833-464	20.0
AD9833-46	





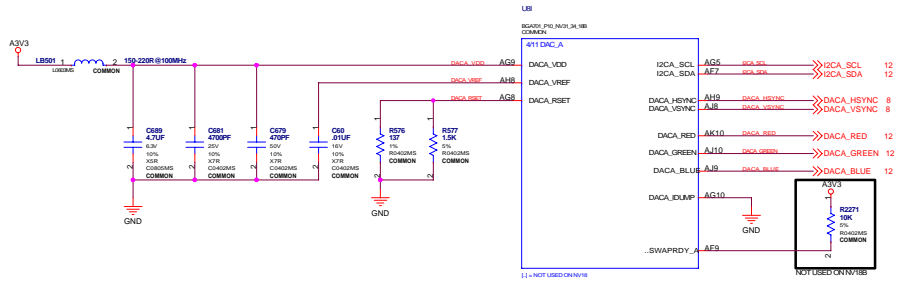
NV18 STRAPPING, I/O INTERFACE, BIOS, FAN CONTROL AND TEMP SENSOR



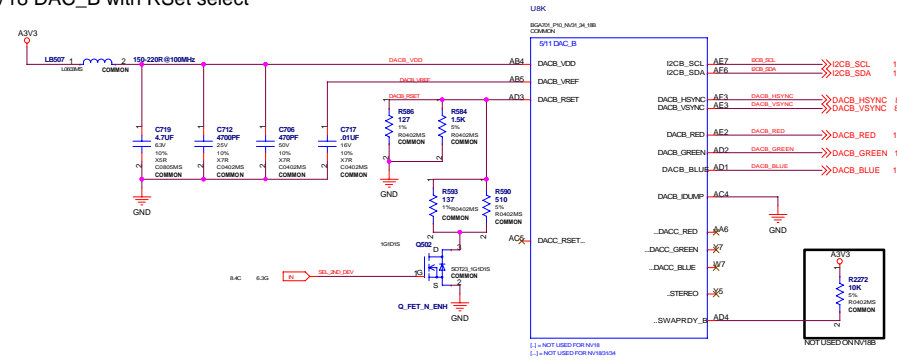
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

NV18 DAC_A, DAC_B, PLL, SYNC AMPL

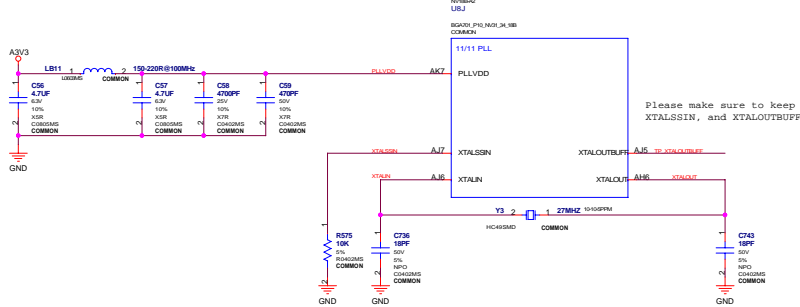
NV18 DAC_A



NV18 DAC_B with RSet select



NV18 PLL

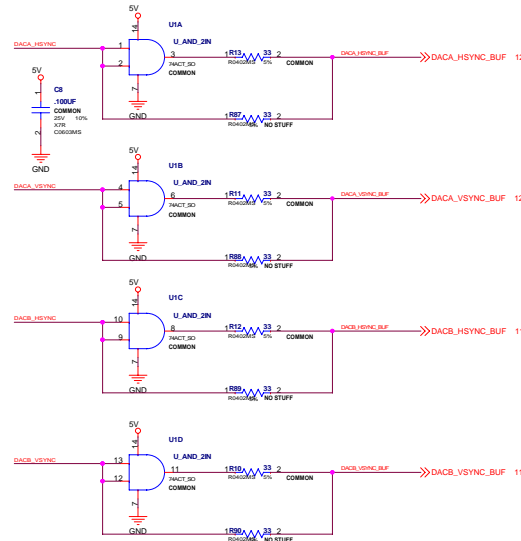


Please make sure to keep all components and nets related to pins XTALIN, XTALOUT, XTALSSIN, and XTALOUTBUFF away from everything else (place all on TOP).

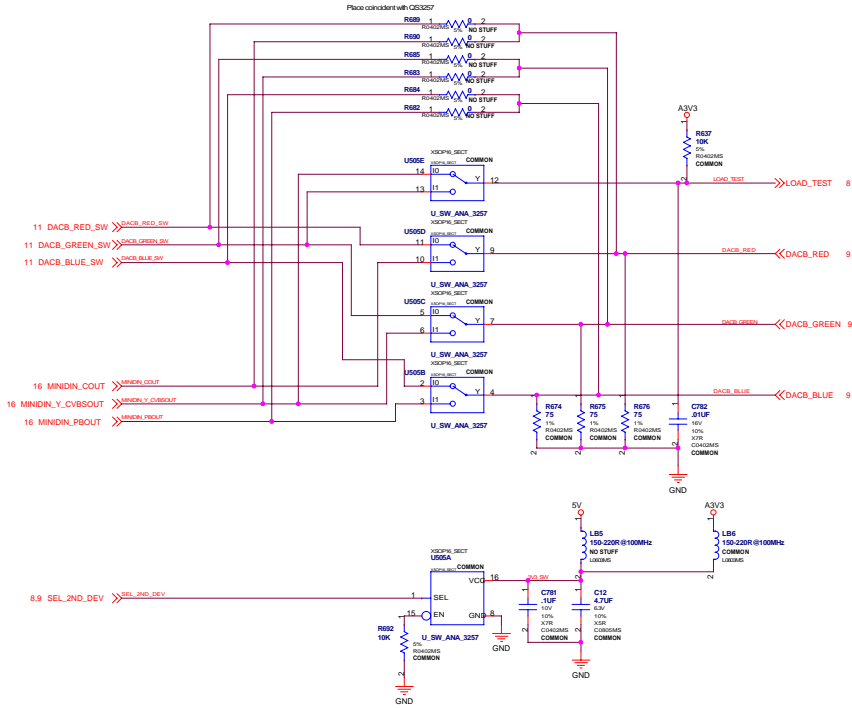
NET	NET_PHYSICAL_TYPE	VOLTAGE
DACA_VDD	12M_TRACE	3.3V
DACA_VREF	12M_TRACE	3.3V
DACA_VREF	12M_TRACE	3.3V
DACA_VREF	12M_TRACE	3.3V
DACA_VREF	12M_TRACE	3.3V
DACA_VREF	12M_TRACE	3.3V
DACA_VREF	12M_TRACE	3.3V
DACA_VREF	12M_TRACE	3.3V
DACA_VREF	12M_TRACE	3.3V
DACA_VREF	12M_TRACE	3.3V
PLL_VDD	12M_TRACE	3.3V

NET	IMPEDANCE	NET_SPACING_RULE
DACA_RED	37.5 OHM	20M_QSG_30M
DACA_GREEN	37.5 OHM	20M_QSG_30M
DACA_BLUE	37.5 OHM	20M_QSG_30M
DACA_RED	37.5 OHM	20M_QSG_30M
DACA_GREEN	37.5 OHM	20M_QSG_30M
DACA_BLUE	37.5 OHM	20M_QSG_30M

SYNC Amplifier




DACB SWITCH BETWEEN VGA OUT AND TV OUT



NET	IMPEDANCE	NET_SPACING_RULE
11 DACB_RED_SW	37.5 OHM	20MIL_GST_20MIL
11 DACB_GREEN_SW	37.5 OHM	20MIL_GST_20MIL
11 DACB_BLUE_SW	37.5 OHM	20MIL_GST_20MIL
16 MININ_COUT	37.5 OHM	20MIL_GST_20MIL
16 MININ_Y_CVBSOUT	37.5 OHM	20MIL_GST_20MIL
16 MININ_PBOUT	37.5 OHM	20MIL_GST_20MIL

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS:
NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

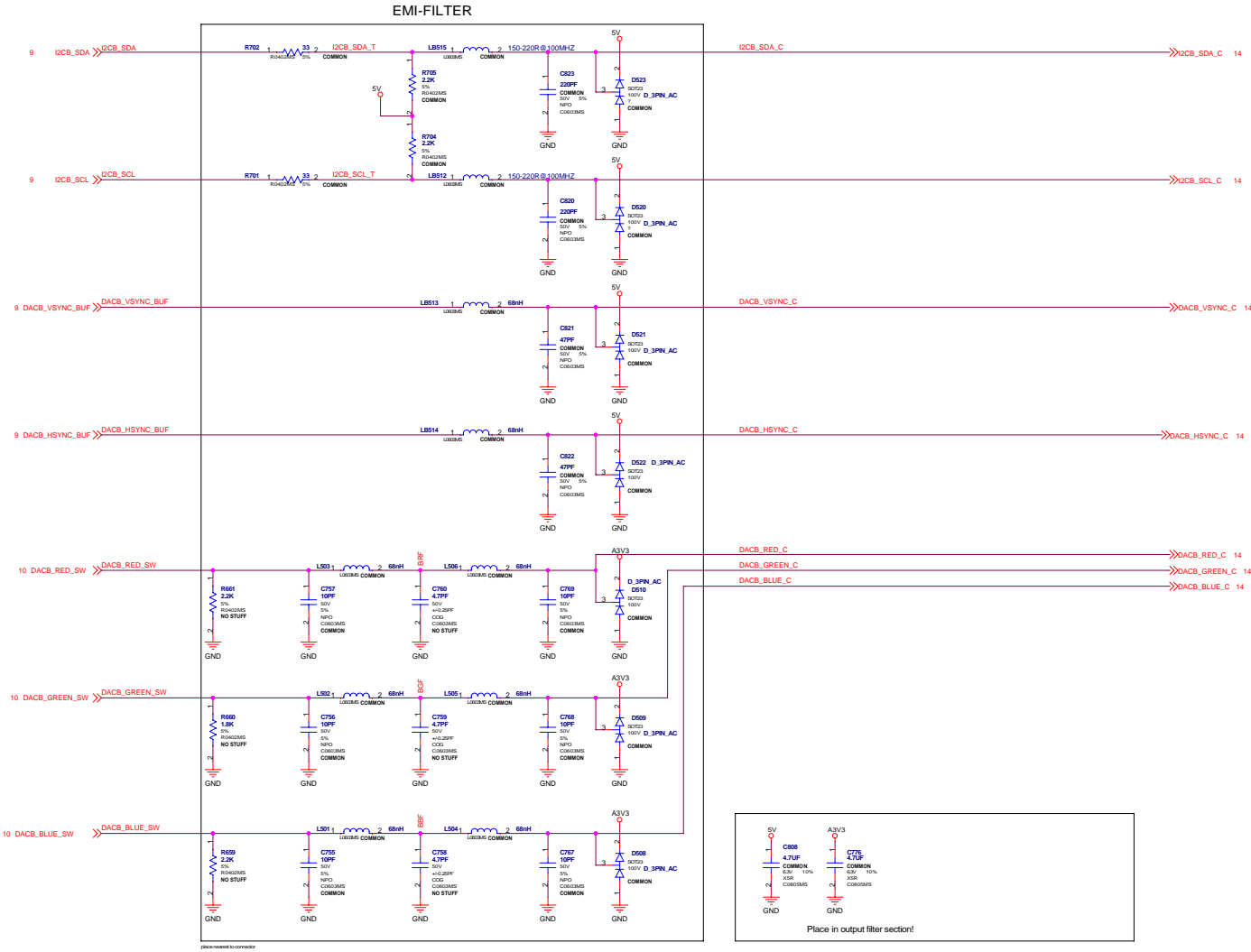


Micro-Star International Co., LTD.

MS-8907-200


Size: Document Number
Custom: SWITCH BETWEEN VGA AND TV-OUT
Date: Monday, February 23, 2003 Sheet: 10 of 18

DACB output



NET	IMPEDANCE	NET_SPACING_RULE
SDA	37.5 OHM	200.000.000.000
SOL	37.5 OHM	200.000.000.000
SYNC	37.5 OHM	200.000.000.000
DACB_RED_C	10MIL TRACE	200.000.000.000
DACB_GREEN_C	10MIL TRACE	200.000.000.000
DACB_BLUE_C	10MIL TRACE	200.000.000.000

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS:
NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.



Micro-Star International Co., LTD.

MS-8907-200

Document Number

Rev 200

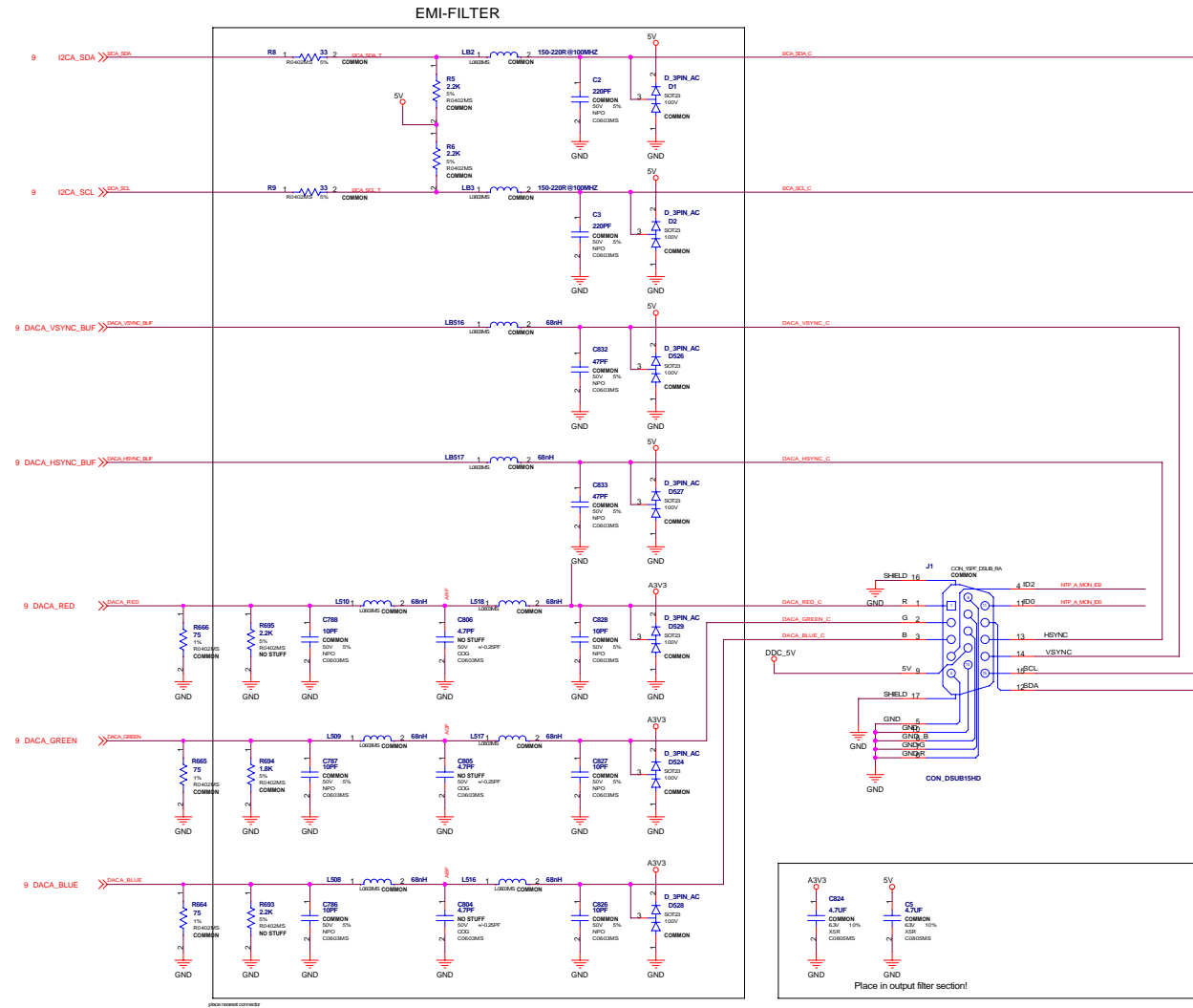
Size Custom

DAC B CONNECT

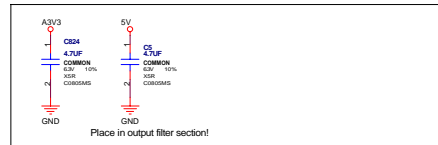
Date Monday, February 23, 2009

Sheet 11 of 18

DACB output

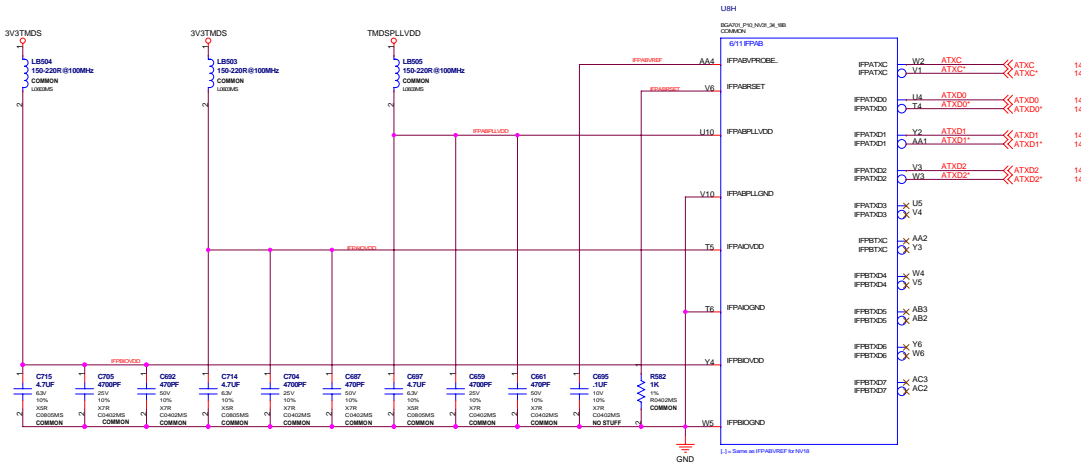


NET	IMPEDANCE	NET_SPACING_RULE
REF	37.5 OHM	20MIL 20G 30MIL
PCB	37.5 OHM	20MIL 20G 30MIL
REF	37.5 OHM	20MIL 20G 30MIL
DACA_RED_C	10MIL TRACE	20MIL 20G 30MIL
DACA_GREEN_C	10MIL TRACE	20MIL 20G 30MIL
DACA_BLUE_C	10MIL TRACE	20MIL 20G 30MIL

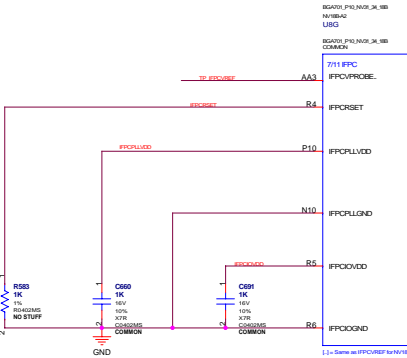
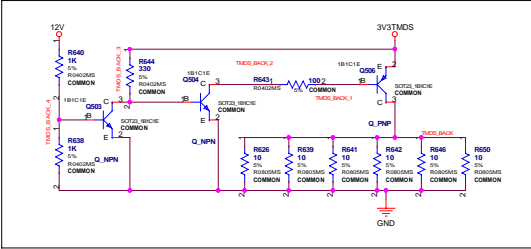


INTERNAL TMDS POWER AND DECOUPLING

NET	NET_PHYSICAL_TYPE	VOLTAGE
IFPABUSE	USB_TRACE	3.3V
IFPABLLVD	USB_TRACE	3.3V
IFPABVDD	USB_TRACE	3.3V
IFPABVDD2	USB_TRACE	3.3V
IFPABVDD3	USB_TRACE	3.3V
IFPABVDD4	USB_TRACE	3.3V
IFPABVDD5	USB_TRACE	3.3V
IFPABVDD6	USB_TRACE	3.3V
IFPABVDD7	USB_TRACE	3.3V
IFPABVDD8	USB_TRACE	3.3V

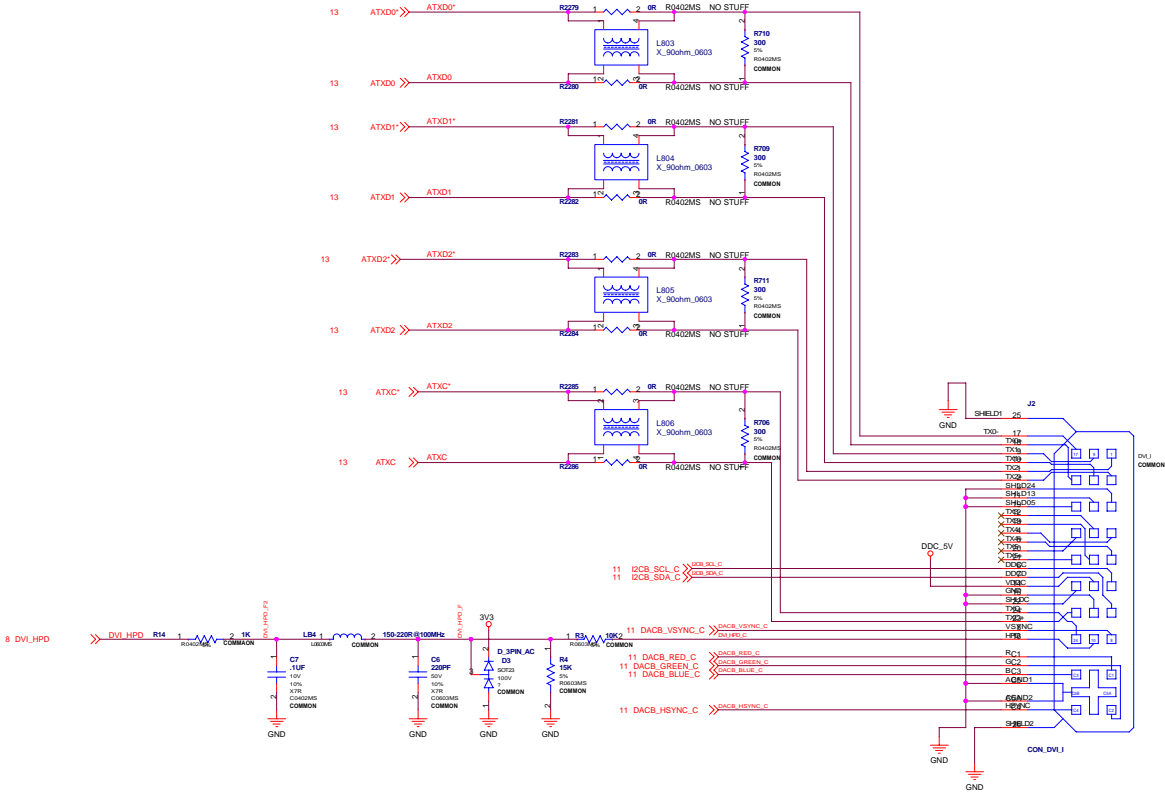


TMDS backdrive prevention




ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

DVI_I OUTPUT



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS:
NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.



Micro-Star International Co., LTD.

MS-8907-200

Size: Custom

Document Number: DVI CONNECT

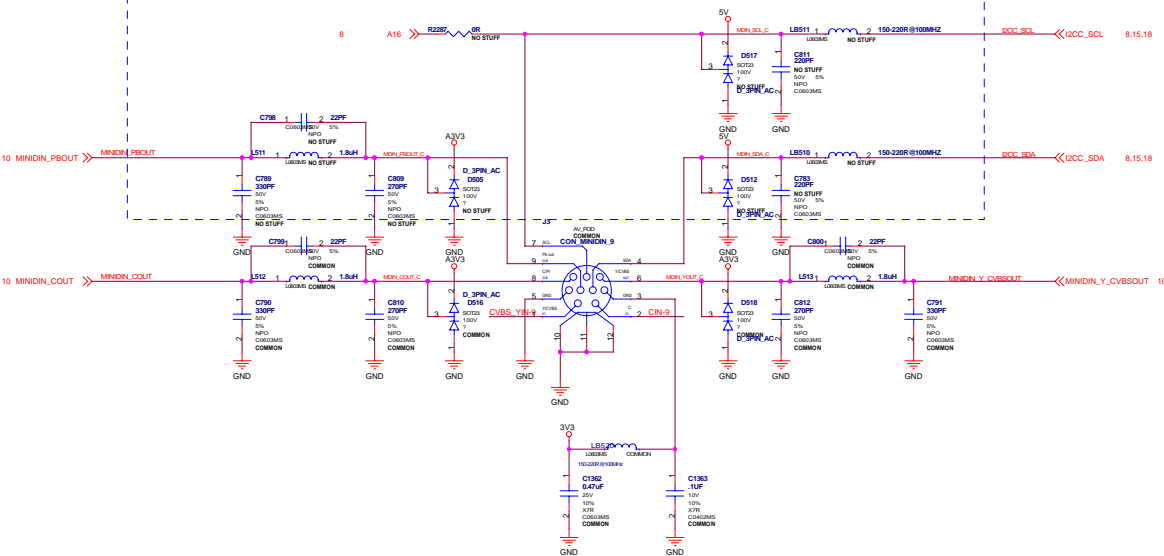
Date: Monday, February 23, 2003

Rev: 200

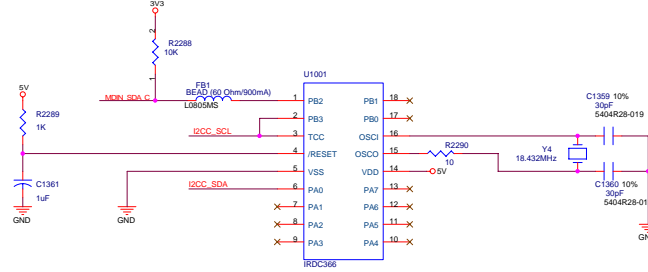
Sheet: 14 of 18

VIDEO IN/OUT CONNECTOR

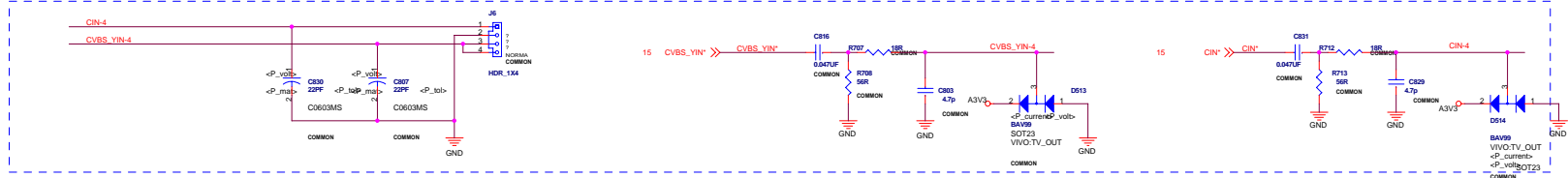
FOR 9 PIN VIVO CONNECTOR




IR Function



FOR 4 PIN VIDEO IN CONNECTOR (option)





Micro-Star International Co., LTD.

MS-8907-200

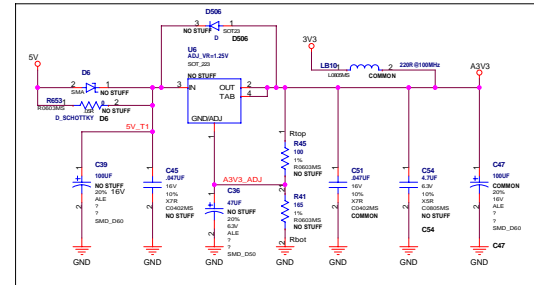
Size: Custom, Document Number: VIDEO IN/OUT CONNECT, Rev: 200

Date: Monday, February 23, 2003, Sheet: 16 of 18

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS: NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

POWER
SUPPLY

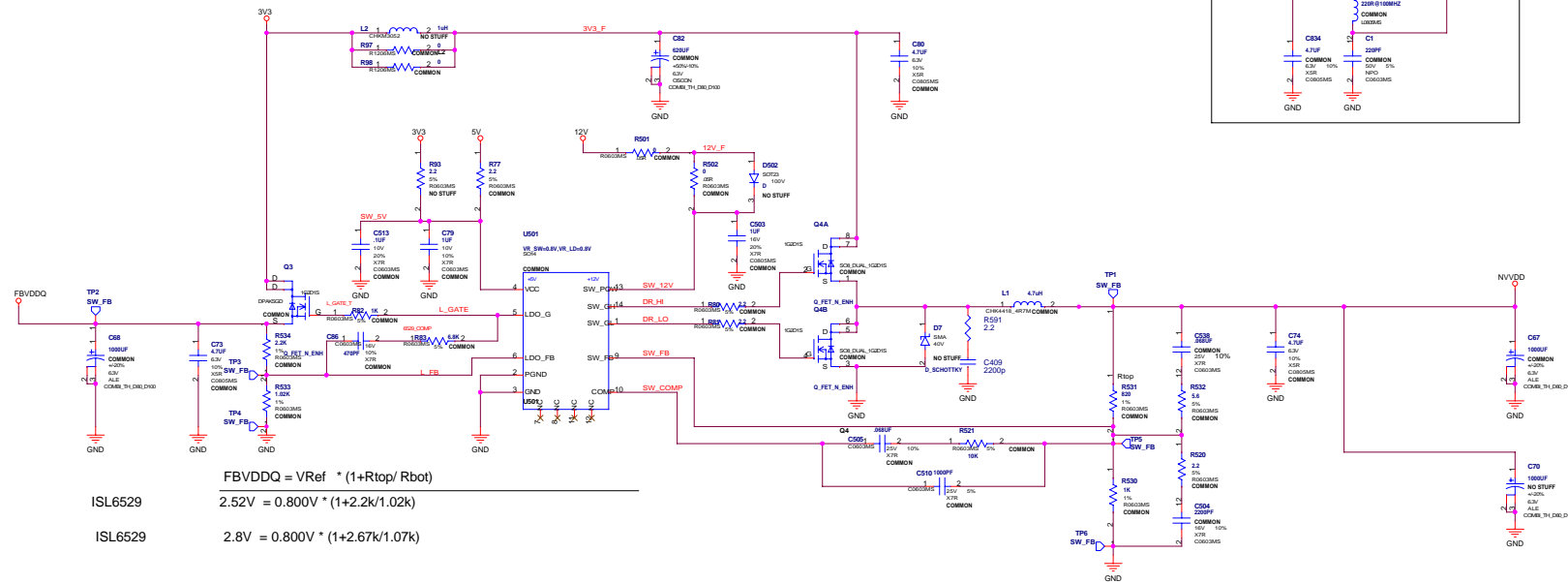
ANALOG 3V3



$$V_{out} = V_{Ref} * (1 + R_{bot}/R_{top})$$

$$3.31V = 1.25V * (1 + (165/100))$$

NVDD-SWITCHER / FBVDD-LDO CONTROLER ISL6529



$$FBVDDQ = V_{Ref} * (1 + R_{top} / R_{bot})$$

$$\text{ISL6529} \quad 2.52\text{V} = 0.800\text{V} * (1 + 2.2\text{k}/1.02\text{k})$$

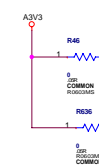
ISL6529 $2.8V = 0.800V * (1+2.67k/1.07k)$

$$NVDD = V_{Ref} * (1 + R_{top} / R_{bot})$$

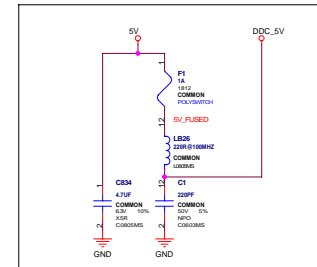
ISL6529

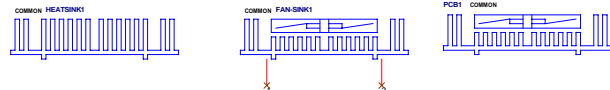
$$1.656V = 0.800V * (1 + 1070/1000)$$

TMDS 3V3 Supply
TMDS PLL Supply

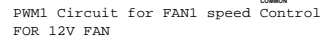


DDC 5V

[illegible]



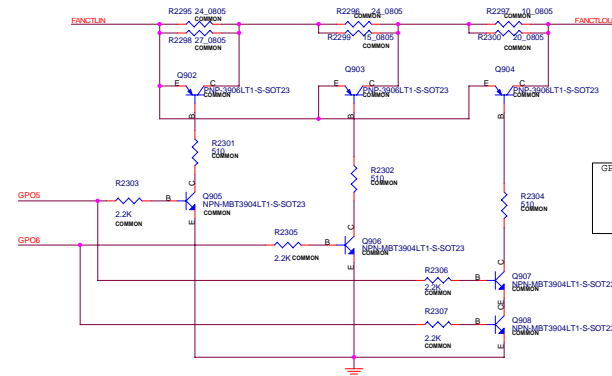
NO STUFF
EXCEPT J7



AGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS," WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE COPYRIGHT OWNER OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

The schematic diagram illustrates the power supply section of the TTP7 SW. It begins with a 5V input connected to a network of capacitors (C1147, C1148, C1149) and resistors (R57, R58, R79) to filter and regulate the voltage. A 7805 voltage regulator (Q557) is used to provide a stable 5V output (FBVDD). The output is further filtered by capacitors C1150 and C1151. The final output is connected to the FBVDD pin of the TTP7 SW.

$$3.300V = 1.250V * (1 + 187/115)$$



GPO5	GPO6	Q1	Q2	Q3	Vout
0	0	off	off	off	9V
1	0	on	off	off	10V
0	1	off	on	off	11V
1	1	on	on	on	12V