P70, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, video capture, stereo, AGP4X

PCI DEVICE ID 0X0=0X171 FOR NV17-128D.

HISTORY:

X00:
first version for layout start. No video capture, no stereo. NO DRC CHECK.

X01:
fixed PCB footprints for IC_SO14_150MIL and CON_DVI-I_RA
added end-termination r-packs for address-status-bus
changed RGB filter to integrated 5-pole only
added video capture, BIOS, Strapping
changed RefDes
NO DRC CHECK

X02:
added missing end termination for FBBAx
changed stereo 3pin header
added clamp diodes for TV-out and video capture
changed topology for 2nd DDC (VGA / DVI)
NO DRC CHECK

X03:
splitted analog/digital suply for SAA7113 (no component change)
Fixed some RefDes
Changed the strapping resistors cases to 0402
NO DRC CHECK

X04:
changed C617 to SMD0603
changed U502 and U503 to TSSOP14
added CKE connection to the memories
added D505 to the stereo section
changed L501, L502, L503 to 0603
NO DRC CHECK

X05:
changed U601 to SOT223-DPAK-D2PAK
added bracket
changed L600 to IND_CDR73
added VIP connector
NO DRC CHECK

X06:
deleted VIP
changed TPs to HOLE_48C28P
changed switcher gate circuit (no component change)
added C641 and C642 to the linear voltage regulator
pinswap of memory termination
NO DRC CHECK

X07:
deleted page 10: 5.b ViVo
changed filter topology for RGB
added return traces for RGB
NO DRC CHECK

X08:
added TV filter caps with reference to GND (C511,C517,C522)
separated RGB returns (NOTE: there will be a change for DAC2)
NO DRC CHECK

X09:
added net names to unused panel signals (test points)
NO DRC CHECK

X10:
added decoupling for DVO rail (C529 and C530)
added GND connection to pin 1 of U700
added R520 pull down for DVOCLKIN
DRC CHECK DONE

X11:
changed caps in power section to the combined footprints

X12:
data bus swappings

X13:
swapped CLKs for U201 and U202

X14:
connected the RGB returns of VGA2 together

X15:
update materials

X16:
update stuffings

X17-A01:
release A01
changed DVOVDD from VID3.3V to A3.3V
add linear regulator for NV17's VDD33
connected the IFP-RSETs to GND
deleted C134 and C135

X18:
change to target release A02
changed I2C assignments
added I2C filter components for ViVo (L506,L507,R521-R524,D506,D507,C531,C532)

X19:
added R243-R250 for clock pull-up.

X20-A02:
material changes.

X21-A03:
fixed values and descriptions for R609, R613 and C640
changed the RGB filter topology:
- delete R325-R330
- connect all DACRTN to GND
- move the 75R termination resistors to the connector
changed RGB clamping to A3.3V
add testpoint net XTALOUTBUFF
changed XTAL-load caps C320 and C321 to 18pF
removed obsolete 0603 0Ohm resistors
NO_STUFFed the stereo 3-pin header.

X22-A03:
changed bulk decoupling in VGA section from 3.3V to A3.3V
fixed DAC1BLUE (net name was missing)

X23-A03:
changed VDD33 to A3.3V

X24-A03:
added C643 for memory core decoupling

X25-A03:
changed the long body VGA connector to a three pin type
changed C425 connection for fan decoupling

PAGE OVERVIEW

1 top (this) page
2 1. AGP interface, core decoupling
3 2.a NV17 Frame Buffer
4 2.b Frame Buffer 0..63
5 2.b Frame Buffer 64...127
6 3.a Dual DAC, 1st VGA
7 3.b Dual DAC, 2nd VGA
8 4. Panel
9 5.a TV-out, video capture, stereo
10 6. Power supply
11 7. BIOS, Strapping

Stuffing Options	Meaning
COMMON	common components for all skus
NO_STUFF	no assembly at all
XTAL_27	stuff the 27MHz xtal for the GPU
XTAL_14	stuff the 14.318MHz xtal for the GPU
VIVO	stuff video I/O
VIDCAP	stuff video capture
TV_OUT	stuff TV-out
DVI-I	stuff the DVI-I option
DVI	stuff the DVI-D option
2NDVGA	stuff a second VGA
NO_DVI	don't stuff any DVI
SYNC_DRIVER2	stuff the termination resistors for the DACB syncs
SYNC_DRIVER	stuff the sync driver chip
NO_SYNC_DRIVER2	bypass the sync driver for the DAC B syncs
NO_SYNC_DRIVER	bypass the sync driver for the DAC A syncs
STEREOSYNCS	stuff the switchable stereo sync circuit
STEREOSYNC2	sync stereo to DAC B
STEREOSYNC1	sync stereo to DAC A
STEREO	stuff the generic stereo circuit
SI2C_PROT	stuff the protection diodes for syncs and I2C at DAC A
RGB_PROT	stuff the protection diodes for RGB at DAC A
2NDVGA_RGB_PROT	stuff the protection diodes for RGB at DAC B
2NDSI2C_PROT	stuff the protection diodes for syncs and I2C at DAC B
SET_NVVDD_ISL	set NVVDD voltage at Intersil switcher
SET_NVVDD_IRU	set NVVDD voltage at IR/Uniseml switcher
SET_FBVDDQ_ISL	set FBVDDQ voltage at Intersil switcher
SET_FBVDDQ_IRU	set FBVDDQ voltage at IR/Uniseml switcher
NO_1117	bypass the A3.3V regulator to AGP3.3V
ISL	stuff the Intersil switcher
IRU	stuff the IR/Unisem switcher
FBVDD_3.3	connect FBVVDD with AGP3.3V
FBVDD_2.5	connect FBVVDD with FBVDDQ
1117_ADJ	stuff the adjustable regulator for A3,3V
1117	stuff the fixed regulator for A3,3V
PASSIVE_HS	have passive heatsink
FAN	fan sink and components
BRCKT_VGA_TV_VGA	Bracket VGA-TV-VGA
BRCKT_VGA_TV_DVI	Bracket VGA-TV-DVI
BRCKT_VGA_TV	Bracket VGA-TV
BRCKT_VGA	Bracket VGA
MEMSTRAP1111	strap memory to 1111
MEM-64B	stuff 64 bit memory - 2pcs
MEM-128B	stuff 128 bit memory - 4pcs
NV17-128D	stuff NV17-128D

140-10070-0000-A03
602-10070-0000-A03

NVIDIA Corporation
3535 Monroe St
Santa Clara, CA 95051, USA

P70, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, video capture, stereo, AGP4x

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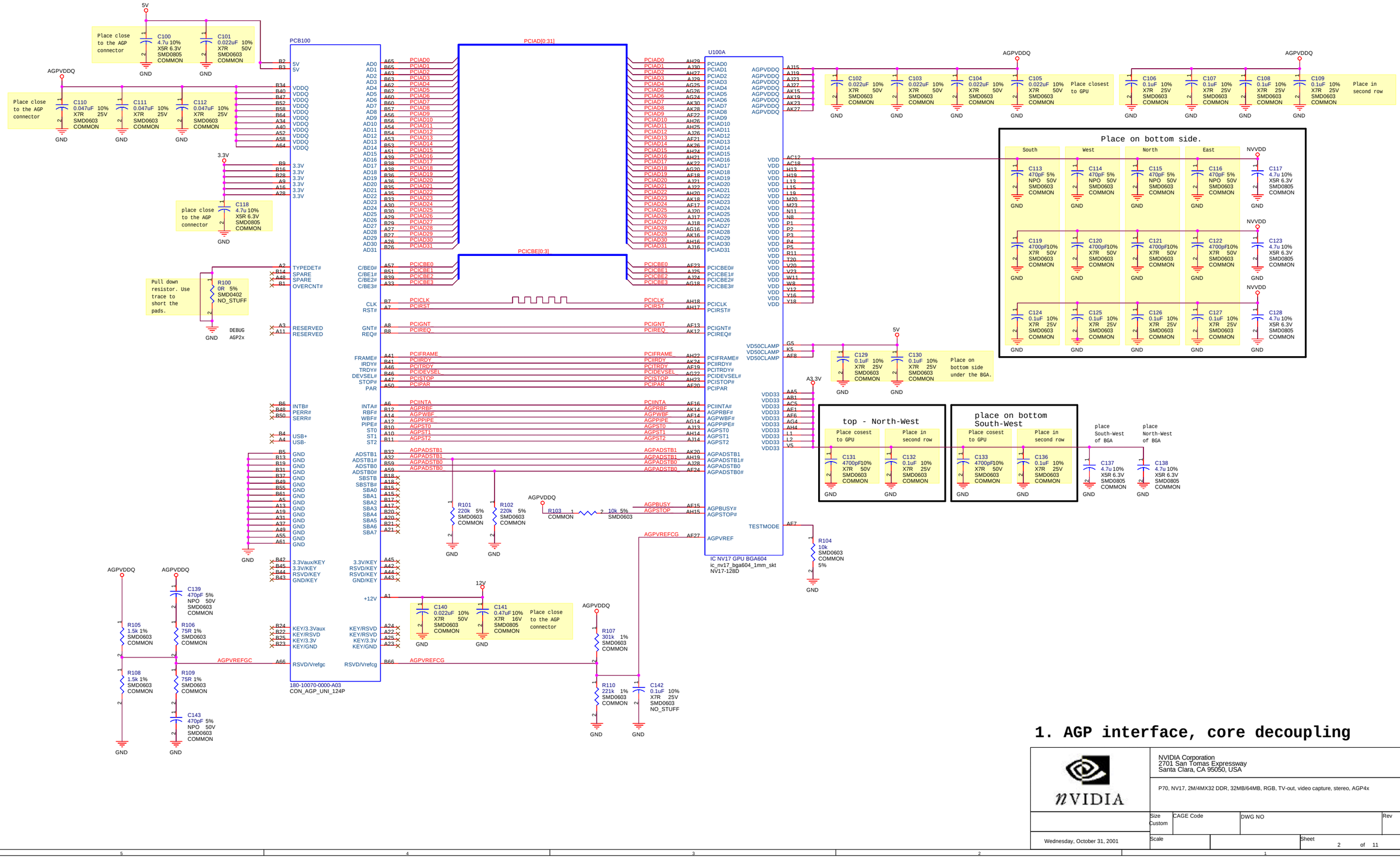
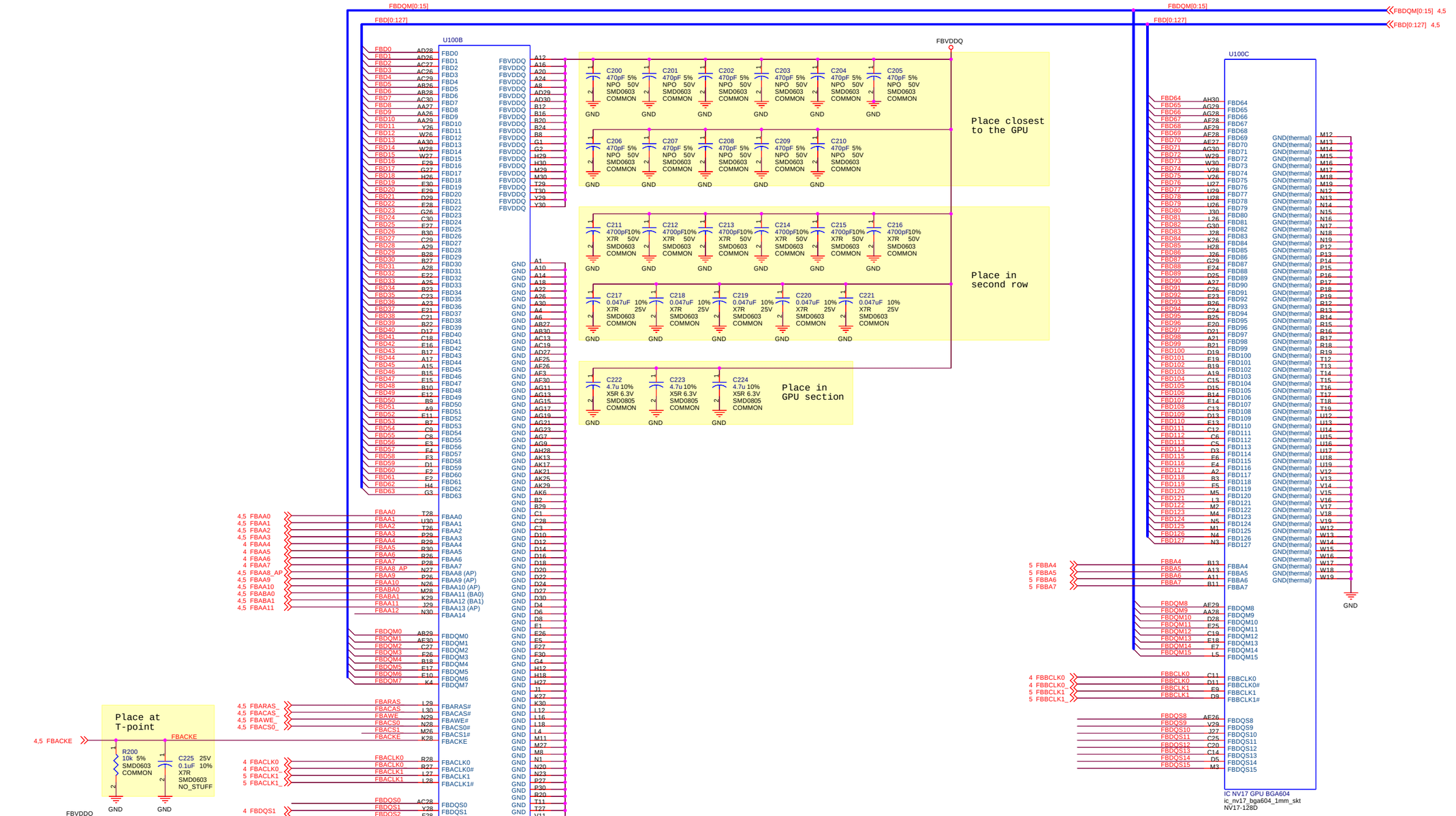
```
Item\tQty\tRefDes\tDescription\tAssembly\tNVPN\tNotes\tValue\tParam_voltage\tParam_material\tParam_tolerance\tParam_power\tParam_esr\tParam_ripple\tParam_current\tPCB Footprint
{Item}\t{Qty}\t{Reference}\t{Description}\t{Assembly}\t{NVPN}\t{Notes}\t{Value}\t{P_volt}\t{P_mat}\t{P_tol}\t{P_pow}\t{P_esr}\t{P_ripple}\t{P_current}\t{PCB Footprint}
```


PCB100
U100A
PCIAD[0:31]
PCICBE[0:3]
IC NV17 GPU BGA604
ic_nv17_bga604_1mm_skt
NV17-128D
180-10070-0000-A03
CON_AGP_UNI_124P
Place close to the AGP connector
Pull down resistor. Use trace to short the pads.
DEBUG AGP2x
Place on bottom side.
Place on bottom side under the BGA.
Place closest to GPU
Place in second row
top - North-West
place on bottom South-West
Place cosest to GPU
Place in second row
place South-West of BGA
place North-West of BGA
1. AGP interface, core decoupling
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P70, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, video capture, stereo, AGP4x
Wednesday, October 31, 2001
Sheet 2 of 11



2.a NV17 Frame Buffer

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Santa Clara, CA 95050, USA

P70, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, video capture, stereo, AGP4x

	Size Custom	CAGE Code	DWG NO	Rev
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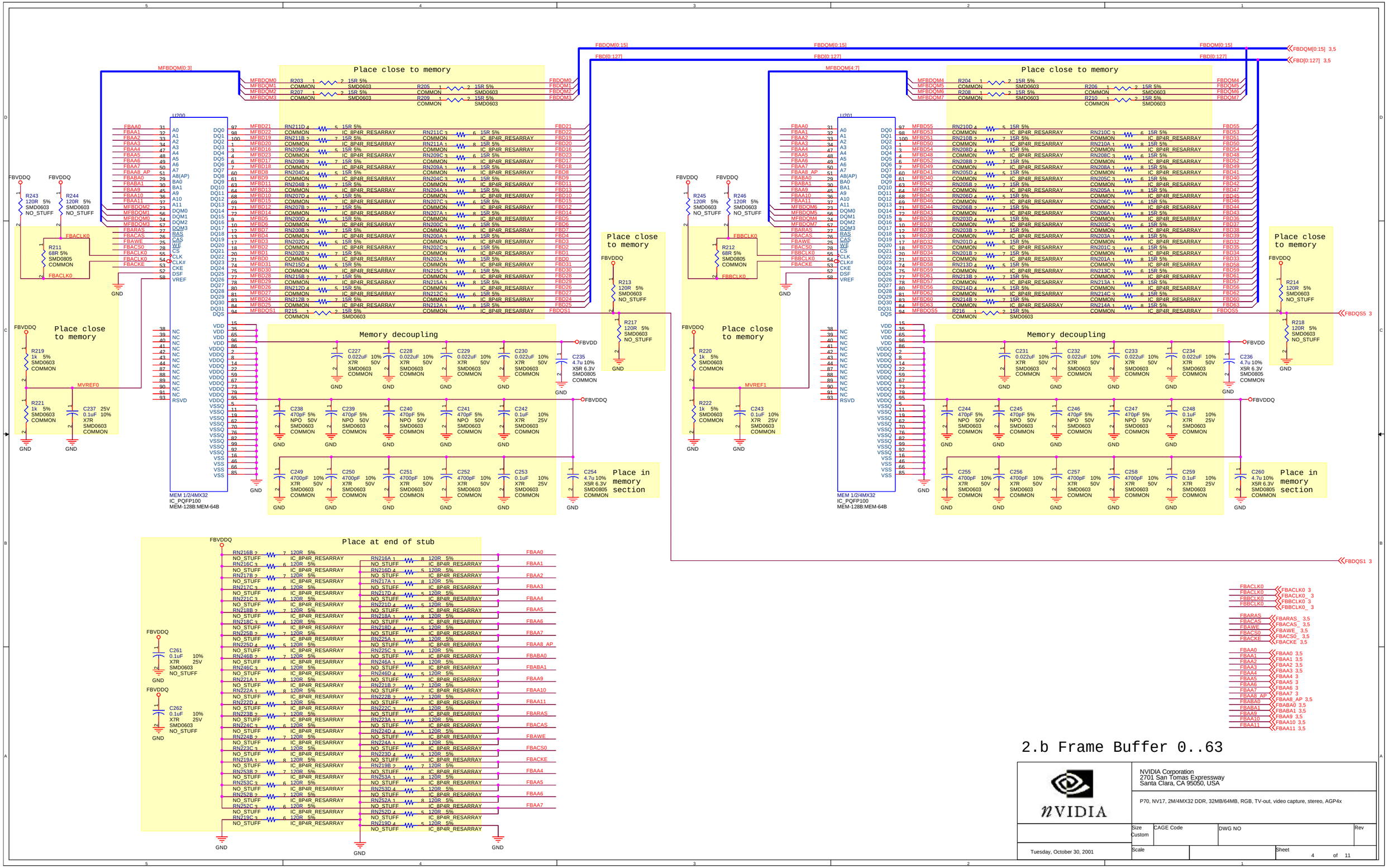
Place close to memory
Memory decoupling
Place close to memory
Place close to memory
Memory decoupling
Place close to memory
Place close to memory
Place close to memory
Place close to memory
Place in memory section
Place in memory section
Place at end of stub
MFBDQM[0:3]
FBDQM[0:15]
FBD[0:127]
MFBDQM[4:7]
FBDQM[0:15]
FBD[0:127]
FBDQM[0:15] 3,5
FBD[0:127] 3,5
U200
U201
MEM 1/2/4MX32
IC_PQFP100
MEM-128B:MEM-64B
FBVDDQ
GND
FBACLK0
FBBCLK0
MVREF0
MVREF1
FBDQS1 3
FBDQS5 3
2.b Frame Buffer 0..63
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2701 San Tomas Expressway
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P70, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, video capture, stereo, AGP4x
Size Custom
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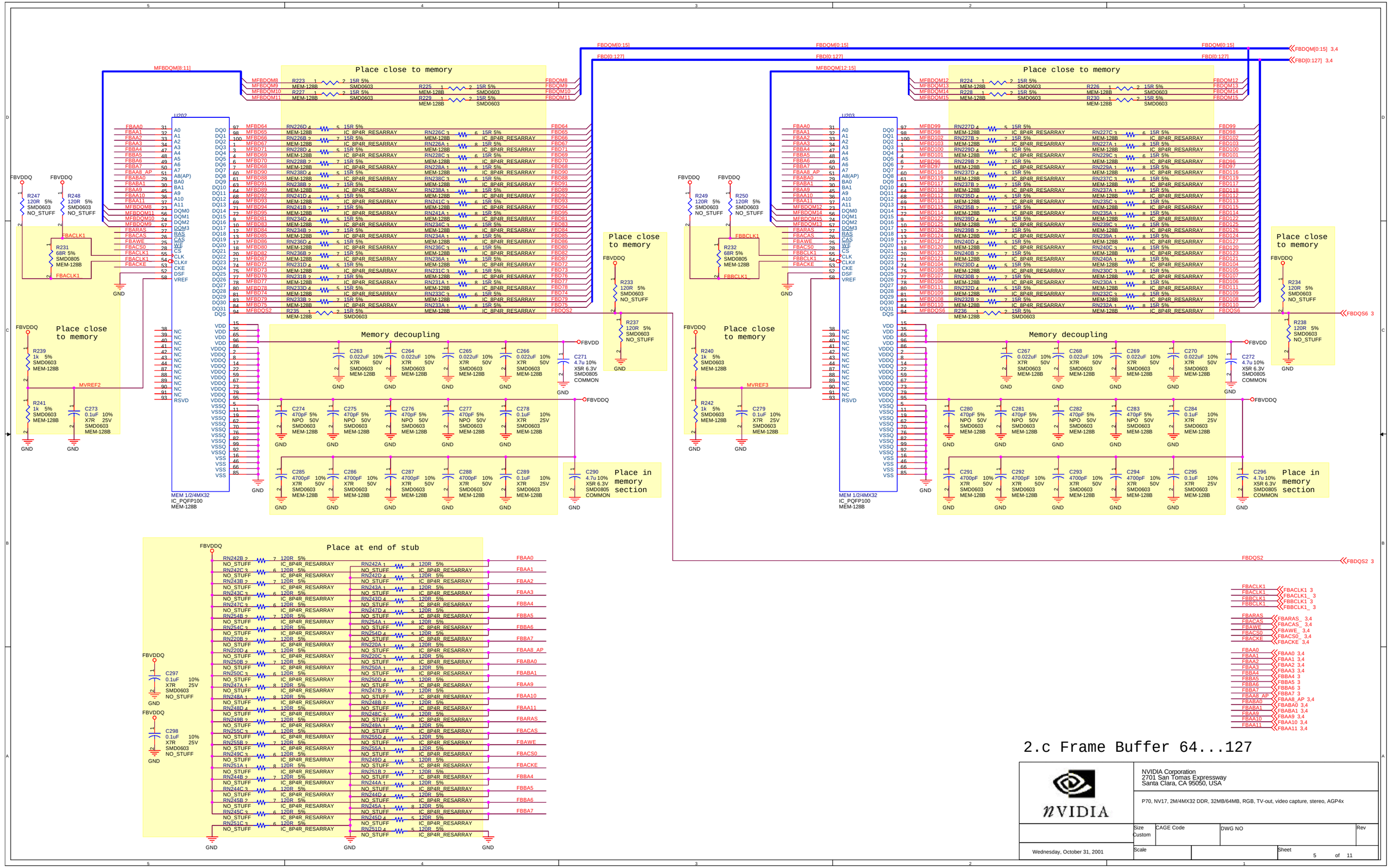
Place close to memory
Memory decoupling
Place close to memory
Place close to memory
Place close to memory
Memory decoupling
Place close to memory
Place close to memory
Place in memory section
Place in memory section
Place at end of stub
U202
U203
MEM 1/2/4MX32
IC_PQFP100
MEM-128B
MFBDQM[8:11]
MFBDQM[12:15]
FBDQM[0:15]
FBD[0:127]
FBVDDQ
GND
MVREF2
MVREF3
FBACLK1
FBBCLK1
FBDQS2
2.c Frame Buffer 64...127
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P70, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, video capture, stereo, AGP4x
Wednesday, October 31, 2001
Size Custom
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3.a Dual DAC, 1st VGA

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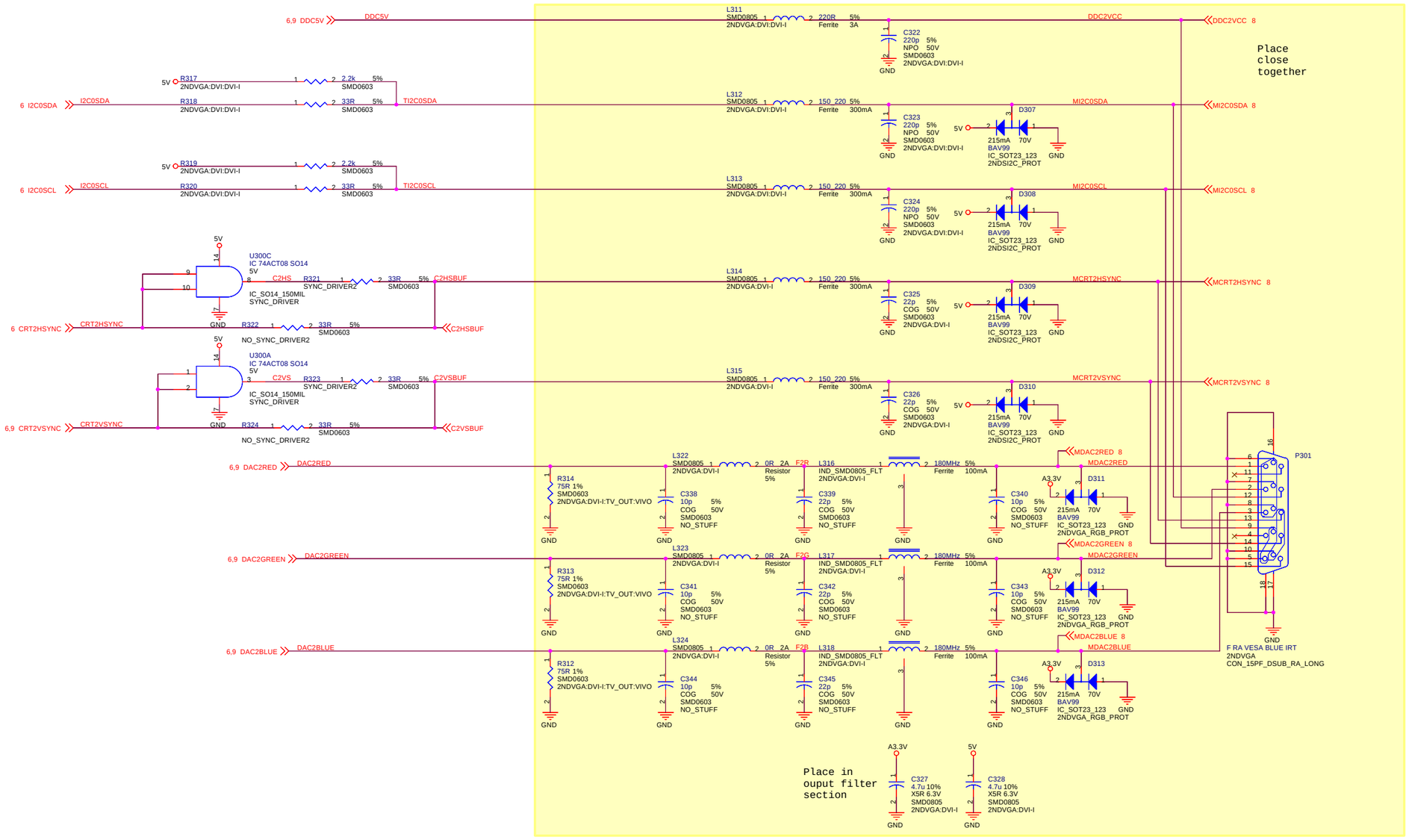
	Size: Custom; CAGE Code; DWG NO; Rev
Tuesday, October 30, 2001	Scale; Sheet 6 of 11



3.b Dual DAC, 2nd VGA

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Tuesday, October 30, 2001	Size Custom	CAGE Code	DWG NO	Rev
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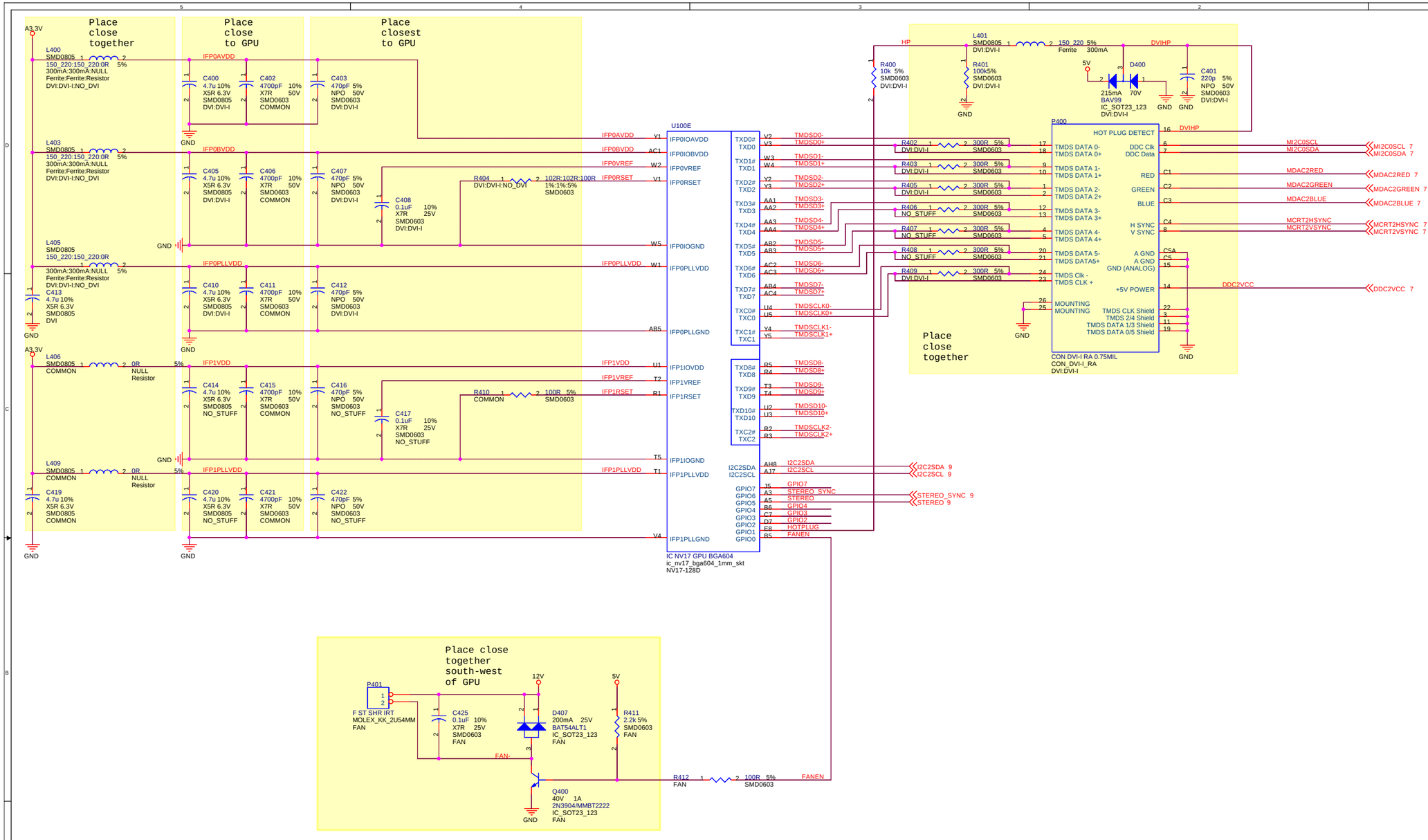

4. Panel

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Custom			

Wednesday, October 31, 2001 — Scale — Sheet 8 of 11

Place south west of GPU.

Only for tests with NV11B!

Place close together and close to P500

Place close to P500

Place cose to P500

Decoupling U500

Decoupling U502

Decoupling U503

5. TV out,video capture,stereo

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Wednesday, October 31, 2001	Size: Custom	CAGE Code	DWG NO	Rev
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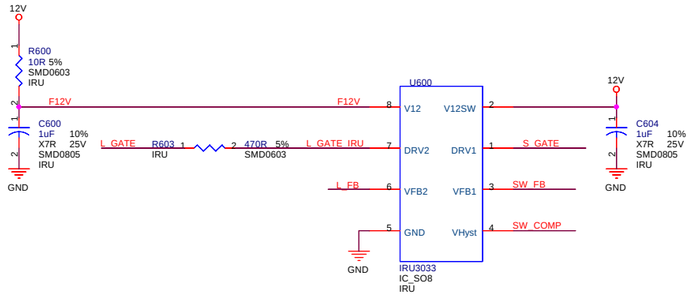
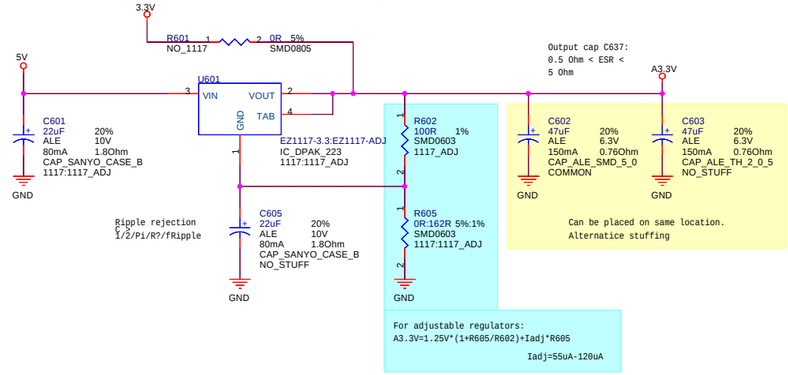
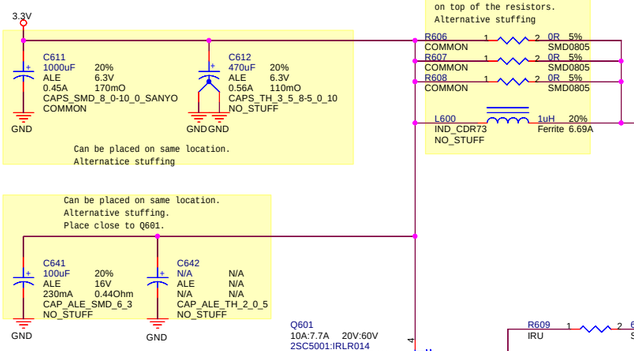
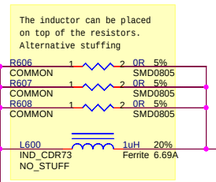


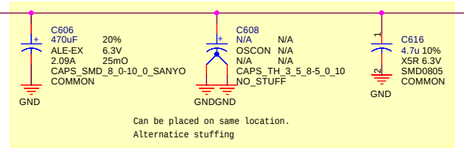
Analog 3.3V



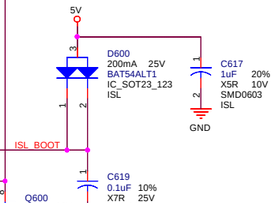


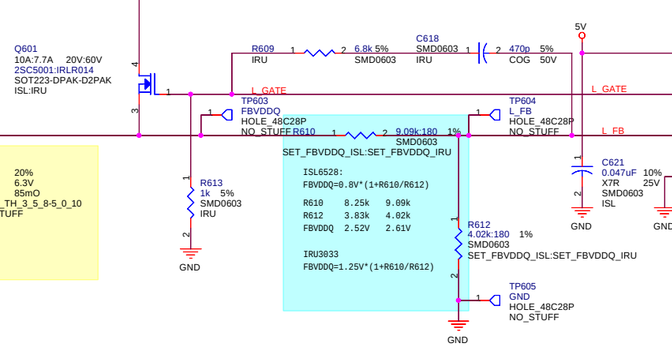


F3.3V

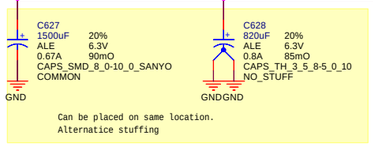


F3.3V

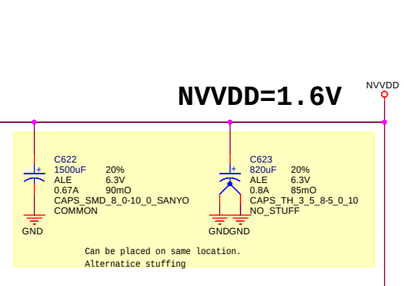




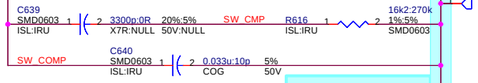
FBVDDQ



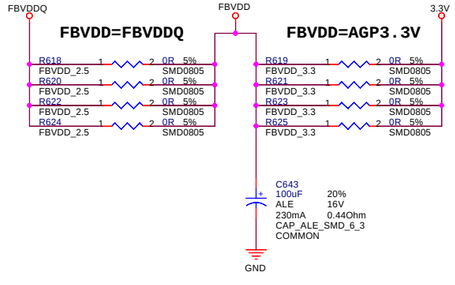
NVVDD=1.6V



SW_FB



FBVDD



6. Power supply

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

P70, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, video capture, stereo, AGP4x

	Size	CAGE Code	DWG NO	Rev
	Custom			
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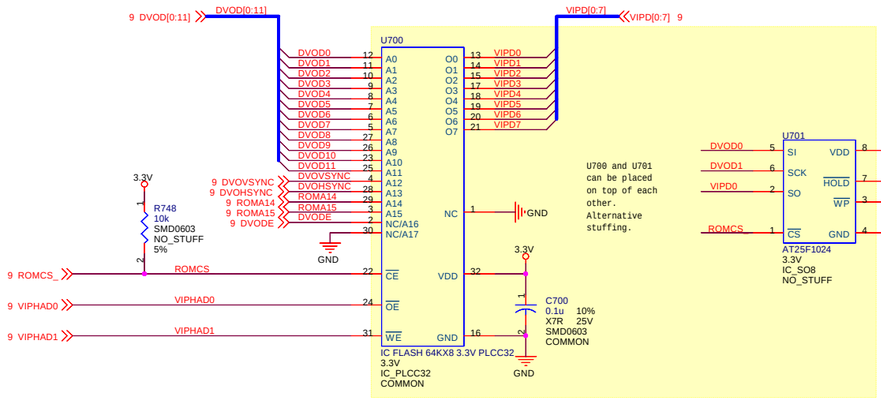
0	R700 NO_STUFF	10k 5% SMD0402	DVOD0	R701 COMMON	10k 5% SMD0402	PCI_AD_SWAP	0: REVERSED 1: NORMAL default
1	R702 NO_STUFF	10k 5% SMD0402	DVOD1	R703 COMMON	10k 5% SMD0402	SUB_VENDOR	0: system BIOS 1: adapter BIOS default
2	R704 NO_STUFF	10k 5% SMD0402	DVOD2	R705 MEMSTRAP1111	10k 5% SMD0402	RAM_CFG_0	[3:0] 1111: 4Mx32 DDR SDRAM, DQS per 32 bits, dll-on, low drive strength
3	R706 NO_STUFF	10k 5% SMD0402	DVOD3	R707 MEMSTRAP1111	10k 5% SMD0402	RAM_CFG_1	
4	R708 NO_STUFF	10k 5% SMD0402	DVOD4	R709 MEMSTRAP1111	10k 5% SMD0402	RAM_CFG_2	
5	R710 NO_STUFF	10k 5% SMD0402	DVOD5	R711 MEMSTRAP1111	10k 5% SMD0402	RAM_CFG_3	
6	R712 XTAL_27	10k 5% SMD0402	DVOD6	R713 XTAL_14	10k 5% SMD0402	CRYSTAL_0	[1:0] 00: 13.5MHz 01: 14.318MHz 10: 27MHz 11: unknown
22	R714 XTAL_14	10k 5% SMD0402	VIPD6	R715 XTAL_27	10k 5% SMD0402	CRYSTAL_1	
7	R716 NO_STUFF	10k 5% SMD0402	DVOD7	R717 COMMON	10k 5% SMD0402	TVMODE_0	[1:0] 00: SECAM 01: NTSC 10: PAL 11: VGA
8	R718 VIVO:TV_OUT	10k 5% SMD0402	DVOD8	R719 2NDVGA	10k 5% SMD0402	TVMODE_1	
9	R722 COMMON	10k 5% SMD0402	DVOD9	R723 NO_STUFF	10k 5% SMD0402	AGP4x	0: enabled default 1: disabled
11	R724 COMMON	10k 5% SMD0402	VIPD7	R725 NO_STUFF	10k 5% SMD0402	AGP_FW	0: enabled default 1: disabled
12	R726 NO_STUFF	10k 5% SMD0402	VIPD4	R727 NV17-128D	10k 5% SMD0402	PCI_DEVID_0	[3:0] 0001: NV17-128D
13	R728 NV17-128D	10k 5% SMD0402	VIPD5	R729 NO_STUFF	10k 5% SMD0402	PCI_DEVID_1	
20	R730 NV17-128D	10k 5% SMD0402	VIPD3	R731 NO_STUFF	10k 5% SMD0402	PCI_DEVID_2	
21	R732 NV17-128D	10k 5% SMD0402	DVOHSYNC	R733 NO_STUFF	10k 5% SMD0402	PCI_DEVID_3	
14	R734 NO_STUFF	10k 5% SMD0402	DVOD11	R735 COMMON	10k 5% SMD0402	BUS_TYPE	0: PCI 1: AGP default
16	R736 COMMON	10k 5% SMD0402	VIPD0	R737 NO_STUFF	10k 5% SMD0402	USER_0	USER[0]=0: PC default USER[0]=1: MAC
17	R738 COMMON	10k 5% SMD0402	VIPD1	R739 NO_STUFF	10k 5% SMD0402	USER_1	
18	R740 COMMON	10k 5% SMD0402	VIPHAD0	R741 NO_STUFF	10k 5% SMD0402	USER_2	
19	R742 COMMON	10k 5% SMD0402	VIPHAD1	R743 NO_STUFF	10k 5% SMD0402	USER_3	
29	R744 COMMON	10k 5% SMD0402	DVOD10	R745 NO_STUFF	10k 5% SMD0402	ROMTYPE_0	[1:0] 00: parallel 01: serial AT25F 10: serial SST45V not supported 11: serial future not supported
30	R746 COMMON	10k 5% SMD0402	VIPD2	R747 NO_STUFF	10k 5% SMD0402	ROMTYPE_1	



7. BIOS, Strapping

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

P70, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, video capture, stereo, AGP4x

Size	CAGE Code	DWG NO	Rev
Custom			

Tuesday, October 30, 2001

Scale

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