

P654 - GT200/NVIO2

P654, GT200-100, 896MB/1792MB - GDDR3 BGA136 16M/32Mx32

DVI-I + DVI-I/DP + HD/SD/TVout, SPDIF, Dual SLI

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REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-1064-BASE-A03	BASE LEVEL, GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-1064-0000-000	DT: GT200-100, 55013501000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I + HDTV
2	SKU0001	600-1064-0001-000	DT: GT200-100, 55013501000, 896MB - 16Mx32 GDDR3, DVI-I + DP + HDTV
3	SKU0051	600-1064-0051-300	DT: GT200-100, 57612421000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I
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MS-V180 -0A
PAGE 21:VGS SLIM
PAGE 22:remove DACB HDTV Circuit
PAGE 24:DVI change HDMI
PAGE 25:DP modify DSDA/DSCL circuit
PAGE 28:ADD I2C0_SCL/SDA and GPIO 3 circuit,remove GPIO 12
PAGE 29:remove R112,R113 and GPIO8_FAN_TACH link to U21
PAGE 33:remove R671,R572
PAGE 35:remove RT8805CQVA change UPI6205 and UPI6262 circuit
PAGE 36:remove NCP5388MNR2G change UPI6208 circuit
PAGE 37/38 :remove NCP3418B change UPI6281 circuit
PAGE 39 :Add WL83L786C circuit

MS-V180 -10
1.PAGE 37,38 modify D15-D21 footprint
2..PAGE 37,38 add CAP

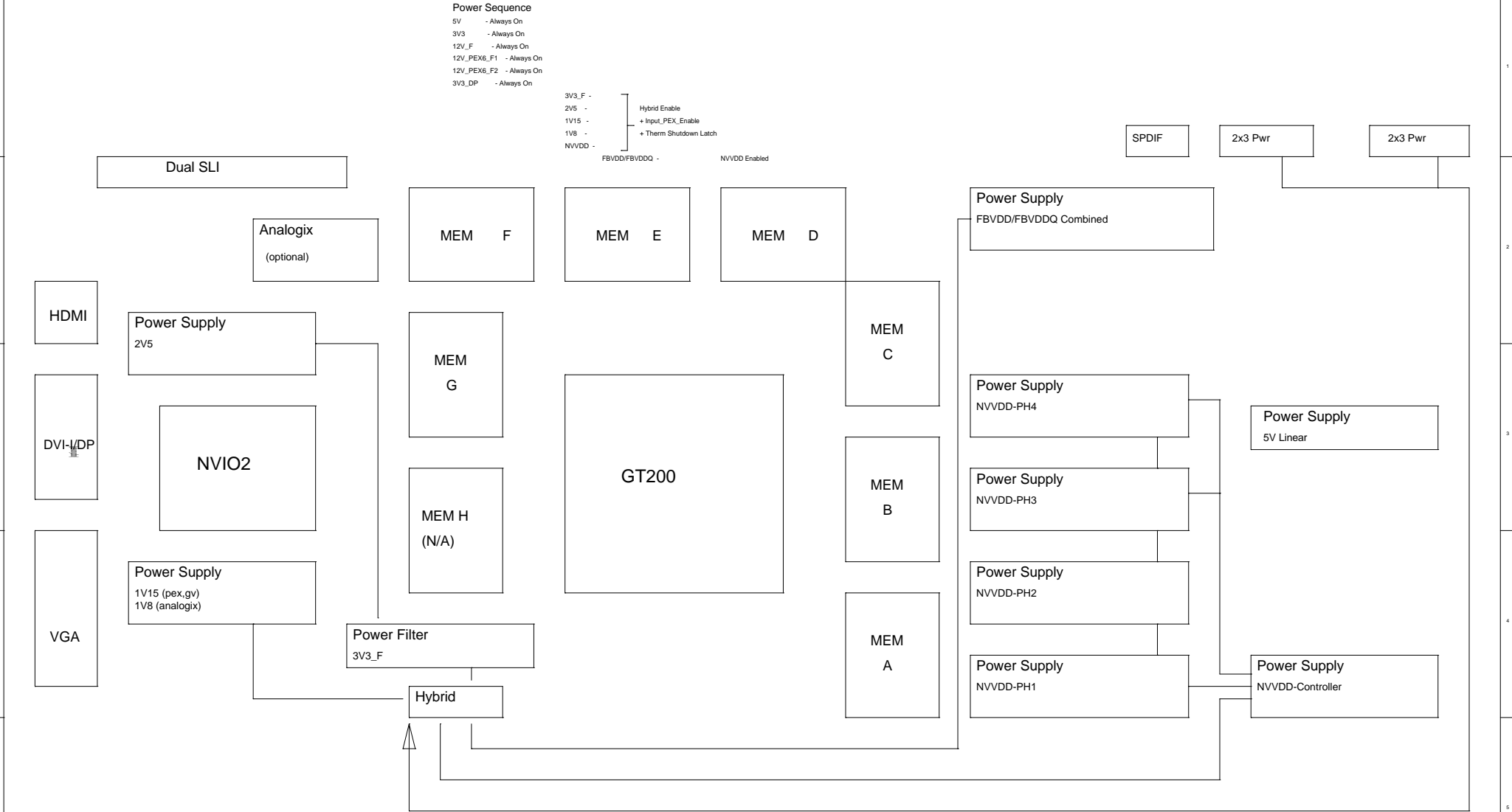
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Block Diagram



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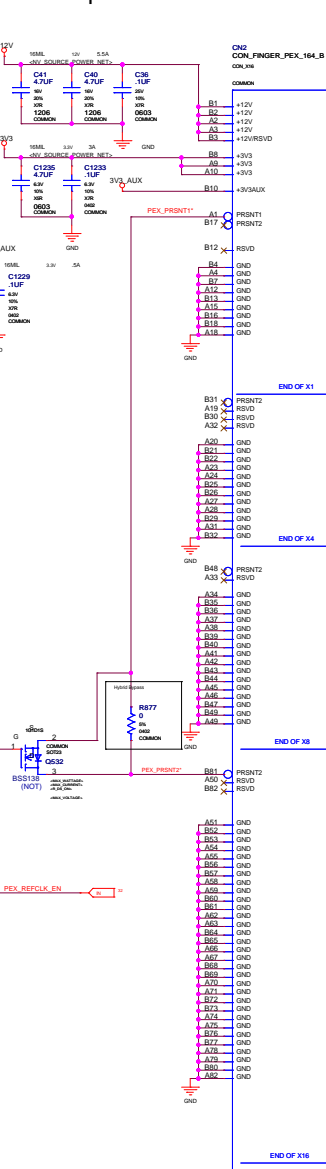
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Block Diagram



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PCI Express / JTAG



JTAG



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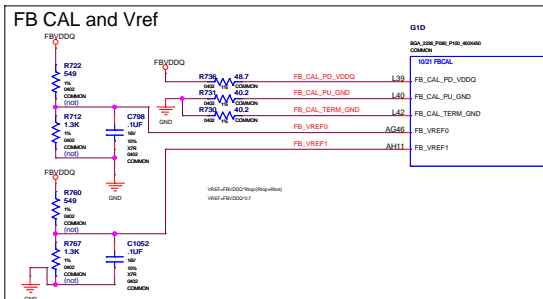
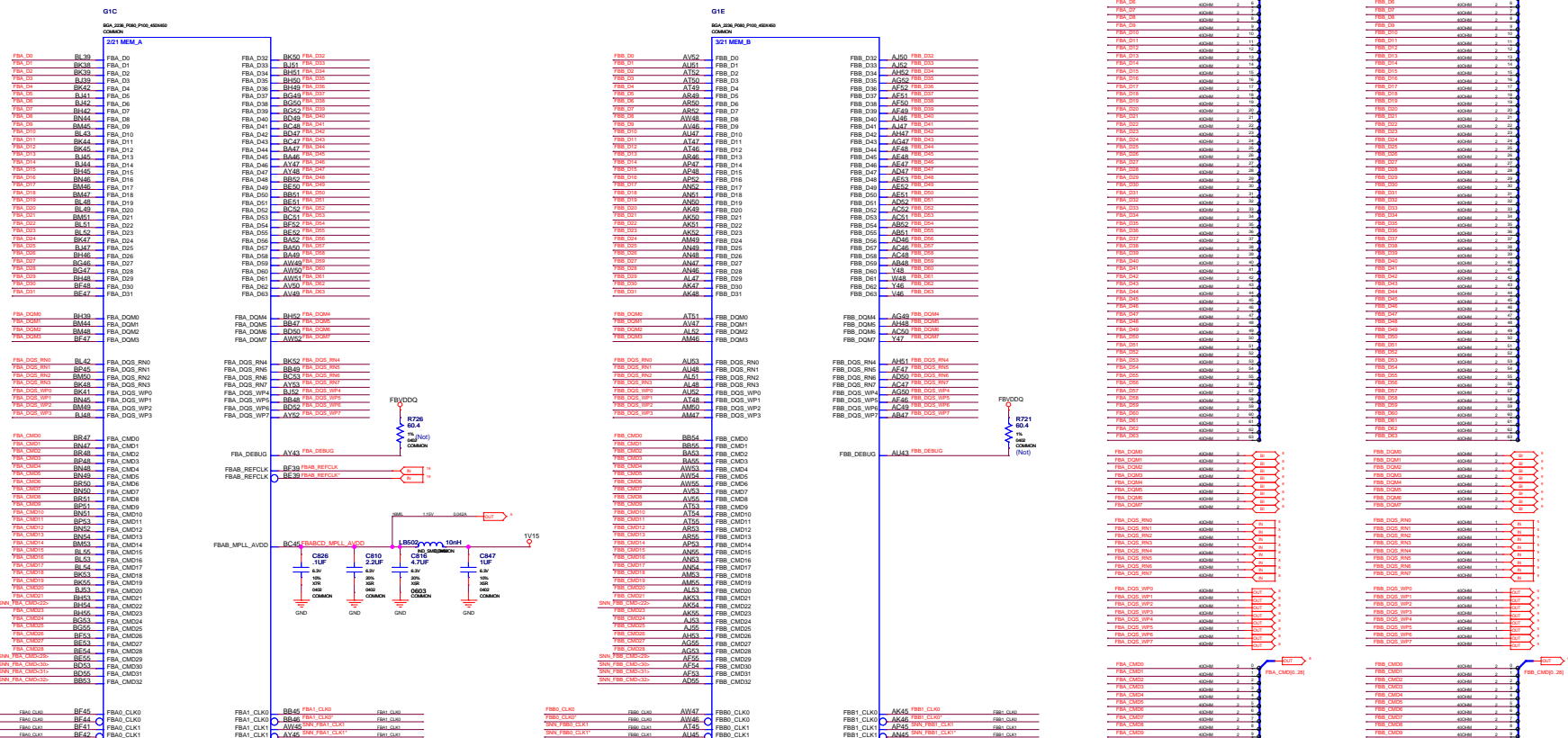
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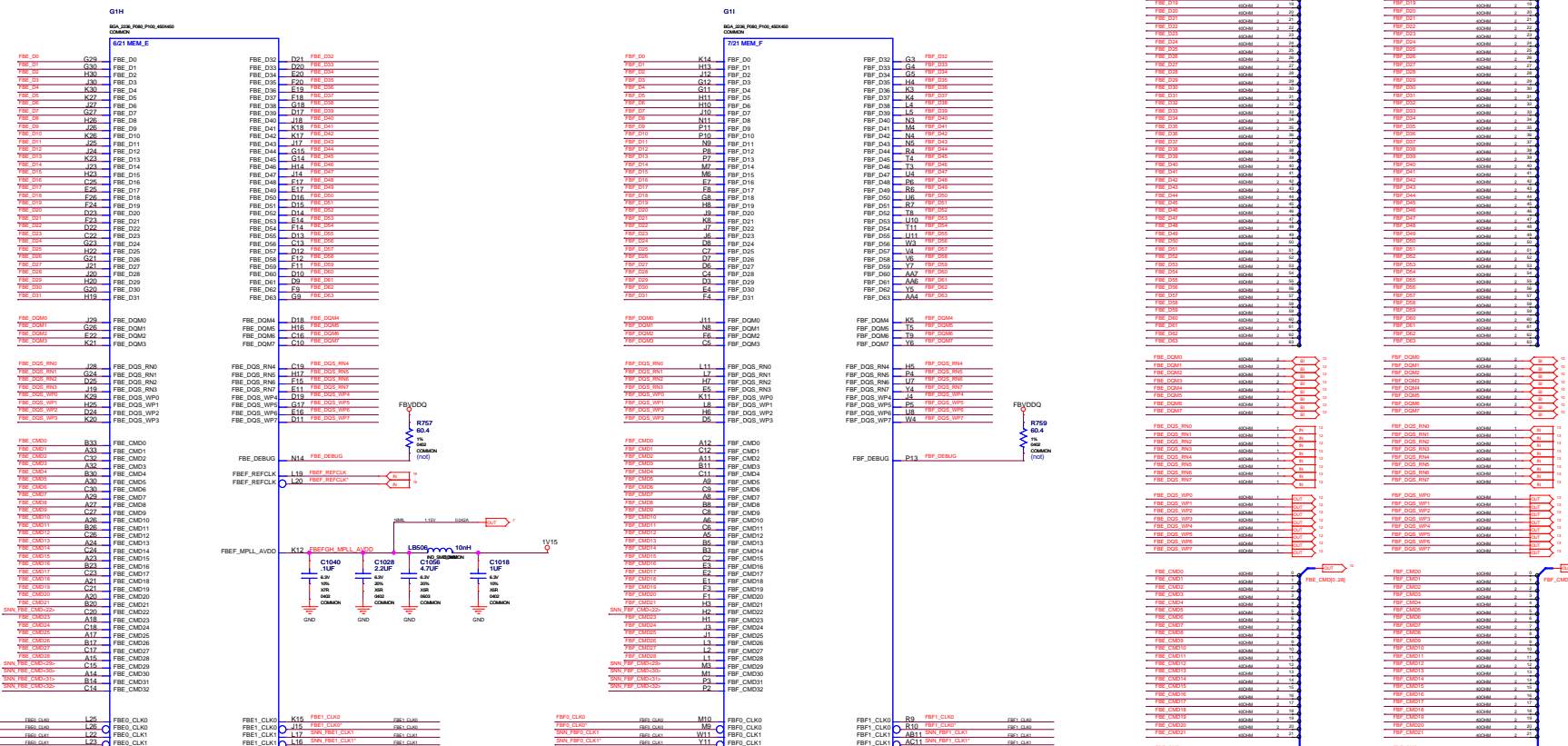
Framebuffer A,B: GPU Section + Calibration



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Framebuffer E,F: GPU Section



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ABCDEFGH

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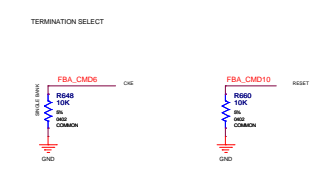
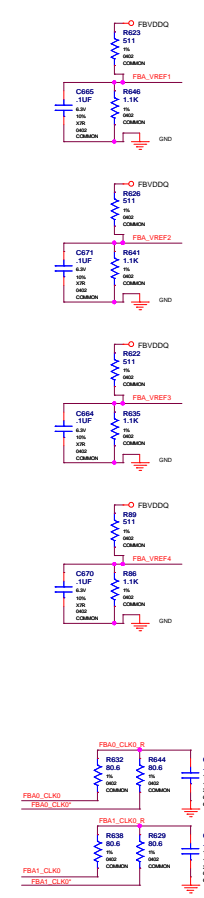
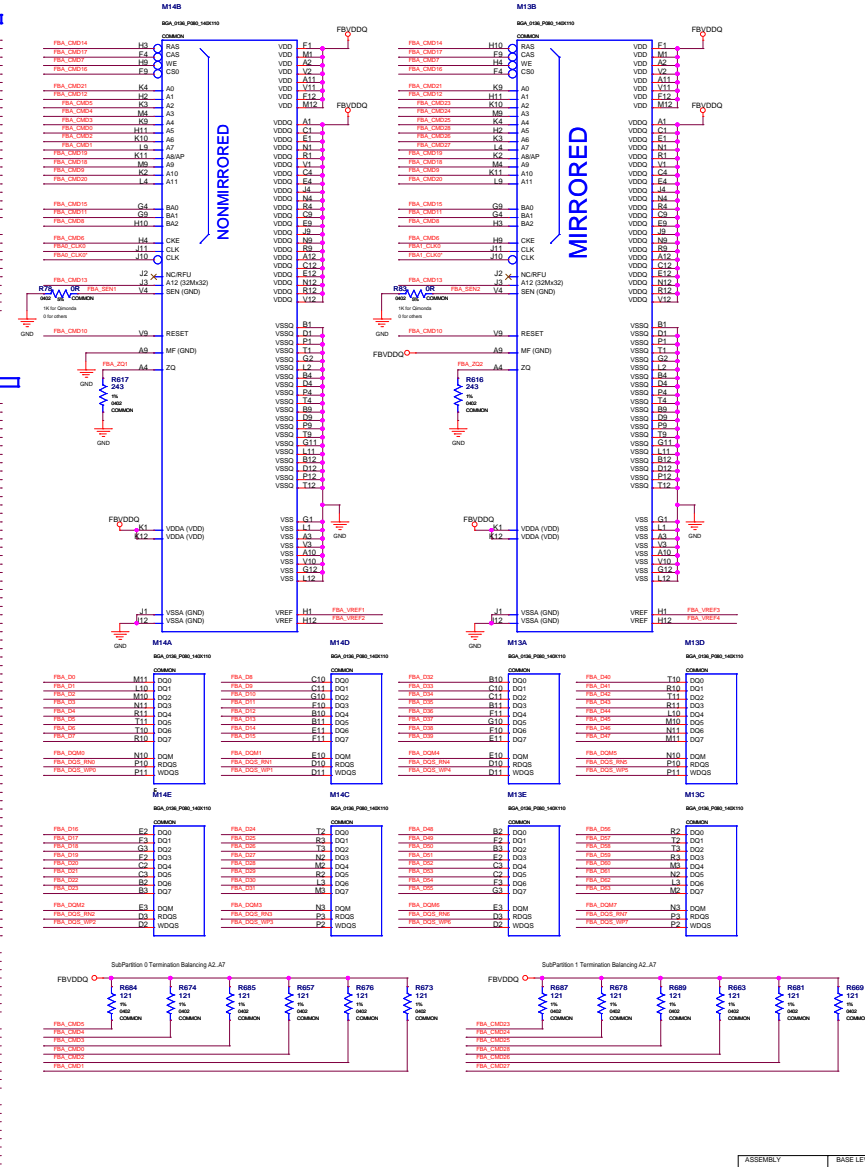
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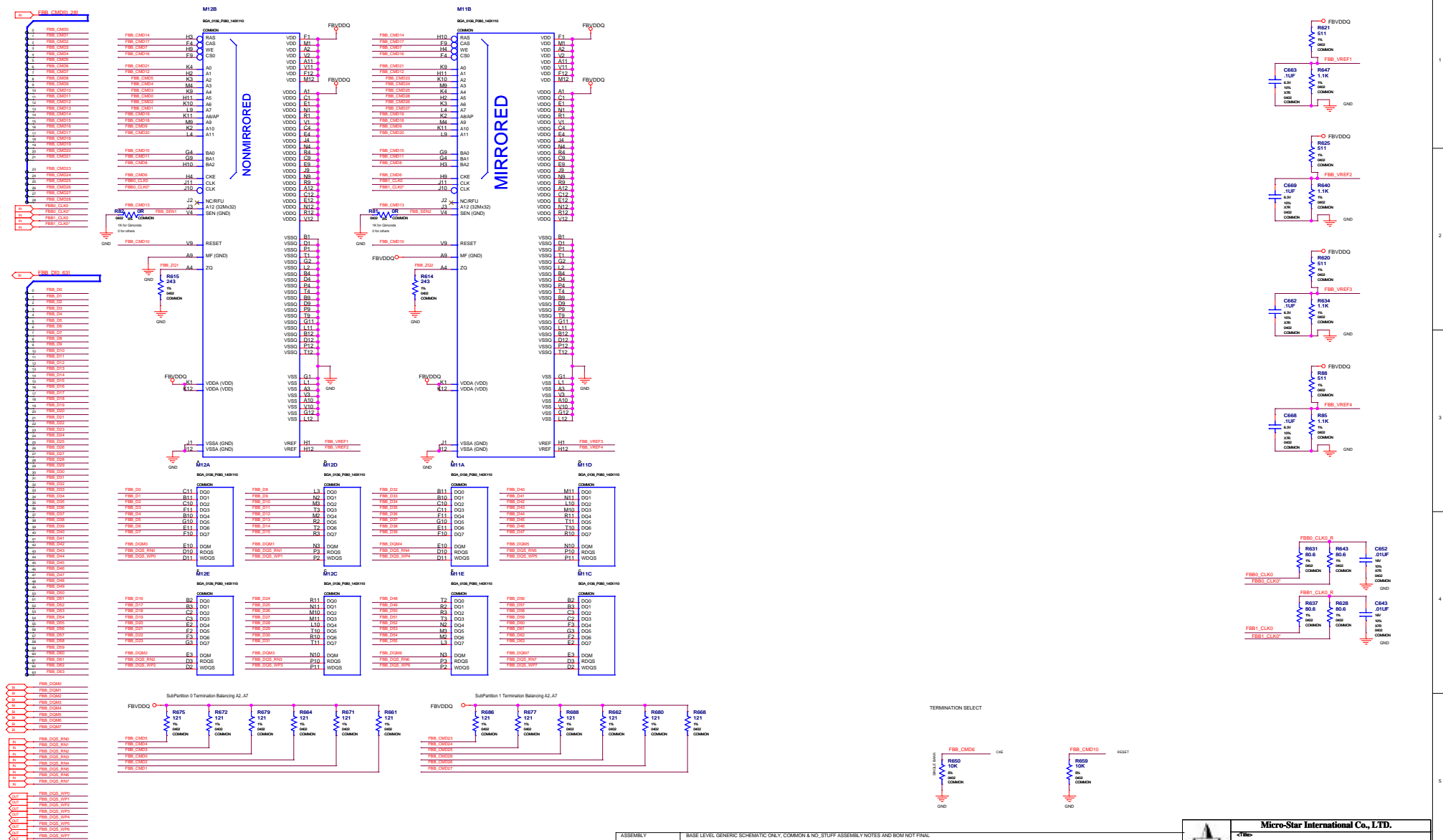
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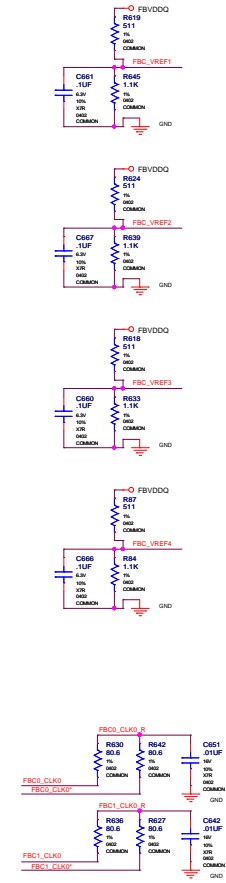
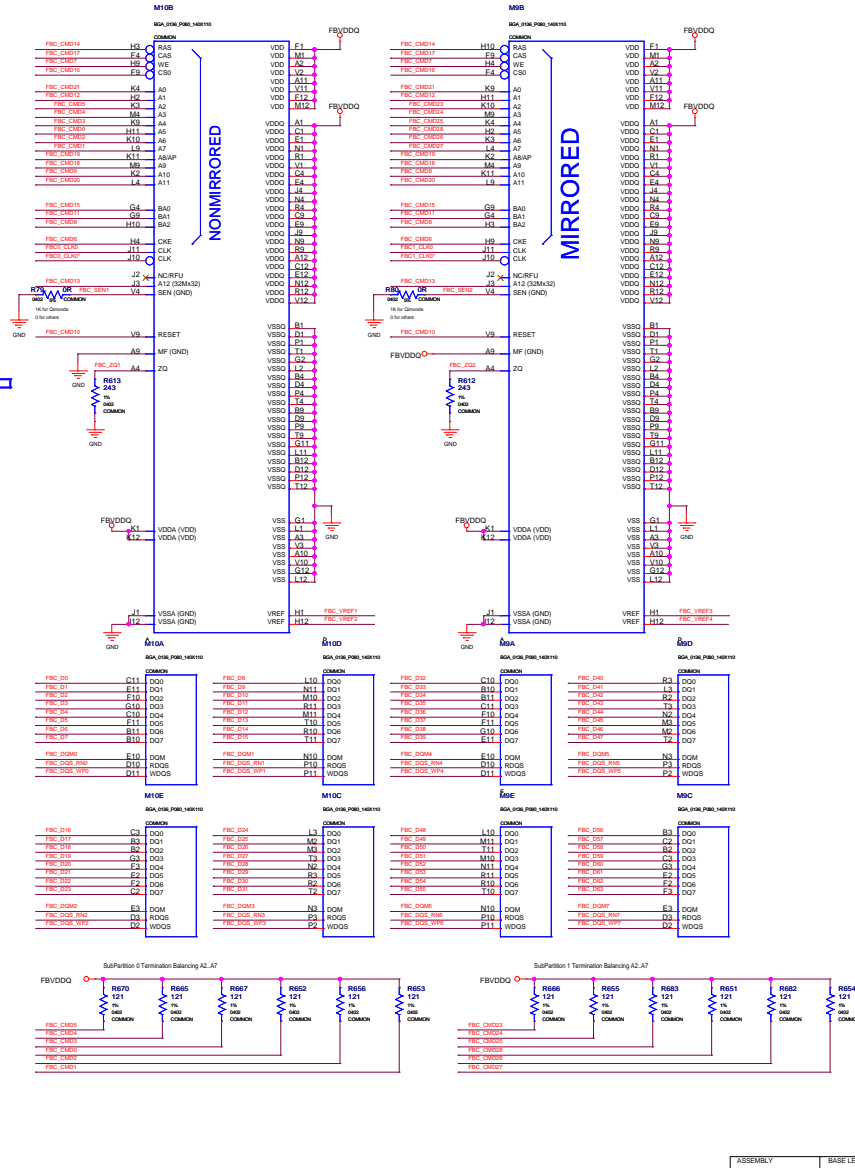
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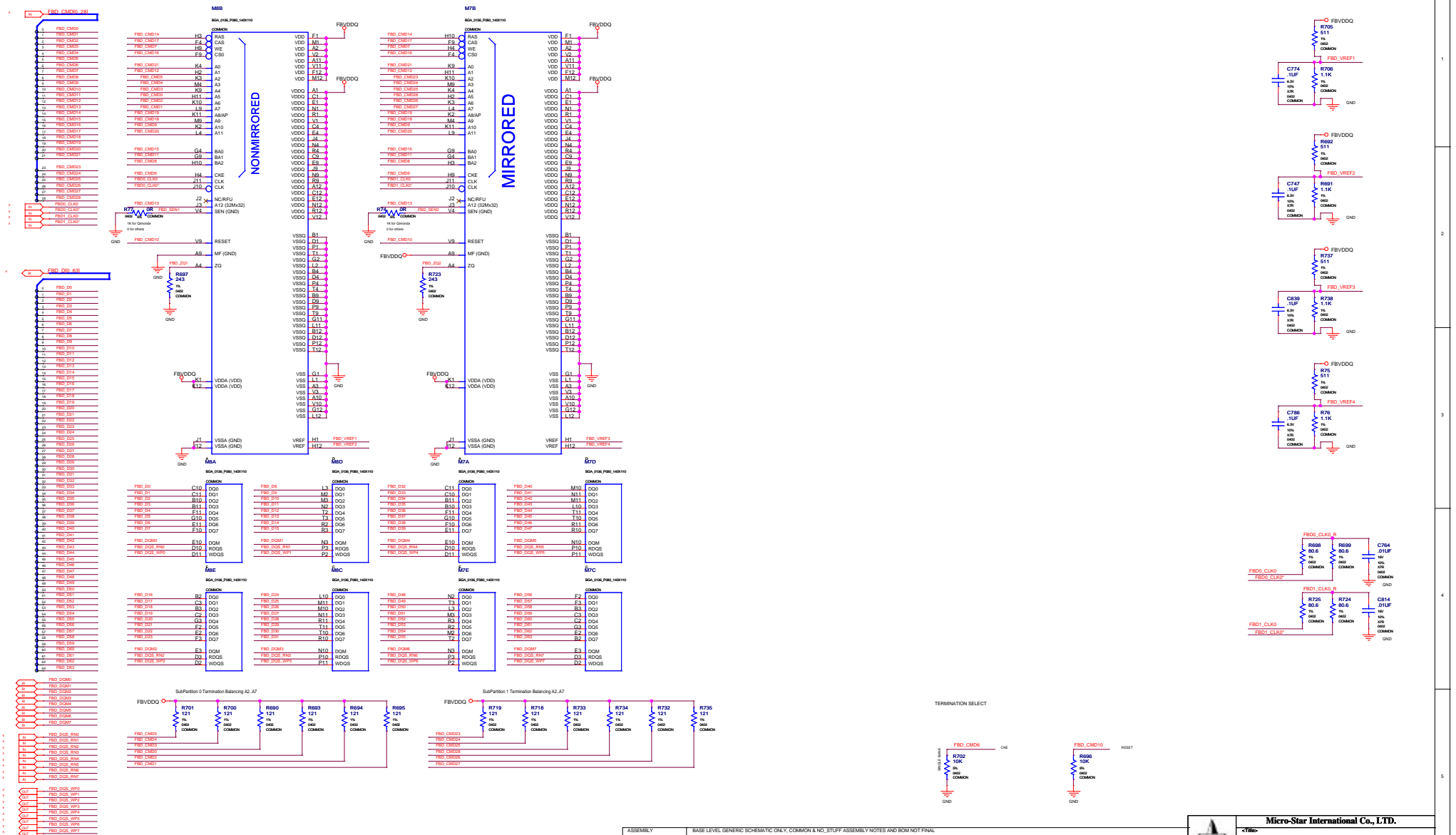
Framebuffer B: Memory Section



FCM - CARGO 205	
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165</	



Framebuffer D: Memory Section



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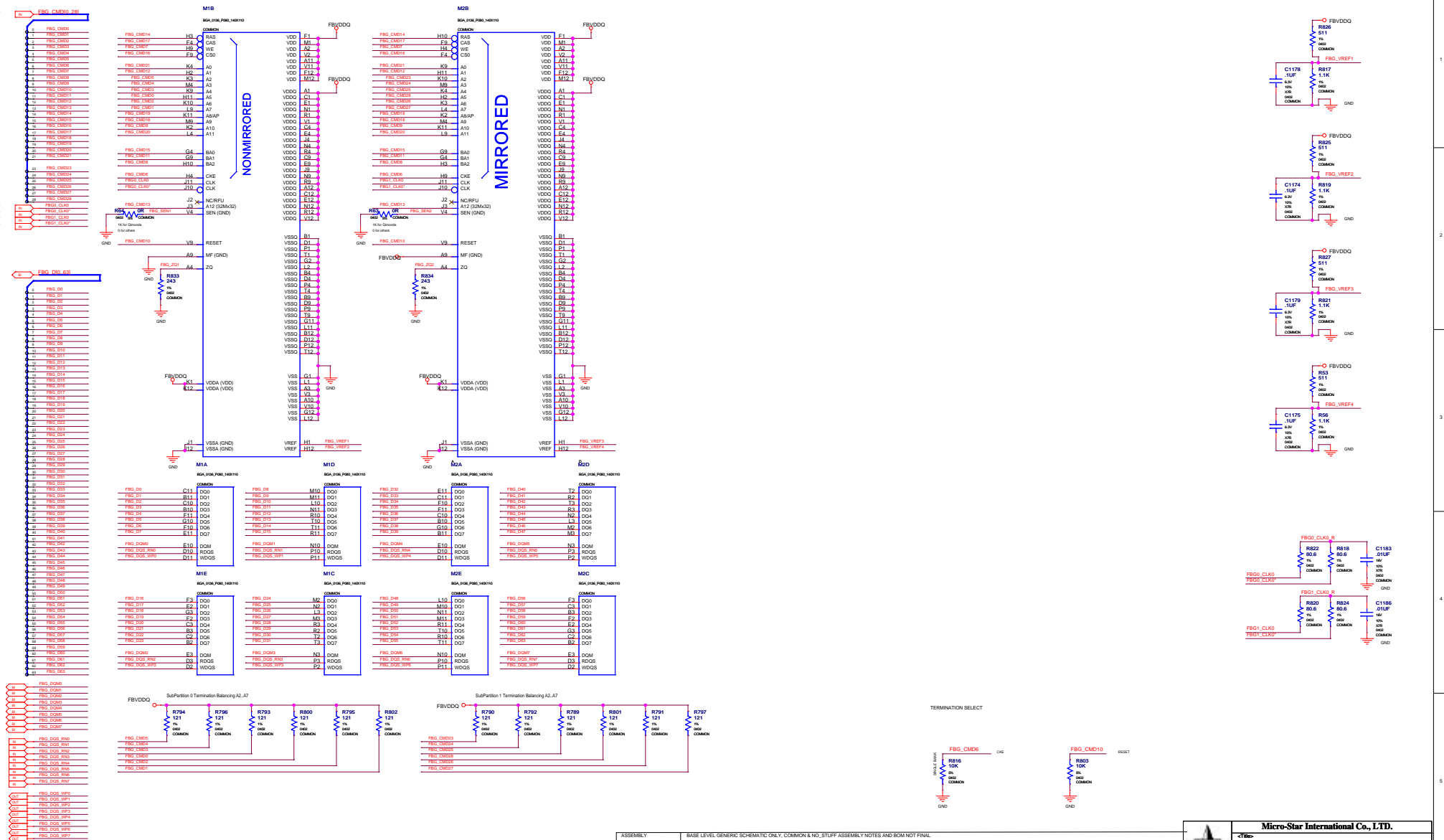


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Framebuffer G: Memory Section



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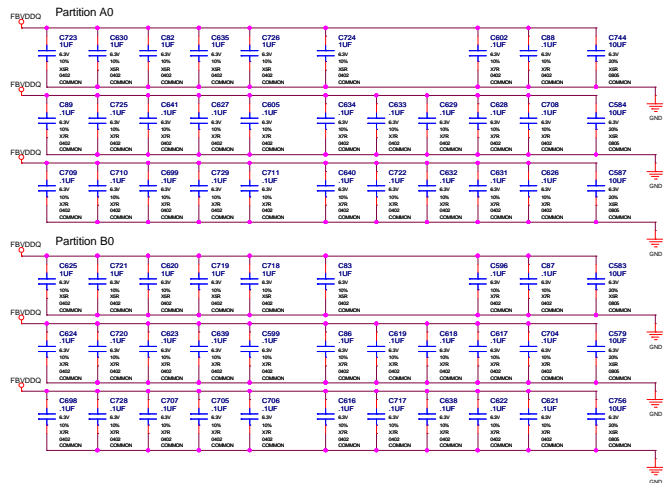
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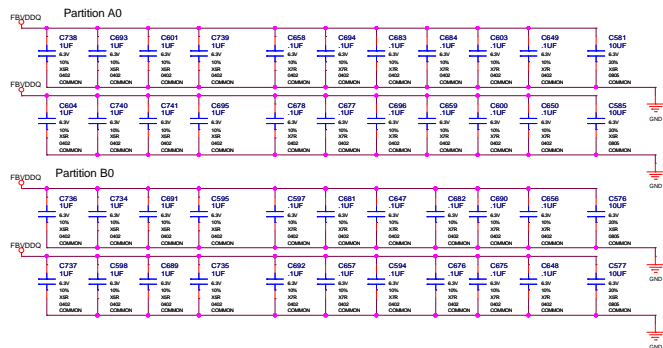
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Decoupling: Memory Section A-D

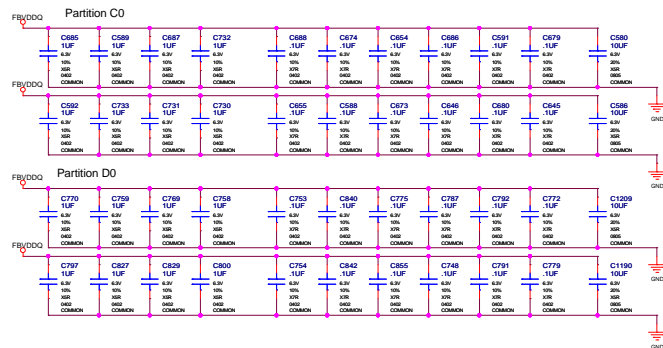
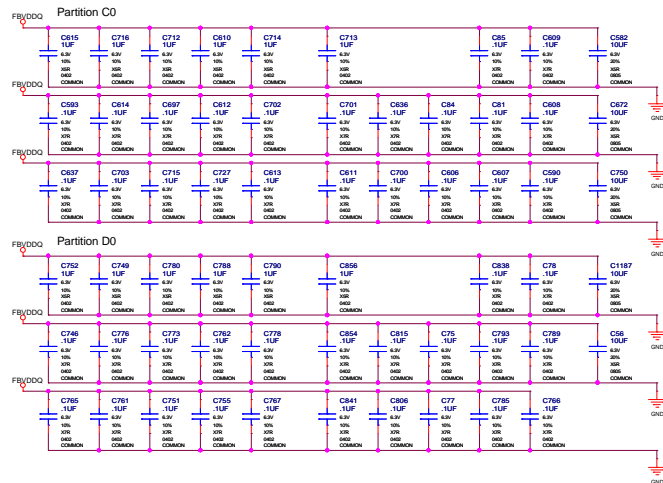
Decoupling for FBVDDQ



Decoupling for FBVDDQ



Banks A-D FBVDDQ
Combined Distributed Capacitance
280 uF



ASSEMBLY
PAGE DETAIL

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Decoupling Memory Section A-D



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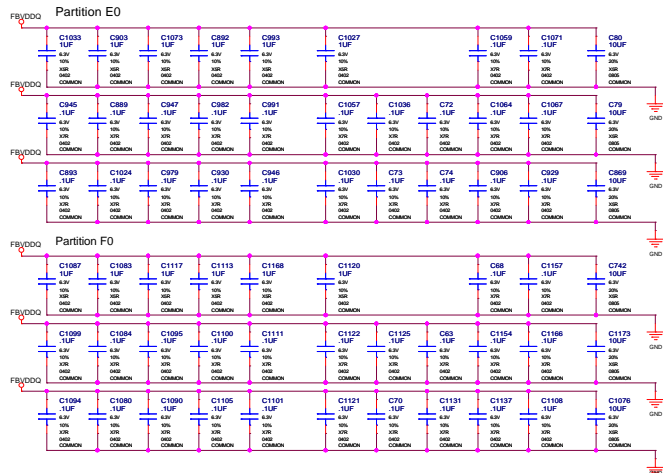
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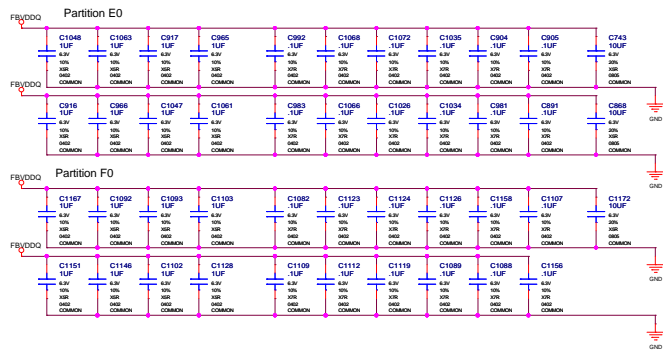
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Decoupling: Memory Section E-G

Decoupling for FBVDDQ



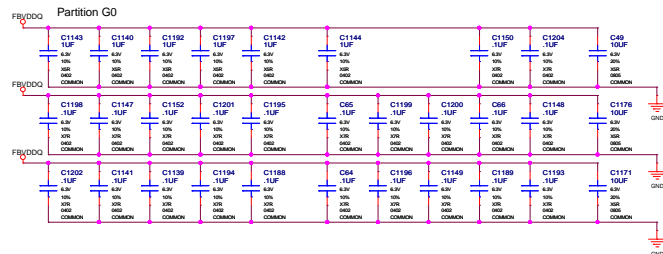
Decoupling for FBVDDQ



Banks E-G FBVDDQ

Combined Distributed Capacitance

210 uF



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BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Decoupling Memory Section E-G



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Date: Monday, April 13, 2009
Sheet: 17 of 41

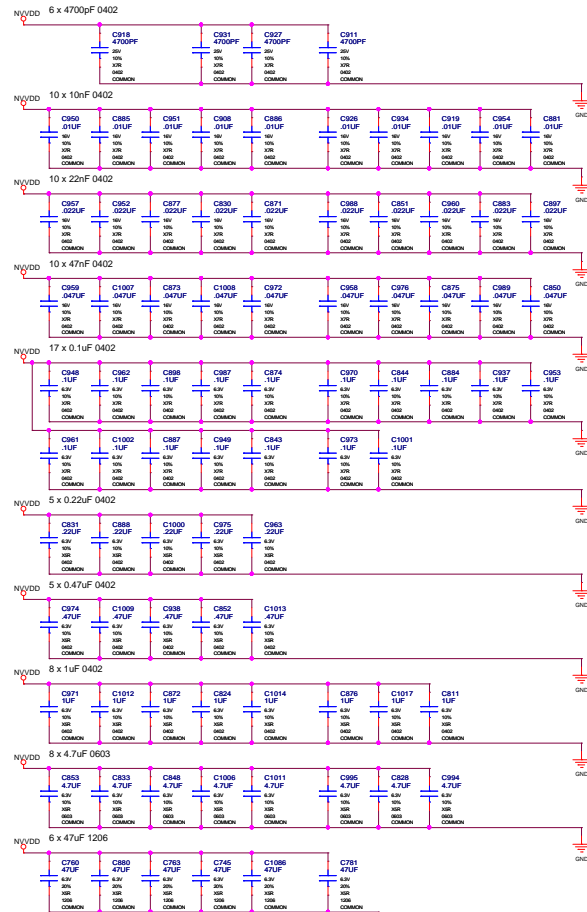
Decoupling: GPU (NVVDD, FBVDDQ)

Decoupling for NVVDD (under GPU)

GPU - NVVDD

Combined Distributed Capacitance

494 uF

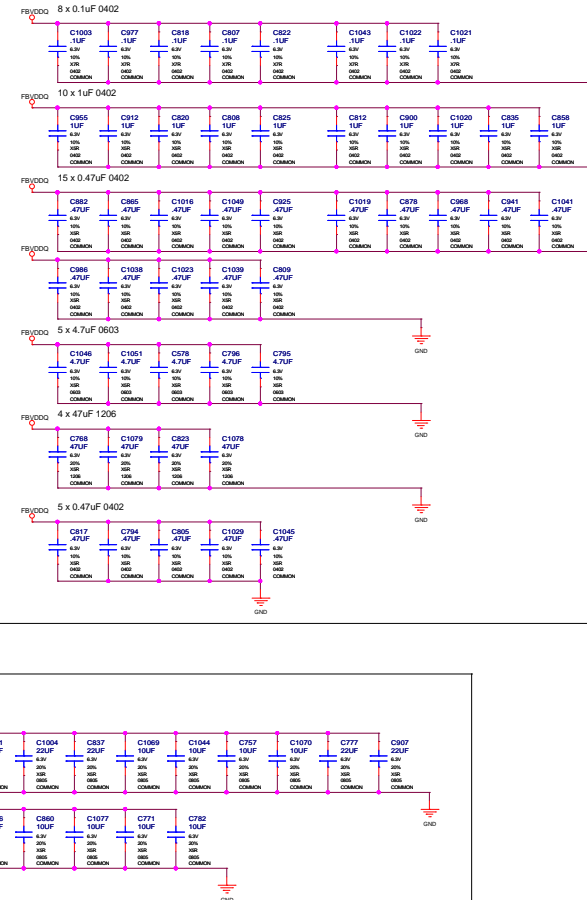


Decoupling for FBVDDQ (under GPU)

GPU - FBVDD/Q

Combined Distributed Capacitance

230 uF

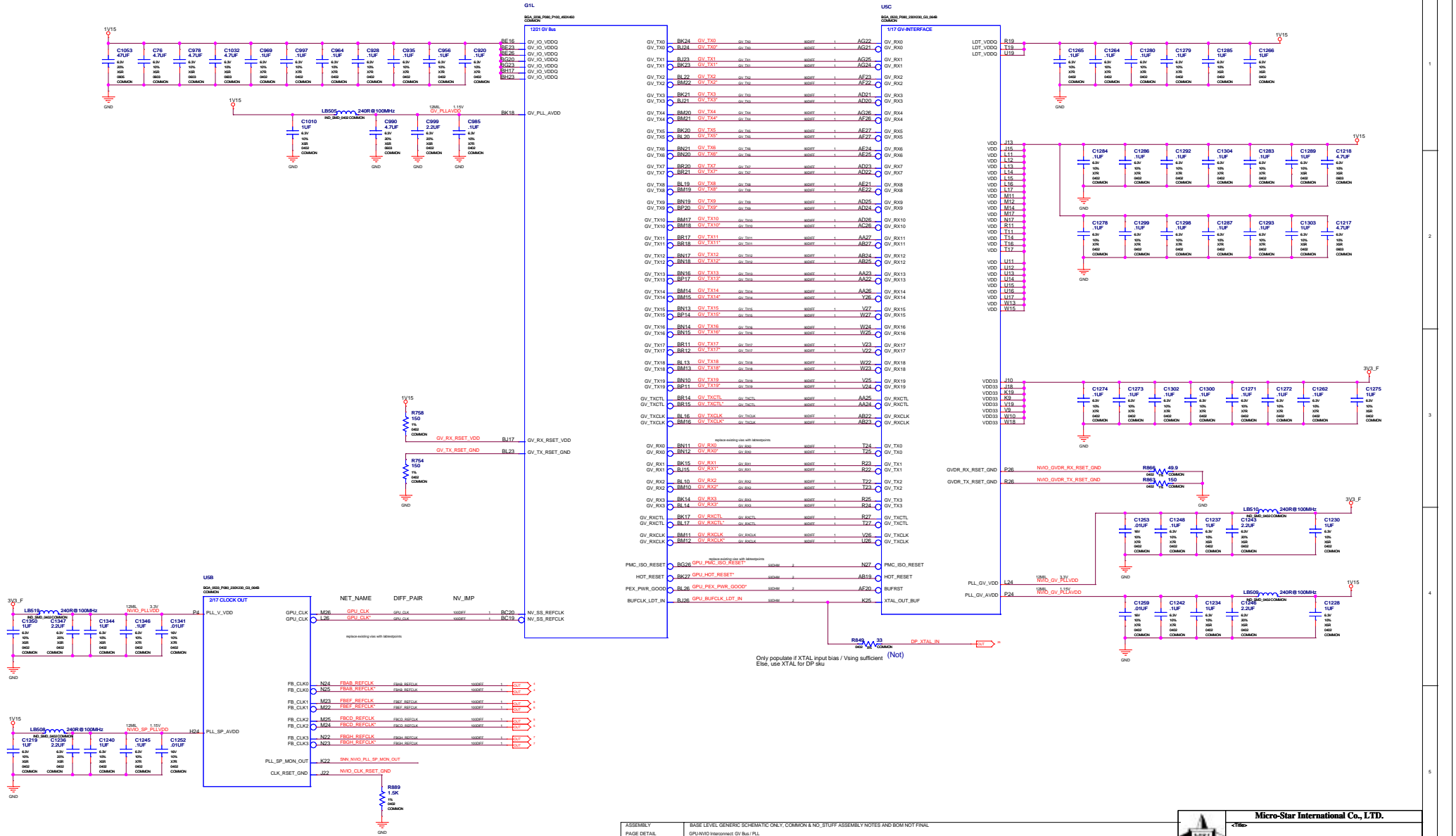


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PAGE DETAIL
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Decoupling GPU (NVVDD, FBVDDQ)

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GPU-NVIO Interconnect: GV Bus / PLL



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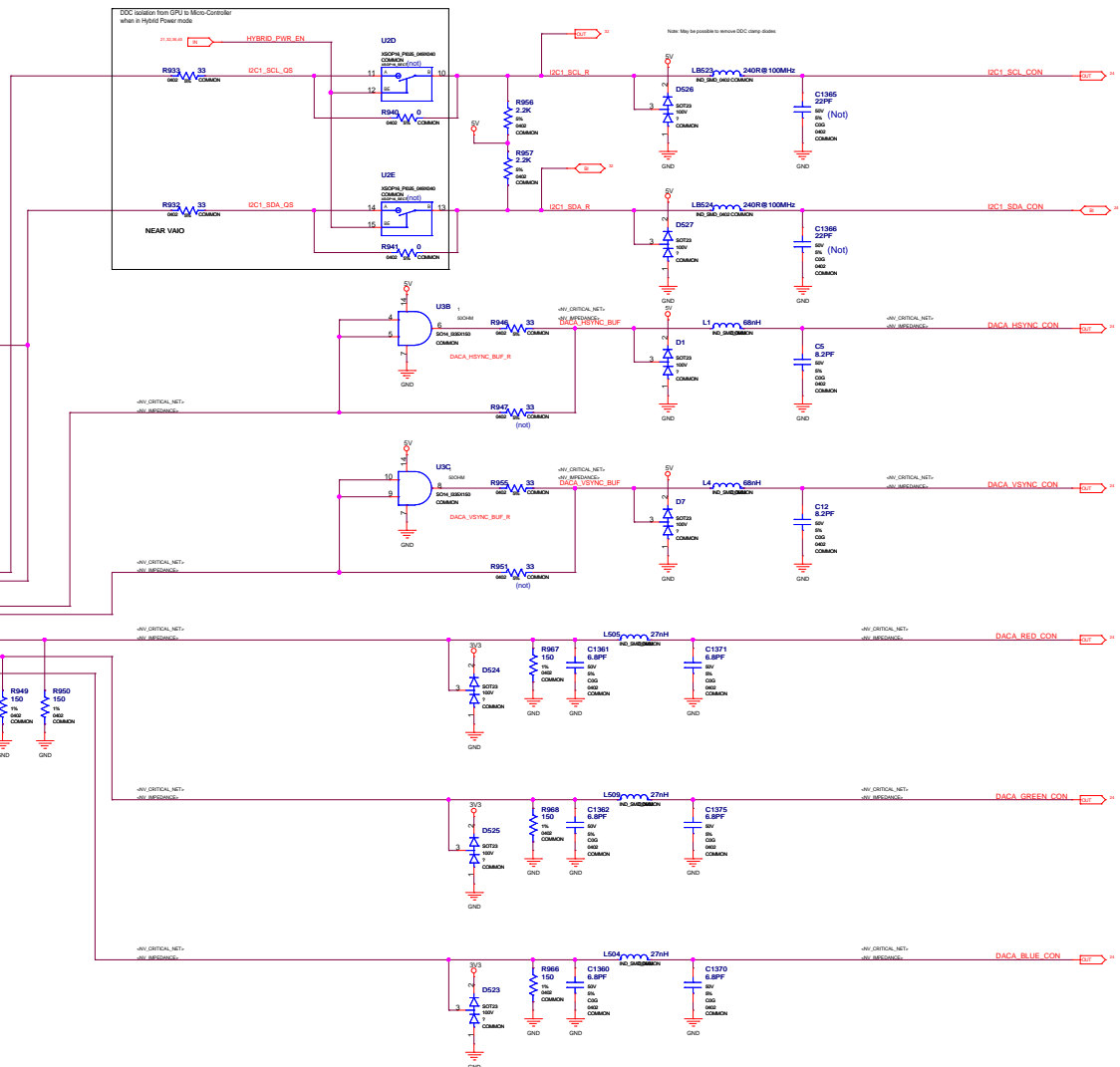
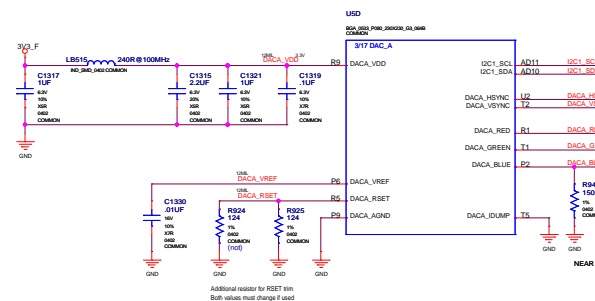
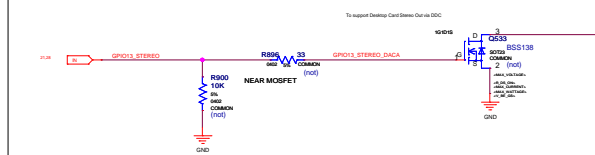
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Display: DACA (Middle DVI-I)



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PAGE DETAIL	Display: DACA (Middle DVI-I)

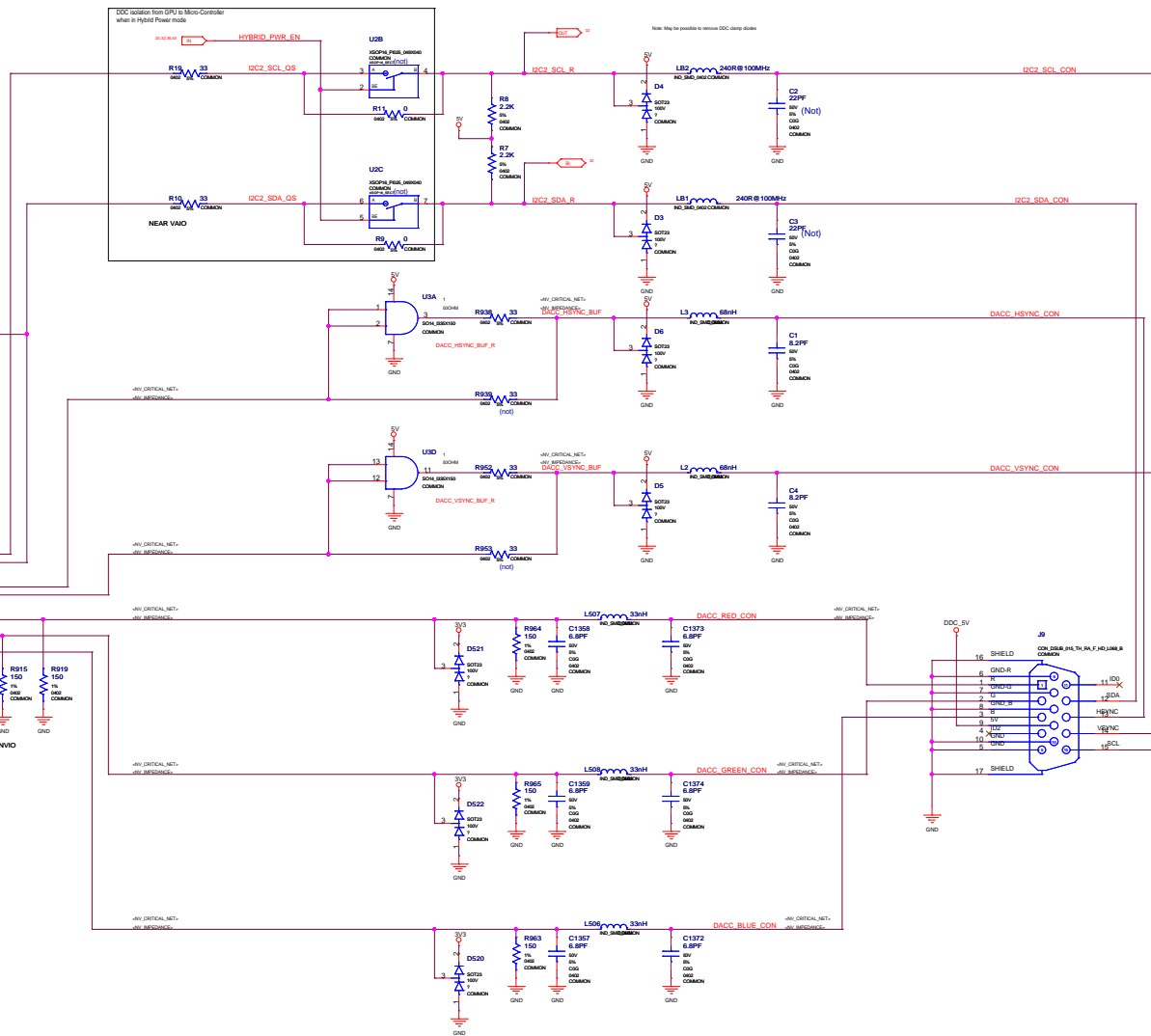
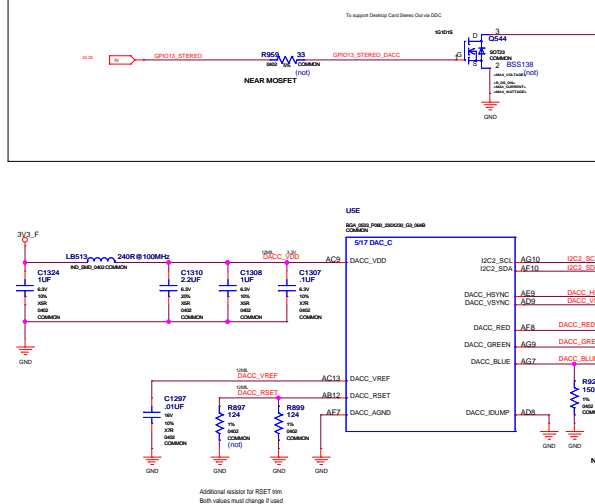


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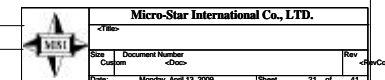
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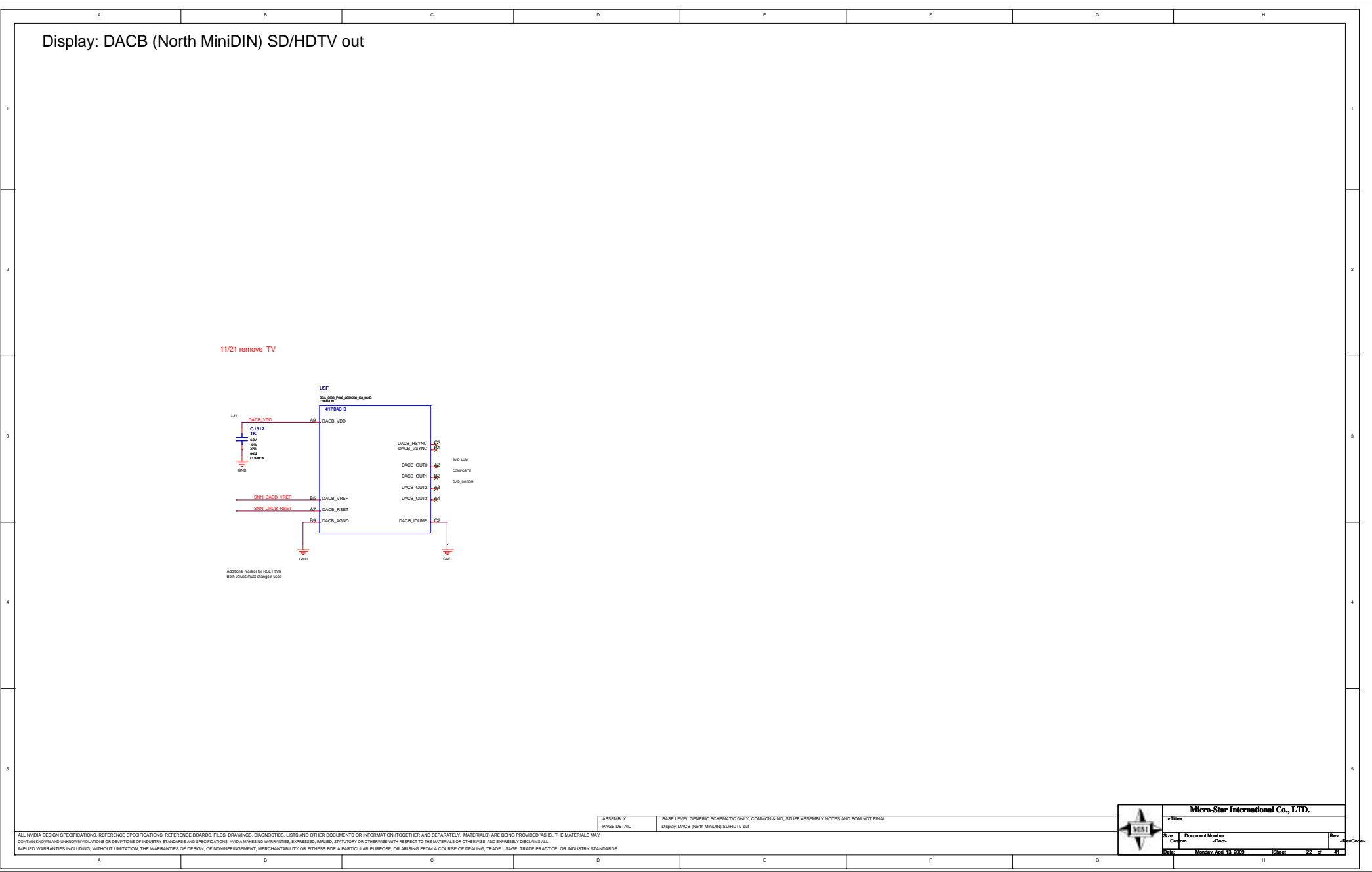
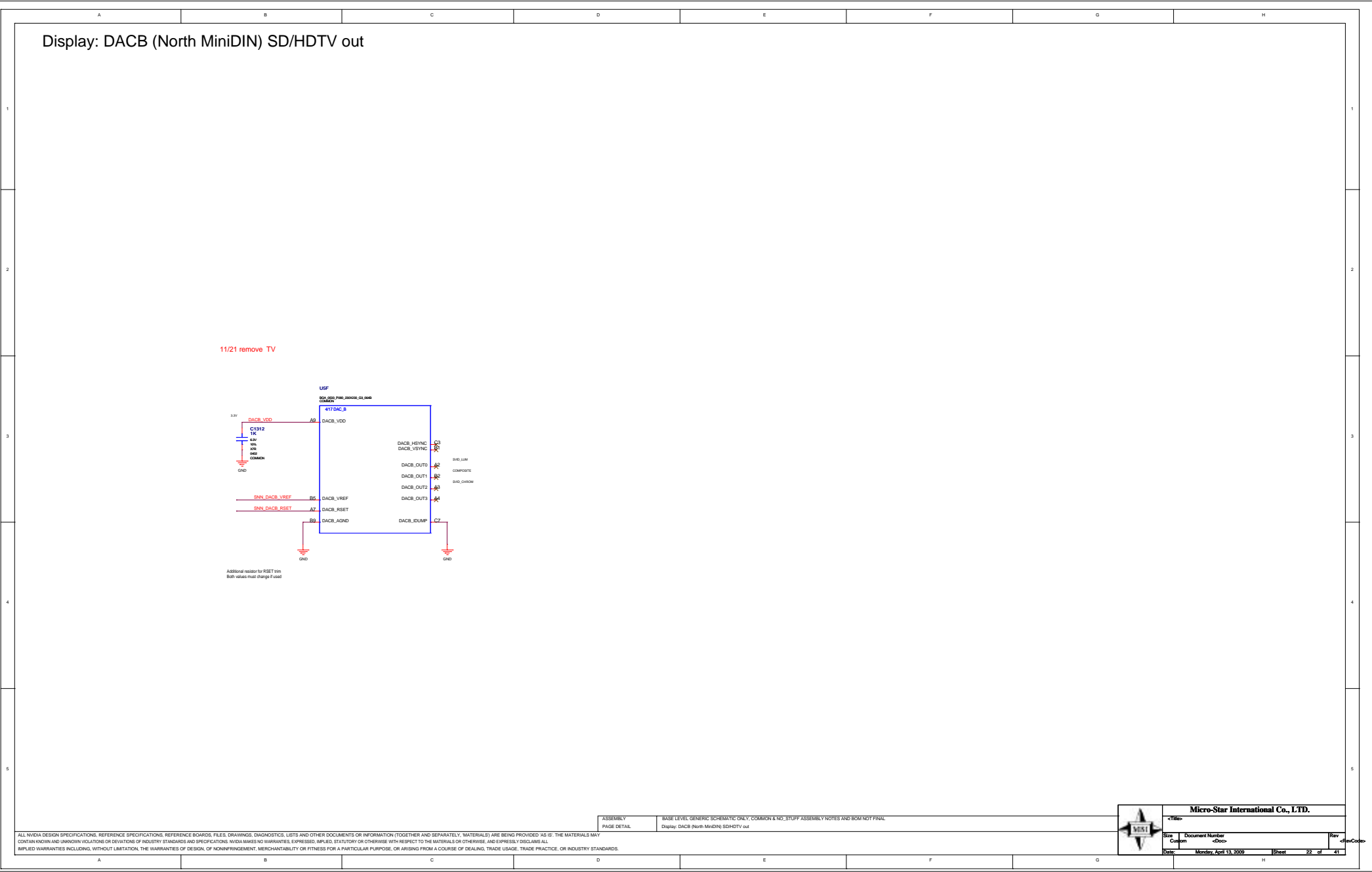
Display: DACC (South DVI-I)




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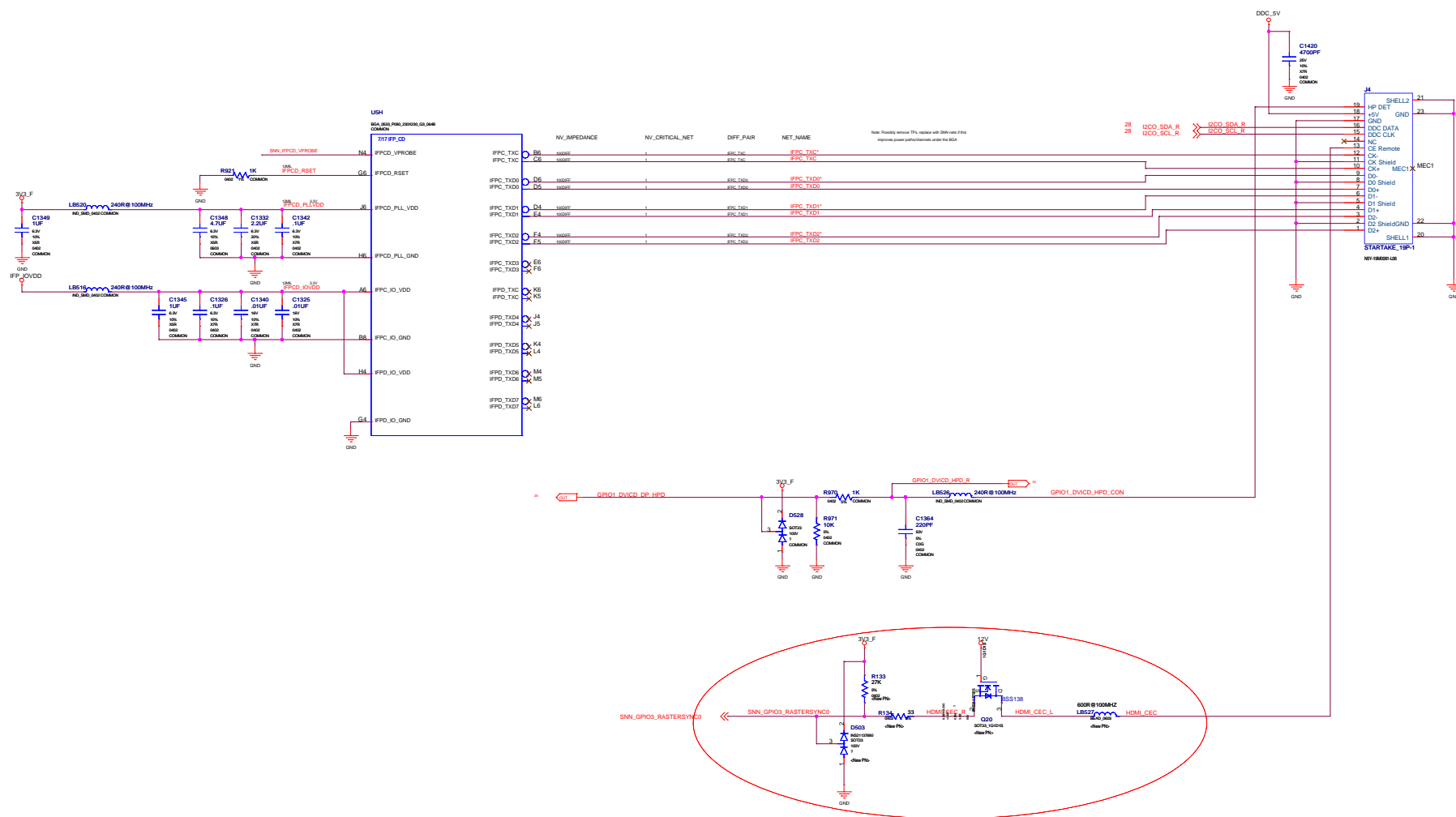
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28 GPIO0_DVIAB_DP_HPD_CON

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Display: IFPCD for middle DVI-I (with DACA)



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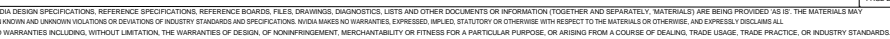
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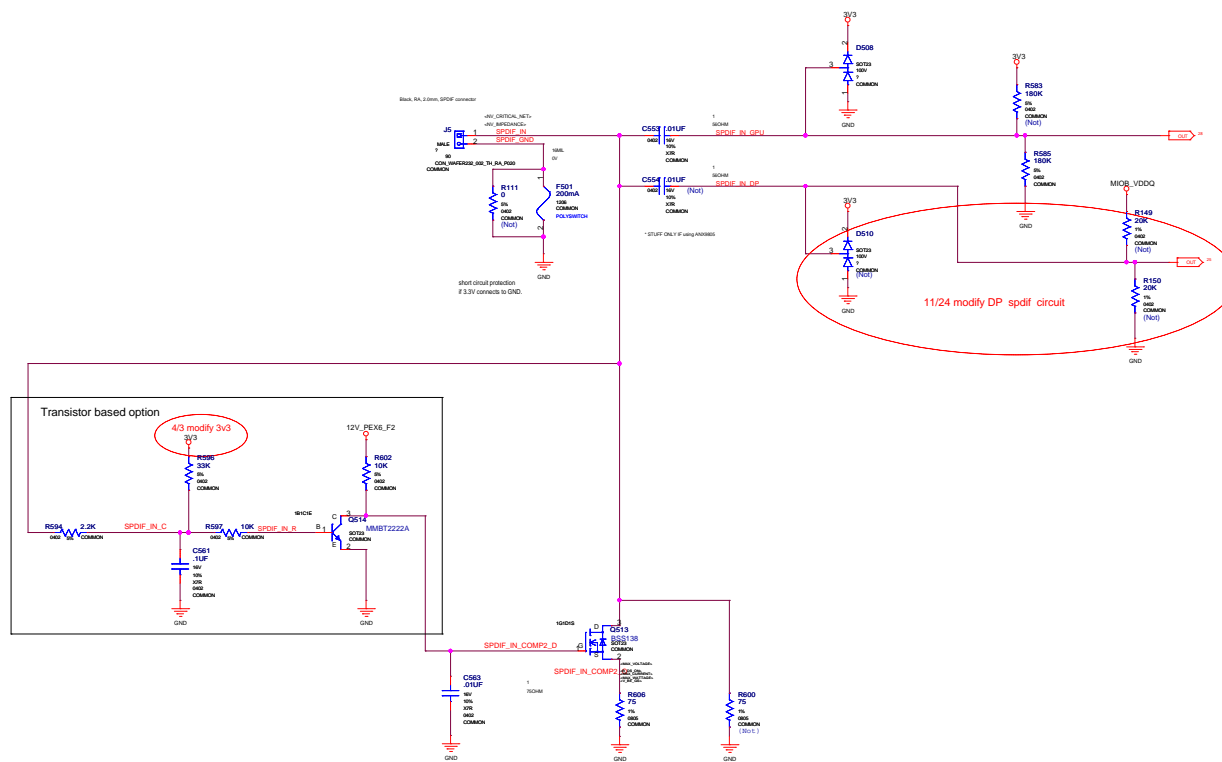
- GPIO3 - to DP mode, from pin 13, grounded on AN08B02
 - place GND resistor away from ARK device if needed
- GPIO2 - grounded on AN08B02
 - place GND resistor away from ARK device if needed
- CC - support via FET and pull-up, grounded on AN08B02
 - place GND resistor away from ARK device if needed
- GPIOF1 - to GND, input select 0/1 through internal register
- GPIOF0 - support for Audio input, grounded on AN08B02
 - place GND resistor away from ARK device if needed
- NC - to GND



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Connectors: SPDIF

SPDIF INPUT / Level Detection



Transistor based option

4/3 modify 3v3

12V_PEX6_F2

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ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Connectors: SPDIF



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Monday April

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Chart 2


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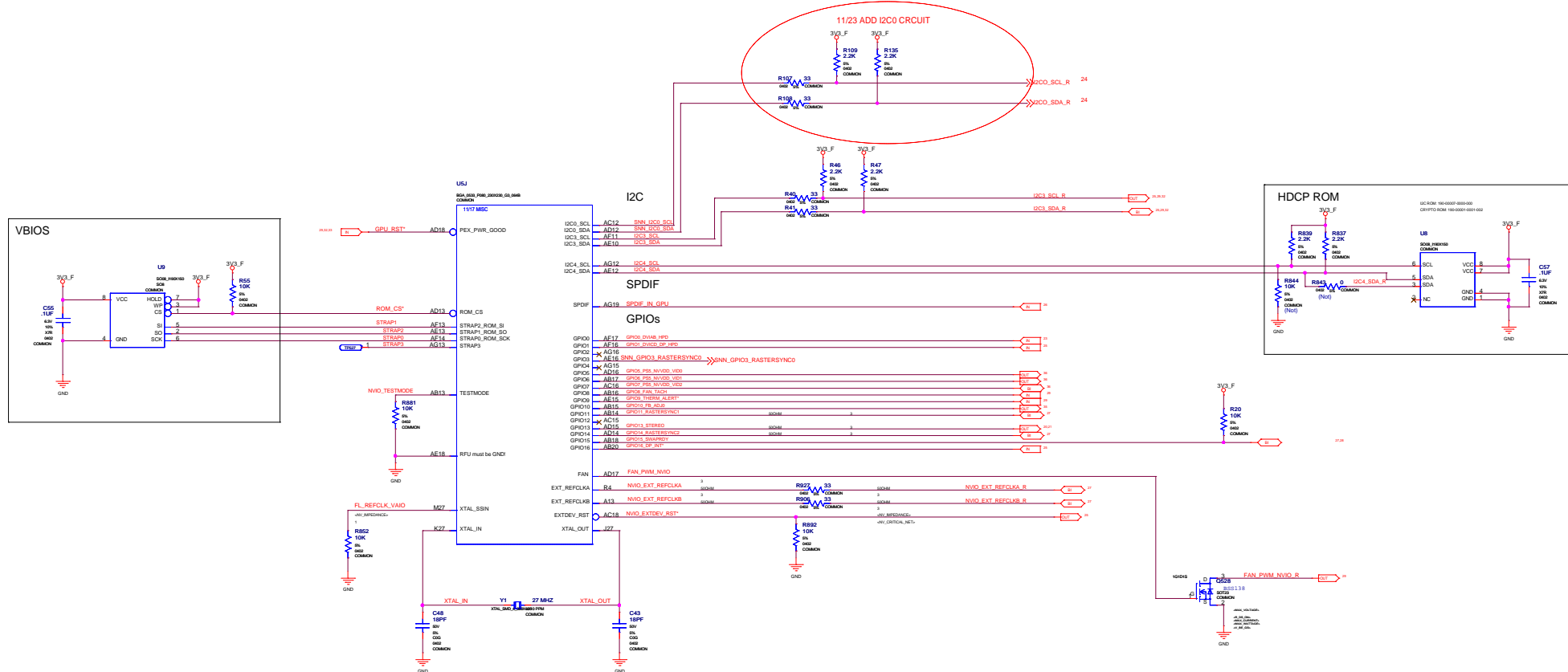
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MISC: GPIO / XTAL / VBIOS / HDCP / I2C

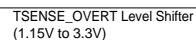


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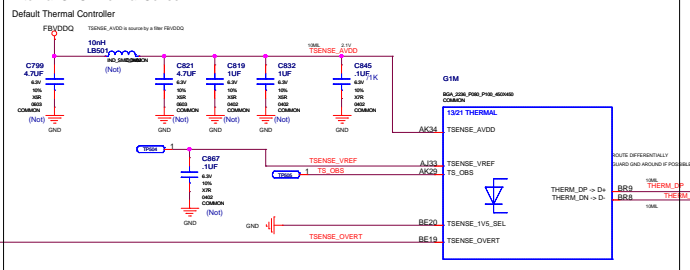
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BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
MISC: GPIO / XTAL / VBIOS / HDCP / I2C

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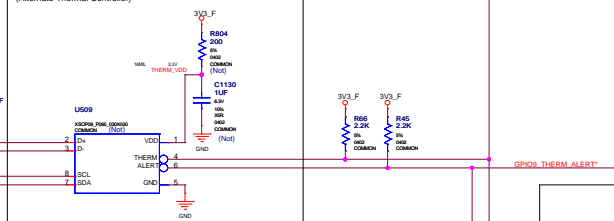
MISC: FAN / THERM



Internal GPU Thermal Sensor



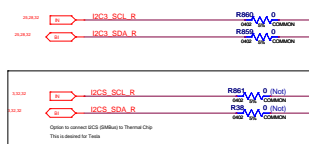
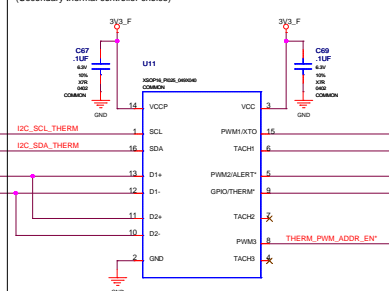
tsuruse_ts2_ssel=2: TS_AVDD = 1.7V ~ 2.1V (default) (wired to gnd)
tsuruse_ts2_ssel=1: TS_AVDD = 1.65V ~ 1.7V (wired to NVVDD)



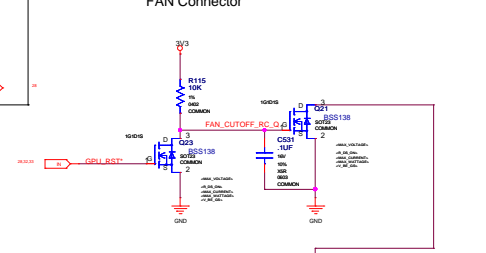
Note: PCR internal thermal controls and external controls will be DN1

ADT7473

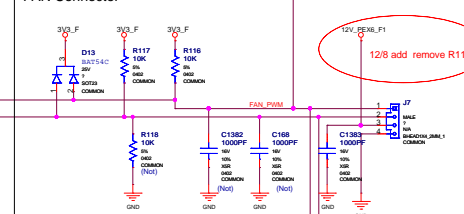
(Secondary thermal controller choice)



FAN Connector



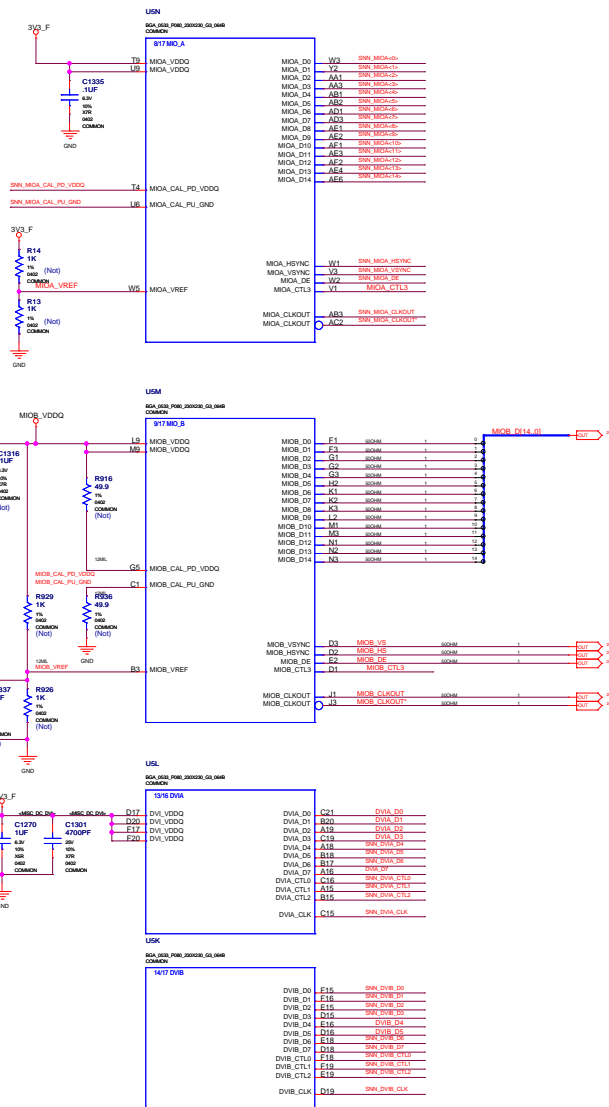
FAN Connector



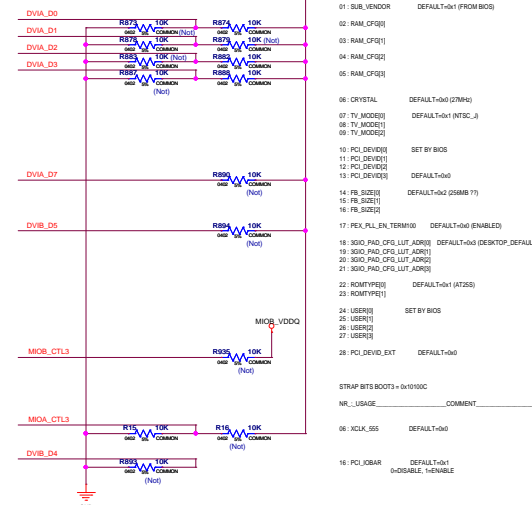
GPU Driven Fan and Tach



MISC: MIO / DVI / STRAPS



STRAPS



F	STRAP BITS BOOT0 - 0x01000	
	NR__USAGE	COMMENT
01	0V_VINDR	DEFAULT=0x0(WIDE)
01	SUB_VENDOR	DEFAULT=0x1(FROM BIOS)
02	RAM_CFG[0]	
03	RAM_CFG[1]	
04	RAM_CFG[2]	
05	RAM_CFG[3]	
06	CRYSTAL	DEFAULT=0x0(7MHz)
07	TV_MODE[0]	DEFAULT=0x1(NTSC_3)
08	TV_MODE[1]	
09	TV_MODE[2]	
10	PCI_DEV[0]	SET BY BIOS
11	PCI_DEV[1]	
12	PCI_DEV[2]	
13	PCI_DEV[3]	DEFAULT=0x0
14	FB_SIZE[0]	DEFAULT=0x0(256MB TT)
15	FB_SIZE[1]	
16	FB_SIZE[2]	
17	PEXPL_FLR_TERM[0]	DEFAULT=0x0(ENABLED)
18	SIO0_PIO_CFG_LUT_ADDR[0]	DEFAULT=0x0(SCKPT0_DEFAULT)
19	SIO0_PIO_CFG_LUT_ADDR[1]	
20	SIO0_PIO_CFG_LUT_ADDR[2]	
21	SIO0_PIO_CFG_LUT_ADDR[3]	
22	ROMVTP[0]	DEFAULT=0x1(JTAG2S)
23	ROMVTP[1]	
24	USER[RN]	SET BY BIOS
25	USER[EN]	
26	USER[EN2]	
27	USER[EN3]	
28	PCI_DEV[4]	DEFAULT=0x0
	STRAP BITS BOOT0 - 0x01000	
	NR__USAGE	COMMENT
06	XCUL_S5S	DEFAULT=0x0
16	PCI_L0BAR	DEFAULT=0x0 L0BAR=0x0BAR=0

CFG Config With: Vendor

0000	Reserved
0001	16Mx32 512-bit Geminis
0010	32Mx32 512-bit Hyla*
0011	16Mx32 512-bit Samsung*
0100	Reserved
0101	32Mx32 512-bit Geminis
0110	32Mx32 512-bit Hyla
0111	32Mx32 512-bit Samsung
1000	Reserved
1001	16Mx32 448-bit Geminis
1010	16Mx32 448-bit Hyla
1011	16Mx32 448-bit Samsung
1100	Reserved
1101	32Mx32 448-bit Geminis
1110	32Mx32 448-bit Hyla
1111	32Mx32 448-bit Samsung

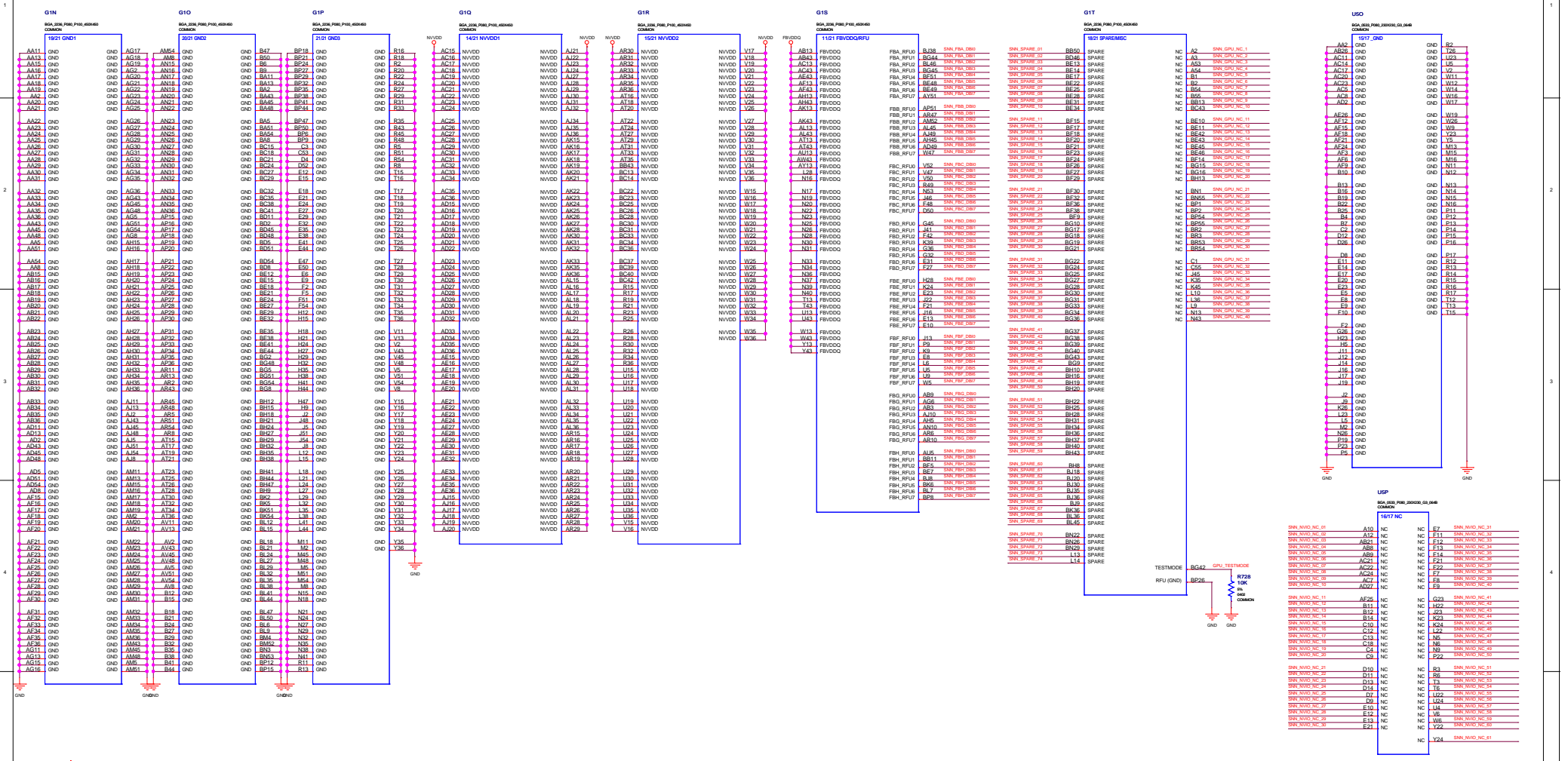
Power and GND (GPU and NVIOx)

GPU SECTION GND

GPU SECTION POWER

GPU SECTION MISC

NVIOx SECTION GND



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Power and GND (GPU and NVIOx)



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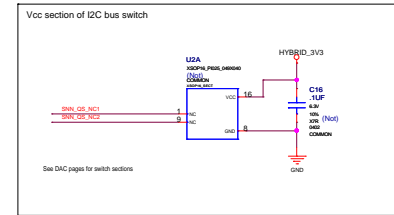
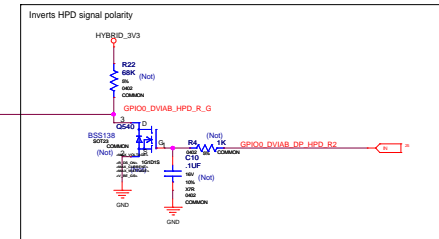
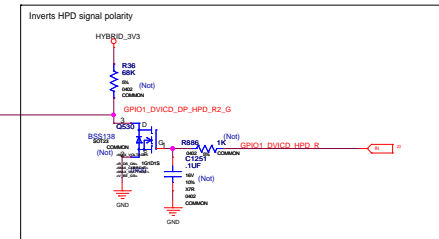
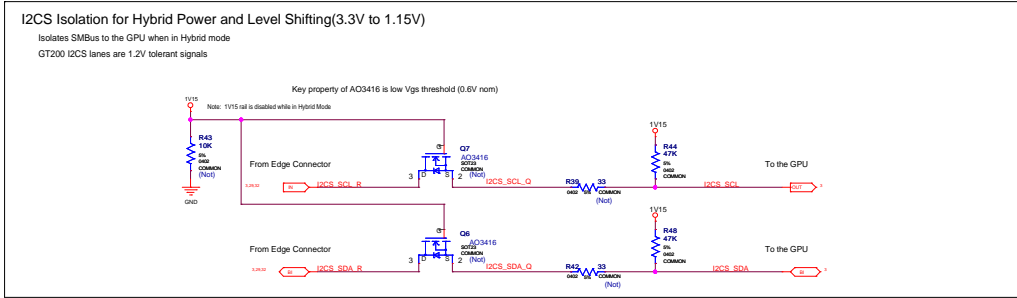
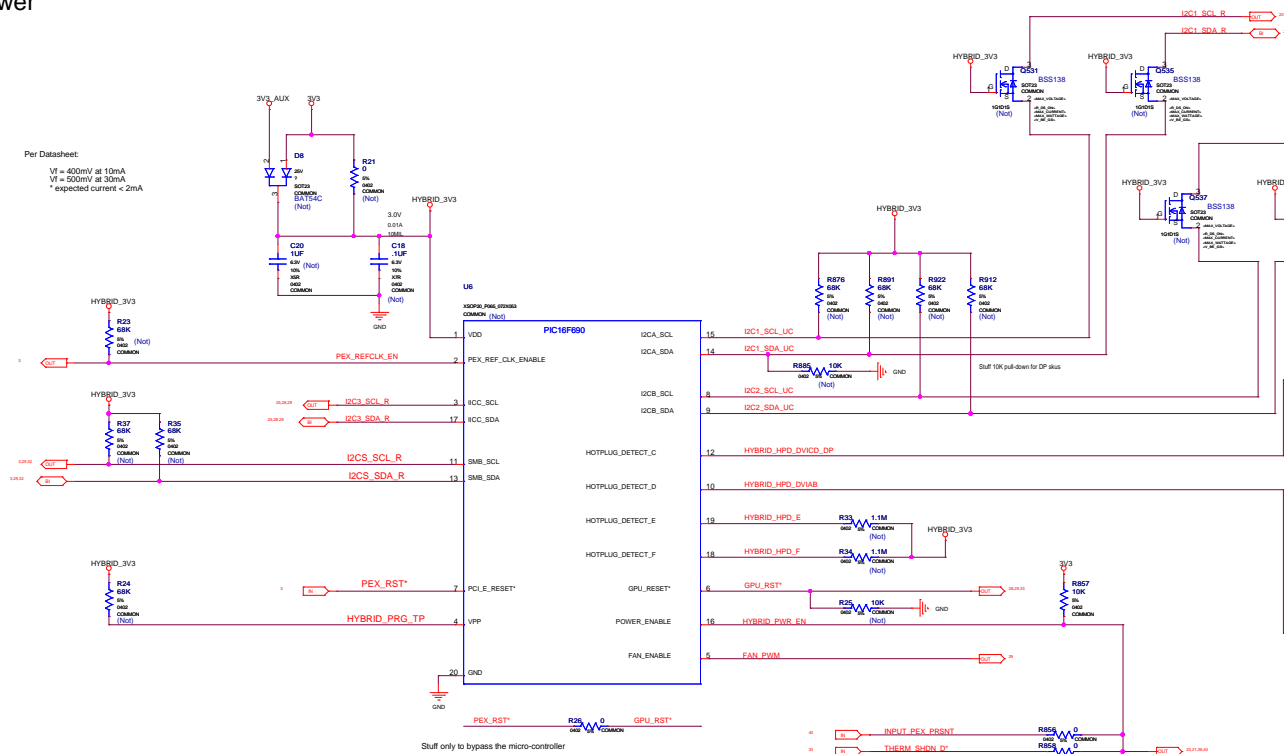
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Rev:
Date:
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Power: Hybrid Power

Per Datasheet:
VI = 400mV at 10mA
VI = 500mV at 30mA
* expected current < 2mA

Weak pull-ups needed for I2CS:
* If SMBus is isolated from the GPU
* If MB does not support SMBus
* If MB does not support 3V3ALX



ASSEMBLY
PAGE DETAIL
BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Power Hybrid Power

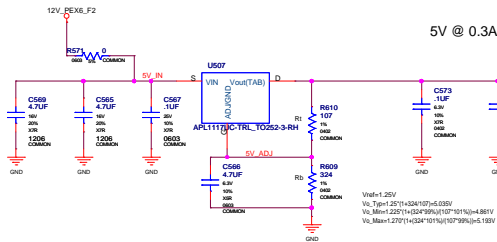
Micro-Star International Co., LTD.

Rev: <Rev>
Doc: <Doc>
Date: Monday, April 13, 2009 Sheet: 32 of 41

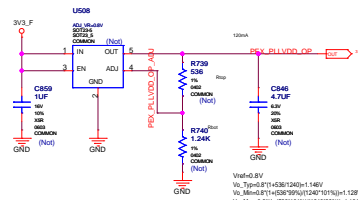
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Power Supply: 5V LDO / 3V3_DP / THERM SHUTDOWN LATCH / IFP_IOVDD / PEX_PLVDD

5V Linear



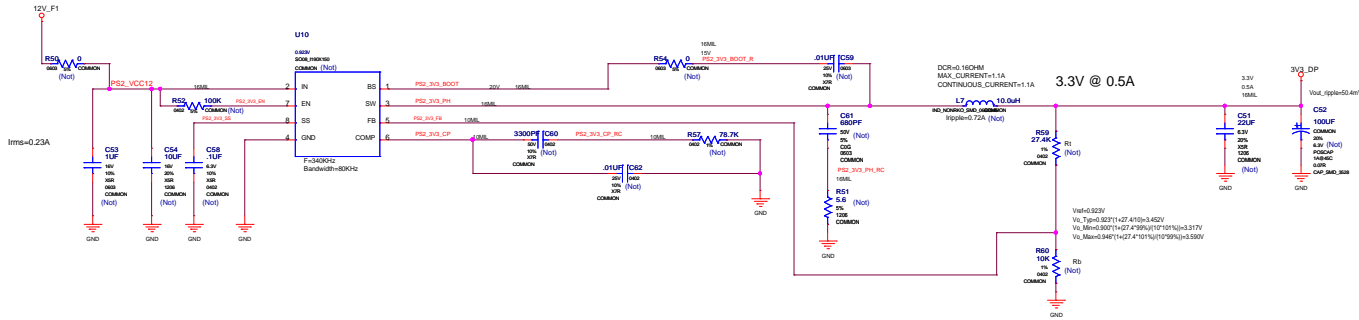
PEX PLLVDD optional Supply



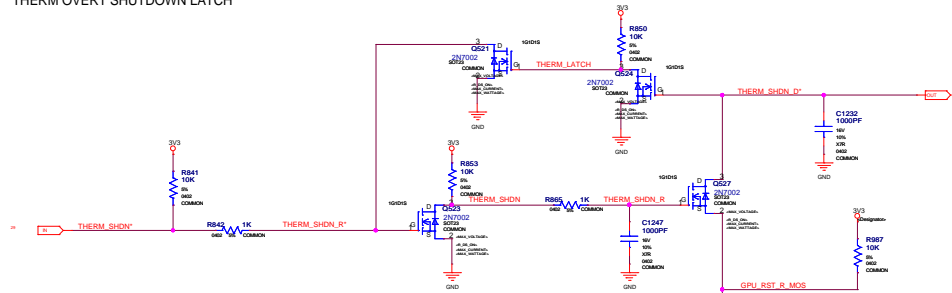
DCC_5V



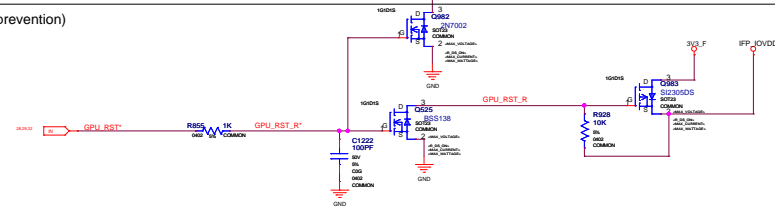
3V3_DP SWITCHER (Only required for DisplayPort SKU)



THERM OVERT SHUTDOWN LATCH



IFP_IOVDD (backdrive prevention)



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 31UFF ASSEMBLY NOTES AND BOM NOT FINAL
Power Supply 5V @ 0.3A / SHDN LATCH / IFP_IOVDD

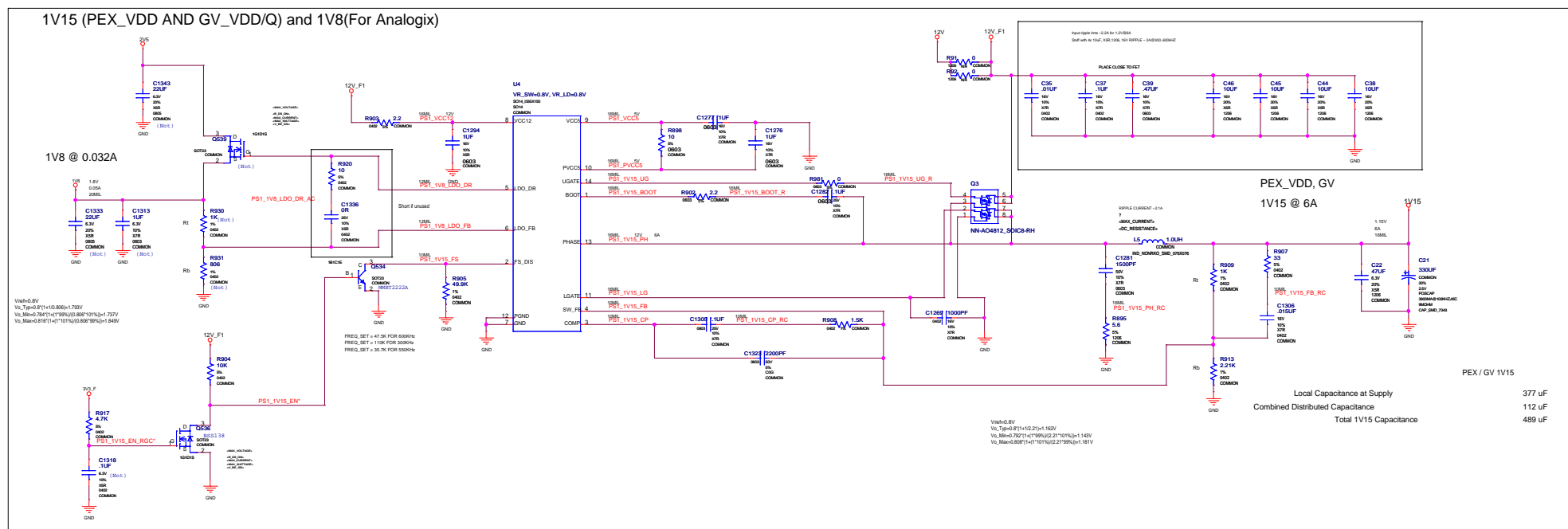
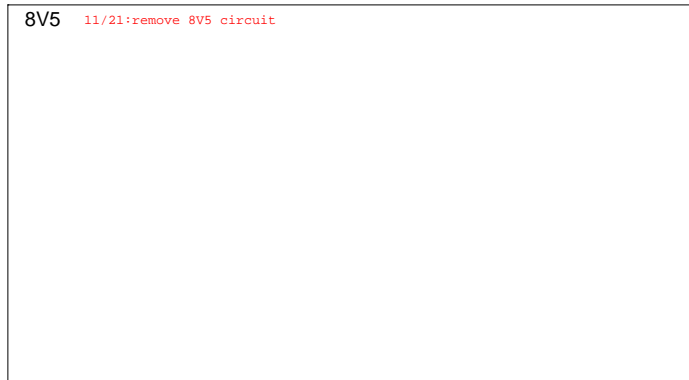
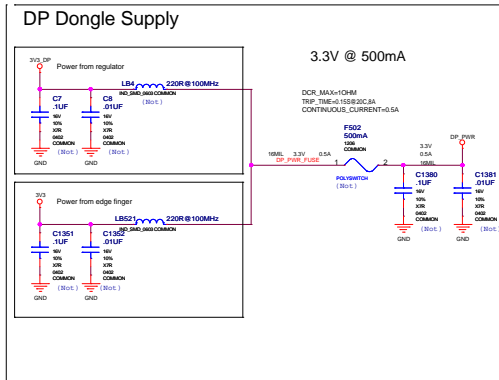
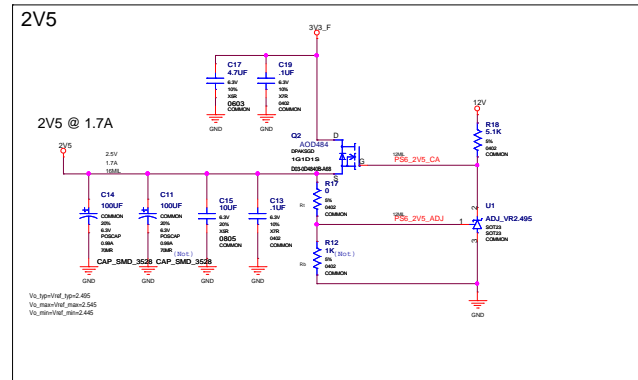


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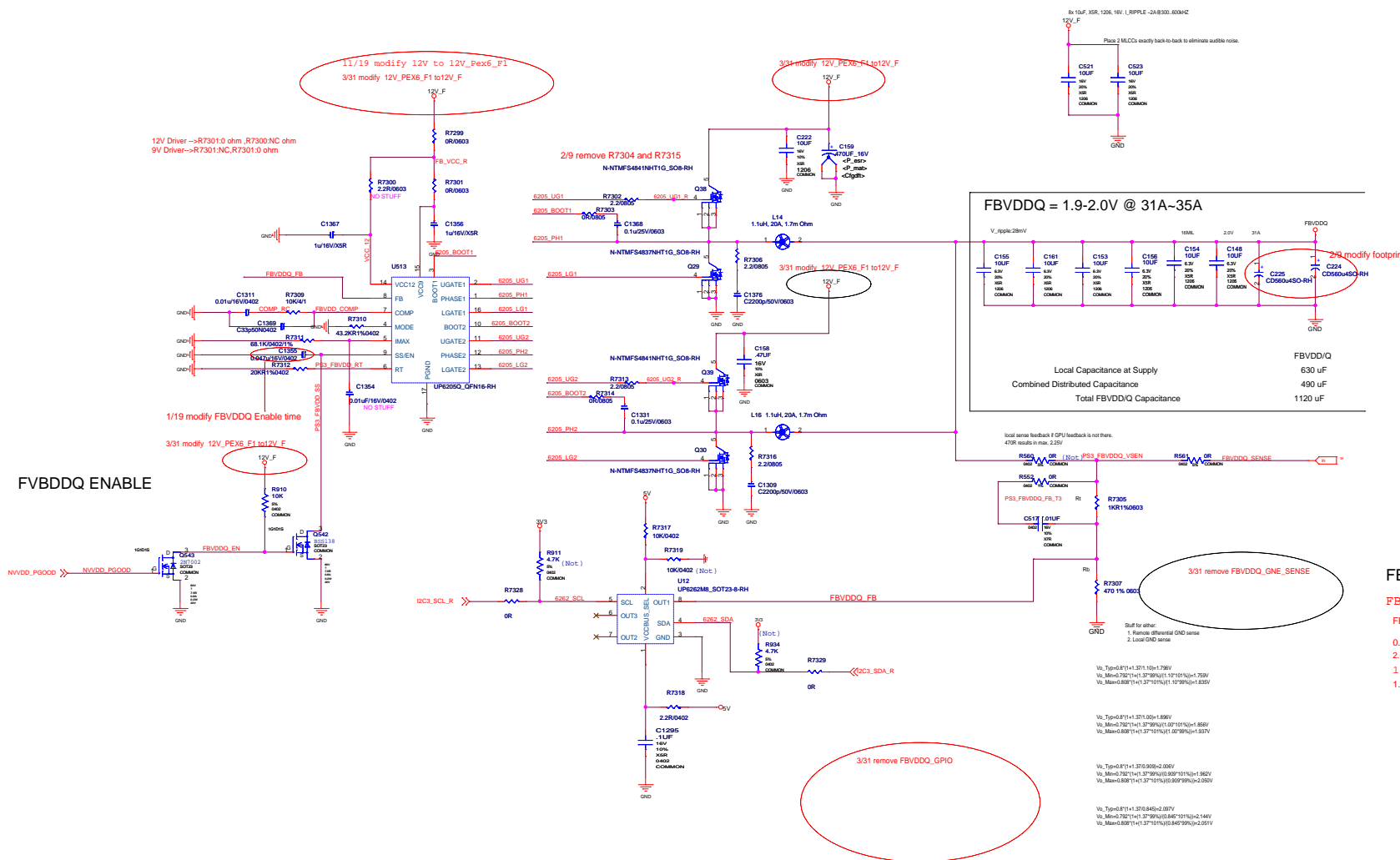
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Power Supply: 2V5, DP_PWR, 8V5 1V15 (PEX_VDD, GV_VDD)



Power Supply: Combined FBVDD/Q



nv量測
FBVDDQ:17.68A

FBVDDQ = 1.9-2.0V @ 31A~35A

[illegible]

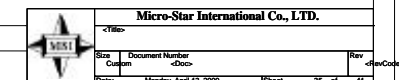
FBVDDQ Power Supply

FBVDDQ =1.9-20V @ 31A~35A

FB VOLTAGE SENSE

$$\begin{aligned} 0.6 \text{ V} &\times (1 + R_{top} / R_{bot}) \\ 2.057 \text{ V} &= 0.6 \text{ V} \times (1 + 2.55 \text{ K} / 1.05 \text{ K}) \\ 1.833 \text{ V} &= 0.6 \text{ V} \times (1 + 2.55 \text{ K} / 1.24 \text{ K}) \\ 1.93 \text{ V} &= 0.6 \text{ V} \times (1 + 2.55 \text{ K} / 1.15 \text{ K}) \end{aligned}$$
$$\begin{aligned} V_{o_Typ} &= 0.8 \cdot (1 + (1.37/1.10)) = 1.796V \\ V_{o_Min} &= 0.792 \cdot (1 + (1.37/99\%)) (1.10/101\%) = 1.750V \\ V_{o_Max} &= 0.808 \cdot (1 + (1.37/101\%)) (1.10/99\%) = 1.835V \end{aligned}$$
$$\begin{aligned} V_{o_Typ} &= 0.8 * (1 + 1.37 / 1.00) = 1.896V \\ V_{o_Min} &= 0.792 * (1 + (1.37 * 99\%) / (1.00 * 101\%)) = 1.856V \\ V_{o_Max} &= 0.808 * (1 + (1.37 * 101\%) / (1.00 * 99\%)) = 1.937V \end{aligned}$$
$$\begin{aligned} V_{o_Typ} &= 0.8 \cdot (1 + (1.37/0.909)) = 2.006V \\ V_{o_Min} &= 0.792 \cdot (1 + (1.37/99\%)) / (0.909/101\%) = 1.962 \\ V_{o_Max} &= 0.808 \cdot (1 + (1.37/101\%)) / (0.909/99\%) = 2.050 \end{aligned}$$
$$\begin{aligned} V_{o_Typ} &= 0.8 \cdot (1 + 1.37/0.845) = 2.097V \\ V_{o_Min} &= 0.792 \cdot (1 + (1.37/99\%)(0.845/101\%)) = 2.144V \\ V_{o_Max} &= 0.808 \cdot (1 + (1.37/101\%)(0.845/99\%)) = 2.051V \end{aligned}$$

ASSEMBLY PAGE DETAIL	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL Power Supply: Combined FBVDDQ
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Power Supply: NVVDD Regulator

nv量測
NVVDD:91.62A
diag:112.1A

GTS 260 VID
GPIO[7..5]=000=>1.025V
GPIO[7..5]=100=>1.125V
GPIO[7..5]=001=>1.05V
GPIO[7..5]=010=>1.0625V
11/05 modify GPIO 7-5 三種電壓mode

GTS 275
GPIO[10..5]=000=>1.1875V
GPIO[10..5]=010=>1.125V
GPIO[10..5]=011=>1.05V
GPIO[10..5]=001=>1.175V

GT200-103-B3					
BOOT VOLTAGE		1.1875V	0	0	0
VB0	3D MODE, P0 MODE;	1.1750V	0	0	1
VB1	3D MODE, P0 MODE;	1.1250V	0	1	0
VB0/VB1	2D MODE, P8 MODE; 2D MODE, P12 MODE; 2D MODE, DOS;	1.0500V	1	0	1

NVVDD Voltage Select		
Regulator: NCP2305		
Control via I2C (GPIO[3..0])		
VID	NVVDD	
543210		
011001	1.23750	(OFFSET +200mV)
000001	1.0500	VOLTAGE1
000110	0.93750	(OFFSET -100mV)
011000	1.26250	(OFFSET +200mV)
000001	1.06250	VOLTAGE2
000101	0.96250	(OFFSET -100mV)
110101	1.32500	(OFFSET +200mV)
111101	1.12500	VOLTAGE3
100010	1.02500	(OFFSET -100mV)
010011	1.38750	(OFFSET +200mV)
011011	1.18750	DEFAULT
000000	1.08750	(OFFSET -100mV)

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ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL Power Supply: NVVDD REGULATOR




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1
2
3
4
5

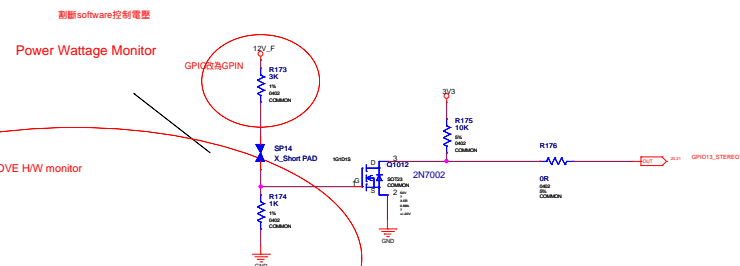


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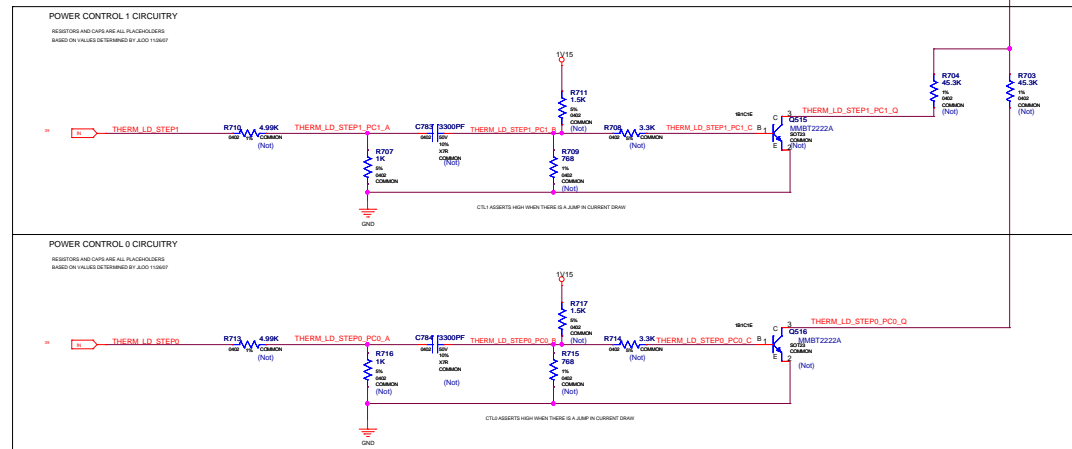
Power Supply: NVVDD Phase 5~8 powered from internal PEX edge connector

	Micro-Star International Co., LTD.		
	<Title>		
	Size Custom	Document Number <Doc>	Rev <Rev Code>
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Power Supply: NVVDD power control

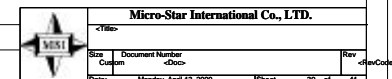


NVVDD & FBVDDQ SENSE/MSUR



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	NVDD & FBVDDQ SENSEMSUR

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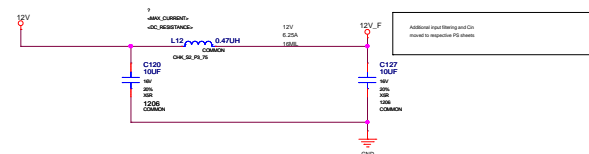


Power: Input Rail Filter and Detection Logic

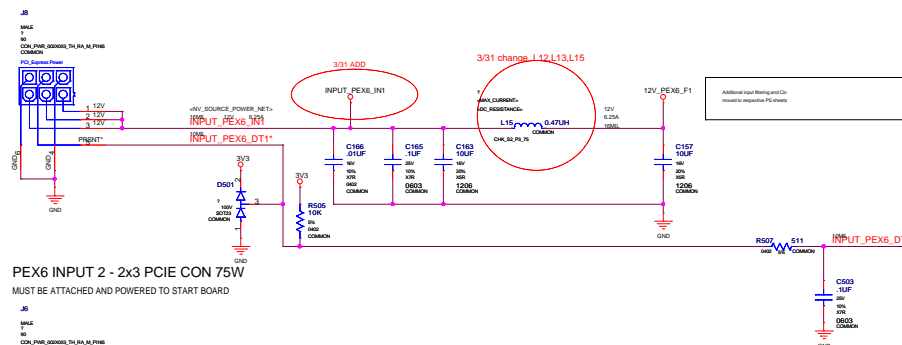
Connector Power State Table

2d3 Connector	2nd Connector		Power	STATE
Connected	Connected		220W	Full Pot
Connected	Not Connected		150W	Board Off
Not Connected	Connected		150W	Board Off
Not Connected	Not Connected		75W	Board Off

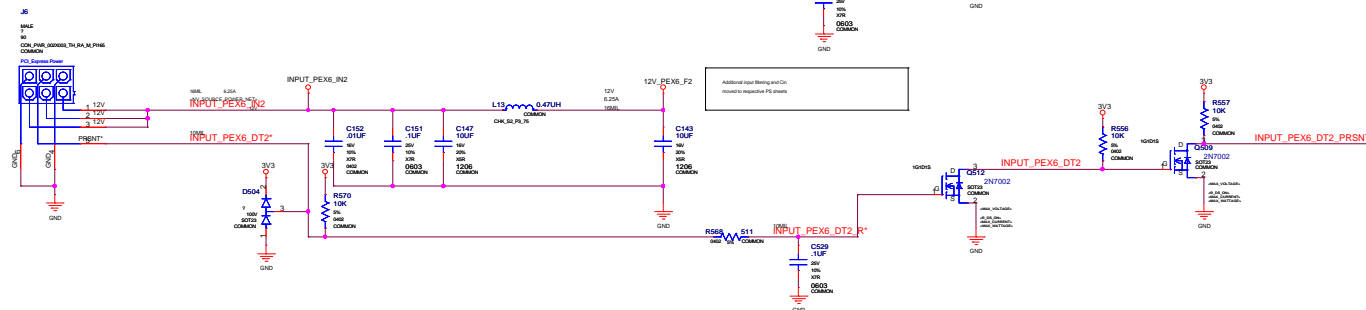
PEX 12V INPUT - 66W



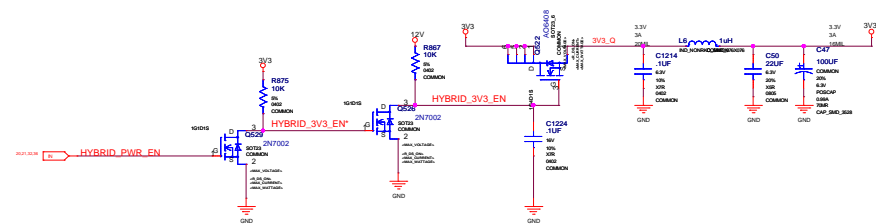
PEX6 INPUT 1 - 2x3 PCIE CON 75W
MUST BE ATTACHED AND POWERED TO START BOARD



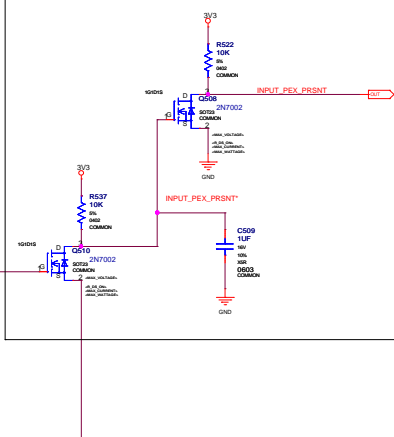
PEX6 INPUT 2 - 2x3 PCIE CON 75W
MUST BE ATTACHED AND POWERED TO START BOARD



PEX 3V3 INPUT - 10W



Summary PEX input present



Thermal/Mechanical/ID

Bracket and Assembly



GPU Socket



GPU Stiffener



NVIOx Socket

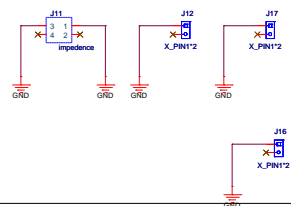
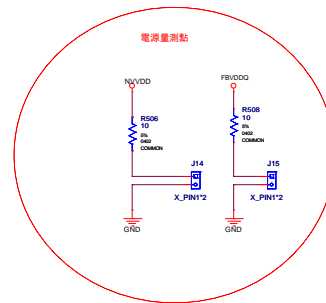
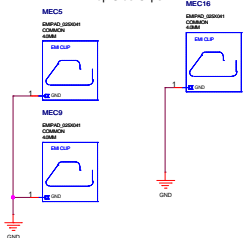


Hockey Stick Retention Mechanism

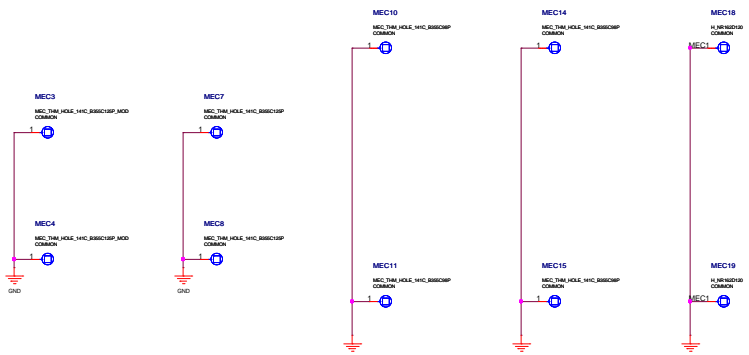


EMI Gnd Clips

Top Side Clips



THERMAL/MECHANICAL HOLES



ASSEMBLY
PAGE DETAIL

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Thermal/Mechanical



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