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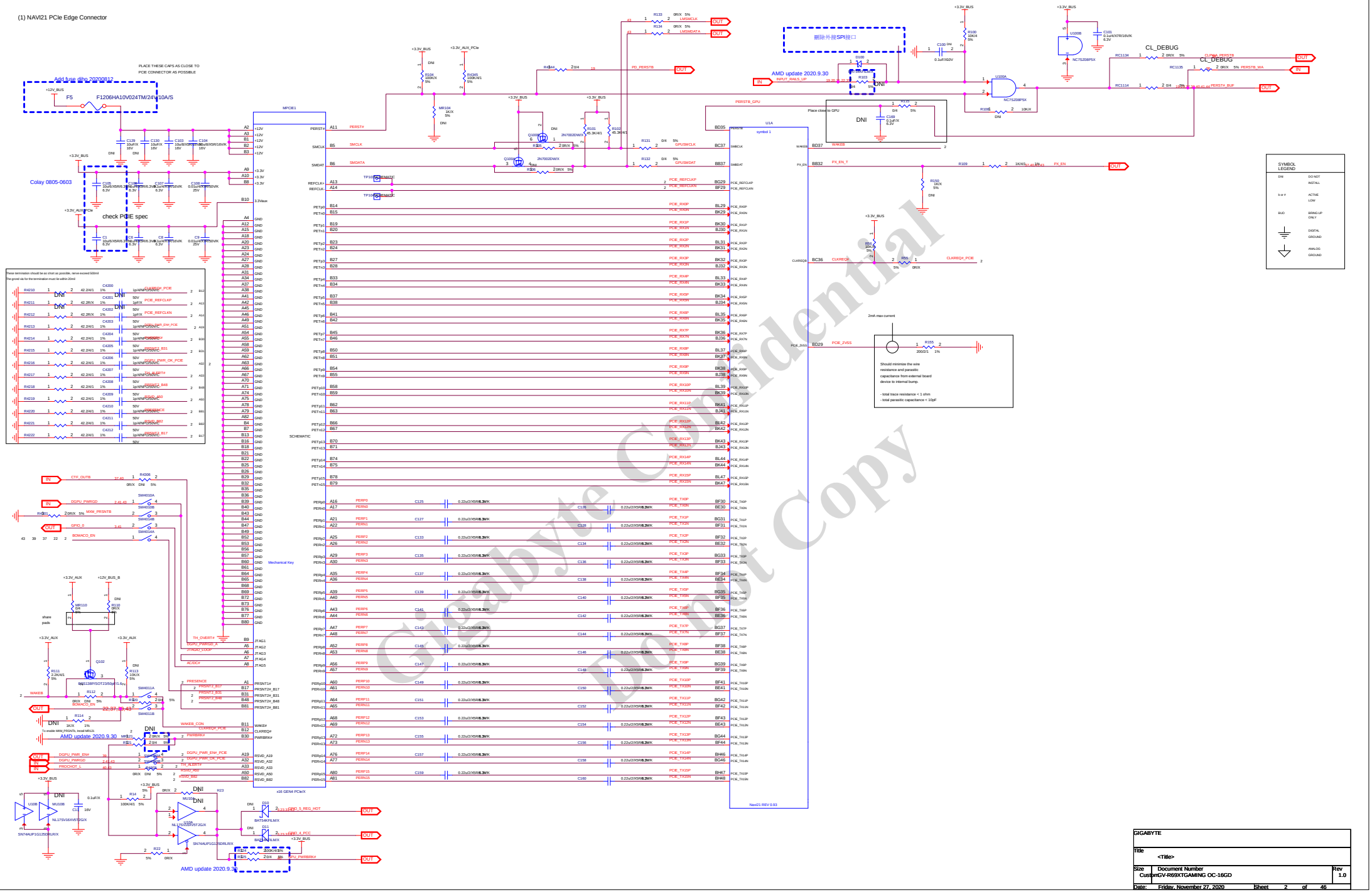

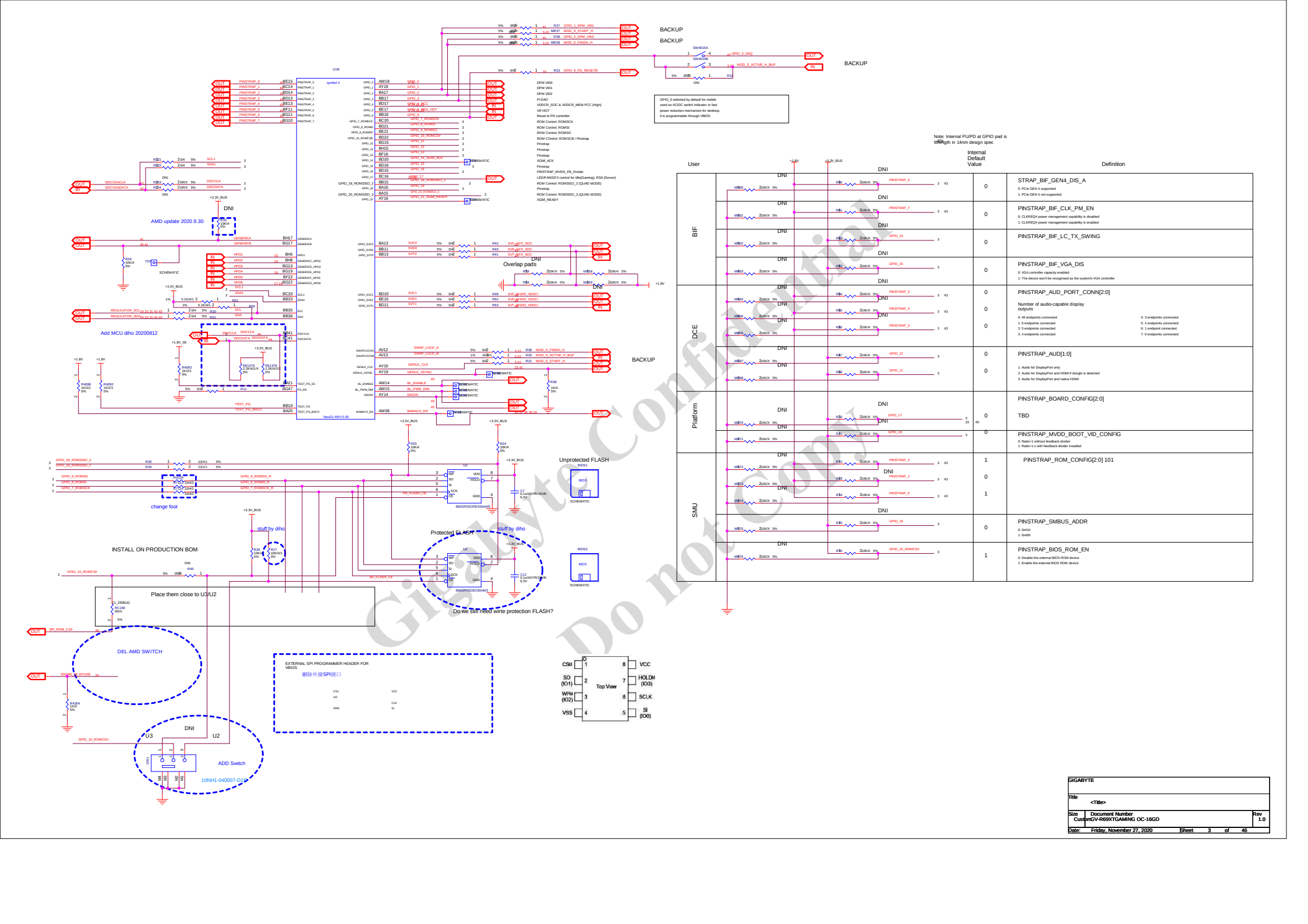

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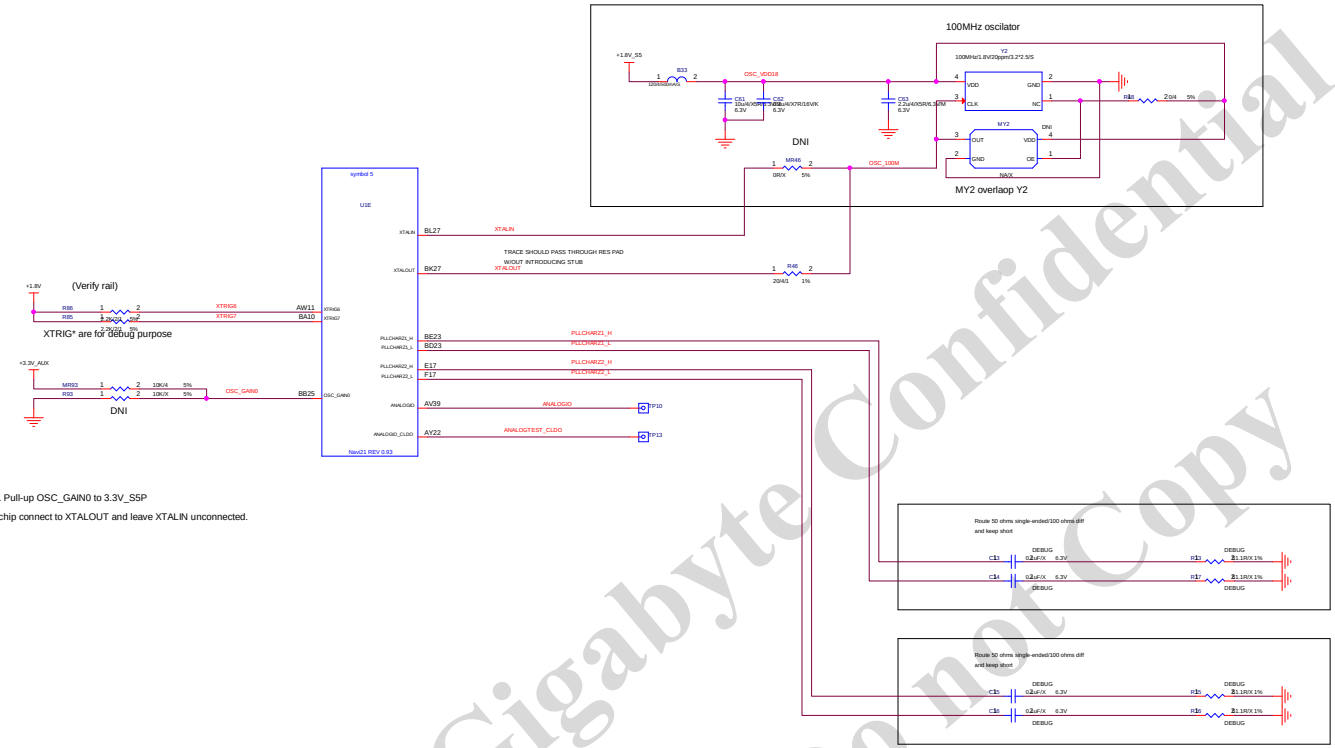

Default OSC_GAIN is 0x7. Pull-up OSC_GAIN0 to 3.3V_S5P

When 0x7, external clock chip connect to XTALOUT and leave XTALIN unconnected.

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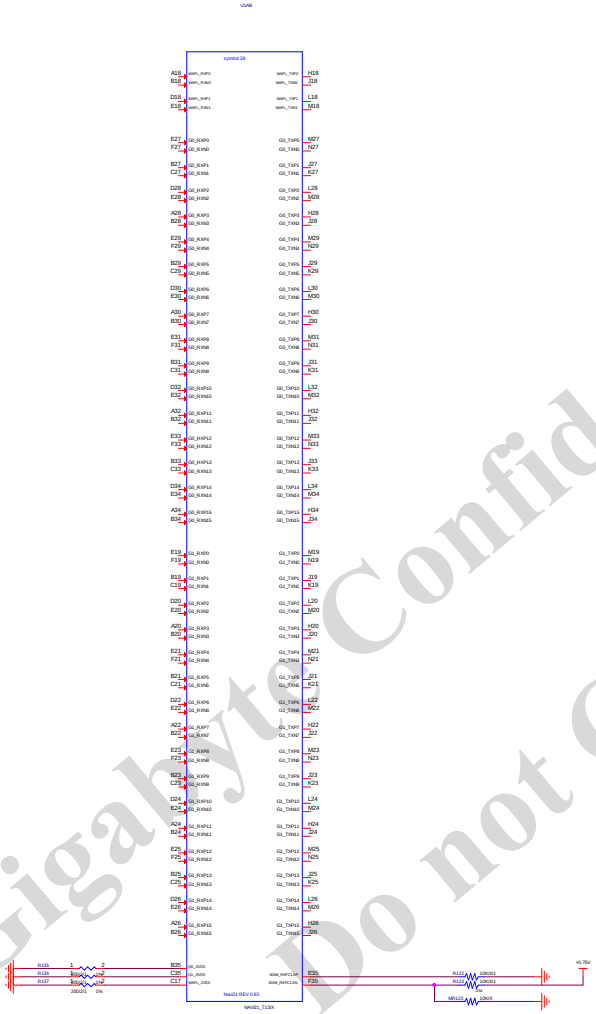
Navi21 XGMI LINK 0 & 1



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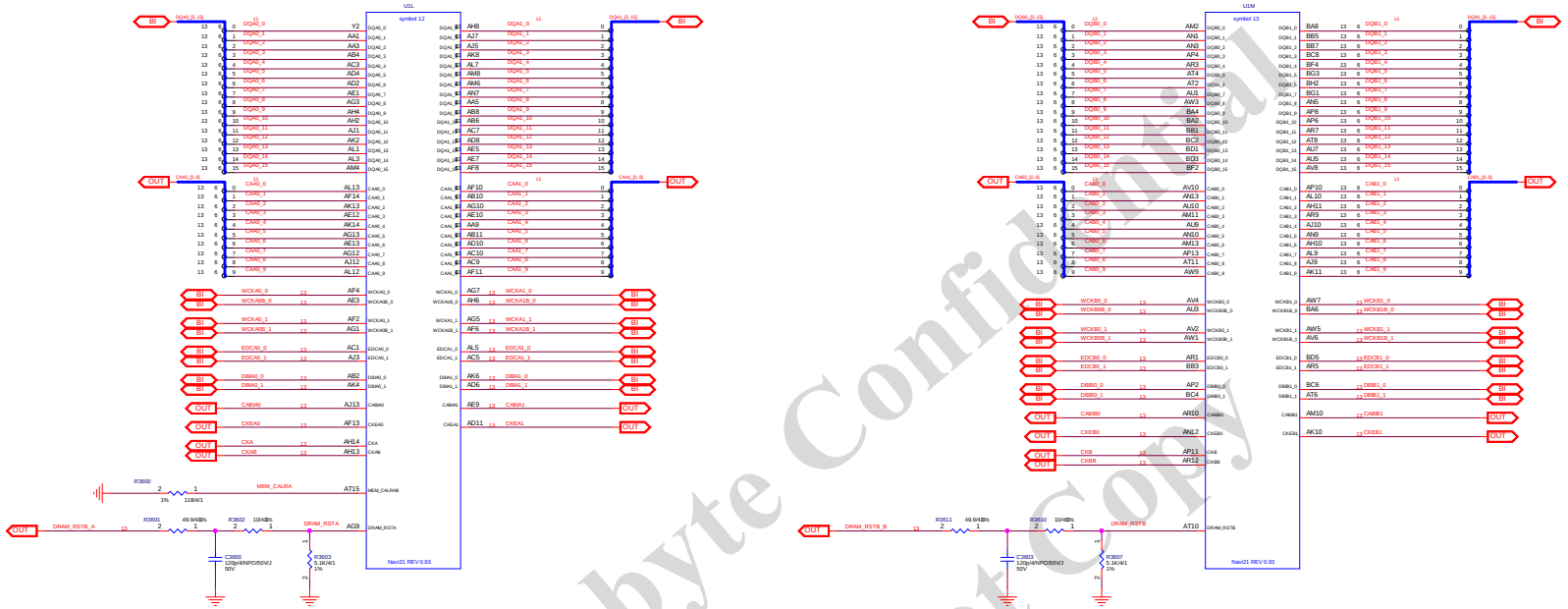
(1) NAVI 10 MEM INTERFACE CH A/B



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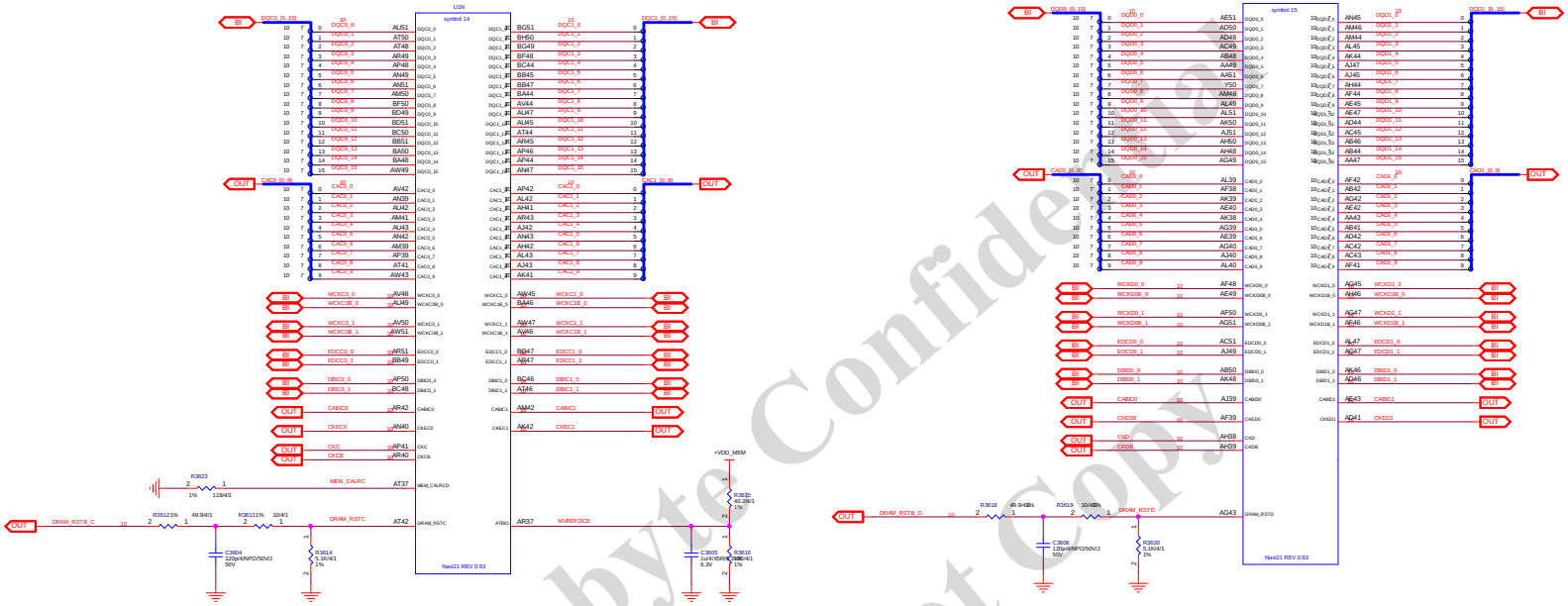
(2) NAVI 10 MEM INTERFACE CH C/D



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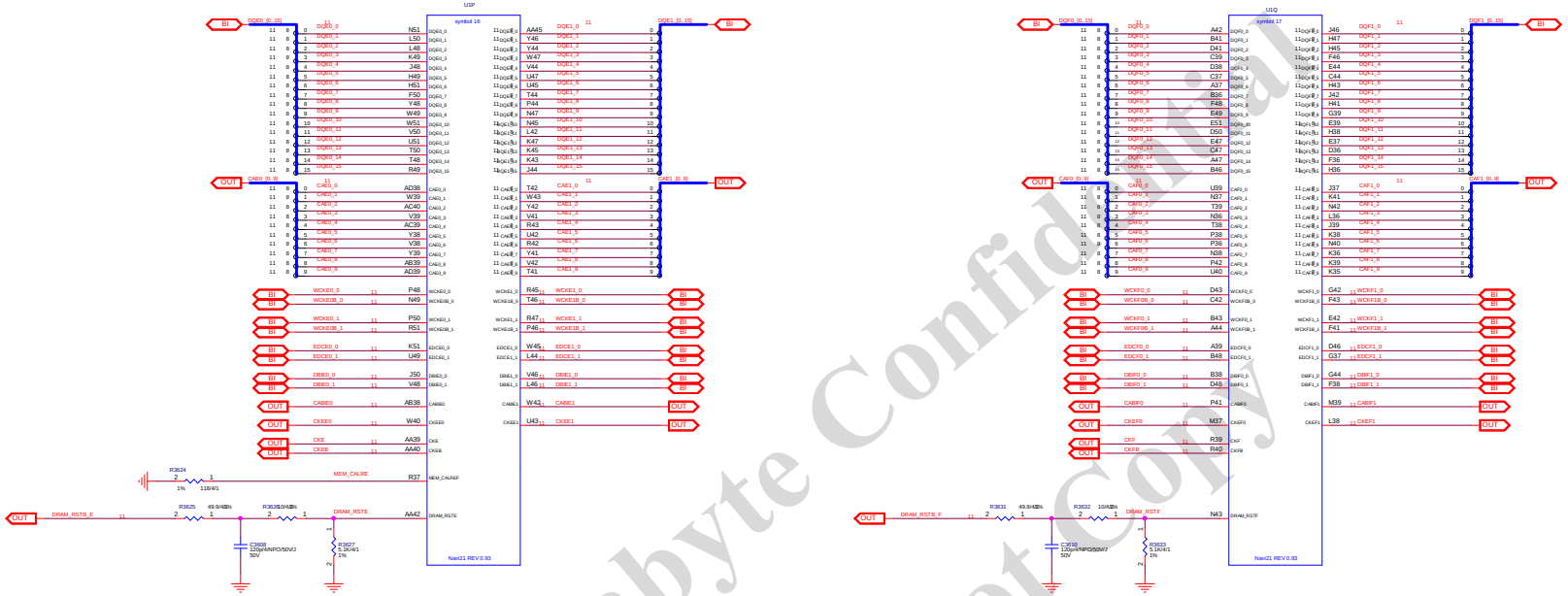

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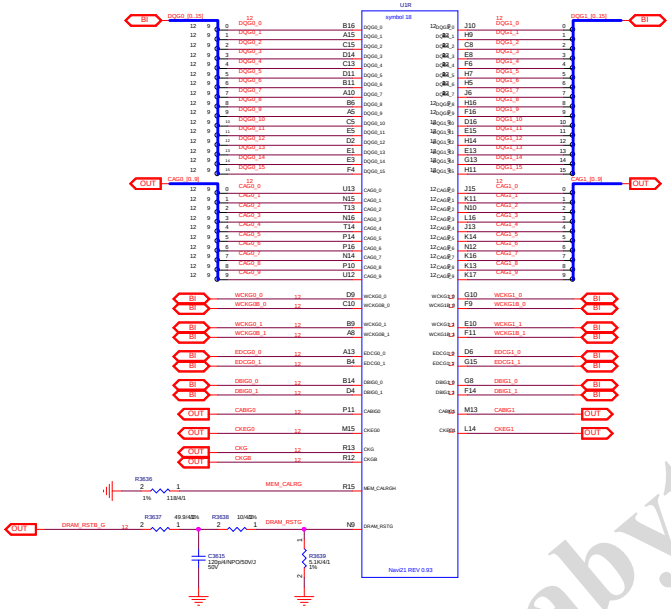
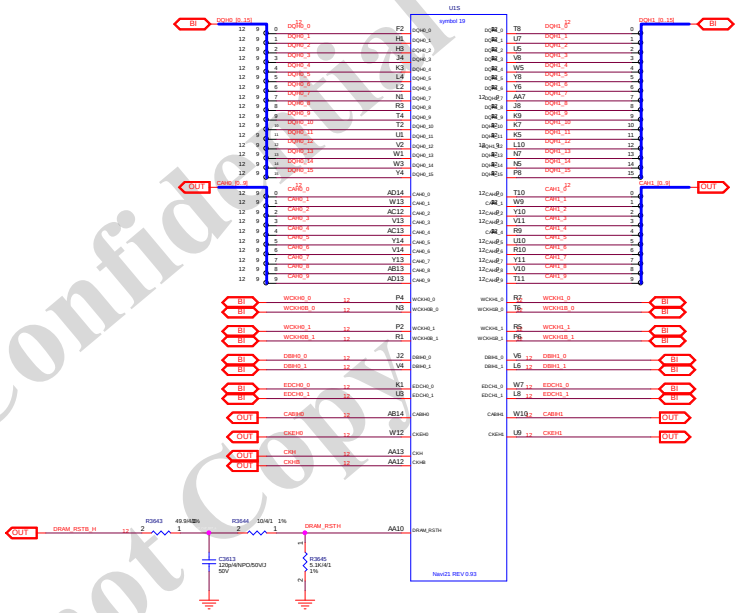
(4) NAVI 10 MEM INTERFACE CH G/H





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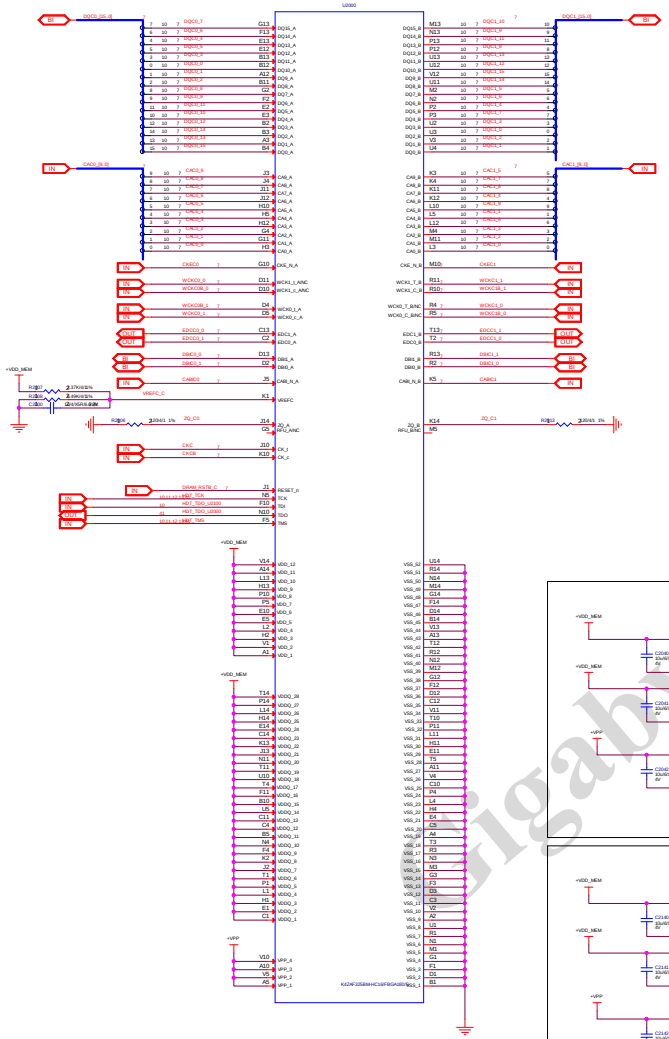
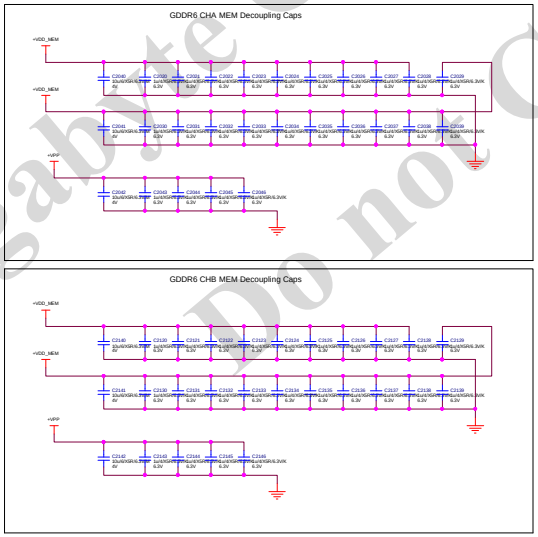
ASIC CH0 -> MEM CHA
ASIC CH1 -> MEM CHB





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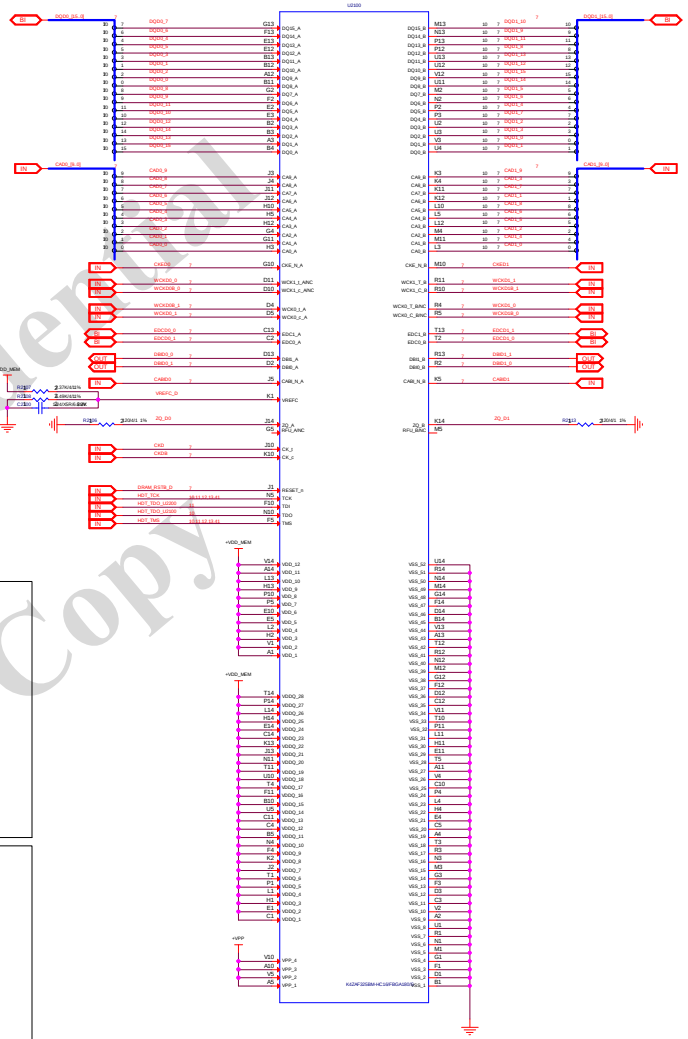

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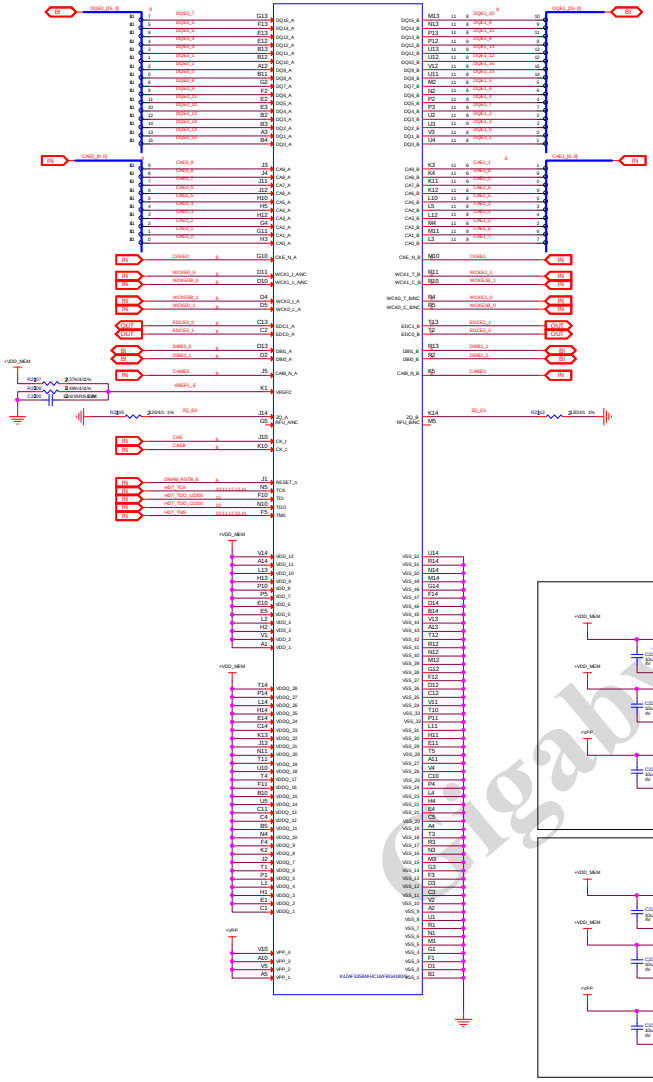

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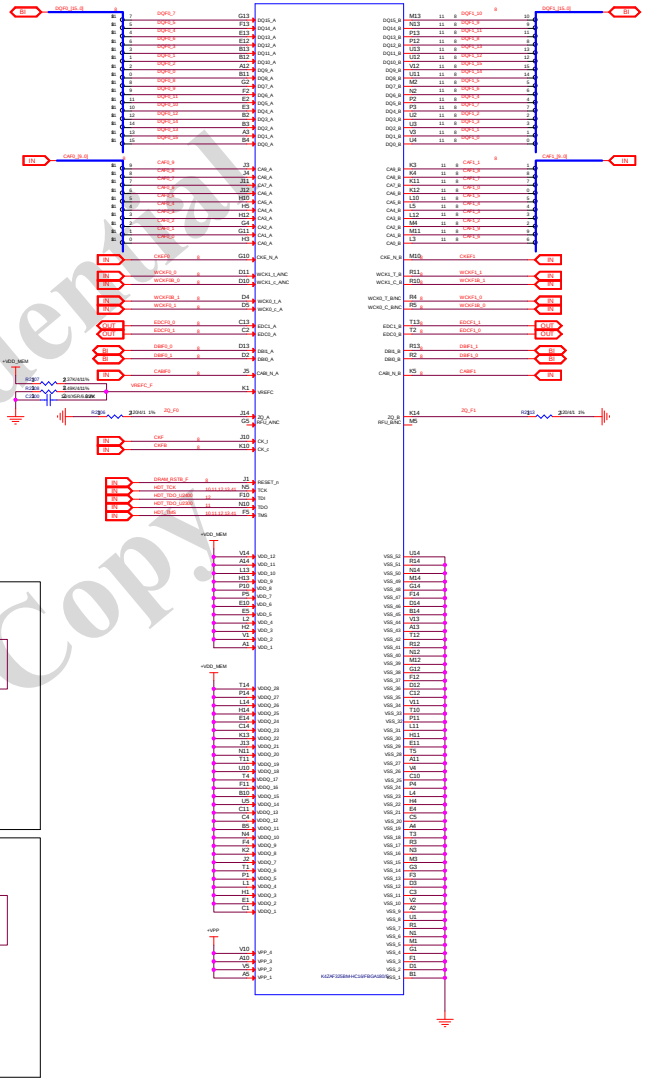

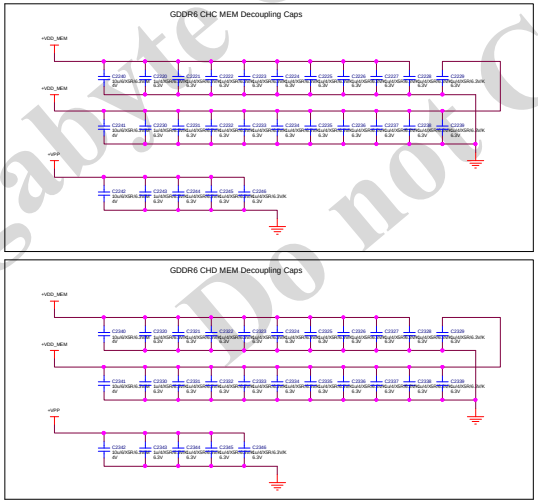

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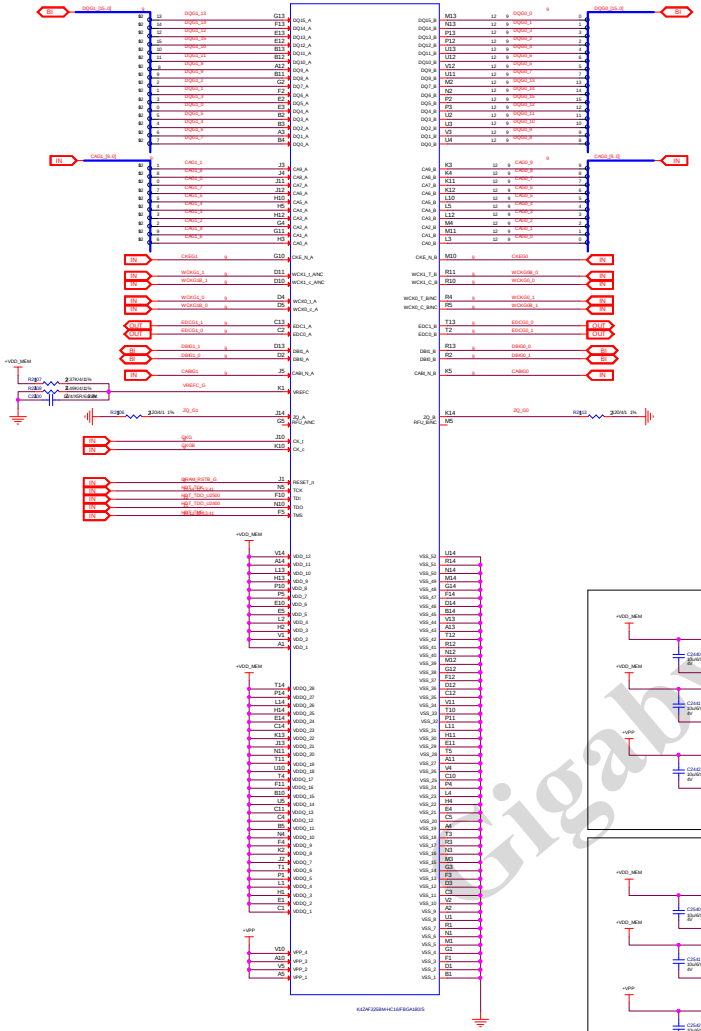

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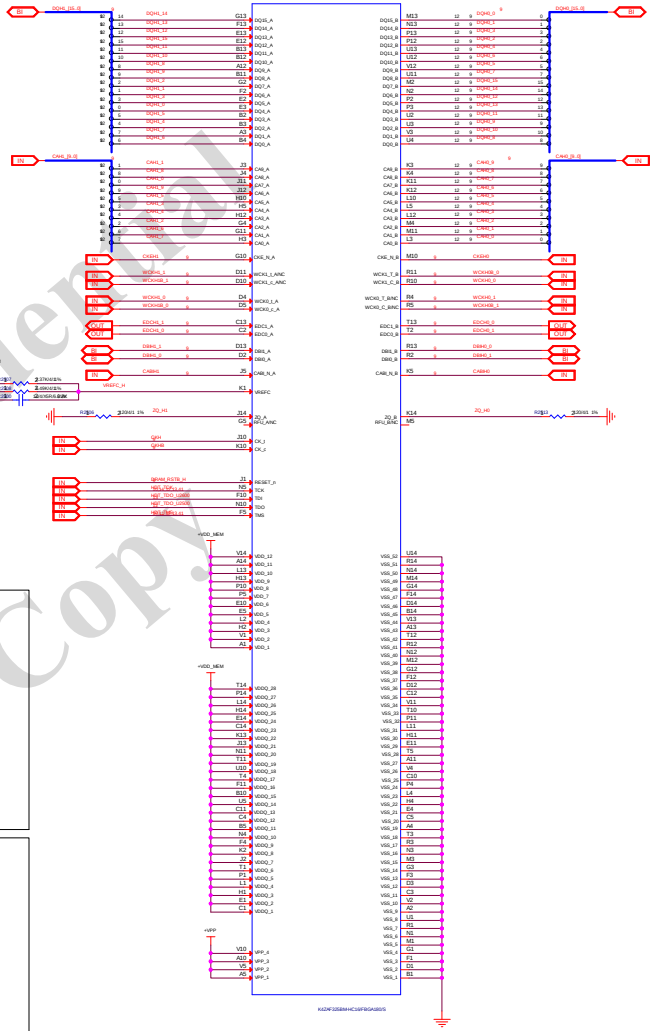

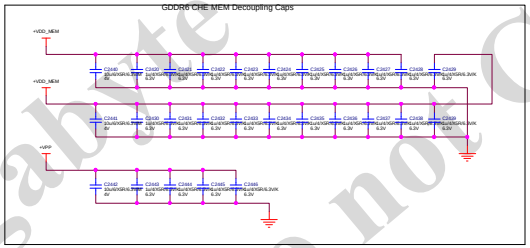

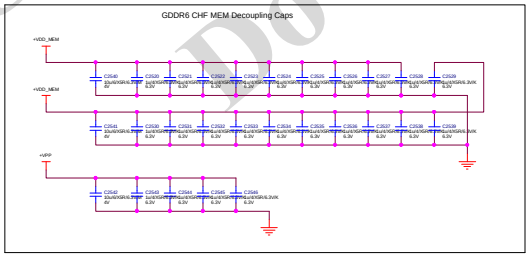

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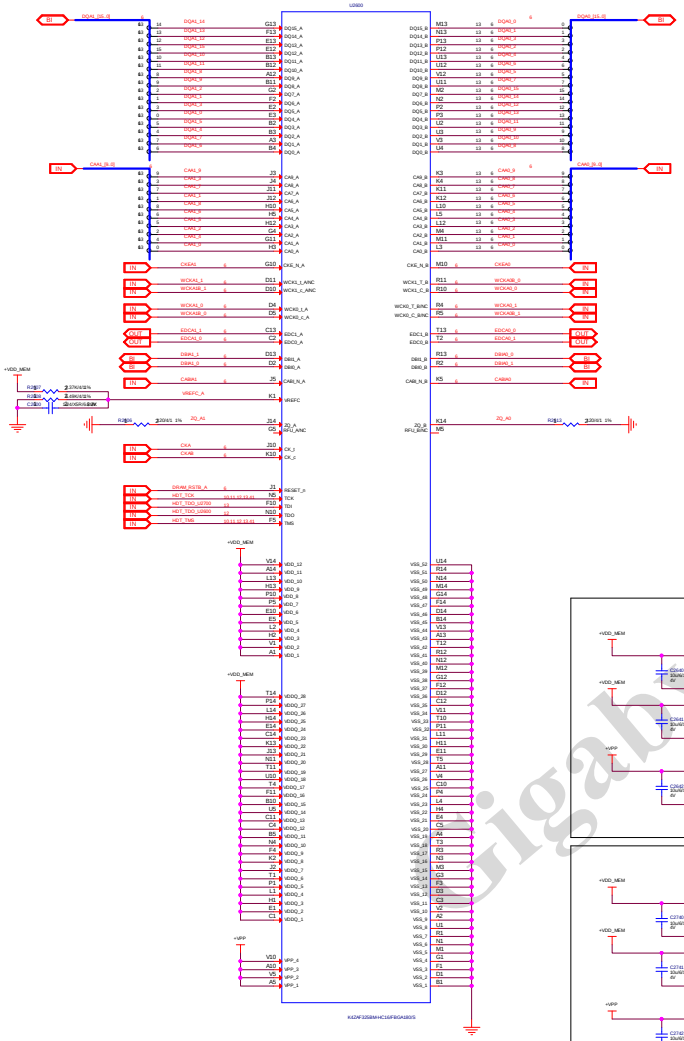

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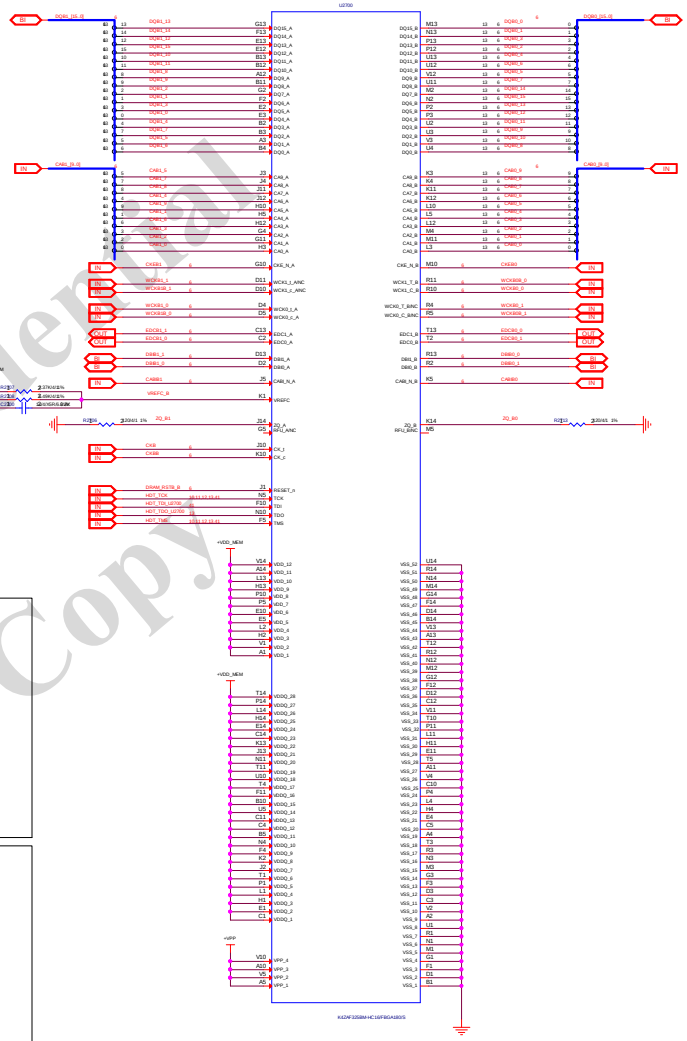

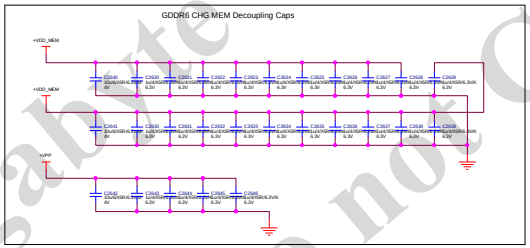

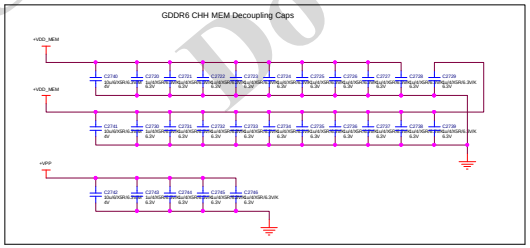

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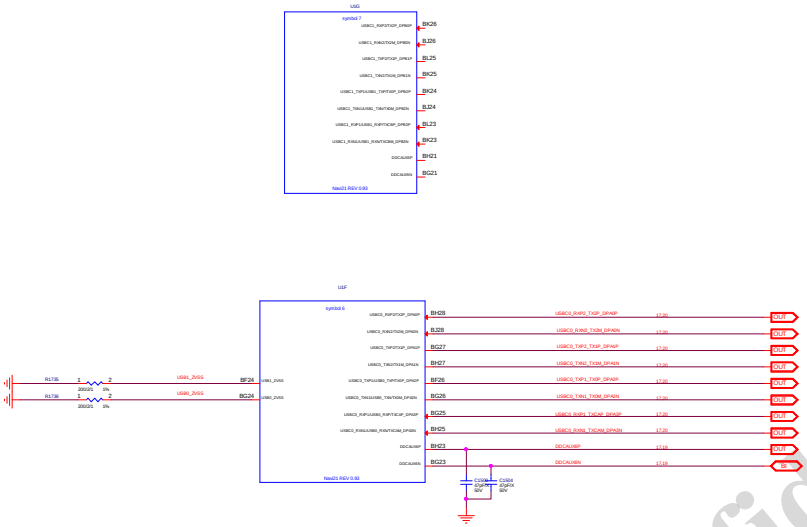

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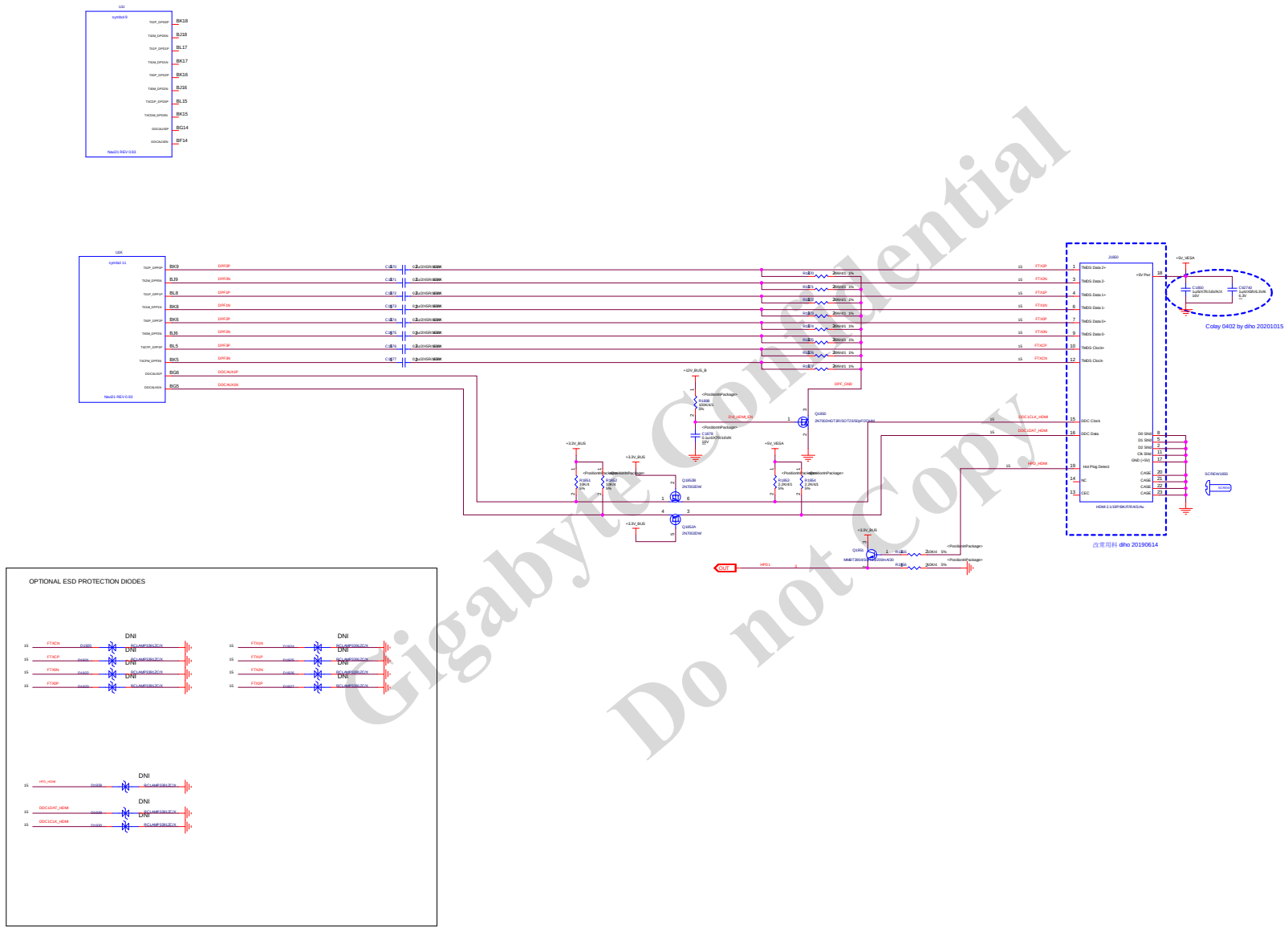

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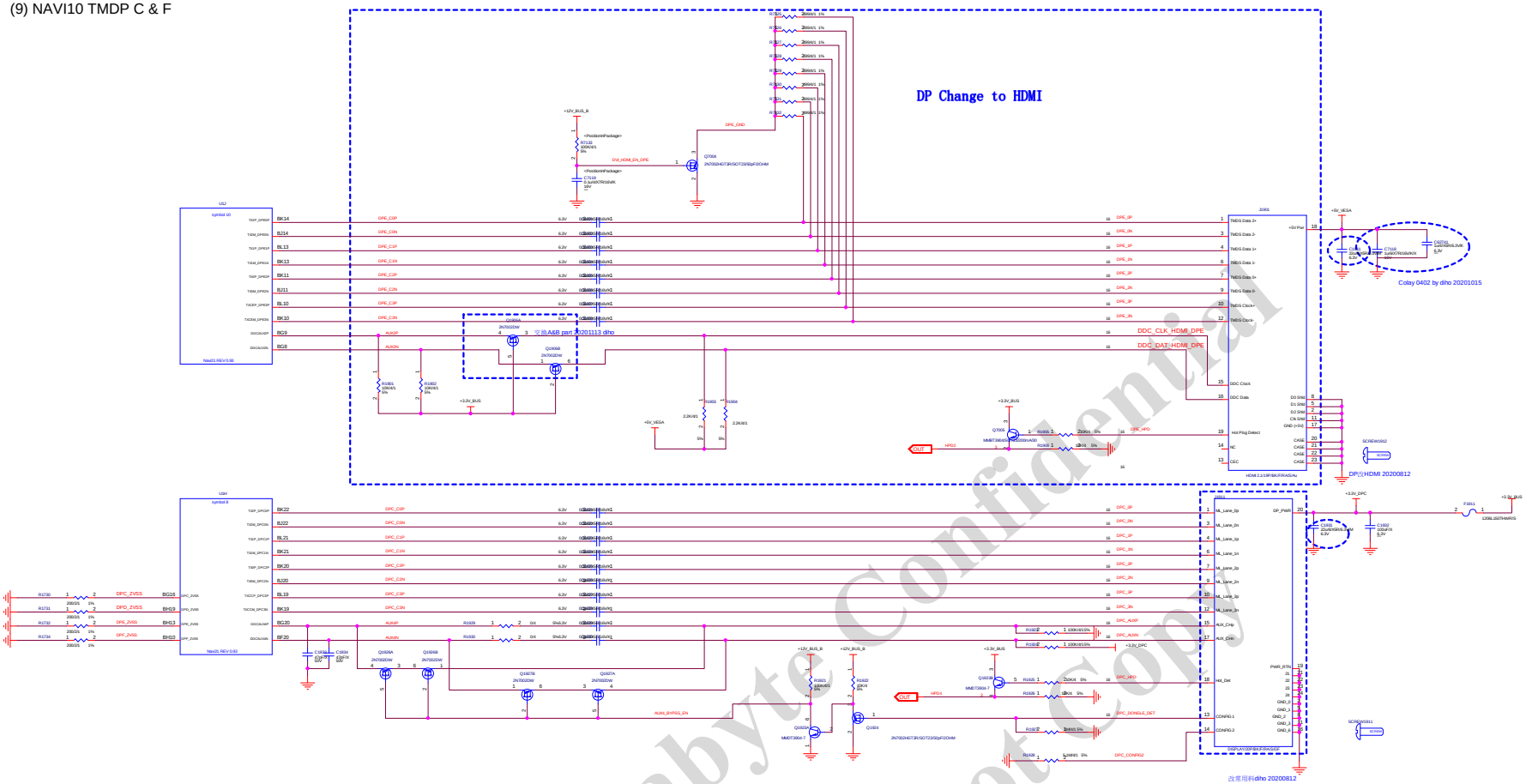
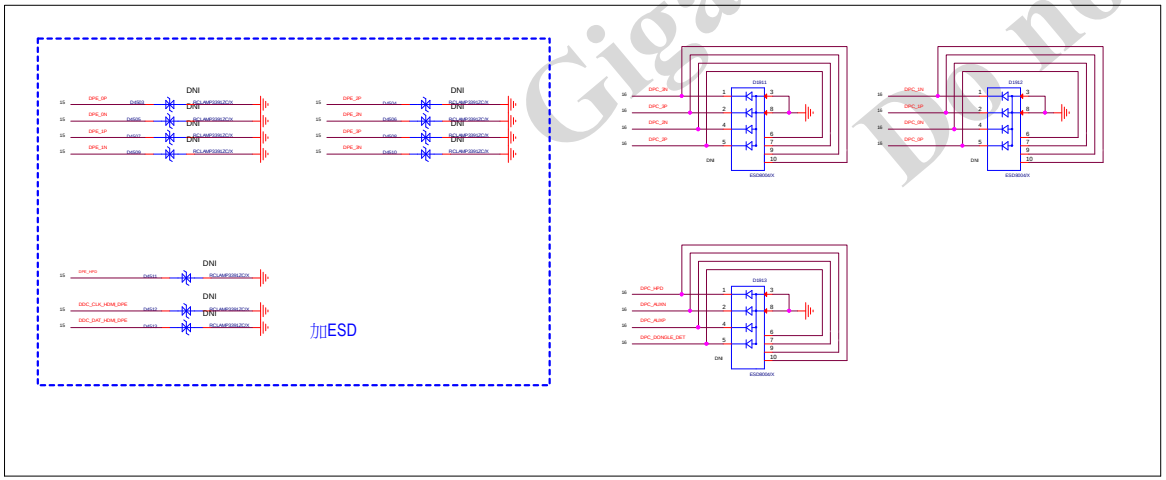
(9) NAVI10 TMDP C & F





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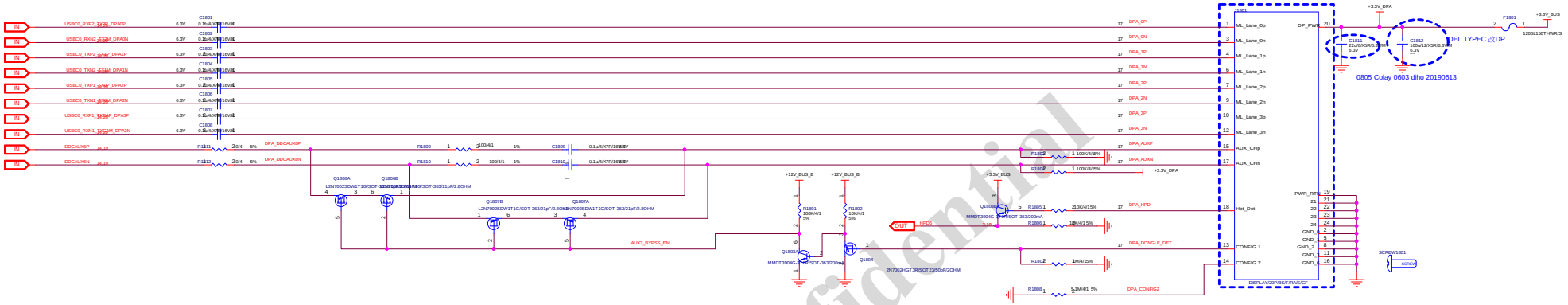

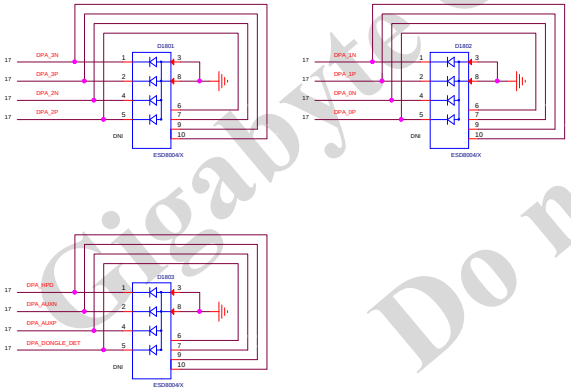

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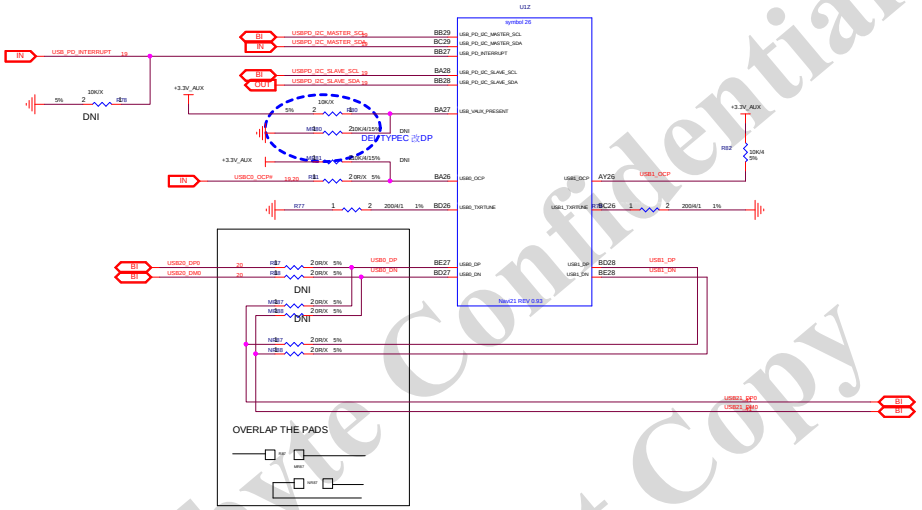

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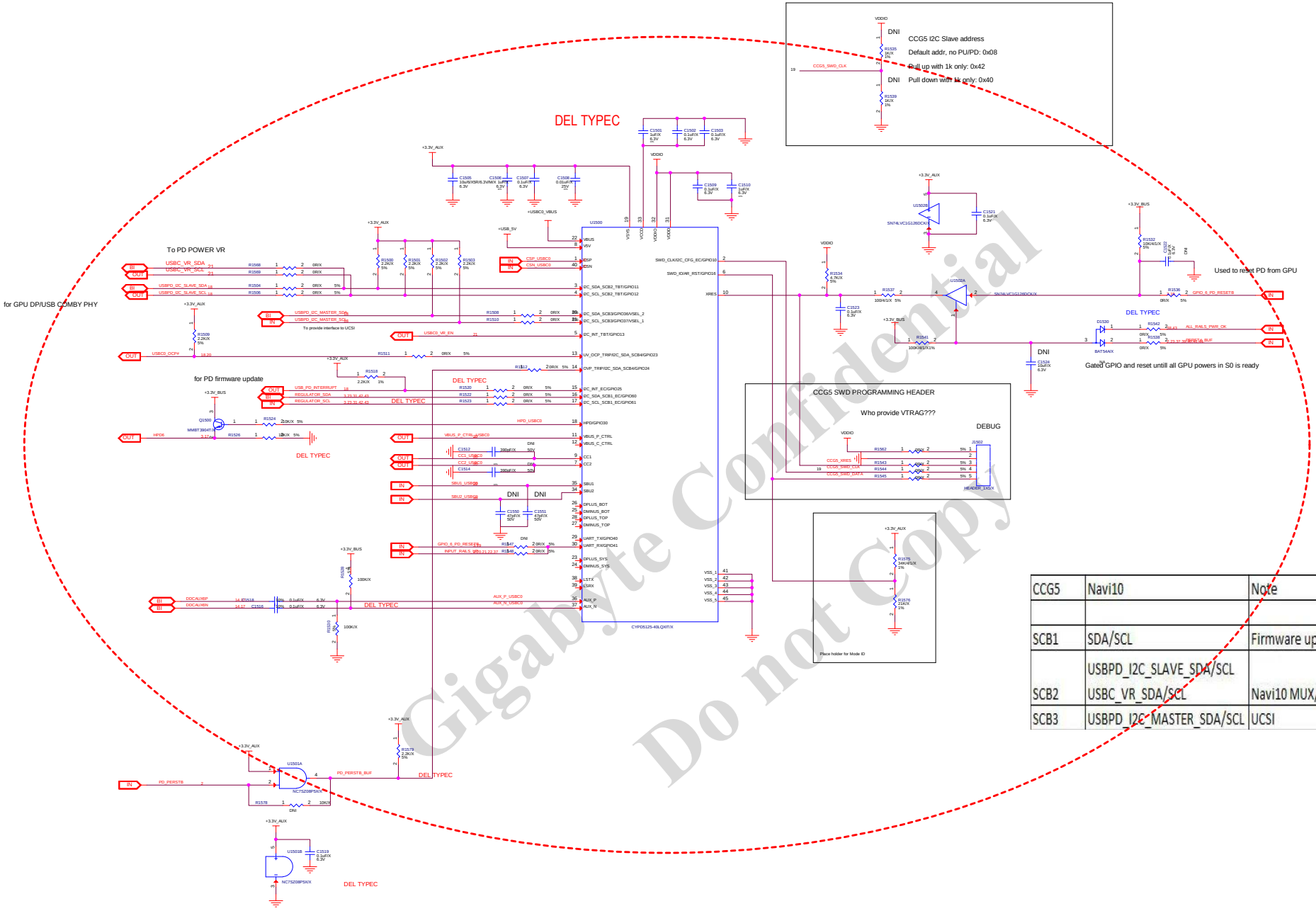

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SCB2	USBPD_I2C_SLAVE_SDA/SCL USBC_VR_SDA/SCL	Navi10 MUX/PD_Regulator/re-driver
SCB3	USBPD_I2C_MASTER_SDA/SCL	UCSI

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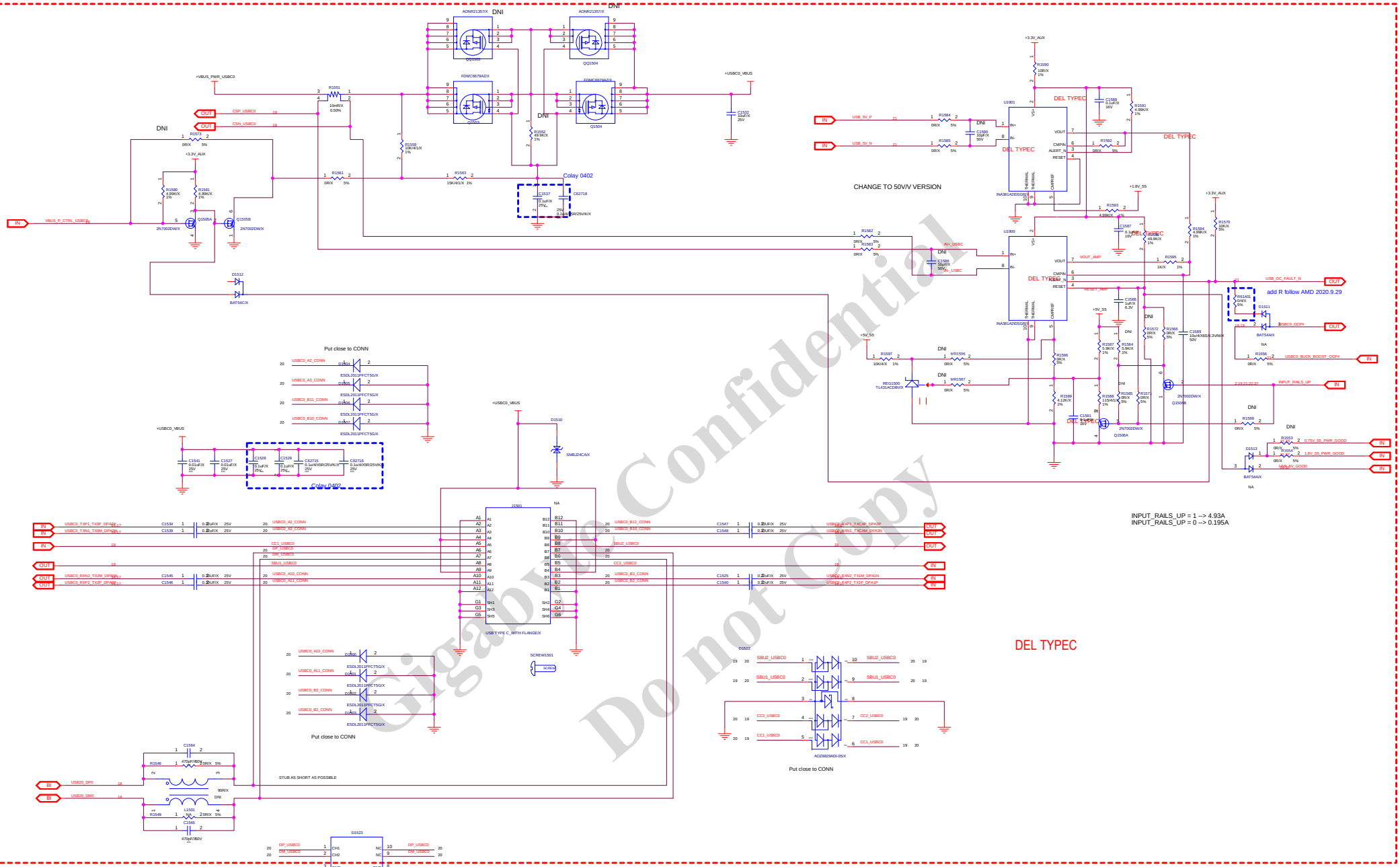

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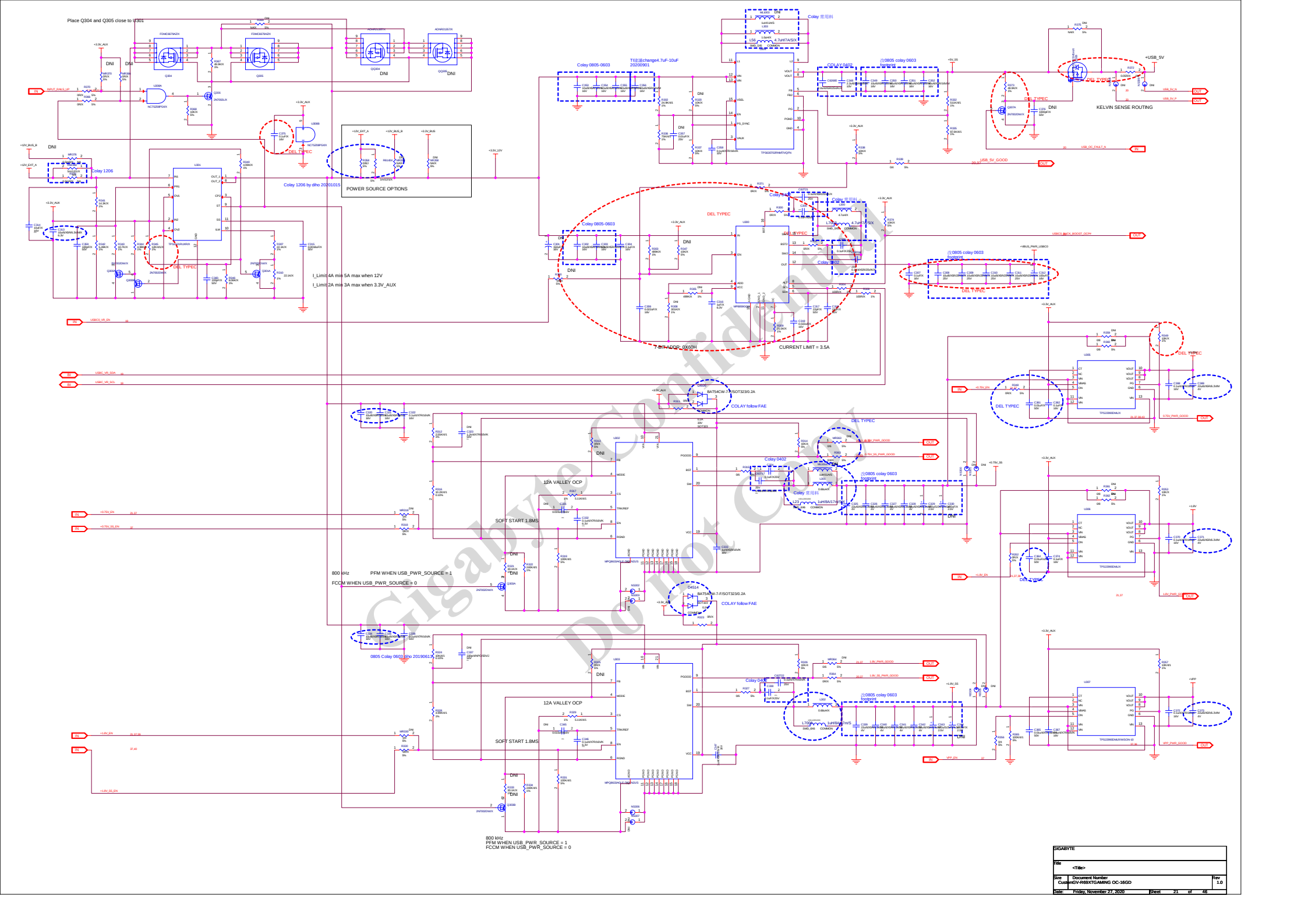

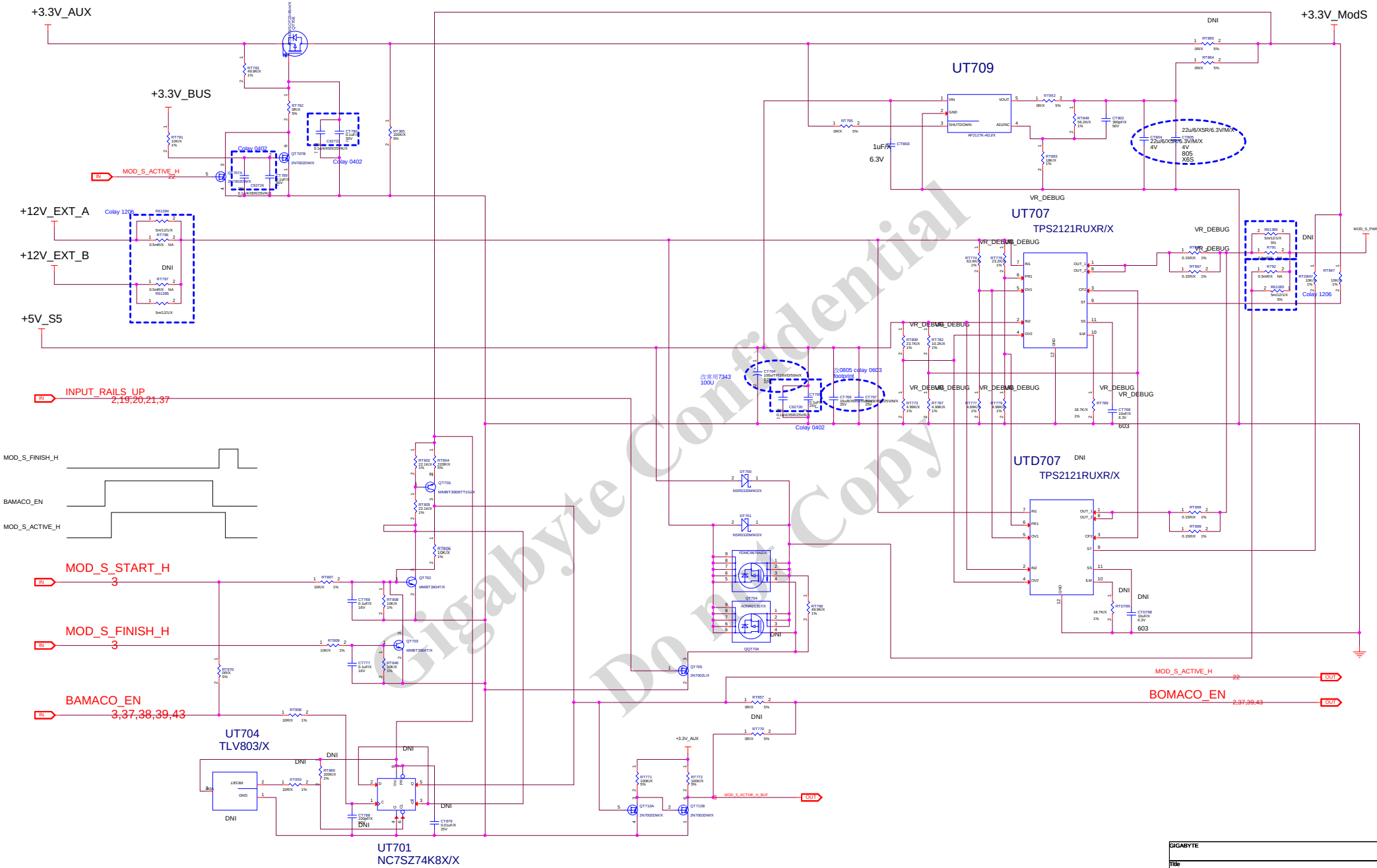

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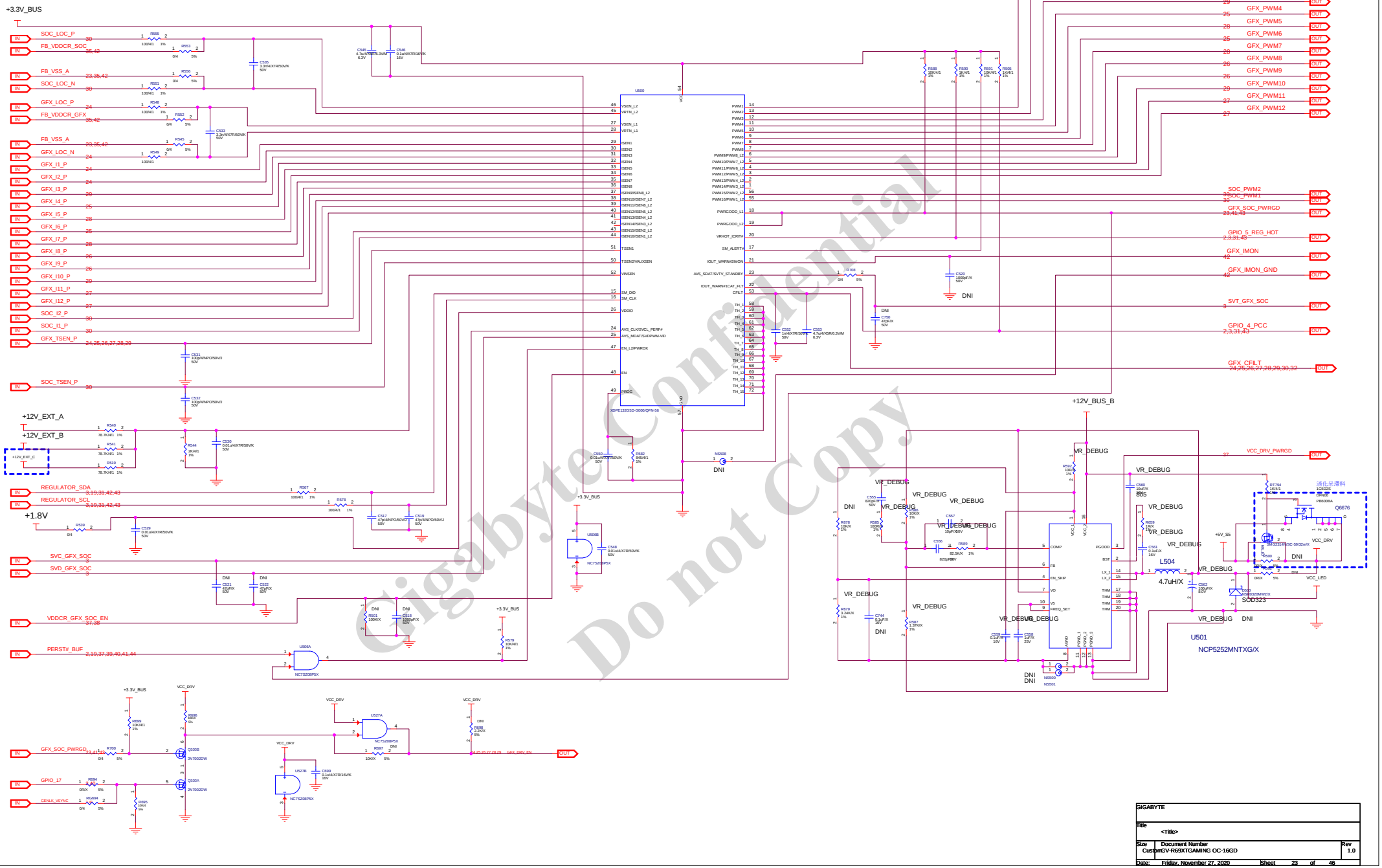
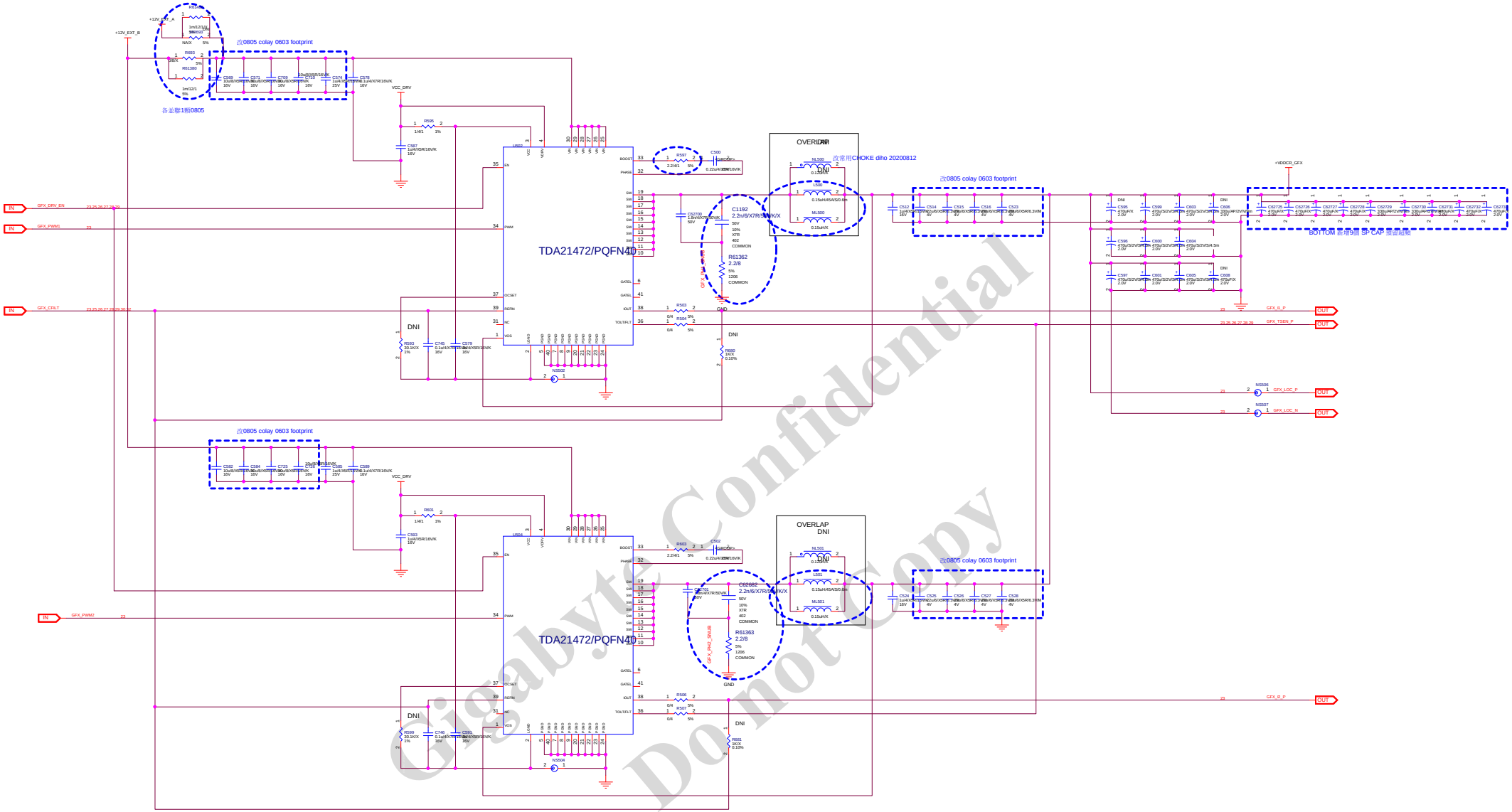
(14) GFX & SOC CONTROLLER





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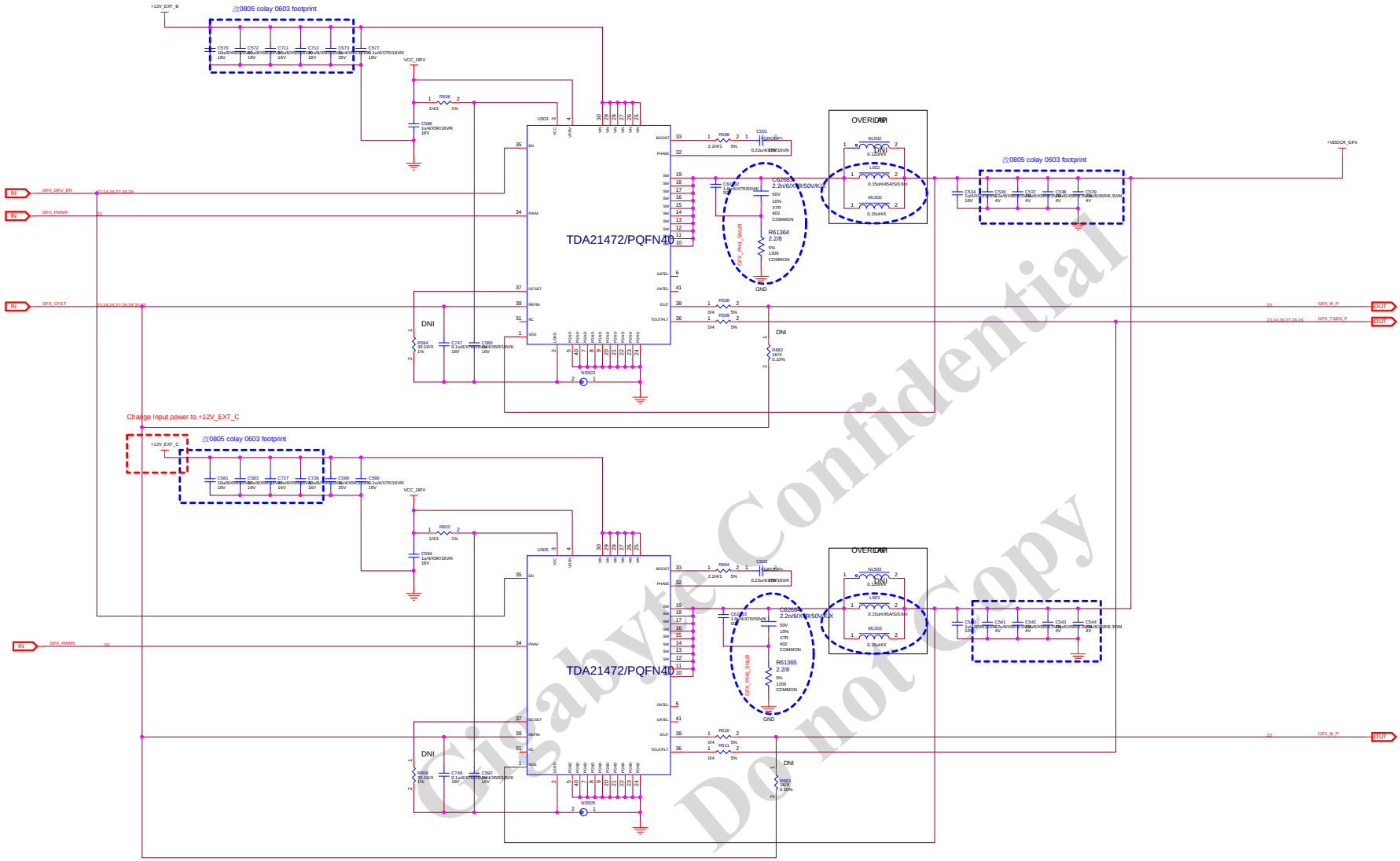

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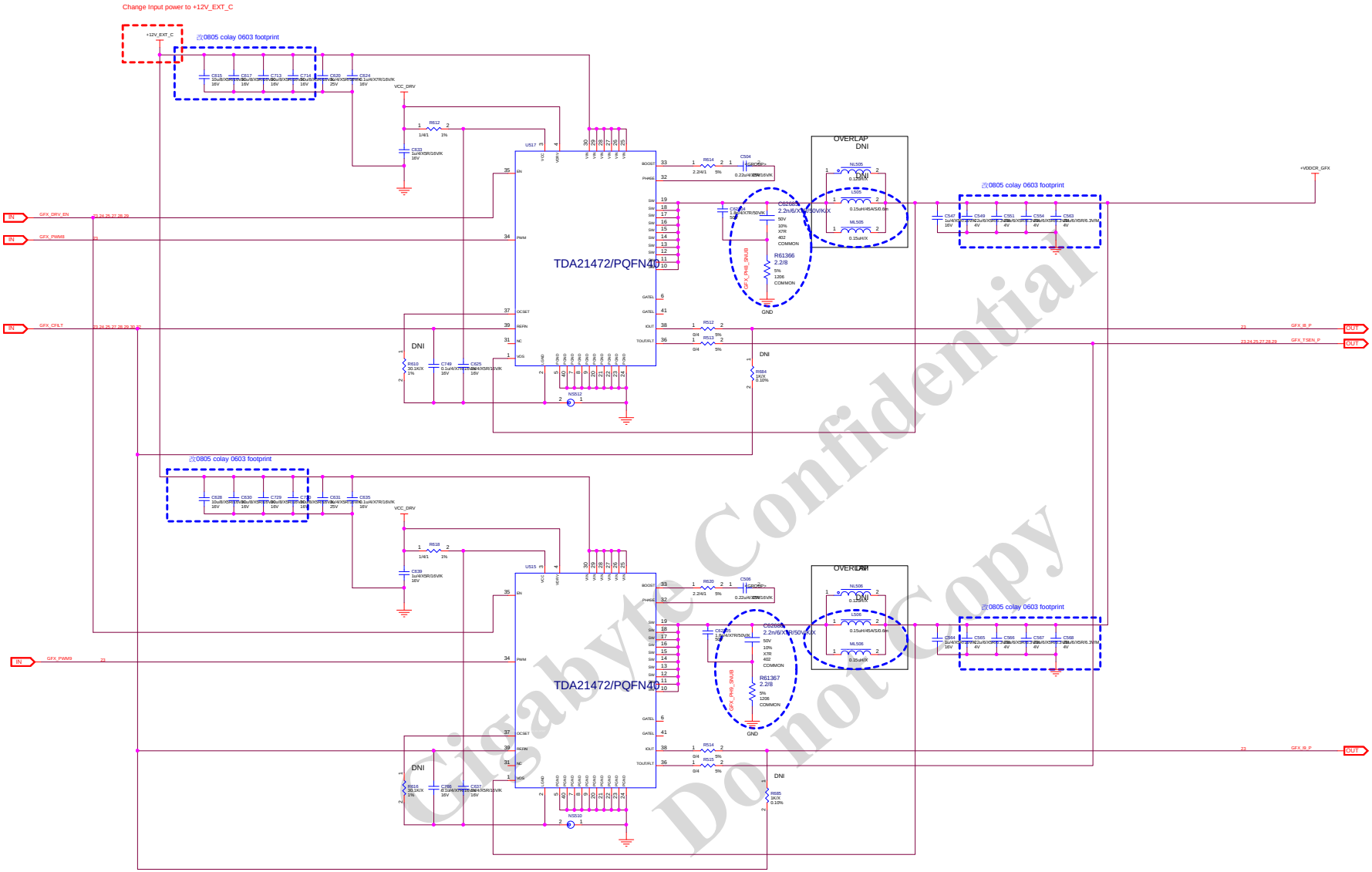

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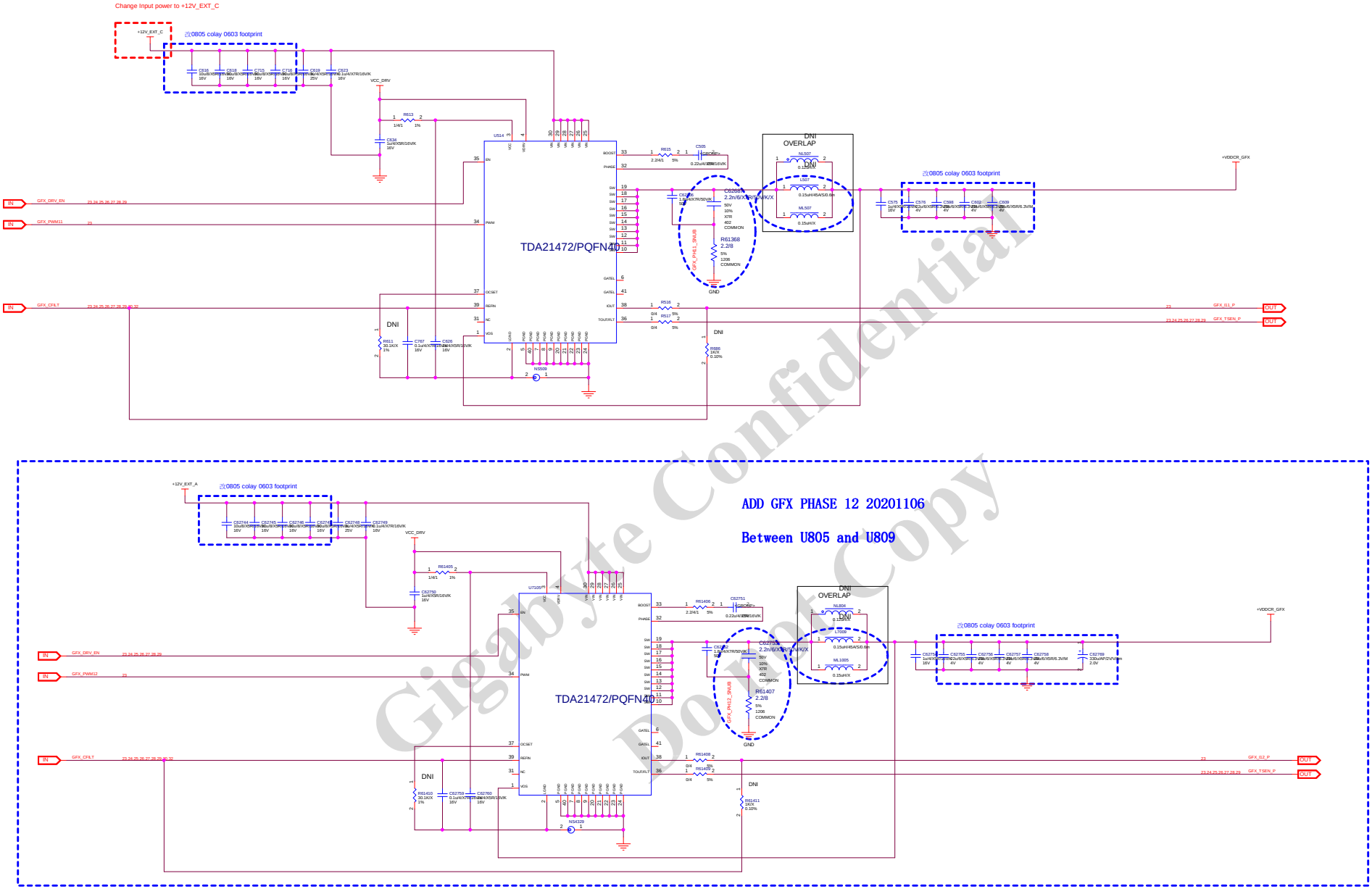

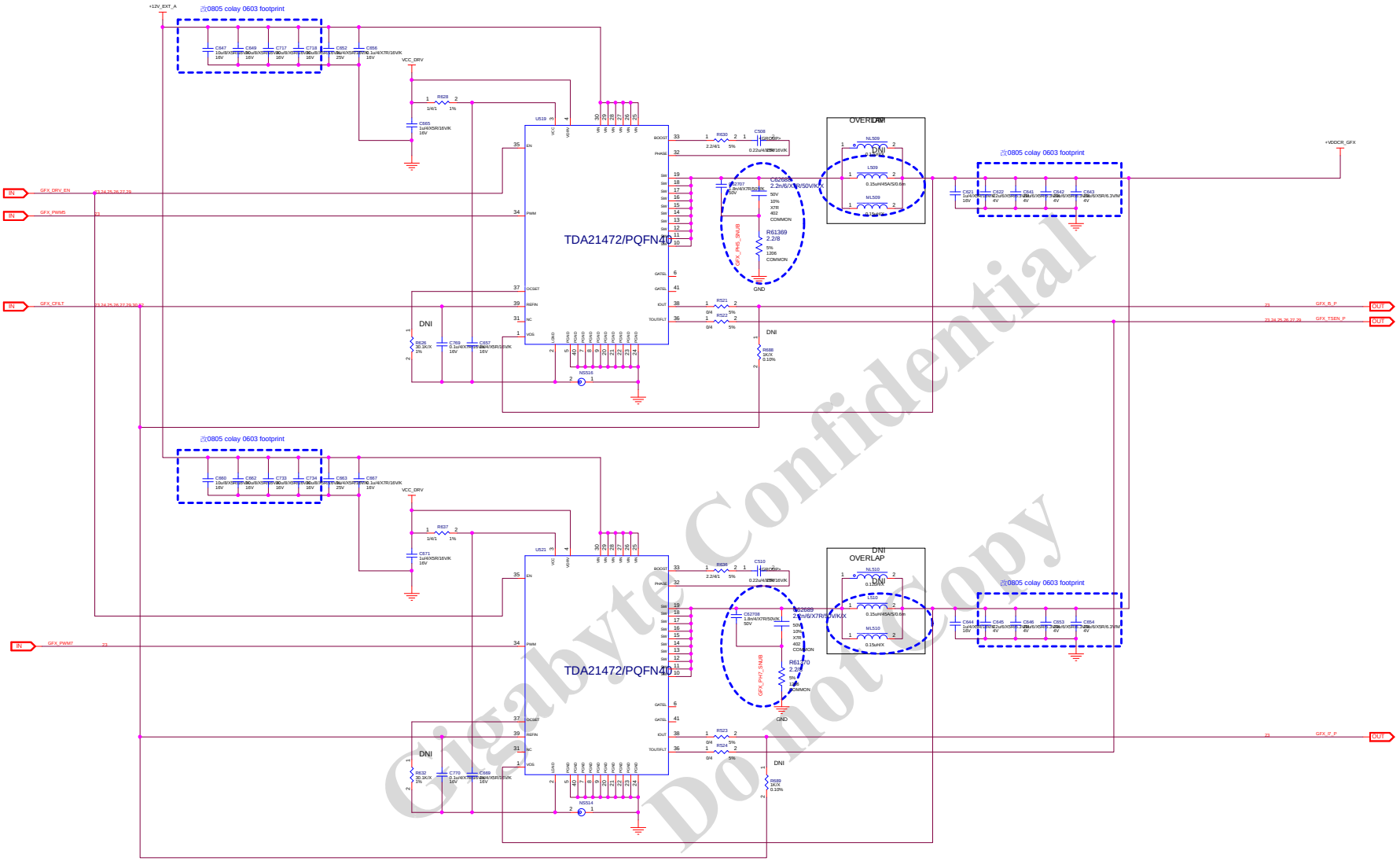

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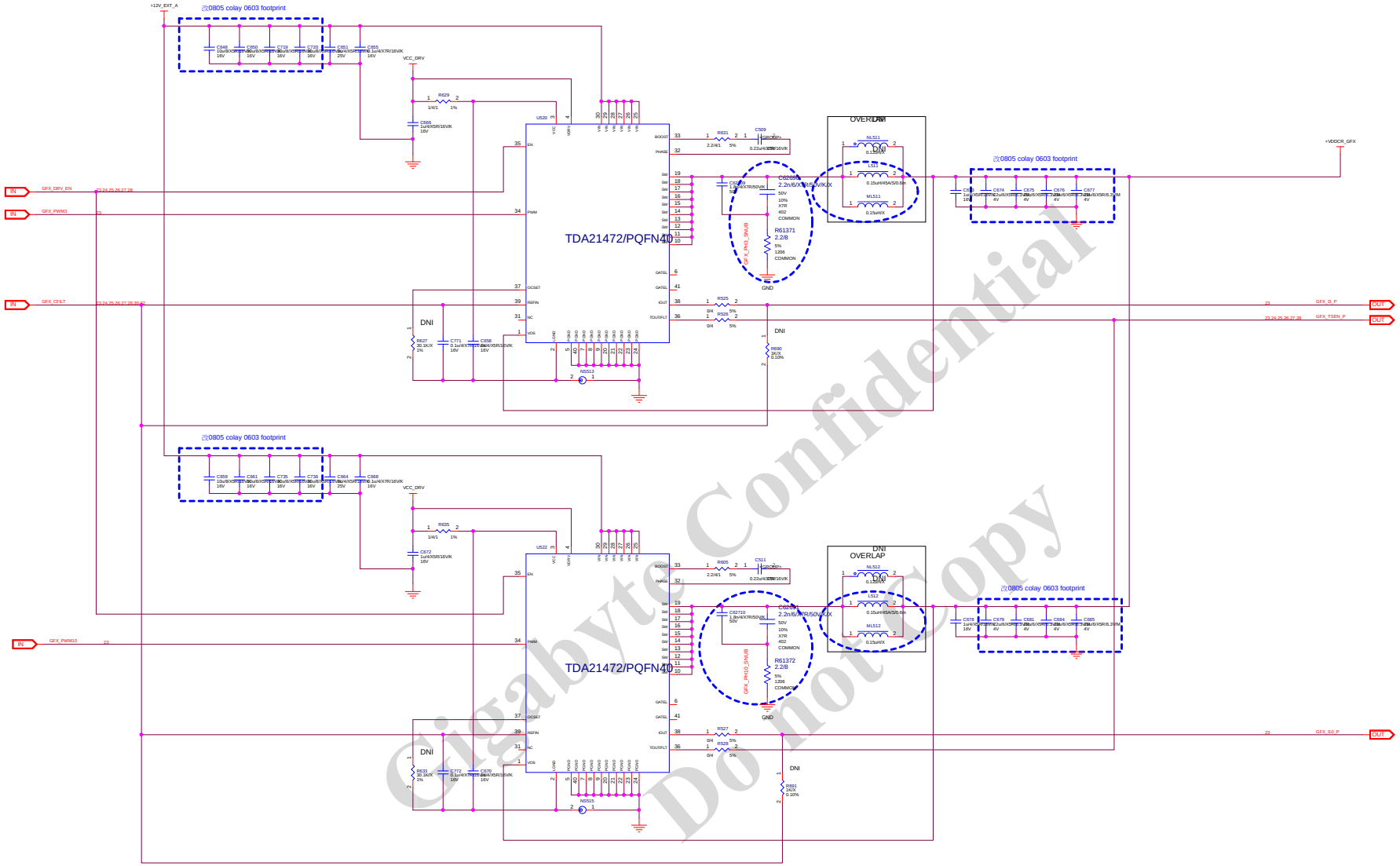

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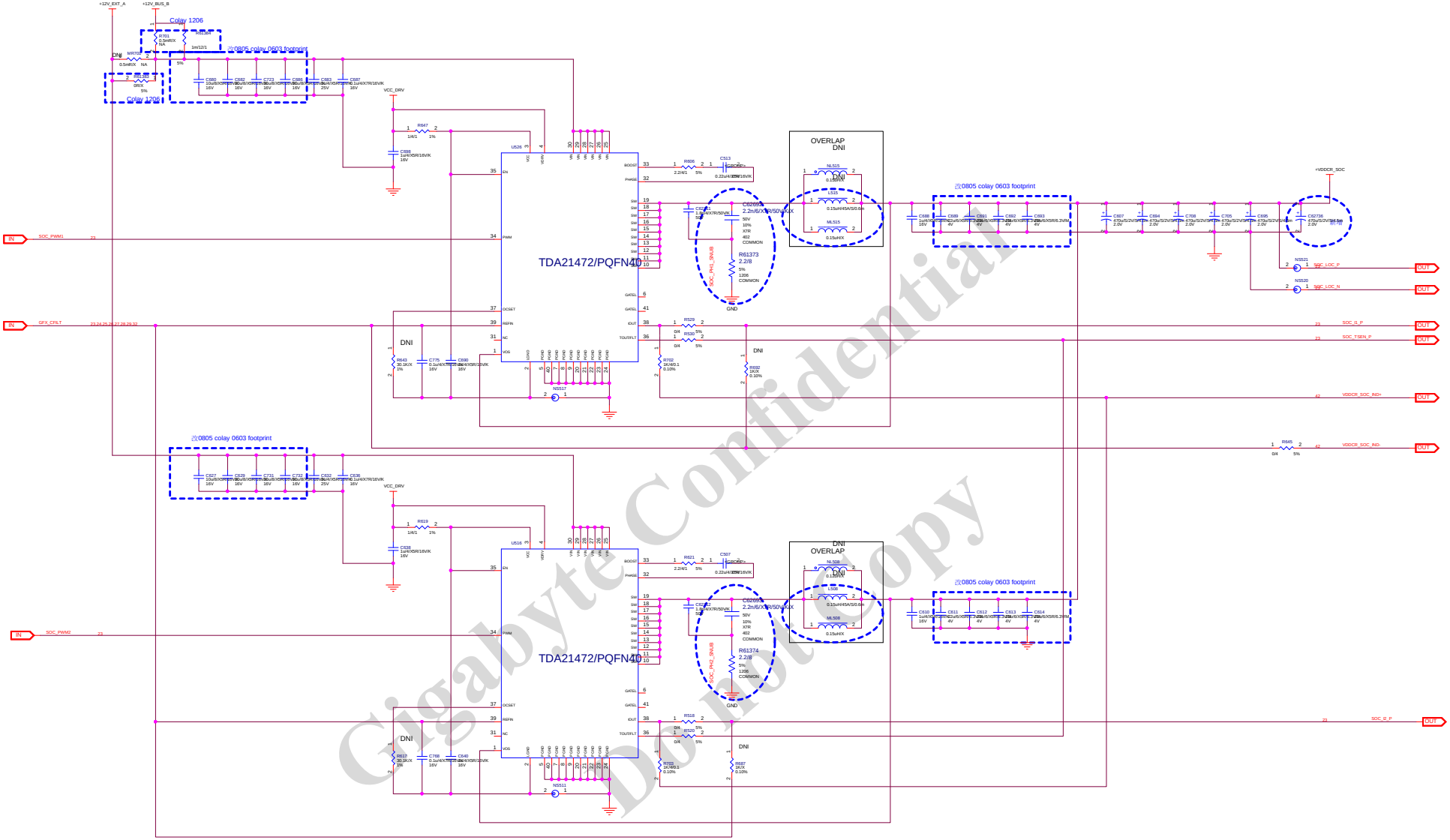

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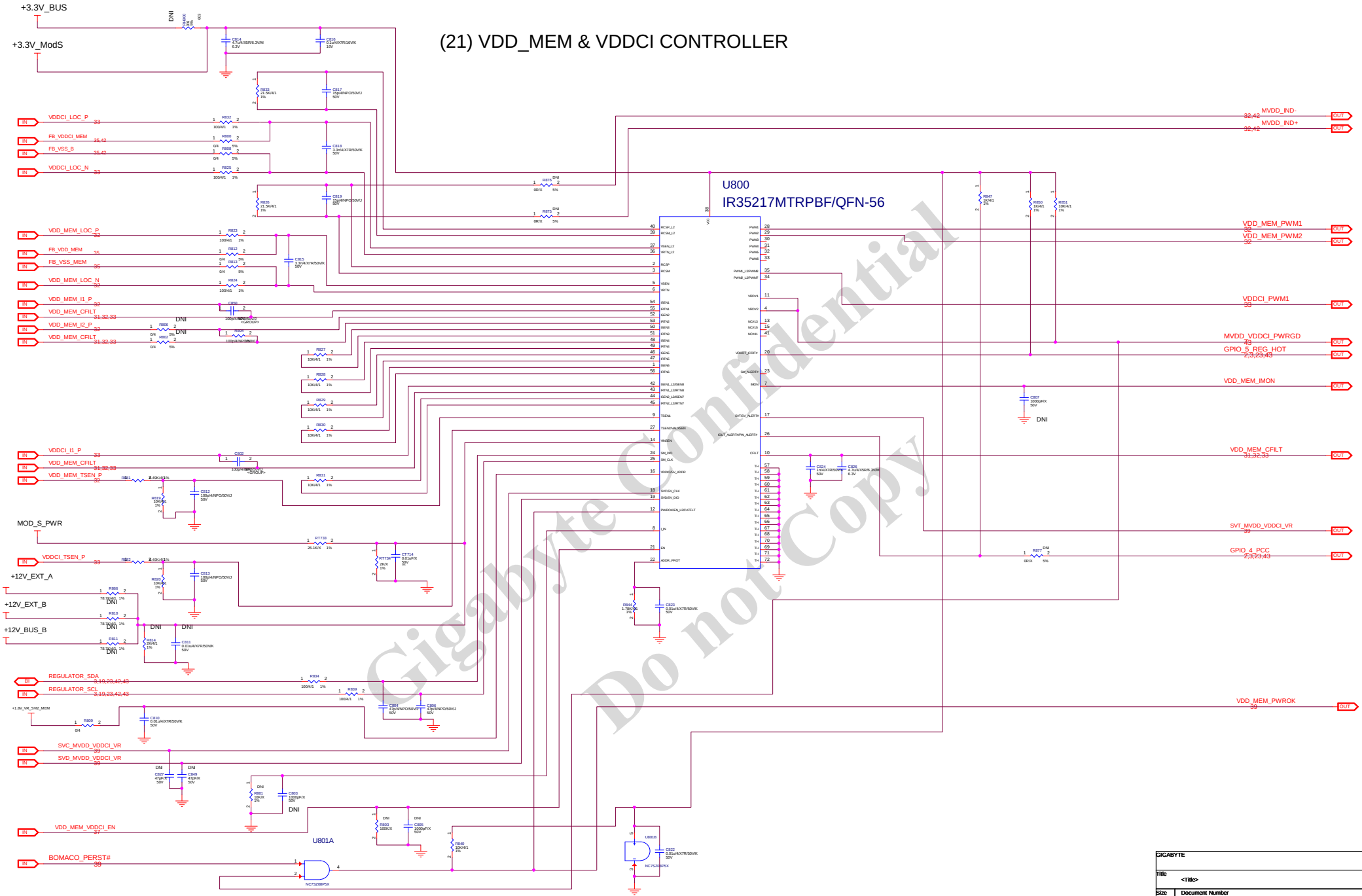
(21) VDD_MEM & VDDCI CONTROLLER



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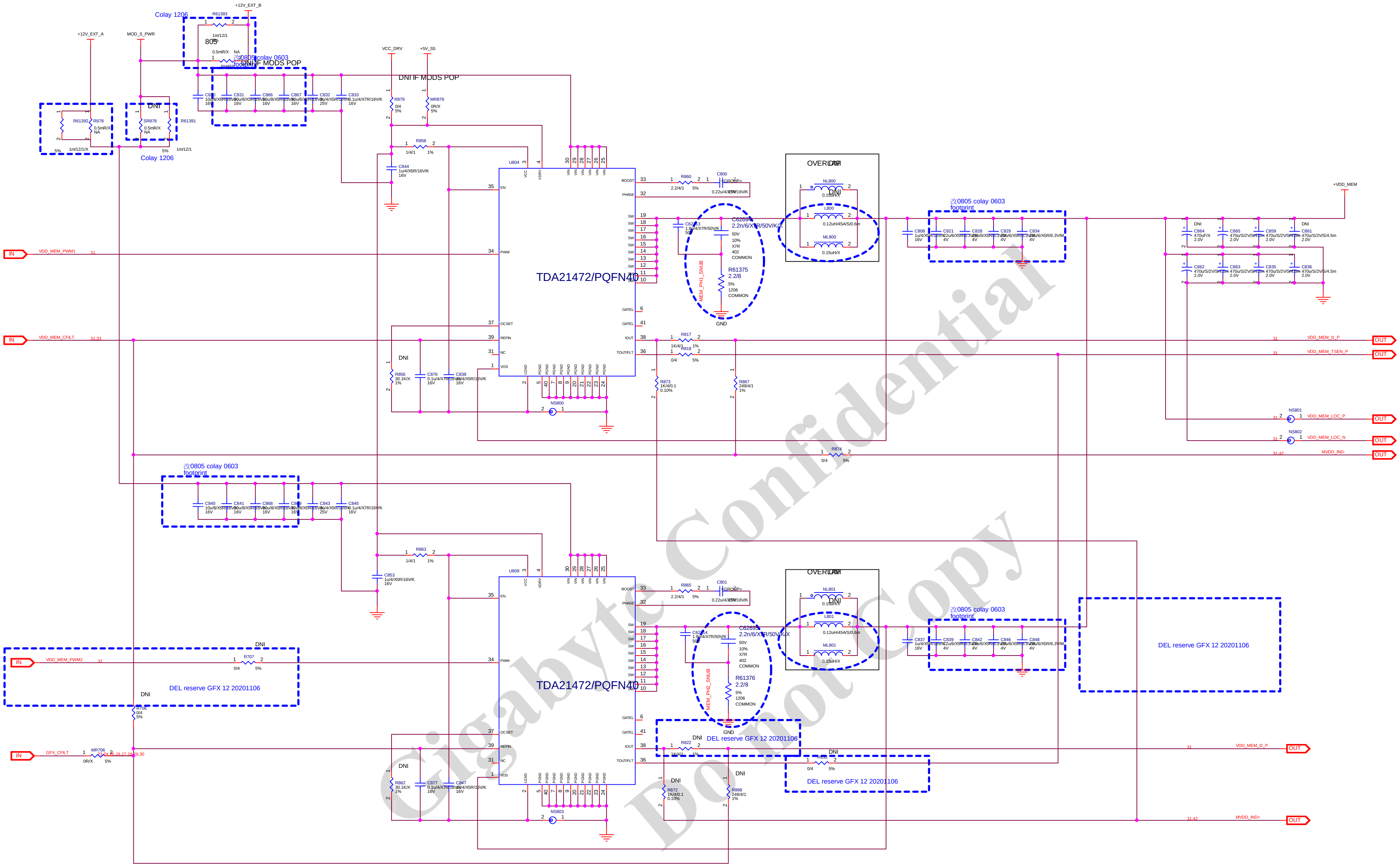

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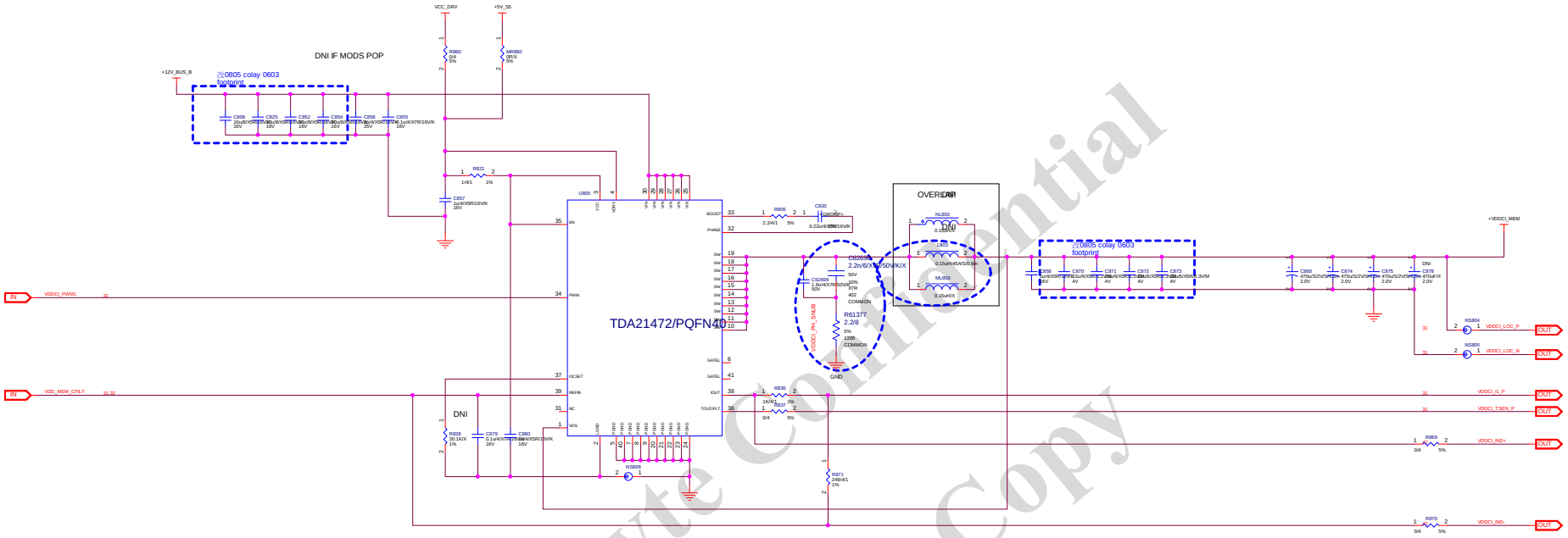

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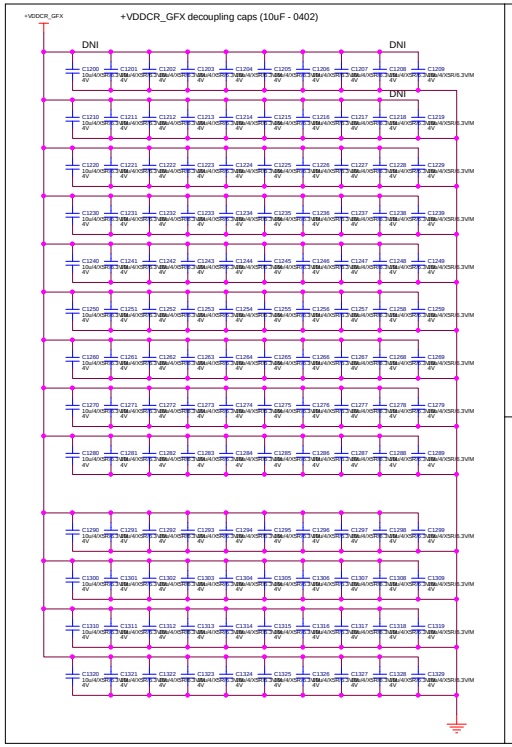
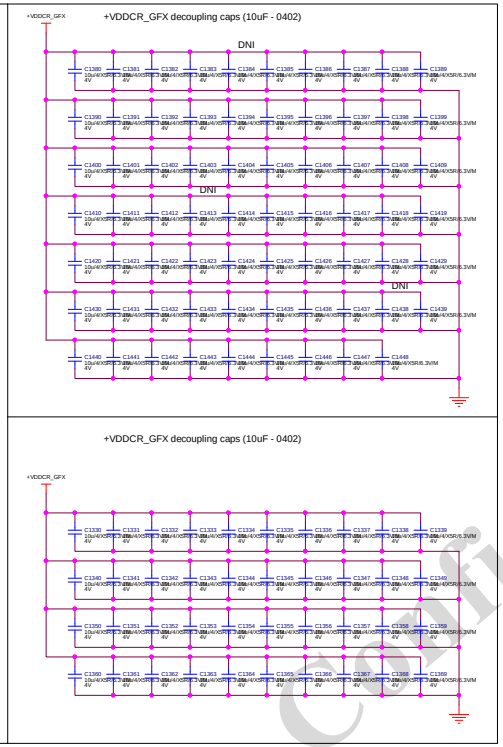
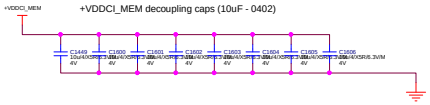
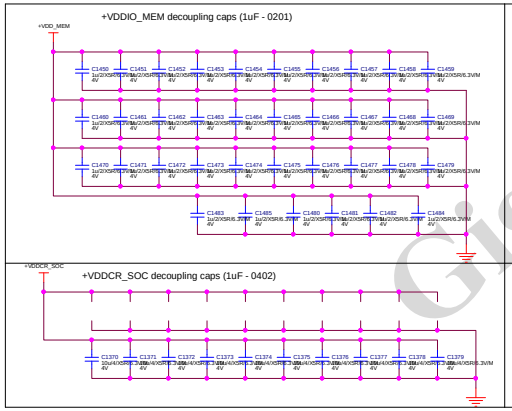


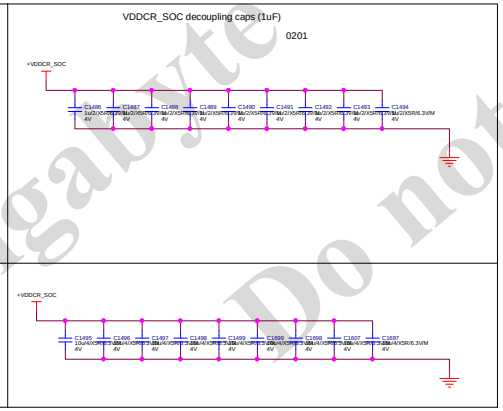


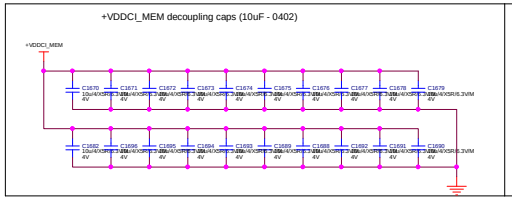


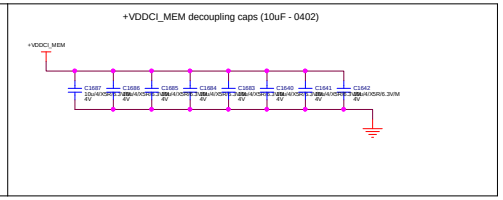
DNI these six caps to match SLT board and keep the design consistent across SKUs

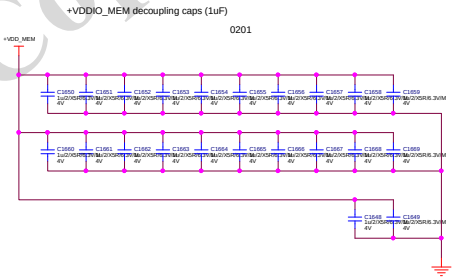
C1218
C1208
C1200
C1438
C1413
C1384











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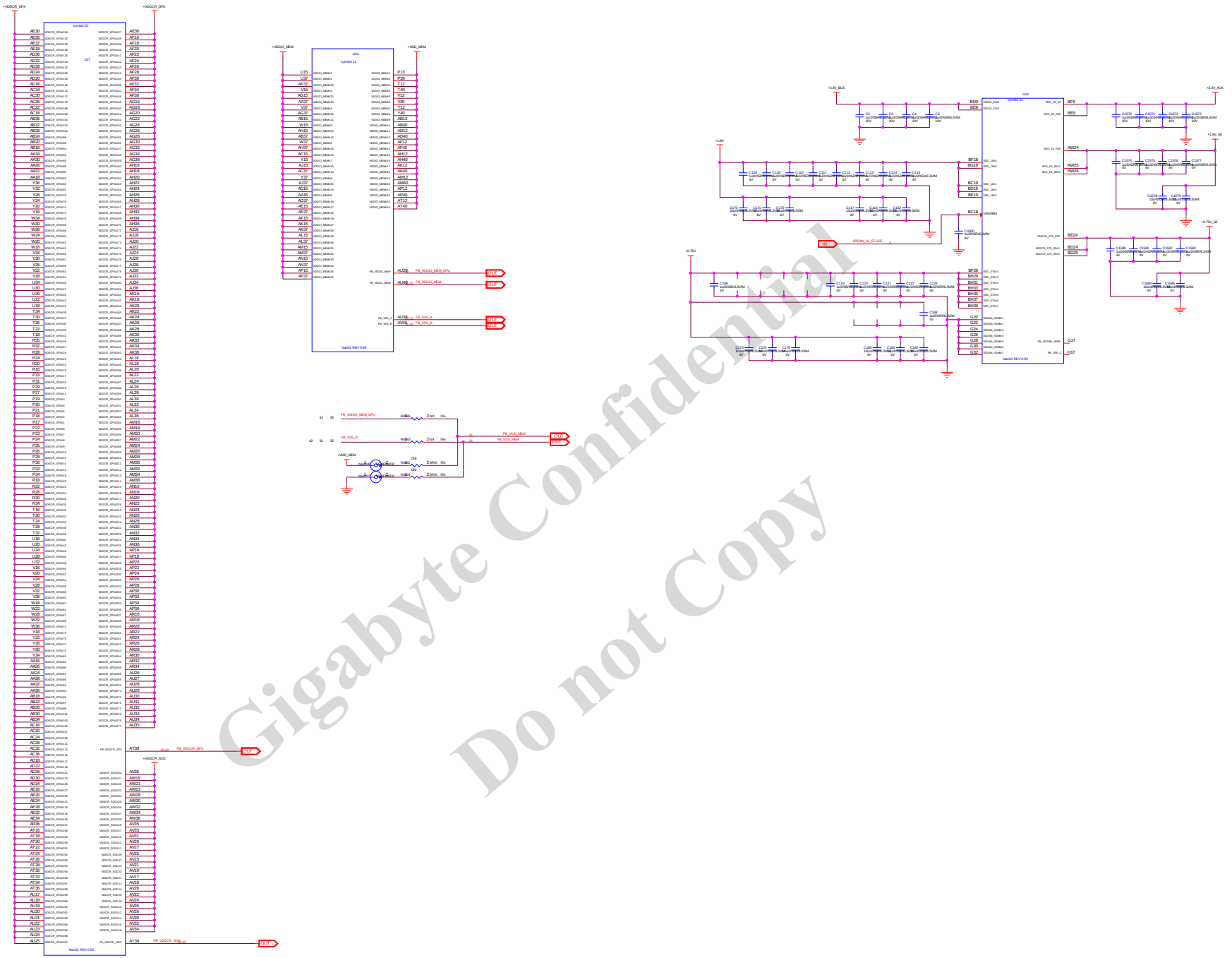

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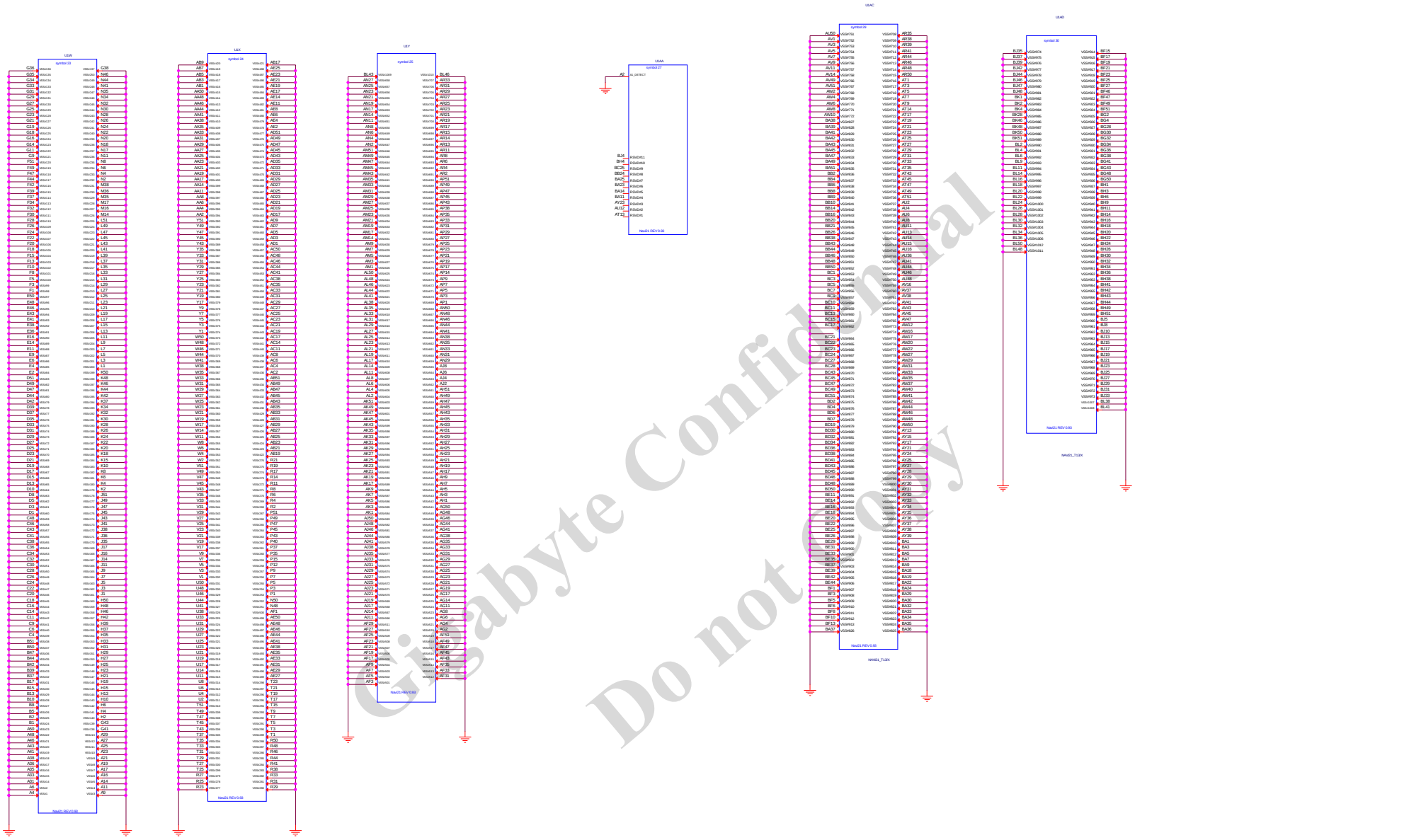

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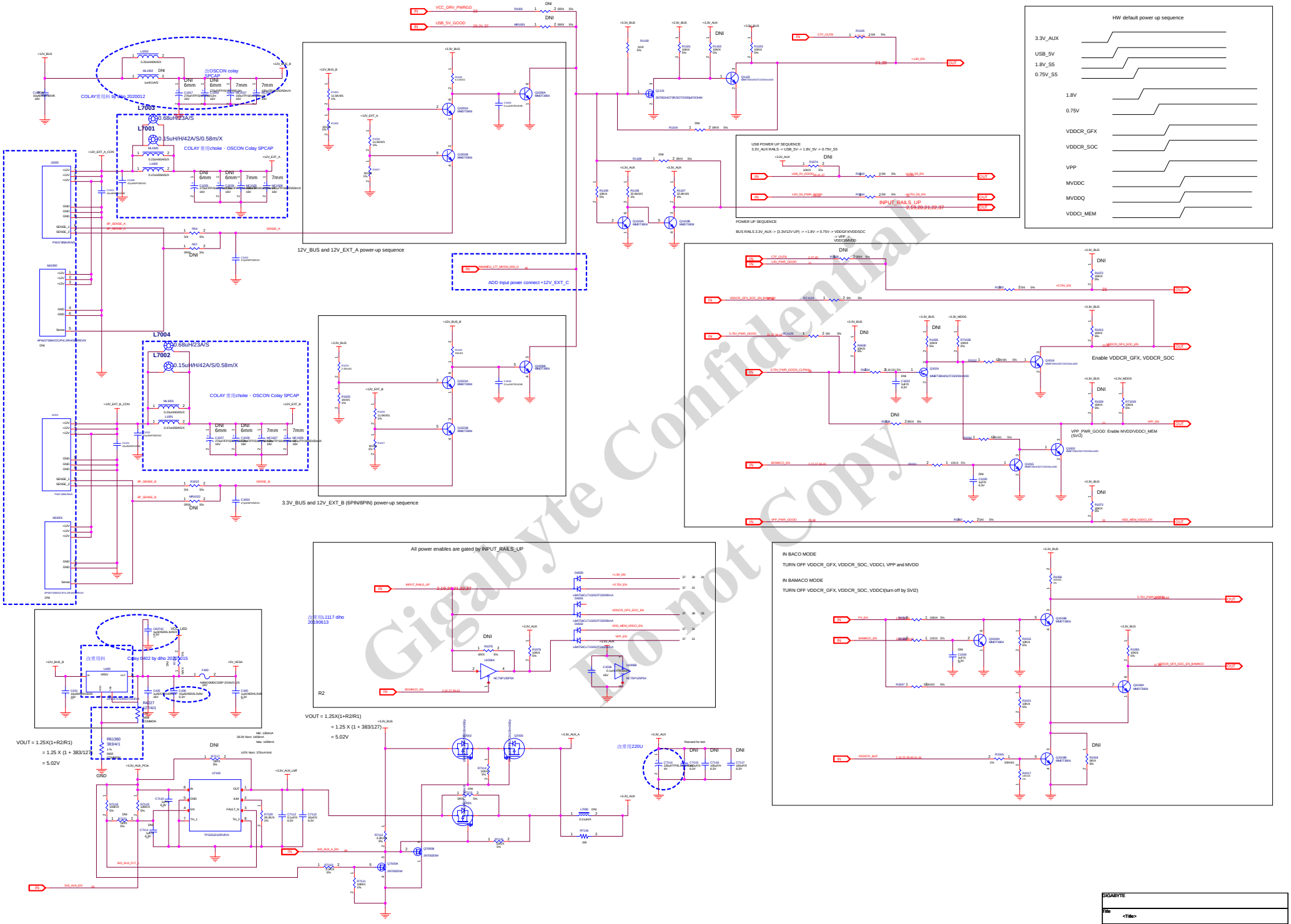
HW default power up sequence
3.3V_AUX
USB_5V
1.8V_S5
0.75V_S5
1.8V
0.75V
VDDCR_GFX
VDDCR_SOC
VPP
MVDDC
MVDDQ
VDDCI_MEM
12V_BUS and 12V_EXT_A power-up sequence
ADD Input power connect +12V_EXT_C
3.3V_BUS and 12V_EXT_B (6PIN/8PIN) power-up sequence
USB POWER UP SEQUENCE
3.3V_AUX RAILS -> USB_5V -> 1.8V_5V -> 0.75V_S5
INPUT_RAILS_UP
2,19,20,21,22,37
POWER UP SEQUENCE
BUS RAILS 3.3V_AUX -> (3.3V/12V UP) -> +1.8V -> 0.75V -> VDDGF/VDDSOC -> VPP -> VDDCI/MVDD
Enable VDDCR_GFX, VDDCR_SOC
VPP_PWR_GOOD: Enable MVDD/VDDCI_MEM (SVI2)
All power enables are gated by INPUT_RAILS_UP
IN BACO MODE
TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI, VPP and MVDD
IN BAMACO MODE
TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI(turn off by SVI2)
L7003
0.68uH/23A/S
L7001
0.15uH/H/42A/S/0.58m/X
L7004
0.68uH/23A/S
L7002
0.15uH/H/42A/S/0.58m/X
COLAY常用choke，OSCON Colay SPCAP
改OSCON colay SPCAP
COLAY常用料 by dho 20200012
改常用料
Colay 0402 by dho 20200715
改常用LL1117 dho 20190613
VOUT = 1.25X(1+R2/R1)
= 1.25 X (1 + 383/127)
= 5.02V
改常用220U
Reserved for test
Gigabyte Confidential
Do not Copy
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GFX/SOC and VPP enable

GFX/SOC EN in BAMACO

CL_DEBUG

CL_DEBUG

INVERTER

INVERTER

AND

OR

OR

AND

AND

Figure 10. 2-input NAND gate with input A inverted or 2-input OR gate with input C inverted

Figure 11. 2-input NOR gate with input B inverted or 2-input AND gate with input C inverted

Figure 12. 2-input OR gate

Figure 13. Inverter

Figure 14. Buffer

Figure 8. 2-input MUX

Figure 9. 2-input AND gate

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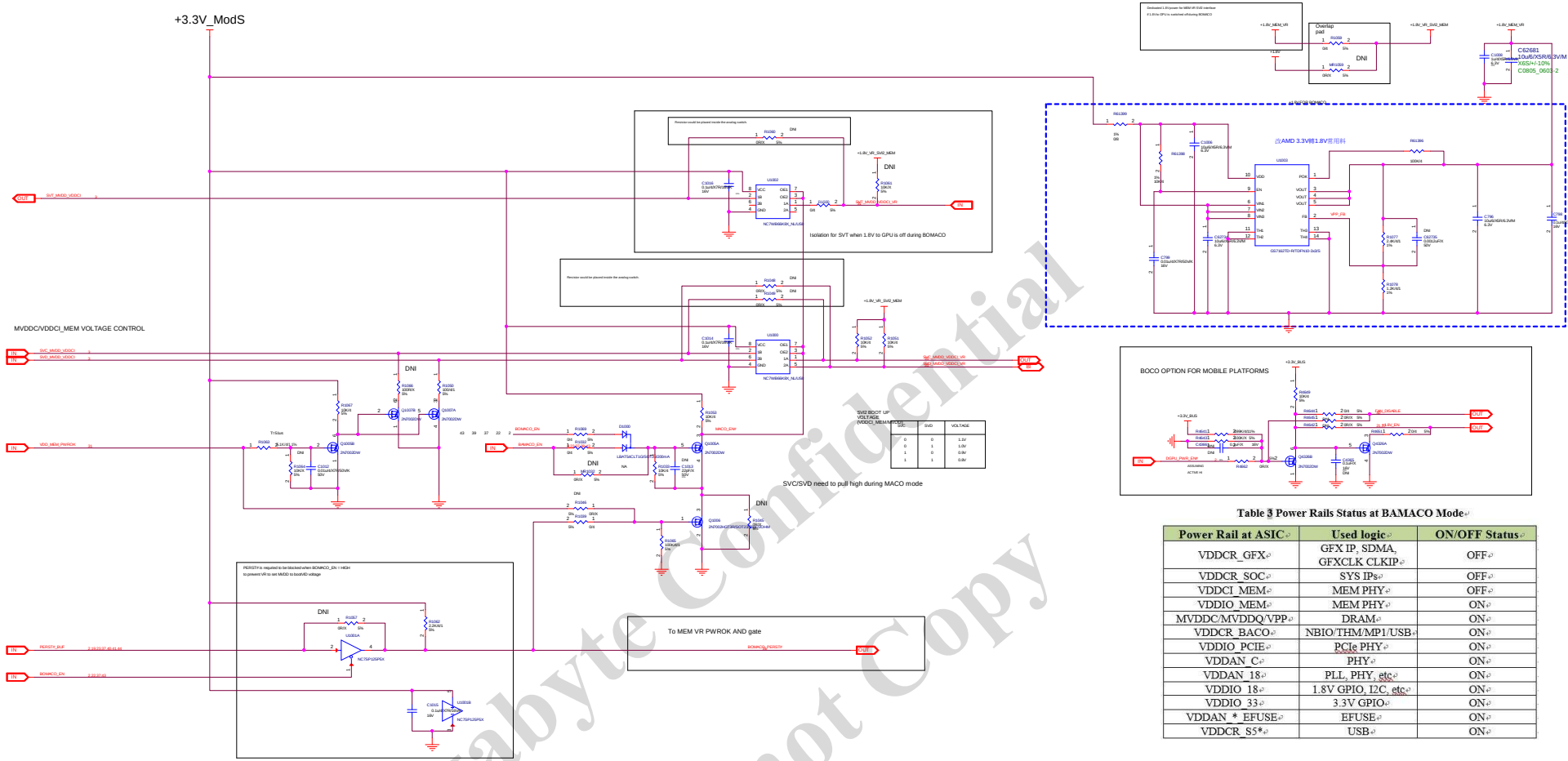

Table 3 Power Rails Status at BAMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	ON
VDDIO_PCIE	PCIe PHY	ON
VDDAN_C	PHY	ON
VDDAN_18	PLL, PHY, etc	ON
VDDIO_18	1.8V GPIO, I2C, etc	ON
VDDIO_33	3.3V GPIO	ON
VDDAN_*_EFUSE	EFUSE	ON
VDDCR_S5*	USB	ON

Table 4 Key Signals at Different PM Modes

Signals	Default	BOCO	BOMACO
PX_EN	LOW	N/A	N/A
MACO_EN	N/A	N/A	N/A
PERSTb	HIGH	1->0->1	1->0->1
PWR_EN	HIGH	LOW	LOW
BOMACO_EN	LOW	LOW	HIGH

Table 5 Platform to Support BOMACO

BOMACO_EN	SVC PU/PD	SVD PU/PD
HIGH	PU	PU
LOW	bootVID	bootVID

Table 3 Power Rails Status at BOMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status for BOMACO-A
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	OFF
VDDIO_PCIE	PCIe PHY	OFF
VDDAN_C	PHY	OFF
VDDAN_18	PLL, PHY, etc	OFF
VDDIO_18	1.8V GPIO, I2C, etc	OFF
VDDIO_33	3.3V GPIO	OFF
VDDAN_*_EFUSE	EFUSE	OFF
VDDCR_S5*	USB	ON

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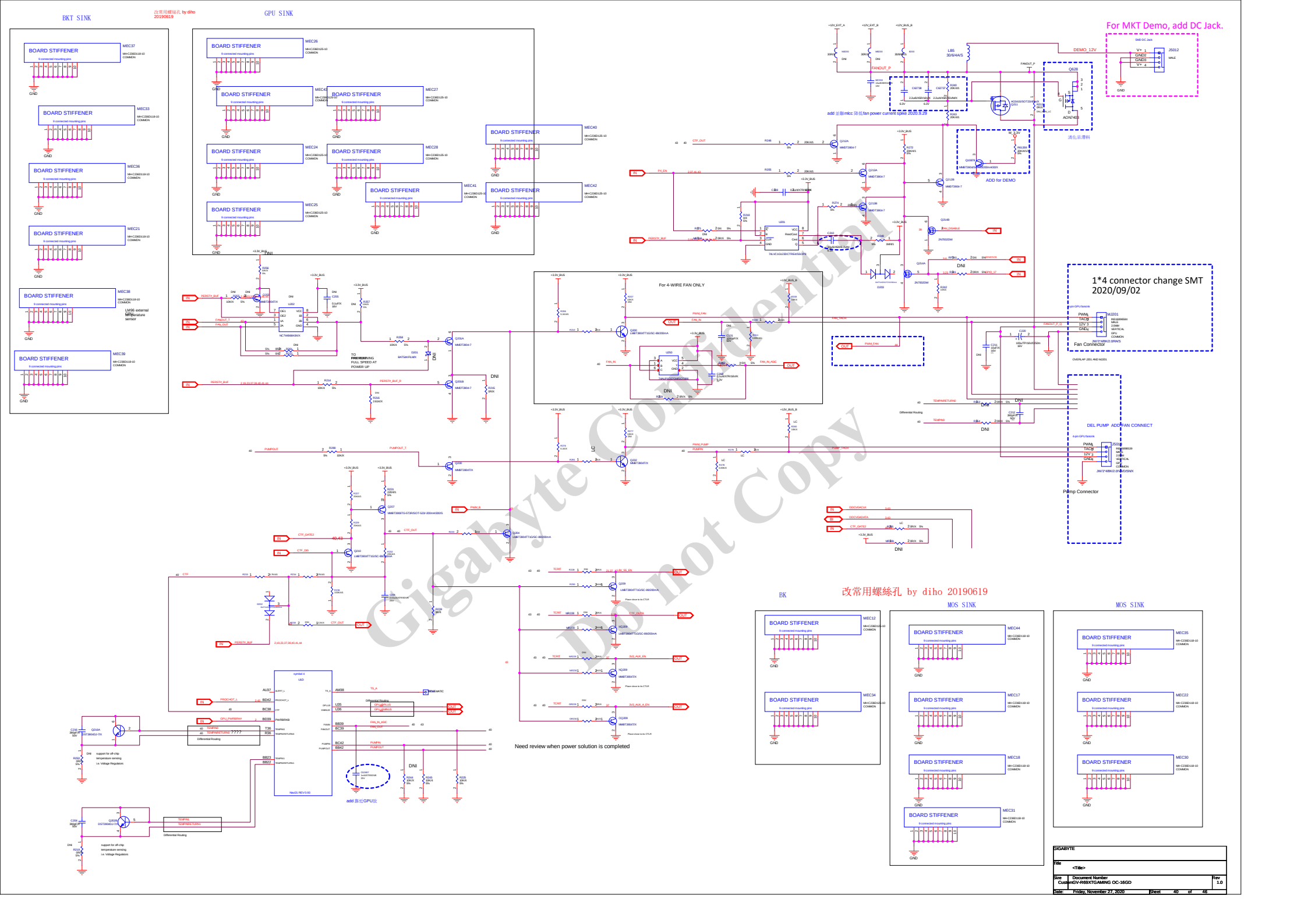
BKT SINK
改常用螺絲孔 by diho
20190619
GPU SINK
For MKT Demo, add DC Jack.
add 並聯mlcc 降低fan power current spike 2020.9.25
add for DEMO
液化吳澤料
For 4-WIRE FAN ONLY
1*4 connector change SMT
2020/09/02
Fan Connector
DEL PUMP ADD FAN CONNECT
Pump Connector
TO PREVENT RUNNING FULL SPEED AT POWER UP
add 並聯GPU吹
Need review when power solution is completed
BK
改常用螺絲孔 by diho 20190619
MOS SINK
MOS SINK
Gigabyte Confidential
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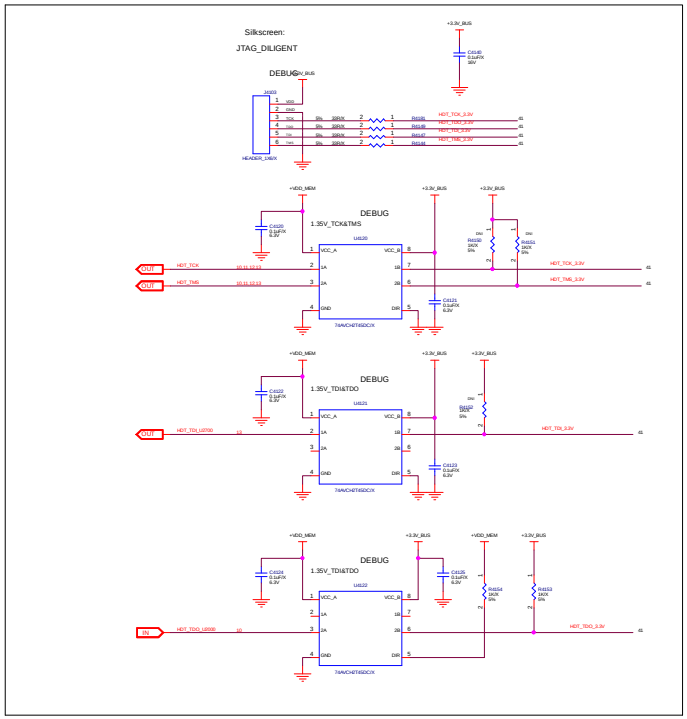

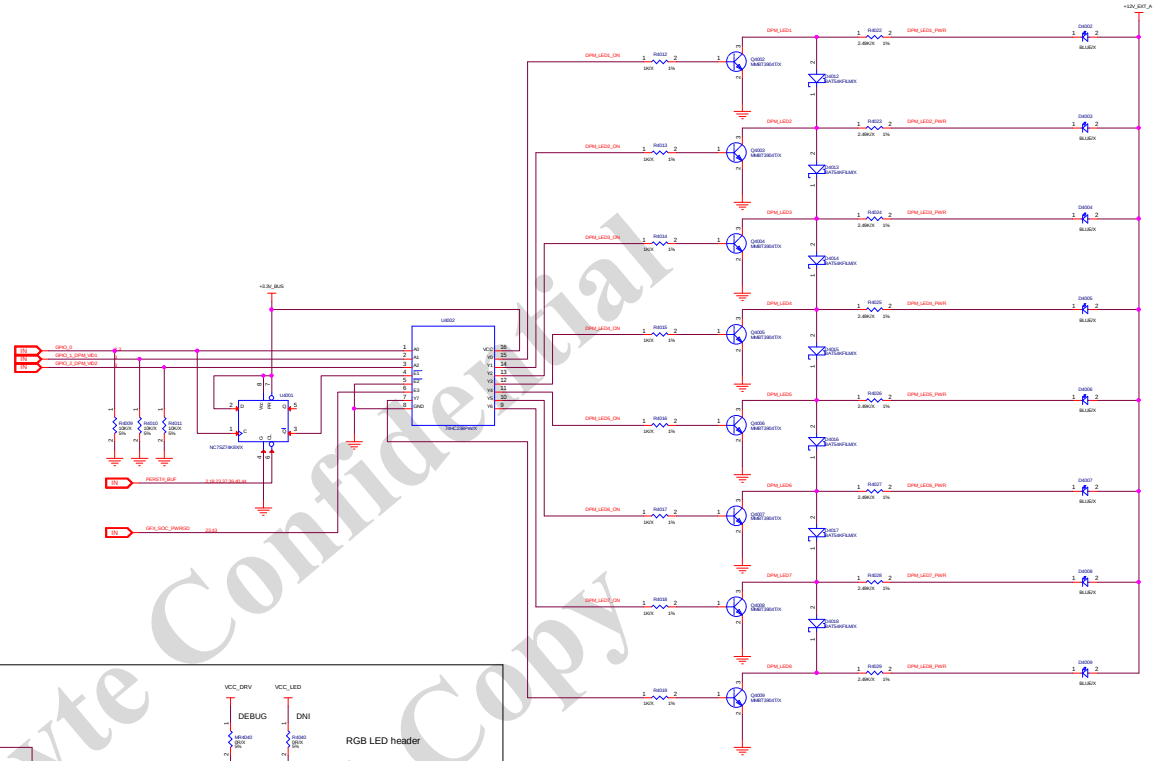

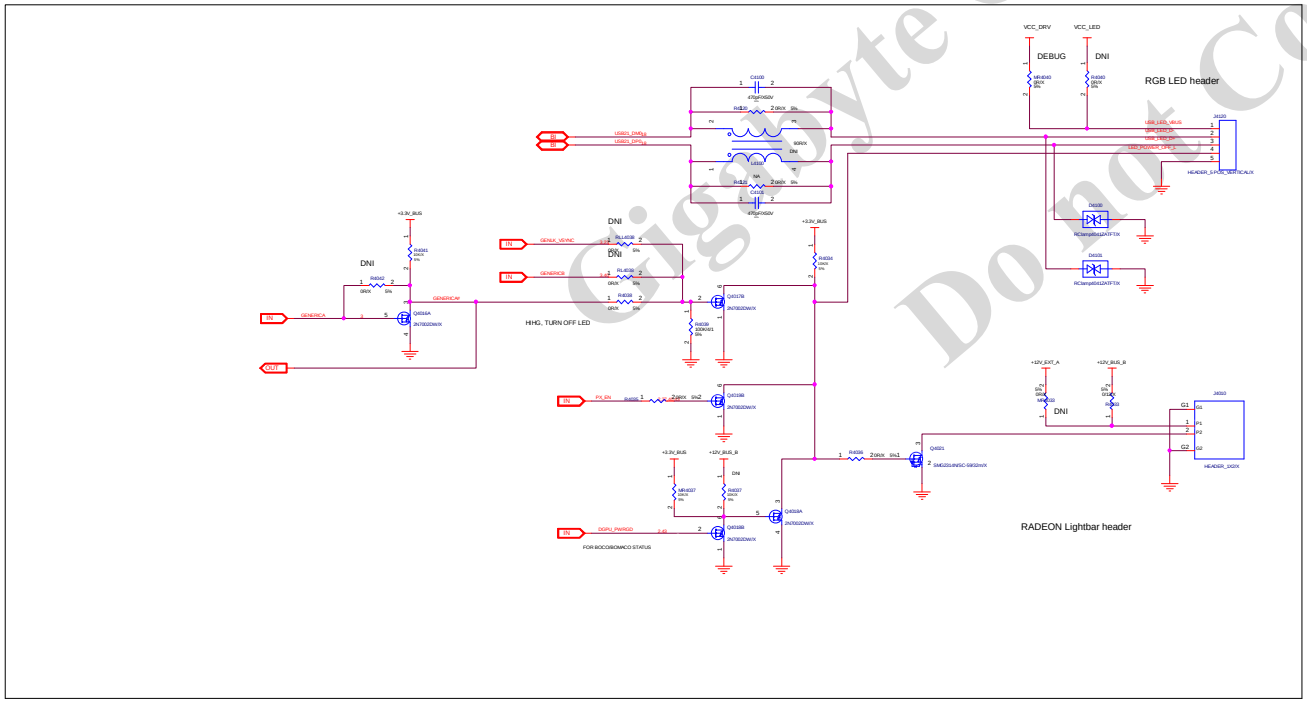

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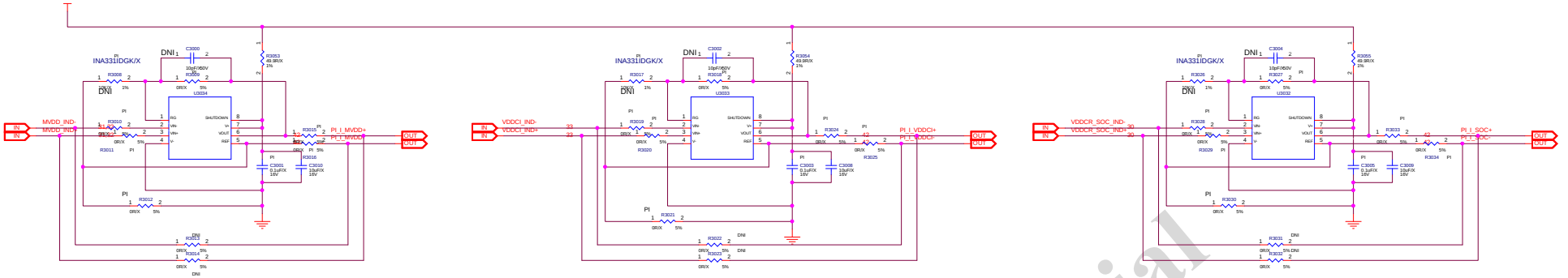
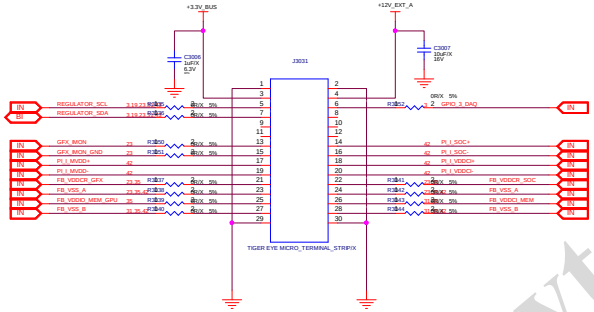
+3.3V_ModS



FOR PI DAUGHTER CARD



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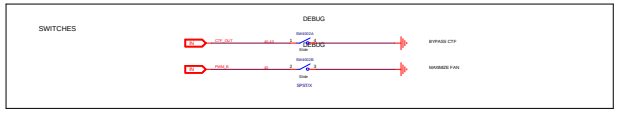
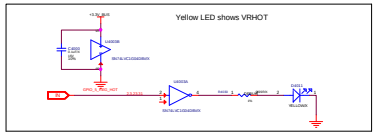
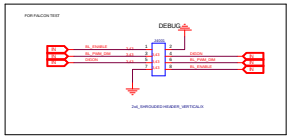
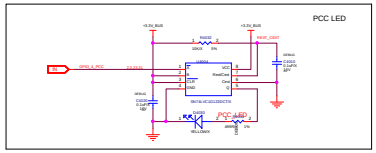
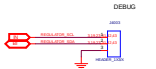
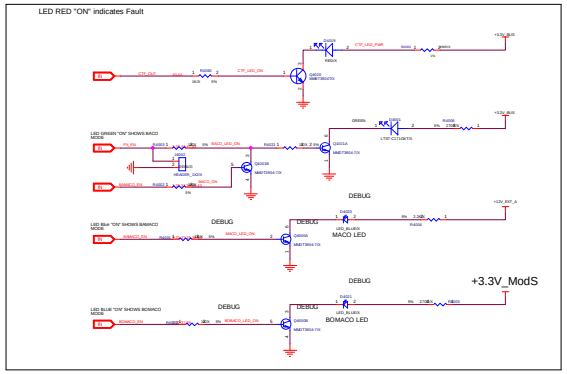


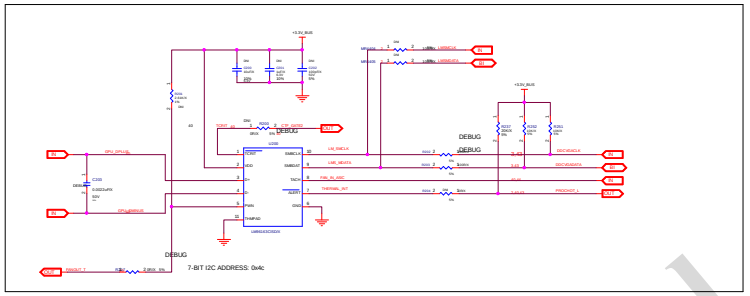


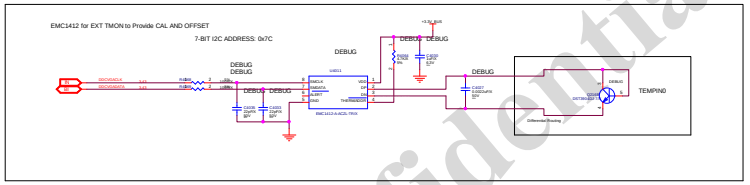


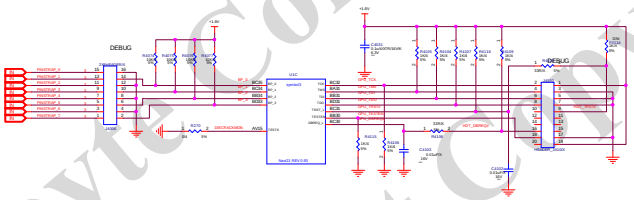












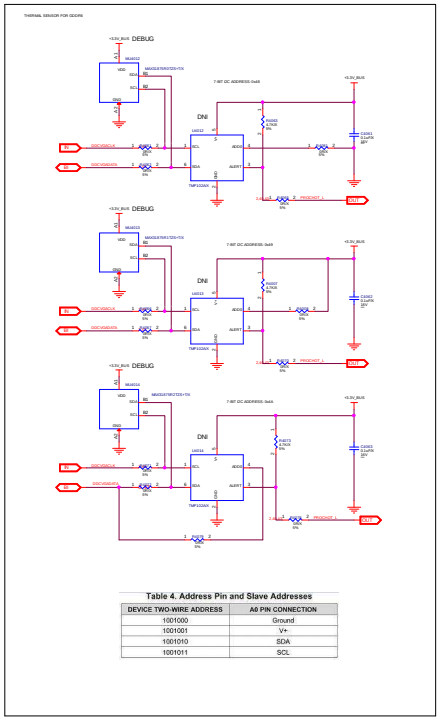
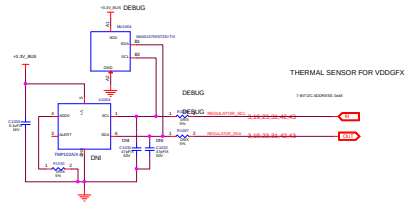
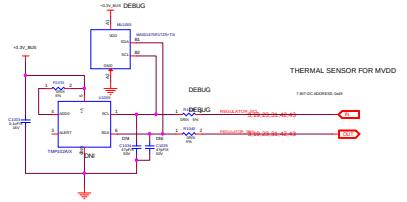
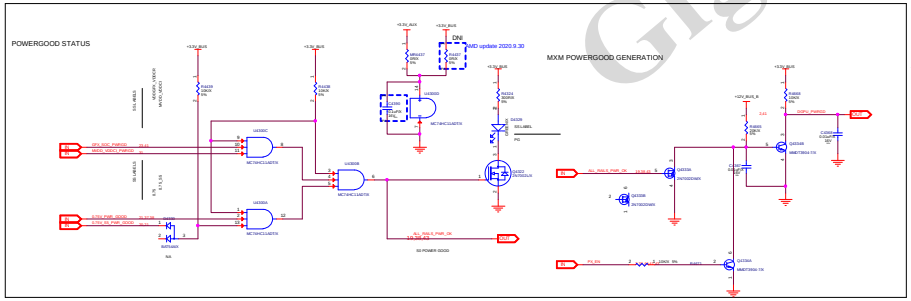


Table 4. Address Pin and Slave Addresses

DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL







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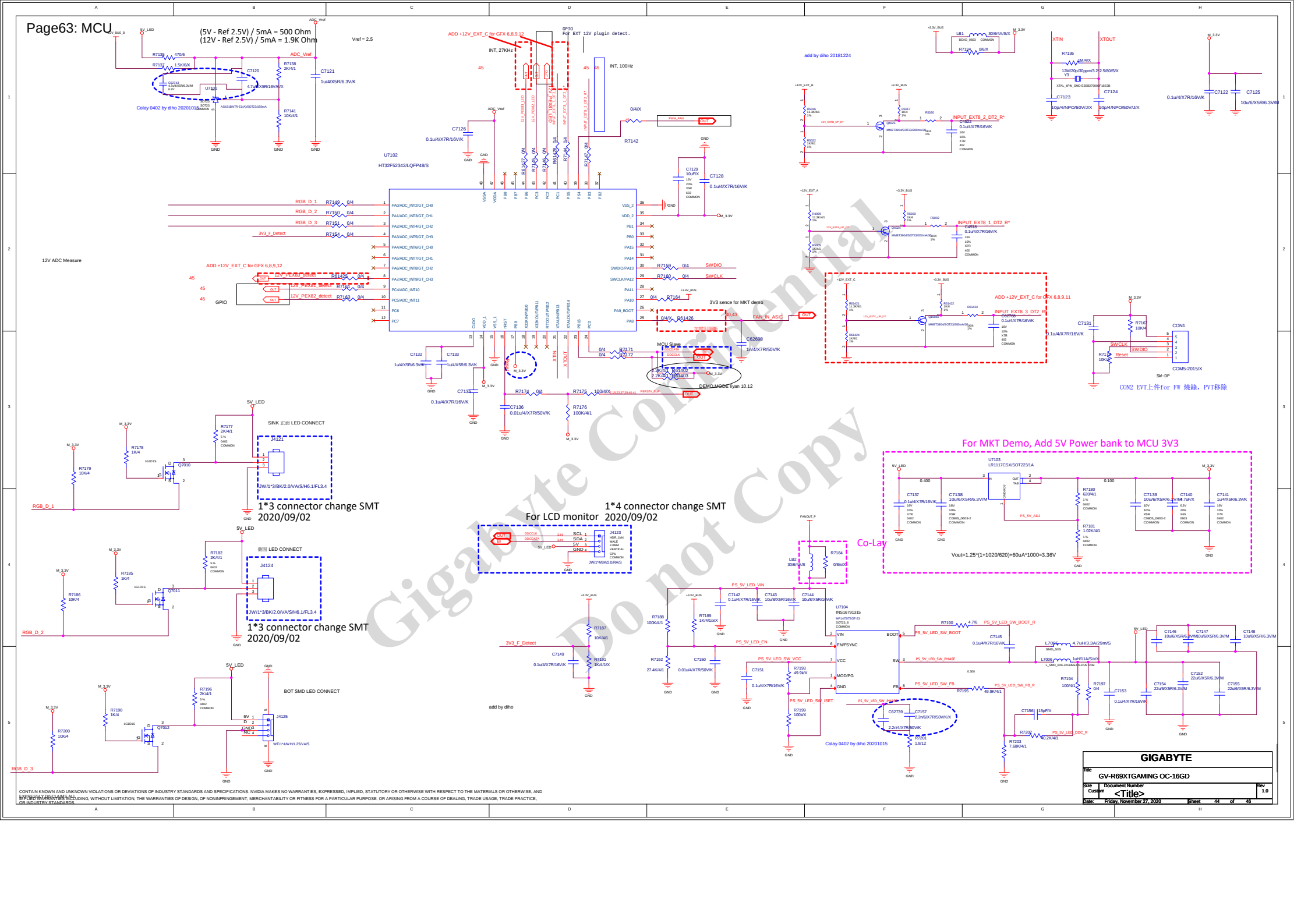

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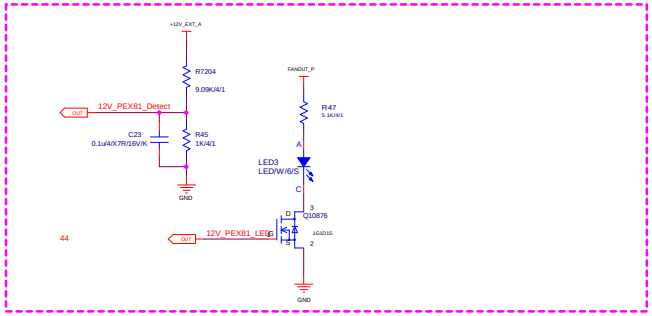
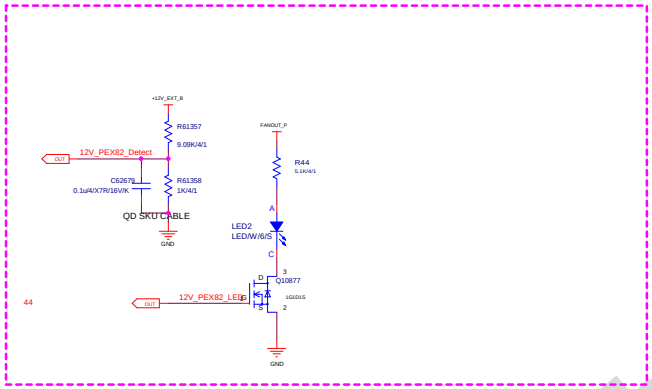
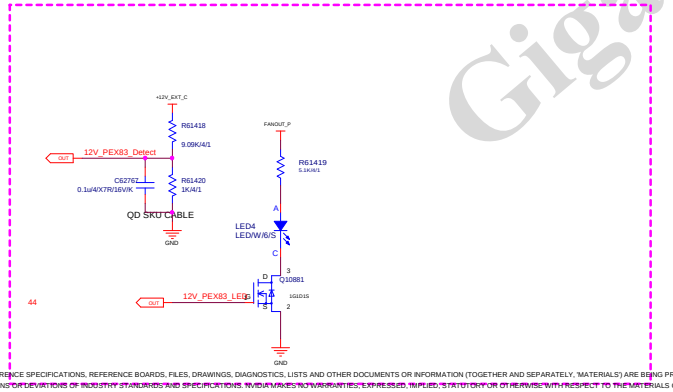
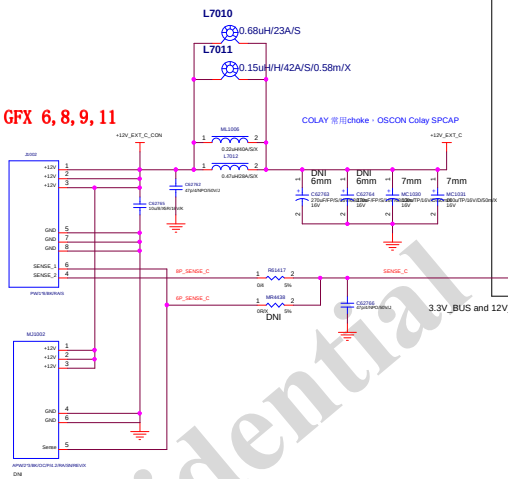


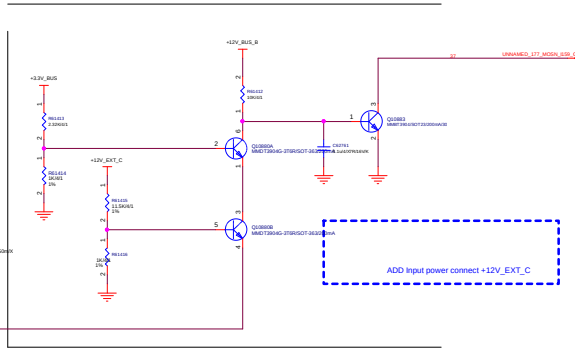




ADD +12V_EXT_C for GFX 6,8,9,11

0805 COLAY 0603 dlho 2018.12.02





3.3V_BUS and 12V_EXT_C (6PIN/8PIN) power-up sequence

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0	A	07/23/2019	Initial schematic creation
1	-00B	Nov 11 2019	Added MODS circuit
1	-00C	Jan 21 2020	Connected +1.8V_S5 to OSC_VDD18 Gated +VBUS_PWR_USBC0 by USB_CC_PWR_USBC0 Added Power protection circuits

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