

TITLE: Oland G5 2GB VGA/sDVI++HDMI/DP

TITLE: _____

DOCUMENT NUMBER: 105-C869xx-00B

D

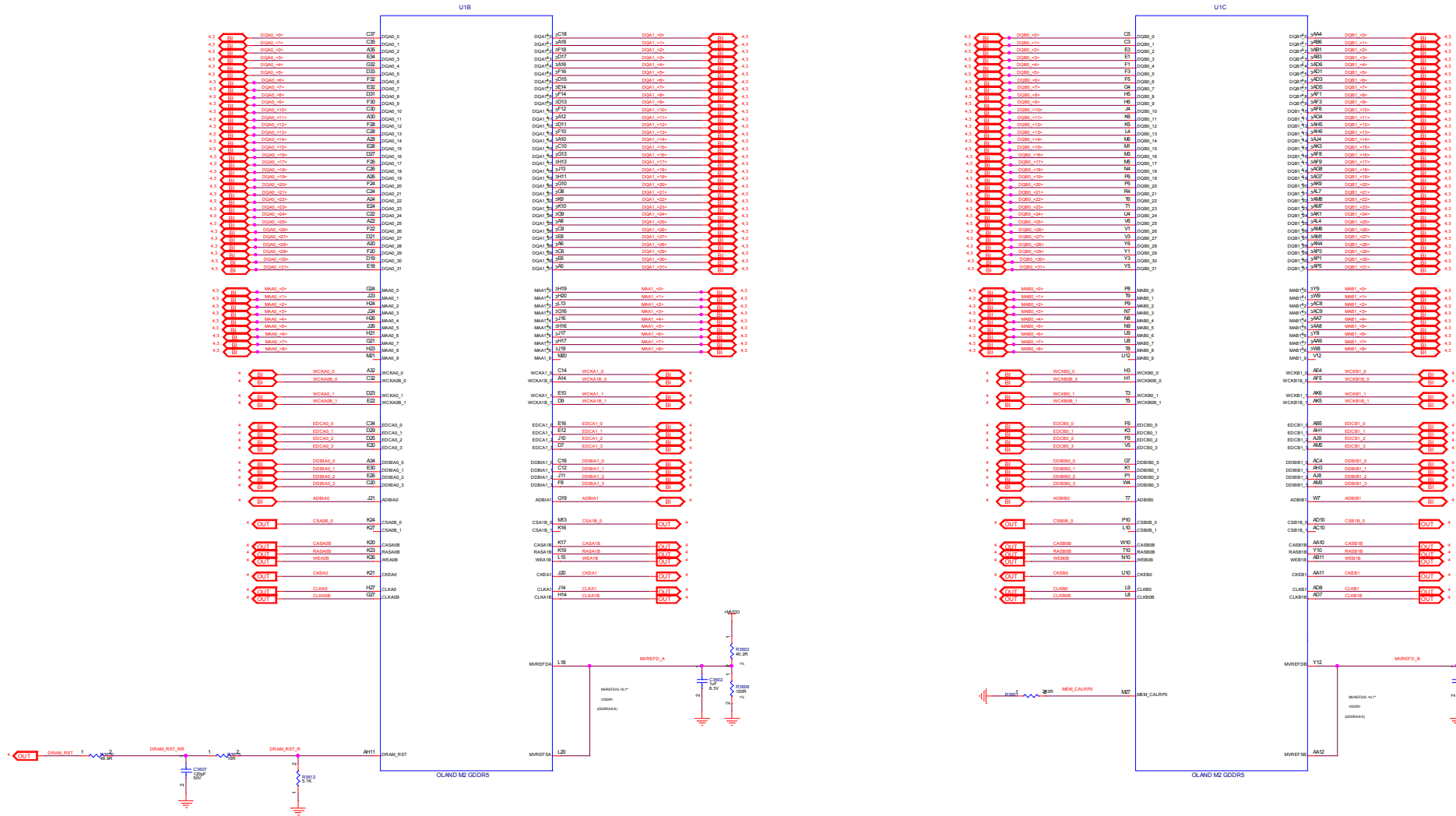
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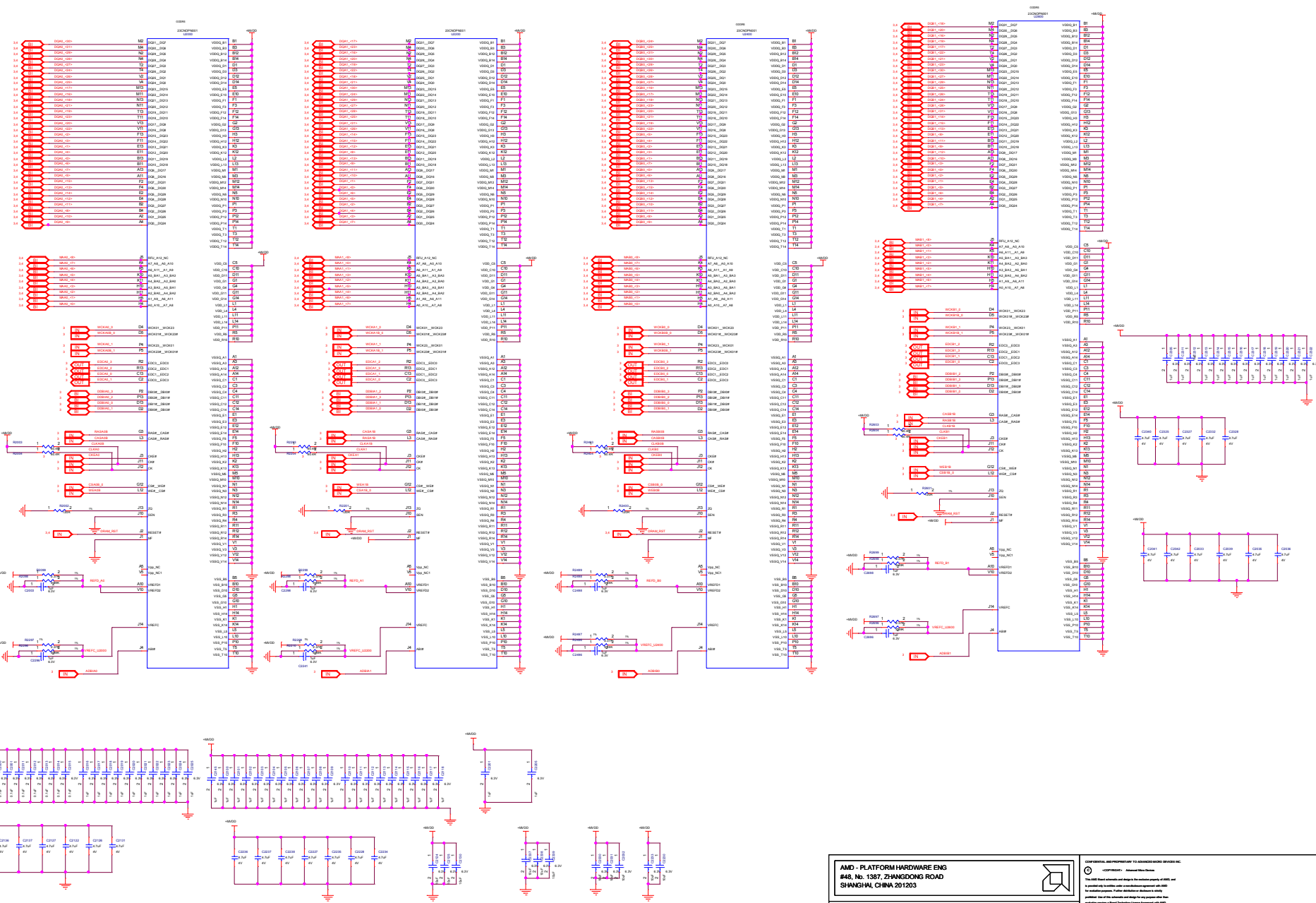


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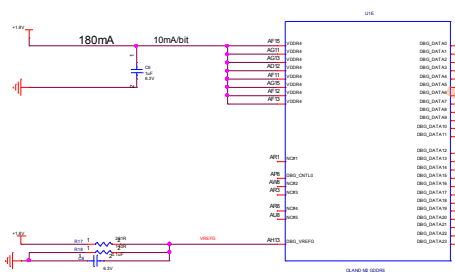
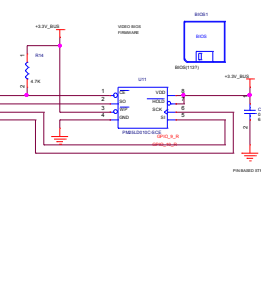
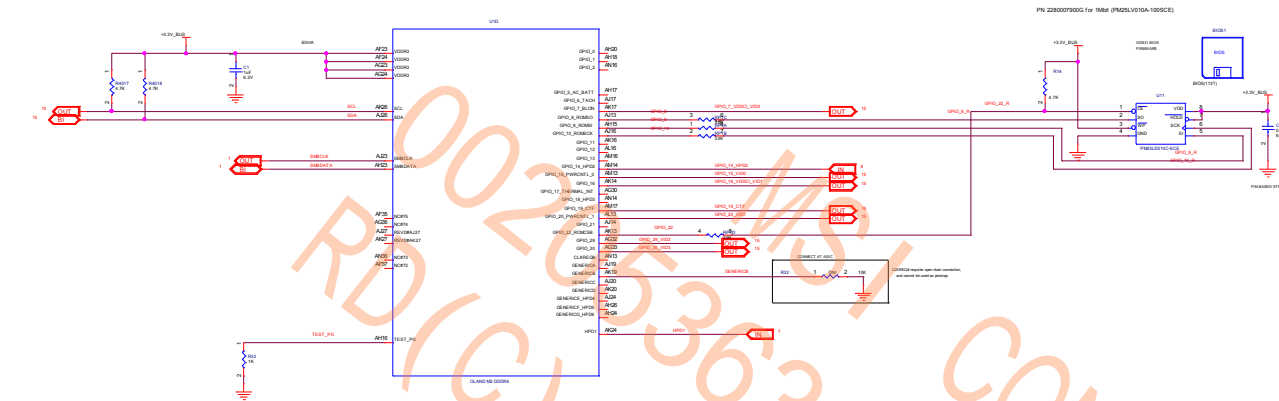
REV: 2.0

TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP





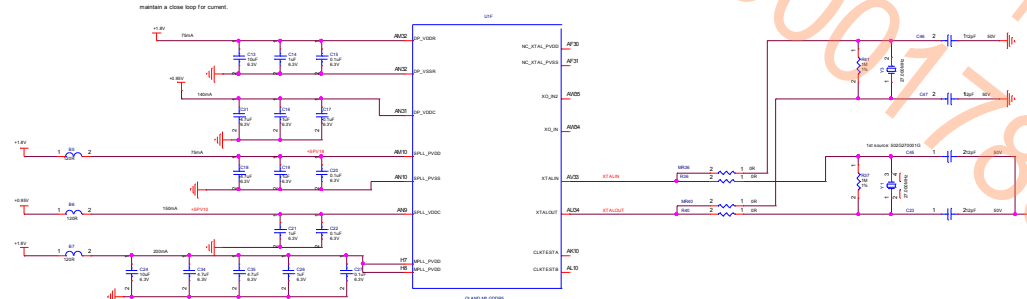
OLAND GPIOs Strap CF XTAL OSC



Place the crossfire
testpoints near the ASIC and
not the connector



Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.



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SHEET: 01 of 01 Class: EPIC STRAP PLATE

DATE: Mon Sep 21 10:05:39 2015

REV: 2.0

SHEET NUMBER: 5 OF 20

DOCUMENT NUMBER: 105-C869xx-00B

NOTES:

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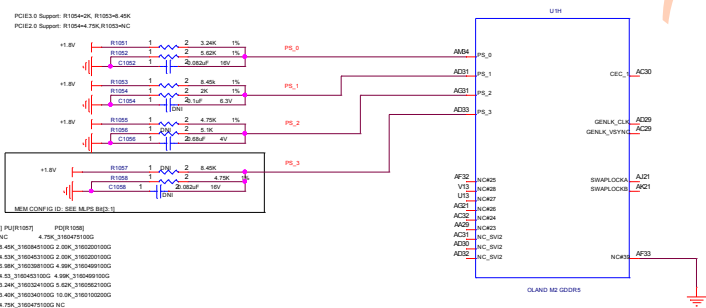
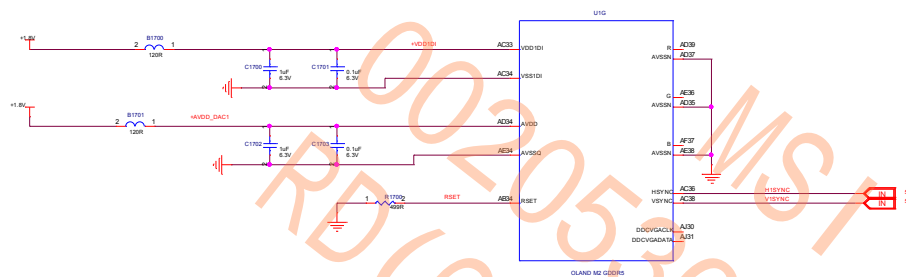
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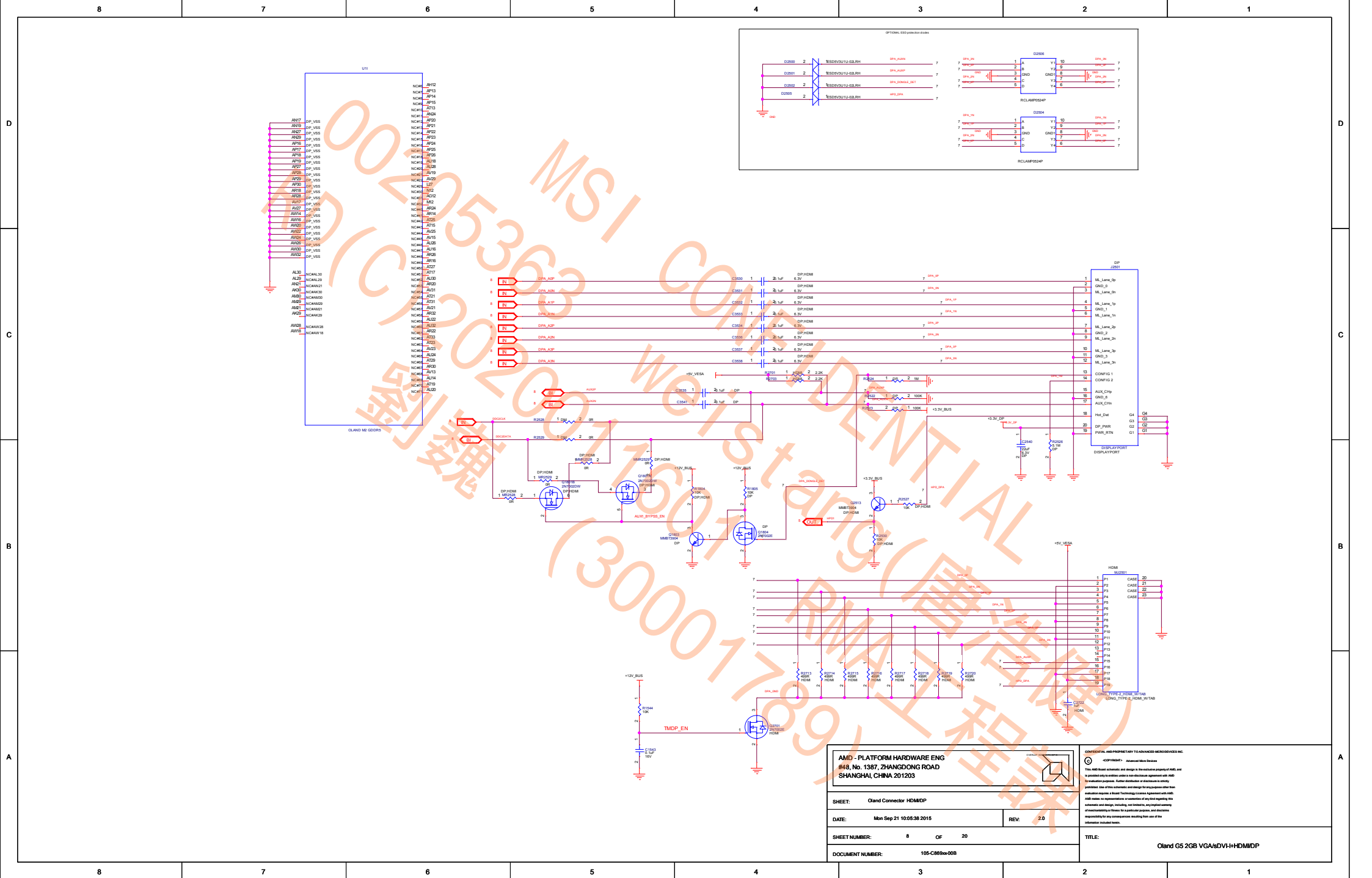
for evaluation purposes. Further distribution or disclosure is strictly

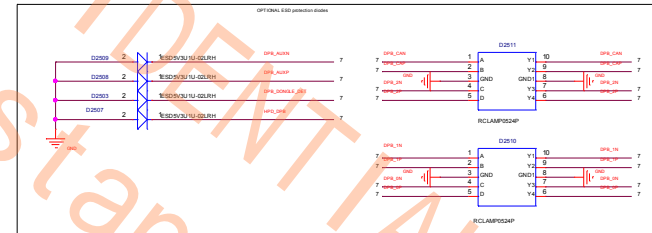
evaluation requires a Broad Technology License Agreement with NXP.

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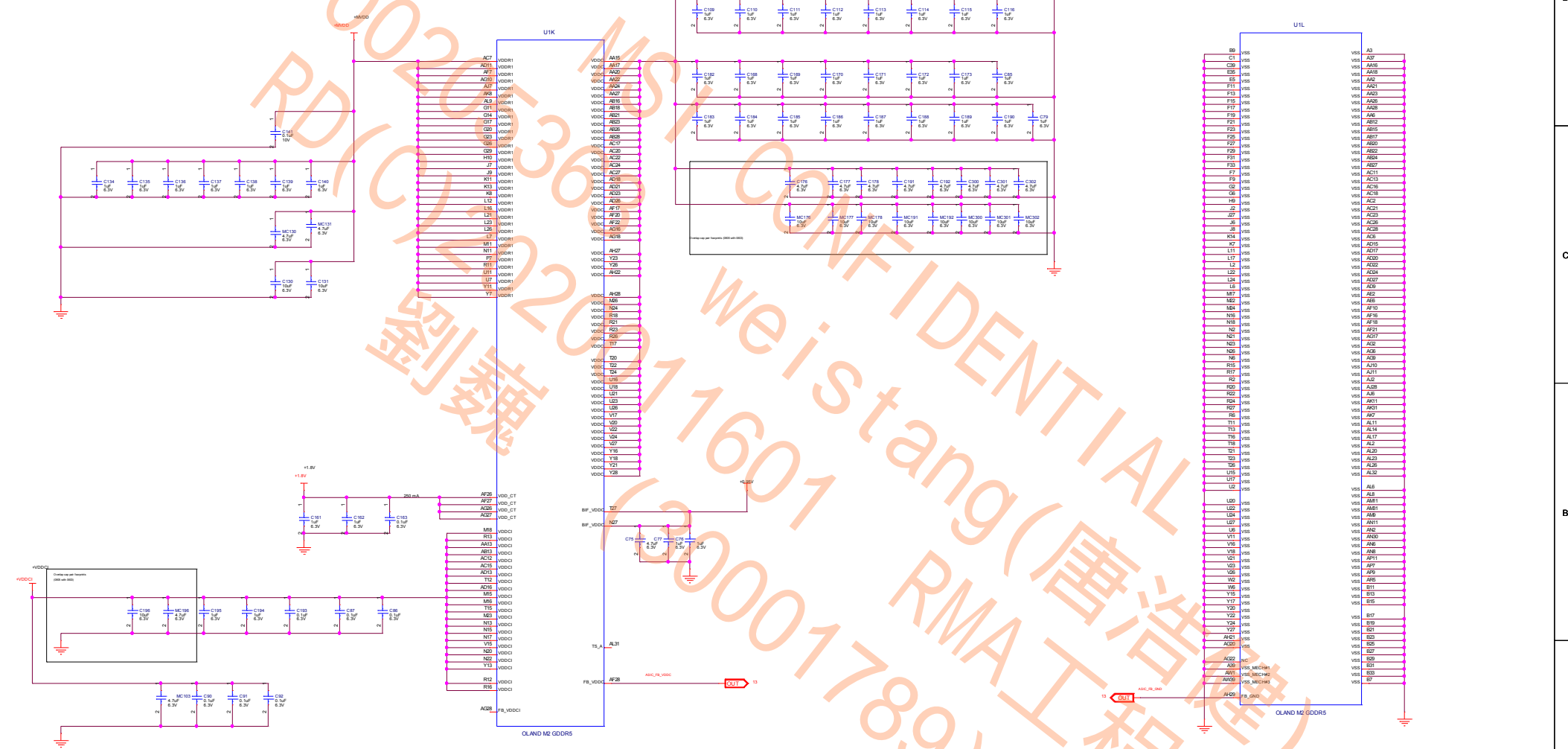


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<p>SHEET: Oland DAC and MLPS</p>	
<p>DATE: Tue Sep 22 06:32:58 2015</p>	<p>REV: 2.6</p>
<p>SHEET NUMBER: 6 OF 20</p>	
<p>DOCUMENT NUMBER: 105-C869xx-00B</p>	
<p>NOTES: NOTE</p>	<p>TITLE:</p> <p style="text-align: center; font-weight: bold;">Oland G5 2GB VGA/SDV1+HDMI/DP</p>





OLAND Power & GND



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SHEET: 01and Power&GND

DATE: Mon Sep 21 10:05:46 2015

REV: 2.0

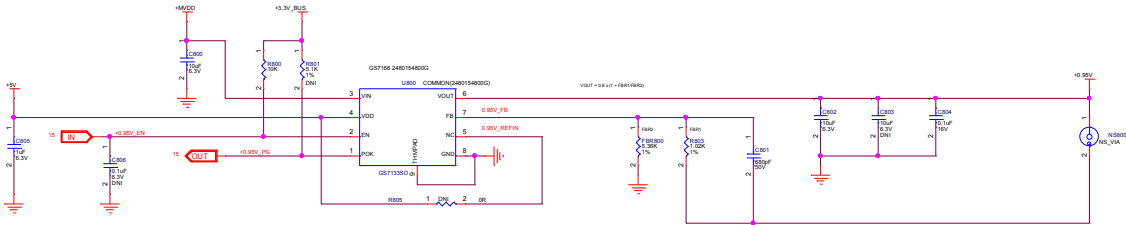
SHEET NUMBER: 9 OF 20

TITLE:

Oland G5 2GB VGA/sDVI-I+HDMI/DP

Linear Regulators

LDO #1: $V_{in} = +1.5V \pm 2\%$ $V_{out} = +0.95V \pm 2\%$ $I_{out} = 1.44A (T_{BV})_{RMS MAX}$
PCB: 50 to 70mm sq. copper area for cooling



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SHEET: 0.95V

DATE: Mon Sep 21 10:06:44 2015

REV: 2.0

SHEET NUMBER: 10 OF 20

DOCUMENT NUMBER: 105-C86900-008


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Regulator for MIDD

Use rVDDC_Source to share L801 to eliminate PCIe 12V current slew rate over spec issue(0.1A/us)
rVDDC_Source

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SHEET: VDDCI

DATE: Tue Sep 22 06:32:59 2015REV: 2.0

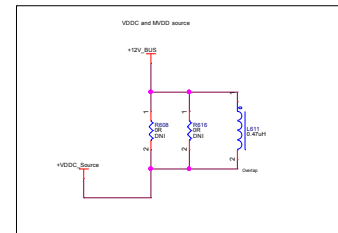
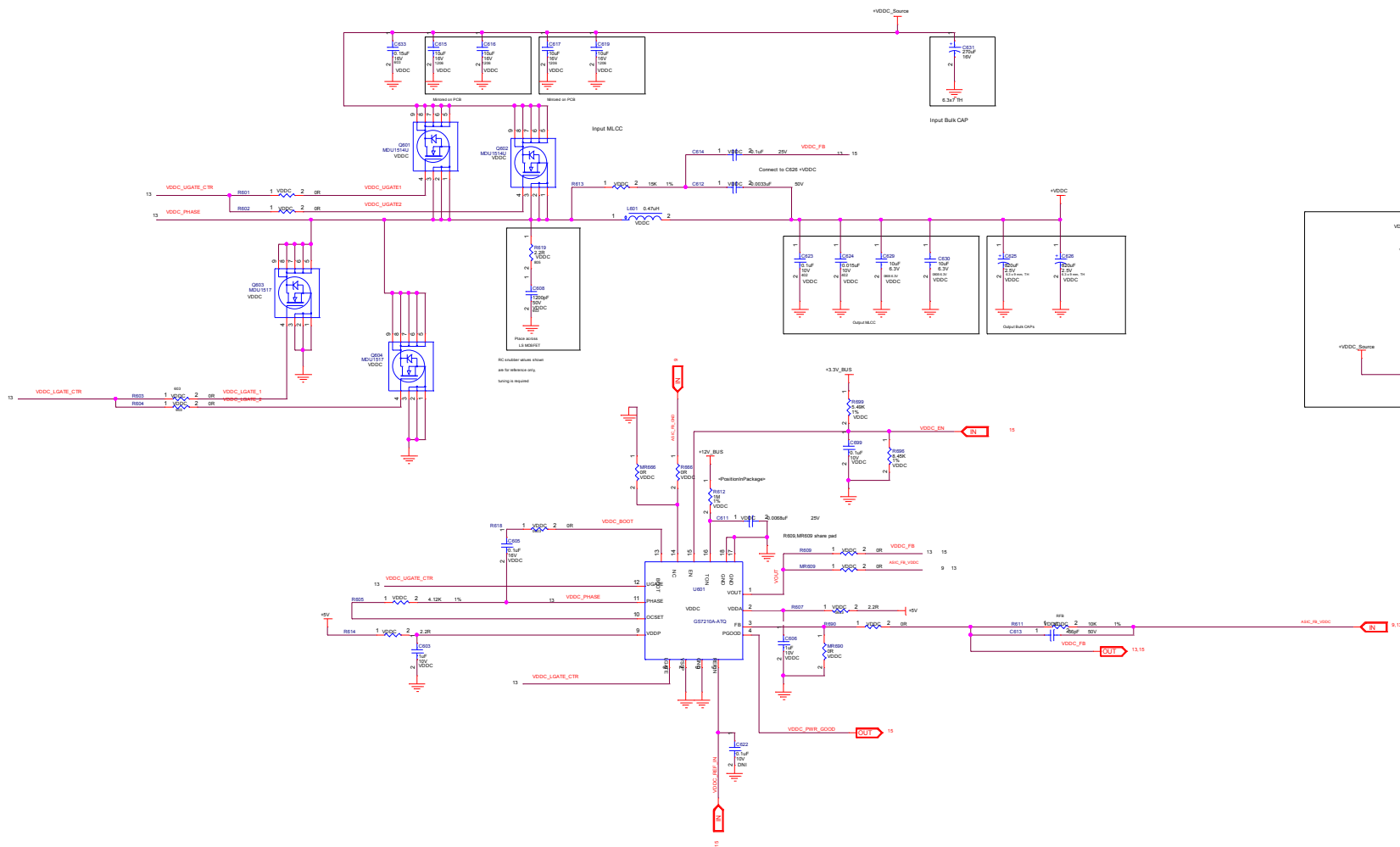
SHEET NUMBER: 12 OF 20

DOCUMENT NUMBER: 105-C869xx-008

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TITLE:
Oland G5 2GB VGA/sDVI-HDMI/DP

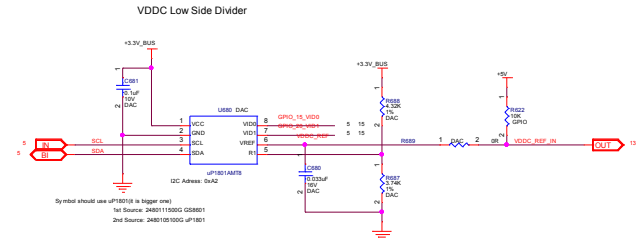
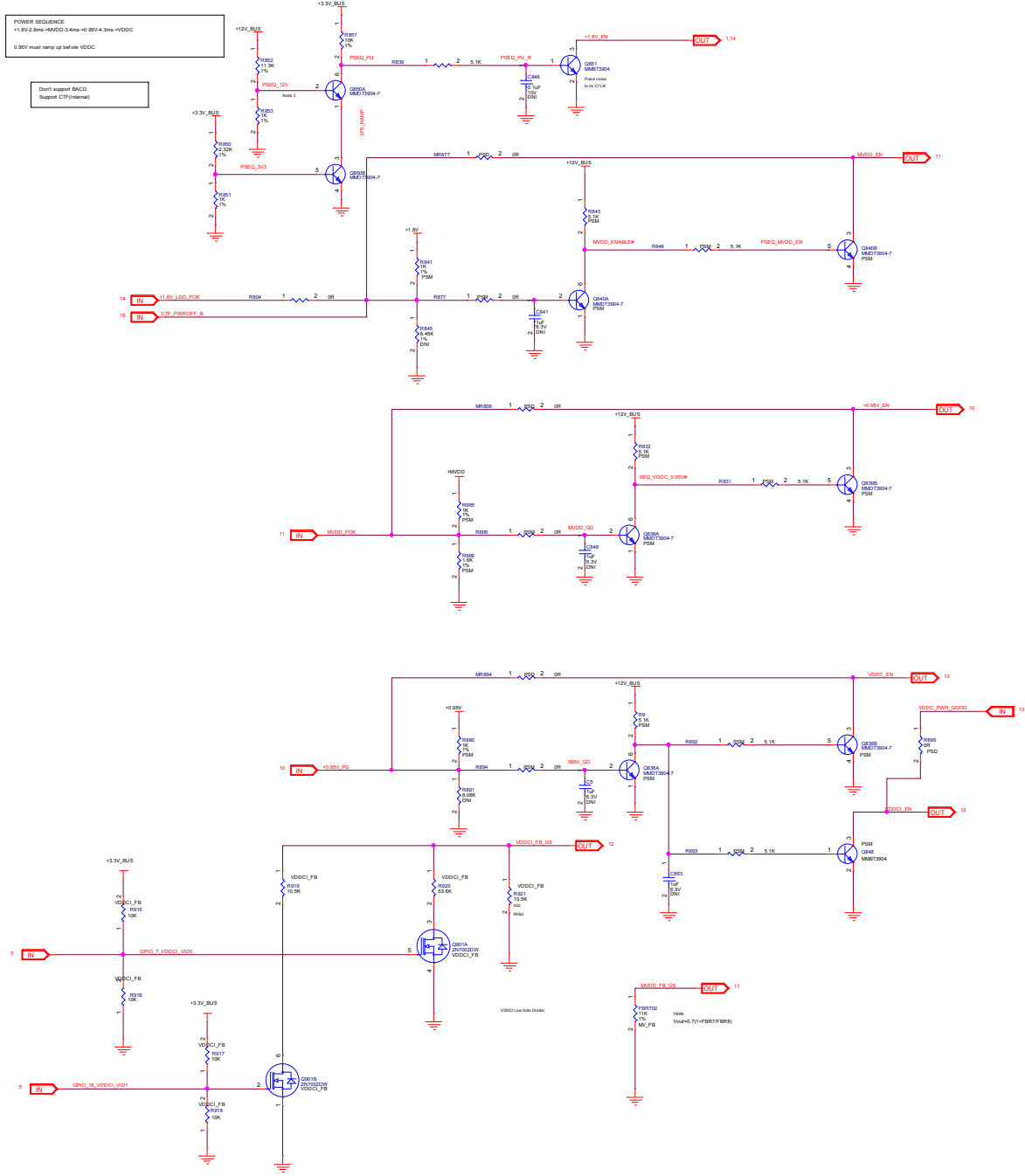


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SHEET: VDDC		REV: 2.0	
DATE: Mon Sep 21 10:06:41 2015		SHEET NUMBER: 13 OF 20	
DOCUMENT NUMBER: 105-C869-008		TITLE: Oland G5 2GB VGA+DVI+HDMI+DP	

Power Management - Power Gating and Dynamic Voltage Control

POWER SEQUENCE
+1.8V, 2.5ms-HVDDIO, 3.4ms-HVDDIO, 4.3ms-HVDDIO
0.95V must ramp up before VDDIO

Don't support SACD
(Support CTS/Deassert)



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SHEET: PWR MGMT & SEQ

DATE: Tue Sep 22 02:06:31 2016

SHEET NUMBER: 15 OF 20

DOCUMENT NUMBER: 105-C8600-008

REV: 2.0

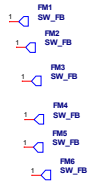
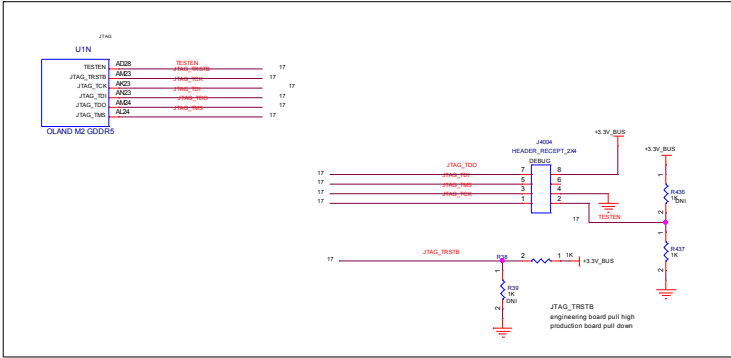
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TITLE: Oland G5 2GB VGA+DVI+HDMI+DP

(19) Debug Circuits



TOP
Single end
mem data
45 ohm +/- 5ohm
5.12 mils



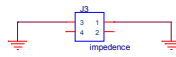
L3 INNER
Single end
Memory data
45 ohm +/- 5 ohm
6.89 mils



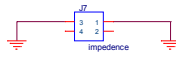
Bottom
Different
Address trunk
37 ohm +/- 5 ohm
7.05mils



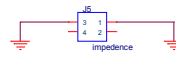
L4 INNER
Single end
Memory data
45 ohm +/- 5 ohm
6.89 mils



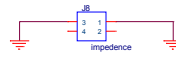
TOP
Different
TMS/ DP
85 ohm +/- 10 %
4.33 mils / 5.51 mils




L3 INNER
Different
TMS/DP
85 ohm +/- 10 %
4.33 mils / 5.51 mils

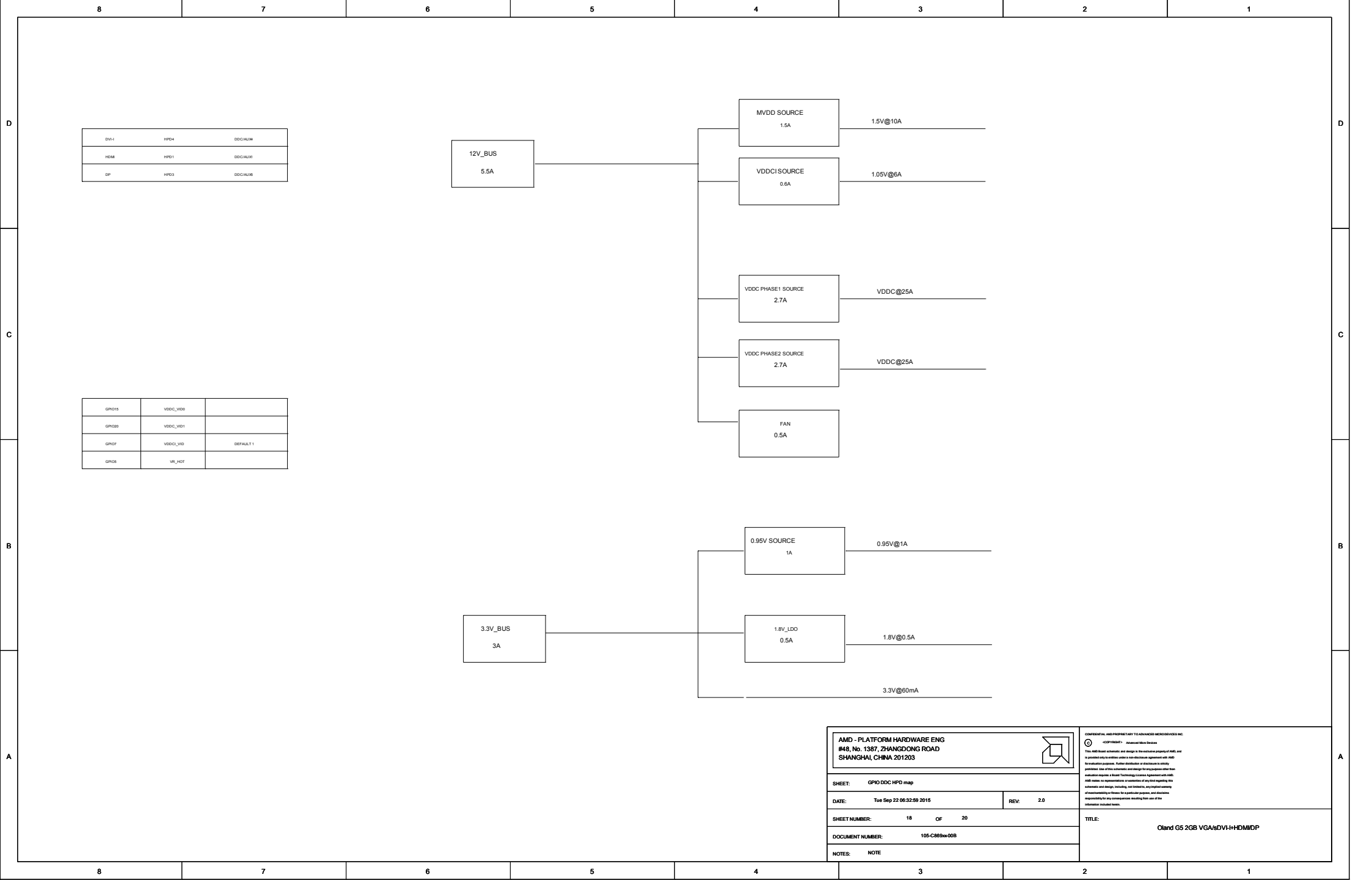


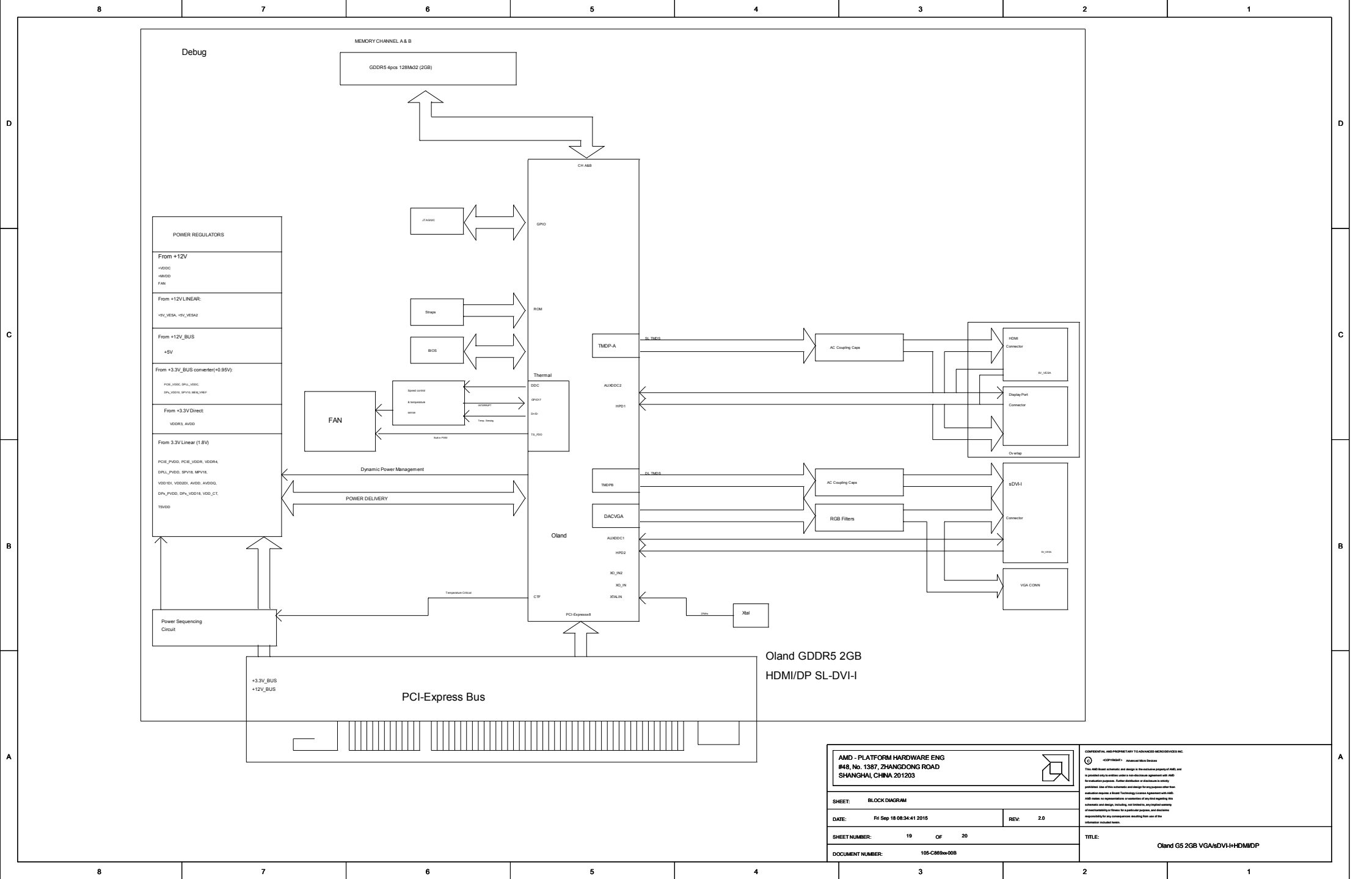
Bottom
Different
PEX PCIE
85 Ohm +/- 10 %
4.33mils/5.51mils



L4 INNER
Different
Mem Clock
80 ohm +/- 10 %
5.12 mils / 7.48 mils

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SHEET: Debug Circuit				TITLE:	
DATE: Mon Sep 21 10:05:47 2015		REV: 2.0		Oland G5 2GB VGA/ndVI-HDMI/DP	
SHEET NUMBER: 17 OF 20					
DOCUMENT NUMBER: 105-C869rev-008					





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<div>AMD</div> <div></div>		TITLE: <div>Oland G6 2GB VGA/sDV/H+HDMI/DP</div>		DOCUMENT NUMBER: <div>105-C889wa-008</div>		DATE: <div>Tue Sep 22 02:20:17 2015</div>		SHEET NUMBER: <div>20 OF 20</div>		REV: <div>2.0</div>			
REVISION HISTORY				ENGINEER: <div>Tony Yang</div>		NOTES: <div>NOTE</div>		<div>CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRODEVICES INC. This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for customer purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of its kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of this information included herein.</div>		<div>C ©COPYRIGHT Advanced MicroDevices</div>		AMD - PLATFORM HARDWARE ENG #48, No. 1367, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SCH Rev		PCB Rev		Date		REVISION DESCRIPTION							
1.00		000		06/19/14		1 Initial release							
2.00		000		09/22/15		2 Add VGA, etc							

D	
C	
B	
A	