

256/512MB 128-BIT GDDR2
LVDS, DVI-A, DVI-B, TV-OUT, VGA, HDMI
SLI, HDCP, MXM V2.0 TTP SUPPORT

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ID#	VARIANT	N/P/N	ASSEMBLY
0	BASE	86D-955S-950-000	SIDE LEVEL GENERIC SCHEMATIC ONLY - COMMON X VOL STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	86D-955S-950-000	S&H-430-450MS-220MS-10MS-GDDCZ-18MAN-BF&ICA-LIDS+DVS_AJVL_3=TV_OUT+VGA_MINI13X-HOCP
2	SKU000	86D-955S-950-000	S&H-430-450MS-10MS-10MS-GDDCZ-22MAN-BF&ICA-LIDS+DVS_AJVL_3=TV_OUT+VGA_MINI13X-HOCP
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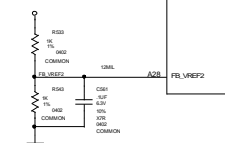
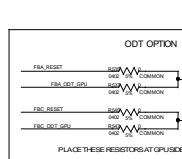
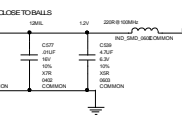
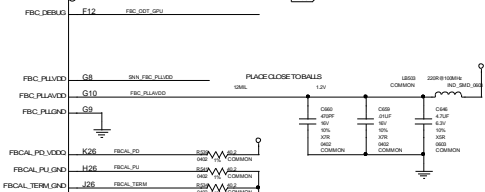
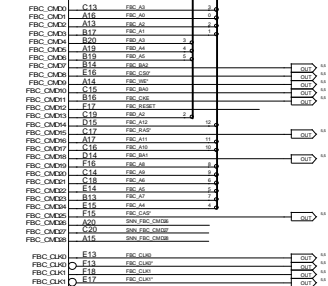
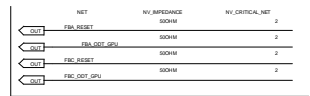
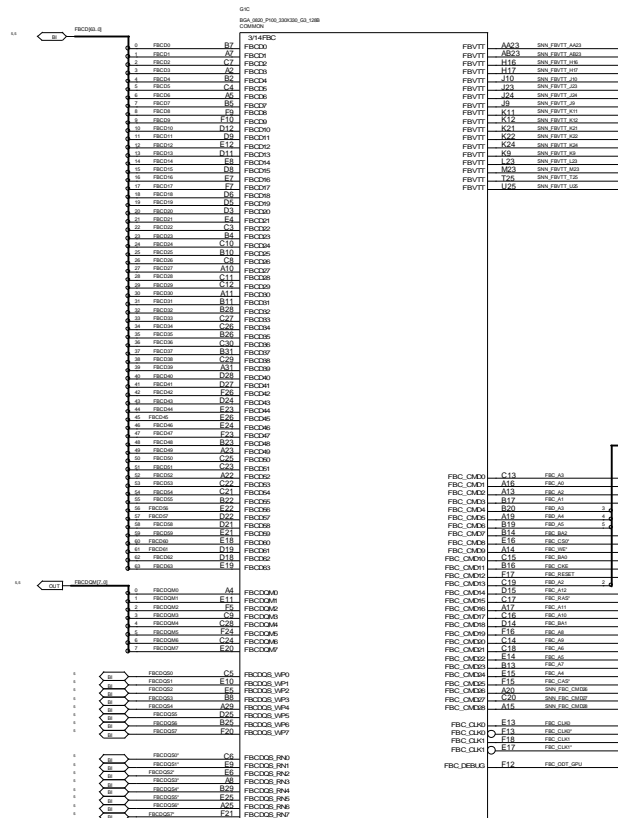
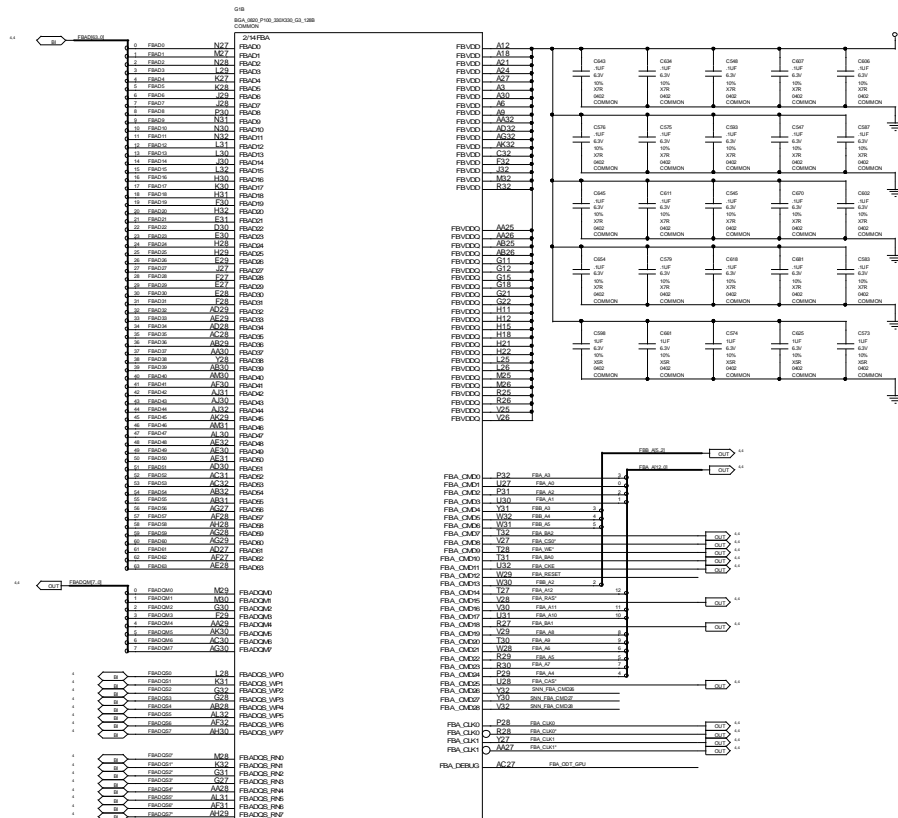
- 1) Change MEC1 JEDEC_TYPE from MCH_MXM2_HOLES to MECH_MXM2_HOLES_103NP_4VIAS
- 2) Add pull low resistor to MIOA_D[0] for straps
- 3) Add pull up resistor to MIOA_D[6] for straps

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FIN
PAGE DETAIL	Cover Page

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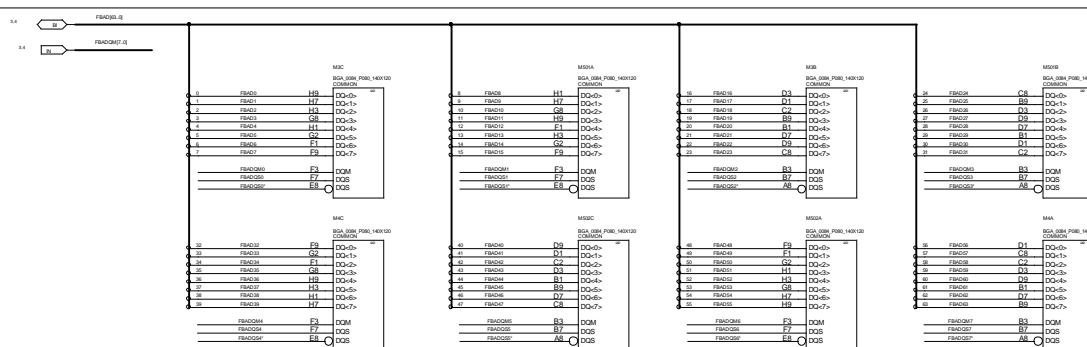
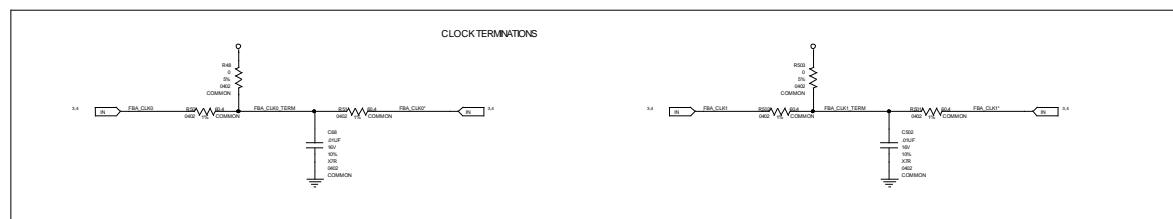
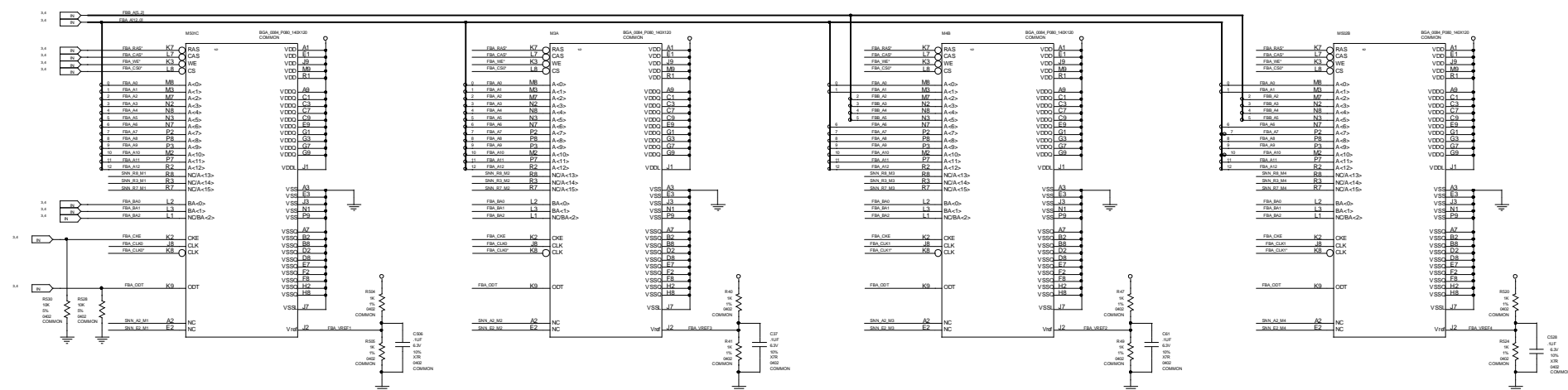
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[illegible]



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	10	FBA_VREF3	SWL	0.00V
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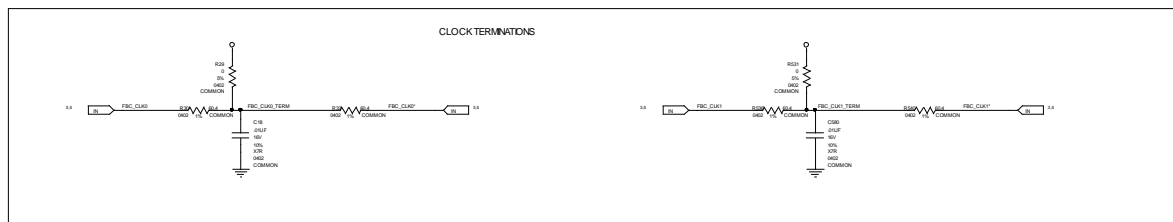
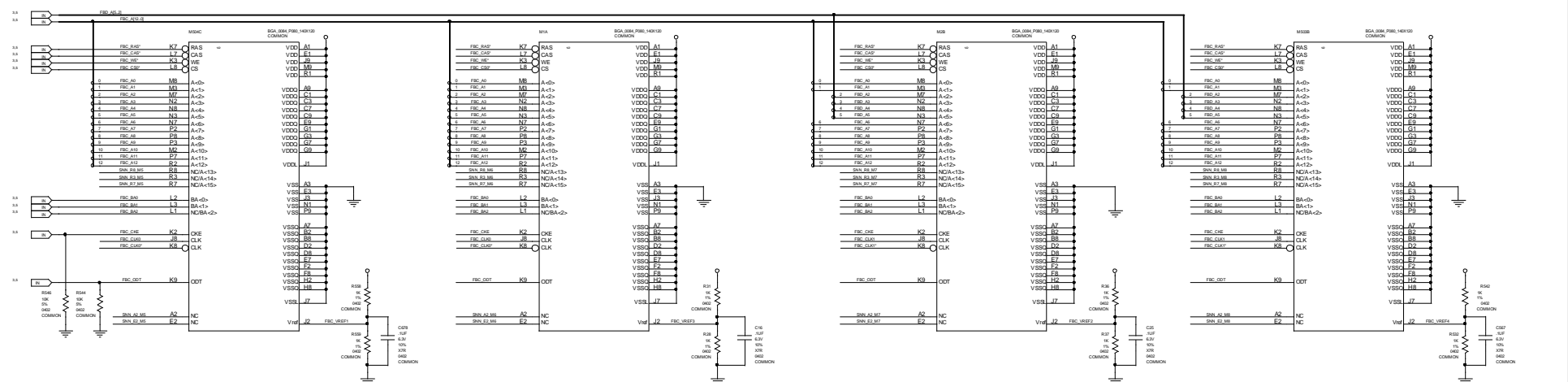


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PAGE DETAIL	Frame Buffer Partition A Memories

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SGL 0004 PIRL NERVO COMB										SGL 0004 PIRL NERVO COMB										SGL 0004 PIRL NERVO COMB										SGL 0004 PIRL NERVO COMB									
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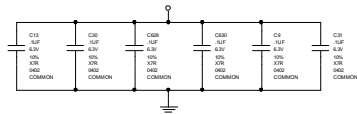
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PAGE DETAIL	Frame Buffer Partition C Memories

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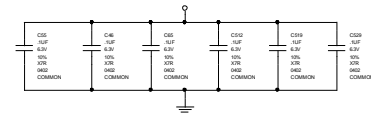
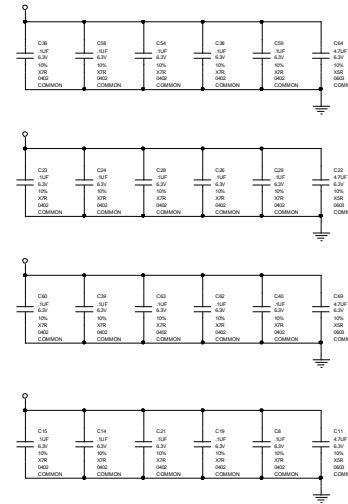
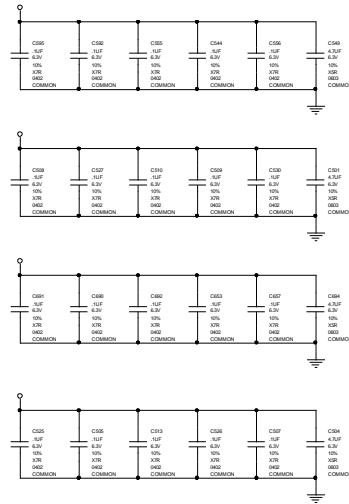


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DECOUPLING CAPS FOR MEMOIRS (PARTION A AND PARTION C)



NVDD TRANSITION CAP NEAR BY PARTION A



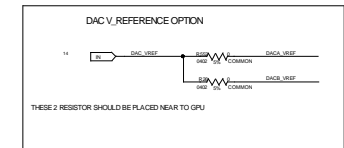
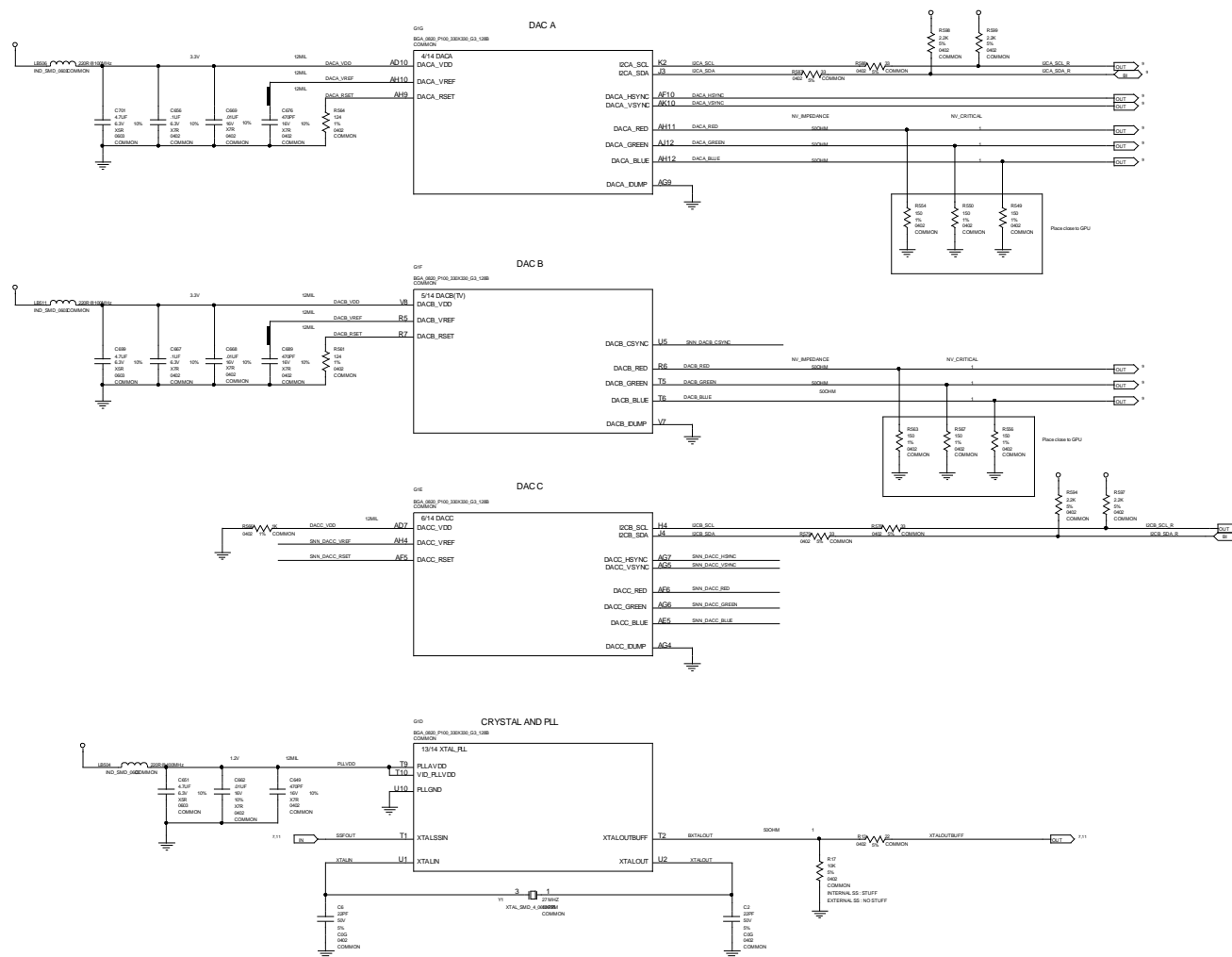
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FRIDGE DETAIL	Memory Decoupling Caps

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DATE		DATE	21-DEC-2006

PAGE 7) DAC_A, DAC_B, DAC_C, PLL, CRYSTAL



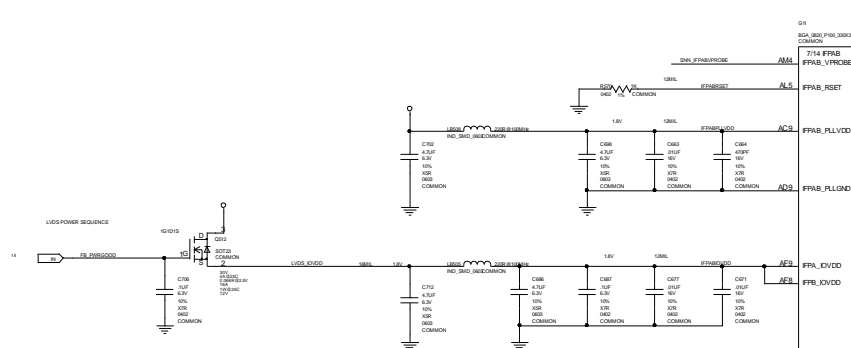
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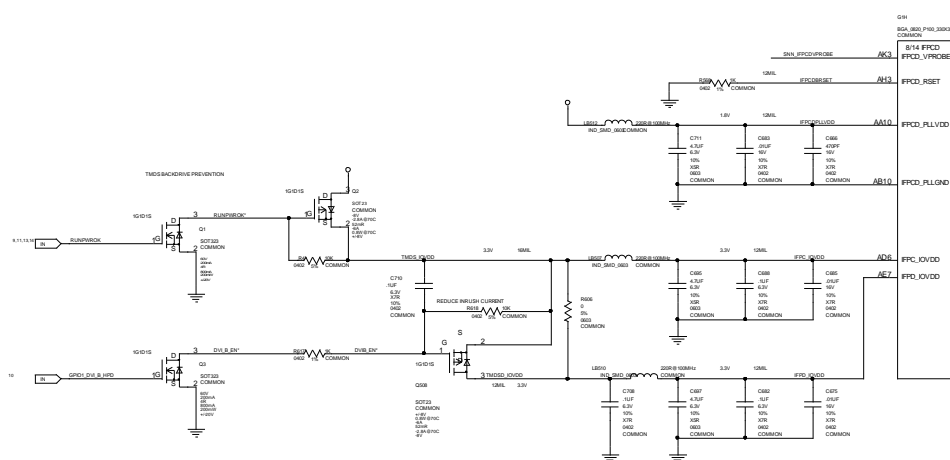
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LVDS

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FPR_TXD1 FPR_TXD1	A4	FPR17D1	FPR17D1	1	100001
	A4	FPR17D1	FPR17D1	1	100001
FPR_TXD1 FPR_TXD1	A17	FPR17D1	FPR17D1	1	100001
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FPR_TXD2 FPR_TXD2	A3	FPR17D2	FPR17D2	1	100001
	A3	FPR17D2	FPR17D2	1	100001
FPR_TXD3 FPR_TXD3	A15A	FPR17D3	FPR17D3	1	100001
	A3	FPR17D3	FPR17D3	1	100001
FPR_TAC	A5.4	FPR17C	FPR17C	1	100001
	A5.4	FPR17C	FPR17C	1	100001
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	A15	FPR17D4	FPR17D4	1	100001
FPR_TXD5 FPR_TXD5	A1.7	FPR17D5	FPR17D5	1	100001
	A17	FPR17D5	FPR17D5	1	100001
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	A1C	FPR17D6	FPR17D6	1	100001
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TMS

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PFC_TICD	<u>AE2</u>	EPFC7ICD	1	USPFC7
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PFC_TID	<u>AE1</u>	EPFC7IC	1	USPFC7
PFC_TICD	<u>AH1</u>	EPFC7ICD	1	USPFC7
PFC_TICD	<u>AK1</u>	EPFC7ICD	1	USPFC7
PFC_TIC	<u>AH2</u>	EPFC7IC	1	USPFC7
PFC_TIC	<u>AK2</u>	EPFC7IC	1	USPFC7
PFC_TICD	<u>AJ1</u>	EPFC7ICD	1	USPFC7
PFC_TICD	<u>AK1</u>	EPFC7ICD	1	USPFC7
PFC_TICD	<u>AL1</u>	EPFC7ICD	1	USPFC7
PFC_TICD	<u>AL2</u>	EPFC7ICD	1	USPFC7
PFC_TICD	<u>AO</u>	EPFC7ICD	1	USPFC7
PFC_TICD	<u>AO</u>	EPFC7ICD	1	USPFC7

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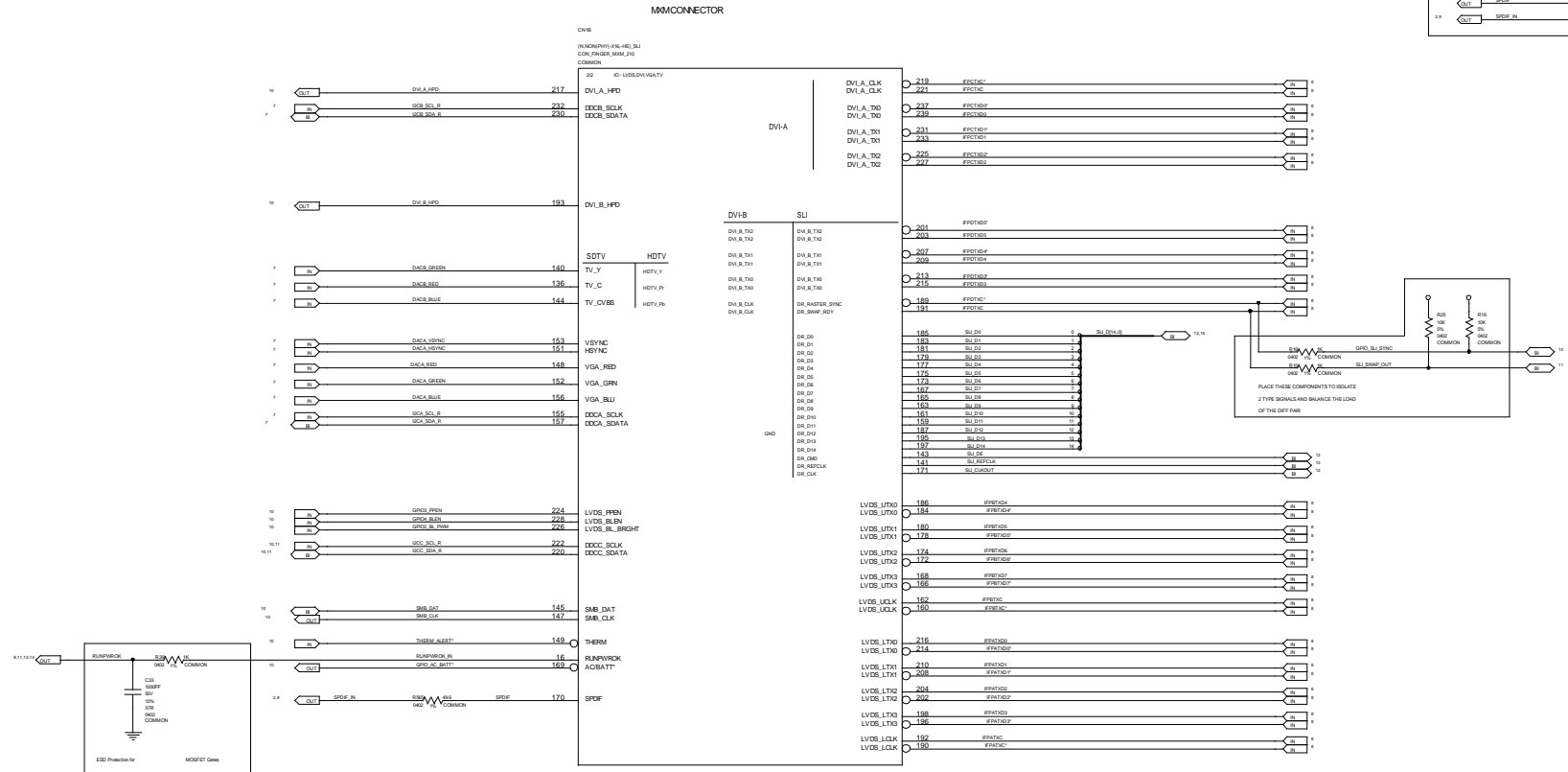
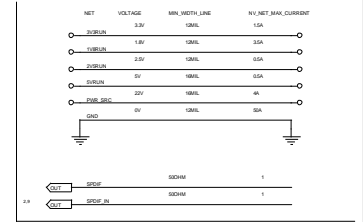
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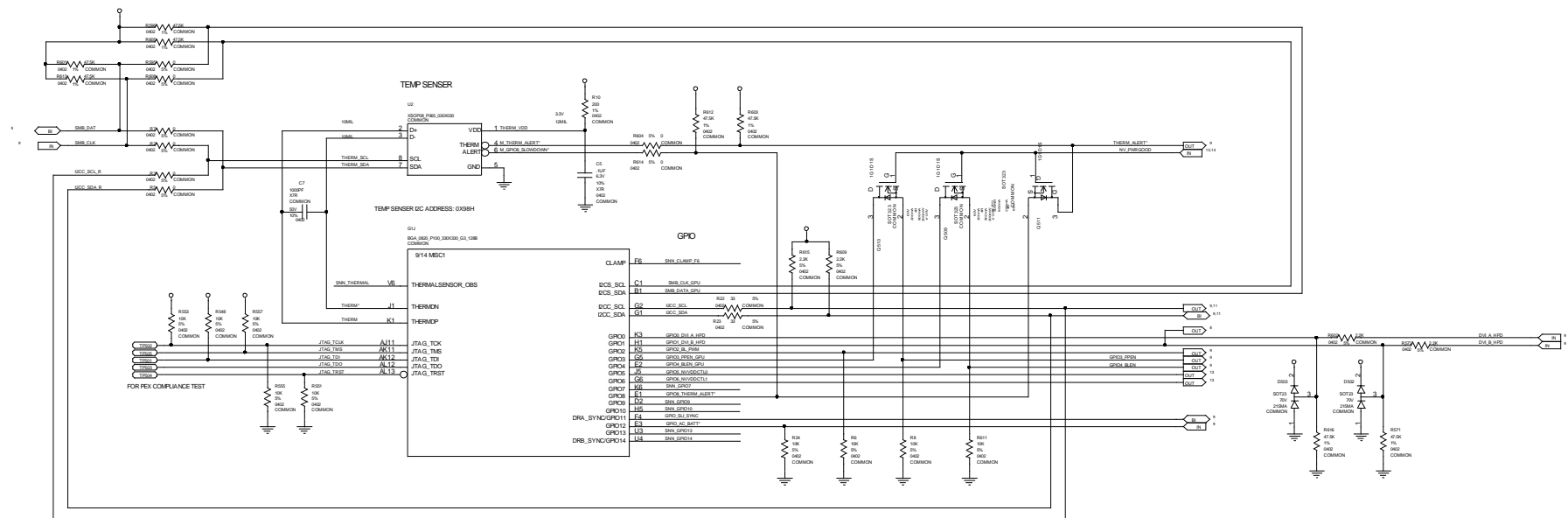
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PAGE DETAIL	GPIOs, JTAG, Thermal Sensor

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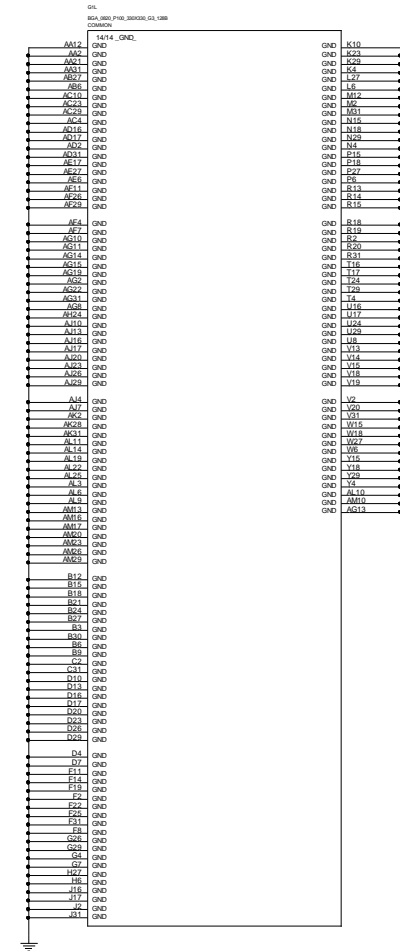
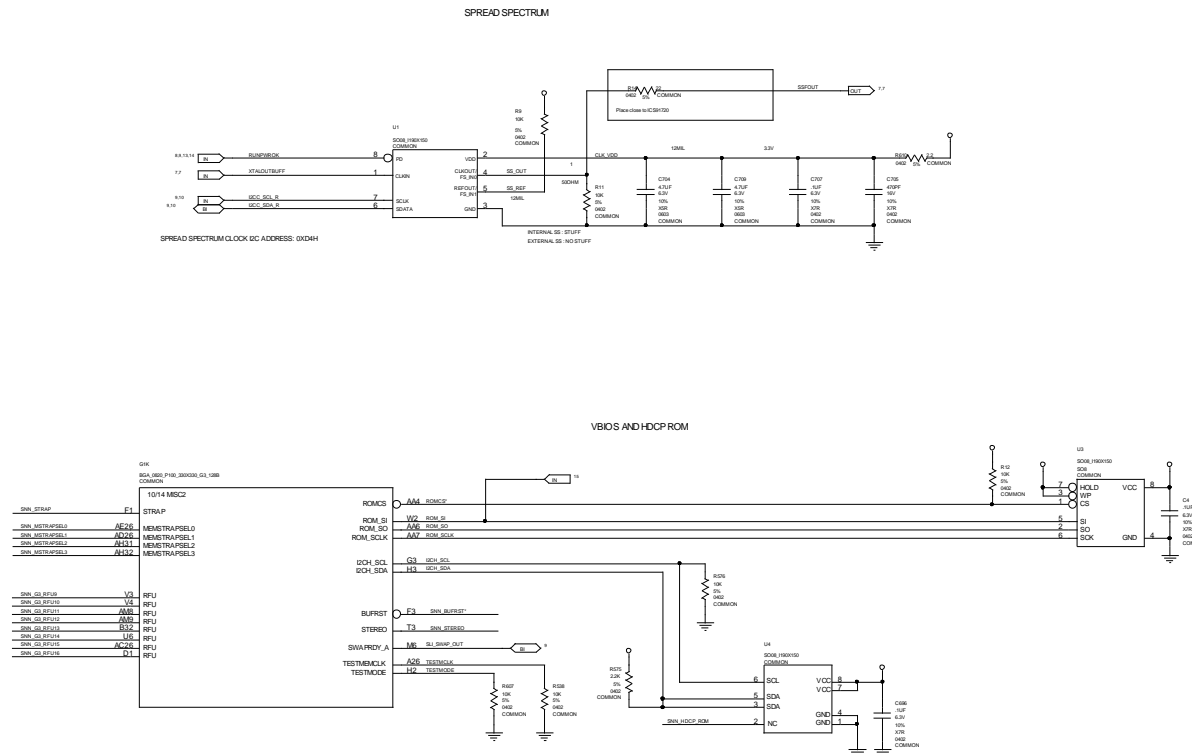
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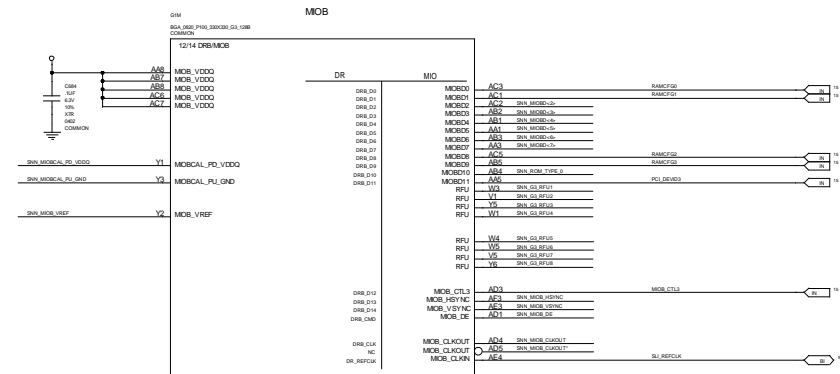
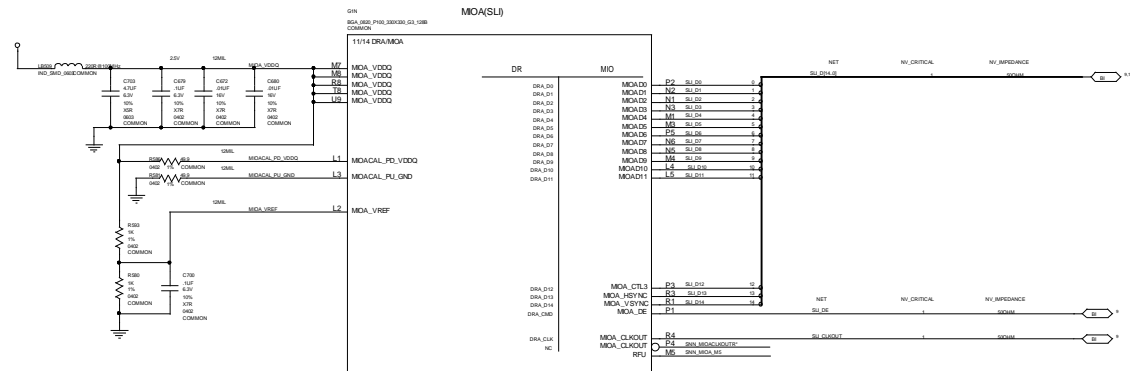
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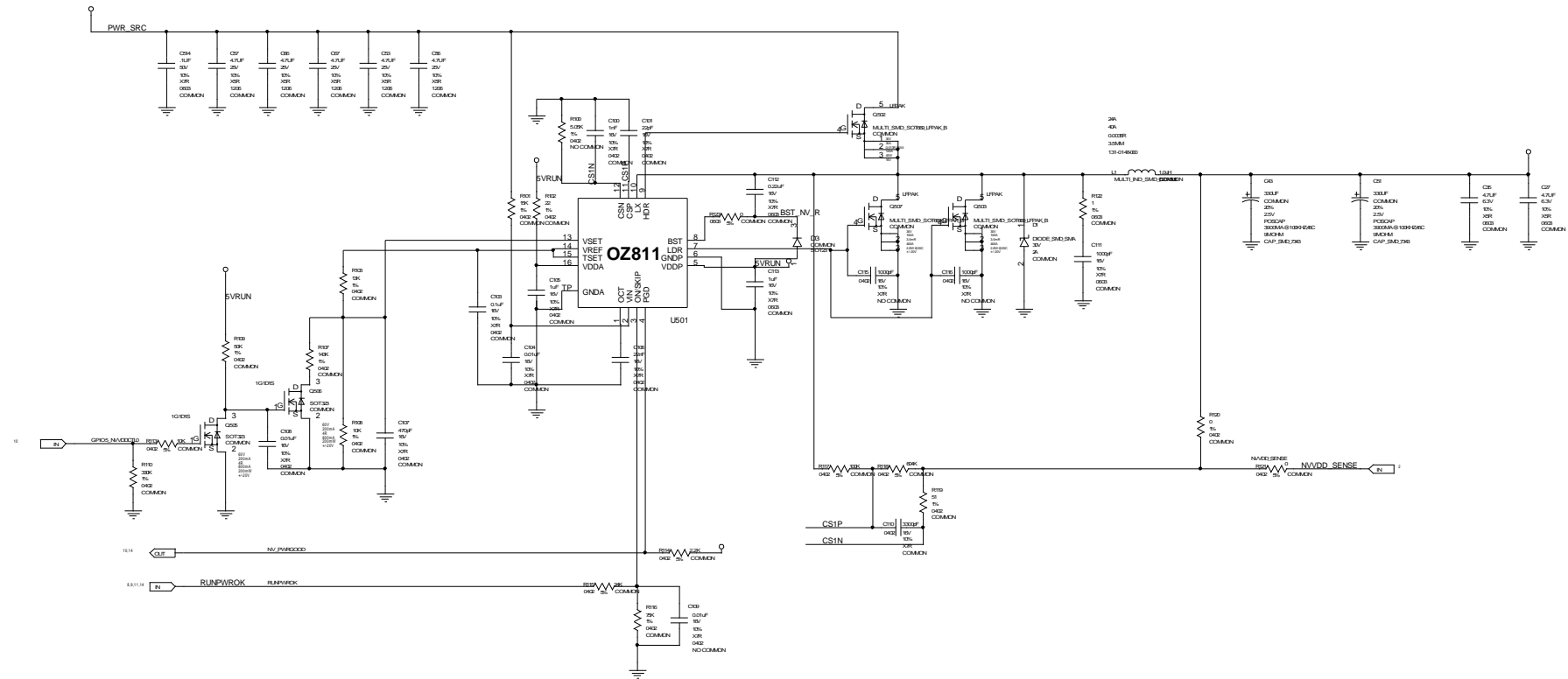
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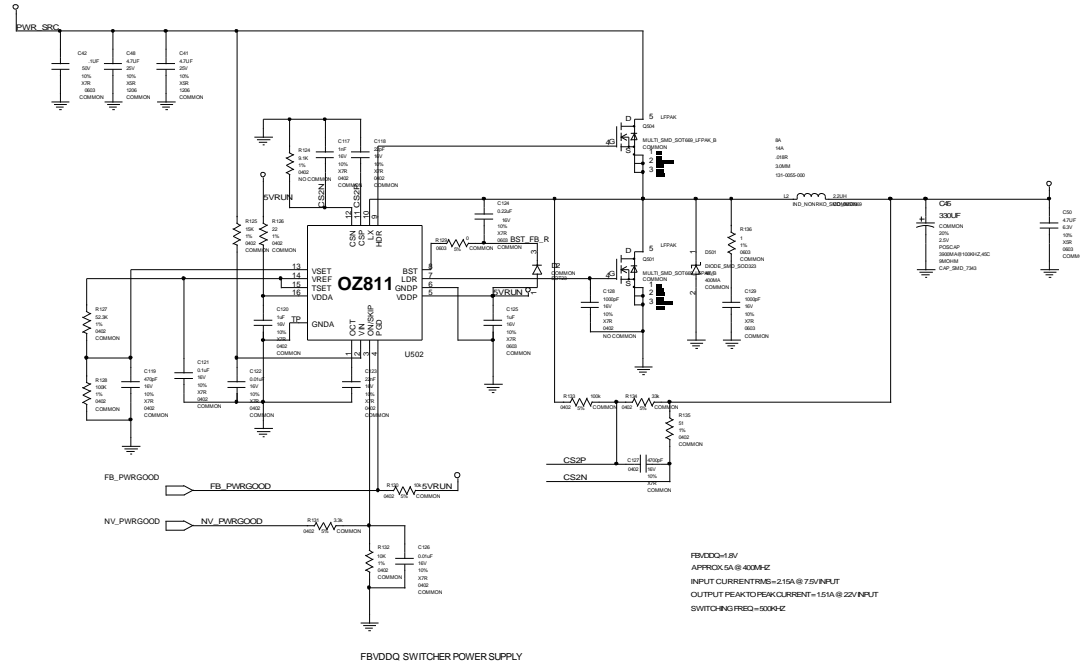
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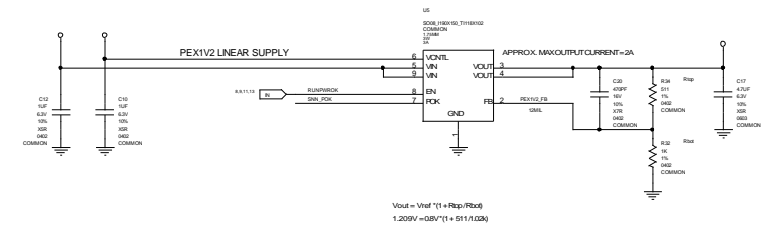
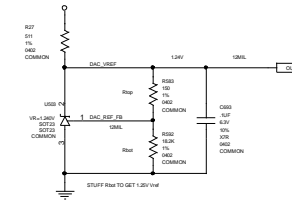
ID	NAME	DATE	21-DEC-2005



NET	VOLTAGE	MIN. WIDTH, LINE	MIN. NET MAX. CURRENT
PEX1V2	1.2V	10MIL	2A
FBVDDQ	1.8V	10MIL	1A



DAC V. REFERENCE SUPPLY



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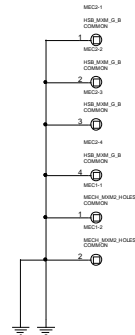
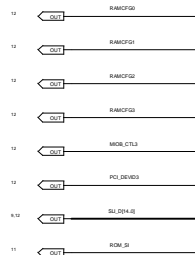
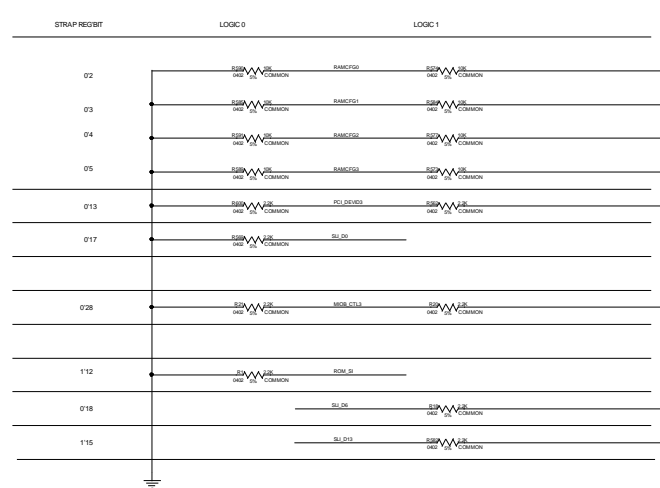
SANTA CLARA, CALIFORNIA 95050, USA

NV_PN 800-10555-9998-000 A

NAME

DATE 21 DEC 2008





RAM_CFG_0	<p>RAM_CFG[3]</p> <p>MS_0000: 16Mx16 DDR2 128Mx SRAM, ELUDA.</p> <p>MS_0001: 16Mx16 DDR2 128Mx SRAM, SAMSUNG, MOKION</p> <p>MS_0002: 16Mx16 DDR2 128Mx SRAM, INFINEON</p> <p>MS_0011: 16Mx16 DDR2 128Mx SRAM, HYUNDAI</p> <p>MS_0100: 32Mx16 DDR2 128Mx SRAM, ELUDA.</p> <p>MS_0101: 32Mx16 DDR2 128Mx SRAM, SAMSUNG, MOKION</p> <p>MS_0110: 32Mx16 DDR2 128Mx SRAM, INFINEON</p> <p>MS_0111: 32Mx16 DDR2 128Mx SRAM, HYUNDAI</p>
RAM_CFG_1	
RAM_CFG_2	
RAM_CFG_3	
PCI_DEVID_3	<p>MS_0: DEVICE ID = 0x0407: G84M00.</p> <p>MS_1: DEVICE ID = 0x0408: G84B700</p> <p>MS_1: DEVICE ID = 0x0428: G88M700</p>
PEX_PLL_EN_TERM00	
PCI_DEVID_EXT	
MOA_EN_3.3V	
3GIO_PADCFG_LUT_ADR[0]	
SLOT_CLOCK_CONFIGURATION	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	STRAPS, TTP, MOUNTING HOLE

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NAME		DATE	21-DEC-2006

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1	DNN_Q3_RPU11 11.4A DNN_Q3_RPU12 11.4A DNN_Q3_RPU13 11.4A DNN_Q3_RPU14 11.4A DNN_Q3_RPU15 11.4A DNN_Q3_RPU16 11.4A DNN_QND_SENSE 2.3P DNN_GPD7 10.3D DNN_GPD9 10.3D DNN_GPD10 10.3D DNN_GPD13 10.3D DNN_GPD14 10.3D DNN_GPU_A012 2.1D DNN_GPU_A013 2.3D DNN_HDCP_ROM 11.4D DNN_PPAPVPGORE 8.1D DNN_PPDEVPGORE 8.3D DNN_MICGLCOUTR* 12.2E DNN_MICL_M5 12.2E DNN_MICBICAL_PD_10D 12.3C Q DNN_MICBICAL_PU_QND 12.3C DNN_MICRD<-> 12.3E DNN_MICRD<-> 12.3E DNN_MICRD<-> 12.3E DNN_MICRD<-> 12.3E DNN_MICRD<-> 12.3E DNN_MICRD<-> 12.3E DNN_MICRD<-> 12.3E DNN_MICR_CLKOUT 12.4E DNN_MICR_CLKOUT* 12.4E DNN_MICR_DE 12.4E DNN_MICR_HSVNC 12.4E DNN_MICR_VREF 12.4C DNN_MICR_VSVNC 12.4E DNN_METRAPSEL0 11.3A DNN_METRAPSEL1 11.3A DNN_METRAPSEL2 11.3A DNN_METRAPSEL3 11.3A DNN_PCK 14.4C DNN_R3_M1 4.2A DNN_R3_M2 4.2C DNN_R3_M3 4.2E DNN_R3_M4 4.2D DNN_R3_M5 5.3A DNN_R3_M6 5.3C DNN_R3_M7 5.2E DNN_R3_M8 5.2D DNN_R7_M1 4.2A DNN_R7_M2 4.2C DNN_R7_M3 4.2E DNN_R7_M4 4.2D DNN_R7_M5 5.2A DNN_R7_M6 5.2C DNN_R7_M7 5.2E DNN_R7_M8 5.2D DNN_R8_M1 4.2A DNN_R8_M2 4.2C DNN_R8_M3 4.2E DNN_R8_M4 4.2D DNN_R8_M5 5.3A DNN_R8_M6 5.3C DNN_R8_M7 5.2E DNN_R8_M8 5.2D DNN_RCM_TTYPE_0 12.3E DNN_STEREO 11.4C DNN_STRAP 11.3A DNN_THERMAL 10.3B SPDF_IN 9.1D> 9.4C SPDF_IN 2.5G< 9.1D> 9.4B> SPDF_OUT 7.4C< 7.5G< 11.2D> SS_OUT 11.2C SS_REF 11.2C TESTNCLK 11.4C TESTNODE 11.4C THERM 10.3B THERM 10.3B THERM_ALERT* 9.4B> 10.2P> THERM_SCL 10.2B THERM_SDA 10.2B THERM_VDD 10.2C TMOSD_OVDD 8.4C TMOSD_OVDD 8.4B MVALN 7.4C 7.5G< MVALOUT 7.4D 7.5D> MVALOUTBUFF 7.4P> 7.5G> 11.2B>								
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<div><div>ASSEMBLY</div><div>BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL</div></div> <div><div>PAGE DETAIL</div><div><edit here to insert page detail></div></div>									<div><div>NVIDIA CORPORATION</div><div>2701 SAN TOMAS EXPRESSWAY</div><div>SANTA CLARA, CA 95050 USA</div><div><div>NV_PN</div><div>600-10555-9998-000 A</div></div><div><div>ID</div><div></div><div>PAGE</div><div></div></div><div><div>NAME</div><div><ENGINEER></div><div>DATE</div><div>21-DEC-2008</div></div></div>
	A	B	C	D	E	F	G	H	

