

# P360-A00 Base Design

P360-A00, G92, 16Mx32 GDDR3 (900MHz),TV(OPTION)  
DVI-I-DL, DVI-I-DL

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- V186-1.0 Base on P360
- 1.PAGE11: ADD VGA display connector
  - 2.PAGE12: Move IFP C/D HDMI to page 13
  - 3.PAGE13: Unused DACB Interface, ADD IFP C/D HDMI interface
  - 4.PAGE15: Use I2CC for HDMI control, add GPIO10/14 for HDMI control
  - 5.PAGE18:Add FM1~FM6
- V186-1.1 Base on V186-1.0
- V186-1.1 Base on V186-1.0 remove the reference place of the 6.1 mil RGB signal.
- V186-1.2 Base on V186-1.1
- V186-1.2 Base on V186-1.1 change PCB color from RED to Coffee


REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10360-base-000	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0050	600-10360-0050-000	P360 G92 287 512MB GDDR3 16Mx32 DVI-I-DV11
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3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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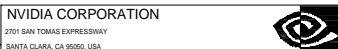
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2701 SAN TOMAS EXPRESSWAY

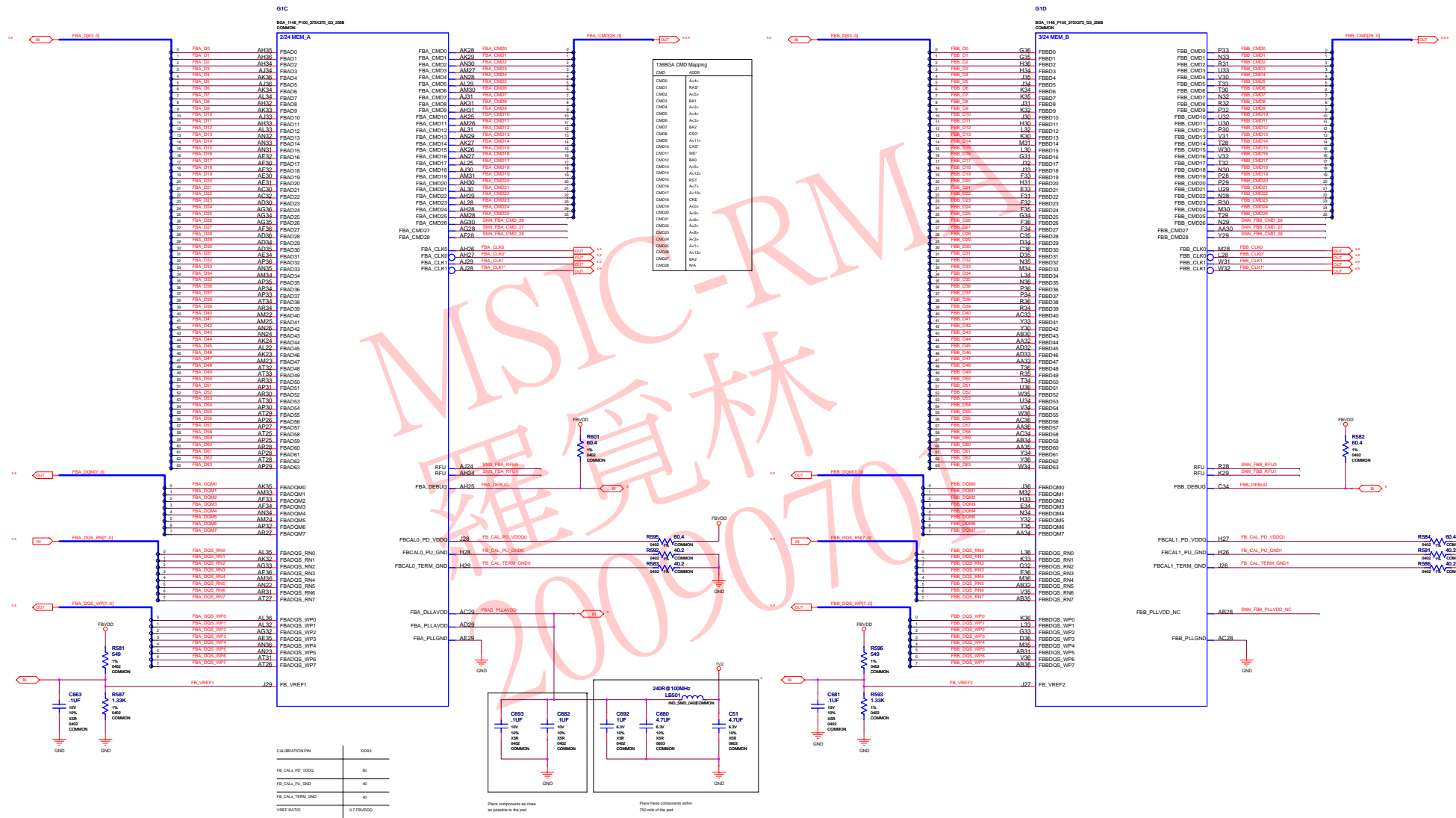
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PAGE DETAIL	Overview		
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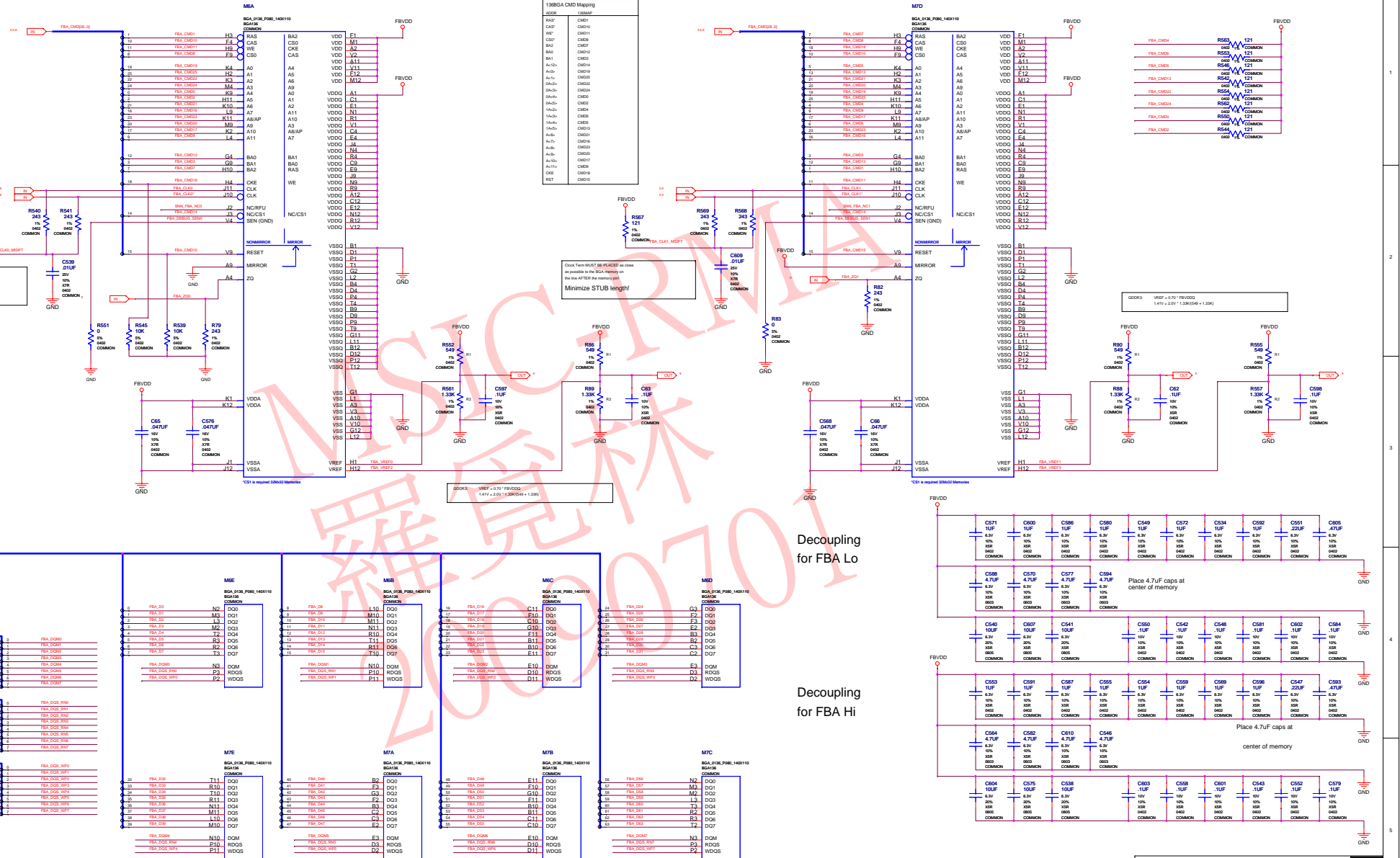


NV_PN	600-10360-base-000 A		
ID		PAGE	
NAME		DATE	22-JAN-2009





1386SA CMD Mapping	
ADDR	1386MAP
RAG*	CMD1
CAS*	CMD10
WE*	CMD11
CSP*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
Arc12p	CMD14
Arc0	CMD18
Arc1s	CMD25
DA-2p	CMD20
DA-0-3p	CMD4
DA-0-4	CMD0
DA-0-5	CMD2
1A-0-2	CMD4
1A-0-3	CMD6
1A-0-4	CMD5
1A-0-5	CMD13
Arc0	CMD21
Arc-7	CMD15
Arc-8	CMD22
Arc-9	CMD26
Arc10	CMD7
Arc11p	CMD9
CHK	CMD18
RST	CMD15



## Decoupling for FBA Lo

Decoupling  
for FBA Hi

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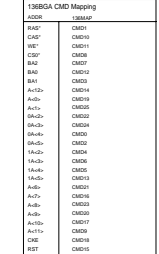


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PAGE DETAIL	FBA Partition

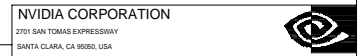
13860A CMD Mapping	
J2000	J1986AP
RAS*	CM01
CAS*	CM10
WE*	CM11
CM0*	CM08
BA2	CM07
BA0	CM12
BA1	CM03
Au-12b	CM14
Au-12c	CM19
Ac-1*	CM05
0A-2*	CM02
0A-3*	CM04
0A-4*	CM03
0A-5*	CM02
1A-2*	CM04
1A-3*	CM06
1A-4*	CM05
1A-5*	CM13
Au-6*	CM21
Ac-7*	CM16
Au-8*	CM22
Ac-9*	CM20
Ac-10*	CM17
Ac-11*	CM09
CNE	CM18
not	CM15



Click Term **MUST BE PLACED** as close as possible to the BGA memory on the line **AFTER** the memory pin!

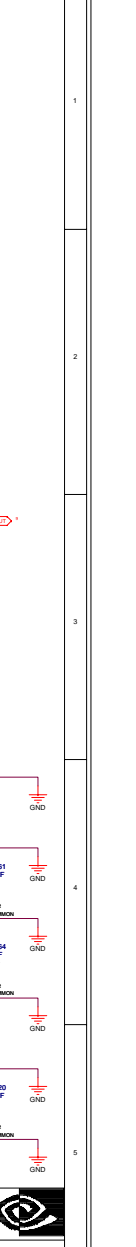
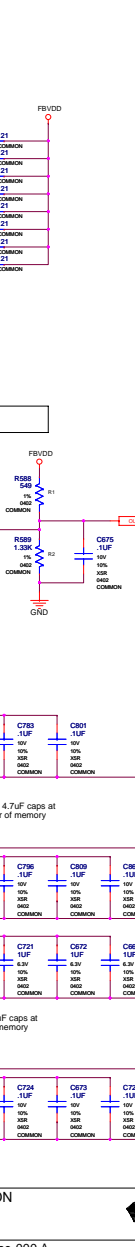
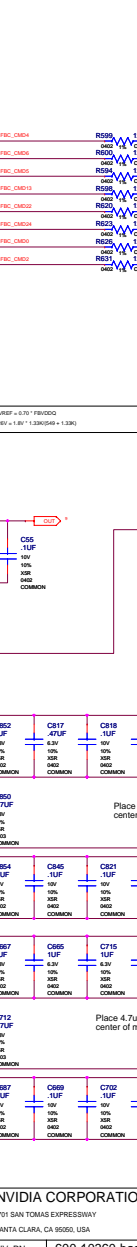
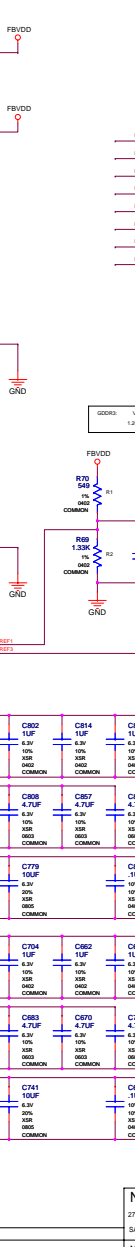
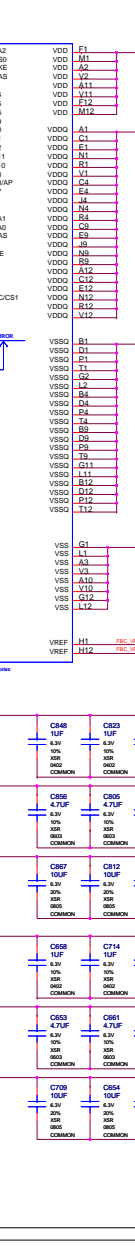
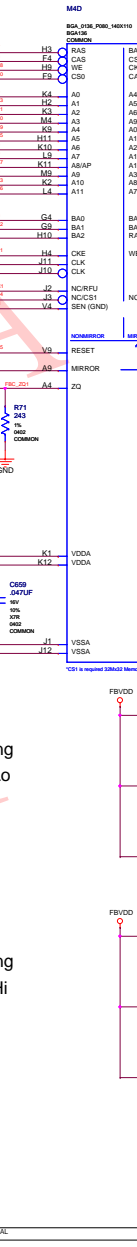
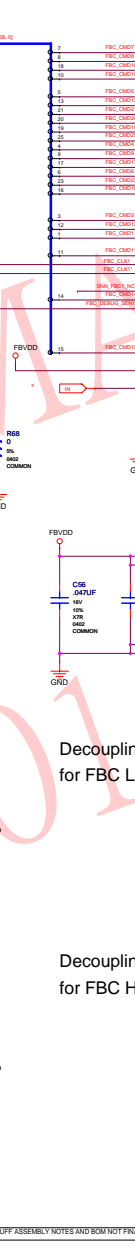
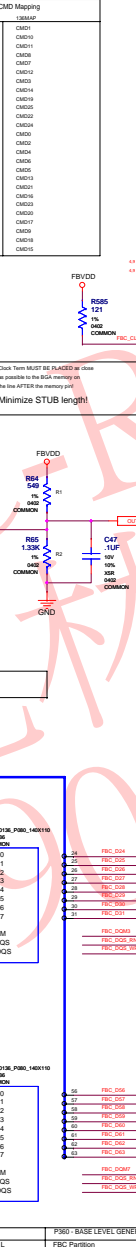
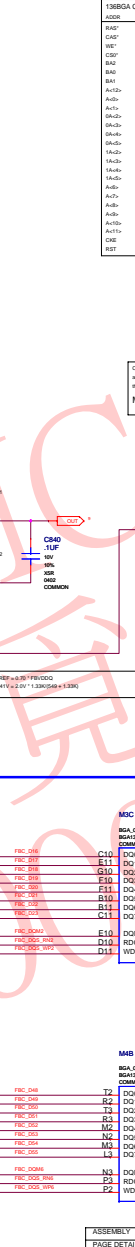
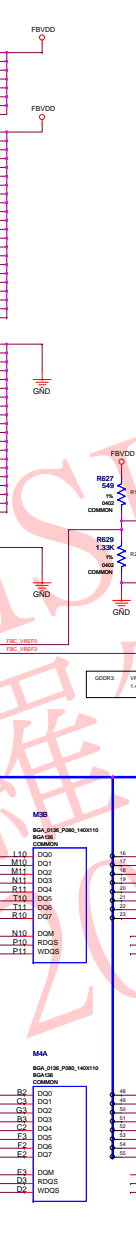
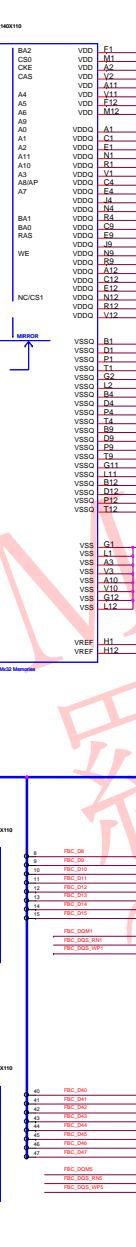
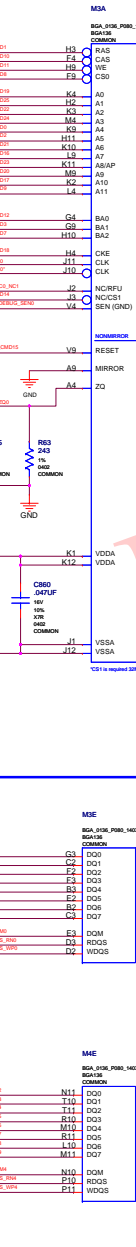
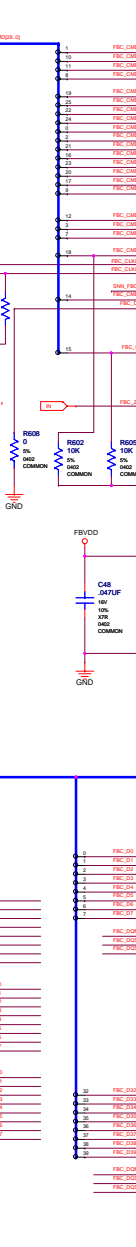
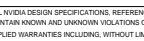
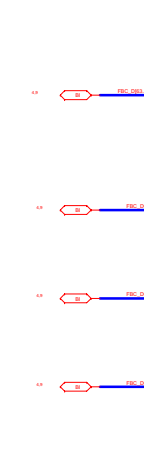
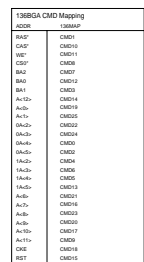
**Minimize STUB length!**

GD03:  $V_{REF} = 0.70 \times FBVDDQ$   
 $1.41V = 2.0V \times 1.33K(549 + 1.33K)$

Decoupling  
for FBB Hi


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1368GA CMD Mapping	
ADDR	1368MAP
BA0	CM01
CAS*	CM02
WE*	CM011
CS0*	CM07
BA2	CM07
BA0	CM012
BA1	CM03
A12a	CM014
A12b	CM019
A11a	CM035
0Aa2	CM022
0Aa3	CM024
0Aa4a	CM00
0Aa5	CM02
1Aa2	CM04
1Aa3	CM06
1Aa4	CM05
1Aa5	CM013
Aa6	CM021
Aa7a	CM016
Aa8	CM023
Aa9	CM020
Ac10	CM017
Ac11a	CM00
CM2	CM018
RST	CM015

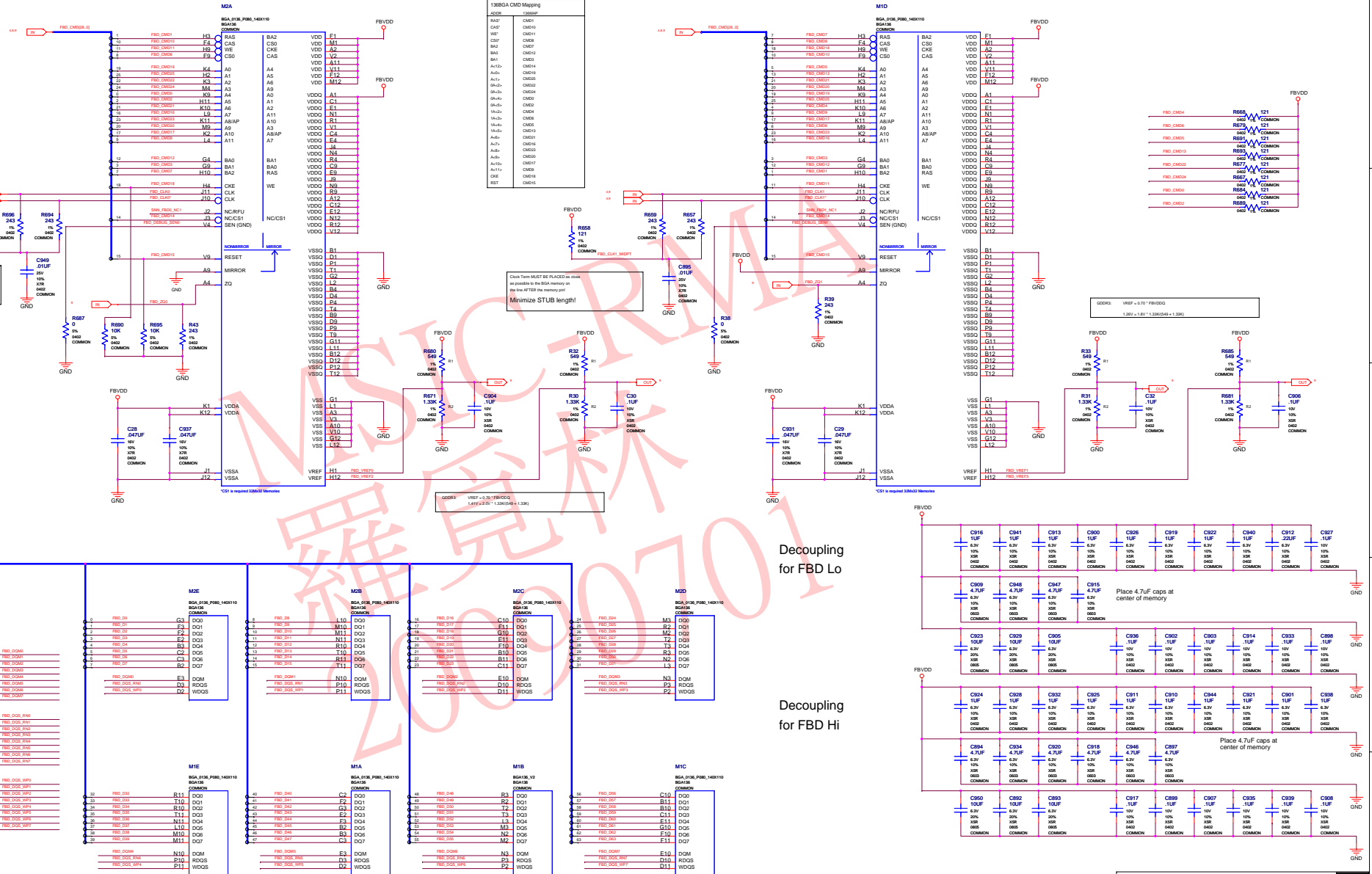


## Decoupling for FRC Li

[illegible]

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<b>NV_PN</b>	600-10360-base-000 A		
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<b>NAME</b>		<b>DATE</b>	22-JAN-2009





## Decoupling for FBD Lo

Decoupling  
for FBD Hi

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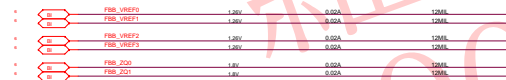
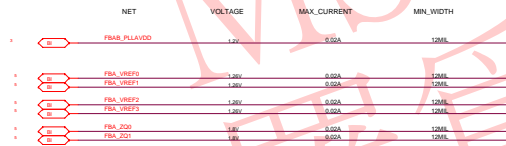
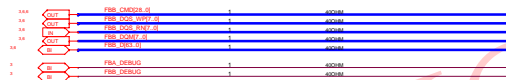
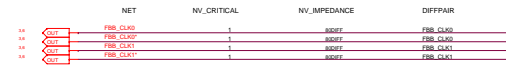
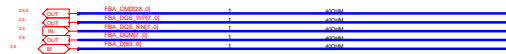
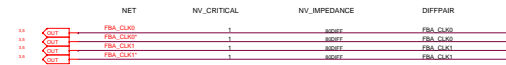
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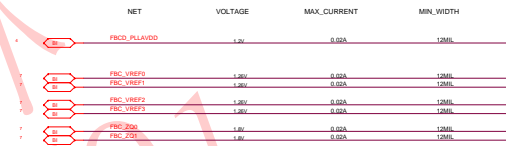
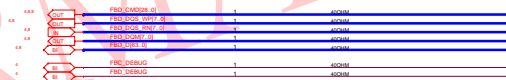
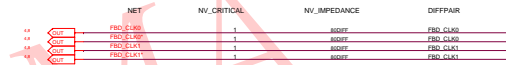
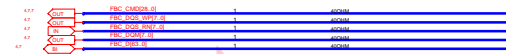
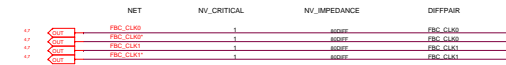
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PAGE DETAIL	FBD Partition

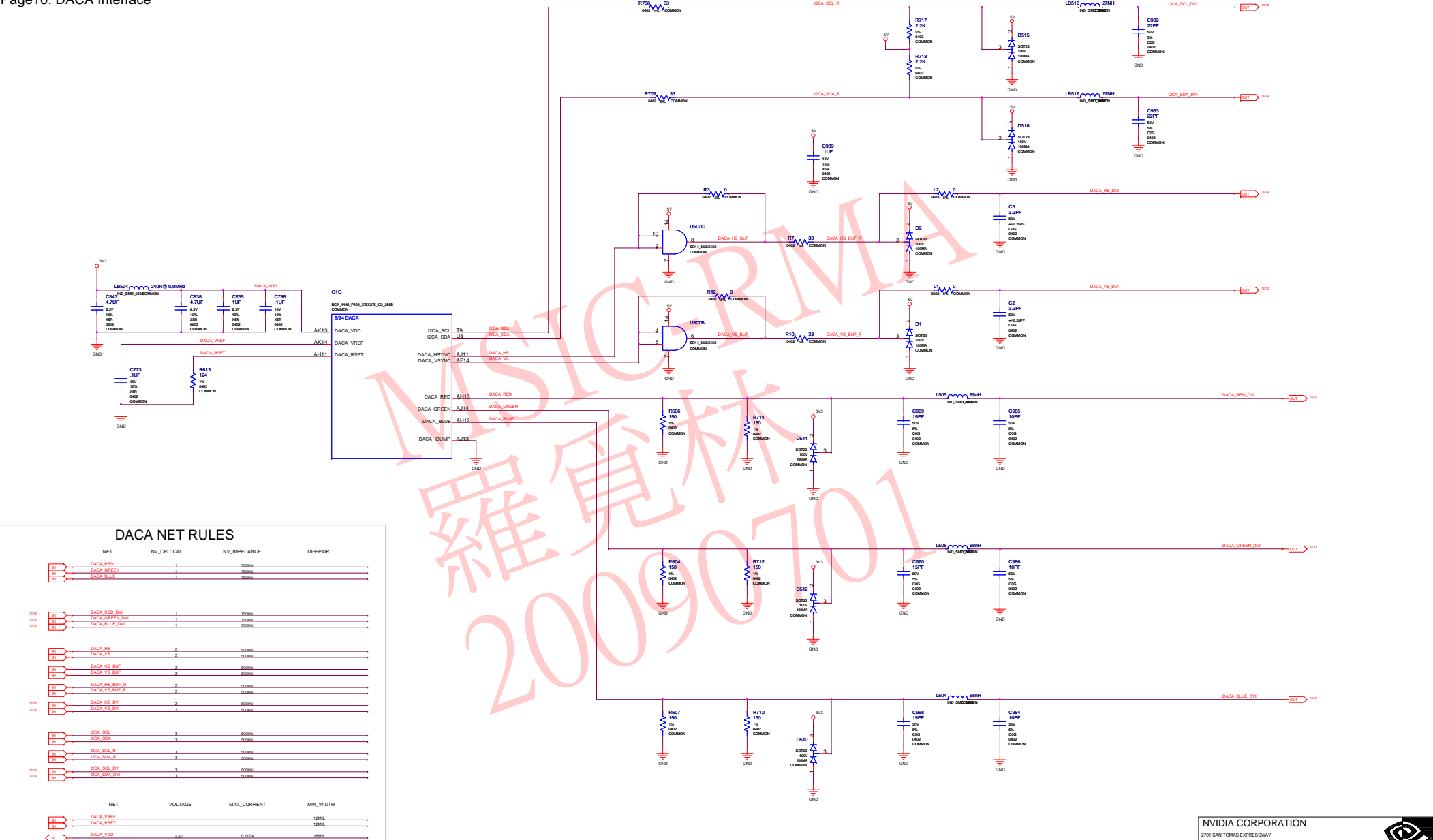


## NET RULES for FrameBuffer A/B



## NET RULES for FrameBuffer C/D





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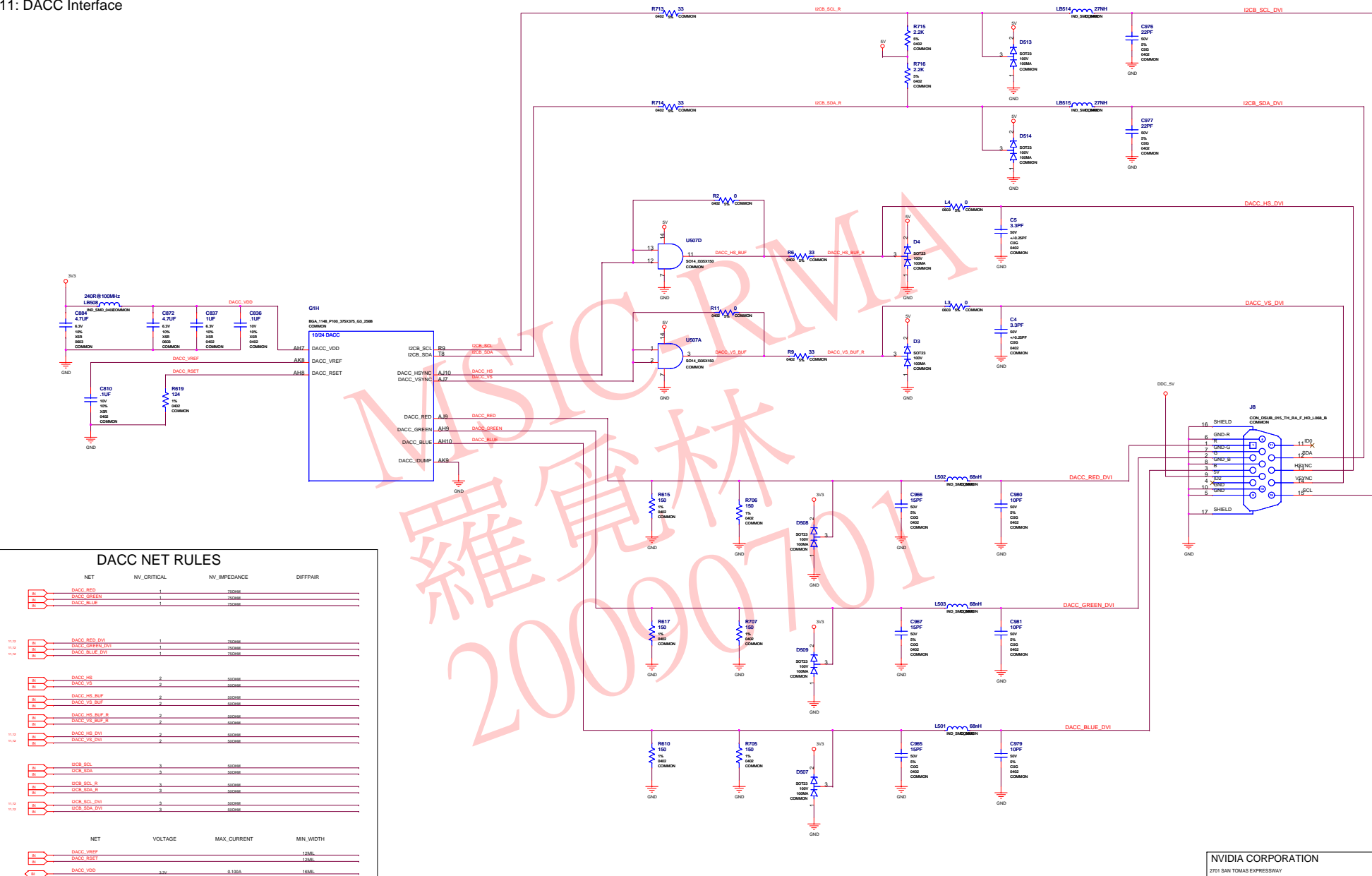
ASSEMBLY P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO 3YUFF ASSEMBLY NOTES AND BOM NOT FINAL  
PAGE DETAIL DACA Interface

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PAGE DETAIL	DACC Interface

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IFPABCD NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RST			12MS
GPIOD_DVAB_HPD_F	3	50OHM	
GPIOD_DVAB_HPD_R	3	50OHM	
IFPAB_PLLVDD	1.8V	0.05A	18MS
IFPAB_VDDIO	1.8V	0.05A	18MS

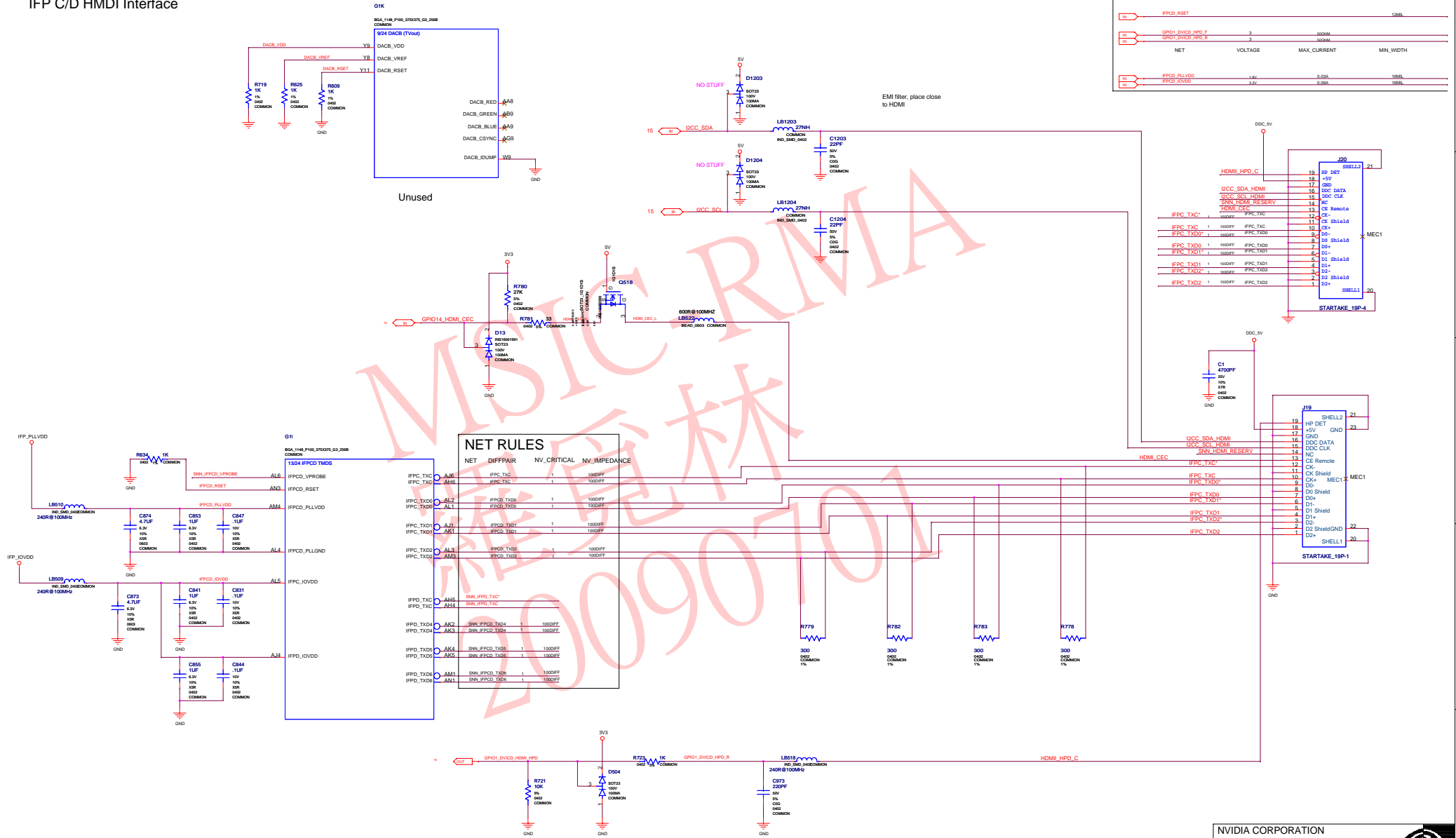
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLLVDD	1.8V	0.05A	18MS
IFPAB_VDDIO	1.8V	0.05A	18MS

NET RULES

NET	DIFFPAIR	NV_CRITICAL	NV_IMPEDANCE
IFPA_TYC	IFPA_TYC	1	100OHM
IFPA_TYC	IFPA_TYC	1	100OHM
IFPA_TXD0	IFPA_TXD0	1	100OHM
IFPA_TXD0	IFPA_TXD0	1	100OHM
IFPA_TXD1	IFPA_TXD1	1	100OHM
IFPA_TXD1	IFPA_TXD1	1	100OHM
IFPA_TXD2	IFPA_TXD2	1	100OHM
IFPA_TXD2	IFPA_TXD2	1	100OHM
IFPA_TXD3	IFPA_TXD3	1	100OHM
IFPA_TXD3	IFPA_TXD3	1	100OHM
IFPA_TXD4	IFPA_TXD4	1	100OHM
IFPA_TXD4	IFPA_TXD4	1	100OHM
IFPA_TXD5	IFPA_TXD5	1	100OHM
IFPA_TXD5	IFPA_TXD5	1	100OHM
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IFPA_TXD6	IFPA_TXD6	1	100OHM
IFPA_TXD7	IFPA_TXD7	1	100OHM
IFPA_TXD7	IFPA_TXD7	1	100OHM
IFPA_TXD8	IFPA_TXD8	1	100OHM
IFPA_TXD8	IFPA_TXD8	1	100OHM
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IFPA_TXD10	IFPA_TXD10	1	100OHM
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IFPA_TXD29	IFPA_TXD29	1	100OHM
IFPA_TXD30	IFPA_TXD30	1	100OHM
IFPA_TXD30	IFPA_TXD30	1	100OHM
IFPA_TXD31	IFPA_TXD31	1	100OHM
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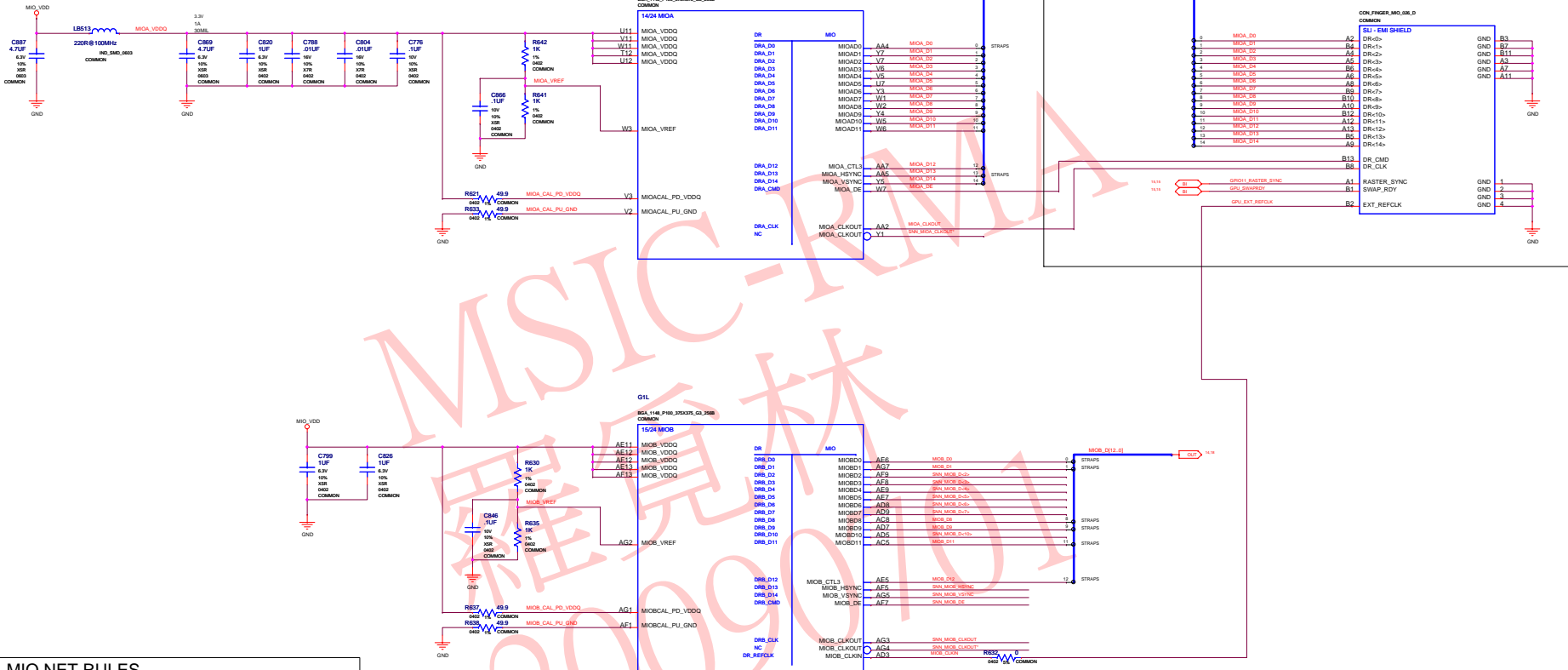
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Page13: DACB Interface Unused  
IFP C/D HDMI Interface



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# MIO Feature Connector

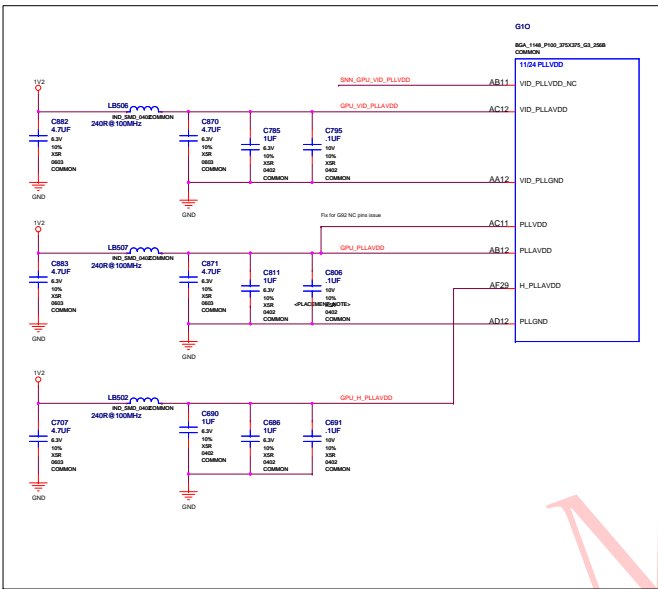


## MIO NET RULES

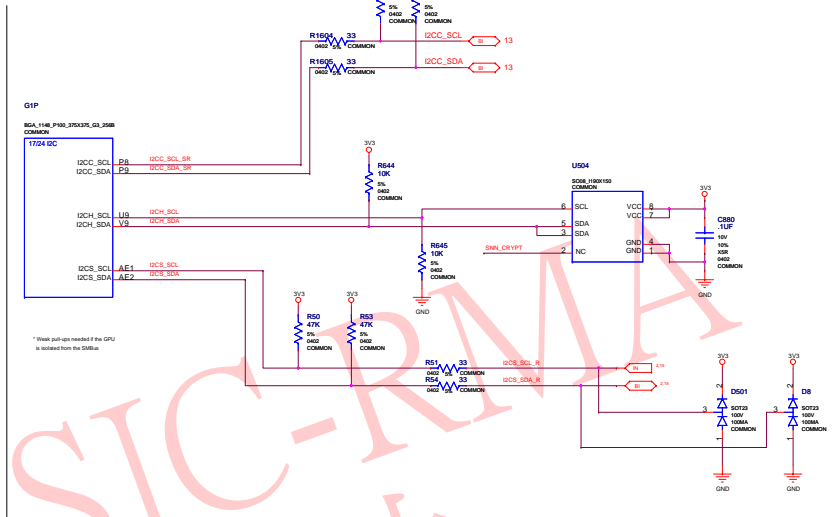
NET	IV_CRITICAL	IV_IMPEDANCE	DIFFPAIR
MIOA_D14_0	1	50OHM	
MIOA_D15_0	1	50OHM	
MIOB_D12_0	1	50OHM	
MIOB_D13_0	1	50OHM	
MIOB_CLKIN	1	50OHM	
GPU_EXT_REFCLK	1	50OHM	
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	1.80V	12MA	12MIL
MIOA_CAL_PD_VDDQ	1.80V	12MA	12MIL
MIOA_CAL_PD_GND	1.80V	12MA	12MIL
MIOB_VREF	1.80V	12MA	12MIL
MIOB_CAL_PD_VDDQ	1.80V	12MA	12MIL
MIOB_CAL_PD_GND	1.80V	12MA	12MIL

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ASSEMBLY P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. 31000 ASSEMBLY NOTES AND BOM NOT FINAL  
PAGE DETAIL Multi-use IOMIO Interface



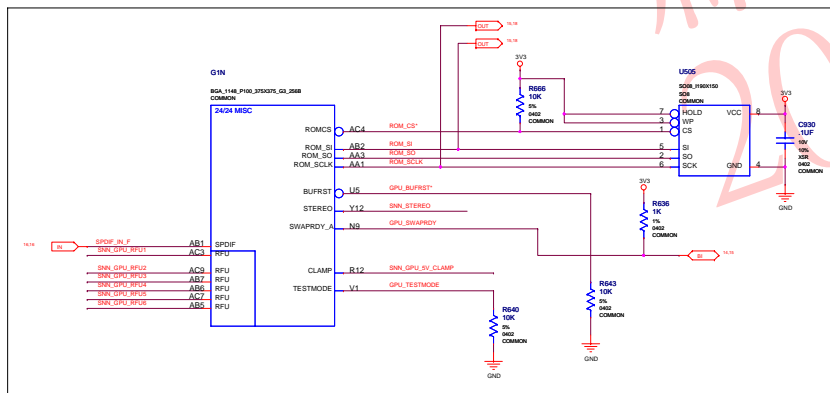
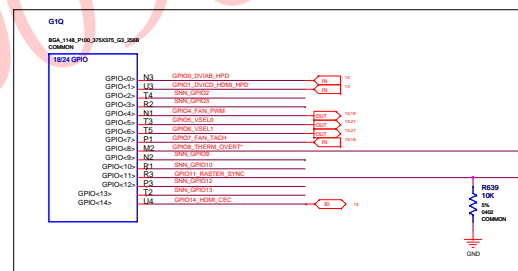
**G1P**



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5	0	0	0
6	0	0	0
7	0	0	0
8	0	0	0
9	0	0	0
10	0	0	0
11	0	0	0
12	0	0	0
13	0	0	0
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98	0	0	0
99	0	0	0
100	0	0	0

15	ODC_SCL	3	500MHz	
16	ODC_SDA	3	500MHz	
17	ODS_SCL	3	500MHz	
18	ODS_SDA	3	500MHz	
19	ODCS_SCL_R	3	500MHz	
20	ODCS_SDA_R	3	500MHz	
21	ROM_C0	3	500MHz	
22	ROM_E	3	500MHz	
23	ROM_E0	3	500MHz	
24	ROM_E0A	3	500MHz	
25				
26	GPU_STREAM0	3	500MHz	
27	GPU_STREAM0R	3	500MHz	
28	GPU0D_DV1_A_HPD	3	500MHz	
29	GPU0D_DV1_C_HPD	3	500MHz	
30				
31	GPU0D_FAN_PWM	3	500MHz	
32	GPU0D_VBEL0	3	500MHz	
33	GPU0D_VBEL1	3	500MHz	
34	GPU0D_FAN_FACH	3	500MHz	
35	GPU0D_THERM_COVERT	3	500MHz	
36				
37	GPU0D_RASTER_SYNC	3	500MHz	
38				
39	XTAL_BGN	1	500MHz	
40	XTAL_EN	1	500MHz	
41	XTAL_OUT0	1	500MHz	
42	XTAL_OUT0BUFF	1	500MHz	
43				
	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
44	GPU_V0_PILL0D	1.2V	0.05A	12MIL
45	GPU_V0_PILL0D0	1.2V	0.05A	12MIL
46	GPU_V0_PILL0D1	1.2V	0.05A	12MIL
47	GPU_V0_PILL0D2	1.2V	0.05A	12MIL
48	GPU_V0_PILL0D3	1.2V	0.05A	12MIL

## (BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)

BCA\_11  
000000[illegible]

GPIO	I/O	Function
0	IN	D01 Hoping Detect South
1	IN	D01 Hoping Detect North
2	N/A	Frameback Interrupt
3	OUT	Fan PWM Output
4	OUT	Voltage Select 0
5	OUT	Voltage Select 1
6	IN	Fan tach Input
7	OUT	THERM_OVERT**
8	N/A	Not used
9	N/A	Not used
10	OUT	RASTER (BL) SYNC
11	N/A	Not used
12	N/A	Not used
13	N/A	Not used
14	IN	GPIO14_JD0M1_CEC

2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA



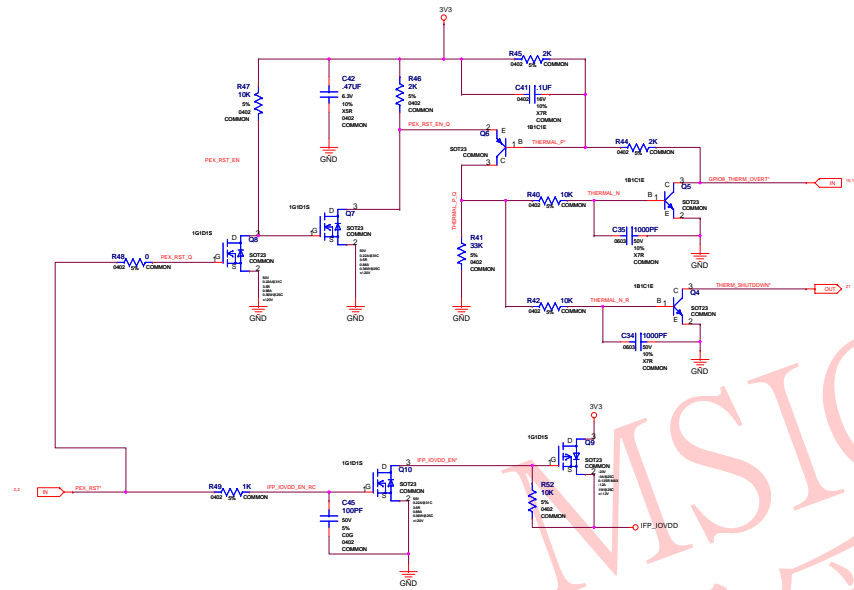
ID		PAGE	
NAME		DATE	22-JAN-2009

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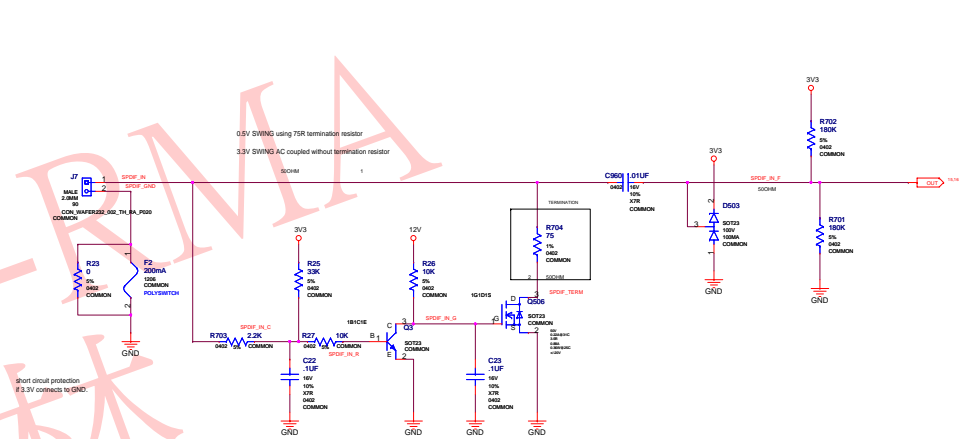
ASSEMBLY	P960 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO, I2C, BIOS, PLL, and XTAL



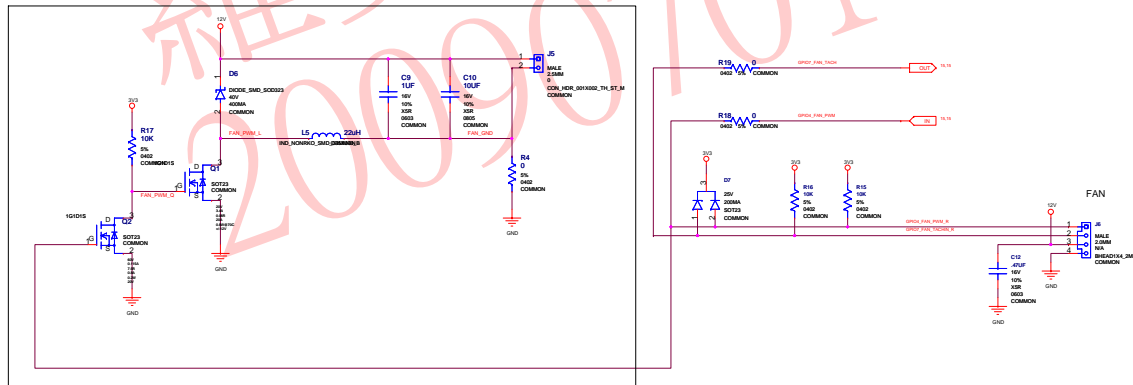
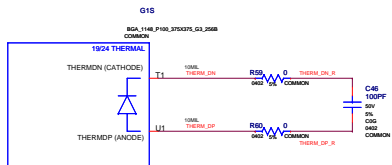
### THERMAL PROTECTION/TMDS BACKDRIVE



### SPDIF INPUT / DETECTION



### THERMAL DIODE



2-pin fan option

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SANTA CLARA, CA 95050, USA



NV\_PN 600-10360-base-000 A

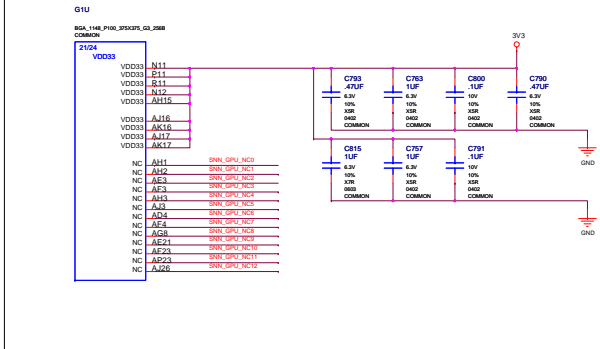
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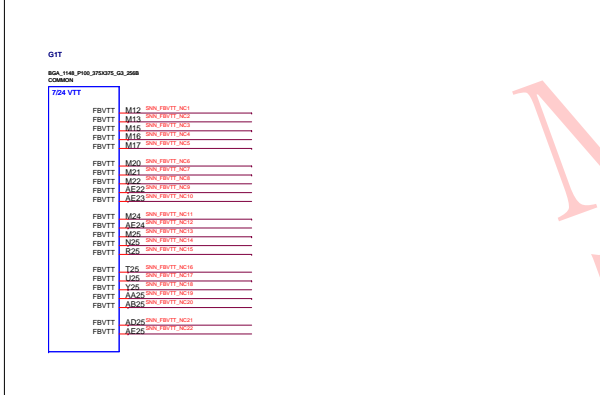
# Page17: Power/GND and Decoupling

NVVD and FBVDD decoupling need final data from SI

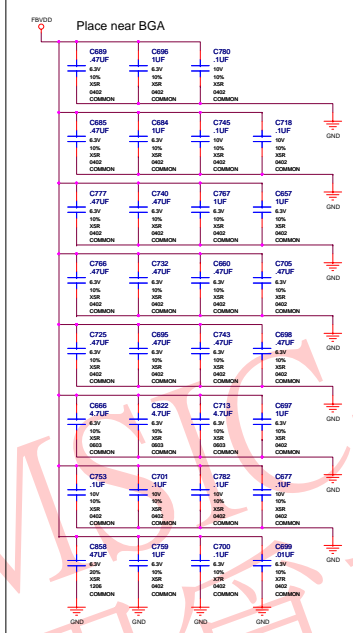
## VDD33



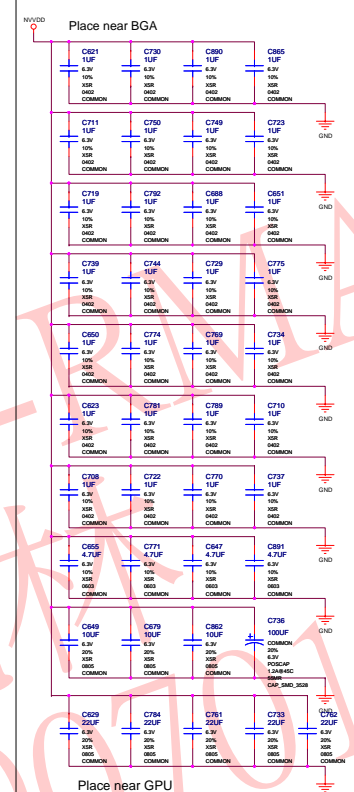
## FBVTT



## FBVDDQ

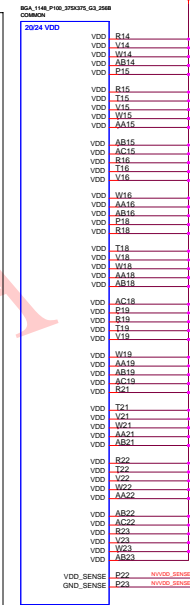


## NVVDD

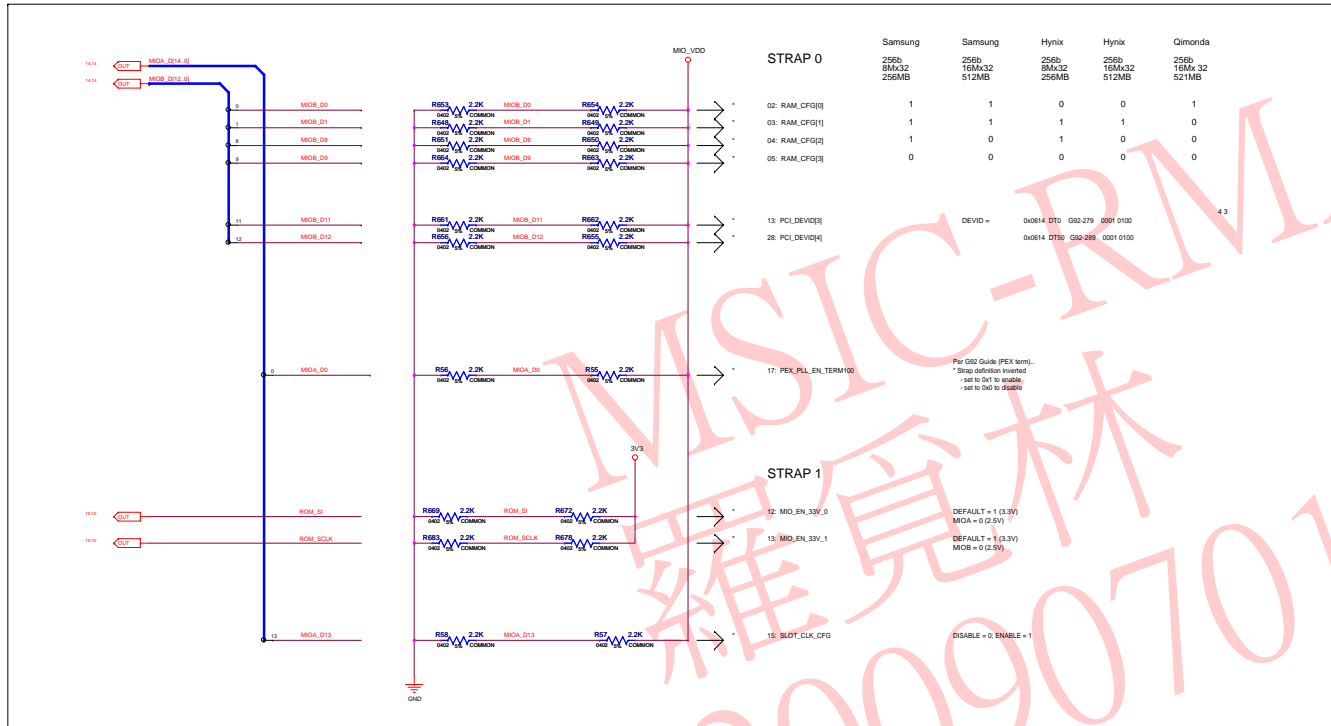


Place near GPU

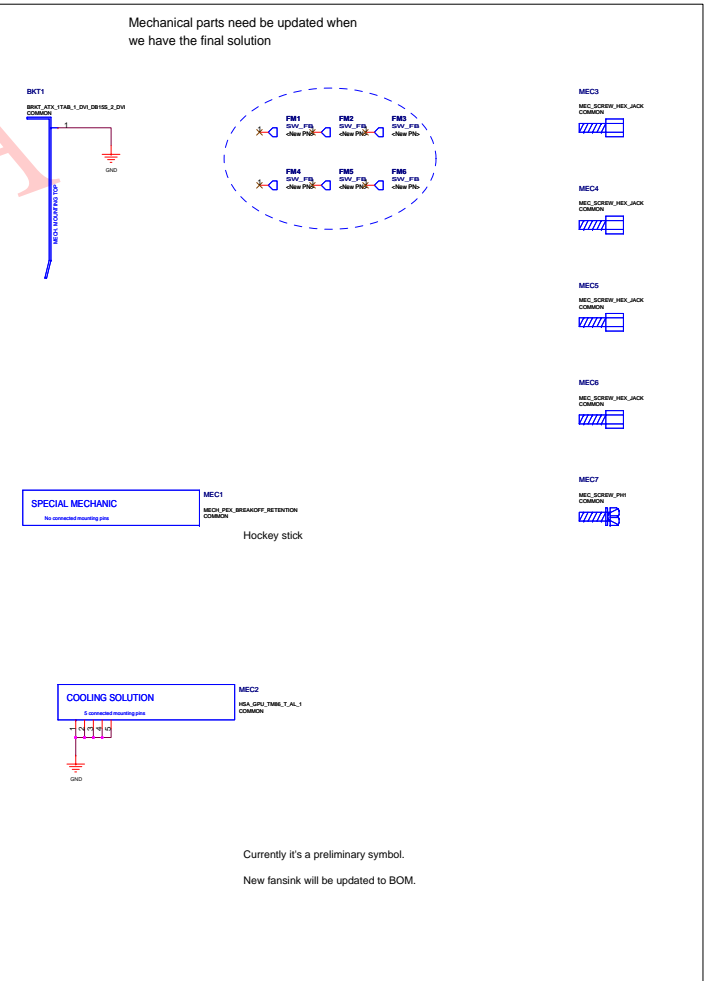
## G1V



## STRAPS



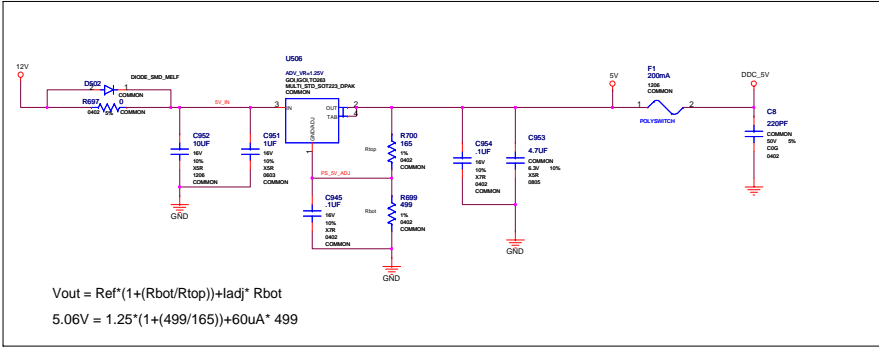
## MECHANICAL



# Page 19:Power Supply:IFP\_PLLVDD,MIO\_VDD,PEX\_PLLVDD Option,DDV\_5V

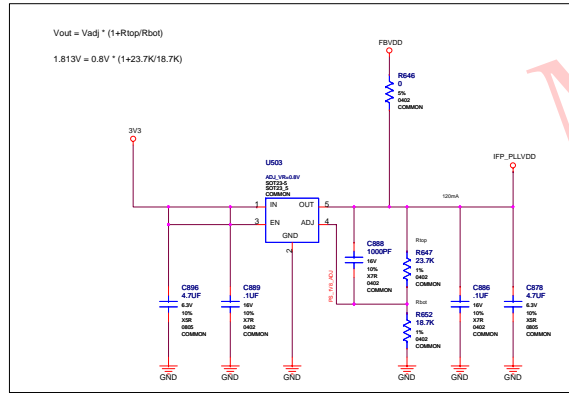
## 5V REGULATOR

## 5V DDC

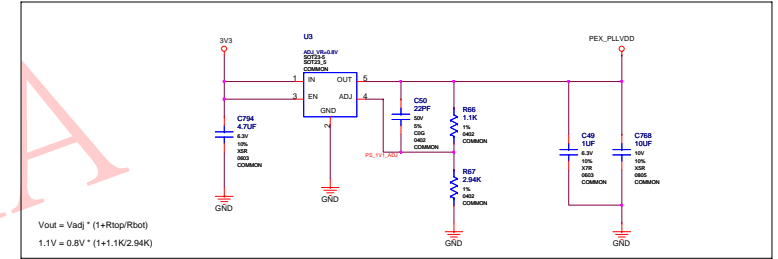
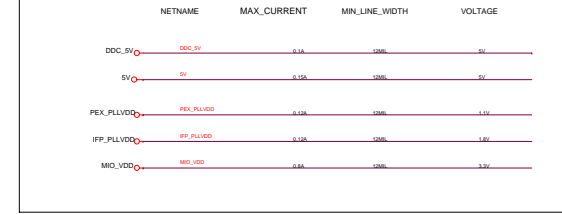


## IFP PLL Supply 1.8V

(Stuff option)

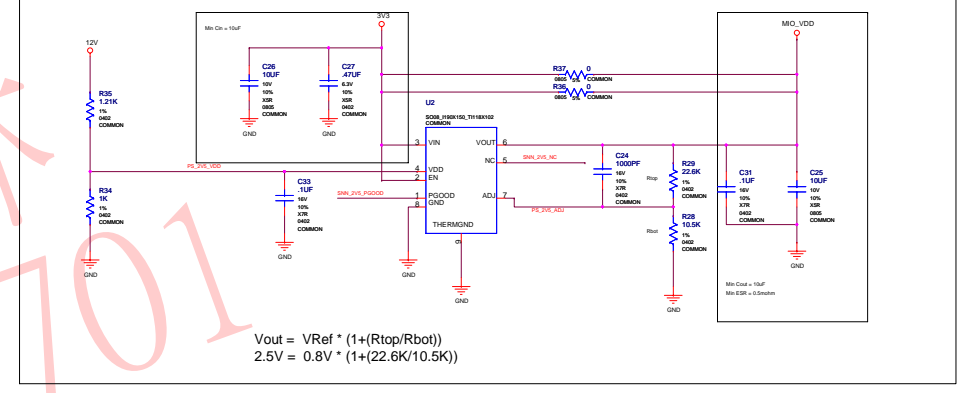




## PEX\_PLLVDD Optional (Stuff option)

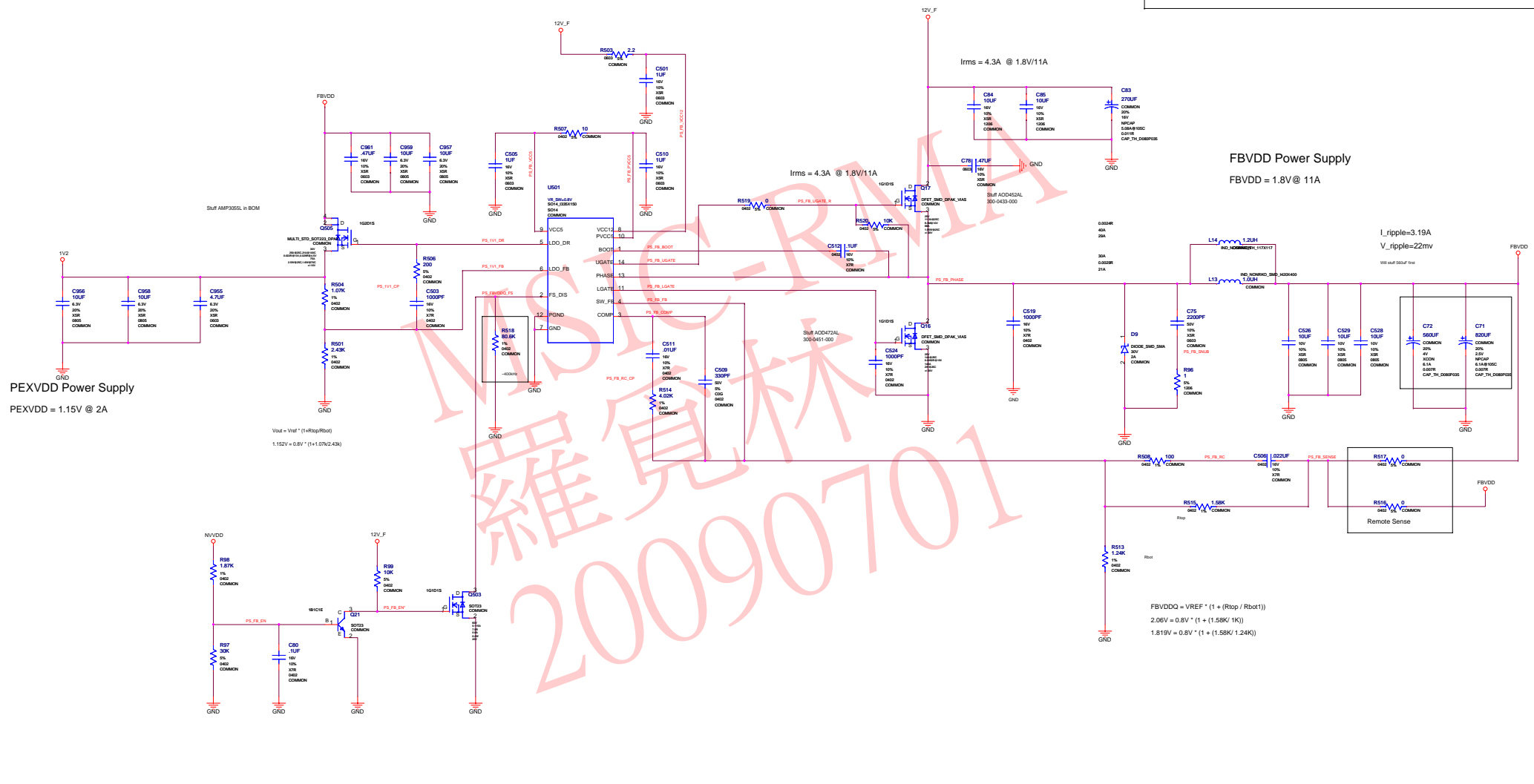



## MIO\_VDD

(Stuff option)



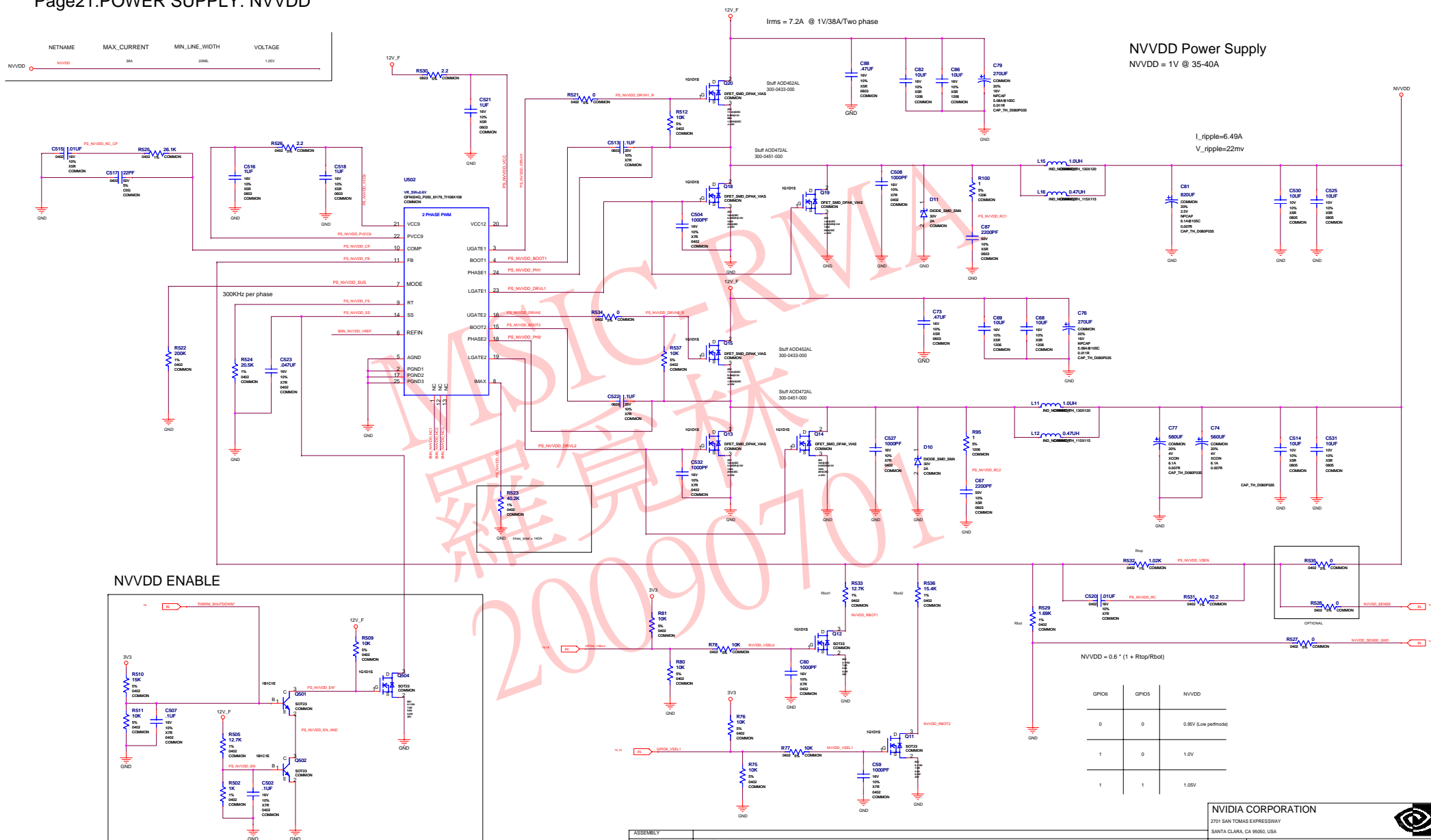
	NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
FBVDD		11A	20MIL	1.8V
1V2		2A	16MIL	1.15V



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## Page21:POWER SUPPLY: NVVDD



GPI06	GPI05	NVDD
0	0	0.95V (Low power)
1	0	1.0V
1	1	1.05V

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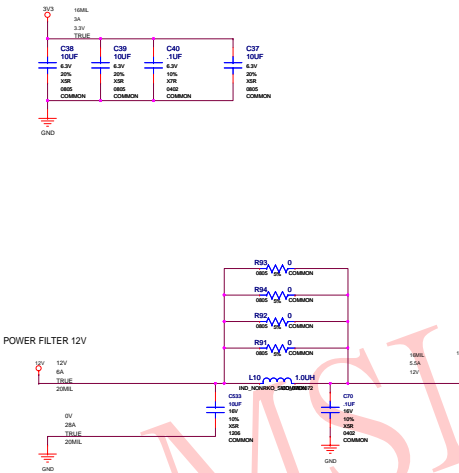
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