

P1041-B01 GF104

GF104-300, 768MB/1536MB, GDDR5 192b 32M/64Mx32  
DVI -I -DL, DVI -I -DL/DP, mHDMI

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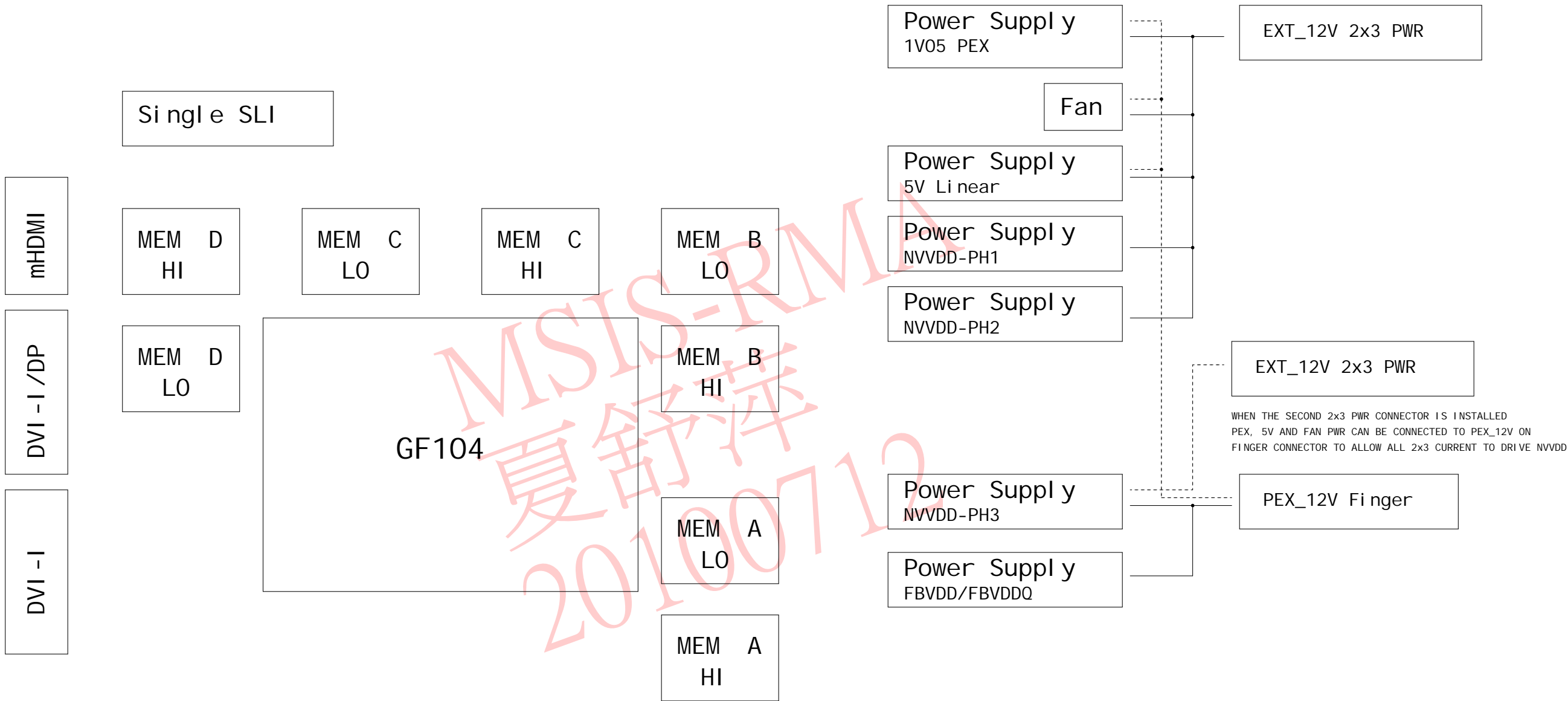
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1	SKU0000	600-11041-0000-300	P1041 GF104-300 768MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
2	SKU0010	600-11041-0010-300	P1041 GF104-350 1024MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
3	QS1	600-11041-0000-QS1	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
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7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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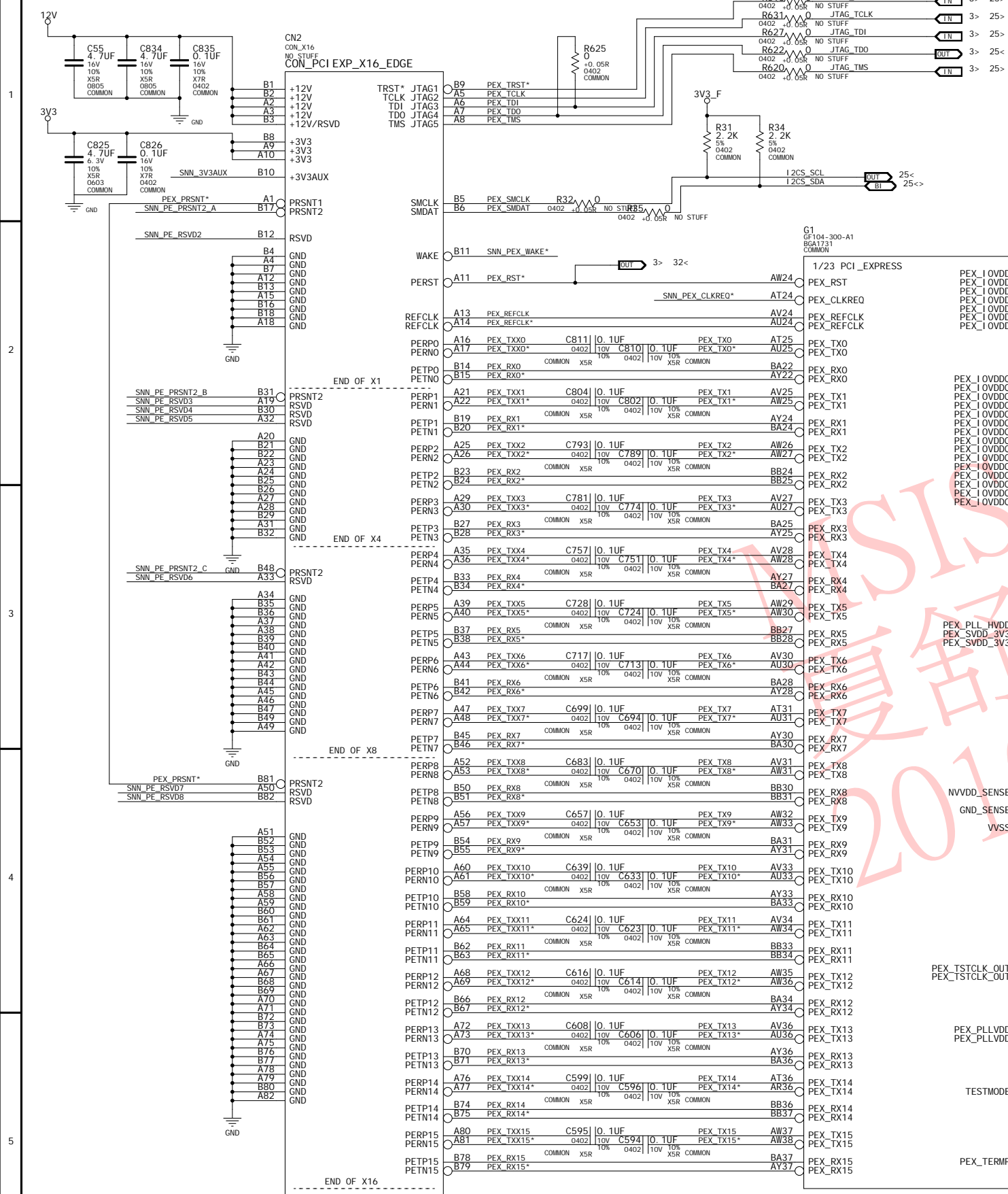
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ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
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Page3: PCI Express



PEX NET RULES

NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
PEX_REFCLK	1	90DI FF	PEX_REFCLK
PEX_REFCLK*	1	90DI FF	PEX_REFCLK
PEX_TX0	1	90DI FF	PEX_TX0
PEX_TX0*	1	90DI FF	PEX_TX0
PEX_TX1	1	90DI FF	PEX_TX1
PEX_TX1*	1	90DI FF	PEX_TX1
PEX_TX2	1	90DI FF	PEX_TX2
PEX_TX2*	1	90DI FF	PEX_TX2
PEX_TX3	1	90DI FF	PEX_TX3
PEX_TX3*	1	90DI FF	PEX_TX3
PEX_TX4	1	90DI FF	PEX_TX4
PEX_TX4*	1	90DI FF	PEX_TX4
PEX_TX5	1	90DI FF	PEX_TX5
PEX_TX5*	1	90DI FF	PEX_TX5
PEX_TX6	1	90DI FF	PEX_TX6
PEX_TX6*	1	90DI FF	PEX_TX6
PEX_TX7	1	90DI FF	PEX_TX7
PEX_TX7*	1	90DI FF	PEX_TX7
PEX_TX8	1	90DI FF	PEX_TX8
PEX_TX8*	1	90DI FF	PEX_TX8
PEX_TX9	1	90DI FF	PEX_TX9
PEX_TX9*	1	90DI FF	PEX_TX9
PEX_TX10	1	90DI FF	PEX_TX10
PEX_TX10*	1	90DI FF	PEX_TX10
PEX_TX11	1	90DI FF	PEX_TX11
PEX_TX11*	1	90DI FF	PEX_TX11
PEX_TX12	1	90DI FF	PEX_TX12
PEX_TX12*	1	90DI FF	PEX_TX12
PEX_TX13	1	90DI FF	PEX_TX13
PEX_TX13*	1	90DI FF	PEX_TX13
PEX_TX14	1	90DI FF	PEX_TX14
PEX_TX14*	1	90DI FF	PEX_TX14
PEX_TX15	1	90DI FF	PEX_TX15
PEX_TX15*	1	90DI FF	PEX_TX15
PEX_RX0	1	90DI FF	PEX_RX0
PEX_RX0*	1	90DI FF	PEX_RX0
PEX_RX1	1	90DI FF	PEX_RX1
PEX_RX1*	1	90DI FF	PEX_RX1
PEX_RX2	1	90DI FF	PEX_RX2
PEX_RX2*	1	90DI FF	PEX_RX2
PEX_RX3	1	90DI FF	PEX_RX3
PEX_RX3*	1	90DI FF	PEX_RX3
PEX_RX4	1	90DI FF	PEX_RX4
PEX_RX4*	1	90DI FF	PEX_RX4
PEX_RX5	1	90DI FF	PEX_RX5
PEX_RX5*	1	90DI FF	PEX_RX5
PEX_RX6	1	90DI FF	PEX_RX6
PEX_RX6*	1	90DI FF	PEX_RX6
PEX_RX7	1	90DI FF	PEX_RX7
PEX_RX7*	1	90DI FF	PEX_RX7
PEX_RX8	1	90DI FF	PEX_RX8
PEX_RX8*	1	90DI FF	PEX_RX8
PEX_RX9	1	90DI FF	PEX_RX9
PEX_RX9*	1	90DI FF	PEX_RX9
PEX_RX10	1	90DI FF	PEX_RX10
PEX_RX10*	1	90DI FF	PEX_RX10
PEX_RX11	1	90DI FF	PEX_RX11
PEX_RX11*	1	90DI FF	PEX_RX11
PEX_RX12	1	90DI FF	PEX_RX12
PEX_RX12*	1	90DI FF	PEX_RX12
PEX_RX13	1	90DI FF	PEX_RX13
PEX_RX13*	1	90DI FF	PEX_RX13
PEX_RX14	1	90DI FF	PEX_RX14
PEX_RX14*	1	90DI FF	PEX_RX14
PEX_RX15	1	90DI FF	PEX_RX15
PEX_RX15*	1	90DI FF	PEX_RX15
PEX_TX0	1	90DI FF	PEX_TX0
PEX_TX0*	1	90DI FF	PEX_TX0
PEX_TX1	1	90DI FF	PEX_TX1
PEX_TX1*	1	90DI FF	PEX_TX1
PEX_TX2	1	90DI FF	PEX_TX2
PEX_TX2*	1	90DI FF	PEX_TX2
PEX_TX3	1	90DI FF	PEX_TX3
PEX_TX3*	1	90DI FF	PEX_TX3
PEX_TX4	1	90DI FF	PEX_TX4
PEX_TX4*	1	90DI FF	PEX_TX4
PEX_TX5	1	90DI FF	PEX_TX5
PEX_TX5*	1	90DI FF	PEX_TX5
PEX_TX6	1	90DI FF	PEX_TX6
PEX_TX6*	1	90DI FF	PEX_TX6
PEX_TX7	1	90DI FF	PEX_TX7
PEX_TX7*	1	90DI FF	PEX_TX7
PEX_TX8	1	90DI FF	PEX_TX8
PEX_TX8*	1	90DI FF	PEX_TX8
PEX_TX9	1	90DI FF	PEX_TX9
PEX_TX9*	1	90DI FF	PEX_TX9
PEX_TX10	1	90DI FF	PEX_TX10
PEX_TX10*	1	90DI FF	PEX_TX10
PEX_TX11	1	90DI FF	PEX_TX11
PEX_TX11*	1	90DI FF	PEX_TX11
PEX_TX12	1	90DI FF	PEX_TX12
PEX_TX12*	1	90DI FF	PEX_TX12
PEX_TX13	1	90DI FF	PEX_TX13
PEX_TX13*	1	90DI FF	PEX_TX13
PEX_TX14	1	90DI FF	PEX_TX14
PEX_TX14*	1	90DI FF	PEX_TX14
PEX_TX15	1	90DI FF	PEX_TX15
PEX_TX15*	1	90DI FF	PEX_TX15
PEX_PLL_CLK_OUT	1	90DI FF	PEX_PLL_CLK_OUT
PEX_PLL_CLK_OUT*	1	90DI FF	PEX_PLL_CLK_OUT
PEX_RST*	1	50OHM	PEX_RST*
PEX_TRST*	1	50OHM	PEX_TRST*
PEX_TCLK	1	50OHM	PEX_TCLK
PEX_TDI	1	50OHM	PEX_TDI
PEX_TDO	1	50OHM	PEX_TDO
PEX_TMS	1	50OHM	PEX_TMS
JTAG_TCLK	1	50OHM	JTAG_TCLK
JTAG_TMS	1	50OHM	JTAG_TMS
JTAG_TDI	1	50OHM	JTAG_TDI
JTAG_TDO	1	50OHM	JTAG_TDO
JTAG_TRST*	1	50OHM	JTAG_TRST*
NET	VOLTAGE	MAX_CURRENT	MI_N_WI DTH
12V	12V	5.5A	24MI L
3V3	3V3	3.0A	20MI L
GND	GND	8.5A	16MI L
PEX_PLLVDD	1.05V	0.16A	12MI L

ASSEMBLY P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI  
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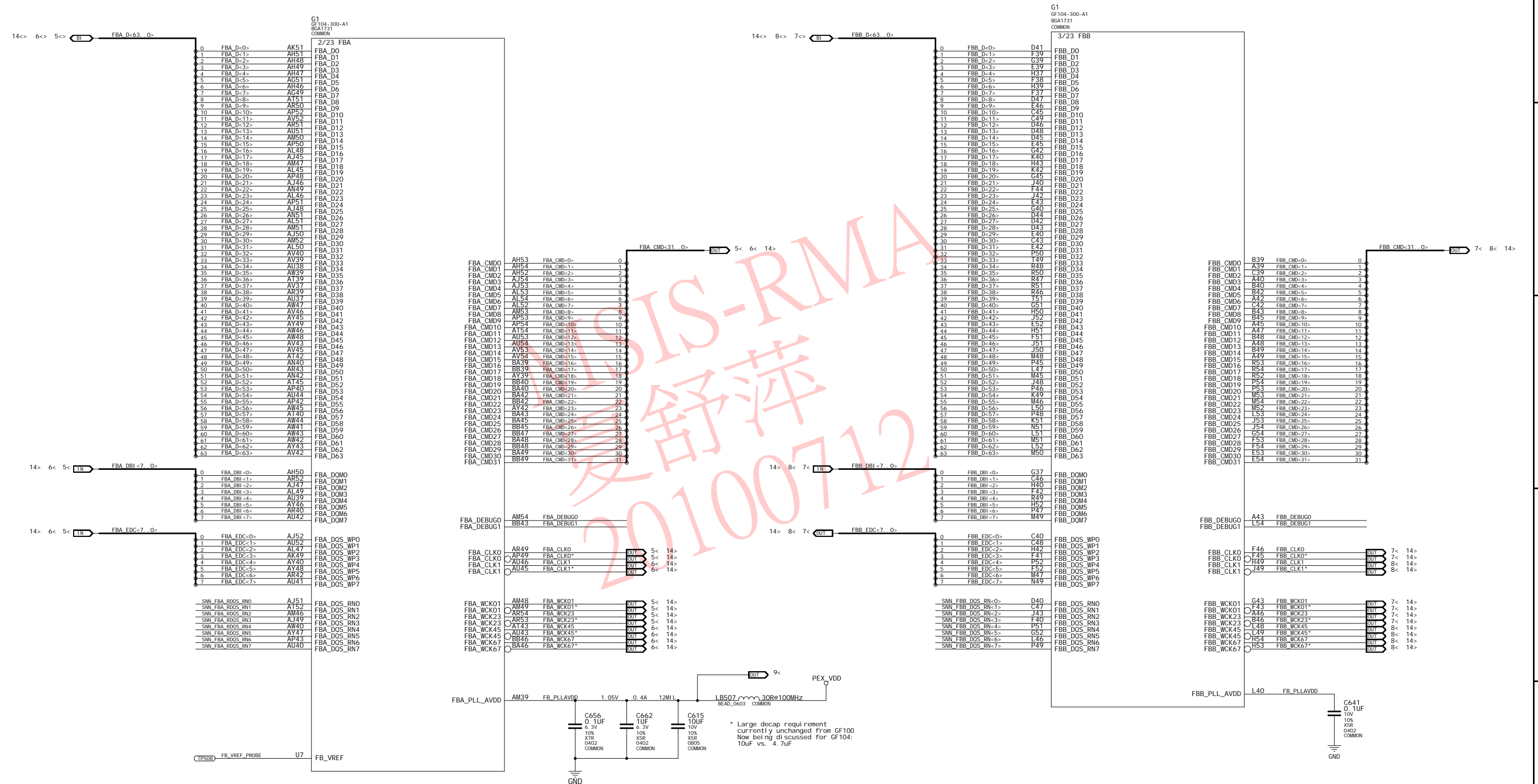
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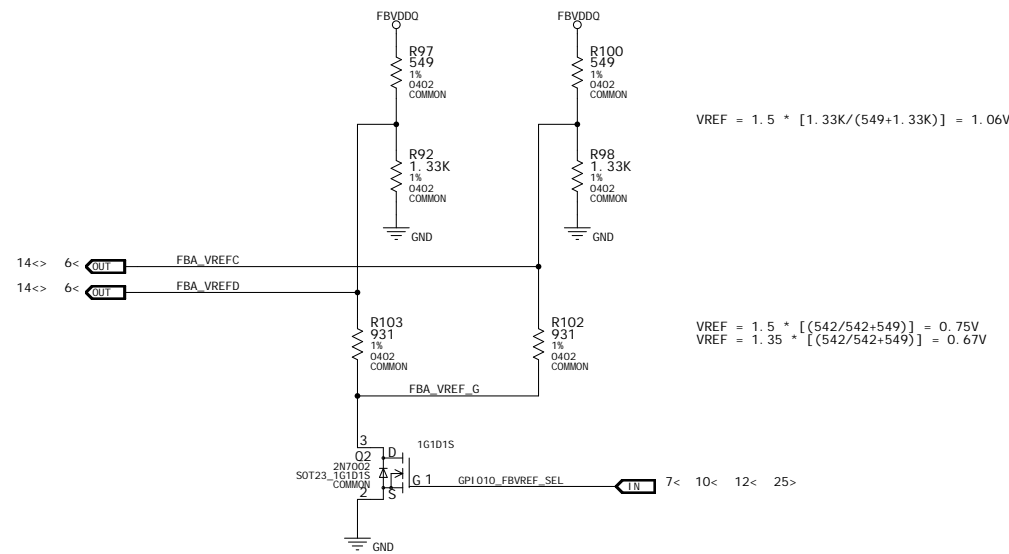
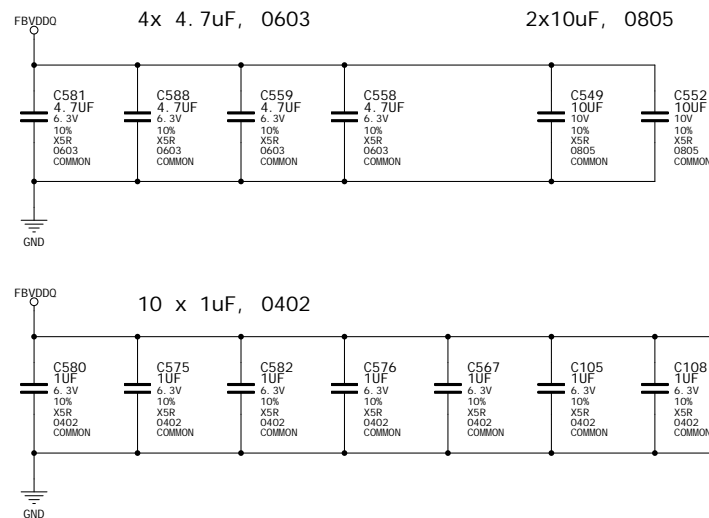
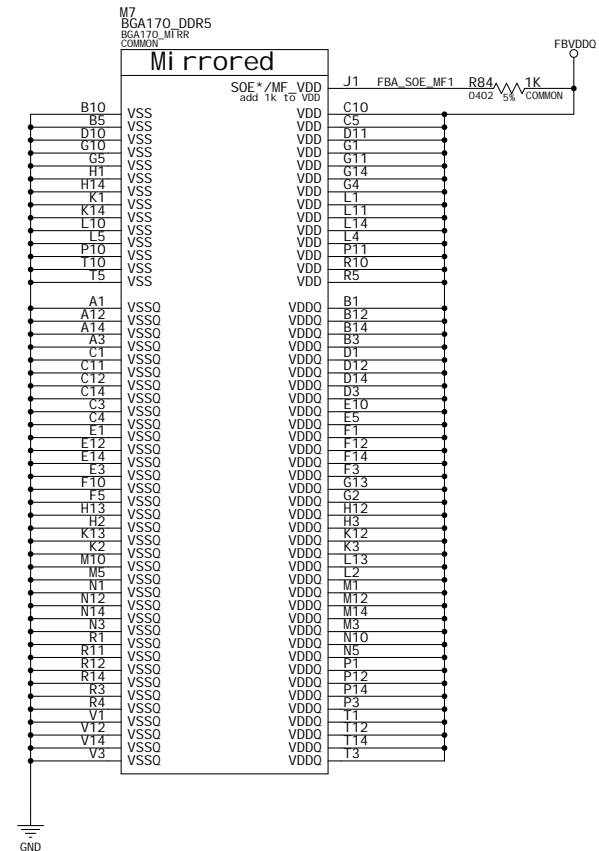
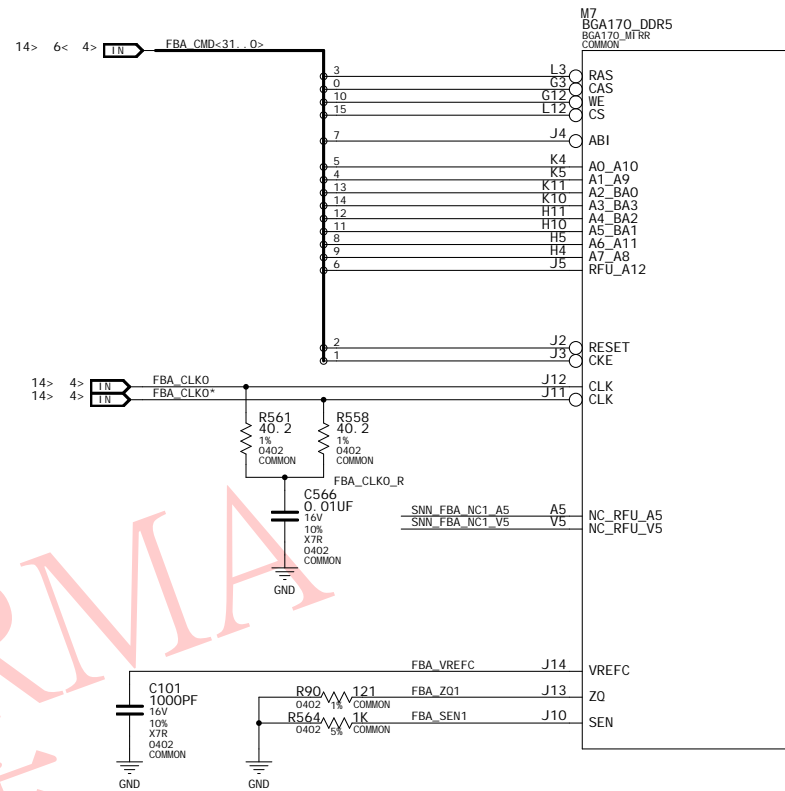
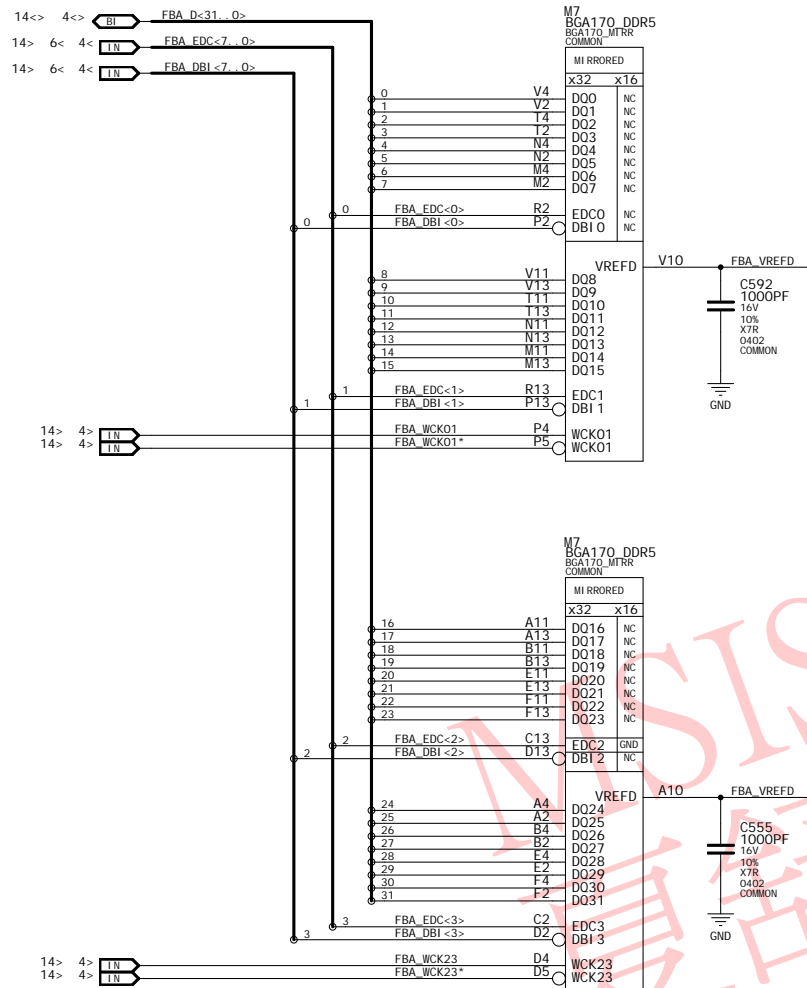



GDdR5	CMD	Mappi ng
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	AB1*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		AB1*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

```

** Vref swi tching options:
- internal Vref should be POR for VrefD
- potential for update

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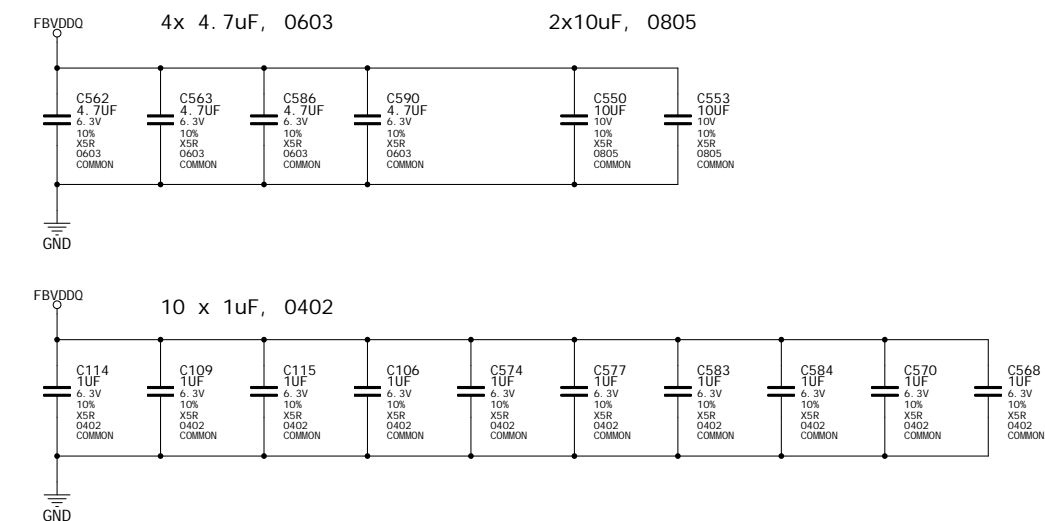
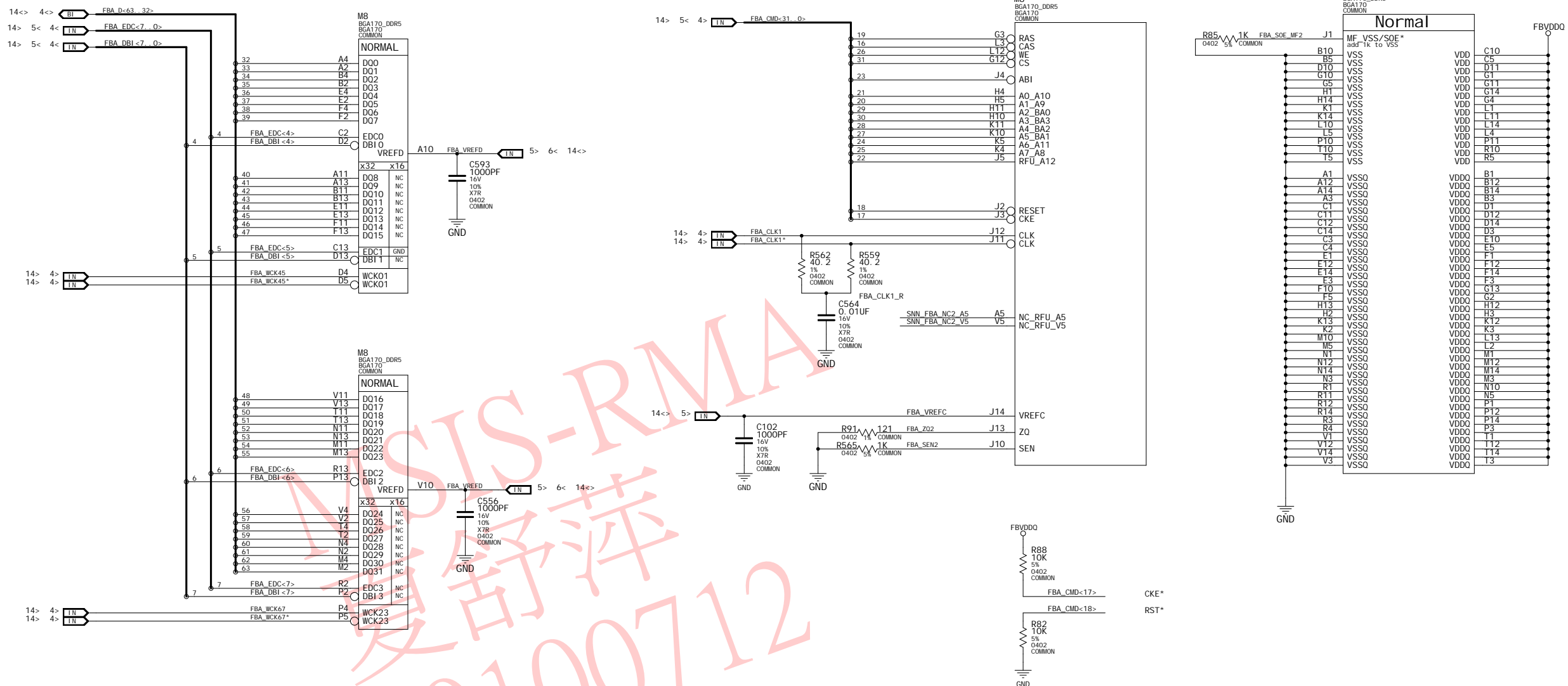
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GDDR5 CMD Mapping		
CMD	0 ... 31	32 ... 63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	AB1 *	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_A6	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		AB1 *
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_A6
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

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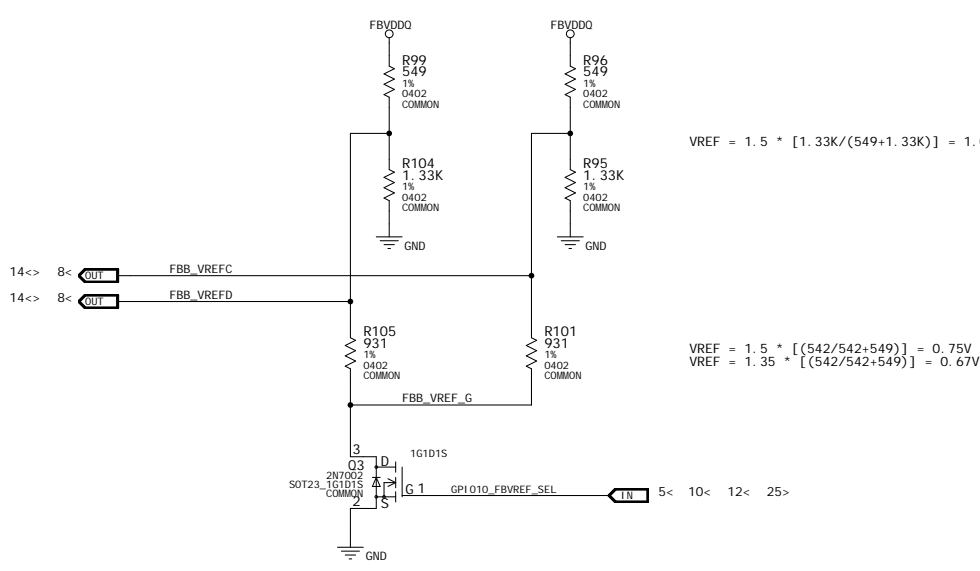
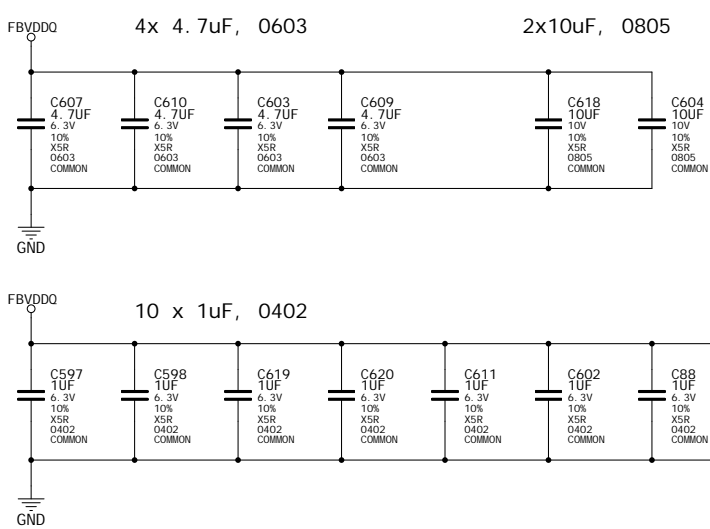
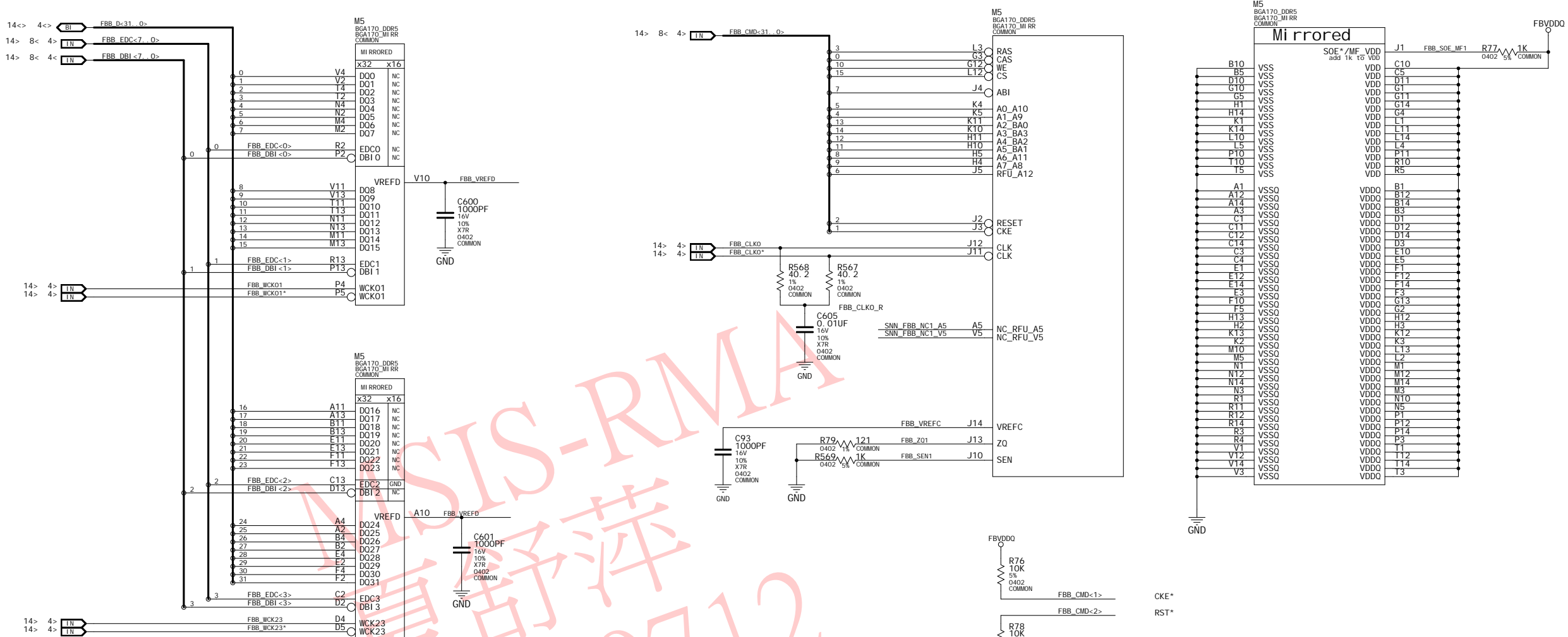
** Vref swi tching options:
- internal Vref should be POR for VrefD
- potential for update

```



GDDR5 CMD Mapping			
CMD	0..31	32..63	
CMD0	CAS*		
CMD1	CKE*		
CMD2	RST*		
CMD3	RAS*		
CMD4	A1_A9		
CMD5	A0_A10		
CMD6	A12_RFU		
CMD7	AB1*		
CMD8	A6_A11		
CMD9	A7_A8		
CMD10	WE*		
CMD11	A5_BA1		
CMD12	A4_BA2		
CMD13	A2_BA0		
CMD14	A3_BA3		
CMD15	CS*		
CMD16	CAS*		
CMD17	CKE*		
CMD18	RST*		
CMD19	RAS*		
CMD20	A1_A9		
CMD21	A0_A10		
CMD22	A12_RFU		
CMD23	AB1*		
CMD24	A6_A11		
CMD25	A7_A8		
CMD26	WE*		
CMD27	A5_BA1		
CMD28	A4_BA2		
CMD29	A2_BA0		
CMD30	A3_BA3		
CMD31	CS*		

\*\* Vref switching options:  
- internal Vref should be POR for VrefD  
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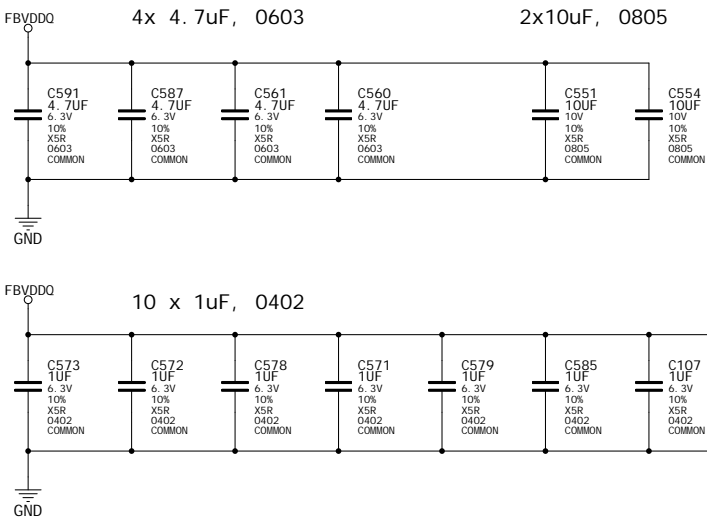
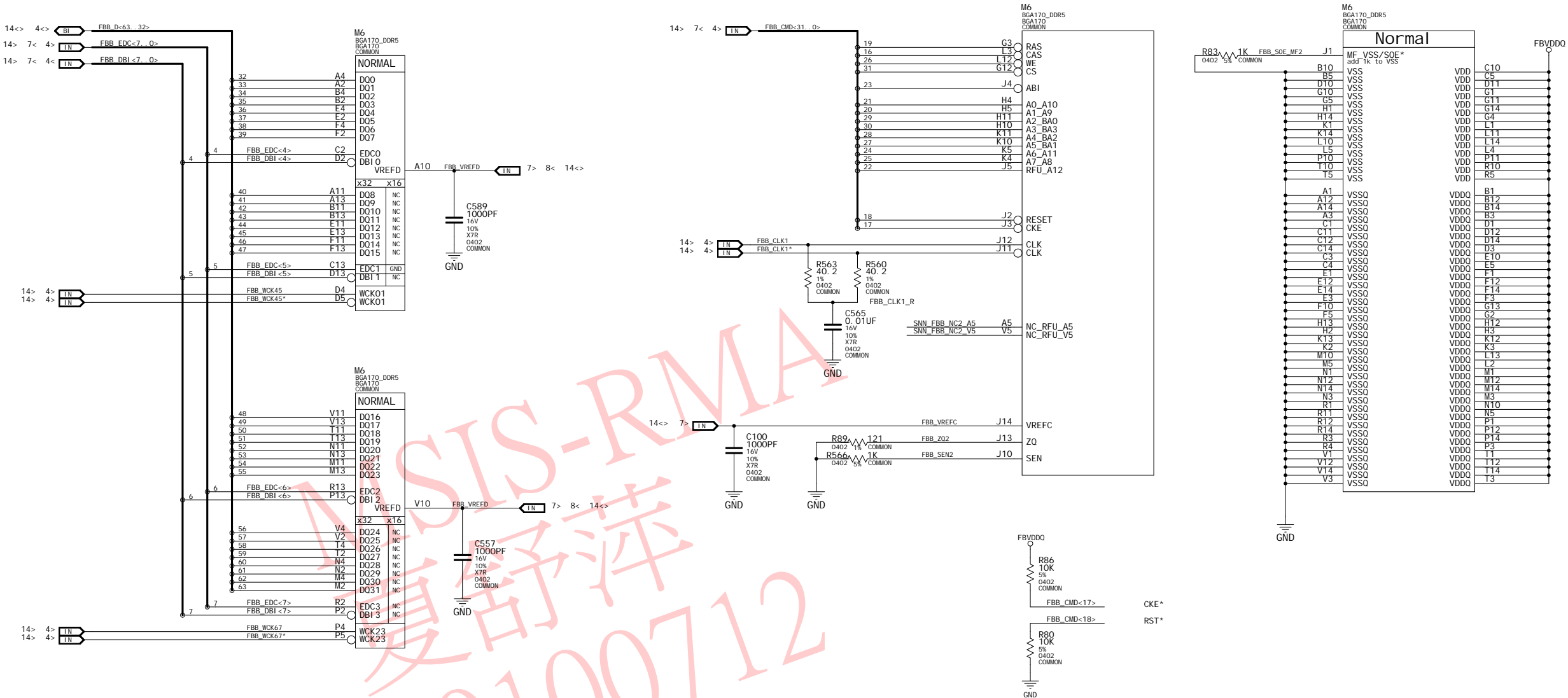
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$$VREF = 1.5 * [(542 / 542 + 549)] = 0.75V$$
  
$$VREF = 1.35 * [(542 / 542 + 549)] = 0.67V$$

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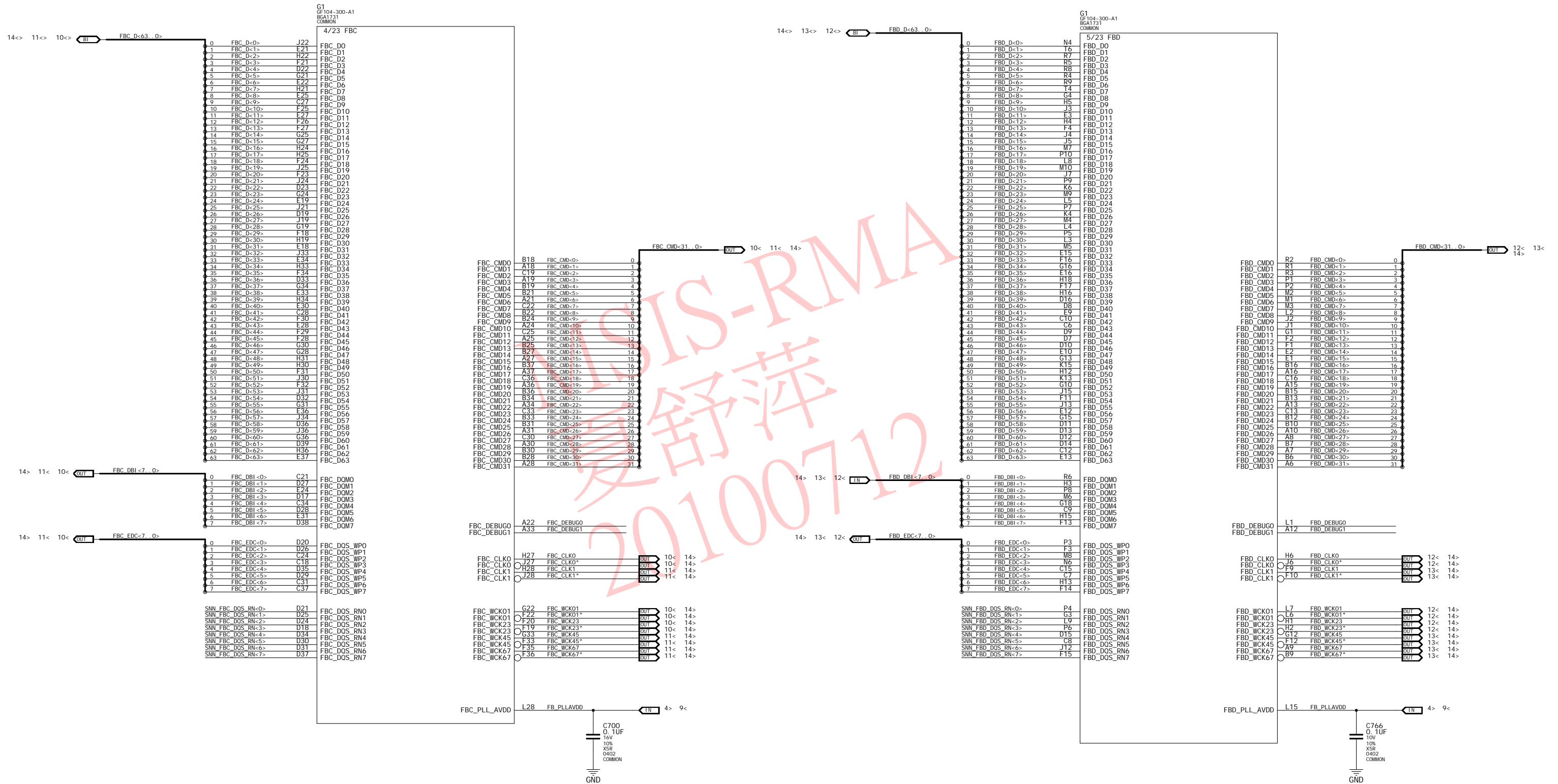
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GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RA*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	AB1*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16	CAS*	
CMD17	CKE*	
CMD18	RST*	
CMD19	RA*	
CMD20	A1_A9	
CMD21	A0_A10	
CMD22	A12_RFU	
CMD23	AB1*	
CMD24	A6_A11	
CMD25	A7_A8	
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CMD28	A4_BA2	
CMD29	A2_BA0	
CMD30	A3_BA3	
CMD31	CS*	

\*\* Vref' swi tching options:  
- internal Vref should be POR for VrefD  
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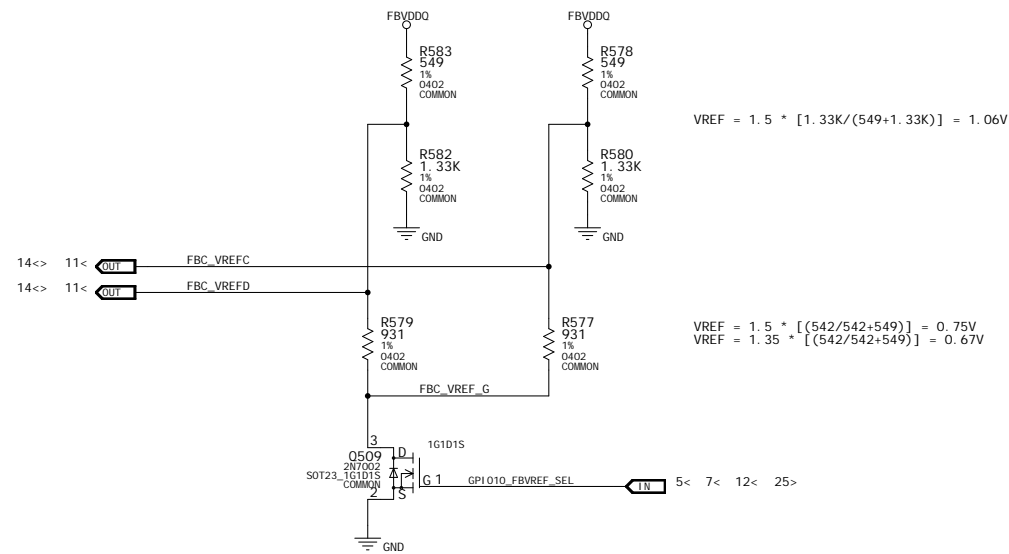
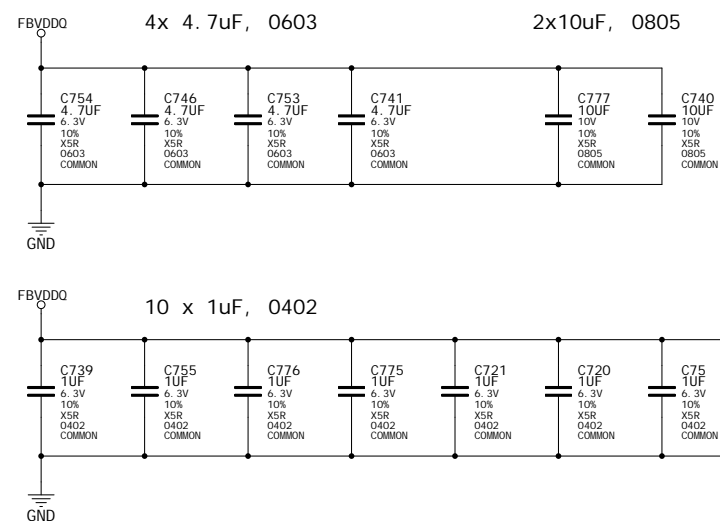
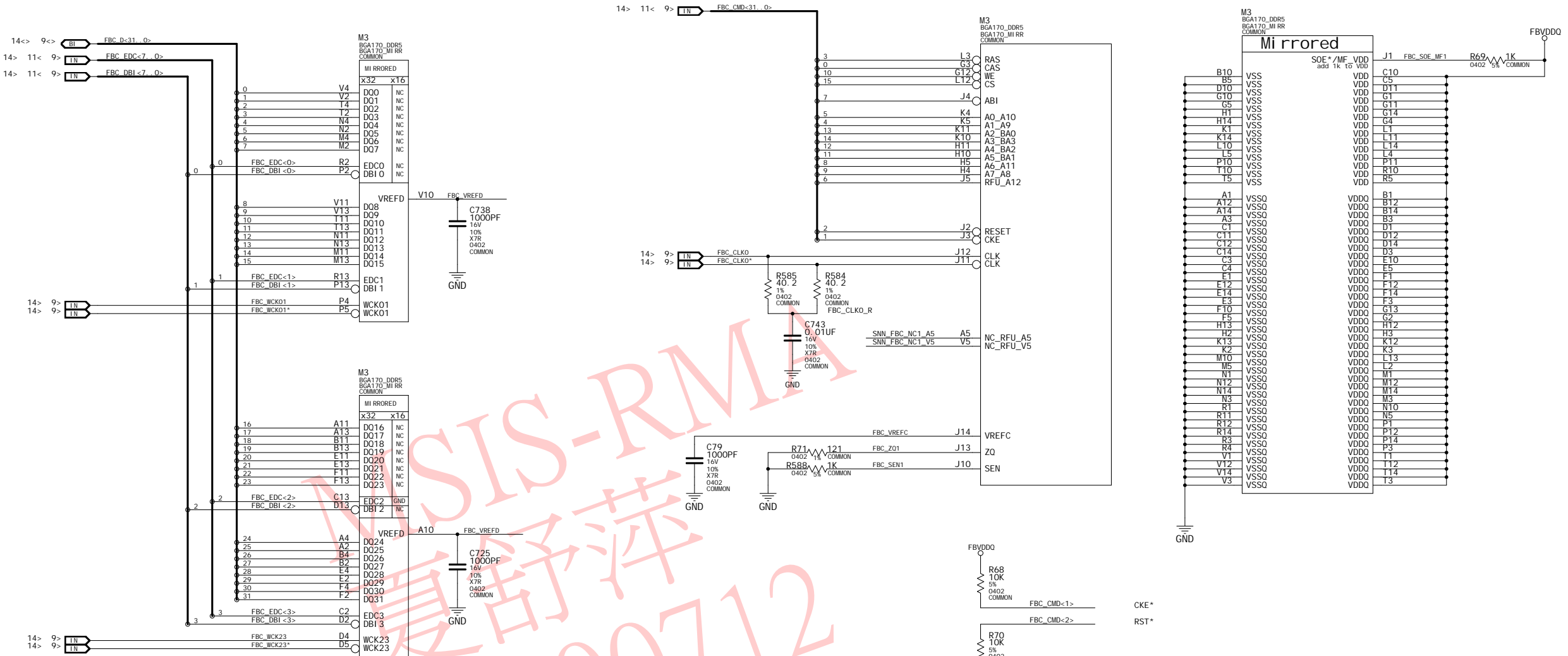







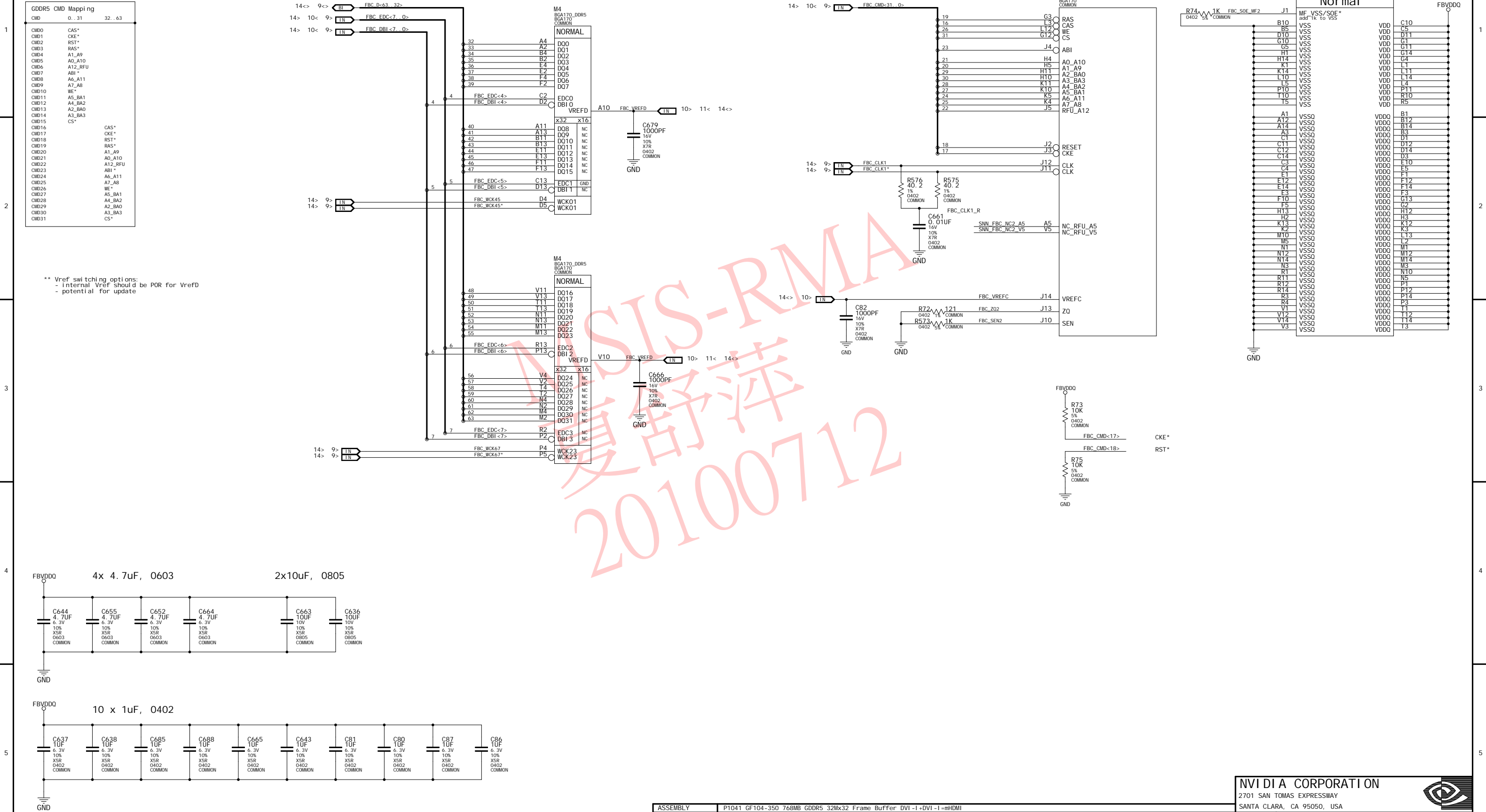
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CMD1	CKE*	
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CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		AB1*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

```
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- potential for update
```



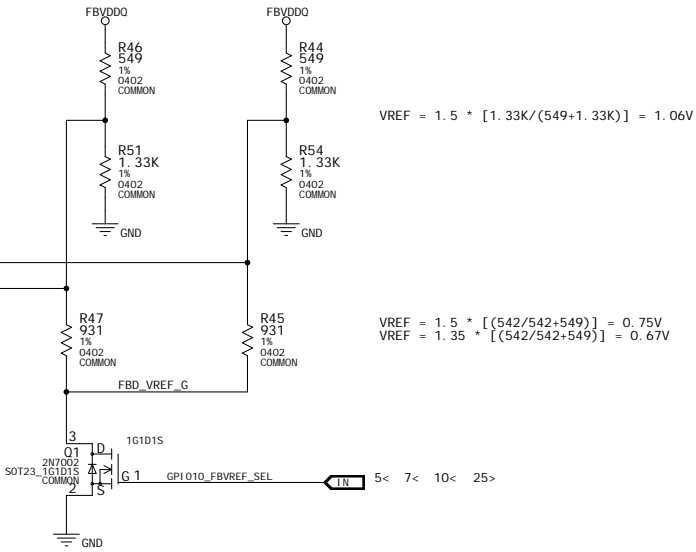
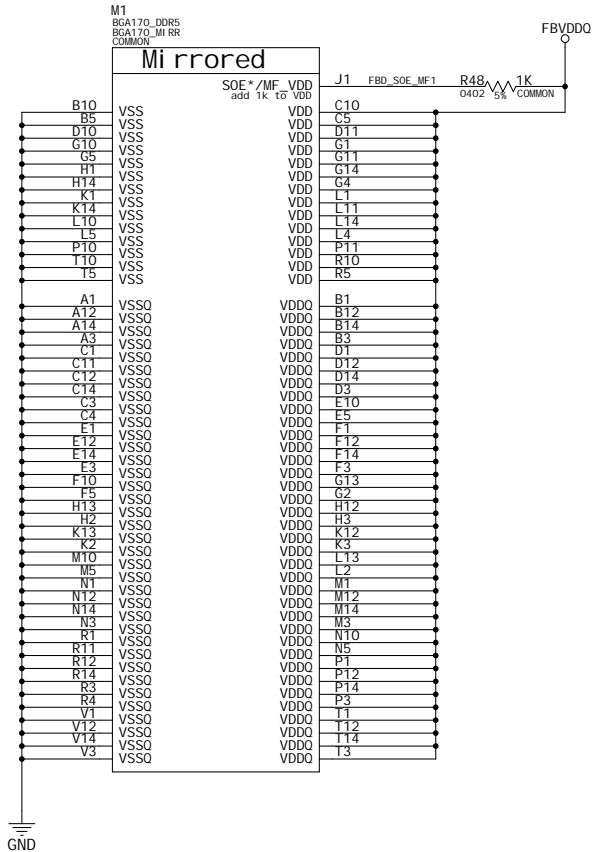
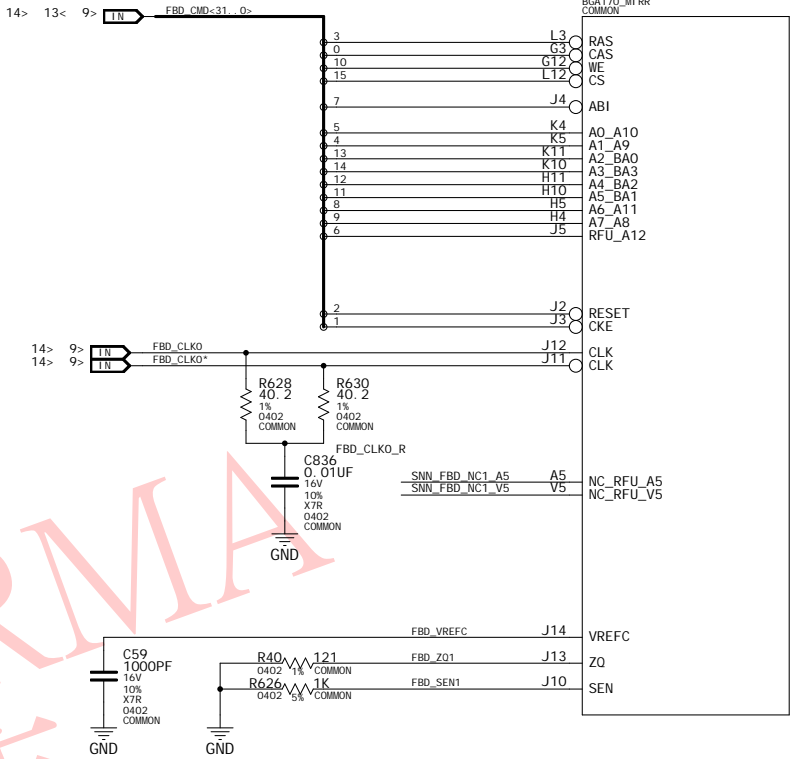
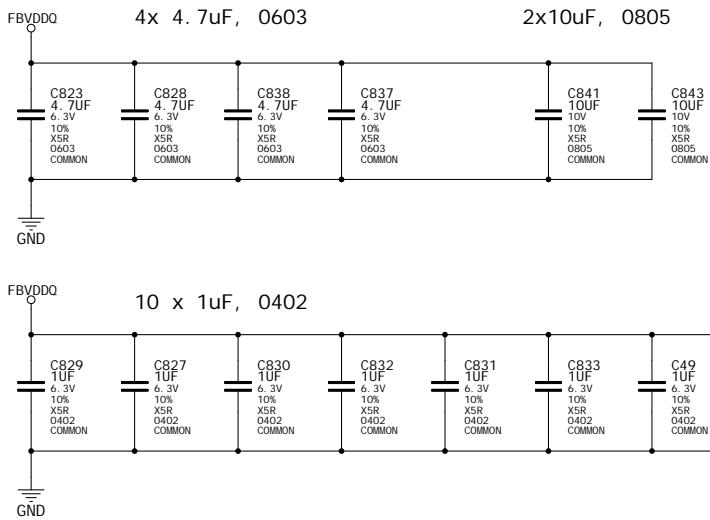
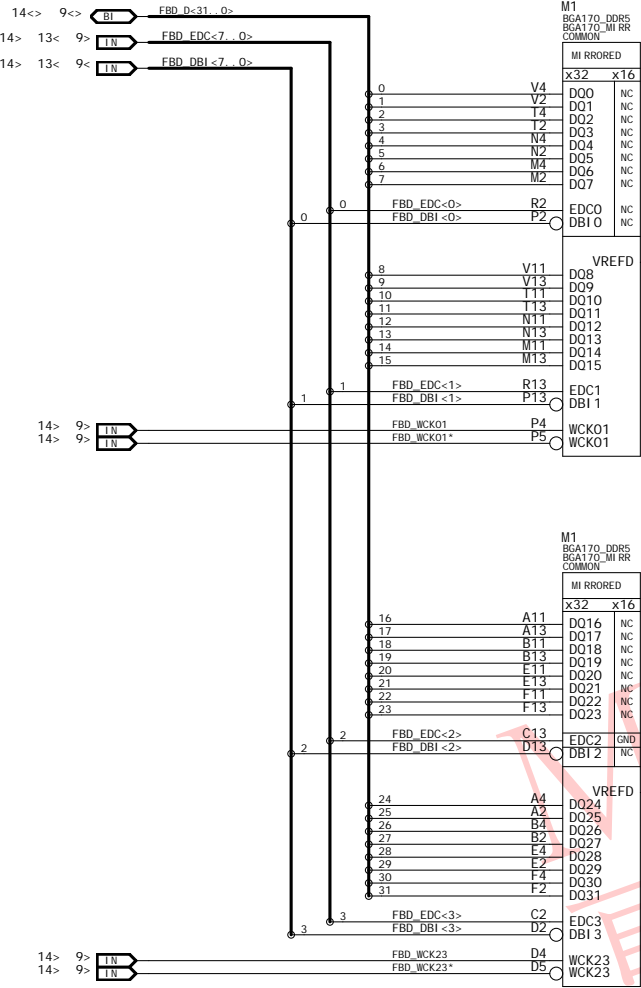
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SANTA CLARA, CA 95050, USA			
NV_PN	600-11041-0000-QS1		
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GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	AB1 *	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16	CAS*	
CMD17	CKE*	
CMD18	RST*	
CMD19	RAS*	
CMD20	A1_A9	
CMD21	A0_A10	
CMD22	A12_RFU	
CMD23	AB1 *	
CMD24	A6_A11	
CMD25	A7_A8	
CMD26	WE*	
CMD27	A5_BA1	
CMD28	A4_BA2	
CMD29	A2_BA0	
CMD30	A3_BA3	
CMD31	CS*	

\*\* Vref switching options:  
- internal Vref should be POR for VrefD  
- potential for update

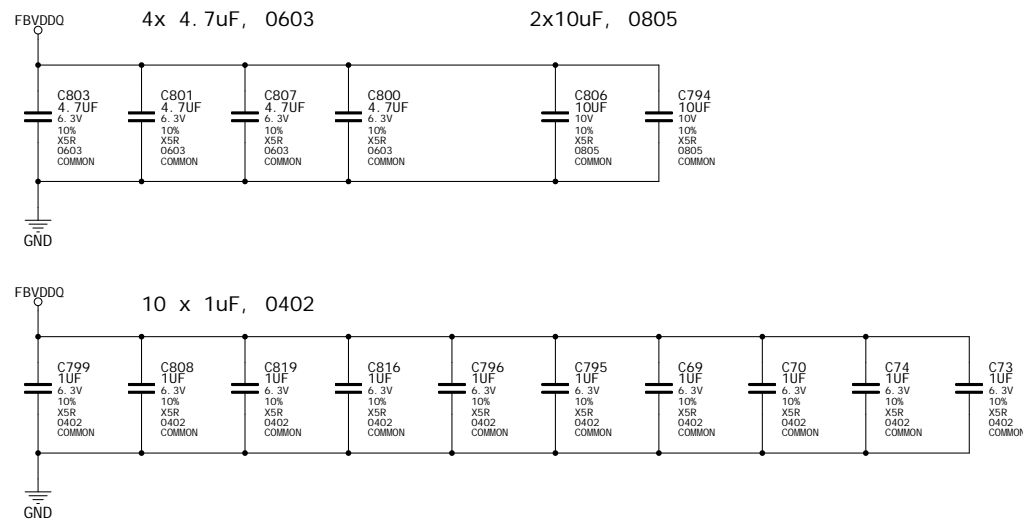
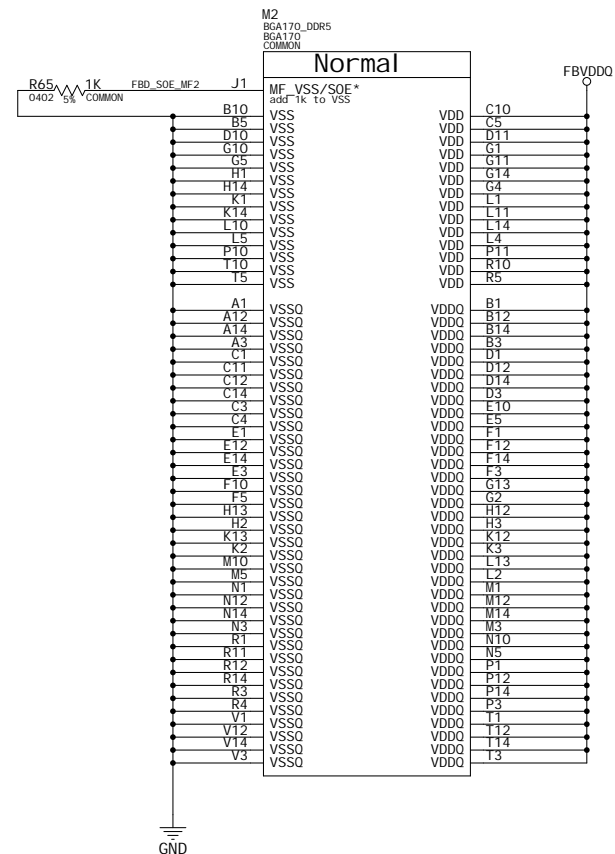
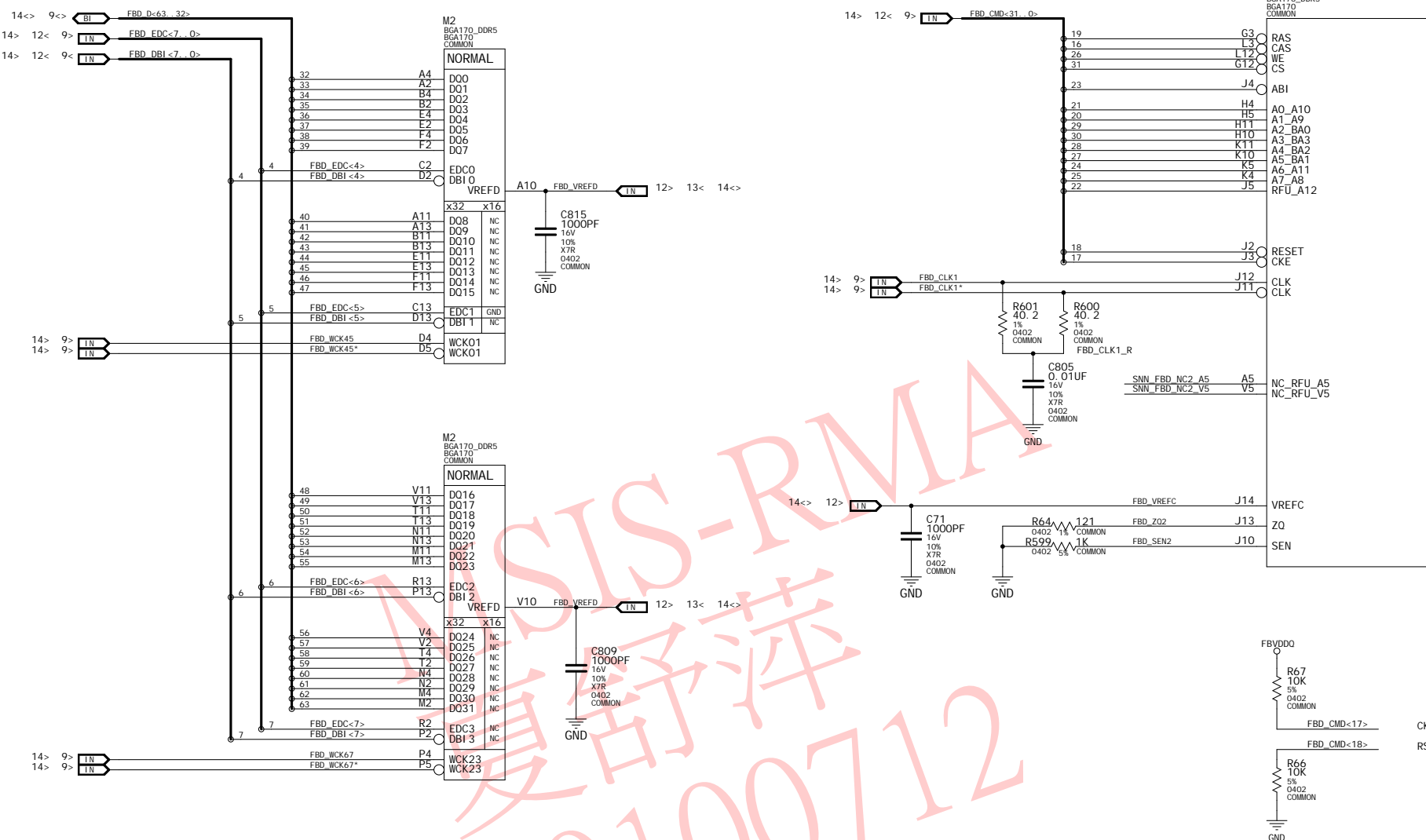


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

































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



































GDDR5	CMD	Mappi ng
CMD	0 . 31	32 . 63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	AB1*	
CMD8	A6_A11	
CMD9	A7_AB	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		AB1*
CMD24		A6_A11
CMD25		A7_AB
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

```
** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update
```



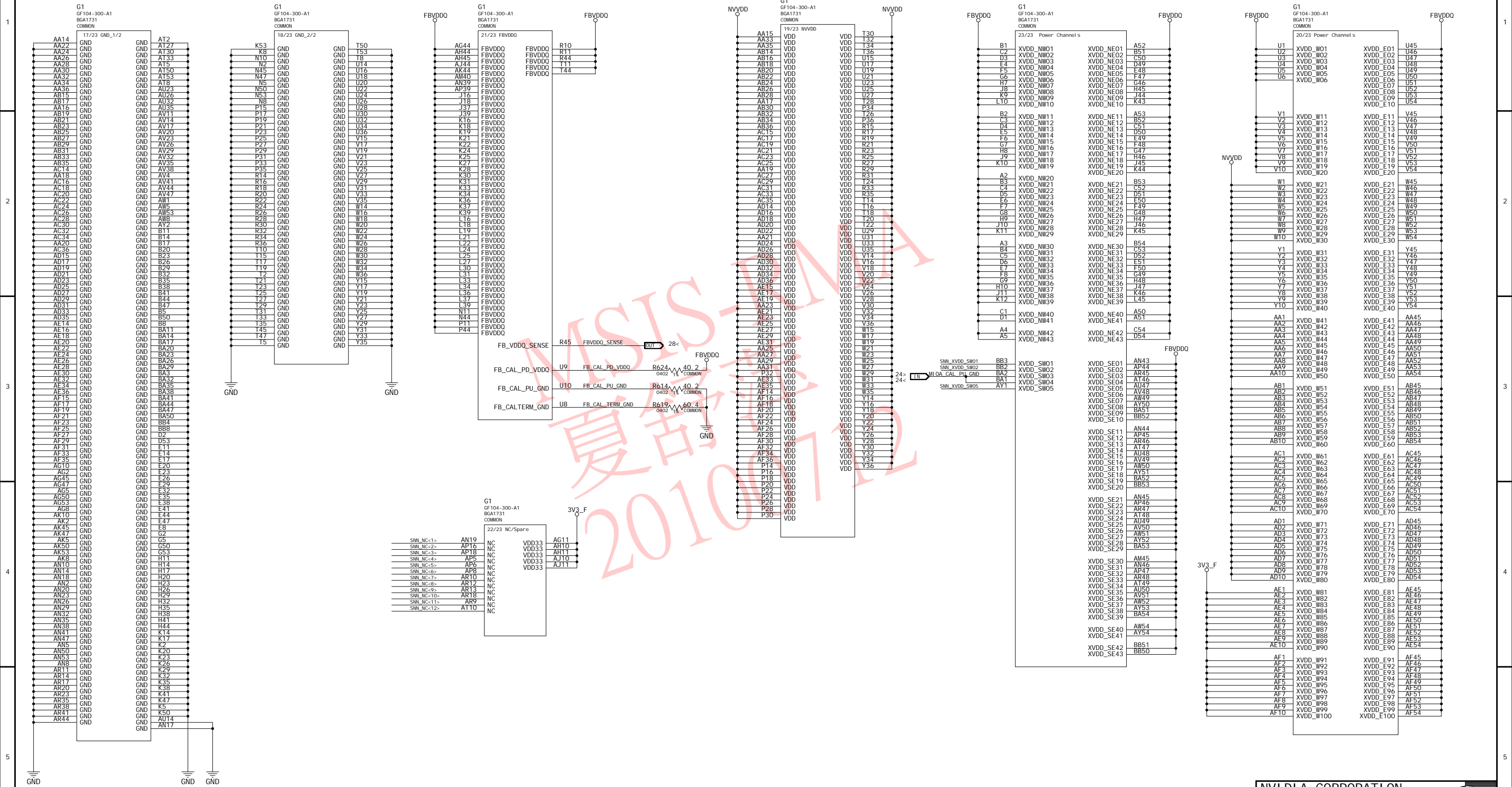


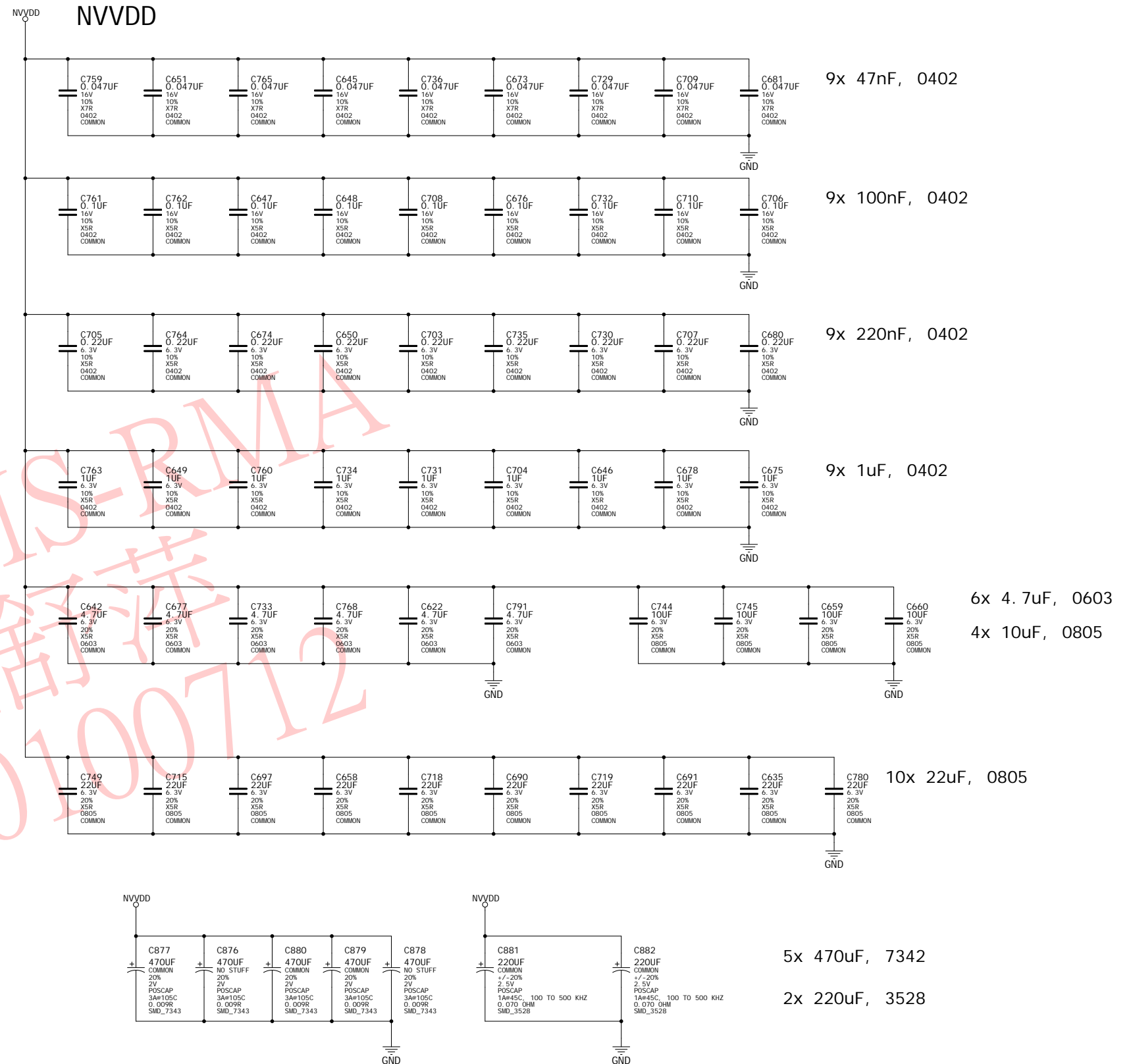
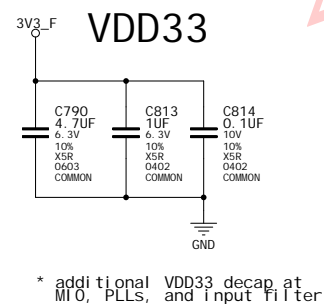
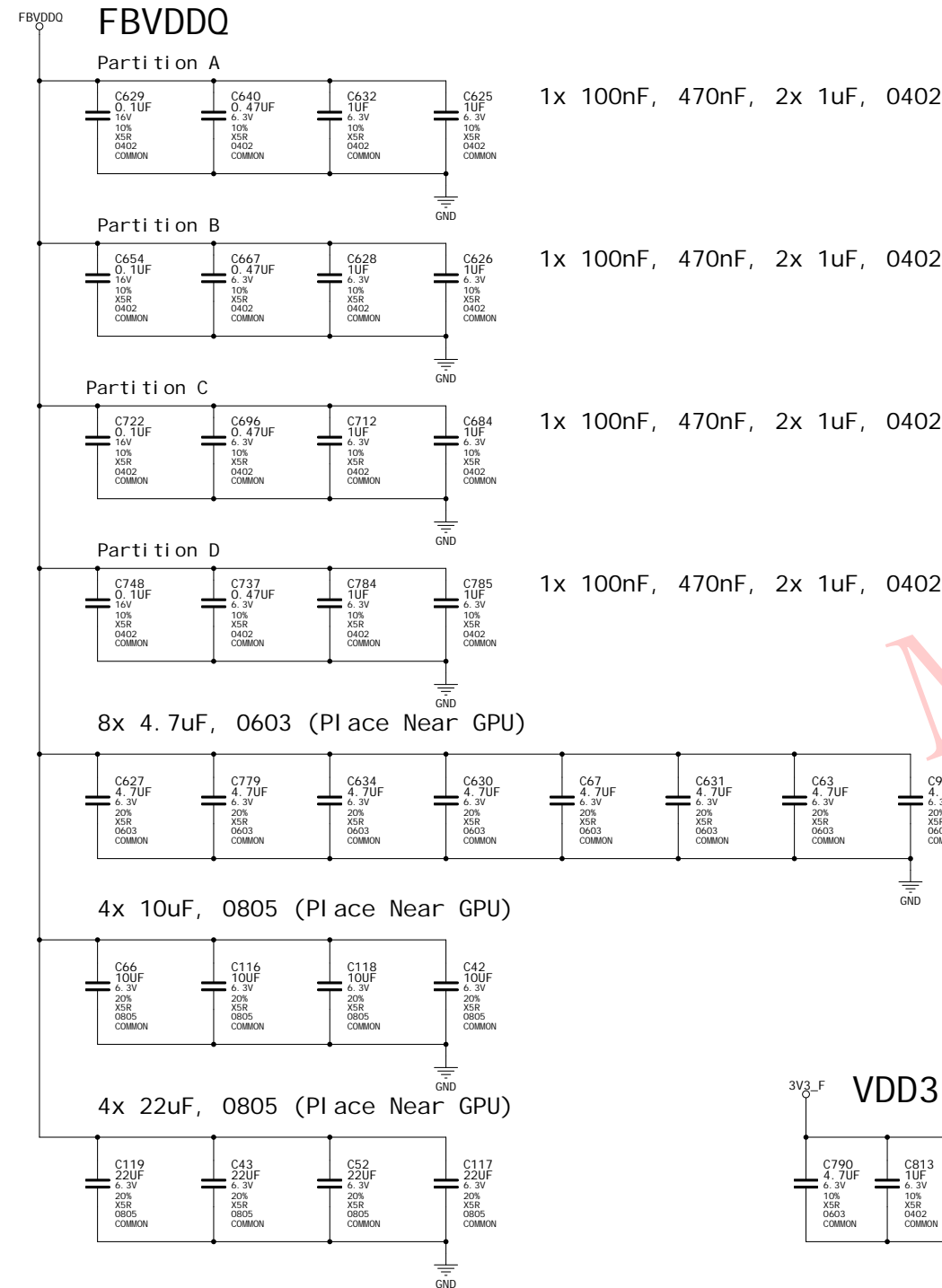
NET RULES for FrameBuffer A/B				
NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
5< 4>	 FBA_CLK0	1	80DI FF	FBA_CLK0
5< 4>	 FBA_CLK0*	1	80DI FF	FBA_CLK0
6< 4>	 FBA_CLK1	1	80DI FF	FBA_CLK1
6< 4>	 FBA_CLK1*	1	80DI FF	FBA_CLK1
7< 4>	 FBB_WCK01	1	80DI FF	FBB_WCK01
7< 4>	 FBB_WCK01*	1	80DI FF	FBB_WCK01
7< 4>	 FBB_WCK23	1	80DI FF	FBB_WCK23
7< 4>	 FBB_WCK23*	1	80DI FF	FBB_WCK23
8< 4>	 FBB_WCK45	1	80DI FF	FBB_WCK45
8< 4>	 FBB_WCK45*	1	80DI FF	FBB_WCK45
8< 4>	 FBB_WCK67	1	80DI FF	FBB_WCK67
8< 4>	 FBB_WCK67*	1	80DI FF	FBB_WCK67
6< 5< 4>	 FBA_CMD<31..0>	1	45OHM	
6< 5< 4>	 FBA_EDC<7..0>	1	45OHM	
6< 5< 4<	 FBA_DBI<7..0>	1	45OHM	
6<> 5<> 4<>	 FBA_D<63..0>	1	45OHM	
NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
7< 4>	 FBB_CLK0	1	80DI FF	FBB_CLK0
7< 4>	 FBB_CLK0*	1	80DI FF	FBB_CLK0
8< 4>	 FBB_CLK1	1	80DI FF	FBB_CLK1
8< 4>	 FBB_CLK1*	1	80DI FF	FBB_CLK1
5< 4>	 FBA_WCK01	1	80DI FF	FBA_WCK01
5< 4>	 FBA_WCK01*	1	80DI FF	FBA_WCK01
5< 4>	 FBA_WCK23	1	80DI FF	FBA_WCK23
5< 4>	 FBA_WCK23*	1	80DI FF	FBA_WCK23
6< 4>	 FBA_WCK45	1	80DI FF	FBA_WCK45
6< 4>	 FBA_WCK45*	1	80DI FF	FBA_WCK45
6< 4>	 FBA_WCK67	1	80DI FF	FBA_WCK67
6< 4>	 FBA_WCK67*	1	80DI FF	FBA_WCK67
8< 7< 4>	 FBB_CMD<31..0>	1	45OHM	
8< 7< 4>	 FBB_EDC<7..0>	1	45OHM	
8< 7< 4<	 FBB_DBI<7..0>	1	45OHM	
8<> 7<> 4<>	 FBB_D<63..0>	1	45OHM	
NET		VOLTAGE	MAX_CURRENT	MI N_WI DTH
6< 5>	 FBA_VREFD	1.00V	0.02A	8MI L
6< 5>	 FBA_VREFC	1.00V	0.02A	8MI L
8< 7>	 FBB_VREFD	1.00V	0.02A	8MI L
8< 7>	 FBB_VREFC	1.00V	0.02A	8MI L

NET RULES for FrameBuffer C/D				
NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
10< 9>	 FBC_CLK0	1	80DI FF	FBC_CLK0
10< 9>	 FBC_CLK0*	1	80DI FF	FBC_CLK0
11< 9>	 FBC_CLK1	1	80DI FF	FBC_CLK1
11< 9>	 FBC_CLK1*	1	80DI FF	FBC_CLK1
10< 9>	 FBC_WCK01	1	80DI FF	FBC_WCK01
10< 9>	 FBC_WCK01*	1	80DI FF	FBC_WCK01
10< 9>	 FBC_WCK23	1	80DI FF	FBC_WCK23
10< 9>	 FBC_WCK23*	1	80DI FF	FBC_WCK23
11< 9>	 FBC_WCK45	1	80DI FF	FBC_WCK45
11< 9>	 FBC_WCK45*	1	80DI FF	FBC_WCK45
11< 9>	 FBC_WCK67	1	80DI FF	FBC_WCK67
11< 9>	 FBC_WCK67*	1	80DI FF	FBC_WCK67
11< 10< 9>	 FBC_CMD<31..0>	1	45OHM	
11< 10< 9>	 FBC_EDC<7..0>	1	45OHM	
11< 10< 9>	 FBC_DBI<7..0>	1	45OHM	
11<> 10<> 9<>	 FBC_D<63..0>	1	45OHM	
NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
12< 9>	 FBD_CLK0	1	80DI FF	FBD_CLK0
12< 9>	 FBD_CLK0*	1	80DI FF	FBD_CLK0
13< 9>	 FBD_CLK1	1	80DI FF	FBD_CLK1
13< 9>	 FBD_CLK1*	1	80DI FF	FBD_CLK1
12< 9>	 FBD_WCK01	1	80DI FF	FBD_WCK01
12< 9>	 FBD_WCK01*	1	80DI FF	FBD_WCK01
12< 9>	 FBD_WCK23	1	80DI FF	FBD_WCK23
12< 9>	 FBD_WCK23*	1	80DI FF	FBD_WCK23
13< 9>	 FBD_WCK45	1	80DI FF	FBD_WCK45
13< 9>	 FBD_WCK45*	1	80DI FF	FBD_WCK45
13< 9>	 FBD_WCK67	1	80DI FF	FBD_WCK67
13< 9>	 FBD_WCK67*	1	80DI FF	FBD_WCK67
13< 12< 9>	 FBD_CMD<31..0>	1	45OHM	
13< 12< 9>	 FBD_EDC<7..0>	1	45OHM	
13< 12< 9>	 FBD_DBI<7..0>	1	45OHM	
13<> 12<> 9<>	 FBD_D<63..0>	1	45OHM	
NET		VOLTAGE	MAX_CURRENT	MI N_WI DTH
11< 10>	 FBC_VREFD	1.00V	0.02A	8MI L
11< 10>	 FBC_VREFC	1.00V	0.02A	8MI L
13< 12>	 FBD_VREFD	1.00V	0.02A	8MI L
13< 12>	 FBD_VREFC	1.00V	0.02A	8MI L



\*\* Power channels are configurable.  
XVDD\_\* pins are not connected on the substrate.  
Therefore, XVDD\_\* pins can be assigned as needed.





ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI -I +DVI -I =mHDMI
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<b>NV_PN</b> 600-11041-0000-QS1			
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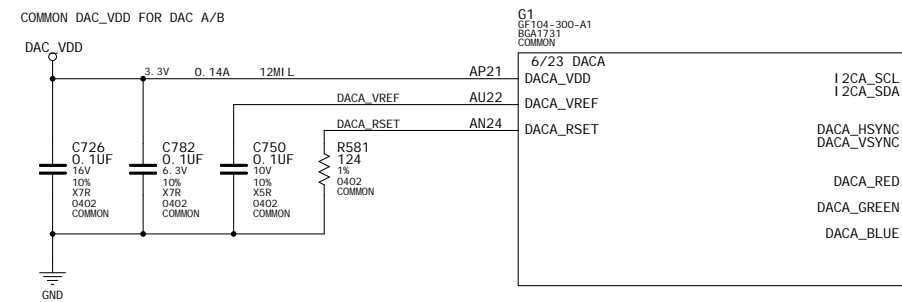
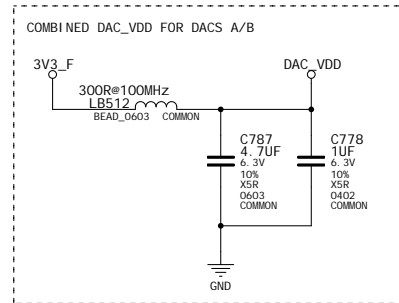
MSIS-RMA  
夏舒萍  
20100712

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
PAGE DETAIL	<edit here to insert page detail>

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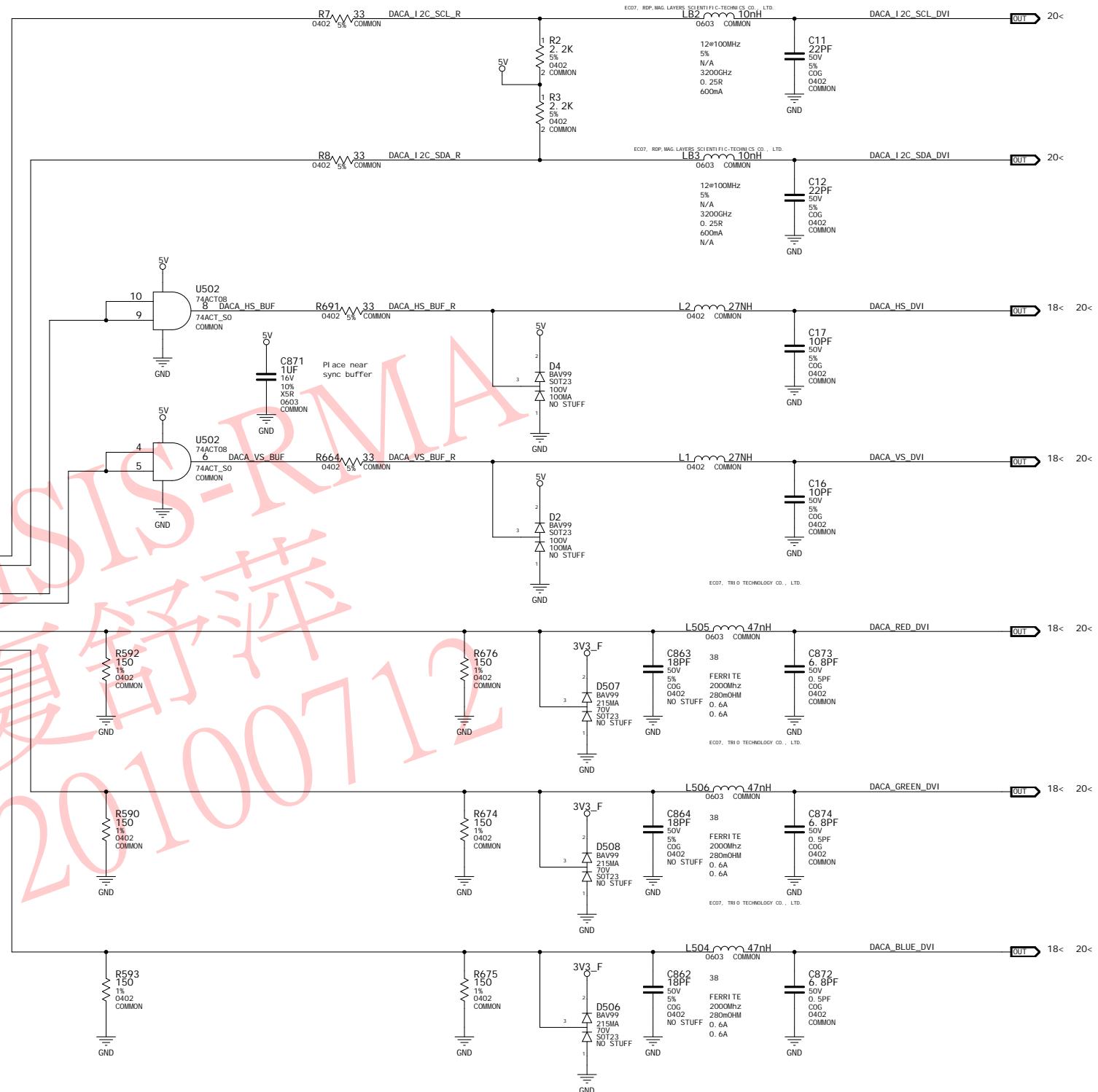
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2701 SAN TOMAS EXPRESSWAY			
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NV_PN	600-11041-0000-QS1		
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## DACA NET RULES

	NET	NV_CRI TI CAL	NV_I MPEDANCE
I/N	DACA_RED	1	750HM
	DACA_GREEN	1	750HM
	DACA_BLUE	1	750HM
I/N	DACA_RED_DVI	1	750HM
	DACA_GREEN_DVI	1	750HM
	DACA_BLUE_DVI	1	750HM
I/N	DACA_HSYNC	2	500HM
	DACA_VSYNC	2	500HM
	DACA_HS_BUF	2	500HM
I/N	DACA_VS_BUF	2	500HM
	DACA_HS_BUF_R	2	500HM
	DACA_VS_BUF_R	2	500HM
I/N	DACA_HS_DVI	2	500HM
	DACA_VS_DVI	2	500HM



ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
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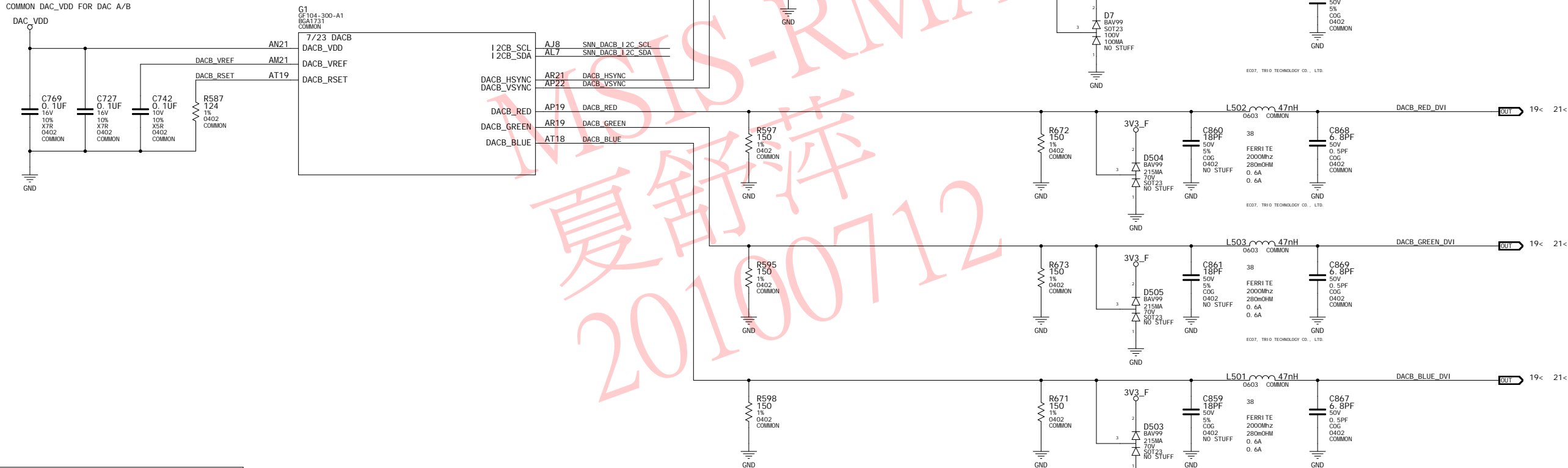
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## DACB NET RULES

		NET	NV_CRITICAL	NV_IMPEDANCE
		IN DACB_RED	1	750HM
		IN DACB_GREEN	1	750HM
		IN DACB_BLUE	1	750HM
21<	19>	IN DACB_RED_DVI	1	750HM
21<	19>	IN DACB_GREEN_DVI	1	750HM
21<	19>	IN DACB_BLUE_DVI	1	750HM
		IN DACB_HSYNC	2	500HM
		IN DACB_VSYNC	2	500HM
		IN DACB_HS_BUF	2	500HM
		IN DACB_VS_BUF	2	500HM
		IN DACB_HS_BUF_R	2	500HM
		IN DACB_VS_BUF_R	2	500HM
21<	19>	IN DACB_HS_DVI	2	500HM
21<	19>	IN DACB_VS_DVI	2	500HM

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI -I +DVI -I =mHDMI
PAGE DETAIL	<edit here to insert page detail>

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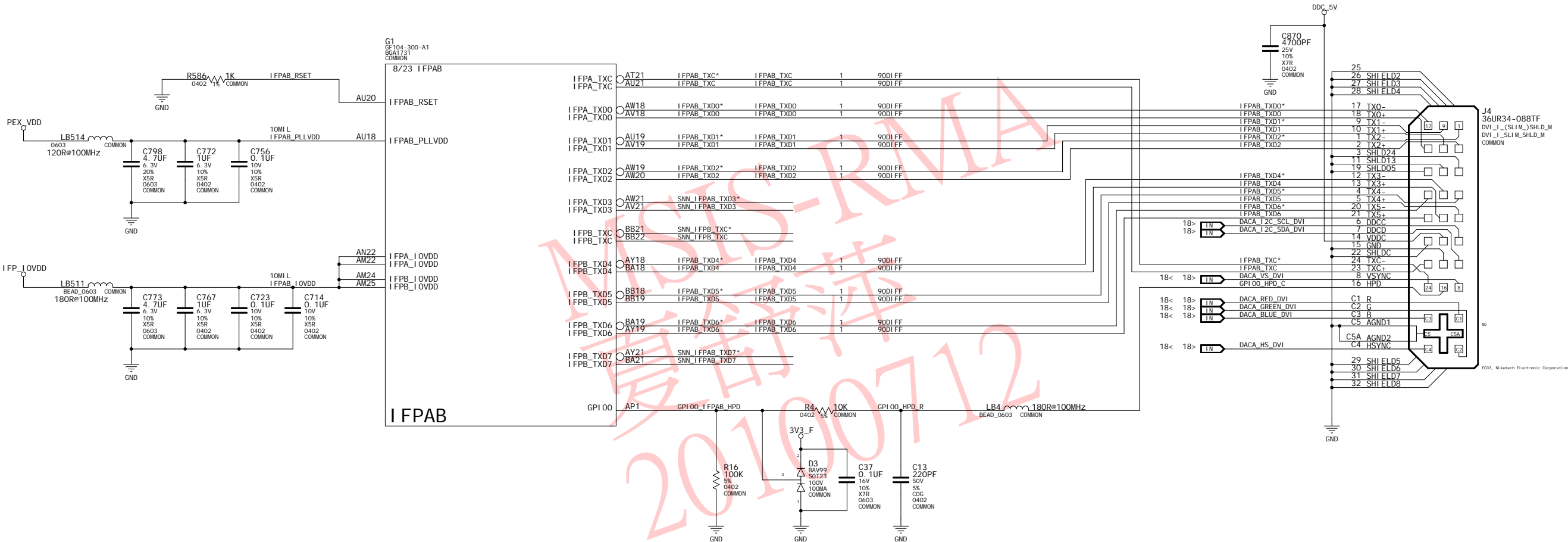
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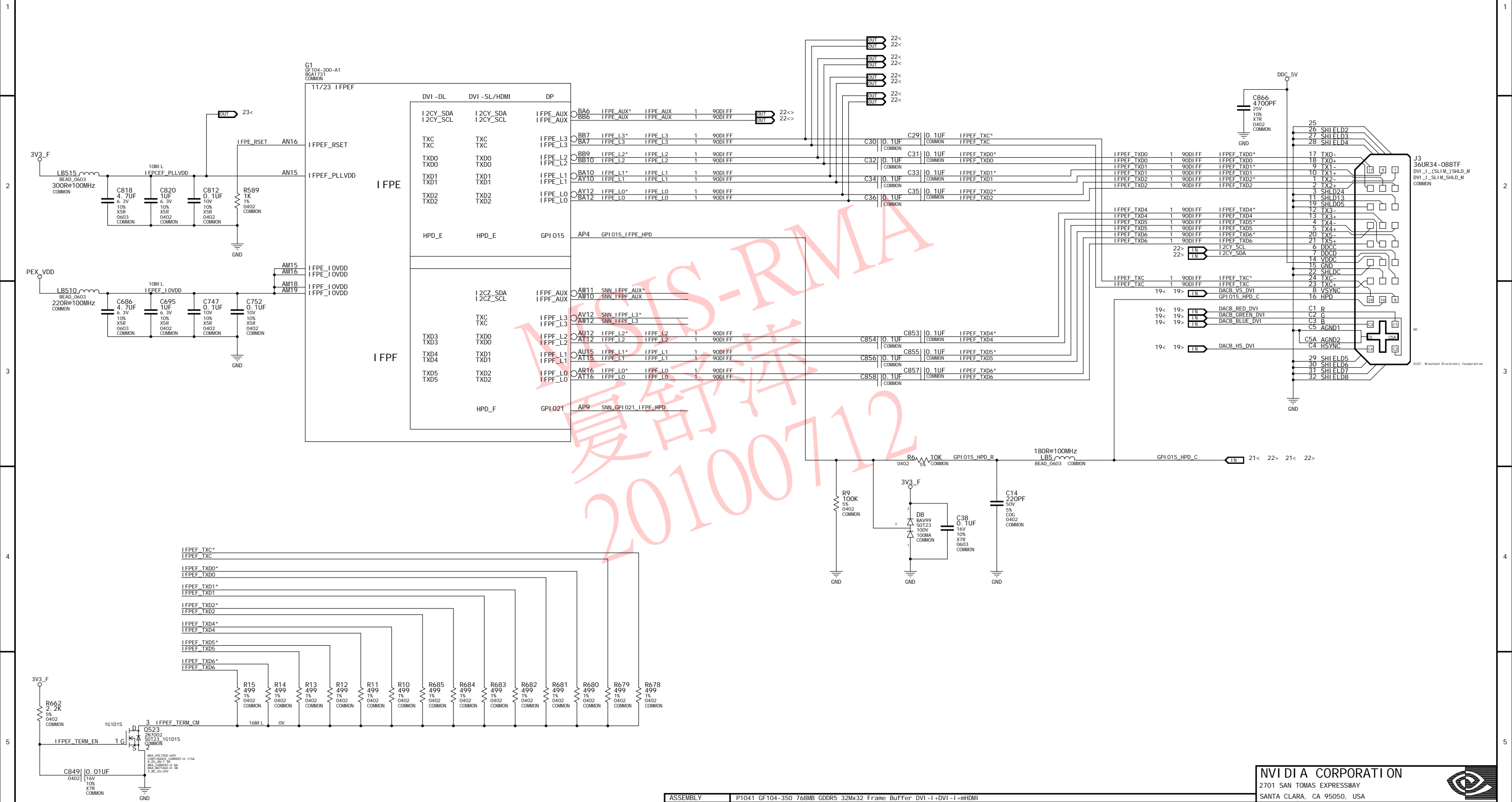
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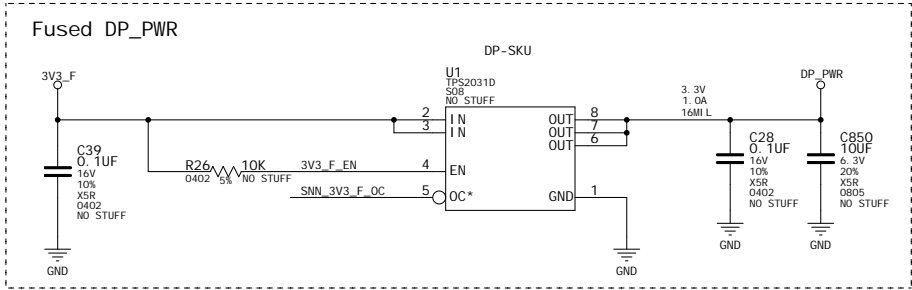
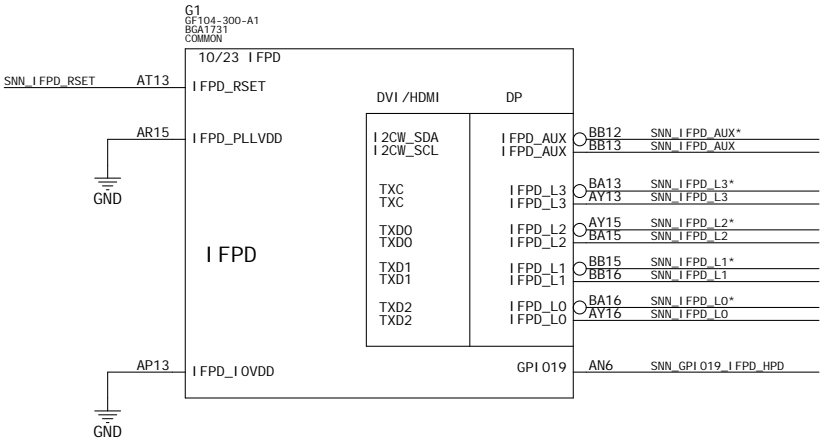
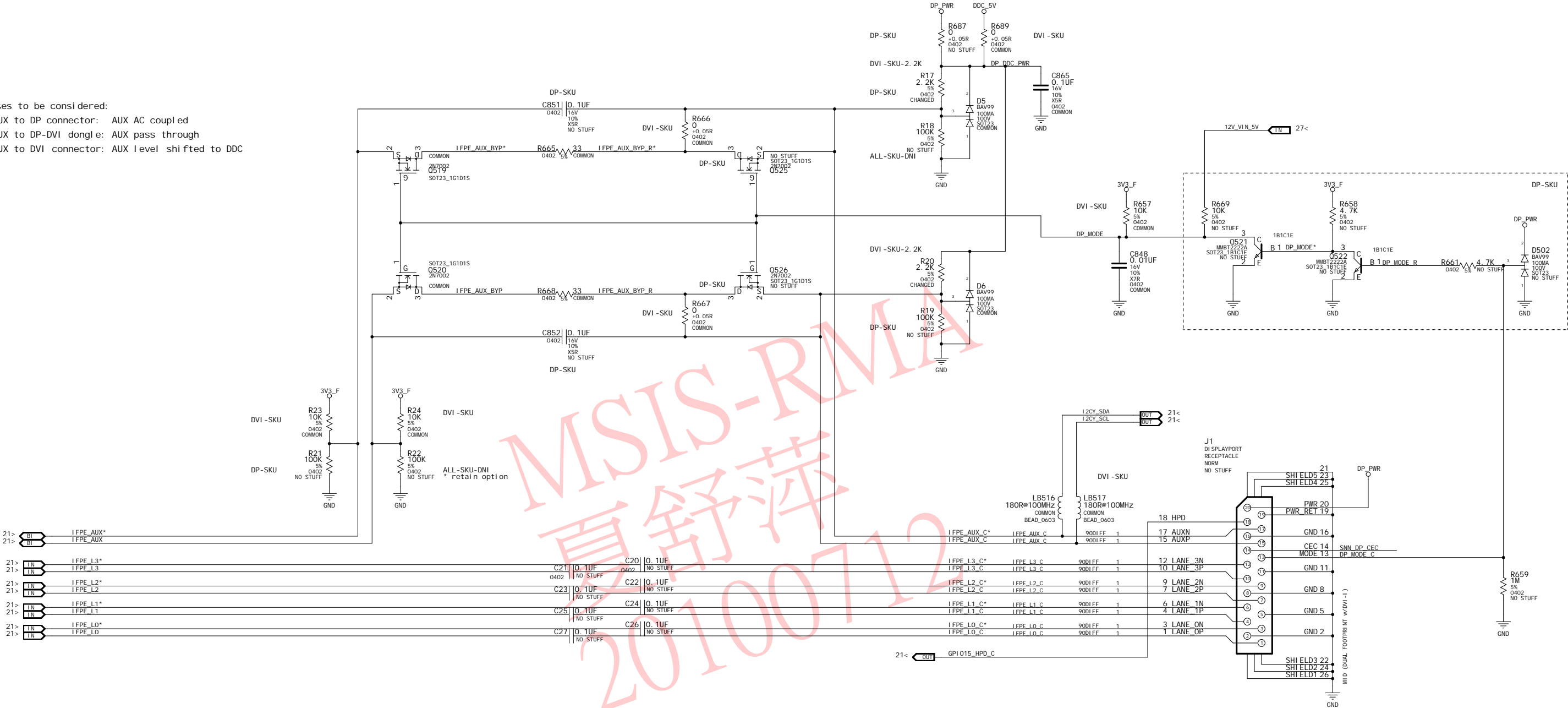


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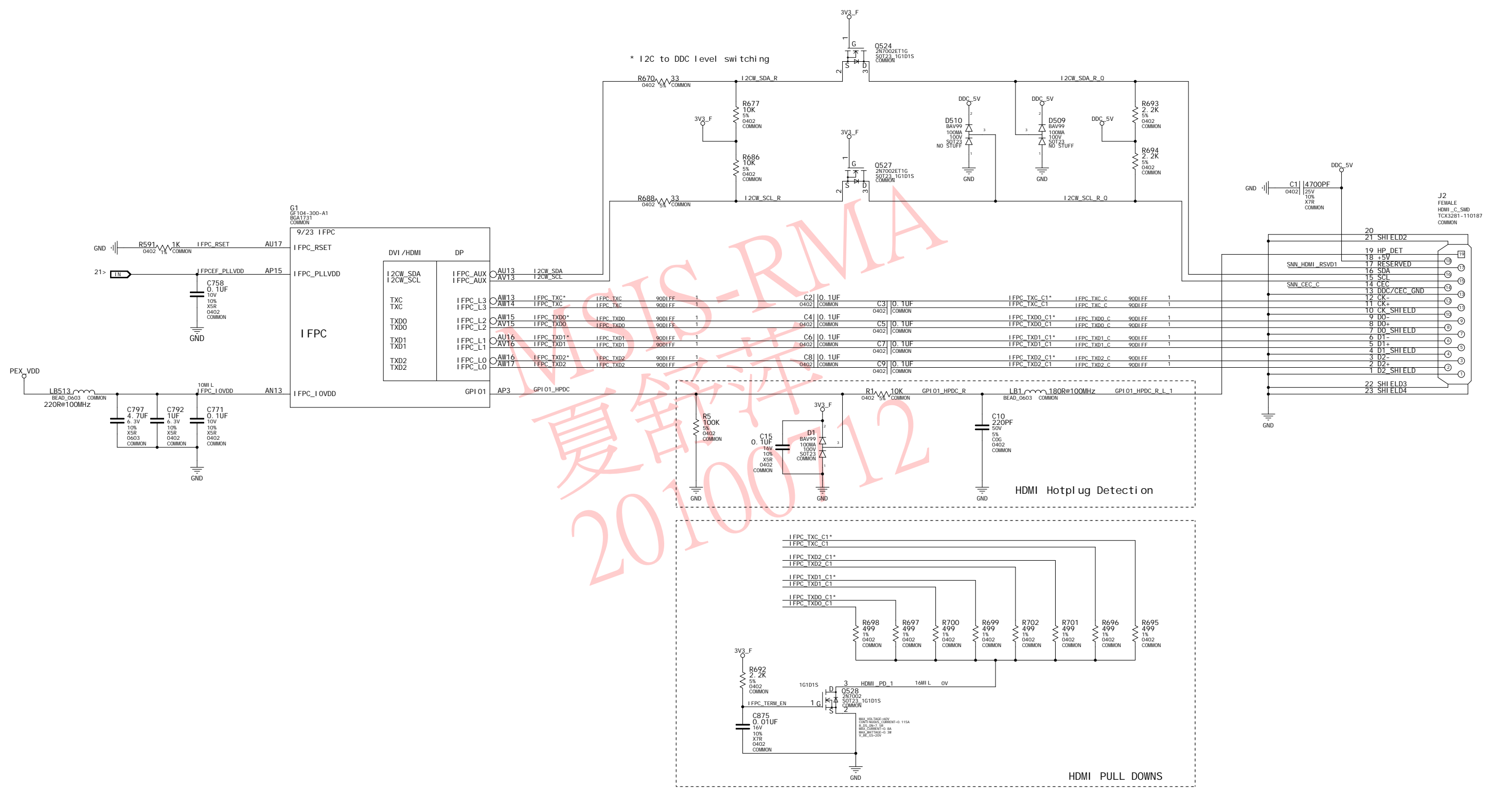
Three cases to be considered:

- 1. DP AUX to DP connector: AUX AC coupled
- 2. DP AUX to DP-DVI dongle: AUX pass through
- 3. DP AUX to DVI connector: AUX level shifted to DDC

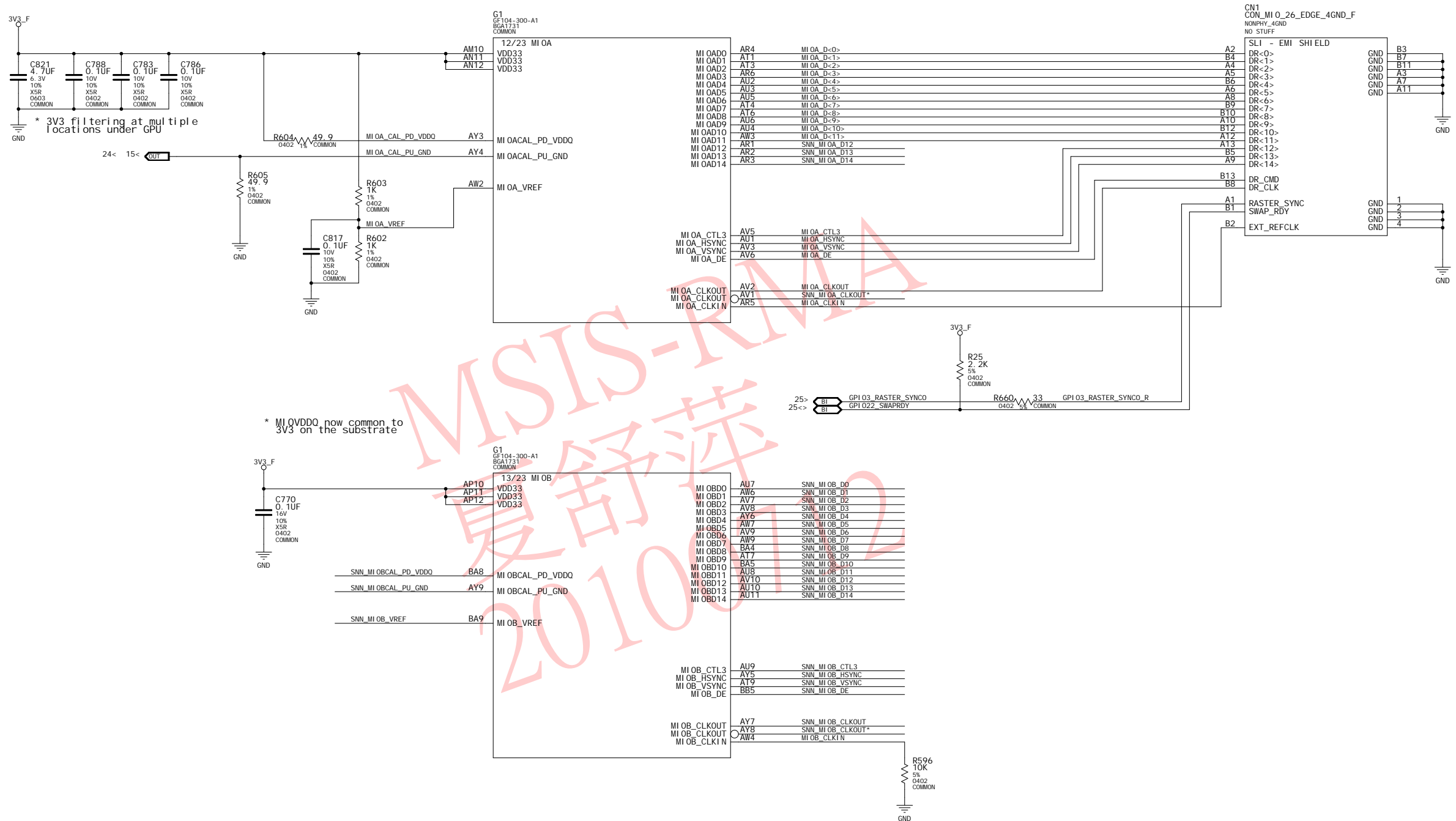


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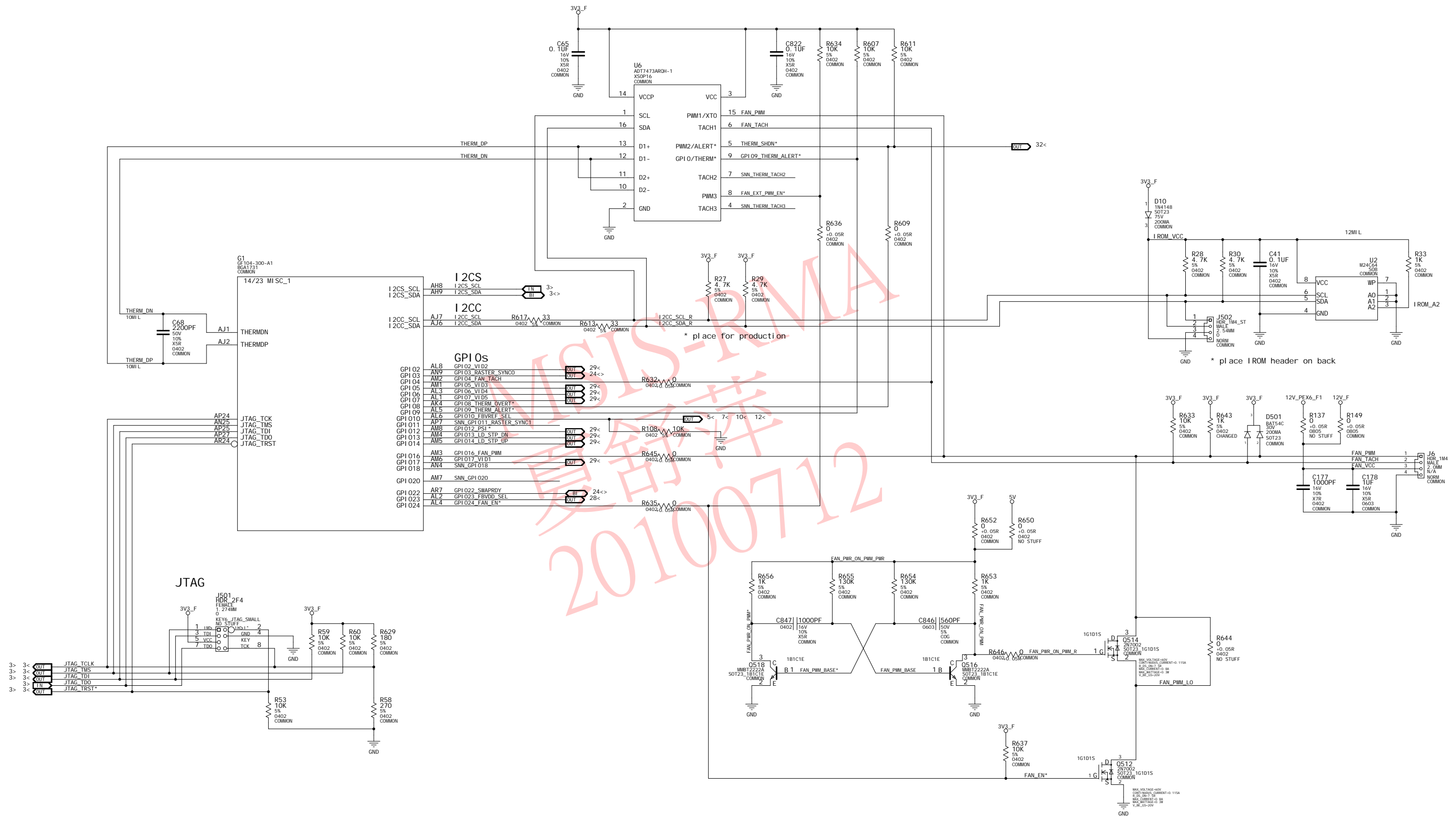
## MI 0 NET RULES

	NET	NV_CRI T I CAL	NV_I MPEDANCE	DI FFPAI R
1	MI OA_D<11...0>	1	500HM	
1	MI OA_HSYN C	1	500HM	
1	MI OA_VSYN C	1	500HM	
1	MI OA_C T L3	1	500HM	
1	MI OA_DE	1	500HM	
1	MI OA_C LKOUT	1	500HM	
1	MI OA_C LK_I N	1	500HM	

	NET	VOLTAGE	MI_N_WI_DTH
1N	MI_OA_VREF	1.65V	6MI_L
1N	MI_OA_CAL_PD_VDDO	3.3V	6MI_L
1N	MI_OA_CAL_PU_GND	0.0V	6MI_L


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<b>PCB REV</b>	<b>P1041-B01</b>	<b>PAGE</b>	<b>24 OF 34</b>
<b>BOM REV</b>	<b>A</b>	<b>DATE</b>	<b>12-MAY-2010</b>



ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI -I+DVI -I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

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PCB REV	P1041-B01	PAGE	25 OF 34
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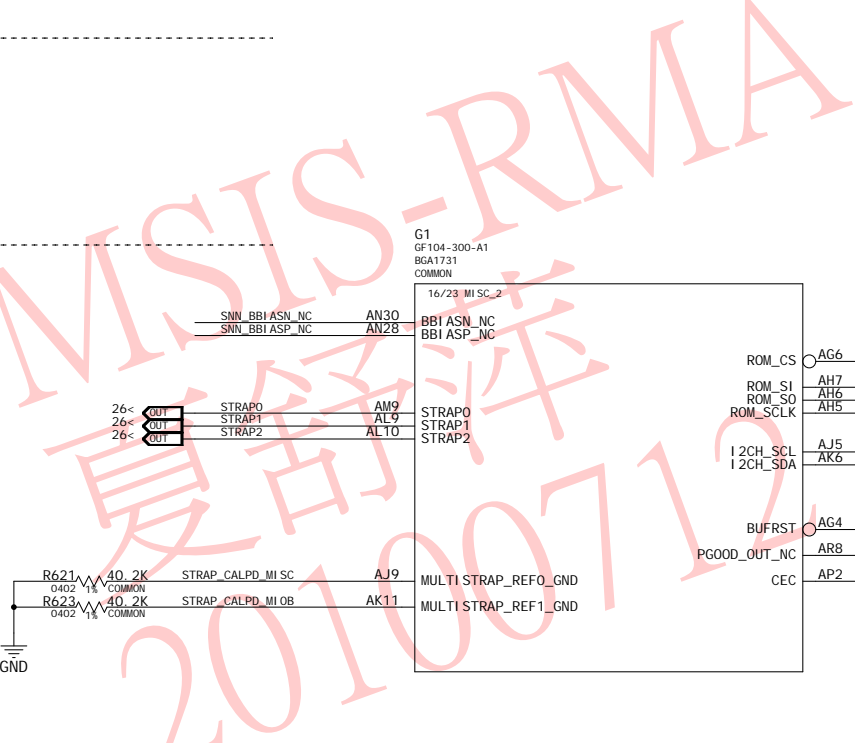
Page26: Mi sc: ROM, HDCP, XTAL, Straps

STRAPO	USER_BIT [3..0]	0000: => 5K PD
STRAP1	3GIO_PADCFG_LUT_ADR	0000 : =>5K PD      0000 Desktop
STRAP2	PCI_DEVID [3:0]	0010 For 0x0E22 : => 15K PD 0100 For 0x0E24 : => 25K PD
ROM_SI	RAMCFG[0]	32Mx32 256 bit Samsung for SKU 10 first memory 0011: PD 20K 32Mx32 256 bit Hynix for SKU 10 2'nd memory 0010: PD 15K
	RAMCFG[1]	
	RAMCFG[2]	32Mx32 192 bit Samsung for SKU 0 first memory 1011: PU 20K 32Mx32 192 bit Hynix for SKU 0 2'nd memory 1010: PU 15K
	RAMCFG[3]	
ROM_SO	VGA_DEVICE	1
	SMB_ALT_ADDR	0
	FB[0]_BAR_SIZE	0
ROM_SCLK	XCLK_417	0
	PEX_PLL_EN_TERM100	1 ENABLED
	SLOT_CLK_CFG	1 ENABLE
	SUB_VENDOR	1 Dedicated BIOS
	PCI_DEVID_EXT	0 0xC
		10k PD
		45K PD

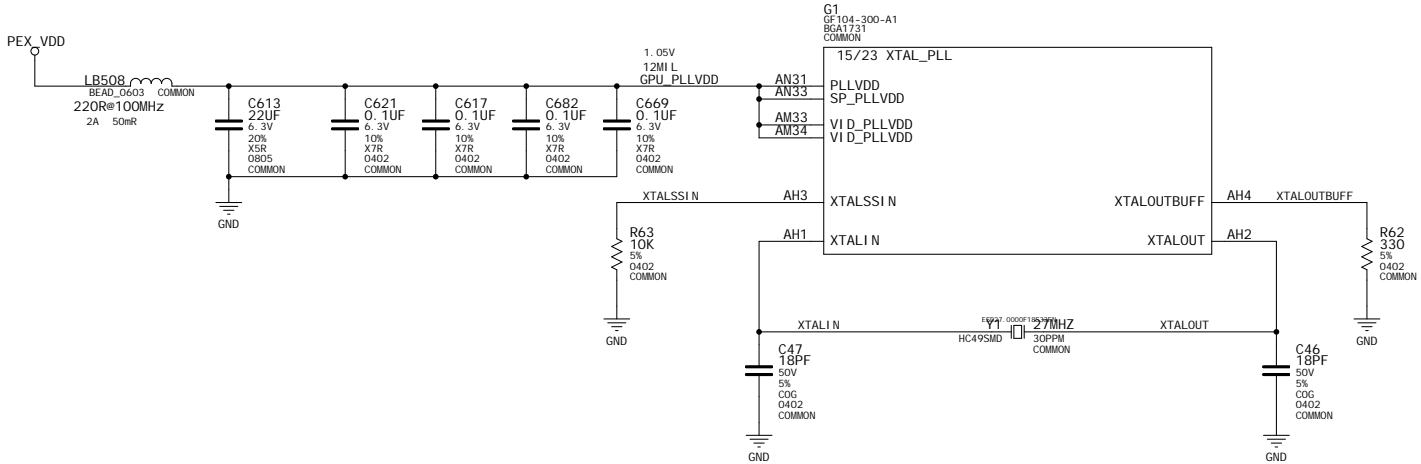
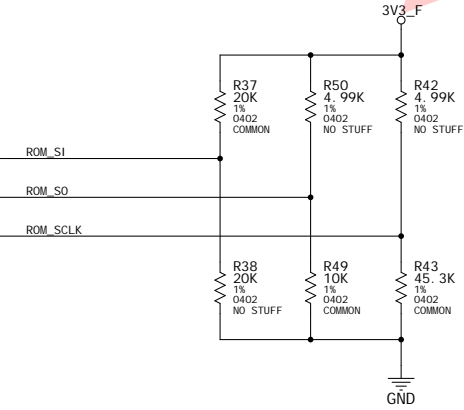
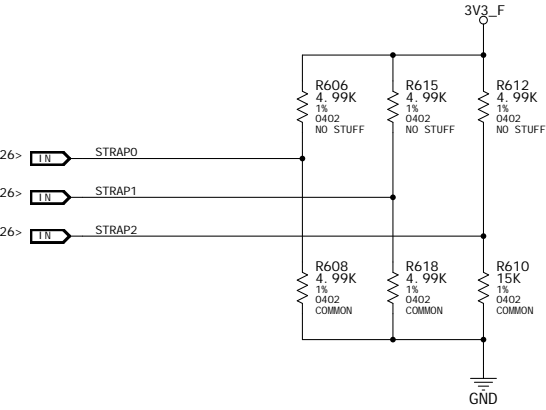
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit Qimonda	
0010	32Mx32 256-bit Hynix	
0011	32Mx32 256-bit Samsung	
0100	Reserved	
0101	64Mx32 256-bit Qimonda	
0110	64Mx32 256-bit Hynix	
0111	64Mx32 256-bit Samsung	
1000	Reserved	
1001	32Mx32 192-bit Qimonda	
1010	32Mx32 192-bit Hynix	
1011	32Mx32 192-bit Samsung	
1100	Reserved	
1101	64Mx32 192-bit Qimonda	
1110	64Mx32 192-bit Hynix	
1111	64Mx32 192-bit Samsung	

MISC NET RULES			
NET	NV_CRTICAL	NV_IMPEDANCE	
XTALSSIN	1	50OHM	
XTALIN	1	50OHM	
XTALOUT	1	50OHM	

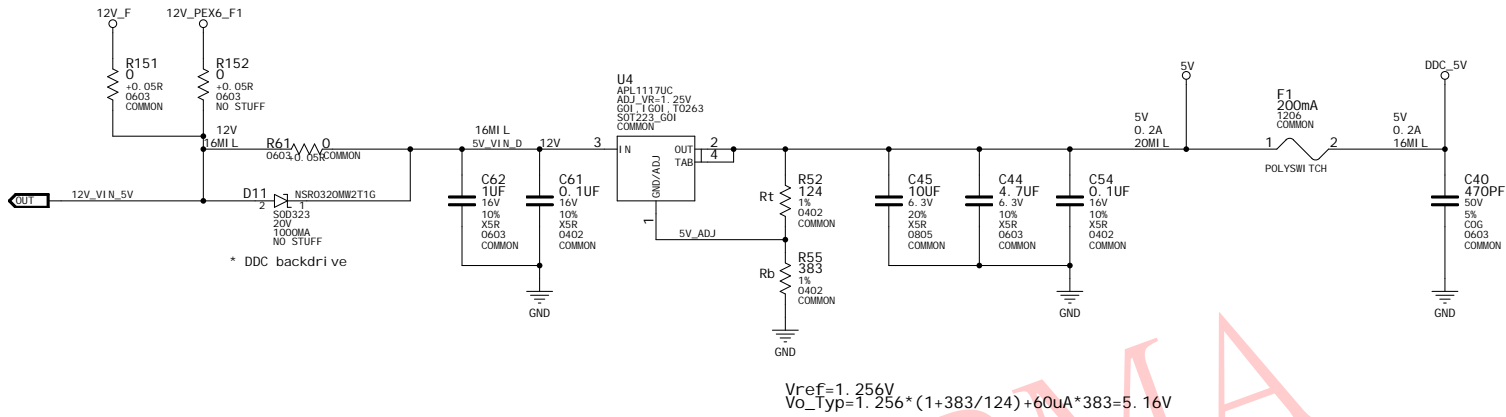


BINARY PRODUCTION	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY BRINGUP	NC	NC
MULTI-LEVEL	40.2k 1% TO GND	40.2k 1% TO GND

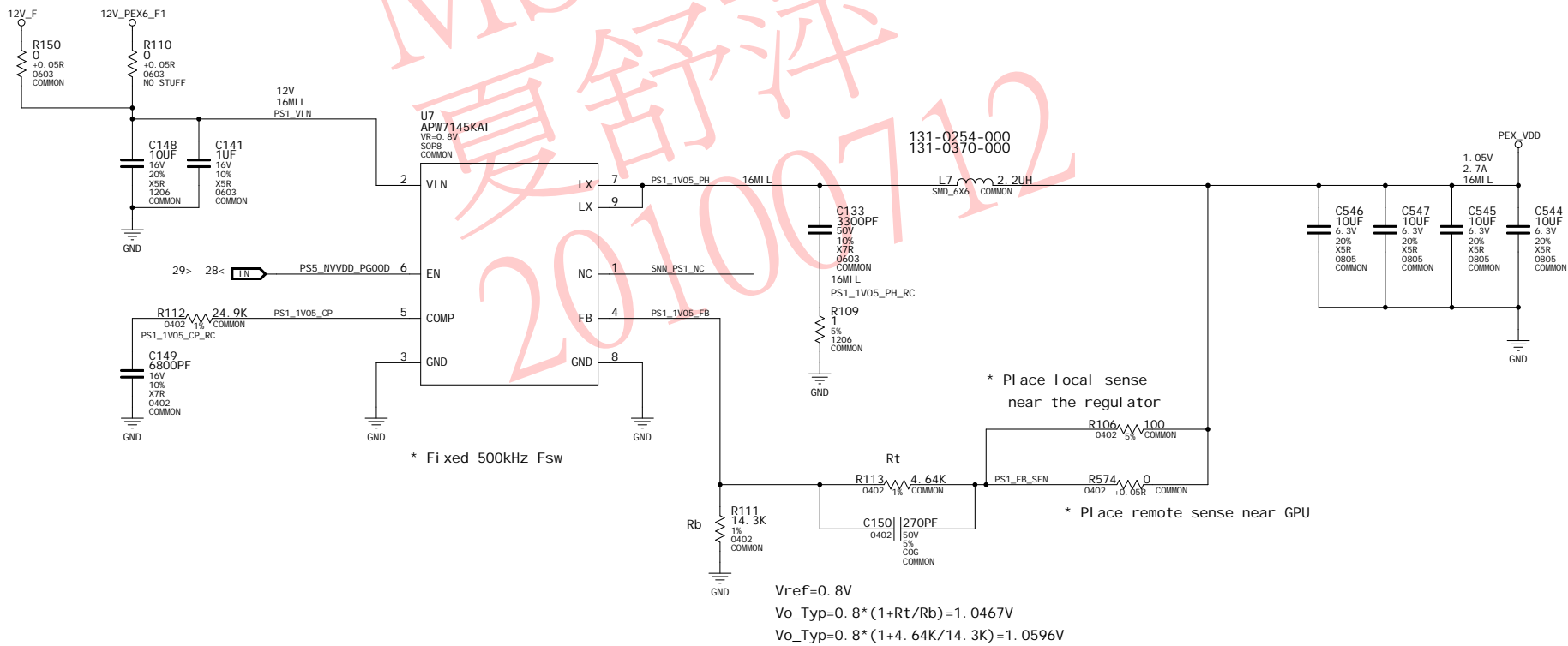


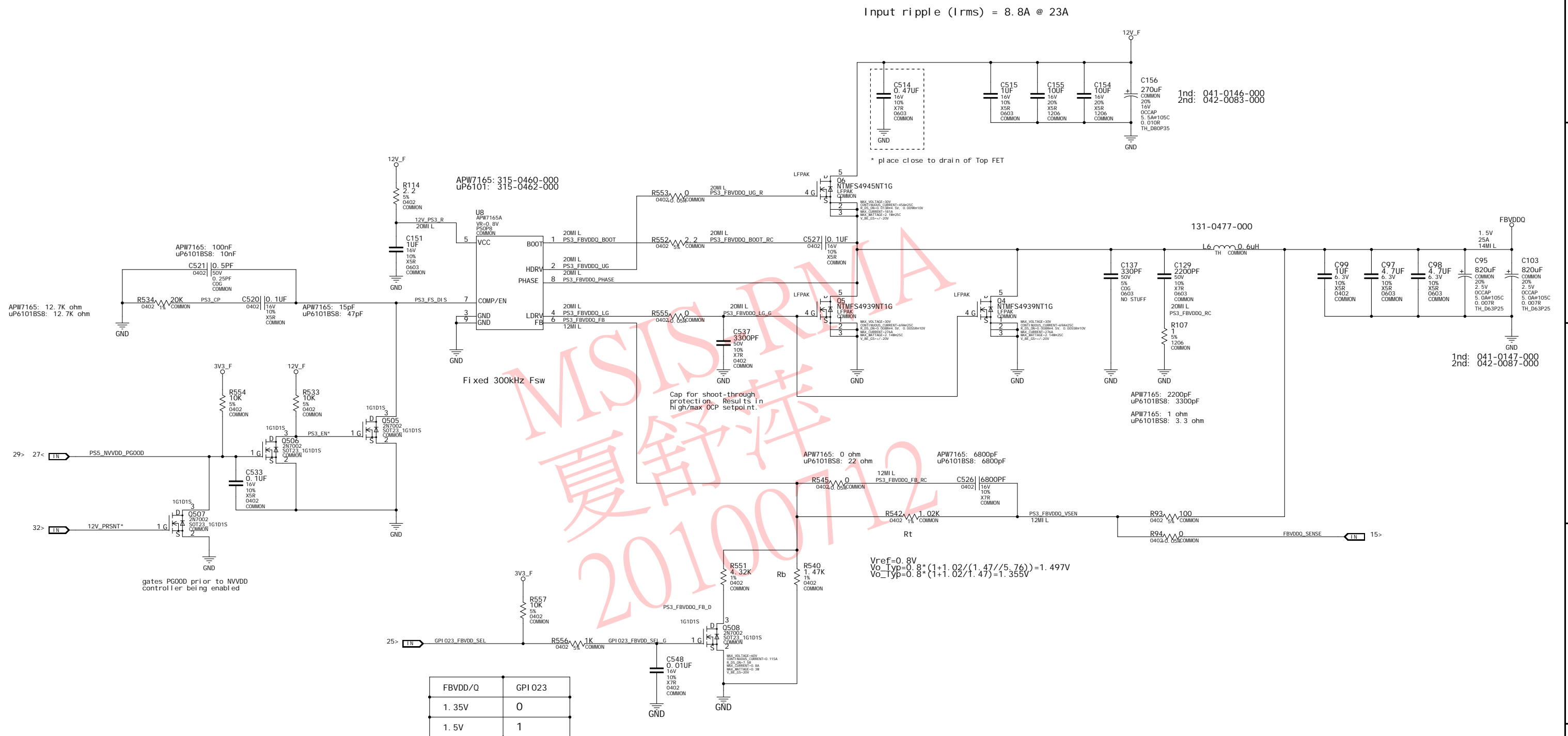
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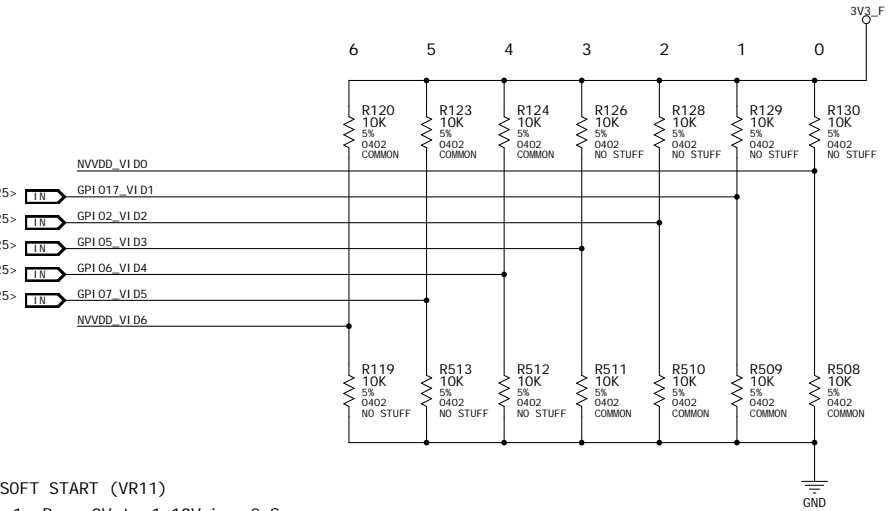
Input ripple ( $I_{rms}$ ) =  $\sim 0.9A @ 2.7A$





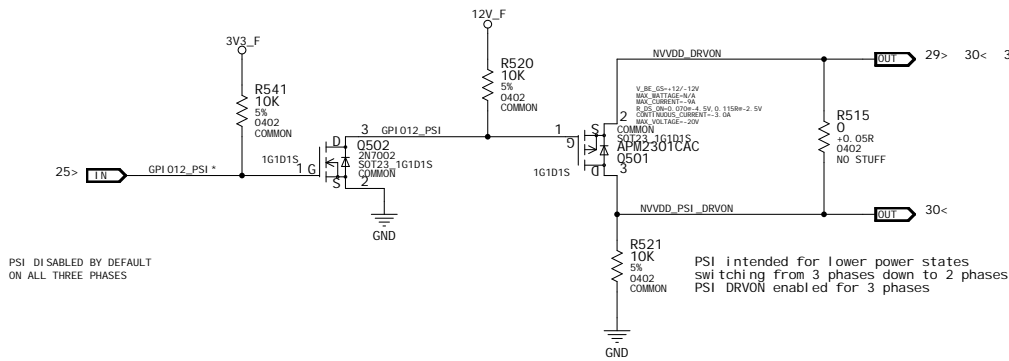


VID Table					
GPI 07	GPI 06	GPI 05	GPI 02	GPI 017	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V



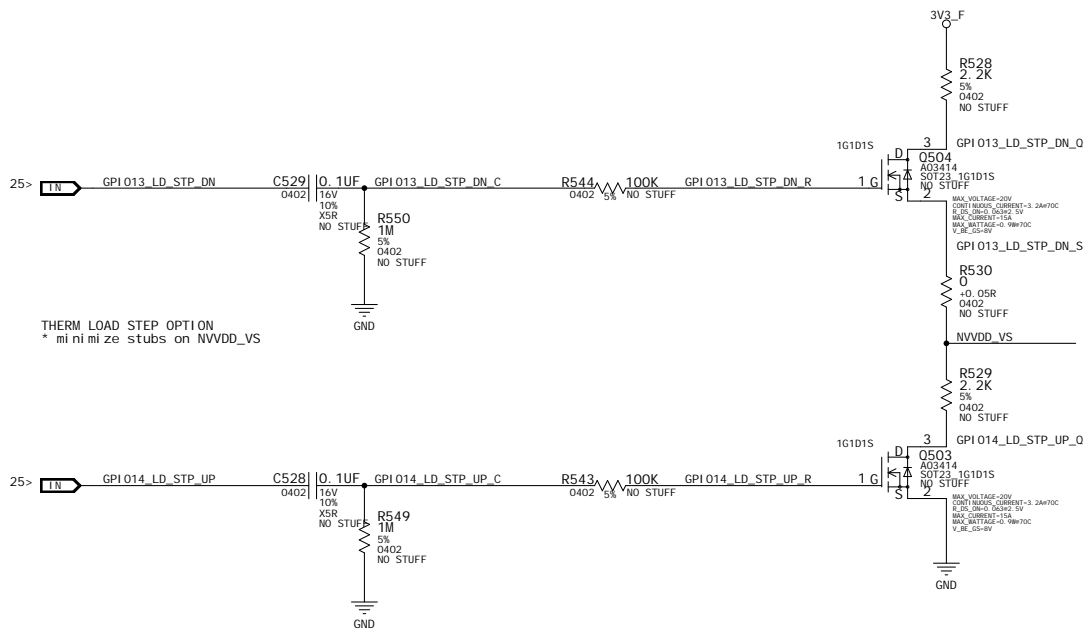
- SOFT START (VR11)
1. Ramp OV to 1.10V in ~2mS
  2. Hold at 1.10V for 170uS
  3. Read VID
  4. VID set to 0.9V during GPIO tri-state  
VID[5:1]=11000 to set 0.9125V

- P-STATE VOLTAGES
1. P0 at 1.05V
  2. P8/P12 at 0.80V

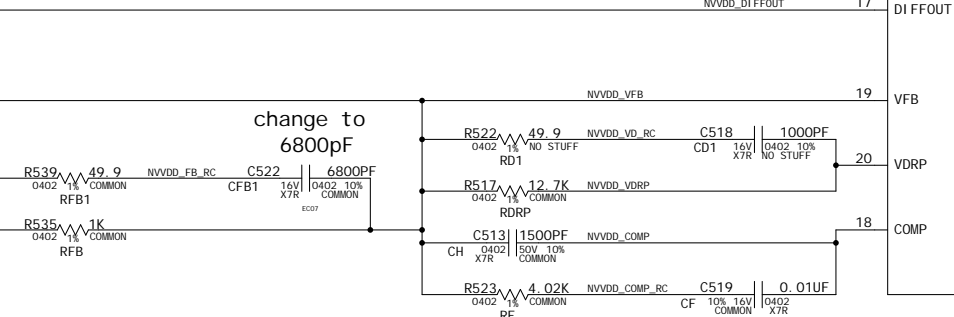


PSI DISABLED BY DEFAULT ON ALL THREE PHASES

PSI intended for lower power states  
Switching from 3 phases down to 2 phases  
PSI DRVON enabled for 3 phases

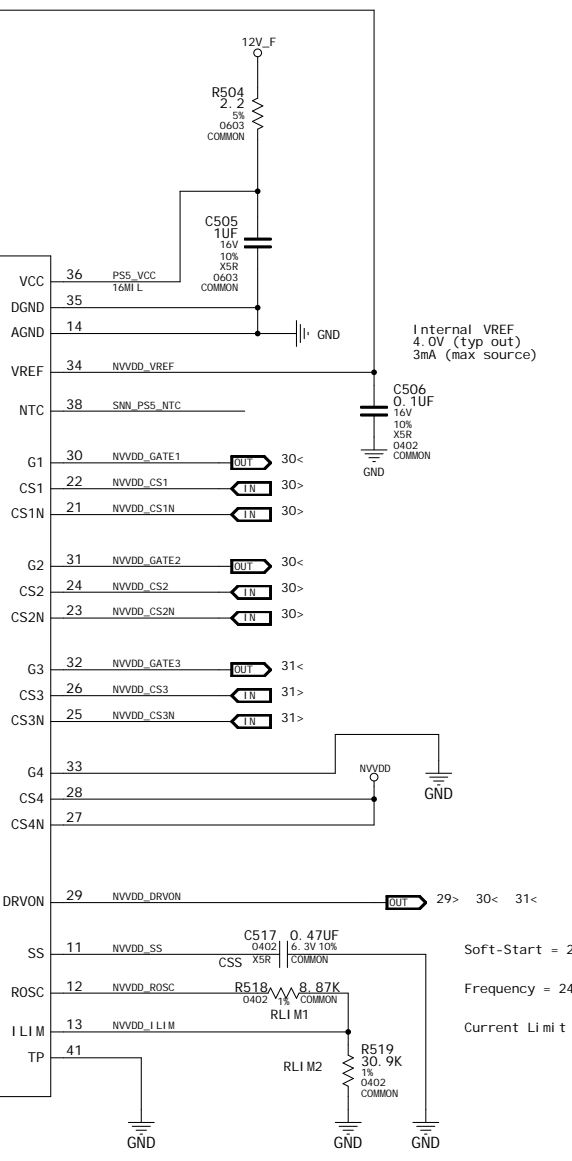


Vset offset option  
\* do not populate



Updated compensation 09/02, per P1025 analysis, phase margin

- RFB1 to 232 ohm
- CFB1 to 22nF
- RF to 464 ohm
- CF to 0.1uF
- CH to 3300pF



Internal VREF  
4.0V (typ out)  
3mA (max source)

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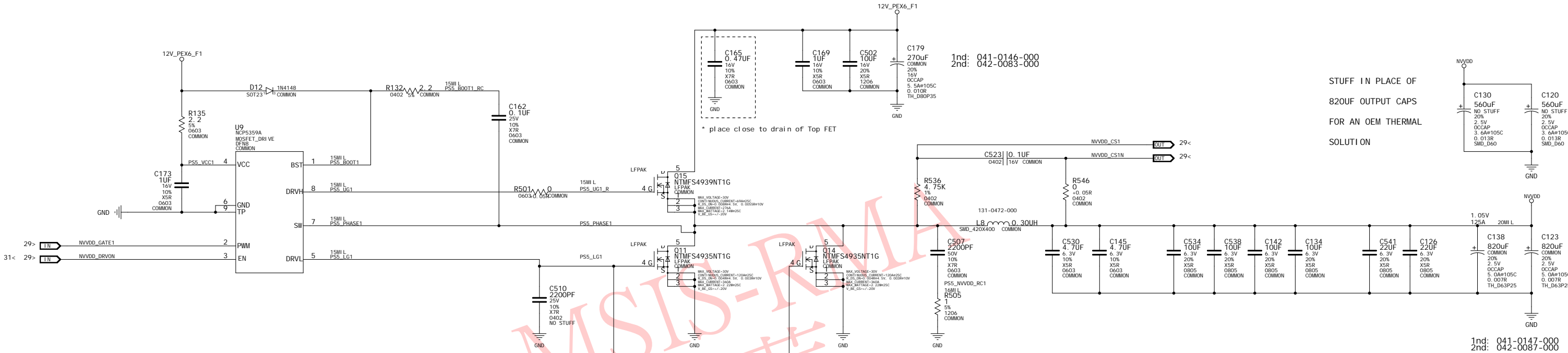
PAGE

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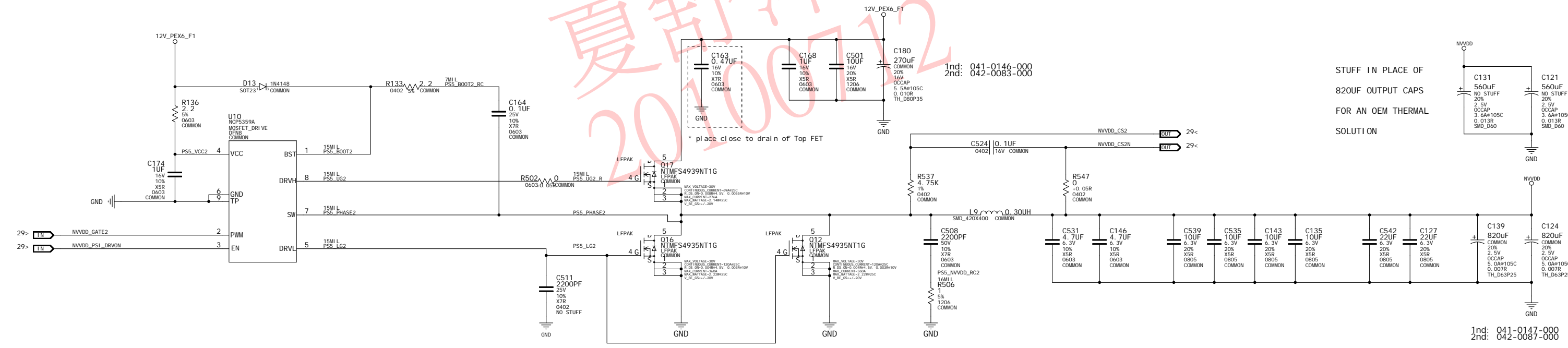
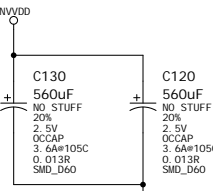
DATE

12-MAY-2010

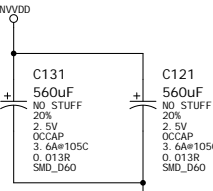
Input ripple (I<sub>rms</sub>)/phase = 10.175A @ 90A  
I<sub>rms</sub> shared across phase 1-2 input caps

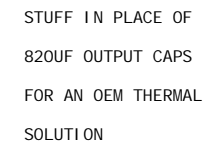


STUFF IN PLACE OF  
820UF OUTPUT CAPS  
FOR AN OEM THERMAL  
SOLUTION

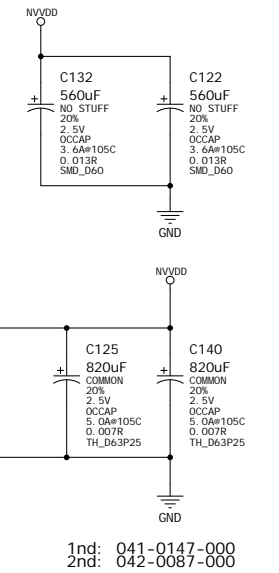


STUFF IN PLACE OF  
820UF OUTPUT CAPS  
FOR AN OEM THERMAL  
SOLUTION



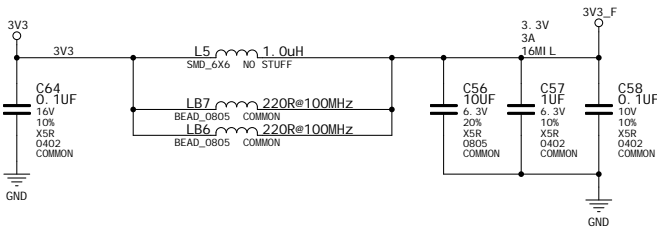


STUFF IN PLACE OF  
820UF OUTPUT CAPS  
FOR AN OEM THERMAL  
SOLUTION



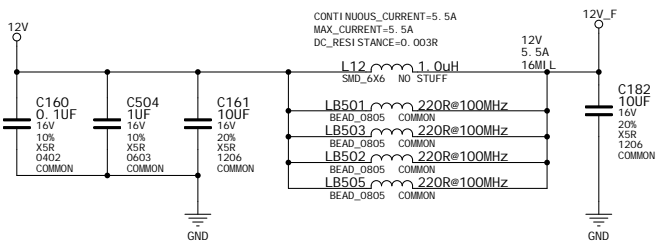
1

PEX 3V3 INPUT - 10W



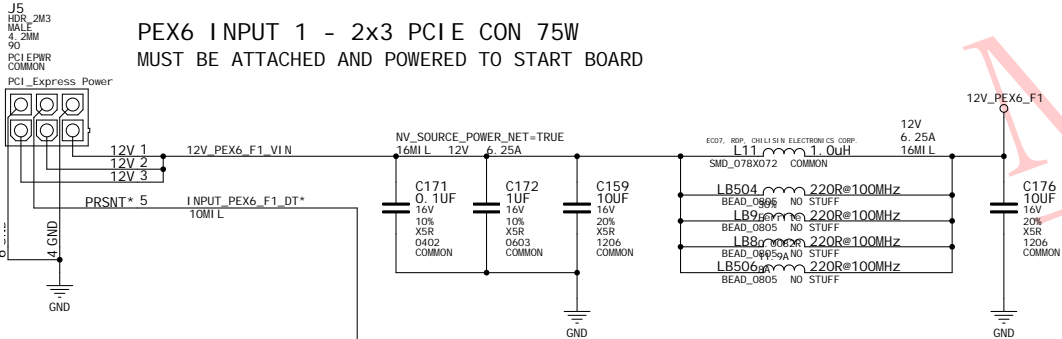
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PEX\_12V INPUT - 66W



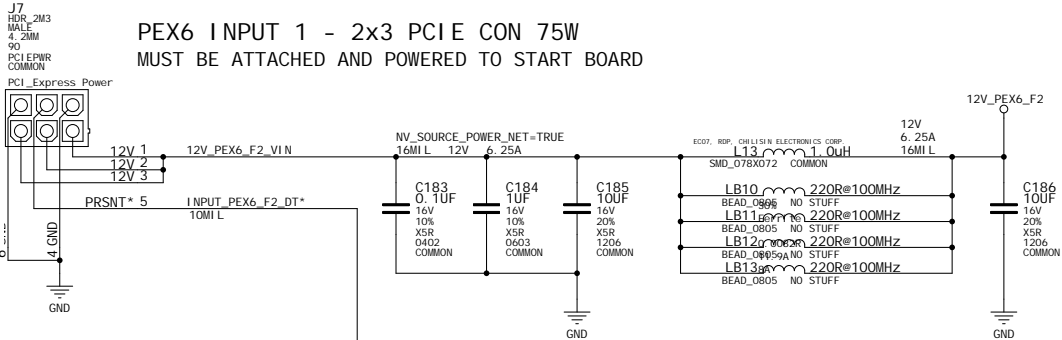
3

PEX6 INPUT 1 - 2x3 PCIe CON 75W  
MUST BE ATTACHED AND POWERED TO START BOARD



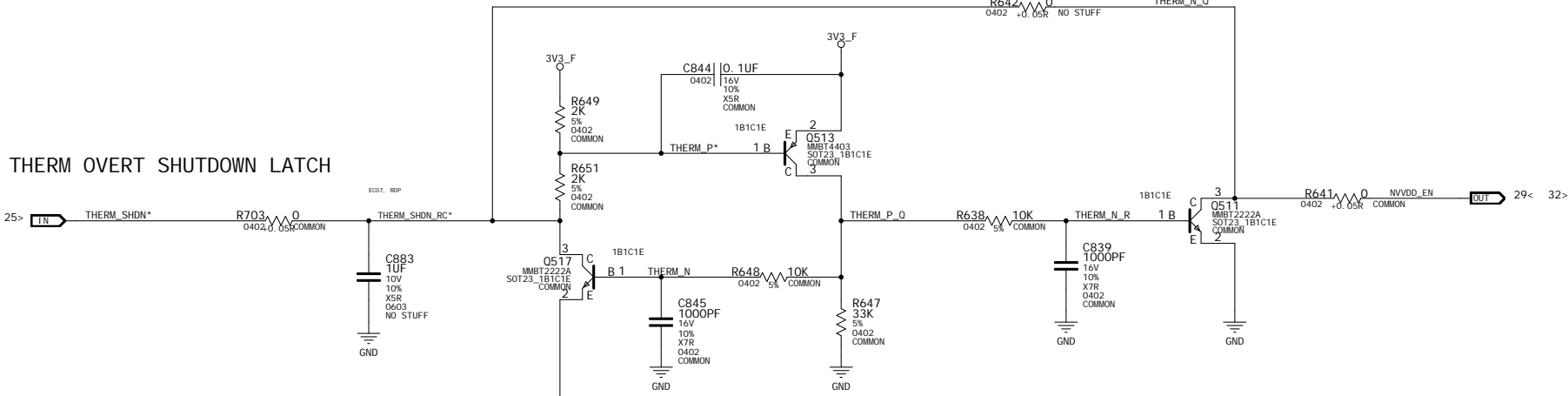
4

PEX6 INPUT 1 - 2x3 PCIe CON 75W  
MUST BE ATTACHED AND POWERED TO START BOARD

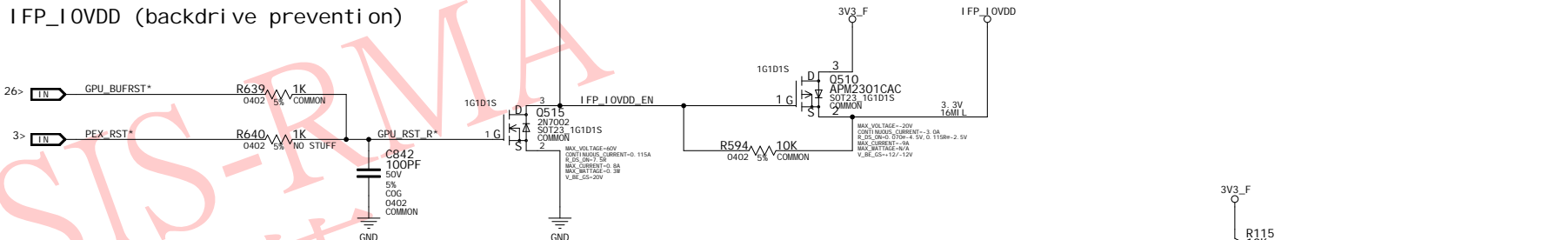


5

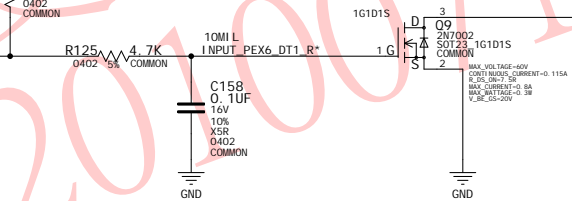
THERM OVERT SHUTDOWN LATCH



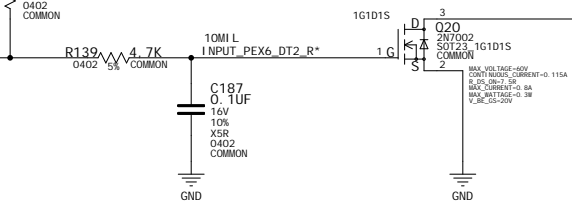
I FP\_I0VDD (backdrive prevention)



PEX Input Present 1



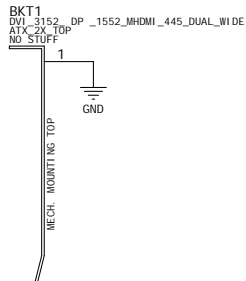
PEX Input Present 1



STUFF IF ONLY  
ONE 6-PIN POWER  
CONNECTOR IS USED

Brackets:

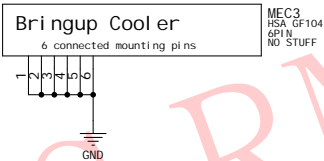
Bracket with DVI\_DP\_mHDMI : 151-10001-0355-071



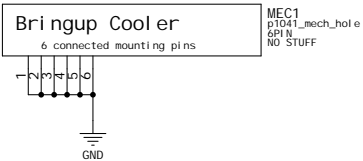
Bracket Screw



Cooler/GPU Sti ffener



P1041 MOUNTING HOLE LOCATIONS



MSIS-RMA  
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20100712



A		B		C		D		E		F		G		H	
Page34:  Bl ank															
1															
2															
3															
4															
5															

ASSEMBLY

PAGE DETAIL

P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI

<edit here to insert page detail>

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DATE

12-MAY-2010

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