

PG161-A00

TU106 6GB GDDR6, 192b, X16  
DVI-D/DP + DP + HDMI

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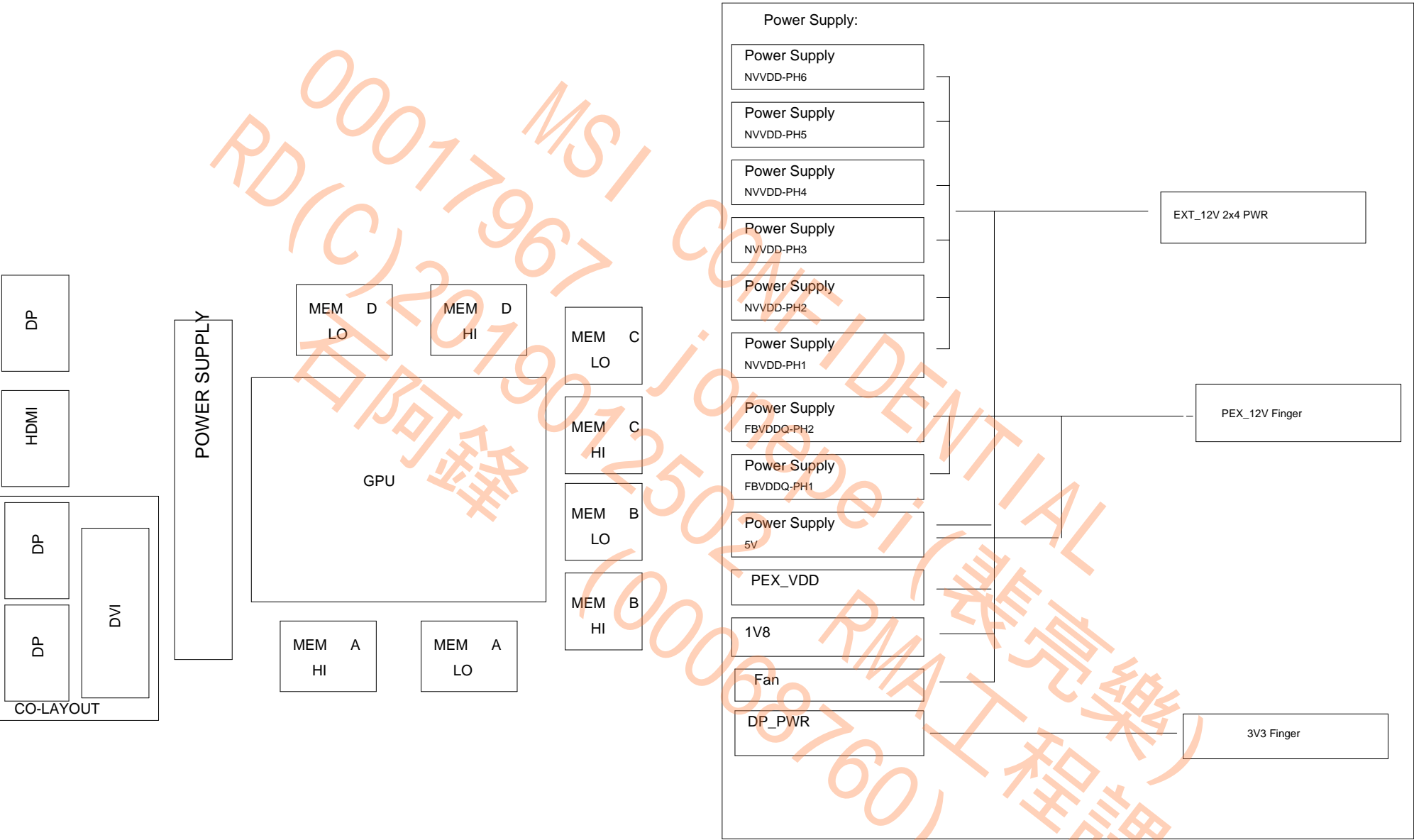
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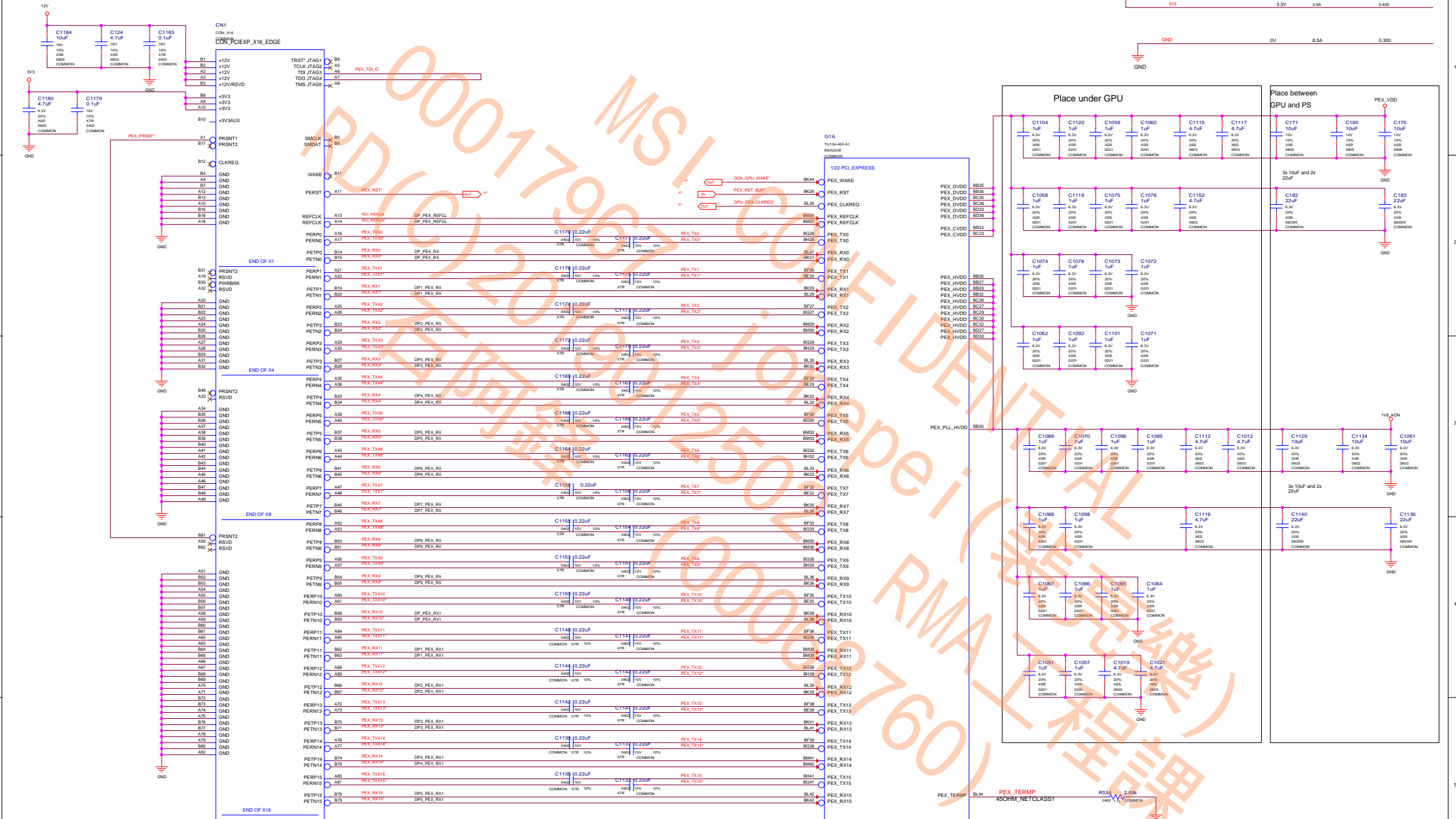
Page Description

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|----|----------------|
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V375-20  
1. 移除 CO-LAY  
2. Core Power: uP9512SQKI (QFN 4x4) + (NCP302045 x 4)  
Memory Power: I32-S725602-N03 + (UBIQ 3103+3107\*2)  
3. P.34 add R779  
4. P.30 & 44 移除PS\_FBVDD\_BUFF換頁符號  
換 FBVDD controller · 換成1PHASE 上1下2  
5. P.52 add HDMI & DVI 螺絲  
6. IO 換常用料 · footprint 不變



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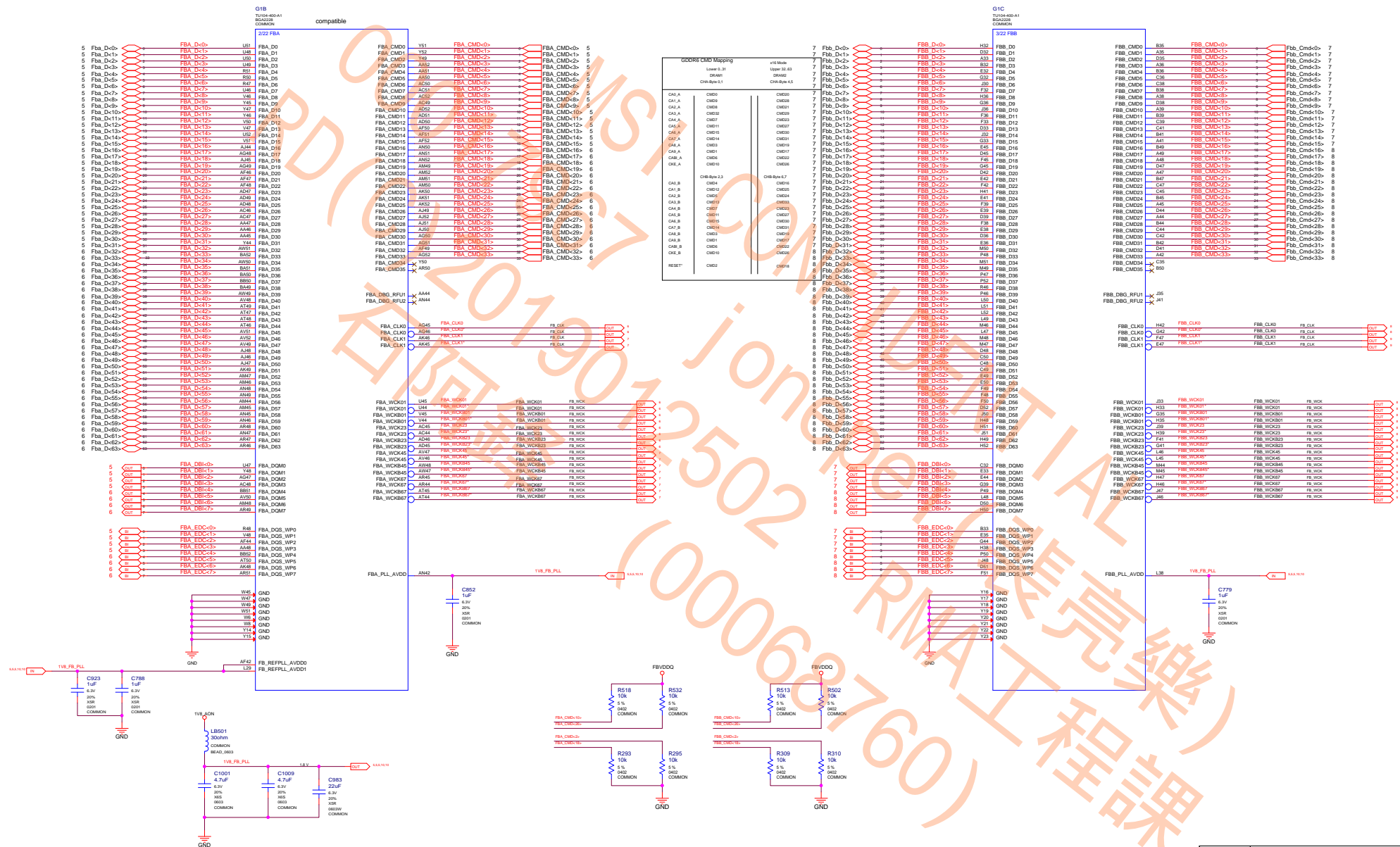
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DELETE RC TERMINATIONS

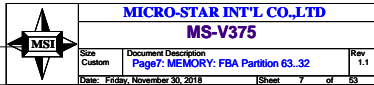
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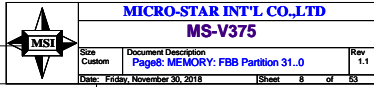
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| MS-V375                         |                      |               |
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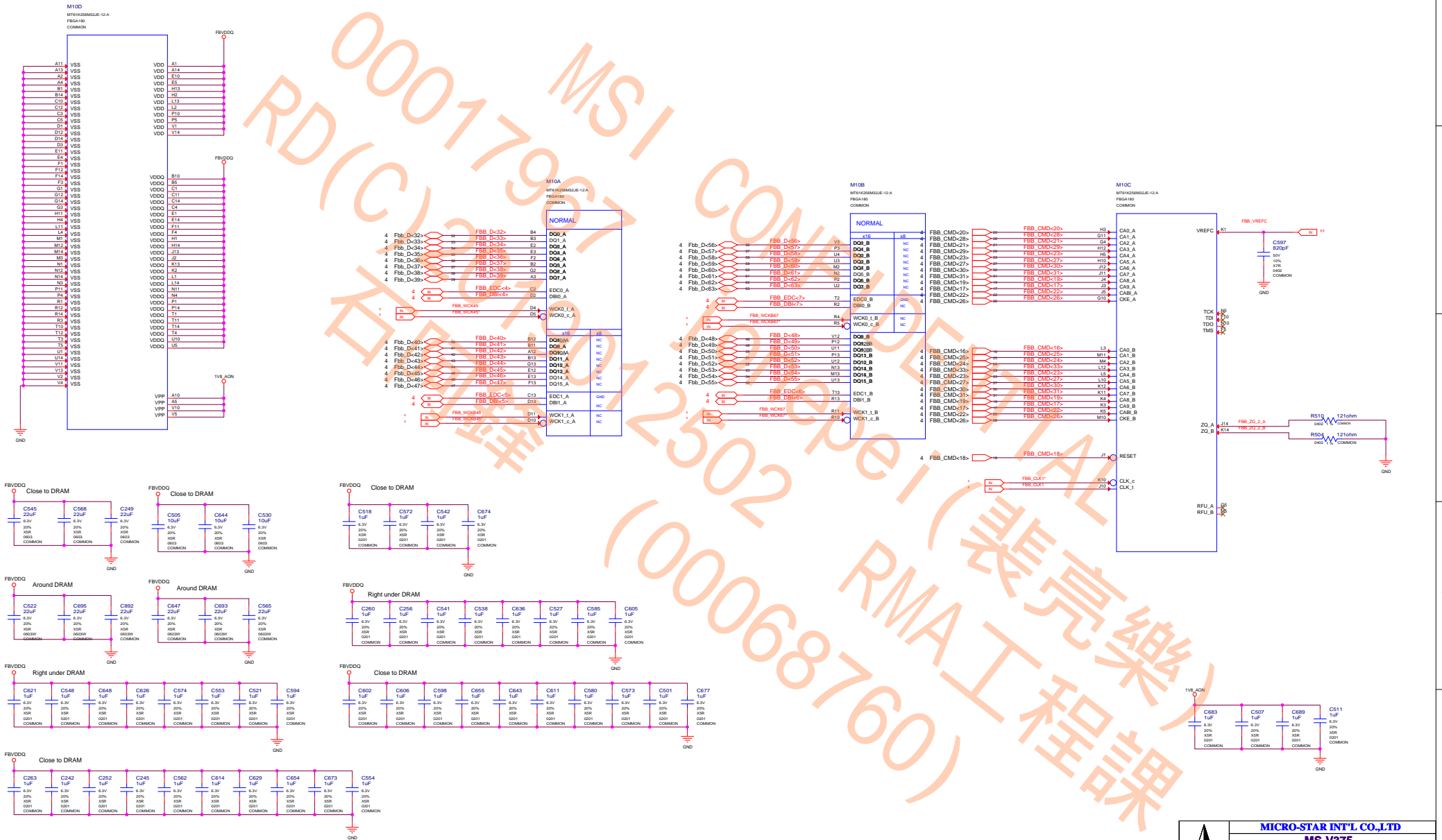




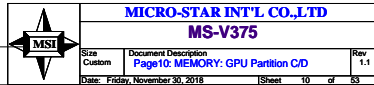


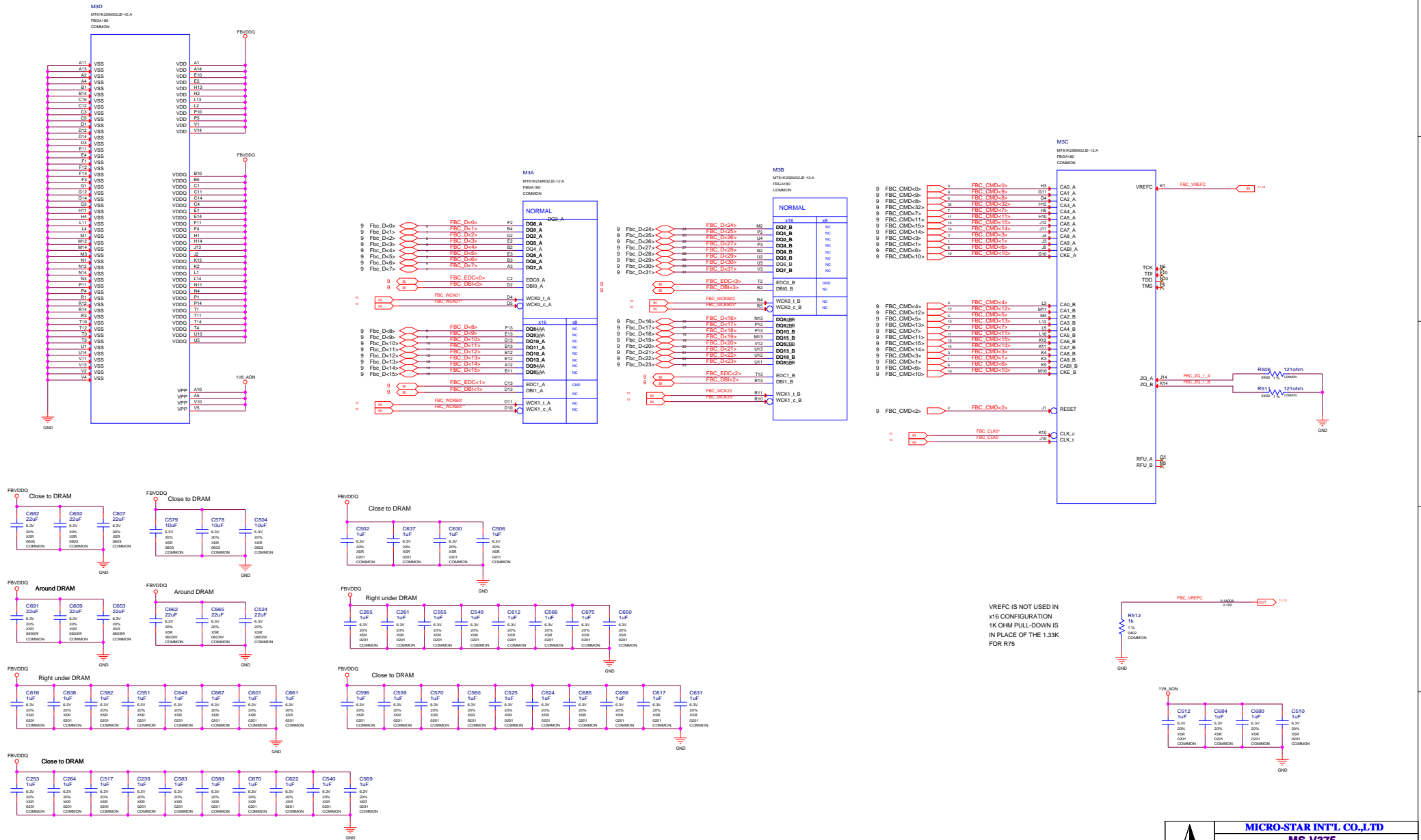




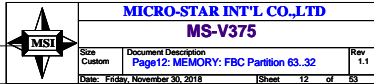


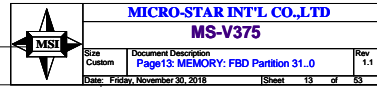
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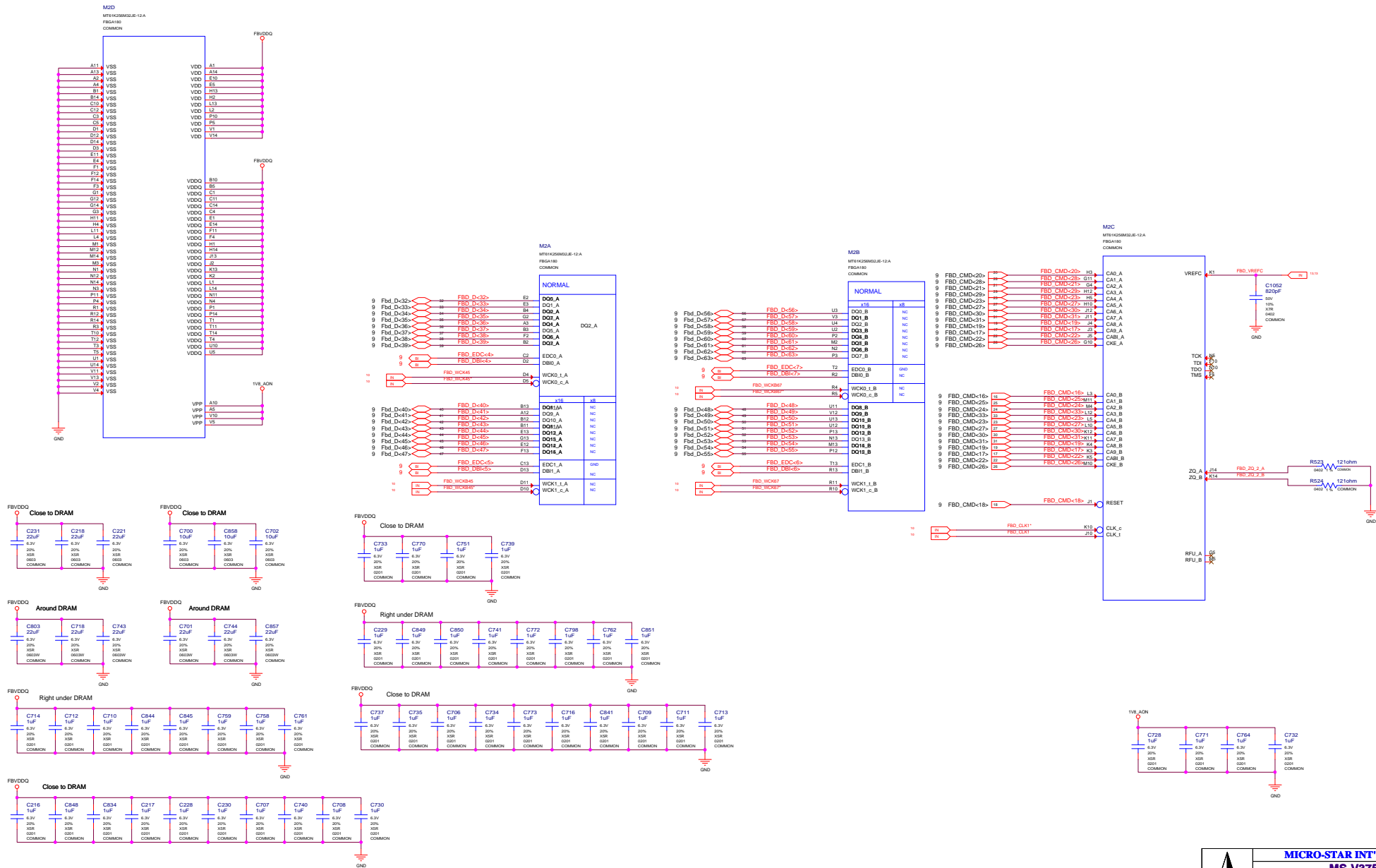




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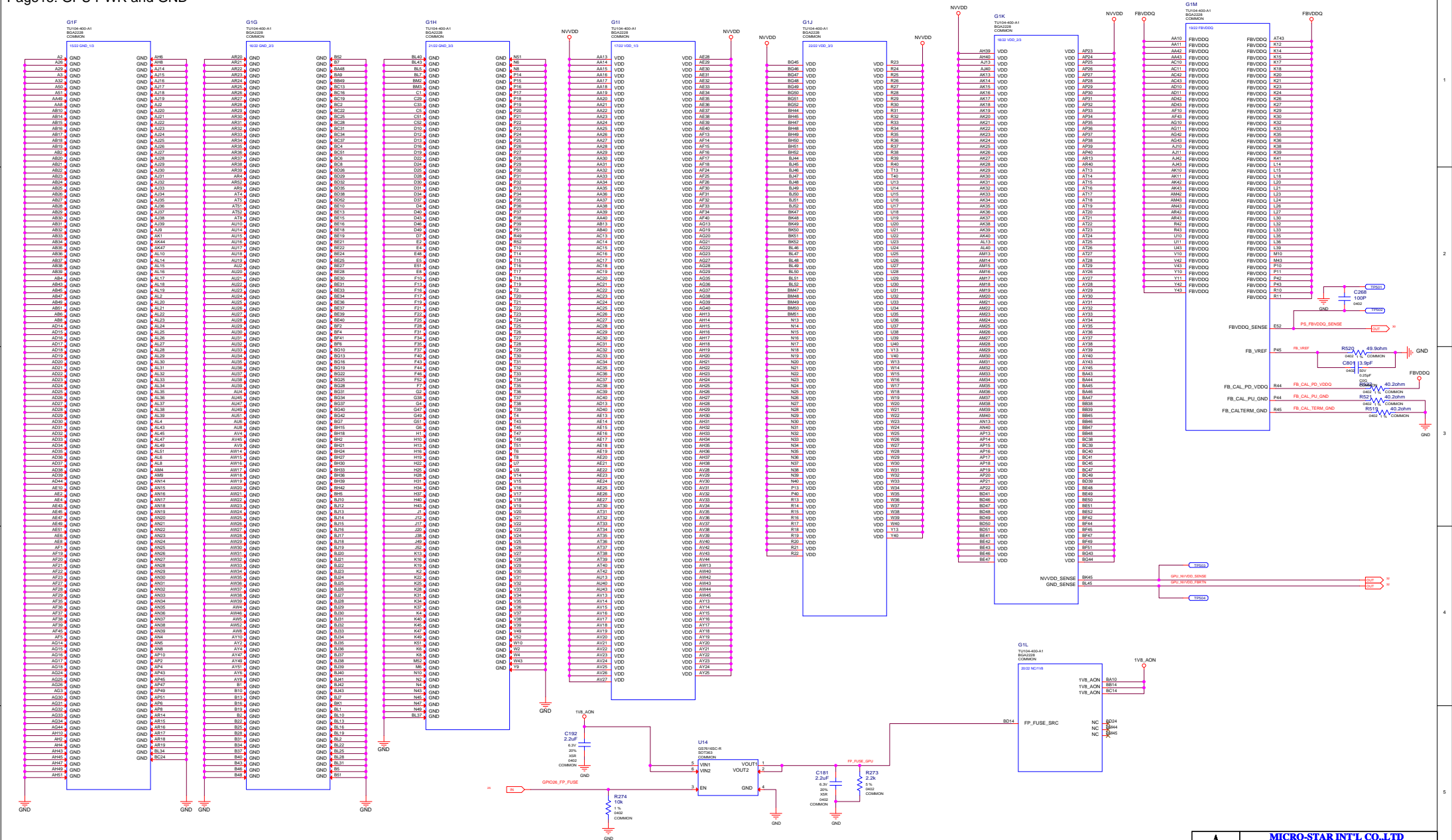


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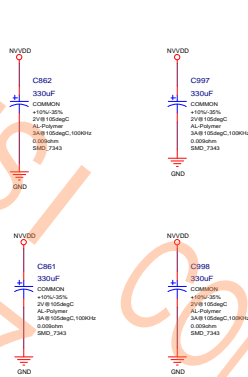
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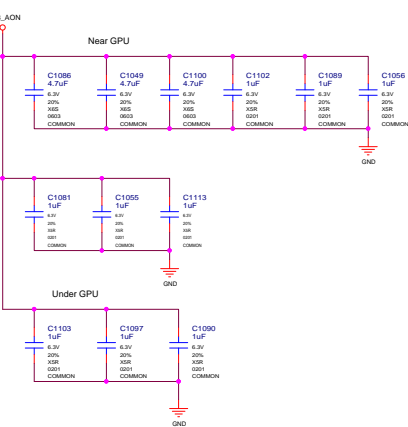
FBVDDQ



NVVDD

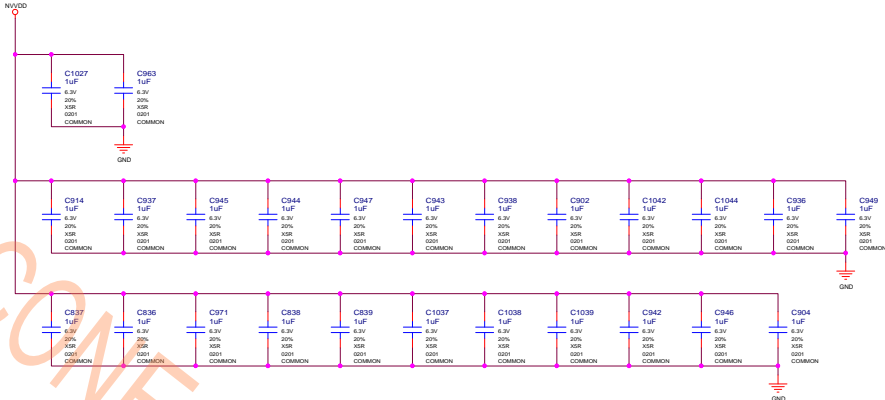


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NVDD

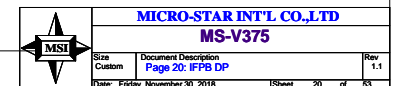


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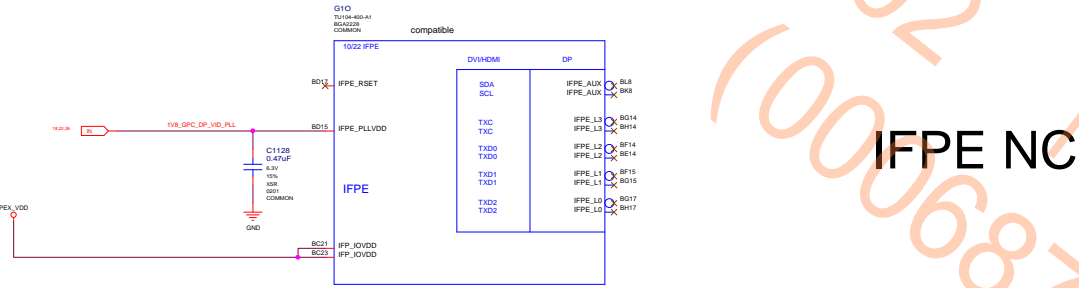
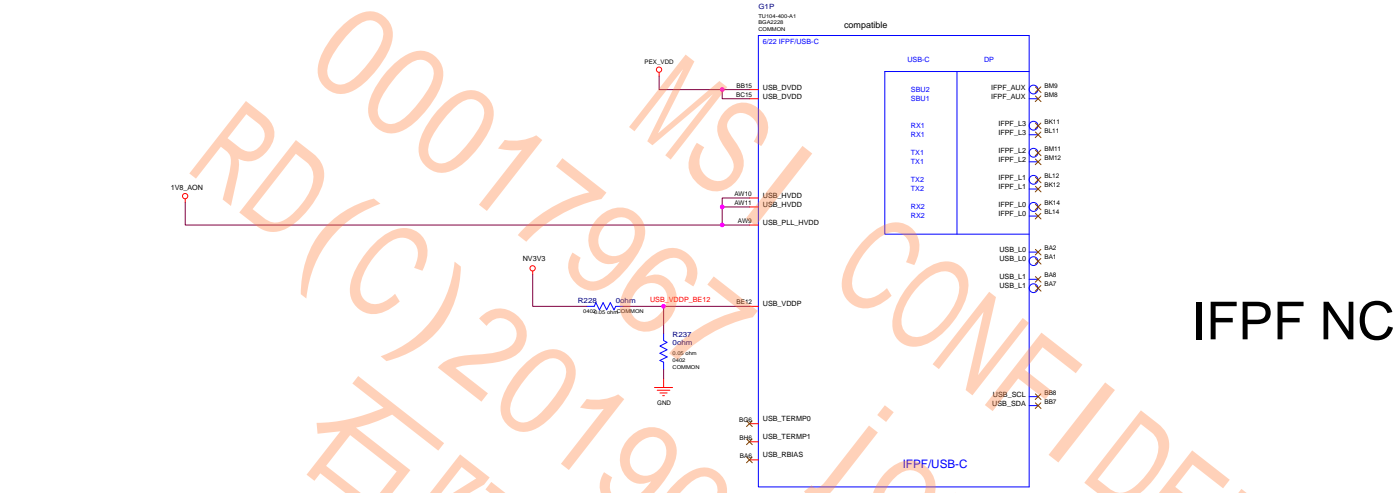
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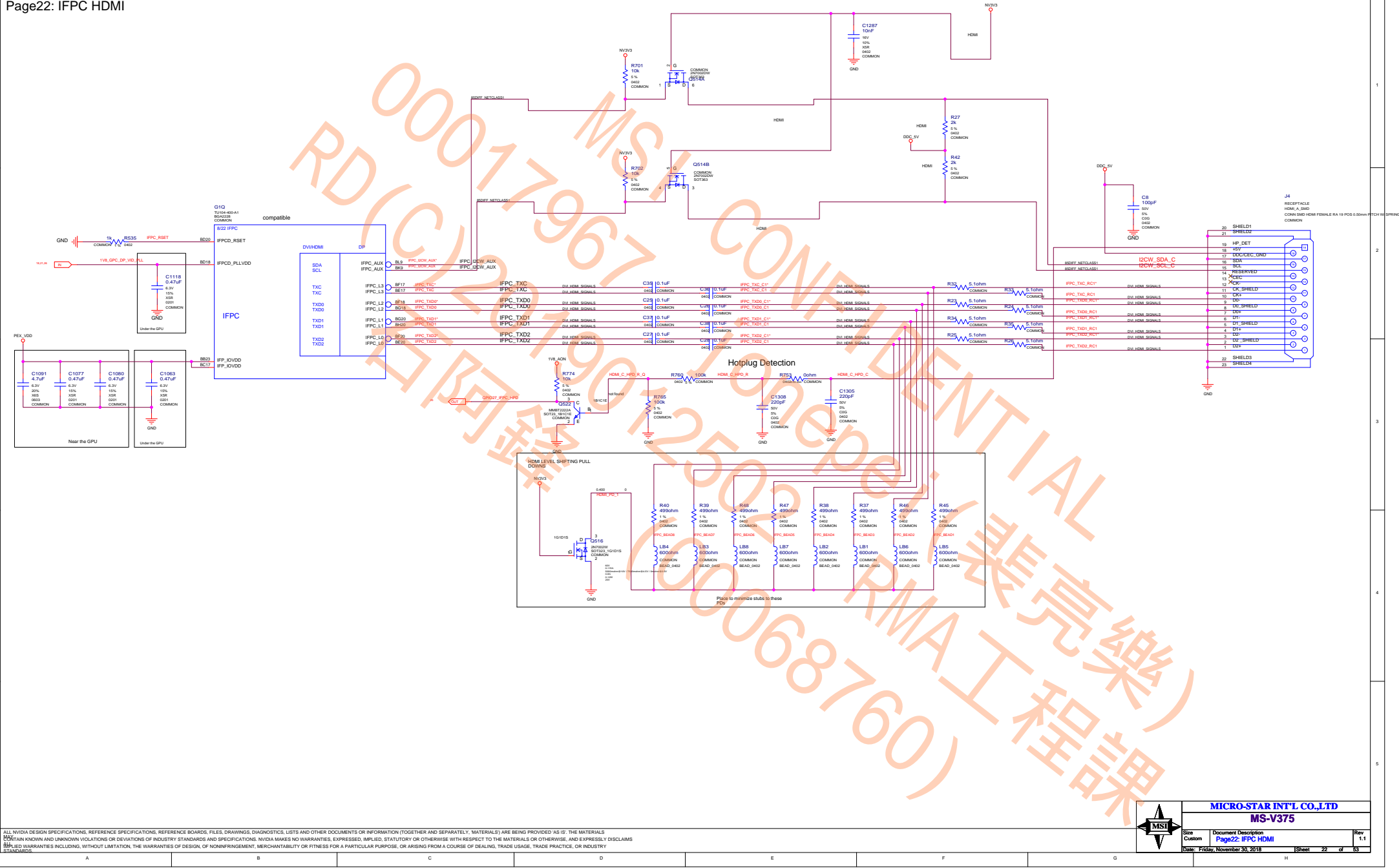


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| Size<br>Custom                  | Document Description<br><b>Page 20: IFPB DP</b> | Rev<br>1.1     |
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ID: IFPE & IFPF USB-C NC



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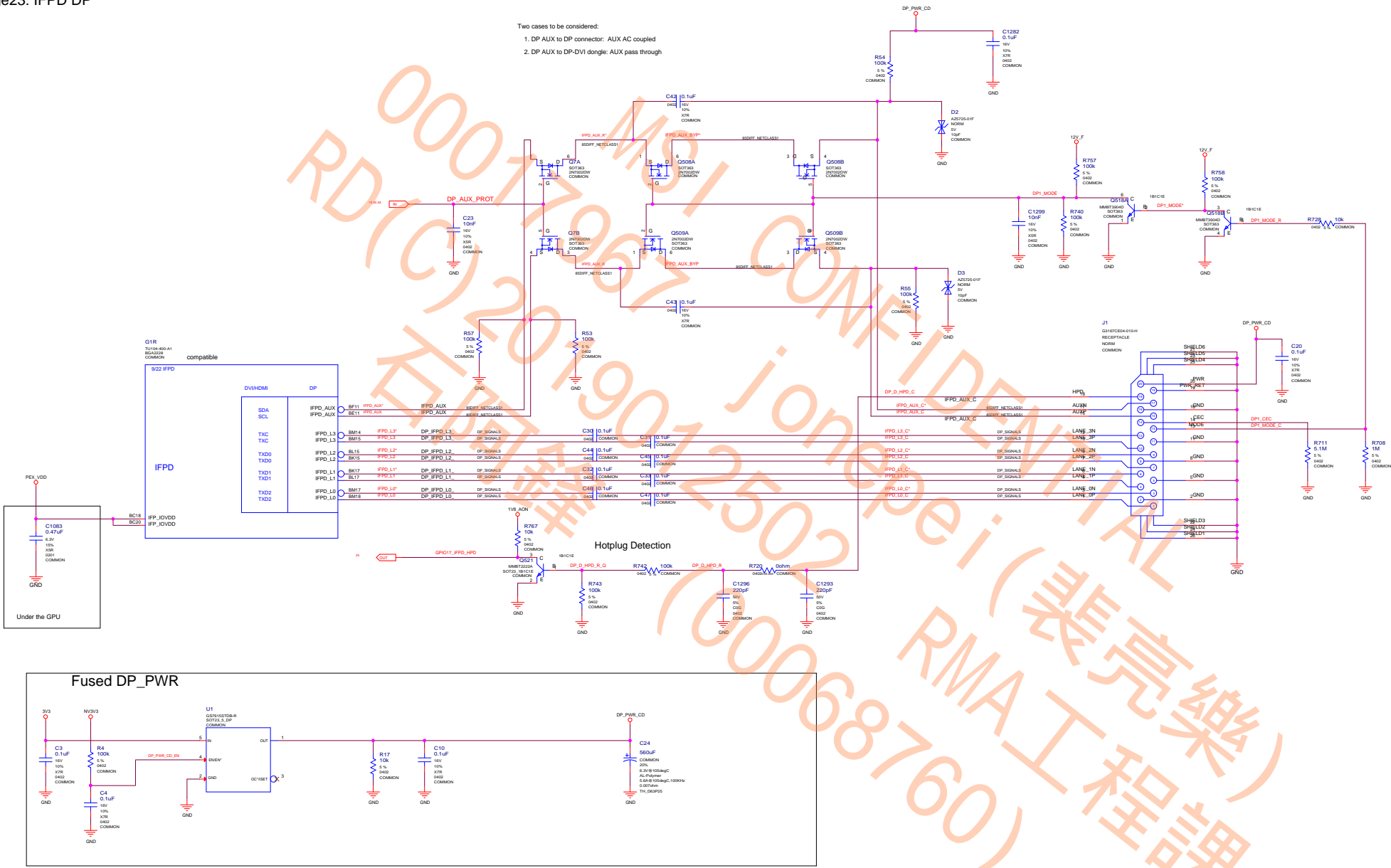
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| Rev                             | Document Description | Rev |
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| 1.1                             | Page22: IFPC-HDMI    | 1.1 |
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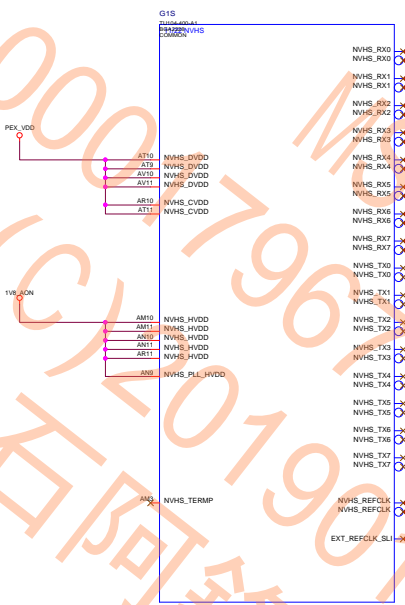


Two cases to be considered:  
1. DP AUX to DP connector: AUX AC coupled  
2. DP AUX to DP-DVI dongle: AUX pass through

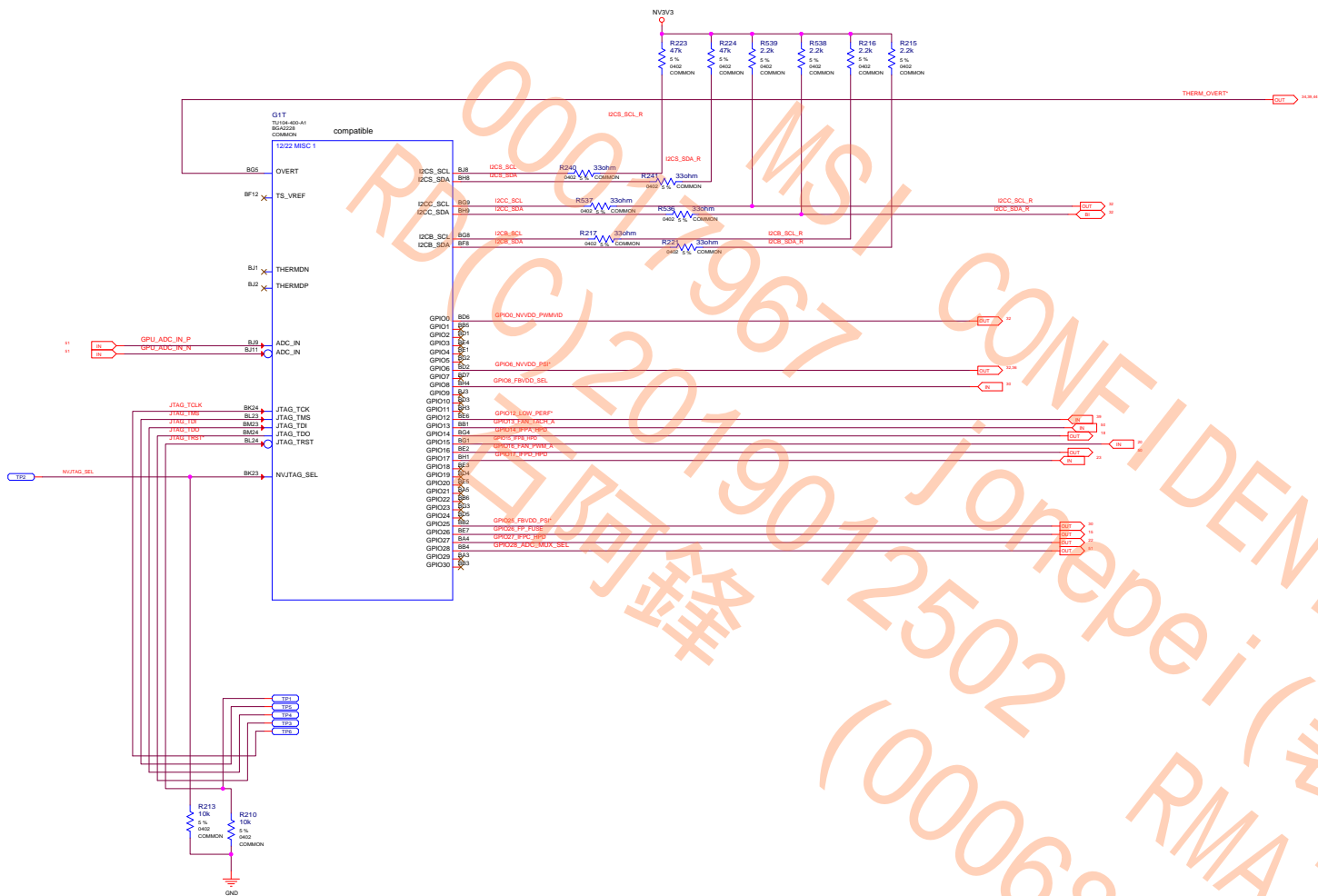


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| STRAP2 | STRAP1 | STRAP0 | RAMCFG[4:0] |
|--------|--------|--------|-------------|
| L      | L      | L      | 00000       |
| L      | L      | H      | 00001       |
| L      | H      | L      | 00010       |
| L      | H      | H      | 00011       |
| H      | H      | L      | 00110       |
| H      | H      | H      | 00111       |
| L      | L      | M      | 01000       |

| RAMCFG[4:0] | DENSITY | WIDTH   | VENDOR  | DIE |
|-------------|---------|---------|---------|-----|
| 00000       | 8Gb     | 256-bit | Samsung | C   |
| 00001       | 8Gb     | 256-bit | Micron  | A   |
| 00010       | 8Gb     | 256-bit | Hynix   | M   |
| 00011       | 8Gb     | 256-bit | Samsung | C   |
| 00100       | 8Gb     | 256-bit | Micron  | A   |
| 00101       | 8Gb     | 256-bit | Hynix   | M   |
| 00110       | 16Gb    | 256-bit | Samsung | M   |
| 00111       |         |         |         |     |

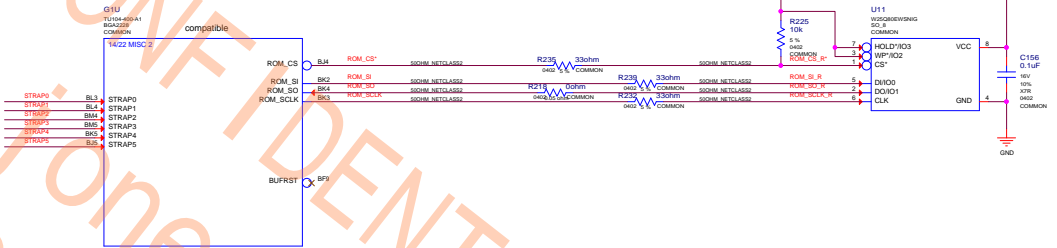
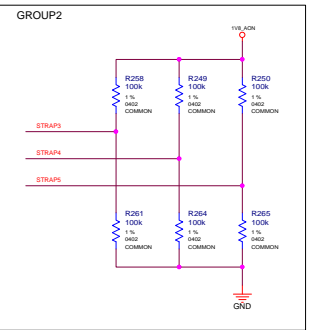
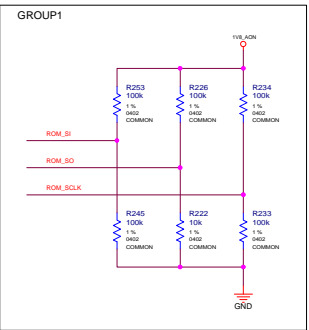
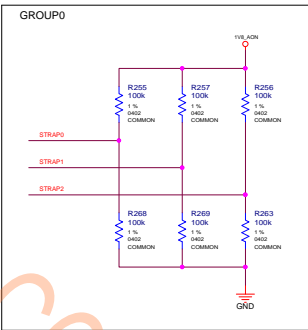
| ROM_SO | ROM_SI | ROM_SCLK | DUMMY[2:0].FS_OVERT | 1:ENABLE 0:DISABLE | DEFAULT |
|--------|--------|----------|---------------------|--------------------|---------|
| L      | L      | L        | XXX1                | FS_OVERT ENABLE    |         |
| L      | L      | M        | XXX0                | FS_OVERT DISABLE   |         |

| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |
|--------|--------|--------|--------------|-----------|----------|------------|
| M      | H      | H      | 1            | 1         | 1        | 1          |
| M      | H      | L      | 1            | 1         | 1        | 0          |
| M      | L      | H      | 1            | 1         | 0        | 1          |
| M      | L      | L      | 1            | 1         | 0        | 0          |
| L      | H      | M      | 1            | 0         | 1        | 1          |
| L      | M      | H      | 1            | 0         | 1        | 0          |
| L      | M      | L      | 1            | 0         | 0        | 1          |
| L      | L      | M      | 1            | 0         | 0        | 0          |
| H      | H      | H      | 0            | 1         | 1        | 1          |
| H      | H      | L      | 0            | 1         | 1        | 0          |
| H      | L      | H      | 0            | 1         | 0        | 1          |
| H      | L      | L      | 0            | 1         | 0        | 0          |
| L      | H      | H      | 0            | 0         | 1        | 1          |
| L      | H      | L      | 0            | 0         | 1        | 0          |
| L      | L      | H      | 0            | 0         | 0        | 1 DEFAULT  |
| L      | L      | L      | 0            | 0         | 0        | 0          |

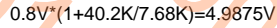
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

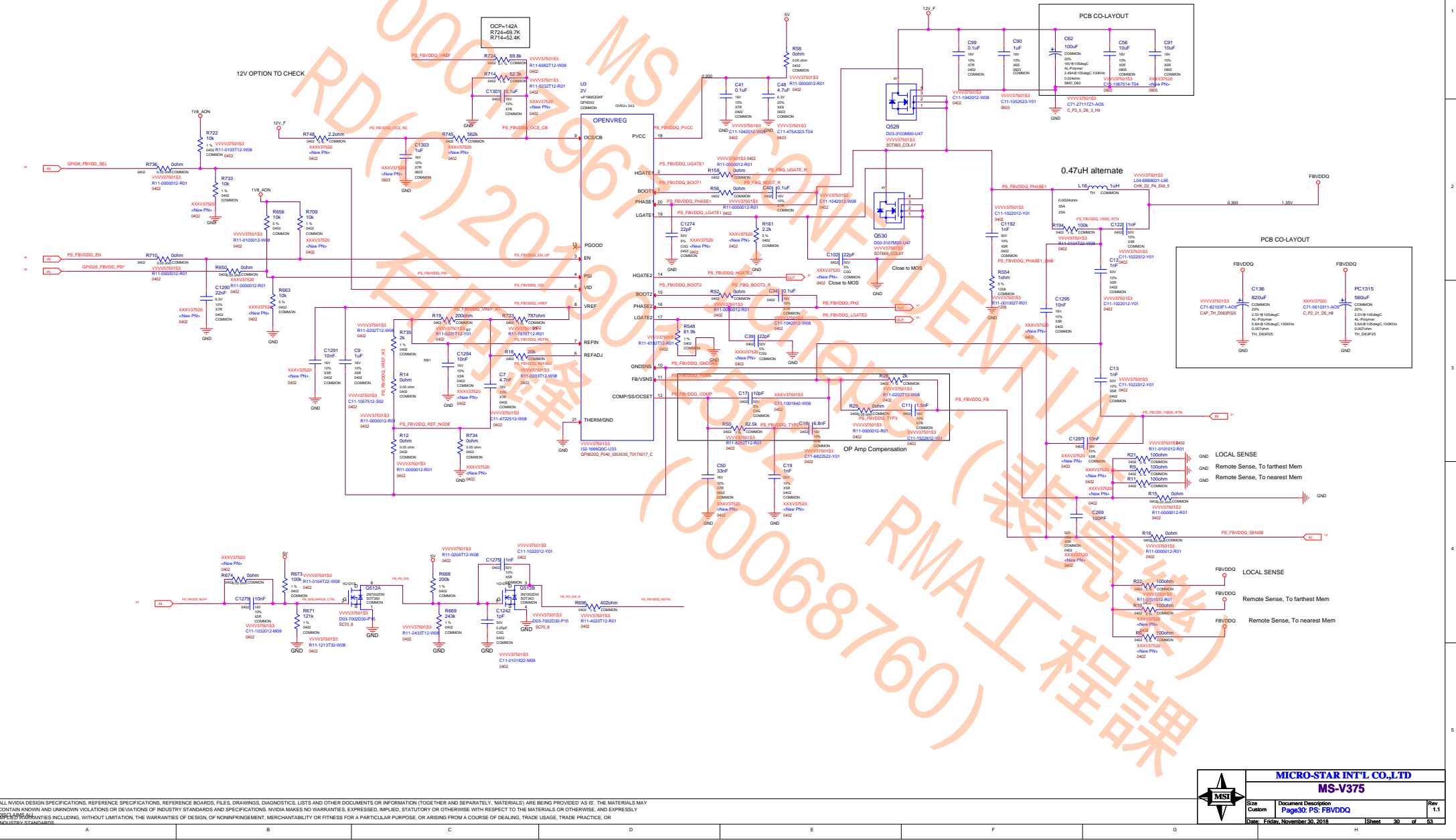


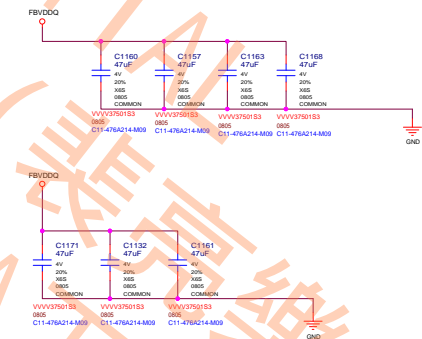
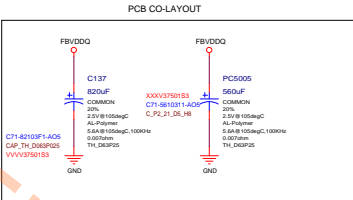
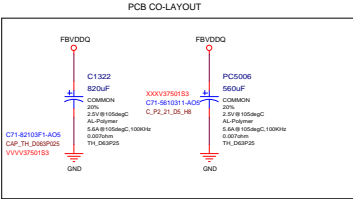
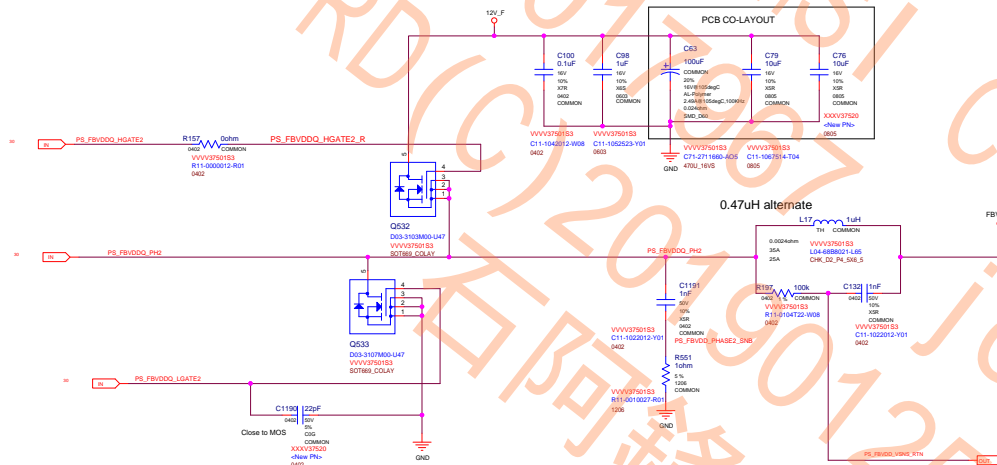




$$0.6V \cdot (1 + 10K/14.7K) = 1.008V$$





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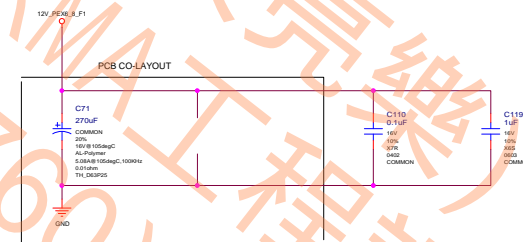


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DROP OVR3i SOLUTION

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| Custom                          | Page33: PS: NVVDD CTR OVR3i | 1.1            |
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| Size<br>Custom                  | Document Description<br><b>Page34: PS: NVDD PH6&amp;4</b> | Rev<br>1.1     |
| Date: Friday, November 30, 2018 |   | Sheet 34 of 53 |








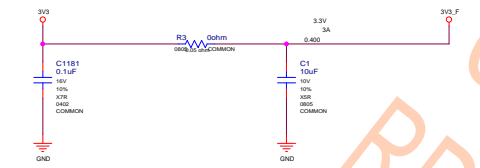
DELETE RAIL BALANCE CIRCUIT

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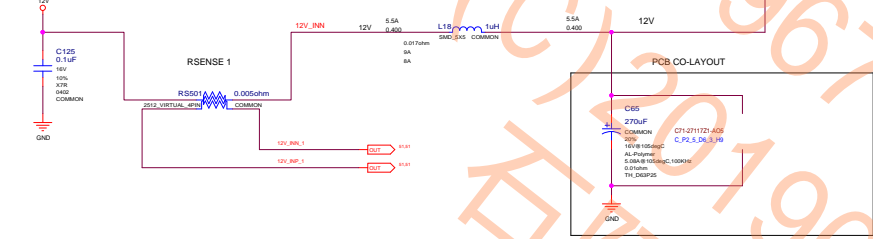
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| Custom  | Page37: Input Power Balancing Switcher | 1.1   |                          |       |
| Date: Friday, November 30, 2018   |  | Sheet | 37                       | of 53 |

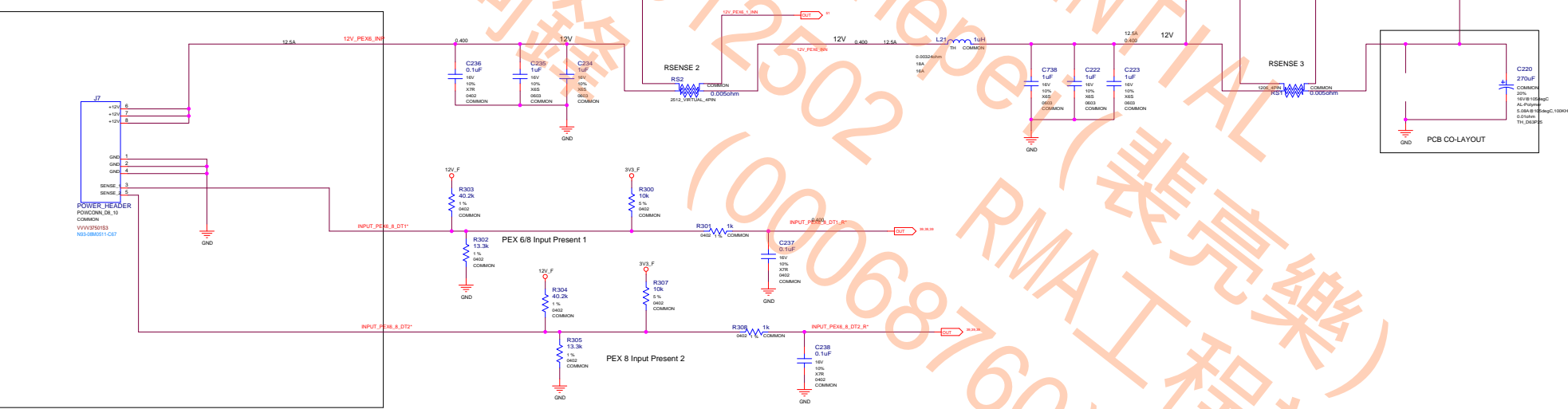
PEX 3V3 INPUT - 10W



PEX\_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIe CON 150W



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| Custom                          | Page40: BUCKBOOST    | 1.1            |
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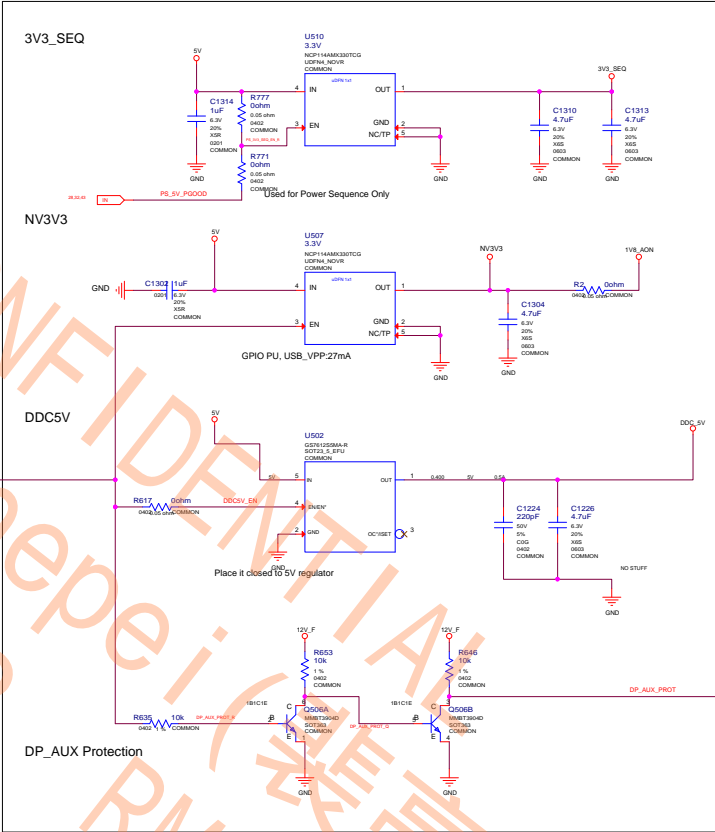
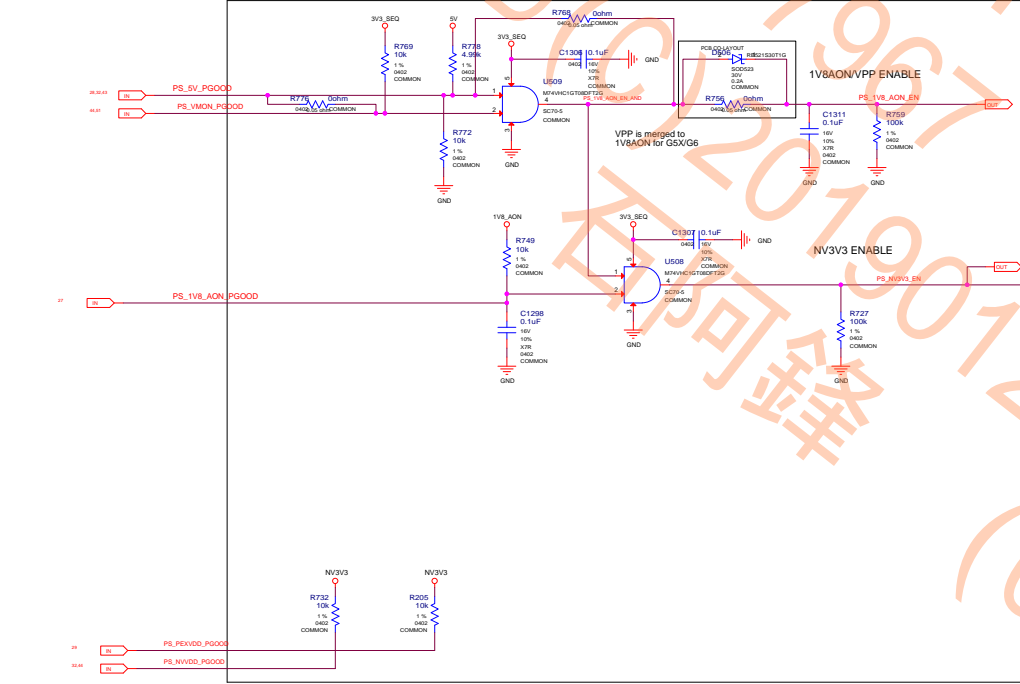
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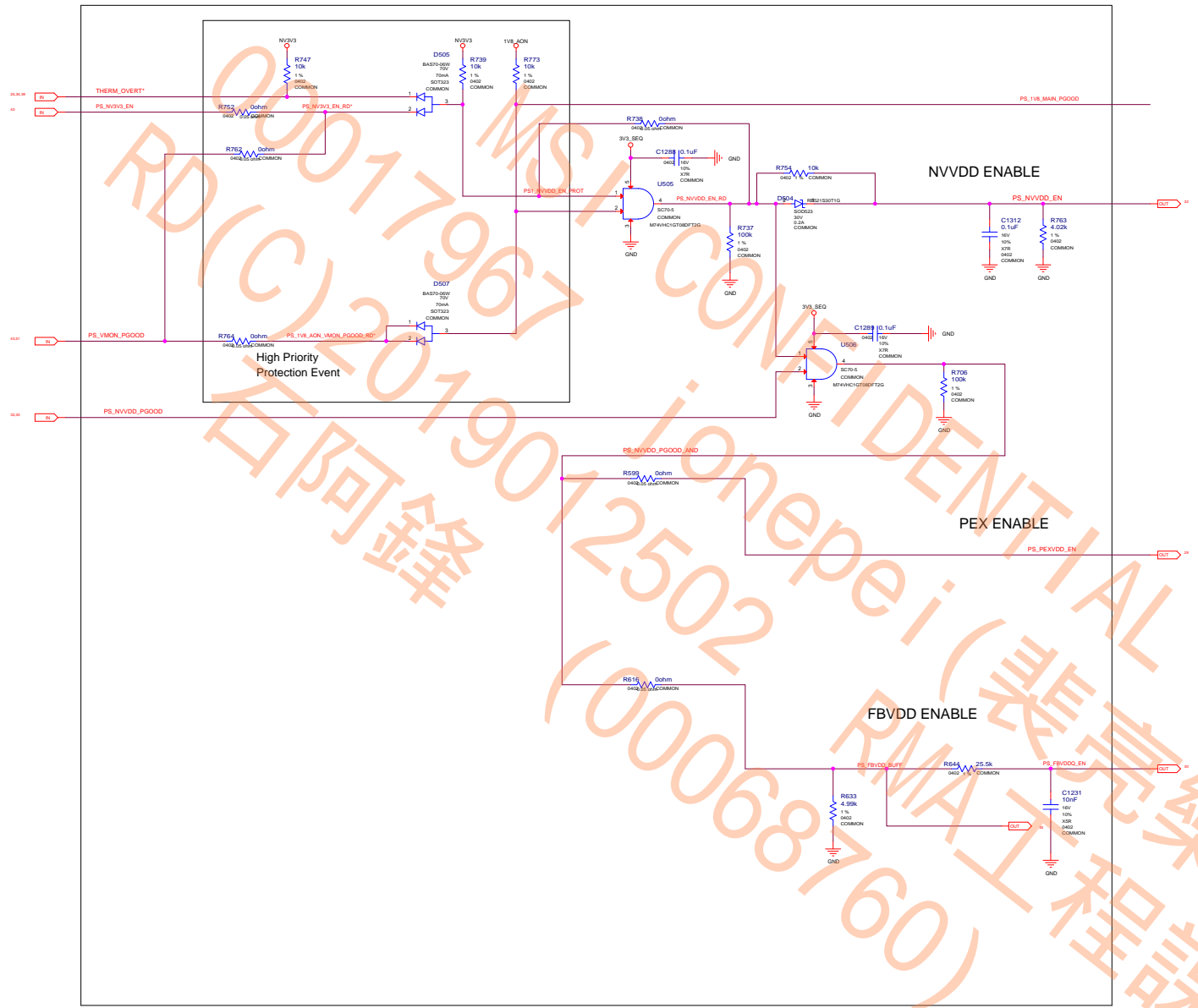
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| Custom                          | Page42: 12V & 3V3_A SWITCHER | 1.1            |
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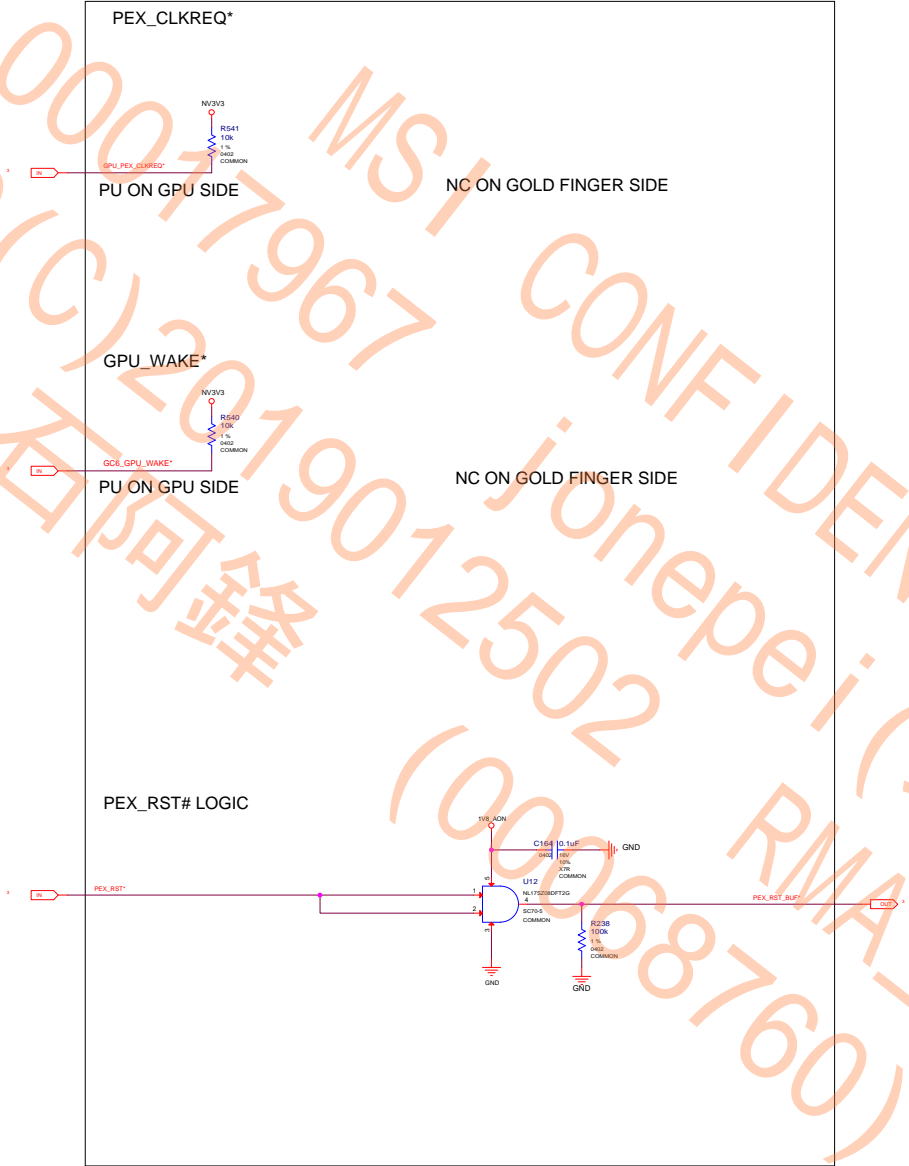
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| Size                            | Document Description             | Rev            |
| Custom                          | Page45: SEQUENCE:Voltage Monitor | 1.1            |
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| Custom                          | Page46: SEQUENCE:Discharge | 1.1            |
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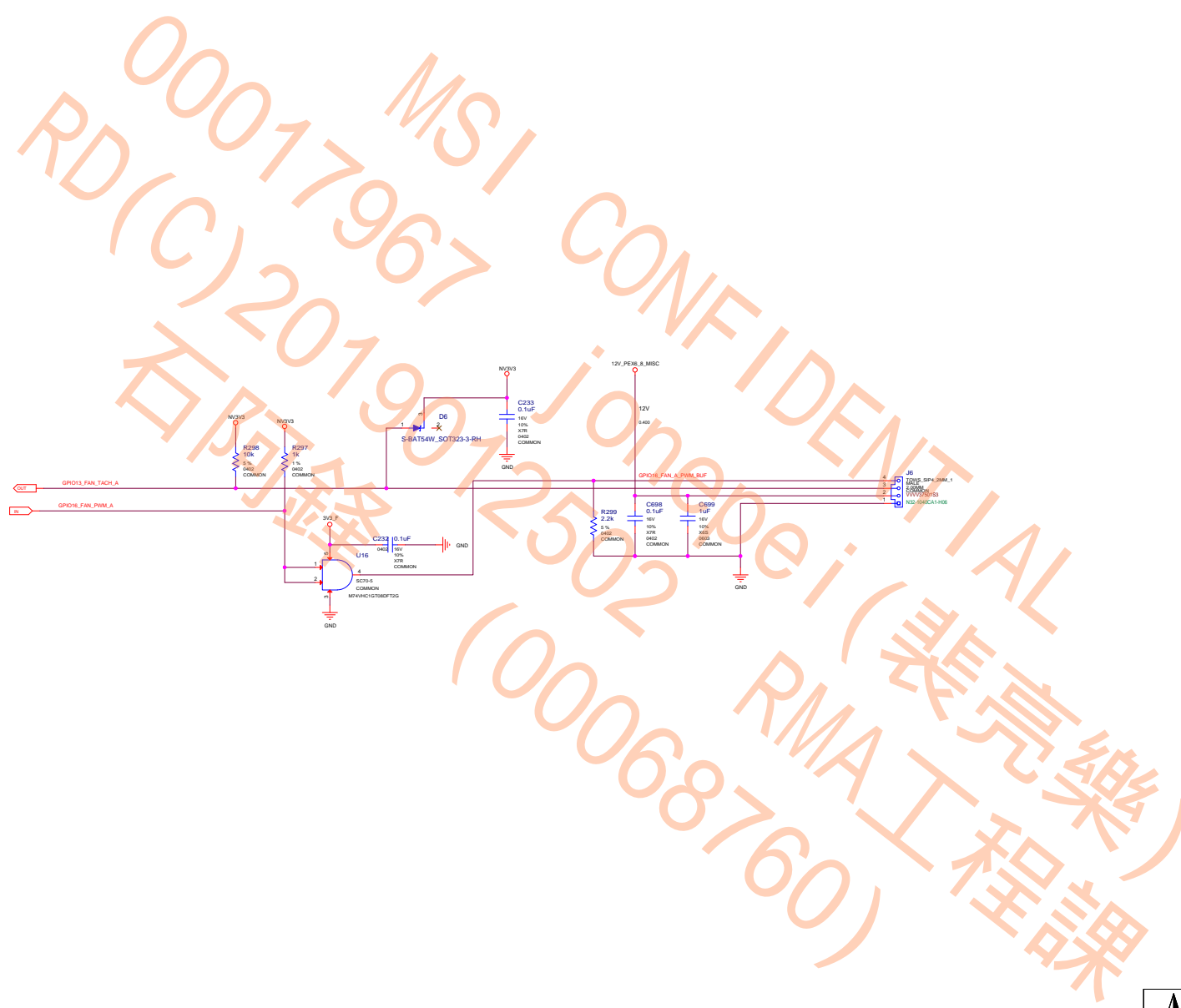
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| Custom                          | Page48: LOGO LED     | 1.1              |
| Date: Friday, November 30, 2018 |                      | (Sheet 48 of 53) |

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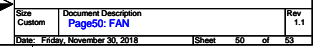
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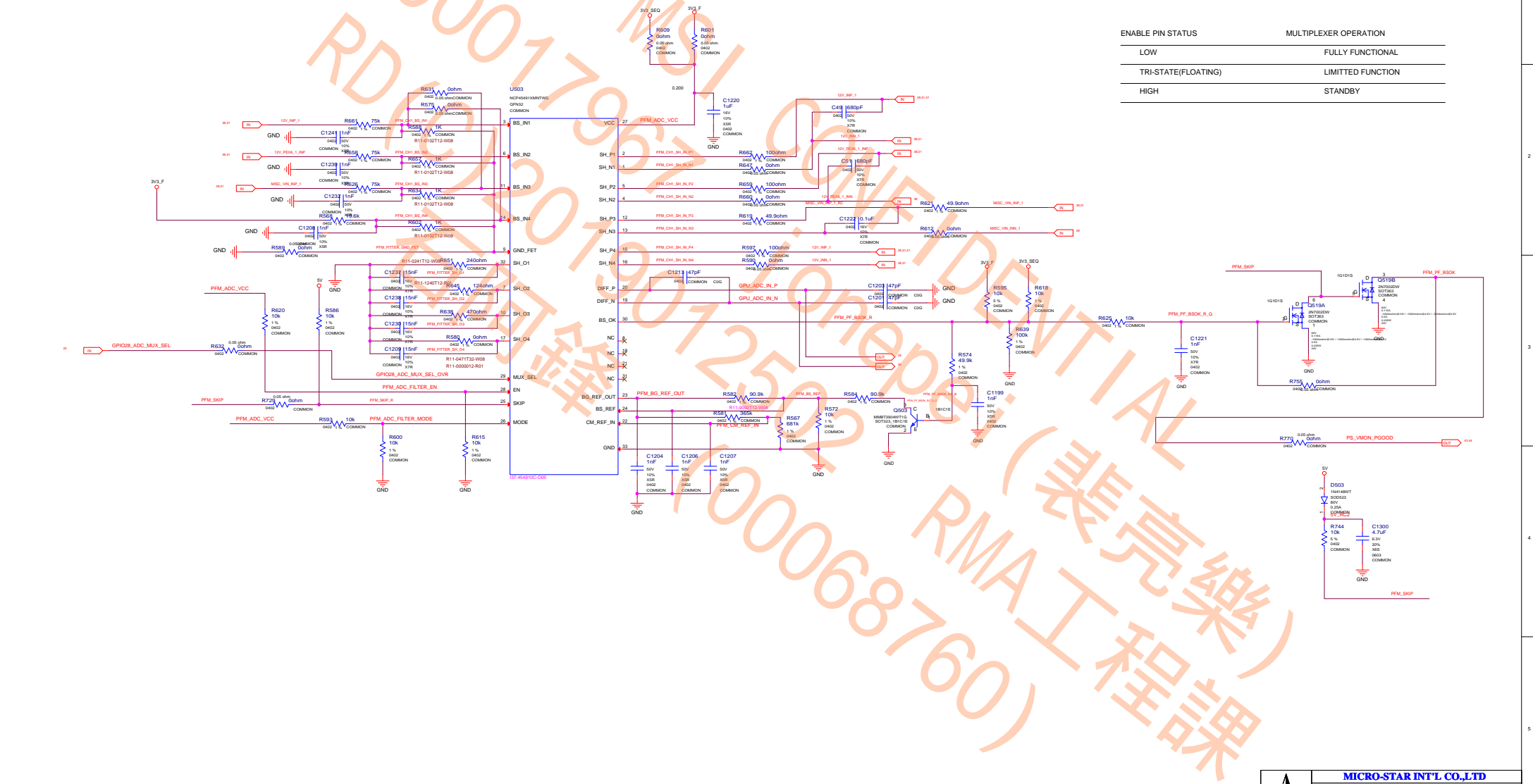


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| Custom                          | Page49: LED DRIVER & Boost | 1.1            |
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| A | B | C | D |
|---|---|---|---|
|---|---|---|---|





| MODE PIN STATUS     | MULTIPLEXER OPERATION |
|---------------------|-----------------------|
| LOW                 | DEVICE A              |
| TRI-STATE(FLOATING) | STAND-ALONE           |
| HIGH                | DEVICE B              |

| ENABLE PIN STATUS   | MULTIPLEXER OPERATION |
|---------------------|-----------------------|
| LOW                 | FULLY FUNCTIONAL      |
| TRI-STATE(FLOATING) | LIMITED FUNCTION      |
| HIGH                | STANDBY               |

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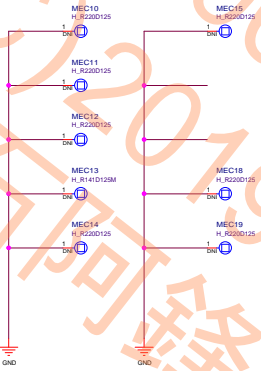
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| Size Custom                     | Document Description<br><b>Page51: PWR SENSE</b> | Rev 1.1 |
| Date: Friday, November 30, 2018 | Sheet 51 of 53                                   |         |

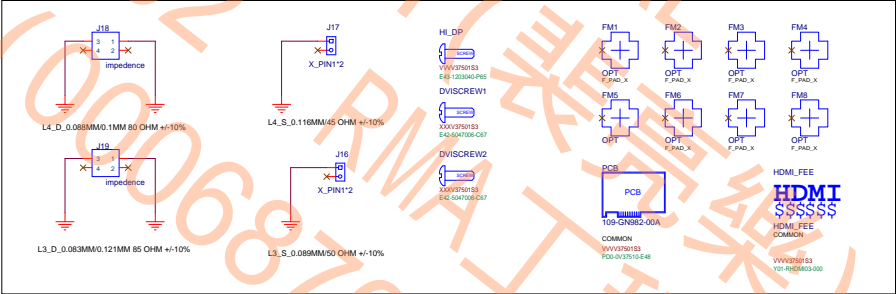
Bracket:



Mechanical Holes Symbol



BACK STIFFENER:



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| Custom   | Page53: PTC          | 1.1 |
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