

MS-V236-2.0 change list

Base on MS-V236-1.1 modified below items,

2010/08/27

Page05 deleted M501 and data net link to M5  
Page06 deleted M502 and data net link to M6  
Page07 deleted M504 and data net link to M3  
Page08 deleted M503 and data net link to M4  
Page09 deleted M506 and data net link to M1  
Page10 deleted M505 and data net link to M2

change list

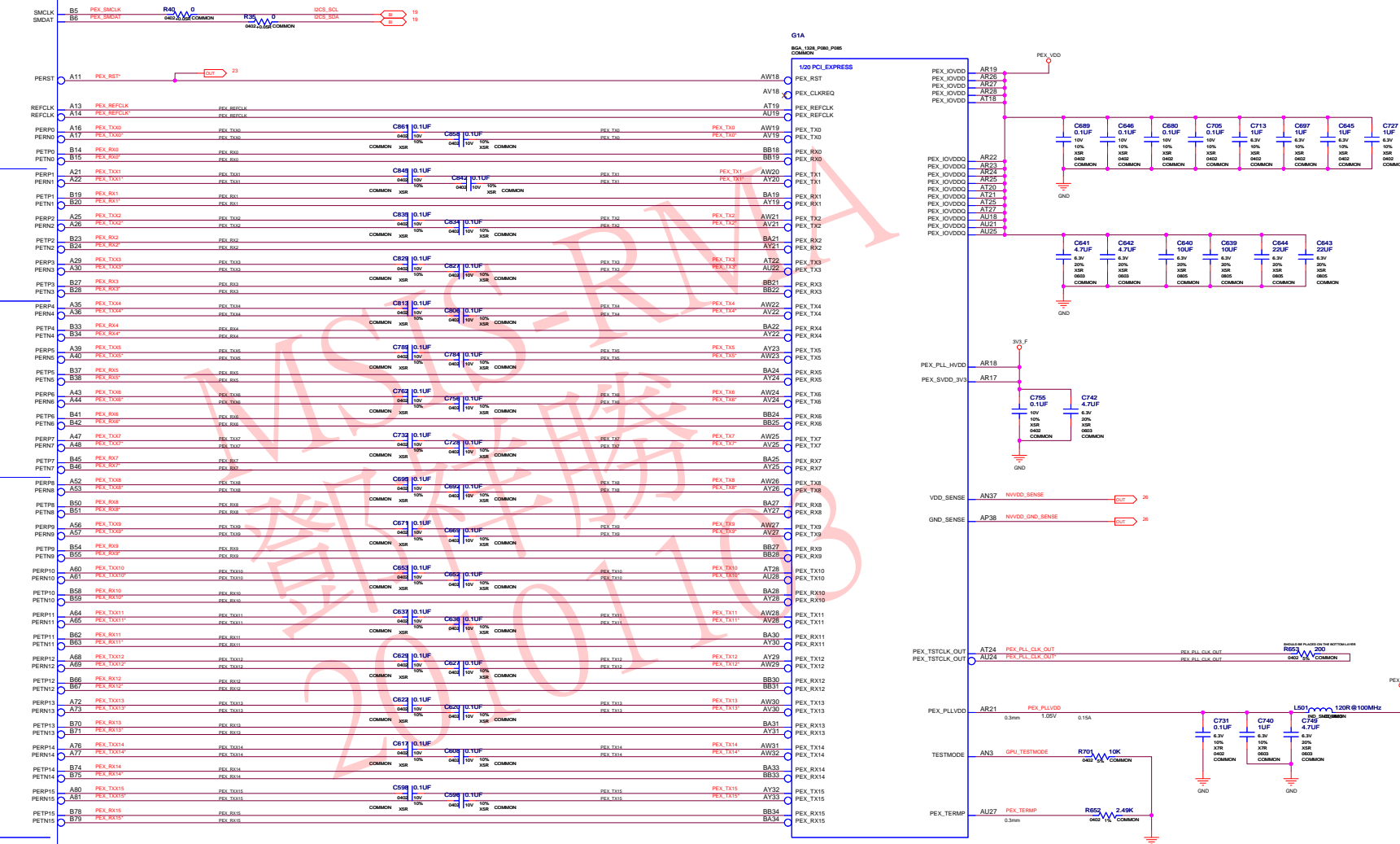
P13 D-sub add DACB的SCL SDA線路  
P15 刪除J3部份的I/O，power 保留  
P16 mHDMI copy V229 的SMD HDMI  
P17 刪除DP線路，加6262 IC  
P19 刪除U6，J501. 接I2CC給6262  
P22 add Hi-C CAP(C943)  
P24 12V\_PEX choke change to R50  
P25 FBVDD output choke 改R68  
P26 NVVDD output choke都改R68，加預留一顆大電容C82  
P28 刪除mec1，加光學點，阻抗條，防彎條  
0813  
P13 I/O power net name改5V\_VDD  
P24 L17 感值描述改回R50  
P25 memory MOS改0903Bk，同時改footprint  
P25 26，R68改正式料號  
P26 NVVDD MOS改4939+4935  
P28 FAN foot\_print 改回自己的，防連錫

REV	VARIANT	NVPIN	ASSEMBLY
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1	SKU0001	600-11060-0001-200	GF106-275 42 1600MHz/2000MHz 1024MB (8pcs)64Mx16 BGA170 GDDR5 (iron grid), DVI+DVI+miniHDMI, 140W
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3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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5	SKU0005	600-11060-0005-200	GF106-275 42 1600MHz/2000MHz 1024MB (8pcs)64Mx16 BGA170 GDDR5 on FBB/FBC, DVI+DP+miniHDMI, 140W
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11	SKU0011	600-11060-0011-200	GF106-250 42 1400/2000MHz 1024MB (8pcs) 64Mx16 BGA170 GDDR5 (iron grid), DVI+DVI+miniHDMI, 95W
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15	SKU0021	600-11060-0021-200	GF106-TBD 3/3 1400/2000MHz 1563MB (12pcs) 64Mx16 BGA170 GDDR5 (iron grid), DVI+DVI+miniHDMI, 125W

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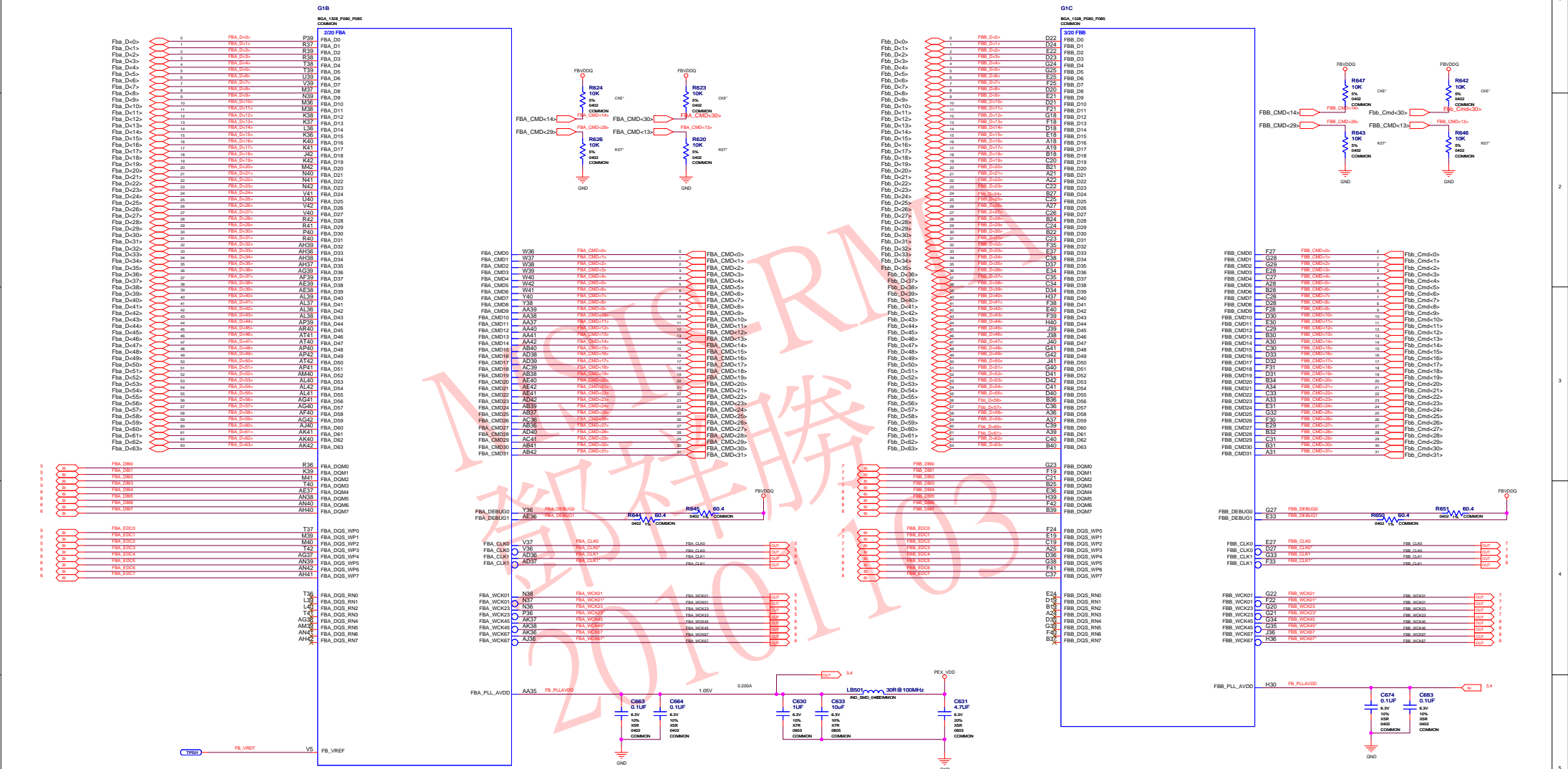
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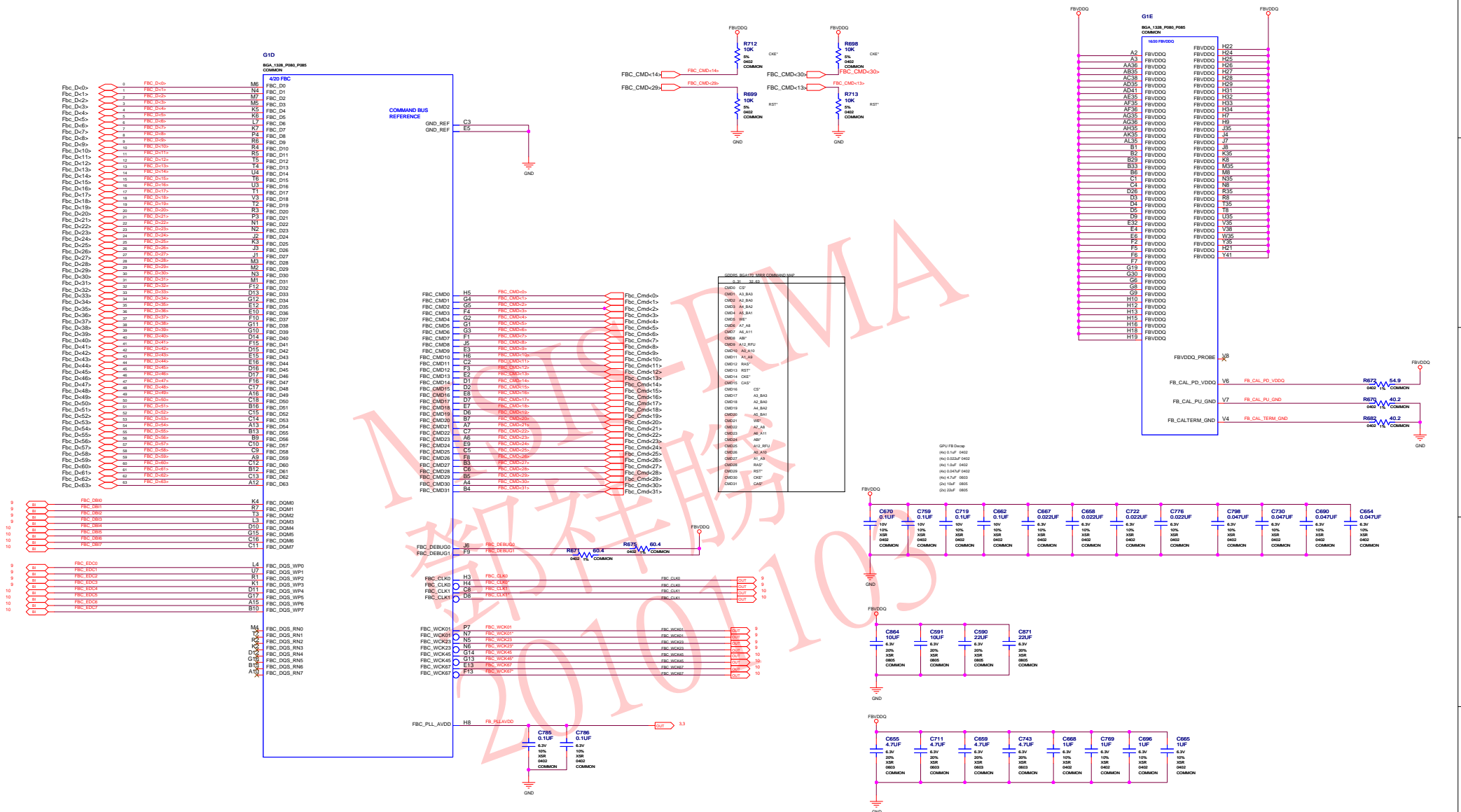
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# MEMORY: GPU FB Partition A and B



MEMORY: GPU FB Partition C AND GPU FB Decap



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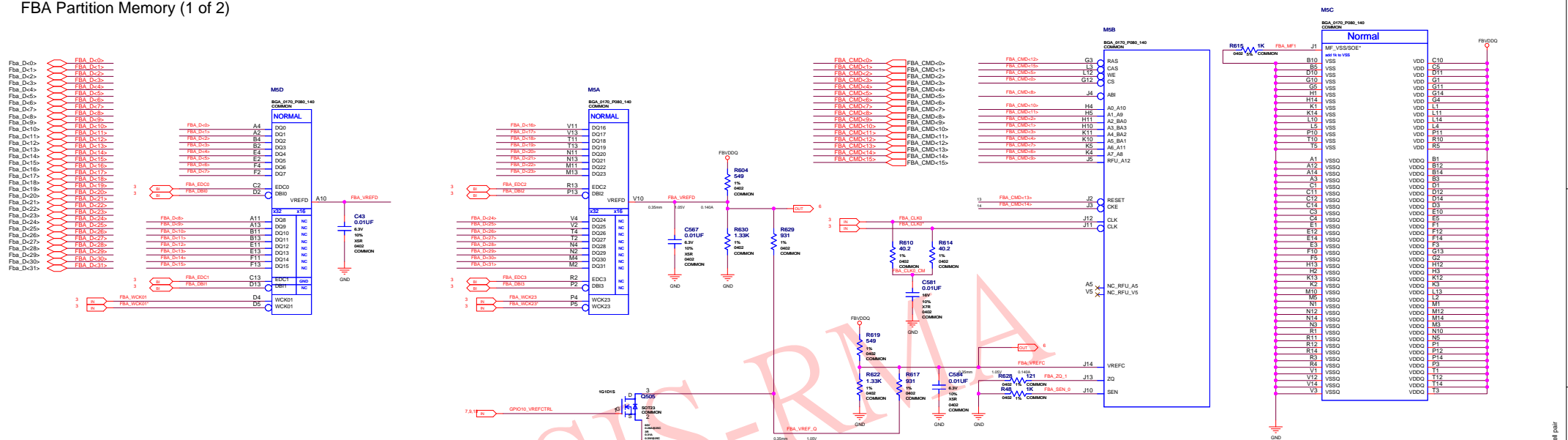
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PAGE DETAIL	GPU FB Partition C and GPU FB Decap
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## FBA Partition Memory (1 of 2)



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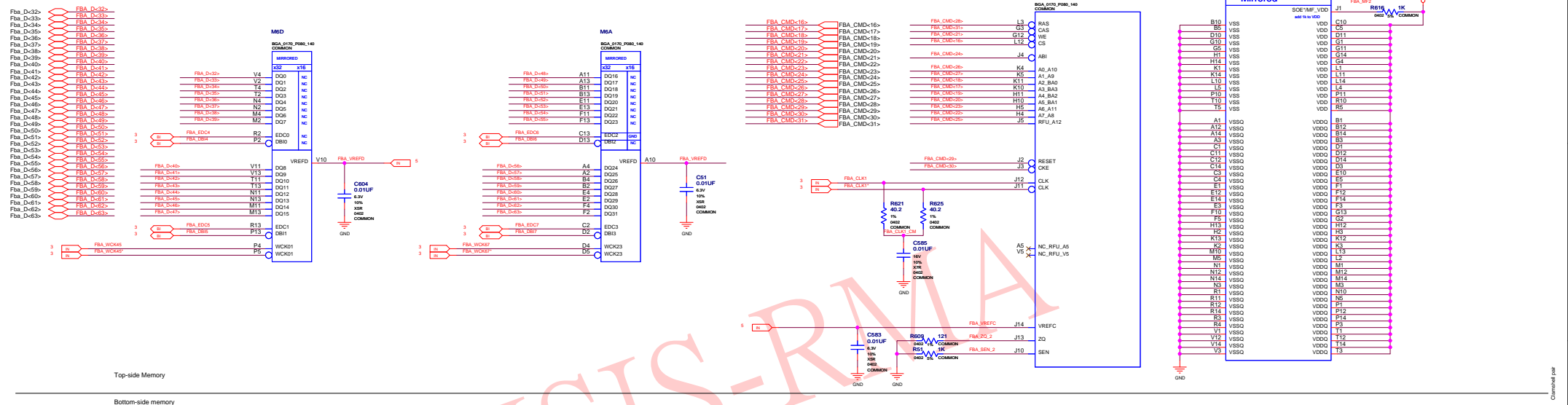
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## FBA Partition Memory (2 Of 2)



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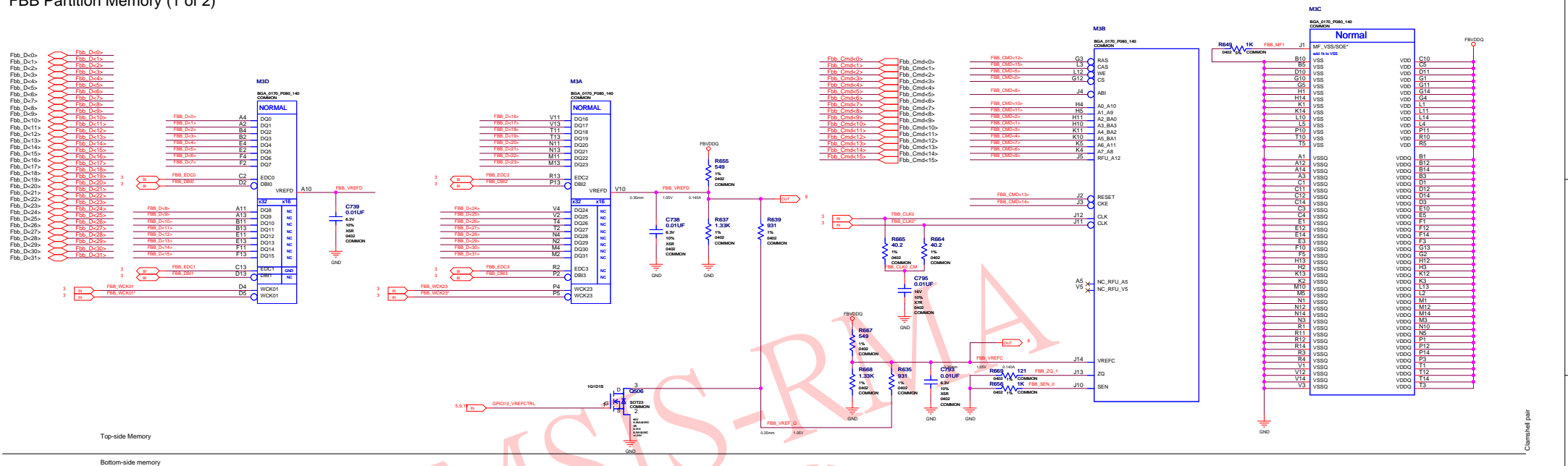
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## FBB Partition Memory (1 of 2)



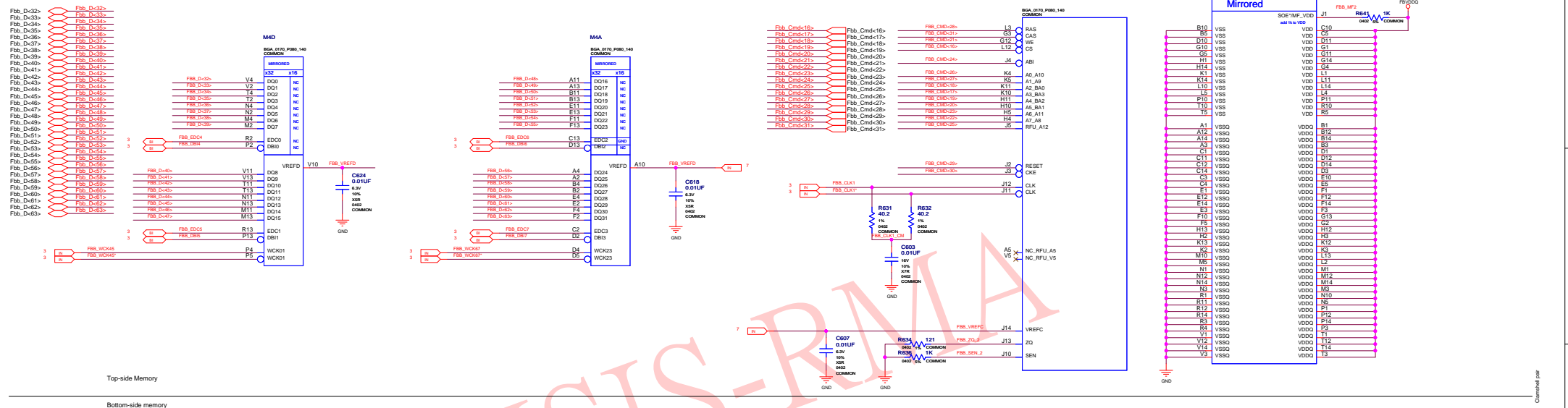
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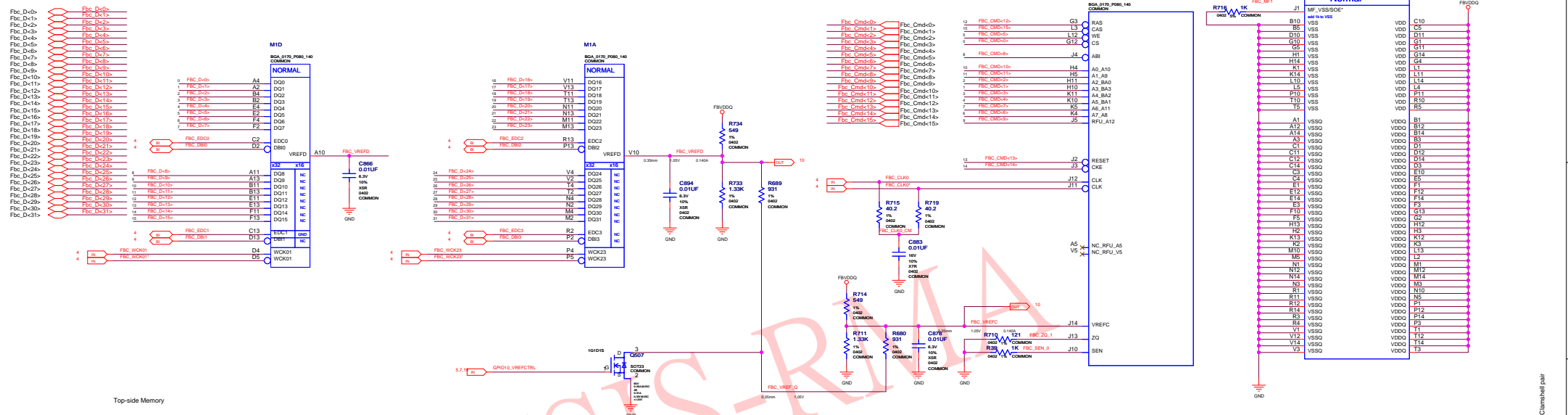
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## FBC Partition Memory (1 of 2)



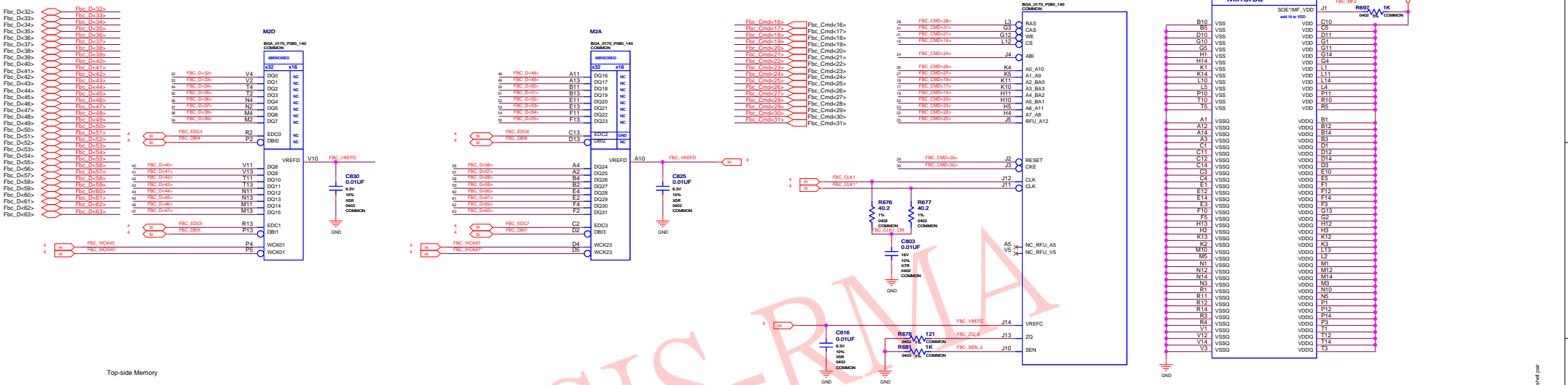
Clamshell pair

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## FBC Partition (2 of 2)




### Top-side Memory

Bottom-side memory

Clamshell pair

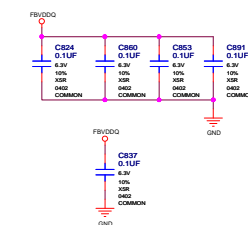
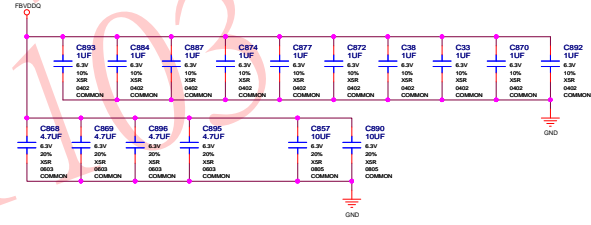
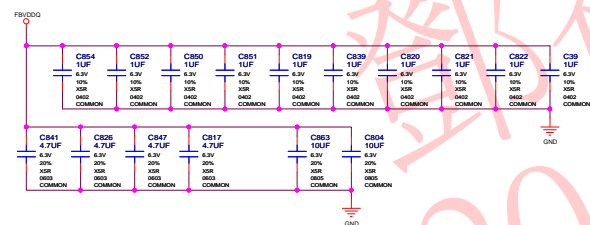
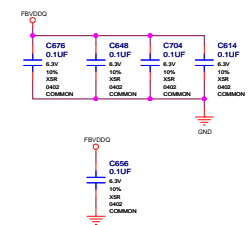
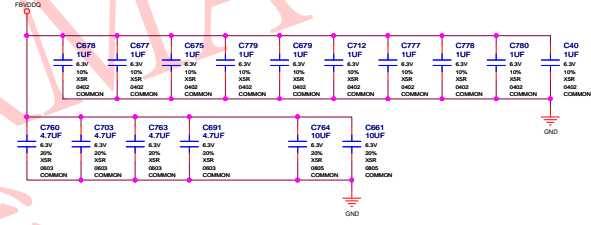
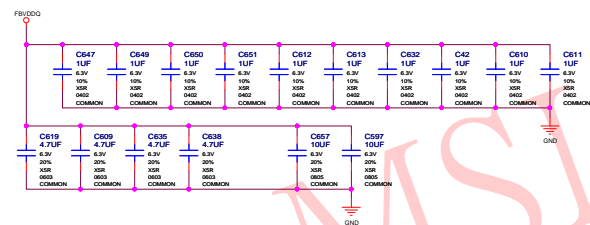
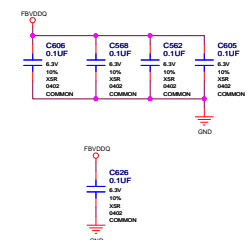
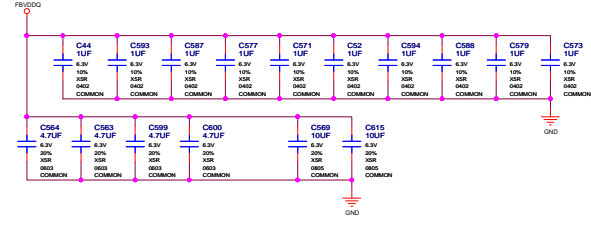
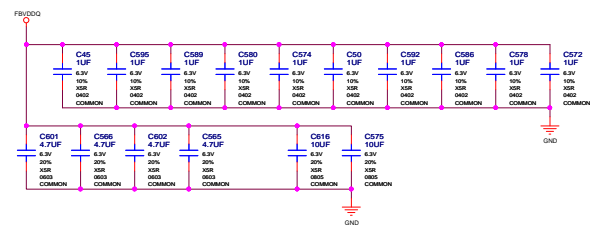
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## FB MEMORY DECAP



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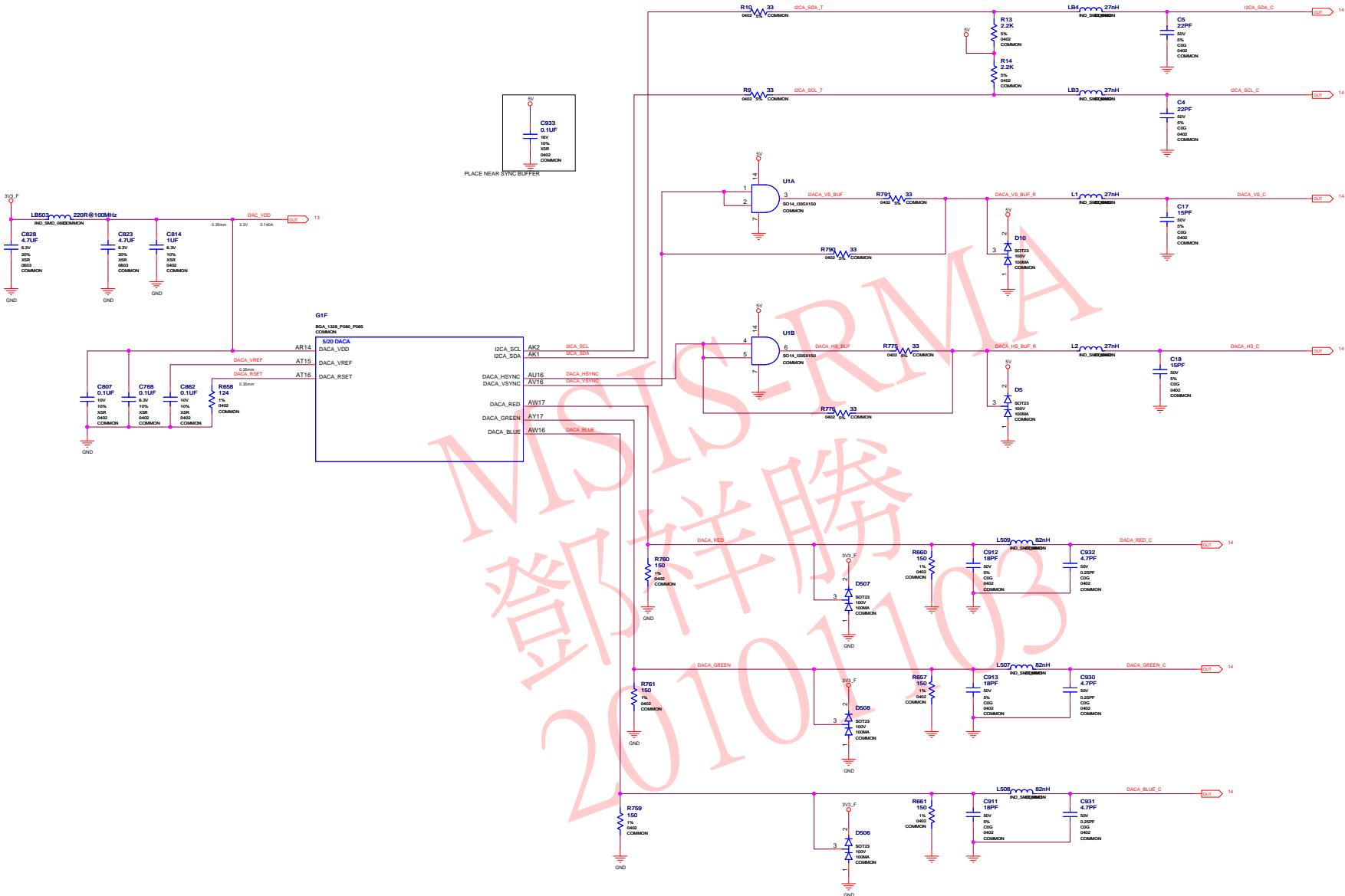
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# DACA for South DVI Interface

## DACA RGB-FILTER



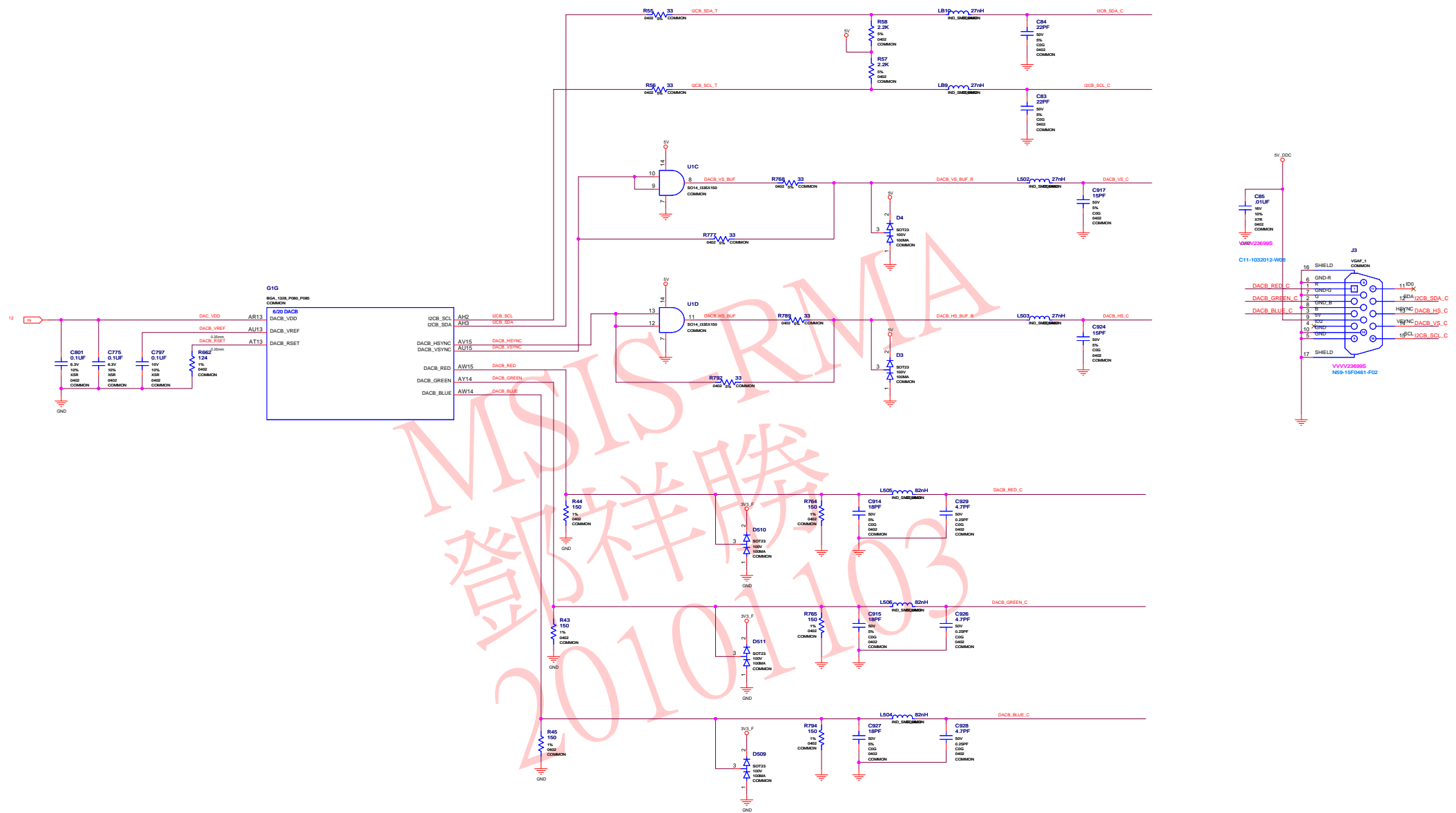
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PAGE DETAIL	DACA Interface for DVI Connector, South

### DACB for Mid DVI Interface

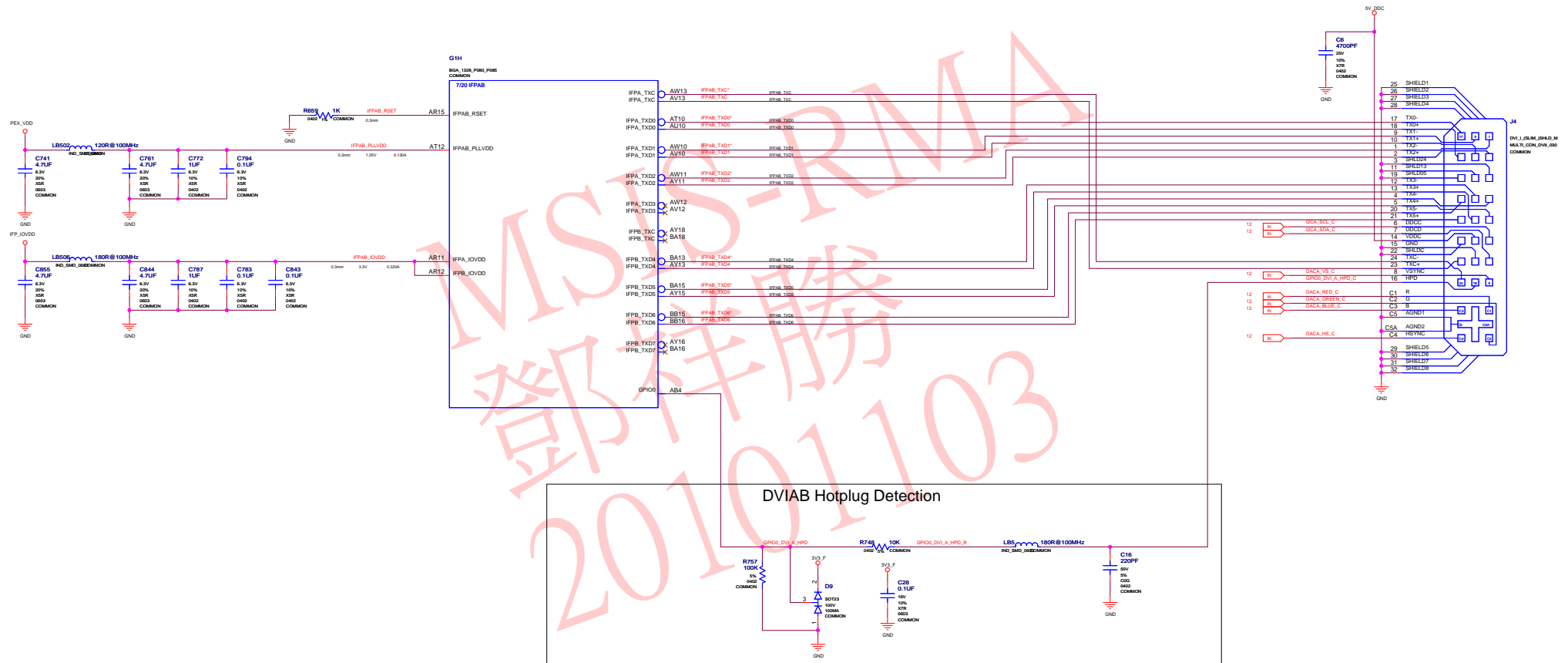
## DACB RGB-FILTER



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## IFP A/B Interface -- DVI Connector, South



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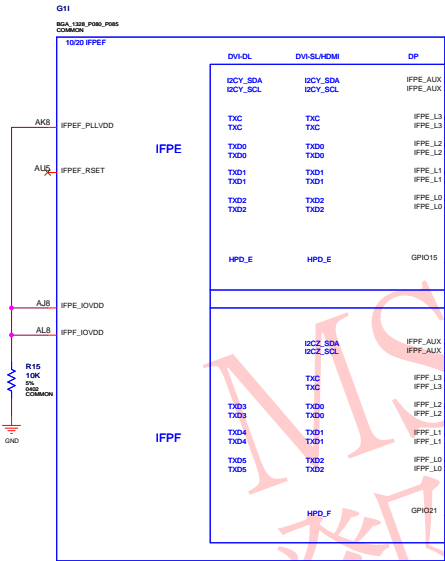
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IFP E/F Interface -- DVI Connector, Mid

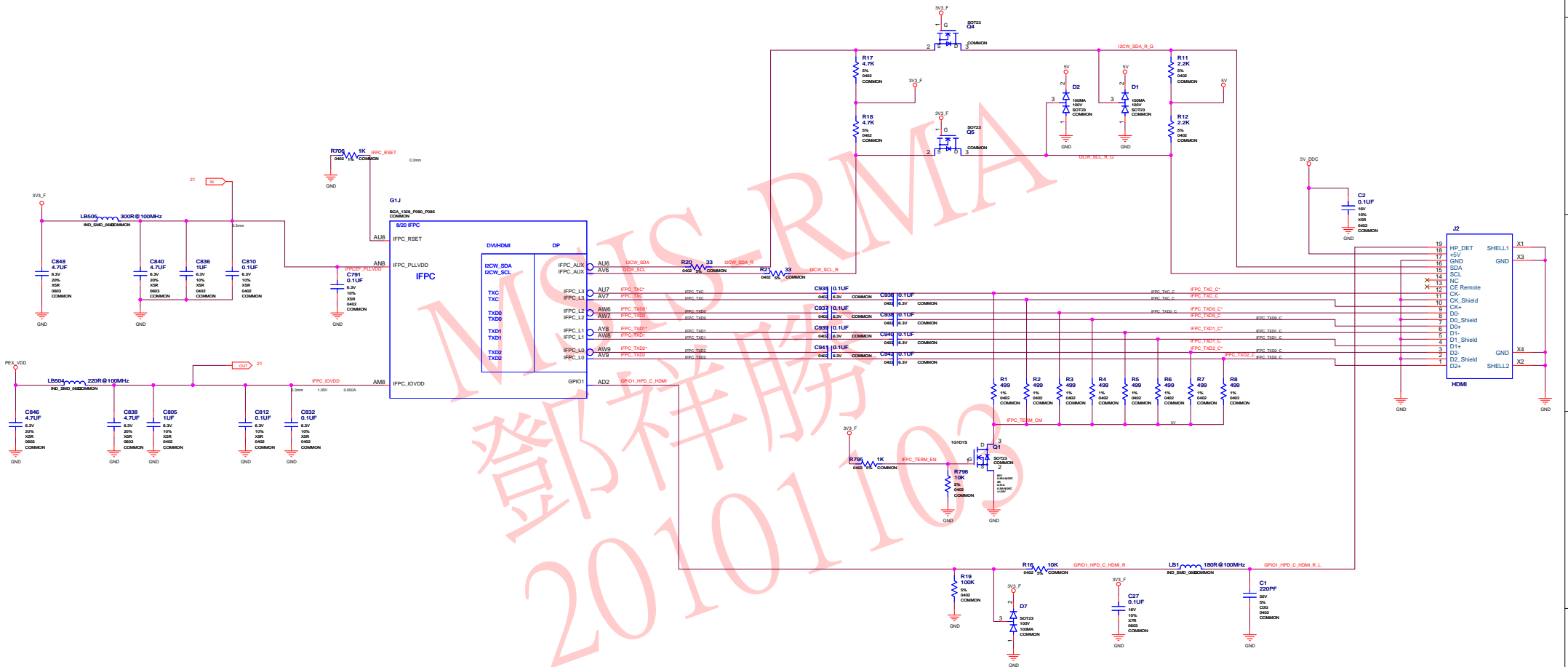


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IFP C Interface -- HDMI, North



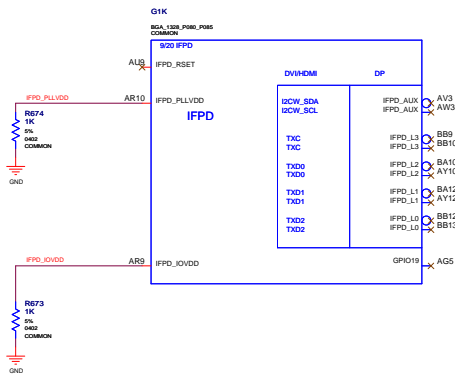
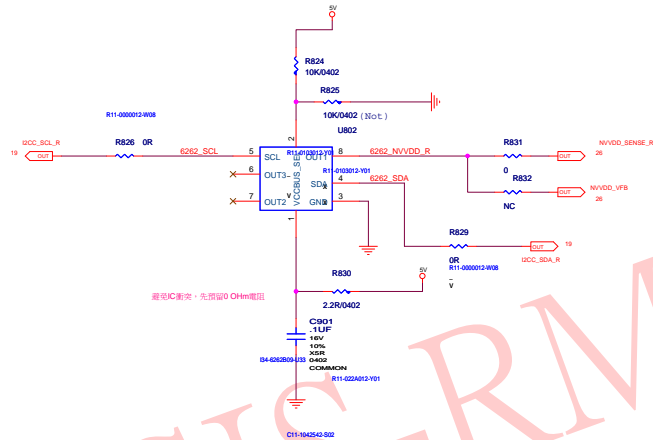
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PCB REV	P1000-002
BOM REV	A
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IFP D INTERFACE (UNUSED), DP from IFPE, Mid

- Three cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
  2. DP AUX to DP-DVI dongle: AUX pass through
  3. DP AUX to DVI connector: AUX level shifted to DDC



ASSEMBLY		P1060 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO.3100F ASSEMBLY NOTES AND BOM NOT FINAL	
PAGE DETAIL		DP FROM IFPE, Mid IFPD (UNUSED)	

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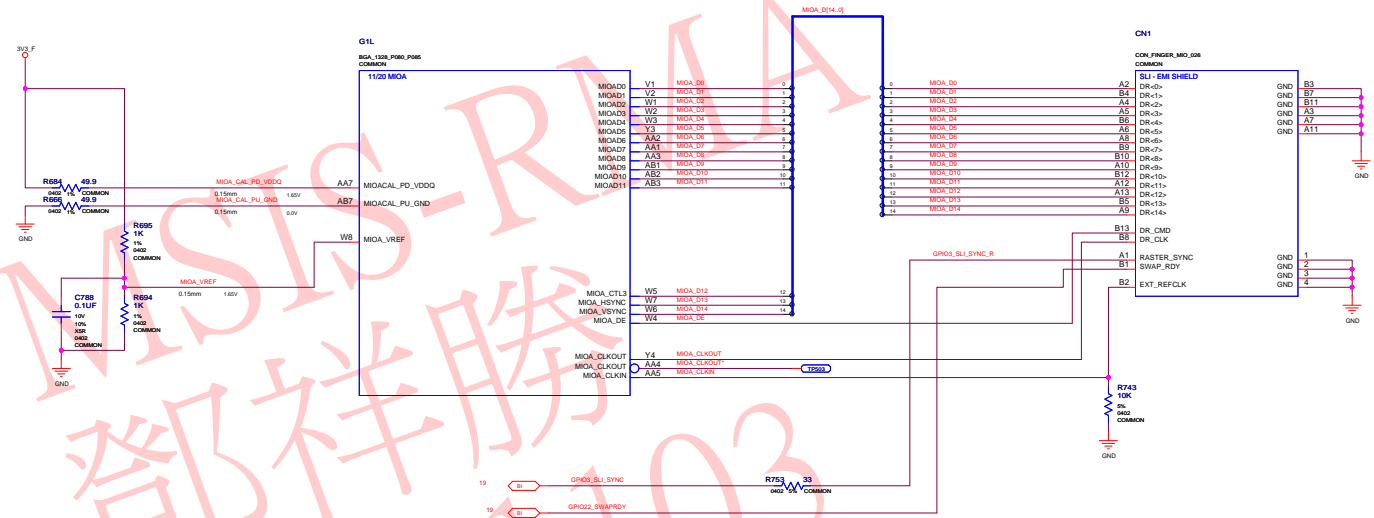
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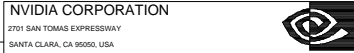
DATE

24 MAY 2010

MIO A Interface, SLI

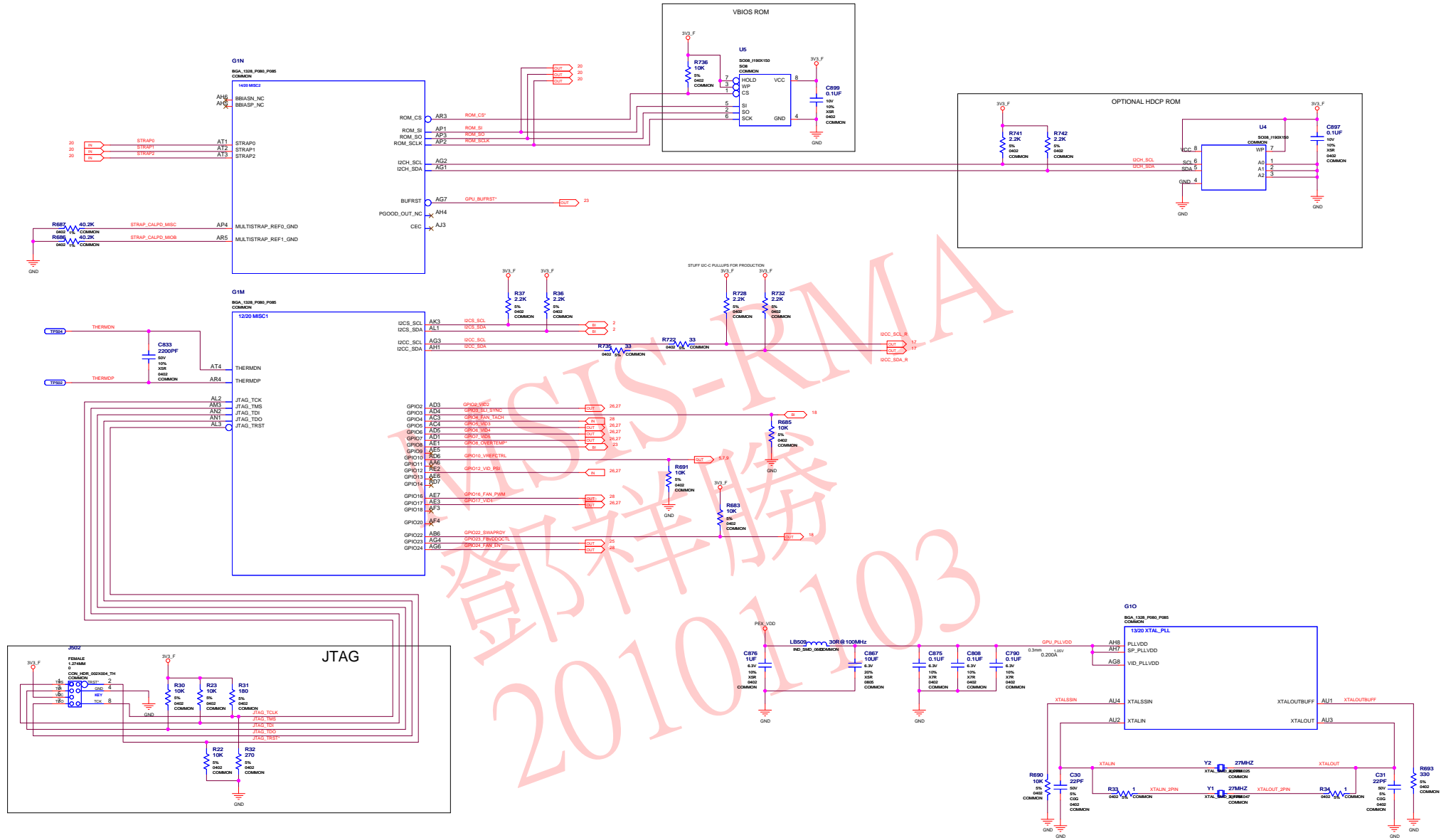


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# MISC GPIO I2C ROM HDCP and XTAL



ASSEMBLY	P1060 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO, I2C, ROM, HDCP, and XTAL

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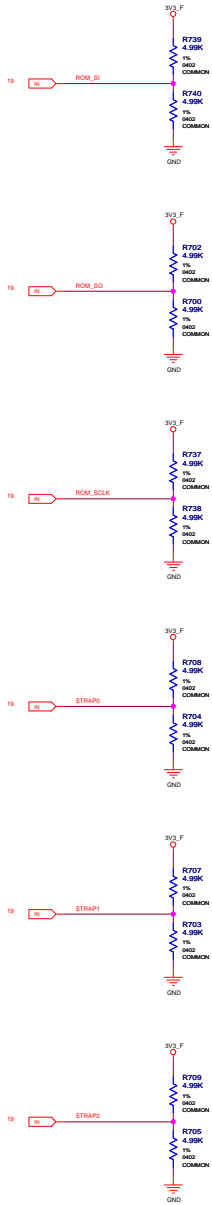
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PCB REV	P1060-702	PAGE	
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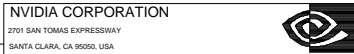
Strap Configuration



ROM_SO	VGA_DEVICE DMS_A17_A00M PL_3_BAH_SIZE XCLK_A17	LSB MSB	1: VGA_DEVICE 0: Disabled (P0) 0: 277MHz	PU	P0 10K
ROM_SI	RAM_CFG2[0]		Out: 64MB/16 128MB Samsung Out: 64MB/16 128MB Hynix Out: 64MB/16 128MB Samsung Out: 64MB/16 128MB Hynix	DI DI DI DI	45K 33K 45K 33K
ROM_SCLK	PEA_PLL_EN_TERMINUS SLUT_CLK_DIVID5 CLK_VENOR PCI_DEV0_BUT	LSB MSB	0: Disabled (P0) 1: GPU and HIGH COMMON RESETCLK 1: VBUS ROM IS PRESENT 0: PCIe/USB		33K
STRAP0	USER_BT3[0]		Out: Default		3K
STRAP1	SDIO_PIOCFG_LUT_A0M3[0]		Out: Default (High swing)		5K
STRAP2	PCI_DEV0B0M		Out: PCI_DEV0B0M0C1		10K

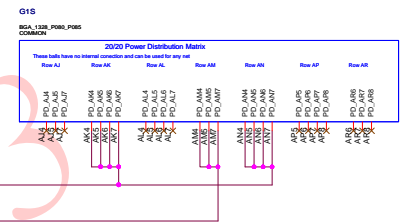
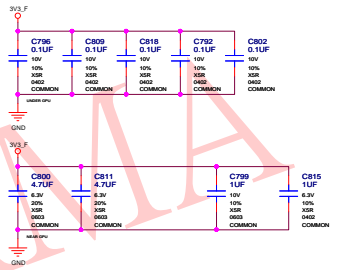
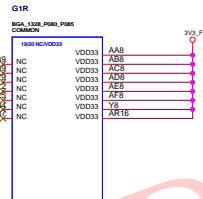
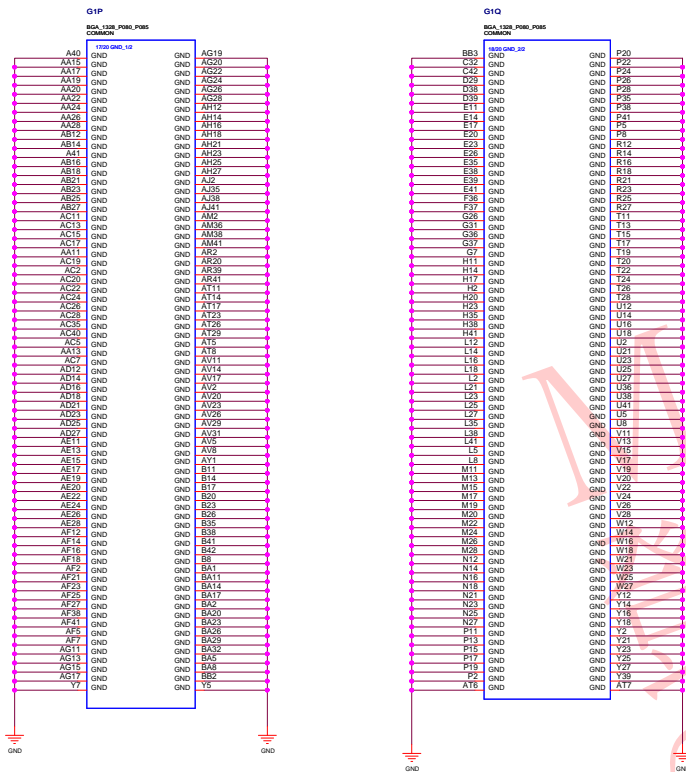
Multi-level Strap Resistor Values
Strap RUF0 Res (Ohm)
0: P0 15
1: P0 10
2: P0 15
3: P0 20
4: P0 25
5: P0 30
6: P0 35
7: P0 40
8: PU 5
9: PU 10
10: PU 15
11: PU 20
12: PU 25
13: PU 30
14: PU 35
15: PU 40

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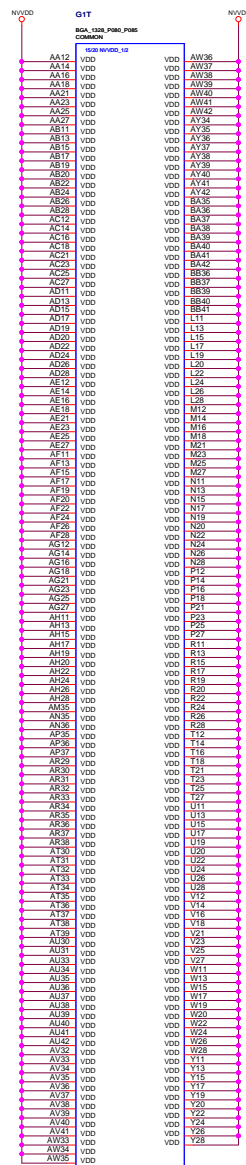
PWR and GND Signals



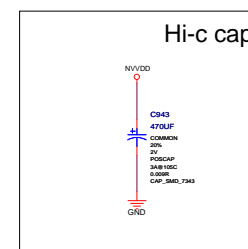
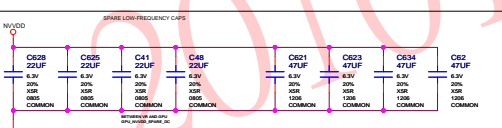
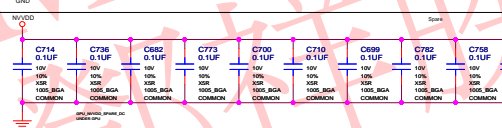
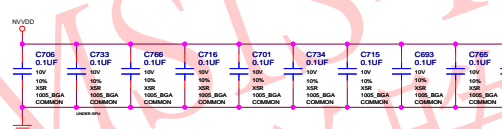
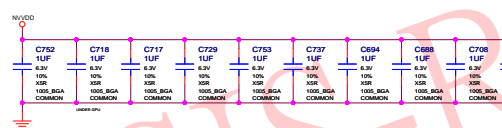
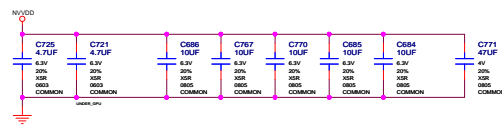
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## NVVDD Decoupling



## GF106 NVVDD Decap Guidelines



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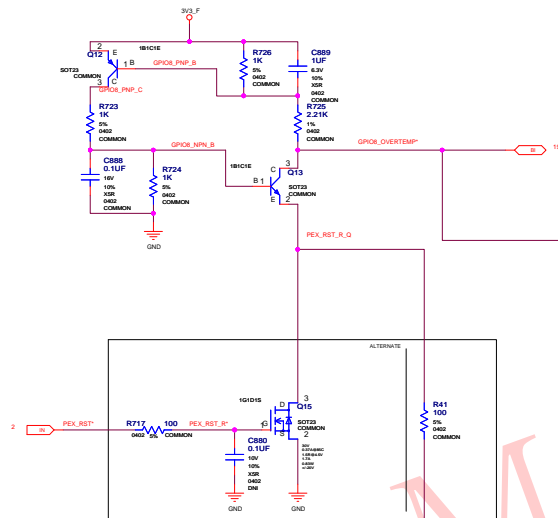
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PAGE DETAIL	NVVDD Decoupling

PTUG0 BASE LEVEL
NVVD0 Decoupling

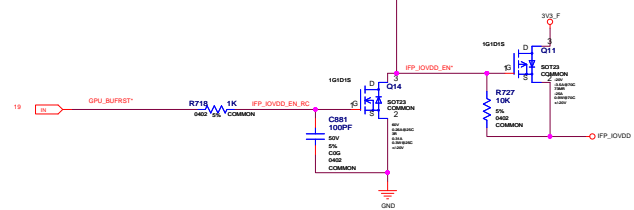


## Power Sequencing, Thermal Protection, and IFP\_IOVDD Power Supply

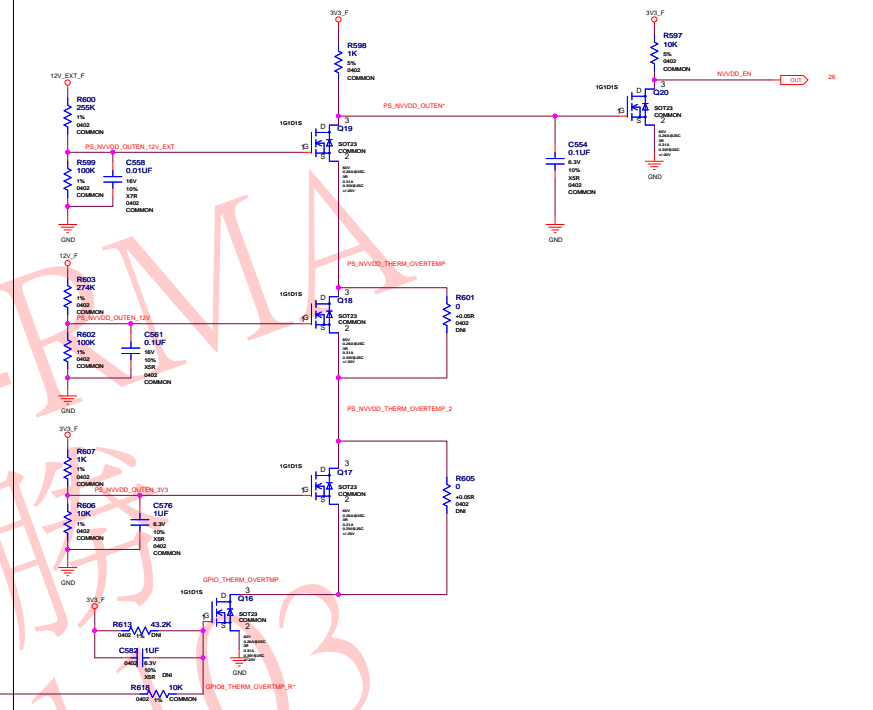
Thermal Protection (latch)



## IFP\_IOVDD Backdrive Prevention




### NVVDD Sequence



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PAGE DETAIL	Backdrive and Thermal Protection, Power Sequencing

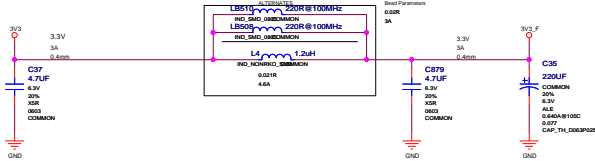
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# PS I: 3V3, 12V, and 12V\_EXT Power Supply Filter, 5V, DDC VOLTAGE

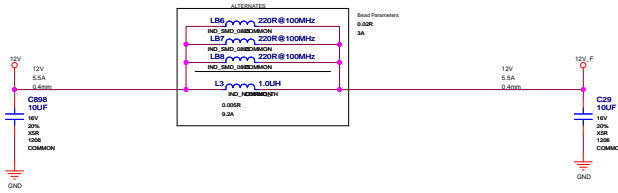
## 3V3 Power Supply Filter

3V3\_F = 3.3V @ 2.4A

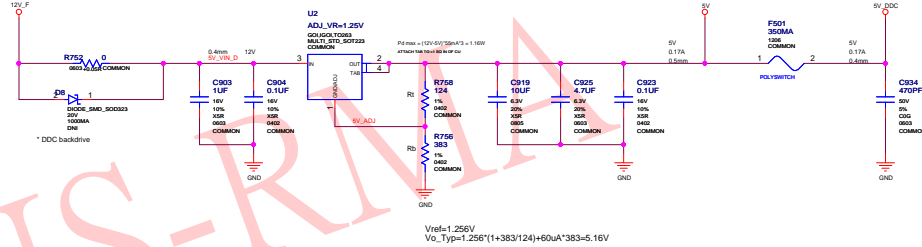


## 12V Power Supply Filter

12V\_F = 12V @ 5.5A



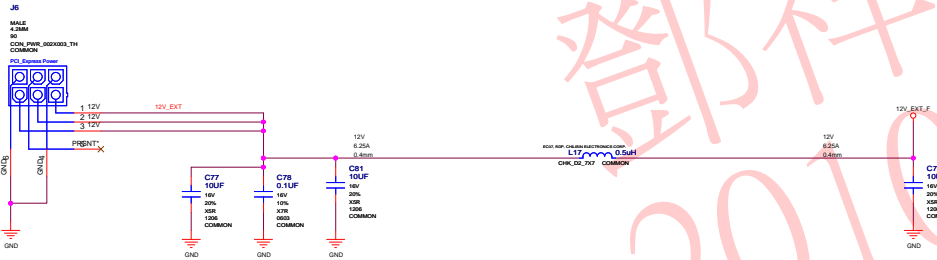
## 5V POWER SUPPLY, DDC POWER



## 12V\_EXT Power Connector

## 12V\_EXT Power Supply Filter

12V\_EXT\_F = 12V @ 6A



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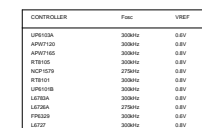
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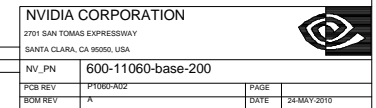
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PAGE DETAIL	PS I Input Power Supply Filter, 5V AND DDC VOLTAGE



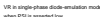
NV_PN	600-11060-base-200		
PCB REV	P1060-A02	PAGE	
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2-PHASE OR 3-PHASE DESIGN  
(UNSTUFF PHASE 2 FOR 2-PHASE CONFIG)



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