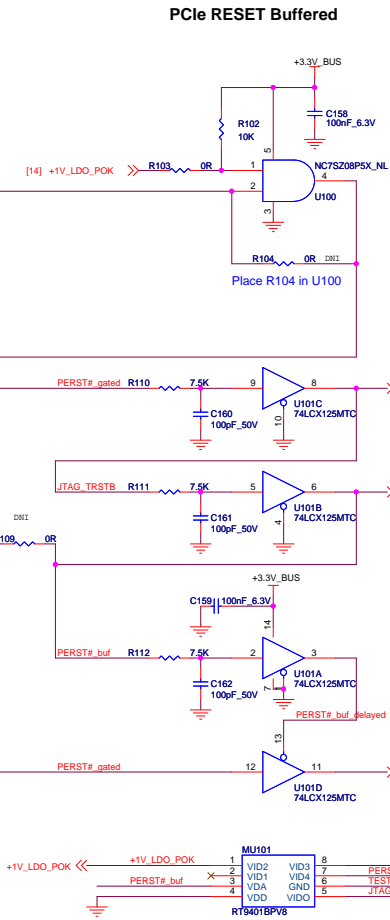
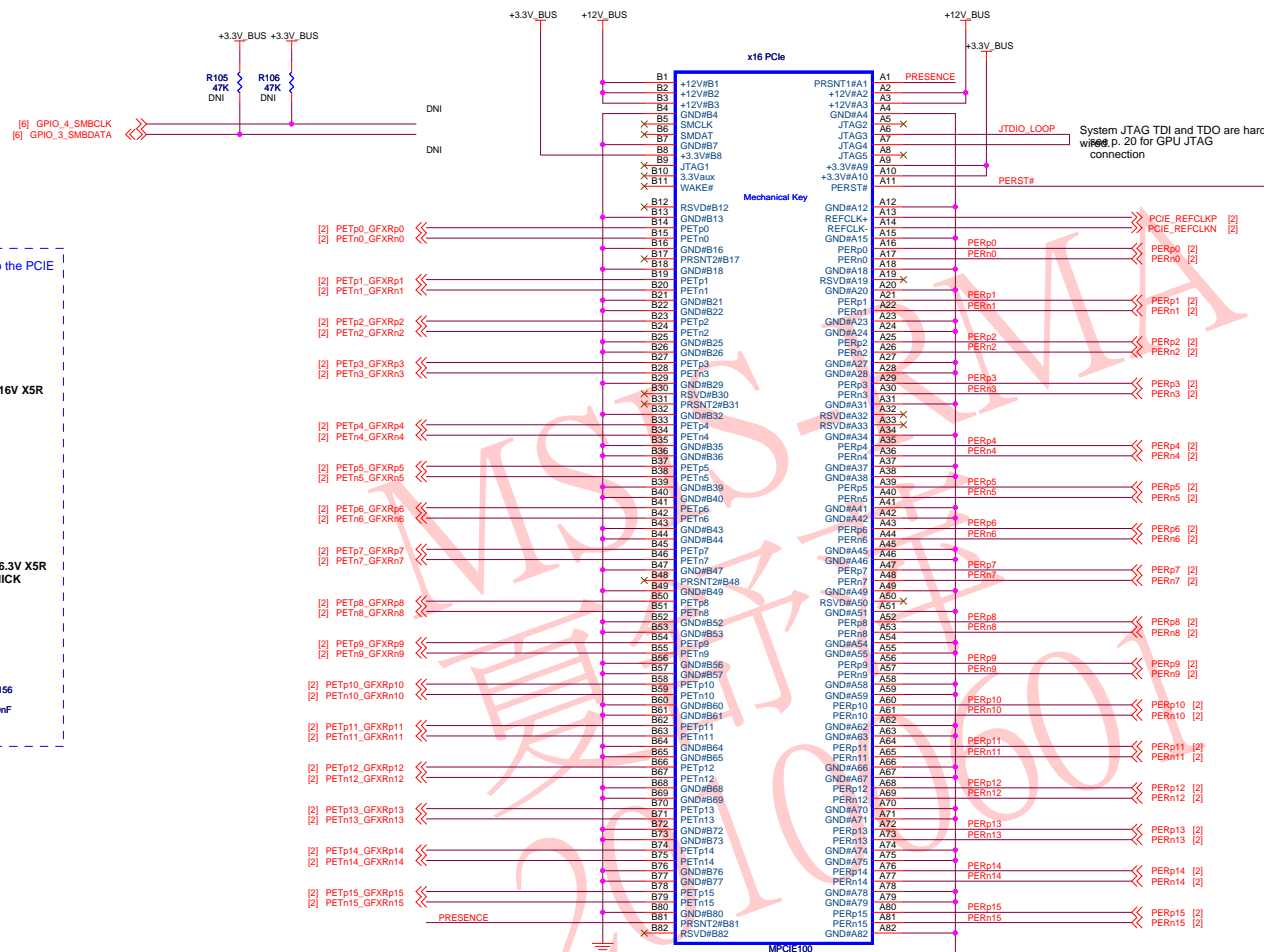
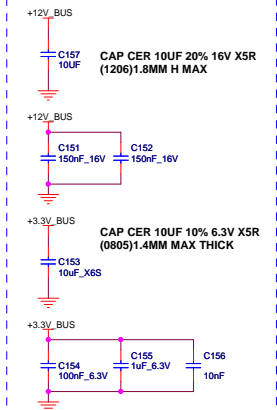


# PCI-EXPRESS EDGE CONNECTOR

## REDWOOD WOLVERINE

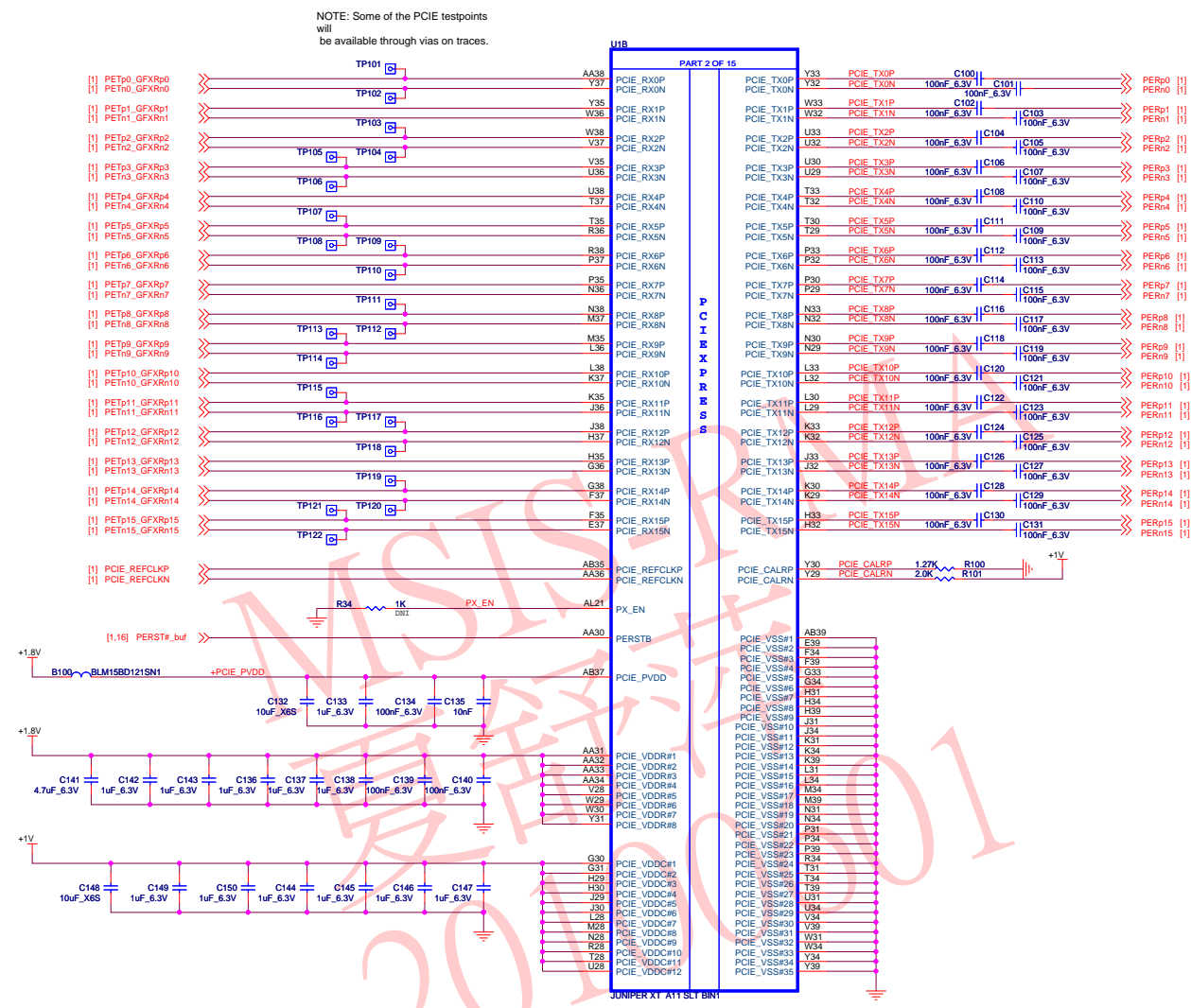


Place these caps as close to the PCIe connector as possible

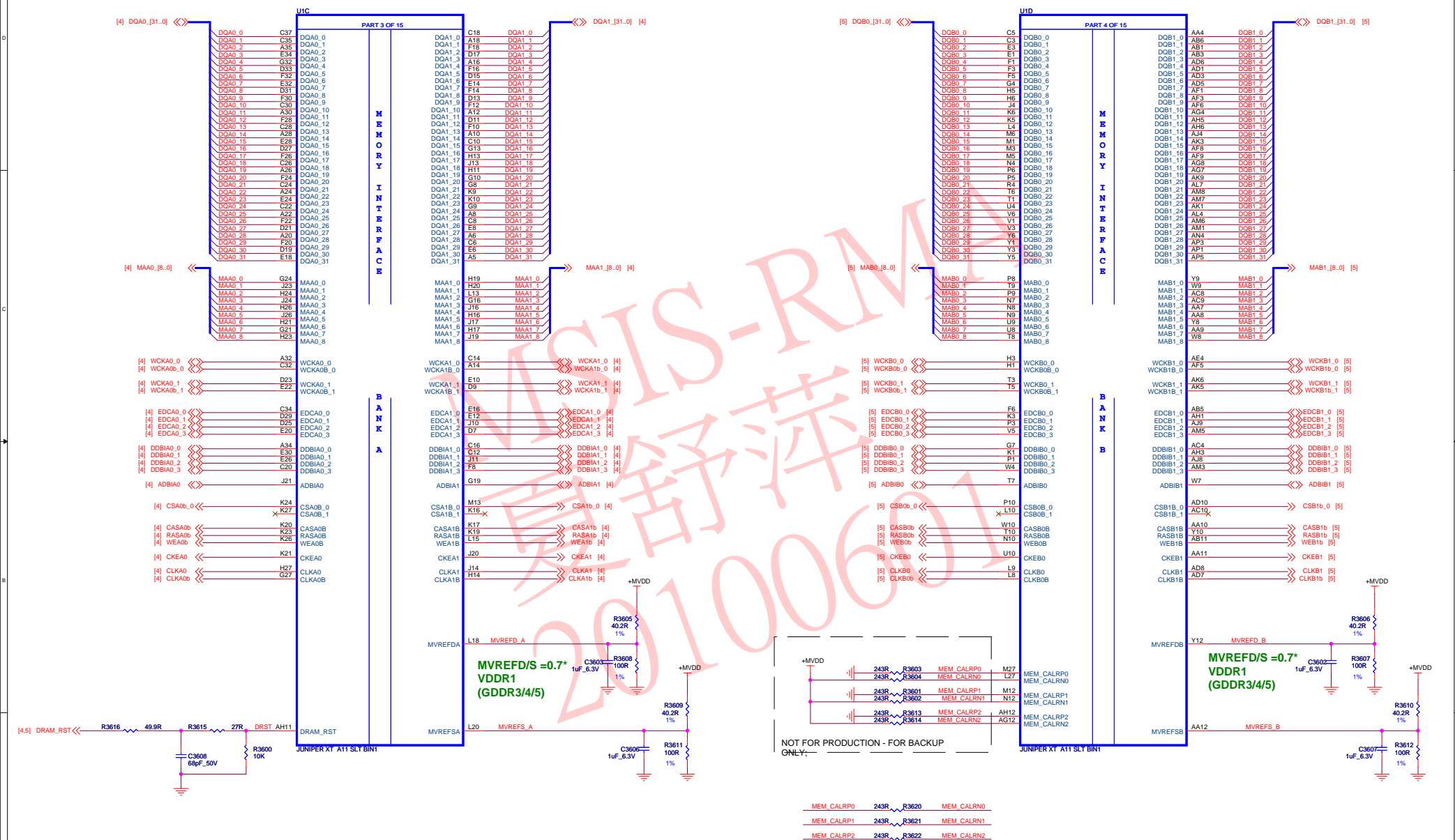


SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

(2) REDWOOD PCIe Interface

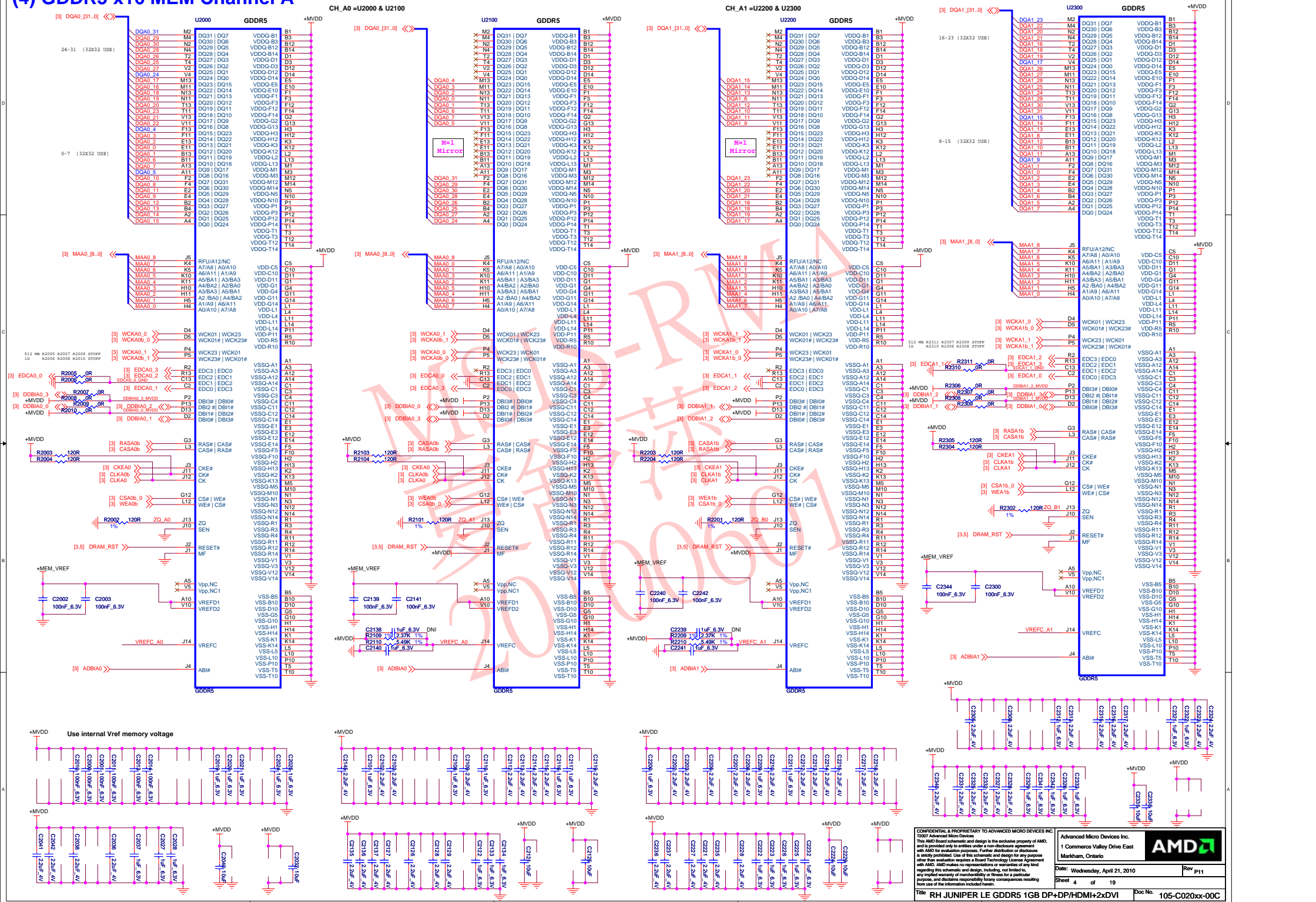


### (3) REDWOOD MEM Interface Ch A&B

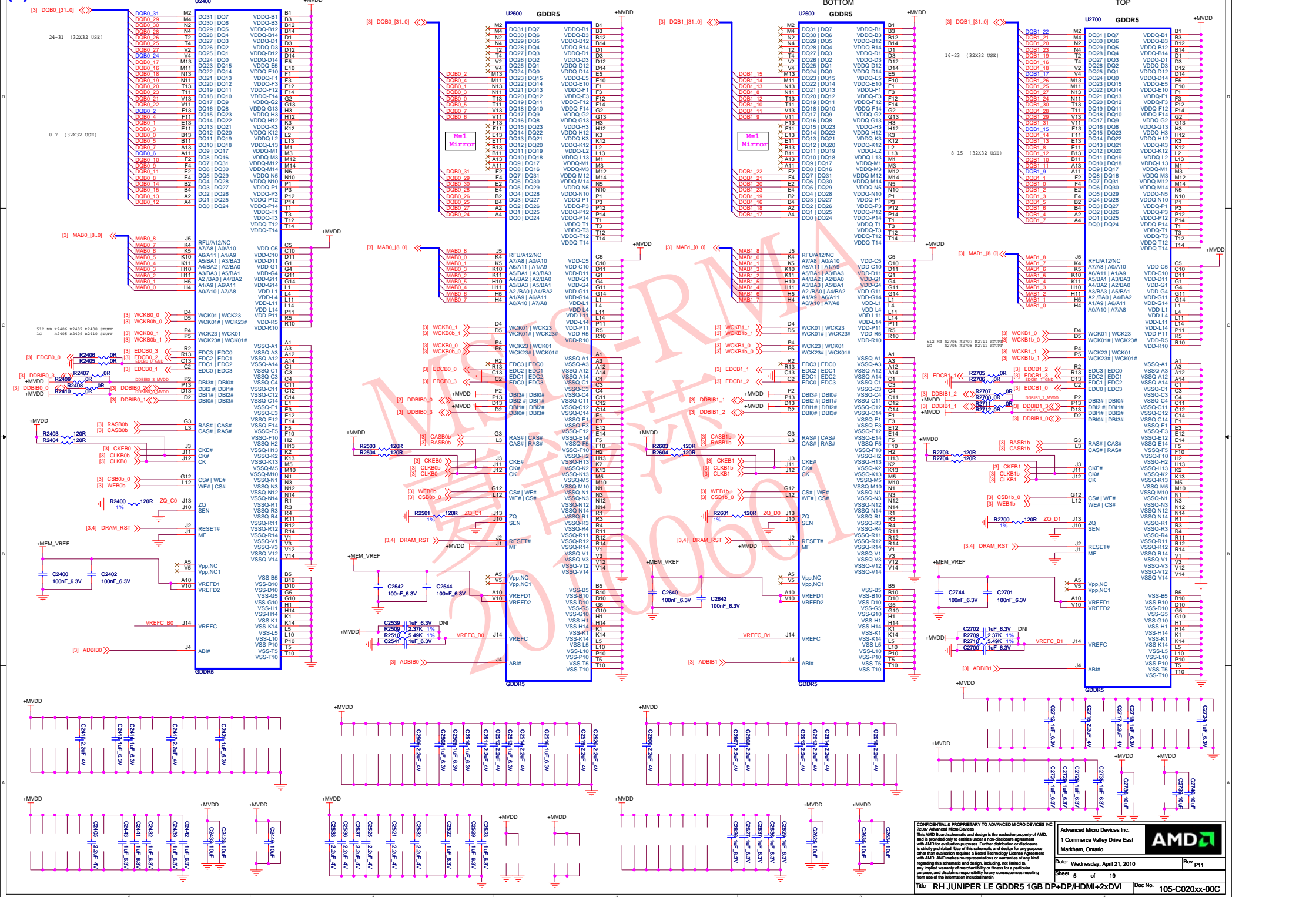


#### (4) GDDR5 x16 MEM Channel A

CH\_A0 =U2000 & U2100



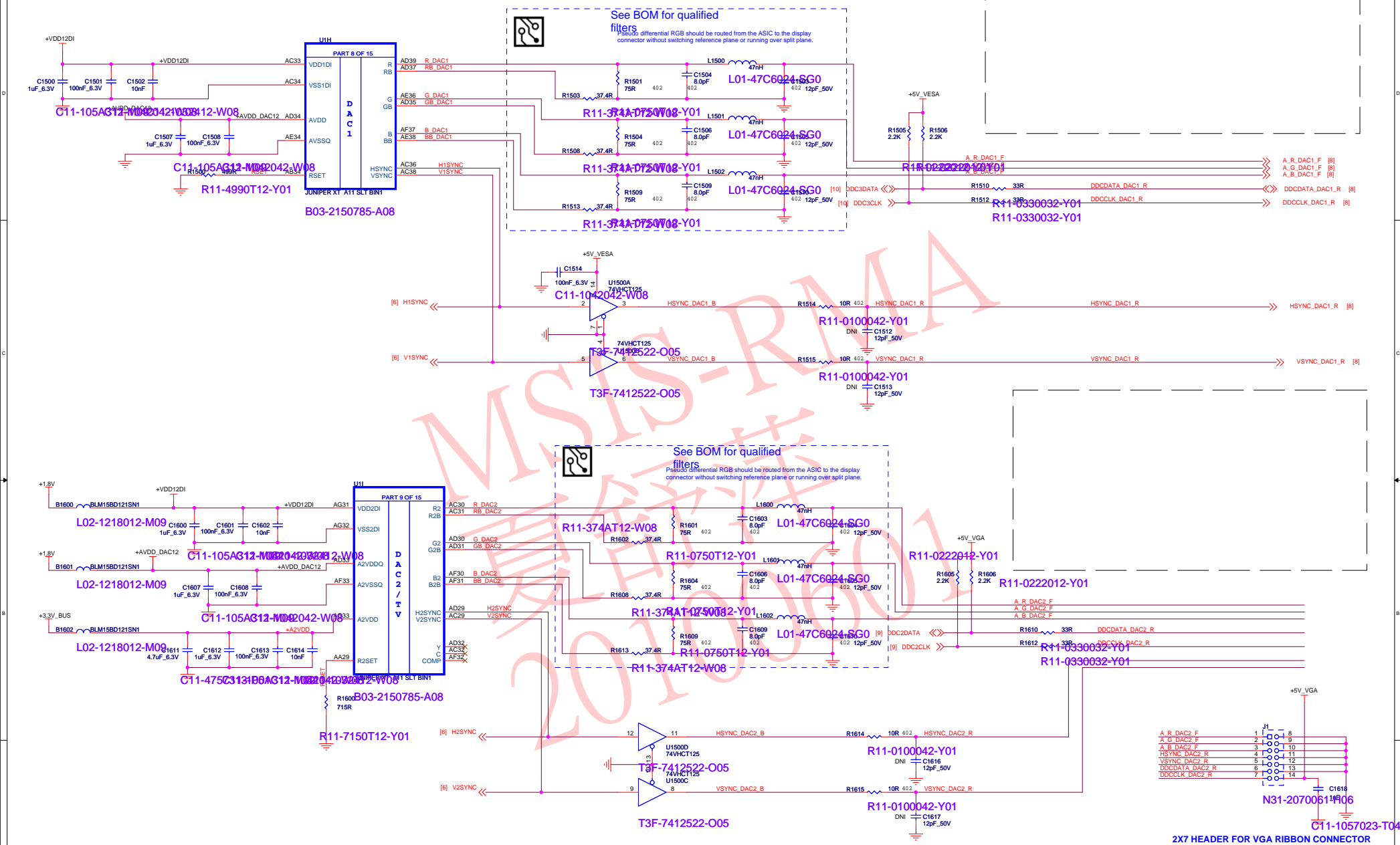
5	
(5) GDDR5 x16 MEM Channel B	



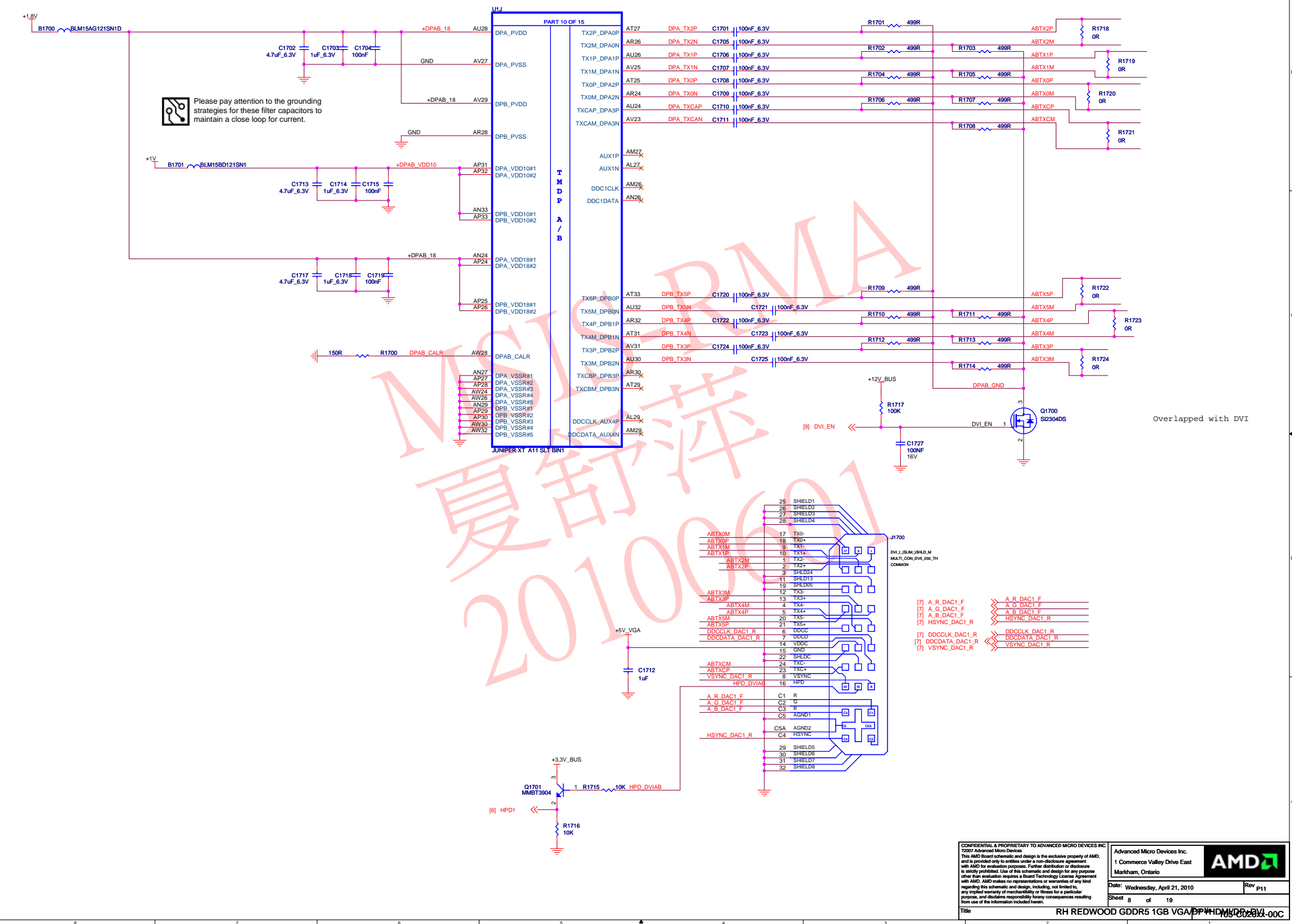




### (07) REDWOOD DAC1 and DAC2

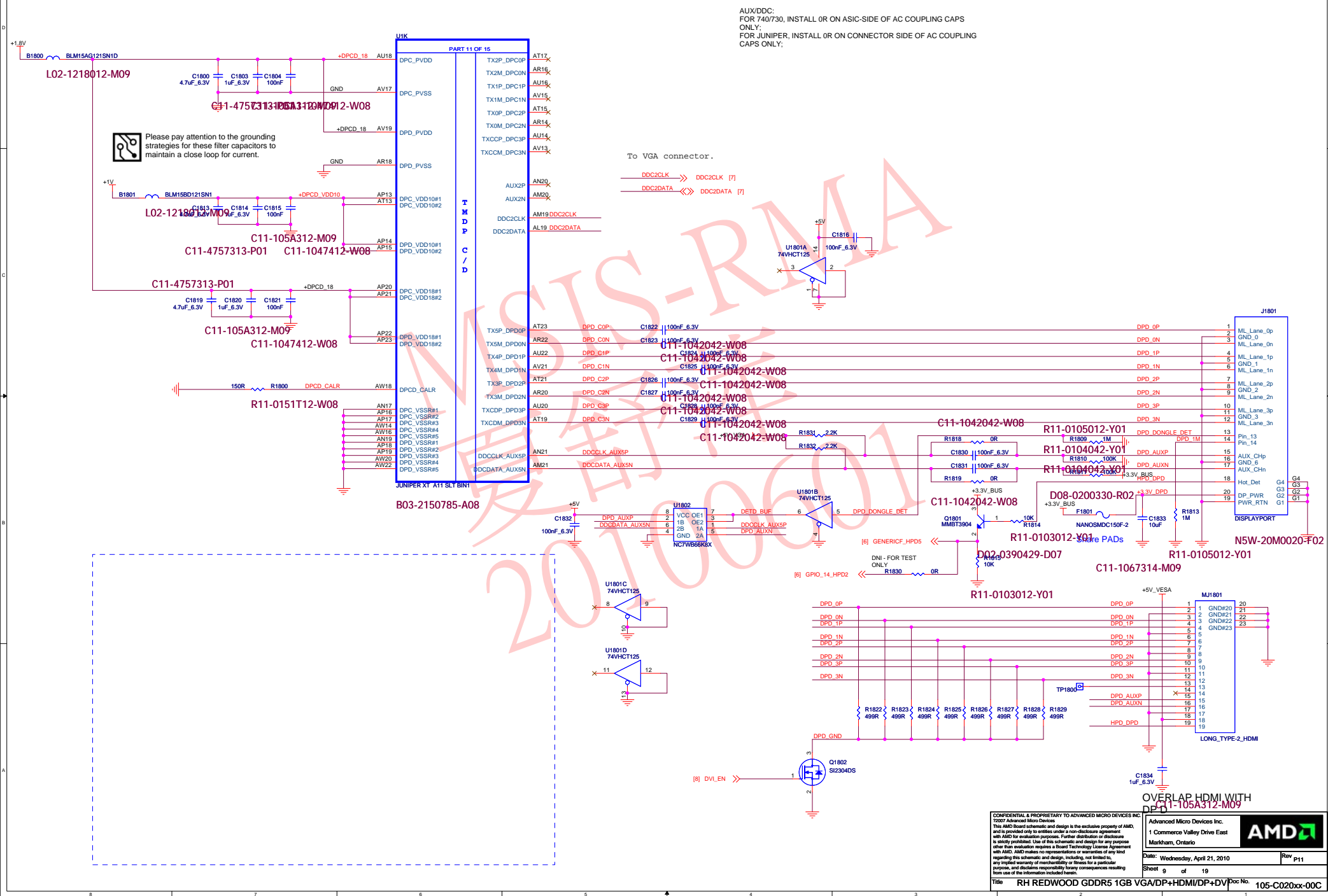


(08) REDWOOD TMDP A&B dDVI-I TOP

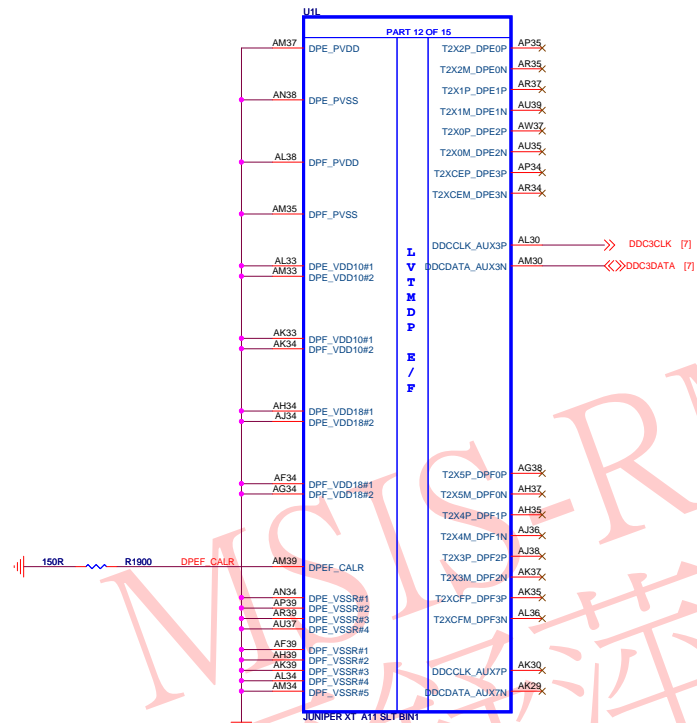




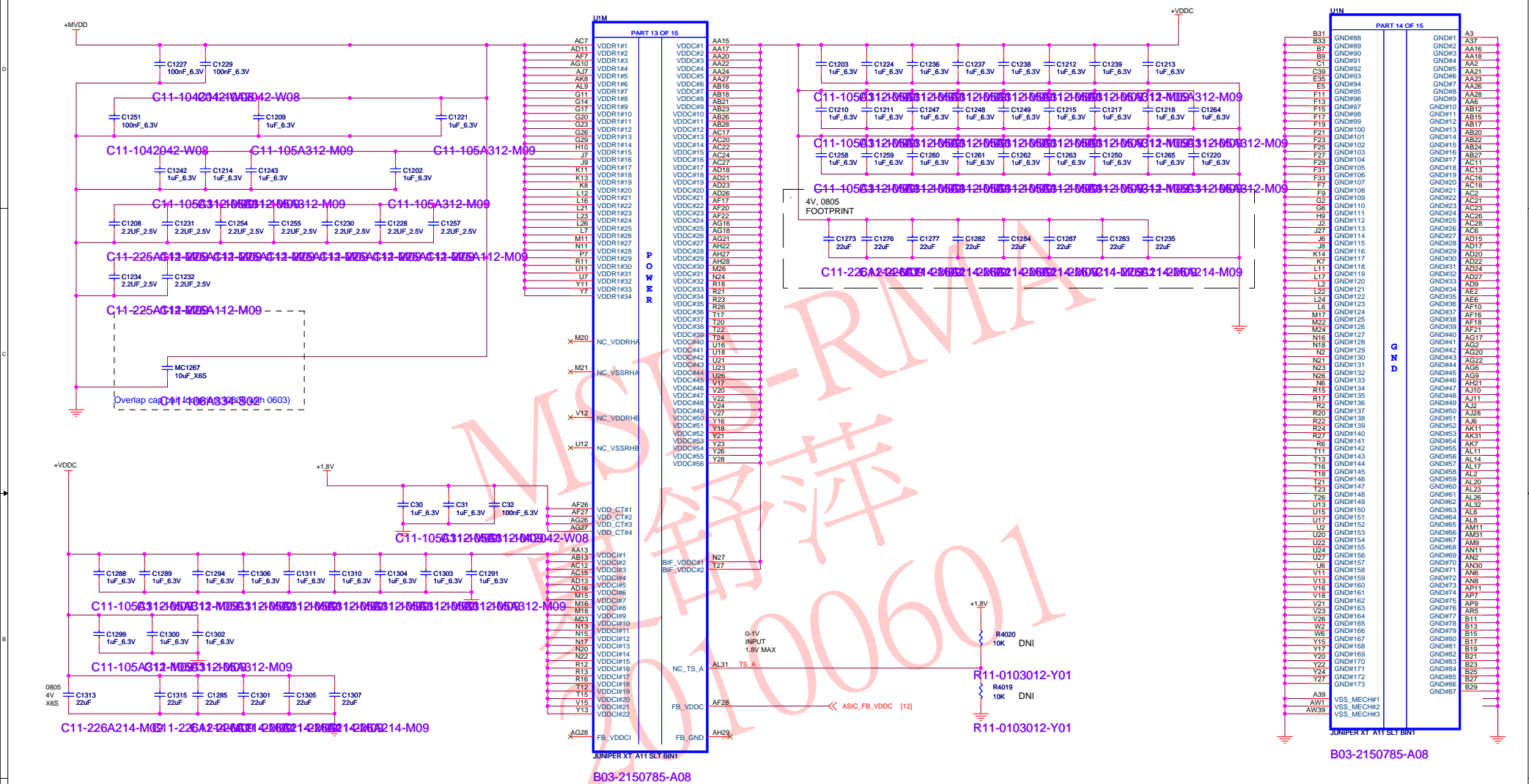
**(09) REDWOOD Display Port C & Display Port/HDMI D**



(10) REDWOOD LVTMDP E&F



## (11) REDWOOD Power & GND









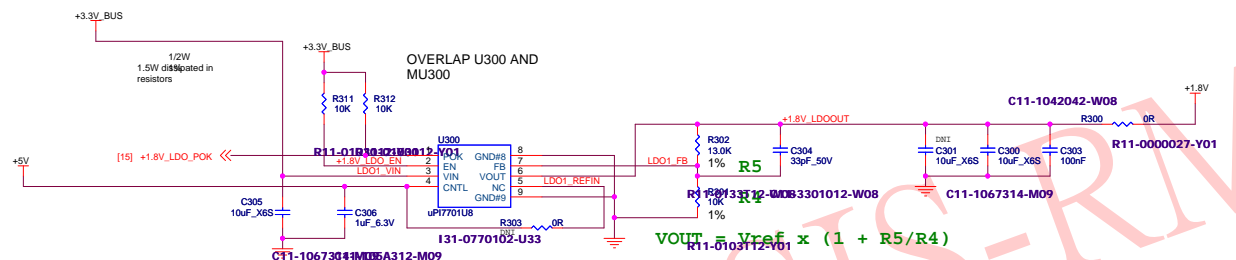
## (15) Linear Regulators

**LDO #1:** Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling

USE 6x 3.6R  
AMD PN  
3180006800G

### 1.8V WORST-CASE REQUIREMENT

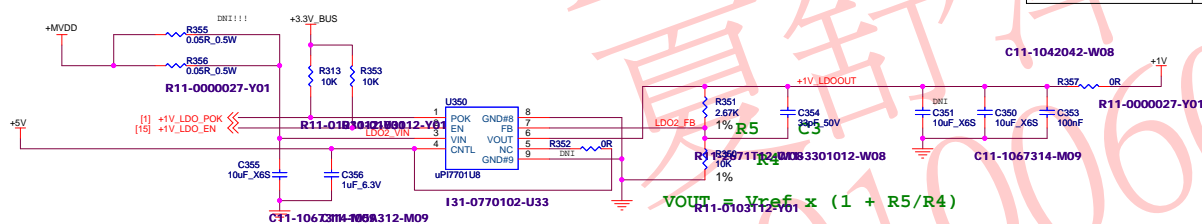
Display Config	Est. Current
DVI+HDMI+DP	1330mA



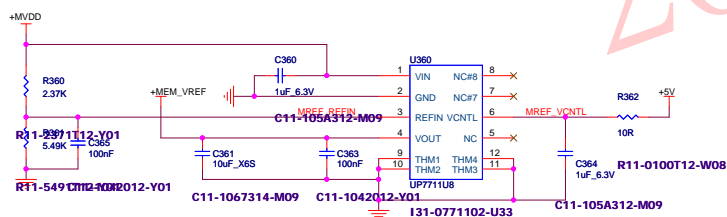
**LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX**  
**PCB: 50 to 70mm sq. copper area for cooling**

1.0V WORST-CASE REQUIREMENT

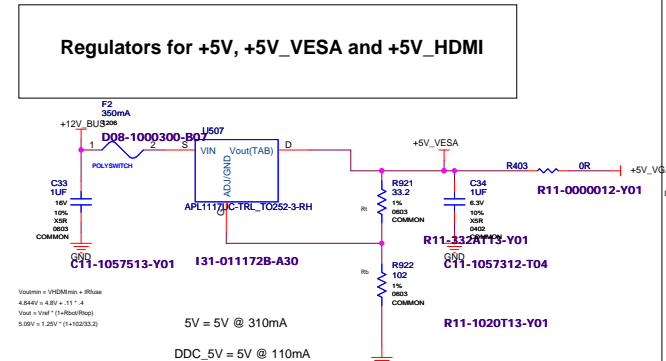
Display Config	Est. Current
DVI+HDMI+DP	1560mA



**Memory VREF:**       $V_{in} = MVDDQ$        $V_{out} = 0.7 \times MVDDQ$

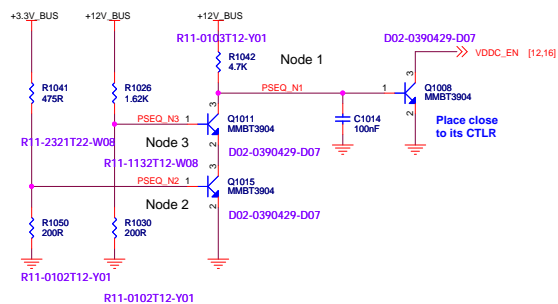


There must be one 100nF at each VREF pin  
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices

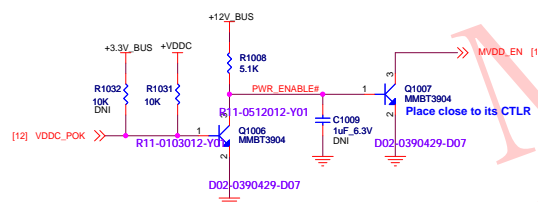


## (16) Power Management - Power Gating and Dynamic Voltage Control

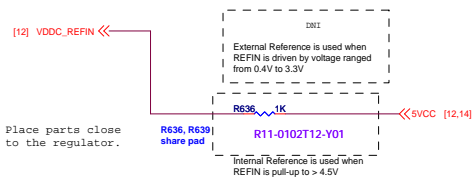
## 12V\_BUS & 3V3\_BUS POWER SEQUENCING



## POWER SEQUENCING CIRCUIT

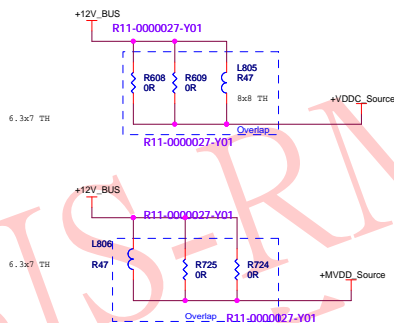
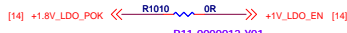


### VDDC Reference Voltage Selection



Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

Install R1010 to gate 1V LDO with 1.8V LDO.



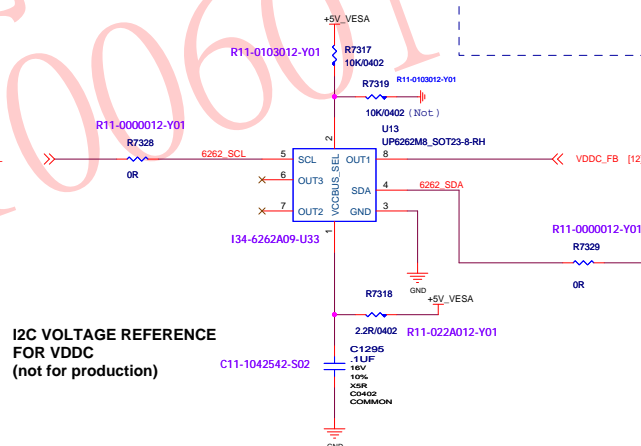
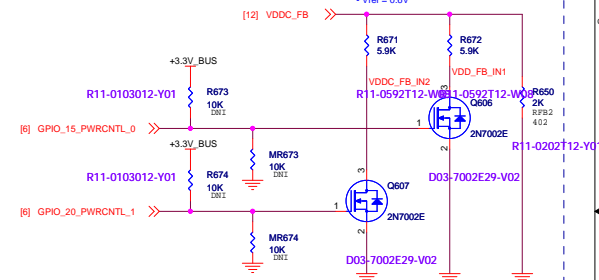
### MVDD Low Side Divider



### VDDC Low Side Divider

R650 must be populated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.

- Hi-Side Divider R651 is Fixed to 5.11K
- $V_o = V_{ref} * (1 + R651 / R650)$
- $V_{ref} = 0.6V$



**I2C VOLTAGE REFERENCE  
FOR VDDC  
(not for production)**

I2C  
ADDRESS:  
A4

I2C  
ADDRESS:  
A4

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Date: Wednesday, April 21, 2010

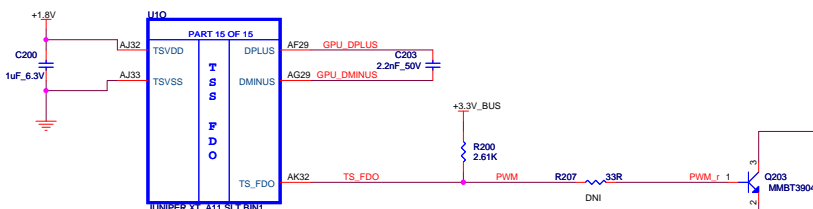
Rev P11

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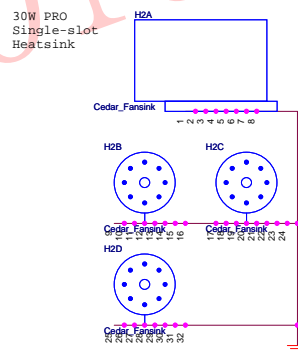
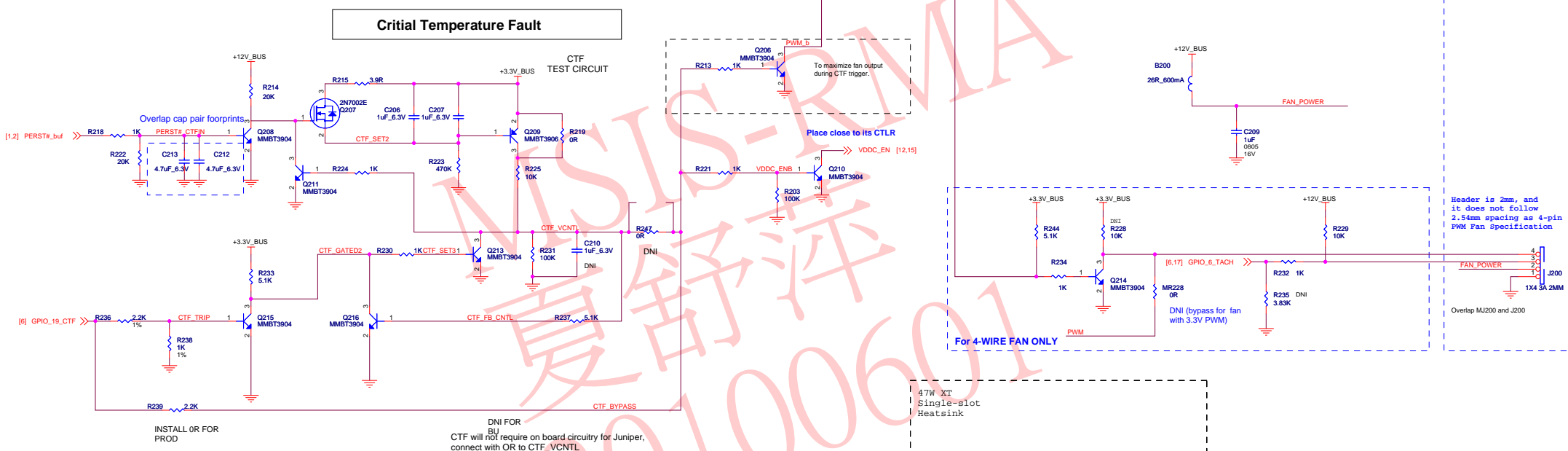
Title	RH REDWOOD GDDR5 1GB VGA/DP+HDMI/DP+DVI	Doc No.	105-C020xx-00C
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## (19) Mechanical and Thermal Management



**Warning: TS\_FDO is not 5V tolerant. MAX sink current 1.65mA**

**If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.**



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Rev D14

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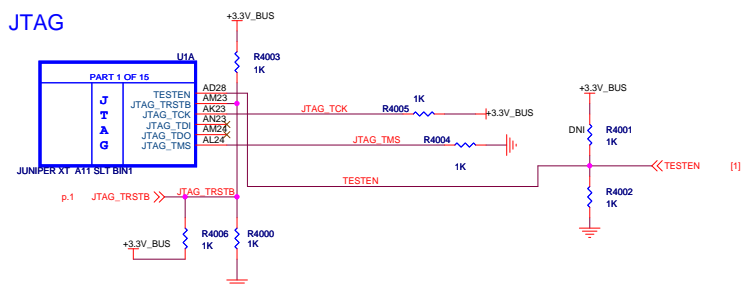
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VI	Doc No. 105-C020yx
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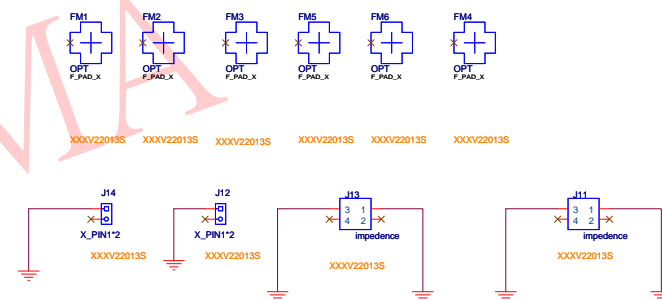
2	
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1	100 002000
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## JTAG



LM96163 FOR BACKUP THERMAL CONTROL



```
J11 8 層 MEM_CLK 80OHM 5.118/7.4803
J13 1 層 TMD5 100 OHM 3.98/11.77
J12 1層 45OHM 5.118/ 12 MEM DATA
J14 8 層 45OHM 5.118/ 12 MEM ADD
```



Place connector on the back side  
(easily accessible and not blocked by the heatsink).

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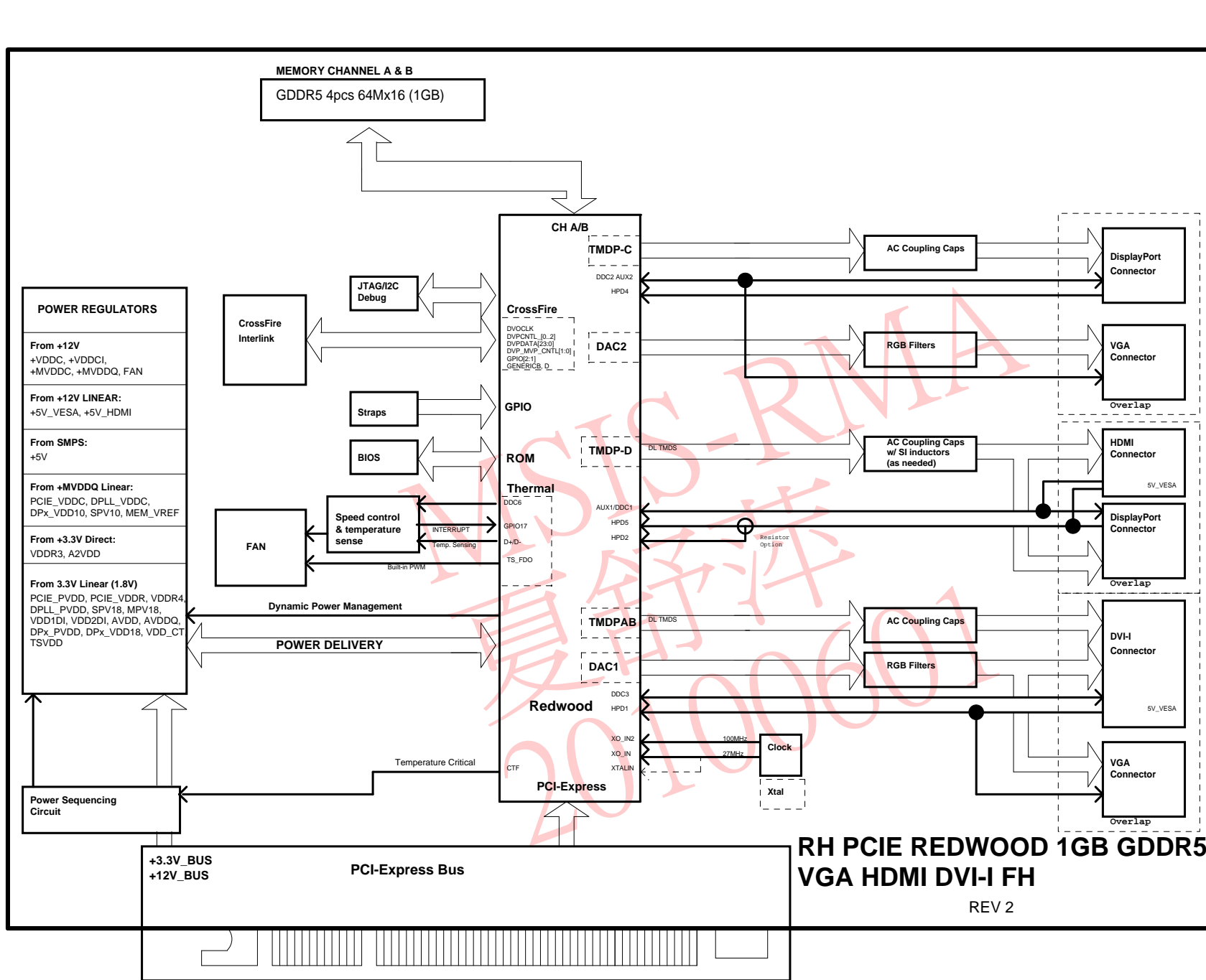
Date: Wednesday, April 21, 2010

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Title **BH REDWOOD GDDR5 1GB VGA/DP+HDMI/DP+DV**

Doc No.	105-C020xx-00C
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**RH PCIE REDWOOD 1GB GDDR5  
VGA HDMI DVI-I FH**  
REV 2



<div>AMD</div>			Title		Schematic No.		Date:				
			RH REDWOOD GDDR5 1GB VGA/DP+HDMI/DP+DVI		105-C020xx-00C		Wednesday, April 21, 2010				
			REVISION HISTORY					NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.		Rev P11	
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION								
00	00A	2009/05/08									
01	00B	2009/08/20									
02	00C	2009/09/28	REDWOOD XT GDDR5 1GB - Initial Release								

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