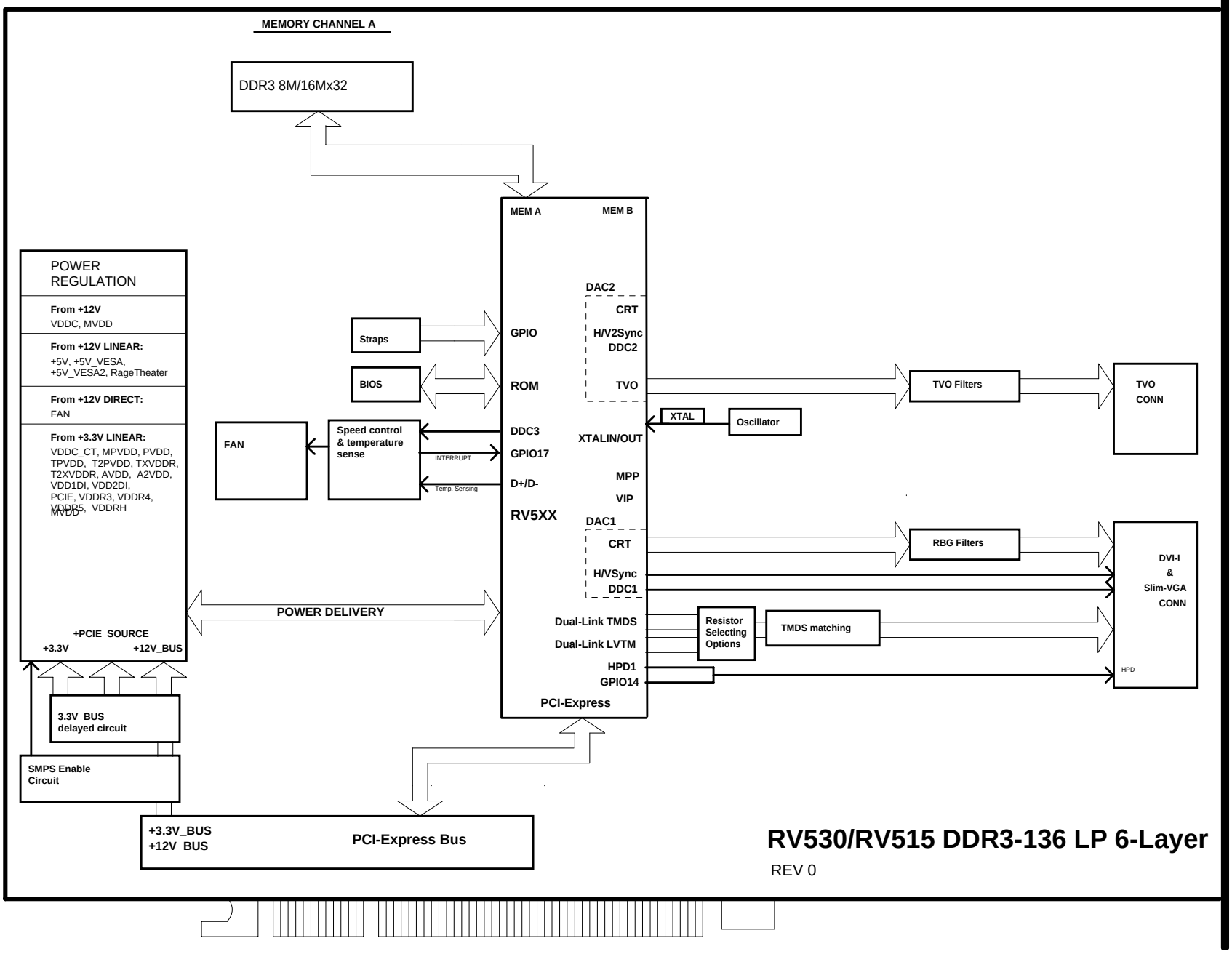
<variant Name>

Title	Schematic No.	Date:
RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP	105-A843xx-00	Thursday, November 03, 2005

REVISION HISTORY

Rev 1

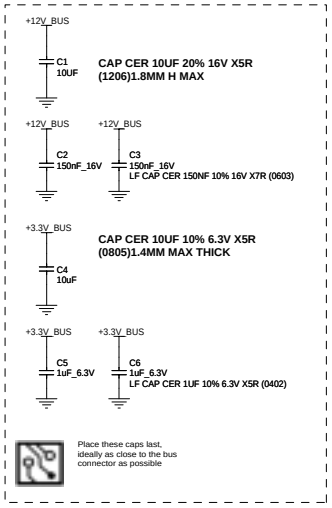
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	05/09/07	Design based on A683-00A - Change memory channel from A0/A1 to A0/B0 - Add dynamic VDDC support - Add CrossFire Slave support
1	00	05/10/24	- Add CrossFire slave support (GPIO_5) - Add internal HDCP support - Add 5V reference option for 2.5V REG - Add C987 for linear MVDD REG - Add op-amp fan control circuit

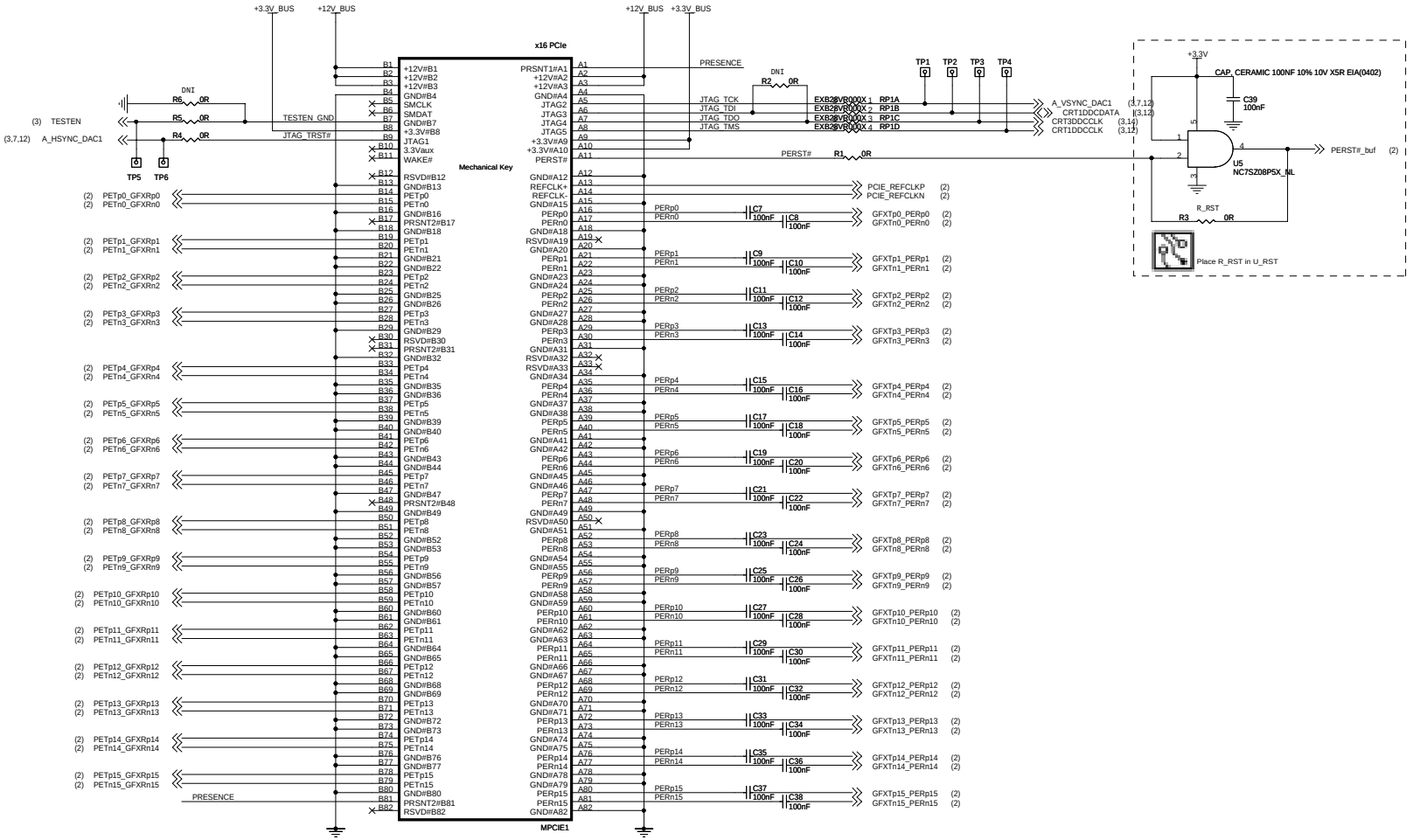


ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

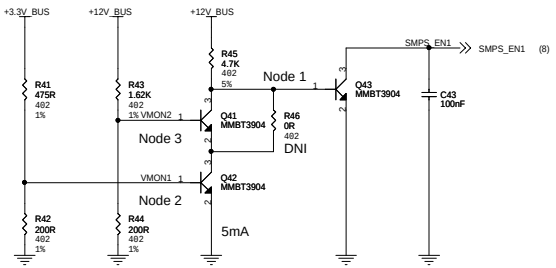
Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP	
Size C	Document Number 105-A843xx-00	Rev 1
Date: Thursday, November 03, 2005	Sheet 17 of 17	

PCI-EXPRESS EDGE CONNECTOR





POWER SEQUENCING



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

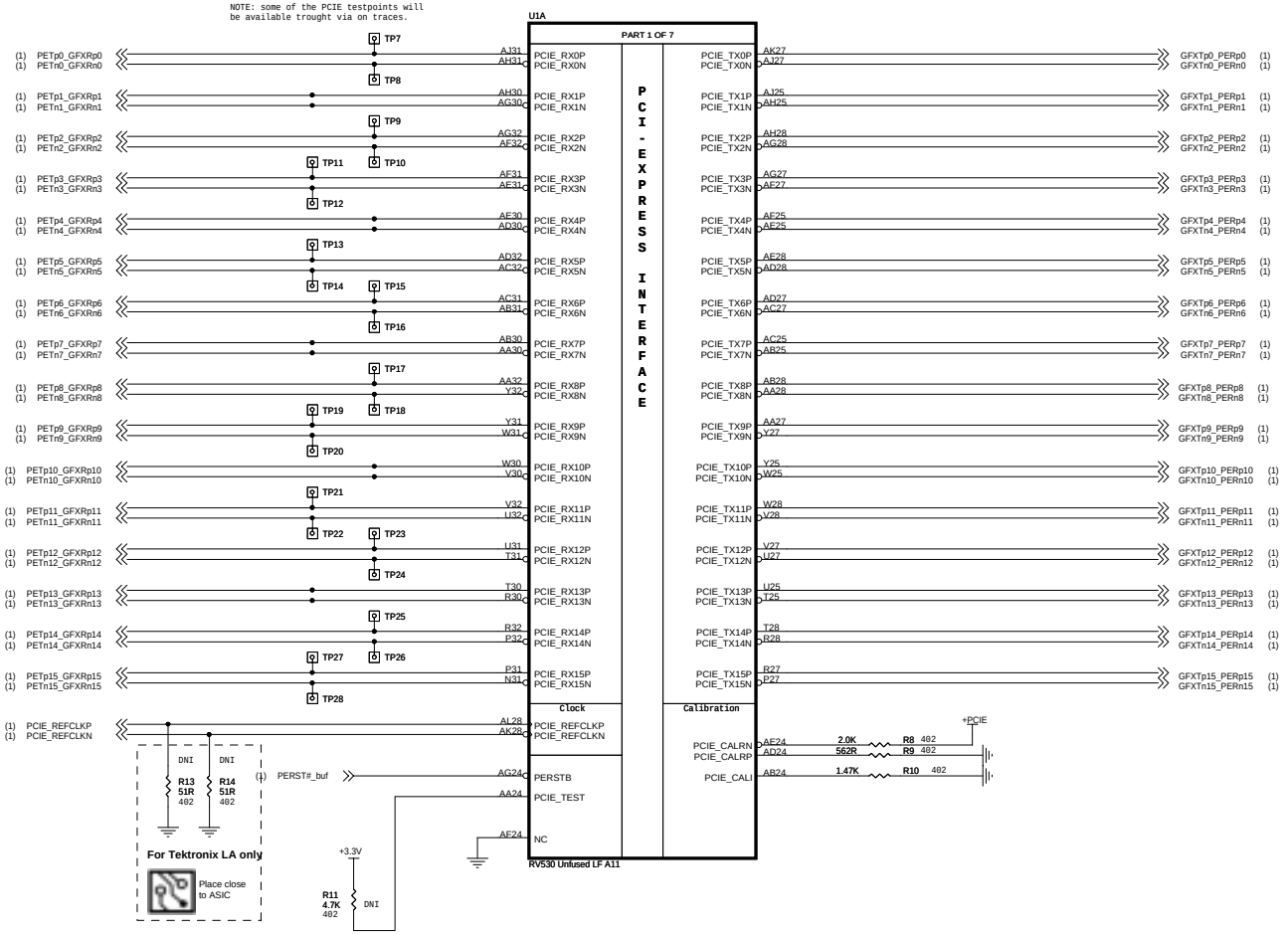
Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

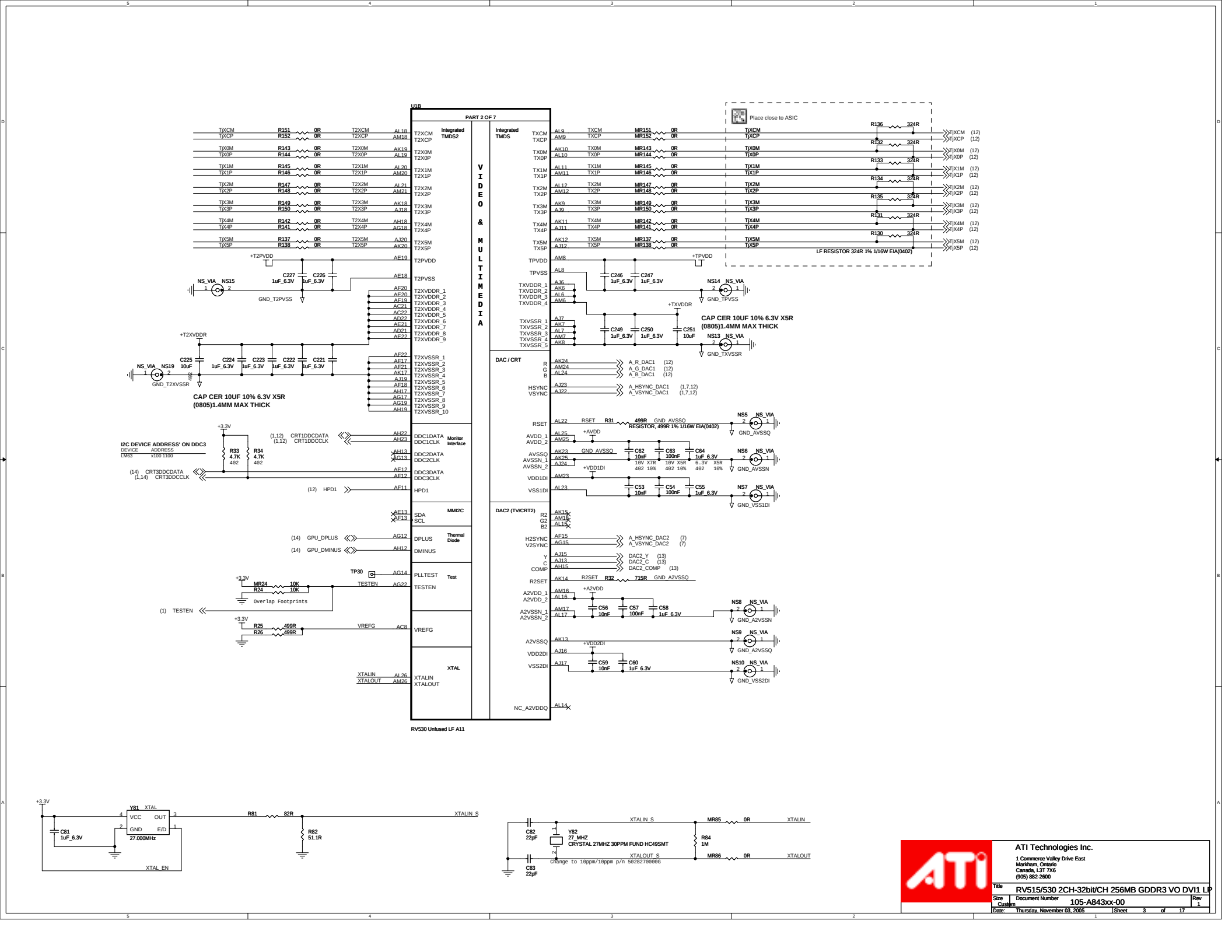
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

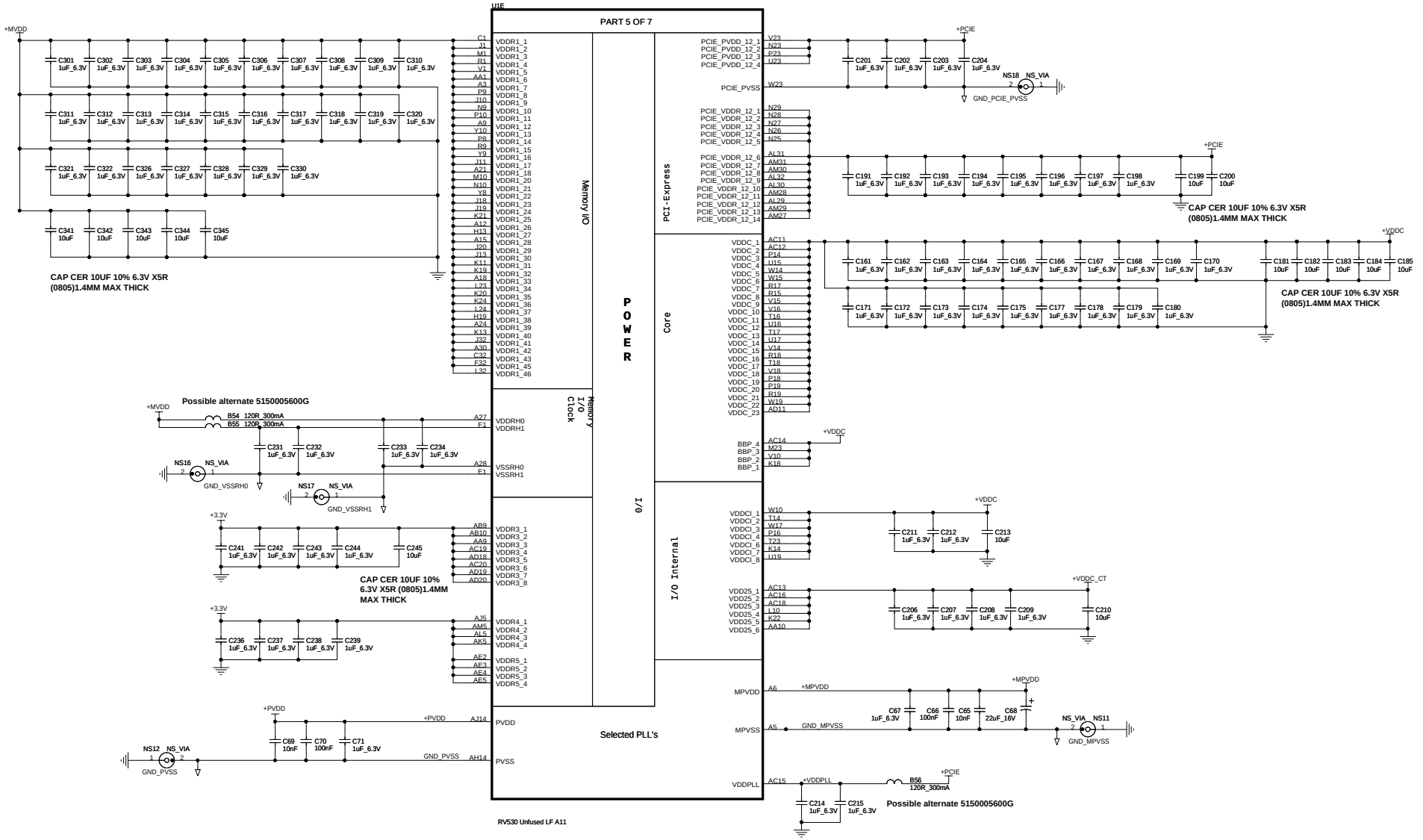
Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP	
Size C	Document Number 105-A843xx-00	Rev 1
Date: Thursday, November 03, 2005	Sheet 1 of 17	



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

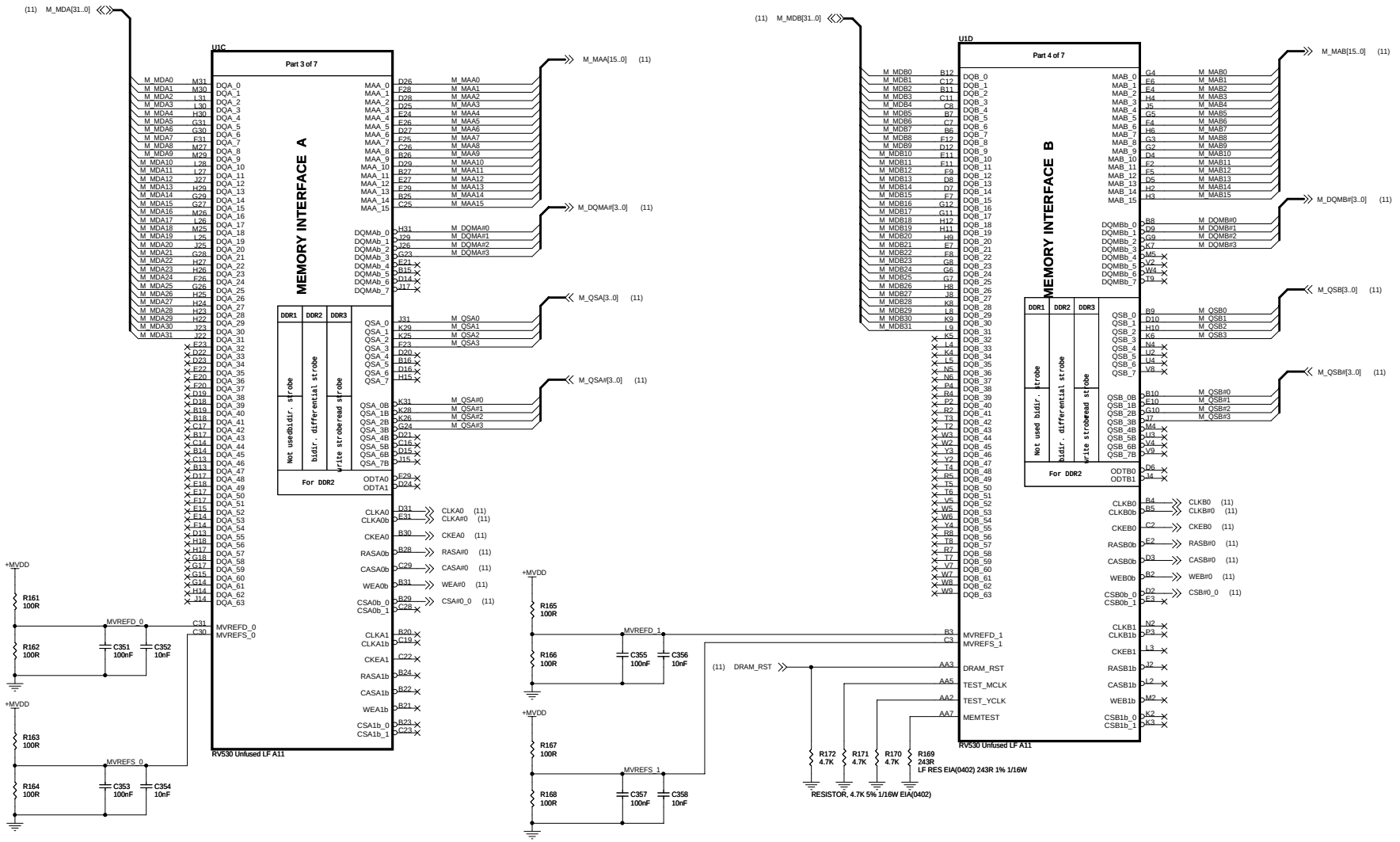
Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP		
Size C	Document Number 105-A843xx-00		Rev 1
Date: Thursday, November 03, 2005	Sheet 2 of 17		


U1B
PART 2 OF 7
VIDEO & MULTIMEDIA
Integrated TMDS2
Integrated TMDS
Monitor Interface
MMI2C
Thermal Diode
Test
XTAL
DAC / CRT
DAC2 (TV/CRT2)
Place close to ASIC
LF RESISTOR 324R 1% 1/16W EIA(0402)
CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK
I2C DEVICE ADDRESS' ON DDC3
RESISTOR, 499R 1% 1/16W EIA(0402)
Overlap Footprints
RV530 Unfused LF A11
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600
RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP
105-A843xx-00
Thursday, November 03, 2005



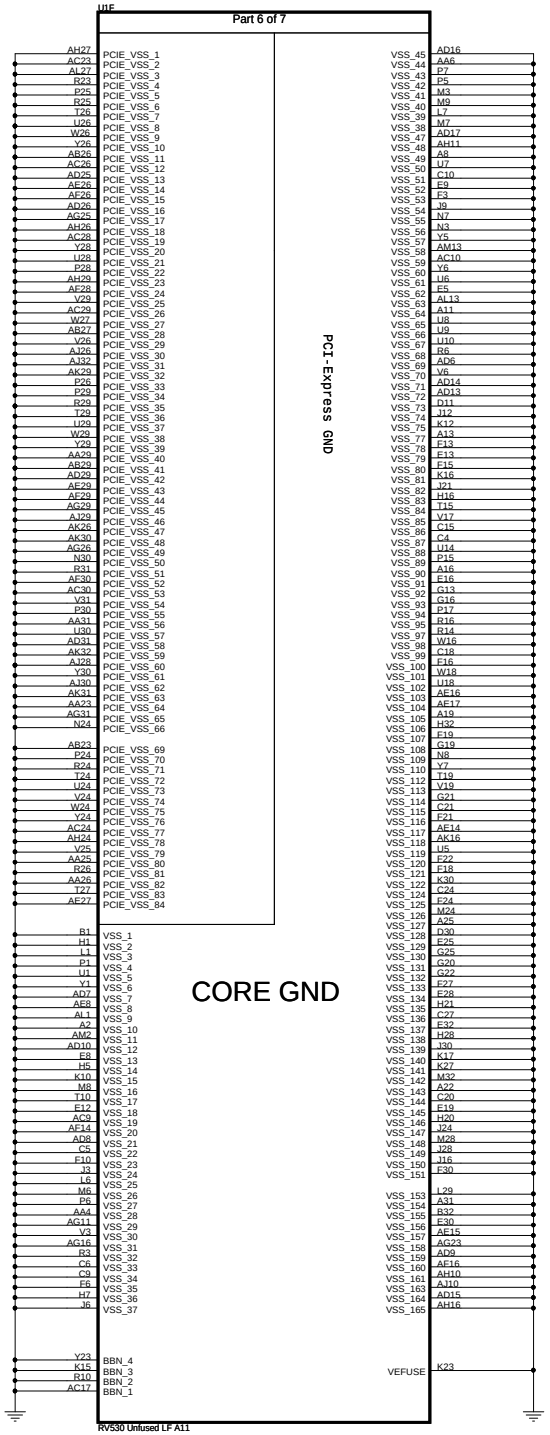
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP		
Size C	Document Number 105-A843xx-00		Rev 1
Date: Thursday, November 03, 2005	Sheet 4	of 17	



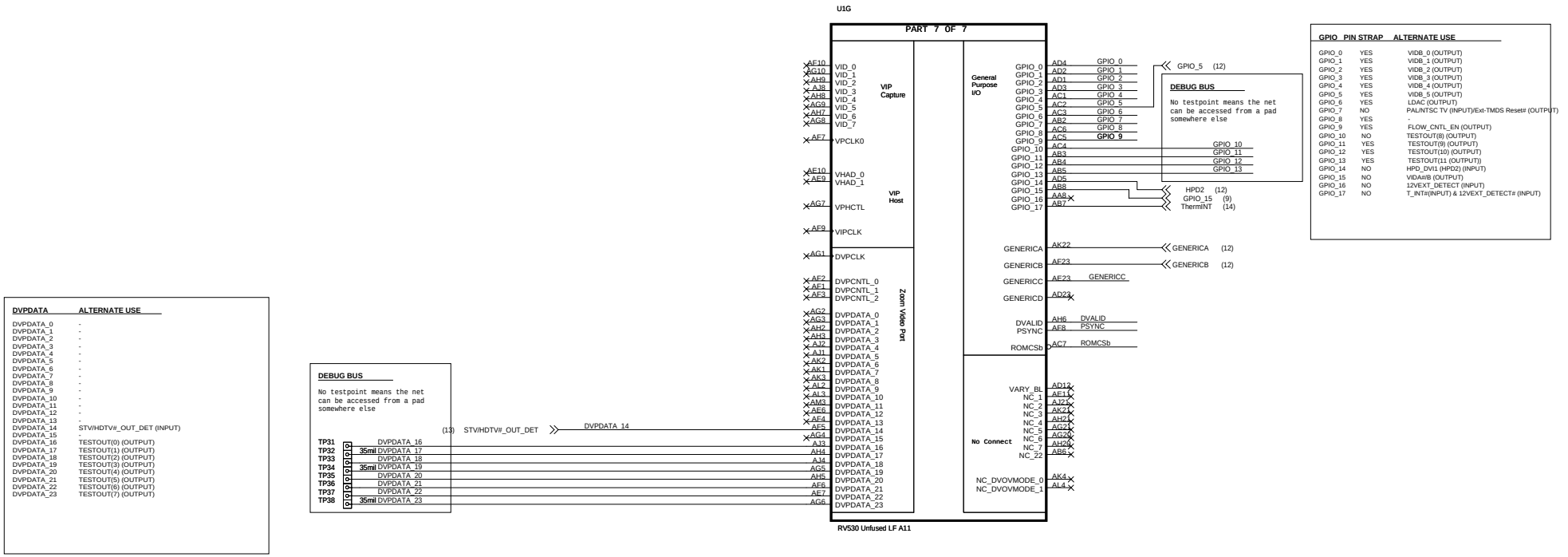
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP		
Size C	Document Number 105-A843xx-00		Rev 1
Date: Thursday, November 03, 2005		Sheet 5 of 17	



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

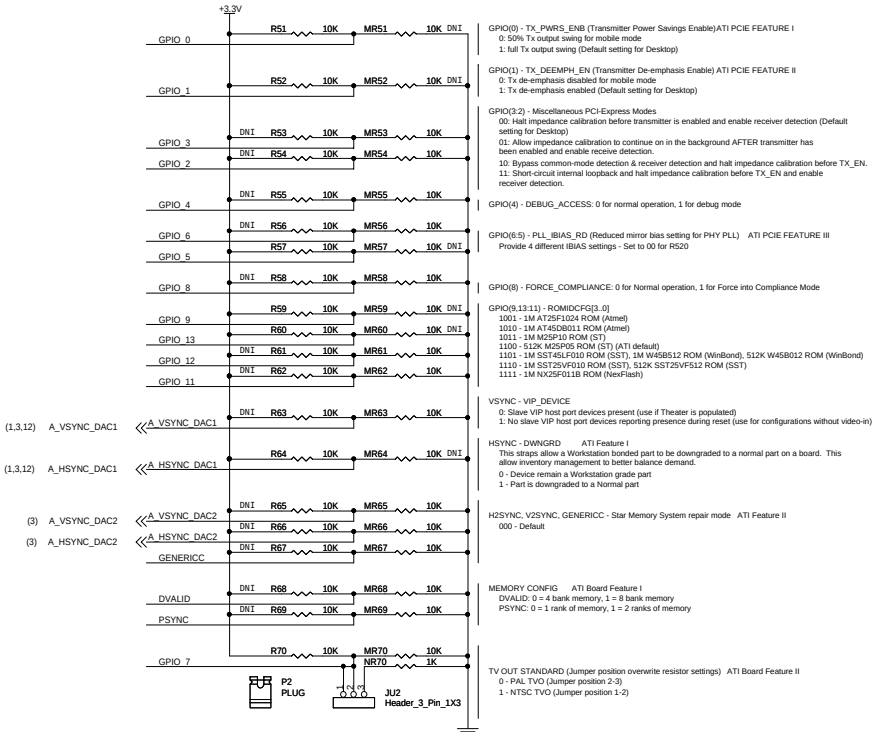
Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP	
Size C	Document Number 105-A843xx-00	Rev 1
Date: Thursday, November 03, 2005	Sheet 6 of 17	

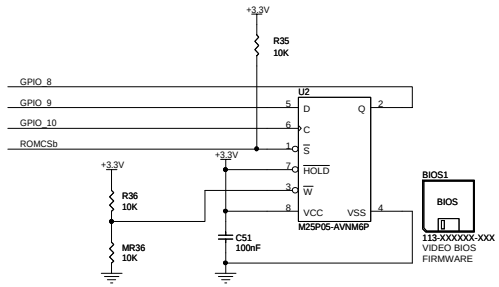


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)/Ext-TMDS Reset# (OUTPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDAtriB (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

DVPDATA	ALTERNATE USE
DVPDATA_0	-
DVPDATA_1	-
DVPDATA_2	-
DVPDATA_3	-
DVPDATA_4	-
DVPDATA_5	-
DVPDATA_6	-
DVPDATA_7	-
DVPDATA_8	-
DVPDATA_9	-
DVPDATA_10	-
DVPDATA_11	-
DVPDATA_12	-
DVPDATA_13	-
DVPDATA_14	STV/HDTV#_OUT_DET (INPUT)
DVPDATA_15	-
DVPDATA_16	TESTOUT(0) (OUTPUT)
DVPDATA_17	TESTOUT(1) (OUTPUT)
DVPDATA_18	TESTOUT(2) (OUTPUT)
DVPDATA_19	TESTOUT(3) (OUTPUT)
DVPDATA_20	TESTOUT(4) (OUTPUT)
DVPDATA_21	TESTOUT(5) (OUTPUT)
DVPDATA_22	TESTOUT(6) (OUTPUT)
DVPDATA_23	TESTOUT(7) (OUTPUT)

PIN BASED STRAPS

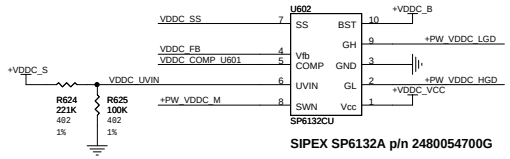




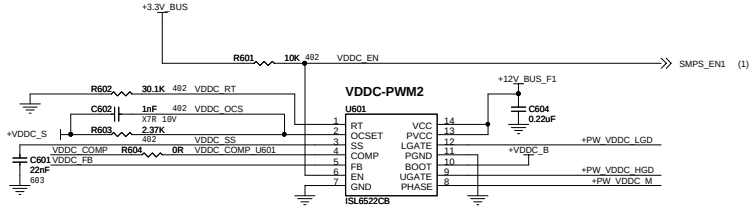
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP		
Size C	Document Number 105-A843xx-00		Rev 1
Date: Thursday, November 03, 2005		Sheet 7 of 17	

VDDC-PWM1

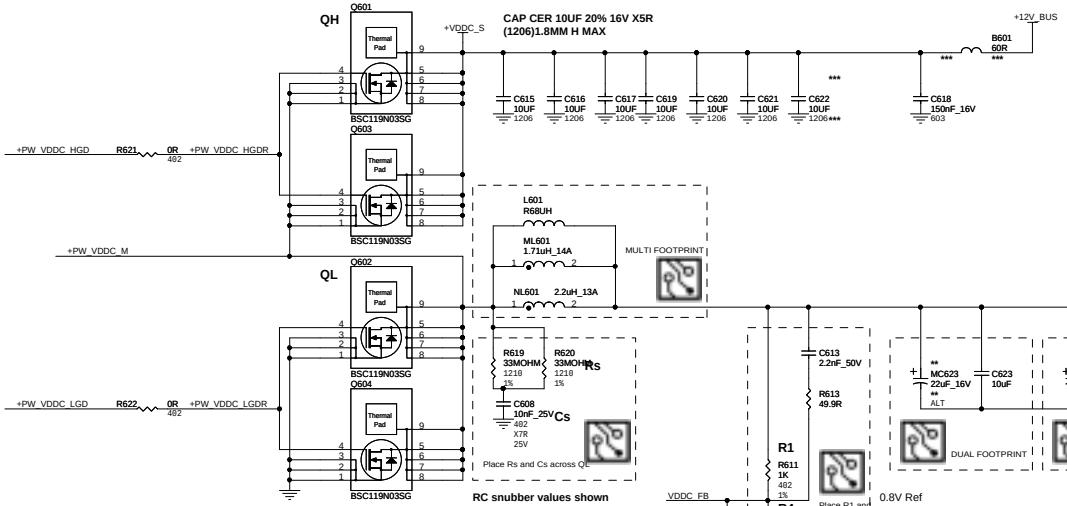


SIPEX SP6132A p/n 2480054700G

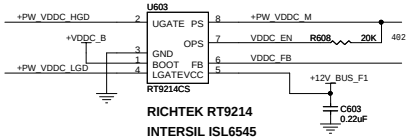


VDDC-PWM2

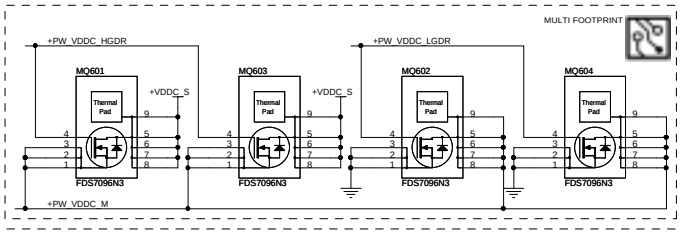
INTERSIL ISL6522/ISL6535
RICHTEK RT9232/RT9232A
ANPEC APW7062A
ANPEC APW7062B



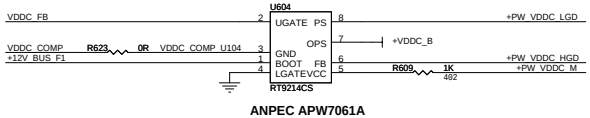
VDDC-PWM3



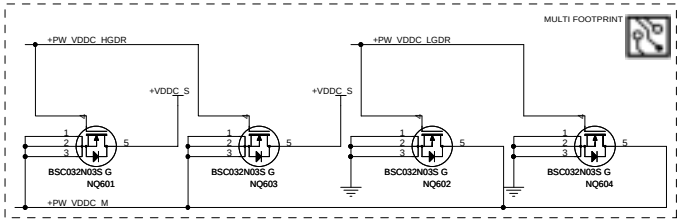
RICHTEK RT9214
INTERSIL ISL6545

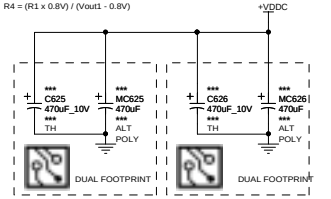


VDDC-PWM4



ANPEC APW7061A

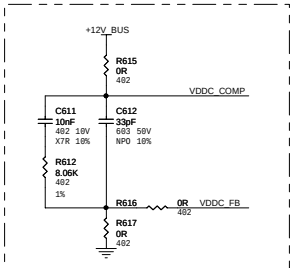




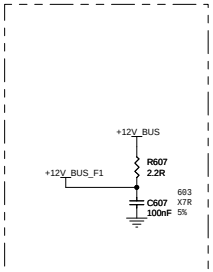
CAP AE 470UF 20% 10V 10x12 .5MM LOW ESR

LF CAP, AL/POLY, 470UF 6.3V, LOW ESR, 8MM DIA, SMT

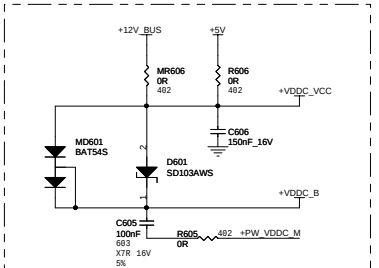
COMPENSATION CIRCUIT



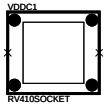
FILTERED +12V_BUS



BOOT CIRCUIT



This symbol is used for 103 SMPS p/n.



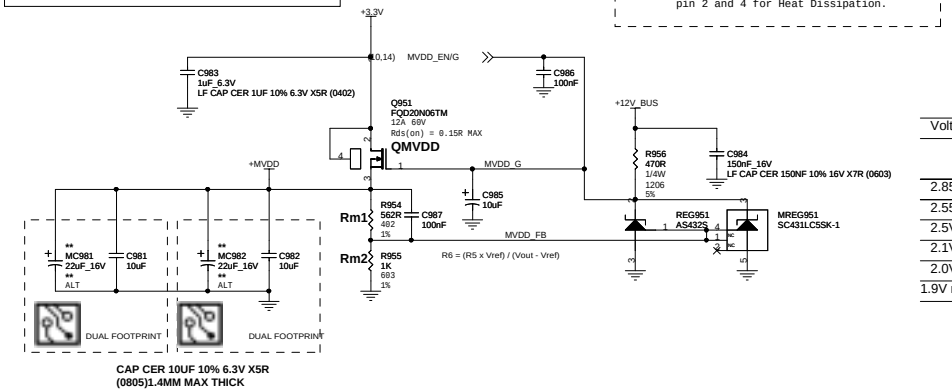
Regulator for VDDC (ASIC Core)
Vout = 1V ~ 1.3V

Part	Vout	R1	R2
0.8V Ref	1.2V	1.00K 1%	2.00K 1%
	1.25V	1.00K 1%	1.78K 1%
	1.3V	1.00K 1%	1.6K 1%

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

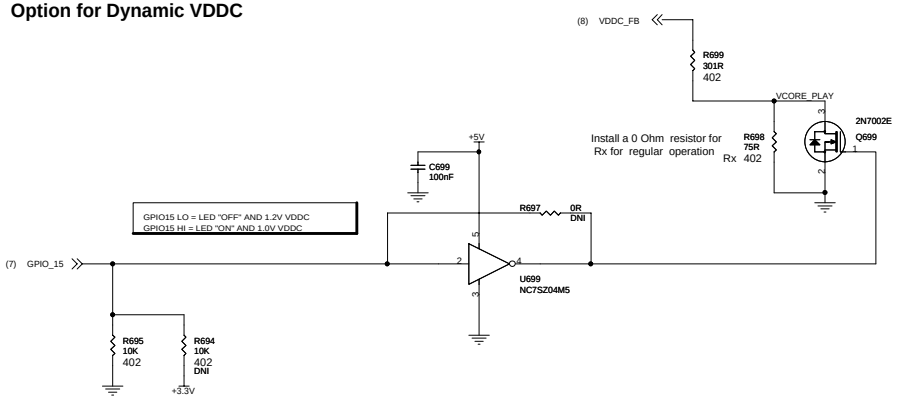
Title: RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP
Size: Custom | Document Number: 105-A843xx-00 | Rev: 1
Date: Thursday, November 03, 2005 | Sheet 8 of 17

Regulator for +MVDDQ
Vout = 1.85V ~ 2.65V
Iout = 1.7A MAX
P_QMVDD = 2.5W MAX



Voltage Req.	Rm1		Rm2		
2.85V					
2.55V	22.1R	316022R100G	1.1K	3240110100G	2.5V Ref.
2.5V	0R	3150000000	DNI		2.5V Ref.
2.1V min	681R	3160681000G	953R	3240953000	1.24V Ref.
2.0V min	681R	3160681000G	1.1K	3240110100G	1.24V Ref.
1.9V min, 1.94V nom.	562R	3160562000G	1K	3160100100G	1.24V Ref.

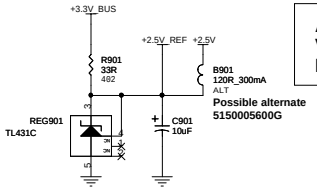
Option for Dynamic VDDC

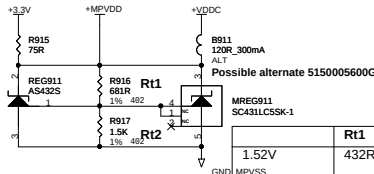


ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

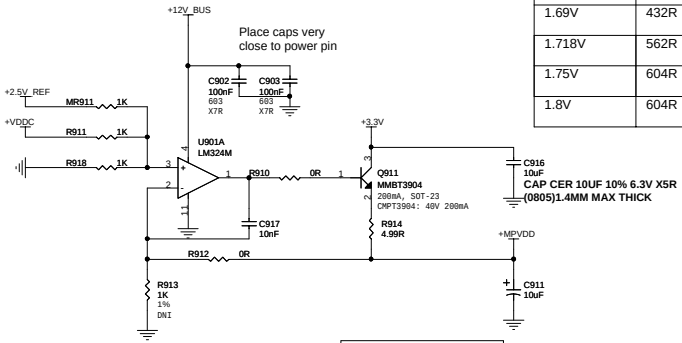
Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP	
Size: Custom	Document Number: 105-A843xx-00	Rev: 1
Date: Thursday, November 03, 2005	Sheet 9 of 17	

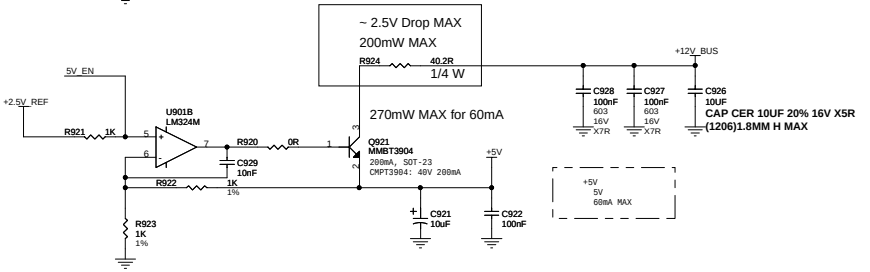
Alt regulator for +MPVDD
Vout = 1.2V (not tracking to VDDC)
Iout = 10mA MAX

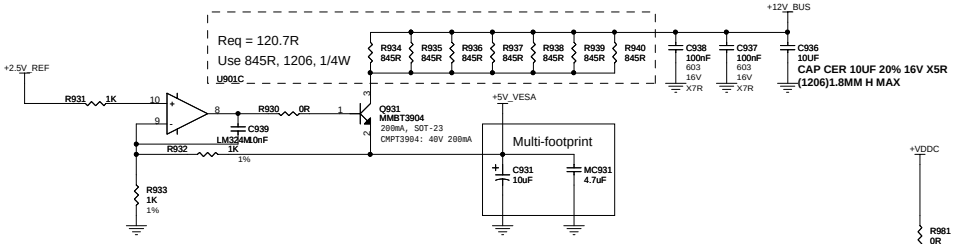




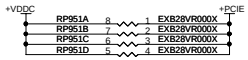
	Rt1		Rt2	
1.52V	432R	3240432000 3160432000	2.15K	3160215100
1.61V	432R	3240432000	1.5K 1.5K	3230015200 3160150100
1.69V	432R	3240432000	1.21K	3240121100
1.718V	562R	3240562000	1.5K 1.5K	3230015200 3160150100
1.75V	604R	3160604000	1.5K 1.5K	3230015200 3160150100
1.8V	604R	3160604000	1.37K	3160137100

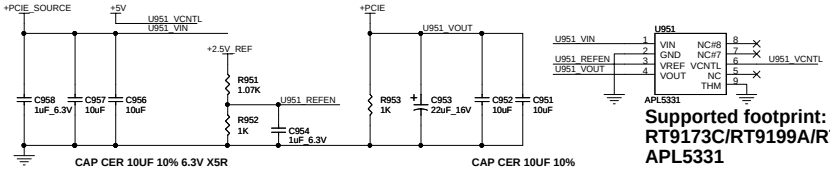






Optional regulator for +PCIE
Vout = 1.2V ~1.25V
Iout = 1.2A MAX





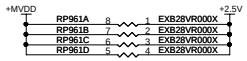
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

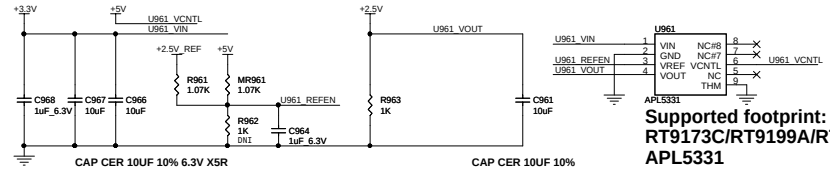
CAP CER 10UF 10%
6.3V X5R (0805)1.4MM
MAX THICK

Supported footprint:
RT9173C/RT9199A/RT9199
APL5331

RT9199 p/n 2480054800G (480mR RdsON Max)
RT9199A (300mR RdsON Max)
RT9173C (250mR RdsON Max)
APL5331 p/n 2480054200G (350mR MAX for 2A)

Optional regulator for +2.5V
Vout = 2.5V
Iout = 600mA MAX



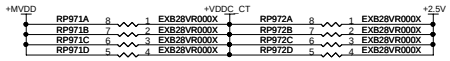


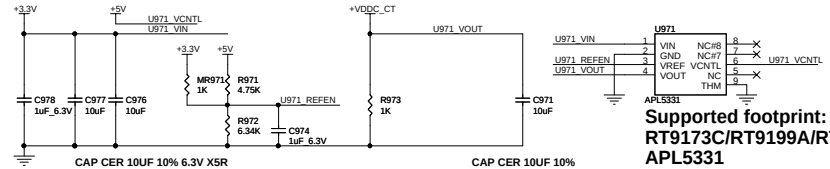
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

CAP CER 10UF 10%
6.3V X5R (0805)1.4MM
MAX THICK

Supported footprint:
RT9173C/RT9199A/RT9199
APL5331

Optional Regulator for +VDDC_CT
Vout = 2.5V ~ 2.85V
Iout = 100mA MAX

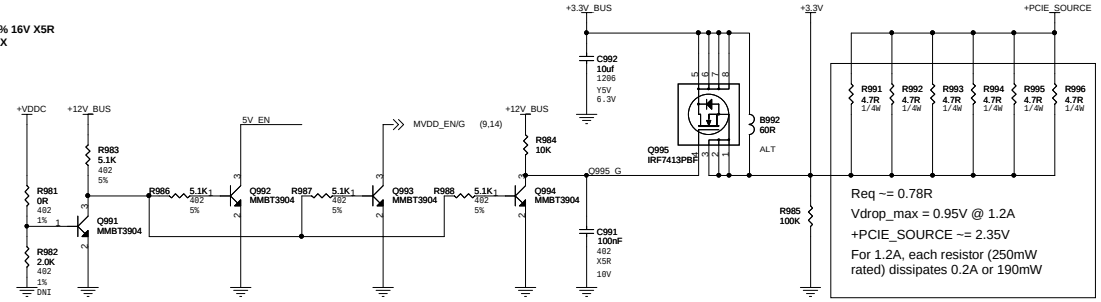




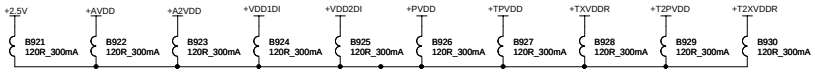
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

CAP CER 10UF 10%
6.3V X5R (0805)1.4MM
MAX THICK

Supported footprint:
RT9173C/RT9199A/RT9199
APL5331



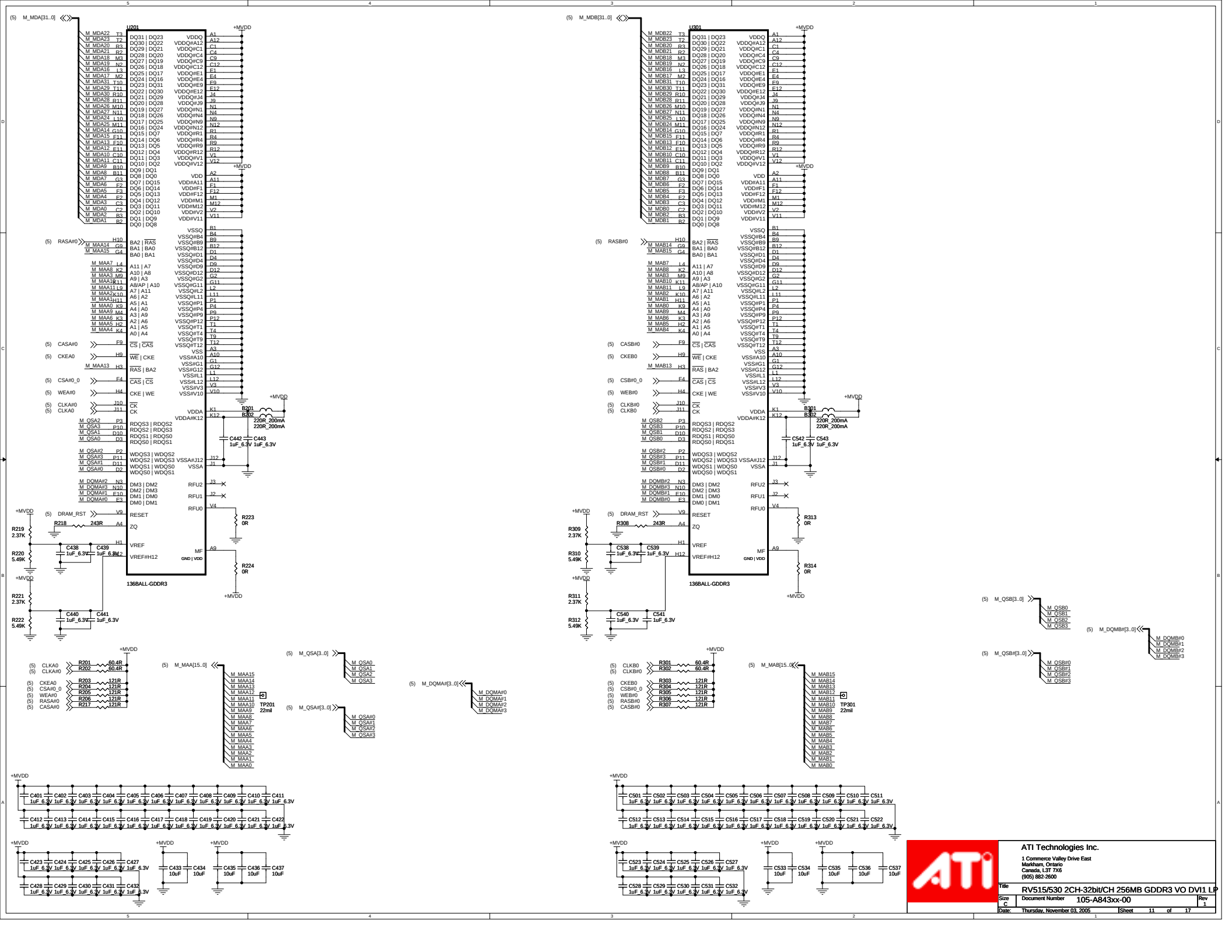
Req ~= 0.78R
Vdrop_max = 0.95V @ 1.2A
+PCIE_SOURCE ~= 2.35V
For 1.2A, each resistor (250mW rated) dissipates 0.2A or 190mW

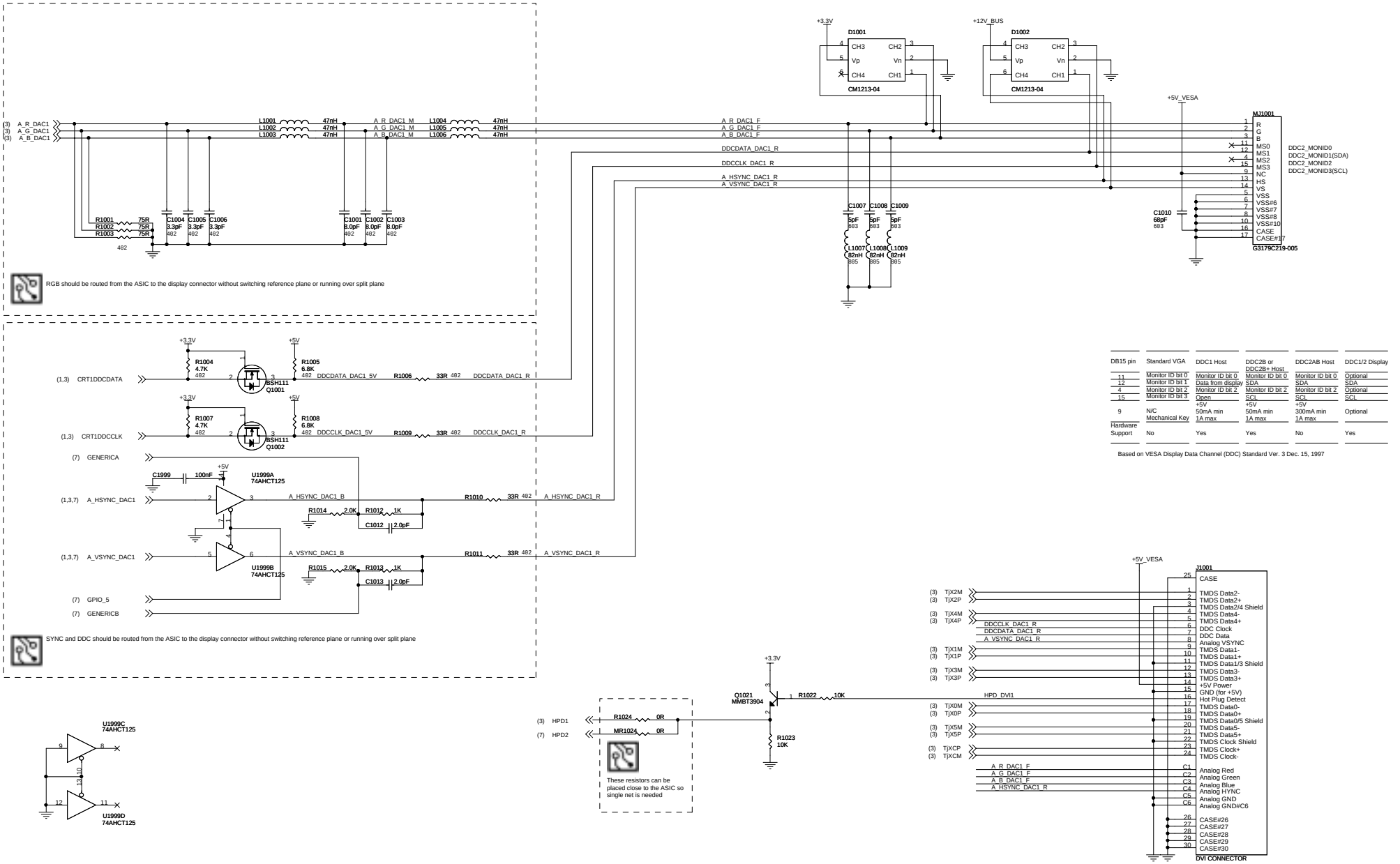


Possible alternate 5150005600G

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP	
Size C	Document Number 105-A843xx-00	Rev 1
Date: Thursday, November 03, 2005	Sheet 10 of 17	


(5) M_MDA[31..0]
U201
136BALL-GDDR3
(5) M_MDB[31..0]
U301
136BALL-GDDR3
+MVDD
(5) RASA#0
(5) CASA#0
(5) CKEA0
(5) WEA#0
(5) CSA#0_0
(5) CLKA#0
(5) CLKA0
(5) DRAM_RST
(5) RASB#0
(5) CASB#0
(5) CKEB0
(5) WEB#0
(5) CSB#0_0
(5) CLKB#0
(5) CLKB0
B201 220R_200mA
B202 220R_200mA
B301 220R_200mA
B302 220R_200mA
R218 243R
R219 2.37K
R220 5.49K
R221 2.37K
R222 5.49K
R223 0R
R224 0R
R308 243R
R309 2.37K
R310 5.49K
R311 2.37K
R312 5.49K
R313 0R
R314 0R
C438 1uF_6.3V
C439 1uF_6.3V
C440 1uF_6.3V
C441 1uF_6.3V
C442 1uF_6.3V
C443 1uF_6.3V
C538 1uF_6.3V
C539 1uF_6.3V
C540 1uF_6.3V
C541 1uF_6.3V
C542 1uF_6.3V
C543 1uF_6.3V
R201 60.4R
R202 60.4R
R203 121R
R204 121R
R205 121R
R206 121R
R217 121R
R301 60.4R
R302 60.4R
R303 121R
R304 121R
R305 121R
R306 121R
R307 121R
(5) M_MAA[15..0]
(5) M_QSA[3..0]
(5) M_QSA#[3..0]
(5) M_DQMA#[3..0]
(5) M_MAB[15..0]
(5) M_QSB[3..0]
(5) M_QSB#[3..0]
(5) M_DQMB#[3..0]
TP201 22mil
TP301 22mil
C401 C402 C403 C404 C405 C406 C407 C408 C409 C410 C411 1uF_6.3V
C412 C413 C414 C415 C416 C417 C418 C419 C420 C421 C422 1uF_6.3V
C423 C424 C425 C426 C427 1uF_6.3V
C428 C429 C430 C431 C432 1uF_6.3V
C433 C434 10uF
C435 C436 C437 10uF
C501 C502 C503 C504 C505 C506 C507 C508 C509 C510 C511 1uF_6.3V
C512 C513 C514 C515 C516 C517 C518 C519 C520 C521 C522 1uF_6.3V
C523 C524 C525 C526 C527 1uF_6.3V
C528 C529 C530 C531 C532 1uF_6.3V
C533 C534 10uF
C535 C536 C537 10uF
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600
Title RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP
Size C
Document Number 105-A843xx-00
Rev 1
Date: Thursday, November 03, 2005
Sheet 11 of 17

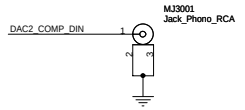


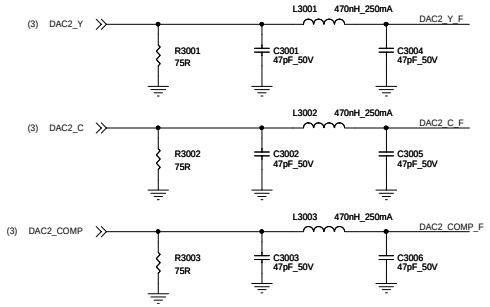
DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
Mechanical Key		1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

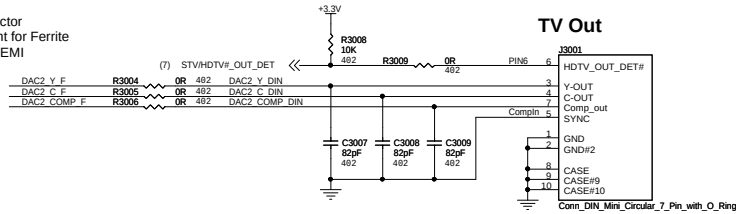
Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP	
Size: Custom	Document Number: 105-A843xx-00	Rev: 1
Date: Thursday, November 03, 2005	Sheet 12 of 17	





Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI

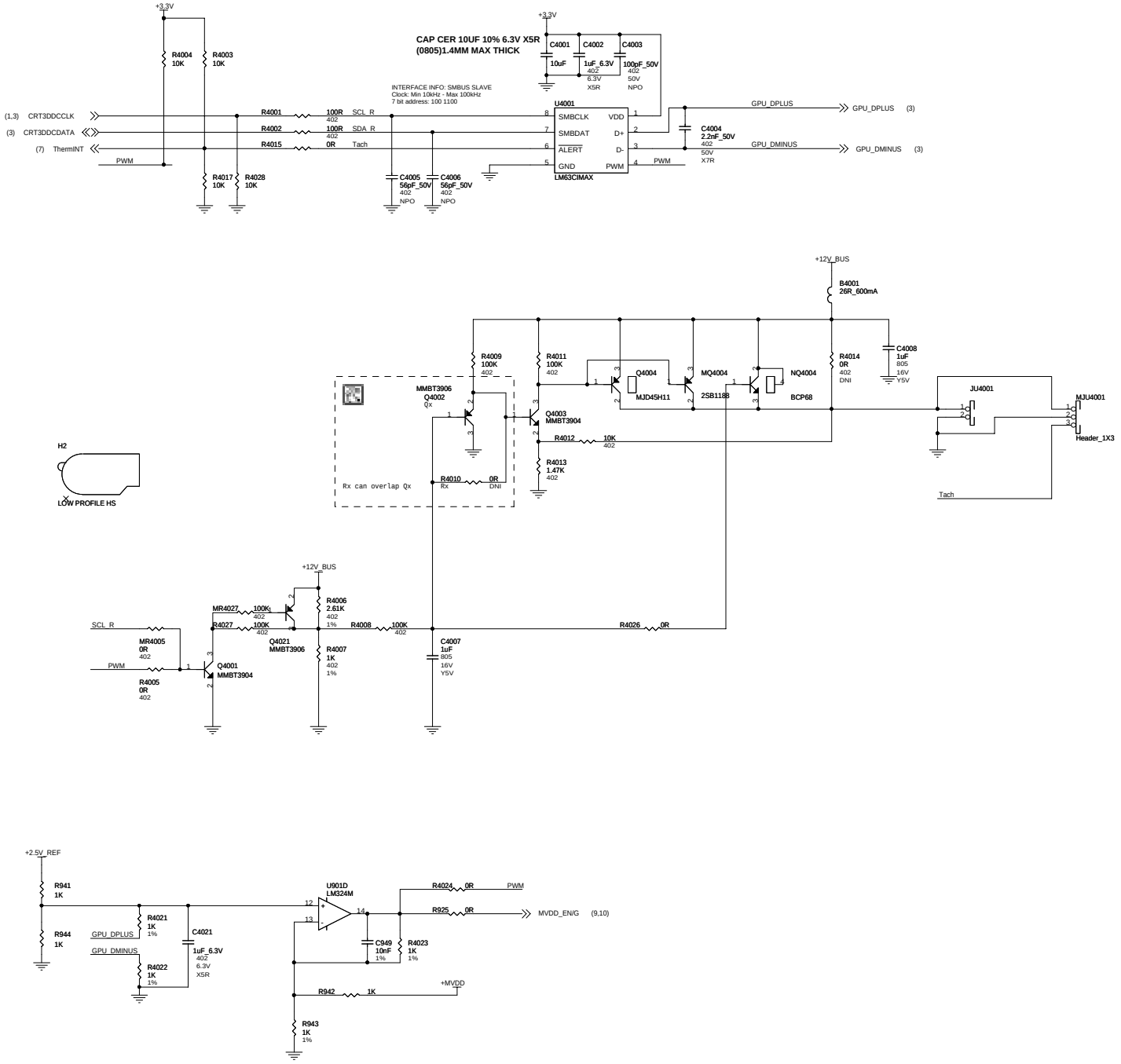
TV Out



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP	
Size C	Document Number 105-A843xx-00	Rev 1
Date: Thursday, November 03, 2005	Sheet 13 of 17	



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP	
Size C	Document Number 105-A843xx-00	Rev 1
Date: Thursday, November 03, 2005	Sheet 14 of 17	

DVI/VGA SCREWS

ASSY-SCREW1

SCREW
JACKSCREW
ASSY
7020000800

ASSY-SCREW2

SCREW
JACKSCREW
ASSY
7020000800

ASSY-SCREW5

SCREW
PAN_HEAD
7020001700

MT1
MT_Hole_0.136_in.
DNI

MT2
MT_Hole_0.136_in_6VIA
DNI

DNI

SK1

RV410SOCKET

PCB1

RV410SOCKET

<Variant Name>

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title: RV515/530 2CH-32bit/CH 256MB GDDR3 VO DVI1 LP

Size: C | Document Number: 105-A843xx-00 | Rev: 1

Date: Thursday, November 03, 2005 | Sheet 15 of 17