

# PG150-C03

384b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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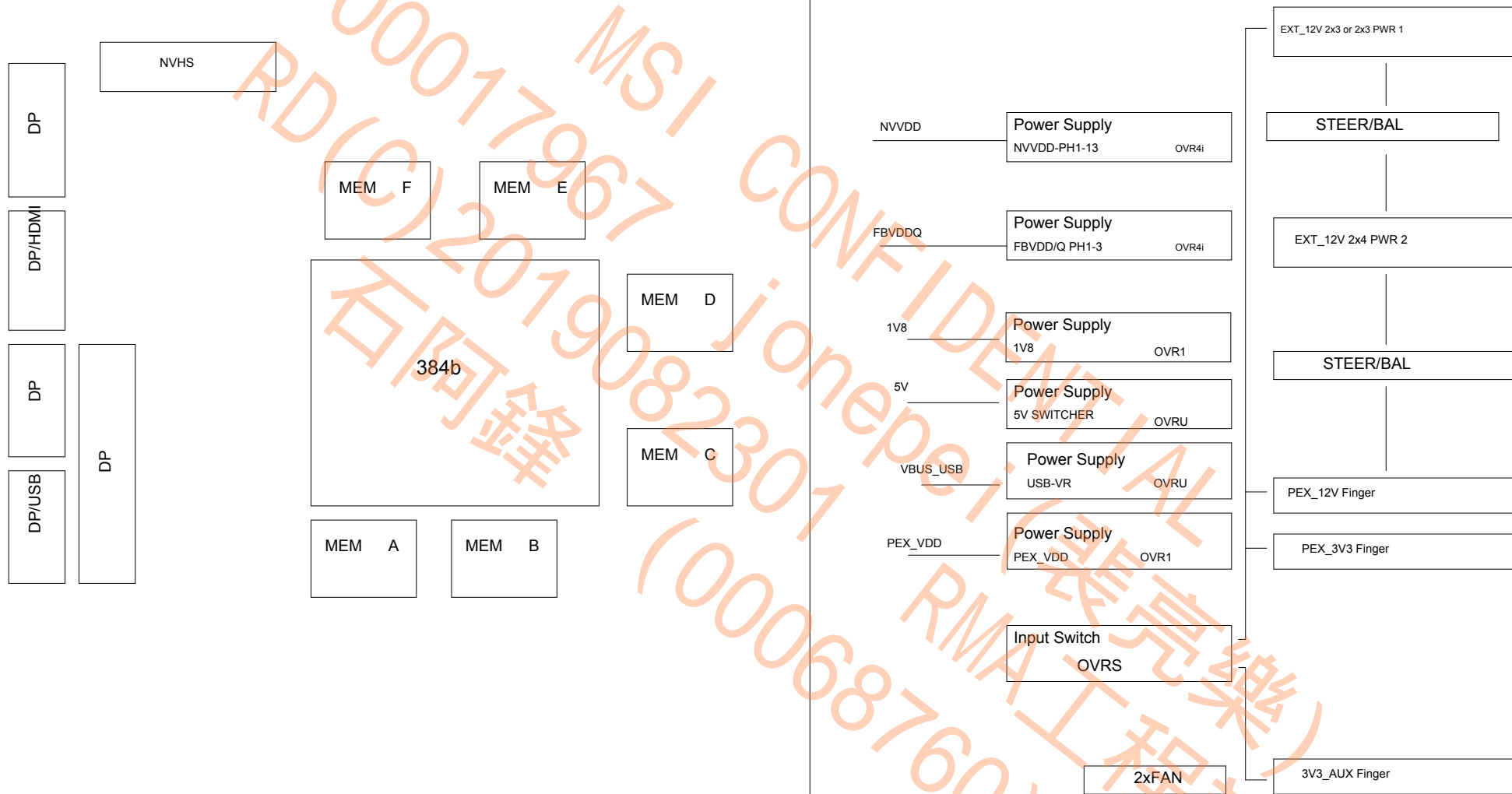
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Block Diagram



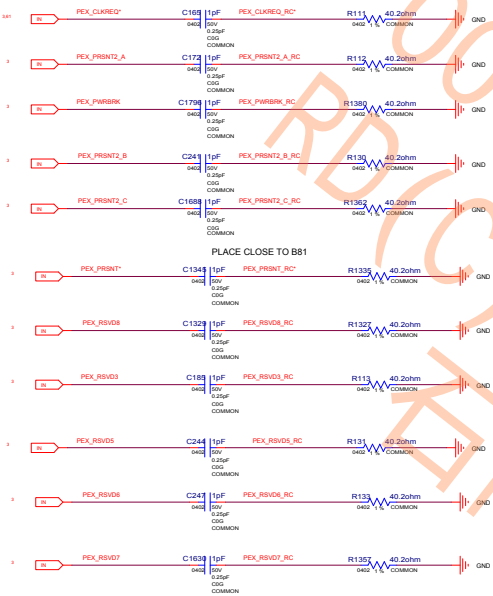
PCI Express



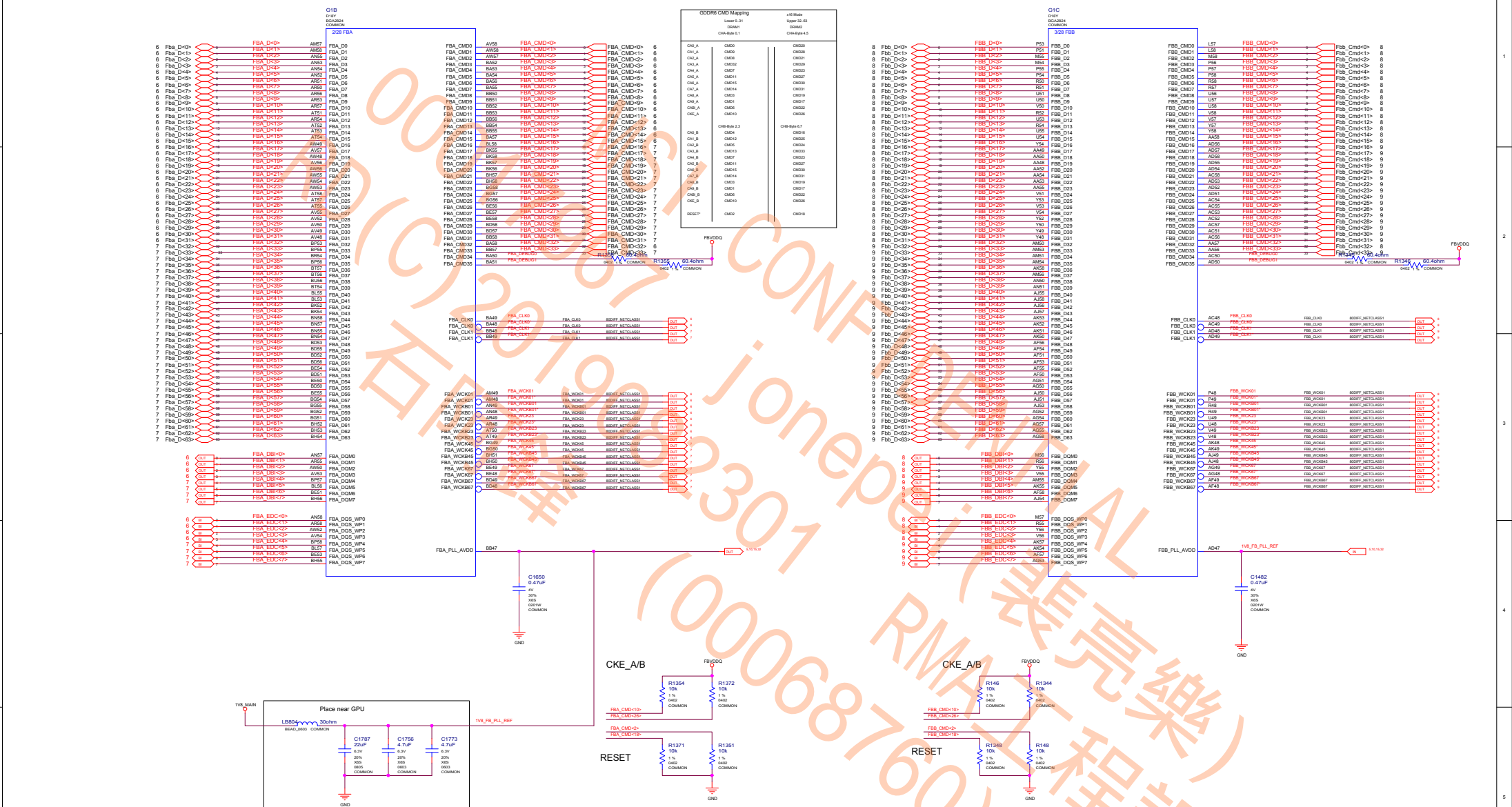
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**MS-V371**

Size Custom	Document Description <b>PCIE</b>	Rev 6.0
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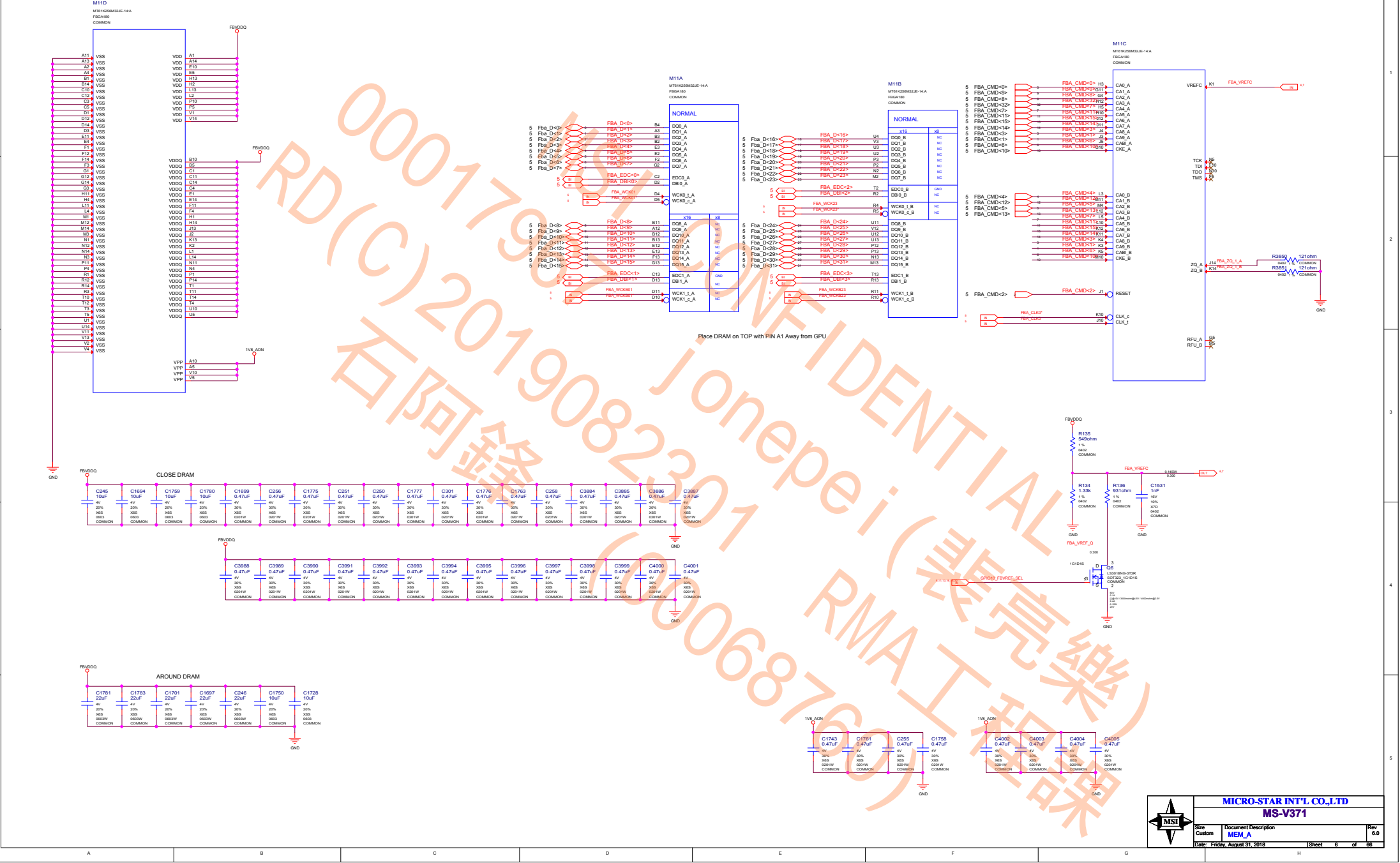
PCI TERM

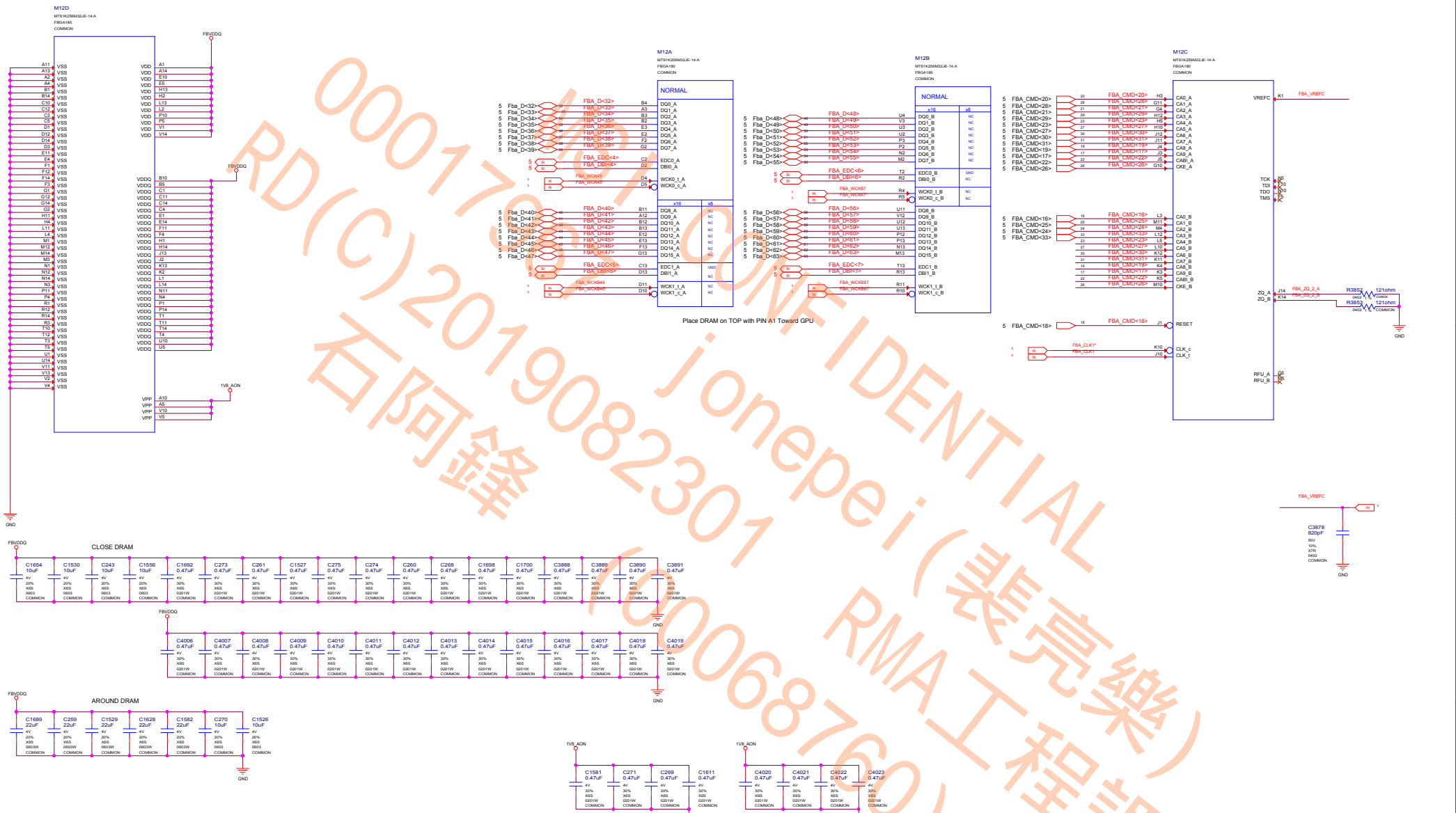


MEMORY: GPU Partition A/B

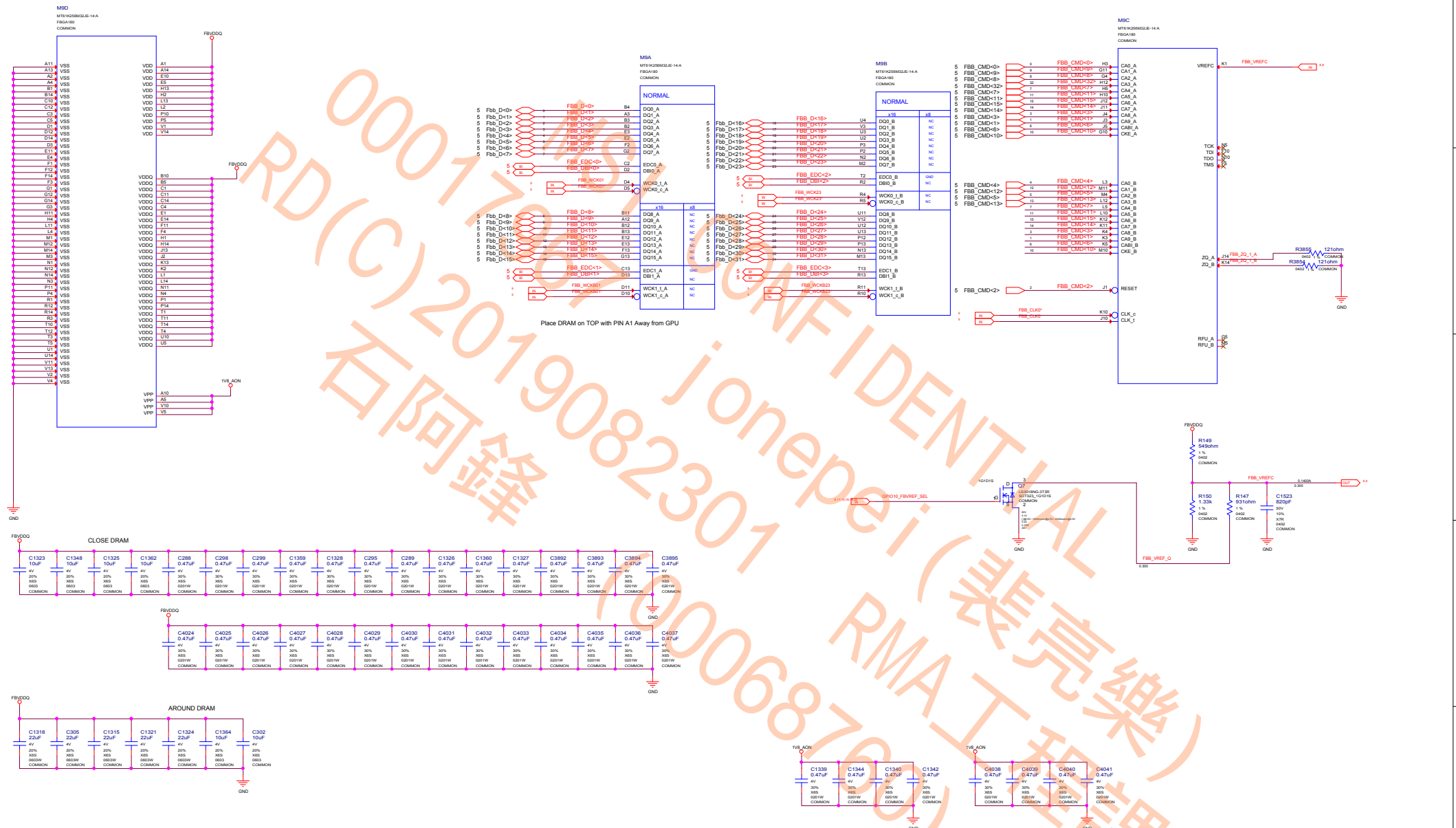


# MEMORY: FBA Partition 31..0

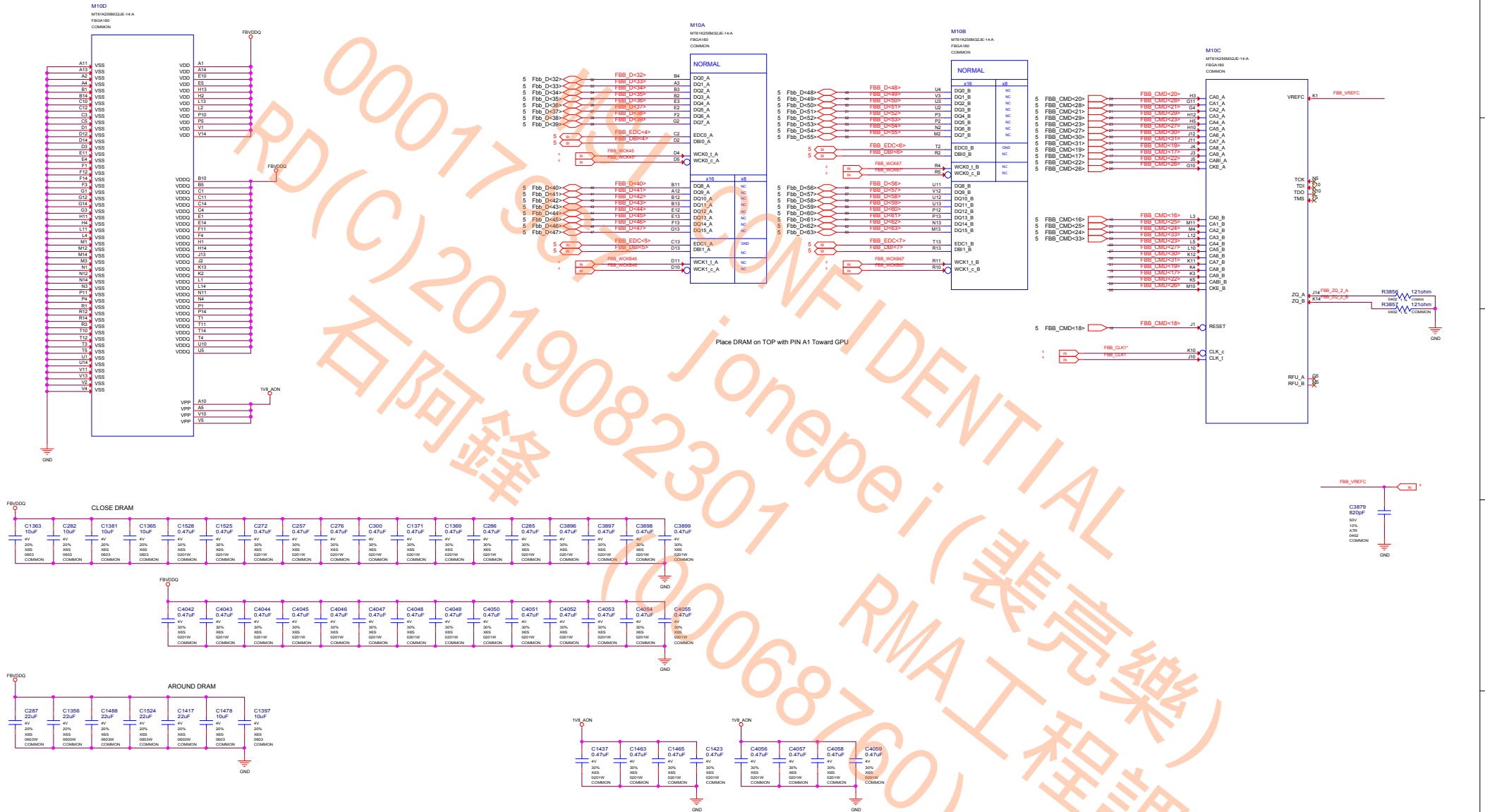


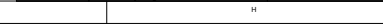




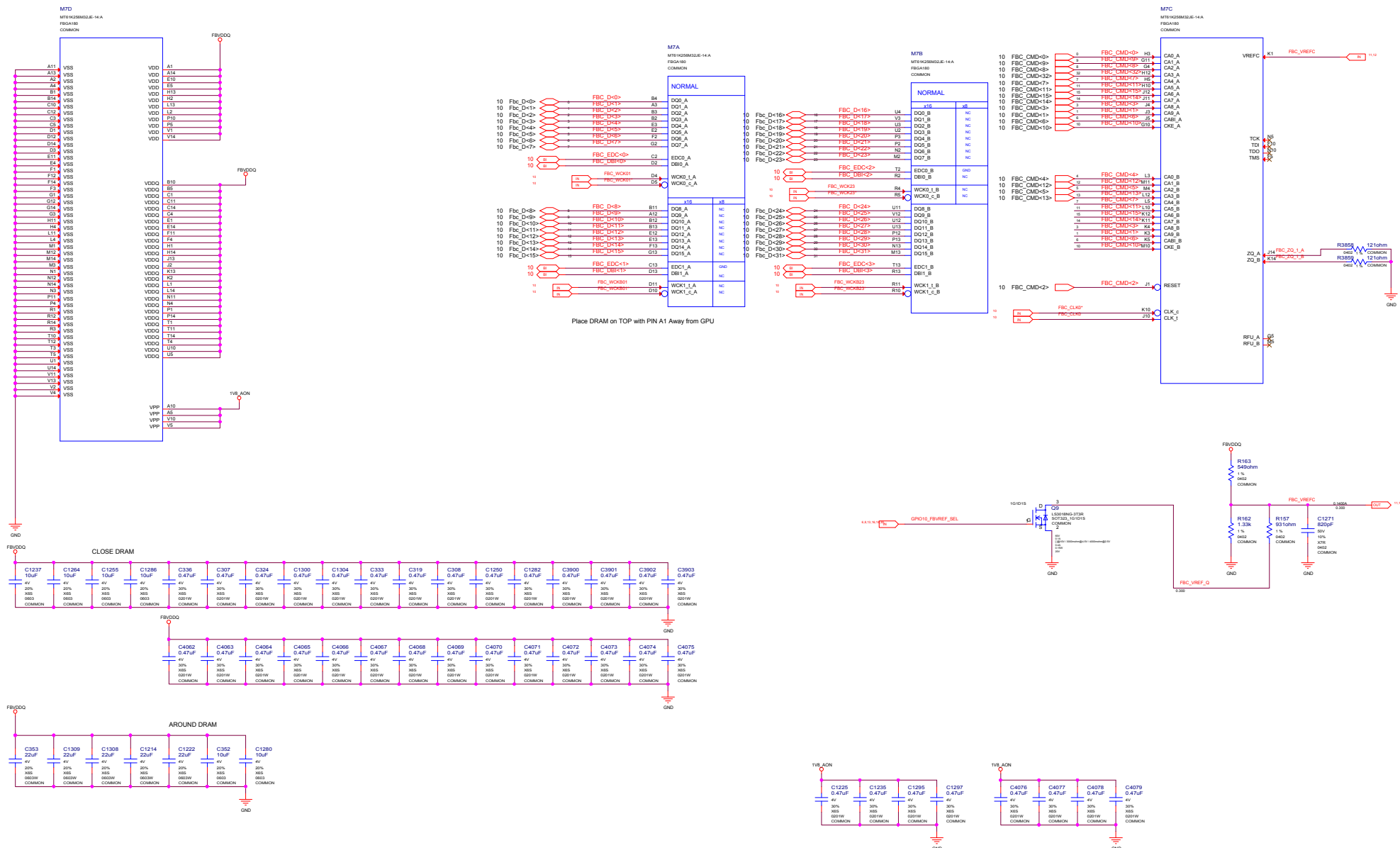






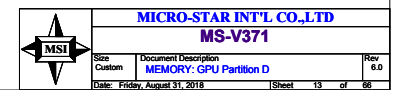
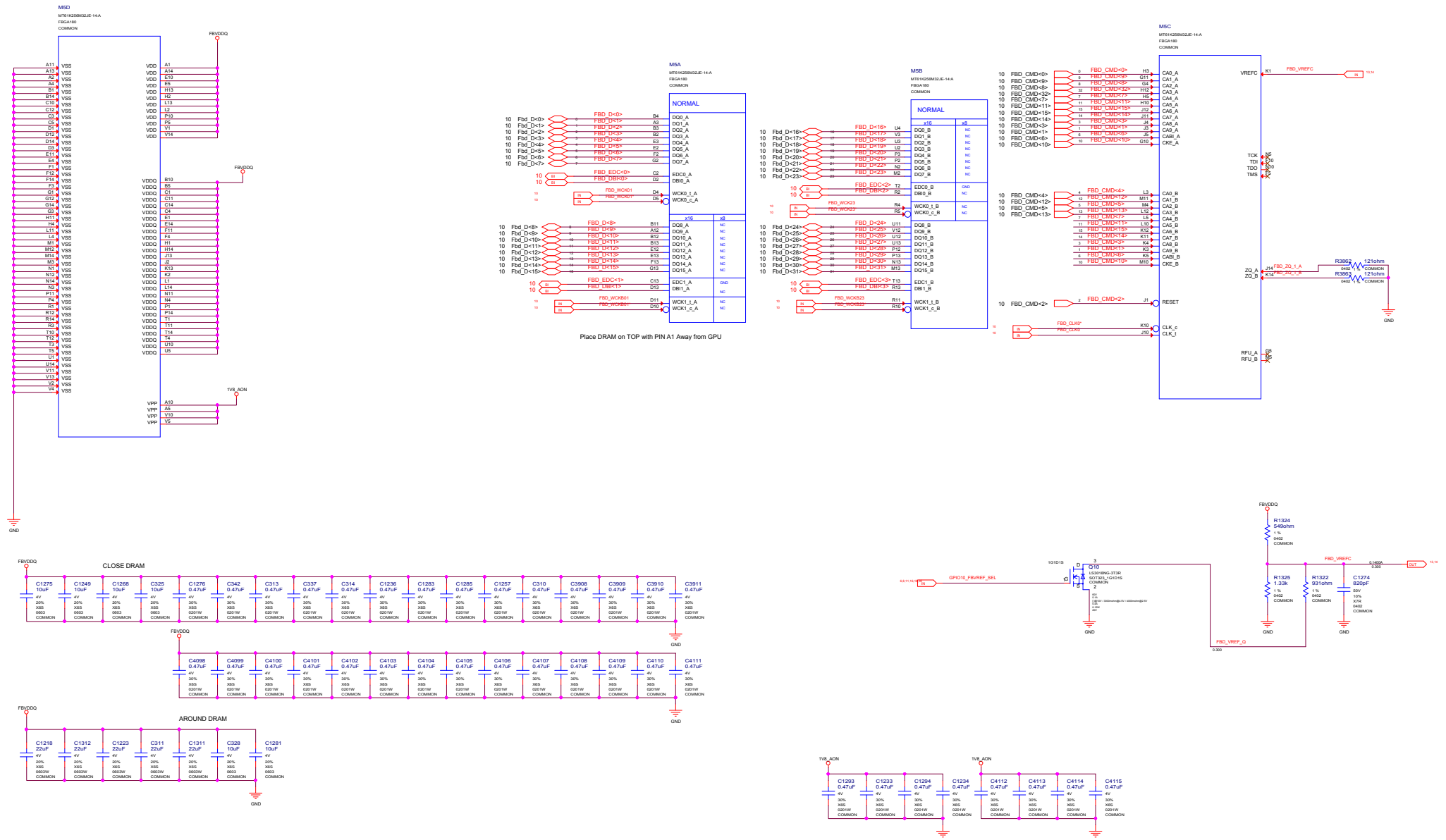


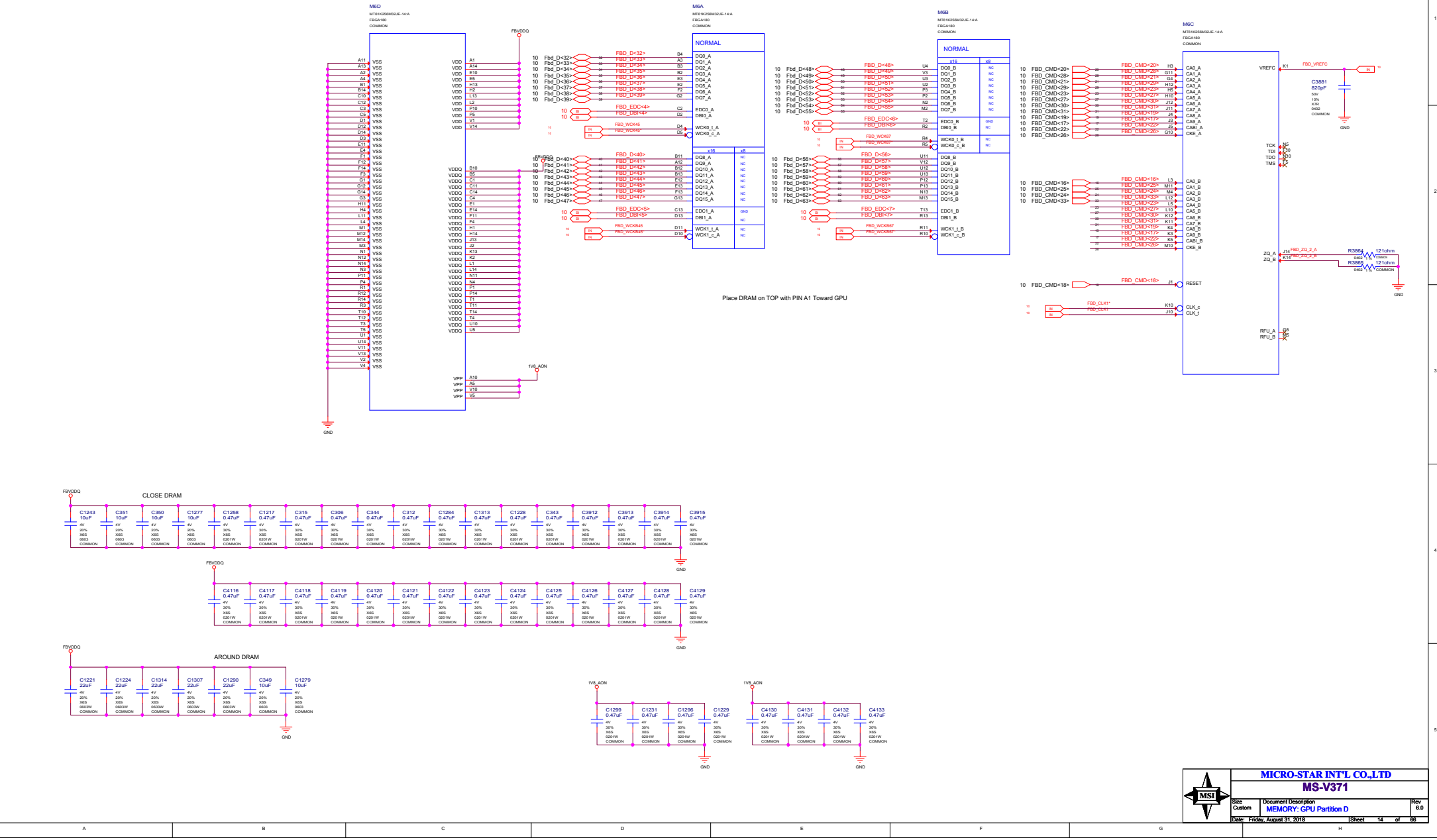
MEMORY: FBC Partition 31..0





MEMORY: FBD Partition 31..0

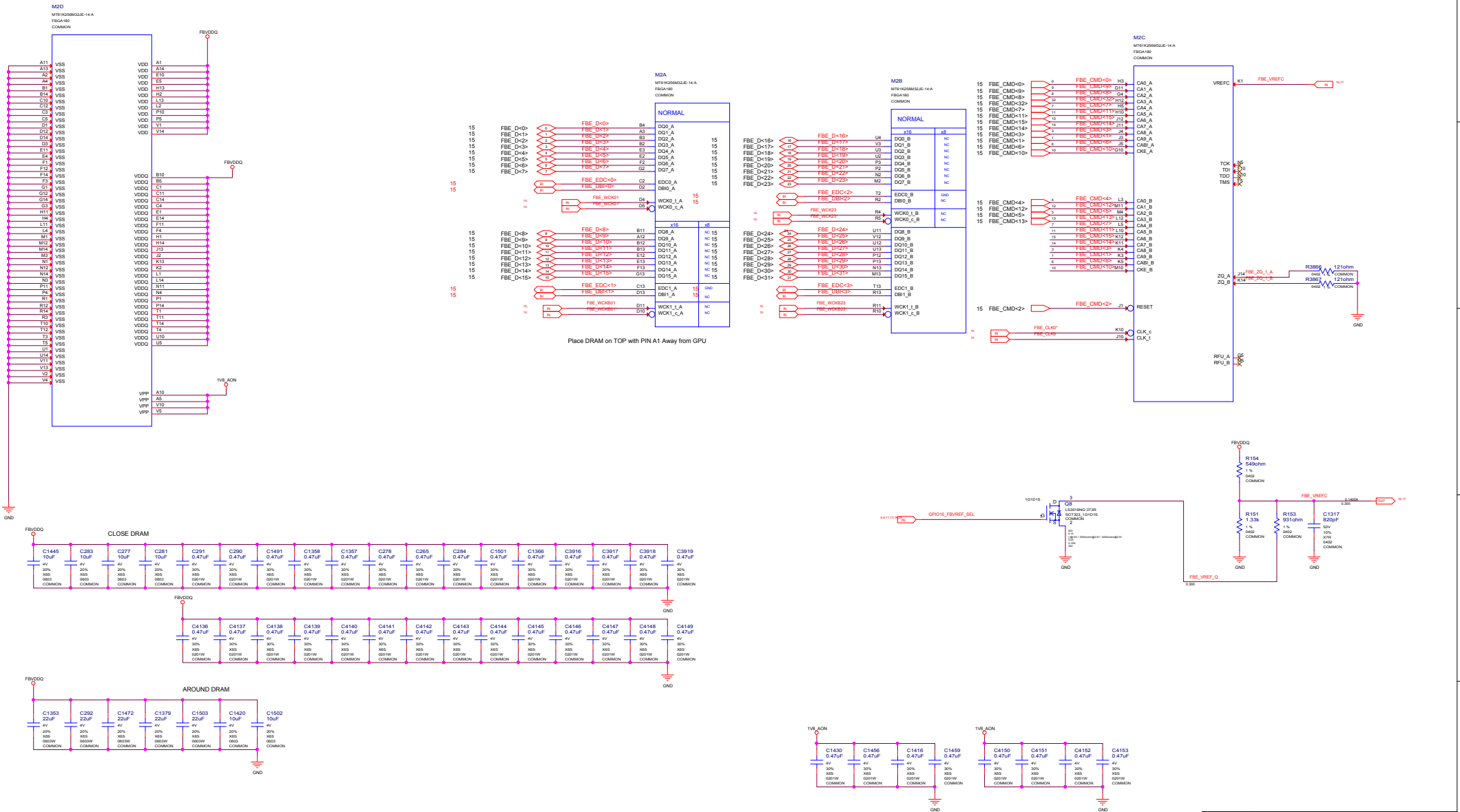






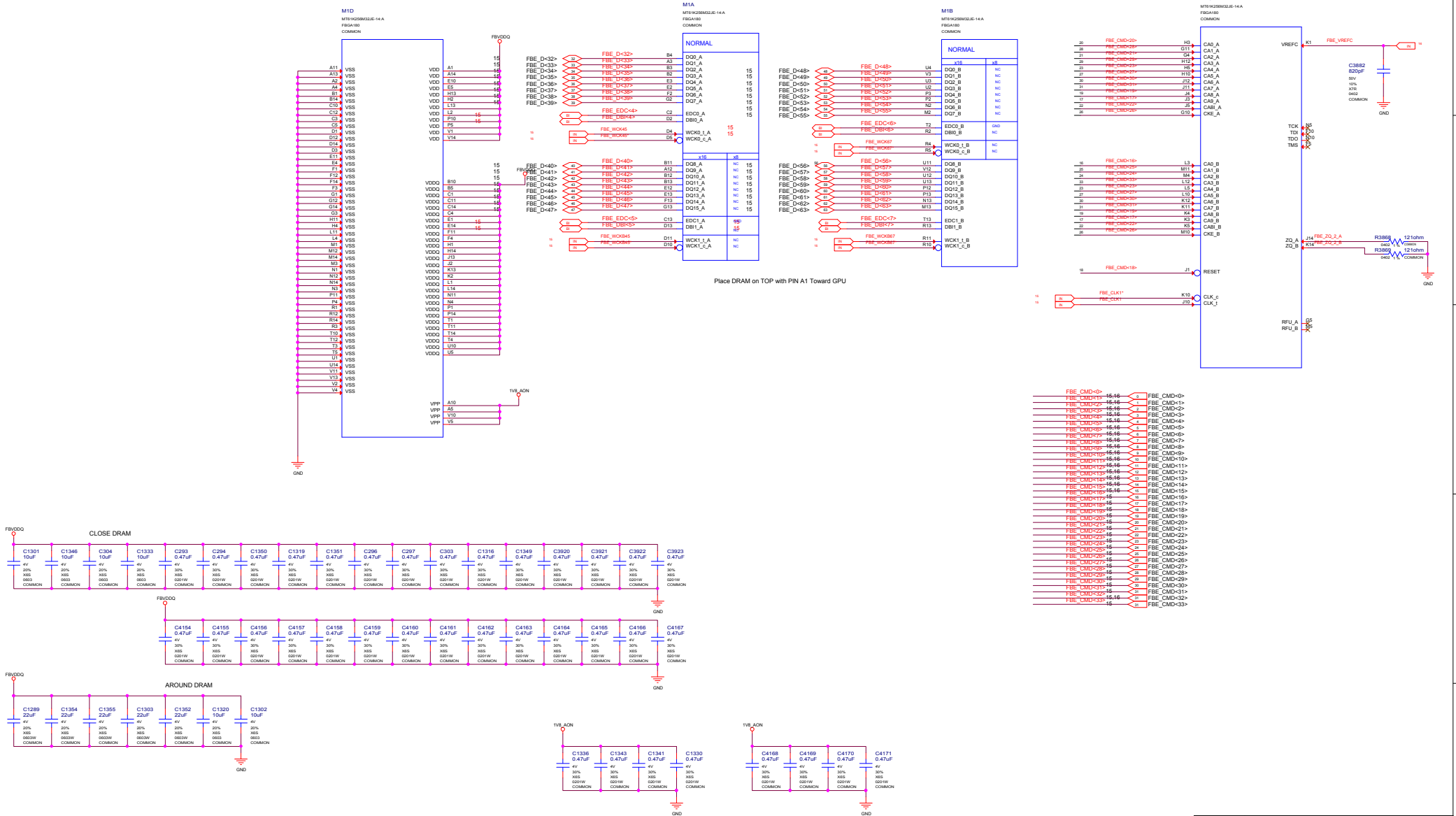


MEMORY: FBE Partition 31..0

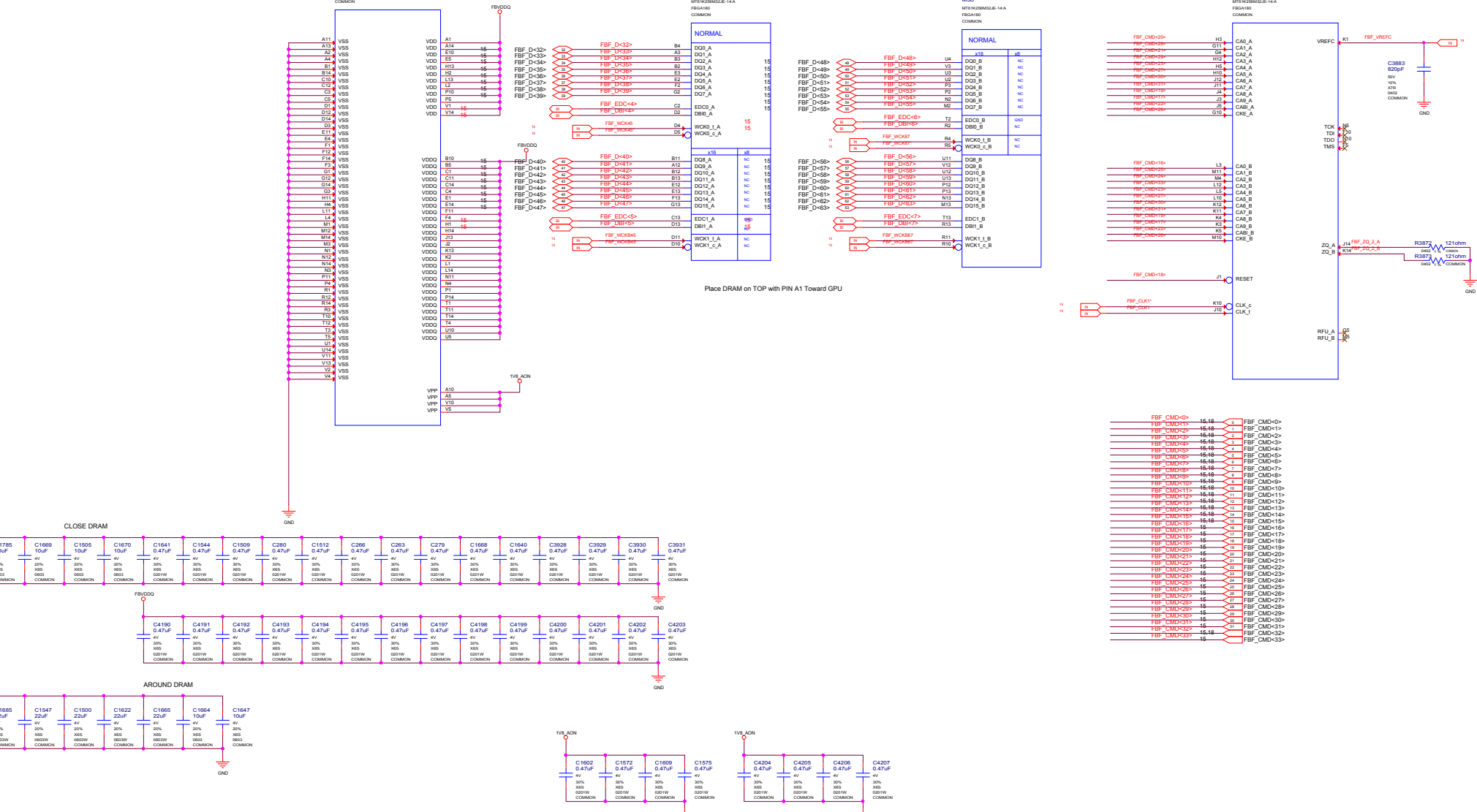


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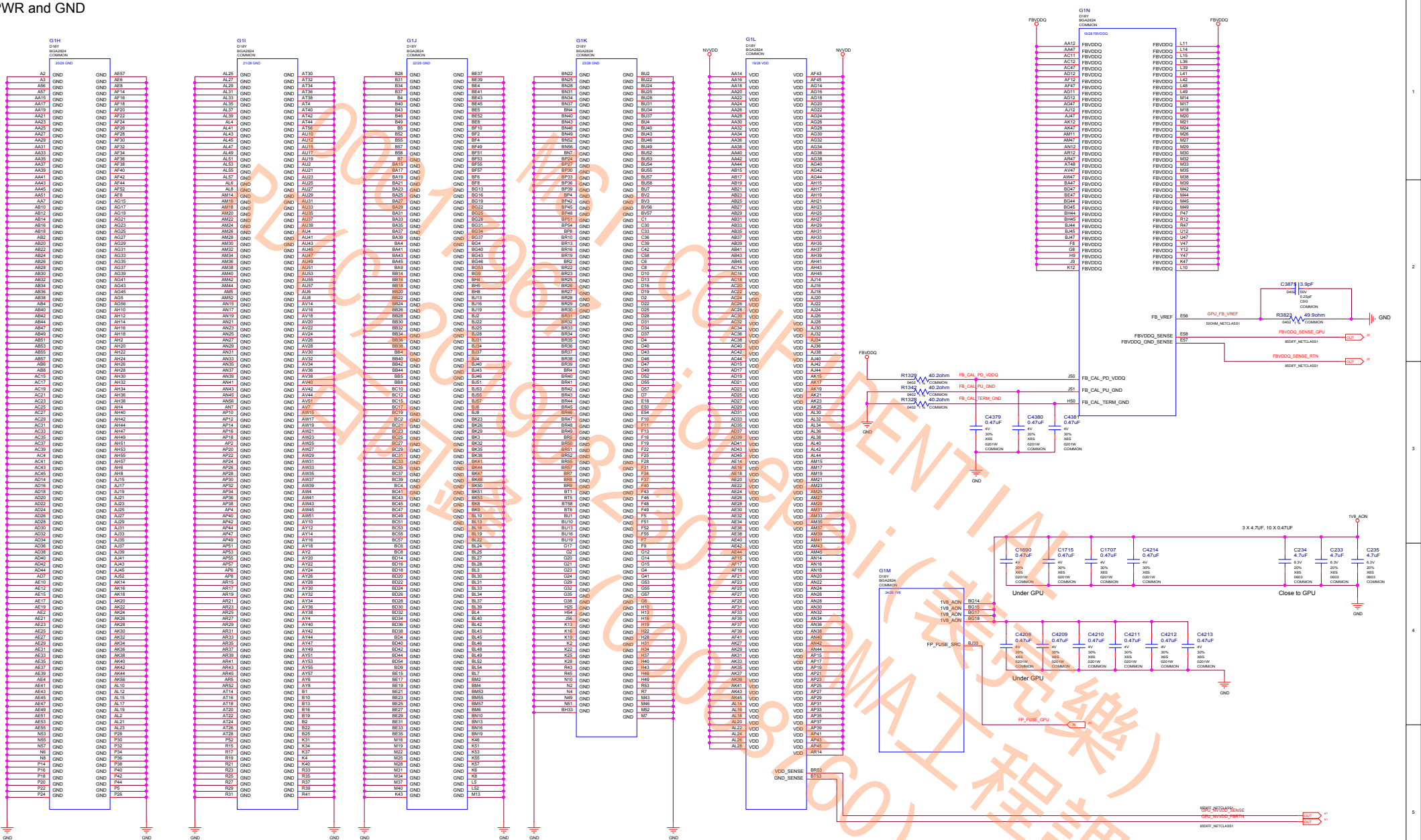
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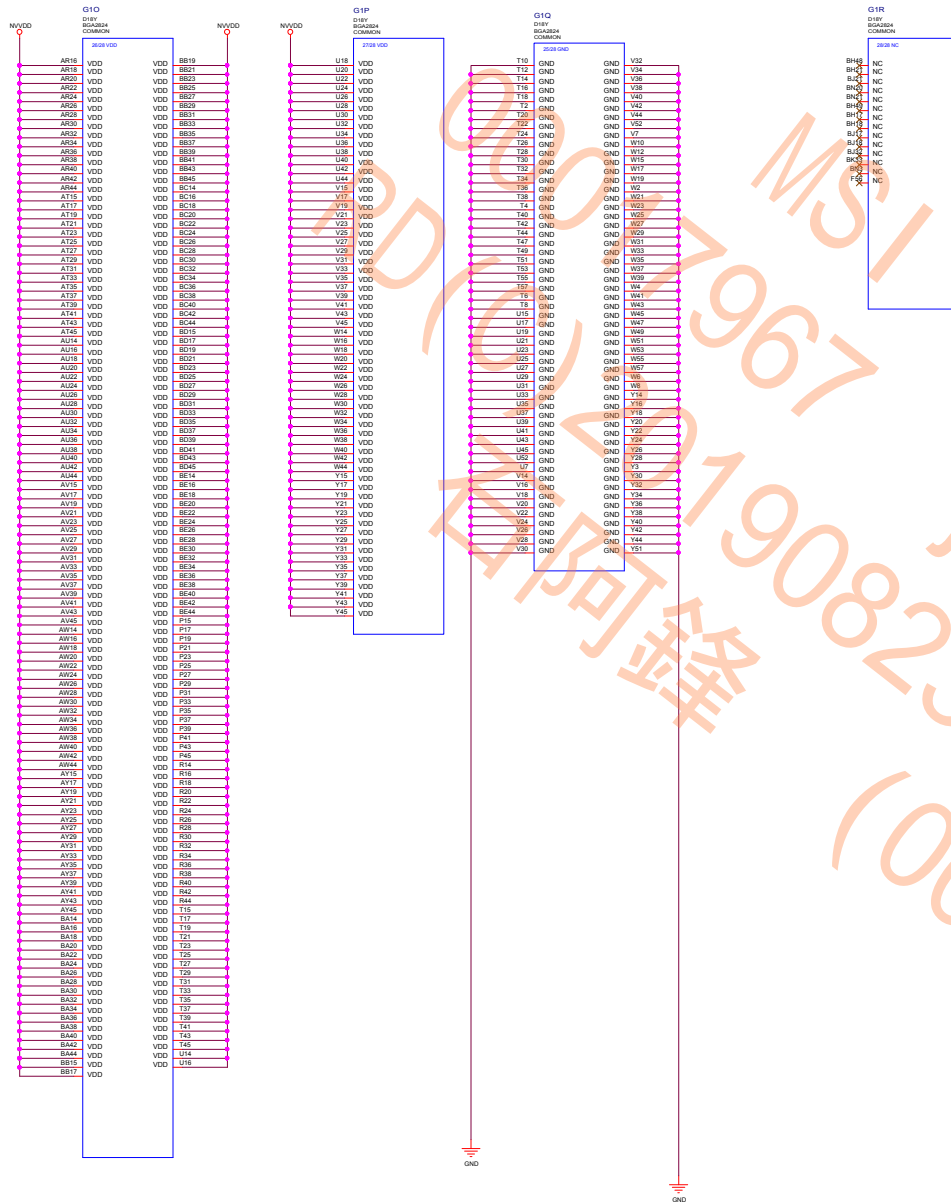
## GPU PWR and GND



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## GPU PWR GND NCs



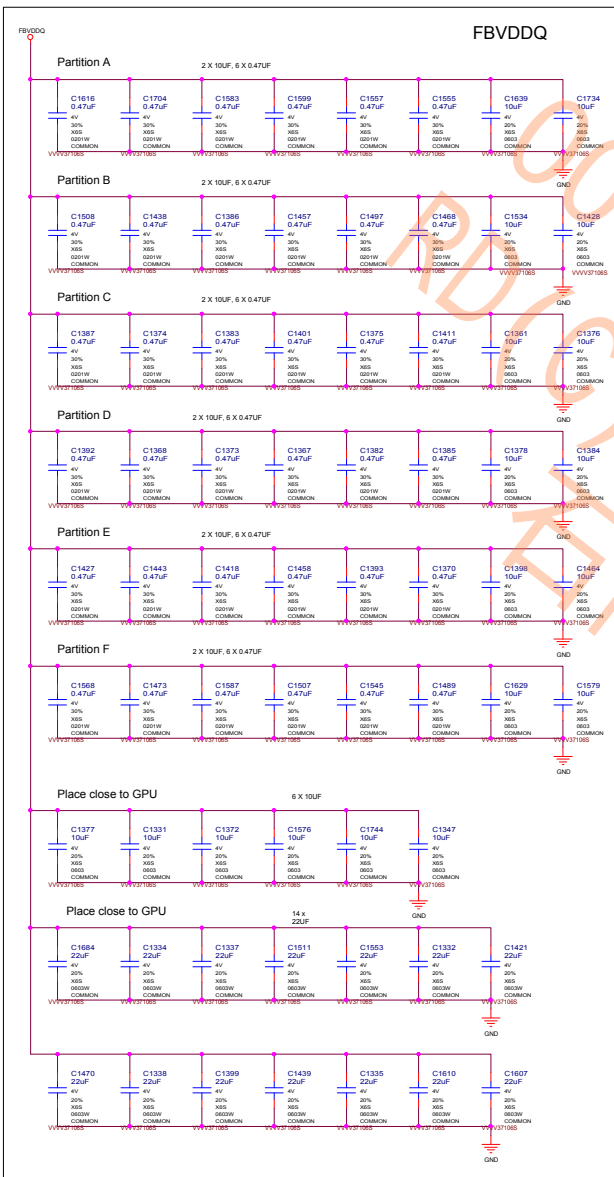
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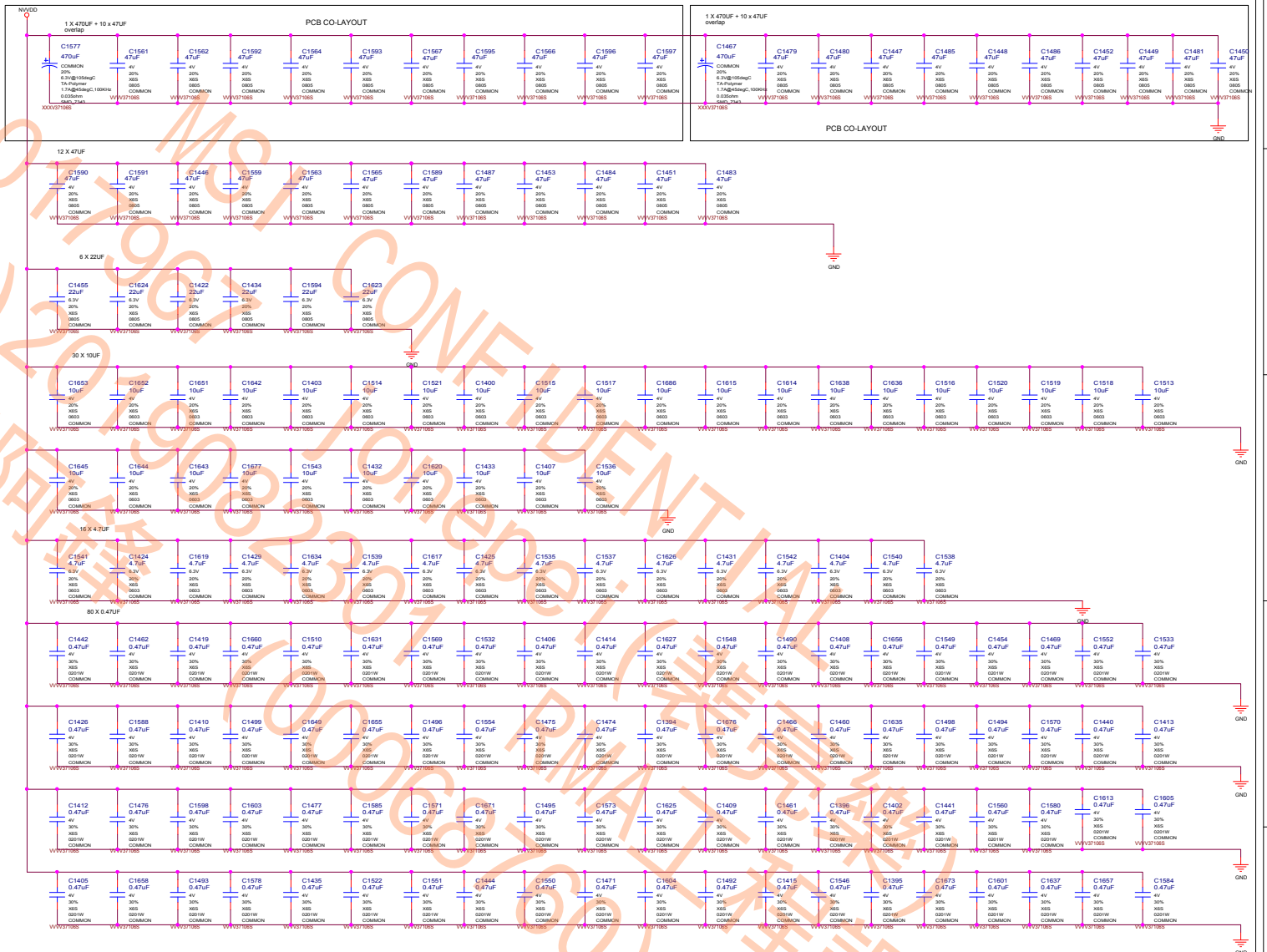
Size	Document Description	Rev
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Custom	GPU PWR GND	6.0
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## GPU Decoupling



## NVVDD

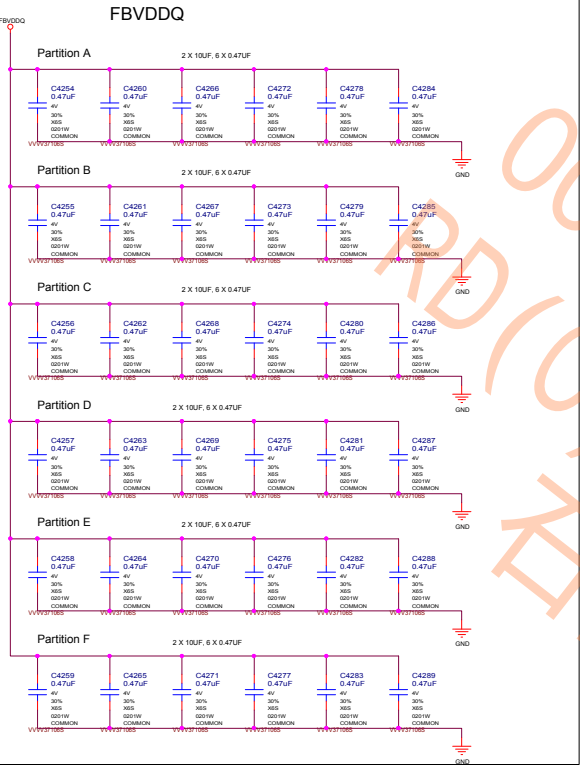


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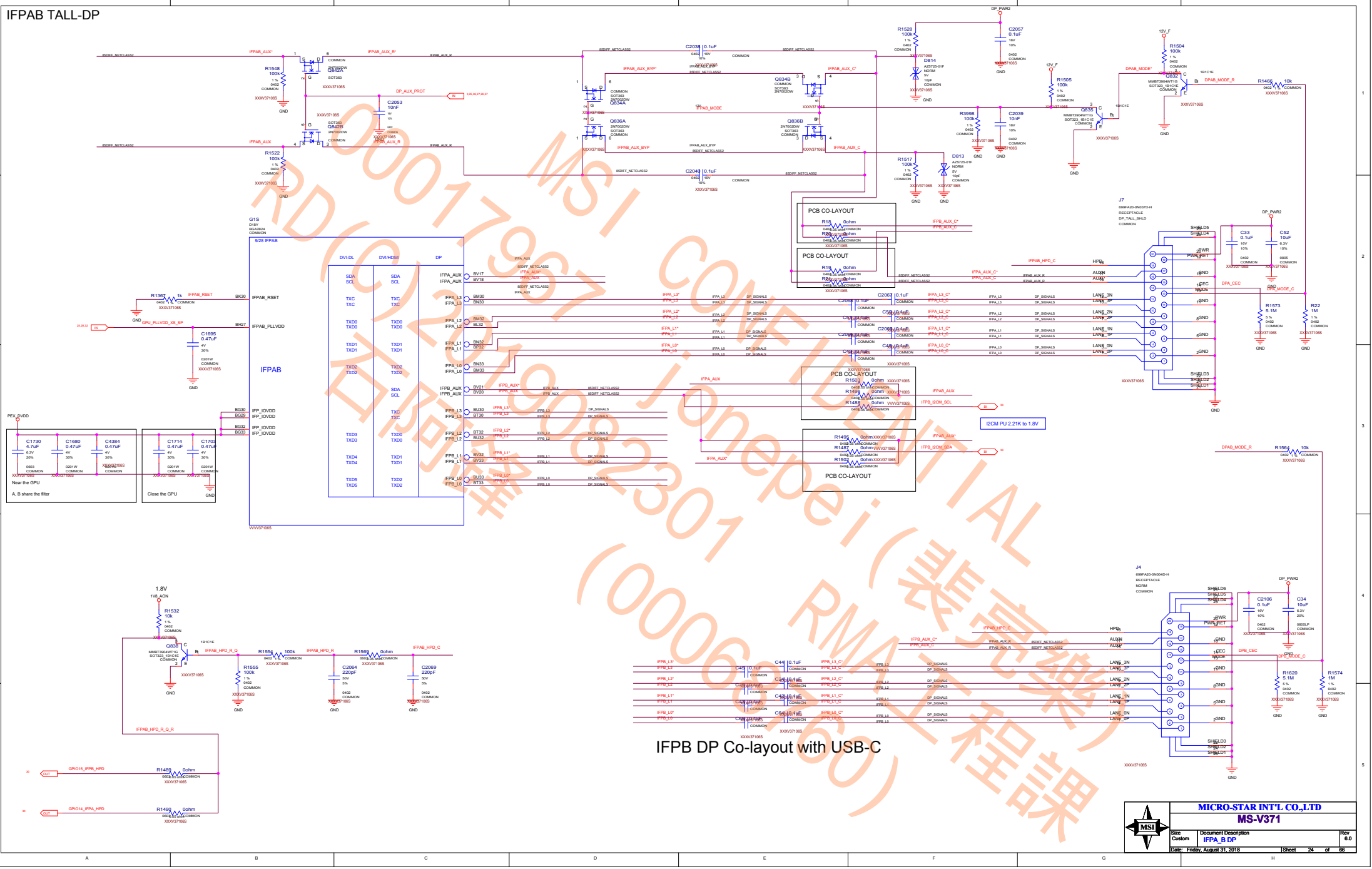
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GPU Decoupling



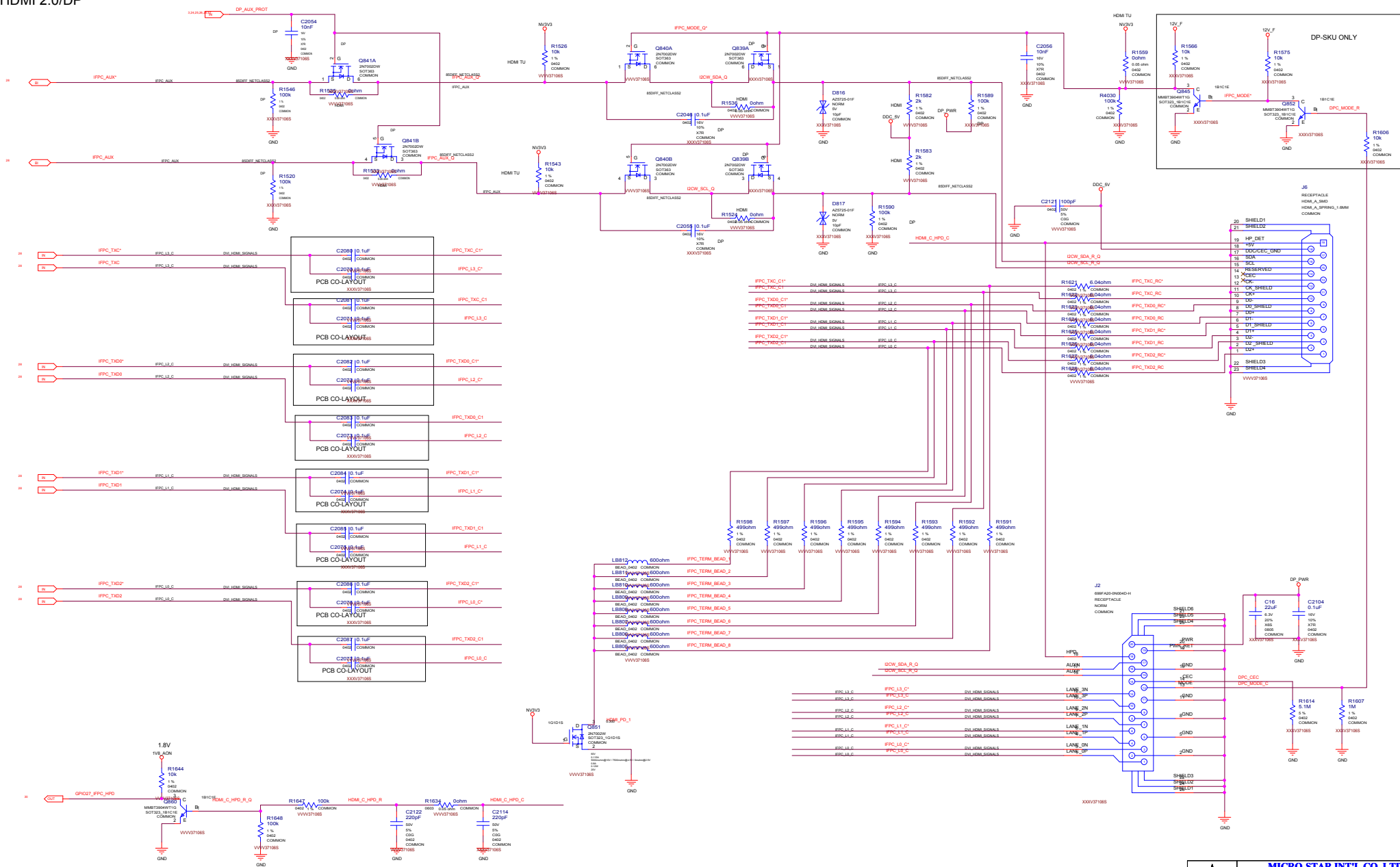
IFPAB TALL-DP





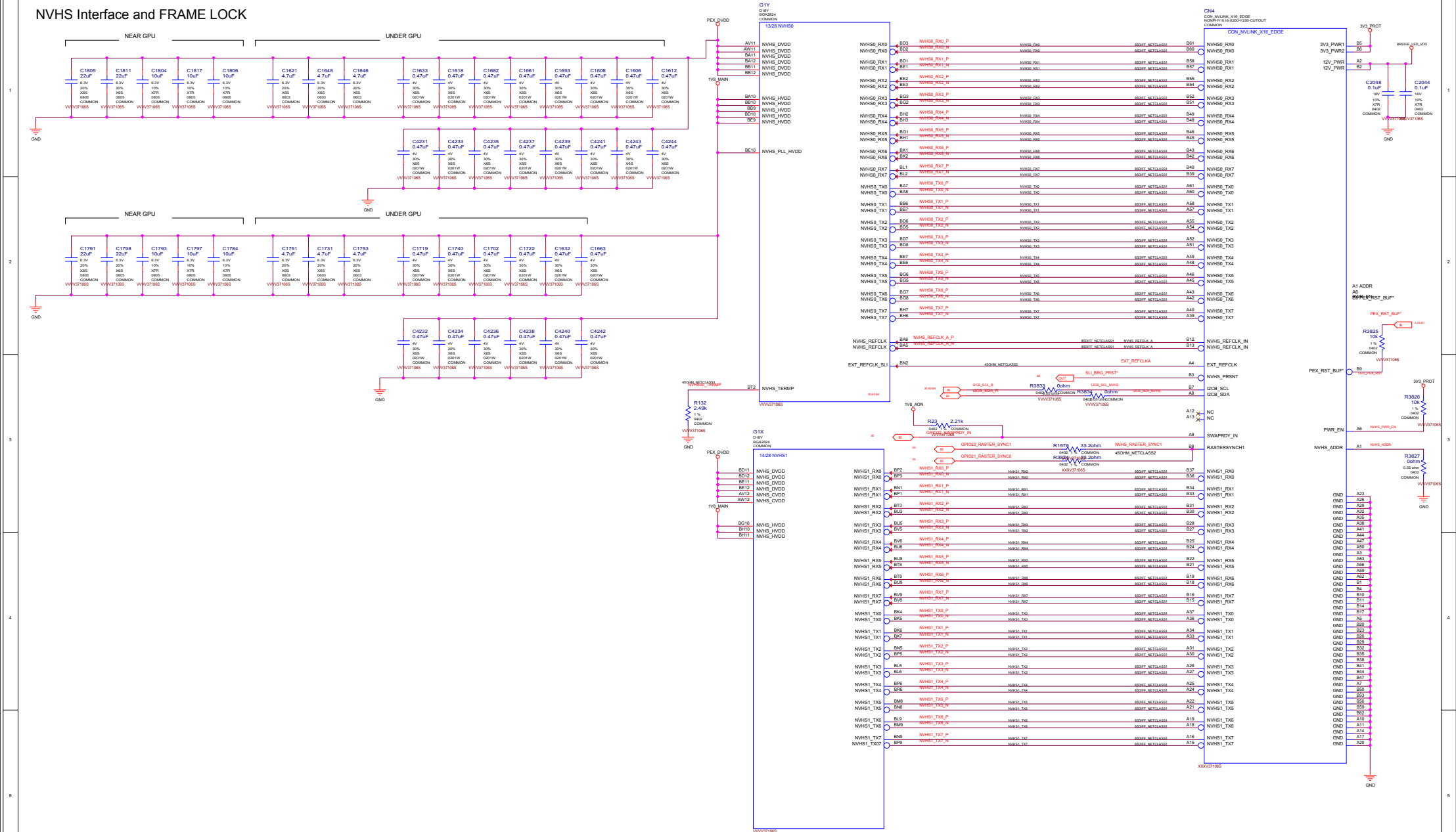


## IFPC HDMI 2.0/DP





## NVHS Interface and FRAME LOCK

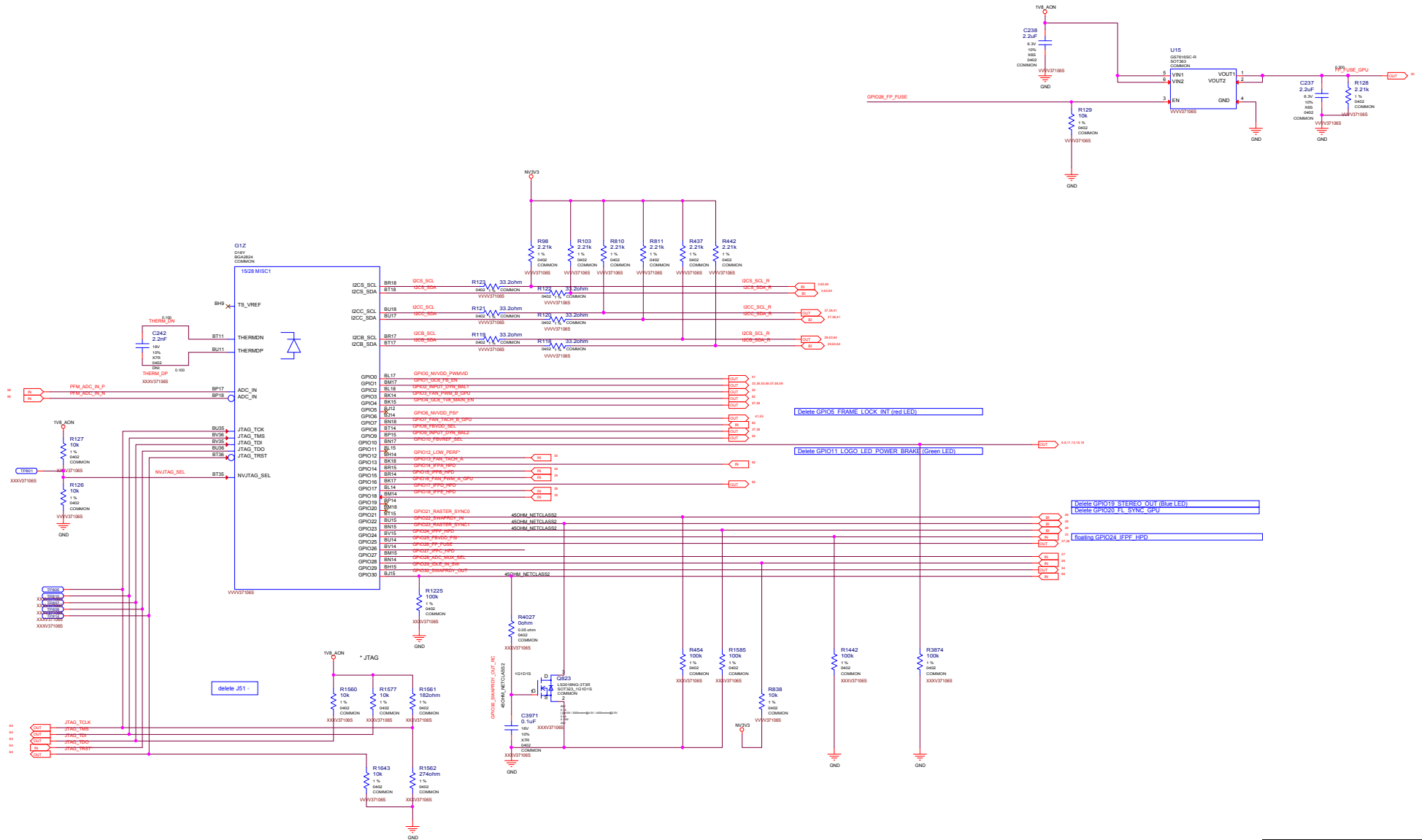


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## MISC1: Fan, Thermal, JTAG, GPIO, STEREO



MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
H	L	H	00101
H	H	L	00110
H	H	H	00111
L	L	M	01000
L	M	L	01001

DEFAULT

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

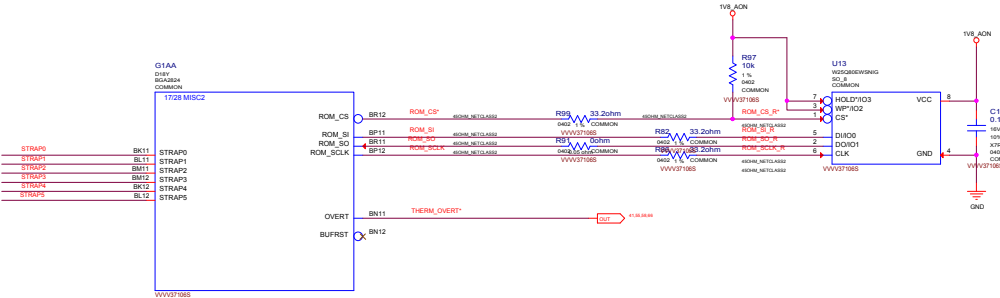
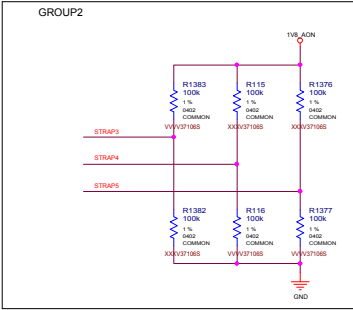
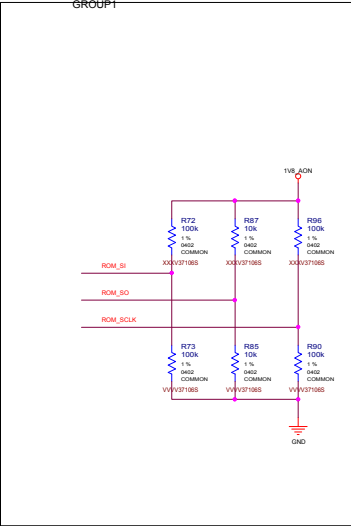
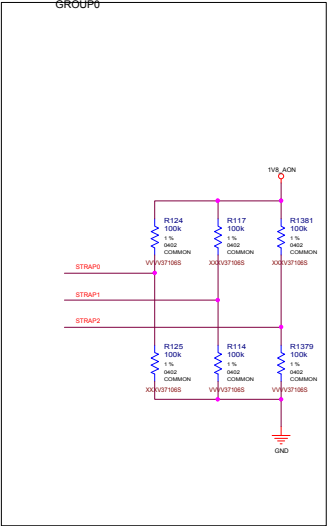
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0].FS_OVERT	1.ENABLE 0.DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	H	XXX0	FS_OVERT DISABLE

DEFAULT

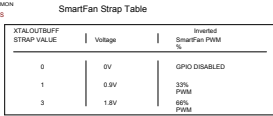
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

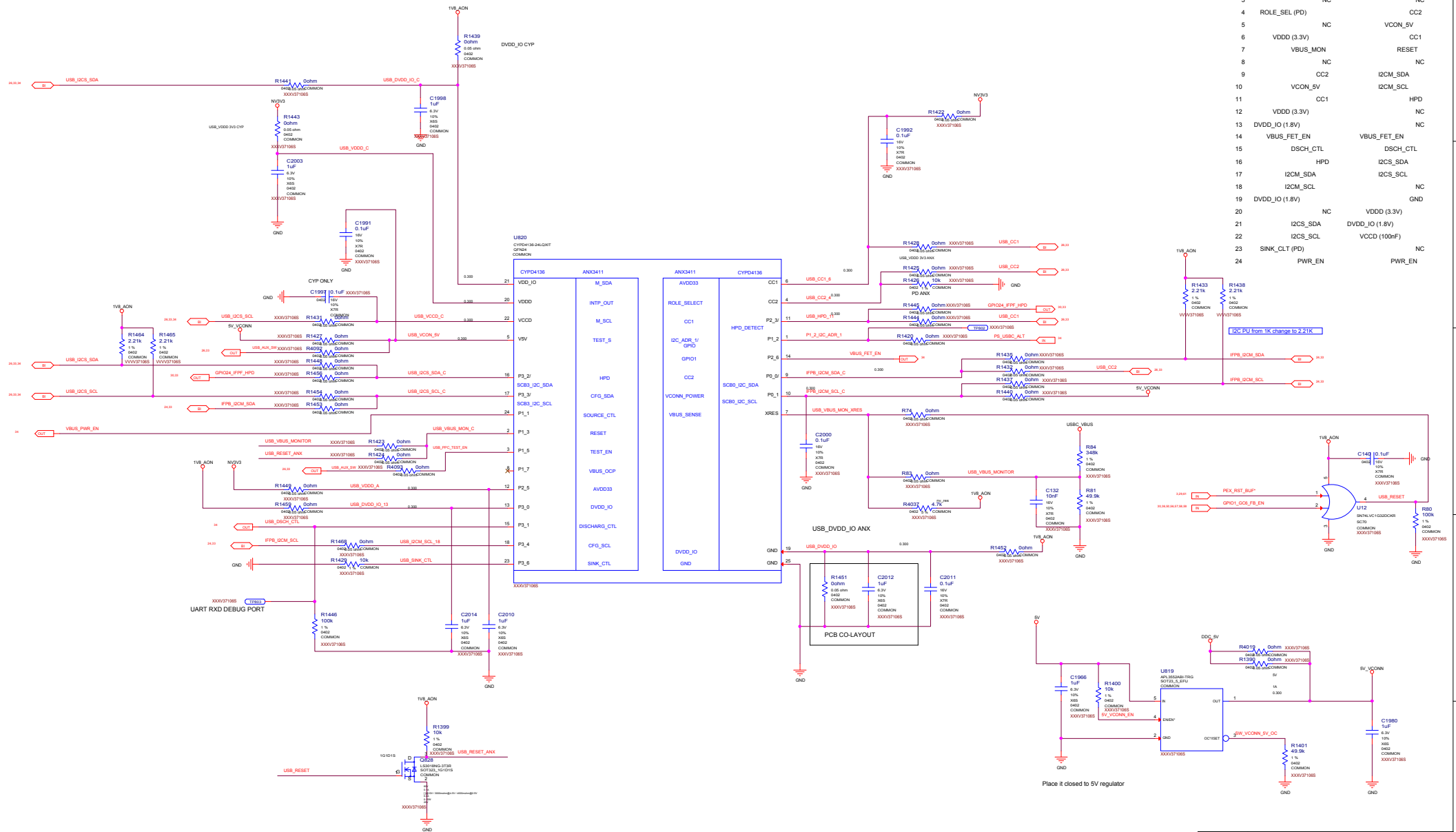
SKU 200



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## MISC: USB PPC

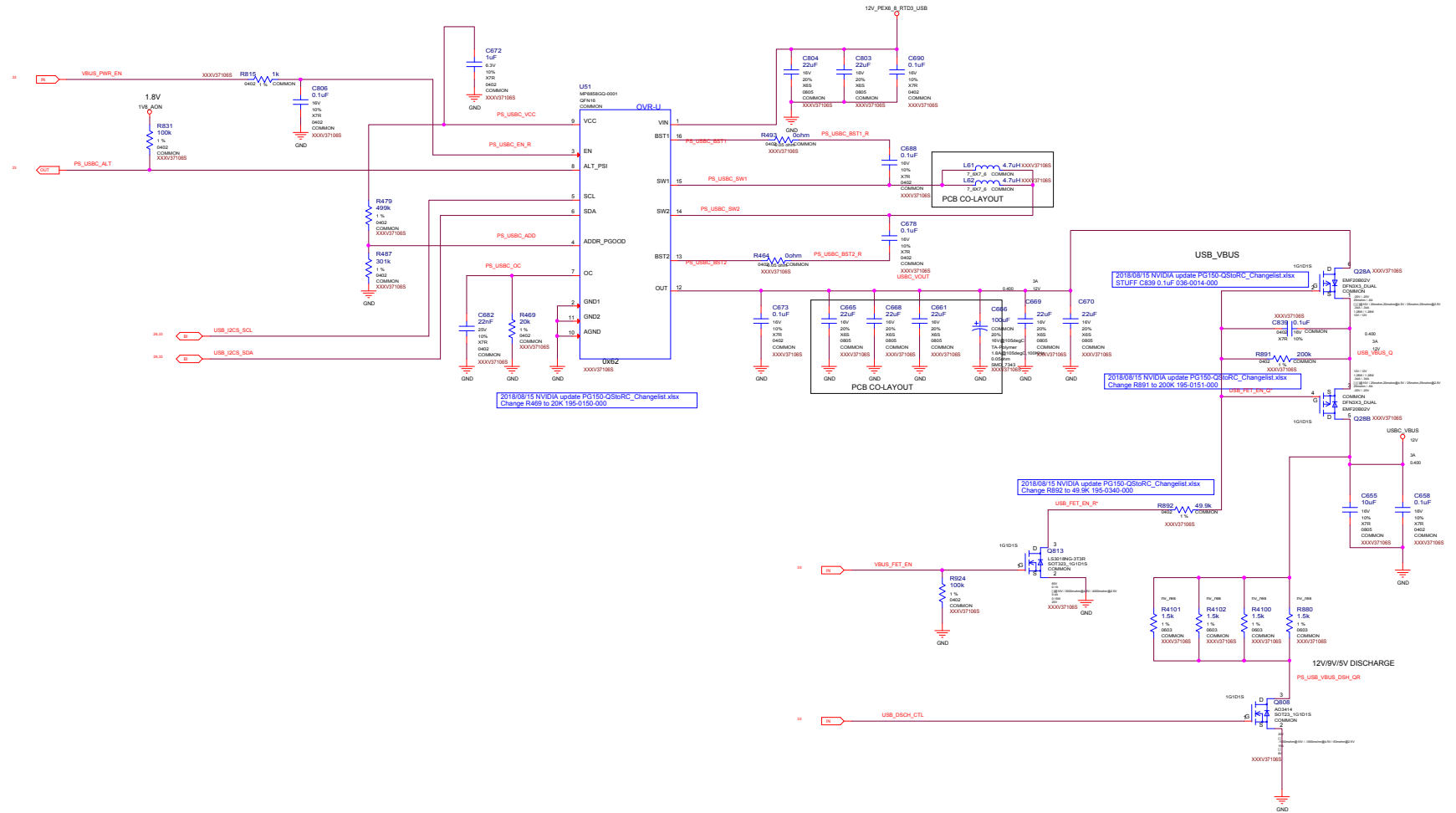


PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_SV
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_SV	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100mF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN



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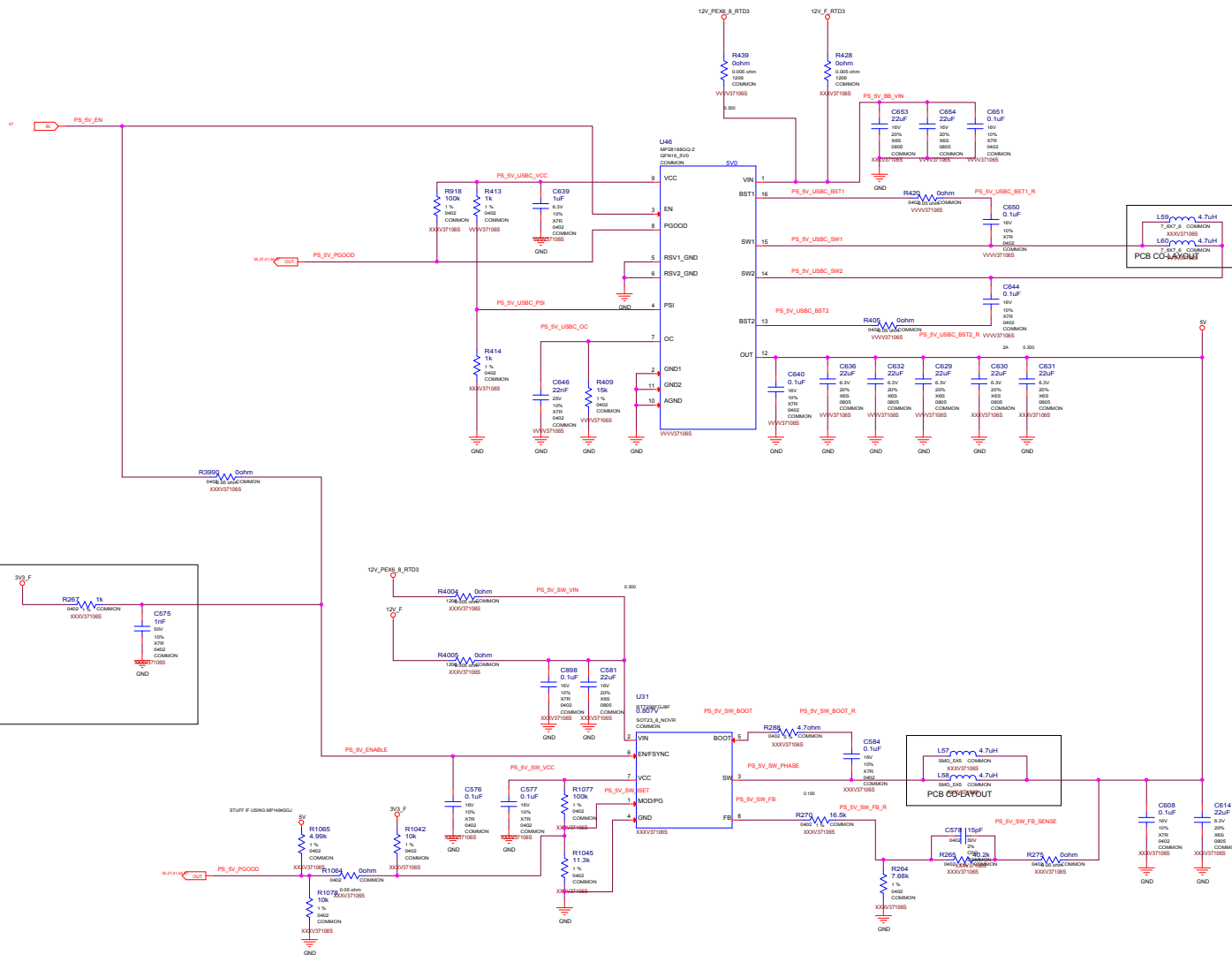
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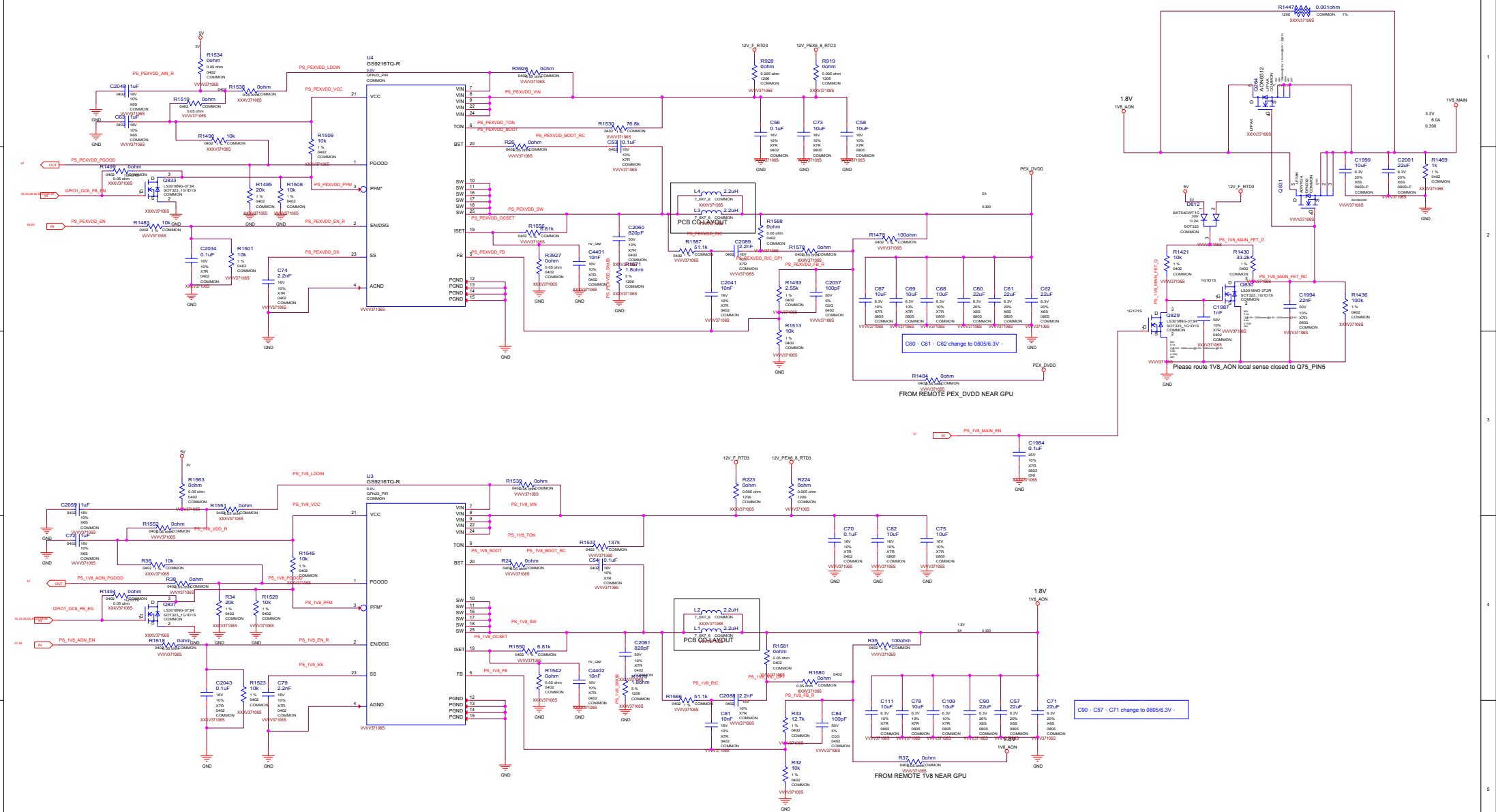
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Size Custom	Document Description <b>USB VR</b>	Rev 6.0
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PS: 5V, 5V\_BACKUP



PS: PEXVDD 1V8 Rail

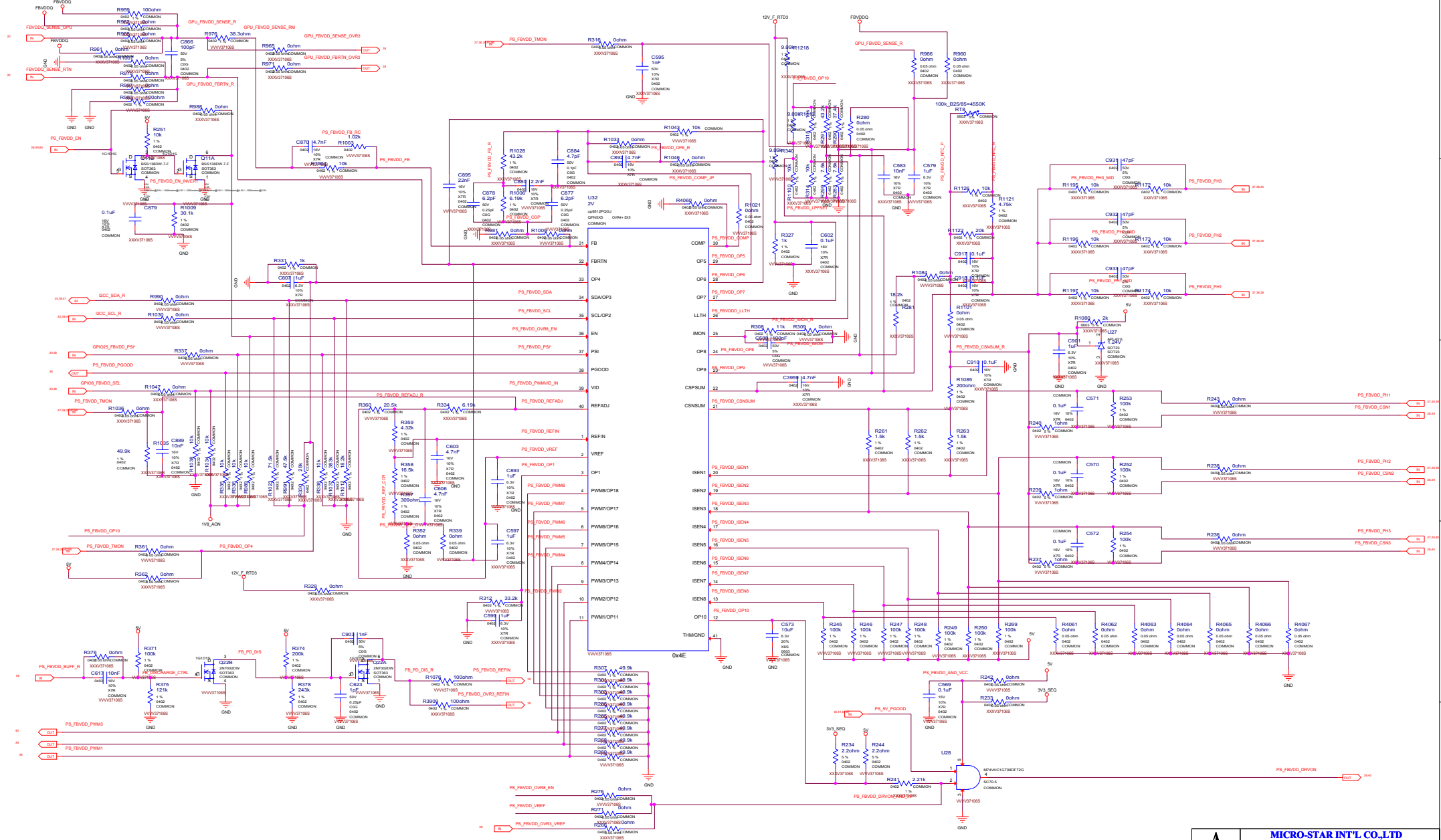


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Size Custom	Document Description 1V8	Rev 6.0
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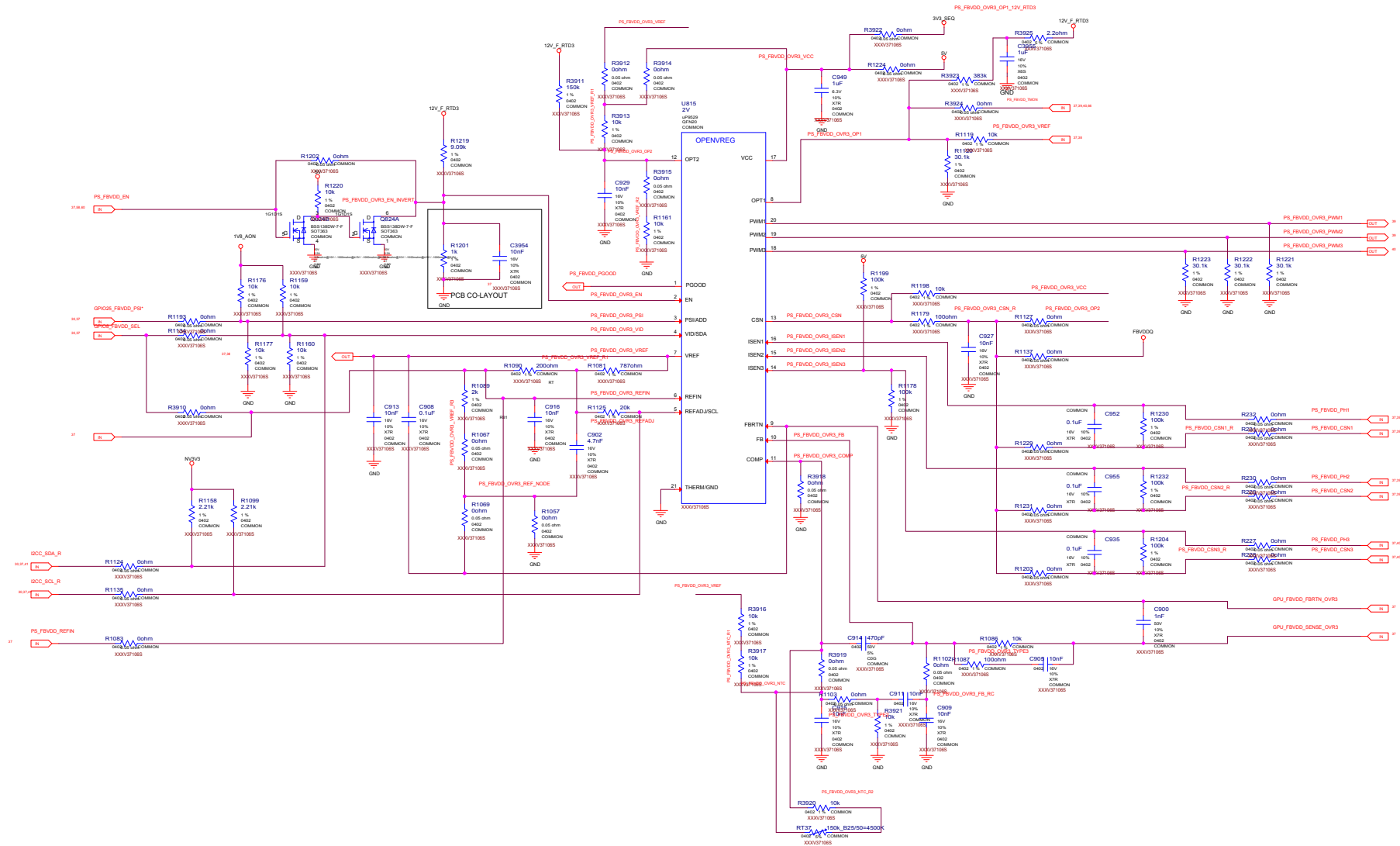
## PS: FBVDD Controller



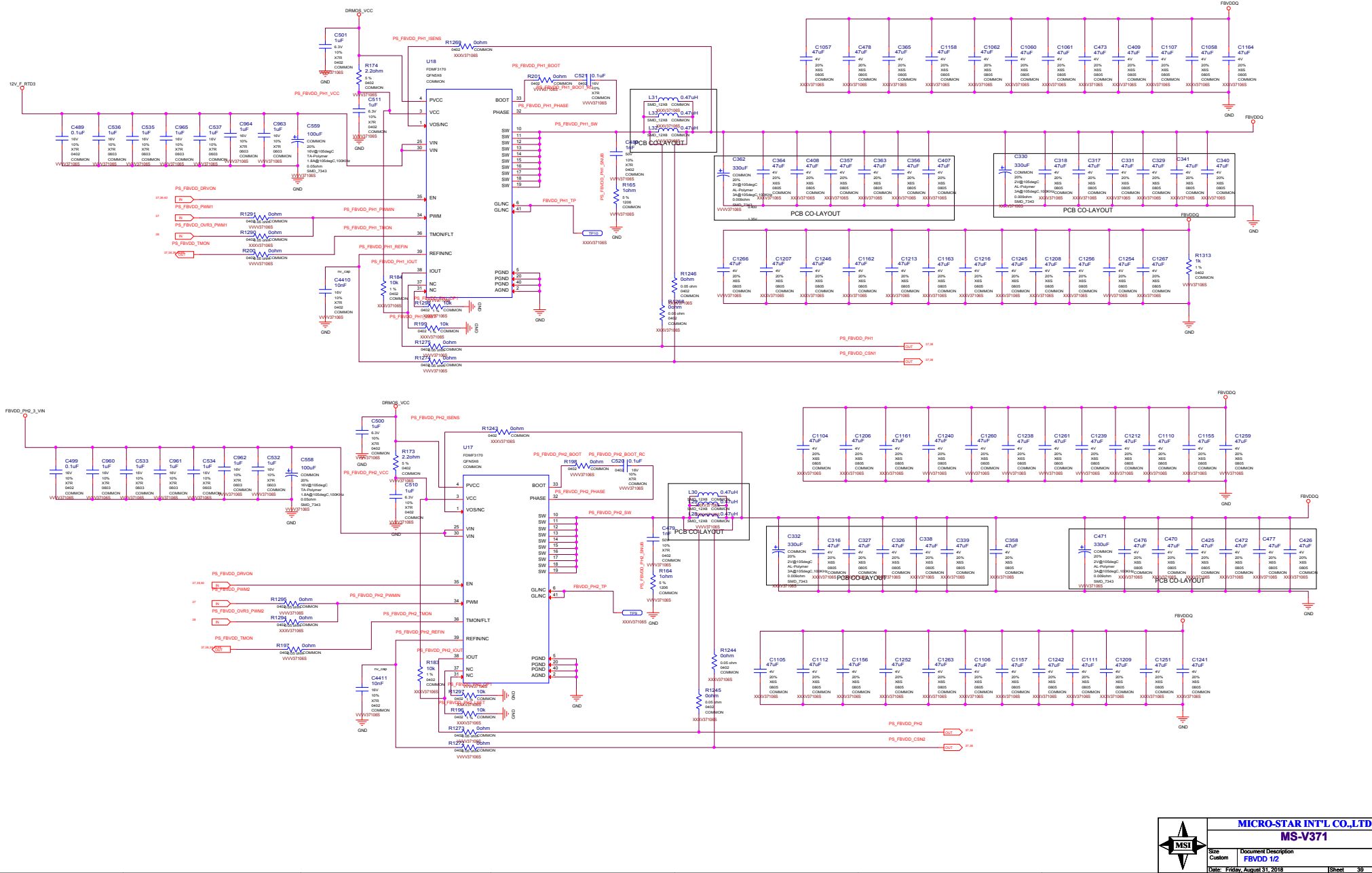
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Size Custom	Document Description <b>FBVDD</b>	Rev 6.0
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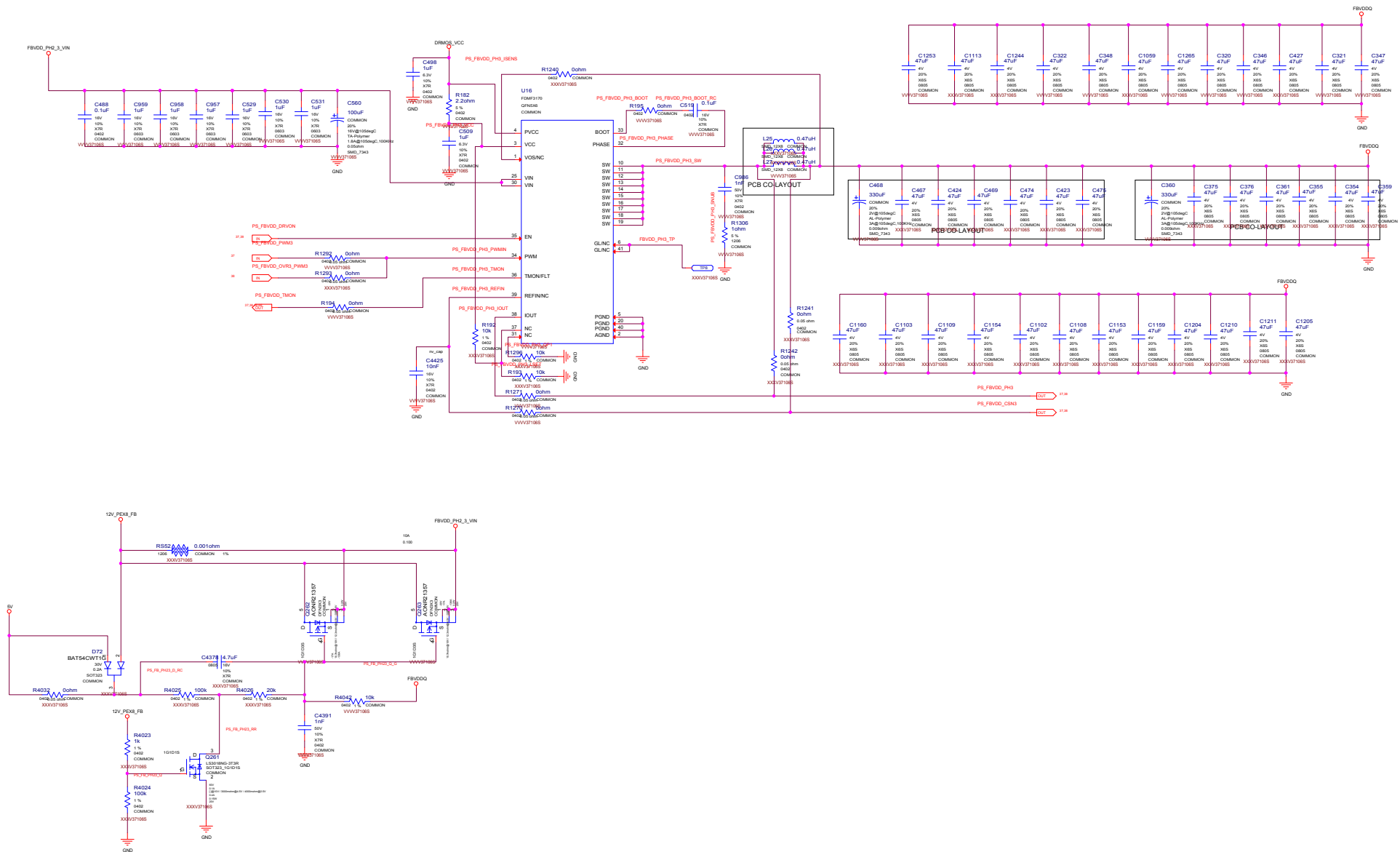
## PS: FBVDD Controller OVR3



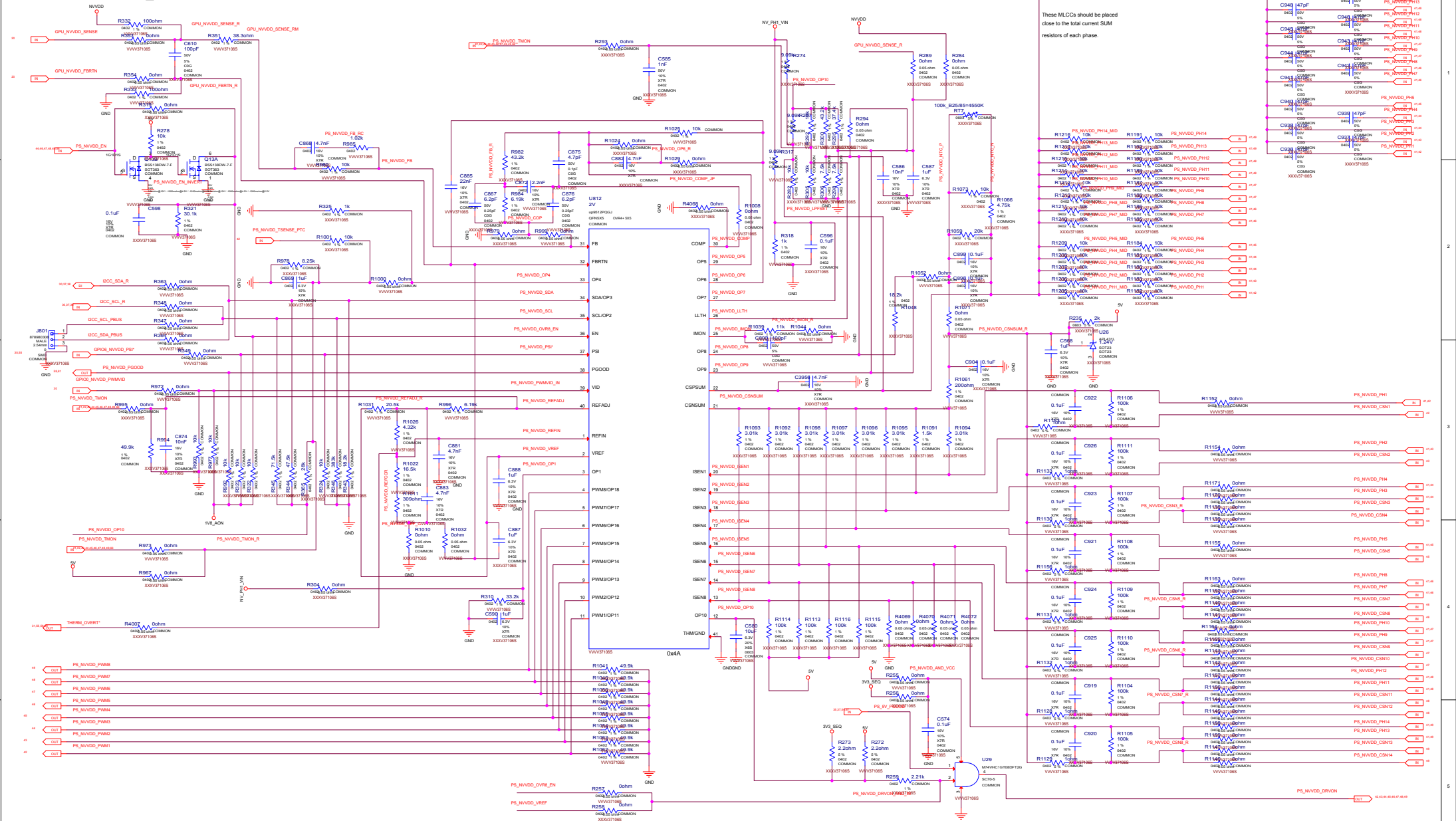
PS: FBVDD PH1, 2



## PS: FBVDD PH3



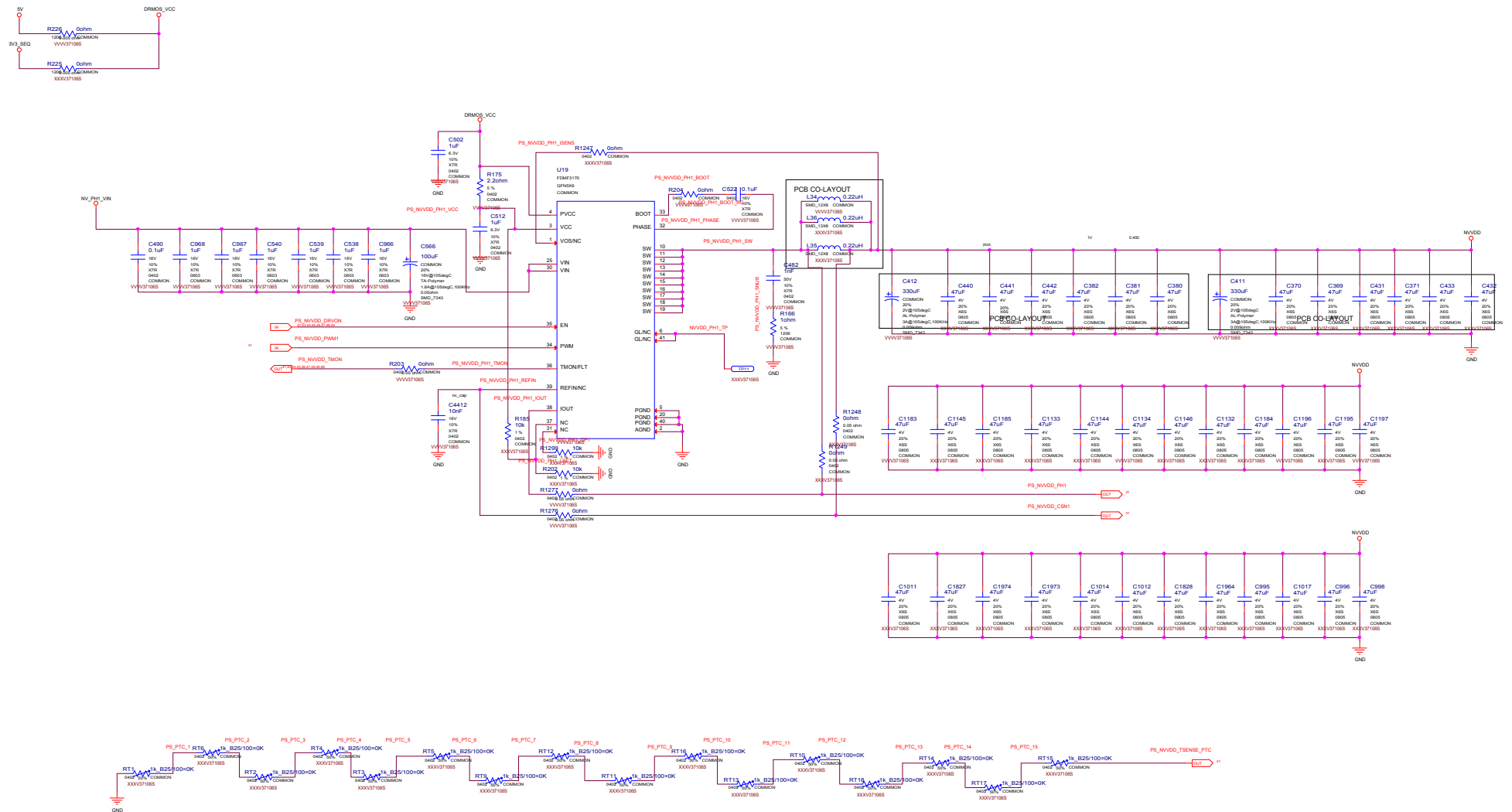
## PS: NVVDD Controller\_OVR8



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**MS-V371**

Size Custom	Document Description NVDD OVR8	Rev 6.0
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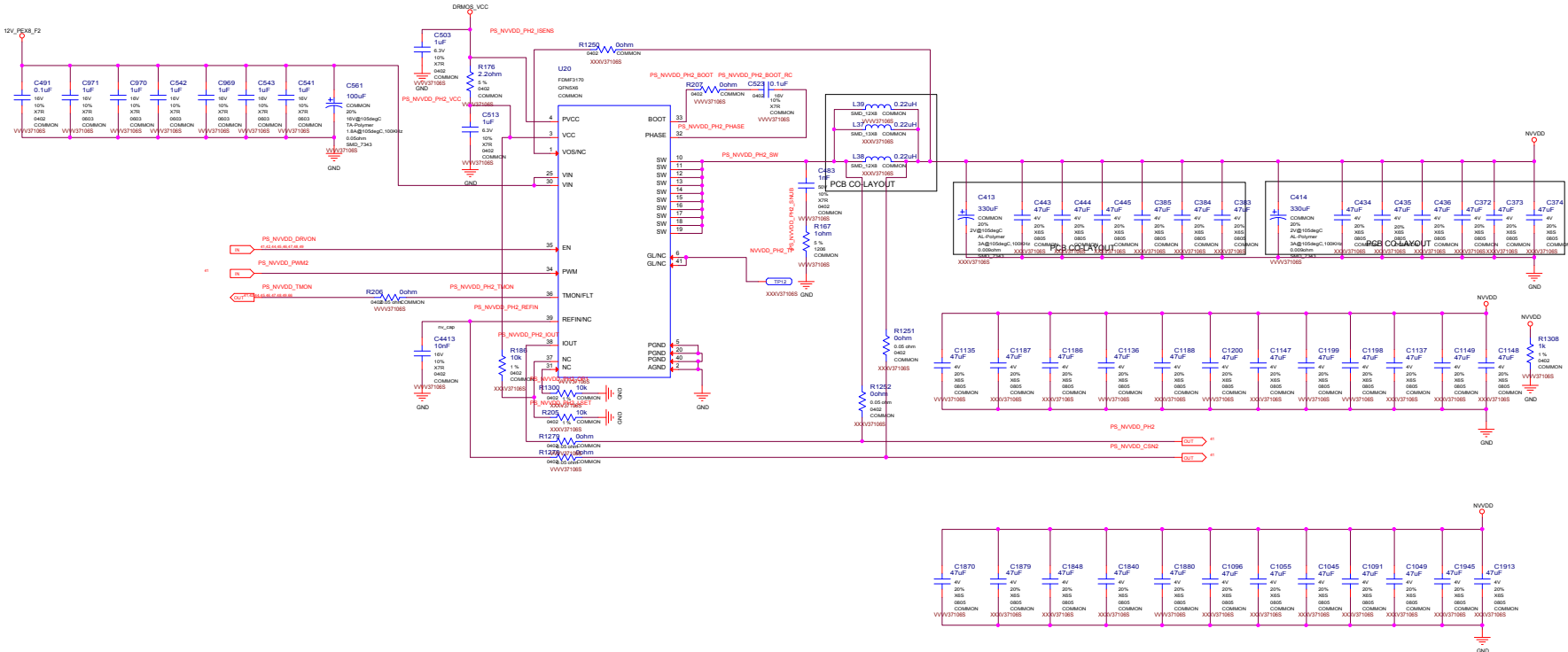
## PS: NVVDD Phase 1

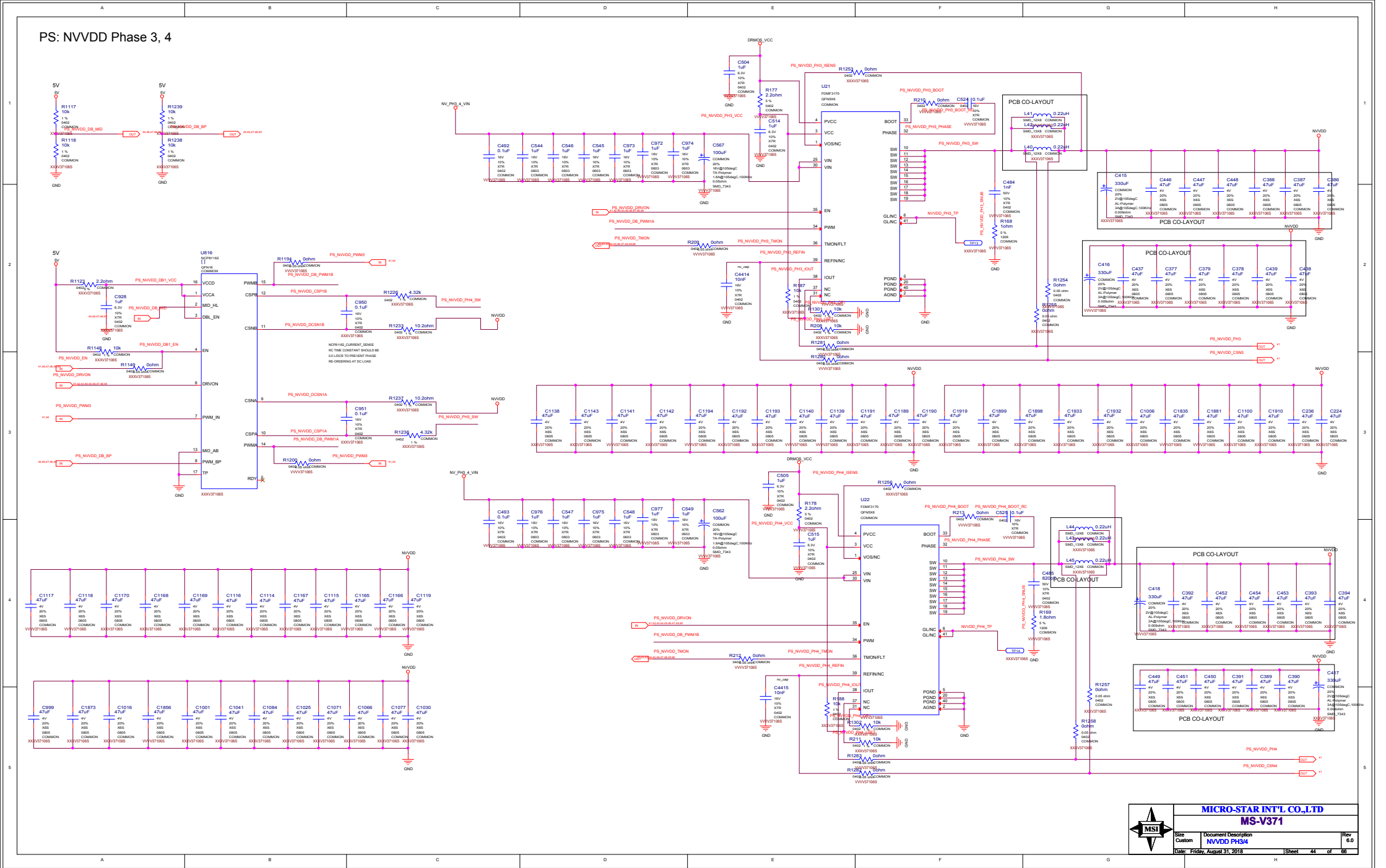


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Size Custom	Document Description <b>NVDD PH1</b>	Rev 6.0
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PS: NVDD Phase 2

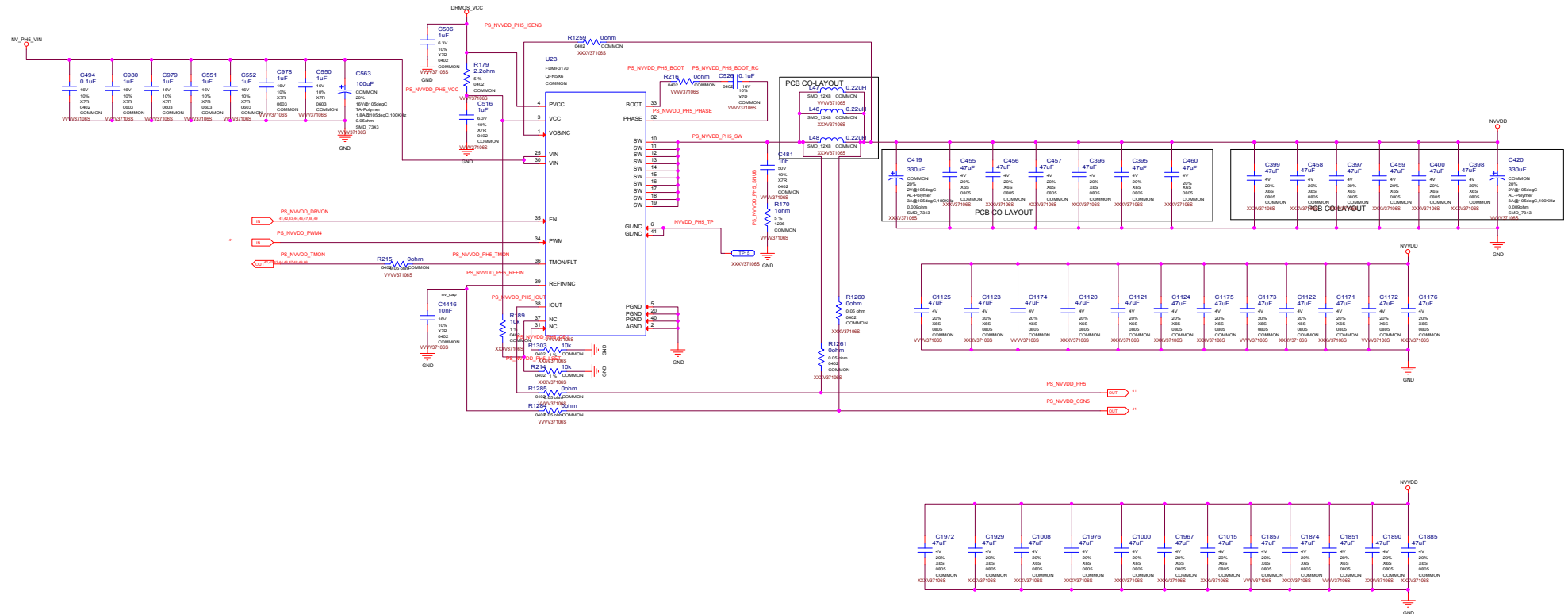




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Size Custom	Document Description NVDD PH3/4	Rev 6.0
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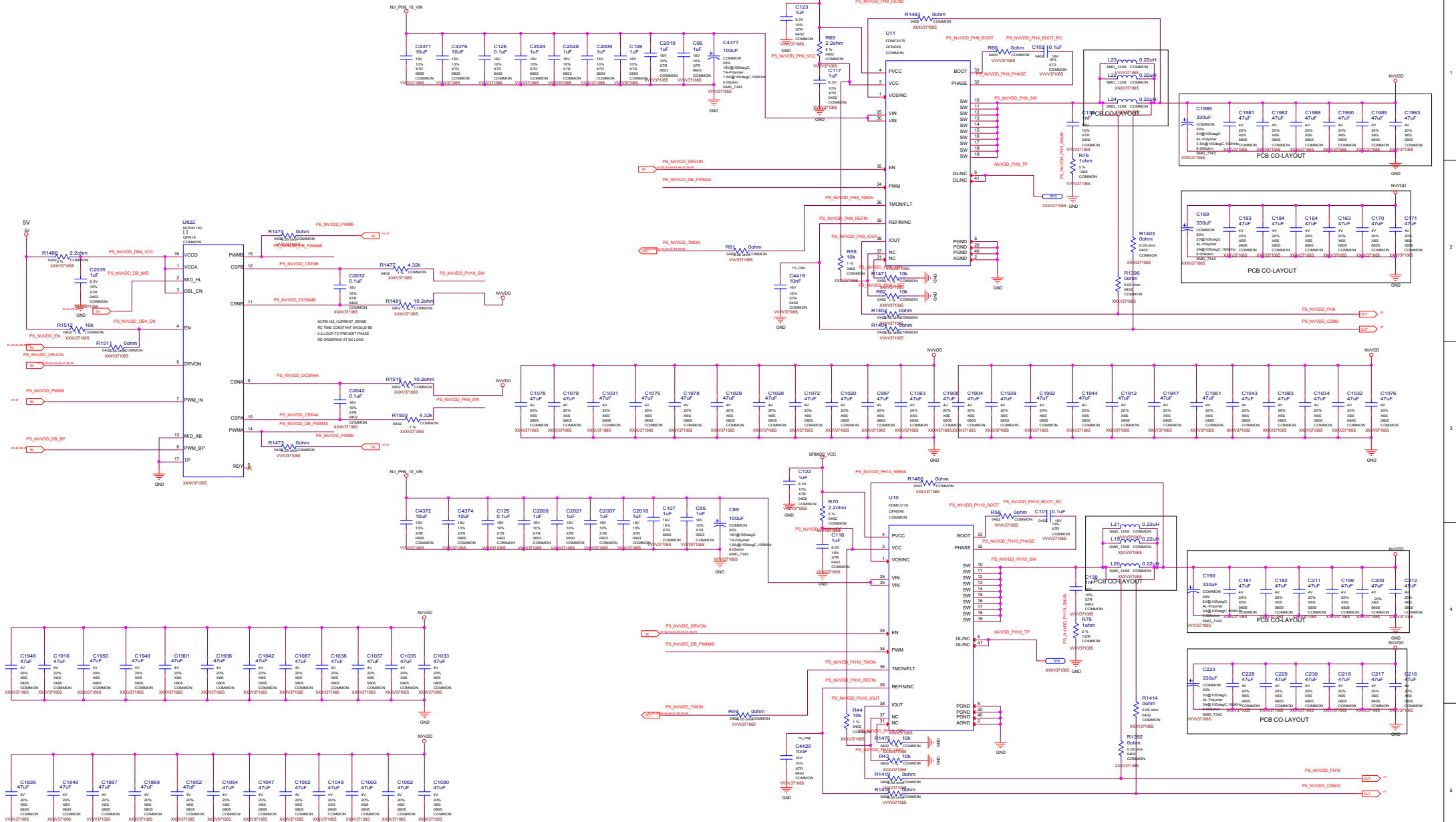




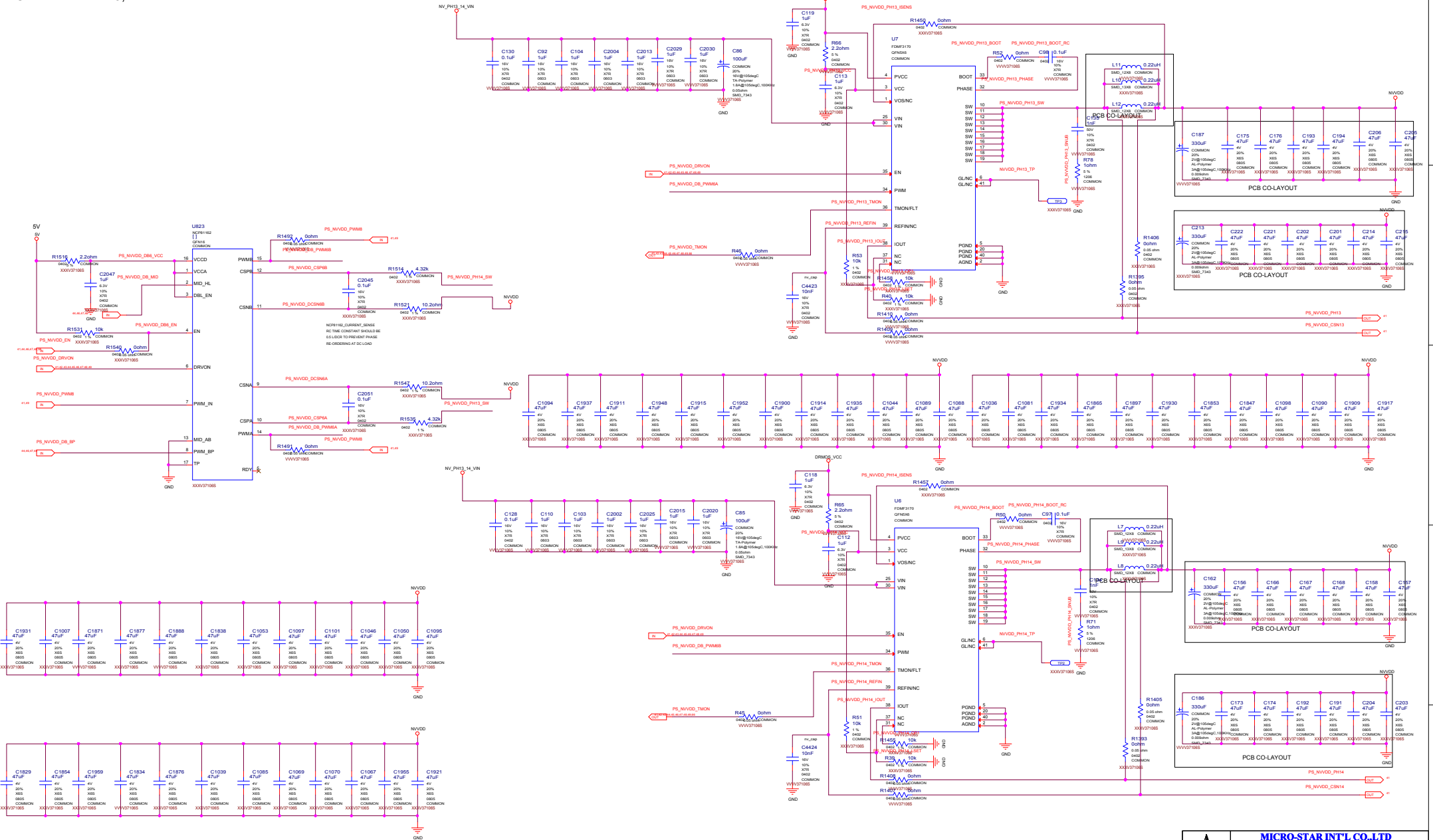
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Size Custom	Document Description <b>NVDD 5/6</b>	Rev 6.0
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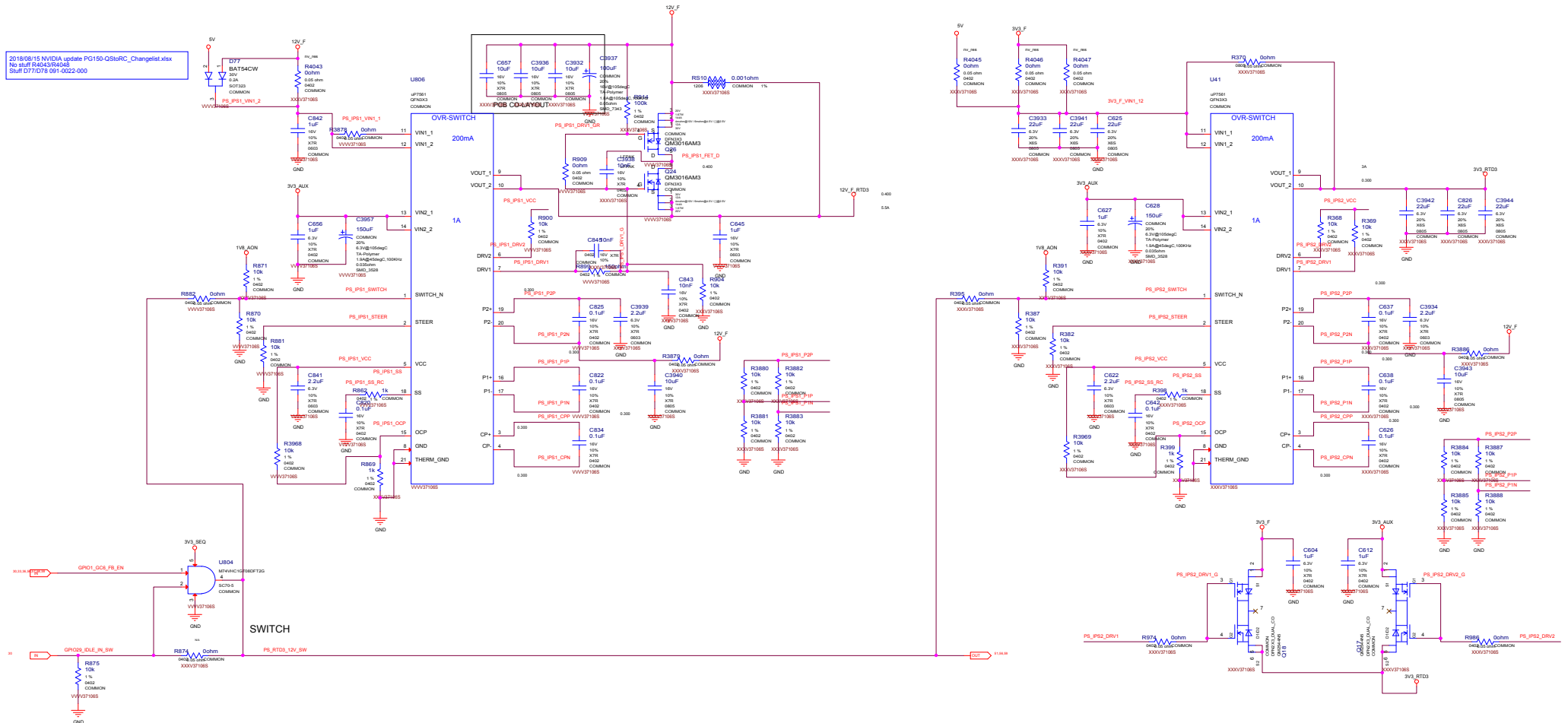
## PS: INPUT SWITCH RTD3

### AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

### AND GATE LOGIC FOR P-BOARD

GPI01	GPI029	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

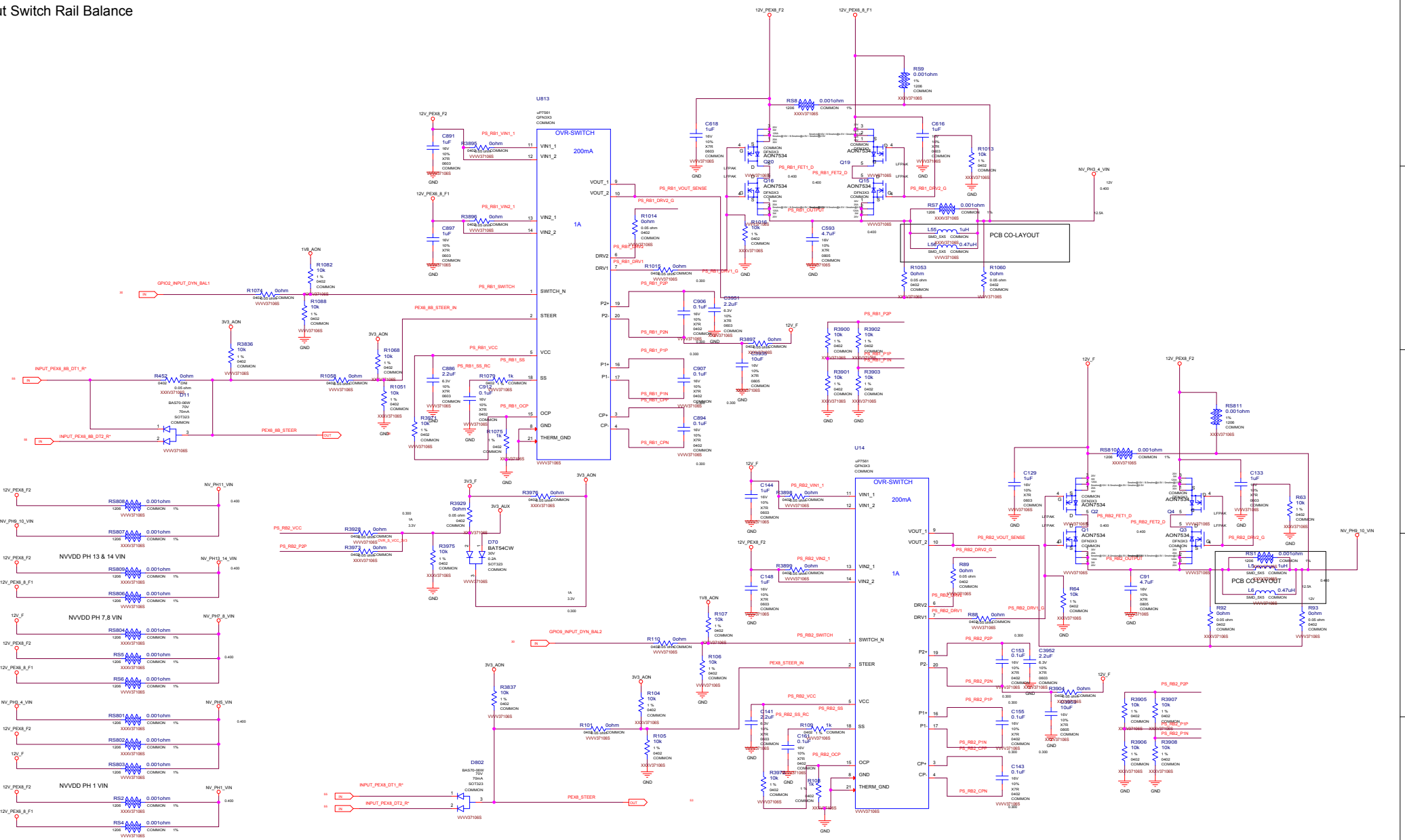


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## PS: Input Switch Rail Balance

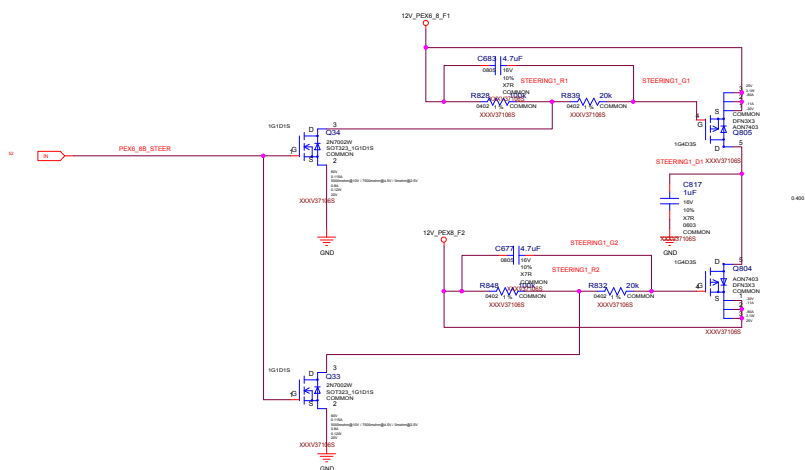


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Size Custom	Document Description <b>PS: Input Switch Rail Balance</b>	Rev 6.0
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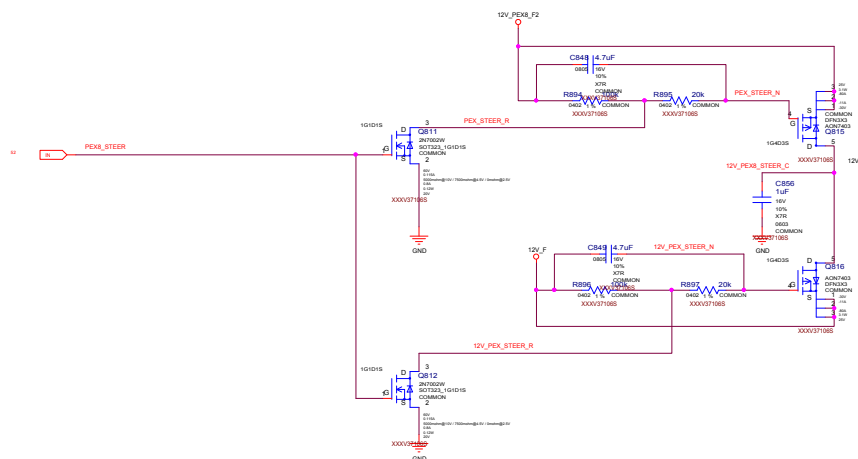


12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

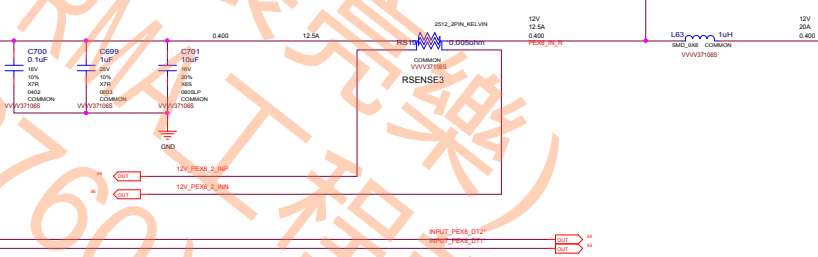
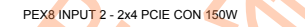
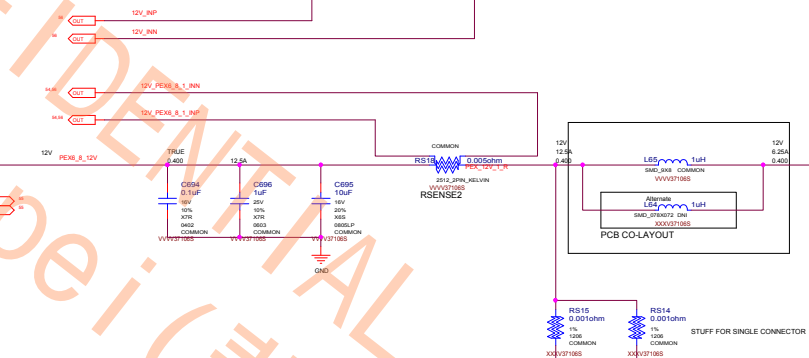
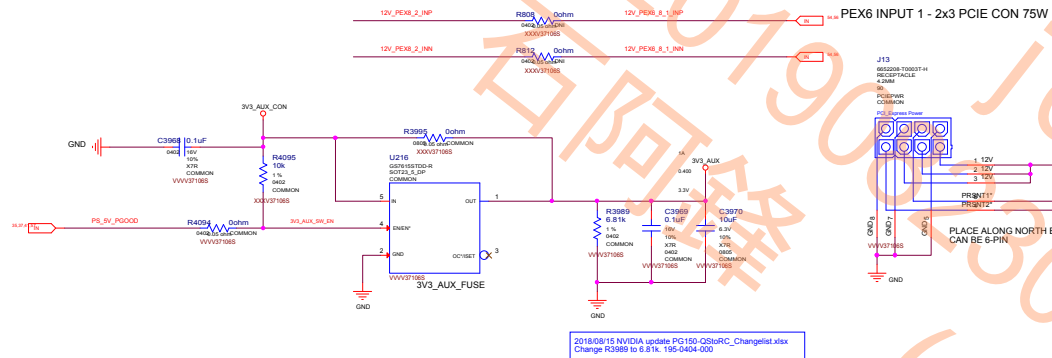
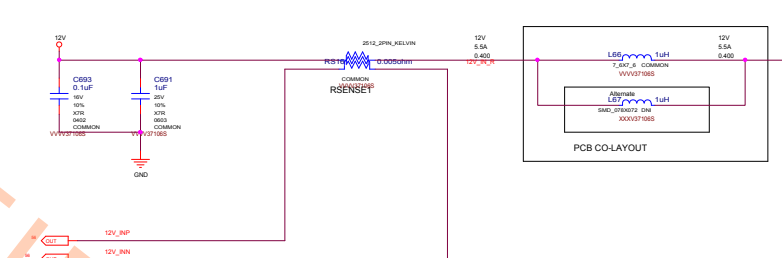
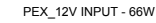
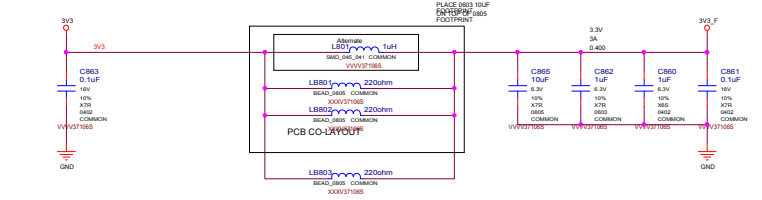
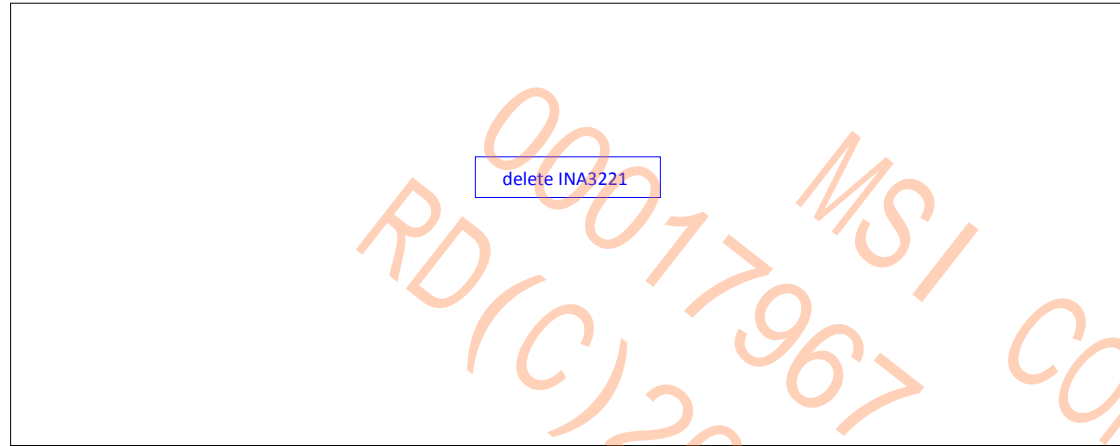


12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

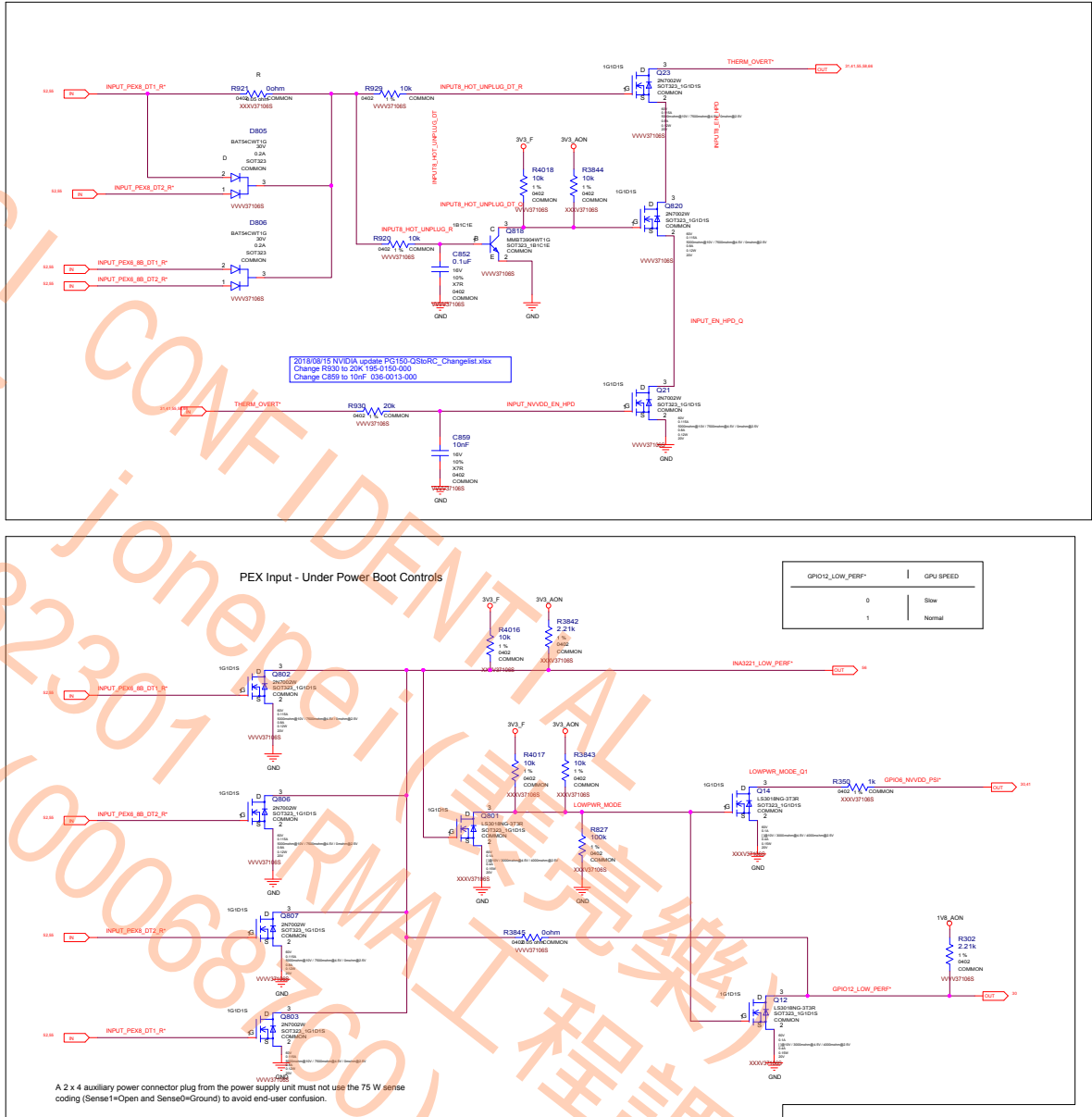
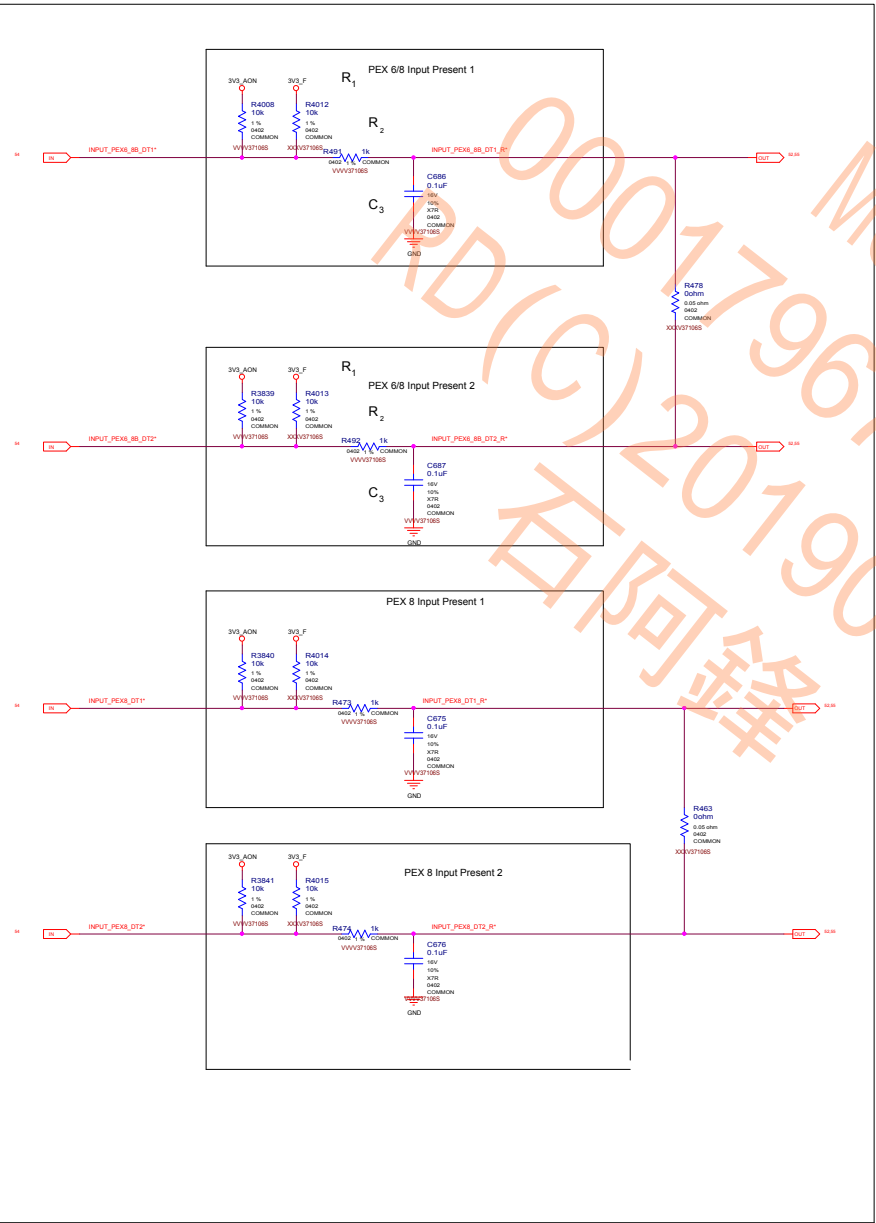
For OpenVing Type4 + Phase Doubler, 2 phase PSI mode



## PS: Inputs, Filtering, and Monitoring

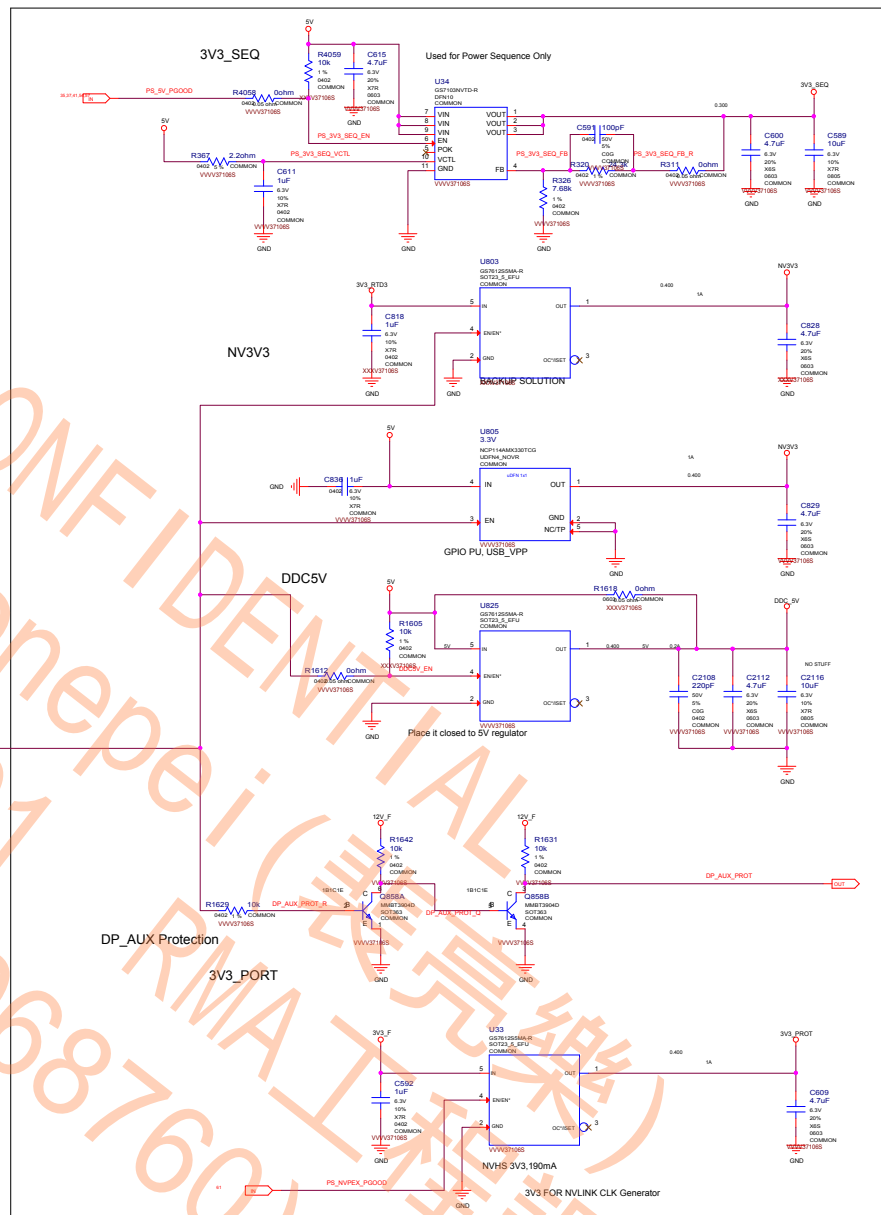
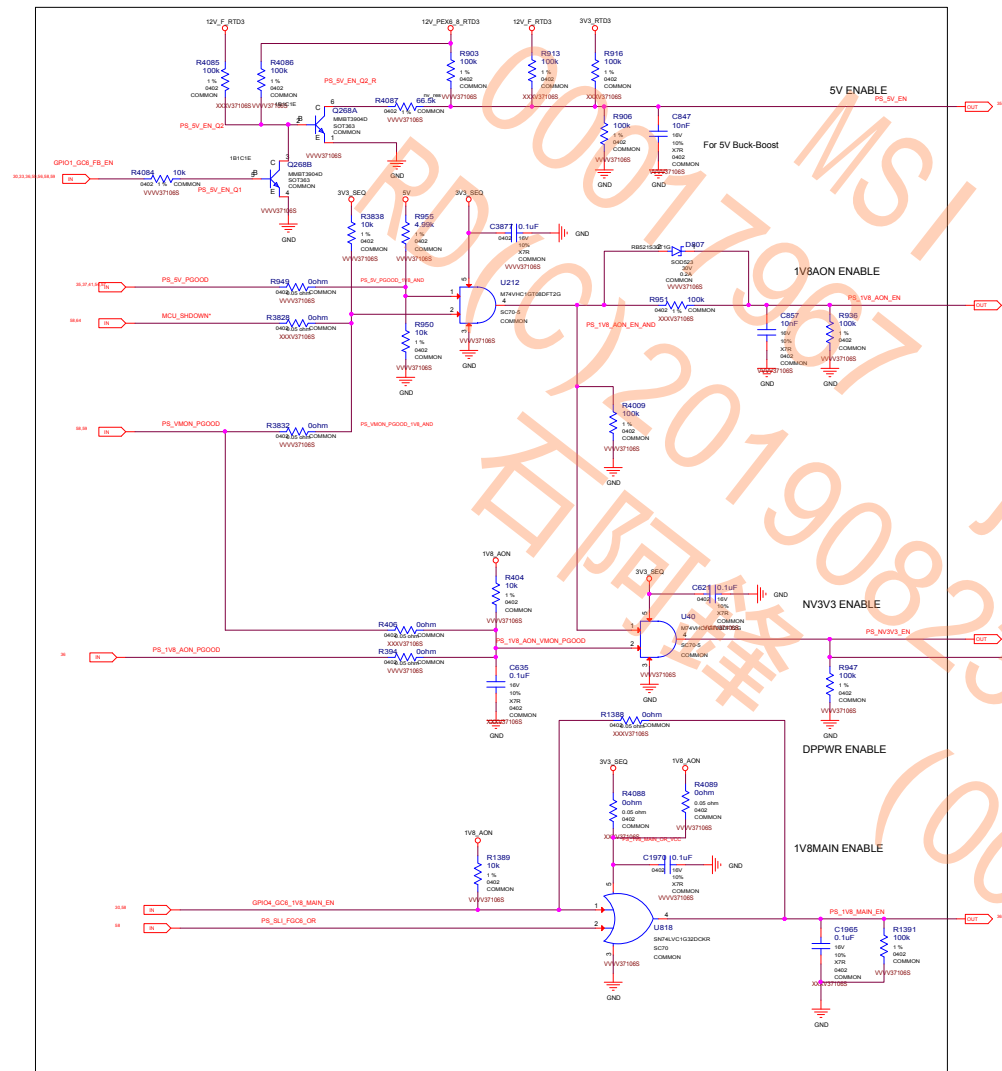


PS: 12V Current Steering & Hot Unplug Detect





SEQUENCE:5V,1V8,NV3V3 ENABLE

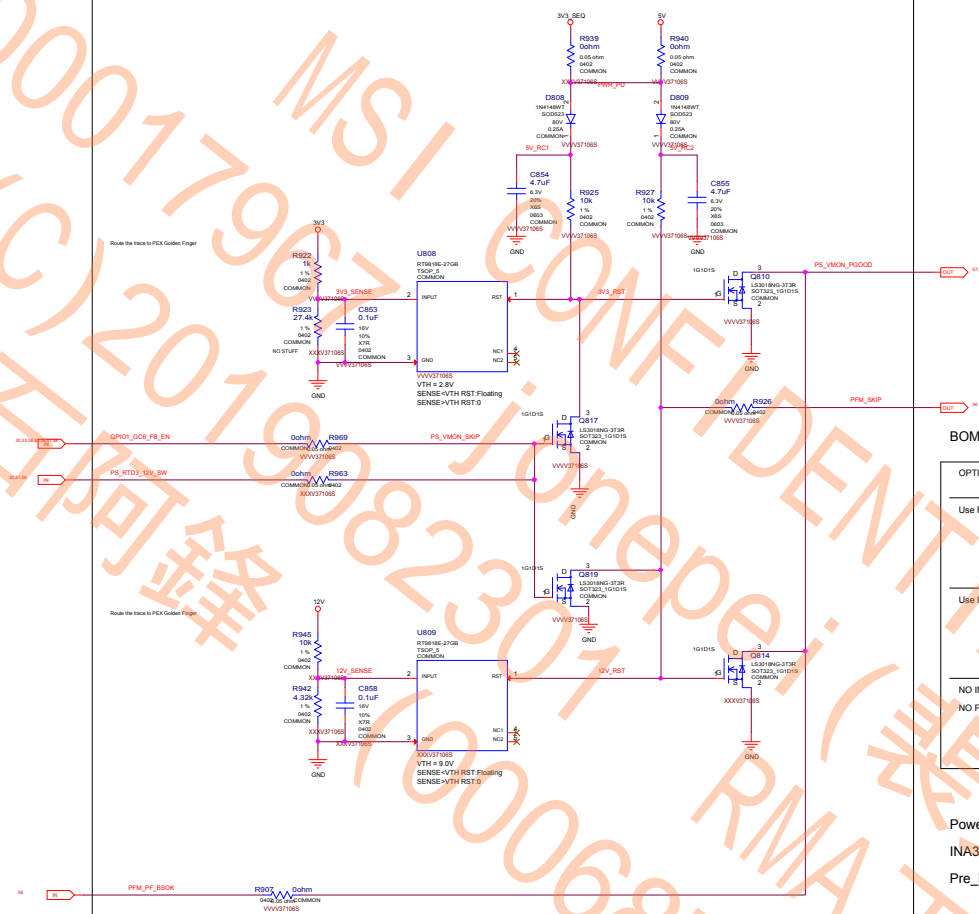


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## PCIE Voltage Monitor



### BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

## Power Supply

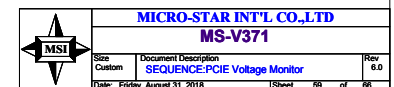
INA3221:3V3\_SEQ

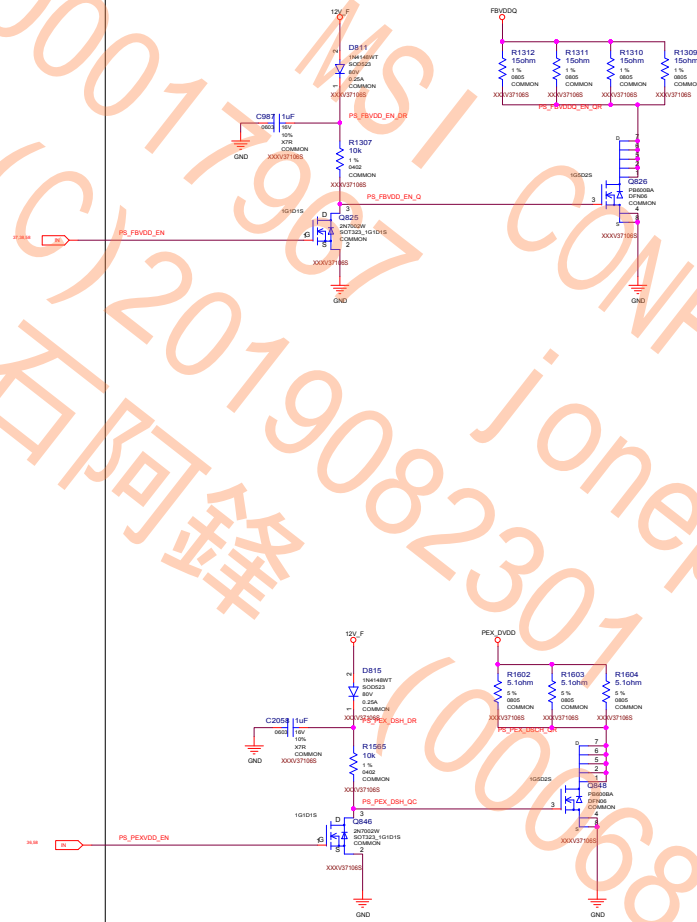
Pre\_Filter(ADC\_MUX):3V3(PEX)

Dual Pre-Filter case:

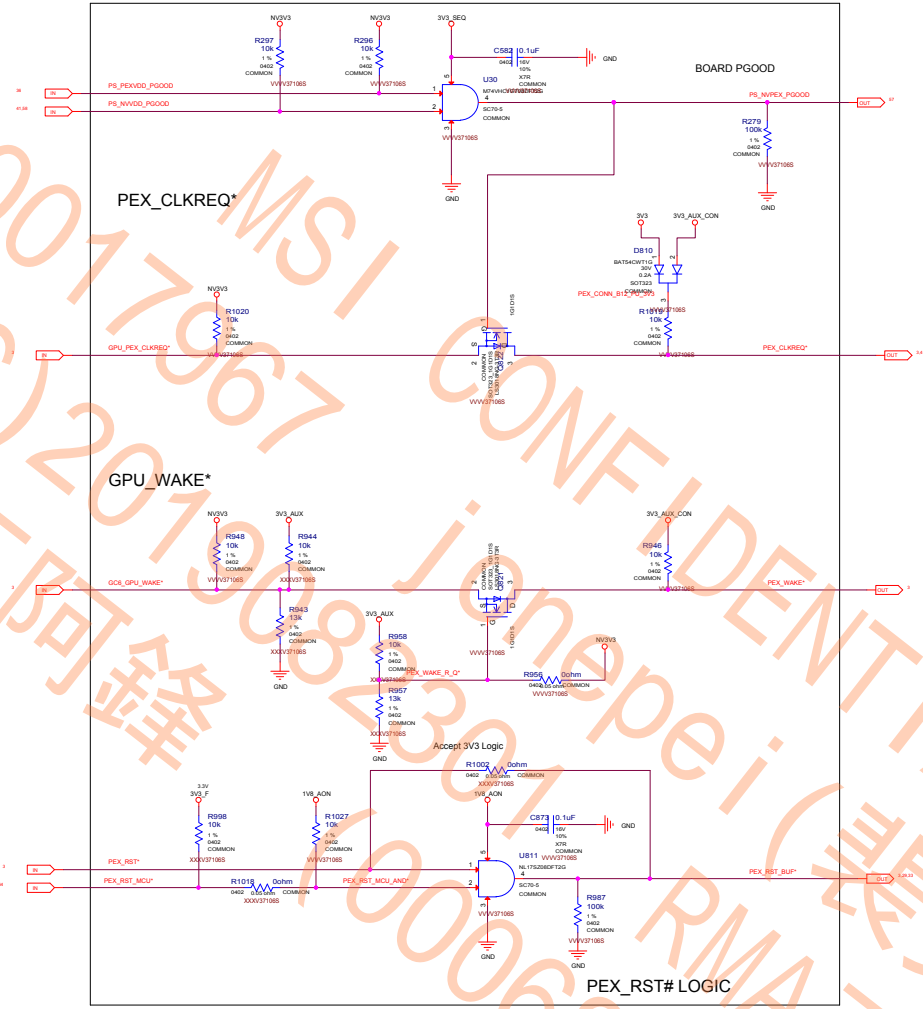
Only use the Primary Pre-Filter to sense 3V3PEX  
and All Input 12Vs

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence.Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	For INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSKOK	INPUT	For INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN & IDLE_IN_SW







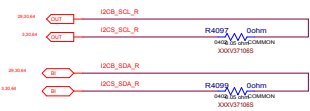


MISC: FAN & LED1

delete RGB control signals

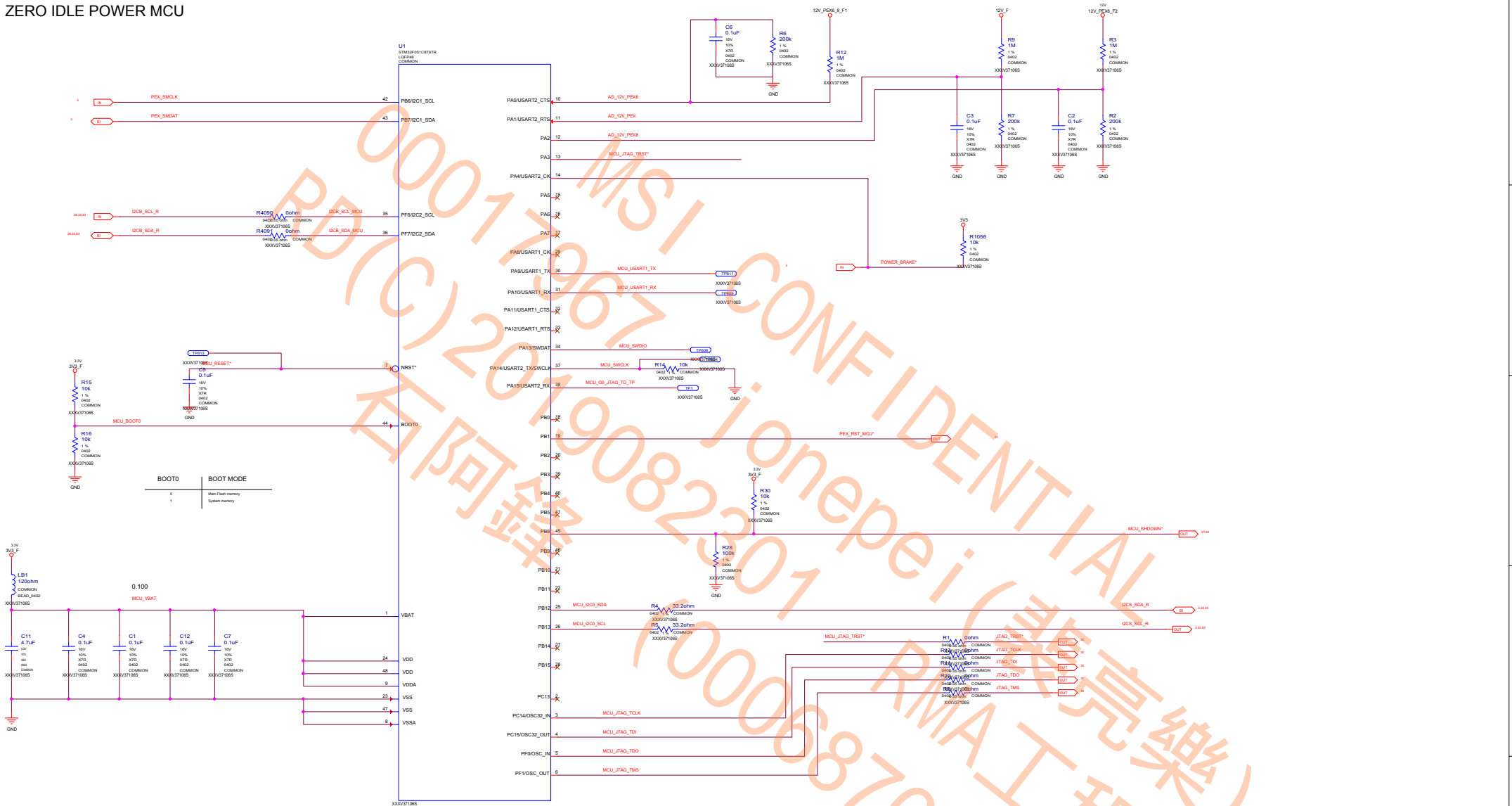
LED BOOST

delete LED's power



delete RGB control signals

## ZERO IDLE POWER MCU

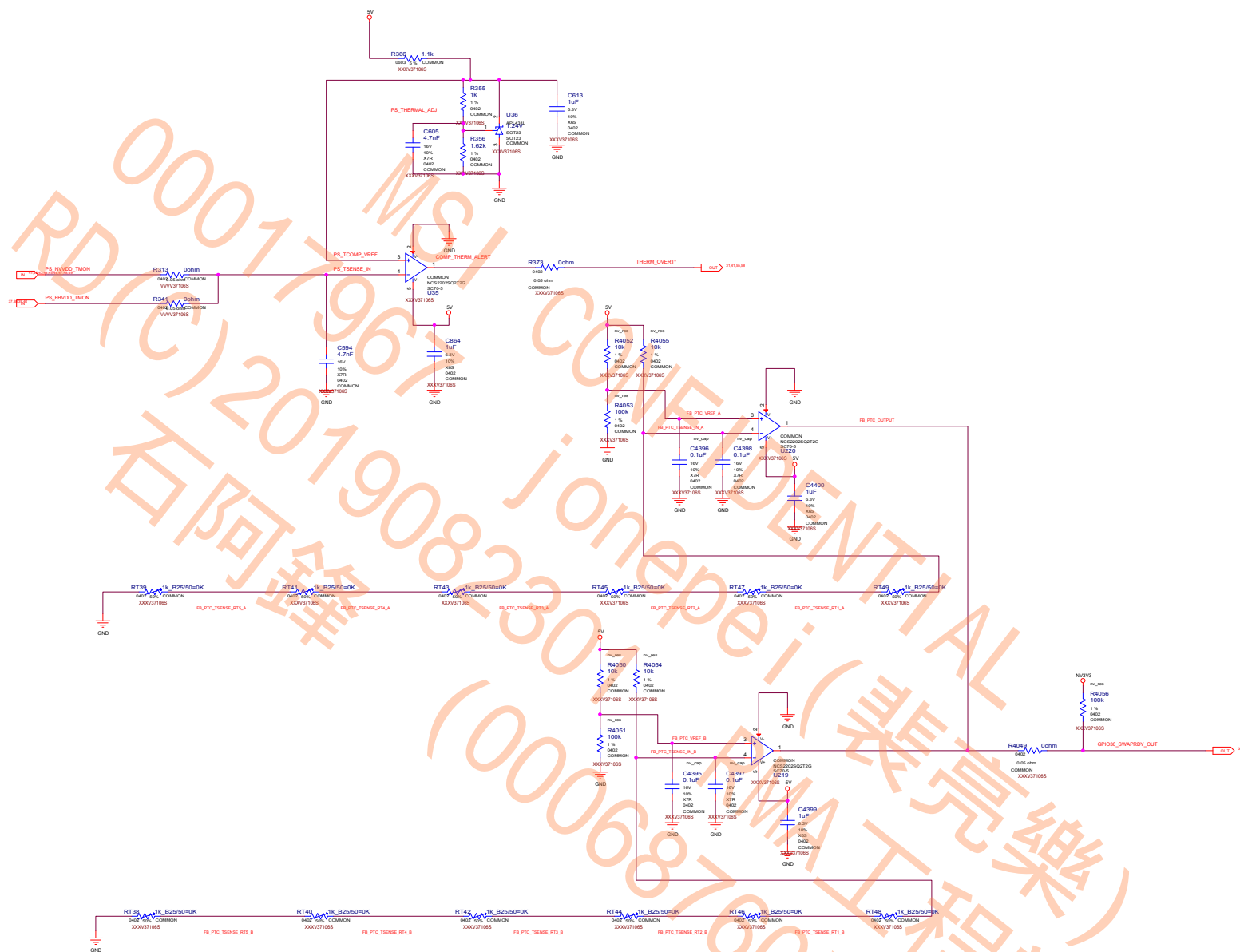


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## VR THERMAL PROTECTION



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