

# P1041-B01 GF104

GF104-300, 768MB/1536MB, GDDR5 192b 32M/64Mx32  
DVI-I-DL, DVI-I-DL/DP, mHDMI

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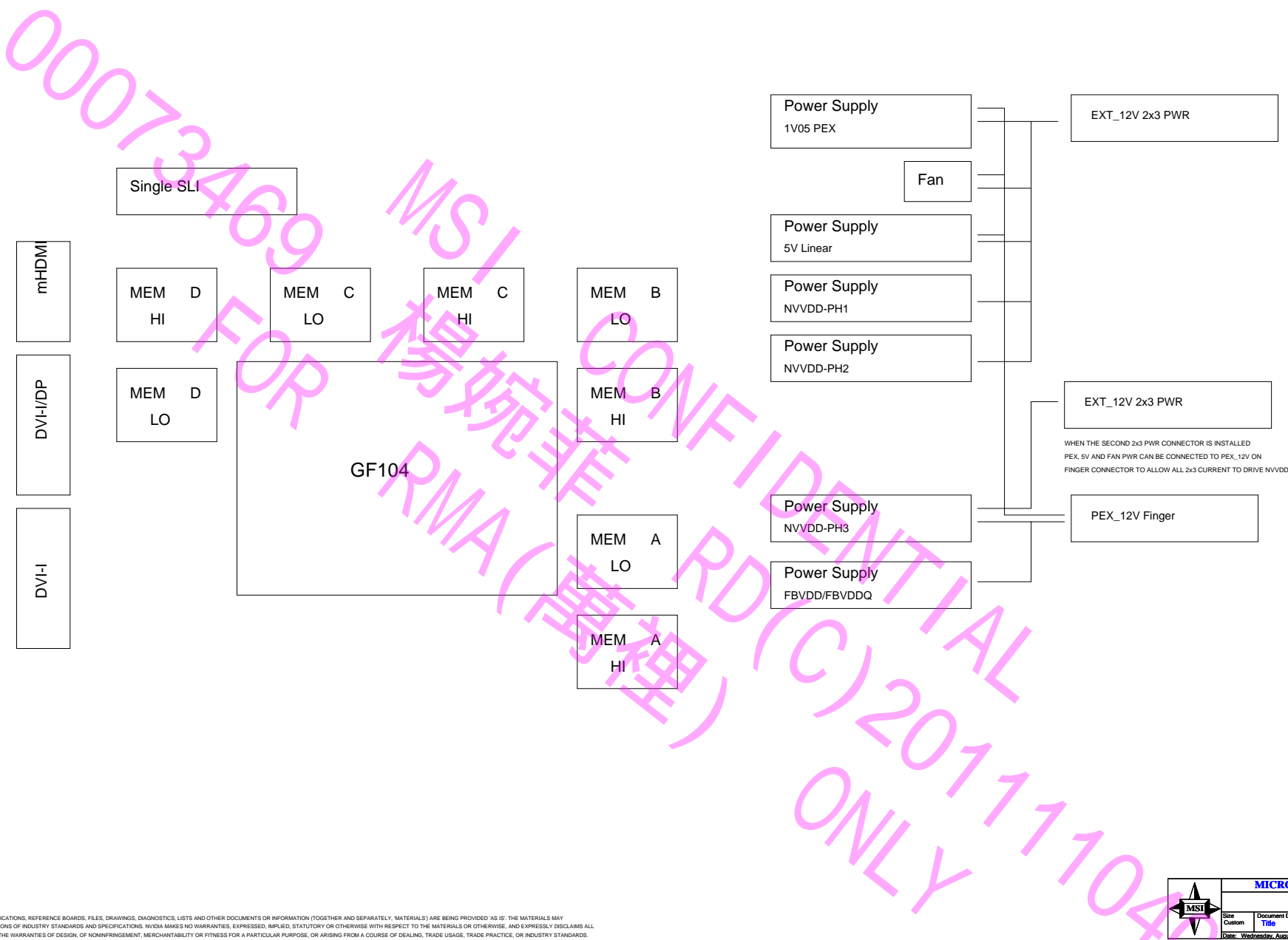
## 變更記錄

- P17，移除IC 7718
- P27，變更PEX\_VDD線路
- P28，增加R110電阻
- P29，更改PWM IC為UP6128,並且關閉第7,8兩相, 移除Xtreme Cool and OCP Unlocker對應線路
- P30，移除9V線路,LED移除,MOS改為上一下二
- P31，移除9V線路,LED移除,MOS改為上一下二
- P32，Input電感SMD改為DIP R50
- P33，增加2個MOS HSK 螺絲孔位,移除J8/J9/J10 V-check線路

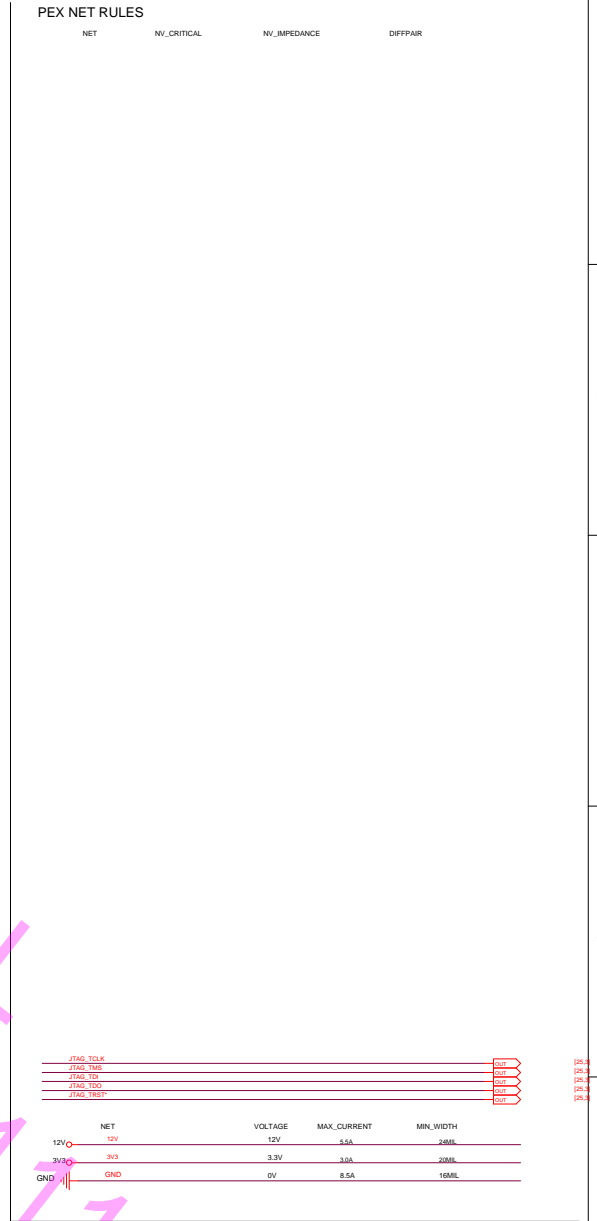
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1	SKU0000	600-11041-0000-300	P1041 GF104-300 768MB GDDR5 32Kx32 DVI-I+HDMI Frame Buffer
2	SKU0010	600-11041-0010-300	P1041 GF104-350 1536MB GDDR5 32Kx32 DVI-I+HDMI Frame Buffer
3	QS1	600-11041-0000-QS1	P1041 GF104-350 768MB GDDR5 32Kx32 Frame Buffer DVI-I+HDMI
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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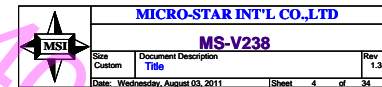


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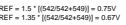
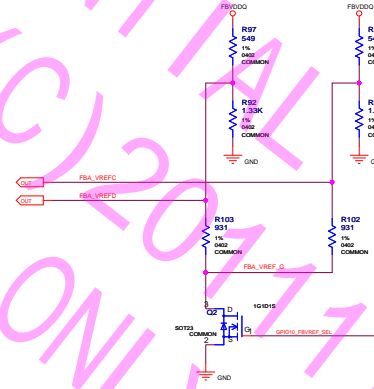
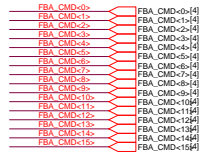
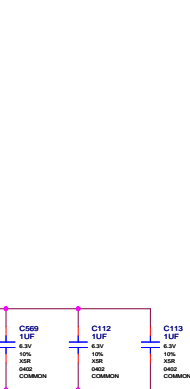
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[4]	Fba_D-0	FBA_D-0
[4]	Fba_D-1	FBA_D-1
[4]	Fba_D-2	FBA_D-2
[4]	Fba_D-3	FBA_D-3
[4]	Fba_D-4	FBA_D-4
[4]	Fba_D-5	FBA_D-5
[4]	Fba_D-7	FBA_D-7
[4]	Fba_D-8	FBA_D-8
[4]	Fba_D-9	FBA_D-9
[4]	Fba_D-10	FBA_D-10
[4]	Fba_D-11	FBA_D-11
[4]	Fba_D-12	FBA_D-12
[4]	Fba_D-13	FBA_D-13
[4]	Fba_D-14	FBA_D-14
[4]	Fba_D-15	FBA_D-15
[4]	Fba_D-16	FBA_D-16
[4]	Fba_D-17	FBA_D-17
[4]	Fba_D-18	FBA_D-18
[4]	Fba_D-19	FBA_D-19
[4]	Fba_D-20	FBA_D-20
[4]	Fba_D-21	FBA_D-21
[4]	Fba_D-22	FBA_D-22
[4]	Fba_D-23	FBA_D-23
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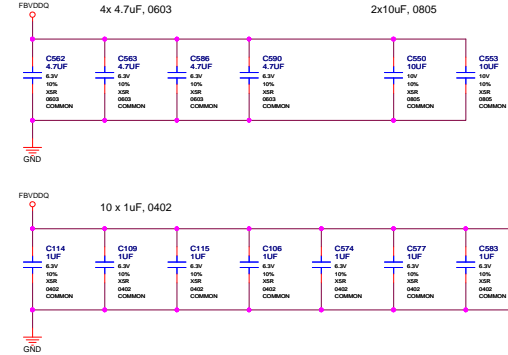
\*\* Vref switching options:  
 - internal Vref should be POR for VrefD  
 - potential for update



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GDDR5 CMD Mapping		
Cmd	IO	IO
Cmd0	CAS*	
Cmd1	CS*	
Cmd2	RST*	
Cmd3	RA*	
Cmd4	A1, A0	
Cmd5	A0, A10	
Cmd6	A0, A10	
Cmd7	AB*	
Cmd8	A0, A11	
Cmd9	A0, A0	
Cmd10	A0, A0	
Cmd11	A0, A0	
Cmd12	A0, A0	
Cmd13	A0, A0	
Cmd14	A0, A0	
Cmd15	CS*	
Cmd16	CAS*	
Cmd17	CS*	
Cmd18	RST*	
Cmd19	RA*	
Cmd20	A1, A0	
Cmd21	A0, A10	
Cmd22	A0, A10	
Cmd23	AB*	
Cmd24	A0, A11	
Cmd25	A0, A0	
Cmd26	A0, A0	
Cmd27	A0, A0	
Cmd28	A0, A0	
Cmd29	A0, A0	
Cmd30	A0, A0	
Cmd31	CS*	

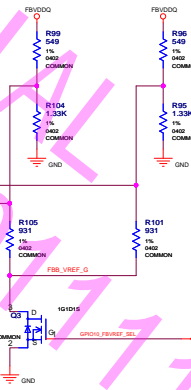
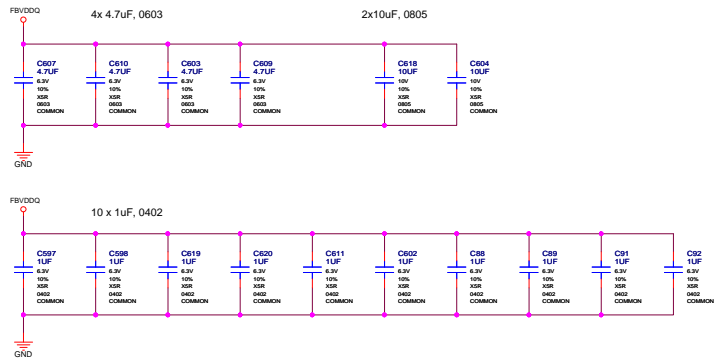
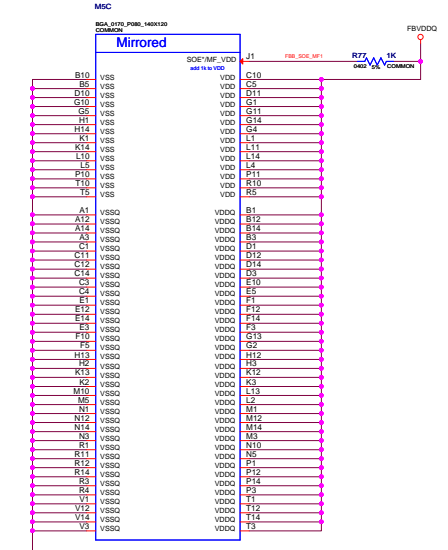
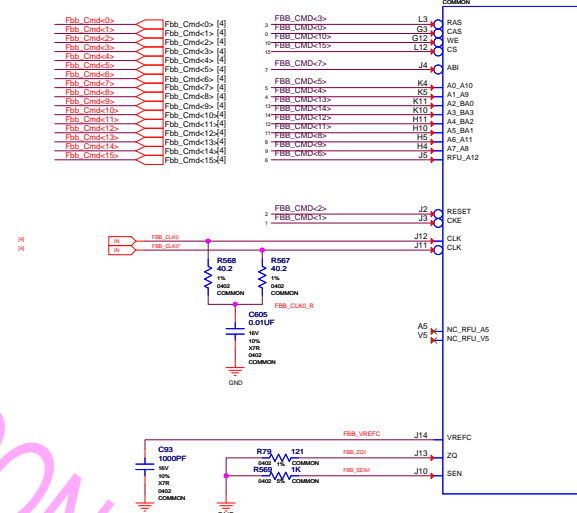
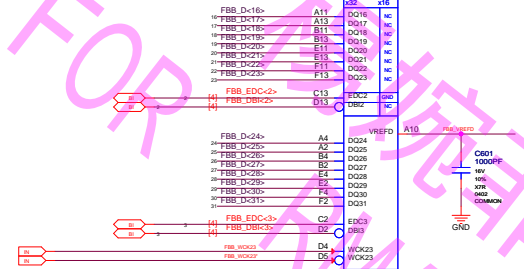
\*\* Vref switching option:  
external Vref should be POR for VrefH  
potential for update



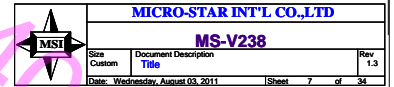
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A	B	C	D	E	F	G	H
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Figure 1: Schematic representation of the 1000 Genomes Project. The figure shows a vertical list of 1000 samples, each with a color-coded label (e.g., Fbb, D-1, Fbb, D-2) and a corresponding colored bar representing the sample's genetic data. The samples are grouped into 100 clusters, each containing 10 samples. The clusters are color-coded: red (1-10), orange (11-20), yellow (21-30), green (31-40), blue (41-50), purple (51-60), brown (61-70), pink (71-80), grey (81-90), and black (91-100). The samples are arranged in a grid-like fashion, with the sample ID on the left and the colored bar on the right.



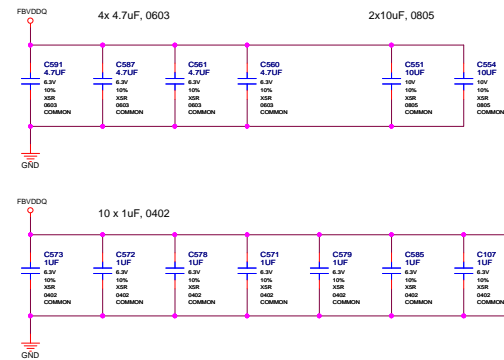
$$\begin{aligned} V_{REF} &= 1.5 * ((542/542+549)) = 0.75V \\ V_{REF} &= 1.35 * ((542/542+549)) = 0.67V \end{aligned}$$





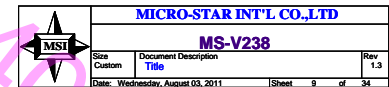
GDDR5 CMD Mapping		
Cmd	0..31	32..63
Cmd0	CAS*	
Cmd1	OE*	
Cmd2	REST	
Cmd3	RA*	
Cmd4	A1..A8	
Cmd5	AL..A15	
Cmd6	A10..RFU	
Cmd7	AB*	
Cmd8	HE*	
Cmd9	A1..A8	
Cmd10	AL..A15	
Cmd11	AL..BA1	
Cmd12	AL..BA2	
Cmd13	AL..BA3	
Cmd14	AL..BA3	
Cmd15	CD*	
Cmd16		CAS*
Cmd17		OE*
Cmd18		REST
Cmd19		RA*
Cmd20		A1..A8
Cmd21		AL..A15
Cmd22		A10..RFU
Cmd23		AB*
Cmd24		HE*
Cmd25		A1..A8
Cmd26		AL..A15
Cmd27		AL..BA1
Cmd28		AL..BA2
Cmd29		AL..BA3
Cmd30		AL..BA3
Cmd31		CD*

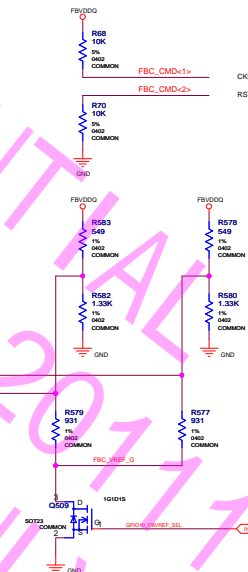
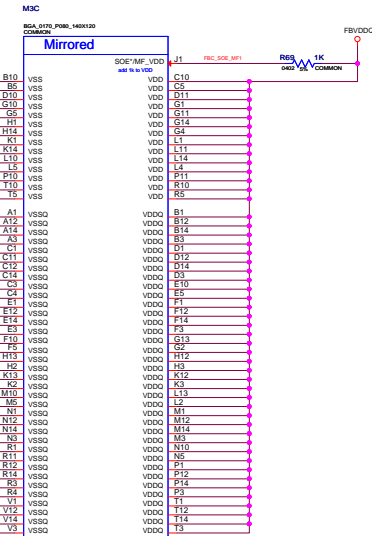
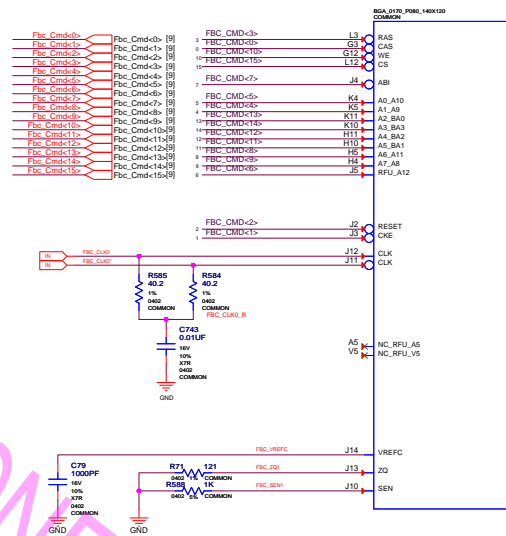
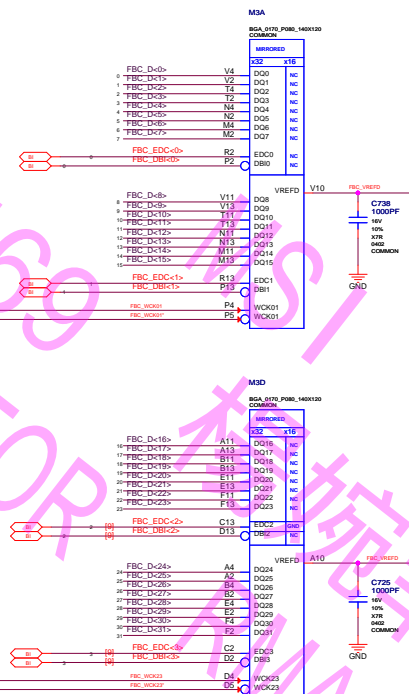
\*\* Vref switching options:  
- Internal Vref should be POR for VrefD  
- potential for update



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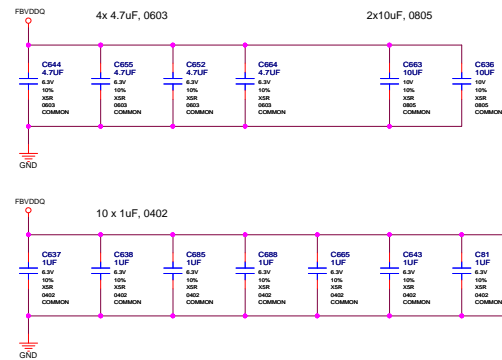
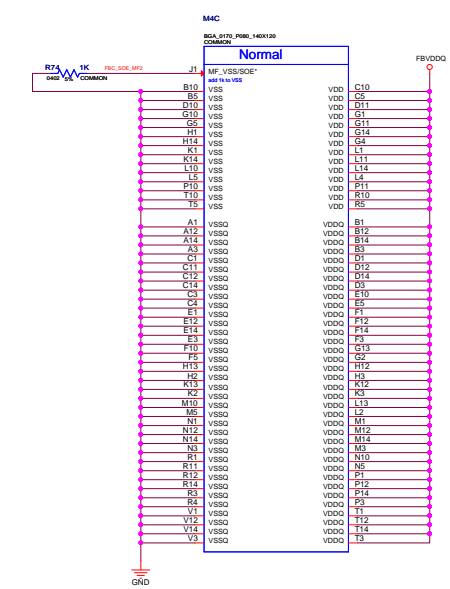
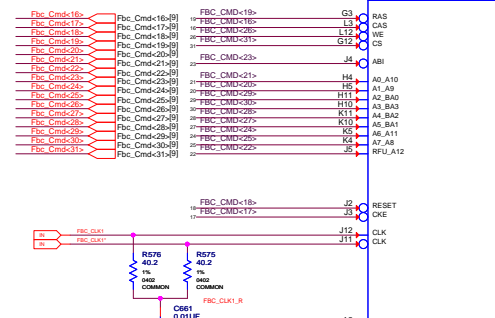
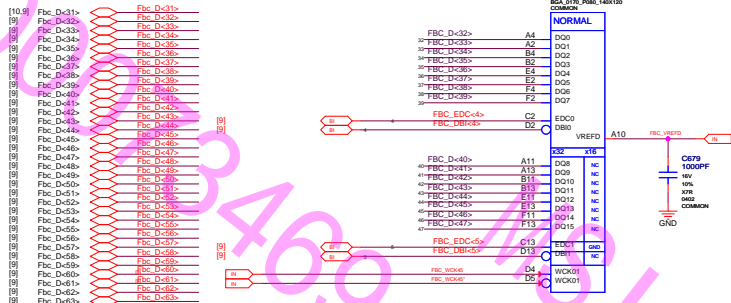




$$\begin{aligned} \text{VREF} &= 1.5 \cdot \left[ \frac{1.33\text{K}}{(549+1.33\text{K})} \right] = 1.06\text{V} \\ \text{VREF} &= 1.5 \cdot \left[ \frac{542/542+549}{542/542+549} \right] = 0.75\text{V} \\ \text{VREF} &= 1.35 \cdot \left[ \frac{542/542+549}{542/542+549} \right] = 0.67\text{V} \end{aligned}$$

GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CAS*	
CMD2	RST*	
CMD3	BA0*	
CMD4	A1..A9	
CMD5	A0..A10	
CMD6	A10..RPU	
CMD7	AB*	
CMD8	AL..A11	
CMD9	AZ..AB	
CMD10	WE*	
CMD11	AL..BA1	
CMD12	AL..BA2	
CMD13	A3..BA3	
CMD14	A3..BA3	
CMD15	CS*	
CMD16	CAS*	
CMD17	CAS*	
CMD18	RST*	
CMD19	BA0*	
CMD20	A1..A9	
CMD21	A0..A10	
CMD22	A10..RPU	
CMD23	AB*	
CMD24	AL..A11	
CMD25	AZ..AB	
CMD26	WE*	
CMD27	AL..BA1	
CMD28	AL..BA2	
CMD29	A3..BA3	
CMD30	A3..BA3	
CMD31	CS*	

\*\* Vref switching options:  
 - Internal Vref should be POR for VrefD  
 - potential for options



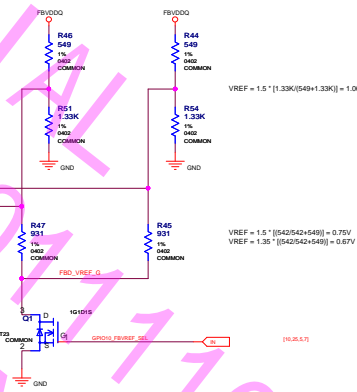
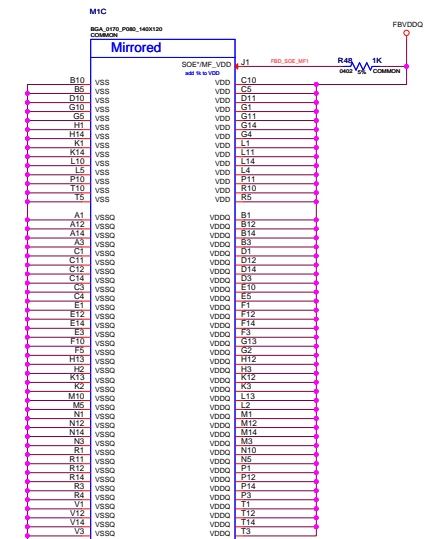
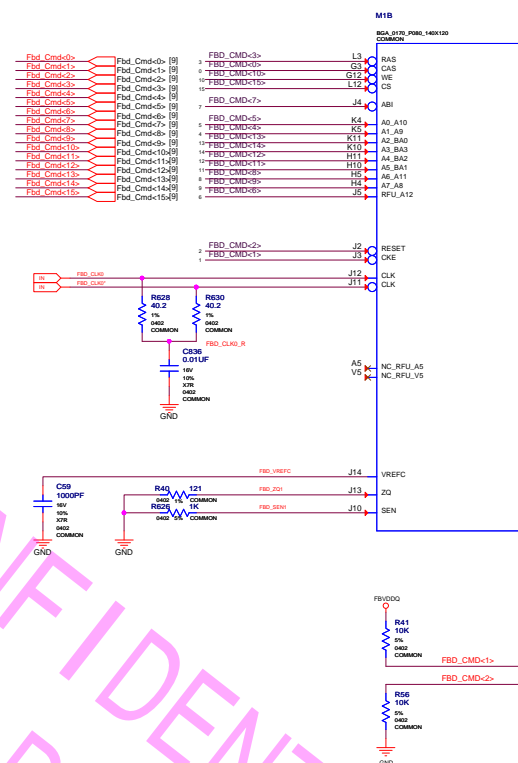
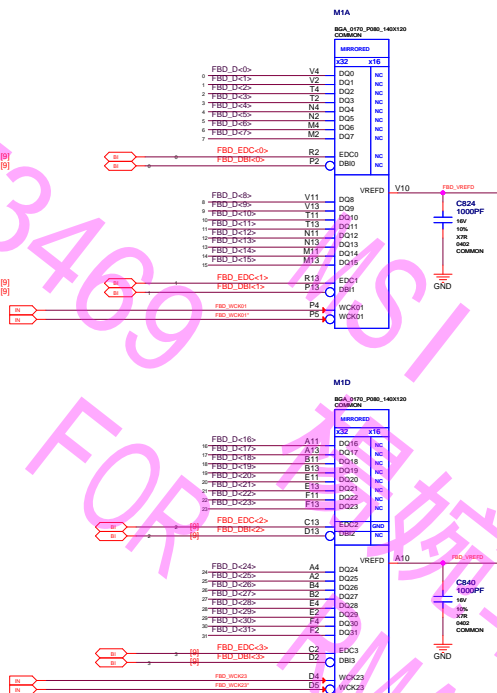
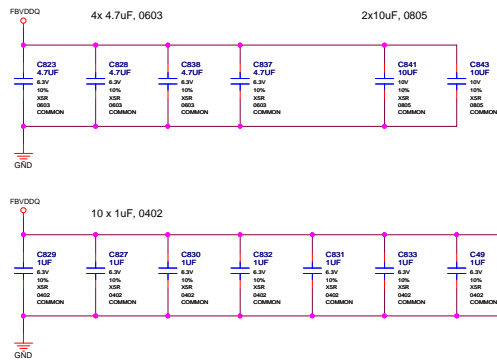
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GDORs CMD Mapping		
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CM01	CM07	
CM02	CM07	
CM03	CM07	
CM04	CM07	
CM05	CM07	
CM06	CM07	
CM07	CM07	
CM08	CM07	
CM09	CM07	
CM10	CM07	
CM11	CM07	
CM12	CM07	
CM13	CM07	
CM14	CM07	
CM15	CM07	
CM16	CM07	
CM17	CM07	
CM18	CM07	
CM19	CM07	
CM20	CM07	
CM21	CM07	
CM22	CM07	
CM23	CM07	
CM24	CM07	
CM25	CM07	
CM26	CM07	
CM27	CM07	
CM28	CM07	
CM29	CM07	
CM30	CM07	
CM31	CM07	

\*\* Vref switching option:  
- Internal Vref should be POR for VrefD  
- potential for update

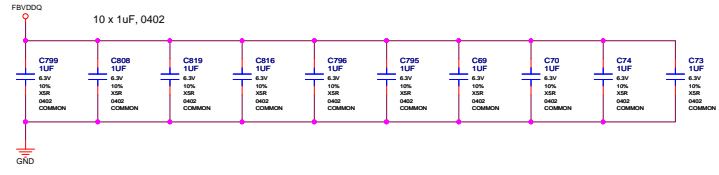
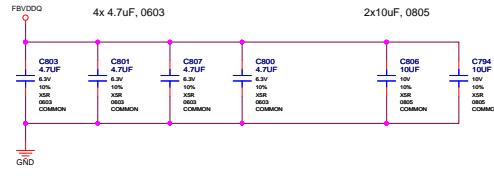
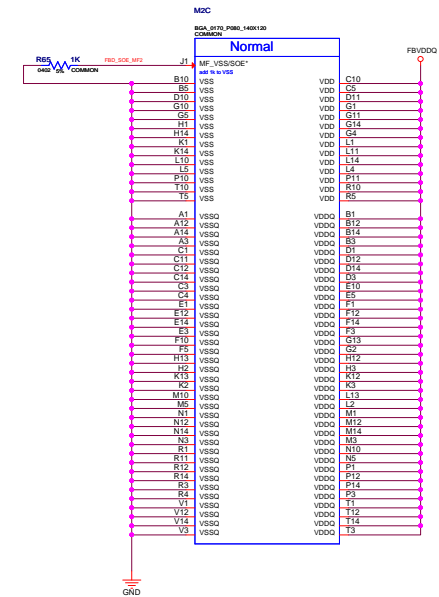
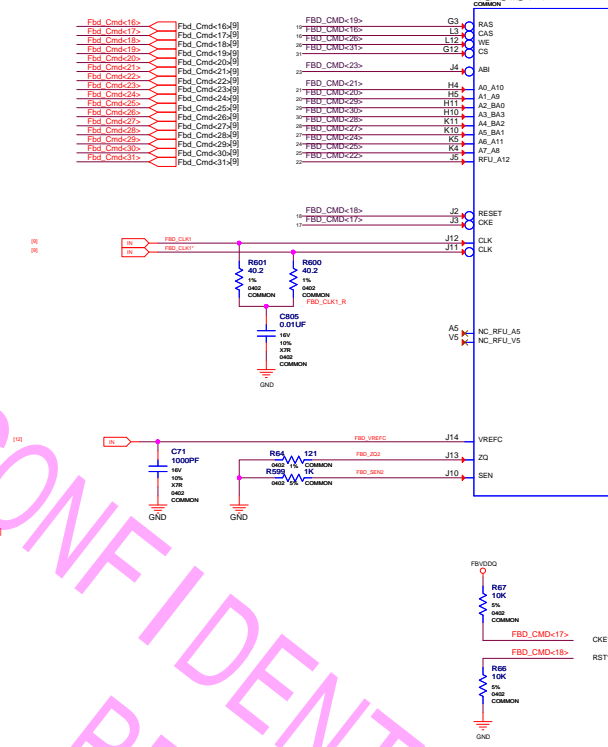
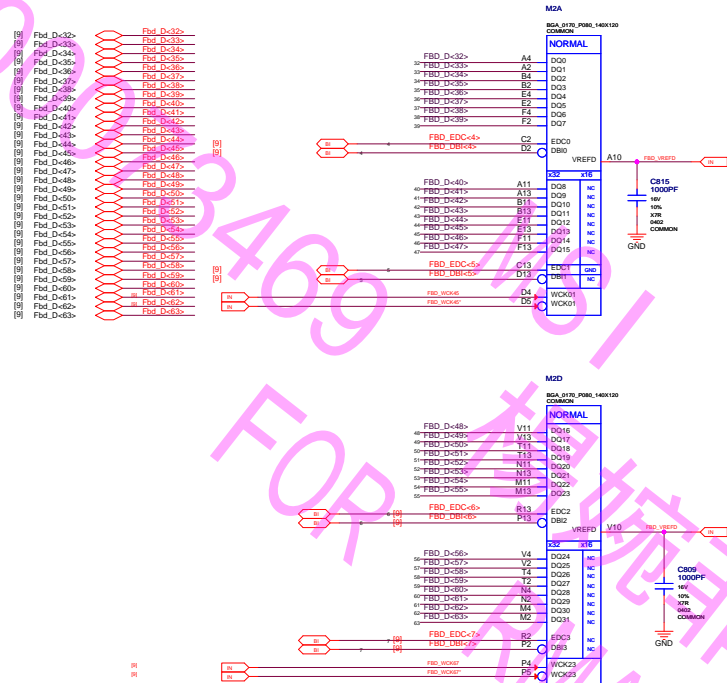


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Custom	Title	1.3
Date:	Wednesday, August 03, 2011	Sheet 12 of 34

GDGERS CMD Mapping		
CMD	S-31	S0-03
CMD0	CAS?	
CMD1	CDE?	
CMD2	RAS?	
CMD3	BS?	
CMD4	A1_A3	
CMD5	A2_A10	
CMD6	A2_IFPU	
CMD7	AB?	
CMD8	AE_A11	
CMD9	AE_A8	
CMD10	W?	
CMD11	AS_A4	
CMD12	AS_BA2	
CMD13	A3_BA0	
CMD14	A3_BA3	
CMD15	C?	
CMD16		CAS?
CMD17		CDE?
CMD18		BS?
CMD19		RAS?
CMD20		A1_A3
CMD21		A2_A10
CMD22		A2_IFPU
CMD23		AB?
CMD24		AE_A11
CMD25		AE_A8
CMD26		W?
CMD27		AS_A4
CMD28		AS_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		C?

- internal Vref should be POR for VrefD
- potential for update

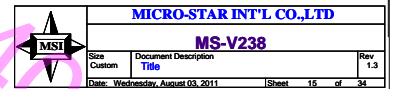


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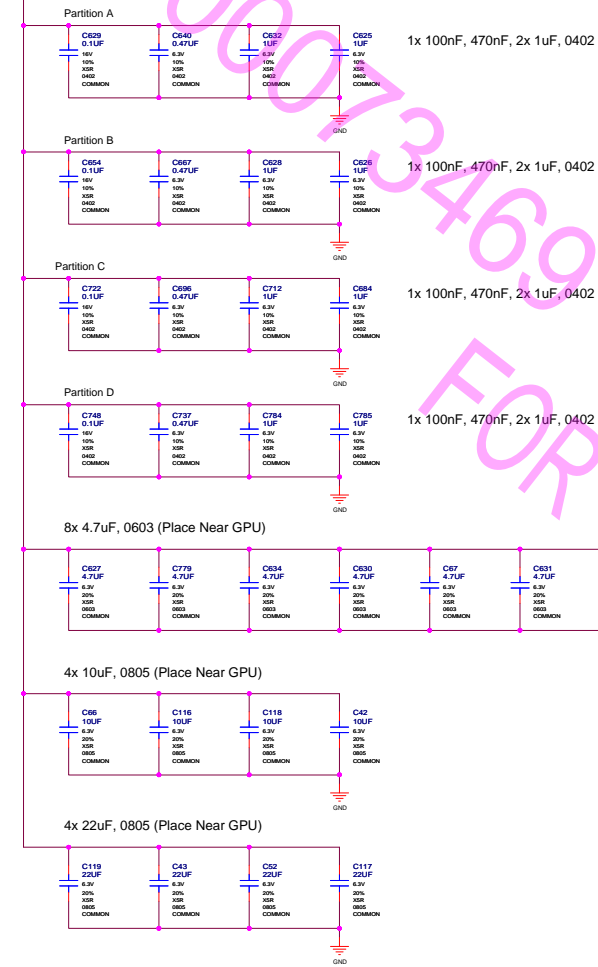
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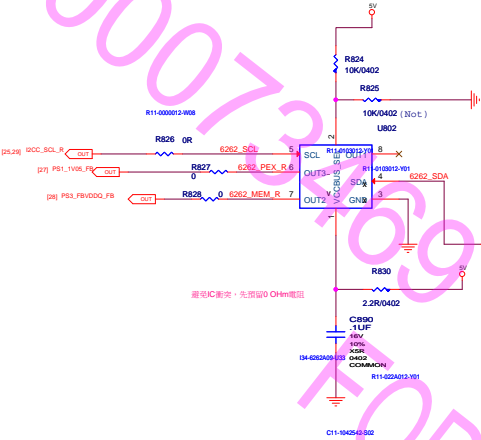


## FBVDDQ



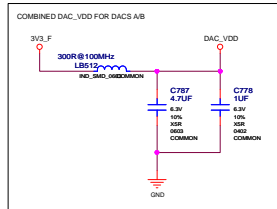
## NVVDD



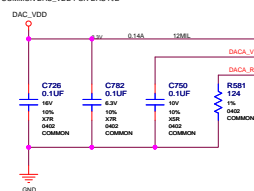


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COMMON DAC\_VDD FOR DAC A/B



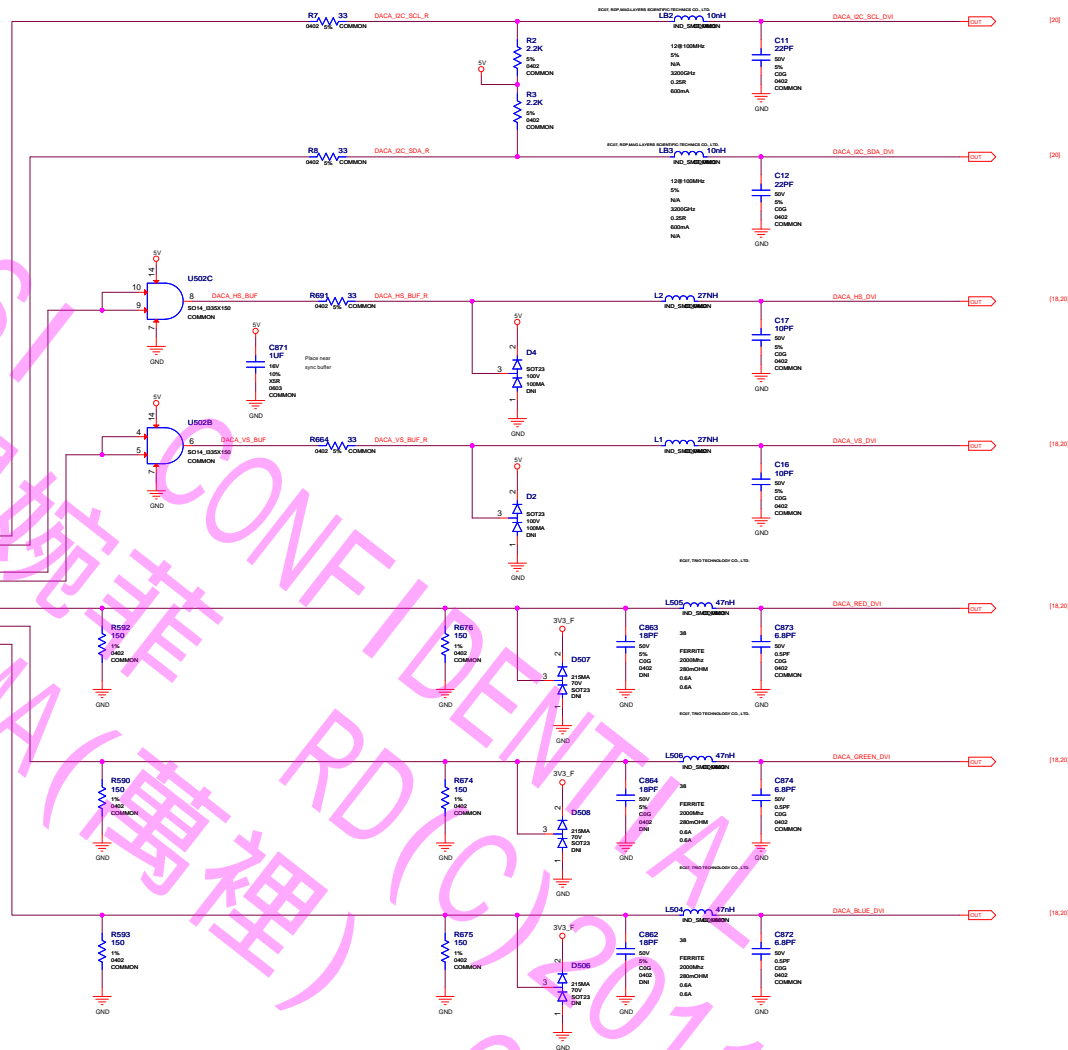
## DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE
DACA_RED_DVI	1	75OHM
DACA_GREEN_DVI	1	75OHM
DACA_BLUE_DVI	1	75OHM
DACA_HS_DVI	2	50OHM
DACA_VS_DVI	2	50OHM

NET	NV_CRITICAL	NV_IMPEDANCE
DACA_RED_DVI	1	75OHM
DACA_GREEN_DVI	1	75OHM
DACA_BLUE_DVI	1	75OHM

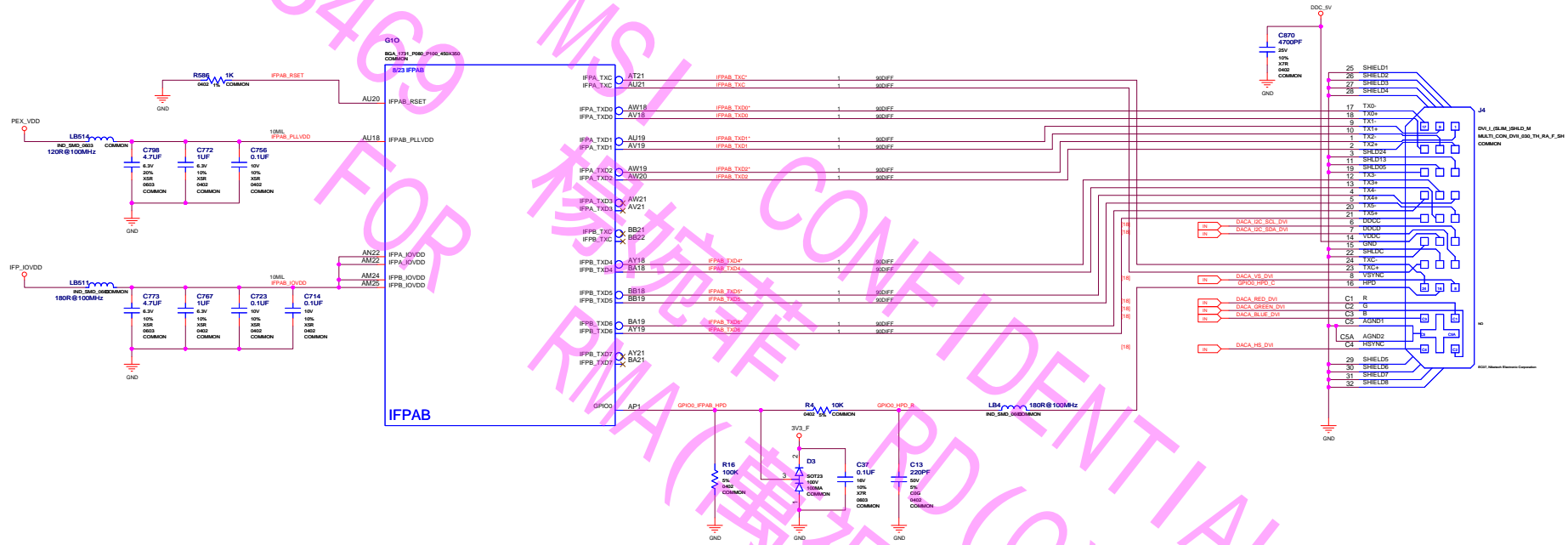
NET	NV_CRITICAL	NV_IMPEDANCE
DACA_HS_DVI	2	50OHM
DACA_VS_DVI	2	50OHM

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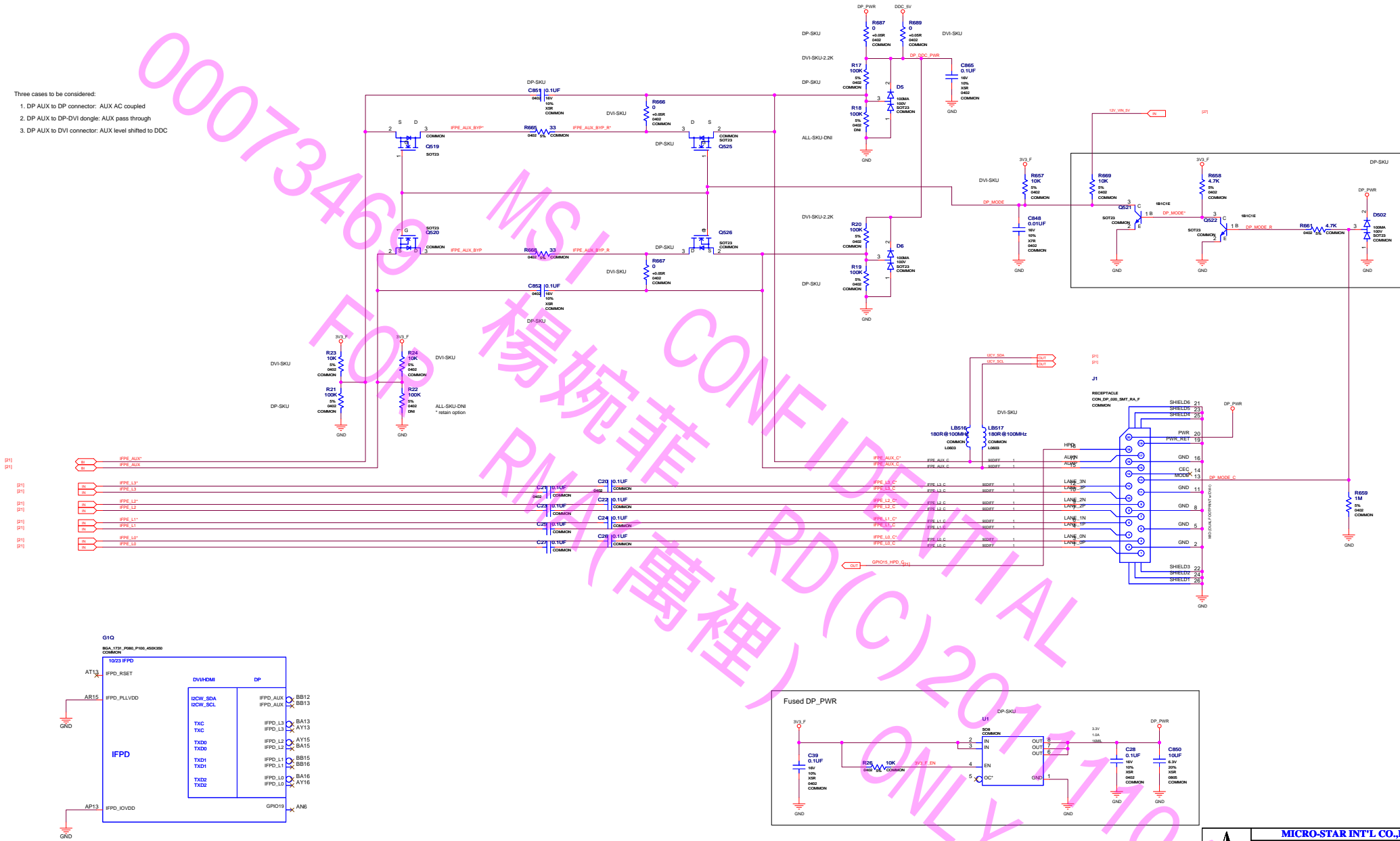


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- Three cases to be considered:
- 1. DP AUX to DP connector: AUX AC coupled
  - 2. DP AUX to DP-DVI dongle: AUX pass through
  - 3. DP AUX to DVI connector: AUX level shifted to DDC

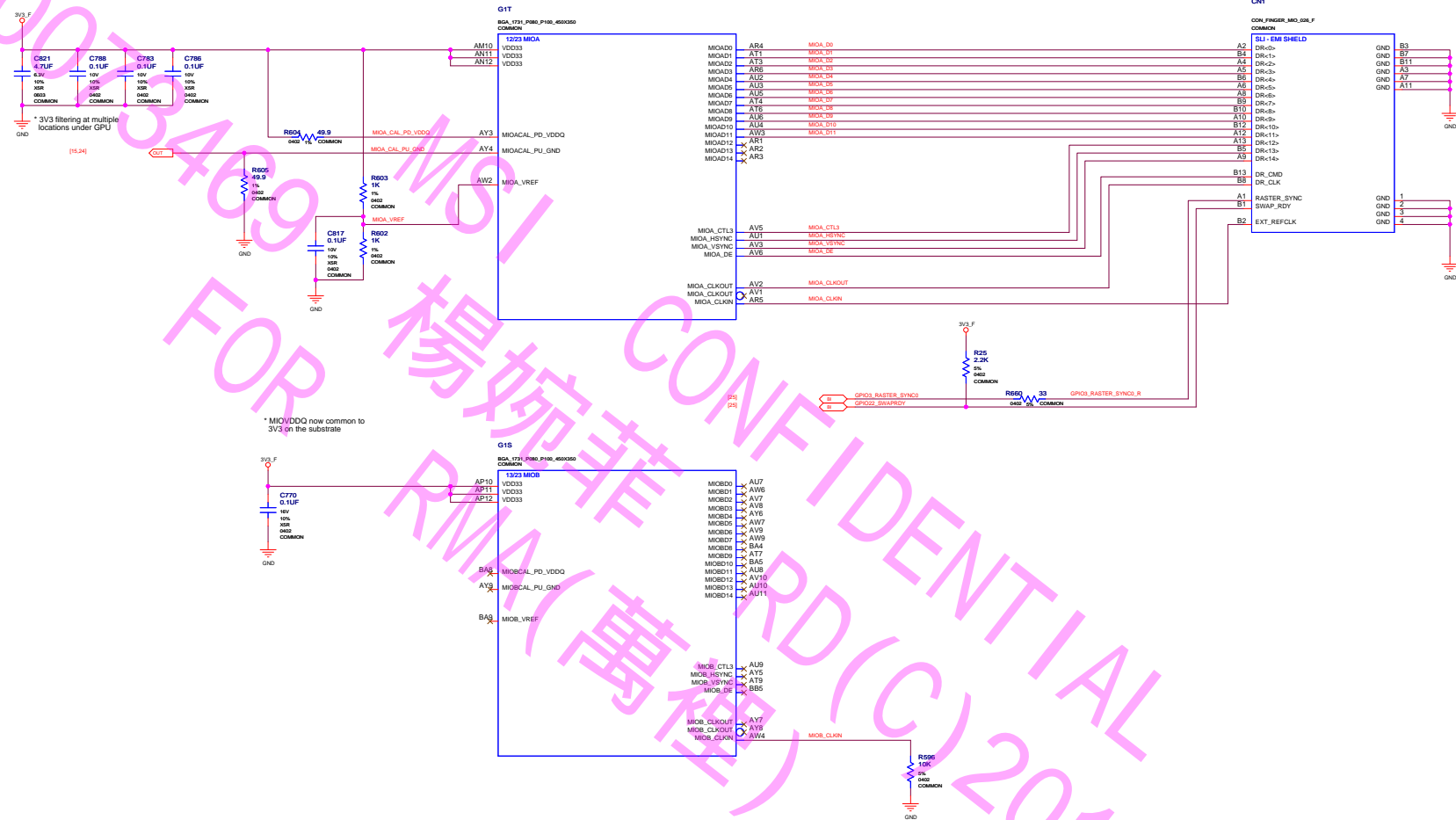


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#### MIO NET RULES

NET NV\_CRITICAL NV\_IMPEDANCE DIFFPAIR

NET	VOLTAGE	MIN_WIDTH
MIOA_CAL_PU_GND	0.0V	8MIL

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# Page26: Misc: ROM, HDCP, XTAL, Straps

STRAP0	USER_BIT [3..0]	0000 => 5K PD	
STRAP1	3GIO_PADCFG_LUT_ADR	0000 =>5K PD	0000 Desktop
STRAP2	PCI_DEVID [3..0]	0010 For 0x0E22 => 15K PD 0100 For 0x0E24 => 25K PD	
ROM_SI	RAMCFG[0]	<small>32Mx32 256-bit Samsung for SKU 10 first memory 0011 PD 20K 32Mx32 256-bit Hynix for SKU 10 2nd memory 0110 PD 10K</small>	
	RAMCFG[1]		
	RAMCFG[2]	<small>32Mx32 192-bit Samsung for SKU 0 first memory 1011 PD 20K 32Mx32 192-bit Hynix for SKU 0 2nd memory 1110 PD 10K</small>	
	RAMCFG[3]		
ROM_SO	VGA_DEVICE	1	
	SMB_ALT_ADDR	0	10k PD
	FB[0]_BAR_SIZE	0	
ROM_SCLK	XCLK_417	0	
	PEX_PLL_EN_TERM100	1 ENABLED	
	SLOT_CLK_CFG	1 ENABLE	
	SUB_VENDOR	1 Dedicated BIOS	45K PD
	PCI_DEVID_EXT	0 0xC	

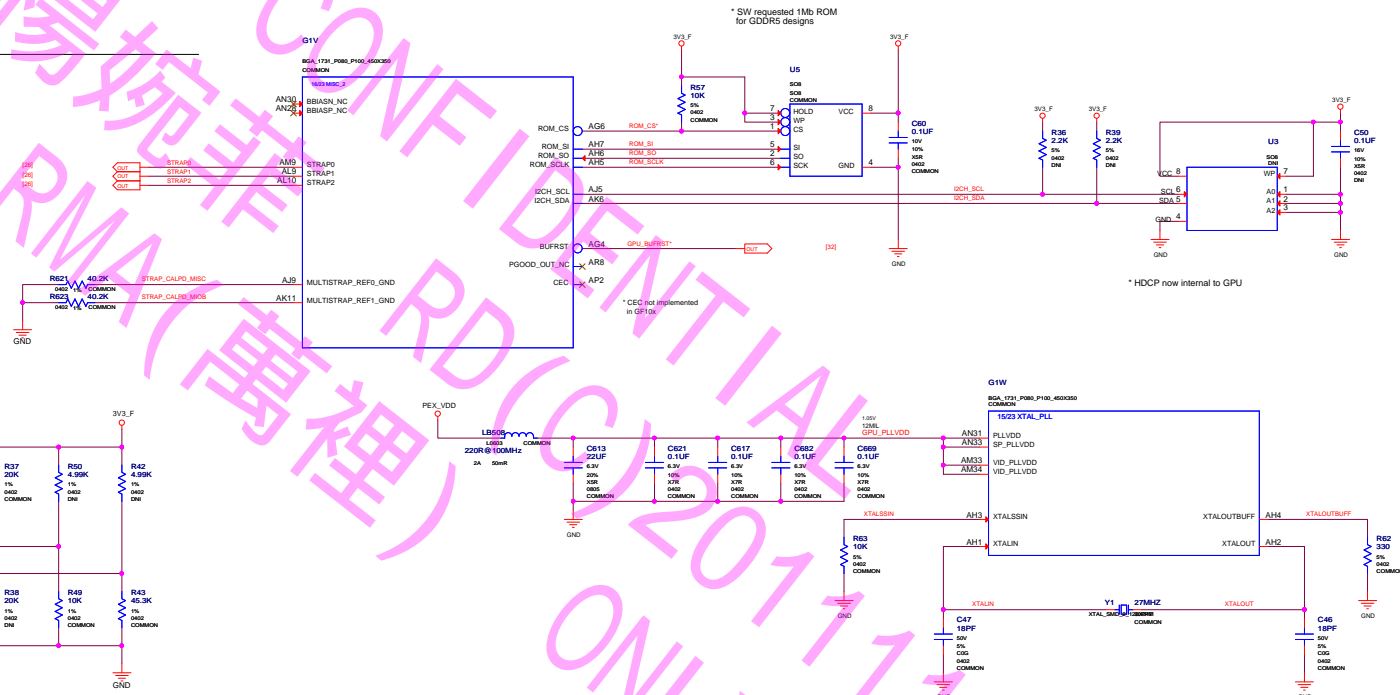
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3..0] Config Width	Vendor
0000	Reserved
0001	32Mx32 256-bit Qimonda
0010	32Mx32 256-bit Hynix
0011	32Mx32 256-bit Samsung
0100	Reserved
0101	64Mx32 256-bit Qimonda
0110	64Mx32 256-bit Hynix
0111	64Mx32 256-bit Samsung
1000	Reserved
1001	32Mx32 192-bit Qimonda
1010	32Mx32 192-bit Hynix
1011	32Mx32 192-bit Samsung
1100	Reserved
1101	64Mx32 192-bit Qimonda
1110	64Mx32 192-bit Hynix
1111	64Mx32 192-bit Samsung

## MISC NET RULES

NET NV\_CRITICAL NV\_IMPEDANCE

	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	45.2k 1% TO GND	NC
BINARY BRINGUP	NC	NC
MULTI-LEVEL	45.2k 1% TO GND	45.2k 1% TO GND





[illegible]

1nd: 041-0147-000  
2nd: 042-0087-000

Vref=0.8V  
Vo\_Typ=0.8\*(1+1.02/(1.47//5.76))=1.497V  
Vo\_Typ=0.8\*(1+1.02/1.47)=1.355V

FBVDD/Q	GPIO23
1.35V	0
1.5V	1

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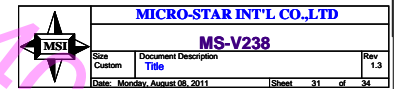


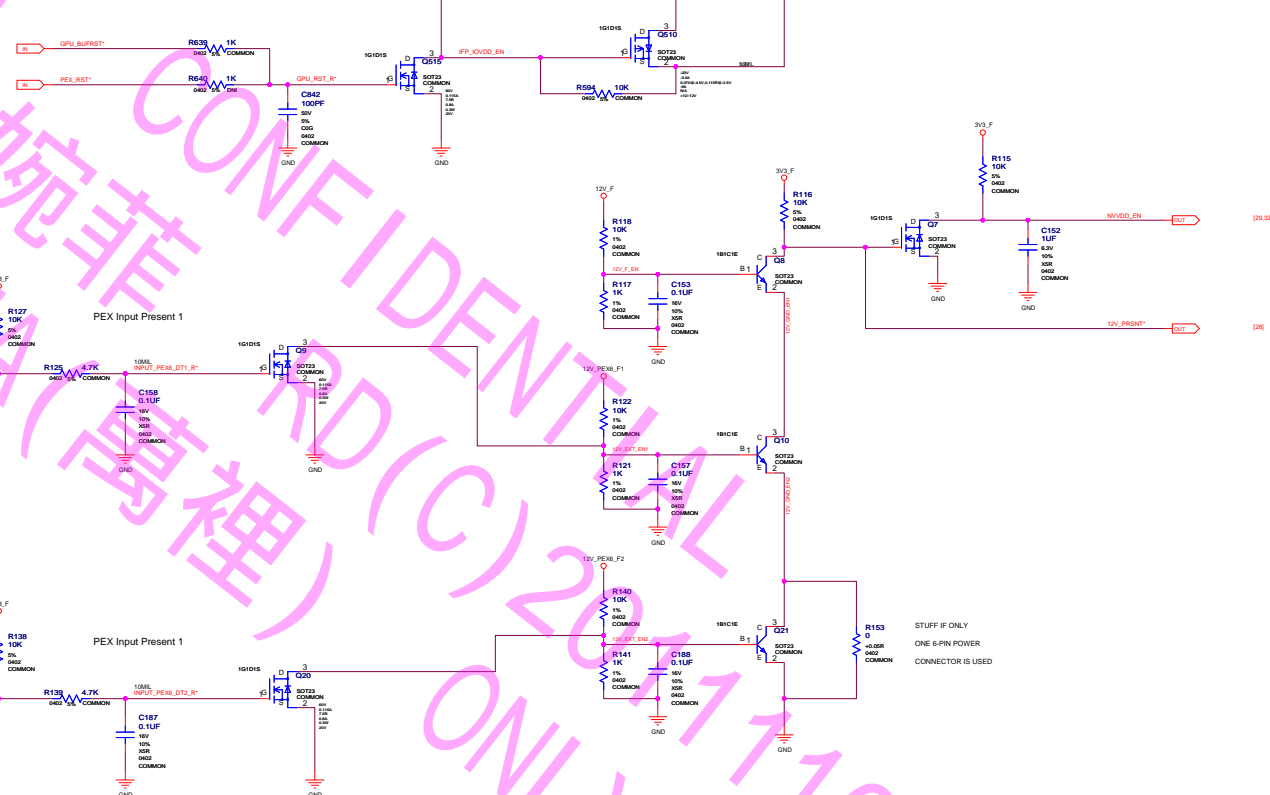
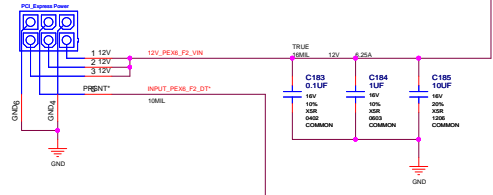
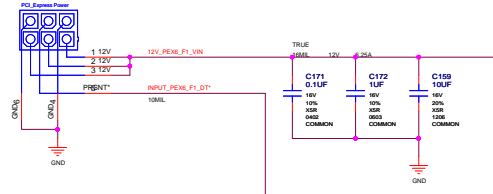
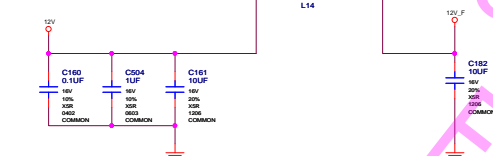
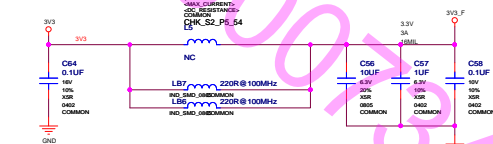


1nd: 041-0147-000  
2nd: 042-0087-000



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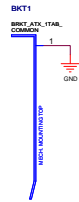


STUFF IF ONLY  
ONE 6-PIN POWER  
CONNECTOR IS USED

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Brackets:

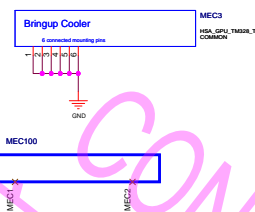
Bracket with DVI\_DP\_mHDMI: 151-10001-0355-071



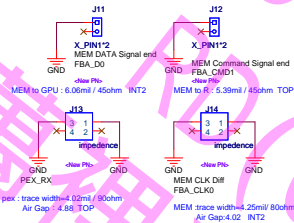
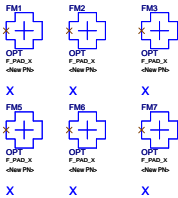
Bracket Screw



Cooler/GPU Stiffener



remove mec1



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