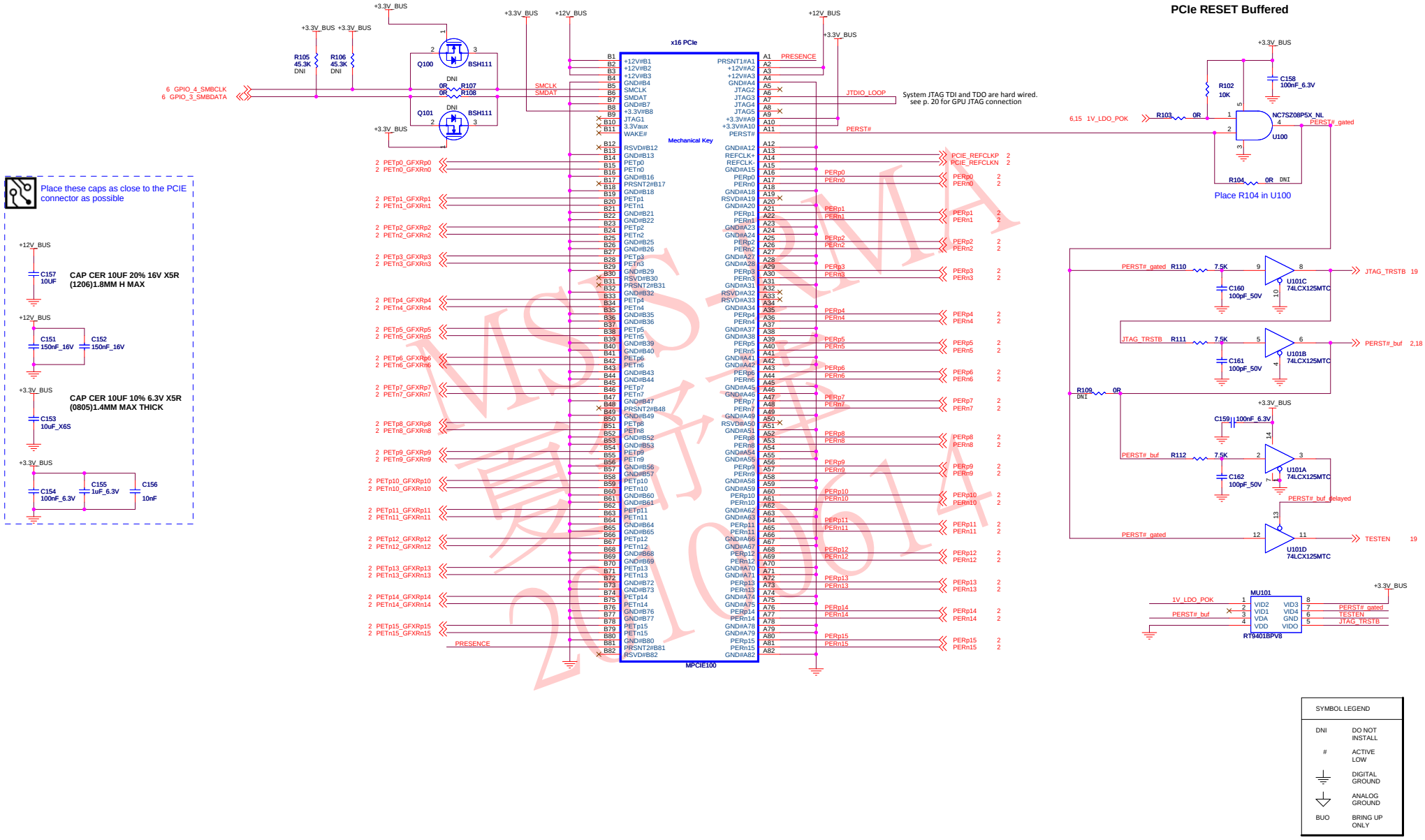
PCI-EXPRESS EDGE CONNECTOR

CORVETTE



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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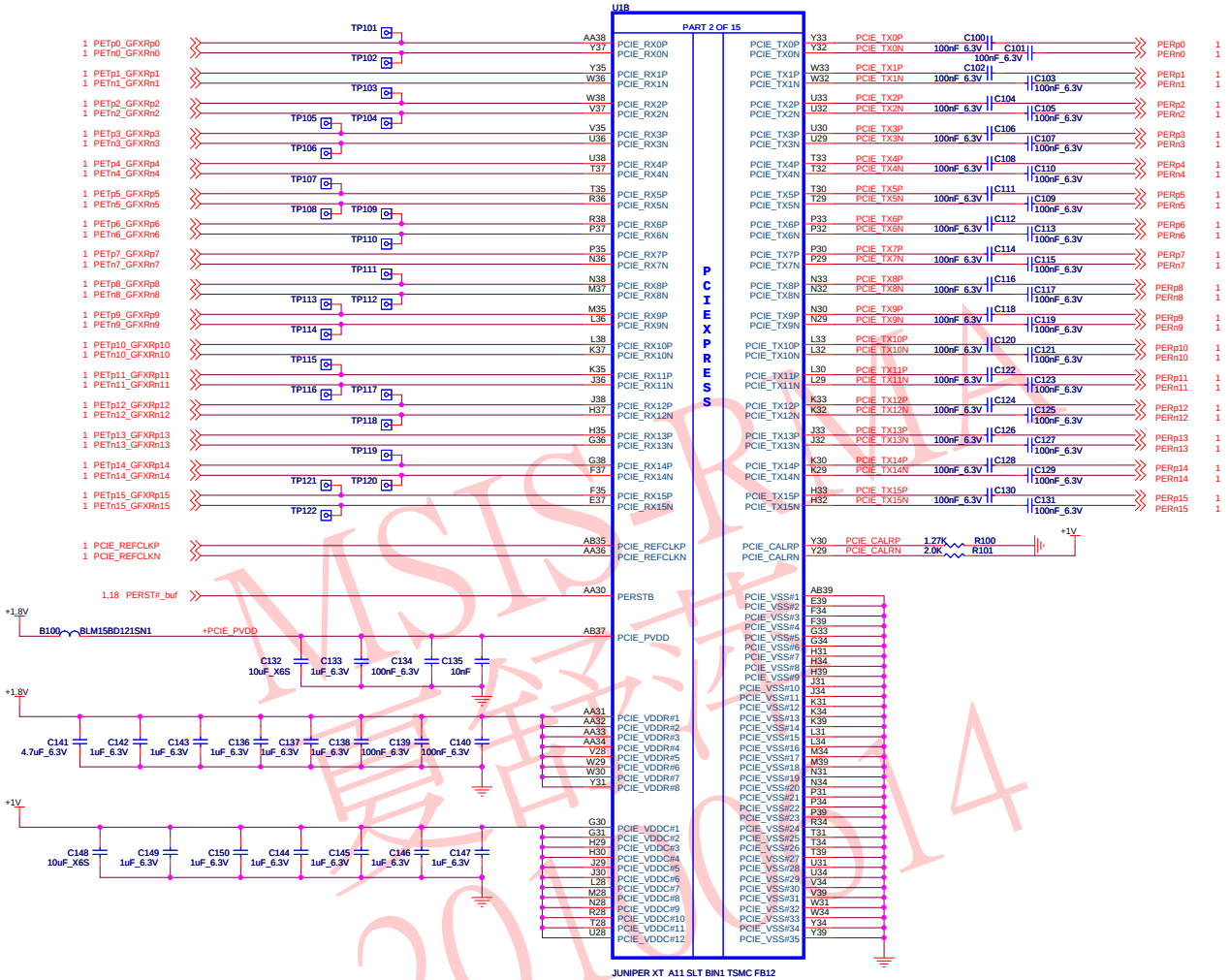
(2) JUNIPER PCIe Interface

NOTE: Some of the PCIE testpoints will be available through vias on traces.



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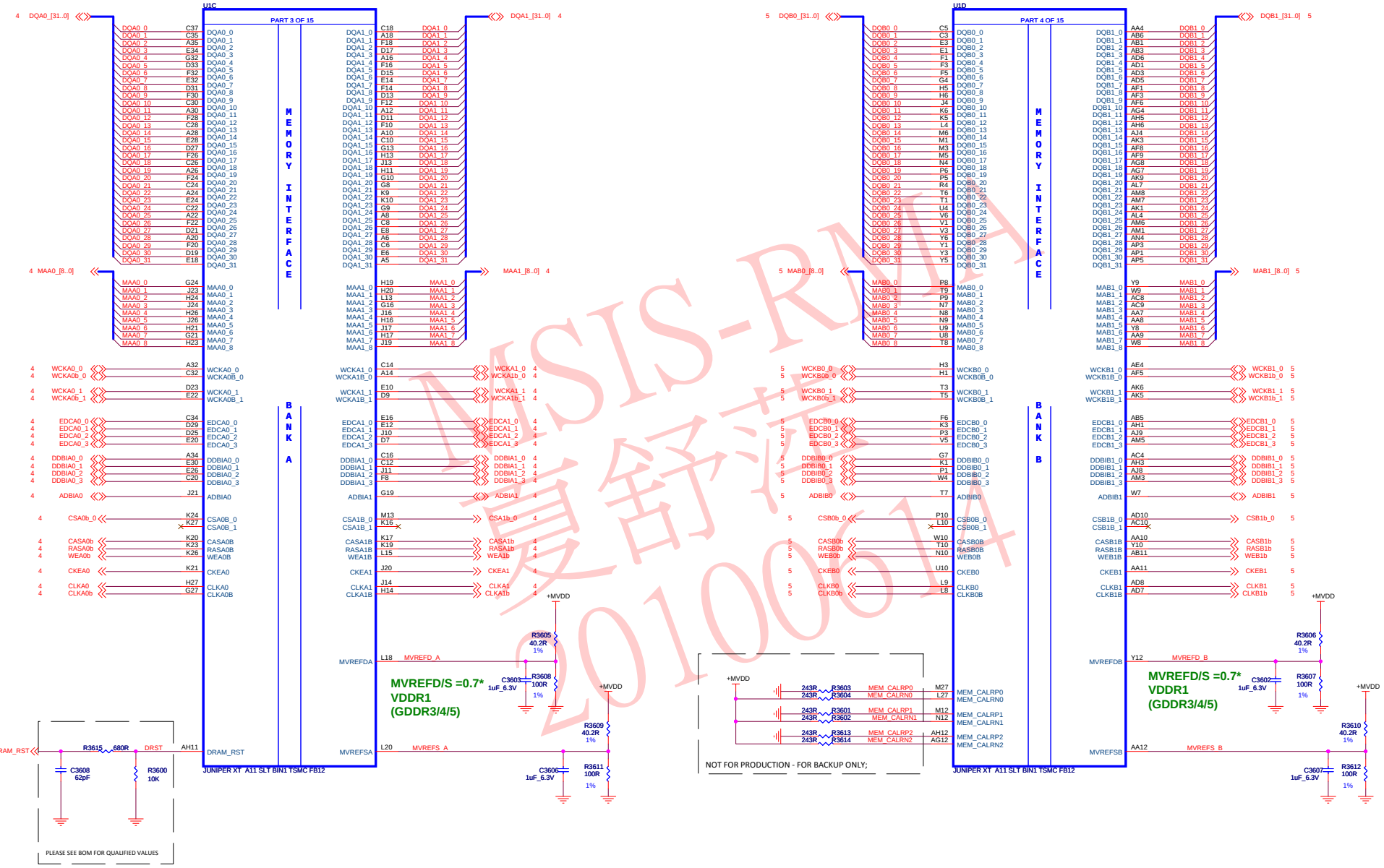
(3) JUNIPER MEM Interface Ch A&B



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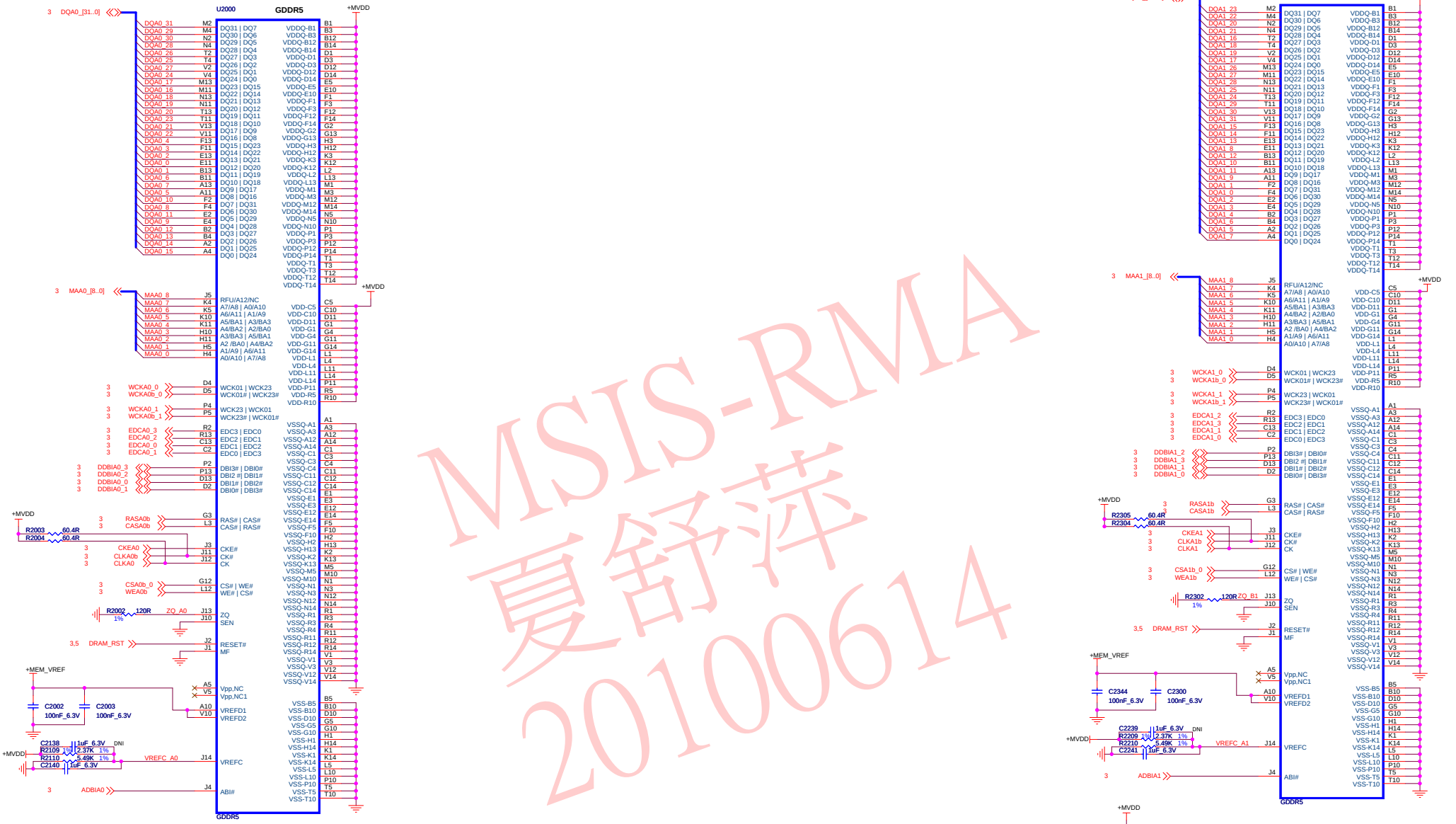
(4) GDDR5 x32 MEM Channel A

CH_A0 =U2000 & U2100

CH_A1 =U2200 & U2300



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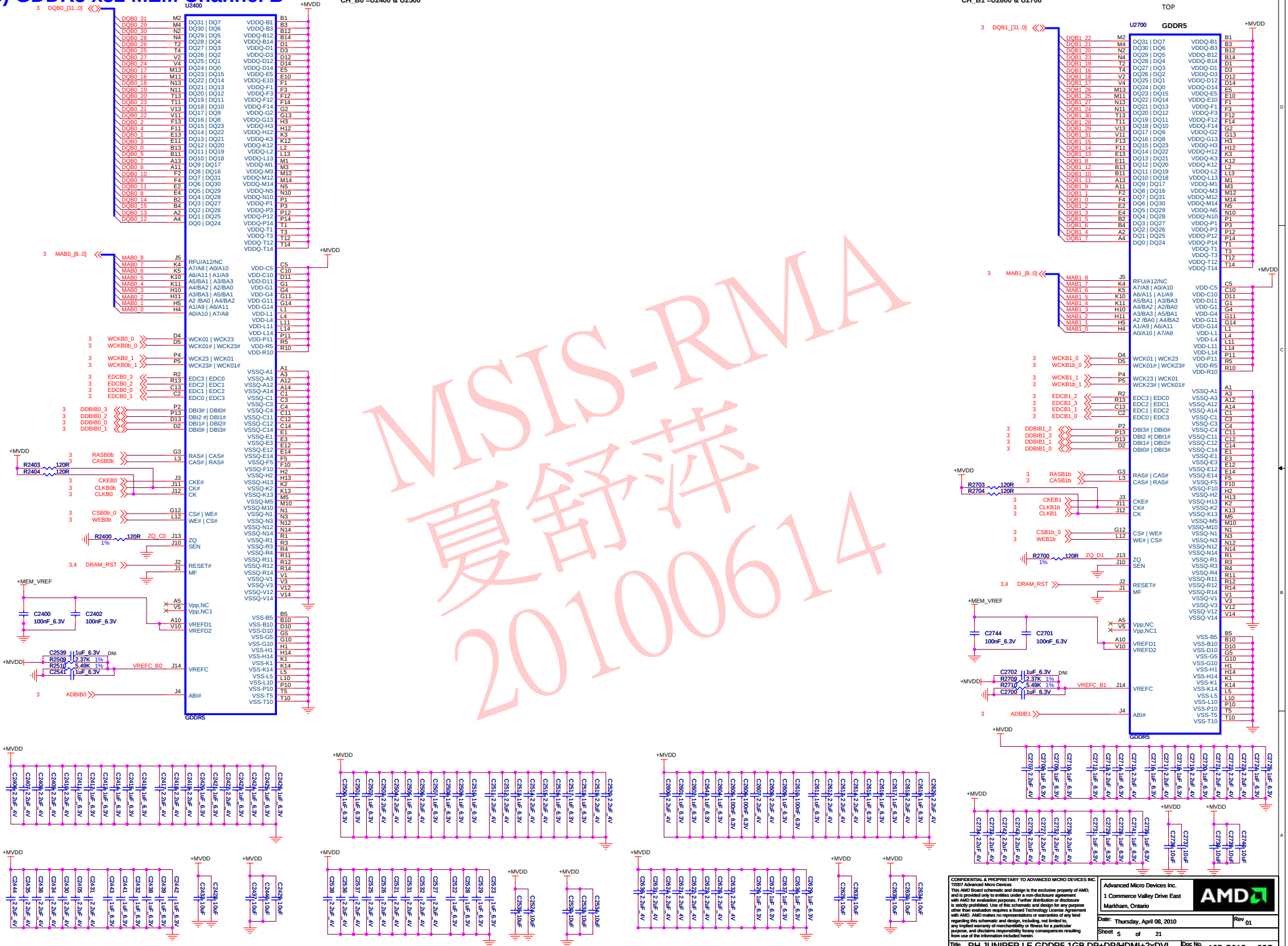
(5) GDDR5 x32 MEM Channel B

CH_B0 =U2400 & U2500

CH_B1 =U2600 & U2700

TOP



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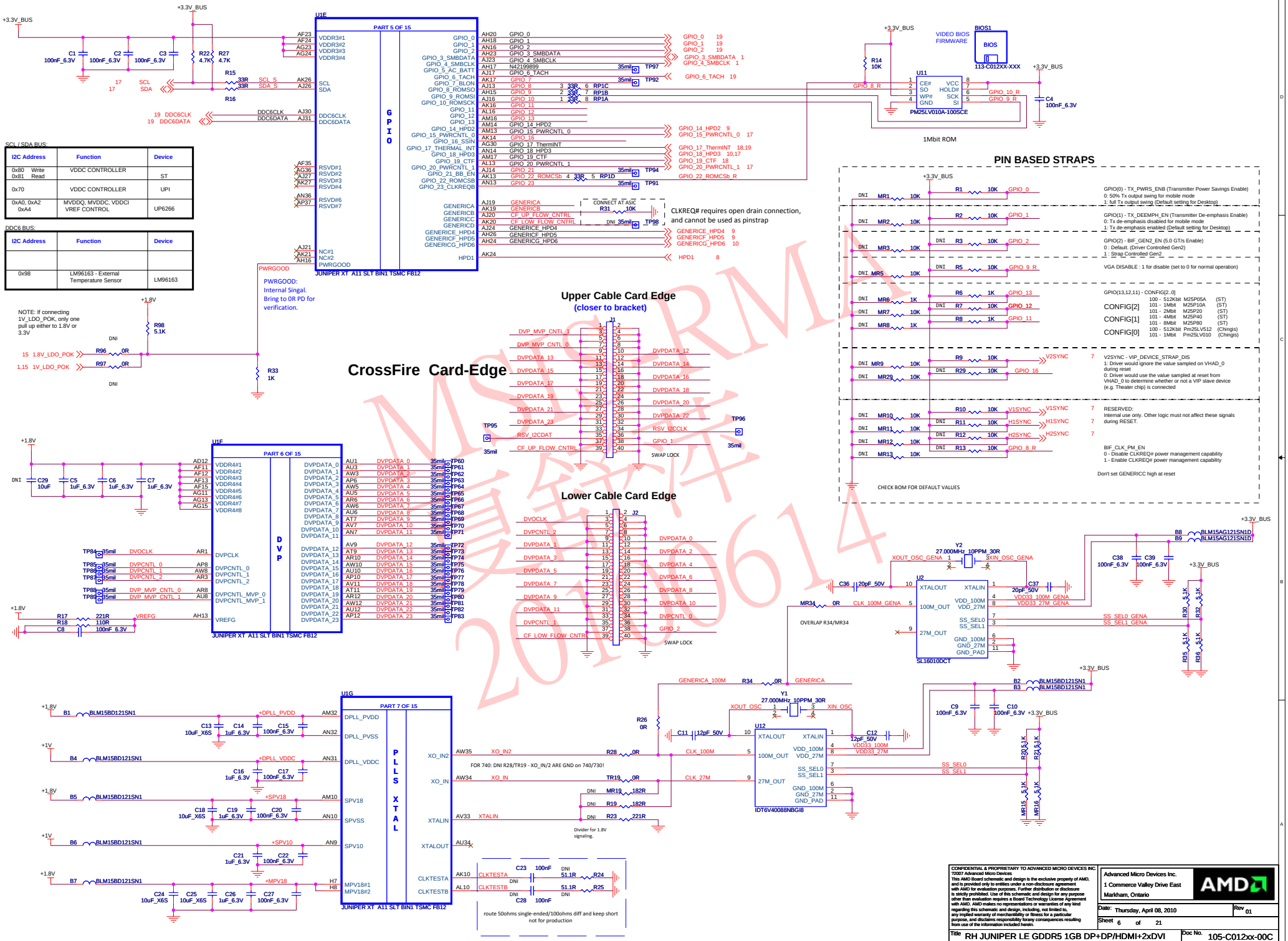
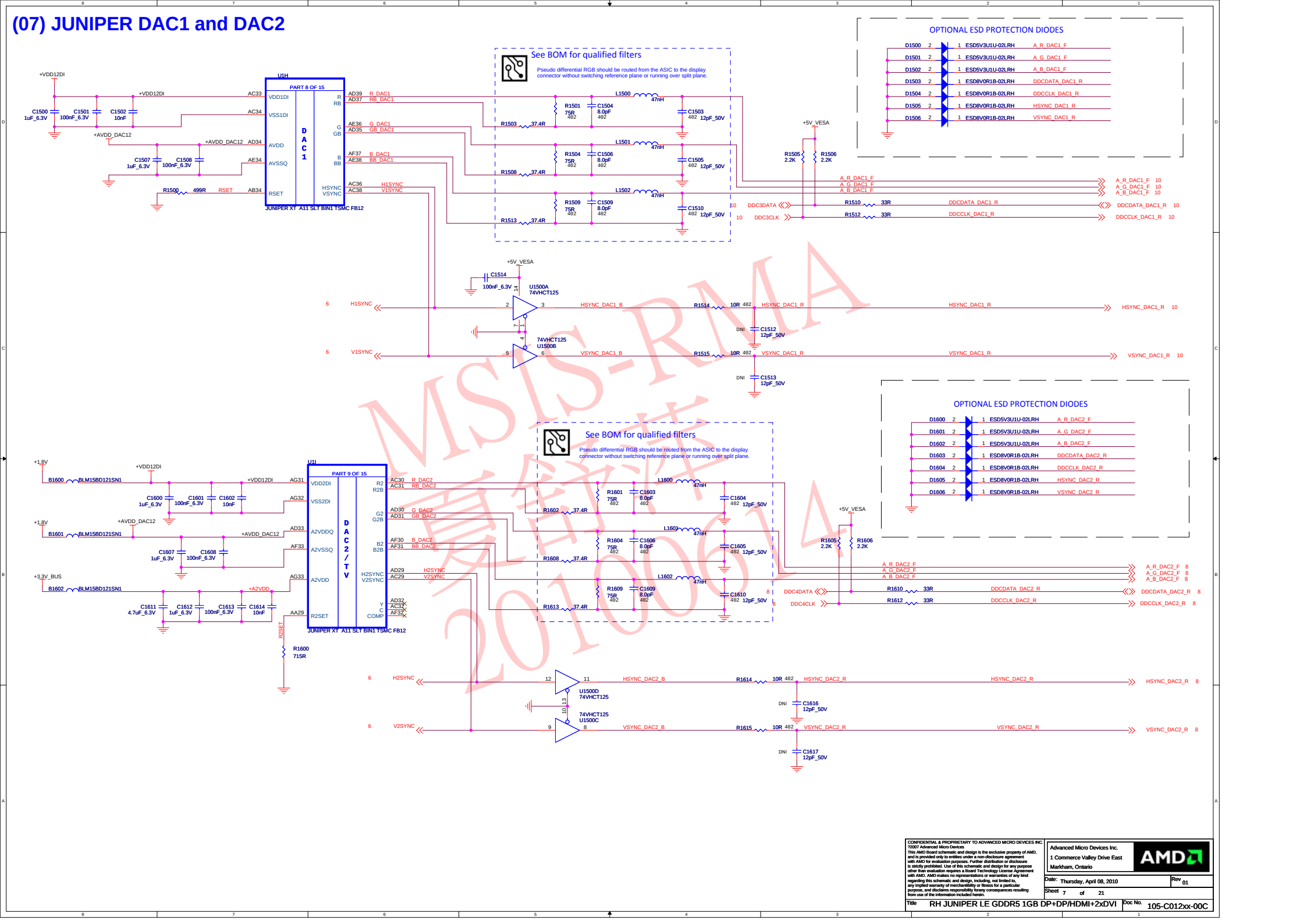
(06) JUNIPER GPIOs Strap CF XTAL OSC



(07) JUNIPER DAC1 and DAC2



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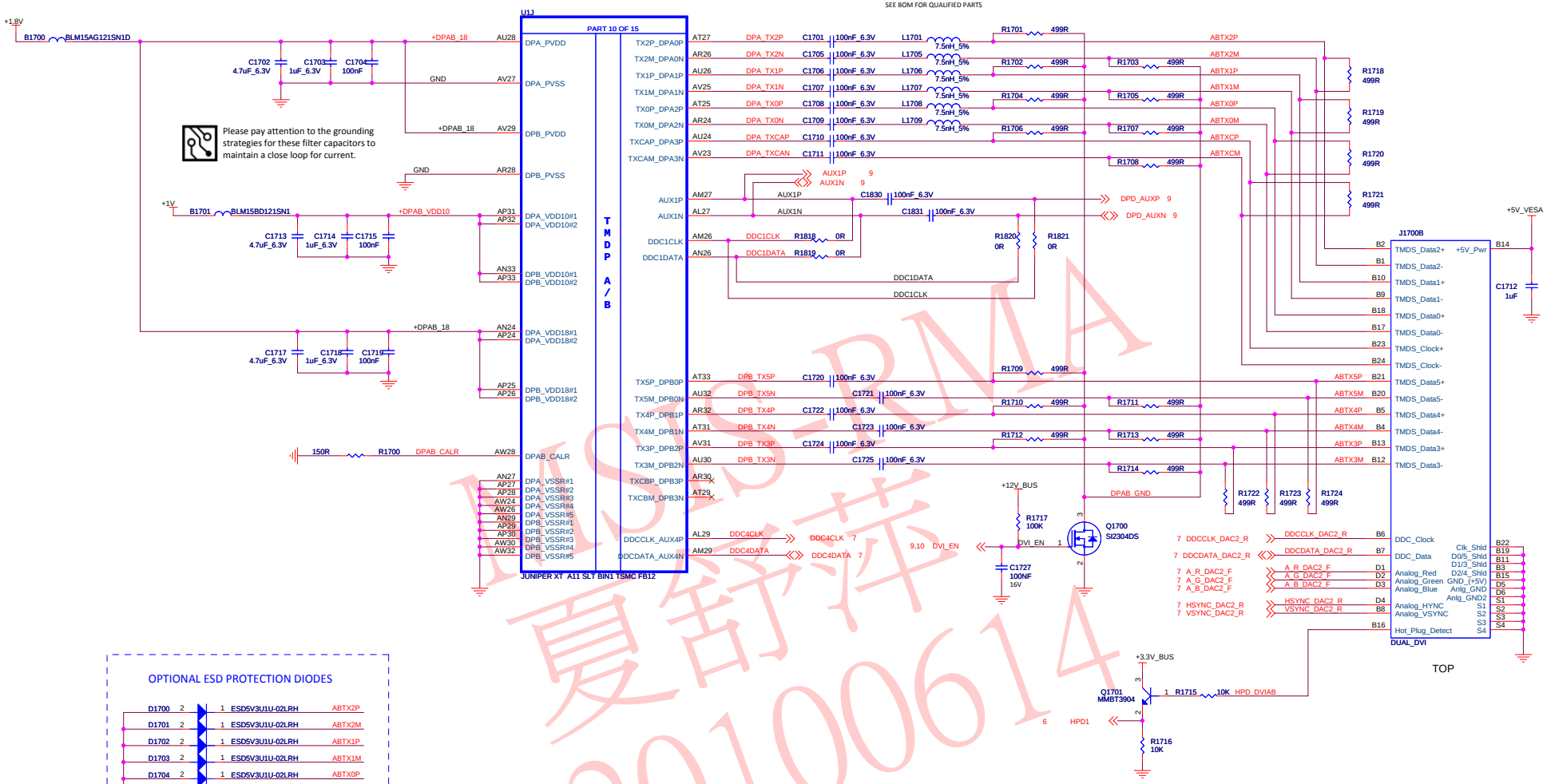
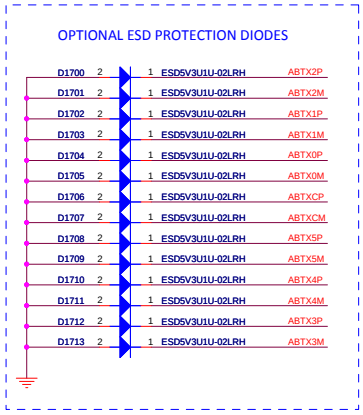
(08) JUNIPER TMDP A&B dDVI-I TOP





ASSY-SCREW1700

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

7020000800G

ASSY-SCREW1701

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

7020000800G

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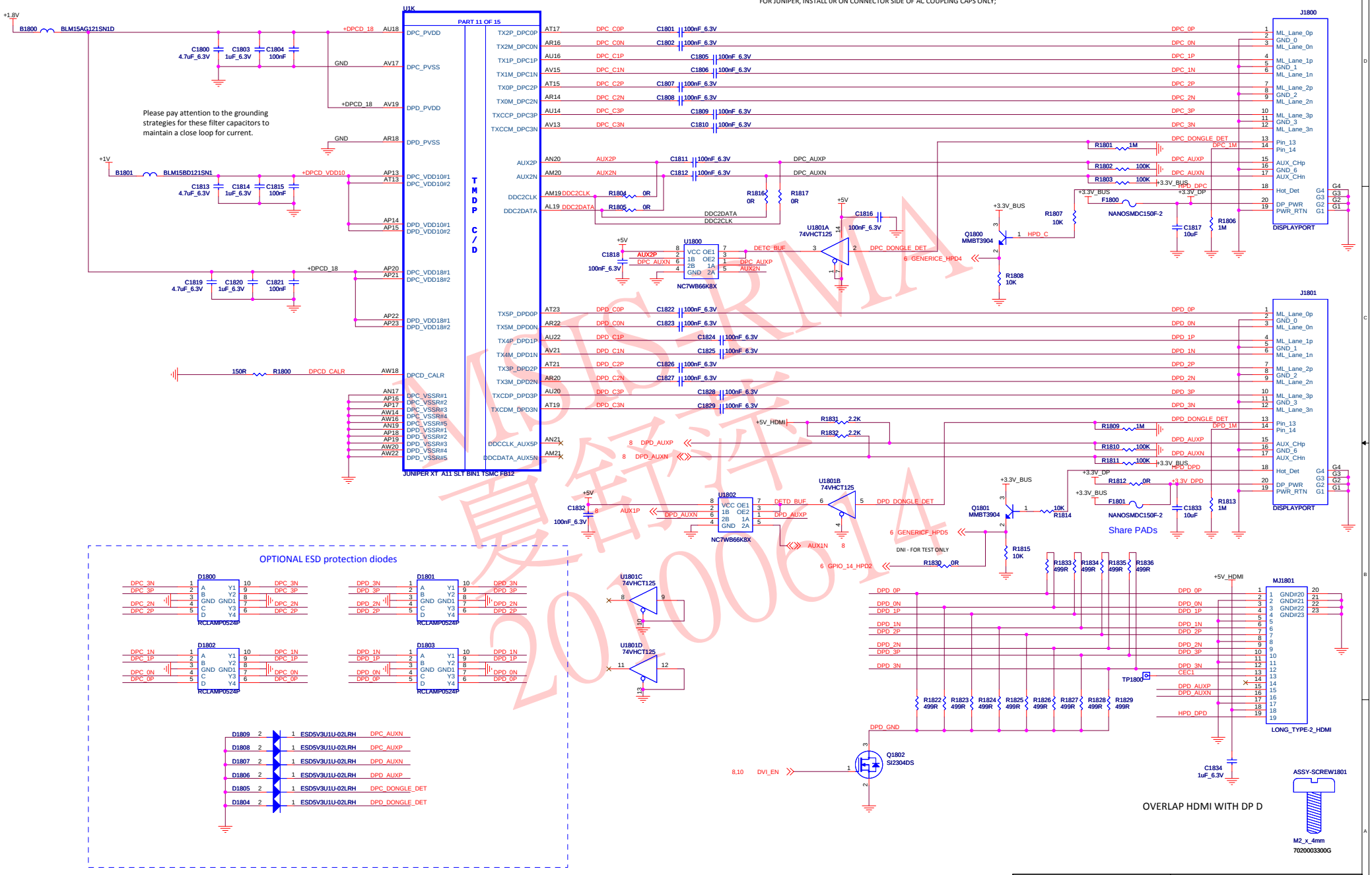
(09) JUNIPER Display Port C & Display Port/HDMI D



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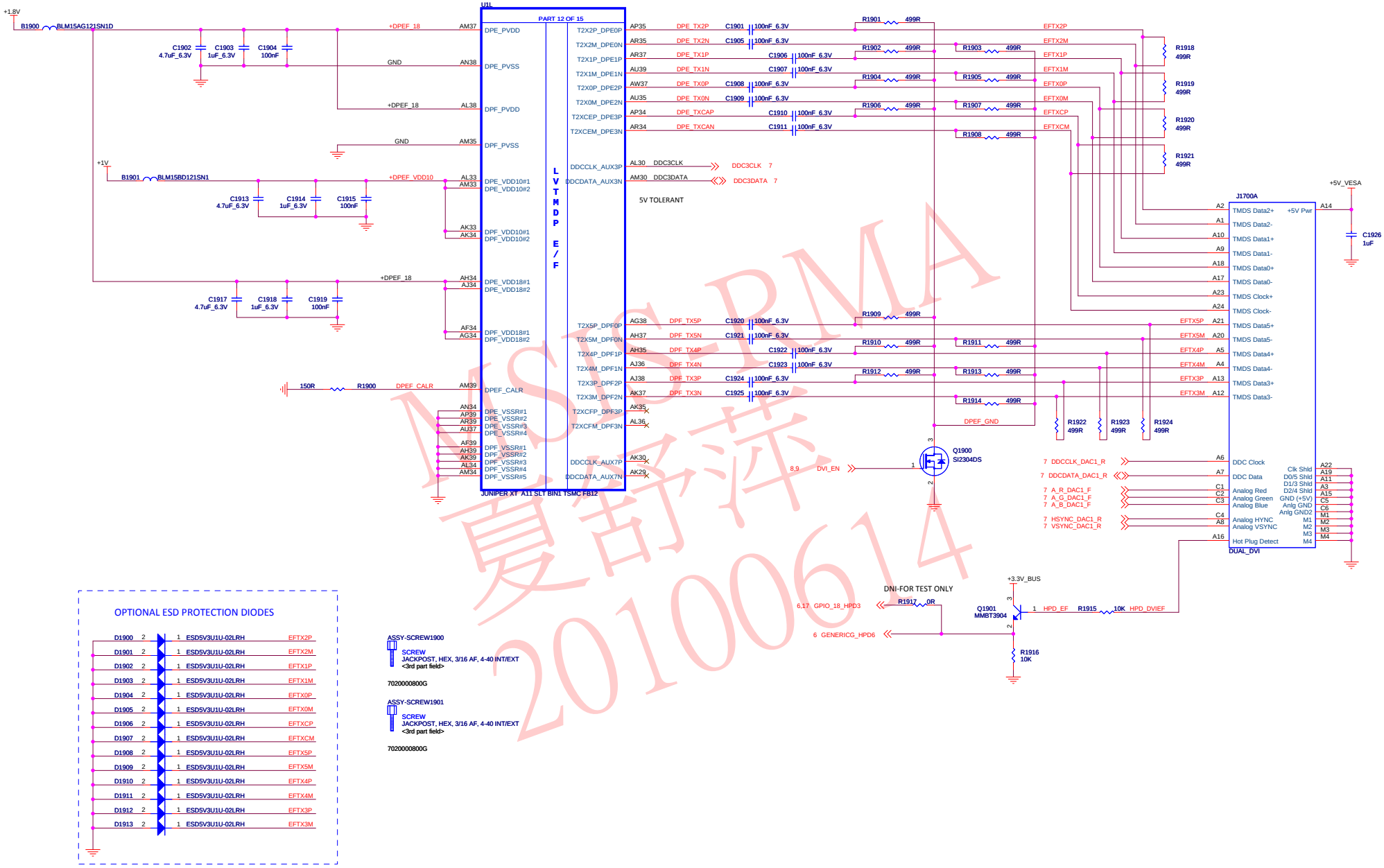
(10) JUNIPER LVTMDP E&F dDVI-I BOTTOM



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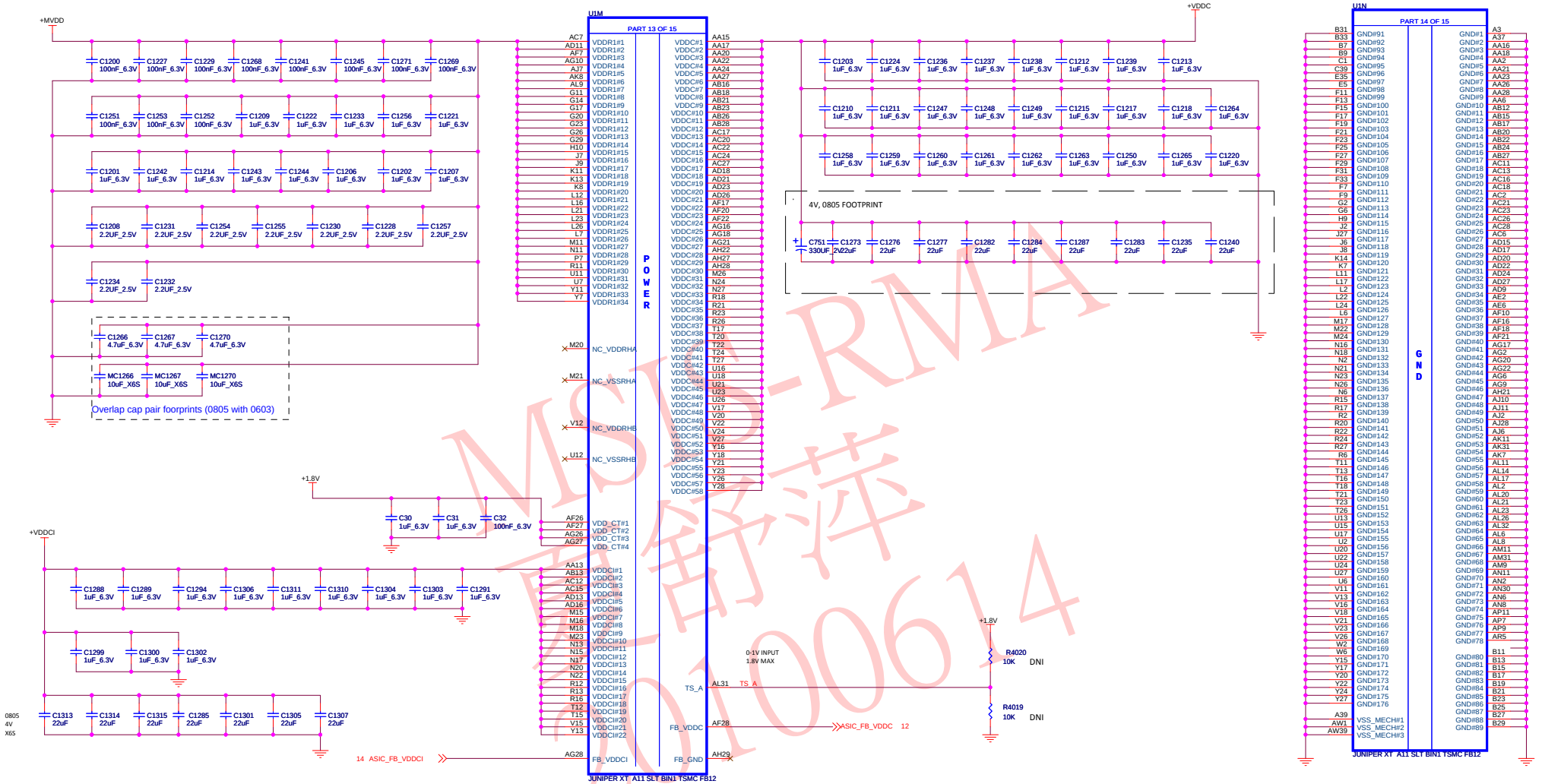
(11) JUNIPER Power & GND



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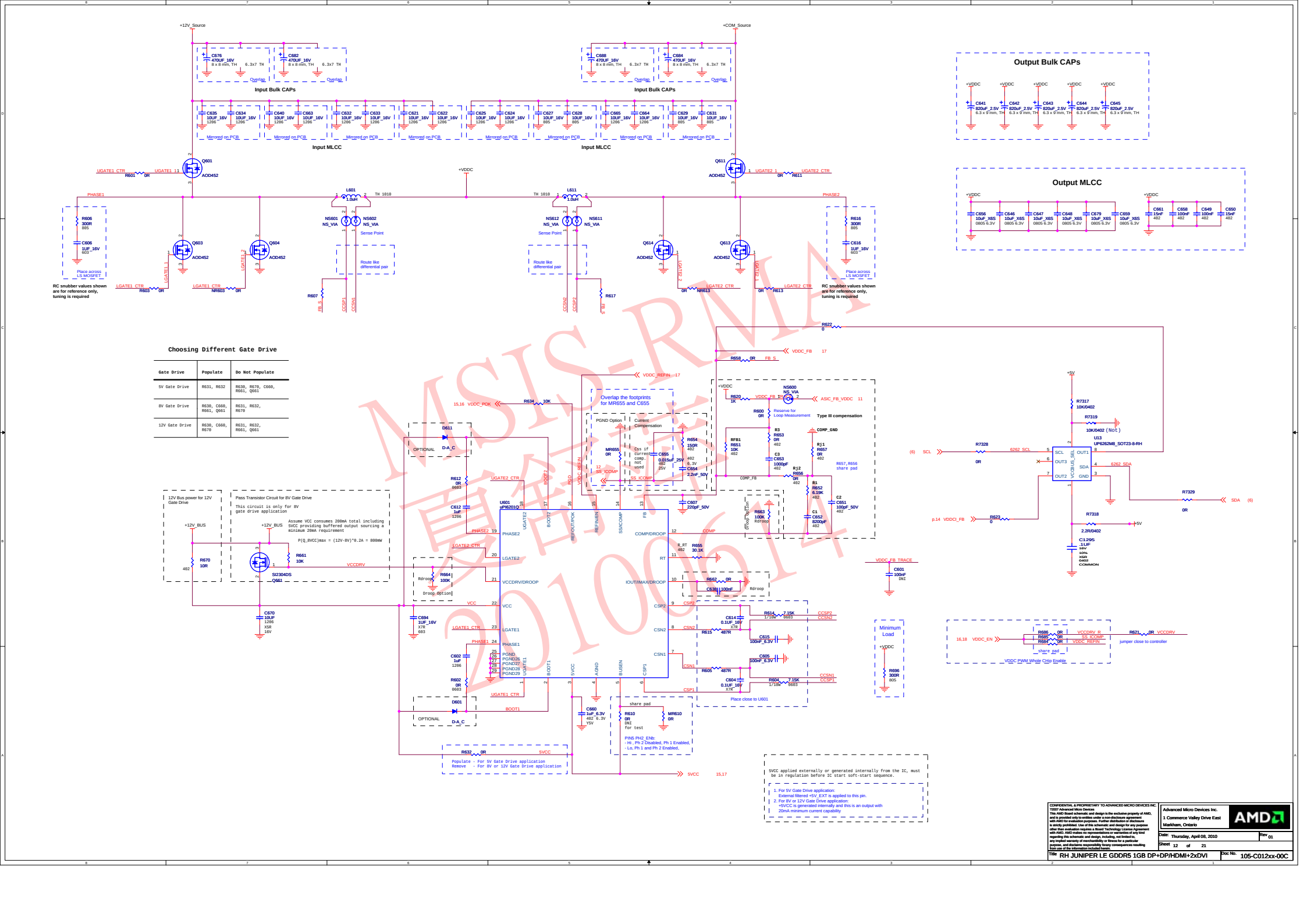
Output Bulk CAPs
Output MLCC
Input Bulk CAPs
Input MLCC
Choosing Different Gate Drive
Gate Drive | Populate | Do Not Populate
5V Gate Drive | R631, R632 | R630, R670, C660, R661, Q661
8V Gate Drive | R630, C660, R661, Q661 | R631, R632, R670
12V Gate Drive | R630, C660, R661, Q661 | R631, R632, R661, Q661
RC snubber values shown are for reference only, tuning is required
Overlap the footprints for MR655 and C655
Type III compensation
Minimum Load
Place close to U601
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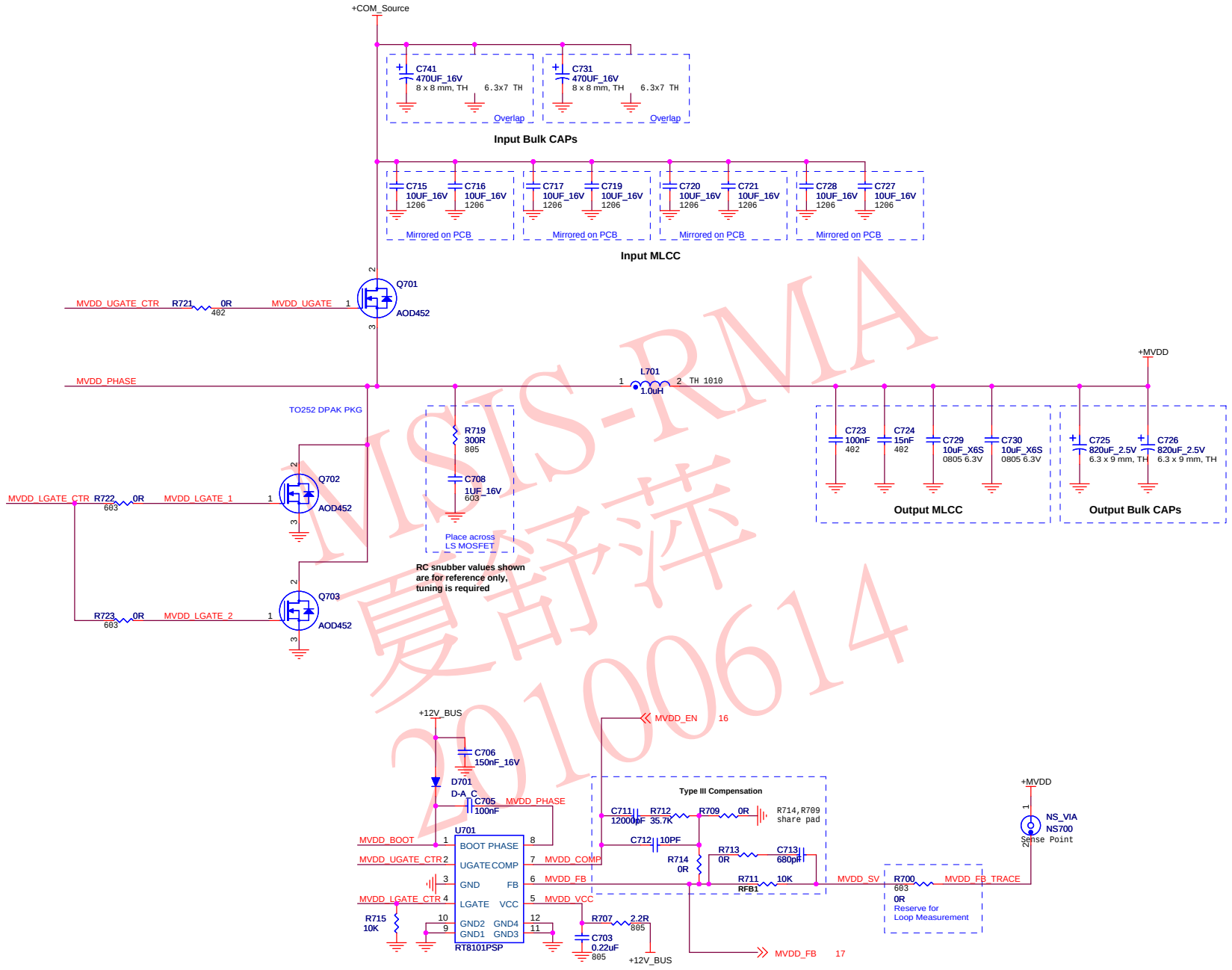

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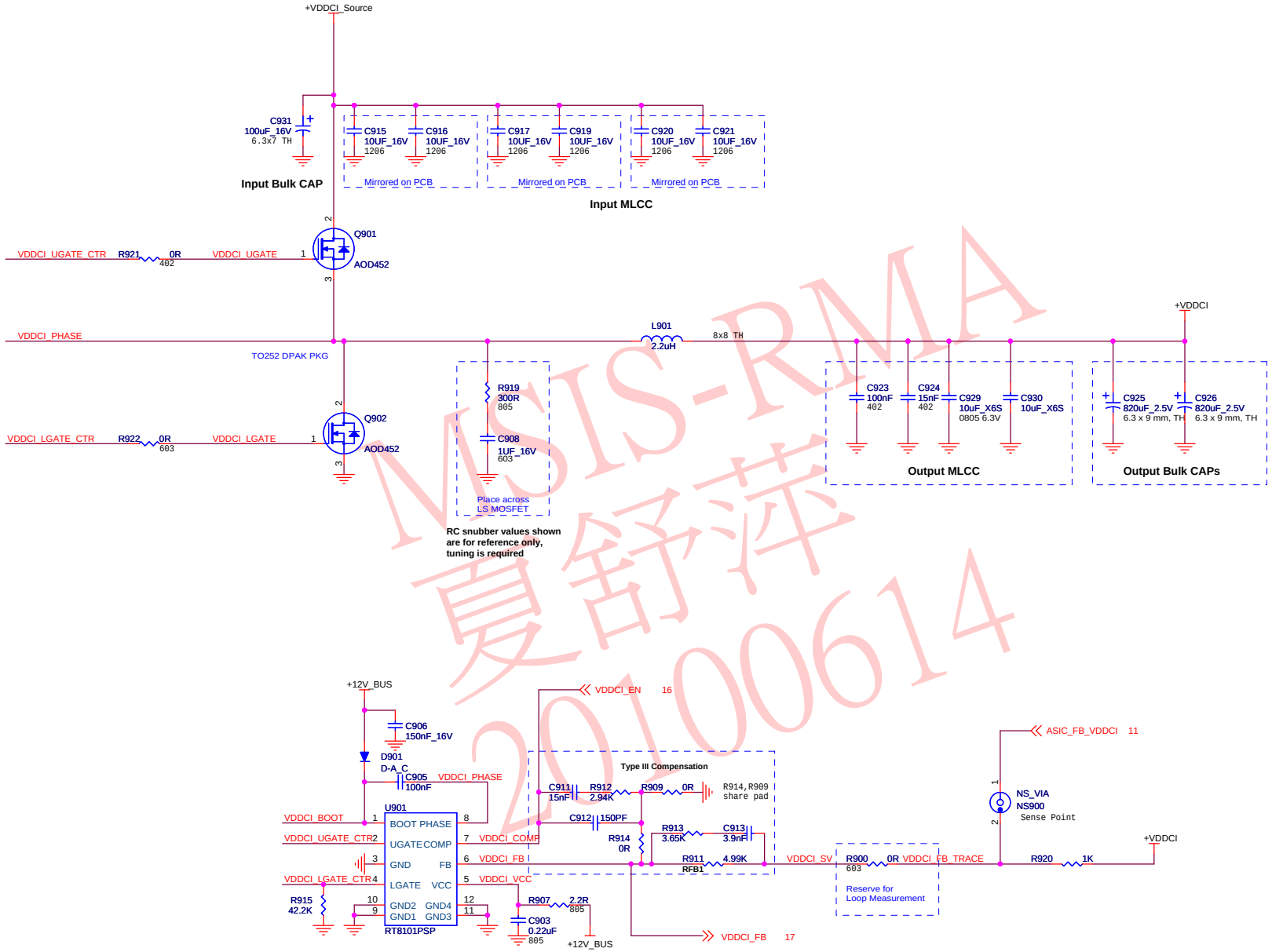

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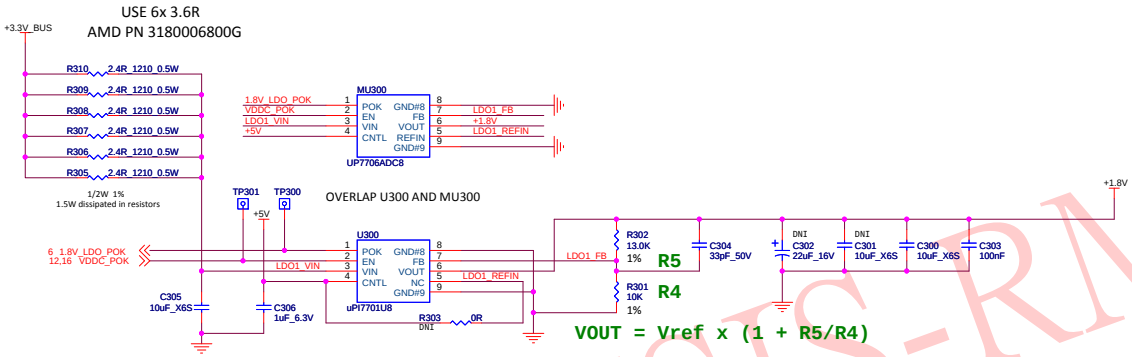
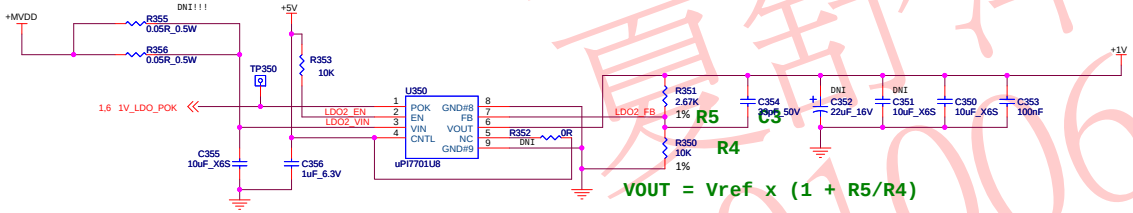
(15) Linear Regulators

Regulators for +5V, +5V_VESA and +5V_HDMI

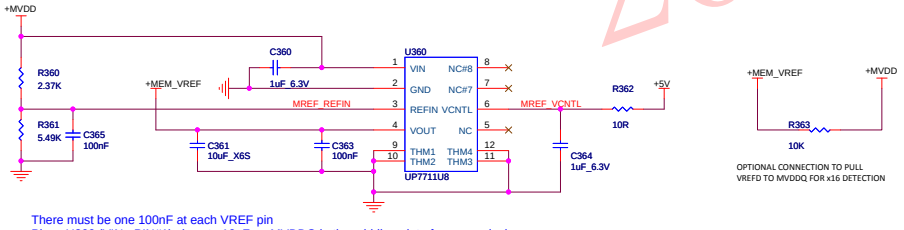
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



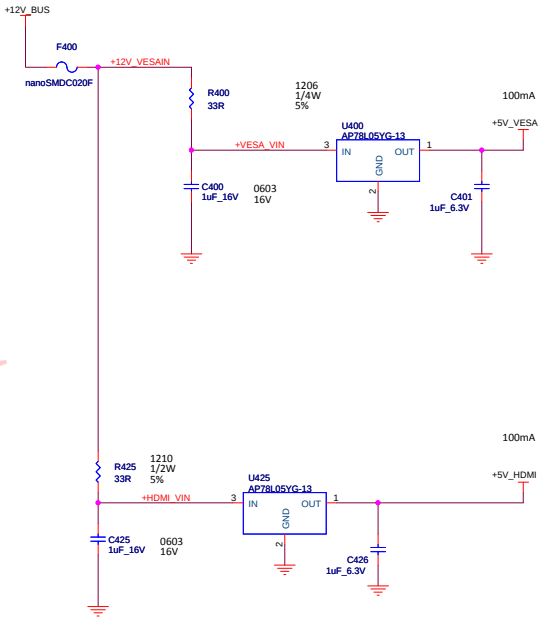
LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

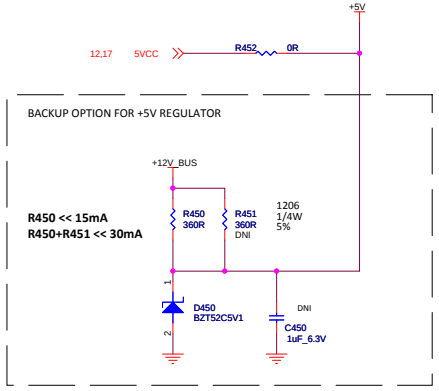


Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ



There must be one 100nF at each VREF pin
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices





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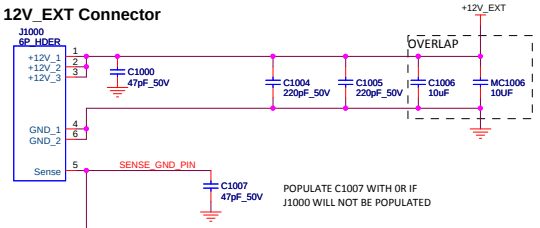
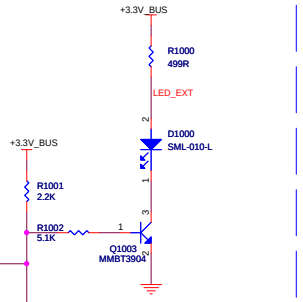
(16) Power Management - Power Gating and External Power Detect

12V_EXT Connector

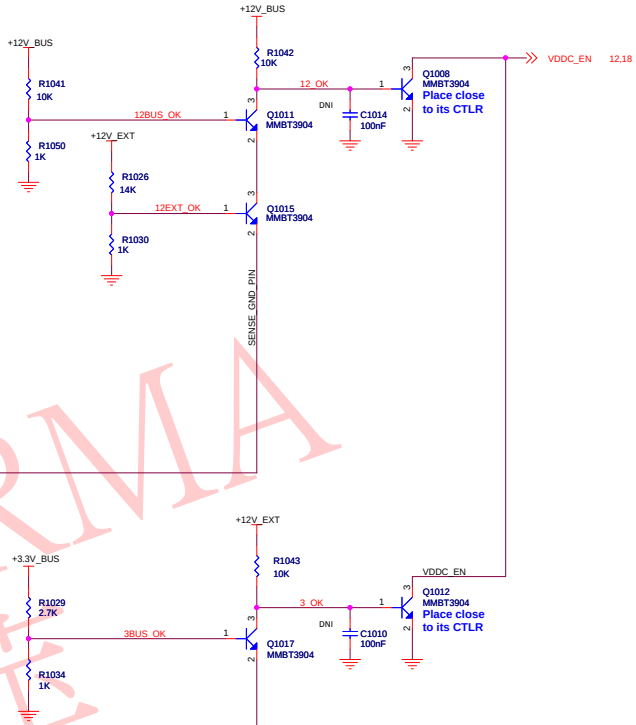


OPTIONAL LED

(LED " ON" indicates 12V_EXT power is not connected)
(client request only)

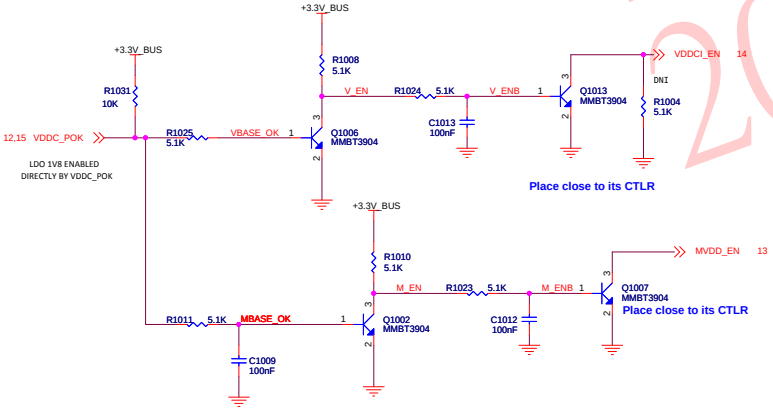


12V_BUS, 12V_EXT & 3V3_BUS POWER SEQUENCING



POWER SEQUENCING CIRCUIT

FOR MVDD & VDDCI
(ENABLES CANNOT BE SHARED SINCE IT IS ALSO THE COMPENSATION PIN OF THE SMPS REGULATOR)



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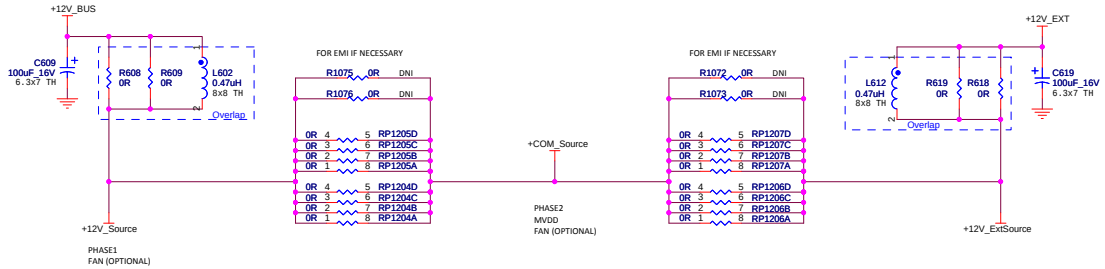
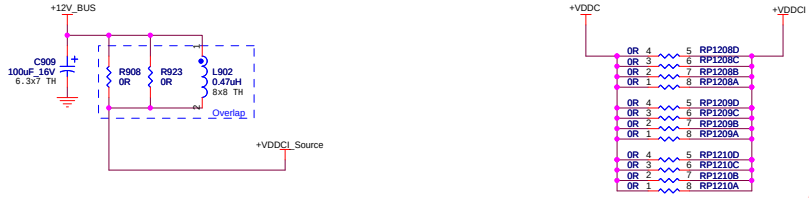
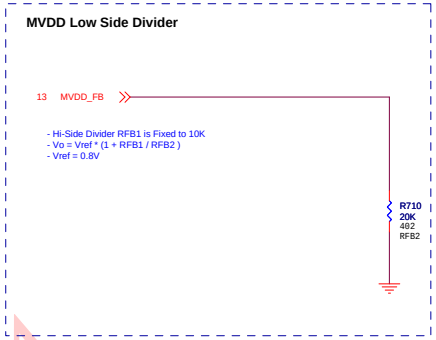
(18) Power Management 2

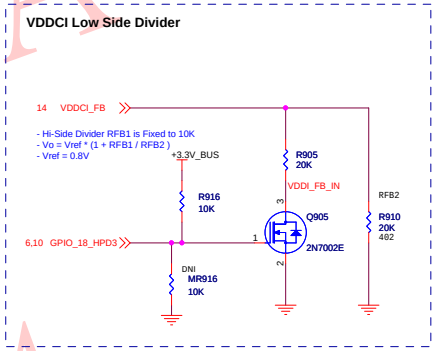




MVDD Low Side Divider

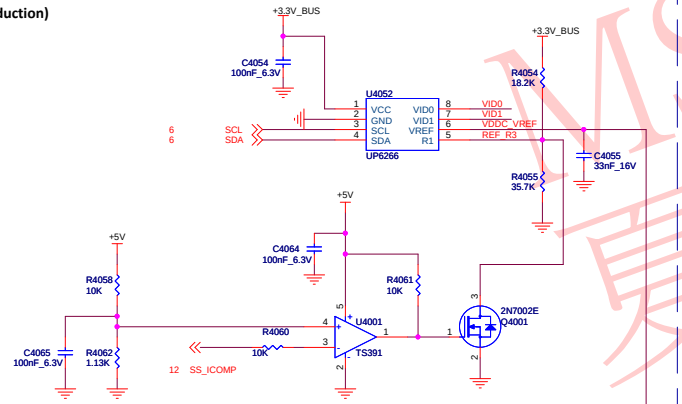


VDDCI Low Side Divider



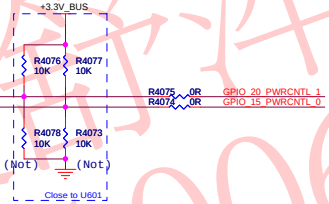
I2C VOLTAGE REFERENCE FOR VDDC (not for production)

I2C ADDRESS:
A4



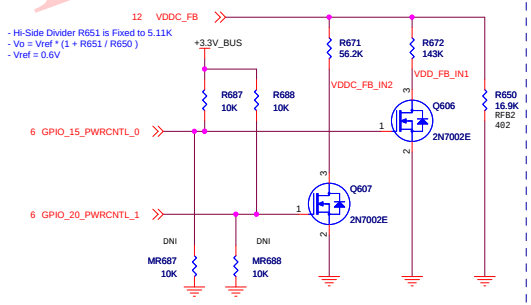
+VDDCi Voltage

GPIO18	Voltage	
0	0.999V	Idle and Video mode
1	1.1V	Boot and 3D mode

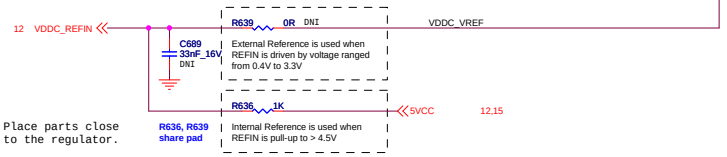


VDDC Low Side Divider

R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V.
Then this will set VDDC to a fixed value.



VDDC Reference Voltage Selection



VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

+VDDC Voltage

GPIO20	GPIO15	Voltage	
0	0	0.955V	Idle mode
0	1	0.997V	
1	0	1.061V	Video mode
1	1	1.1V	Boot and 3D mode

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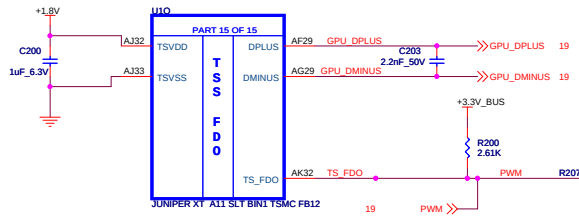
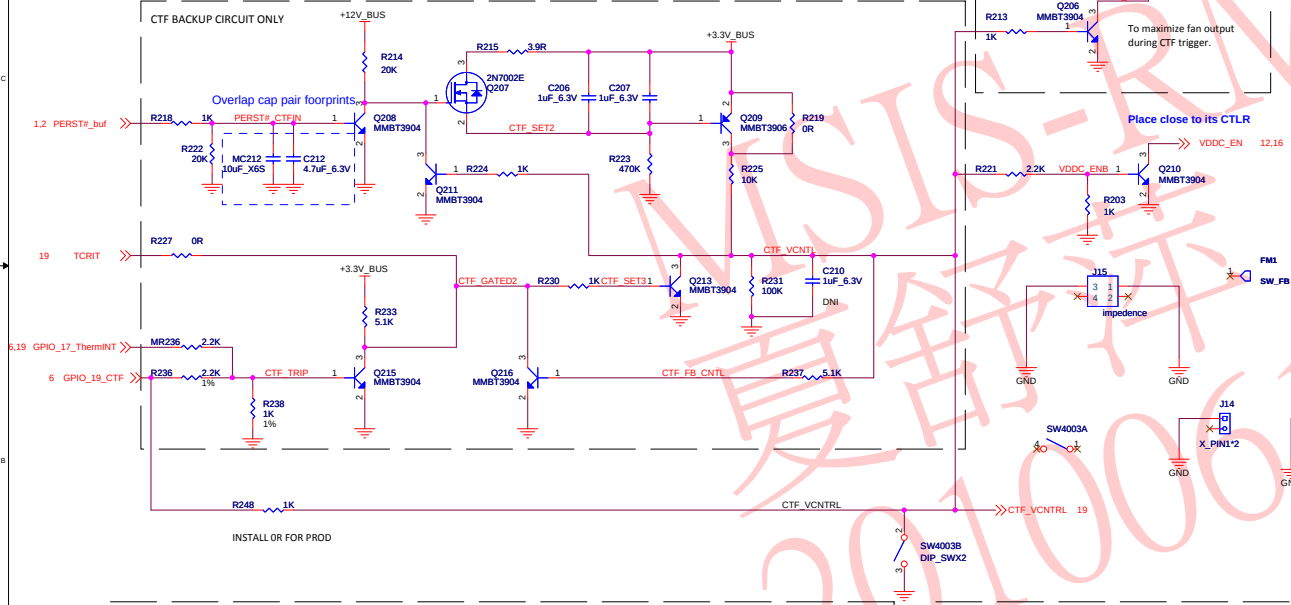
(19) Mechanical and Thermal Management



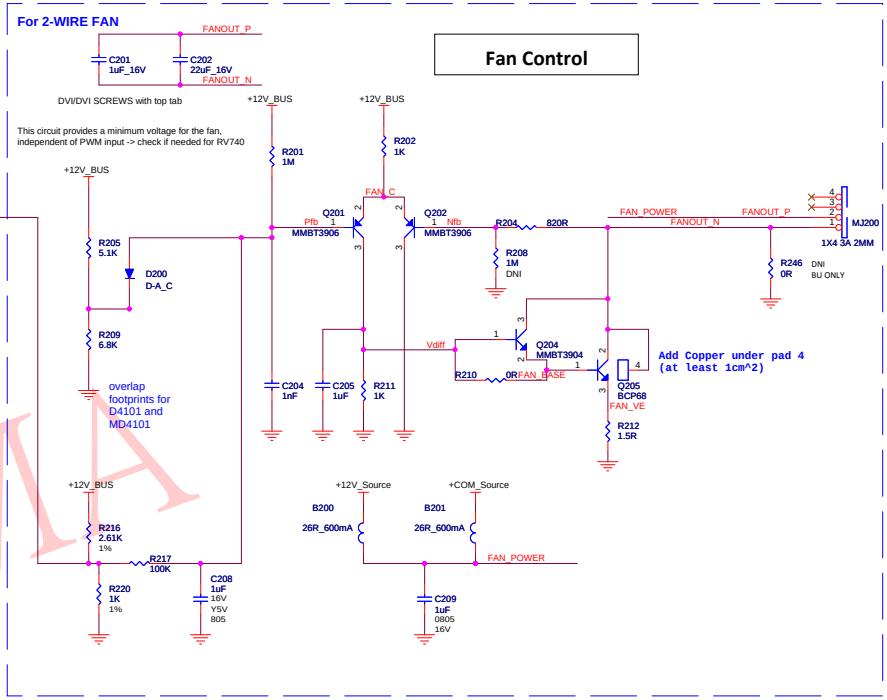
Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board.
This is an open collector signal. Active level is hard pull down to ground.

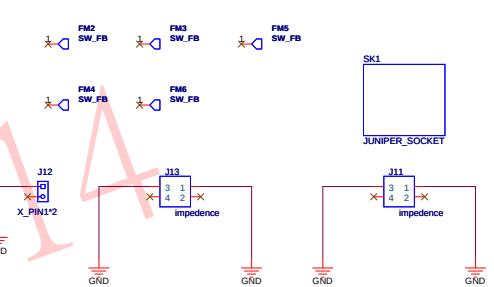
Critial Temperature Fault



For 2-WIRE FAN



Fan Control



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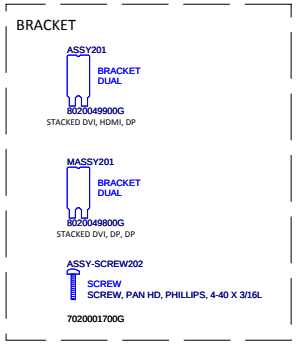
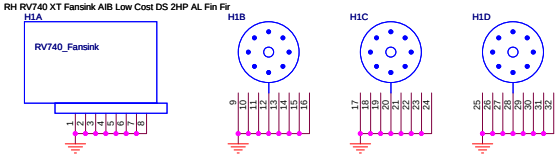


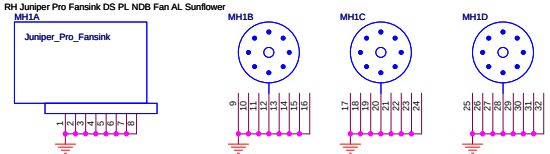
HEATSINK

7120574000G
7120574000G
7120384000G

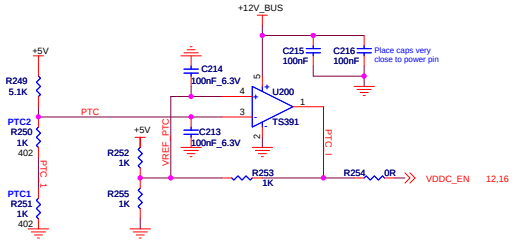
RH RV740 XT Fansink AIB Low Cost DS 2HP AL Fin Fir



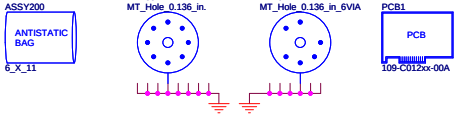
RH Juniper Pro Fansink DS PL NDB Fan AL Sunflower



VDDC Thermal Protection



J11 1層 80OHM (0.13mm/0.19mm =>5.1181 mils/7.4803 mils) WCK
J13 3 層 80OHM (0.175mm/0.28mm=>6.889 mils/11.0236 mils) WCK
J12 1.6層 45OHM (0.13mm => 5.1181 mils)
J14 3 層 45OHM (0.175mm =>6.9mils)
J15 6 層 80OHM (0.14mm/0.17mm =>5.7 mils/6.8 mils) CLK



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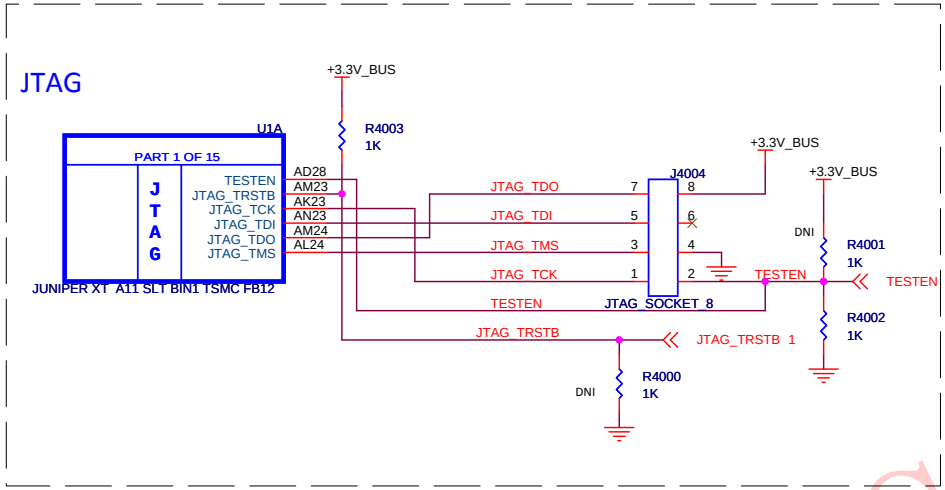
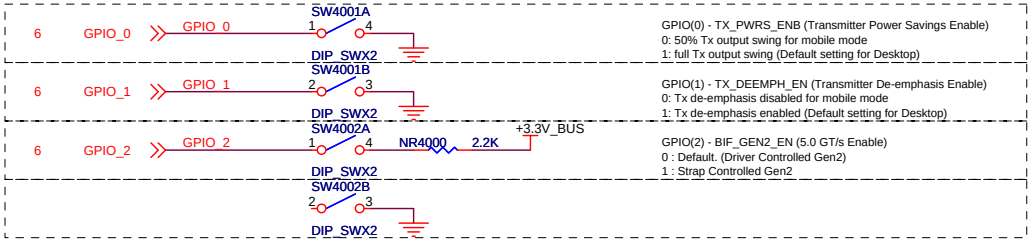
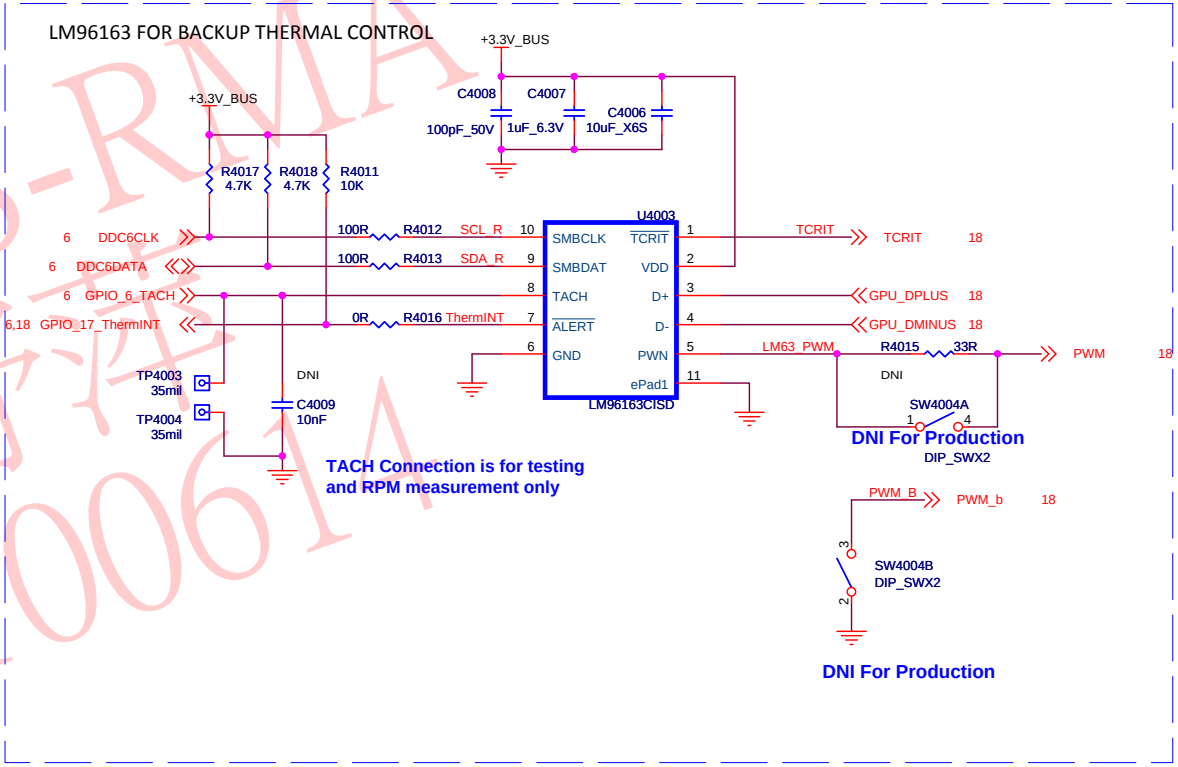
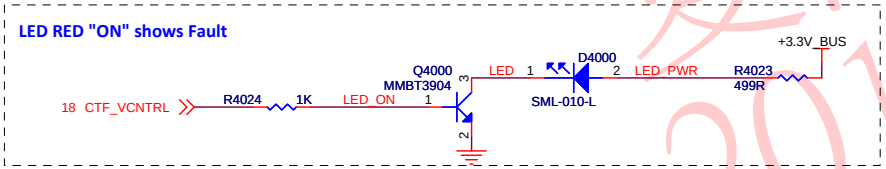
(19) Debug Circuits



SWITCH CONNECTIONS TO PINSTRAPS







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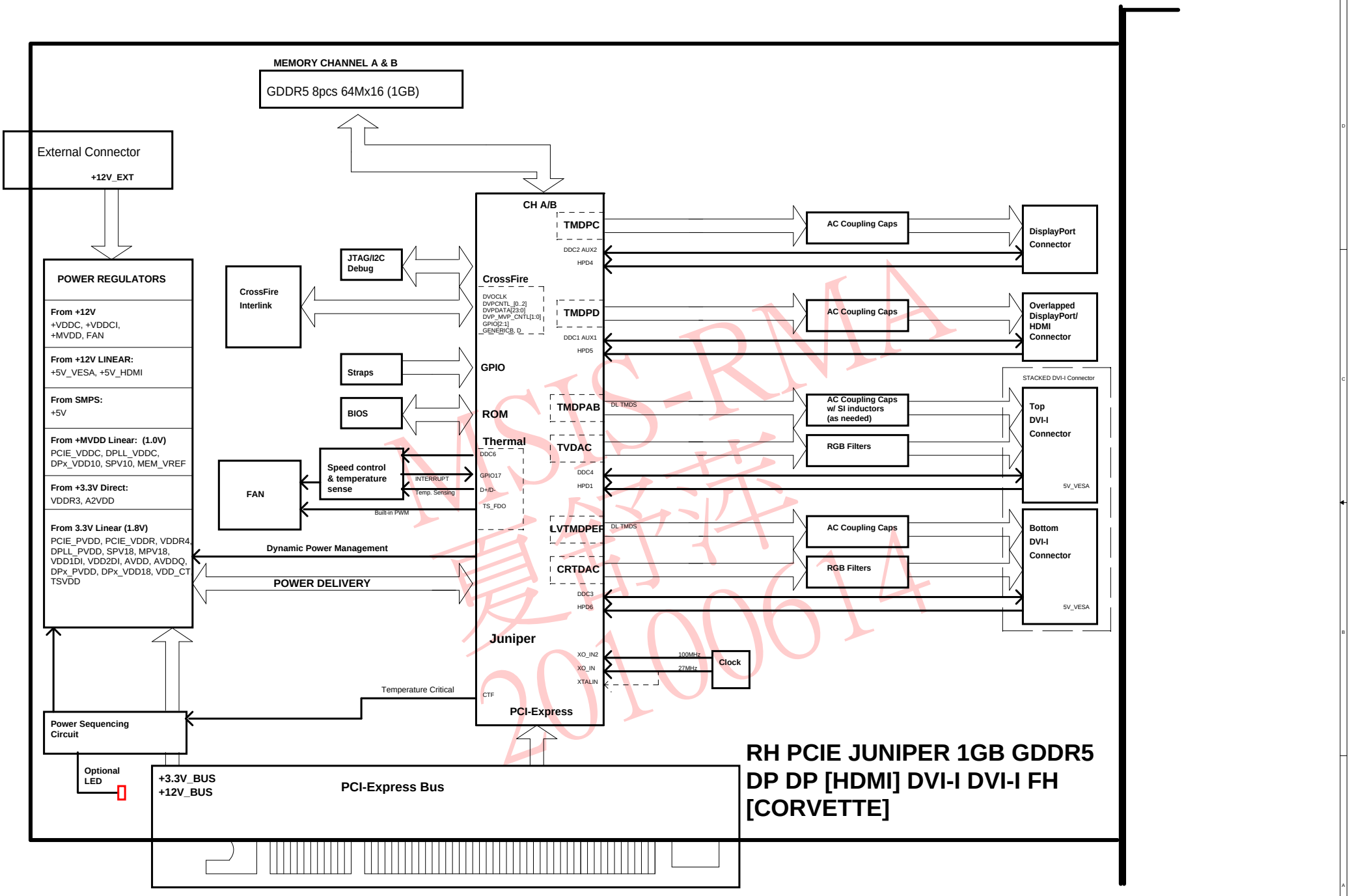

RH PCIE JUNIPER 1GB GDDR5 DP DP [HDMI] DVI-I DVI-I FH [CORVETTE]

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Title	Schematic No.	Date:
RH JUNIPER LE GDDR5 1GB DP+DP/HDMI+2xDVI	105-C012xx-00C	Tuesday, April 06, 2010

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 02

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/03/23	JUNIPER LE GDDR5 1GB - BASED ON C010 REV43;
01	00B	2009/07/13	
02	00C	2009/09/09	Added PCIe Reset Circuitry
	20	2010/04/01	Page 04 Removed U2100,U2200 ; U2000,U2300 set to x32 mode Page 05 Removed U2500,U2600 ; U2400,U2700 set to x32 mode Page 08 Add EMI bridge resister R1718~R1724 for DVI top Page 09 Add EMI bridge resister R1833~R1836 for HDMI Page 10 Add EMI bridge resister R1918~R1924 for DVI bot Page 11 Add POSCAP C751 Page 12 Add UP6262 VDDC adj circuit changed VDDC output choke footprint Page 13 changed MVDD output choke footprint Page 14 changed VDDCi output choke footprint Page 17 Add UP6266 VID circuit for VDDC adj Page 18 changed FAN connector to 4pin from 2pin