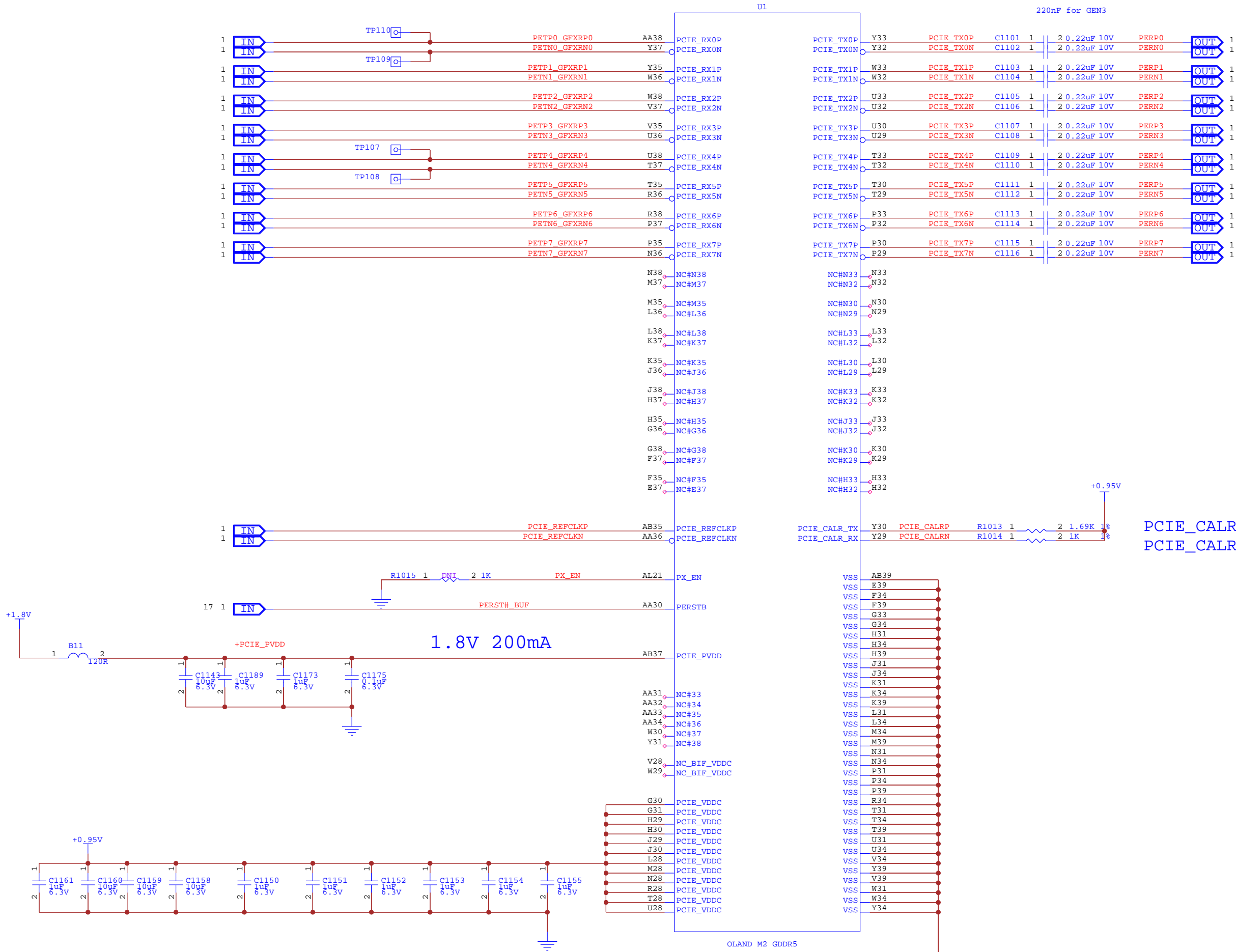


Oland PCIe Interface

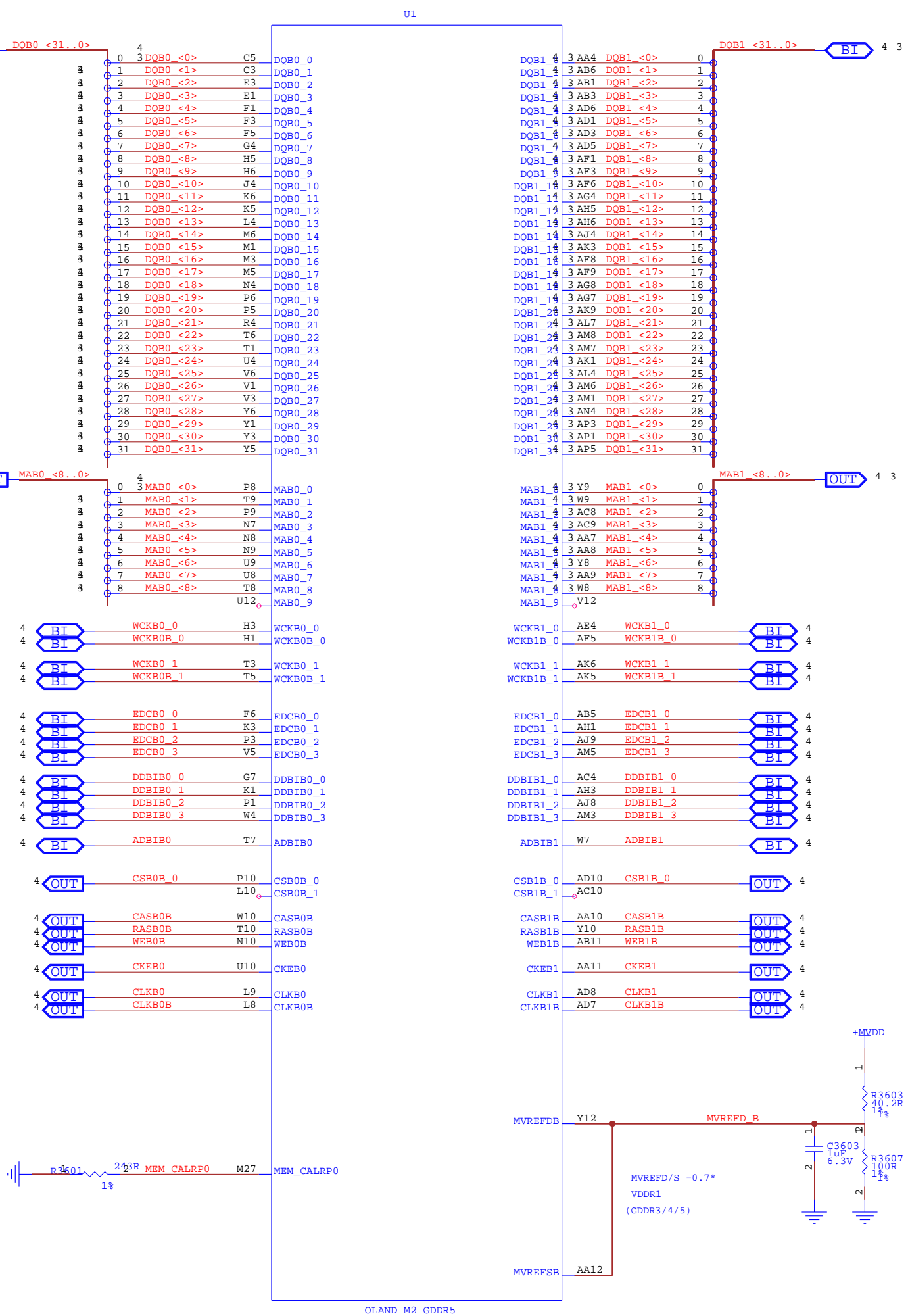
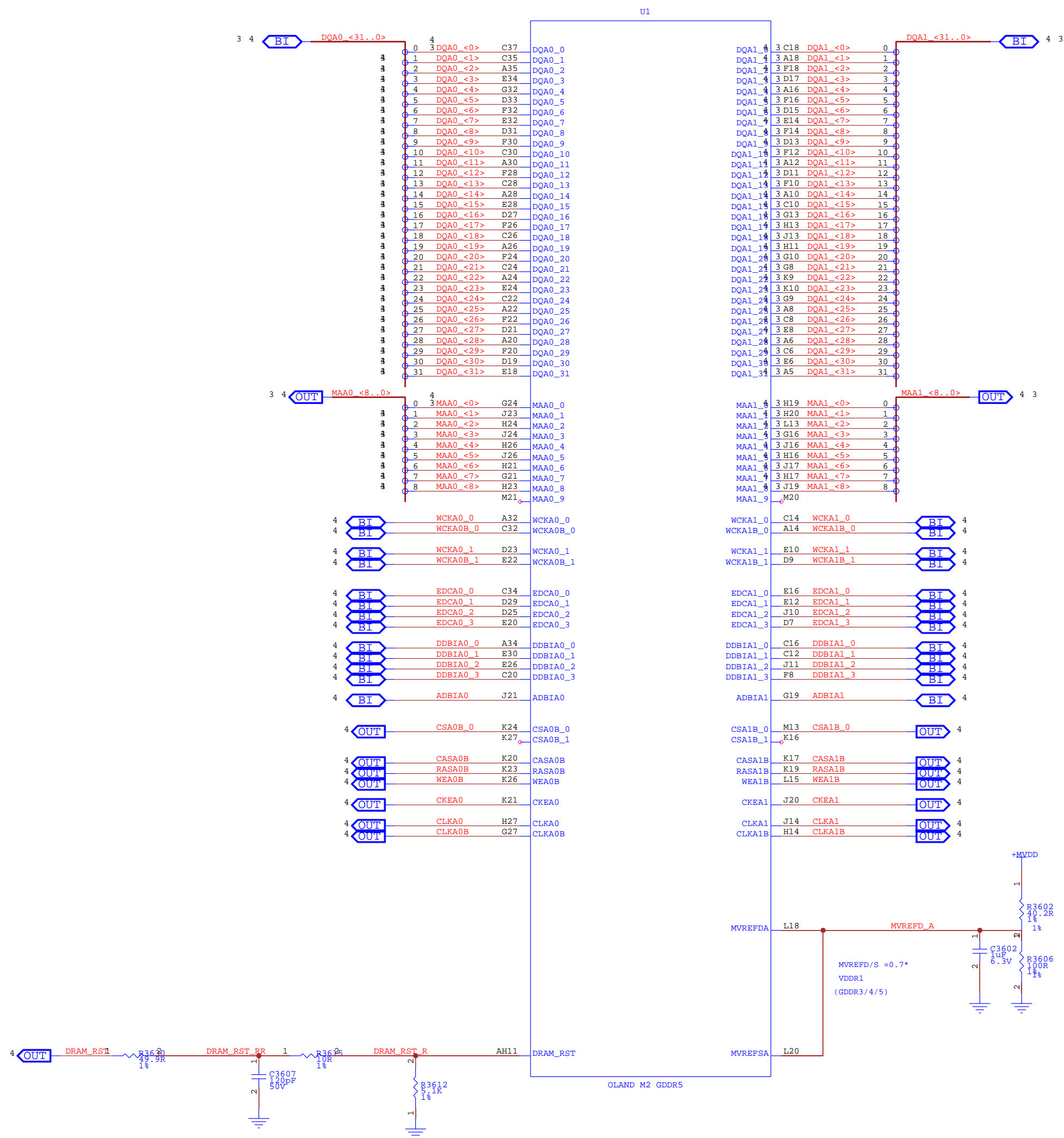
NOTE: Some of the PCIe testpoints will be available through vias on traces.



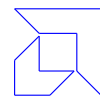
PCIE\_CALR\_TX 1.69k pull up for Oland  
PCIE\_CALR\_RX 1k pull up for Oland

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SHEET: Oland PCIe Interface		TITLE:	
DATE: Fri Oct 28 17:09:40 2016	REV: 1.0	TITLE	
SHEET NUMBER: 2 OF 21			
DOCUMENT NUMBER: 105_CXXX00_00A			

(3) Oland MEM Interface Ch A&B



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SHEET: Oland MEMORY INTERFACE

DATE: Fri Oct 28 17:09:40 2016

REV: 1.0

SHEET NUMBER: 3 OF 21

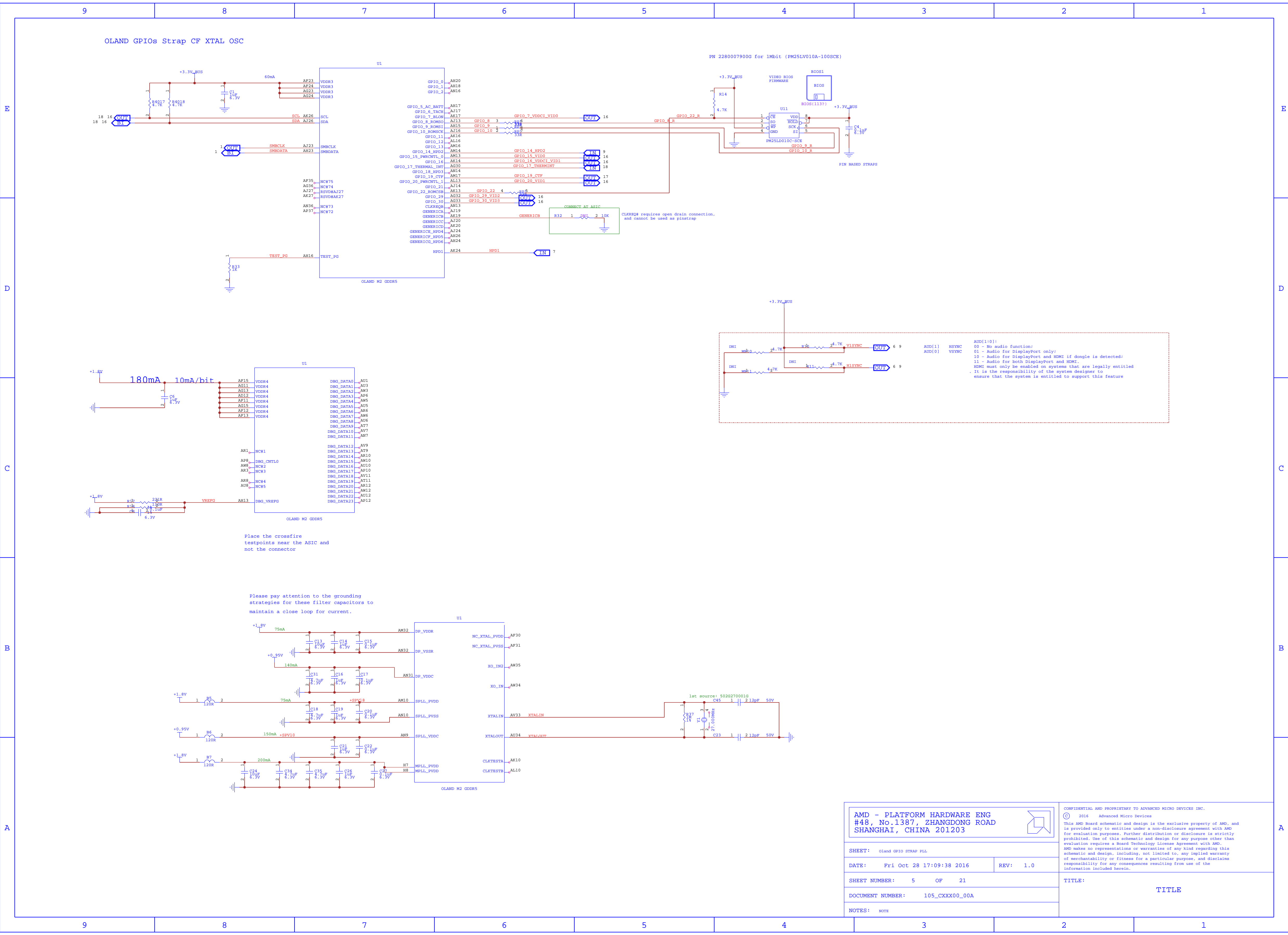
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DOCUMENT NUMBER: 105\_CXXX00\_00A

TITLE

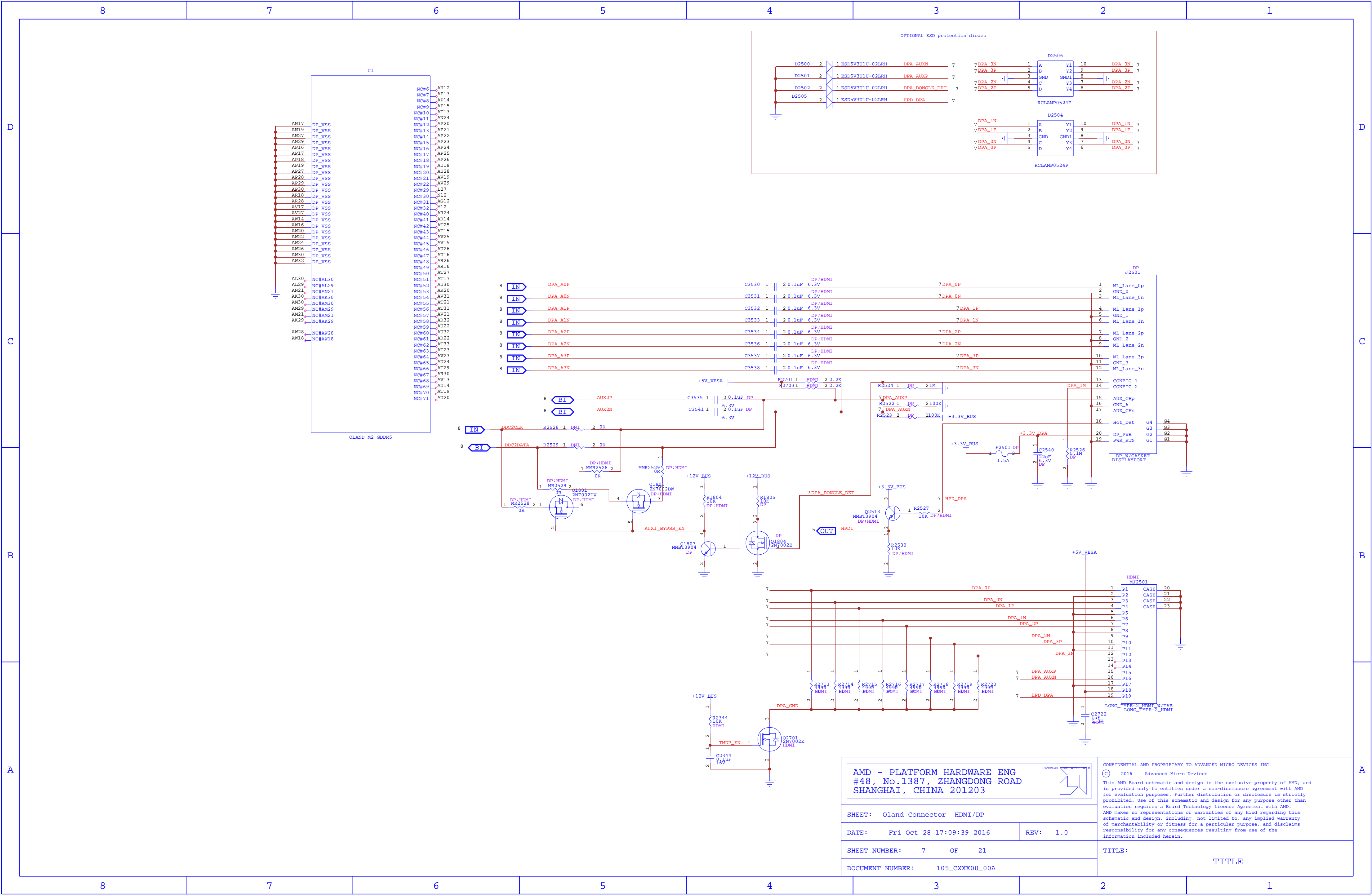




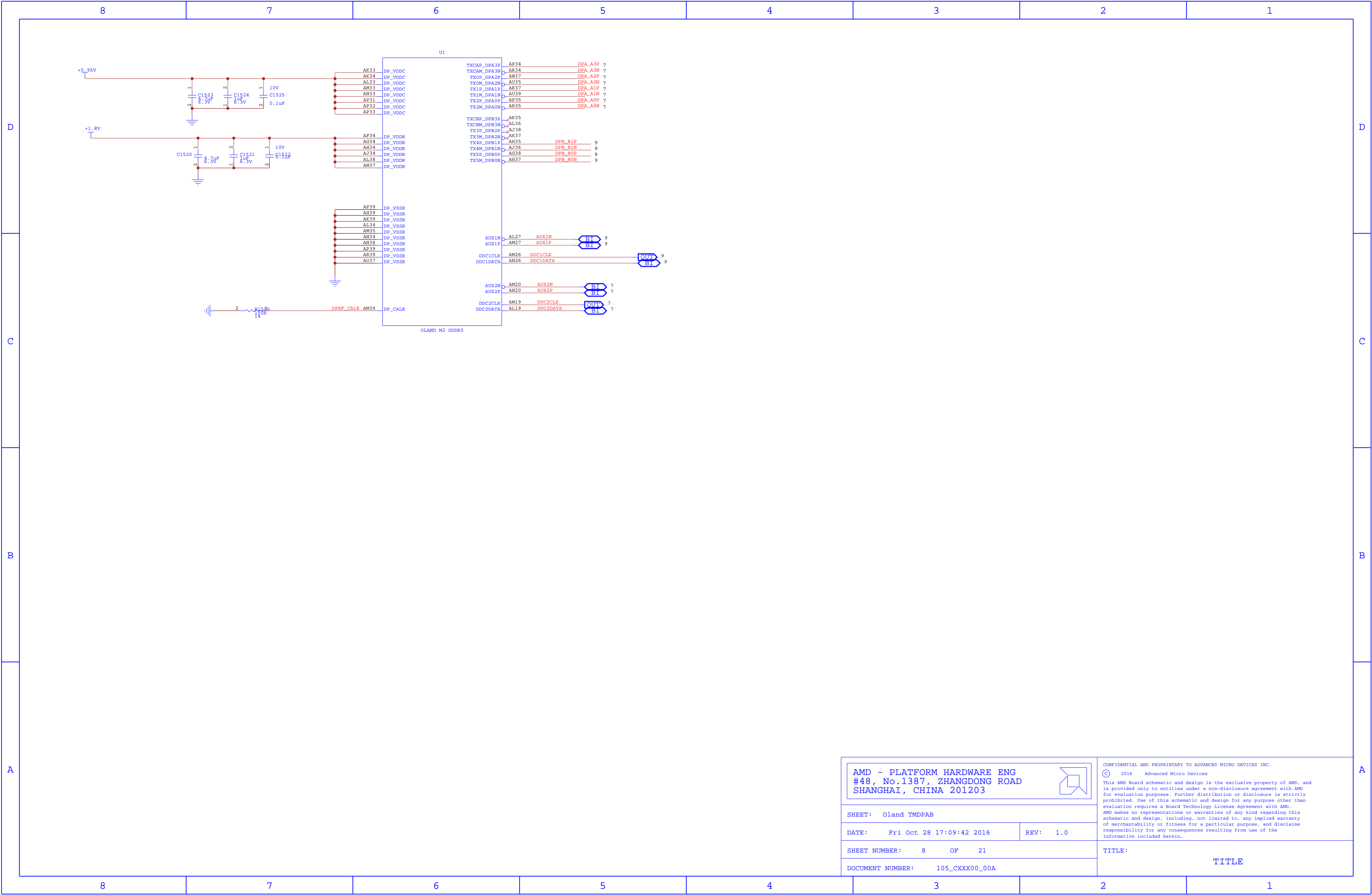


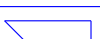
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SHEET:	Oland GPIO STRAP PLL				
DATE:	Fri Oct 28 17:09:38 2016		REV:	1.0	
SHEET NUMBER:	5	OF	21	TITLE:	
DOCUMENT NUMBER:	105_CXXX00_00A			TITLE	
NOTES:	NOTE				



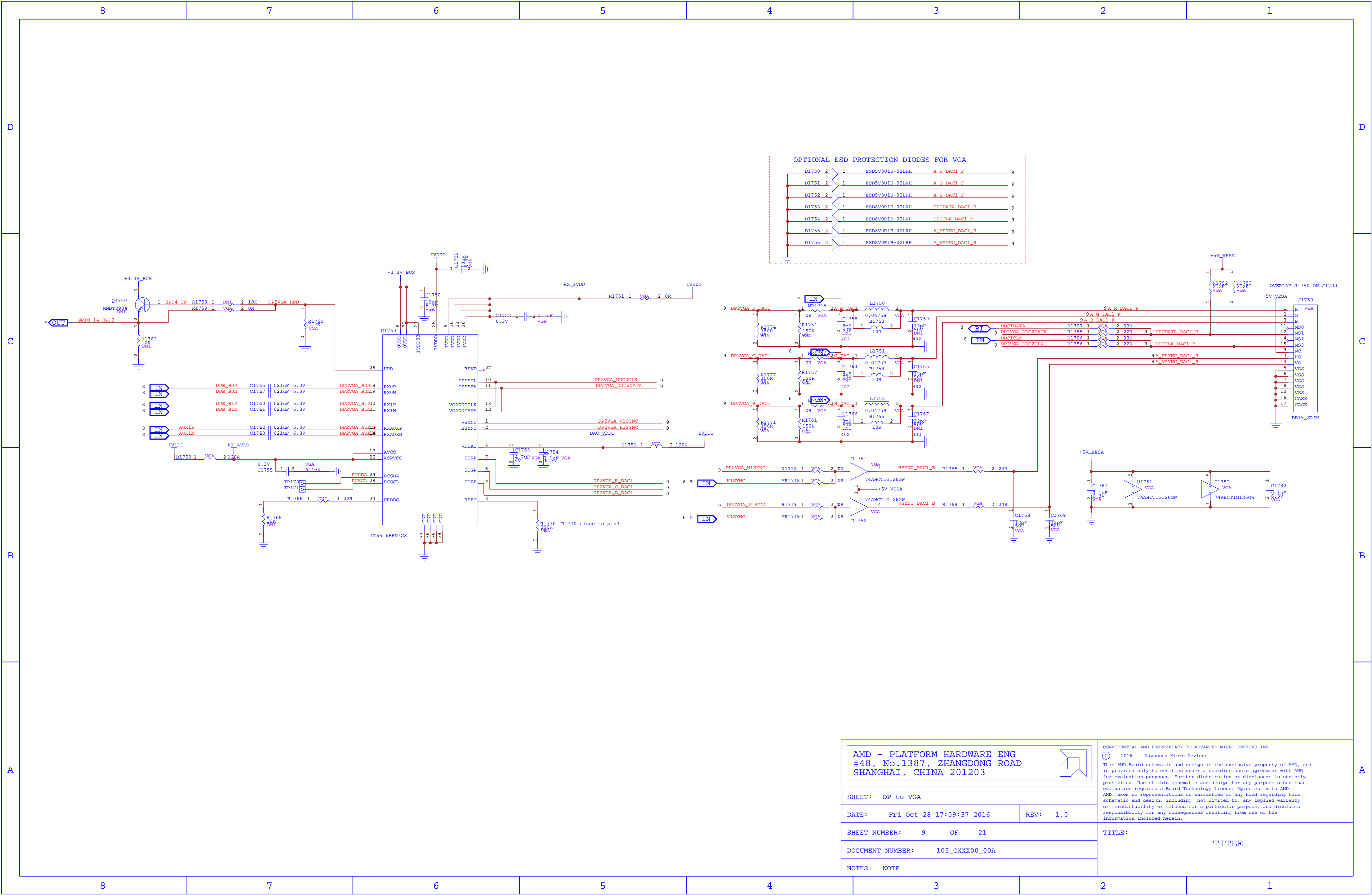


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SHEET: Oland Connector HDMI/DP		TITLE:	
DATE: Fri Oct 28 17:09:39 2016	REV: 1.0	TITLE	
SHEET NUMBER: 7 OF 21			
DOCUMENT NUMBER: 105_CXXX00_00A			



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SHEET: Oland TMDPAB				© 2016 Advanced Micro Devices	
DATE: Fri Oct 28 17:09:42 2016		REV: 1.0	<p>This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD.</p> <p>AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.</p>		
SHEET NUMBER: 8 OF 21		TITLE:			
DOCUMENT NUMBER: 105_CXXX00_00A		TITLE			





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SHEET: DP to VGA			TITLE: TITLE		
DATE: Fri Oct 28 17:09:37 2016		REV: 1.0			
SHEET NUMBER: 9 OF 21					
DOCUMENT NUMBER: 105_CXX00_00A					
NOTES: NOTE					

[illegible]

REV: 1.0

TITLE

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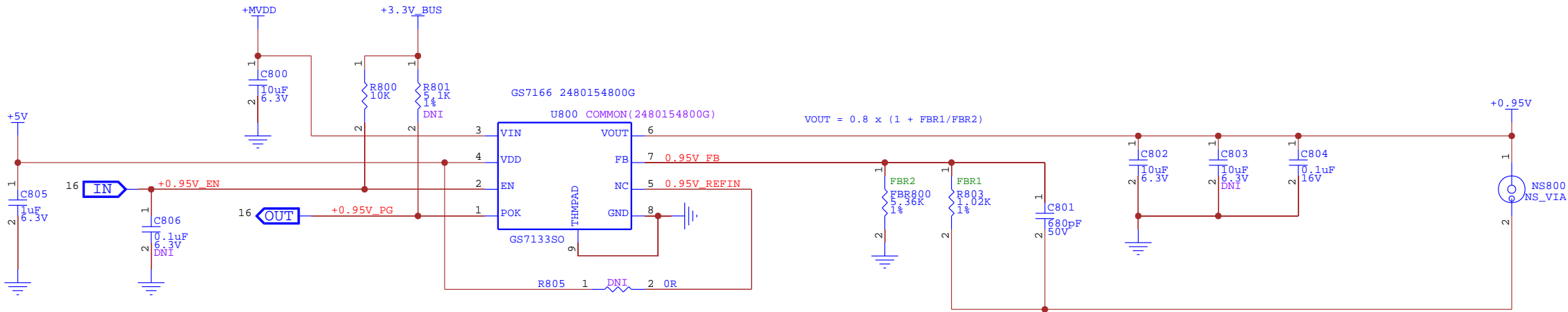
B

A

Linear Regulators

LDO #1: Vin = +1.5V +/-2% Vout = +0.95V +/- 2% Iout = 1.44A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



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SHEET: 0.95V			TITLE:	
DATE: Fri Oct 28 17:09:36 2016		REV: 1.0	TITLE	
SHEET NUMBER: 11 OF 21		DOCUMENT NUMBER: 105_CXXX00_00A		

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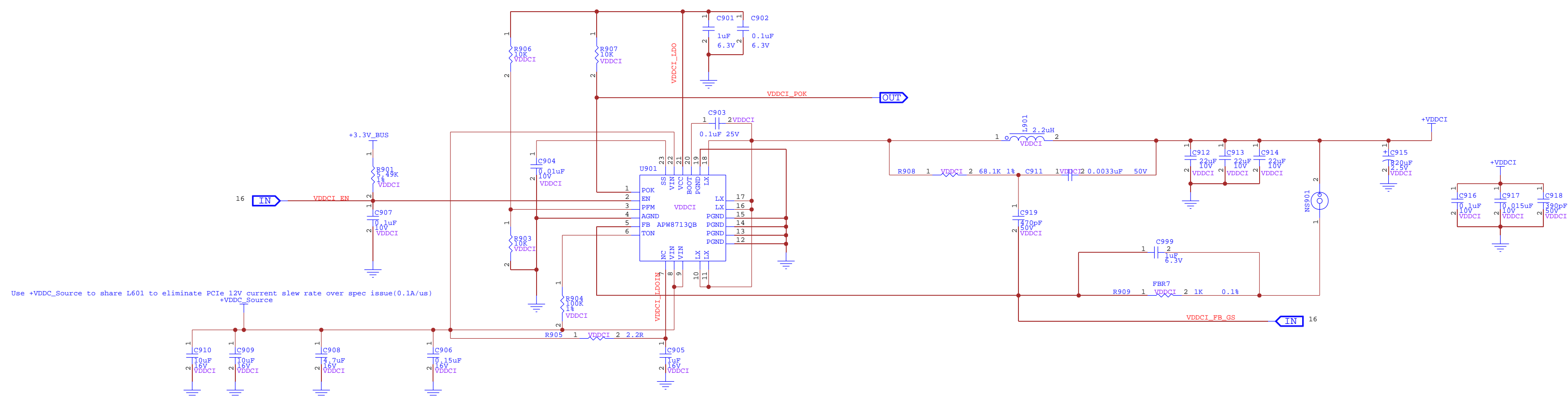
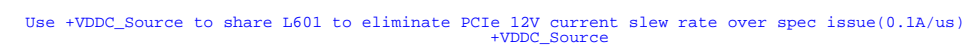
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A



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NOTES: NOTE

TITLE

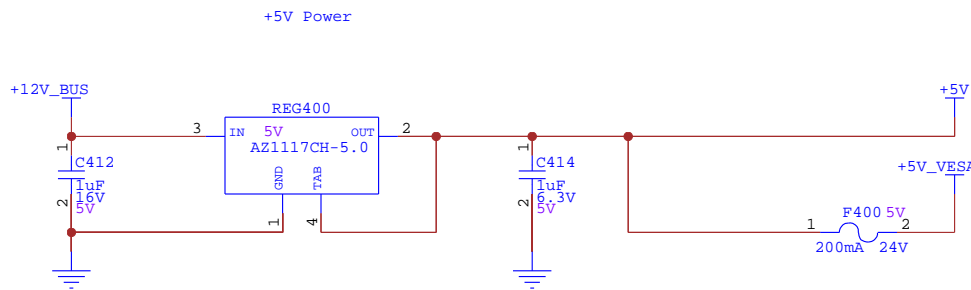
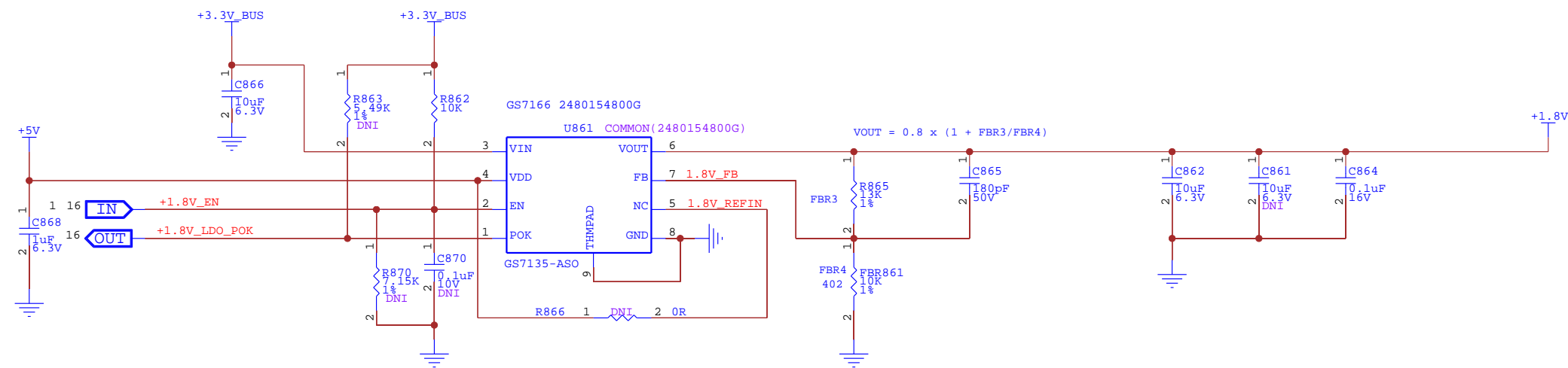




8		7		6		5		4		3		2		1	
Linear Regulators															
<div>LDO #2: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2% Iout = 1.6A (TBV) RMS MAX</div> <div>PCB: 50 to 70mm sq. copper area for cooling</div>															
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SHEET: Linear Regulators										TITLE: TITLE					
DATE: Fri Oct 28 17:09:41 2016					REV: 1.0										
SHEET NUMBER: 15 OF 21															
DOCUMENT NUMBER: 105_CXXX00_00A															
8		7		6		5		4		3		2		1	

Linear Regulators

LDO #2: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2% Iout = 1.6A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling

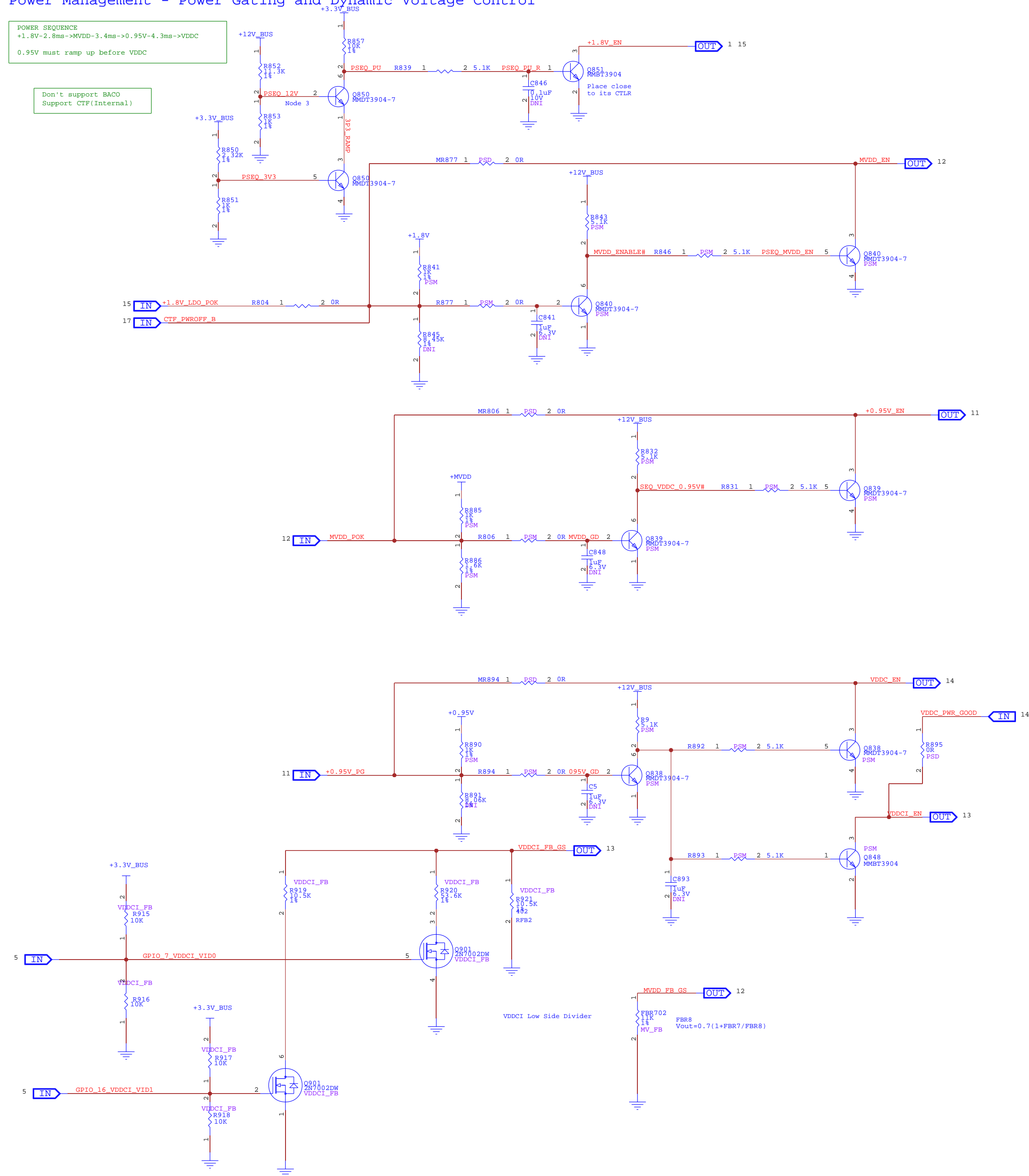


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SHEET: Linear Regulators			TITLE:  TITLE		
DATE: Fri Oct 28 17:09:41 2016		REV: 1.0			
SHEET NUMBER: 15 OF 21					
DOCUMENT NUMBER: 105_CXXX00_00A					

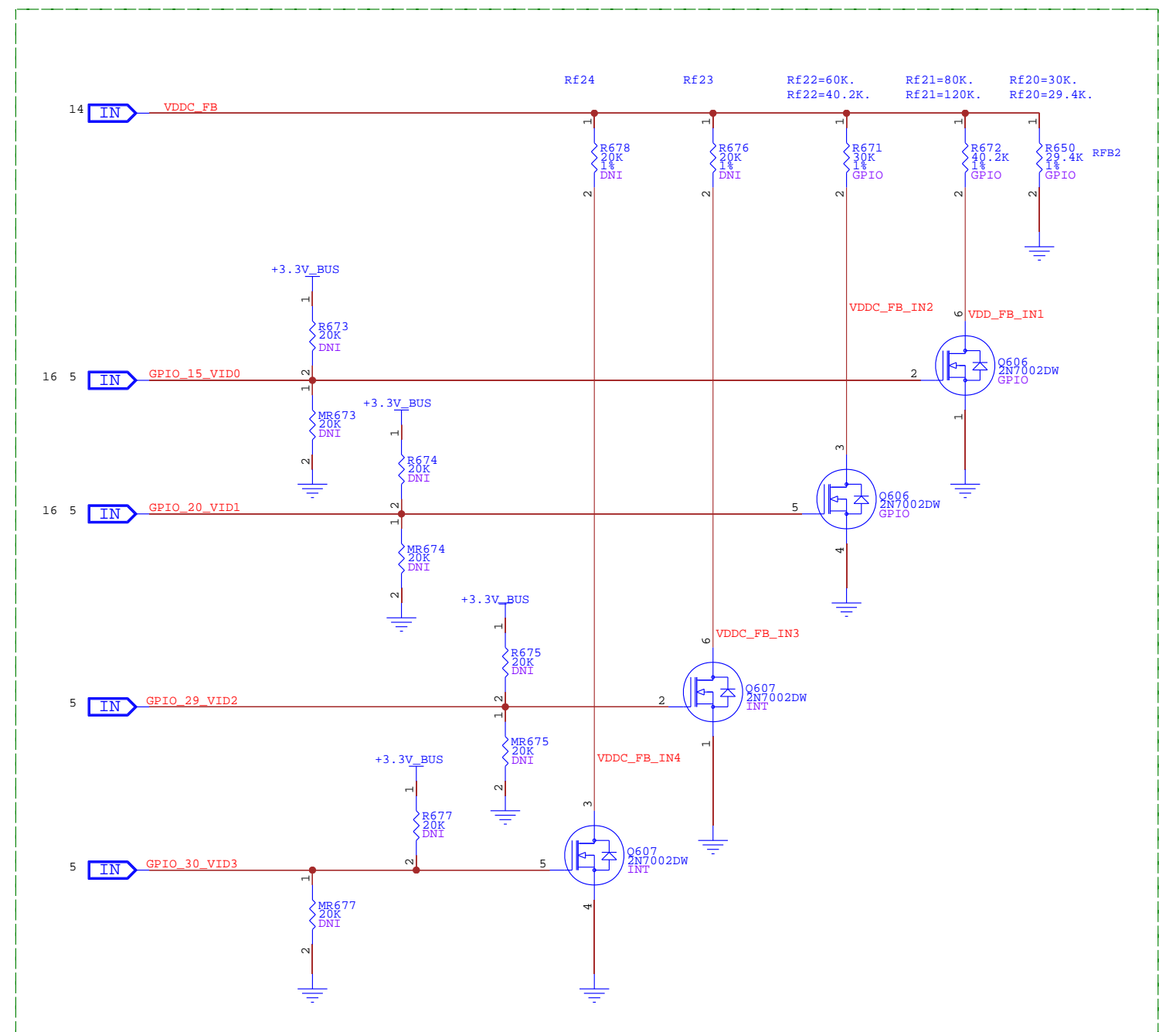
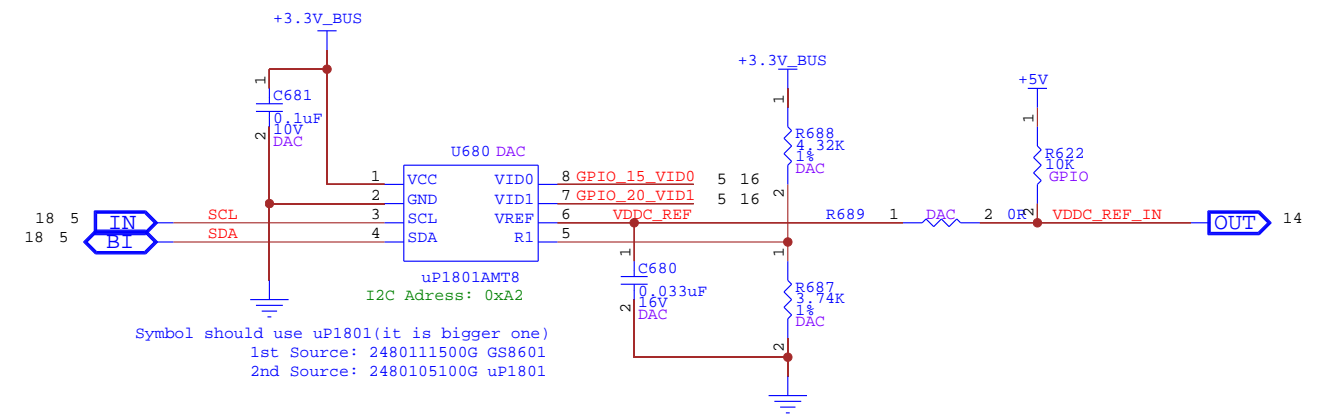
## Power Management - Power Gating and Dynamic Voltage Control

POWER SEQUENCE  
+1.8V-2.8ms->MVDD-3.4ms->0.95V-4.3ms->VDDC  
0.95V must ramp up before VDDC

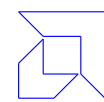
```
Don't support BACO
Support CTF(Internal)
```



### VDDC Low Side Divider



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SHEET: PWR MGMT &amp; SEQ

DATE: Fri Oct 28 17:09:39 2016

SHEET NUMBER: 16 OF 21

DOCUMENT NUMBER: 105\_CXXX00\_00A

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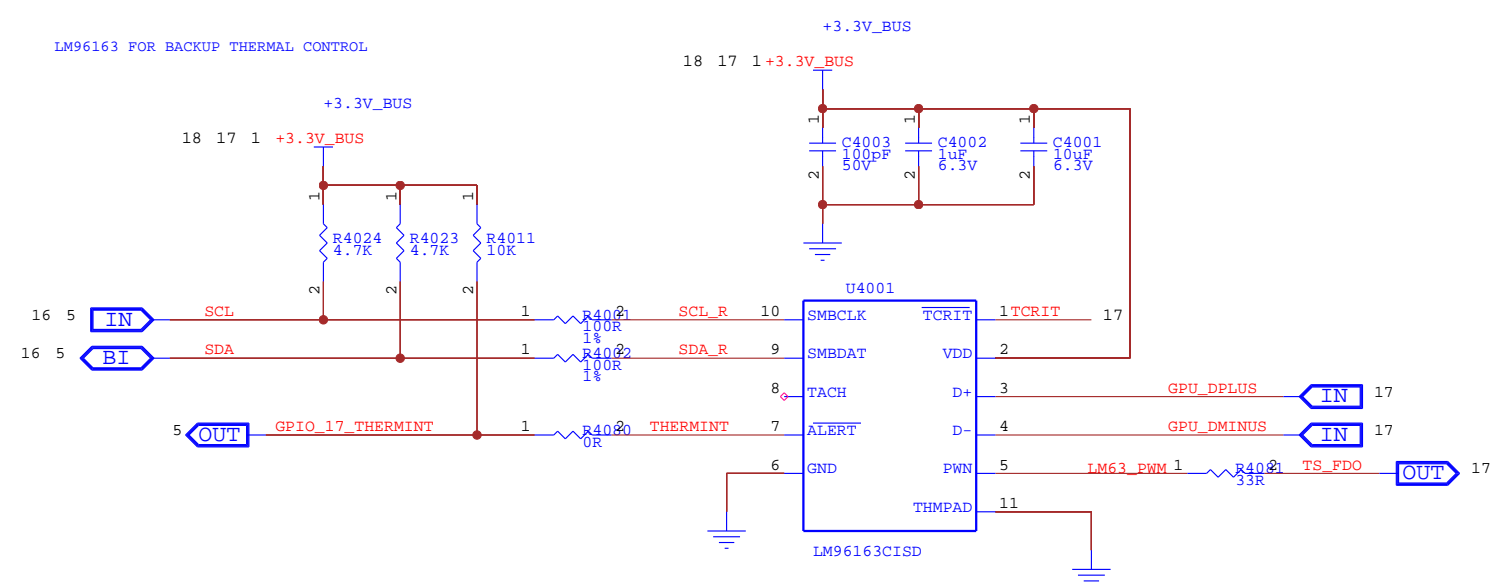
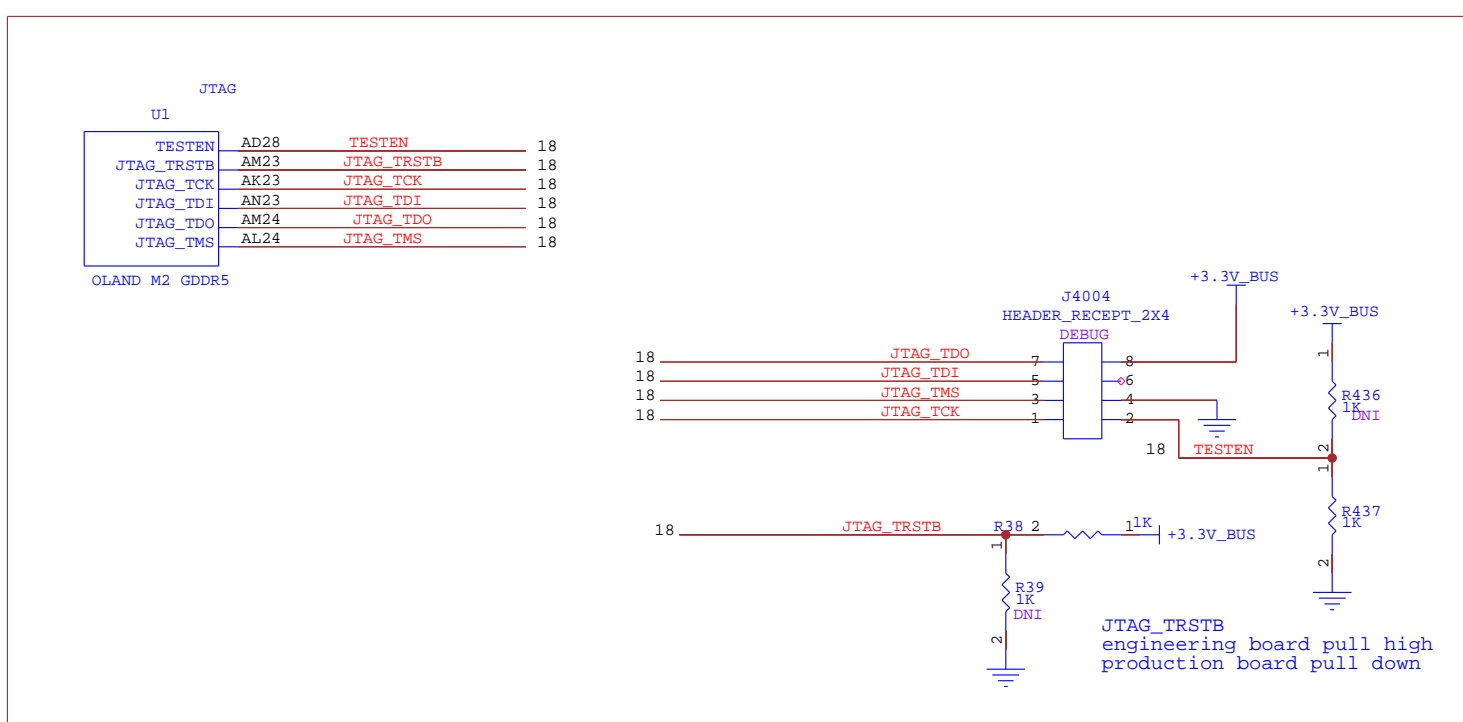
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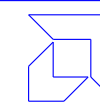
TITLE



## (19) Debug Circuits



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SHEET: Debug Circuit

DATE: Fri Oct 28 17:09:42 2016

REV: 1.0

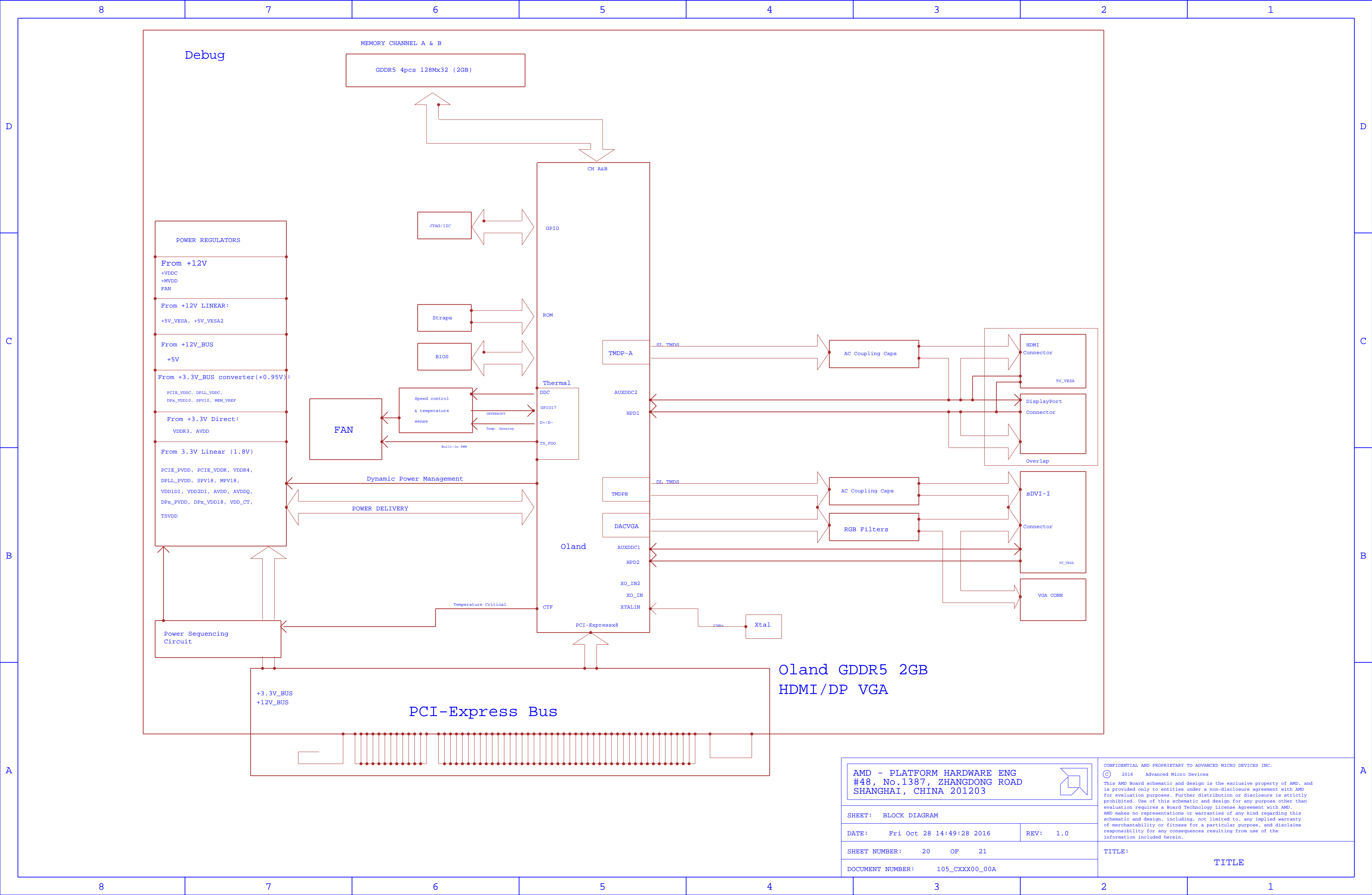
SHEET NUMBER: 18 OF 21

TITLE:

TITLE







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SHEET: BLOCK DIAGRAM		TITLE:	
DATE: Fri Oct 28 14:49:28 2016	REV: 1.0	TITLE	
SHEET NUMBER: 20 OF 21			
DOCUMENT NUMBER: 105_CXXX00_00A			

8				7		6		5		4		3		2		1					
<div>AMD</div>				TITLE:				DOCUMENT NUMBER: 105_CXXX00_00A				DATE: Fri Oct 28 14:49:28 2016				SHEET NUMBER: 21 OF 21				REV: 1.0	
REVISION HISTORY				ENGINEER: XXX				NOTES: NOTE				CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. C • 2016 Advanced Micro Devices This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.				AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203					
SCH Rev		PCB Rev		Date		REVISION DESCRIPTON															
1.00		00A		2016-10-28		Based on C869, initial release															
8				7		6		5		4		3		2		1					