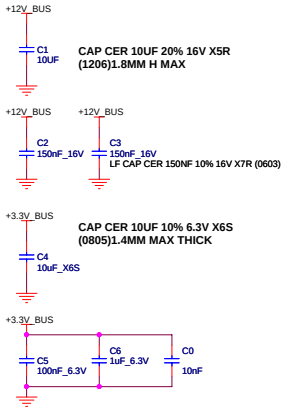
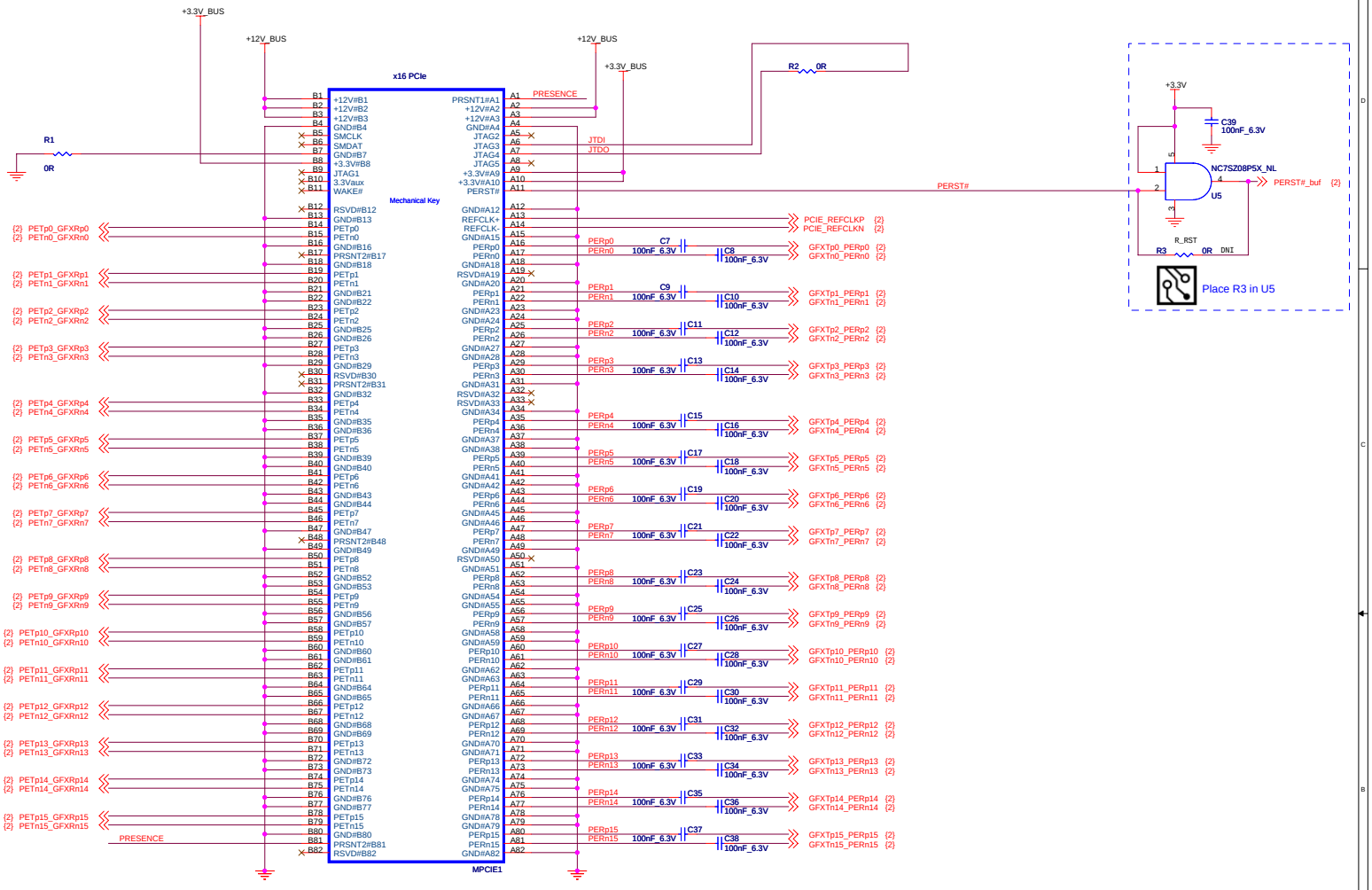
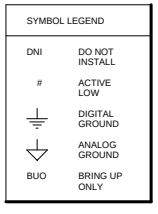
PCI-EXPRESS EDGE CONNECTOR



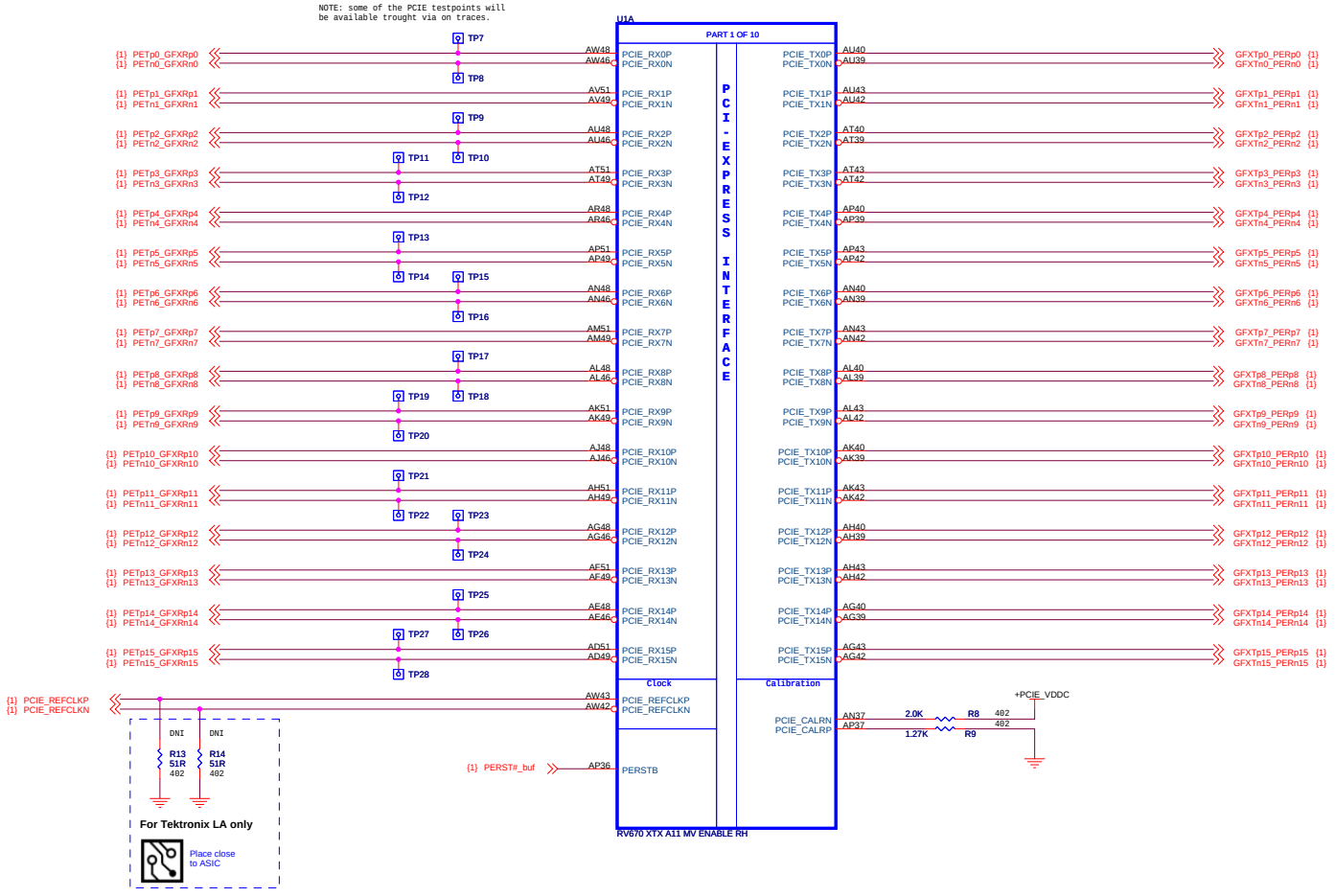
Place these caps as close to the PCIE connector as possible





Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Monday, October 08, 2007
Rev	1
Sheet	1 of 21
Title	RH RV670 - PCI-E Edge Connector
Doc No.	105-B340xx-00B



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1 Commerce Valley Drive East
Markham, Ontario

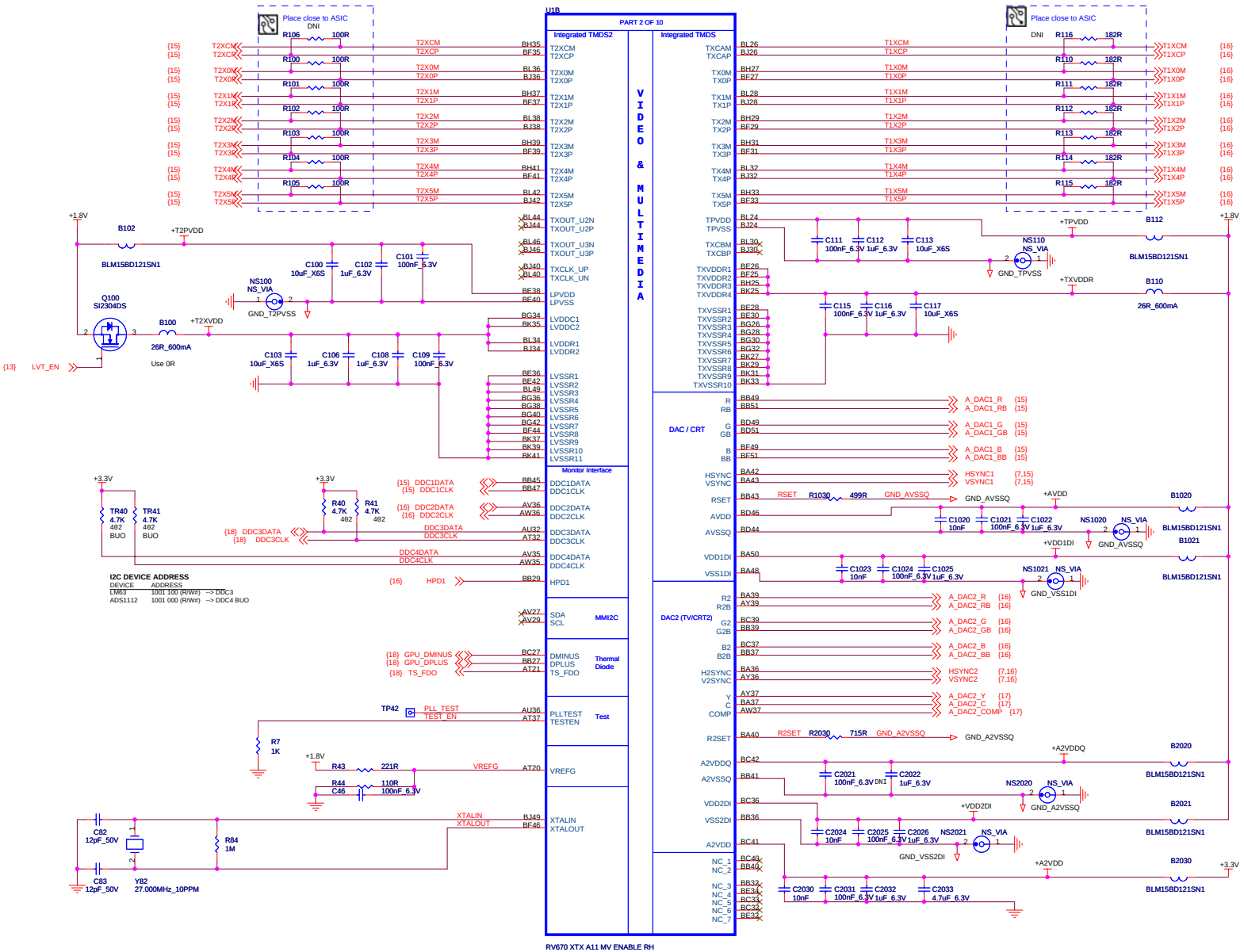
Date: Monday, October 08, 2007 Rev 1

Sheet 2 of 21

Title RH RV670 - ASIC PCIE_Interface

Doc No. 105-B340xx-00B

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
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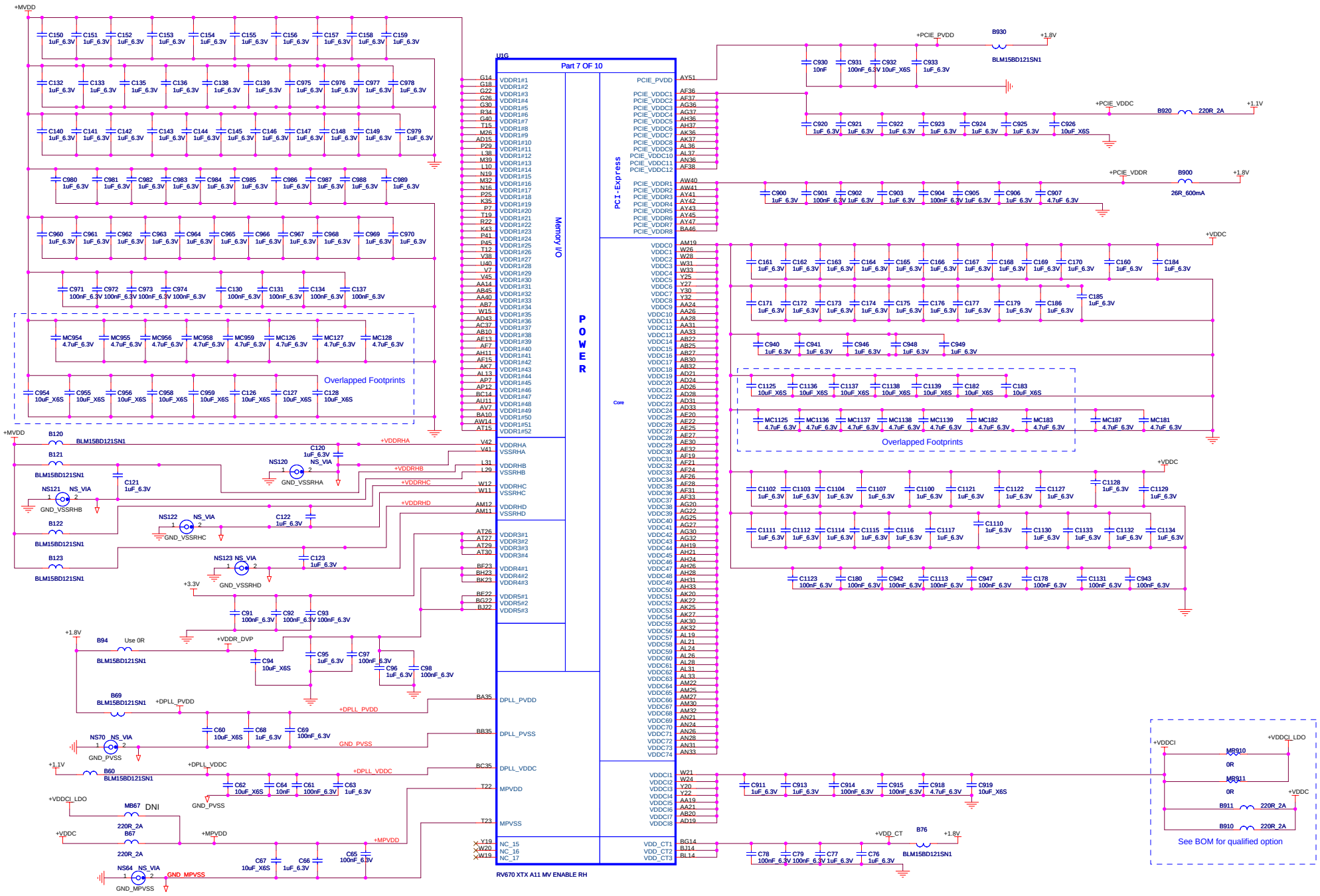
Date:	Monday, October 08, 2007
Rev	1
Sheet	3 of 21
Title	RH RV670 - ASIC MAIN
Doc No.	105-B340xx-00B


U1G
Part 7 OF 10
POWER
Memory I/O
PCI-Express
Core
Overlapped Footprints
Overlapped Footprints
See BOM for qualified option
RV670 XTX A11 MV ENABLE RH
+MVDD
+VDDC
+PCIE_PVDD
+PCIE_VDDC
+PCIE_VDDR
+VDDRHA
+VDDRHB
+VDDRHC
+VDDRHD
+VDDR3
+3.3V
+1.8V
+1.1V
+DPLL_PVDD
+DPLL_VDDC
+MPVDD
+VDDCI
+VDDCI_LDO
+VDD_CT
GND_VSSRHA
GND_VSSRHB
GND_VSSRHC
GND_VSSRHD
GND_PVSS
GND_MPVSS
B930
BLM15BD121SN1
B920
220R_2A
B900
26R_600mA
B120
B121
B122
B123
B94
Use 0R
B69
B60
B67
MB67
DNI
B76
MR910
0R
MR911
0R
B911
220R_2A
B910
220R_2A
PCIE_PVDD
PCIE_VDDC1
PCIE_VDDC2
PCIE_VDDC3
PCIE_VDDC4
PCIE_VDDC5
PCIE_VDDC6
PCIE_VDDC7
PCIE_VDDC8
PCIE_VDDC9
PCIE_VDDC10
PCIE_VDDC11
PCIE_VDDC12
PCIE_VDDR1
PCIE_VDDR2
PCIE_VDDR3
PCIE_VDDR4
PCIE_VDDR5
PCIE_VDDR6
PCIE_VDDR7
PCIE_VDDR8
VDDC0
VDDC1
VDDC2
VDDC3
VDDC4
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VDDC6
VDDC7
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VDDC9
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VDDCI6
VDDCI7
VDDCI8
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VDD_CT2
VDD_CT3
VDDR1#1
VDDR1#2
VDDR1#3
VDDR1#4
VDDR1#5
VDDR1#6
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DPLL_PVSS
DPLL_VDDC
MPVDD
MPVSS
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NC_16
NC_17
NS120
NS121
NS122
NS123
NS70
NS64
NS_VIA
C120
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C130
C131
C134
C137
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C173
C174
C175
C176
C177
C179
C186
C185
MC954
MC955
MC956
MC958
MC959
MC126
MC127
MC128
MC1125
MC1136
MC1137
MC1138
MC1139
MC182
MC183
MC187
MC181
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402
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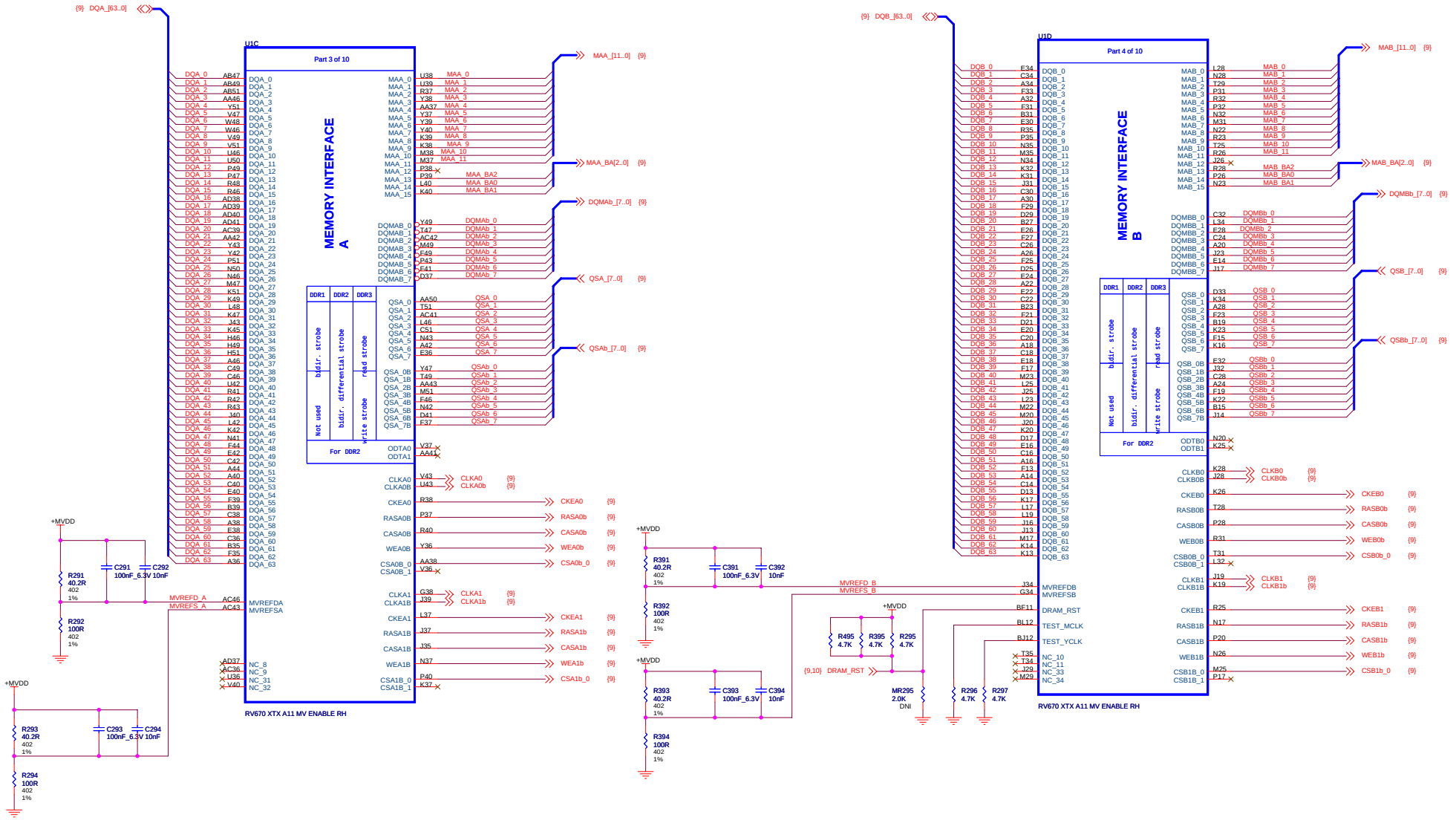
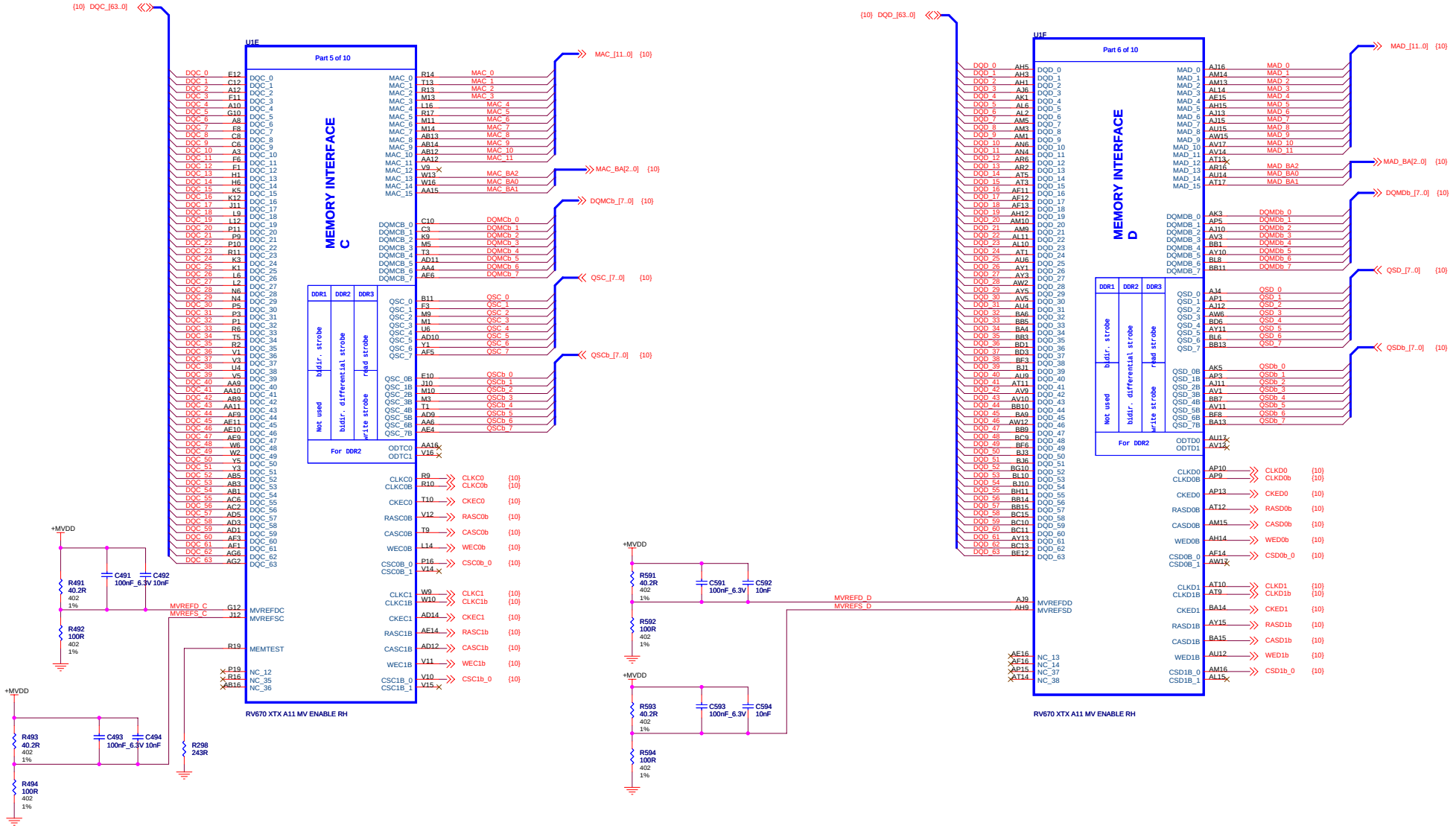
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario
Date: Monday, October 08, 2007
Rev 1
Sheet 4 of 21
Title RH RV670 - ASIC Power
Doc No. 105-B340xx-00B



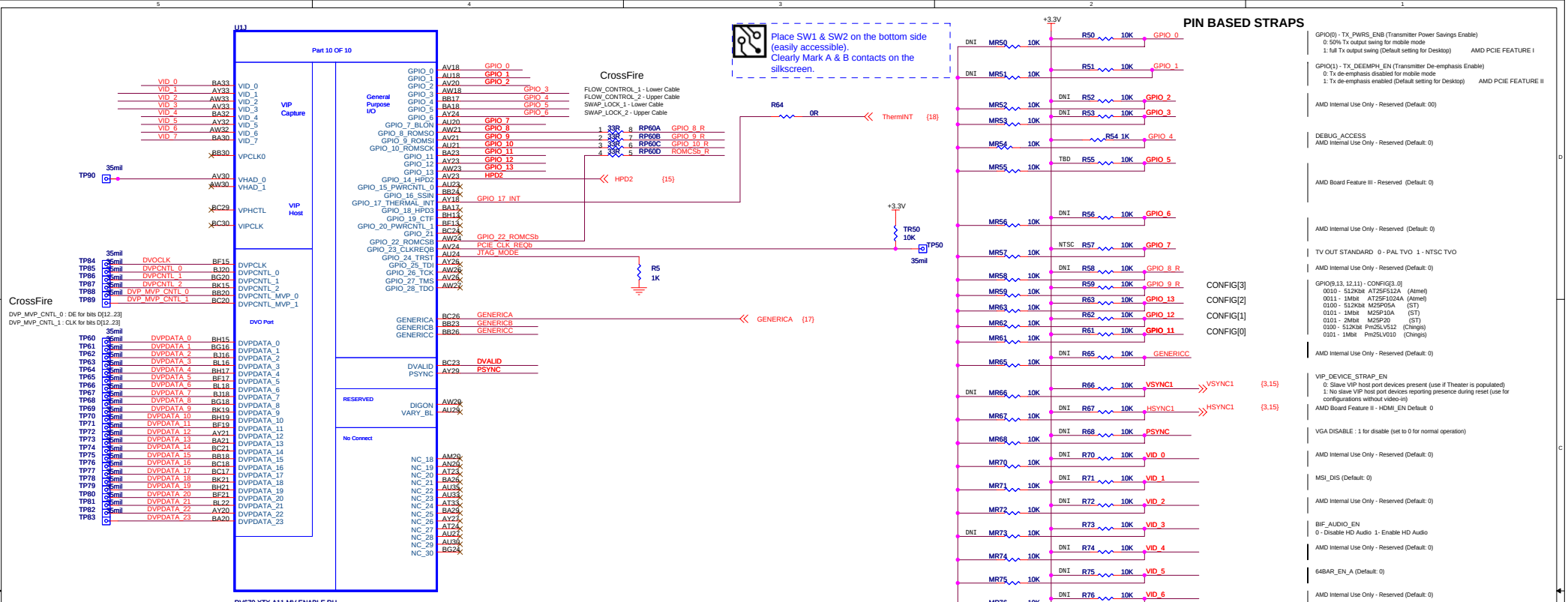
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Monday, October 08, 2007
Rev	1
Sheet	5 of 21
Title	RH RV670 - ASIC Memory Interface (Channel A & B)
Doc No.	105-B340xx-00B



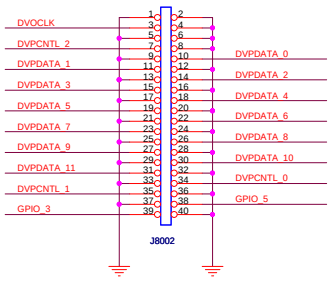
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Monday, October 08, 2007
Rev	1
Sheet	6 of 21
Title	RH RV670 - ASIC Memory Interface (Channel C & D)
Doc No.	105-B340xx-00B

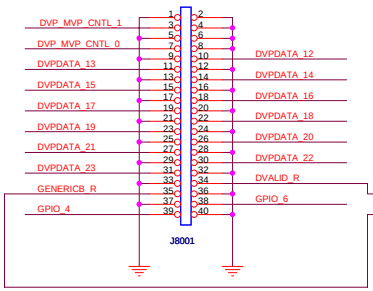


CrossFire Card-Edge

Lower Cable Card Edge

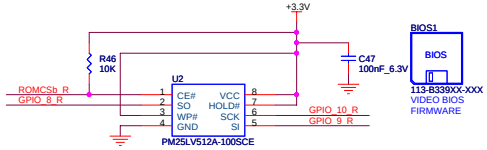


Upper Cable Card Edge



Bundle B

Bundle A (closer to the bracket)



Advanced Micro Devices Inc.
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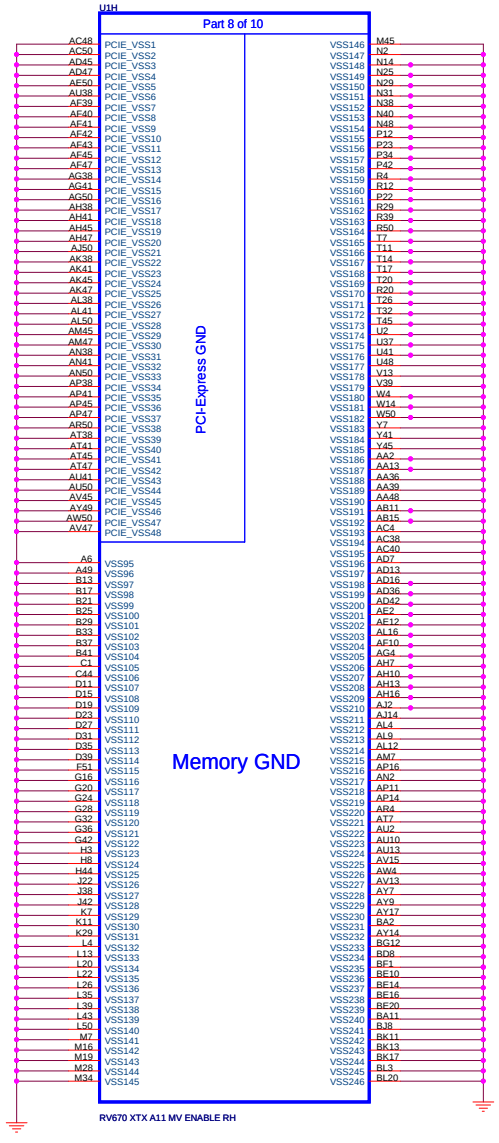
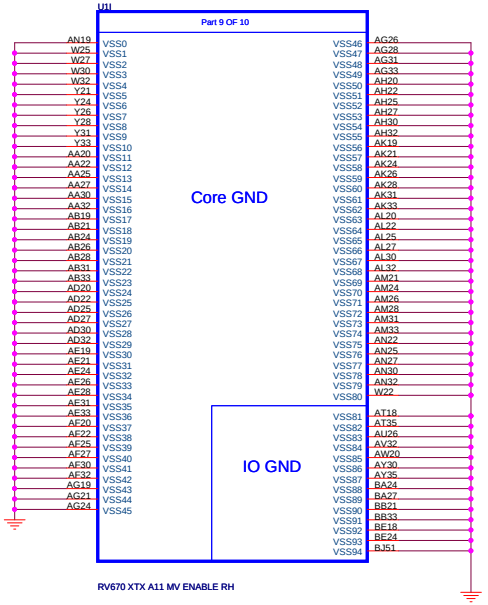
Markham, Ontario

Date:	Monday, October 08, 2007
Rev	1
Sheet	7 of 21
Title	RH RV670 - ASIC DVO, VIP & GPIOs
Doc No.	105-B340xx-00B





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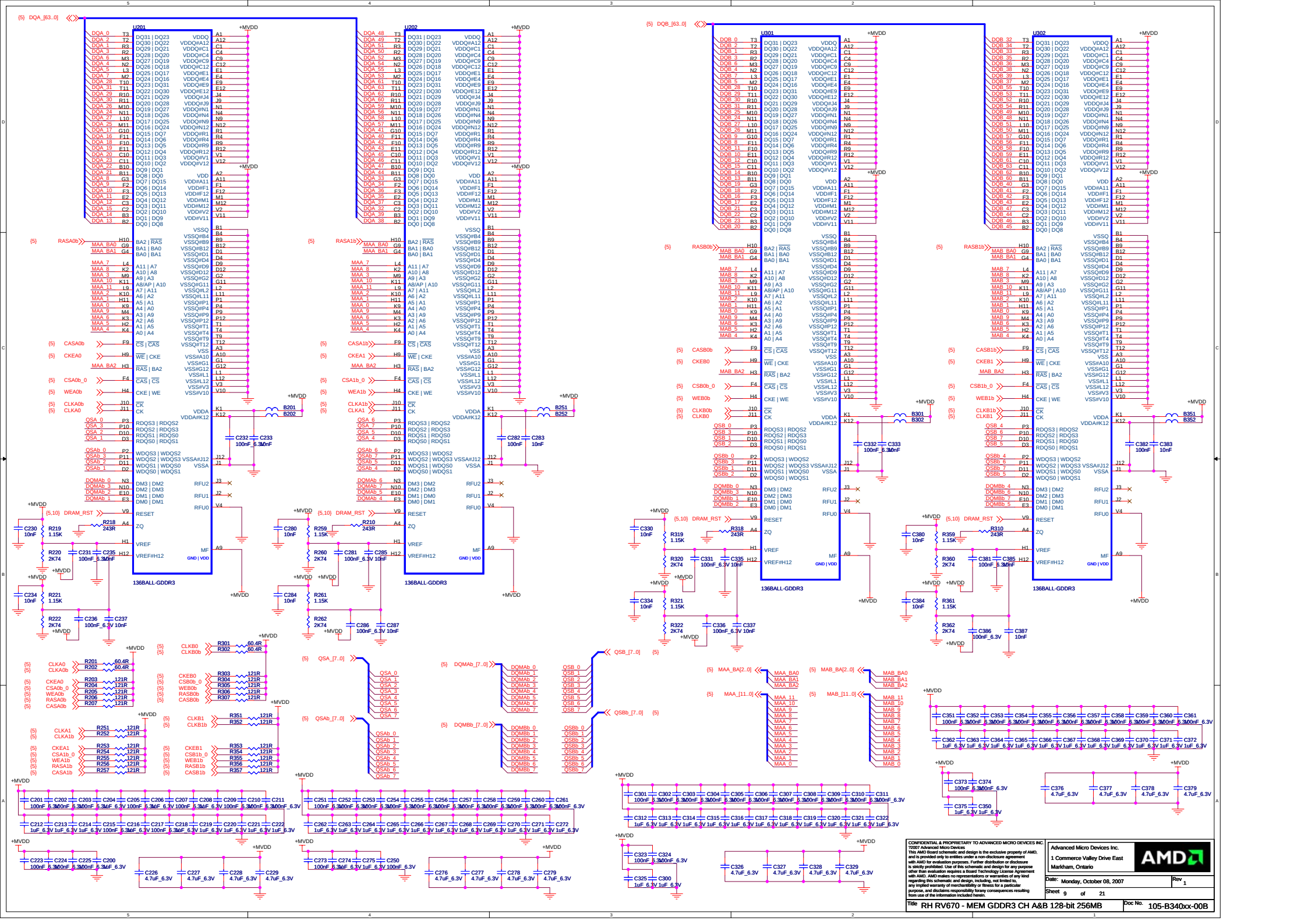
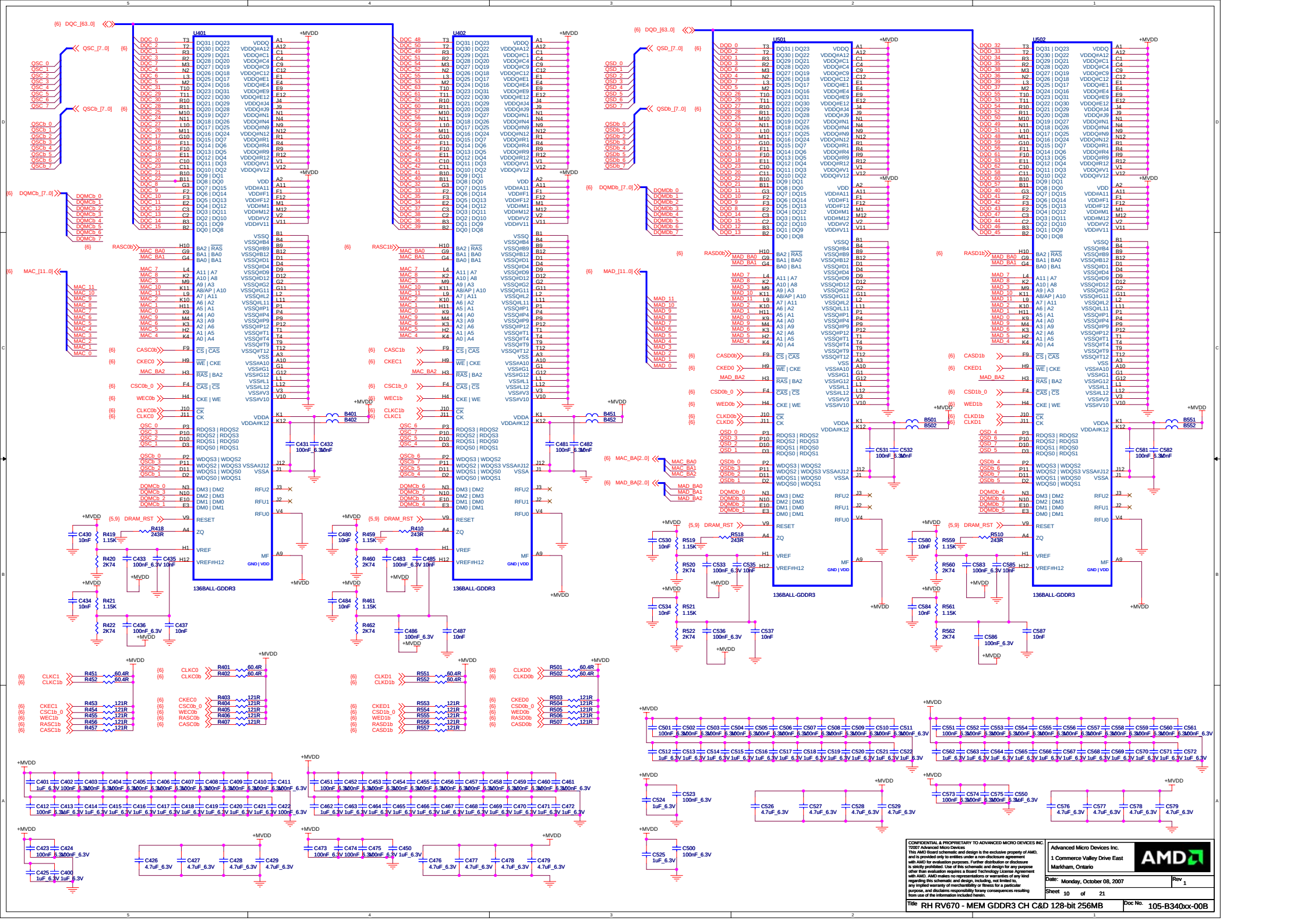
Title RH RV670 - ASIC Grounds

Doc No. 105-B340xx-00B



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Monday, October 08, 2007
Rev	1
Sheet	9 of 21
Title	RH RV670 - MEM GDDR3 CH A&B 128-bit 256MB
Doc No.	105-B340xx-00B


U401
U402
U501
U502
136BALL-GDDR3
+MVDD
DQC_[63..0]
DQD_[63..0]
QSC_[7..0]
QSCb_[7..0]
QSD_[7..0]
QSDb_[7..0]
DQMCb_[7..0]
DQMDb_[7..0]
MAC_[11..0]
MAD_[11..0]
RASC0b
RASC1b
RASD0b
RASD1b
CASC0b
CASC1b
CASD0b
CASD1b
CKEC0
CKEC1
CKED0
CKED1
WEC0b
WEC1b
WED0b
WED1b
CLKC0b
CLKC1b
CLKD0b
CLKD1b
MAC_BA[2..0]
MAD_BA[2..0]
DRAM_RST
RESET
ZQ
VREF
MF
GND | VDD
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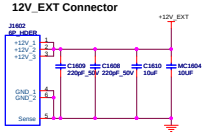
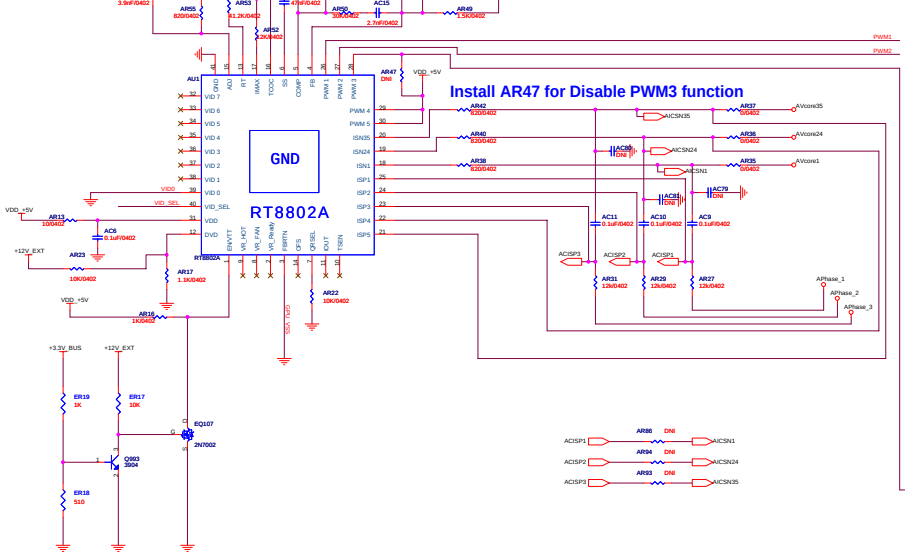
1 Commerce Valley Drive East
Markham, Ontario
Date: Monday, October 08, 2007
Rev 1
Sheet 10 of 21
Title RH RV670 - MEM GDDR3 CH C&D 128-bit 256MB
Doc No. 105-B340xx-00B

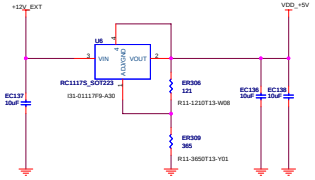
12V_EXT Connector



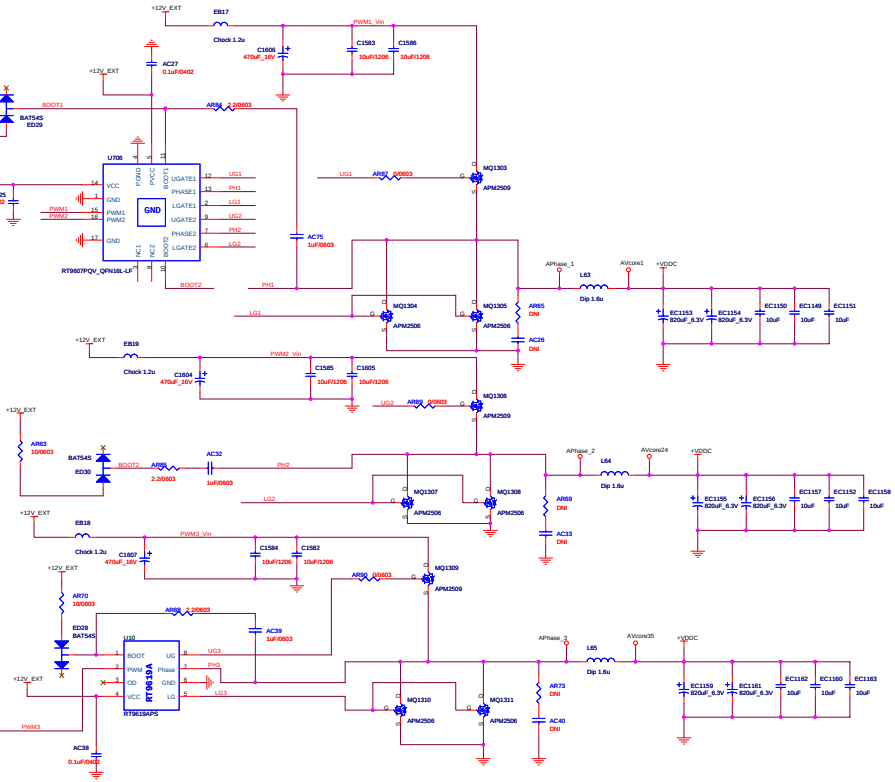
+VDDC=0.8 * (1+ (AR49 / AR82))

Install AR47 for Disable PWM3 function



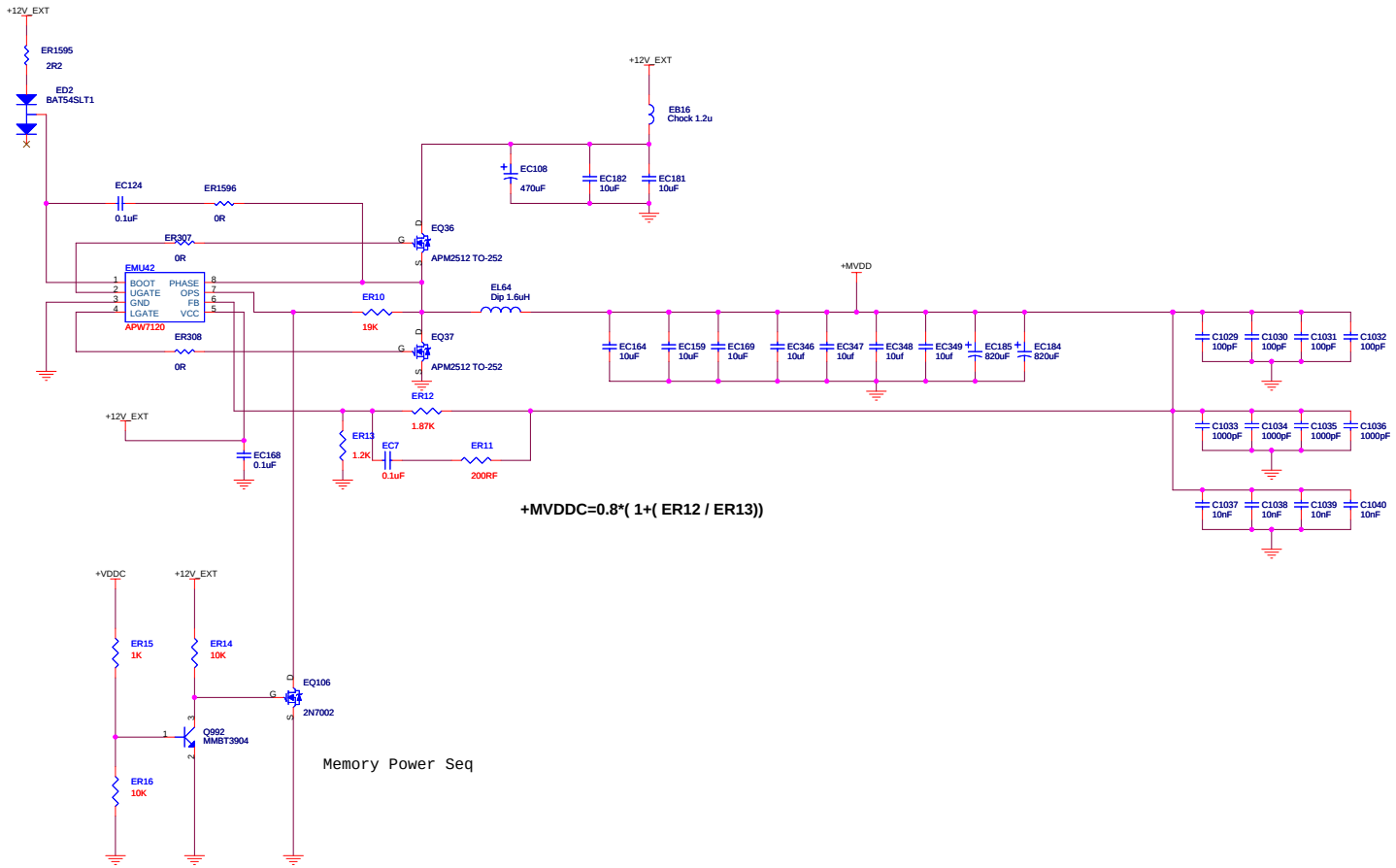


Vout=1.25V* [1+(ER305/ER304)]



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Monday, October 08, 2007 Rev: 1
Sheet 11 of 21
Title: RH RV670 - VDDC SMPS 03
Doc No. 105-B340xx-008



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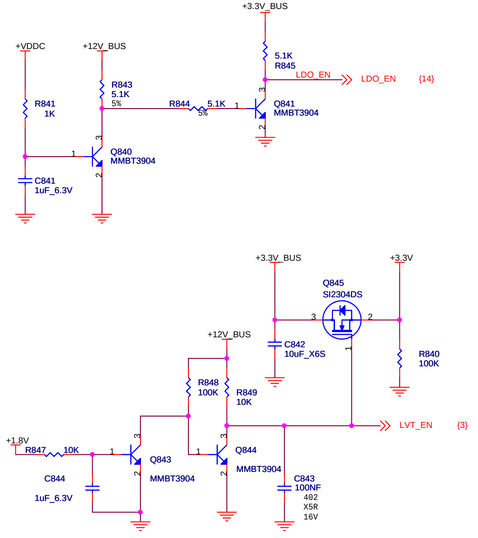
1 Commerce Valley Drive East
Markham, Ontario

Date:	Monday, October 08, 2007
Rev	1
Sheet	12 of 21
Title	RH RV670 - MVDD SMPS 02
Doc No.	105-B340xx-00B

Power up Sequencing



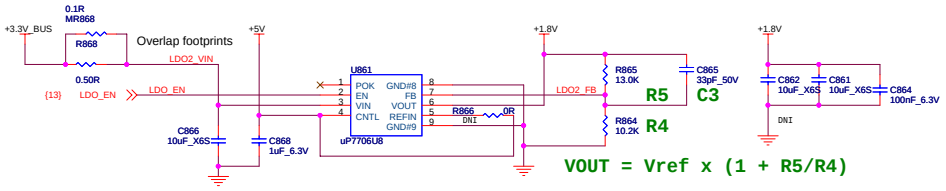
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

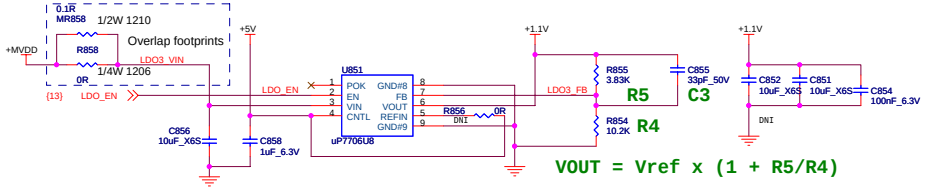
Title	RH RV670 - Power Management		
Title	RV630 GDDR3 - Power Management		
Size	Document Number		Rev
Custom	105-B148xx-00A		1
Doc No.	105-B340xx-00B		A
Date:	Monday, October 08, 2007	Sheet 13 of 21	

Regulators for +5V, +5V_VESA and +5V_VESA2

LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

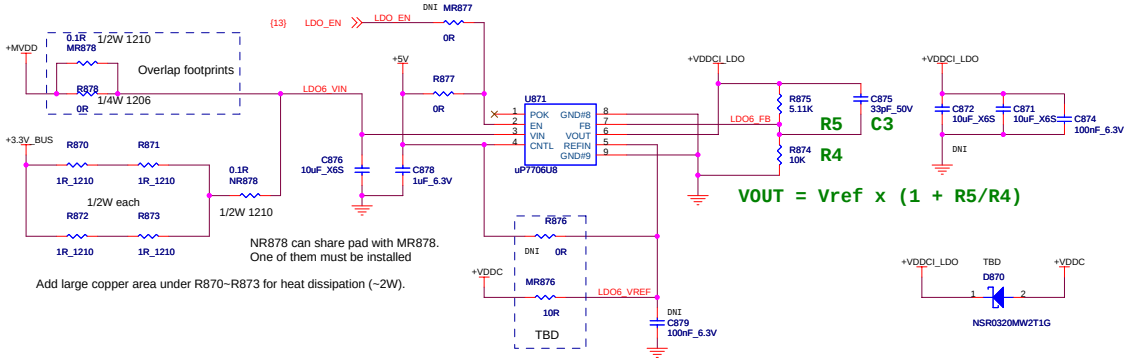


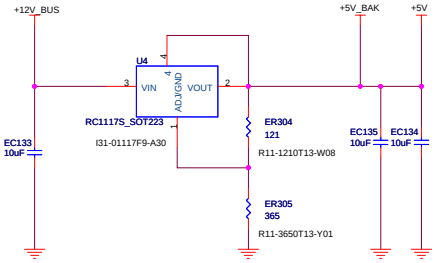
LDO #3: Vin = +1.70V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



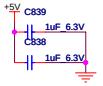
LDO #6: For fixed output voltage: Vin = +1.70V to 2.1V MAX Vout = +1.20V +/- 3% Iout = 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

LDO #6: For tracking VDDC: Vin = TBD Vout = TBD Iout = 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling





Vout=1.25V* [1+(ER305/ER304)]



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Doc No. 105-B340xx-00B

See BOM for qualified filters

{3} A_DAC1_R — R1001 75R 402 — C1004 8.0pF 402 — L1001 47nH ML1001 36NH — C1001 12pF_50V 402

R1027 37.4R

{3} A_DAC1_RB — R1001 75R 402 — C1004 8.0pF 402 — L1001 47nH ML1001 36NH — C1001 12pF_50V 402

{3} A_DAC1_G — R1002 75R 402 — C1005 8.0pF 402 — L1002 47nH ML1002 36NH — C1002 12pF_50V 402

R1028 37.4R

{3} A_DAC1_GB — R1002 75R 402 — C1005 8.0pF 402 — L1002 47nH ML1002 36NH — C1002 12pF_50V 402

{3} A_DAC1_B — R1003 75R 402 — C1006 8.0pF 402 — L1003 47nH ML1003 36NH — C1003 12pF_50V 402

R1029 37.4R

{3} A_DAC1_BB — R1003 75R 402 — C1006 8.0pF 402 — L1003 47nH ML1003 36NH — C1003 12pF_50V 402

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

L100x and ML100x footprints are overlapped

For ESD Protection

D1001 CM1213-04 (CH1, CH2, Vp, Vn, CH3, CH4)

D1002 CM1213-04 (CH1, CH2, Vp, Vn, CH3, CH4)

+3.3V, +5V_VESA, +5V_VESA2, +5V

EF1 0.2A

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

C1010 104pF

MJ1001 G3179C219-005

MJ1001 pin	Signal
1	R
2	G
3	B
11	MS0
12	MS1
4	MS2
15	MS3
9	NC
13	HS
14	VS
5	VSS
6	VSS#6
7	VSS#7
8	VSS#8
10	VSS#10
16	CASE
17	CASE#17

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

{3} DDC1DATA — R1004 10K — R1005 2.2K — Q1001 BSH111 — DDCDATA_DAC1_5V — R1006 33R 402 — DDCDATA_DAC1_R

{3} DDC1CLK — R1007 10K — R1008 2.2K — Q1002 BSH111 — DDCCLK_DAC1_5V — R1009 33R 402 — DDCCLK_DAC1_R

{3,7} HSYNC1 — C1999 100nF_6.3V — U1999A SN74HCT125D — HSYNC_DAC1_B — R1010 10R 402 — HSYNC_DAC1_R

{3,7} VSYNC1 — U1999B SN74HCT125D — VSYNC_DAC1_B — R1011 10R 402 — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

Q1021 MMBT3904 — R1022 10K — HPD_DVI2 — {7} HPD2 — R1023 10K

+5V_VESA

J1001 DVI_CONNECTOR

J1001 pin	Signal
25	CASE
1	TMDS Data2-
2	TMDS Data2+
3	TMDS Data2/4 Shield
4	TMDS Data4-
5	TMDS Data4+
6	DDC Clock
7	DDC Data
8	Analog VSYNC
9	TMDS Data1-
10	TMDS Data1+
11	TMDS Data1/3 Shield
12	TMDS Data3-
13	TMDS Data3+
14	+5V Power
15	GND (for +5V)
16	Hot Plug Detect
17	TMDS Data0-
18	TMDS Data0+
19	TMDS Data0/5 Shield
20	TMDS Data5-
21	TMDS Data5+
22	TMDS Clock Shield
23	TMDS Clock+
24	TMDS Clock-
C1	Analog Red
C2	Analog Green
C3	Analog Blue
C4	Analog HYNC
C5	Analog GND
C6	Analog GND#C6
26	CASE#26
27	CASE#27
28	CASE#28
29	CASE#29
30	CASE#30

{3} T2X2M, {3} T2X2P — TMDS Data2-, TMDS Data2+
{3} T2X4M, {3} T2X4P — TMDS Data4-, TMDS Data4+
DDCCLK_DAC1_R — DDC Clock
DDCDATA_DAC1_R — DDC Data
VSYNC_DAC1_R — Analog VSYNC
{3} T2X1M, {3} T2X1P — TMDS Data1-, TMDS Data1+
{3} T2X3M, {3} T2X3P — TMDS Data1/3 Shield, TMDS Data3-, TMDS Data3+
+5V Power
GND (for +5V)
{3} T2X0M, {3} T2X0P — Hot Plug Detect, TMDS Data0-, TMDS Data0+
{3} T2X5M, {3} T2X5P — TMDS Data0/5 Shield, TMDS Data5-, TMDS Data5+
{3} T2XCP, {3} T2XCM — TMDS Clock Shield, TMDS Clock+, TMDS Clock-
A_R_DAC1_F — Analog Red
A_G_DAC1_F — Analog Green
A_B_DAC1_F — Analog Blue
HSYNC_DAC1_R — Analog HYNC
Analog GND
Analog GND#C6

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Title: RH RV670 - DAC1/TMDS2 | Doc No. 105-B340xx-00B

See BOM for qualified filters

{3} A_DAC2_R
{3} A_DAC2_RB
{3} A_DAC2_G
{3} A_DAC2_GB
{3} A_DAC2_B
{3} A_DAC2_BB

R2027 37.4R
R2028 37.4R
R2029 37.4R

R2001 75R 402
R2002 75R 402
R2003 75R 402

C2004 8.0pF 402
C2005 8.0pF 402
C2006 8.0pF 402

L2001 47nH
ML2001 36NH
L2002 47nH
ML2002 36NH
L2003 47nH
ML2003 36NH

C2001 12pF_50V 402
C2002 12pF_50V 402
C2003 12pF_50V 402

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

L200x and ML200x footprints are overlapped

+3.3V
+5V_VESA2

D2001
D2002
CM1213-04
CM1213-04

CH3 CH2 Vp Vn CH4 CH1

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R

MJ2001
R G B MS0 MS1 MS2 MS3 NC HS VS VSS VSS#6 VSS#7 VSS#8 VSS#10 CASE CASE#17
G3179C219-005

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

{3} DDC2DATA
{3} DDC2CLK

R2004 10K
R2007 10K
R2005 2.2K 402 DDCDATA_DAC2_5V
R2008 2.2K 402 DDCCLK_DAC2_5V
R2006 33R 402 DDCDATA_DAC2_R
R2009 33R 402 DDCCLK_DAC2_R

Q2001 BSH111
Q2002 BSH111

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

{3,7} HSYNC2
{3,7} VSYNC2

U1999C SN74HCT125D
U1999D SN74HCT125D

HSYNC_DAC2_B
VSYNC_DAC2_B
R2010 10R 402 HSYNC_DAC2_R
R2011 10R 402 VSYNC_DAC2_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

+3.3V
Q2021 MMBT3904
R2022 10K
HPD_DVI1
{3} HPD1
R2023 10K

{3} T1X2M {3} T1X2P
{3} T1X4M {3} T1X4P
{3} T1X1M {3} T1X1P
{3} T1X3M {3} T1X3P
{3} T1X0M {3} T1X0P
{3} T1X5M {3} T1X5P
{3} T1XCP {3} T1XCM

DDCCLK_DAC2_R
DDCDATA_DAC2_R
VSYNC_DAC2_R
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
HSYNC_DAC2_R

+5V_VESA2
J2001
CASE
TMDS Data2-
TMDS Data2+
TMDS Data2/4 Shield
TMDS Data4-
TMDS Data4+
DDC Clock
DDC Data
Analog VSYNC
TMDS Data1-
TMDS Data1+
TMDS Data1/3 Shield
TMDS Data3-
TMDS Data3+
+5V Power
GND (for +5V)
Hot Plug Detect
TMDS Data0-
TMDS Data0+
TMDS Data0/5 Shield
TMDS Data5-
TMDS Data5+
TMDS Clock Shield
TMDS Clock+
TMDS Clock-
Analog Red
Analog Green
Analog Blue
Analog HYNC
Analog GND
Analog GND#C6
CASE#26
CASE#27
CASE#28
CASE#29
CASE#30
DVI_CONNECTOR

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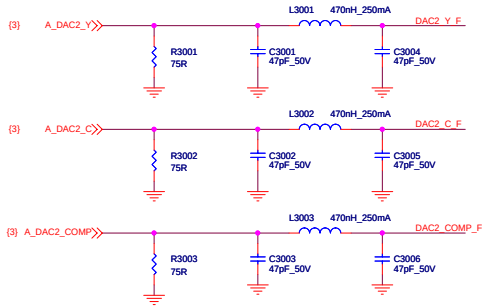

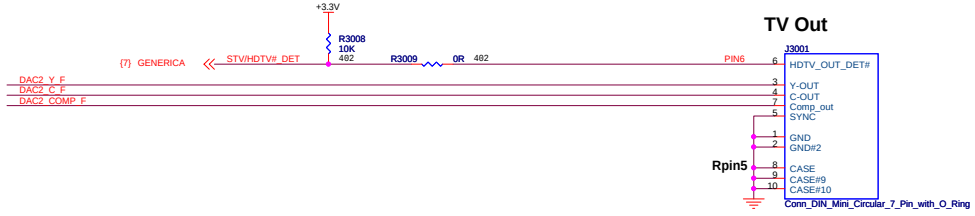

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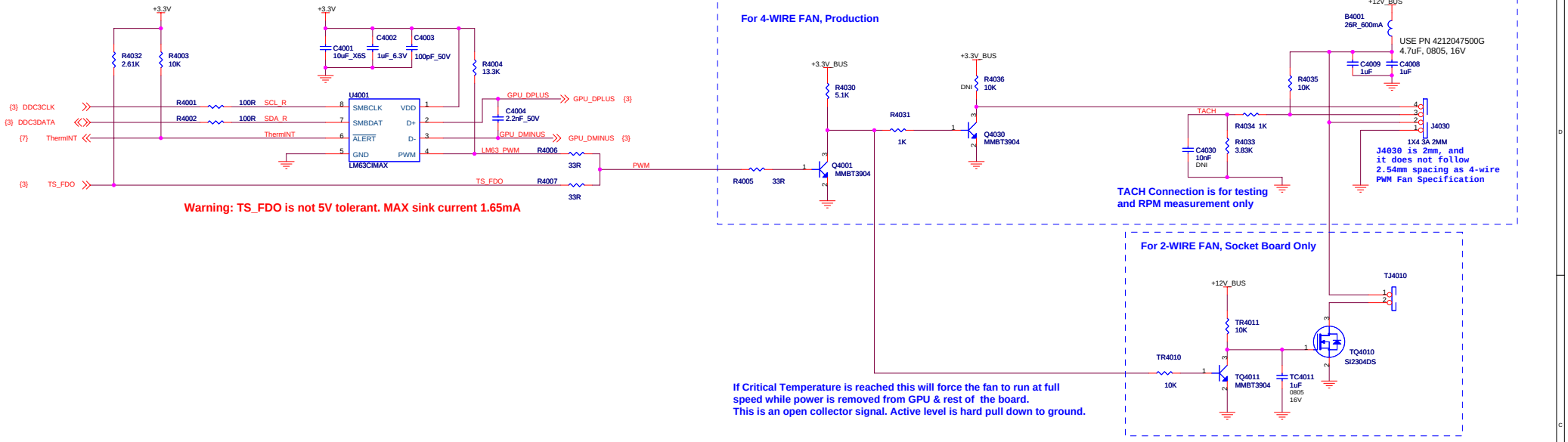
Title RH RV670 - TV OUT | Doc No. 105-B340xx-00B



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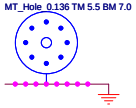
Title: RH RV670 - Thermal Management | Doc No. 105-B340xx-00B

MT1
MT_Hole_0.136 TM 5.5 BM 7.0



SK1

Socket_RV670/M88L

PCB1

PCB

109-B34031-00B

ASSY1

ANTISTATIC BAG

6_X_11

BKT1

BRACKET

8020038600G

FM1
SW_FB

FM2
SW_FB

FM3
SW_FB

FM4
SW_FB

FM5
SW_FB

FM6
SW_FB

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<variant_name>

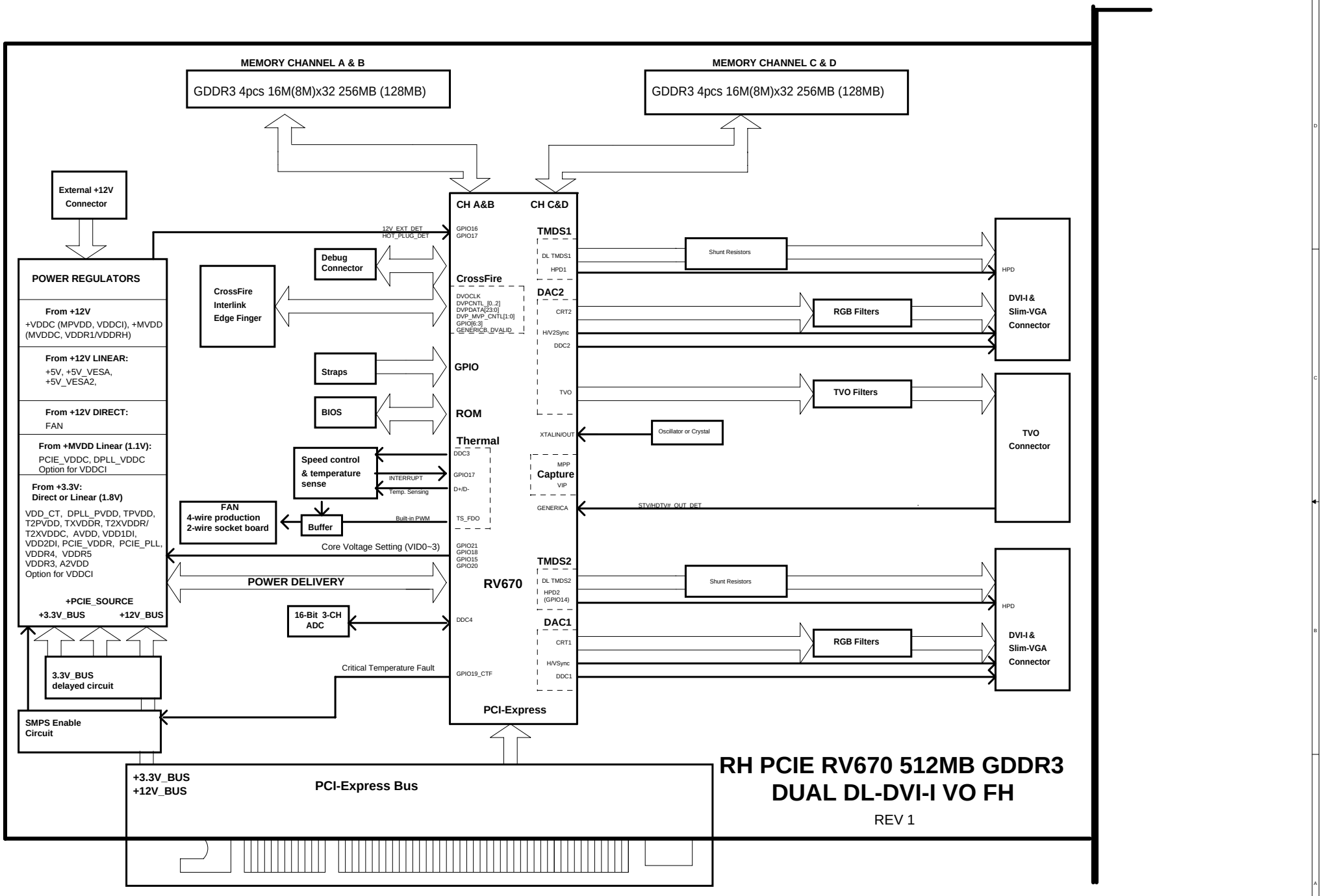
Title	Schematic No.	Date:
RH PCIE RV670 512MB GDDR3 DUAL DL-DVI-I VO FH	105-B340xx-00B	Friday, October 05, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/05/11	Initial design for RV670 GDDR3 (Revival) based on B339
1	00B	07/08/1	(pg 1) Adding R1 and connecting switch #7 of TSW1. Some mother boards require B7 to be grounded. Table-1 updated accordingly (pg 7) Adding R64 and MR64 to select HOT_PLUG_DET or ThermINT as the interrupt source. (pg 13) Adding R1617, MR1617, R1616, Q1613, R1615, R1618, and R1619 as option to support hot plug detection of external cable. (pg 13) Adding R1282, MR1282, R1283, MR1283, R1284, MR1284, R1281, R1285, Q1280, and C1280 as option for thermal protection for VDDC SMPS MOSFETs (pg 13) Adding MC1603 (overlapped with C1603) (pg 14) Adding D870 as option for power up sequencing (pg 18) Adding heatsink symbol/footprint (Layout) Increasing spacing between DDC4DATA & DDC4CLK going to U1270 to reduce the crosstalk



RH PCIE RV670 512MB GDDR3
DUAL DL-DVI-I VO FH

REV 1

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