

P403-A01 DESIGN -- G84-200, 256 MB DDR2,DVI-I, VGA, HDTV

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REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10403-0000-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0010	600-10403-0010-100	P403-A01 G84-200-450400MHz 256MB 16Mx16 BCABA CDDR2 DVI-I+VGA+HDTV CLU
2	SKU0001	600-10403-0001-100	P403-A01 G84-200-450400MHz 256MB 16Mx16 BCABA CDDR2 DVI-I+VGA+HDTV CLU
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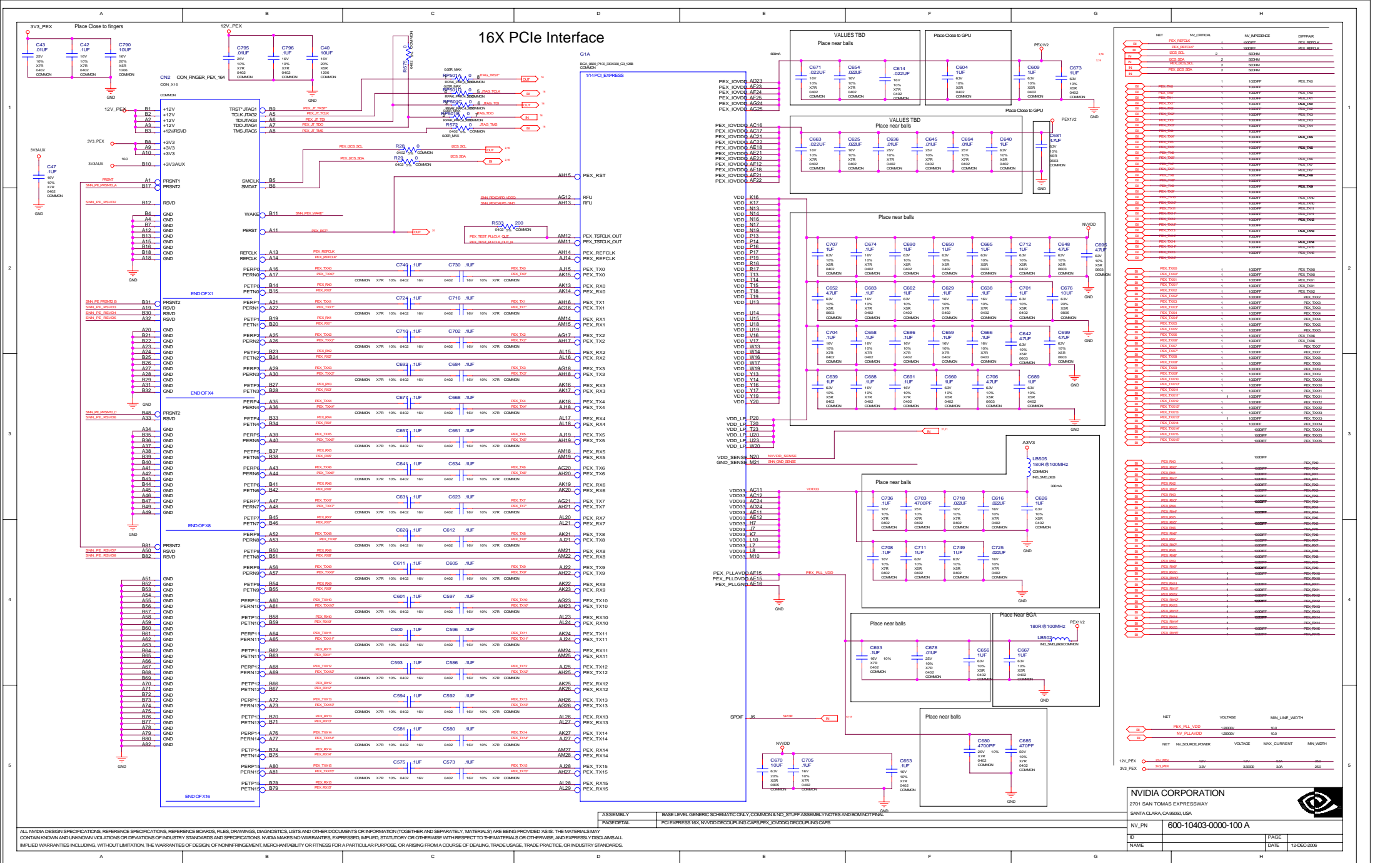
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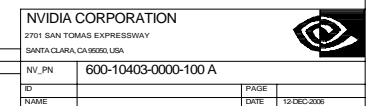
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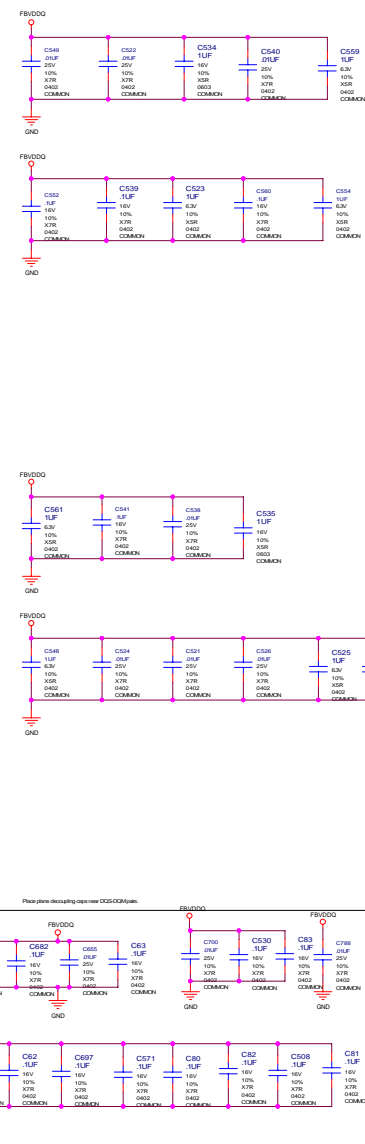
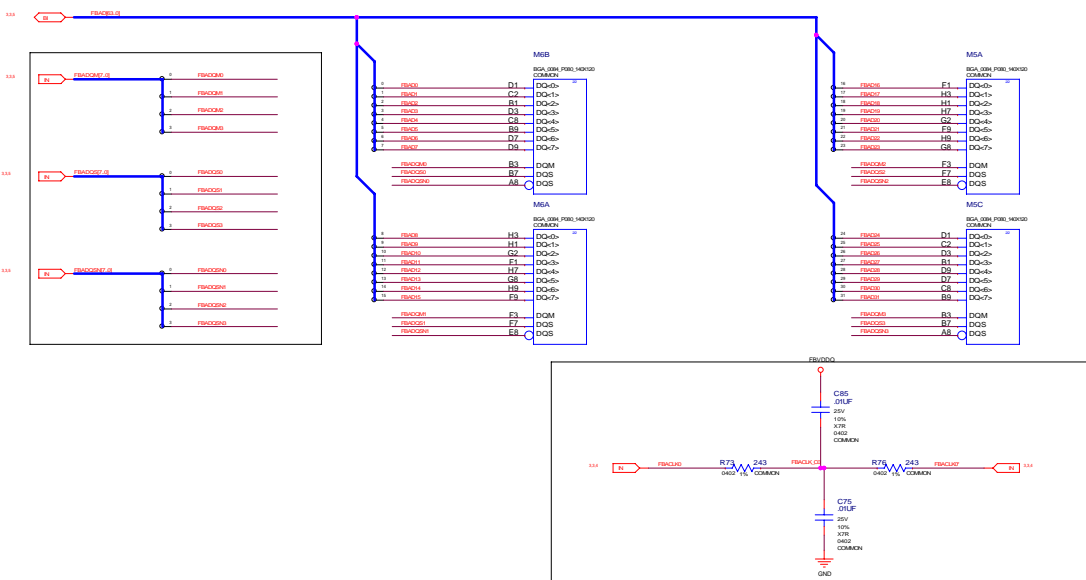
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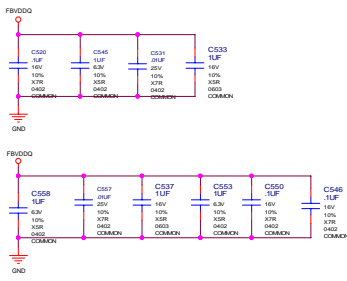
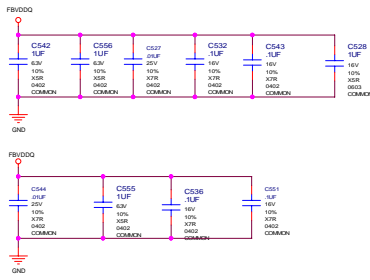
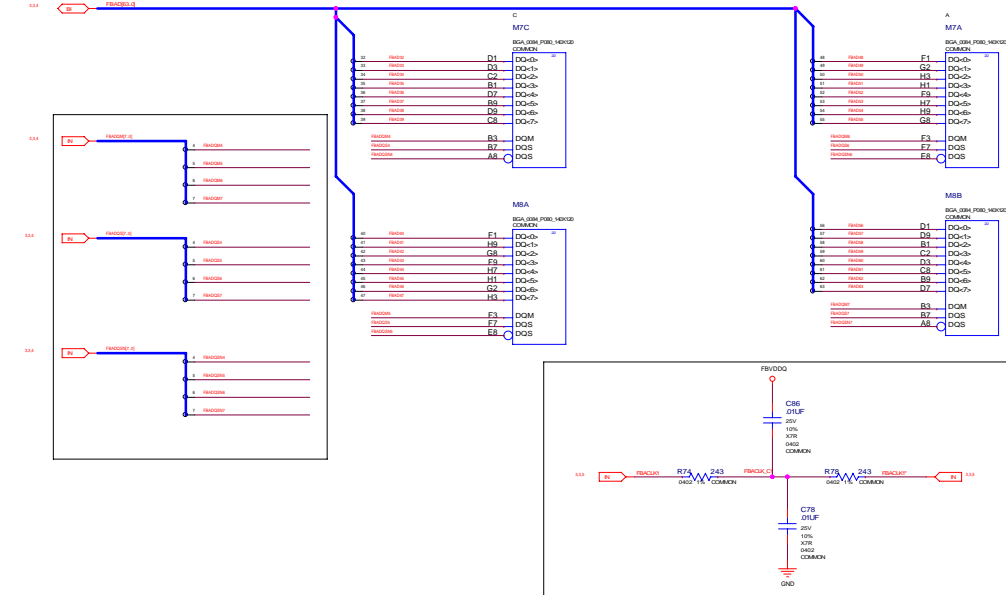
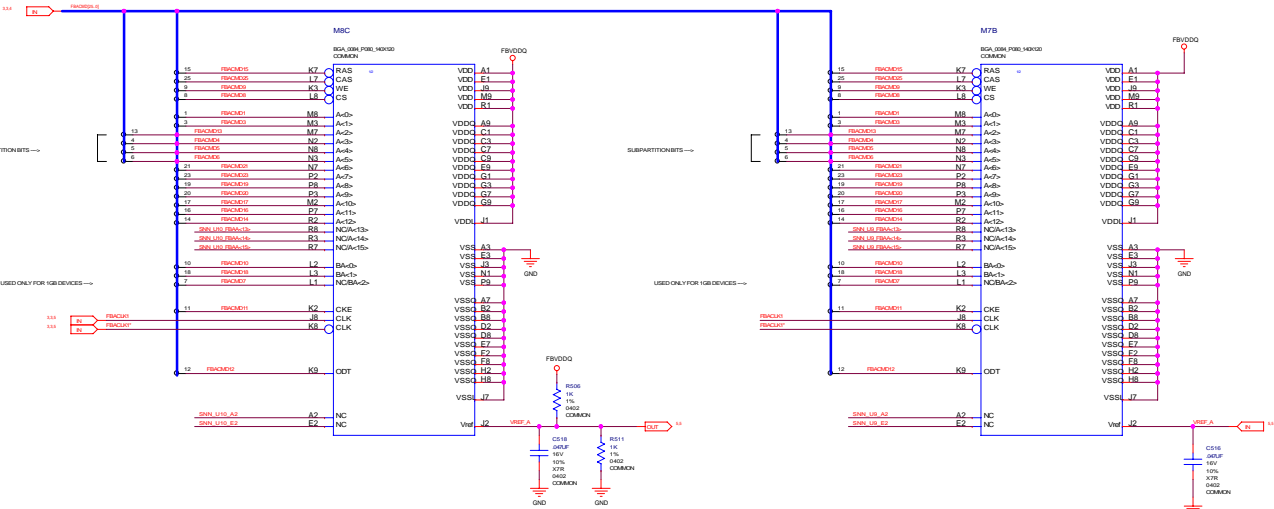
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FBA MEMORY 1st bank 32..63

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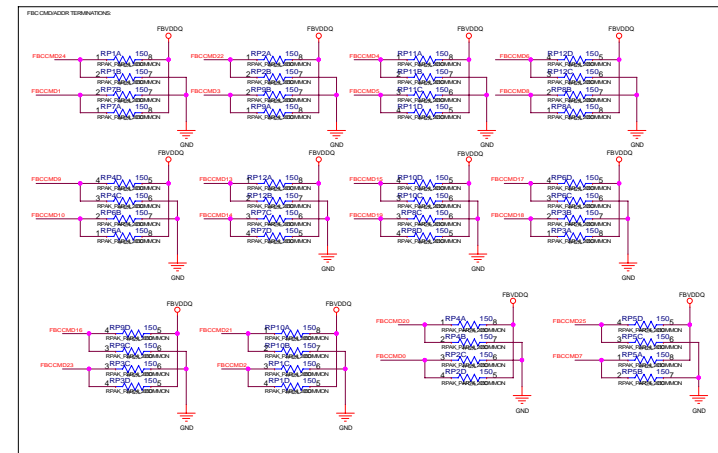
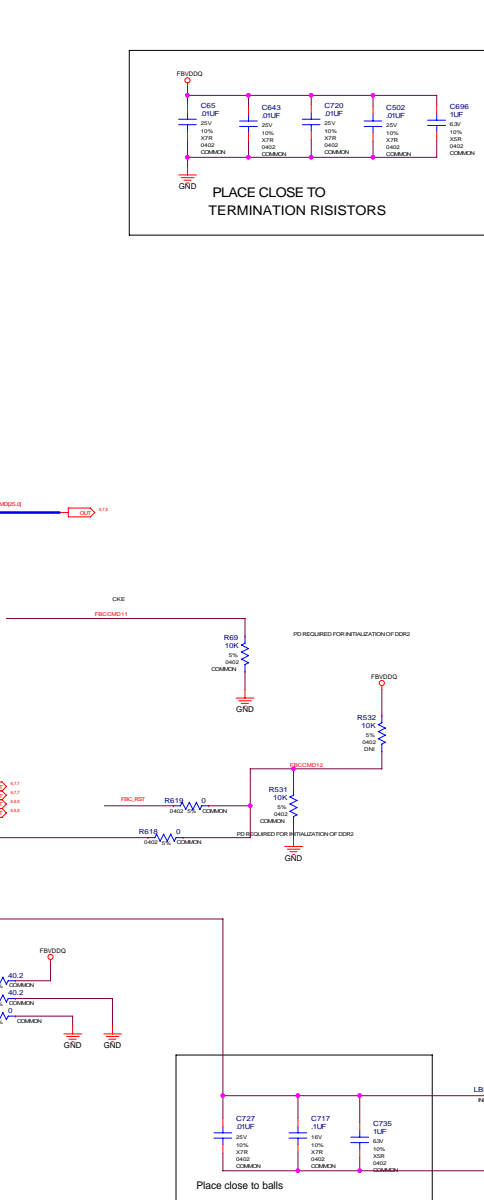
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PAGE DETAIL	FBA 10M1C DQ2 MEMORIES, 1ST BANK 32..63

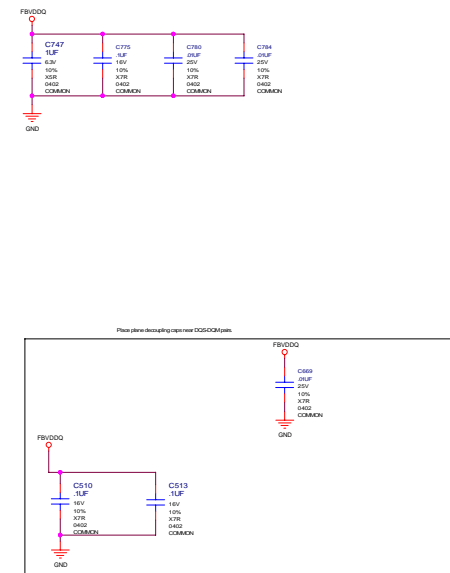
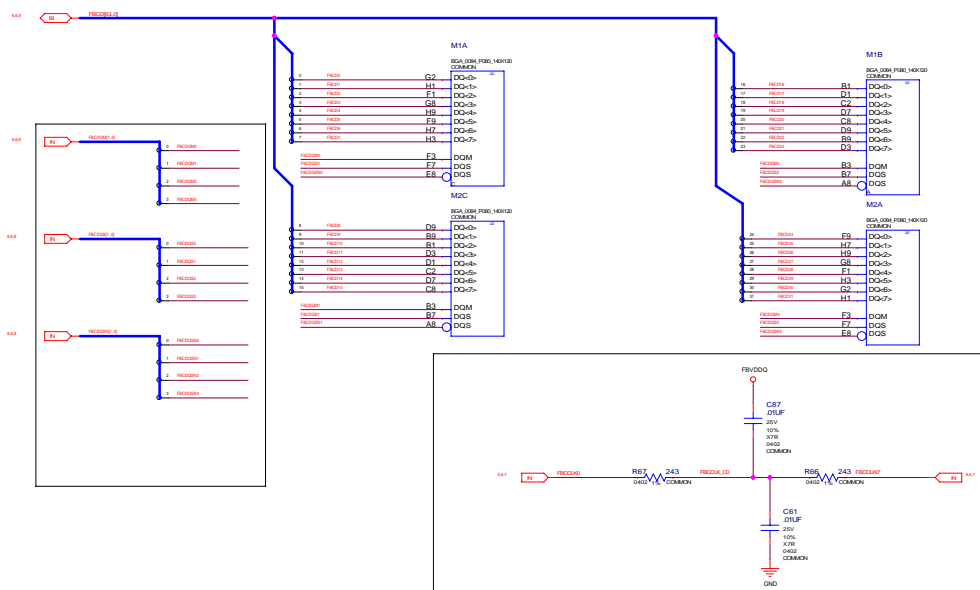
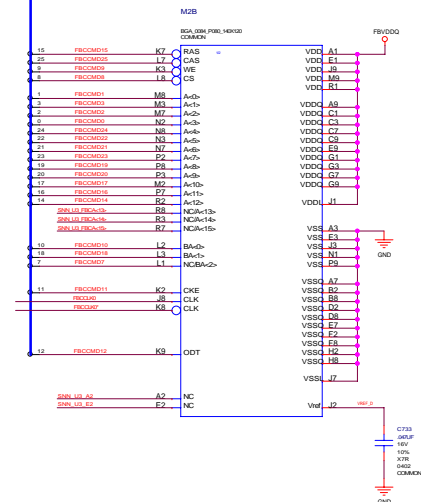
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DATA	FRIC MEMORY INTERFACE, GPU/FB/TT, FRM000

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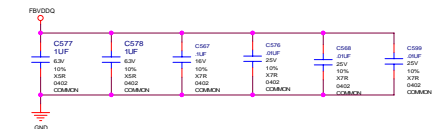
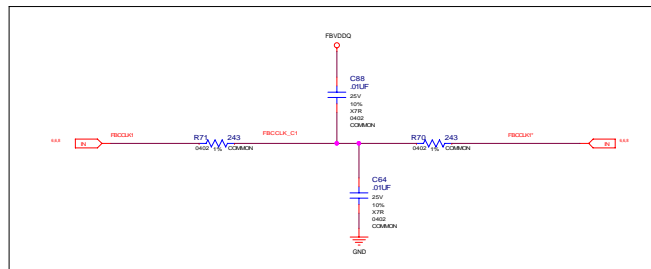
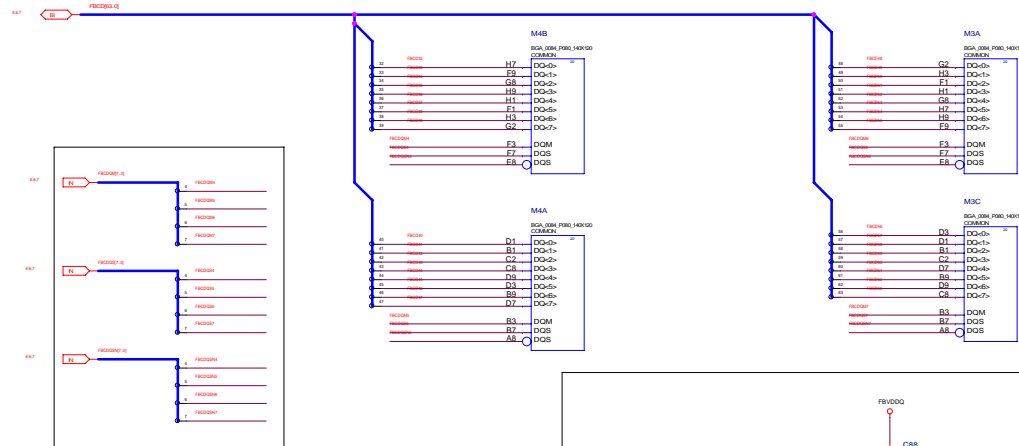
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE/DETAIL	FBC 16MX16 DDR2 MEMORIES, 2ND BANK 0.31

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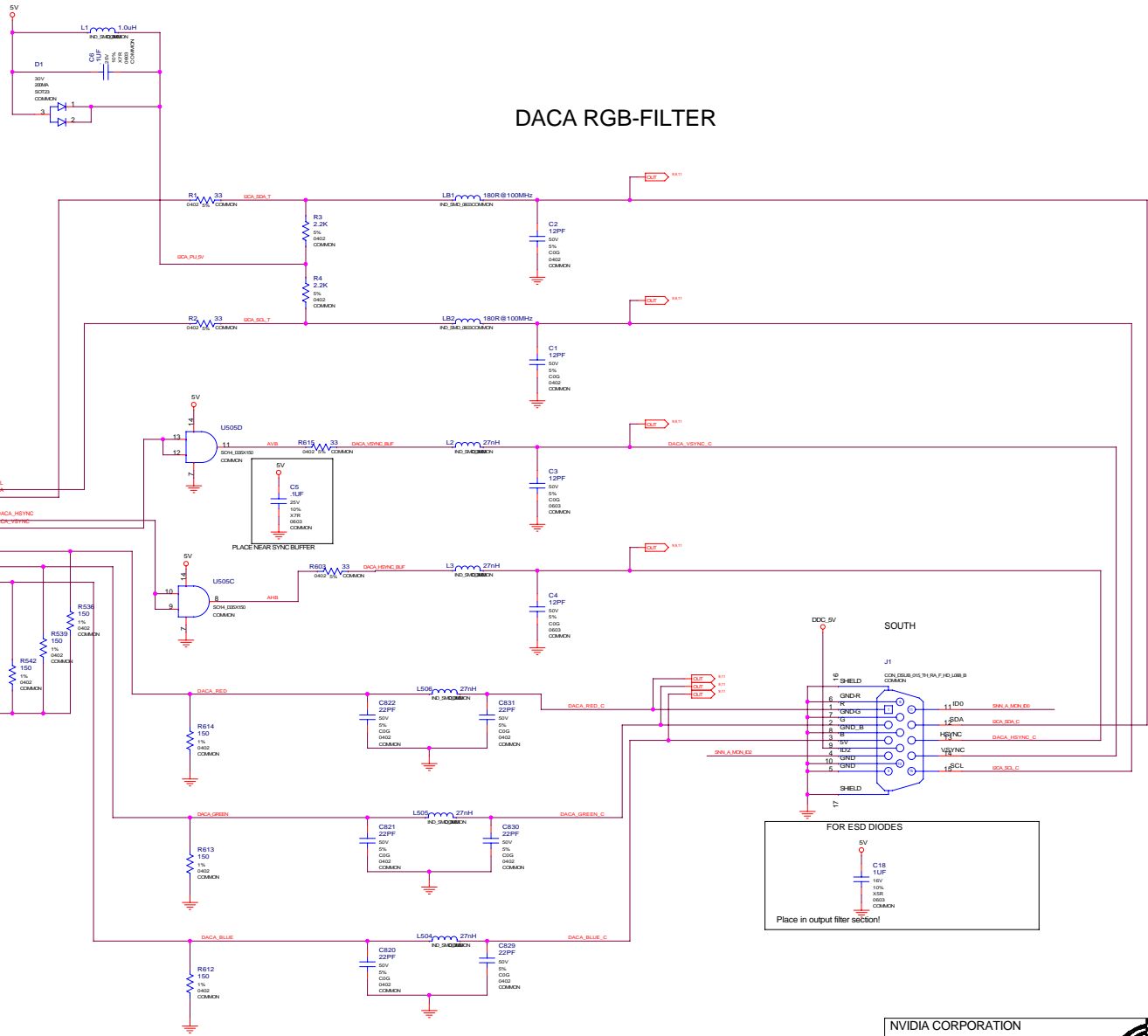
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PAGE DETAIL	FBC 16Mx16 DDR2 MEMORIES, 2ND BANK (32.63)



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98	0	0	0
99	0	0	0
100	0	0	0

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
SI	DACA_VDD	3.30000V	0.07A	16.0
SI	DACA_VREF			10.0
SI	DACA_RESET			10.0

Primary Display (DACA), Slim DB15



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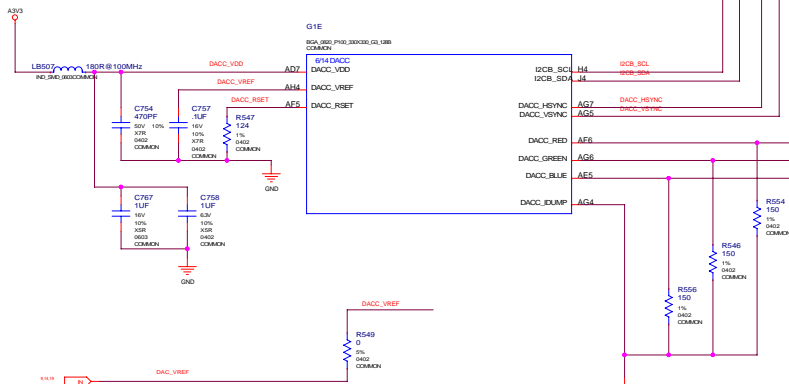
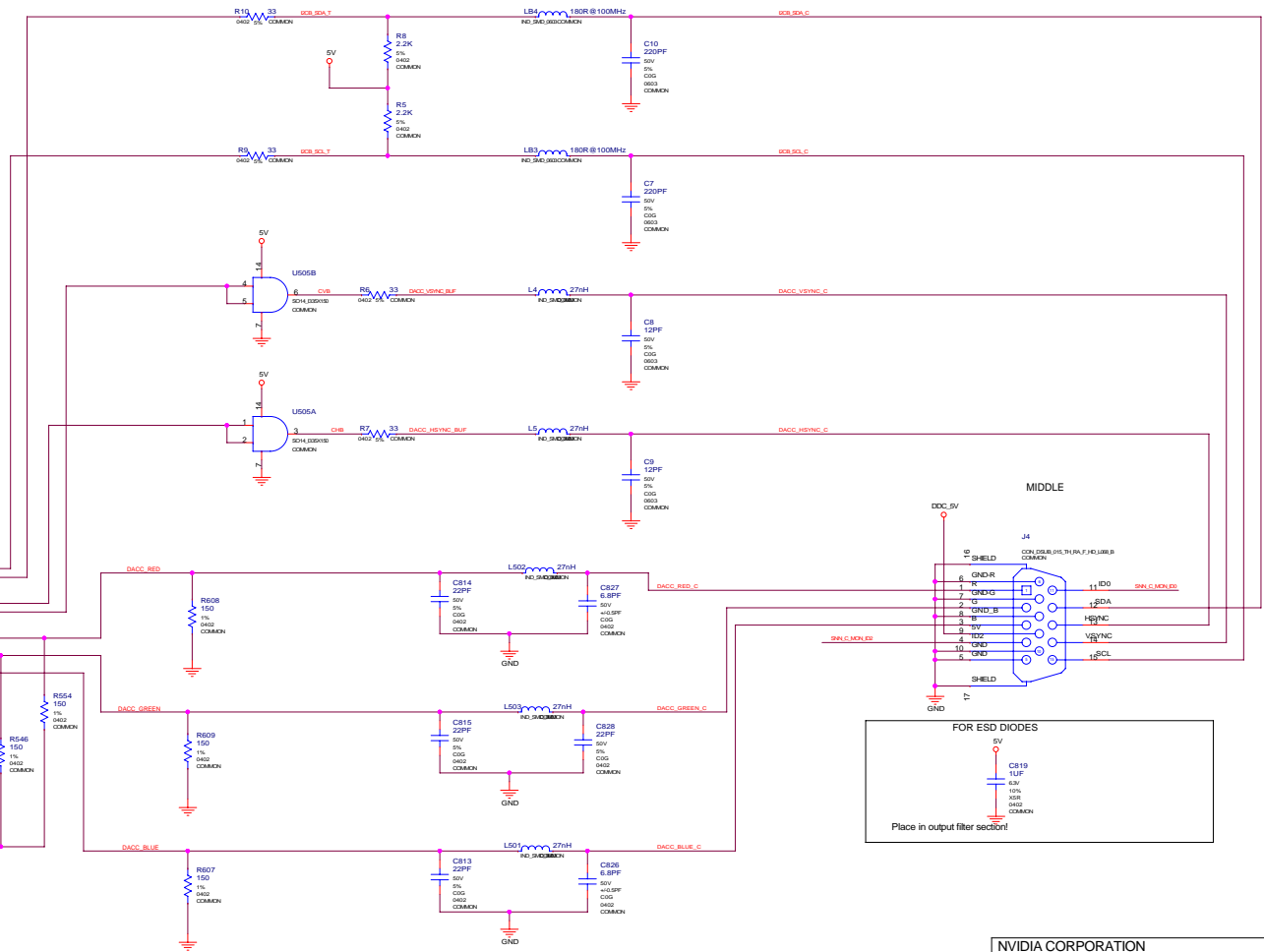
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NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
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Secondary Display (DACC), DB15

DACC RGB-FILTER



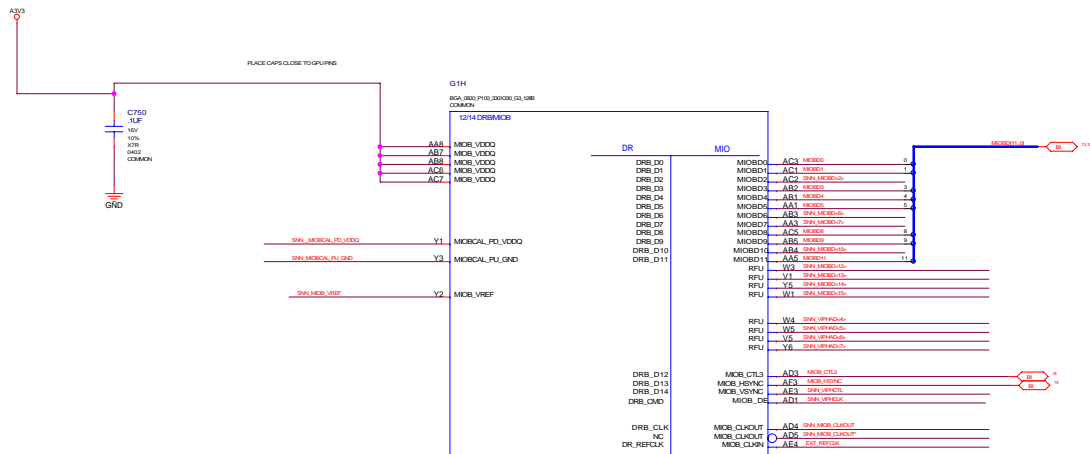
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## G3 VIP/MIOB



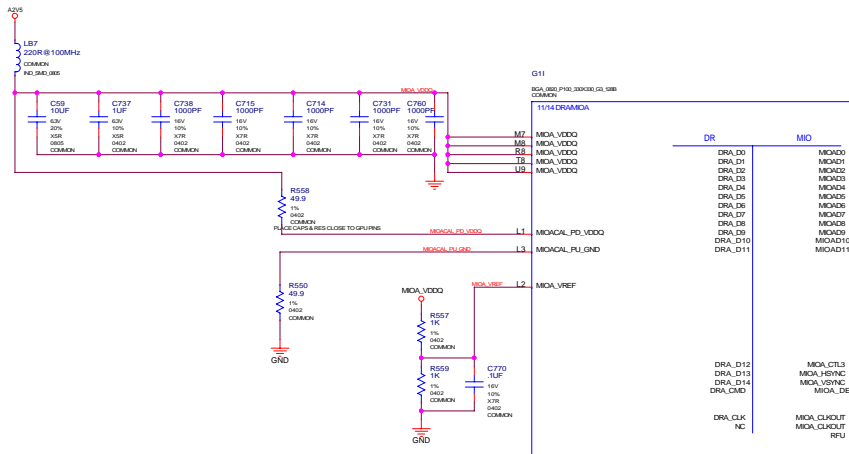
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12V4	2	50OHM	
EXT_REFCLK	2	50OHM	
MIOB_CLKOUT	2	50OHM	
MIOB_CLKIN	2	50OHM	
12V4	2	50OHM	
SPDIO1_B1_SYNC	2	50OHM	
12V4	2	50OHM	

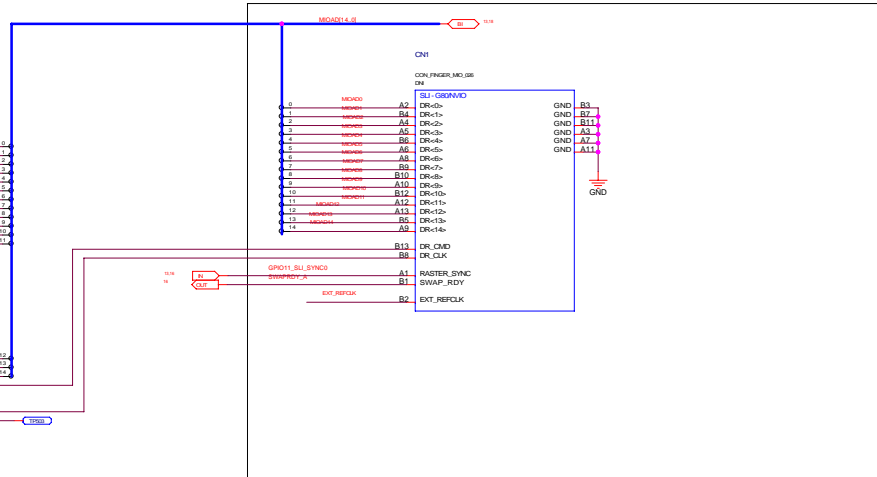
  

NET	VOLTAGE	MAX_CURRENT	MIN_LENGTH
MIOB_VDDQ	1.2V	0.8A	12.0
MIOB_VREF	1.2V	0.8A	12.0
MIOBAL_PU_VDDQ	1.2V	0.8A	12.0
MIOBAL_PU_GND	1.2V	0.8A	12.0

## G3 MIOA



## SLI Connector



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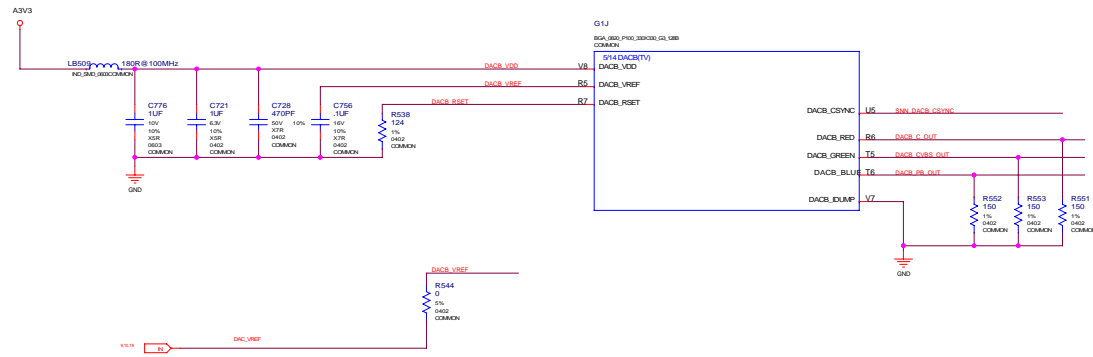
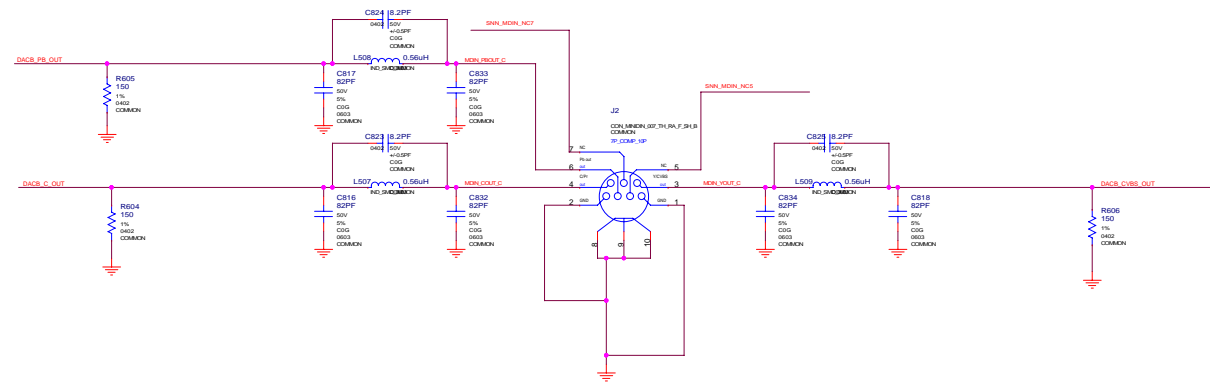
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PAGE DETAIL MIOA & MIOB

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## DACB .. MiniDIN VIDEO OUT CONNECTOR

## DACB NET RULES

NET		NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
D1	DACB_C_OUT	1	50OHM	
D2	MDIN_COUT_C	1	50OHM	
D3	DACB_CVDS_OUT	1	50OHM	
D4	MDIN_COUT_C	1	50OHM	
D5	DACB_PL_OUT	1	50OHM	
D6	MDIN_COUT_C	1	50OHM	
D7	MDIN_PLD	2	50OHM	
D8	MDIN_PLD-C	2	50OHM	
D9				
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH	
D10	DACB_VDD	3.3000V	0.07A	16.0
D11	DACB_PSEF			16.0
D12	DACB_PSEF			16.0



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, SYNC STRIPPER, MINIDIN CONNECTOR NORTH/HDTV HEADER

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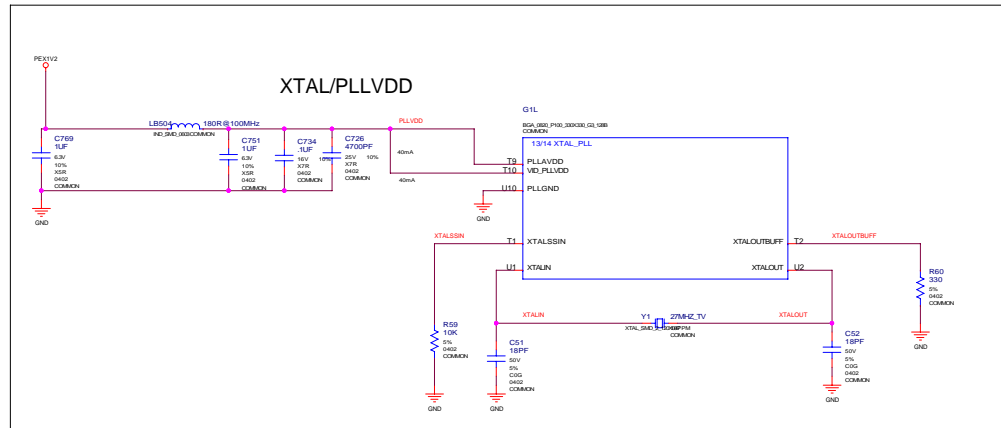
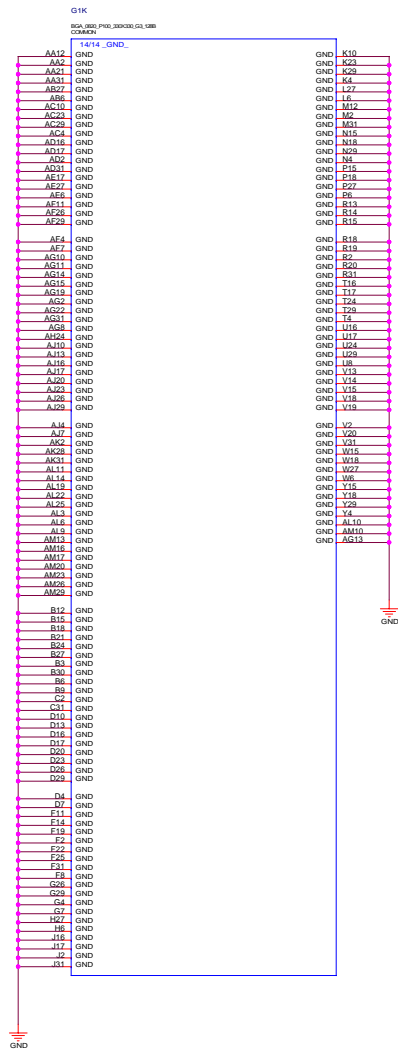
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## GPU GND CONNECTION, XTAL



	NET	INV_CRITICAL	INV_AMPEDANCE	DIFFPAIR
R1	STATUS	1	300M	
R2	STATUSOUT	1	300M	
	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
R1	PLUUSD	12V	0.3A	12MIL

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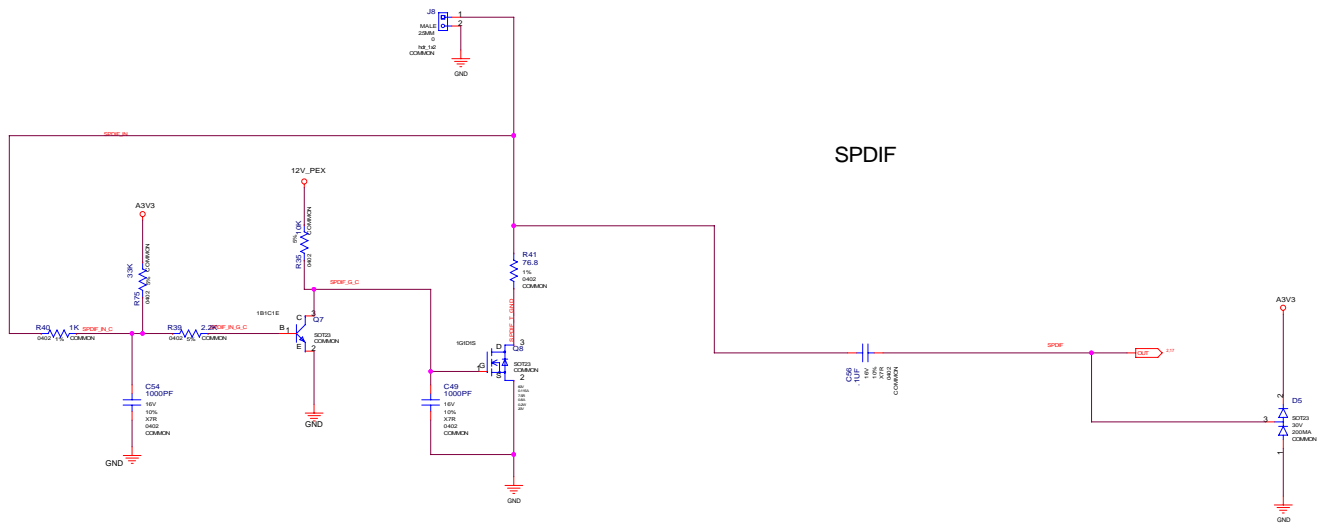
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PAGE DETAIL	GPU GND CONNECTION, XTAL



SPDIF

SPDIF



place close to GPU

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND CHECKLIST FINAL
PAGE DETAIL	SPDIF

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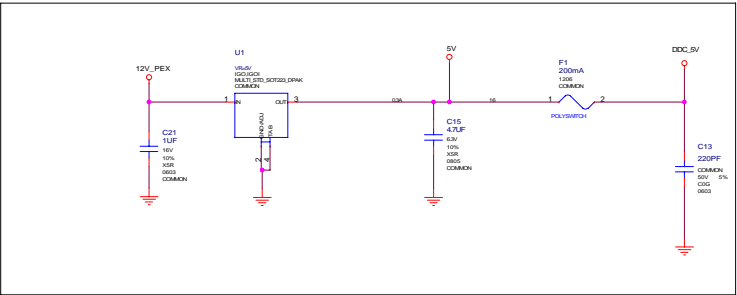
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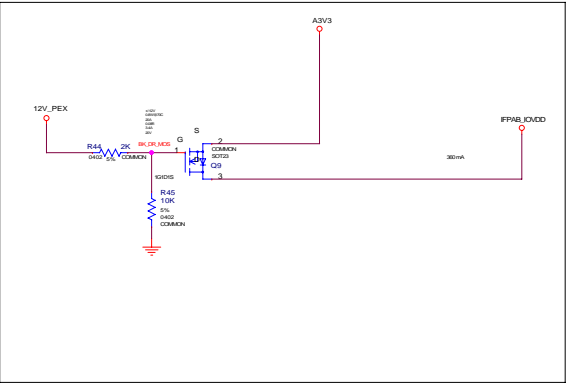


Power SupplyI:TMDS\_IOVDD A3V3 DDC\_5V IFP\_PLLVDD

DDC 5V



TMDS IO SUPPLY WITH BACKDRIVE PROTECTION

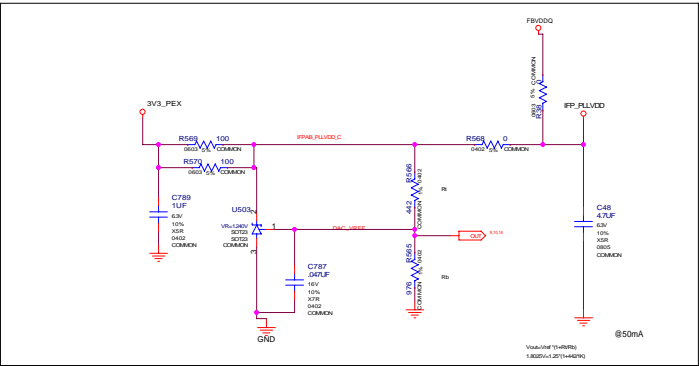


NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE	
DDC_5V	DDC_5V	0.1A	120	5.00000
A3V3	A3V3	1.5A	300	3.3
IFPAB_IOVDD	IFPAB_IOVDD	0.0A	10.0A	3.00000
	GND		250	0.00000
IFP_PLLVDD	IFP_PLLVDD	0.0A	10.0A	1.00000

A3V3 Power Supply



IFP\_PLL SUPPLY



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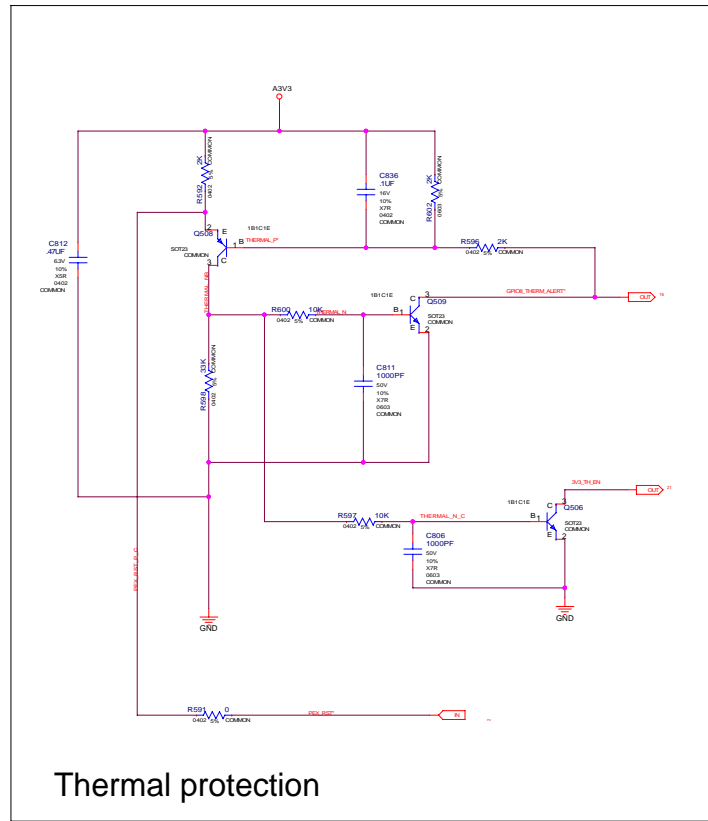
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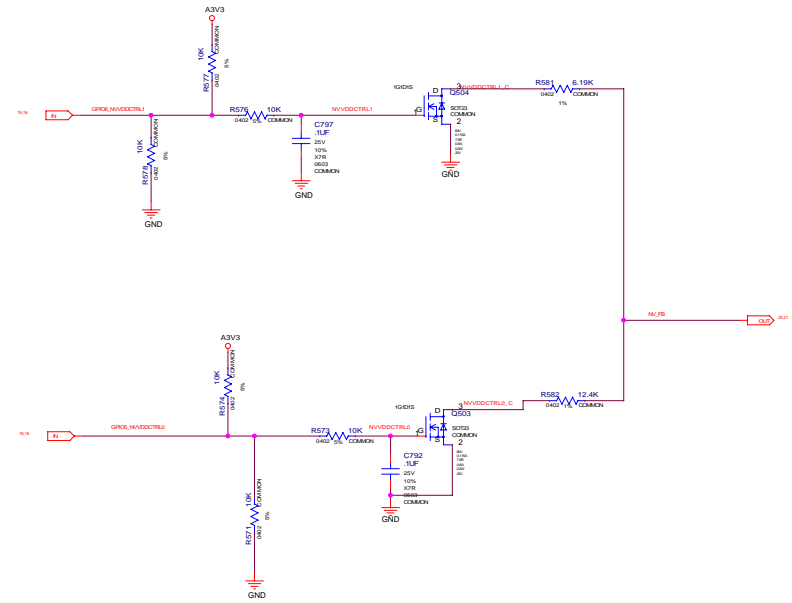
DATE

12 DEC 2006

## Thermal protection



## dynamic NVVDD



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PAGE DETAIL	thermal protection and dynamic NVDD

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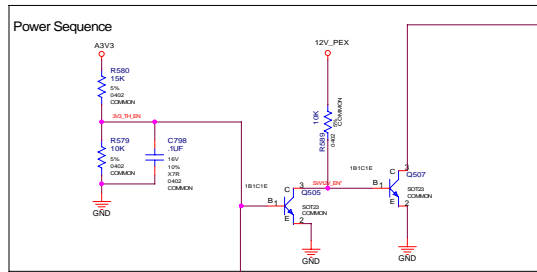
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## PowerSupplyII: NVVDD, 2.5V

A2V5

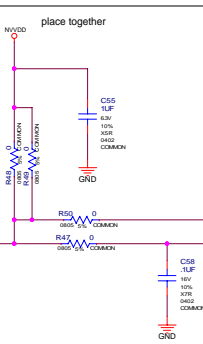
$V_{out} = V_{Ref} \cdot (1 + R_{top}/R_{bot})$   
 $2.52V = 0.8V \cdot (1 + (2.26k/1.05k))$  (ISL6549)



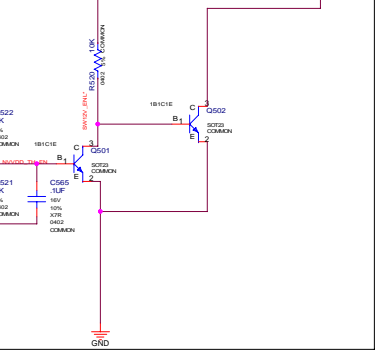
# PowerSupplyIII: FBVDDQ, PEX1V2

## PEX1V2

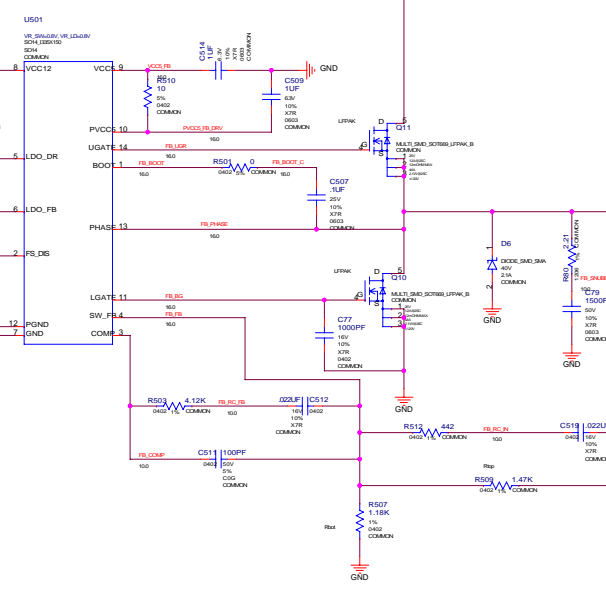
$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$   
 $1.227V = 0.8V * (1 + (1.65K/3.09K))$  (ISL6549)



## Power Sequence

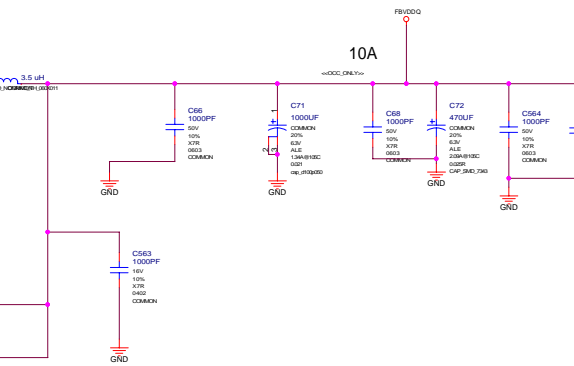


## ISL6549



Net Name	LINE_WIDTH	CURRENT	Voltage
FBVDDQ	100	1000	1.227V

FBVDDQ:  
 $V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$   
 $1.796V = 0.8V * (1 + (1.47K/1.18K))$  (ISL6549)  
 $2.005V = 0.8V * (1 + (1.47K/0.976K))$  (ISL6549)



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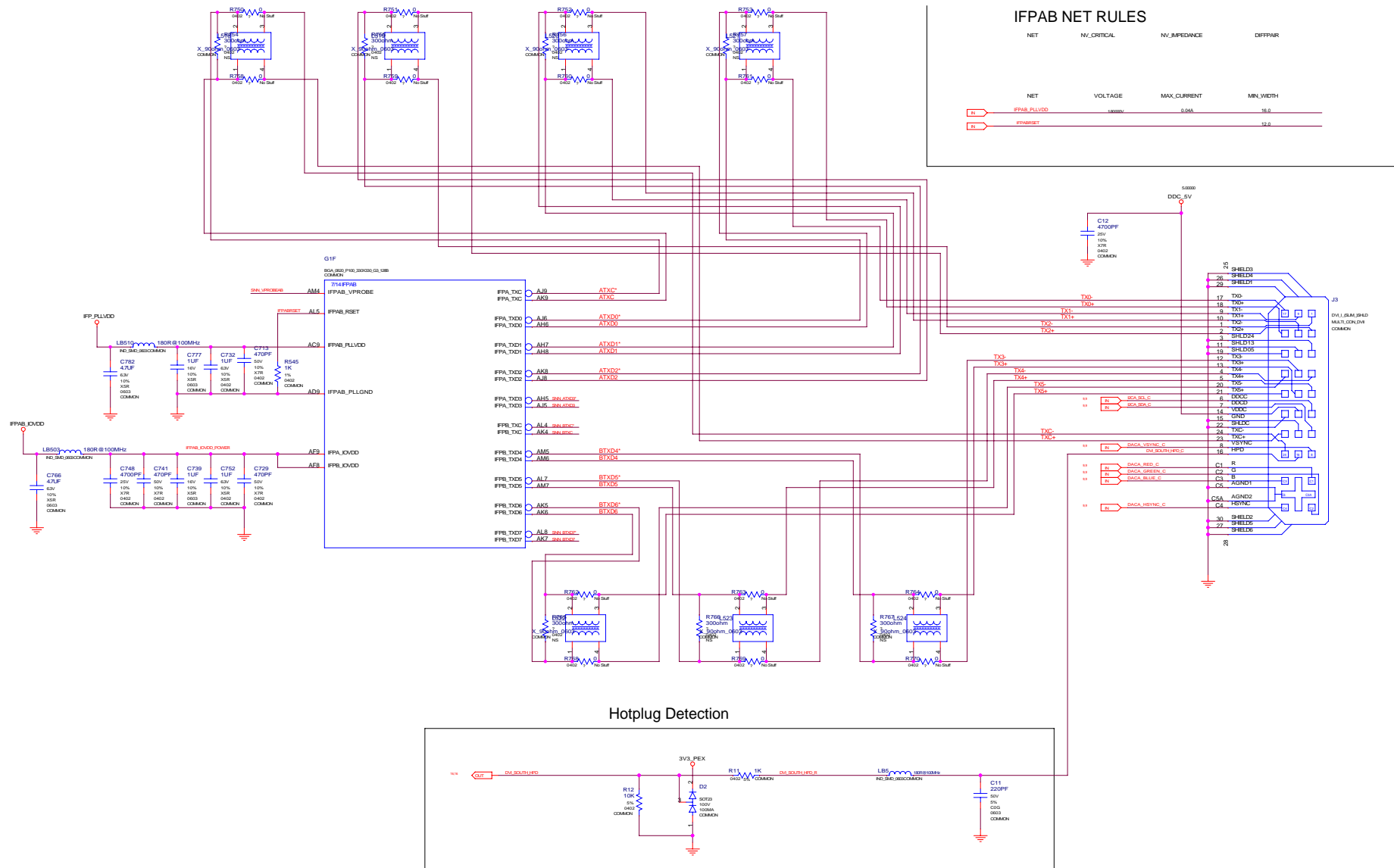
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE/DETAIL	PowerSupplyIII FBVDDQ, PEX1V2
REV	1
DATE	12/26/2006

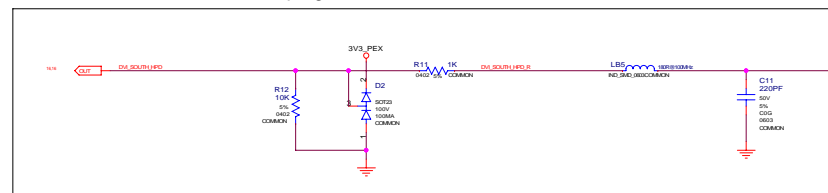
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## INTERNAL TMDS .. LINK A &amp; B



## Hotplug Detection



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PAGE DETAIL	TMD5 LINK A & PU1s, DVI CONNECTOR SOUTH

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