

P360-A00 Base Design

P360-A00, G92, 16Mx32 GDDR3 (900MHz),TV(OPTION)
DVI-I-DL, DVI-I-DL

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V186-1.0 Base on P360

- 1.PAGE11: ADD VGA display connector
- 2.PAGE12: Move IFP C/D HMDI to page 13
- 3.PAGE13: Unused DACB Interface, ADD IFP C/D HMDI interface
- 4.PAGE15: Use I2CC for HDMI control, add GPIO10/14 for HDMI control
- 5.PAGE18:Add FM1~FM6

V186-1.1 Base on V186-1.0

V186-1.1 Base on V186-1.0 remove the reference place of the 6.1 mil RGB signal.

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10360-base-000	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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NV_PN

600-10360-base-000 A

ID

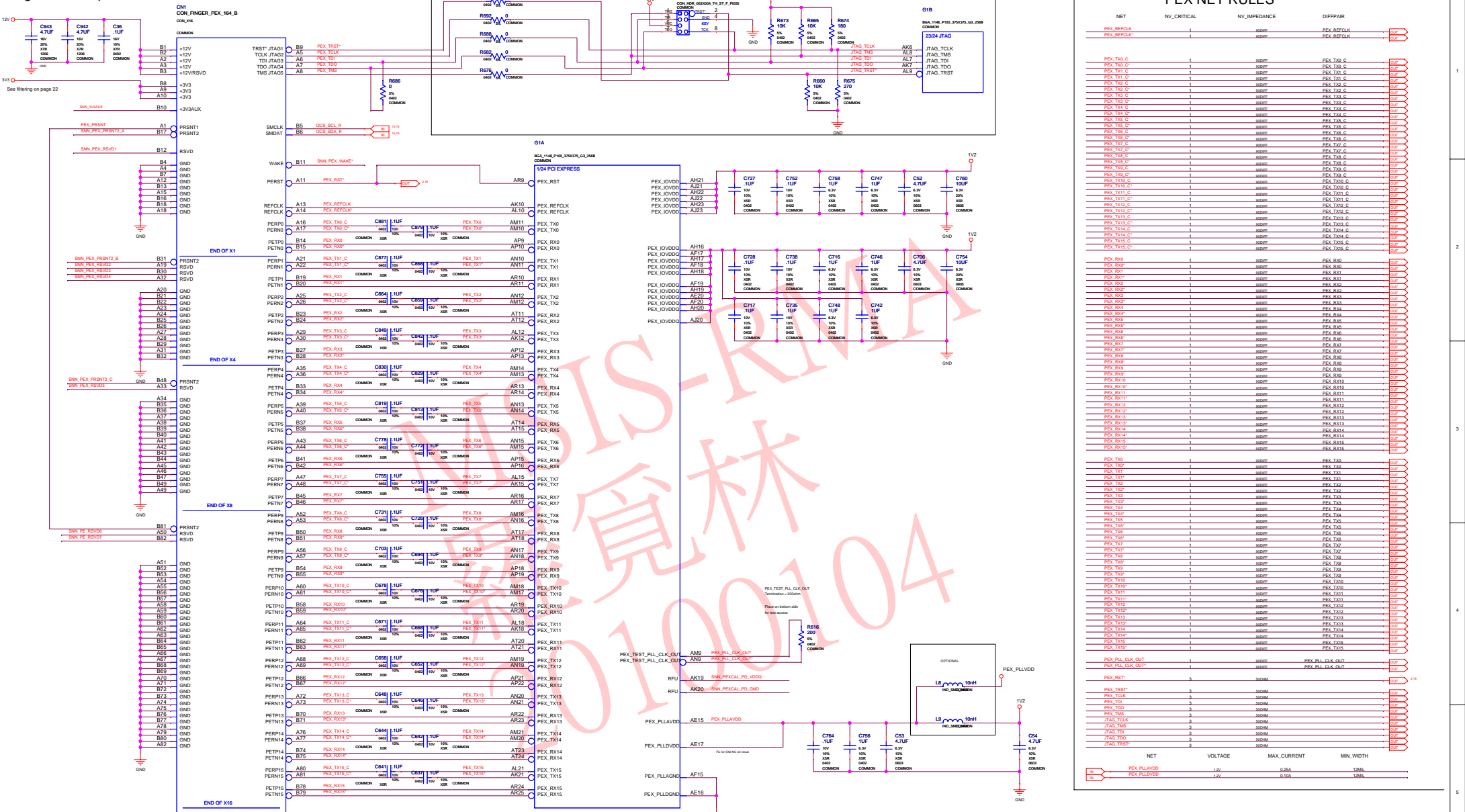
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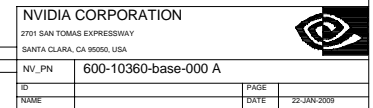




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ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express 1.0

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750 mils of the pad

ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: GPU Partition C/D

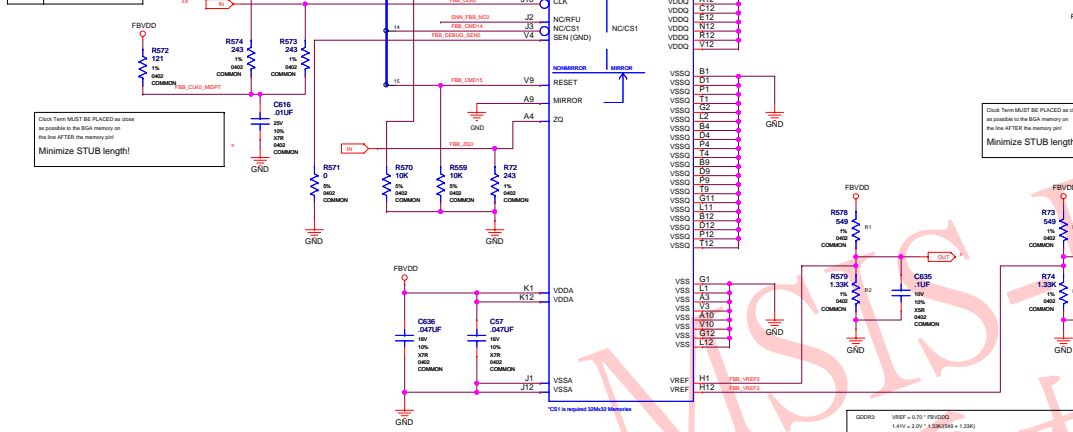
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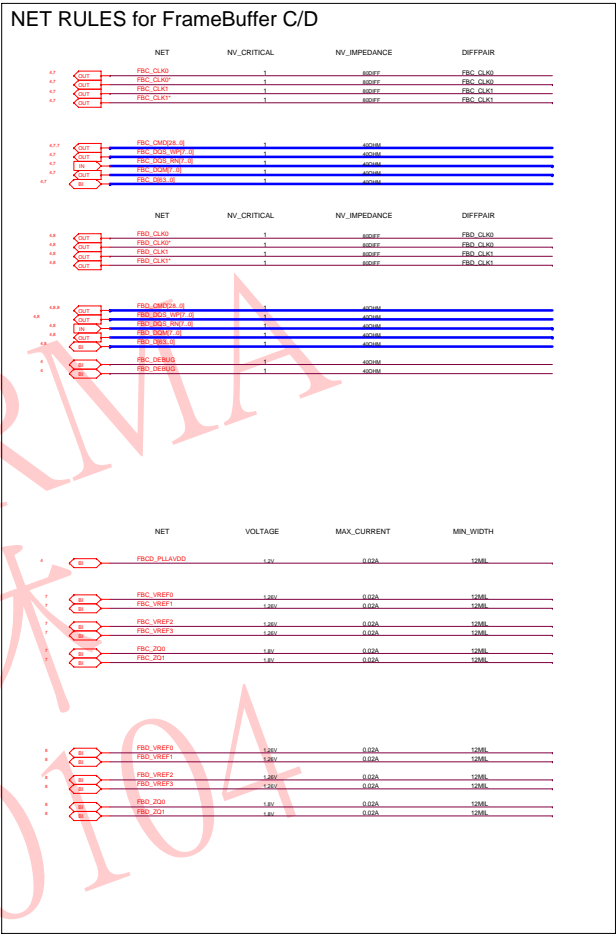
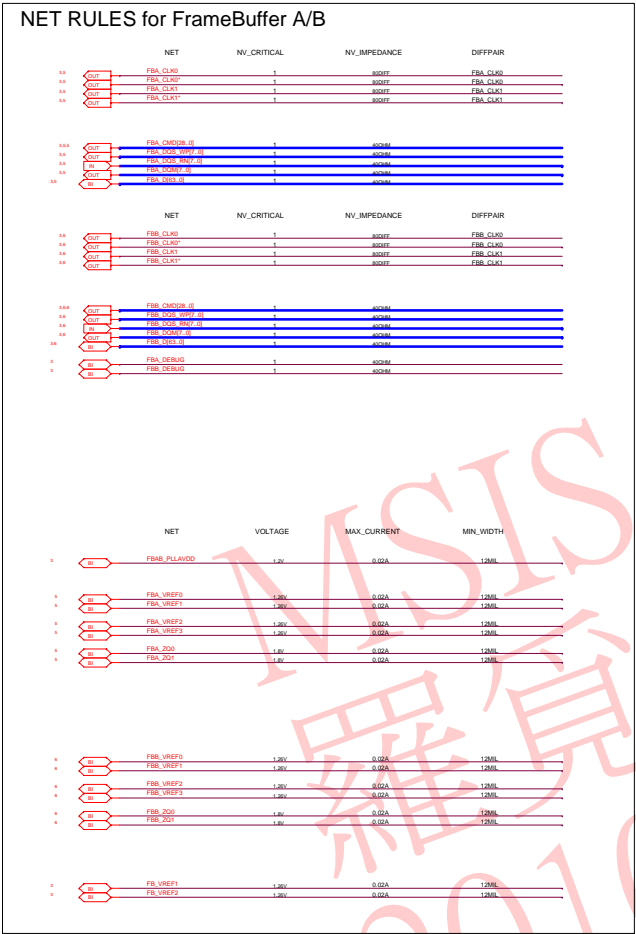
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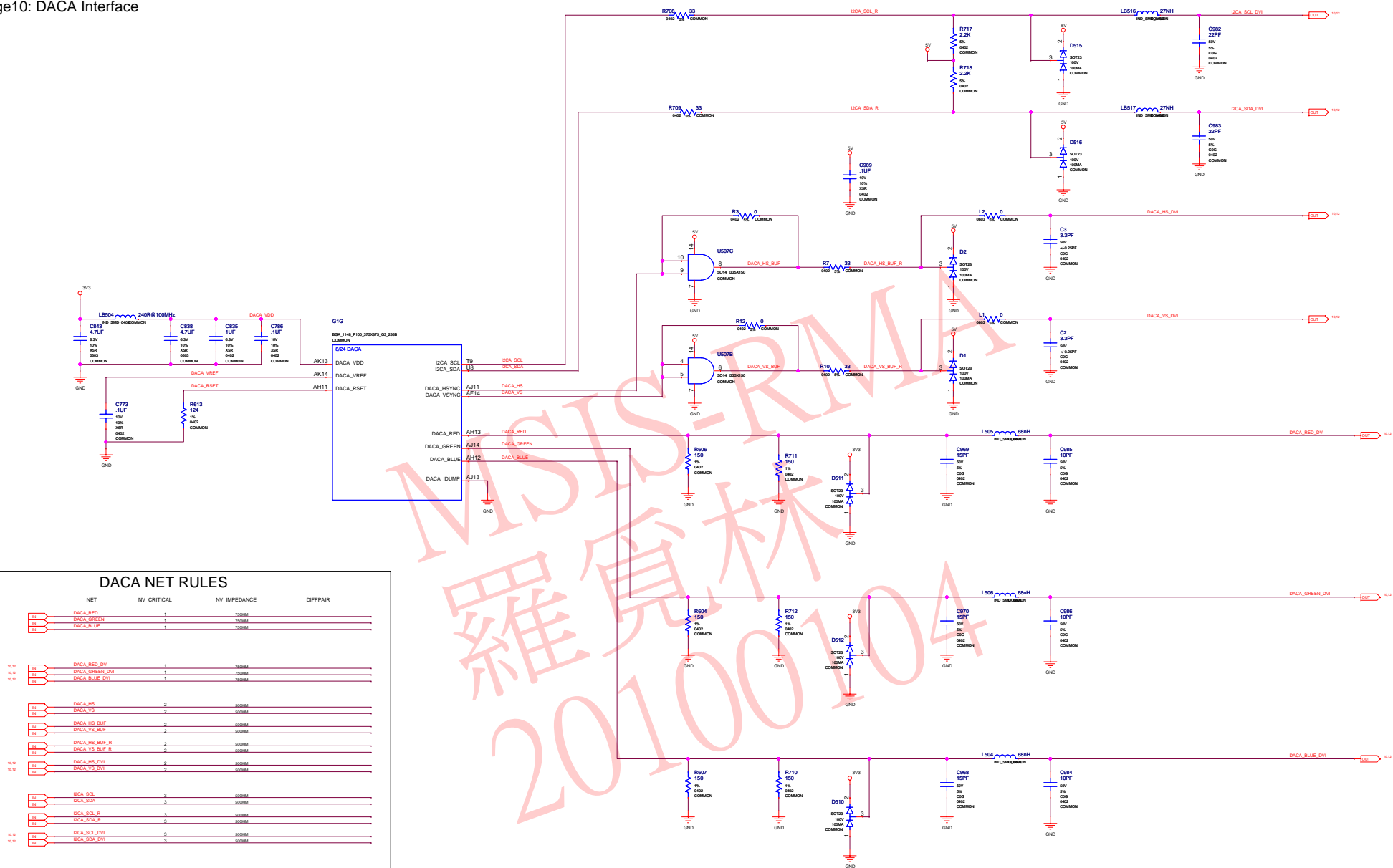


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A588</	



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ASSEMBLY P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL FrameBuffer Net Rules




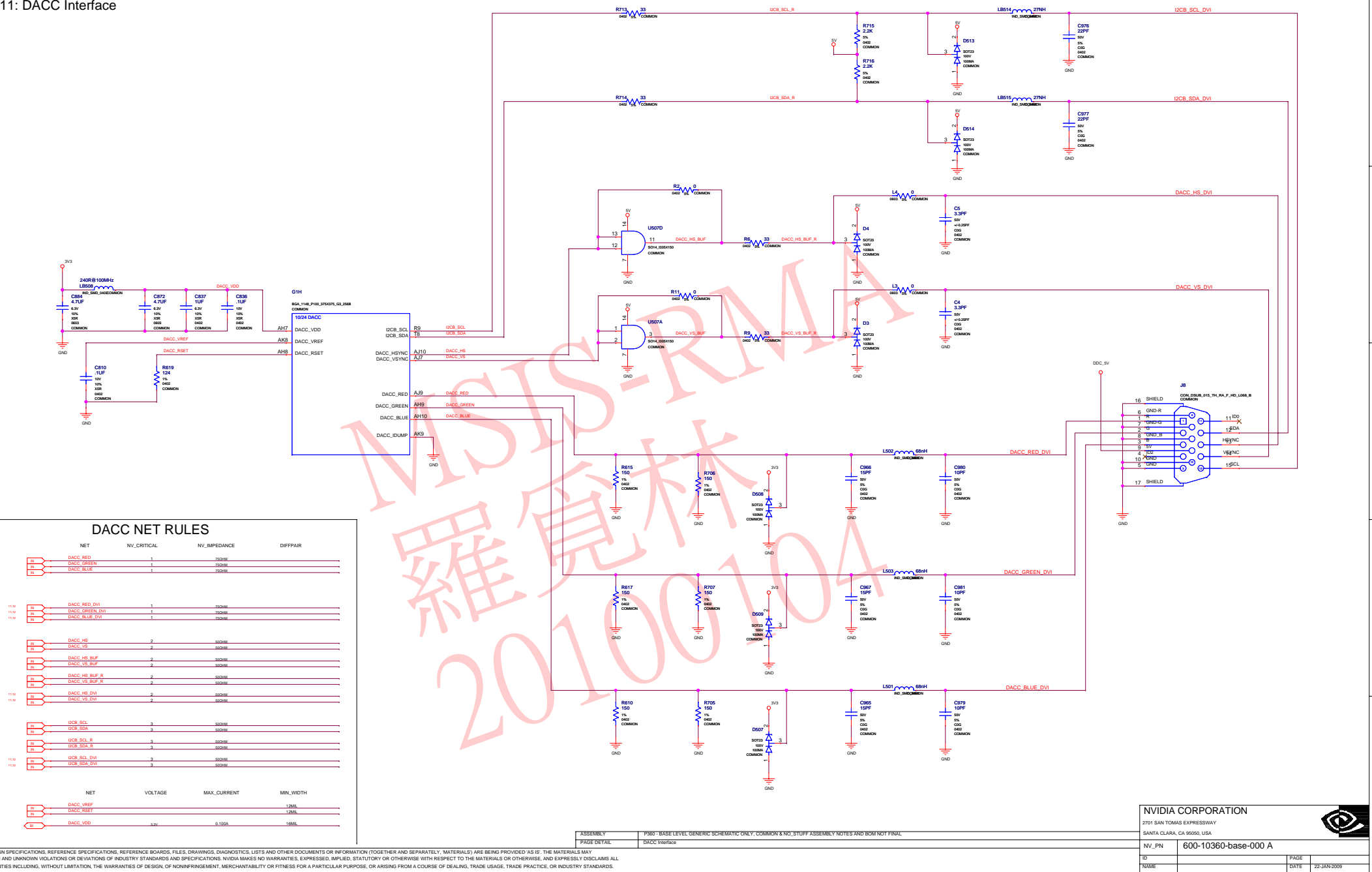
DACA NET RULES

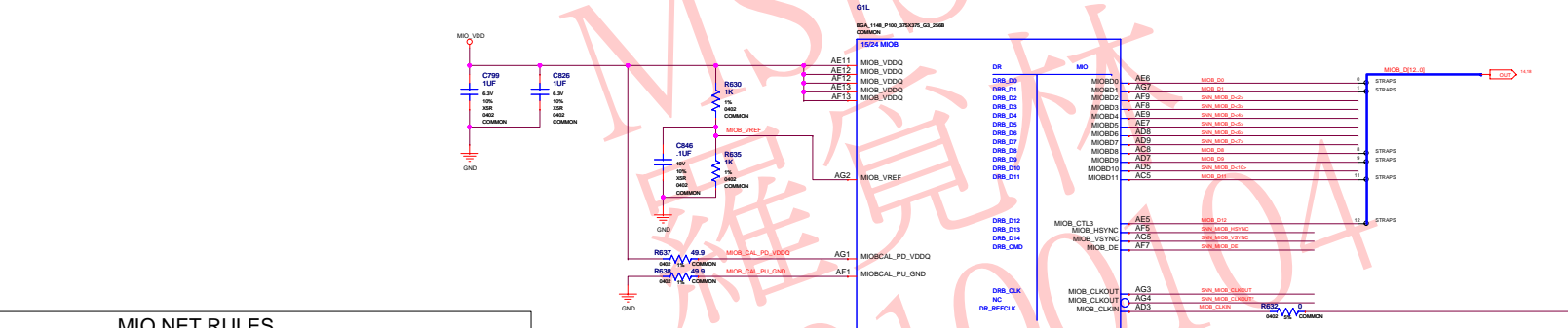
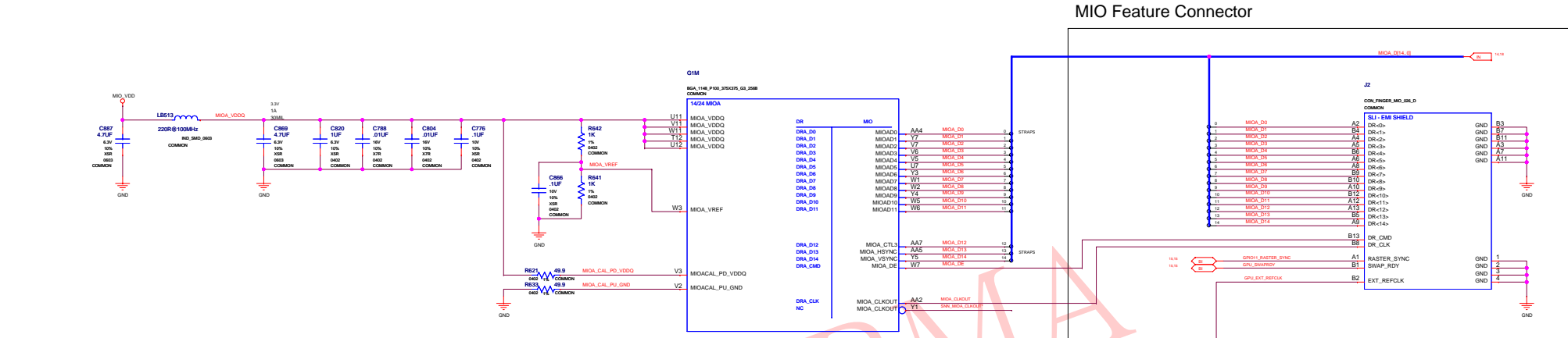
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	DACA_RED	1	750MR	
	DACA_GREEN	1	750MR	
	DACA_BLUE	1	750MR	
10:10	DACA_RED_DVI	1	750MR	
10:10	DACA_GREEN_DVI	1	750MR	
10:10	DACA_BLUE_DVI	1	750MR	
	DACA_HS	2	500MR	
	DACA_VS	2	500MR	
	DACA_HS_BUF	2	500MR	
	DACA_VS_BUF	2	500MR	
	DACA_HS_BUF_R	2	500MR	
	DACA_VS_BUF_R	2	500MR	
10:10	DACA_HS_DVI	2	500MR	
10:10	DACA_VS_DVI	2	500MR	
	DCA_S0L	3	500MR	
	DCA_S0A	3	500MR	
	DCA_S0L_R	3	500MR	
	DCA_S0A_R	3	500MR	
10:10	DCA_S0L_DVI	3	500MR	
10:10	DCA_S0A_DVI	3	500MR	
	NET			
	DACA_VREF			12MR
	DACA_WSET			12MR
	DACA_VDD	3.3V	0.100A	10MR

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ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA Interface

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MIO NET RULES			
NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
MIOA_D14_0	1	100ohm	
MIOB_CLKOUT	1	100ohm	
MIOA_DE	1	100ohm	
MIOB_D12_0	1	100ohm	
MIOB_CLKIN	1	100ohm	
GPU_EXT_REFCLK	1	100ohm	
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	1.85V		12mil
MIOB_VREF	1.85V		12mil
MIOA_PU_GND	1.85V		12mil
MIOB_PU_GND	1.85V		12mil

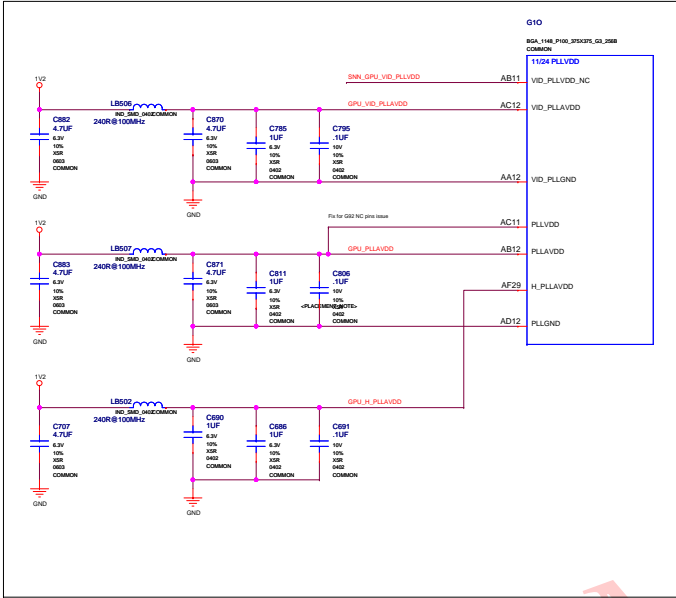
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ASSEMBLY P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NC STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL Multi-use IO(MIO) Interface

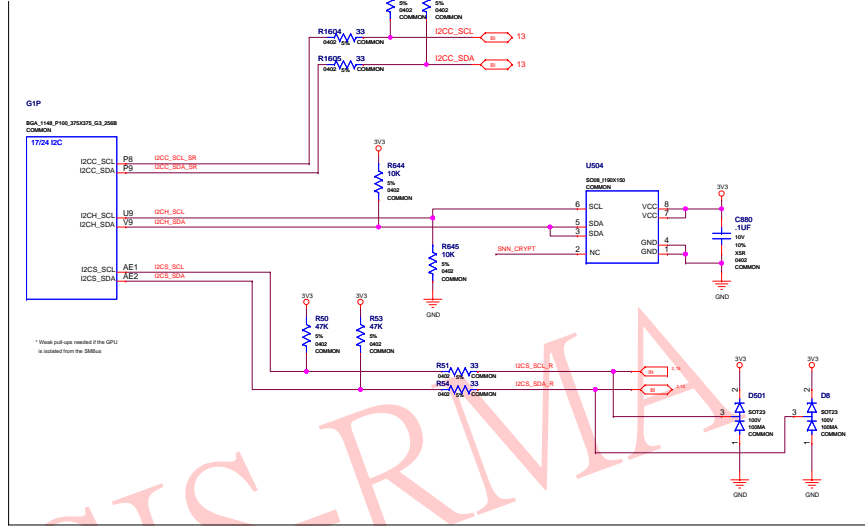
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PLLVD/VID_PLLVD



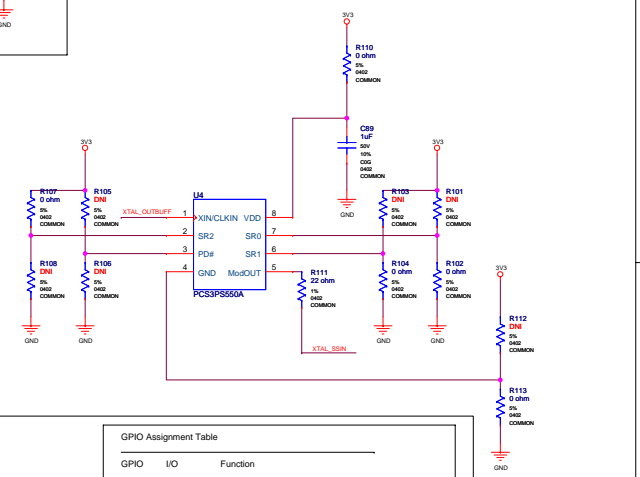
I2CC / I2CH(+ HDCP ROM) / I2CS



MISC NET RULES

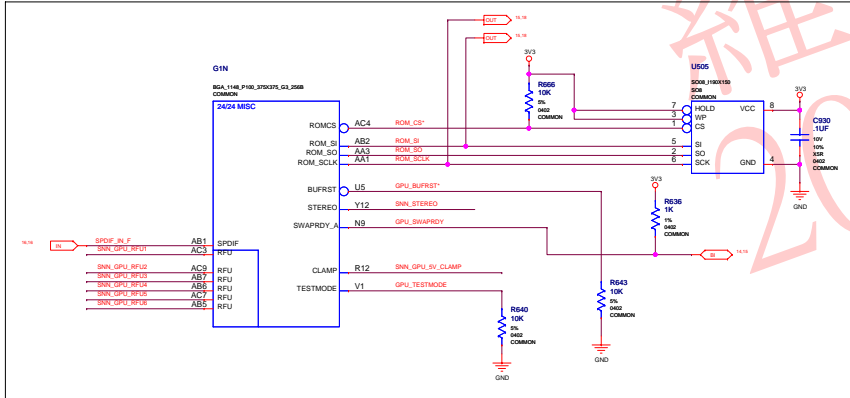
NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
GDH_SCL	3	100R	
GDH_SDA	3	100R	
GDH_SDA_B	3	100R	
GDH_SDA_R	3	100R	
ROM_CS*	3	100R	
ROM_B	3	100R	
ROM_CS	3	100R	
ROM_SCLX	3	100R	
GPU_SWAPRDY	3	100R	
GPU_TESTMODE	3	100R	
GPU0V_DV1_A_HPD	3	100R	
GPU0V_DV1_C_HPD	3	100R	
GPU0V_FAN_PWM	3	100R	
GPU0V_VBEL	3	100R	
GPU0V_VBEL	3	100R	
GPU0V_FAN_TACH	3	100R	
GPU0V_THERM_OVERT*	3	100R	
GPU01_RASTER_SYNC	3	100R	
XTAL_SSN	1	100R	
XTAL_IN	1	100R	
XTAL_OUT	1	100R	
XTAL_OUTBUFF	1	100R	
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
GPU_VID_PLLVD	1.2V	0.05A	12MIL
GPU_VID_PLLVD	1.2V	0.05A	12MIL
GPU_H_PLLVD	1.2V	0.05A	12MIL
GPU_H_PLLVD	1.2V	0.05A	12MIL
GPU_H_PLLVD	1.2V	0.05A	12MIL

XTAL

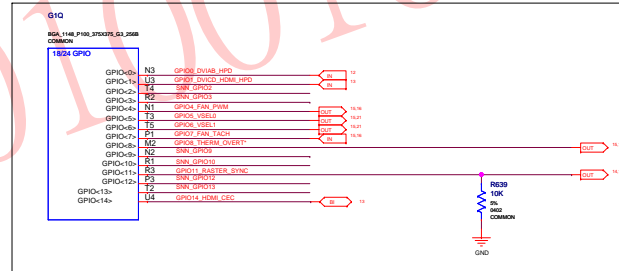


ROM / MISC

(BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)



GPIO



GPIO	I/O	Function
0	IN	DV1 Hotplug Detect South
1	IN	DV1 Hotplug Detect North
2	N/A	Framework Interrupt
3	N/A	Not used
4	OUT	Fan PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fan Tach Input
8	OUT	THERM_OVERT*
9	N/A	Not used
10	N/A	Not used
11	OUT	RASTER (SLI) SYNC
12	N/A	Not used
13	N/A	Not used
14	IN	GPIO14_IDM1_CEC

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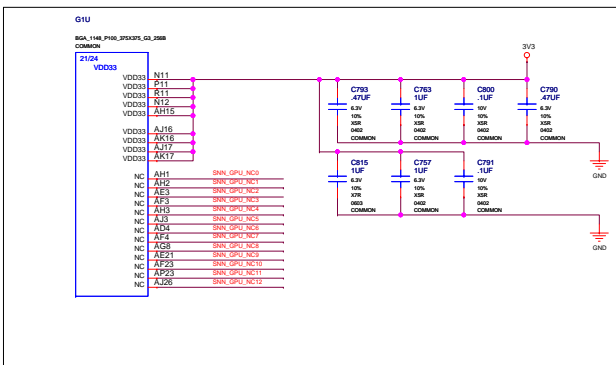
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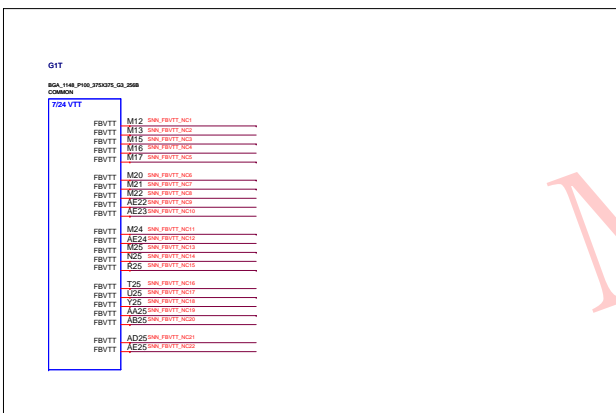
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ASSEMBLY P365 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL MISC: GPIO, I2C, BIOS, PLL, and XTAL

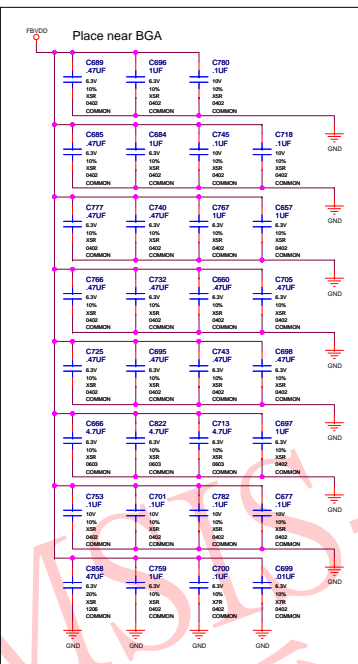
VDD33



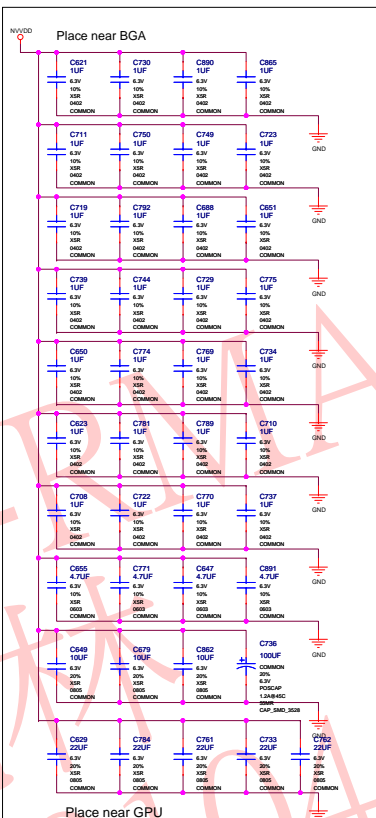
FBVTT



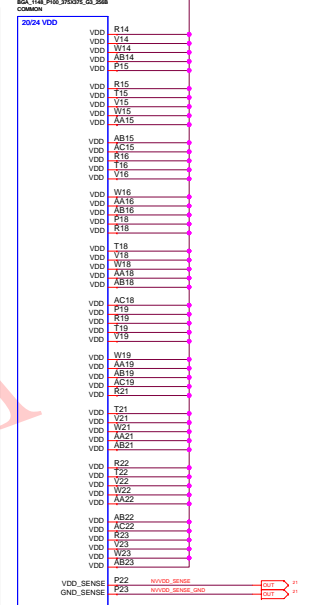
FBVDDQ



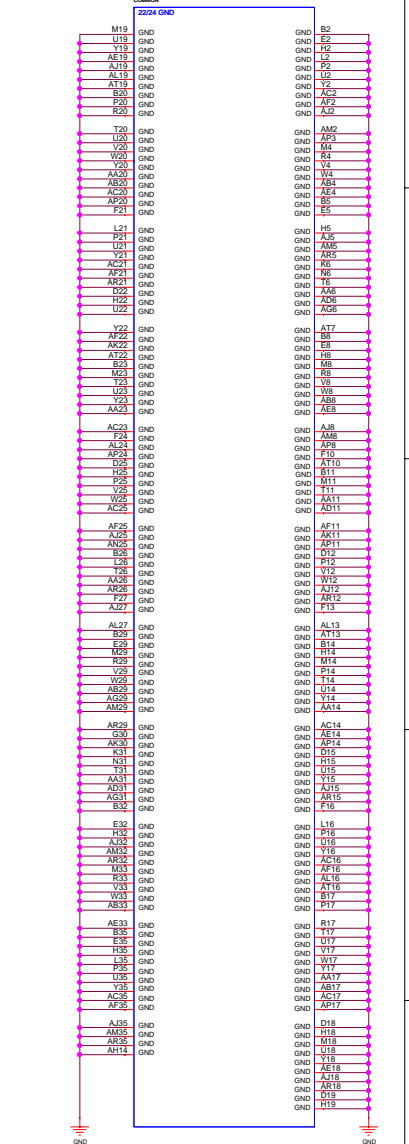
NVVDD



G1V



G1X



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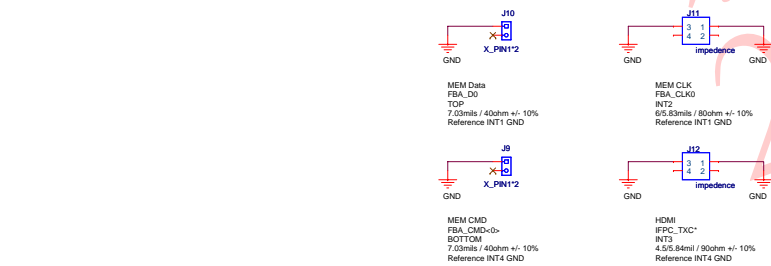
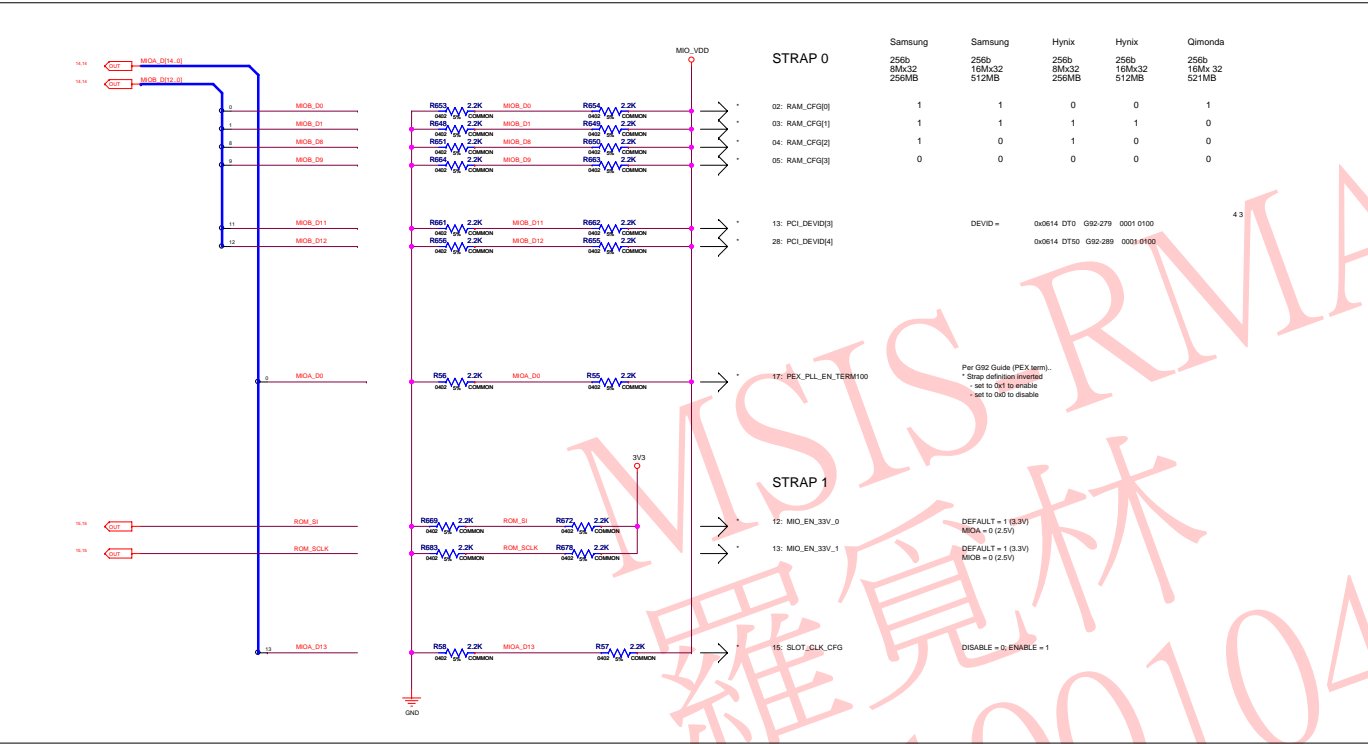
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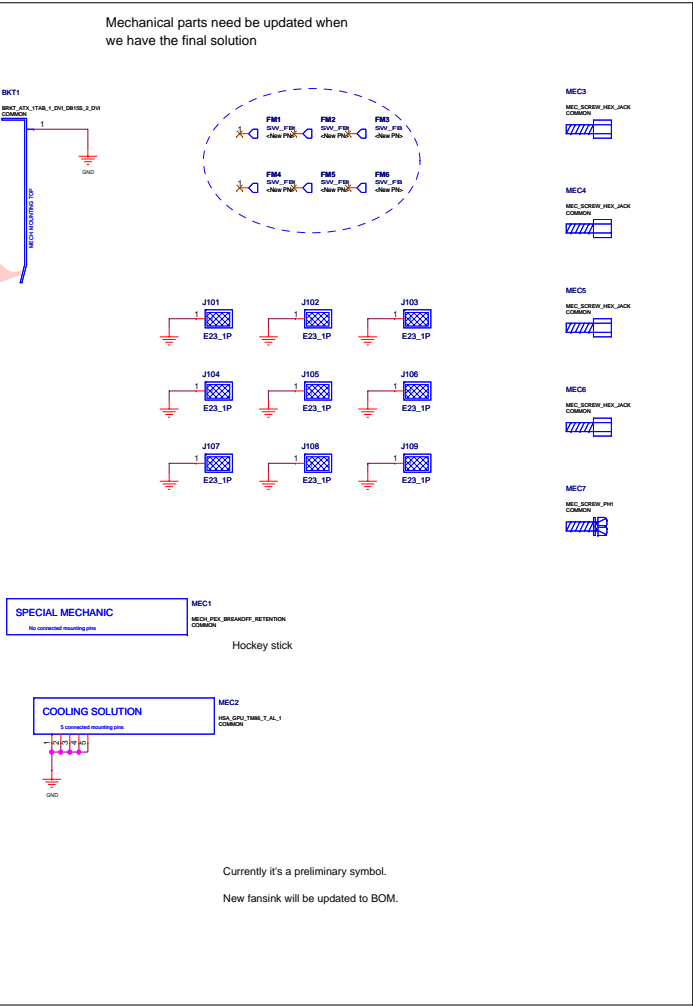
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ASSEMBLY P360 - BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
PAGE DETAIL Power/GND and Decoupling

STRAPS

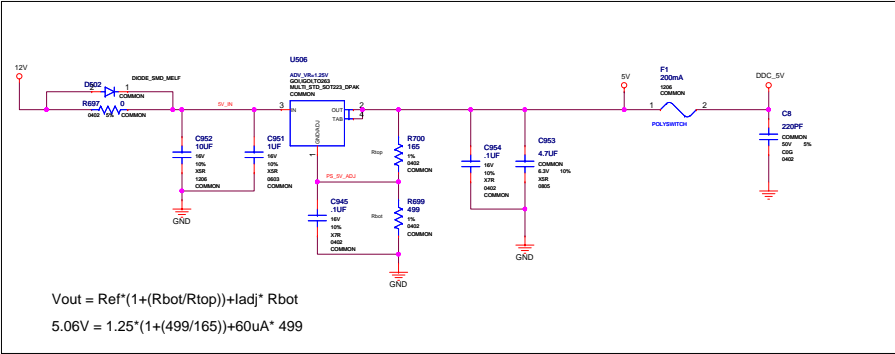


MECHANICAL



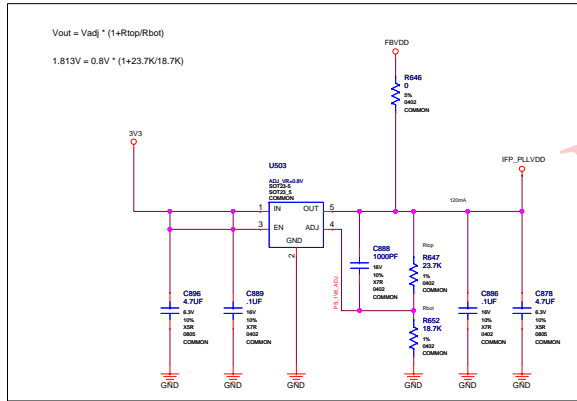
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5V REGULATOR

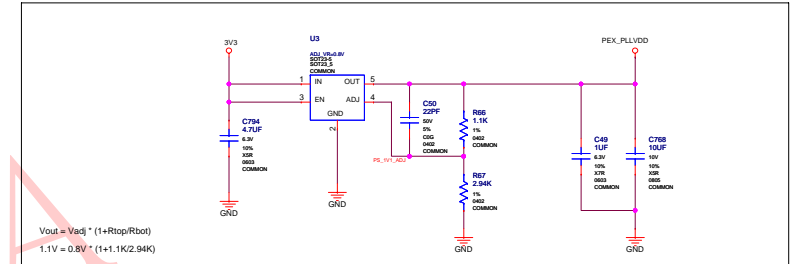


IFP PLL Supply 1.8V

(Stuff option)

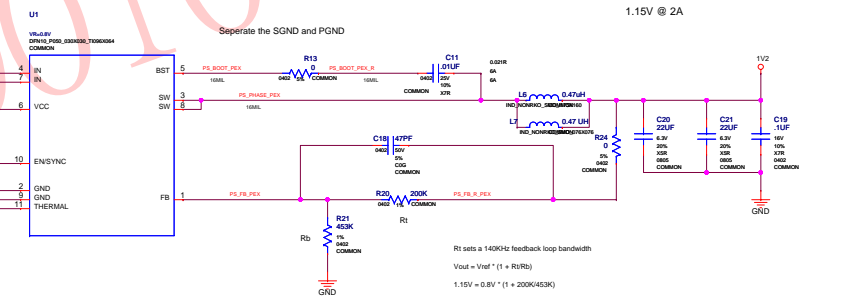
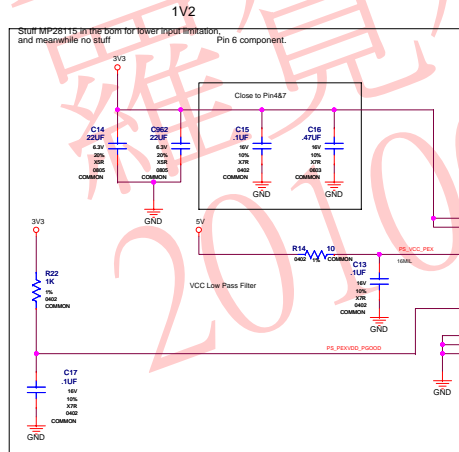
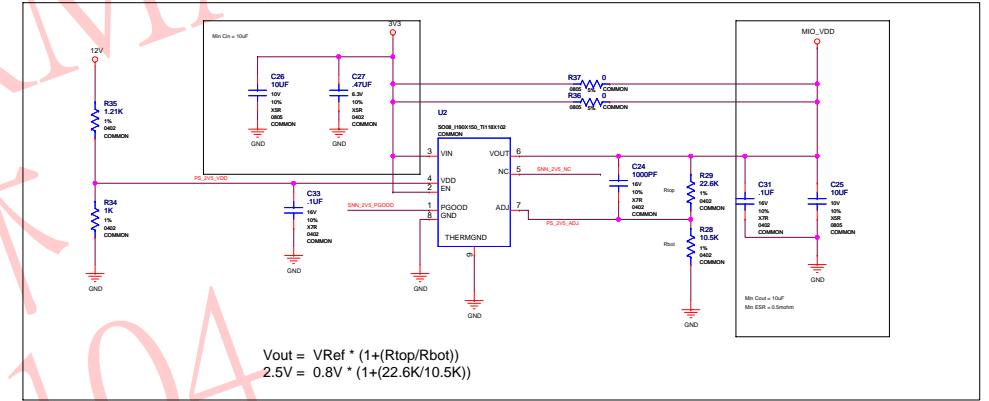


PEX_PLLVDD Optional (Stuff option)



MIO_VDD

(Stuff option)



NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	0.8A	120M	5V
5V	0.8A	120M	5V
PEX_PLLVDD	0.1A	120M	1.1V
IFP_PLLVDD	0.1A	120M	1.8V
MIO_VDD	0.8A	120M	2.5V

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
FBVDD	11A	35MIL	1.8V
1V2	2A	16MIL	1.15V

PEXVDD Power Supply

PEXVDD = 1.15V @ 2A

$V_{out} = V_{ref} * (1 + (R_{top}/R_{bot}))$
 $1.152V = 0.8V * (1 + (1.07K/2.43K))$

FBVDD Power Supply

FBVDD = 1.8V@ 11A

$I_{ripple} = 3.19A$
 $V_{ripple} = 22mV$

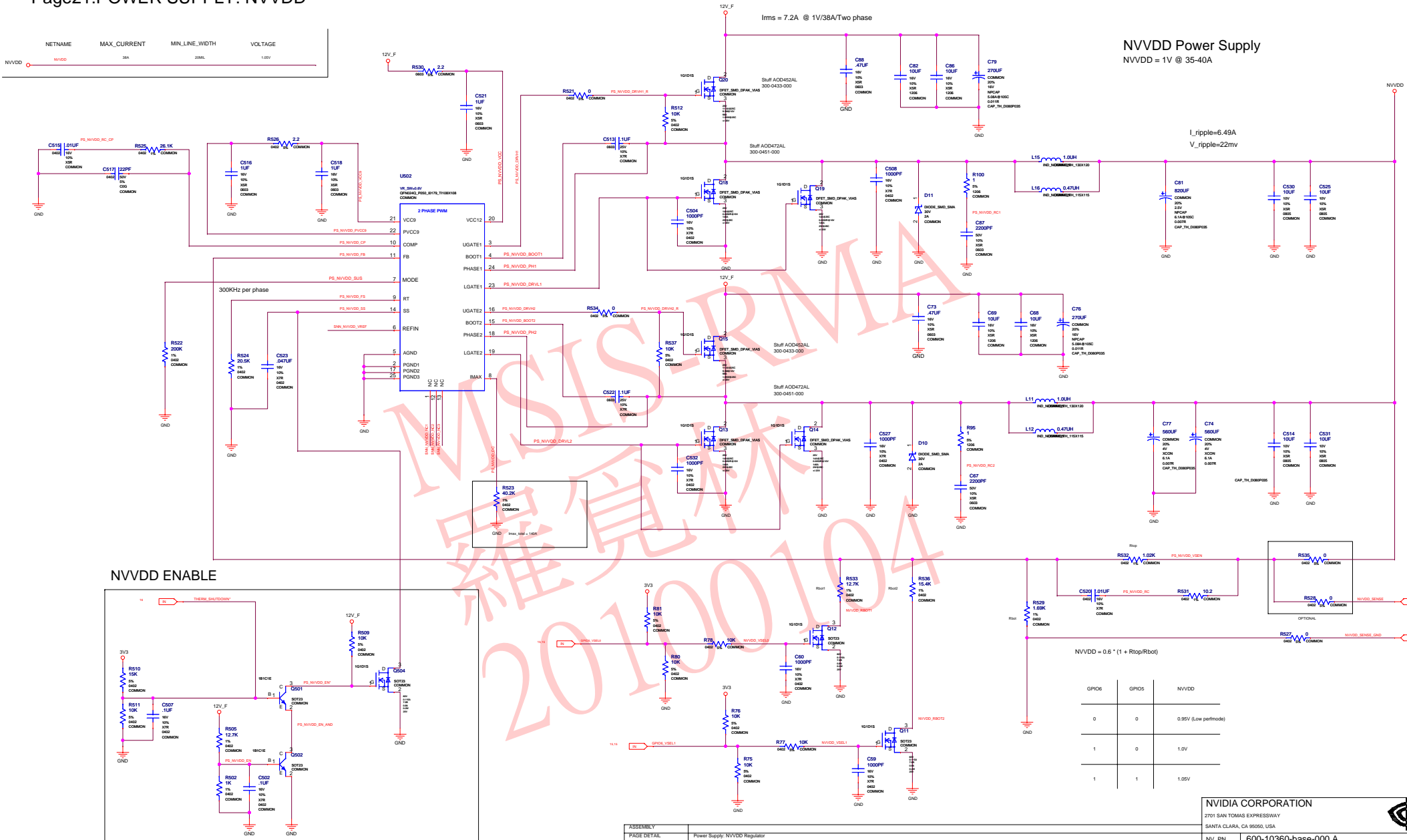
$FBVDDQ = V_{REF} * (1 + (R_{top}/R_{bot1}))$
 $2.06V = 0.8V * (1 + (1.58K/1K))$
 $1.819V = 0.8V * (1 + (1.58K/1.24K))$

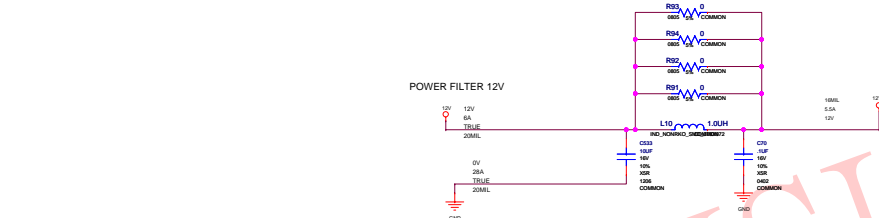
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Page21:POWER SUPPLY: NVVDD


NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
NVVDD	35A	20MIL	1.05V





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