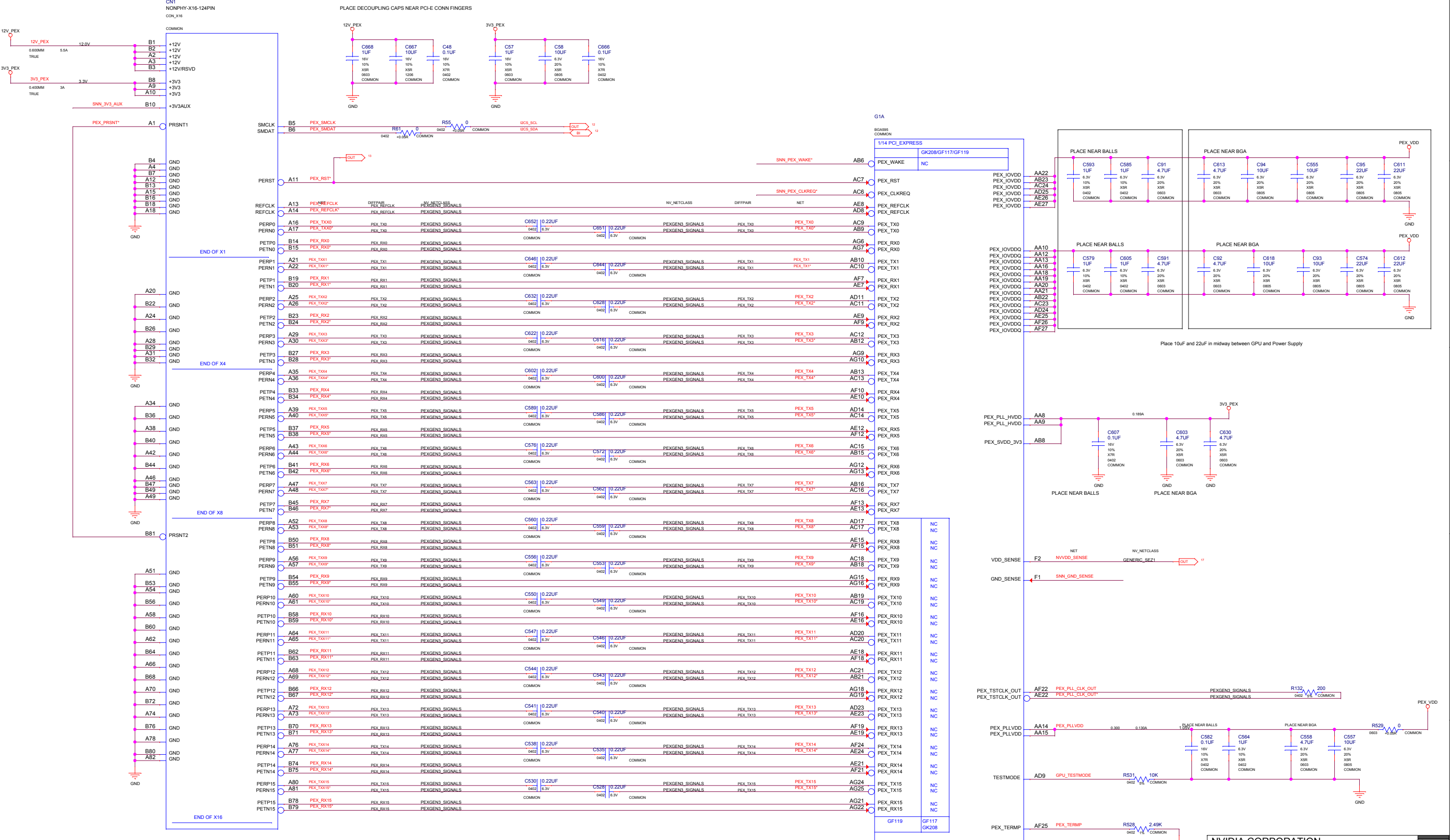
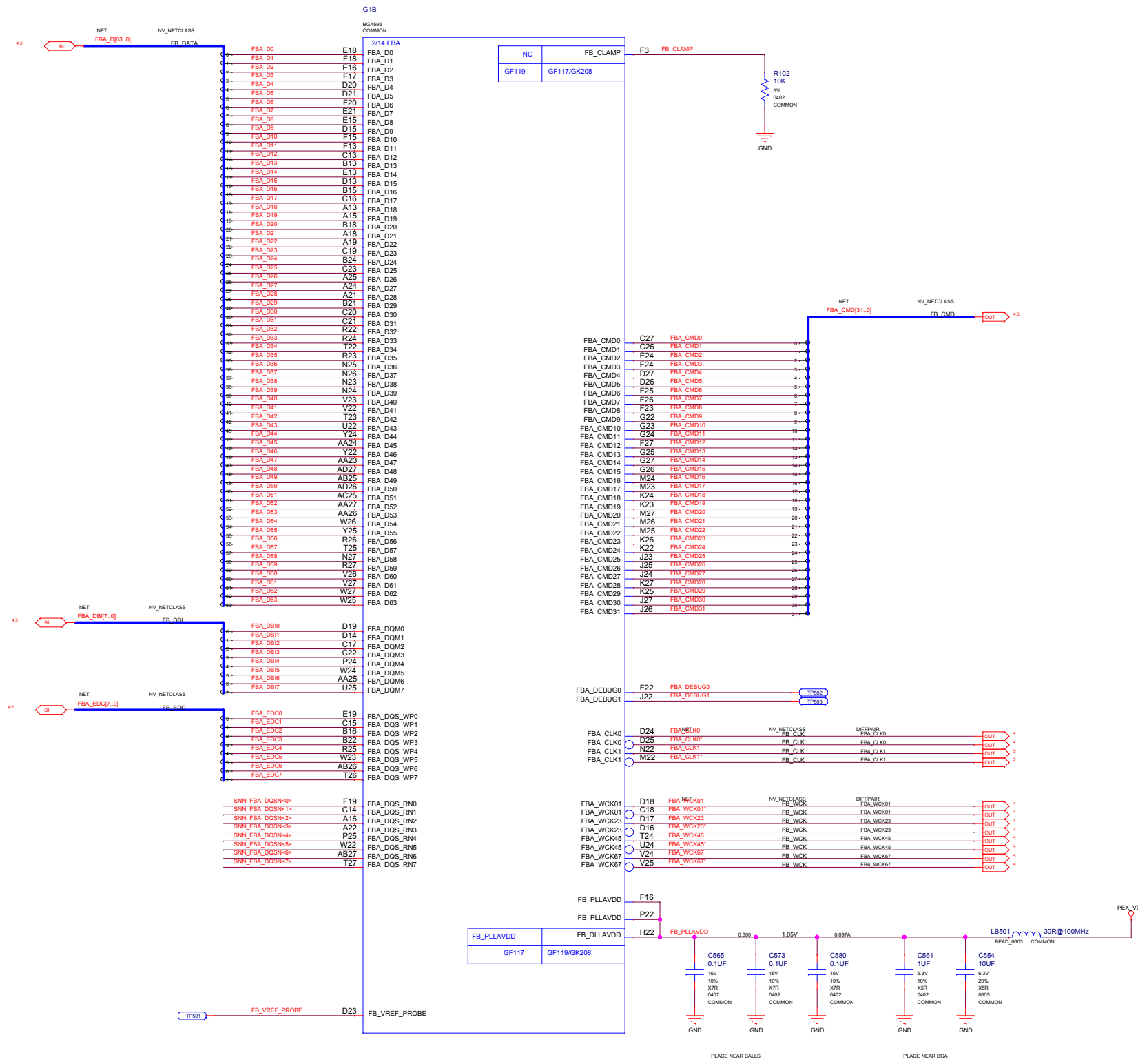


GK208 GDDR5 X16 64BIT
DVI-I/DVI-D/SlimVGA + HDMI/DP + VGA

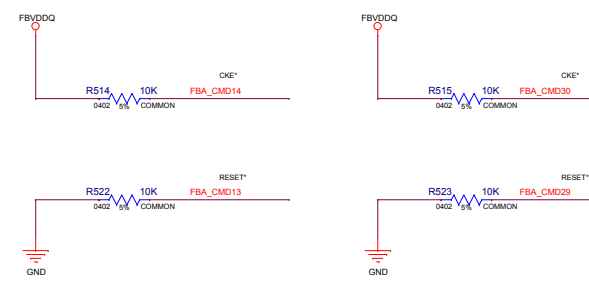
Page	Description
1	Table of Contents
2	PCI EXPRESS
3	GPU MEMORY FBA
4	FB Partition A bits 31..0
5	FB Partition A bits 63..32
6	DECOUPLING for DRAMs
7	POWER/DECOUPLING: NVVDD, FBVDDQ, VDD33, GND
8	IFPA/B TMDs DUAL LINK
9	IFPC HDMI/DP, DP_PWR
10	UNUSED IFPD, IFPE & IFPF
11	DACA VGA
12	BIOS, JTAG, GPIO & XTAL
13	PCI-E Reset, STRAPS & FAN
14	PS: 5V, PEXVDD
15	PEX_VDD: Open VR Type0
16	PS: FBVDDQ
17	PS: NVVDD

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CMD	31.0	63.32
CMD0	C3'	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE'	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB'	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS'	
CMD13	RST'	
CMD14	CKE'	
CMD15	CAS'	
CMD16		C3'
CMD17	A3_BA3	
CMD18	A2_BA0	
CMD19	A4_BA2	
CMD20	A5_BA1	
CMD21	WE'	
CMD22	A7_A8	
CMD23	A6_A11	
CMD24	AB'	
CMD25	A12_RFU	
CMD26	A0_A10	
CMD27	A1_A9	
CMD28	RAS'	
CMD29	RST'	
CMD30	CKE'	
CMD31	CAS'	

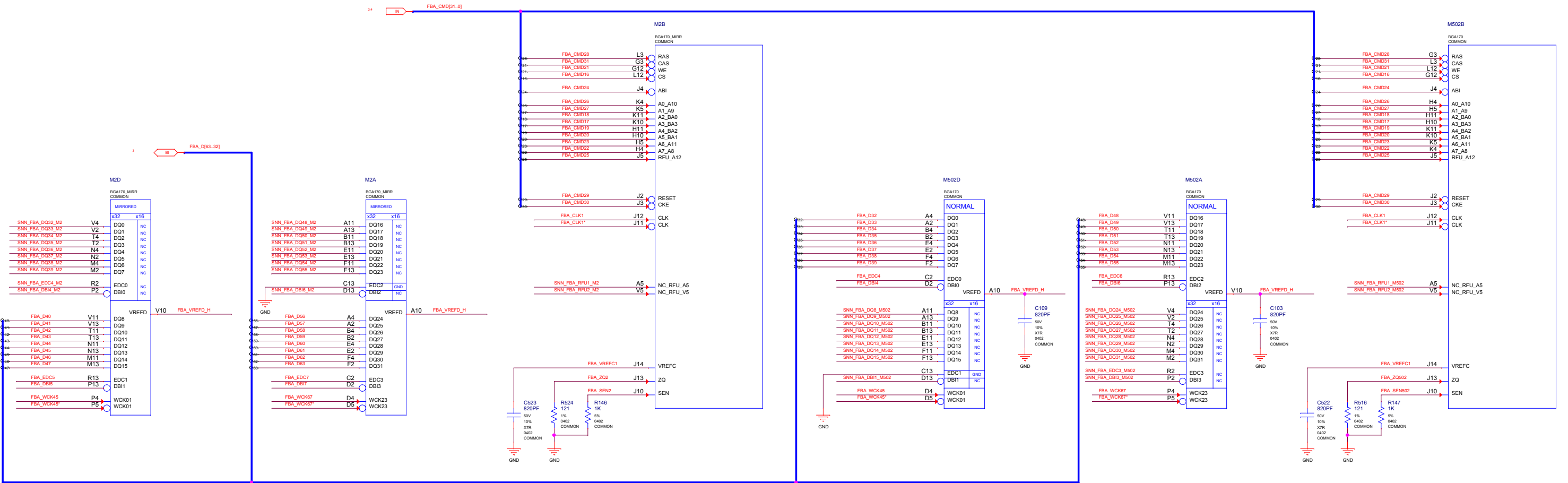


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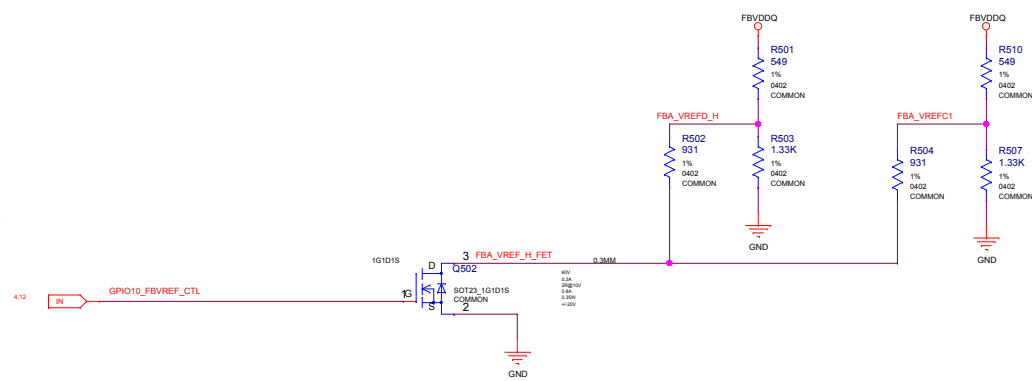
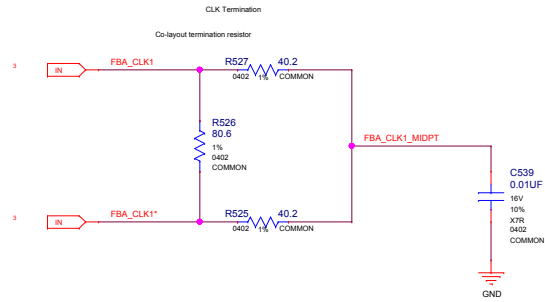
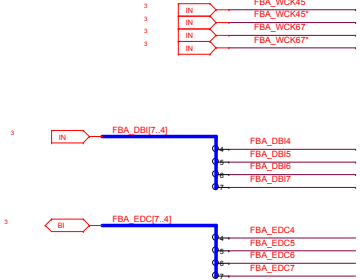
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU MEMORY FBA



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CMD	31..0	63..32
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17	A3_BA3	
CMD18	A2_BA0	
CMD19	A4_BA2	
CMD20	A5_BA1	
CMD21	WE*	
CMD22	A7_A8	
CMD23	A6_A11	
CMD24	AB*	
CMD25	A12_RFU	
CMD26	A0_A10	
CMD27	A1_A9	
CMD28	RAS*	
CMD29	RST*	
CMD30	CKE*	
CMD31	CAS*	



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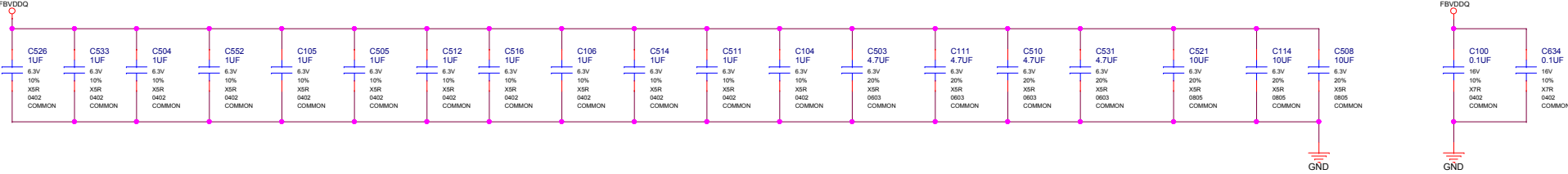
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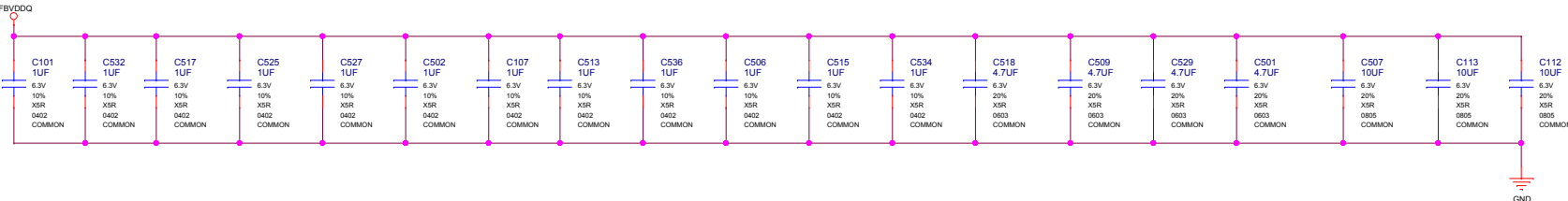
ASSEMBLY	
PAGE DETAIL	FB Partition A bits 63..32



DECOUPLING FOR M1 and M501 DEVICE



DECOUPLING FOR M2 and M502 DEVICE

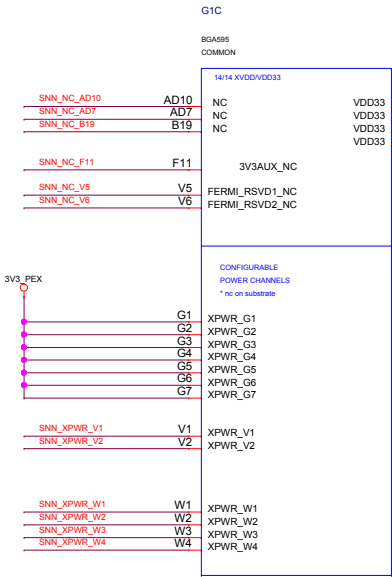
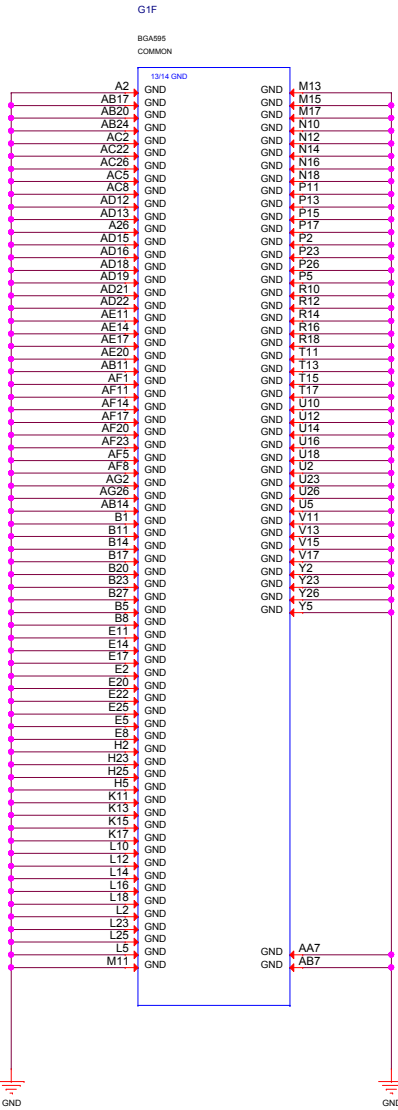
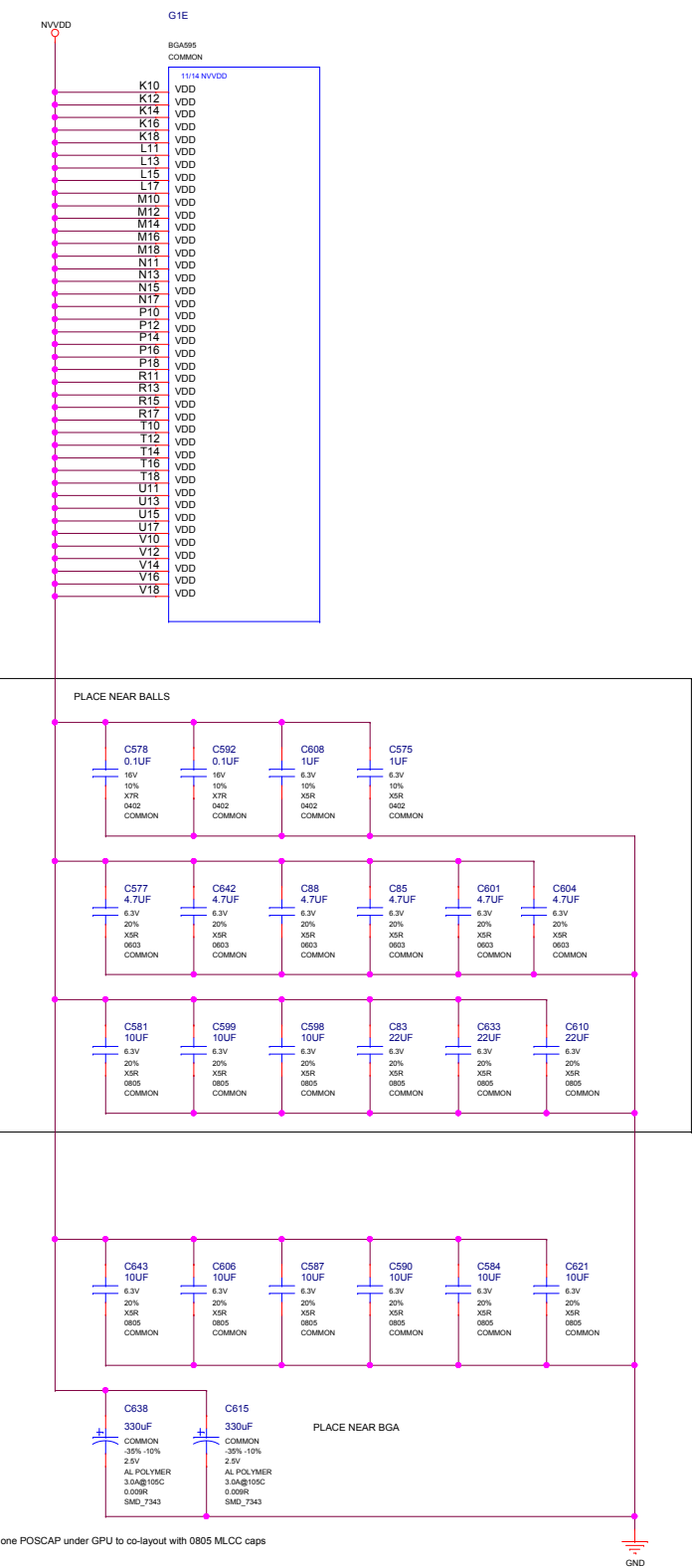
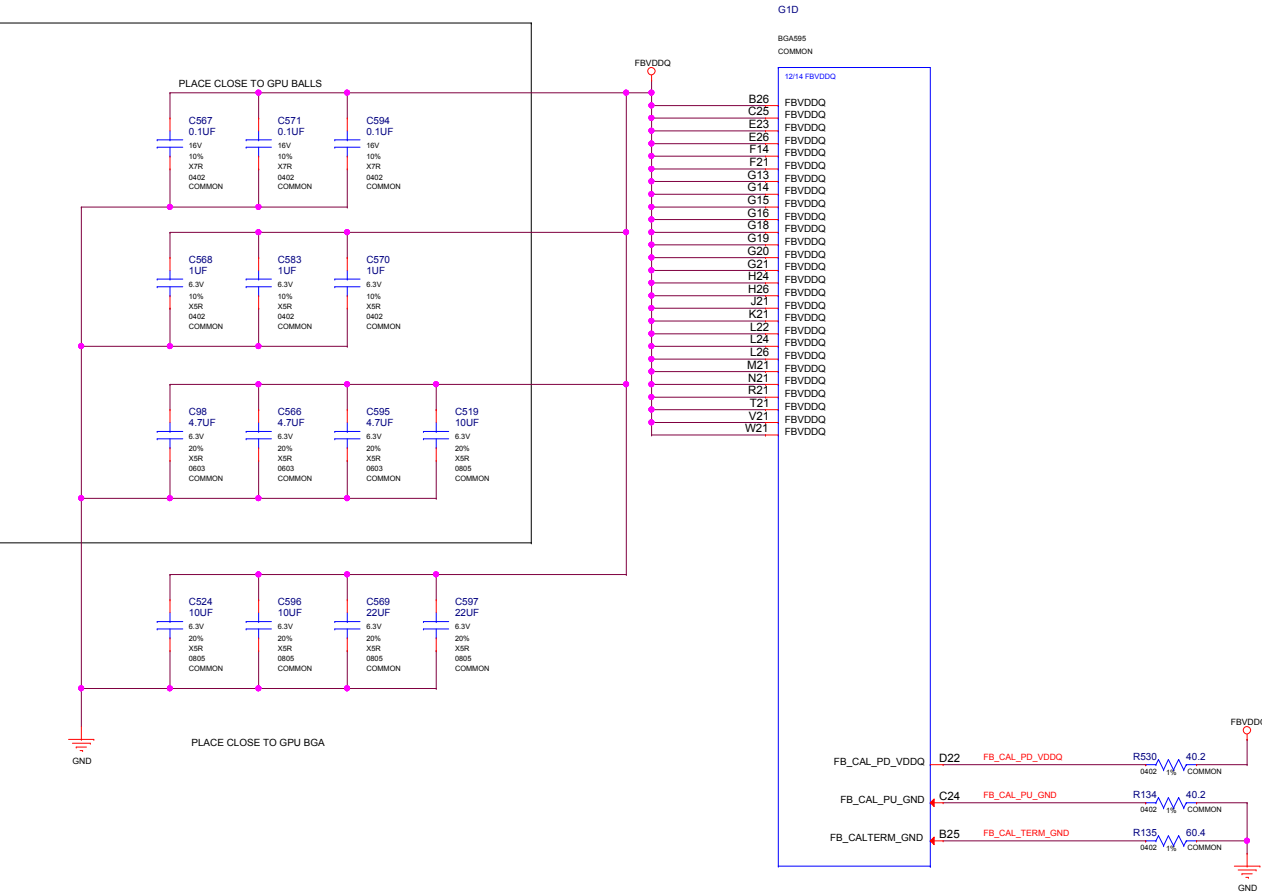


PLACE 1uF CAPS CLOSEST TO THE MEMORY DEVICES

PLACE LARGER CAPACITORS SLIGHTLY FARTHER AWAY

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** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.
Connection will be modified according to Layout.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	POWER/DECOUPLING: NVVDD, FBVDDQ, VDD33, GND

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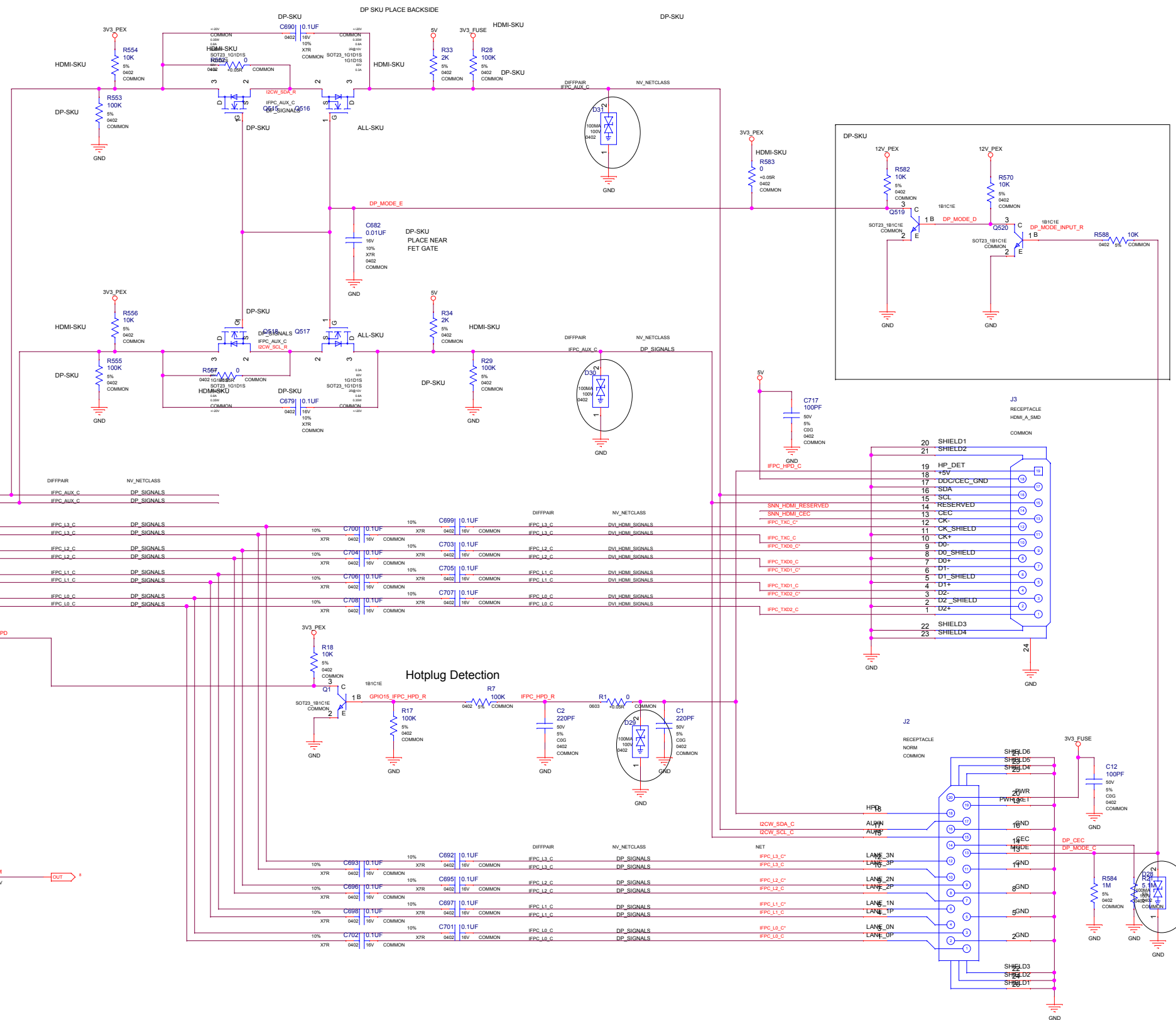
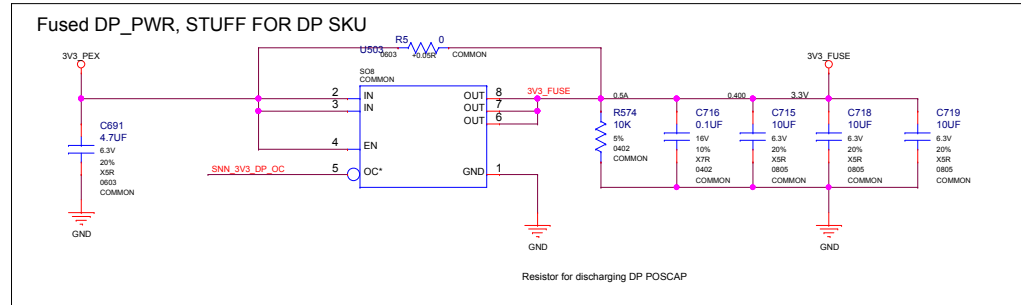
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPC HDMI/DP, DP_PWR

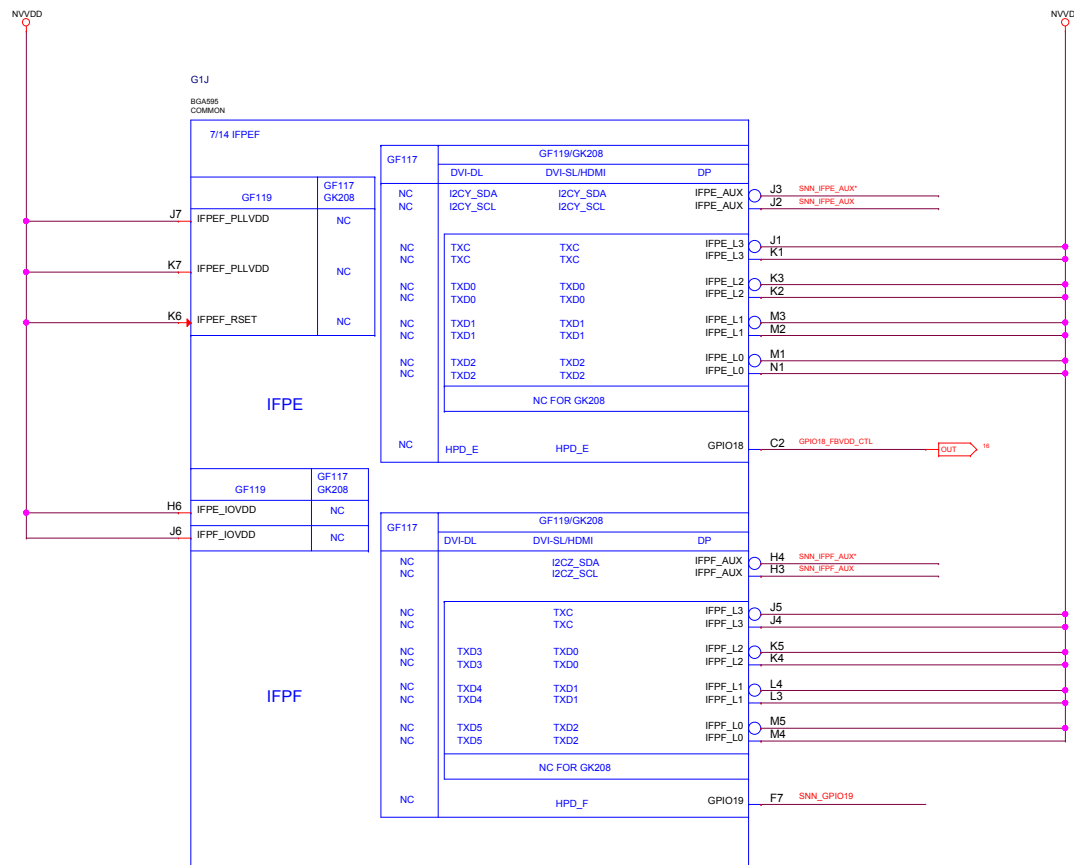
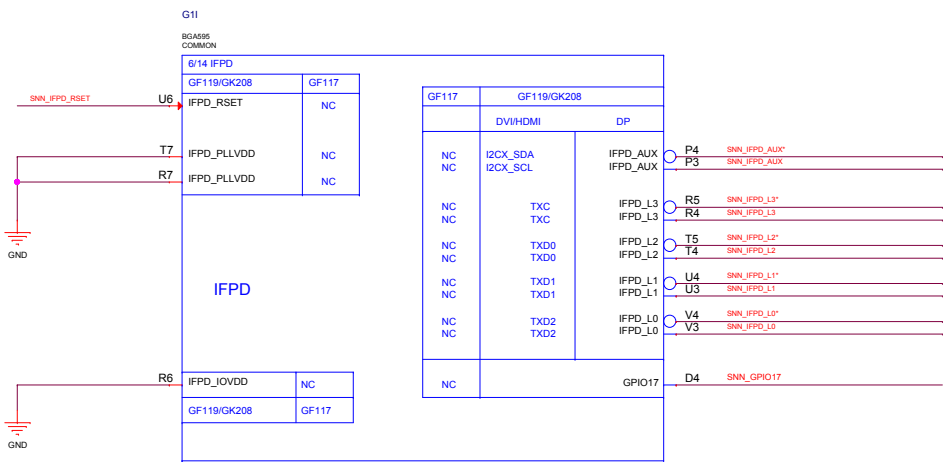
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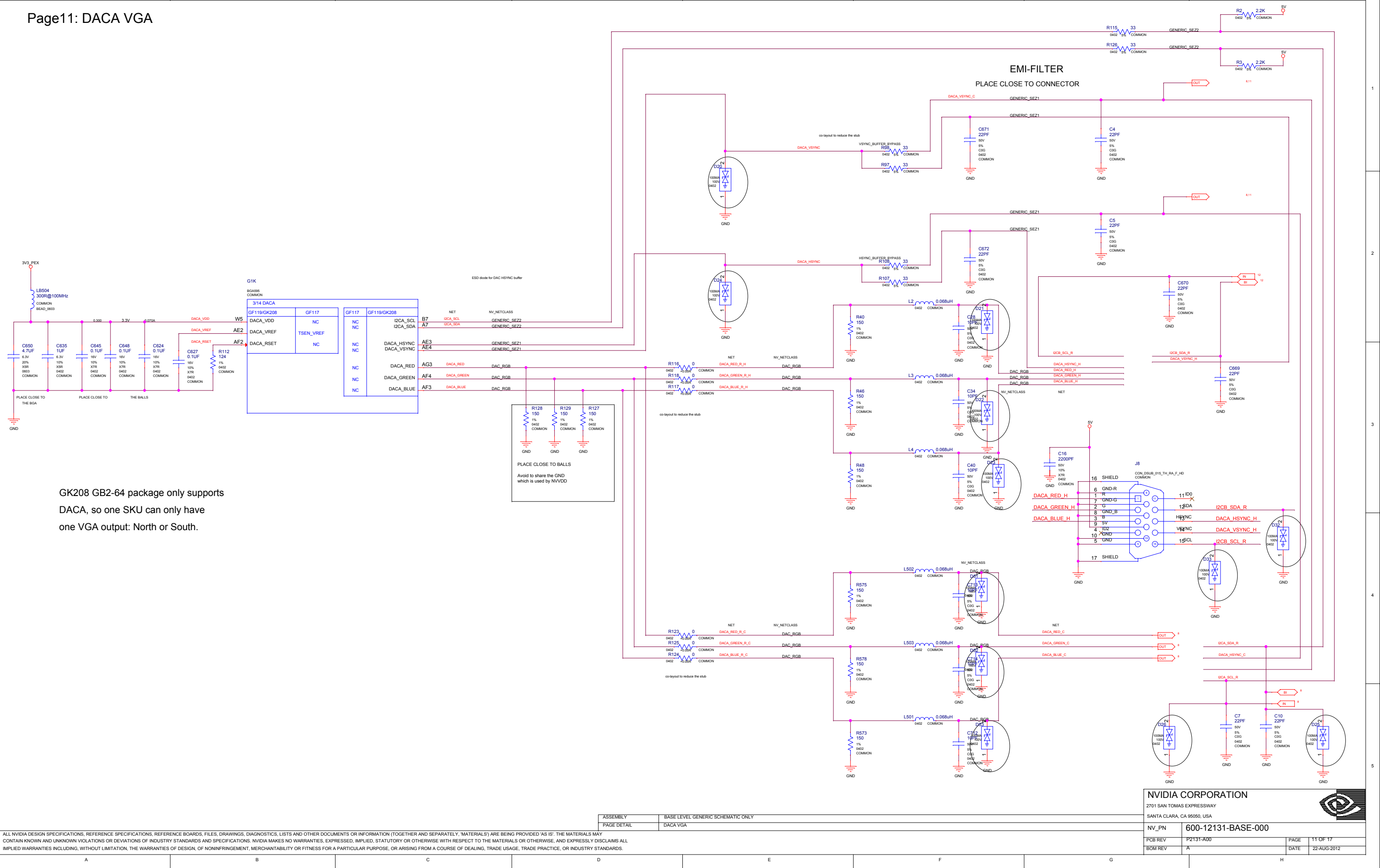
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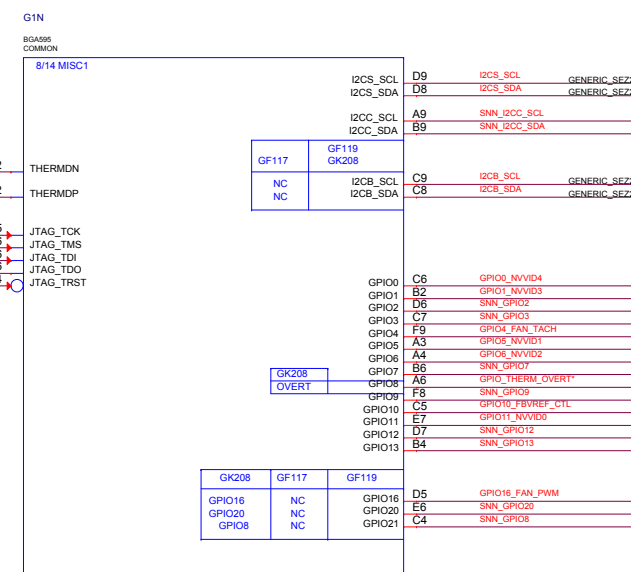
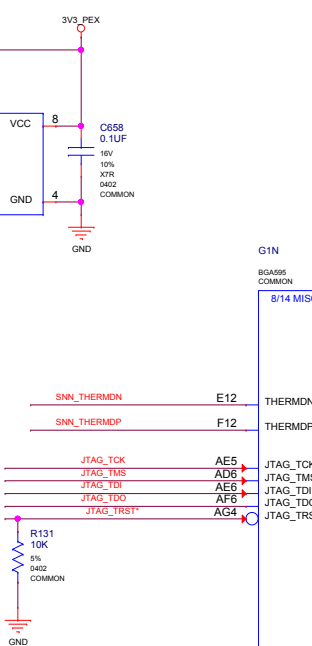
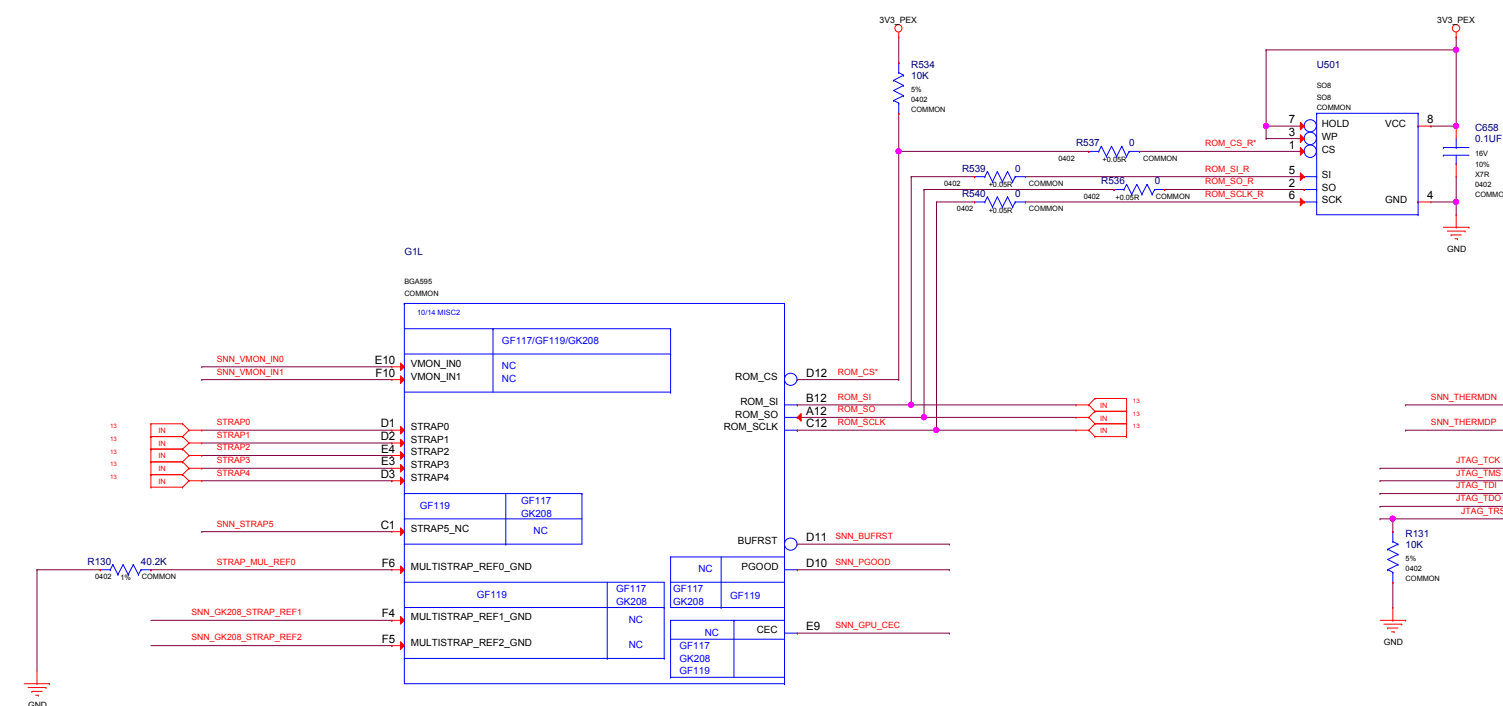
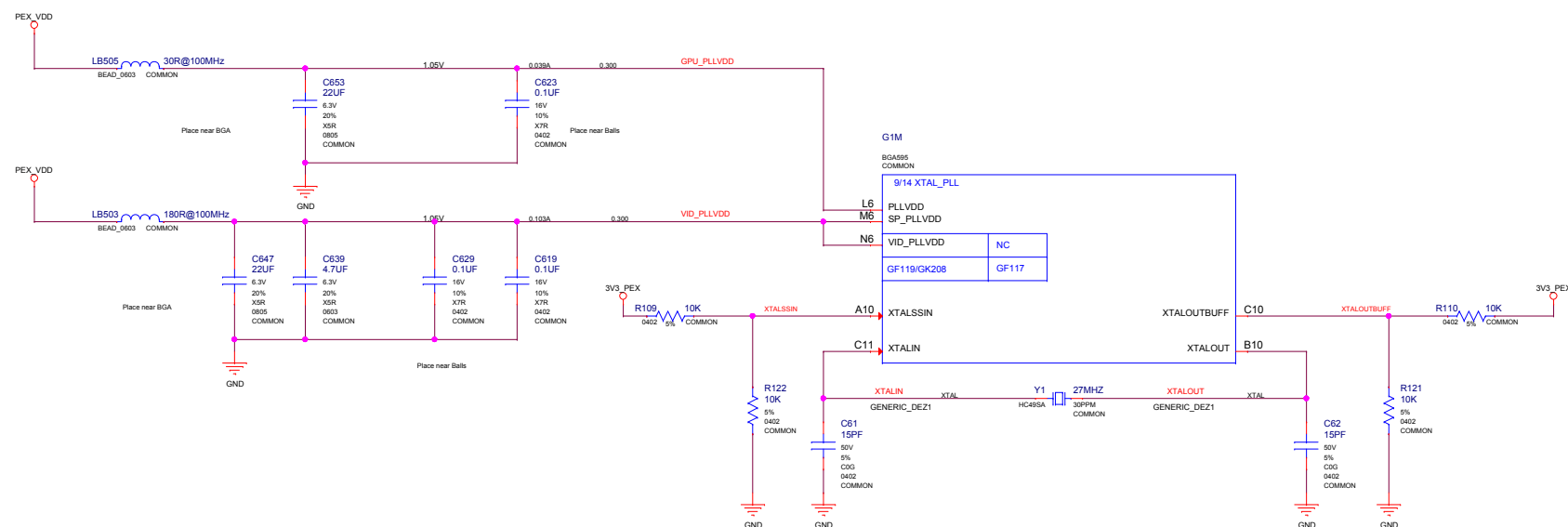


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	UNUSED IFPD, IFPE & IFPF

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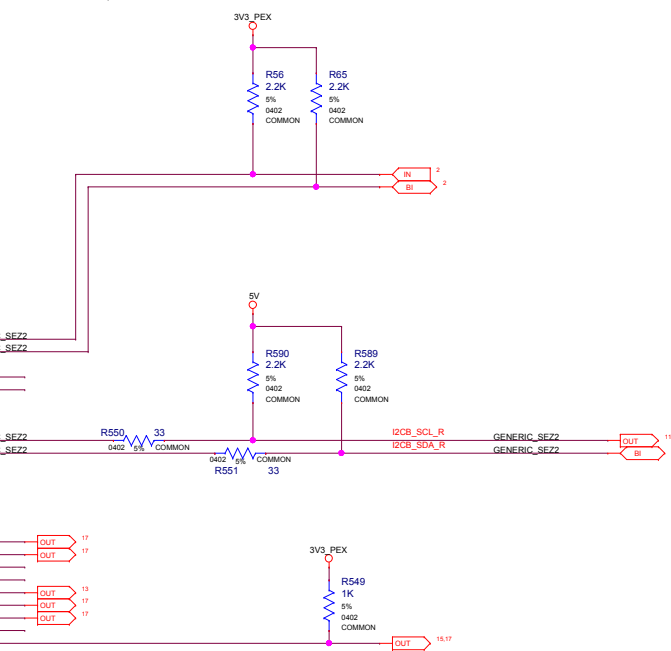
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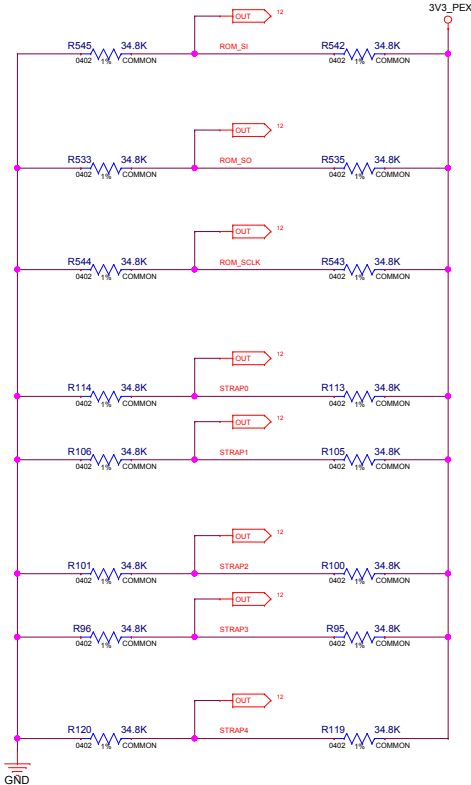
Smart Fan

XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

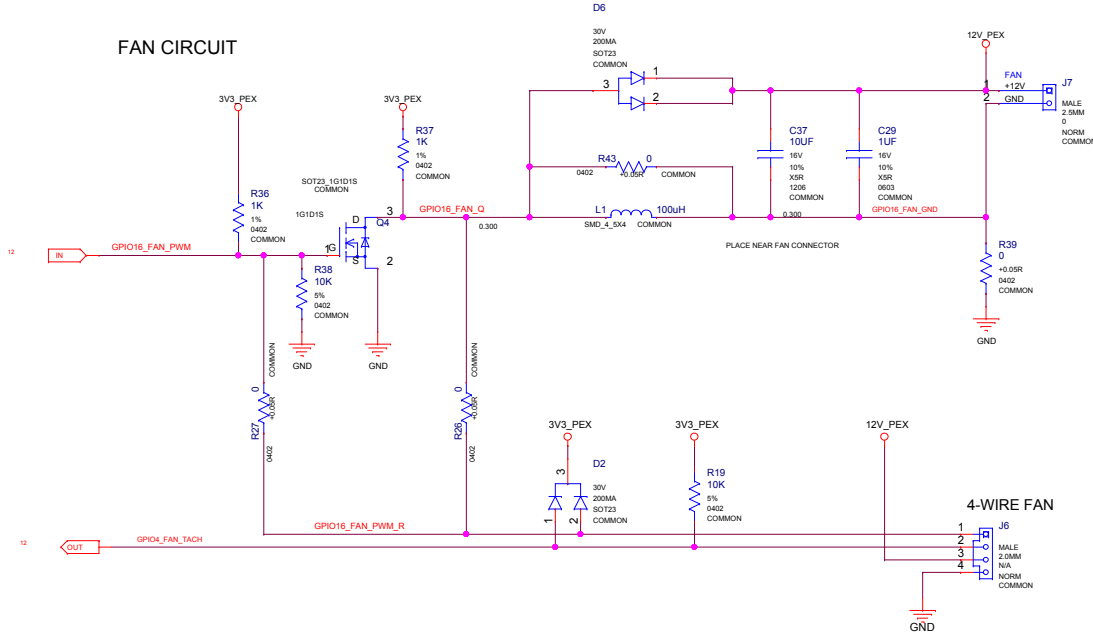


Multilevel Straps


GK208 Straps

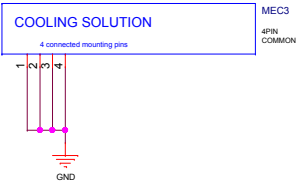
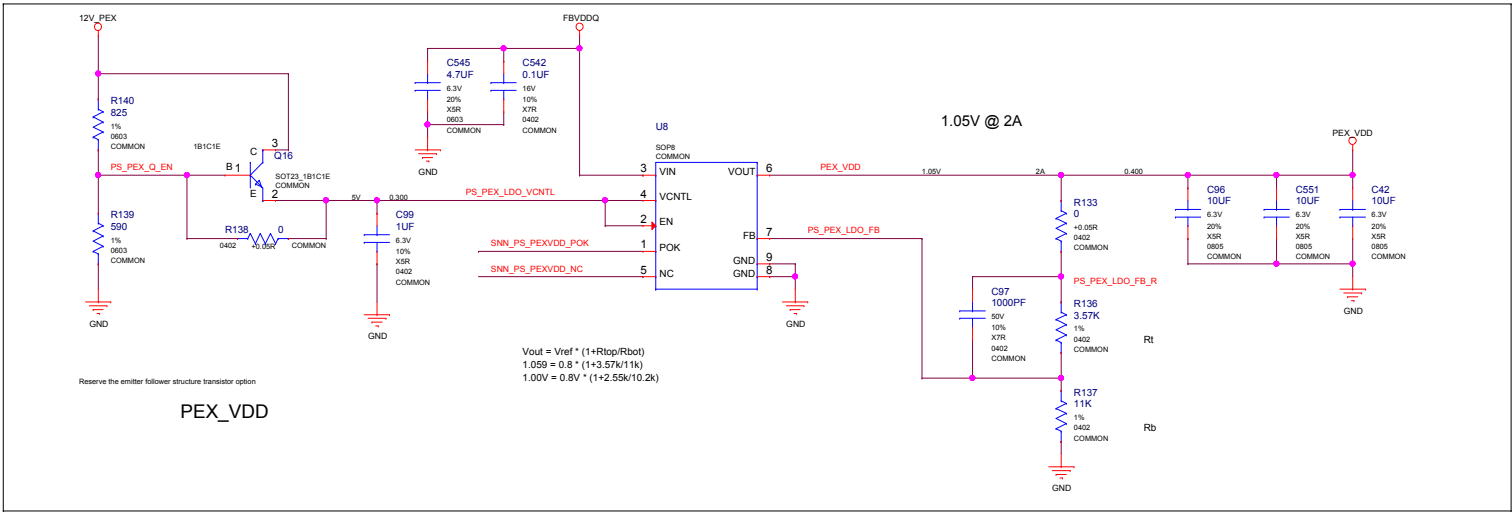
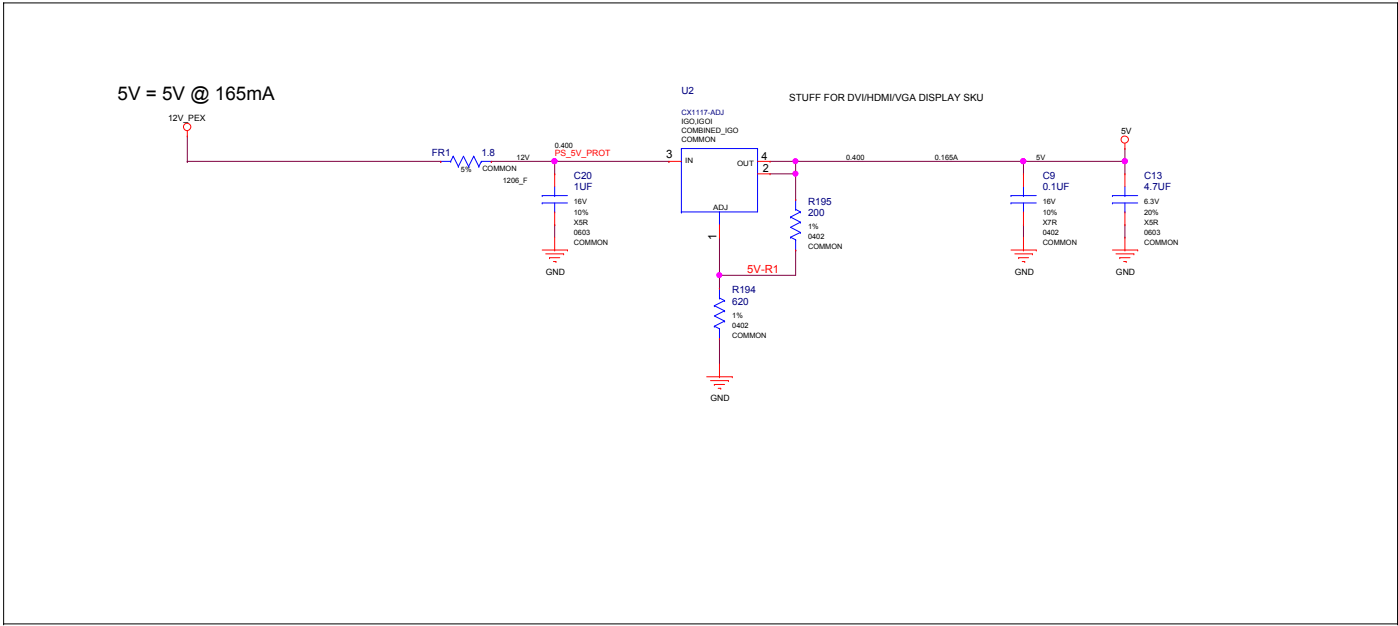


Bit Signal	Values				
03: RAMCFG[3]					ROM_SI
02: RAMCFG[2]	0000	Reserved			
01: RAMCFG[1]	0001	128Ma16 GDORS X16 64bit Elpida			
	0010	128Ma16 GDORS X16 64bit Hynix A-die			
00: RAMCFG[0]	0011	128Ma16 GDORS X16 64bit Samsung D-die			
03: FB[1]	01	128MB			ROM_SO
02: FB[0]	10	256MB			
01: SMB_ALT_ADDR	0	DISABLED	1	ENABLED	
00: VGA_DEVICE	0	DISABLED	1	ENABLED	
03: PCI_DEVID_EXT	SKU0	0	SKU1	TBD	ROM_SCLK
02: SUB_VENDOR	0	NO_BIOS	1	BIOS	
01: PCI_DEVID_EXT_BITS	SKU0	0	SKU1	TBD	
00: PEX_FLT_EN_TERM100	0	DISABLED	1	ENABLED	
03: USER[3]	0000	INIT			
02: USER[2]					Strap0
01: USER[1]					
00: USER[0]					
03: XIG0_PADCFG_LUT_ADR[3]	0000	DISKTOP_DEFAULT	1000	DISKTOP_NTHRS	
	0001	MOBILE_DEFAULT	1001	MOBILE_NTHRS_NAMP	
02: XIG0_PADCFG_LUT_ADR[2]	0010	MOBILE_NTHRS_LLAMP	1010	MOBILE_NTHRS_LLAMP	
	0011	MOBILE_NTHRS_LLAMP	1011	MOBILE_NTHRS_LLAMP	
01: XIG0_PADCFG_LUT_ADR[1]	0100	MOBILE_NTHRS_HAMP	1100	MOBILE_NTHRS_HAMP	
	0101	MOBILE_NTHRS_HAMP	1101	MOBILE_NTHRS_HAMP	
00: XIG0_PADCFG_LUT_ADR[0]	0110	MOBILE_NTHRS_HHAMP	1110	MOBILE_NTHRS_HHAMP	
	0111	MOBILE_NTHRS_HHAMP	1111	MOBILE_NTHRS_HHAMP	
03: PCI_DEVID[3]	SKU0	0010			Strap2
02: PCI_DEVID[2]					
01: PCI_DEVID[1]					
00: PCI_DEVID[0]	SKU1	TBD			
03: SOR3_EXPOSED	0	DISABLED	1	ENABLED	Strap3
02: SOR2_EXPOSED	0	DISABLED	1	ENABLED	
01: SOR1_EXPOSED	0	DISABLED	1	ENABLED	
00: SOR0_EXPOSED	0	DISABLED	1	ENABLED	
02: PCIE_SPEED_CHANGE_GEN3	0	DISABLED	1	ENABLED	Strap4
01: PCIE_MAX_SPEED	0	GEN1	1	GEN23	
00: DP_PLL_VDDO_3V3	0	USE IV8	1	USE3V3	



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PCI-E Reset, STRAPS & FAN

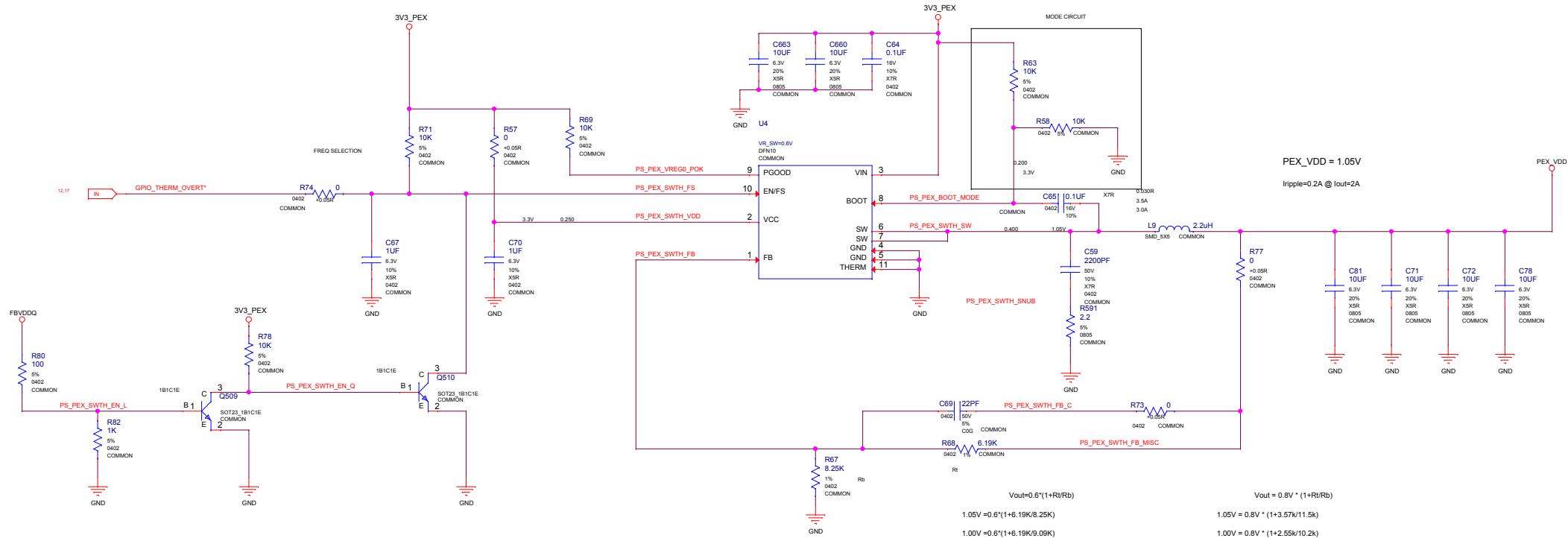
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 5V, PEXVDD

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OPEN VREG TYPE-0

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PAGE DETAIL	PEX_VDD: Open VR Type0

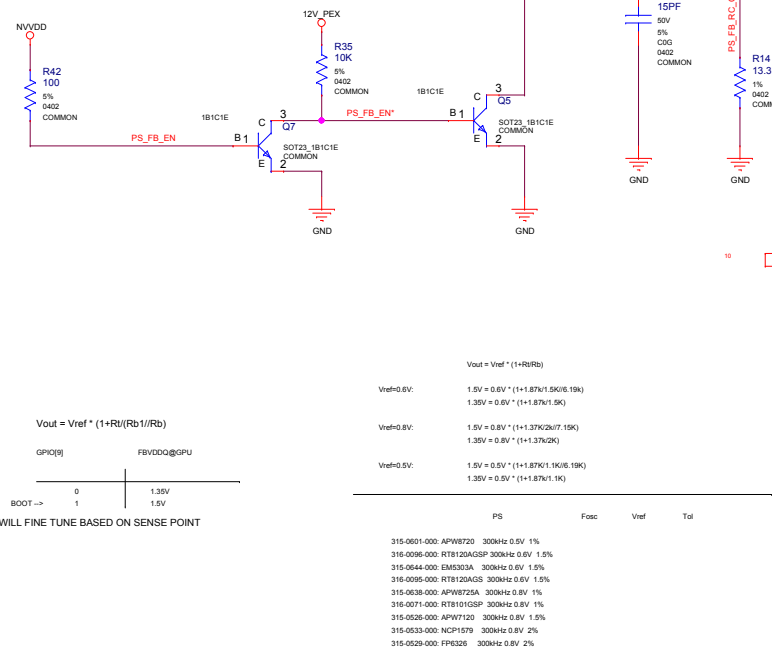
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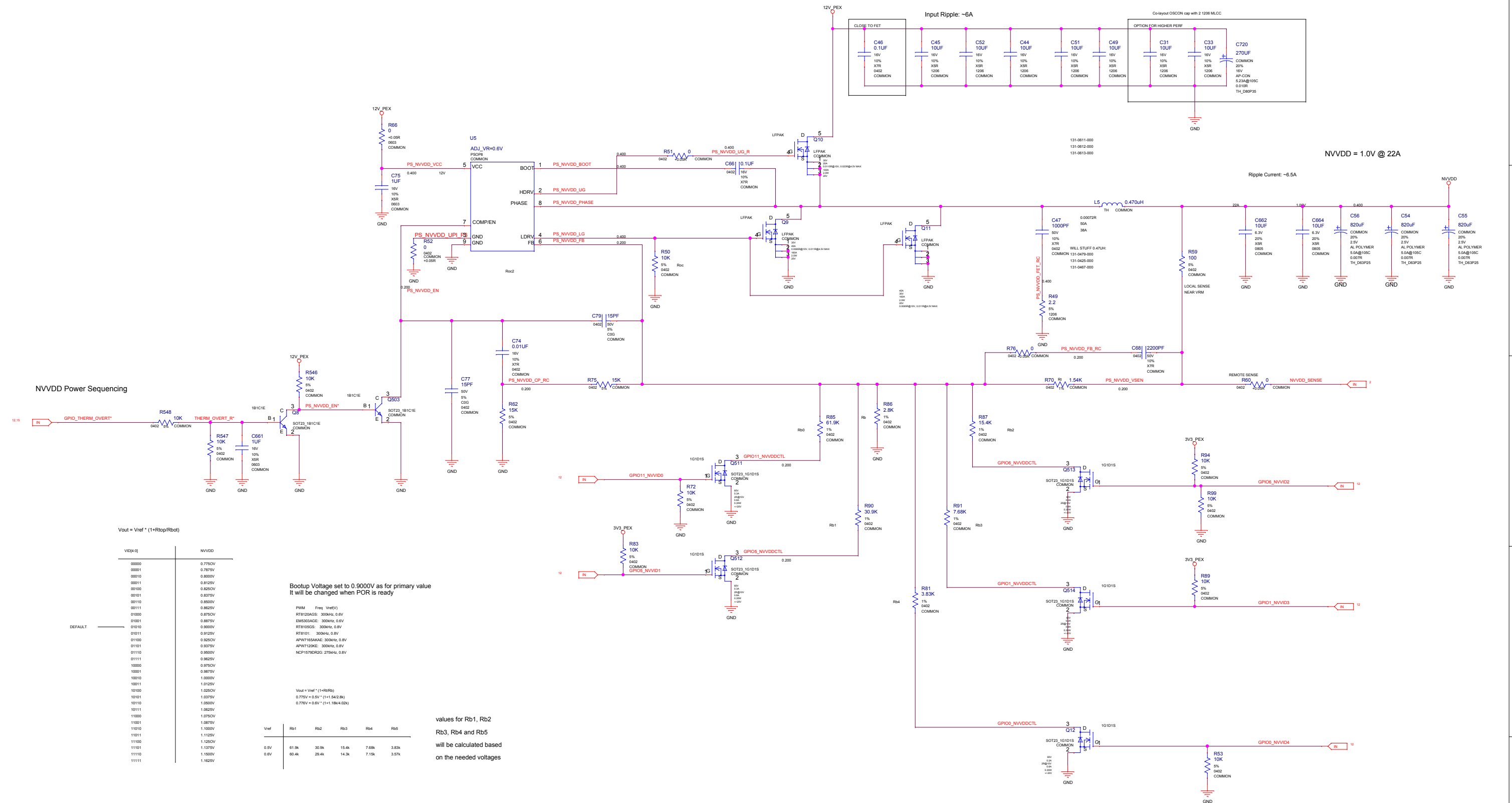



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FBVDDQ Power Sequencing





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