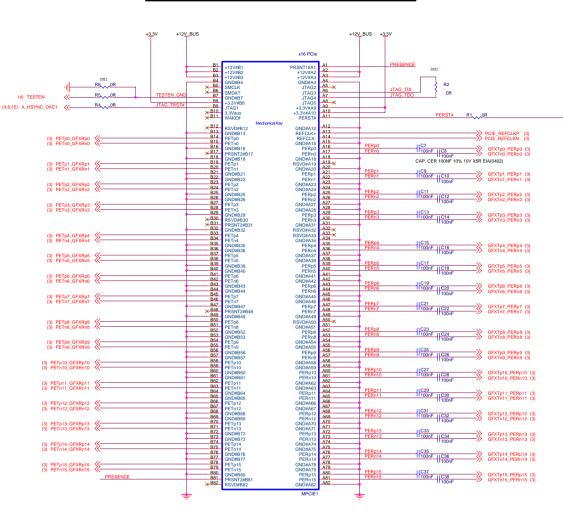


# **PCI-EXPRESS EDGE CONNECTOR**



Power Sequence Circuit to ensure SMPS\_EN is released after +12V\_BUS and +3.3V\_BUS are both in regulation.
Pull-up may or may not be required on SMPS\_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS\_EN will be helt low Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS\_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)
Typical trigger when +3.3V ramps above 2.2V (650mV)

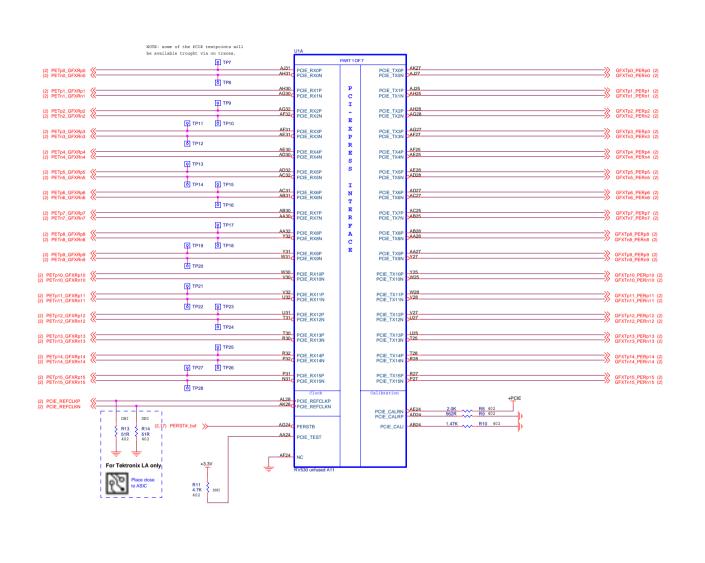
Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS\_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)
Typical trigger when +12V ramps above 10V (1.1V)

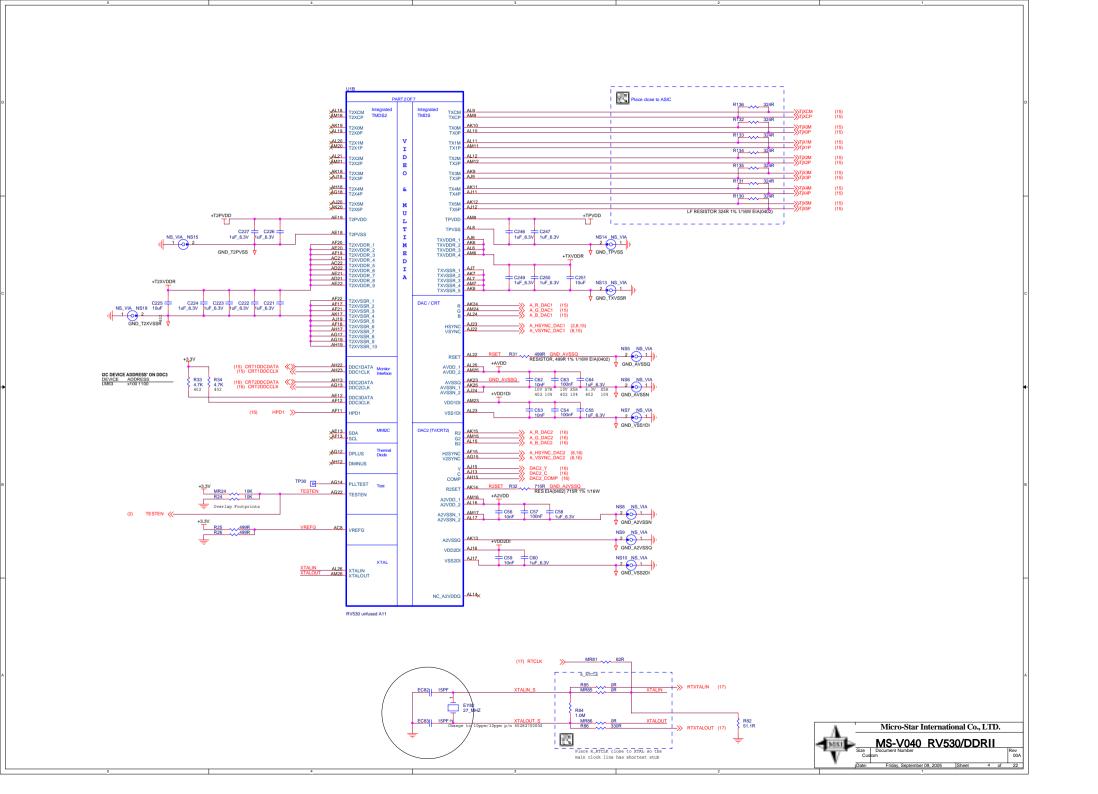


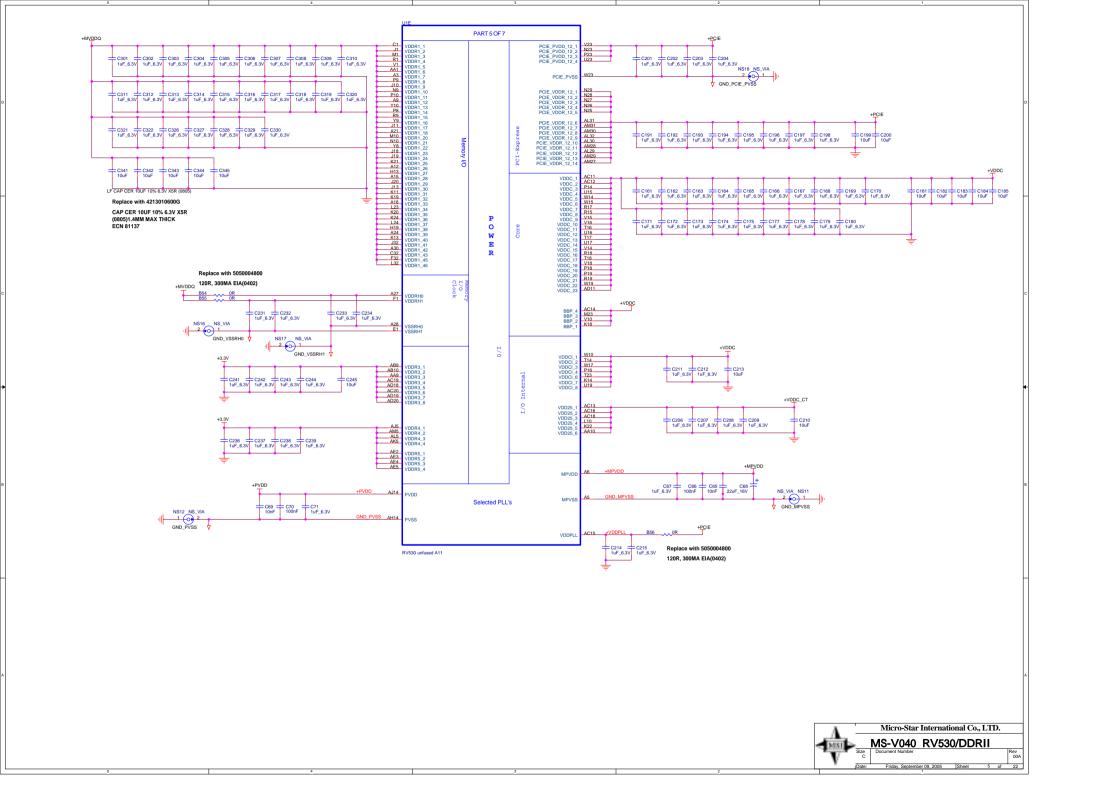
CAP CERAMIC 100NE 10% 10V X5R EIA(0402)





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#### RV530 MEMORY CHANNELS A and B Channel B Channel A (14) M\_MDB[63..0] «>> M\_MAB[12..0] (14) Part 4 of 7 (13) M\_MDA[63..0] «> →>> M\_MAA[12..0] (13) Part 3 of 7 M31 DOA, 0 M30 DOA, 1 L30 DOA, 2 L30 DOA, 2 L30 DOA, 2 L30 DOA, 3 L30 DOA, 2 L30 DOA, 3 L30 DOA, 2 L30 DOA, 3 L30 DOA, 3 L30 DOA, 3 L30 DOA, 3 L30 DOA, 5 MAA\_0 MAA\_1 MAA\_2 MAA\_3 MAA\_6 MAA\_6 MAA\_7 MAA\_1 MAA\_1 MAA\_1; MAA\_1; MAA\_1; MAA\_1; MEMORY INTERFACE A MEMORY INTERFACE B M\_MAA[15..14] (13) >>> M\_DQMA#[7..0] (13) DQMBb DQMBb DQMBb DQMBb DQMBb DQMBb DQMBb DQMBb DQMBb DQMAb\_C DQMAb\_C DQMAb\_C DQMAb\_C DQMAb\_C DQMAb\_C DQMAb\_C ✓ M\_QSB[7..0] (14) ✓ M\_QSA[7..0] (13) QSB\_0 QSB\_1 QSB\_2 QSB\_3 QSB\_4 QSB\_5 QSB\_6 QSB\_7 QSA\_G QSA\_G QSA\_G QSA\_G QSA\_G QSA\_G QSB\_0B QSB\_1B QSB\_2B QSB\_3B QSB\_4B QSB\_5B QSB\_6B QSB\_7B QSA\_0B QSA\_1B QSA\_2B QSA\_3B QSA\_4B QSA\_5B QSA\_6B QSA\_7B ODTB0 $\begin{array}{c} \text{ODTA0} \\ \text{ODTA1} \end{array}$ $\begin{array}{c} \text{D24} \\ \times \end{array}$ $\begin{array}{c} \text{ODTA0} \end{array}$ (13) For DDR2 CLKB0 CLKB0b C2 >>> CKEB0 CKEB0 CKEA0 \_B30 \_\_\_\_\_\_\_ CKEA0 (13) o<sup>E2</sup>→>> RASB#0 RASB0b RASA0b DB28 >>> RASA#0 (13) CASB0b DD3 CASB#0 CASA0b DC29 >>> CASA#0 (13) +MVDDQ WEB0b DB2 >> WEB#0 +MVDDQ (14) WEA0b 0B31 >>> WEA#0 (13)

C355 C356 100nF 10nF

CLKA1 CLKA1 (13)
CLKA1b CLKA#1 (13)

CKEA1 C22 >>> CKEA1 (13)

RASA1b 0B24 >>> RASA#1 (13)

CASA1b 0B22 >>> CASA#1 (13)

WEA1b 0B21 >>> WEA#1 (13)

C351 C352 100nF 10nF

R162 100R 1%



CKEB1 13 CKEB1

RASB1b OJ2 >>> RASB#1

CASB1b OL2 >>> CASB#1

WEB1b 0M2\_>> WEB#1

K2\_→> CSB#1\_0 (14)

DRAM RST

TEST MOLK

TEST\_YCLK

MEMTEST

R169 > 243R LF RES EIA(0402) 243R 1% 1/16W

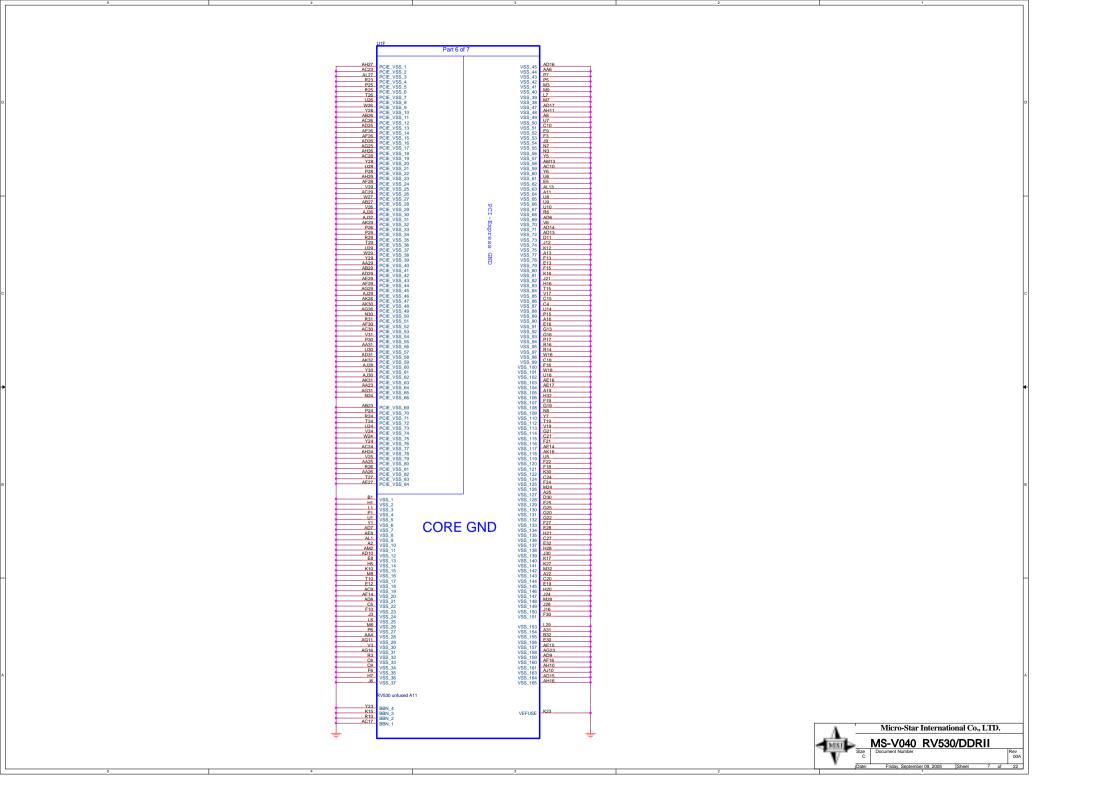
R172 R171 R170 4.7K 4.7K 4.7K

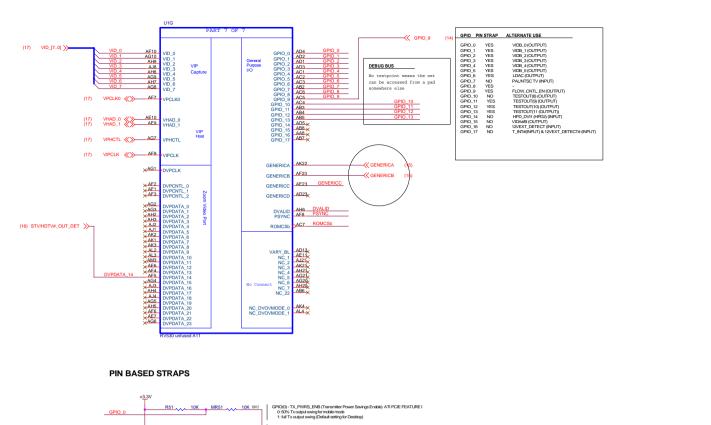
RESISTOR, 4.7K 5% 1/16W EIA(0402)

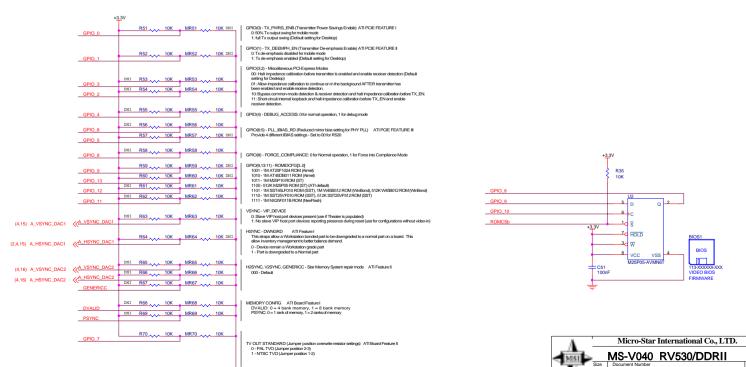
(14)

(14)

(14)

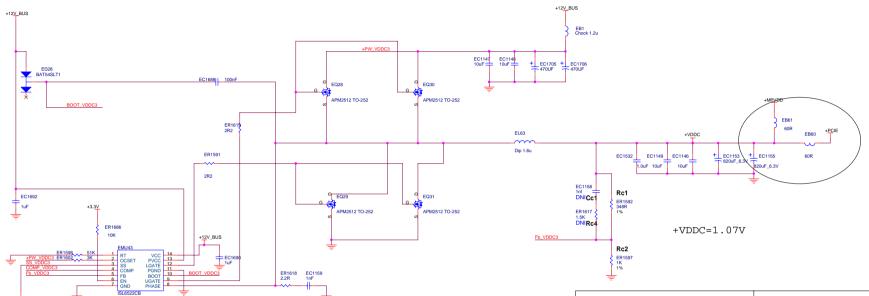






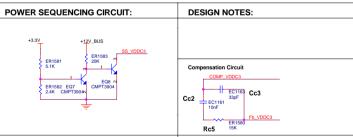
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### **CORE REGULATOR VDDC**



Lower MOSFET should be surrounded by a lot of copper for heat dissipation

ISL6522CB : SOIC ISL6522CV : TSSOF



#### FOR ALTERNATE #1

#### **FOR ALTERNATE #2**

Remove R374, R375, R371, C168 and U32 Change C157 for 10 uF and C121 for 1 uF Replace C764 by 0 Ohm resistor Install R370, R112, R954, R305-R308, C16&eplace R314 with a bead C159 and MU32 Remove R954, R370, R305

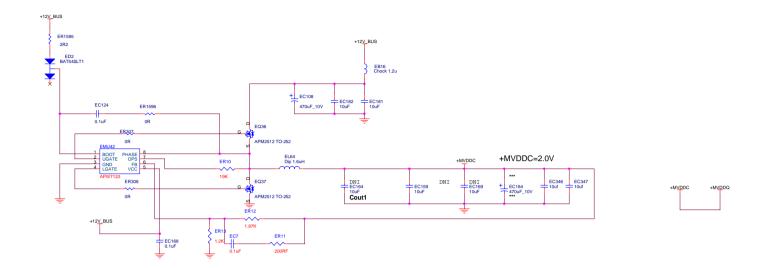
Remove R954, R370, R305-R308, C159, R112, C160 and MU32

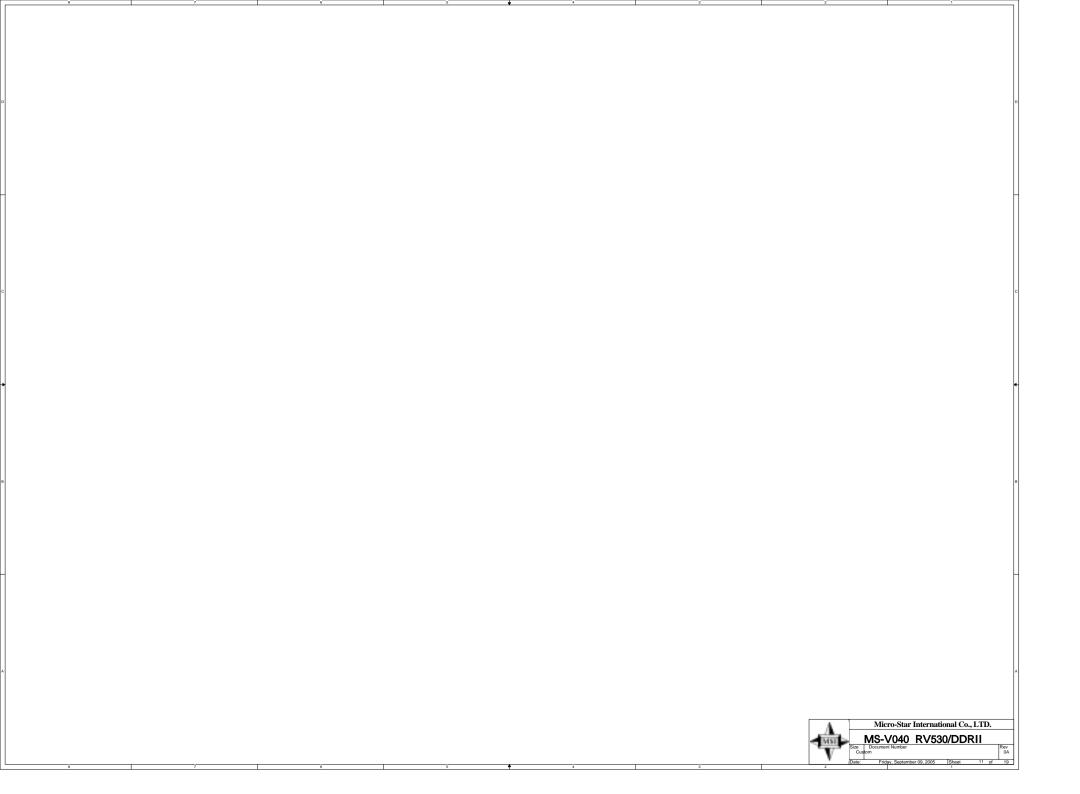
Install R374, R375, R371, C168 and U32

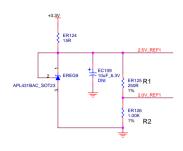
# Compensation circuit

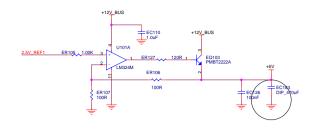
Rc1 = 10K, Rc2 = 8.06K R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF

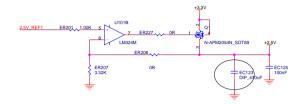


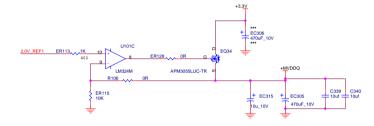


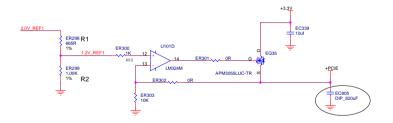










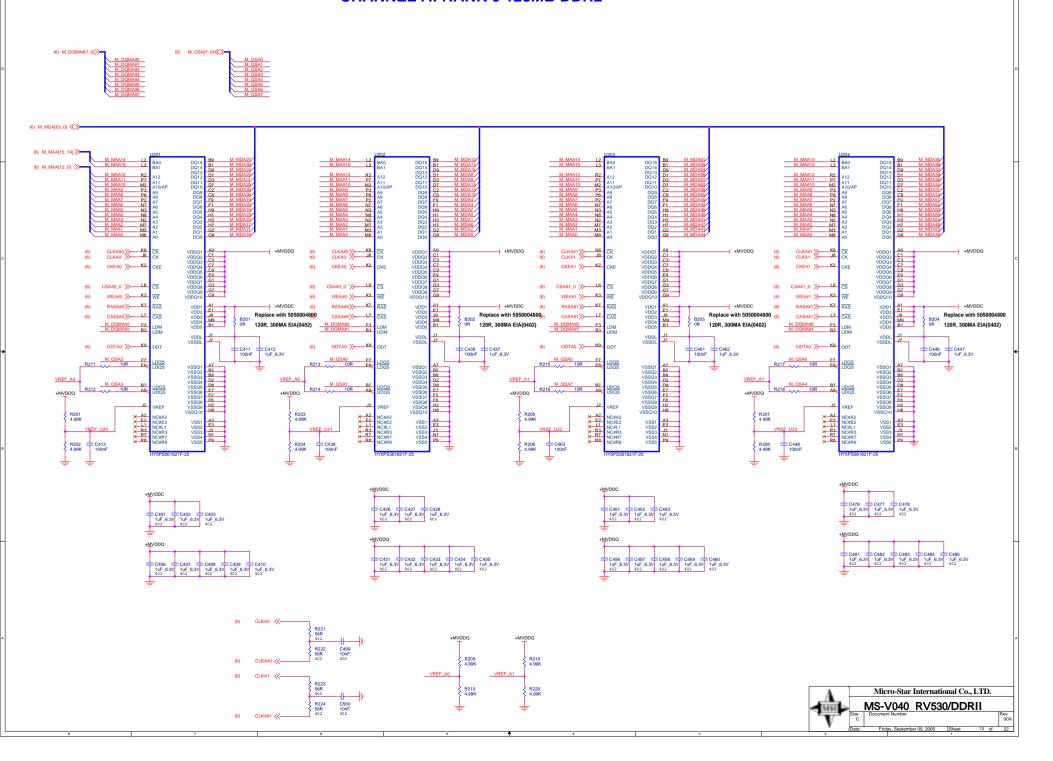


+2	.5V +/	AVDD +	A2VDD +V	DD1DI +VI	DD2DI +P	/DD +TF	PVDD +T	(VDDR +T2	PVDD +T2	XVDDR +VDD	C_CT
		B922 0R	B923 0R	B924 0R	B925 0R	B926 0R	B927 0R	B928 0R	B929 0R	B930 0R	EB9 0R
		1	1								

Replace with 5050004800 120R, 300MA EIA(0402)

1	<u>А</u>	Micro-Star International Co., LTD.							
		MS-V040 RV530/DDRII							
	V	Size C	Document Number	Rev 00A					
		Date:	Friday, September 09, 2005 Sheet 12 of	22					

# **CHANNEL A: RANK 0 128MB DDR2**



# **CHANNEL B: RANK 0 128MB DDR2**

