MS8906

ATI R300 9500Pro, 8MX16 DDR, DUAL VGA, VIDEO IN, TV-OUT, AGP 8X

FREQUENCY	MHZ
CORE	275
MEMORY	250

MS-8906 ATI R300 9500PRO

Size	Document Number	Rev
B	COVER	0A

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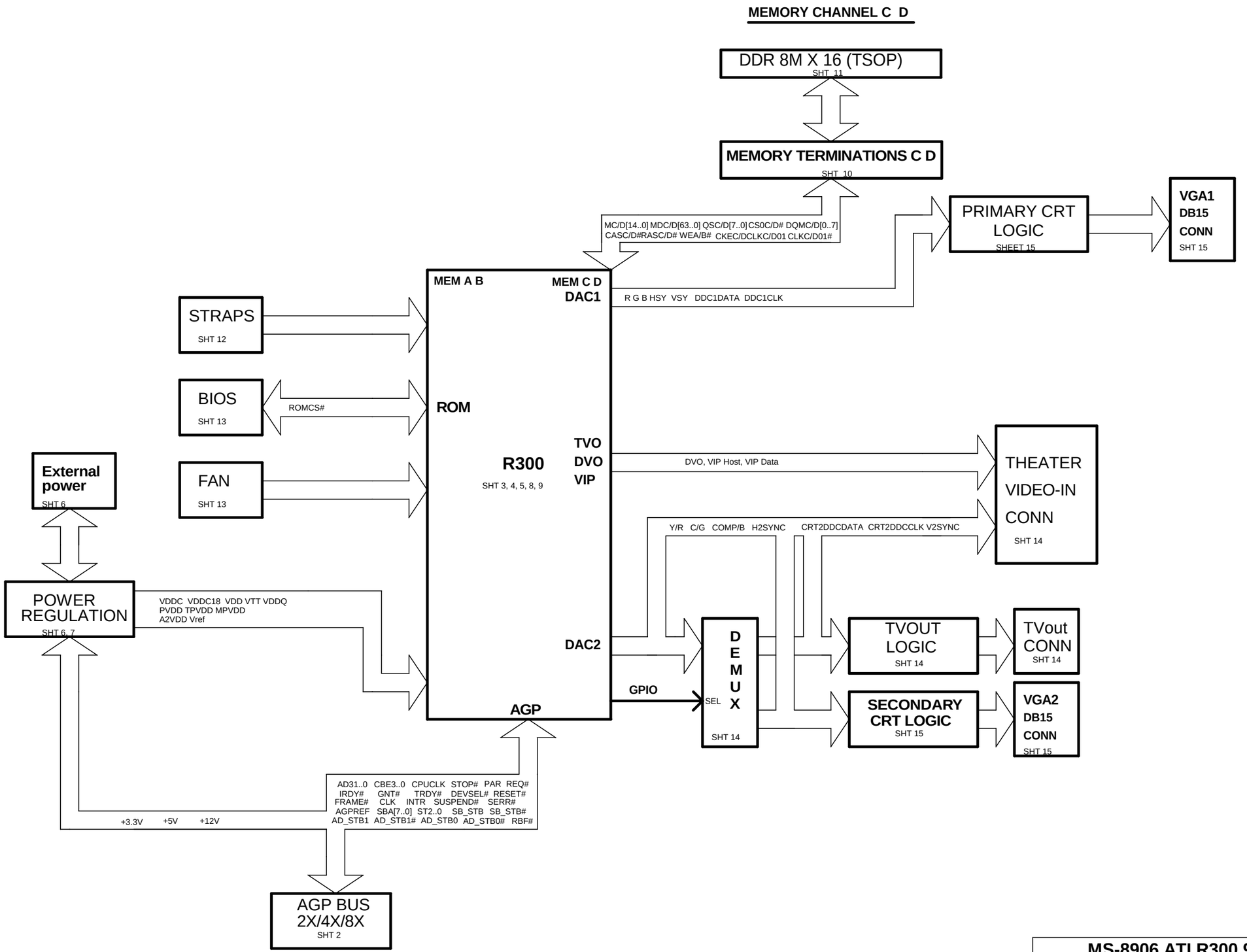

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Size	Document Number	Rev
Custom	**BLOCK**	0A
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2X/4X/8X AGP BUS

GND_AVSSN GND_MPVSS GND_PVSS GND_TPVSS GND_TXVSSR GND_A2VSSN GND_A2VSSQ GND_AVSSQ GND_R2SET GND_RSET GND_TVVSSN

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

+12V_BUS — C1 4.7uF 16V ALU
+5V_BUS — C2 100uF 16V
+3.3V_BUS — C3 100uF 16V

MAGP1 — UNIVERSAL AGP BUS

A1	12V	B1	OVRCNT#
A2	TYPEDET#	B2	5.0V
A3	GC_DET#/RESEVED	B3	5.0V
A4	USB-	B4	USB+
A5	GND	B5	GND
A6	INTA#	B6	INTB#
A7	RST#	B7	CLK
A8	GNT#	B8	REQ#
A9	VCC3.3	B9	VCC3.3
A10	ST1	B10	ST0
A11	MB_DET#/RESERVED	B11	ST2
A12	DBI_HI/PIPE#	B12	RBF#
A13	GND	B13	GND
A14	WBF#	B14	DBI_LO/RESERVED
A15	SBA1	B15	SBA0
A16	VCC3.3	B16	VCC3.3
A17	SBA3	B17	SBA2
A18	SB_STB#	B18	SB_STB
A19	GND	B19	GND
A20	SBA5	B20	SBA4
A21	SBA7	B21	SBA6
A22	KEY	B22	KEY
A23	KEY	B23	KEY
A24	KEY	B24	KEY
A25	KEY	B25	KEY
A26	AD30	B26	AD31
A27	AD28	B27	AD29
A28	VCC3.3	B28	VCC3.3
A29	AD26	B29	AD27
A30	AD24	B30	AD25
A31	GND	B31	GND
A32	AD_STB1#	B32	AD_STB1
A33	C/BE3#	B33	AD23
A34	VDDQ	B34	VDDQ
A35	AD22	B35	AD21
A36	AD20	B36	AD19
A37	GND	B37	GND
A38	AD18	B38	AD17
A39	AD16	B39	C/BE#2
A40	VDDQ	B40	VDDQ
A41	FRAME#	B41	IRDY#
A42	KEY	B42	KEY
A43	KEY	B43	KEY
A44	KEY	B44	KEY
A45	KEY	B45	KEY
A46	TRDY#	B46	DEVSEL#
A47	STOP#	B47	VDDQ
A48	PME#	B48	PERR#
A49	GND	B49	GND
A50	PAR	B50	SERR#
A51	AD15	B51	C/BE1#
A52	VDDQ	B52	VDDQ
A53	AD13	B53	AD14
A54	AD11	B54	AD12
A55	GND	B55	GND
A56	AD9	B56	AD10
A57	C/BE0#	B57	AD8
A58	VDDQ	B58	VDDQ
A59	AD_STB0#	B59	AD_STB0
A60	AD6	B60	AD7
A61	GND	B61	GND
A62	AD4	B62	AD5
A63	AD2	B63	AD3
A64	VDDQ	B64	VDDQ
A65	AD0	B65	AD1
A66	VREFGC	B66	VREFCG

AGP_C/BE#[3..0] — AGP_C/BE#[3..0] (3)
AGP_AD[31..0] — AGP_AD[31..0] (3)
AGP_SBA[7..0] — AGP_SBA[7..0] (3)
AGP_ST[2..0] — AGP_ST[2..0] (3)

(3) AGP_INTR#
TYDET R1 0R GND_TY
AGP_GC_8X_DET# — R2 0R
AGP_RST#
(3) AGP_GNT#
(3) AGP_MB_8X_DET# — R4 0R
(3) AGP_DBI_HI — R5 0R
(3) AGP_WBF#
+VDDQ_BUS — R7 8K2 — (3) AGP_SBSTB#
+VDDQ_BUS — R9 8K2 — (3) AGP_ADSTB1#
+VDDQ_BUS — R16 8K2 — (3) AGP_ADSTB0#
(3) AGP_FRAME#
(16) AGP_TRDY#_R
(3,16) AGP_TRDY#
(3,16) AGP_STOP#
(16) AGP_STOP#_R
DNI R13 0R
DNI R15 0R
(3) AGP_PAR
(3,16) AGP_VREFGC — AGP_VREFGC

AGP_AGPCLK_R — R3 0R — AGP_AGPCLK (3,16)
AGP_REQ# (3)
C4 10pF DNI
AGP_DBI_LO_R — R6 0R — AGP_RBF# (3) / AGP_DBI_LO (3)
AGP_SBSTB_R — R8 0R — AGP_SBSTB (3)
AGP_ADSTB1_R — R10 0R — AGP_ADSTB1 (3)
AGP_IRDY# (3)
AGP_DEVSEL#_R — AGP_DEVSEL#_R (3,16)
AGP_ADSTB0_R — R17 0R — AGP_ADSTB0 (3)
AGP_AGPREF (3)
C1127 1.0uF

+5V_BUS — C5 100nF — R19 10K
U2A 74ACT08MTC
(3,14,16) AGP_RESET# — R22 100R
AGP_RST#
PWGOOD_VDDC (6)
DNI R854 180R
R25 180R
DNI C731 100nF

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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Size B	Document Number AGP_4X / 8X_BUS	Rev 0A
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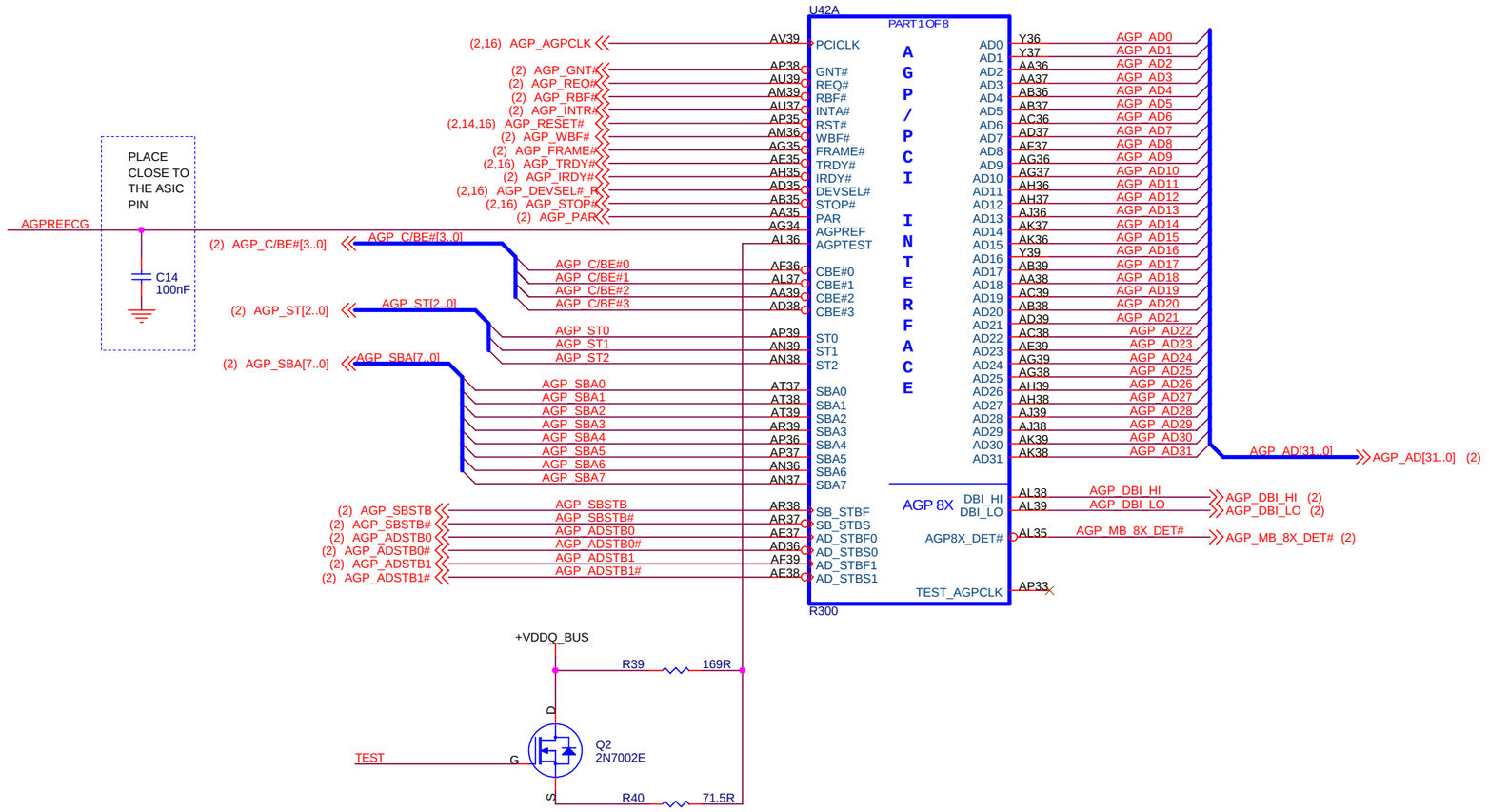

MS-8906 ATI R300 9500PRO		
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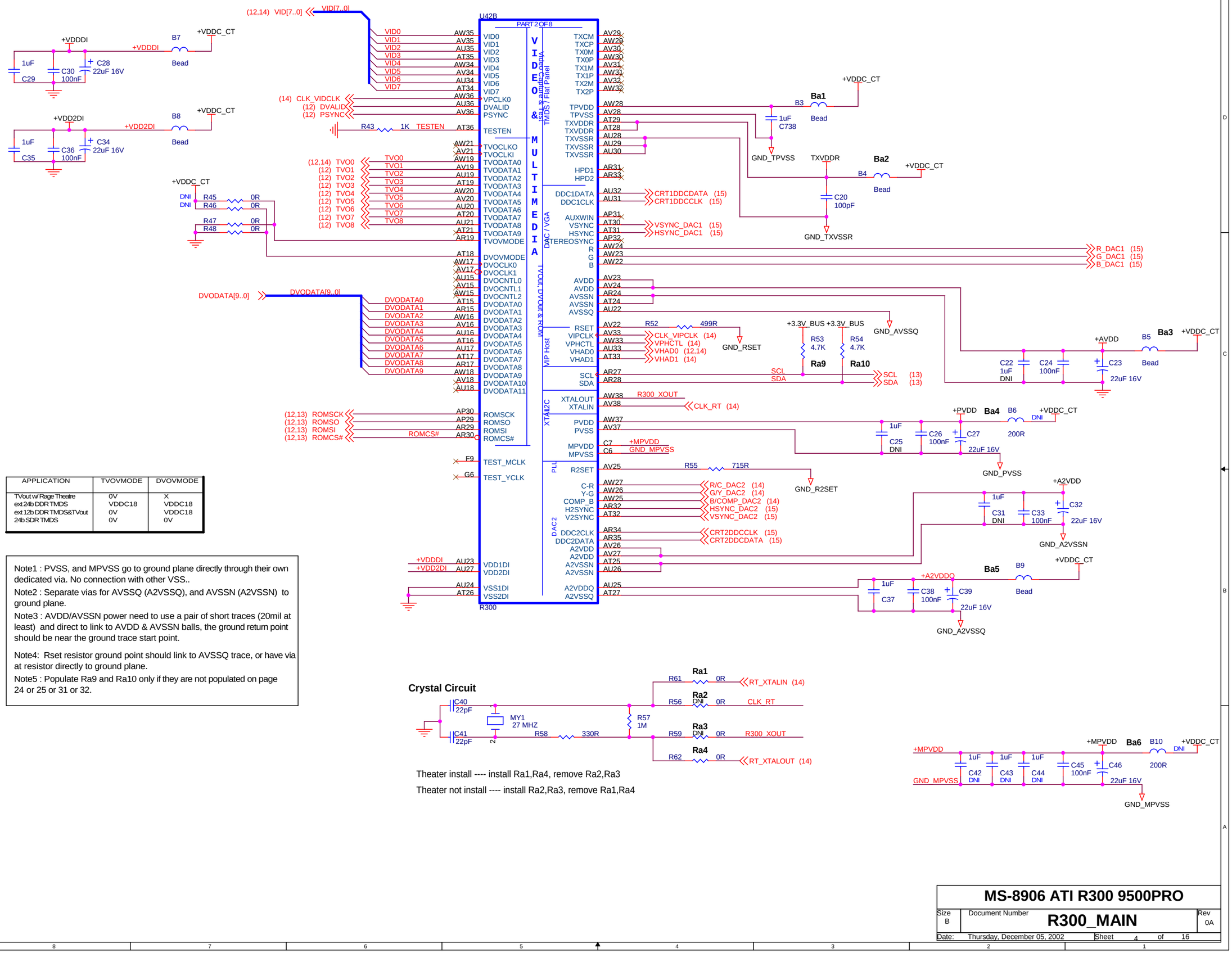

APPLICATION	TVOVMODE	DVOVMODE
TVout w/ Rage Theatre	0V	X
ext 24b DDR TMDS	VDDC18	VDDC18
ext 12b DDR TMDS&TVout	0V	VDDC18
24b SDR TMDS	0V	0V

Note1 : PVSS, and MPVSS go to ground plane directly through their own dedicated via. No connection with other VSS..

Note2 : Separate vias for AVSSQ (A2VSSQ), and AVSSN (A2VSSN) to ground plane.

Note3 : AVDD/AVSSN power need to use a pair of short traces (20mil at least) and direct to link to AVDD & AVSSN balls, the ground return point should be near the ground trace start point.

Note4: Rset resistor ground point should link to AVSSQ trace, or have via at resistor directly to ground plane.

Note5 : Populate Ra9 and Ra10 only if they are not populated on page 24 or 25 or 31 or 32.

Theater install ---- install Ra1,Ra4, remove Ra2,Ra3

Theater not install ---- install Ra2,Ra3, remove Ra1,Ra4

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B	R300_MAIN	0A

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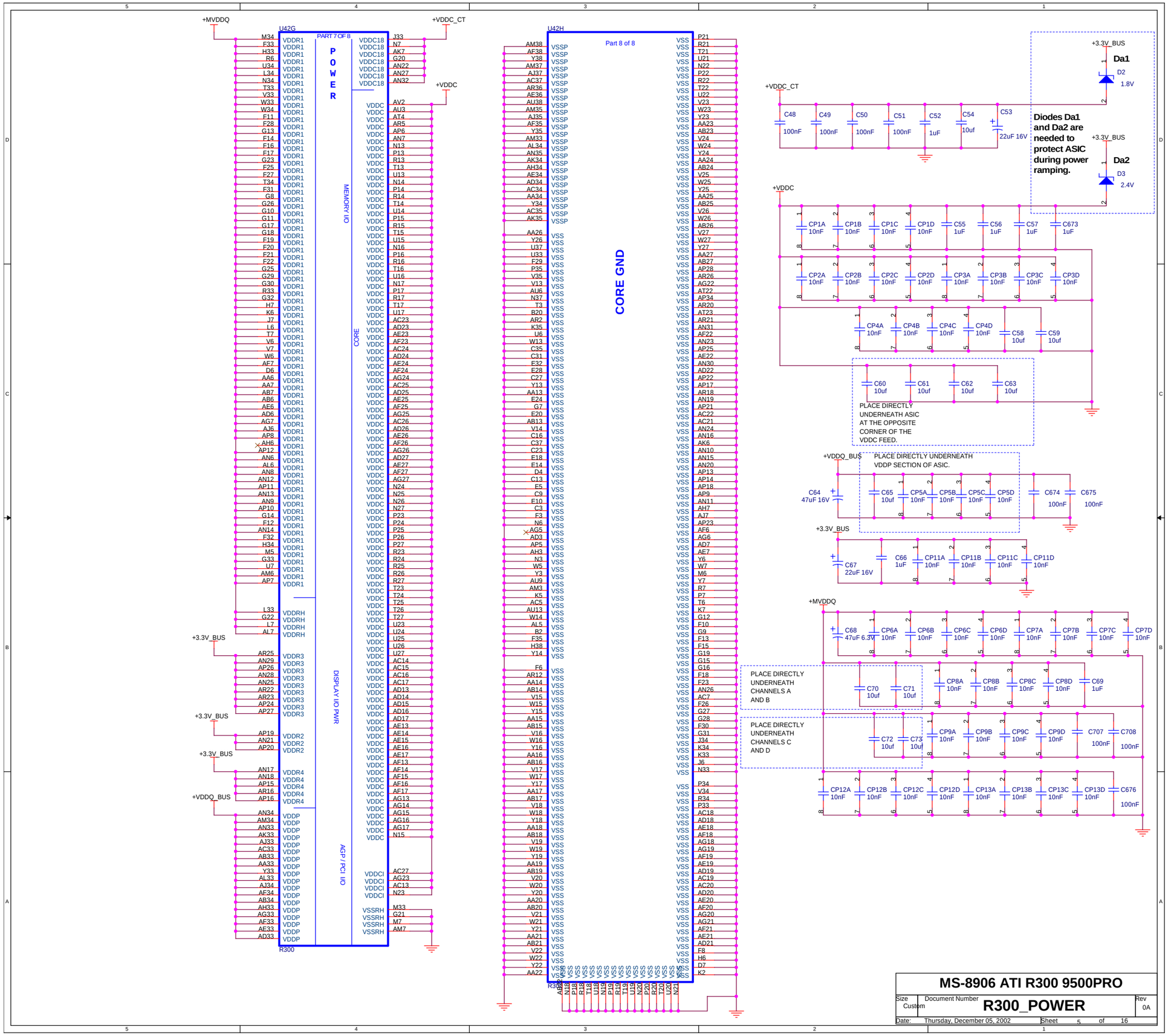
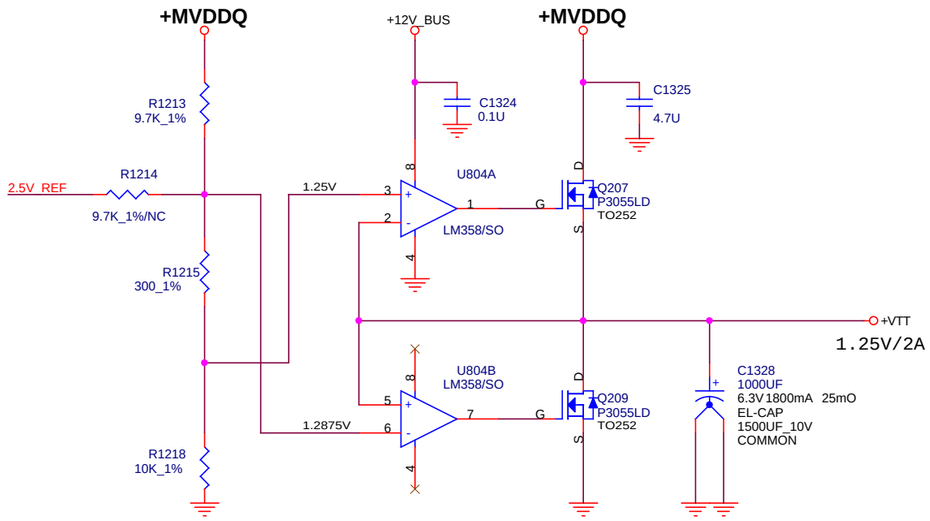
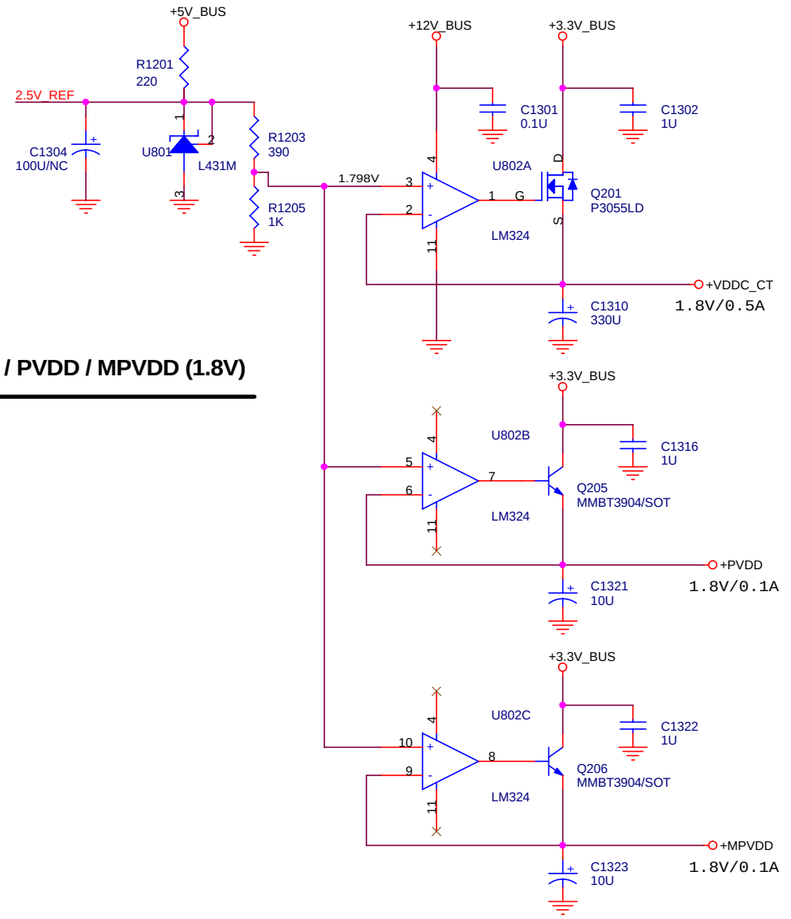


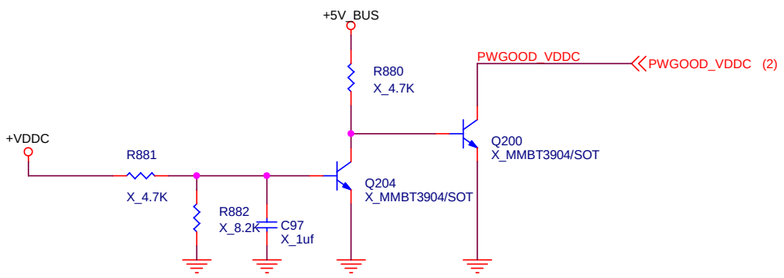
VTT



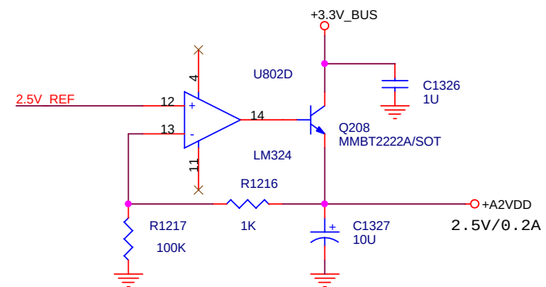
VDDC_CT / PVDD / MPVDD (1.8V)



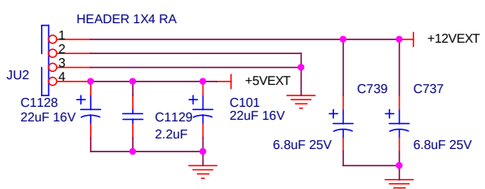
POWER SEQUENCE

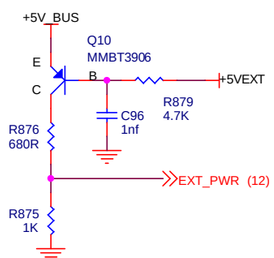


A2VDD (2.5V)



EXTERNAL POWER DETECT





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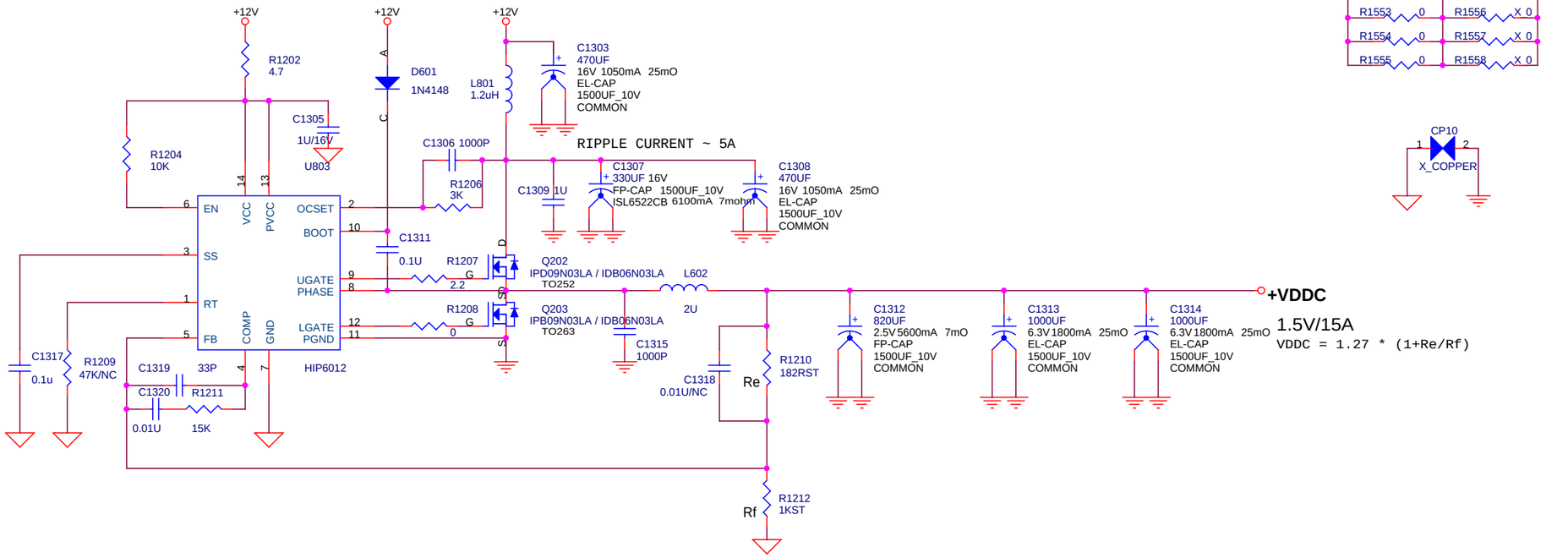
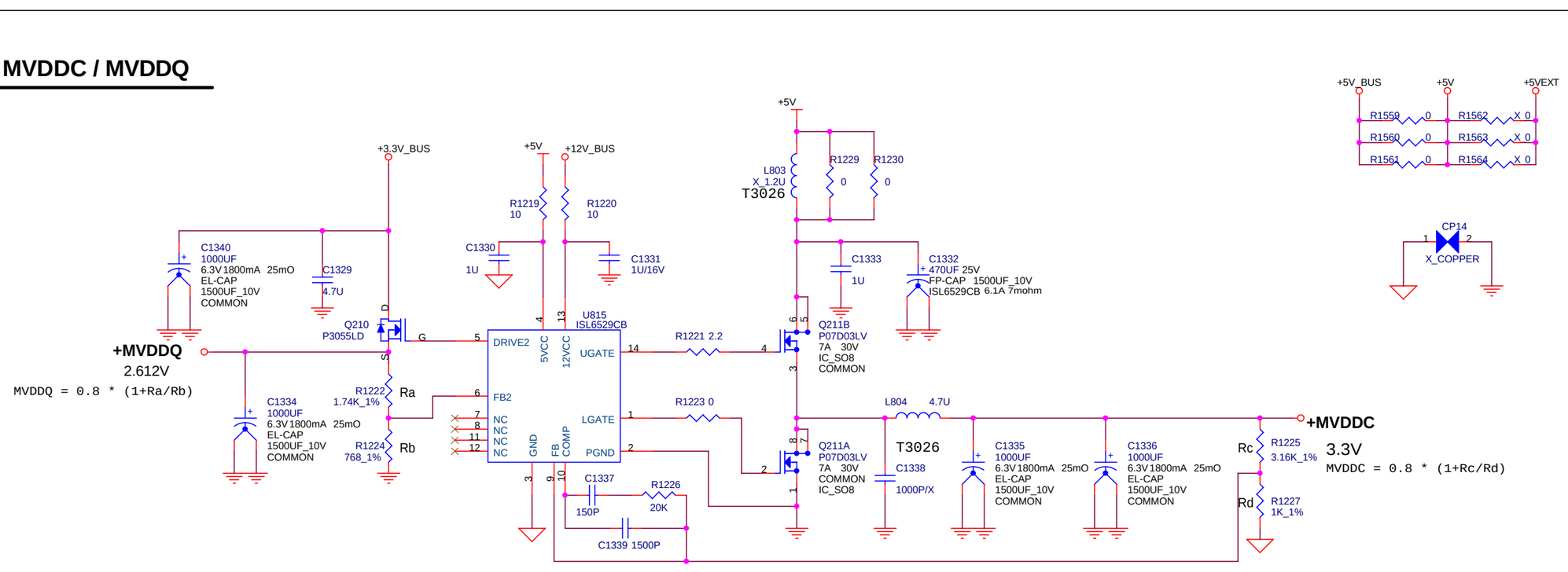
VDDC



MVDDC / MVDDQ



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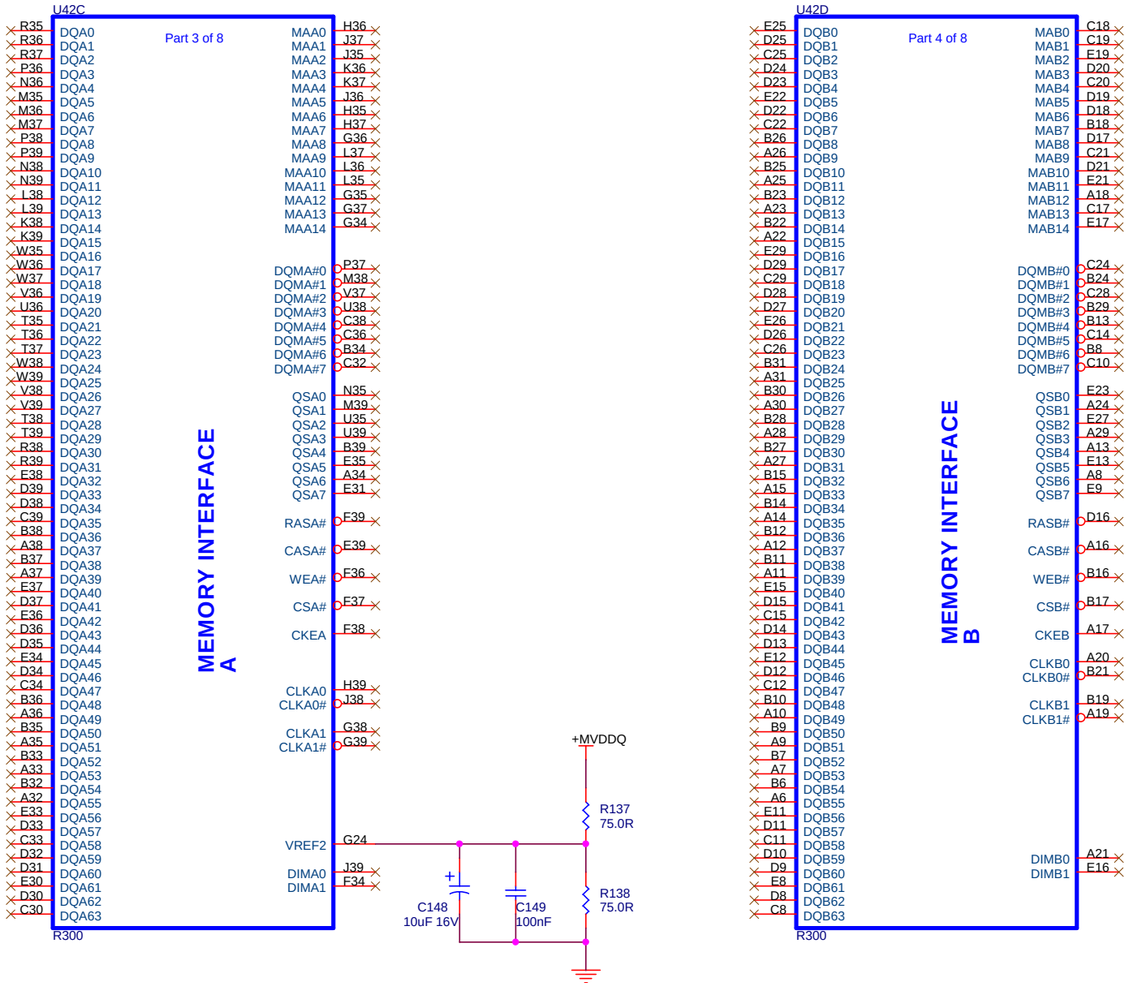
R-300
MEMORY CHANNELS A and B



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Size B	Document Number **MEMORY CHANNELS A and B**	Rev 0A
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R-300
MEMORY CHANNELS C and D

MAC8X → R905 0R → MAC8
MAC9X → R907 0R DNI → MAC9
R889 0R
R887 0R DNI

MAD8X → R906 0R → MAD8
MAD9X → R908 0R DNI → MAD9
R890 0R
R888 0R DNI

POPULATE R907,R887,R908,R888 FOR SAMSUNG 8X32 ONLY

(10,11) MAC[14..0]
(10) MDC[63..0]
MAC[14..0]

U42E — Part 5 of 8

MDC0	G4	DQC0	
MDC1	G3	DQC1	
MDC2	H5	DQC2	
MDC3	H4	DQC3	
MDC4	J4	DQC4	
MDC5	J3	DQC5	
MDC6	K4	DQC6	
MDC7	K3	DQC7	
MDC8	D2	DQC8	
MDC9	D1	DQC9	
MDC10	E2	DQC10	
MDC11	E1	DQC11	
MDC12	G2	DQC12	
MDC13	G1	DQC13	
MDC14	H2	DQC14	
MDC15	H1	DQC15	
MDC16	C5	DQC16	
MDC17	C4	DQC17	
MDC18	D5	DQC18	
MDC19	D3	DQC19	
MDC20	E6	DQC20	
MDC21	F5	DQC21	
MDC22	F4	DQC22	
MDC23	G5	DQC23	
MDC24	B5	DQC24	
MDC25	A5	DQC25	
MDC26	B4	DQC26	
MDC27	A4	DQC27	
MDC28	A2	DQC28	
MDC29	B1	DQC29	
MDC30	C2	DQC30	
MDC31	C1	DQC31	
MDC32	P2	DQC32	
MDC33	P1	DQC33	
MDC34	R2	DQC34	
MDC35	R1	DQC35	
MDC36	U2	DQC36	
MDC37	U1	DQC37	
MDC38	V2	DQC38	
MDC39	V1	DQC39	
MDC40	U4	DQC40	
MDC41	U3	DQC41	
MDC42	V5	DQC42	
MDC43	V4	DQC43	
MDC44	W3	DQC44	
MDC45	Y5	DQC45	
MDC46	Y4	DQC46	
MDC47	AA5	DQC47	
MDC48	W2	DQC48	
MDC49	W1	DQC49	
MDC50	Y2	DQC50	
MDC51	Y1	DQC51	
MDC52	AB2	DQC52	
MDC53	AB1	DQC53	
MDC54	AC2	DQC54	
MDC55	AC1	DQC55	
MDC56	AA4	DQC56	
MDC57	AA3	DQC57	
MDC58	AB5	DQC58	
MDC59	AB4	DQC59	
MDC60	AC3	DQC60	
MDC61	AD5	DQC61	
MDC62	AD4	DQC62	
MDC63	AE5	DQC63	

R300

MEMORY INTERFACE C

MAC0	N2	MAC0	
MAC1	N5	MAC1	
MAC2	M2	MAC2	
MAC3	M4	MAC3	
MAC4	M3	MAC4	
MAC5	M1	MAC5	
MAC6	N4	MAC6	
MAC7	N1	MAC7	
MAC8	P4	MAC8X	MAC8
MAC9	L3	MAC9X	MAC9
MAC10	L4	MAC10	
MAC11	L5	MAC11	
MAC12	P5	MAC12	
MAC13	P3	MAC13	
MAC14	P6	MAC14	
DQMC#0	H3	DQMC#0	
DQMC#1	F2	DQMC#1	
DQMC#2	E4	DQMC#2	
DQMC#3	B3	DQMC#3	
DQMC#4	T2	DQMC#4	
DQMC#5	V3	DQMC#5	
DQMC#6	AA2	DQMC#6	
DQMC#7	AB3	DQMC#7	→ DQMC#[7..0] (10)
QSC0	J5	QSC0	
QSC1	F1	QSC1	
QSC2	E3	QSC2	
QSC3	A3	QSC3	
QSC4	T1	QSC4	
QSC5	W4	QSC5	
QSC6	AA1	QSC6	
QSC7	AC4	QSC7	→ QSC[7..0] (10)
RASC#	R4	RASC#	→ RASC# (10,11)
CASC#	T4	CASC#	→ CASC# (10,11)
WEC#	T5	WEC#	→ WEC# (10,11)
CSC#	R3	CSC#	→ CSC# (10,11)
CKEC	R5		→ M_CKEC (10,11)
CLKC0	K1		→ M_CLKC0 (10,11)
CLKC0#	J2		→ M_CLKC#0 (10,11)
CLKC1	L2		→ M_CLKC1 (10,11)
CLKC1#	L1		→ M_CLKC#1 (10,11)
DIMC0	J1		
DIMC1	U5		

C304 10pF C305 10pF C306 10pF C307 10pF FOR EMI

(10,11) MAD[14..0]
(10) MDD[63..0]
MAD[14..0]

U42F — Part 6 of 8

MDD0	AJ4	DQD0	
MDD1	AJ3	DQD1	
MDD2	AK5	DQD2	
MDD3	AK4	DQD3	
MDD4	AL3	DQD4	
MDD5	AM5	DQD5	
MDD6	AM4	DQD6	
MDD7	AN5	DQD7	
MDD8	AJ2	DQD8	
MDD9	AJ1	DQD9	
MDD10	AK2	DQD10	
MDD11	AK1	DQD11	
MDD12	AM2	DQD12	
MDD13	AM1	DQD13	
MDD14	AN2	DQD14	
MDD15	AN1	DQD15	
MDD16	AE4	DQD16	
MDD17	AE3	DQD17	
MDD18	AF5	DQD18	
MDD19	AF4	DQD19	
MDD20	AG3	DQD20	
MDD21	AH5	DQD21	
MDD22	AH4	DQD22	
MDD23	AJ5	DQD23	
MDD24	AD2	DQD24	
MDD25	AD1	DQD25	
MDD26	AE2	DQD26	
MDD27	AE1	DQD27	
MDD28	AG2	DQD28	
MDD29	AG1	DQD29	
MDD30	AH2	DQD30	
MDD31	AH1	DQD31	
MDD32	AV5	DQD32	
MDD33	AW5	DQD33	
MDD34	AV6	DQD34	
MDD35	AW6	DQD35	
MDD36	AV8	DQD36	
MDD37	AW8	DQD37	
MDD38	AV9	DQD38	
MDD39	AW9	DQD39	
MDD40	AT7	DQD40	
MDD41	AU7	DQD41	
MDD42	AR8	DQD42	
MDD43	AT8	DQD43	
MDD44	AT9	DQD44	
MDD45	AR10	DQD45	
MDD46	AT10	DQD46	
MDD47	AU10	DQD47	
MDD48	AV10	DQD48	
MDD49	AW10	DQD49	
MDD50	AV11	DQD50	
MDD51	AW11	DQD51	
MDD52	AV13	DQD52	
MDD53	AW13	DQD53	
MDD54	AV14	DQD54	
MDD55	AW14	DQD55	
MDD56	AR11	DQD56	
MDD57	AT11	DQD57	
MDD58	AU11	DQD58	
MDD59	AT12	DQD59	
MDD60	AT13	DQD60	
MDD61	AR14	DQD61	
MDD62	AT14	DQD62	
MDD63	AU14	DQD63	

R300

MEMORY INTERFACE D

MAD0	AT3	MAD0	
MAD1	AT6	MAD1	
MAD2	AR4	MAD2	
MAD3	AP3	MAD3	
MAD4	AR6	MAD4	
MAD5	AR3	MAD5	
MAD6	AT5	MAD6	
MAD7	AU5	MAD7	
MAD8	AU2	MAD8X	MAD8
MAD9	AP4	MAD9X	MAD9
MAD10	AN3	MAD10	
MAD11	AN4	MAD11	
MAD12	AU4	MAD12	
MAD13	AU1	MAD13	
MAD14	AV4	MAD14	
DQMD#0	AK3	DQMD#0	
DQMD#1	AL2	DQMD#1	
DQMD#2	AF3	DQMD#2	
DQMD#3	AF2	DQMD#3	
DQMD#4	AV7	DQMD#4	
DQMD#5	AU8	DQMD#5	
DQMD#6	AV12	DQMD#6	
DQMD#7	AU12	DQMD#7	→ DQMD#[7..0] (10)
QSD0	AL4	QSD0	
QSD1	AL1	QSD1	
QSD2	AG4	QSD2	
QSD3	AF1	QSD3	
QSD4	AW7	QSD4	
QSD5	AR9	QSD5	
QSD6	AW12	QSD6	
QSD7	AR13	QSD7	→ QSD[7..0] (10)
RASD#	AW4	RASD#	→ RASD# (10,11)
CASD#	AW2	CASD#	→ CASD# (10,11)
WED#	AW3	WED#	→ WED# (10,11)
CSD#	AV3	CSD#	→ CSD# (10,11)
CKED	AV1		→ M_CKED (10,11)
CLKD0	AR1		→ M_CLKD0 (10,11)
CLKD0#	AP2		→ M_CLKD#0 (10,11)
CLKD1	AT2		→ M_CLKD1 (10,11)
CLKD1#	AT1		→ M_CLKD#1 (10,11)
VREF1	AC6		
DIMD0	AP1		
DIMD1	AR7		
MEMVMODE0	E7	MEMMODE0	
MEMVMODE1	F7	MEMMODE1	
MEMTEST	F24		

+MVDDQ
C308 10pF C309 10pF C310 10pF C311 10pF FOR EMI
R773 75.0R
C150 10uF 16V C151 100nF
R774 75.0R
R166 47R

MEMMODE0 R164 4.7K → +VDDC_CT
MEMMODE1 R165 4.7K DNI
R167 4.7K
R168 4.7K DNI

+MVDDQ C894 0.1uF
+MVDDQ C895 0.1uF
+VDDC_CT C896 0.1uF
+VDDC_CT C897 0.1uF
+VDDC_CT C898 0.1uF

MEMVMODE[1:0]	MEMORY IO VOLTAGE
0 1	2.5V (DDR)
1 0	1.8V (DDR)
1 1	3.3V (SDR)

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Size	Document Number	Rev
B	MEMORY CHANNELS C and D	0A

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Vtt TERMINATION for DDR

Differential CLOCK termination

Differential termination should be placed close to the memory.

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B	VTT TERMINATION C and D	0A
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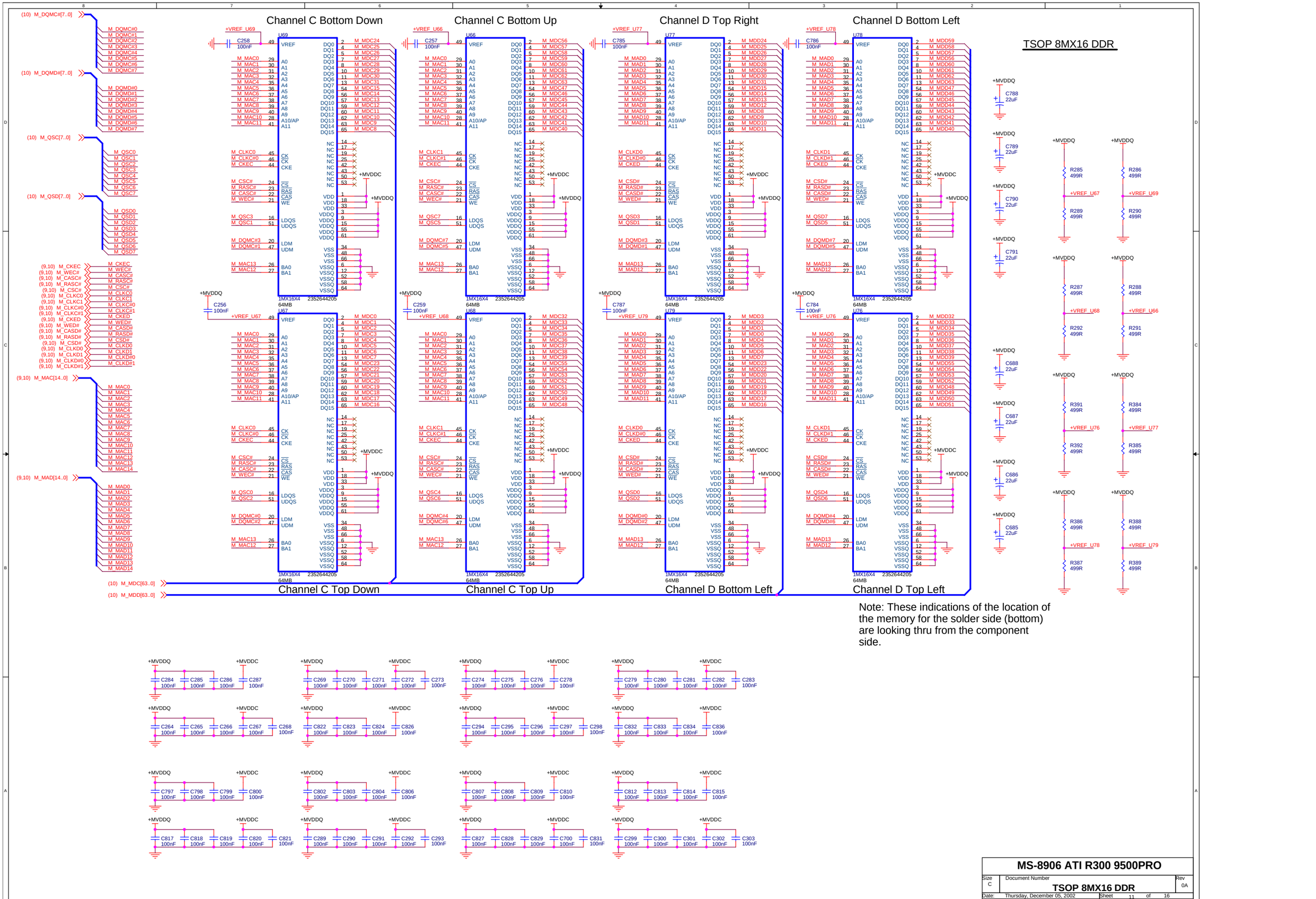
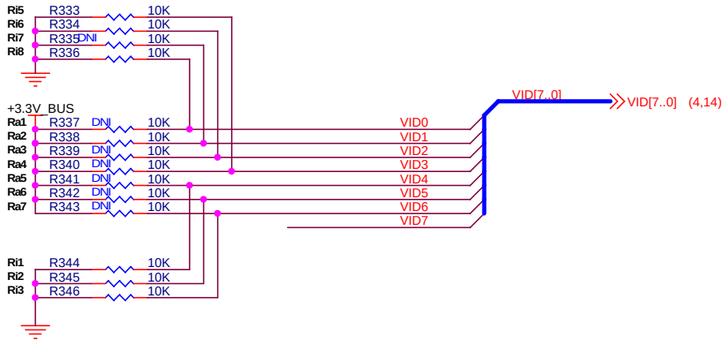
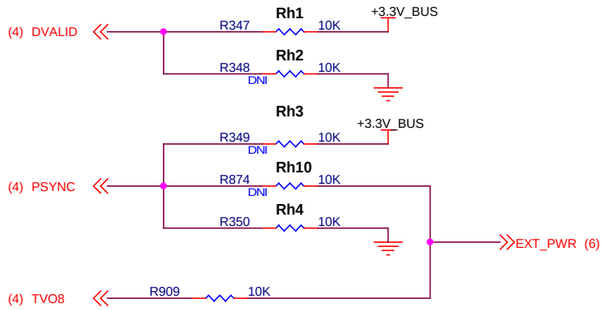
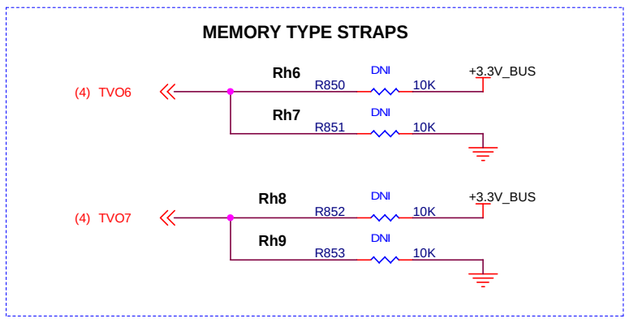
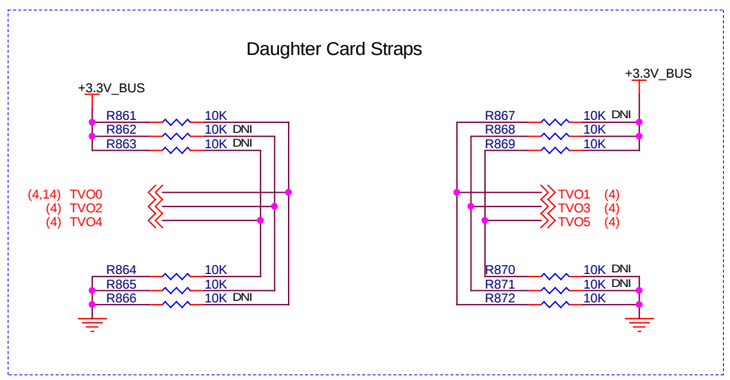


STRAPPING









AGPFBSKEW – VID(1:0)

Ra2	Ra1	Ri7	Ri8	
DNI	DNI	10K	10K	refclk slightly earlier than feedback (00)
DNI	10K	10K	DNI	refclk 1 tap earlier than feedback (01)
10K	DNI	DNI	10K	refclk 1 tap later than feedback DEFAULT (10)
10K	10K	DNI	DNI	refclk 2 taps earlier than feedback (11)

X0CLK_SKEW –VID(3:2)

Ra4	Ra3	Ri5	Ri6	
DNI	DNI	10K	10K	x0clk to agpclk 0 tap delay DEFAULT
DNI	10K	10K	DNI	x0clk to agpclk 1 tap delay
10K	DNI	DNI	10K	x0clk to agpclk 2 taps delay
10K	10K	DNI	DNI	x0clk to agpclk 3 taps delay

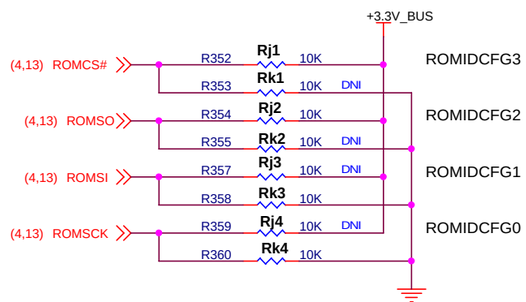
INSTALL	DEVICE ID
Rh1	NORMAL ID (default) Install it all the time when it is normal device ID
Rh2	Use workstation DEVICE_ID when WSEN = 1

INSTALL	DNI	ID_DISABLE
Rh4	**Rh10**	Normal operation
Rh3	**Rh10**	CHIP SHUTS DOWN
Ⓒ **Rh10**	**Rh3 Rh4**	Circuitry for external power detection. (DEFAULT)

INSTALL	VIP DEVICE
Rh5	NO SLAVE VIP (DEFAULT) Install it when internal pull-up doesn't work
	SLAVE VIP – VIP device will drive low when VIP is attached.

MEMORY TYPE STRAPS

MEMORY TYPE	Rh6	Rh7	Rh8	Rh9
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD



BUSCFG -- VID(6:4)

BUSTYPE_2 VID6		**BUSTYPE_1** VID5		**BUSTYPE_0** VID4		
Ra7	Ri3	Ra6	Ri2	Ra5	Ri1	AGP8X_DET = 0 (both GC and MB 8x capable) DESCRIPTION
DNI	10K	DNI	10K	DNI	10K	AGP 8X, 0.8V signaling PLL CLK, IDSEL = AD16
DNI	10K	DNI	10K	10K	DNI	AGP 8X, 0.8V signaling PLL CLK, IDSEL = AD17
DNI	10K	10K	DNI	DNI	10K	AGP 4X, 0.8V signaling PLL CLK, IDSEL = AD16
DNI	10K	10K	DNI	10K	DNI	AGP 4X, 0.8V signaling PLL CLK, IDSEL = AD17
						AGP8X_DET = 1 (either GC or MB not 8x capable)
DNI	10K	DNI	10K	DNI	10K	AGP 4X, PLL CLK, IDSEL = AD16
DNI	10K	DNI	10K	10K	DNI	AGP 4X, PLL CLK, IDSEL = AD17
DNI	10K	10K	DNI	DNI	10K	AGP 1X/2X, PLL CLK, IDSEL = AD16
DNI	10K	10K	DNI	10K	DNI	AGP 1X/2X, PLL CLK, IDSEL = AD17
10K	DNI	DNI	10K	DNI	10K	PCI 66MHz, PLL CLK
10K	DNI	DNI	10K	10K	DNI	PCI 33MHz, 3.3V, REF CLK
10K	DNI	10K	DNI	DNI	10K	AGP 1X, REF CLK, IDSEL = AD16
10K	DNI	10K	DNI	10K	DNI	AGP 1X, REF CLK, IDSEL = AD17

Rj1	Rk1	Rj2	Rk2	Rj3	Rk3	Rj4	Rk4	ROMIDCFG[3:0]
DNI	10K	DNI	10K	DNI	10K	DNI	10K	No ROM, CHG ID = 00
DNI	10K	DNI	10K	10K	DNI	DNI	10K	No ROM, CHG ID = 01
DNI	10K	10K	DNI	DNI	10K	DNI	10K	No ROM, CHG ID = 10
DNI	10K	10K	DNI	10K	DNI	DNI	10K	No ROM, CHG ID = 11
10K	DNI	DNI	10K	DNI	10K	DNI	10K	Parallel ROM on TVO (default)
10K	DNI	DNI	10K	DNI	10K	10K	DNI	Serial AT25F1024, ID's from ROM
10K	DNI	DNI	10K	10K	DNI	DNI	10K	Serial AT45DB011, ID's from ROM
10K	DNI	DNI	10K	10K	DNI	10K	DNI	Serial ST M25P10, ID's from ROM
10K	DNI	10K	DNI	DNI	10K	DNI	10K	Serial ST M25P05, ID's from ROM
10K	DNI	10K	DNI	DNI	10K	10K	DNI	Serial SST45LF010, ID's from ROM
10K	DNI	10K	DNI	10K	DNI	DNI	10K	Parallel ROM on DVO
10K	DNI	10K	DNI	10K	DNI	10K	DNI	Serial ISSI NX25F011B, ID's from ROM

TVO1	
0	PAL
1	NTSC

TVO2	
0	YPrPb
1	NTSC

TVO4	
0	NO
1	YES

TVO0	TVO3	DAC2
0	0	OFF
0	1	TV-OUT
1	0	CRT
1	1	BOTH

TVO5	
0	NO VIDEO CAPATURE
1	RAGE THEATER 1 OR 2

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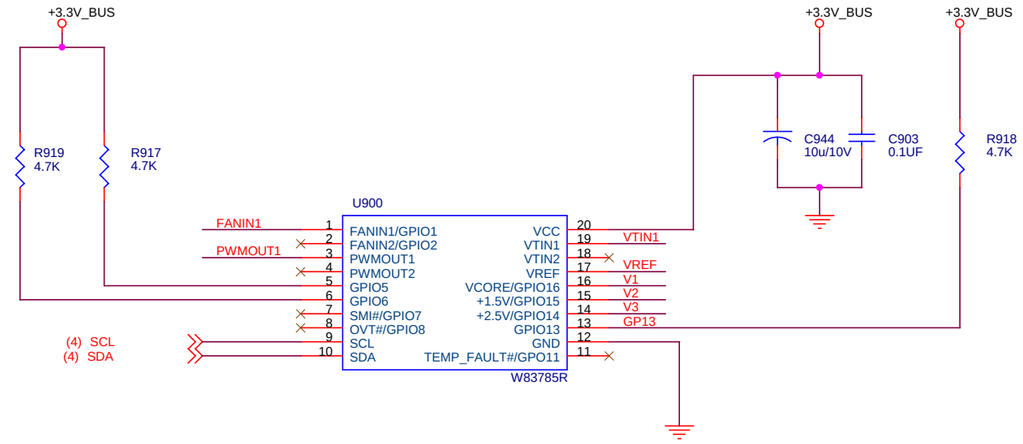
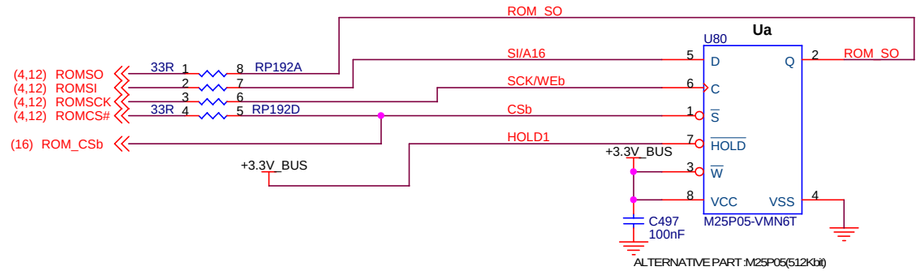
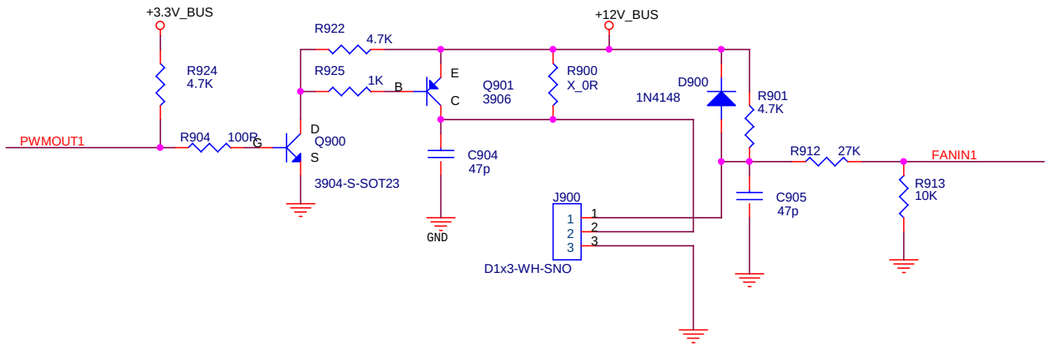
HARDWARE MONITOR



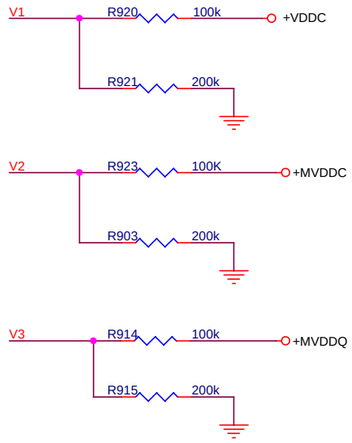
SERIAL EEPROM 512K/1M

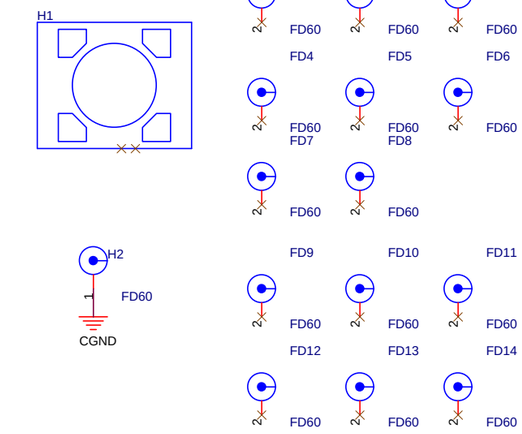


FAN SPEED CONTROL

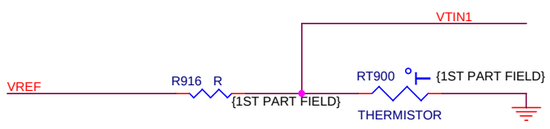


VOLTAGE SENSORING CIRCUIT

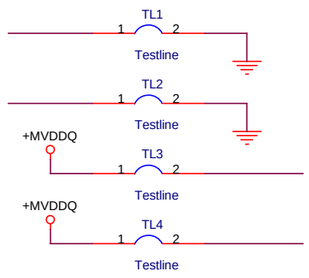




TEMPERATURE SENSORING CIRCUIT



Impendence Test Line



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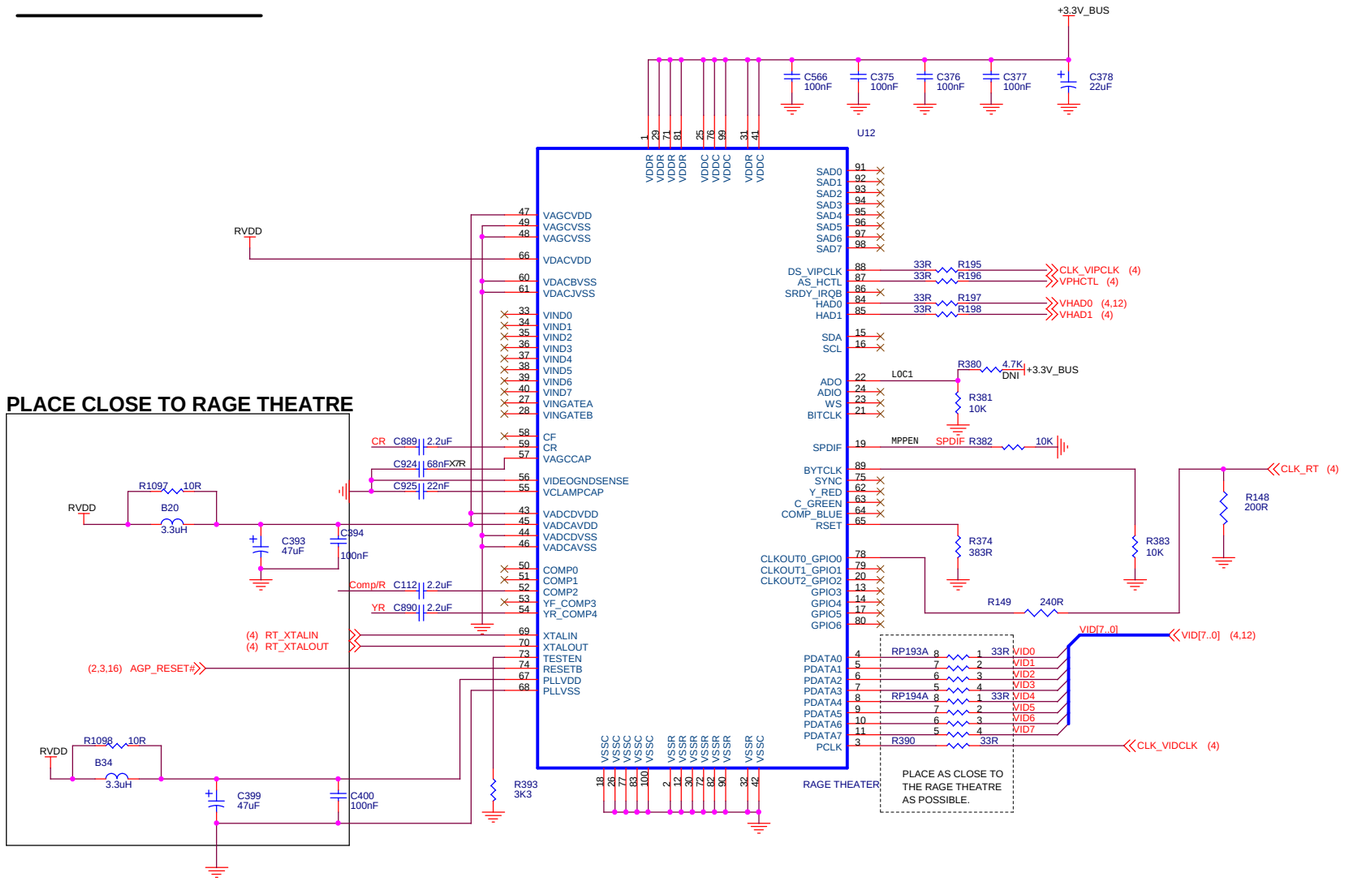
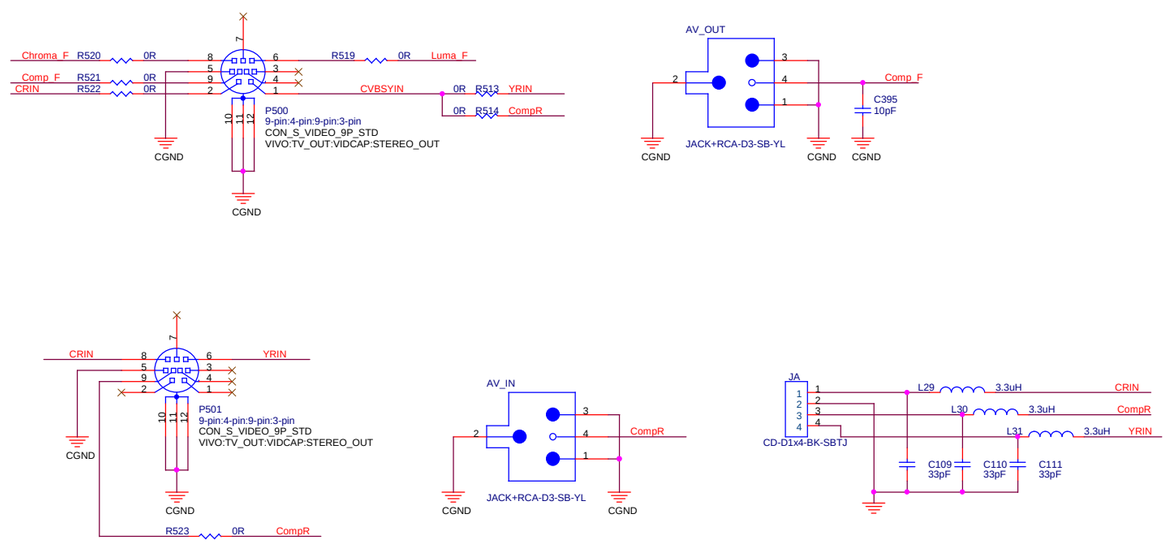
THEATER & TV-OUT

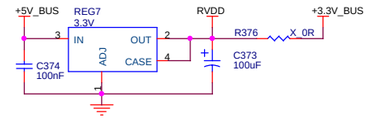
PLACE CLOSE TO RAGE THEATRE



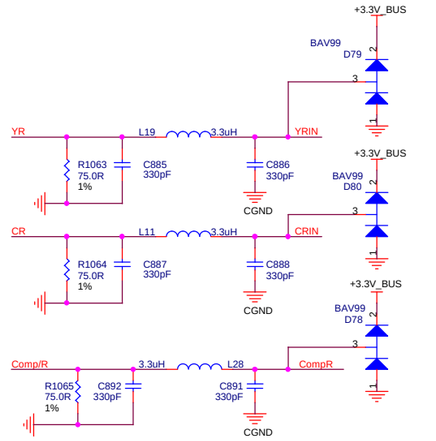
VIVO Connector



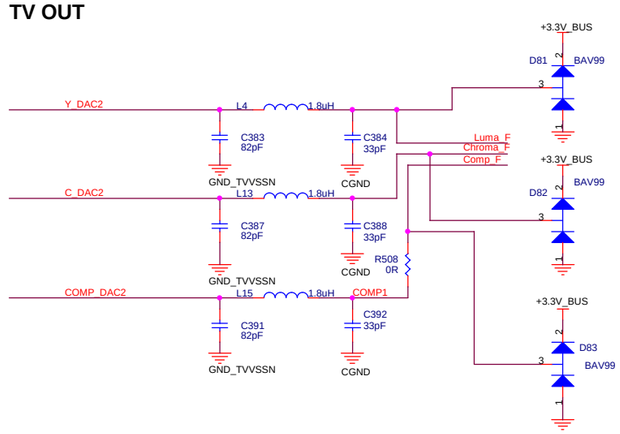
Regulator for RVDD



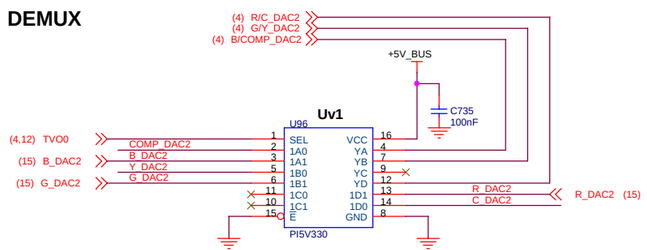
VIDEO IN



TV OUT



DEMUX



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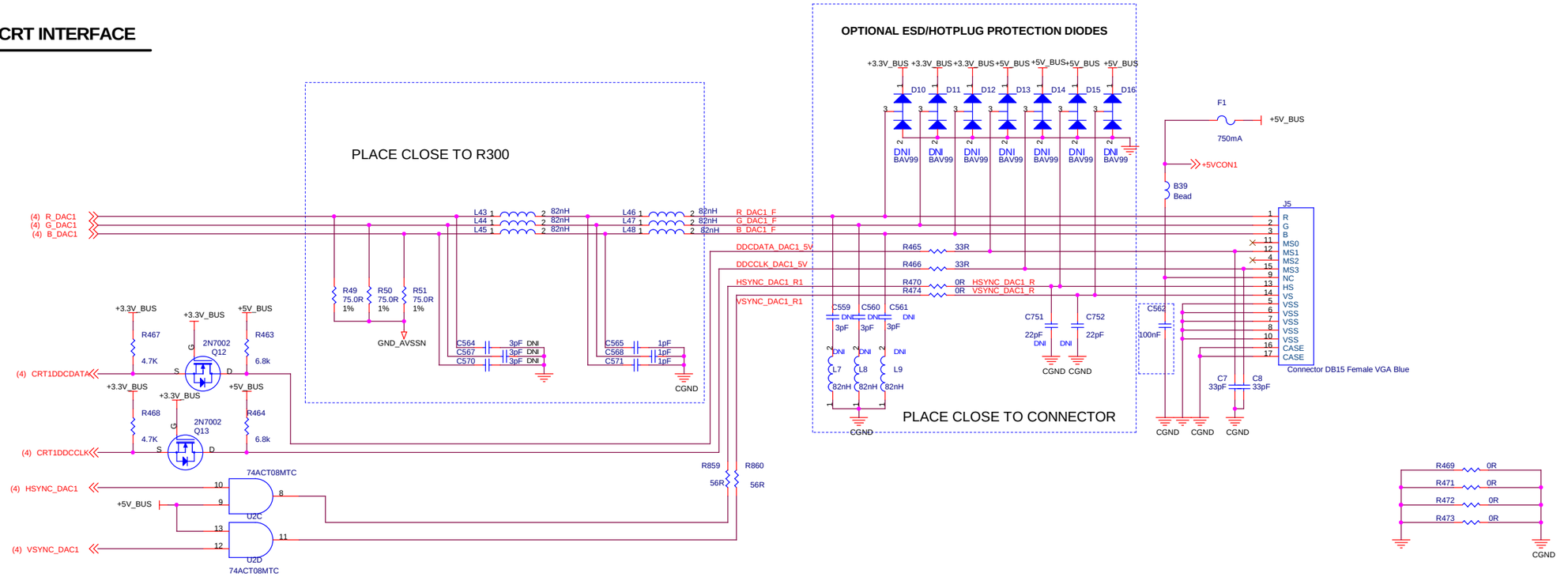
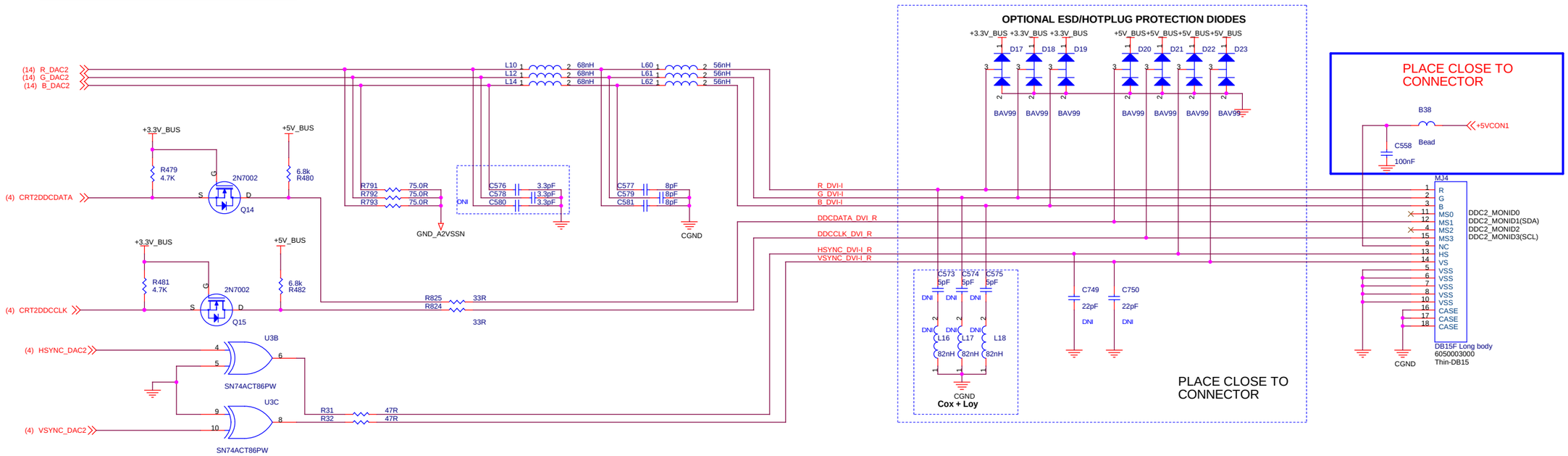
PRIMARY CRT INTERFACE



SECONDARY CRT INTERFACE



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Hijack Circuit

(3) 8X_DET#

MU106
TK11819M
IN- 1 Vin
2 OSC
IN+ 3 DK
T1 6
GND 5 DEVSEL_TTL
Vout 4
USED FOR THE FOOTPRINT
+5V_BUS

+5V_BUS
C753
100nF
U3A
SN74ACT86PW
R943 0R
R1552
10K
DNI

DEVSEL_TTL
+5V_BUS
C761
100nF
U106
LMV7219M
R1547
100K
DNI
(2,3) AGP_VREFGC
R1550 4.99K
IN+
(2,3) AGP_DEVSEL#_R
R1548 1.0K
IN-
R1551
100K
DNI
+5V_BUS
U107
VDD VCC
OUT IN+
GND IN-
LATCH VEE
MAX9203EKA-T
C760
100nF
Block_DEVSEL#

Place closest possible to AGP connector with minimum possible stub on AGP_DEVSEL#_R signal.

HighSpeed Comparator

+5V_BUS
C759
100nF
(13) ROM_CSb
U99A
SN74HCT02PWR
R952
0R
C1126
100nF
DNI

+5V_BUS
C757
100nF
U103A
74VHCT74MTC
R951
0R
U103B
74VHCT74MTC

Block_DEVSEL#
R947
0R
U99D
SN74HCT02PWR
SWAP

(2,3,14) AGP_RESET#

(2,3) AGP_AGPCLK
Minimum possible stub on this signal.
R946
270R
U99B
SN74HCT02PWR
U99C
SN74HCT02PWR

MK1
SELECT NO
V+ COM
GND NC
NLAS4599DF
+5V_BUS
K1
MAX4625EUT-T
SWAP
C755
100nF
K2
MAX4625EUT-T
C756
100nF
MK2
SELECT NO
V+ COM
GND NC
NLAS4599DF

Place closest possible to AGP connector with absolute minimum possible trace lengths and vias.

AGP_TRDY#_R (2)
AGP_TRDY# (2,3)
AGP_STOP#_R (2)
AGP_STOP# (2,3)

AGP CONNECTOR SIDE

R300 SIDE

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