P162, NV34, 4Mx16/8Mx16/16Mx16DDR, 64/128MBMB, Video OUT, VGA

Page Overview

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2 AGP Interface

3 NV34 Frame Buffer

4 Frame Buffer 0..31

5 Frame Buffer 32..63

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8 DAC A,B, DAC B MUX, PLL, Video OUT

9 DAC A,B RGB filter

10 Power Supply A3V3, FBVDD/FBVDDQ, Mechanicals.

11 BIOS and Strapping

12 DVO,GPIOs and Xtal.

13 TMDS LinkA and its power supplies, Backdrive.

14 NVVDD SW.

15 Current Supplement and Fan control.

16 Net Rules.

P160 HISTORY:

X00	INITIAL VERSION
X01	Cleaned up schematics - changes from initial design review meeting
X02	Imported board file #65 and synchronized with latest version of schematics.
X03	Nov 18/02 - Replaced LB502 with an 805 bead, changed PLLVDD rail to 3V3 instead of A3V3, and removed AGPVDDQ deoupling caps C130, C257, and C570.
X04	Nov 21/02 - C75 is changed to decouple 3V3 to GND.
X05	Nov 22/02 - VIP interface rail changed to 3V3 instead of A3V3 due to short between VIPVDDQ and VDD33.
X06	Nov 25/02 - FRWR_VAUXP rail changed to 3V3.
X07	Nov 26/02 - Changed DACB_LOAD_TEST GPIO assignment for NV34.
X08	Dec 02/02 - AGP_PLL_VDD and FB_DLLVDD are supplied from A3V3 rail.

P162-A00 History:

1-Added P162 specific features:

- SW PS,TMDS LinkA, Backdrive, new slim VGA, Fan Cntl.
- Added Current sharing, TMDS IO and PLL linear regulators.

2-Added TH parts in PS section as ALT.
3-Added SST serial support.
4-Changed AGP_PLL_VDD, FB_PLLVDD, DAC_A/B_VDD and PLL_VDD to A3V3.
5-Added 10 caps as part of P160 sync up.
6-Added PU resitors on Jtag TMS and TDI
7-Incorporated recommendations from PS Vendor.
8-Added extra X elements near connectors to bridge CGND and GND cut.
9-Added an option to use a single dual FET for low end bd.
10-Fixed error on 6529 power good and current supplement.
11-Changed C302 to 0603 (too big pkg for .1uf in 0805)
12-Deleted C296 and C293 (shared them with C313, C324)
13-Changed C329 and C324 to 0603 pkg.
14-Removed alternate Semtech SW (could not route).

Changes after the design review:

1-Remove C301 and R137-left over from Semtech PS circuit.
2-Remove sync buffer bypass resistors.
3-Remove R122 and R123 from Intersil power rails.
4-Add snubber circuit for NVVDD PS.
5-Add PD res on TP_XTALOUTBUF to terminate the signal.
6-Fan controler PU to 3V3 from A3V3.
7-Cleaned up Unnamed nets.

8-Split CGND into 2 nets (added CGND1 to J6.25 and J2. 16).
9-Added PD resistor on FAN_ON.
10-Added 8 caps for DQS/DQM routings that break plane reference.

X-RELEASE.

P162-A01 History:

Merged net IFPBIOVDD with IFPAIOVDD.
Merged Q4 and Q5 into one package.
Implemented TV signal return scheme thru zero Ohm resistors.

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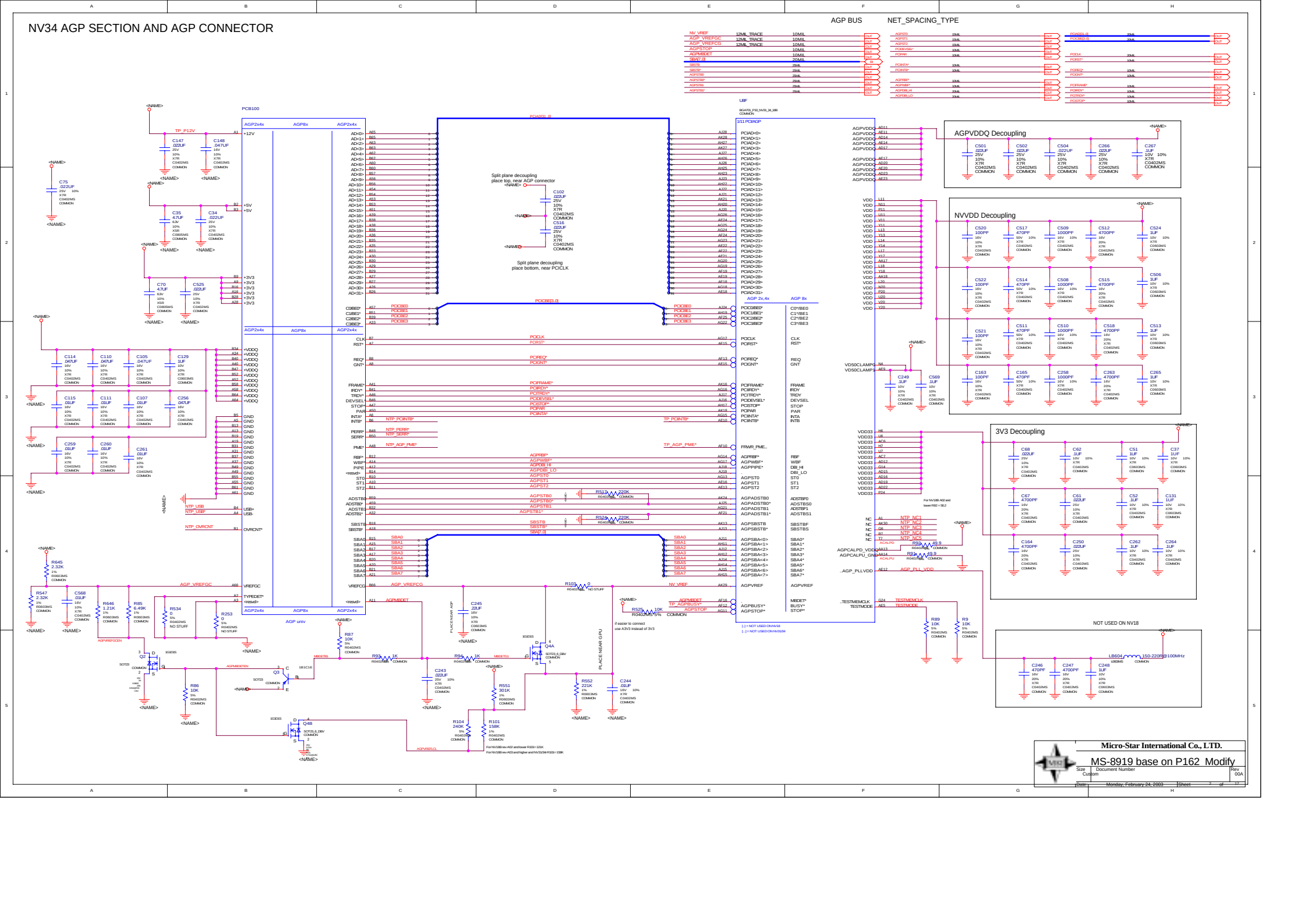
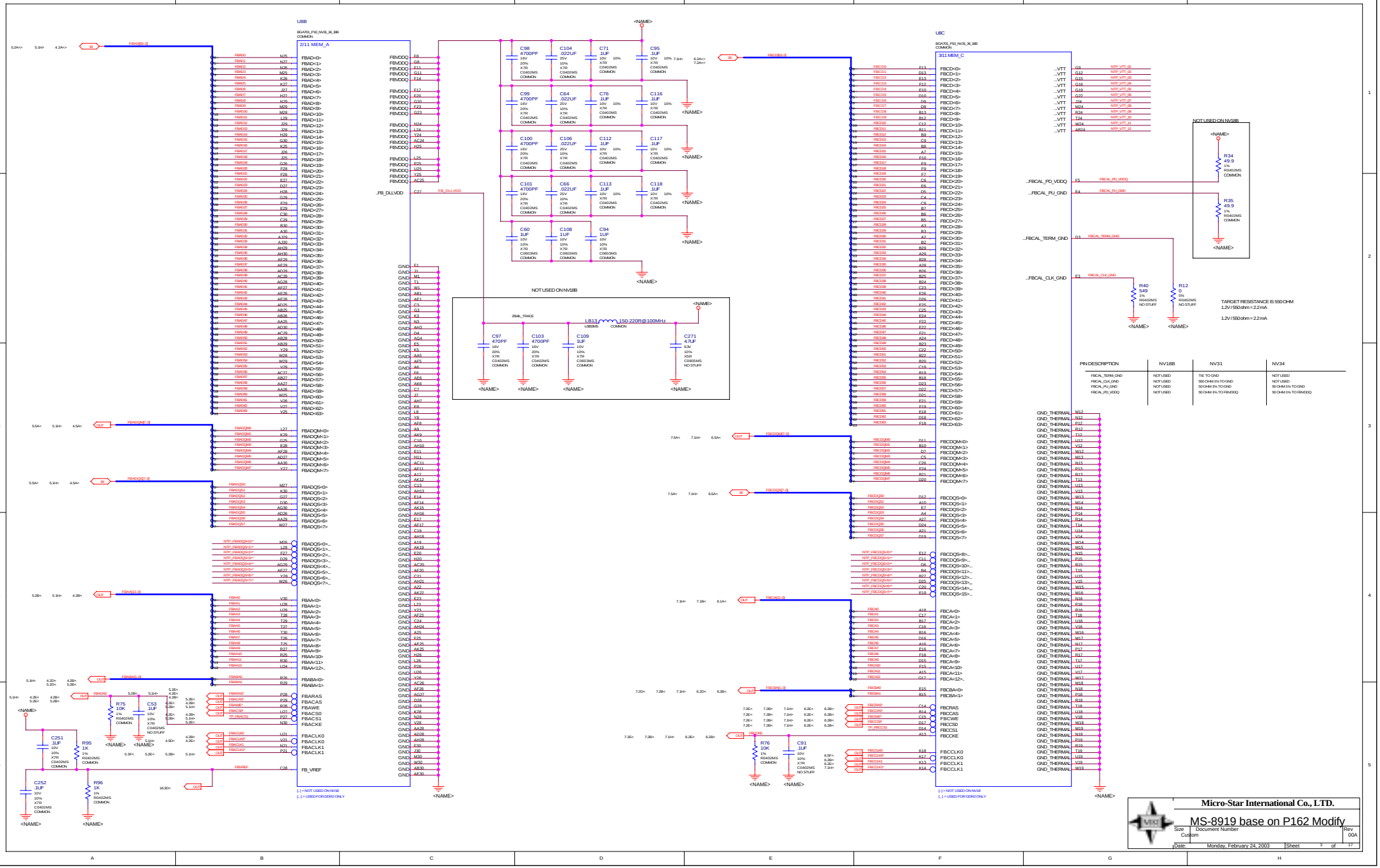
NV34 AGP SECTION AND AGP CONNECTOR




U8B
2/11 MEM_A
U8C
3/11 MEM_C
NOT USED ON NV18B
PIN DESCRIPTION
NV18B
NV31
NV34
TARGET RESISTANCE IS 550 OHM
1.2V / 550 ohm = 2.2 mA
1.2V / 550 ohm = 2.2 mA
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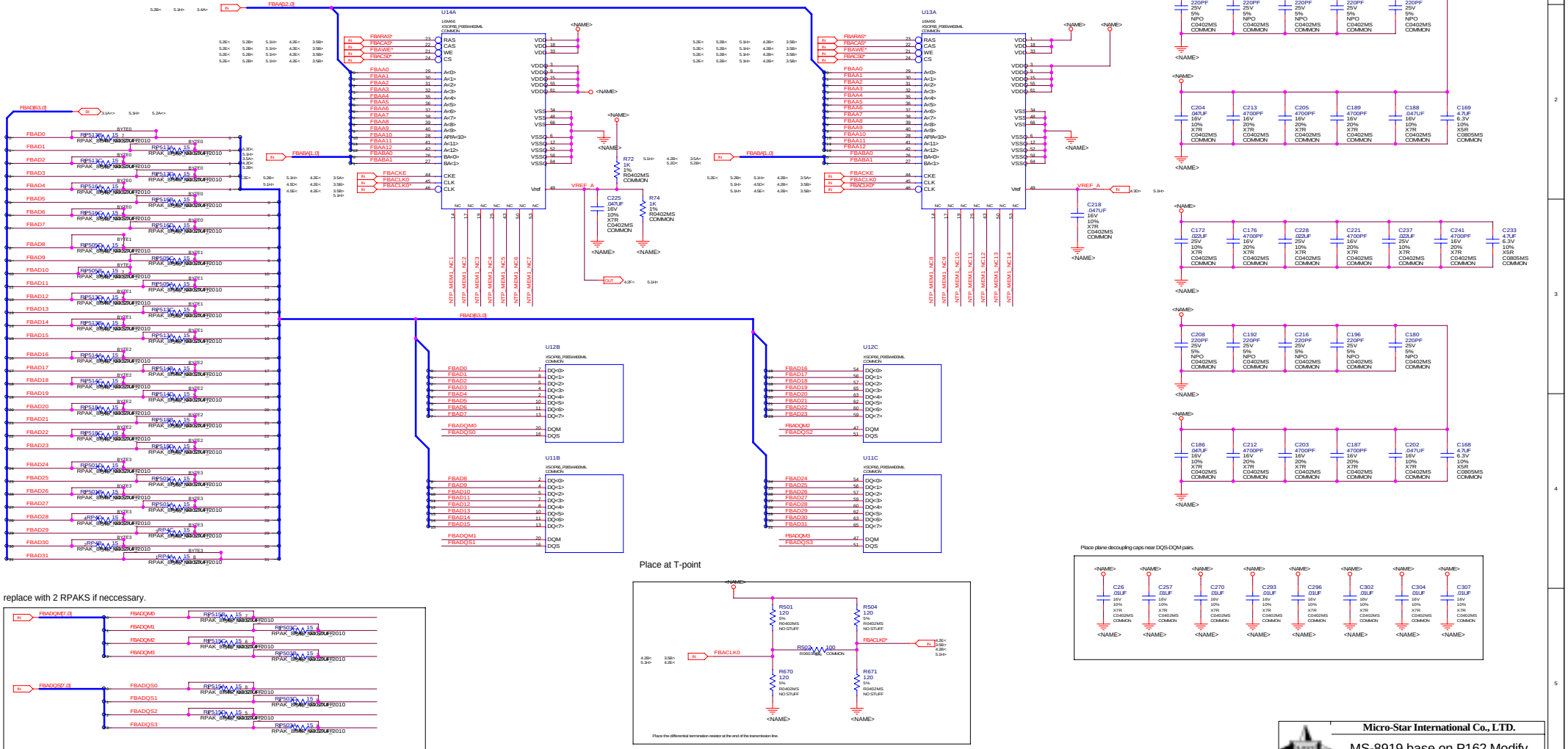
MEMORY 1st bank 0..31
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

NV31 FB i/f can be configured in two ways:
2x64 bits or 2x32 bits

THIS REQUIRES THAT BOTH PARTITIONS

TO BE CONNECTED TO BE FUNCTIONAL



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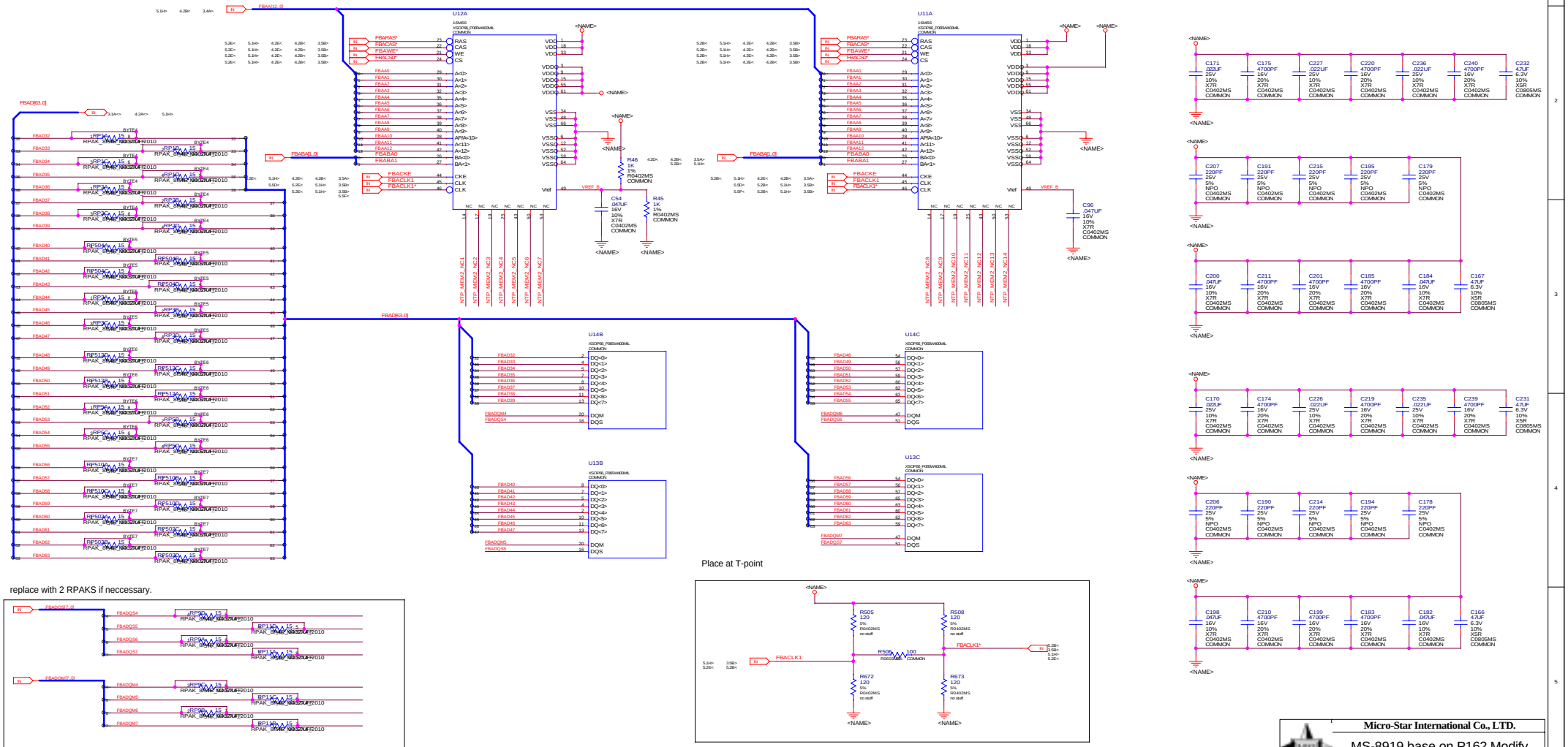
MEMORY 1st bank 32..63
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



replace with 2 RPAKS if neccessary.

Place at T-point

NET_PHYSICAL_TYPE	NET_SPACING_TYPE	Diffpair
FBACLK0	20MIL G2G 30MIL	FBACLK0
FBACLK0*	20MIL G2G 30MIL	FBACLK0
FBACLK1	20MIL G2G 30MIL	FBACLK1
FBACLK1*	20MIL G2G 30MIL	FBACLK1
FBAD[63:0]	10MIL	
FBADQM7..0]	10MIL	
FBADQS7..0]	15MIL	
FBAA[12..0]	10MIL	
FBARAS*	10MIL	
FBACAS*	10MIL	
FBAWE*	10MIL	
FBACS0*	10MIL	
FBABA[1..0]	10MIL	
FBACKE	10MIL	
VREF_A	12MIL TRACE	10MIL
VREF_B	12MIL TRACE	10MIL

C171 .022UF 25V 10% X7R C0402MS COMMON	C175 4700PF 16V 20% X7R C0402MS COMMON	C227 .022UF 25V 10% X7R C0402MS COMMON	C220 4700PF 16V 20% X7R C0402MS COMMON	C236 .022UF 25V 10% X7R C0402MS COMMON	C240 4700PF 16V 20% X7R C0402MS COMMON	C232 4.7UF 6.3V 10% X5R C0805MS COMMON
C207 220PF 25V 5% NPO C0402MS COMMON	C191 220PF 25V 5% NPO C0402MS COMMON	C215 220PF 25V 5% NPO C0402MS COMMON	C195 220PF 25V 5% NPO C0402MS COMMON	C179 220PF 25V 5% NPO C0402MS COMMON		
C200 .047UF 16V 10% X7R C0402MS COMMON	C211 4700PF 16V 20% X7R C0402MS COMMON	C201 4700PF 16V 20% X7R C0402MS COMMON	C185 4700PF 16V 20% X7R C0402MS COMMON	C184 .047UF 16V 10% X7R C0402MS COMMON	C167 4.7UF 6.3V 10% X5R C0805MS COMMON	
C170 .022UF 25V 10% X7R C0402MS COMMON	C174 4700PF 16V 20% X7R C0402MS COMMON	C226 .022UF 25V 10% X7R C0402MS COMMON	C219 4700PF 16V 20% X7R C0402MS COMMON	C235 .022UF 25V 10% X7R C0402MS COMMON	C239 4700PF 16V 20% X7R C0402MS COMMON	C231 4.7UF 6.3V 10% X5R C0805MS COMMON
C206 220PF 25V 5% NPO C0402MS COMMON	C190 220PF 25V 5% NPO C0402MS COMMON	C214 220PF 25V 5% NPO C0402MS COMMON	C194 220PF 25V 5% NPO C0402MS COMMON	C178 220PF 25V 5% NPO C0402MS COMMON		
C198 .047UF 16V 10% X7R C0402MS COMMON	C210 4700PF 16V 20% X7R C0402MS COMMON	C199 4700PF 16V 20% X7R C0402MS COMMON	C183 4700PF 16V 20% X7R C0402MS COMMON	C182 .047UF 16V 10% X7R C0402MS COMMON	C166 4.7UF 6.3V 10% X5R C0805MS COMMON	

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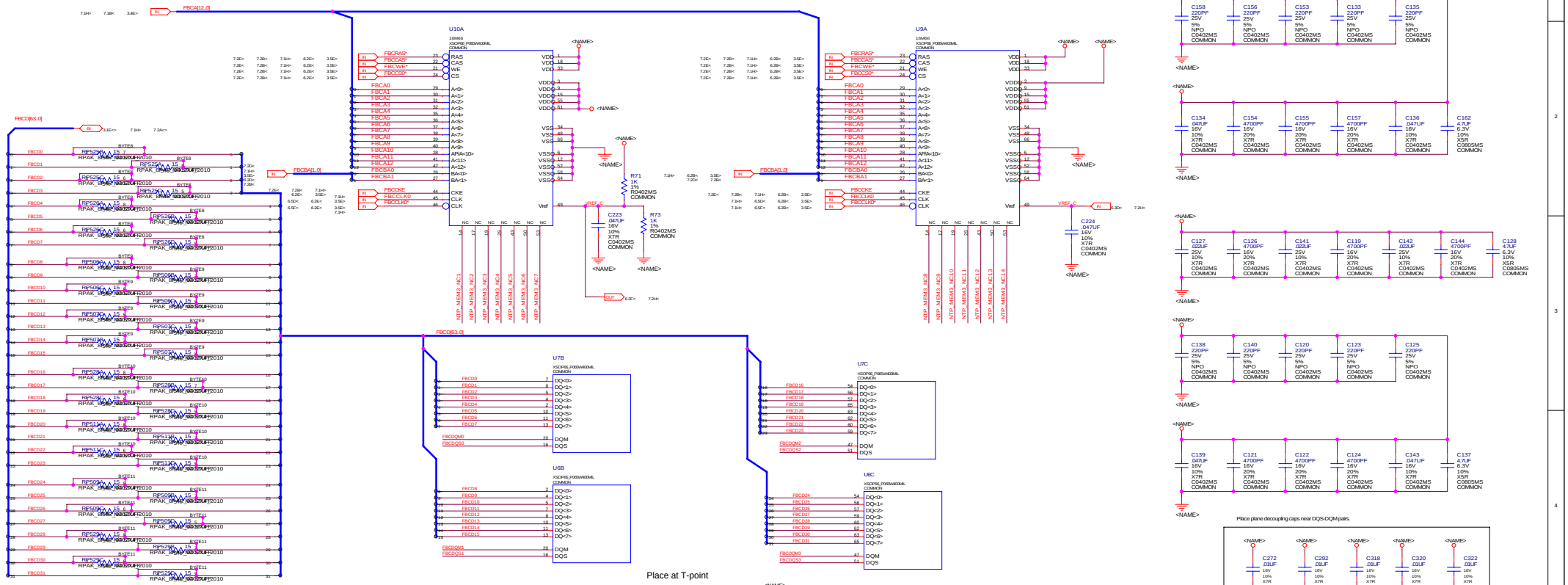
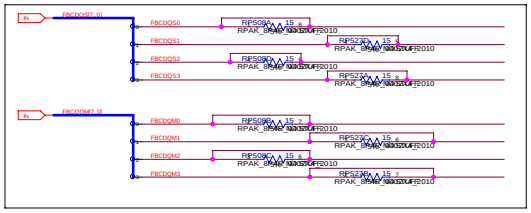
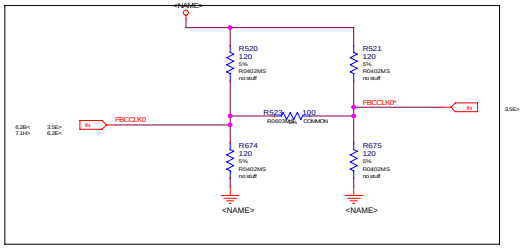
MEMORY 2nd bank 0..31
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



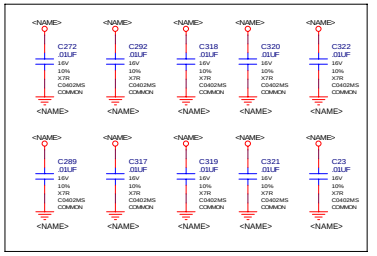
replace with 2 RPAKS if neccessary.



Place at T-point



Place plane decoupling caps near DQS-DQM pairs.



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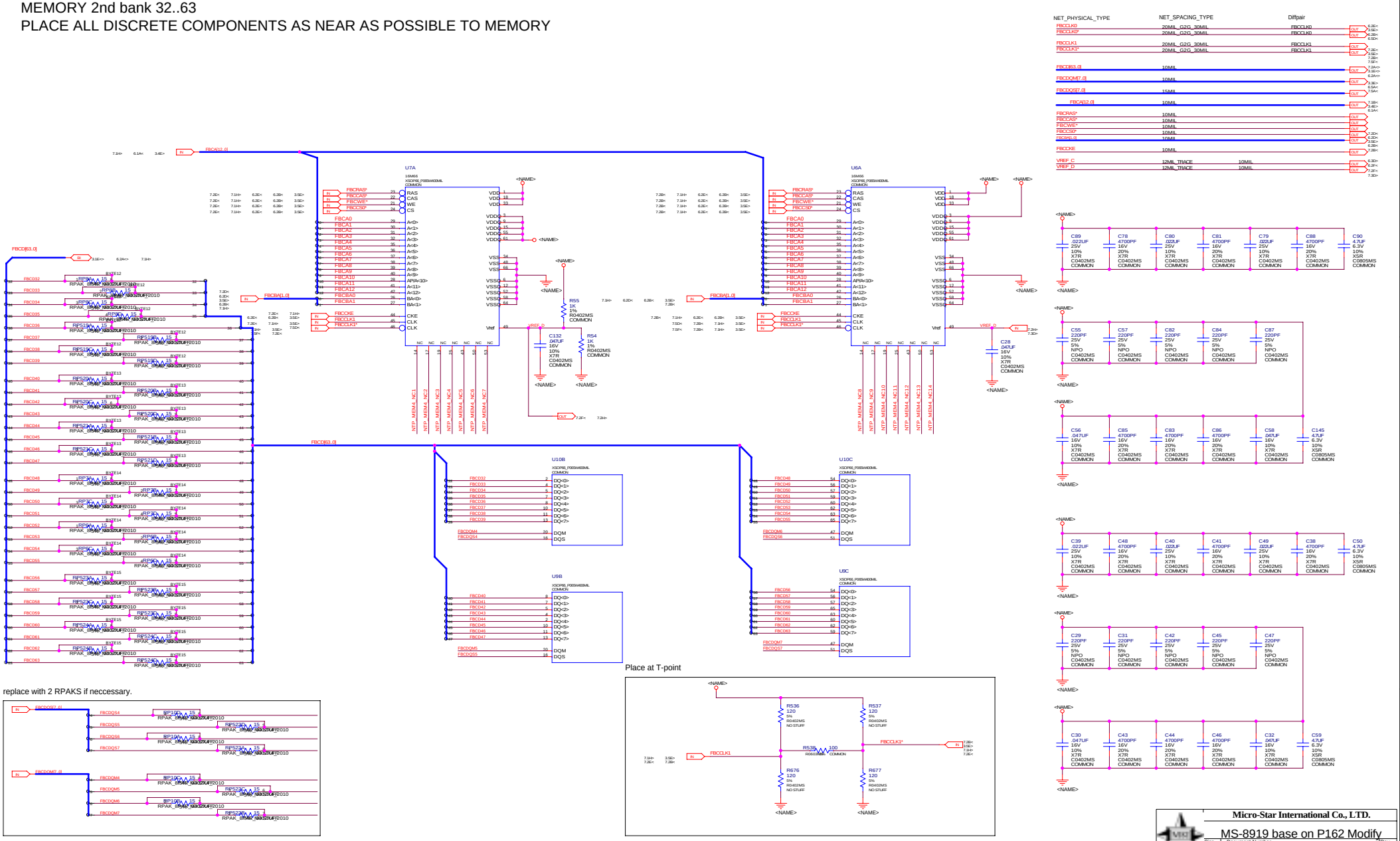
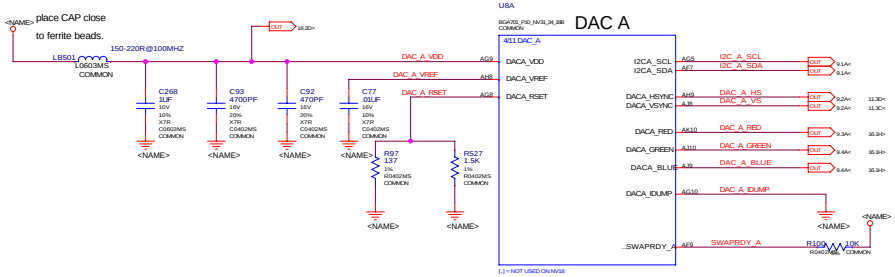
MEMORY 2nd bank 32..63
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

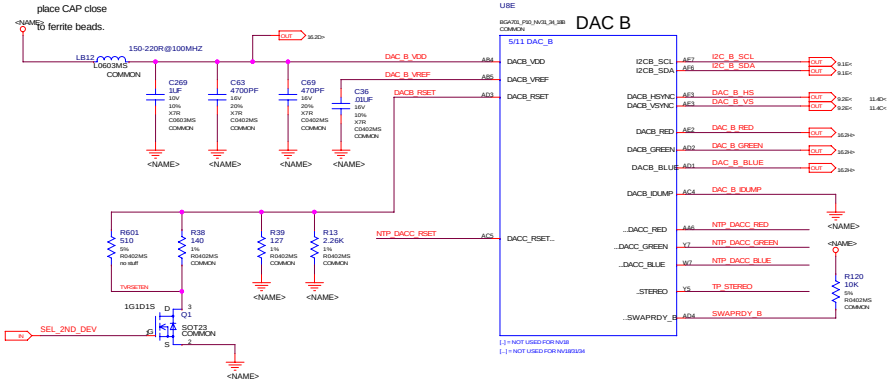


replace with 2 RPAKS if neccessary.

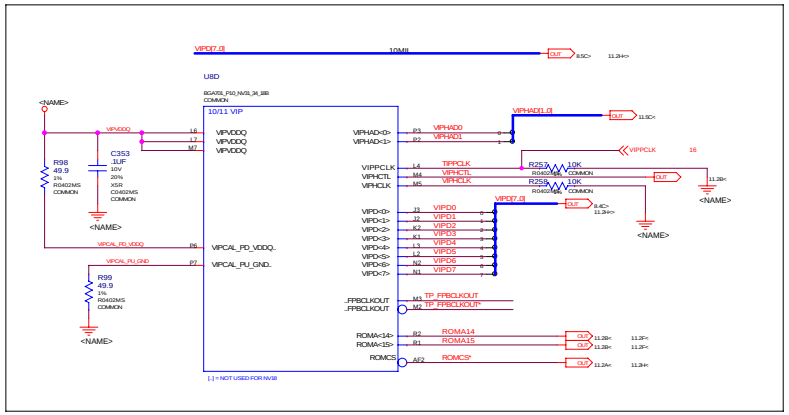
DAC A



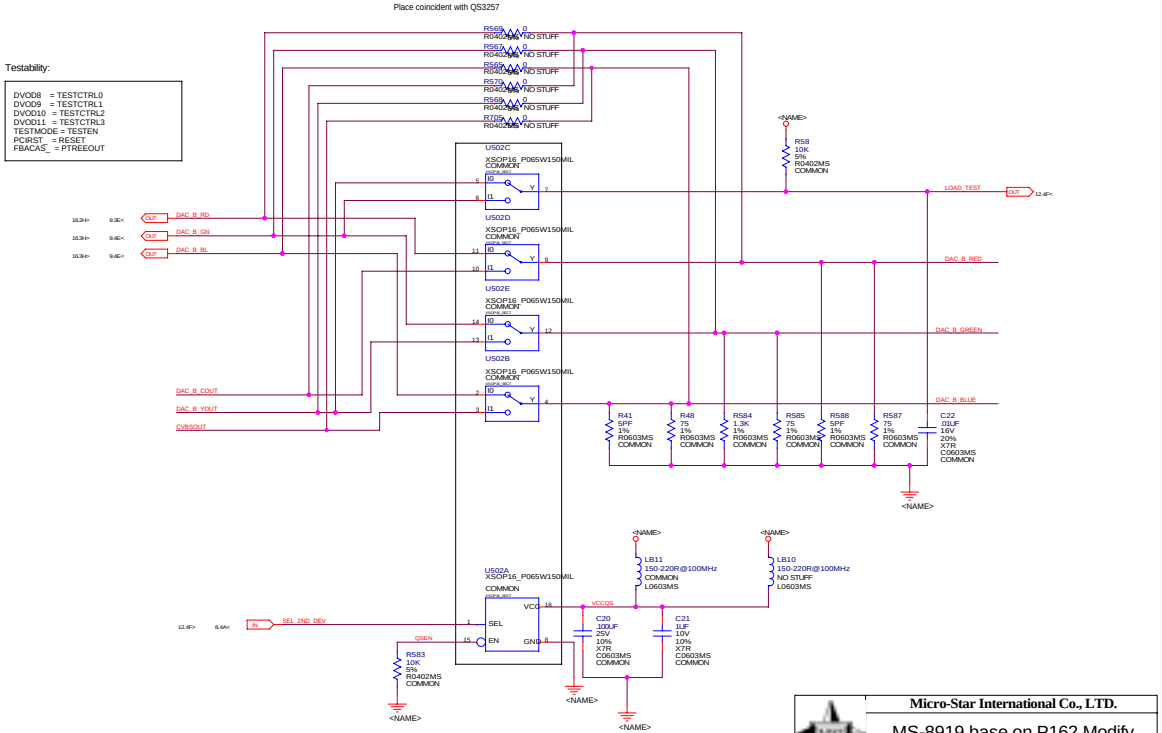
DAC B



VIP



DACB SWITCH BETWEEN VGA OUT AND TV OUT



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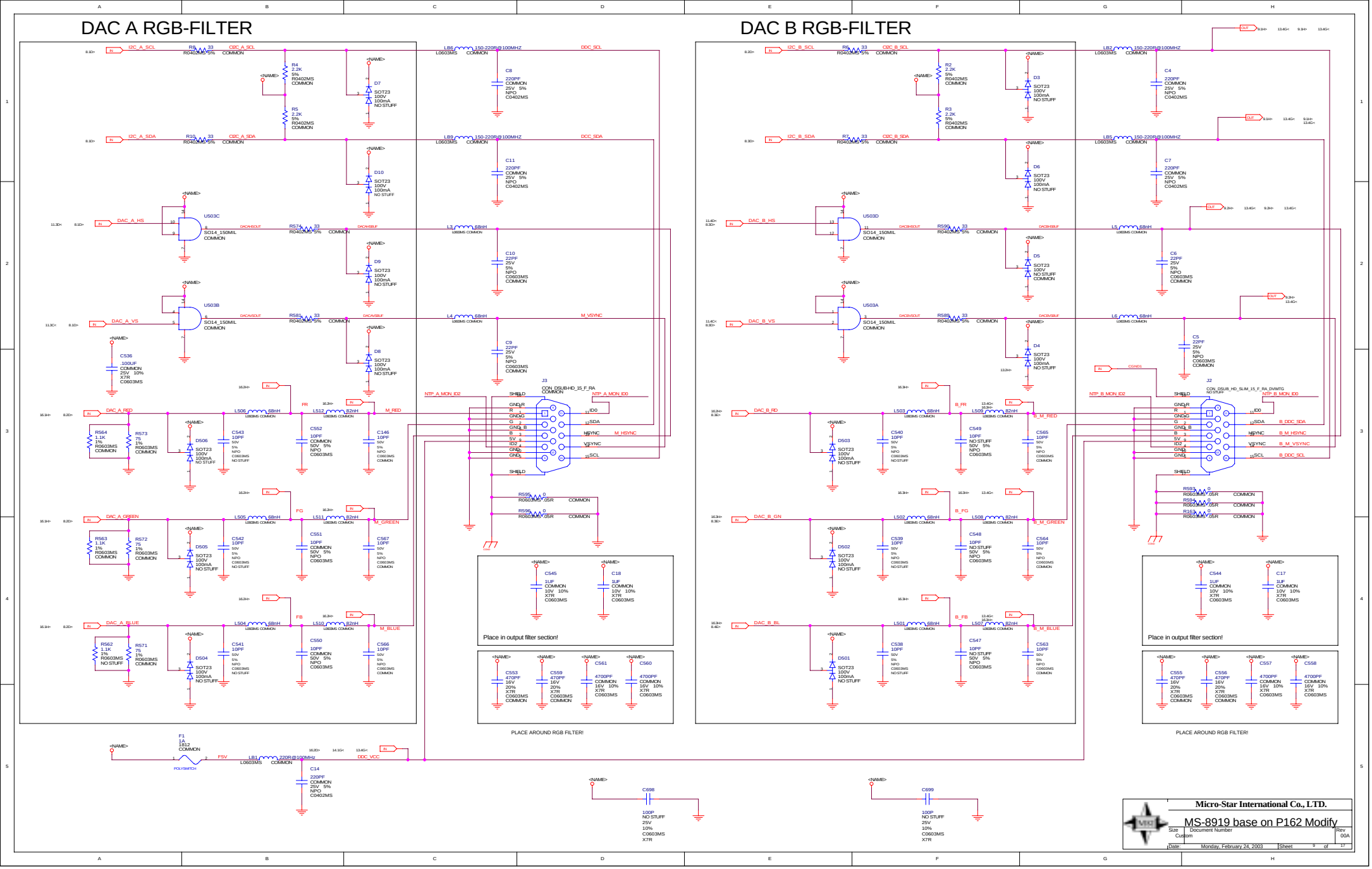
DAC A RGB-FILTER
DAC B RGB-FILTER
I2C_A_SCL
I2C_A_SDA
DAC_A_HS
DAC_A_VS
DAC_A_RED
DAC_A_GREEN
DAC_A_BLUE
I2C_B_SCL
I2C_B_SDA
DAC_B_HS
DAC_B_VS
DAC_B_RD
DAC_B_GN
DAC_B_BL
DDC_SCL
DDC_SDA
M_VSYNC
M_HSYNC
M_RED
M_GREEN
M_BLUE
B_M_HSYNC
B_M_VSYNC
B_DDC_SDA
B_DDC_SCL
DDC_VCC
F5V
NTP_A_MON_ID2
NTP_A_MON_ID0
NTP_B_MON_ID2
NTP_B_MON_ID0
CON_DSUB-HD_15_F_RA
CON_DSUB_HD_SLIM_15_F_RA_DVIMTG
SO14_150MIL
SOT23
Place in output filter section!
PLACE AROUND RGB FILTER!
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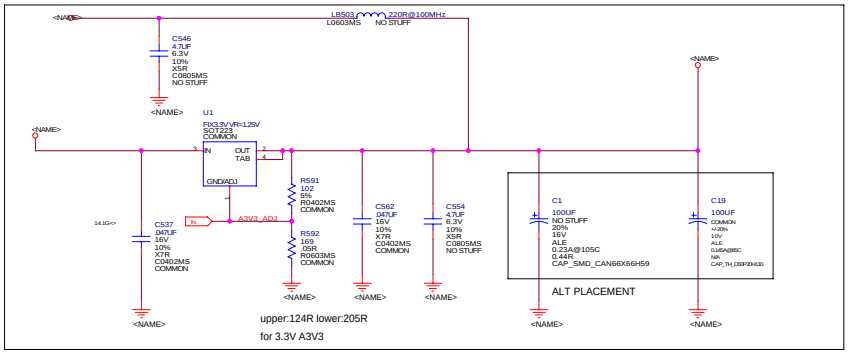
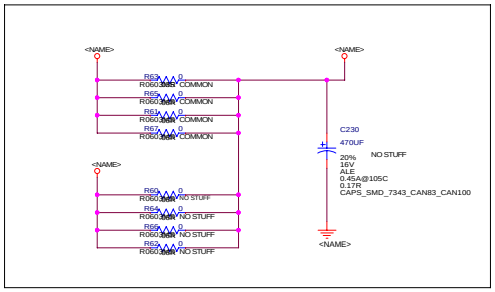
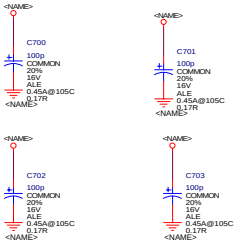
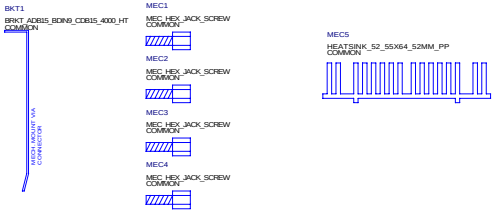
Analog Power Supply



FBVDD 3.3/2.5V







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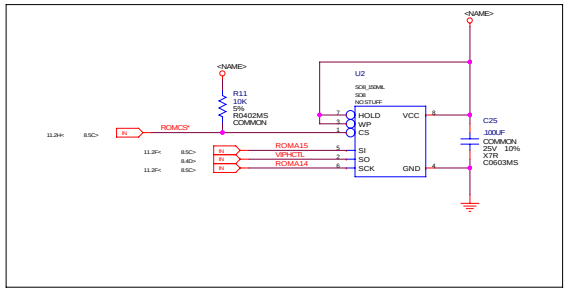
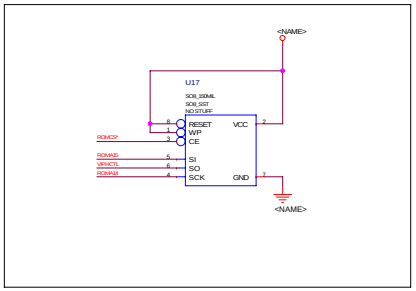
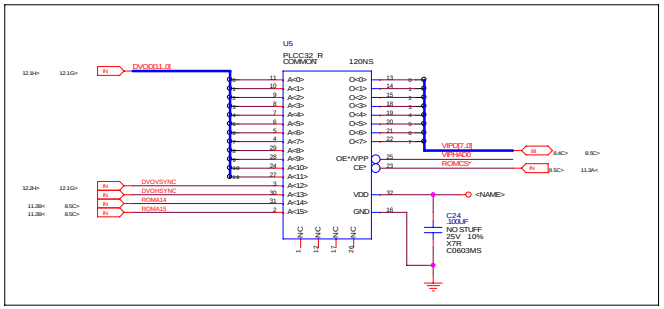
ATL BIOS (ATMEL Serial ROM)



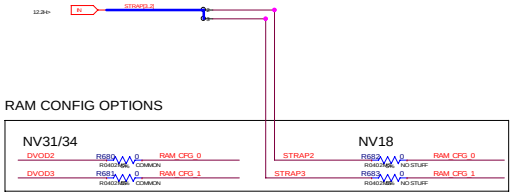
BIOS (SST Serial ROM)

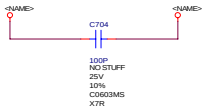


PARALLEL EPROM

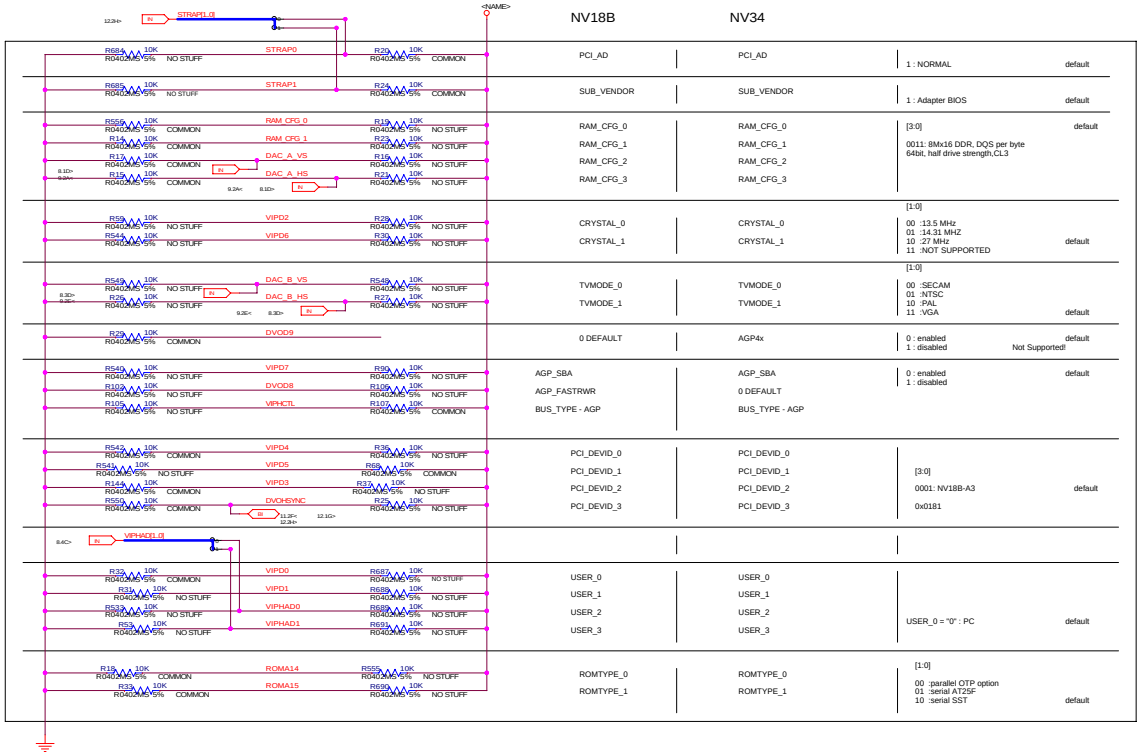


RAM CONFIG OPTIONS





STRAPPING



	NV18B	NV34		
	PCI_AD	PCI_AD	1 : NORMAL	default
	SUB_VENDOR	SUB_VENDOR	1 : Adapter BIOS	default
	RAM_CFG_0	RAM_CFG_0	[3:0]	default
	RAM_CFG_1	RAM_CFG_1	0011: 8Mx16 DDR, DQS per byte 64bit, half drive strength,CL3	
	RAM_CFG_2	RAM_CFG_2		
	RAM_CFG_3	RAM_CFG_3		
	CRYSTAL_0	CRYSTAL_0	[1:0] 00 :13.5 MHz 01 :14.31 MHZ 10 :27 MHz 11 :NOT SUPPORTED	
	CRYSTAL_1	CRYSTAL_1		default
	TVMODE_0	TVMODE_0	[1:0] 00 :SECAM 01 :NTSC 10 :PAL 11 :VGA	
	TVMODE_1	TVMODE_1		default
	0 DEFAULT	AGP4x	0 : enabled 1 : disabled	default Not Supported!
	AGP_SBA	AGP_SBA	0 : enabled 1 : disabled	default
	AGP_FASTRWR	0 DEFAULT		
	BUS_TYPE - AGP	BUS_TYPE - AGP		
	PCI_DEVID_0	PCI_DEVID_0		
	PCI_DEVID_1	PCI_DEVID_1	[3:0]	
	PCI_DEVID_2	PCI_DEVID_2	0001: NV18B-A3	default
	PCI_DEVID_3	PCI_DEVID_3	0x0181	
	USER_0	USER_0	USER_0 = "0" : PC	default
	USER_1	USER_1		
	USER_2	USER_2		
	USER_3	USER_3		
	ROMTYPE_0	ROMTYPE_0	[1:0] 00 :parallel OTP option 01 :serial AT25F 10 :serial SST	
	ROMTYPE_1	ROMTYPE_1		default

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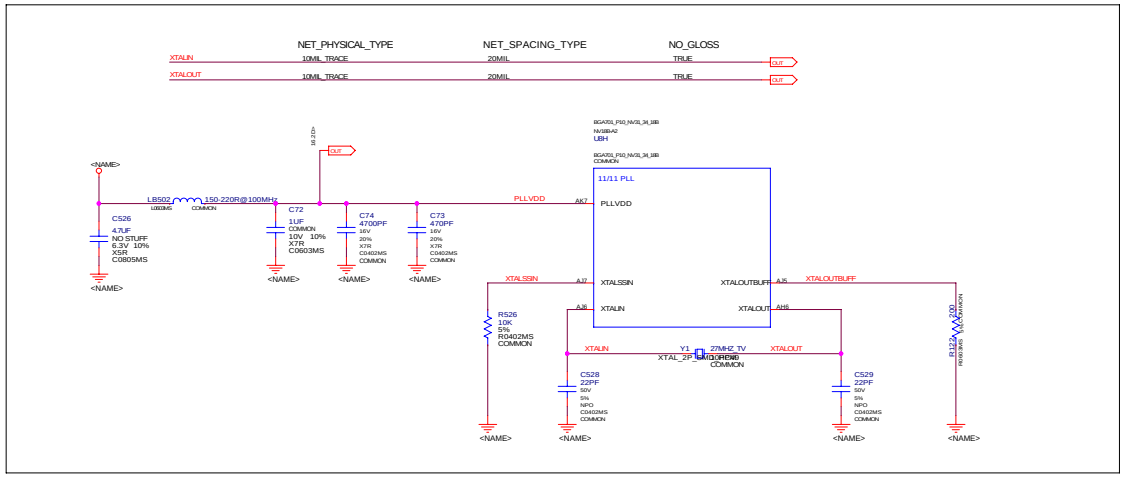
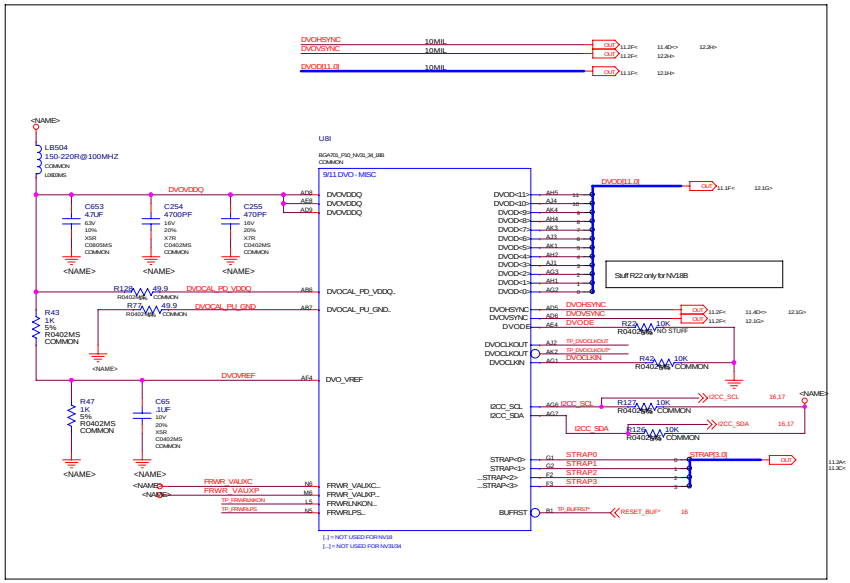
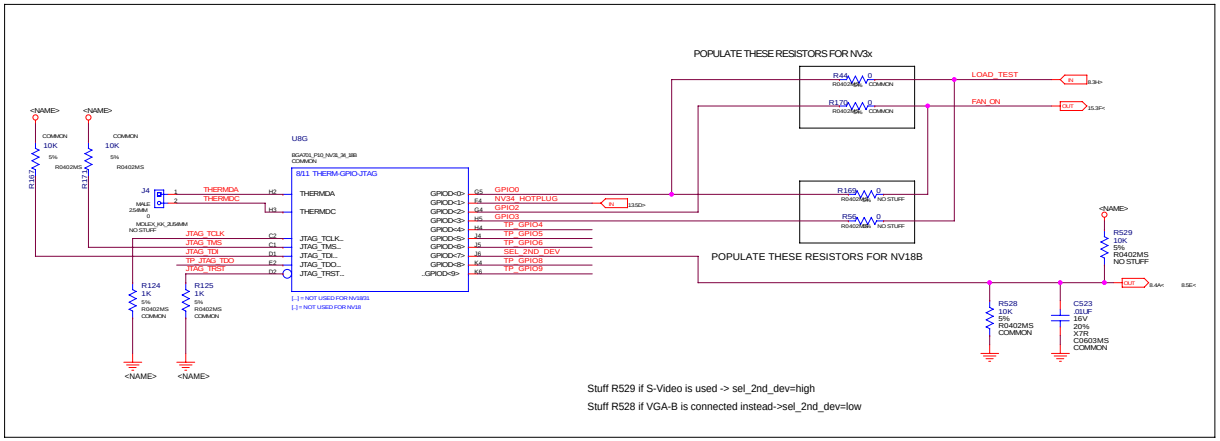
CLOCK

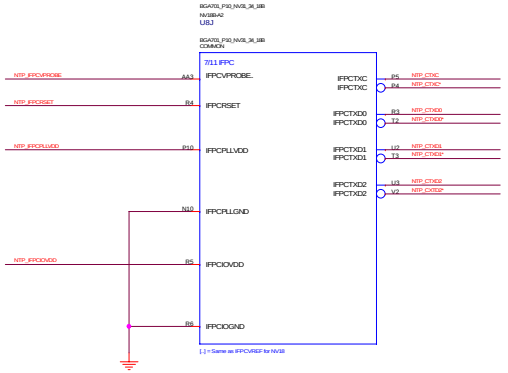


DVO



NV34 THERMAL





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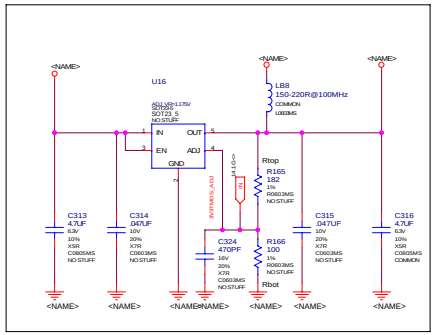
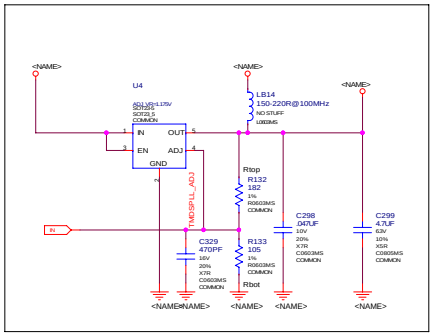
TMDS IO Supply



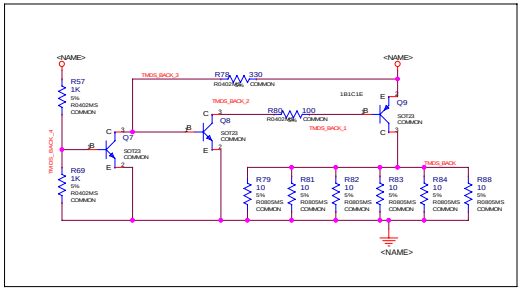
Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+(100/182))

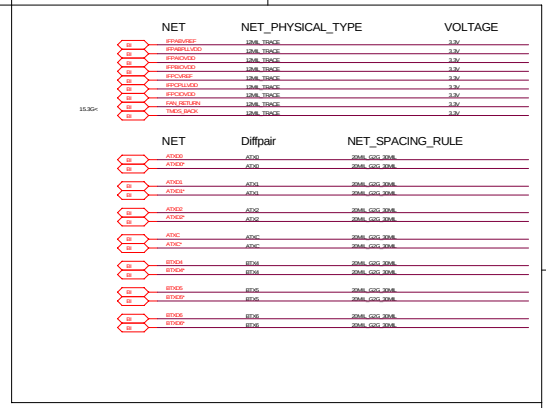
TMDS PLL Supply



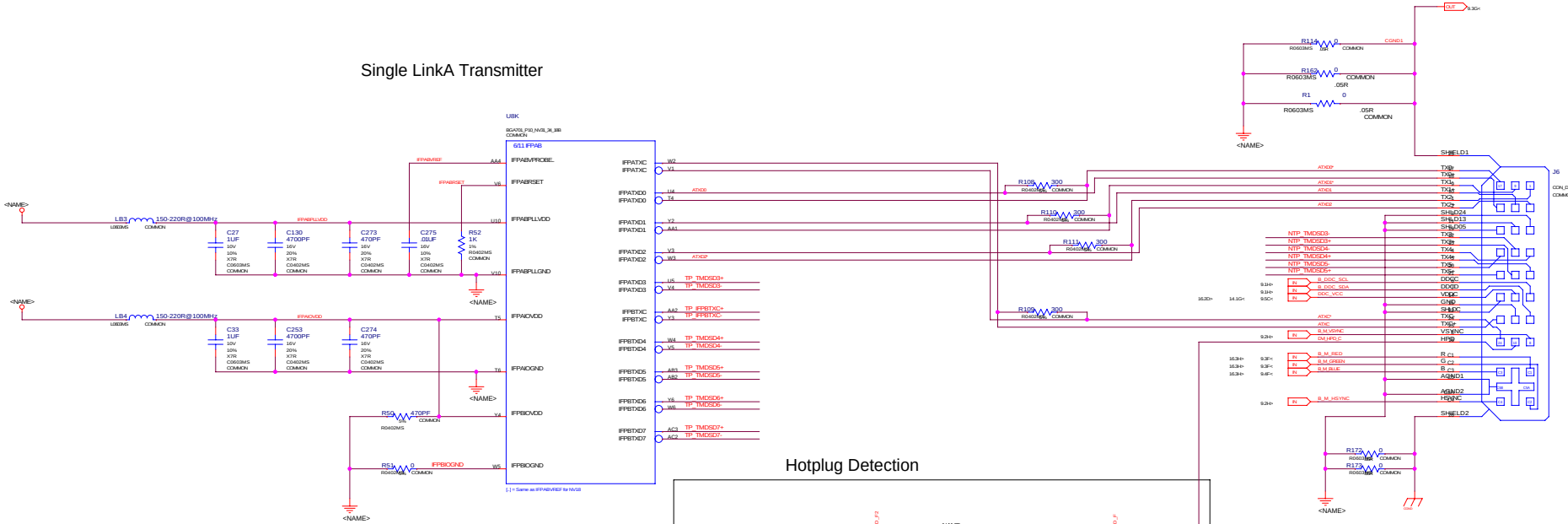
Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+(100/182))

TMDS backdrive prevention

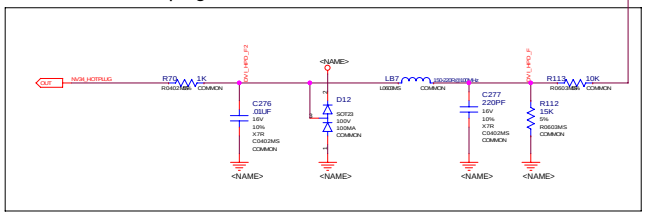


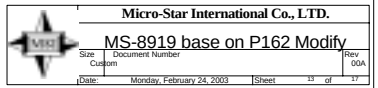


Single LinkA Transmitter

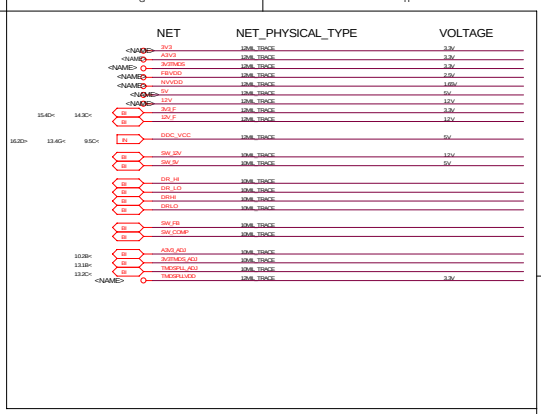


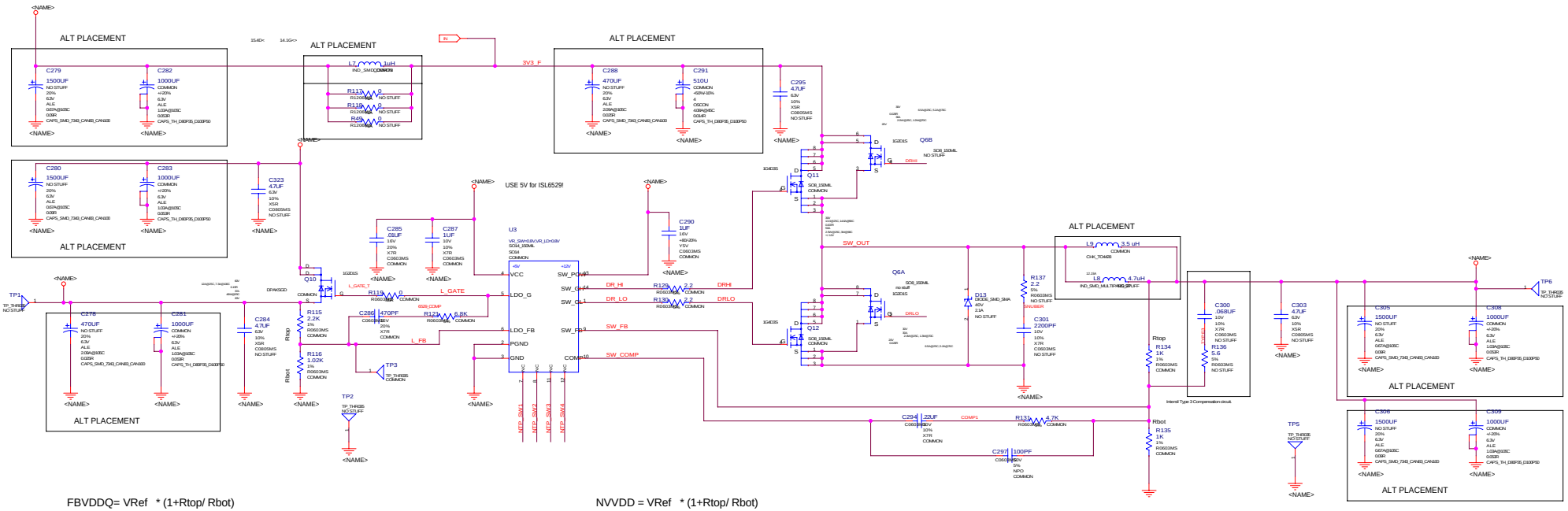
Hotplug Detection





NVVDD-SWITCHER / FBVDDQ-LDO CONTROLER ISL6529





	FBVDDQ= VRef * (1+Rtop/ Rbot)		NVVDD = VRef * (1+Rtop/ Rbot)
ISL6529	2.52V = 0.800V * (1+2.2k/1.02k)	NV18B	1.60V = 0.800V * (1+1000/1000)
		NV31	1.107V = 0.800V * (1+392/1020)

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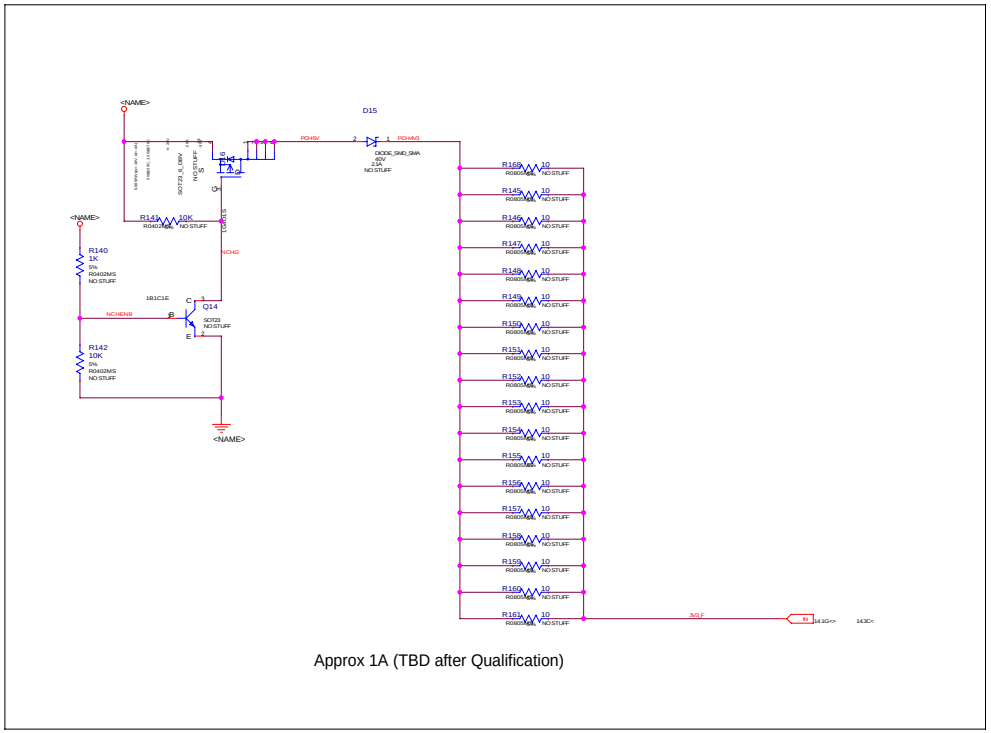
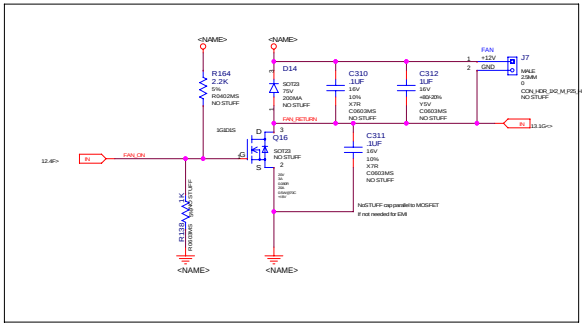
NVVDD Current Supplement.



Approx 1A (TBD after Qualification)

FAN Control



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MS-8919 base on P162 Modify			
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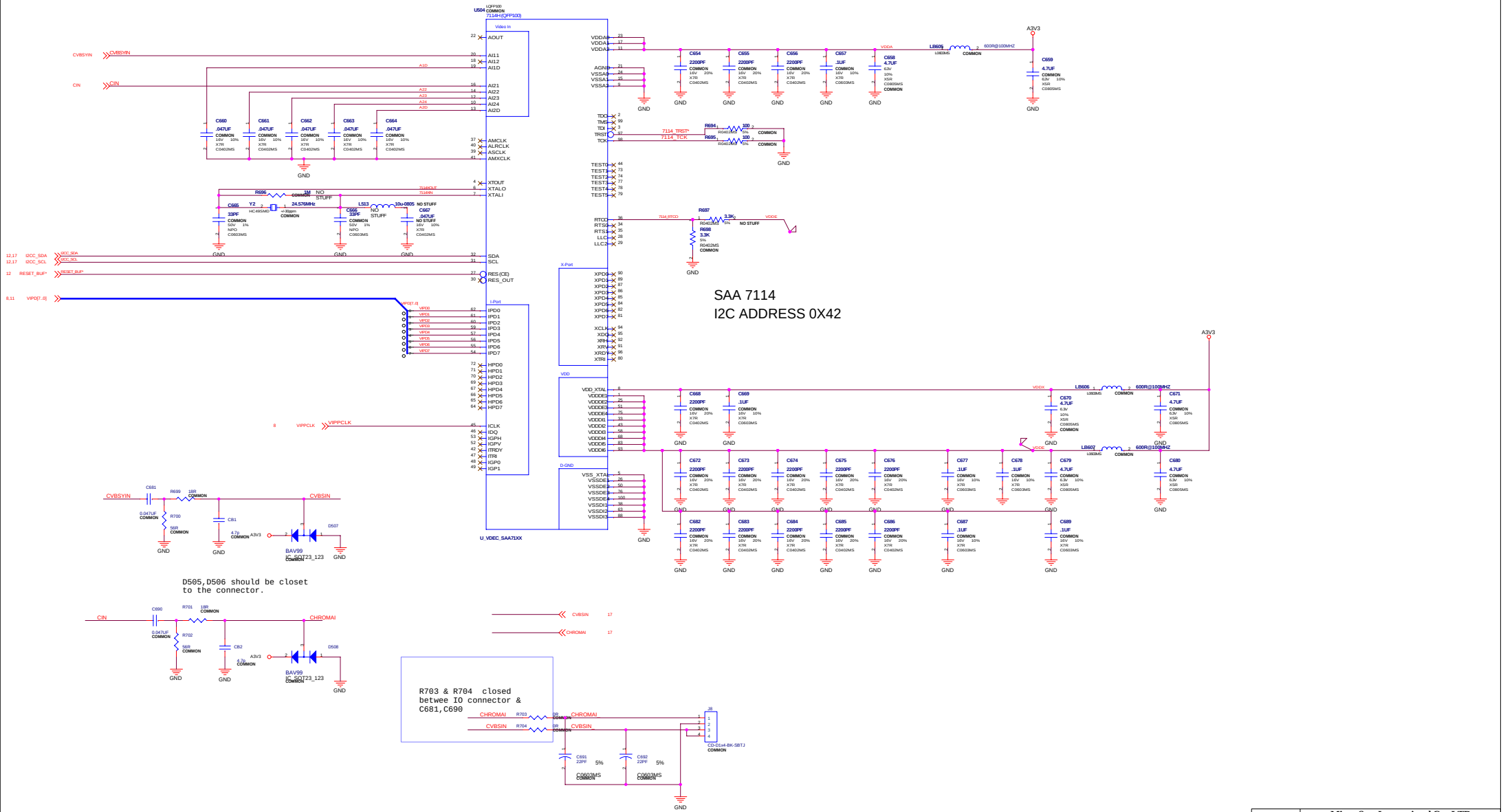
U504 COMMON
7114H(QFP100)
Video In
U_VDEC_SAA7IXX
SAA 7114
I2C ADDRESS 0X42
D505,D506 should be closet
to the connector.
R703 & R704 closed
betwee IO connector &
C681,C690
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VIDEO OUT , internal DAC