

C116, NV18, 8MX16DDR, 128MB, Video IN/OUT, DVI-I, VGA

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	NVVDD, MEM_VDD, A3V3, TMDS3V3, TMDSPLL
	20 MECHANICS, and FBVDD

HISTORY:

X00:	INITIAL VERSION
X01	Remove R117, C87, C131, C143 for CKE
	Change C736, C743 to 18pf capacitors.
	Remove C1099 - additional Capacitor for AGPVREFcg
	Changed AGPVREFcg circuit.

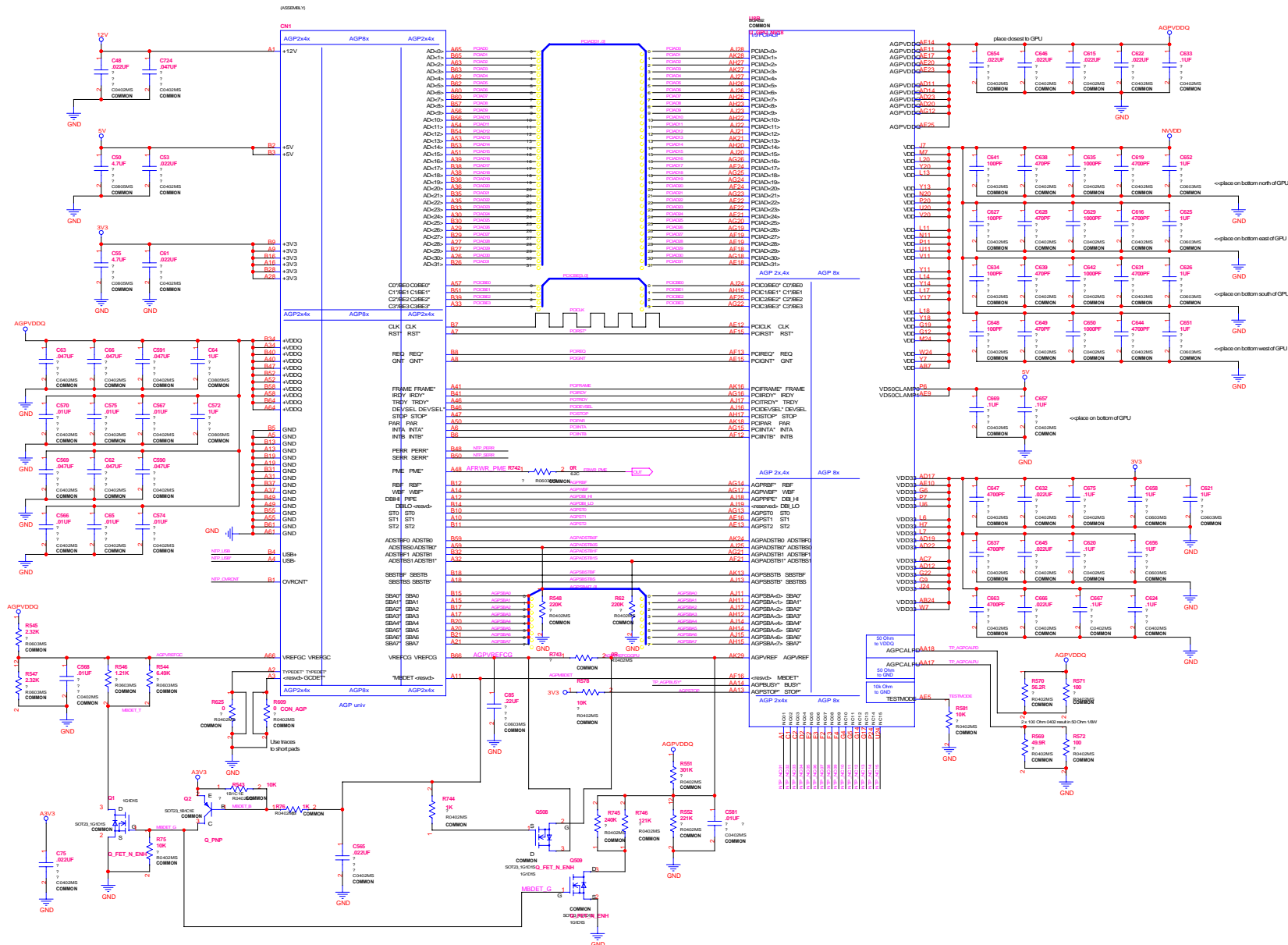
C116 Base on P112 to Modify.

- 1. Change page 4~7 & page 18 Reference.
- 2. Change J1 foot print from slim type to stand D-SUB.
- 3. Remove I1394 function.
- 4. Page 2, change voltage C75.1 & Q2.E from 3V3 to A3V3.
- 5. Page 8, Add Twin Bios for MSI function.
- 6. Page 16 ,replace INTERNAL VIDEO CAPTURE CONNECTOR.
- 7. Page 17 ,ADD C874 & C1098 ALE CAP. (DUAL-LAY)
- 8. Page 18 , Add H/W Monitor founction for MSI .

600-10116-000X-A00

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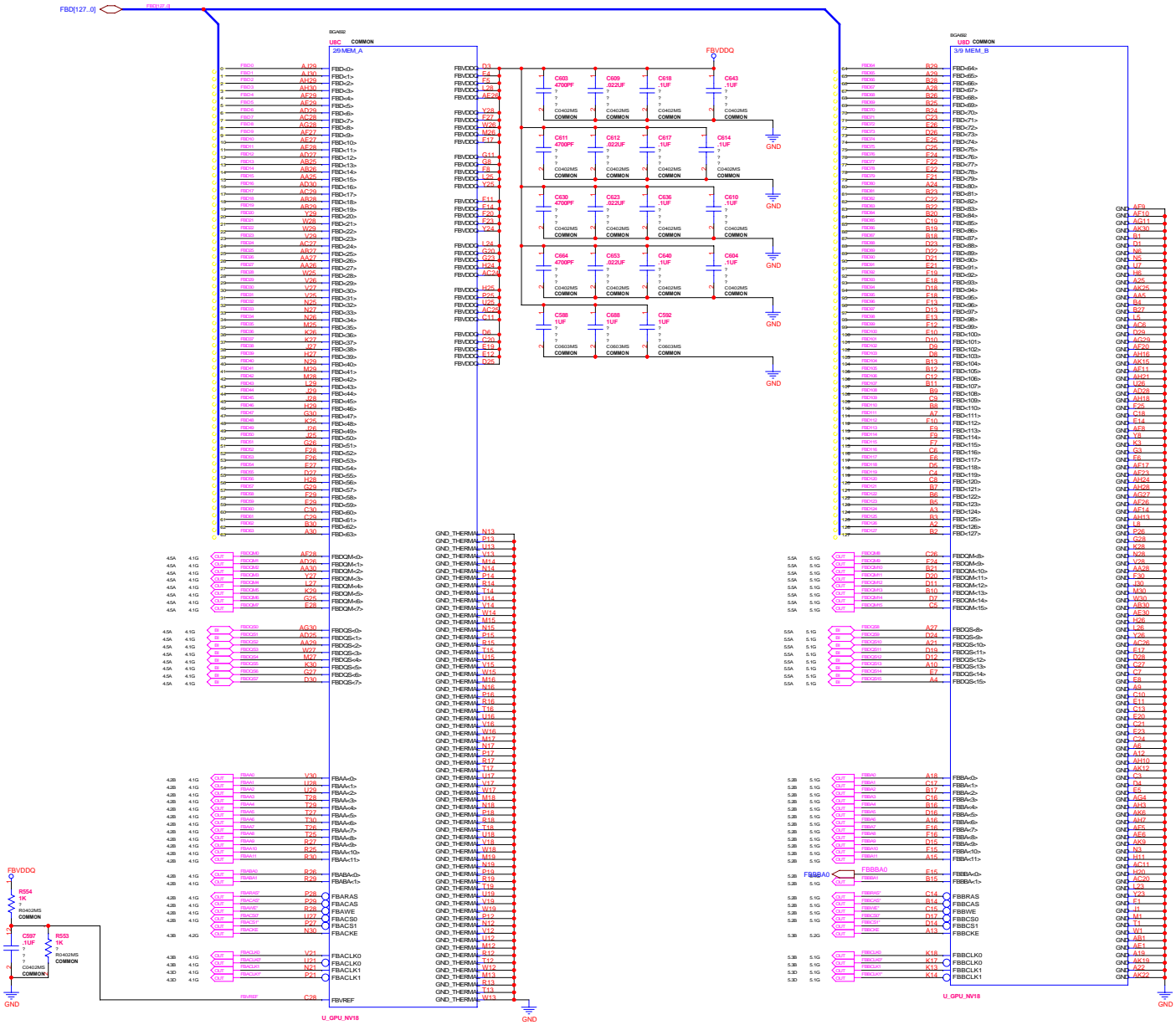
## NV18 AGP SECTION AND AGP CONNECTOR



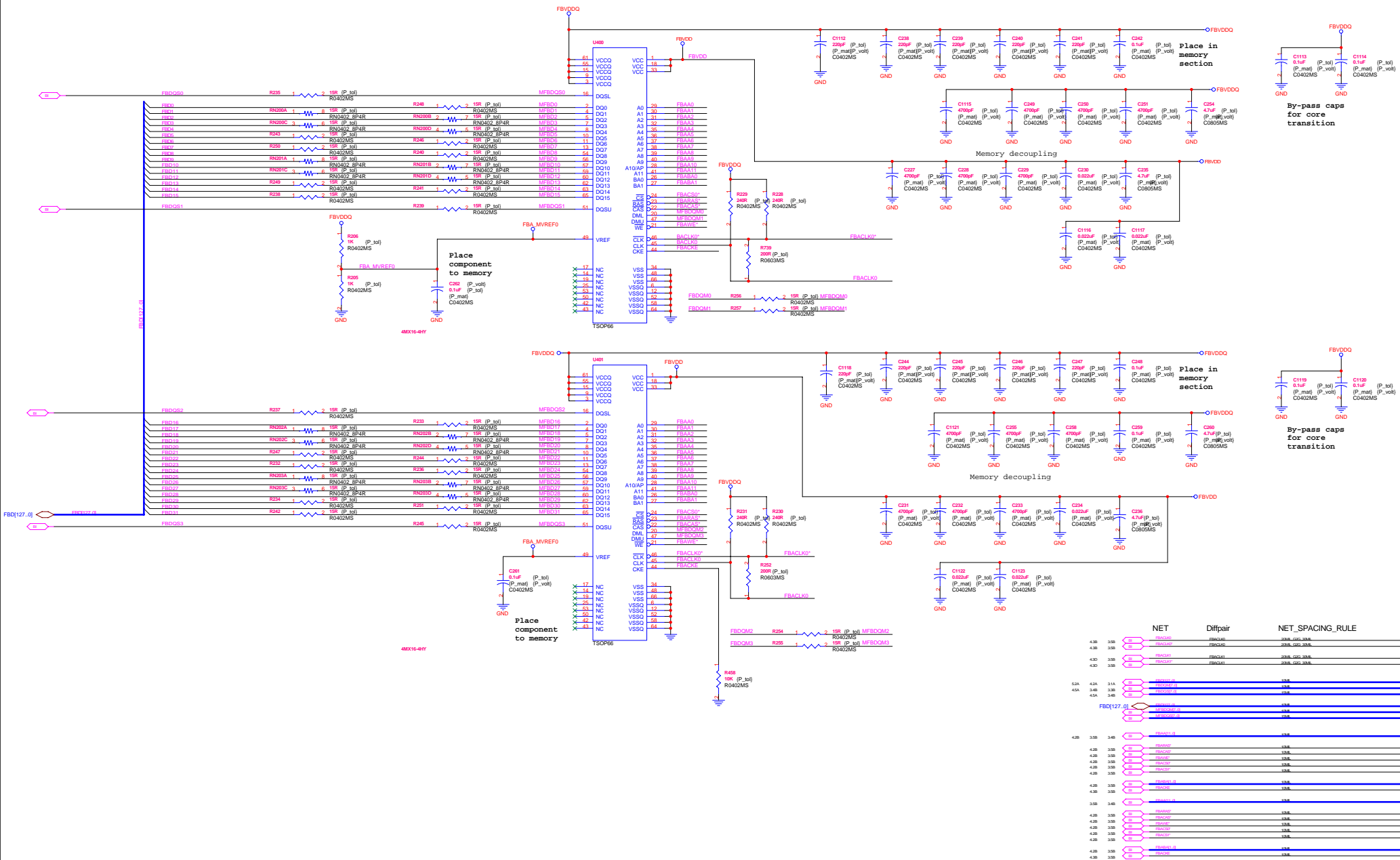
## AGP spacing rules

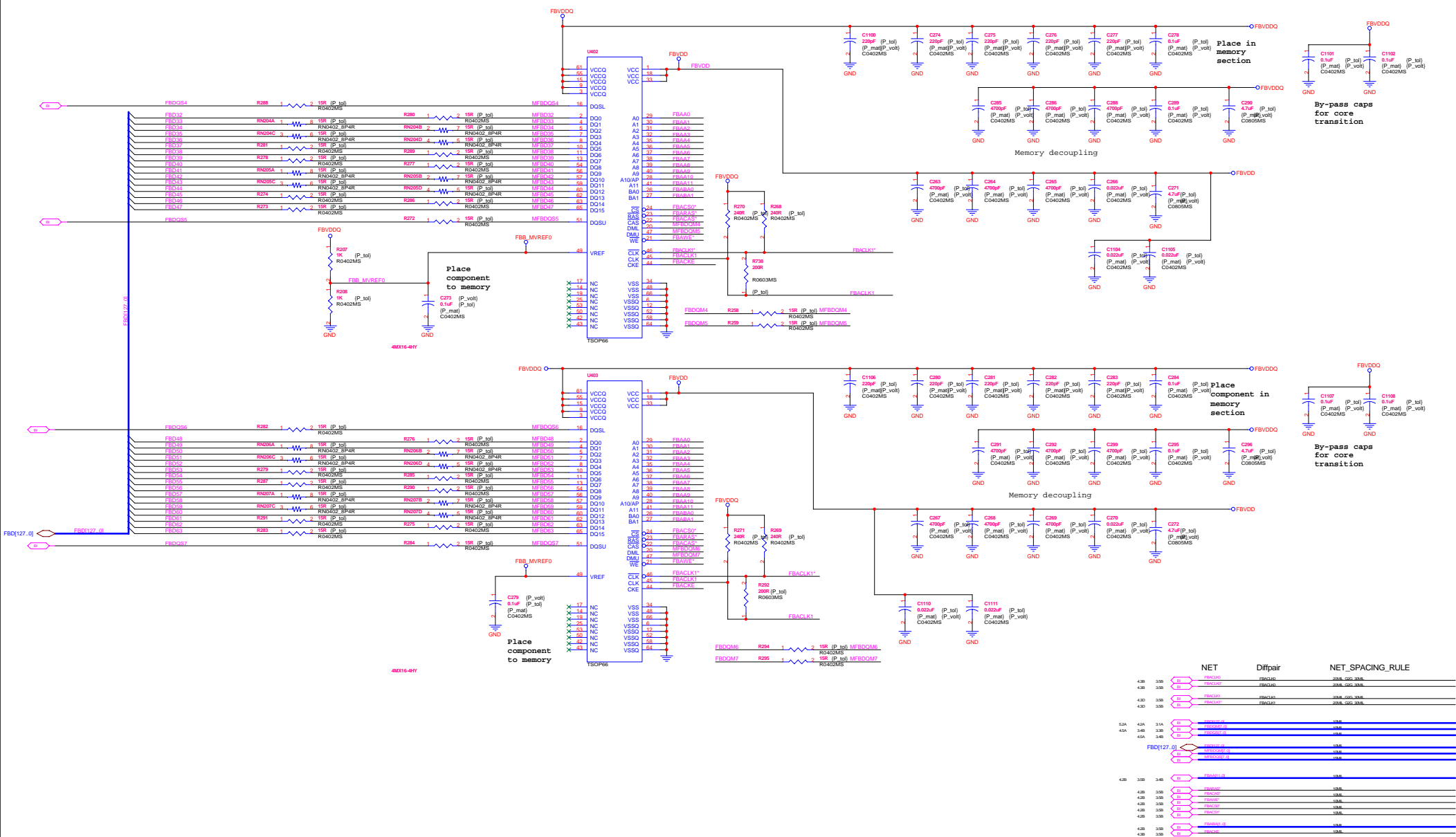
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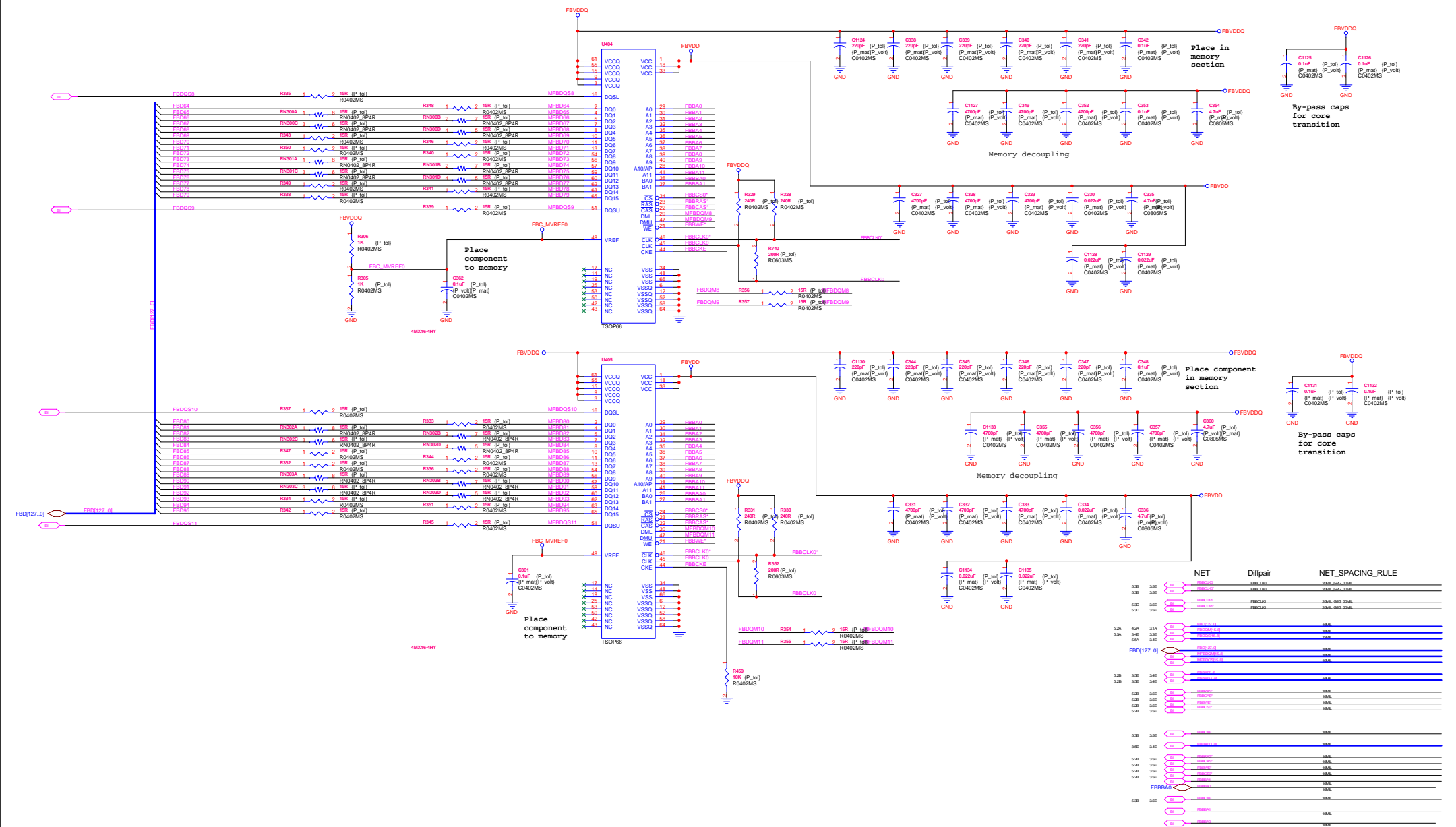
## NV18 FRAMEBUFFER INTERFACE AND DECOUPLING

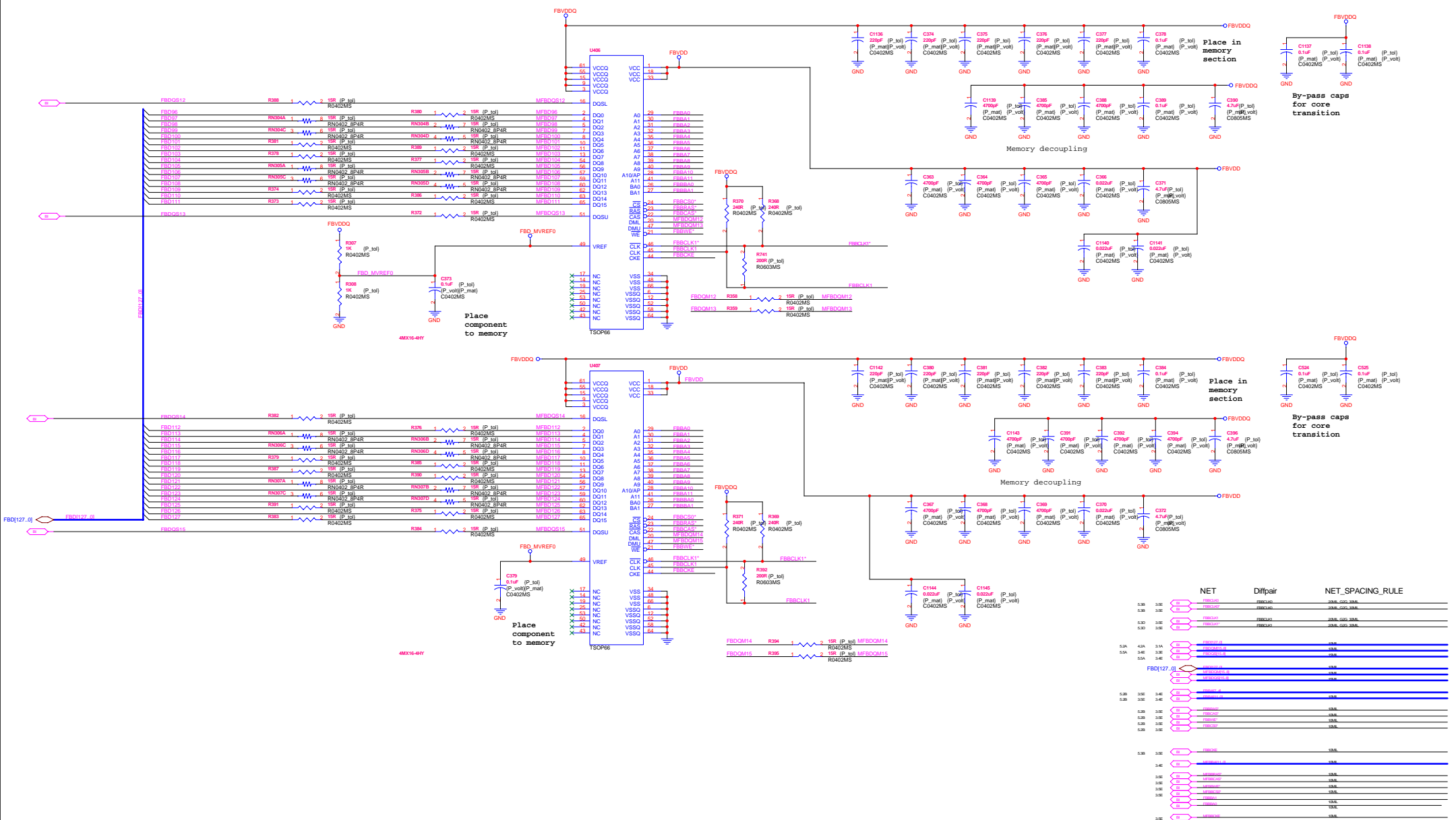


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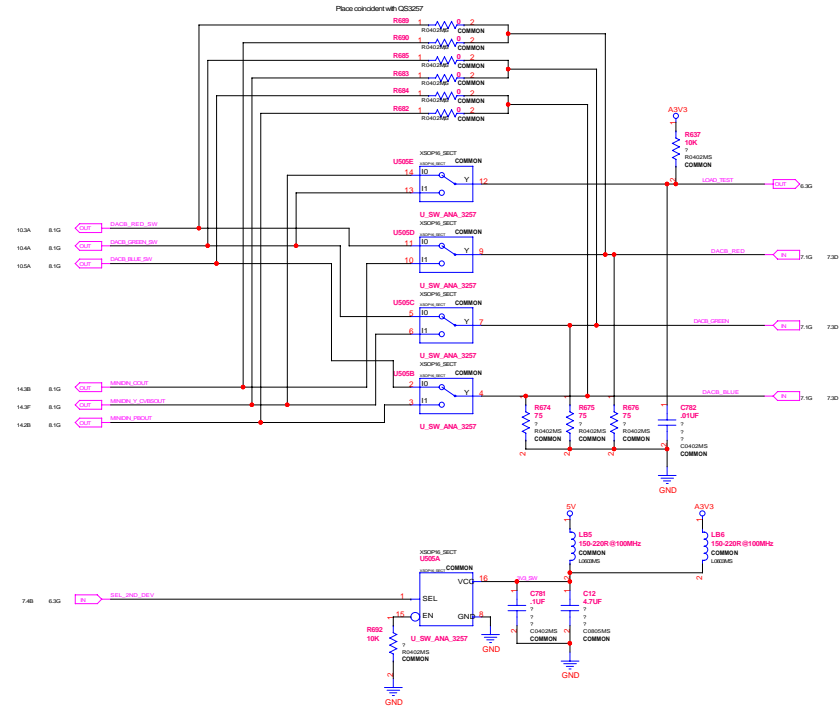








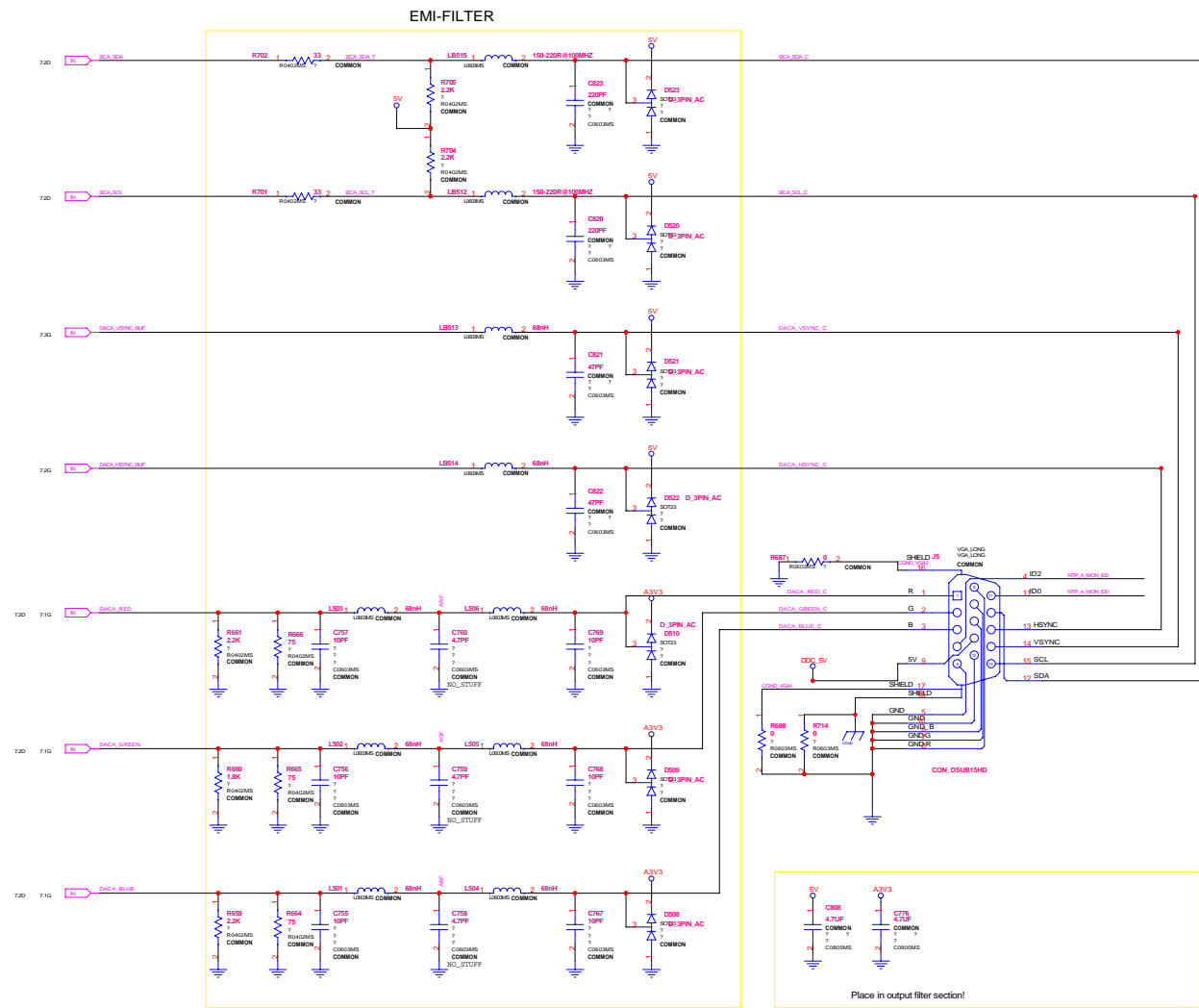
## DACB SWITCH BETWEEN VGA OUT AND TV OUT



	NET	Diffpair	NET_SPACING_RULE
103A	0.3C	0.5C	0.25M, 0.05C, 0.05M
104A	0.3C	0.5C	0.25M, 0.05C, 0.05M
105A	0.3C	0.5C	0.25M, 0.05C, 0.05M
143B	0.3C	0.5C	0.25M, 0.05C, 0.05M
143F	0.3C	0.5C	0.25M, 0.05C, 0.05M
143B	0.3C	0.5C	0.25M, 0.05C, 0.05M

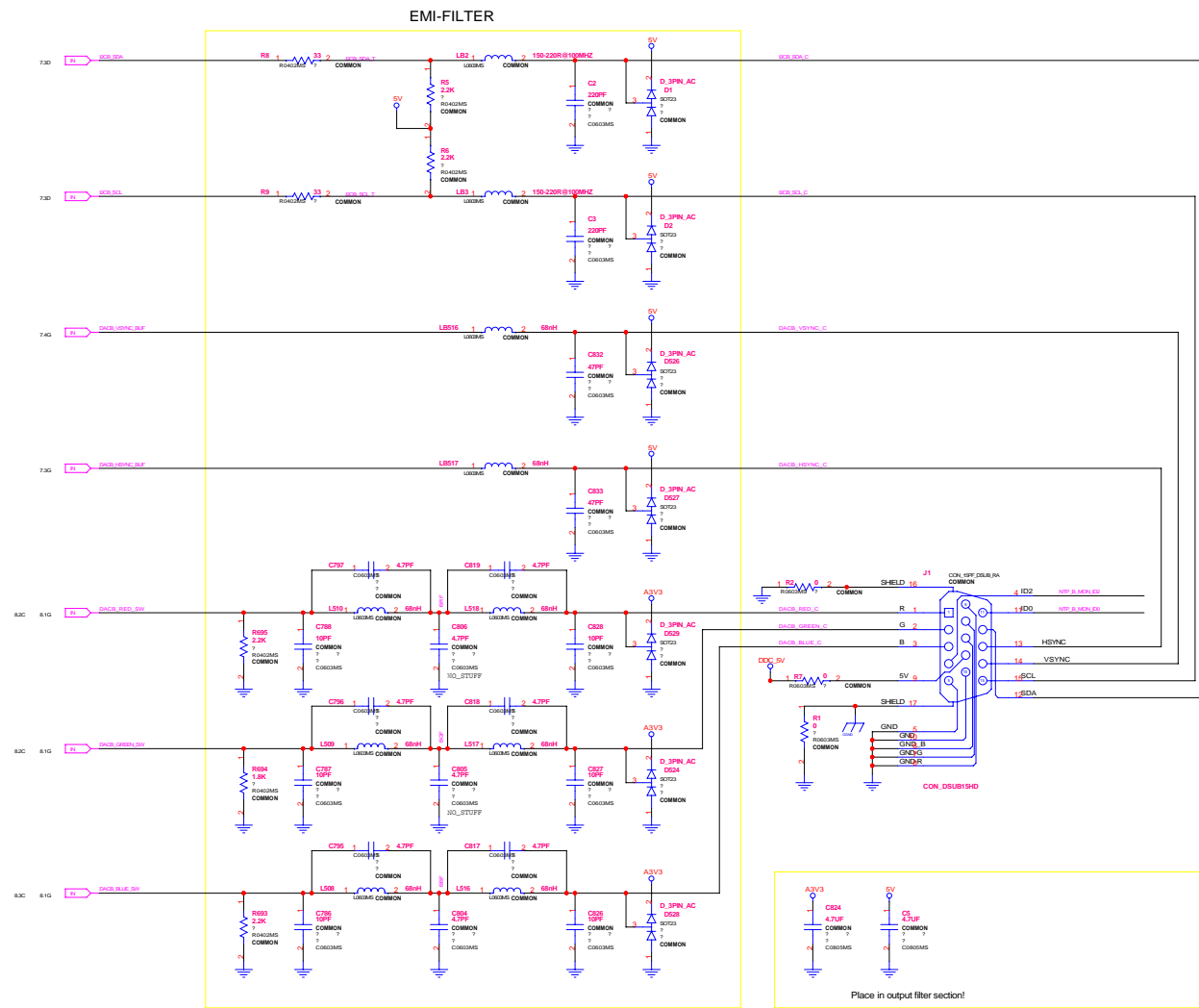
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DACA output



NET	Diffpair	NET_SPACING_RULE
DIFF		DIFF_001_20M
DIFF		DIFF_002_20M
DIFF		DIFF_003_20M
DACA_RED_0		DIFF_001_20M
DACA_GREEN_0		DIFF_001_20M
DACA_BLUE_0		DIFF_001_20M

DACB output



NET	Diffpair	NET_SPACING_RULE
C1	DIFF	20MIL_GND_20MIL
C2	DIFF	20MIL_GND_20MIL
C3	DIFF	20MIL_GND_20MIL
C4	DIFF	20MIL_GND_20MIL
C5	DIFF	20MIL_GND_20MIL
C6	DIFF	20MIL_GND_20MIL
C7	DIFF	20MIL_GND_20MIL
C8	DIFF	20MIL_GND_20MIL
C9	DIFF	20MIL_GND_20MIL
C10	DIFF	20MIL_GND_20MIL
C11	DIFF	20MIL_GND_20MIL
C12	DIFF	20MIL_GND_20MIL
C13	DIFF	20MIL_GND_20MIL
C14	DIFF	20MIL_GND_20MIL
C15	DIFF	20MIL_GND_20MIL
C16	DIFF	20MIL_GND_20MIL
C17	DIFF	20MIL_GND_20MIL
C18	DIFF	20MIL_GND_20MIL
C19	DIFF	20MIL_GND_20MIL
C20	DIFF	20MIL_GND_20MIL
C21	DIFF	20MIL_GND_20MIL
C22	DIFF	20MIL_GND_20MIL
C23	DIFF	20MIL_GND_20MIL
C24	DIFF	20MIL_GND_20MIL
C25	DIFF	20MIL_GND_20MIL
C26	DIFF	20MIL_GND_20MIL
C27	DIFF	20MIL_GND_20MIL
C28	DIFF	20MIL_GND_20MIL
C29	DIFF	20MIL_GND_20MIL
C30	DIFF	20MIL_GND_20MIL
C31	DIFF	20MIL_GND_20MIL
C32	DIFF	20MIL_GND_20MIL
C33	DIFF	20MIL_GND_20MIL
C34	DIFF	20MIL_GND_20MIL
C35	DIFF	20MIL_GND_20MIL
C36	DIFF	20MIL_GND_20MIL
C37	DIFF	20MIL_GND_20MIL
C38	DIFF	20MIL_GND_20MIL
C39	DIFF	20MIL_GND_20MIL
C40	DIFF	20MIL_GND_20MIL
C41	DIFF	20MIL_GND_20MIL
C42	DIFF	20MIL_GND_20MIL
C43	DIFF	20MIL_GND_20MIL
C44	DIFF	20MIL_GND_20MIL
C45	DIFF	20MIL_GND_20MIL
C46	DIFF	20MIL_GND_20MIL
C47	DIFF	20MIL_GND_20MIL
C48	DIFF	20MIL_GND_20MIL
C49	DIFF	20MIL_GND_20MIL
C50	DIFF	20MIL_GND_20MIL
C51	DIFF	20MIL_GND_20MIL
C52	DIFF	20MIL_GND_20MIL
C53	DIFF	20MIL_GND_20MIL
C54	DIFF	20MIL_GND_20MIL
C55	DIFF	20MIL_GND_20MIL
C56	DIFF	20MIL_GND_20MIL
C57	DIFF	20MIL_GND_20MIL
C58	DIFF	20MIL_GND_20MIL
C59	DIFF	20MIL_GND_20MIL
C60	DIFF	20MIL_GND_20MIL
C61	DIFF	20MIL_GND_20MIL
C62	DIFF	20MIL_GND_20MIL
C63	DIFF	20MIL_GND_20MIL
C64	DIFF	20MIL_GND_20MIL
C65	DIFF	20MIL_GND_20MIL
C66	DIFF	20MIL_GND_20MIL
C67	DIFF	20MIL_GND_20MIL
C68	DIFF	20MIL_GND_20MIL
C69	DIFF	20MIL_GND_20MIL
C70	DIFF	20MIL_GND_20MIL
C71	DIFF	20MIL_GND_20MIL
C72	DIFF	20MIL_GND_20MIL
C73	DIFF	20MIL_GND_20MIL
C74	DIFF	20MIL_GND_20MIL
C75	DIFF	20MIL_GND_20MIL
C76	DIFF	20MIL_GND_20MIL
C77	DIFF	20MIL_GND_20MIL
C78	DIFF	20MIL_GND_20MIL
C79	DIFF	20MIL_GND_20MIL
C80	DIFF	20MIL_GND_20MIL
C81	DIFF	20MIL_GND_20MIL
C82	DIFF	20MIL_GND_20MIL
C83	DIFF	20MIL_GND_20MIL
C84	DIFF	20MIL_GND_20MIL
C85	DIFF	20MIL_GND_20MIL
C86	DIFF	20MIL_GND_20MIL
C87	DIFF	20MIL_GND_20MIL
C88	DIFF	20MIL_GND_20MIL
C89	DIFF	20MIL_GND_20MIL
C90	DIFF	20MIL_GND_20MIL
C91	DIFF	20MIL_GND_20MIL
C92	DIFF	20MIL_GND_20MIL
C93	DIFF	20MIL_GND_20MIL
C94	DIFF	20MIL_GND_20MIL
C95	DIFF	20MIL_GND_20MIL
C96	DIFF	20MIL_GND_20MIL
C97	DIFF	20MIL_GND_20MIL
C98	DIFF	20MIL_GND_20MIL
C99	DIFF	20MIL_GND_20MIL
C100	DIFF	20MIL_GND_20MIL

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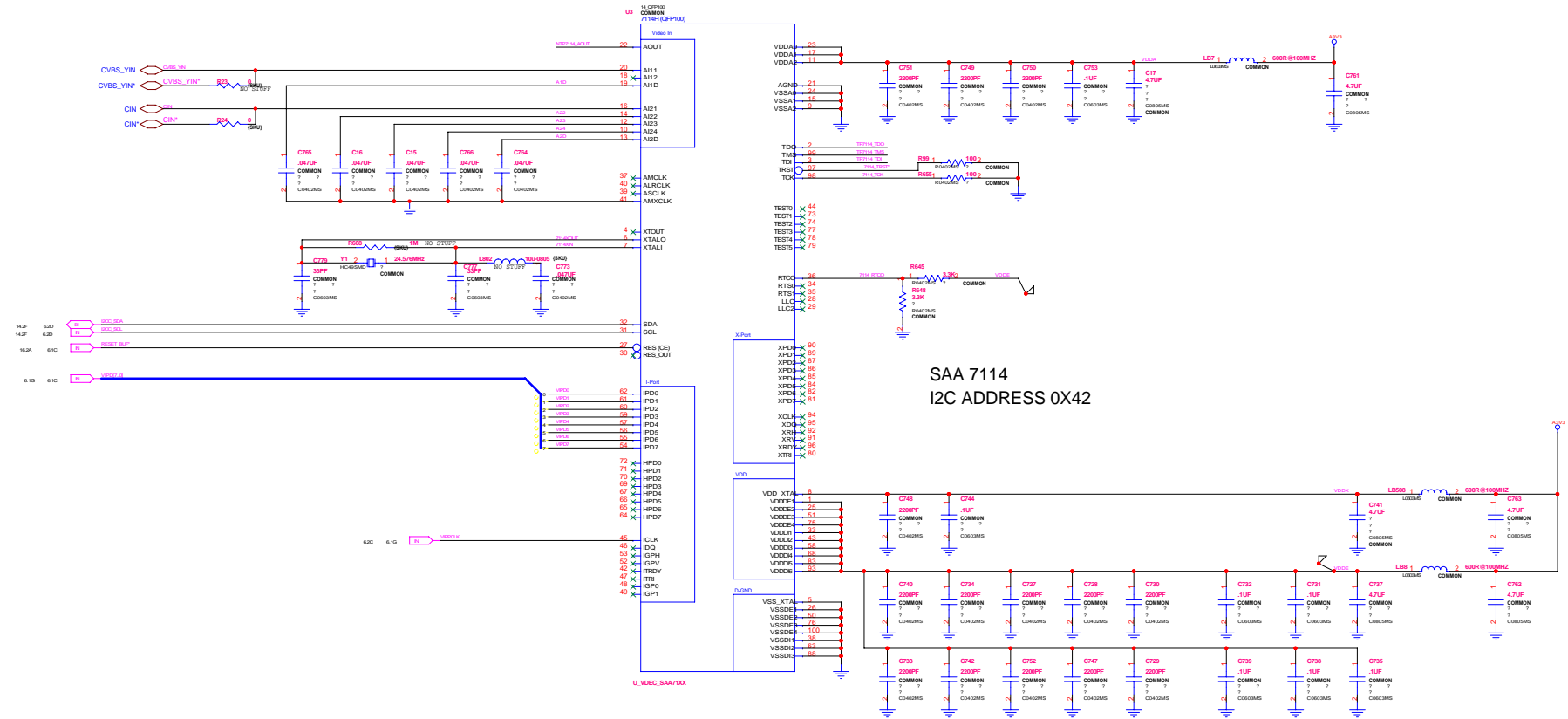
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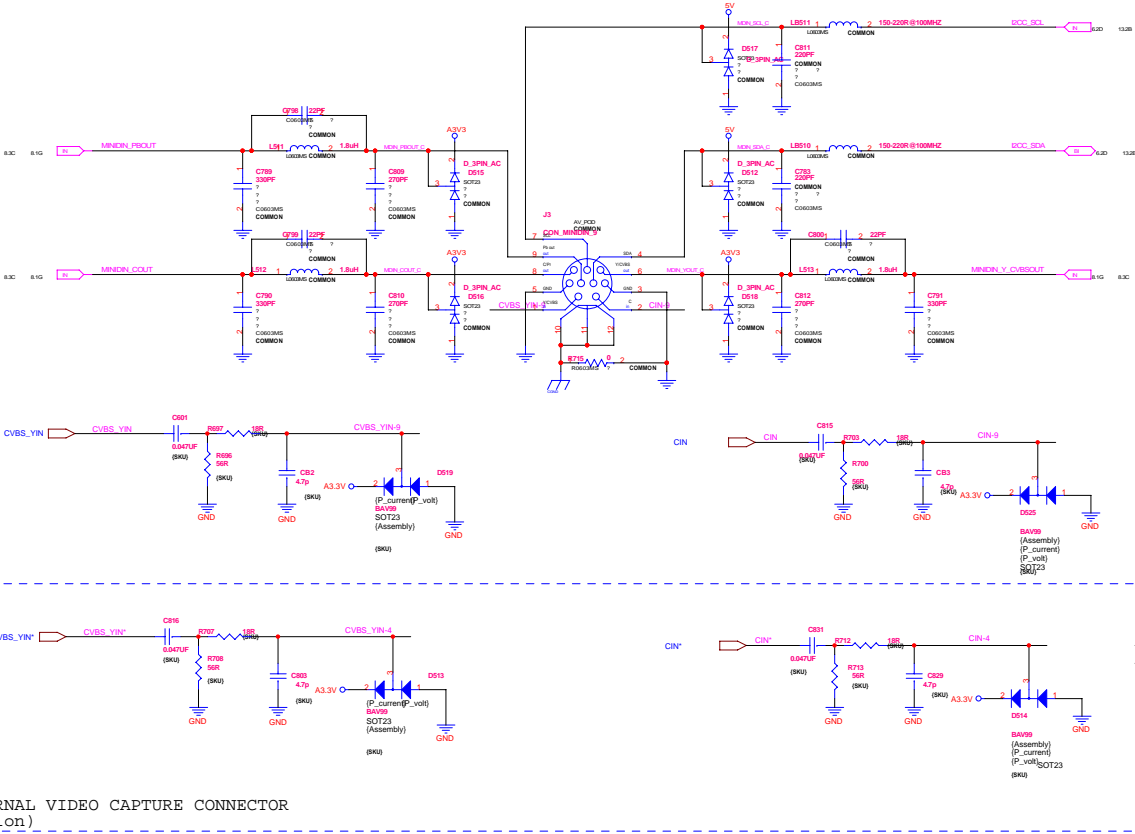
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## VIDEO CAPTURE



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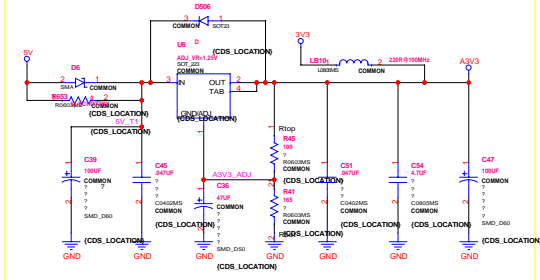
VIDEO IN/OUT CONNECTOR



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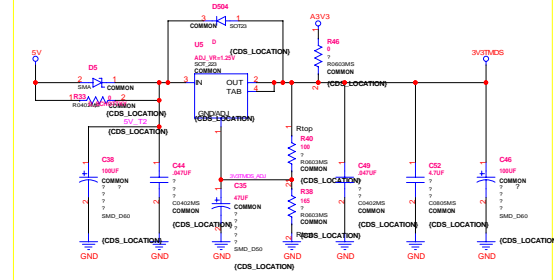


## ANALOG 3V3



$$V_{out} = V_{Ref} * (1 + R_{bot}/R_{top})$$
$$3.31V = 1.25V * (1 + (165/100))$$

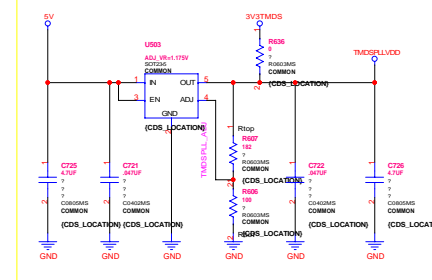
### TMD5 3V3 Supply



$$V_{out} = V_{Ref} * (1 + R_{bot}/R_{top})$$

$$3.31V = 1.25V * (1 + (165/100))$$

TMDS PLL Supply

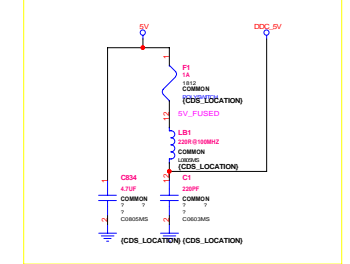


$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

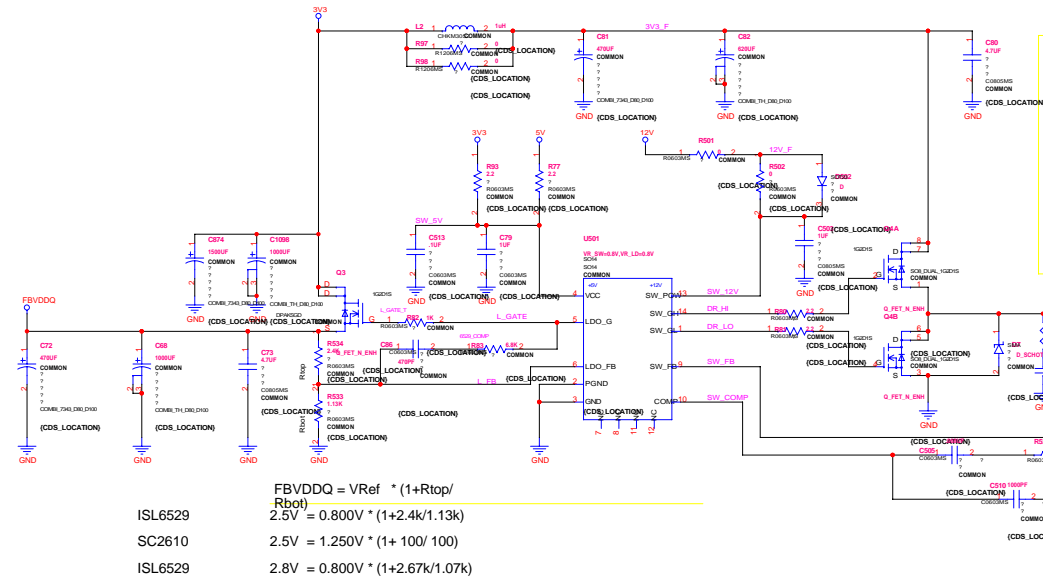
$$3.31V = 1.175V * (1 + (100/182))$$

[illegible]

## DDC 5V

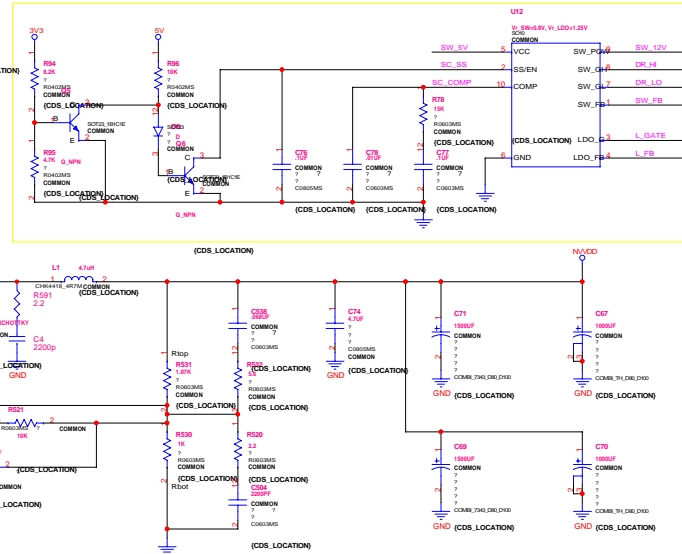


## NVDD-SWITCHER / FBVDD-LDO CONTROLER ISL6529



	$FBVDDQ = V_{Ref} * (1 + R_{top}/R_{bot})$
ISL6529	$2.5V = 0.800V * (1 + 2.4k/1.13k)$
SC2610	$2.5V = 1.250V * (1 + 100/100)$
ISL6529	$2.8V = 0.800V * (1 + 2.67k/1.07k)$

## ALTERNATIVE TO ISL6529



$$NVDD = V_{Ref} * (1 + R_{top} / R_{bot})$$

ISL6529	$1.656V = 0.800V * (1+1070/1000)$
SC2610	$1.656V = 0.800V * (1+1070/1000)$

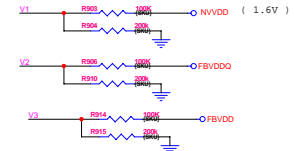
BRACKET

RACK 1, TOP COMMON

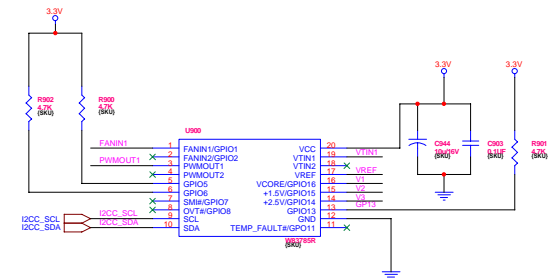
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RED WINGS

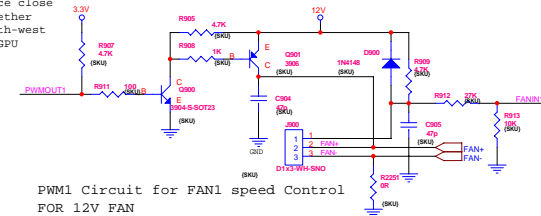
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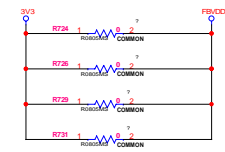
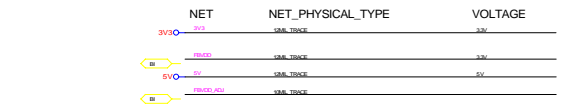
### VOLTAGE SENSING CIRCUIT



Place close  
together  
south-west  
of GPU



PWM1 Circuit for FAN1 speed Control  
FOR 12V FAN

[illegible]

$$3.300V = 1.250V * (1 + 187/115)$$