

P393-A01 Base Design

P393-A01, G92, 8Mx32/16Mx32 GDDR3 (800/1000 MHz),
DVI-I-DL, DVI-I-DL/DisplayPort, HDTVout/Stereo


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REV	VARIANT	NVPN	ASSEMBLY
00	BASE	600-10393-Base-100	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU_DT_0000	600-10393-0000-100	P393 G92-300 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
2	SKU_DT_0002	600-10393-0002-100	P393 G92-200 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
3	SKU_WB_0500	600-10393-0500-100	P393 G92-475 512MB GDDR3 16Mx32 DVI-I+DP+STEREO
4	SKU_WB_0501	600-10393-0501-100	P393 G92-850 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
5	SKU_DT_0004	600-10393-0004-100	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

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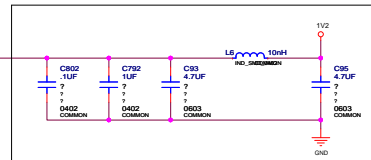
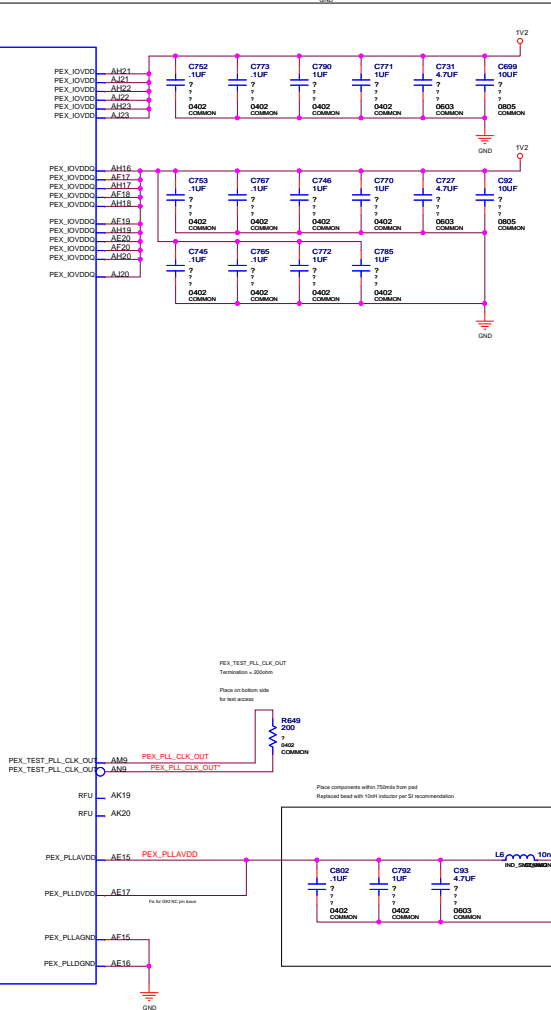
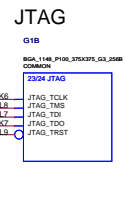
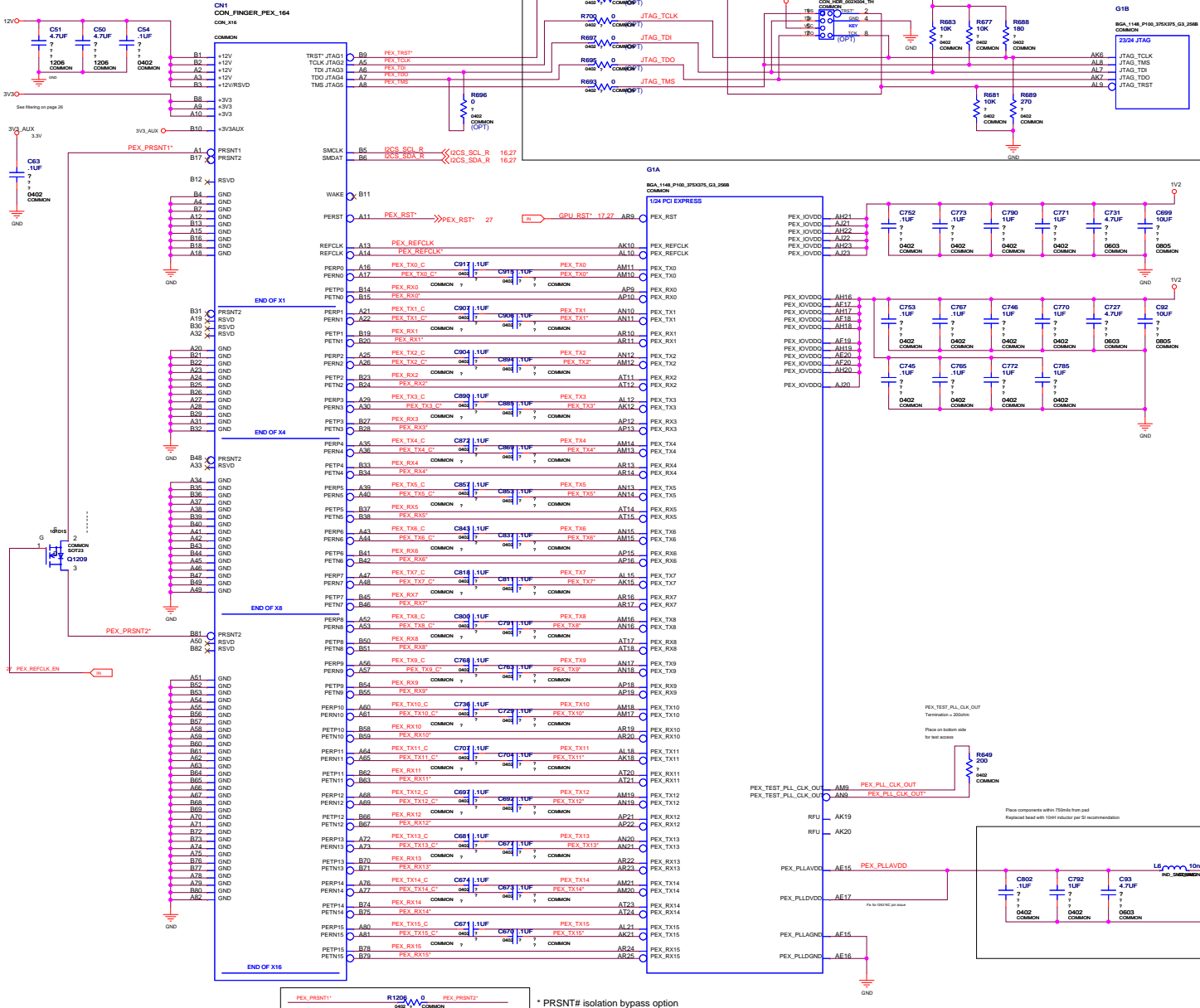


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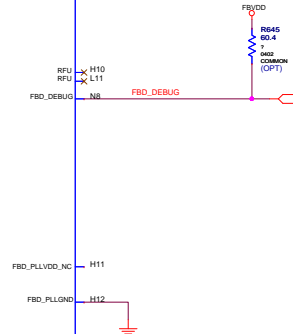
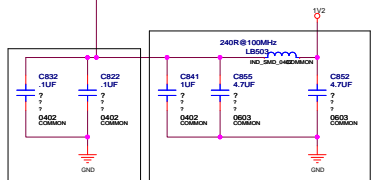
SUMMARY

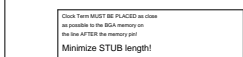
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Date: Thursday, May 26, 2006 Sheet: 1 of 27









Click Term **MUST BE PLACED** as close as possible to the SGA memory on the line **AFTER** the memory pin!

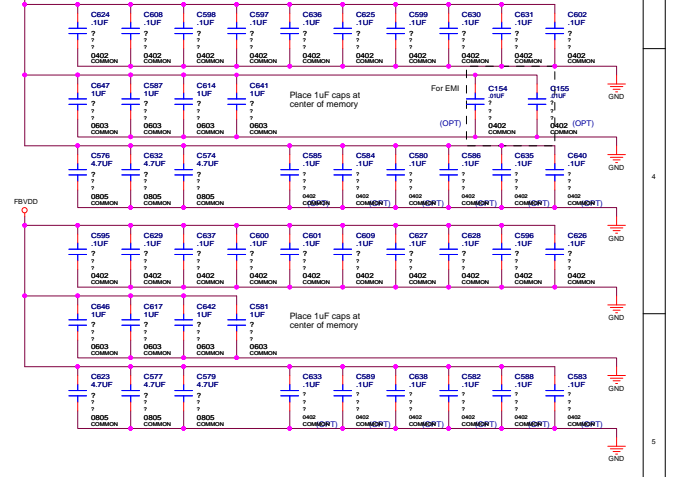
Minimize STUB length!

GDDR3: $V_{REF} = 0.70 \cdot FB/VDDQ$
 $1.41V = 2.0V \cdot 1.33K/(1549 + 1.33K)$

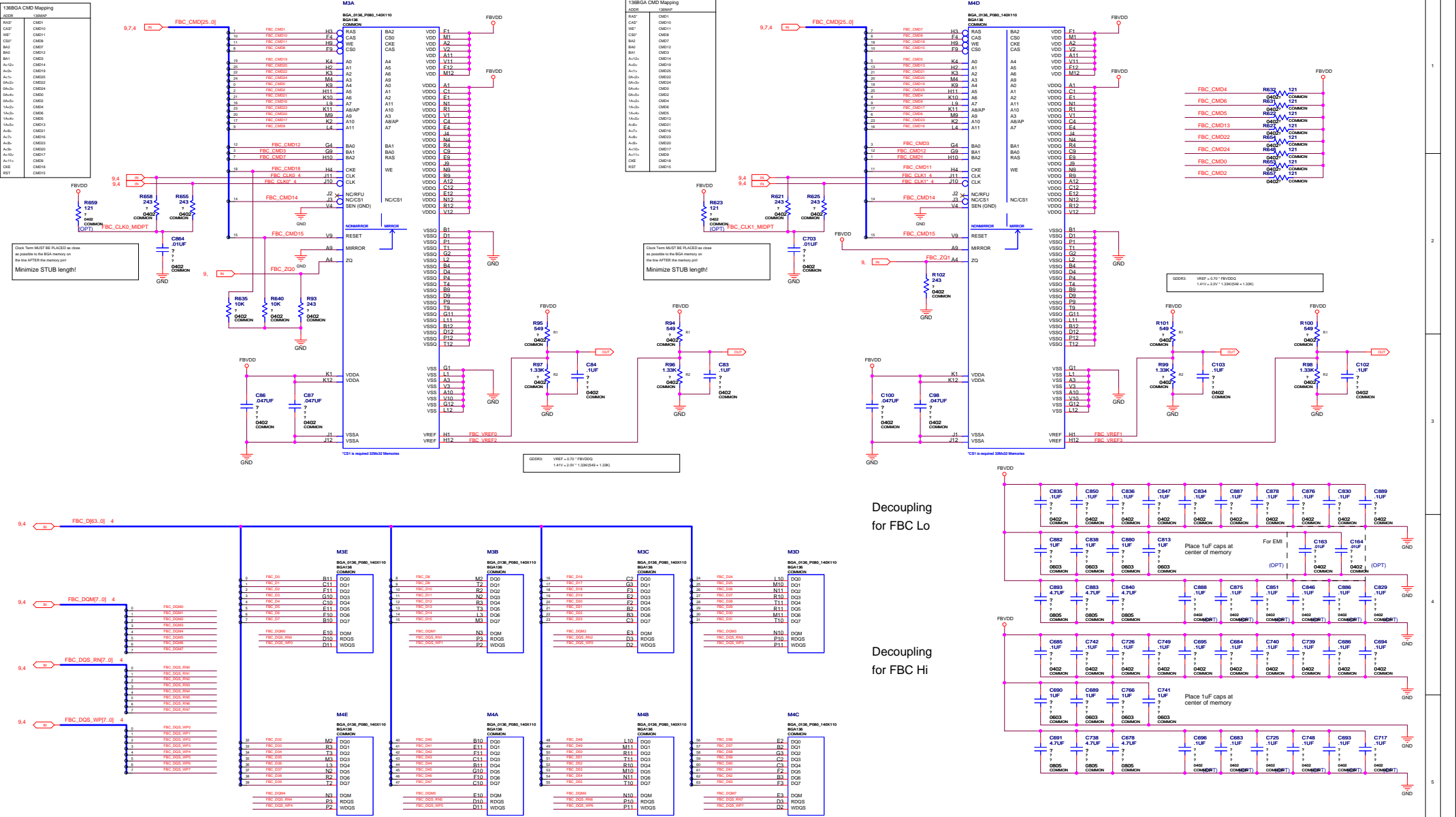
GDOR1: VREF = 0.70 * FBV(DOQ)
1.41V = 2.0V * 1.33K(549 + 1.33K)

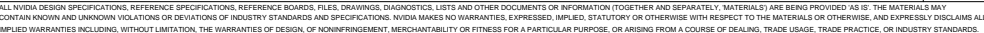
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138MGA CMD Mapping	138MGP
RAD	CM01
CAP	CM02
WE	CM03
CSP	CM04
BA2	CM05
BA1	CM06
BA0	CM07
BA3	CM08
BA4	CM09
BA5	CM10
BA6	CM11
BA7	CM12
BA8	CM13
BA9	CM14
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BA516	CM521





NET RULES for FrameBuffer A/B

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
OUT FBA_CLK0 3.5	1	800FF	FBA_CLK0
OUT FBA_CLK0P 3.5	1	800FF	FBA_CLK0
OUT FBA_CLK1 3.5	1	800FF	FBA_CLK1
OUT FBA_CLK1P 3.5	1	800FF	FBA_CLK1

OUT FBA_CMDS0 3.5	1	800H	
OUT FBA_CMDS0P 3.5	1	800H	
OUT FBA_CMDS1 3.5	1	800H	
OUT FBA_CMDS1P 3.5	1	800H	
OUT FBA_VIO 3.5	1	800H	

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
OUT FBB_CLK0 3.5	1	800FF	FBB_CLK0
OUT FBB_CLK0P 3.5	1	800FF	FBB_CLK0
OUT FBB_CLK1 3.5	1	800FF	FBB_CLK1
OUT FBB_CLK1P 3.5	1	800FF	FBB_CLK1

OUT FBB_CMDS0 3.5	1	800H	
OUT FBB_CMDS0P 3.5	1	800H	
OUT FBB_CMDS1 3.5	1	800H	
OUT FBB_CMDS1P 3.5	1	800H	
OUT FBB_VIO 3.5	1	800H	

OUT FBA_DEVID 3	1	800H	
OUT FBB_DEVID 3	1	800H	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
OUT FBAB_PLAVDD 3	1.2V	0.02A	12MIL
OUT FBA_VREF0 5	1.40V	0.02A	12MIL
OUT FBA_VREF1 5	1.40V	0.02A	12MIL
OUT FBA_VREF2 5	1.40V	0.02A	12MIL
OUT FBA_VREF3 5	1.40V	0.02A	12MIL
OUT FBA_Z00 5	2.0V	0.02A	12MIL
OUT FBA_Z01 5	2.0V	0.02A	12MIL

OUT FBB_VREF0 5	1.40V	0.02A	12MIL
OUT FBB_VREF1 5	1.40V	0.02A	12MIL
OUT FBB_VREF2 5	1.40V	0.02A	12MIL
OUT FBB_VREF3 5	1.40V	0.02A	12MIL
OUT FBB_Z00 5	2.0V	0.02A	12MIL
OUT FBB_Z01 5	2.0V	0.02A	12MIL

OUT FB_VREF1 3	1.40V	0.02A	12MIL
OUT FB_VREF2 3	1.40V	0.02A	12MIL

NET RULES for FrameBuffer C/D

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
OUT FBC_CLK0 4.7	1	800FF	FBC_CLK0
OUT FBC_CLK0P 4.7	1	800FF	FBC_CLK0
OUT FBC_CLK1 4.7	1	800FF	FBC_CLK1
OUT FBC_CLK1P 4.7	1	800FF	FBC_CLK1

OUT FBC_CMDS0 4.7	1	800H	
OUT FBC_CMDS0P 4.7	1	800H	
OUT FBC_CMDS1 4.7	1	800H	
OUT FBC_CMDS1P 4.7	1	800H	
OUT FBC_VIO 4.7	1	800H	

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
OUT FBD_CLK0 4.8	1	800FF	FBD_CLK0
OUT FBD_CLK0P 4.8	1	800FF	FBD_CLK0
OUT FBD_CLK1 4.8	1	800FF	FBD_CLK1
OUT FBD_CLK1P 4.8	1	800FF	FBD_CLK1

OUT FBD_CMDS0 4.8	1	800H	
OUT FBD_CMDS0P 4.8	1	800H	
OUT FBD_CMDS1 4.8	1	800H	
OUT FBD_CMDS1P 4.8	1	800H	
OUT FBD_VIO 4.8	1	800H	

OUT FBC_DEVID 4	1	800H	
OUT FBD_DEVID 4	1	800H	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
OUT FBBD_PLAVDD 4	1.2V	0.02A	12MIL
OUT FBC_VREF0 7	1.40V	0.02A	12MIL
OUT FBC_VREF1 7	1.40V	0.02A	12MIL
OUT FBC_VREF2 7	1.40V	0.02A	12MIL
OUT FBC_VREF3 7	1.40V	0.02A	12MIL
OUT FBC_Z00 7	2.0V	0.02A	12MIL
OUT FBC_Z01 7	2.0V	0.02A	12MIL

OUT FBD_VREF0 8	1.40V	0.02A	12MIL
OUT FBD_VREF1 8	1.40V	0.02A	12MIL
OUT FBD_VREF2 8	1.40V	0.02A	12MIL
OUT FBD_VREF3 8	1.40V	0.02A	12MIL
OUT FBD_Z00 8	2.0V	0.02A	12MIL
OUT FBD_Z01 8	2.0V	0.02A	12MIL

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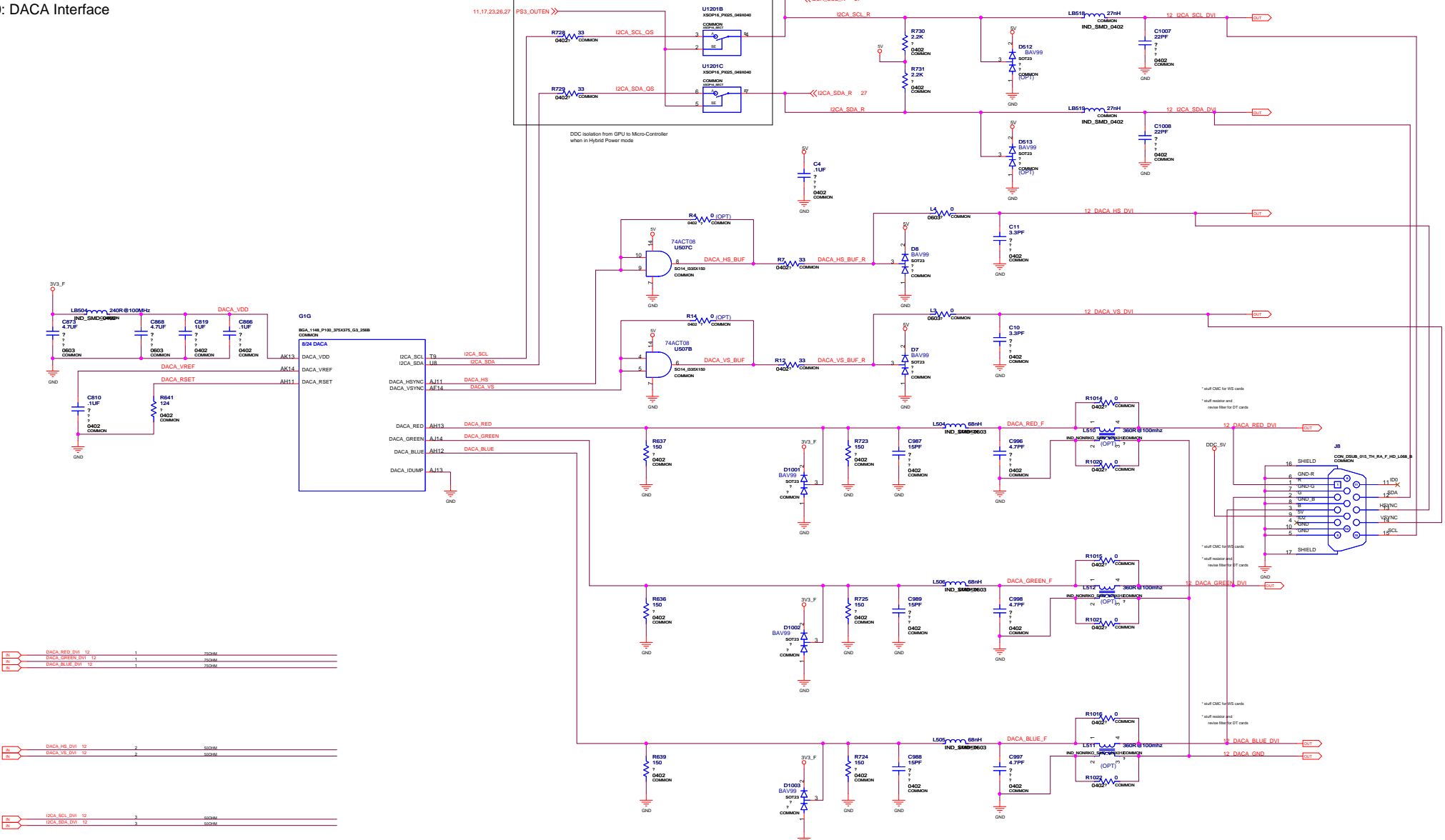
ASSEMBLY PAGE DETAIL P303 - BASE LTRC GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL FrameBuffer Net Rules



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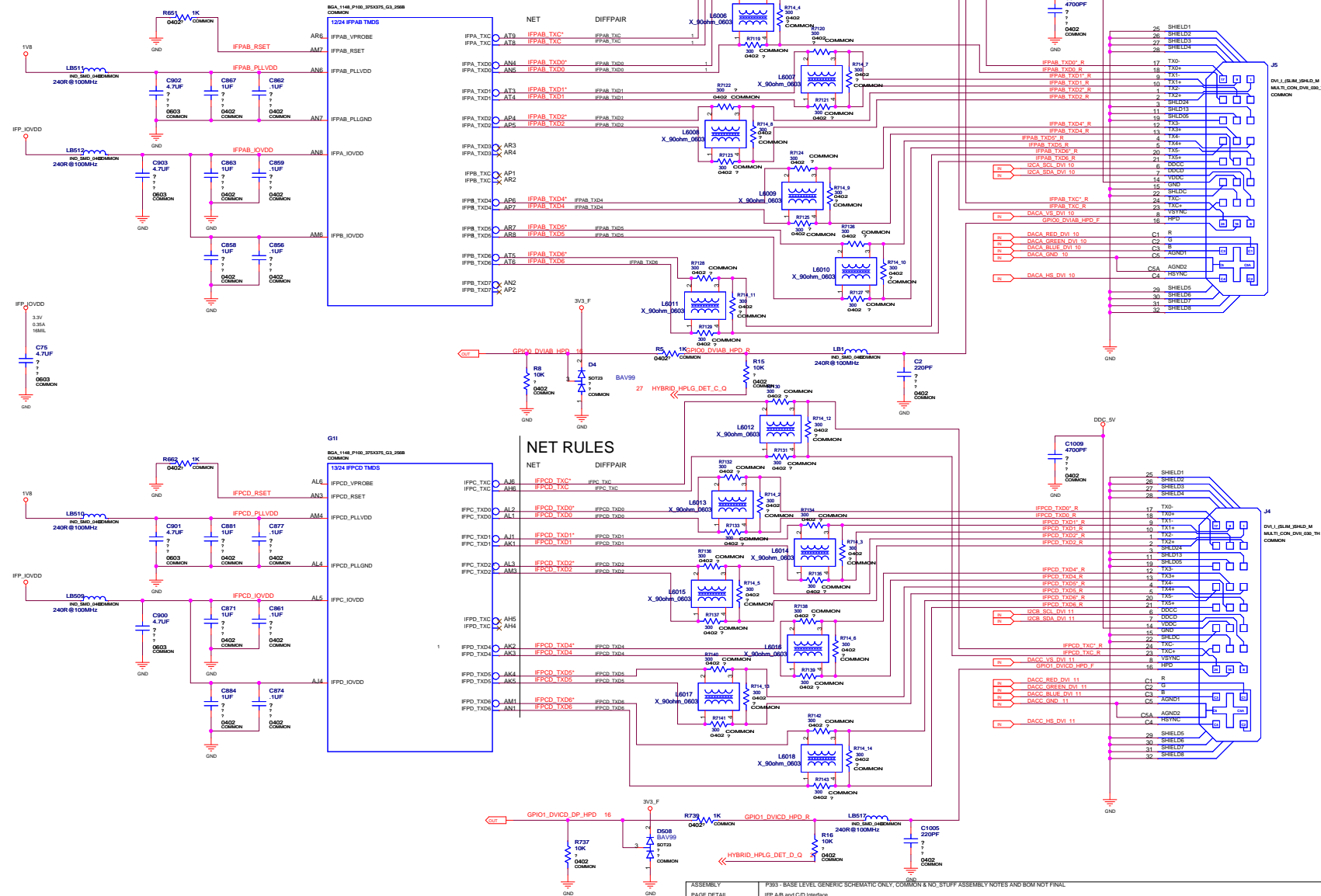
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ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DAGA Interface






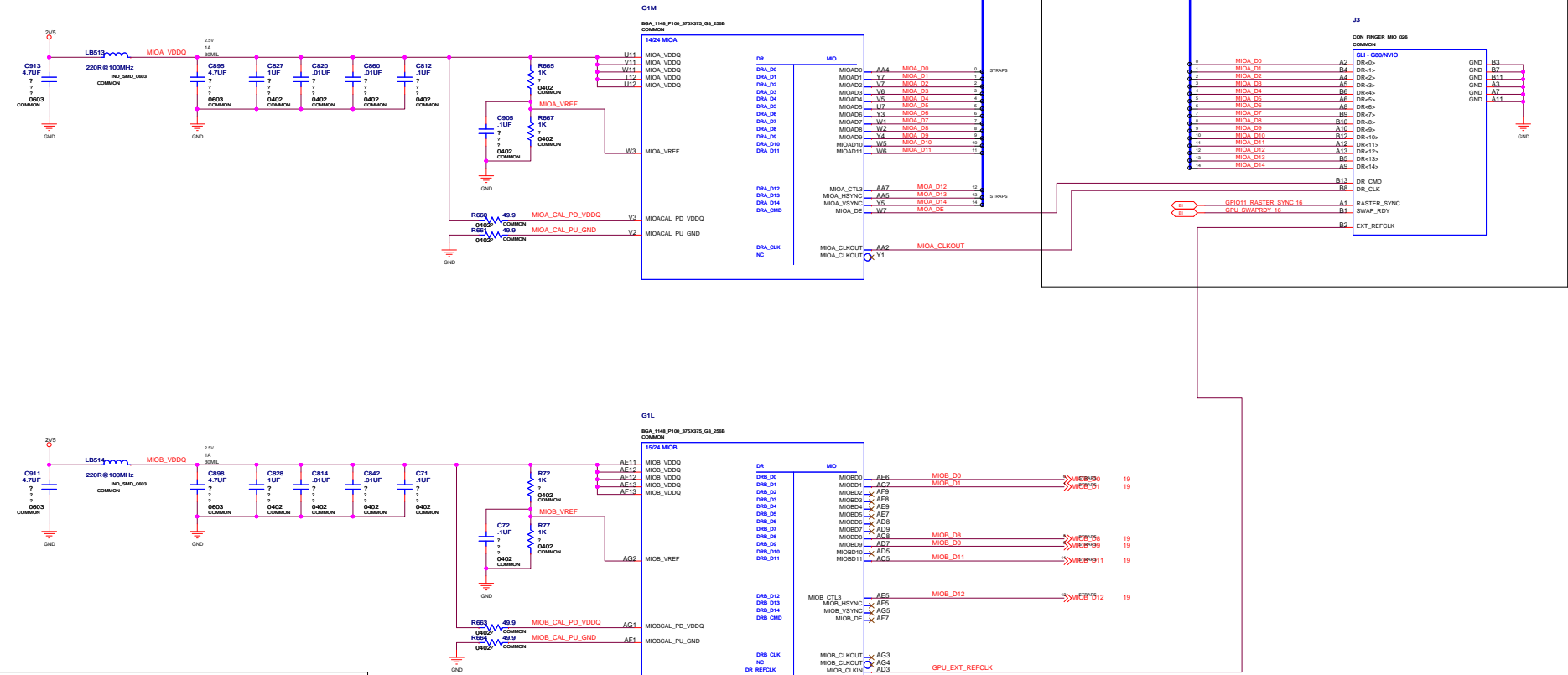
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ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB and Stereo Interface

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	DACB and Stereo Interface		
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MIO Feature Connector




MIO NET RULES



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ASSEMBLY PAGE DETAIL P301 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL Multi-use IO(MIO) Interface



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Multi-use IO(MIO) Interface
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Control

Page15: Display Port (Analogix ANX9802/ANX9805)

* DDC keepers circuit removed

* ANX9805 support

pin 76 - GPIO3 to DP mode, from pin 13, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 74 - GPIO2, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 73 - DDC support via I2C and pull-up, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 71 - SPOUT1 - tie to GND, input select 01 through internal register

pin 70 - SPOUT0 - support for Audio input, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 68 - NC - tie to GND

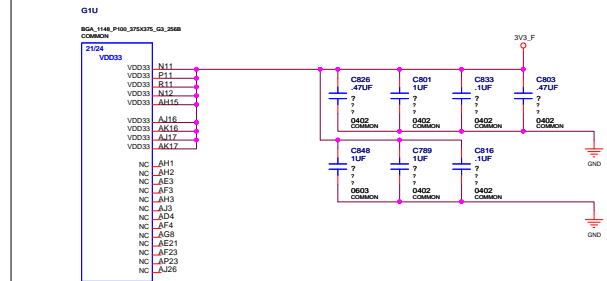
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PAGE DETAIL	Display Port

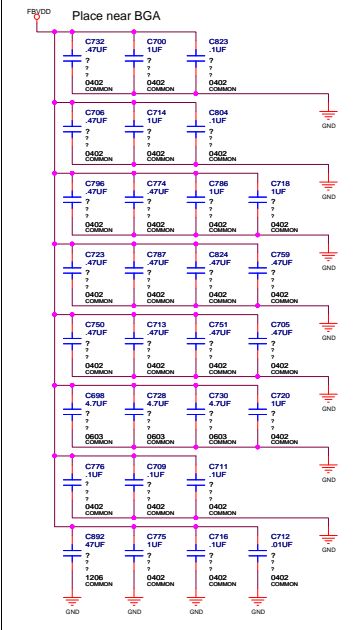


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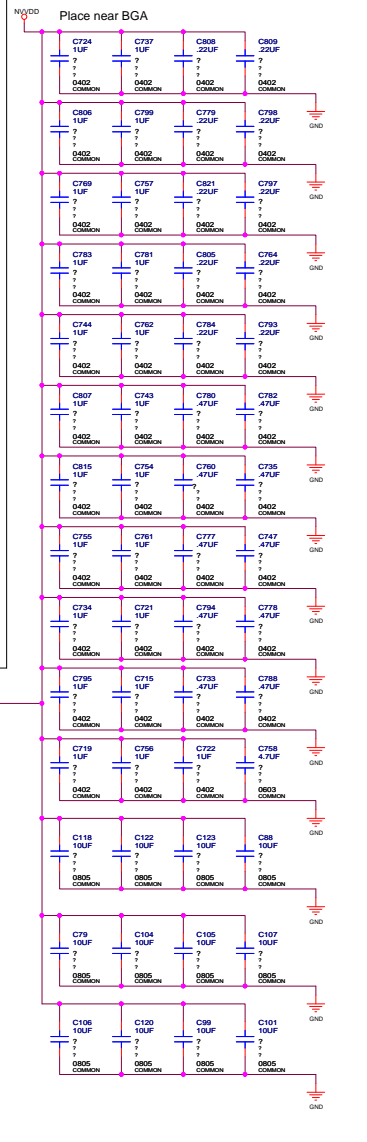
VDD33



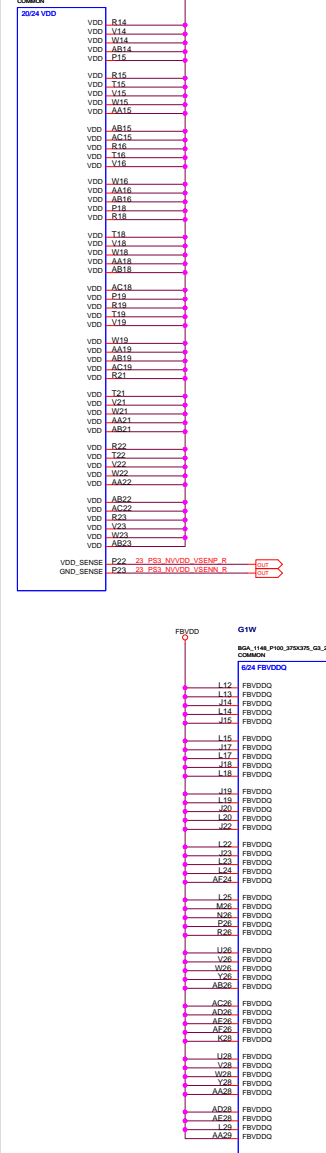
FBVDDQ



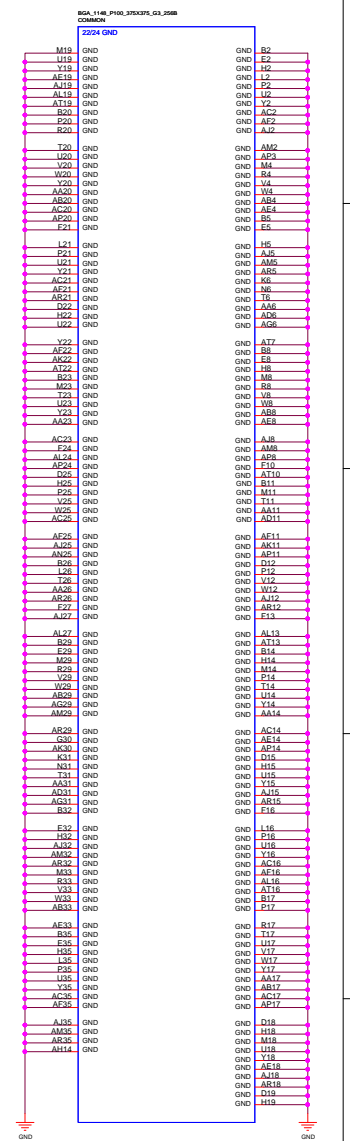
NVVDD



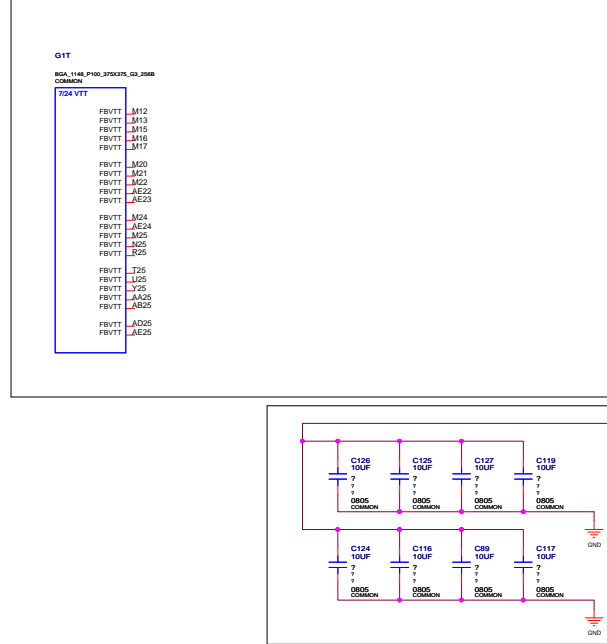
G1V



G1X



FBVTT



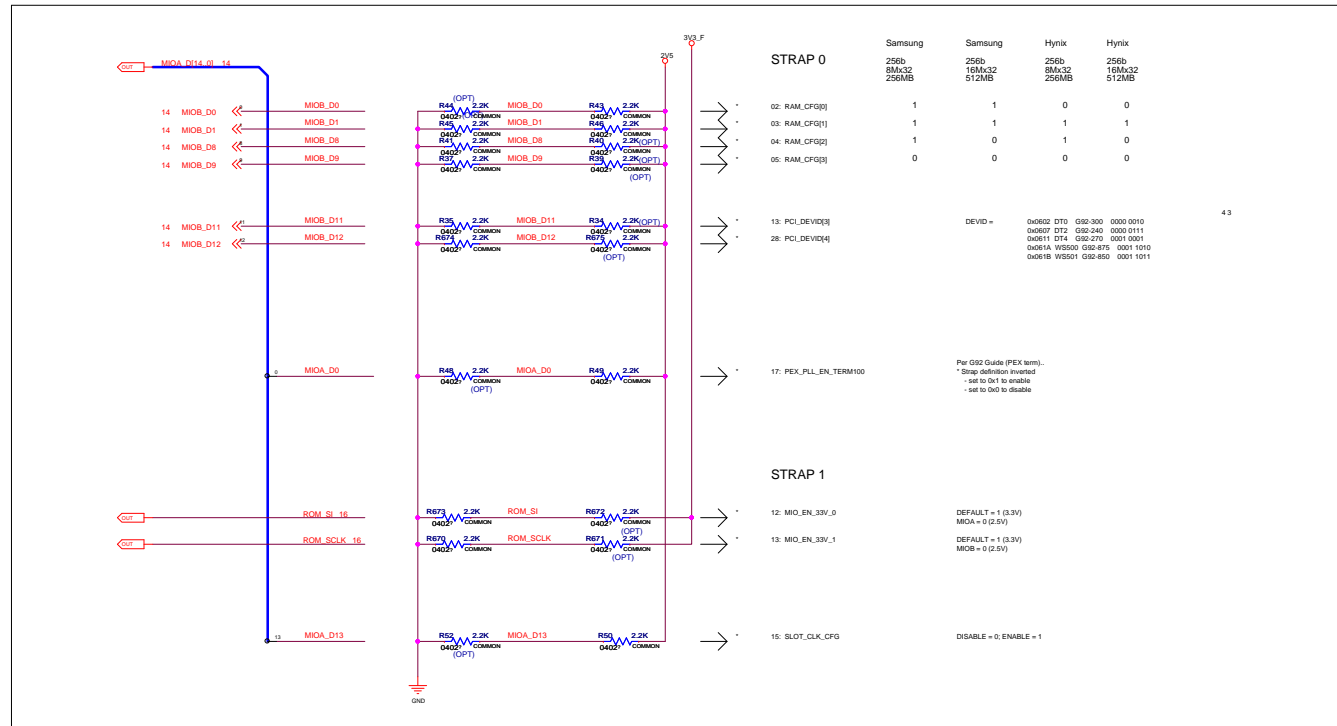
NET	INV_CRITICAL	INV_IMPEDANCE	DIFFPAIR
P03_NVDD_SENSE_P_23	1	60000	NOVDD_SENSE
P03_NVDD_SENSE_N_23	1	60000	NOVDD_SENSE

ASSEMBLY
PAGE DETAIL
P03 - BASE LAYER GENERIC SCHEMATIC ONLY; COMMON & NO-STOP ASSEMBLY NOTES AND BOM NOT FINAL
Power/GND and Decoupling

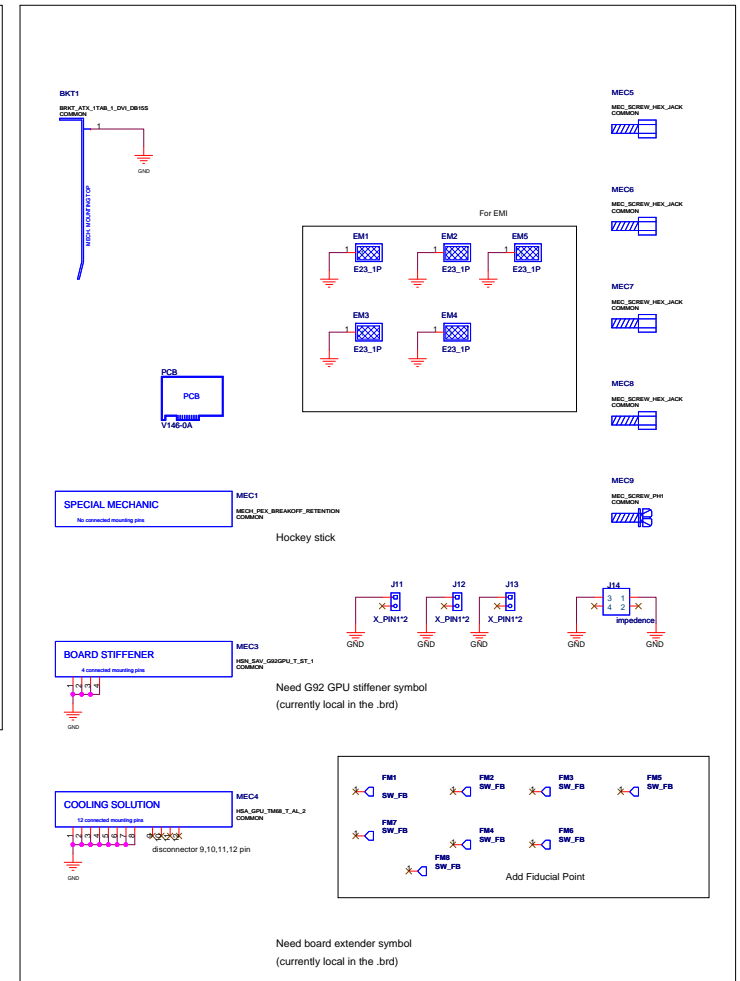
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Power/GND and Decoupling
Size: Custom
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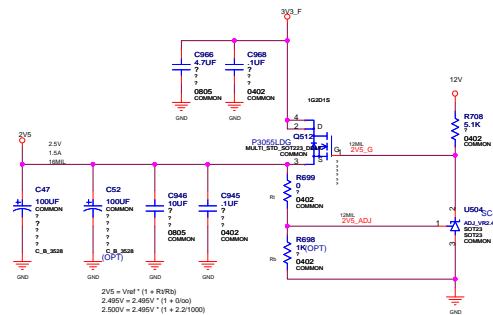
STRAPS



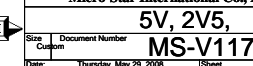
MECHANICAL



2V5 Supply


$$\begin{aligned} 2V_5 &= V_{ref} * (1 + R_t/R_b) \\ 2.495V &= 2.495V * (1 + 0/\infty) \\ 2.500V &= 2.495V * (1 + 2.2/1000) \end{aligned}$$

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 5V, STEREO_5V, 2V5, DP_PWR





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ASSEMBLY	P303 - BASE LUTIC GENERIC SCHEMATIC ONLY, COMMON & NO STOPP ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 1 & 2



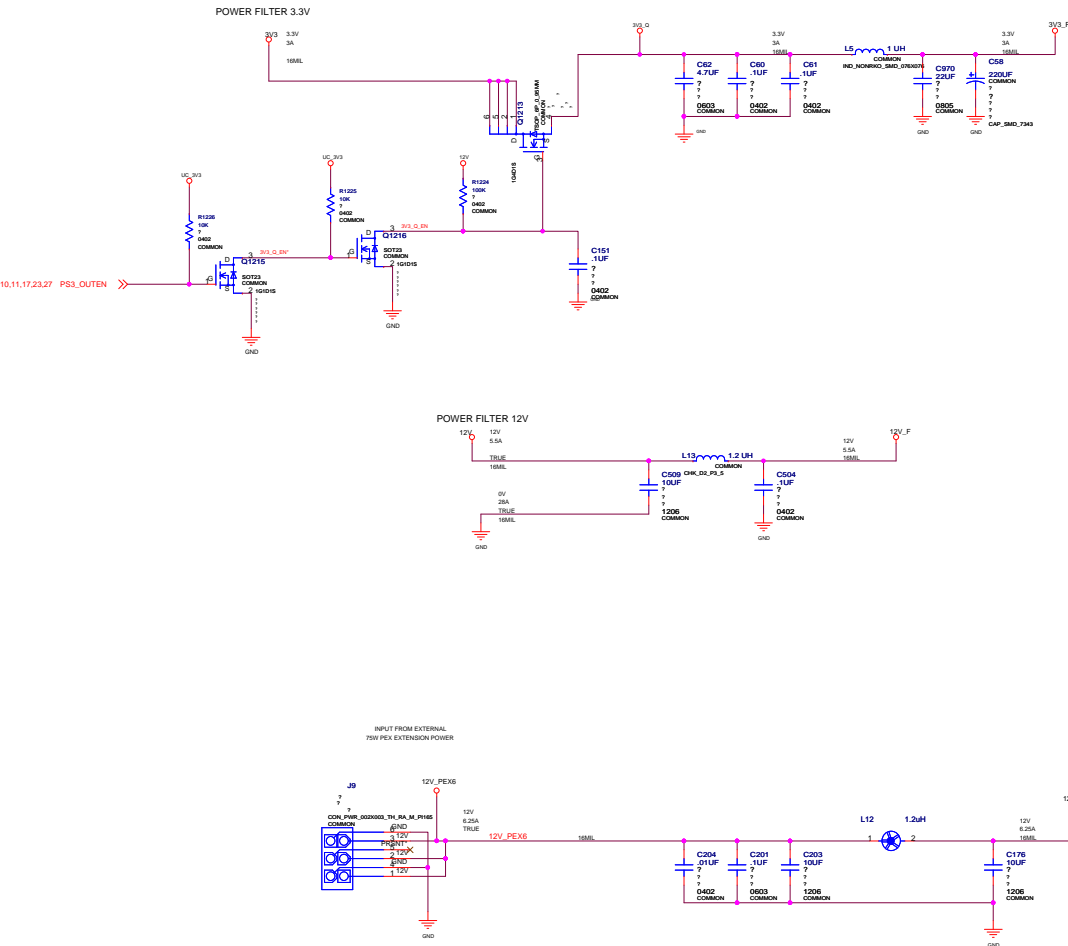
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ASSEMBLY
PAGE DETAIL
P303 - BASE LUTIC GENERIC SCHEMATIC ONLY, COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Power Supply: NVVDD Phase 3



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ASSEMBLY PAGE DETAIL P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_3TUFF ASSEMBLY NOTES AND BOM NOT FINAL Power Supply: Filter/Detection of 3V3, 12V, 12V_PEX



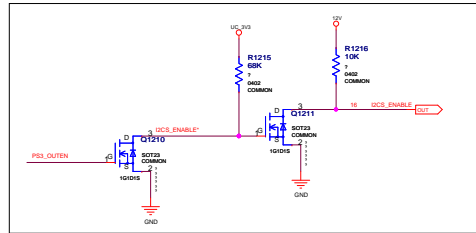
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3V3,12V,12V_PEX

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ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: Hybrid Power