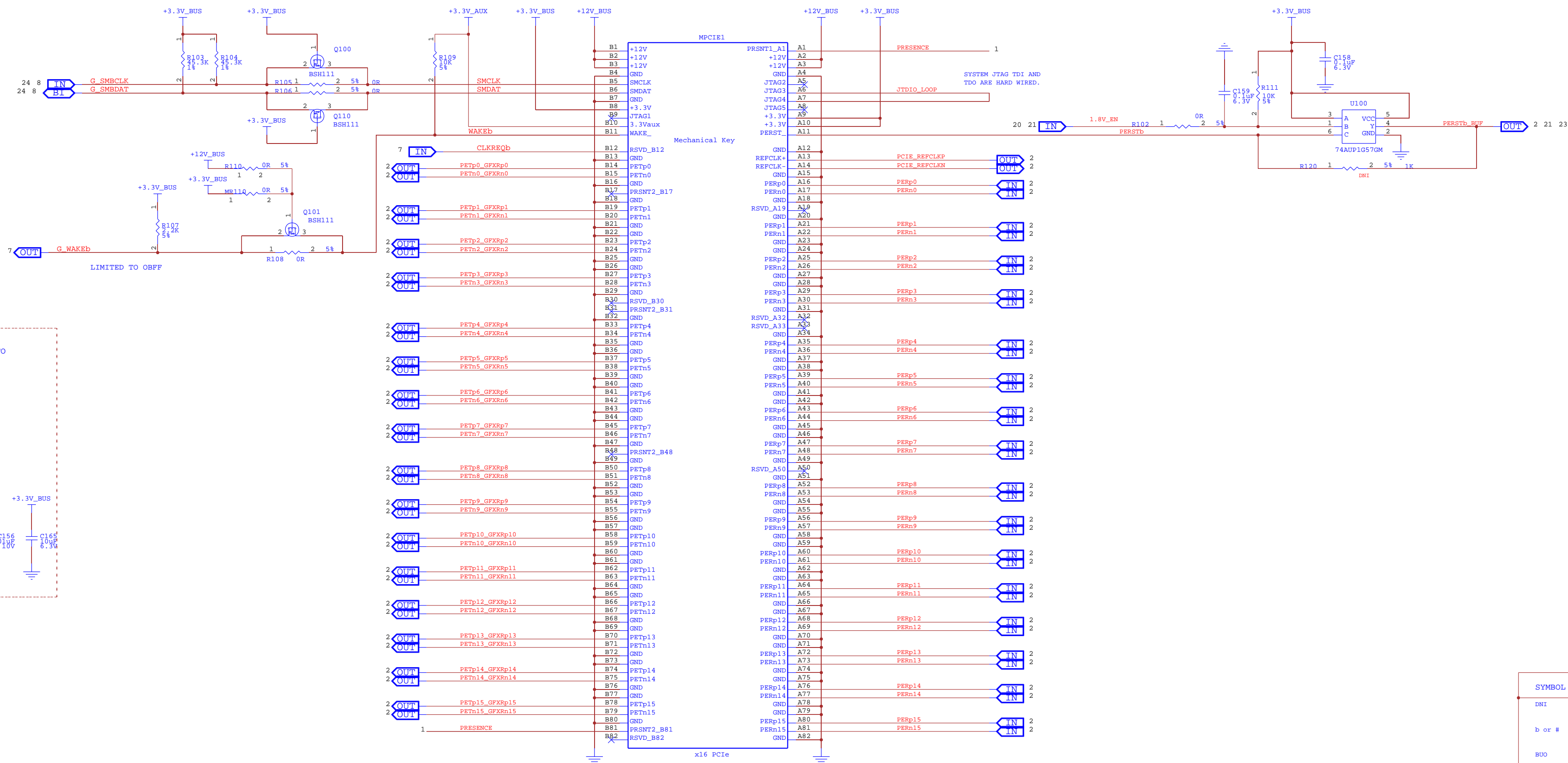


(1) PCI-EXPRESS EDGE CONNECTOR



AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: PCIE EDGE CONNECTOR

DATE: Wed Mar 23 13:12:19 2016

REV: 1.0

SHEET NUMBER: 1 OF 26

TITLE:

DOCUMENT NUMBER: 105_CXXX00_00A

TITLE

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D

C

B

A

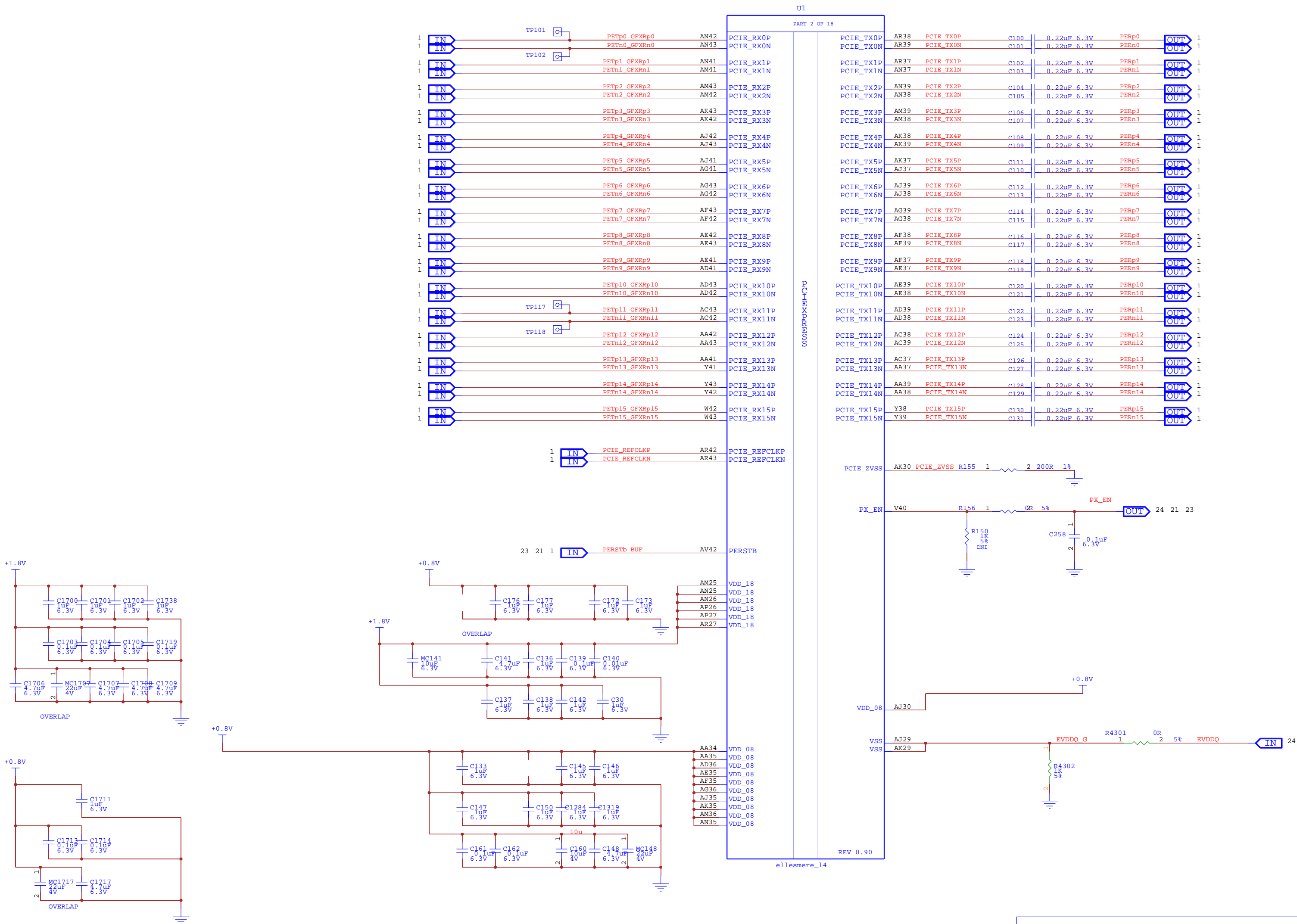
D

C

B

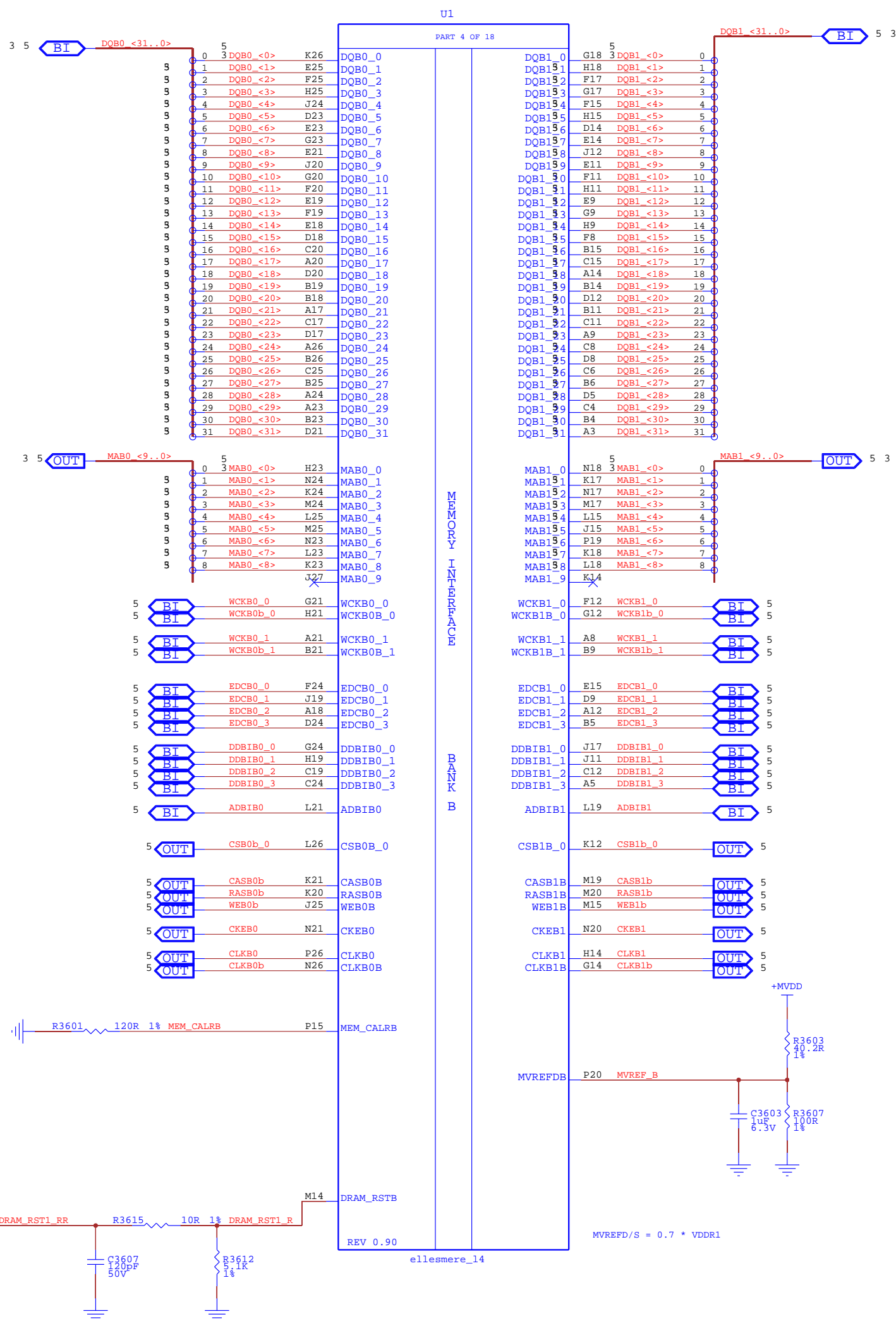
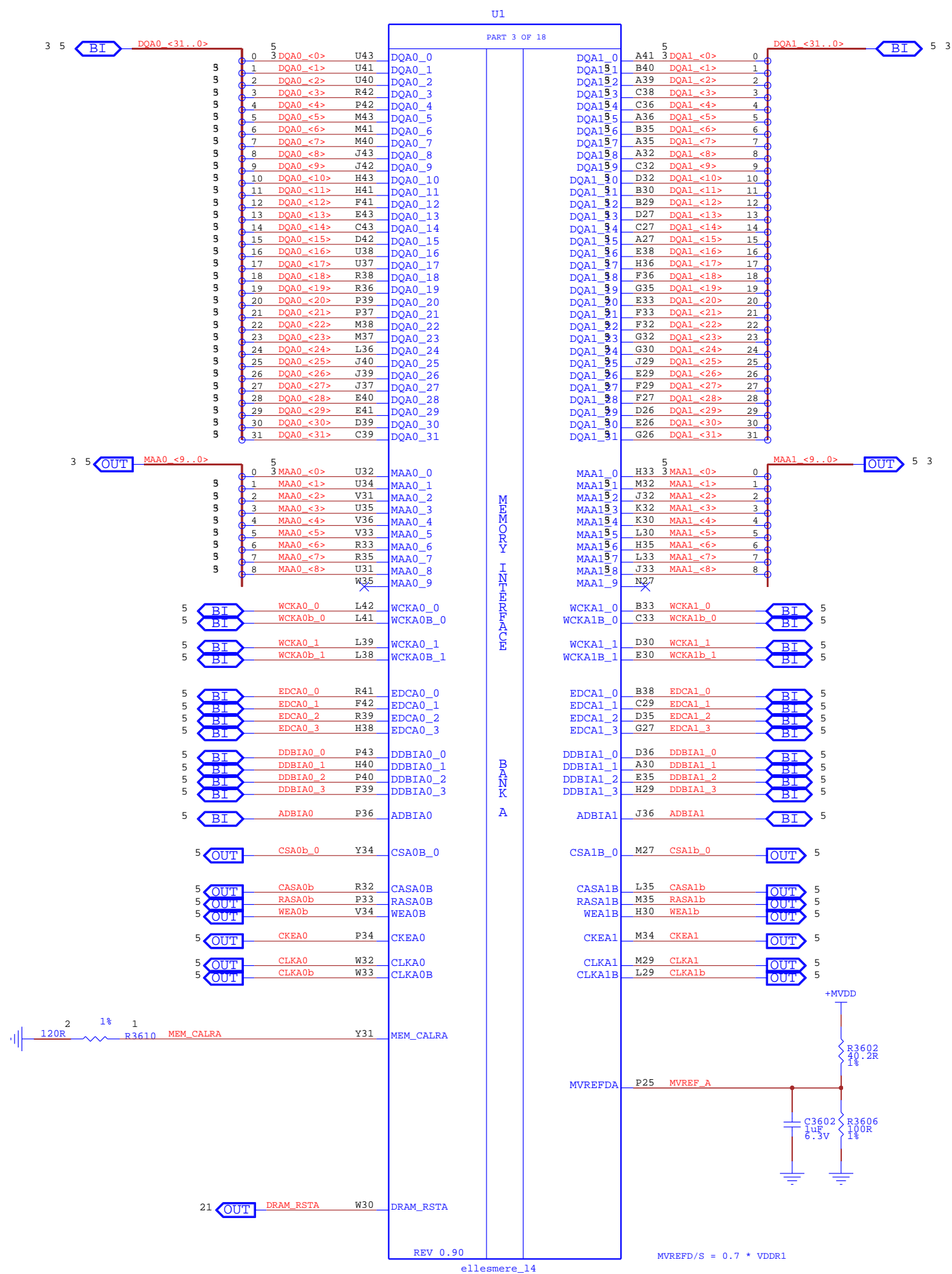
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(2) ELLESMERE PCIE INTERFACE

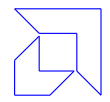


| | | | |
|---|----------|--|--|
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| SHEET: ELLESMERE PCIE INTERFACE | | TITLE: | |
| DATE: Wed Mar 23 13:12:24 2016 | REV: 1.0 | TITLE | |
| SHEET NUMBER: 2 OF 26 | | | |
| DOCUMENT NUMBER: 105_CXXX00_00A | | | |

(3) ELLESMERE MEM INTERFACE CH A/B



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SHEET: ELLESMERE MEM CH AB

DATE: Wed Mar 23 13:12:25 2016

REV: 1.0

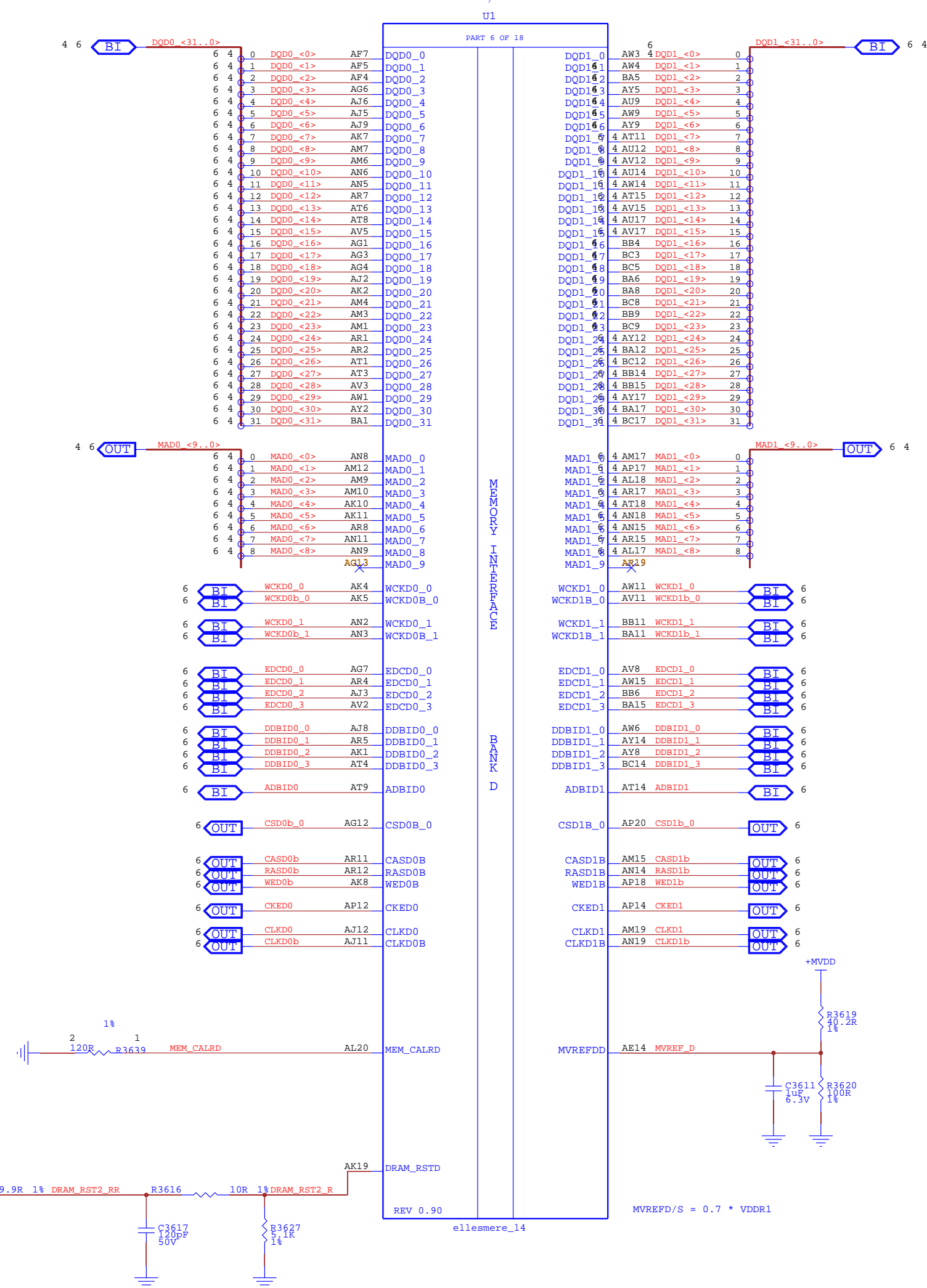
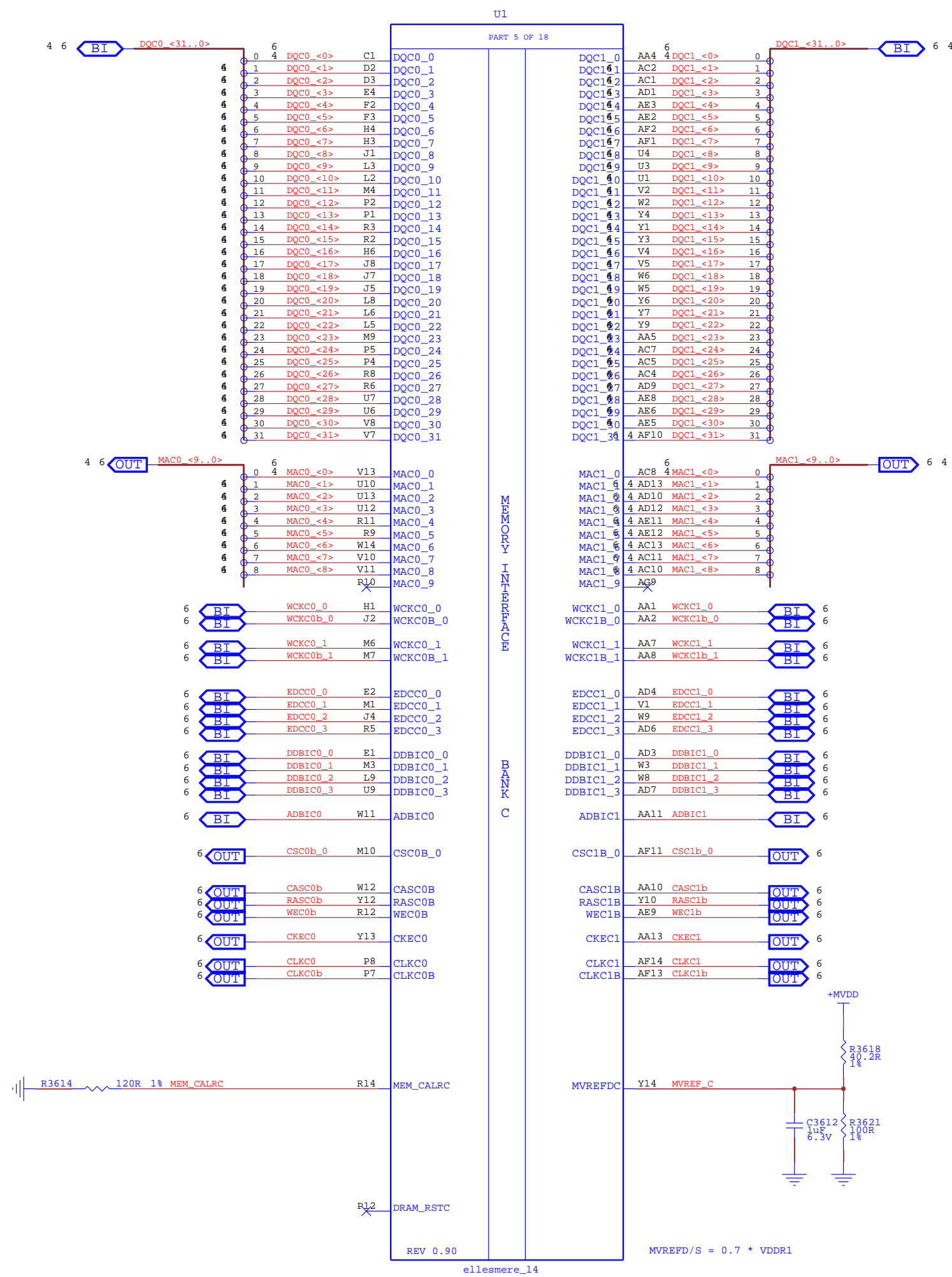
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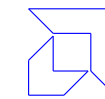
DOCUMENT NUMBER: 105_CXXX00_00A

TITLE

(4) ELLESMERE MEM INTERFACE CH C/D



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SHEET: ELLESMERE MEM CH CD

DATE: Wed Mar 23 13:12:26 2016

REV: 1.0

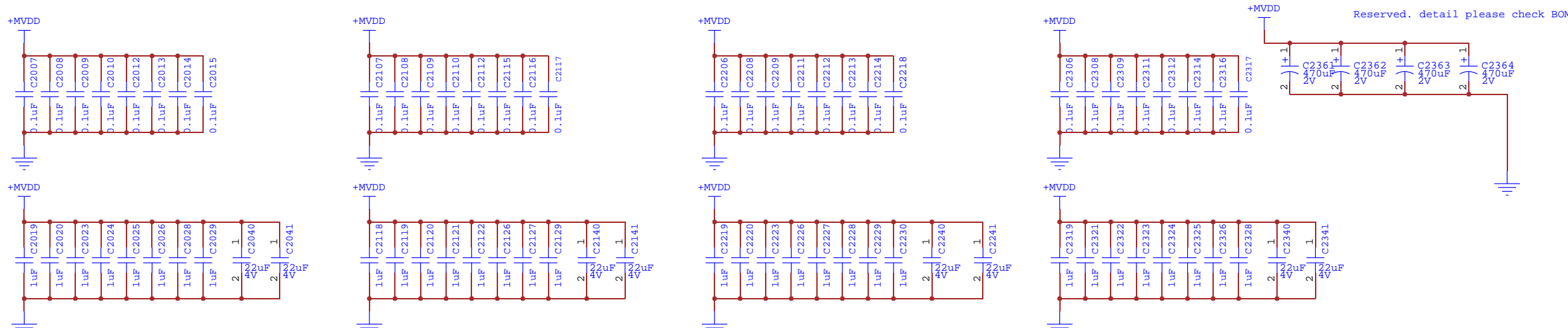
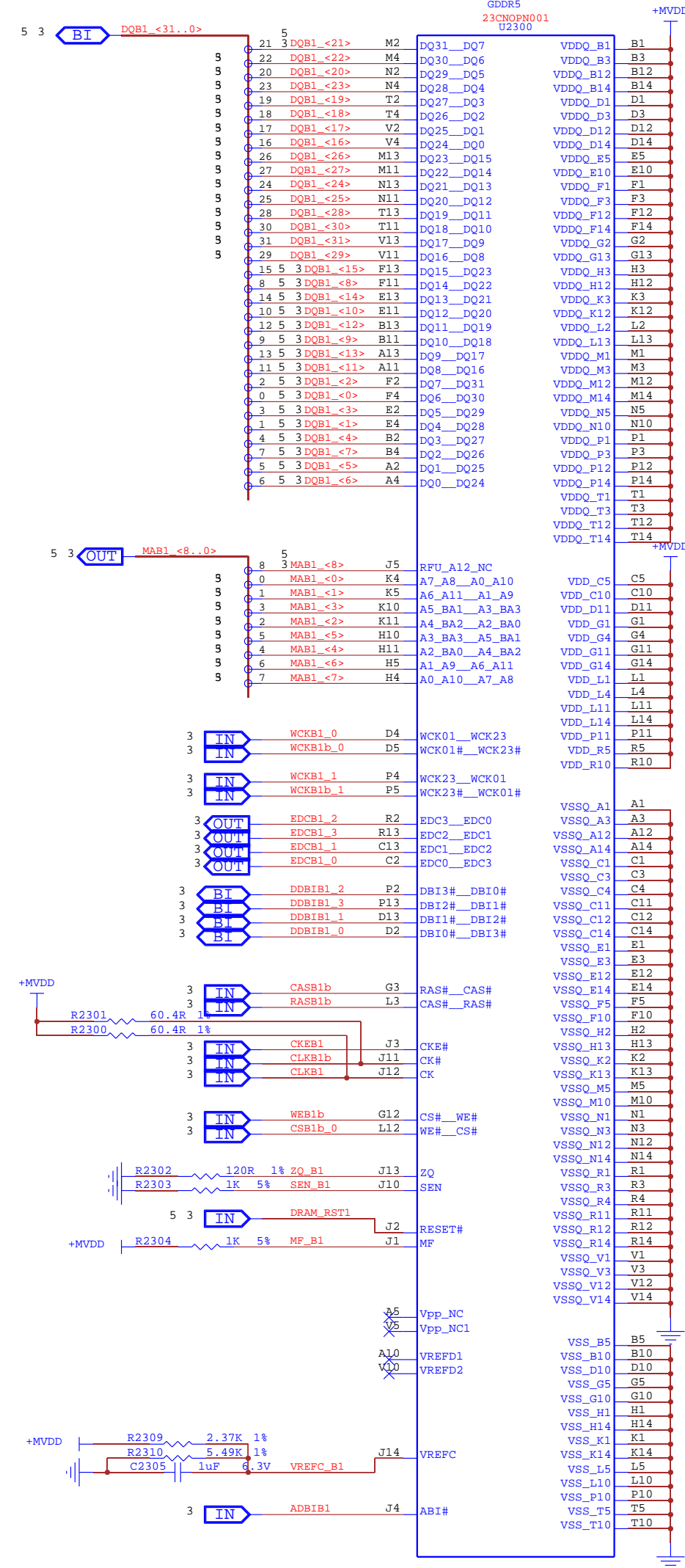
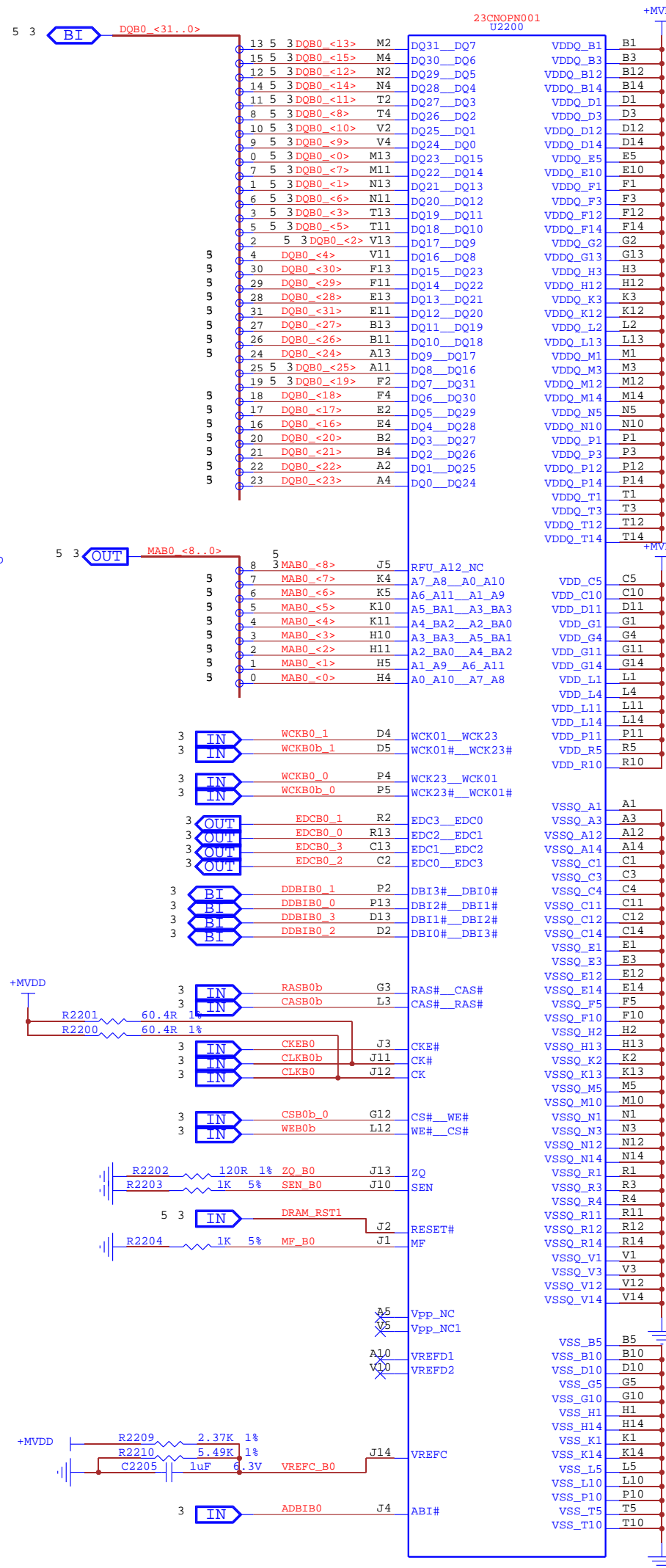
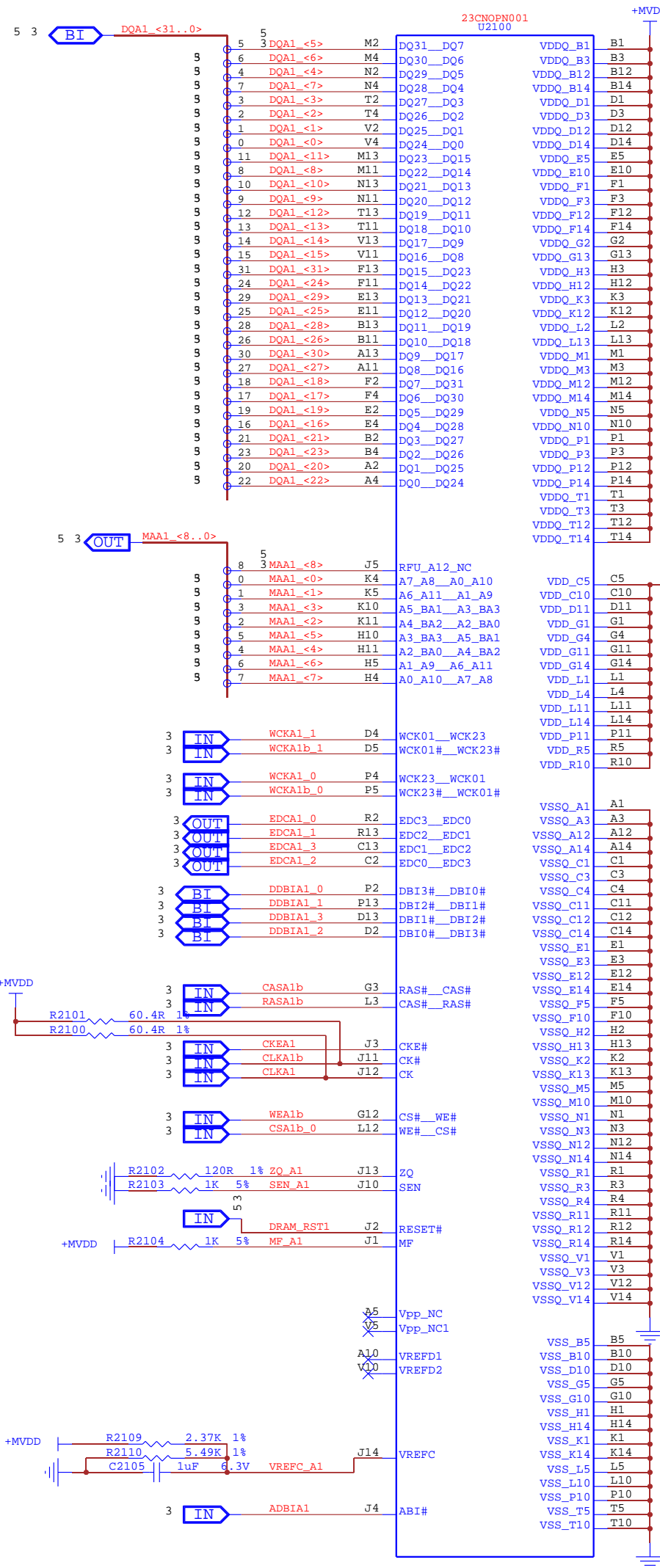
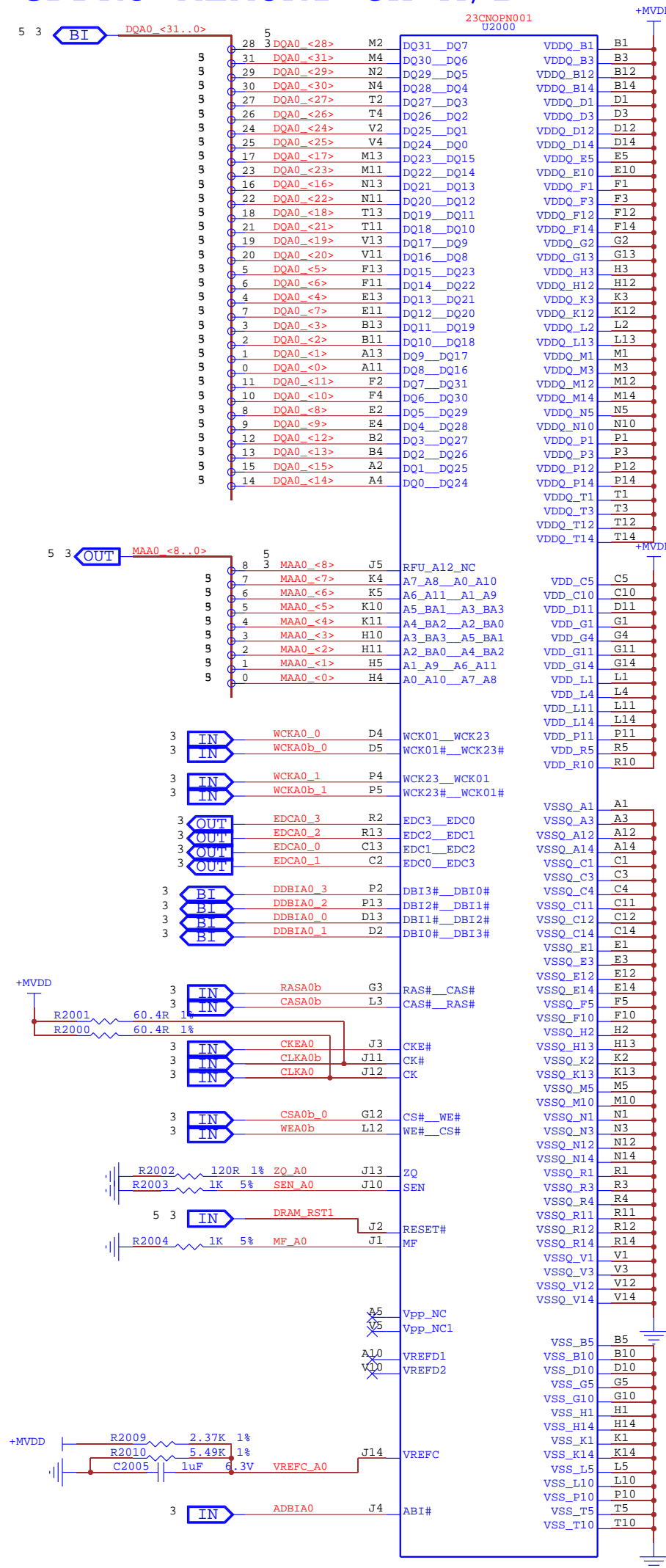
SHEET NUMBER: 4 OF 26

TITLE:

DOCUMENT NUMBER: 105_CXXX00_00A

TITLE

(5) GDDR5 MEMORY CH A/B



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SHANGHAI, CHINA 201203

SHEET: GDDR5 MEM CH AB

DATE: Wed Mar 23 13:12:27 2016

SHEET NUMBER: 5 OF 26

DOCUMENT NUMBER: 105_CXXX00_00A

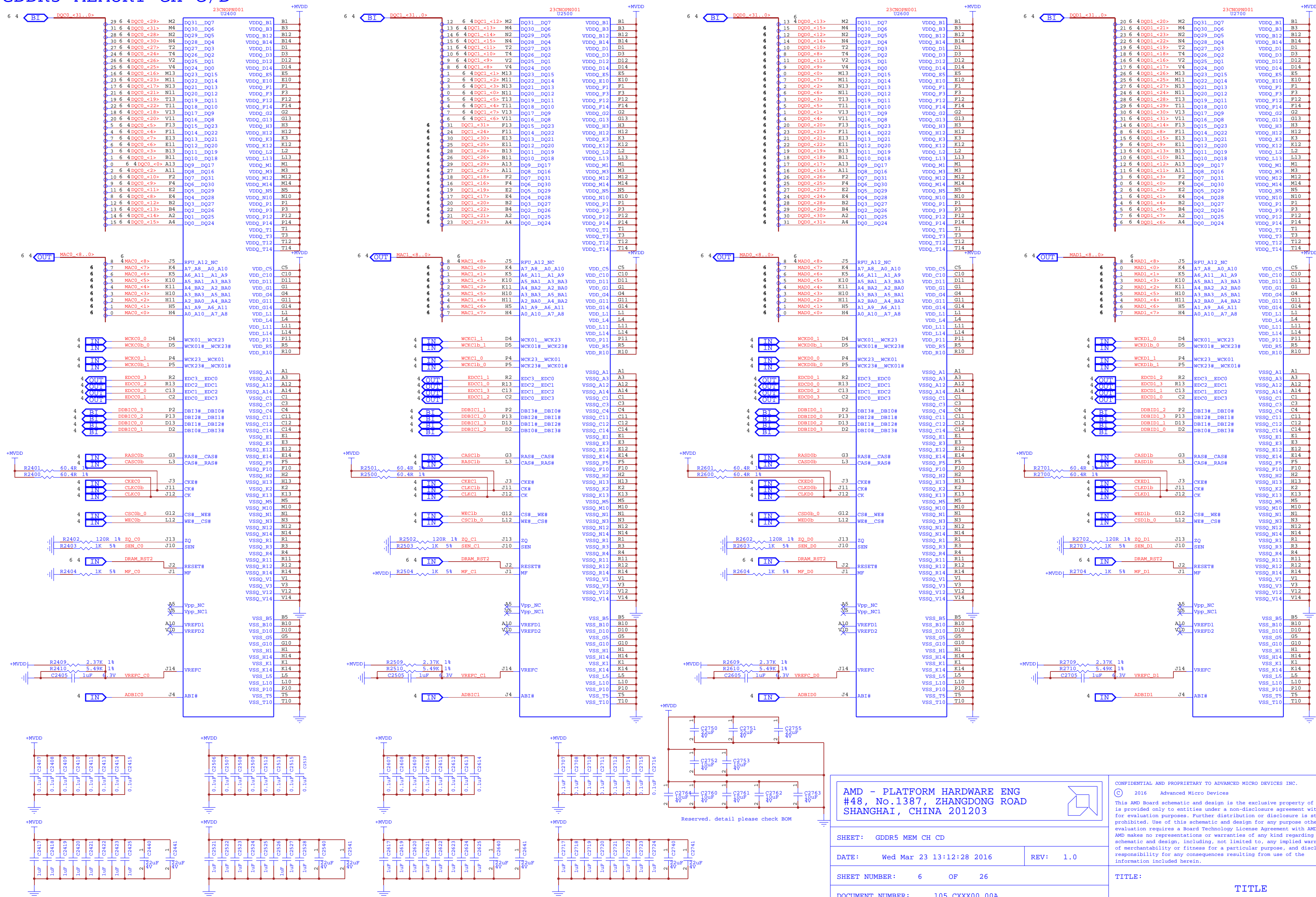
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TITLE

(6) GDDR5 MEMORY CH C/D



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SHEET: GDDR5 MEM CH CD

DATE: Wed Mar 23 13:12:28 2016

SHEET NUMBER: 6 OF 26

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TITLE:

TITLE

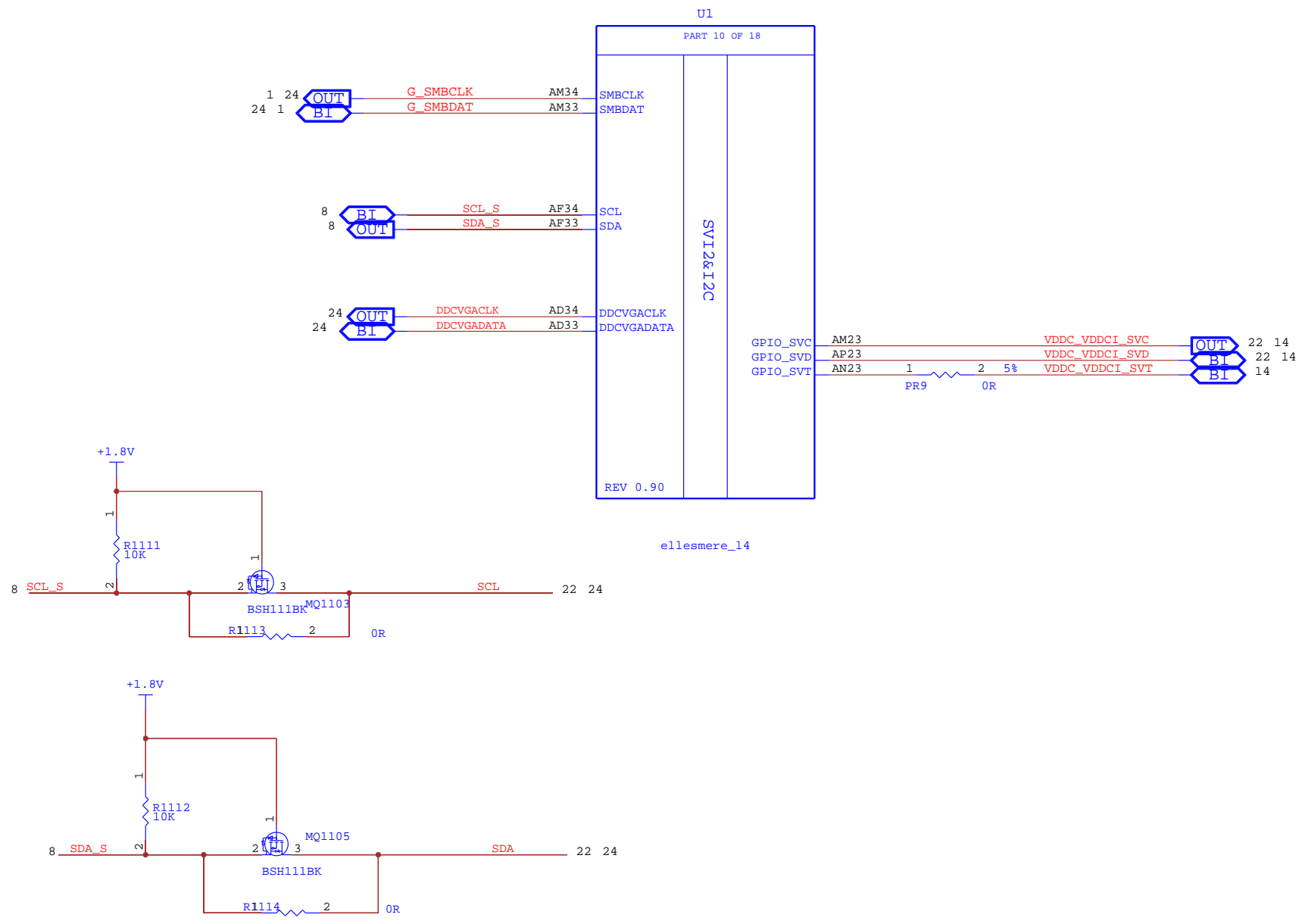
D



A

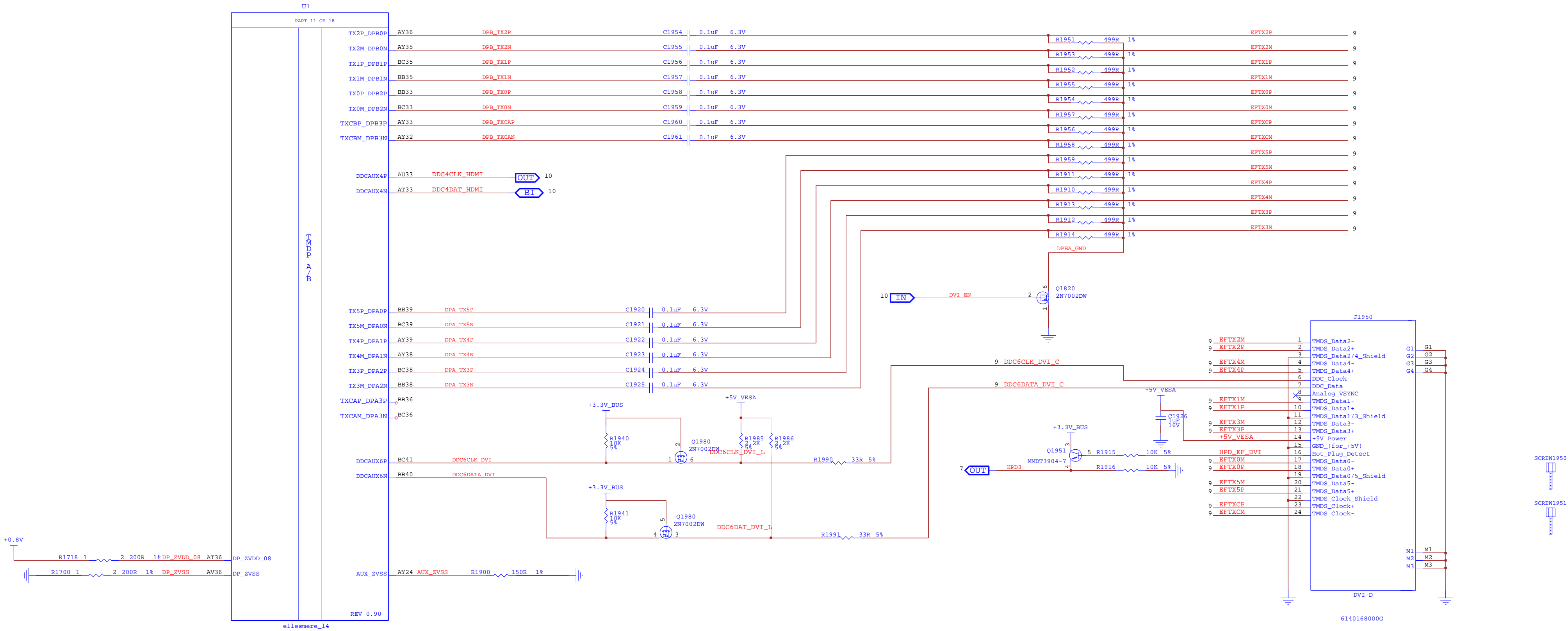
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(8) ELLESMERE DAC1 LOCK

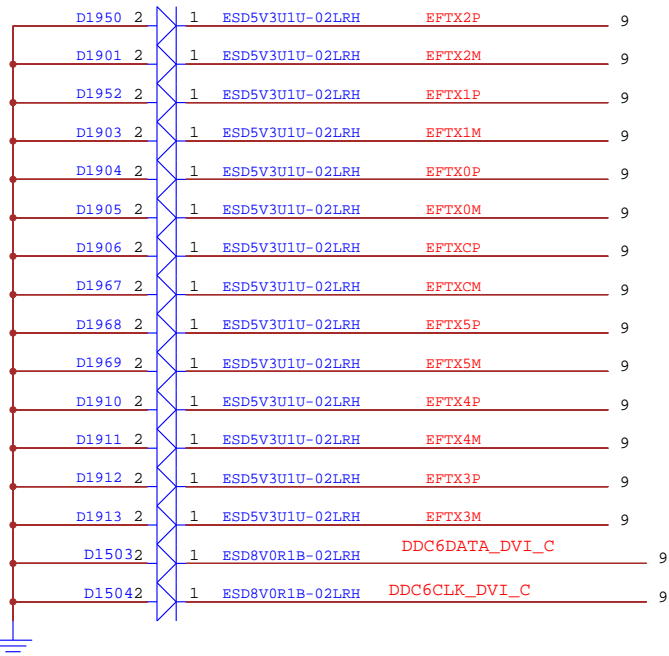


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| SHEET: ELLESMERE SV12&I2C | | | |
| DATE: Wed Mar 23 13:12:20 2016 | | REV: 1.0 | |
| SHEET NUMBER: 8 OF 26 | | TITLE: | |
| DOCUMENT NUMBER: 105_CXXX00_00A | | TITLE | |

(9) ELLESMERE TMDP A/B



OPTIONAL ESD PROTECTION DIODES



| | | | |
|---|----------|--|--|
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| SHEET: ELLESMERE TMDPAB dDVI | | TITLE: | |
| DATE: Wed Mar 23 13:12:20 2016 | REV: 1.0 | TITLE | |
| SHEET NUMBER: 9 OF 26 | | | |
| DOCUMENT NUMBER: 105_CXXX00_00A | | | |

D



A



SHEET:

DATE: Wed Mar 23 13:12:19 2016

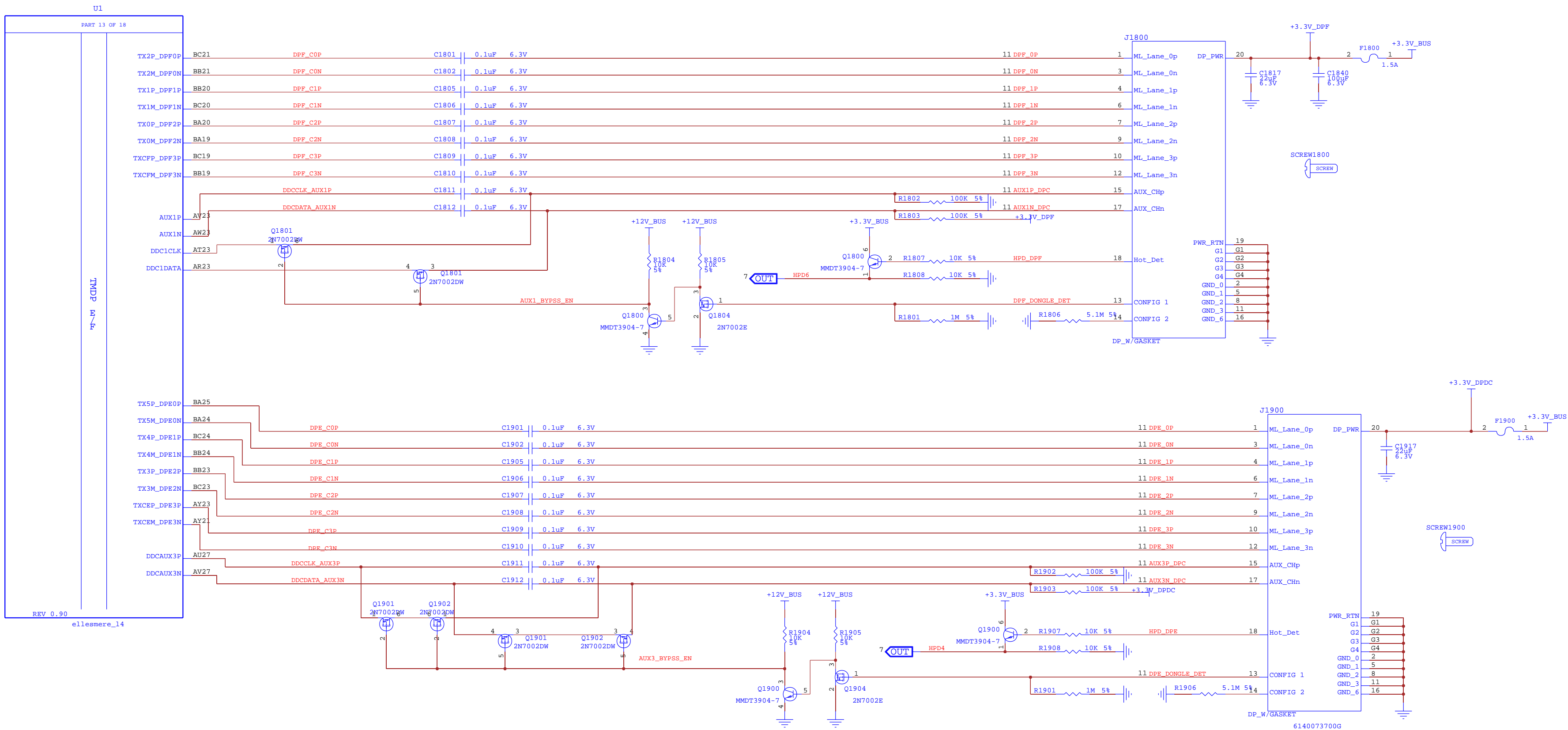
REV: 1.0

SHEET NUMBER: 10 OF 26

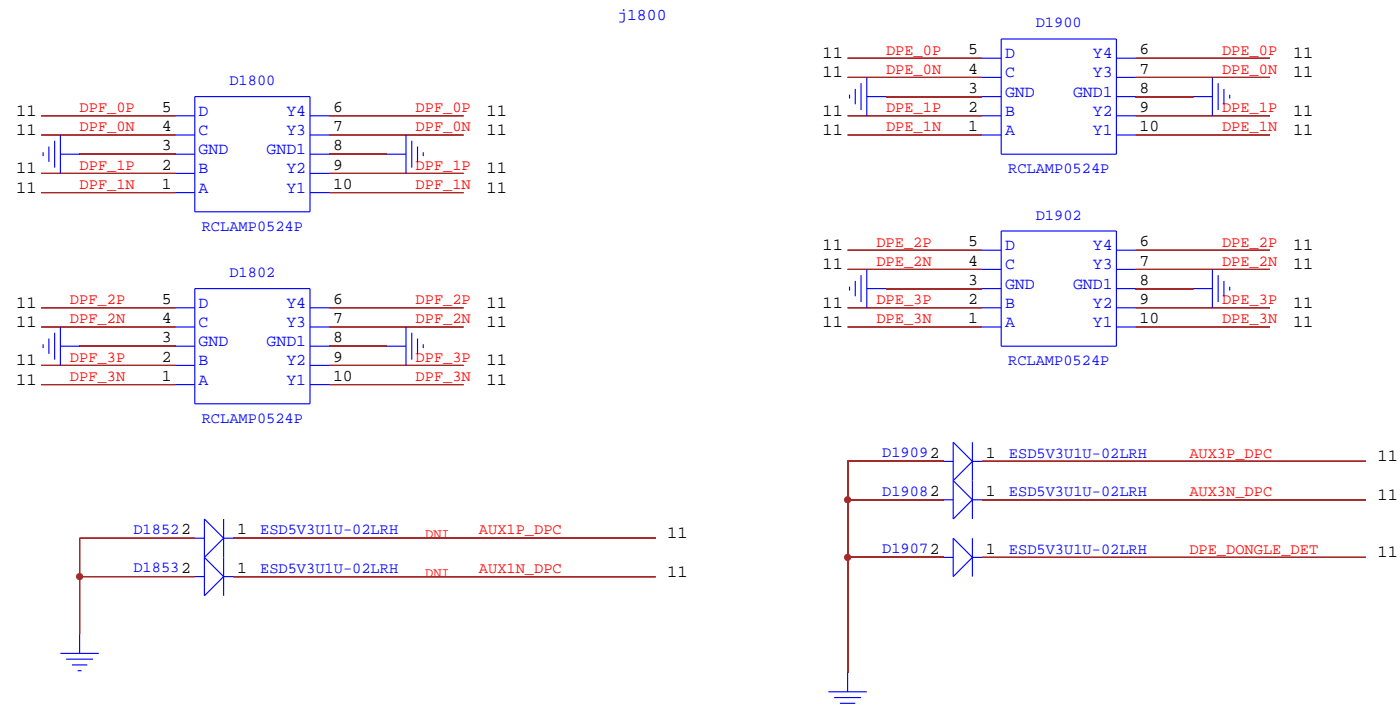
TITLE:

TITLE

(11) ELLESMERE LVTMDP E/F



OPTIONAL ESD PROTECTION DIODES



| | | | |
|---|--|--|--|
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| SHEET: ELLESMERE TMDP DP DP | | TITLE: | |
| DATE: Wed Mar 23 13:12:21 2016 | | REV: 1.0 | |
| SHEET NUMBER: 11 OF 26 | | TITLE: | |
| DOCUMENT NUMBER: 105_CXXX00_00A | | TITLE: | |

(12) ELLESMERE POWER

D

C

B

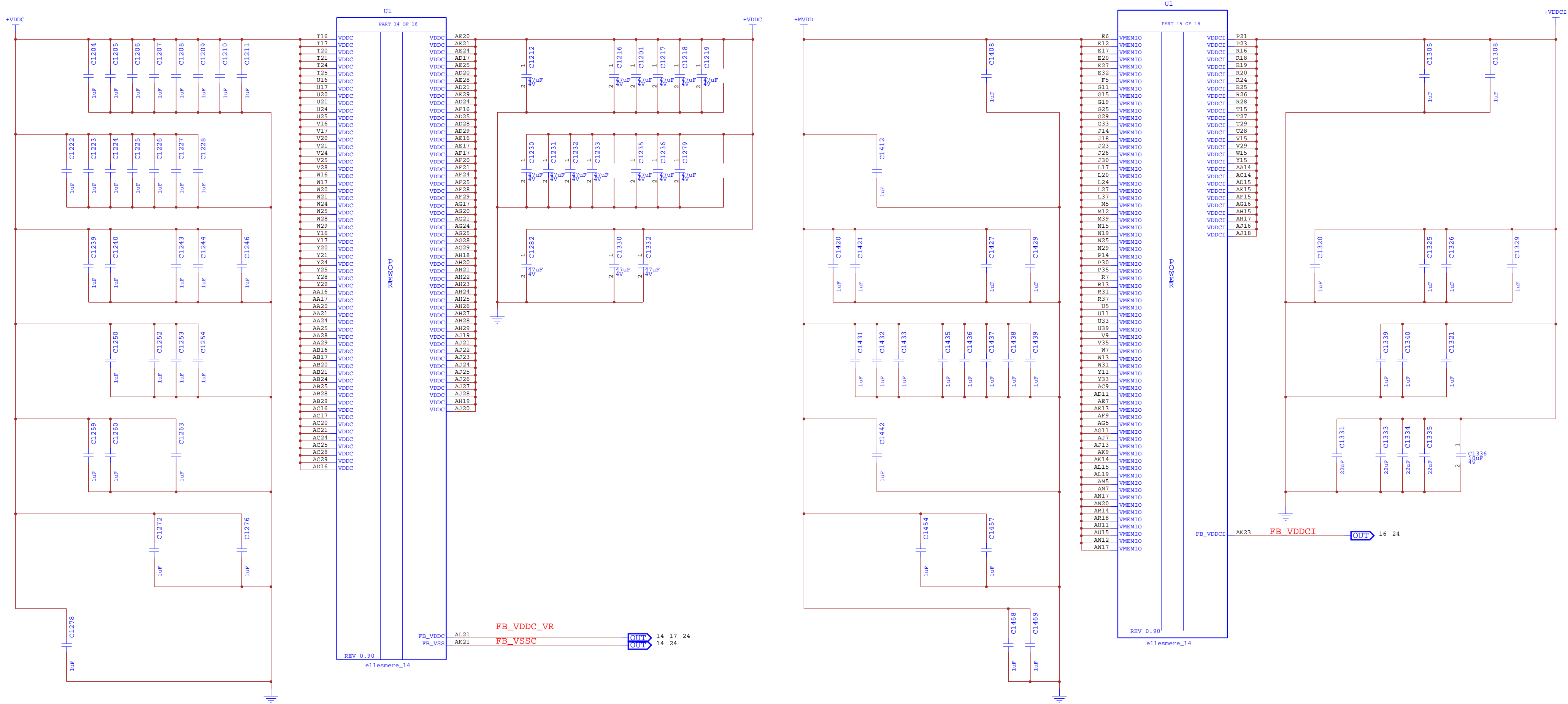
A

D

C

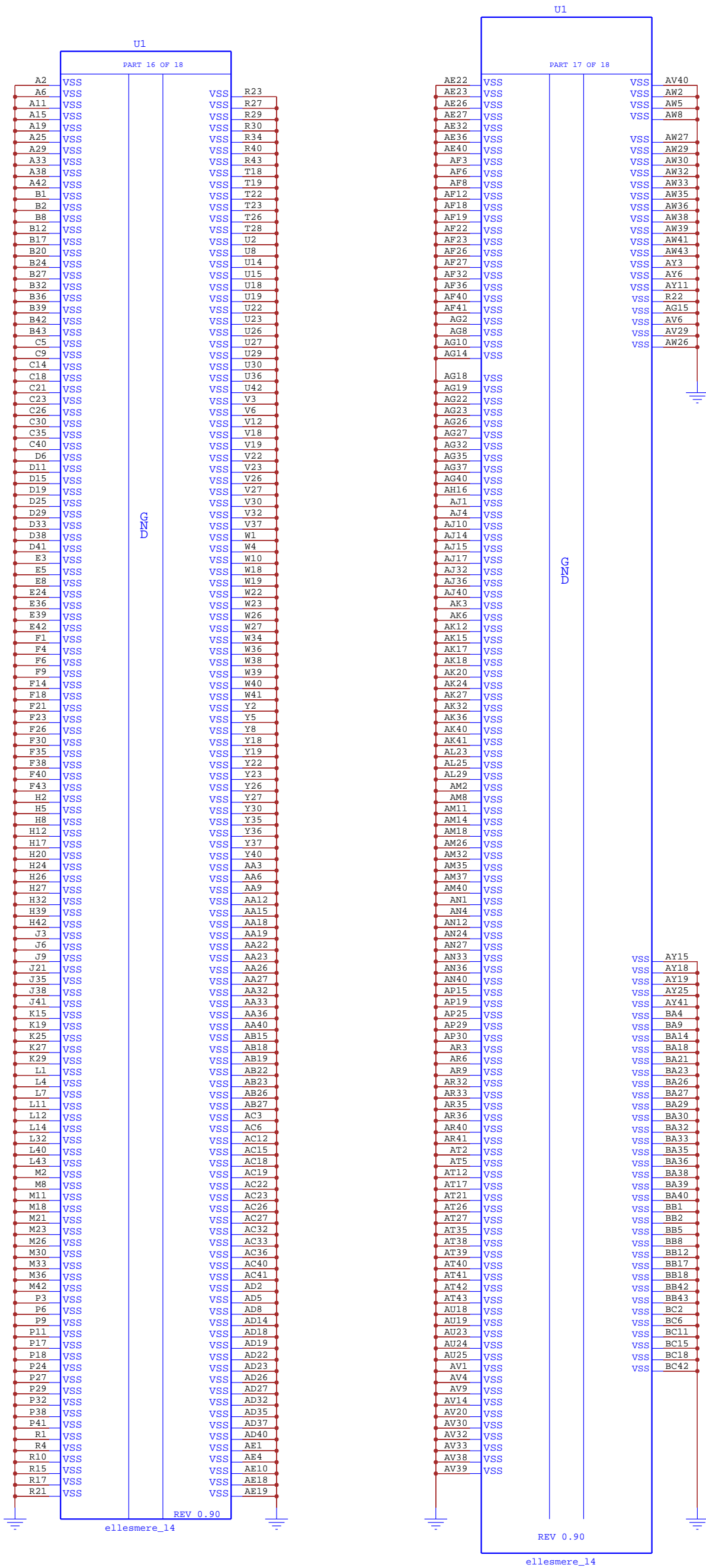
B

A

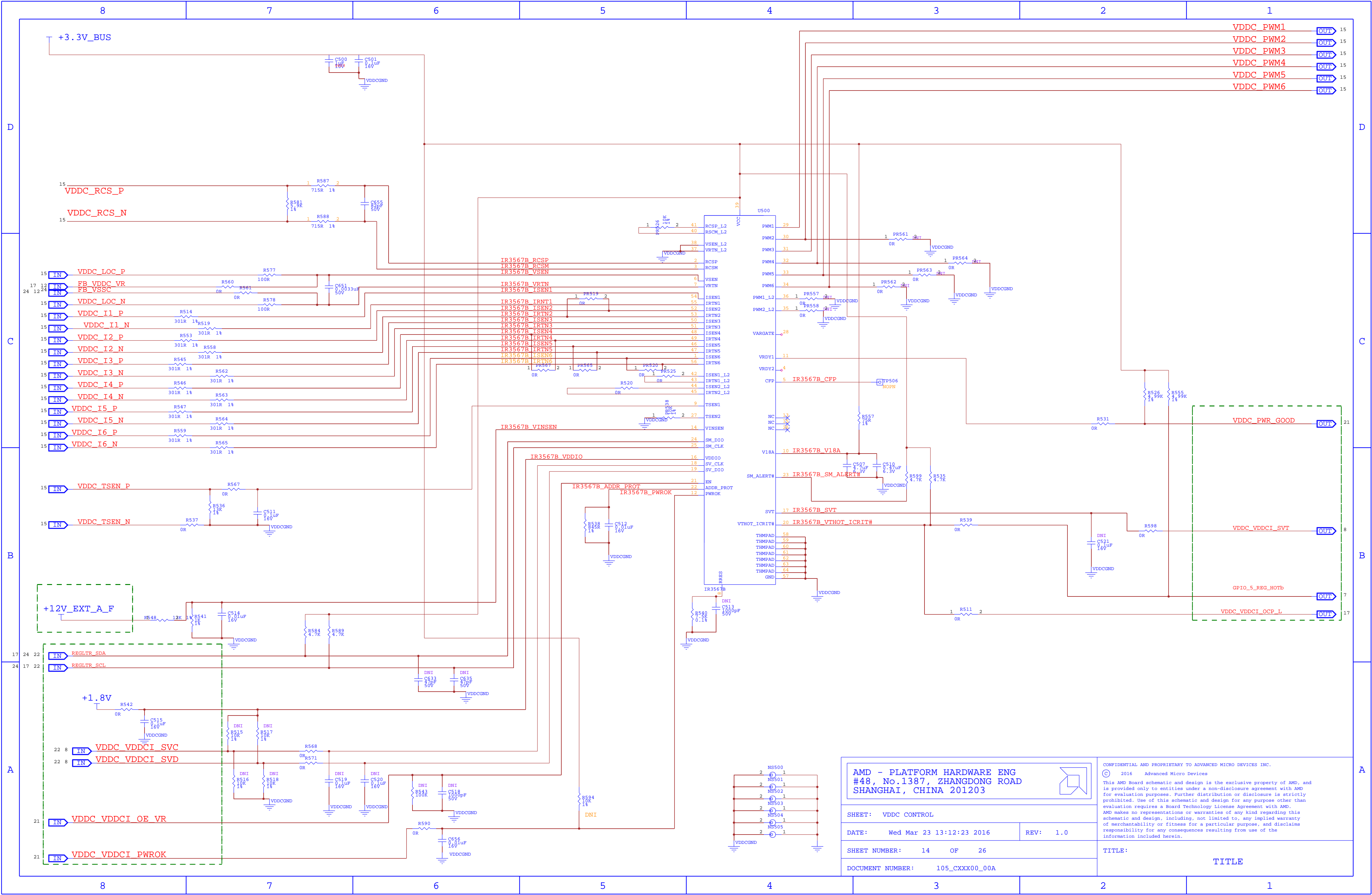


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|--|--|----------|---|--|--|
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| SHEET: ELLESMERE POWER | | | TITLE: | | |
| DATE: Wed Mar 23 13:12:25 2016 | | REV: 1.0 | TITLE | | |
| SHEET NUMBER: 12 OF 26 | | | | | |
| DOCUMENT NUMBER: 105_CXXX00_00A | | | | | |

(13) ELLESMERE GROUND



| | | | |
|---|----------|--|--|
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| SHEET: ELLESMERE GND | | TITLE: | |
| DATE: Wed Mar 23 13:12:28 2016 | REV: 1.0 | TITLE | |
| SHEET NUMBER: 13 OF 26 | | | |
| DOCUMENT NUMBER: 105_CXXX00_00A | | | |



AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: VDDC CONTROL

DATE: Wed Mar 23 13:12:23 2016

SHEET NUMBER: 14 OF 26

DOCUMENT NUMBER: 105_CXXX00_00A

REV: 1.0

TITLE:

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TITLE

VDDC

PLACE NEXT TO PHASE 3 HALF BRIDGE

PLACE BETWEEN PHASE 1 AND 2 INDUCTORS

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SHEET: VDDC

DATE: Wed Mar 23 13:12:24 2016

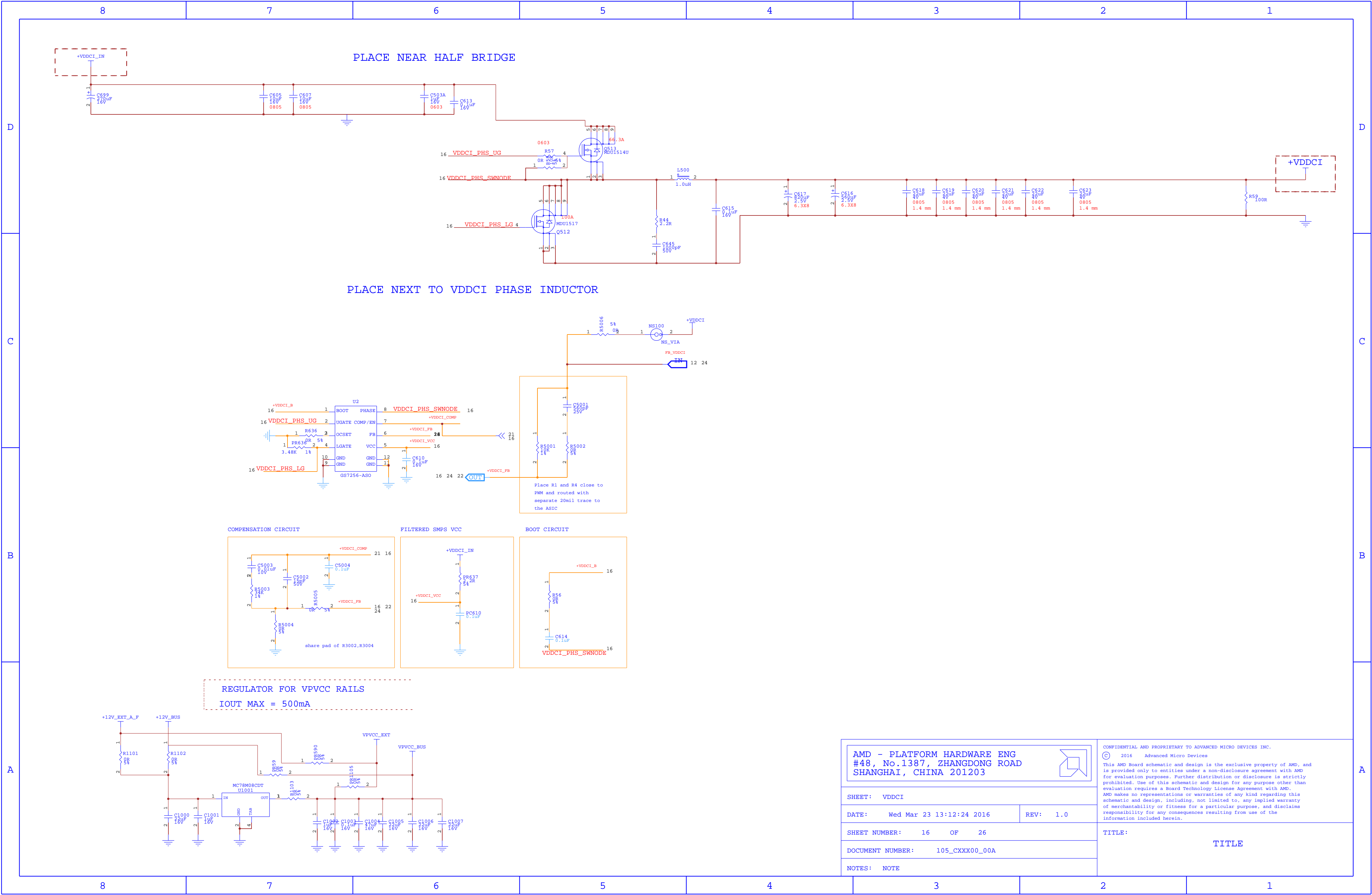
REV: 1.0

SHEET NUMBER: 15 OF 26

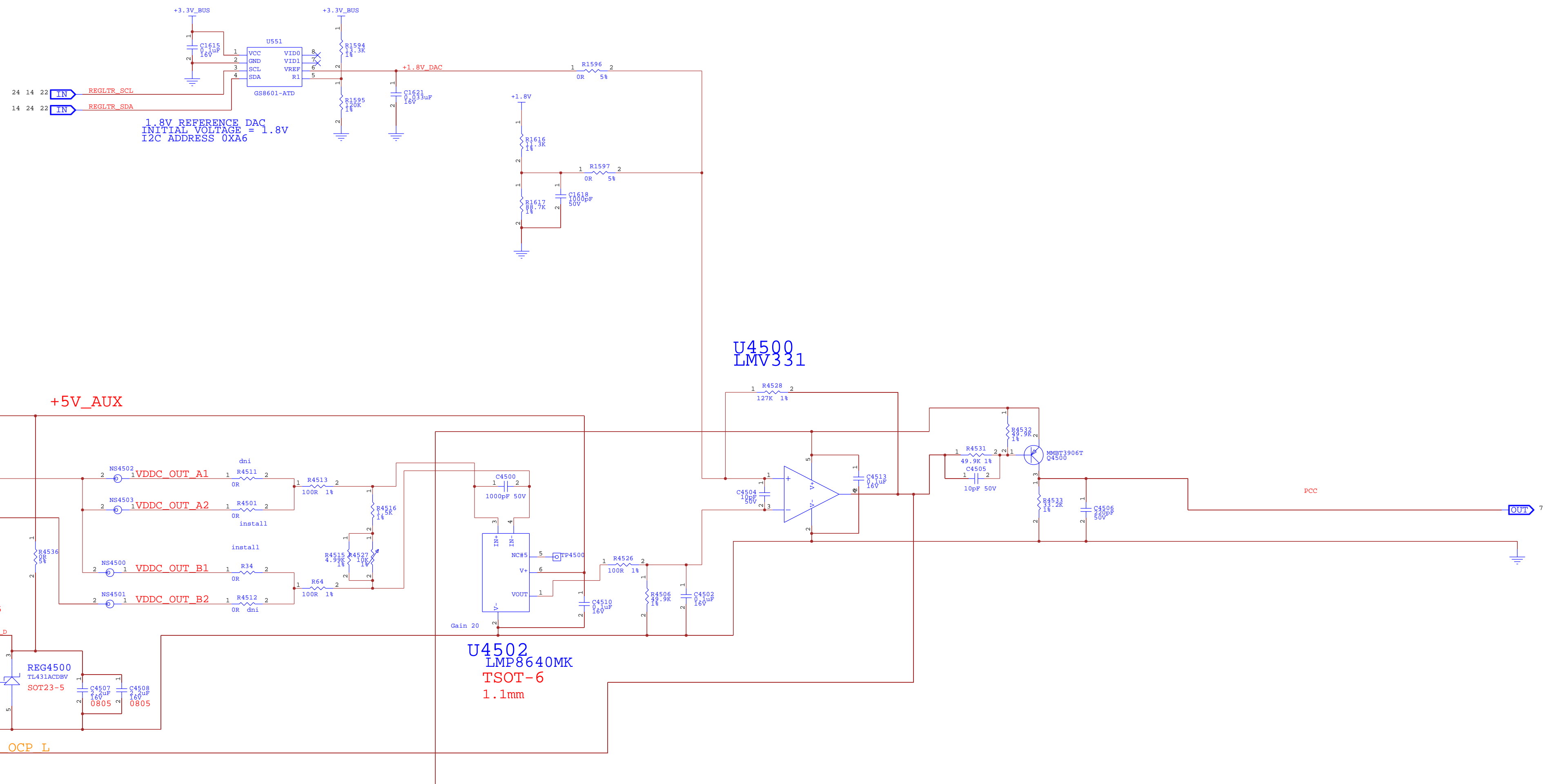
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NOTES: NOTE

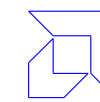
TITLE:
TITLE



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| SHEET: VDDCI | | | <div>TITLE:</div> <div>TITLE</div> | | |
| DATE: Wed Mar 23 13:12:24 2016 | | REV: 1.0 | | | |
| SHEET NUMBER: 16 OF 26 | | | | | |
| DOCUMENT NUMBER: 105_CXXX00_00A | | | | | |
| NOTES: NOTE | | | | | |



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SHEET: PCC VDDC

DATE: Wed Mar 23 13:12:24 2016

REV: 1.0

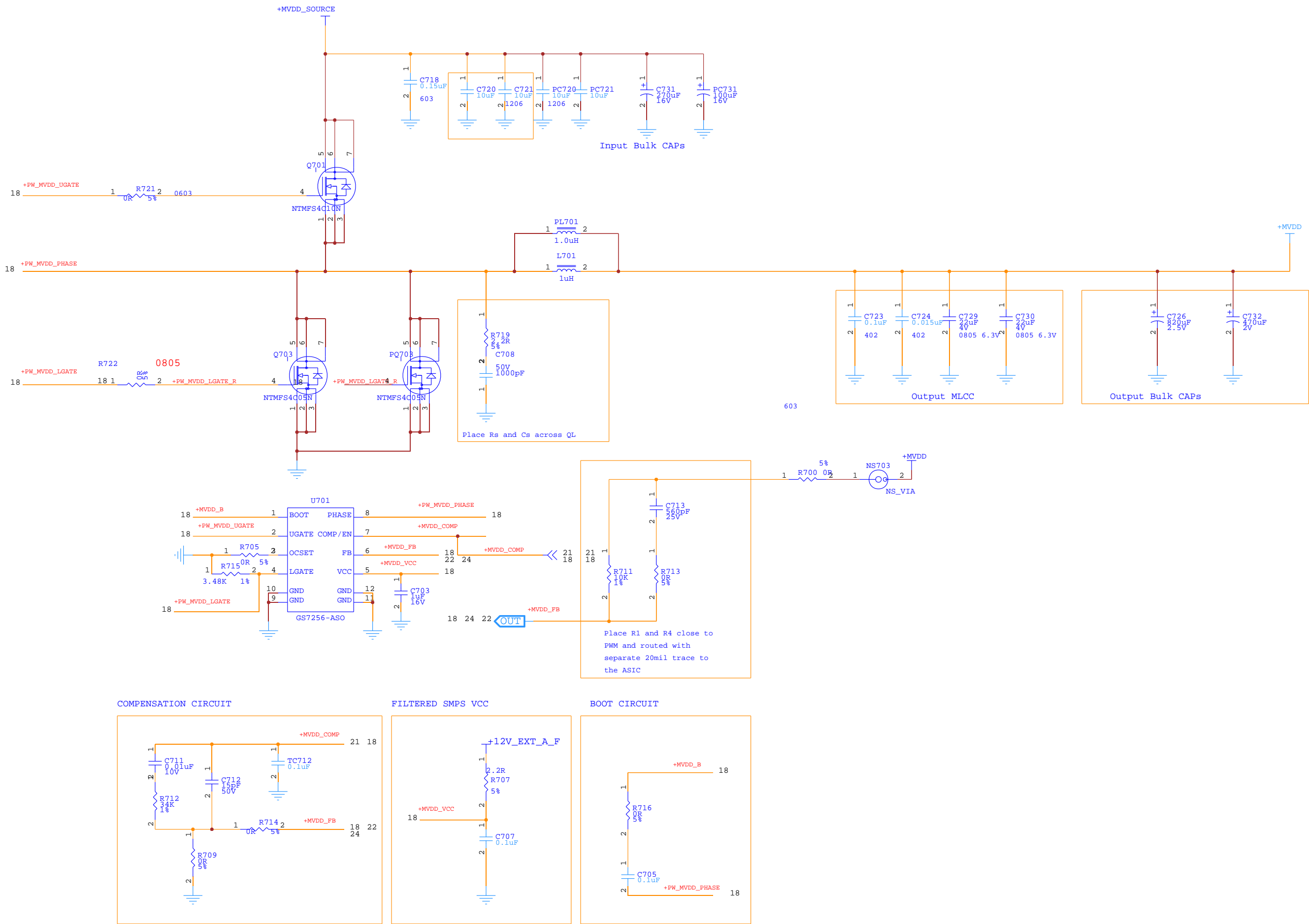
SHEET NUMBER: 17 OF 26

DOCUMENT NUMBER

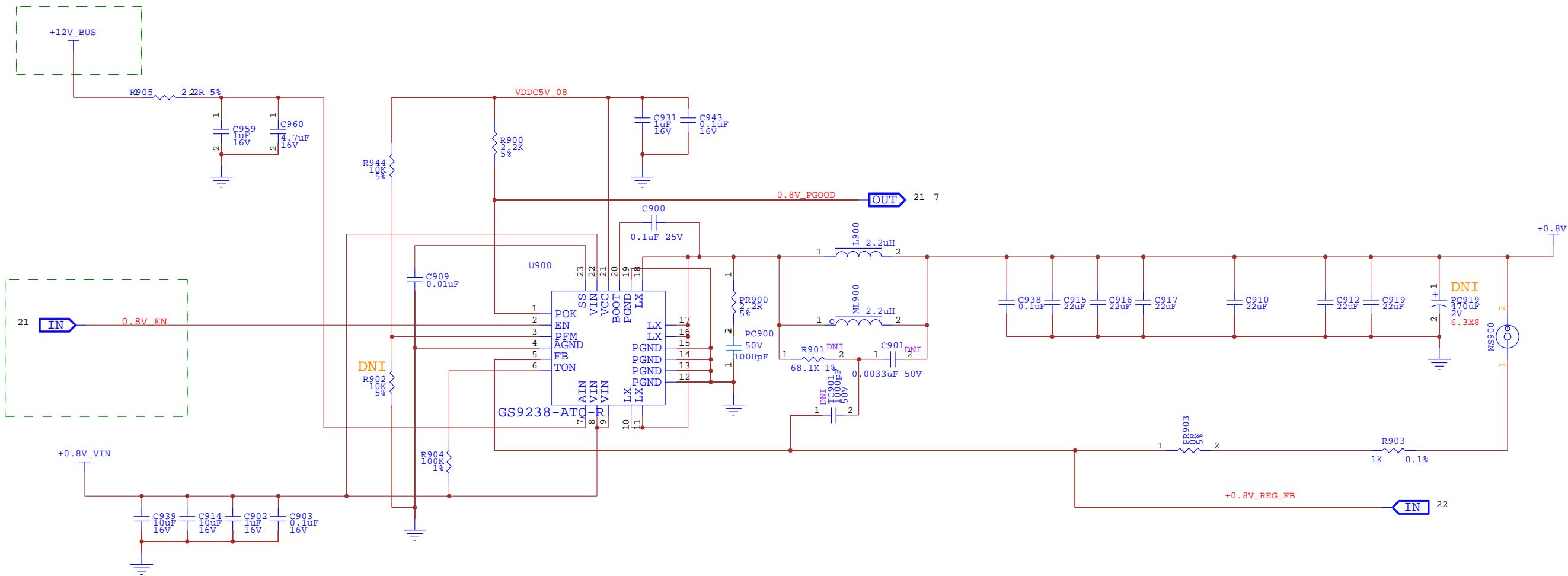
TITLE:

TITLE

(16) MVDD



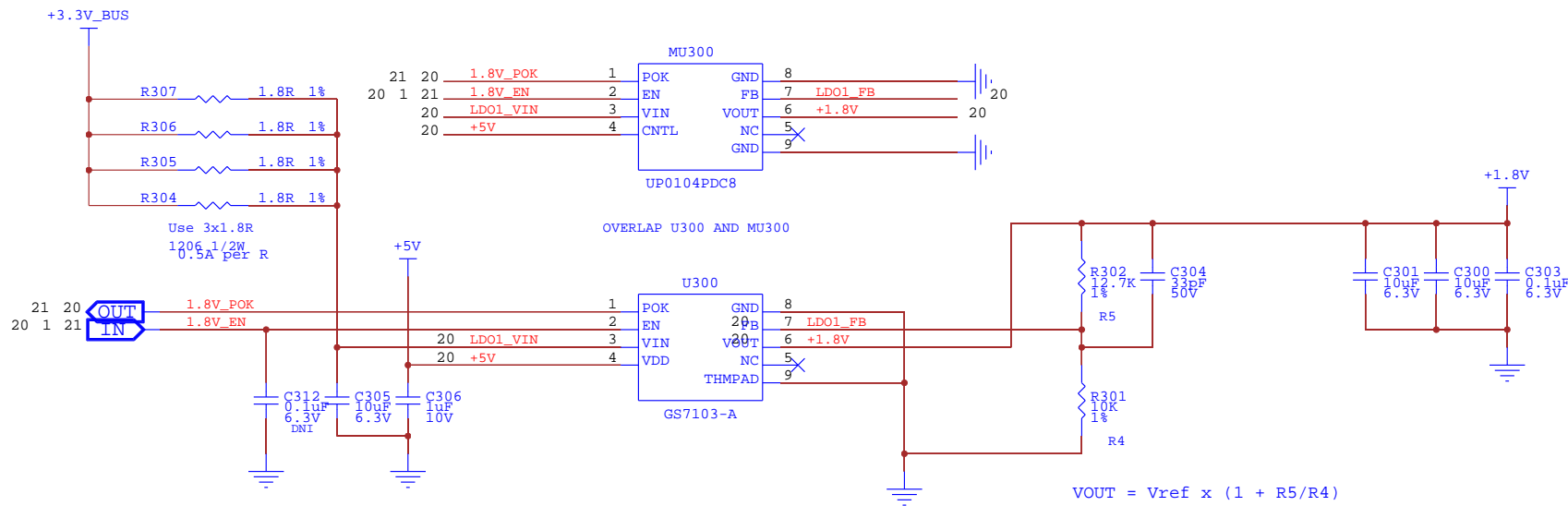
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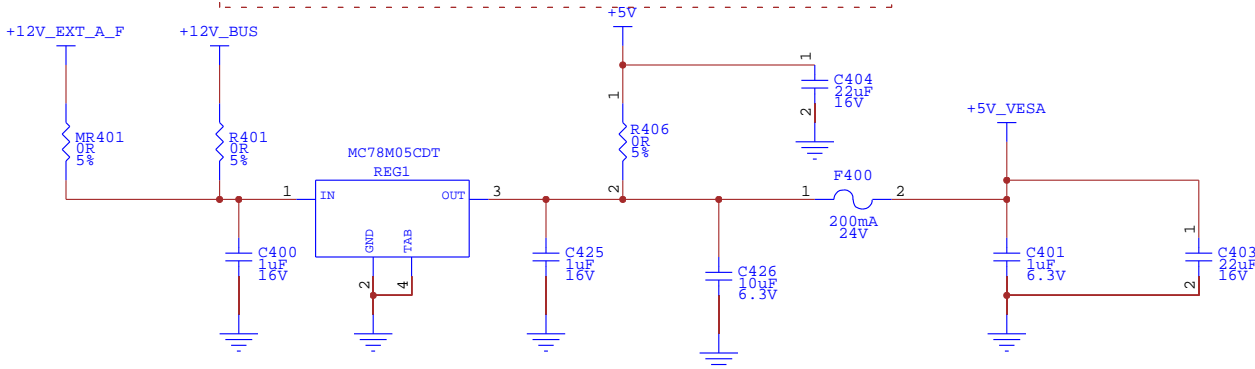
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| SHEET: 0.8V REG | | TITLE: | |
| DATE: Wed Mar 23 13:12:21 2016 | | REV: 1.0 | |
| SHEET NUMBER: 19 OF 26 | | TITLE | |
| DOCUMENT NUMBER: 105_CXXX00_00A | | | |
| NOTES: NOTE | | | |

(18) SMALL RAIL REGULATORS

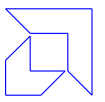
LDO #1: VIN = 3.0V TO 3.6V MAX VOUT = +1.8V +/- 2% IOUT = 1.3A RMS MAX
PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING



REGULATOR FOR +5V RAILS
IOUT MAX = 150mA



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SHEET: SMALL RAIL REGULATORS

DATE: Wed Mar 23 13:12:22 2016

REV: 1.0

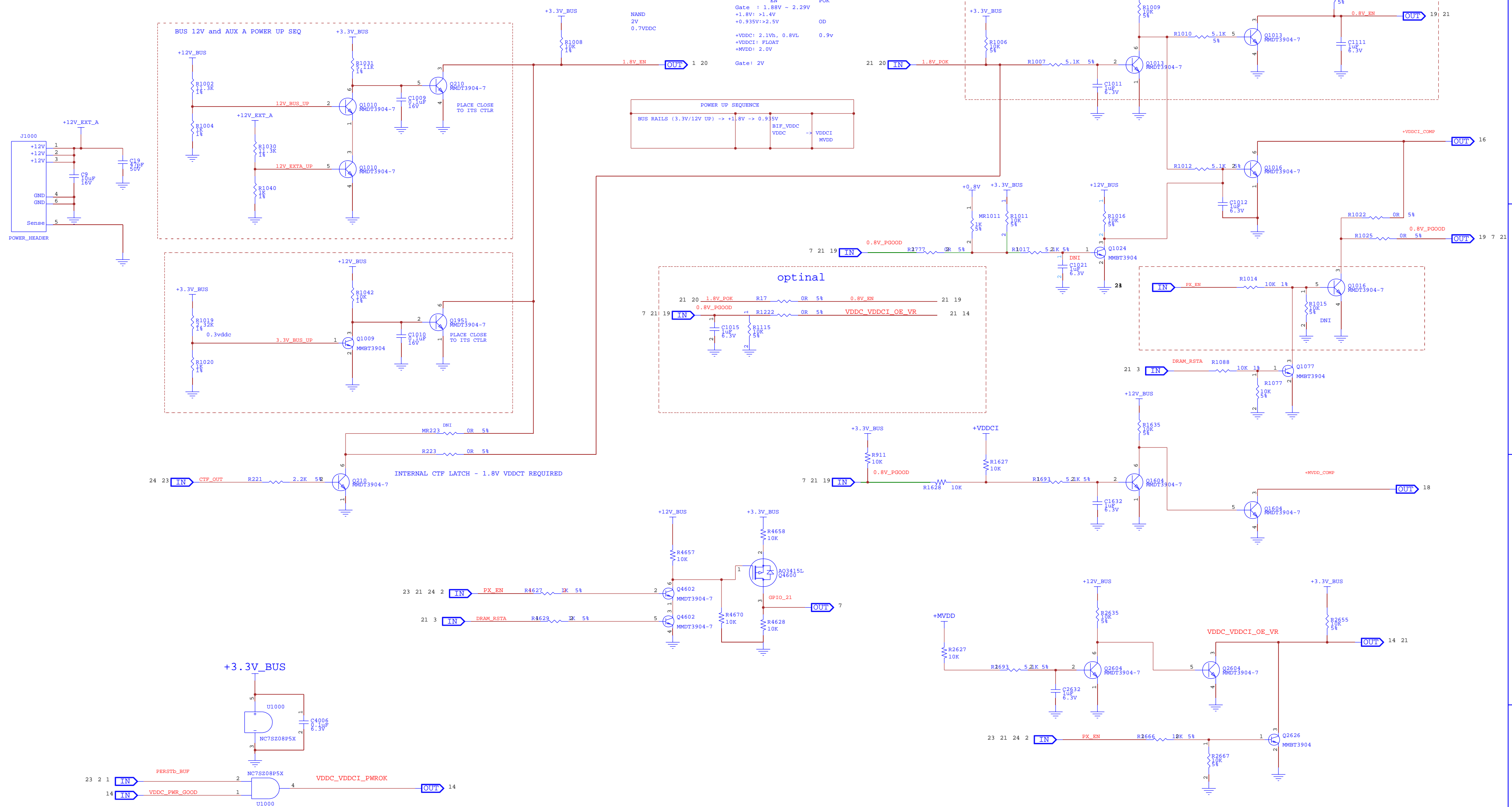
SHEET NUMBER: 20 OF 26

DOCUMENT NUMBER: 105_CXXX00_00A

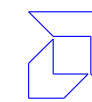
TITLE:

TITLE

(19) POWER MANAGEMENT



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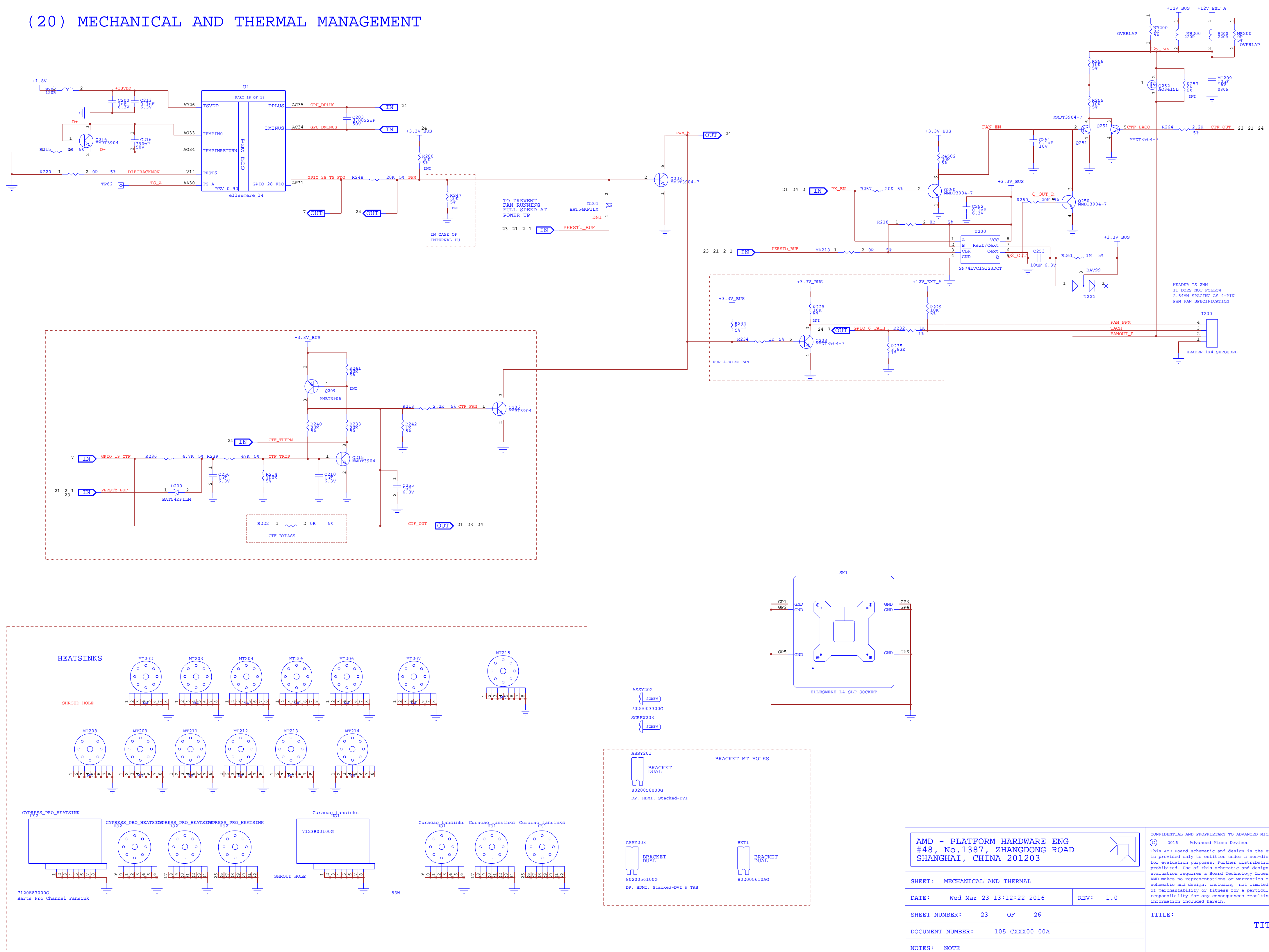
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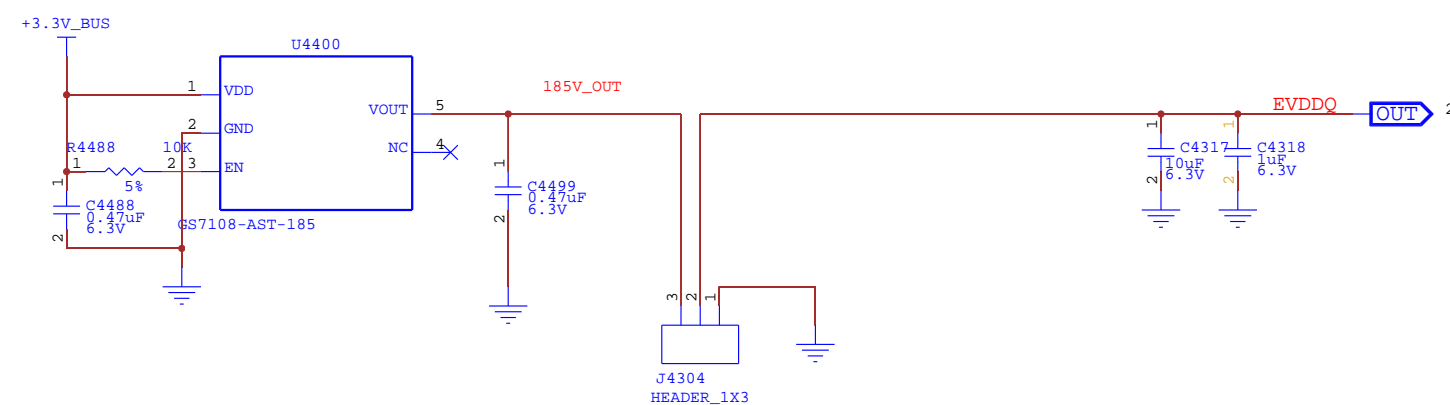
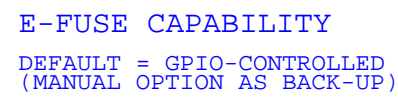
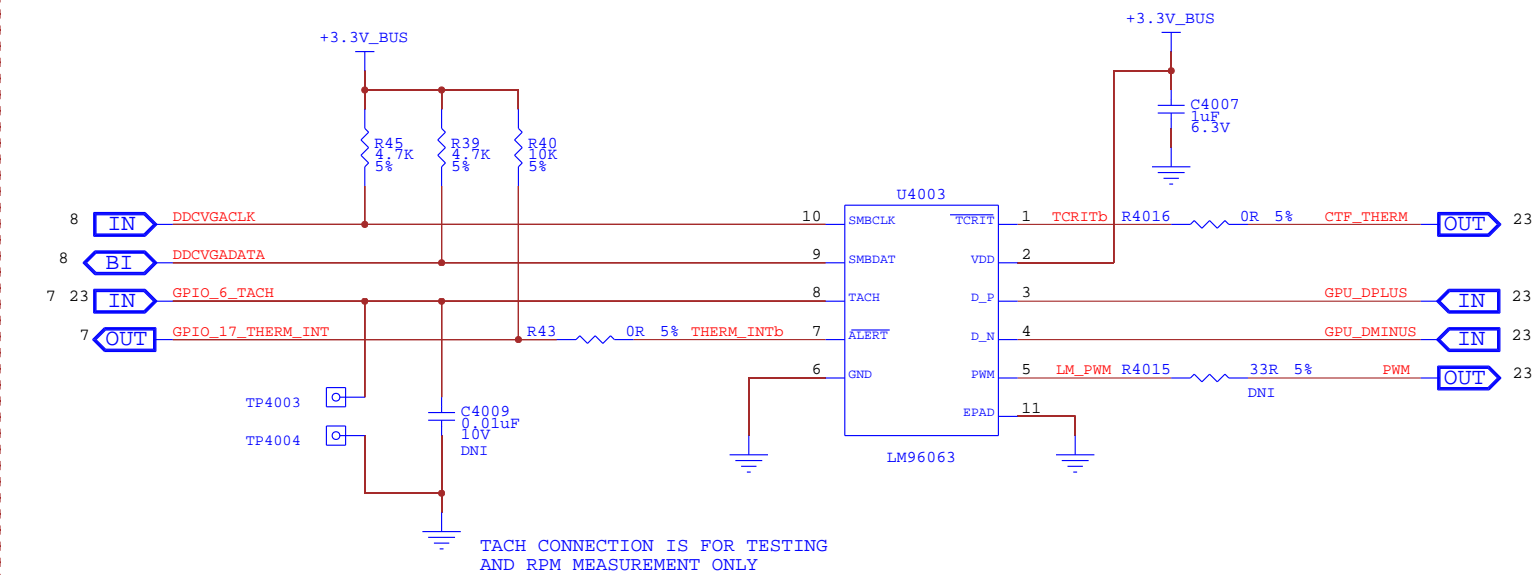
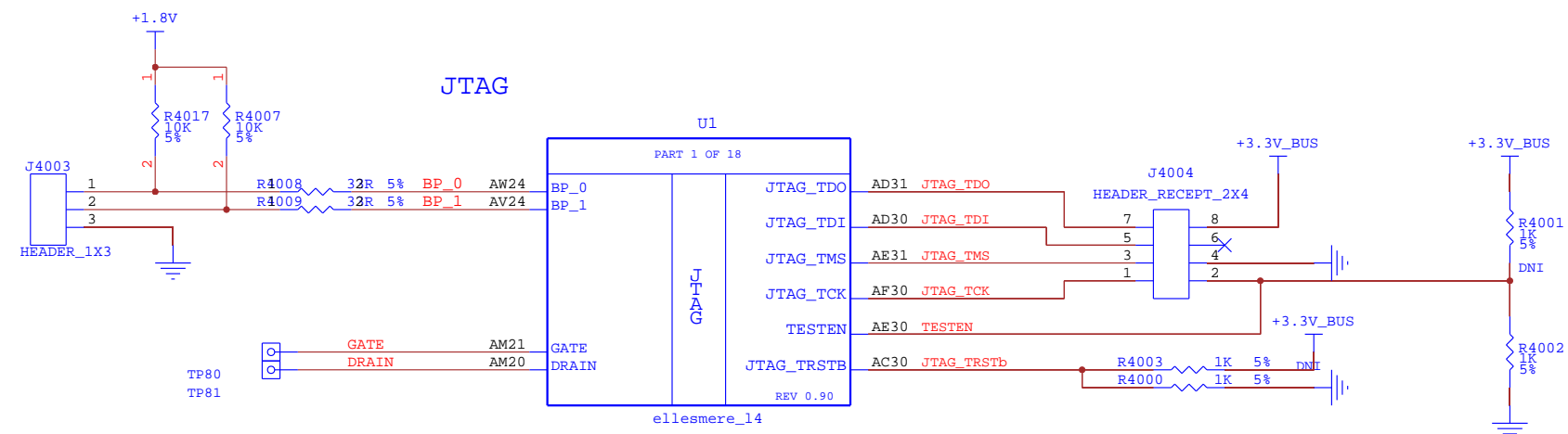
| | |
|--------------------------------|----------|
| SHEET: POWER MANAGEMENT1 | |
| DATE: Wed Mar 23 13:12:19 2016 | REV: 1.0 |
| SHEET NUMBER: 21 OF 26 | |
| DOCUMENT NUMBER: 105_CXX00_00A | |

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| TITLE: | TITLE |
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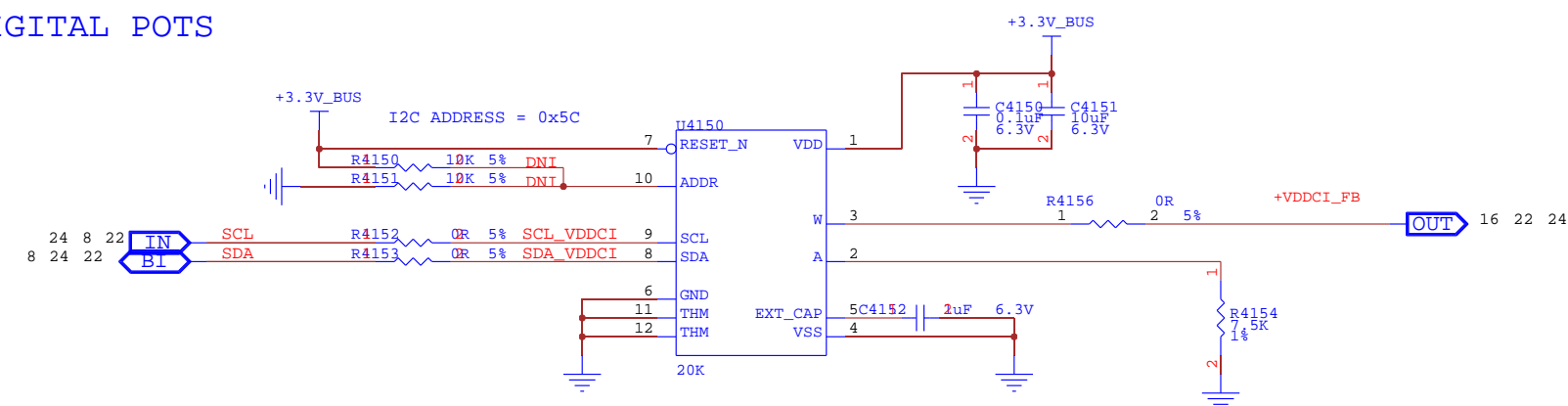
(20) MECHANICAL AND THERMAL MANAGEMENT



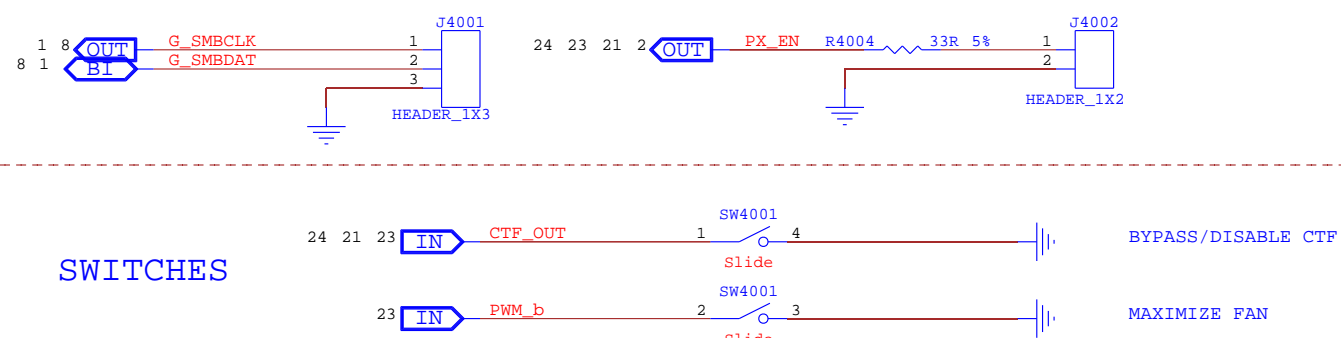
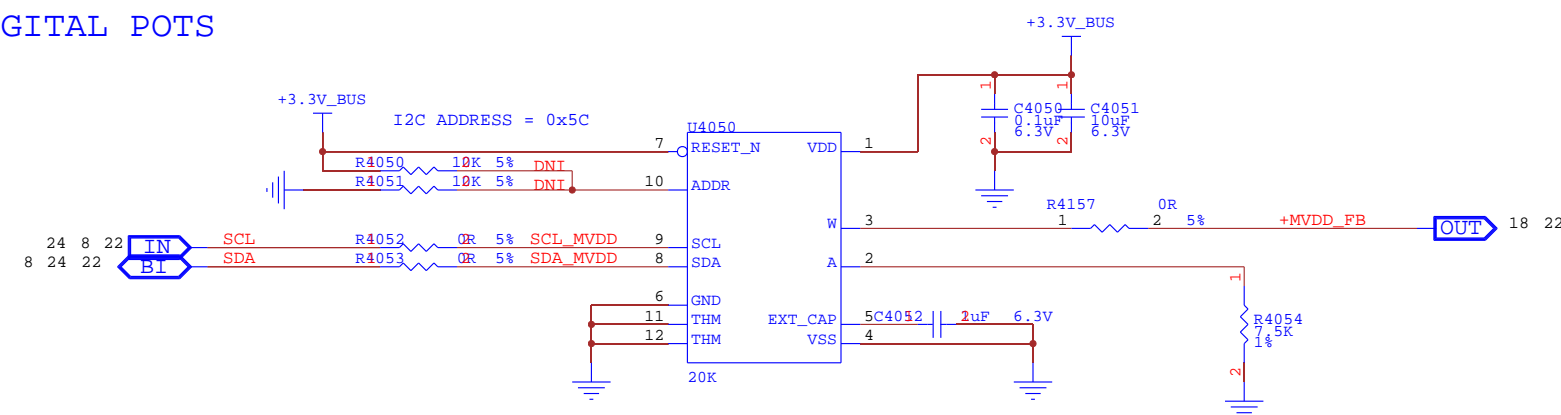
(21) DEBUG CIRCUITS



DIGITAL POTS

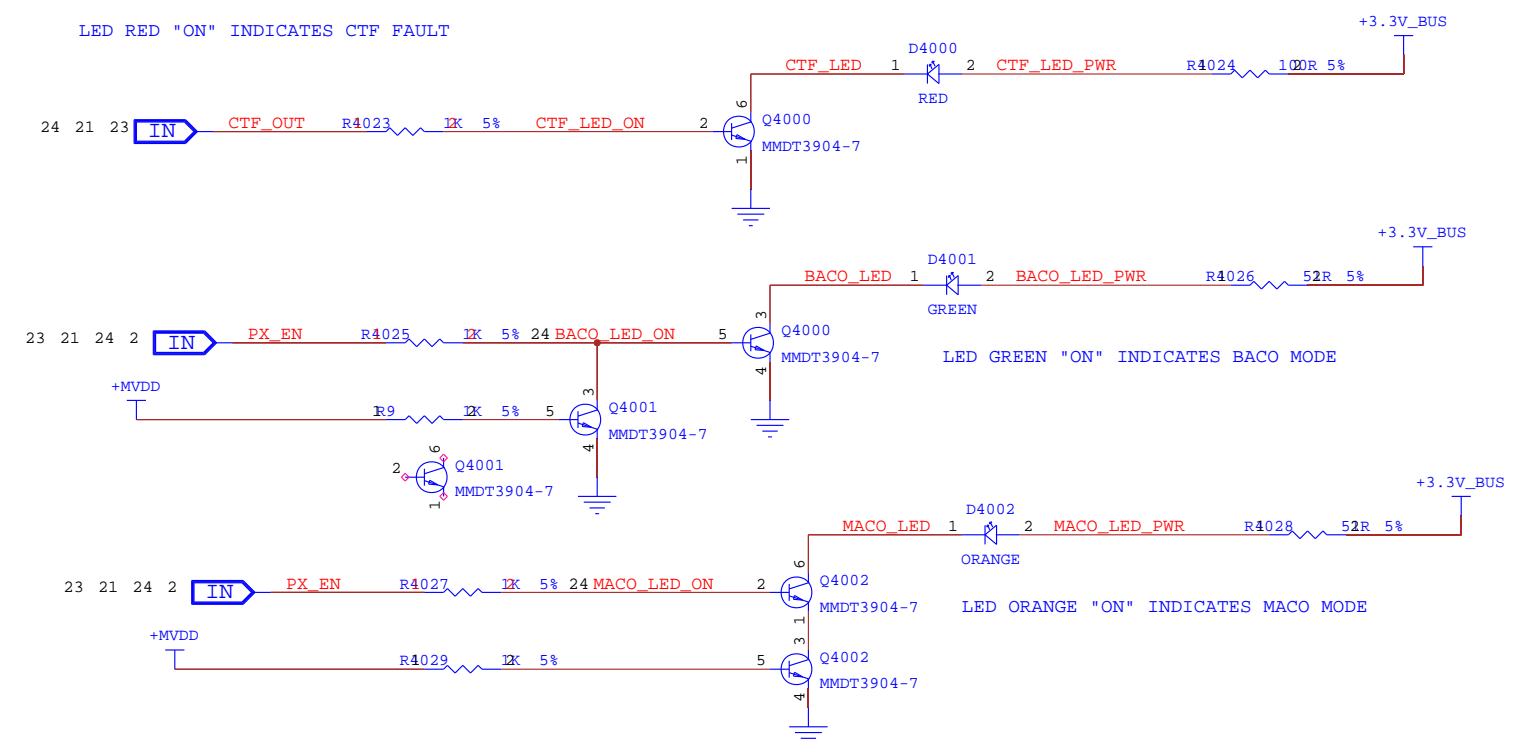


DIGITAL POTS

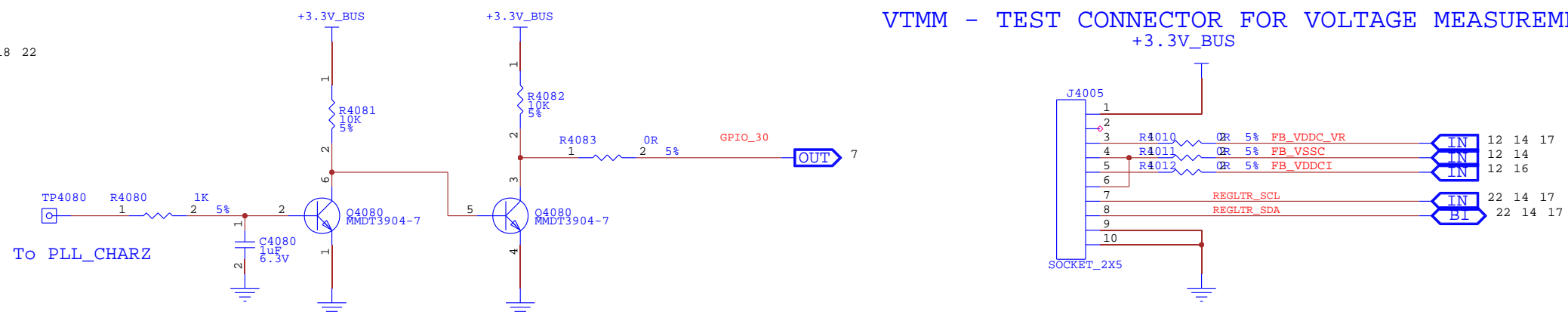


LED LIGHTS

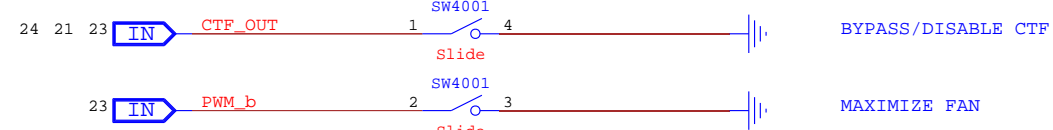
LED RED "ON" INDICATES CTF FAULT



VTMM - TEST CONNECTOR FOR VOLTAGE MEASUREMENTS
+3.3V_BUS



SWITCHES



AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

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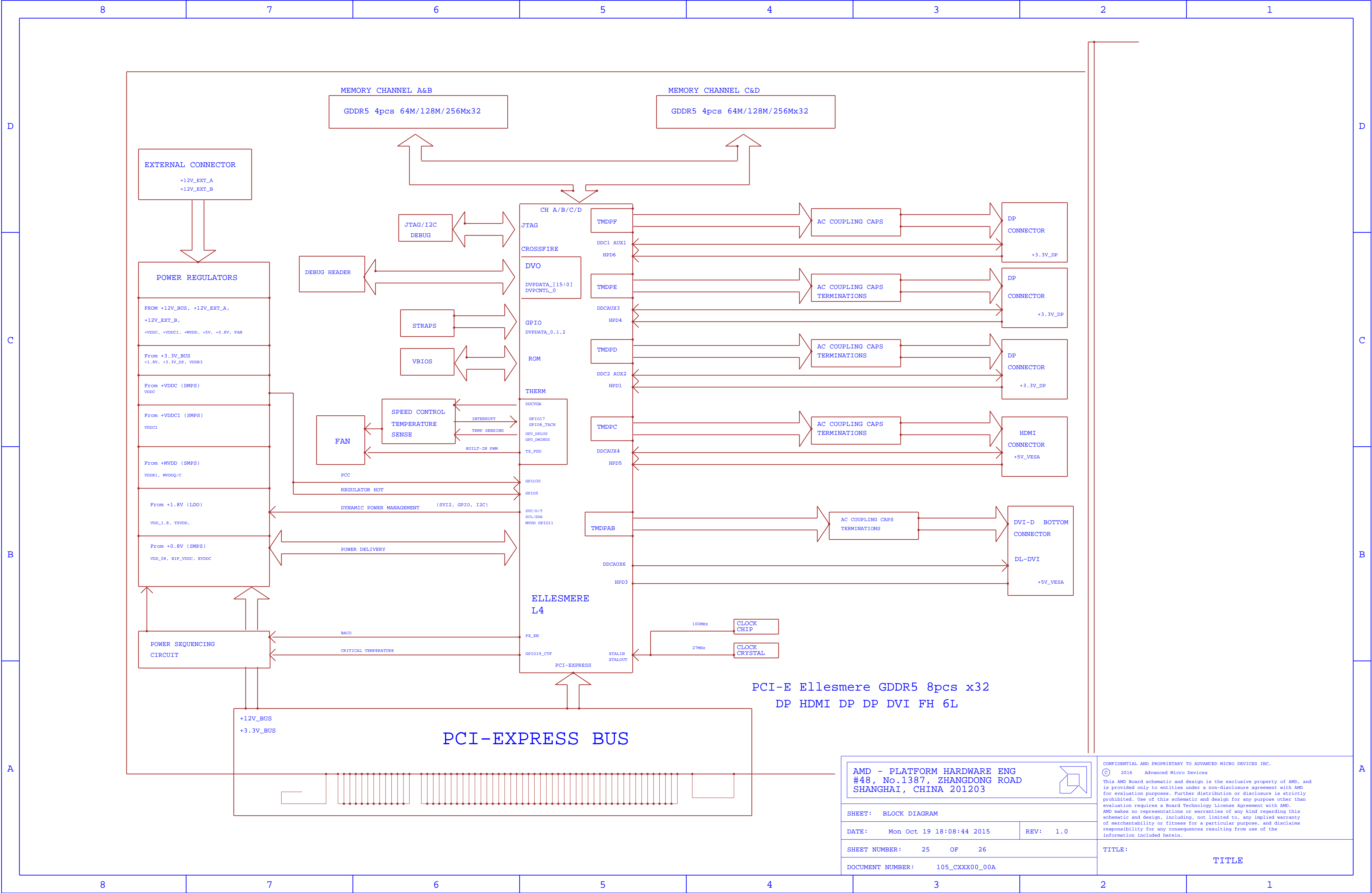
SHEET: DEBUG CIRCUITS/ E-FUSE

DATE: Wed Mar 23 13:12:22 2016

SHEET NUMBER: 24 OF 26

TITLE:

TITLE



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| 8 | | 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | | | |
| <div>AMD</div> | | TITLE: | | | | DOCUMENT NUMBER: 105_CXXX00_00A | | | | DATE: Wed Mar 23 13:57:36 2016 | | | | SHEET NUMBER: 26 OF 26 | | REV: 1.0 | |
| REVISION HISTORY | | | | ENGINEER: XXX | | NOTES: NOTE | | | | CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. C • 2016 Advanced Micro Devices This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein. | | | | AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203 | | | |
| SCH Rev | | PCB Rev | | Date | | REVISION DESCRIPTON | | | | | | | | | | | |
| 0 | | 00A | | 08/28/2015 | | | | | | | | | | | | | |
| 1 | | 00B | | 10/19/2015 | | 1. Add GPIO1 for dynamic VDDCI 2. update VDDC driver sequence | | | | | | | | | | | |
| 2 | | 00C | | 03/23/2016 | | HDMI: - add series resistor R1880 ~R1887 - add pull down inductor L1880 ~L1887 remove C405, C403, VR400,C410,C414,R405 | | | | | | | | | | | |
| 8 | | 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | | | |