

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV

ECN

DESCRIPTION OF REVISION

CK APPD  
DATE

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0001052699

PRODUCTION RELEASED

2011-01-10

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PDF CSA CONTENTS

11

1

TABLE OF CONTENTS

MIKE

N/A

22

2

BLOCK DIAGRAM: SYSTEM

MIKE

N/A

33

5

BOM TABLE

MIKE

N/A

44

6

AP: MAIN

JAMES

N/A

55

7

AP: I/Os

JAMES

N/A

66

8

AP: NAND

JAMES

N/A

77

9

AP: TV,DP,MIPI

JAMES

N/A

88

10

AP: PWR

JAMES

N/A

99

11

AP: PWR

JAMES

N/A

1010

12

AP: MISC & ALIASES

JAMES

N/A

1111

13

AP: VIDEO BUFFER,BB USB MUXES

JAMES

N/A

1212

14

NAND

JONATHAN

N/A

1313

17

VIDEO: DISPLAY PORT

JAMES

N/A

1414

20

VIDEO: MLC

MIKE

N/A

1515

21

VIDEO: MLC ALIASES

MIKE

N/A

1616

22

VIDEO: LVDS CONNECTOR

ALEX

N/A

1717

30

GRAPE: GROUNDHOG,CONN,BOOST

RAMSIN

N/A

1818

31

GRAPE: Z1, Z2

RAMSIN

N/A

1919

36

AUDIO: L63 CODEC

LENG

N/A

2020

37

AUDIO: SPEAKER AMP

LENG

N/A

2121

38

AUDIO: HEADPHONE OUT

LENG

N/A

2222

39

AUDIO: BLANK

LENG

N/A

2323

42

AUDIO: DETECT/MIC BIAS

LENG

N/A

2424

43

AUDIO: HP/MIC FILTERS

LENG

N/A

2525

54

CONNECTOR: CANADA FLEX CONN,SENSOR PANEL

MARK B.

N/A

2626

55

CONNECTOR: CANADA FLEX FILTERS

MARK B.

N/A

2727

56

CONNECTOR: SENSOR PANEL CONNECTOR

MARK B.

N/A

2828

57

IO FLEX: DOCK COMPONENTS

JAMES

N/A

2929

59

IO FELX: B2B Connector

JAMES

N/A

3030

60

CONNECTOR: X23 WIFI/BT

MIKE

N/A

3131

61

CONNECTOR: X24 CELLULAR/GPS

MIKE

N/A

PDF CSA CONTENTS

32

73

POWER: ALIASES

YOSH

N/A

33

75

POWER: BATTERY CONNECTOR

YOSH

N/A

34

81

POWER: PMU

YOSH

N/A

35

82

POWER: PMU

YOSH

N/A

36

83

POWER: 3.3V VR

YOSH

N/A

37

90

DEBUG AND MISC

MIKE

N/A

38

93

FCT/ICT TEST/BRACKETS

MIKE

N/A

39

100

CONSTRAINTS: ASSIGNMENTS

MIKE

N/A

40

101

CONSTRAINTS: ASSIGNMENTS

MIKE

N/A

41

102

CONSTRAINTS: MLB RULES

MIKE

N/A

42

106

CONSTRAINTS: RF RULES

MIKE

N/A

DRAWING

TITLE=BACH

ABBREV=DRAWING

DRAWING TITLE

Apple Inc.

051-8962

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D	<div>Page Notes</div> <div>Power aliases required by this page: (NONE)</div> <hr/> <div>Signal aliases required by this page: (NONE)</div> <hr/> <div>BOM options provided by this page:</div>																																																																																																																																																									
	<div>ALL AVAIL BOM OPTIONS</div> <div>COMMON ALTERNATE 16GB_PROD 32GB_PROD 64GB_PROD BKLT_PLL DEVELOPMENT_JTAG DEVELOPMENT_JTAG_TAP JTAG_DAP JTAG_TAP_NOT SPEAKER INTERNAL_MIC PORTRAIT_DOCK MLC_DEV MLC_PROD  K93 K94</div>																																																																																																																																																									
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SYNC MASTER=MIKE

SYNC DATE=N/A

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ALL AVAIL BOM OPTIONS

BOM GROUP	BOM OPTIONS
BASIC	COMMON ,ALTERNATE

ADD DEVELOPMENT AND OTHER BOMS ONCE YOU GET BOM NUMBERS


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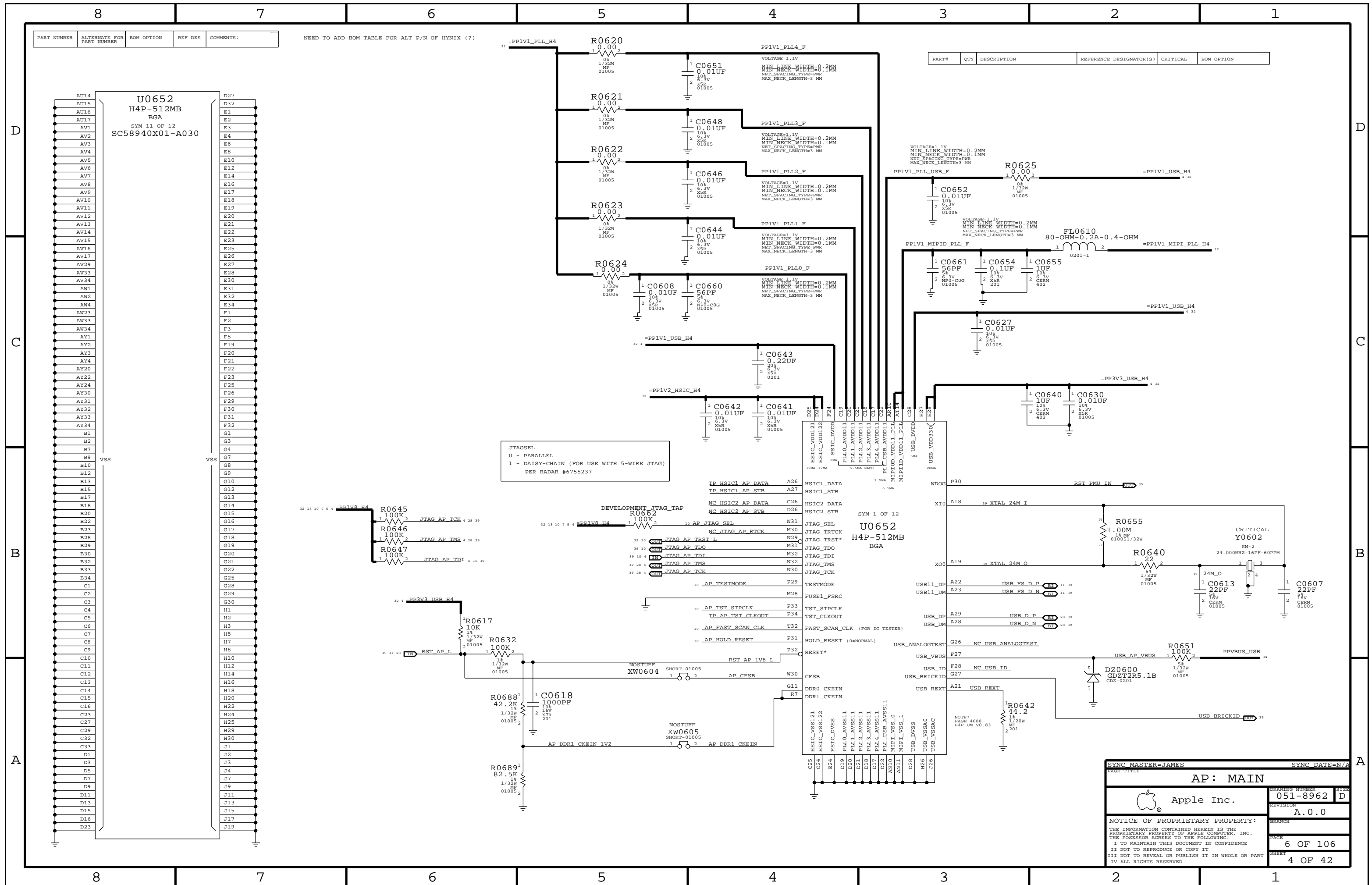
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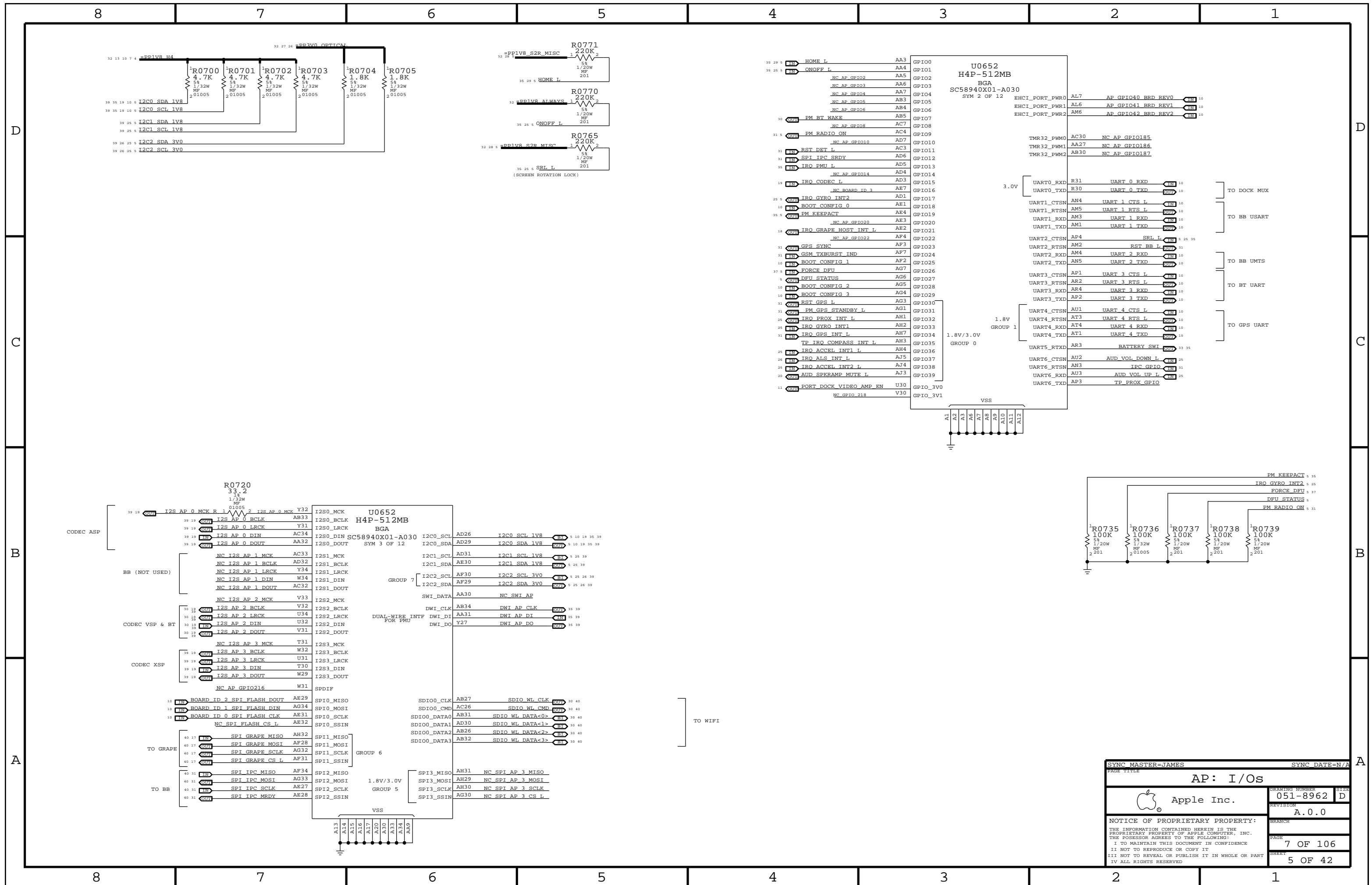
TOP BARCODE LABEL/EEE CODES  
(ONLY ONE IS USED PER BOM)

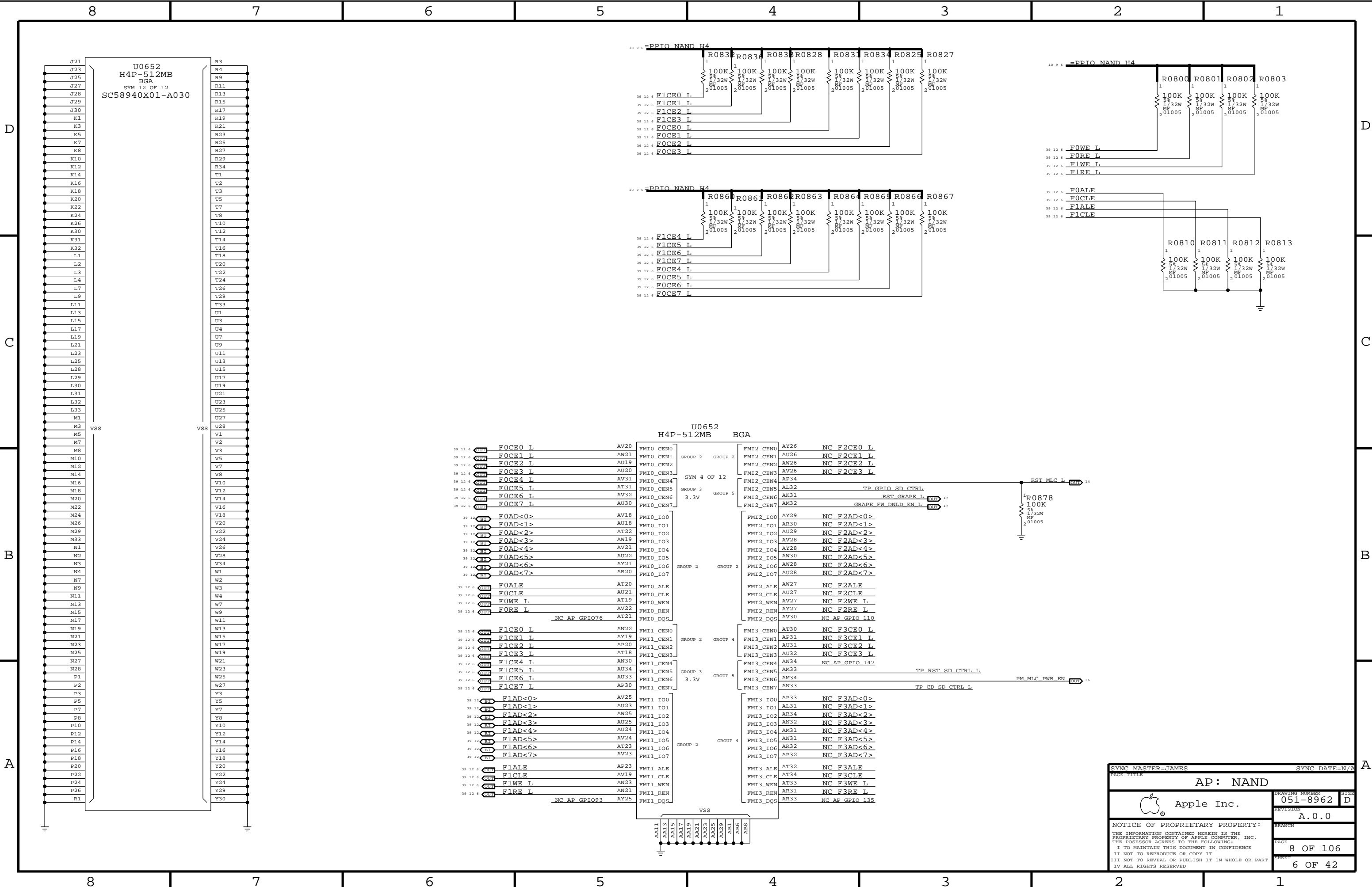
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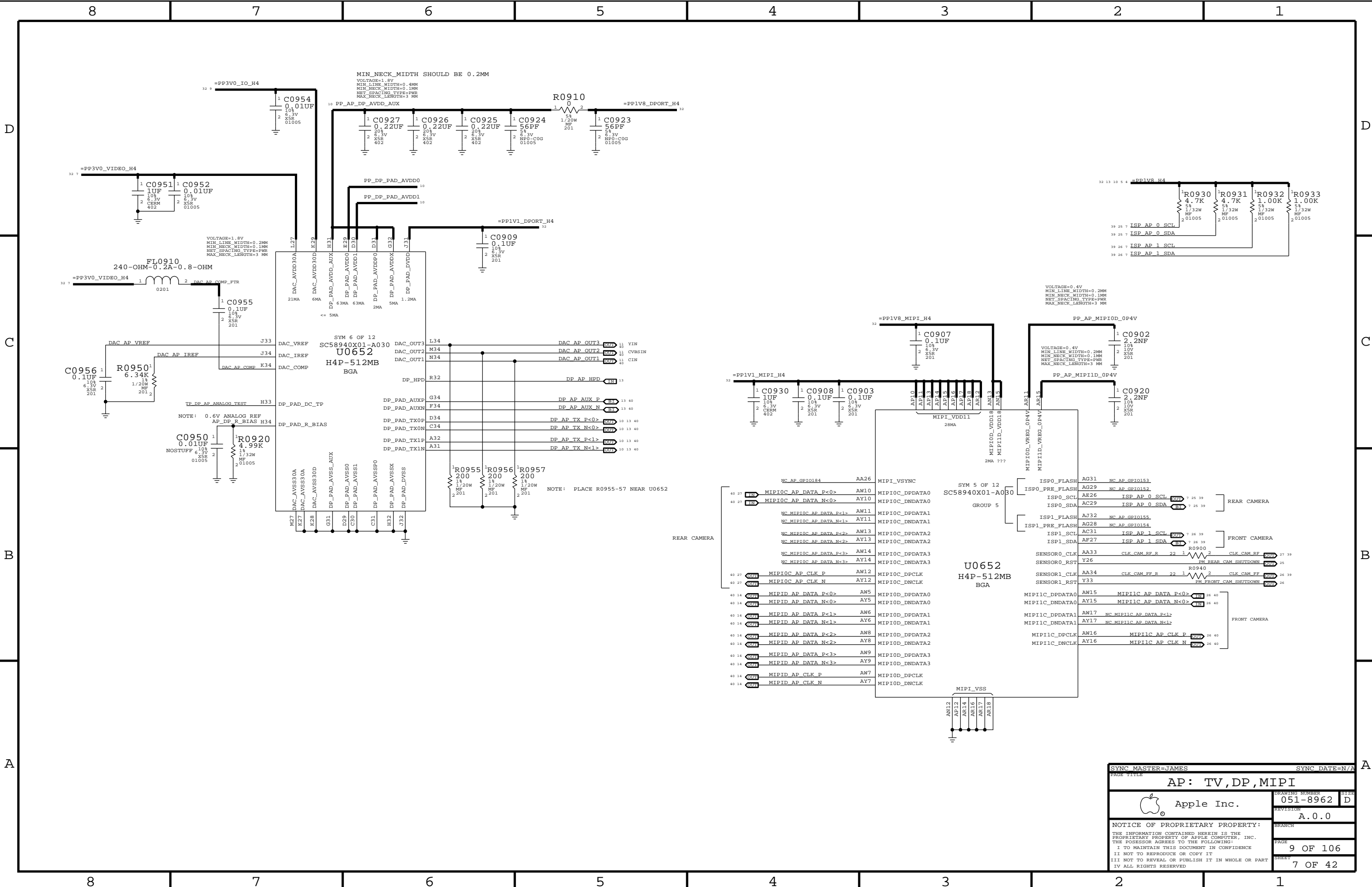
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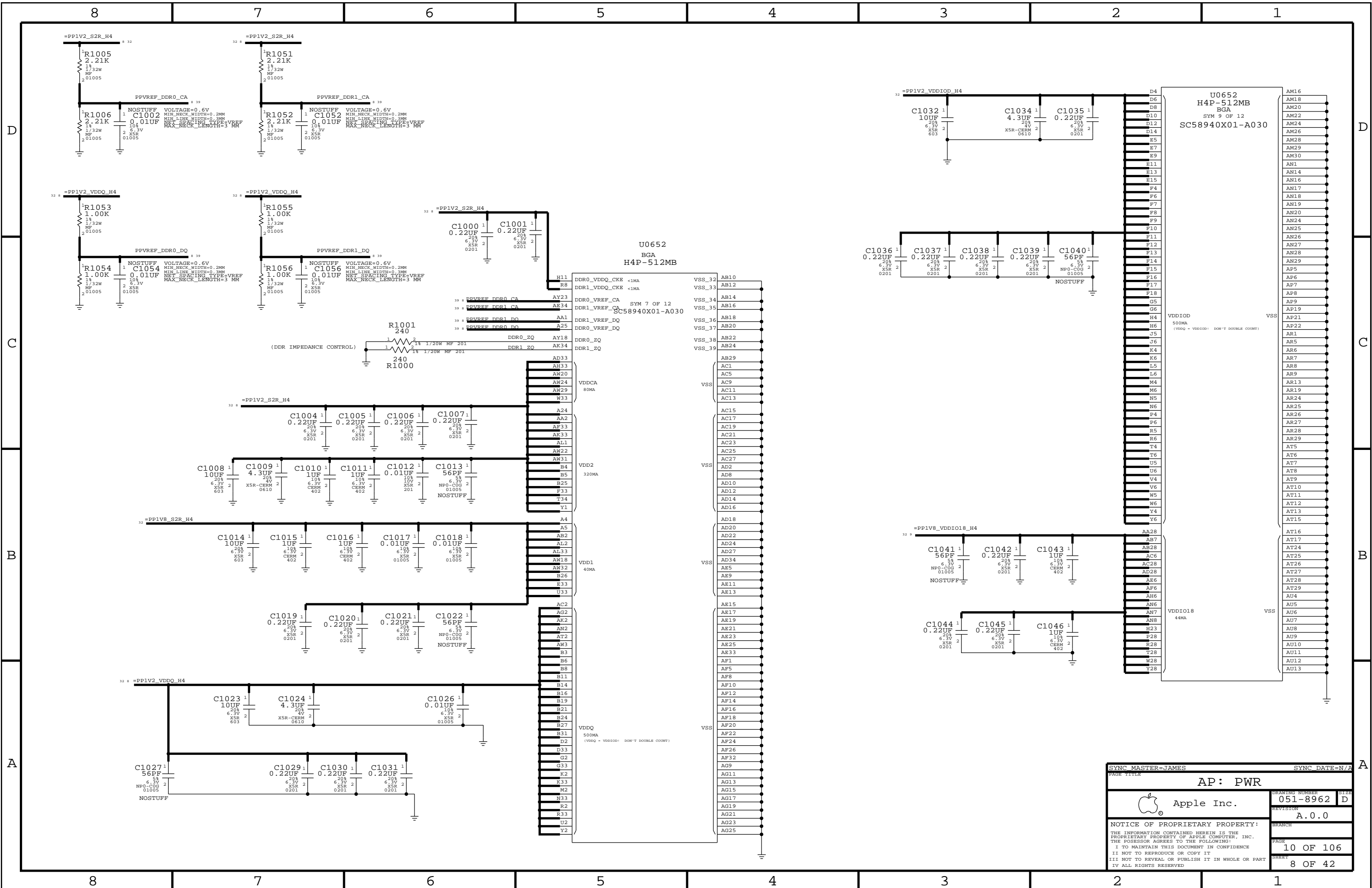
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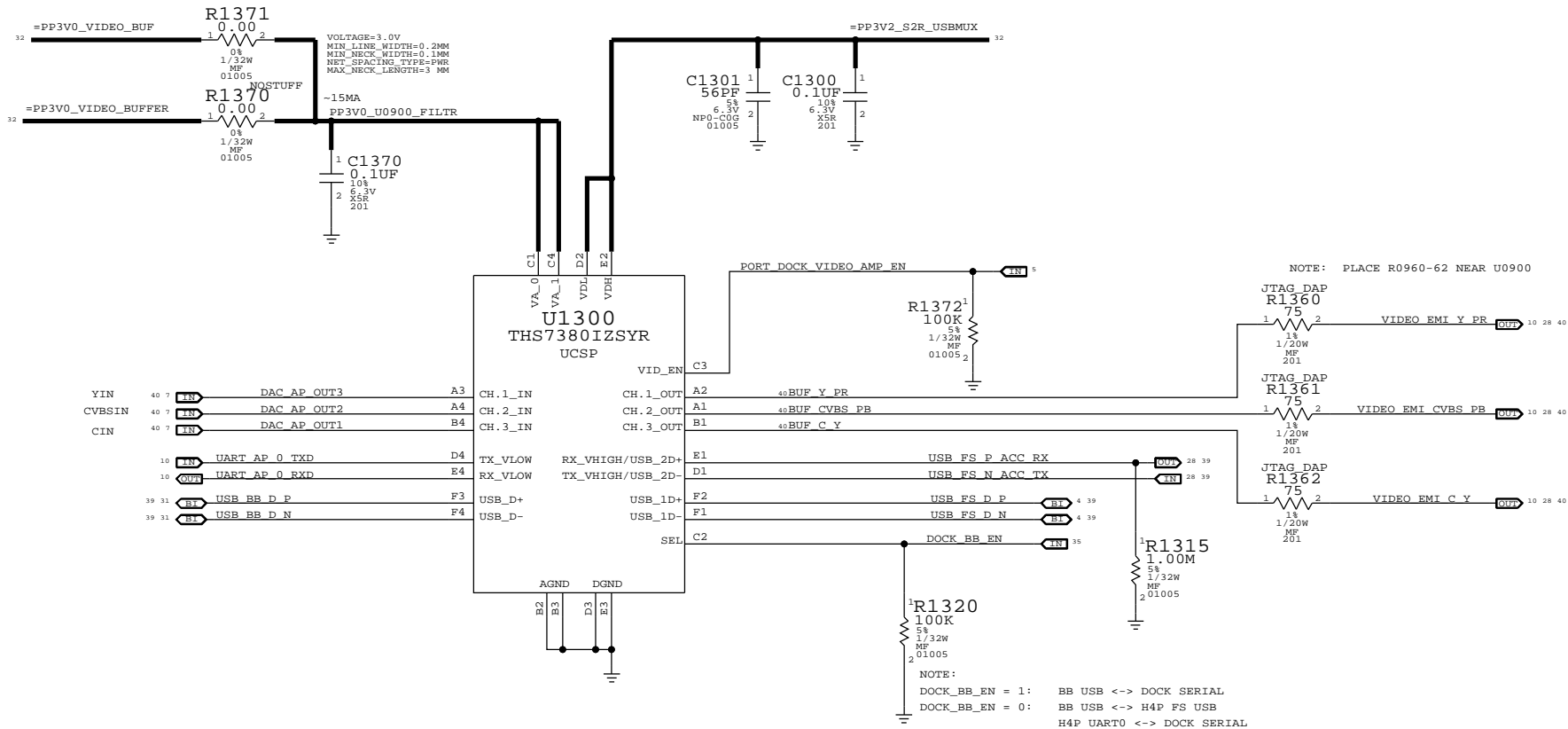


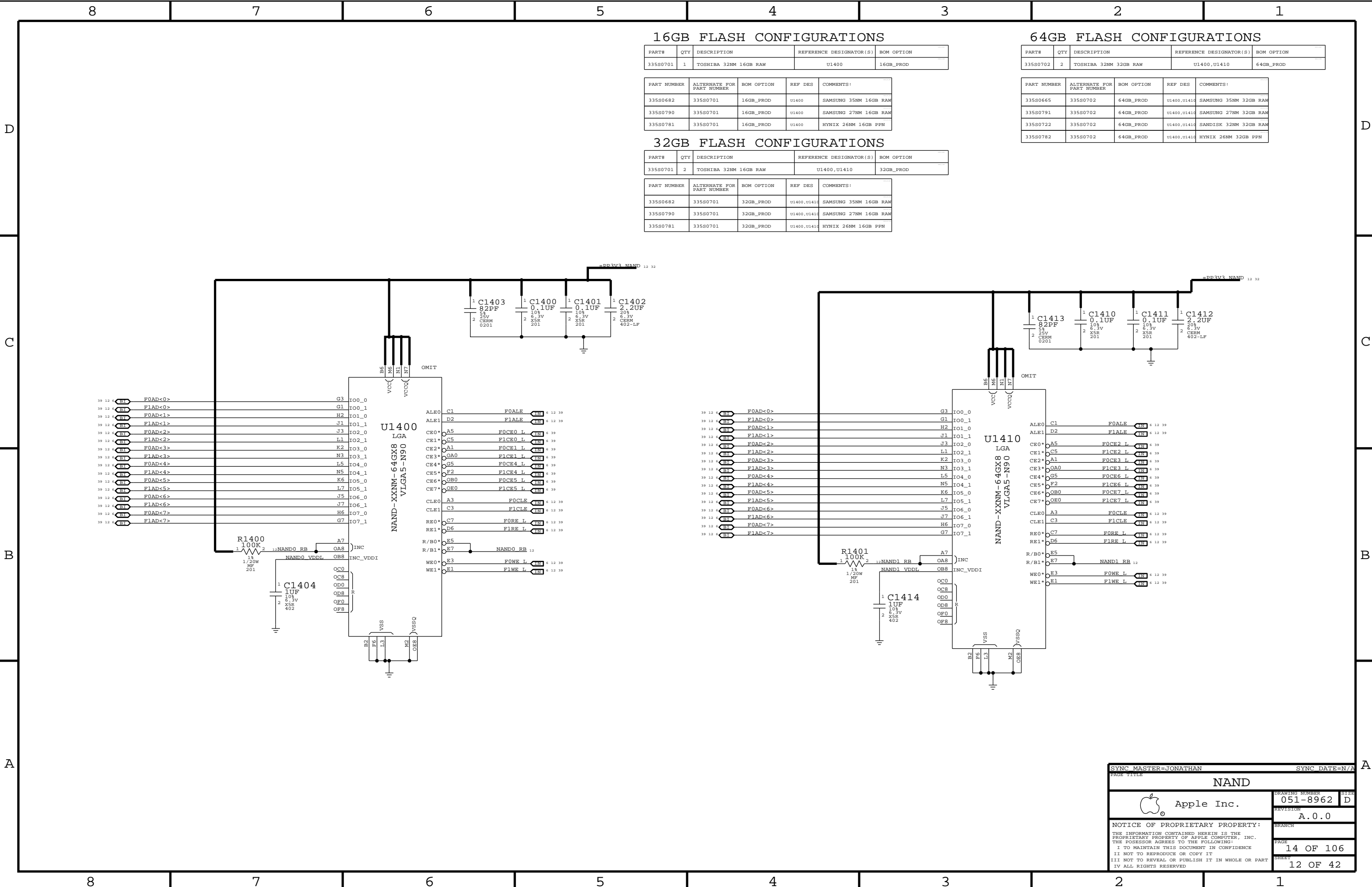






NOTE:  
LDO3 PROVIDES 50MA TO BOTH H4P AND U1300  
IF THAT'S NOT ENOUGH, STUFF R1371 AND NOSTUFF R1370





16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	1	TOSHIBA 32NM 16GB RAW	U1400	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	16GB_PROD	U1400	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	16GB_PROD	U1400	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	16GB_PROD	U1400	HYNIX 26NM 16GB PPN

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	2	TOSHIBA 32NM 16GB RAW	U1400,U1410	32GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	32GB_PROD	U1400,U1410	HYNIX 26NM 16GB PPN

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0702	2	TOSHIBA 32NM 32GB RAW	U1400,U1410	64GB_PROD


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0665	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 35NM 32GB RAW
335S0791	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 27NM 32GB RAW
335S0722	335S0702	64GB_PROD	U1400,U1410	SANDISK 32NM 32GB RAW
335S0782	335S0702	64GB_PROD	U1400,U1410	HYNIX 26NM 32GB PPN

SYNC MASTER=JONATHAN

SYNC DATE=N/A

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NAND

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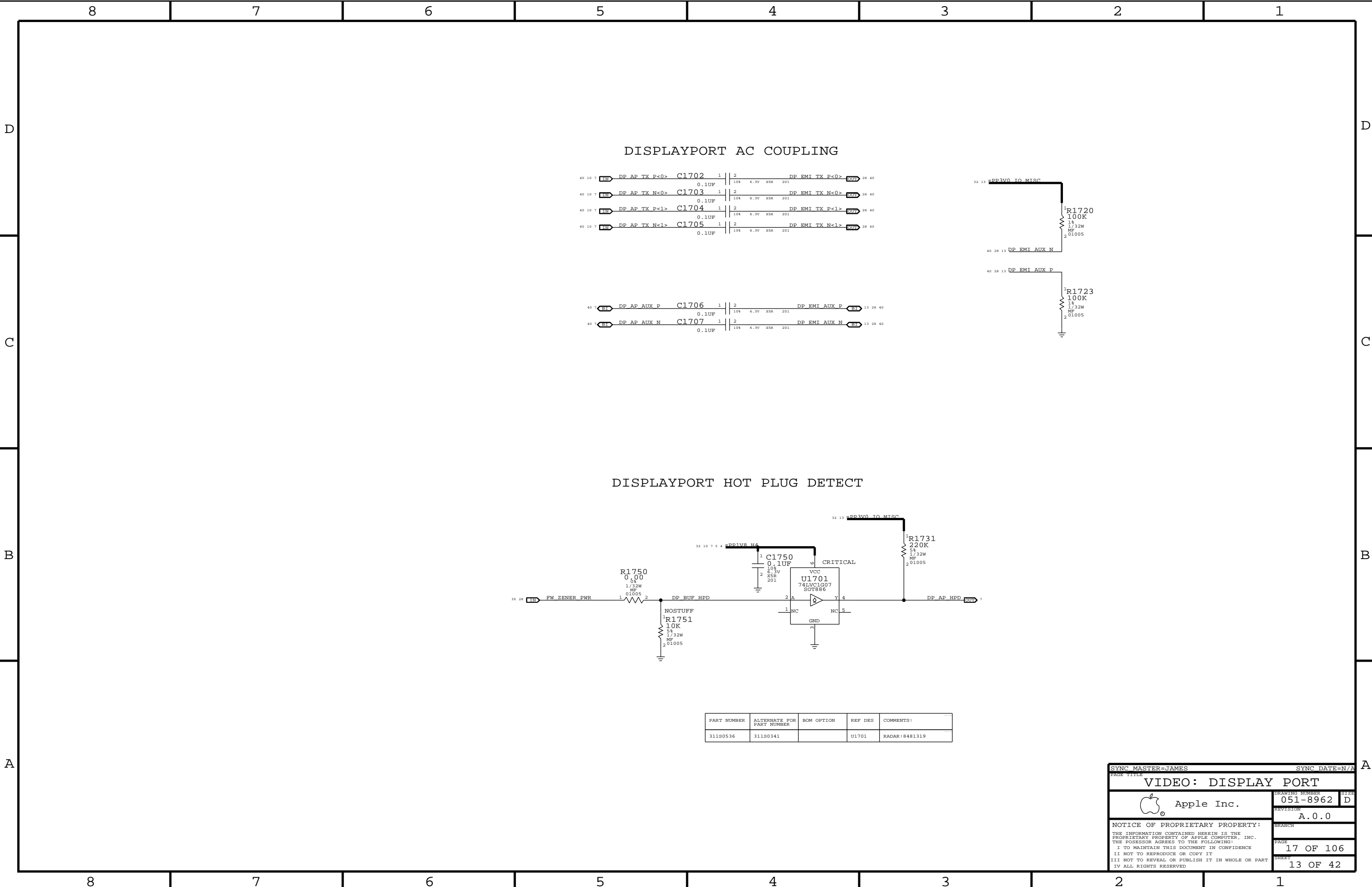
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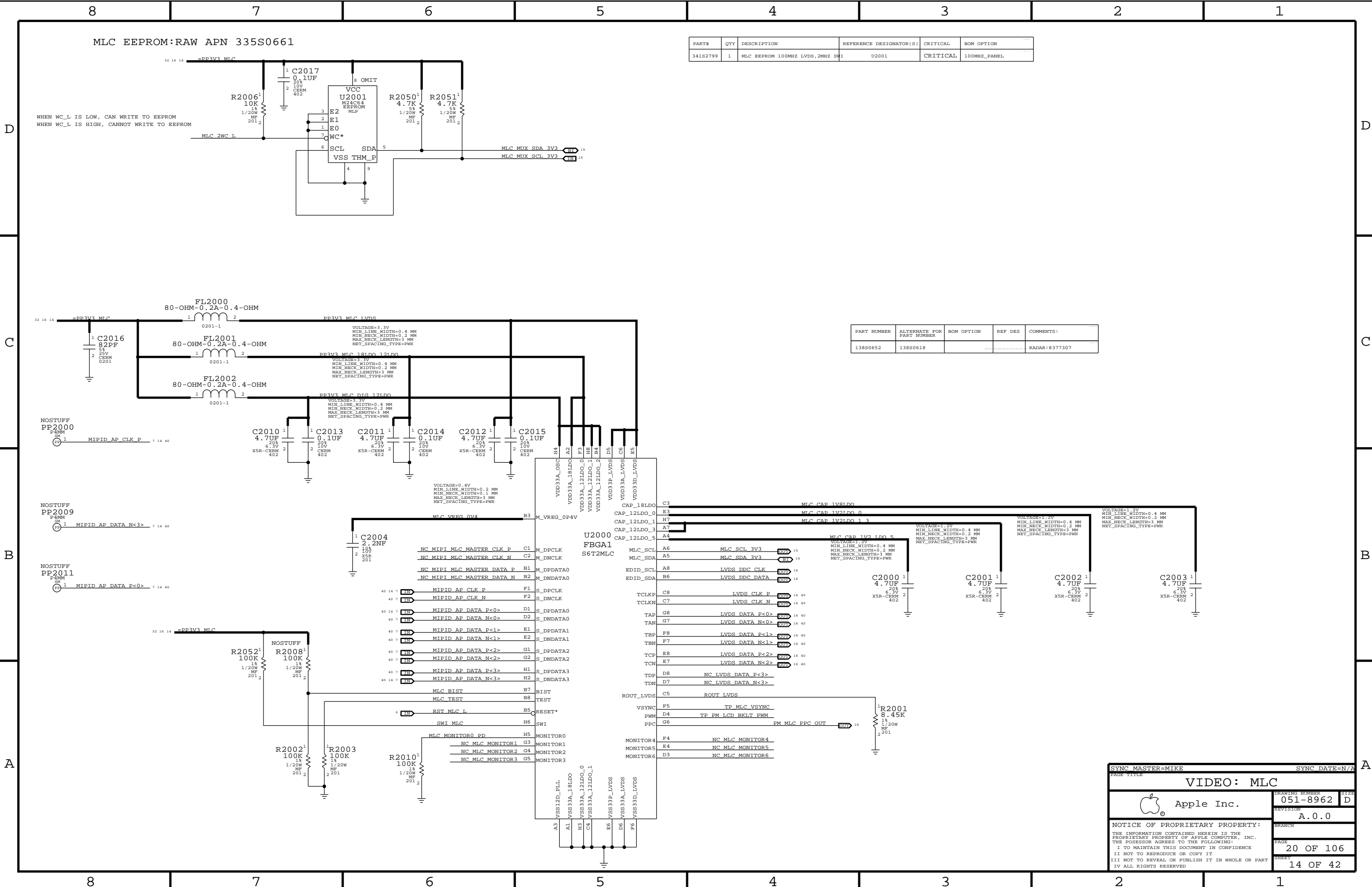
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2799	1	MLC EEPROM 100MHZ LVDS, 2MHZ SWI	U2001	CRITICAL	100MHZ_PANEL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0618			RADAR:8377307

SYNC MASTER=MIKE

SYNC DATE=N/A

VIDEO: MLC

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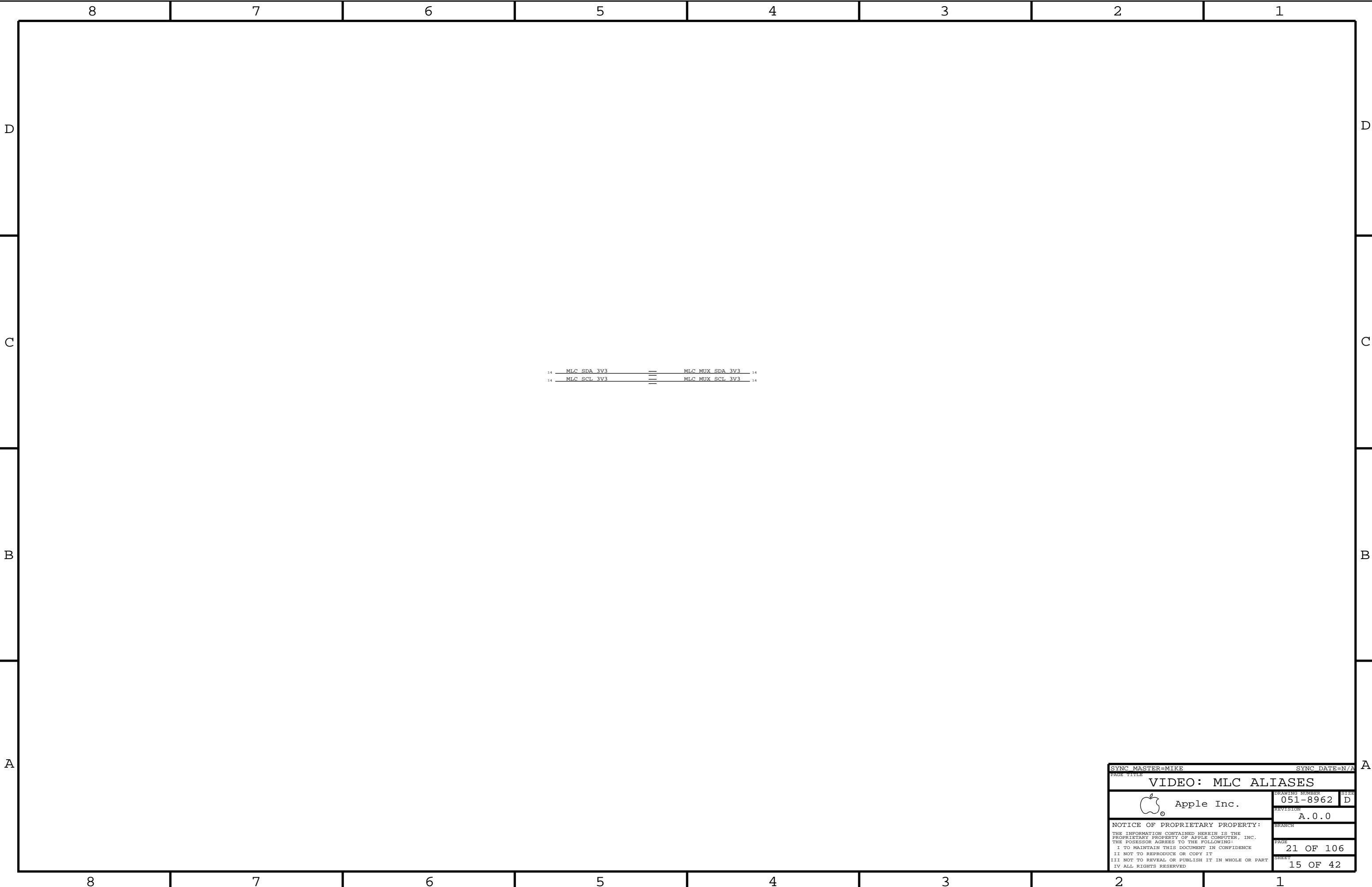
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14 MLC\_SDA\_3V3 == MLC\_MUX\_SDA\_3V3 14  
14 MLC\_SCL\_3V3 == MLC\_MUX\_SCL\_3V3 14

SYNC\_MASTER=MIKE

SYNC\_DATE=N/A

PAGE\_TITLE

VIDEO: MLC ALIASES



Apple Inc.

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DRAWING\_NUMBER

051-8962

SIZE

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REVISION

A.0.0

BRANCH

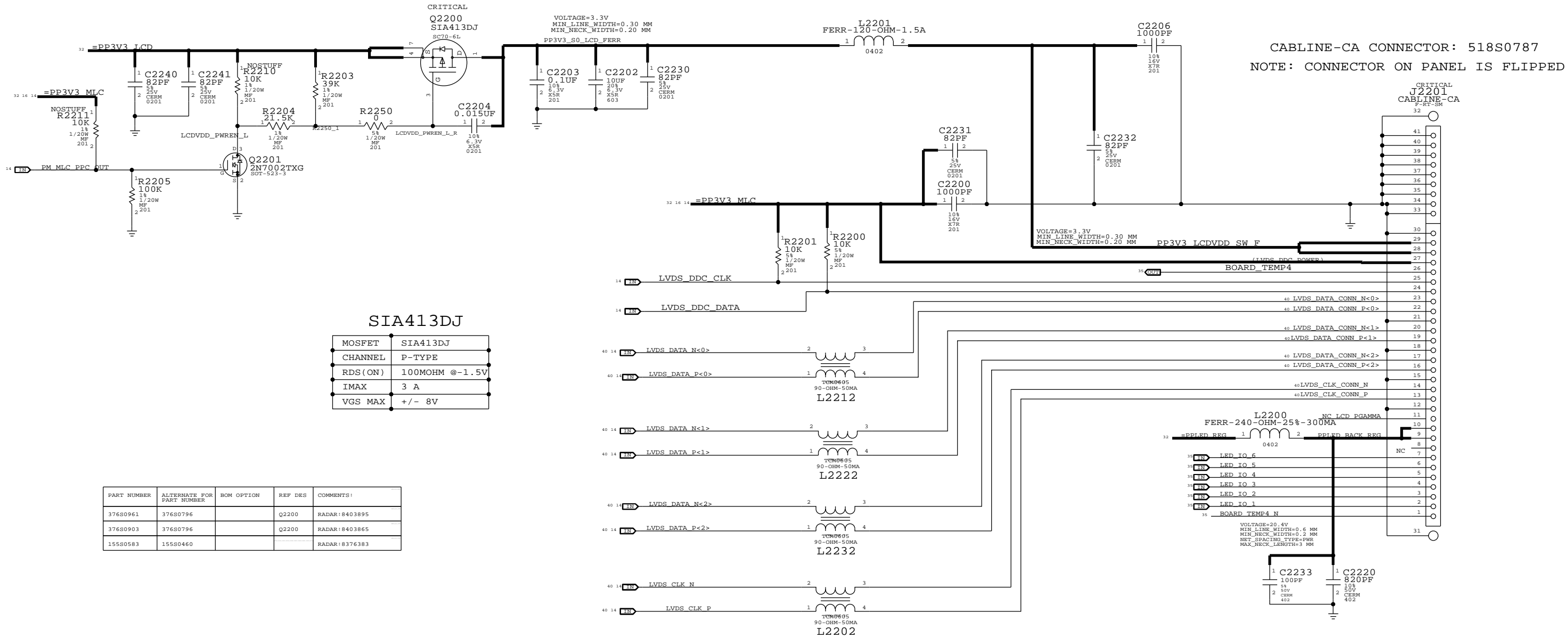
PAGE

21 OF 106


SHEET

15 OF 42

# LVDS CONNECTOR



NOSTUFF RESISTORS ARE THERE TO INVESTIGATE POSSIBILITY OF REMOVING THE CHOKE

SYNC MASTER=ALEX		SYNC DATE=N/A	
PAGE TITLE			
VIDEO: LVDS CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-8962
		REVISION	A.0.0
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BRANCH			
PAGE		22 OF 106	
SHEET		16 OF 42	

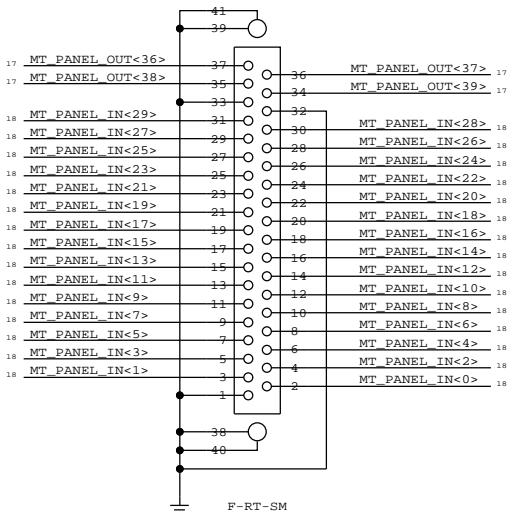


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

18 MUX_IN<0>	B1	MUX0	VSTM0	A1	MT_PANEL_OUT<0>	17
18 MUX_IN<1>	C1	MUX1	VSTM1	B2	MT_PANEL_OUT<1>	17
18 MUX_IN<2>	E1	MUX2	VSTM2	C2	MT_PANEL_OUT<2>	17
18 MUX_IN<3>	F2	MUX3	VSTM3	D1	MT_PANEL_OUT<3>	17
18 MUX_IN<4>	H1	MUX4	VSTM4	D2	MT_PANEL_OUT<4>	17
18 MUX_IN<5>	J1	MUX5	VSTM5	E2	MT_PANEL_OUT<5>	17
18 MUX_IN<6>	J2	MUX6	VSTM6	F1	MT_PANEL_OUT<6>	17
18 MUX_IN<7>	J3	MUX7	VSTM7	G1	MT_PANEL_OUT<7>	17
18 MUX_IN<8>	K4	MUX8	VSTM8	G2	MT_PANEL_OUT<8>	17
18 MUX_IN<9>	H5	MUX9	VSTM9	I1	MT_PANEL_OUT<9>	17
18 MUX_IN<10>	I5	MUX10	VSTM10	H2	MT_PANEL_OUT<10>	17
18 MUX_IN<11>	J8	MUX11	VSTM11	I2	MT_PANEL_OUT<11>	17
18 MUX_IN<12>	J9	MUX12	VSTM12	K1	MT_PANEL_OUT<12>	17
18 MUX_IN<13>	K8	MUX13	VSTM13	K2	MT_PANEL_OUT<13>	17
18 MUX_IN<14>	J10	MUX14	VSTM14	I3	MT_PANEL_OUT<14>	17
18 MUX_IN<15>	I10	MUX15	VSTM15	K3	MT_PANEL_OUT<15>	17
18 MUX_IN<16>	H10	MUX16	VSTM16	J4	MT_PANEL_OUT<16>	17
18 MUX_IN<17>	F11	MUX17	VSTM17	I4	MT_PANEL_OUT<17>	17
18 MUX_IN<18>	C11	MUX18	VSTM18	K6	MT_PANEL_OUT<18>	17
18 MUX_IN<19>	E10	MUX19	VSTM19	H6	MT_PANEL_OUT<19>	17
NC	A11	MUX20	VSTM20	K5	MT_PANEL_OUT<20>	17
NC	B4	MUX21	VSTM21	J5	MT_PANEL_OUT<21>	17
NC	A5	MUX22	VSTM22	I7	MT_PANEL_OUT<22>	17
NC	A2	MUX23	VSTM23	K9	MT_PANEL_OUT<23>	17
18 Z1_BON_L<0>	C7	BON_L0	VSTM24	I8	MT_PANEL_OUT<24>	17
18 Z1_BON_L<1>	A7	BON_L1	VSTM25	K10	MT_PANEL_OUT<25>	17
18 Z1_BON_L<2>	B7	BON_L2	VSTM26	I6	MT_PANEL_OUT<26>	17
18 Z1_BON_L<3>	B8	BON_L3	VSTM27	J7	MT_PANEL_OUT<27>	17
18 Z1_BON_L<4>	A8	BON_L4	VSTM28	K11	MT_PANEL_OUT<28>	17
18 Z1_BON_L<5>	C8	BON_L5	VSTM29	I9	MT_PANEL_OUT<29>	17
NC	C6		VSTM30	J11	MT_PANEL_OUT<30>	17
NC	D3		VSTM31	I11	MT_PANEL_OUT<31>	17
NC	D4		VSTM32	H11	MT_PANEL_OUT<32>	17
NC	D5		VSTM33	G11	MT_PANEL_OUT<33>	17
NC	D6		VSTM34	G10	MT_PANEL_OUT<34>	17
NC	D8		VSTM35	F10	MT_PANEL_OUT<35>	17
NC	D9		VSTM36	C10	MT_PANEL_OUT<36>	17
NC	E4		VSTM37	D10	MT_PANEL_OUT<37>	17
NC	E8		VSTM38	E11	MT_PANEL_OUT<38>	17
NC	F4		VSTM39	D11	MT_PANEL_OUT<39>	17
NC	F5		VSTM40	B11	NC	
NC	F8		VSTM41	B10	NC	
NC	F9		VSTM42	C4	NC	
NC	G3		VSTM43	A4	NC	
NC	G4		VSTM44	B5	NC	
NC	G9		VSTM46	A3	NC	
NC	H3		VSTM45	C5	NC	
NC	H4		VSTM47	B3	NC	
NC	H7			A_AD_R0	A10	Z1_B_ADR<0>
NC	H8			A_AD_R1	B9	Z1_B_ADR<1>
NC	H9			A_AD_R2	A9	Z1_B_ADR<2>
NC	J6					
NC	K7					

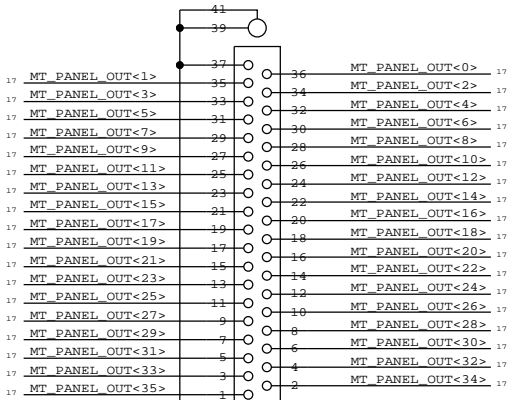
## CONNECTORS TO GRAPE FLEX

P/N 518S0817



F-RT-SM  
502250-8237  
J3010

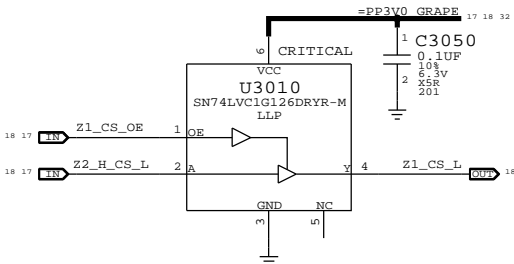
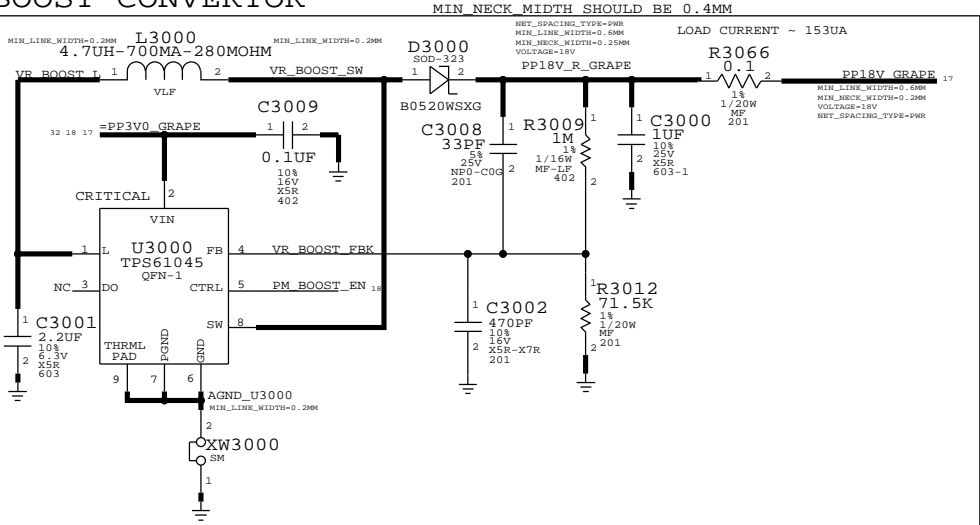
MATES WITH LEFTMOST GRAPE FLEX TAIL



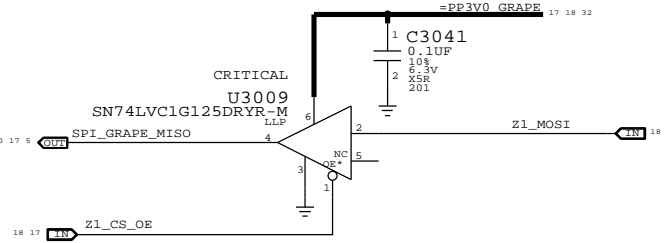
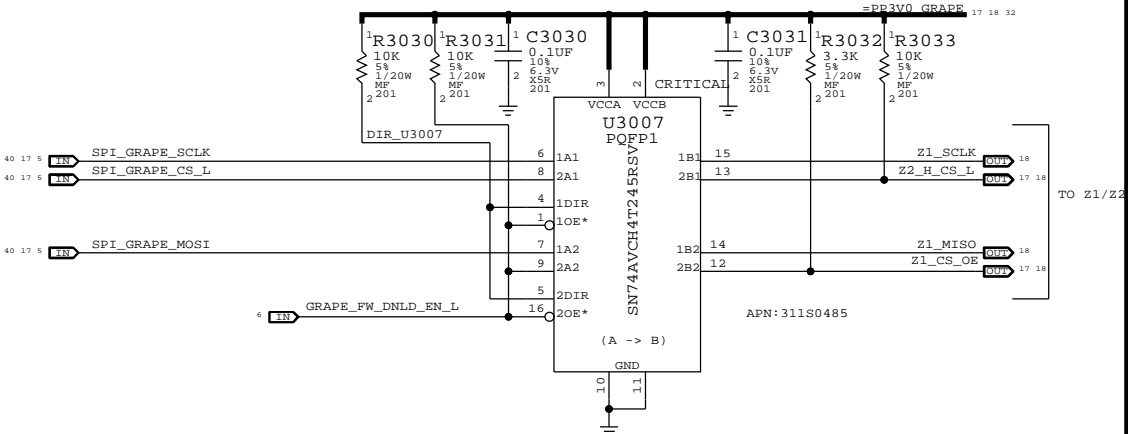
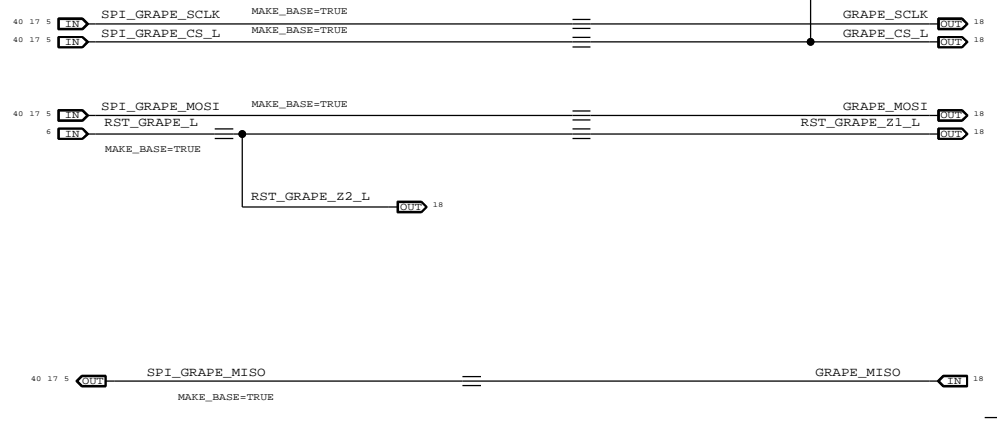
F-RT-SM  
502250-8237  
J3011

MATES WITH RIGHTMOST GRAPE FLEX TAIL

## BOOST CONVERTOR

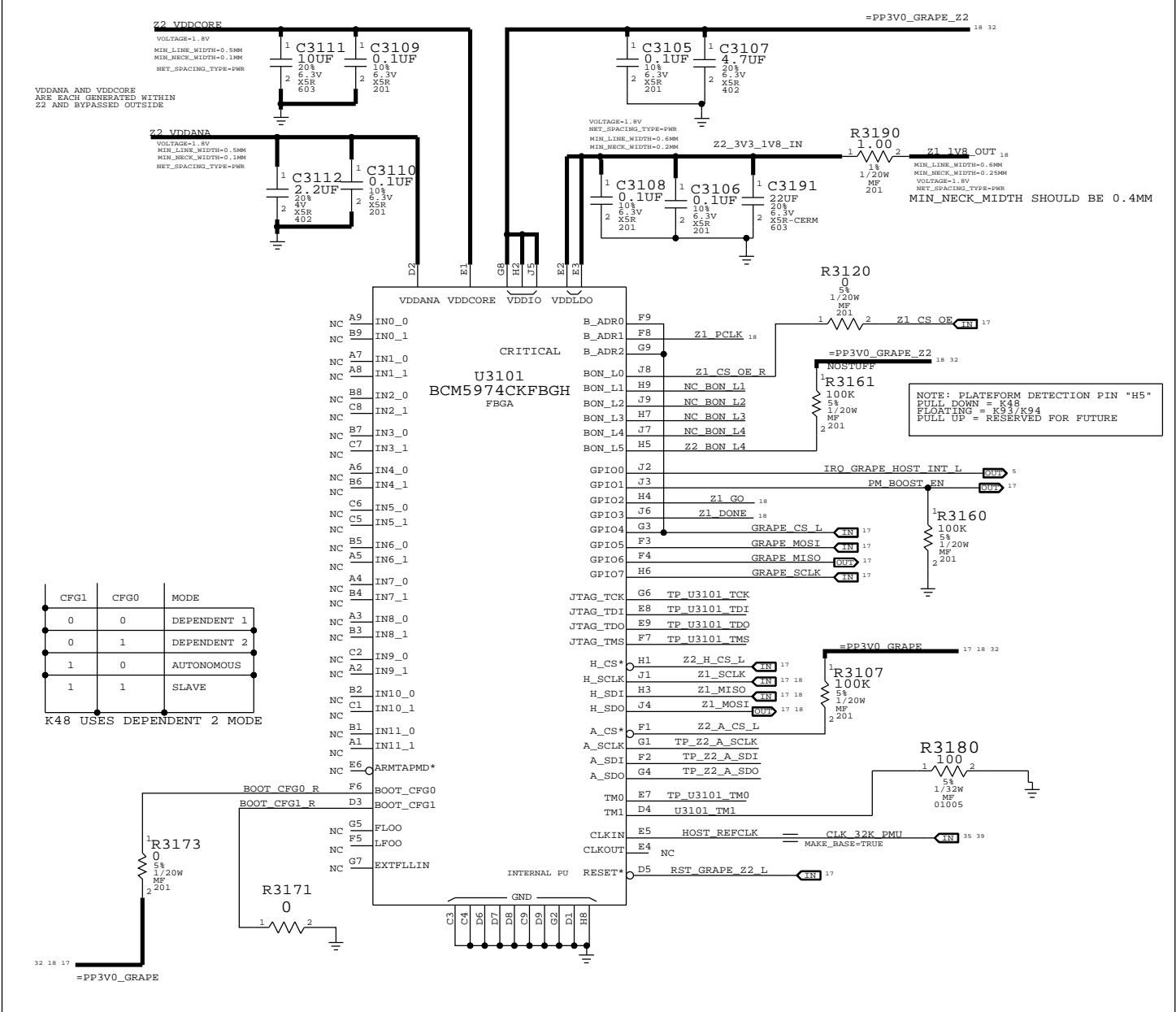


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31180525	31180532		U3010	



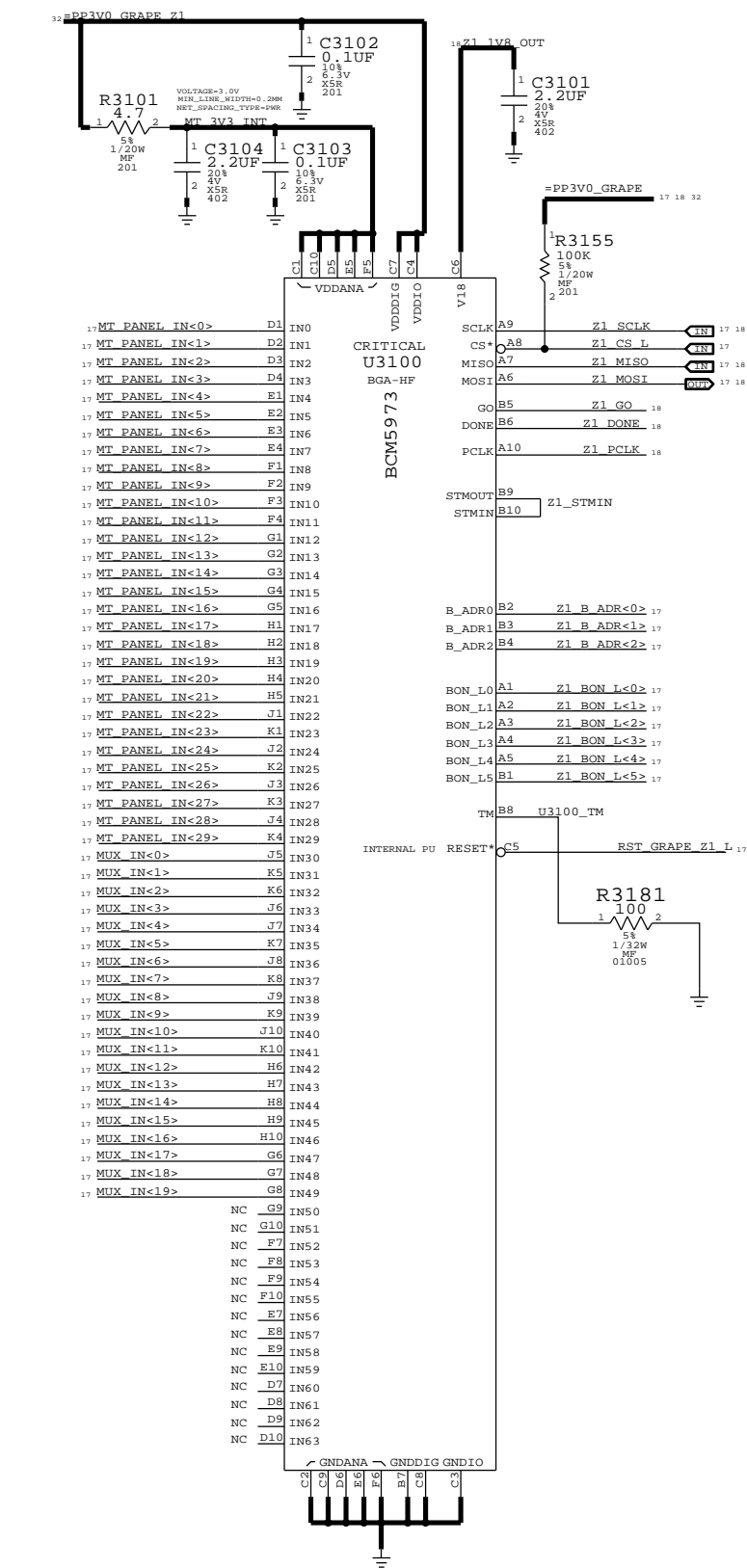
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GRAPE: GROUNDHOG, CONN, BOOST		DRAWING NUMBER	
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		17 OF 42	


ARM9 MCU (Z2 BASED)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0648		C3107	RADAR: 8392120
138S0618	138S0648		C3107	BOM CONSOLIDATION

ZEPHYR 1+ ASIC



SYNC MASTER=RAMSIN		SYNC DATE=N/A	
PAGE TITLE			
GRAPE: Z1, Z2			
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		SIZE	D
		REVISION	A.0.0
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		PAGE	31 OF 106
		SHEET	18 OF 42

## D



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A

SPEAKER AMPLIFIER

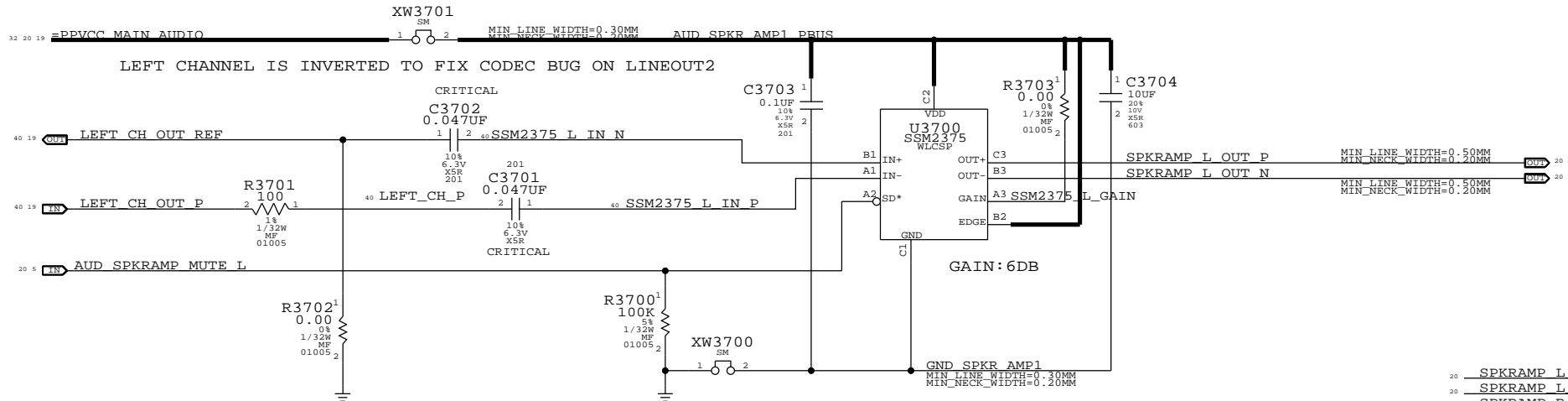
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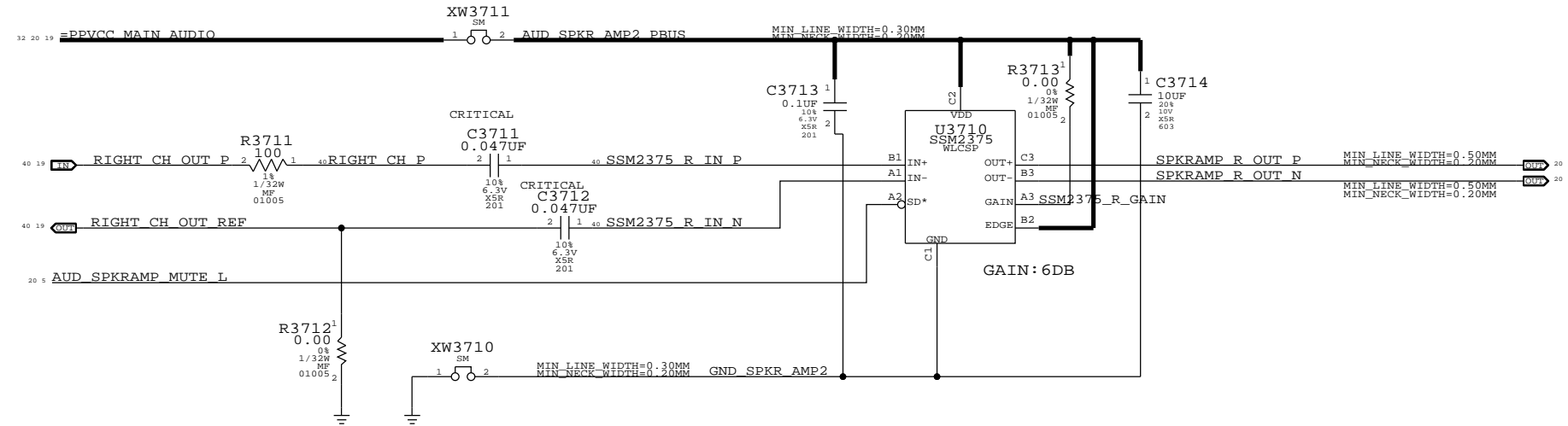
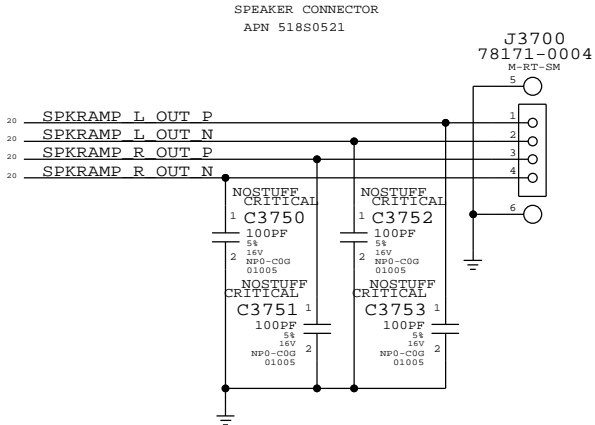
80HZ +/- XXX%


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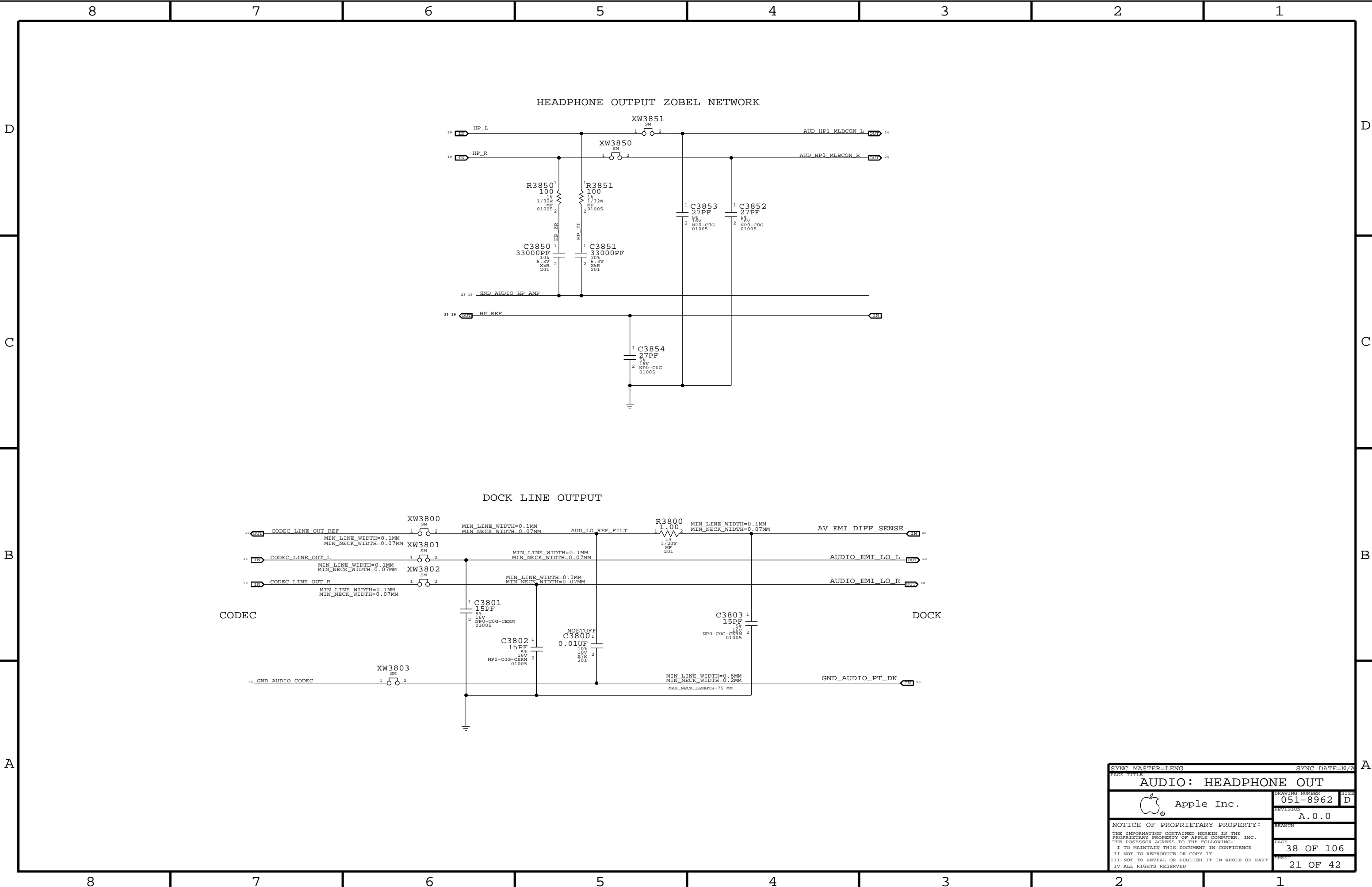
GAIN	VDD	GND
12DB	47K	NC
9DB	NC	47K
6DB	SHORT	NC
3DB	NC	NC
0DB	NC	SHORT



L63 LINEOUT2A IS CONNECTED TO U3700  
L63 LINEOUT2B IS CONNECTED TO U3710




SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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		PAGE	37 OF 106
		SHEET	20 OF 42



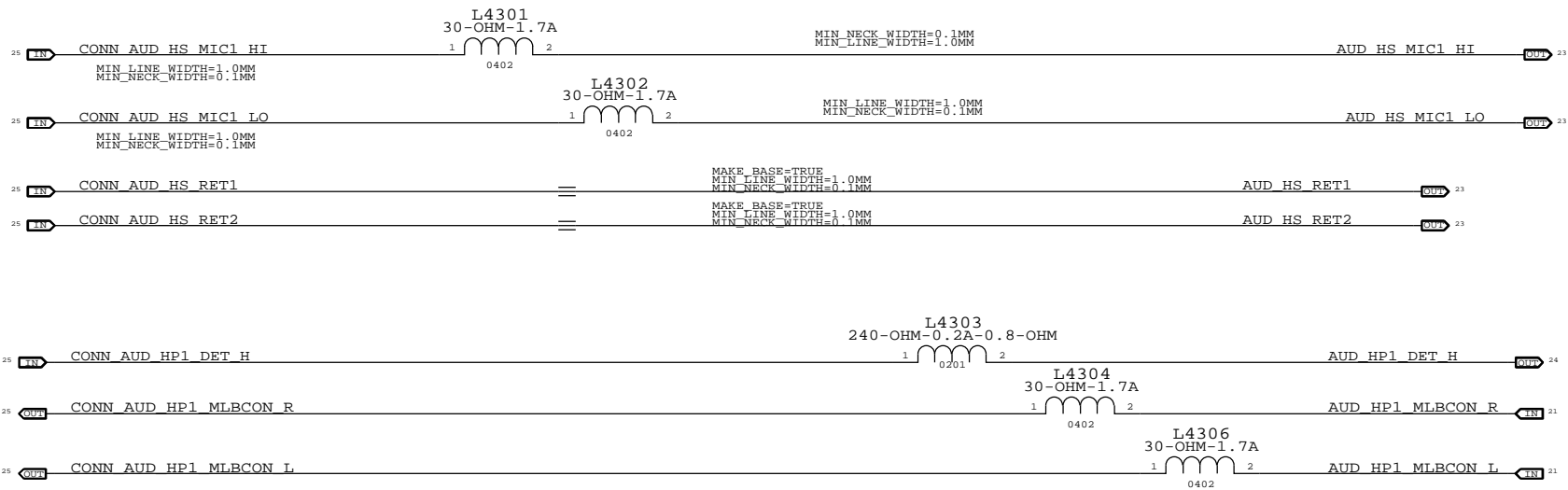


The schematic diagram illustrates the U4200 TS3A8235YFP W CSP microphone amplifier circuit. The central component is the U4200 IC, which is connected to VDD and GND. The circuit includes several resistors (R4201, R4202, R4203, R4212, R4213) and capacitors (C4200, C4201, C4211, C4212, C4213, C4217) for signal conditioning and filtering. The input stage features a microphone (MIC1, MIC2) connected to the MIC1 and MIC2 pins of the U4200. The output stage includes a low-pass filter (EXT MIC LPF FC = 677KHZ) and a buffer (EXT MIC P, EXT MIC REF). The circuit is powered by a 3.3V supply (PP3V0\_S2R\_HALL\_CHSW) and a 1.8V supply (HP\_REF). The output is connected to the CHS\_SCL and CHS\_SDA pins of the U4200.

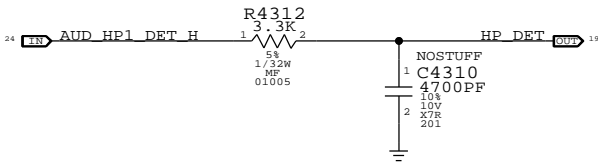
EXT MIC LPF FC = 677KHZ

SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TYPE		PAGE NO.	
AUDIO: DETECT/MIC BIAS			
 Apple Inc.		DRAWING NUMBER 051-8962	
		SIZE D	
		REVISION A.0.0	
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HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29  
PLACE ALL COMPONENTS NEAR J5501



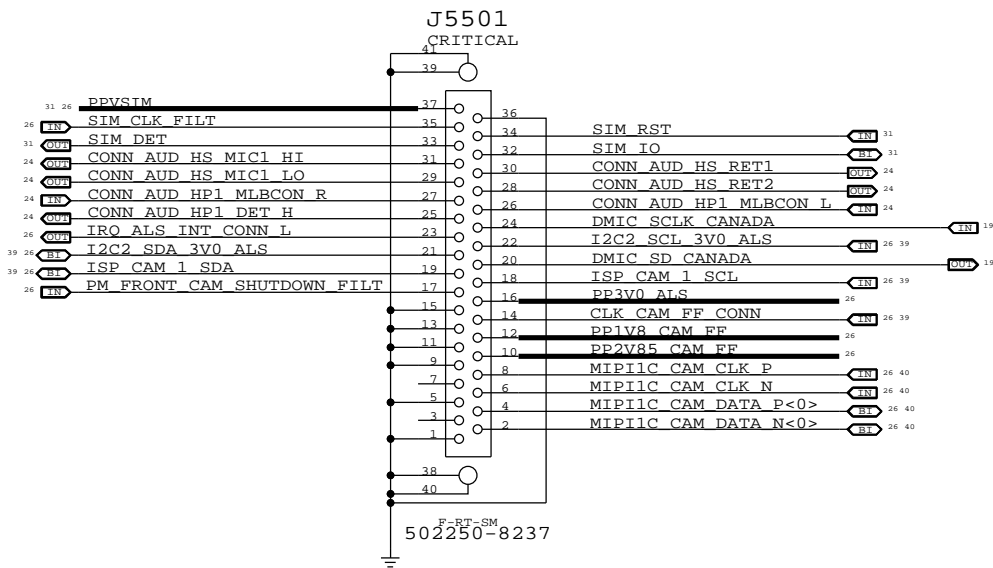
HEADSET JACK INSERTION DETECT





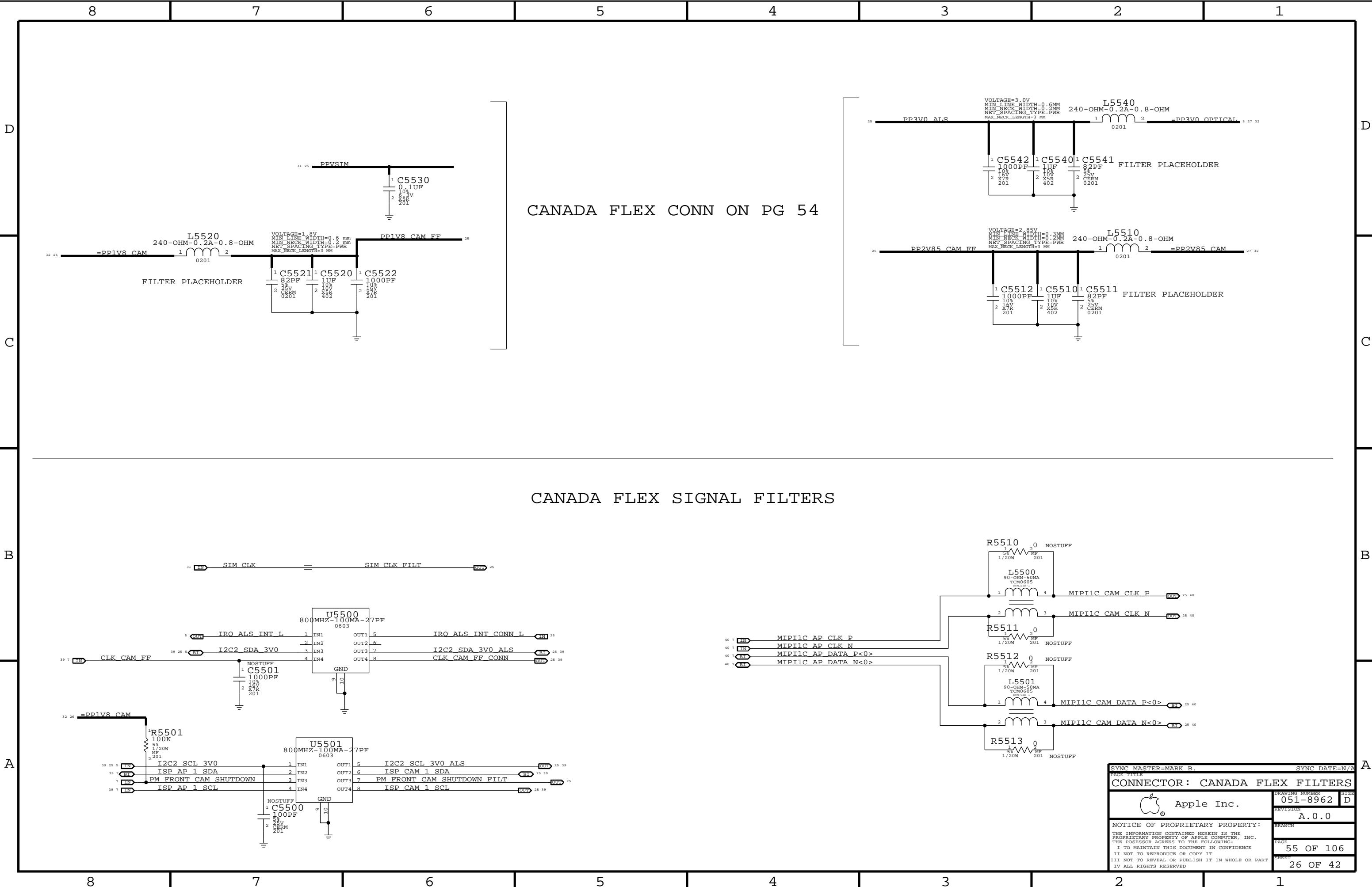
CANADA FLEXES CONN.

APN: 518S0817




SENSOR BOARD CONN ALIASES

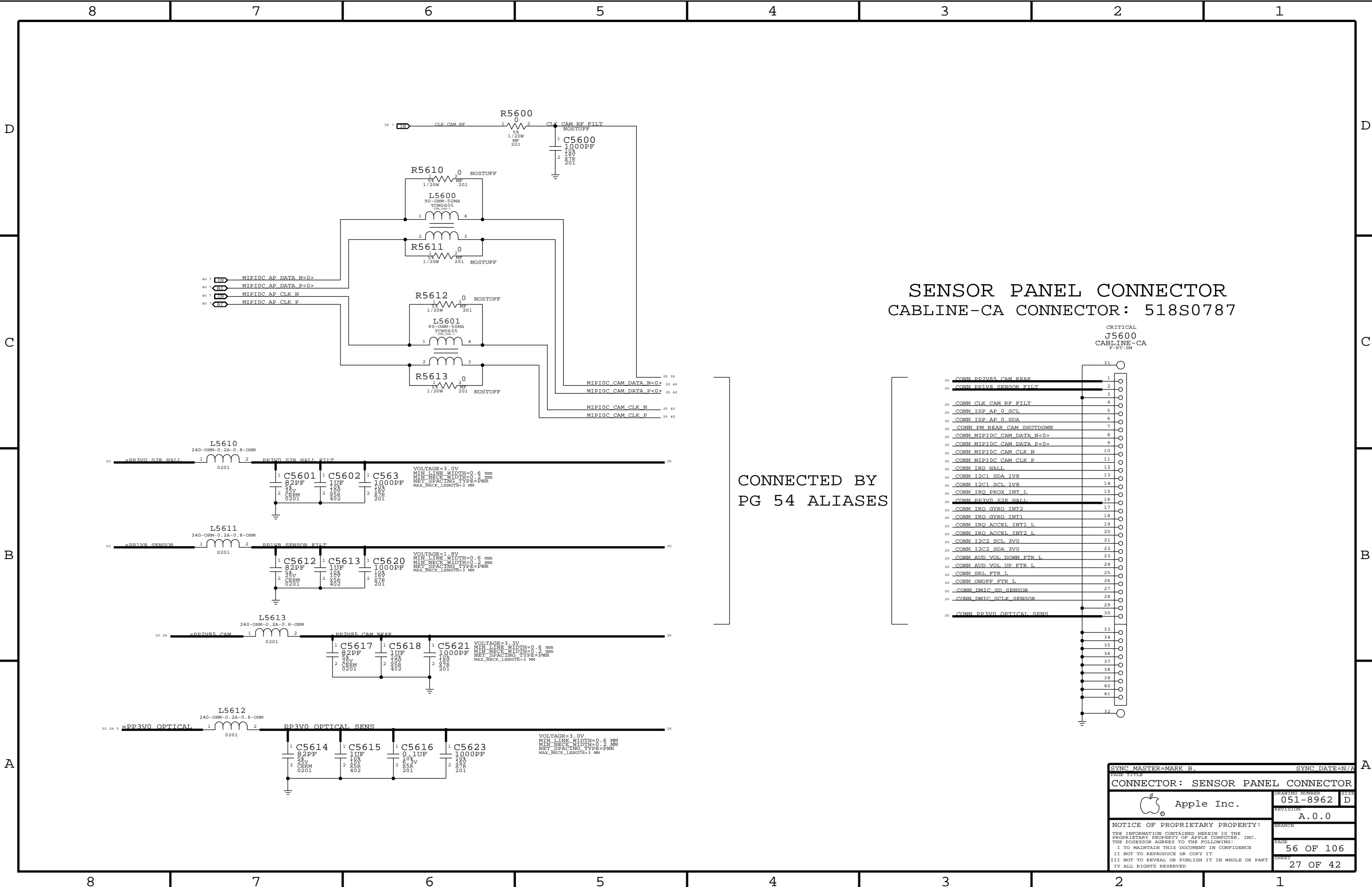
39	27	CLK CAM RF FILT	==	CONN CLK CAM RF FILT	27	
40	27	MIPI0C CAM DATA N<0>	MAKE_BASE=TRUE	==	CONN MIPI0C CAM DATA N<0>	27
40	27	MIPI0C CAM DATA P<0>	MAKE_BASE=TRUE	==	CONN MIPI0C CAM DATA P<0>	27
40	27	MIPI0C CAM CLK N	MAKE_BASE=TRUE	==	CONN MIPI0C CAM CLK N	27
40	27	MIPI0C CAM CLK P	MAKE_BASE=TRUE	==	CONN MIPI0C CAM CLK P	27
7	7	PM REAR CAM SHUTDOWN	MAKE_BASE=TRUE	==	CONN PM REAR CAM SHUTDOWN	27
27	27	PP1V8 SENSOR FILT	MAKE_BASE=TRUE	==	CONN PP1V8 SENSOR FILT	27
27	27	PP2V85 CAM REAR	MAKE_BASE=TRUE	==	CONN PP2V85 CAM REAR	27
19	19	DMIC SD SENSOR	MAKE_BASE=TRUE	==	CONN DMIC SD SENSOR	27
19	19	DMIC SCLK SENSOR	MAKE_BASE=TRUE	==	CONN DMIC SCLK SENSOR	27
39	7	ISP AP 0 SCL	MAKE_BASE=TRUE	==	CONN ISP AP 0 SCL	27
39	7	ISP AP 0 SDA	MAKE_BASE=TRUE	==	CONN ISP AP 0 SDA	27
39	26	I2C2 SCL 3V0	MAKE_BASE=TRUE	==	CONN I2C2 SCL 3V0	27
39	26	I2C2 SDA 3V0	MAKE_BASE=TRUE	==	CONN I2C2 SDA 3V0	27
5	5	IRO ACCEL INT1 L	MAKE_BASE=TRUE	==	CONN IRO ACCEL INT1 L	27
5	5	IRO ACCEL INT2 L	MAKE_BASE=TRUE	==	CONN IRO ACCEL INT2 L	27
5	5	IRO GYRO INT1	MAKE_BASE=TRUE	==	CONN IRO GYRO INT1	27
5	5	IRO GYRO INT2	MAKE_BASE=TRUE	==	CONN IRO GYRO INT2	27
39	5	I2C1 SCL 1V8	MAKE_BASE=TRUE	==	CONN I2C1 SCL 1V8	27
39	5	I2C1 SDA 1V8	MAKE_BASE=TRUE	==	CONN I2C1 SDA 1V8	27
35	35	IRO HALL	MAKE_BASE=TRUE	==	CONN IRO HALL	27
35	35	IRO PROX INT L	MAKE_BASE=TRUE	==	CONN IRO PROX INT L	27
27	27	PP3V0 S2R HALL FILT	MAKE_BASE=TRUE	==	CONN PP3V0 S2R HALL	27
15	5	ONOFF L	MAKE_BASE=TRUE	==	CONN ONOFF FTR L	27
15	5	SRL L	MAKE_BASE=TRUE	==	CONN SRL FTR L	27
15	5	AUD VOL UP L	MAKE_BASE=TRUE	==	CONN AUD VOL UP FTR L	27
15	5	AUD VOL DOWN L	MAKE_BASE=TRUE	==	CONN AUD VOL DOWN FTR L	27
27	27	PP3V0 OPTICAL SENS	MAKE_BASE=TRUE	==	CONN PP3V0 OPTICAL SENS	27



CANADA FLEX CONN ON PG 54

CANADA FLEX SIGNAL FILTERS

SYNC MASTER=MARK B.		SYNC DATE=N/A	
PAGE TITLE			
CONNECTOR: CANADA FLEX FILTERS			
 Apple Inc.		DRAWING NUMBER	051-8962
		REVISION	A.0.0
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		PAGE	55 OF 106
		SHEET	26 OF 42




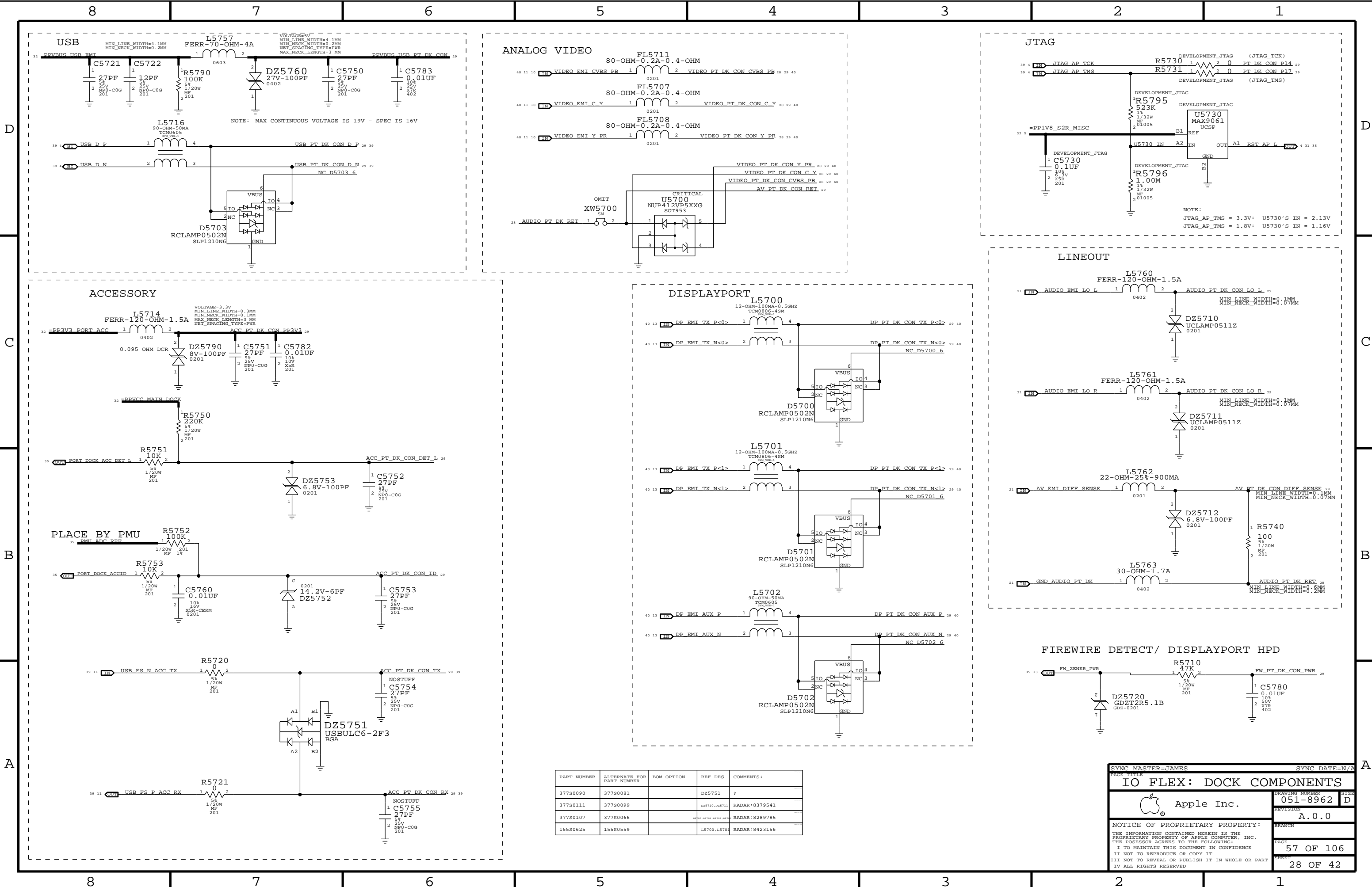
SENSOR PANEL CONNECTOR  
CABLINE-CA CONNECTOR: 518S0787

CRITICAL  
J5600  
CABLINE-CA  
F-RT-SM

CONNECTED BY  
PG 54 ALIASES

CONN PP2V85 CAM REAR	1
CONN PP1V8 SENSOR FILT	2
	3
CONN CLK CAM RF FILT	4
CONN ISP AP 0 SCL	5
CONN ISP AP 0 SDA	6
CONN PM REAR CAM SHUTDOWN	7
CONN MIPI0C CAM DATA N<0>	8
CONN MIPI0C CAM DATA P<0>	9
CONN MIPI0C CAM CLK N	10
CONN MIPI0C CAM CLK P	11
CONN IRO HALL	12
CONN I2C1 SDA 1V8	13
CONN I2C1 SCL 1V8	14
CONN IRO PROX INT L	15
CONN PP3V0 S2R HALL	16
CONN IRO GYRO INT2	17
CONN IRO GYRO INT1	18
CONN IRO ACCEL INT1 L	19
CONN IRO ACCEL INT2 L	20
CONN I2C2 SCL 3V0	21
CONN I2C2 SDA 3V0	22
CONN AUD VOL DOWN FTR L	23
CONN AUD VOL UP FTR L	24
CONN SRL FTR L	25
CONN ONOFF FTR L	26
CONN DMIC SD SENSOR	27
CONN DMIC SCLK SENSOR	28
	29
CONN PP3V0 OPTICAL SENS	30
	31
	32
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	41
	42

SYNC MASTER=MARK B.		SYNC DATE=N/A	
PAGE TITLE			
CONNECTOR: SENSOR PANEL CONNECTOR			
 Apple Inc.	DRAWING NUMBER		SIZE
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	REVISION		A.0.0
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SHEET		27 OF 42	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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377S0111	377S0099		DZ5710, DZ5711	RADAR: 8379541
377S0107	377S0066		DZ5710, DZ5711, DZ5712	RADAR: 8289785
155S0625	155S0559		L5700, L5701	RADAR: 8423156

SYNC MASTER=JAMES

SYNC DATE=N/A

IO FLEX: DOCK COMPONENTS

Apple Inc.

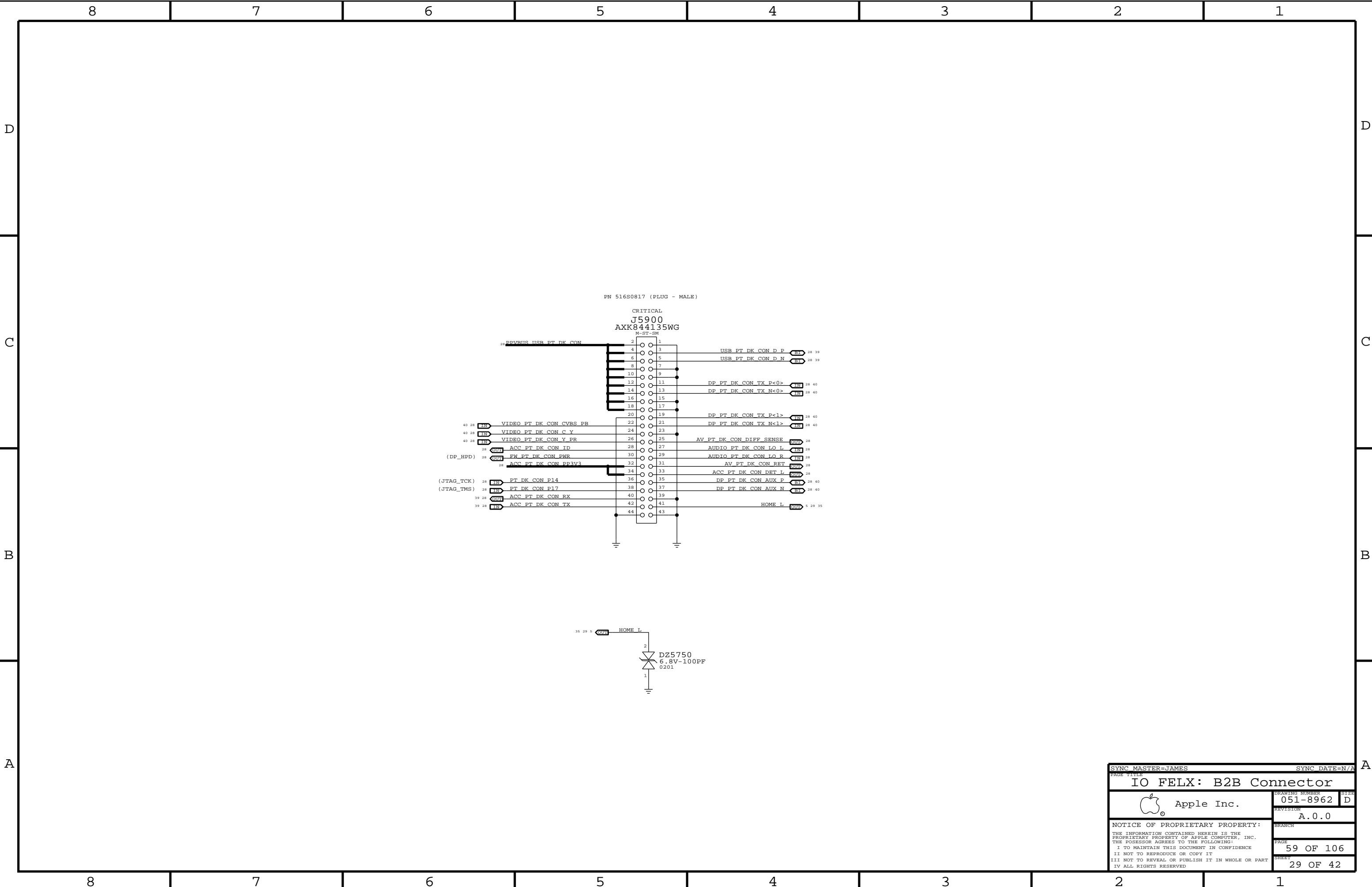
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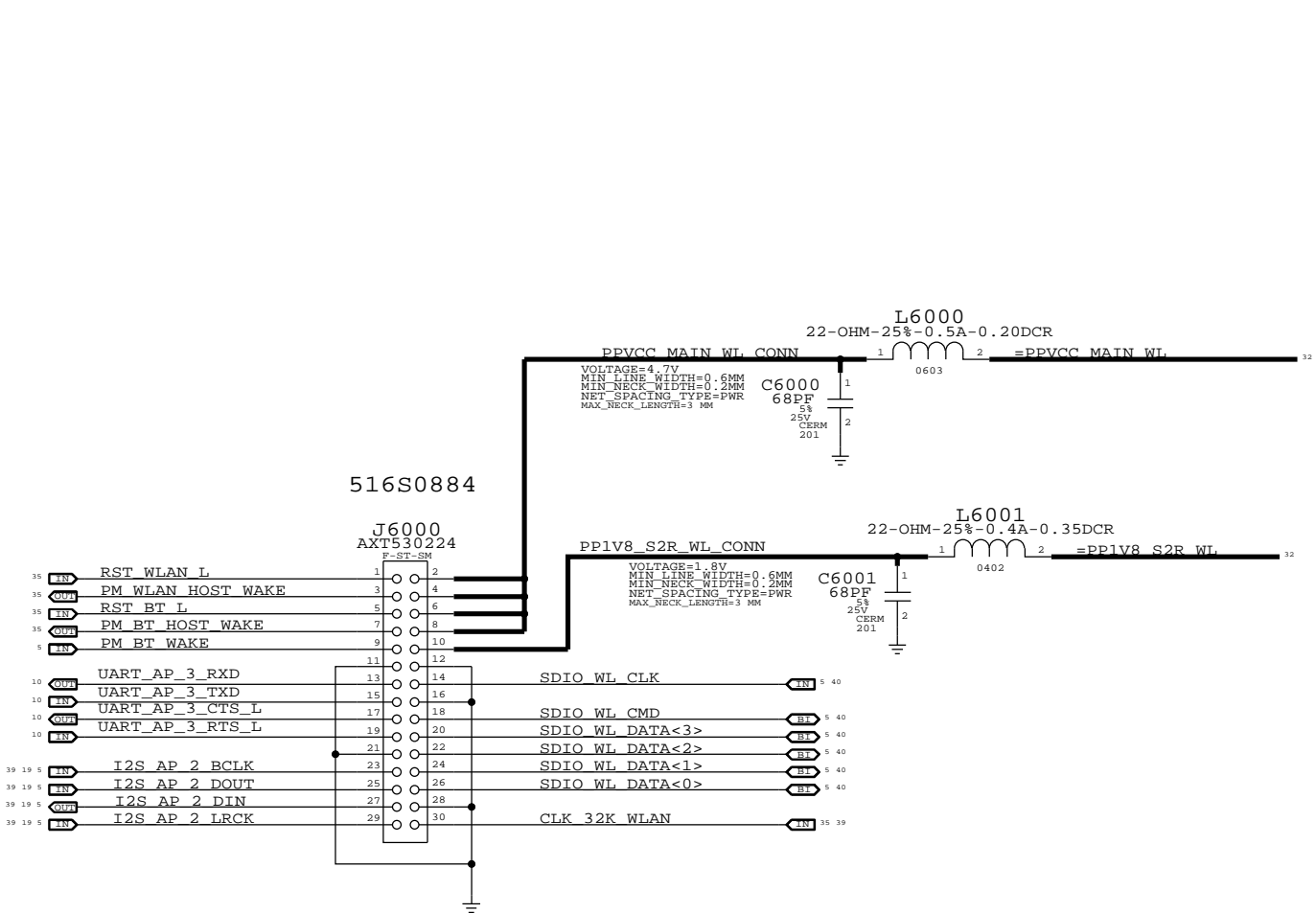
REVISION  
A.0.0

PAGE  
57 OF 106

SHEET  
28 OF 42



X23 WIFI/BT CONNECTOR



## D



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8	7	6	5	4	3	2	1
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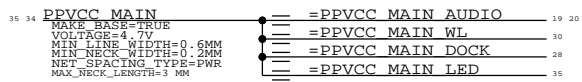
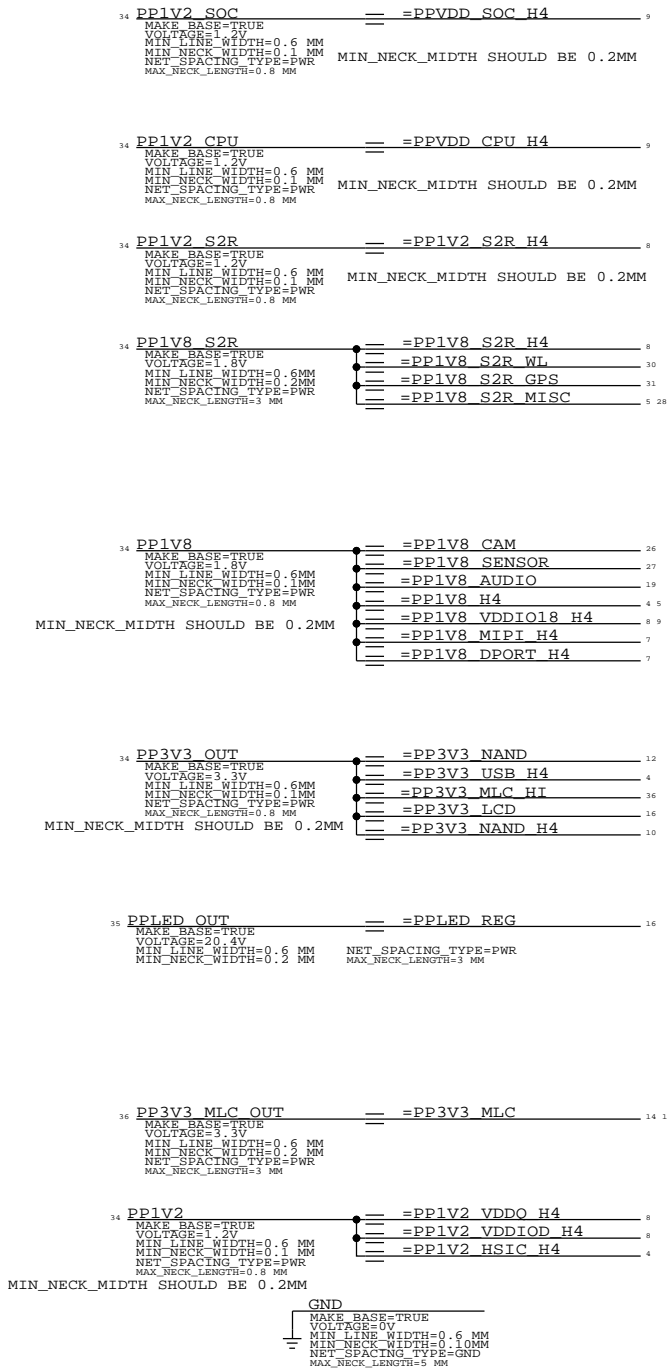
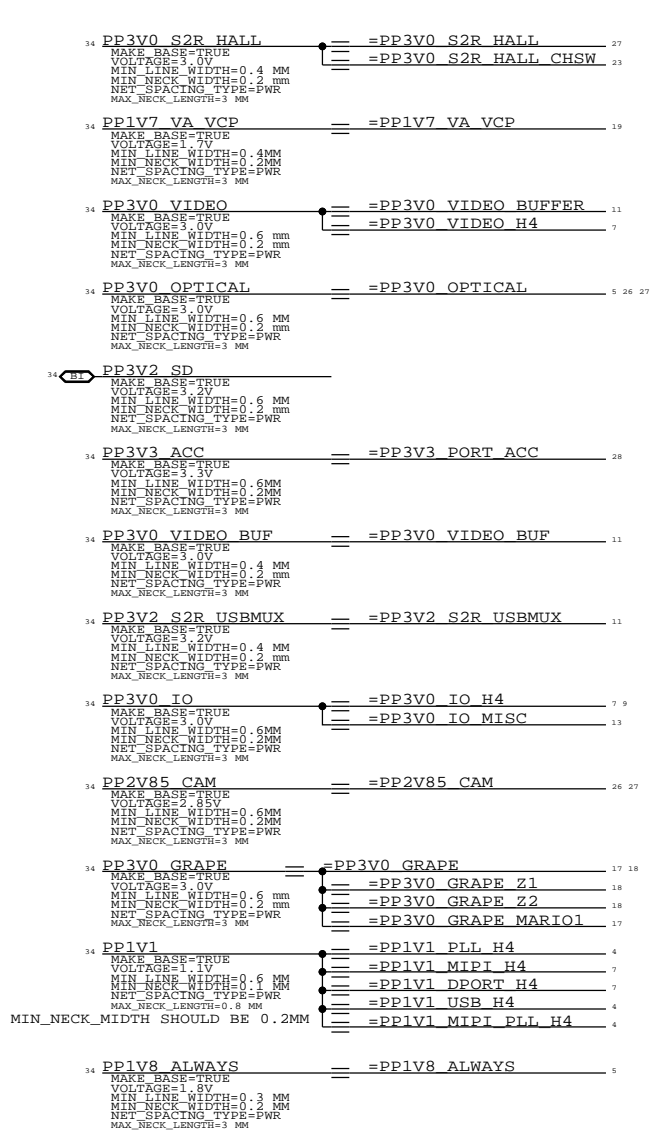
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## LDO RAILS

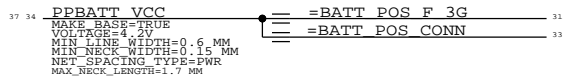
PROGRAMMABLE ON/OFF

## BUCK RAILS

## CHARGER MAIN




## BATTERY

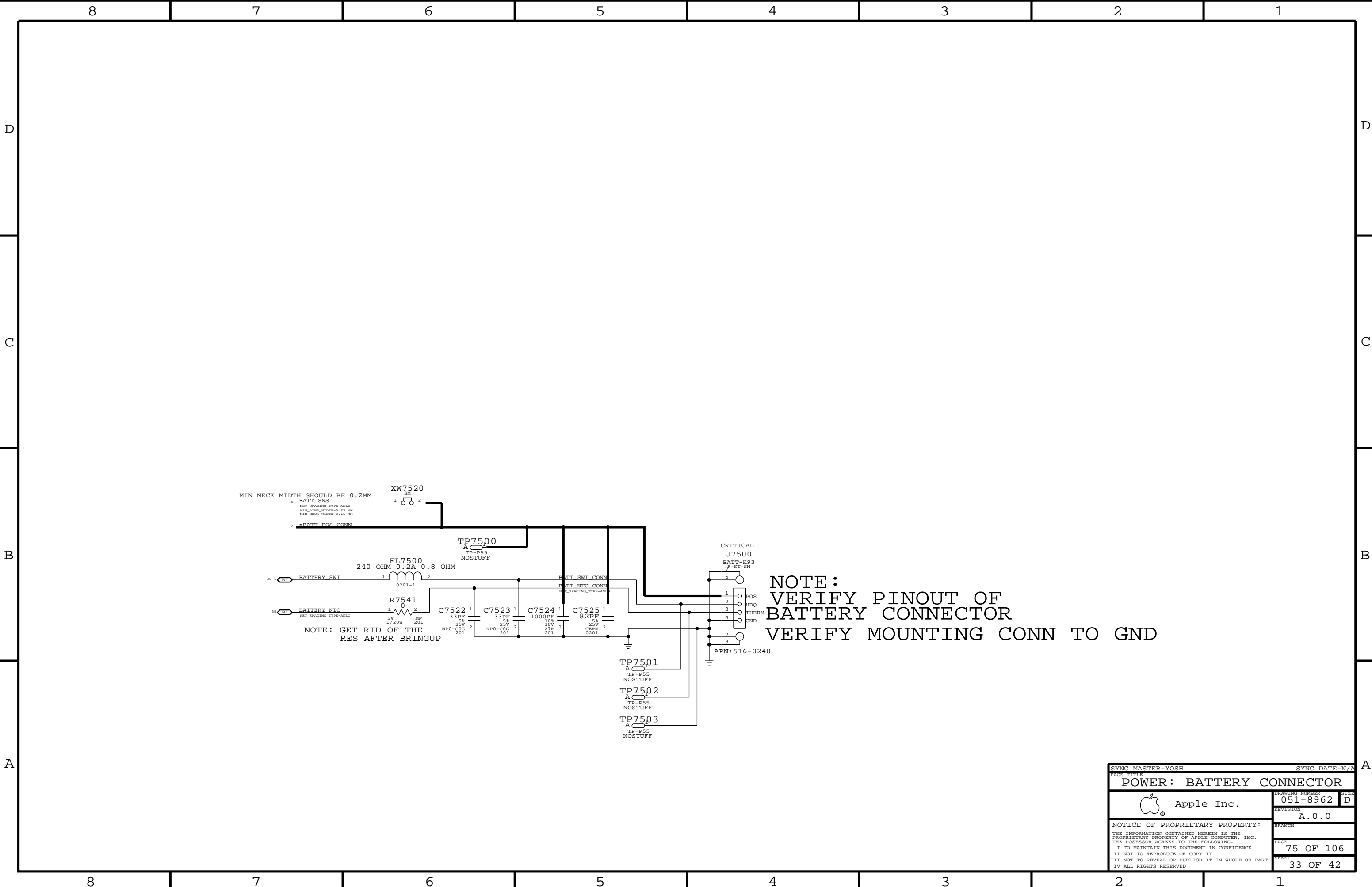


USB POWER INPUT




SYNC MASTER-YOSH		SYNC DATE-N/A	
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NOTE:  
VERIFY PINOUT OF  
BATTERY CONNECTOR  
VERIFY MOUNTING CONN TO GND

SYNC MASTER=YOSH		SYNC DATE=N/A	
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0392	197S0299		Y8138	ALT FOUNDRY

D

D

C

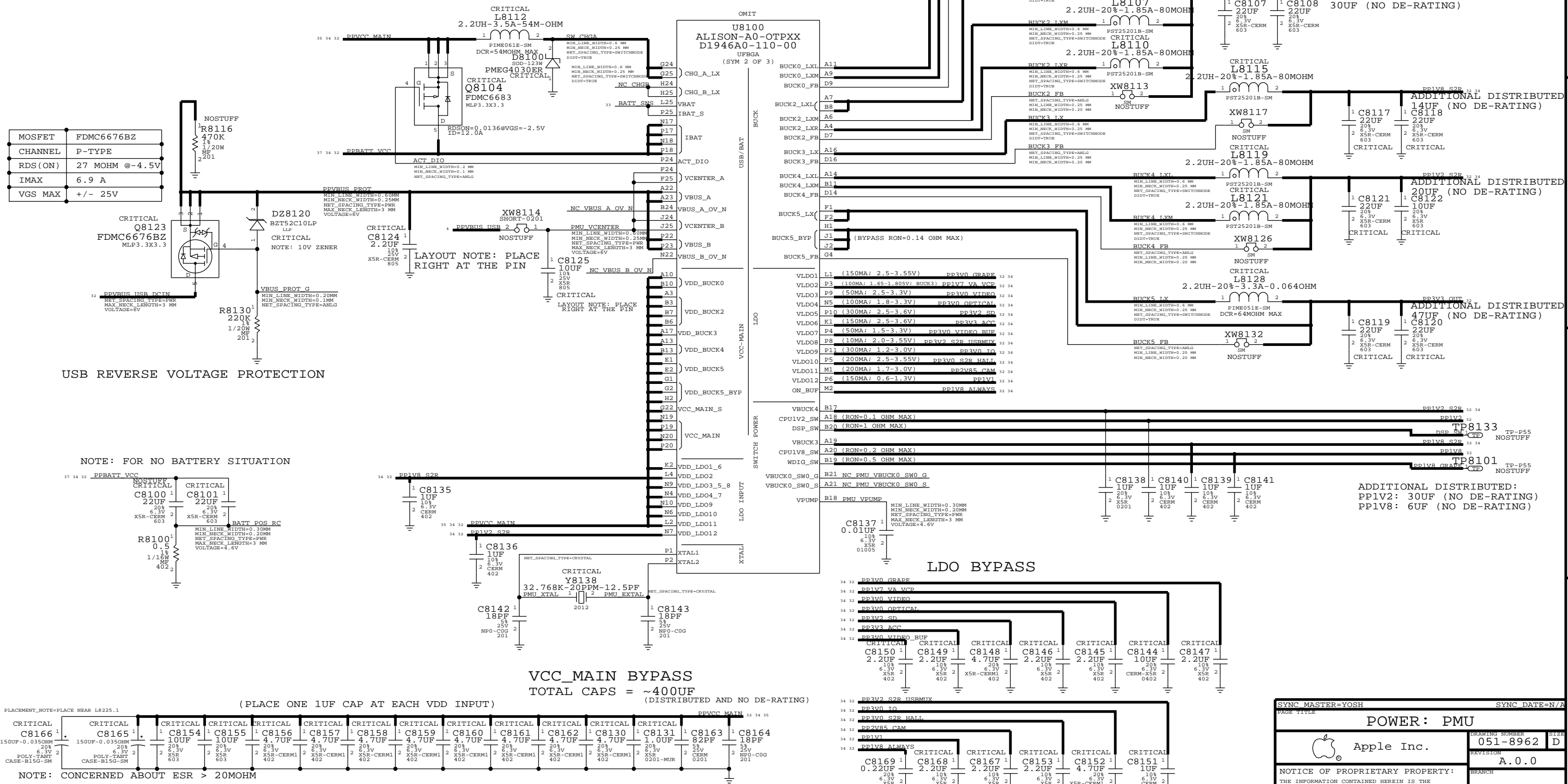
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
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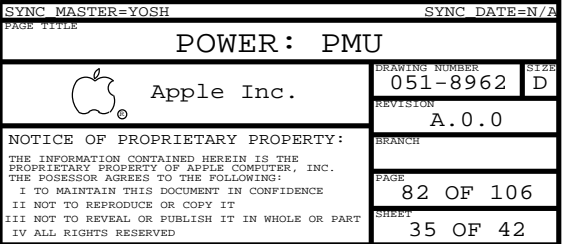
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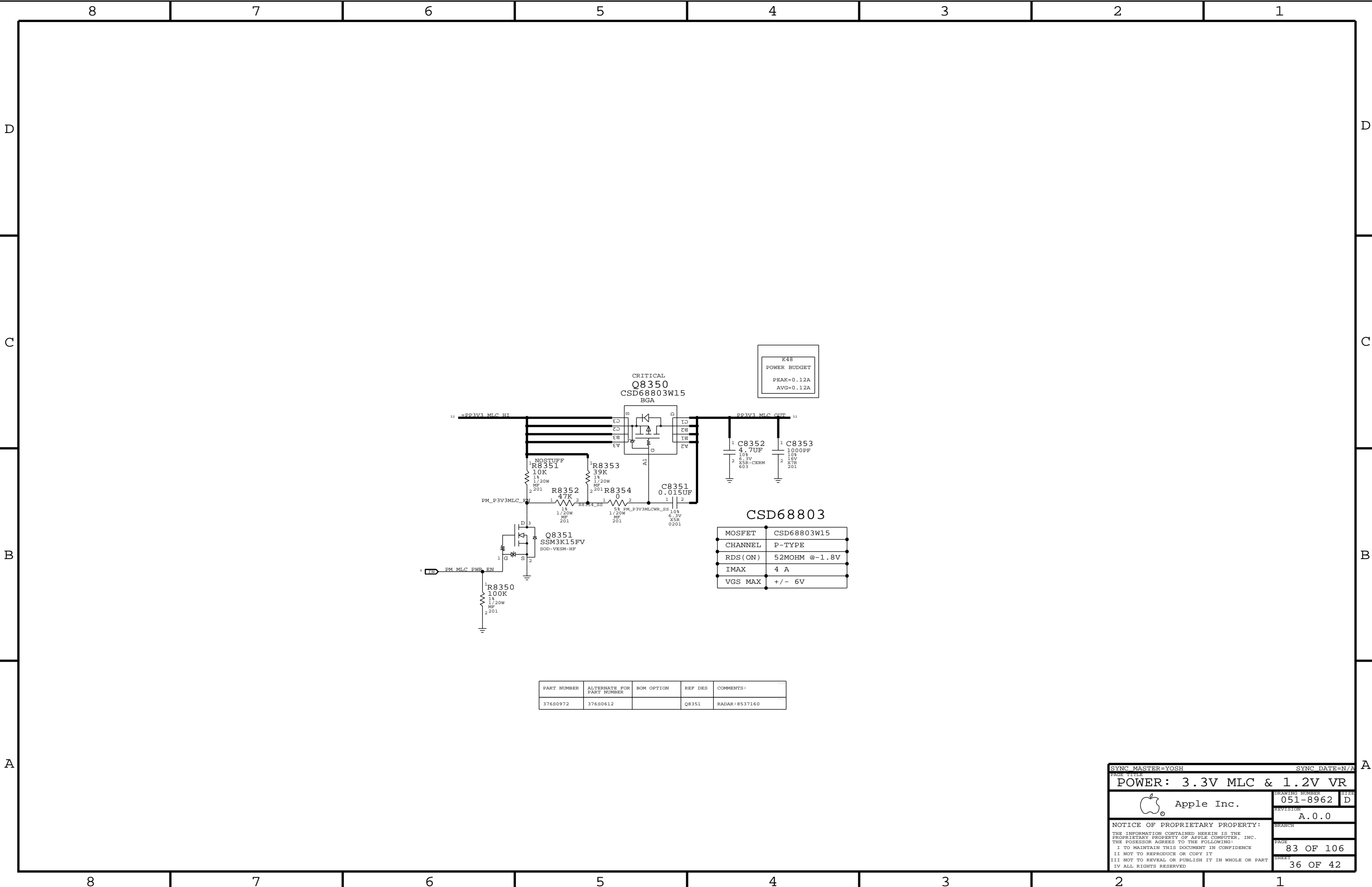
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POWER: PMU			
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0972	376S0612		Q8351	RADAR: 8537160

SYNC MASTER=YOSH

SYNC DATE=N/A

POWER: 3.3V MLC & 1.2V VR

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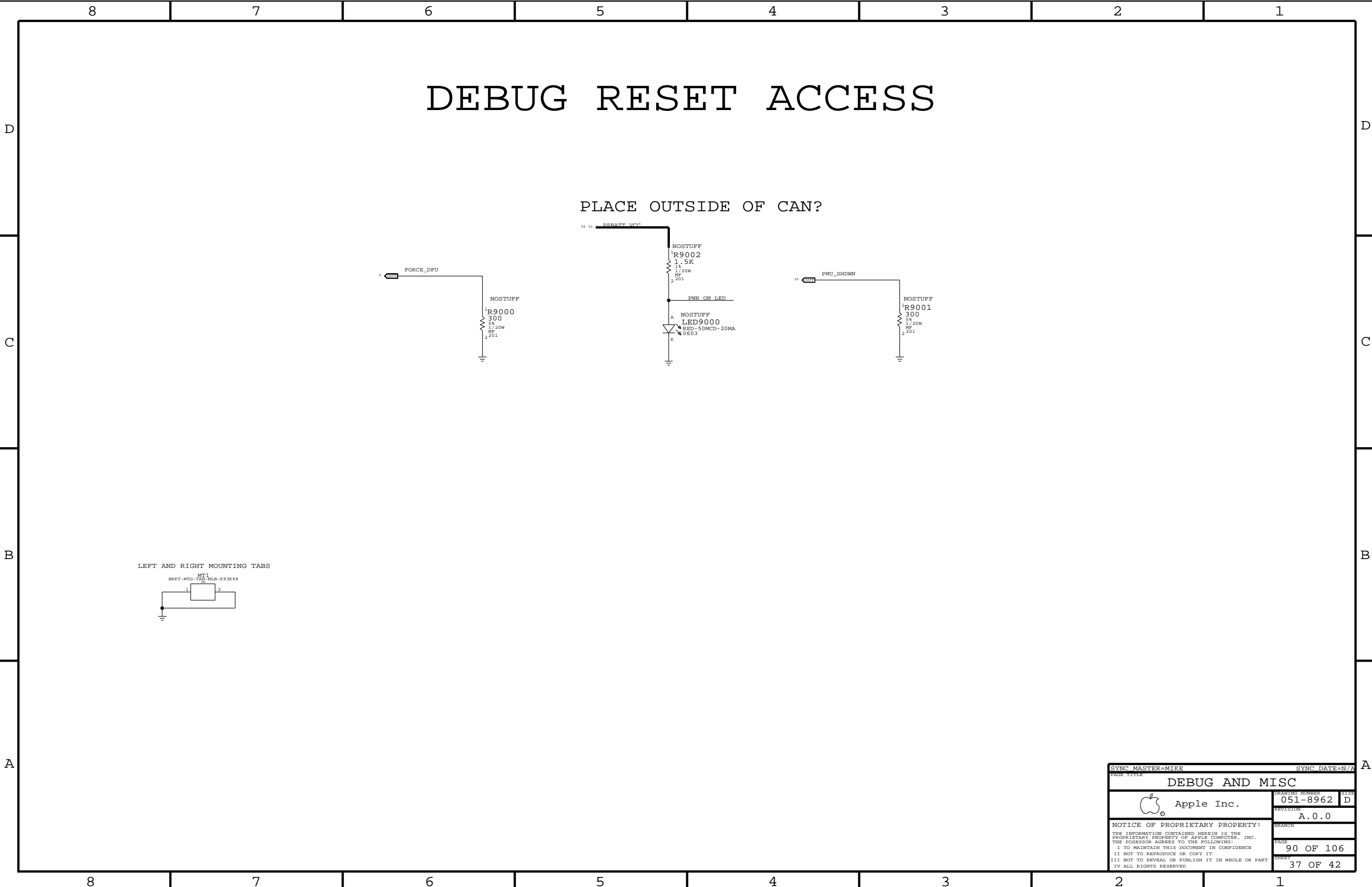
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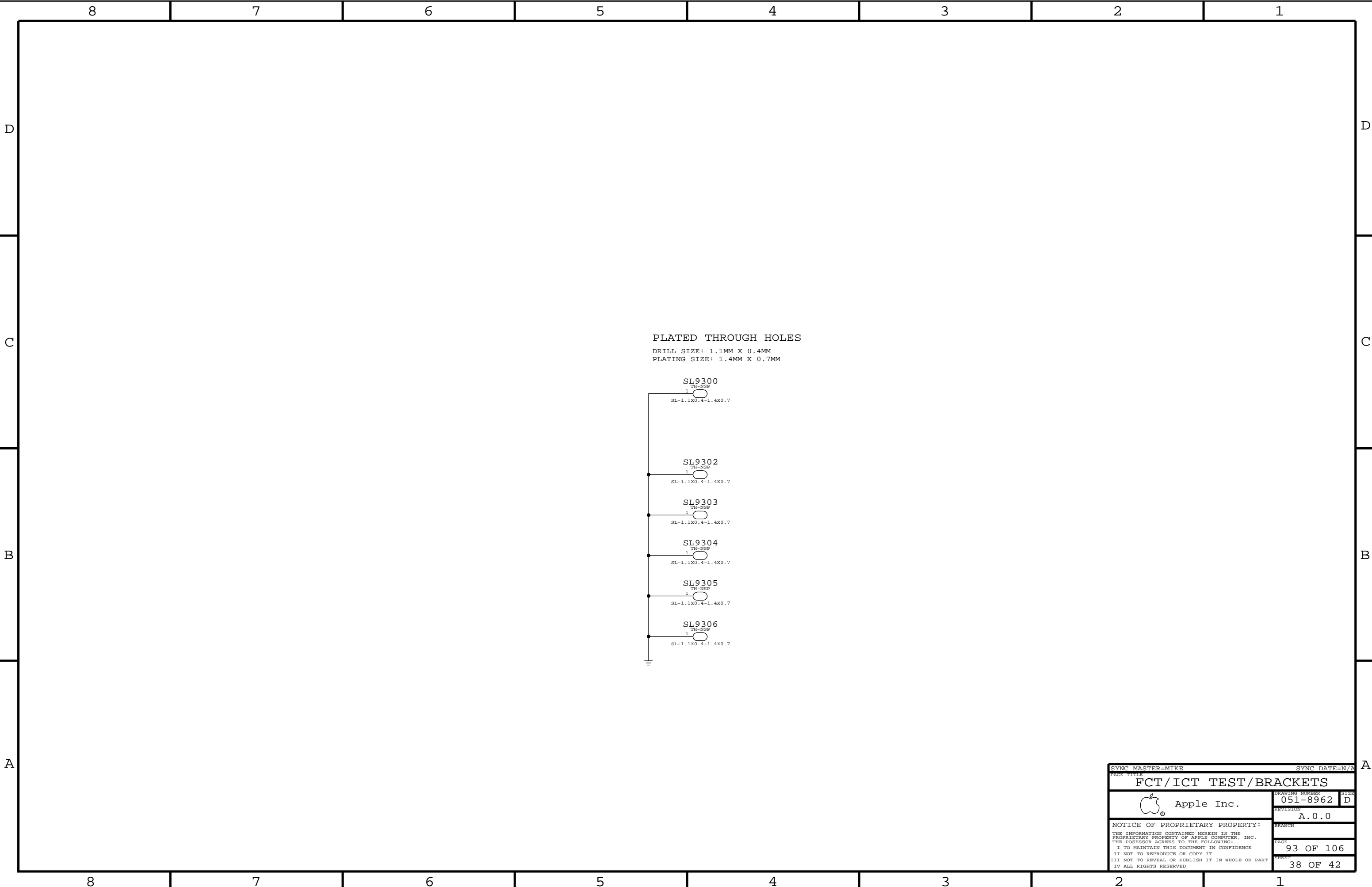
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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R182	CLK_50S	CLK	CLK 32K PMU 18 35
R183	CLK_50S	CLK	CLK 32K WLAN 30 35
R184	CLK_50S	CLK	CLK 32K GPS 31 35
R185	CLK_50S	CLK	CLK CAM FF 7 26
R186	CLK_50S	CLK	CLK CAM FF FILT 25 26
R187	CLK_50S	CLK	CLK CAM FF CONN 7 27
R188	CLK_50S	CLK	CLK CAM RF 25 27
R189	CLK_50S	CLK	CLK CAM RF FILT 25 27
R190	CLK_50S	CLK	I2S AP 0 MCK 5
R191	CLK_50S	CLK	I2S AP 0 MCK R 5 19
R192	CLK_50S	CLK	CLK CAM FF R 7
R193	CLK_50S	CLK	CLK CAM RF R 7

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R180	NAND_50S	NAND	F0AD<7...0> 6 12
R181	NAND_50S	NAND	F0CE0 L 6 12
R182	NAND_50S	NAND	F0CE1 L 6 12
R183	NAND_50S	NAND	F0CE2 L 6 12
R184	NAND_50S	NAND	F0CE3 L 6 12
R185	NAND_50S	NAND	F0CE4 L 6 12
R186	NAND_50S	NAND	F0CE5 L 6 12
R187	NAND_50S	NAND	F0CE6 L 6 12
R188	NAND_50S	NAND	F0CE7 L 6 12
R189	NAND_50S	NAND	F0CLE 6 12
R190	NAND_50S	NAND	F0ALE 6 12
R191	NAND_50S	NAND	FORE L 6 12
R192	NAND_50S	NAND	F0WE L 6 12
R193	NAND_50S	NAND	F0WP L 6 12
R194	NAND_50S	NAND	F1AD<7...0> 6 12
R195	NAND_50S	NAND	F1CE0 L 6 12
R196	NAND_50S	NAND	F1CE1 L 6 12
R197	NAND_50S	NAND	F1CE2 L 6 12
R198	NAND_50S	NAND	F1CE3 L 6 12
R199	NAND_50S	NAND	F1CE4 L 6 12
R200	NAND_50S	NAND	F1CE5 L 6 12
R201	NAND_50S	NAND	F1CE6 L 6 12
R202	NAND_50S	NAND	F1CE7 L 6 12
R203	NAND_50S	NAND	F1CLE 6 12
R204	NAND_50S	NAND	F1ALE 6 12
R205	NAND_50S	NAND	F1RE L 6 12
R206	NAND_50S	NAND	F1WE L 6 12
R207	NAND_50S	NAND	F1WP L 6 12
R208	NAND_50S	NAND	F2AD<7...0>
R209	NAND_50S	NAND	F2CE0 L
R210	NAND_50S	NAND	F2CE1 L
R211	NAND_50S	NAND	F2CE2 L
R212	NAND_50S	NAND	F2CE3 L
R213	NAND_50S	NAND	F2CLE
R214	NAND_50S	NAND	F2ALE
R215	NAND_50S	NAND	F2RE L
R216	NAND_50S	NAND	F2WE L
R217	NAND_50S	NAND	F2WP L
R218	NAND_50S	NAND	F3AD<7...0>
R219	NAND_50S	NAND	F3CE0 L
R220	NAND_50S	NAND	F3CE1 L
R221	NAND_50S	NAND	F3CE2 L
R222	NAND_50S	NAND	F3CE3 L
R223	NAND_50S	NAND	F3CLE
R224	NAND_50S	NAND	F3ALE
R225	NAND_50S	NAND	F3RE L
R226	NAND_50S	NAND	F3WE L
R227	NAND_50S	NAND	F3WP L

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R180		JTAG	JTAG AP TCK 4 28
R181		JTAG	JTAG AP TMS 4 28
R182		JTAG	JTAG AP TDI 4 10
R183		JTAG	JTAG AP TDO 4 10
R184		JTAG	JTAG AP TRST L 4 10

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R180	I2C_50S	I2C	I2C1 SDA 1V8 5 25
R181	I2C_50S	I2C	I2C1 SCL 1V8 5 25
R182	I2C_50S	I2C	I2C0 SDA 1V8 5 10 19 35
R183	I2C_50S	I2C	I2C0 SCL 1V8 5 10 19 35
R184	I2C_50S	I2C	I2C2 SDA 3V0 5 25 26
R185	I2C_50S	I2C	I2C2 SCL 3V0 5 25 26
R186	I2C_50S	I2C	ISP AP 0 SCL 7 25
R187	I2C_50S	I2C	ISP AP 0 SDA 7 25
R188	I2C_50S	I2C	ISP AP 1 SCL 7 26
R189	I2C_50S	I2C	ISP AP 1 SDA 7 26
R190	I2C_50S	I2C	I2C2 SCL 3V0 ALS 25 26
R191	I2C_50S	I2C	I2C2 SDA 3V0 ALS 25 26
R192	I2C_50S	I2C	ISP CAM 1 SCL 25 26
R193	I2C_50S	I2C	ISP CAM 1 SDA 25 26

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R180		CRYSTAL	XTAL 24M I 4
R181		CRYSTAL	XTAL 24M O 4
R182		CRYSTAL	24M_O 4

VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R180		VREF	PPVREF DDR0 CA 8
R181		VREF	PPVREF DDR0 DO 8
R182		VREF	PPVREF DDR1 CA 8
R183		VREF	PPVREF DDR1 DO 8

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R180	USB_90D	USB	USB D P 4 28
R181	USB_90D	USB	USB D N 4 28
R182	USB_90D	USB	USB PT DK CON D P 28 29
R183	USB_90D	USB	USB PT DK CON D N 28 29
R184	USB_90D	USB	USB BB D P 11 31
R185	USB_90D	USB	USB BB D N 11 31
R186	USB_90D	USB	USB FS D P 4 11
R187	USB_90D	USB	USB FS D N 4 11
R188	USB_90D	USB	USB FS N ACC TX 11 28
R189	USB_90D	USB	USB FS P ACC RX 11 28
R190	USB_90D	USB	ACC PT DK CON TX 28 29
R191	USB_90D	USB	ACC PT DK CON RX 28 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R180	I2S_50S	I2S	I2S AP 0 BCLK 5 19
R181	I2S_50S	I2S	I2S AP 0 LRCK 5 19
R182	I2S_50S	I2S	I2S AP 0 DIN 5 19
R183	I2S_50S	I2S	I2S AP 0 DOUT 5 19
R184	I2S_50S	I2S	I63 ASP SDOUT 19
R185	I2S_50S	I2S	I2S AP 2 BCLK 5 19 30
R186	I2S_50S	I2S	I2S AP 2 LRCK 5 19 30
R187	I2S_50S	I2S	I2S AP 2 DIN 5 19 30
R188	I2S_50S	I2S	I2S AP 2 DOUT 5 19 30
R189	I2S_50S	I2S	I63 VSP SDOUT 19
R190	I2S_50S	I2S	I2S AP 3 BCLK 5 19
R191	I2S_50S	I2S	I2S AP 3 LRCK 5 19
R192	I2S_50S	I2S	I2S AP 3 DIN 5 19
R193	I2S_50S	I2S	I2S AP 3 DOUT 5 19
R194	I2S_50S	I2S	I63 XSP SDOUT 19

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R180		DWI	DWI AP CLK 5 35
R181		DWI	DWI AP DI 5 35
R182		DWI	DWI AP DO 5 35

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ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
R200	VID_50S	ANALOG_VIDEO	DAC AP OUT1 7 11
R200	VID_50S	ANALOG_VIDEO	DAC AP OUT2 7 11
R200	VID_50S	ANALOG_VIDEO	DAC AP OUT3 7 11
R200	VID_50S	ANALOG_VIDEO	BUF C Y 11
R200	VID_50S	ANALOG_VIDEO	BUF CVBS PB 11
R200	VID_50S	ANALOG_VIDEO	BUF Y PR 11
R200	VID_50S	ANALOG_VIDEO	VIDEO EMI CVBS_PB 10 11 28
R200	VID_50S	ANALOG_VIDEO	VIDEO EMI C_Y 10 11 28
R200	VID_50S	ANALOG_VIDEO	VIDEO EMI Y PR 10 11 28
R200	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON_CVBS_PB 28 29
R200	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON_C_Y 28 29
R200	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON_Y_PR 28 29

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	4:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
R200	LVDS_100D	LVDS	LVDS DATA P<2..0> 14 16
R200	LVDS_100D	LVDS	LVDS DATA N<2..0> 14 16
R200	LVDS_100D	LVDS	LVDS DATA CONN_P<2..0> 16
R200	LVDS_100D	LVDS	LVDS DATA CONN_N<2..0> 16
R200	LVDS_100D	LVDS	LVDS CLK_P 14 16
R200	LVDS_100D	LVDS	LVDS CLK_N 14 16
R200	LVDS_100D	LVDS	LVDS CLK CONN_P 16
R200	LVDS_100D	LVDS	LVDS CLK CONN_N 16

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
R200	DP_100D	DP	DP AP TX P<0> 7 10 13
R200	DP_100D	DP	DP AP TX N<0> 7 10 13
R200	DP_100D	DP	DP AP TX P<1> 7 10 13
R200	DP_100D	DP	DP AP TX N<1> 7 10 13
R200	DP_100D	DP	DP AP AUX_P 7 13
R200	DP_100D	DP	DP AP AUX_N 7 13
R200	DP_100D	DP	DP EMI TX P<0> 13 28
R200	DP_100D	DP	DP EMI TX N<0> 13 28
R200	DP_100D	DP	DP EMI TX P<1> 13 28
R200	DP_100D	DP	DP EMI TX N<1> 13 28
R200	DP_100D	DP	DP EMI AUX_P 13 28
R200	DP_100D	DP	DP EMI AUX_N 13 28
R200	DP_100D	DP	DP PT DK CON_TX_P<0> 28 29
R200	DP_100D	DP	DP PT DK CON_TX_N<0> 28 29
R200	DP_100D	DP	DP PT DK CON_TX_P<1> 28 29
R200	DP_100D	DP	DP PT DK CON_TX_N<1> 28 29
R200	DP_100D	DP	DP PT DK CON_AUX_P 28 29
R200	DP_100D	DP	DP PT DK CON_AUX_N 28 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
R200	MIPI_100D	MIPT	MIPID AP DATA P<0> 7 14
R200	MIPI_100D	MIPT	MIPID AP DATA N<0> 7 14
R200	MIPI_100D	MIPT	MIPID AP DATA P<1> 7 14
R200	MIPI_100D	MIPT	MIPID AP DATA N<1> 7 14
R200	MIPI_100D	MIPT	MIPID AP DATA P<2> 7 14
R200	MIPI_100D	MIPT	MIPID AP DATA N<2> 7 14
R200	MIPI_100D	MIPT	MIPID AP DATA P<3> 7 14
R200	MIPI_100D	MIPT	MIPID AP DATA N<3> 7 14
R200	MIPI_100D	MIPT	MIPID AP CLK_P 7 14
R200	MIPI_100D	MIPT	MIPID AP CLK_N 7 14
R200	MIPI_100D	MIPT	MIPI0C AP DATA P<0> 7 27
R200	MIPI_100D	MIPT	MIPI0C AP DATA N<0> 7 27
R200	MIPI_100D	MIPT	MIPI0C AP CLK_P 7 27
R200	MIPI_100D	MIPT	MIPI0C AP CLK_N 7 27
R200	MIPI_100D	MIPT	MIPI0C CAM DATA P<0> 25 27
R200	MIPI_100D	MIPT	MIPI0C CAM DATA N<0> 25 27
R200	MIPI_100D	MIPT	MIPI0C CAM CLK_P 25 27
R200	MIPI_100D	MIPT	MIPI0C CAM CLK_N 25 27
R200	MIPI_100D	MIPT	MIPI1C AP DATA P<0> 7 26
R200	MIPI_100D	MIPT	MIPI1C AP DATA N<0> 7 26
R200	MIPI_100D	MIPT	MIPI1C AP CLK_P 7 26
R200	MIPI_100D	MIPT	MIPI1C AP CLK_N 7 26
R200	MIPI_100D	MIPT	MIPI1C CAM DATA P<0> 25 26
R200	MIPI_100D	MIPT	MIPI1C CAM DATA N<0> 25 26
R200	MIPI_100D	MIPT	MIPI1C CAM CLK_P 25 26
R200	MIPI_100D	MIPT	MIPI1C CAM CLK_N 25 26

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
R200	AUDIO	AUDIO	LEFT_CH_OUT_P 19 20
R200	AUDIO	AUDIO	LEFT_CH_OUT_REF 19 20
R200	AUDIO	AUDIO	LEFT_CH_P 20
R200	AUDIO	AUDIO	SSM2375_L_IN_P 20
R200	AUDIO	AUDIO	SSM2375_L_IN_N 20
R200	AUDIO	AUDIO	RIGHT_CH_OUT_P 19 20
R200	AUDIO	AUDIO	RIGHT_CH_OUT_REF 19 20
R200	AUDIO	AUDIO	RIGHT_CH_P 20
R200	AUDIO	AUDIO	SSM2375_R_IN_P 20
R200	AUDIO	AUDIO	SSM2375_R_IN_N 20
R200	AUDIO	AUDIO	EXT_MIC_P 19 23
R200	AUDIO	AUDIO	EXT_MIC_REF 19 23

SDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SDIO_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SDIO	*	*	2:1_SPACING
SDIO_CLK	*	*	4:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
R200	SDIO_50S	SDIO_CLK	SDIO_WL_CLK 5 30
R200	SDIO_50S	SDIO_CLK	SDIO_WL_CLK_R 5 30
R200	SDIO_50S	SDIO	SDIO_WL_CMD 5 30
R200	SDIO_50S	SDIO	SDIO_WL_DATA<3..0> 5 30

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
R200	SPT_50S	SPT	SPI_GRAPE_MISO 5 31
R200	SPT_50S	SPT	SPI_GRAPE_MOSI 5 31
R200	SPT_50S	SPT	SPI_GRAPE_SCLK 5 31
R200	SPT_50S	SPT	SPI_GRAPE_CS_L 5 31
R200	SPT_50S	SPT	SPI_IPC_MISO 5 31
R200	SPT_50S	SPT	SPI_IPC_MOSI 5 31
R200	SPT_50S	SPT	SPI_IPC_SCLK 5 31
R200	SPT_50S	SPT	SPI_IPC_MRDY 5 31

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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, BOTTOM	NO_TYPE, BGA, BGA06-06	MM	15.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES  
45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2, ISL3, ISL8, ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	3.0 MM		
45_OHM_SE	*	N	0.060 MM	0.060 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

50 OHMS - CLEAR ON LAYER 2 AND 5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP	Y	0.240 MM	0.240 MM	3.0 MM		
50_OHM_SE	ISL4	Y	0.060 MM	0.060 MM	3.0 MM		

50 OHMS - CLEAR ON TOP AND BOTTOM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL2, ISL9	Y	0.090 MM	0.090 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES

100 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP, BOTTOM	Y	0.076 MM	0.076 MM		0.210 MM	0.210 MM
100_OHM_DIFF	N	Y	0.057 MM	0.057 MM	=STANDARD	0.300 MM	0.300 MM

90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL3, ISL8, ISL9	Y	0.054 MM	0.054 MM	=STANDARD	0.200 MM	0.100 MM
90_OHM_DIFF	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	=STANDARD	0.200 MM	0.100 MM

AUDIO PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.060 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.090 MM	?
2:1_SPACING	*	0.120 MM	?
2.5:1_SPACING	*	0.150 MM	?
3:1_SPACING	*	0.180 MM	?
4:1_SPACING	*	0.240 MM	?
5:1_SPACING	*	0.300 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

\*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP, BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

NOTES:


- 0.075 MM ~ 3 MIL
- 0.089 MM ~ 3.5 MIL
- 0.102 MM ~ 4 MIL
- 0.114 MM ~ 4.5 MIL
- 0.125 MM ~ 5 MIL
- 0.140 MM ~ 5.5 MIL
- 0.15 MM ~ 6 MIL
- 0.18 MM ~ 7 MIL
- 0.2 MM ~ 8 MIL
- 0.25 MM ~ 10 MIL
- 0.3 MM ~ 12 MIL
- 0.33 MM ~ 13 MIL
- 0.4 MM ~ 16 MIL
- 1.0 MM = 39.37 MIL

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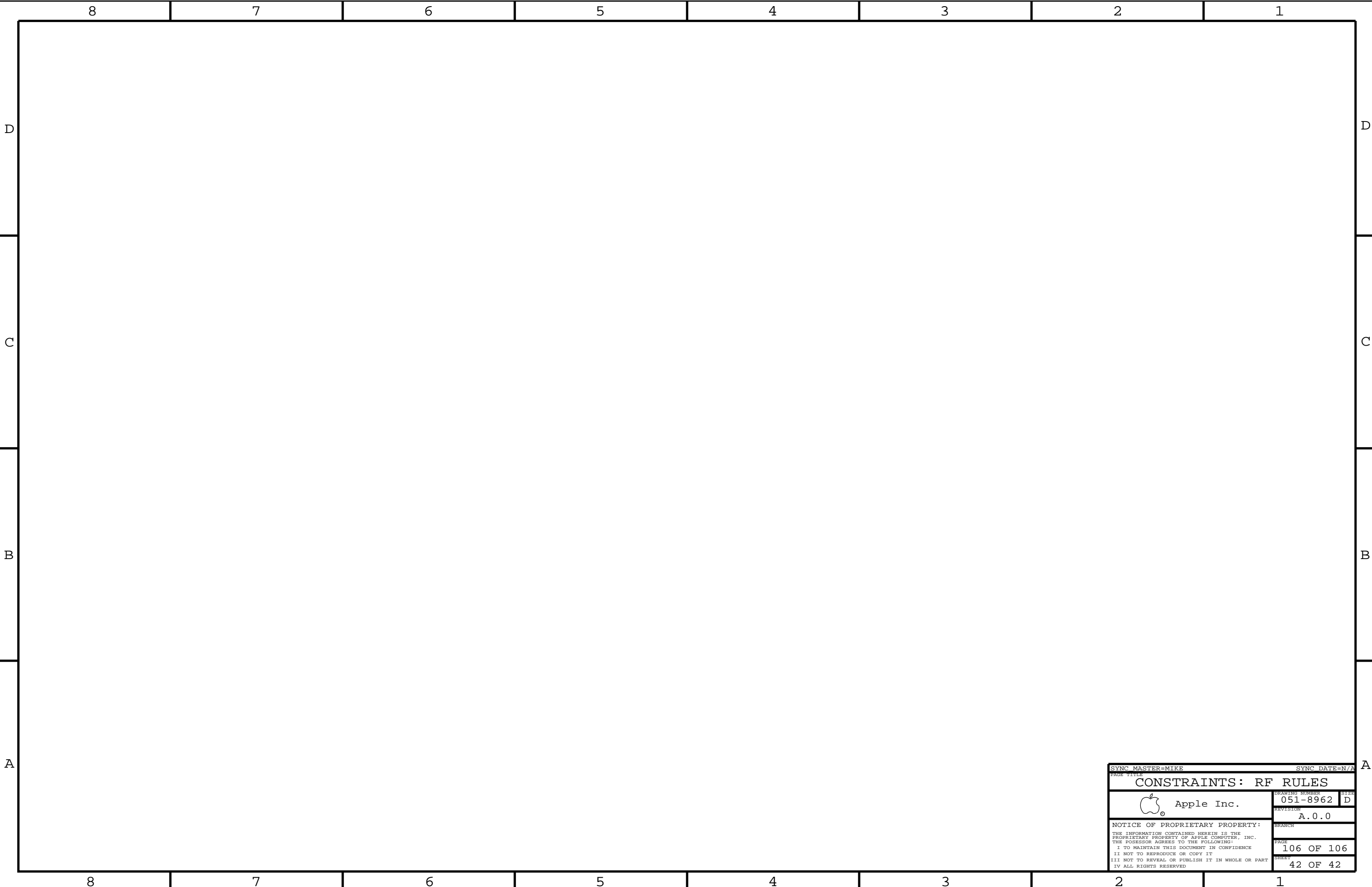
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