

SUMMARY:

Rev History

- 1. Base on V069-100 to Modify HDMI change to internal support
- 2. BGA-136 DDRIII
- 3. RT-8805 Two Phase PWM for NVVDD
- 4. MS-11 for FBVDD

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- Page 11: MIOA/MIOB
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- Page 23: FBVDD with MS-11 MS-V1

OA

- Page 3 Enable G23pin H_PLLVDD 1V2 for G84 only
- Page 11 reserve G84 SLI circuit
- Page 12,13,14 reserve DAC_Vref power for G84 DACA,B,C
- Page 16 reserve 1V8 for G84 IFPAB_PLLVDD
- Page 17 reserve 1V8 for G84 IFPCD_PLLVDD
- Page 18 reserve 1V2 for G84 PLLVDD and VID_PLLVDD
- Page 20 reserve MIOB_CTL3 new strap for G84 PCI_DEVID_4
- Page 20 reserve ROM_SI pull-down resister required if MIOA VDDQ=2.5V for G84
- Page 21add 1V8 power for G84
- Page 22,23 Reserve MS-V1co-lay circuit

100

- Page 3 H_PLLVDD 1V2 use 0ohm connect to PEX1V2
- Page 3 Reserve G84 Dual Rank(Stacked Die) circuit FBA_CMD7----CS1 FBA_CMD27---BA2
- Page 7 Reserve G84 Dual Rank(Stacked Die) circuit FBC_CMD7----CS1 FBC_CMD27---BA2
- Page 7 Reserve I2CS citcuit for G84
- Page 6,10 Enable FBAA2 and FBCC2 BA2 Pin this is for Stacked Die Function
- Page 13 Modify RGB circuit
- Page 15 Modify SAA7115 RESET circuit
- Page 18 Modify Spidf circuit
- Page 21 Modify Linear Power circuit
- Page 22 NVVDD PWM Change to RT-8805 Two Phase
- Page 22,23 Remove MS-V1co-lay circuit

110

- Page 3 Connect FBVDD for G84
- Page 18 Reerve other Spidf circuit
- Page 22 Co-lay small chock for NVVDD

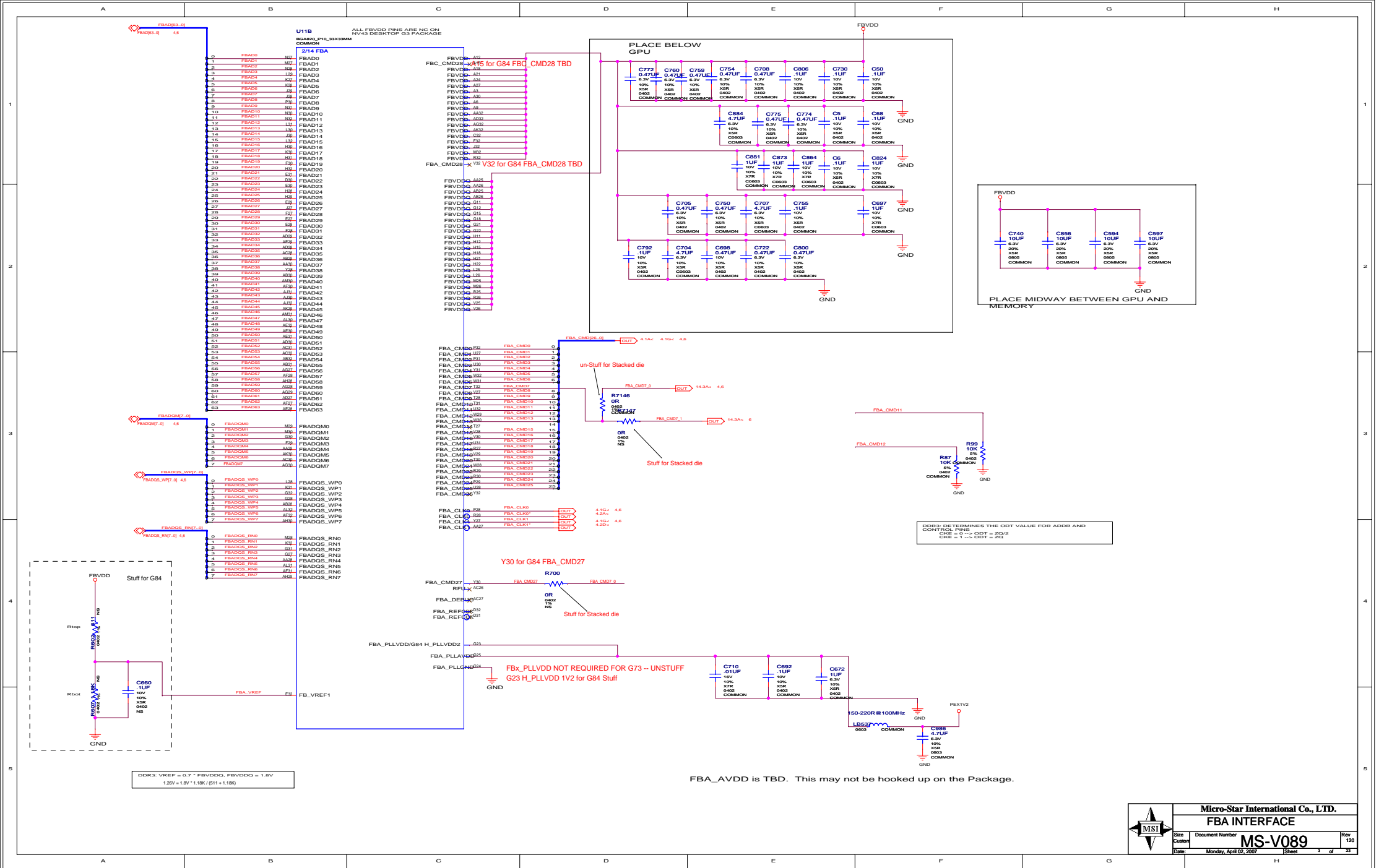
120

- Remove all G73 co-lay circuit
- Page 18 Spidf circuit add 100K R for fix noise

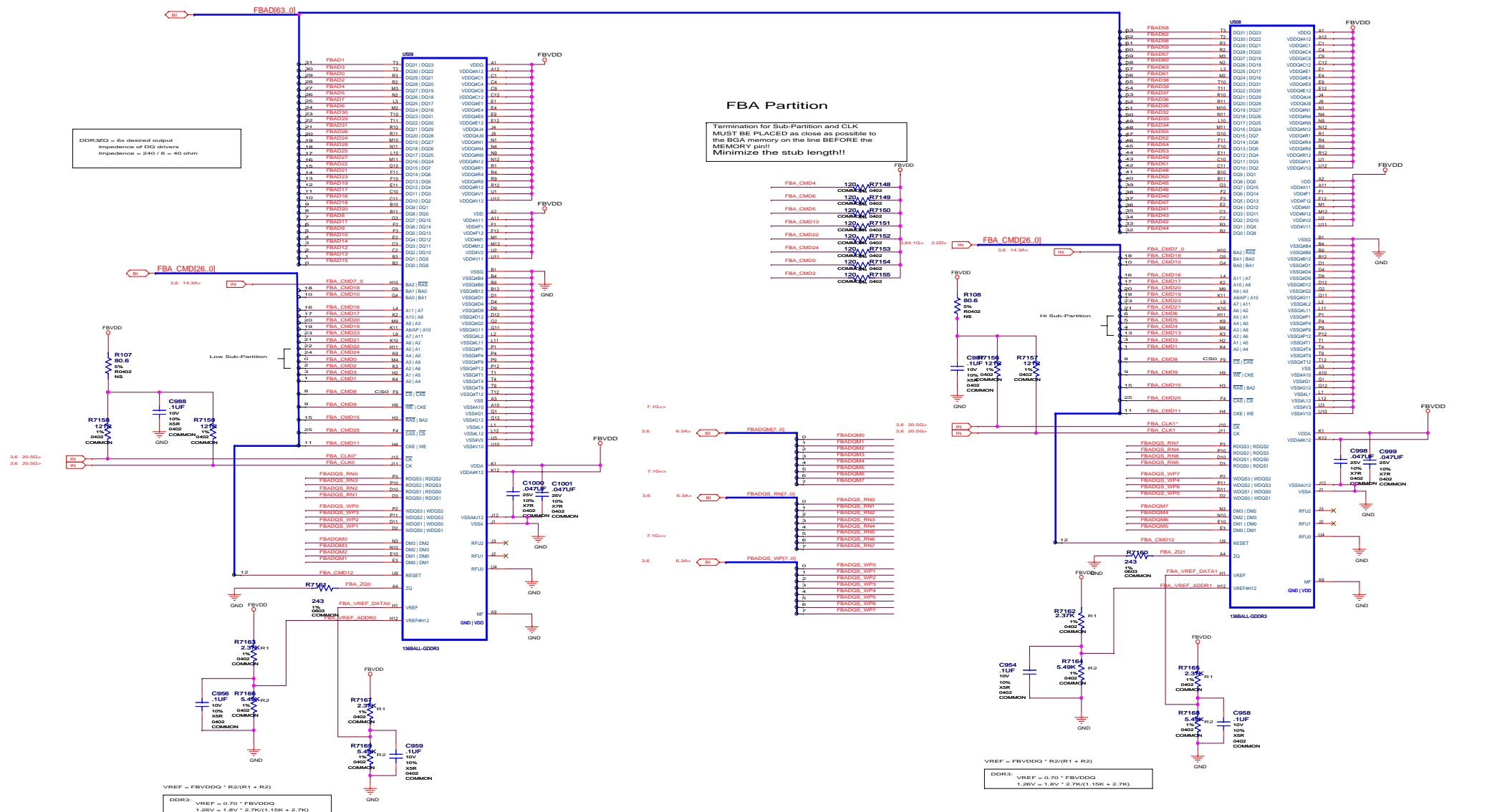
short duration contention possible
 $3.3V^2/100 =$



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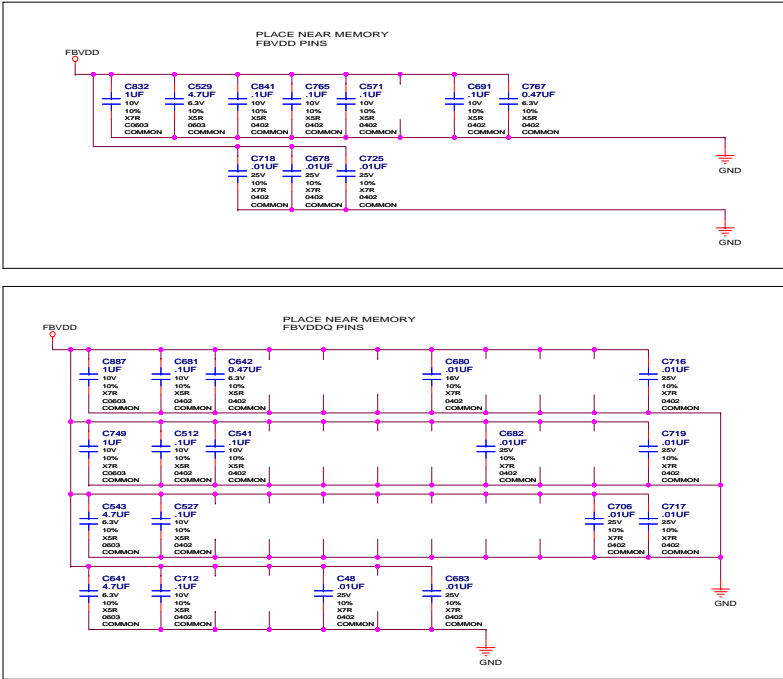


Framebuffer: Partition A
16Mx32 BGA136 DDR3

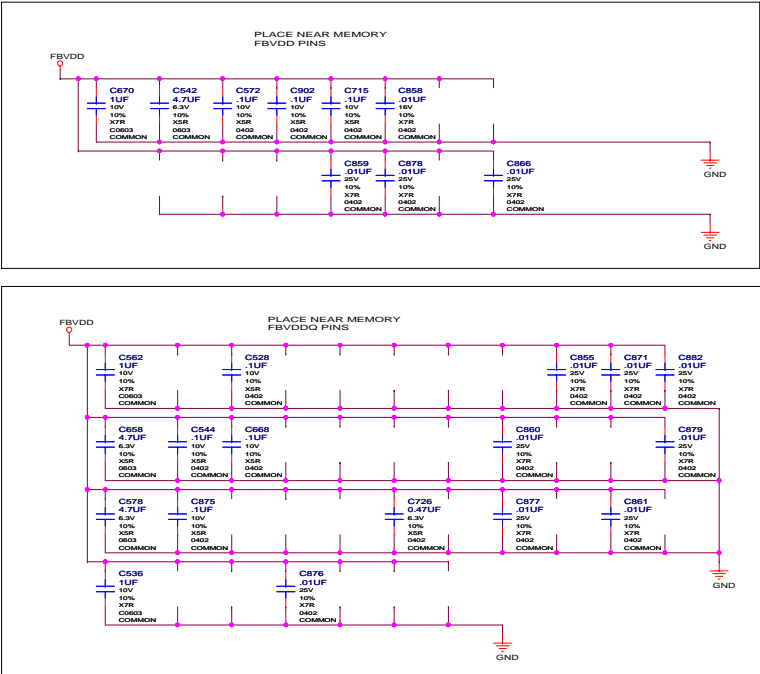


FRAME BUFFER: PARTITION A
DECOUPLING

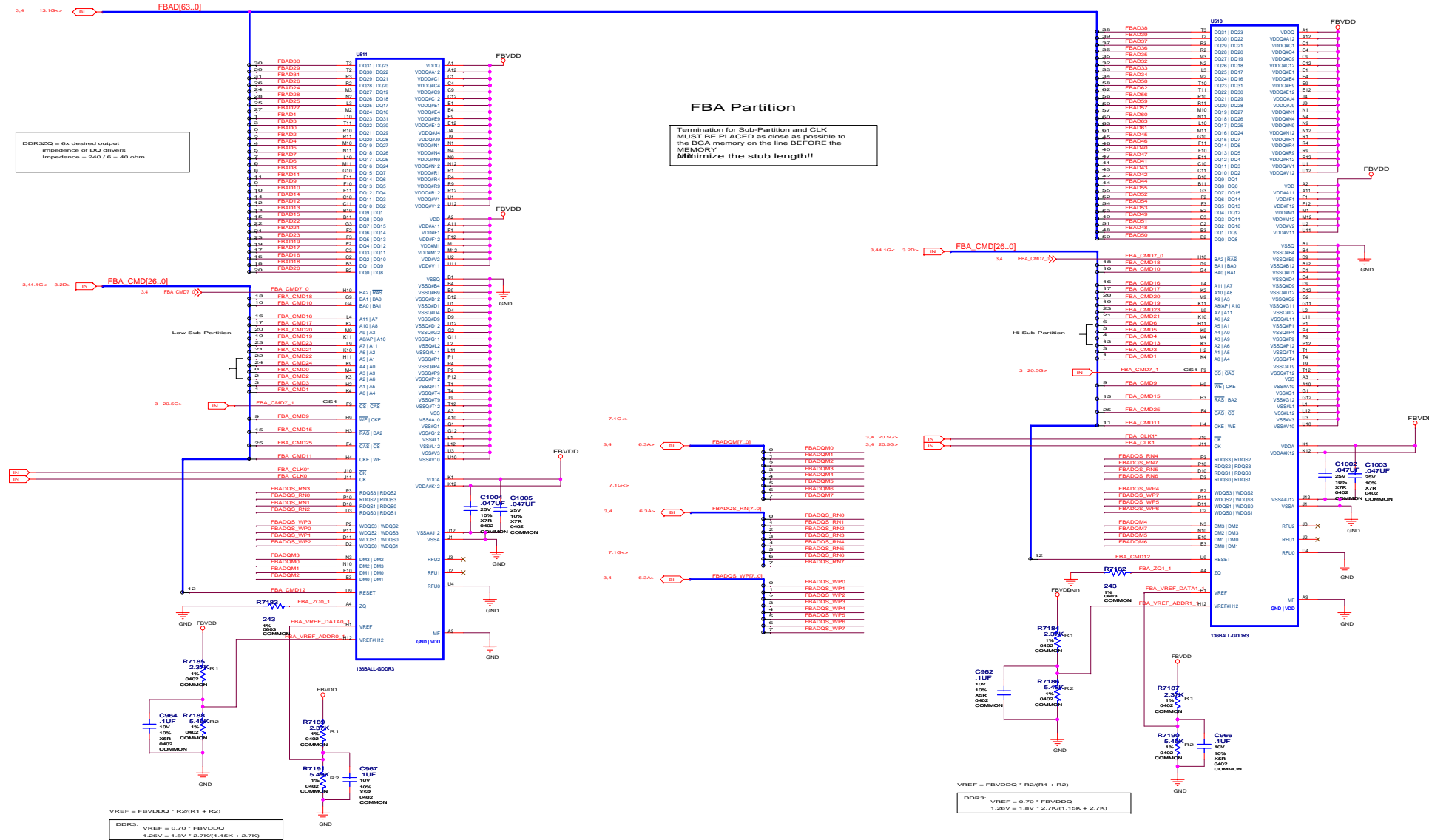
Decoupling for FBA 0..31



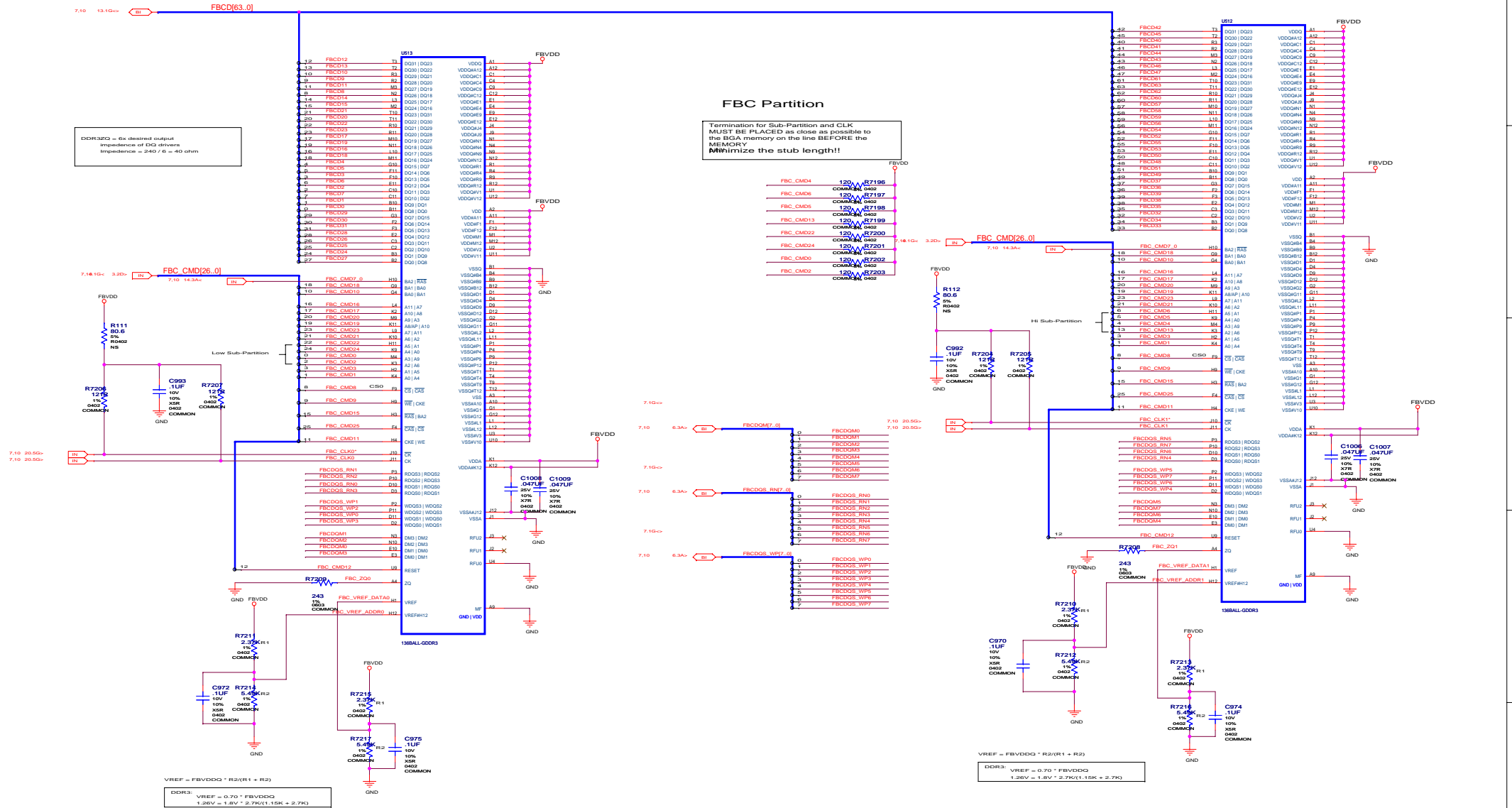
Decoupling for FBA 32..63



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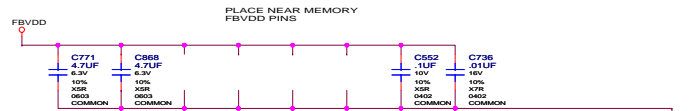


FRAMEBUFFER: PARTITION
C 16Mx32 BGA136 DDR3

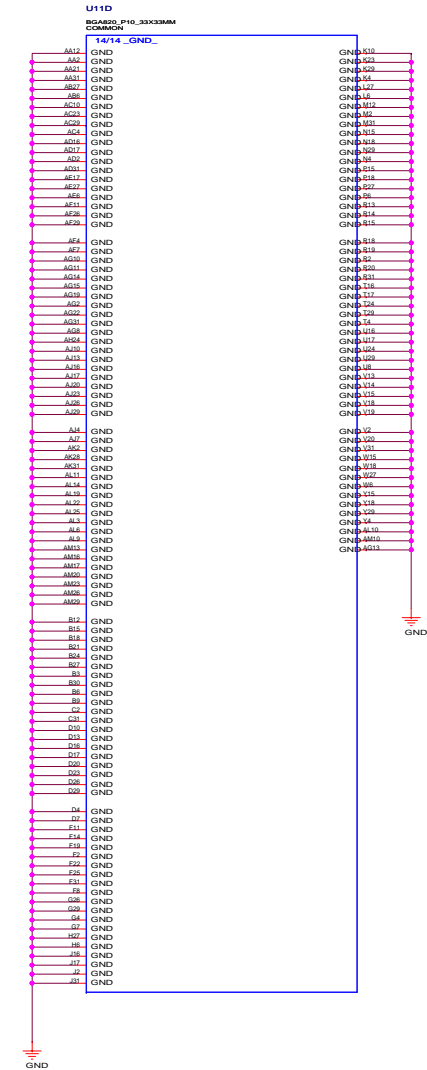
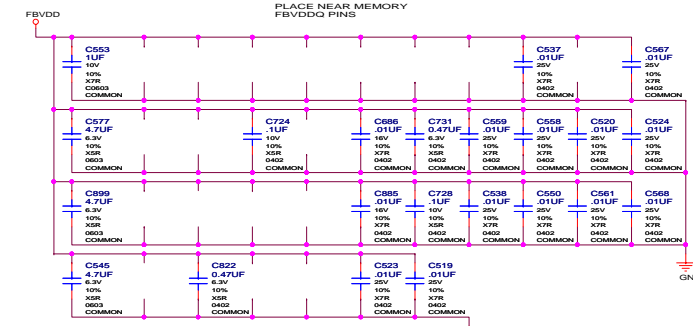
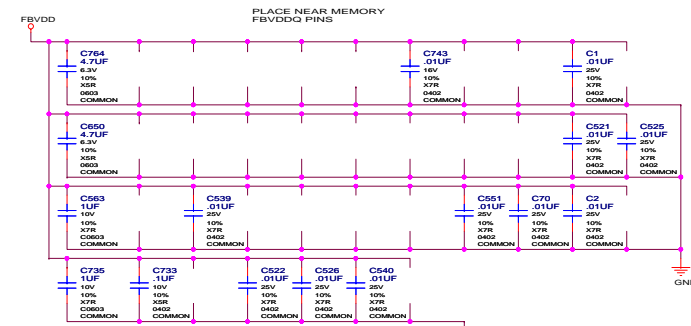
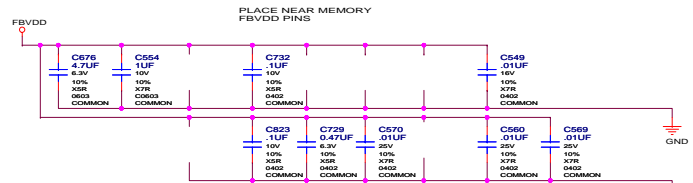


FRAMEBUFFER: PARTITION C DECOUPLING

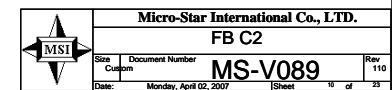
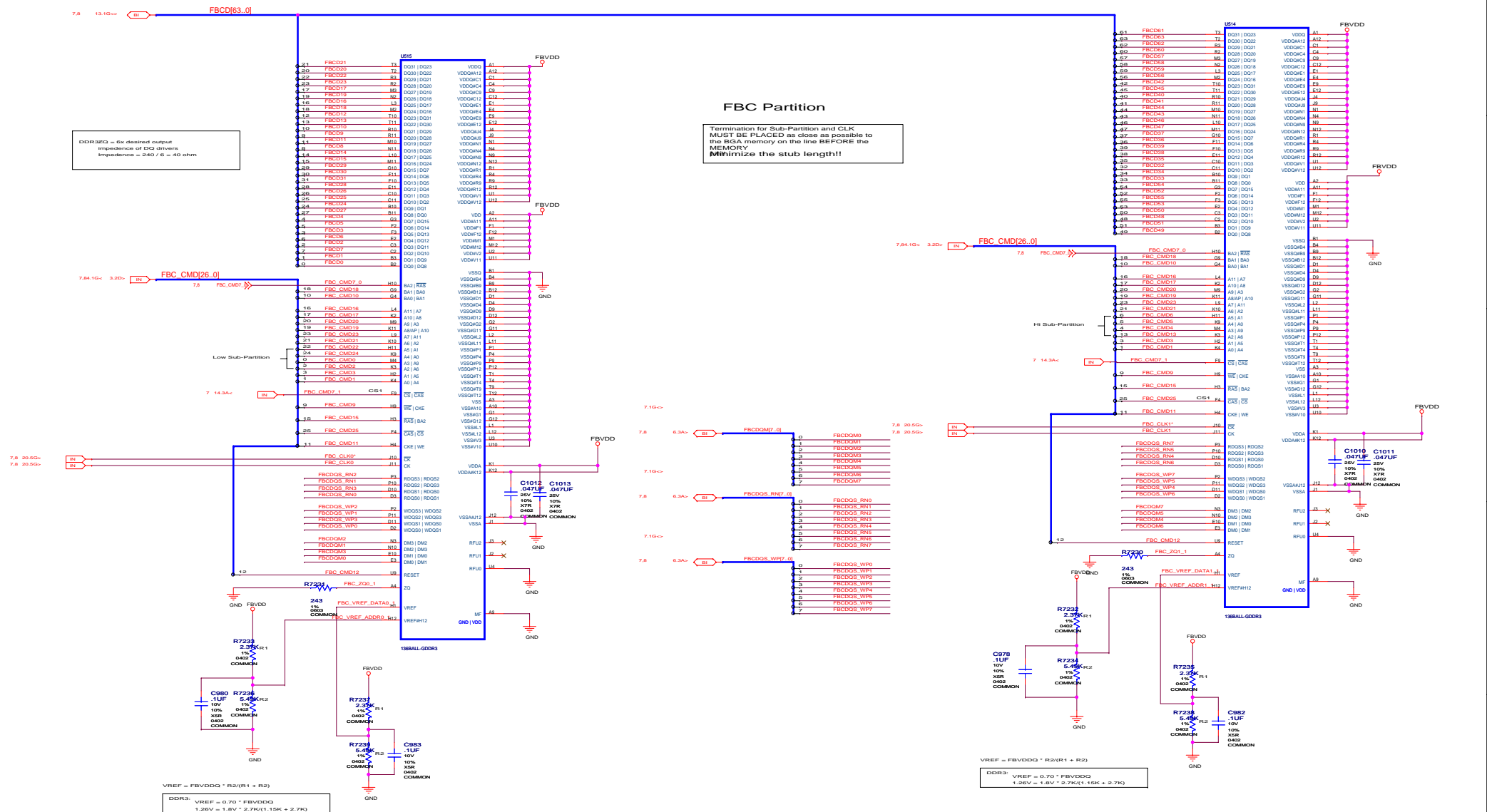
Decoupling for FBC 0..31



Decoupling for FBC 32..63

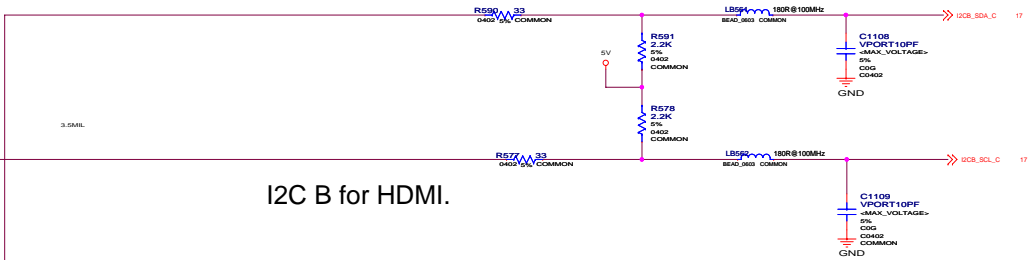
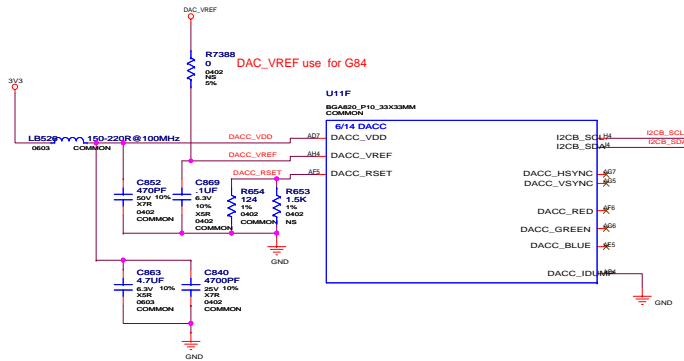


FRAMEBUFFER: PARTITION
C 8Mx32 BGA136 DDR3

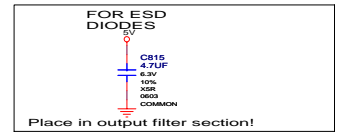


Secondary Display (DACC), HDMI

I2C B for HDMI.

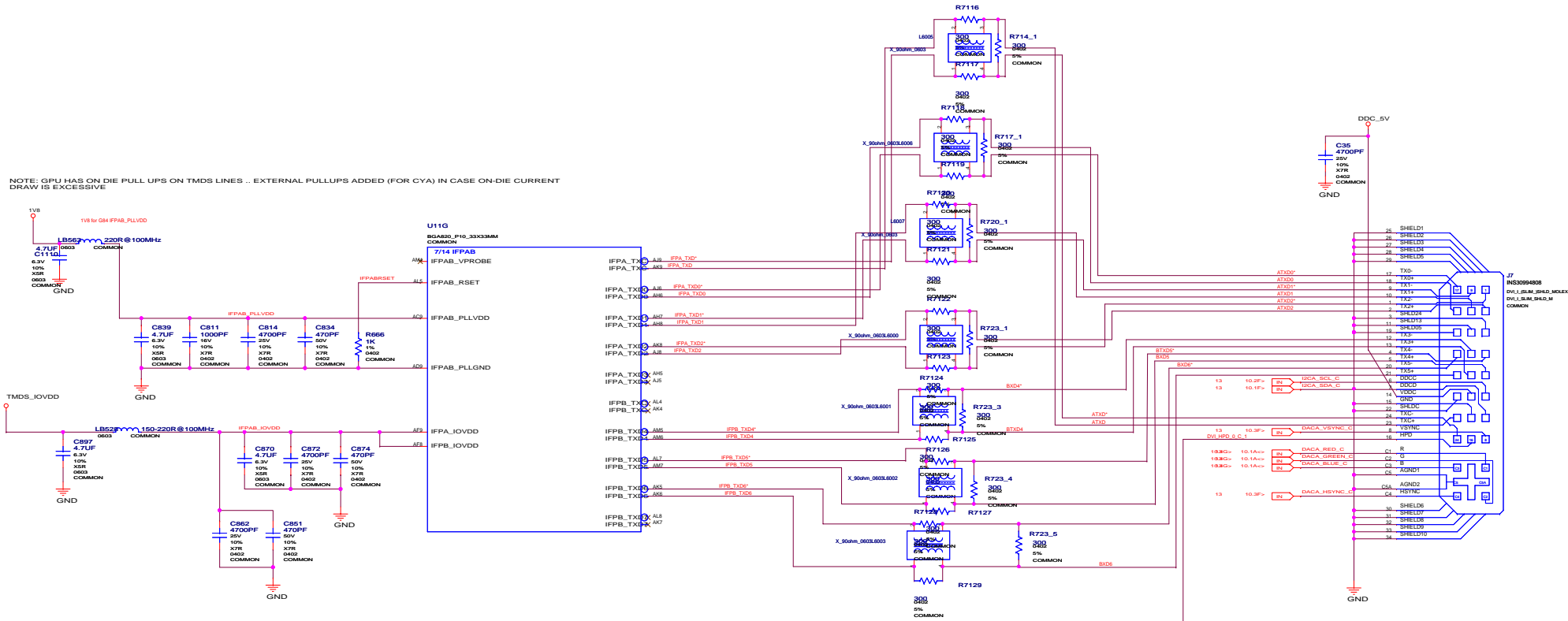


DACA
RGB-FILTER

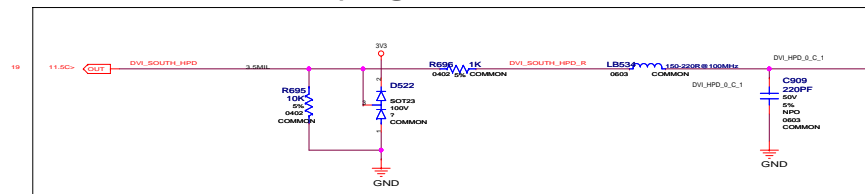


INTERNAL TMDS .. LINK A & B

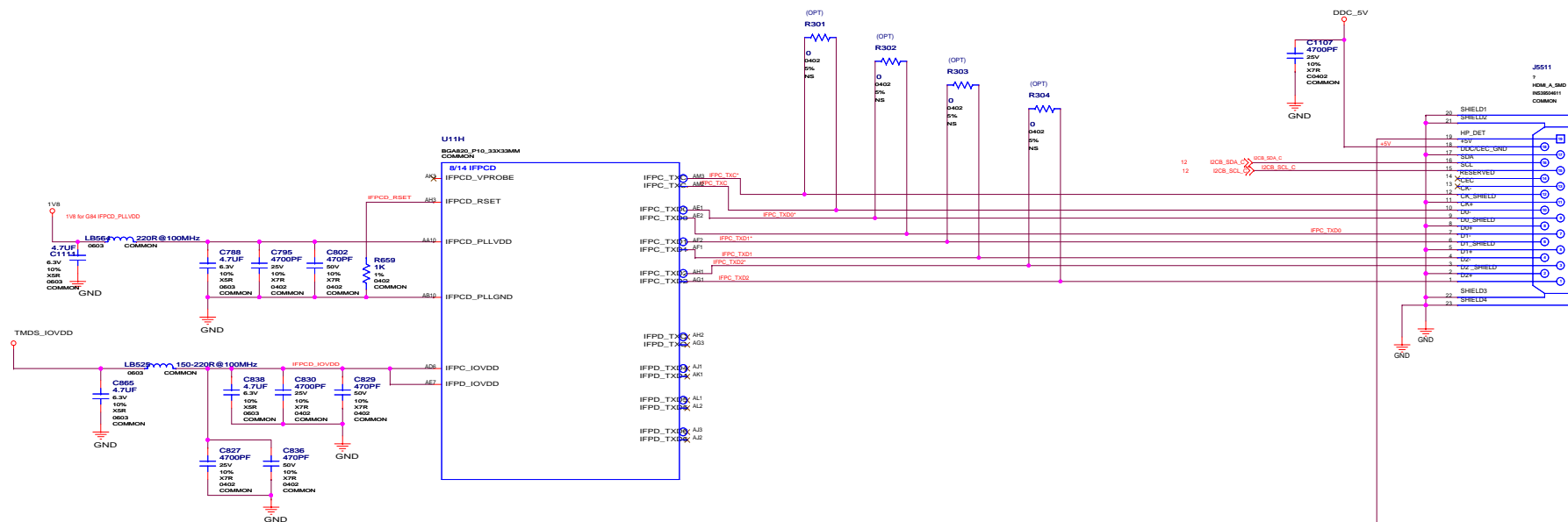
NOTE: GPU HAS ON DIE PULL UPS ON TMDS LINES .. EXTERNAL PULLUPS ADDED (FOR CYA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE



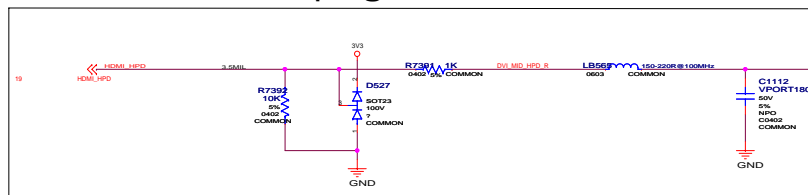
Hotplug Detection



INTERNAL TMDS
.. LINK C & D



Hotplug Detection

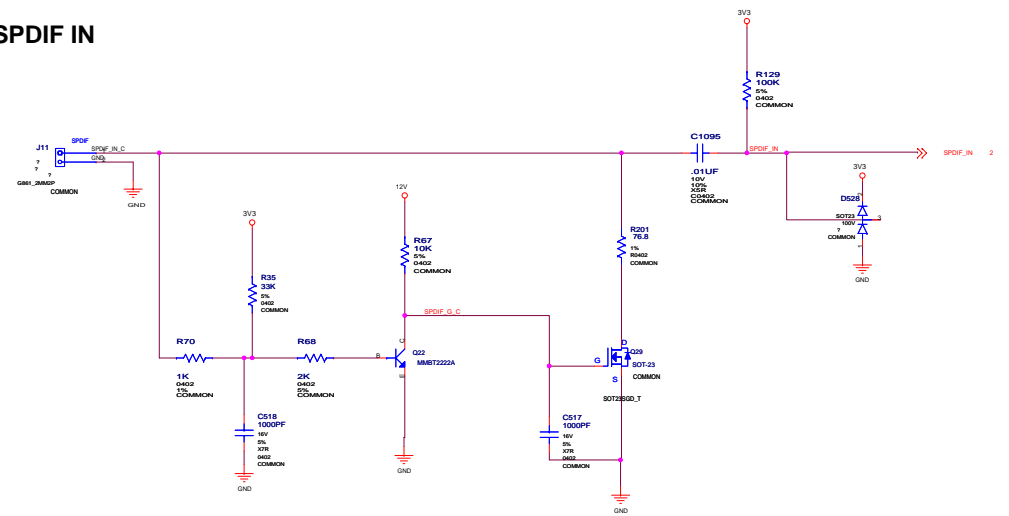


Micro-Star International Co., LTD.

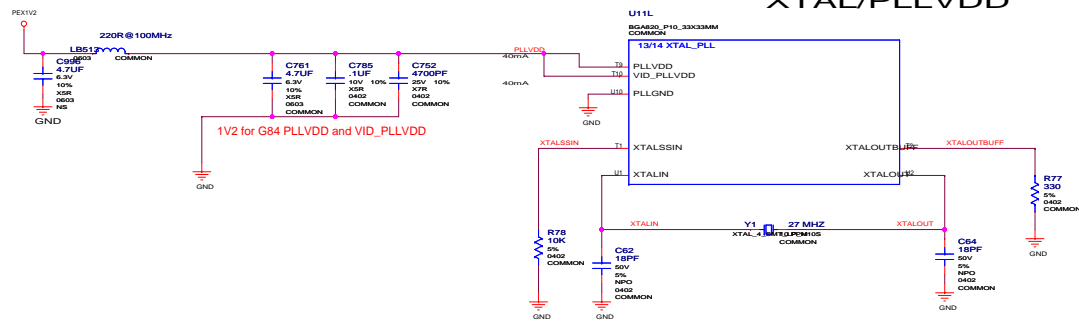
TMD5 LINK C & D

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SPDIF IN



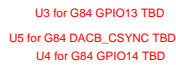
XTAL/PLLVDD



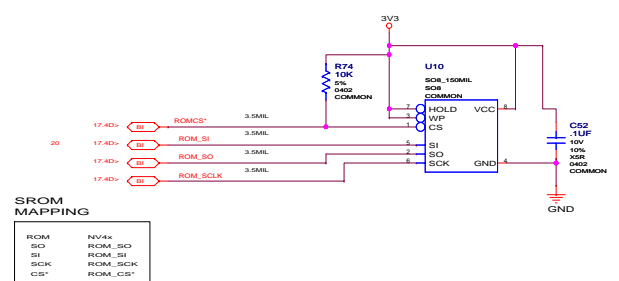


GPIO Assignment Table	
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GPIO	FUNCTION
0 IN	DVI MID HOTPLUG DET
1 IN	HDMI hotplug
2 IN	RESERVED
3 IN	RESERVED
4 IN	TUNER IRQ
5 OUT	NVDD VOLTAGE SELECT 0
6 OUT	NVDD VOLTAGE SELECT 1
7 OUT	TPI INTERRUPT ENABLE
8 IN	RESERVED
9 OUT	PWM FAN
10 IN	INT from Sil930
11 IN	TVRSET
12 IN	uC PROGRAMMING CONTROL



BIOS (serial)



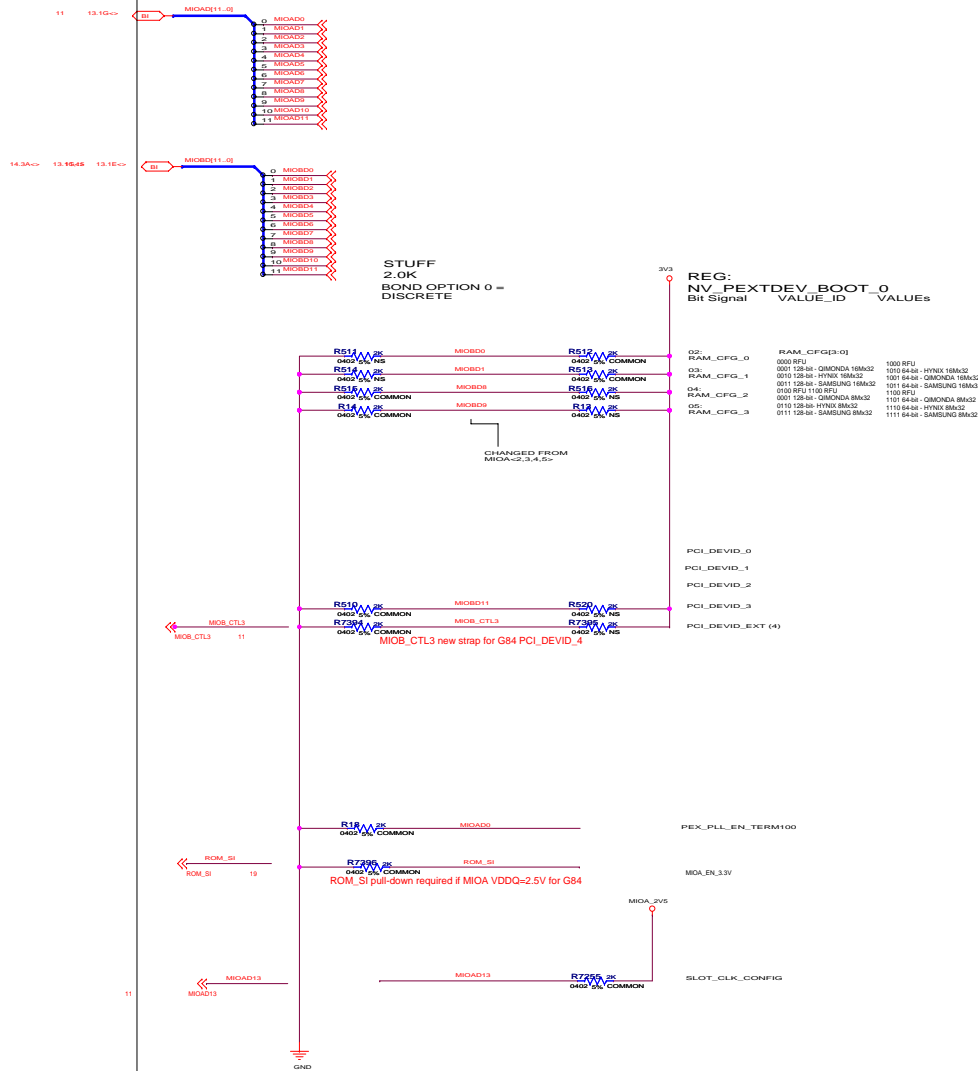
Micro-Star International Co., LTD.

GPIO/ROM/HDCP ROM

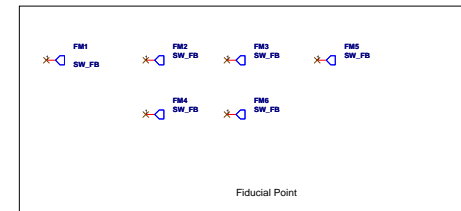
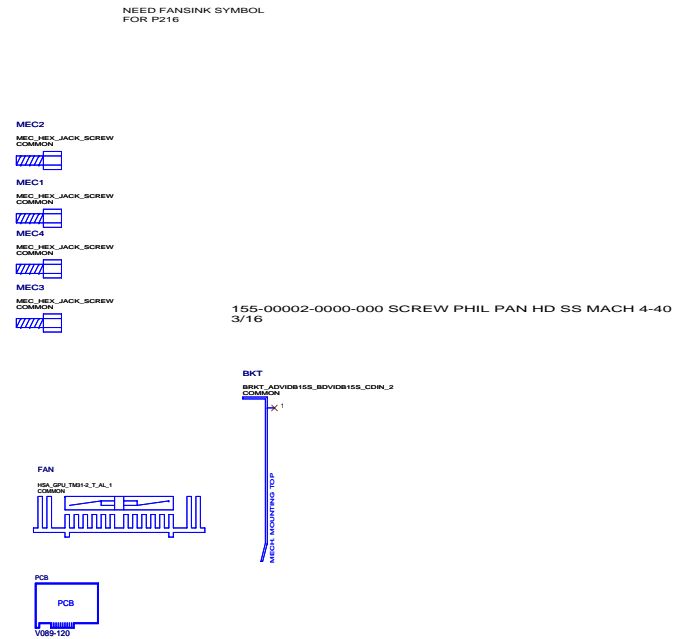
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BIOS, Straps, Misc

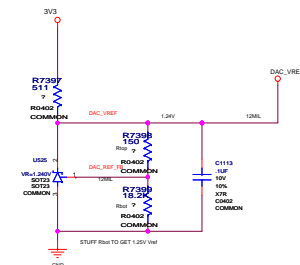
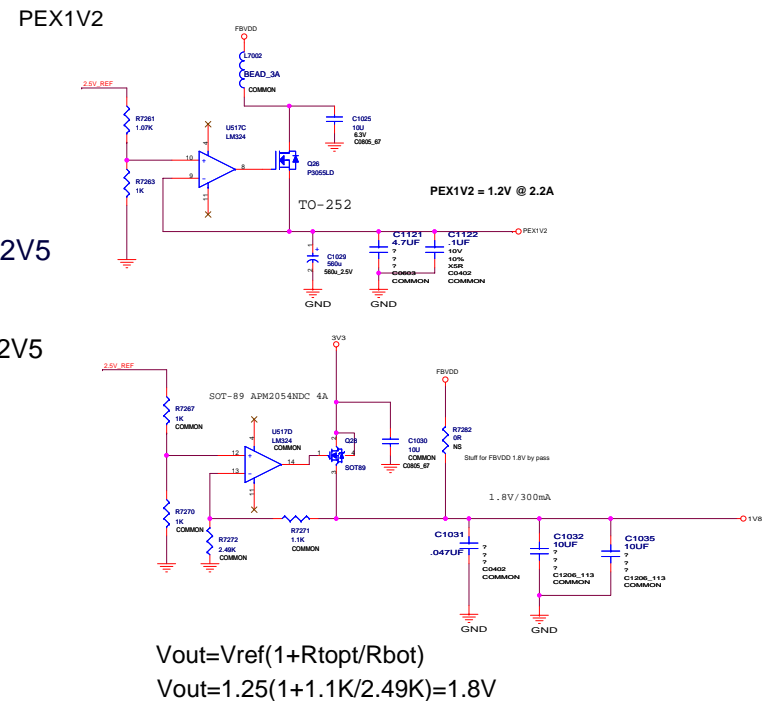
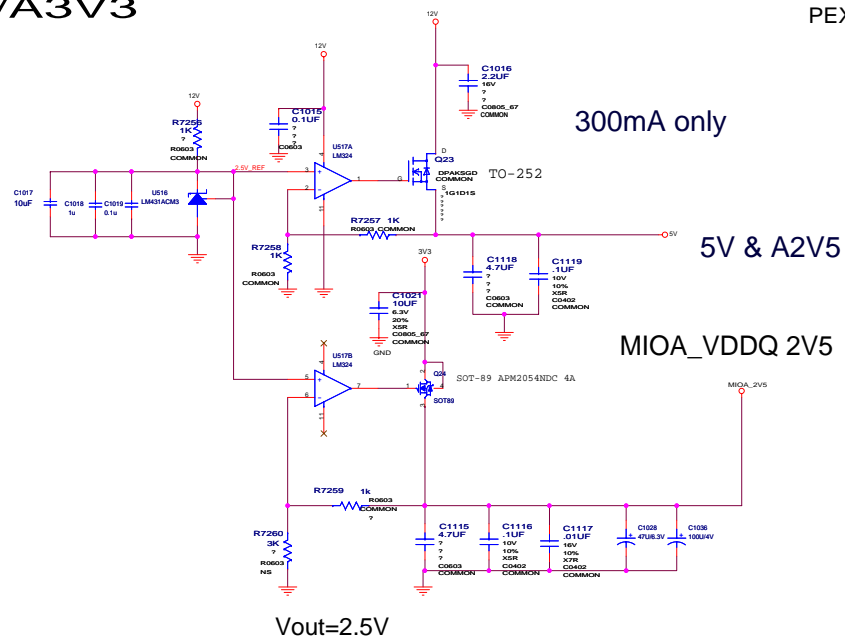
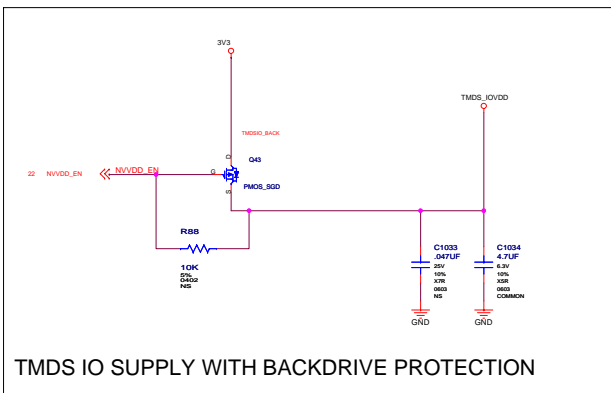
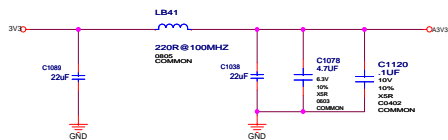
Assembly:
BIOS



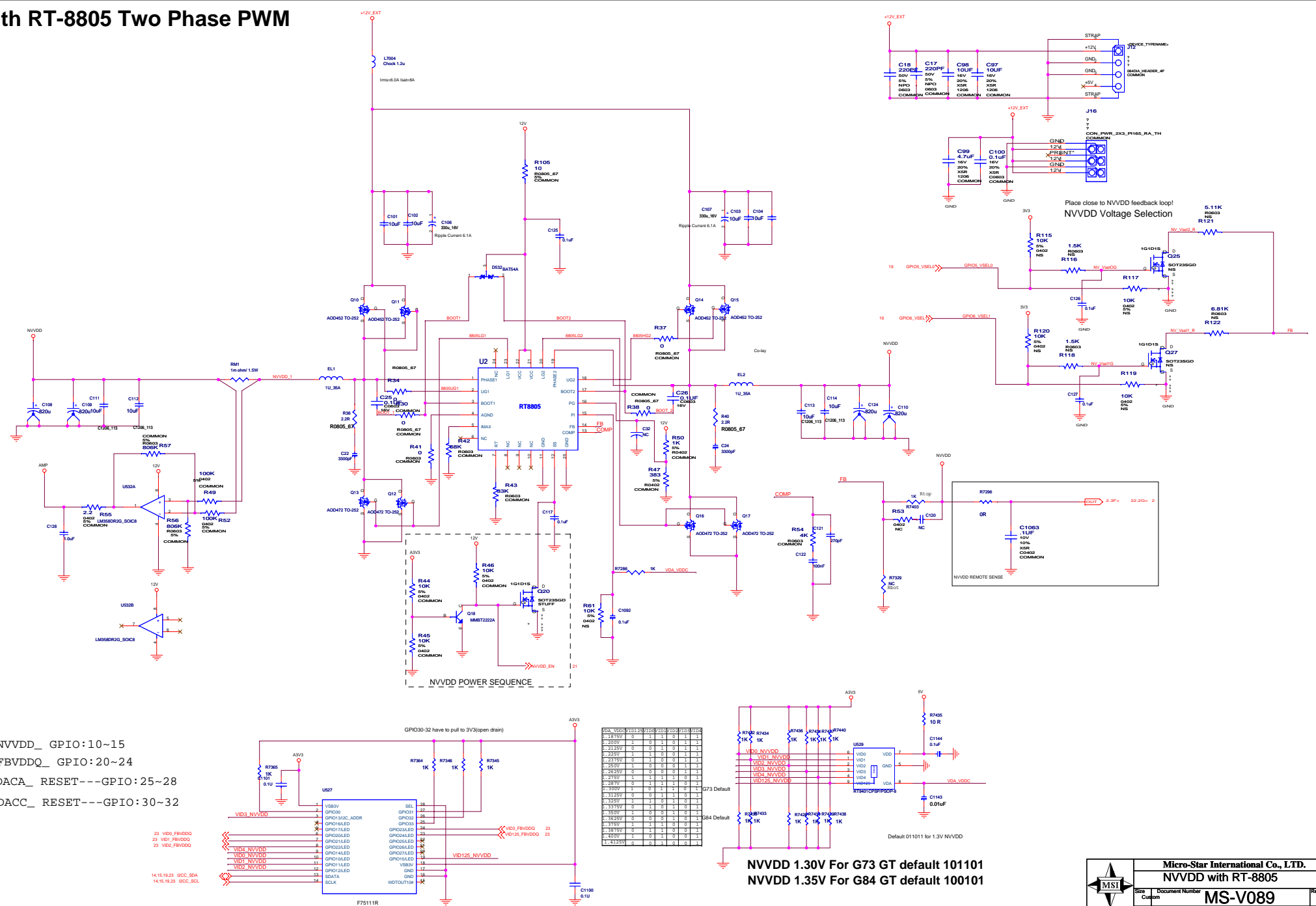
Mechanical parts



POWER_DDC5V



NVVDD with RT-8805 Two Phase PWM



NVVDD 1.30V For G73 GT default 101101
NVVDD 1.35V For G84 GT default 100101

