## P141-A05, NV31 8Mx16, 128MB, VIDEO IN/OUT, DVI-I, VGA

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## **HISTORY:**

A00

INITIAL VERSION X00:

X01: First Review

> Replaced series resistors in sync lines with 33ohms Moved clamping diodes next to GPU

Added parallel caps to EMI filter DACB Removed not needed strap on SAA7114

Connected RESET and WP of SST ROM to ROMVCC

Added parallel ROM and Strapps

Added FBVDD regulator

Added STEREO glasses circuit

Removed Decoupling CAPs on VIP VDD, covered by Caps on page 2

Added ROM\_VCC for cleaner planes

Changed used TMDS lines of IFPA and IFPB to TP from NTP

Changed Resistor for AGP Vref circuit to 158k

X02: Final Review

Added clock termination resistors

Added net name for FBCALxxx

Added cap on filter input for FB\_DLLVDD, DACA\_VDD & DACB\_VDD

Changed netnames for SAA7114 NTPs to NTP\_xxx Added 1uF cap parallel to fan connector Changed all xxCALxx resistors to 50 Ohms

Changed all FBxDQS\*<x> to NTP\_FBxDQS\*<x> with NO\_TEST property

A 0 1

X00: Fixed pin swap on parallel ROM A12 & A13

Added charge pump for SC2612

Added resitstors to swap GPIO for DACB loadtest

Added resitstors for I2C on internal Video IN connector

Updated variant information for new Sbom structure

X00: Added sw adjust for NVVDD

Exchanged TMDSIOVDD regulator to lower the voltage drop Changed TMDSPLLVDD regulator bypass to A3V3

Addrd 1k series resistor in DACB load detection circuit

A03

X00: Removed GPIO5 from NVVDD adjust

Fixed values for DAC Rset resitors Removed Sync Buffer bypass

Removed 2nd voltage selection fet Changed to new internal video connector

Added snubber to NVVDD and FBVDD regulator

Added 100 ps skew to TMDS pairs

A05

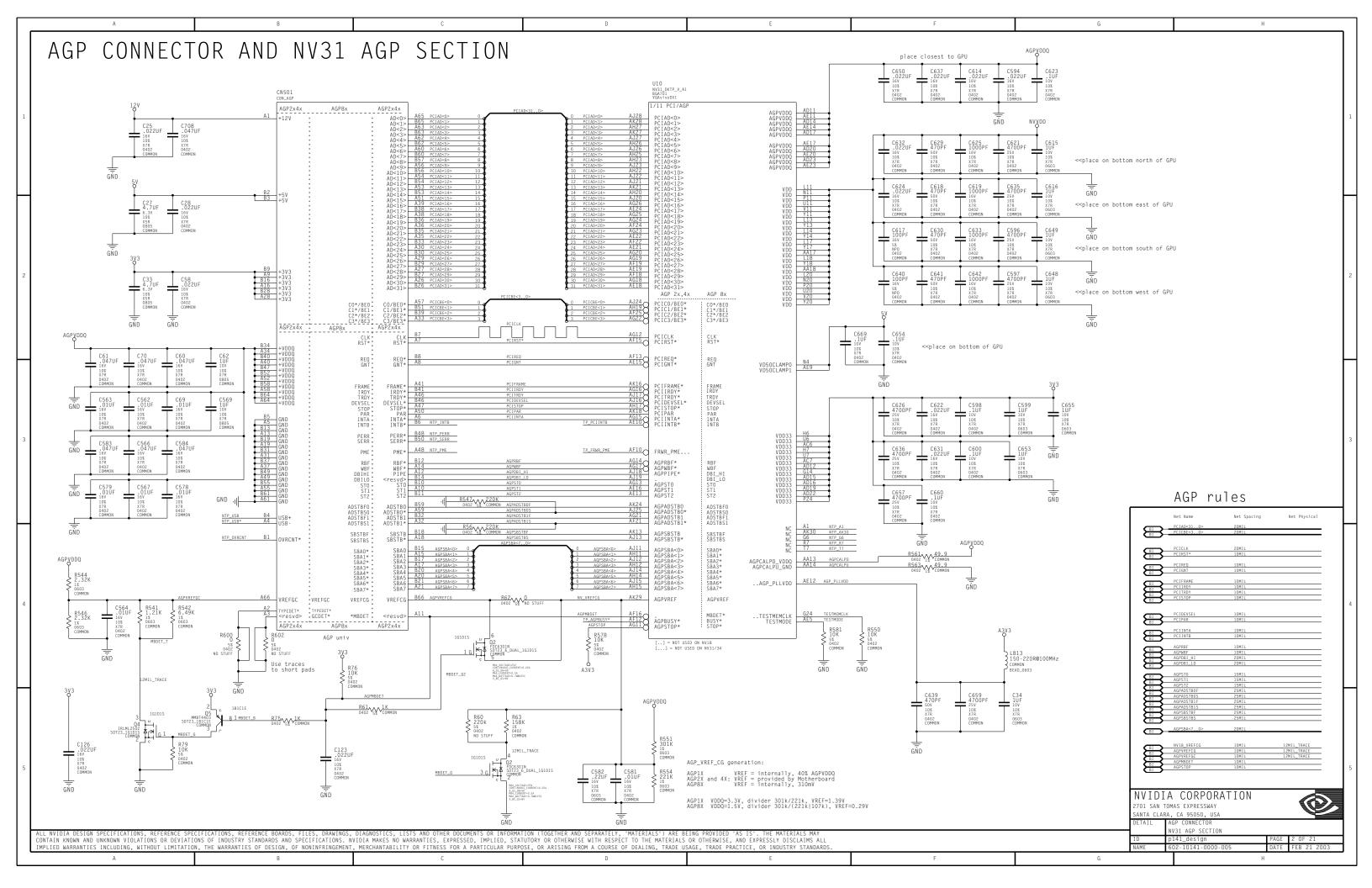
Merged CGND and GND

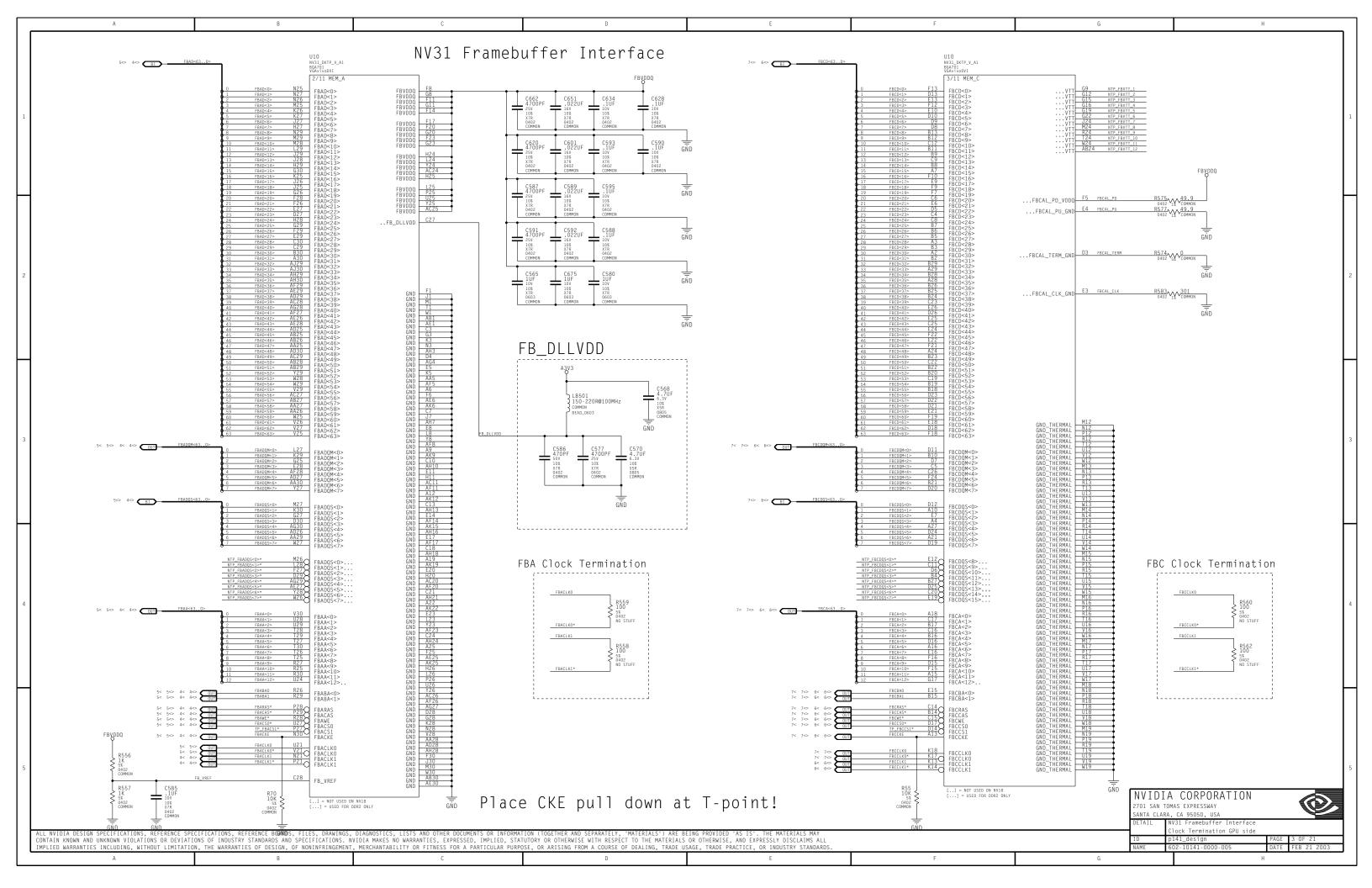
602-10141-0000-005 Base Schematic

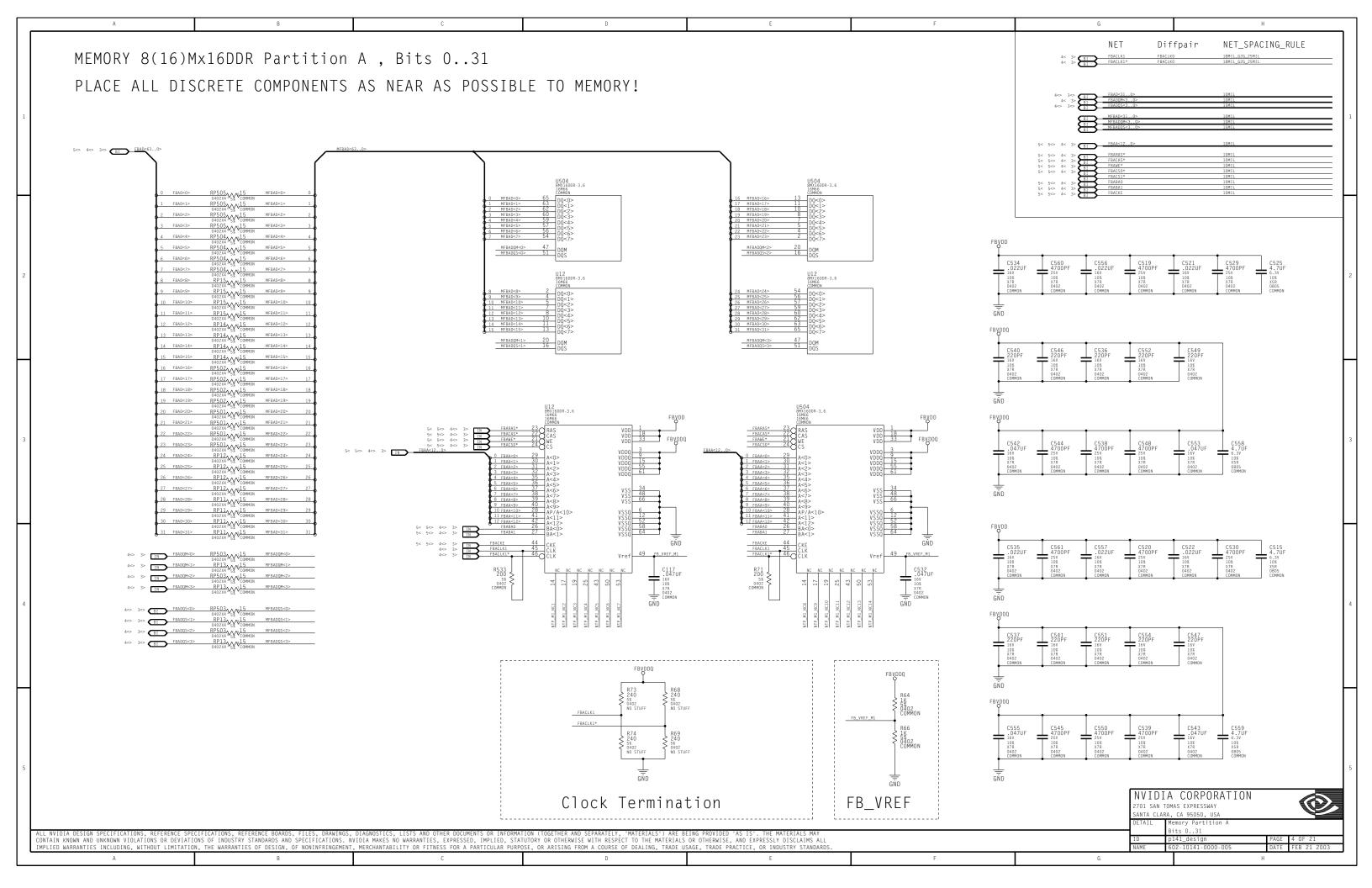
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY

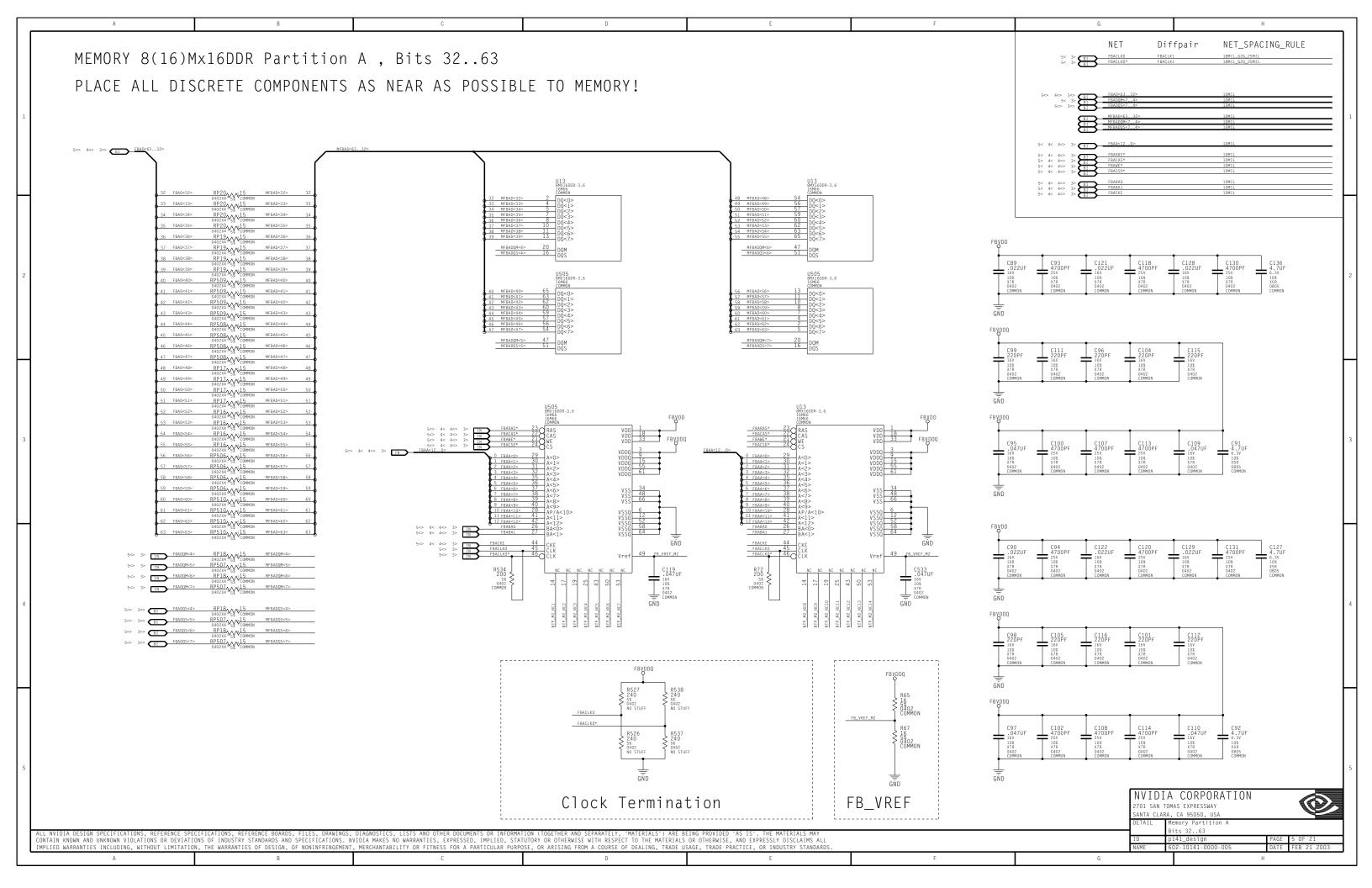
FRVIFW

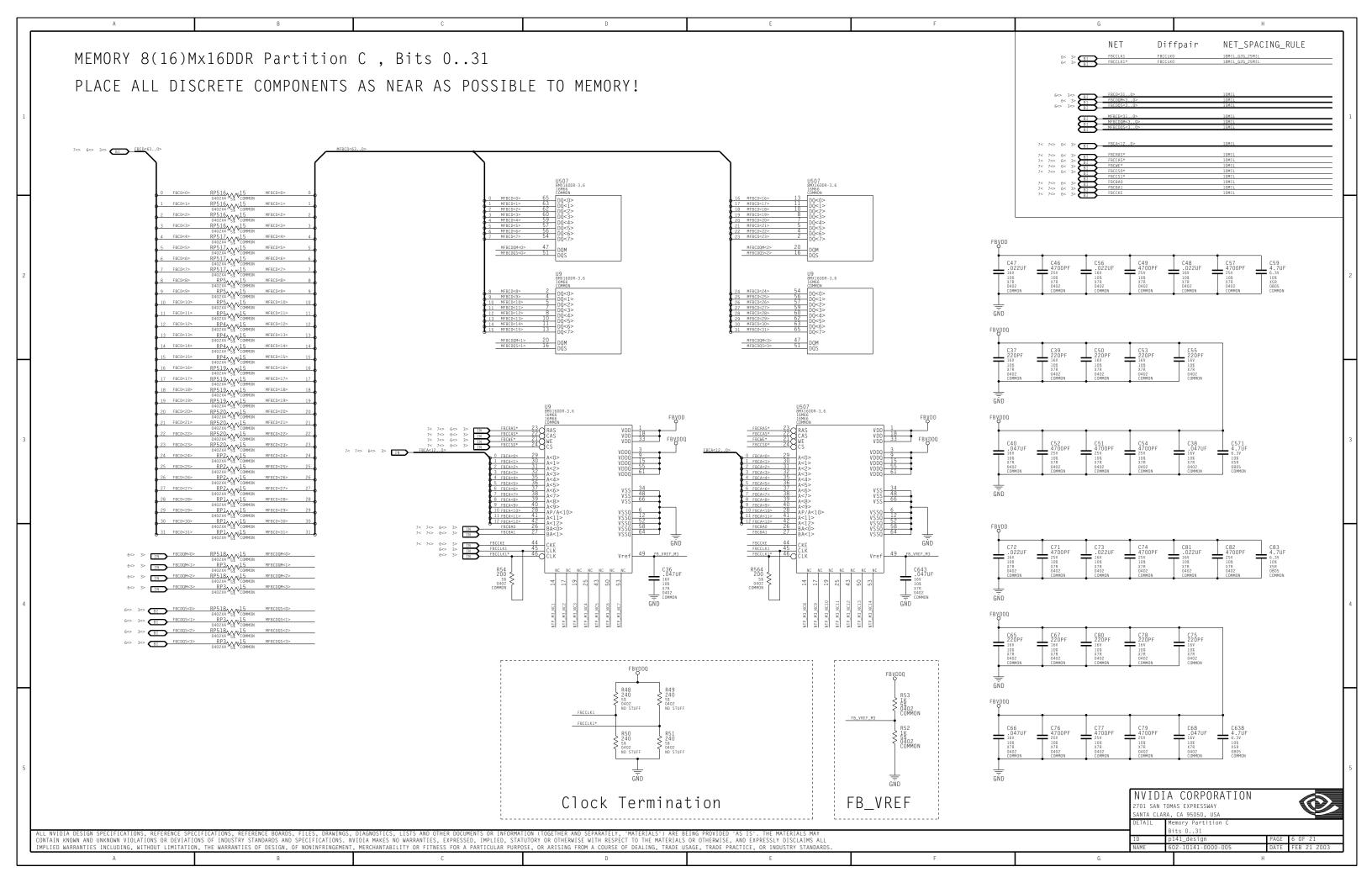
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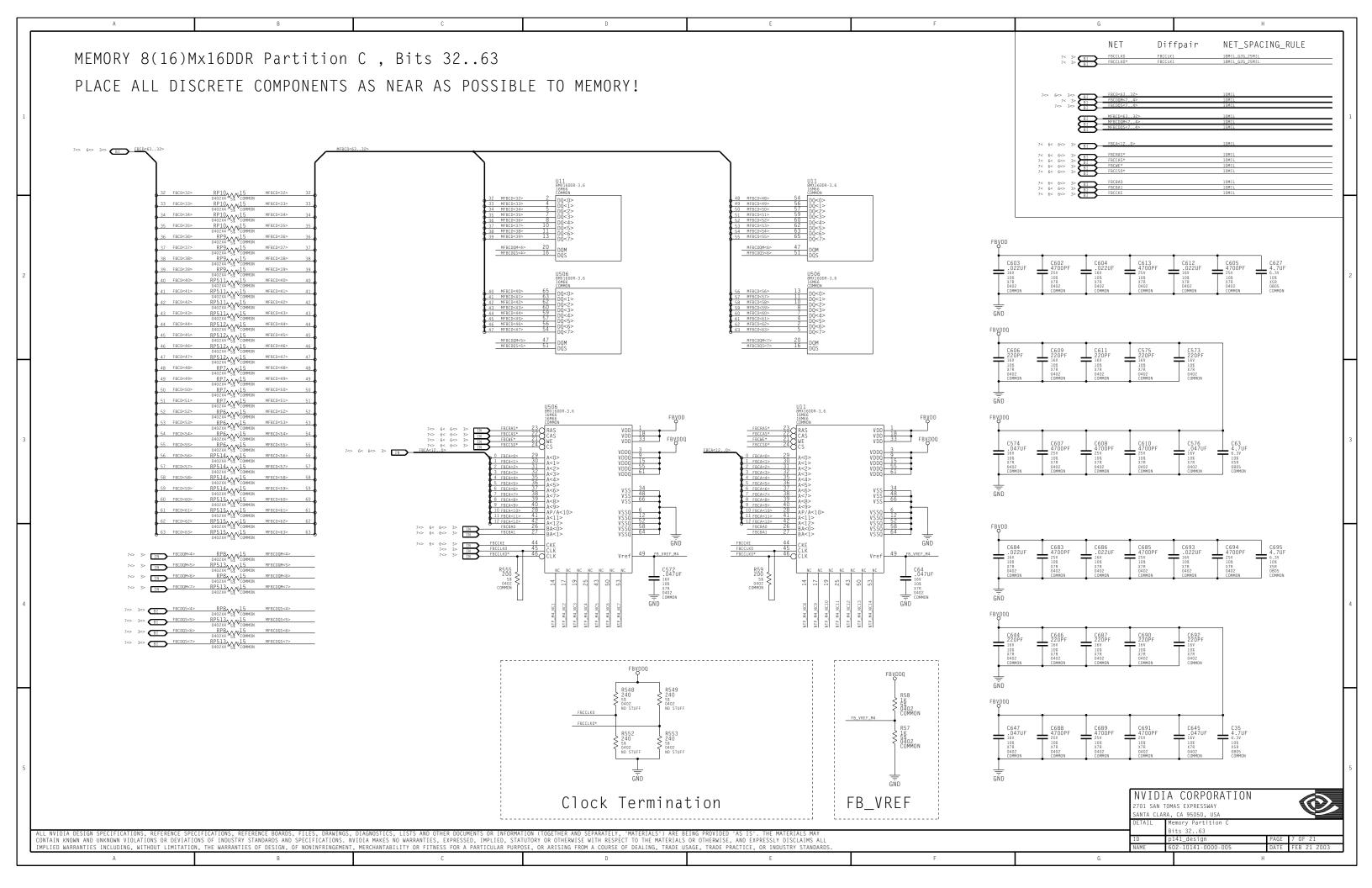


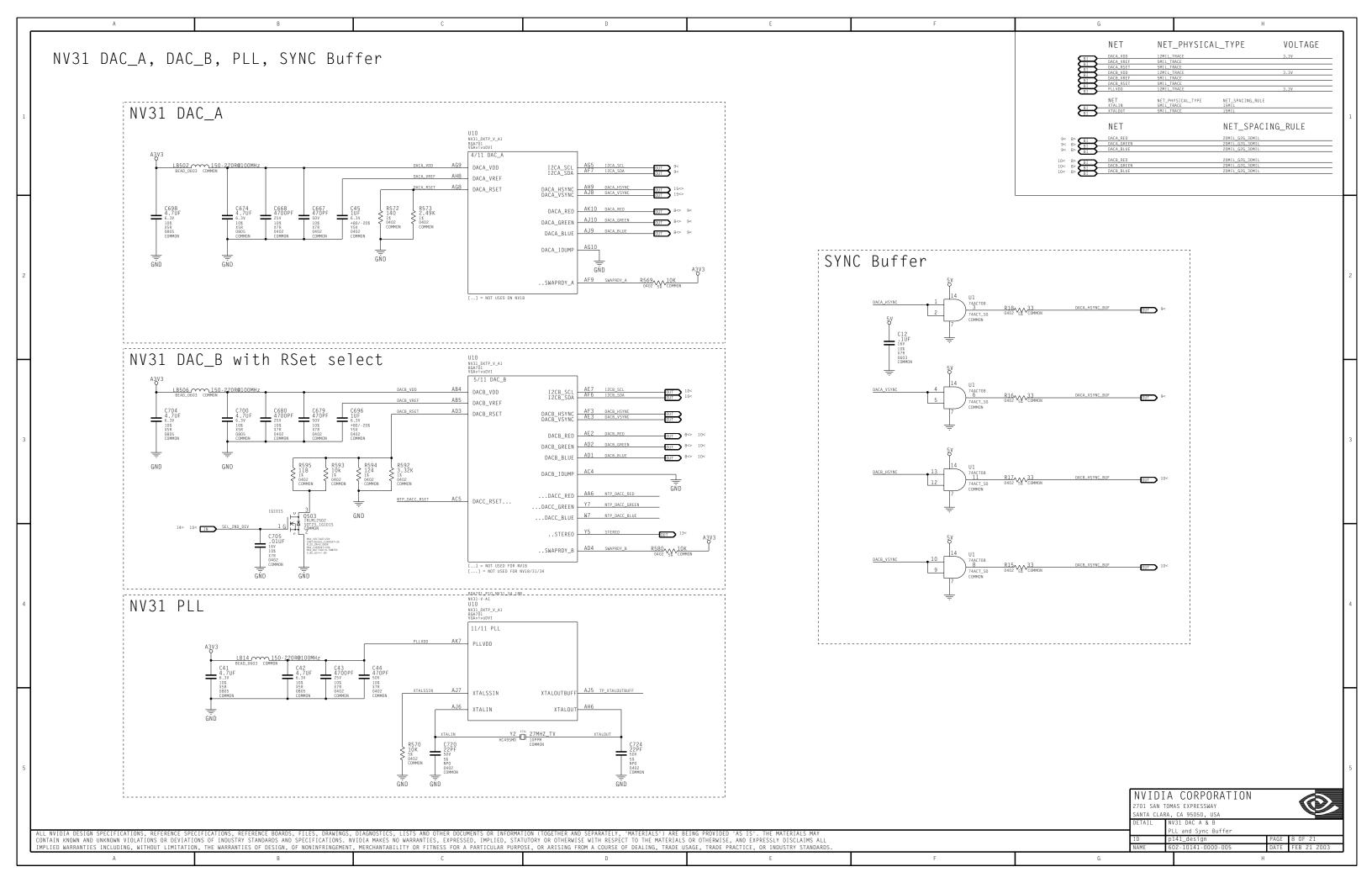


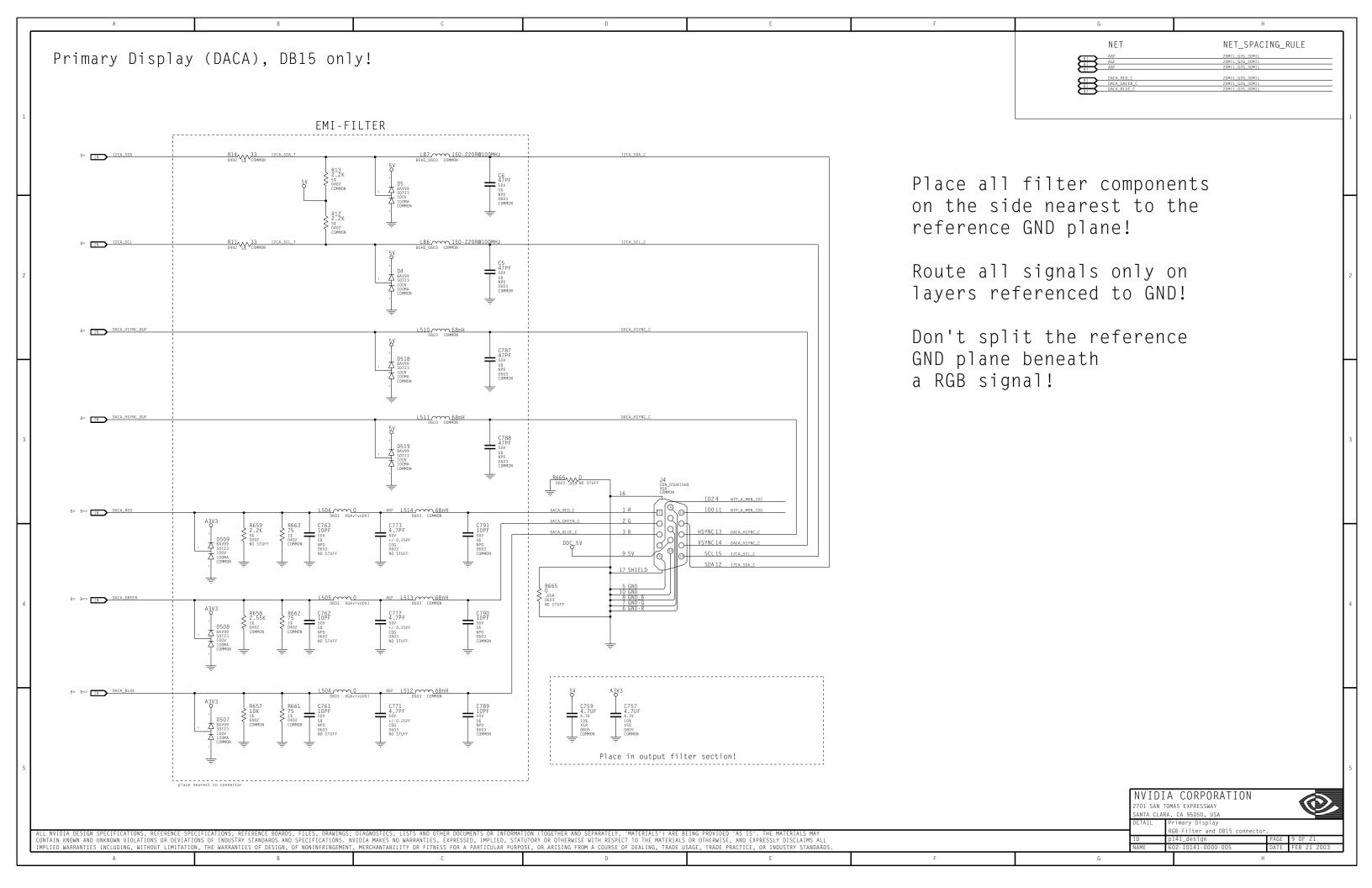


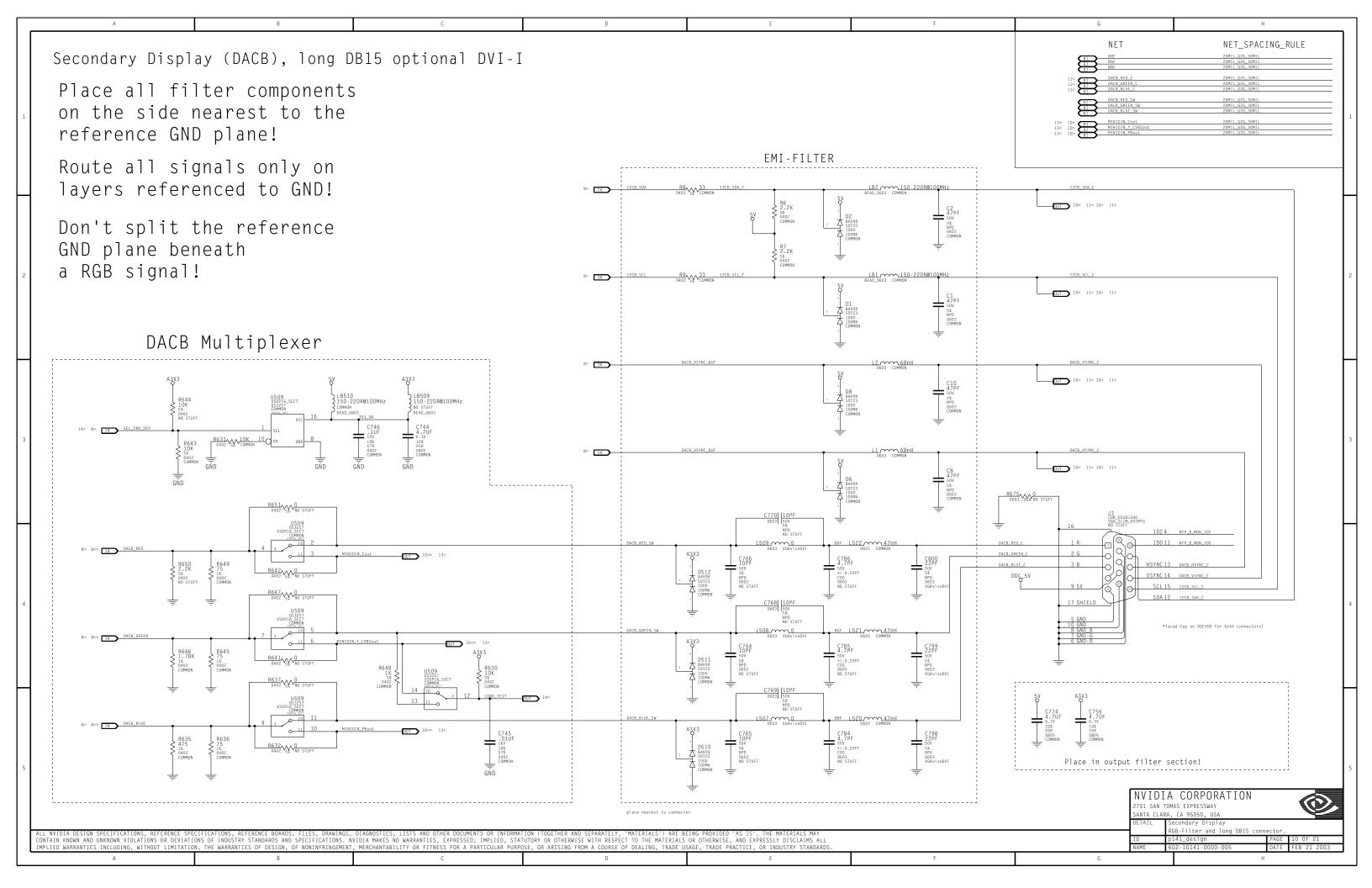


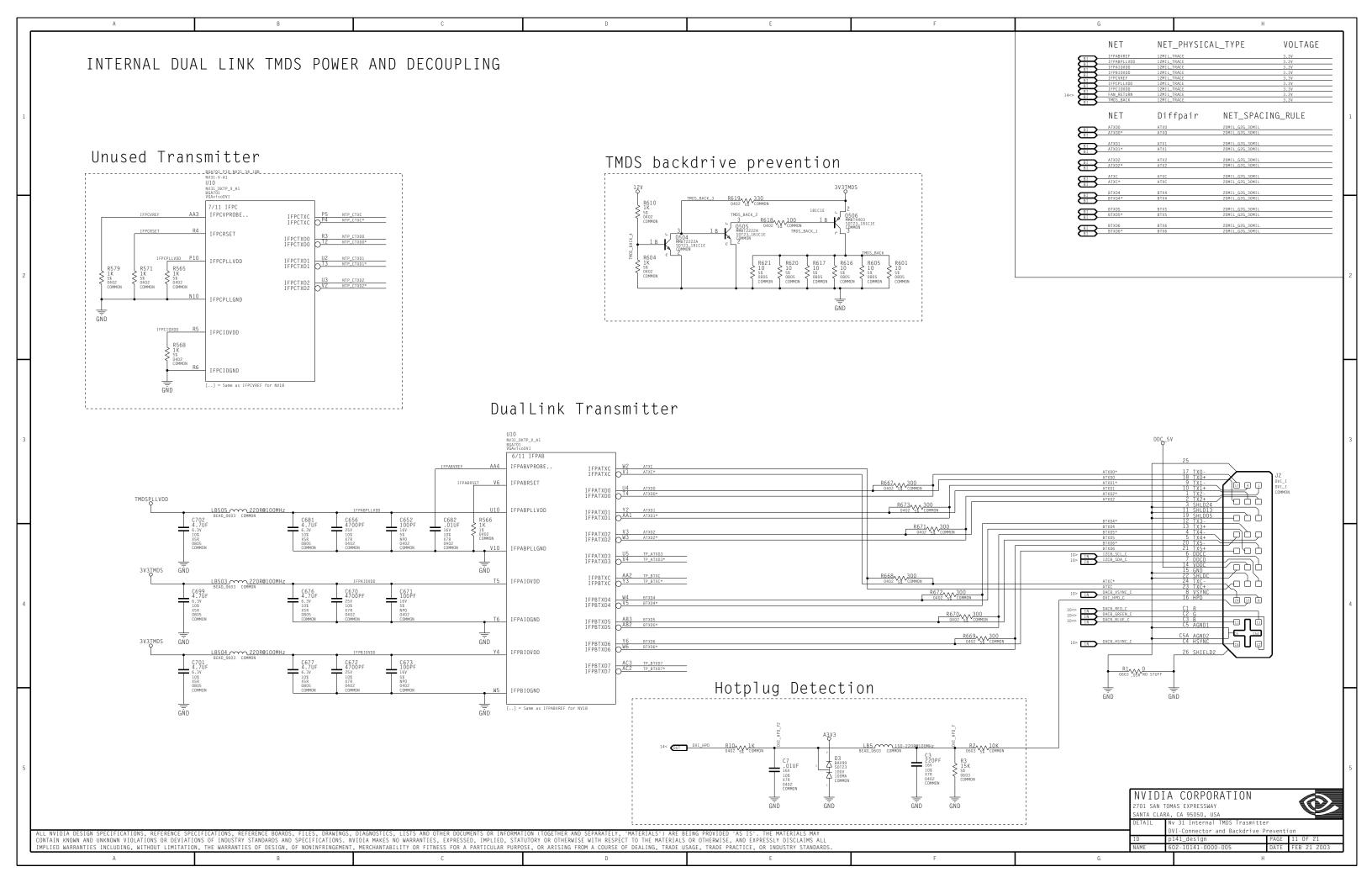


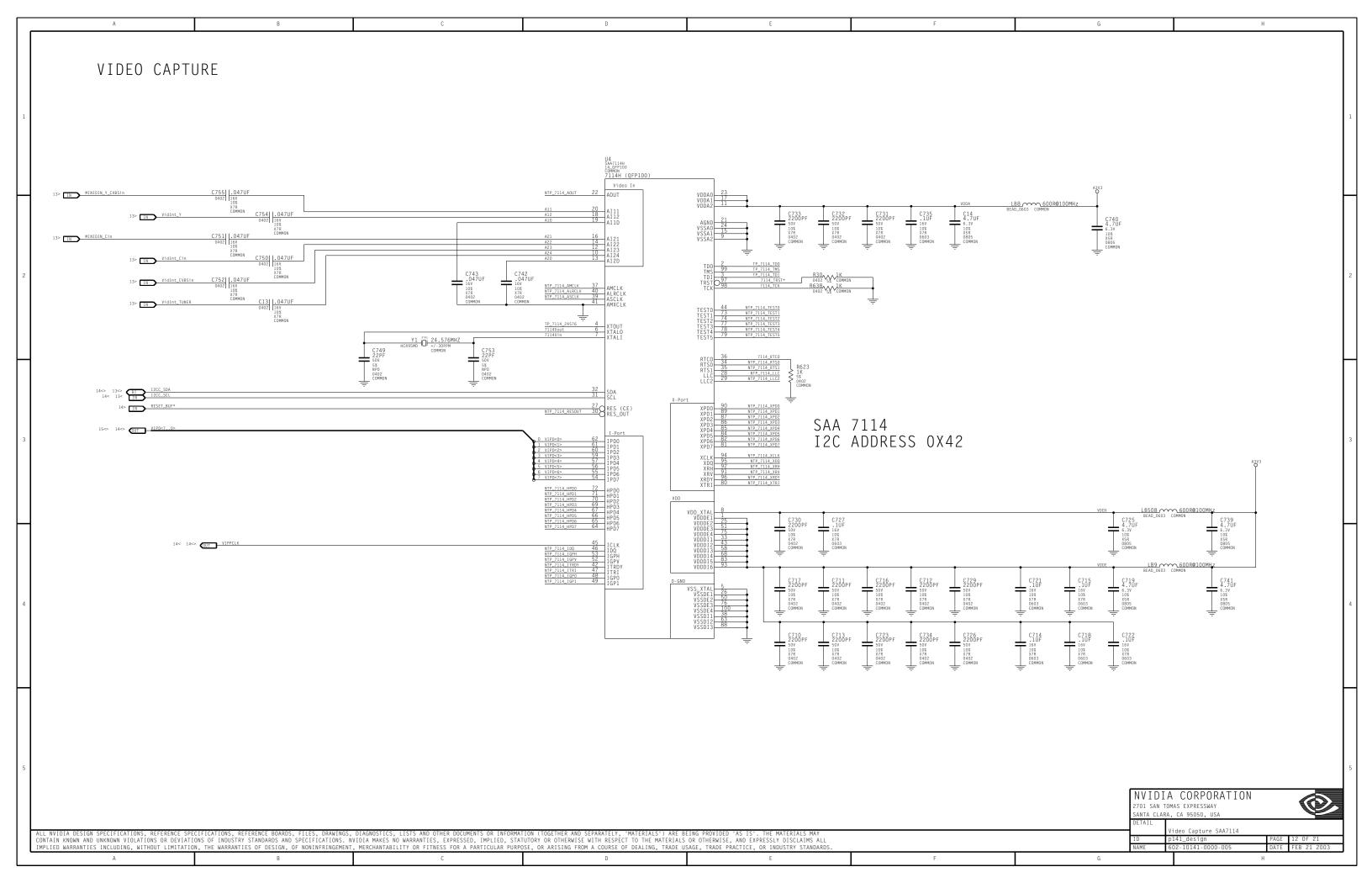


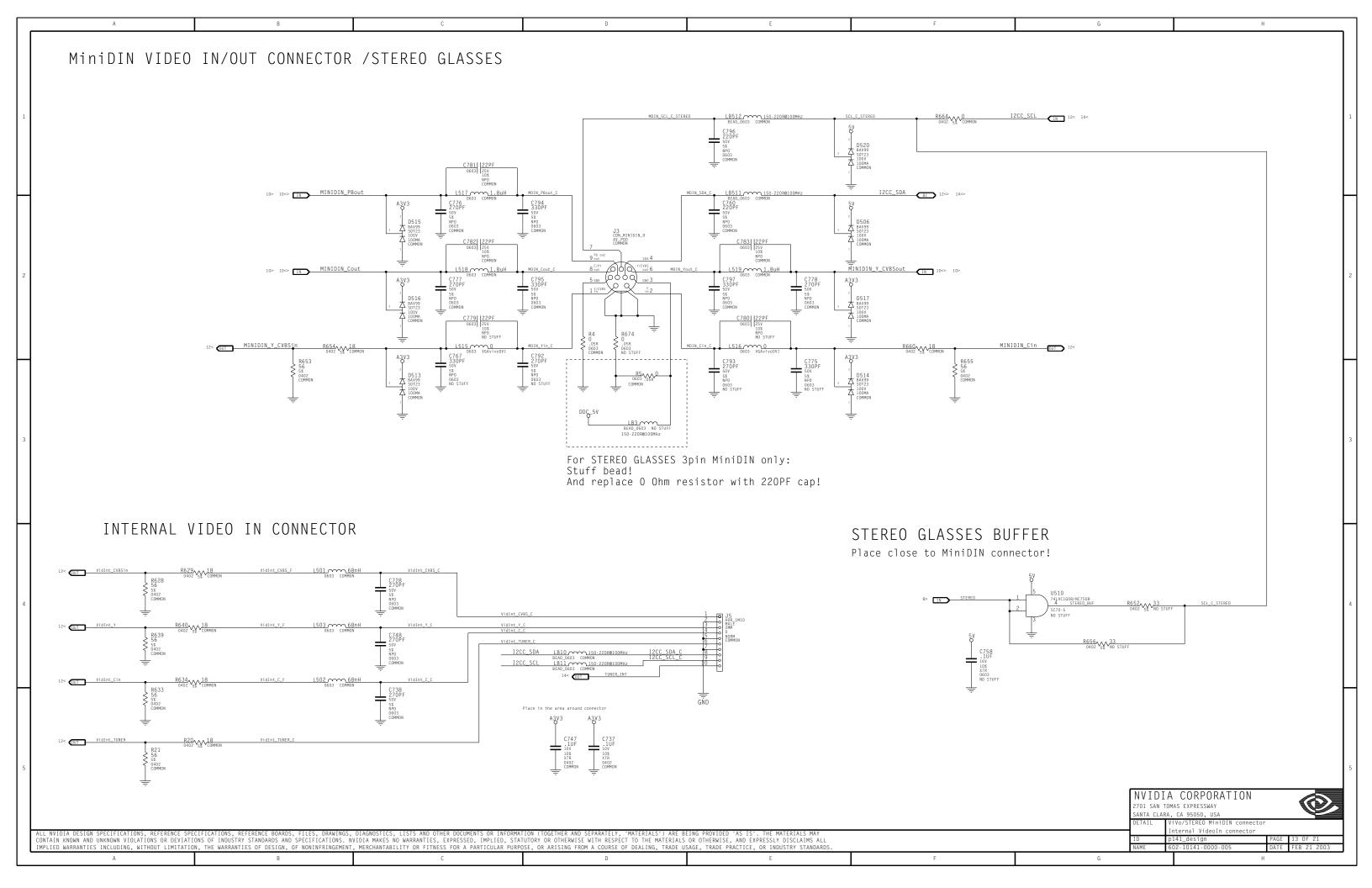


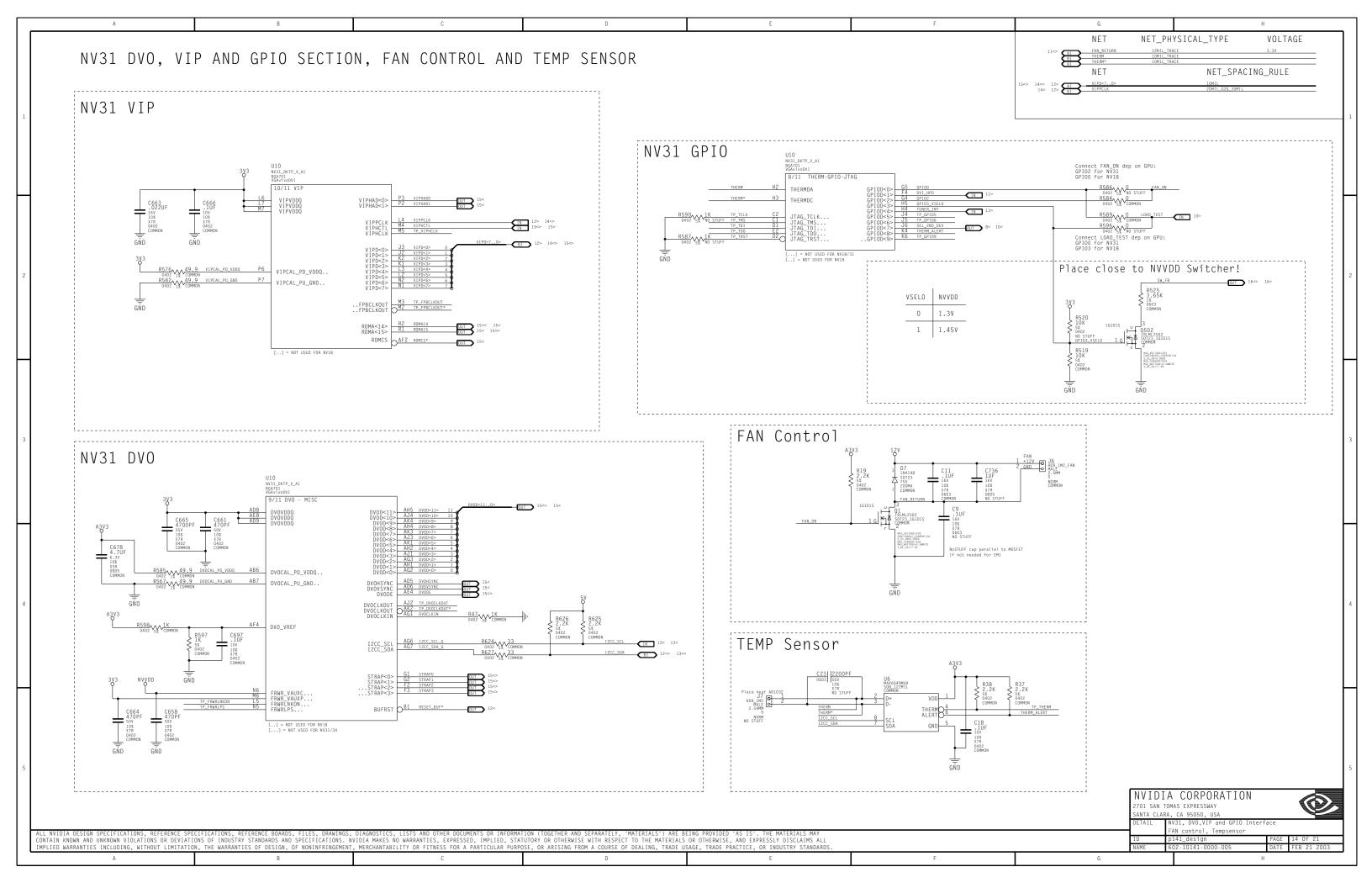


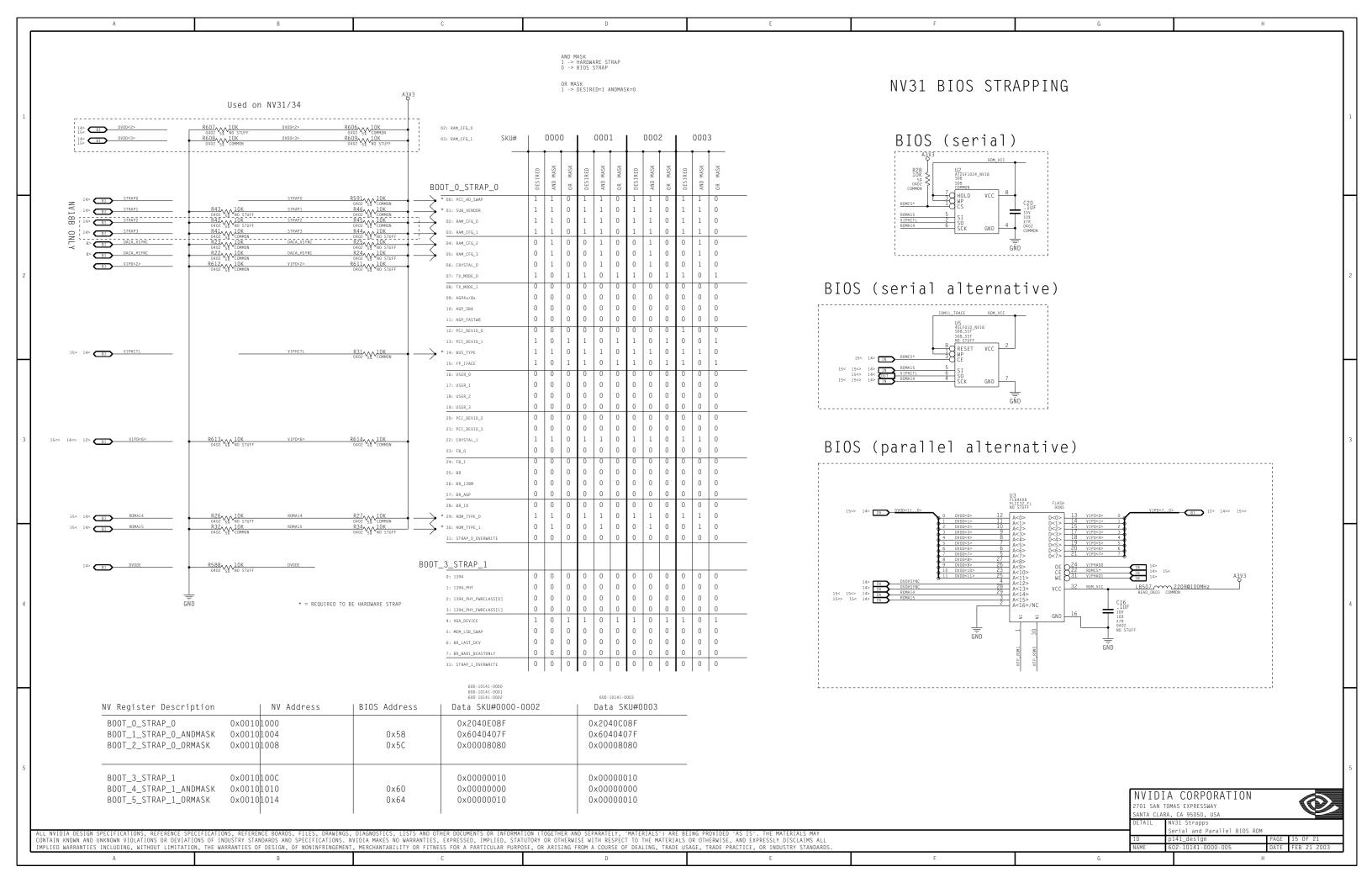


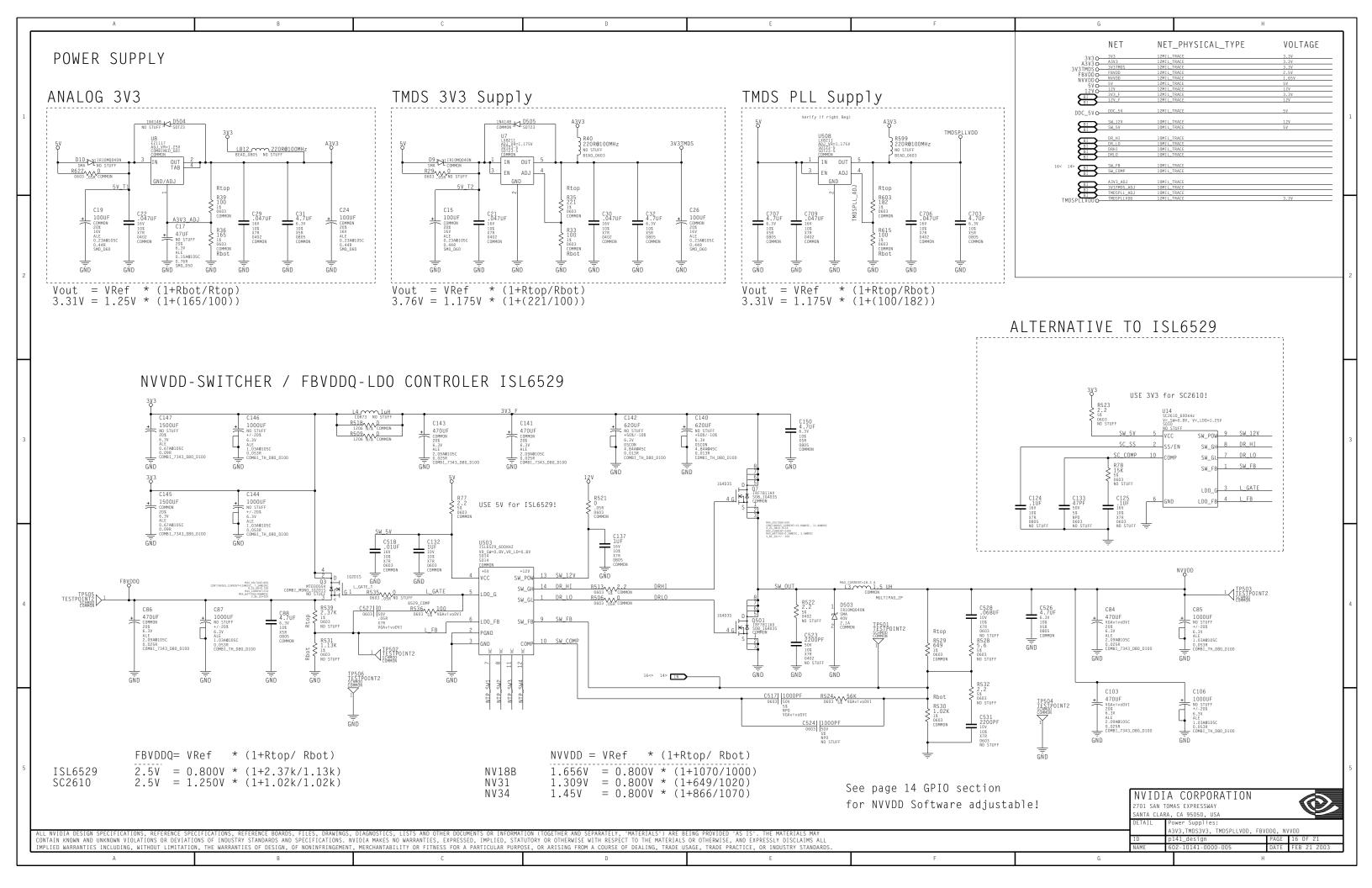


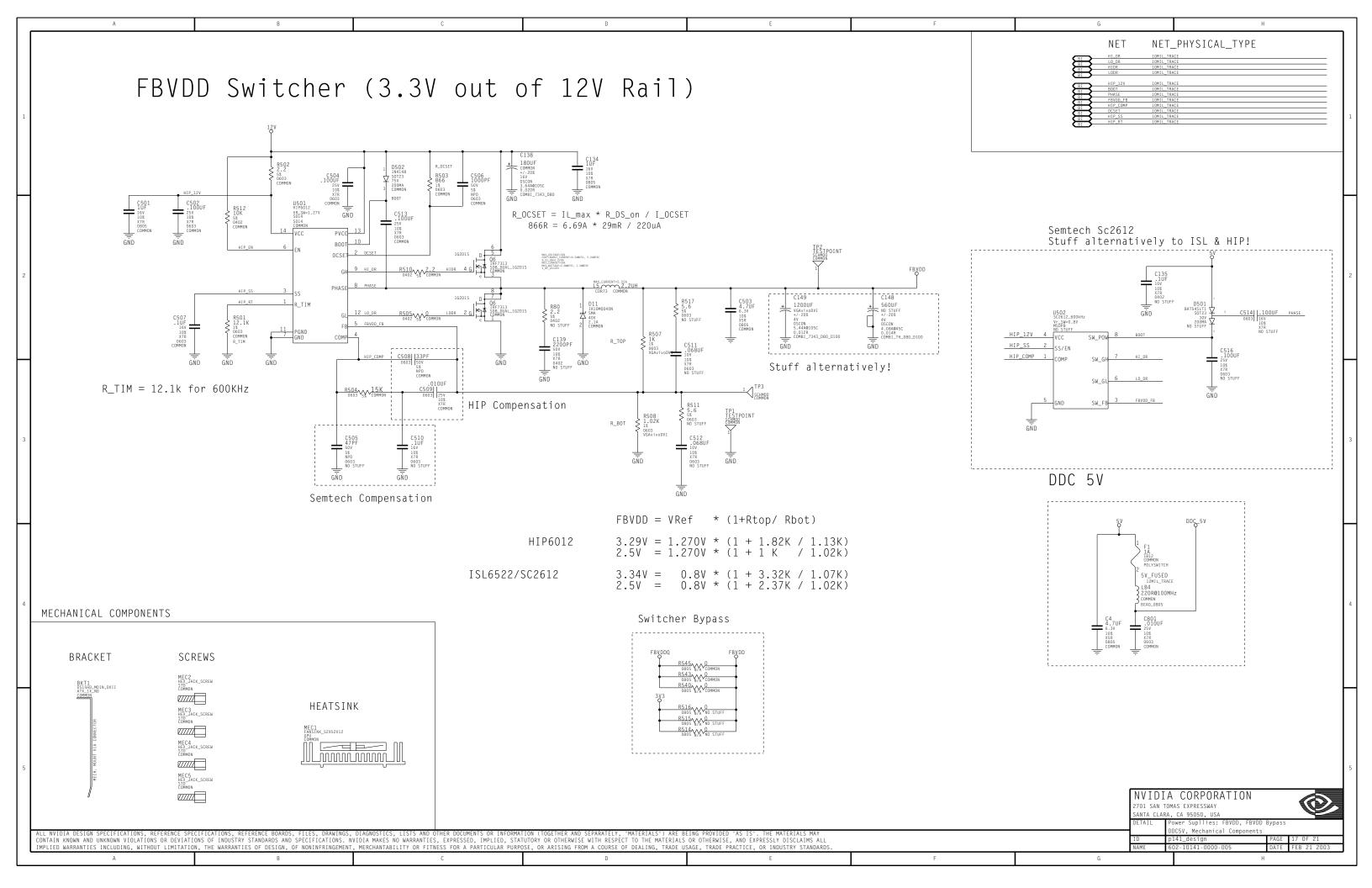












\*\*\* Signal Cross-Reference for the entire design \*\* 3.5B> 4.1G 4.3C 4.3E 5.1G FBAA<4> 3.4B 4.3C 4.3E 5.3C 5.3E FBARAS\* FBCDQS<0> 3.3F 6.4A<> MFBADQM<4> 5.2C 5.4B 3.4B 4.3C 4.3E 5.3C 5.3E 3.4B 4.3C 4.3E 5.3C 5.3E 3.4B 4.3C 4.3E 5.3C 5.3E 5.3C< 5.3E 3.5B> 4.16⇔ 4.3C< 4.3E 5.16⇔ 5.3C< 5.3E 3.4F 6.3C 6.3E 7.3C 7.3E FRAA<5> FRCDOS<3...02 MFRADOM<7...4> MFBADQM<5> MFBADQM<6> 16.1G 16.2A A3V3\_ADJ FBAA<8> 3.4B 4.3C 4.3E 5.3C 5.3E FBCA<0> FBCDQS<2> 3.3F 6.4A MFBADQM<7> 5.2E 5.4E FBAA<10> FBAA<11> FBAA<12> 9.16 9.50 3.4B 4.3C 4.3E 5.3C 5.3E FBCA<12..0> 6.1G ⇔ 6.3C < 6.3E 7.1G ⇔ 7.3C < 7.3E FBCDOS<3> 3.3F 6.4A MFBADOS<0> 4.2C 4.4E 9.16 9.4C 9.16 9.4C 2.3C 2.56 2.3C 2.56 3.4F 7.4A< FBCA<63..0 FBCDQS<7.. FBCDQS<5> 3.4E> 3.4F 6.3C 6.3E 7.3C 7.3E AGPADSTB1F 2.3C 2.5G<> FBABA0 3.5B> 4.1G \$\infty 4.4C < 4.4E 5.1G \$\infty\$ FBCA<2> 3.4F 6.3C 6.3E 7.3C 7.3E FBCDOS<6> 3.4F 7.4A<> MFBADOS<3> 4.2E 4.4B 3.4F 6.3C 6.3E 7.3C 7.3E AGPANSTRIS 2 30 2 56<> 5.4C< 5.4E FRC4<3> FRCDOS<75 3 AF 7 AA<> MERADOS<4> 5.2C 5.4B 2.3C 2.4G 2.3C 2.4G 2.3C 2.4G 2.4D 2.5C 2.5G 5.4C< 5.4E 3.5B> 4.1G $\Leftrightarrow$  4.4C< 4.4E 5.1G $\Leftrightarrow$ 5.4C< 5.4E 3.5B> 4.1G $\Leftrightarrow$  4.3C< 4.3E 5.1G $\Leftrightarrow$ FBABA1 FBCRAS\* 3.5E> 6.1G⇔ 6.3C< 6.3E 7.1G⇔ AGPDBI\_LO MFBADQS<5> FBCWE\* 3.5E> 6.1G⇔ 6.3C< 6.3E 7.1G⇔ FBACAS\* FBCA<6> AGPMBDET MFBADQS<6> 5.2E 5.4E AGPRBF 2.3C 2.4G<> 5.3C< 5.3E FBCA<7> 3.4F 6.3C 6.3E 7.3C 7.3E 7.3C< 7.3E MFBADOS<7> 5.2E 5.4B 5.3L< 5.3E 3.5B> 4.2G<> 4.4C< 4.4E 5.2G<> 5.4C< 5.4E 3.4F 6.3C 6.3E 7.3C 7.3E FBVDD\_FB HIDR HIP\_12V 17.16 > 17.20 17.36 17.16 > 17.20 17.1A 17.16 > 17.2F FBCA<8> FBCA<9> FBACKE 3.4D 3.5B> 5.1G >> 5.4C < 5.4E 5.5D 2.4C 2.4D FBCA<10 MFBCD<63..0> AGPSBA<1> HIP\_COMP HIP\_RT HIP\_SS HI\_DR AGPSBA<2> 2.4C 2.4D FBACLKO\* 3.4D 3.5B> 5.1G $\Leftrightarrow$  5.4C< 5.4E 5.5D 3.4D 3.5B> 4.1G $\Leftrightarrow$  4.4C< 4.4E 4.5D FBCA<11> 3.4F 6.3C 6.3E 7.3C 7.3E 17.16⇔ 17.2C 17.2F 17.16⇔ 17.2B MFBCD<1> 6.2B 6.20 AGPSBA<3> 2.40 2.40 FBACLK1 FBCA<12 3.4F 6.3C 6.3E 7.3C 7.3E MFBCD<2> 6.2B 6.2C 3.4D 3.5B> 4.1G $\diamondsuit$  4.4C< 4.4E 4.5D 3.5B> 4.1G $\diamondsuit$  4.3C< 4.3E 5.1G $\diamondsuit$ 17.16 17.28 17.2F 17.16 17.2C 17.2G FBACLK1 FBACSO\* FBCBA0 FBCBA1 3.5E> 6.1G<> 6.4C< 6.4E 7.1G<> I2CA\_SCL 8.1D> 9.2A< AGPSBA<6> 2.4C 2.4D 5.3C< 5.3E MFBCD<5> 6.2B 6.2C AGPSBA<7> 2.4C 2.4D 2.4C 2.5G<> FBACS1\* 7.4C< 7.4F IZCA SDA 8.1D> 9.1A< 8.3D> 10.2D< MERCD<6> 6.2B 6.20 FBAD<0>
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MFBCDQM<3> DRLO DR\_HI DR LO 16.1G → 16.3H 16.4D FBAD<60> 3.3B 5.3A FBCD<49> 3.2F 7.3A MFBAD<43> 5.2B 5.2C MFBCDOM<4> 7.2C 7.4B FBAD<61> FBAD<62> FBAD<63> 3.3B 5.3A 3.3B 5.3A 3.3B 5.4A 5.2B 5.2C 5.2B 5.2C 5.2B 5.2C 11.5D> 14.2F< FBCD<50 MFBAD<44> MERCHOM<7 4> 14.4C 15.3F 14.3D> 15.3F< FBCD<51> FBCD<52> MFBAD<45> MFBAD<46> MFBCDQM<5> MFBCDQM<6> DV0D<1> 14.4C 15.3F FBADQM<0> 3.3B 4.4A< FBCD<53> 3.3F 7.3A MFBAD<47> 5.2B 5.2C 5.2E 5.3B MFBCDQM<7> DVOD<2> 14.4C 15.1A⇔ 15.1B 15.4F FBADOM<3..0> FBCD<54> 3.3F 7.3A MFBAD<48> MFBCDOS<0> 6.2C 6.4B FBADQM<63..0> FBADQM<1> MFBAD<49> MFBAD<50> 5.2E 5.3B 5.2E 5.3B 14.4C 15.1A >> 15.1B 15.4F MFBCDOS<3..0> 3.3B 4.4A< 3.3B 4.4A< MFBCDQS<1> MFBCDQS<2> DV0D<5> 14.4C 15.4F FBADQM<2> FBCD<57> 3.3F 7.3A MFBAD<51> 5.2E 5.3B 6.2E 6.4B DV0D<6> 14.4C 15.4F 14.4C 15.4F FBADQM<3> 3.3B 4.4A< FBCD<58> FBCD<59> 3.3F 7.3A 3.3F 7.3A MFBAD<52> MFBAD<53> 5.2E 5.3B 5.2E 5.3B MFBCDQS<3> 6.2E 6.4B 7.2C 7.4B DV0D<7> FBADOM<4> 3.3B 5.4A< MFBCDOS<4> FBADQM<7. FBADQM<5> MFBCDQS<7..4> MFBCDQS<5> MFBCDQS<6> DV0D<10: 14.3C 15.4F FBADQM<6> 3.3B 5.4A< FBCD<62> 3.3F 7.3A MFBAD<56> 5.2E 5.3B 7.2E 7.4B DV0D<11> 14.3C 15.4F 14.4C> 15.4A<> 15.4B FRADOM<7> 3.38 5.4A< FBCD<63> MERAD<57> MERCDOS<7> 7.2F 7.4B 12.2A< 13.2G> 10.1G<> 10.4C> 13.2B< 10.1G<> 10.5C> 13.2B< FRANCS<0> 3.3B 4.4A FRCDOM<0: 3.3F 6.4A< MFBAD<58> MINIDIN CIN MFBAD<59> MFBAD<60> 14.4C> 15.4F< FBADQS<63..0> FBCDQM<63..0> MINIDIN\_PBOUT 3.3B 4.4A FAN\_RETURN 11.1G⇔ 14.1G⇔ 14.3F FBADQS<1> FBCDQM<1> 3.3F 6.4A< MFBAD<61> 5.2E 5.3B MINIDIN\_Y\_CVBSIN 12.2A< 13.2B> 3.4B 4.3C 4.3E 5.3C 5.3E FRADOS<2> 3.38 4.4A< FBCDOM<2> 3.3F 6.4A< MFRAD<62> MINIDIN Y CVBSOUT 10.16 10.4C 13.2E NV18\_VREFCG OCSET PCIAD<0> FBADOS<3> FBAA<63..0> 2.1C 2.1D FBADQS<7..4> FBCDQM<7..4> MFBADQM<3..0> 4.1G<> NVIDIA CORPORATION 3.4B 4.3C 4.3E 5.3C 5.3E FBAA<1> FBADQS<5> 3.4B 5.4A<> FBCDQM<5> 3.3F 7.4A< MFBADQM<1> 4.2C 4.4B PCIAD<31..0> 2.1D 2.4G<> FBAA<2> FBADQS<6> 3.4B 5.4A FBCDQM<6> 3.3F 7.4A< MFBADQM<2> PCIAD<1> 2.1C 2.1D 2701 SAN TOMAS EXPRESSWAY ONTINUED. ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS DATE FEB 21 2003 G

