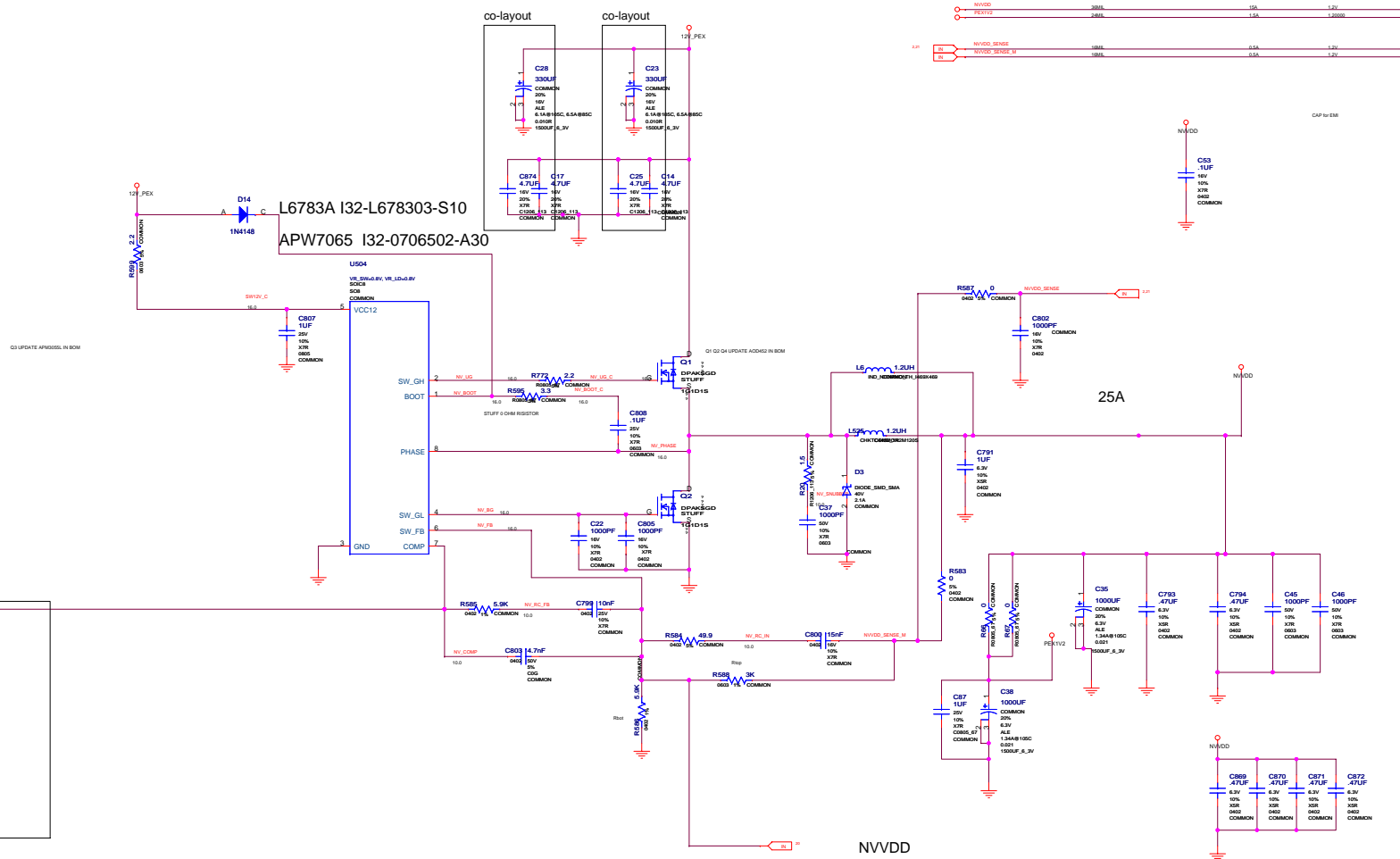
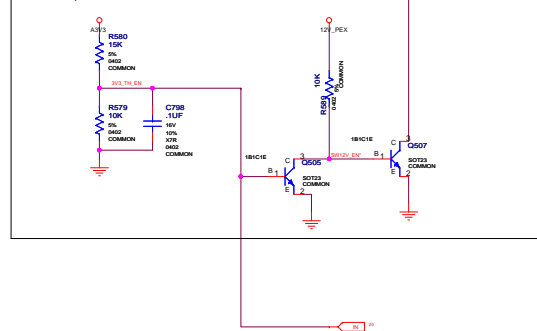


# PowerSupplyII: NVVDD

## Power Sequence



## NVVDD

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

$$1.1V = 0.8V * (1 + (1.54k/4.02k)) \quad (ISL6549)$$

$$1.2V = 0.8V * (1 + (1.54k/3.09k)) \quad (ISL6549)$$

$$1.2V = 0.8V * (1 + (10k/20k)) \quad (APW7065)$$

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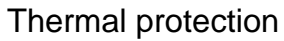


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## thermal protection and dynamic NVVDD



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PAGE DETAIL	thermal protection and dynamic NVDD

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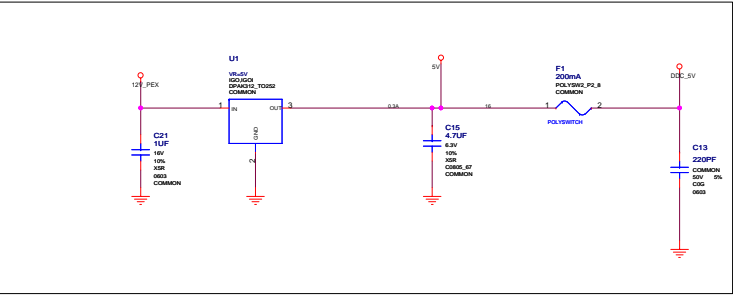


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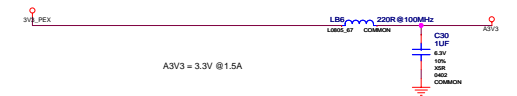
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NAME		DATE	12-JAN-2007

Power Supply:TMDS\_IOVDD A3V3 DDC\_5V IFP\_PLLVDD FBVDDQ

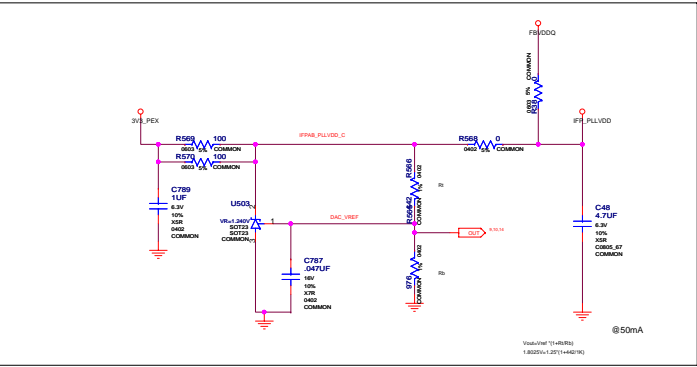
DDC 5V



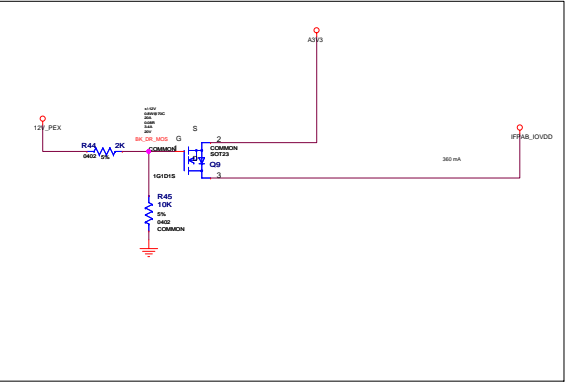
A3V3 Power Supply



IFP\_PLL\_SUPPLY

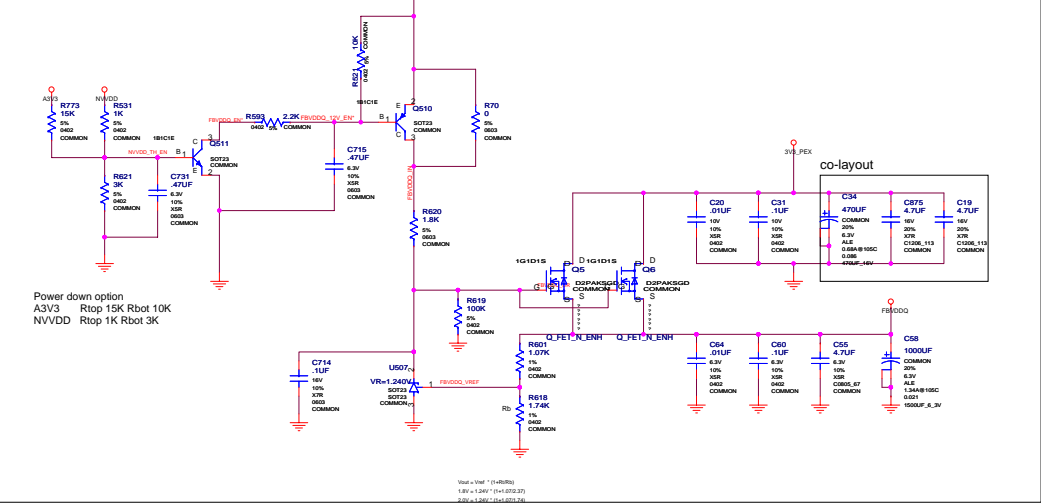


TMDS IO SUPPLY WITH BACKDRIVE PROTECTION



FBVDDQ

Power Sequence



NETNAME MAX\_CURRENT MIN\_LINE\_WIDTH VOLTAGE

DDC_5V	0.1A	12.0	5.00000V
A3V3	1.5A	30.0	3.30000V
IFPAB_OVDD	0.3A	16	3.30000V
GND		30.0	0.00000V
IFP_PLLVDD	0.3A	16	1.80000V

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: TMDS IOVDD_5V_A3V3

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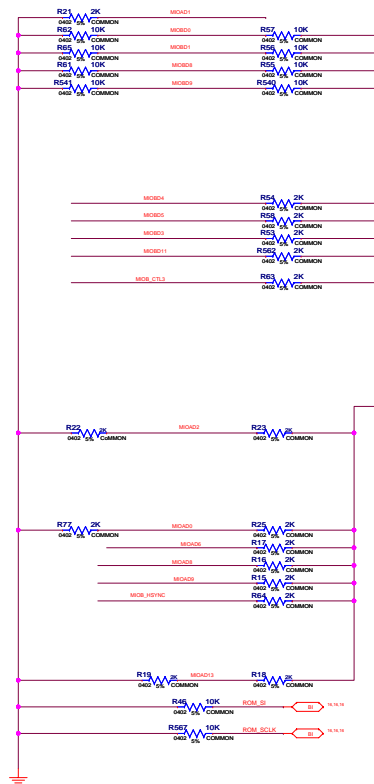
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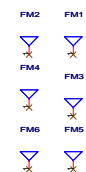
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## Straps



17 PEK_RL_EN_TERM00	0 (default - internal term only)	
18 SG0_PACQCT_LUT_ADR01	0000-Default 0001-Abalone	1001-Abalone HTMR0 NAAMP
19 SG0_PACQCT_LUT_ADR01	0101-Abalone NTHRS LLAMP 0011-Abalone NTHRS LAMP	1001-Abalone HTMR0 LLAMP 1101-Abalone HTMR0 LAMP
20 SG0_PACQCT_LUT_ADR02	0102-Abalone NTHRS LLAMP 0012-Abalone NTHRS LAMP	1102-Abalone HTMR0 LLAMP 1002-Abalone HTMR0 LAMP
21 SG0_PACQCT_LUT_ADR02	0103-Abalone NTHRS HHAMP 0013-Abalone NTHRS HHAMP	1103-Abalone HTMR0 HHAMP 1003-Abalone HTMR0 HHAMP
21-30 SG0_PACQCT_LUT_ADR02	0111-Abalone NTHRS HHAMP 0000-Default HTMR0	1111-Abalone HTMR0 HHAMP 1111-Abalone HTMR0 HH00A

REG: NV_STAP_1		
Bit Signal	VALUE_ID	VALUEs
15: Set Clock Configuration		0:Disable 1:Enable
12: MIO_EN_33V_0	MIOA_VDDQ Voltage	0:2.5V 1:3.3V
13: MIO_EN_33V_1	MIOB_VDDQ Voltage	0:2.5V 1:3.3V
16: PCI_J0BAR		0:Disable 1:Enable

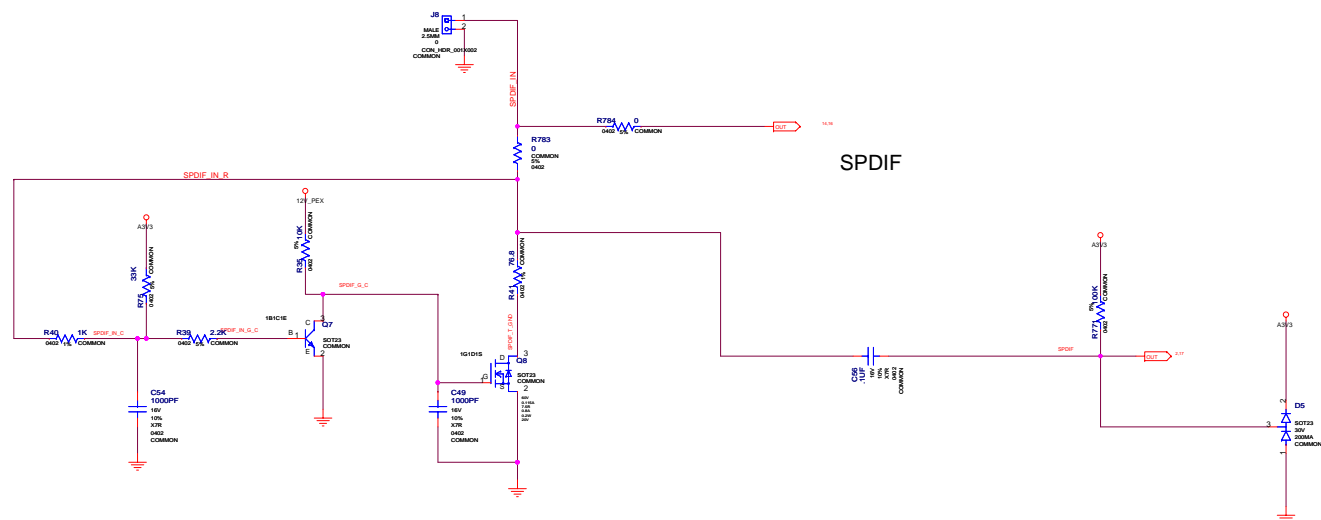
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## SPDIF



place close to GPU

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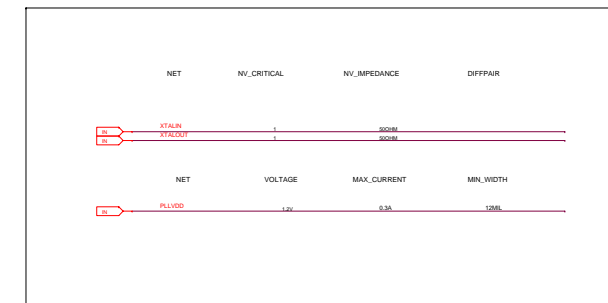
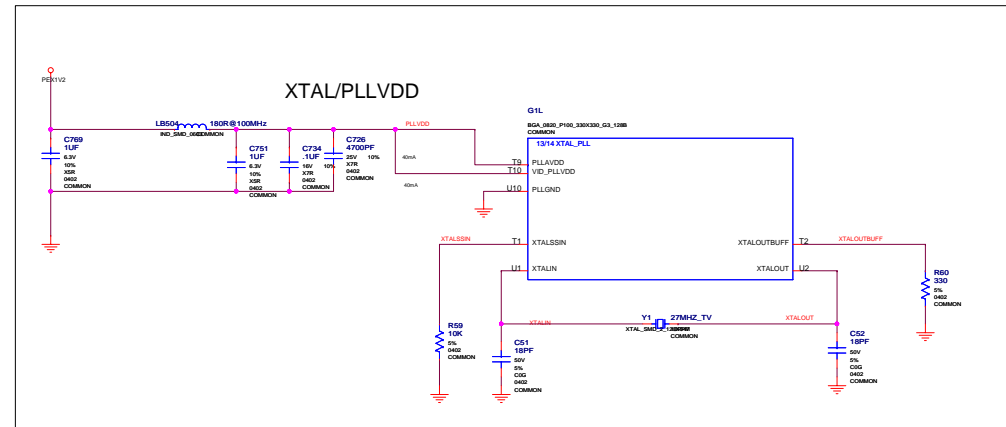
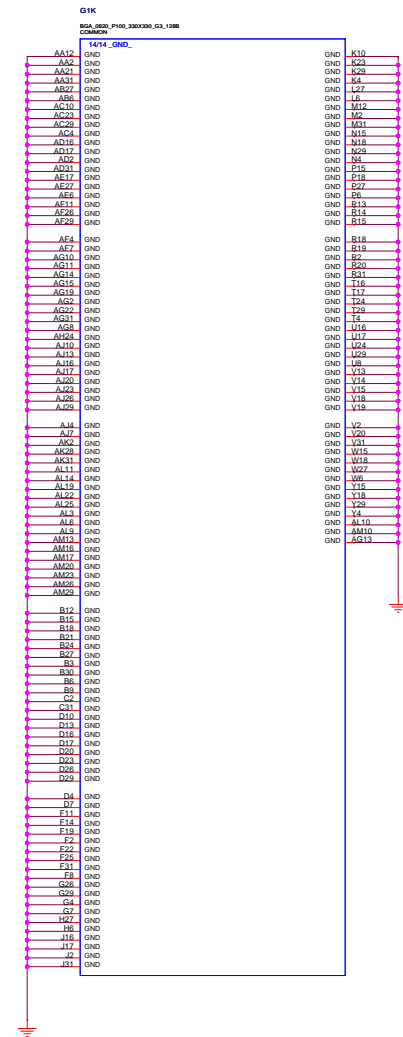


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## GPU GND CONNECTION, XTAL



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PAGE DETAIL	GPU GND CONNECTION, XTAL

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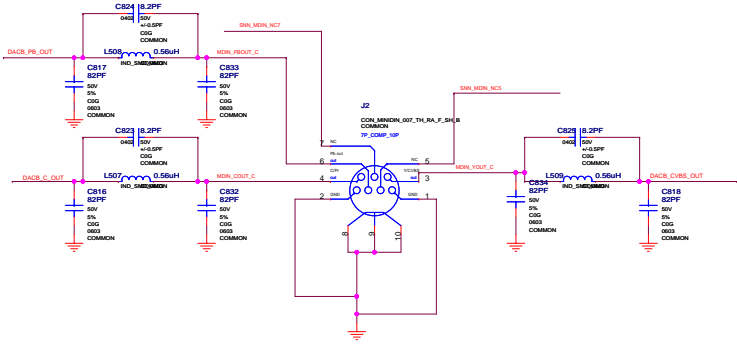
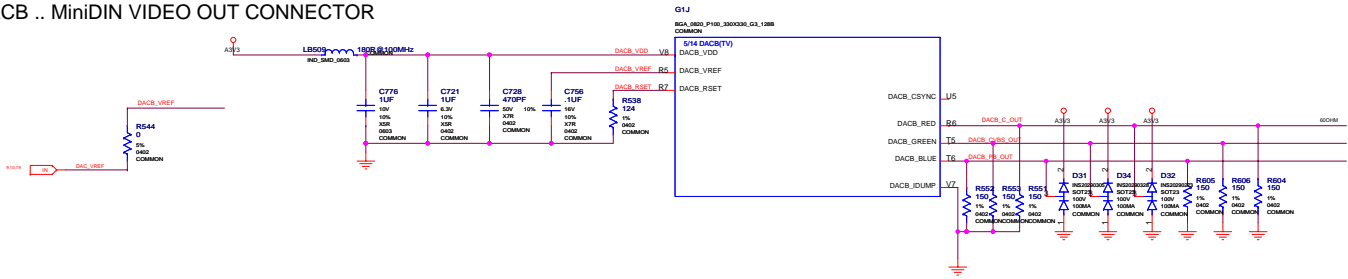


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DACB .. MiniDIN VIDEO OUT CONNECTOR



DACB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACB_C_OUT	1	50OHM	
DACB_CVBS_OUT	1	50OHM	
DACB_PBS_OUT	1	50OHM	
DACB_PBS_OUT	1	50OHM	
DACB_PBS_OUT	1	50OHM	

MON_SDL_C	2	50OHM	
MON_MON_C	2	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACB_VDD	3.3000V	0.07A	16.0
DACB_VREF			16.0
DACB_RSET			16.0

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ASSEMBLY	BASIC LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STOP/ ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTER, SYNC STRIPPER, MINIDIN CONNECTOR NORTH/HDV HEADER

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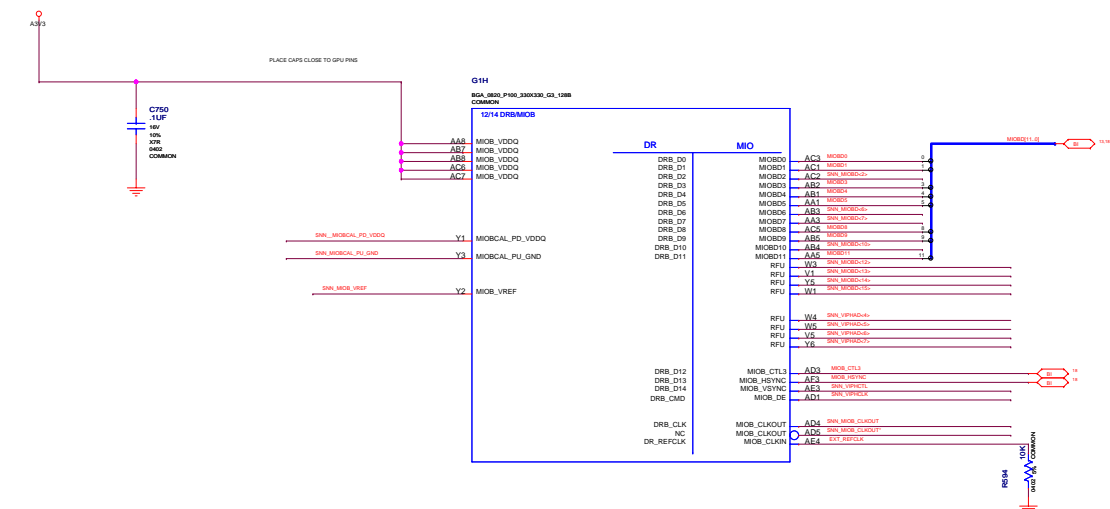
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G3 VIP/MIOB



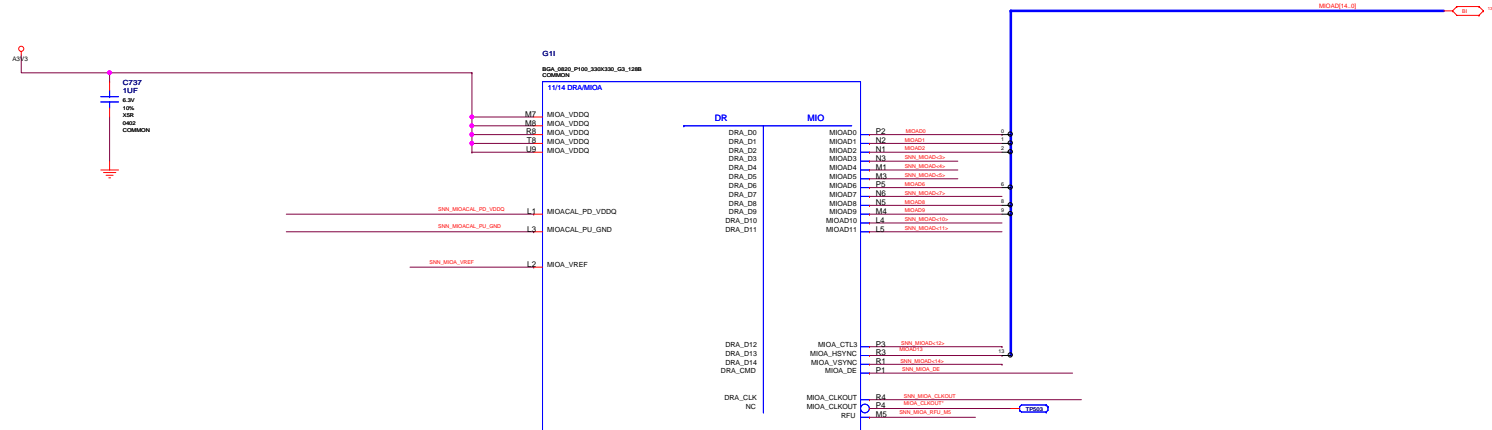
MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
MIOBCTL3	2	50OHM	
EXT_REFCLK	2	50OHM	
MIOB_CLKOUT	2	50OHM	
MIOBCTL3	2	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOB_VREF	1.25000V		12.0
MIOBCTL3_VDDQ	1.25000V		12.0
MIOBCTL3_VDDQ	1.25000V		12.0

G3 MIOA



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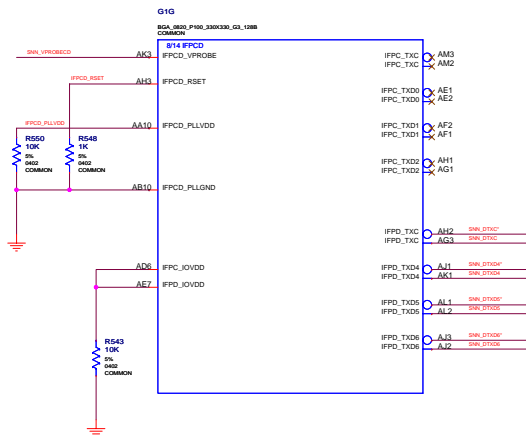
## INTERNAL TMDS .. LINK C

## IFPAB NET RULES




## NET RULES

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
(N)	IFPCD_PLLVDD	3.300000	0.04	16.0
(N)	IFPD_IOVDD	0.000000	0	10.0
(N)	IFPC_IOVDD	3.300000	0.15	16.0



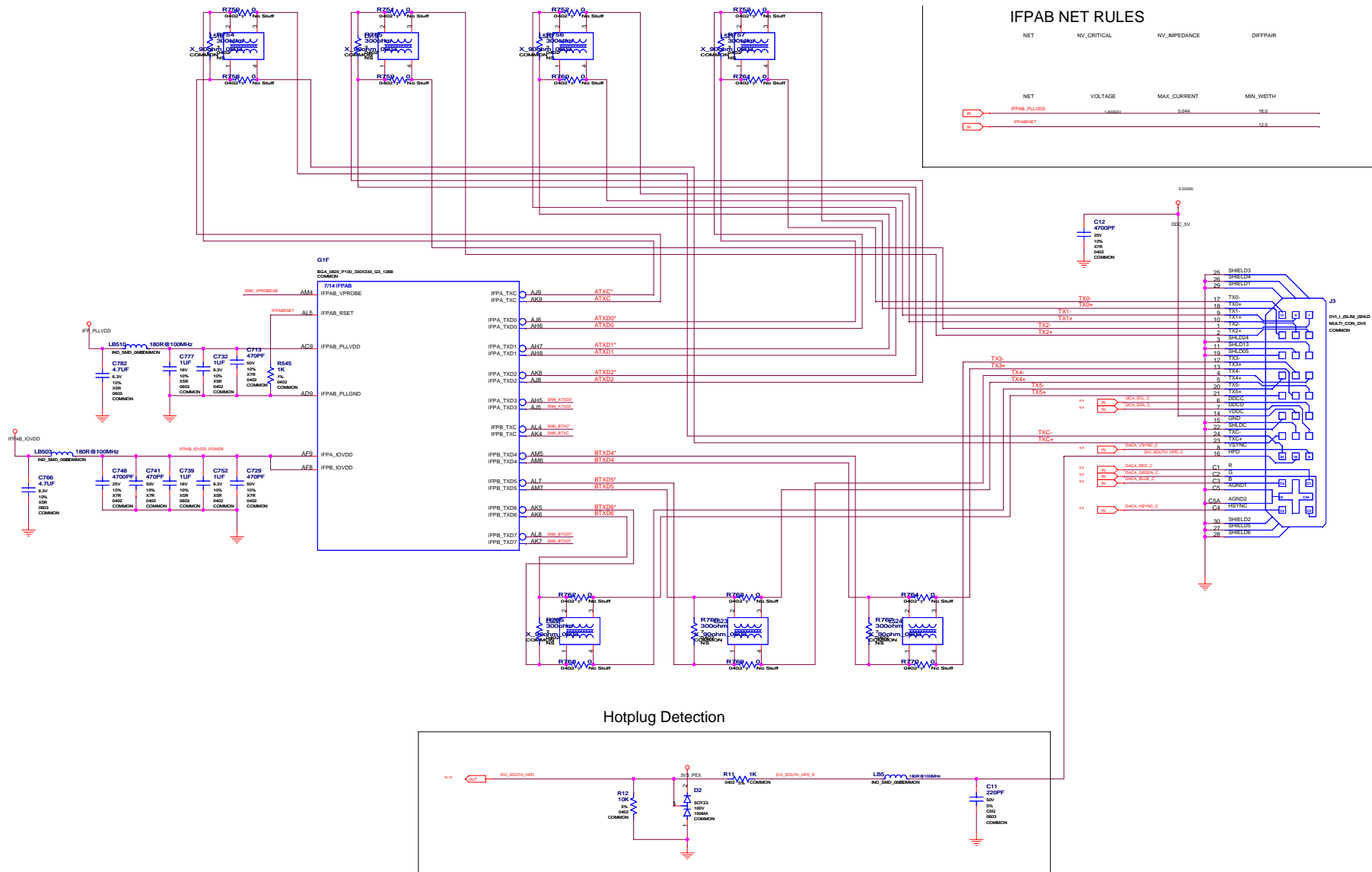
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMD5 LINK C

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## INTERNAL TMDS .. LINK A &amp; B



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PAGE DETAIL	TMD5 LINK A & PU's, DVI CONNECTOR SOUTH

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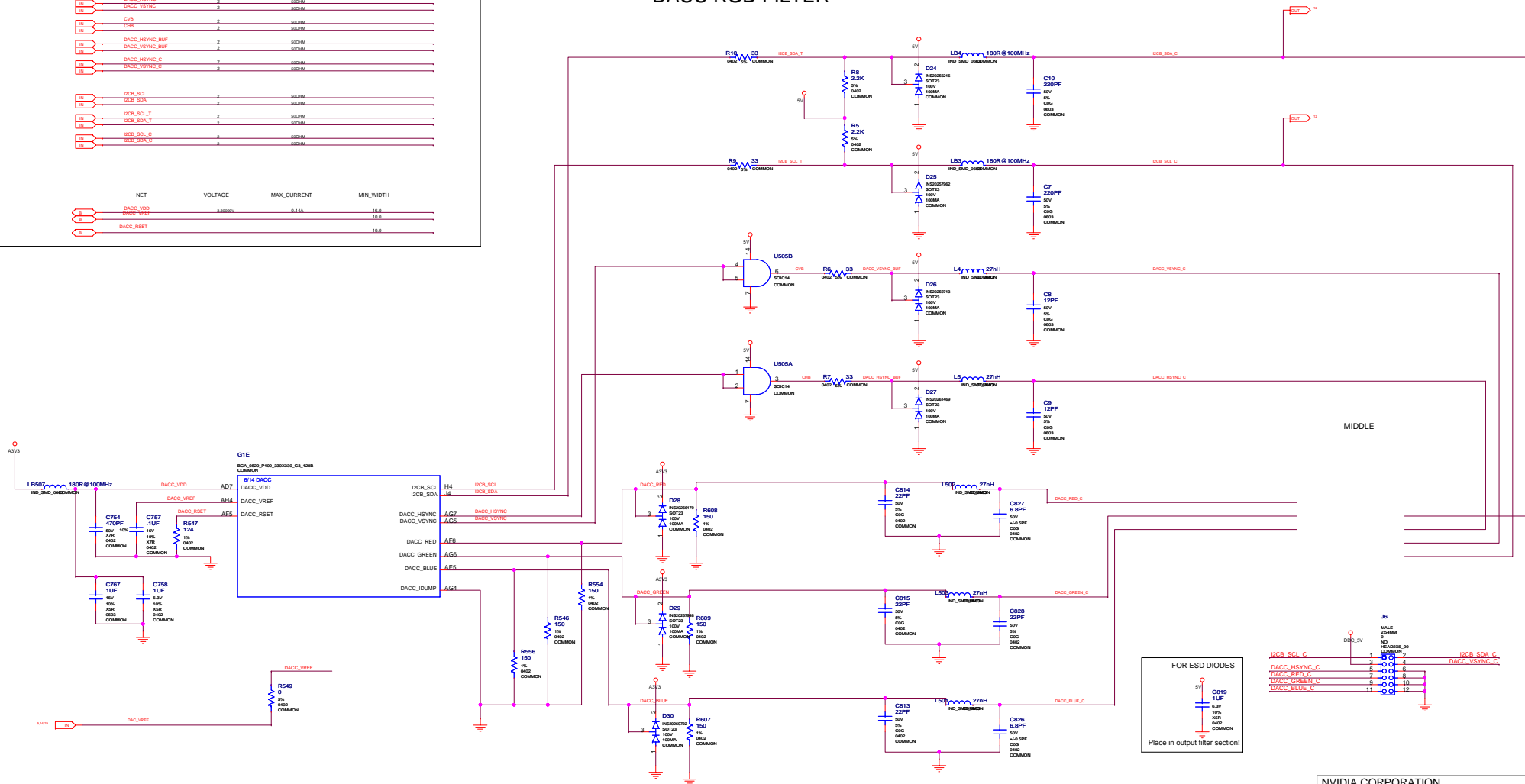
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NAME	DATE 12-JAN-2007

# DACC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACC_RED	1	50OHM	
DACC_GREEN	1	50OHM	
DACC_BLUE	1	50OHM	
DACC_RED_C	1	50OHM	
DACC_GREEN_C	1	50OHM	
DACC_BLUE_C	1	50OHM	
DACC_HSYNC	2	50OHM	
DACC_VSYNC	2	50OHM	
CVB	2	50OHM	
CVB	2	50OHM	
DACC_HSYNC_BUF	2	50OHM	
DACC_VSYNC_BUF	2	50OHM	
DACC_HSYNC_C	2	50OHM	
DACC_VSYNC_C	2	50OHM	
DCB_SCL	2	50OHM	
DCB_SDA	2	50OHM	
DCB_SCL_T	2	50OHM	
DCB_SDA_T	2	50OHM	
DCB_SCL_C	2	50OHM	
DCB_SDA_C	2	50OHM	
DACC_VDD	330000	0.14A	18.0
DACC_RESET			18.0

## Secondary Display (DACC), DB15

### DACC RGB-FILTER



ASSEMBLY

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PAGE DETAIL

DACC FILTERS, DACC SYNC BUFFERS & DB15 MID

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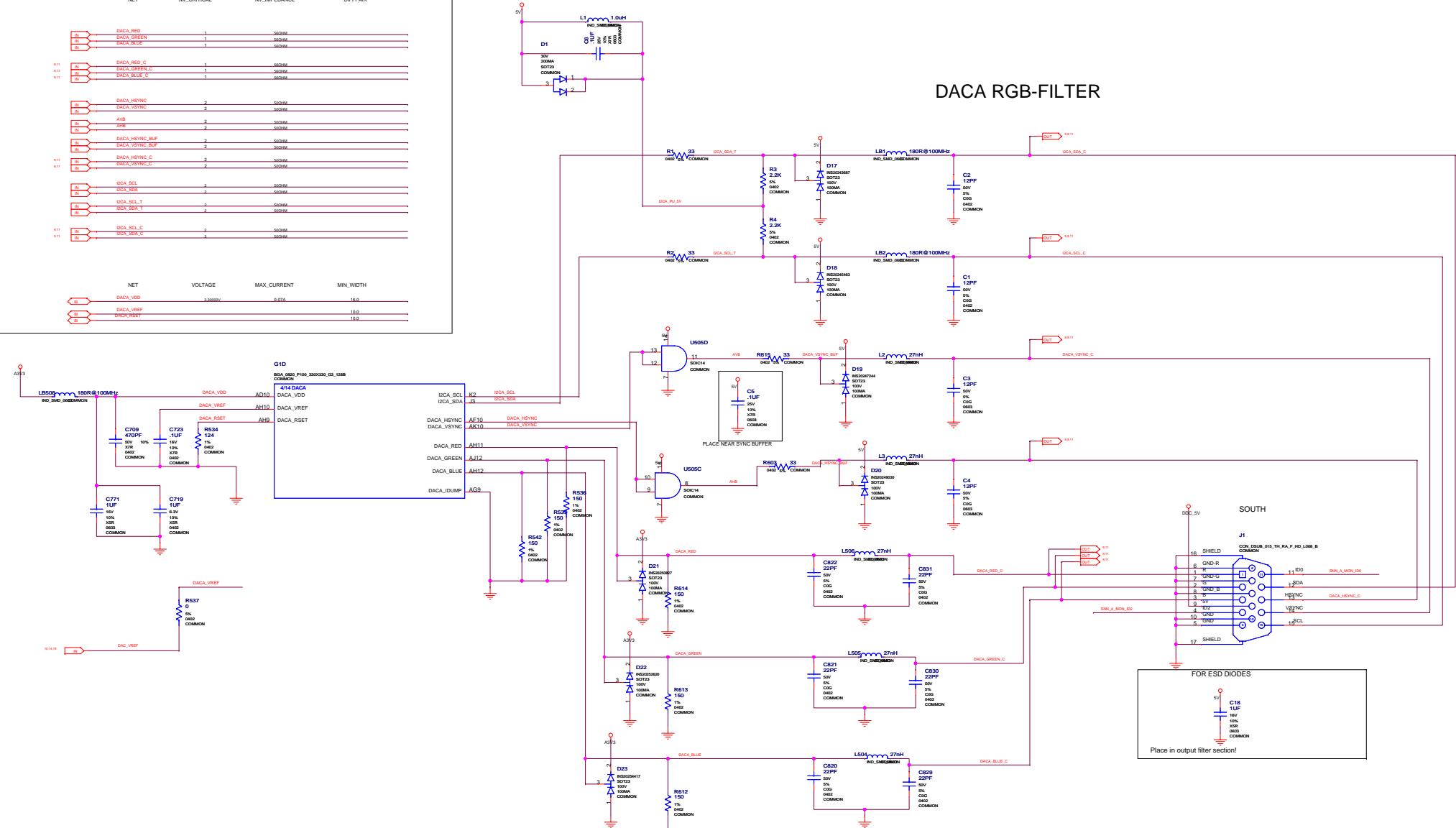
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# DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACA_RED	1	50OHM	
DACA_GREEN	1	50OHM	
DACA_BLUE	1	50OHM	
DACA_RED_C	1	50OHM	
DACA_GREEN_C	1	50OHM	
DACA_BLUE_C	1	50OHM	
DACA_HSYNC	2	50OHM	
DACA_VSYNC	2	50OHM	
AUX	2	50OHM	
DACA_HSYNC_BUF	2	50OHM	
DACA_VSYNC_BUF	2	50OHM	
DACA_SCL	2	50OHM	
DACA_SDA	2	50OHM	
DACA_SCL_T	2	50OHM	
DACA_SDA_T	2	50OHM	
DACA_SCL_C	2	50OHM	
DACA_SDA_C	2	50OHM	
DACA_VDD	3.3000V	0.07A	18.0
DACA_VREF			10.0
DACA_RESET			10.0

## Primary Display (DACA), Slim DB15

## DACA RGB-FILTER



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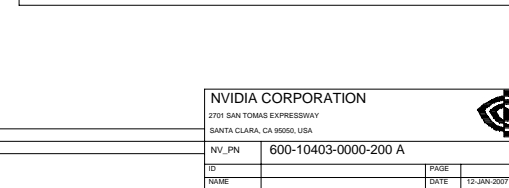
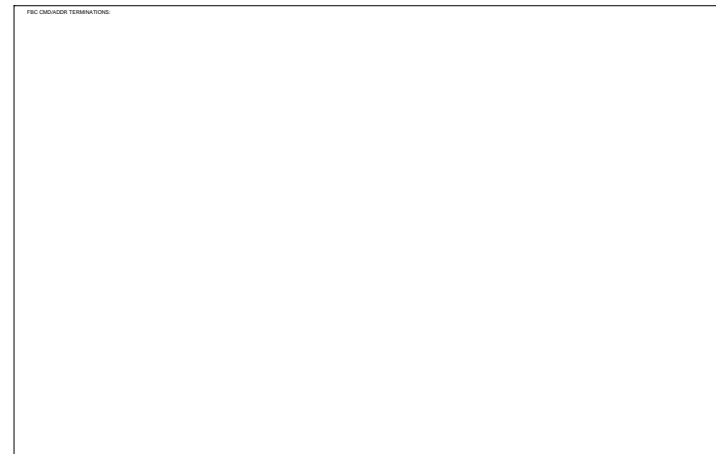
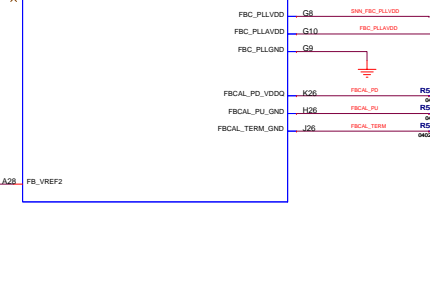
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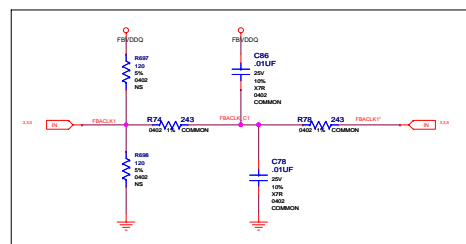
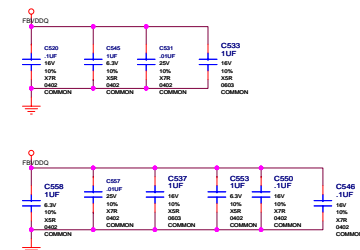
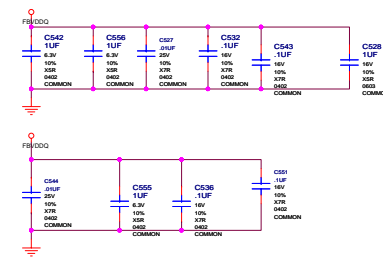



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PAGE DETAIL: DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH



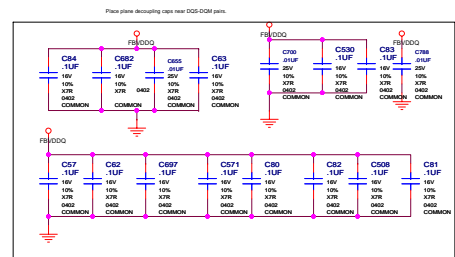
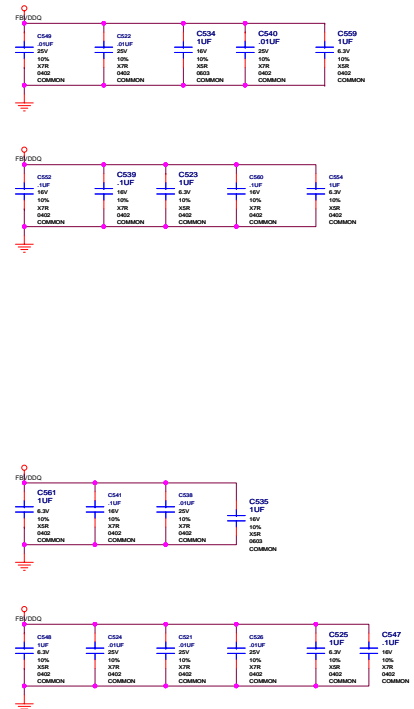
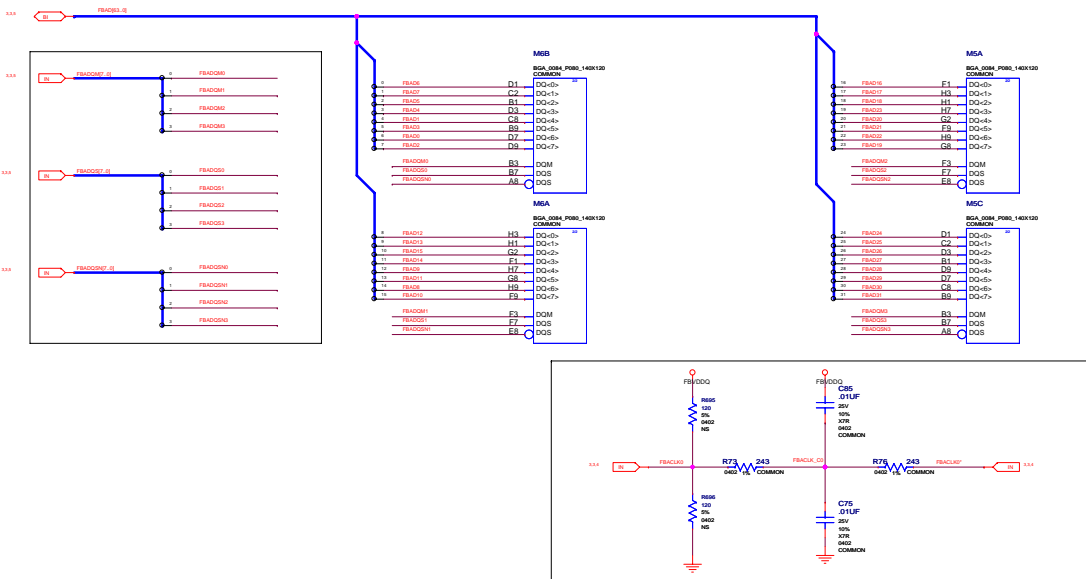
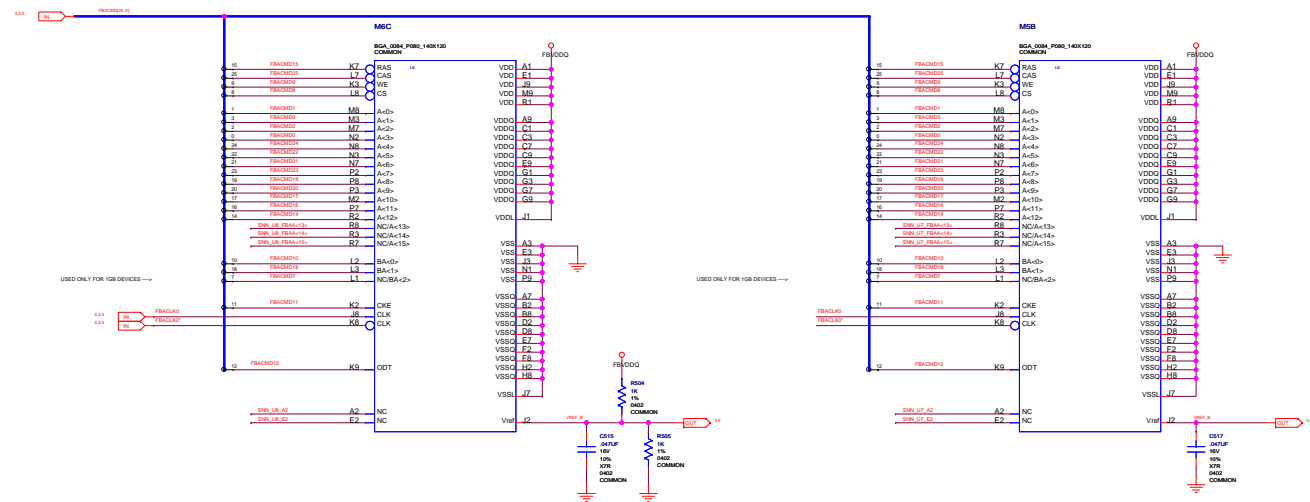
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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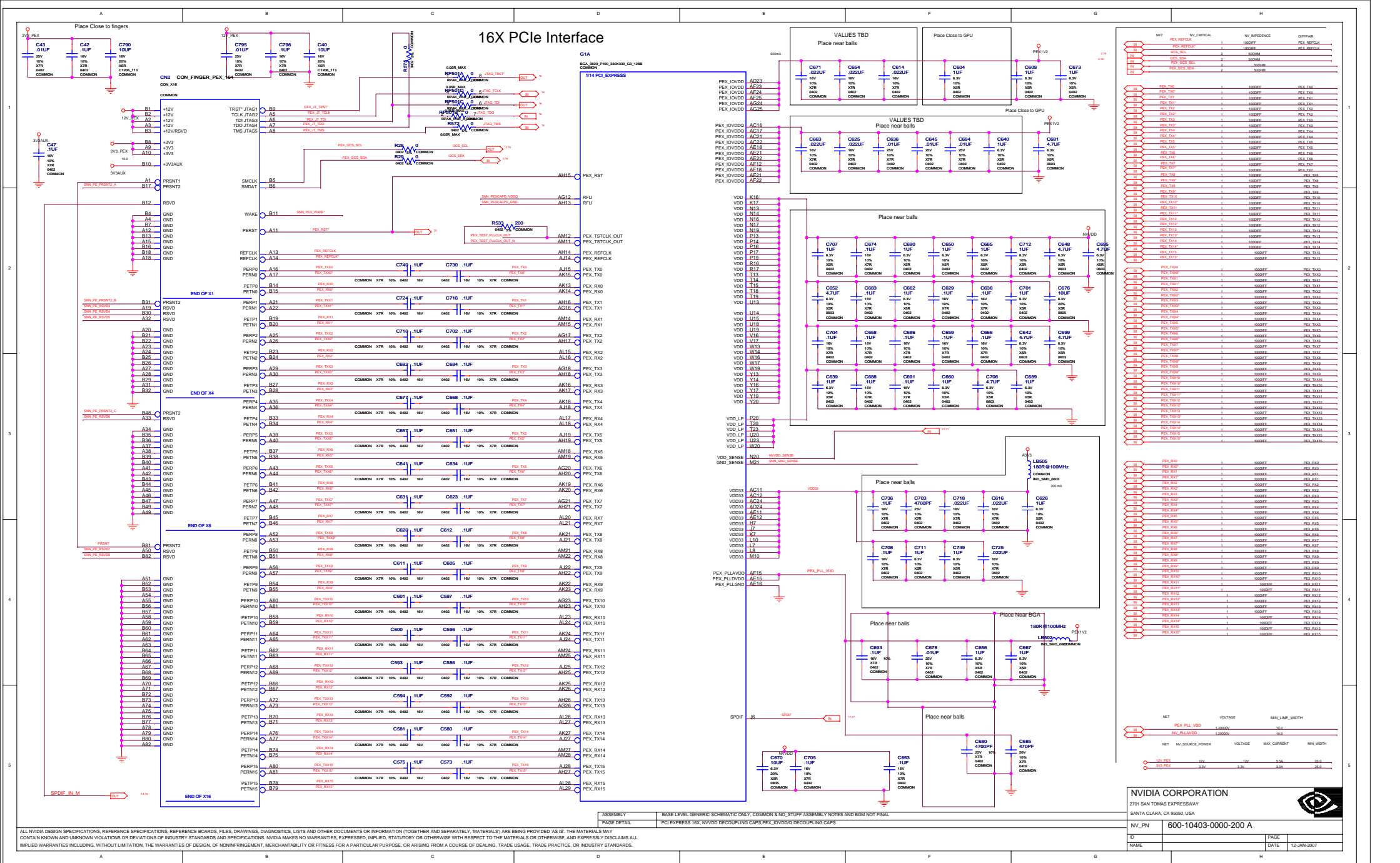


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16Mx16 DDR2 MEMORIES, BANK 0..31







P403-B00 DESIGN -- G84-200, 256 MB DDR2,DVI-I, VGA, HDTV

PAGE SUMMARY:

Page 1: TABLE OF CONTENTS & REVISION HISTORY  
Page 2: PCI EXPRESS 16X, NVVDD DECOUPLING CAPS,PEX\_IOVDD/Q DECOUPLING CAPS  
Page 3: FBA MEMORY INTERFACE, GPU FBVDD/Q DECOUPLING CAPS, FBVTT TERMINATION  
Page 4: FBA 16Mx16 DDR2 MEMORIES, BANK 0..31  
Page 5: FBA 16Mx16 DDR2 MEMORIES, 1ST BANK 32..63  
Page 6: FBC MEMORY INTERFACE, GPU FBVTT, FBVDDQ  
Page 7: FBC 16MX16 DDR2 MEMORIES, 2ND BANK 0..31  
Page 8: FBC 16Mx16 DDR2 MEMORIES, 2ND BANK 32..63  
Page 9: DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH  
Page 10: DACC FILTERS, DACC SYNC BUFFERS & DB15 MID  
Page 11: TMDS LINK A & PU's, DVI CONNECTOR SOUTH  
Page 12: TMDS LINK C  
Page 13: MIOA & MIOB  
Page 14: DACB FILTERS, SYNC STRIPPER, MINIDIN CONNECTOR NORTH,HDTV HEADER  
Page 15: GPU GND CONNECTION, XTAL  
Page 16: JTAG, BIOS ROM, HDCP ROM, FAN CONTROL, GPIO  
Page 17: SPDIF  
Page 18: BIOS STRAPS & MECHANICALS  
Page 19: POWER SUPPLY: TMDS IOVDD,SV,ASV3  
Page 20: thermal protection and dynamic NVVDD  
Page 21: PowerSupplyII: NVVDD  
Page 22: PowerSupplyIII: FBVDDQ, PLLVDD

REV HISTORY

96/10/30 Design change to G84-G53 Large size 8400GS circuit PCB LP costdown version

- 1. Remove FBC 2ND 0..63
- 2. Remove TMDS C HDMI circuit
- 3. Remove SCART function form DACB
- 4. Change Fancontrol func to Direct driver
- 5. Change FBVDDQ PWM power solution to 431 LDO solution

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10403-0000-200	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0020	600-10403-0020-200	P403-B00 G84-300 459/400MHz 256MB 16Mx16 BGA84 GDDR2 DVI-I-DL+VGA+HDTV-Out
2	SKU0021	600-10403-0021-200	P403-B00 G84-200 459/400MHz 256MB 16Mx16 BGA84 GDDR2 DVI-I-DL+VGA+HDTV-Out
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