

V141-0A

P729: G96, DDR2 MEMORY 32MX16/16MX16

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- Page 19: Power Supply II: FBVDDQ
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REV HISTORY

- Modify Power Sequencing  
02/25  
PAGE 14.EDIT NET  
R562 : I2CD\_SCL\_R to I2CC\_SCL\_R  
R563 : I2CD\_SDA\_R to I2CC\_SDA\_R  
R172,R173 Pull high 5V
- PAGE 19.EDIT footprint  
C87 footprint 0805 to 1206
- PAGE 11.Remove R130  
HDMI gate pull down  
02/26  
PAGE 2.Change 3V3\_PEX to 3V3\_AUX

REV	VARIANT	WVFN	ASSEMBLY
B	BASE	600-10729-xxxx-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10729-0000-000	G96-300-A1, 550500MHz, 512MB 32mx16 DDR2 BGAB4 DVI-DL+VGA+HDTV
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P729 Overview

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```
change to 3V3_AUX
```

OB3-ONB(MC)

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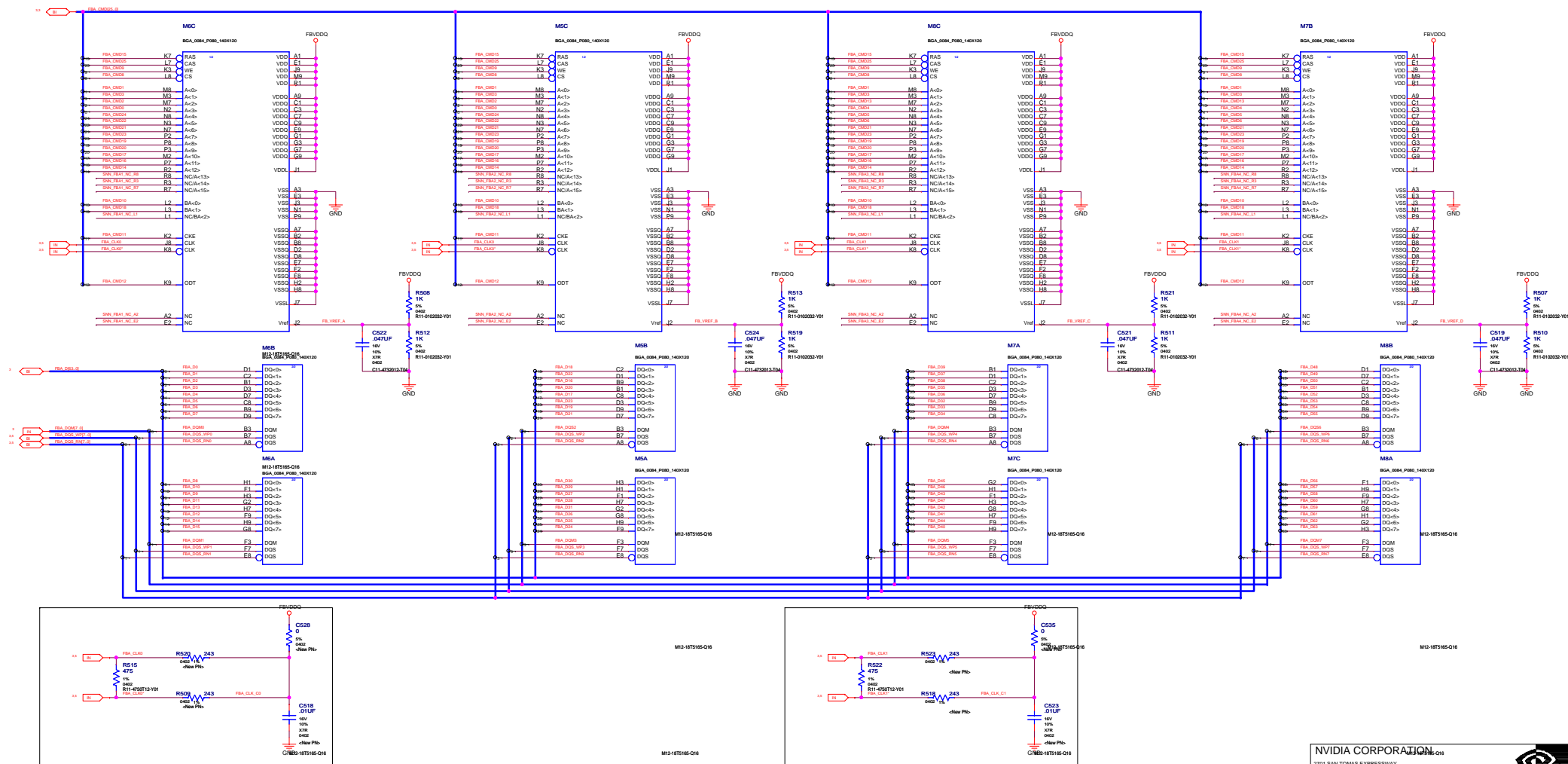
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## Partition A Memories



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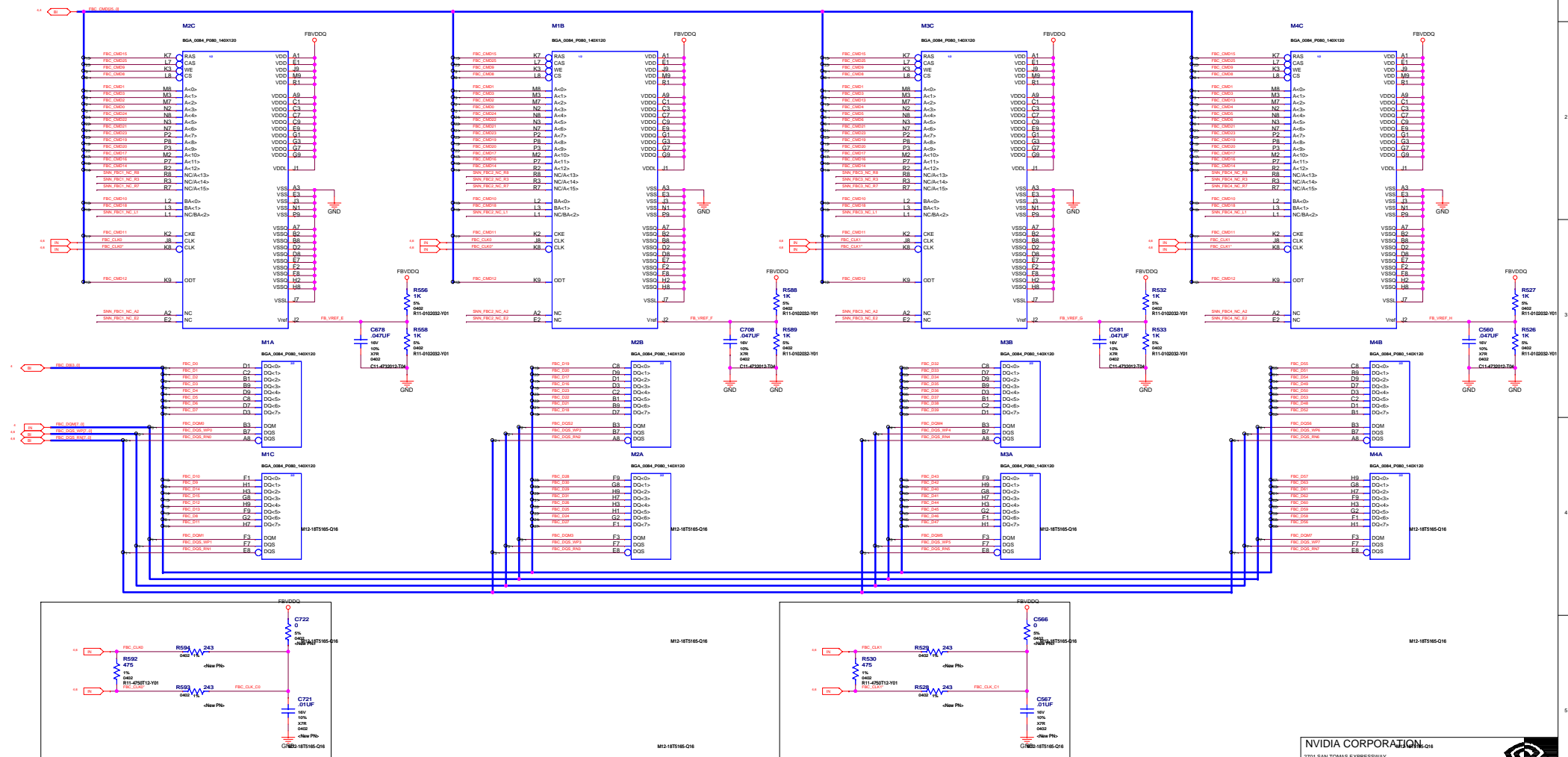
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PAGE DETAIL	Partition & Memories

## Partition C Memories



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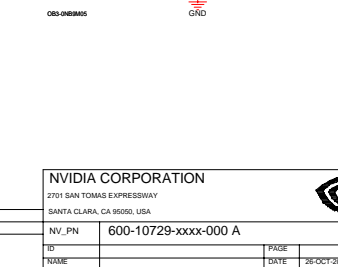
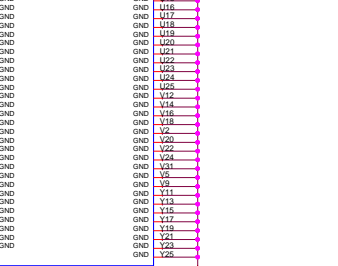
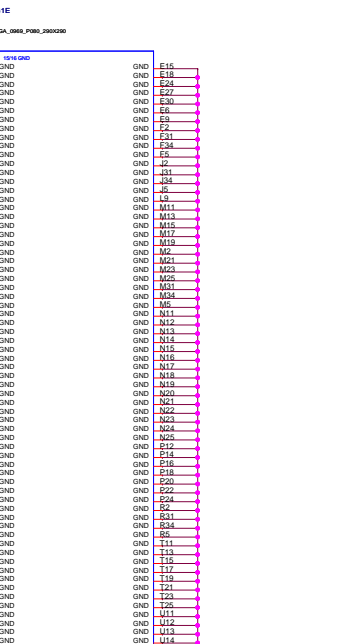
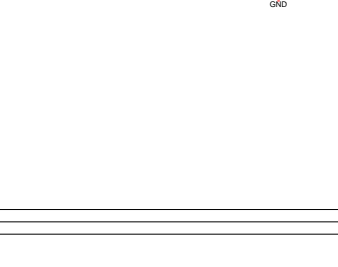
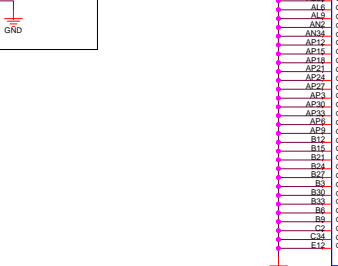
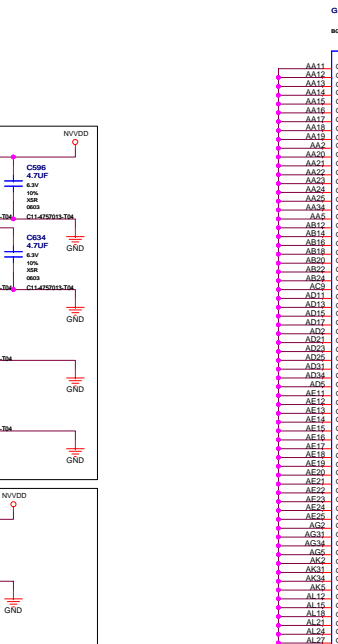
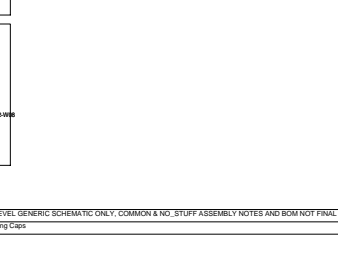
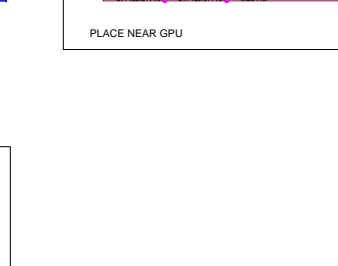
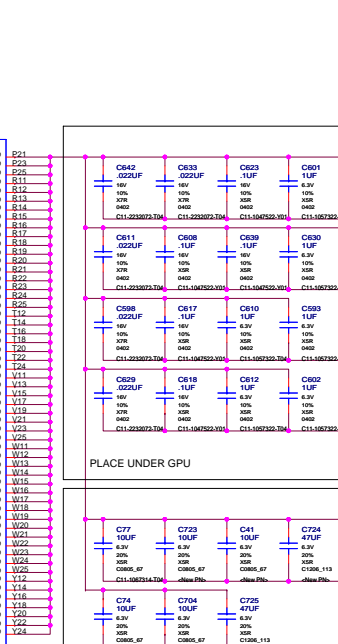
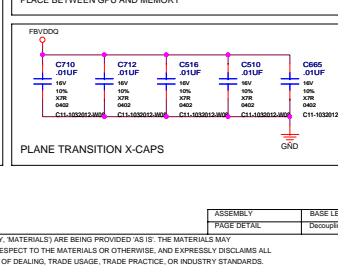
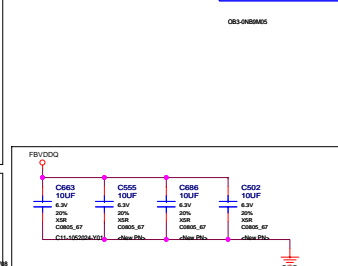
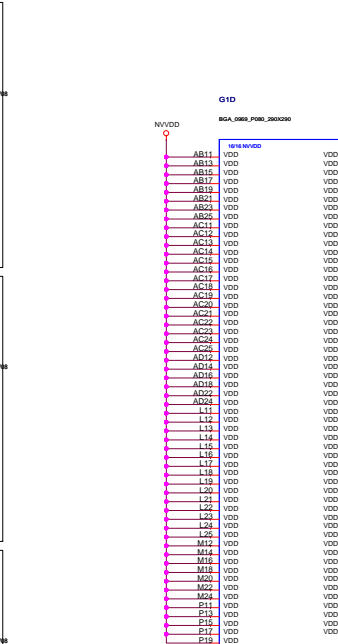
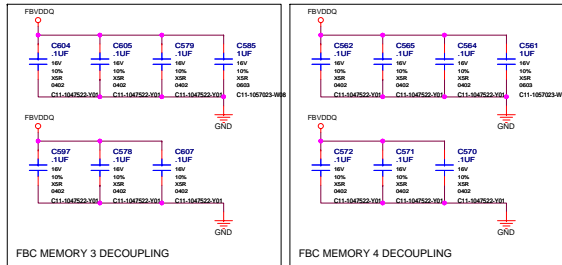
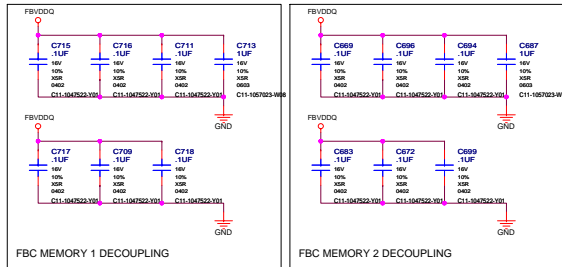
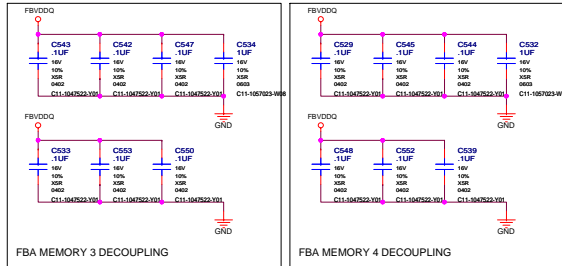
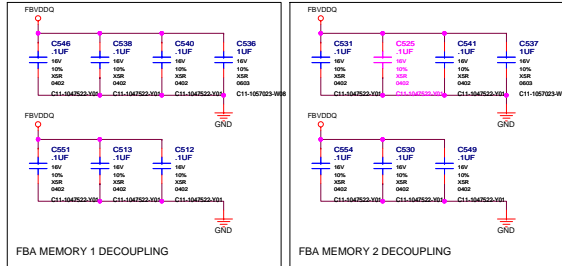
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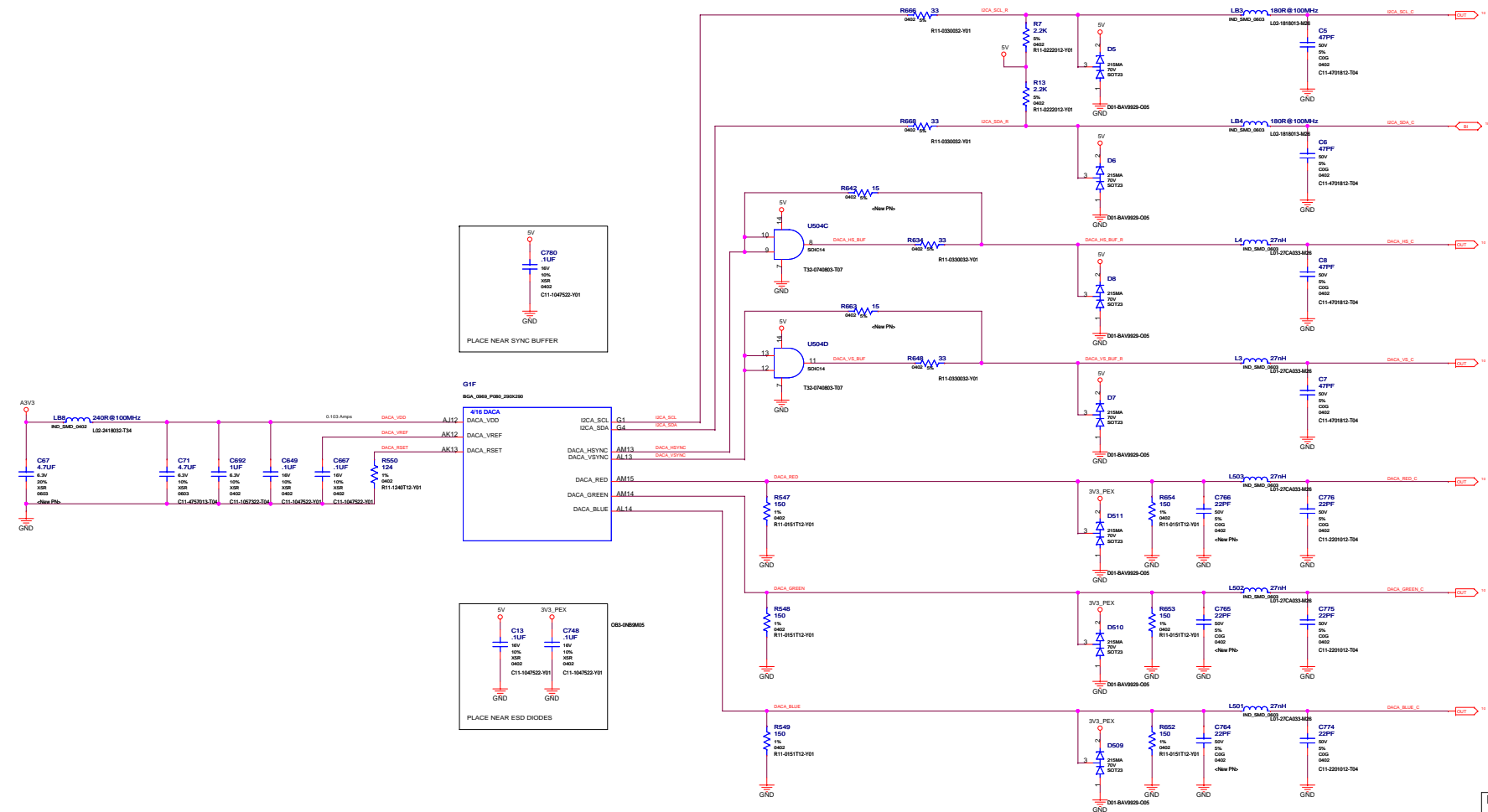
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Partition C Memories


# Decoupling Caps



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## DACA

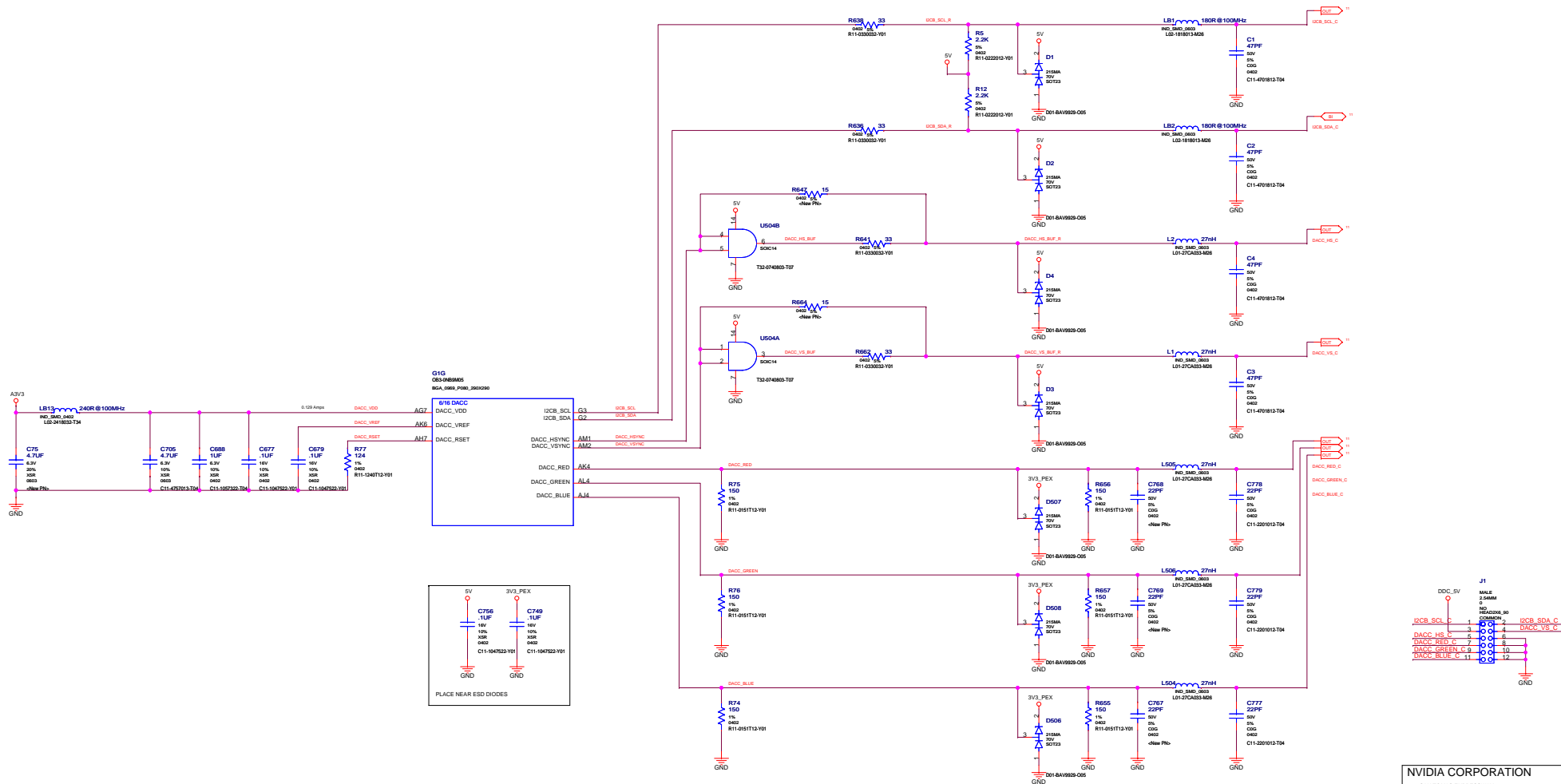



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA



## DACC, Slim DB15 Connector



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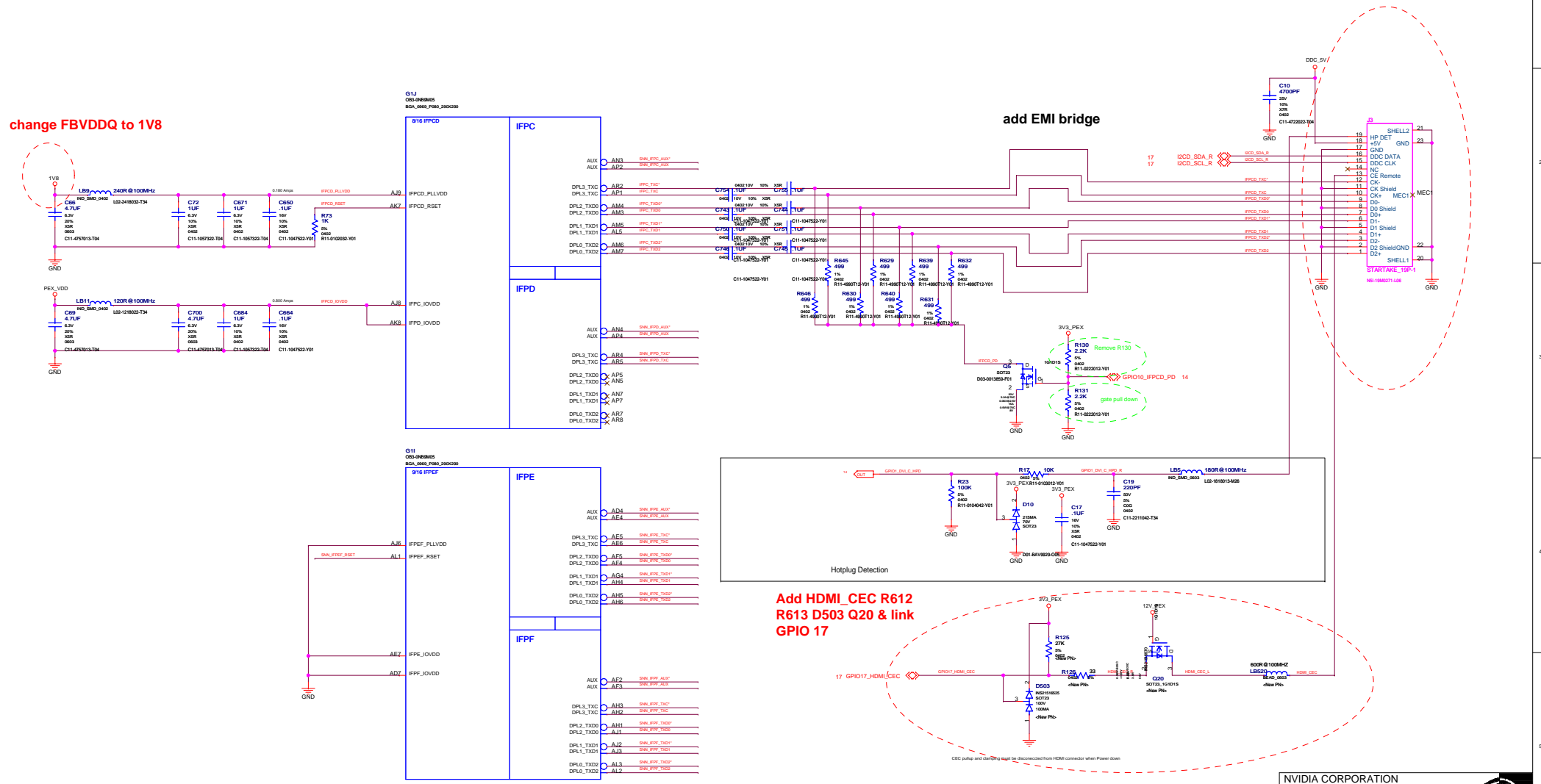
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### Internal TMDS .. Link C & D

**change FBVDDQ to 1V8**

## Change DVI to HDMI



**Add HDMI\_CEC R612  
R613 D503 Q20 & link  
GPIO 17**

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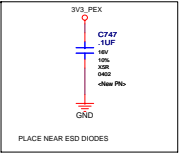
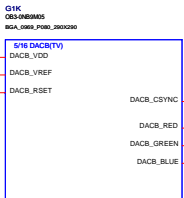
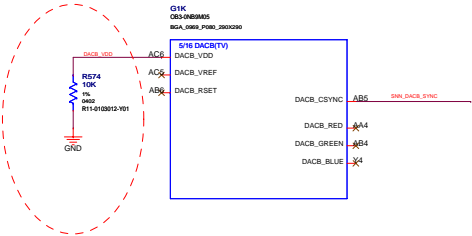


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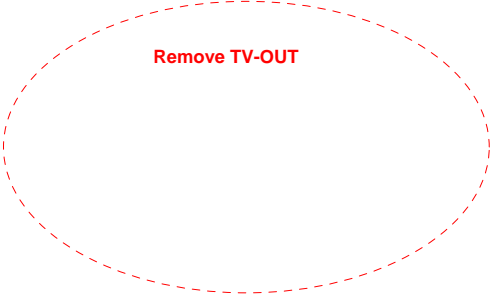
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PAGE DETAIL	Internal TMD5 .. Link C & D

DACB, MINIDIN Connector

Change R574 to 10K



Remove TV-OUT

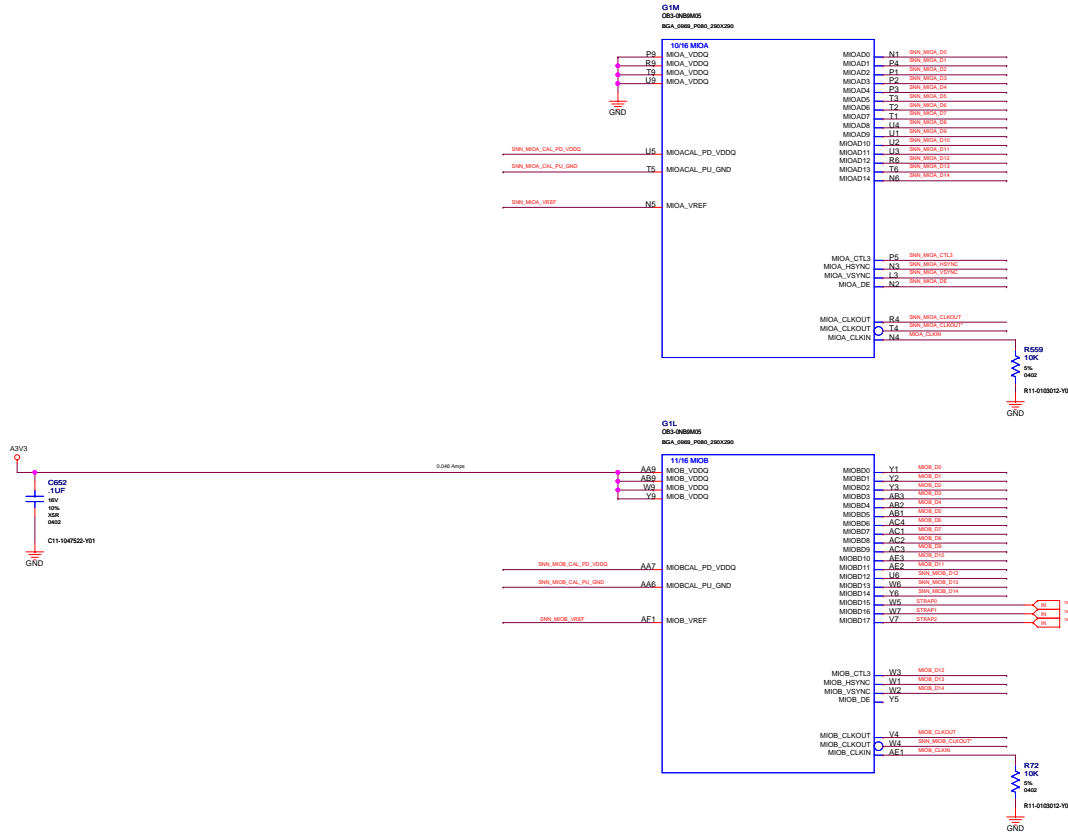


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ASSEMBLY	BASIC LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB, MINIDIN Connector


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MIOA, MIOB Interface

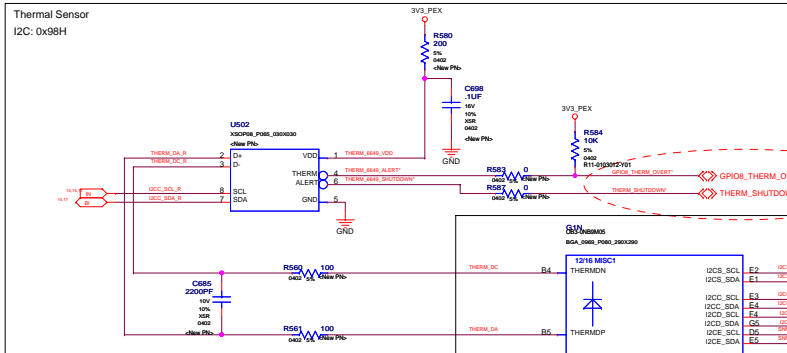


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PAGE DETAIL	MIOA, MIOB Interface

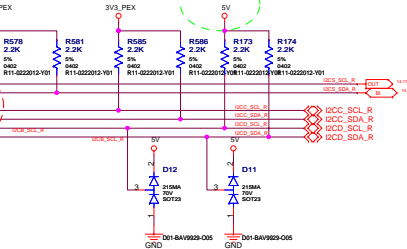
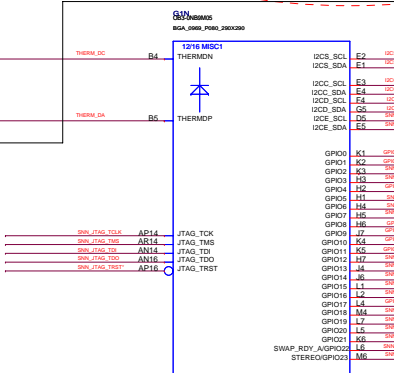
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# Thermal Sensors, GPIOs, XTAL, JTAG, Fan

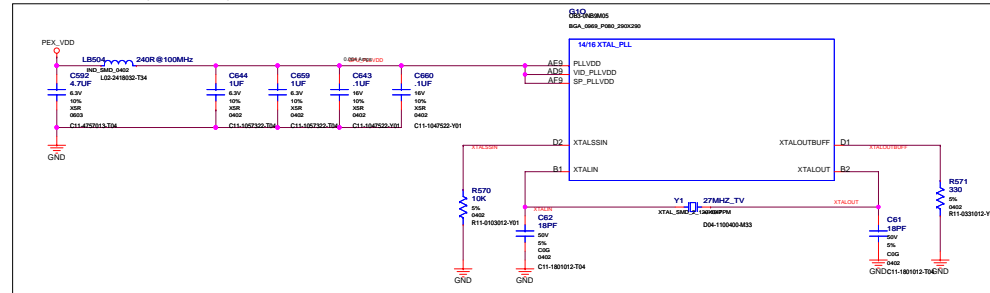


Add R171 R172 R173 R174  
I2CD\_SCL & I2CD\_SDA

change Thermal protection

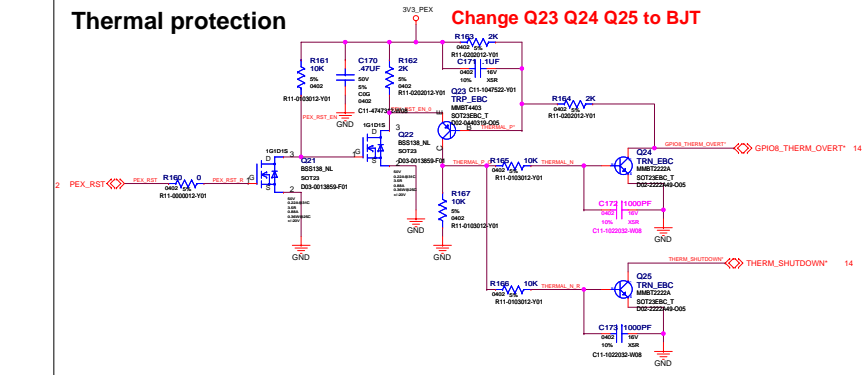


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14  
11

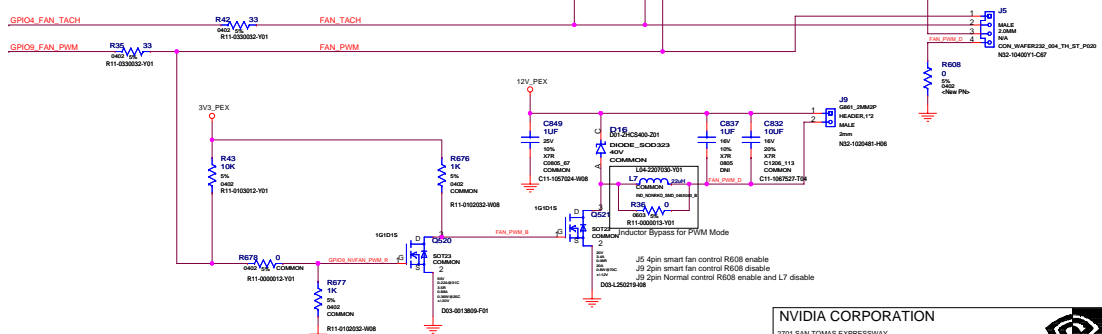


## Thermal protection

Change Q23 Q24 Q25 to BJT



2-pin/4-pin Fan Control



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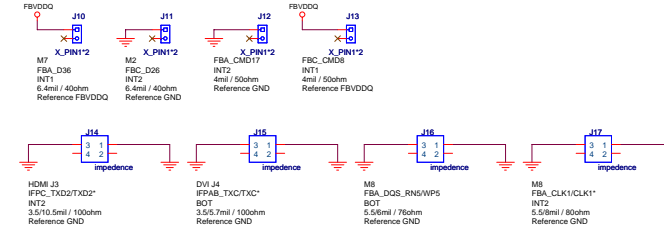
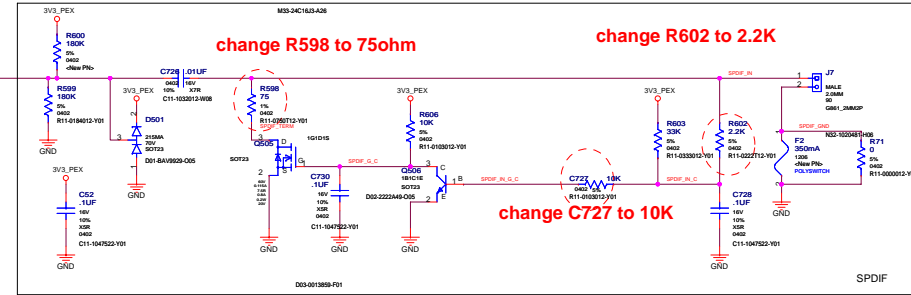
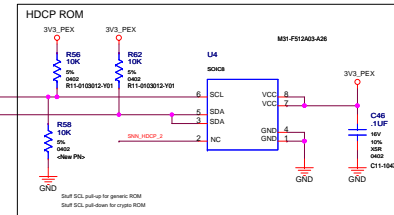
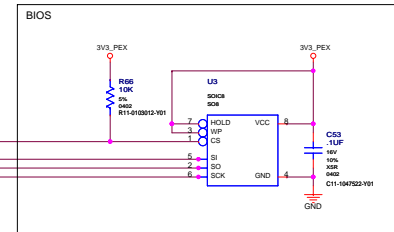
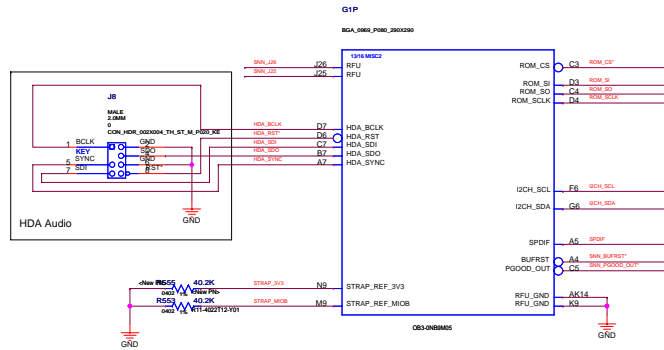



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ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO\_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: Thermal Sensors, GPIOs, XTAL, JTAG, Fan

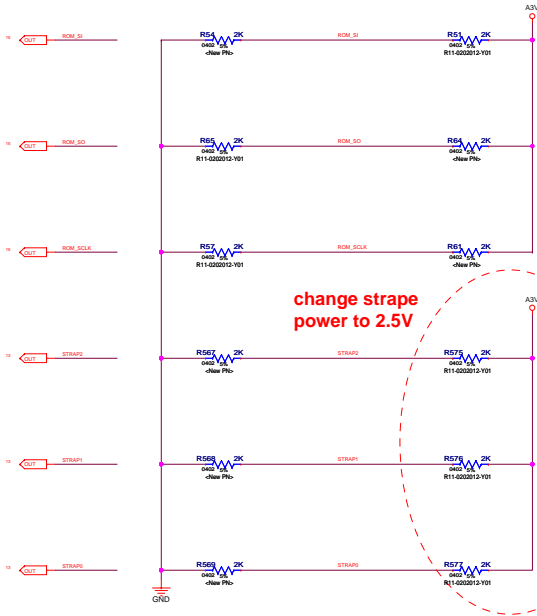
## BIOS, HDCP, SPDIF, HDA, Mechanical



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Straps



G94 Straps  
Multilevel Mode

Bit Signal

Values

03	ACLK_277	0 DISABLE 1 ENABLE
02	TVMODE[2]	000 NTSC_A 001 NTSC_J 010 PAL_M 011 PAL_N 100 PAL_CN 101 PAL_CN2 110 RESERVE0 111 RESERVE1
01	TVMODE[1]	
00	TVMODE[0]	
03	PCL_DEV0_EXT	1 G96-300-A1
02	SUB_VENDOR	0 NO BIOS 1 BIOS
01	SLOT_CLK_CFG	0 DISABLE 1 ENABLE
00	PEX_PUL_EN_TERM100	0 DIS 1 EN

Multilevel  
Straps

5K to GND	0000
10K to GND	0001
15K to GND	0010
20K to GND	0011
25K to GND	0100
30K to GND	0101
35K to GND	0110
40K to GND	0111
45K to GND	1000
50K to GND	1001
55K to GND	1010
60K to GND	1011
65K to GND	1100
70K to GND	1101
75K to GND	1110
80K to GND	1111

03	RAMCFG[2]	0000 32Mx16/16Mx16 DDR2 128-bit Hynix 0001 16Mx16 DDR2 128-bit Samsung, Micron 0010 16Mx16 DDR2 128-bit Corsair 0011 16Mx16 DDR2 128-bit Hynix 0100 32Mx16/16Mx16 DDR2 128-bit Hynix 0101 32Mx16/16Mx16 DDR2 128-bit Samsung 0110 32Mx16/16Mx16 DDR2 128-bit Corsair 0111 32Mx16/16Mx16 DDR2 128-bit Hynix
02	RAMCFG[1]	
01	RAMCFG[0]	
00	RAMCFG[3]	

0111 32Mx16 DDR2 128-bit Hynix

03	PCL_DEV0[3]	0001 G96-300-A1
02	PCL_DEV0[2]	
01	PCL_DEV0[1]	
00	PCL_DEV0[0]	
03	SGIO_PACCFG_LUT_ADDR[2]	0000 G96TOP_DEFAULT 0001 MOBILE_JITTERS 0010 MOBILE_JITTERS_LLAMP 0011 MOBILE_JITTERS_LLAMP 0100 MOBILE_JITTERS_LLAMP 0101 MOBILE_JITTERS_LLAMP 0110 MOBILE_JITTERS_LLAMP 0111 MOBILE_JITTERS_LLAMP
02	SGIO_PACCFG_LUT_ADDR[1]	
01	SGIO_PACCFG_LUT_ADDR[0]	
00	SGIO_PACCFG_LUT_ADDR[3]	

03	USER[3]	0000 DEFAULT
02	USER[2]	
01	USER[1]	
00	USER[0]	

G94 Straps  
Binary-Bringup Mode

Bit Signal

Values

SUB_VENDOR	0 NO BIOS 1 BIOS
SLOT_CLK_CFG	0 DISABLE 1 ENABLE
SGIO_PACCFG_LUT_ADDR[2]	0000 G96TOP_DEFAULT 0001 MOBILE_JITTERS 0010 MOBILE_JITTERS_LLAMP 0011 MOBILE_JITTERS_LLAMP 0100 MOBILE_JITTERS_LLAMP 0101 MOBILE_JITTERS_LLAMP 0110 MOBILE_JITTERS_LLAMP 0111 MOBILE_JITTERS_LLAMP
SGIO_PACCFG_LUT_ADDR[1]	
SGIO_PACCFG_LUT_ADDR[0]	
SGIO_PACCFG_LUT_ADDR[3]	

G94 Straps  
Binary-Production Mode

Bit Signal

Values

SLOT_CLK_CFG	0 DISABLE 1 ENABLE
PCL_DEV0_EXT	10 G96-300-A1
PCL_DEV0[3]	
RAMCFG[2]	000 32Mx16/16Mx16 DDR2 128-bit Hynix 0001 16Mx16 DDR2 128-bit Samsung, Micron 0010 16Mx16 DDR2 128-bit Corsair 0011 16Mx16 DDR2 128-bit Hynix 0100 32Mx16/16Mx16 DDR2 128-bit Hynix 0101 32Mx16/16Mx16 DDR2 128-bit Samsung 0110 32Mx16/16Mx16 DDR2 128-bit Corsair 0111 32Mx16/16Mx16 DDR2 128-bit Hynix
RAMCFG[1]	
RAMCFG[0]	
RAMCFG[3]	

NVIDIA CORPORATION

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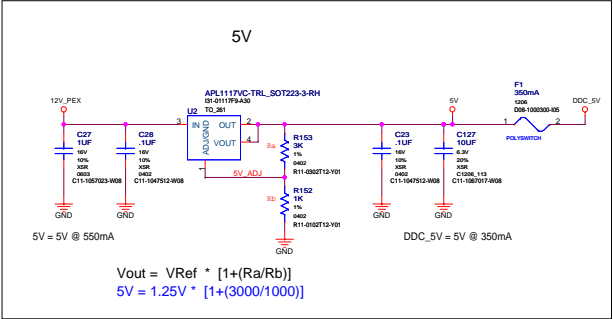
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DATE	25 OCT 2007

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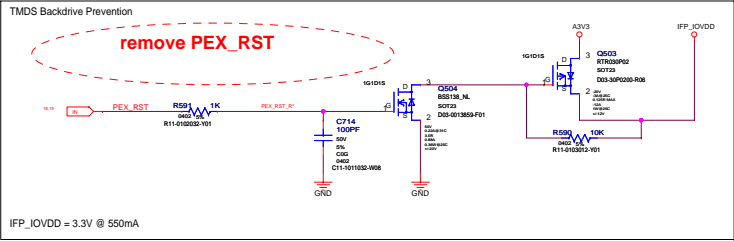


Power Supply I: 1V8, A3V3, 5V, IFP\_IOVDD

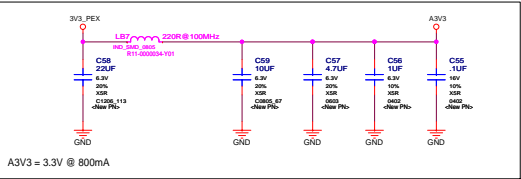
5V



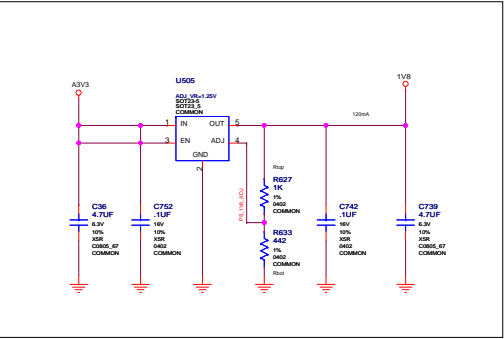
IFP\_IOVDD



A3V3



1V8



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The schematic shows a parallel combination of three branches connected to a common output node. The first branch contains a capacitor labeled C7 with value 0. The second branch contains a series combination of an inductor L7004 (value 1.2u) and a capacitor C8 (value 10n). The third branch contains a series combination of an inductor L7005 (value 1.2u) and a capacitor C9 (value 10n). A label "co-lay" is placed below the bottom right of the circuit.



3inch length from VRM to GPU

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

$$1.1V = 0.8V * (1 + (1.54k/4.02k)) \quad (ISL6549)$$

$$1.2V = 0.8V * (1 + (1.54k/3.09k)) \quad (ISL6549)$$

$$1.0V = 0.8V * (1 + (1.24k/4.87k)) \quad (ISL6549)$$

$$1.0526V = 0.8V * (1 + (1.5k/4.75k)) \quad (ISL6549)$$

5x 10uf 0805 X5R  
2x 47uf 1206 X5R  
3x 470uf ALE/OSCON

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply II: FBVDDQ

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NAME	DATE
NAME	26/01/2007