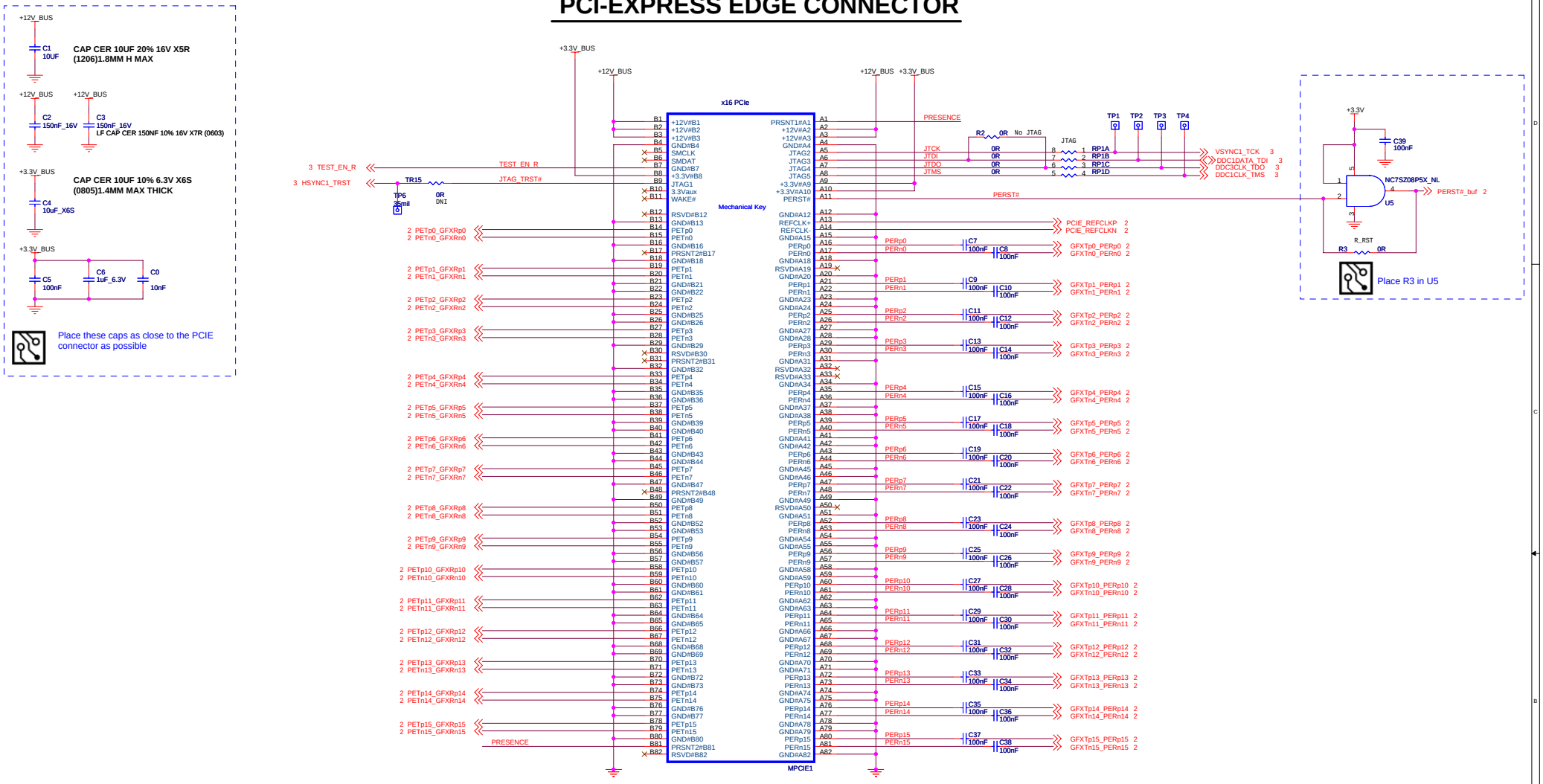
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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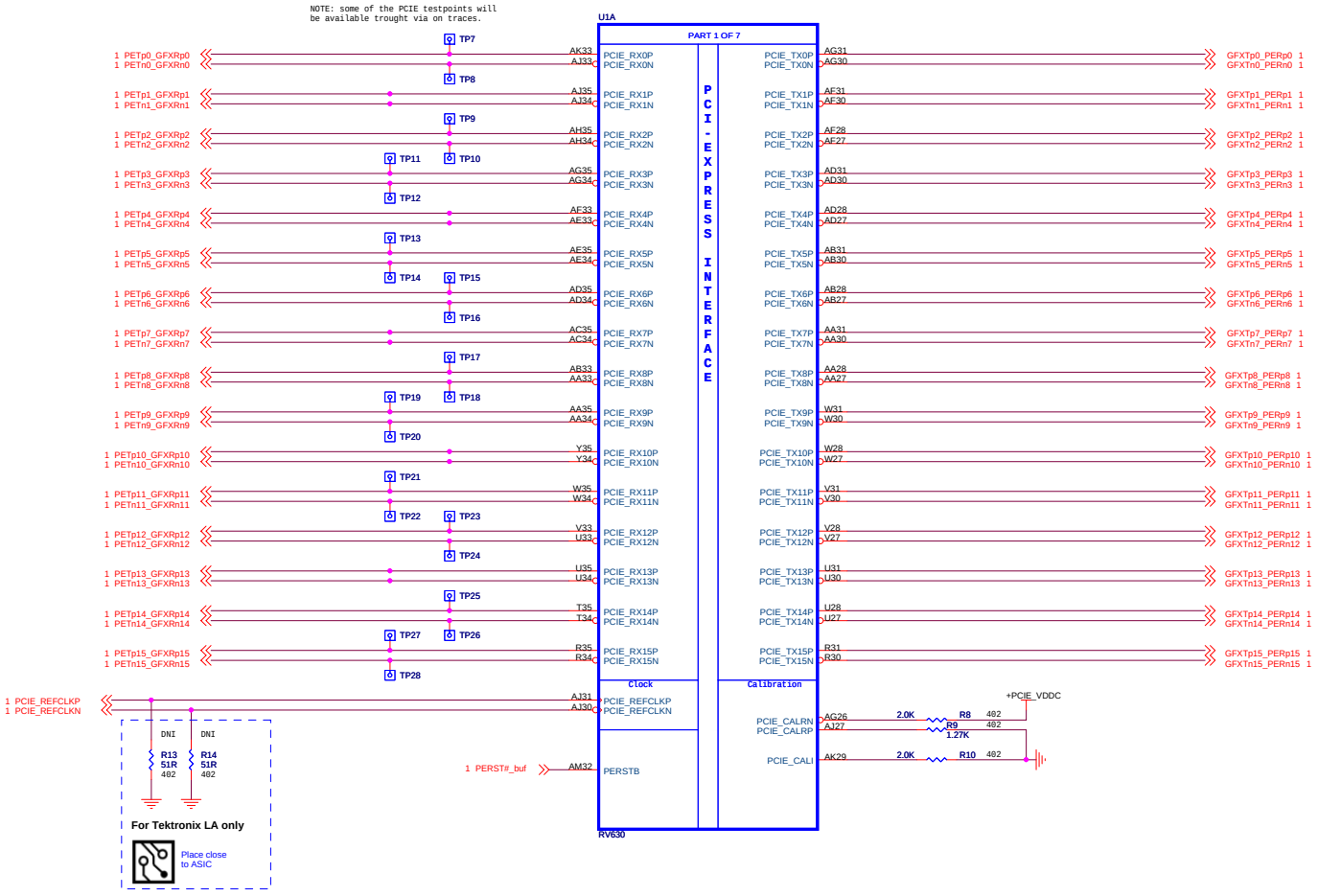
Title	RV630 GDDR3 - PCI-E Edge Connector		
Size C	Document Number 105-B148xx-00A		Rev A
Date: Friday, March 09, 2007		Sheet 1 of 21	



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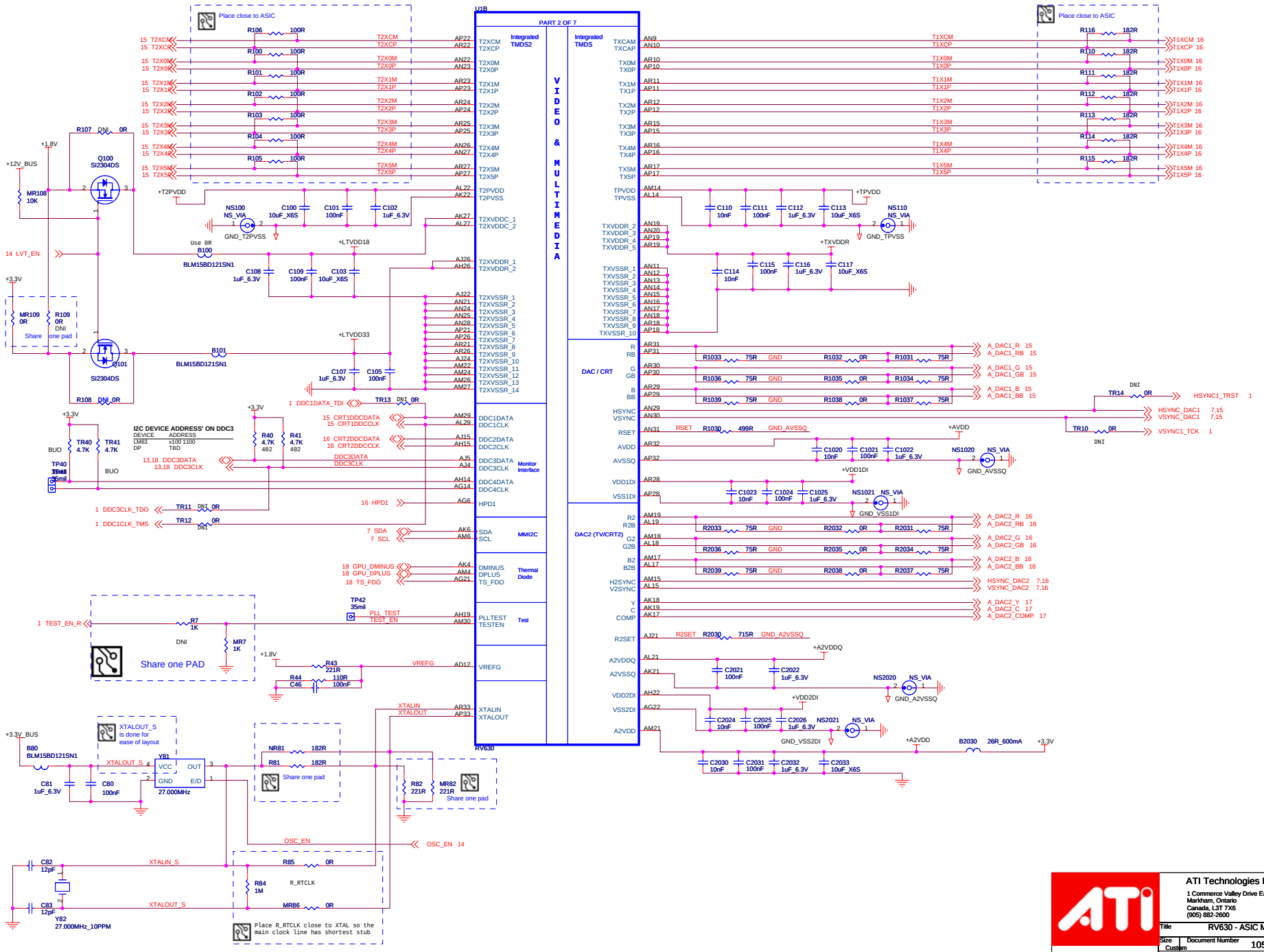
1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600		
Title	RV630 GDDR3 - ASIC PCIE_Interface	
Size: C	Document Number: 105-B148xx-00A	Rev: A
Date: Friday, March 09, 2007	Sheet 2 of 21	

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402



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1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600	
Title	RV630 - ASIC MAIN
Size: Custom	Document Number: 105-B148xx-00A
Rev: A	
Date: Friday, March 09, 2007	Sheet 3 of 21

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402

U1E

PART 5 OF 7

POWER

Memory I/O

PCI-Express

Core

Selected PLL's

Mechanical Pins

RV630

Install only one of these two

Install only one of these two

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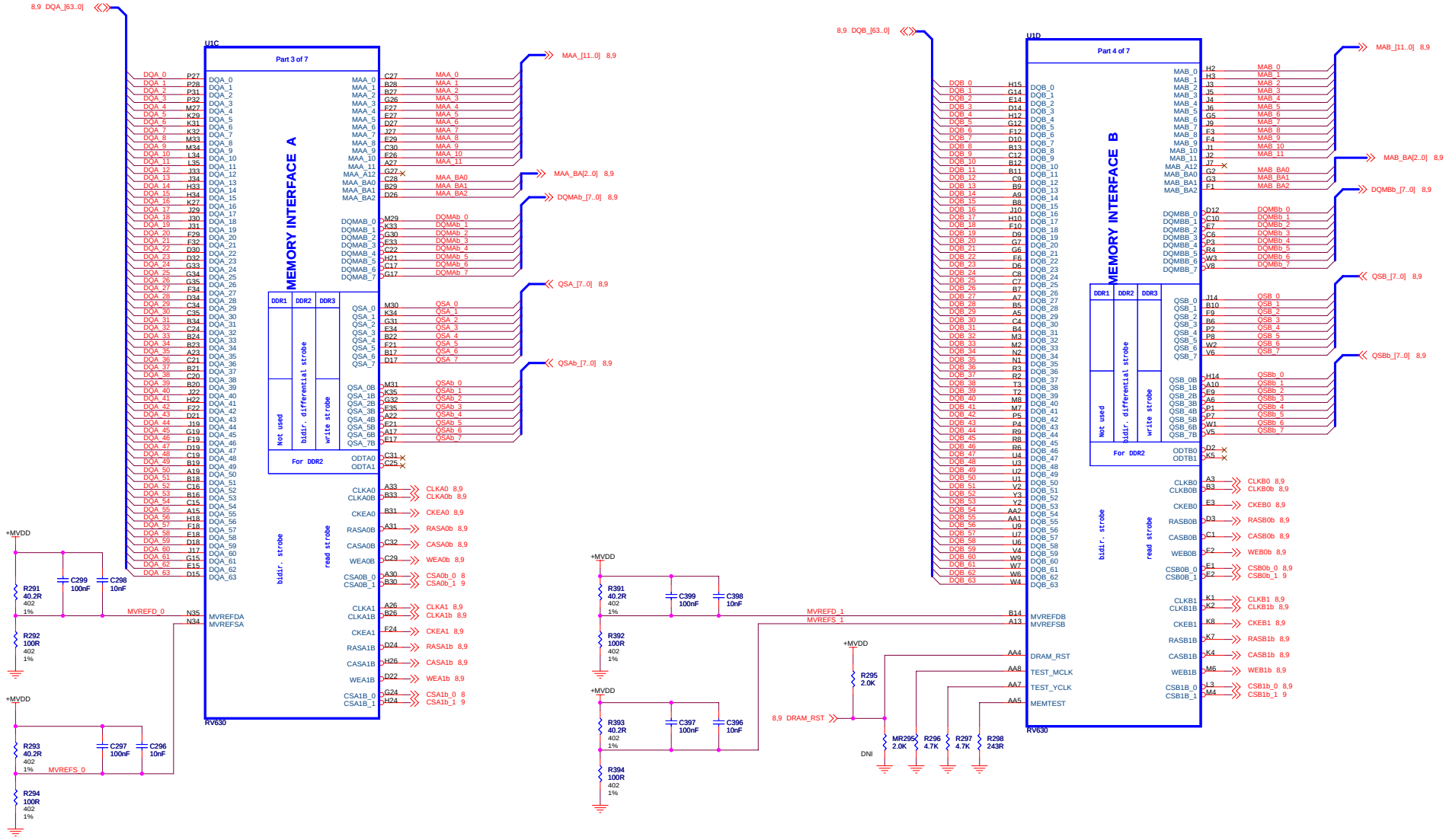
Title	RV630 GDDR3 - ASIC Power		
Size: C	Document Number: 105-B148xx-00A		Rev: A
Date: Friday, March 09, 2007	Sheet 4 of 21		



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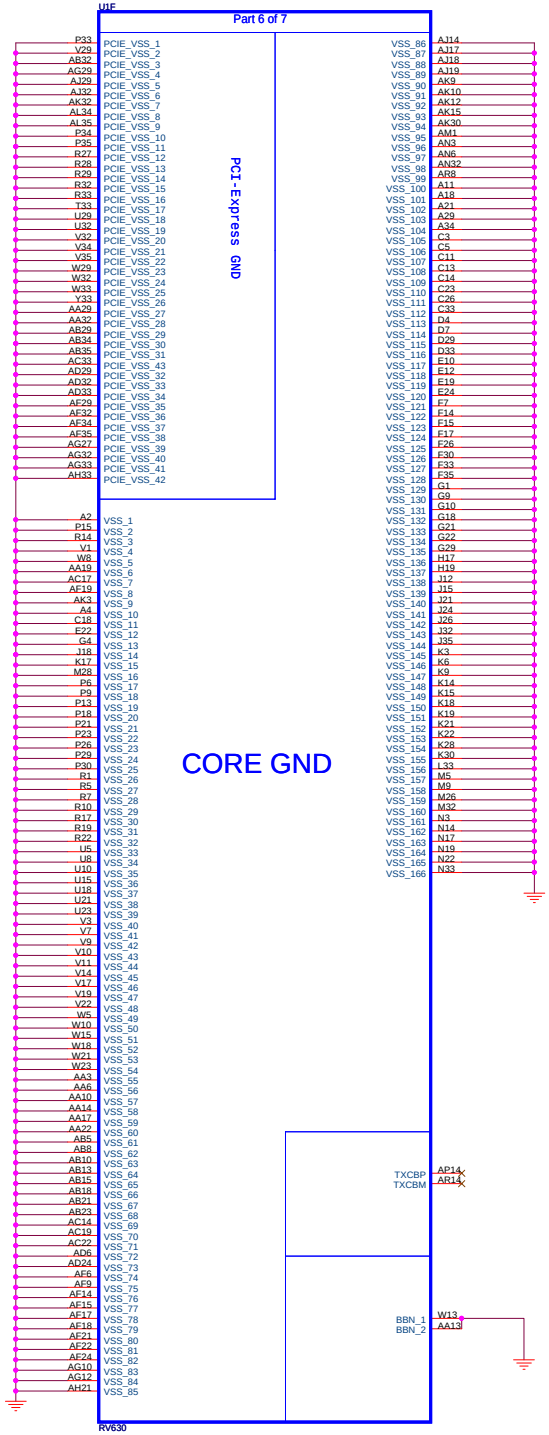
Title: RV630 GDDR3 - ASIC Memory Interface (Channel A & B)

Size	Document Number	Rev
C	105-B148xx-00A	A

Date: Friday, March 09, 2007 | Sheet 5 of 21



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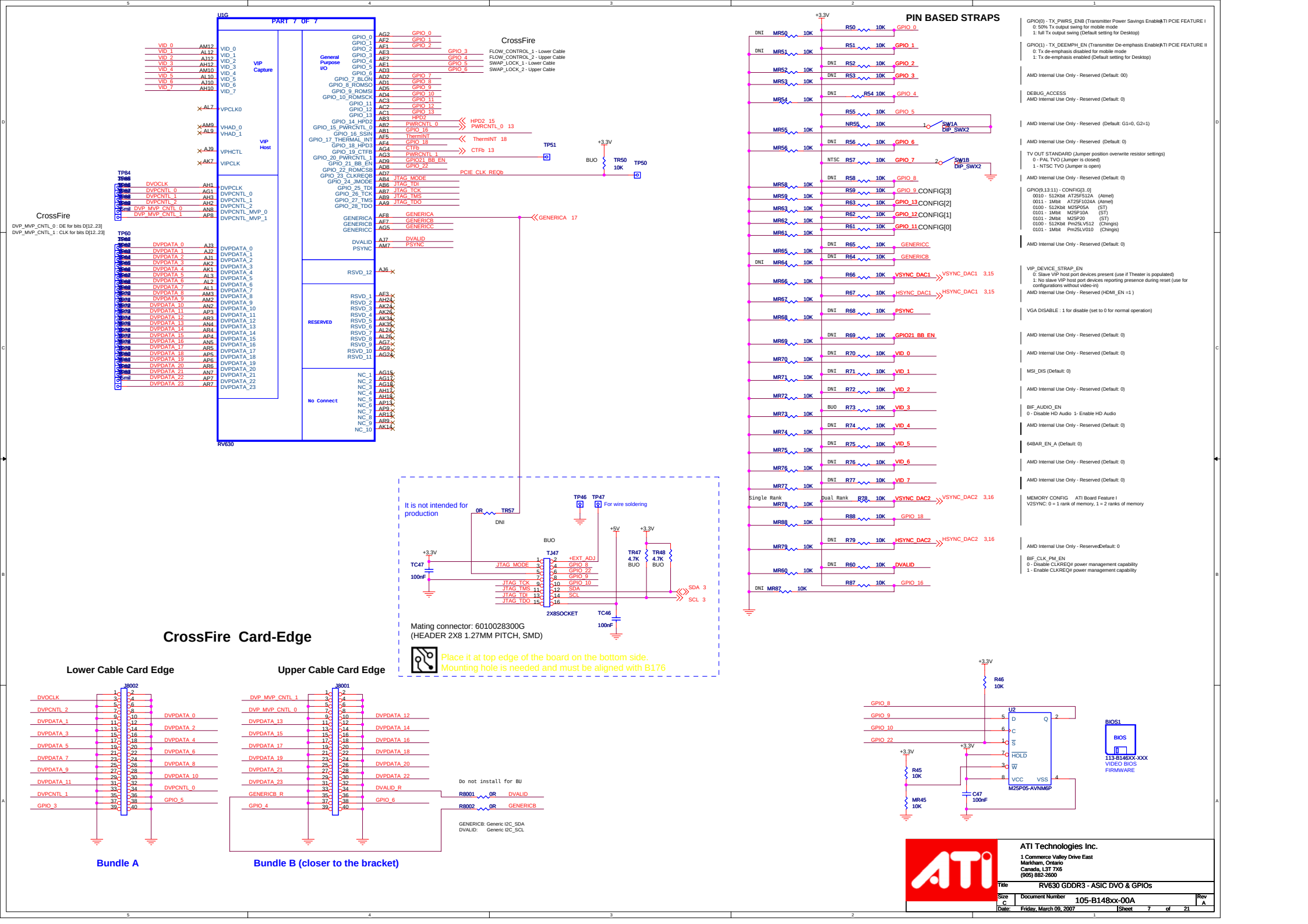
Title	RV630 GDDR3 - ASIC Grounds	
Size: C	Document Number: 105-B148xx-00A	Rev: A
Date: Friday, March 09, 2007	Sheet 6 of 21	


U1G
PART 7 OF 7
RV630
VID_0 AM12
VID_1 AL12
VID_2 AJ12
VID_3 AH12
VID_4 AM10
VID_5 AL10
VID_6 AJ10
VID_7 AH10
VIP Capture
AL7 VPCLK0
AM9 VHAD_0
AL9 VHAD_1
VIP Host
AJ9 VPHCTL
AK7 VIPCLK
TP84
DVOCLK AH1
DVPCNTL_0 AG1
DVPCNTL_1 AH3
DVPCNTL_2 AH2
DVP_MVP_CNTL_0 AN8
DVP_MVP_CNTL_1 AP8
DVPCLK
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_MVP_0
DVPCNTL_MVP_1
CrossFire
DVP_MVP_CNTL_0 : DE for bits D[12..23]
DVP_MVP_CNTL_1 : CLK for bits D[12..23]
TP60
DVPDATA_0 AJ3
DVPDATA_1 AJ2
DVPDATA_2 AJ1
DVPDATA_3 AK2
DVPDATA_4 AK1
DVPDATA_5 AL3
DVPDATA_6 AL2
DVPDATA_7 AL1
DVPDATA_8 AM3
DVPDATA_9 AM2
DVPDATA_10 AN2
DVPDATA_11 AP3
DVPDATA_12 AR3
DVPDATA_13 AN4
DVPDATA_14 AR4
DVPDATA_15 AP4
DVPDATA_16 AN5
DVPDATA_17 AR5
DVPDATA_18 AP5
DVPDATA_19 AP6
DVPDATA_20 AR6
DVPDATA_21 AN7
DVPDATA_22 AP7
DVPDATA_23 AR7
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
General Purpose I/O
GPIO_0 AG2 GPIO_0
GPIO_1 AF2 GPIO_1
GPIO_2 AE1 GPIO_2
GPIO_3 AE3 GPIO_3
GPIO_4 AF2 GPIO_4
GPIO_5 AE1 GPIO_5
GPIO_6 AD3 GPIO_6
GPIO_7_BLON AD2 GPIO_7
GPIO_8_ROMSO AD1 GPIO_8
GPIO_9_ROMSI AD5 GPIO_9
GPIO_10_ROMSCK AD4 GPIO_10
GPIO_11 AC3 GPIO_11
GPIO_12 AC2 GPIO_12
GPIO_13 AC1 GPIO_13
GPIO_14_HPD2 AB3 HPD2
GPIO_15_PWRCNTL_0 AB2 PWRCNTL_0
GPIO_16_SSIN AB1 GPIO_16
GPIO_17_THERMAL_INT AF5 ThermINT
GPIO_18_HPD3 AF4 GPIO_18
GPIO_19_CTFB AG4 CTFb
GPIO_20_PWRCNTL_1 AG3 PWRCNTL_1
GPIO_21_BB_EN AD9 GPIO21_BB_EN
GPIO_22_ROMCSB AD8 GPIO_22
GPIO_23_CLKREQB AD7 PCIE_CLK_REQb
GPIO_24_JMODE AB4 JTAG_MODE
GPIO_25_TDI AB6 JTAG_TDI
GPIO_26_TCK AB7 JTAG_TCK
GPIO_27_TMS AB9 JTAG_TMS
GPIO_28_TDO AA9 JTAG_TDO
HPD2_15
PWRCNTL_0_13
ThermINT_18
CTFb_13
TP51
+3.3V
BUO
TR50 10K
TP50
GENERICA AF8 GENERICA
GENERICB AF7 GENERICB
GENERICC AG5 GENERICC
GENERICA_17
DVALID AJ7 DVALID
PSYNC AM7 PSYNC
RSVD_12 AJ6
RESERVED
RSVD_1 AF3
RSVD_2 AH24
RSVD_3 AK24
RSVD_4 AK26
RSVD_5 AK34
RSVD_6 AK35
RSVD_7 AL24
RSVD_8 AL26
RSVD_9 AG7
RSVD_10 AG9
RSVD_11 AG24
No Connect
NC_1 AG15
NC_2 AG17
NC_3 AG18
NC_4 AH17
NC_5 AH18
NC_6 AP13
NC_7 AP9
NC_8 AR13
NC_9 AR9
NC_10 AK14
CrossFire
FLOW_CONTROL_1 - Lower Cable
FLOW_CONTROL_2 - Upper Cable
SWAP_LOCK_1 - Lower Cable
SWAP_LOCK_2 - Upper Cable
PIN BASED STRAPS
+3.3V
DNI MR50 10K R50 10K GPIO_0
DNI MR51 10K R51 10K GPIO_1
DNI MR52 10K R52 10K GPIO_2
DNI MR53 10K R53 10K GPIO_3
DNI MR54 10K R54 10K GPIO_4
R55 10K GPIO_5
MR55 10K NR55 10K SW1A DIP_SWX2
MR56 10K DNI R56 10K GPIO_6
NTSC R57 10K GPIO_7 SW1B DIP_SWX2
DNI MR58 10K R58 10K GPIO_8
MR59 10K R59 10K GPIO_9 CONFIG[3]
MR63 10K R63 10K GPIO_13 CONFIG[2]
MR62 10K R62 10K GPIO_12 CONFIG[1]
MR61 10K R61 10K GPIO_11 CONFIG[0]
DNI MR65 10K R65 10K GENERICC
DNI MR64 10K R64 10K GENERICB
MR66 10K R66 10K VSYNC_DAC1 VSYNC_DAC1 3,15
MR67 10K R67 10K HSYNC_DAC1 HSYNC_DAC1 3,15
MR68 10K DNI R68 10K PSYNC
MR69 10K DNI R69 10K GPIO21_BB_EN
MR70 10K DNI R70 10K VID_0
MR71 10K DNI R71 10K VID_1
MR72 10K DNI R72 10K VID_2
MR73 10K BUO R73 10K VID_3
MR74 10K DNI R74 10K VID_4
MR75 10K DNI R75 10K VID_5
MR76 10K DNI R76 10K VID_6
MR77 10K DNI R77 10K VID_7
Single Rank MR78 10K Dual Rank R78 10K VSYNC_DAC2 VSYNC_DAC2 3,16
MR88 10K R88 10K GPIO_18
MR79 10K DNI R79 10K HSYNC_DAC2 HSYNC_DAC2 3,16
MR60 10K DNI R60 10K DVALID
DNI MR87 10K R87 10K GPIO_16
GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)
GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)
AMD Internal Use Only - Reserved (Default: 00)
DEBUG_ACCESS
AMD Internal Use Only - Reserved (Default: 0)
AMD Internal Use Only - Reserved (Default: G1=0, G2=1)
AMD Internal Use Only - Reserved (Default: 0)
TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)
AMD Internal Use Only - Reserved (Default: 0)
GPIO(9,13:11) - CONFIG[3..0]
0010 - 512Kbit AT25F512A (Atmel)
0011 - 1Mbit AT25F1024A (Atmel)
0100 - 512Kbit M25P05A (ST)
0101 - 1Mbit M25P10A (ST)
0101 - 2Mbit M25P20 (ST)
0100 - 512Kbit Pm25LV512 (Chingis)
0101 - 1Mbit Pm25LV010 (Chingis)
AMD Internal Use Only - Reserved (Default: 0)
VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)
AMD Internal Use Only - Reserved (HDMI_EN =1)
VGA DISABLE : 1 for disable (set to 0 for normal operation)
AMD Internal Use Only - Reserved (Default: 0)
AMD Internal Use Only - Reserved (Default: 0)
MSI_DIS (Default: 0)
AMD Internal Use Only - Reserved (Default: 0)
BIF_AUDIO_EN
0 - Disable HD Audio 1- Enable HD Audio
AMD Internal Use Only - Reserved (Default: 0)
64BAR_EN_A (Default: 0)
AMD Internal Use Only - Reserved (Default: 0)
AMD Internal Use Only - Reserved (Default: 0)
MEMORY CONFIG ATI Board Feature I
VZSYNC: 0 = 1 rank of memory, 1 = 2 ranks of memory
AMD Internal Use Only - Reserved Default: 0
BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability
It is not intended for production
0R TR57 DNI
TP46 TP47 For wire soldering
BUO
+3.3V
TC47 100nF
TJ47
JTAG_MODE
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
+EXT_ADJ
GPIO_8
GPIO_22
GPIO_9
GPIO_10
SDA
SCL
2X8SOCKET
+5V
+3.3V
TR47 4.7K BUO
TR48 4.7K BUO
SDA_3
SCL_3
TC46 100nF
Mating connector: 6010028300G
(HEADER 2X8 1.27MM PITCH, SMD)
Place it at top edge of the board on the bottom side.
Mounting hole is needed and must be aligned with B176
CrossFire Card-Edge
Lower Cable Card Edge
J8002
DVOCLK
DVPCNTL_2
DVPDATA_1
DVPDATA_3
DVPDATA_5
DVPDATA_7
DVPDATA_9
DVPDATA_11
DVPCNTL_1
GPIO_3
DVPDATA_0
DVPDATA_2
DVPDATA_4
DVPDATA_6
DVPDATA_8
DVPDATA_10
DVPCNTL_0
GPIO_5
Upper Cable Card Edge
J8001
DVP_MVP_CNTL_1
DVP_MVP_CNTL_0
DVPDATA_13
DVPDATA_15
DVPDATA_17
DVPDATA_19
DVPDATA_21
DVPDATA_23
GENERICB_R
GPIO_4
DVPDATA_12
DVPDATA_14
DVPDATA_16
DVPDATA_18
DVPDATA_20
DVPDATA_22
DVALID_R
GPIO_6
Do not install for BU
R8001 0R DVALID
R8002 0R GENERICB
GENERICB: Generic I2C_SDA
DVALID: Generic I2C_SCL
Bundle A
Bundle B (closer to the bracket)
+3.3V
R46 10K
GPIO_8
GPIO_9
GPIO_10
GPIO_22
U2
D Q
C
S
HOLD
W
VCC VSS
M25P05-AVNM6P
R45 10K
MR45 10K
C47 100nF
BIOS1
BIOS
113-B146XX-XXX
VIDEO BIOS
FIRMWARE
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
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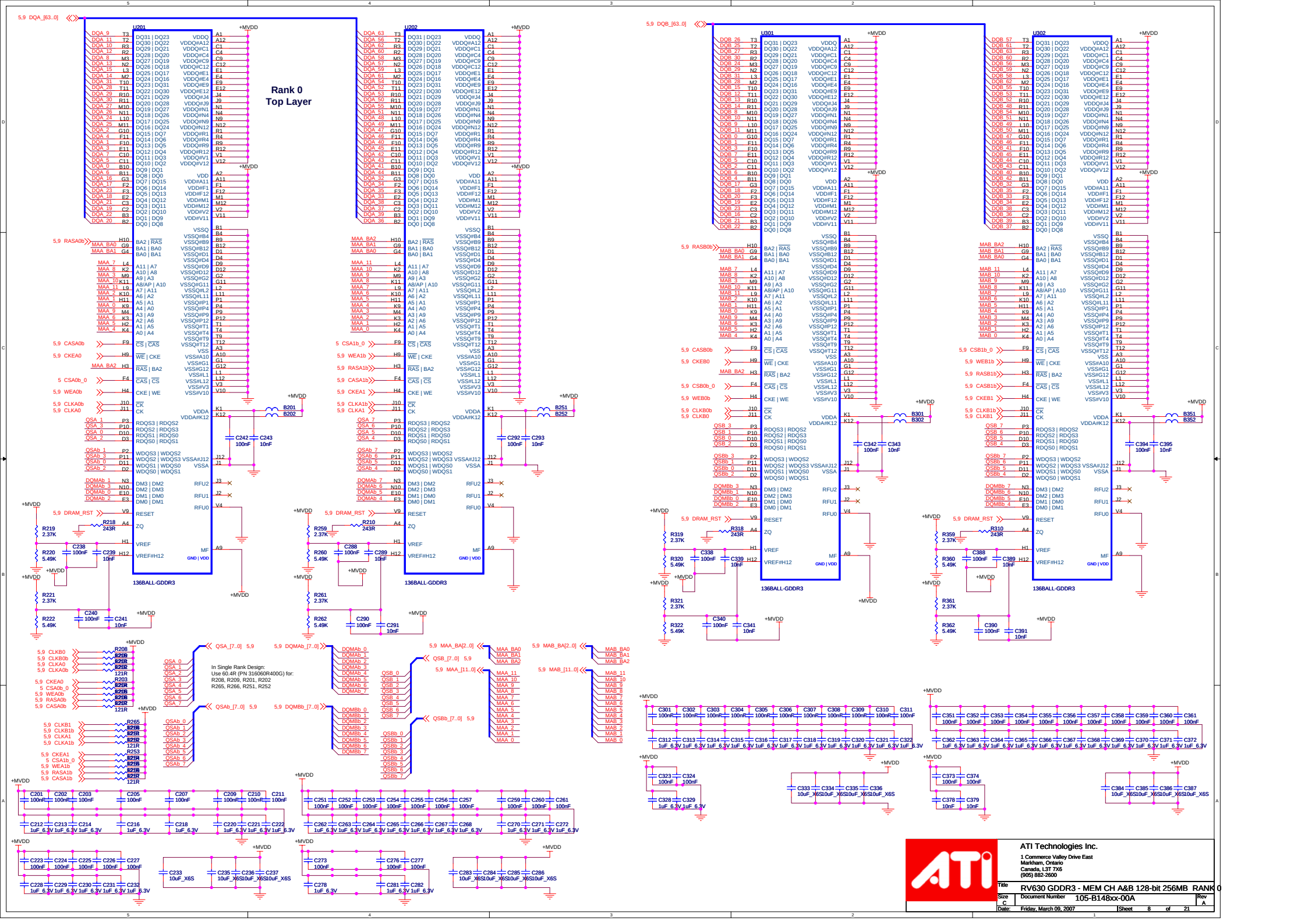
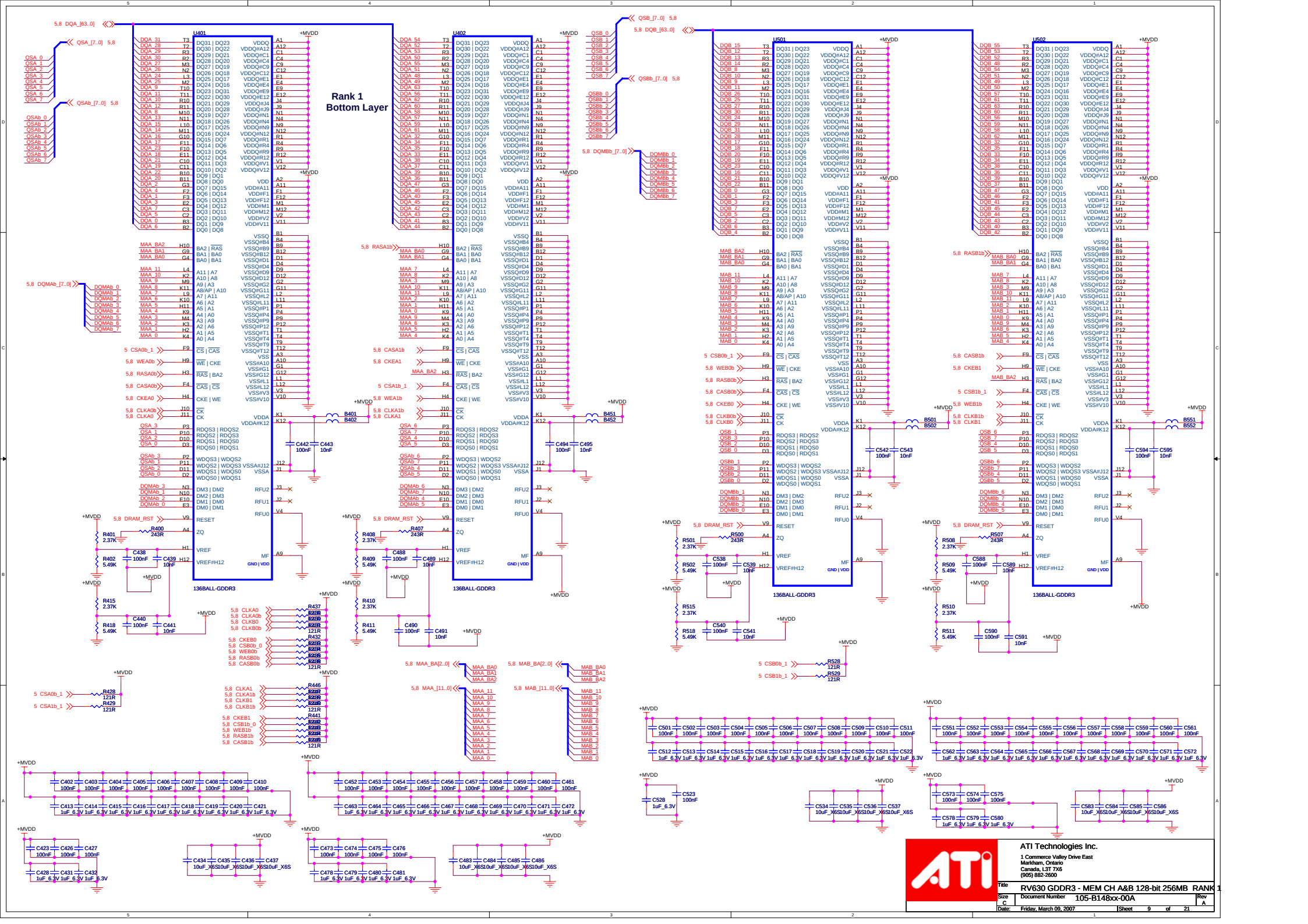
(905) 882-2600
Title RV630 GDDR3 - ASIC DVO & GPIOs
Size C
Document Number 105-B148xx-00A
Rev A
Date: Friday, March 09, 2007
Sheet 7 of 21


Rank 0
Top Layer
U201
U202
U301
U302
136BALL-GDDR3
In Single Rank Design:
Use 60.4R (PN 316060R400G) for:
R208, R209, R201, R202
R265, R266, R251, R252
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600
Title
RV630 GDDR3 - MEM CH A&B 128-bit 256MB RANK 0
Size
C
Document Number
105-B148xx-00A
Rev
A
Date:
Friday, March 09, 2007
Sheet
8
of
21


Rank 1
Bottom Layer
U401
U402
U501
U502
136BALL-GDDR3
5,8 DQA_[63..0]
5,8 DQB_[63..0]
QSA_[7..0] 5,8
QSAb_[7..0] 5,8
QSB_[7..0] 5,8
QSBb_[7..0] 5,8
5,8 DQMAb_[7..0]
5,8 DQMBb_[7..0]
+MVDD
GND | VDD
ATI Technologies Inc.
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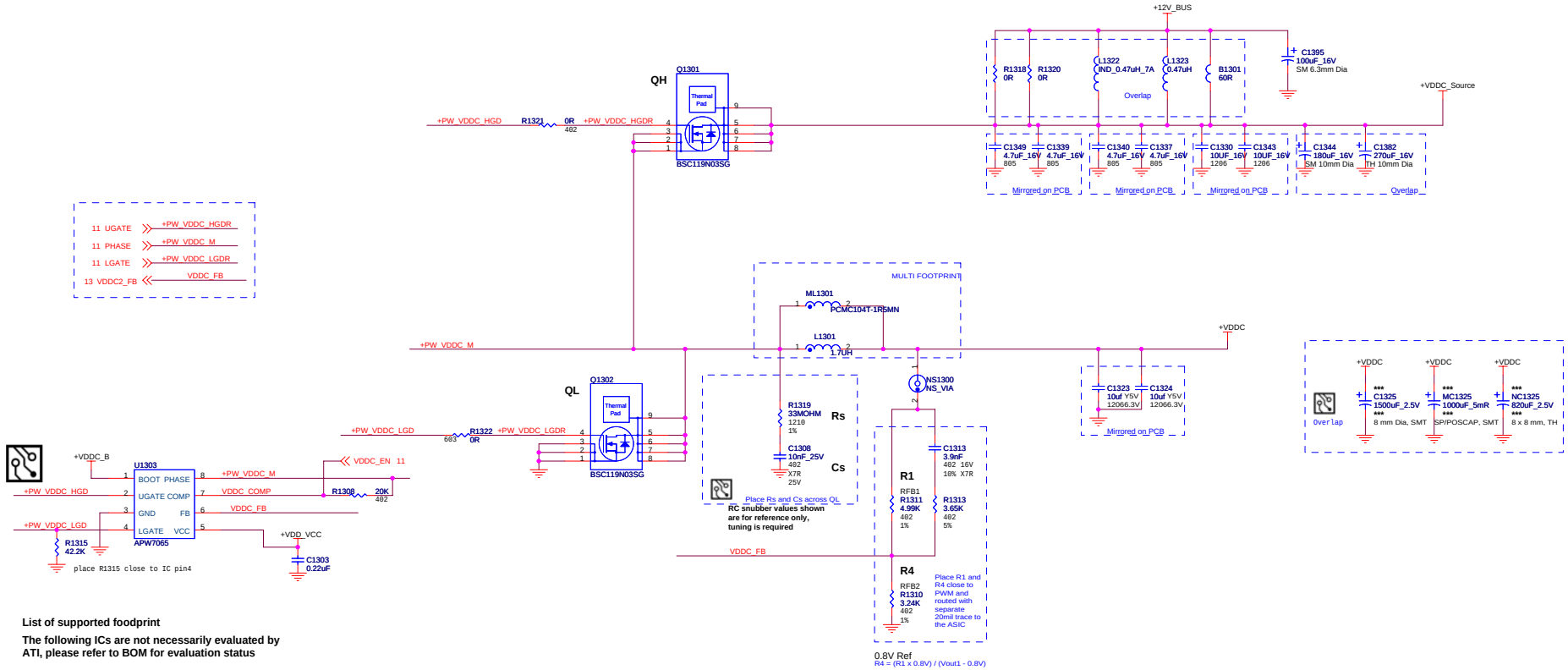
Canada, L3T 7X6
(905) 882-2600
Title RV630 GDDR3 - MEM CH A&B 128-bit 256MB RANK 1
Size C
Document Number 105-B148xx-00A
Rev 1.A
Date: Friday, March 09, 2007
Sheet 9 of 21



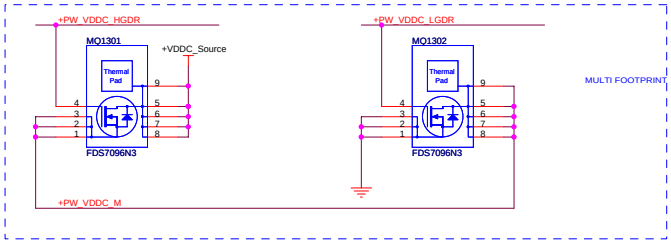
List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7120/APW7065 (12V)
CAT CAT7583 (12V)
INTERSIL ISL6545
NEXSEM NX2114/2307
RICHTEK RT9214/RT8101
OnSemi ON1582
uPI UP6101 (No Ext_Vref in)

Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



SMPS02- Regulator for VDDC

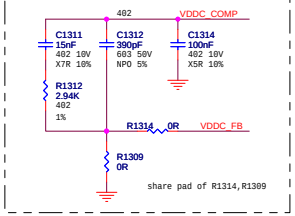
Vout = 0.9V ~ 1.1V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G

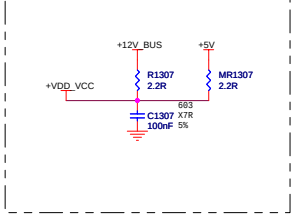
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

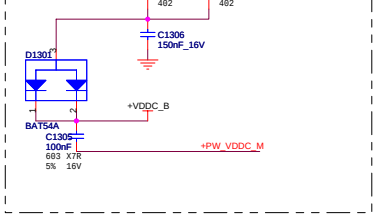
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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Title: RV630 GDDR3 - VDDC SMPS 01
Size: Custom | Document Number: 105-B148xx-00A | Rev: A
Date: Friday, March 09, 2007 | Sheet 10 of 21

Information on Compatable Controller Parts

	PWM IC #1	PWM IC #2	PWM IC #3	PWM IC #4	
Gate drive voltage	5V, 8V, 12V	5V, 8V, 12V	5V only	12V only	
Vref	0.6V	0.6V	0.6V	0.6V	
Bootstrap diodes	Internal (DNP D601, D611)	Internal (DNP D601, D611)	External (Populate D601, D611)	Internal (DNP D601, D611)	
Phase current adjustable (unbalanced between phases)	Yes	Yes	Yes	TBD	
Option Pin Selection					
Pin 10 (IOUT/IMAX/DROOP)	IOUT/DROOP (R662)	IOUT/IMAX	IOUT	IOUT/IMAX	
Pin 11 (RT)	R_RT ~= 10,000,000/Fsw	TBD	R_RT ~= 18,600,000/Fsw	TBD	
Pin 12 (COMP/DROOP)	COMP	DROOP (R663)	COMP	COMP	
Pin 14 (SS/ICOMP)	SS/EN	GND (SS fixed internally)	ICOMP (SS dependent on Fsw)	SS	
Pin 16 (REFOUT/POK)	POK (Open drain)	IREFOUT/POK POK voltage = 1.2V	INREFOUT/POK PGood voltage = 1.25V	INREFOUT/PGOOD Vrefout = 0.6V	
Pin 21 (VCCDRV/DROOP)	VCCDRV	VCCDRV	DROOP (R664)	DROOP (R664)	

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661

External Detection Circuit and Indication

Cases	Behaviour	Notifications
External cable not plugged in +12V_BUS not in regulation	12V_EXT_DETb = X EN1 -> "0" (by Ri2) ENb1 -> 3.3V ENBUS = "0"	VDDC disabled
External cable not plugged in +12V_BUS in regulation	12V_EXT_DETb = "1" EN1 -> 3V (by Ri1 and Ri2) ENb1 = 0V ENBUS = "1"	VDDC enabled External Power Missing
External cable plugged in +12V_XXX not in regulation	12V_EXT_DETb = "0" EN1 < 3V (due to low 12V) ENb1 = 3.3V ENBUS = "0"	VDDC disabled
External cable plugged in +12V_XXX in regulation	12V_EXT_DETb = "0" EN1 -> 3V ENb1 = 0V ENBUS = "1"	VDDC enabled Normal Operation

SMPS03 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	1.2V ; +2.5%/-2.5%	0.8V ~ 1.5V
Vout ripple (DC)	TBD	
Iout	TBD	55A (target 60A) max
Step load	TBD	
Vout ripple (AC)	TBD	
Switching Freq.	TBD	50kHz ~ 1MHz
Protections		

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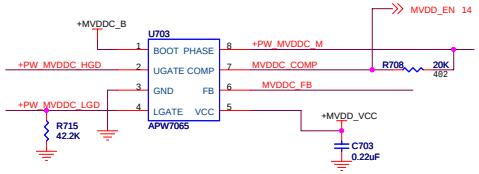
Canada, L3T 7X6
(905) 882-2600

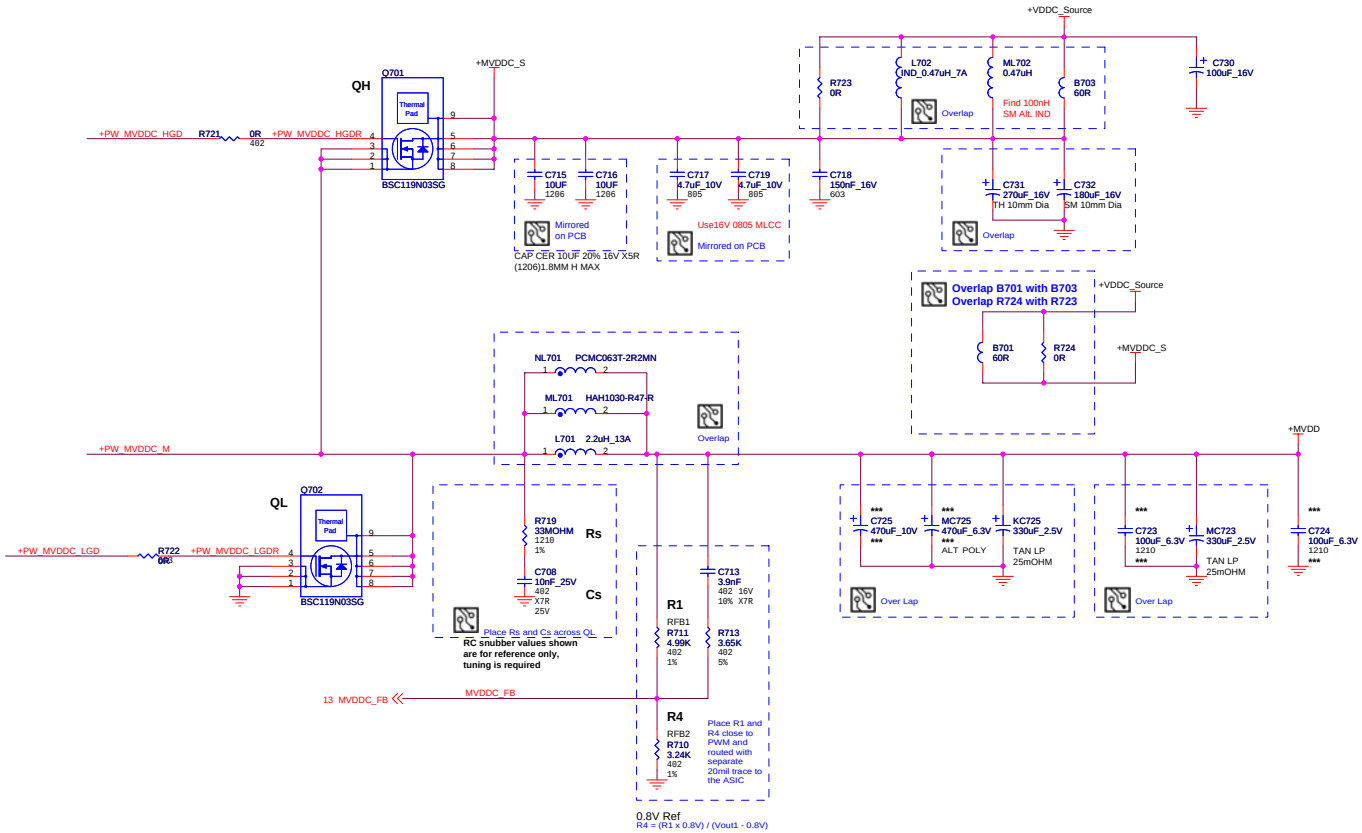
Title: RV630 GDDR3 - VDDC SMPS 02
Size: Custom | Document Number: 105-B148xx-00A | Rev: A
Date: Friday, March 09, 2007 | Sheet 11 of 21

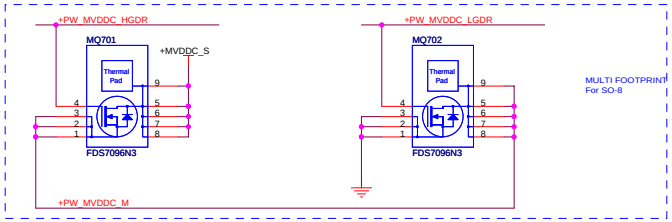


List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

- **ANPEC APW7120/APW7065 (12V)**
- **CAT CAT7583 (12V)**
- **INTERSIL ISL6545**
- **NEXSEM NX2114/2307**
- **RICHTEK RT9214/RT8101**
- **OnSemi ON1582**
- **uPI UP6101 (No Ext_Vref in)**
- **uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**





SMPS02- Regulator for MVDD

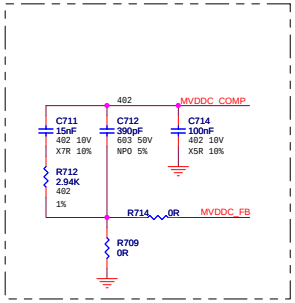
Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G

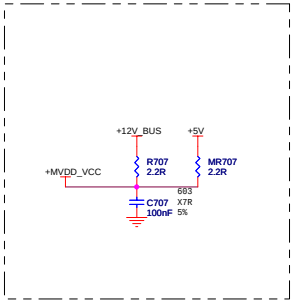
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

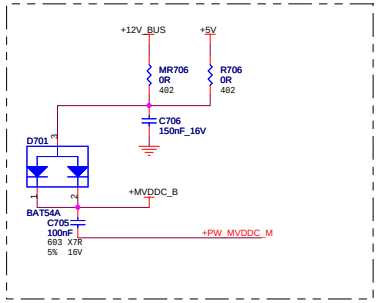
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(Pw MVDDC LGD and Pw MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

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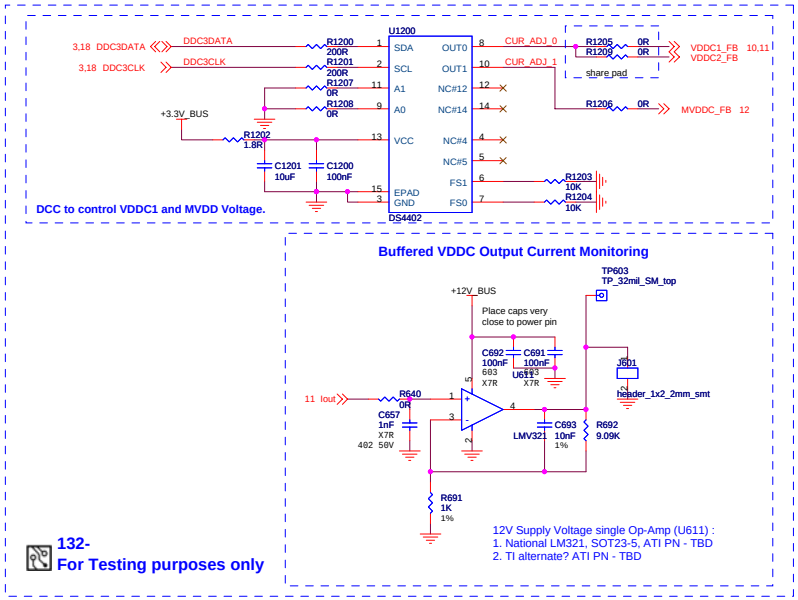
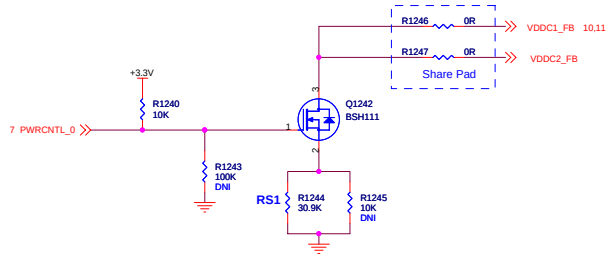
Title: RV630 GDDR3 - MVDD SMPS 01

Size: Custom | Document Number: 105-B148xx-00A | Rev: A

Date: Friday, March 09, 2007 | Sheet 12 of 21

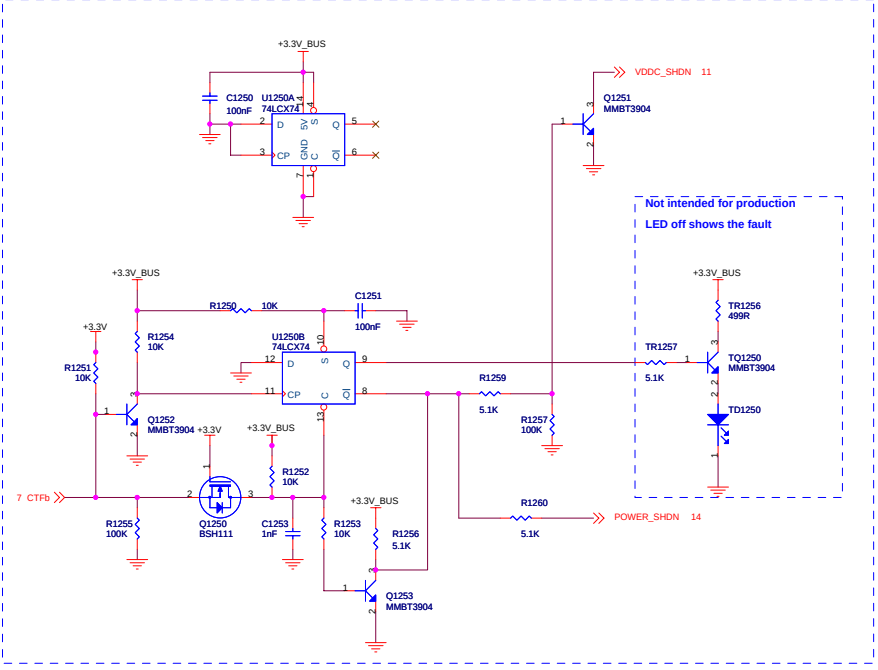




SMPS03- Regulator for VDDC

Vout = .9V ~ 1.2V

	VDDC	RS1	PWRCNTL_0
0.6V Ref	.9V	N/A	LOW
	1.0V	59.0K 1% ATI # 3160590200G	HIGH
	1.1V	30.9K 1% ATI # 3160309200G	HIGH
	1.2V	20.0K 1% ATI # 3160200200G	HIGH



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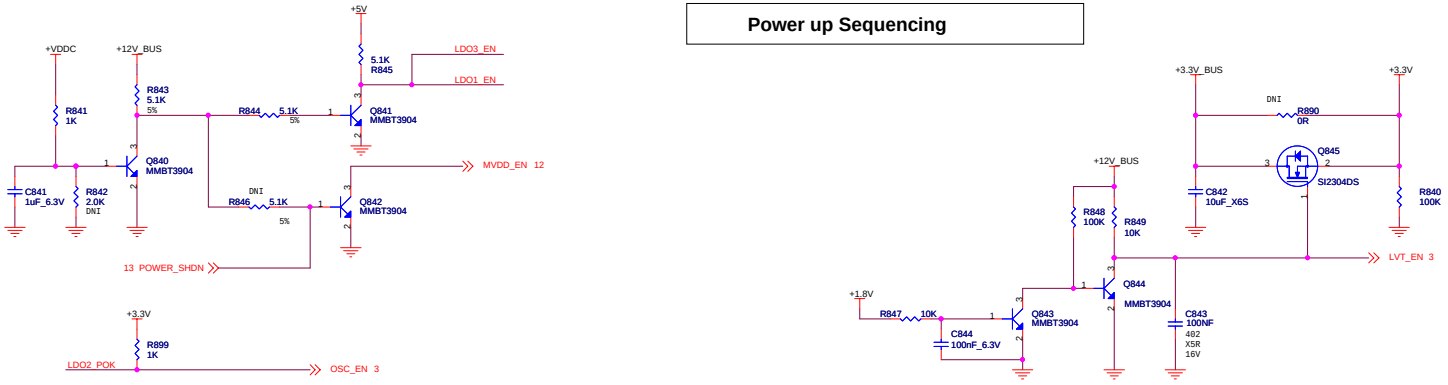
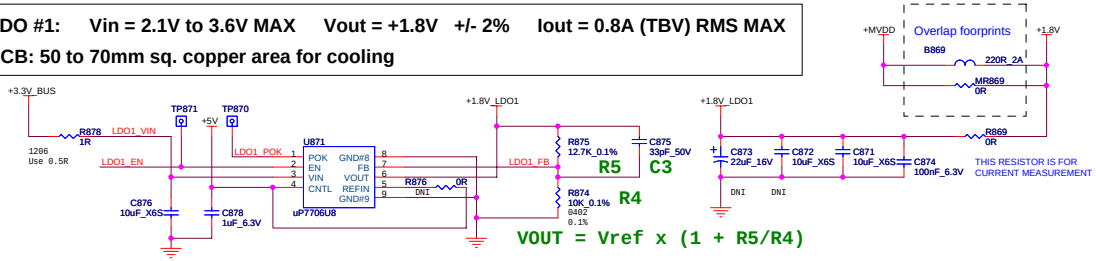
Title	RV630 GDDR3 - Power Management	
Size C	Document Number 105-B148xx-00A	Rev A
Date: Friday, March 09, 2007	Sheet 13 of 21	

Power up Sequencing



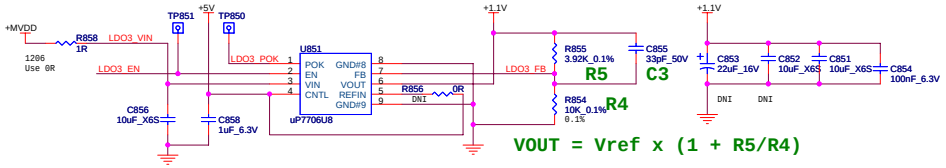
LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

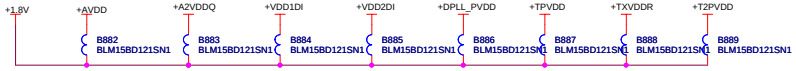


LDO #3: Vin = +1.45V to 2.1VMAX Vout = +1.1V +/- 2% Iout = 1.1A (TBV) RMS MAX

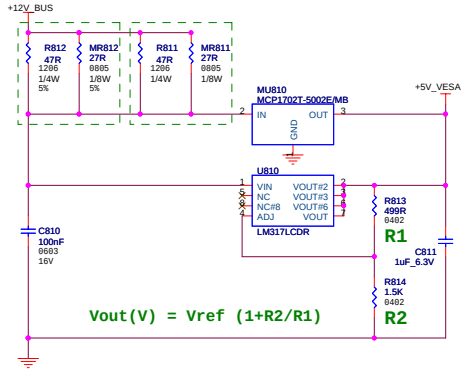
PCB: 50 to 70mm sq. copper area for cooling

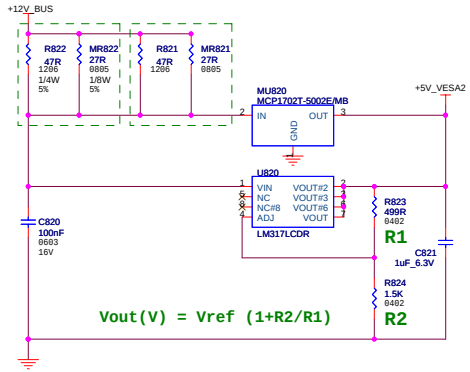


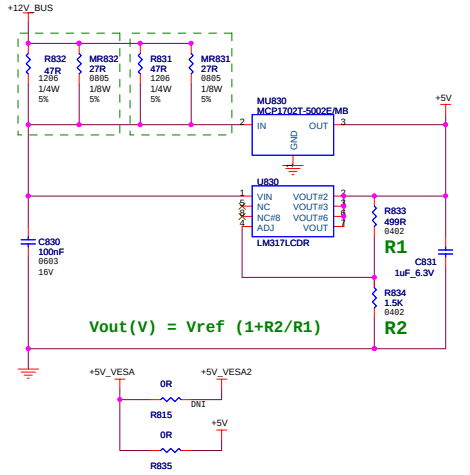
Shared Power Rails



Regulators for +5V, +5V_VESA and +5V_VESA2







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Title	RV630 GDDR3 - Linear Regulators	
Size C	Document Number 105-B148xx-00A	Rev A
Date: Friday, March 09, 2007	Sheet 14 of 21	

See BOM for qualified filters

3 A_DAC1_R
3 A_DAC1_RB
3 A_DAC1_G
3 A_DAC1_GB
3 A_DAC1_B
3 A_DAC1_BB

R1001 75R, C1004 8.0pF, L1001 68nH_300mA, R1024 0R, C1001 12pF_50V, L1004 36NH, A_R_DAC1_M
R1027 37.4R
R1002 75R, C1005 8.0pF, L1002 68nH_300mA, R1025 0R, C1002 12pF_50V, L1005 36NH, A_G_DAC1_M
R1028 37.4R
R1003 75R, C1006 8.0pF, L1003 68nH_300mA, R1026 0R, C1003 12pF_50V, L1006 36NH, A_B_DAC1_M
R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

For ESD Protection

D1001 CM1213-04 (+3.3V)
D1002 CM1213-04 (+5V_VESA)
CH1, CH2, CH3, CH4, Vp, Vn

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

MJ1001 G3179C219-005
R, G, B, MS0, MS1, MS2, MS3, NC, HS, VS, VSS, VSS#6, VSS#7, VSS#8, VSS#10, CASE, CASE#17
DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

C1010 68pF 603

3 CRT1DDCDATA
3 CRT1DDCCLK

R1004 10K, R1005 2.2K, Q1001 BSH111, DDCDATA_DAC1_5V, R1006 33R, DDCDATA_DAC1_R
R1007 10K, R1008 2.2K, Q1002 BSH111, DDCCLK_DAC1_5V, R1009 33R, DDCCLK_DAC1_R

C1999 100nF, U1999A, U1999B 74VHC125

3,7 HSYNC_DAC1
HSYNC_DAC1_B, R1010 10R, HSYNC_DAC1_R
3,7 VSYNC_DAC1
VSYNC_DAC1_B, R1011 10R, VSYNC_DAC1_R

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

7 HPD2
Q1021 MMBT3904, R1022 10K, R1023 10K, HPD_DVI2

3 T2X2M, 3 T2X2P
3 T2X4M, 3 T2X4P
DDCCLK_DAC1_R
DDCDATA_DAC1_R
VSYNC_DAC1_R
3 T2X1M, 3 T2X1P
3 T2X3M, 3 T2X3P
3 T2X0M, 3 T2X0P
3 T2X5M, 3 T2X5P
3 T2XCP, 3 T2XCM
A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
HSYNC_DAC1_R

J1001 DVI_CONNECTOR
CASE
TMDS Data2-, TMDS Data2+, TMDS Data2/4 Shield, TMDS Data4-, TMDS Data4+, DDC Clock, DDC Data, Analog VSYNC, TMDS Data1-, TMDS Data1+, TMDS Data1/3 Shield, TMDS Data3-, TMDS Data3+, +5V Power, GND (for +5V), Hot Plug Detect, TMDS Data0-, TMDS Data0+, TMDS Data0/5 Shield, TMDS Data5-, TMDS Data5+, TMDS Clock Shield, TMDS Clock+, TMDS Clock-
Analog Red, Analog Green, Analog Blue, Analog HYNC, Analog GND, Analog GND#C6
CASE#26, CASE#27, CASE#28, CASE#29, CASE#30

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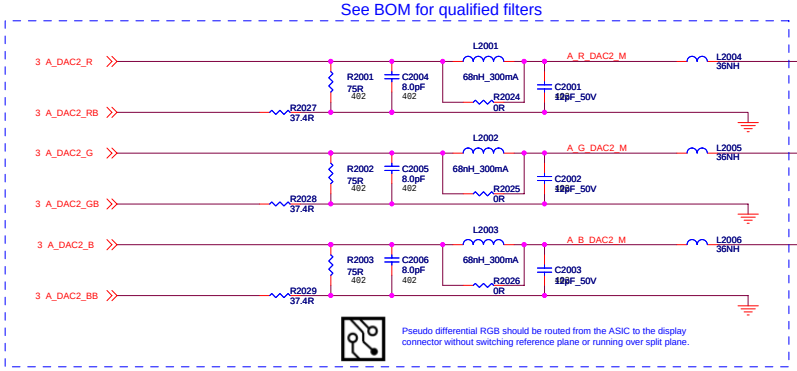
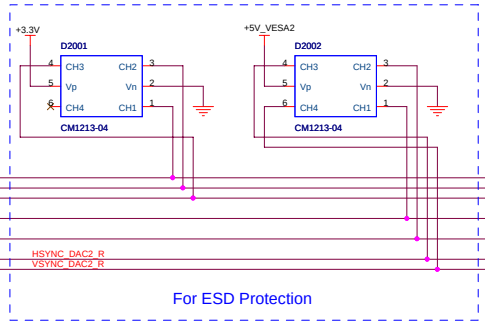
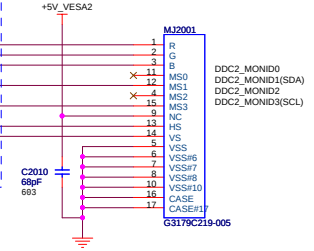
Title: RV630 GDDR3- DAC1&TMDS2
Size: Custom
Document Number: 105-B148xx-00A
Rev: A
Date: Friday, March 09, 2007
Sheet 15 of 21

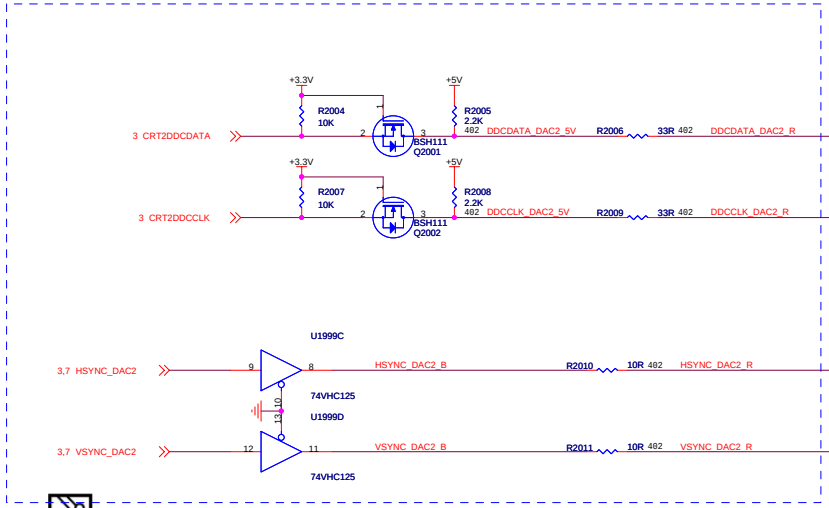
See BOM for qualified filters





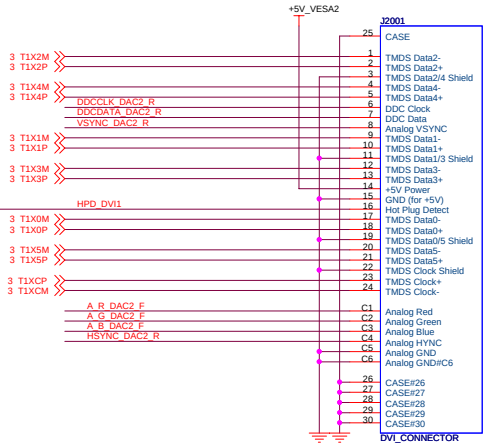


A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



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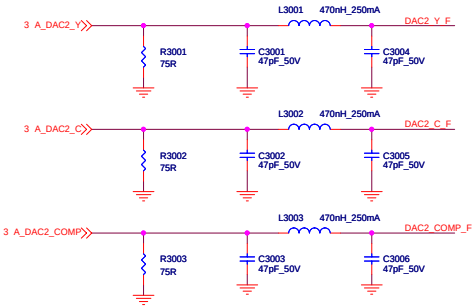
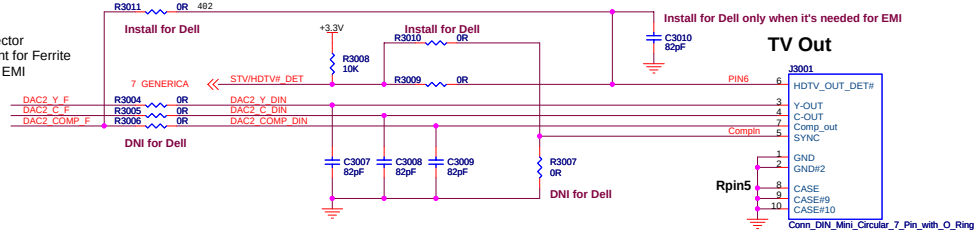
Title	RV630 GDDR3-DAC2/TMDS1	
Size: Custom	Document Number: 105-B148xx-00A	Rev: A
Date: Friday, March 09, 2007	Sheet 16 of 21	



Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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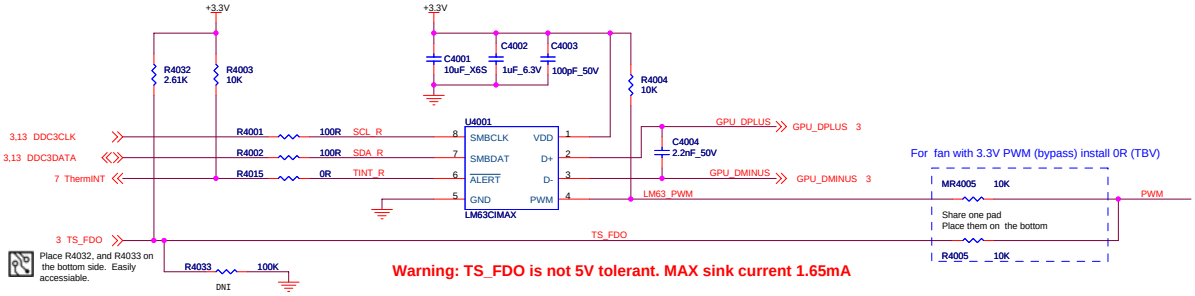
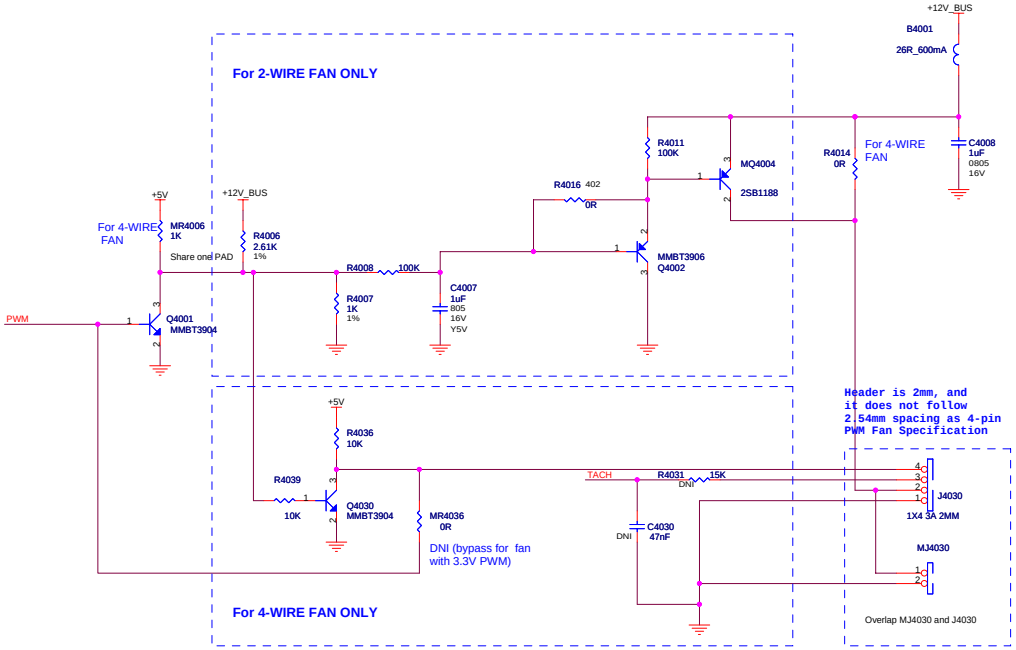
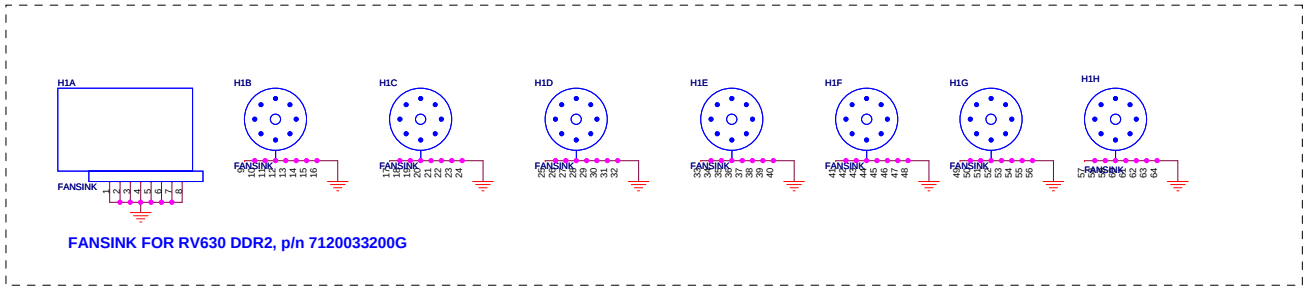
Title	RV630 GDDR3 - TVO	
Size C	Document Number 105-B148xx-00A	Rev A
Date: Friday, March 09, 2007	Sheet 17 of 21	

LM63 is for BU only, until built-in fan controller is verified.



Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA





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Title	RV630 GDDR3- Thermal Management	
Size C	Document Number 105-B148xx-00A	Rev A
Date: Friday, March 09, 2007	Sheet 18 of 21	

DVI/DVI SCREWS with top tab

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET
8020042500G

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

DNI
SK1
RV410SOCKET

MT2
MT_Hole_0.136_in_6VIA

PCB1
PCB
109-GN982-00A

<Variant Name>

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Title	RV630 GDDR3- Mechanical	
Size: C	Document Number: 105-B148xx-00A	Rev: A
Date: Friday, March 09, 2007	Sheet 19 of 21	

<variant Name>

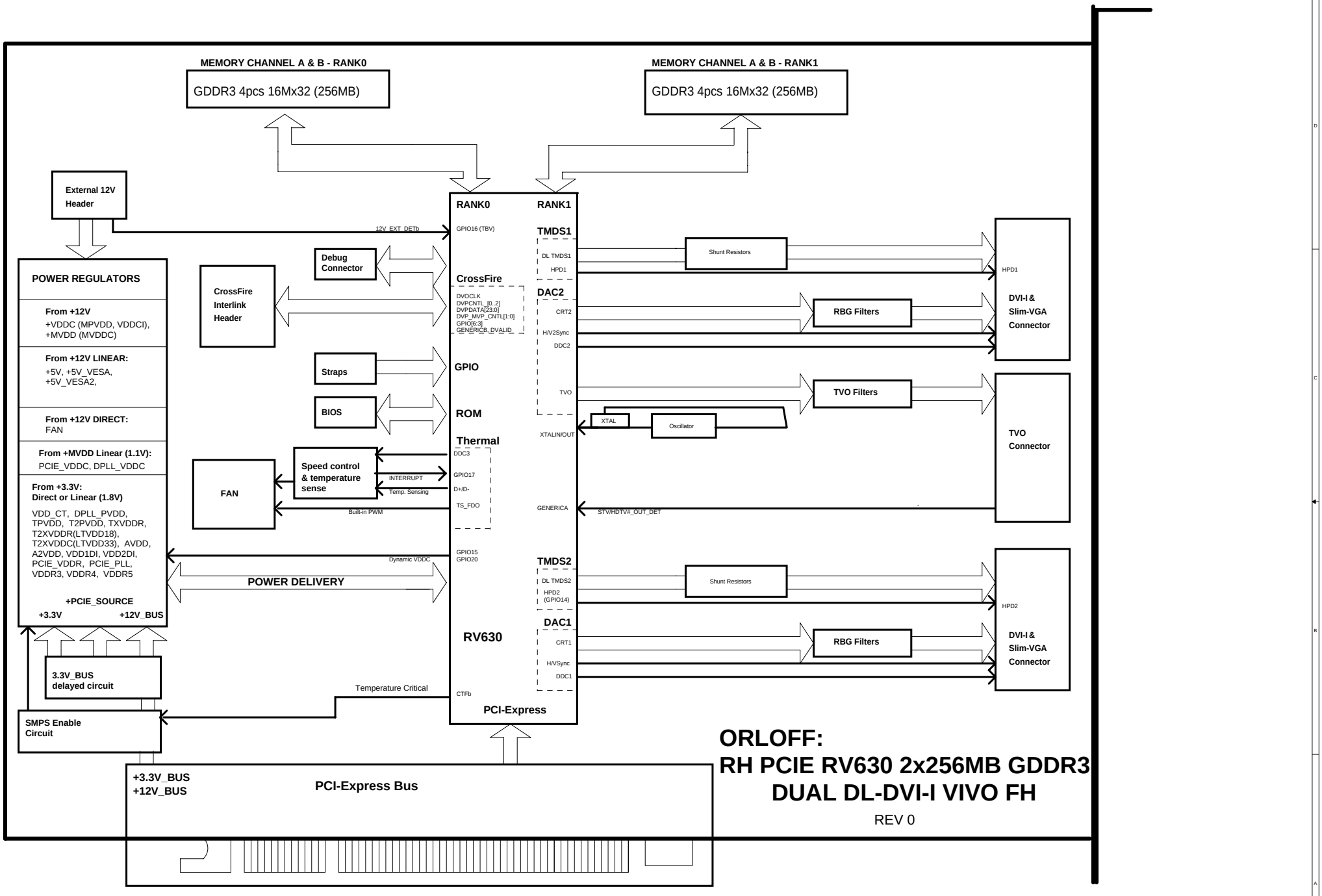
Title	Schematic No.	Date:
RH PCIE RV630 2x256MB GDDR3 DUAL DL-DVI-I VIVO FH	105-B148xx-00A	Friday, March 09, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact ATI representative to obtain latest BOM closest to the application desired.**

Rev A

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/02/06	Initial design for RV630 GDDR3



ORLOFF:
RH PCIE RV630 2x256MB GDDR3
DUAL DL-DVI-I VIVO FH

REV 0

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Title	RV630 GDDR3 - BLOCK DIAGRAM	
Size: C	Document Number: 105-B148xx-00A	Rev: A
Date: Friday, March 09, 2007	Sheet 21 of 21	