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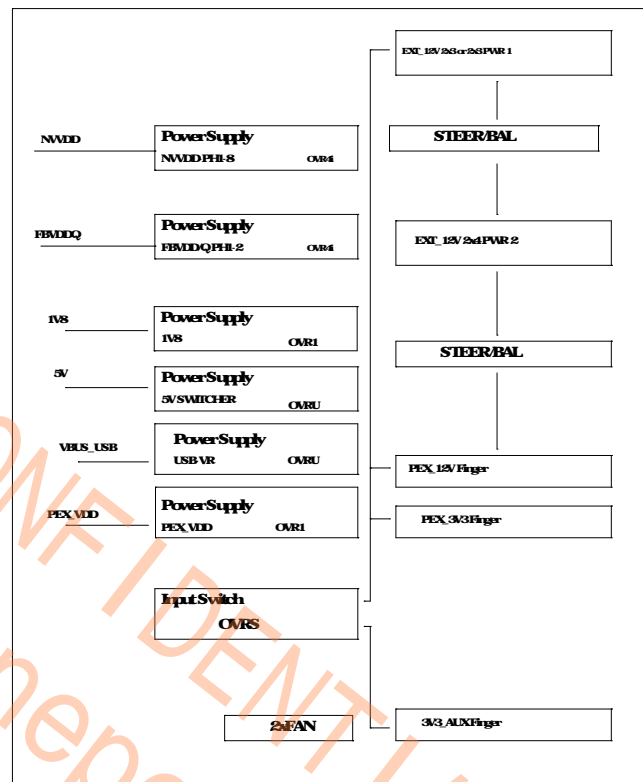
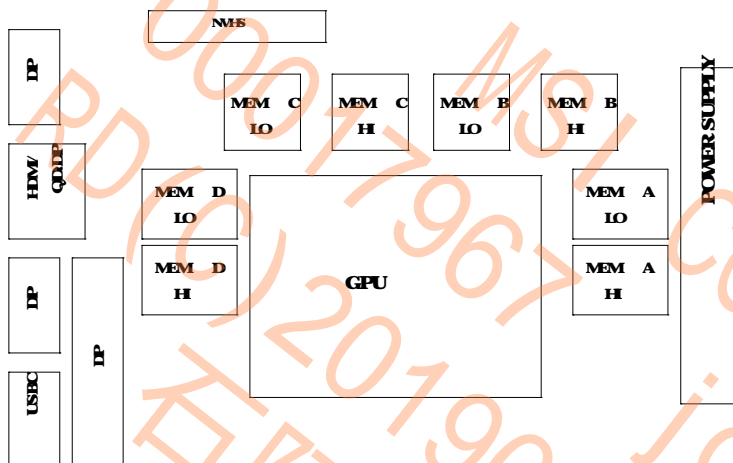
41 PS: INPUT SWITCH/RAIL BALANCE
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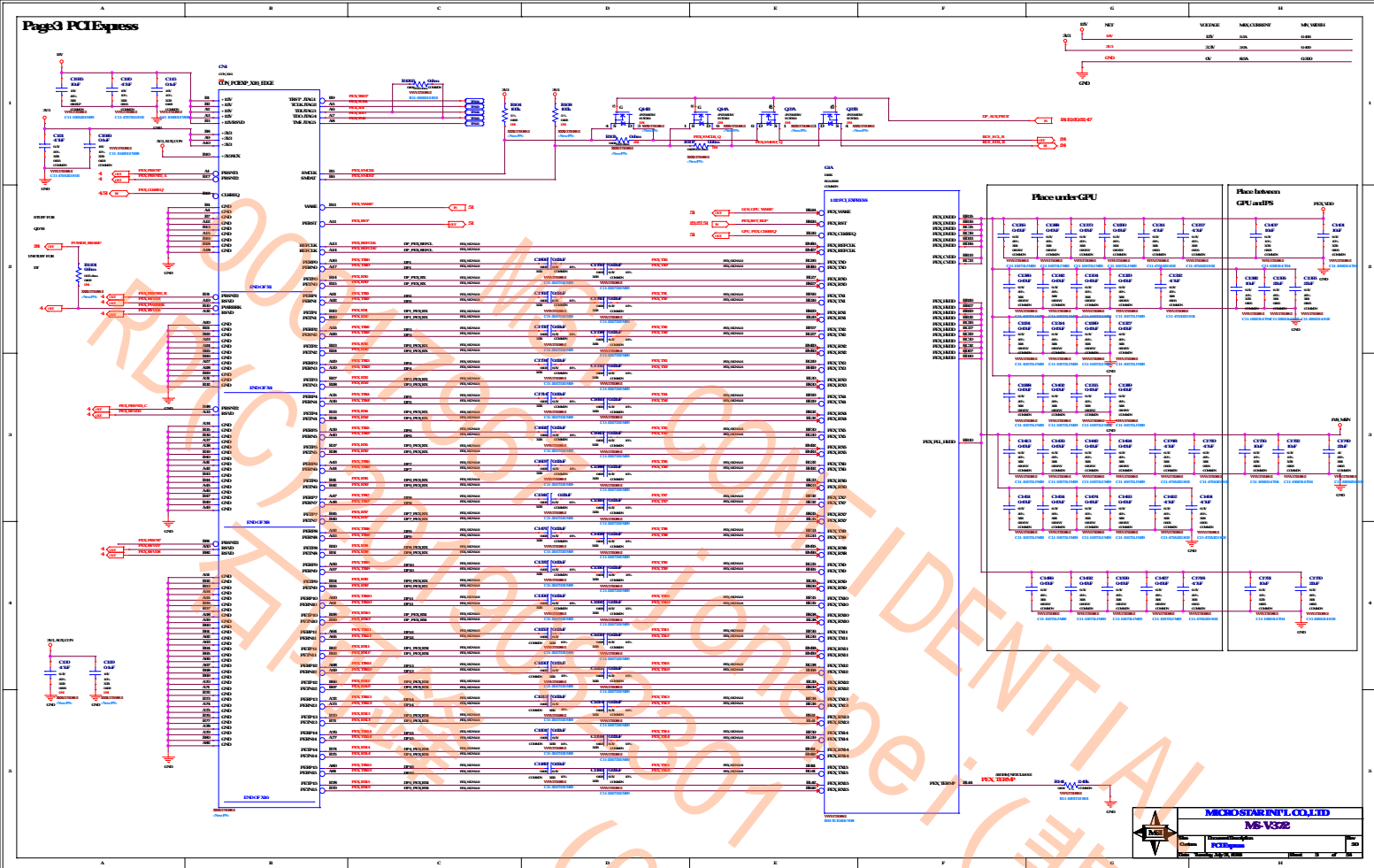
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V352:30 charge list
18 Charge J4fcirp1pt
19 Charge J3fcirp1pt
20 Remove IP co layout
21 Remove JTAG / Burned GPIO
32 Remove GBL PS_FWWD CONTROLLER OVR3
34 NVMD CONTROLLER charge to M22889A
35 DRMS charge to J4phms
36 DRMS charge to J4phms
37 Add NVMD Output CAP
41 Remove INPUT SWITCH Rail Balance
44 J8charge to Spin
Add Fuse F1-F3
Charge I2V input charge for input
45 Add High Updect for JS
Add Remove LED for Vin I2V updm
53 Add MCU H2855 for RGB LED

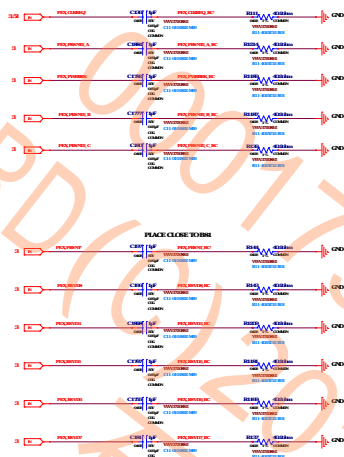
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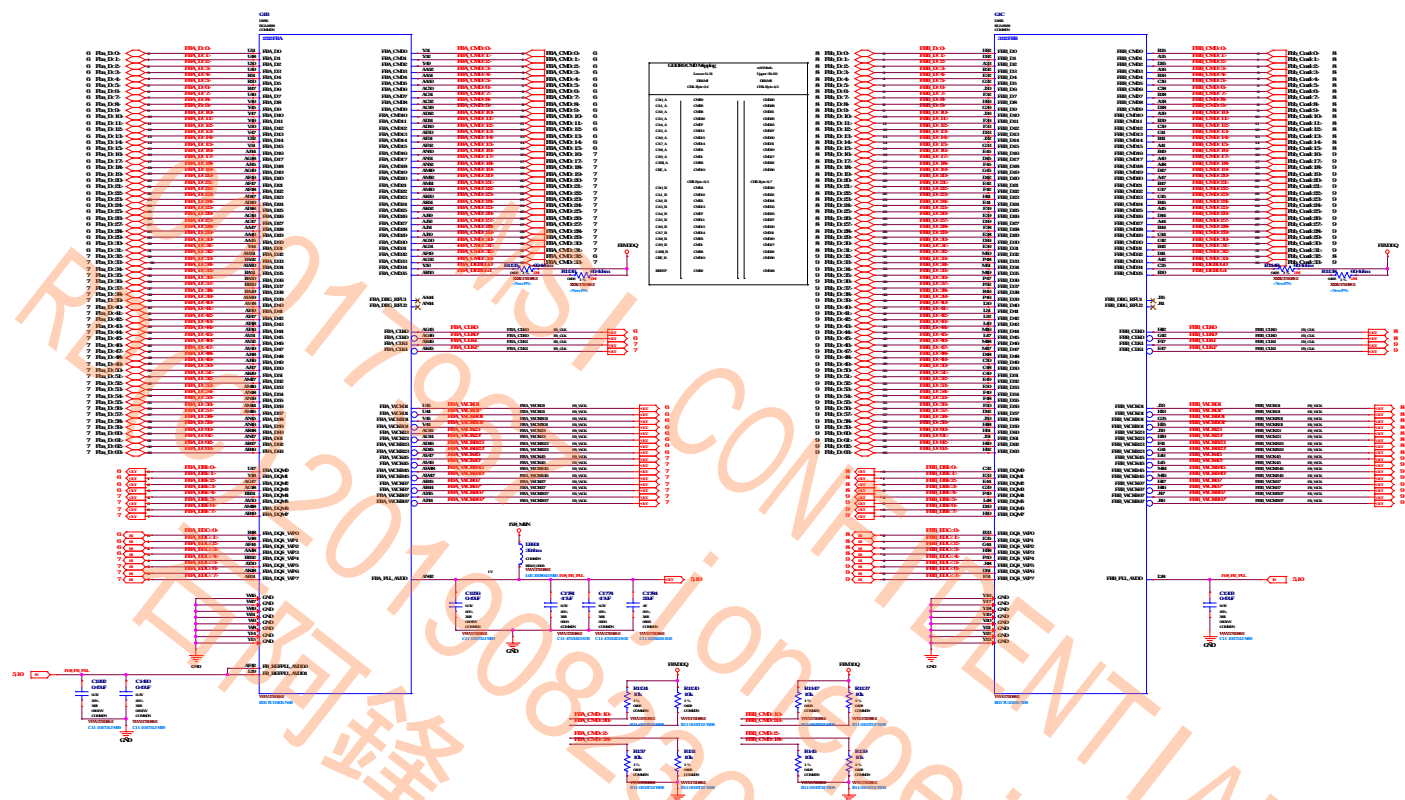


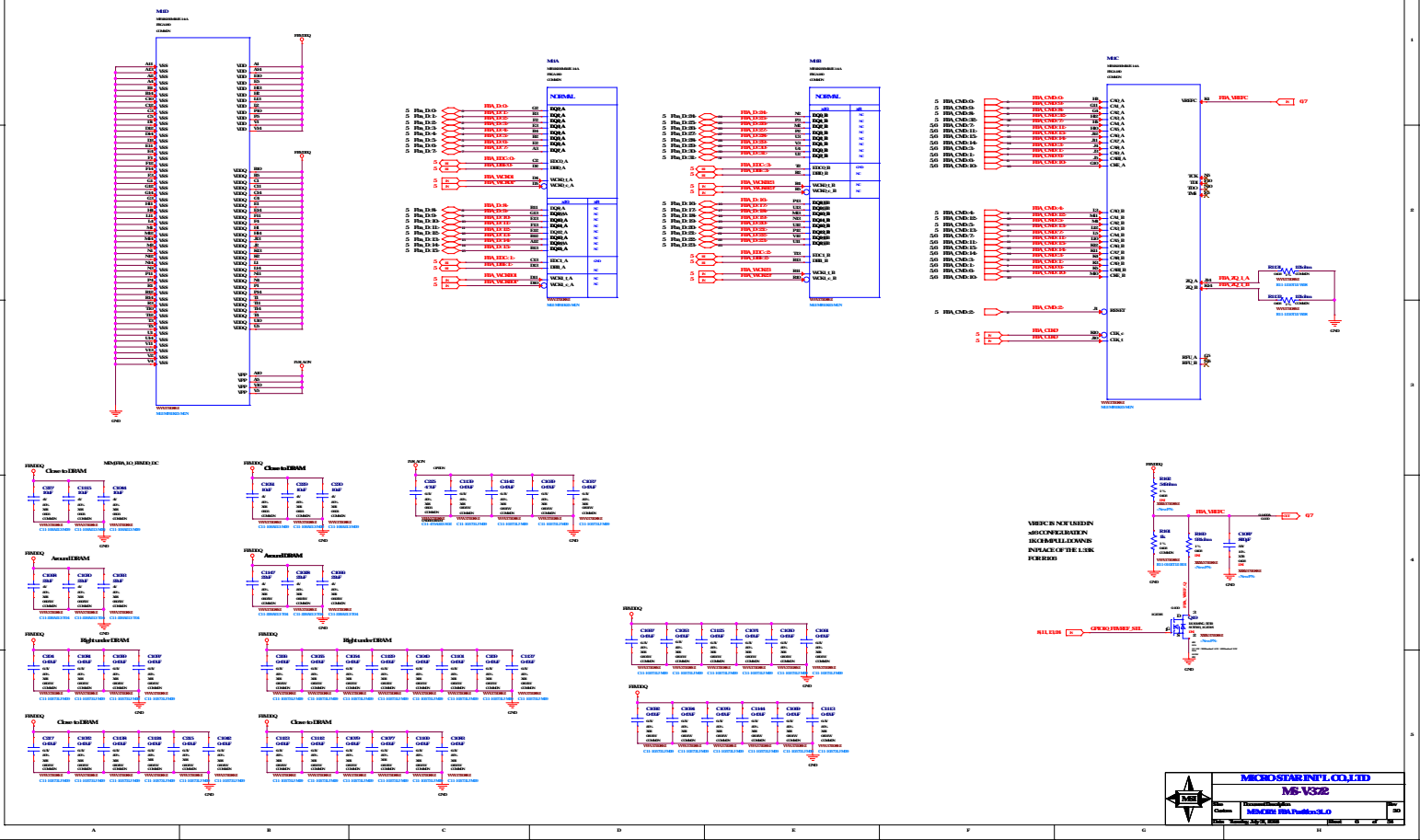


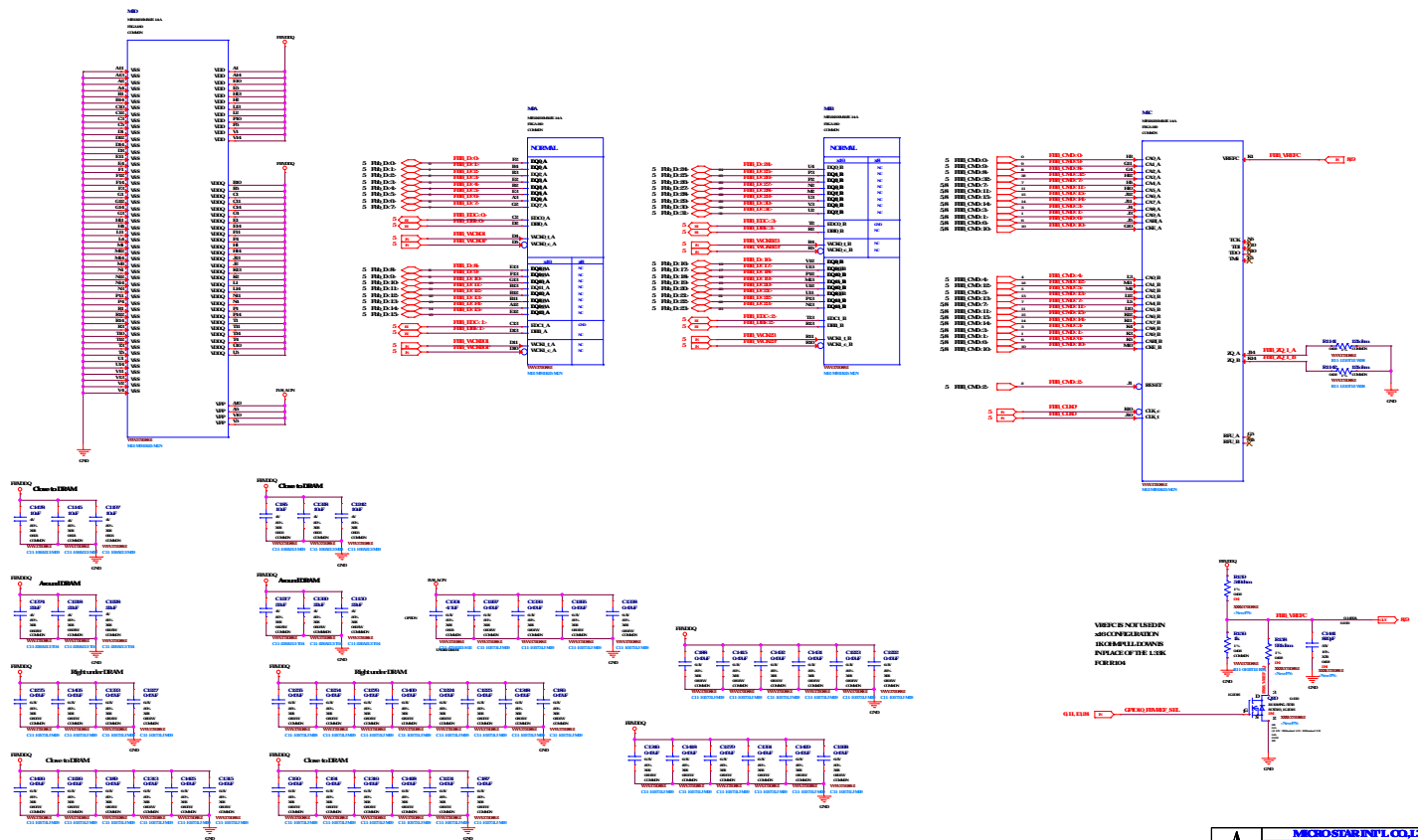


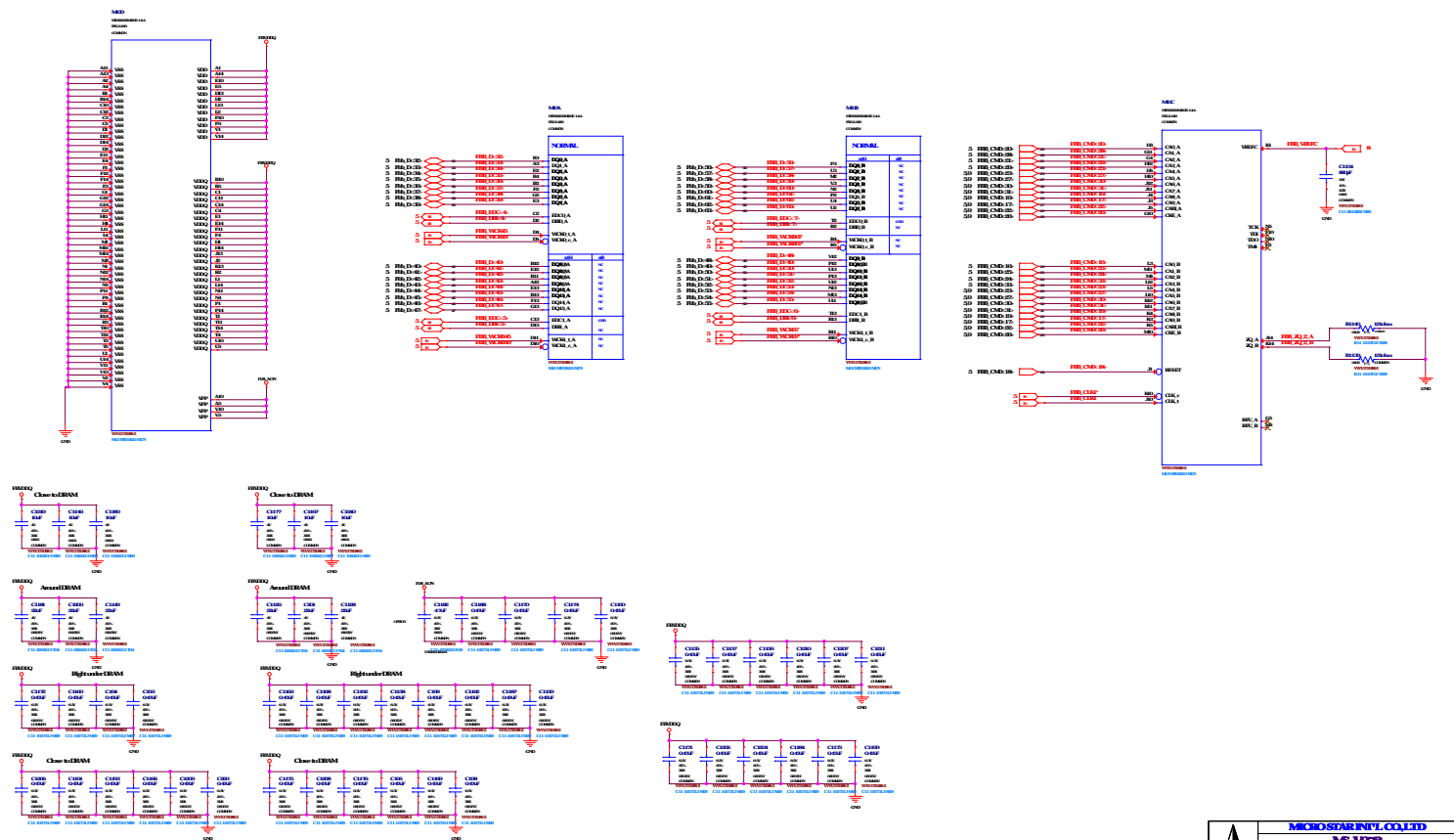
The image shows the top section of a document. On the left, there is a blue rectangular box with the text "Microstar" and "INTERNATIONAL" below it. To the right of this box is a small blue square with a white crosshair. Further right, there is a red square with a white crosshair. On the far right, there is a logo for "MICROSTAR INTERNATIONAL" with the text "MS-V332" below it. The logo features a stylized "M" and "S" inside a square frame.

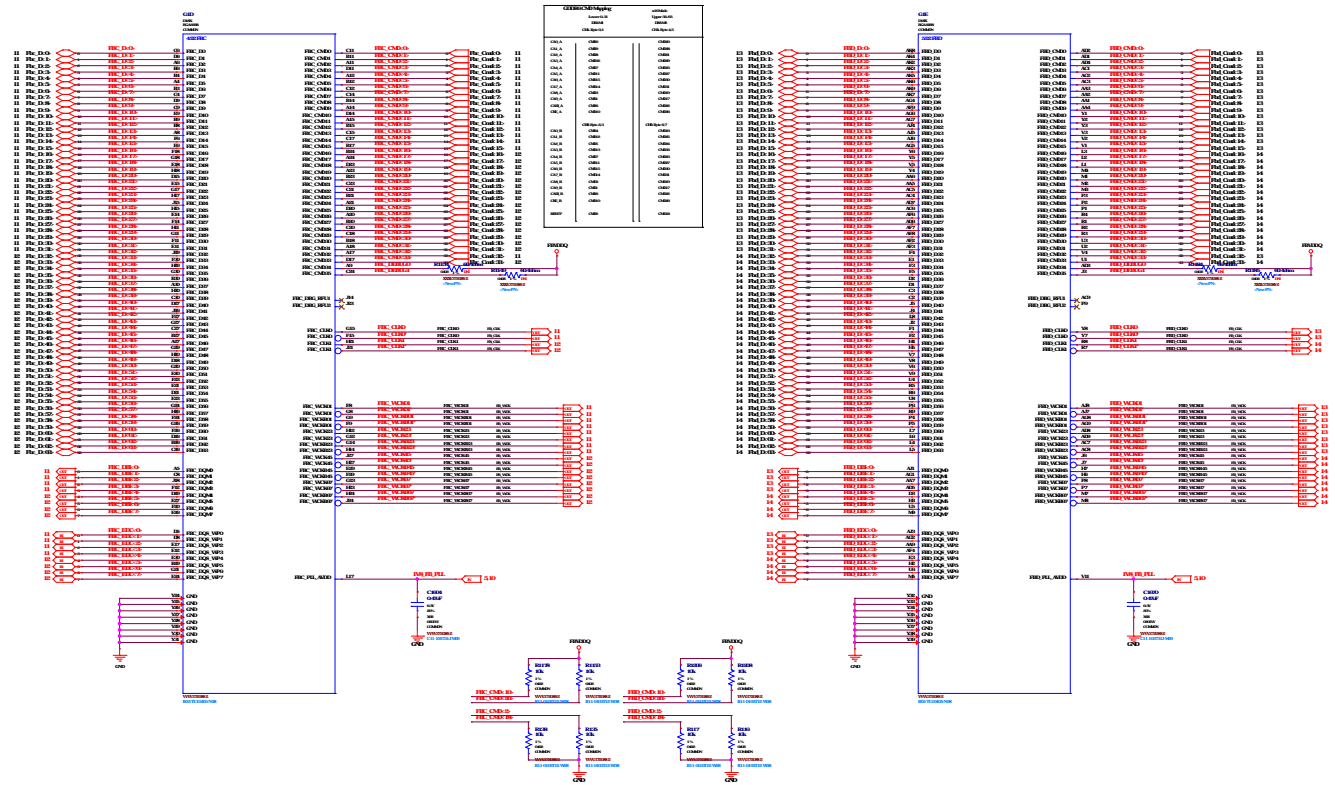


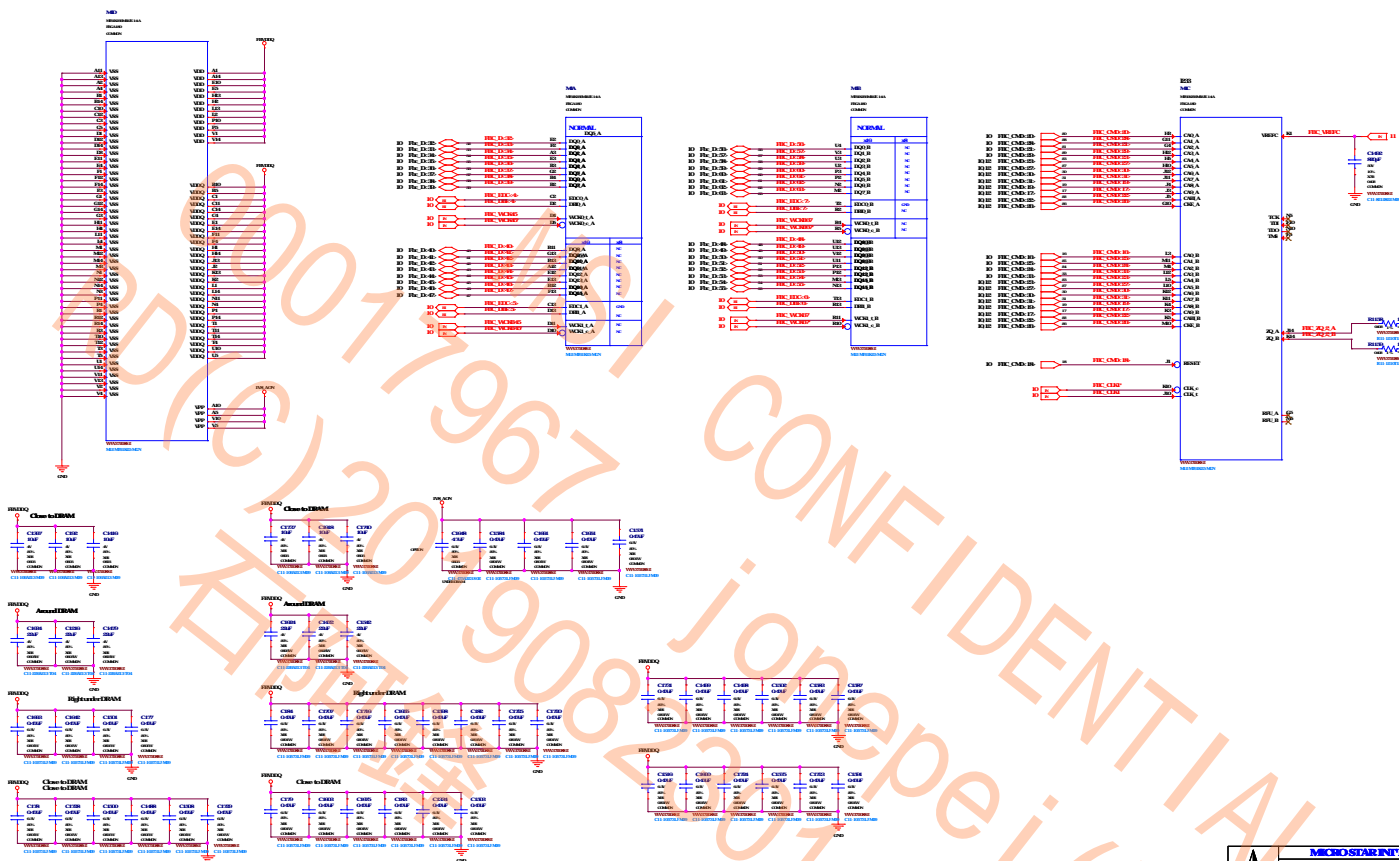


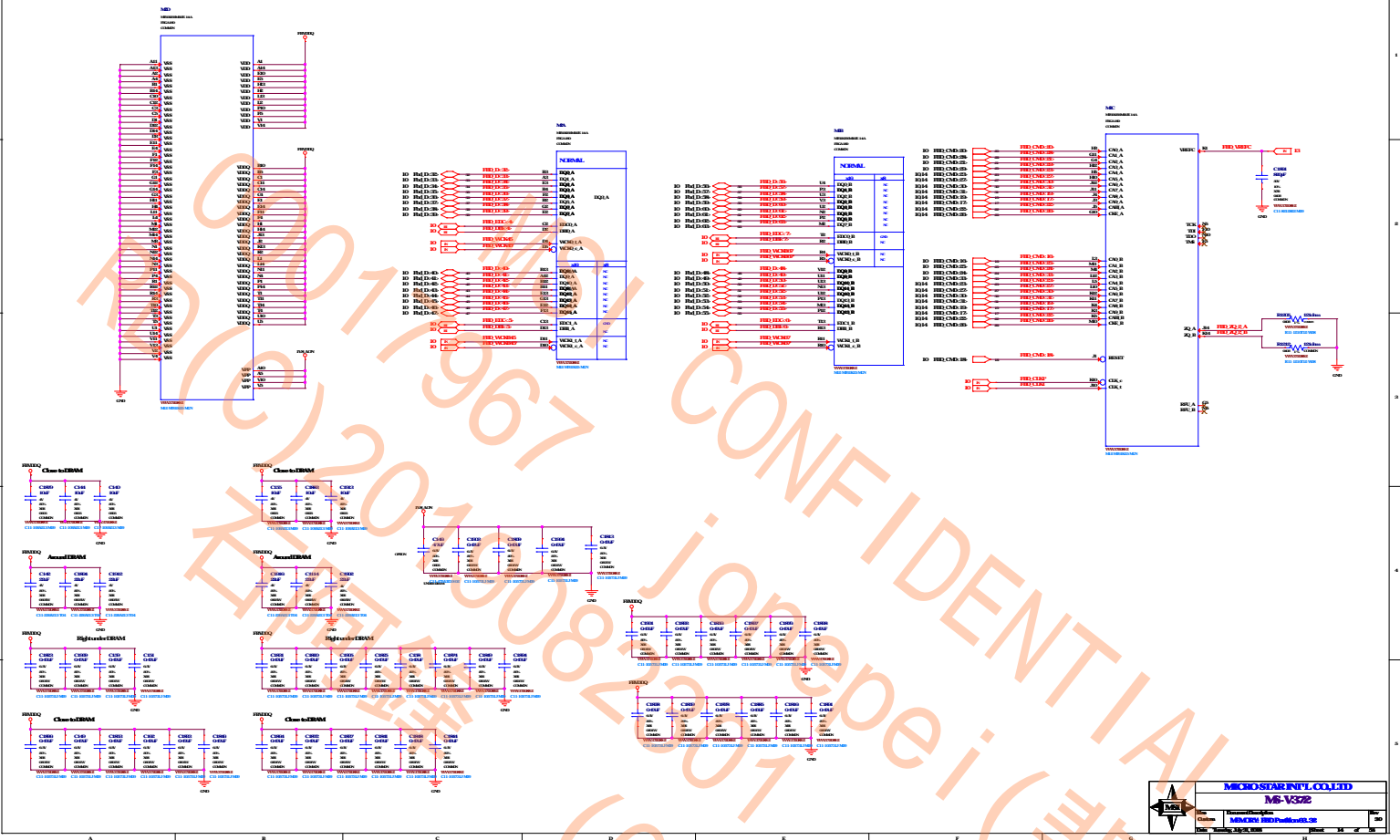




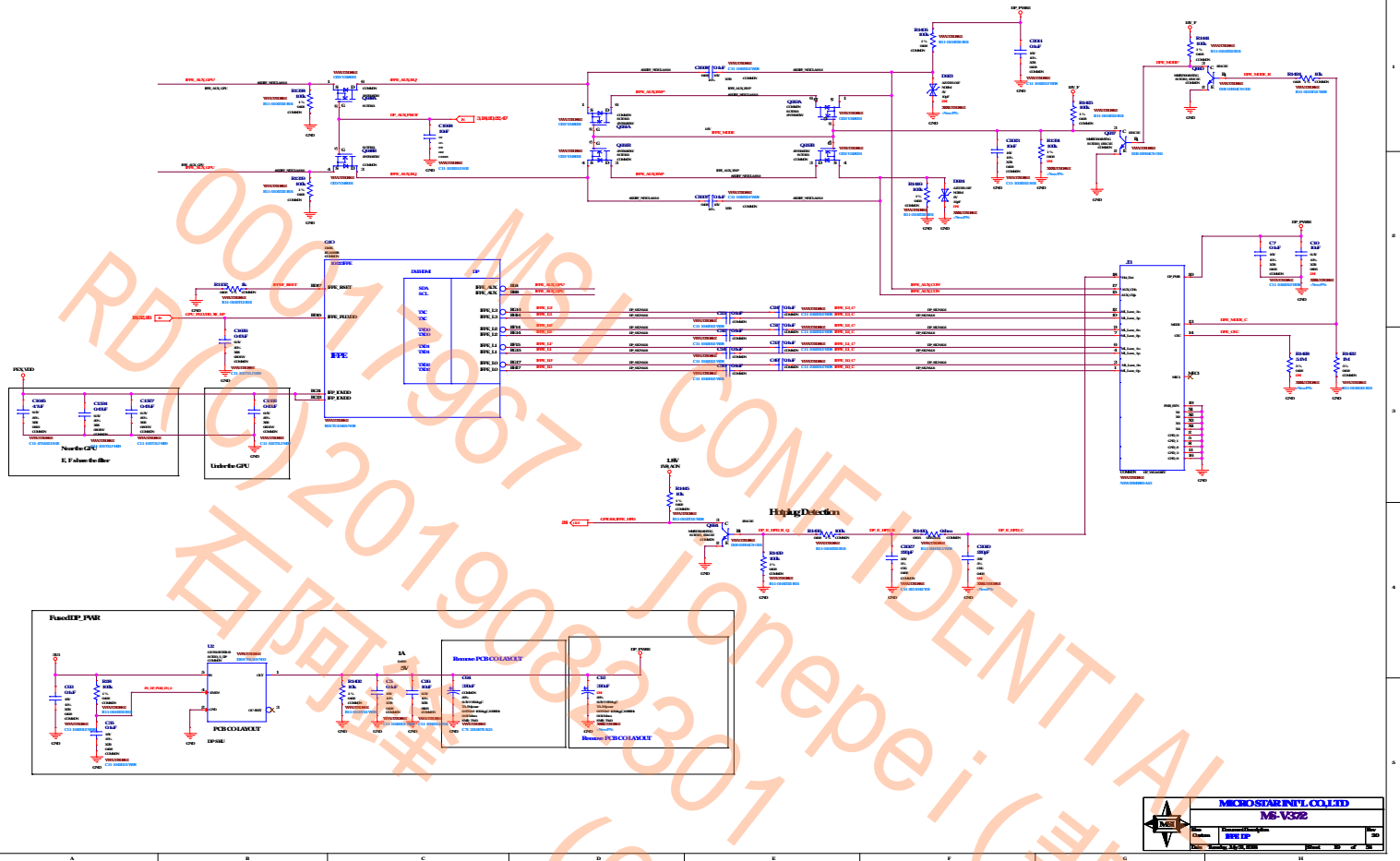


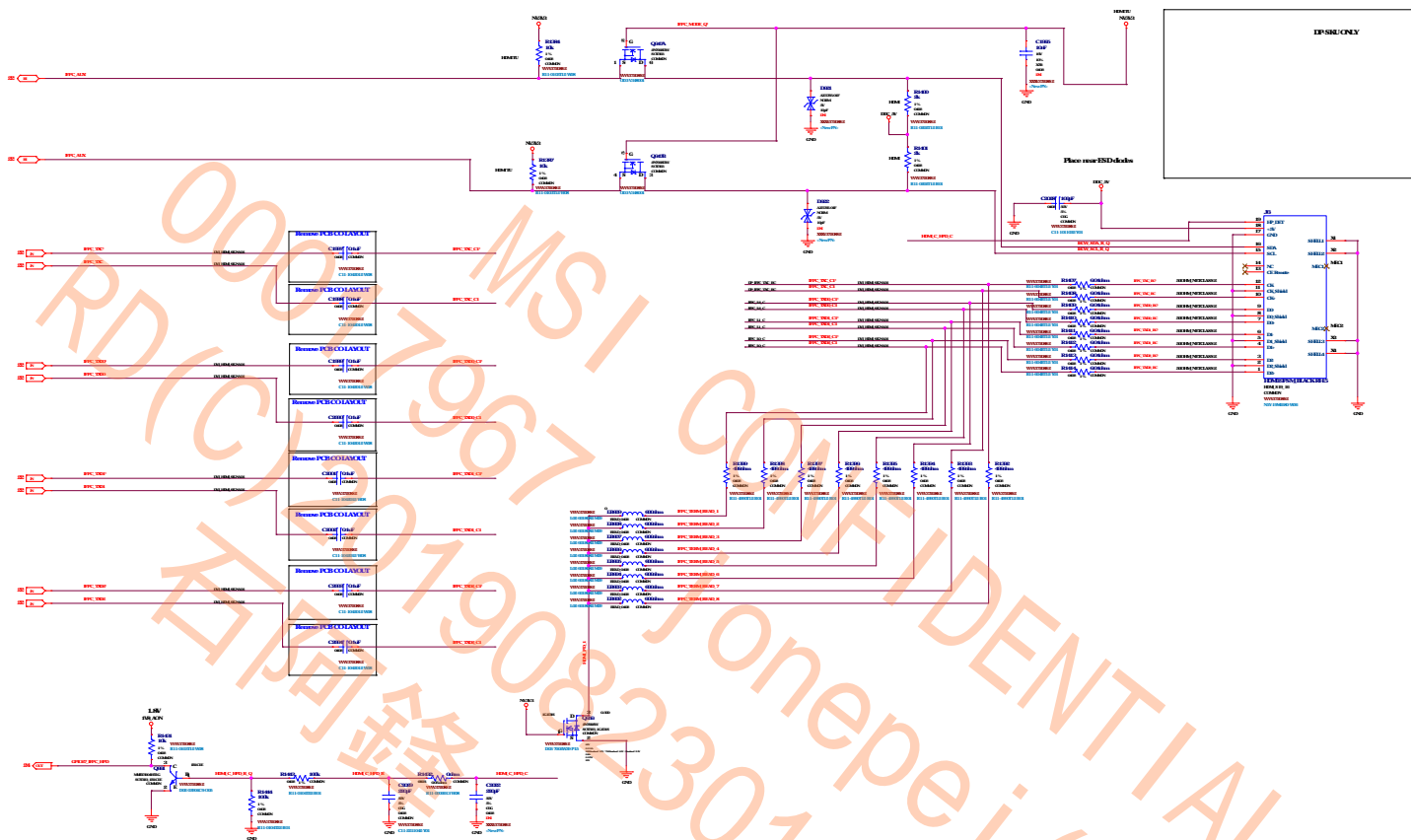


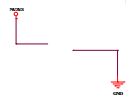
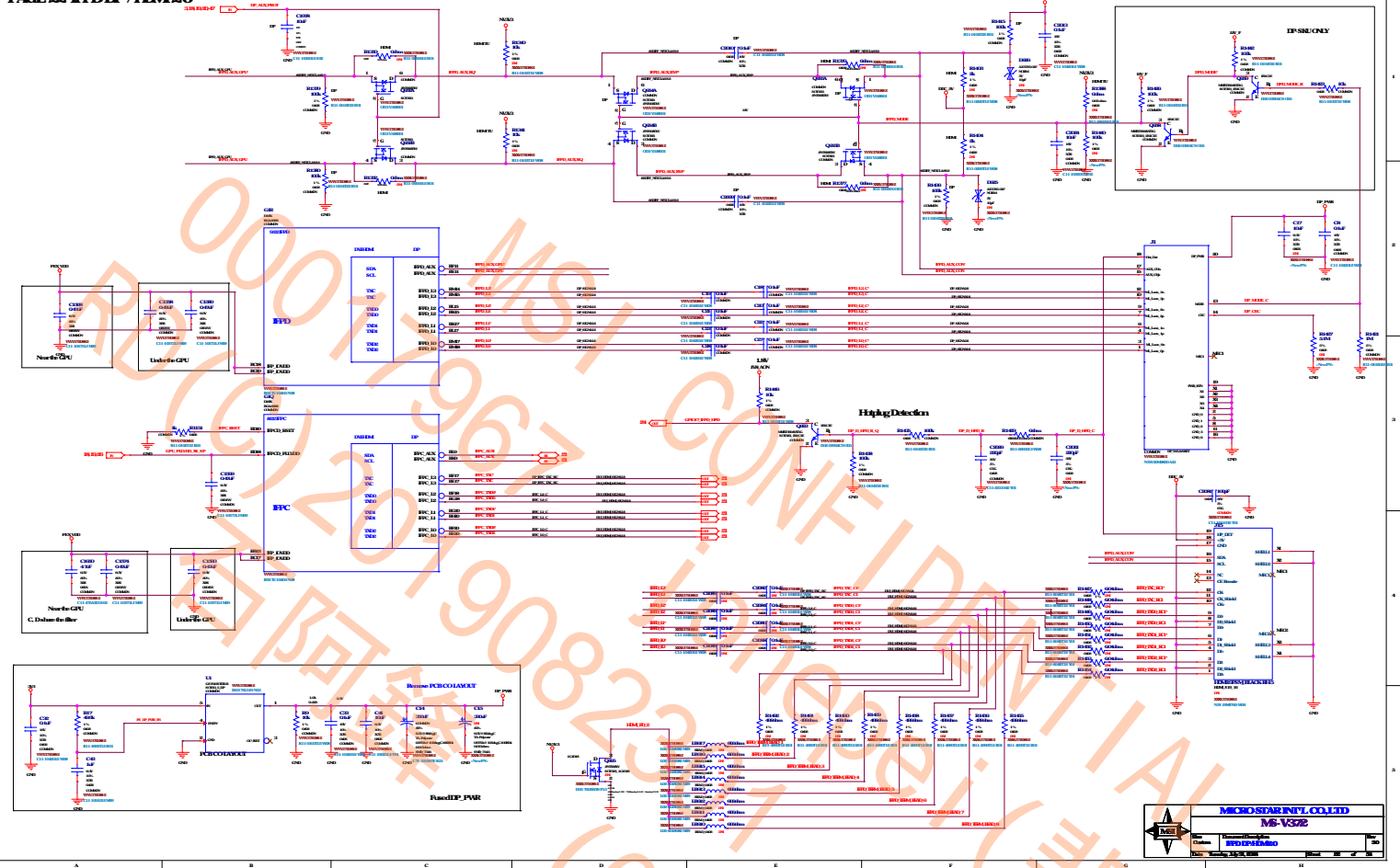


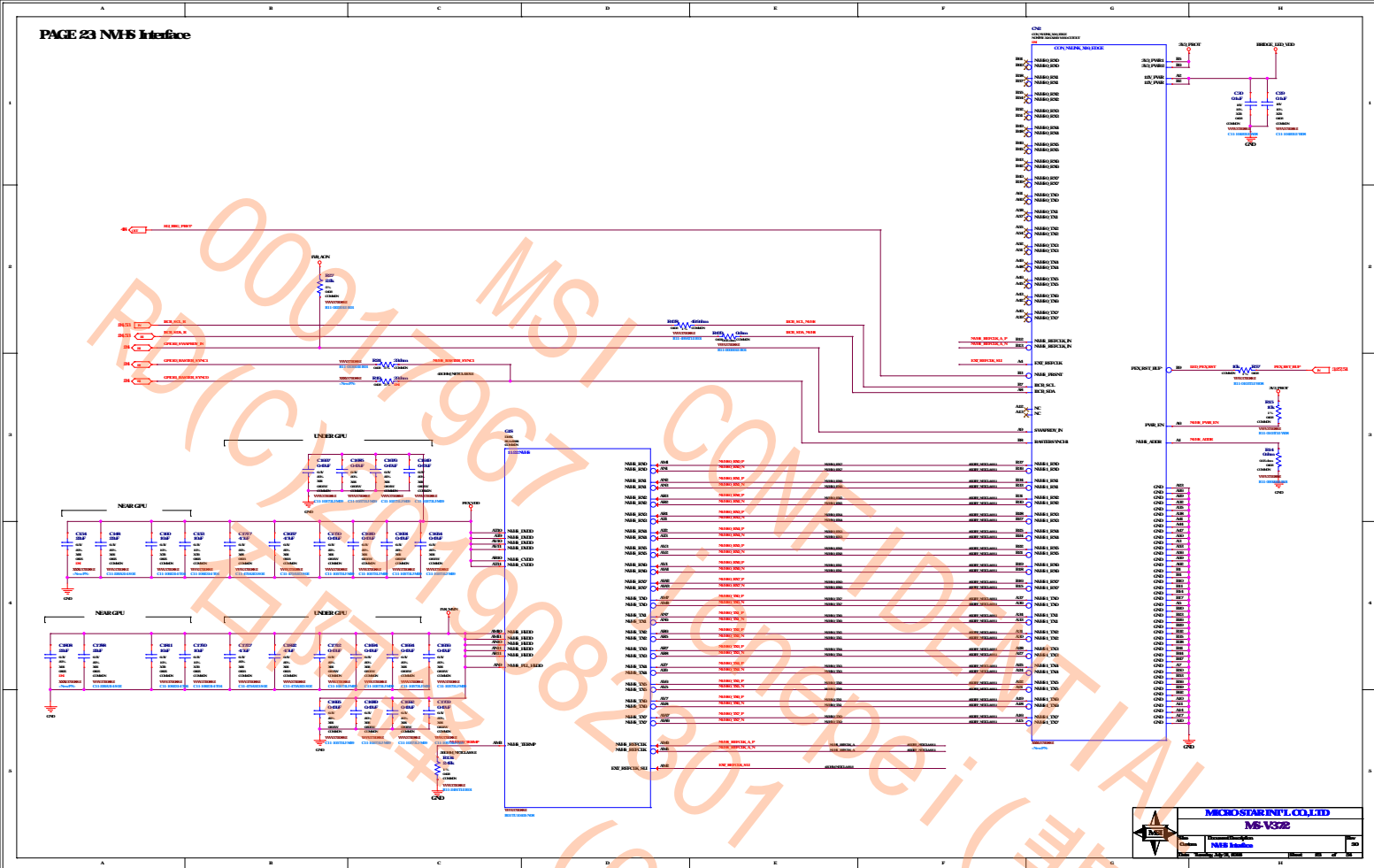












H/High/Hello LS/
M/Mid/Hello GS/
L/Low/Hello GV

STRAP5	STRAP1	STRAP0	RAMCFG40	RAMCFG ID	DEFAULT
L	L	L	0000	RAMCFG ID0	DEFAULT
L	L	H	0001	RAMCFG ID1	
L	H	L	0000	RAMCFG ID2	
L	H	H	0001	RAMCFG ID3	
H	H	L	0010	RAMCFG ID4	
H	H	H	0011	RAMCFG ID5	

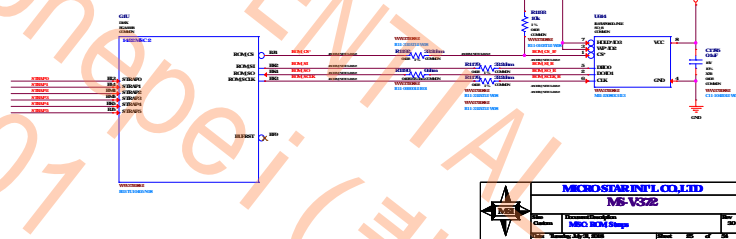
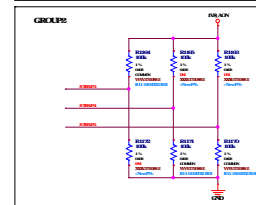
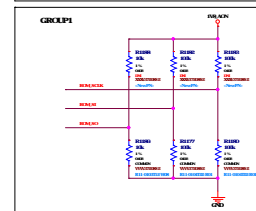
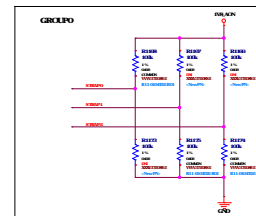
ROM50	ROM51	ROM52K	DUM@@PLS, CHERT	ENABLE/DISABLE	DEFAULT
L	L	L	X000	PS, CHERTENABLE	DEFAULT
L	L	M	X000	PS, CHERTDISABLE	

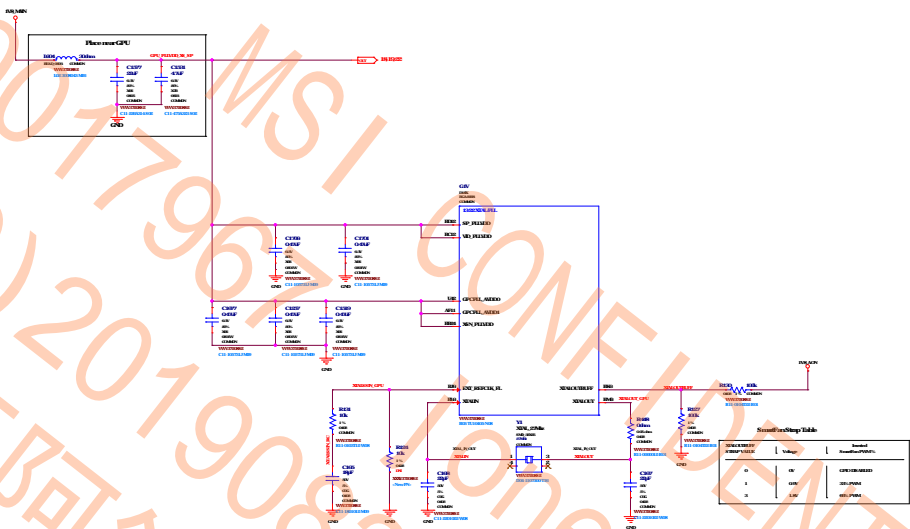
STRAP5	STRAP4	STRAP3	SMI/ALT_ADDR	DEVRSEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

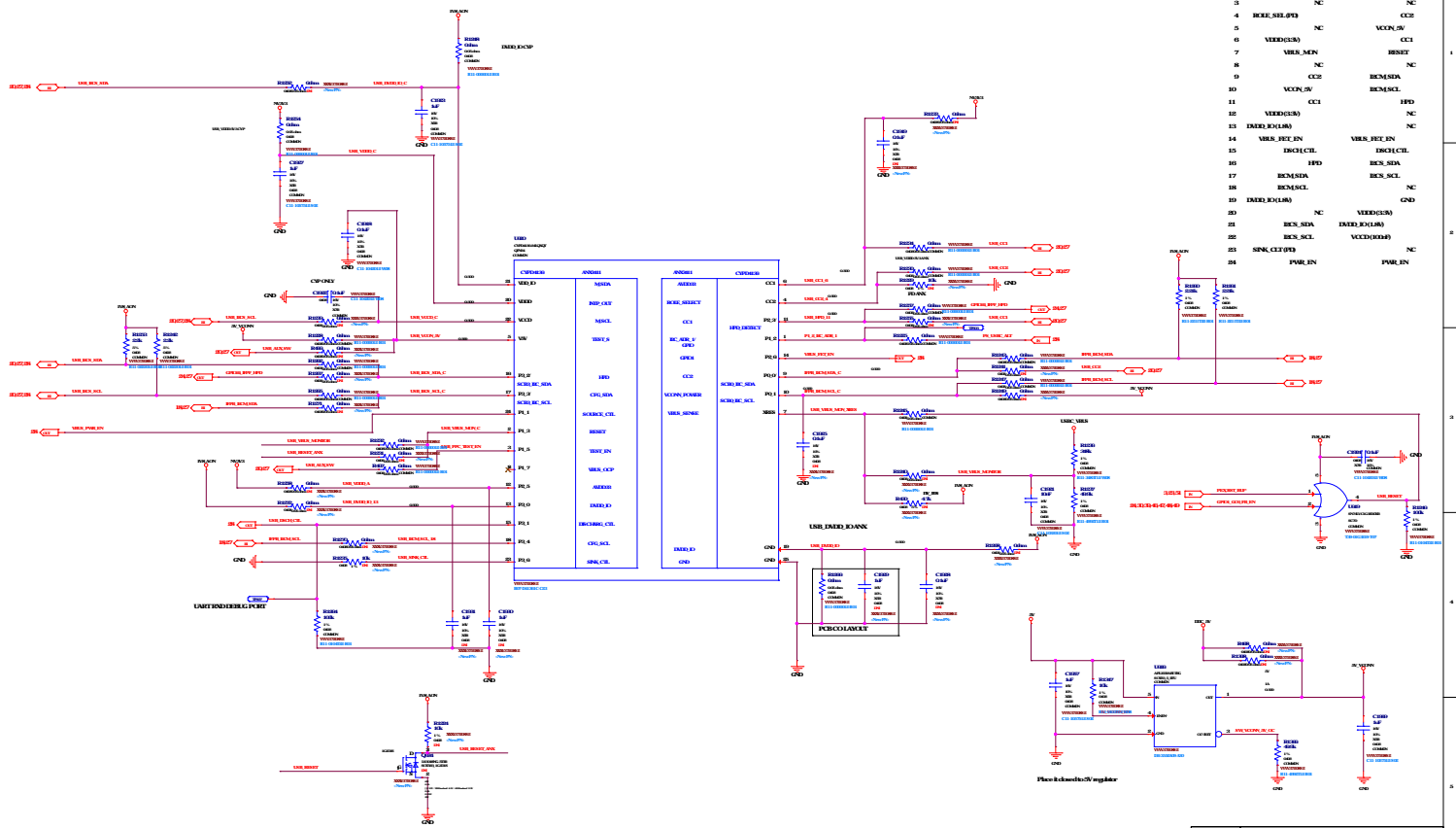
SMI/ALT_ADDRENABLE
SMI/ALT_ADDRDISABLE
DEVRSEL, BBRAND
DEVRSEL, CHERTSEL
PCIE_CFG LOWPOWER
PCIE_CFG HIGHPOWER
VGA_DEVICEENABLE
VGA_DEVICEDISABLE

Default

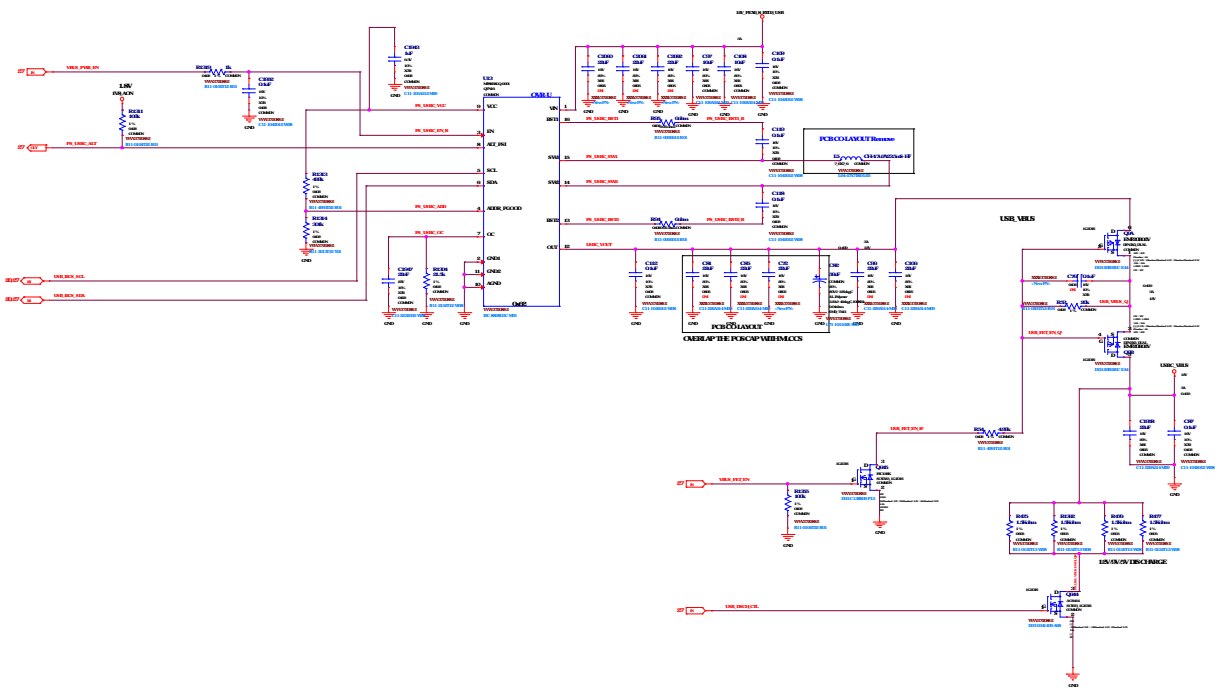
RAMCFG40	DENSITY	WIDTH	VENDOR
0000	8GB	32bit	Samsung
0001	8GB	32bit	Maxim
0000	8GB	32bit	Hynix
0000	8GB	32bit	Samsung
0011	8GB	32bit	Samsung

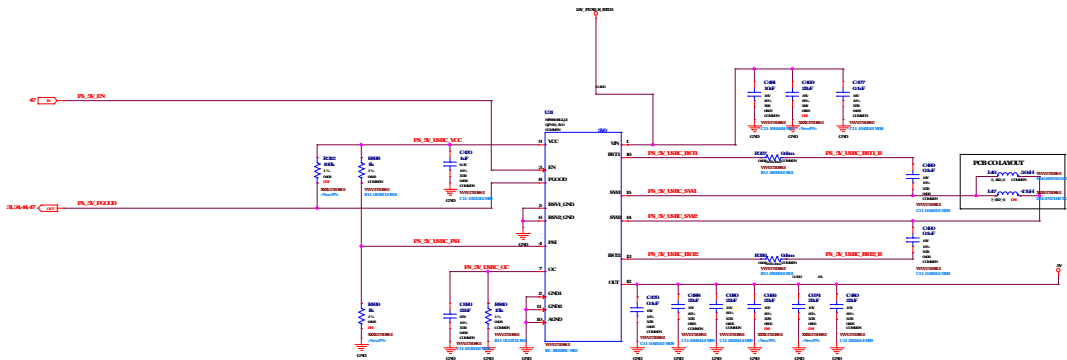




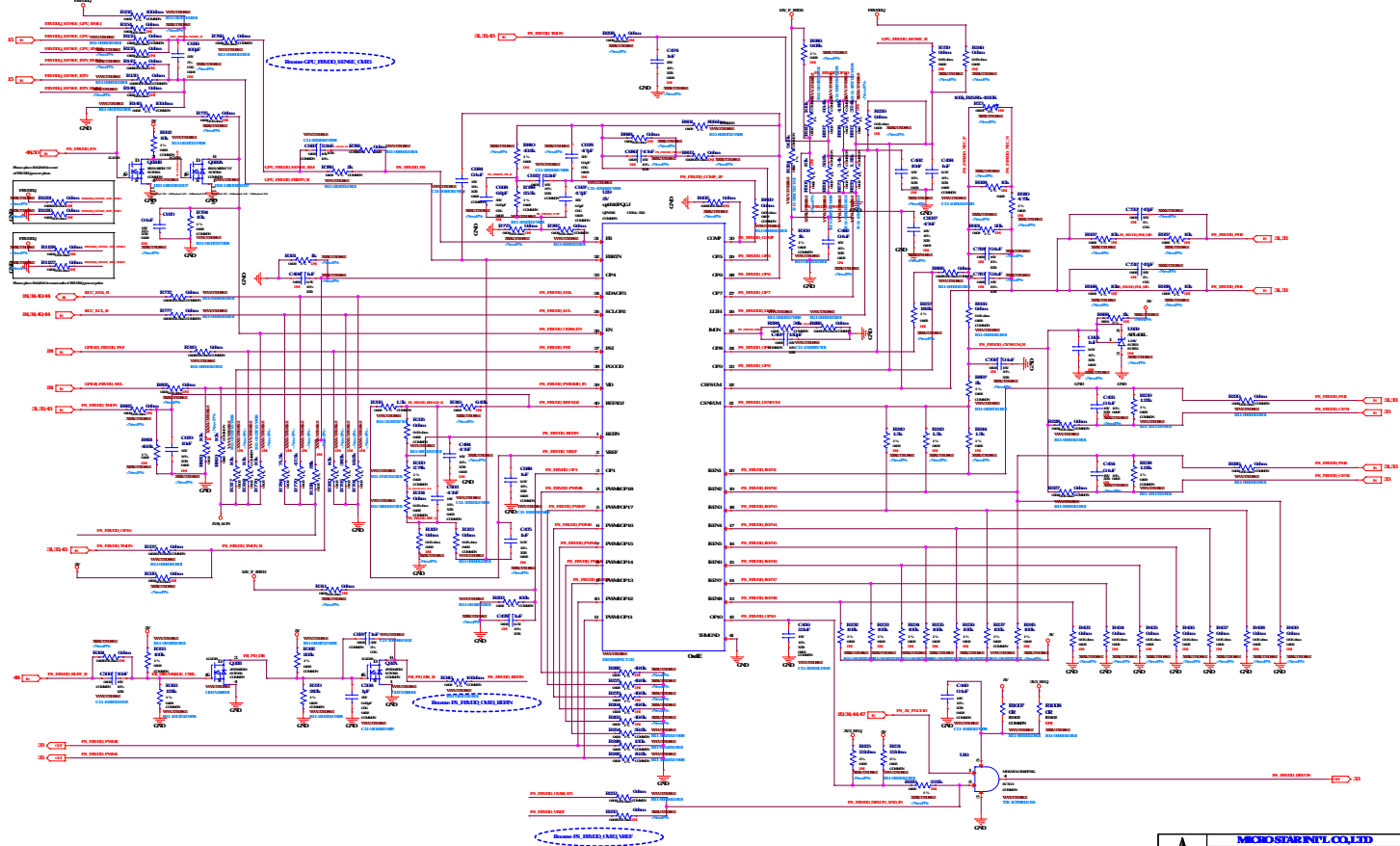


Pin	Annotation	Component
1	TP	TP
2	RESET	VR5A_MEN
3		NC
4	RESET	NC
5		VCC1
6	VR5A_MEN	VR5A_MEN
7	VR5A_MEN	RESET
8		NC
9	CC1	VR5A_MEN
10	VCC1	VR5A_MEN
11	CC1	VR5A_MEN
12	VR5A_MEN	VR5A_MEN
13	VR5A_MEN	VR5A_MEN
14	VR5A_MEN	VR5A_MEN
15	VR5A_MEN	VR5A_MEN
16	VR5A_MEN	VR5A_MEN
17	VR5A_MEN	VR5A_MEN
18	VR5A_MEN	VR5A_MEN
19	VR5A_MEN	VR5A_MEN
20	VR5A_MEN	VR5A_MEN
21	VR5A_MEN	VR5A_MEN
22	VR5A_MEN	VR5A_MEN
23	VR5A_MEN	VR5A_MEN
24	VR5A_MEN	VR5A_MEN





Remove U32 (R1738RGJ8)



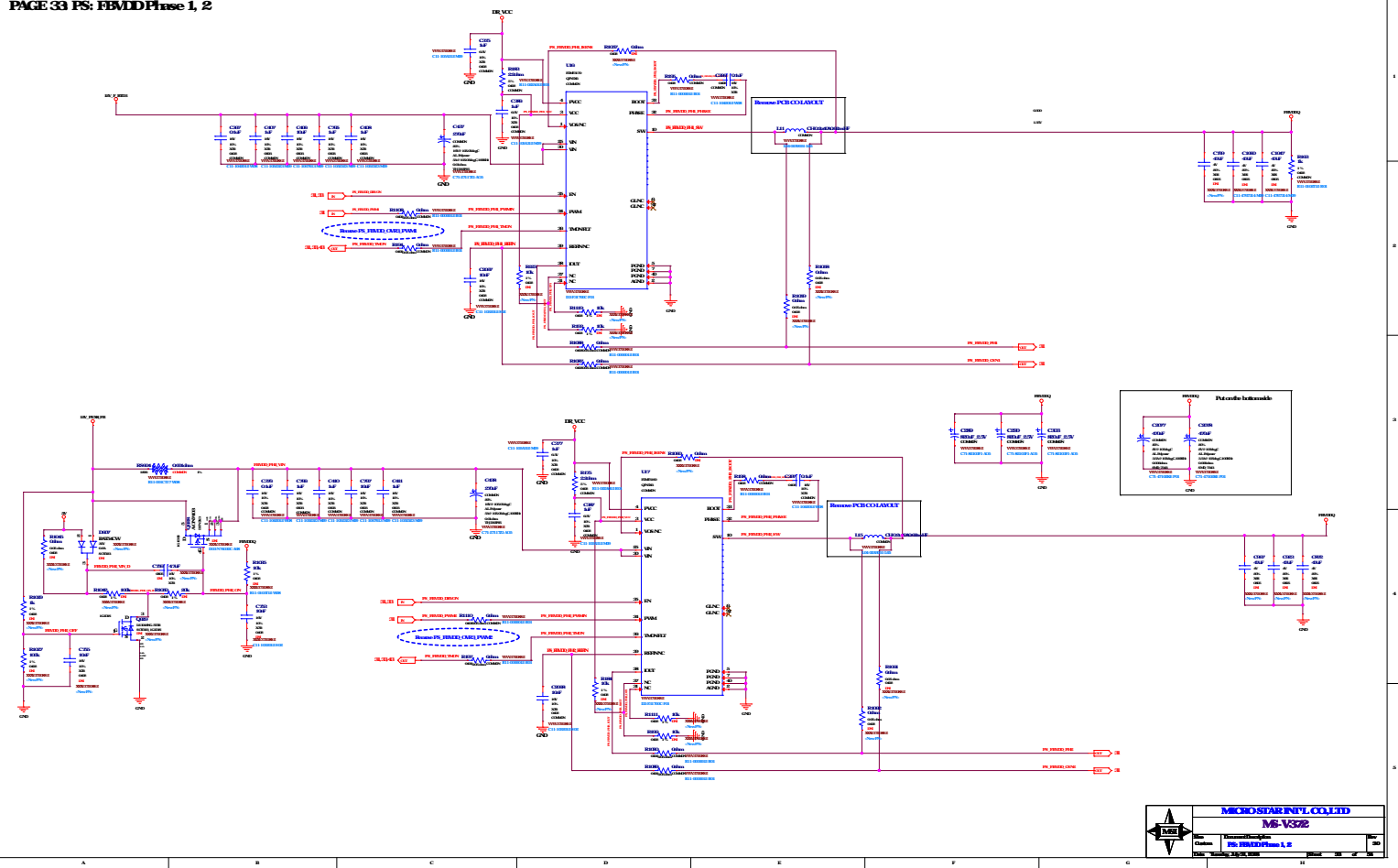


MICROSTAR INT'L CO., LTD.

MS-V3322

Revision: PS: FBVDD Controller-OMR3

Scale: 1:1000000



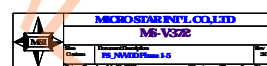
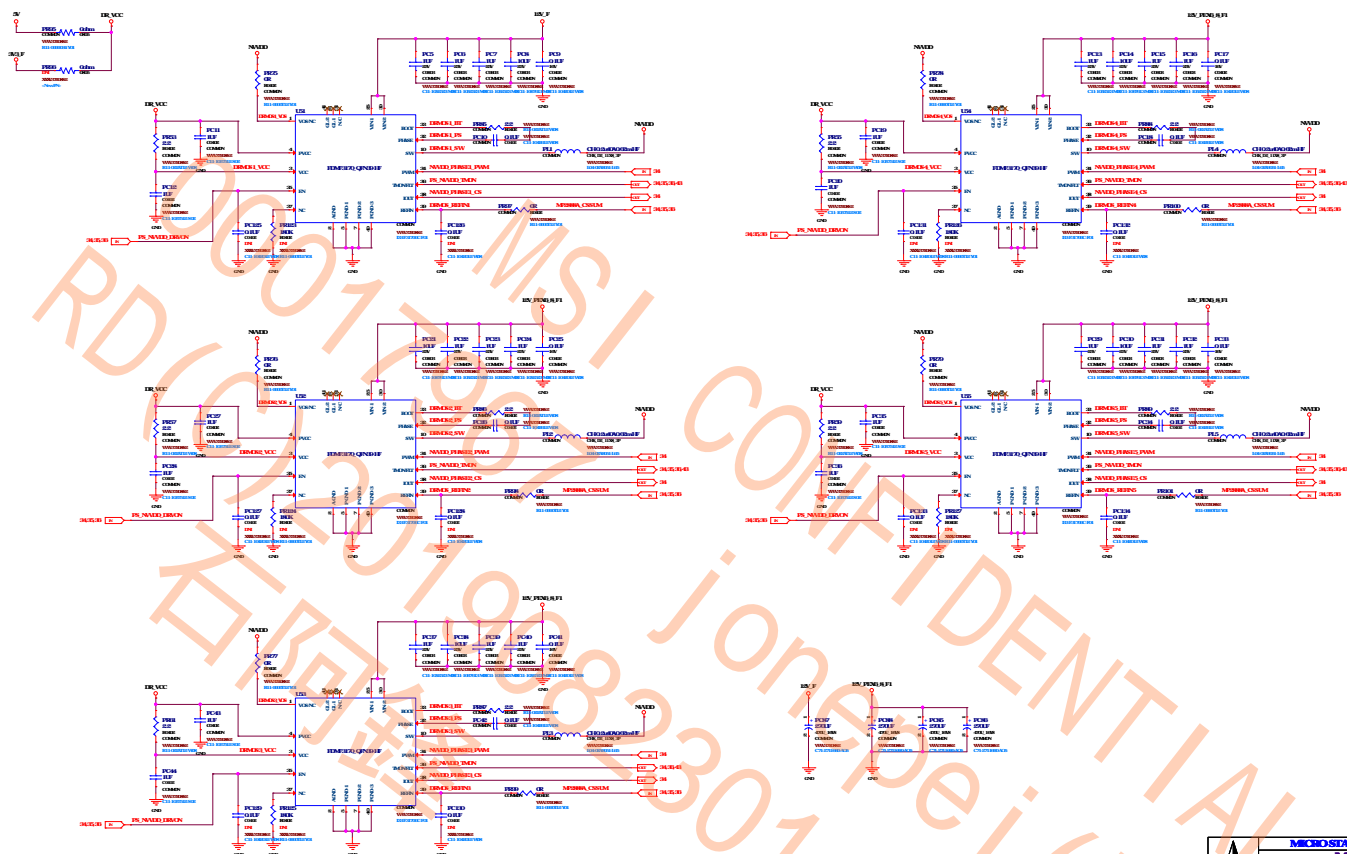
INType	BI
INValue	0%
INUnit	NO

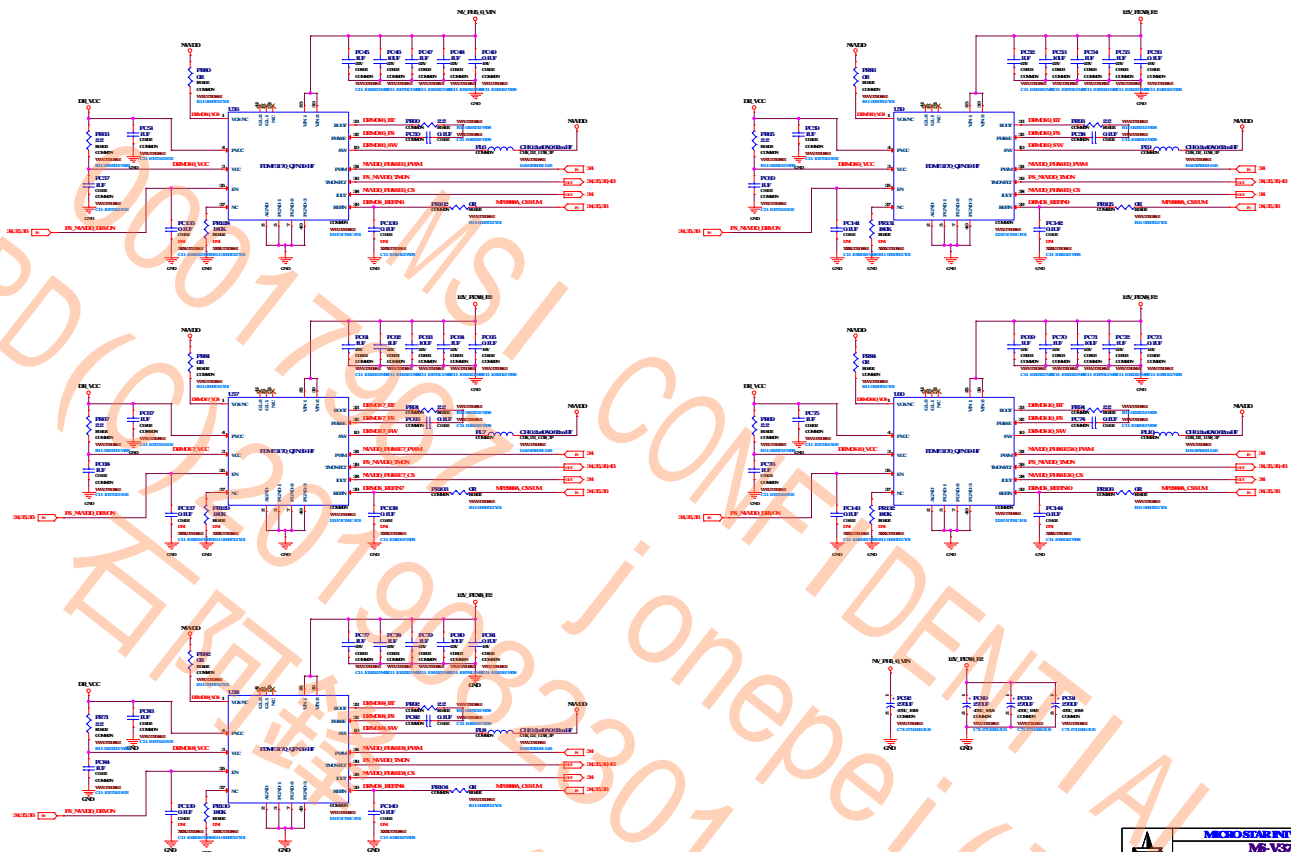
IN	Mode
High	HighFlowGnd
Low	AutoFlowMode
Low	LowFlowGnd

PARAM	Unit
High	MHz/Hz
Low	MHz/Hz

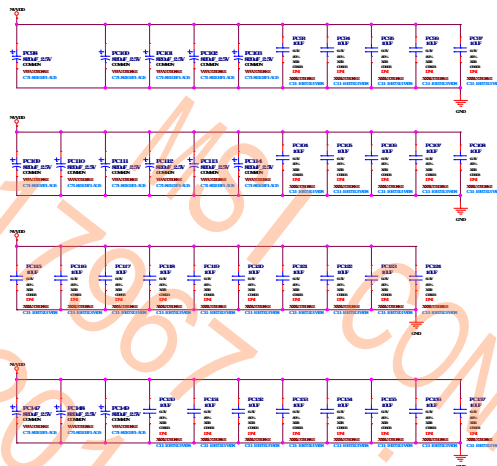
TEC	-NMID
InMin	30A
Modt	06s
Loadline	0uohm

PMBus Address	Setting Point(V)	K _{upper} (KΩ) 3%	K _{lower} (KΩ) 3%
213h	0.031	3.32	0.059
222h	0.057	3.32	0.11
233h	0.084	3.32	0.162
245h	0.116	3.32	0.226
256h	0.156	3.32	0.316
268h	0.205	3.32	0.42
277h	0.266	3.32	0.578
283h	0.340	3.32	0.768
298h	0.430	3.32	1.06
2Ah	0.540	3.32	1.43
2Ch	0.675	3.32	2
26fh	0.844	3.32	2.94
28fh	1.048	3.32	4.64
29fh	1.351	3.32	6.4
2Afh	1.591	3.32	8.1
2Bfh	1.896	3.32	9.8





NVDD Output CAP



MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2019082301 RMA工程課
石阿鋒 (00068760)

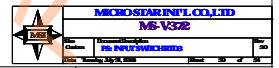
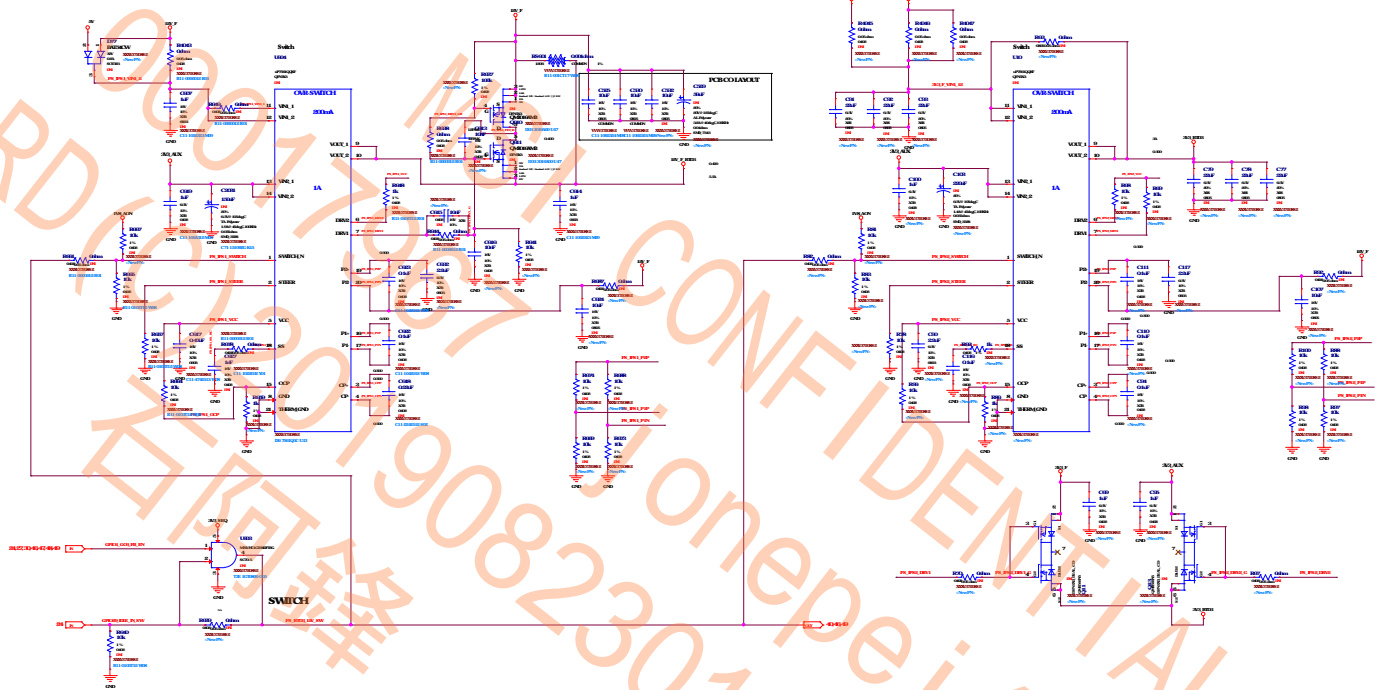


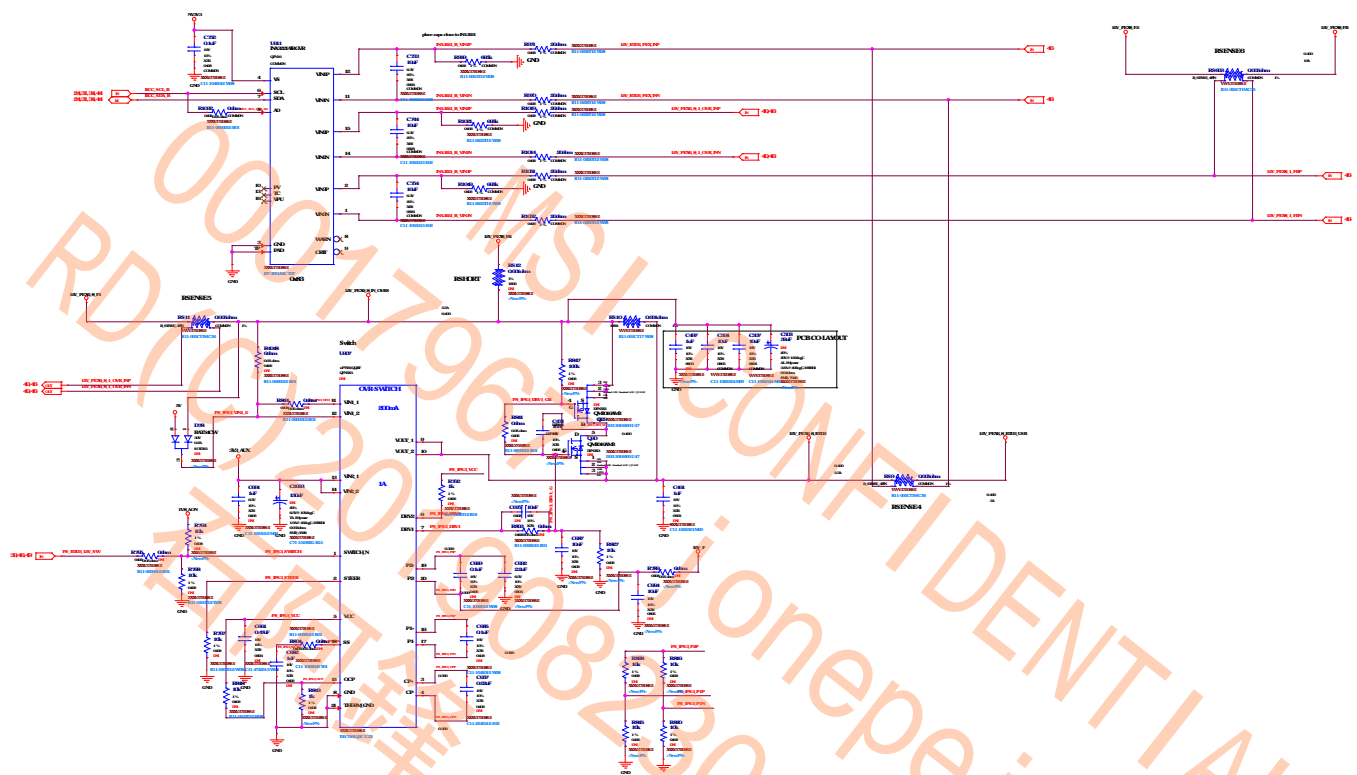
AND GATE LOGIC FOR P BOARD

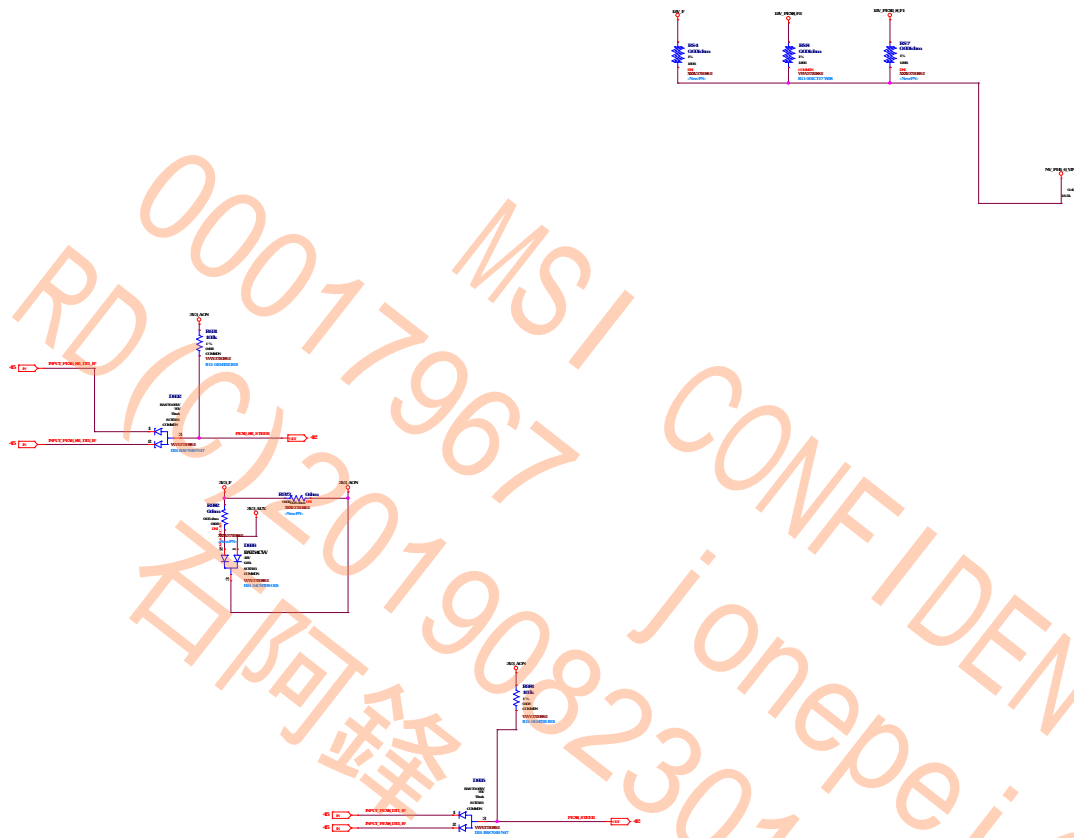
GPEN	GPEN0	SWITCH	VCUT
0	0	0	IN_F
0	1	0	IN_F
1	0	0	IN_F
1	1	1	IN_A

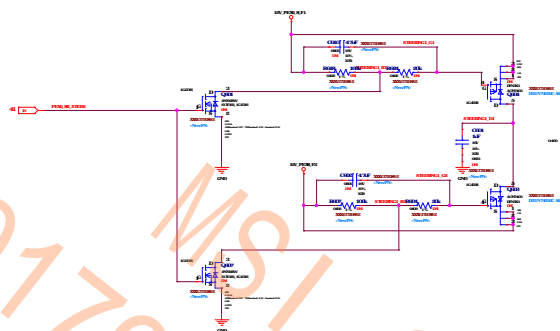
AND GATE LOGIC FOR P BOARD

GPEN	GPEN0	SWITCH	VCUT
0	0	0	IN_C
0	1	0	IN_C
1	0	0	IN_C
1	1	1	IN_A

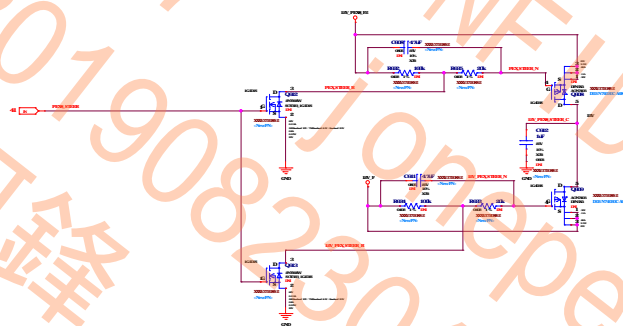


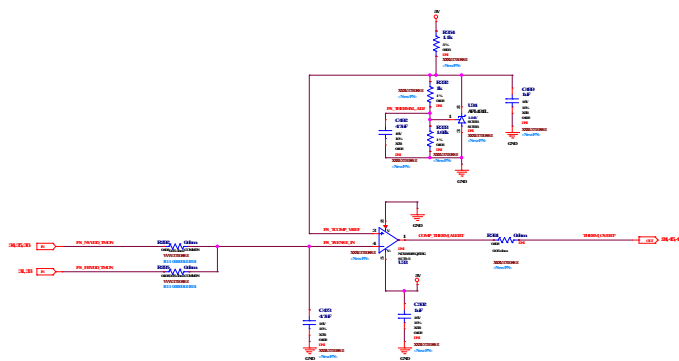


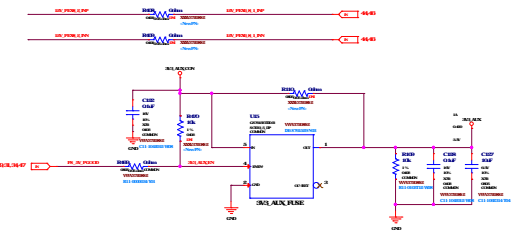
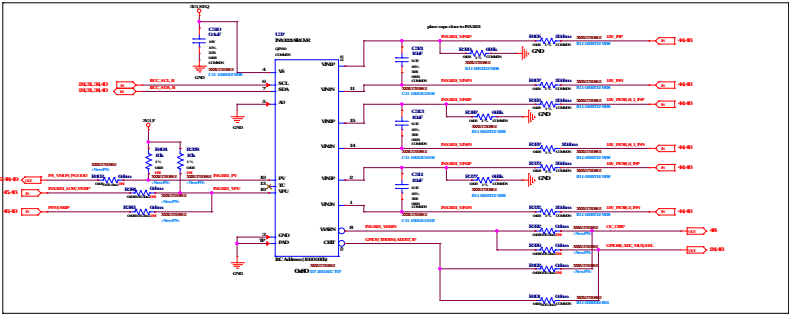




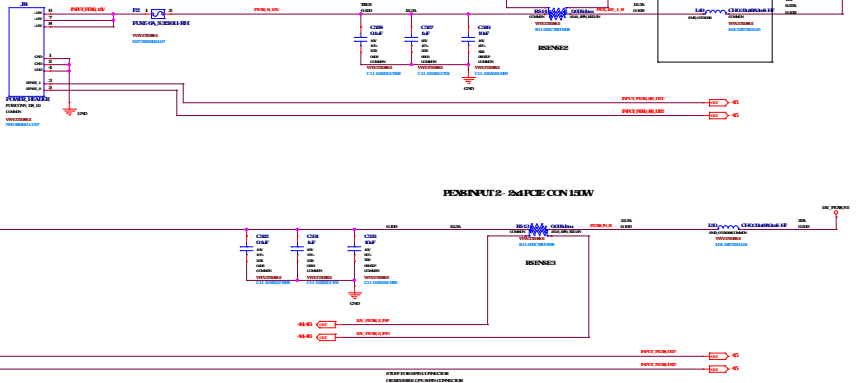
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX SPIN INPUT AREA





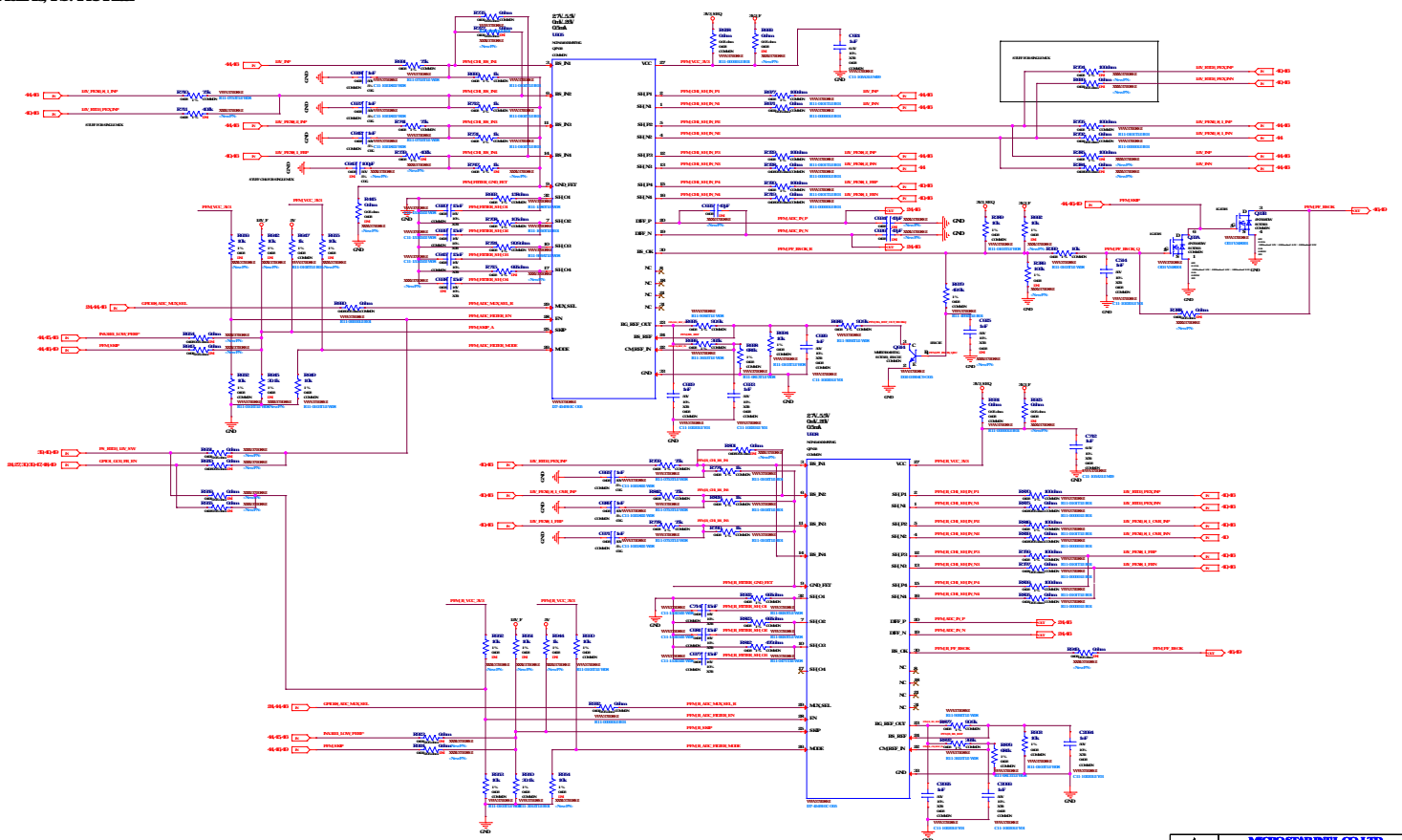


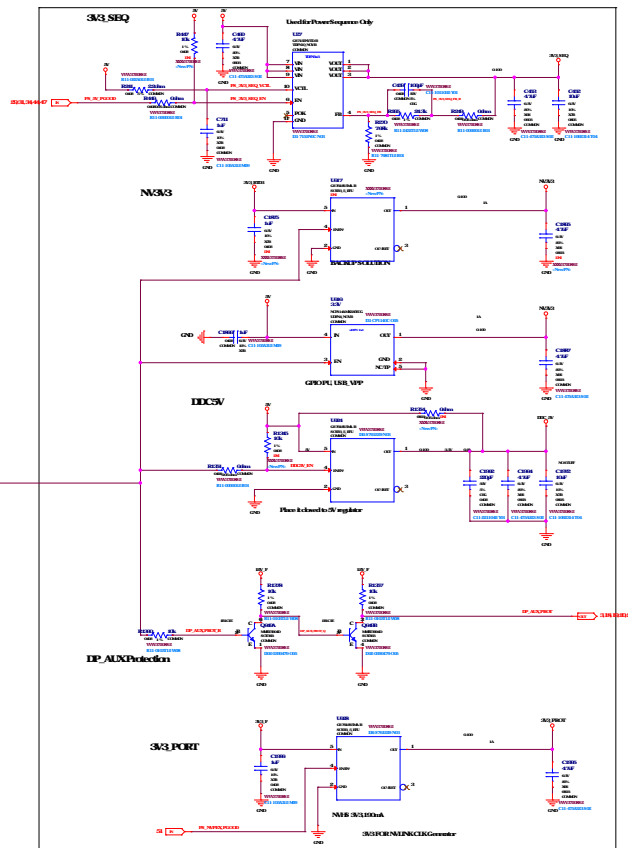
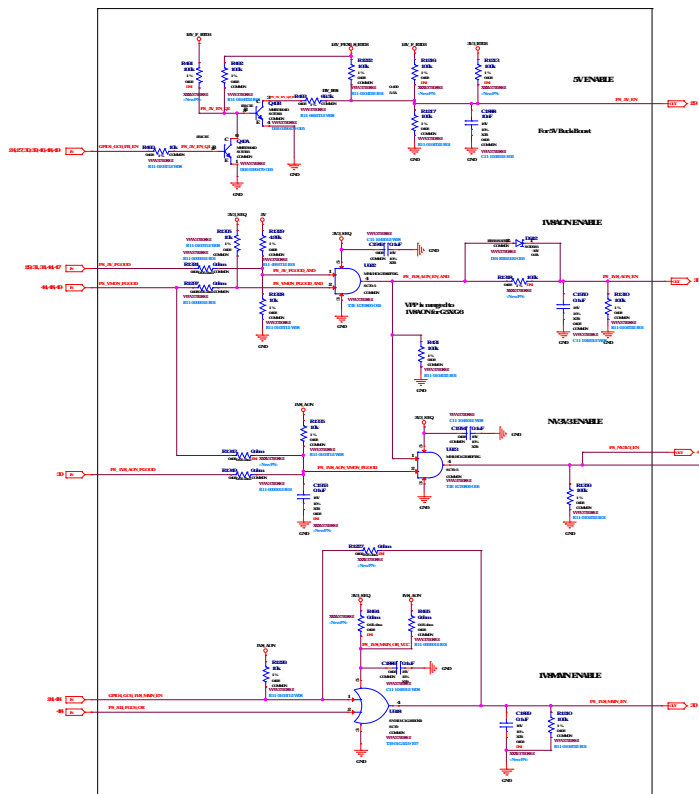
PS: INPUT 1 - 250W



PS: INPUT 2 - 250W







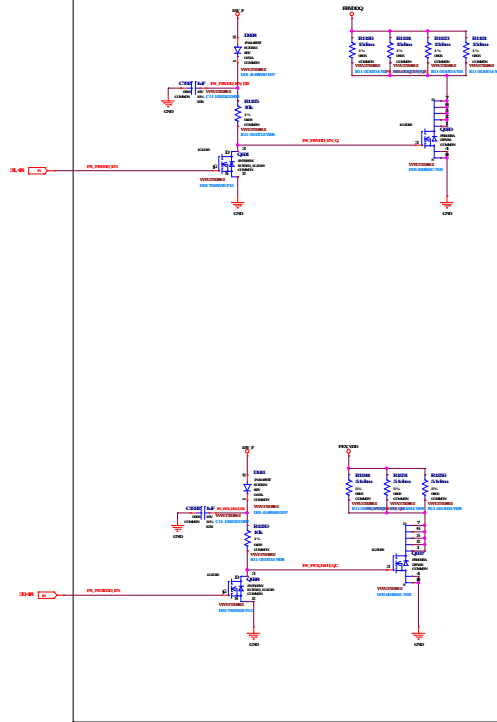


PowerSupply
NA3221-3V3_SEQ
Pre_Filter(ADC_MUX)-3V3(PEN)

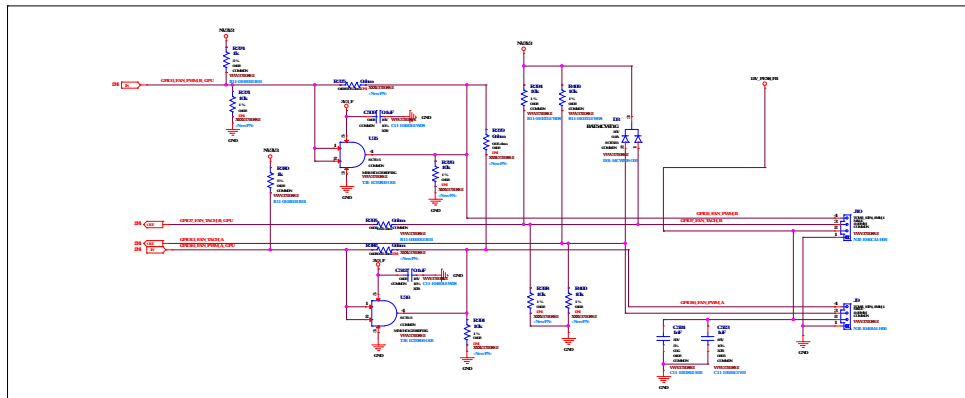
Dual Pre-Filter cases
Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

Signal	Direction	Function
CLK	INPUT	Source for 200 MHzs from CPU, gskkldio@pc
ENET0	INPUT	Source for 100 MHzs from CPU, gskkldio@pc
PC_VDDP1,PGOOD	COMBIN	Wakeup source for CPU Stand by, reset@pc
GPIO18_IN	INPUT	Indicates the BTTGDS000 module has been initialized, VDDP1,PGOOD
PC_FW_DONE	INPUT	Reset@PCVDDP1 or the BttGDS000
PC_FW_ERROR	INPUT	Reset@PCVDDP1 or the BttGDS000_CK0
PC_RESET0,PC_FW	INPUT	GPIO18,ENET0,EE,PC_FW





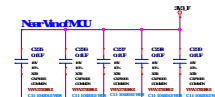
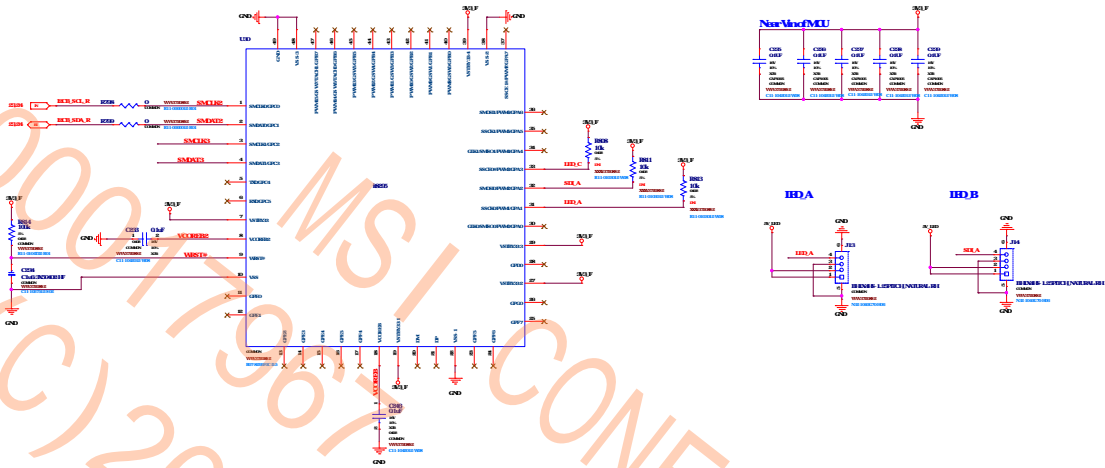
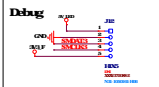
Remove LED



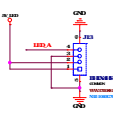
Remove LEDBOOST



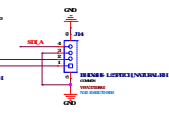
Pinout Diagram



IB/A



IB/B



5V/IBD

