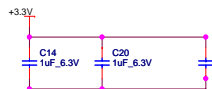
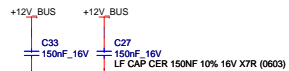
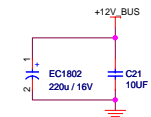
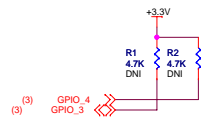


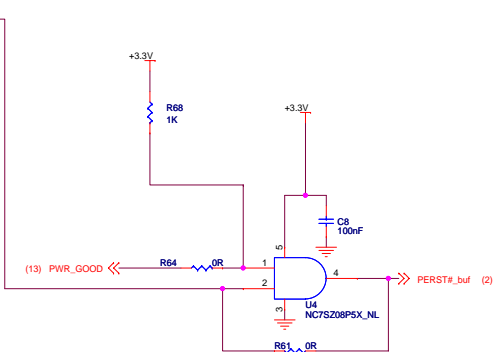
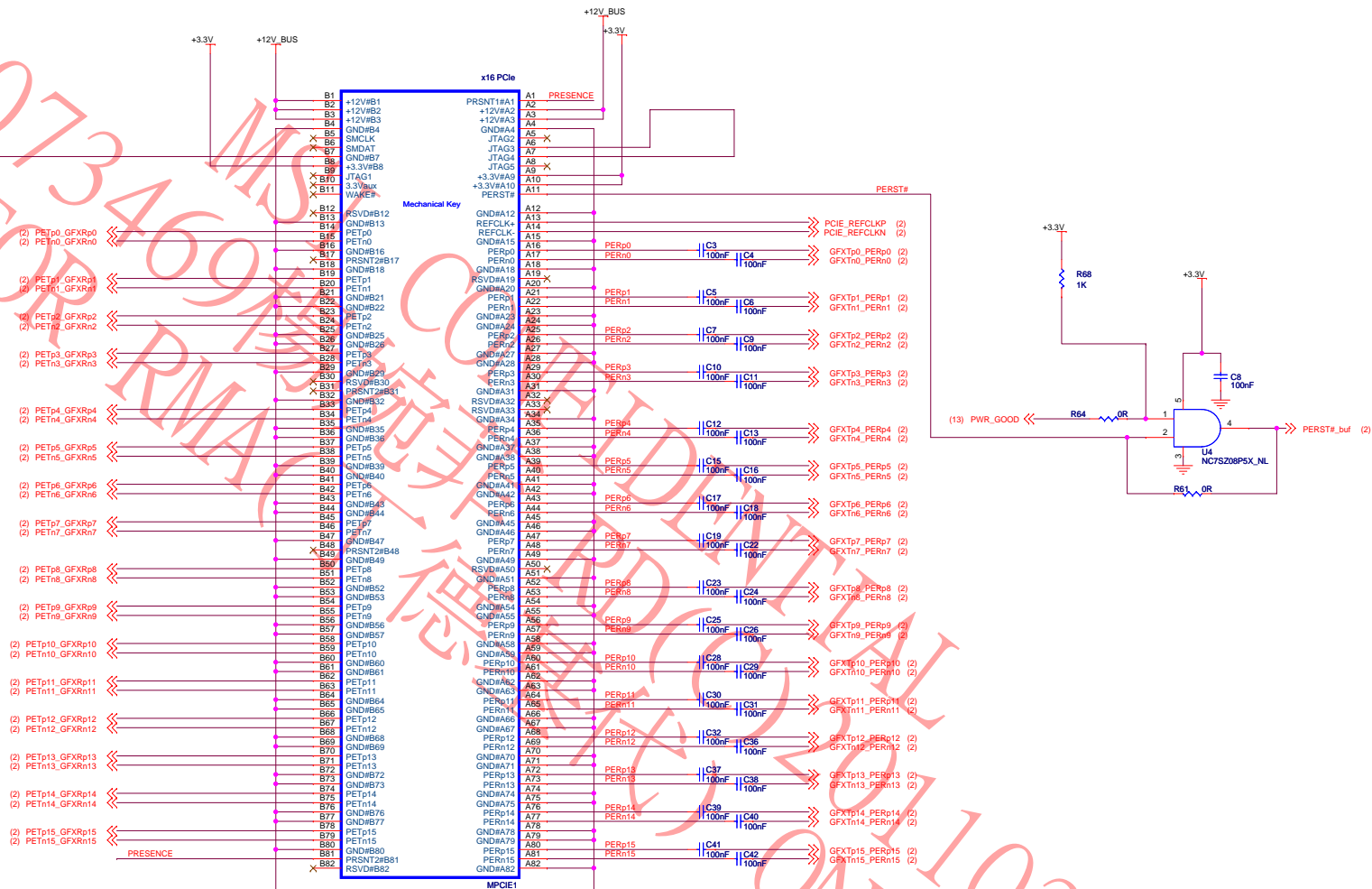
# PCI-EXPRESS EDGE CONNECTOR



Place these caps last,  
ideally as close to the bus  
connector as possible

CAP CER 10UF 20% 16V  
X5R (1206)1.6MM H MAX

CAP CER 10UF 10% 6.3V X5R  
(0805)1.6MM MAX THICK

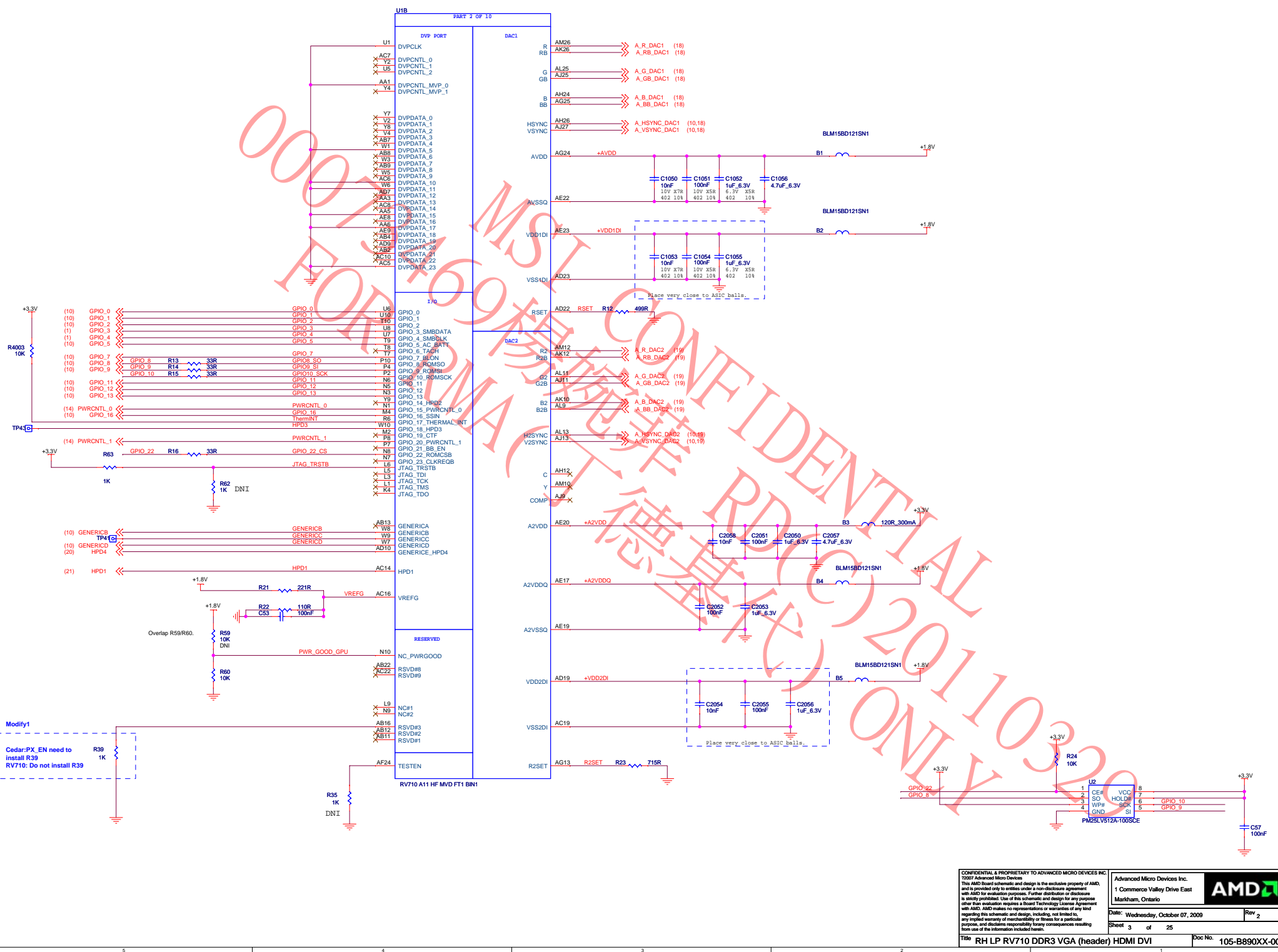


SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

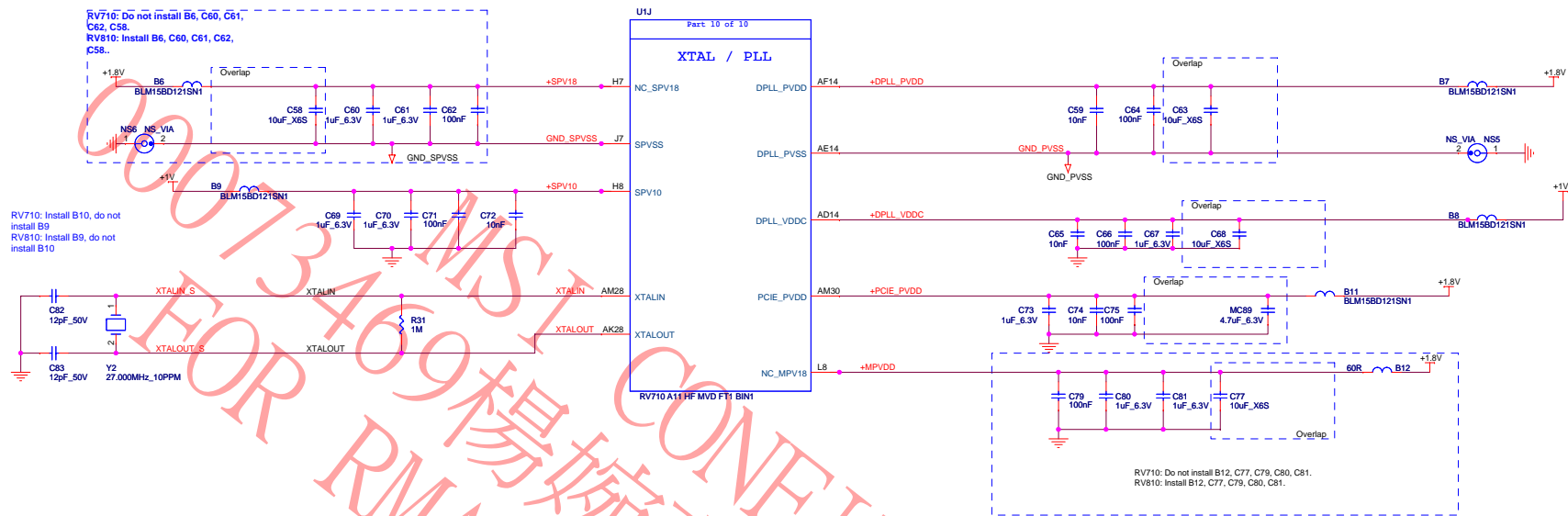
(2) RV710 PCIe Interface



**(3) RV710 Main**



(04) RV710 GPIOs CF XTAL

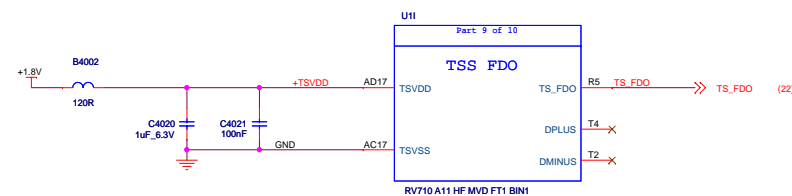
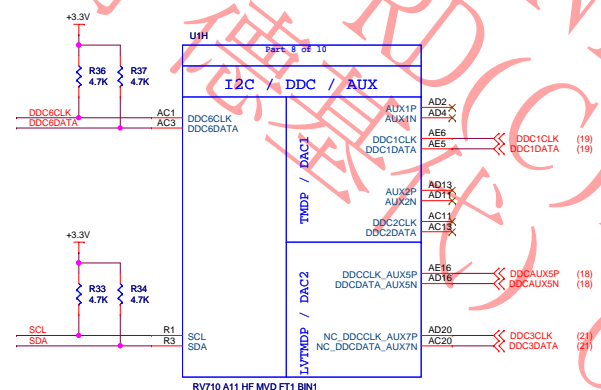


DDC6 BUS:

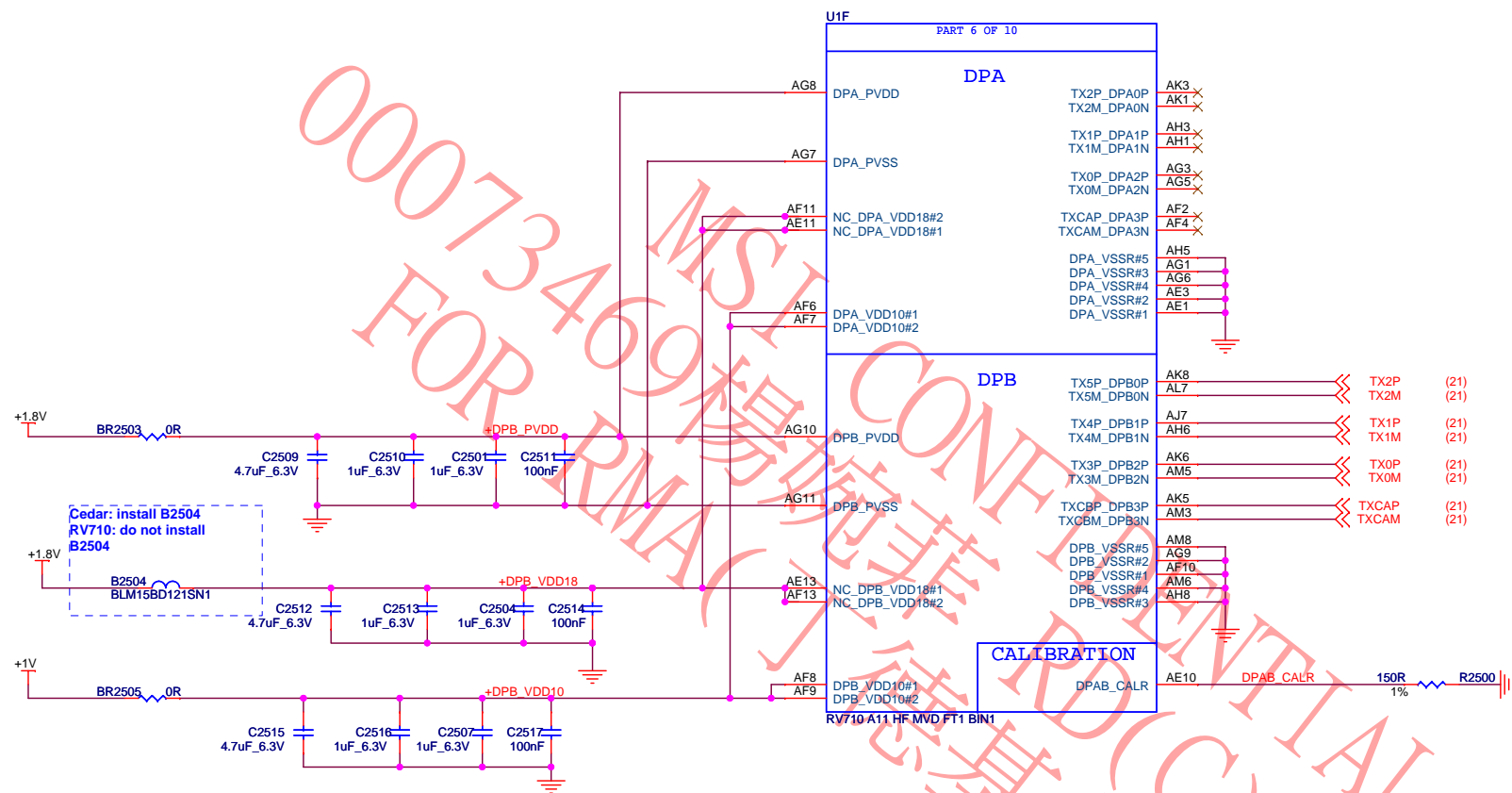
I2C Address	Function	Device
0x90	I2C VDDC Control	DS4402
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A



## TMDP INTERFACE



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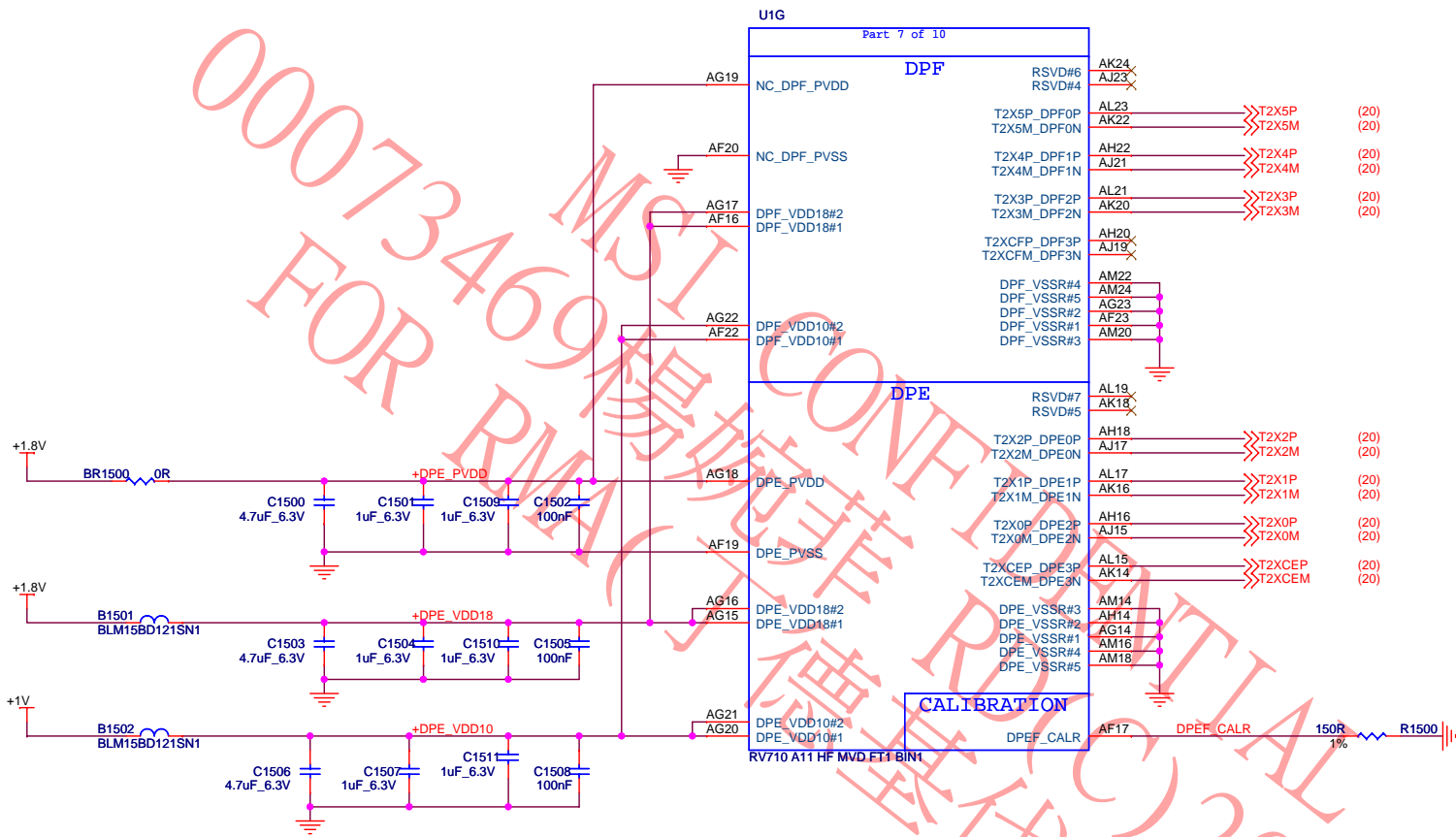
Date: Wednesday, October 07, 2009	Rev 2
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Title	RH LP RV710 DDR3 VGA (header) HDMI DVI
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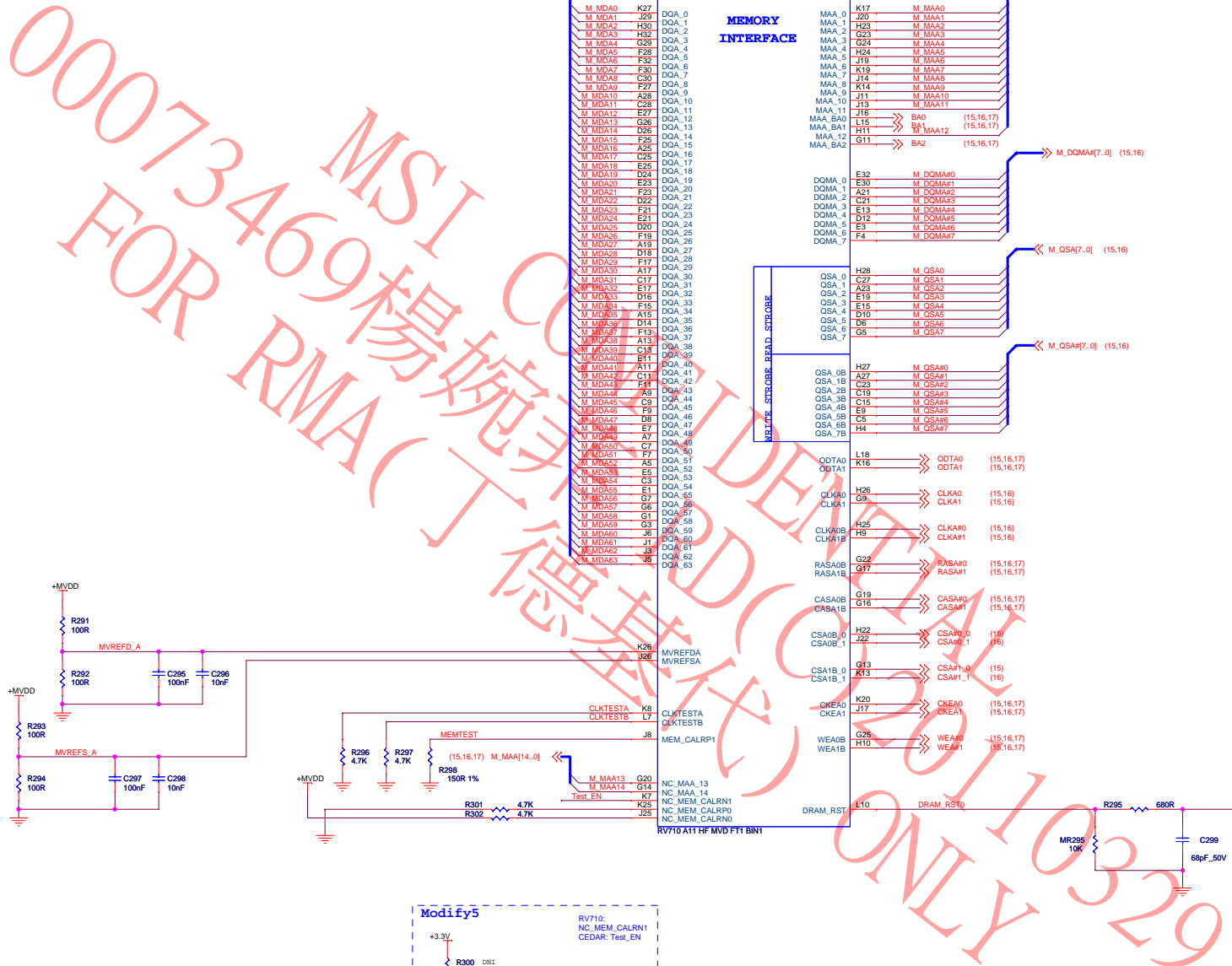
Doc No.	105-B890XX-00B
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LVTMDP INTERFACE

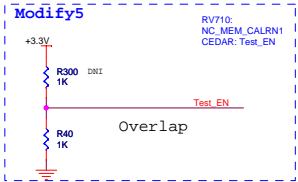


1A

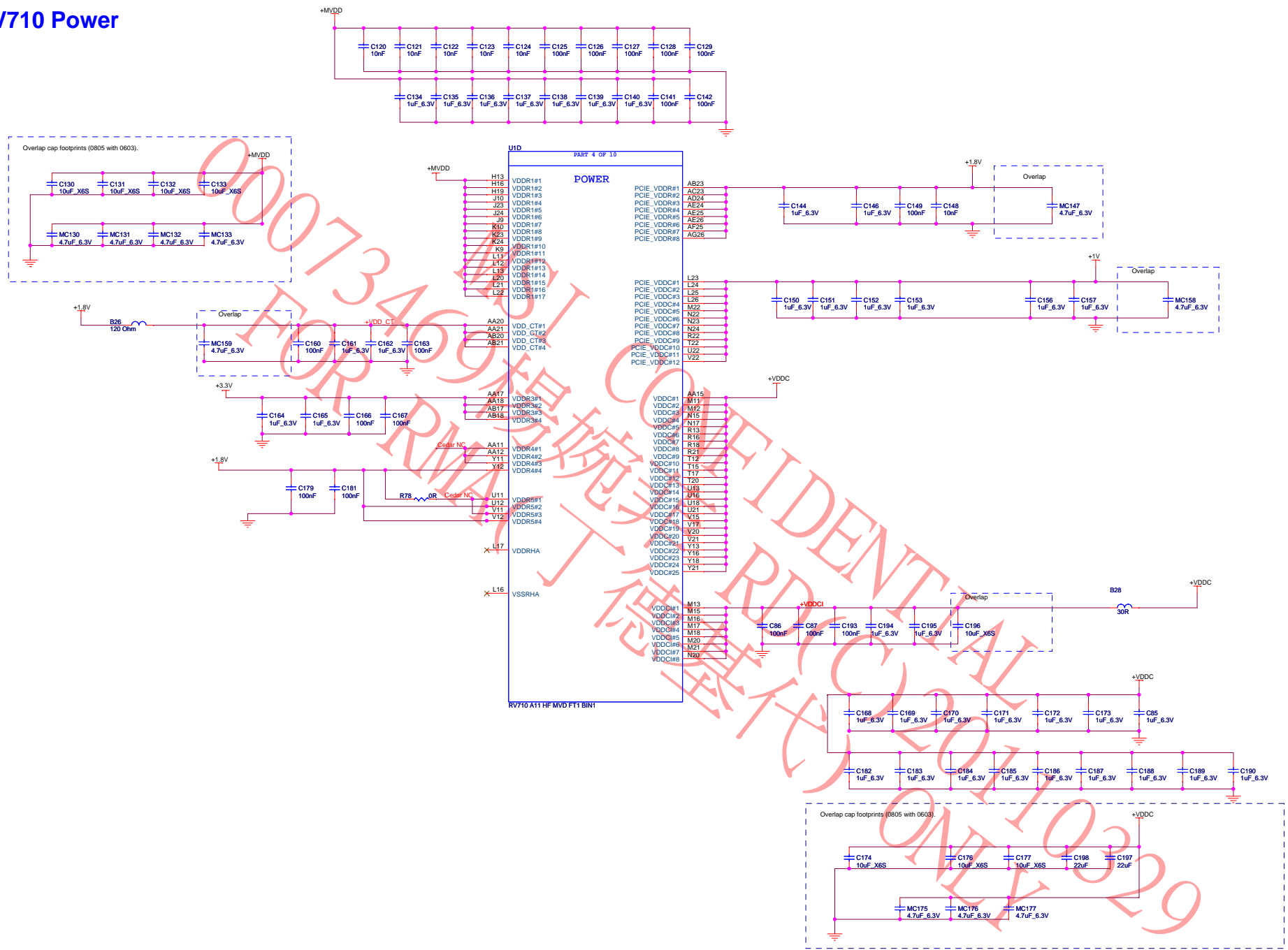
MEMORY INTERFACE



DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R

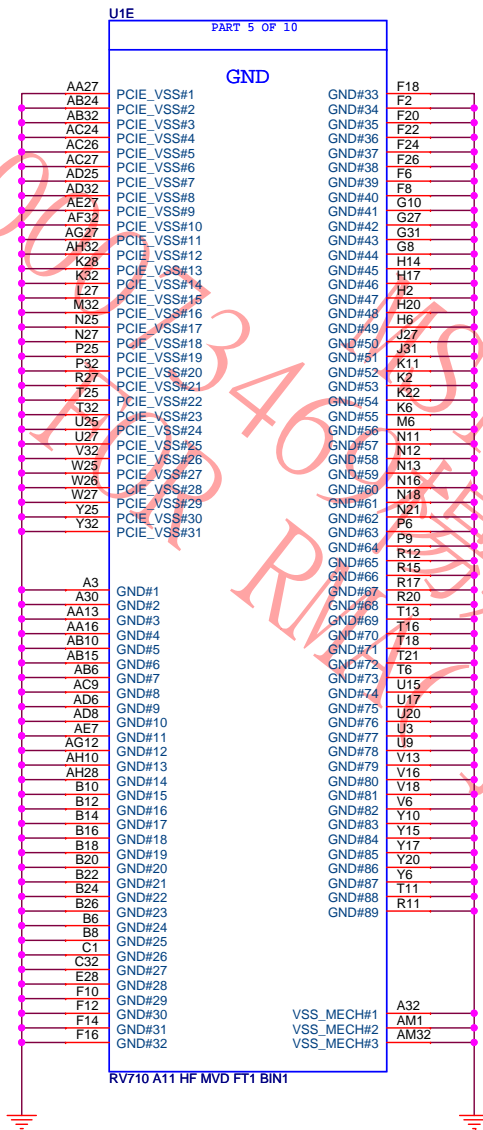


(08) RV710 Power





# (09) RV710 GND



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Title RH LP RV710 DDR3 VGA (header) HDMI DVI

Doc No. 105-B890XX-00B

(10) RV710 STRAPS

PIN BASED STRAPS



VIP\_DEVICE\_STRAP\_EN  
0: Driver would ignore the value sampled on VHAD\_0 during reset  
1: Driver would use the value sampled at reset from VHAD\_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no).

VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO(0) - TX\_PWRS\_ENB (Transmitter Power Savings Enable)  
0: 50% Tx output swing for mobile mode  
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX\_DEEMPH\_EN (Transmitter De-emphasis Enable)  
0: Tx de-emphasis disabled for mobile mode  
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF\_GEN2\_EN (5.0 GT/s Enable)  
0 : Default. (Driver Controlled Gen2)  
1 : Strap Controlled Gen2

GPIO(13, 12,11) - CONFIG[2..0]  
100 - 512Kbit M25P05A (ST)  
101 - 1Mbit M25P10A (ST)  
101 - 2Mbit M25P20 (ST)  
101 - 4Mbit M25P40 (ST)  
101 - 8Mbit M25P80 (ST)  
100 - 512Kbit Pm25LV512 (Chingis)  
101 - 1Mbit Pm25LV010 (Chingis)

AUD[0]

AUD[1]

BIF\_CLK\_PM\_EN  
0 - Disable CLKREQ# power management capability  
1 - Enable CLKREQ# power management capability

[GPIO\_5 : GPIO\_16]

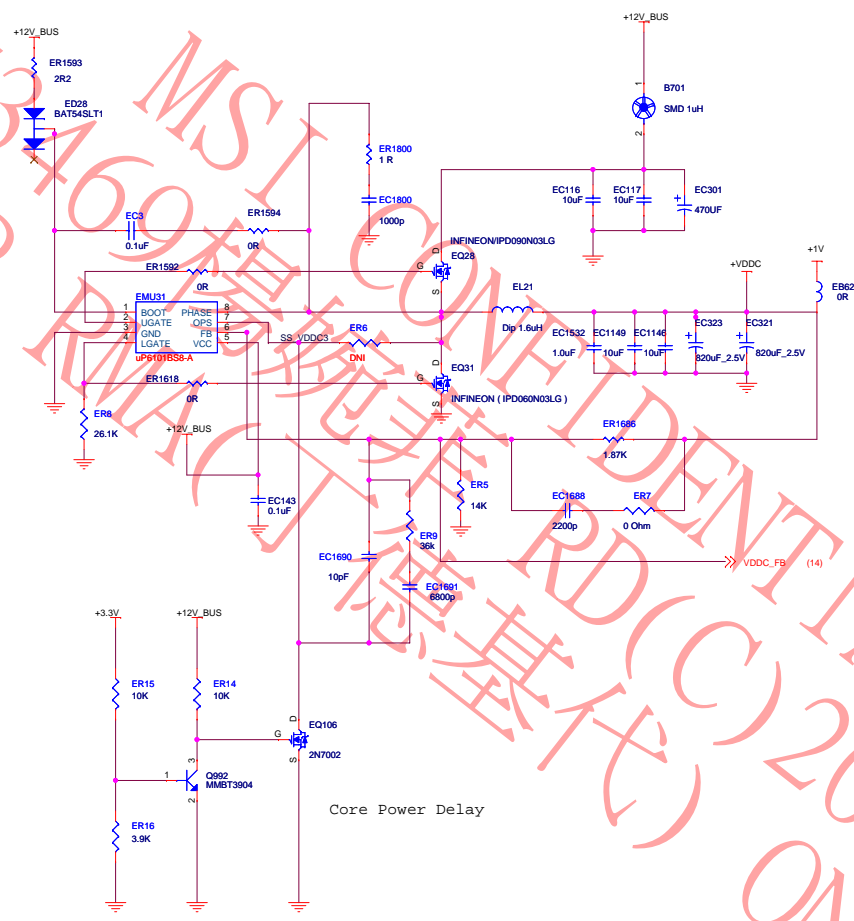
Quimonda [0:0]  
Hynix [0:1]  
Samsung [1:0]

RESERVED :Internal use only. Other logic must not affect this signal during RESET.

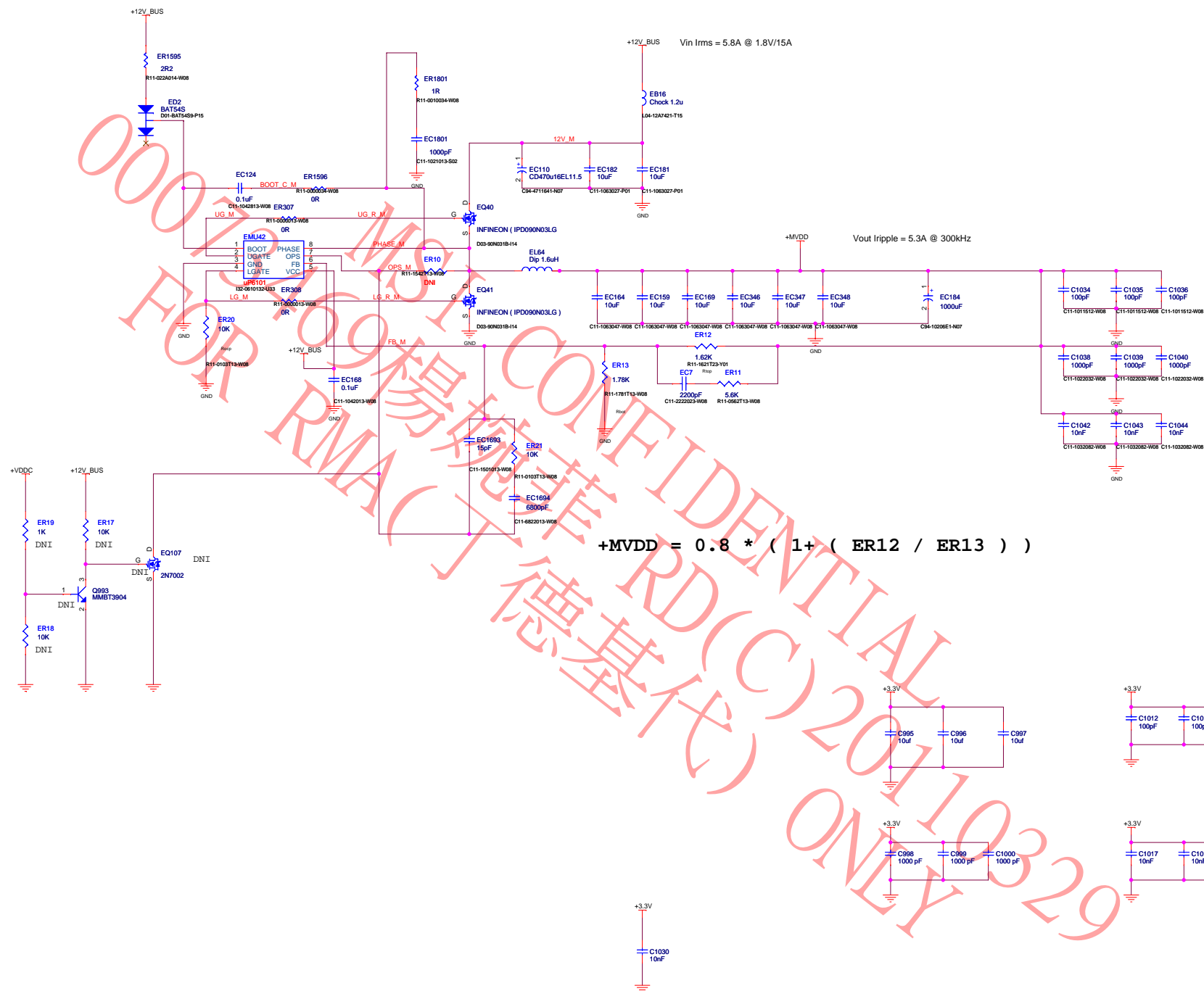
TV OUT STANDARD 0 - PAL TVO 1 - NTSC TVO

GenericB and GenericD will be used for additional memory vendor straps.

(11) VDDC

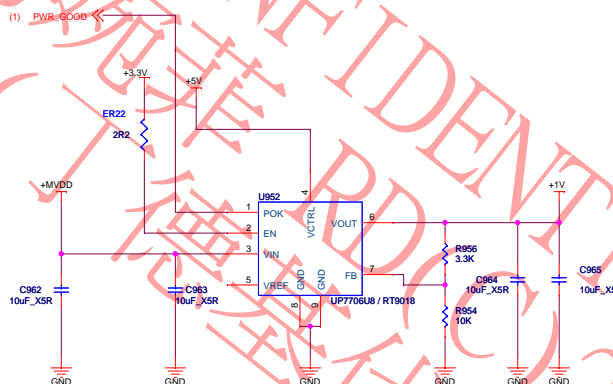
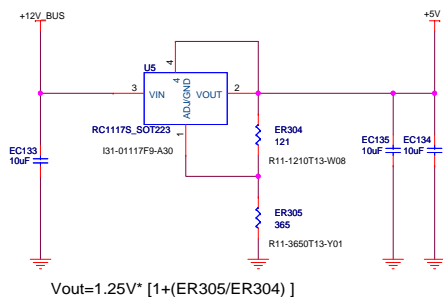
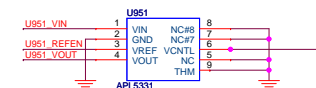
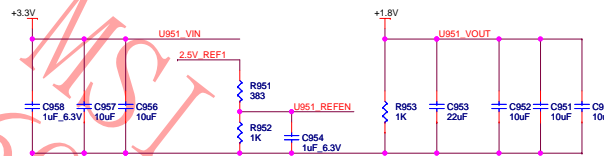
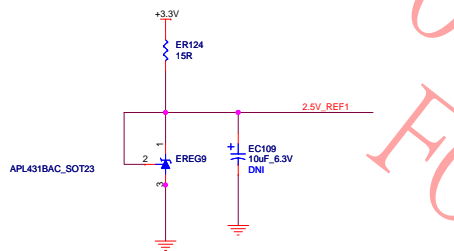


**(12) MVDD**



Memory Power Seq

# (13) Linear Regulators



$$V_{out}=0.8V * ( 1+ R956 / R954 )$$

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Title RH LP RV710 DDR3 VGA (header) HDMI DVI Doc No. 105-B890XX-00B

00073469 MSI CONFIDENTIAL FOR RMA (楊婉菲) (丁德基代) 20110329 ONLY

Power Play

VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V)		RE1= RE2=	RE1= RE2=
		RE1= RE2=	RE1= RE2=		
0	0				
0	1				
1	0				
1	1	1	0	1	Power-up Default

(3) PWRCNTL\_0

(3) PWRCNTL\_1

2N7002E Q1200

2N7002E Q1201

R1226 30K 1%

R1225 14K 1%

MR1240 10K

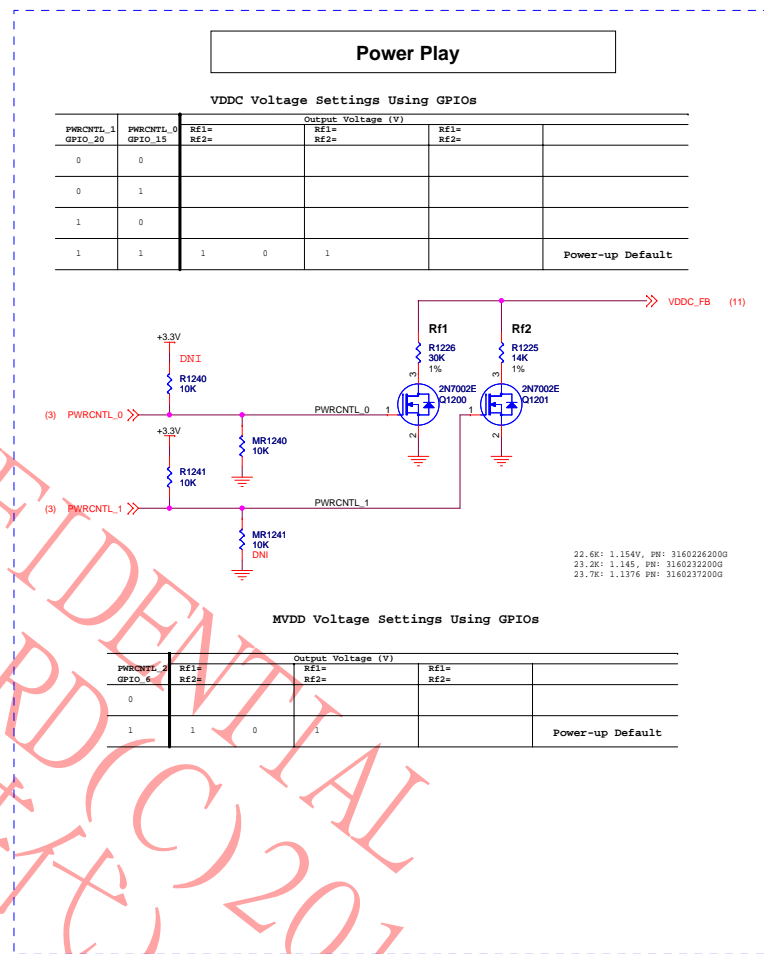
MR1241 10K

DNI

22.6K: 1.154V, PH: 1  
23.2K: 1.145, PH: 31  
23.7K: 1.1376 PH: 31

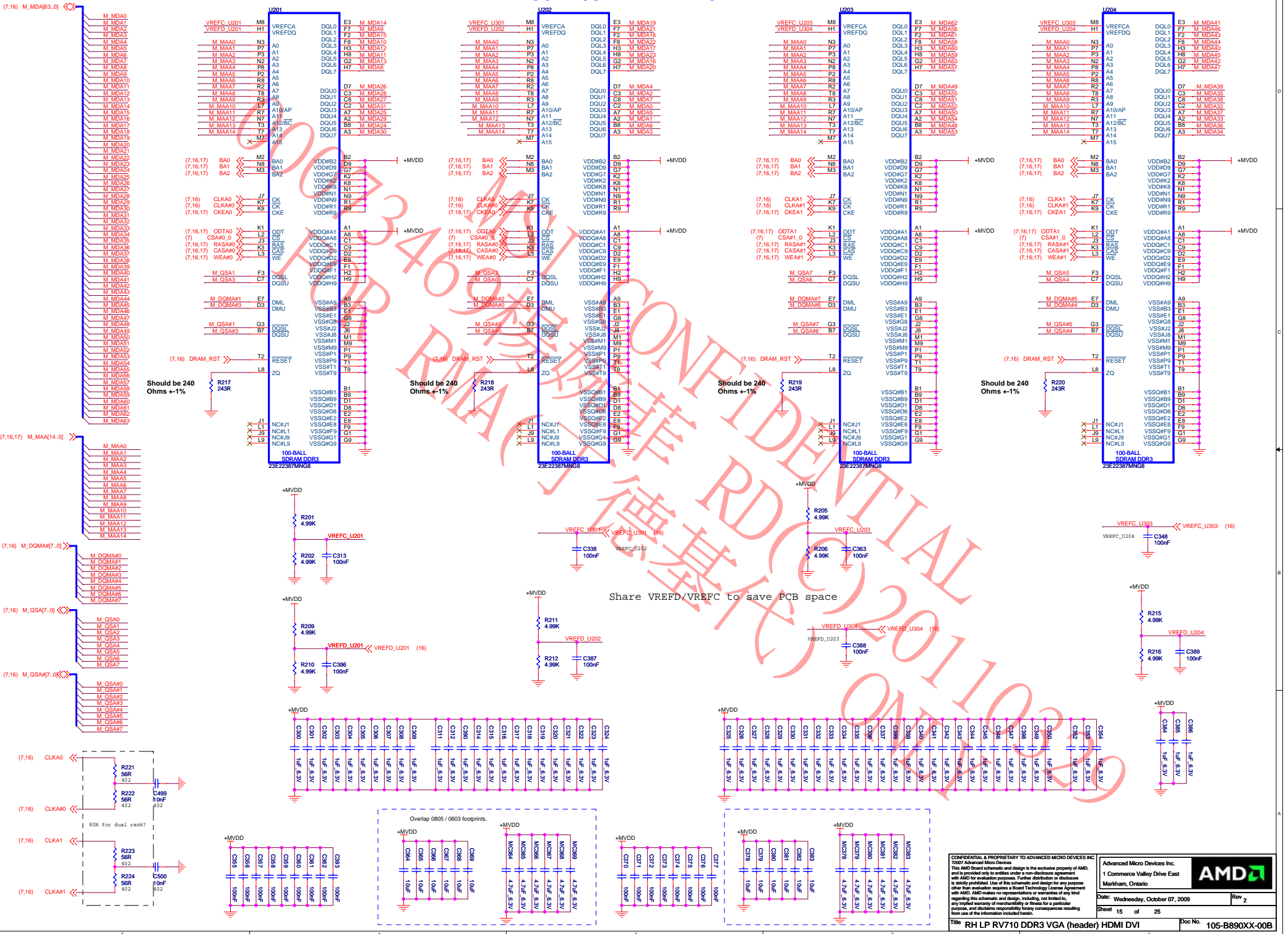
MVDD Voltage Settings Using GPIOs

PWRCNTL_6 GPIO_6	RE1= RE2=	Output Voltage (V)		RE1= RE2=	RE1= RE2=
		RE1= RE2=	RE1= RE2=		
0					
1	1	0	1		Power-up Default



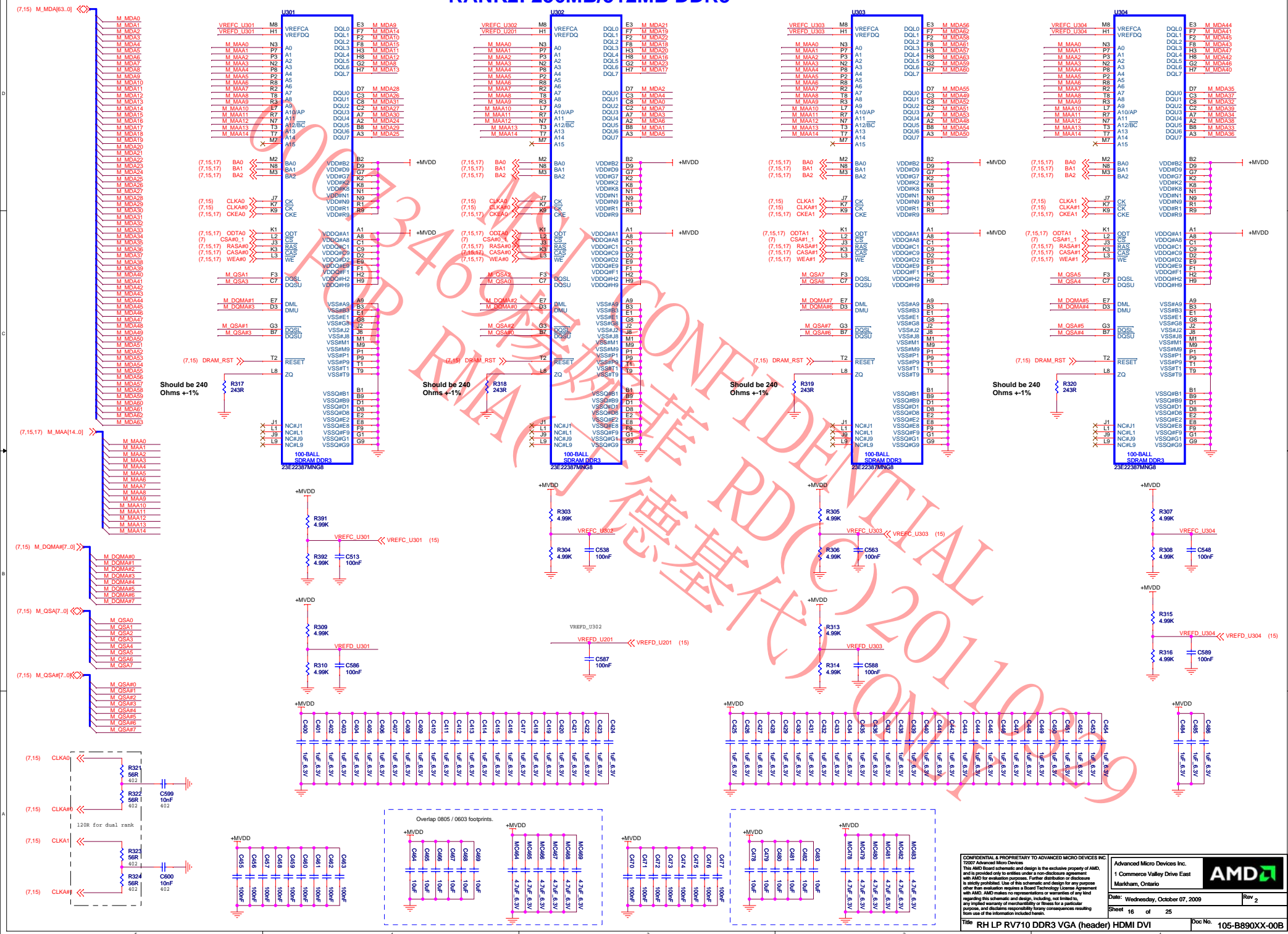
# (15) DDR3 RANK1

## RANK1: 256MB/512MB DDR3



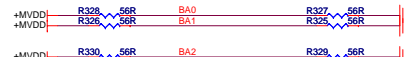
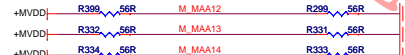
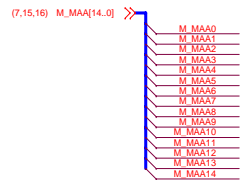


**RANK2: 256MB/512MB DDR3**





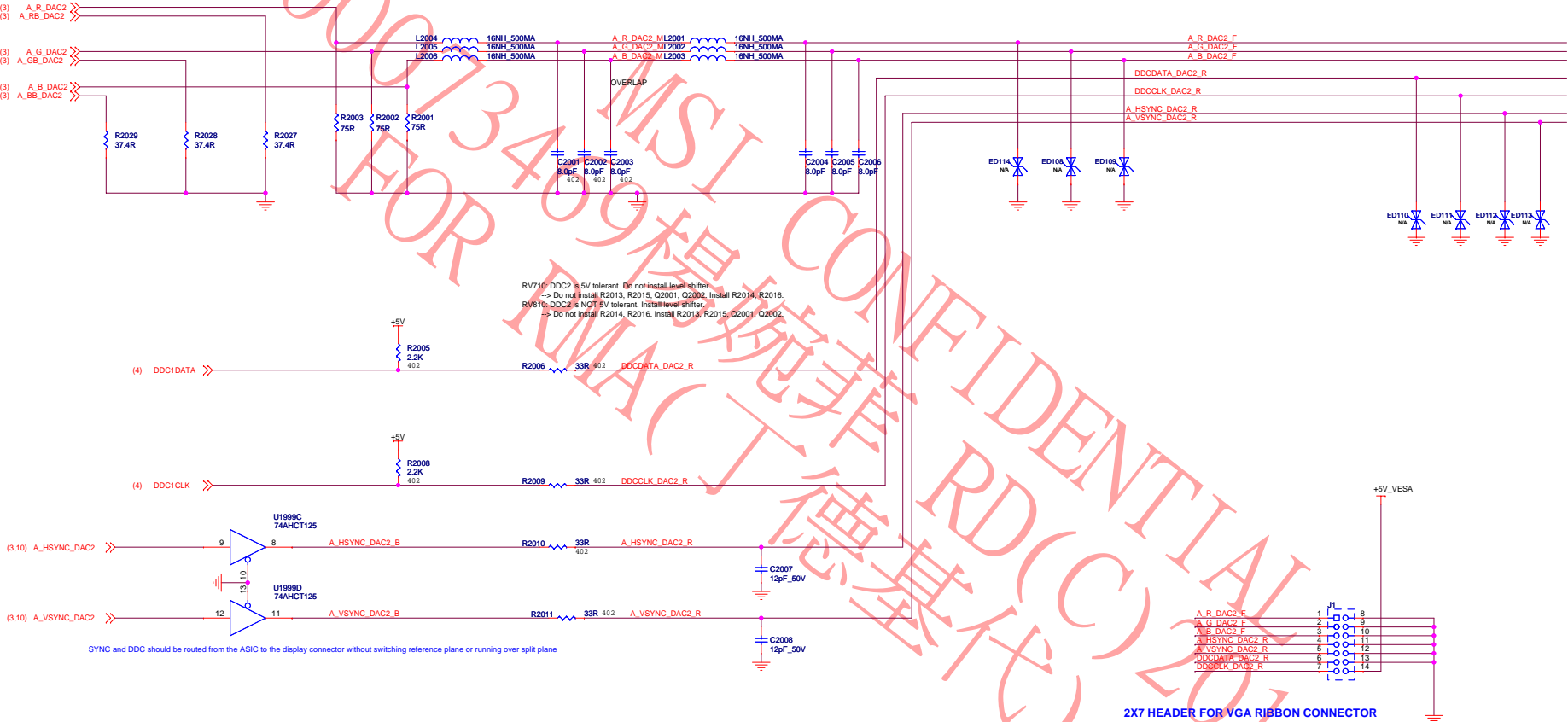
# (17) DDR3 Termination



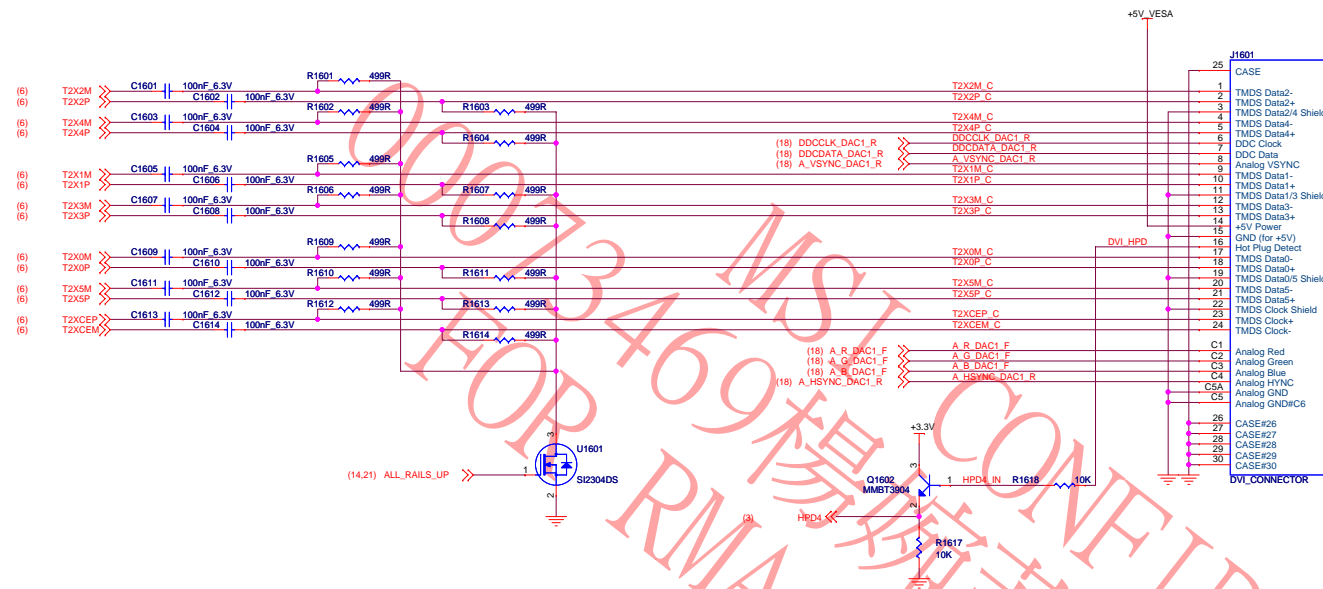




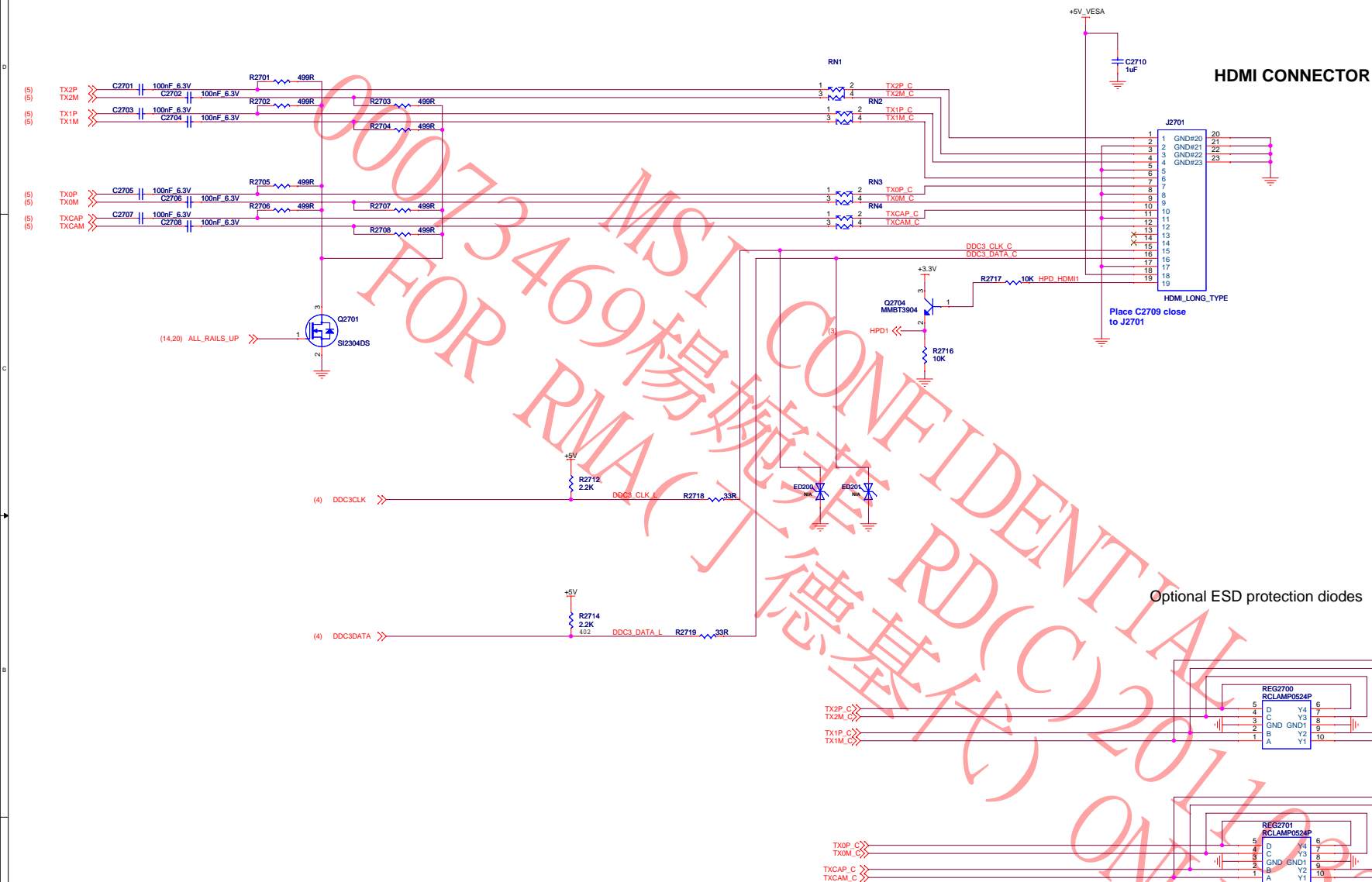
Place close to Connector  
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane



DPE / DPF OUTPUT



## TMDP-B OUTPUT



HDMI CONNECTOR

Optional ESD protection diodes

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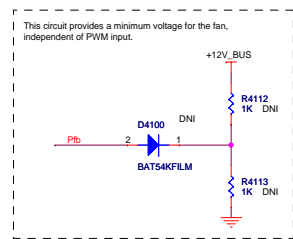
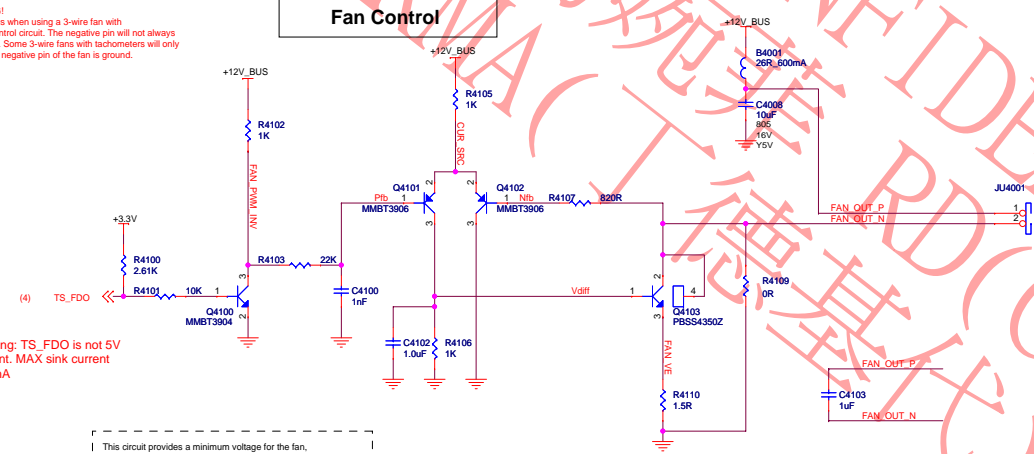


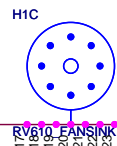
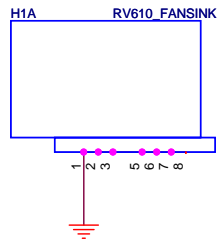
Title: RH LP RV710 DDR3 VGA (header) HDMI DVI  
Doc No.: 105-B890XX-00B

**WARNING!**  
Be cautious when using a 3-wire fan with this fan control circuit. The negative pin will not always be ground. Some 3-wire fans with tachometers will only work if the negative pin of the fan is ground.

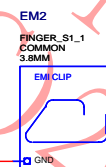
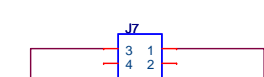
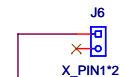
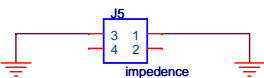
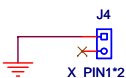
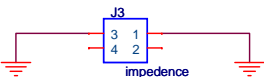
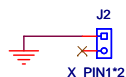
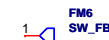
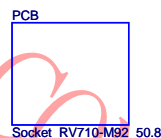
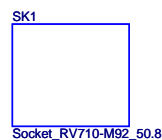
Warning: TS\_FDO is not 5V tolerant. MAX sink current 1.65mA

### Fan Control





7120036200G



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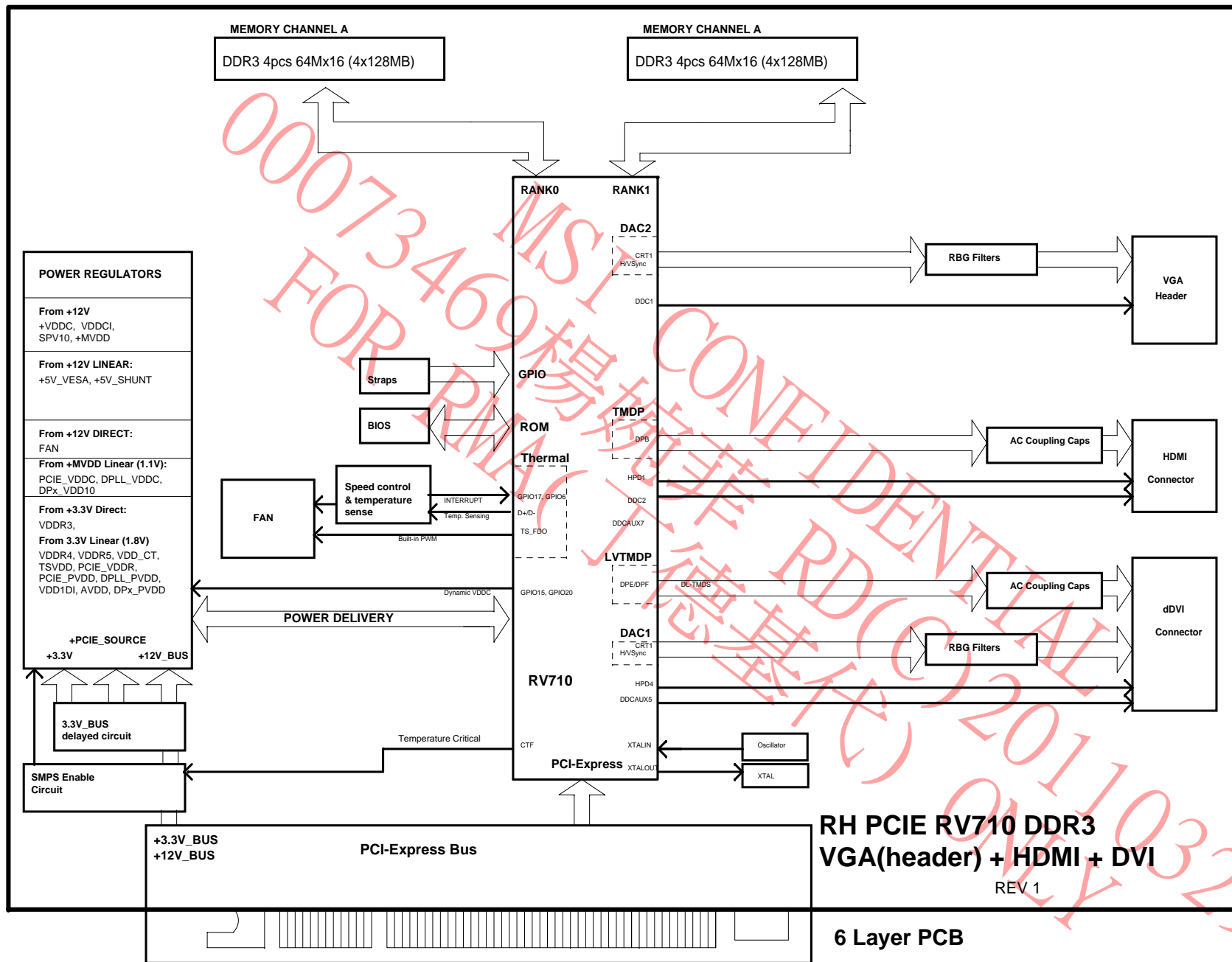
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Title RH LP RV710 DDR3 VGA (header) HDMI DVI Doc No. 105-B890XX-00B



**RH PCIE RV710 DDR3  
VGA(header) + HDMI + DVI**  
REV 1



<div>AMD</div>			Title		Schematic No.		Date:	
			RH LP RV710 DDR3 VGA (header) HDMI DVI		105-B890XX-00B		Wednesday, October 07, 2009	
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.					Rev 2
			RV710 ENGINEERING BOARD			REVISION DESCRIPTION		
Sch Rev	PCB Rev	Date						
0	00A	2008.12.30	INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.					
1	00B	2009.01.22	Sch no change. just modify HDMI connnecro location on PCB					

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