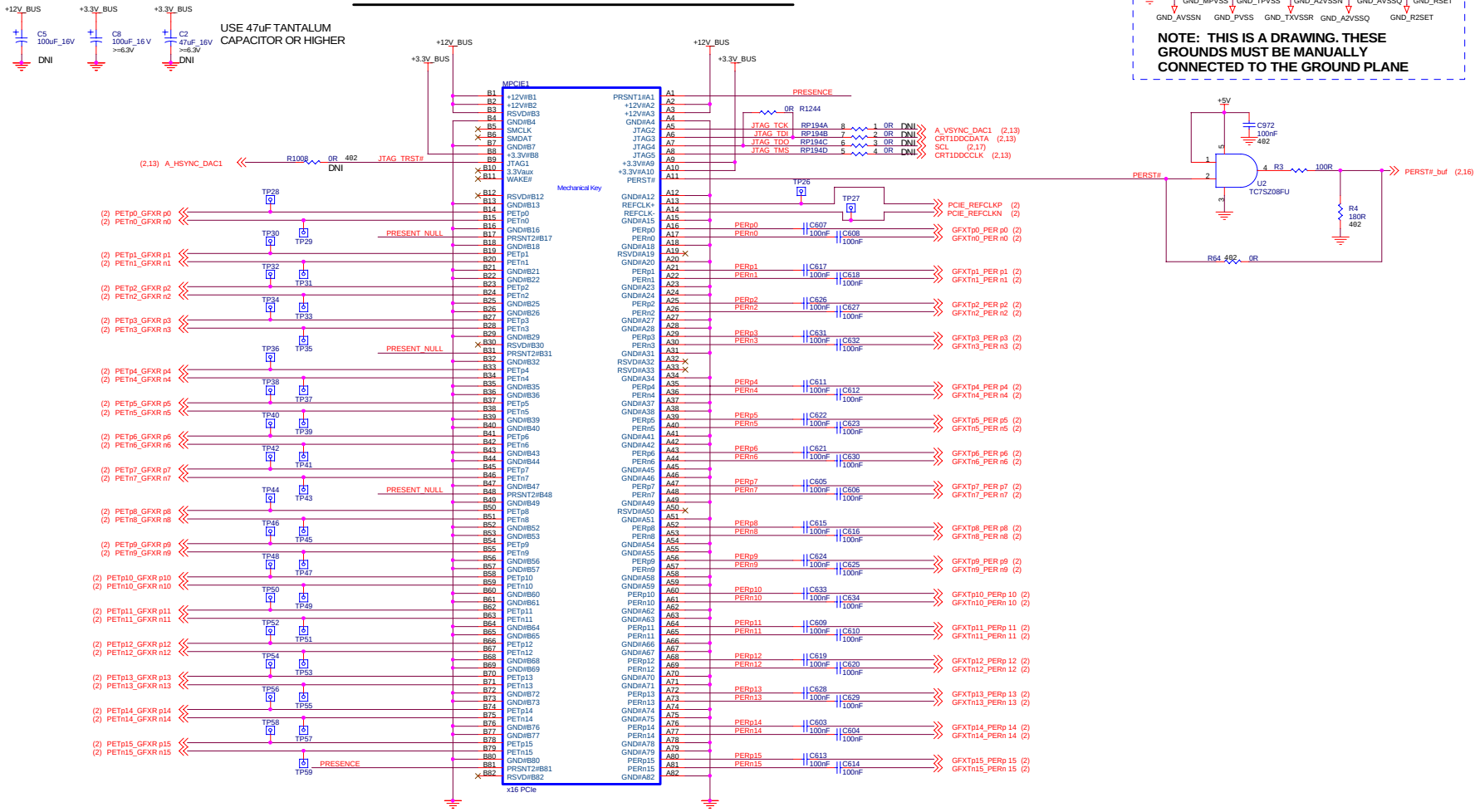
Title	Schematic No.	Date:
PCI-E RV380/370 256M pterm TSOP V-VV-DI	105-A334xx-00	**Tuesday, May 11, 2004**

REVISION HISTORY

Rev 6

Sch Rev		Date	REVISION DESCRIPTION
0	00A	2003-11-24	PRELIMINARY BASED ON 105-A297xx-00A 03-11-24 - (pg 02) Swap DVI DDC clock and data lines
1	00B	2003-12-29	- (pg 07) Add R1043 for power dissipation - (Layout) Move C284, blocking Grantsdale PCIE connector latch
2	00C	2004-03-09	- (Layout) Move fan connector to shorten fan power wire - (Layout) Correct C151 overlap - (pg02, 10) Fix pull-up +VDD_DVO to +VDDR4 - (pg04) Remove CP2, 3, 4, 5, 6 and 8 for dual footprint manufacturing issues (Capacitor packs sharing with 402 footprints) - (pg05) Remove dual-package FET for VDDC - (pg06) Remove C986, C987, C988, C989, C990, C991, C992 and C993) - (pg06) Change R297 to 1206 footprint - (pg07) Add MC917 as multi-footprint for C917, remove L3 (redundant option) - (pg13, 15) +5V supply with current limiting for VESA DDC spec, remove F1, B21 - (Layout/EMI) Connect L60, L61, L62, L80, L81, L82, C502, C504, C506, R513 and R514 to Digital Gnd instead of Chassis Gnd
3	00D	2004-04-01	- (pg04) Delete redundant dual footprint cap arrays (CP9, CP10 and CP11) - (pg05) Add MR357 and MR269 for power sequencing and delete redundant power sequence circuit (R153, R393~R398, Q27~Q30) - (pg05, layout) Improve RC snapper circuits (R15 and C156) layout on PWM - (pg05, layout) Correct overlapping component MU42 and D2 - (pg07) Delete redundant dual footprint caps (MC308 and MC160), delete redundant power sequencing (VDDC_GODD, VDDC_GOOD2 and VDDC_GOOD_PU, see pg05), change MREG37 reference to 1.8V - (pg07) Delete redundant regulators (REG8, U82, Q35, Q36, Q37, MQ37, R814~R816, R116~R119, R121~R123, R125~131, MR128, C14, C15 and C308) - (pg12) Correct some unused straps pull-up to +VDDR4 (R227, R229 and R231) - (pg13, layout) Move JU2 to the left to allow 2 more resistors for Chassis Digital Ground Short (R989 and R990) - (pg14) Add optional TVO filter MC502, MC504 and MC506 to chassis ground, add MR514 to place it below MiniDIN connector - (pg15) Change J2 to fully-shielded DVI connector - (layout) Improve thermal connection to MREG37 - (layout) Ground fill between TMDS pairs
4	00E	2004-04-08	- (pg13) Delete chassis gnd to digital ground resistors, change VGA and Slim-VGA connector chassis gnd to digital gnd - (pg14) Change VO filter, VO and VIVO connector to digital ground only - (pg15) Change DVI connector to digital gnd only - (pg16) Change VINGND of RT to digital gnd thru bead - (pg18) Change mounting hole to digital gnd, remove MT2 - (layout) Remove ground fill between TMDS pairs - (layout) Cut back +3.3V_BUS and +PCIE_VDDR power plans on layer 3 - (pg14) Remove R514, R513 and MR513
5	00F	2004-04-14	-00F revision was created based on customer's request to avoid confusion - (pg15) Add R926, R927, R928 and R929 to meet 70% derating spec of the power dissipation of resistors
6	00	2004-04-28	- Release to 00

PCI-EXPRESS EDGE CONNECTOR



NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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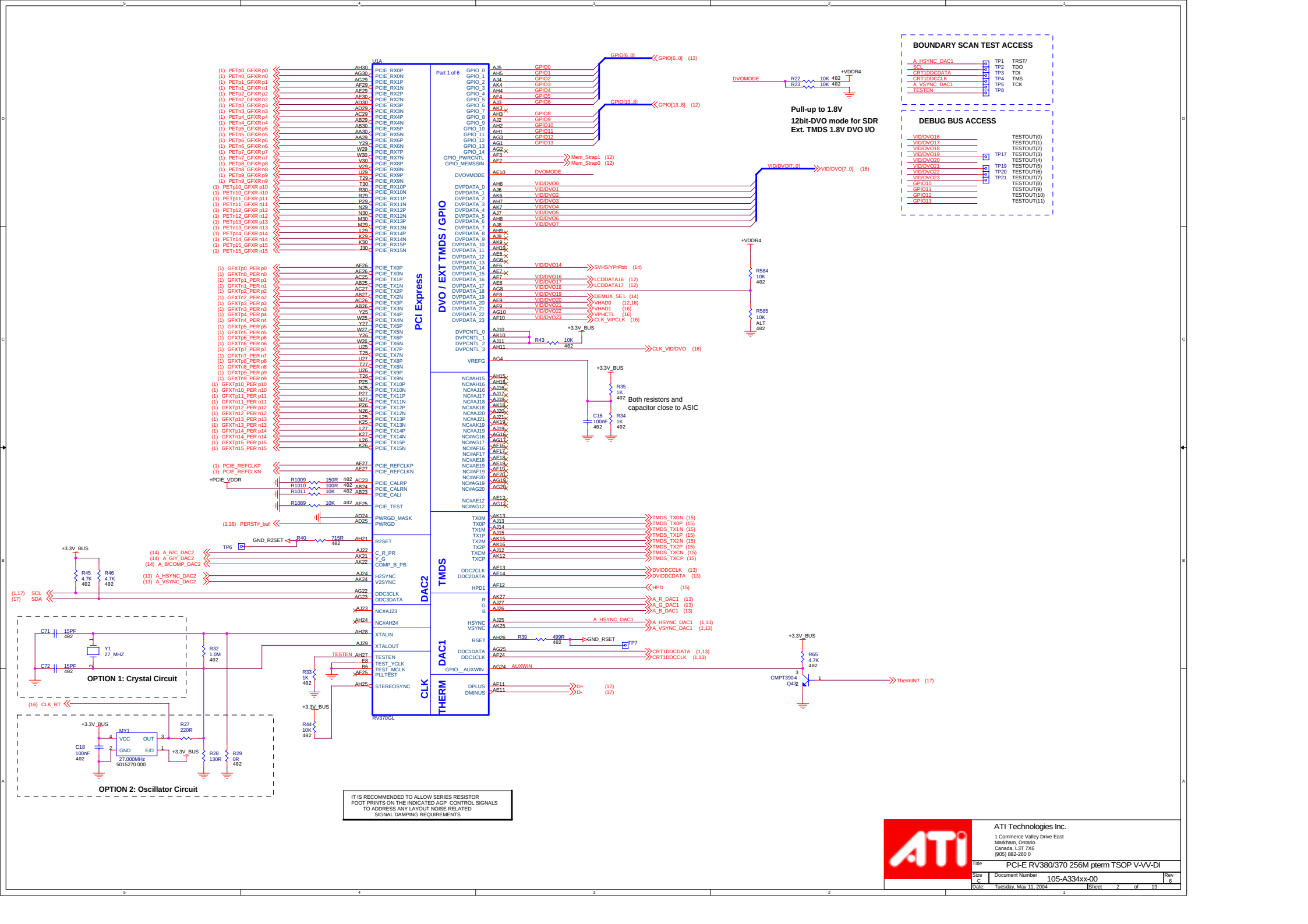
Title	PCI-E RV380/370 256M pterm TSOP V-VV- DI		
Size C	Document Number 105-A334xx-00		Rev 6
Date: Tuesday, May 11, 2004	Sheet 1 of 19		


BOUNDARY SCAN TEST ACCESS
A_HSYNC_DAC1
SCL
CRT1DDCDATA
CRT1DDCCLK
A_VSYNC_DAC1
TESTEN
TP1 TRST/
TP2 TDO
TP3 TDI
TP4 TMS
TP5 TCK
TP8
DEBUG BUS ACCESS
VID/DVO16
VID/DVO17
VID/DVO18
VID/DVO19
VID/DVO20
VID/DVO21
VID/DVO22
VID/DVO23
GPIO10
GPIO11
GPIO12
GPIO13
TP17
TP19
TP20
TP21
TESTOUT(0)
TESTOUT(1)
TESTOUT(2)
TESTOUT(3)
TESTOUT(4)
TESTOUT(5)
TESTOUT(6)
TESTOUT(7)
TESTOUT(8)
TESTOUT(9)
TESTOUT(10)
TESTOUT(11)
U1A
Part 1 of 6
PCI Express
DVO / EXT TMDS / GPIO
DAC2
TMDS
DAC1
CLK
THERM
RV370GL
Pull-up to 1.8V
12bit-DVO mode for SDR
Ext. TMDS 1.8V DVO I/O
DVOMODE
+VDDR4
R22 10K 402
R23 10K 402
VID/DVO[7..0]
R584 10K 402
R585 10K ALT 402
+3.3V_BUS
R43 10K 402
R35 1K 402
C16 100nF 402
R34 1K 402
Both resistors and capacitor close to ASIC
GND_R2SET
R40 715R 402
TP6
R45 4.7K 402
R46 4.7K 402
C71 15PF 402
C72 15PF 402
Y1 27_MHZ
R32 1.0M 402
OPTION 1: Crystal Circuit
R33 1K 402
R44 10K 402
TESTEN
MY1
VCC OUT GND E/D
27.000MHz 5015270 000
C18 100nF 402
R27 220R
R28 130R
R29 0R 402
OPTION 2: Oscillator Circuit
R39 499R 402
TP7
GND_RSET
CMPT390-4 Q42
R65 4.7K 402
ThermINT (17)
IT IS RECOMMENDED TO ALLOW SERIES RESISTOR FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS TO ADDRESS ANY LAYOUT NOISE RELATED SIGNAL DAMPING REQUIREMENTS
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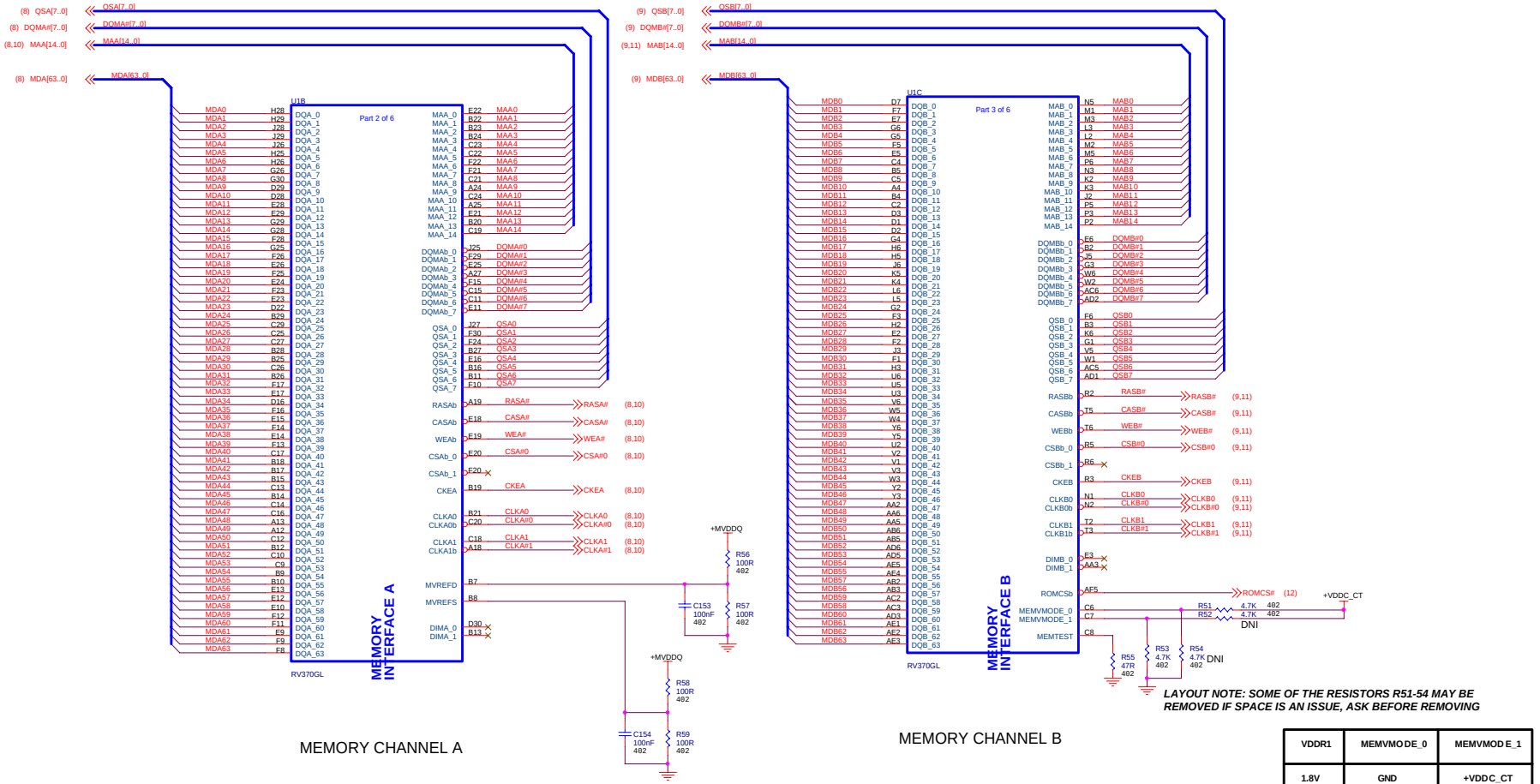
Title PCI-E RV380/370 256M pterm TSOP V-VV-DI
Size C
Document Number 105-A334xx-00
Rev 6
Date: Tuesday, May 11, 2004
Sheet 2 of 19



MEMORY CHANNEL A

MEMORY CHANNEL B

PLACE C351/152 VERY CLOSE TO ASIC

R56/57/58/59 CLOSE TO ASIC AS WELL

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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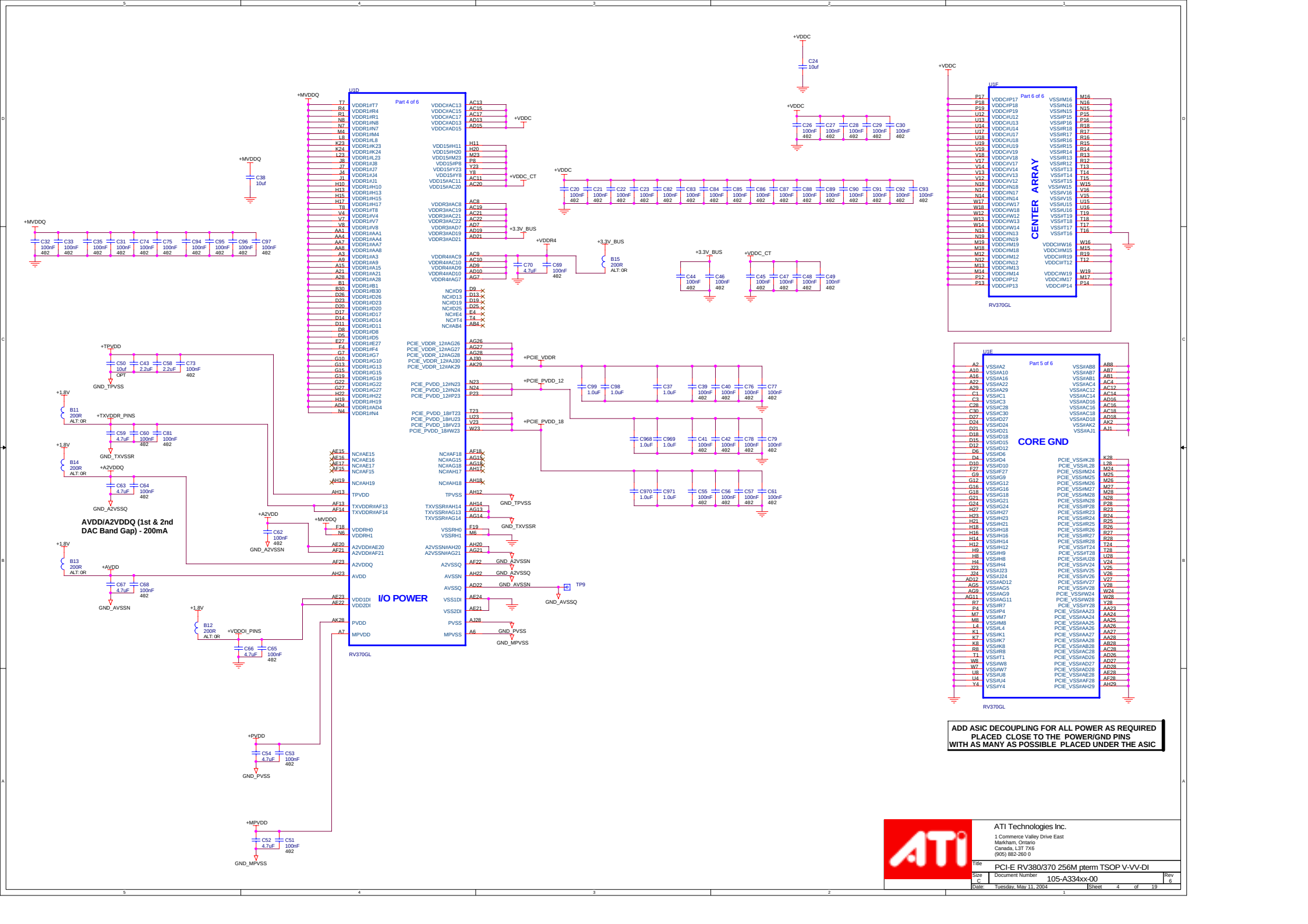
Title: PCI-E RV380/370 256M pterm TSOP V-VV-DI

Size: C | Document Number: 105-A334xx-00 | Rev: 6

Date: Tuesday, May 11, 2004 | Sheet 3 of 19


U1D
Part 4 of 6
RV370GL
I/O POWER
U1F
Part 6 of 6
CENTER ARRAY
RV370GL
U1E
Part 5 of 6
CORE GND
RV370GL
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
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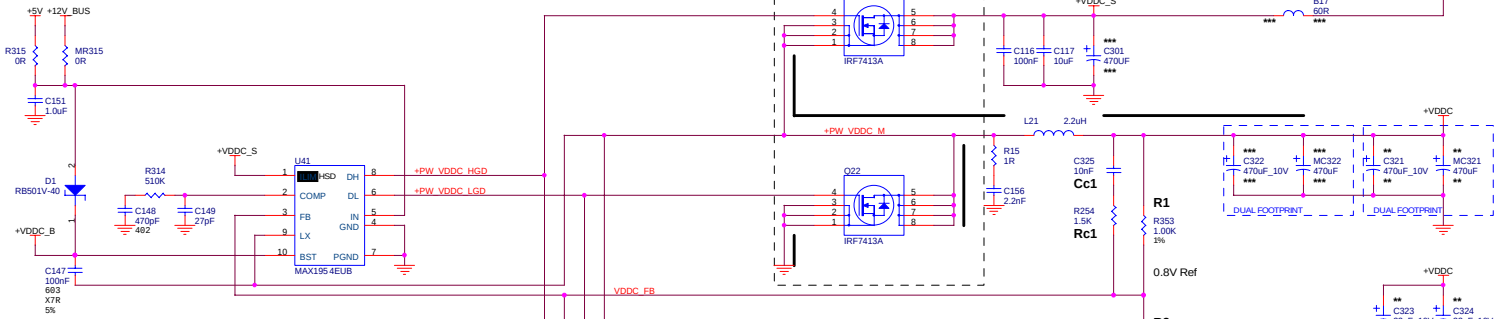
Size C
Document Number 105-A334xx-00
Rev 6
Date: Tuesday, May 11, 2004
Sheet 4 of 19

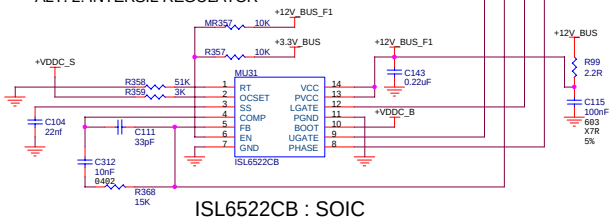
Regulator for VDDC (ASIC Core)

Vout = 1.2V ~ 1.3V

ALT. 1: MAXIM REGULATOR



ALT. 2: INTERSIL REGULATOR

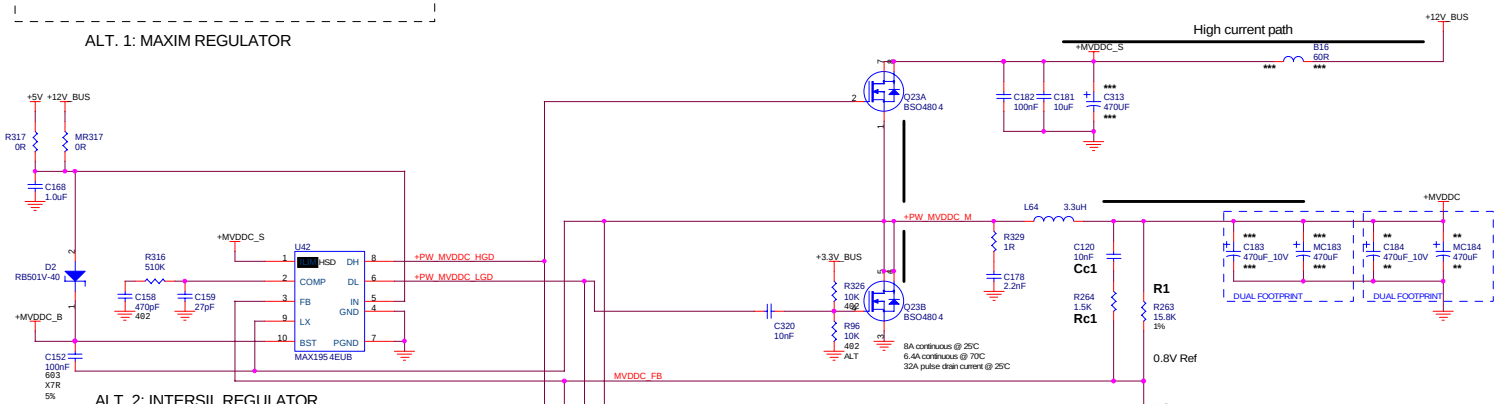


ISL6522CB : SOIC

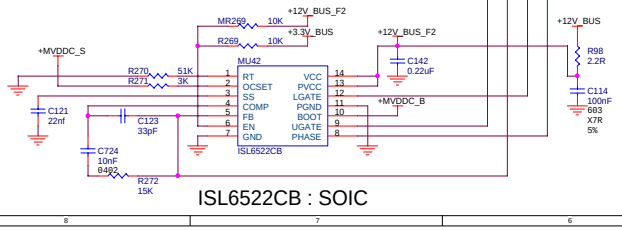
Regulator for MVDDC (Memory Core)

Vout = 2.5V ~ 3.3V

ALT. 1: MAXIM REGULATOR



ALT. 2: INTERSIL REGULATOR



ISL6522CB : SOIC

*** Indicate number of power via required for the connection

Part	NOTES
MAX1954	Do not install Cc1, Rc1
ISL6522	Install Cc1, Rc1

Part	Vout	R1	R2
MAX1954 ISL6522	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
0.8V Ref	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100

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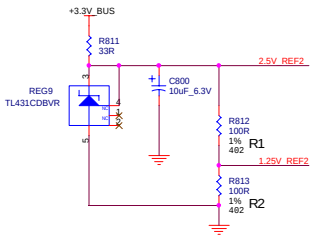
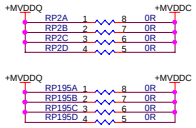
Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI	
Size: C	Document Number: 105-A334xx-00	Rev: 6
Date: Tuesday, May 11, 2004	Sheet 5 of 19	

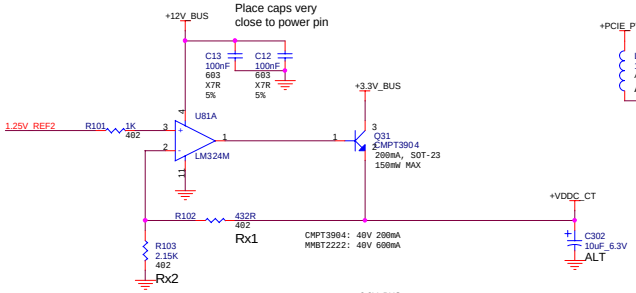


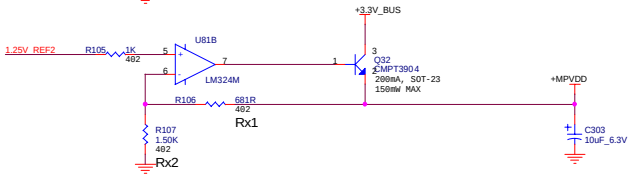
Voltage Req.	R1	R2
0.8V	150R P/N 3160150000 402	71.5R P/N 324075R500
1.25V	100R P/N 3160100000 402	100R P/N 3160100000 402
1.5V	100R P/N 3160100000 402	150R P/N 3160150000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

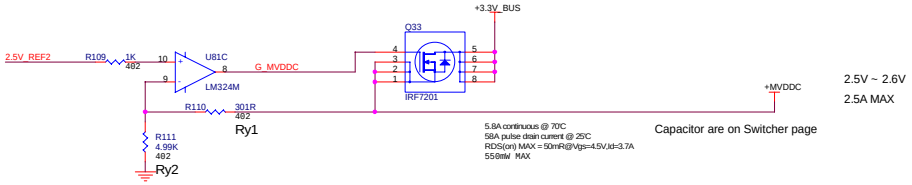
Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.55	475R (402, 1%) P/N 3160475000	2K (402, 1%) P/N 3160200100
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240015200

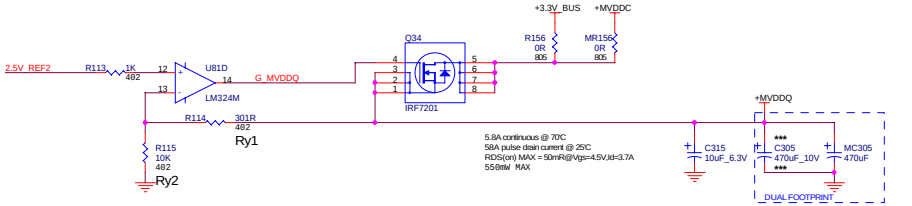
Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.61V	221R (402, 1%) P/N 3160221000	4.99K (402, 1%) P/N 3160499100
2.5V	0R P/N 3230000000 603 P/N 3150000000 402	DNI

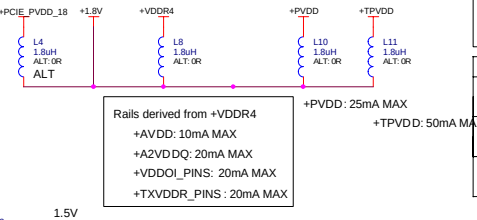






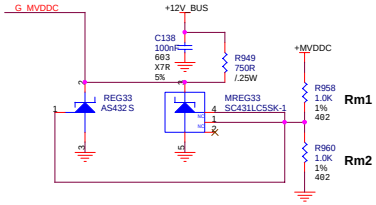






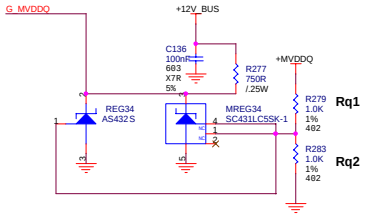
Alt. regulator for +MVDDC
Vout = 2.5V ~ 2.6V
Iout = 500mA MAX

Voltage Req.	Rm1	Rm2
3.34V [-0.04V/+0.04V]	4.32K	2.55K
3.45V [-0.04V/+0.04V]	4.32K	2.43K
2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100



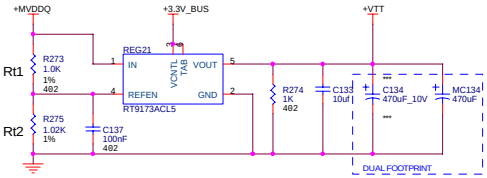
Alt regulator for +MVDDQ
Vout = 2.5V ~ 2.6V
Iout = 200mA MAX

Voltage Req.	Rq1	Rq2
1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
2.5V	1K 3240100100	1K 3240100100
2.6V	4.75K 3240475100	4.32K 3240432100



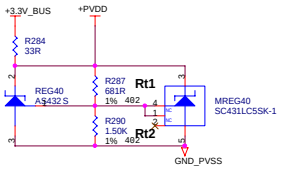
Regulator for +VTT (Termination)
Vout = 1.25V ~ 1.3V with +2.5V +MVDDQ
Iout = 1000mA MAX

+MVDDQ = +2.5V	Rt1	Rt2
1.25V	1K 3240100100	1K 3240100100
1.3V	1.0K 3240100100 603 3160100100 402	1.02K 3240102100

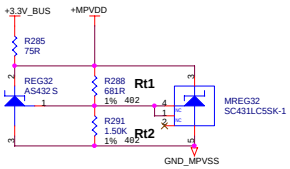


	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100

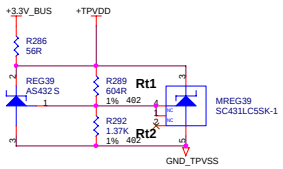
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



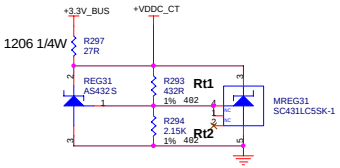
Alt regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX



Alt. regulator for +TPVDD
Vout = 1.65V ~ 1.85V
Iout = 20mA MAX



Alt regulator for +VDDC_CT
Vout = 1.5V
Iout = 70mA MAX



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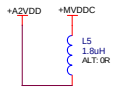
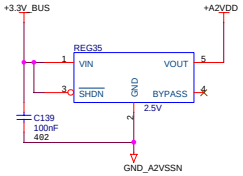
Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI	
Size C	Document Number 105-A334xx-00	Rev 6
Date: Tuesday, May 11, 2004	Sheet 6 of 19	

Alt. regulator for +A2VDD
Vout = 2.5V
Iout = 120mA MAX

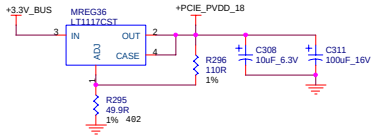
2.5V
120mA





+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.

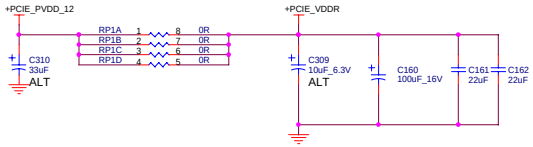
Alt. regulator for PCIE_PVDD_18
Vout = 1.85V
Iout = 500mA MAX



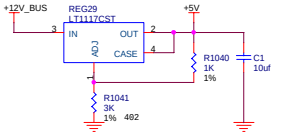
Need at least a 10uF Tant. output cap for stability
Min. Load Current: 10mA

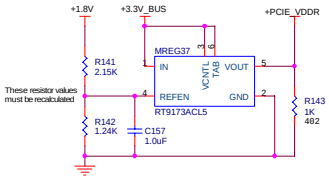
+PCIE_PVDD_12: 1.2V 25 0mA MAX

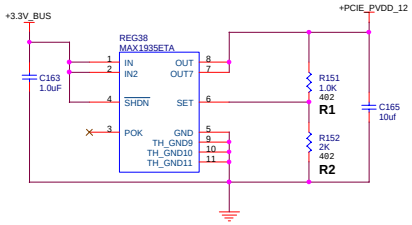
+PCIE_VDDR: 1.2V 13 00mA MAX

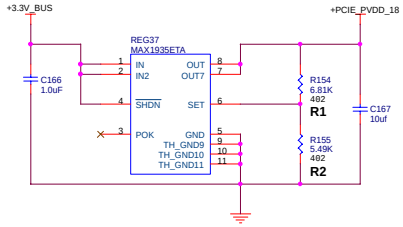


Regulator for +5V
Vout = 5V
Iout = 20mA MAX









Part	Vout	R1	R2
MAX1935 0.8V Ref	1.2V	1.00K 1% 402 ATI P/N 3160100100	2.00K 1% 402 ATI P/N 3160200100
	1.79V	6.81K 1% ATI P/N 3160681100	5.49K 1% 402 ATI P/N 3160549100

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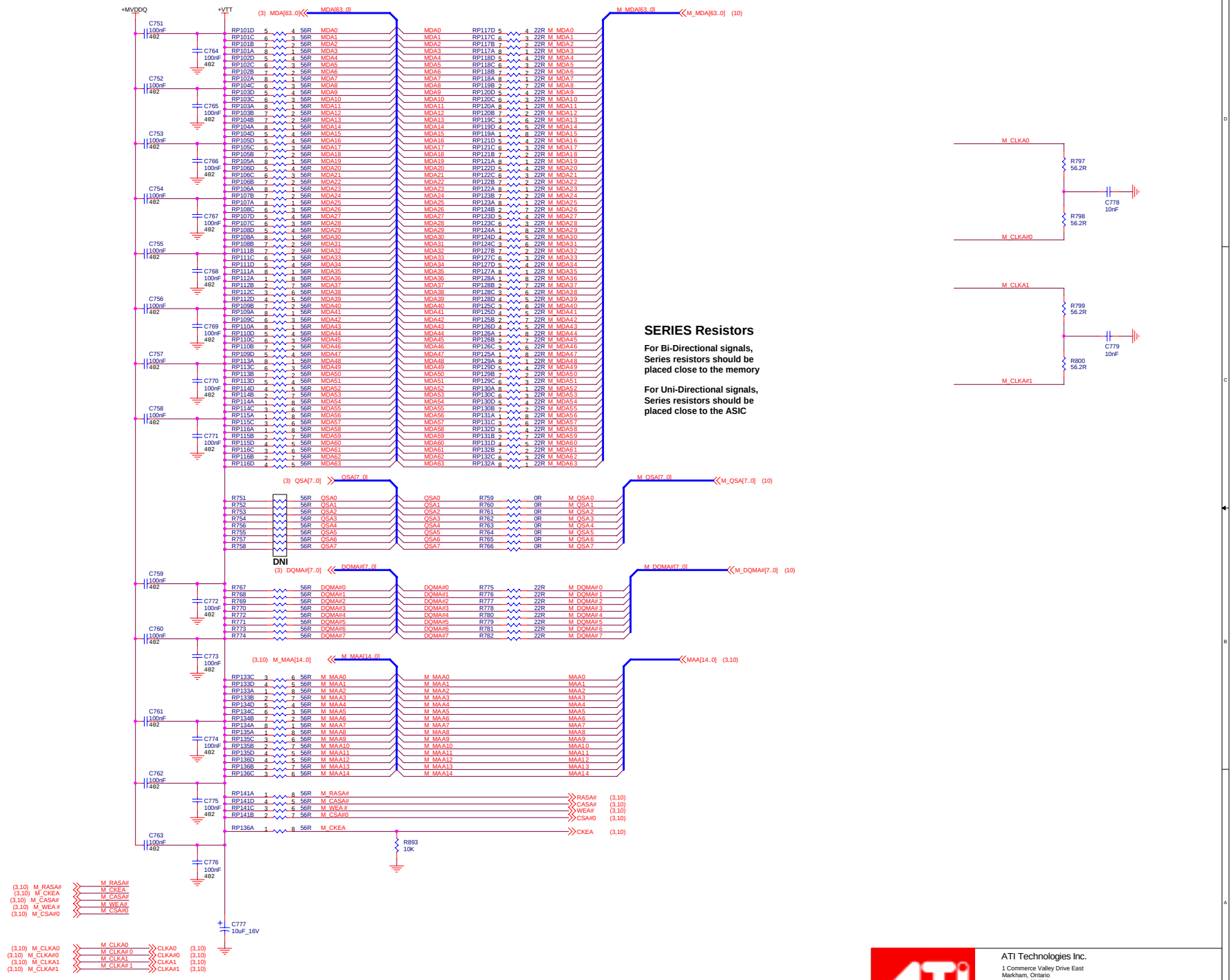
Title	PCI-E RV380/370 256M pterm TSOP V-VV- DI		
Size C	Document Number 105-A334xx-00		Rev 6
Date: Tuesday, May 11, 2004	Sheet 7 of 19		



SERIES Resistors

For Bi-Directional signals, Series resistors should be placed close to the memory

For Uni-Directional signals, Series resistors should be placed close to the ASIC

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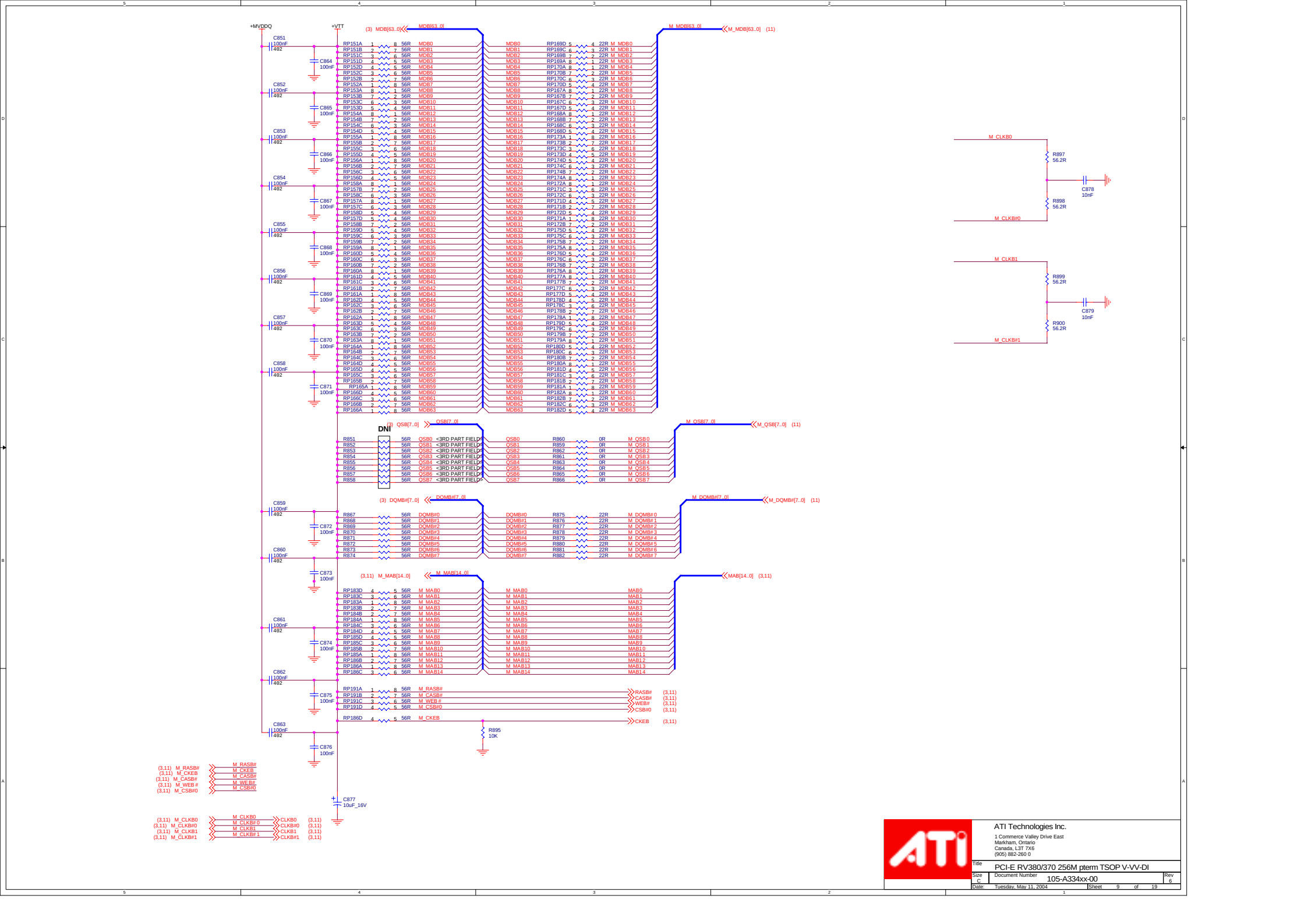
Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI		
Size: C	Document Number: 105-A334xx-00		Rev: 6
Date: Tuesday, May 11, 2004	Sheet 8 of 19		



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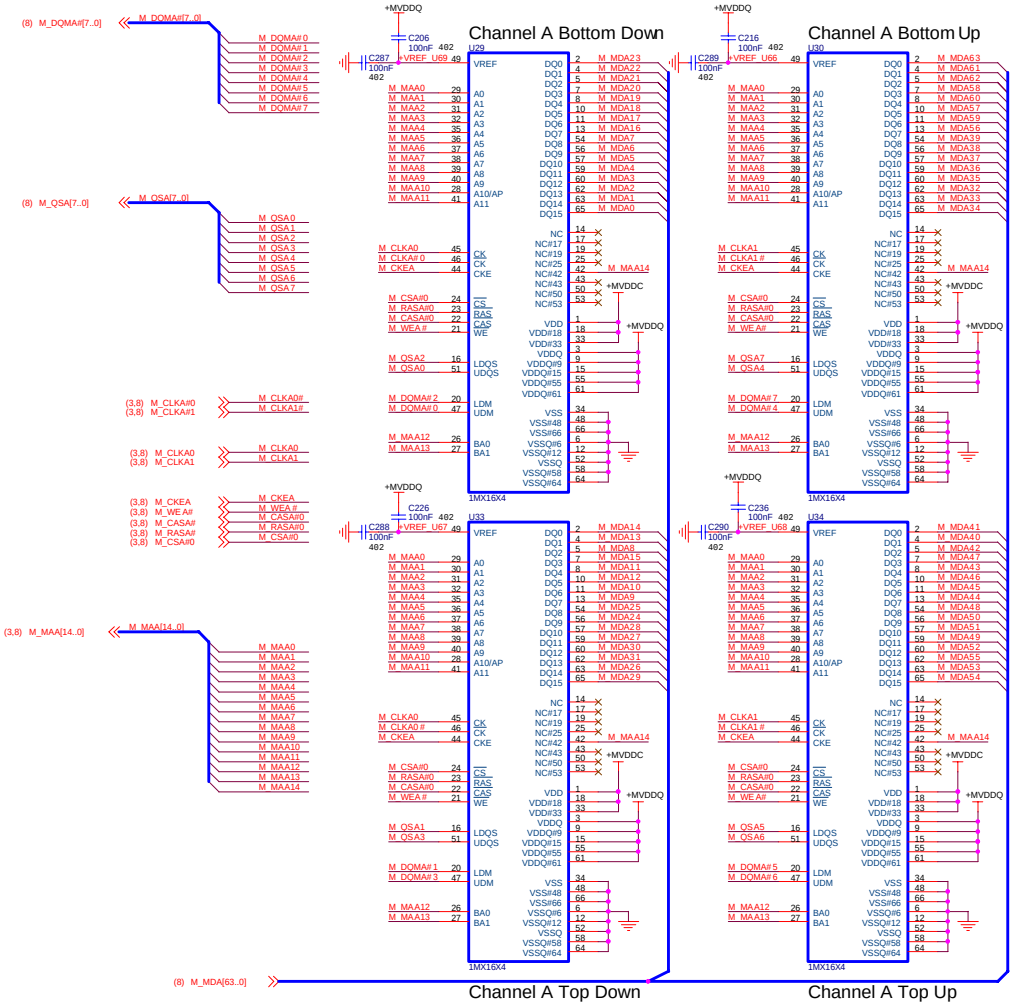
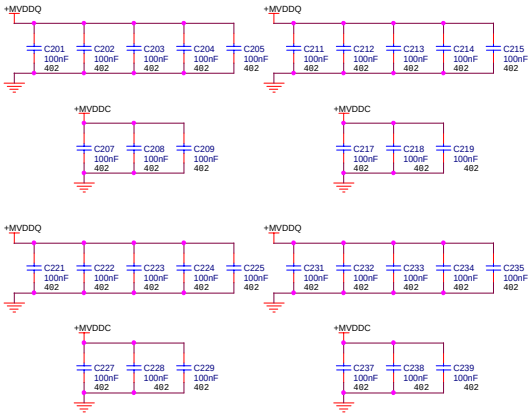
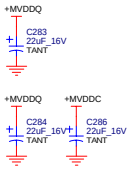
Size: C	Document Number: 105-A334xx-00		Rev: 6
Date: Tuesday, May 11, 2004	Sheet 9 of 19		



Put 1 1uF cap per power pin of memory





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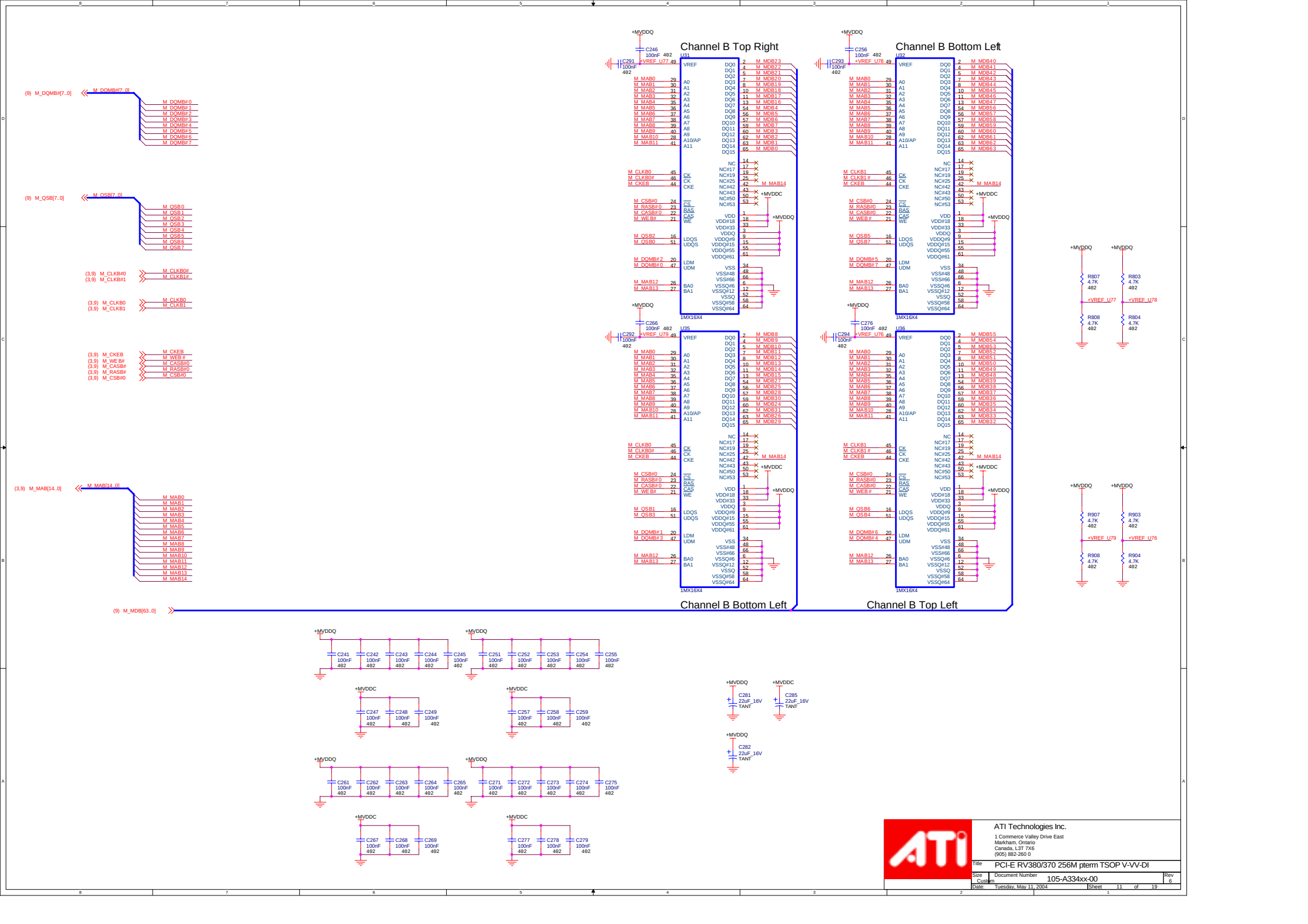
Size: Custom	Document Number: 105-A334xx-00	Rev: 6
Date: Tuesday, May 11, 2004	Sheet 10 of 19	


Channel B Top Right
Channel B Bottom Left
Channel B Bottom Left
Channel B Top Left
(9) M_DQMB#[7..0]
M_DQMB#[7..0]
M_DQMB#0
M_DQMB#1
M_DQMB#2
M_DQMB#3
M_DQMB#4
M_DQMB#5
M_DQMB#6
M_DQMB#7
(9) M_QSB[7..0]
M_QSB[7..0]
M_QSB0
M_QSB1
M_QSB2
M_QSB3
M_QSB4
M_QSB5
M_QSB6
M_QSB7
(3,9) M_CLKB#0
(3,9) M_CLKB#1
M_CLKB0#
M_CLKB1#
(3,9) M_CLKB0
(3,9) M_CLKB1
M_CLKB0
M_CLKB1
(3,9) M_CKEB
(3,9) M_WE B#
(3,9) M_CASB#
(3,9) M_RASB#
(3,9) M_CSB#0
M_CKEB
M_WE B#
M_CASB#0
M_RASB#0
M_CSB#0
(3,9) M_MAB[14..0]
M_MAB[14..0]
M_MAB0
M_MAB1
M_MAB2
M_MAB3
M_MAB4
M_MAB5
M_MAB6
M_MAB7
M_MAB8
M_MAB9
M_MAB10
M_MAB11
M_MAB12
M_MAB13
M_MAB14
(9) M_MDB[63..0]
+MVDDQ
+MVDDC
U31
U32
U35
U36
1MX16X4
C246
C256
C266
C276
C291
C293
C292
C294
100nF
402
+VREF_U77
+VREF_U78
+VREF_U79
+VREF_U76
R807
R803
R808
R804
R907
R903
R908
R904
4.7K
C241
C242
C243
C244
C245
C251
C252
C253
C254
C255
C247
C248
C249
C257
C258
C259
C261
C262
C263
C264
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C271
C272
C273
C274
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C267
C268
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C277
C278
C279
C281
C282
C285
22uF_16V
TANT
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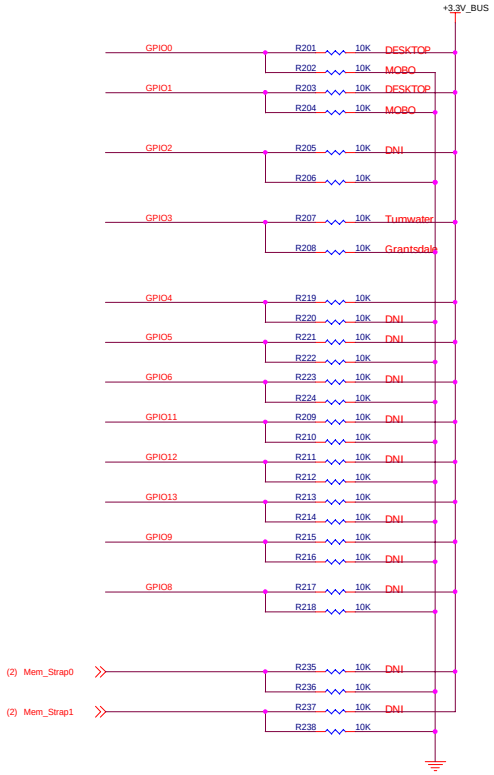
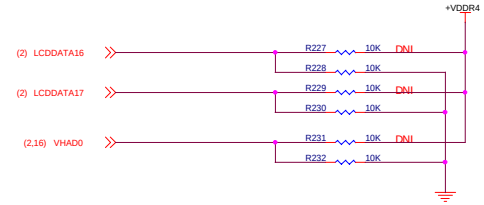
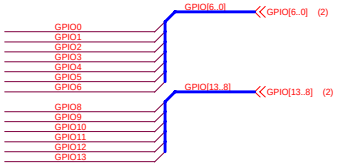
PCI-E RV380/370 256M pterm TSOP V-VV-DI
Size
Custom
Document Number
105-A334xx-00
Rev
6
Date:
Tuesday, May 11, 2004
Sheet
11
of
19

OPTION STRAPS





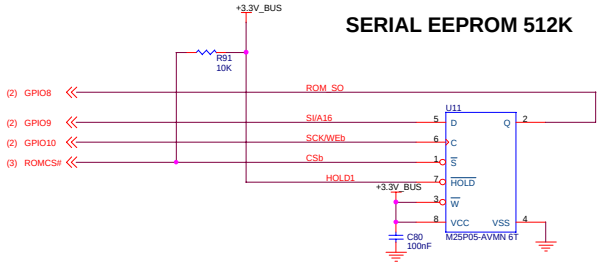


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_EN B	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_E N	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Turnwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PT X_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_B W	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K



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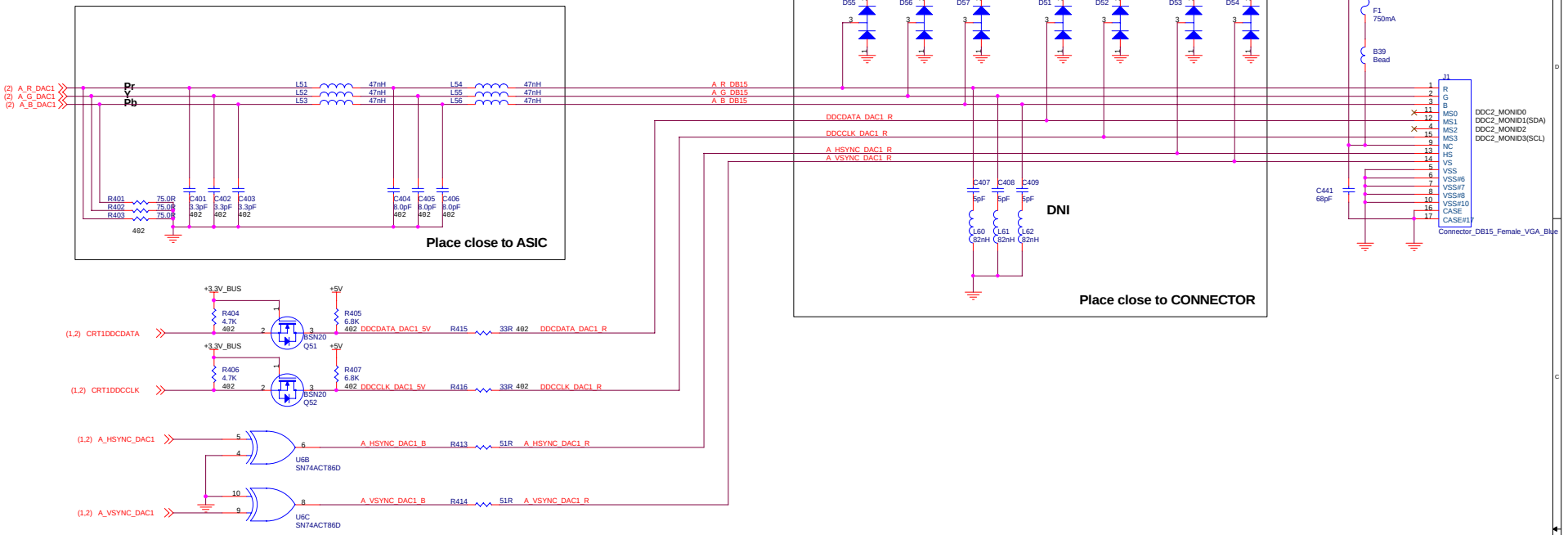
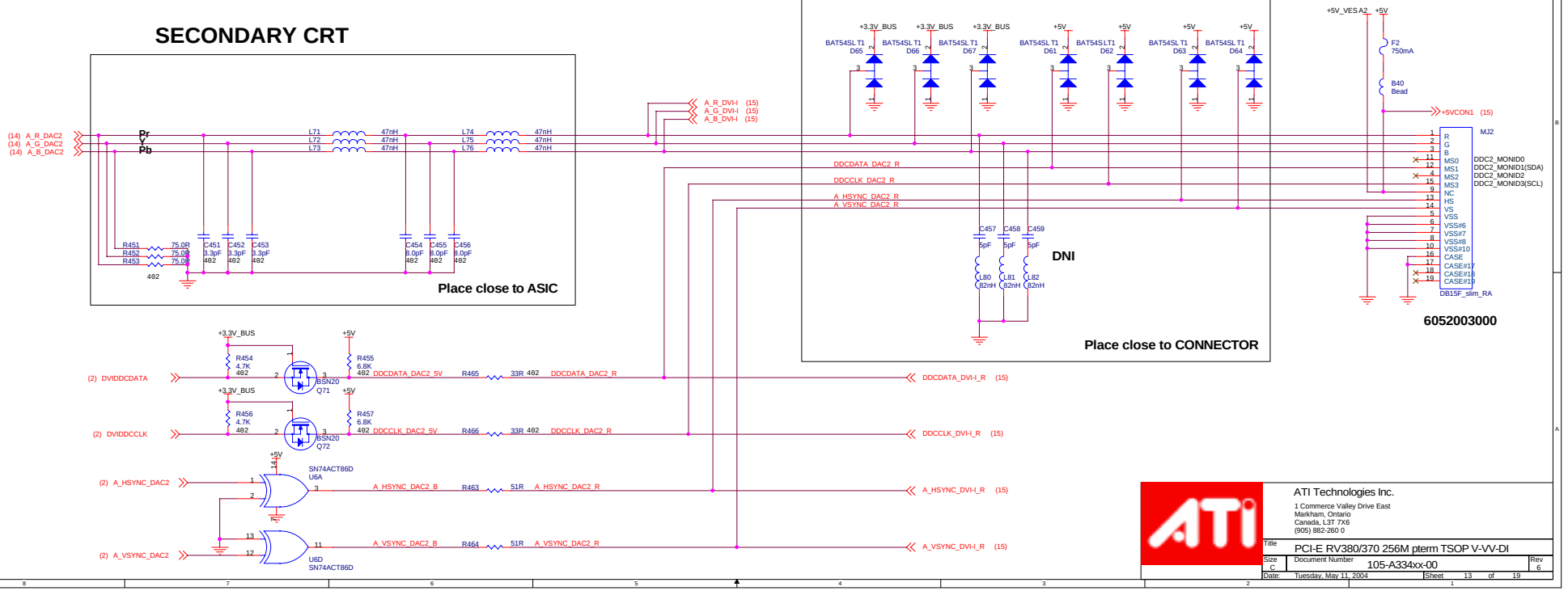
Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI	
Size: Custom	Document Number: 105-A334xx-00	Rev: 6
Date: Tuesday, May 11, 2004	Sheet 12 of 19	

PRIMARY CRT



SECONDARY CRT



Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI
Size	C
Document Number	105-A334xx-00
Rev	6
Date:	Tuesday, May 11, 2004
Sheet	13 of 19

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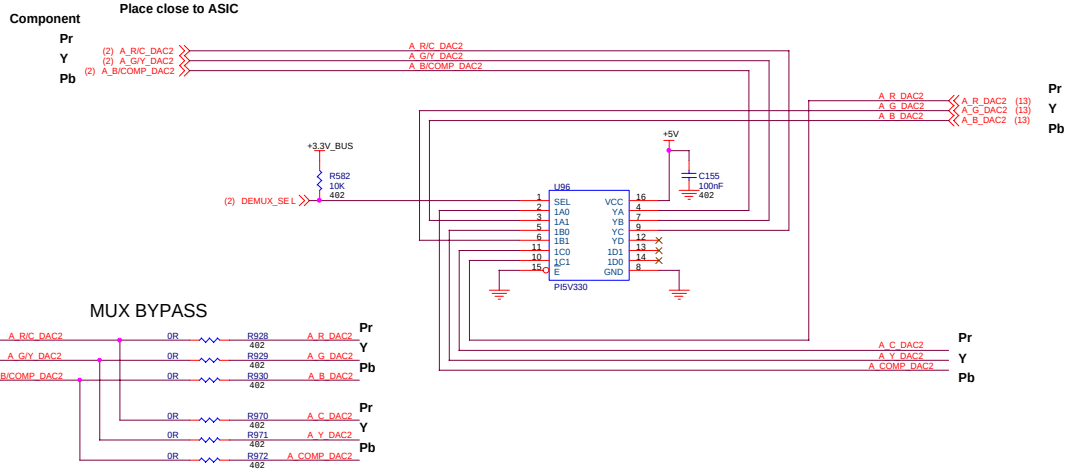

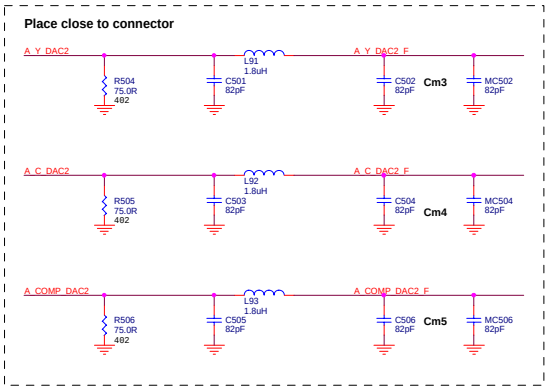

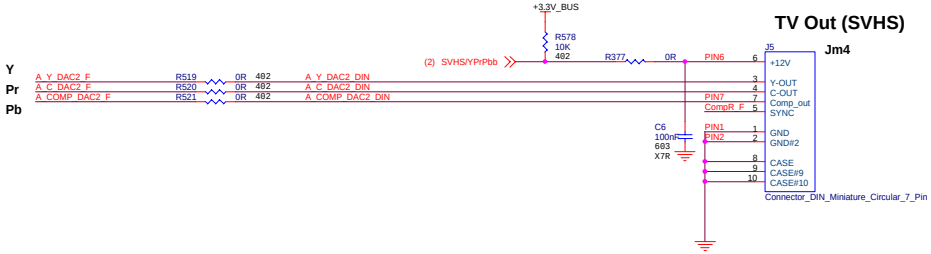

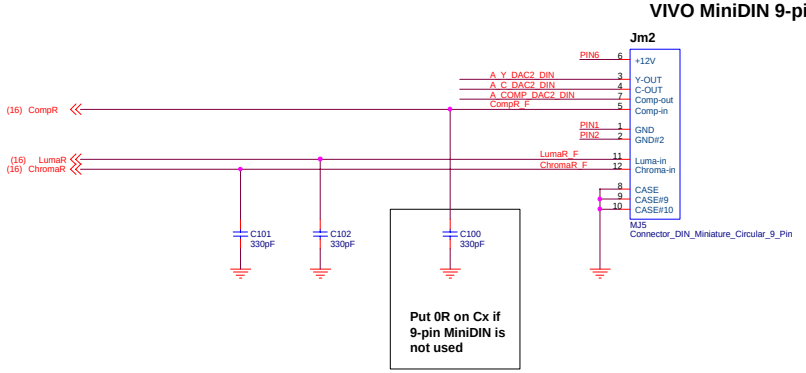

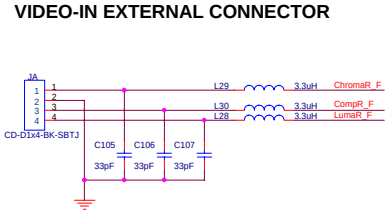

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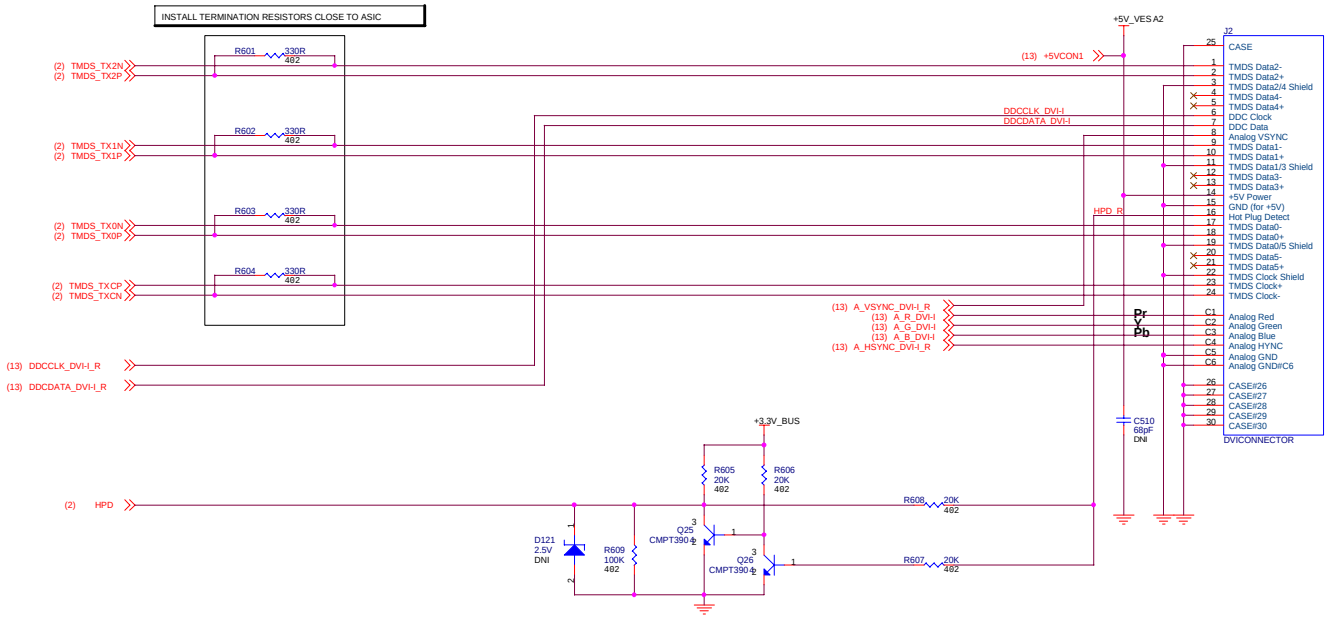
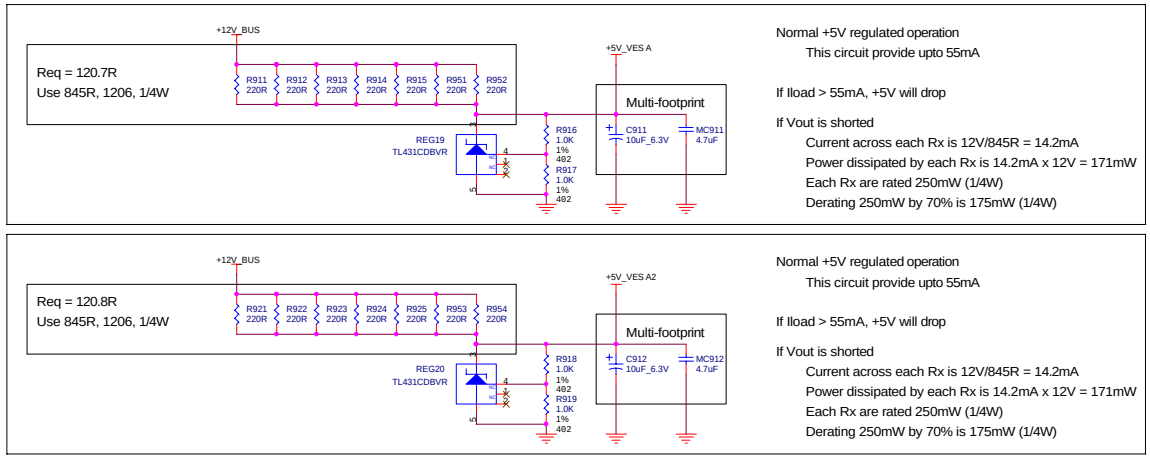
Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI	
Size C	Document Number 105-A334xx-00	Rev 6
Date: Tuesday, May 11, 2004	Sheet 14 of 19	

PRIMARY DVI-I CONNECTOR





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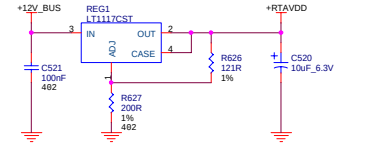
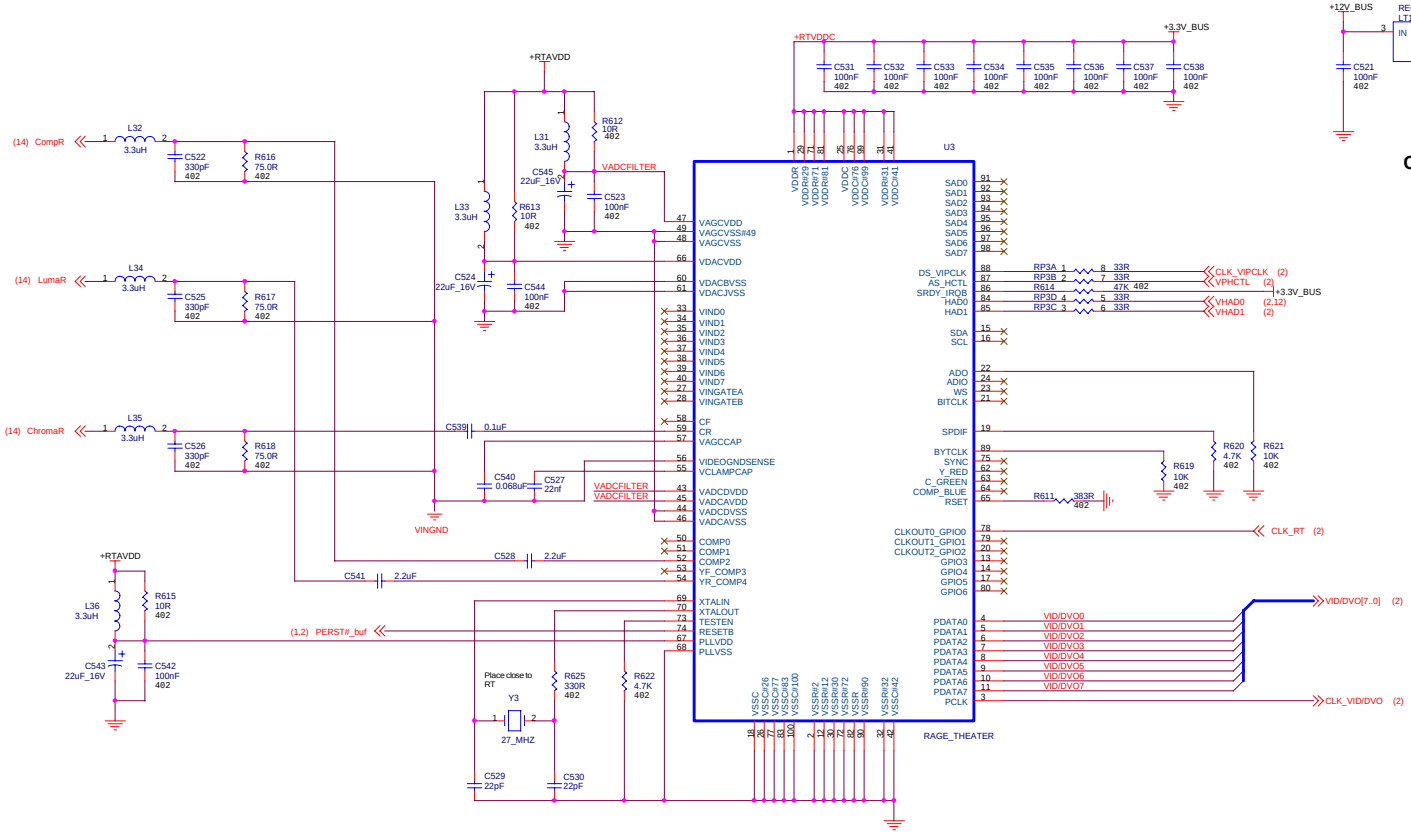
Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI	
Size: Custom	Document Number: 105-A334xx-00	Rev: 6
Date: Tuesday, May 11, 2004	Sheet 15 of 19	

+RTAVDD
Vout = 3.3V
Iout = 125mA MAX, 80mA RMS



Change to 1%



Footprint can be replaced with zero ohm or other.

IMPORTANT

Put 2D line as close as possible to pin 56 of Rage Theater

Layout Guide line of THEATER

#1 : C27 and C28 have to be placed as close as possible to the respective pins of Rage THEATER

#2 : VINGND should be seperated from Digital or Chassis Ground and have no loops

#3 : VINGND should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

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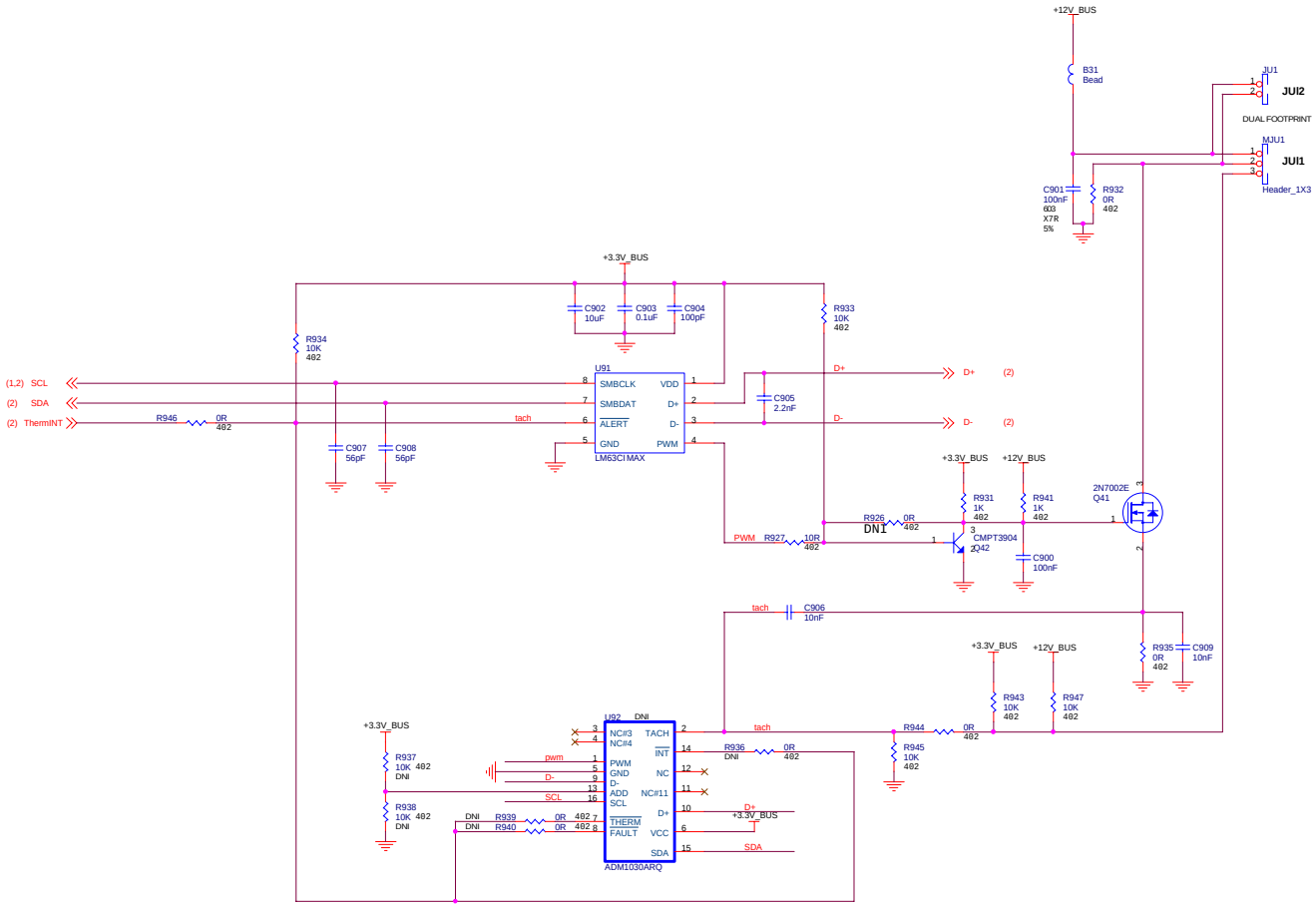
Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI	
Size: Custom	Document Number: 105-A334xx-00	Rev: 6
Date: Tuesday, May 11, 2004	Sheet 16 of 19	

TEMPERATURE SENSE AND SPEED CONTROLLED FAN



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Size: Custom	Document Number: 105-A334xx-00		Rev: 6
Date: Tuesday, May 11, 2004	Sheet 17 of 19		

ASSY1
SCREW
JACKSCREW

ASSY3
SCREW
JACKSCREW

ASSY2
SCREW
JACKSCREW

ASSY4
SCREW
JACKSCREW

H101
heatsink
7120005 800

MH101
HEATSINK

H100
HEATSINK
7120005 100
Spring push-pin

MH100
HEATSINK
7120008 000
ITW push-pin

FD3
MT_Hole_0.136_in.

FD7
MT_Hole_0.136_in.

FD1
MT_Hole_0.136_in.

FD6
MT_Hole_0.136_in.

FD9
MT_Hole_0.136_in.

FD4
MT_Hole_0.136_in.

FD2
MT_Hole_0.136_in.

FD8
MT_Hole_0.136_in.

FD5
MT_Hole_0.136_in.

M1
MT_Hole_0.136_in.

M2
MT_Hole_0.136_in.

MT1
MT_Hole_0.136_in.

MT1
MT_Hole_0.136_in.

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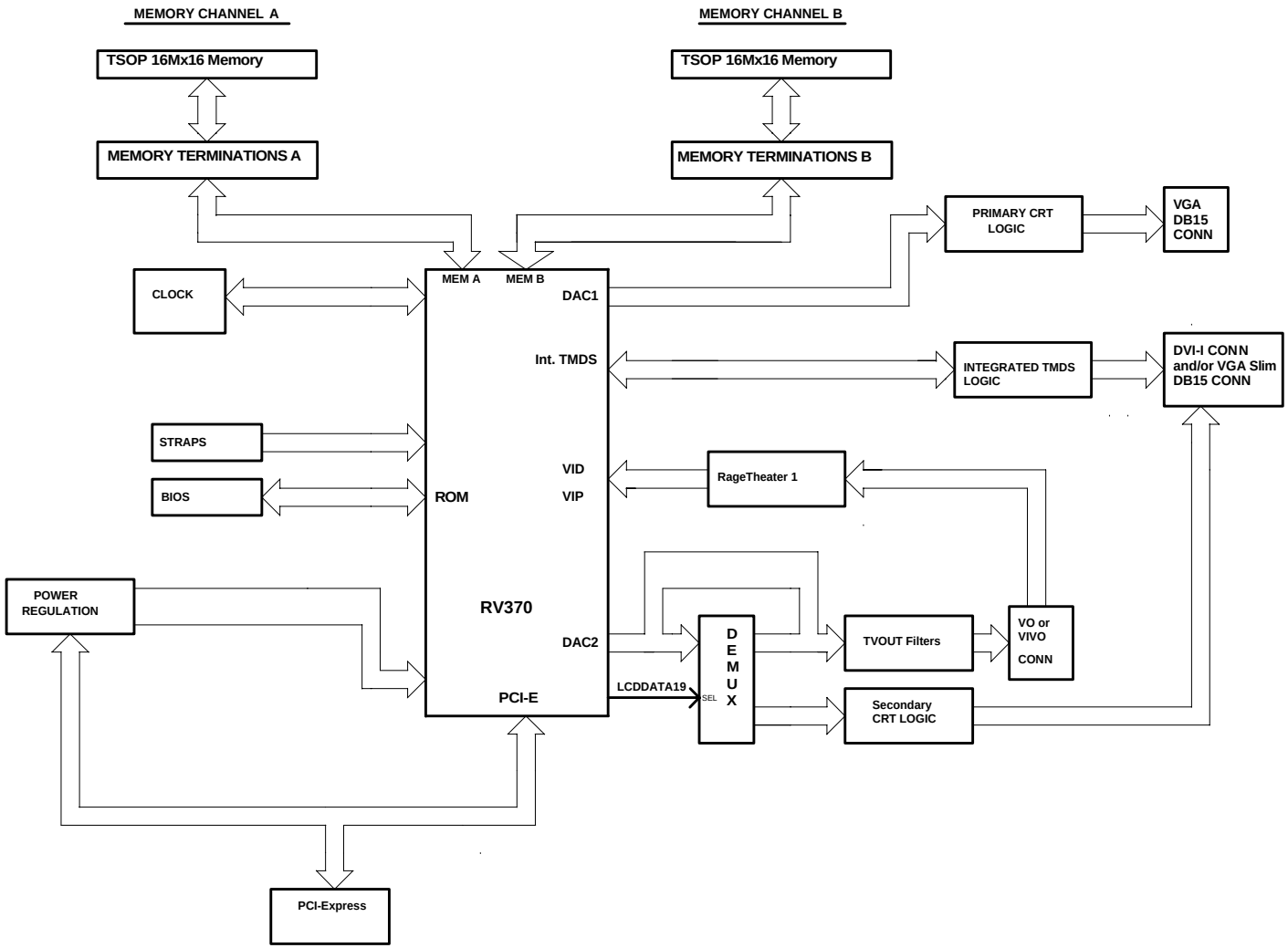
Size: C | Document Number: 105-A334xx-00 | Rev: 6

Date: Tuesday, May 11, 2004 | Sheet 18 of 19



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Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI	
Size C	Document Number 105-A334xx-00	Rev 6
Date: Tuesday, May 11, 2004	Sheet 19 of 19	