

PCI-EXPRESS EDGE CONNECTOR

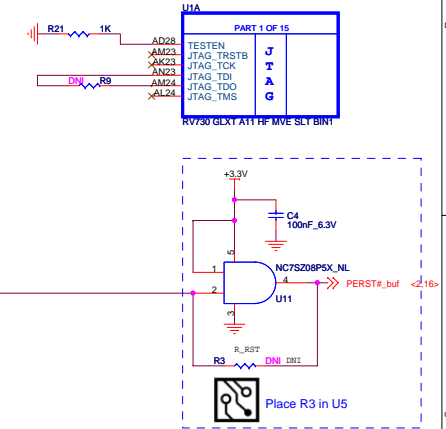
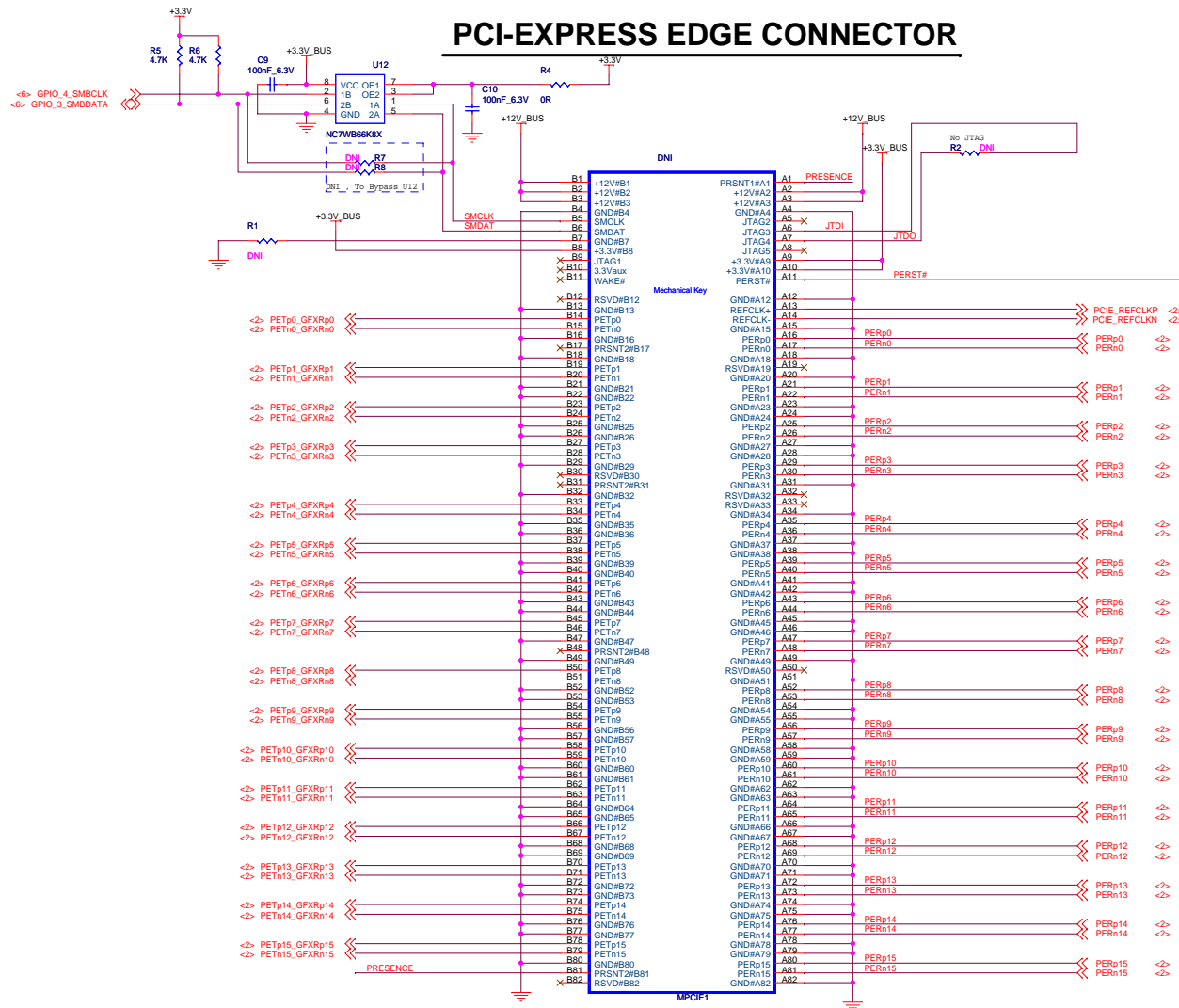
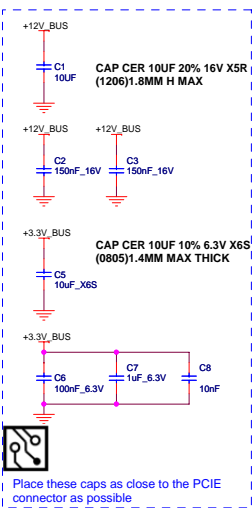
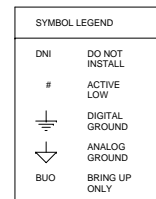


Table 1: Connection for JTAG

Production (No JTAG)	Install R1, R2 & Don't Install TSW1	
Internal Use Only	Install TSW1 & Don't Install R1 & R2	
	JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open
	NO JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.



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Date: Monday, October 06, 2008
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Rev 0

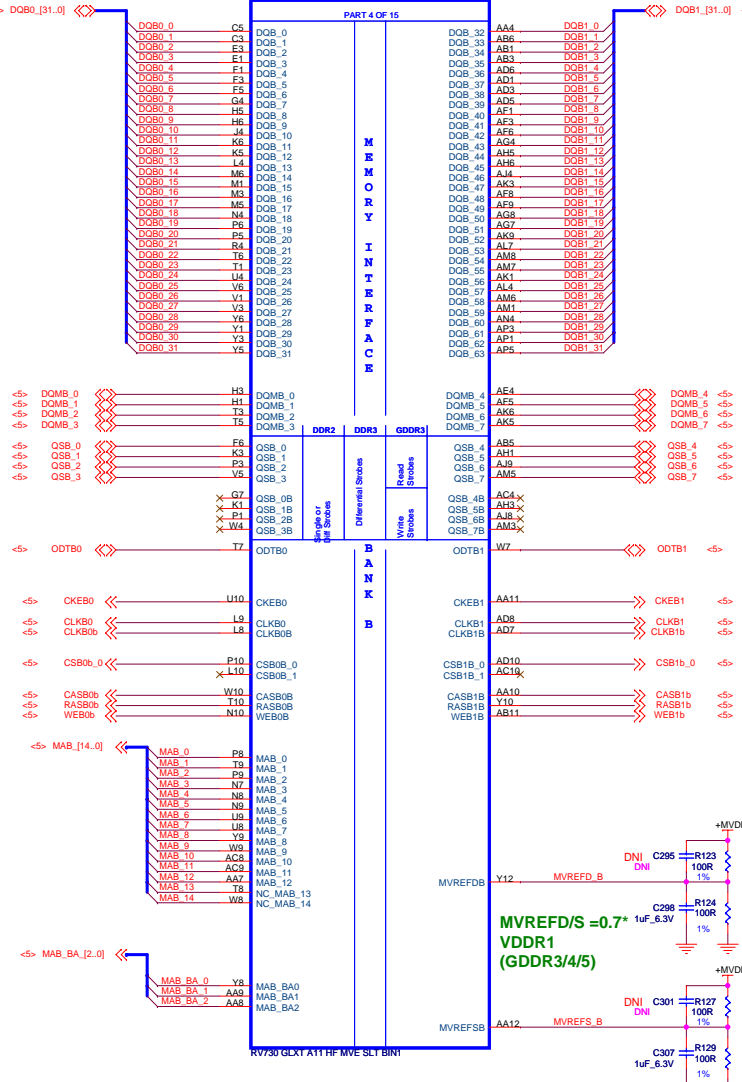
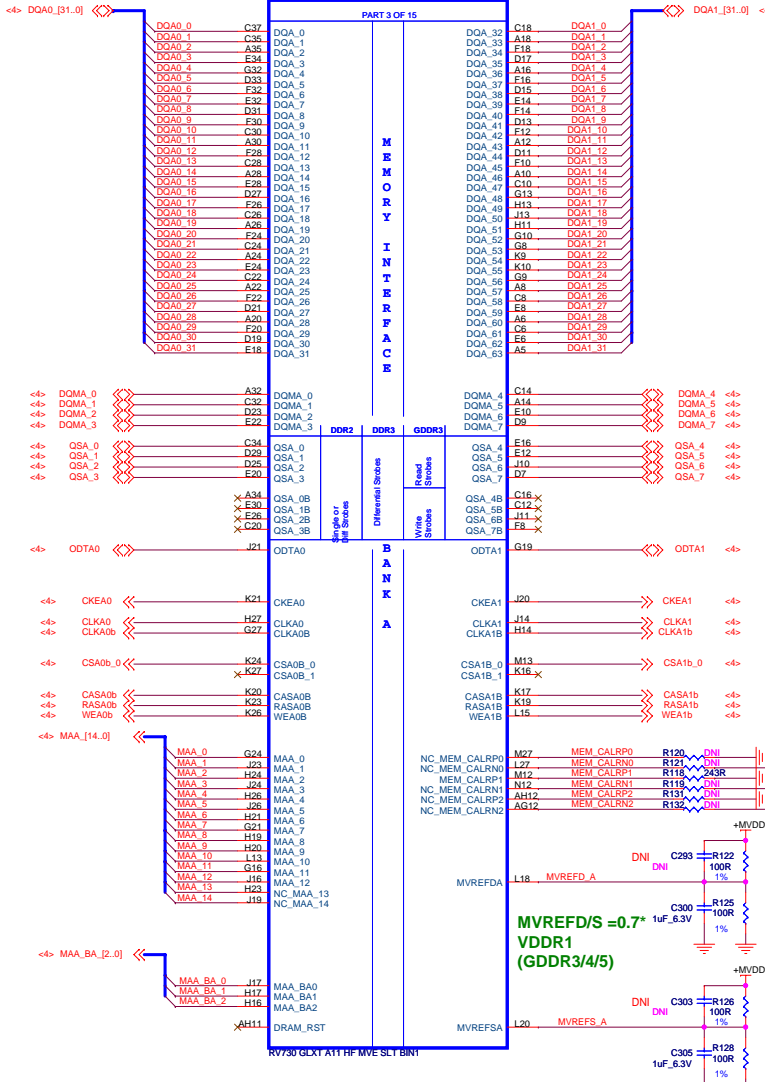
Title **BH RV730 512MB DDR2 DL-DVI DP HDMI FH 6'**

Doc No. 105-B665xx-00A

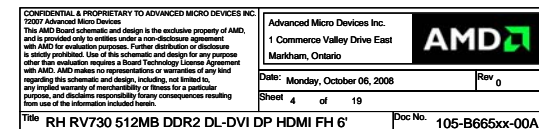


Title	RH RV730 512MB DDR2 DL-DVI DP HDMI FH 6'	Doc No.	105-B665xy-00A
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(3) RV730 MEM Interface Ch A&B

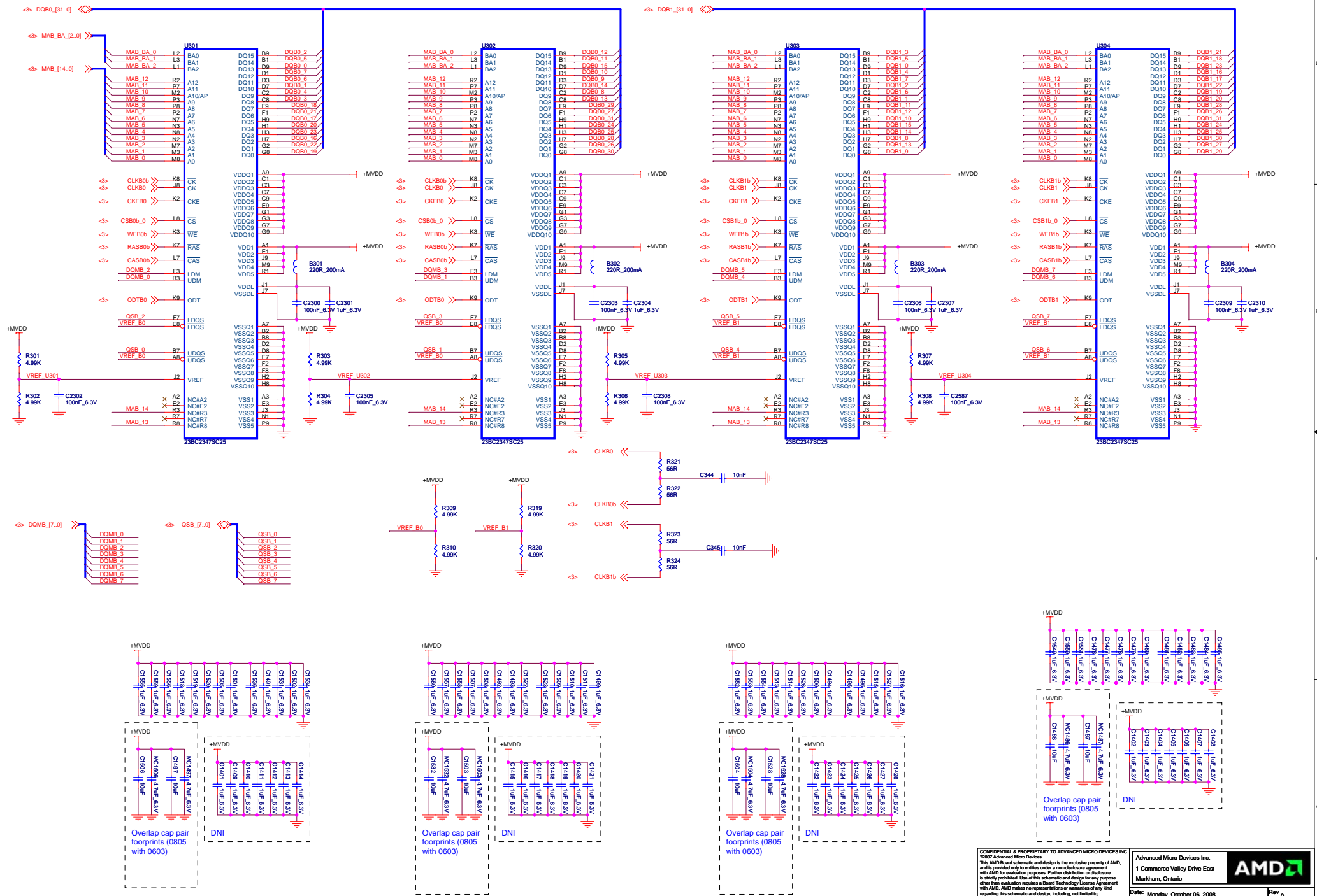


CHANNEL A: 128MB/256MB DDR2

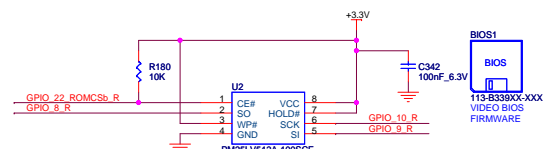
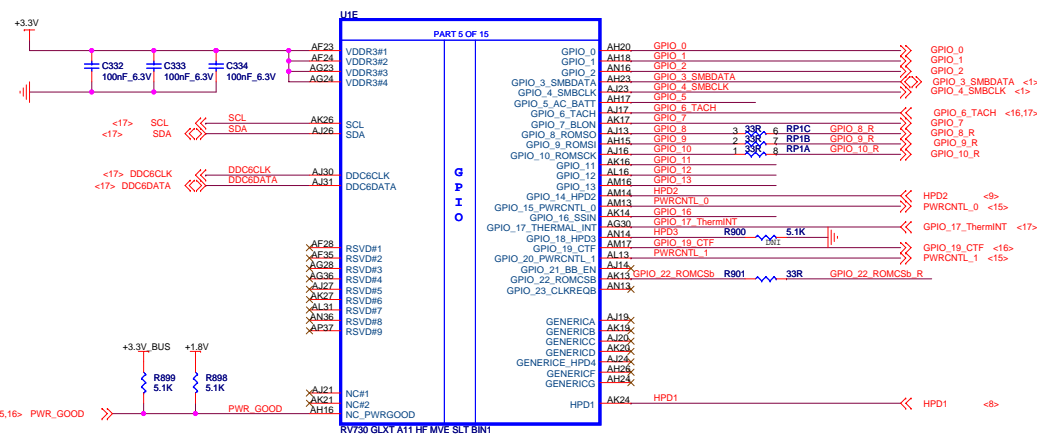


(5) DDR2 Ch B

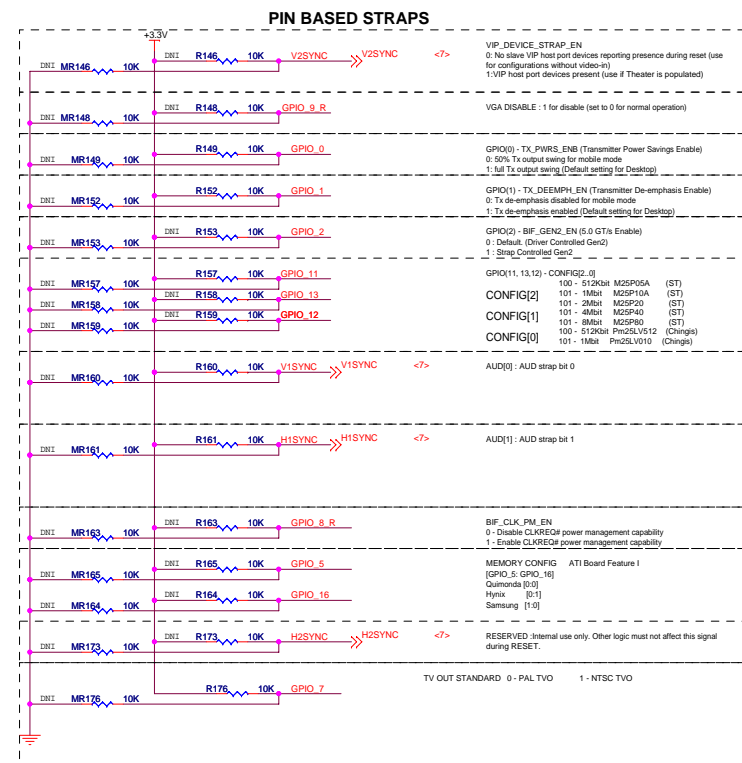
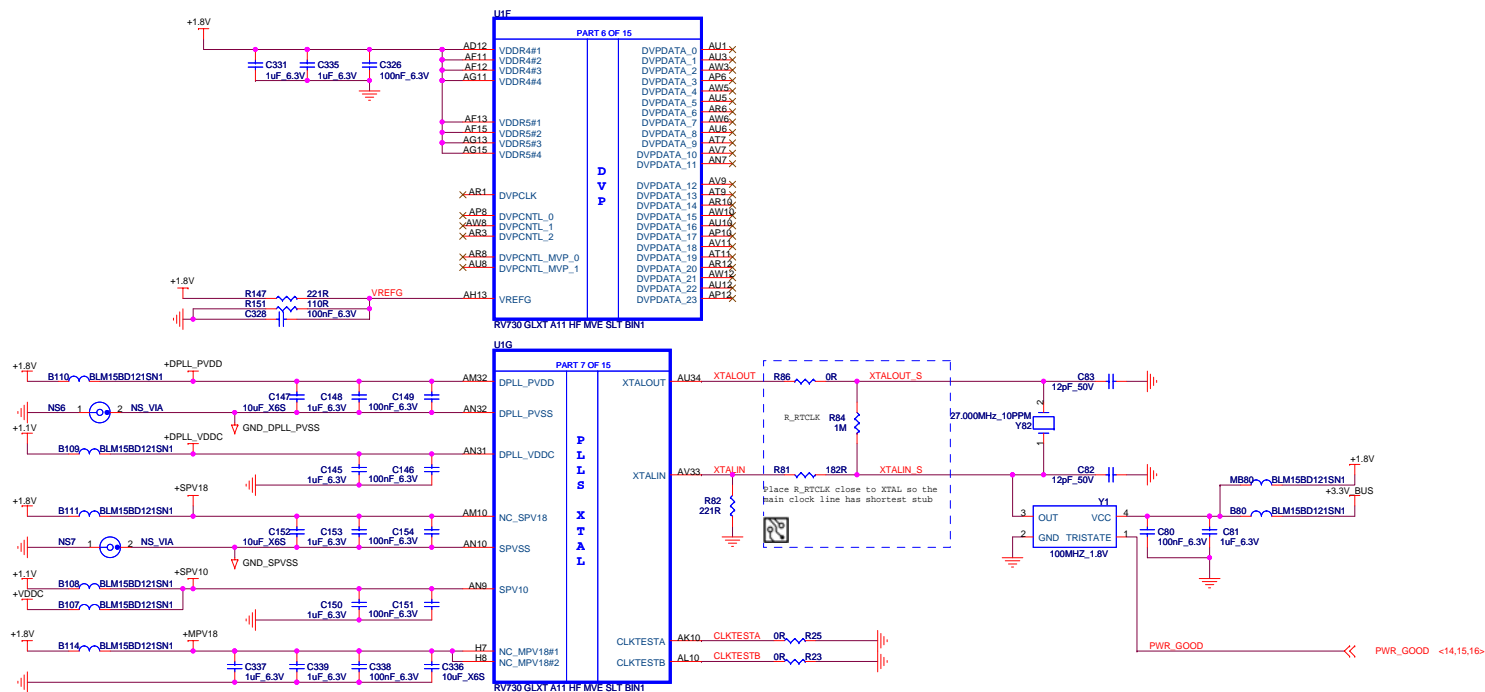
CHANNEL B: 128MB/256MB DDR2



(06) RV730 GPIOs Strap CF XTAL



PN 2280007900G for 1Mbit (PM25LV010A-100SCE)



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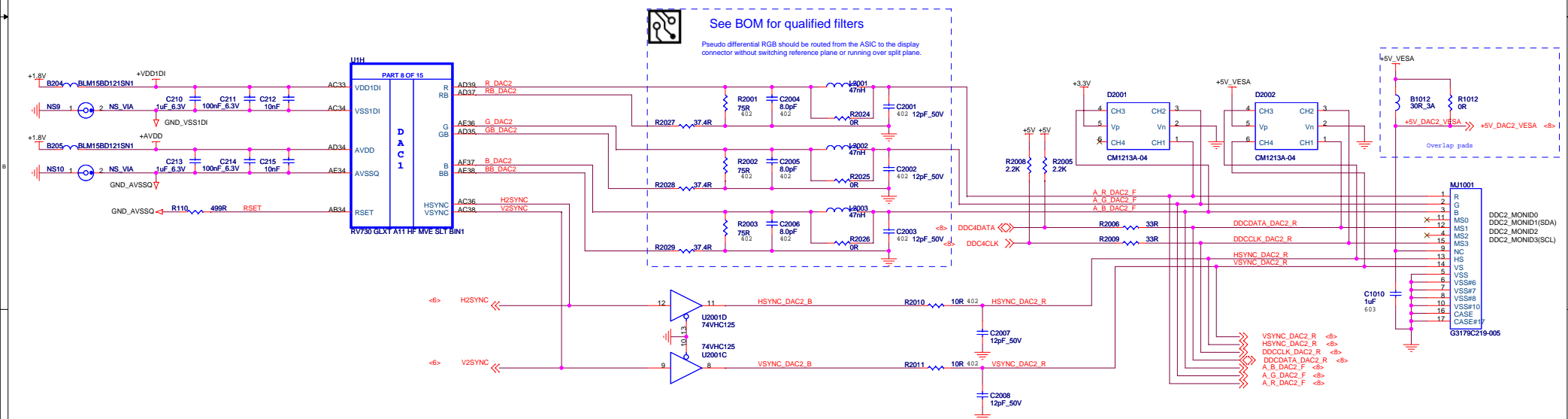
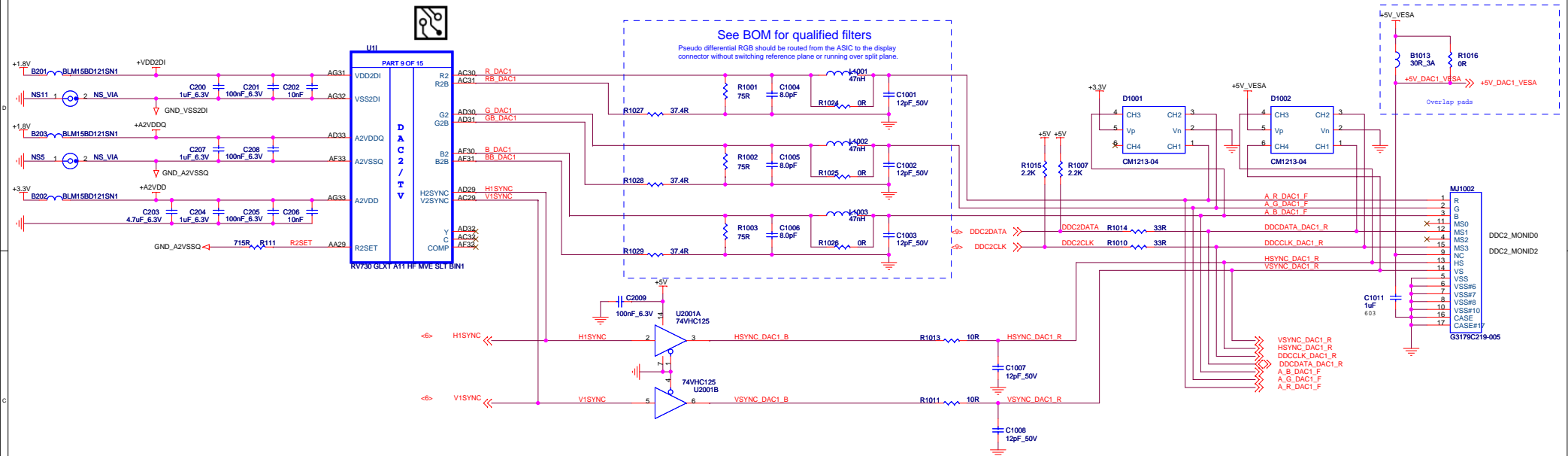
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Title **RH RV730 512MB DDR2 DL-DV/DL DR HDMI FH 6'**

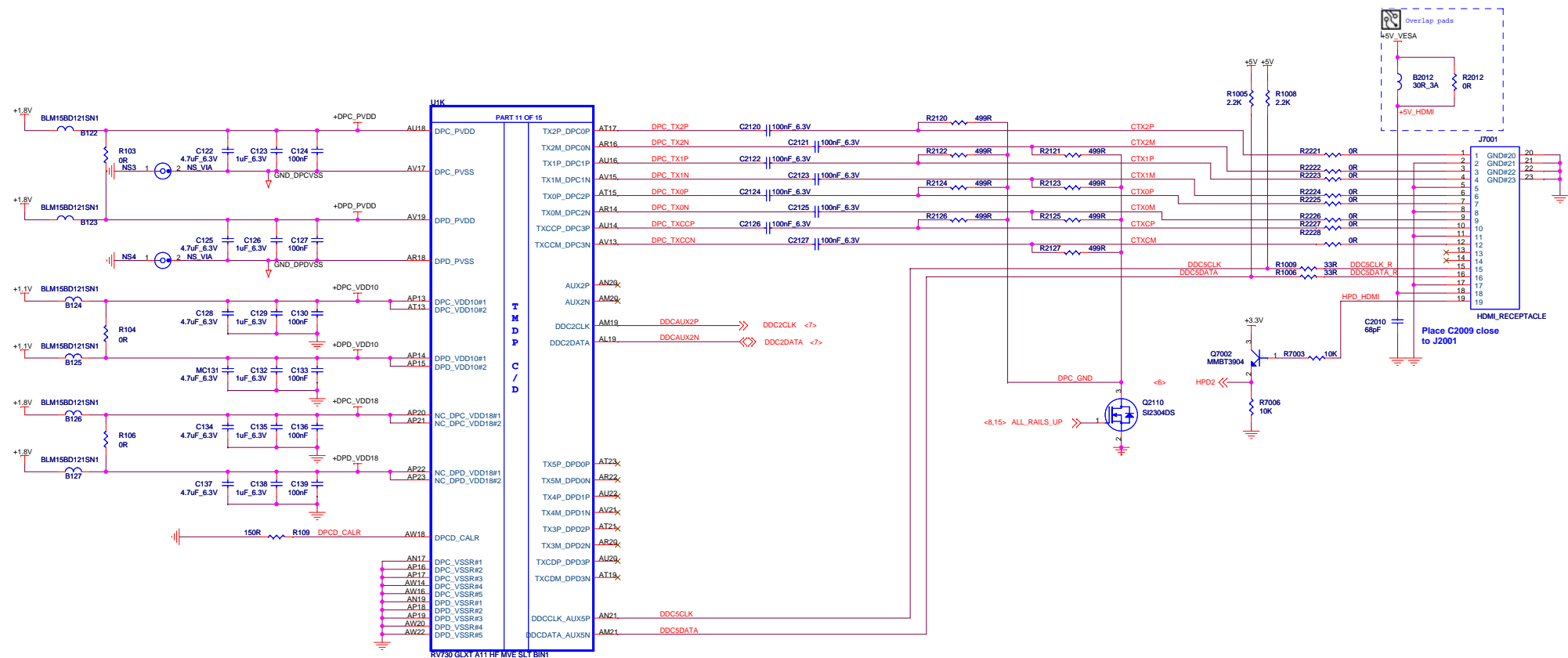
Doc No. 105-B665xx-004

(07) RV730 DAC1 and DAC2/TV

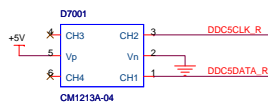
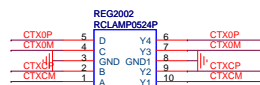
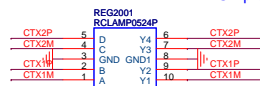




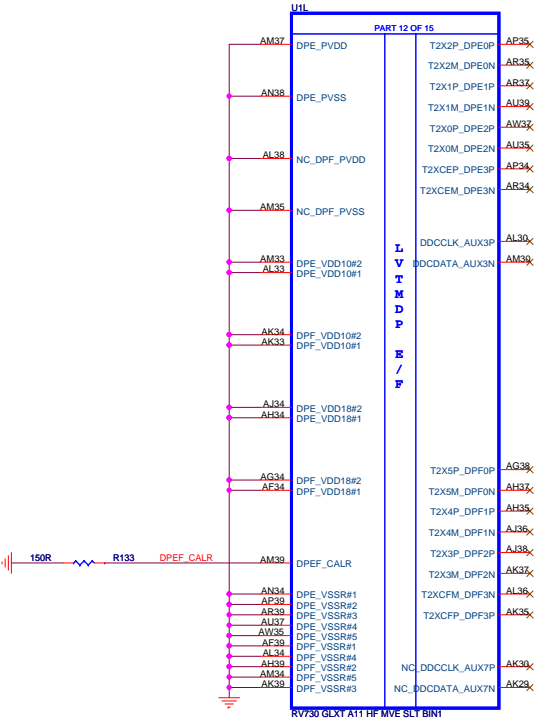
(09) RV730 HDMI and DisplayPort on C&D



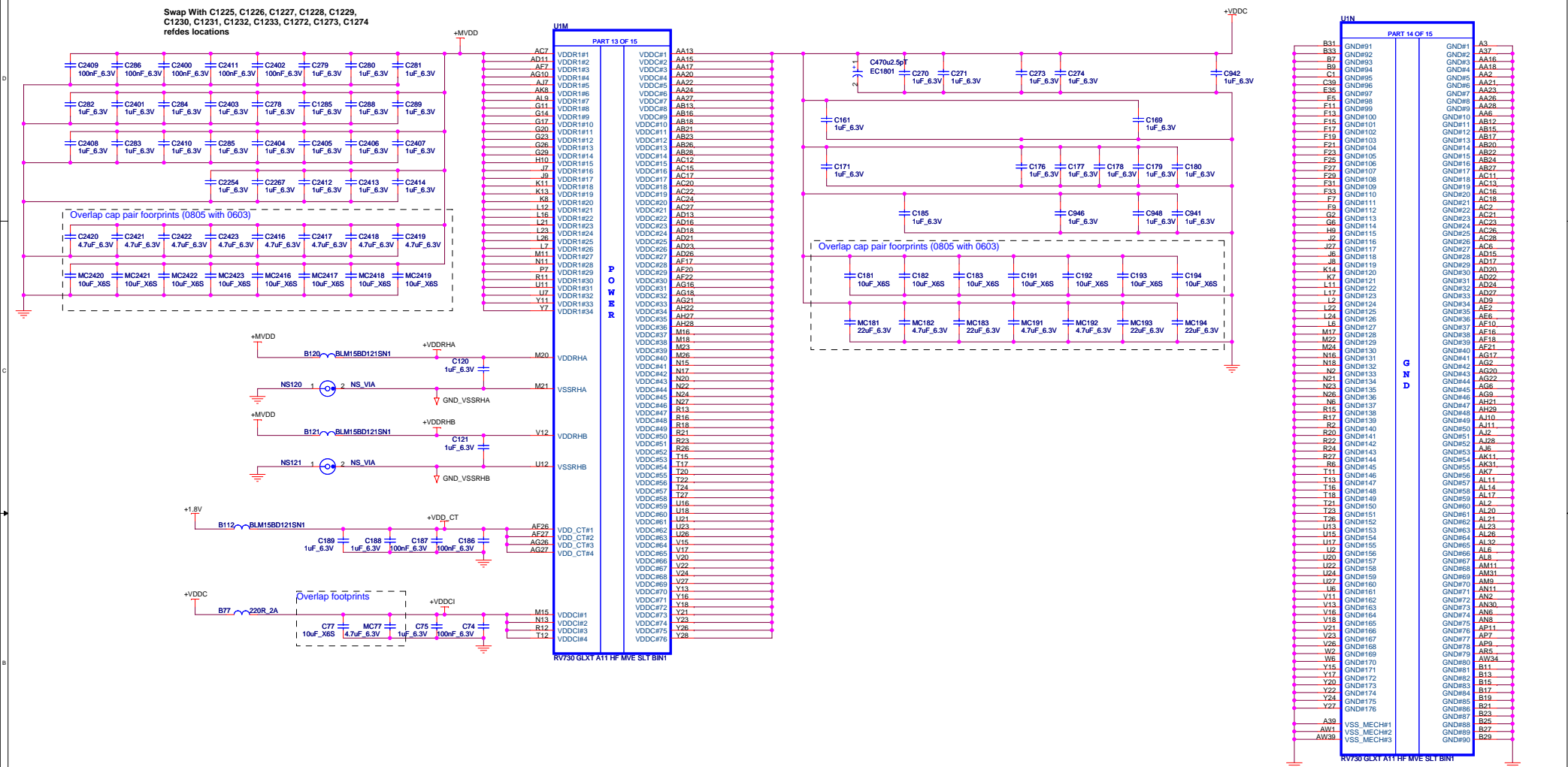
ESD protection diodes



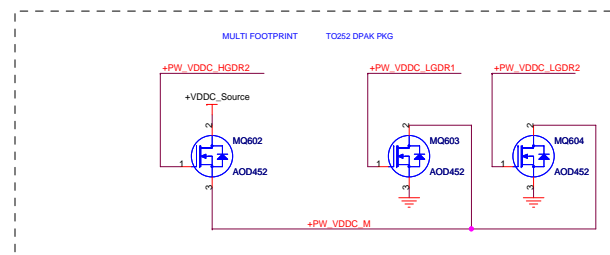
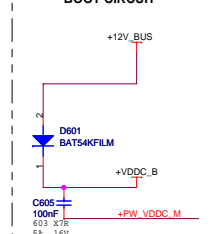
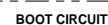
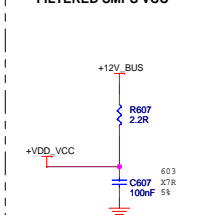
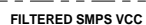
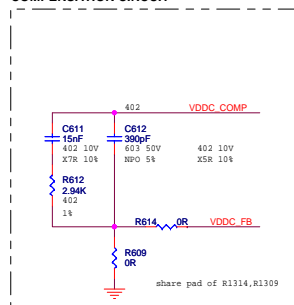
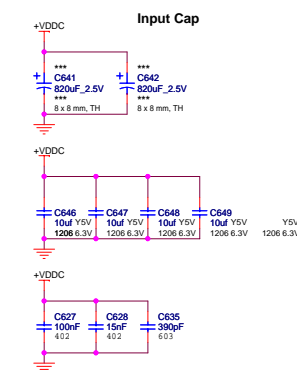
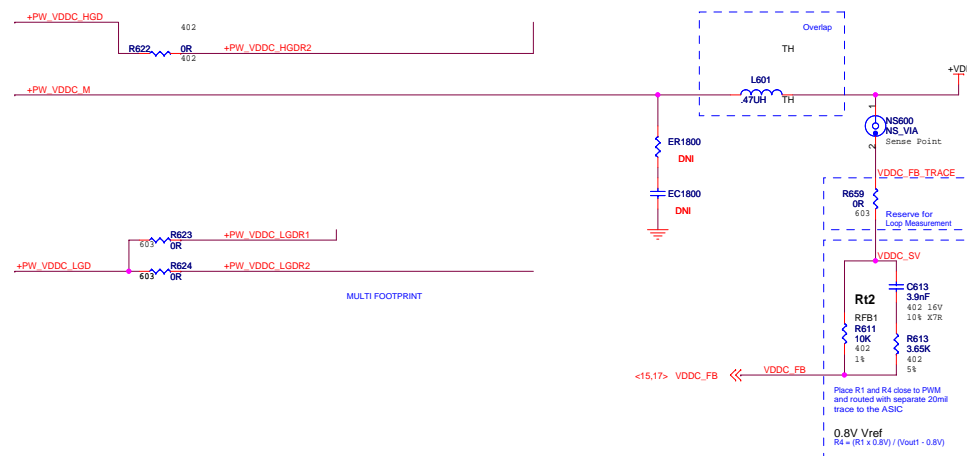
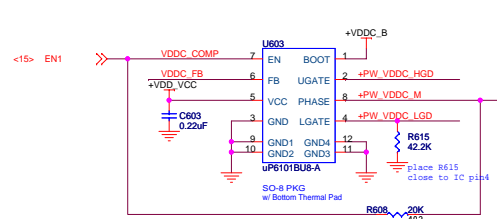
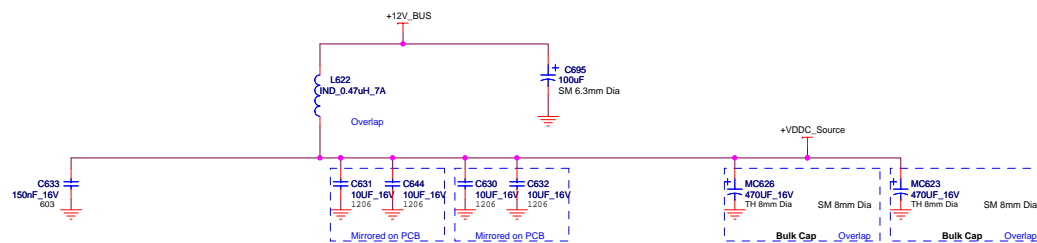
(10) No Connect E&F



(11) RV730 Power & GND



(12) VDDC



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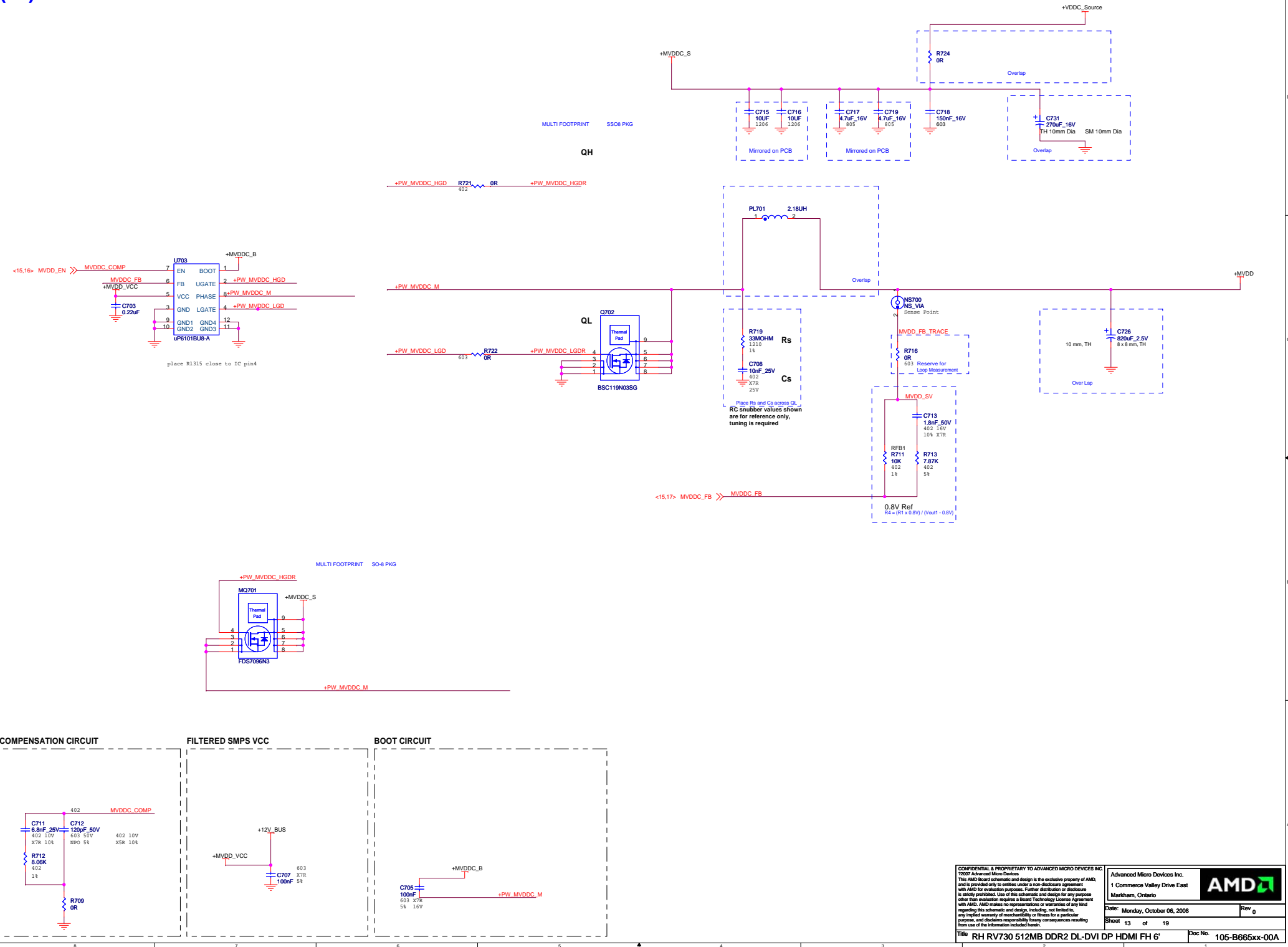
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Title		RH RV730 512MB DDR2 DL-DVI DP HDMI FH 6	
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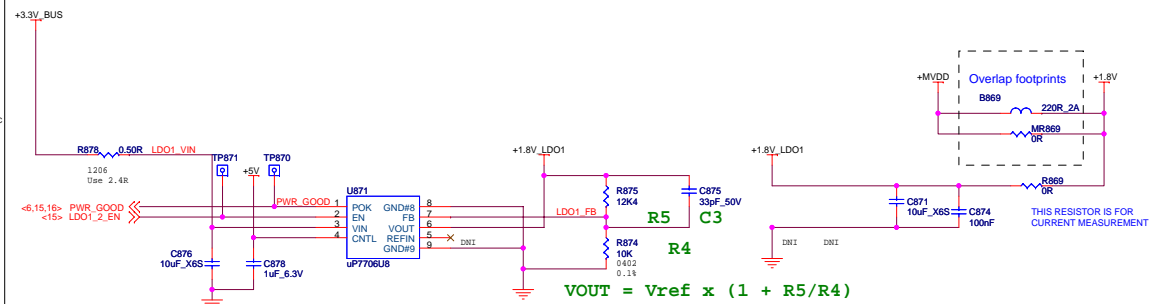
Doc No.	105-B665xx-00A
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(13) MVDD

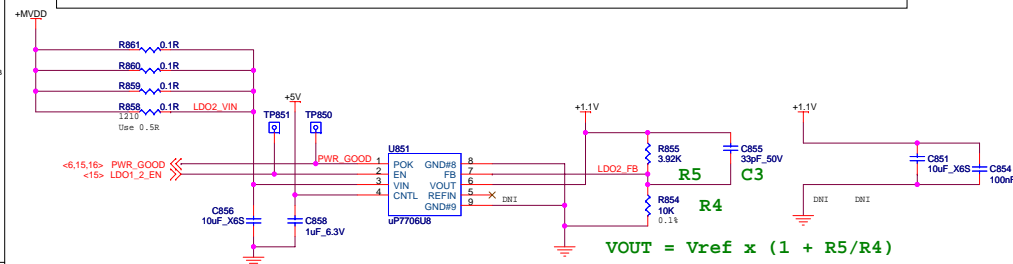


(14) Linear Regulators

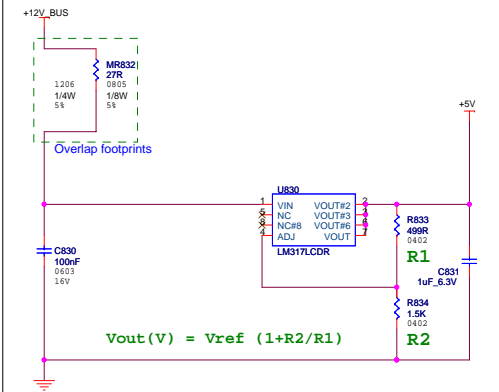
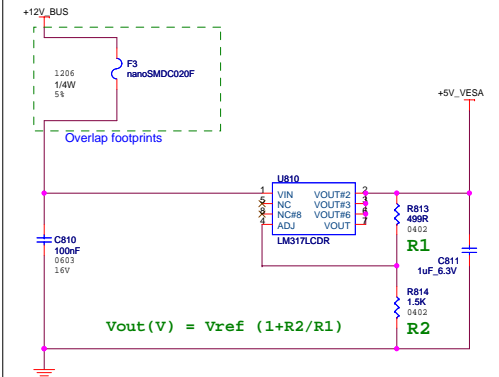
LDO #1: Vin = 3.0V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 1.0A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #2: Vin = +1.5V to 2.0VMAX Vout = +1.1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling




Regulators for +5V, +5V_VESA and +5V_VESA2



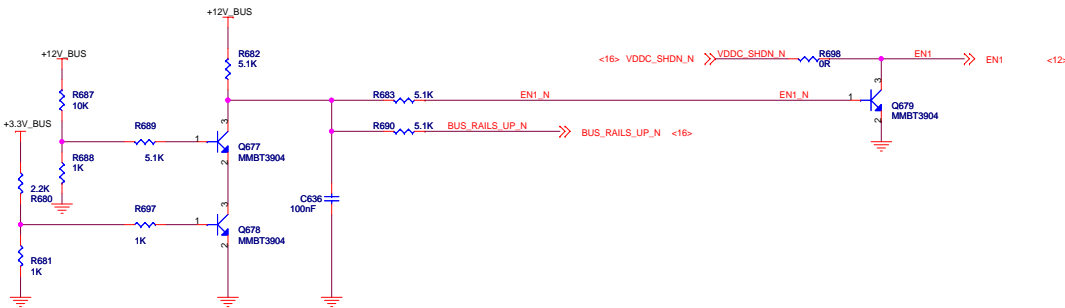
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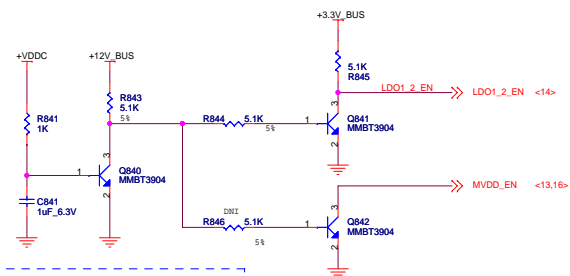
<p>Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario</p>			
<p>Date: Monday, October 06, 2008</p>		<p>Rev 0</p>	
<p>Sheet 14 of 19</p>			
<p>1 DP HDMI FH 6'</p>		<p>Doc No. 105-B665xx-00A</p>	

(15) Power Management

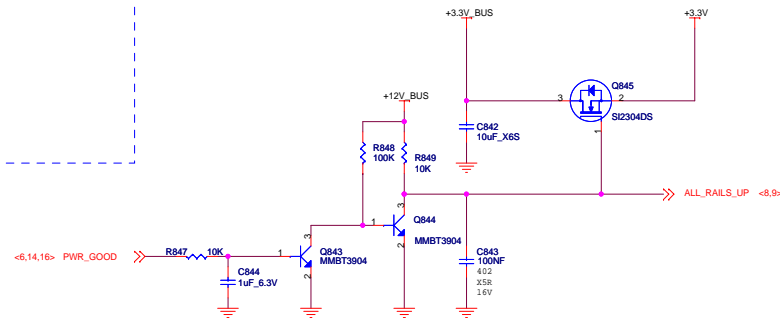
Power up Sequencing



VDDC Enable Circuit



LDOs and MVDD Enable Circuit



3.3V Enable Circuit

Power Play

VDDC Voltage Settings Using GPIOs (for VDDC1 Dual Phase)

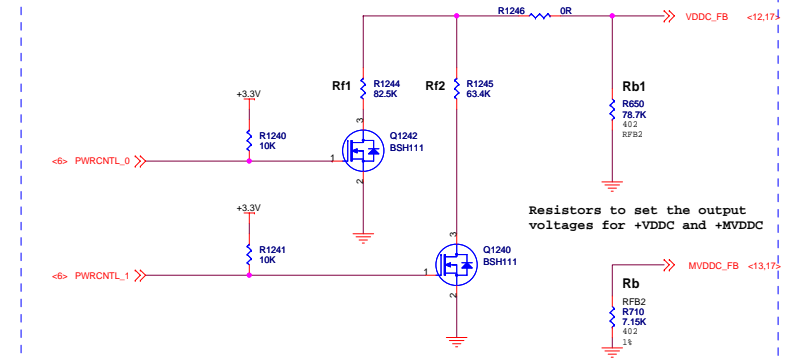
		Output Voltage [V]			
PWRCONTL_1 QF10_20	PWRCONTL_0 QF10_15	Rf1=82.5K Rf2=63.4K	Rf1= Rf2=	Rf1= Rf2=	
0	0	0.90V			
0	1	1.00V			
1	0	1.03V			
1	1	1.125V			Power-up Default

$$V_{out} = V_{ref} * (1 + R_t/R_b)$$

```
VDDC1 (Dual Phase):      Vref = 0.6V, Rt = 5.11K
VDDC2 (Single Phase):    Vref = 0.8V, Rt = 10K
```

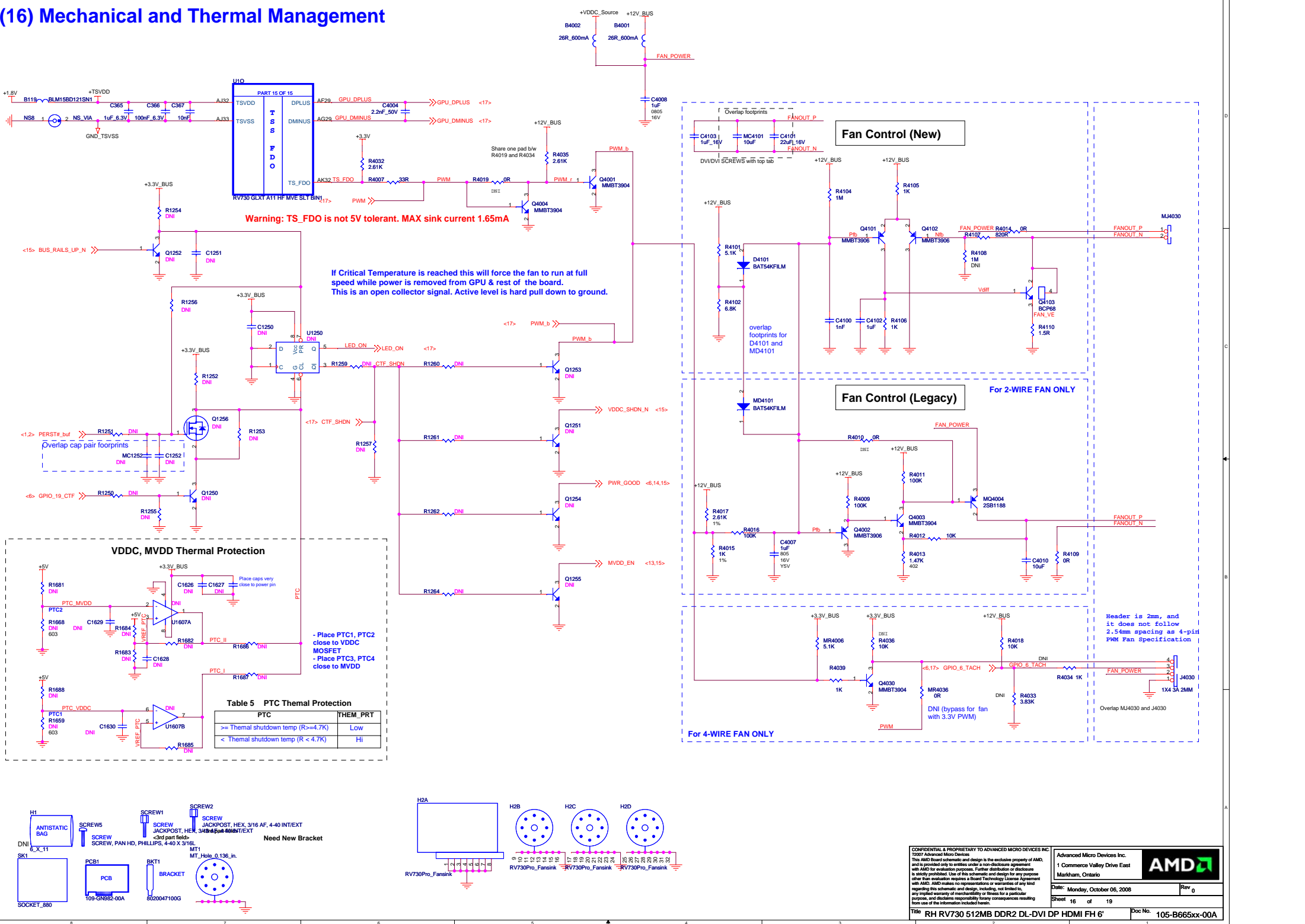
```
VDDC2 (Single Phase):  Vref = 0.8V, Rt = 10K
MDDC (Single Phase):   Vref = 0.8V, Rt = 10K
```

MVDDC (Single Phase): Vref = 0.8V, Rt = 10K



Resistors to set the output
voltages for +VDDC and +MVDDC

(16) Mechanical and Thermal Management



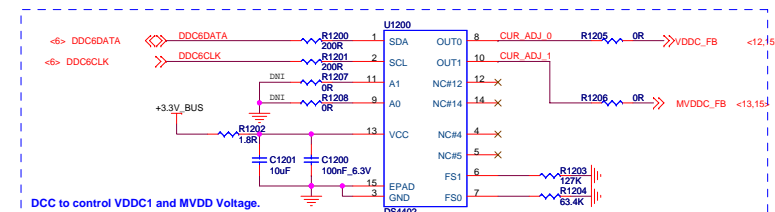
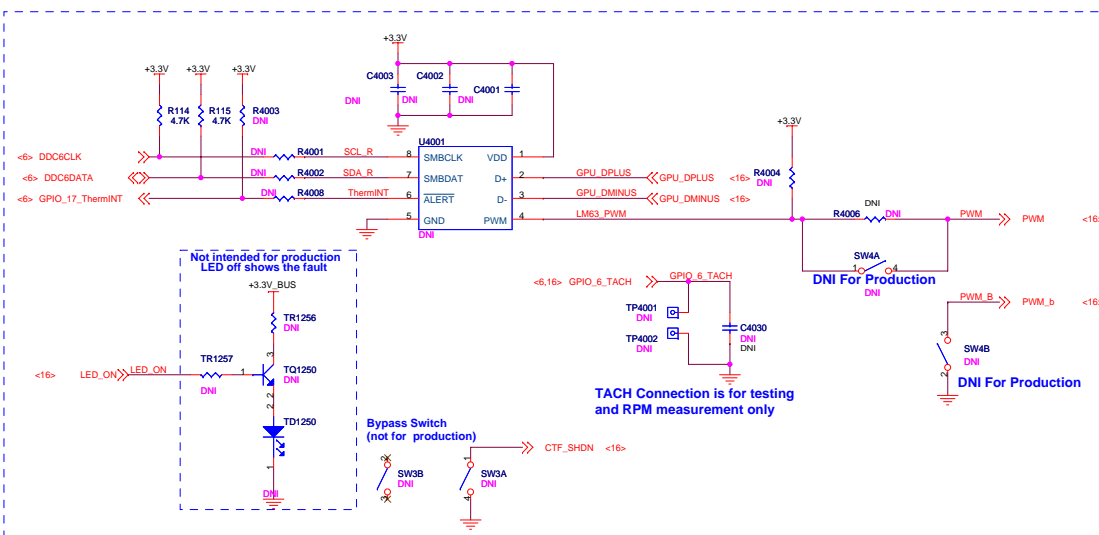
(17) Debug Circuits

In production, this block will not be populated.

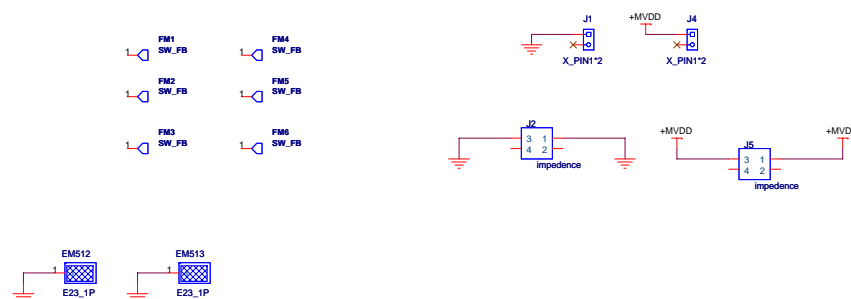
Mating connector: 6010028300G

(HEADER 2X8 1.27MM PITCH, SMD)

When attaching the daughter card (B176) align it by mounting hole.



For Testing purposes only



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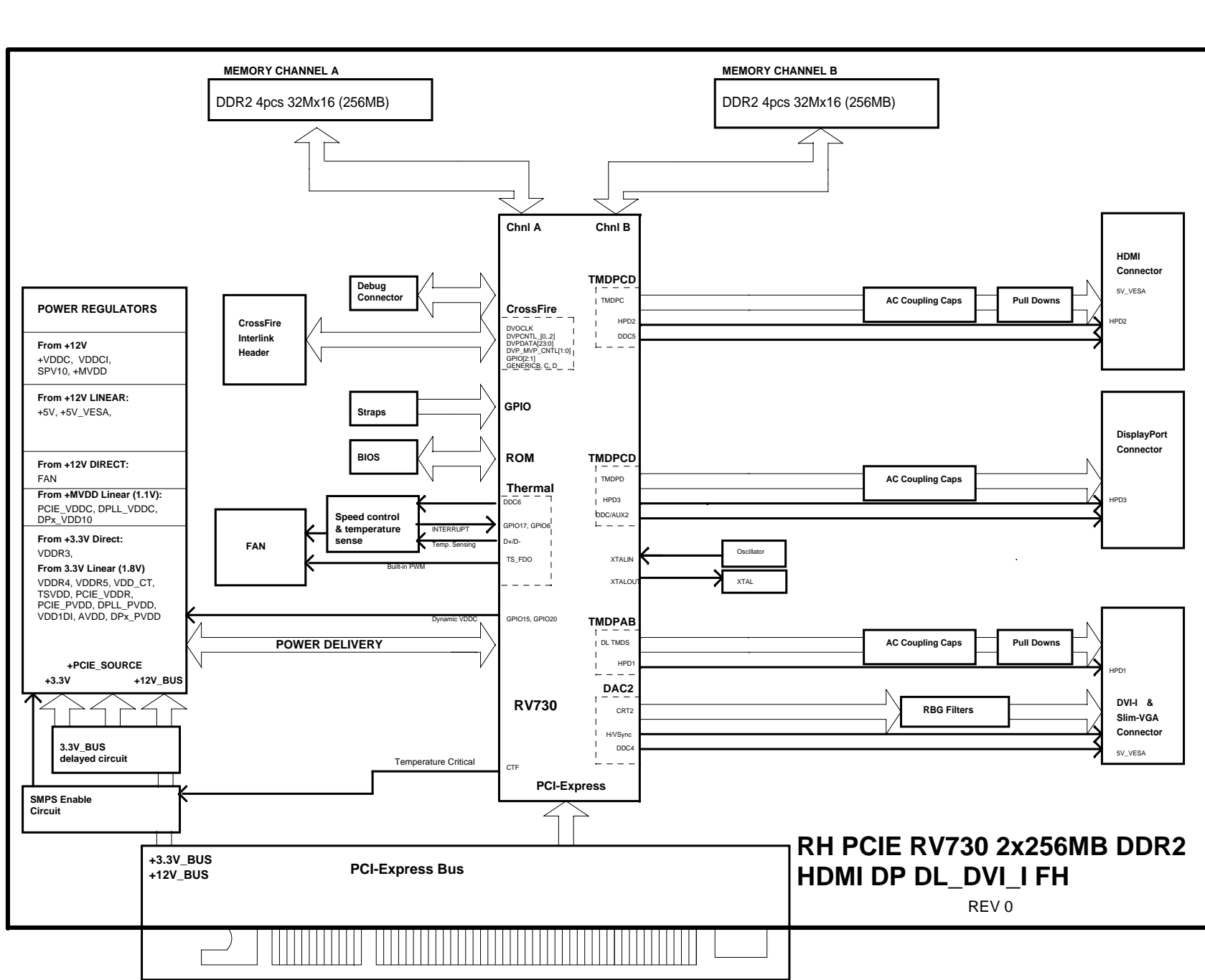


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Rev

Title	RH RV730 512MB DDR2 DL-DVI DP HDMI FH 6'	Doc No.	105-B665xx-00A
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<div>AMD</div>			Title		Schematic No.		Date:	
			RH RV730 512MB DDR2 DL-DVI DP HDMI FH 6'		105-B665xx-00A		Saturday, July 26, 2008	
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.					Rev 0
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION					
0	00A	08/04/01	Initial design for RV730 GDDR3					