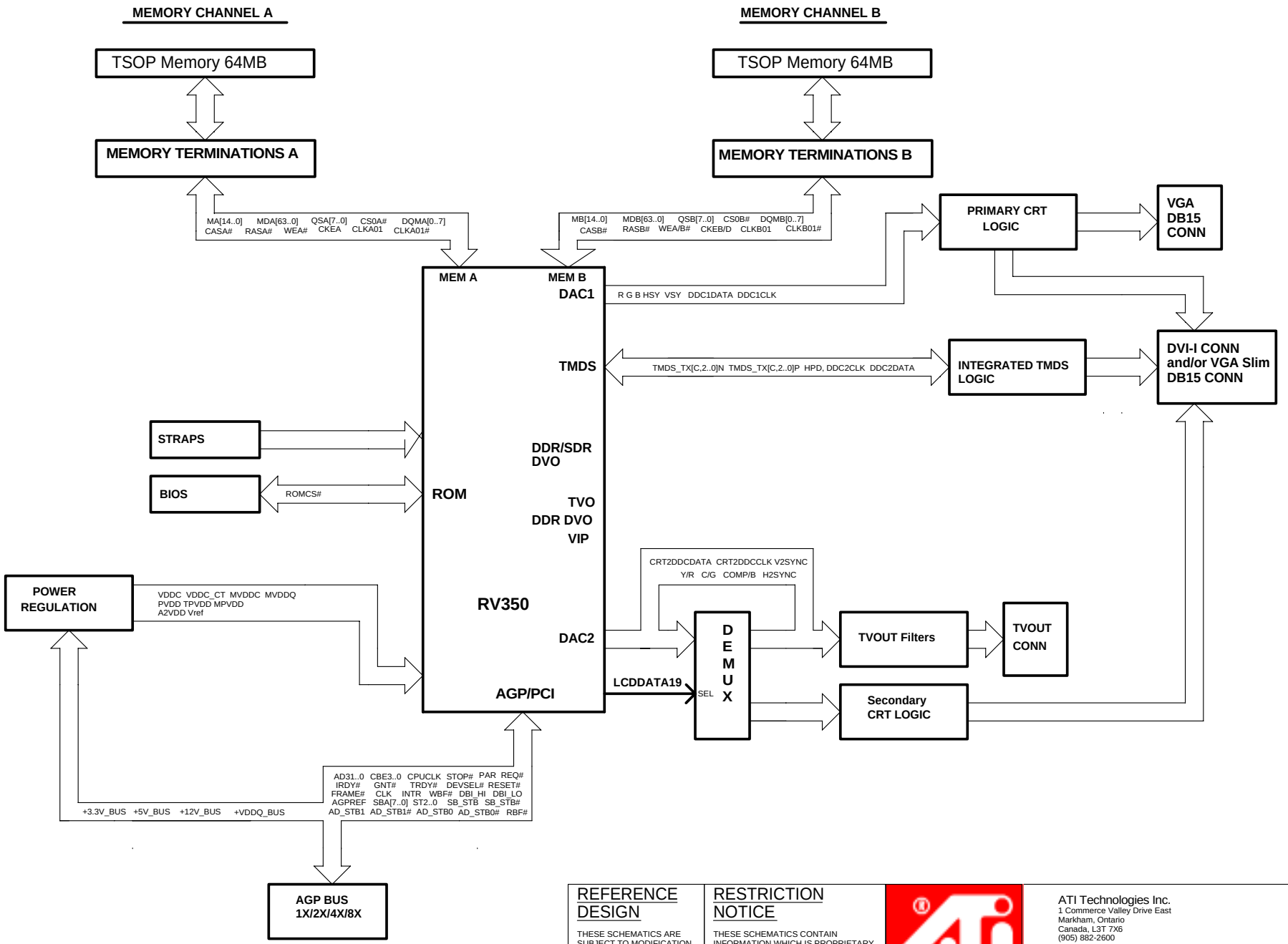

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Title	AGP RV350 128M TSOP VGA DVI VO	
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LAYOUT NOTE: SOME OF THE CAPS BELOW MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

+12V_BUS — C10 10uF_20V 4239010600

+5V_BUS — C5 47uF_6.3V

+3.3V_BUS — C8 47uF_6.3V

+VDDQ_BUS — C2 100uF_6.3V >= 6.3V

Use 47uF Tant. 16V 20% D size (P/N 4230047600), 800mR Max. ESR and Max. ripple 430mA @ 100kHz
or
100uF, Alum. 6.3V 20% 6.3mm dia (P/N 4261010700), 440mR Max. ESR and Max. ripple 230mA @ 100kHz
or
47uF, Alum. 6.3V 20% 5mm dia (P/N 4262047600), 760mR Max. ESR and Max. ripple 150mA @ 100kHz

Place C2 on left side of AGP connector

4X/8X AGP BUS

GND_AVSSN GND_MPVSS GND_TPVSS GND_A2VSSN GND_AVSSQ GND_RSET
GND_AVSSN GND_PVSS GND_TXVSSR GND_A2VSSQ GND_R2SET

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

MAGP1

A1	12V	B1	OVRCNT#
A2	TYPEDET#	B2	5.0V
A3	GC_DET#/RESERVED	B3	5.0V
A4	USB-	B4	USB+
A5	GND	B5	GND
A6	INTA#	B6	INTB#
A7	RST#	B7	CLK
A8	GNT#	B8	REQ#
A9	VCC3.3	B9	VCC3.3
A10	ST1	B10	ST0
A11	MB_DET#/RESERVED	B11	ST2
A12	DBI_HI/PIPE#	B12	RBF#
A13	GND	B13	GND
A14	WBF#	B14	DBI_LO/RESERVED
A15	SBA1	B15	SBA0
A16	VCC3.3	B16	VCC3.3
A17	SBA3	B17	SBA2
A18	SB_STB#	B18	SB_STB
A19	GND	B19	GND
A20	SBA5	B20	SBA4
A21	SBA7	B21	SBA6
A22	RESERVED	B22	RESERVED
A23	GND	B23	GND
A24	RESERVED	B24	3.3VAUX
A25	VCC3.3	B25	VCC3.3
A26	AD30	B26	AD31
A27	AD28	B27	AD29
A28	VCC3.3	B28	VCC3.3
A29	AD26	B29	AD27
A30	AD24	B30	AD25
A31	GND	B31	GND
A32	AD_STB1#	B32	AD_STB1
A33	C/BE3#	B33	AD23
A34	VDDQ1.5	B34	VDDQ1.5
A35	AD22	B35	AD21
A36	AD20	B36	AD19
A37	GND	B37	GND
A38	AD18	B38	AD17
A39	AD16	B39	C/BE2#
A40	VDDQ1.5	B40	VDDQ1.5
A41	FRAME#	B41	IRDY#
A42	KEY	B42	KEY
A43	KEY	B43	KEY
A44	KEY	B44	KEY
A45	KEY	B45	KEY
A46	TRDY#	B46	DEVSEL#
A47	STOP#	B47	VDDQ1.5
A48	PME#	B48	PERR#
A49	GND	B49	GND
A50	PAR	B50	SERR#
A51	AD15	B51	C/BE1#
A52	VDDQ1.5	B52	VDDQ1.5
A53	AD13	B53	AD14
A54	AD11	B54	AD12
A55	GND	B55	GND
A56	AD9	B56	AD10
A57	C/BE0#	B57	AD8
A58	VDDQ1.5	B58	VDDQ1.5
A59	AD_STB0#	B59	AD_STB0
A60	AD6	B60	AD7
A61	GND	B61	GND
A62	AD4	B62	AD5
A63	AD2	B63	AD3
A64	VDDQ1.5	B64	VDDQ1.5
A65	AD0	B65	AD1
A66	VREFGC	B66	VREFCG

1.5V_AGP_BUS
614NOPN062

AGP_C/BE#[3..0] 3 — AGP_AD[31..0] 3 — AGP_SBA[7..0] 3 — AGP_ST[2..0] 3

AGP_TYPEDET# — AGP_GC_8X_DET#

3 AGP_INTR# — 3 AGP_RESET# — 3 AGP_GNT# — AGP_ST1

3 AGP_MB_8X_DET# — 3 AGP_DBI_HI — 3 AGP_WBF#

AGP_SBA1 — AGP_SBA3 — AGP_SBA5 — AGP_SBA7

3 AGP_SBSTB# — R1 0R

AGP_AD30 — AGP_AD28 — AGP_AD26 — AGP_AD24

3 AGP_ADSTB1# — R5 0R

AGP_C/BE#3 — AGP_AD22 — AGP_AD20 — AGP_AD18 — AGP_AD16

3 AGP_FRAME#

3 AGP_TRDY# — 3 AGP_STOP#

3 AGP_PAR — AGP_PAR_R

AGP_AD15 — AGP_AD13 — AGP_AD11 — AGP_AD9 — AGP_C/BE#0

3 AGP_ADSTB0# — R12 0R

AGP_AD6 — AGP_AD4 — AGP_AD2 — AGP_AD0

AGP_VREFGC

AGP_AGPCLK 3 — AGP_REQ# 3

AGP_ST0 — AGP_ST2

AGP_RBF# 3 — AGP_DBI_LO 3

AGP_SBA0 — AGP_SBA2 — AGP_SBA4 — AGP_SBA6

AGP_SBSTB_R R2 0R — AGP_SBSTB 3

AGP_AD31 — AGP_AD29 — AGP_AD27 — AGP_AD25

AGP_ADSTB1_R R6 0R — AGP_ADSTB1 3

AGP_AD23 — AGP_AD21 — AGP_AD19 — AGP_AD17 — AGP_C/BE#2

AGP_IRDY# 3

AGP_DEVSEL# 3

AGP_C/BE#1 — AGP_AD14 — AGP_AD12 — AGP_AD10 — AGP_AD8

AGP_ADSTB0_R R13 0R — AGP_ADSTB0 3

AGP_AD7 — AGP_AD5 — AGP_AD3 — AGP_AD1

AGP_AGPREF

+12V_BUS C4 100nF — +5V_BUS C9 100nF — +3.3V_BUS C15 100nF

Caps for EMI - install close to AGP connector

AGP_TYPEDET# — R19 0R

For retail, 1K ohm pull-down causes AMD system detects AGP2X only
+12V, TYPEDET# short protection for OEM (1KR)

AGP_GC_8X_DET# — R60 0R

UNIVERSAL VREFGC CIRCUIT (4X, 8X)

3 AGP_MB_8X_DET# — R17 47K — Q12 BSN20 — R3 20K — 8X_DET# 3 — TEST

May be placed far from connector -- place C3 FAR from connector, on left side!!

+VDDQ_BUS — Q1 2N7002E — R20 324R — AGP_VREFGC — R21 147R — R24 100R — C6 10nF — Close to ASIC

+5V_BUS — C3 100nF — U2 TC7SZ08FU — R23 1K

UNIVERSAL VREFCG CIRCUIT (4X, 8X)

AGP_AGPREF — +VDDQ_BUS — Q5 2N7002E — TEST — R66 324R — DNI R64 0R — R67 147R — AGP_AGPREFCG — AGP_AGPREFCG 3 — R65 100R — C7 10nF — Close to ASIC

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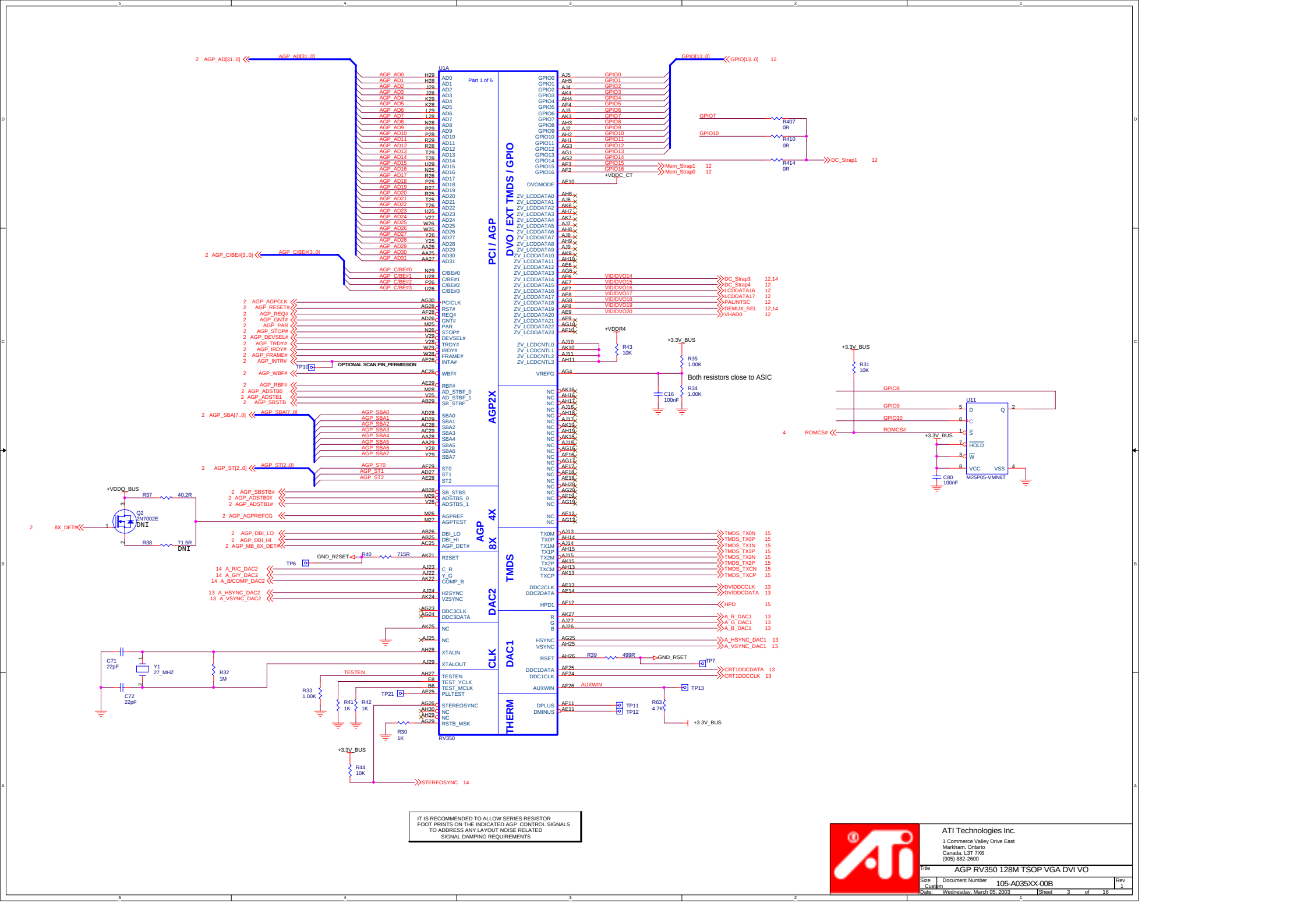
U1A
Part 1 of 6
RV350
PCI / AGP
DVO / EXT TMDS / GPIO
AGP2X
AGP 4X
8X
TMDS
DAC2
DAC1
CLK
THERM
Both resistors close to ASIC
OPTIONAL SCAN PIN_PERMISSION
IT IS RECOMMENDED TO ALLOW SERIES RESISTOR FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS TO ADDRESS ANY LAYOUT NOISE RELATED SIGNAL DAMPING REQUIREMENTS
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Custom
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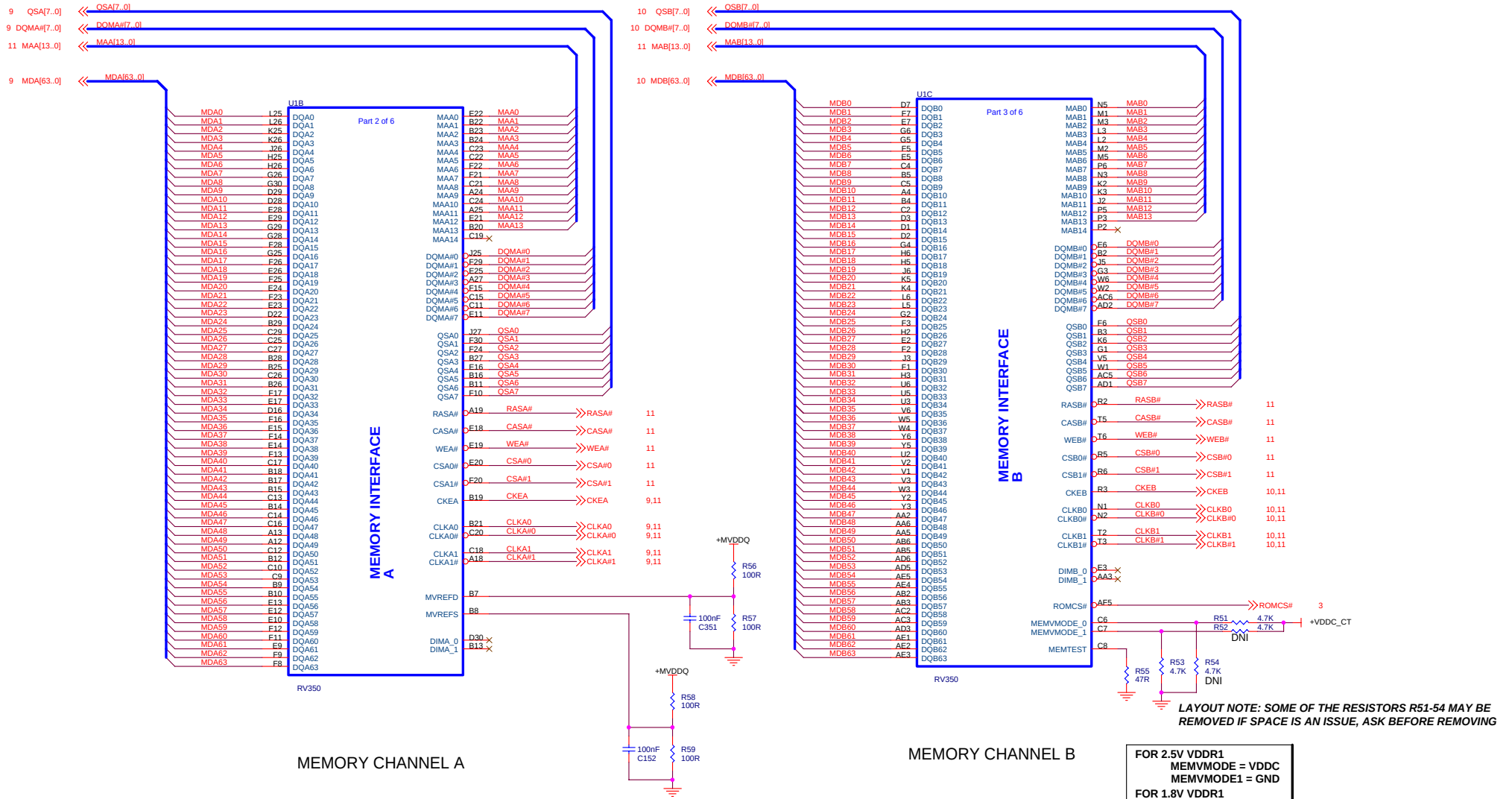
16



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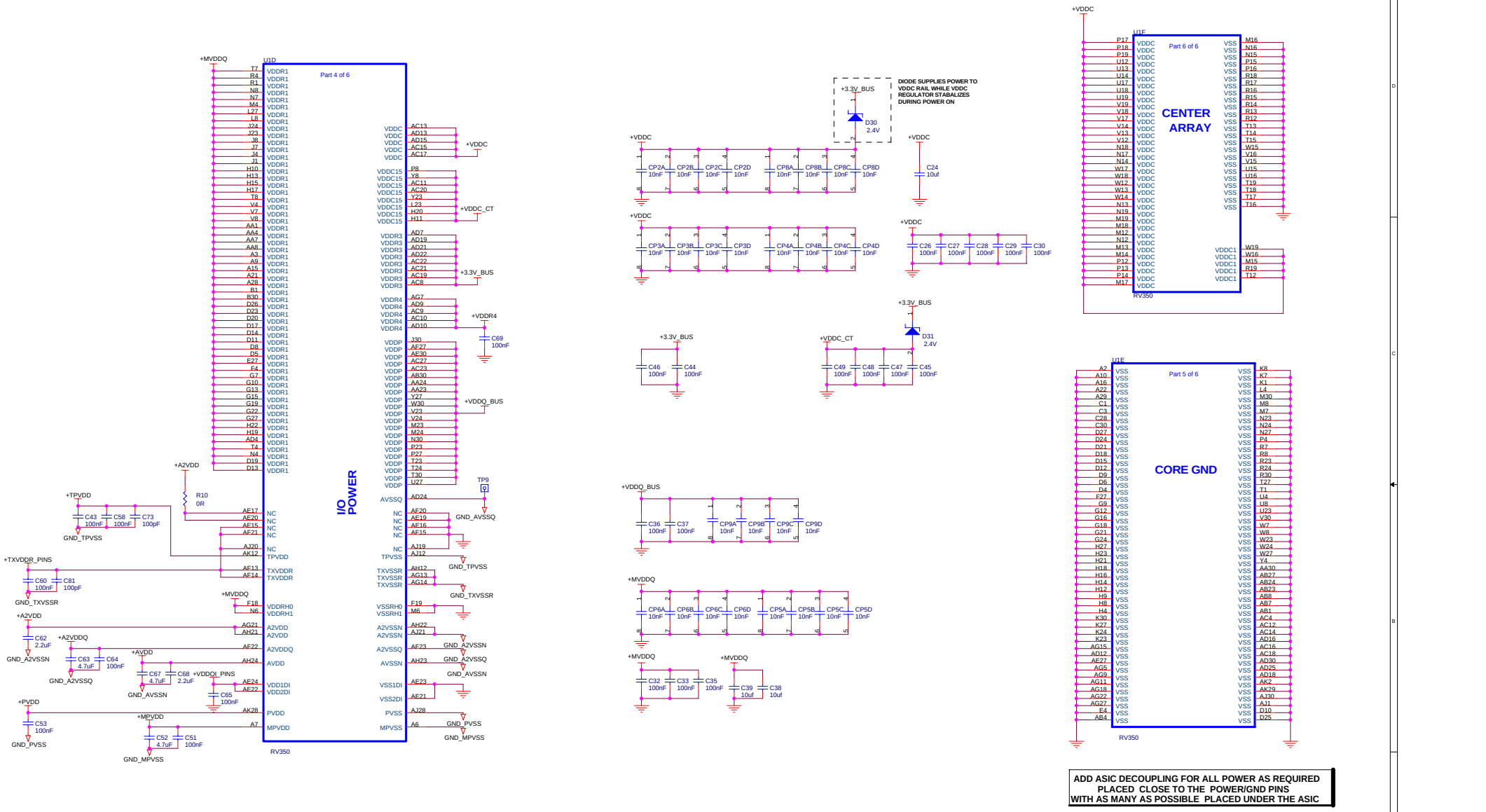

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Regulator for VDDC (ASIC Core)

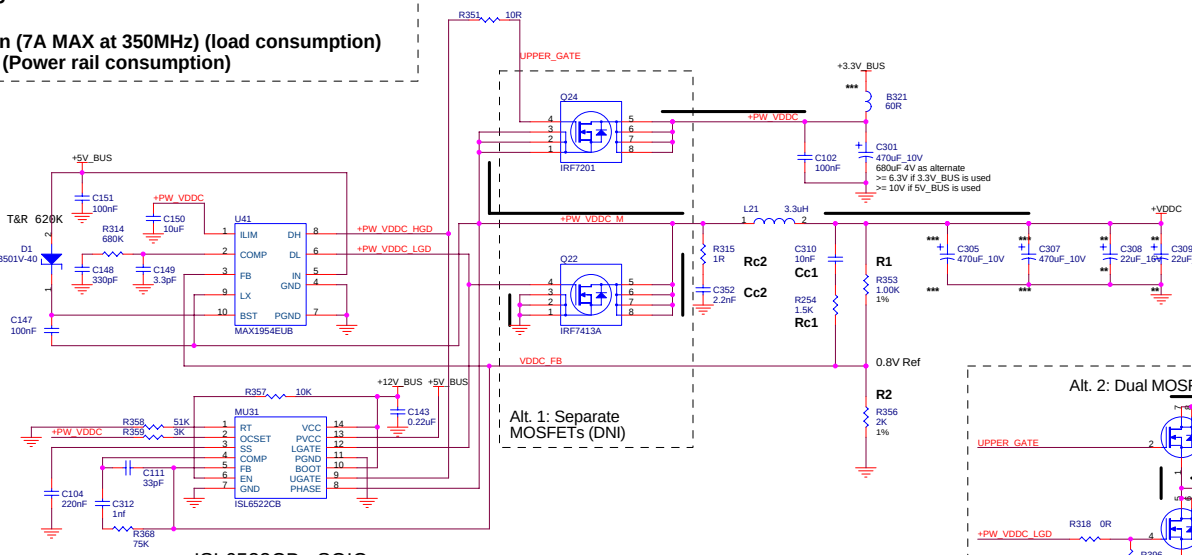
Vin = 3.3V AGP
Vout = 1.2V
Iout = Unknown (7A MAX at 350MHz) (load consumption)
Iout = 3A MAX (Power rail consumption)

Part	NOTES
MAX1954	Do not install Cc1, Rc1 Install Cc2, Rc2
ISL6522	Do not install Cc2, Rc2 Install Cc1, Rc1

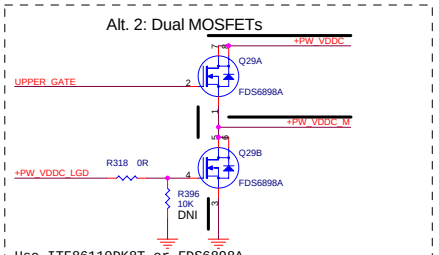
*** Indicate number of via required for the connection

Part	Vout	R1	R2
MAX1954 ISL6522 0.8V Ref	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240110100
	1.62V	1.00K 1% ATI P/N 3240100100	976R 1% ATI P/N 3240976000
	2.5V	1.00K 1% ATI P/N 3240100100	475R 1% ATI P/N 3240475300
	3.3V TSOP Memory	1.00K 1% ATI P/N 3240100100	324R 1% ATI P/N 3240332000
	3.45V TSOP Memory	1.00K 1% ATI P/N 3240100100	301 1% ATI P/N 3240301000

FOR R314 USE 620K:
RES 0.1W 5% SM EIA(0805) T&R 620K



ISL6522CB : SOIC

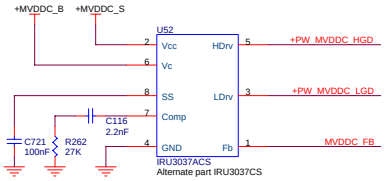


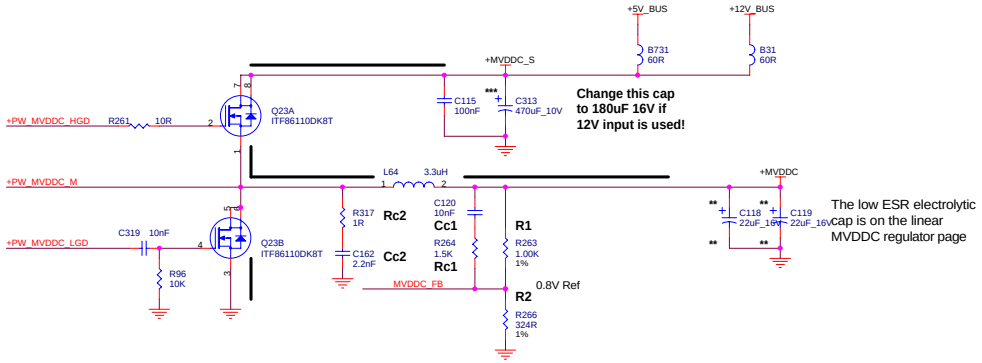
Use ITF86110DK8T or FDS6898A
(Part numbers 2020004100 or 2020007600)
Rated 7A or 9A

Regulator for MVDDC (MEM Core)

Vin = 5V AGP
Vout = 3.3V ~ 3.45V
Iout = 2.7A (330mA x 8) MAX, Burst Mode (load consumption)
Iout (5V) = 2A MAX (Power rail consumption)

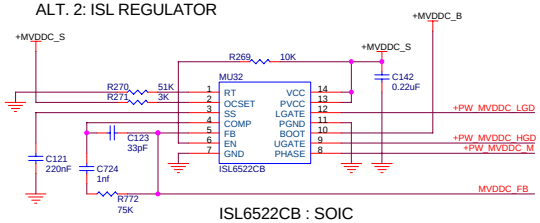
ALT. 1: IRU REGULATOR





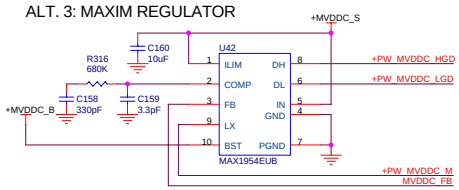
The low ESR electrolytic cap is on the linear MVDDC regulator page

ALT. 2: ISL REGULATOR



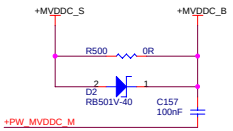
ISL6522CB : SOIC

ALT. 3: MAXIM REGULATOR



DO NOT USE MAXIM REGULATOR IF 12V INPUT IS USED!!!
FOR R316 USE 620K: RES 0.1W 5% SM EIA(0805) T&R 620K

Boot circuit



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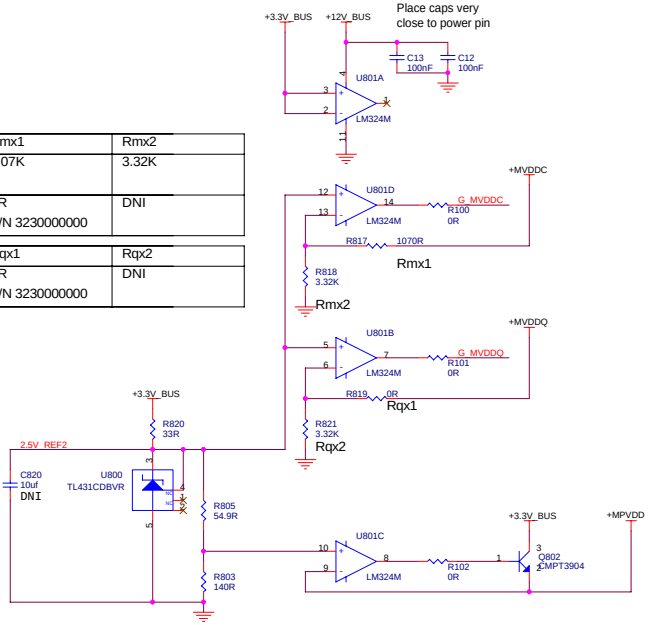
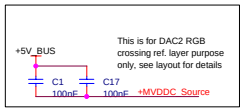
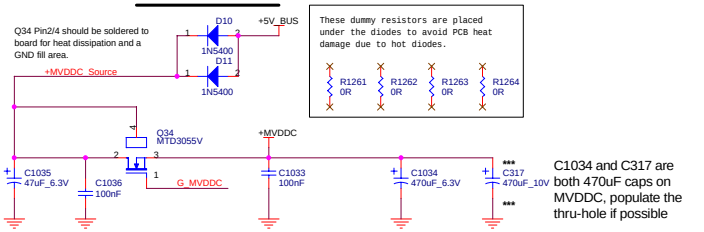
New regulator for MVDDQ, 64MB MVDDC and MPVDD

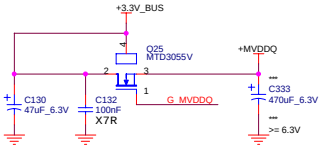


+MVDDC	Voltage Req.	Rmx1	Rmx2
Hynix	3.3V [-0.02V/+0.02V]	1.07K	3.32K
Sumsung	2.5V	0R P/N 3230000000	DNI

+MVDDQ	Voltage Req.	Rqx1	Rqx2
	2.5V	0R P/N 3230000000	DNI



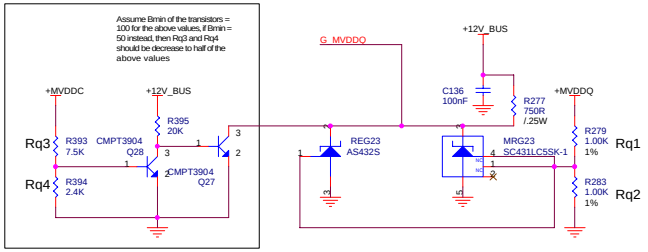




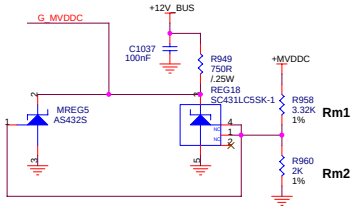
Old regulator for MVDDQ (MEM IO) & VDDR1
Vin = 3.3V AGP
Vout = 2.5V
Iout = 1200mA MAX
Iout = 1000mA Est. MAX

Type	Voltage Req.	Rq1	Rq2
Elpida	1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
	2.5V	1K 3240100100	1K 3240100100
	2.6V	4.75K 3240475100	4.32K 3240432100

+MVDDC	Rq3	Rq4
3.45V (TSOP)	7.5K 3230075200	2.4K 3230024200

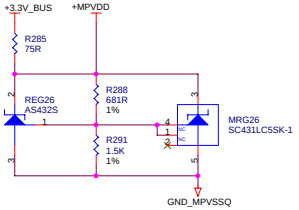


Regulator for MVDDC
Vin = 5V
Vout = 3.3V
Iout = 1.4A MAX



	Voltage Req.	Rm1	Rm2
Hynix	3.34V [-0.04V/+0.04V]	4.32K	2.55K
	3.45V [-0.04V/+0.04V]	4.32K	2.43K
Sumsung	2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100

Old regulator for +MPVDD
Vin = 3.3V
Vout = 1.8V
Iout = 10mA MAX



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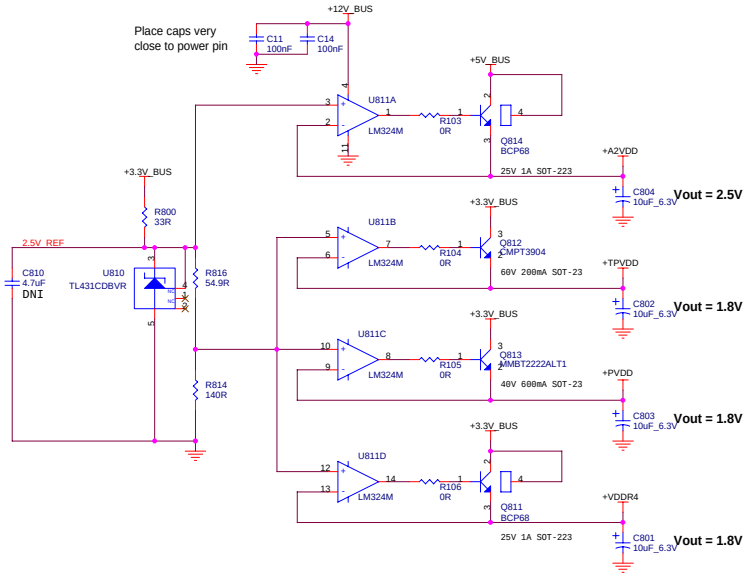
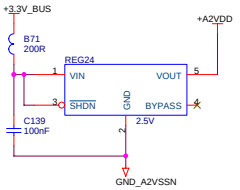
New regulator for VDDR4, PVDD, A2VDD and TPVDD

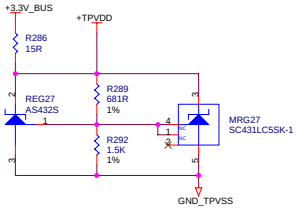


Old Regulator for +A2VDD (150mA)
Vin = +3.3V AGP
Vout = 2.5V

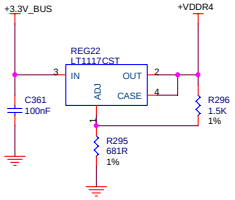


+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.

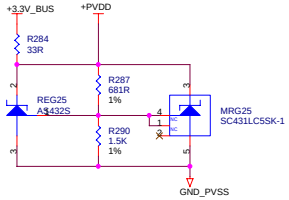
Old regulator for +TPVDD (70mA)
Vin = +3.3V AGP
Vout = 1.8V



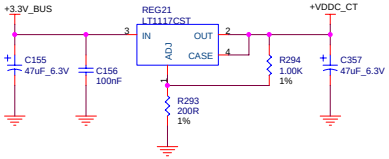
Old Regulator for +VDDR4
Vin = 3.3V
Vout = 1.8V



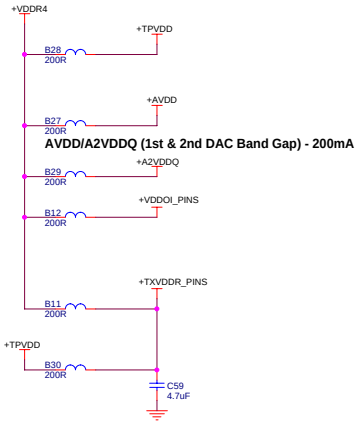
Old regulator for +PVDD (30mA)
Vin = 3.3V AGP
Vout = 1.8V



Regulator for +VDDC_CT (550mA)
Vin = 3.3V
Vout = 1.5V



Derived from VDDR4:



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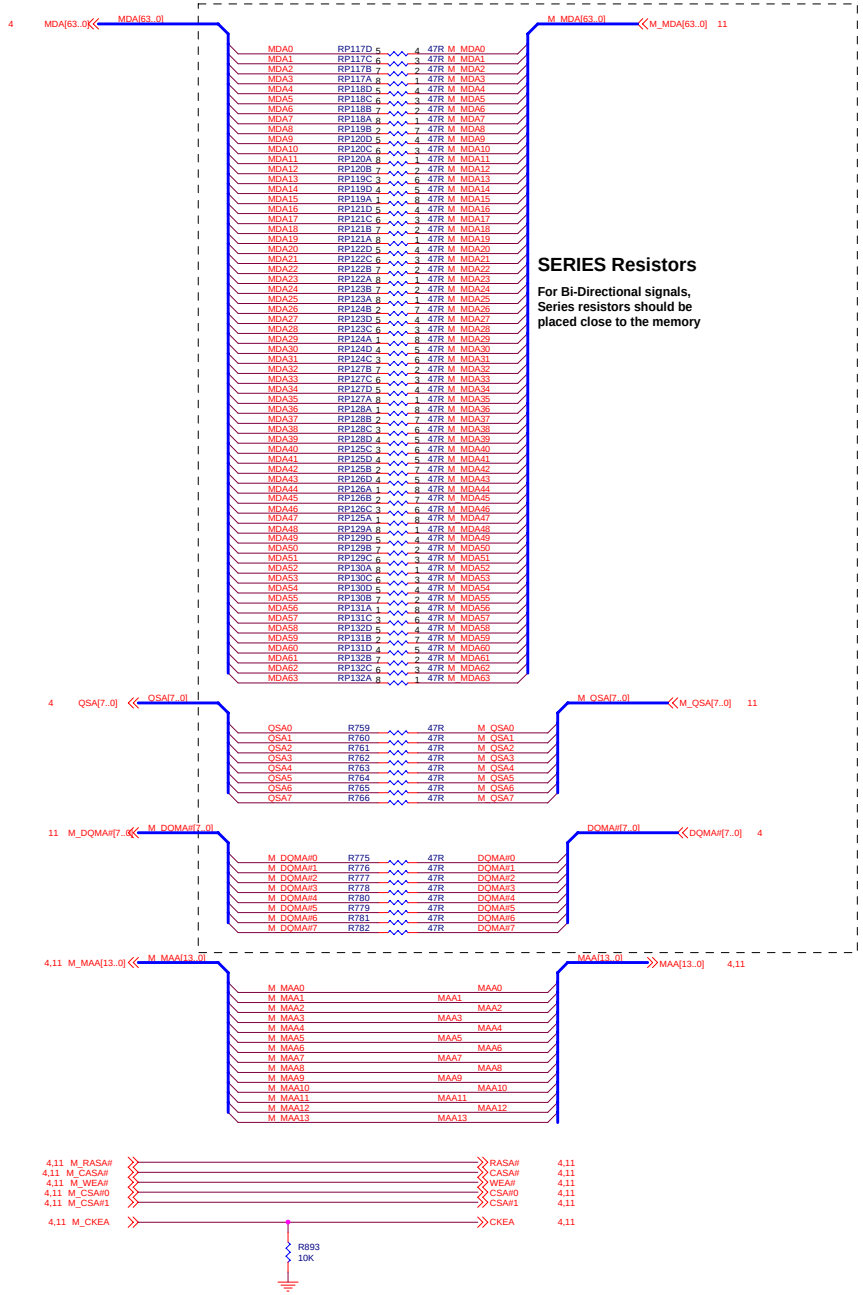
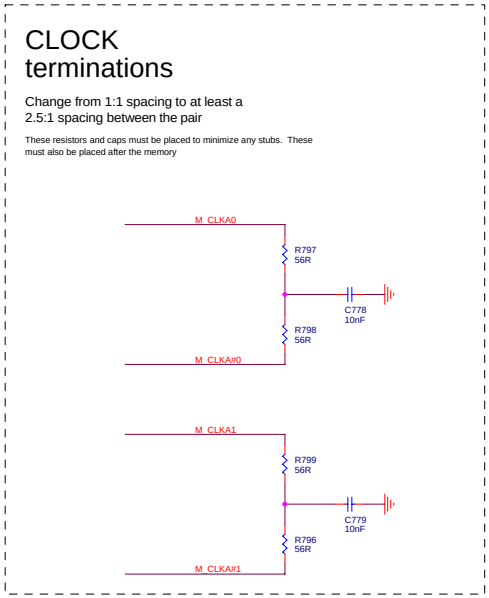
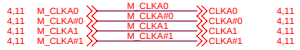
TERMINATION FOR MEMORY CHANNEL A







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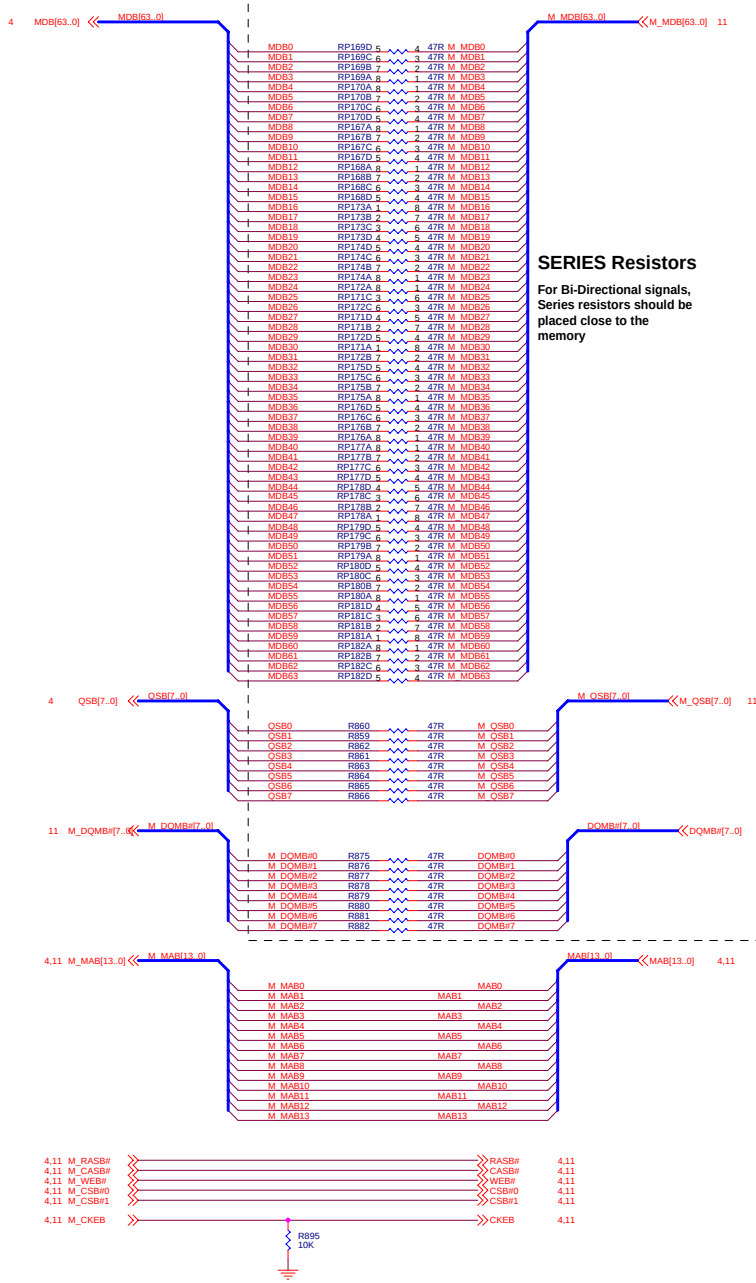
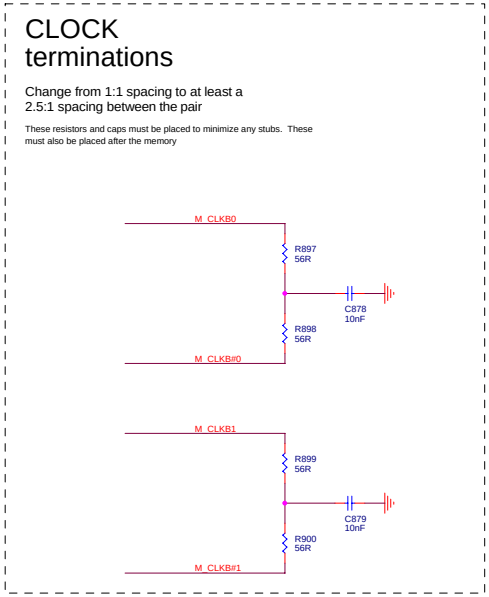
TERMINATION FOR MEMORY CHANNEL B





4,11 M_CLKB0	M_CLKB0	CLKB0	4,11
4,11 M_CLKB#0	M_CLKB#0	CLKB#0	4,11
4,11 M_CLKB1	M_CLKB1	CLKB1	4,11
4,11 M_CLKB#1	M_CLKB#1	CLKB#1	4,11

4,11 M_RASB#	M_RASB#	RASB#	4,11
4,11 M_CASB#	M_CASB#	CASB#	4,11
4,11 M_WEB#	M_WEB#	WEB#	4,11
4,11 M_CSB#0	M_CSB#0	CSB#0	4,11
4,11 M_CSB#1	M_CSB#1	CSB#1	4,11
4,11 M_CKEB	M_CKEB	CKEB	4,11

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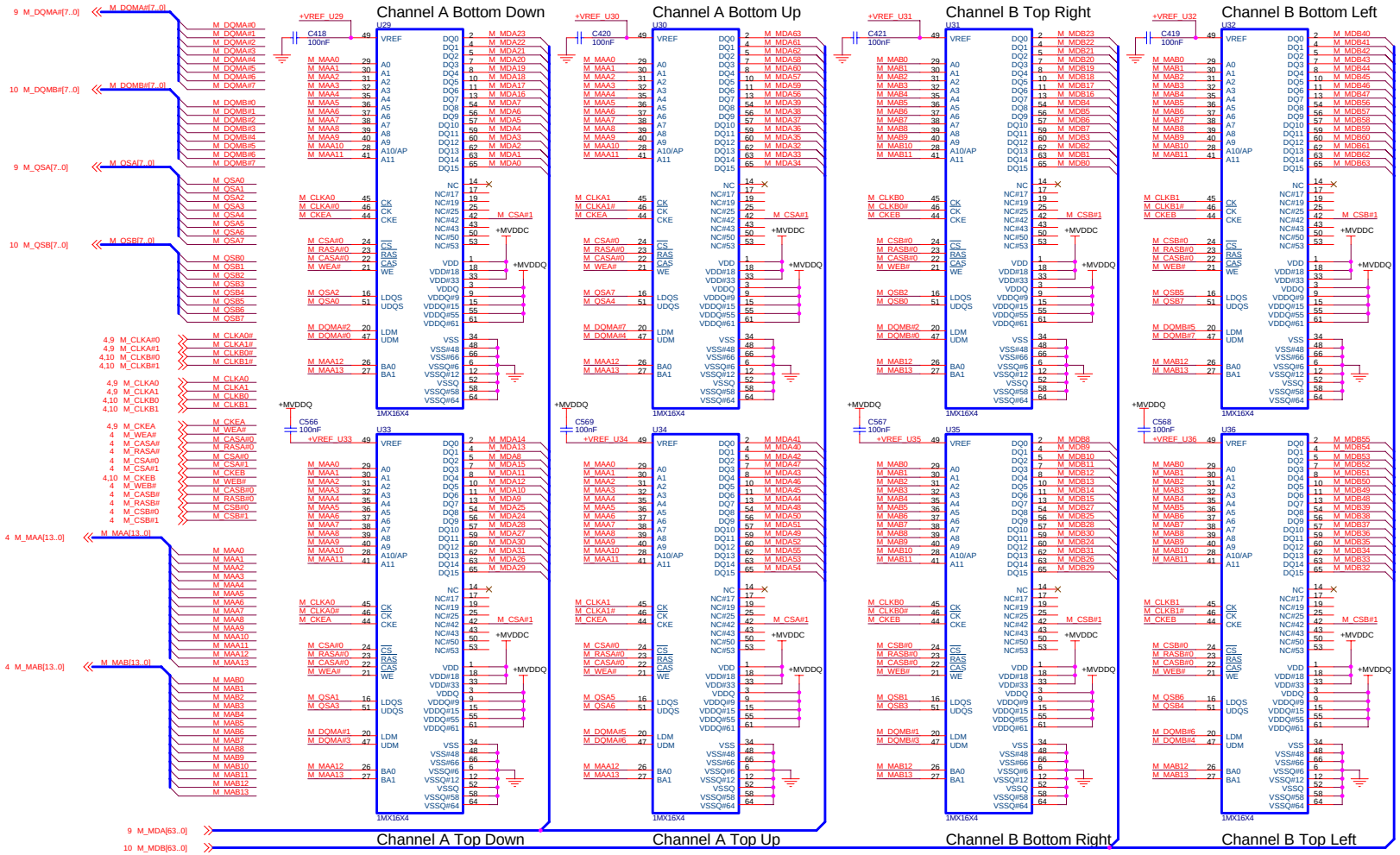
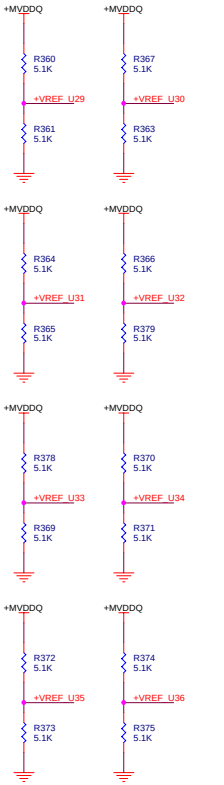


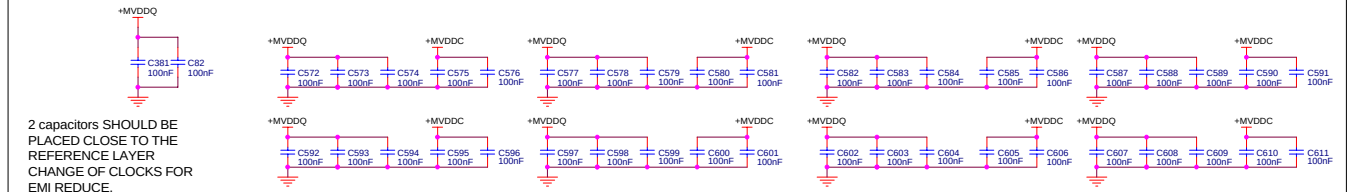
DDR SDRAM 64Mbit 1Mx16x4

DDR SDRAM 128Mbit 2Mx16x4



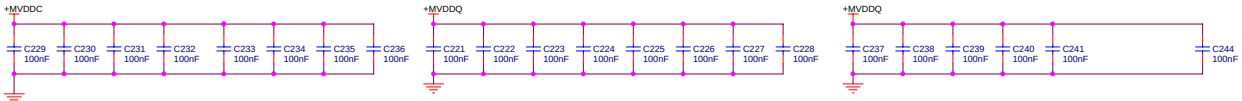
Note: These indications of the location of the memory for the solder side (bottom) are looking thru from the component side.

Put 1 100nF cap per power pin of memory



2 capacitors SHOULD BE PLACED CLOSE TO THE REFERENCE LAYER CHANGE OF CLOCKS FOR EMI REDUCE.

Place as many as possible.



DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

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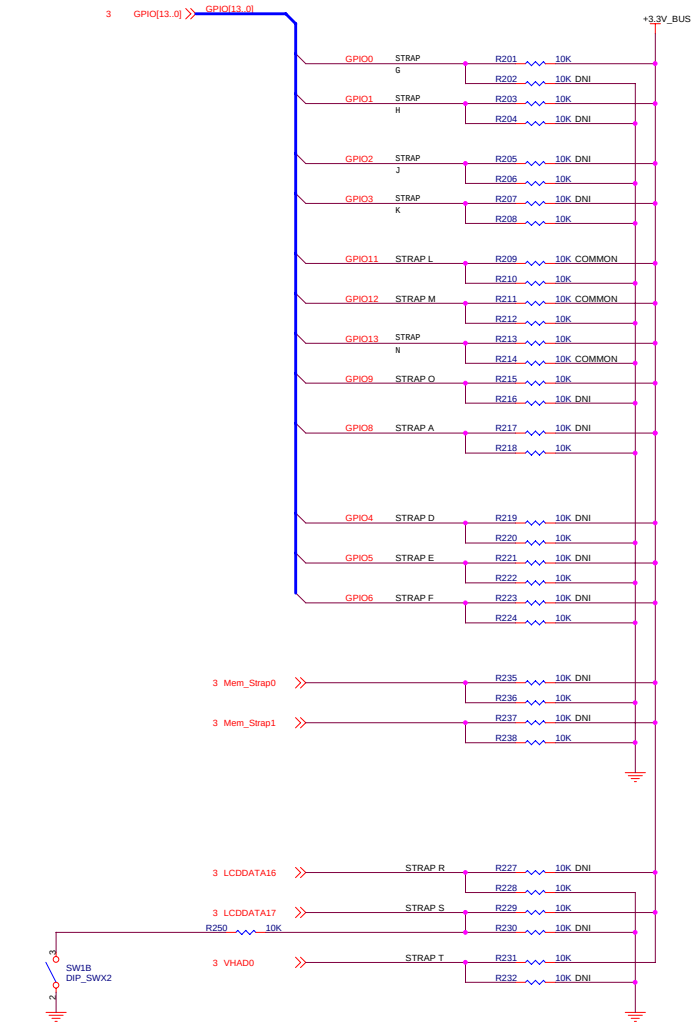
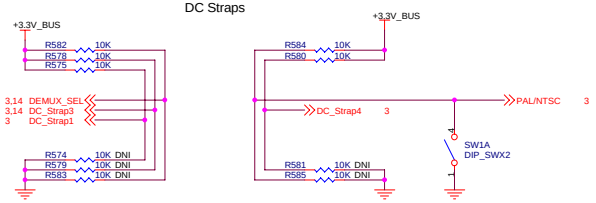
OPTION STRAPS



STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM **1011 - Serial M25P10 ROM (ST), chip IDis from ROM** 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1001
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000 (internal pull-down)
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select **00 - single function device.** 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	00
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

DC Straps



STRAPS	PIN	DESCRIPTION
DC_STRAP1	LCDDATA12	Internal TMDS Enabled **0 - Disabled** 1 - Enabled
DC_STRAP2	LCDDATA13	Video Capture Enabled **0 - Disabled** 1 - Enabled THIS STRAP IS NOT PRESENT ON THIS CARD!
DC_STRAP4 DC_STRAP5	LCDDATA15 LCDDATA19 0 0 0 1 1 0 1 1	DAC2 Configuration DAC2 Off DAC2 On as CRT DAC2 On as TVOUT DAC2 On as TVOUT and CRT
DC_STRAP6	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 -NTSC (on board resistor pull-up)
DC_STRAP3	LCDDATA14	Connected to Component TV-Out Detect pin Normally high, pulled low by Component TVO dongle

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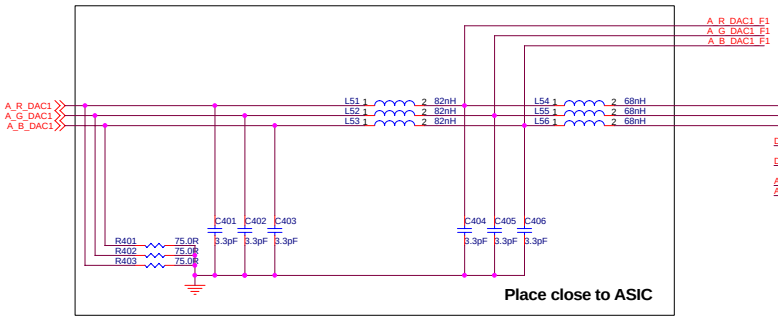
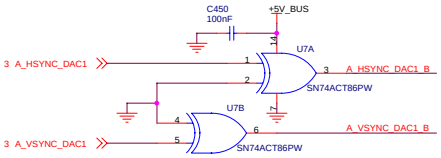
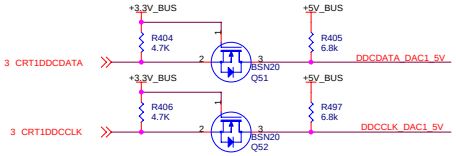
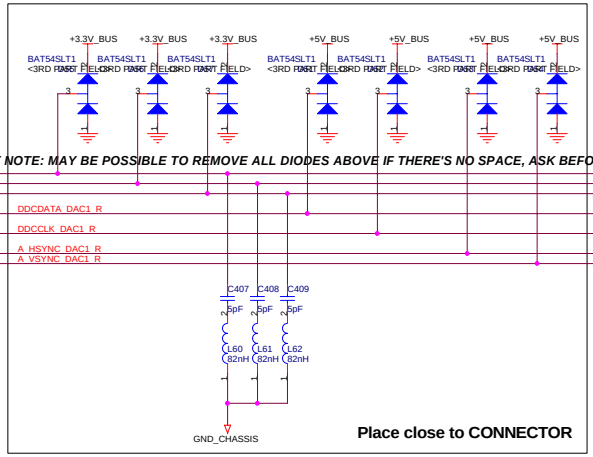
PRIMARY CRT

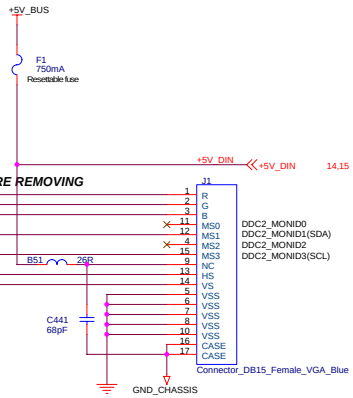




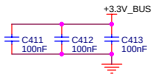


OPTIONAL ESD/HOTPLUG PROTECTION DIODES

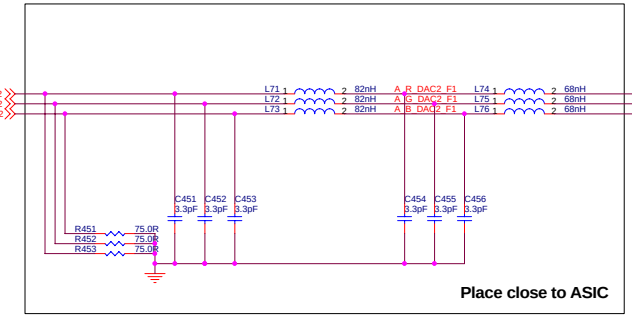


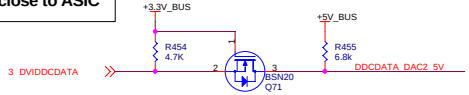


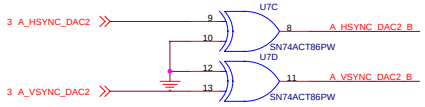
This is for cutting return path

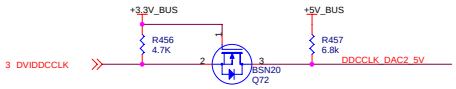


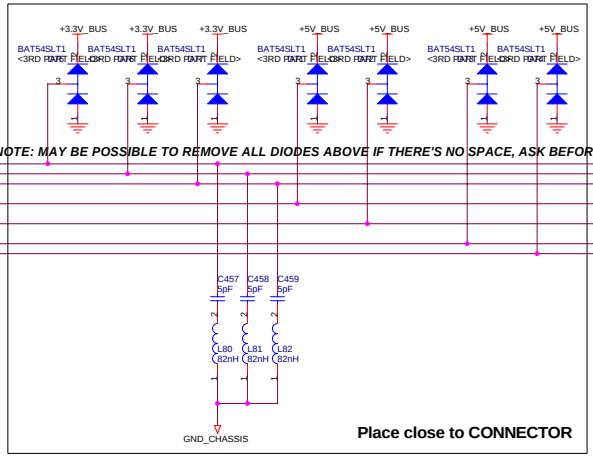
SECONDARY CRT

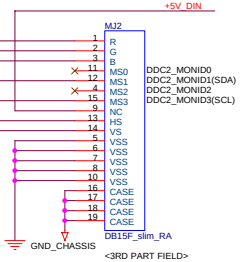


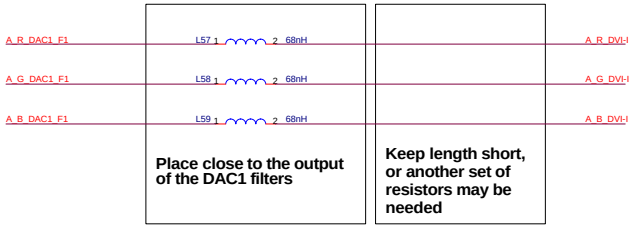


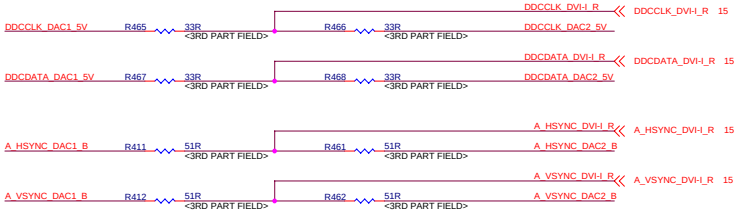


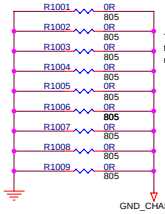












Three on top side, three at the bottom, spreaded high, middle and low vertically

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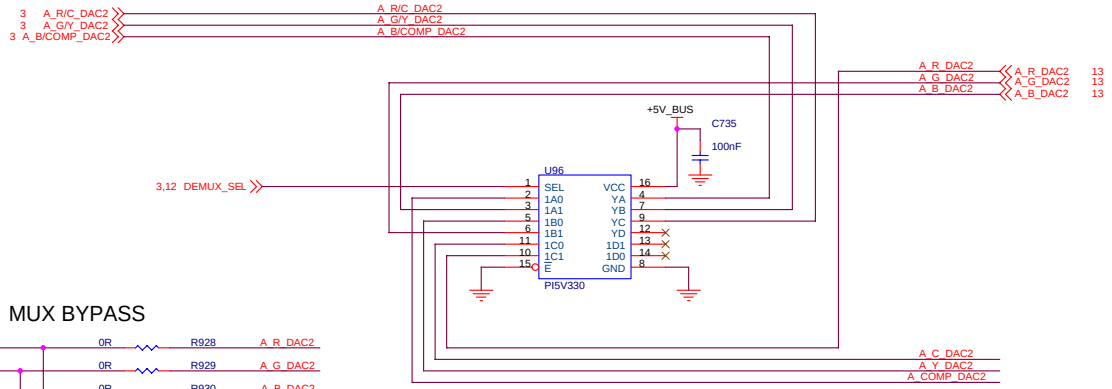
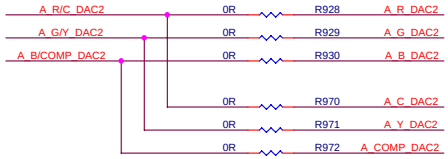
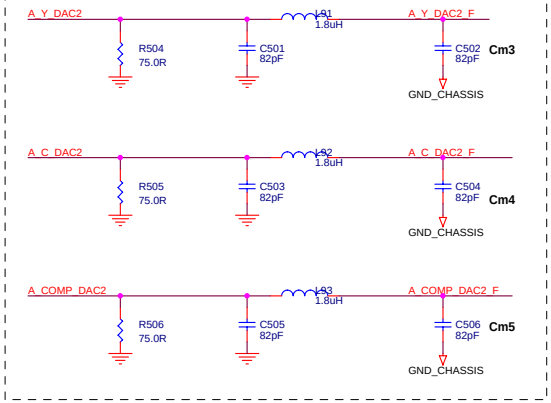
Place close to ASIC



MUX BYPASS

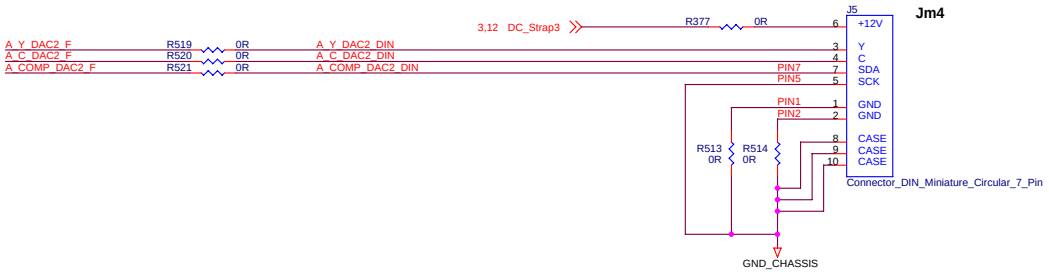


Place close to connector



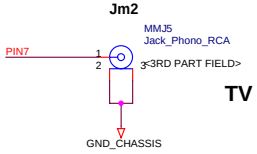
TV Out (SVHS)

Jm4

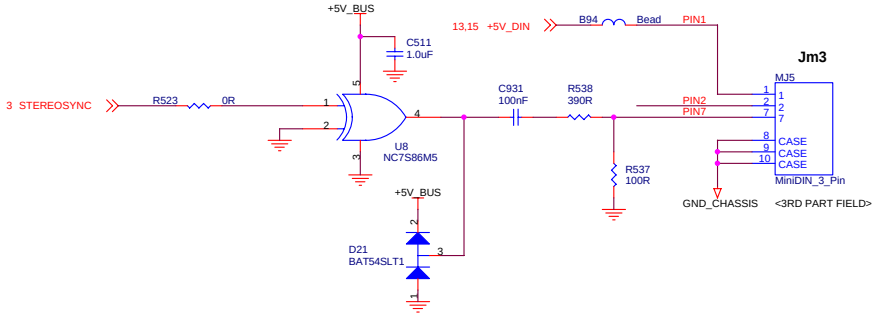


Jm2, Jm3, Jm4 use the same footprint

Jm2



TV Out (Comp)



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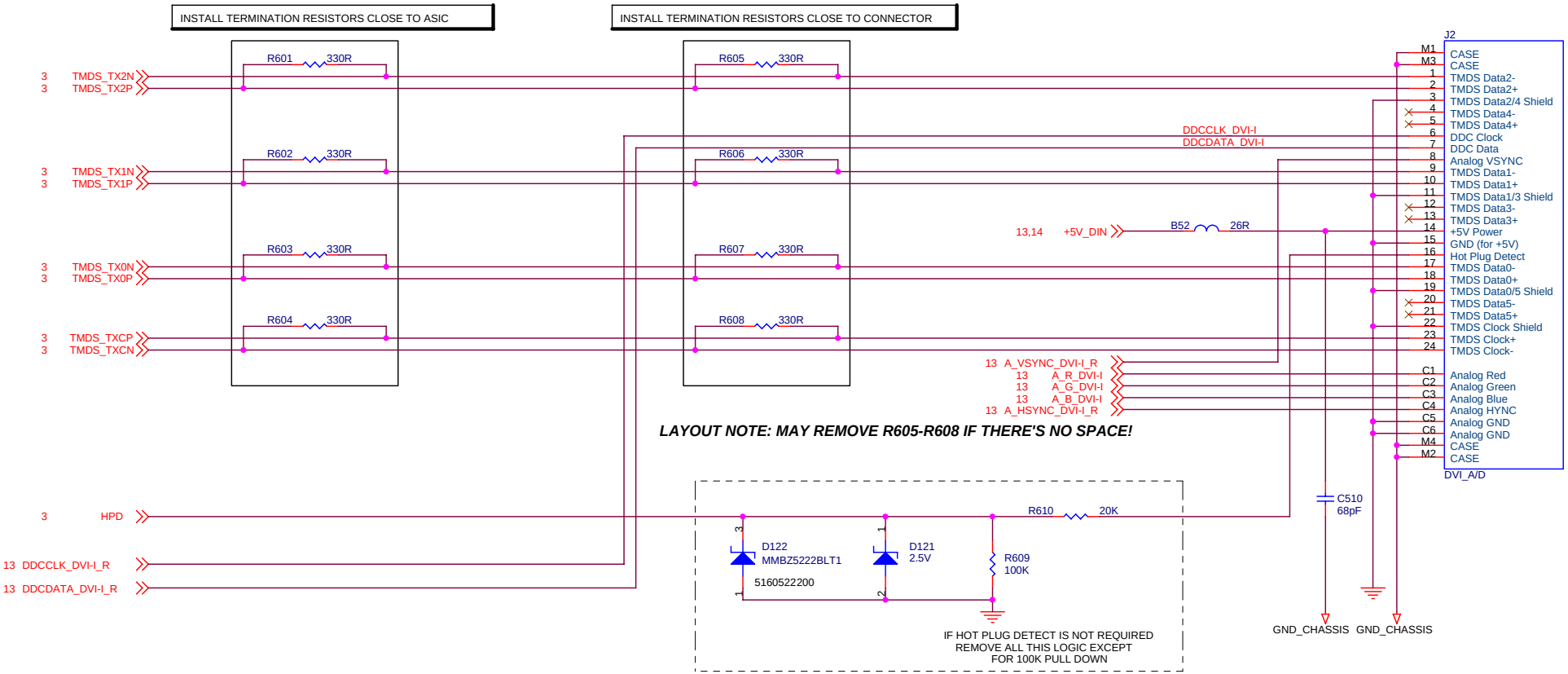
PRIMARY DVI-I CONNECTOR



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CRT SCREWS

ASSY1

SCREW
JACKSCREW
<3rd part field>

ASSY2

SCREW
JACKSCREW
<3rd part field>

DVI SCREWS

ASSY3

SCREW
JACKSCREW
<3rd part field>

ASSY4

SCREW
JACKSCREW
<3rd part field>

ASSY5

SCREW
PAN_HEAD
ASSY

MISC. BOARD PARTS

ASSY7

ANTISTATIC BAG

6_X_11
<3rd part field>

ASSY8

BLANK LABEL

1.50W_X_0.50H
ASSY

REF1

SCHEMATIC

105-A03500-00B
<3rd part field>

REF2

PCB

109-A03500-00B
<3rd part field>

REF5

ATI LOGO LABEL

ATI_LOGO_LABEL

ASSY11

BRACKET
AGP VIDEO OUT, RVA, 317
8020033500

WRONG SYMBOL, MUST BE UPDATED LATER

MH101

HEATSINK

PASSIVE HEATSINK

H103
HEATSINK

Hc

Heatsink cross-hatched finned 45X45X10mm black amodize w/o adhesive

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<variant Name>

Title	Schematic No.	Date:
AGP RV350 128M TSOP VGA DVI VO	105-A035XX-00B	**Wednesday, March 05, 2003**

REVISION HISTORY

Rev 1

Sch Rev	Date	REVISION DESCRIPTION
0	2002/11/27	PRELIMINARY BASED ON A034
1	2003/02/20	Add AND gate footprint for AGP_MB_8X_Det#, delete C3 Change C62 and C68 to 2.2uF (no footprint change) GND_AVSS, GND_A2VSSN and GND_A2VSSQ grounded at 100nF decapling cap (layout change only) Swap memory address 12 and 13 (both channels) Change ceramic caps at the output of the regulator U810 to 10uF tant. Move C55 close to ASIC (Layout change) Add stiching caps between +MVDDC_Source and +5V_BUS (C1 and C17) Add 3 more 0R for Chassis and Digital GND