

P141-A03, NV31/NV34/NV18B

4(8,16)Mx16, 64(128,256)MB, VIDEO IN/OUT, DVI-I, VGA

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17	POWER SUPPLY: FBVDD, DDC5V

HISTORY:

A00

X00:	INITIAL VERSION
X01:	First Review
	Replaced series resistors in sync lines with 33ohms
	Moved clamping diodes next to GPU
	Added parallel caps to EMI filter DACB
	Removed not needed strap on SAA7114
	Connected RESET and WP of SST ROM to ROMVCC
	Added parallel ROM and Strapps
	Added FBVDD regulator
	Added STEREO glasses circuit
	Removed Decoupling CAPs on VIP VDD, covered by Caps on page 2
	Added ROM_VCC for cleaner planes
	Changed used TMDS lines of IFPA and IFPB to TP from NTP
	Changed Resistor for AGP Vref circuit to 158k
X02:	Final Review
	Added clock termination resistors
	Added net name for FBCALxxx
	Added cap on filter input for FB_DLLVDD, DACA_VDD & DACB_VDD
	Changed netnames for SAA7114 NTPs to NTP_xxx
	Added 1uF cap parallel to fan connector
	Changed all xxCALxx resistors to 50 Ohms
	Changed all FBxDQS*-<x> to NTP_FBxDQS*-<x> with NO_TEST property

A01

X00:	Fixed pin swap on parallel ROM A12 & A13
	Added charge pump for SC2612
	Added resistors to swap GPIO for DACB loadtest
	Added resistors for I2C on internal Video IN connector
X01:	Updated variant information for new S bom structure

A02

X00:	Added sw adjust for NVVDD
	Exchanged TMDSIOVDD regulator to lower the voltage drop
	Changed TMDSPLLVD regulator bypass to A3V3
	Addrd 1k series resistor in DACB load detection circuit

A03

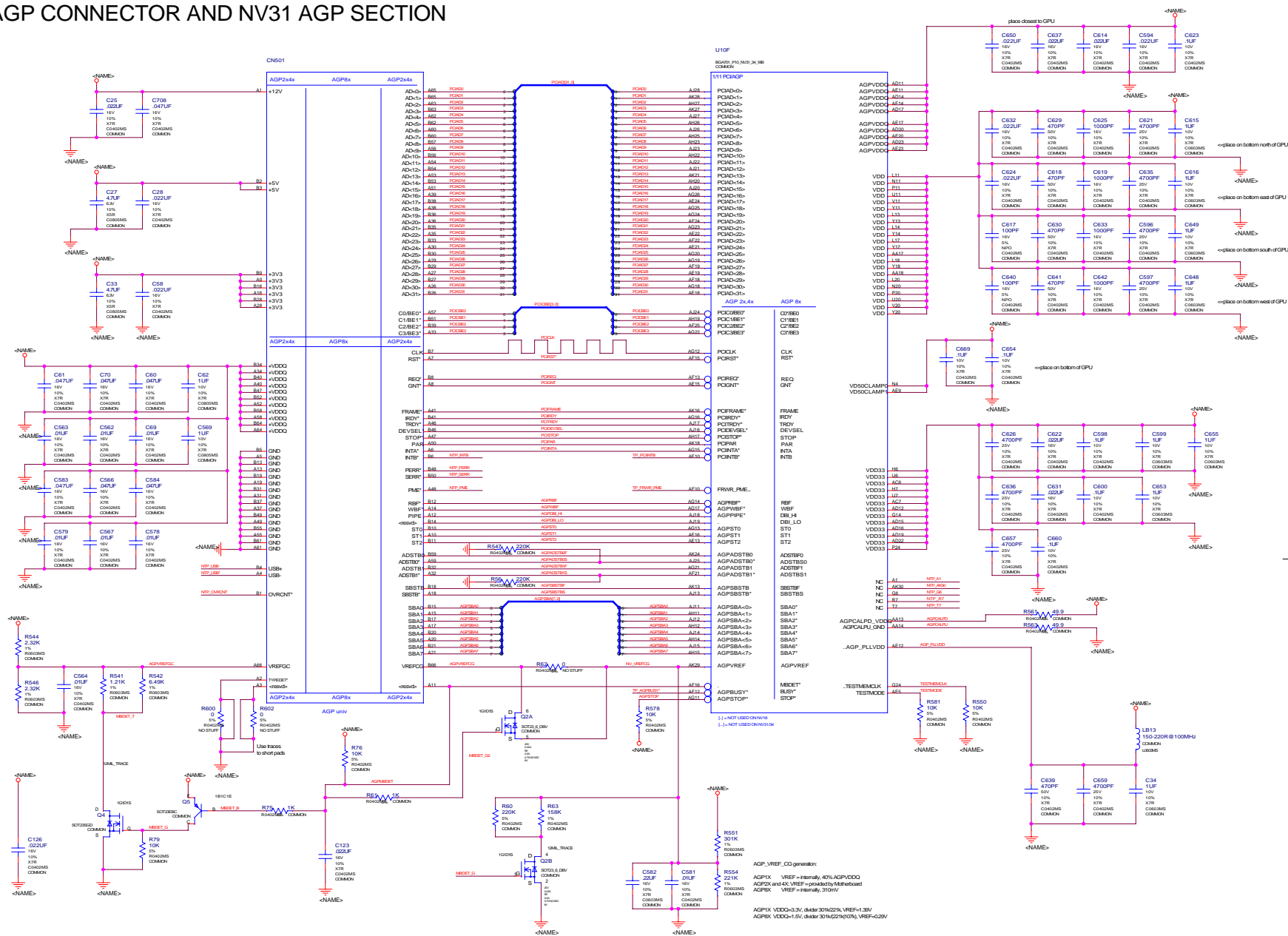
X00:	Removed GPIO5 from NVVDD adjust
	Fixed values for DAC Rset resitors
	Removed Sync Buffer bypass
	Removed 2nd voltage selection fet
	Changed to new internal video connector
	Added snubber to NVVDD and FBVDD regulator

8912 version 210 base on P141-A03 Modify.

1.Page 13 add 1*4 pin vedio-in connector.

602-10141-0000-000 Base Schematic

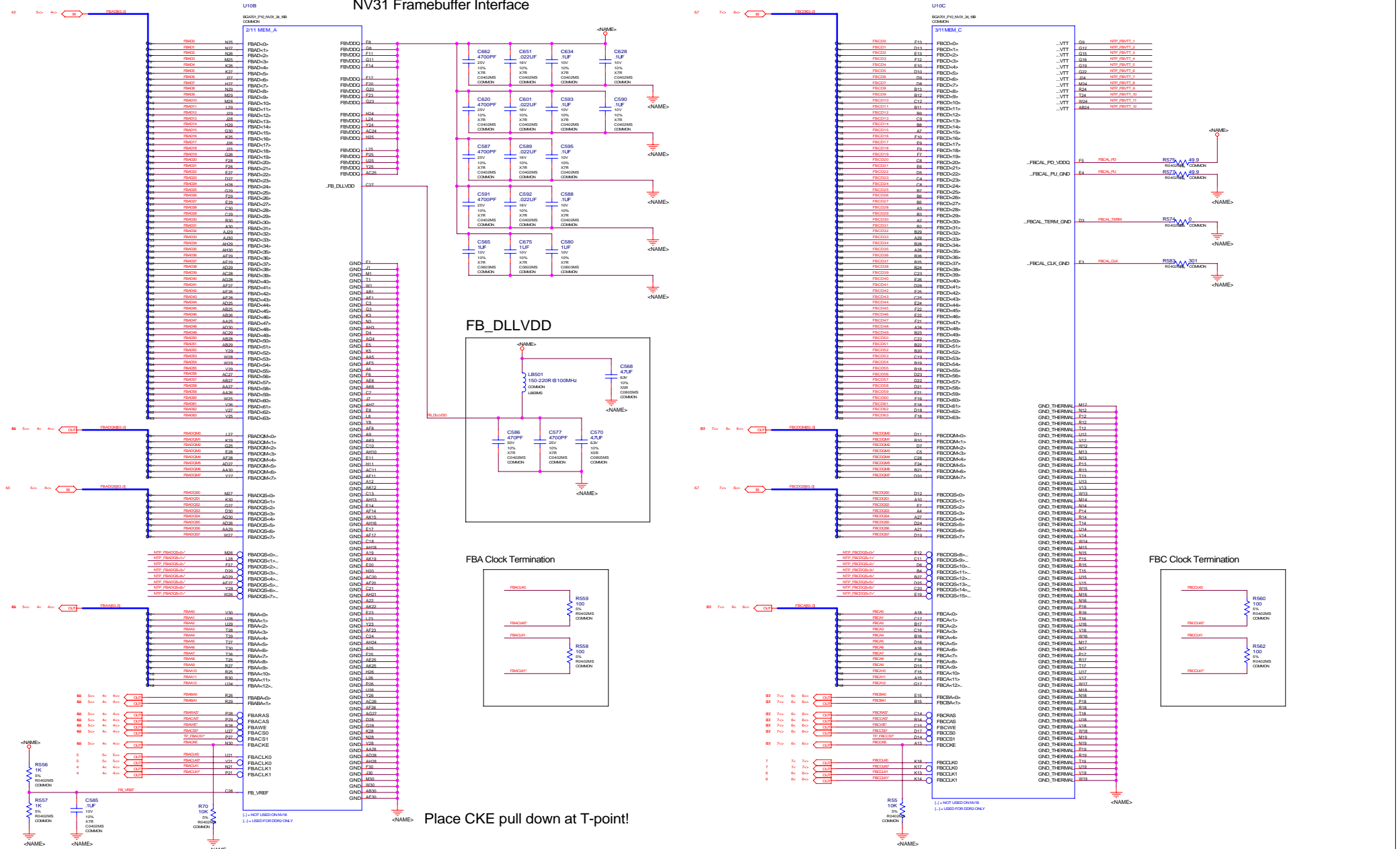
AGP CONNECTOR AND NV31 AGP SECTION



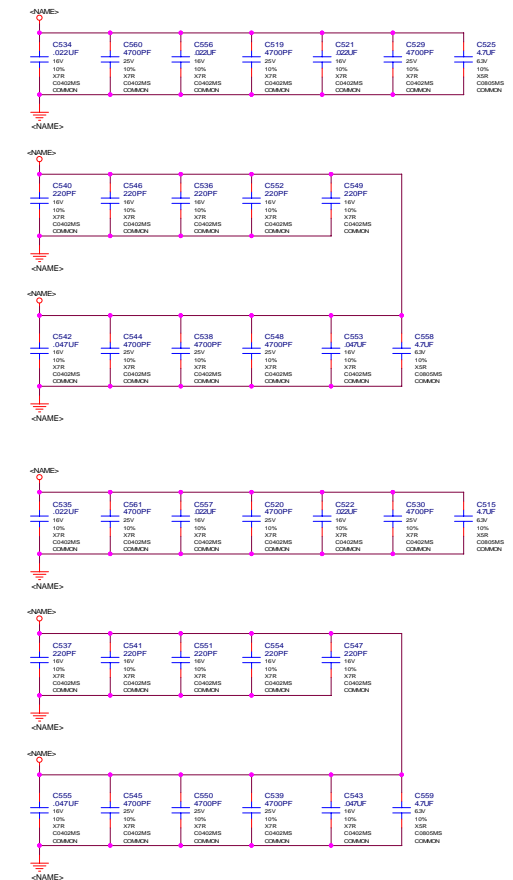
AGP rules

Net Spelling		Net Spelling
00	POWDER 00	13.00
01	POWDER 01	13.00
02	POWDER 02	13.00
03	POWDER 03	13.00
04	POWDER 04	13.00
05	POWDER 05	13.00
06	POWDER 06	13.00
07	POWDER 07	13.00
08	POWDER 08	13.00
09	POWDER 09	13.00
10	POWDER 10	13.00
11	POWDER 11	13.00
12	POWDER 12	13.00
13	POWDER 13	13.00
14	POWDER 14	13.00
15	POWDER 15	13.00
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17	POWDER 17	13.00
18	POWDER 18	13.00
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27	POWDER 27	13.00
28	POWDER 28	13.00
29	POWDER 29	13.00
30	POWDER 30	13.00
31	POWDER 31	13.00
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33	POWDER 33	13.00
34	POWDER 34	13.00
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36	POWDER 36	13.00
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38	POWDER 38	13.00
39	POWDER 39	13.00
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43	POWDER 43	13.00
44	POWDER 44	13.00
45	POWDER 45	13.00
46	POWDER 46	13.00
47	POWDER 47	13.00
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95	POWDER 95	13.00
96	POWDER 96	13.00
97	POWDER 97	13.00
98	POWDER 98	13.00
99	POWDER 99	13.00
100	POWDER 100	13.00

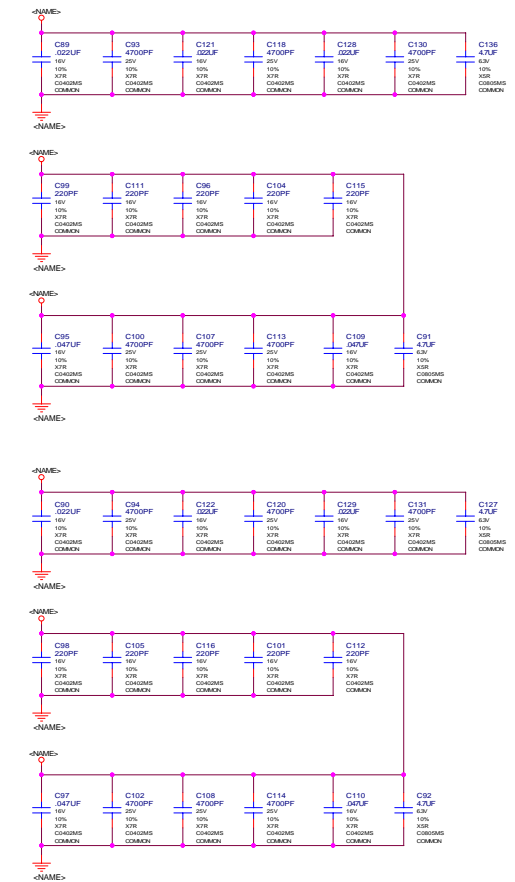
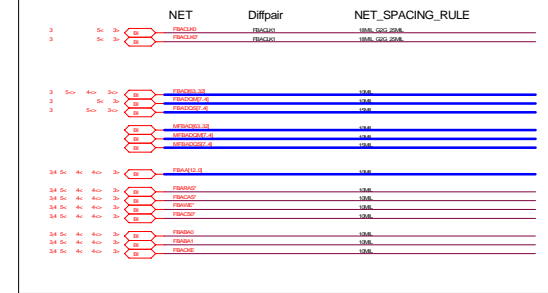
NV31 Framebuffer Interface



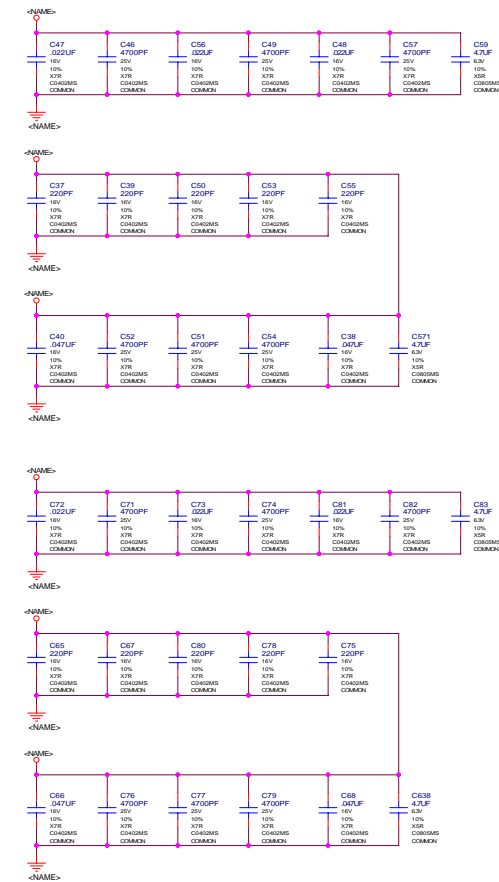
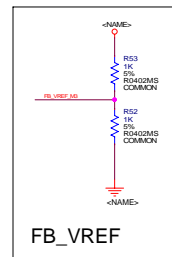
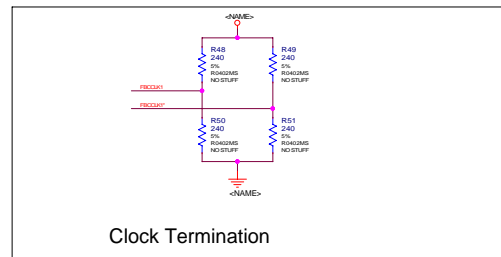
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



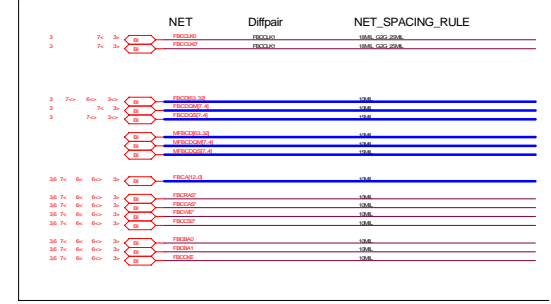
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



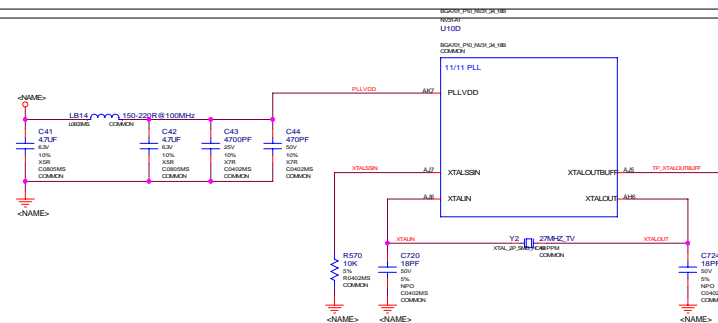
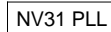
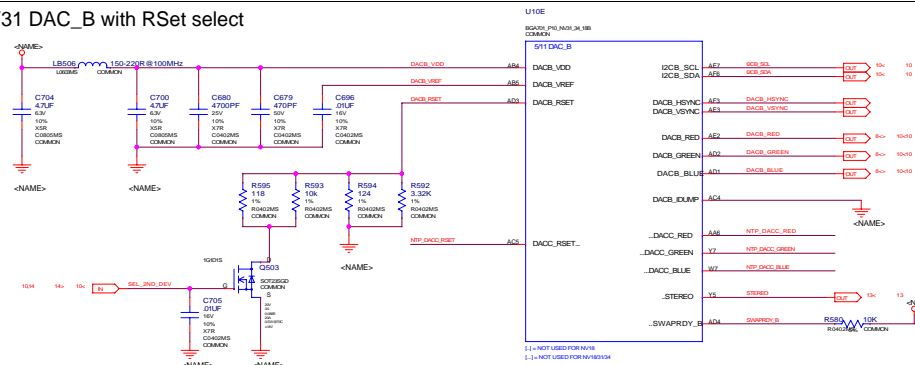
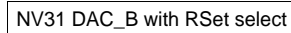
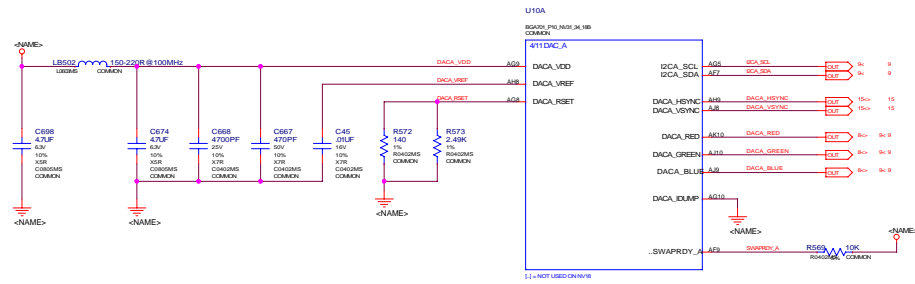
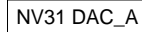
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



FB_VREF

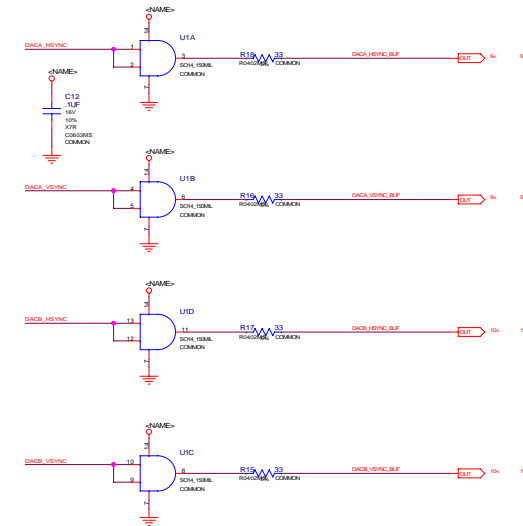


NET		NET_PHYSICAL_TYPE	VOLTAGE
10	DACA_VDD	10M_TDRIVE	3.3V
10	DACA_DMIF	0M_TDRIVE	
10	DACA_DMIF2	0M_TDRIVE	
10	DACB_VDD	10M_TDRIVE	3.3V
10	DACB_DMIF	0M_TDRIVE	
10	DACB_DMIF2	0M_TDRIVE	
10	PL_VDD	10M_TDRIVE	3.3V

NET		NET_PHYSICAL_TYPE	NET_SPACING_RULE
10	XTALOUT	0M_TDRIVE	10M

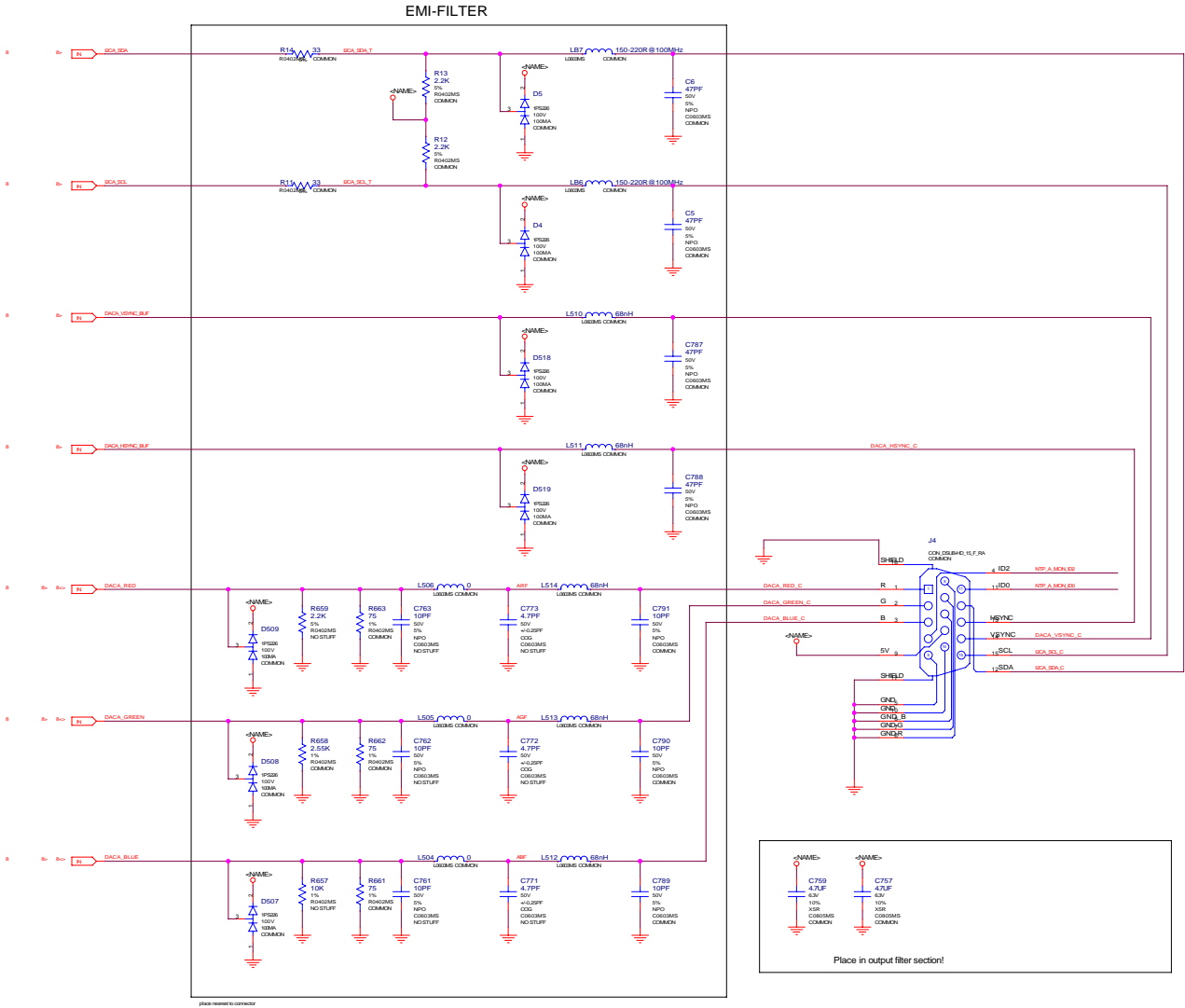
NET		NET_SPACING_RULE
10	DACA_GND	20M_GSG_20M
10	DACA_GNDEN	20M_GSG_20M
10	DACA_BLUE	20M_GSG_20M
10	DACB_GND	20M_GSG_20M
10	DACB_GNDEN	20M_GSG_20M
10	DACB_BLUE	20M_GSG_20M

SYNC Buffer	
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Primary Display (DACA), DB15 only!

NET	NET_SPACING_RULE
REF	20MIL_G02_20MIL
REF	20MIL_G02_20MIL
REF	20MIL_G02_20MIL
DACA_RED_C	20MIL_G02_20MIL
DACA_GREEN_C	20MIL_G02_20MIL
DACA_BLUE_C	20MIL_G02_20MIL



Place all filter components
on the side nearest to the
reference GND plane!

Route all signals only on
layers referenced to GND!

Don't split the reference
GND plane beneath
a RGB signal!

Place all filter components
on the side nearest to the
reference GND plane!

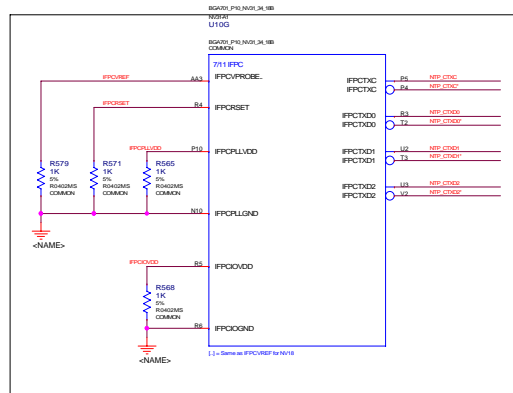
Don't split the reference
GND plane beneath
a RGB signal!

[illegible]

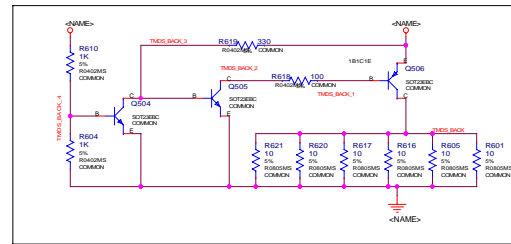
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		10	REF	2000_GSD_2000
11	11	10	CHANCE_BRED_C	2000_GSD_2000
11	11	10	CHANCE_KITTEN_C	2000_GSD_2000
11	11	10	CHANCE_BALUS_C	2000_GSD_2000
		10	CHANCE_BRED_BW	2000_GSD_2000
		10	CHANCE_GIRAFFA_BW	2000_GSD_2000
		10	CHANCE_BEAR_BW	2000_GSD_2000
13	13a	10	WERNER_C	2000_GSD_2000
13	13b	10	WERNER_C_CROSSBUD	2000_GSD_2000
13	13c	10	WERNER_CROSSBUD	2000_GSD_2000

INTERNAL DUAL LINK TMDS POWER AND DECOUPLING

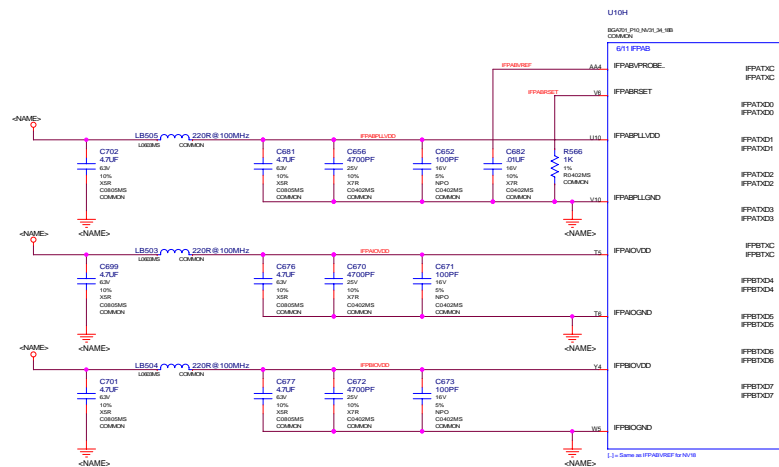
Unused Transmitter



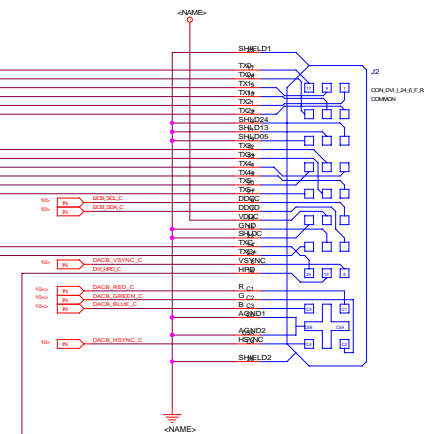
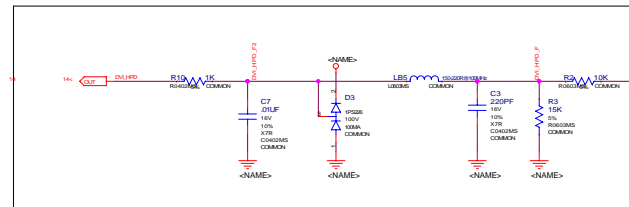
TMDS backdrive prevention

[illegible]

DualLink Transmitter



Hotplug Detection



Micro-Star International Co., LTD.

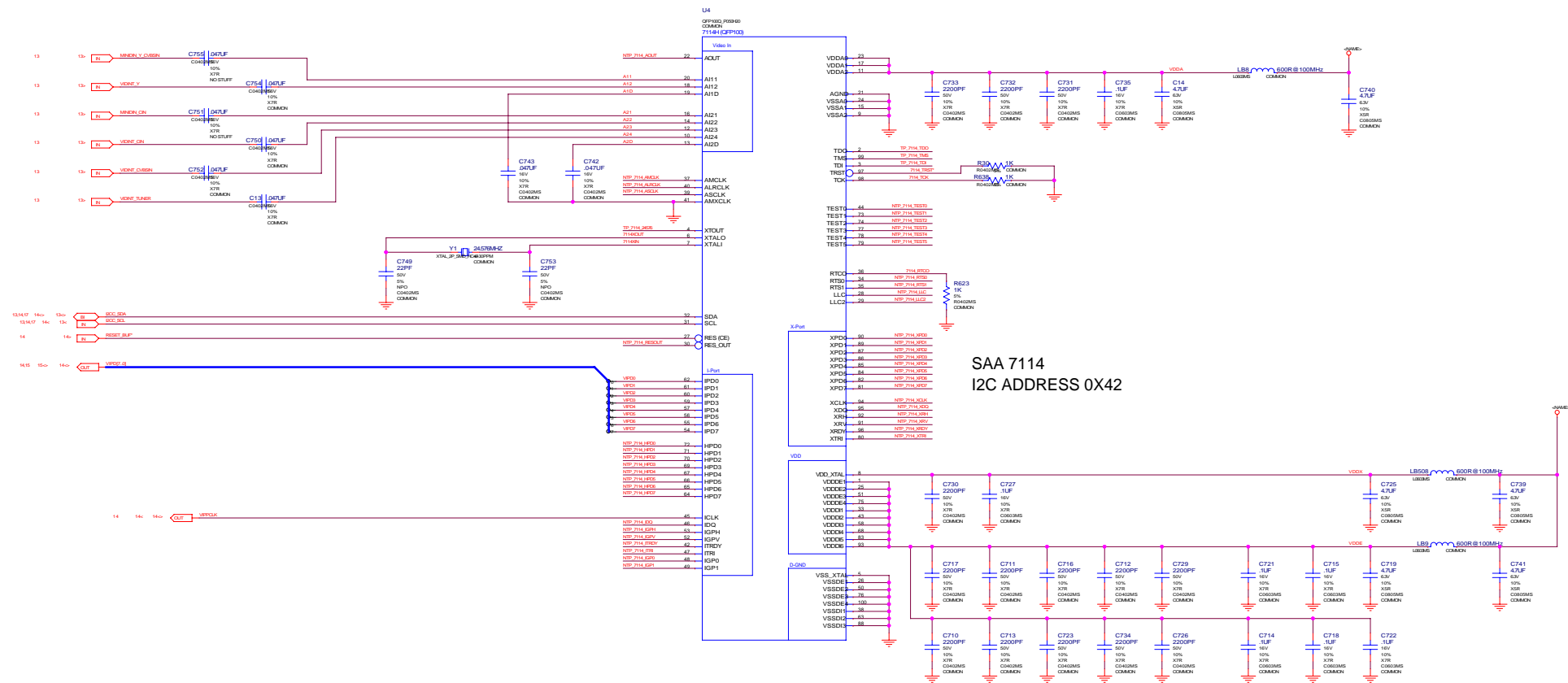
MS-8912 base on P141-A03 modify

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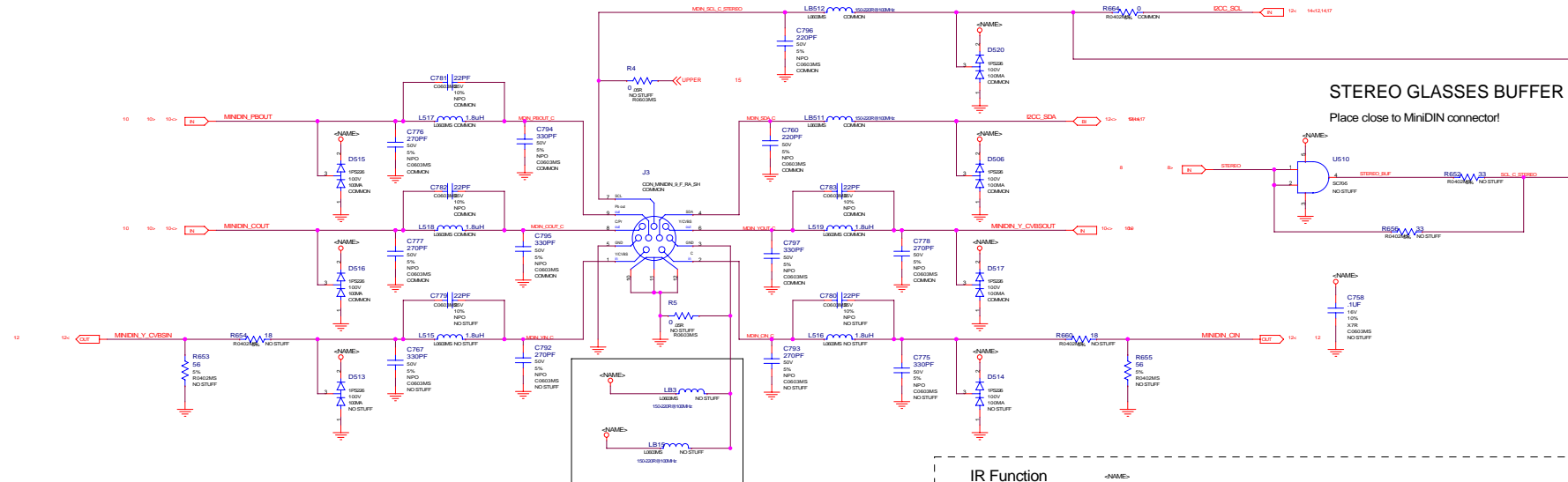
Size	Document Number	Rev
Custom		000

Custom	INTERNAL DUAL LINK TMD5 POWER AND DECOUPLING	300
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VIDEO CAPTURE

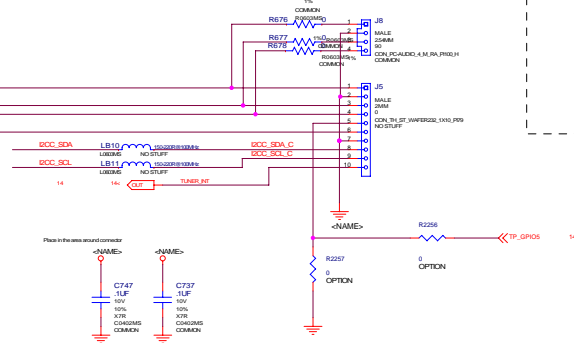
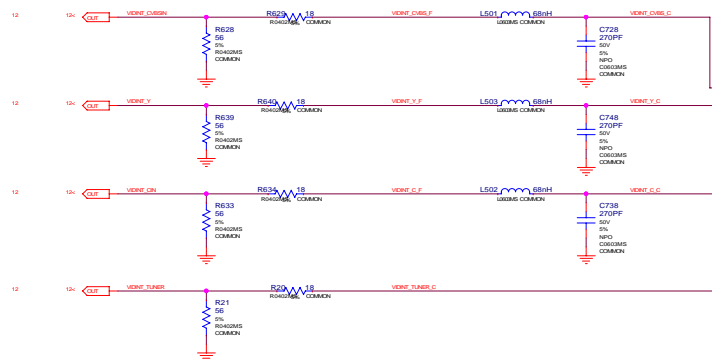


VIDEO IN/OUT CONNECTOR /STEREO GLASSES

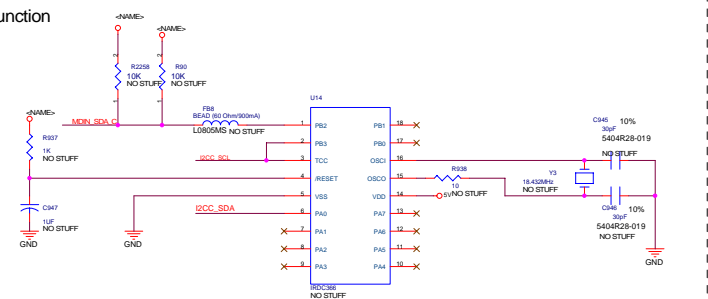


For STEREO GLASSES 3pin MiniDIN only:
Stuff bead!
And replace 0 Ohm resistor with 220PF cap!

INTERNAL VIDEO IN CONNECTOR

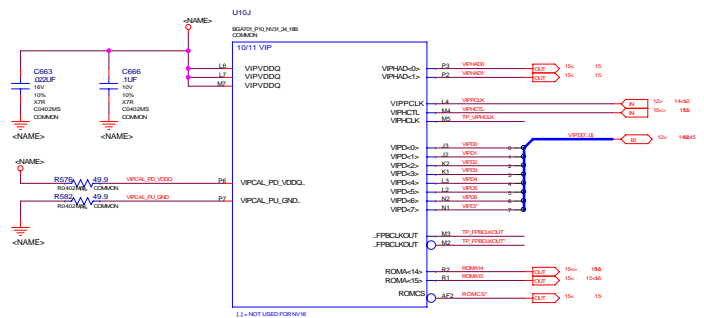


IR Function

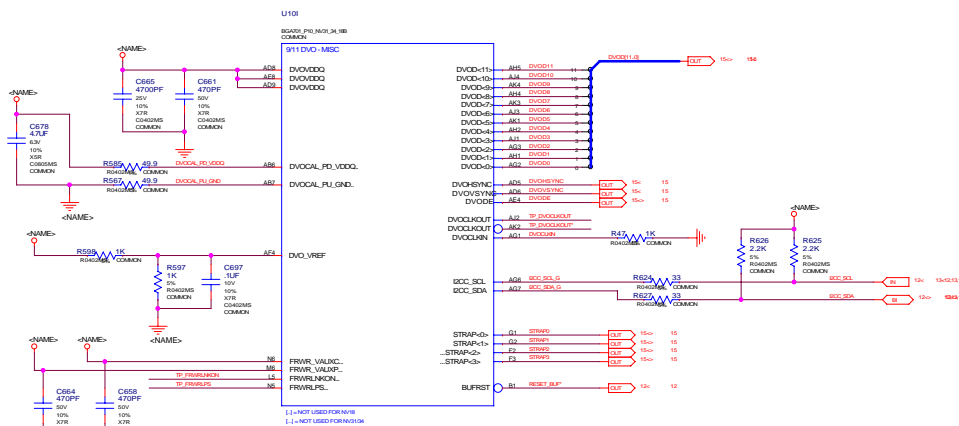


NV31 DVO, VIP AND GPIO SECTION, FAN CONTROL AND TEMP SENSOR

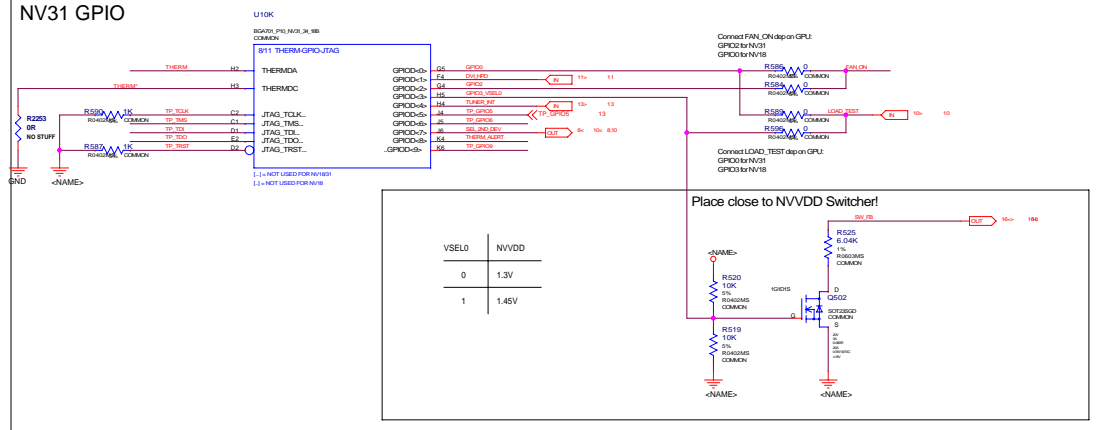
NV31 VIP



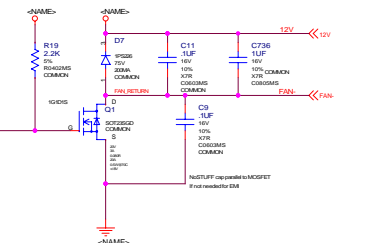
NV31 DVO



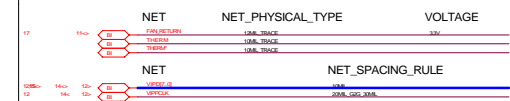
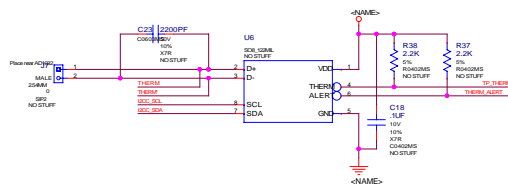
NV31 GPIO



FAN Control

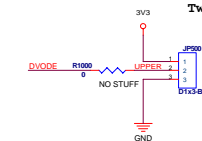



TEMP Sensor



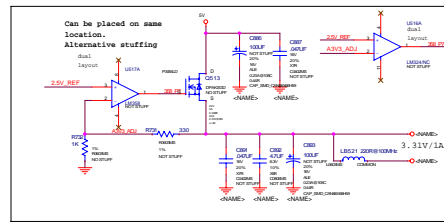
OR MASK
1 \Rightarrow DESIRED=1 AND MASK=0

BIOS (serial)



	Micro-Star International Co., LTD.		
	MS-8912 base on P141-A03 modify		
	Size Custom	Document Number NV31 BIOS STRAPPING	Rev 300

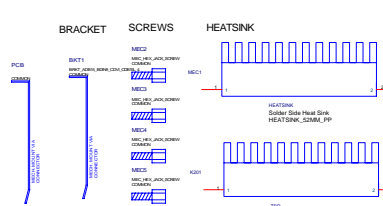
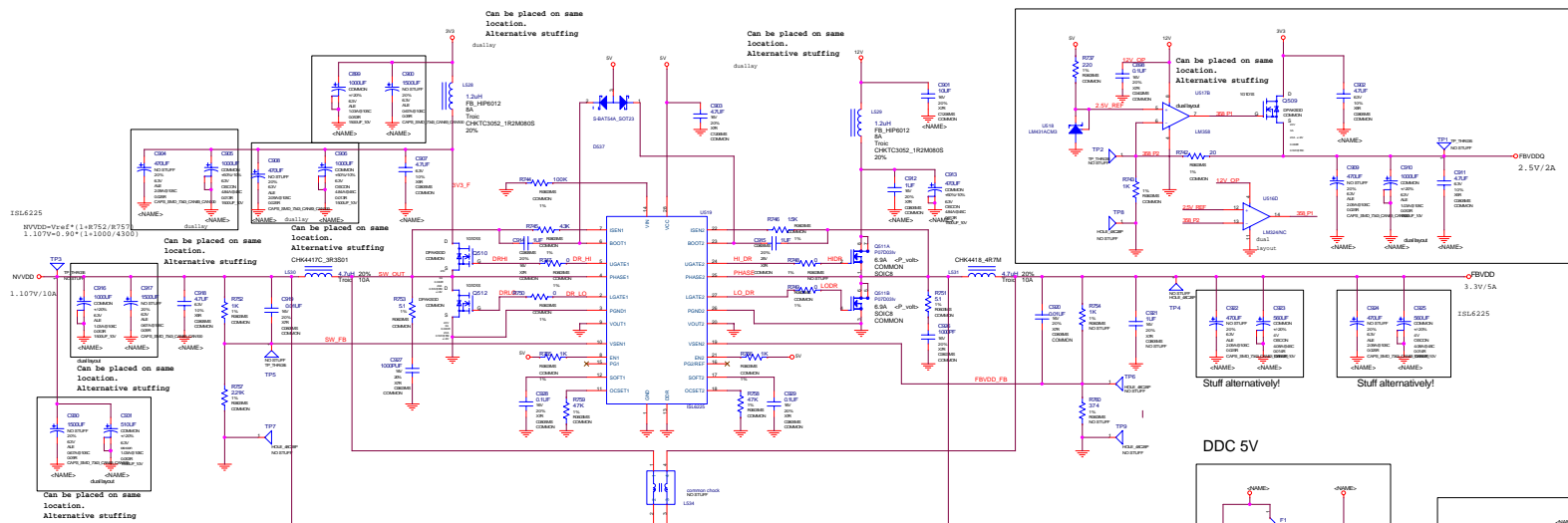
ANALOG 3V3



The diagram shows a 555 timer configured as a monostable multivibrator. The circuit includes a 555 timer, a 10k resistor, a 100k resistor, a 100nF capacitor, and a 100pF capacitor. The output is connected to a 5V supply and a 100k resistor. The circuit is powered by a 5V supply and a 100k resistor.

[illegible]

Replaced ISL6529 with ISL6225.
Replaced P07D03LV with APM7312.

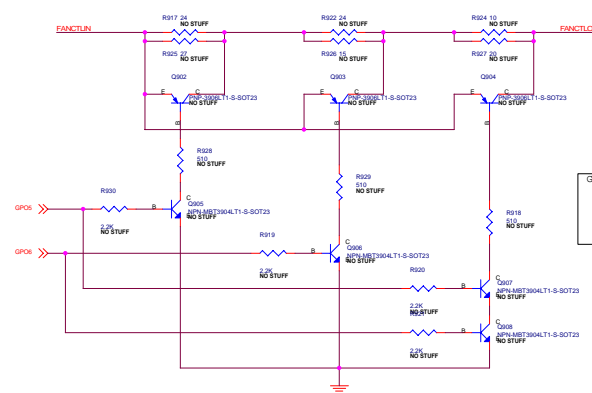
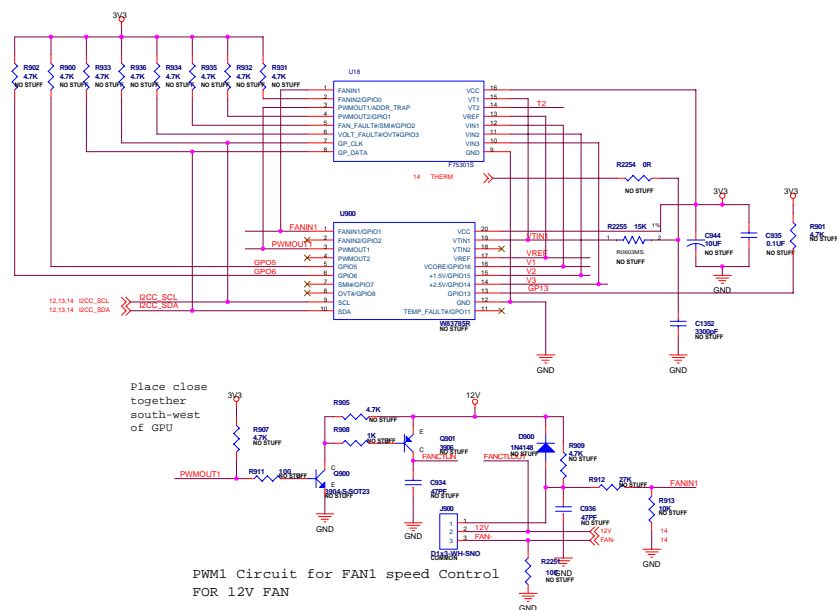
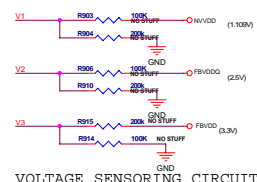
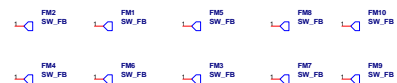


$$\begin{aligned} \text{FBVDDQ} &= V_{\text{Ref}} * (1 + R_{\text{top}} / R_{\text{bot}}) \\ 2.5\text{V} &= 0.800\text{V} * (1 + 2.37\text{k} / 1.13\text{k}) \\ 2.5\text{V} &= 1.250\text{V} * (1 + 1.02\text{k} / 1.02\text{k}) \end{aligned}$$

$$V_o = [0.9V * (R_{top} + R_{bot})] / R_{bot}$$

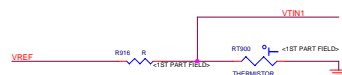
25 FBVDD = [0.9V * (1K+375)] / 375 = 3.3V
 1 NVVDD = [0.9V * (1K+4.3K)] / 4.3K = 1.109V
 8B Stand Volt need 1.656 V.

H/W Monitor Funtion



GPO5	GPO6	Q1	Q2	Q3	Vout
0	0	off	off	off	9V
1	0	on	off	off	10V
0	1	off	on	off	11V
1	1	on	on	on	12V

PWM1 Circuit for FAN1 speed Control FOR 12V FAN



TEMPERATURE SENSING CIRCUIT