NV11, 1/2/4MX32 DDR, RGB, INTERNAL DVI-I, TV, AGP.

PCI DEVICE ID 0X0=0X112 FOR NV11.

STRAPS: AGP4X, SIDEBAND DIS, FAST WRITE ENA, ADP BIOS, NORMAL PCIAD, 14.318MHZ
STRAP_RAM_TYPE [5:2]=1011-1MX32 DDR SDRAM

01. List of Schematic sheets
02. HOST INTERFACE_NEW
03. FB(MEMORY)/NVXX DECOUPLING
04. NVXX BOOT STRAPS
05. DAC and MEDIA PORT
06. LOWER SDRAM FBI
07. BT & CH TV ENCODER
08. DFP/DVI/CLK_DVR
09. DC-DC CONVTR

HISTORY REV. :

1) Based on P39-A00

2) Schematic changes; role rev to B00
   -remove BT device
   -strap resistor changes
   -add/remove resistors and caps
   -remove high dropout reg (u514)
  - R502 changed from 20K to 10K

3) C00:
   - Swapped LVDS signals back to "Rev A connections".

   - Hi Freq. cap arrays Decoupled to GND:
   1) SMB_CLK
   2) SMB_DAT
   3) PID2_I2C_CLK (aka I2CSCL)
   4) PID3_I2C_DAT (aka I2CSDA)
   5) PID3_I2CDAT (aka PID3)
   6) PID2_I2CCLK (aka PID2)
   7) PID1
   8) PID0

   - Added 10K, NO STUFF, from AGP_BUSY# to +3.3VSUS.

   - Connected C279 to +5VSUS.

4) D00:
   A) Power U513 from +3.3vsus instead of +3.3vrun.
   B) Changed R68 to 10K. Change R69 to 9.09K (to decrease static current draw in +2.5v regulator circuit)
   C) (layout change) Moved MVREF divider & caps (R172, R175, C424, C426) next to the RAMs
   D) Added 0-Ohm STUFF OPTION resistors for memory core FBVDD to go from either +3.3VSUS or +2.5V.
   E) Moved C836, C837, C247, C248, C270 to FBVDD
   F) Removed R166 & R126 (DFPCLK is unused)
   G) Moved pin 1 of R501 from +5vsus to +5vrun
   H) (layout change) Split 5vsus bus into +5vrun and +5vsus
   I) Added a NOSTUFF zero ohm resistor from DFP3.3V to +3.3VRUN (adds option to remove dfp regulator
   J) Added a .022uF cap in parallel with R550 (Increase power sequencing delay)
   K) Changed C57 to 330uF, d-size case
   L) Changed C828 is 330uF, d-size case
   M) (layout change) Moved IMI530 part (designator ui) to fix shorting problem
   N) (layout change) Connected J1 connector shield to ground
   O) (layout change) Connected mounting holes to ground. Don't plate inside of hole to allow for pimnut
   Q) Route VDDEN (GPIO3) to pin 166 on connector J10 (FPVCC)
   P) Added 2 Standoffs (1 metal, 1 plastic) and thermal pad per Dell's request.
   R) Connected pin 24 of J10 (ZV_PCLK) to pin B4 (VIPPCLK) on U29 (NV11)
   S) Created +5VRUN net, connect to pin 168 on J10 (+5VRUN)
   T) R155 = 357ohm, R150 is no-stuff
   U) Removed R152. Connected CHTVPIO_1 to CHTVPIO_0.
   V) Adjusted PCB form factor
   W) Changed R548 from 480K 5% to standard 390K 5%
   X) Changed R550 from 600K 5% to standard 620K 5%
   Y) Configured memory to 2Mx32-100lb (R524=NO STUFF, R523= STUFF
   Z) Changed R154, R156 to 10K.

5) E00:
   - Implemented ECO change list "P41_D00_ECOs-X02.doc" in current working directory:
   \\nvcorp\applied\designs\working\nv11\XXX-P0041-0000-E00
   - Sync'd up netlist with Layout.
   - Connect the S0 input of the IMISM530 to 3.3VRUN instead of CLK_VDD

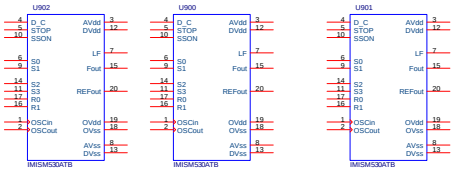
6) E02:
   - Added 1000pf cap (C535) in parallel to R535 for EMI supression.
   - Changed mem termination from +3.3VRUN to +3.3VSUS. Affects R183-R186, C416

6a) E02-X01: Change C279 to no stuff per Dell request.

7) E03: Added SMD0603 foot print to the backside of board, C536 to DVI, DFP page.

{Item}\t{Quantity}\t{Reference}\t{USR DFINE}\t{PN}\t{Assembly}\t{Value}
{Assembly}{Source Package} {Value}{PN}{AVL1}{AVL2}{AVL3}{AVL4}{AVL5}

Micro-Star International Co., LTD.			
MS8832,1/2/4MX32-DDR,TV			
Size: C	Document Number: List of schematic sheets		Rev: 100
Date: Tuesday, April 30, 2002	Sheet 1 of 9		



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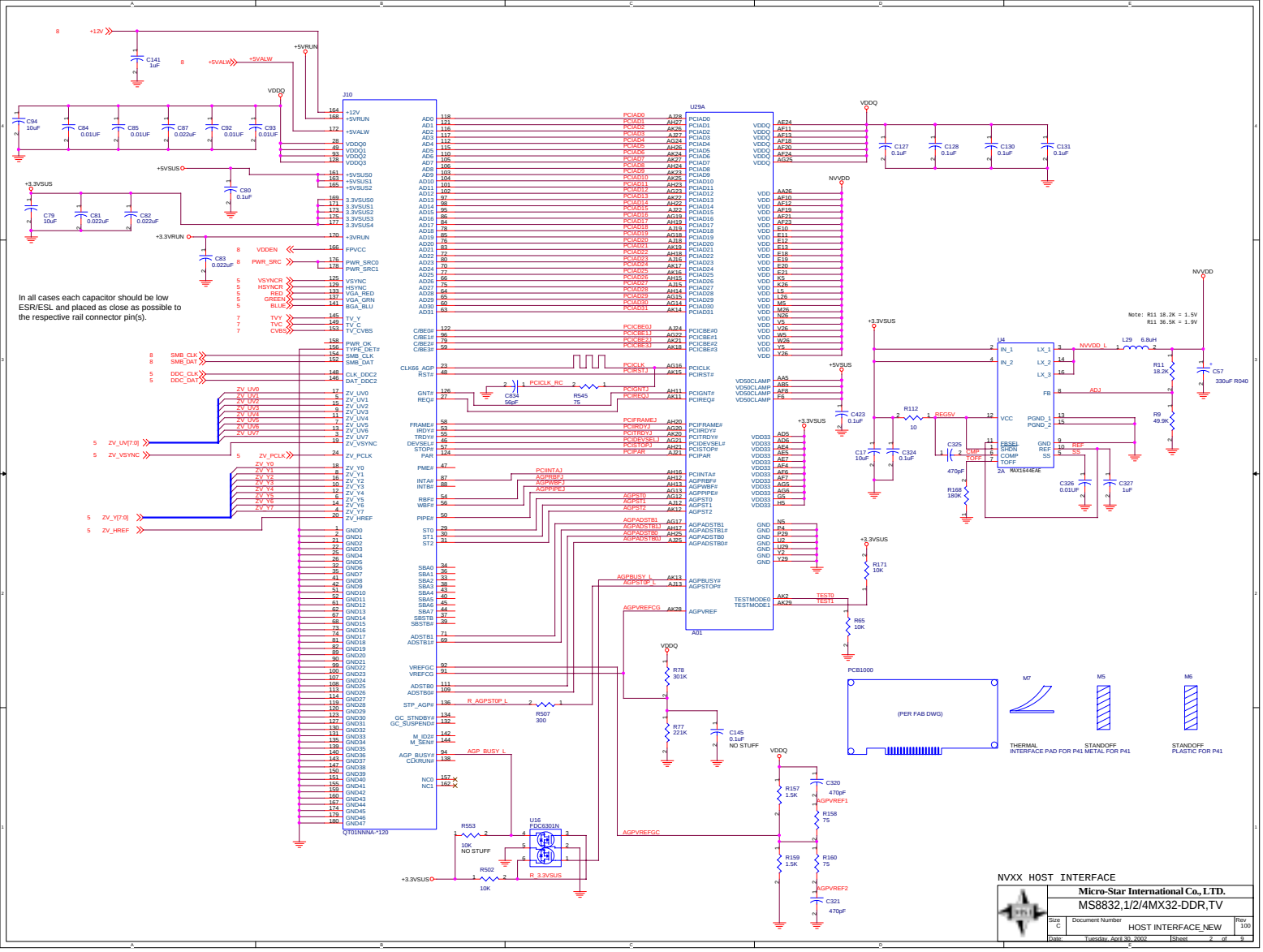
In all cases each capacitor should be low ESR/ESL and placed as close as possible to the respective rail connector pin(s).
J10
QT01NNNA-*120
U29A
A01
U4
NAX1644EAE
U16
FDC6301N
PCB1000
(PER FAB DWG)
M7
THERMAL INTERFACE PAD FOR P41
M5
STANDOFF METAL FOR P41
M6
STANDOFF PLASTIC FOR P41
Note: R11 18.2K = 1.5V
R11 36.5K = 1.9V
NVXX HOST INTERFACE
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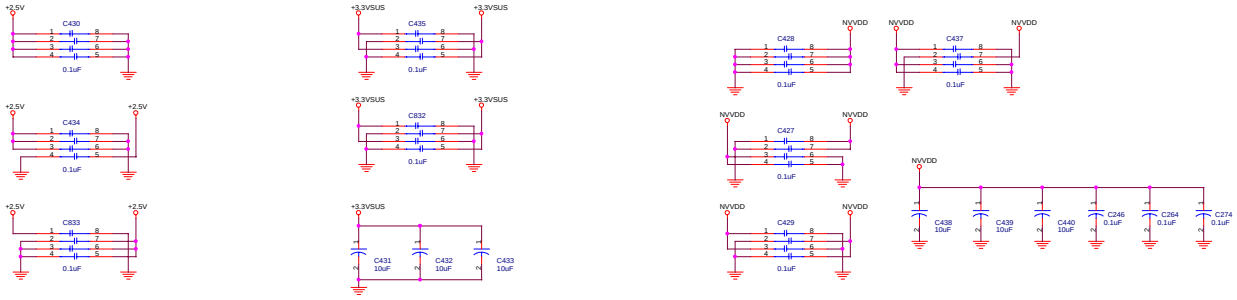
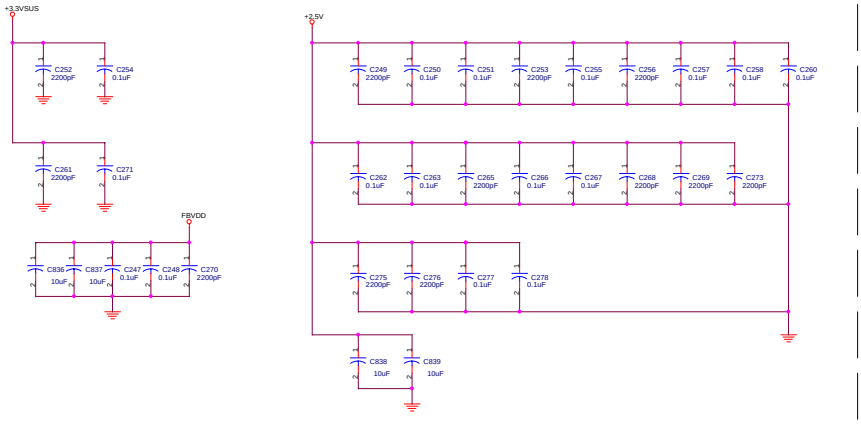
NV11 DECOUPLING



FB (MEMORY) DECOUPLING



FB/NVXX DECOUPLING

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NVXX HOST STRAPS

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Size: C	Document Number: NVXX BOOT STRAPS		Rev: 100
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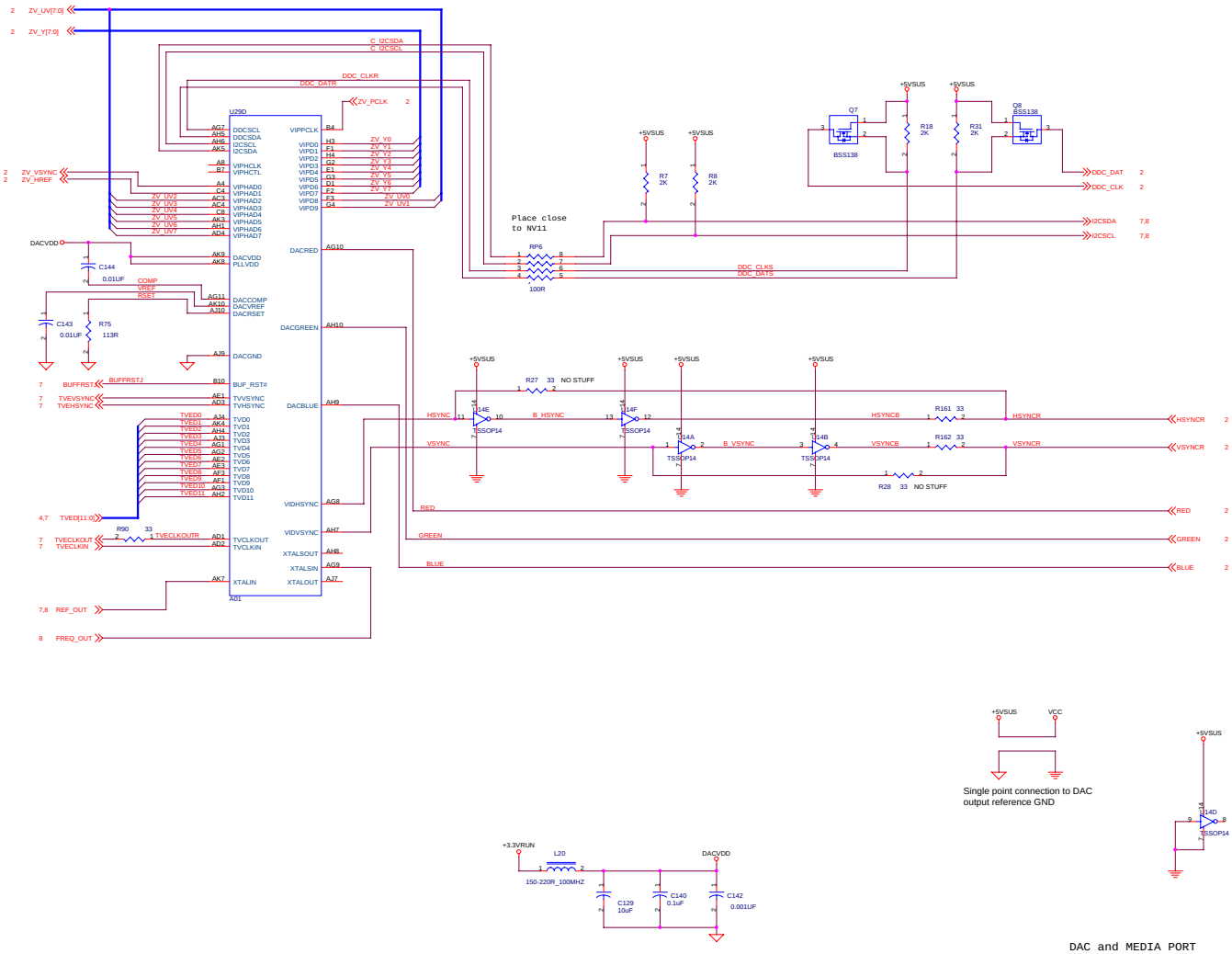

DAC and MEDIA PORT

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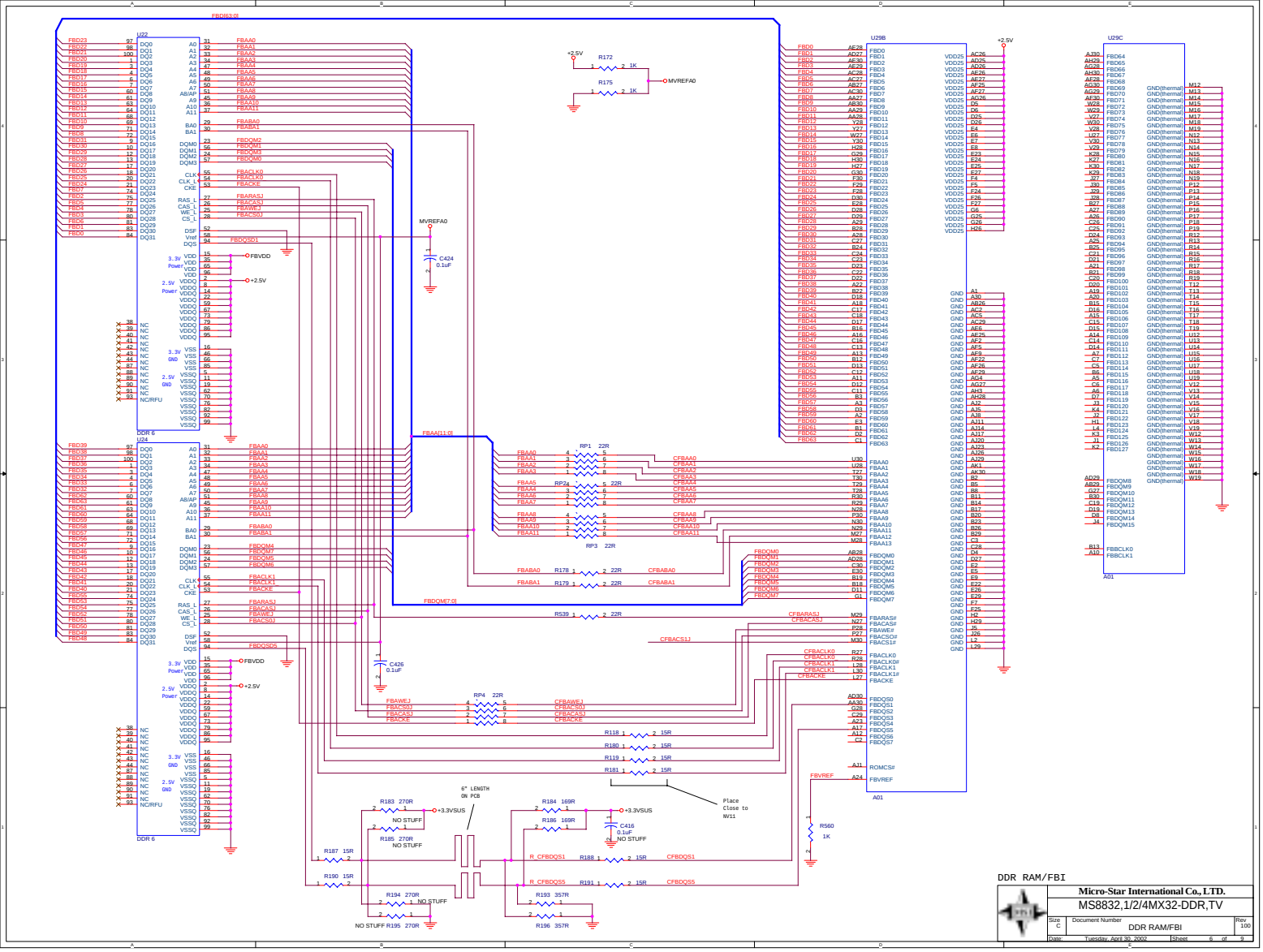
DDR RAM/FBI
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MS8832,1/2/4MX32-DDR,TV
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DDR RAM/FBI
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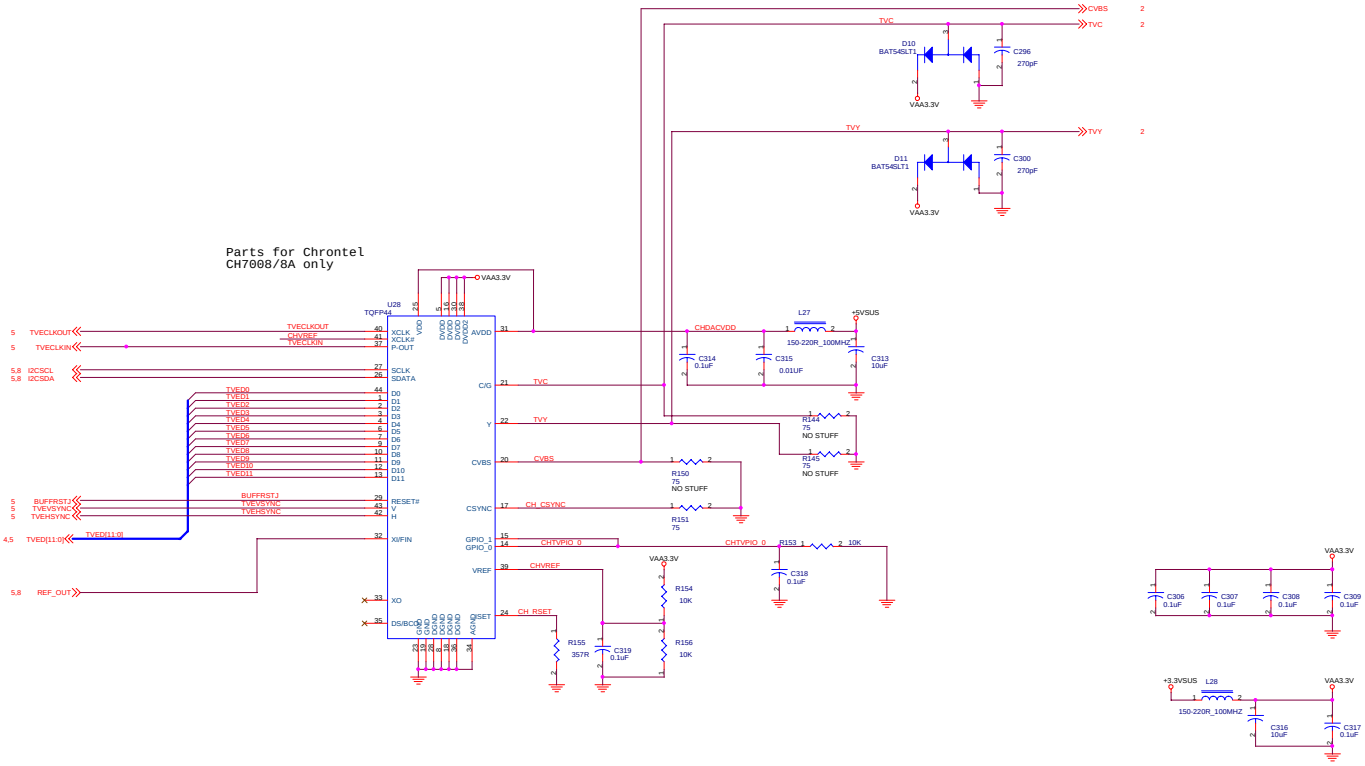

Chrontel TV ENCODER

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Size: C	Document Number: Chrontel TV ENCODER	Rev: 100
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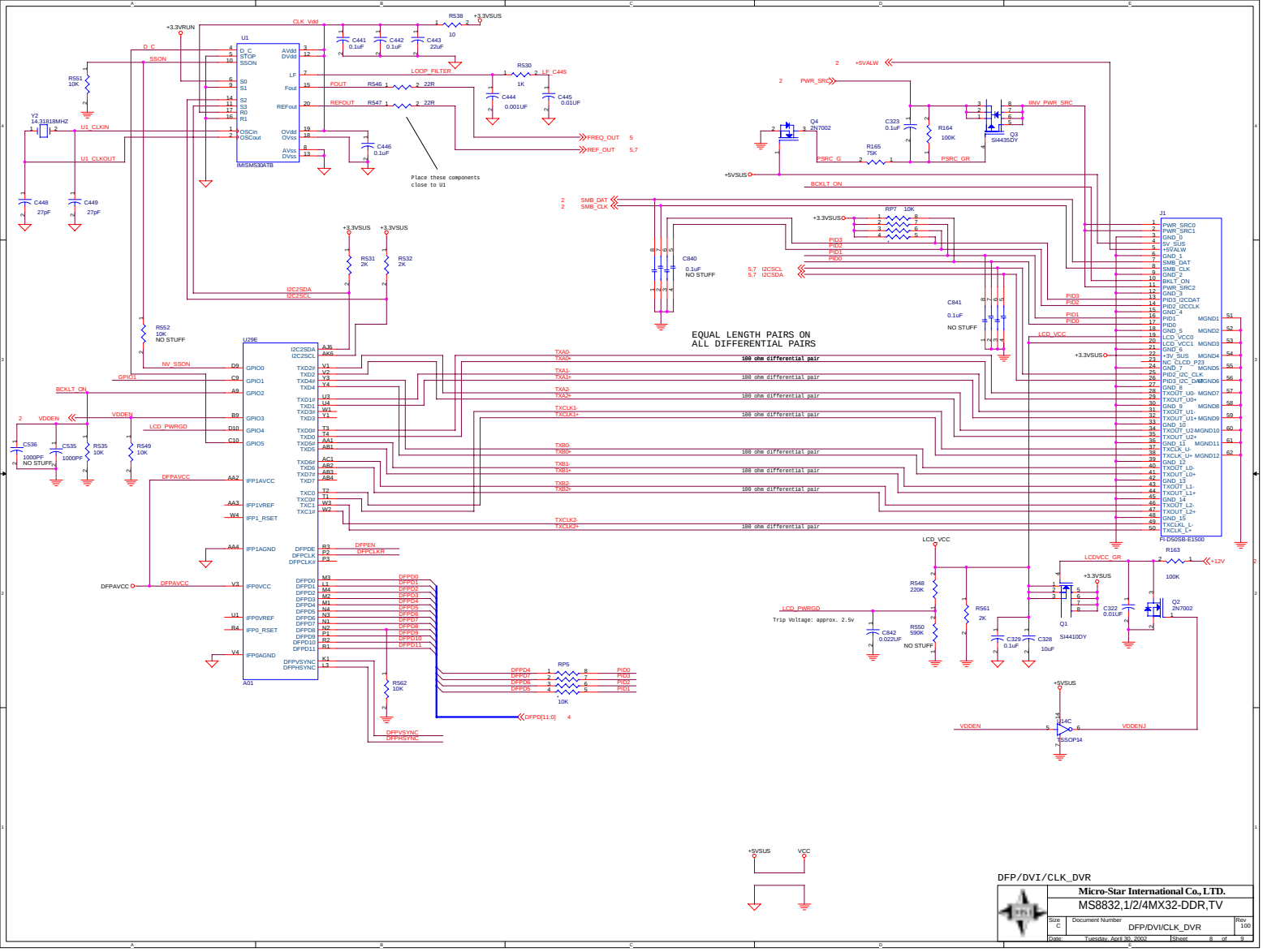

DFP/DVI/CLK_DVR

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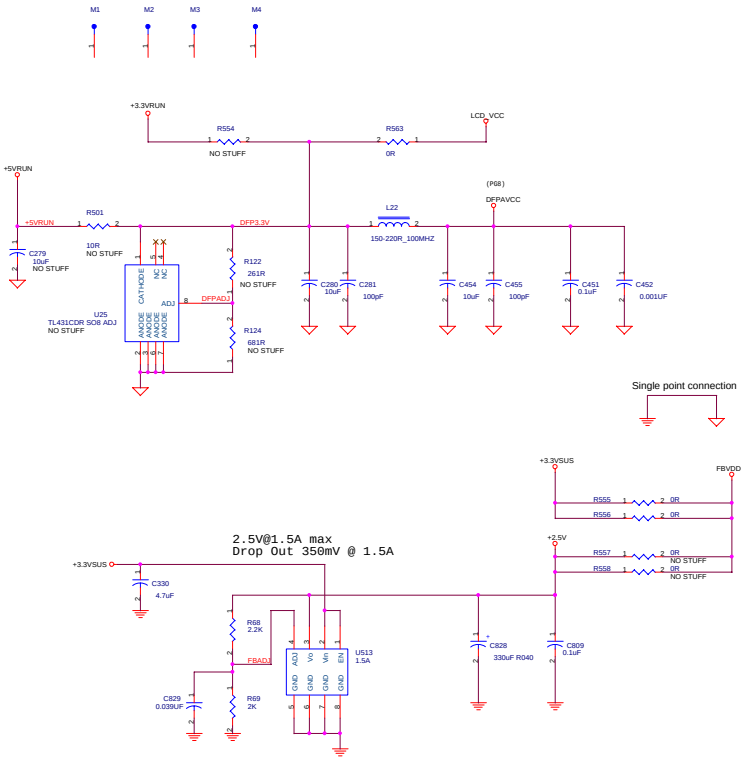

DC-DC CONTVR

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