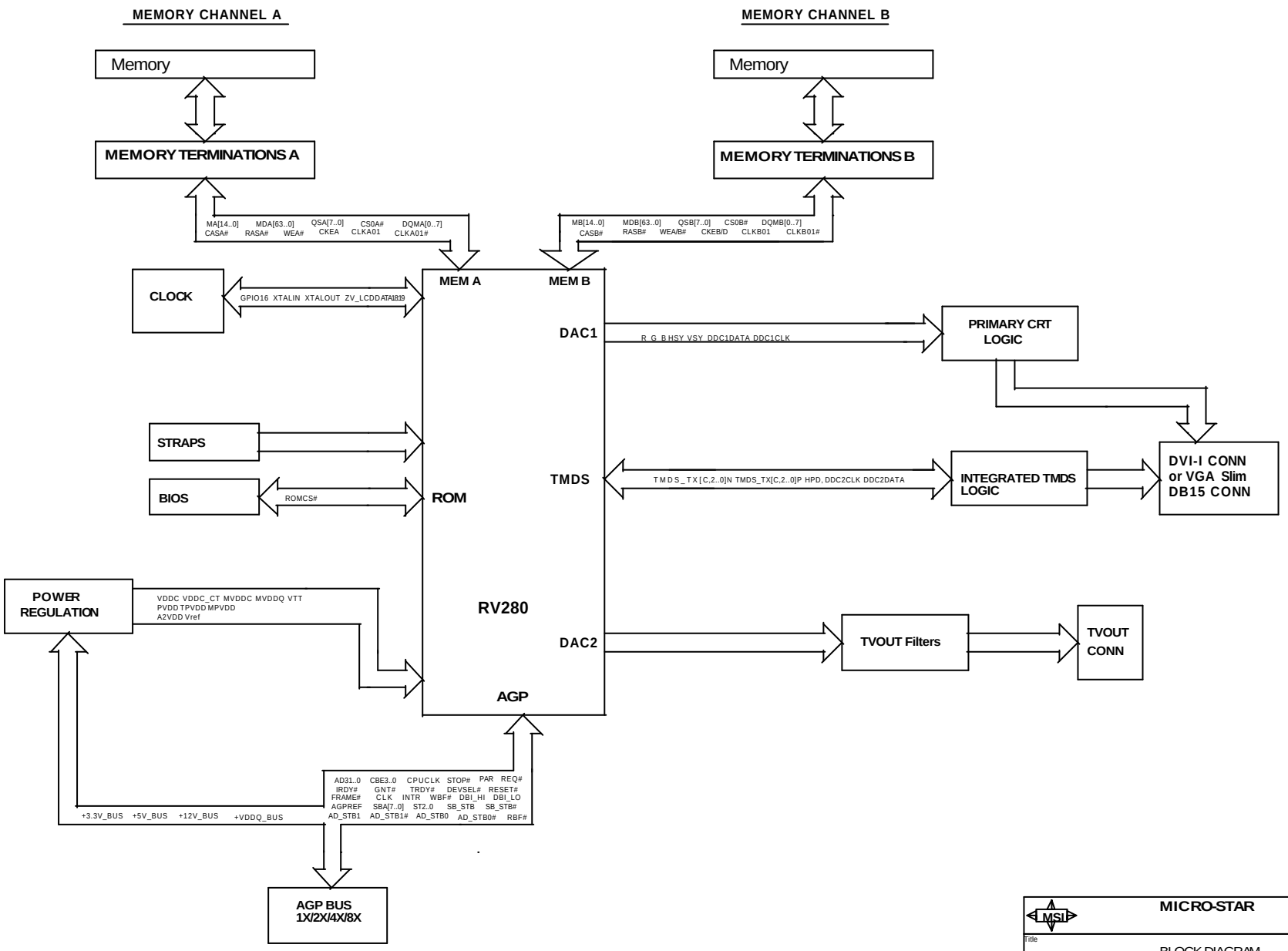
MS-8913 Ver:0A

MICRO-STAR

MSI

Cover Page

MS-8913



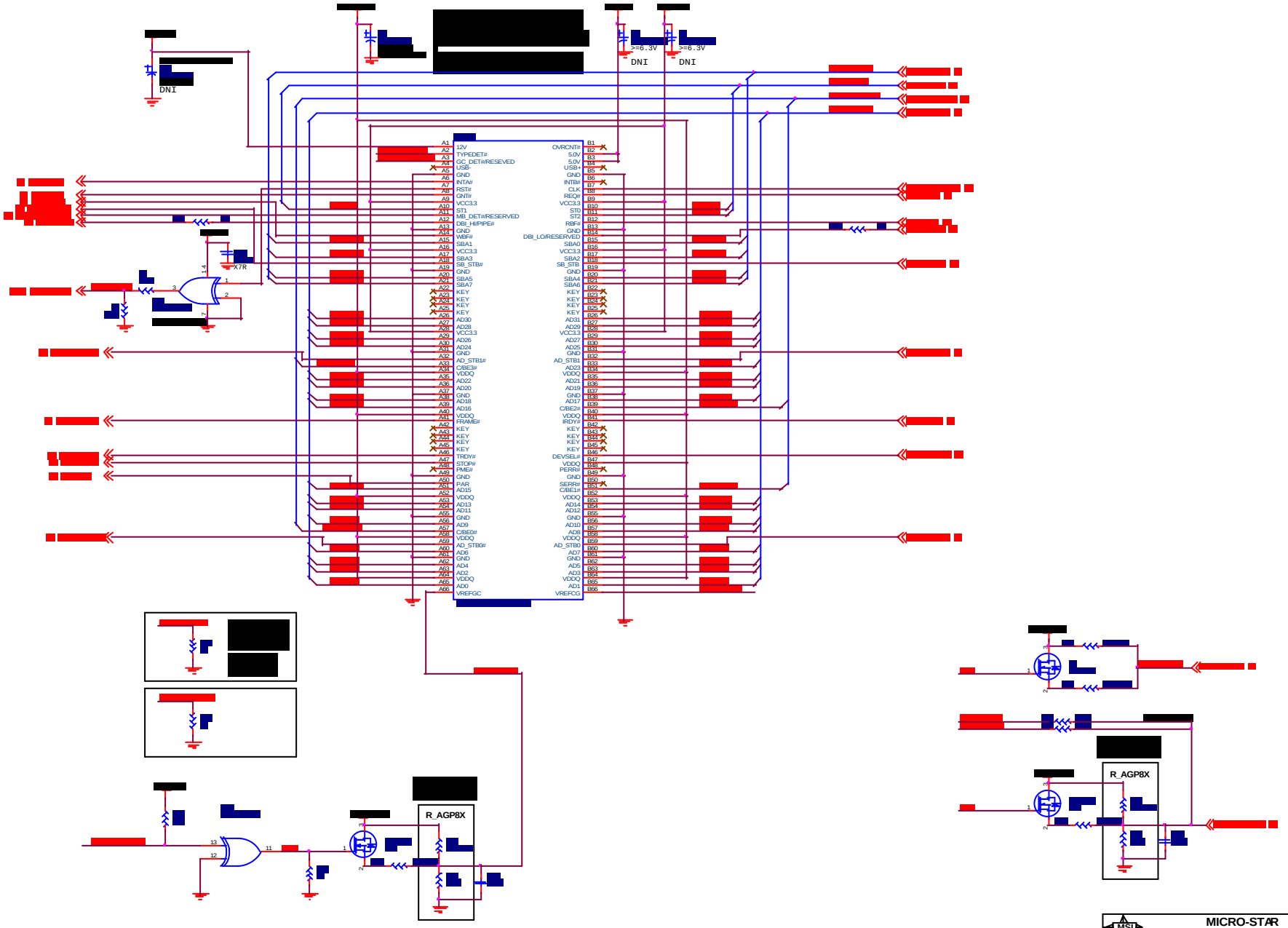
MICRO-STAR

Title: BLOCK DIAGRAM

Size | Document Number: MS-8913 | Rev: 0A

Date: Thursday, January 23, 2003 | Sheet 2 of 16

The following grounds should be routed back to their respective regulators and then tied directly to the ground plane with one via: GND_PVSS, GND_MPVSS, GND_TPVSS, and GND_A2VSSN. The other ground pins (GND_AVSSN, GND_A2VSSQ, GND_RSET, GND_R2SET) should be tied to the ground plane directly through one via as close to the pins as possible without connecting to anything else. If space is an issue it is possible to use one via for two adjacent pins.

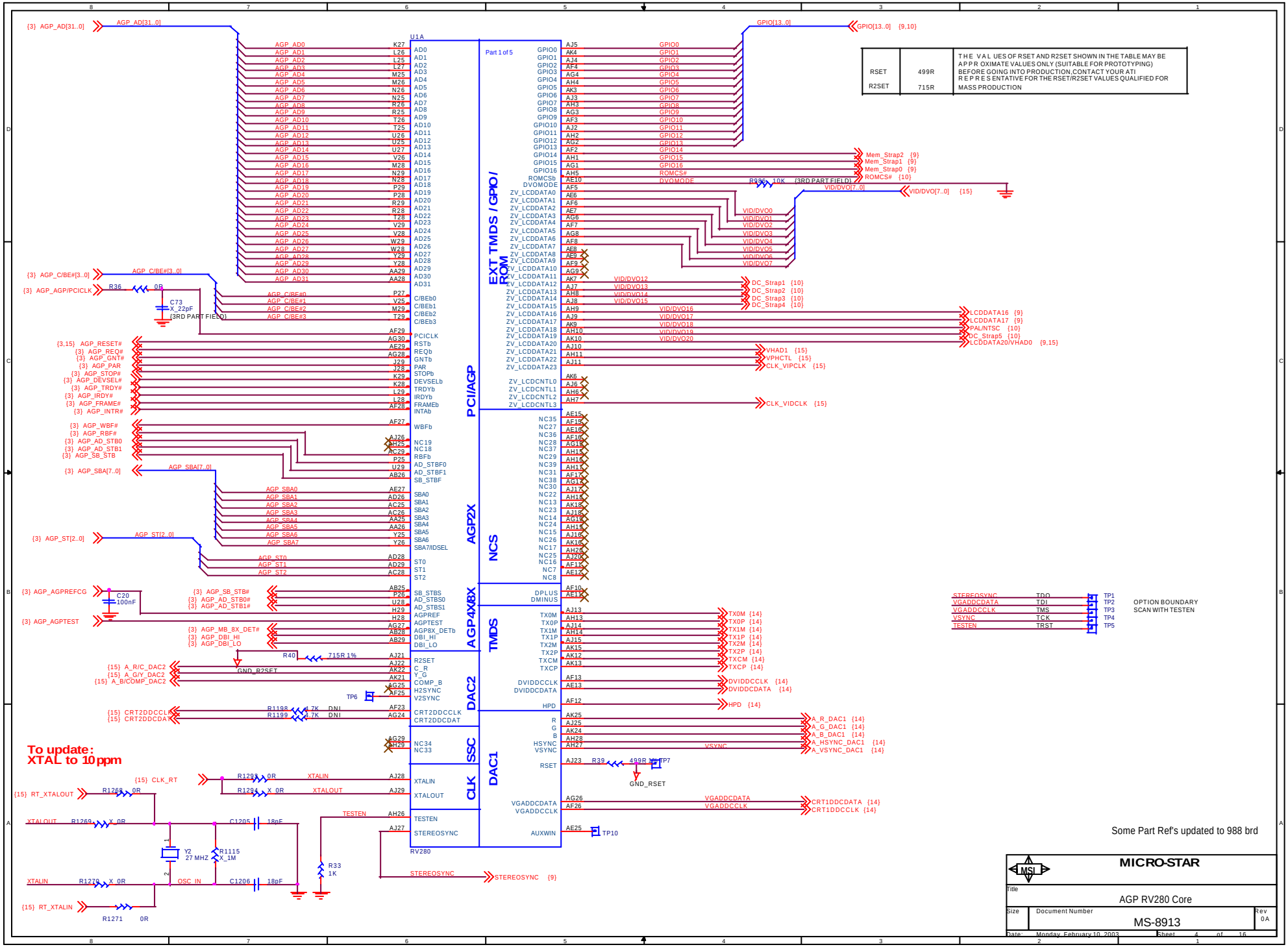


UNIVERSAL VREFGC CIRCUIT (2X, 4X, 8X)

MICRO-STAR

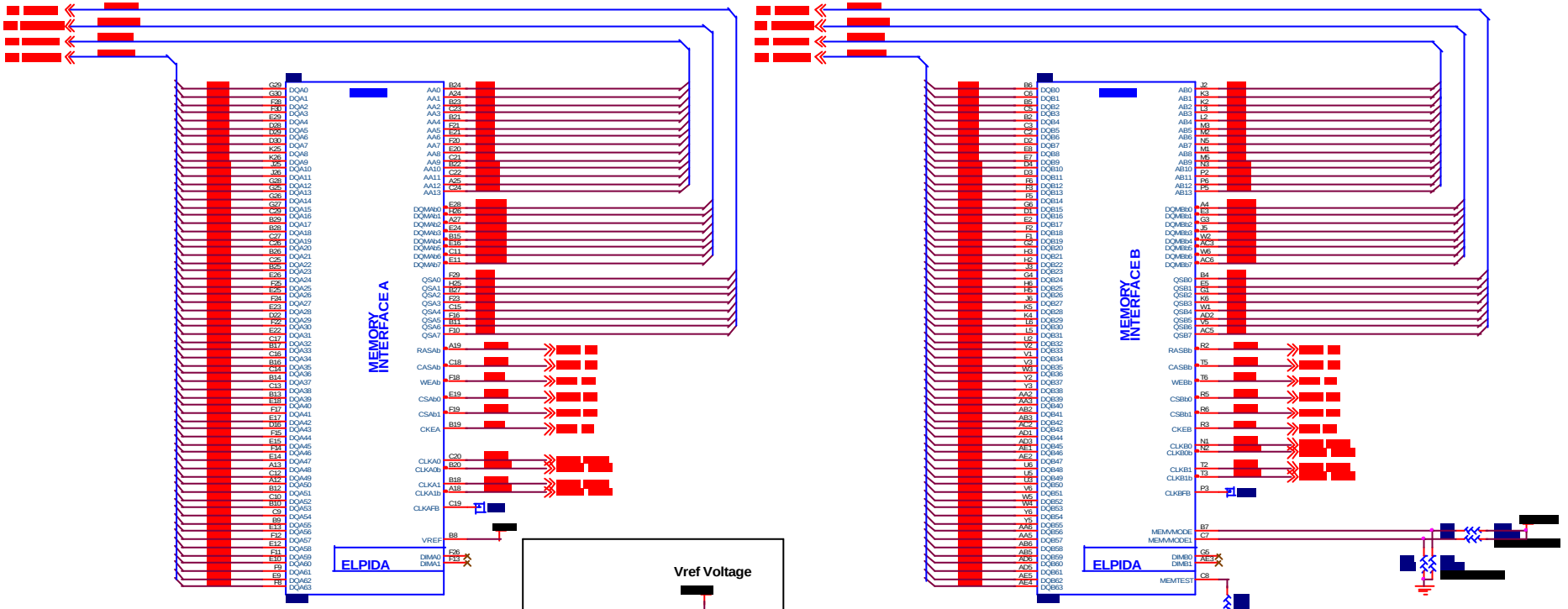
AGP AGP Bus 8X

MS-8913


U1A
Part 1 of 5
PCI/AGP
AGP2X
NCS
AGP4X8X
TMDS
DAC2
SSC
CLK
DAC1
EXT TMDS / GPIO / ROM
RV280
RSET 499R
R2SET 715R
THE VALUES OF RSET AND R2SET SHOWN IN THE TABLE MAY BE APPROXIMATE VALUES ONLY (SUITABLE FOR PROTOTYPING) BEFORE GOING INTO PRODUCTION,CONTACT YOUR ATI REPRESENTATIVE FOR THE RSET/R2SET VALUES QUALIFIED FOR MASS PRODUCTION
To update:
XTAL to 10ppm
Some Part Ref's updated to 988 brd
MICRO-STAR
AGP RV280 Core
MS-8913
Monday, February 10, 2003

MEMORY CHANNEL A

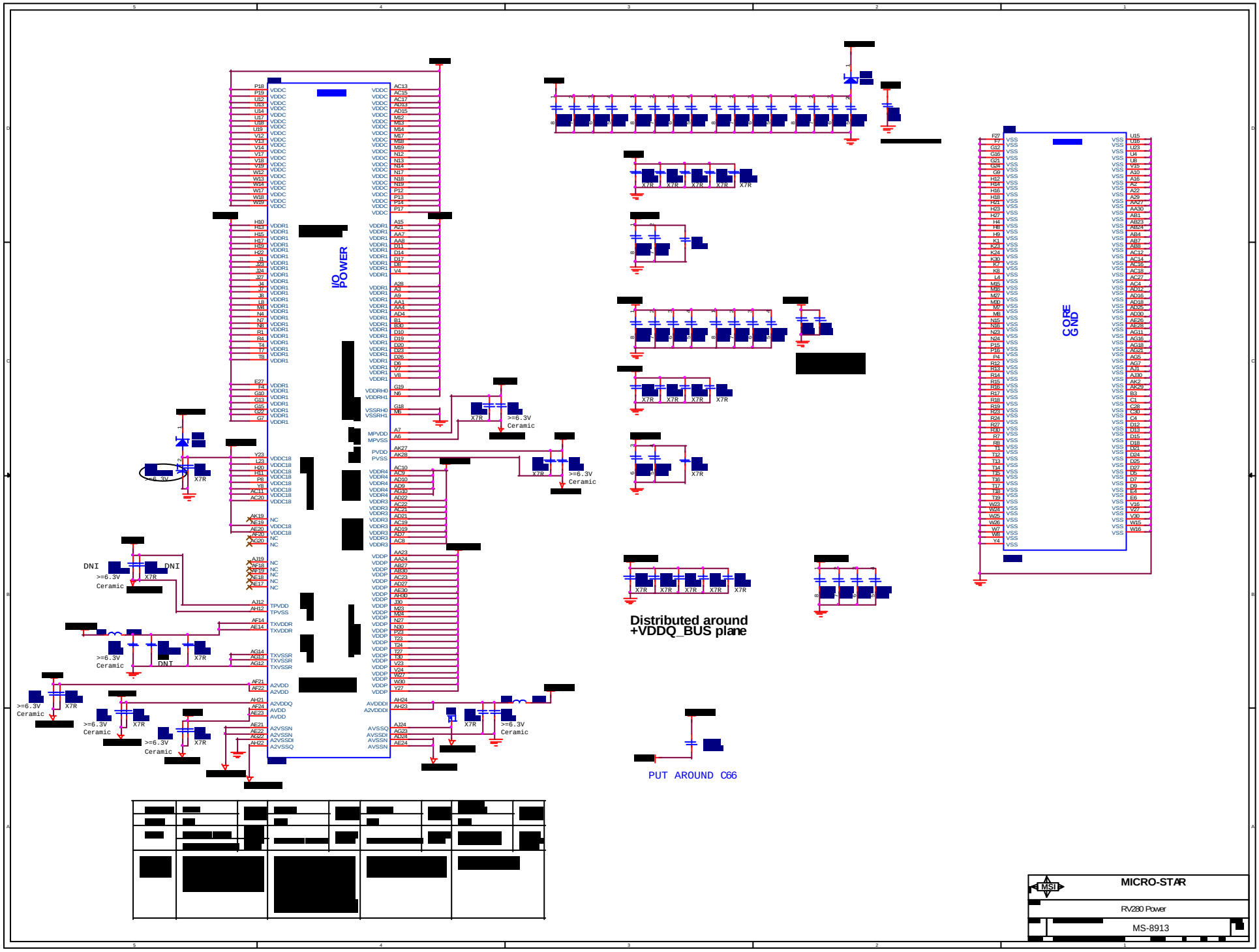
MEMORY CHANNEL B

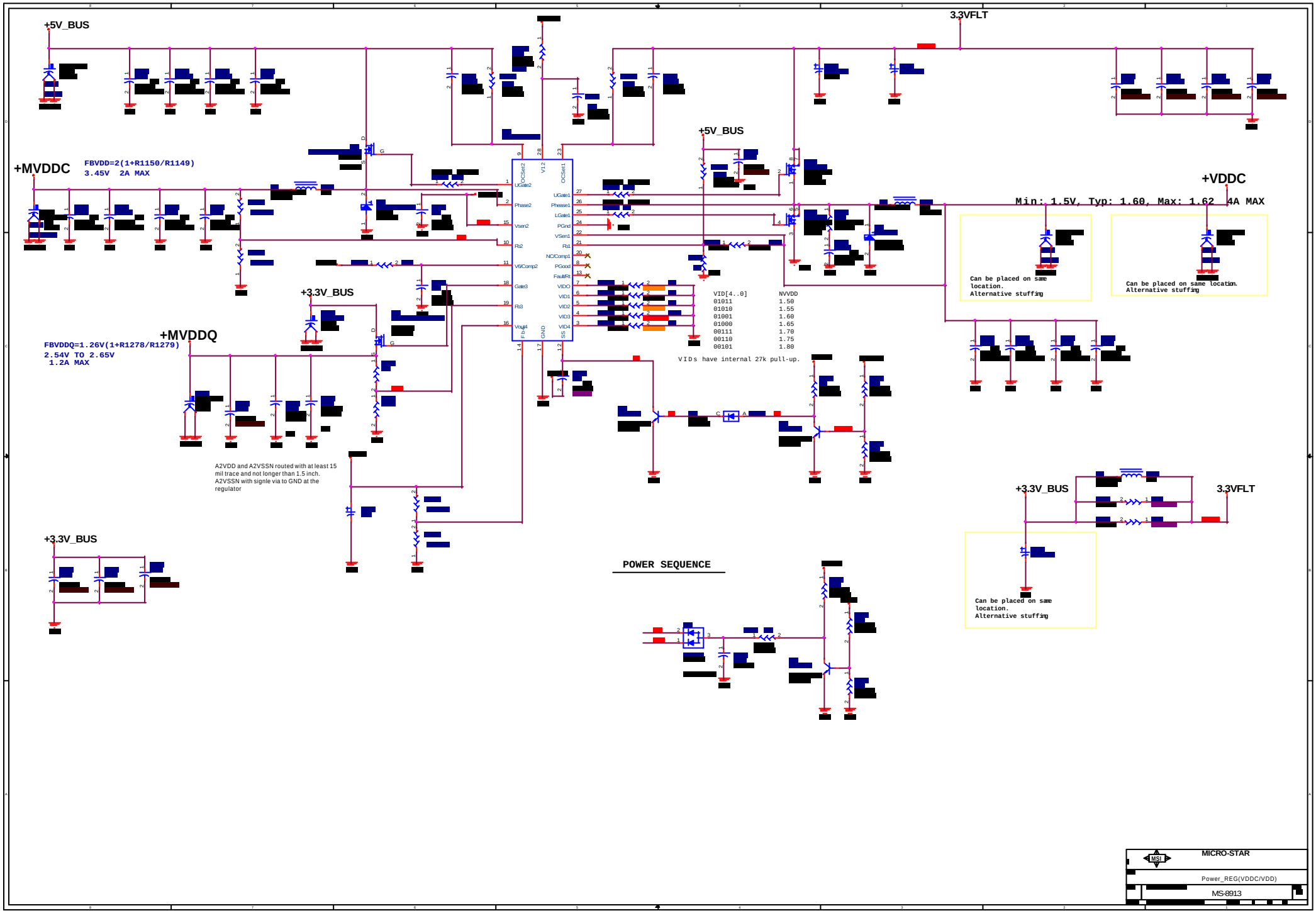


MICRO-STAR

RV280 Mem Interface

MS-8913

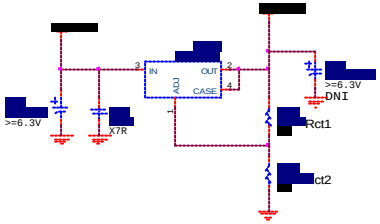

I/O POWER
CORE GND
DNI
>=6.3V Ceramic
X7R
Distributed around +VDDQ_BUS plane
PUT AROUND C66
MICRO-STAR
RV280 Power
MS-8913


+5V_BUS
3.3VFLT
+MVDDC
FBVDD=2(1+R1150/R1149)
3.45V 2A MAX
+5V_BUS
+VDDC
Min: 1.5V, Typ: 1.60, Max: 1.62 4A MAX
Can be placed on same location.
Alternative stuffing
Can be placed on same location.
Alternative stuffing
+3.3V_BUS
+MVDDQ
FBVDDQ=1.26V(1+R1278/R1279)
2.54V TO 2.65V
1.2A MAX
VID[4..0] NVVDD
01011 1.50
01010 1.55
01001 1.60
01000 1.65
00111 1.70
00110 1.75
00101 1.80
VIDs have internal 27k pull-up.
A2VDD and A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch. A2VSSN with signle via to GND at the regulator
+3.3V_BUS
3.3VFLT
Can be placed on same location.
Alternative stuffing
+3.3V_BUS
POWER SEQUENCE
MICRO-STAR
Power_REG(VDDC/VDD)
MS-8913

Regulator for VDDC_CT (Core Transform) and AVDD/A2VDDQ/AVDDDI/A2VDDDI TXVDDR, LVDDRx, MPVDD

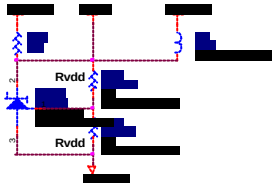
Vin = 3.3V AG P
Vout = 1.8V
Iout = 350mA + 100mA + 50mA = 500mA MAX
Iout = 600mA MAX (with PVDD/TPVDD)

	Rct1			Rct2		
1.8V				422R	3240422000	603
1.9V	1K	3240100100	603	499R	3240499000	603



Regulator for PVDD (Core PLLs) and optional TPVDD (TMDS PLLs)

Vin = 3.3V AG P
Vout = +1.8V
Iout = 25mA MAX (PVDD only)
Iout = 30mA MAX (PVDD + TPVDD)



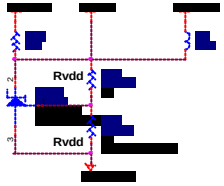
The value of resistor were chosen to reduce failure rate caused by possible defective regulators, i.e., 33R are used instead of 47R or 51R for more start up current. (3.465V - 1.8V) / 33R = 50.5mA

805 package resistor are required for sufficient power rating (0.1W rating). (3.465V - 1.8V) * 50.5mA = 0.085W; therefore, smaller resistor value would require 1206 package

Regulator for MPVDD (Memory PLLs)

Vin = 3.3V AGP
Vout = +1.8V
Iout = 10mA MAX

(Optional)

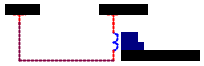


AVDD/A2VDDQ (1st DAC & 2nd DAC Band Gap)

Regulator For TPVDD (TMDS PLLs)

Vin = +3.3V AGP
Vout = 1.8V
Iout = 15mA MAX

(Optional)



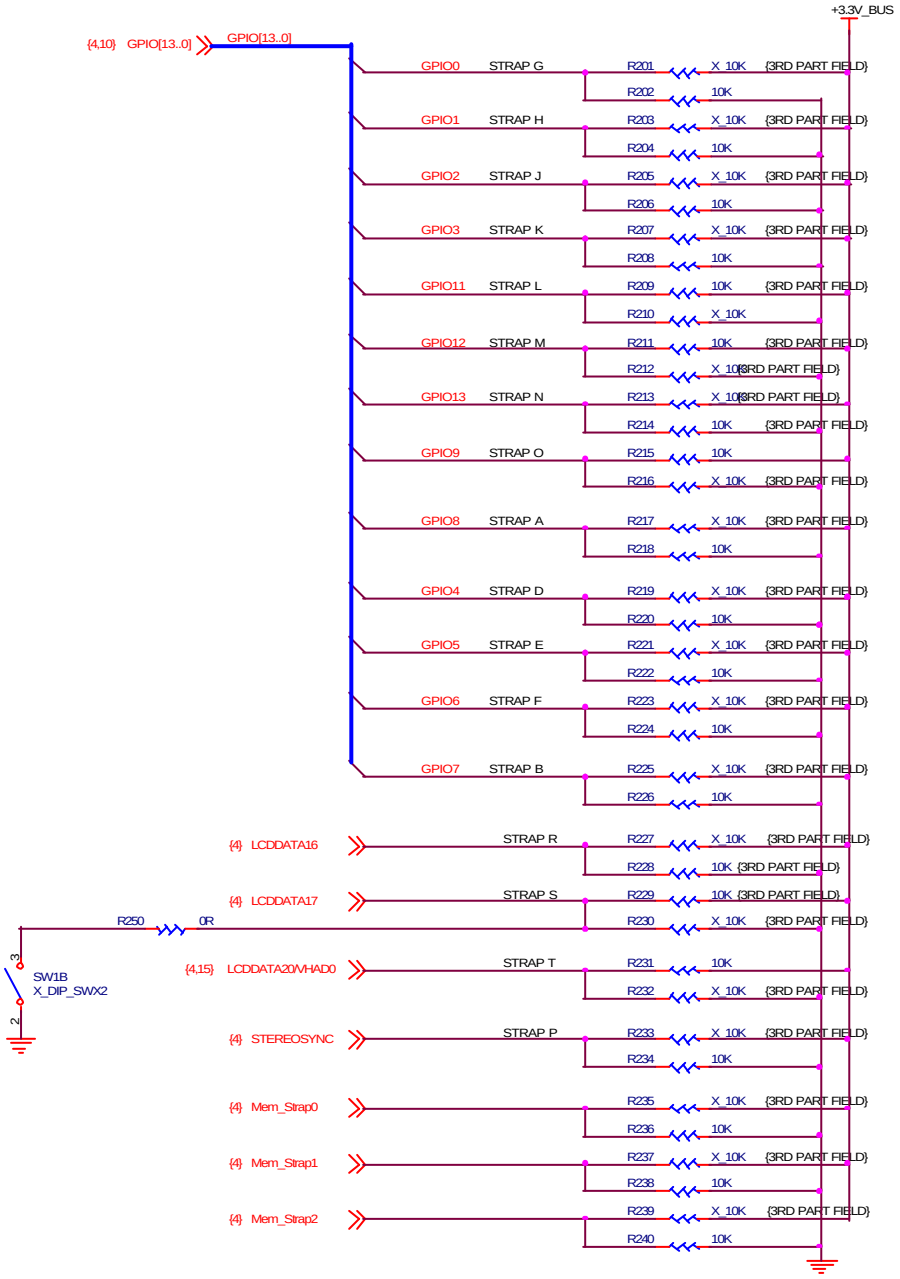
TPVDD = TPVDD + LPVDD + TXVDDR

Some Part Ref's updated to 988 brd

MICRO-STAR

Power_REG(VDDQ/etc)

MS-8913



OPTION STRAPS

STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1011
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap. **IF AGP8X_DETb=0:(both GC or MB 8x capable)** **000-AGP8x,0.8v singaling,PLL clk,IDSEL=AD16** **001-AGP8x,0.8v singaling,PLL clk,IDSEL=AD17** **010-AGP4x,0.8v singaling,PLL clk,IDSEL=AD16** **011-AGP4x,0.8v singaling,PLL clk,IDSEL=AD17**	000 (internal pull-down)
VGA_DISABLE	GPIO(7)	**0 - VGA controller capabillity enabled.** 1 - The device will not be recognized as the systemis VGA controller.	0
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select 00 - single function device. 01 - two function device. No AGP in either function **10 - two function device. AGP only in function 0** 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	10
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. **0 - Slave VIP host port devices present** 1 - No slave VIP host port devices reporting presence during reset	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

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Title: Option Straps

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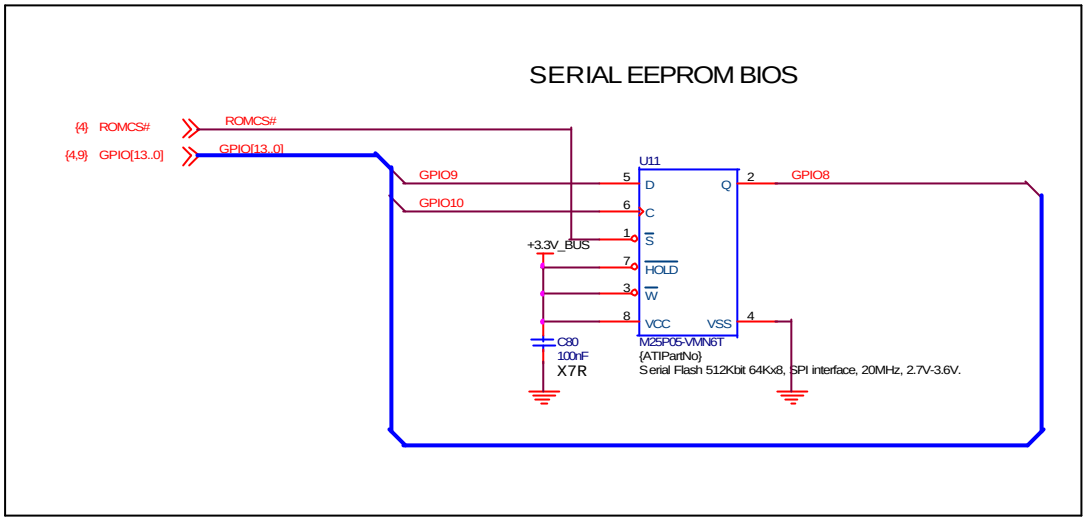
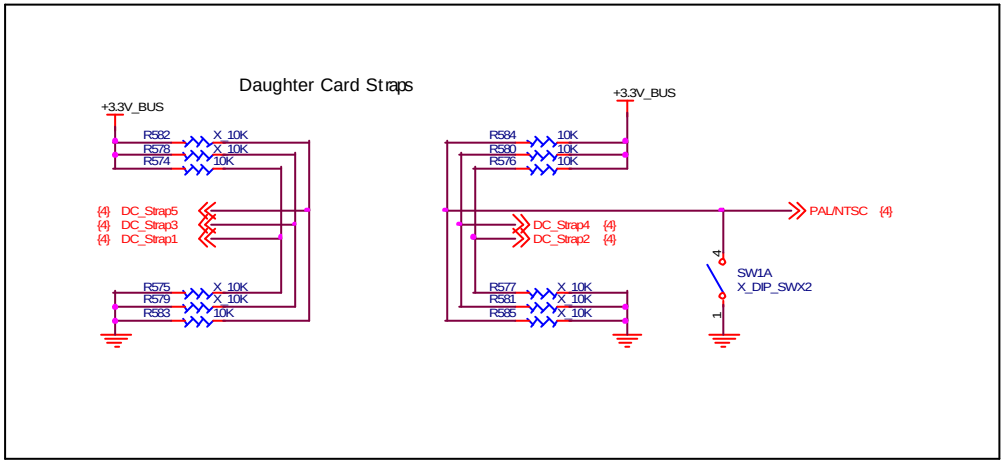




DC_STRAPS

STRAPS	PIN	DESCRIPTION
DC_STRAP1	LCDDATA12	INTERNAL TMDS ENABLE 0--DISABLE 1--ENABLE
DC_STRAP2	LCDDATA13	VIDEO CAPTURE ENABLE 0--DISABLE 1--ENABLE
DC_STRAP4 DC_STRAP5	LCDDATA15 LCDDATA19 0 0 0 1 1 0 1 1	DAC2 CONFIGURATION DAC2 OFF DAC2 ON AS CRT DAC2 ON AS TVOUT DAC2 ON AS TVOUT AND CRT
PAL/NTSC	LCDDATA18	TVOUT STANDARD DEFAULT 0--PAL 1--NTSC

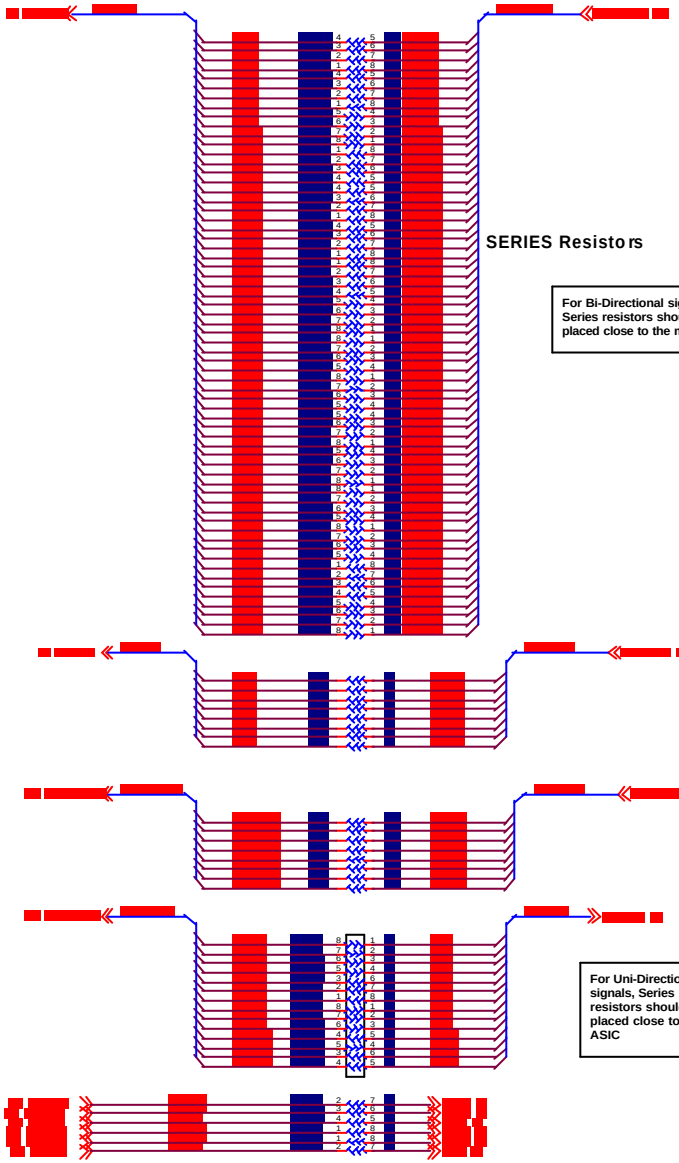
MICRO-STAR

Title: Serial BIOS & HW Straps

Size | Document Number: MS-8913 | Rev: 0A

Date: Monday, February 10, 2003 | Sheet 10 of 16

TERMINATION FOR MEMORY CHANNEL A



SERIES Resistors

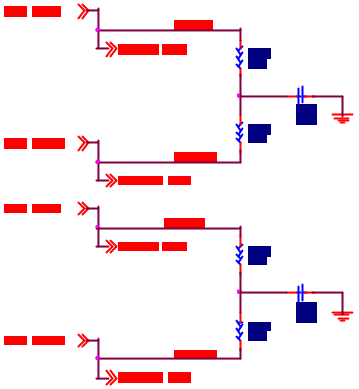
For Bi-Directional signals, Series resistors should be placed close to the memory

For Uni-Directional signals, Series resistors should be placed close to the ASIC

Proper Termination of QSA?

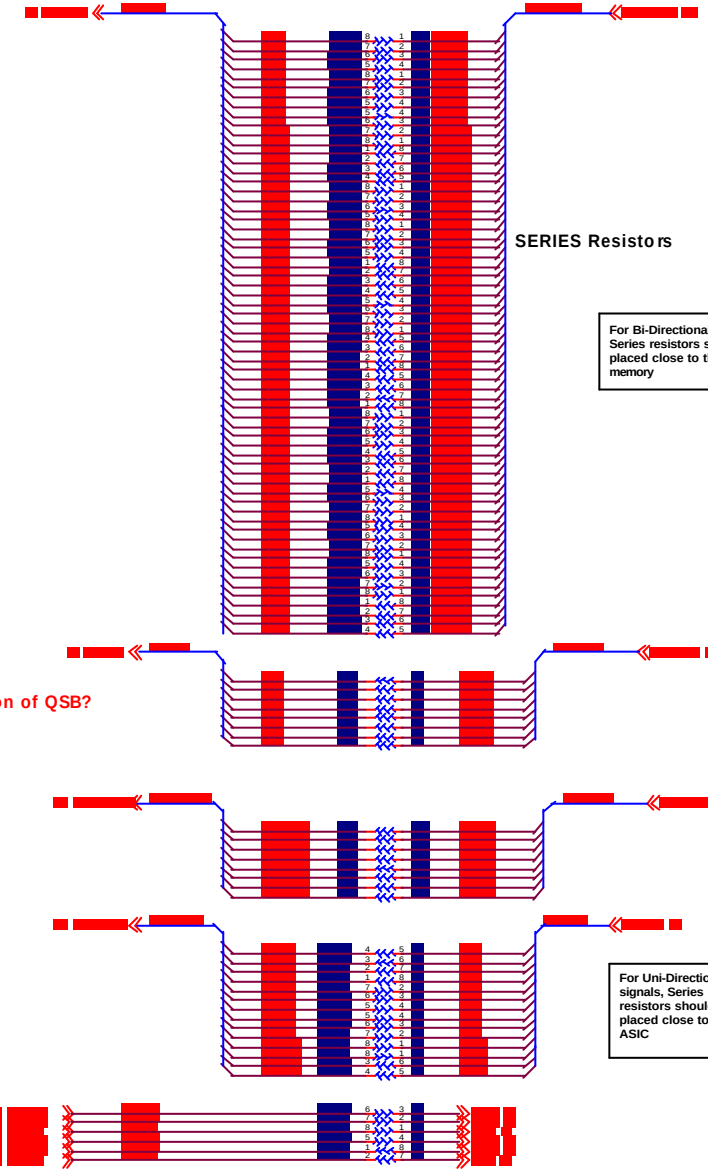
CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair



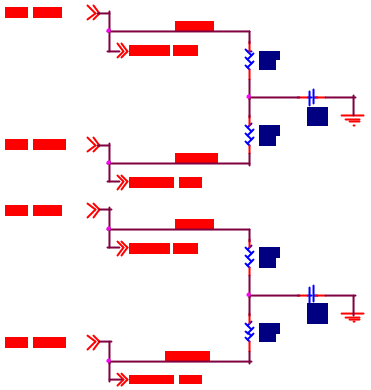
MICRO-STAR	
Serial Termination CH A	
MS-8913	

TERMINATION FOR MEMORY CHANNEL B



CLOCK terminations

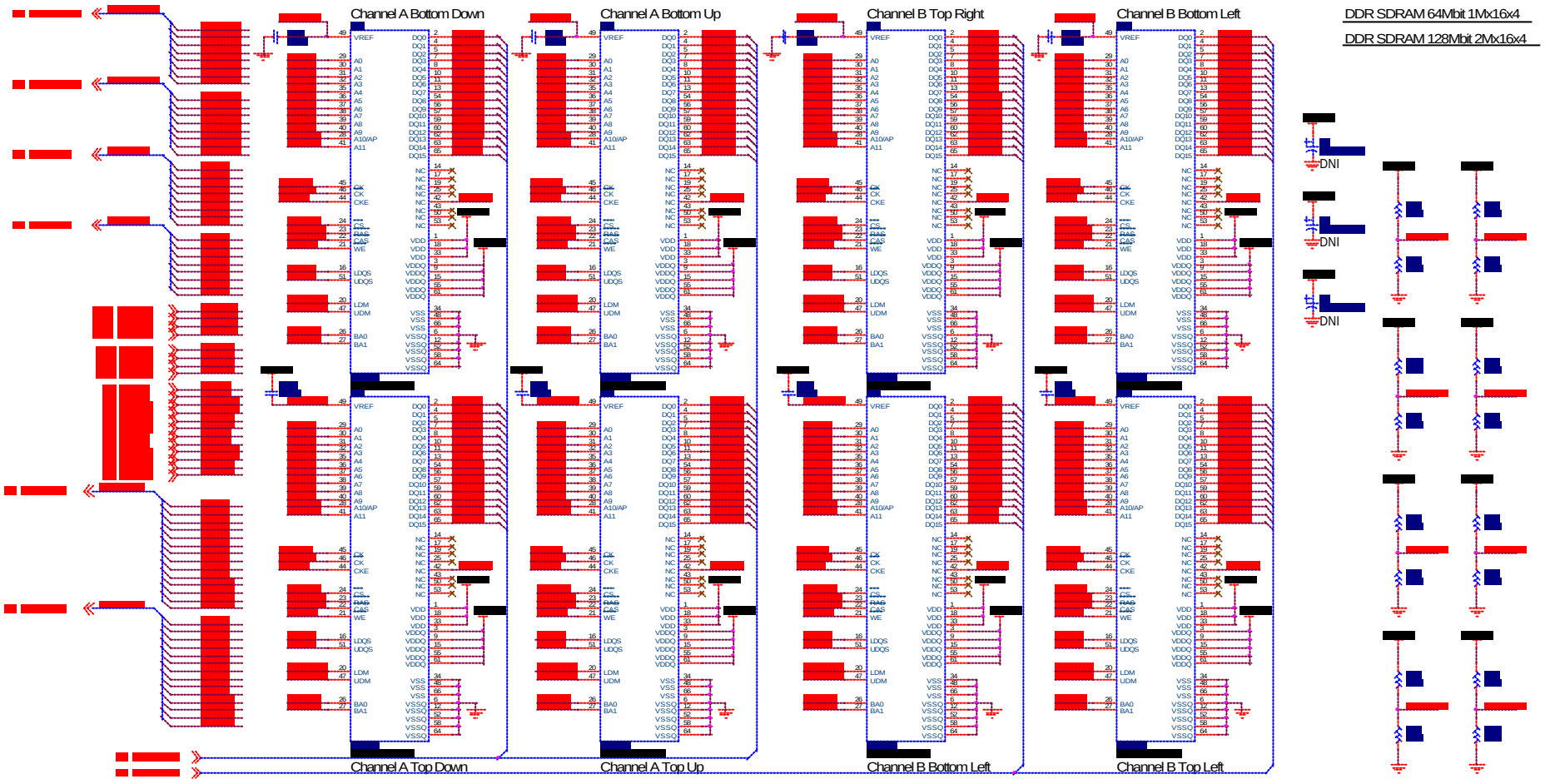
Change from 1:1 spacing to at least a 2.5:1 spacing between the pair



MICRO-STAR

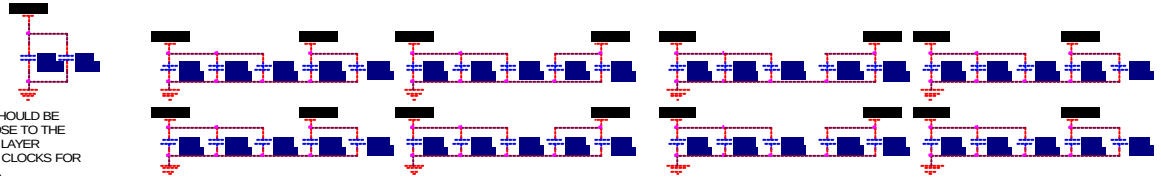
Serial Termination CH B

MS-8913



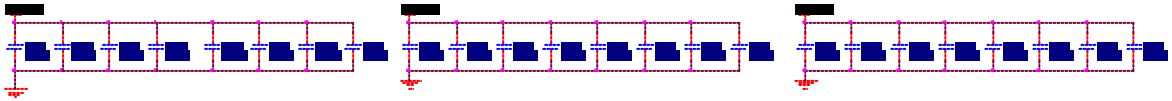
Note: These indications of the location of the memory for the solder side (bottom) are looking thru from the component side.

Put 1 1uF cap per power pin of memory



2 capacitors SHOULD BE PLACED CLOSE TO THE REFERENCE LAYER CHANGE OF CLOCKS FOR EMI REDUCE.

Place as many as possible.



Part number for 8Mx16: 2354274204 (Samsung)

DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

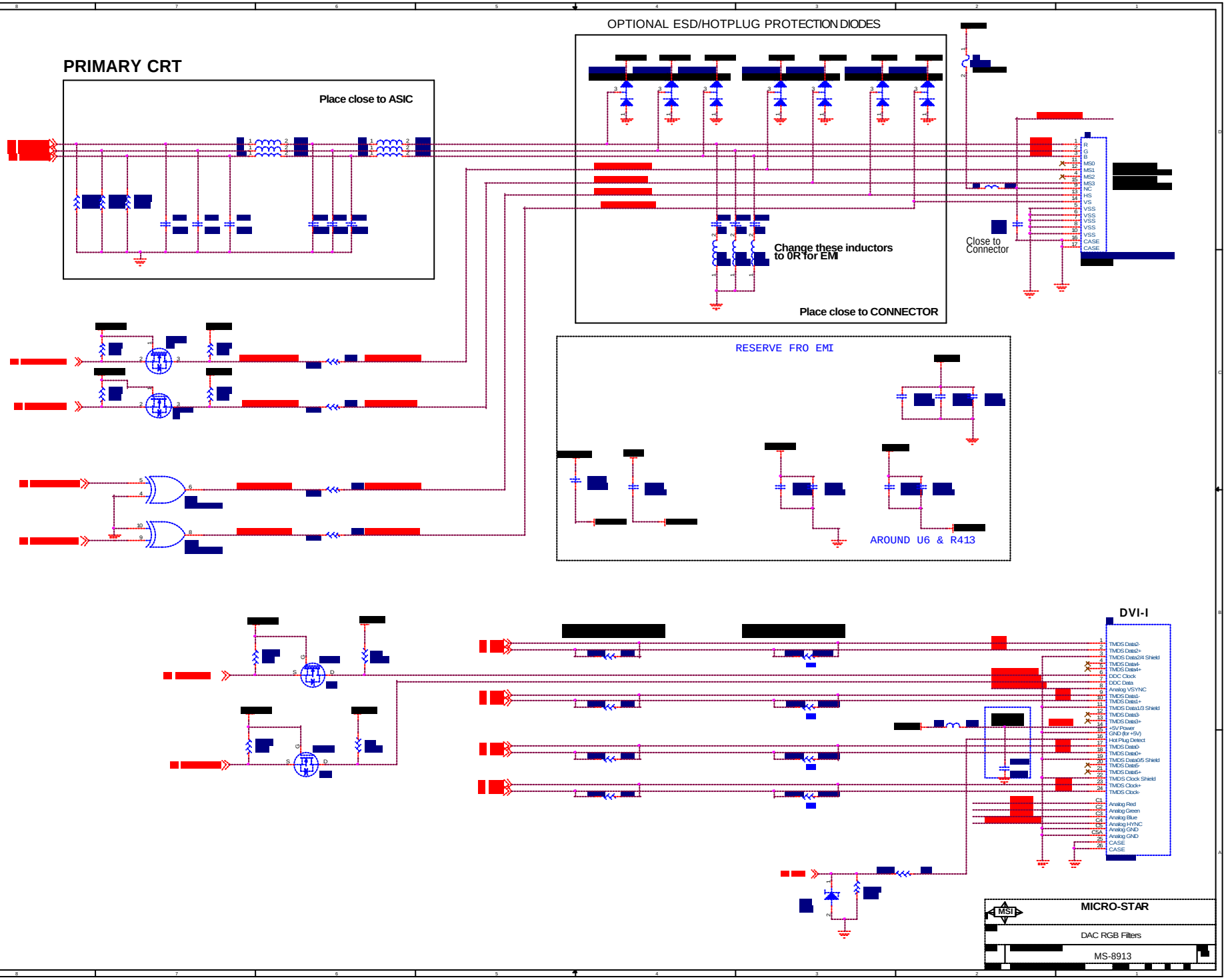
All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

Some Part Ref's updated to 988 brd

MICRO-STAR

TSOP 4/8Mx16 DDR

MS-8913

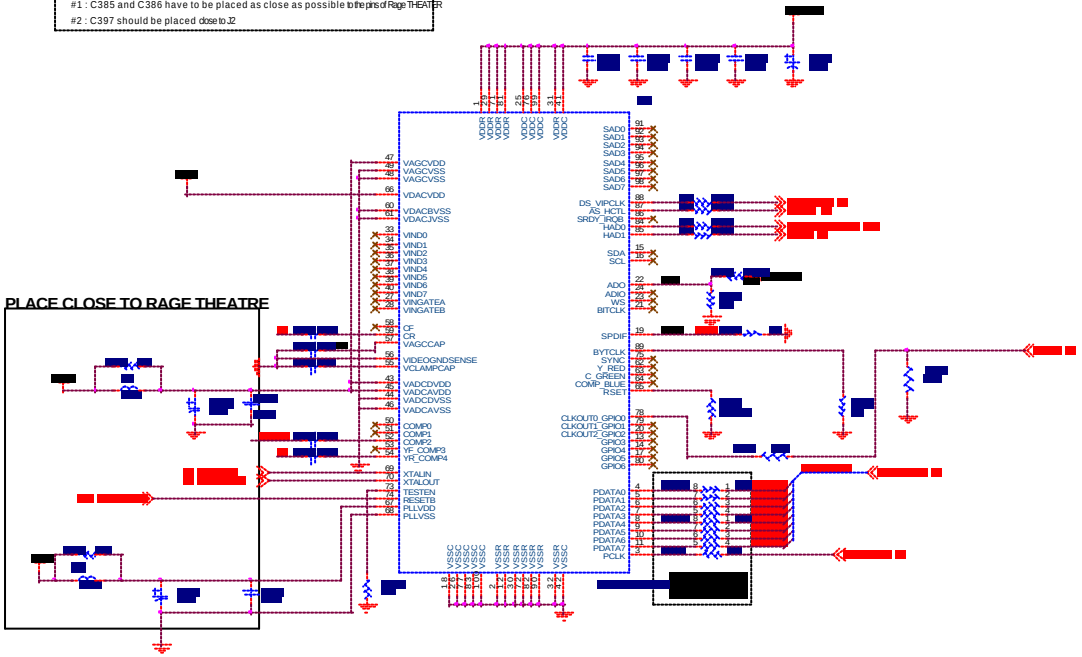

PRIMARY CRT
Place close to ASIC
OPTIONAL ESD/HOTPLUG PROTECTION DIODES
Change these inductors to 0R for EMI
Place close to CONNECTOR
Close to Connector
R
G
B
MS0
MS1
MS2
MS3
NC
HS
VS
VSS
VSS
VSS
VSS
CASE
CASE
RESERVE FRO EMI
AROUND U6 & R413
DVI-I
TMDS Data2-
TMDS Data2+
TMDS Data2/4 Shield
TMDS Data4-
TMDS Data4+
DDC Clock
DDC Data
Analog VSYNC
TMDS Data1-
TMDS Data1+
TMDS Data1/3 Shield
TMDS Data3-
TMDS Data3+
+5V Power
GND (for +5V)
Hot Plug Detect
TMDS Data0-
TMDS Data0+
TMDS Data0/5 Shield
TMDS Data5-
TMDS Data5+
TMDS Clock Shield
TMDS Clock+
TMDS Clock-
Analog Red
Analog Green
Analog Blue
Analog HYNC
Analog GND
Analog GND
CASE
CASE
MICRO-STAR
DAC RGB Filters
MS-8913

Layout Guide line of TH EATER

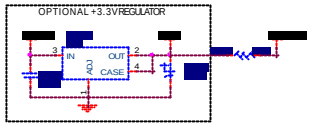
#1 : C385 and C386 have to be placed as close as possible to the pins of Rage THEATER

#2 : C397 should be placed close to J2

PLACE CLOSE TO RAGE THEATRE



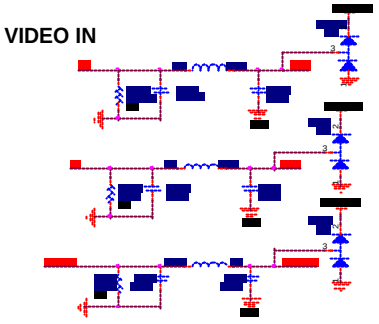
OPTIONAL +3.3VREGULATOR

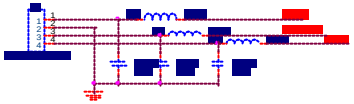


REGULATOR FOR RVDD

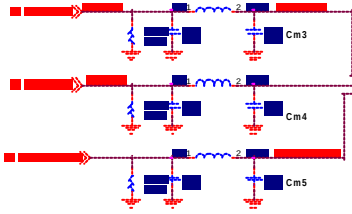
PLACE CLOSE TO RAGE THEATRE

VIDEO IN



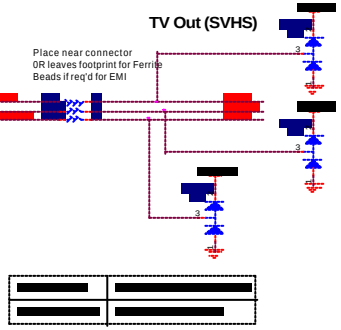


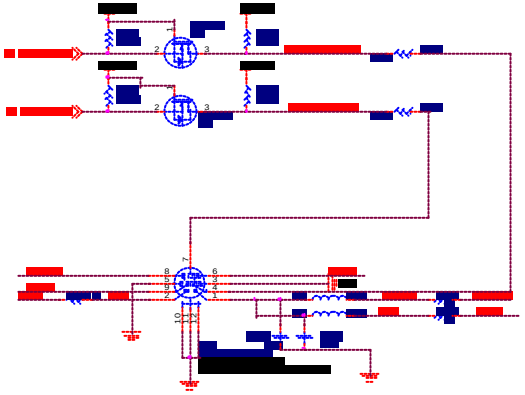
Place Resistors close to ASIC.



TV Out (SVHS)

Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI





MICRO-STAR

VIVO

MS-8913

CRT SCREWS

SCREW1

SCREW
JACKSCREW
{3rd part field}
{ATIPartNo}

SCREW2

SCREW
JACKSCREW
{3rd part field}
{ATIPartNo}

FM4
X_FIDUCIAL

FM8
X_FIDUCIAL

FM3
X_FIDUCIAL

FM7
X_FIDUCIAL

FM2
X_FIDUCIAL

FM6
X_FIDUCIAL

FM1
X_FIDUCIAL

FM5
X_FIDUCIAL

+MVDDQ

TEST

TEST2

BRACKET

BRACKET

{3RD PART FIELD}

BRACKET

PCB

PCB

{ATIPartNo}
{3rd part field}

Heatsink

PASSIVE HEATSINK

H103

Hc

HEATSINK
{3RD PART FIELD}
{ATIPartNo}

Heatsink cross-hatched finned 45X45X10mm black amodize w/o adhesive

MICRO-STAR

Title: Heatsink & Mechanicals

Size | Document Number: MS-8913 | Rev: 0A

Date: Monday, February 10, 2003 | Sheet 16 of 16