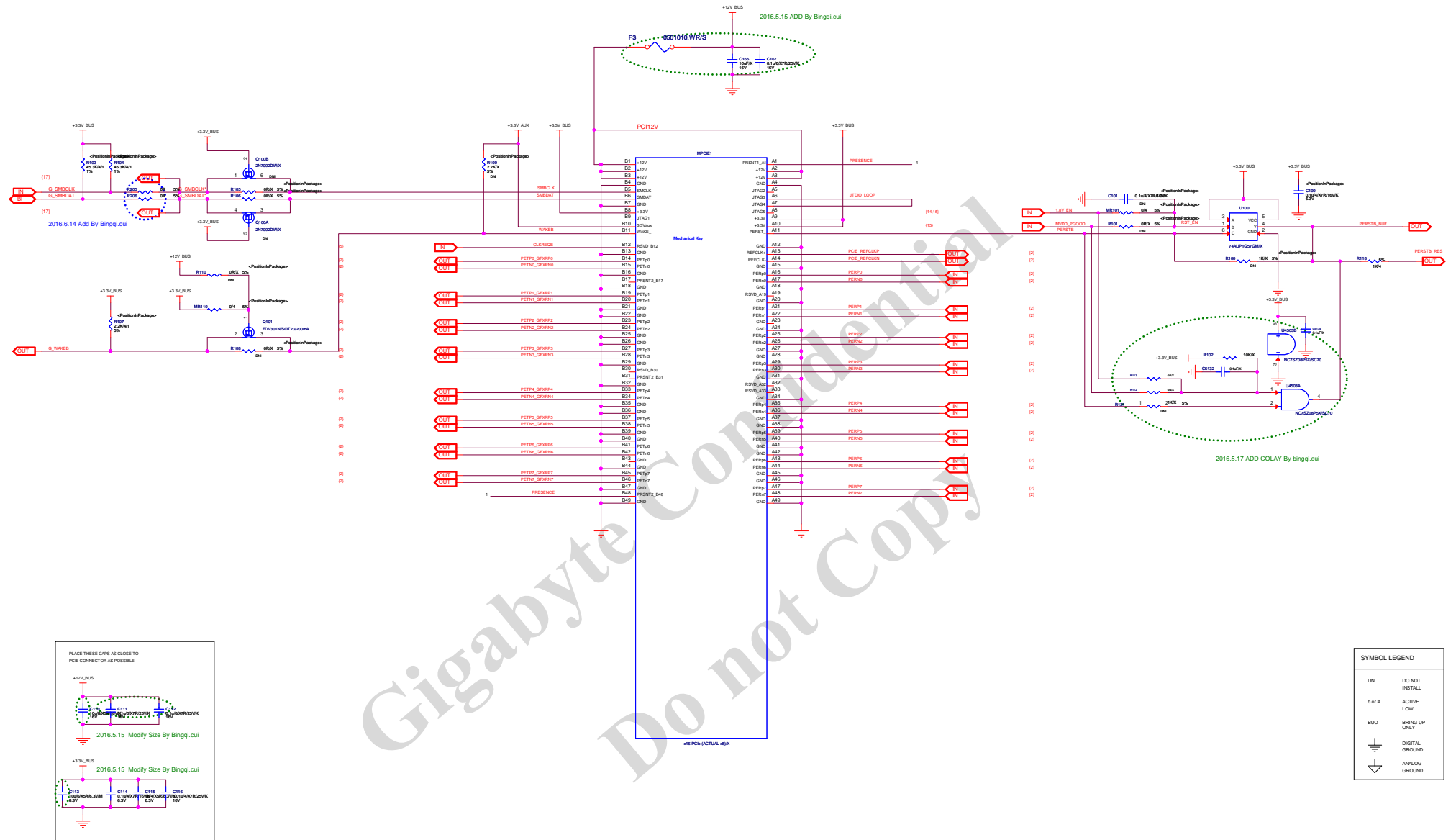
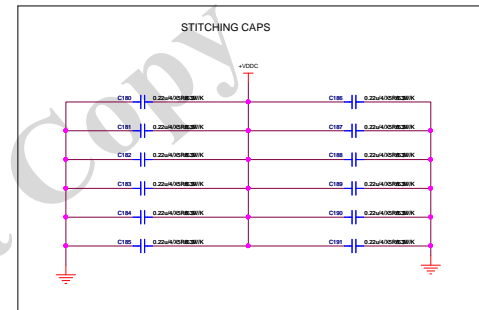


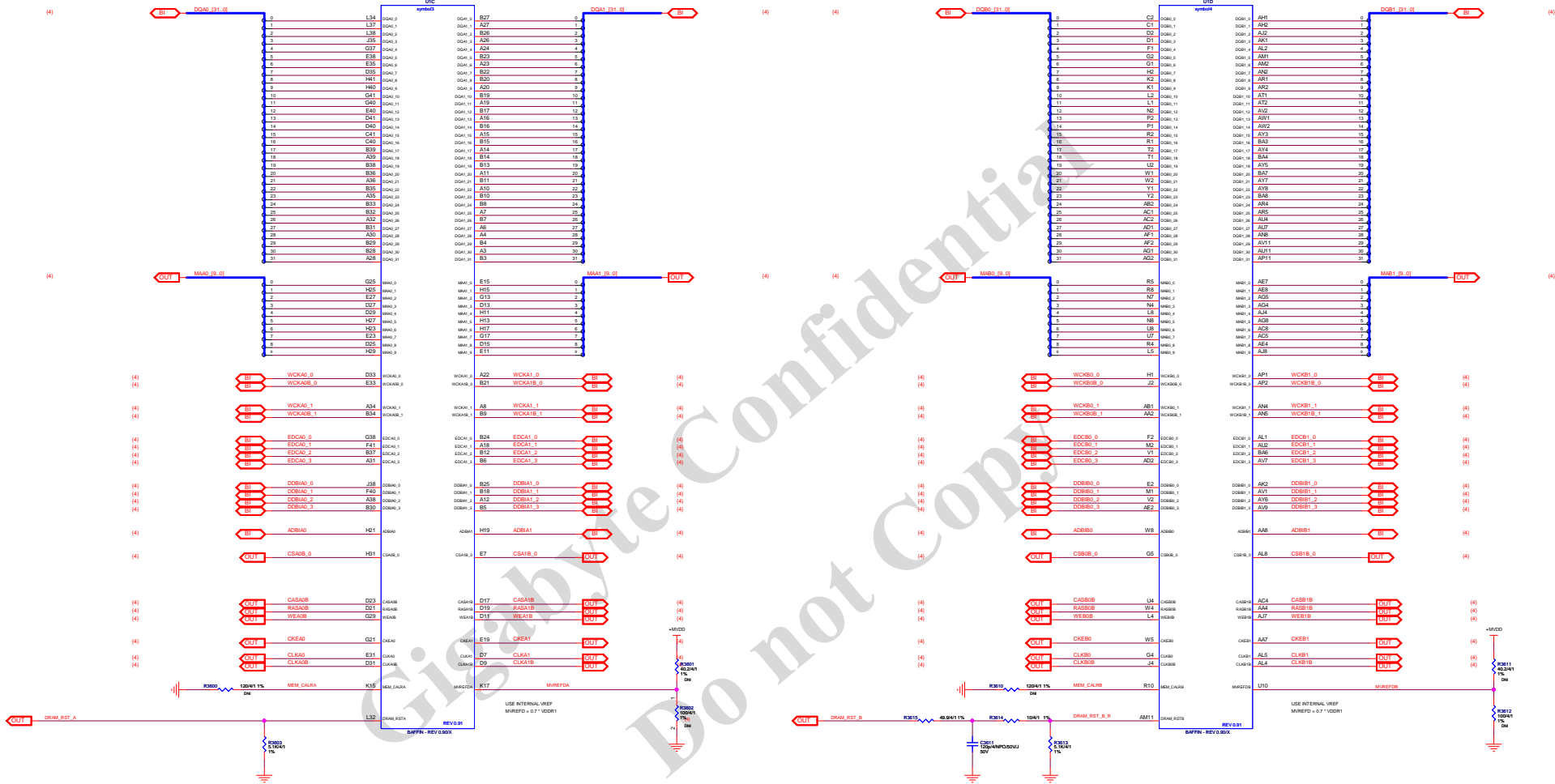
(1) PCIE EDGE CONNECTOR



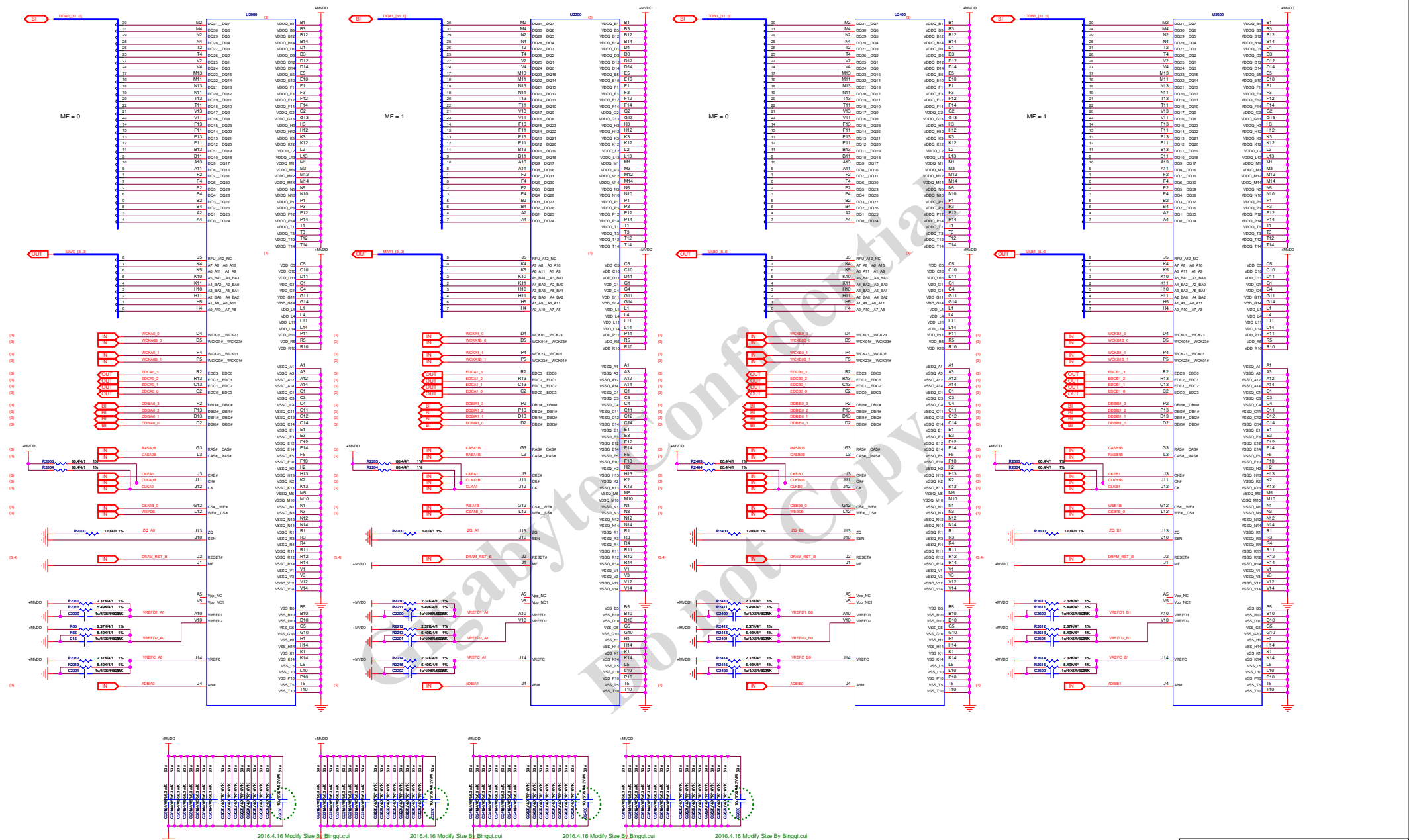
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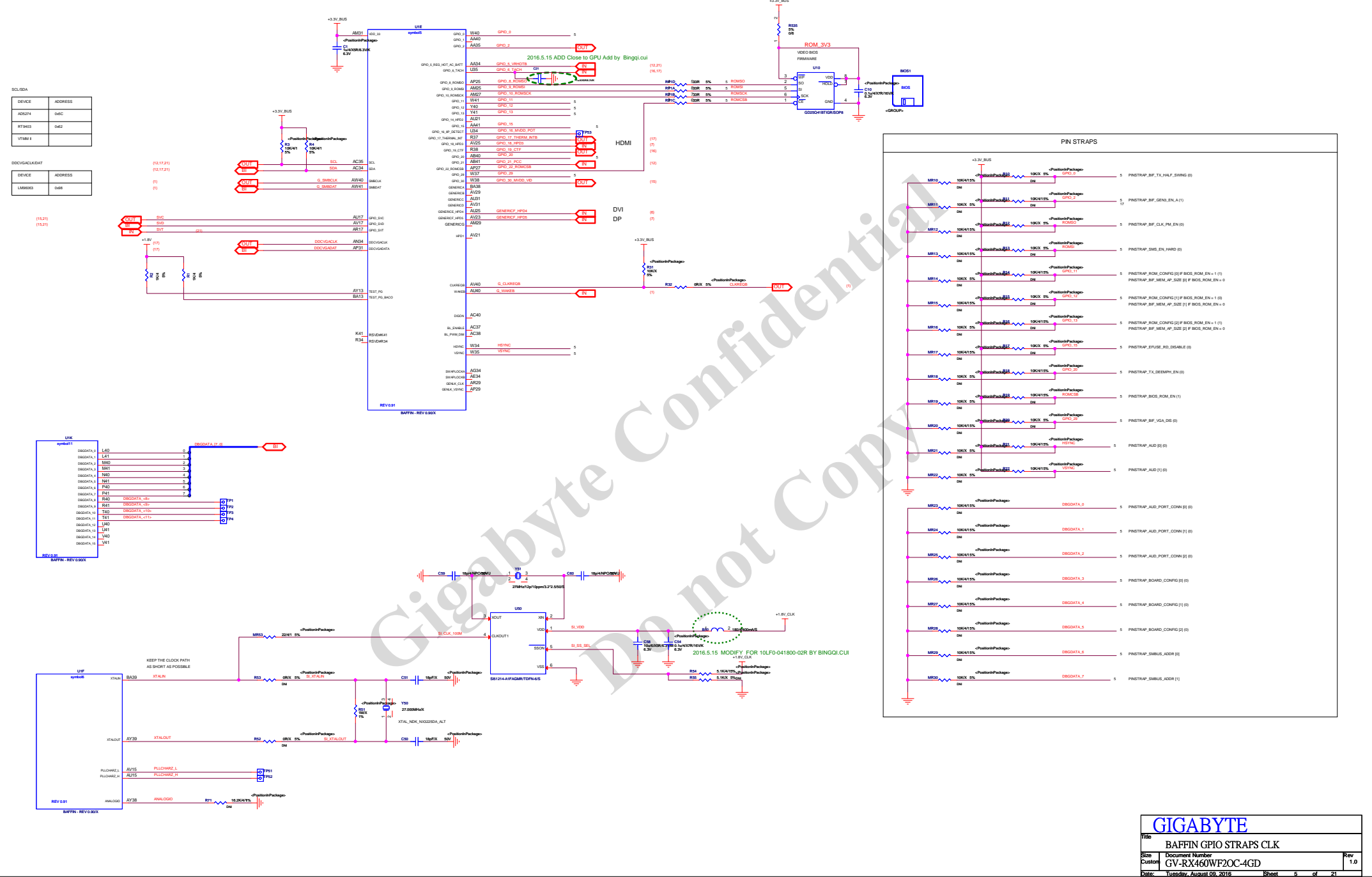
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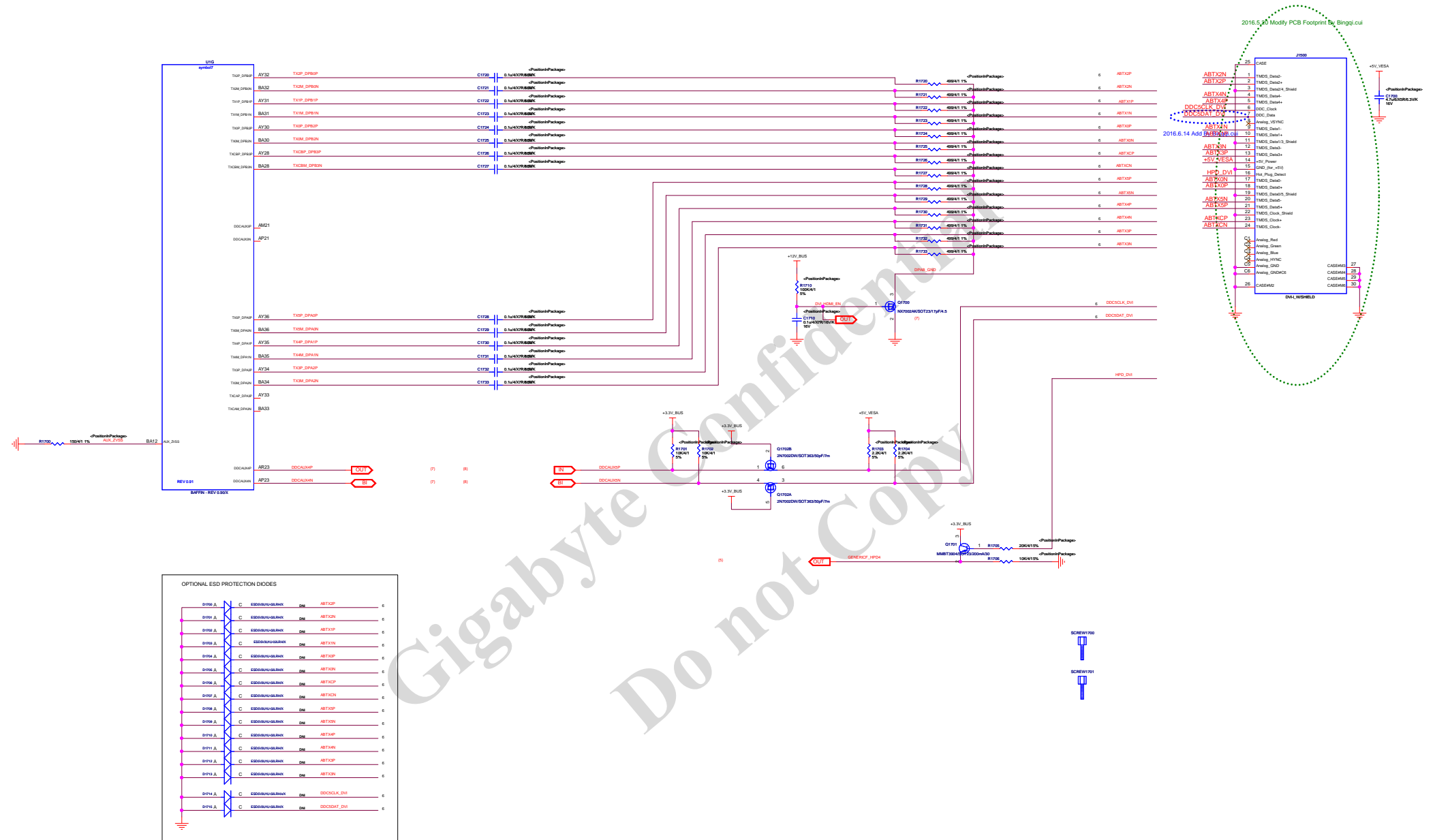


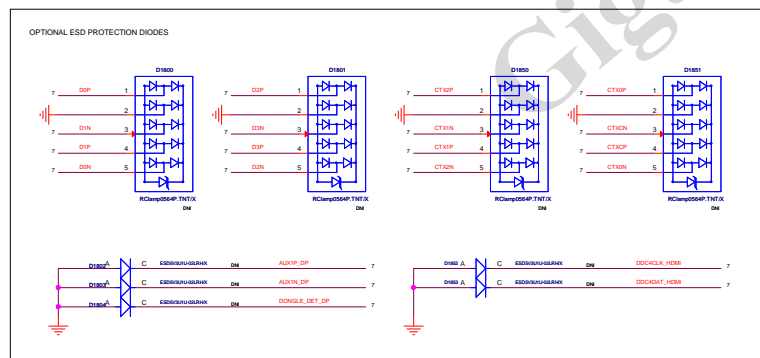
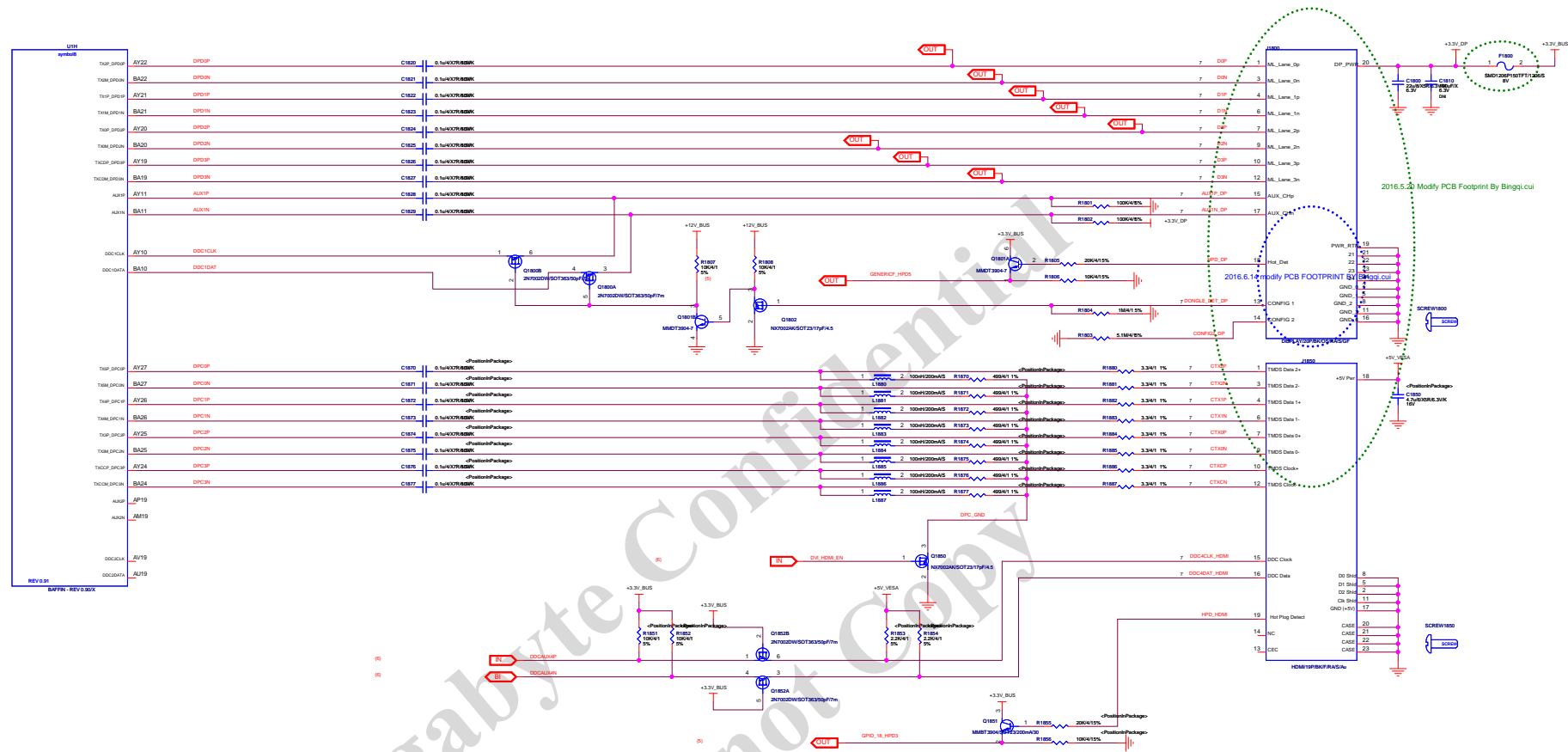
(4) GDDR5 CHAB x32

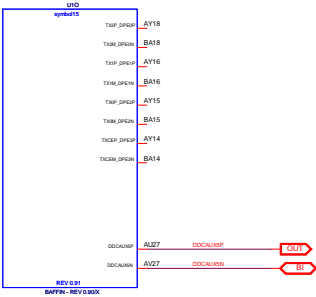


(5) BAFFIN GPIO STRAPS CLK



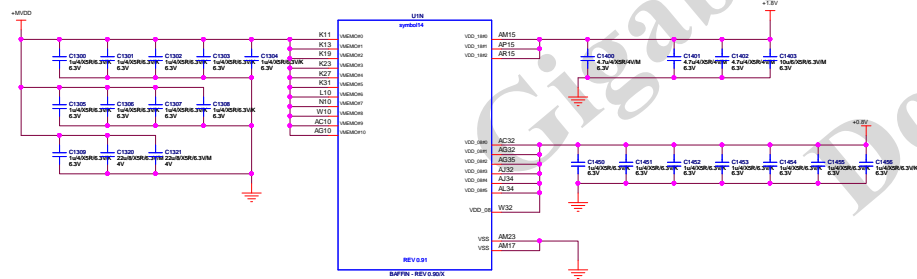
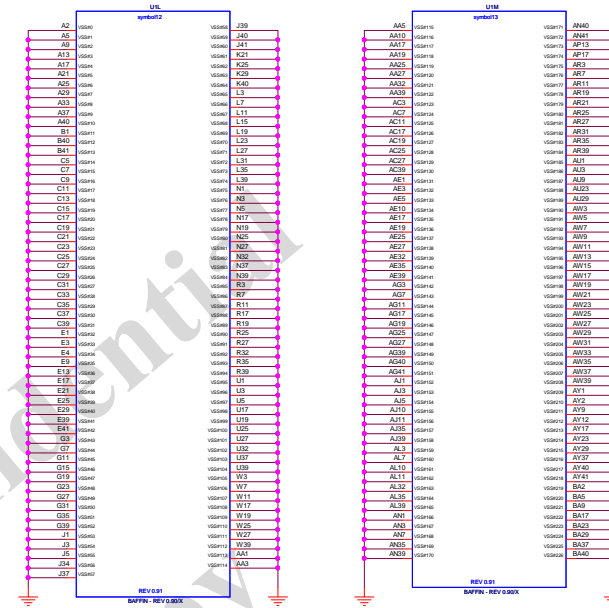
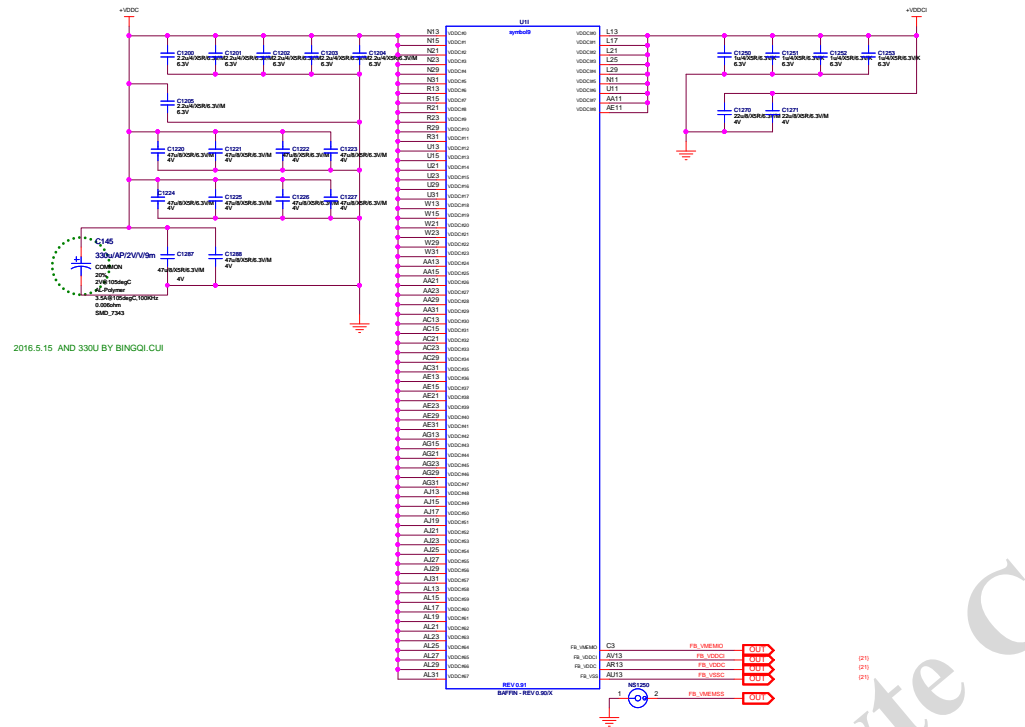




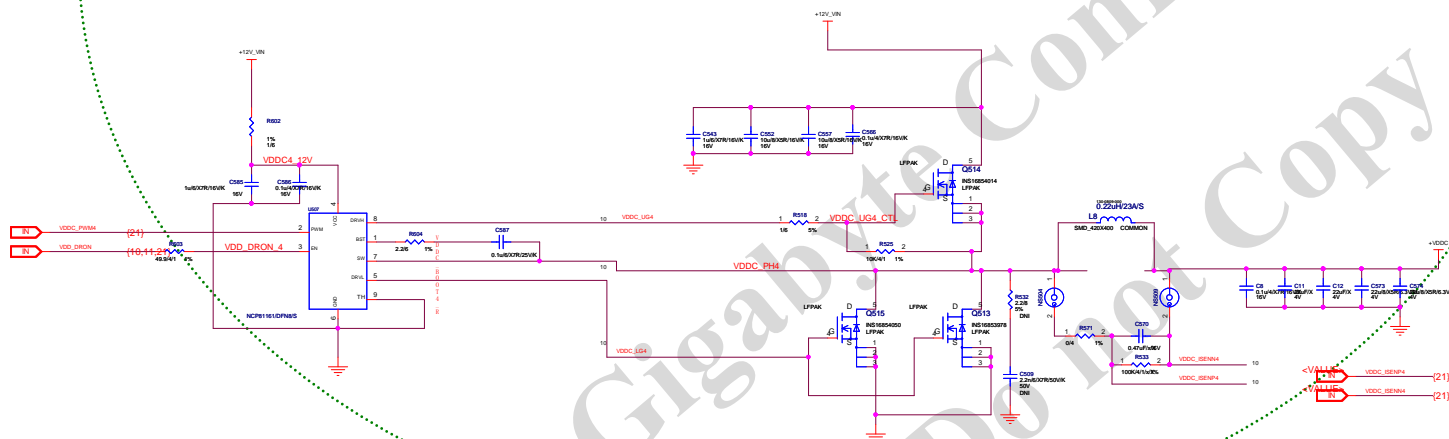
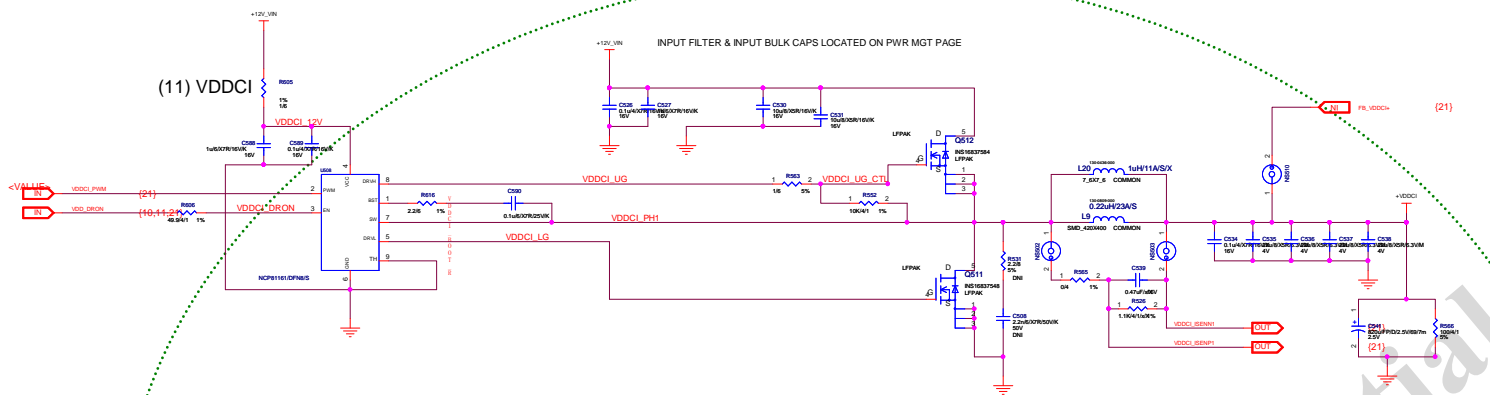


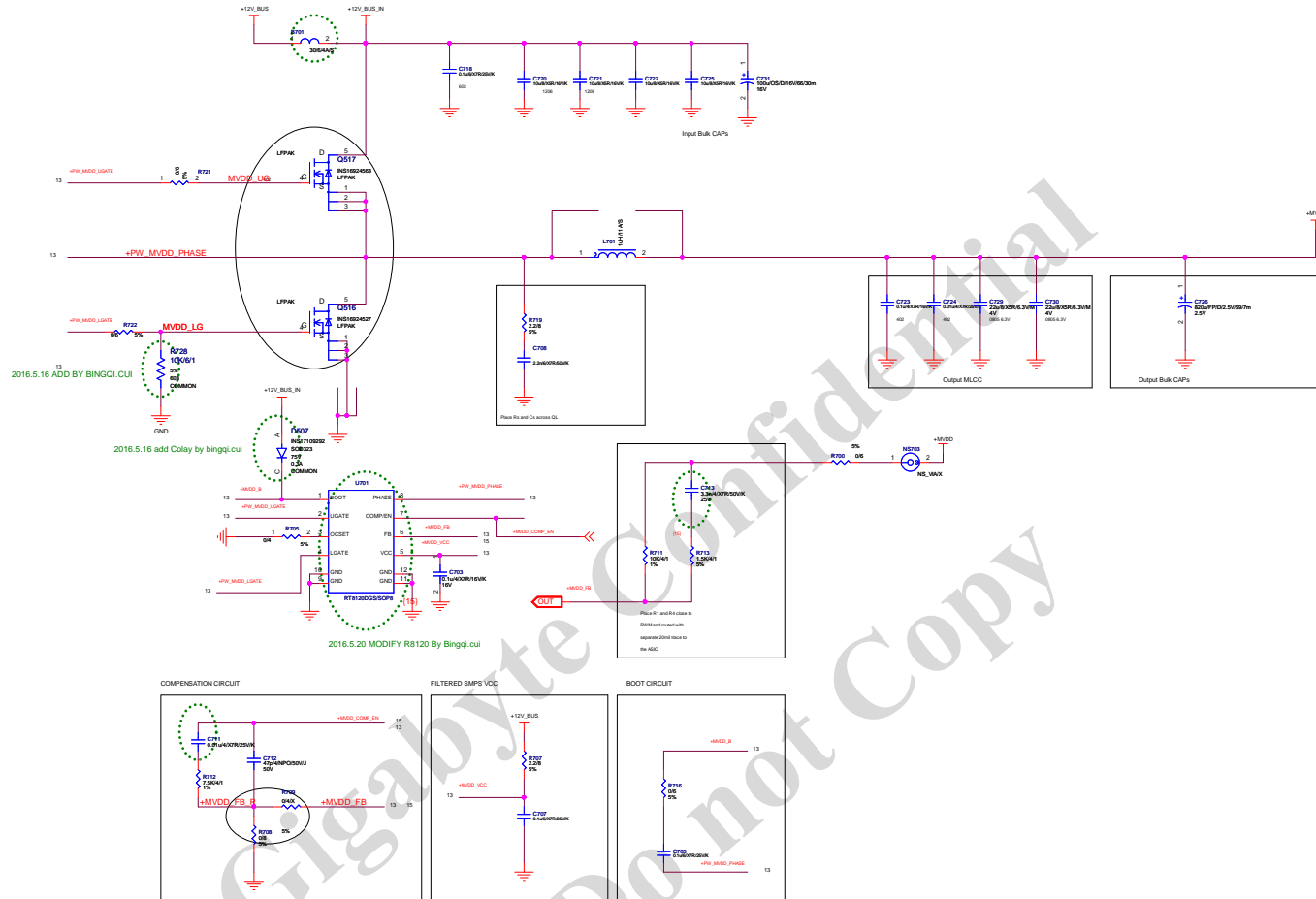
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(9) BAFFIN POWER GND

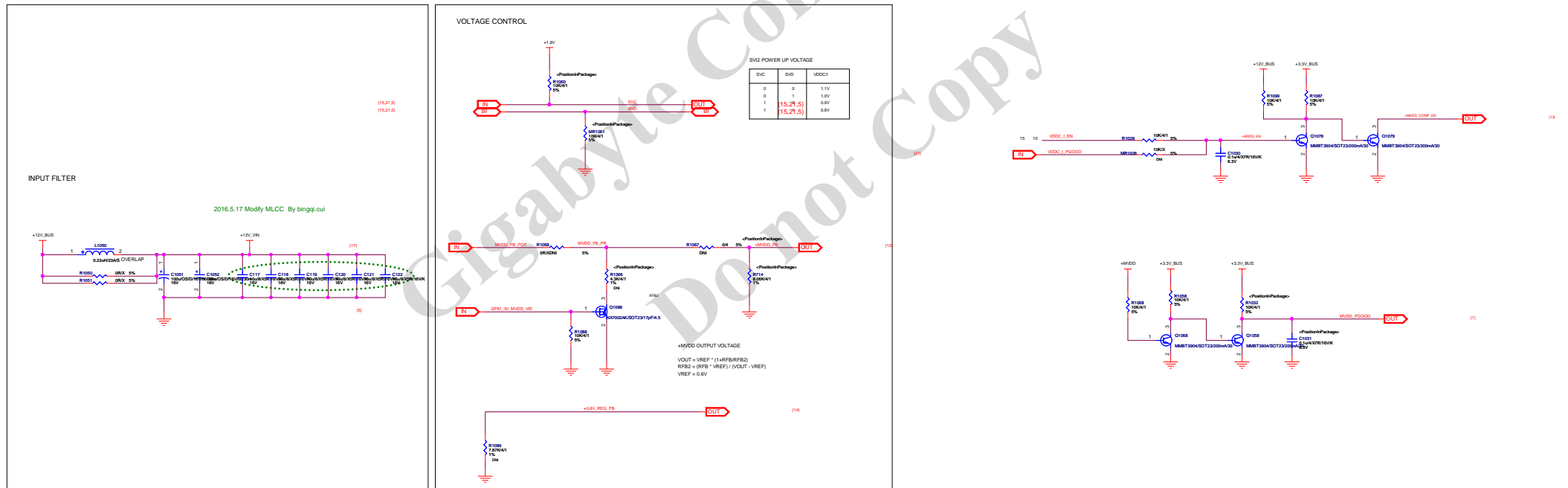
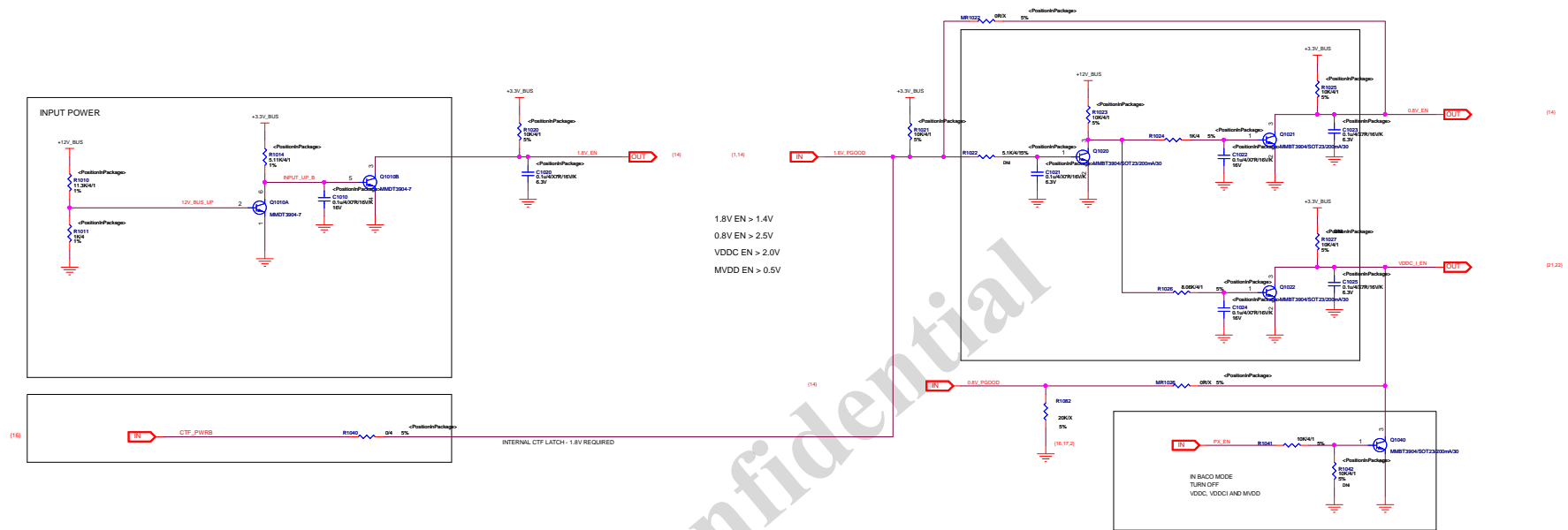




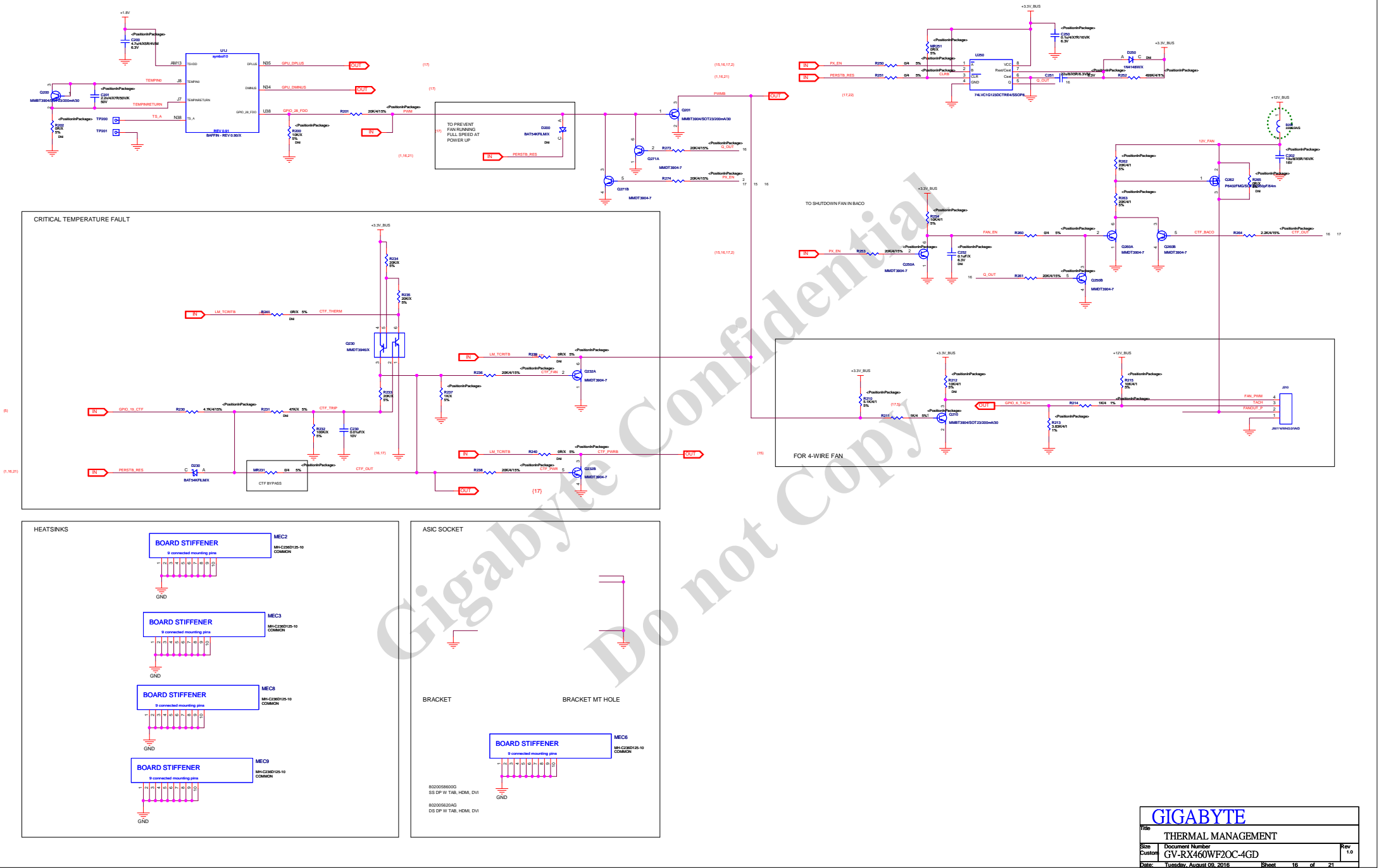




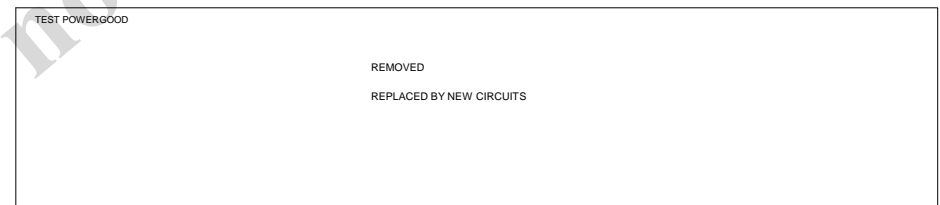
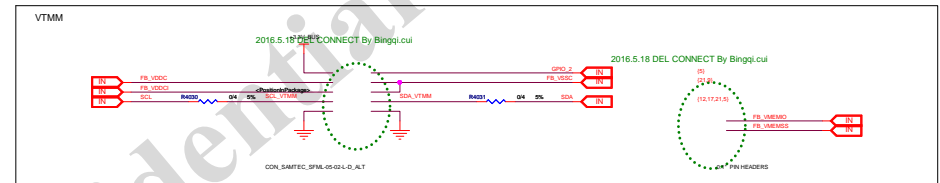
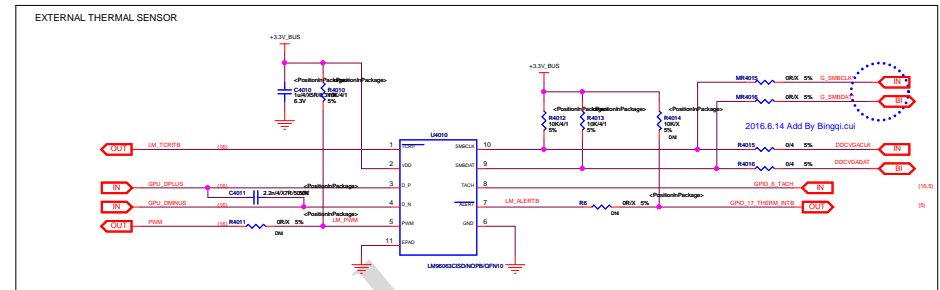
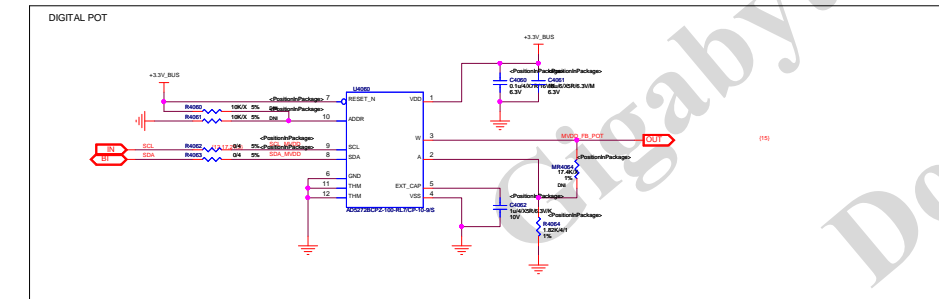
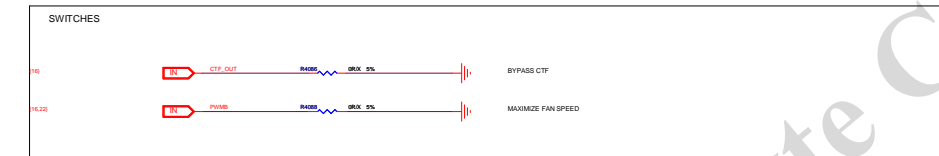
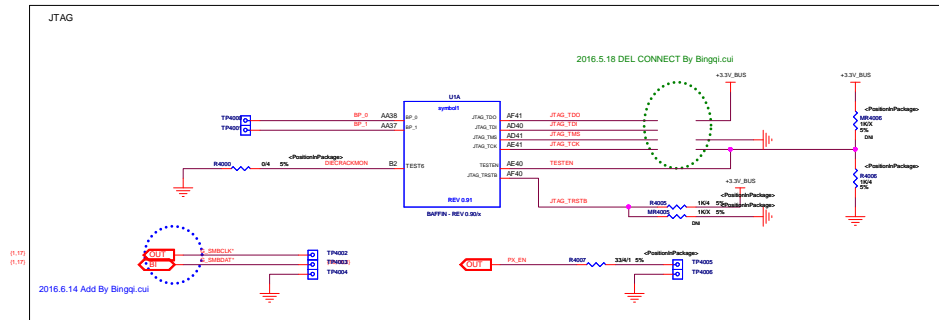
(15) POWER MANAGEMENT



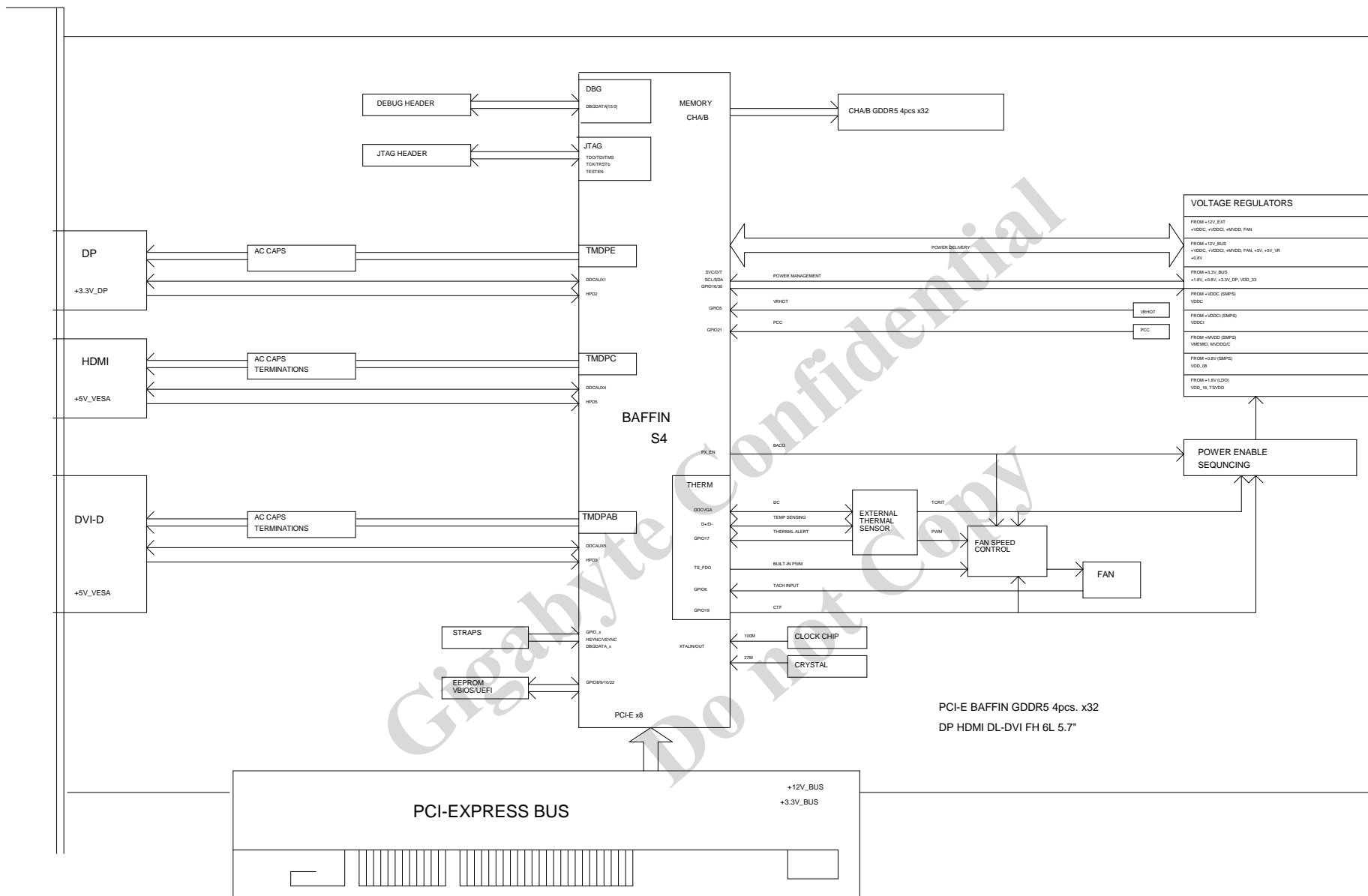
(16) THERMAL MANAGEMENT



(17) DEBUG CIRCUITS



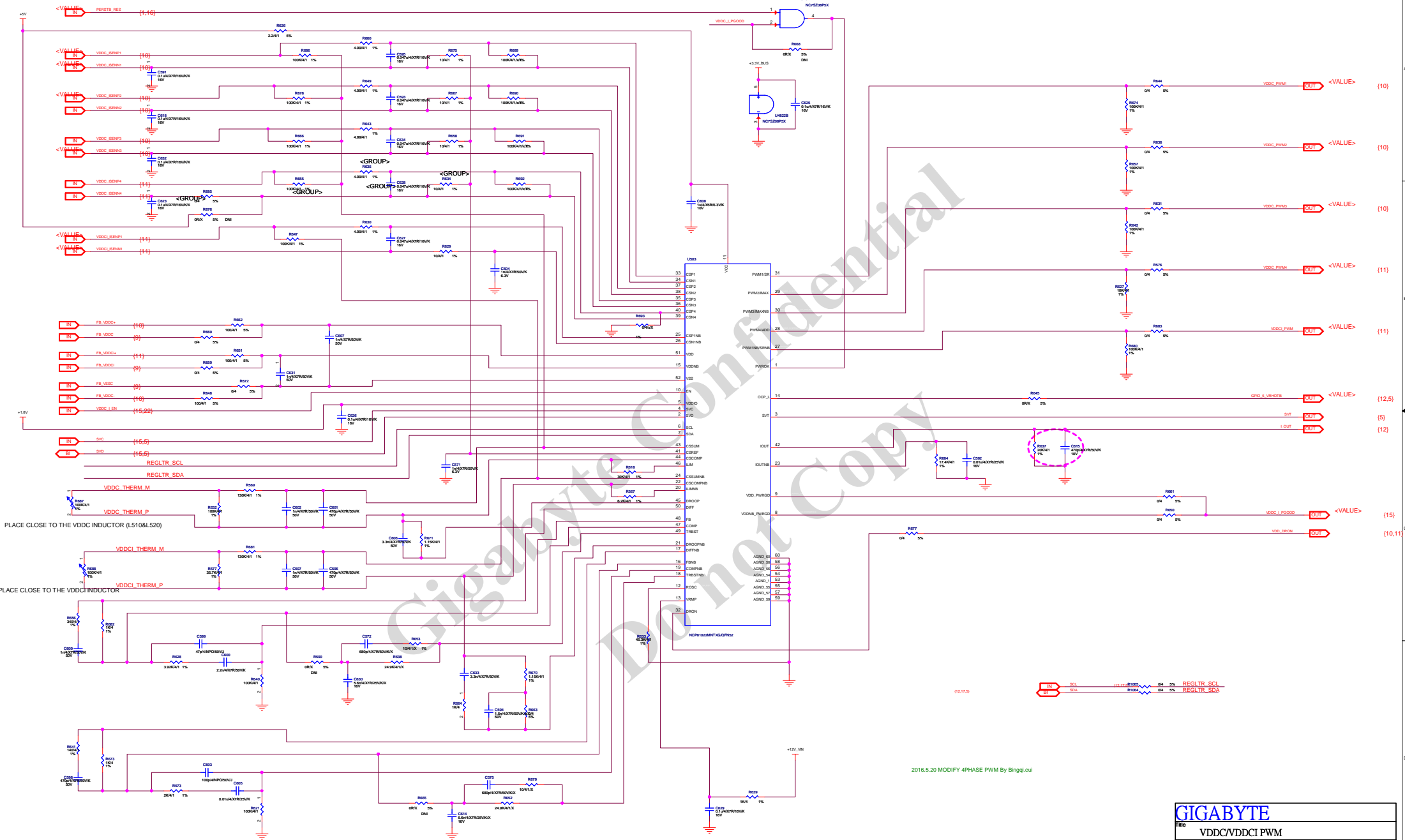
(18) BLOCK DIAGRAM



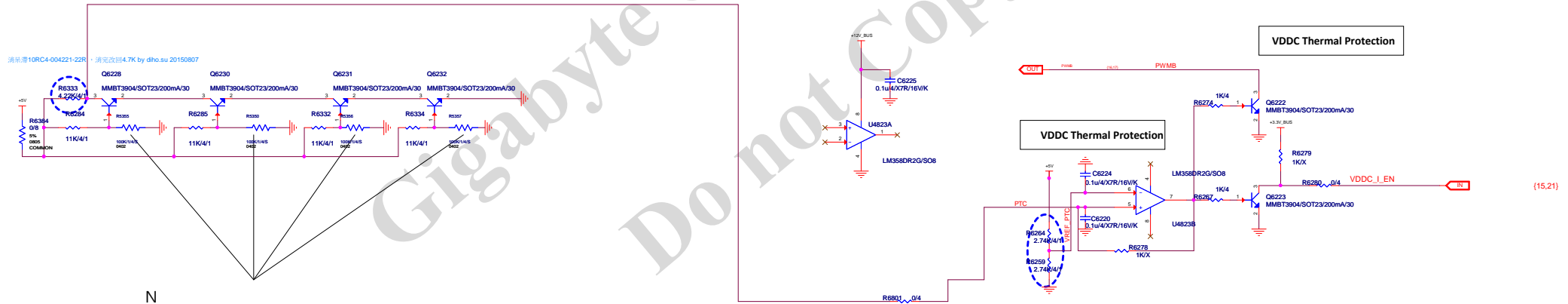
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(20) VDDC/VDDCI PWM



2016.5.15 Add MOS VRHOT CIRCUIT BY BINGQI.CUI



Near VDDC each

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