

PG611 A00	
10GB GDDR5X, 320b, 256Mx32	
DP + DP + HDMI/DP + DP	
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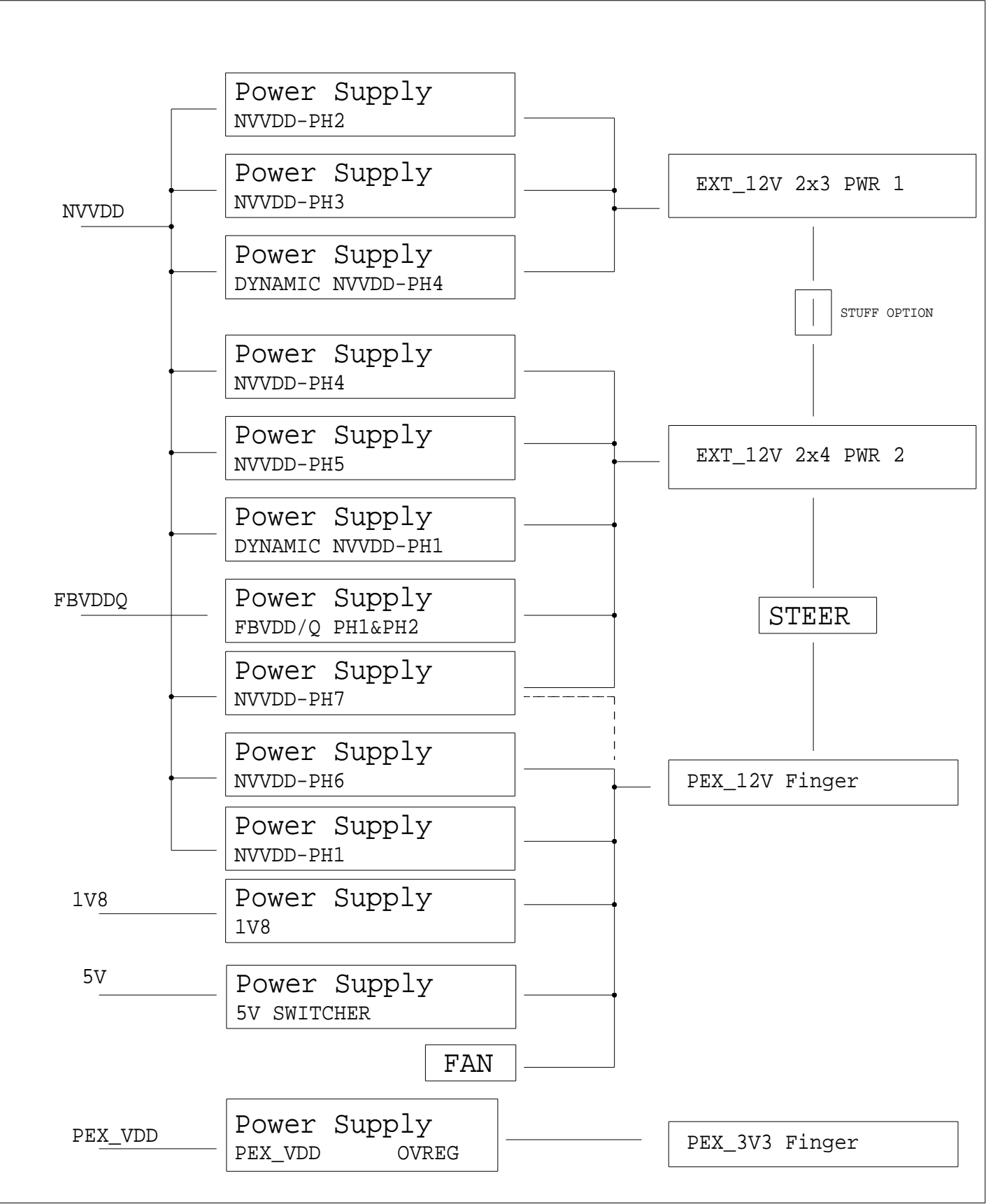
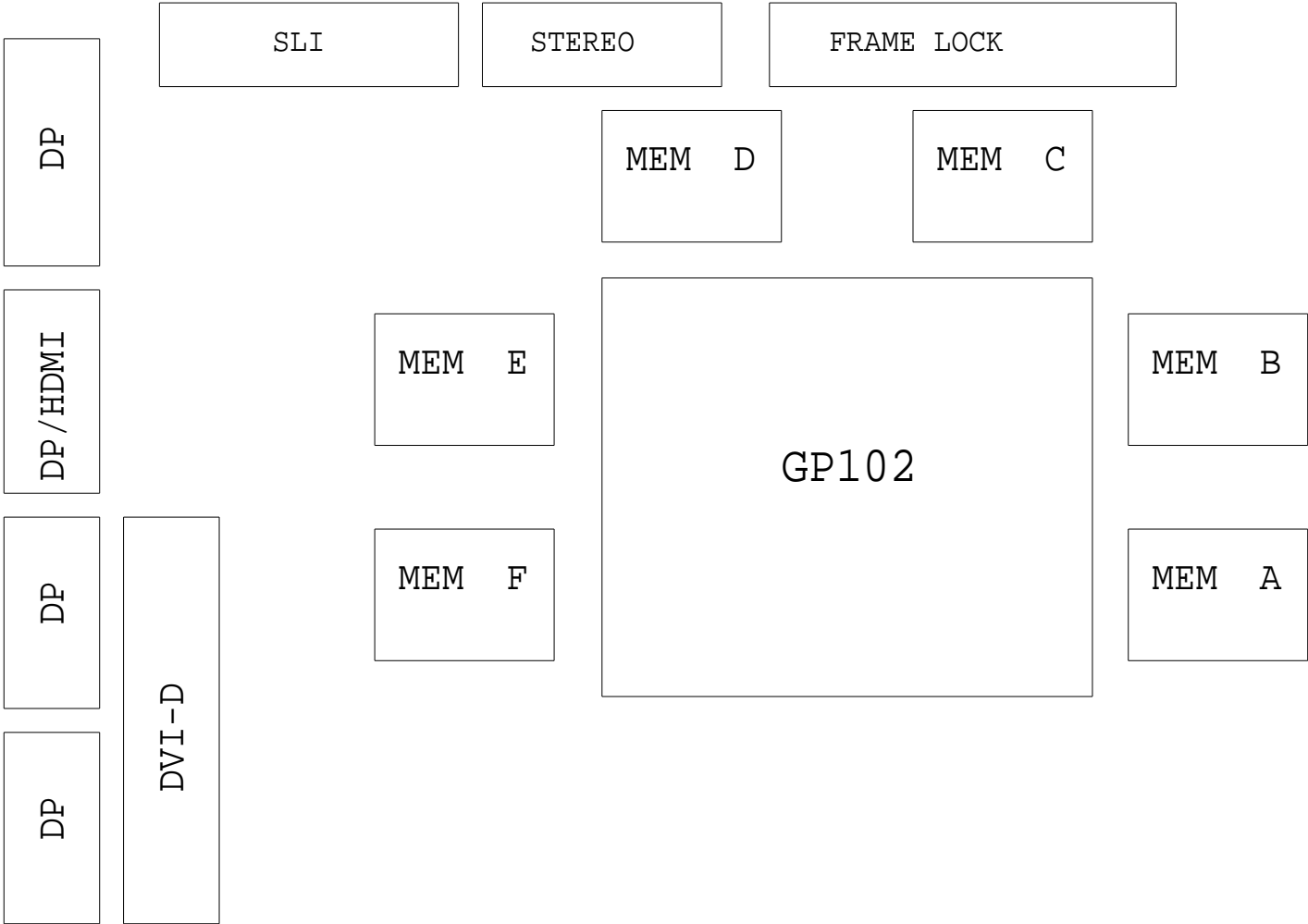
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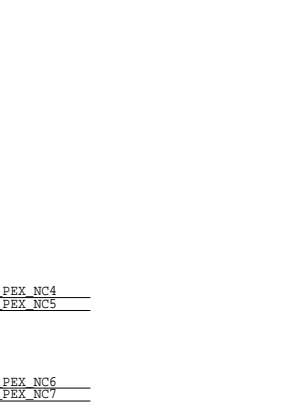
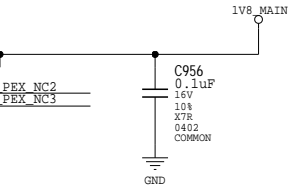
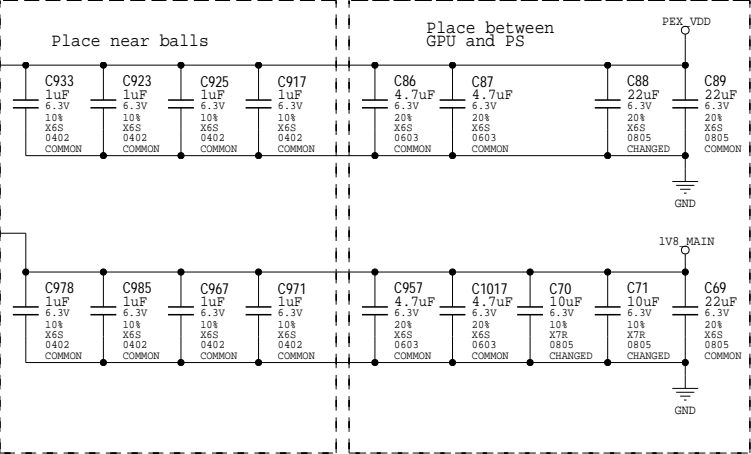
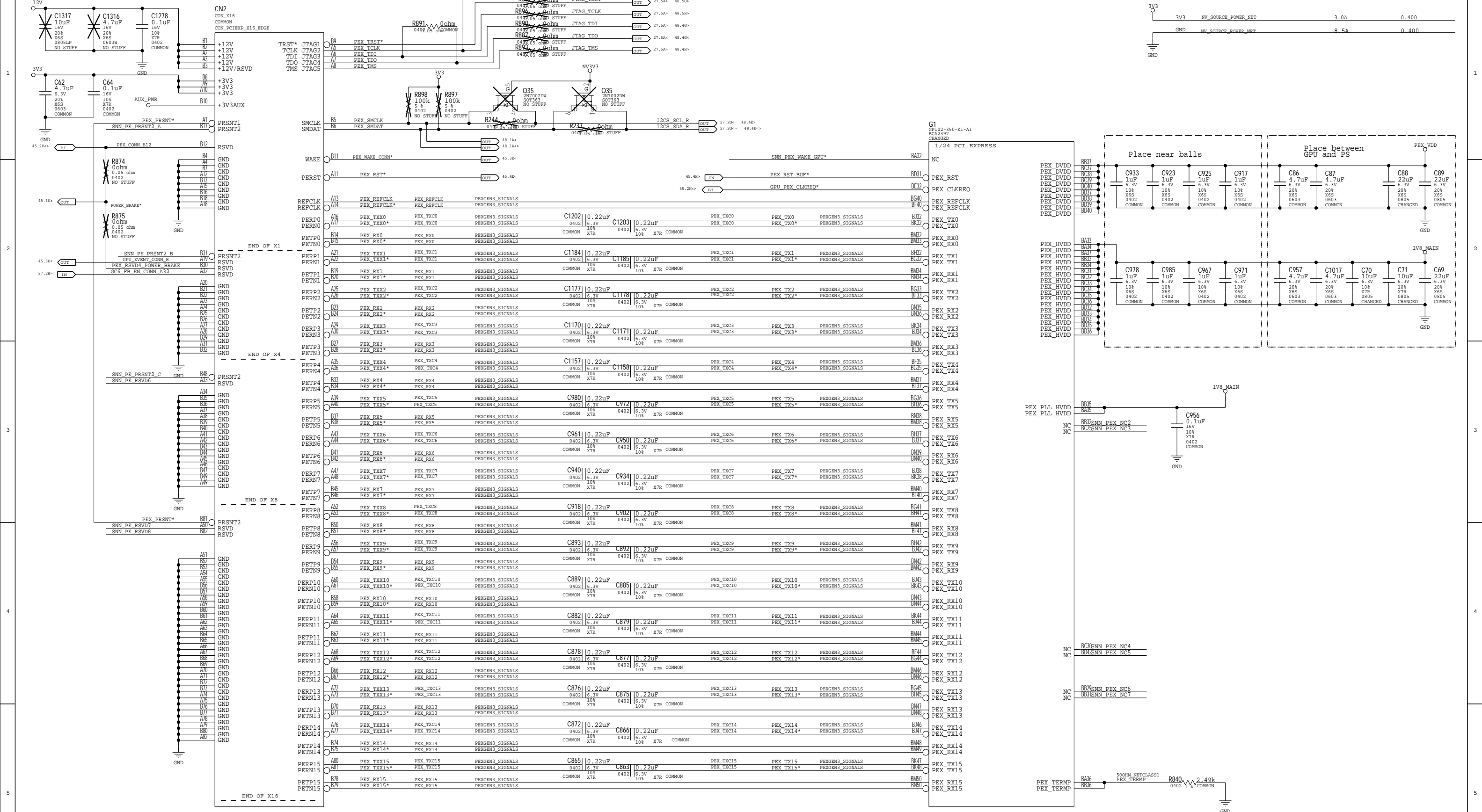
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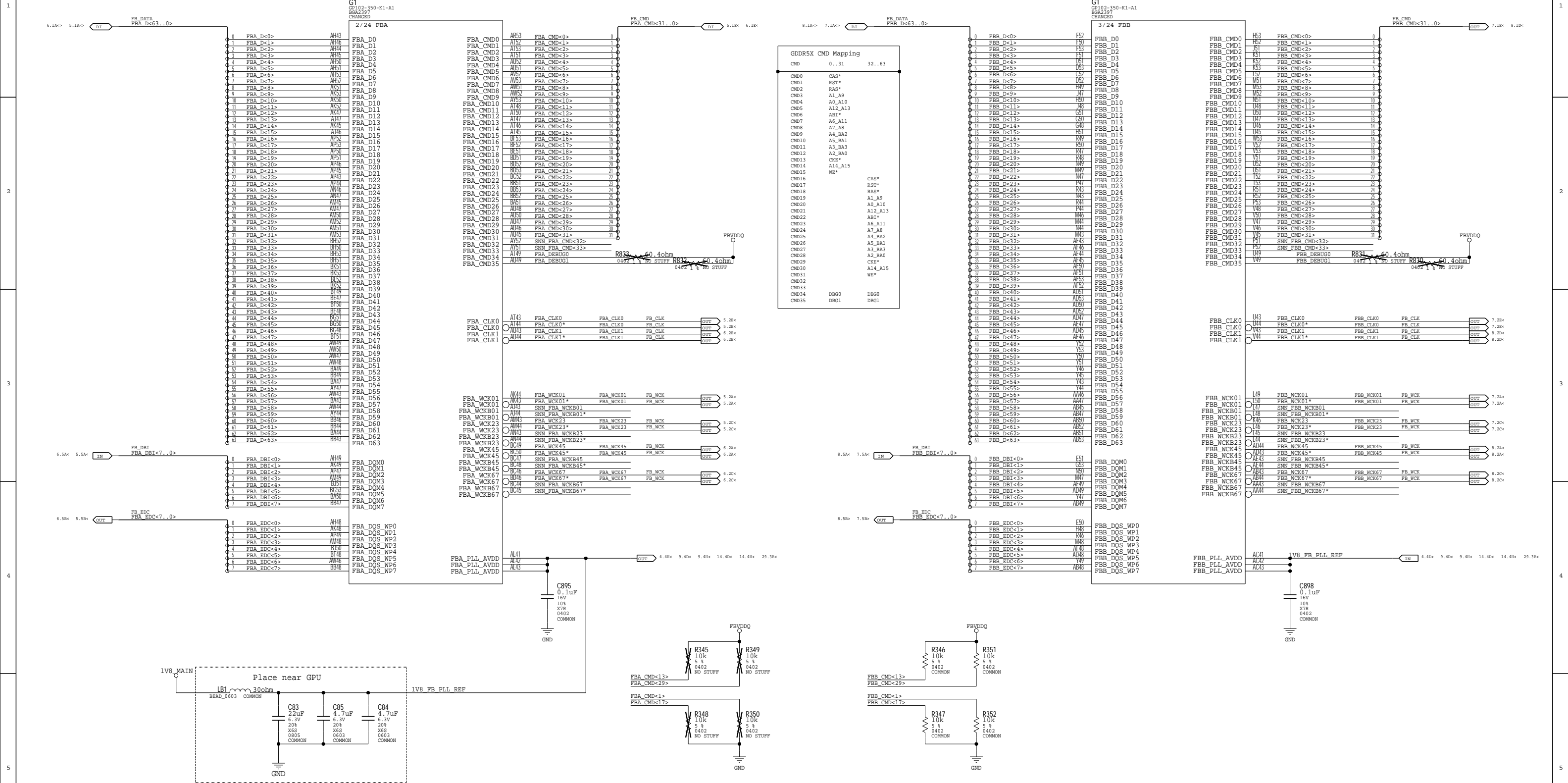
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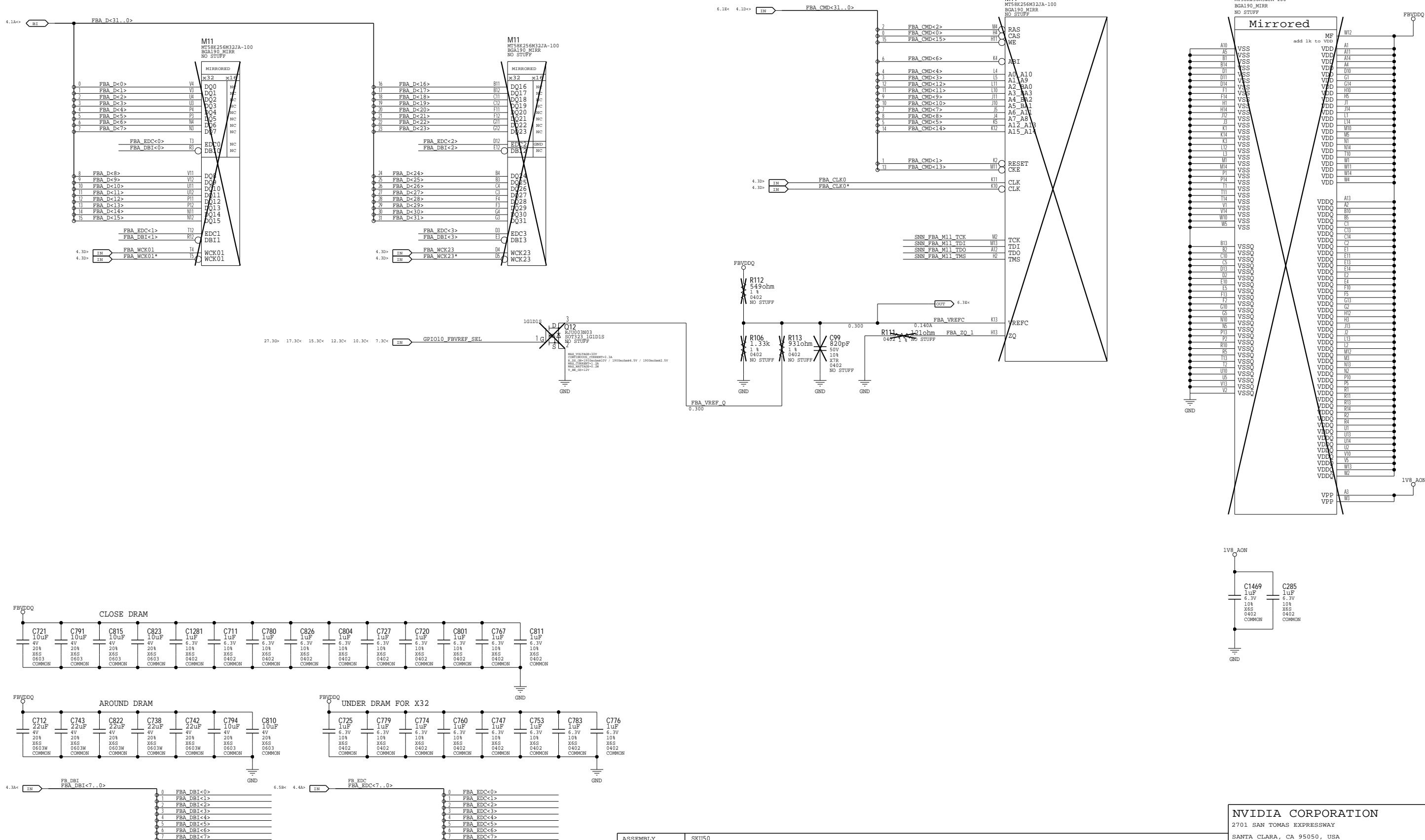
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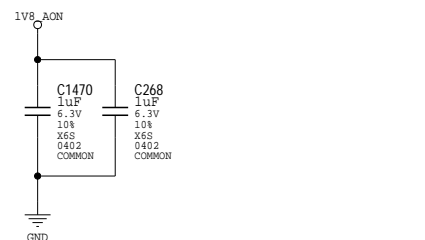
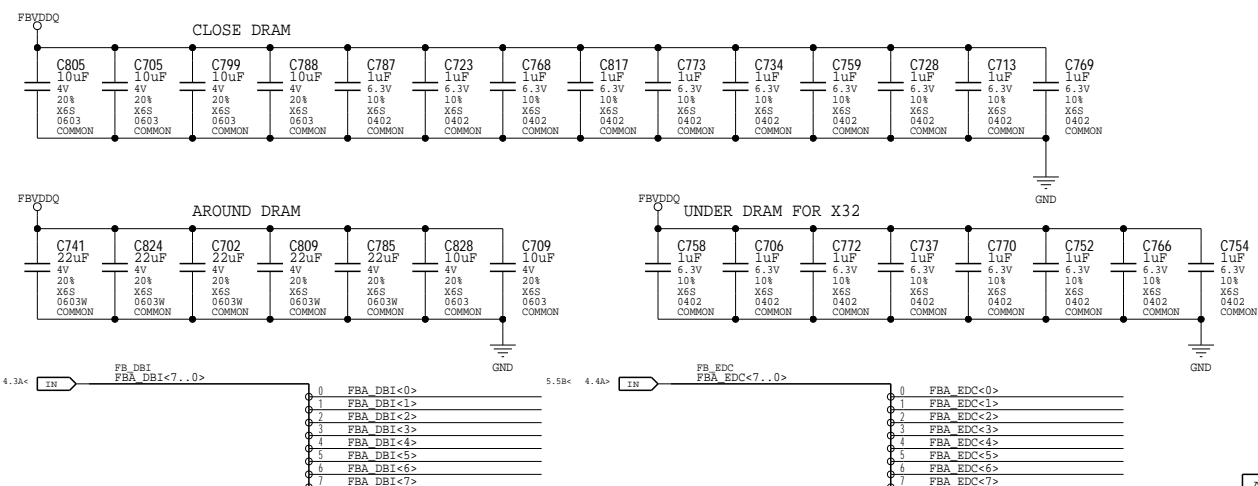
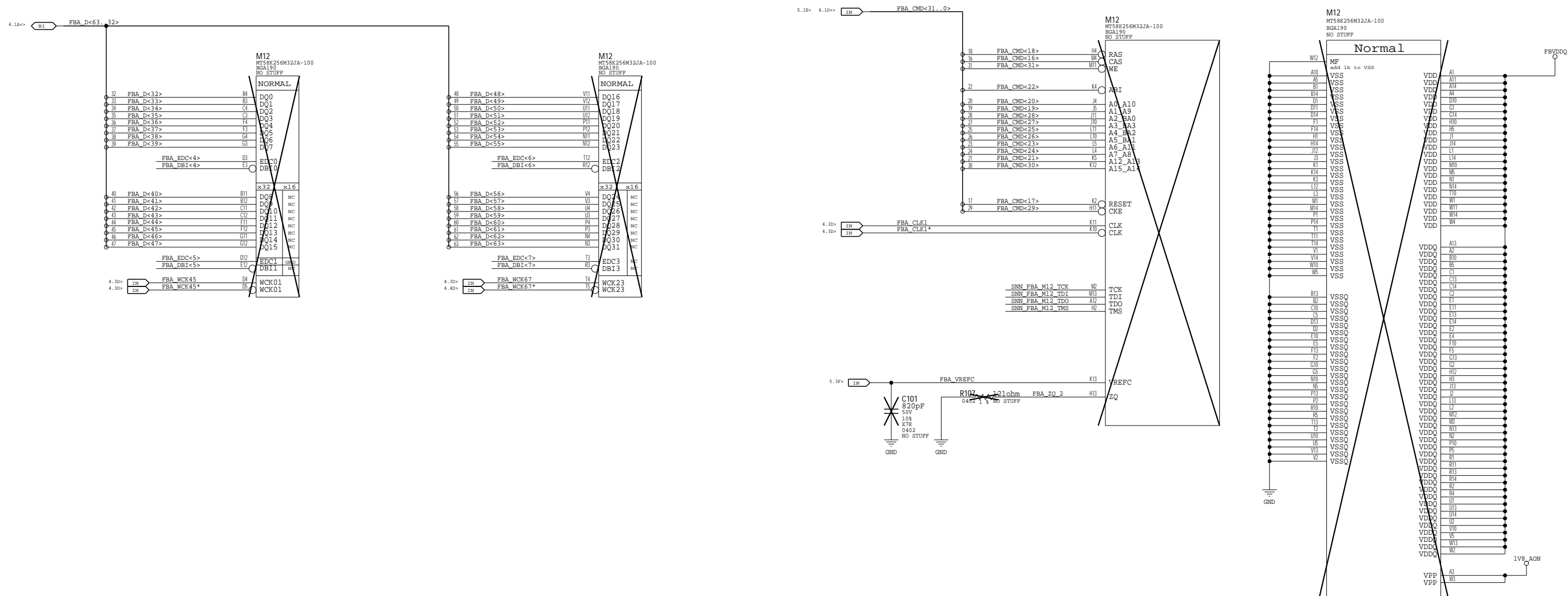
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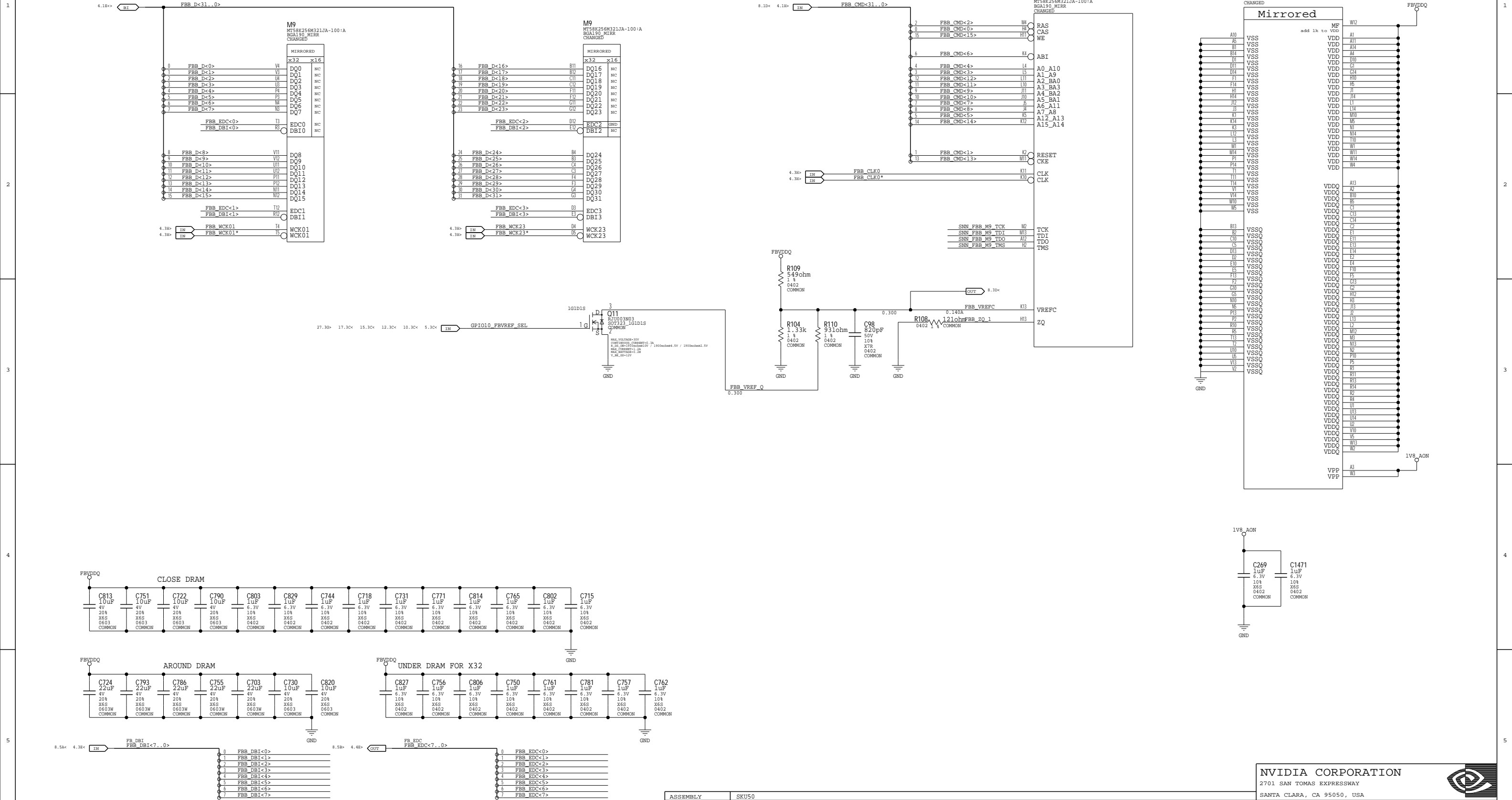
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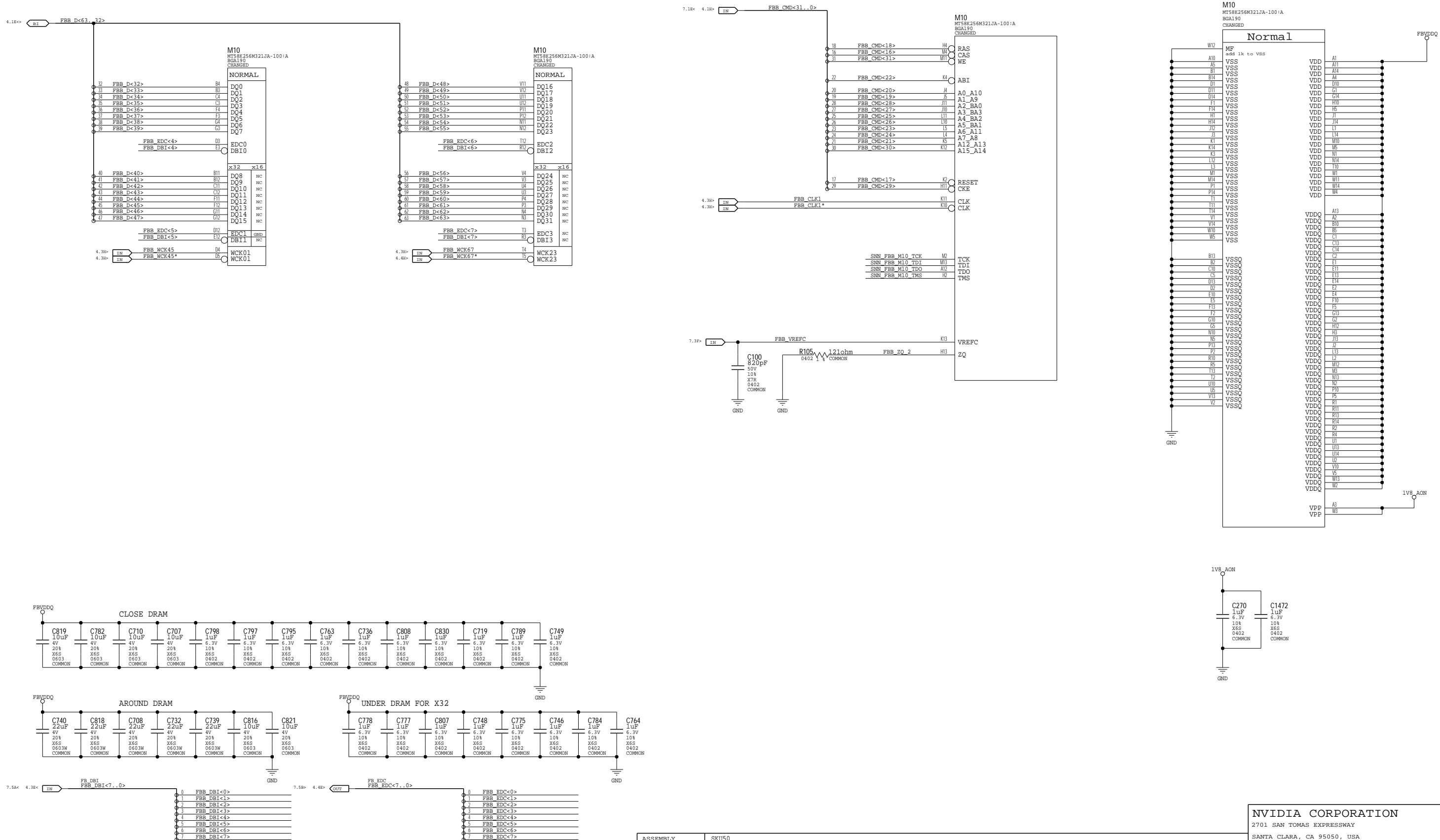
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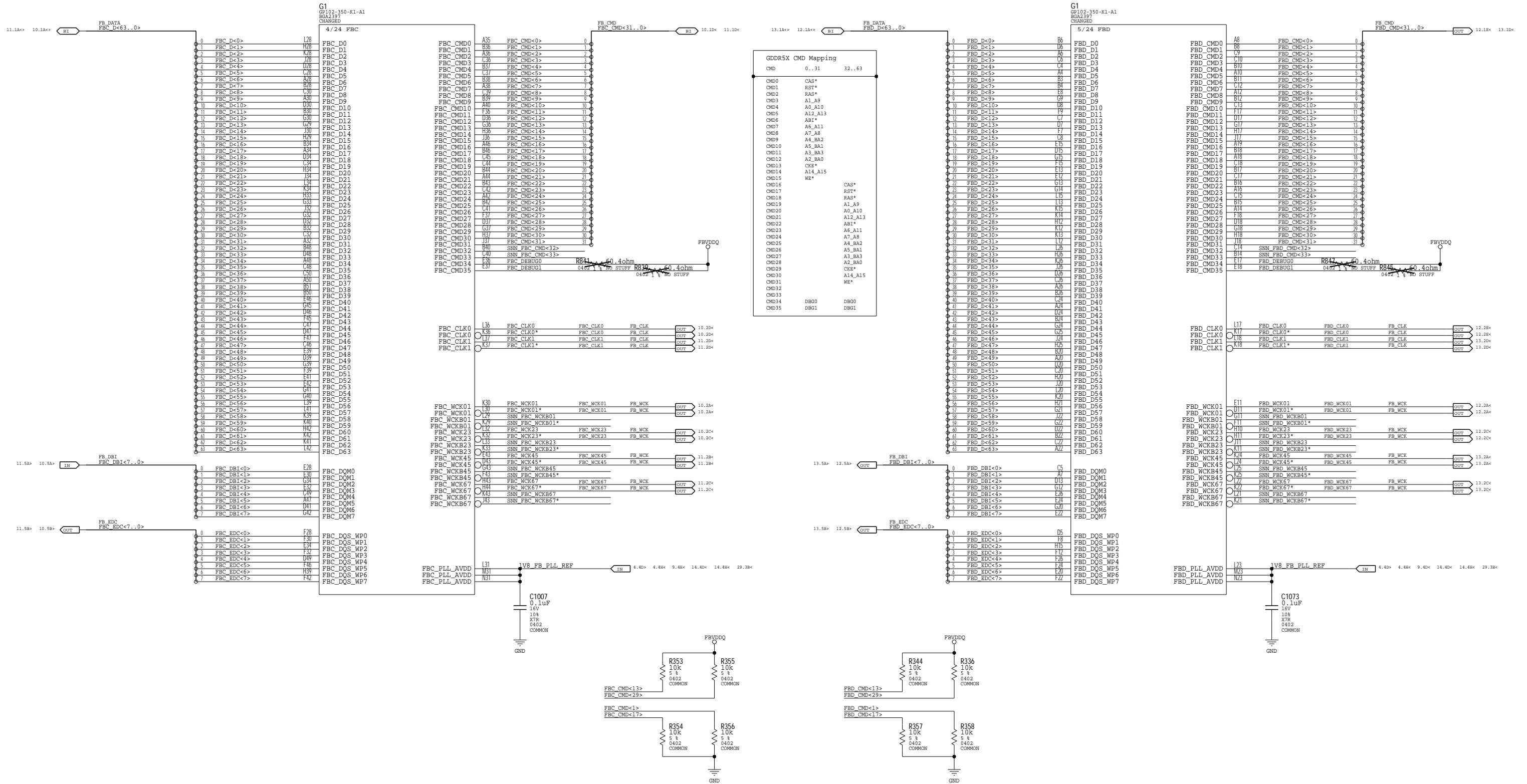
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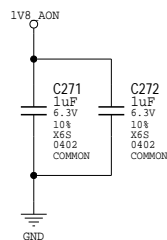
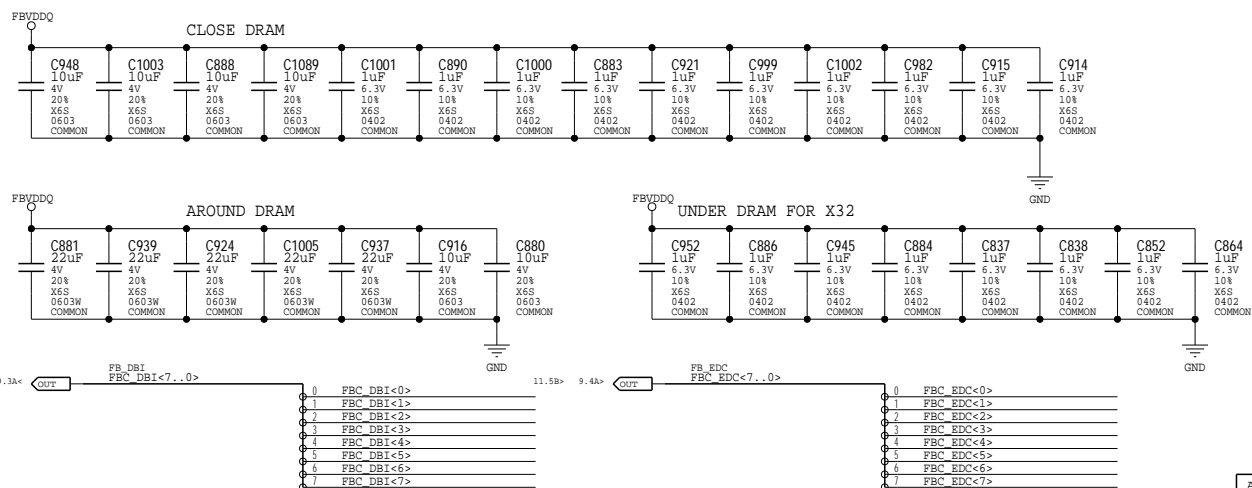
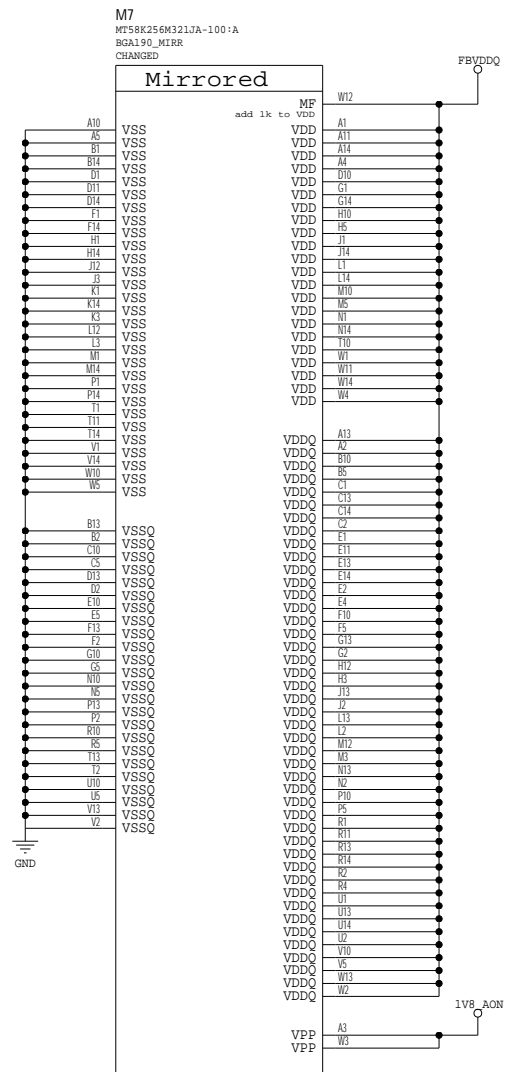
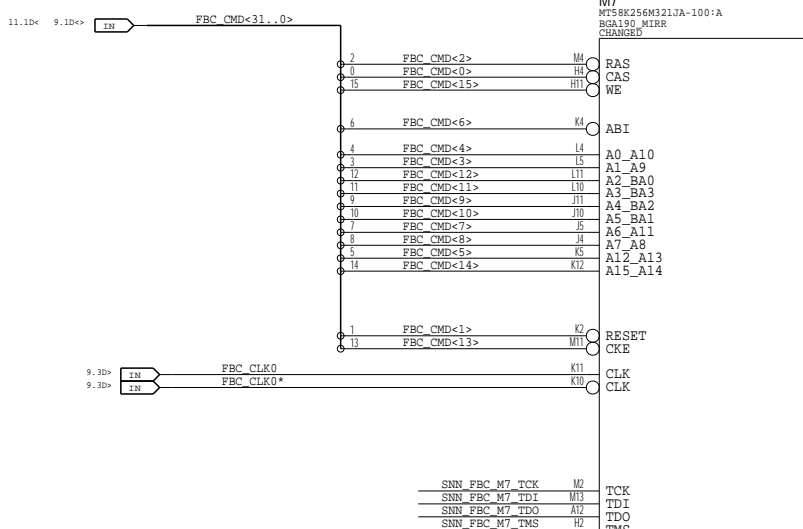
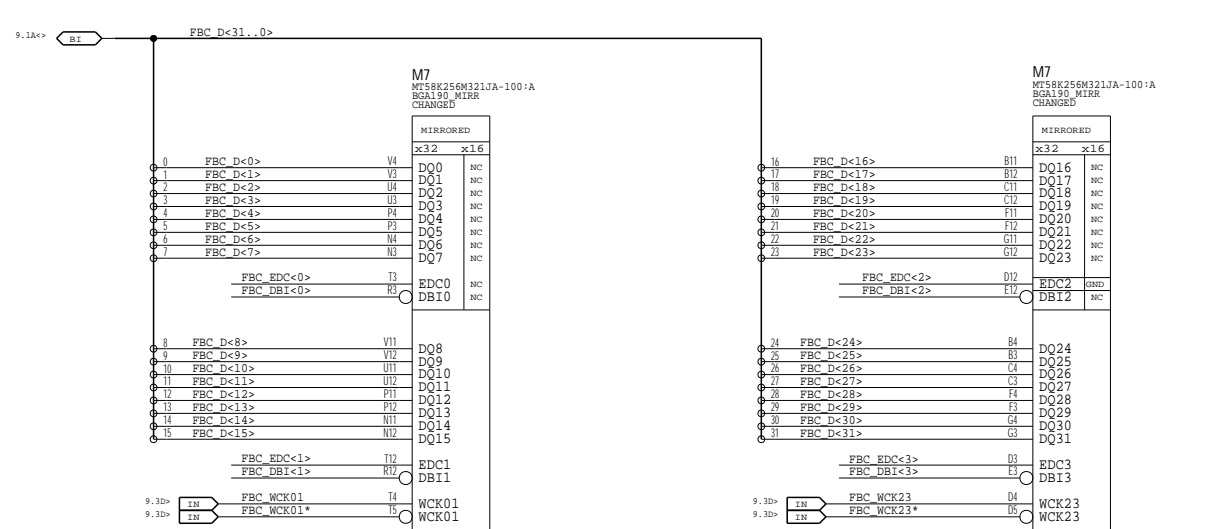
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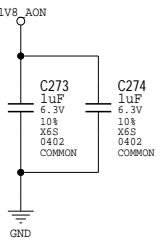
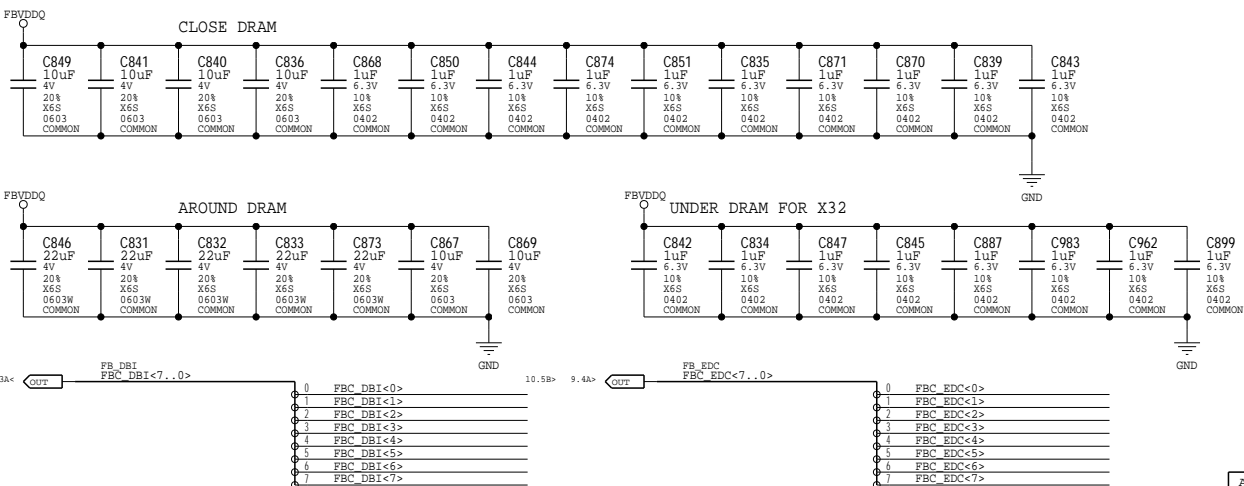
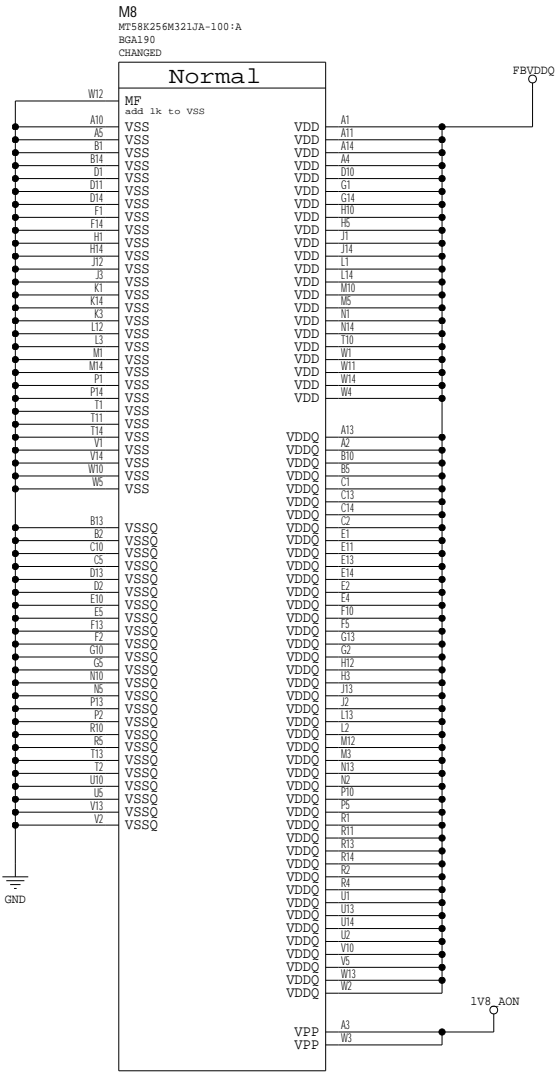
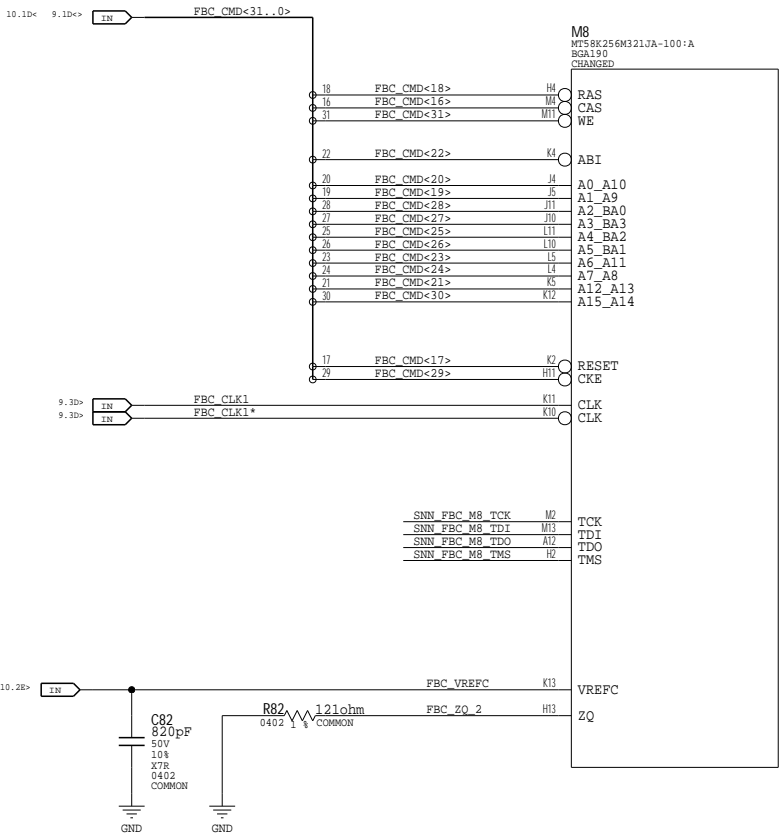
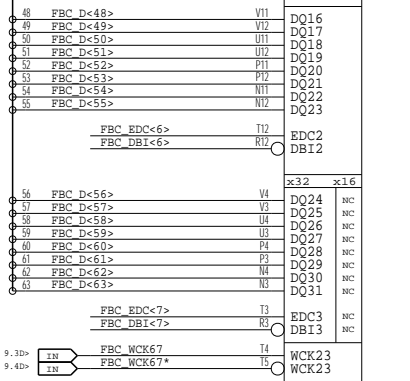
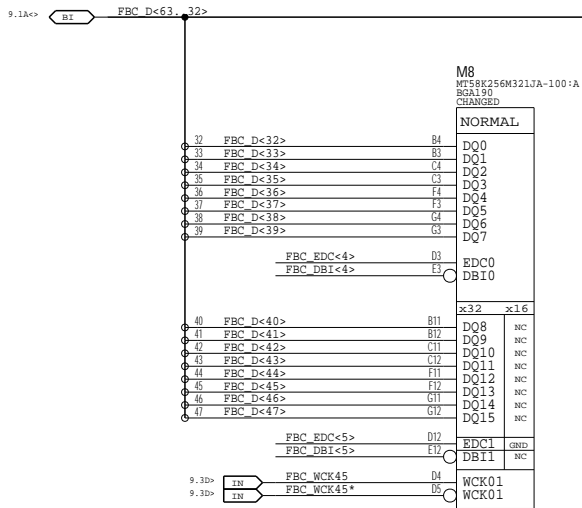
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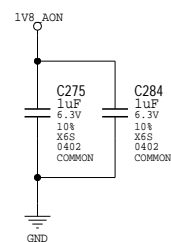
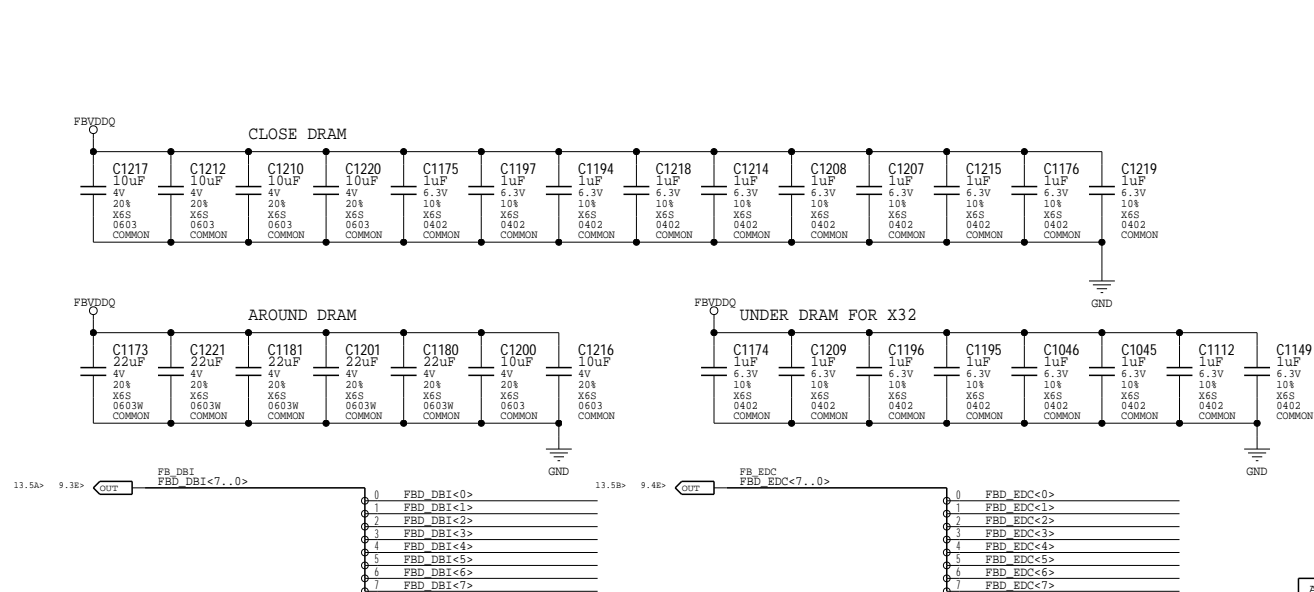
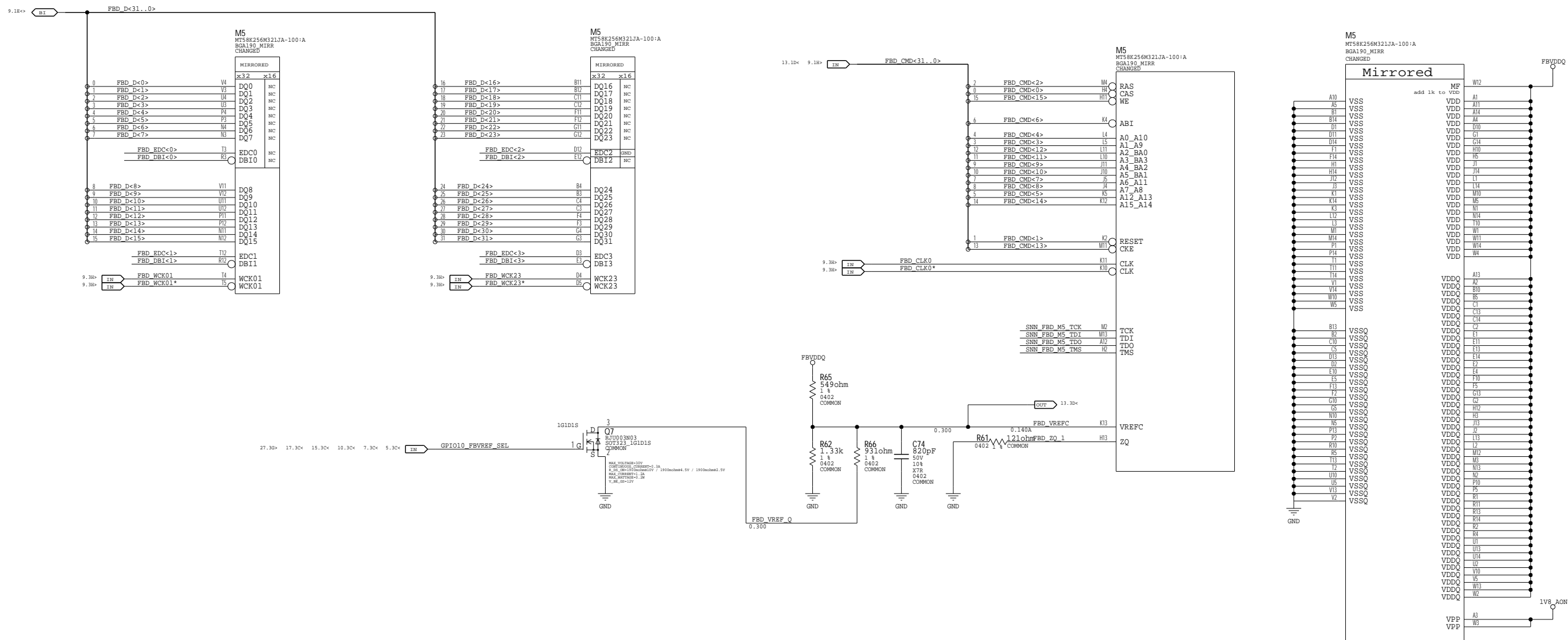


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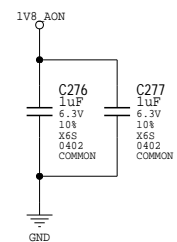
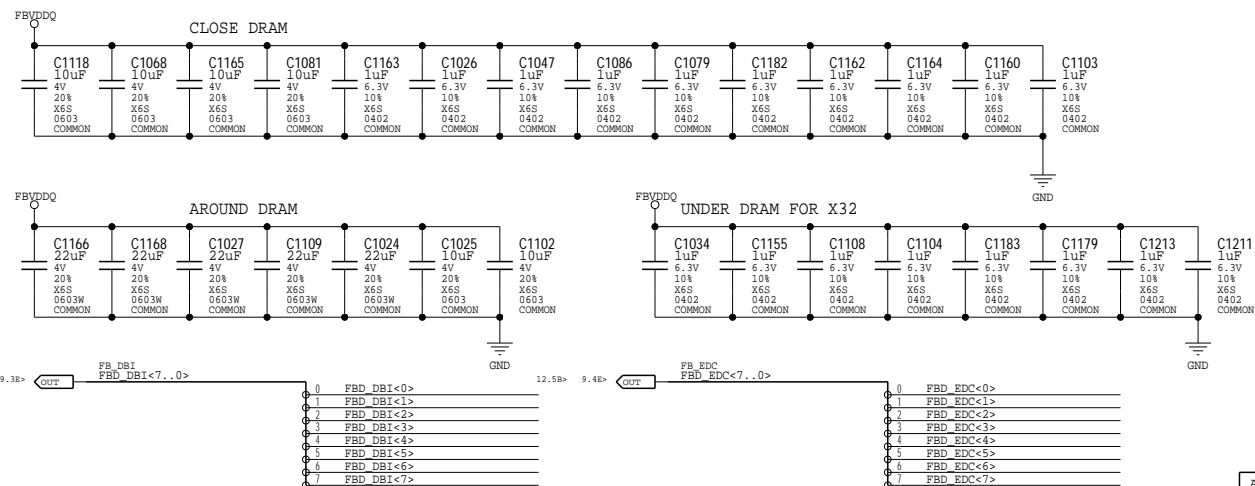
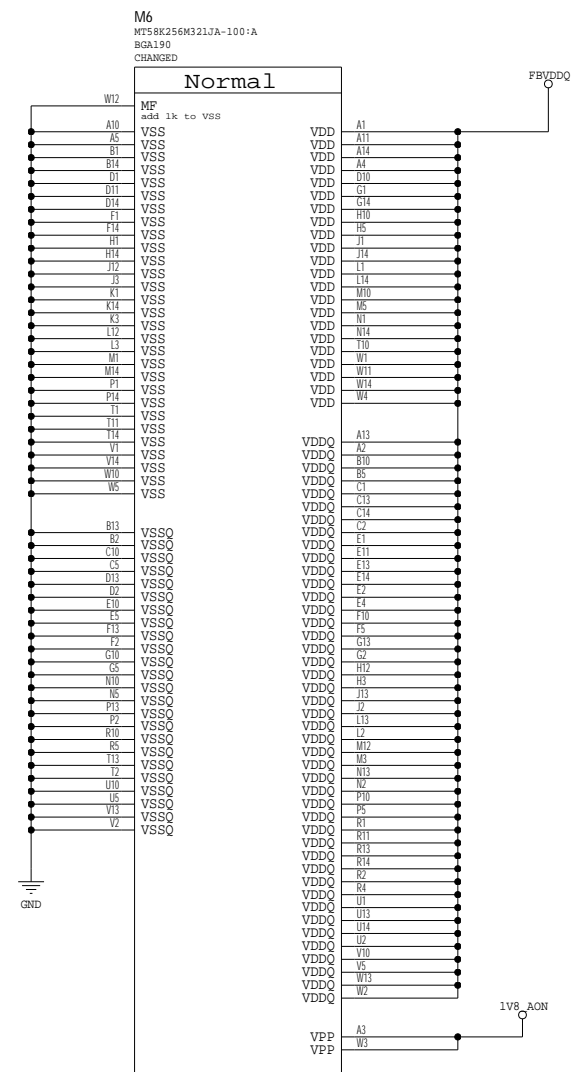
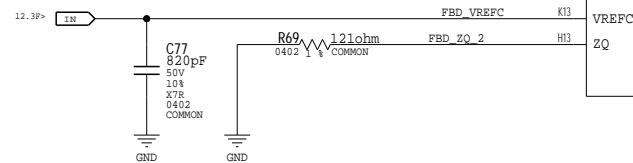
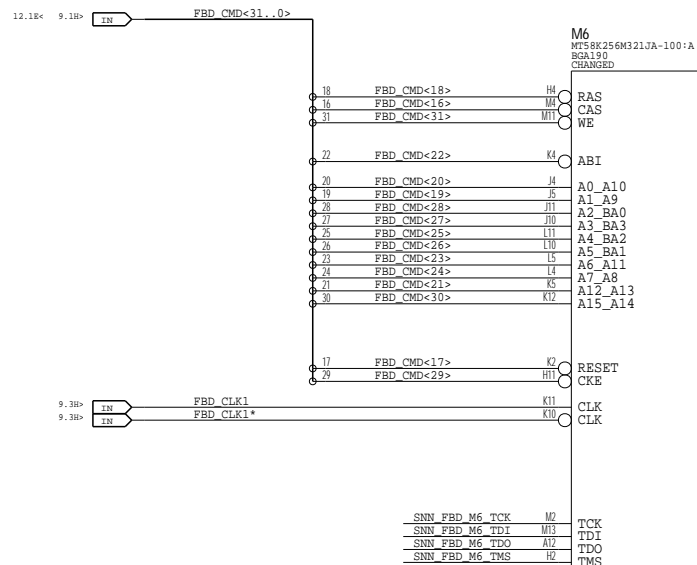
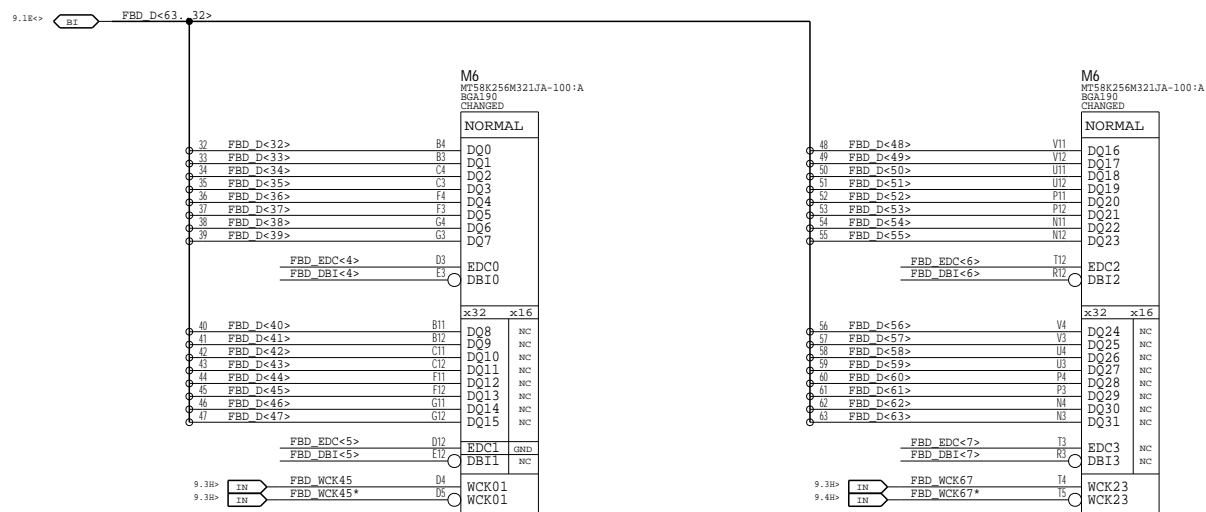
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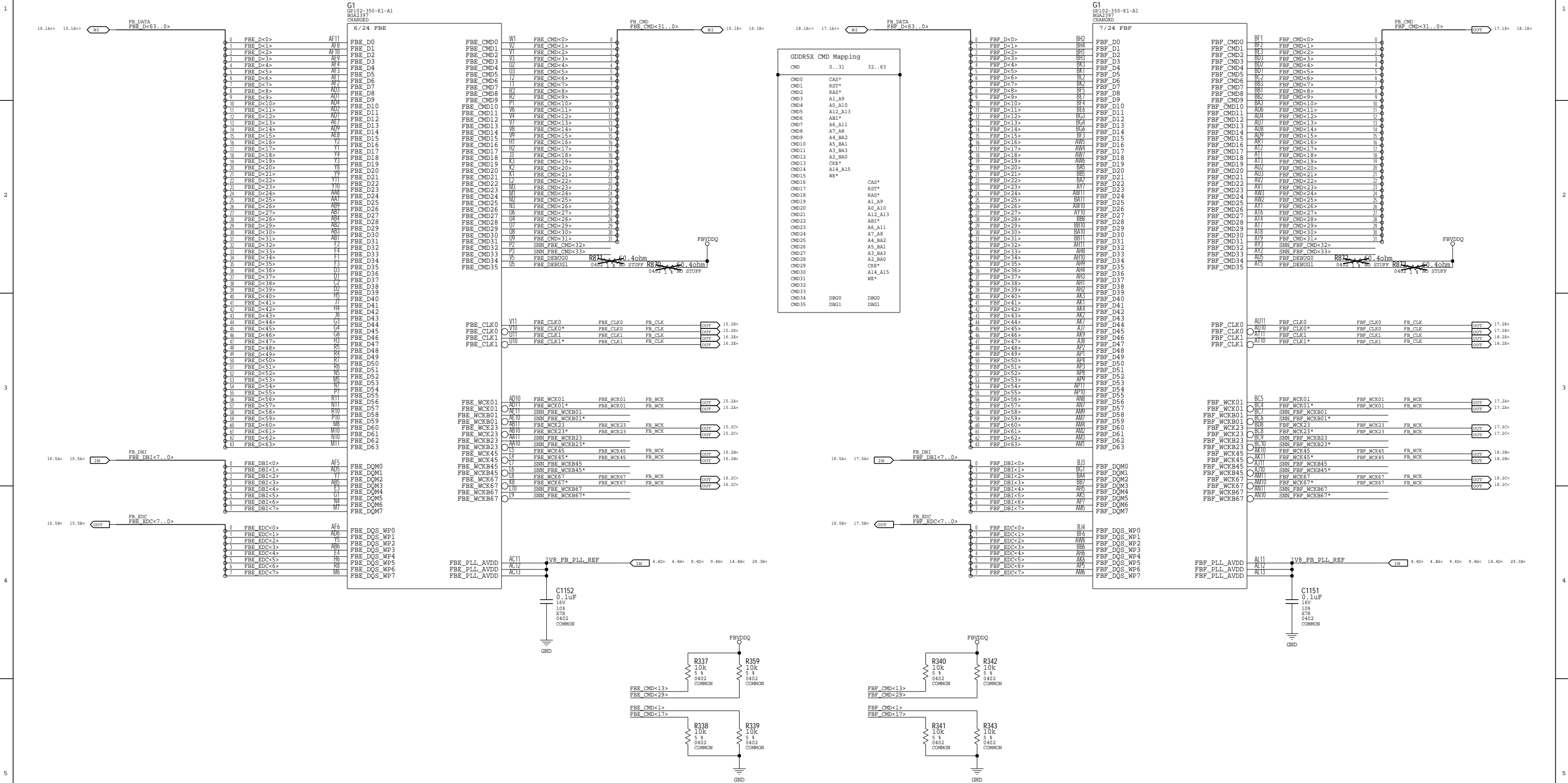
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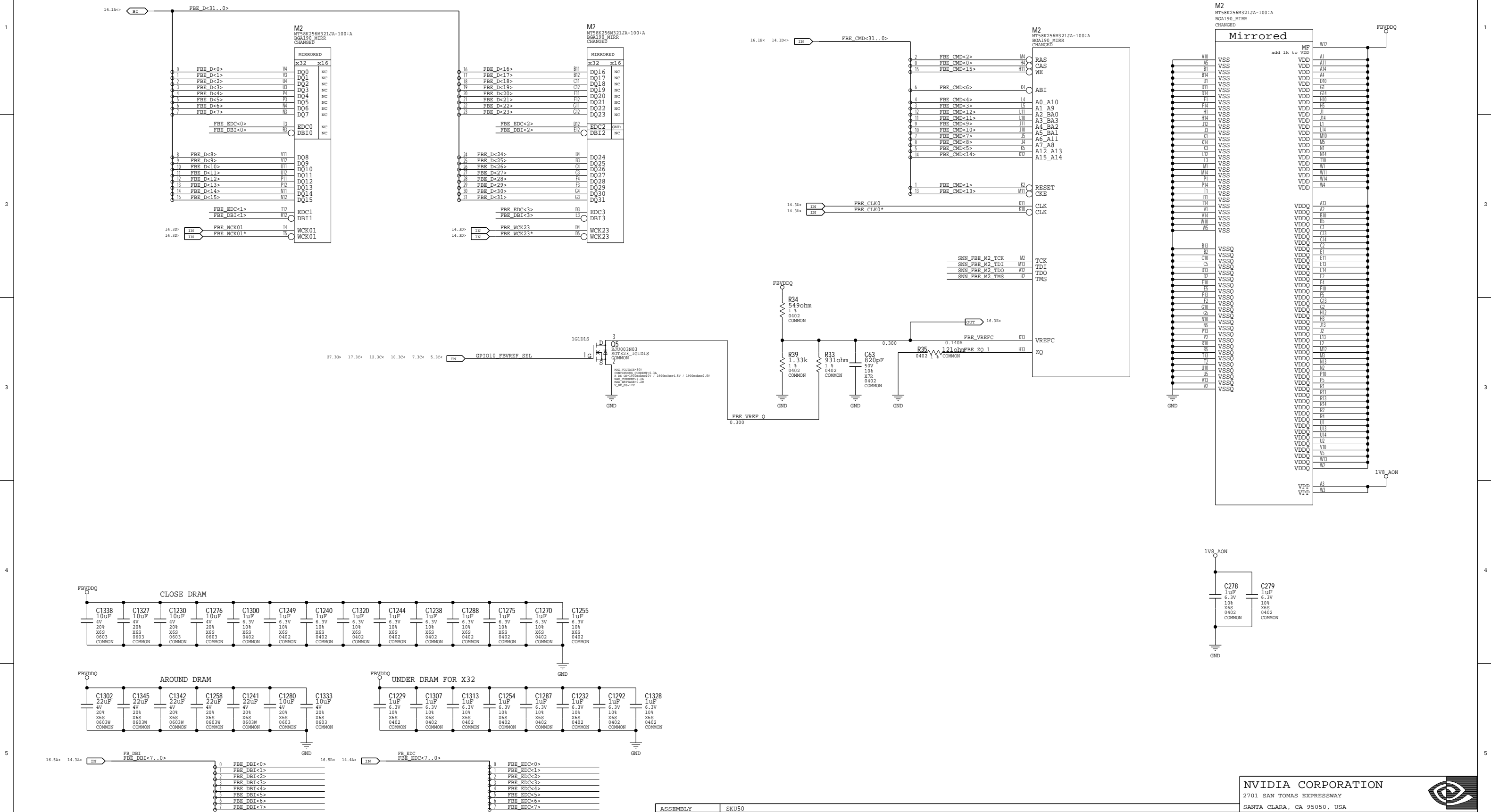
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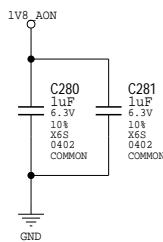
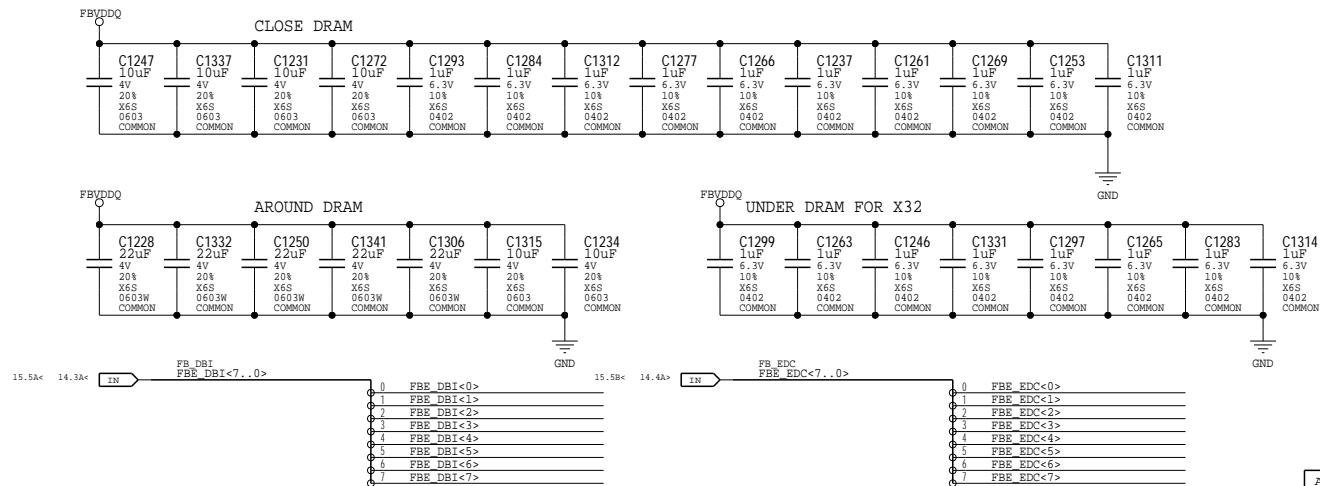
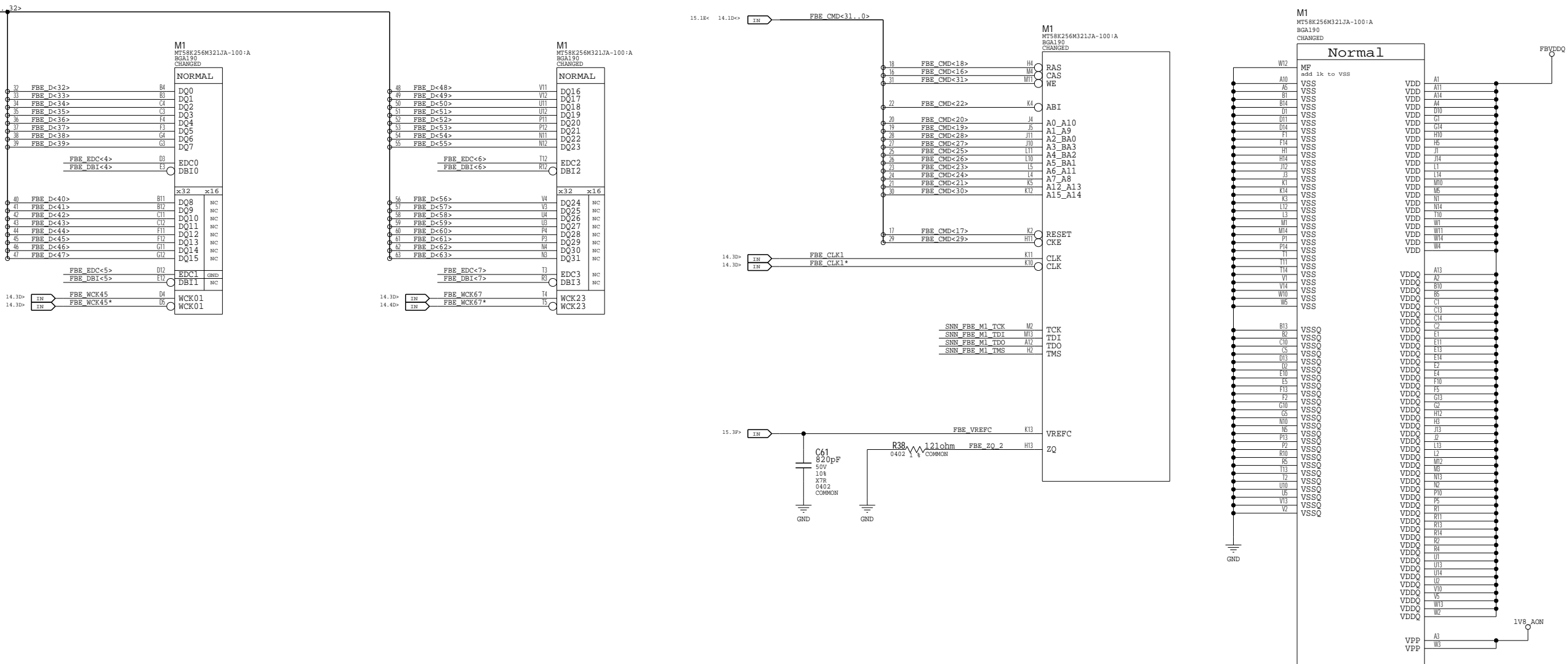
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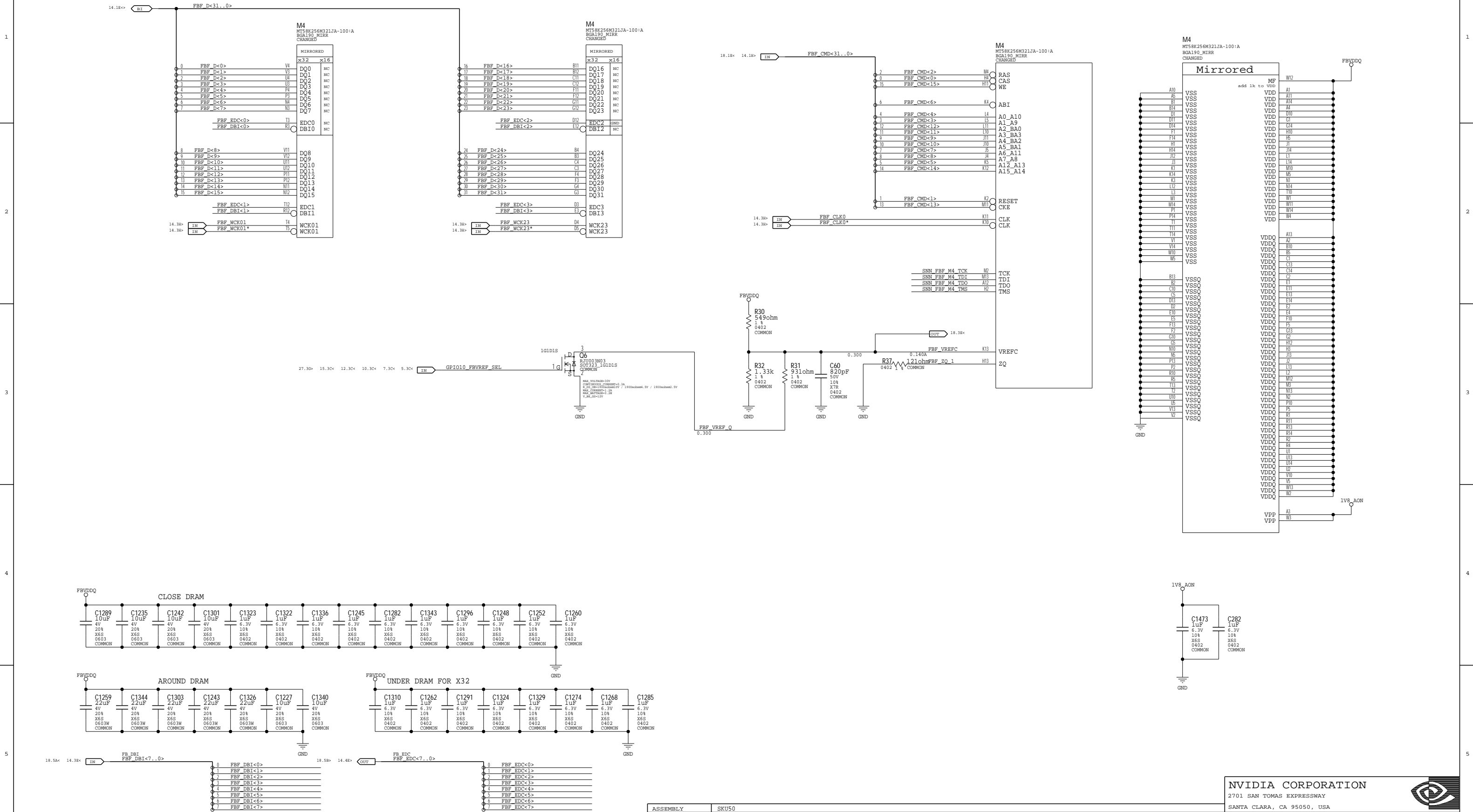
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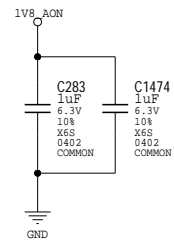
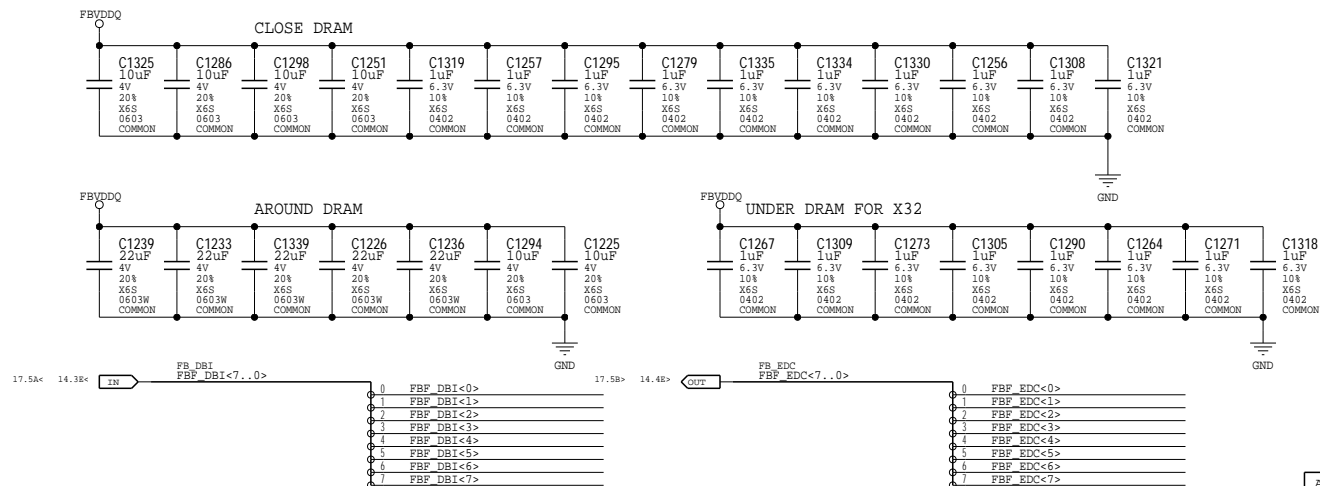
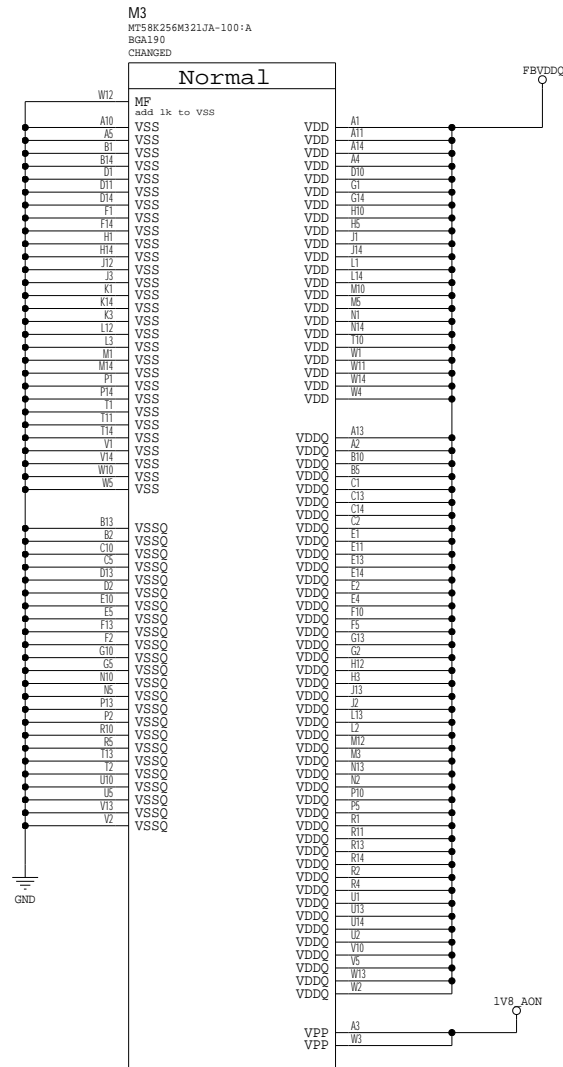
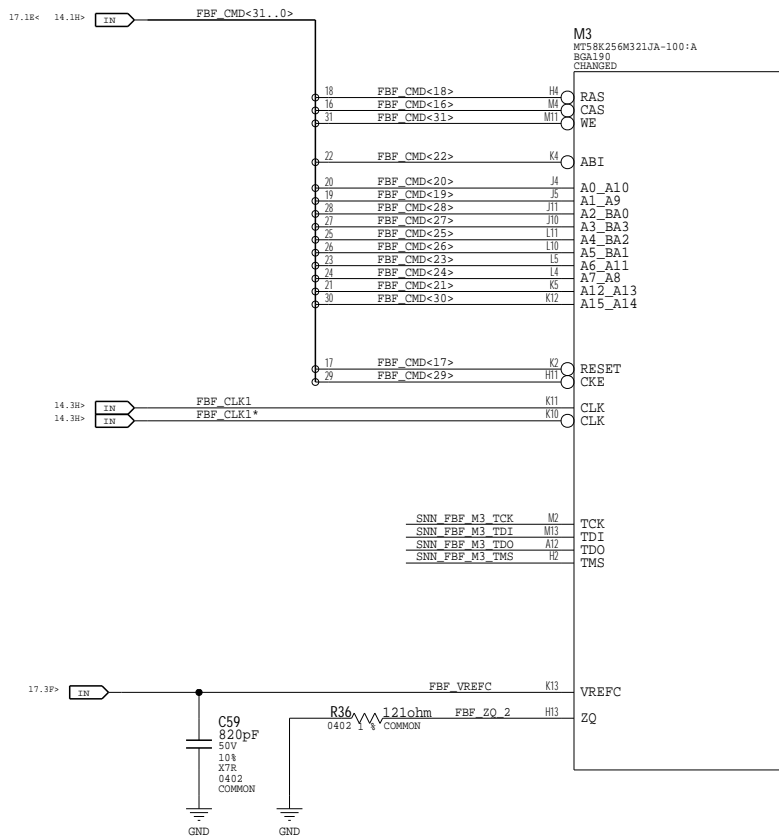
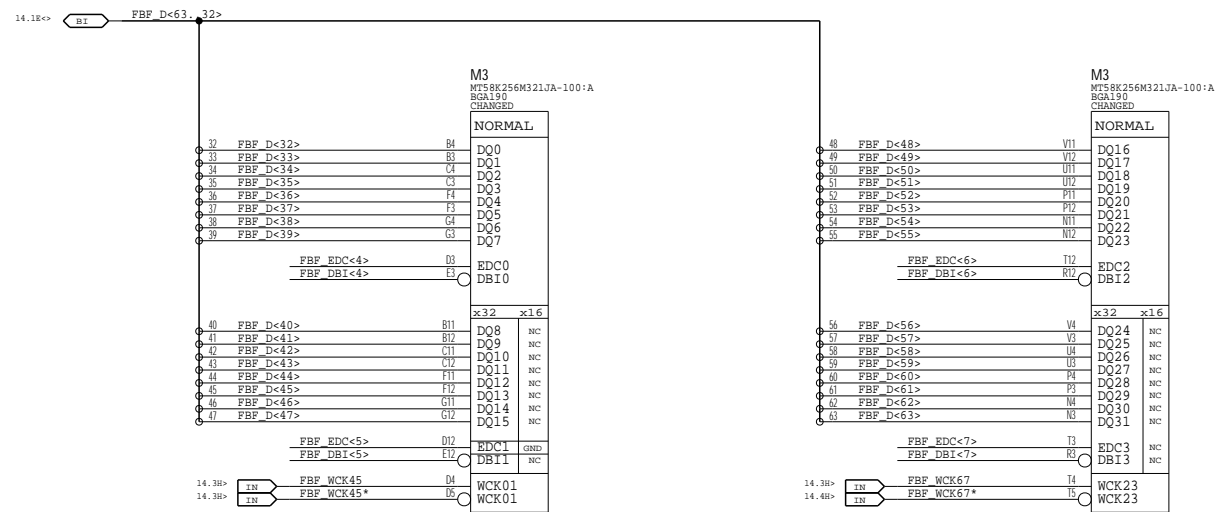
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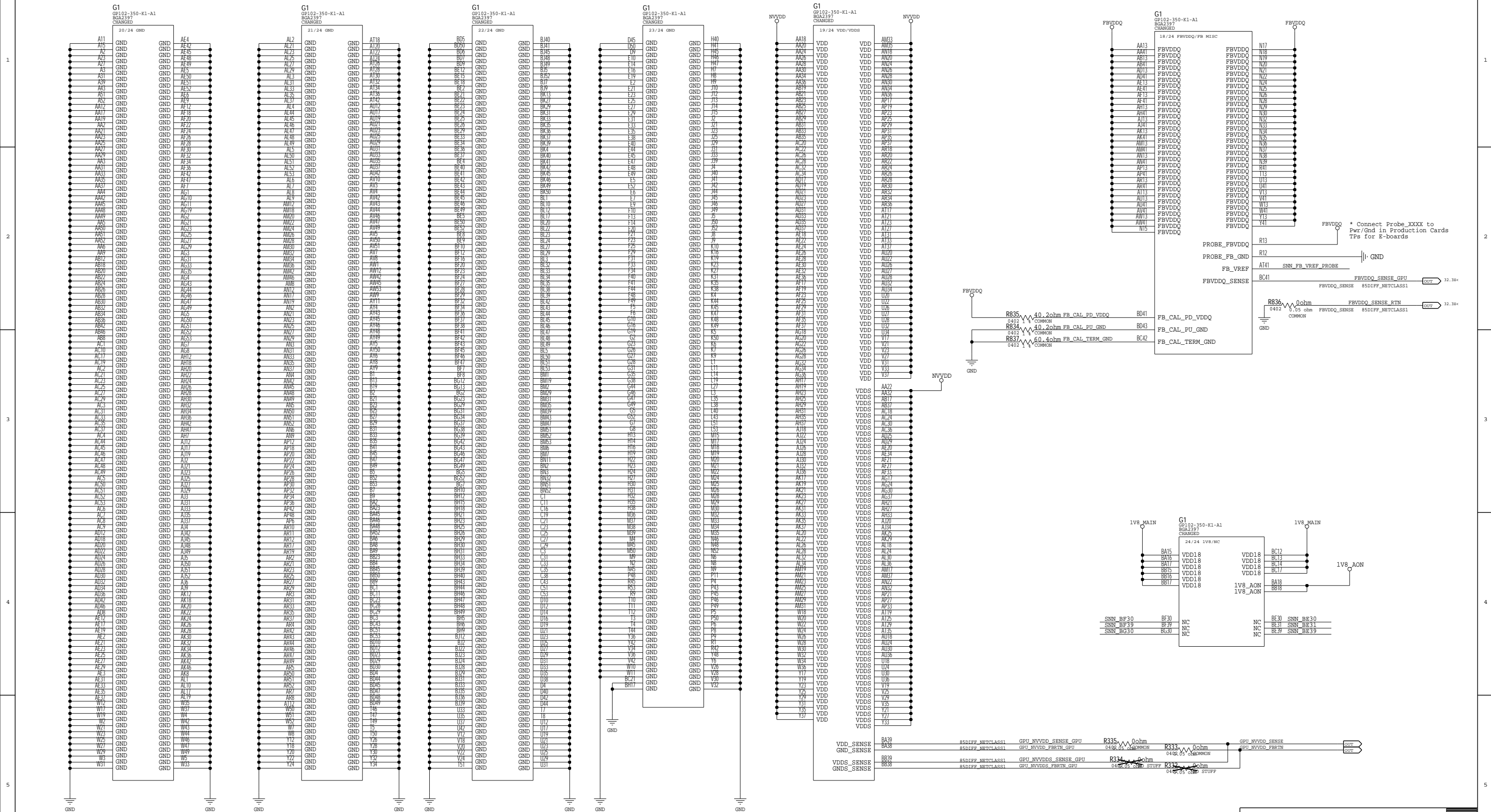
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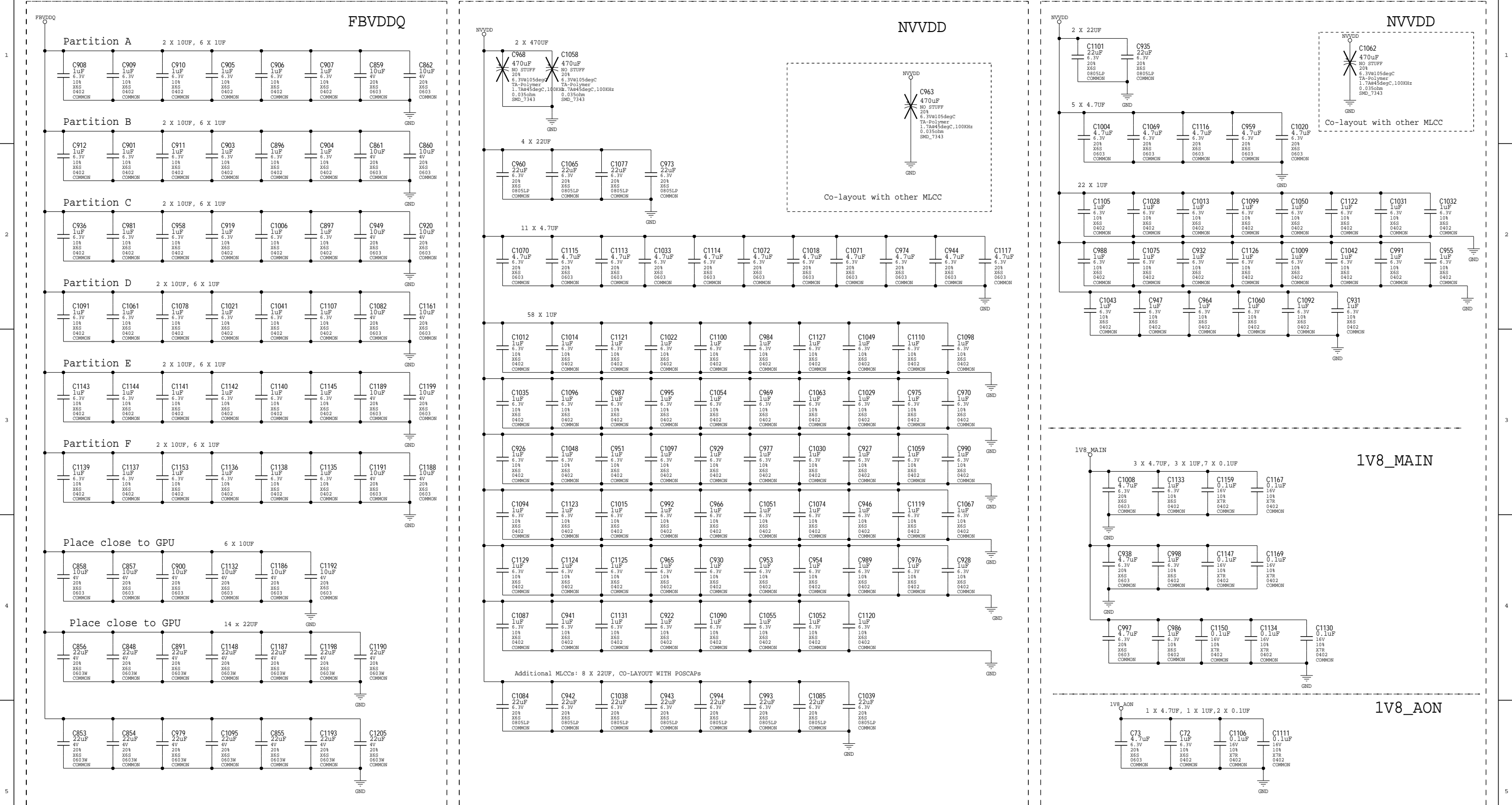
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Page19: GPU PWR and GND





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PAGE DETAIL	GPU DECOUPLING

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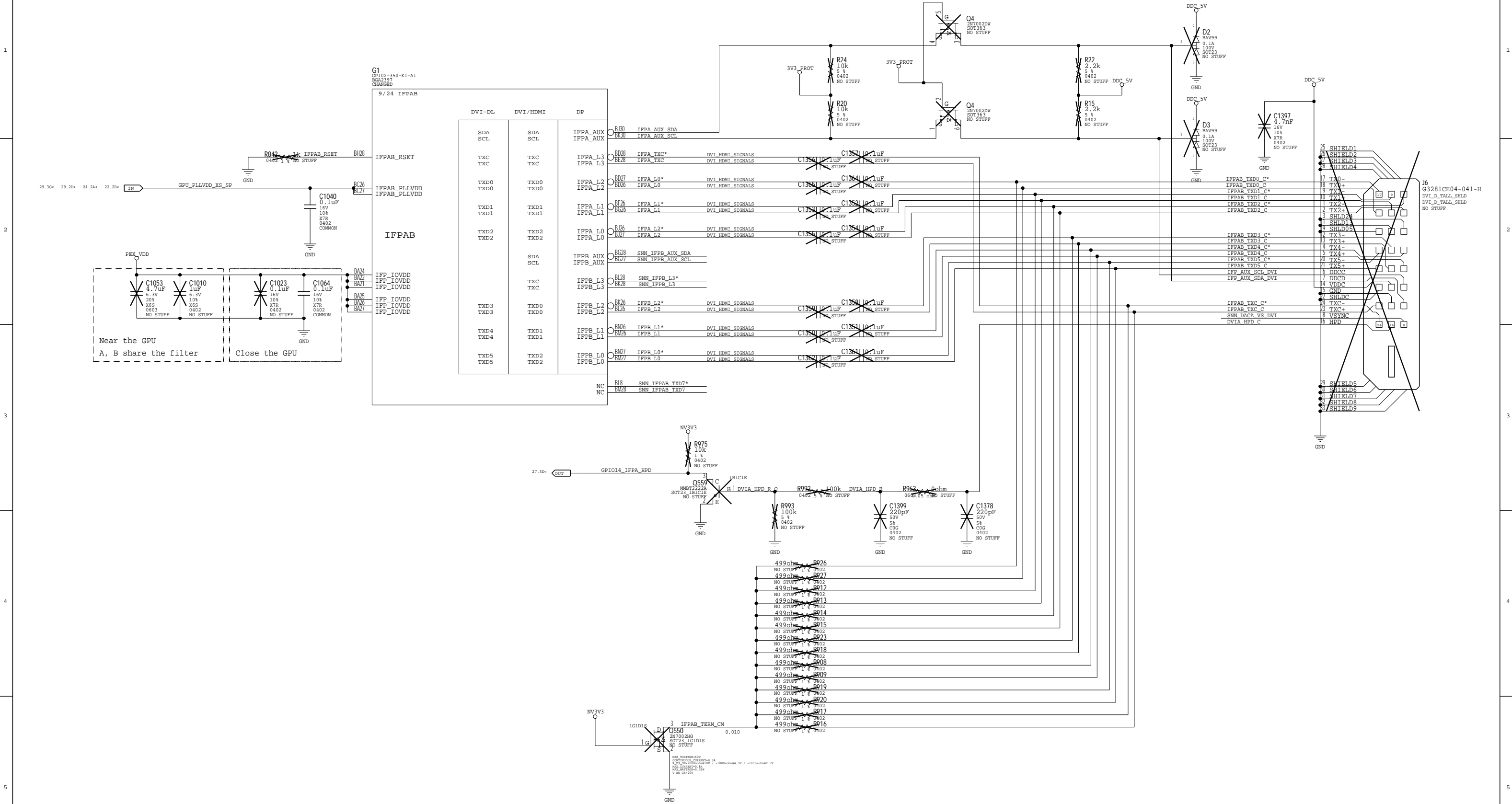
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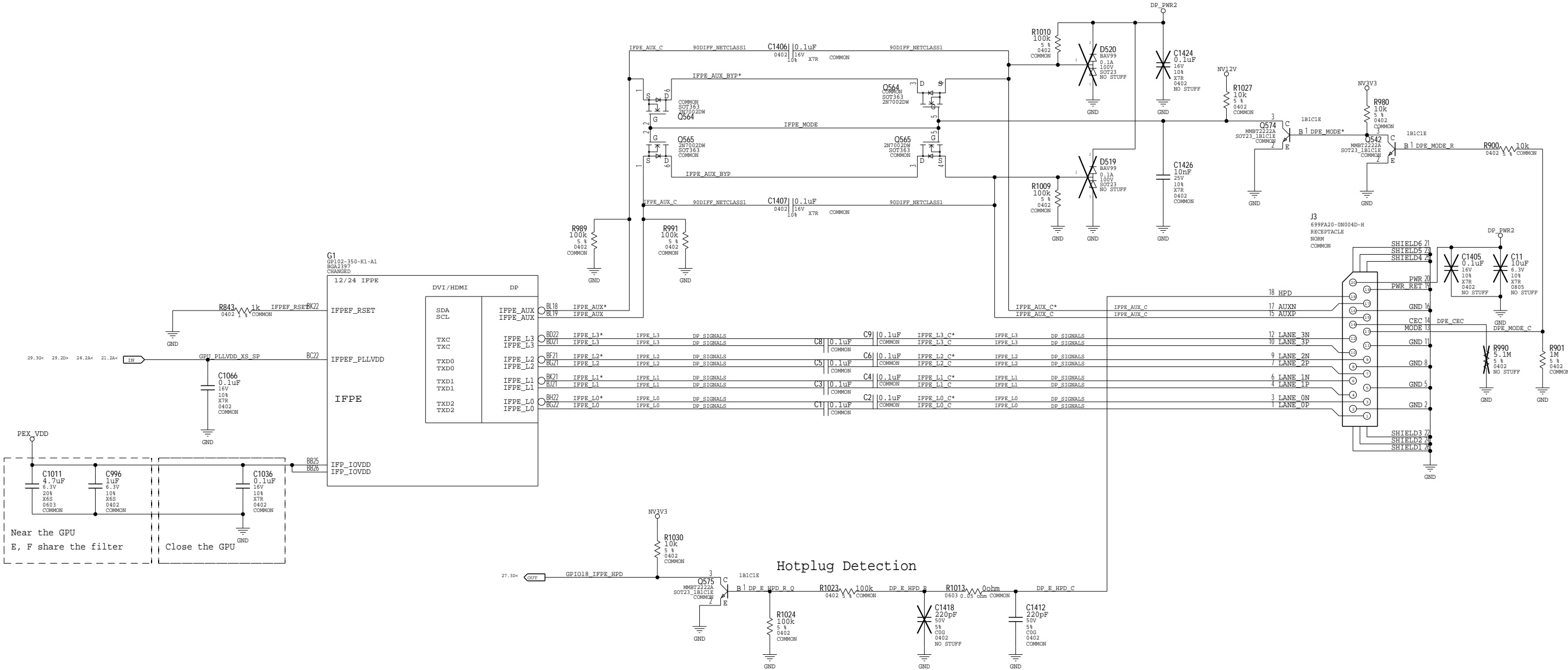
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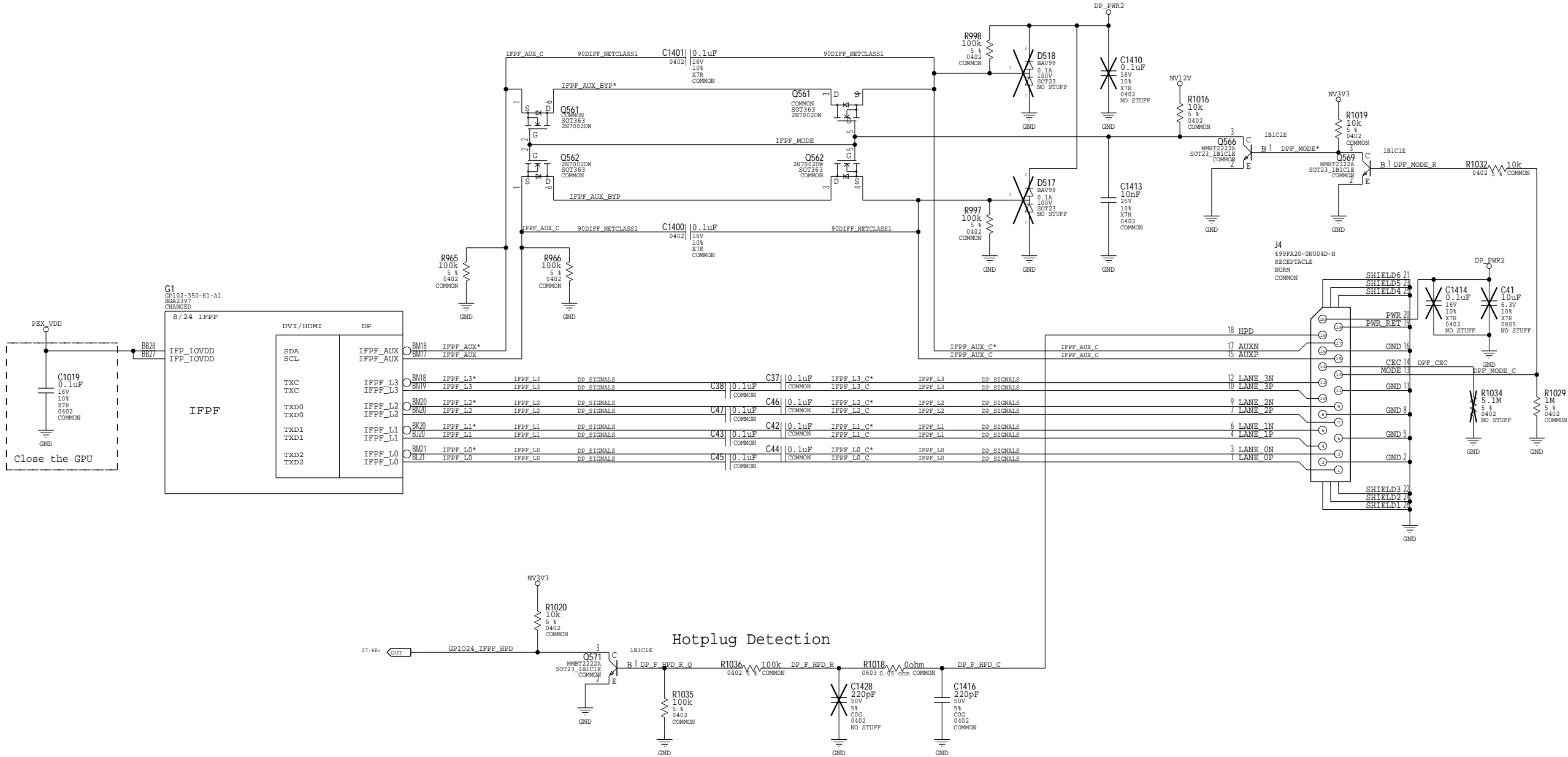
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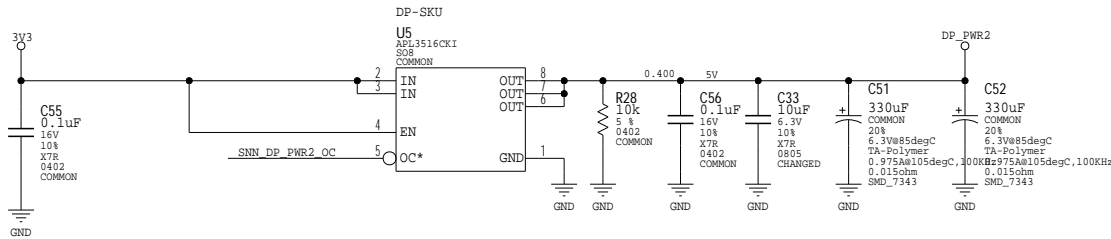
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Fused DP_PWR



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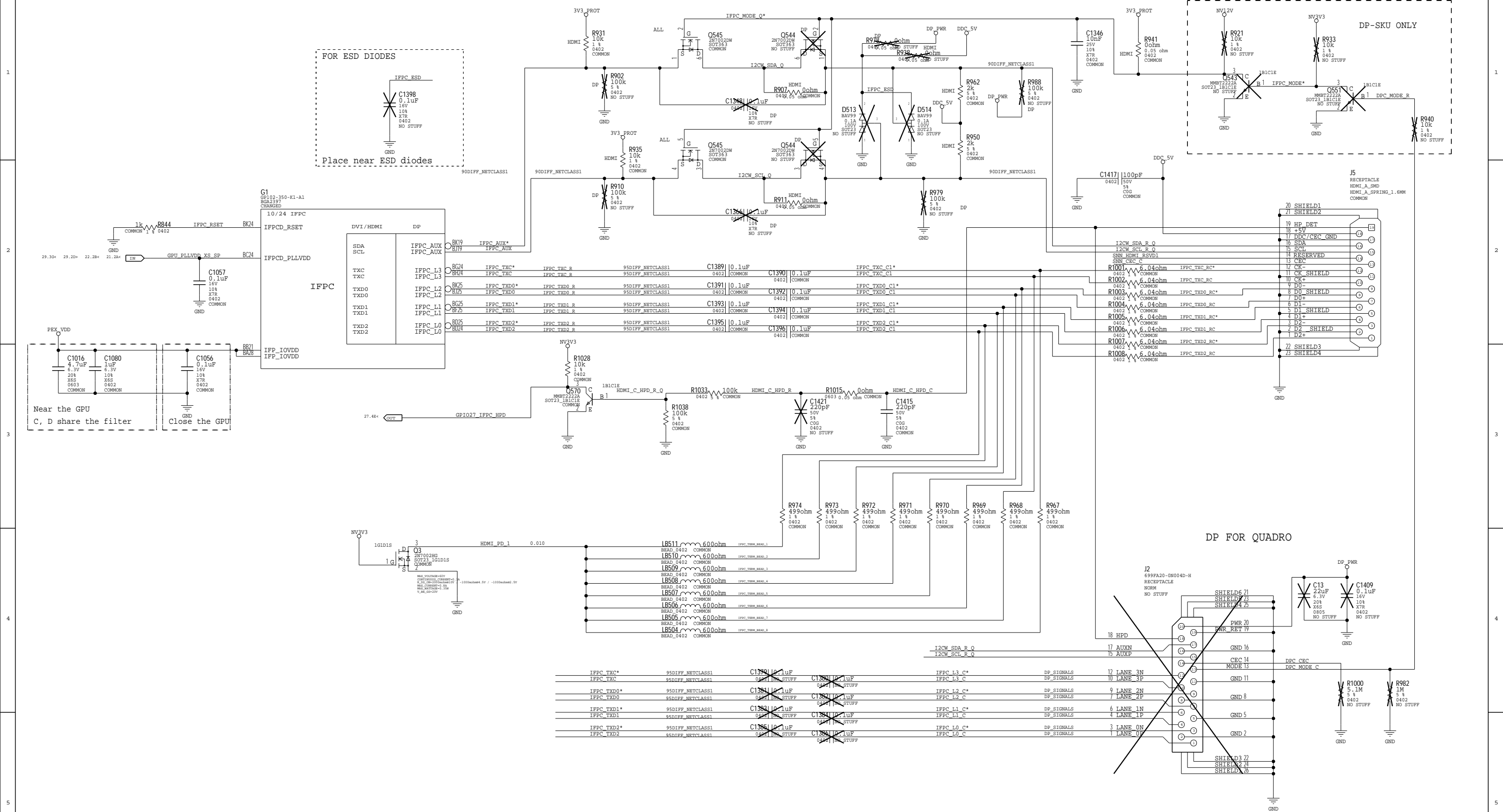
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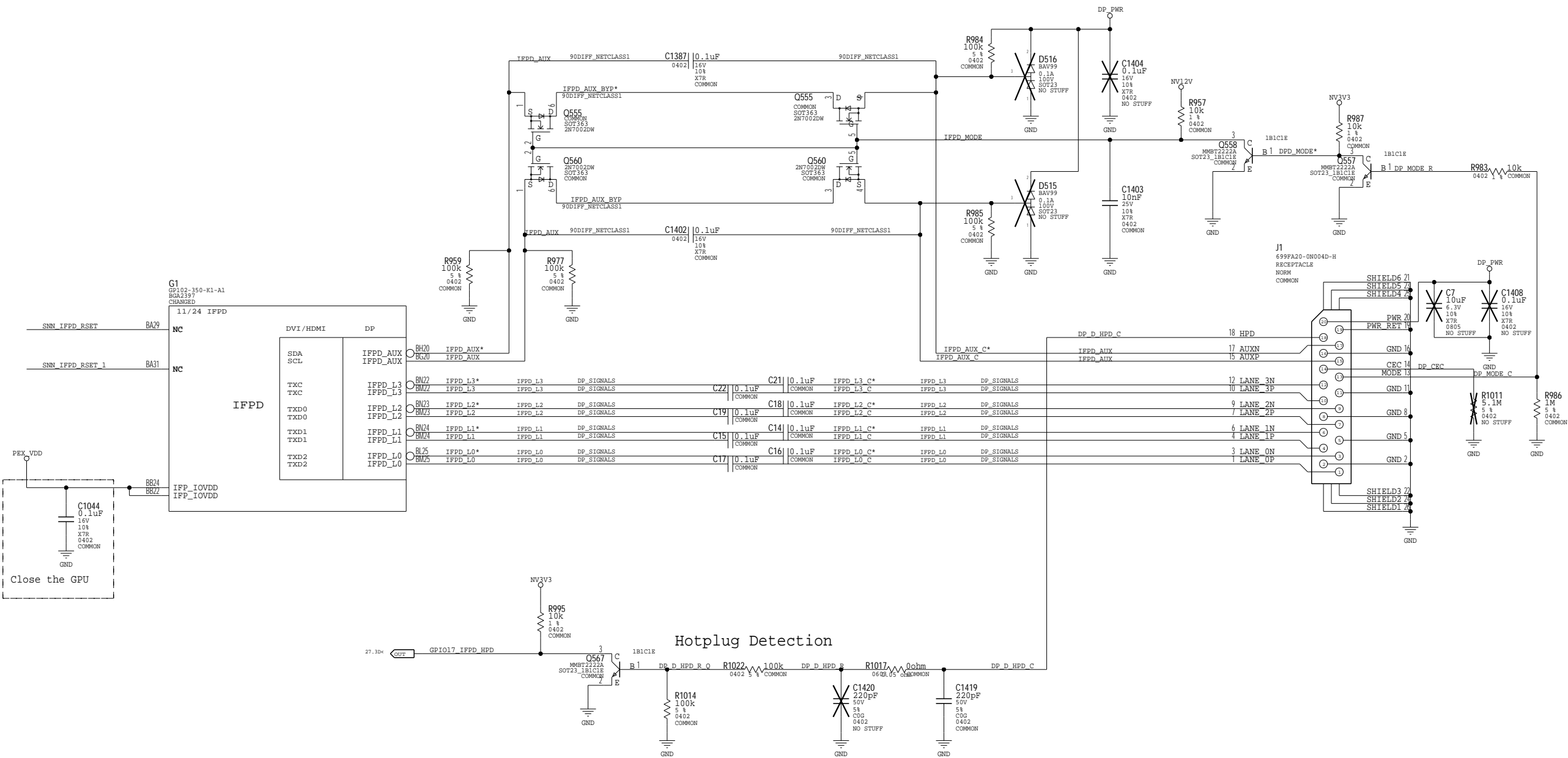


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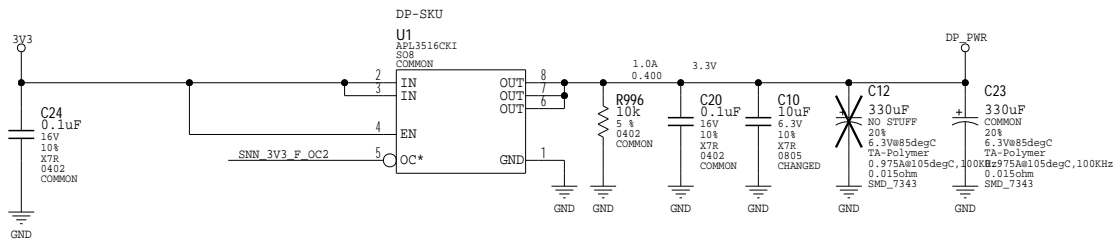
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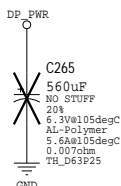




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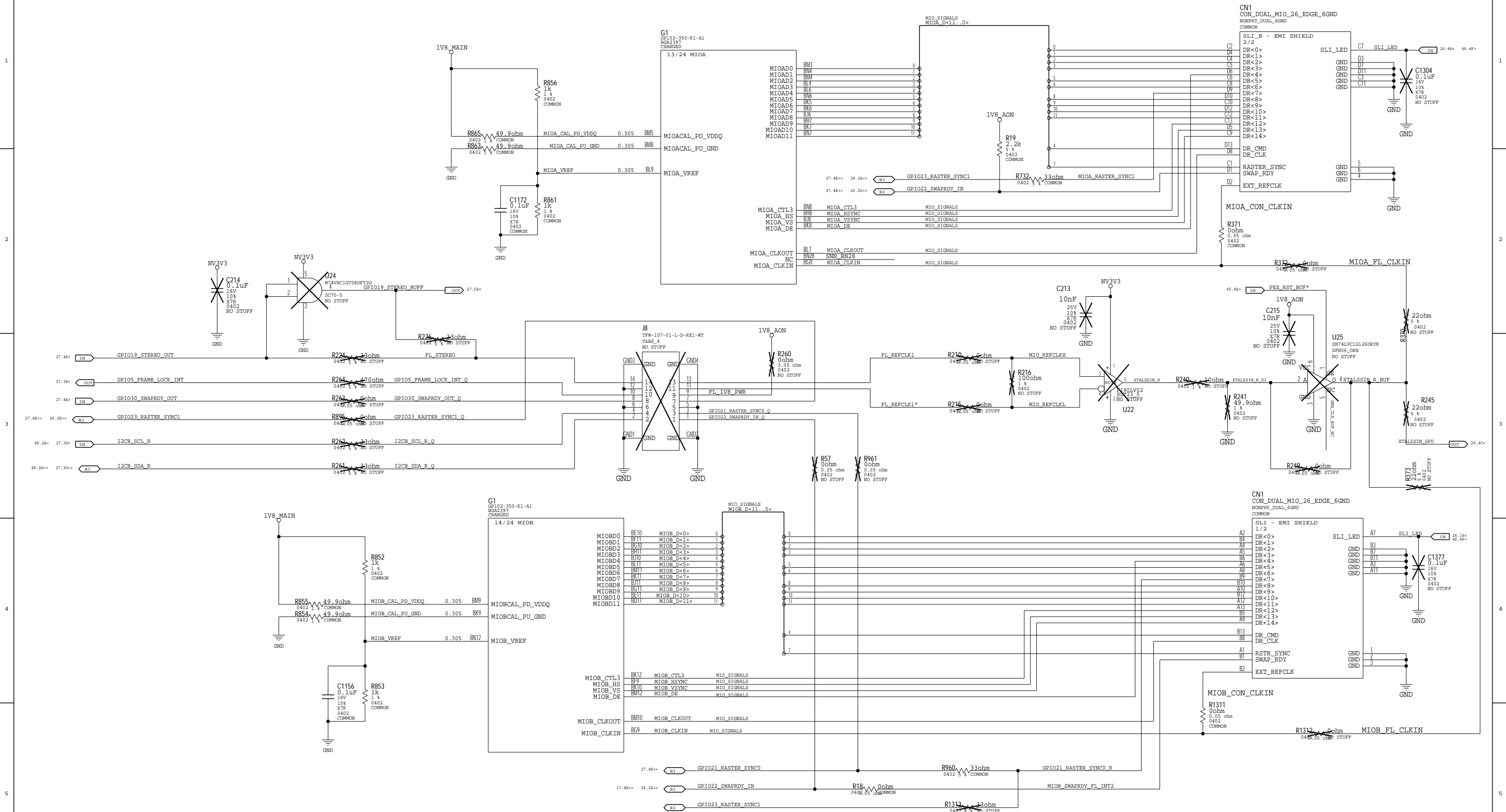
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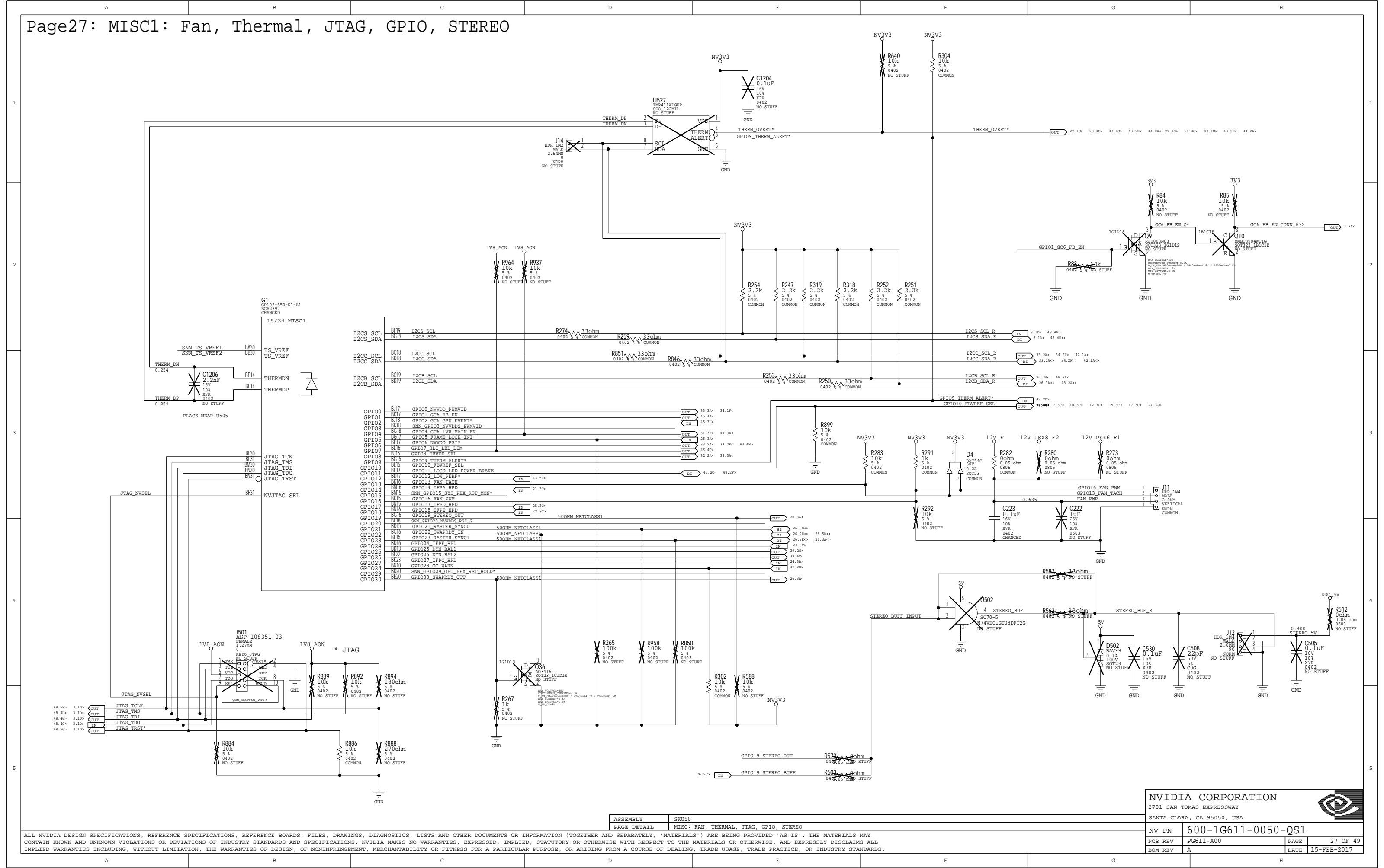
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Page26: MIOA/B Interface and FRAME LOCK





Page28: MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0] 1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT SOR0/1/2/3 ENABLE
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

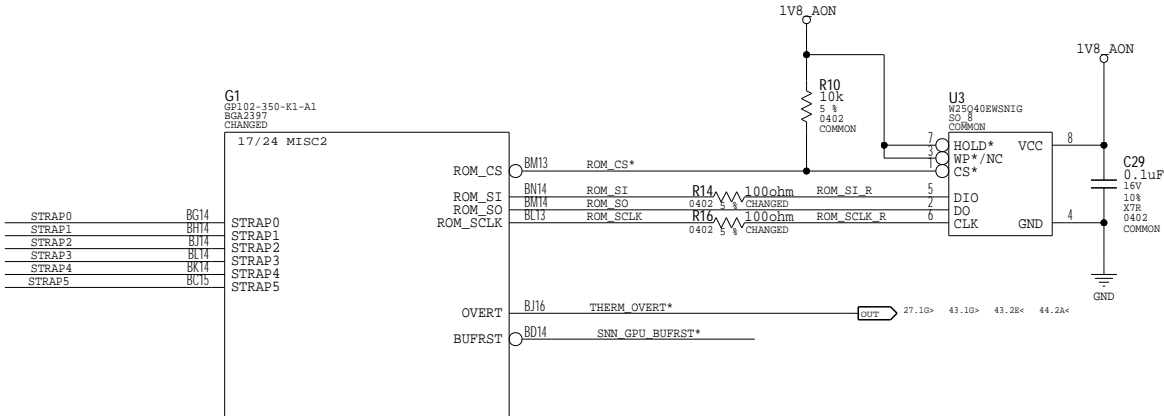
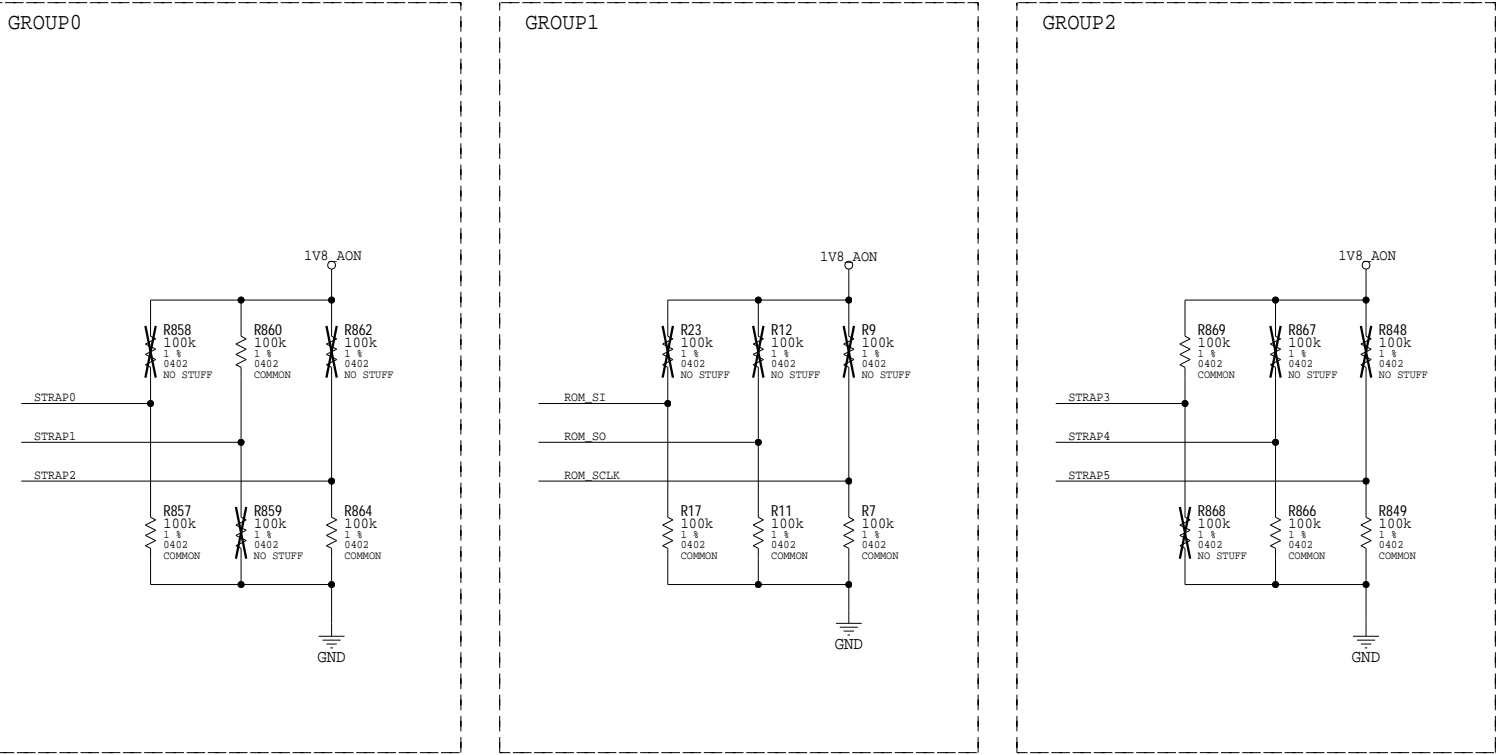
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



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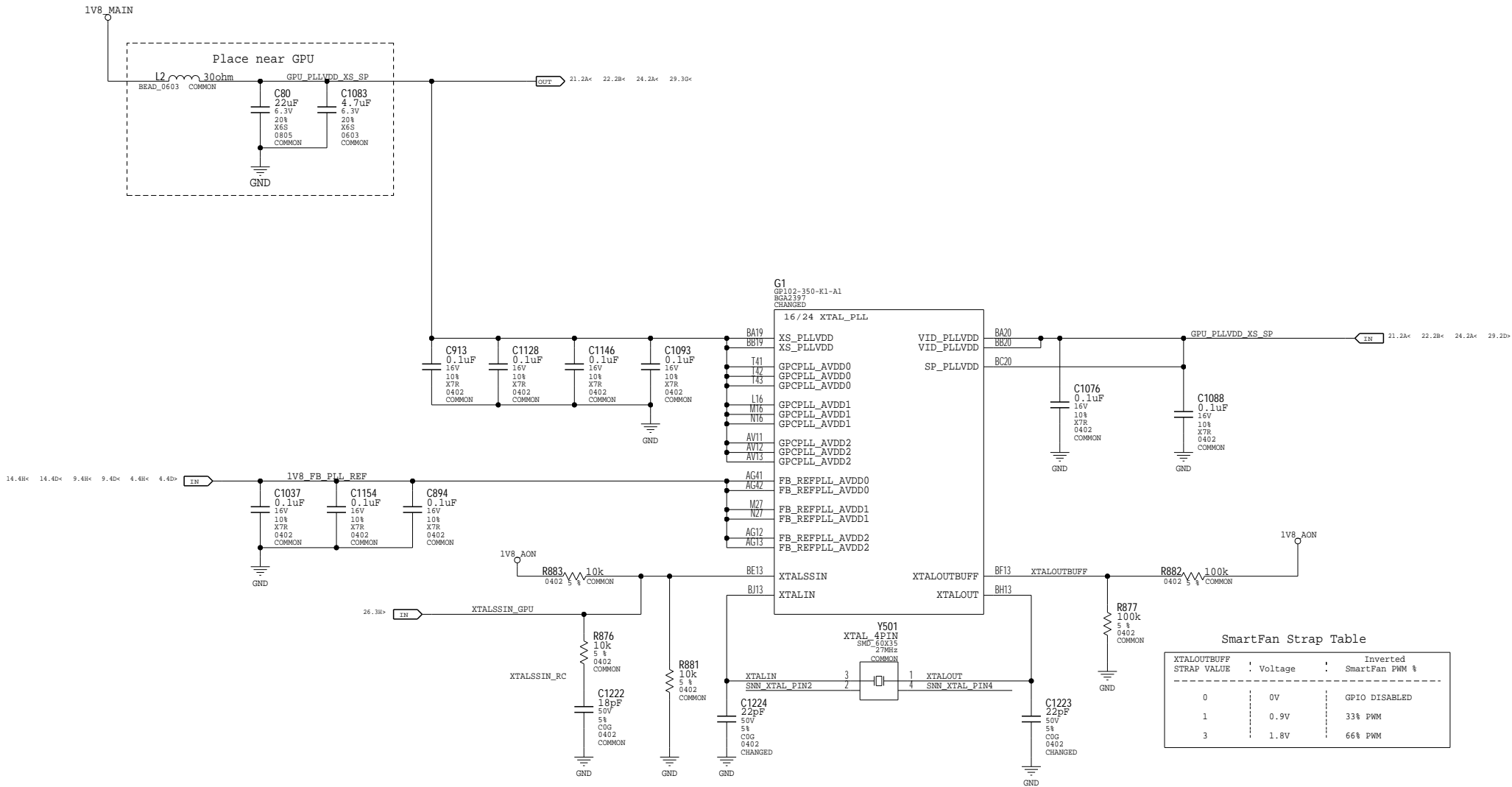
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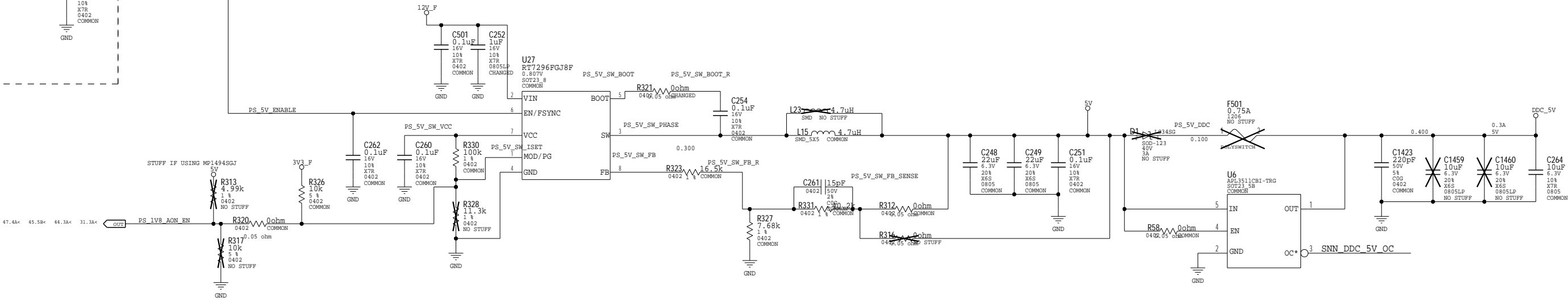
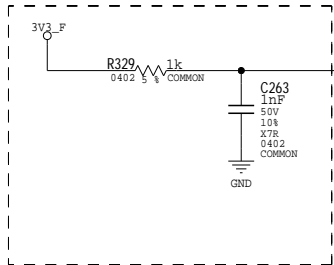
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PEX PLL Switcher

$$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$$
$$1.008 = 0.6 * (1 + 6.81K/10K)$$



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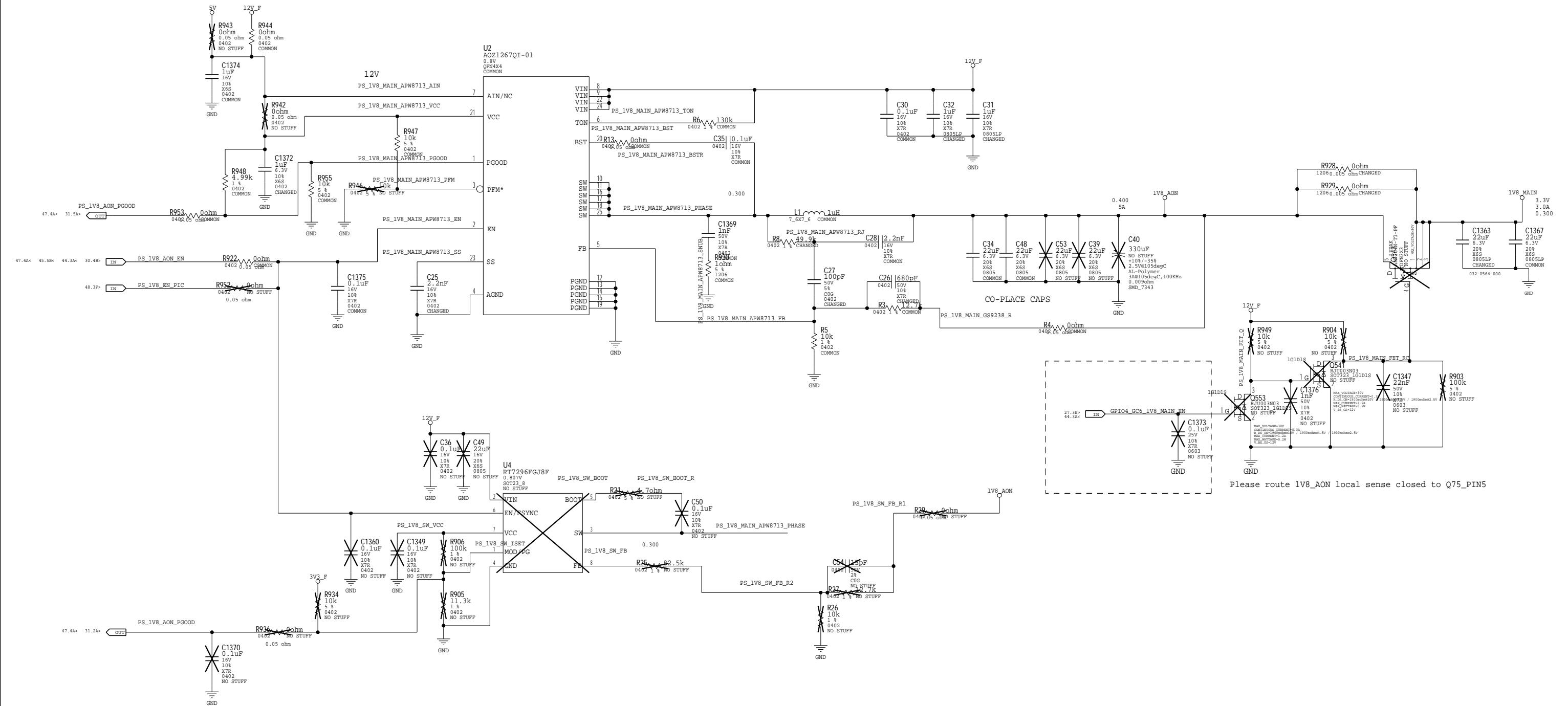
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Page31: PS: 1V8 Rails



$$1.8 = 0.8 * (1 + 18.7K/15K)$$
$$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$$

ASSEMBLY	SKU50
PAGE DETAIL	PS: 1v8 Rails

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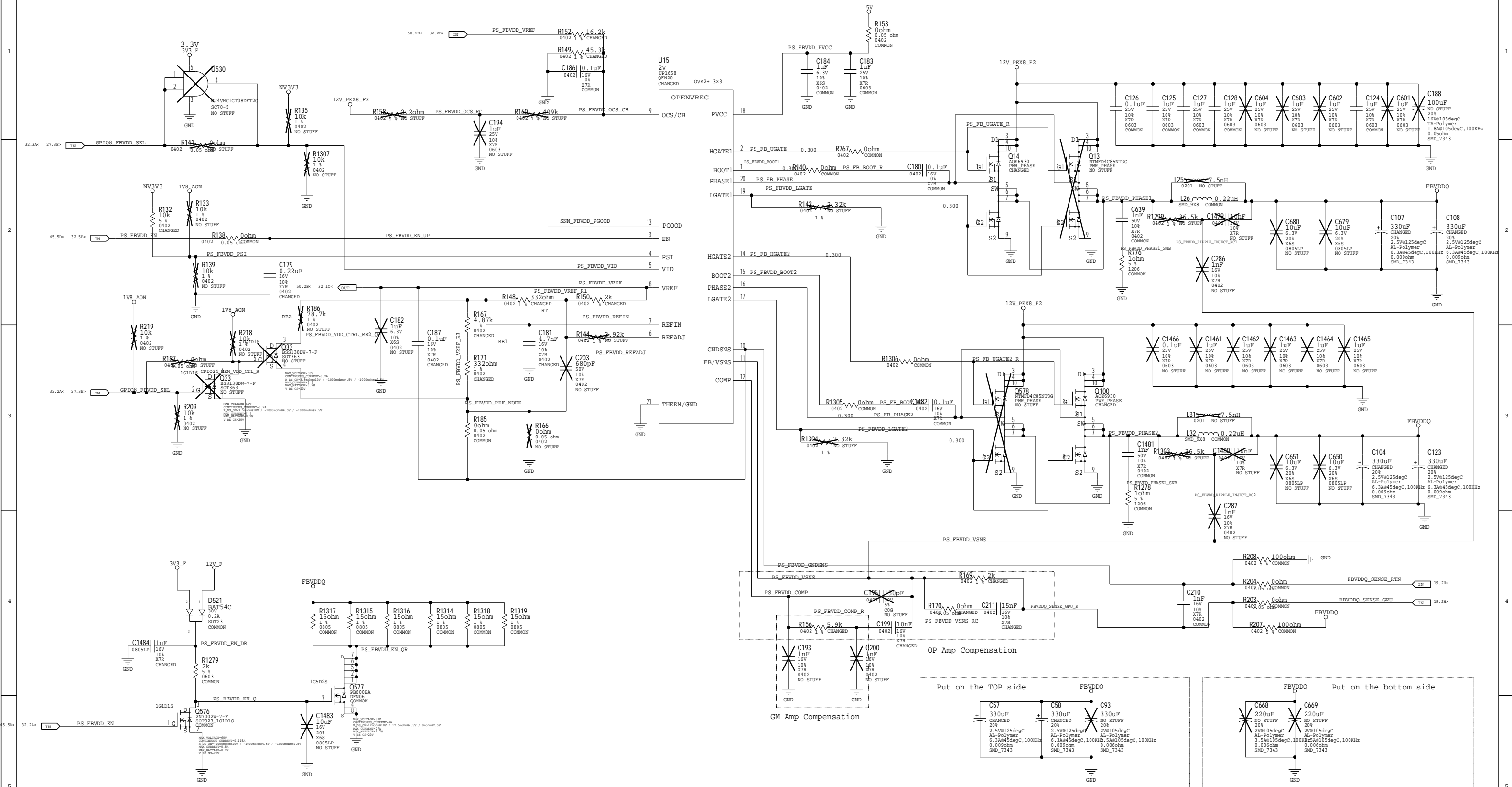
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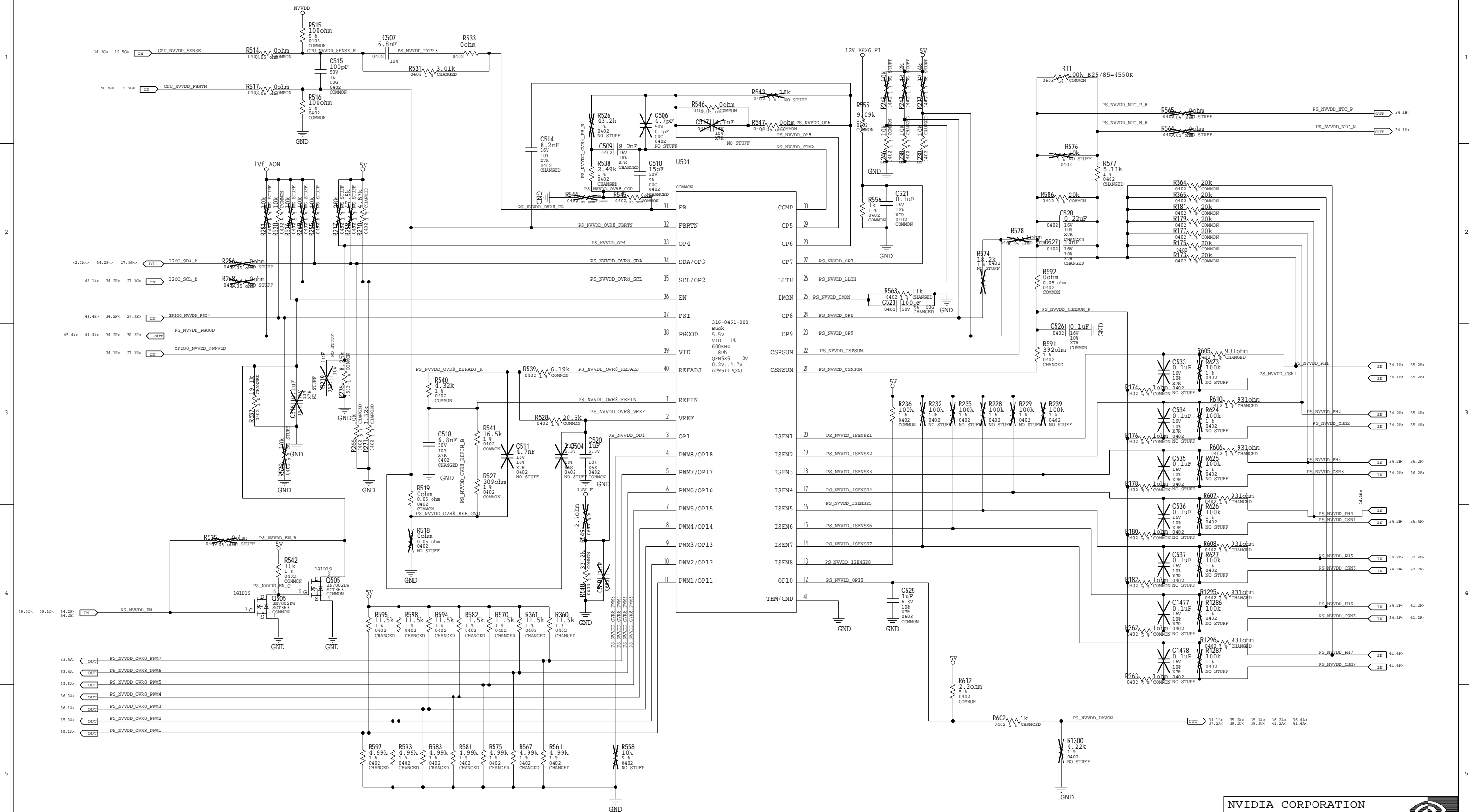


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PAGE DETAIL	PS: FBVDDQ

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Page33: PS: NVVDD Controller_OVR8



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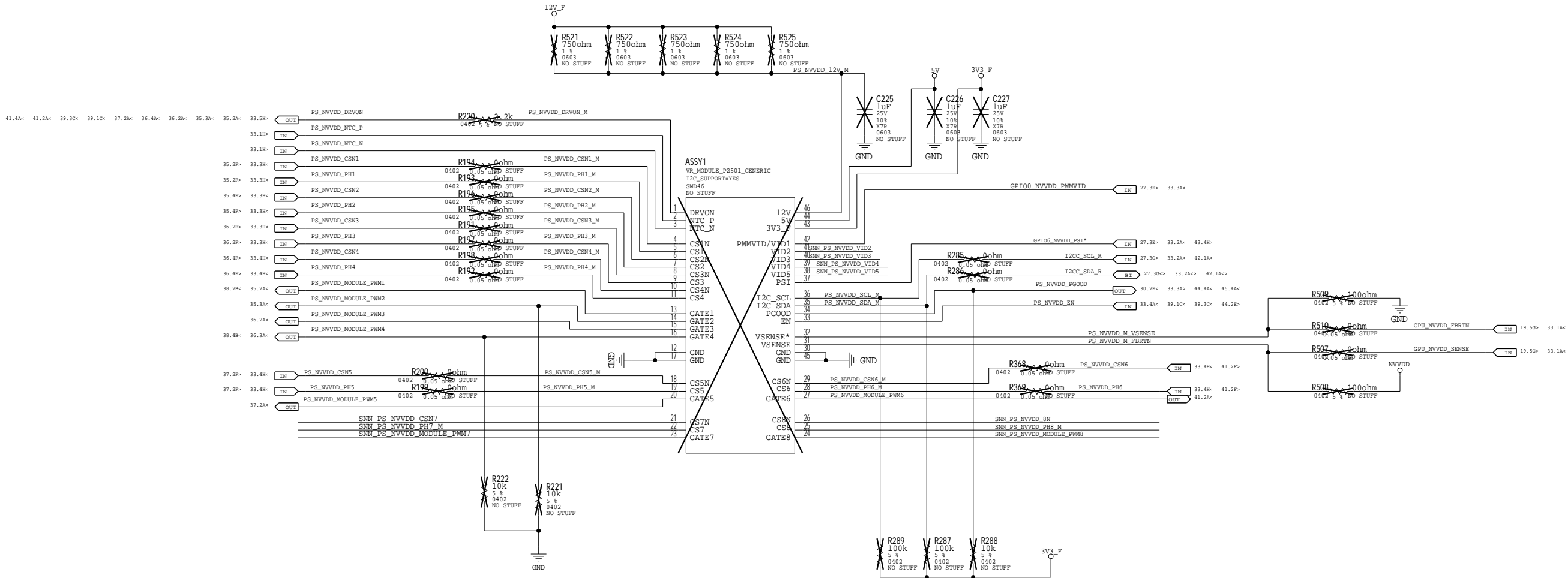
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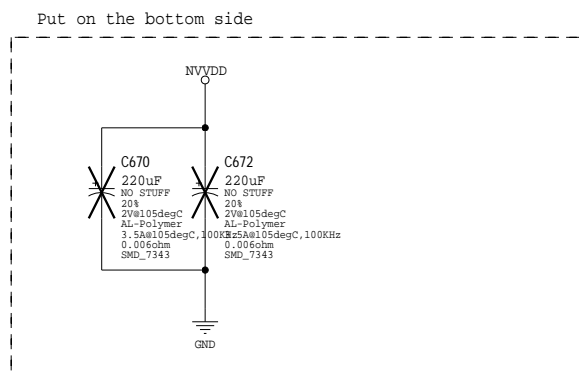
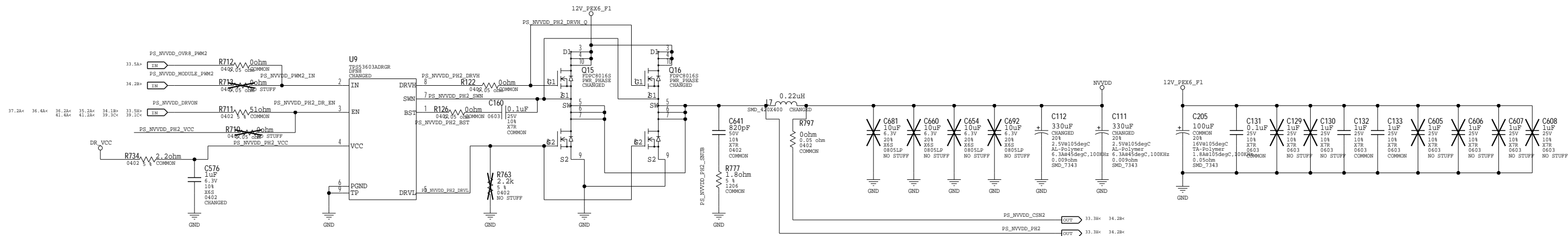
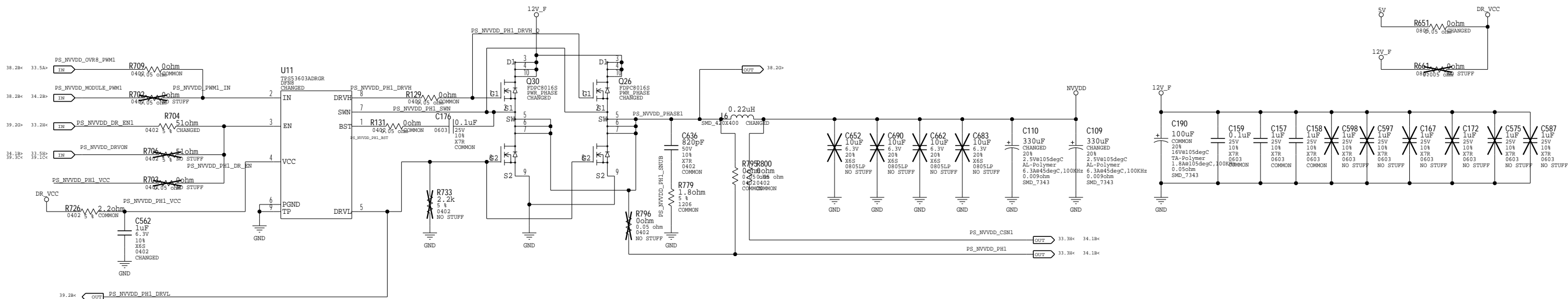
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PAGE DETAIL	PS: NVVDD Phase 1, 2

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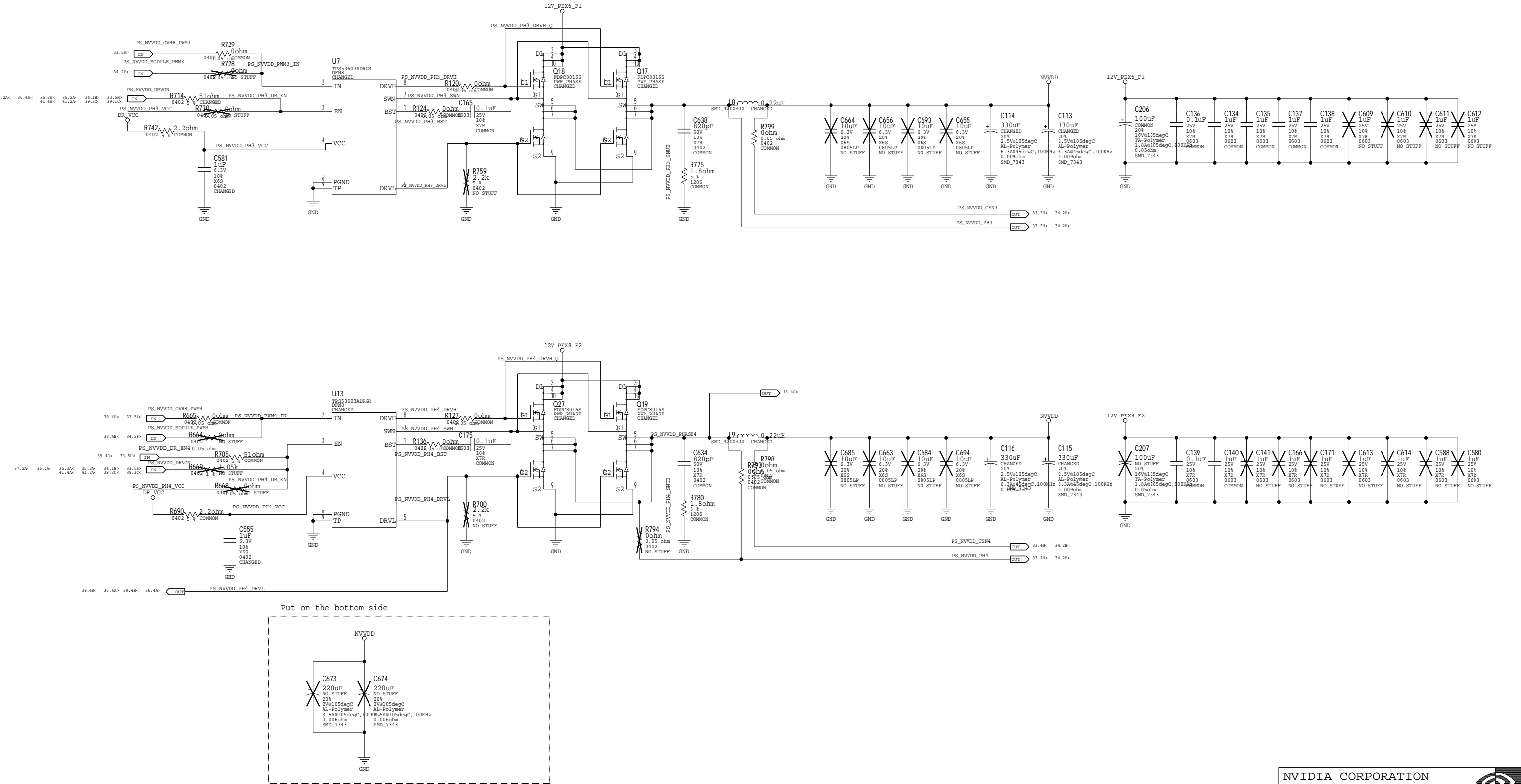
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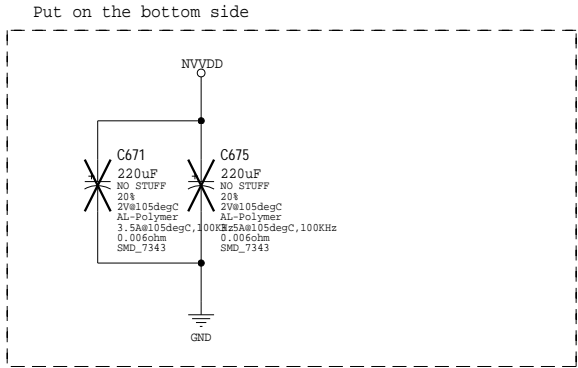
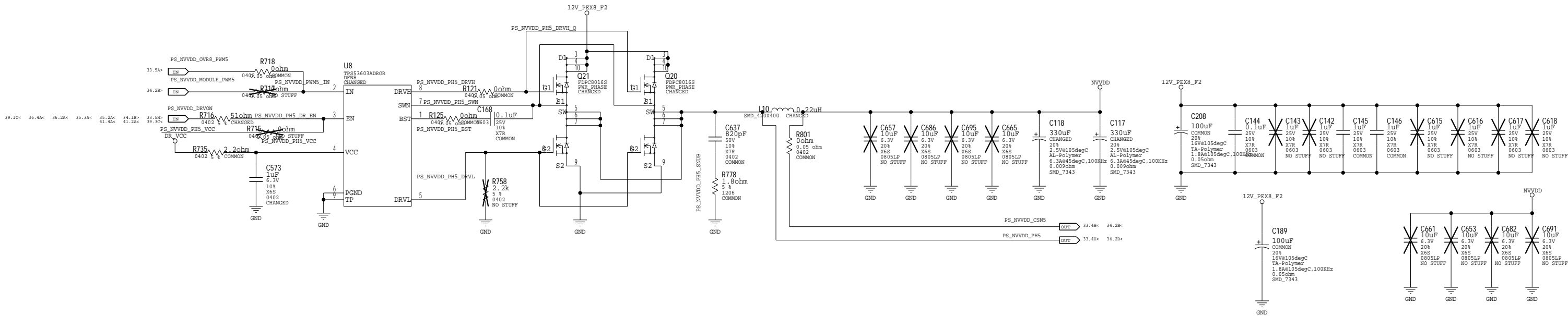
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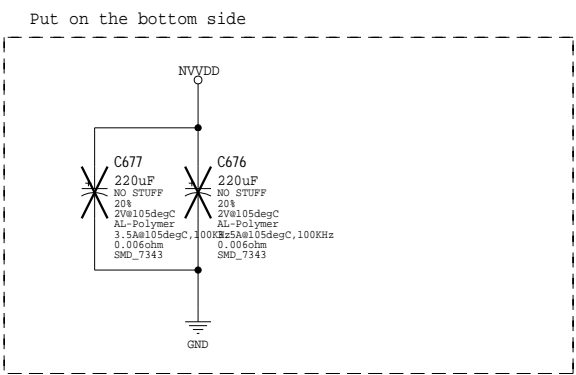
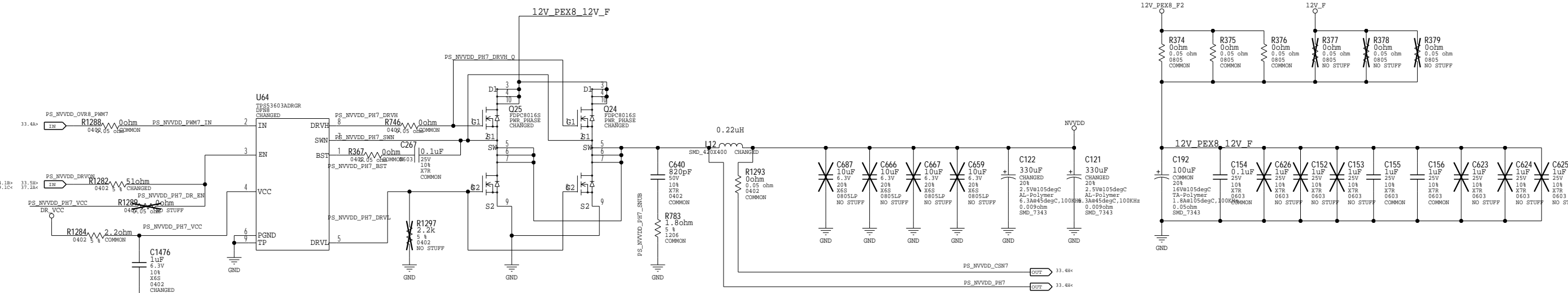
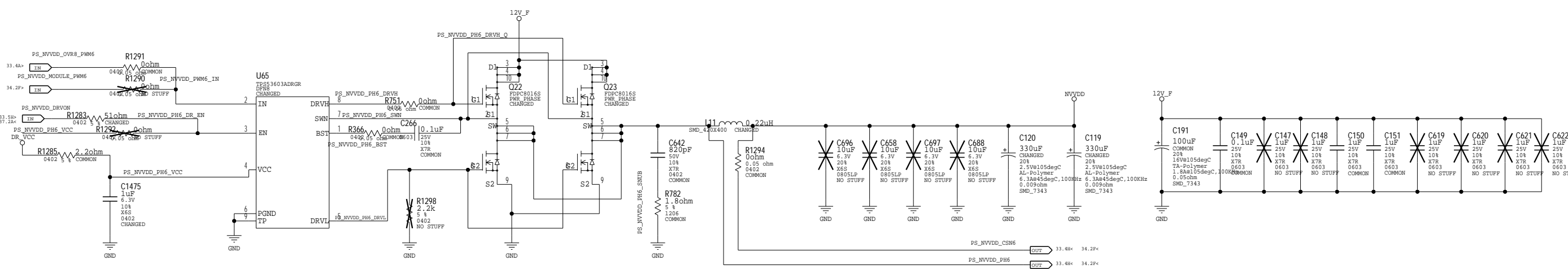
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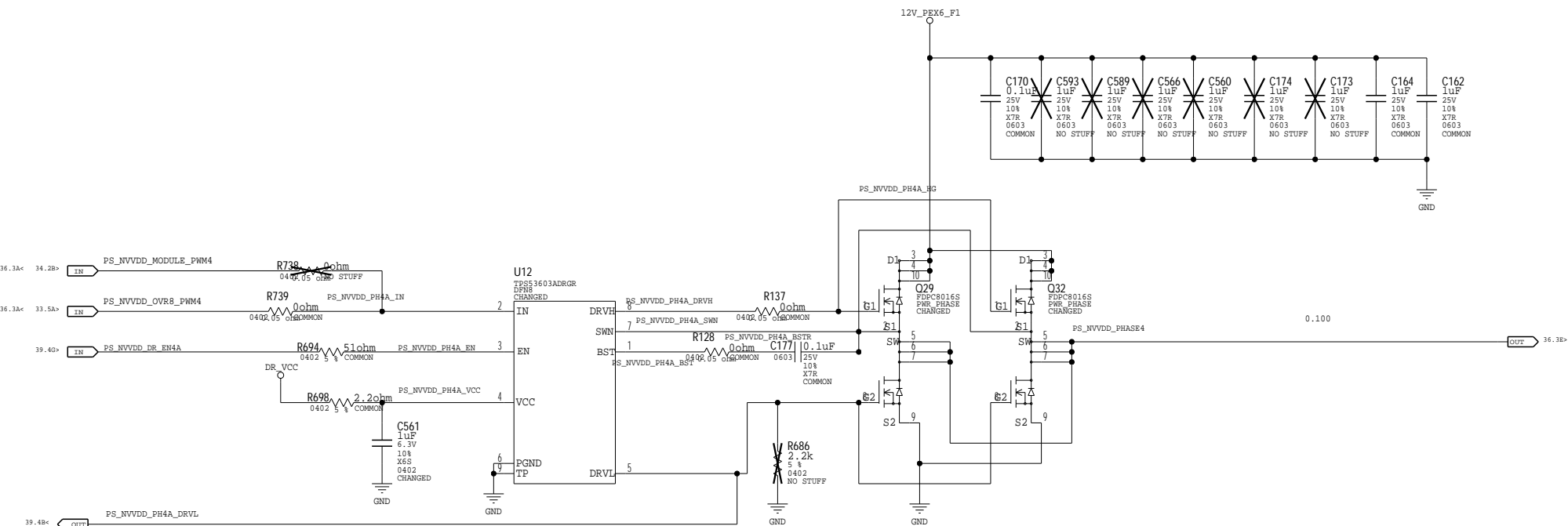
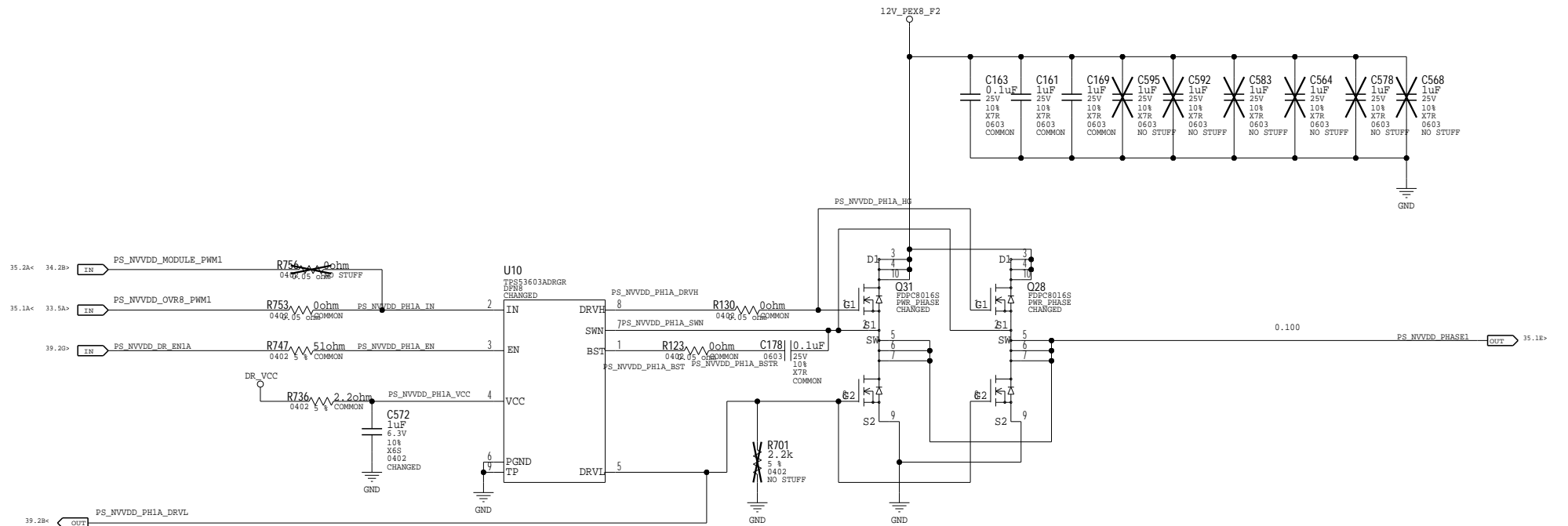
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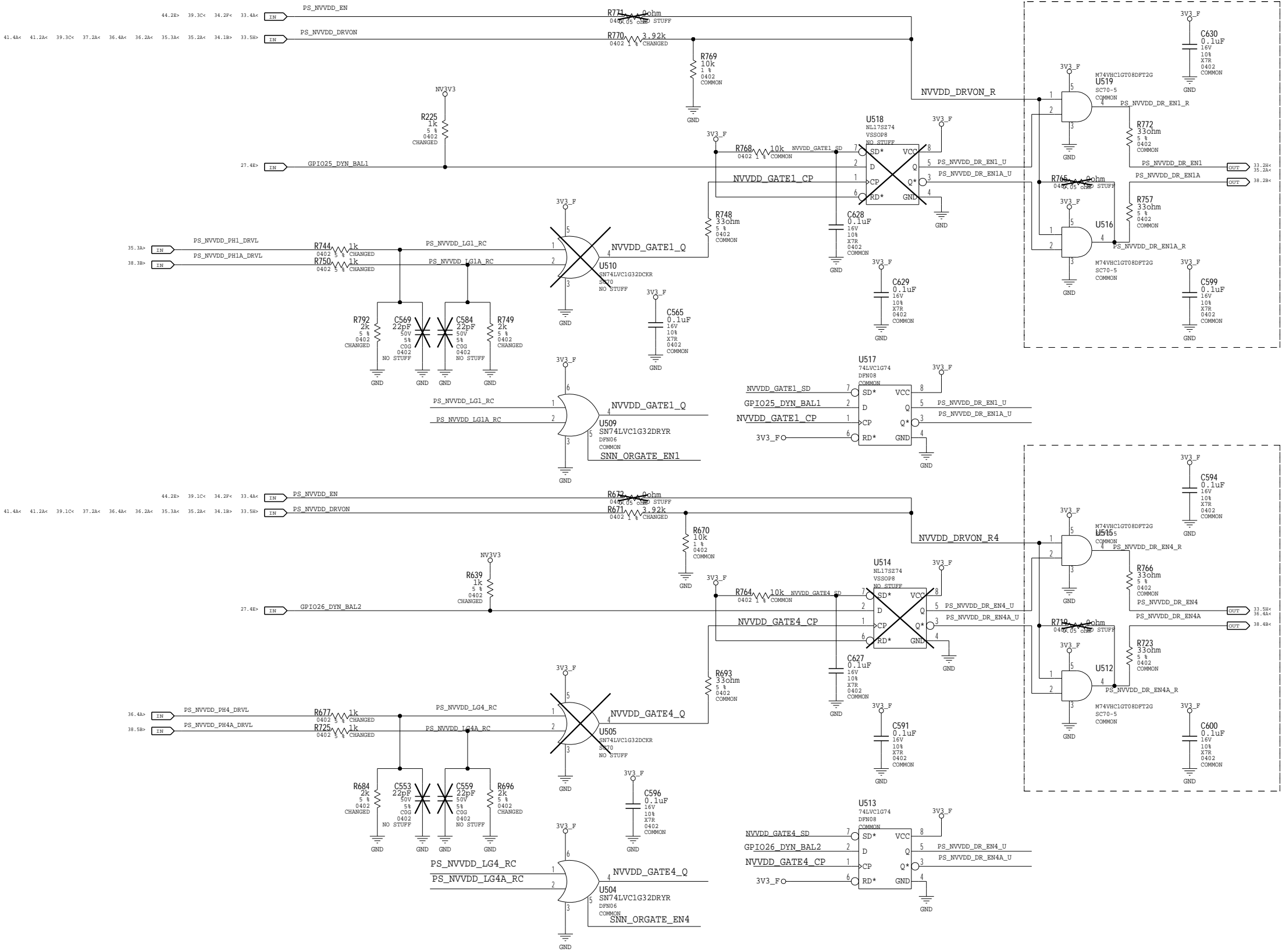
PCB REV PG611-A00

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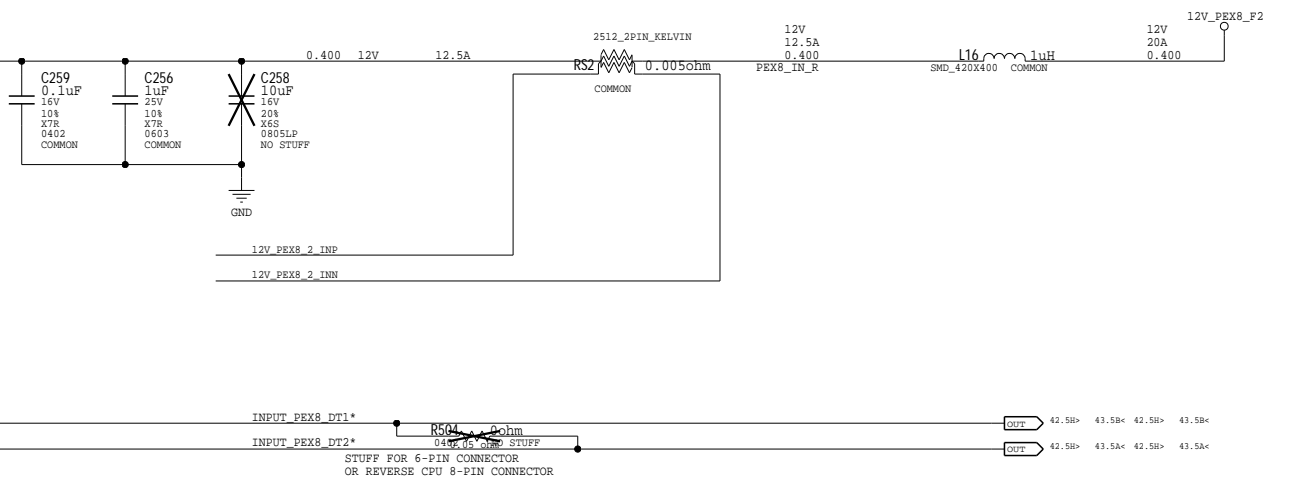
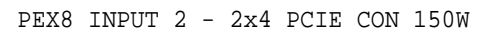
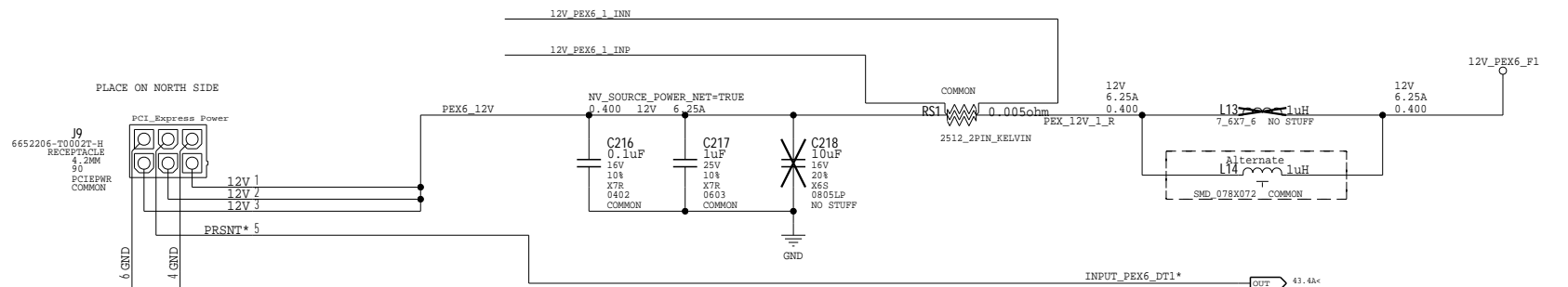
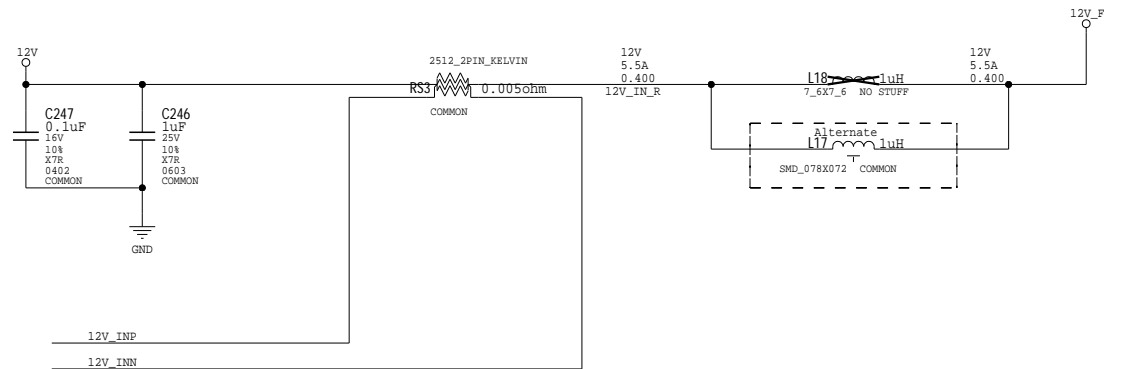
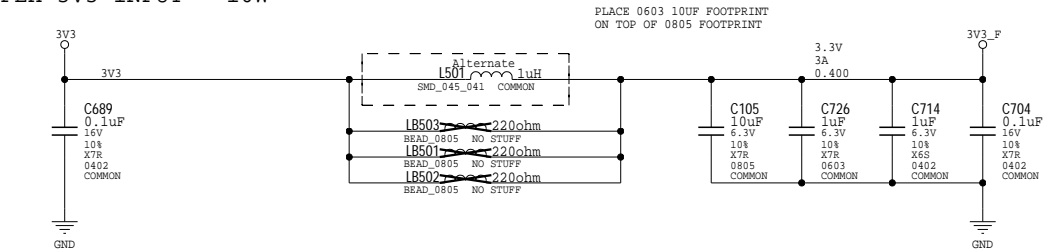
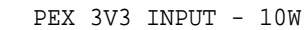
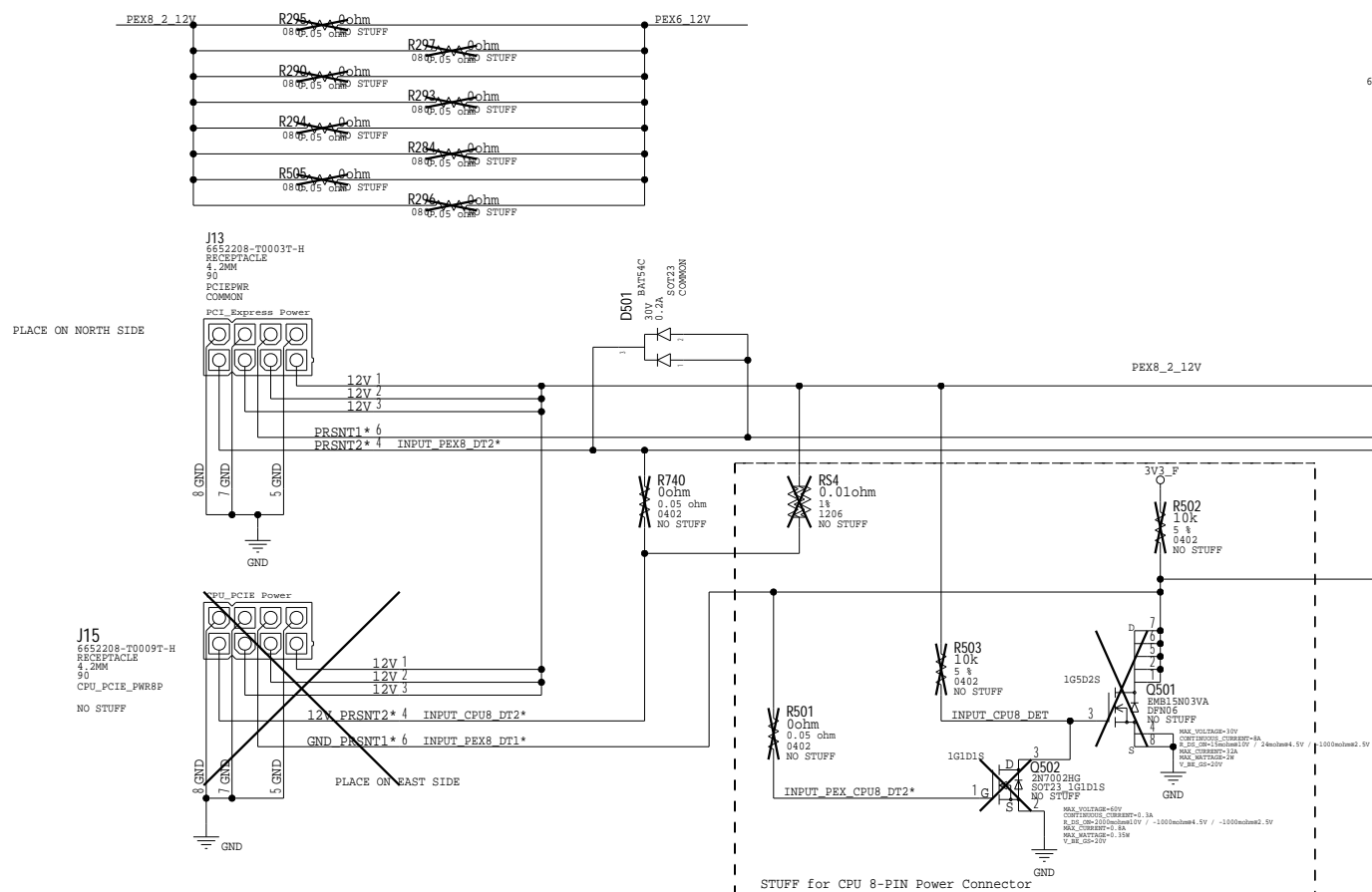
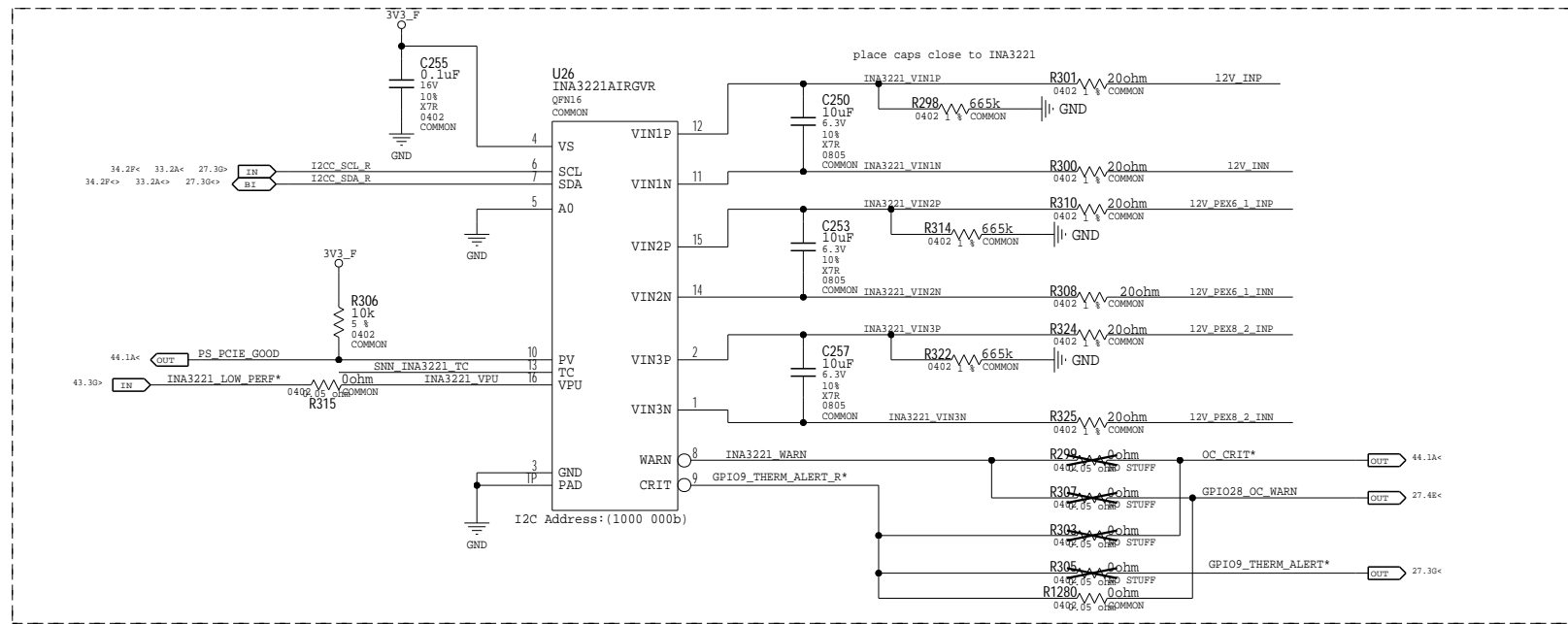
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DATE 15-FEB-2017

Page40: PS: Dynamic Power Balance Logic



Page41: PS: Inputs, Filtering, and Monitoring



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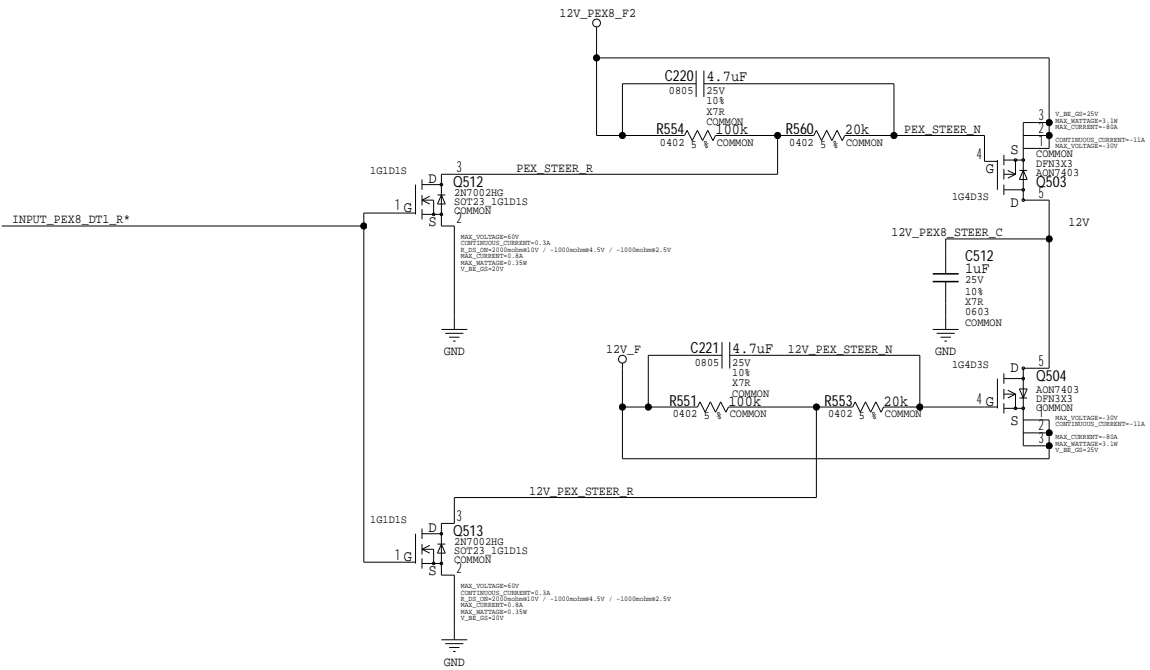
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Page42: PS: 12V Current Steering & Hot Unplug Detect

QUADRO/TESLA:

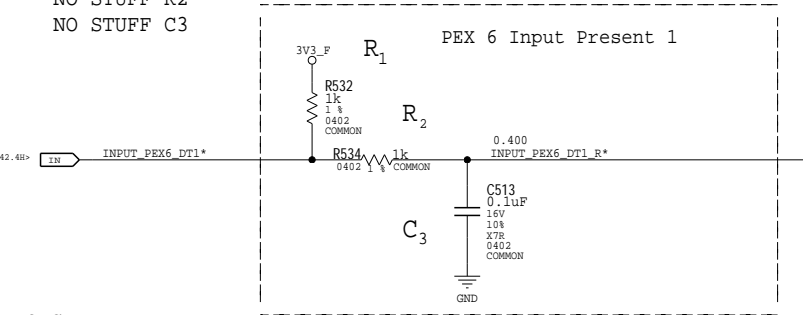
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



PEX 6 INPUT CONNECTOR IS NOT LOADED
PEX 6 INPUT DETECT MUST BE DISABLED
PEX 8 INPUT DETECT MUST BE USED TO CONTROL STEERING

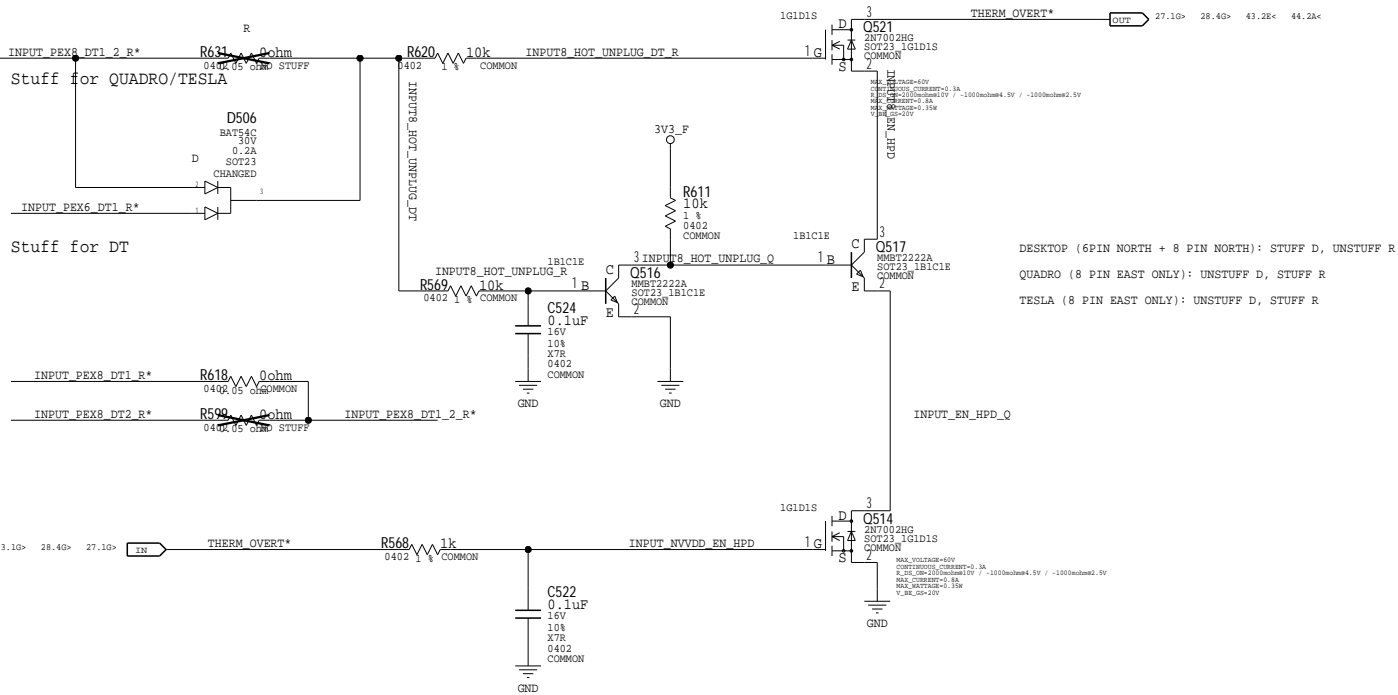
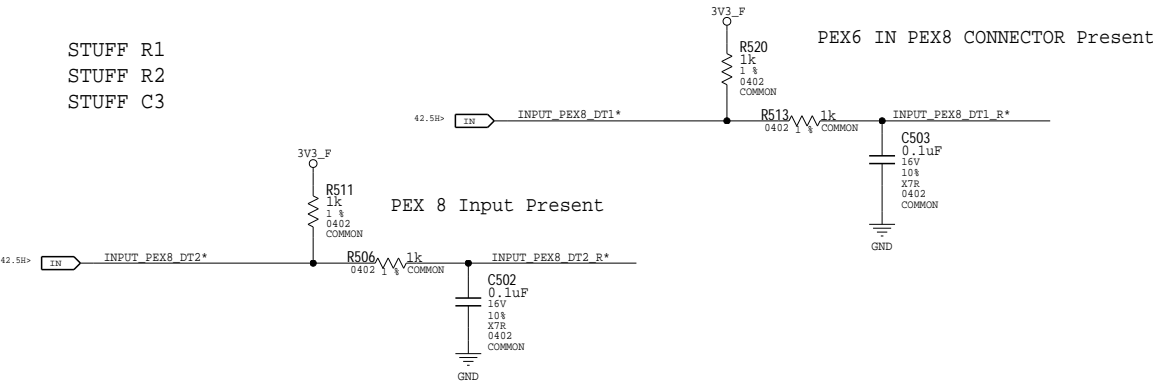
NO STUFF R1
NO STUFF R2
NO STUFF C3



GeFORCE:

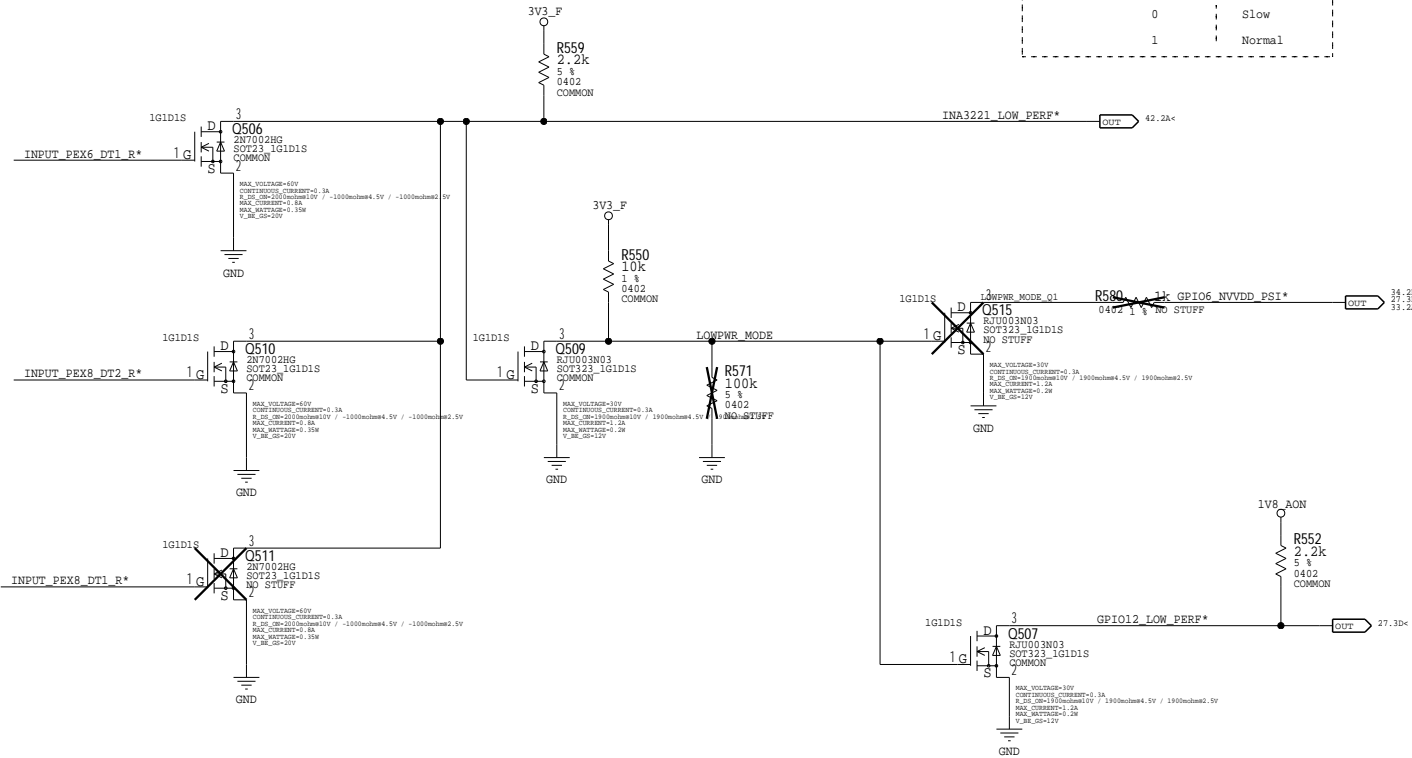
PEX 6 INPUT CONNECTOR IS LOADED
PEX 6 INPUT DETECT MUST BE USED TO CONTROL STEERING

STUFF R1
STUFF R2
STUFF C3



DESKTOP (6PIN NORTH + 8 PIN NORTH): STUFF D, UNSTUFF R
QUADRO (8 PIN EAST ONLY): UNSTUFF D, STUFF R
TESLA (8 PIN EAST ONLY): UNSTUFF D, STUFF R

PEX Input - Under Power Boot Controls



A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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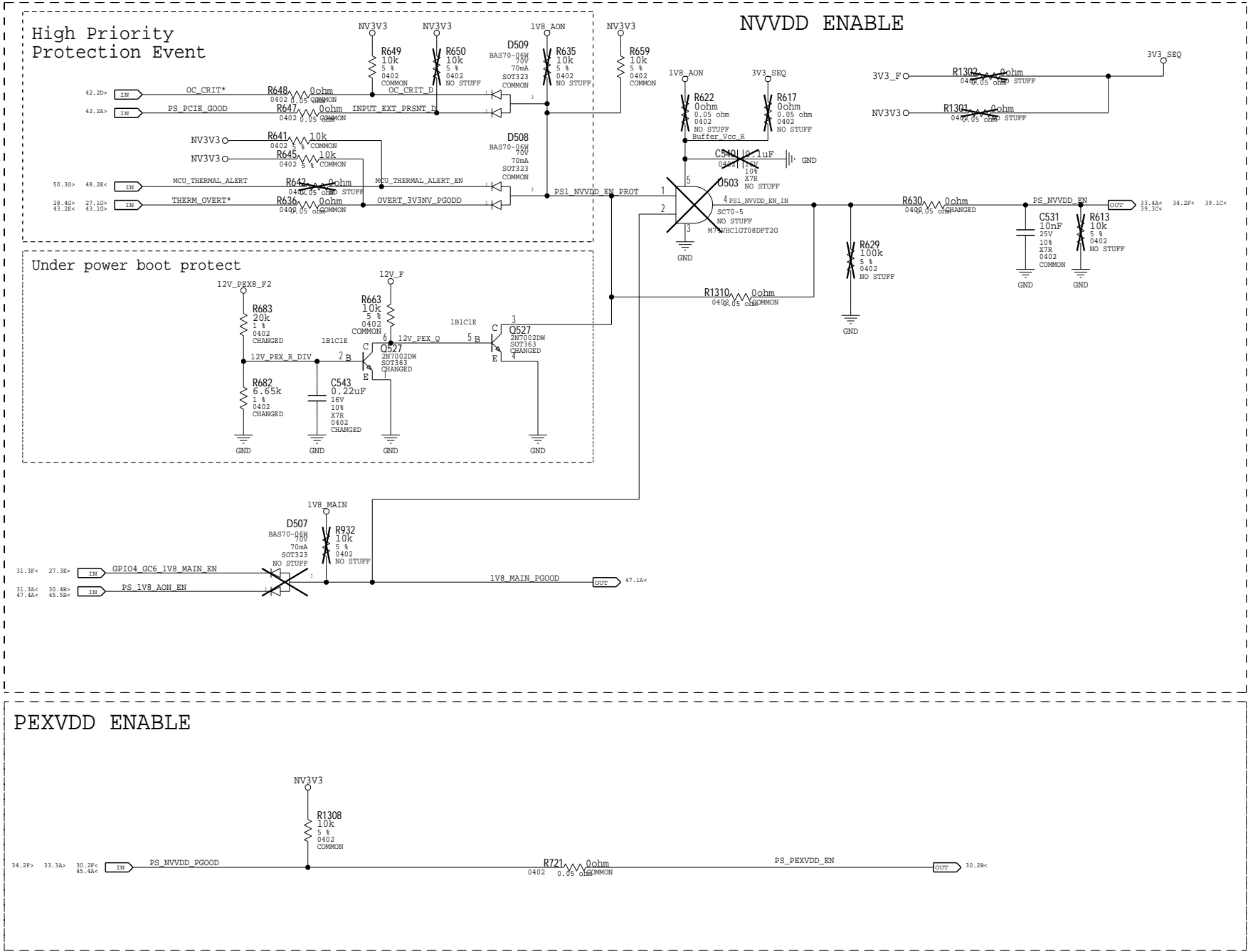
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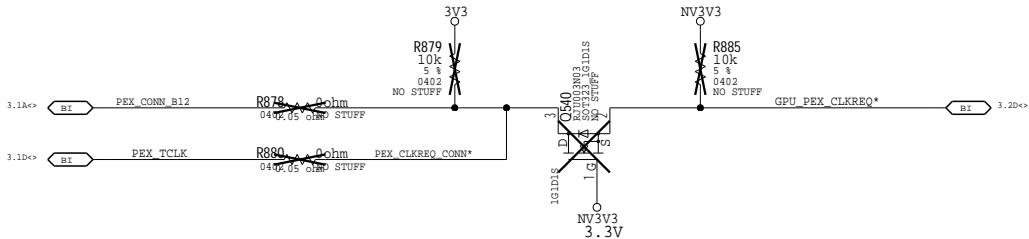
BOM REV A

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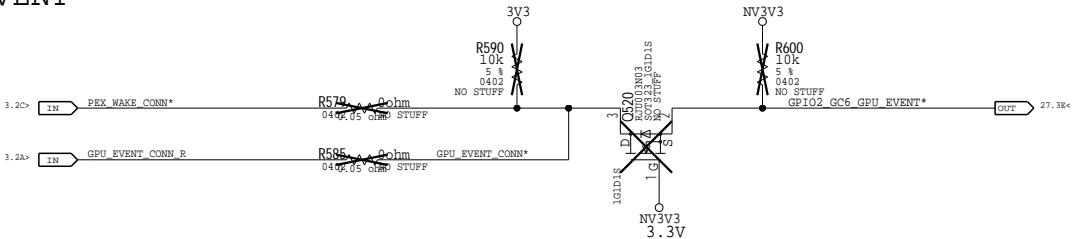
DATE 15-FEB-2017



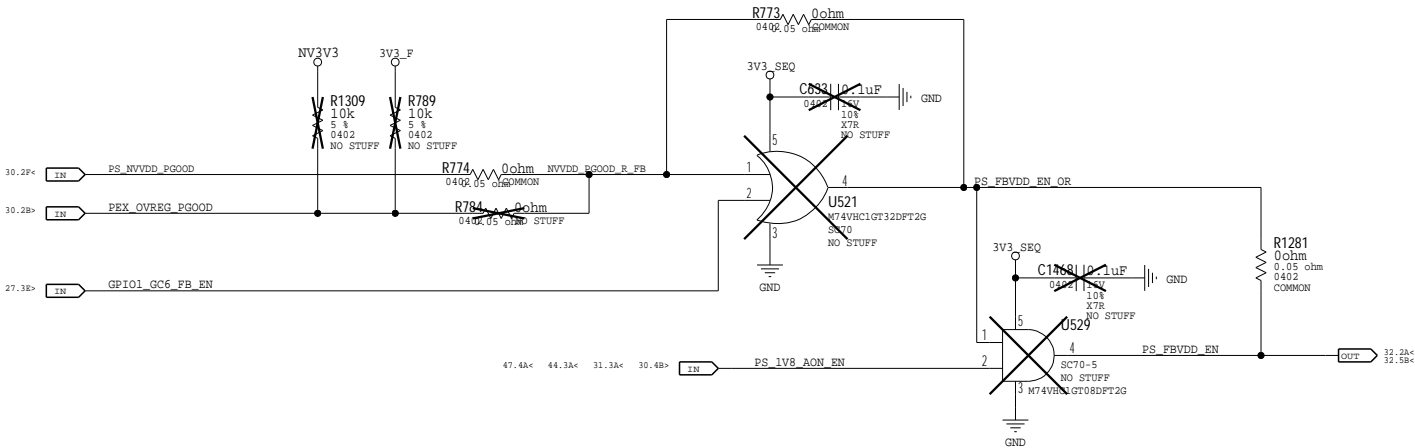
PEX_CLKREQ*



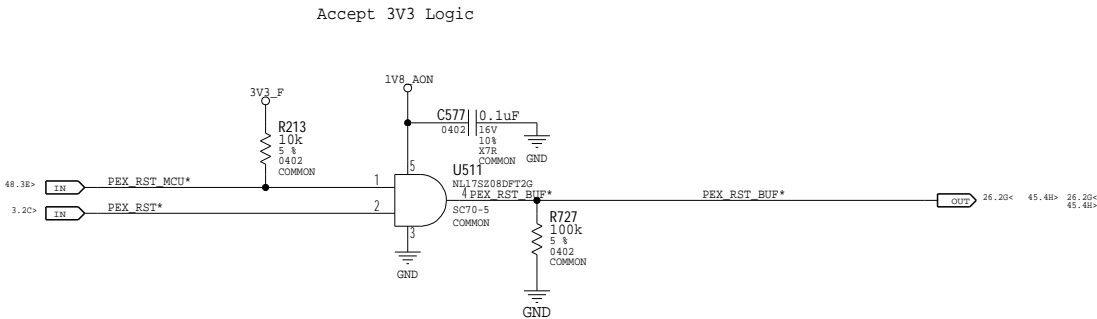
GPU_EVENT*



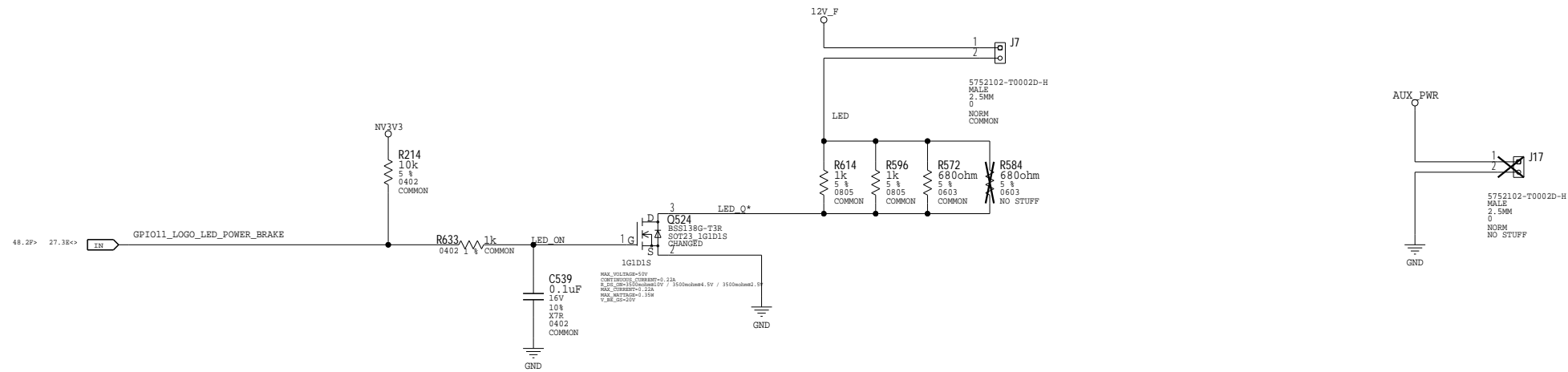
FBVDD/Q ENABLE



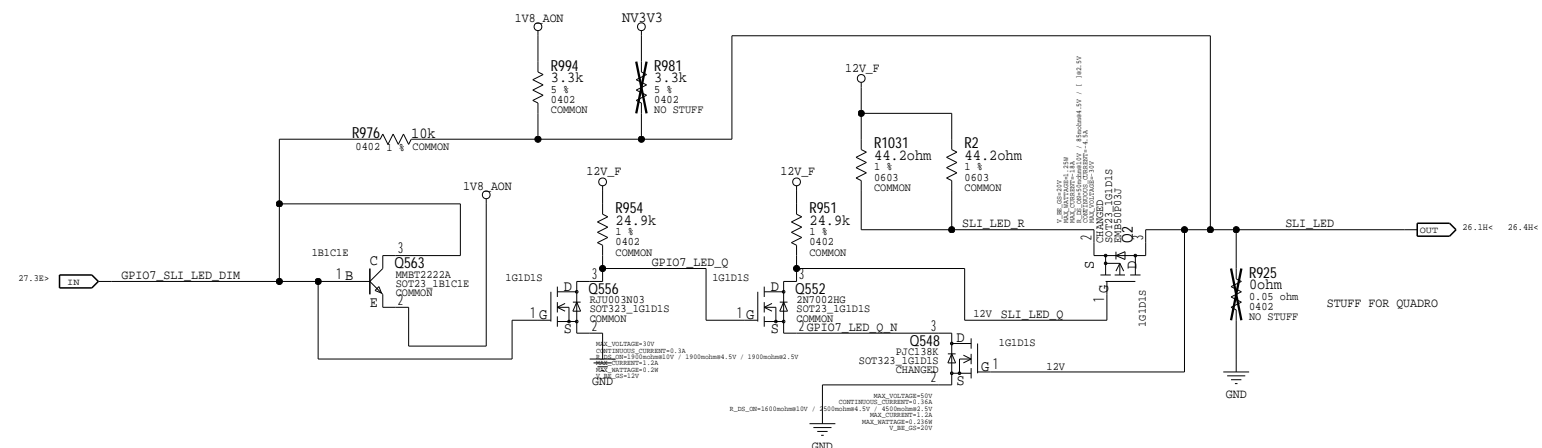
PEX_RST# LOGIC




LED HEADER (GEFORCE ONLY)

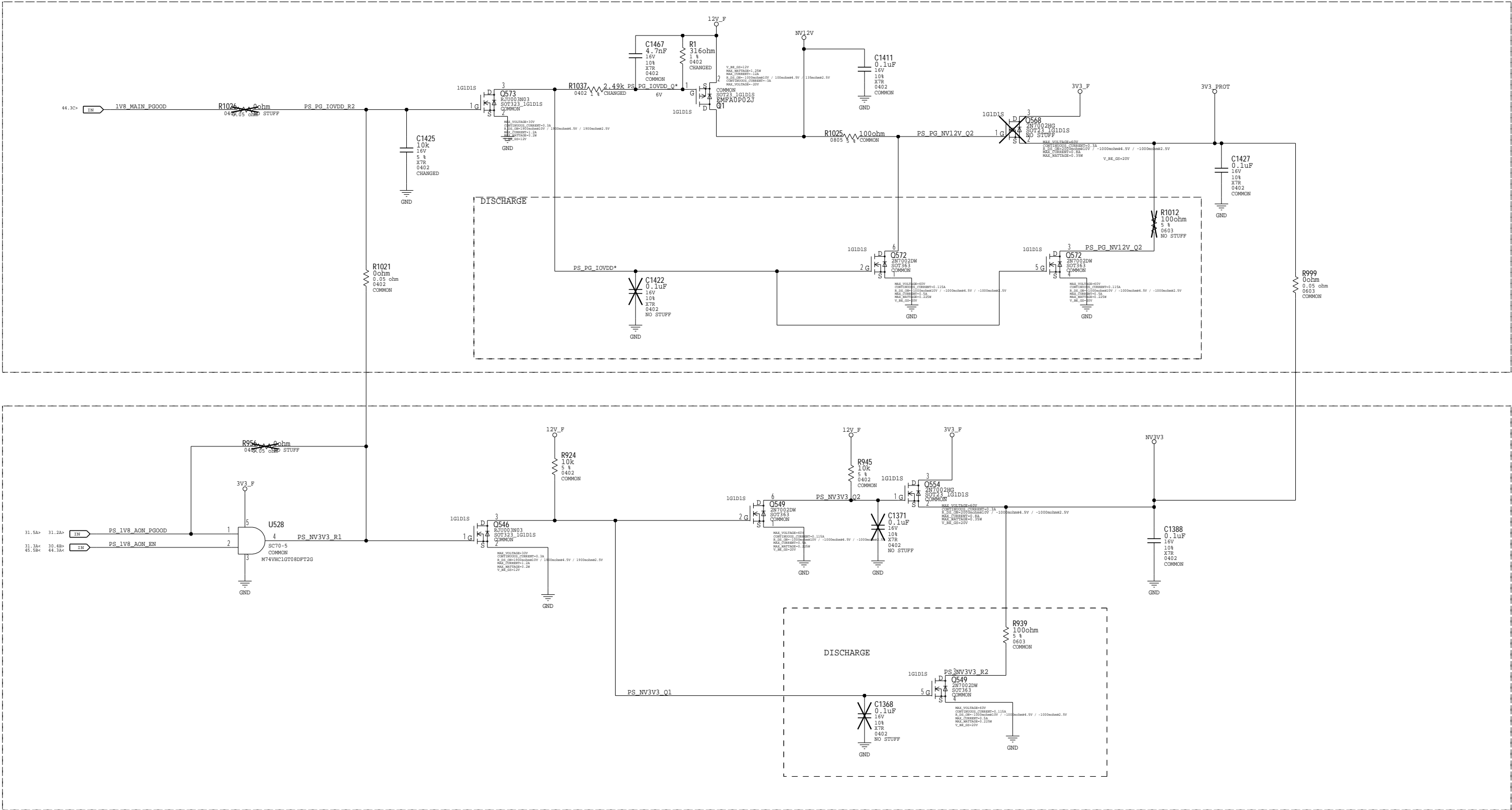


SLI LED (GEFORCE ONLY)



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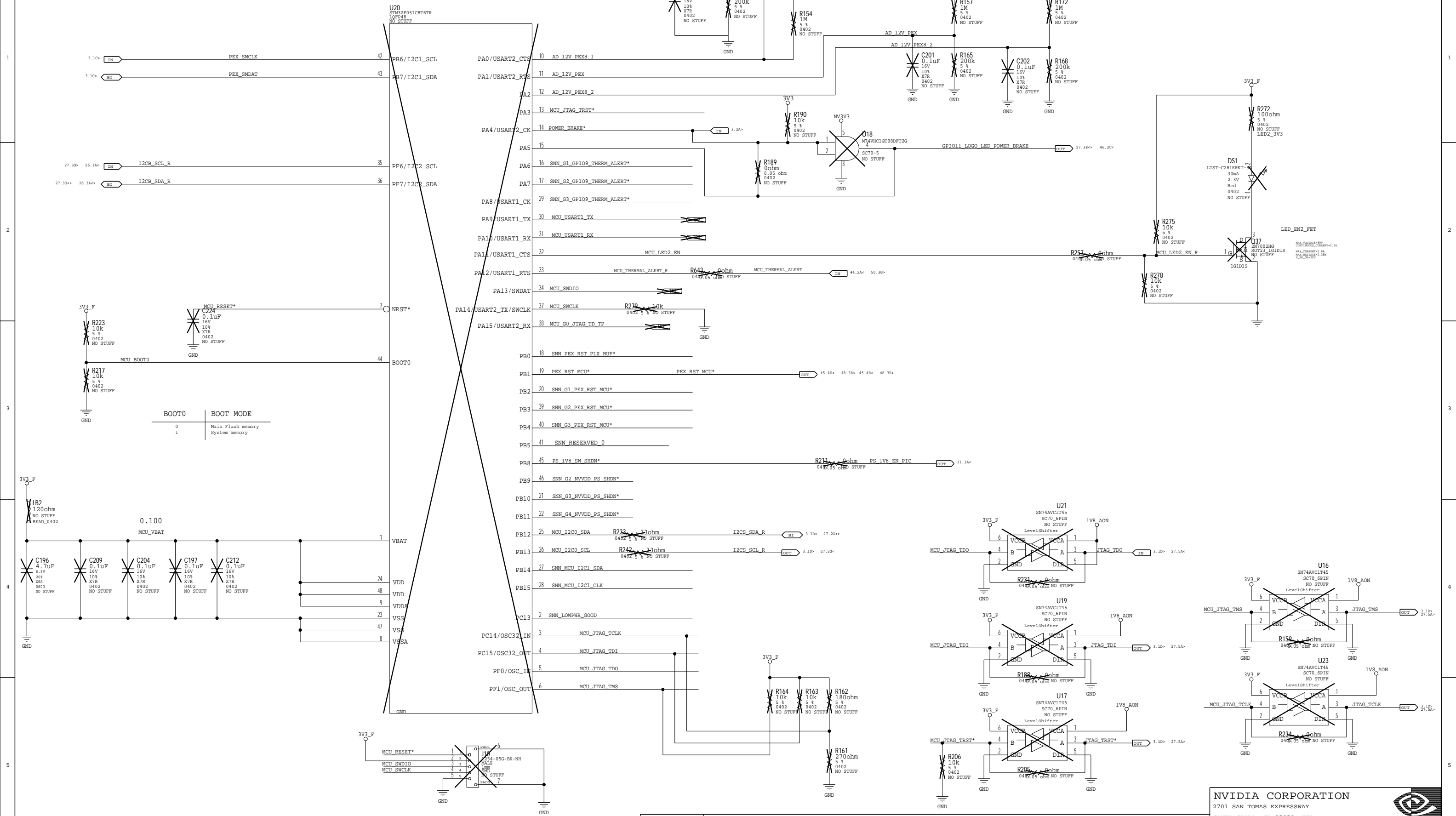
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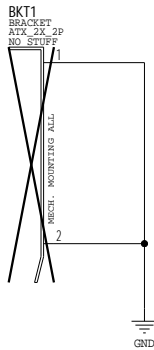
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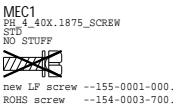
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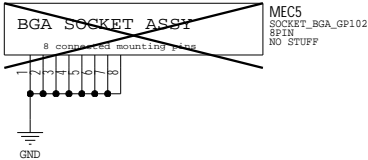
Brackets:



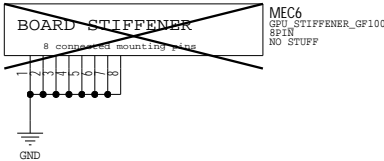
Bracket Screw



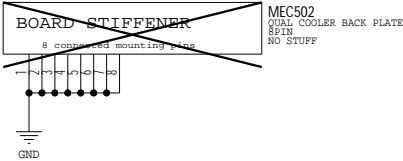
GPU SOCKET



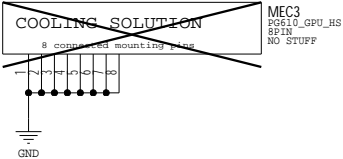
GPU Stiffener (BRING-UP COOLER)



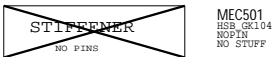
QUAL COOLER STIFFENER



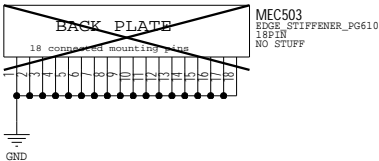
GPU HEATLINK



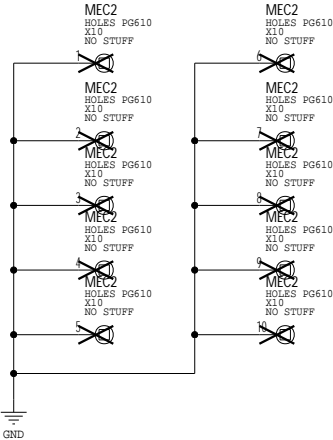
STIFFENER



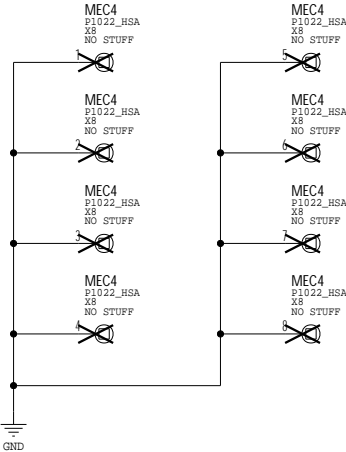
BOARD BACK PLATE

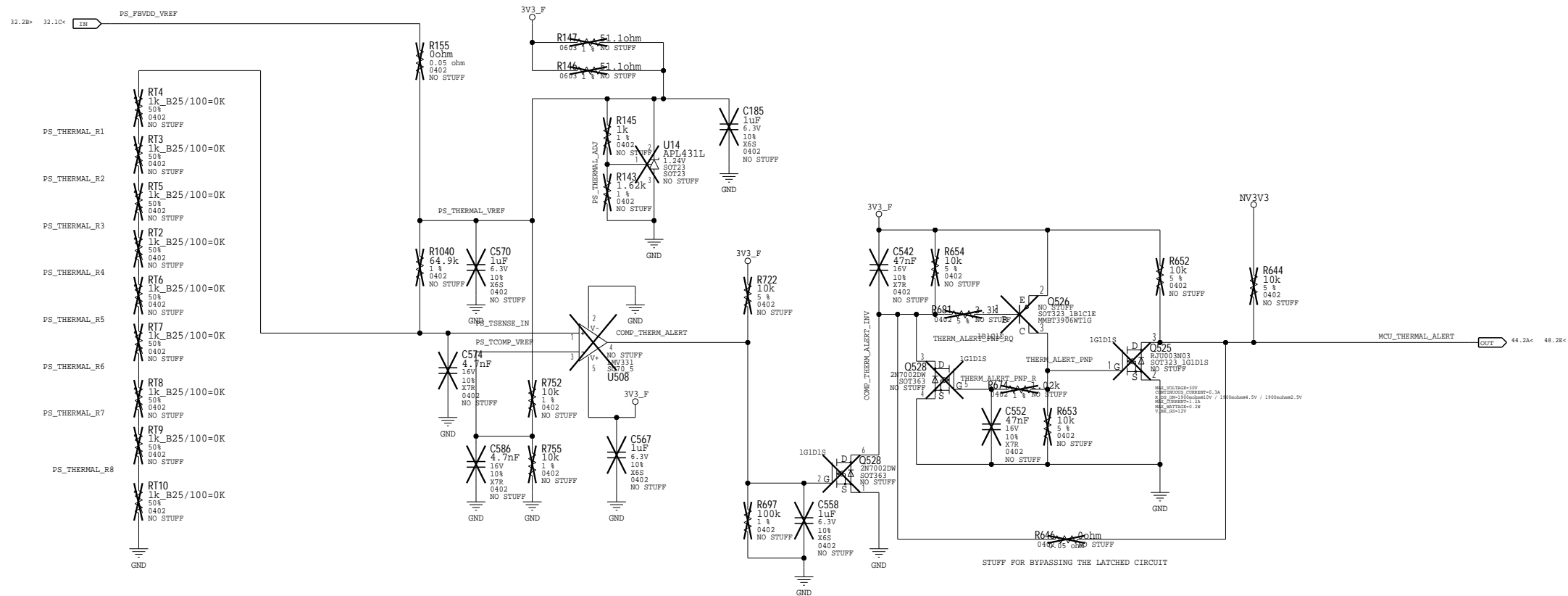


Mechanical Holes Symbol



GPU HOLES SYMBOL





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