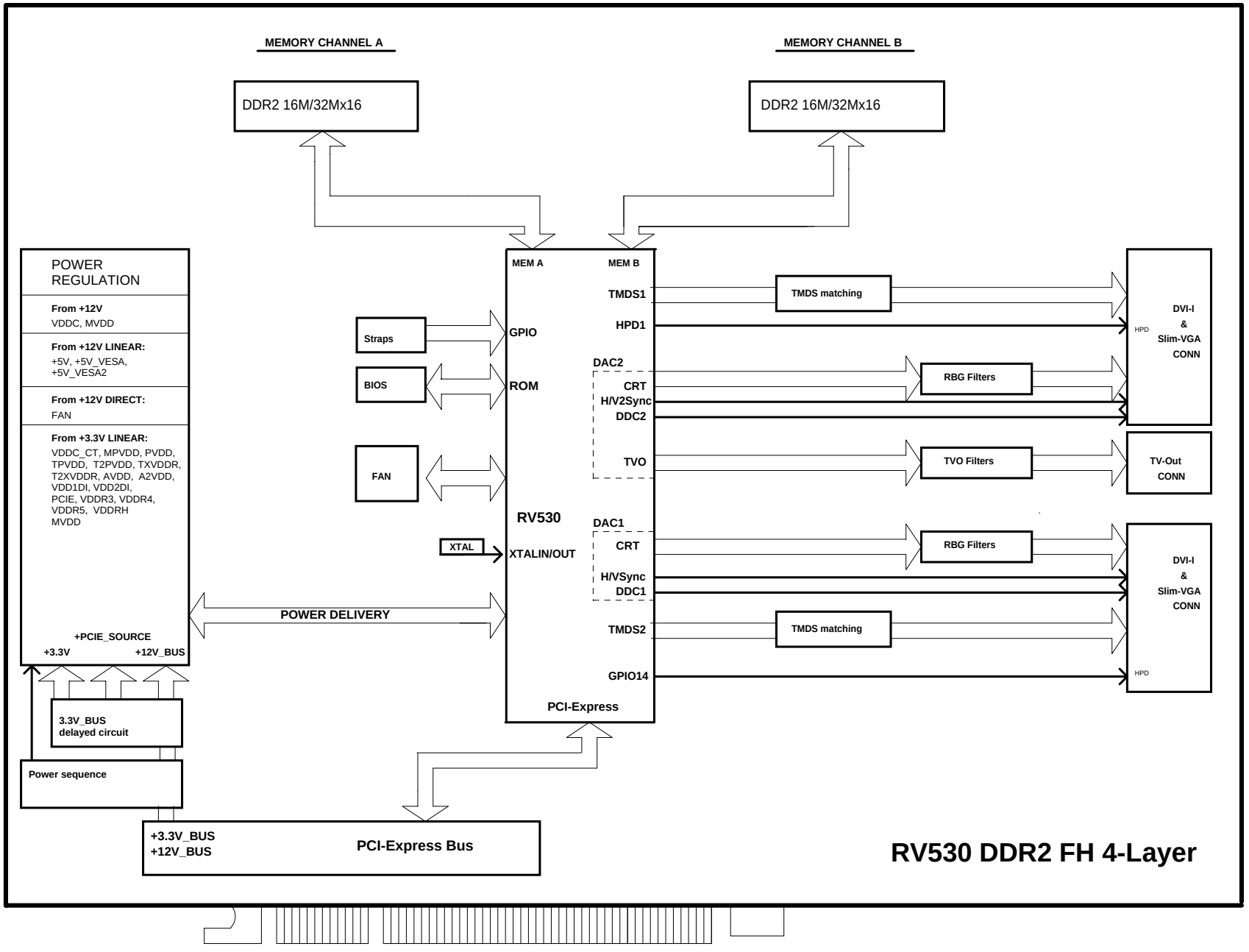

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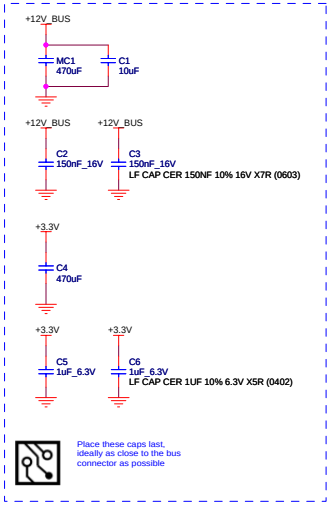
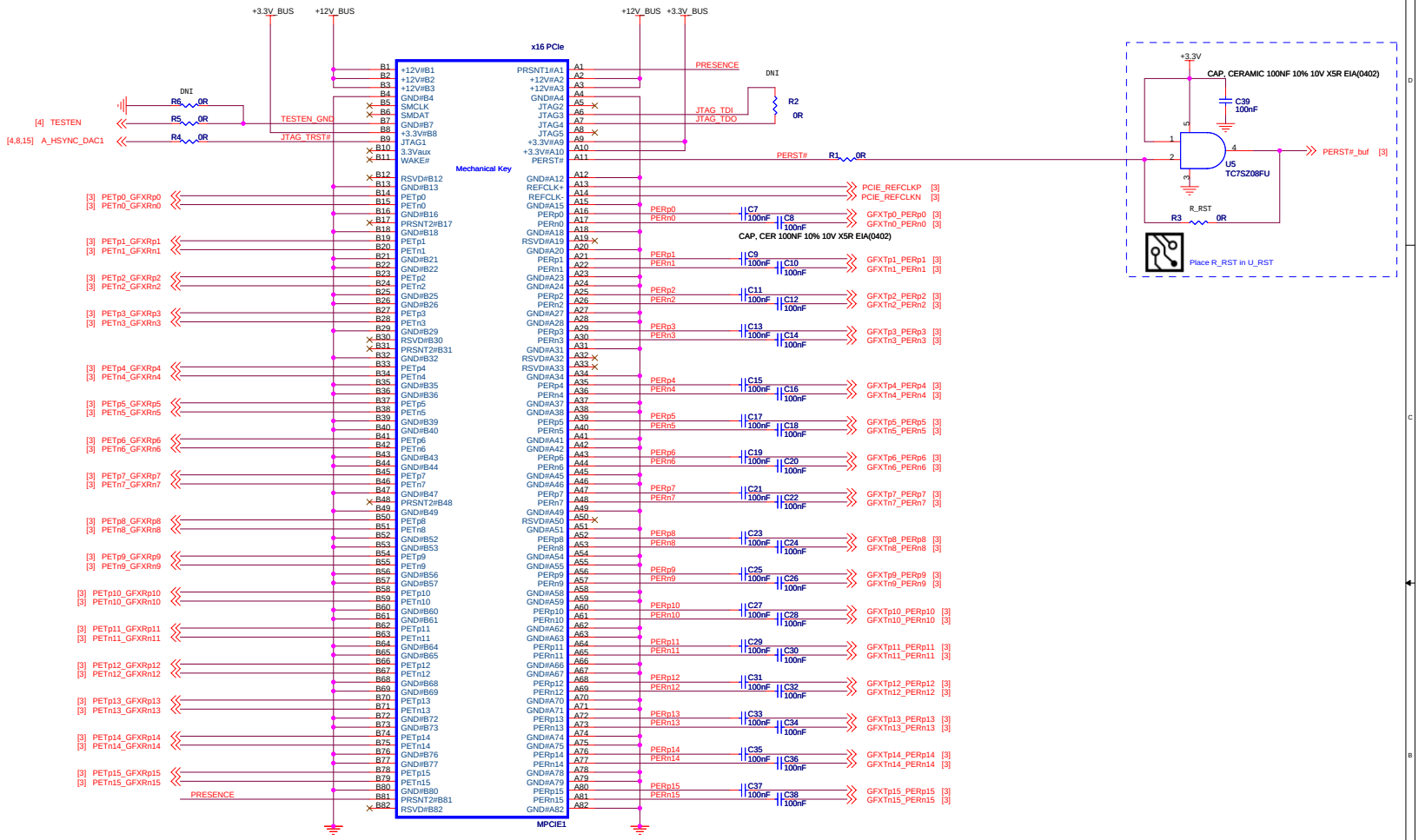
PCI-EXPRESS EDGE CONNECTOR





Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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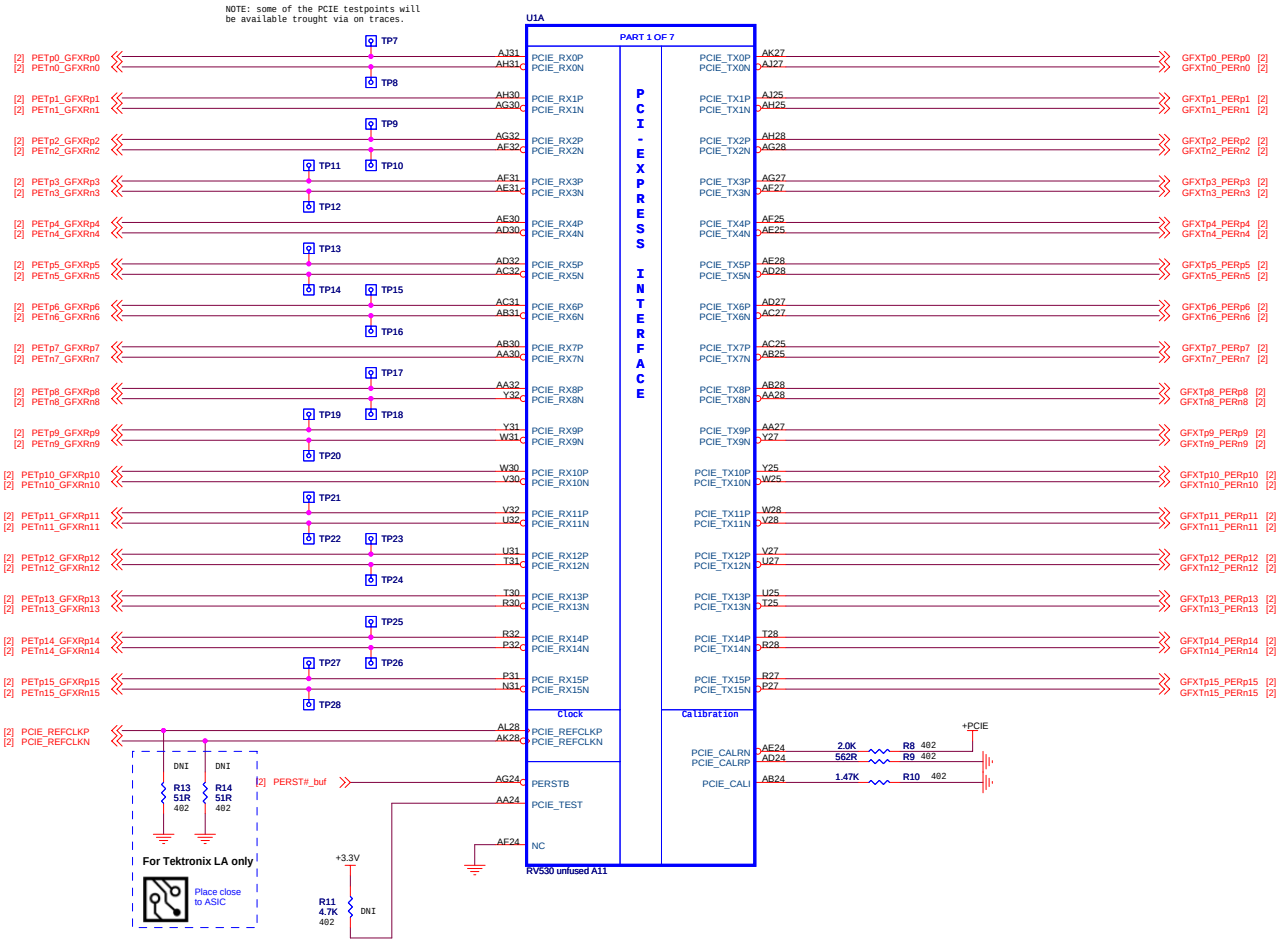

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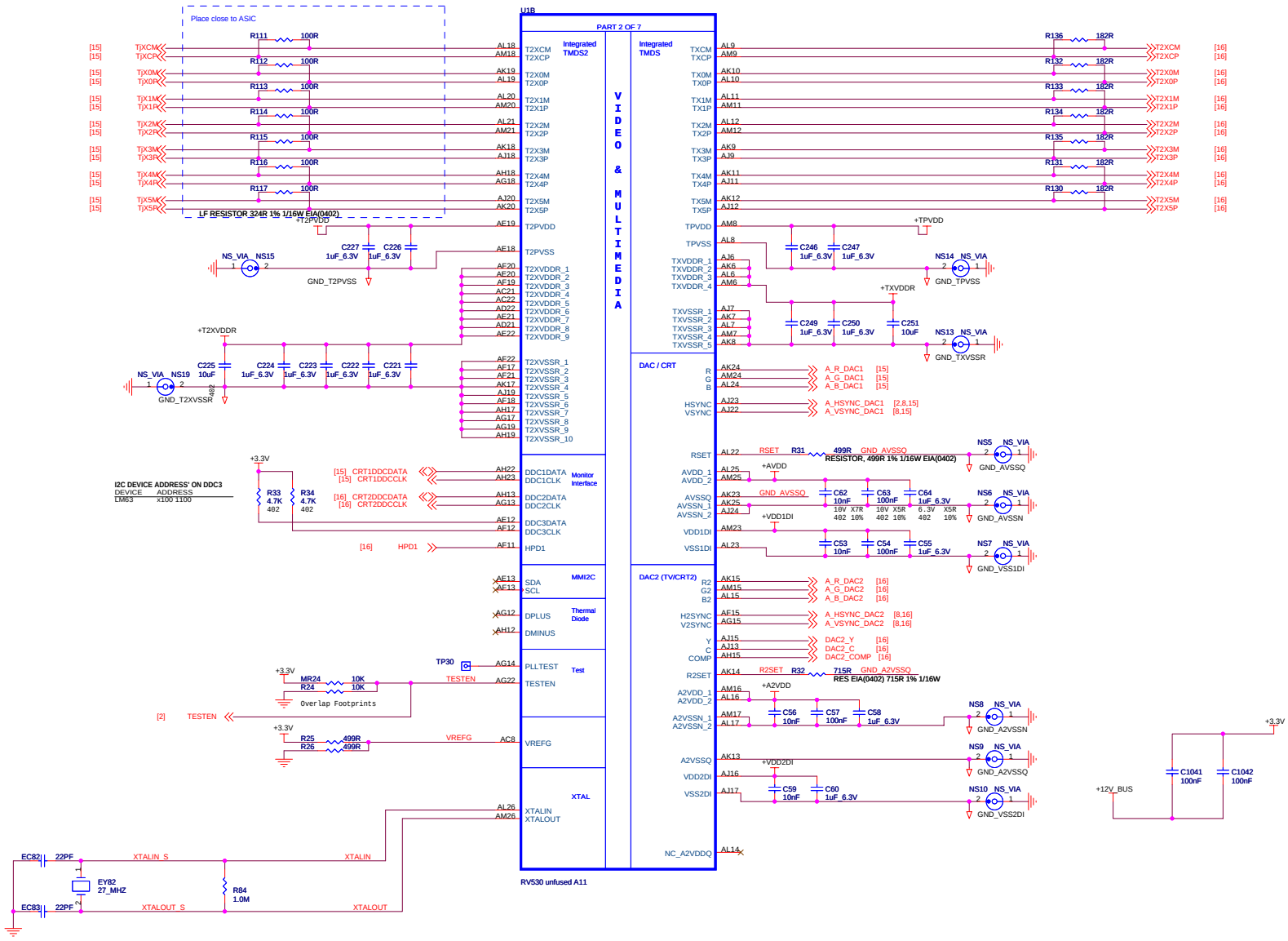
U1B
PART 2 OF 7
VIDEO & MULTIMEDIA
Integrated TMDS2
Integrated TMDS
Place close to ASIC
LF RESISTOR 324R 1% 1/16W EIA(0402)
I2C DEVICE ADDRESS' ON DDC3
DEVICE ADDRESS
LM63 x100 1100
Monitor Interface
MMI2C
Thermal Diode
Test
XTAL
DAC / CRT
DAC2 (TV/CRT2)
RESISTOR, 499R 1% 1/16W EIA(0402)
RES EIA(0402) 715R 1% 1/16W
Overlap Footprints
RV530 unfused A11
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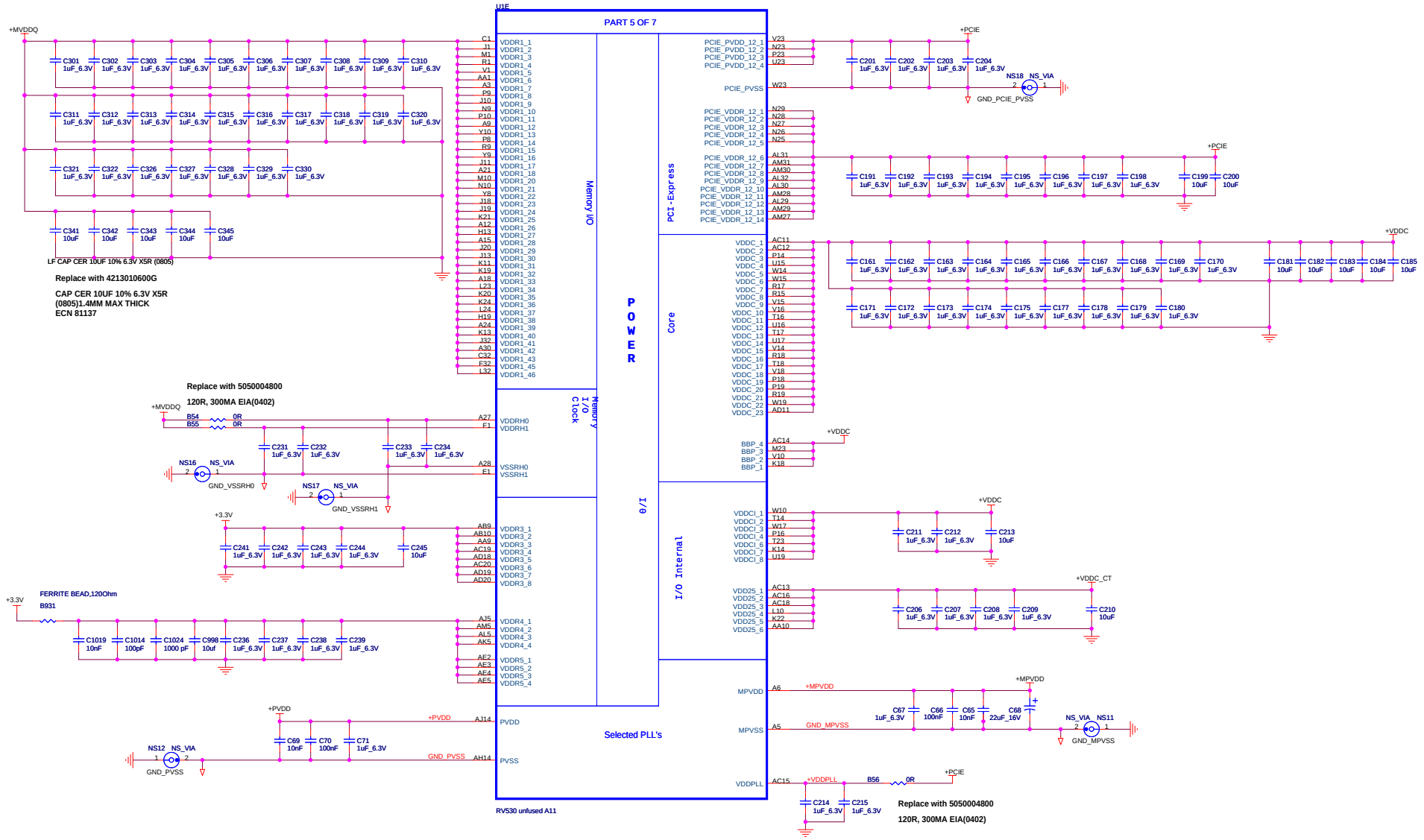

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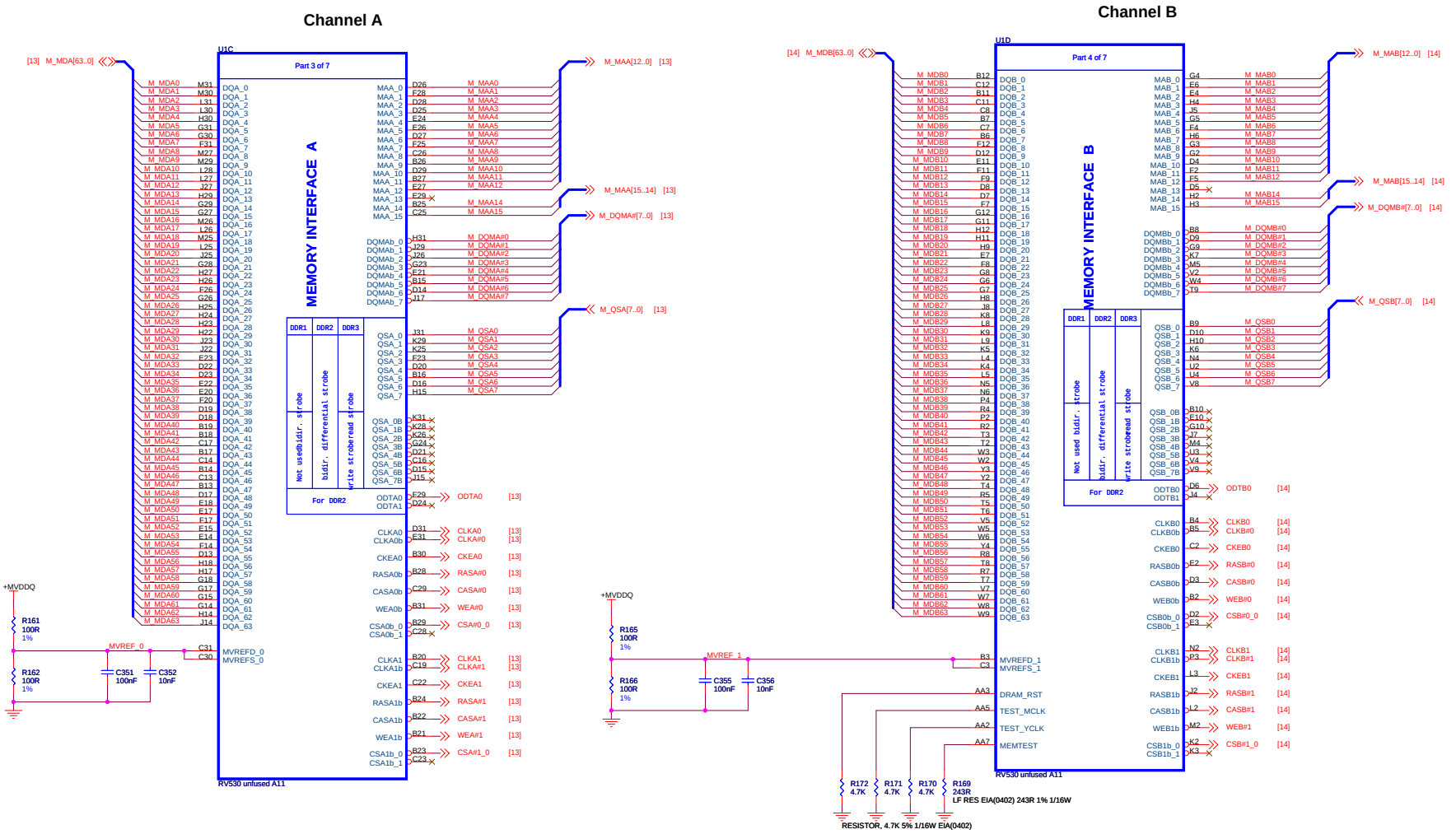
RV530 MEMORY CHANNELS A and B



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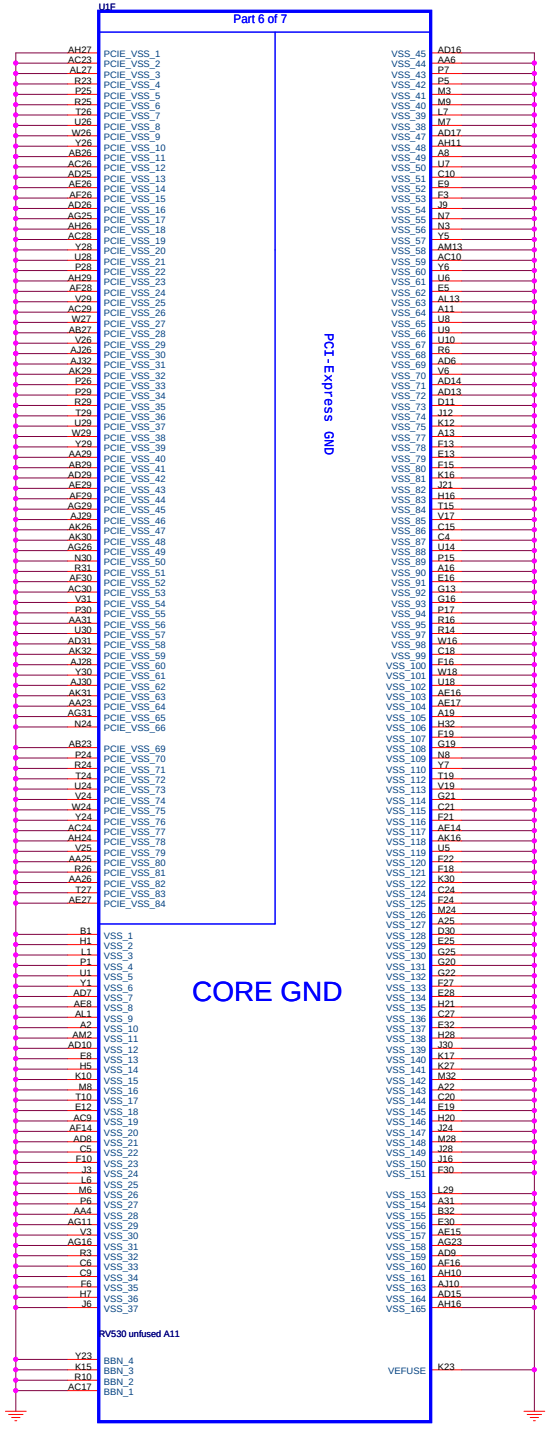

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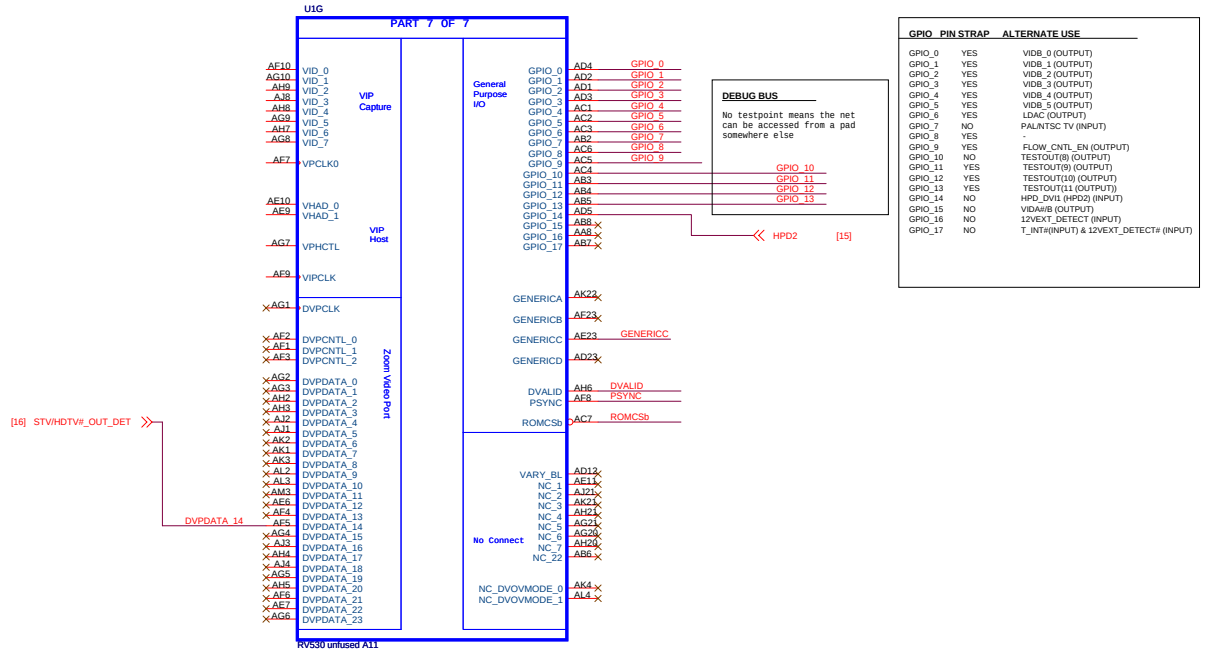
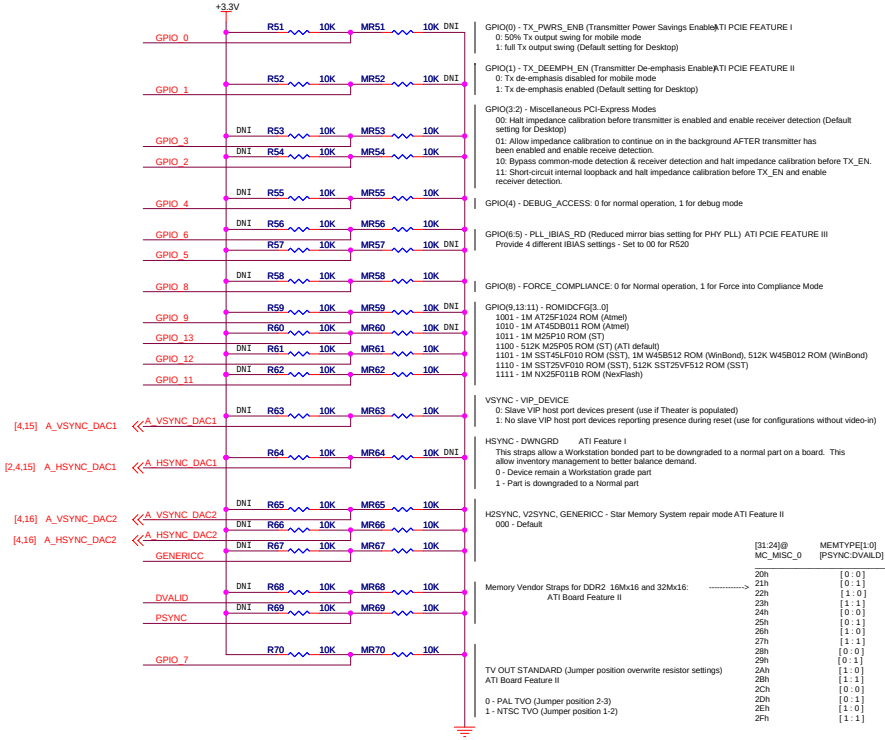


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDAKIB (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

PIN BASED STRAPS



GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - Miscellaneous PCI-Express Modes
00: Halt impedance calibration before transmitter is enabled and enable receiver detection (Default setting for Desktop)
01: Allow impedance calibration to continue on in the background AFTER transmitter has been enabled and enable receive detection.
10: Bypass common-mode detection & receiver detection and halt impedance calibration before TX_EN.
11: Short-circuit internal loopback and halt impedance calibration before TX_EN and enable receiver detection.

GPIO(4) - DEBUG_ACCESS: 0 for normal operation, 1 for debug mode

GPIO(6:5) - PLL_IBIAS_RD (Reduced mirror bias setting for PHY PLL) ATI PCIE FEATURE III
Provide 4 different IBIAS settings - Set to 00 for R520

GPIO(8) - FORCE_COMPLIANCE: 0 for Normal operation, 1 for Force into Compliance Mode

GPIO(9,13:11) - ROMIDCFG[3..0]
1001 - 1M AT25F1024 ROM (Atmel)
1010 - 1M AT45DB011 ROM (Atmel)
1011 - 1M M25P10 ROM (ST)
1100 - 512K M25P05 ROM (ST) (ATI default)
1101 - 1M SST45LF010 ROM (SST), 1M W45B512 ROM (WinBond), 512K W45B012 ROM (WinBond)
1110 - 1M SST25VF010 ROM (SST), 512K SST25VF512 ROM (SST)
1111 - 1M NX25F011B ROM (NexFlash)

VSYNC - VIP_DEVICE
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - DWNGRD ATI Feature I
This straps allow a Workstation bonded part to be downgraded to a normal part on a board. This allow inventory management to better balance demand.
0 - Device remain a Workstation grade part
1 - Part is downgraded to a Normal part

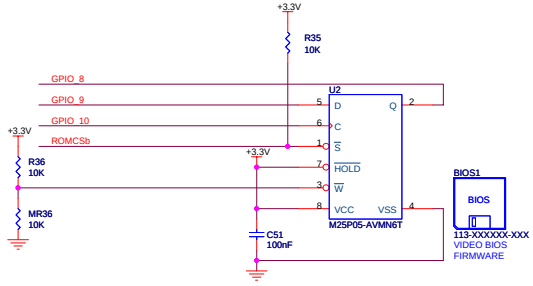
H2SYNC, V2SYNC, GENERICC - Star Memory System repair mode ATI Feature II
000 - Default

Memory Vendor Straps for DDR2 16Mx16 and 32Mx16: ----------> ATI Board Feature II

[31:24]@ MC_MISC_0	MEMTYPE[1:0] [PSYNC:DVAILD]	Memory
20h	[0 : 0]	Common and Infineon 16Mx16 2.0V
21h	[0 : 1]	Samsung 16Mx16
22h	[1 : 0]	Infineon 16Mx16 1.8V
23h	[1 : 1]	Hynix 16Mx16
24h	[0 : 0]	Micron 16Mx16
25h	[0 : 1]	Elpida 16Mx16
26h	[1 : 0]	Reserved
27h	[1 : 1]	Reserved
28h	[0 : 0]	Common 32Mx16
29h	[0 : 1]	Samsung 32Mx16
2Ah	[1 : 0]	Infineon 32Mx16
2Bh	[1 : 1]	Hynix 32Mx16
2Ch	[0 : 0]	Micron 32Mx16
2Dh	[0 : 1]	Elpida 32Mx16
2Eh	[1 : 0]	Reserved
2Fh	[1 : 1]	Reserved

TV OUT STANDARD (Jumper position overwrite resistor settings)
ATI Board Feature II

0 - PAL TVO (Jumper position 2-3)
1 - NTSC TVO (Jumper position 1-2)



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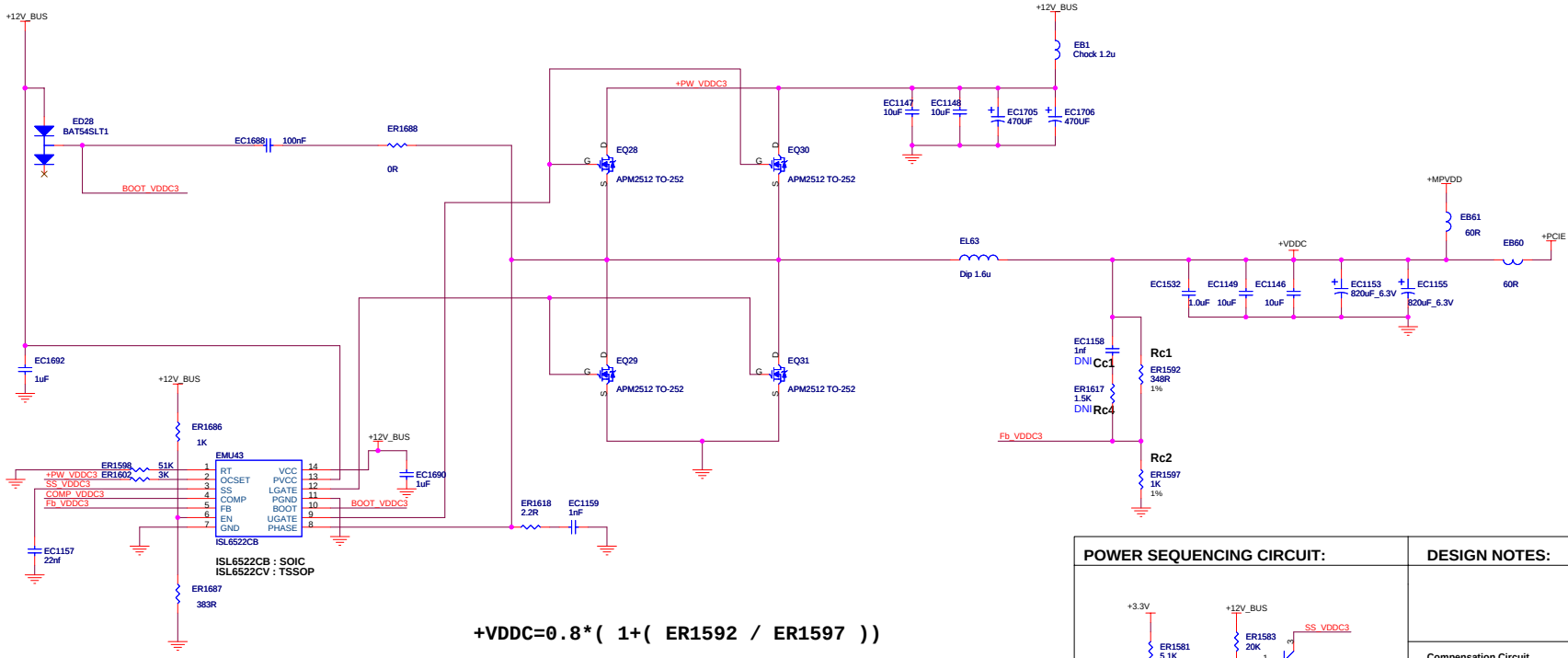
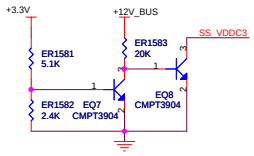
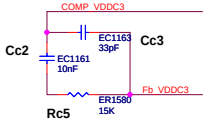
CORE REGULATOR VDDC



+VDDC=0.8*(1+(ER1592 / ER1597))

POWER SEQUENCING CIRCUIT:	DESIGN NOTES:
	Compensation Circuit 
FOR ALTERNATE #1 Remove R374, R375, R371, C168 and U32 Install R370, R112, R954, R305-R308, C160 C159 and MU32	**FOR ALTERNATE #2** Change C157 for 10 uF and C121 for 1 uF Replace C764 by 0 Ohm resistor Replace R314 with a bead Remove R954, R370, R305-R308, C159, R112, C160 and MU32 Install R374, R375, R371, C168 and U32 **Compensation circuit** Rc1 = 10K, Rc2 = 8.06K R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF

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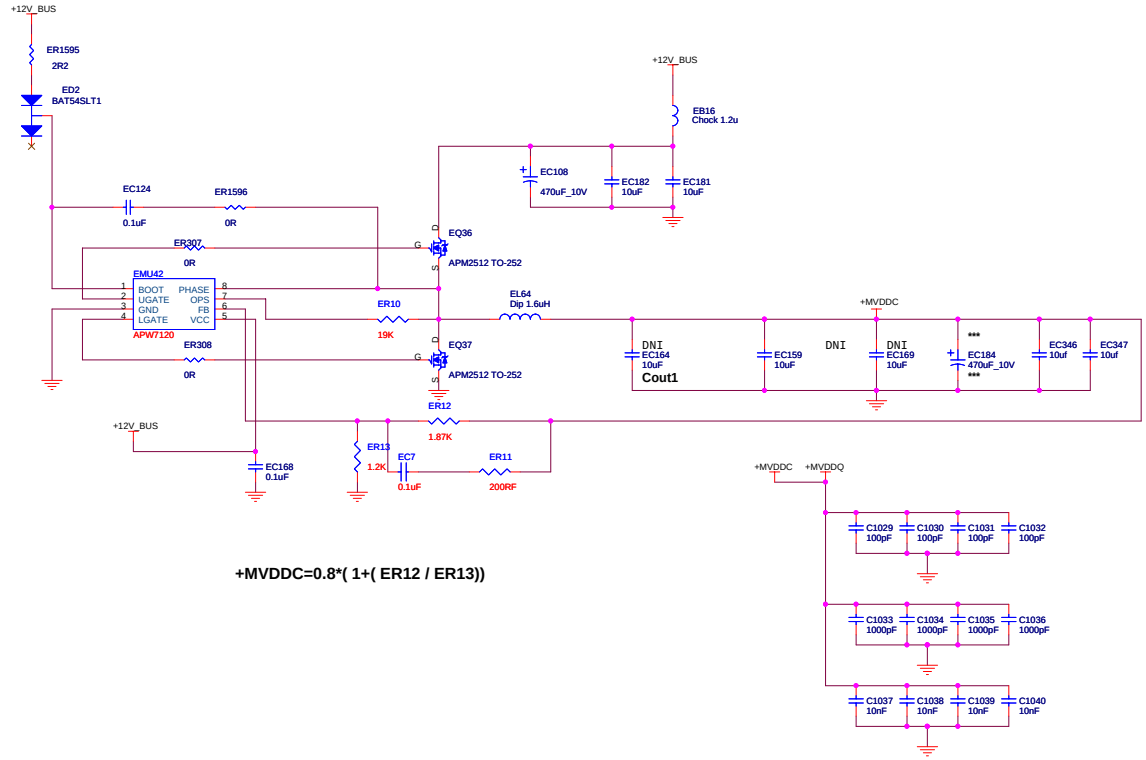

+MVDDC=0.8*(1+(ER12 / ER13))

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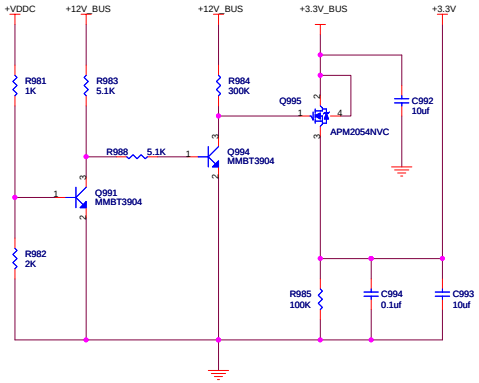

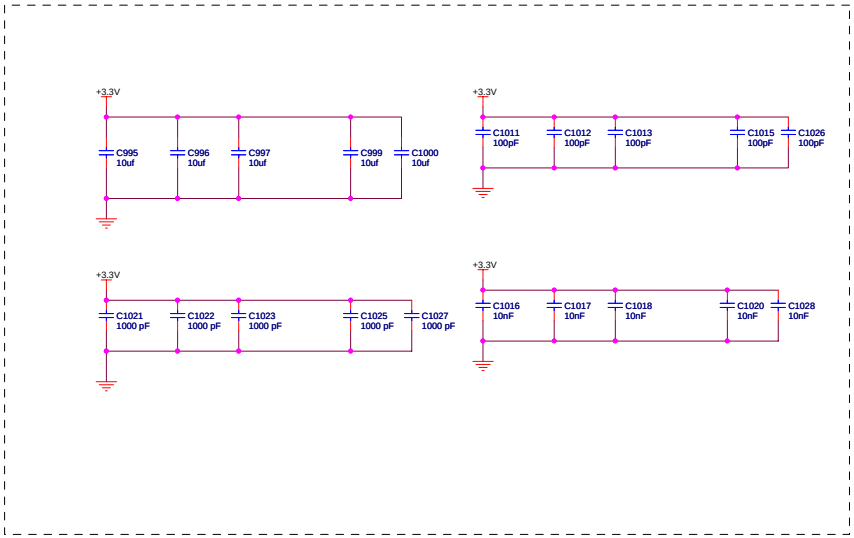

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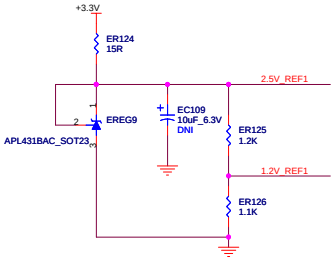
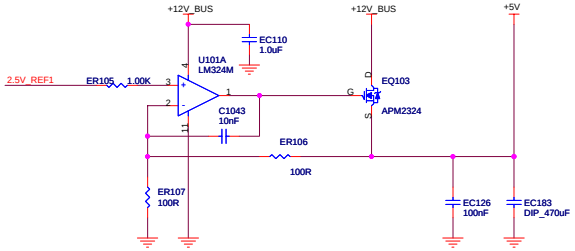
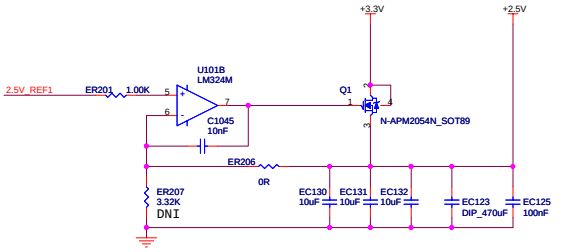
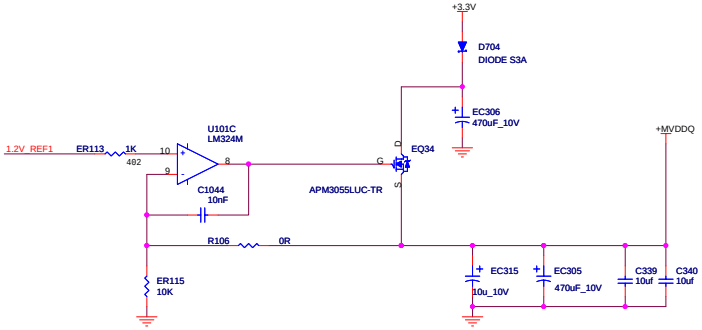
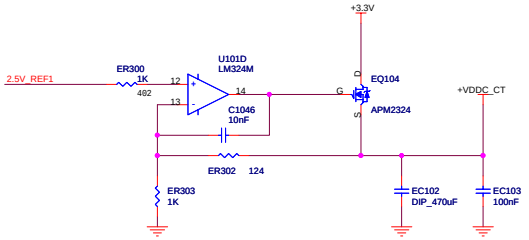


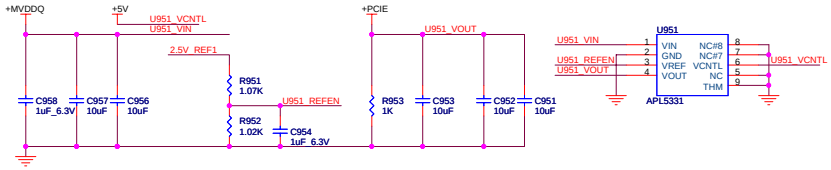








Optional regulator for +PCIE
Vout = 1.2V ~1.25V



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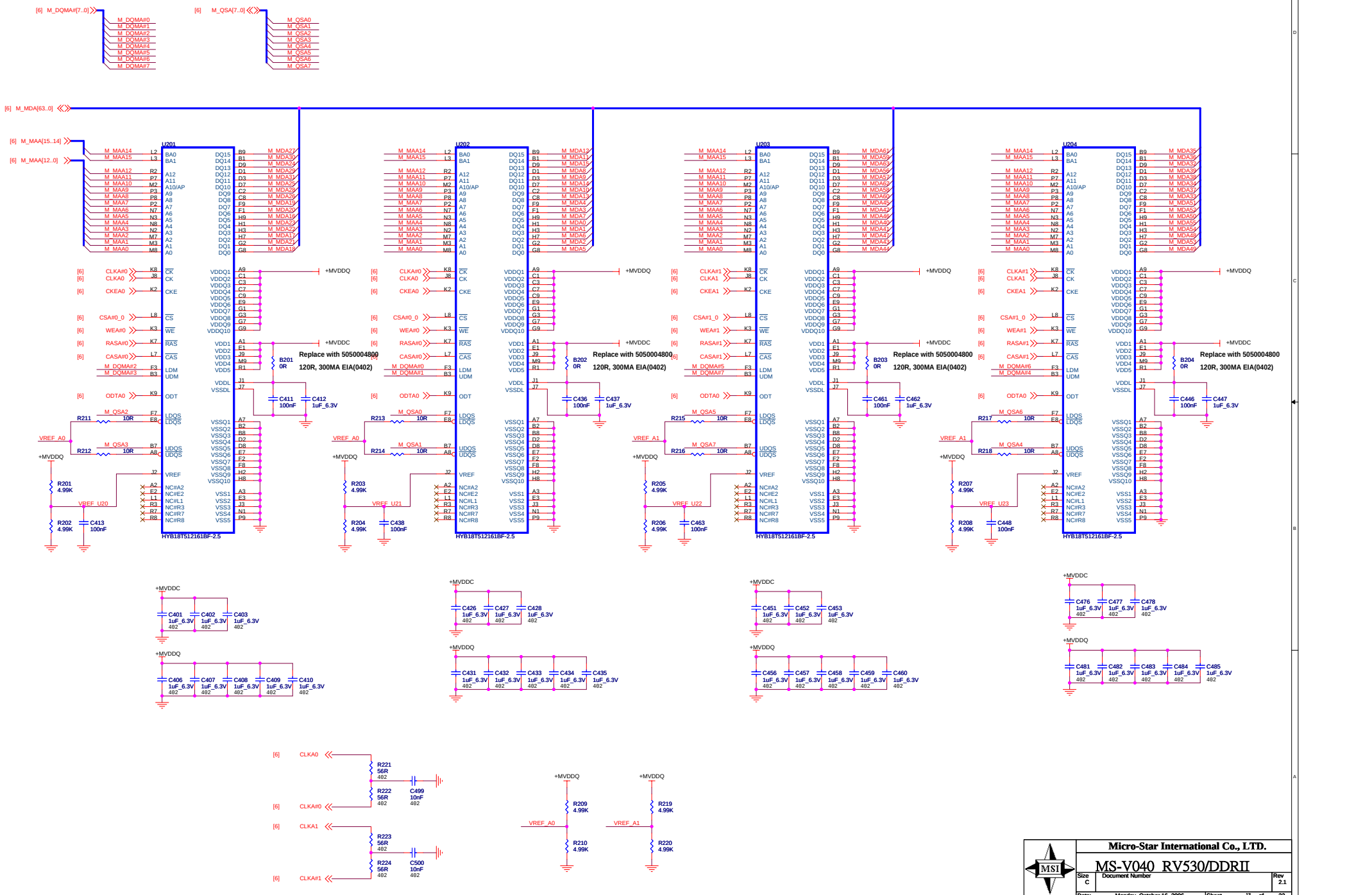
CHANNEL A: RANK 0 DDR2



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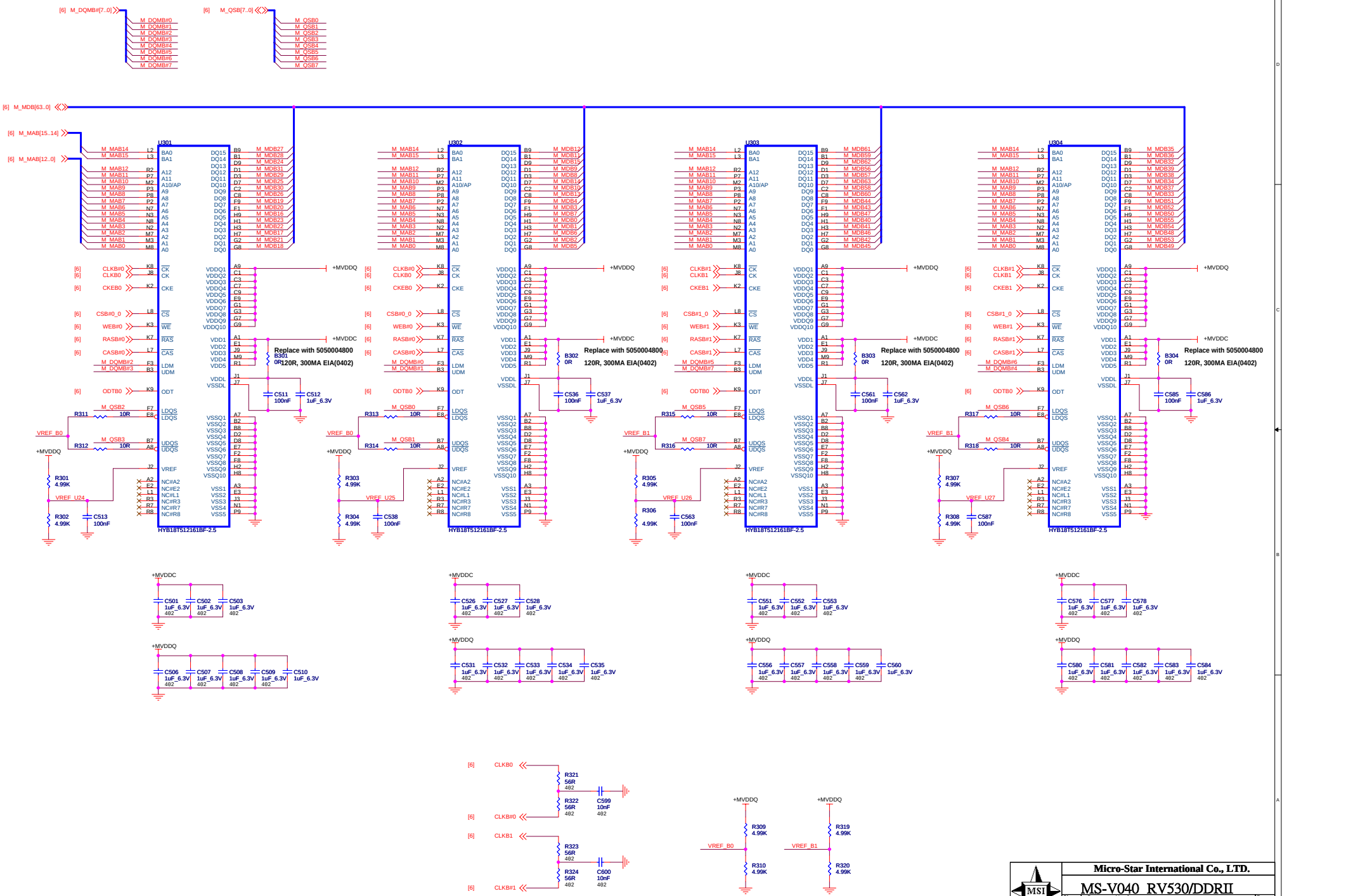
CHANNEL B: RANK 0 DDR2



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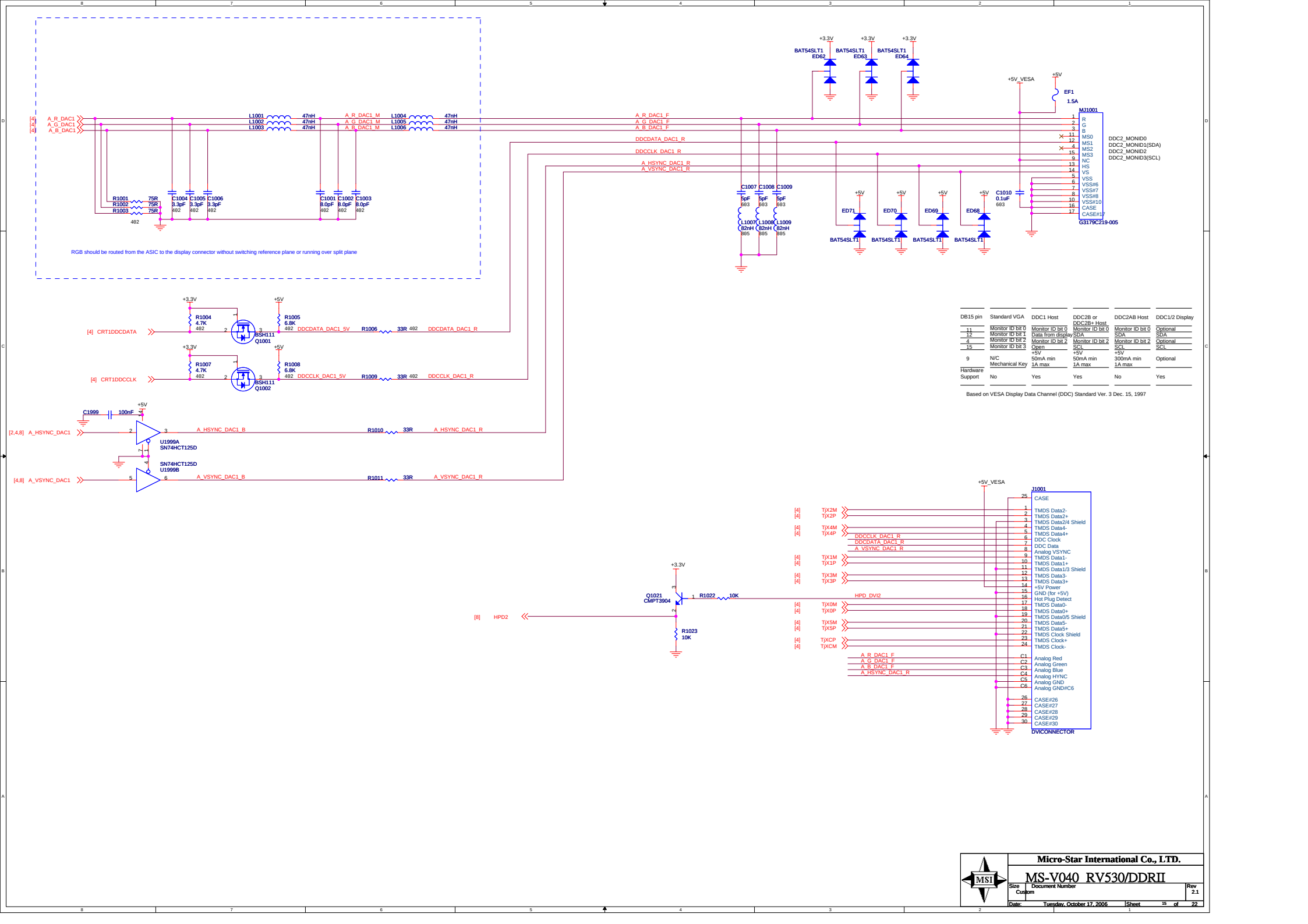

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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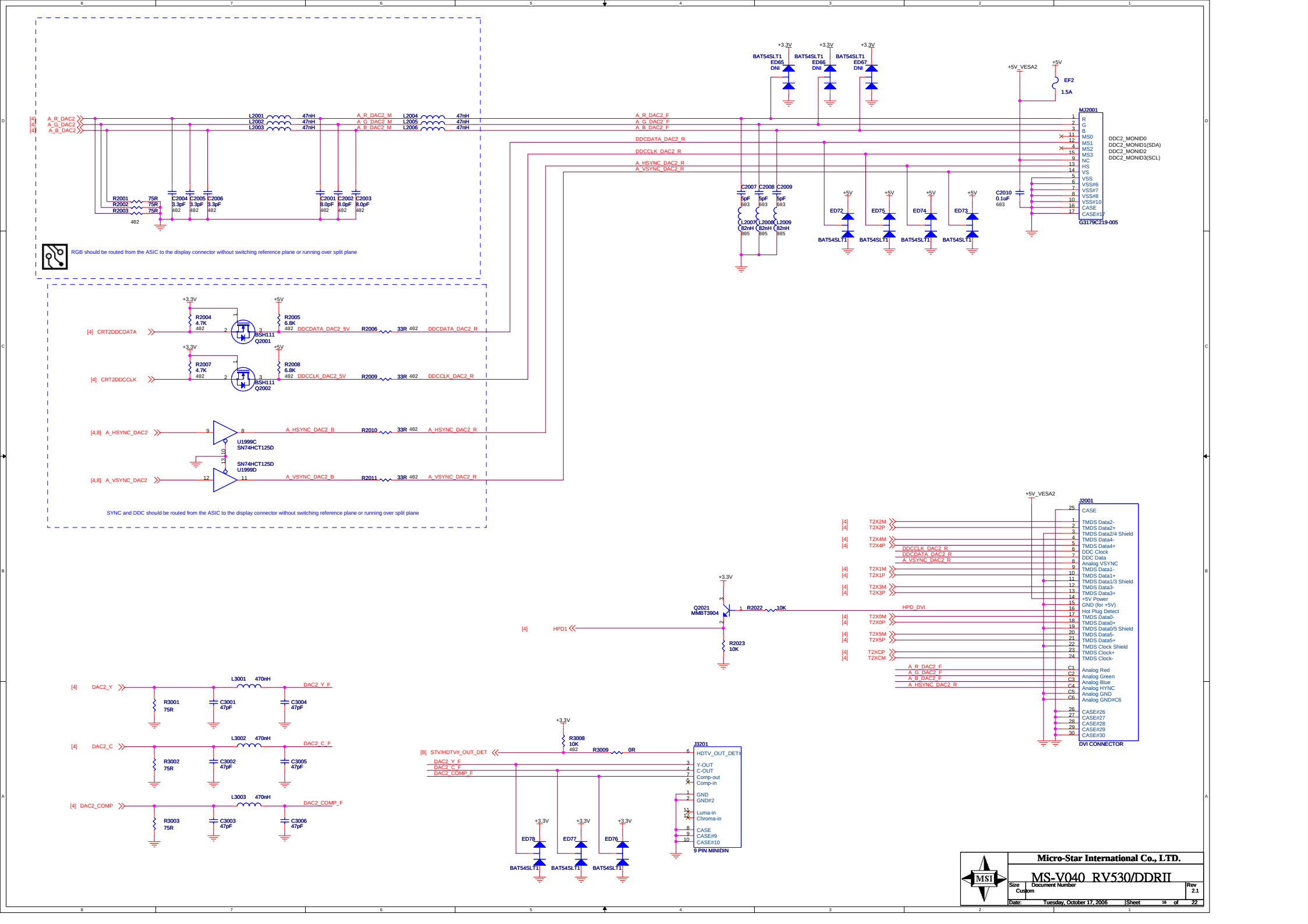
A_R_DAC2
A_G_DAC2
A_B_DAC2
L2001 L2002 L2003 47nH
A_R_DAC2_M
A_G_DAC2_M
A_B_DAC2_M
L2004 L2005 L2006 47nH
R2001 R2002 R2003 75R
C2004 C2005 C2006 3.3pF
C2001 C2002 C2003 8.0pF
402
RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane
BAT54SLT1 ED65 DNI
BAT54SLT1 ED66 DNI
BAT54SLT1 ED67 DNI
+3.3V
+5V_VESA2
+5V
EF2
1.5A
MJ2001
R
G
B
MS0
MS1
MS2
MS3
NC
HS
VS
VSS
VSS#6
VSS#7
VSS#8
VSS#10
CASE
CASE#17
G3179C219-005
DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R
C2007 C2008 C2009 5pF
L2007 L2008 L2009 82nH
C2010 0.1uF
ED72 ED75 ED74 ED73
BAT54SLT1
[4] CRT2DDCDATA
[4] CRT2DDCCLK
R2004 R2007 4.7K
R2005 R2008 6.8K
BSH111 Q2001 Q2002
DDCDATA_DAC2_5V
DDCCLK_DAC2_5V
R2006 R2009 33R
[4,8] A_HSYNC_DAC2
[4,8] A_VSYNC_DAC2
U1999C U1999D SN74HCT125D
R2010 R2011 33R
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane
J2001
CASE
TMDS Data2-
TMDS Data2+
TMDS Data2/4 Shield
TMDS Data4-
TMDS Data4+
DDC Clock
DDC Data
Analog VSYNC
TMDS Data1-
TMDS Data1+
TMDS Data1/3 Shield
TMDS Data3-
TMDS Data3+
+5V Power
GND (for +5V)
Hot Plug Detect
TMDS Data0-
TMDS Data0+
TMDS Data0/5 Shield
TMDS Data5-
TMDS Data5+
TMDS Clock Shield
TMDS Clock+
TMDS Clock-
Analog Red
Analog Green
Analog Blue
Analog HYNC
Analog GND
Analog GND#C6
CASE#26
CASE#27
CASE#28
CASE#29
CASE#30
DVI CONNECTOR
T2X2M T2X2P
T2X4M T2X4P
T2X1M T2X1P
T2X3M T2X3P
T2X0M T2X0P
T2X5M T2X5P
T2XCP T2XCM
Q2021 MMBT3904
R2022 10K
R2023 10K
HPD1
HPD_DVI
DAC2_Y
DAC2_C
DAC2_COMP
L3001 L3002 L3003 470nH
R3001 R3002 R3003 75R
C3001 C3002 C3003 47pF
C3004 C3005 C3006 47pF
DAC2_Y_F
DAC2_C_F
DAC2_COMP_F
[8] STV/HDTV#_OUT_DET
R3008 10K
R3009 0R
J3201
HDTV_OUT_DET#
Y-OUT
C-OUT
Comp-out
Comp-in
GND
GND#2
Luma-in
Chroma-in
CASE
CASE#9
CASE#10
9 PIN MINIDIN
ED78 ED77 ED76
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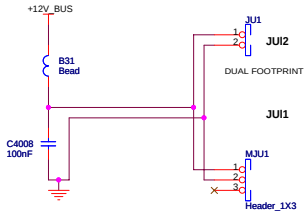

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DVI/VGA SCREWS

SCREW1
SCREW
JACKSCREW
ASSY
7020000800

SCREW2
SCREW
JACKSCREW
ASSY
7020000800

SCREW3
SCREW
JACKSCREW
ASSY
7020000800

SCREW4
SCREW
JACKSCREW
ASSY
7020000800

BKT

MT1
MT_Hole_0.136_in.
DNI

FM1
SW_FB

FM5
SW_FB

FM2
SW_FB

FM6
SW_FB

FM3
SW_FB

FM4
SW_FB

PCB

H2
LOW PROFILE HS

+MVDDQ

J1
X_PIN1*2

J3
X_PIN1*2

J2
X_PIN1*2

J4
X_PIN1*2

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