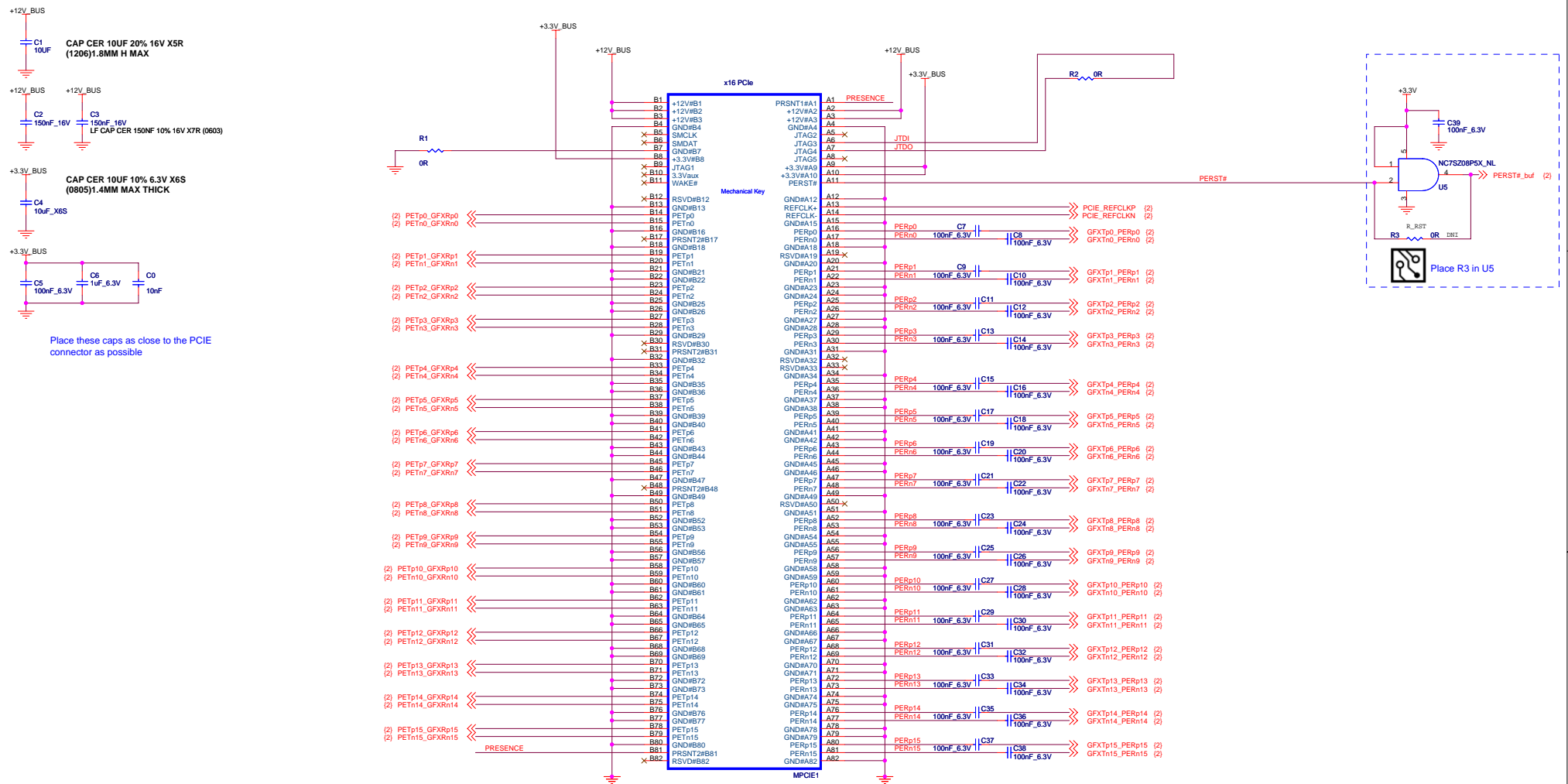





## PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

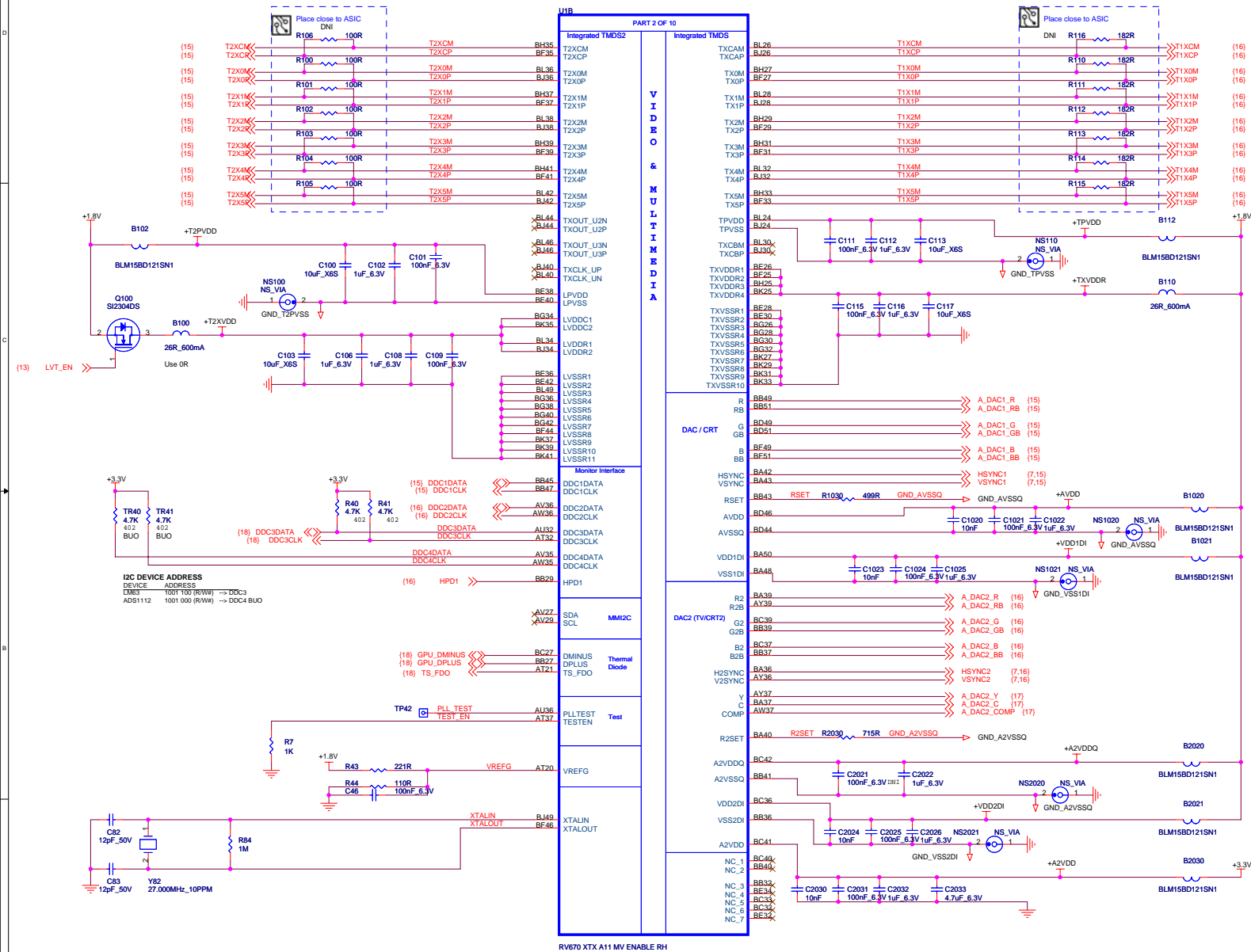
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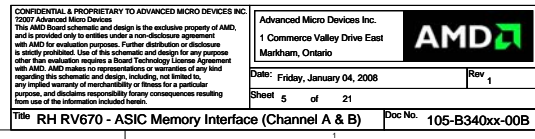
Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario		
Date: Friday, January 04, 2008		Rev 1
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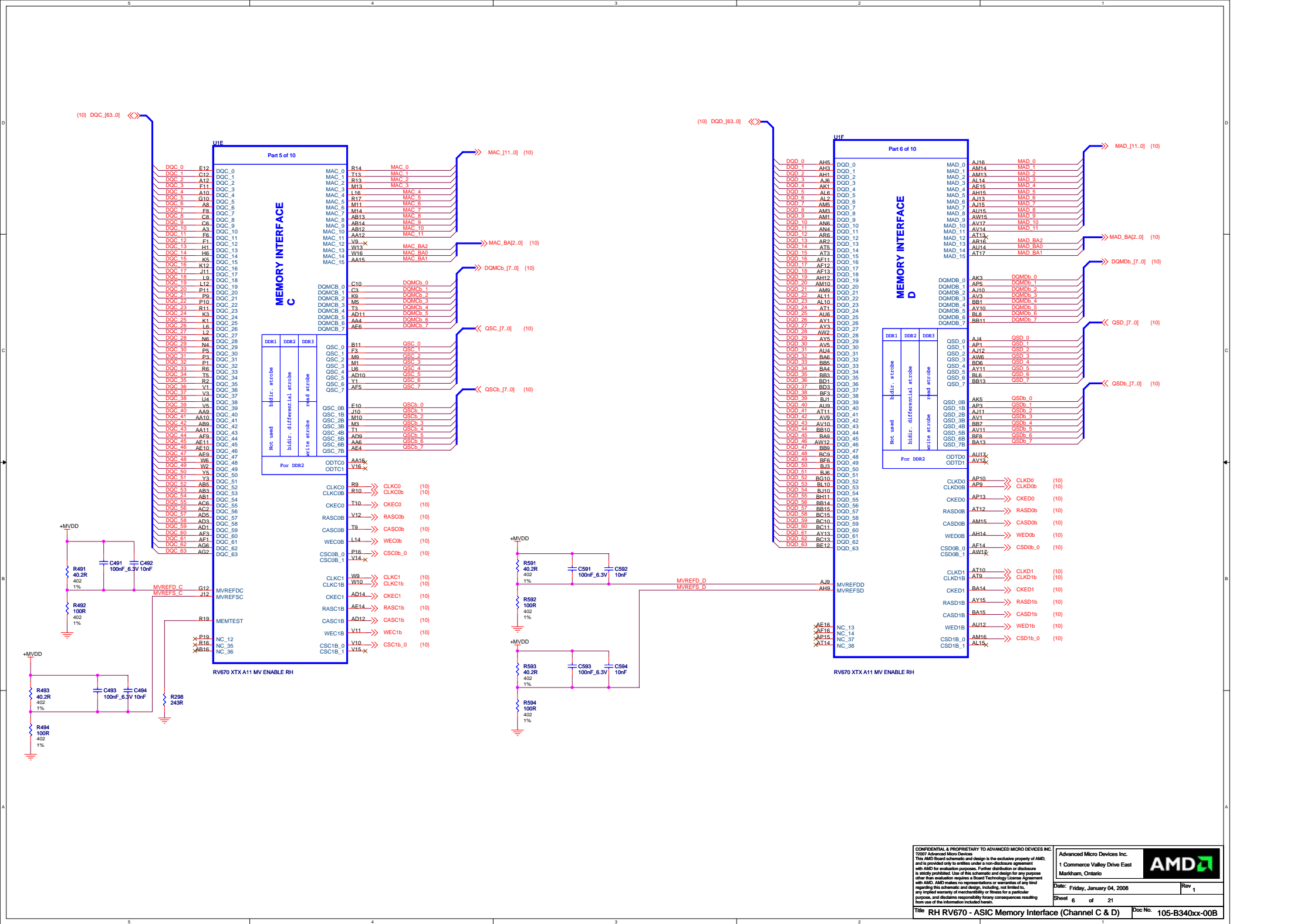


Recommended caps:  
(see BOM for qualified values/vendors)  
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK  
4.7uF , X6S/X5R, 0603, 6.3V/4V  
1uF , X6S, 0402, 6.3V  
100nF, X7R, 0402  
10nF , X7R, 0402



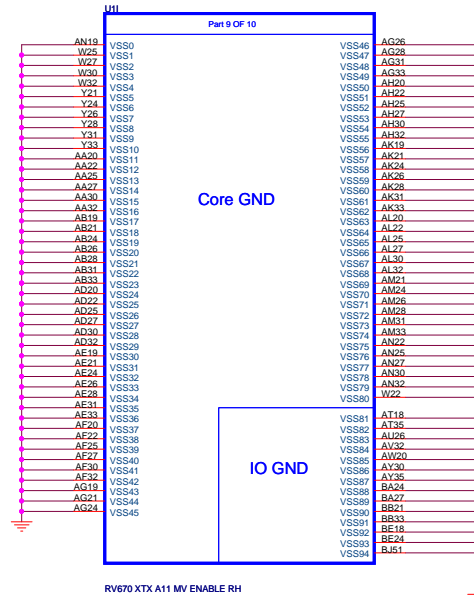
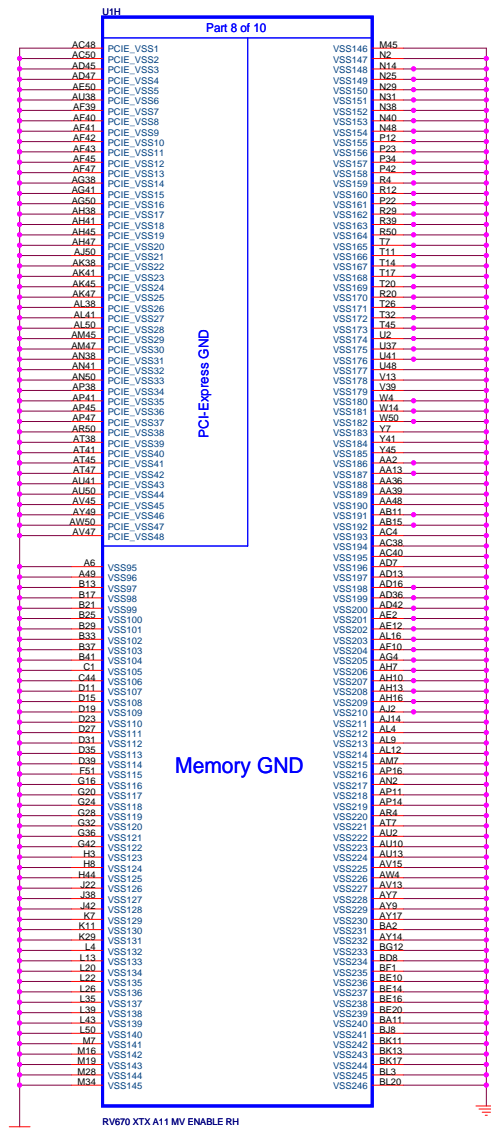




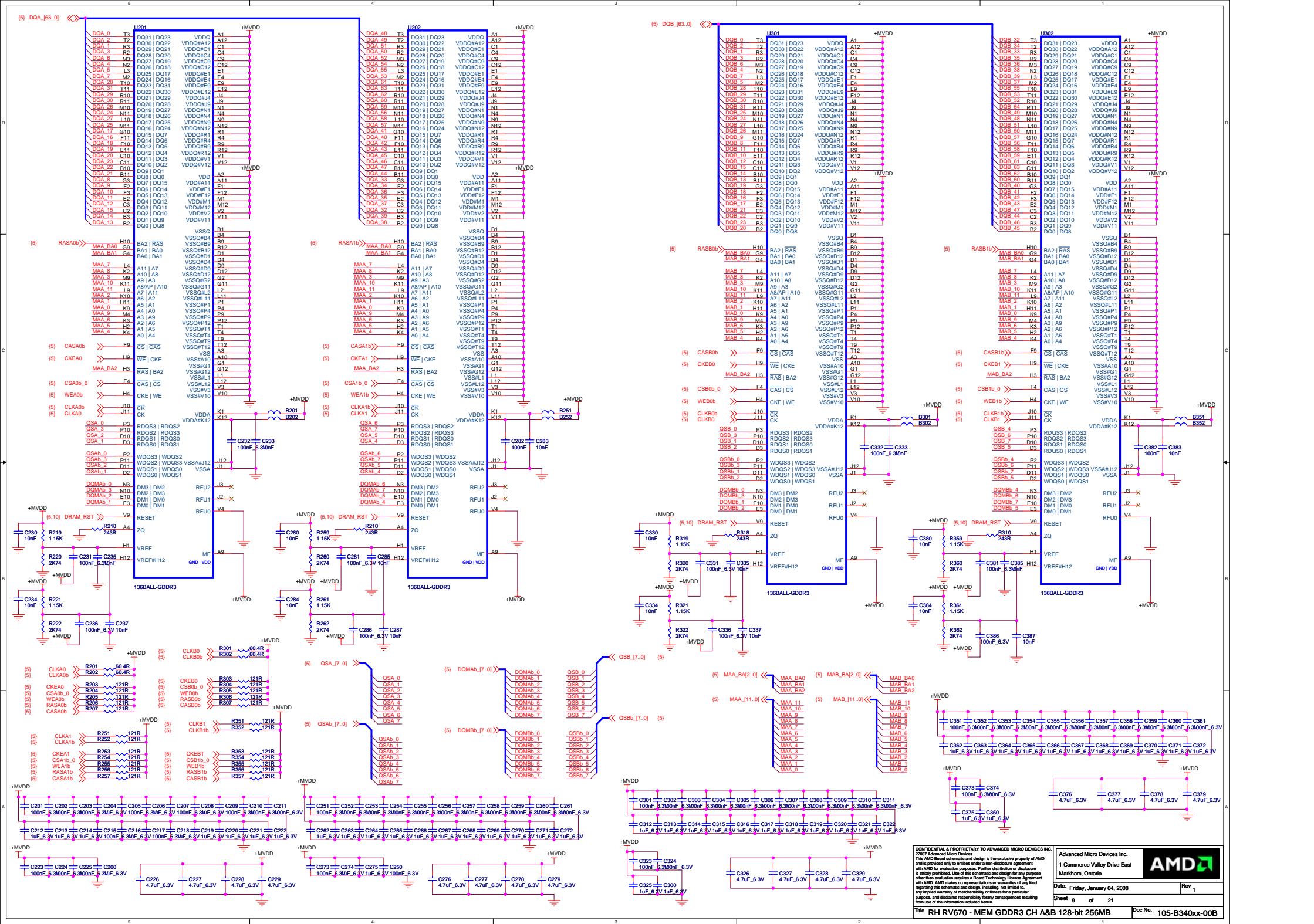


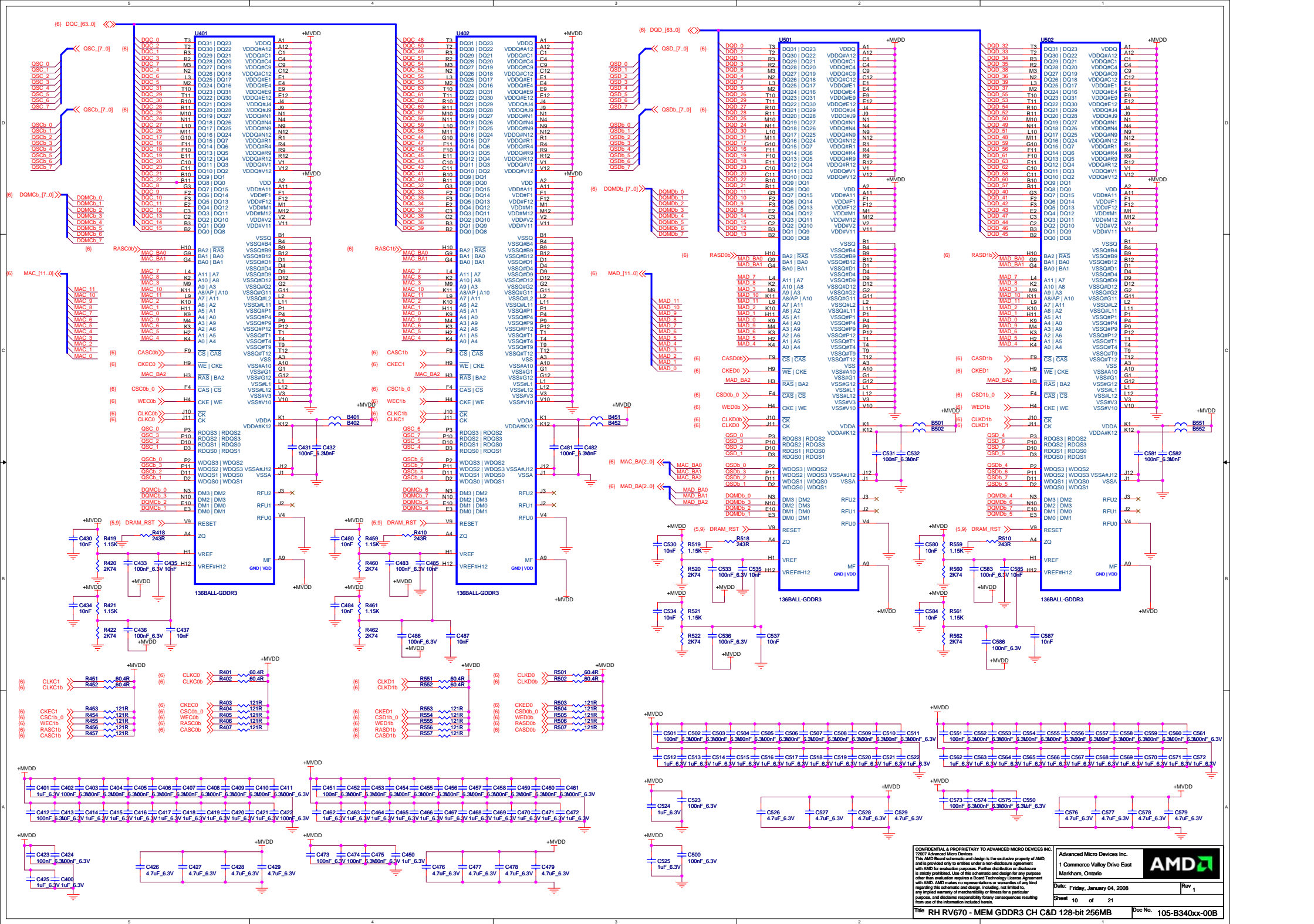
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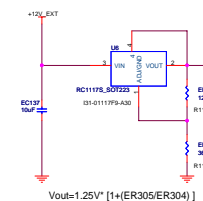
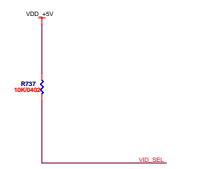


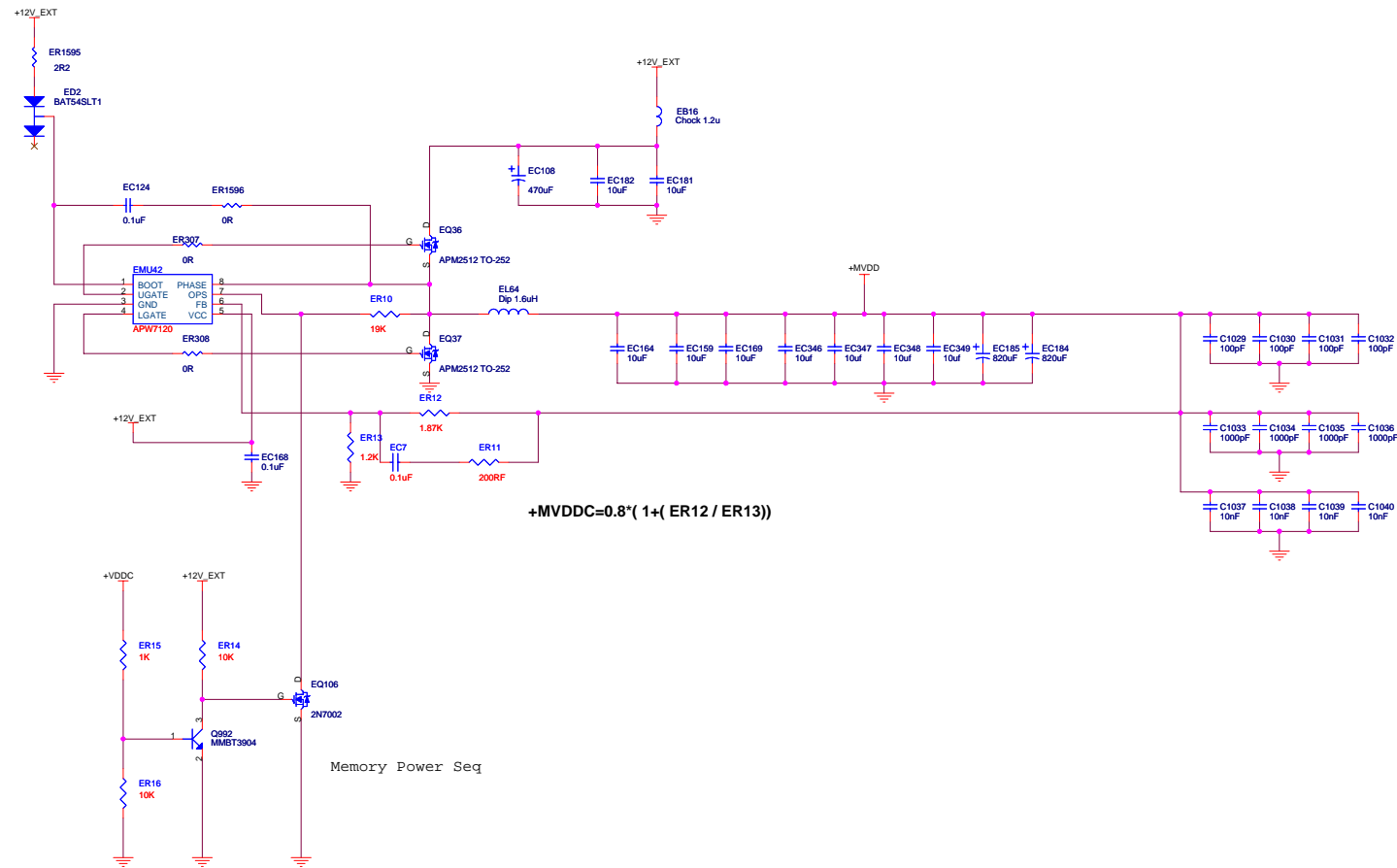




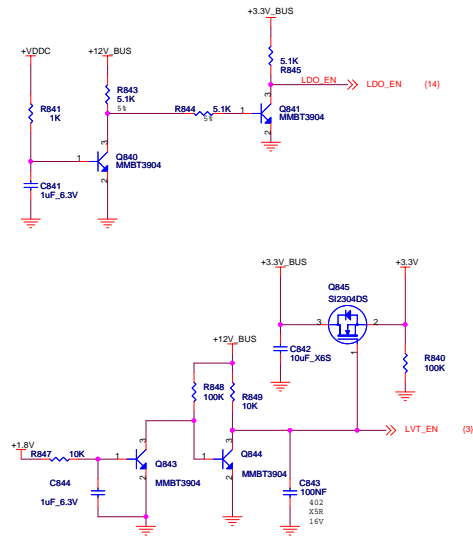


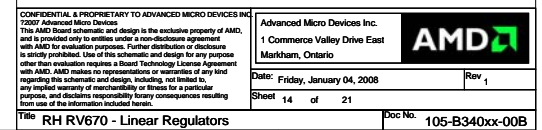
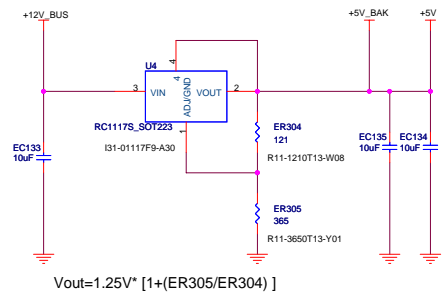
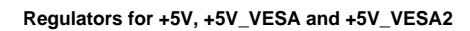
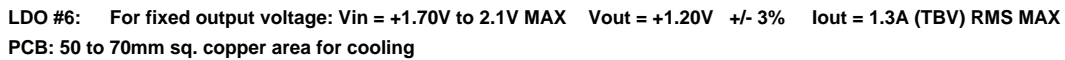
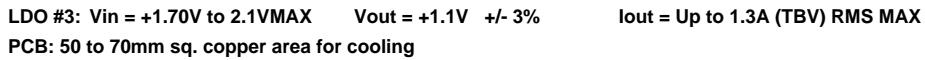
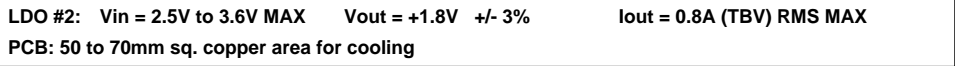


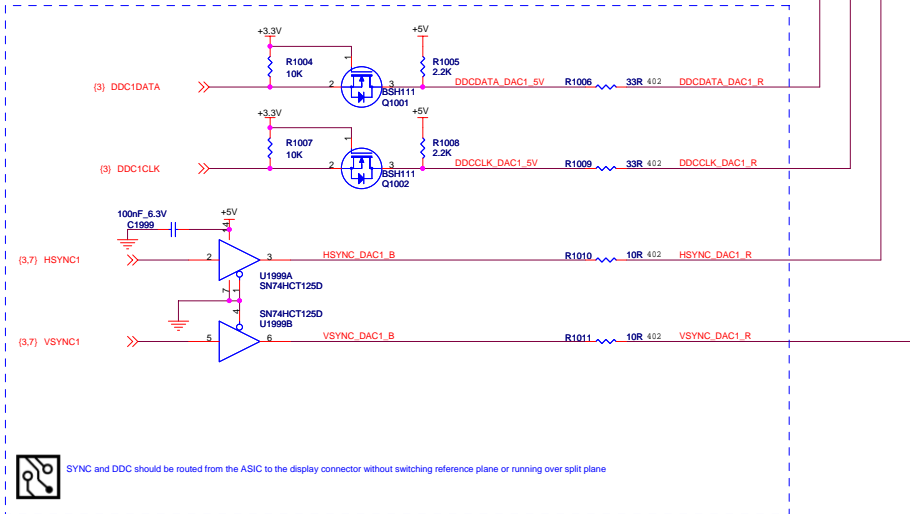
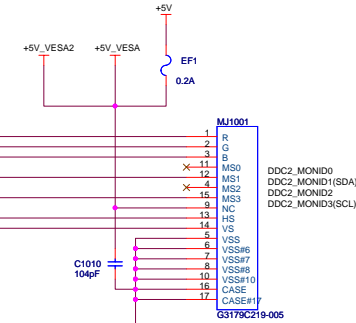
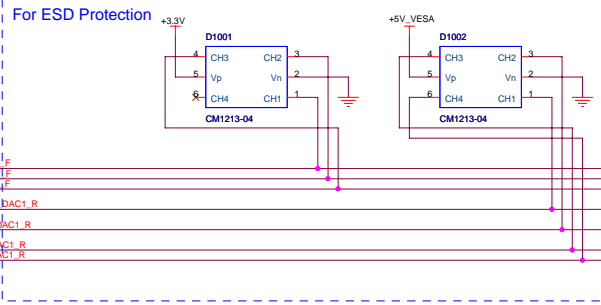
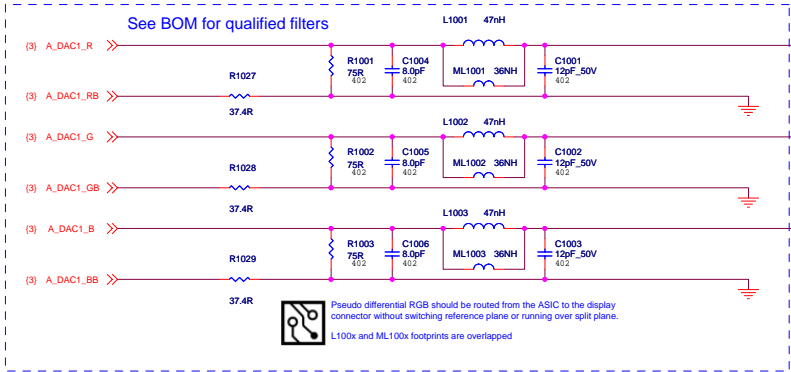




# Power up Sequencing

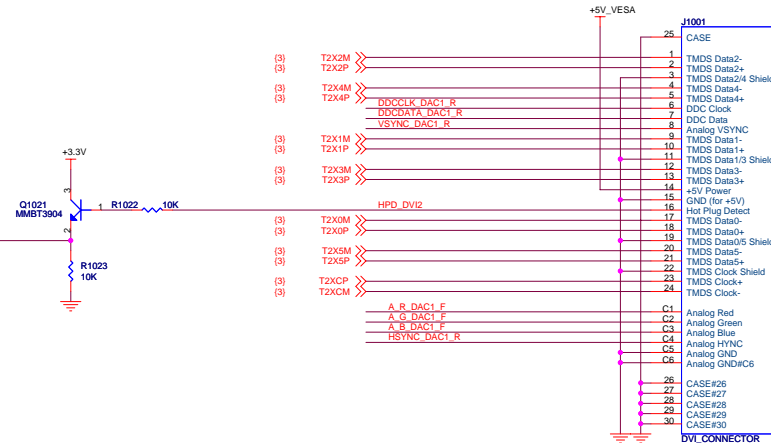




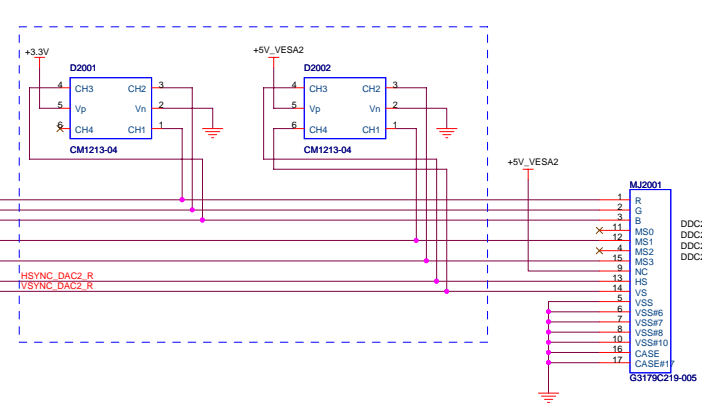
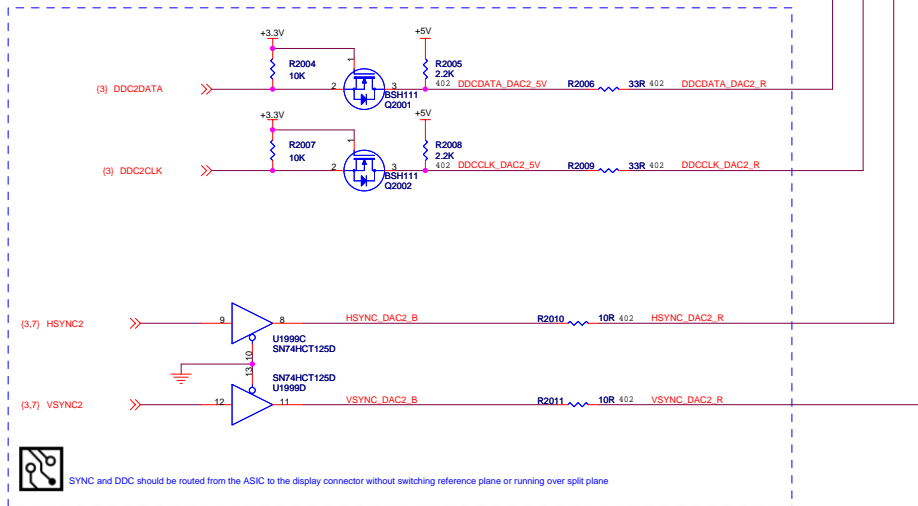
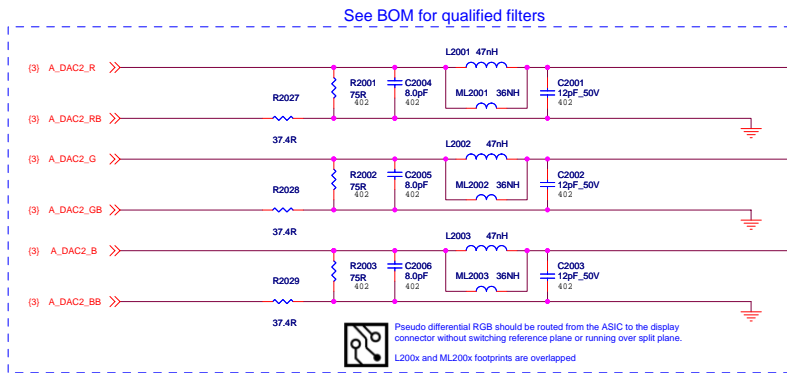


DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional SDA
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional SCL
15	Monitor ID bit 3	Open	Open	Open	Optional SCL
9	N/C	+5V	+5V	+5V	Optional
Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

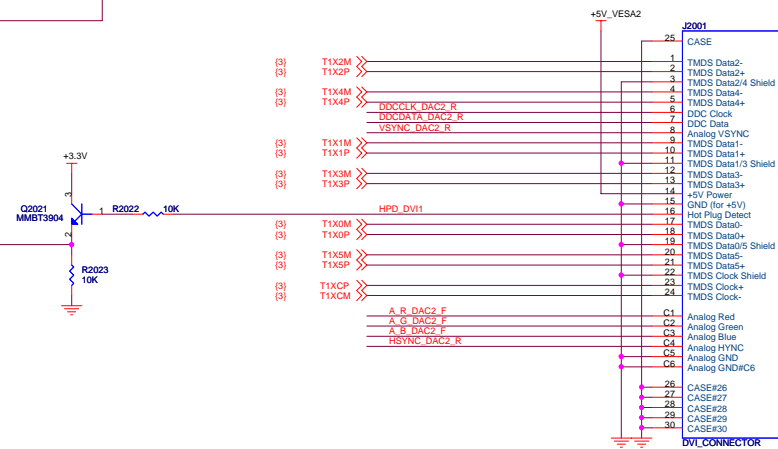


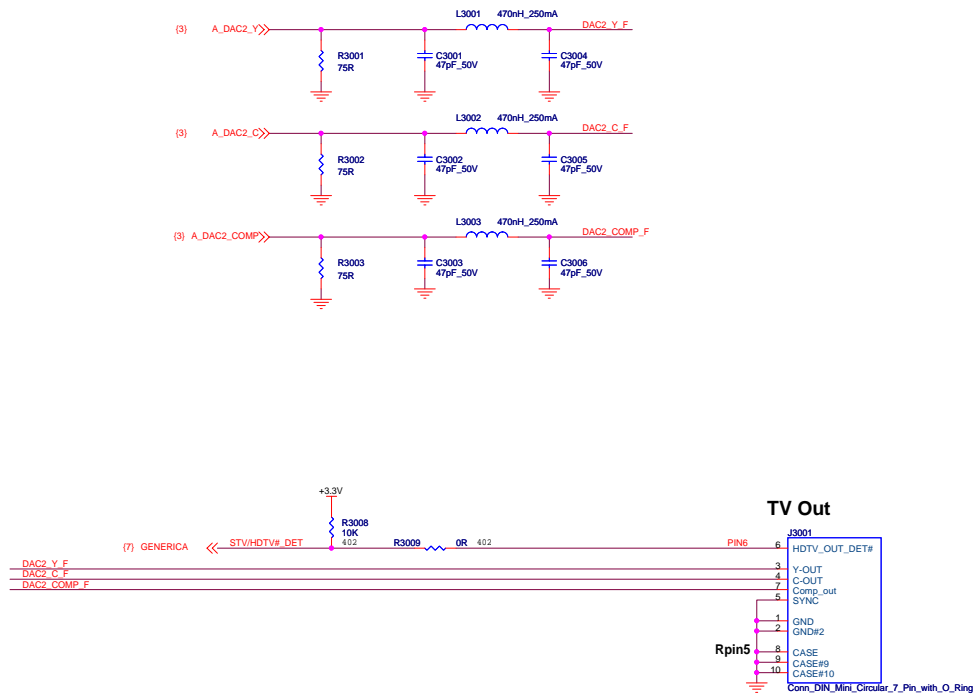




DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional SDA
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional SCL
15	Monitor ID bit 3	Open	Monitor ID bit 3	Monitor ID bit 3	Optional SCL
9	N/C	+5V	+5V	+5V	Optional
Hardware Support	Mechanical Key	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





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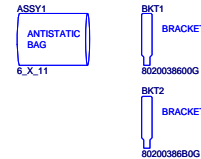
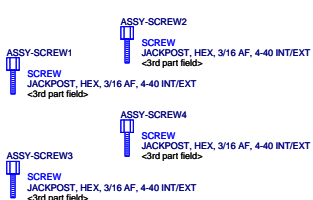
Rev 1

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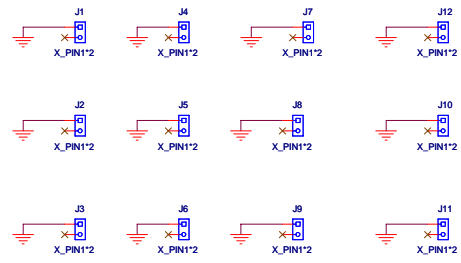
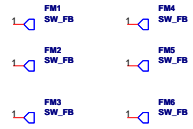
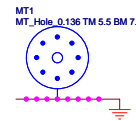
Title RH RV670 - TV OUT

Doc No. 105-B340xx-00B





BKT1: DVI - DIN-DVI  
BKT2: DVI - DVI  
ASSY-SCREWS only for Slim-VGA with upper or lower tab bracket



<div>AMD</div>			Title		Schematic No.	Date:
			RH PCIE RV670 512MB GDDR3 DUAL DL-DVI-I VO FH		105-B340xx-00B	Friday, January 04, 2008
			REVISION HISTORY			Rev 1
			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.			
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION			
0	00A	07/05/11	Initial design for RV670 GDDR3 (Revival) based on B339			
1	00B	07/08/1	(pg 1) Adding R1 and connecting switch #7 of TSW1. Some mother boards require B7 to be grounded. Table-1 updated accordingly (pg 7) Adding R64 and MR64 to select HOT_PLUG_DET or ThermINT as the interrupt source. (pg 13) Adding R1617, MR1617, R1616, Q1613, R1615, R1618, and R1619 as option to support hot plug detection of external cable. (pg 13) Adding R1282, MR1282, R1283, MR1283, R1284, MR1284, R1281, R1285, Q1280, and C1280 as option for thermal protection for VDDC SMPS MOSFETs (pg 13) Adding MC1603 (overlapped with C1603) (pg 14) Adding D870 as option for power up sequencing (pg 18) Adding heatsink symbol/footprint  (Layout) Increasing spacing between DDC4DATA & DDC4CLK going to U1270 to reduce the crosstalk			

