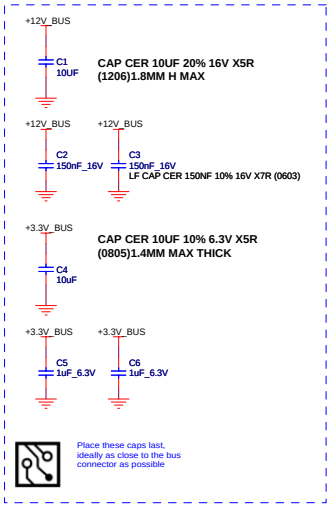
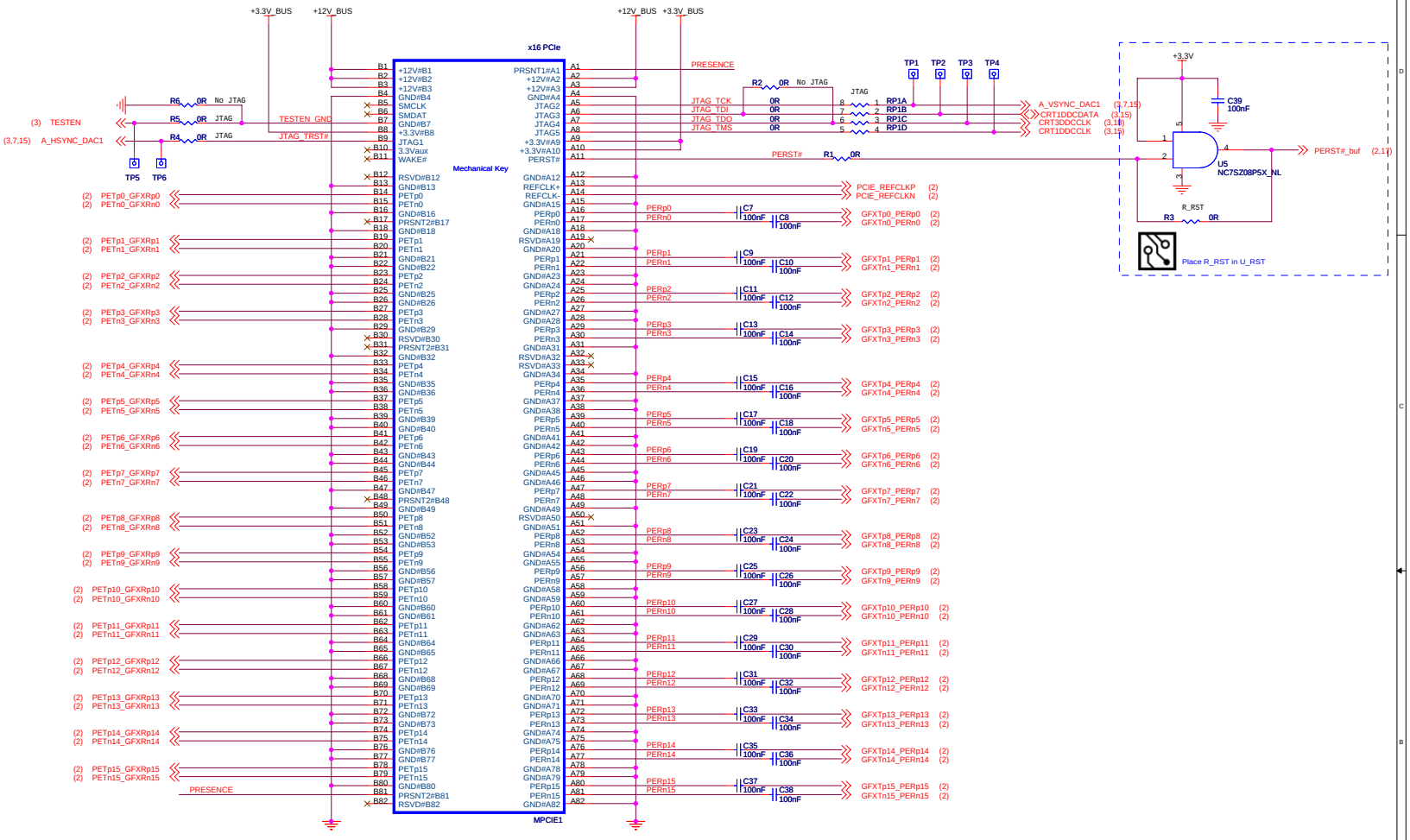
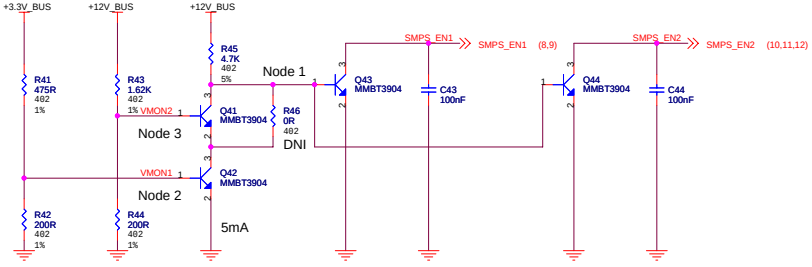
PCI-EXPRESS EDGE CONNECTOR







POWER SEQUENCING

Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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Title	RH PCIE RV560 256MB GDDR3 DUAL DL-DVI-I VIVO 6L FH		
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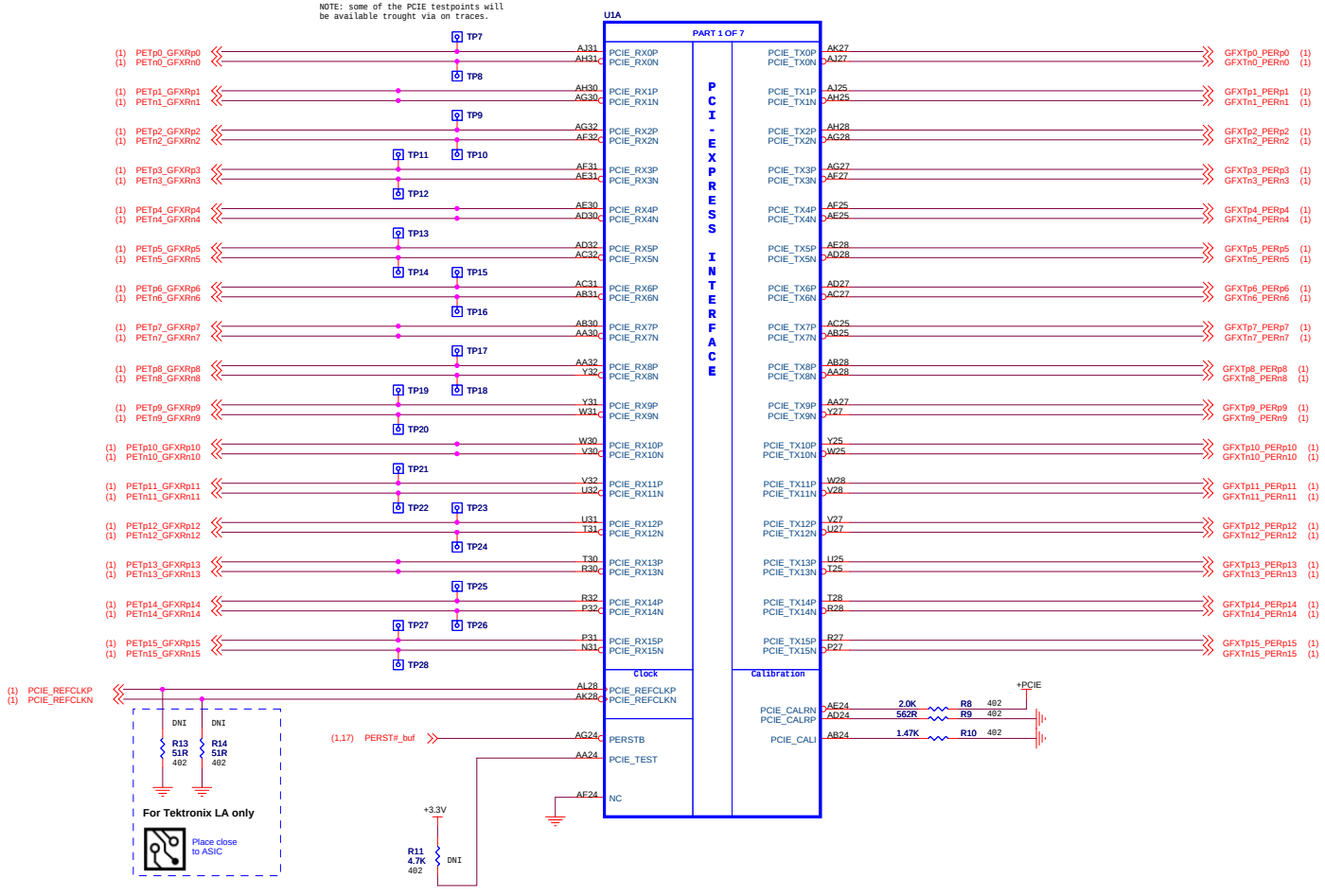

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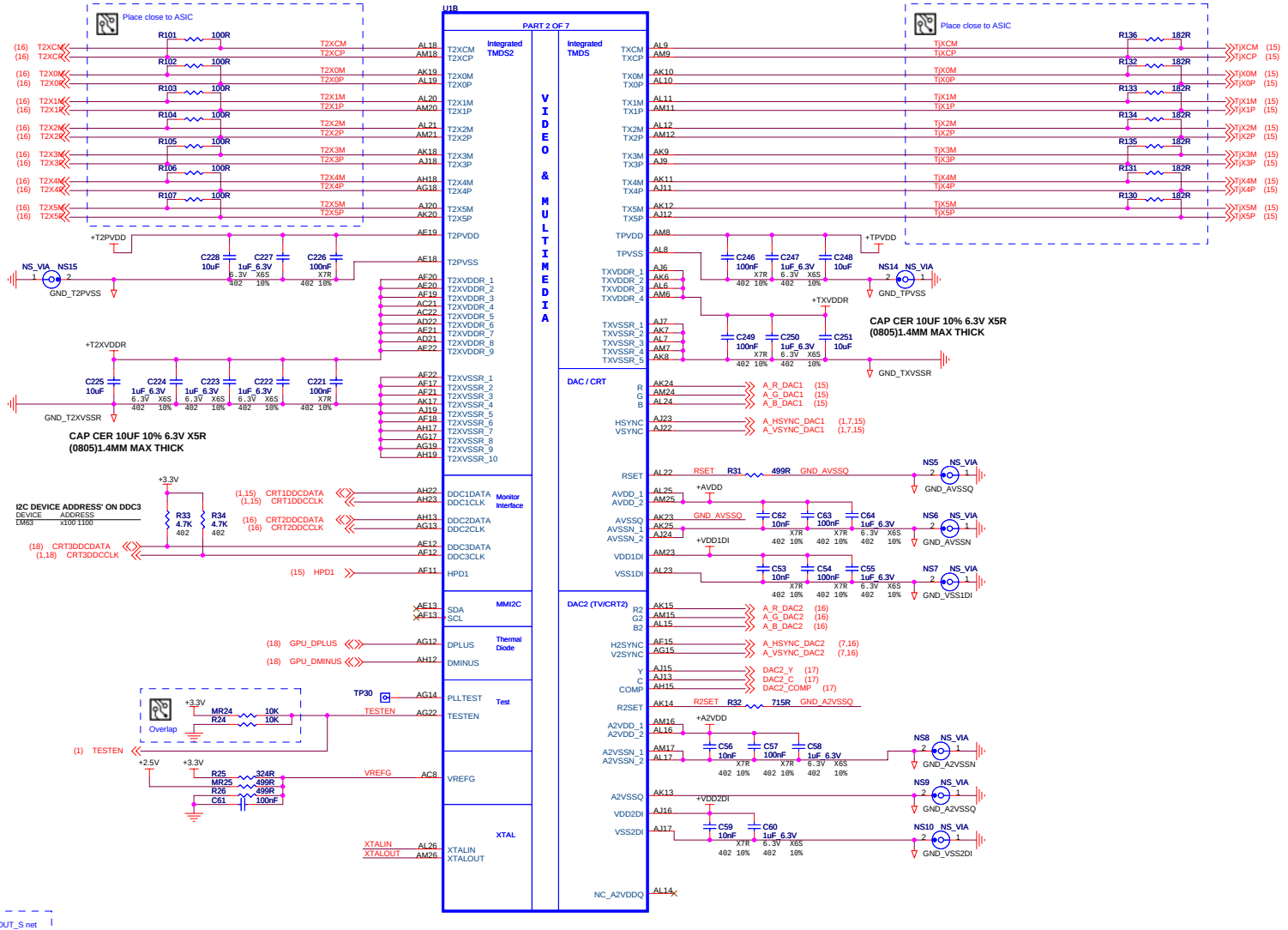
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X5R, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402



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Recommended caps:
(see BOM for qualified values/vendors)
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1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402

U1E

PART 5 OF 7

POWER

Memory I/O

Memory I/O Clock

PCI-Express

Core

DVO I/O

I/O Internal

Selected PLL's

+MVDD

C301 C302 C303 C304 C305 C306 C307 C308 C309 C310 1uF_6.3V

C311 C312 C313 C314 C315 C316 C317 C318 C319 C320 1uF_6.3V

C321 C322 C326 C327 C328 C329 C330 1uF_6.3V

C341 C342 C343 C344 C345 10uF

CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

VDDR1_1 VDDR1_2 VDDR1_3 VDDR1_4 VDDR1_5 VDDR1_6 VDDR1_7 VDDR1_8 VDDR1_9 VDDR1_10 VDDR1_11 VDDR1_12 VDDR1_13 VDDR1_14 VDDR1_15 VDDR1_16 VDDR1_17 VDDR1_18 VDDR1_20 VDDR1_21 VDDR1_22 VDDR1_23 VDDR1_24 VDDR1_25 VDDR1_26 VDDR1_27 VDDR1_28 VDDR1_29 VDDR1_30 VDDR1_31 VDDR1_32 VDDR1_33 VDDR1_34 VDDR1_35 VDDR1_36 VDDR1_37 VDDR1_38 VDDR1_39 VDDR1_40 VDDR1_41 VDDR1_42 VDDR1_43 VDDR1_45 VDDR1_46

+MVDD

B54 BLM15BD121SN1
B55 BLM15BD121SN1

C231 C232 C233 C234 1uF_6.3V

NS16 NS_VIA
NS17 NS_VIA
GND_VSSRH0
GND_VSSRH1

VDDRH0 VDDRH1 VSSRH0 VSSRH1

+3.3V

C241 C242 C243 C244 1uF_6.3V

C245 10uF

CAP CER 10UF 10%
6.3V X5R (0805)1.4MM
MAX THICK

VDDR3_1 VDDR3_2 VDDR3_3 VDDR3_4 VDDR3_5 VDDR3_6 VDDR3_7 VDDR3_8

+1.8V +3.3V +VDDR_DVP

RP73A RP73B RP73C RP73D 0R

MRP73A MRP73B MRP73C MRP73D 0R

C236 C237 C238 C239 1uF_6.3V

VDDR4_1 VDDR4_2 VDDR4_3 VDDR4_4

VDDR5_1 VDDR5_2 VDDR5_3 VDDR5_4

+PVDD

C69 10nF C70 100nF C71 1uF_6.3V

NS12 NS_VIA
GND_PVSS

PVDD PVSS

PCIE_PVDD_12_1 PCIE_PVDD_12_2 PCIE_PVDD_12_3 PCIE_PVDD_12_4 V23 N23 P23 U23

PCIE_PVSS W23

+PCIE

C201 C202 C203 C204 1uF_6.3V

NS18 NS_VIA
GND_PCIE_PVSS

PCIE_VDDR_12_1 PCIE_VDDR_12_2 PCIE_VDDR_12_3 PCIE_VDDR_12_4 PCIE_VDDR_12_5 PCIE_VDDR_12_6 PCIE_VDDR_12_7 PCIE_VDDR_12_8 PCIE_VDDR_12_9 PCIE_VDDR_12_10 PCIE_VDDR_12_11 PCIE_VDDR_12_12 PCIE_VDDR_12_13 PCIE_VDDR_12_14

N29 N28 N27 N26 N25 AL31 AM31 AM30 AL32 AL30 AM28 AL29 AM29 AM27

C191 C192 C193 C194 C195 C196 C197 C198 1uF_6.3V

C199 C200 10uF

CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22 VDDC_23 VDDC_24 VDDC_25 VDDC_26 VDDC_27 VDDC_28 VDDC_29 VDDC_30 VDDC_31 VDDC_32 VDDC_33 VDDC_34 VDDC_35 VDDC_36 VDDC_37 VDDC_38 VDDC_39

AC11 AC12 P14 U15 W14 W15 R17 R15 V15 V16 T16 U16 T17 U17 V14 R18 T18 V19 P18 P19 R19 W19 AD11 N13 N14 N19 N20 P13 P20 W13 W20 Y13 Y14 Y19 Y20 AC14 M23 V10 K18

+VDDC

C161 C162 C163 C164 C165 C166 C167 C168 C169 C170 1uF_6.3V

C181 C182 C183 10uF

C171 C172 C173 C174 C175 C176 C177 C178 C179 C180 1uF_6.3V

C151 C152 1uF_6.3V

CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

VDDCI_1 VDDCI_2 VDDCI_3 VDDCI_4 VDDCI_6 VDDCI_7 VDDCI_8

W10 T14 W17 P16 T23 K14 U19

+VDDCI

C211 C212 C216 1uF_6.3V

C213 10uF

VDD25_1 VDD25_2 VDD25_3 VDD25_4 VDD25_5 VDD25_6

AC13 AC16 AC18 L10 K22 AA10

+VDDC_CT

C206 C207 C208 C209 1uF_6.3V

C210 10uF

MPVDD MPVSS

A6 A5 GND_MPVSS

+MPVDD

C67 1uF_6.3V C66 100nF C65 10nF

C68 22uF_16V

NS_VIA NS11
GND_MPVSS

VDDPLL

AC15 +VDDPLL

B56 BLM15BD121SN1

+PCIE

C214 C215 1uF_6.3V

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C	105-A880xx-01	6
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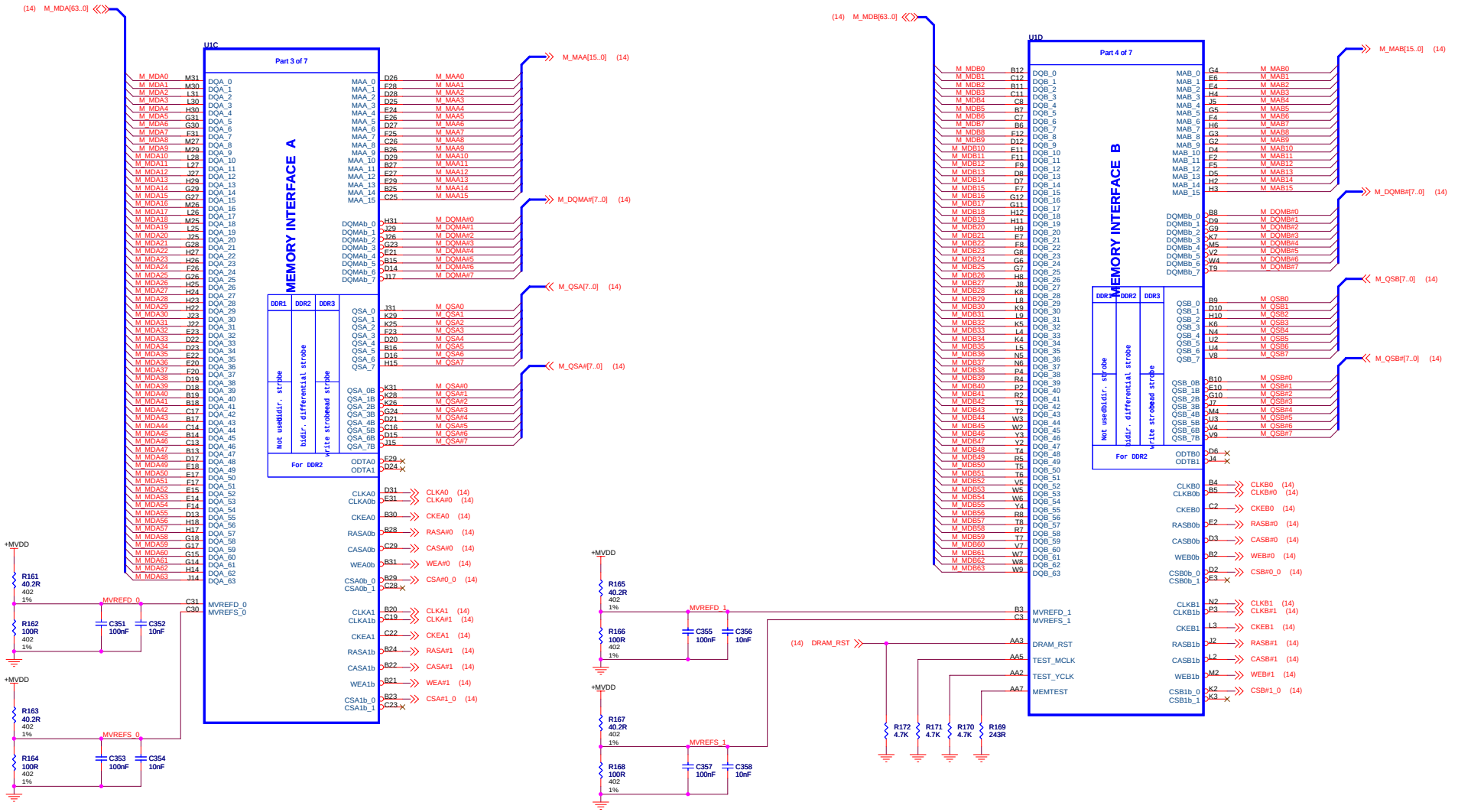

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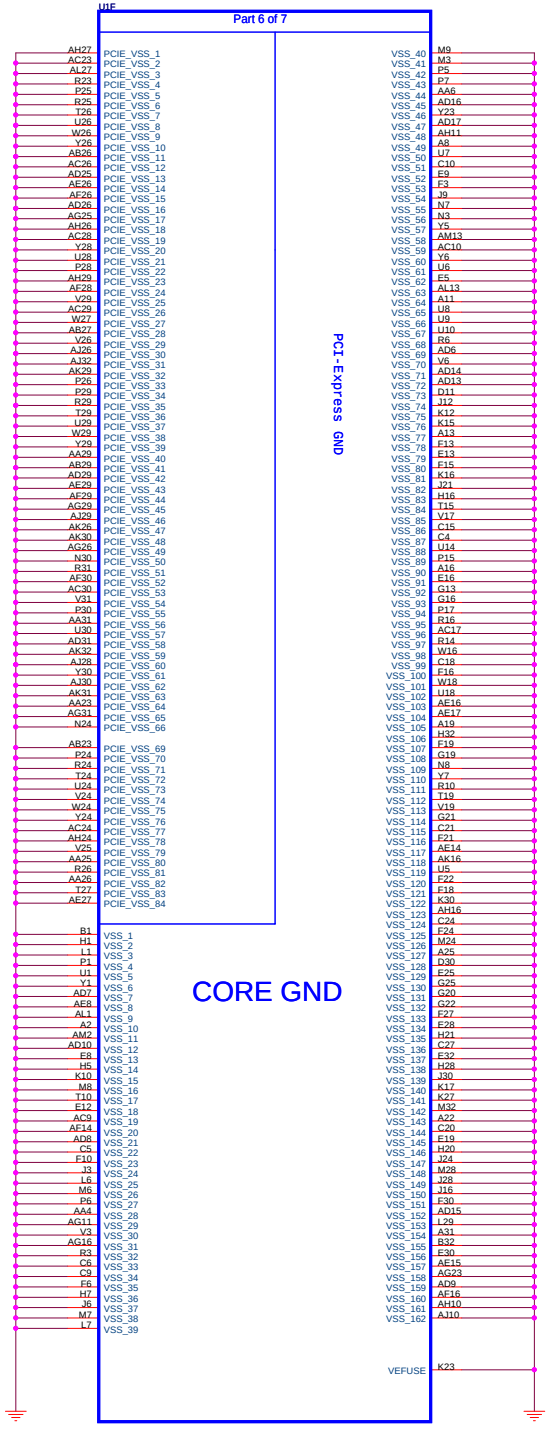

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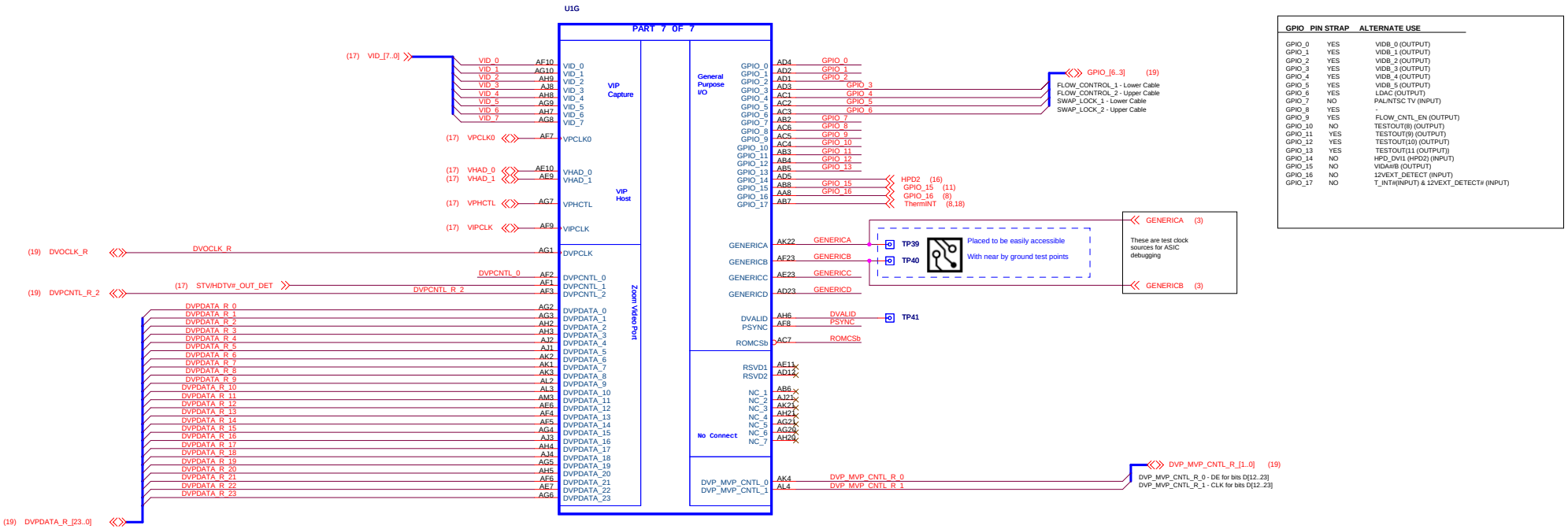
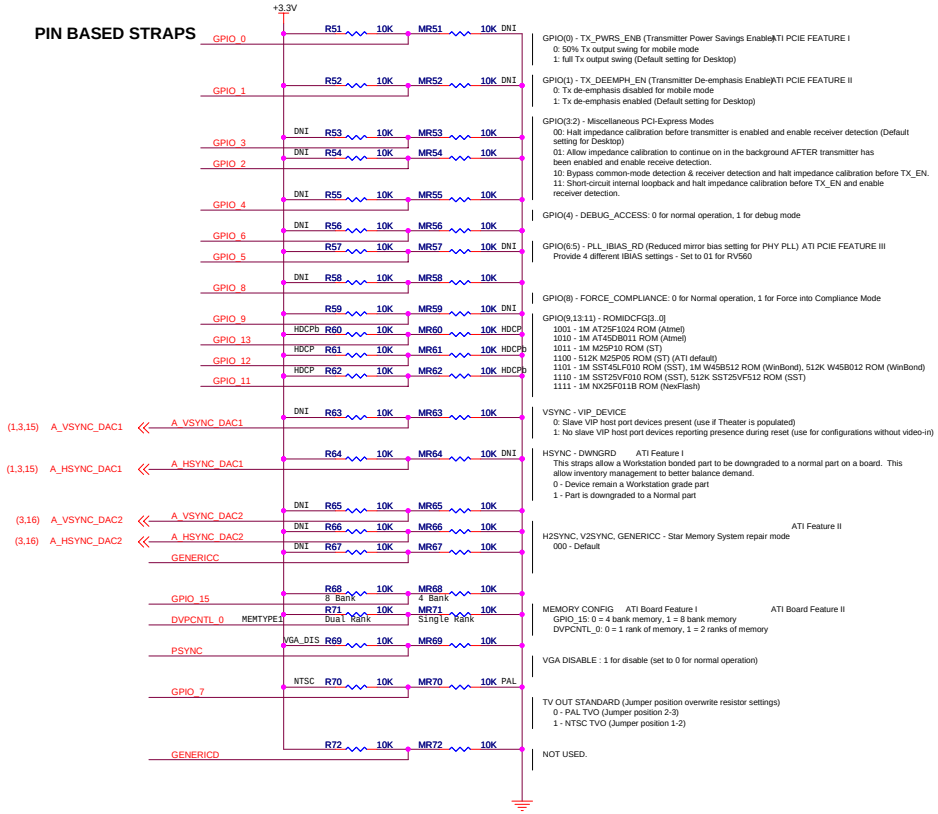
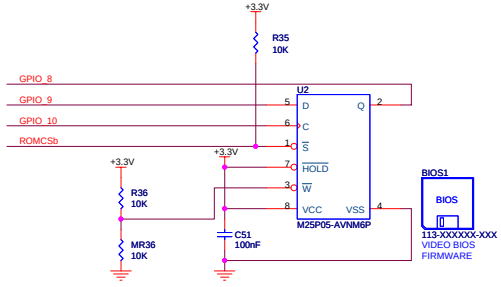


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDAstB (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

PIN BASED STRAPS





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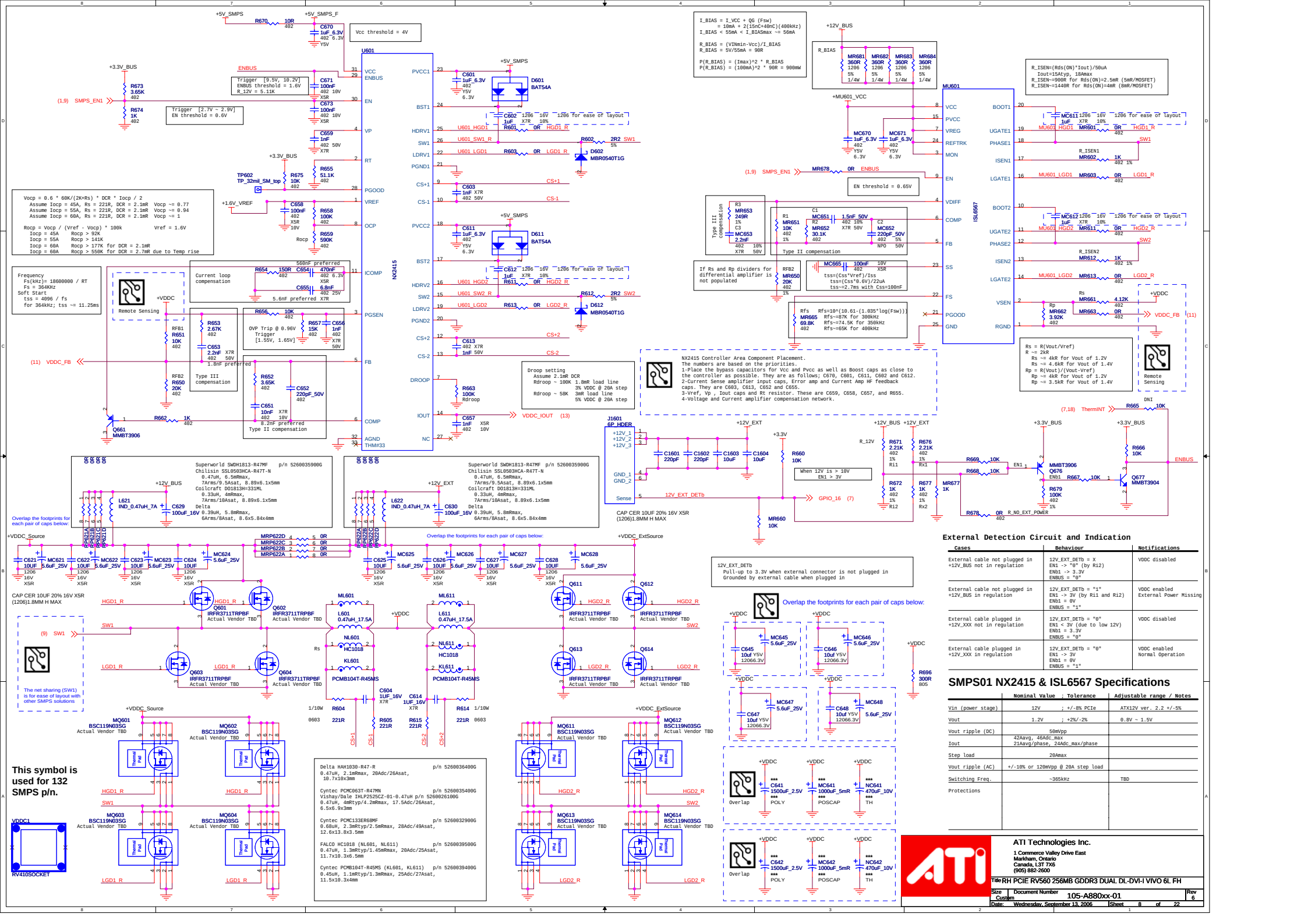
U601
NX2415
ISL6567
MU601
Vcc threshold = 4V
Trigger [9.5V, 10.2V]
ENBUS threshold = 1.6V
R_12V = 5.11K
Trigger [2.7V ~ 2.9V]
EN threshold = 0.6V
Vocp = 0.6 * 60K/(2K+Rs) * DCR * Iocp / 2
Assume Iocp = 45A, Rs = 221R, DCR = 2.1mR Vocp ~= 0.77
Assume Iocp = 55A, Rs = 221R, DCR = 2.1mR Vocp ~= 0.94
Assume Iocp = 60A, Rs = 221R, DCR = 2.1mR Vocp ~= 1
Rocp = Vocp / (Vref - Vocp) * 100k Vref = 1.6V
Iocp = 45A Rocp > 92K
Iocp = 55A Rocp > 141K
Iocp = 60A Rocp > 177K for DCR = 2.1mR
Iocp = 60A Rocp > 550K for DCR = 2.7mR due to Temp rise
Frequency
Fs(kHz)= 18600000 / RT
Fs = 364KHz
Soft Start
tss = 4096 / fs
for 364kHz; tss ~= 11.25ms
Droop setting
Assume 2.1mR DCR
Rdroop ~ 100K 1.8mR load line
3% VDDC @ 20A step
Rdroop ~ 58K 3mR load line
5% VDDC @ 20A step
I_BIAS = I_VCC + QG (Fsw)
= 10mA + 2(15nC+40nC)(400kHz)
I_BIAS < 55mA < I_BIASmax ~= 56mA
R_BIAS = (VINmin-Vcc)/I_BIAS
R_BIAS = 5V/55mA = 90R
P(R_BIAS) = (Imax)^2 * R_BIAS
P(R_BIAS) = (100mA)^2 * 90R = 900mW
R_ISEN=(Rds(ON)*Iout)/50uA
Iout=15Atyp, 18Amax
R_ISEN~=900R for Rds(ON)=2.5mR (5mR/MOSFET)
R_ISEN~=1440R for Rds(ON)=4mR (8mR/MOSFET)
Rs = R(Vout/Vref)
R ~= 2kR
Rs ~= 4kR for Vout of 1.2V
Rs ~= 4.6kR for Vout of 1.4V
Rp = R(Vout)/(Vout-Vref)
Rp ~= 4kR for Vout of 1.2V
Rp ~= 3.5kR for Vout of 1.4V
NX2415 Controller Area Component Placement.
The numbers are based on the priorities.
1-Place the bypass capacitors for Vcc and Pvcc as well as Boost caps as close to the controller as possible. They are as follows; C670, C681, C611, C602 and C612.
2-Current Sense amplifier input caps, Error amp and Current Amp HF feedback caps. They are C603, C613, C652 and C655.
3-Vref, Vp , Iout caps and Rt resistor. These are C659, C658, C657, and R655.
4-Voltage and Current amplifier compensation network.
Superworld SWDH1813-R47MF p/n 5260035900G
Chilisin SSL0503HCA-R47T-N
0.47uH, 6.5mRmax,
7Arms/9.5Asat, 8.89x6.1x5mm
Coilcraft DO1813H=331ML
0.33uH, 4mRmax,
7Arms/10Asat, 8.89x6.1x5mm
Delta
0.39uH, 5.8mRmax,
6Arms/8Asat, 8.6x5.84x4mm
CAP CER 10UF 20% 16V X5R
(1206)1.8MM H MAX
Overlap the footprints for each pair of caps below:
12V_EXT_DETb
Pull-up to 3.3V when external connector is not plugged in
Grounded by external cable when plugged in
When 12V is > 10V
EN1 > 3V
External Detection Circuit and Indication
Cases
Behaviour
Notifications
External cable not plugged in +12V_BUS not in regulation
12V_EXT_DETb = X
EN1 -> "0" (by Ri2)
ENb1 -> 3.3V
ENBUS = "0"
VDDC disabled
External cable not plugged in +12V_BUS in regulation
12V_EXT_DETb = "1"
EN1 -> 3V (by Ri1 and Ri2)
ENb1 = 0V
ENBUS = "1"
VDDC enabled
External Power Missing
External cable plugged in +12V_XXX not in regulation
12V_EXT_DETb = "0"
EN1 < 3V (due to low 12V)
ENb1 = 3.3V
ENBUS = "0"
VDDC disabled
External cable plugged in +12V_XXX in regulation
12V_EXT_DETb = "0"
EN1 -> 3V
ENb1 = 0V
ENBUS = "1"
VDDC enabled
Normal Operation
SMPS01 NX2415 & ISL6567 Specifications
Nominal Value ; Tolerance
Adjustable range / Notes
Vin (power stage) 12V ; +/-8% PCIe ATX12V ver. 2.2 +/-5%
Vout 1.2V ; +2%/-2% 0.8V ~ 1.5V
Vout ripple (DC) 50mVpp
Iout 42Aavg, 46Adc_max 21Aavg/phase, 24Adc_max/phase
Step load 20Amax
Vout ripple (AC) +/-10% or 120mVpp @ 20A step load
Switching Freq. ~365kHz TBD
Protections
This symbol is used for 132 SMPS p/n.
RV410SOCKET
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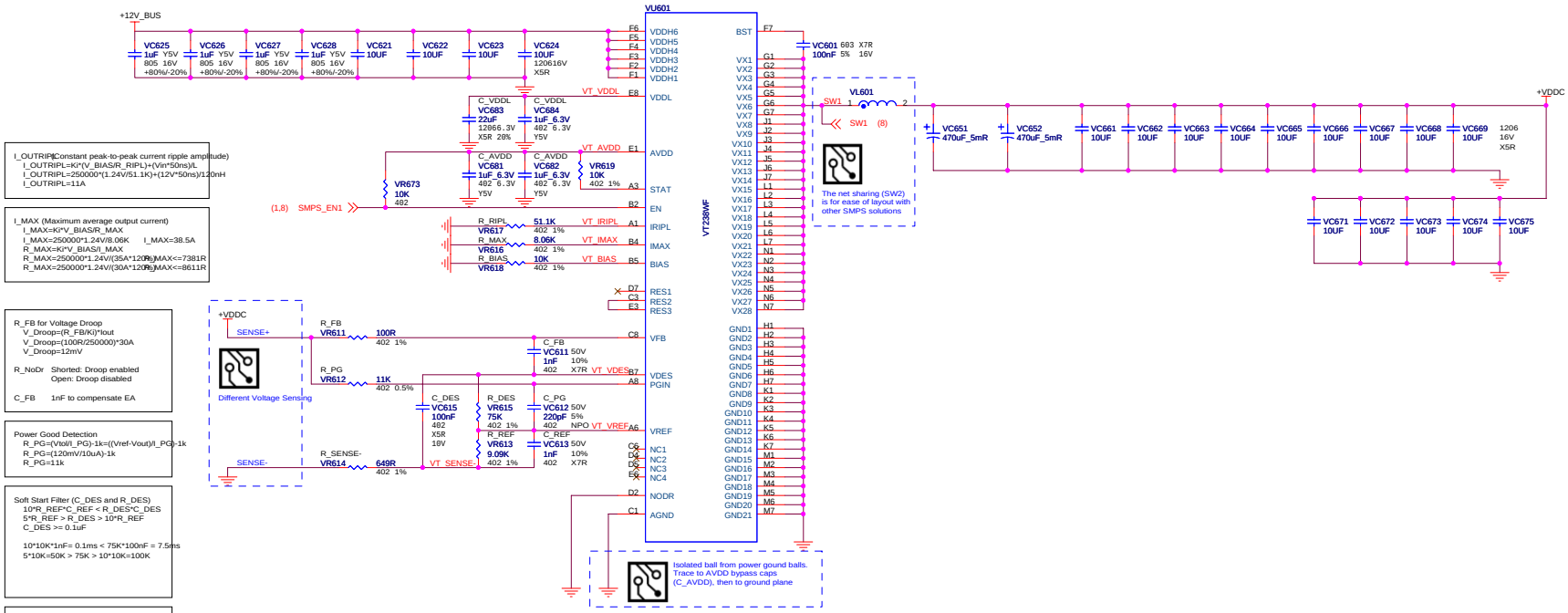

I_OUTRIPL (Constant peak-to-peak current ripple amplitude)
I_OUTRIPL=Ki*(V_BIAS/R_RIPL)+(Vin*50ns)/L
I_OUTRIPL=250000*(1.24V/51.1K)+(12V*50ns)/120nH
I_OUTRIPL=11A

I_MAX (Maximum average output current)
I_MAX=Ki*V_BIAS/R_MAX
I_MAX=250000*1.24V/8.06K I_MAX=38.5A
R_MAX=Ki*V_BIAS/I_MAX
R_MAX=250000*1.24V/(35A*120Rg) I_MAX<=7381R
R_MAX=250000*1.24V/(30A*120Rg) I_MAX<=8611R

R_FB for Voltage Droop
V_Droop=(R_FB/Ki)*Iout
V_Droop=(100R/250000)*30A
V_Droop=12mV

R_NoDr Shorted: Droop enabled
Open: Droop disabled

C_FB 1nF to compensate EA

Power Good Detection
R_PG=(Vtol/I_PG)-1k=((Vref-Vout)/I_PG)-1k
R_PG=(120mV/10uA)-1k
R_PG=11k

Soft Start Filter (C_DES and R_DES)
10*R_REF*C_REF < R_DES*C_DES
5*R_REF > R_DES > 10*R_REF
C_DES >= 0.1uF

10*10K*1nF= 0.1ms < 75K*100nF = 7.5ms
5*10K=50K > 75K > 10*10K=100K

V Reference
V_REF=124uA*(R_REF+R_SENSE-)
V_REF=124uA*(9.09K+649R)
V_REF~=1.208V

VDDC	R_REF	ATI p/n
1.2V		
1.3V		
1.4V		

SMPS01 Volterra Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	1.2V ; +2%/-2%	0.8V ~ 1.5V
Vout ripple (DC)	50mVpp	
Iout	30Aavg, 35Adc_max	
Step load	20Amax	
Vout ripple (AC)	+/-10% or 120mVpp @ 20A step load	
Switching Freq.	1MHz	100ns on time minimum
Protections	UVLO [9.5V, 10.1V] OVLO [13.4V, 14.1V] OTP [120degCj 150degCj] OCP/SCP IMAX	

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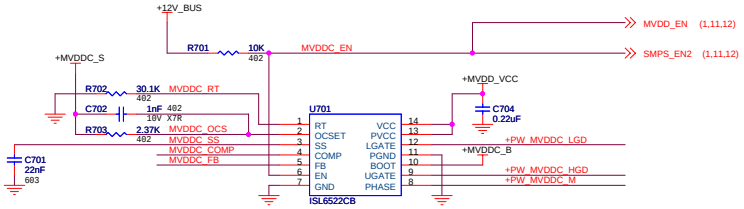
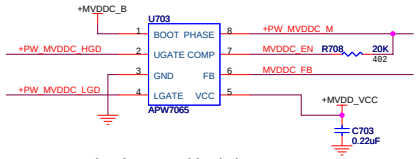


List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7074 (12V)
CAT CAT7522/CAT7523
INTERSIL ISL6522/ISL6535
RICHTEK RT9232/RT9232A/RT9232B

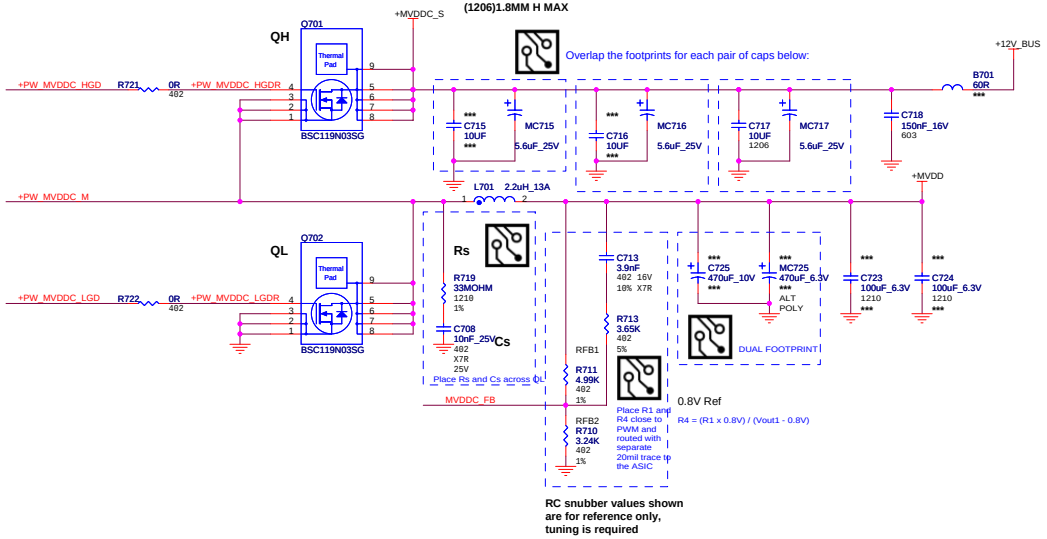


List of supported foodprint

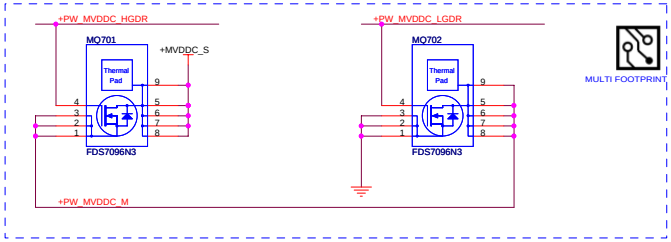
The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7120/APW7065 (12V)
CAT CAT7583 (12V)
INTERSIL ISL6545
NEXSEM NX2114/2307
RICHTEK RT9214/RT8101
OnSemi ON1582

CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX



RC snubber values shown are for reference only, tuning is required



SMPS02- Regulator for MVDD

Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G

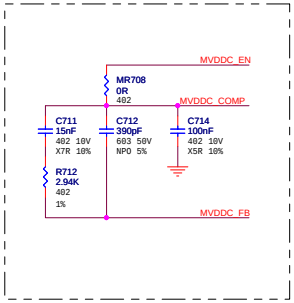
Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

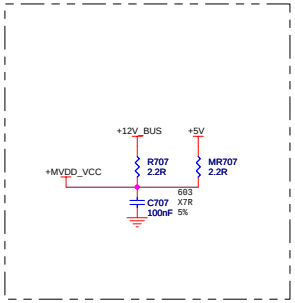
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

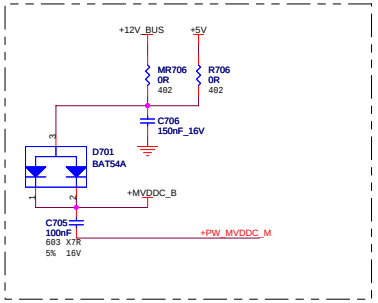
COMPENSATION CIRCUIT



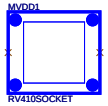
FILTERED SMPS VCC



BOOT CIRCUIT



This symbol is used for 132 SMPS p/n.



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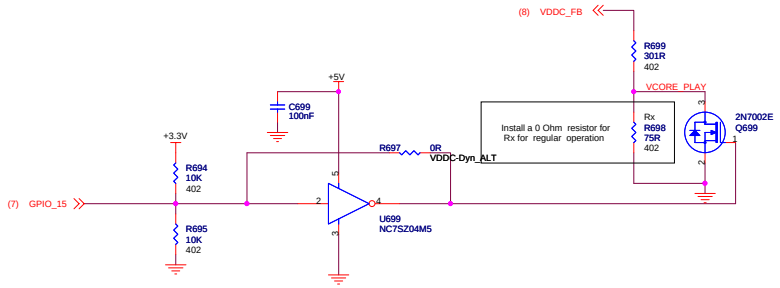
Option for Dynamic VDDC



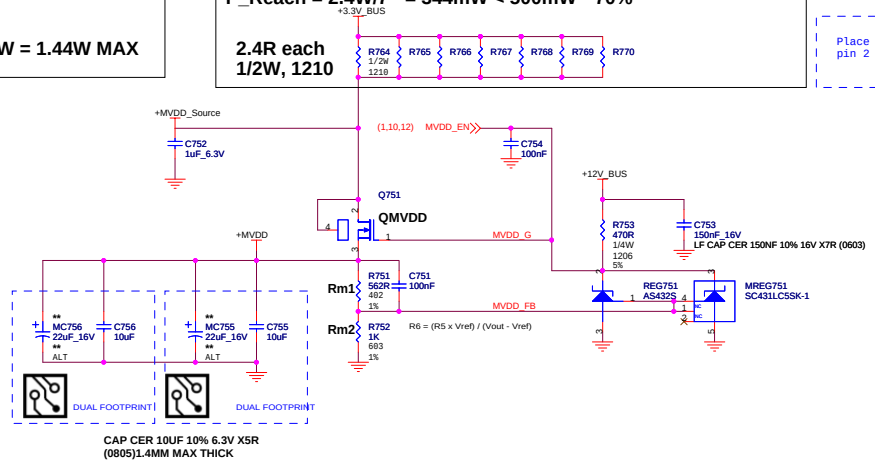
Regulator for +MVDDQ
(if total consumption on 3.3V PCIe allows)
Vout = 1.85V ~ 2.2V
P_QVDD = (3.3V-1.85V)*2.65A - 2.4W = 1.44W MAX

Must be adjusted per memory voltage & current requirement

Req = 2.4R/7 = 0.34R
P_Req = 0.34R * 2.65^2 = 2.4W
P_Reach = 2.4W/7 ~= 344mW < 500mW * 70%

2.4R each 1/2W, 1210

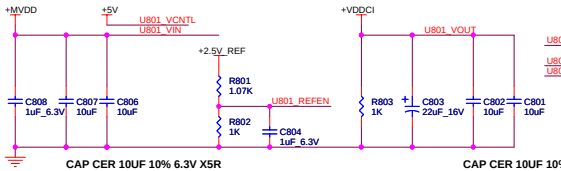
Place Big Copper Area Under QMVDD pin 2 and 4 for Heat Dissipation.



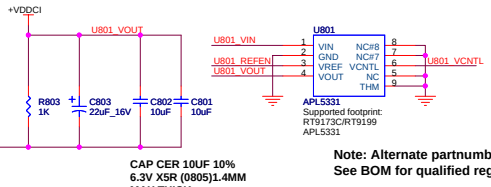
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

Voltage Req.	Rm1		Rm2		
2.85V					
2.55V	22.1R	316022R100G	1.1K	3240110100G	2.5V Ref.
2.5V	0R	3150000000	DNI		2.5V Ref.
2.1V min	681R	3160681000G	953R	3240953000	1.24V Ref.
2.0V min	681R	3160681000G	1.1K	3240110100G	1.24V Ref.
1.9V min, 1.94V nom.	562R	3160562000G	1K	3160100100G	1.24V Ref.

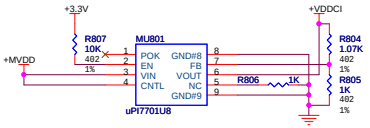
Optional Regulator for +VDDCI
Vout = 1.2V ~ 1.4V



CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK



CAP CER 10UF 10%
6.3V X5R (0805)1.4MM
MAX THICK



Note: Alternate partnumbers are provided as possible choices only.
See BOM for qualified regulators/vendors. Not all combinations are tested.

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Optional regulator for +PCIE
Vout = 1.2V ~1.25V

Note: Alternate partnumbers are provided as possible choices only.
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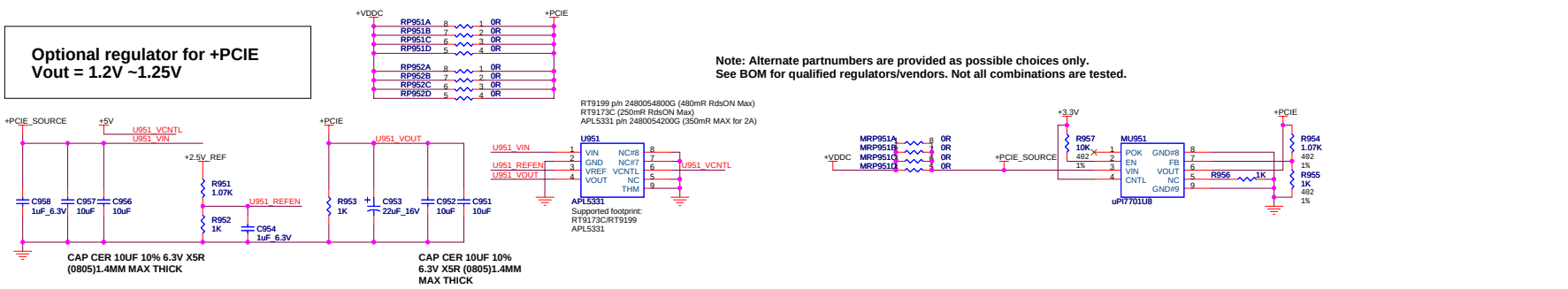
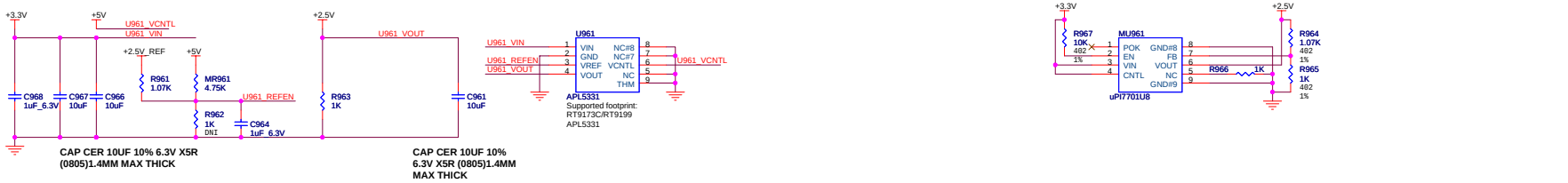
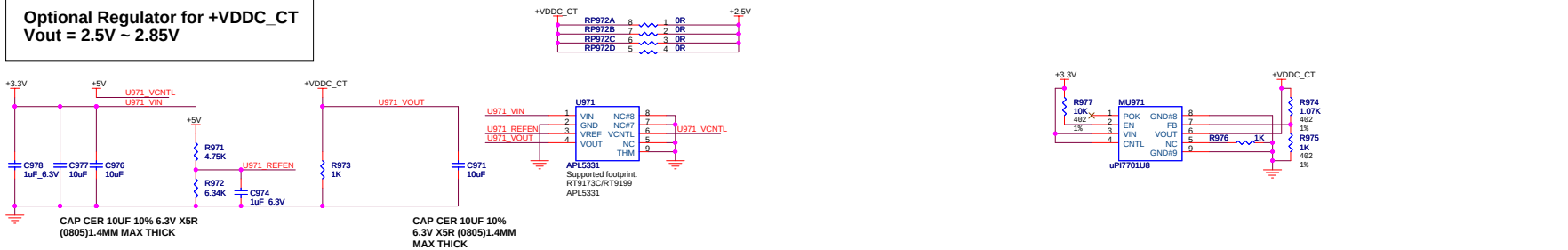
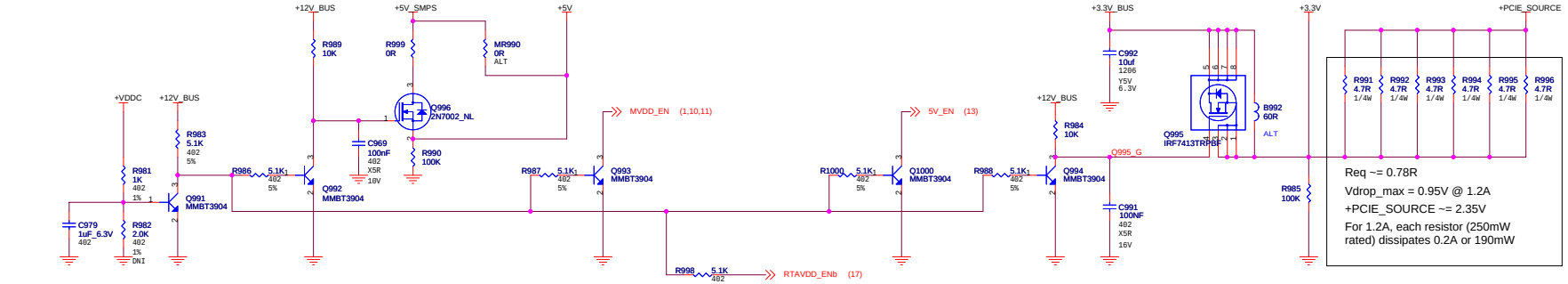


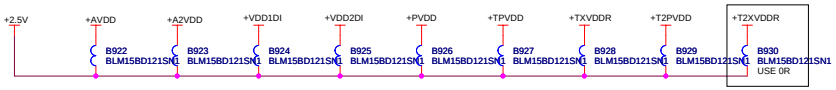
Optional regulator for +2.5V
Vout = 2.5V



Optional Regulator for +VDDC_CT
Vout = 2.5V ~ 2.85V







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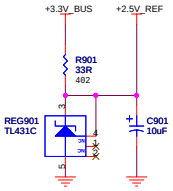
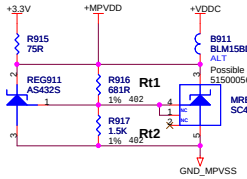
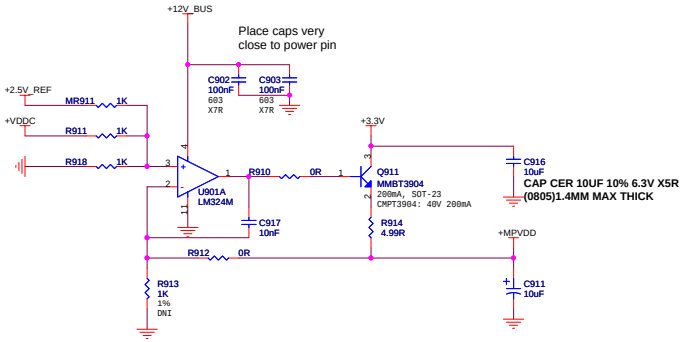
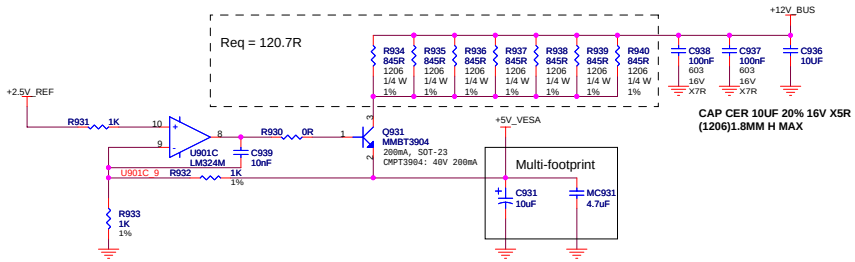


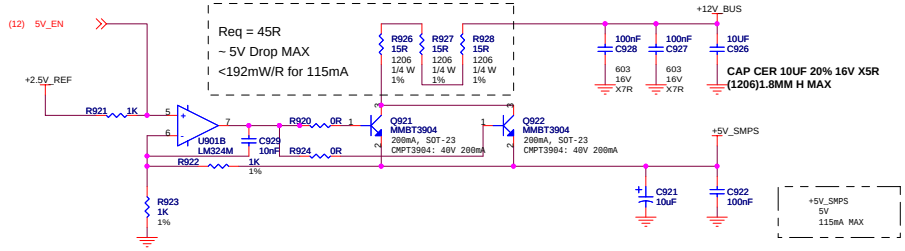
Alt regulator for +MPVDD
Vout = 1.2V (not tracking to VDDC)
Iout = 10mA MAX

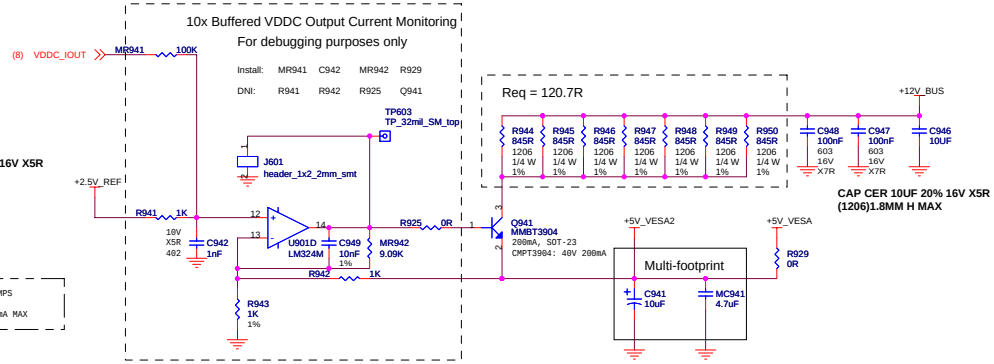


	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100









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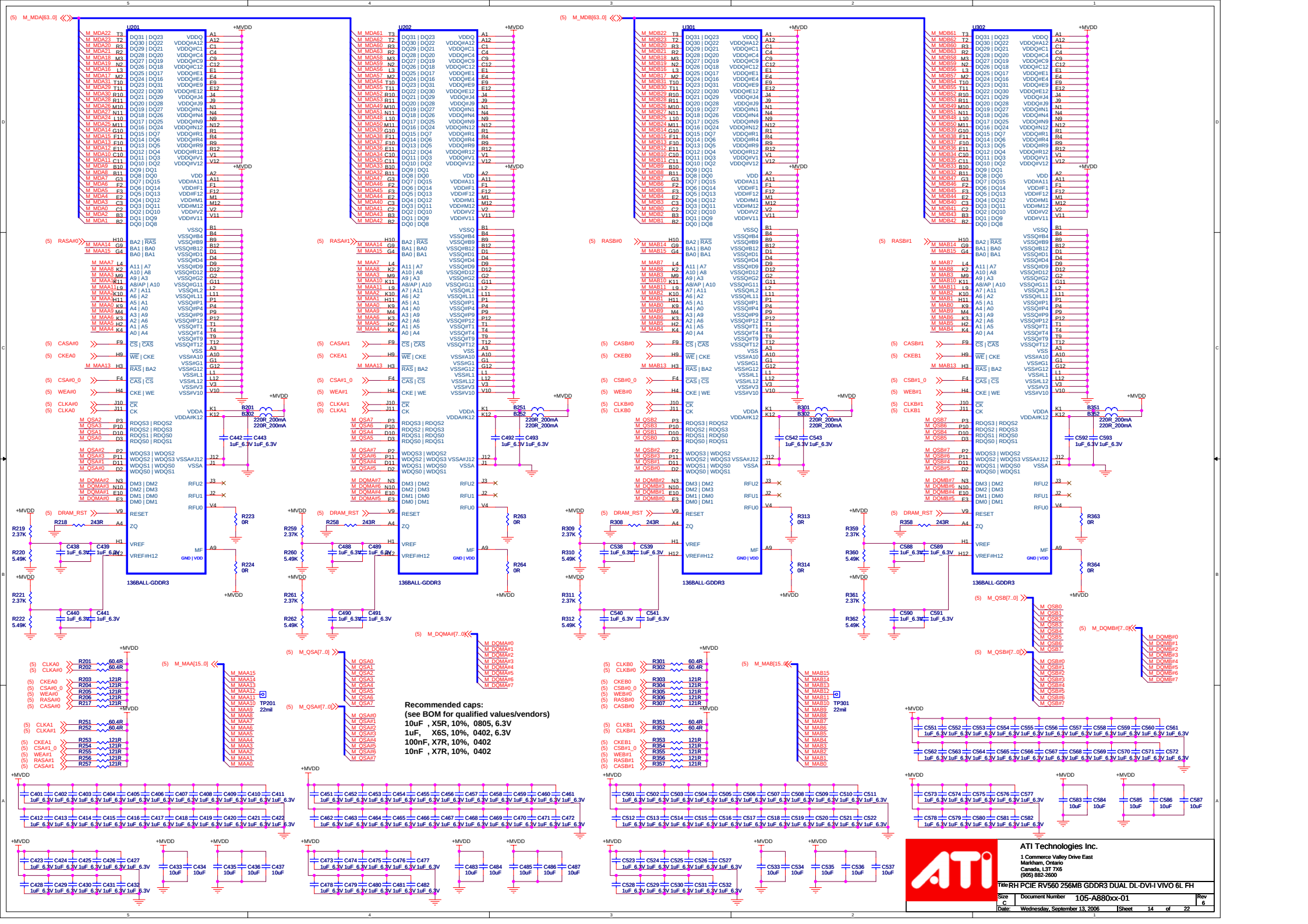
U201
U202
U301
U302
136BALL-GDDR3
+MVDD
M_MDA[63..0]
M_MDB[63..0]
RASA#0
RASA#1
RASB#0
RASB#1
CASA#0
CASA#1
CASB#0
CASB#1
CKEA0
CKEA1
CKEB0
CKEB1
WEA#0
WEA#1
WEB#0
WEB#1
CSA#0_0
CSA#1_0
CSB#0_0
CSB#1_0
CLKA0
CLKA#0
CLKA1
CLKA#1
CLKB0
CLKB#0
CLKB1
CLKB#1
DRAM_RST
M_QSA[7..0]
M_QSB[7..0]
M_DQMA#[7..0]
M_DQMB#[7..0]
M_MAA[15..0]
M_MAB[15..0]
TP201
TP301
22mil
B201
B202
B251
B252
B301
B302
B351
B352
220R_200mA
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X5R, 10%, 0805, 6.3V
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402
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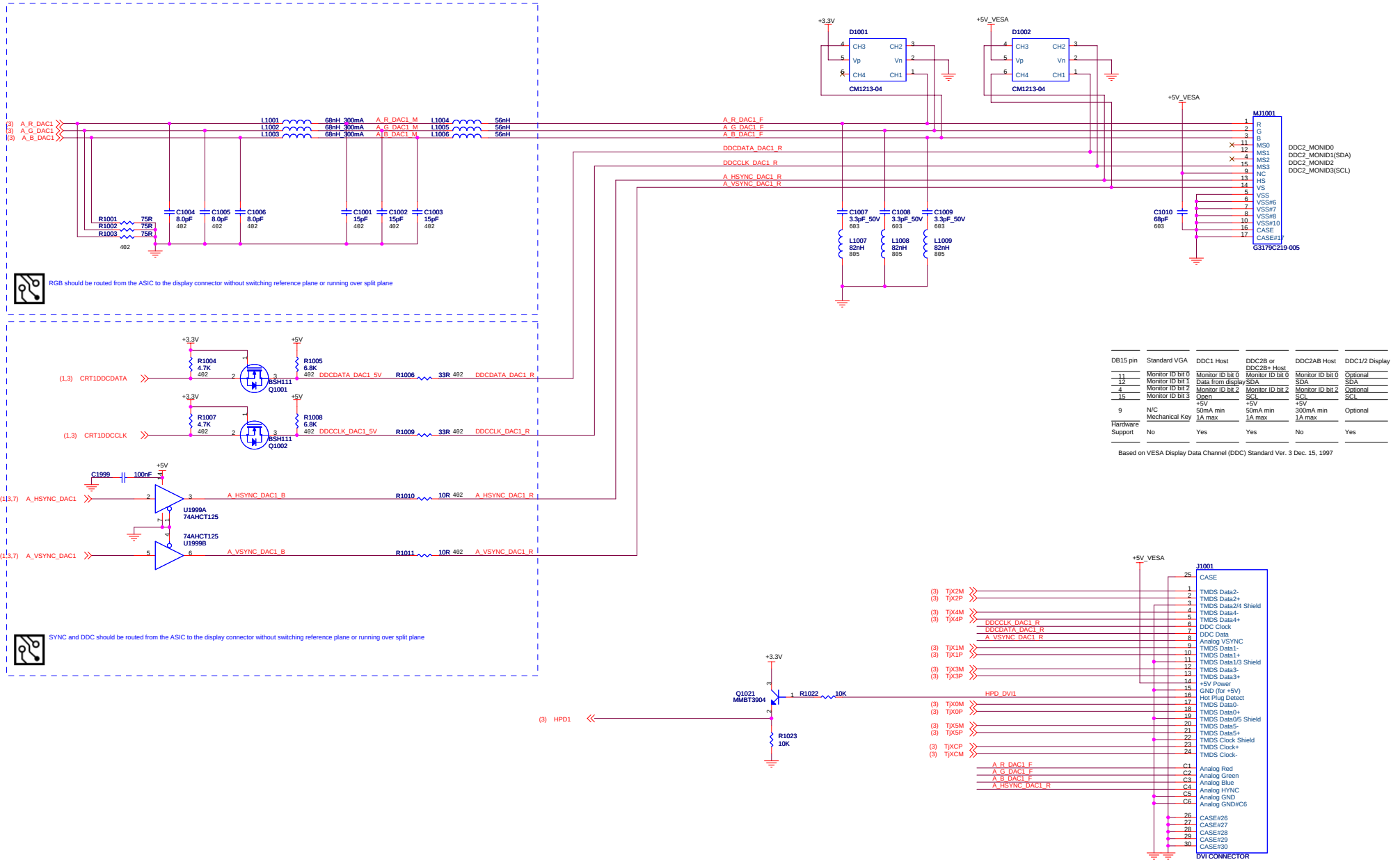

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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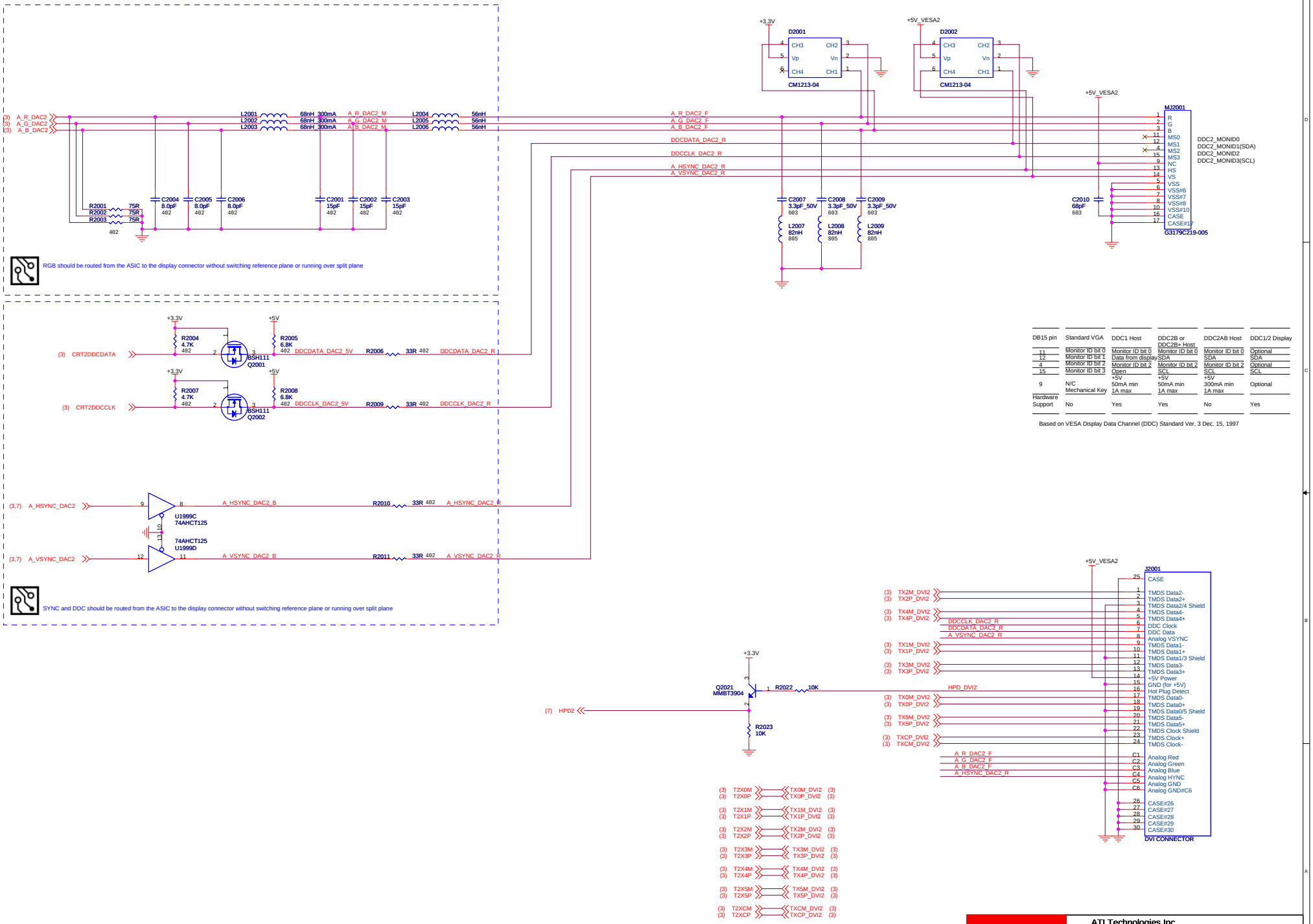

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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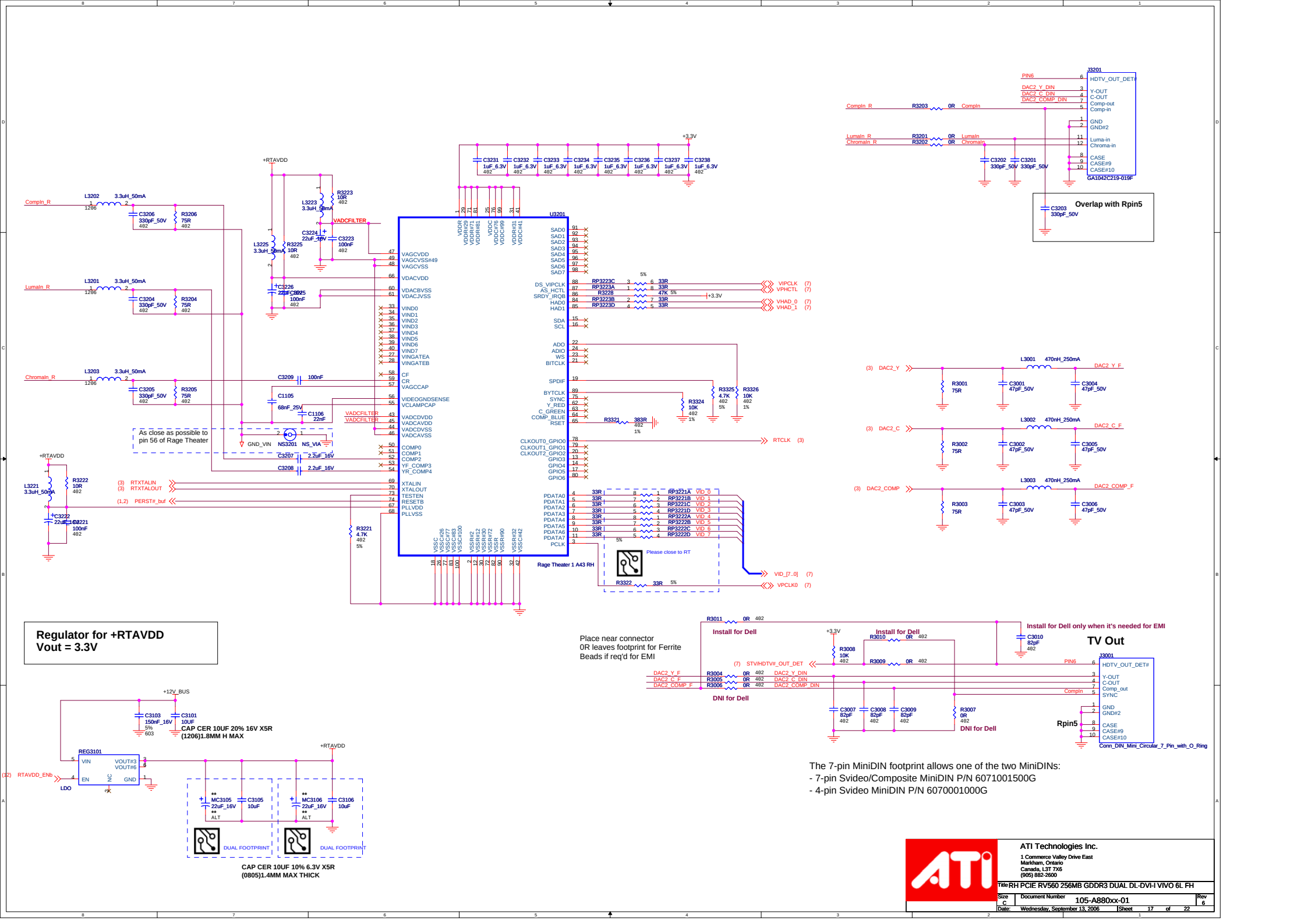
Regulator for +RTAVDD
Vout = 3.3V
Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI
TV Out
Overlap with Rpin5
As close as possible to
pin 56 of Rage Theater
Rage Theater 1 A43 RH
Please close to RT
DUAL FOOTPRINT
DUAL FOOTPRINT
CAP CER 10UF 20% 16V X5R
(1206)1.8MM H MAX
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK
Install for Dell
Install for Dell
Install for Dell only when it's needed for EMI
DNI for Dell
DNI for Dell
The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G
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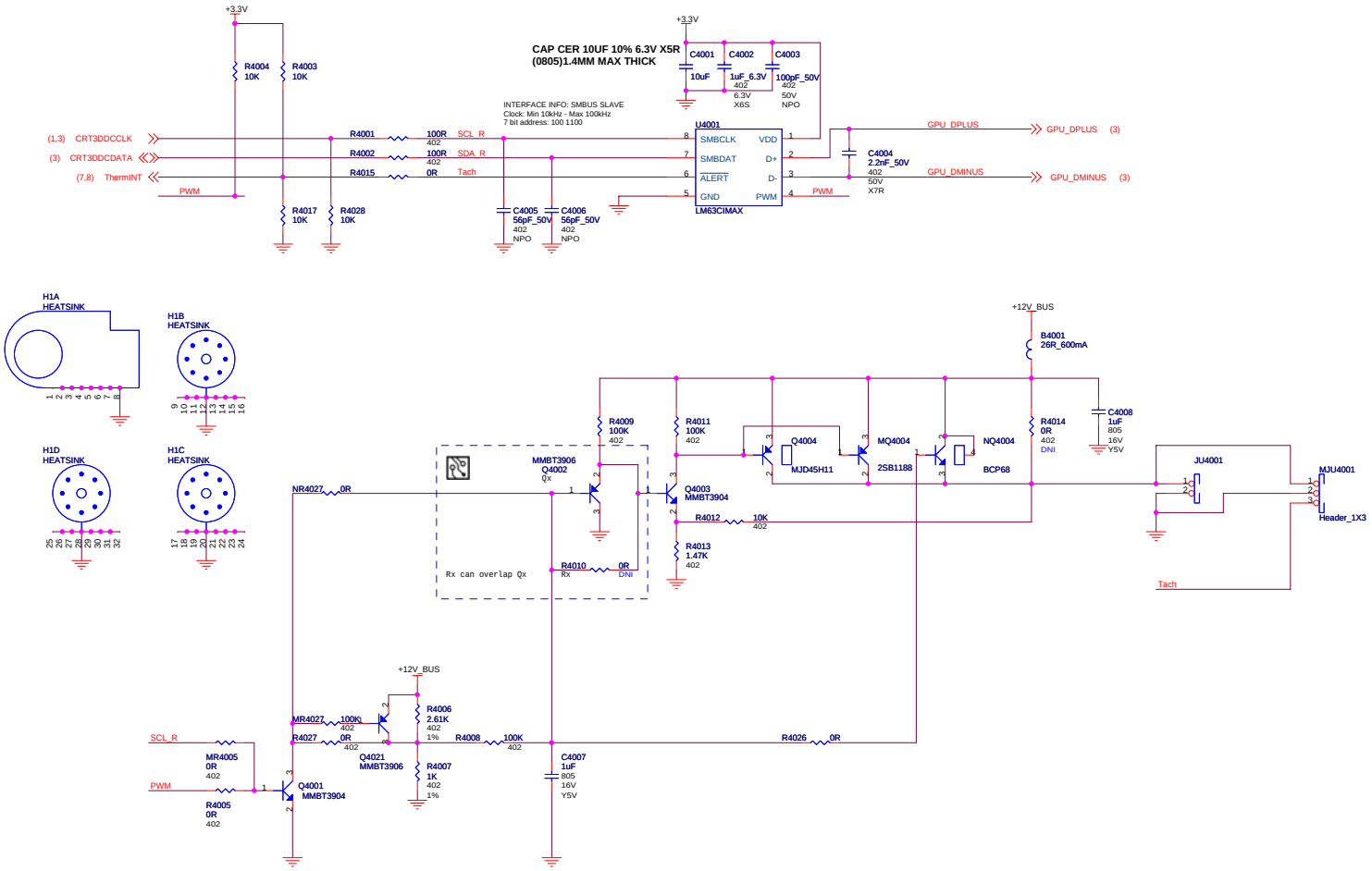

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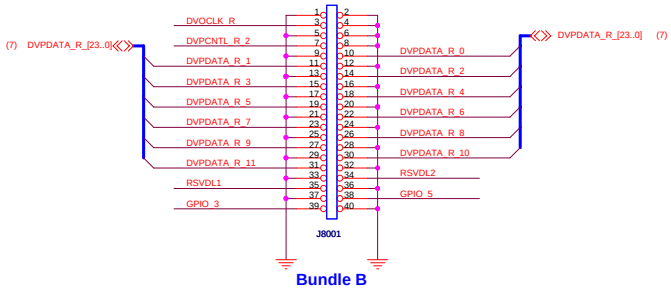
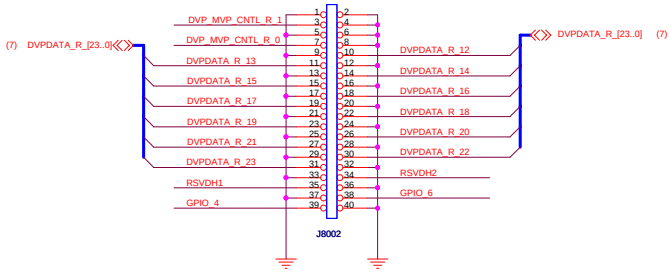
CrossFire Card-Edge

Lower Cable Card Edge

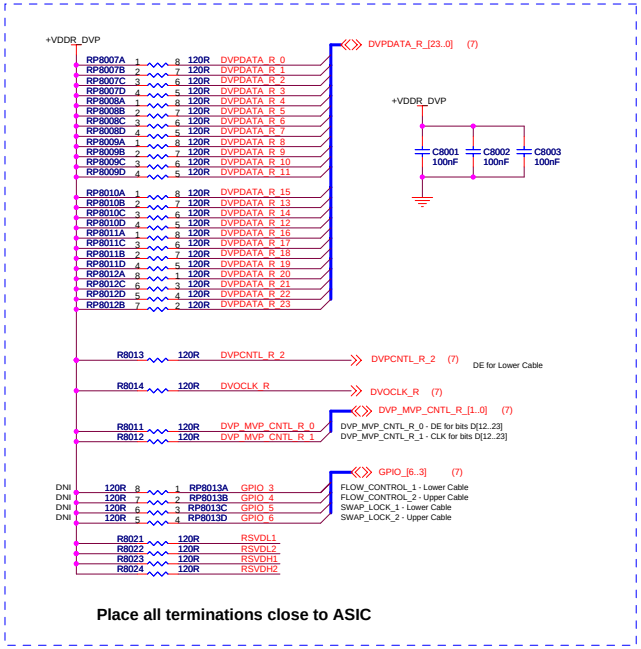


Bundle B

Upper Cable Card Edge

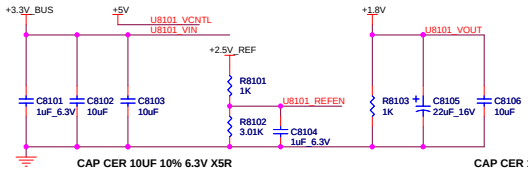


Bundle A



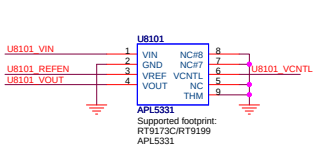
Place all terminations close to ASIC

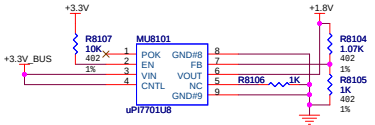
Optional regulator for +1.8V
Vout = 1.8V
Iout = 1A MAX
P = 1W MAX



CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK





Note: Alternate partnumbers are provided as possible choices only.
See BOM for qualified regulators/vendors. Not all combinations are tested.

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DVI/DVI SCREWS with top tab

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

BKT
BRACKET
8020042500G

ASSY1
ANTISTATIC
BAG
6_X_11

MT1
MT_Hole_0.136_in.

MT2
MT_Hole_0.136_in_6VIA

DNI
SK1
RV410SOCKET

PCB1
PCB
109-GN982-00A

<Variant Name>

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(905) 882-2600

Title	RH PCIE RV560 256MB GDDR3 DUAL DL-DVI-I VIVO 6L FH	
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<variant Name>

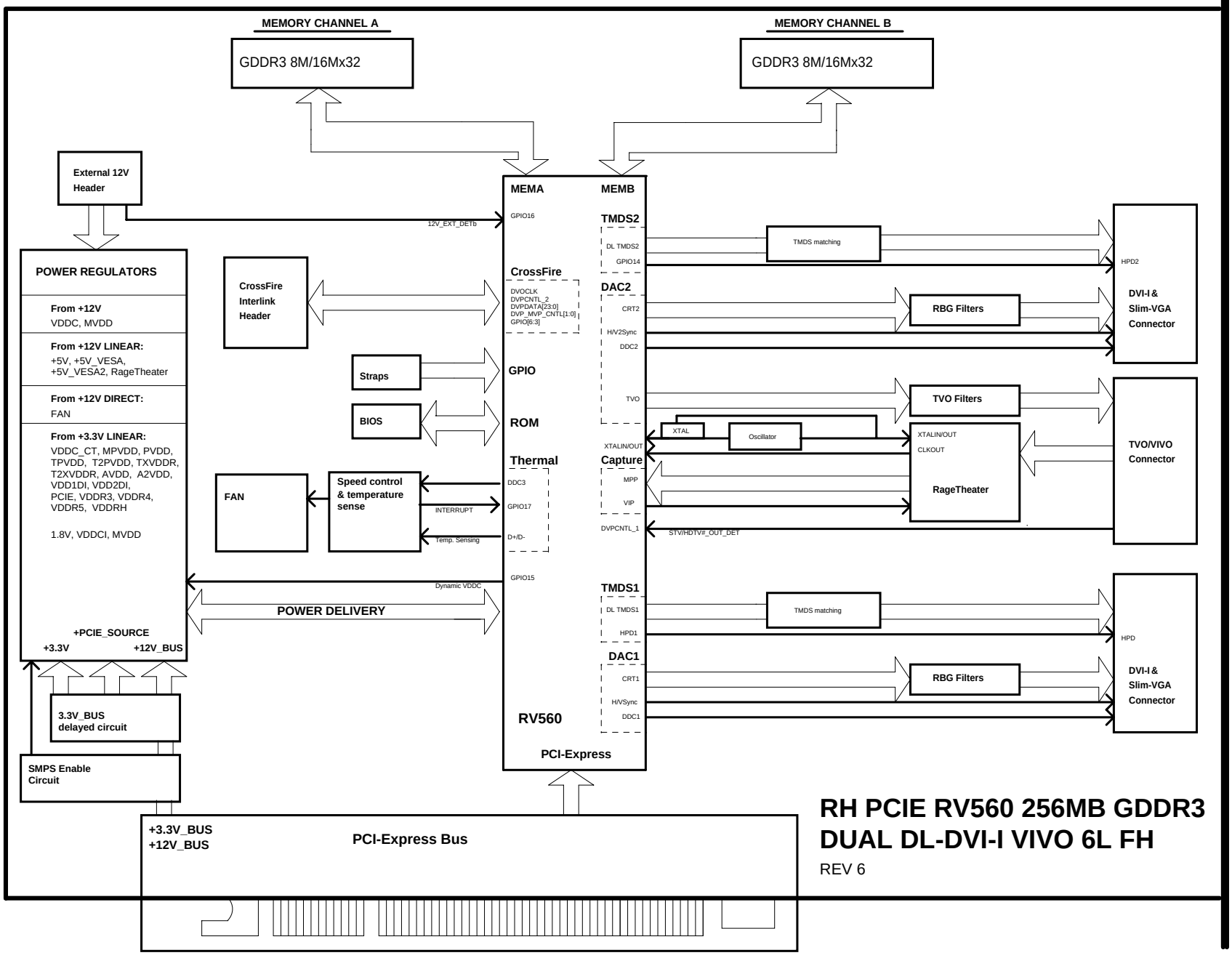
Title	Schematic No.	Date:
RH PCIE RV560 256MB GDDR3 DUAL DL-DVI-I VIVO 6L FH	105-A880xx-01	Saturday, August 26, 2006

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact ATI representative to obtain latest BOM closest to the application desired.**

Rev 6

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/02/27	Design based on 105/109-A671xx-20 (pg 03) Change TMDS power decouplings, change crystal/oscillator sharing circuit (pg 04) Change VDDR4/VDDR5 to have 1.8V/3.3V option , Separate VDDCI from VDDC option, add decoupling for VDDC and VDDCI (pg 07) Connect DVO to CrossFire Edge Connector, change pin straps matching RV570, remove PAL/NTSC header, H/W FPGA Crossfire (pg 08) New SMPS Tile (A800-00A-46) for RV560 VDDC 46A solution (pg 09) New SMPS Tile (A800-00A-30_VT) for RV560 VDDC 30A solution (pg 10) New SMPS Tile (A800-00A-8) for RV560 MVDD 8A solution (pg 11) Remove 1.8V regulator, LED for Dyn. VDDC, add VDDCI regulator (pg 12) Improve power sequencing and +5V sequencing from +5V_SMPS, add LDO new footprints, remove MVDD to 2.5V short (pg 13) Remove +5V_EN, change +5V to +5V_SMPS with current up to 115mA, add VDDC output current monitoring for debugging (pg 15) Remove H/W FPGA CrossFile options, change ESD protection to +5V_VESA (pg 16) Remove H/W FPGA CrossFile options and chnage ESD protetion to +5V_VESA2 (pg 17) Change RTAVDD regulator for power sequencing, add Dell specific TVO mapping (pg 18) Update fan control for other thermal monitoring IC options (pg 19) Add CrossFire Edge Connectors and 1.8V regulator
1	00B	06/03/06	Fix DFM issues on layout (pg 03/07) Add clock source to GenericA/B for ASIC debugging (pg 13) Add J601 for ease of bring up for VDDC current monitoring
2	00C	06/05/08	(pg 03) Add MR25 and C61 for VREFG (pg 03) Change GND_TXVSSR and GND_T2XVSSR directly to GND (pg 08) Remove VR650, VR663, MR676, MR677, MR673, MU678 and U678, modify BUSEN and share it to MU601 (pg 08) Remove redundant external detection circuits (pg 11) Replace RP801 with B801~B803 (pg 11) Add resistors to dissipate Q_MVDD, sourced from 3.3V_BUS (pg 12) Add RP952 for PCIE VDDC share, add 5V_EN, remove Q998 for RTAVDD_ENb (pg 13) Add Q922 for improved power dissipation, use series R926~R928 dissipation and add 5V_EN option (pg 17) Replace RTAVDD regulator with AP1118 (pg 19) Crossfire pin mapping change, 50R impedance matched (Layout) Power distribution layout change (Layout) TMDS1 and TMDS2 termination resistor changes
3	00D	06/06/20	(pg 08) Updating MU601 symbol to swap pin# 5 and 6 (pg 08) Adding inductors NL601, NL611, KL601 and KL611
3	00D	06/06/29	Title and text correction on multiple pages (but no net list or design change).
4	00E	06/07/17	(pg 08) Adding R660, MR660 and MR677 (pg 11) Updating symbol for MU801 (pg 12) Updating symbol for MU951, MU961, MU971 (pg 19) Updating symbol for MU8101 (pg 17) Updating symbol for REG3101 (Layout) Changing location of R25/MR25. (Layout) Routing of Y81 pin4 and removing extra stubs at CrossFire edge connector on L4 (pg 18) Updating H1 and H2 symbols (pg 49) Updating/Adding miscellaneous symbols (pg 08) Adding MC621, MC622, MC623, MC624, MC625, MC626, MC627, MC628, MC645, MC646, MC647, and MC648 (pg 09) Removing VC670 (pg 10) Adding MC715, MC716 and MC717 (pg 08) Changing C604 and C614 from 0402/X5R to 0603/X7R/16V, and changing R604 and R614 to 0603, 1/10W
5	00	06/08/23	(pg 08) Changing BUSEN net label to ENBUS (pg 07) Removing series resistors on CrossFire signals (RP8001 to RP8006, R8001 to R8004, RP13) (Layout) Updating routing design rules for length matching and spacing on CrossFire signals (Layout) Adjusting MAA11 U1-U201 length (Layout) Addressing DFM issues
6	01	06/08/25	(Layout) Updating routing design rules for length matching and spacing on CrossFire DVP_MVP_CNTL_R_[1..0] signals



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REV 6

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