

P527-A00 DESI GN -- G72/G73, 256/128MB 128/64BI T DDR2, DUAL-VGA

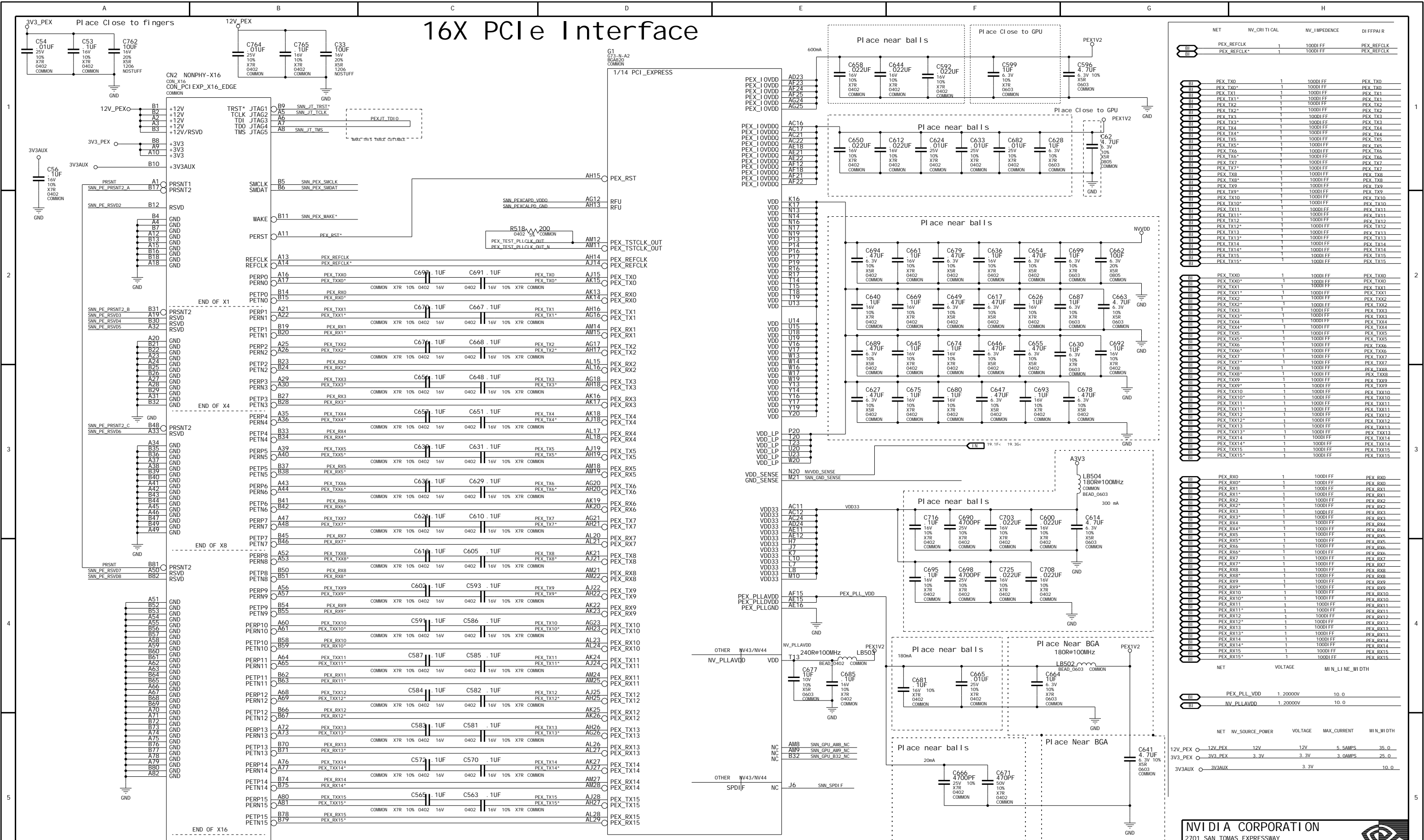
PAGE SUMMARY:

- Page 1: TABLE OF CONTENTS & REVISION HISTORY  
Page 2: PCI EXPRESS 16X, NVVDD DECOUPLING CAPS, PEX\_I OVDD/Q DECOUPLING CAPS  
Page 3: FBA MEMORY INTERFACE, GPU FBVDD/Q DECOUPLING CAPS, FBVTT TERMINATION  
Page 4: FBA 16Mx16 DDR2 MEMORIES, 1ST BANK 0..31  
Page 5: FBA 16Mx16 DDR2 MEMORIES, 1ST BANK 32..63  
Page 6: FBC MEMORY INTERFACE, GPU FBVTT, FBVDDQ  
Page 7: FBC 16MX16 DDR2 MEMORIES, 2ND BANK 0..31  
Page 8: FBC 16Mx16 DDR2 MEMORIES, 2ND BANK 32..63  
Page 9: DACA FILTERS, DACA SYNC BUFFERS  
Page 10: DACC B / DACC FILTERS, DACC SYNC BUFFERS  
Page 11: TMDS LINK A & LINK B INTERFACES  
Page 12: TMDS LINK C&D INTERFACE  
Page 13: MIOA & MIOB INTERFACES  
Page 14: CUSTOM VGA PASS THRU X4PCI E EDGE CONNECTOR  
Page 15: GPU GND CONNECTION, XTAL  
Page 16: JTAG, BIOS ROM, HDCP ROM, FAN CONTROL, GPIO  
Page 17: BIOS STRAPS & MECHANICALS  
Page 18: POWER SUPPLY I: 5V, A3V3  
Page 19: POWER SUPPLY II: NVVDD, A2V5  
Page 20: POWER SUPPLY III: FBVDDQ, PEX1V2

G72 SKU

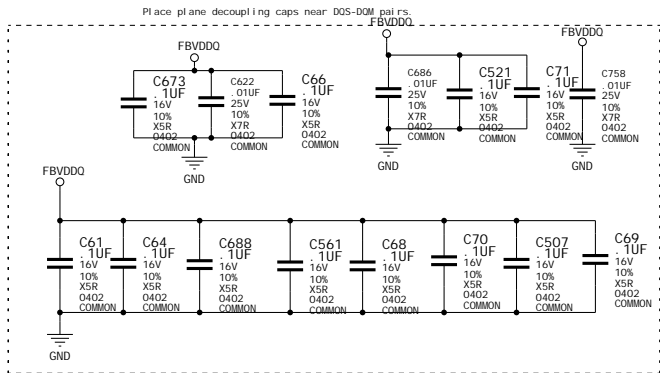
SKU	VARI ANT	NVPN	ASSEMBLY
B	BASE	600-10527-0000-A00	G72 400/400MHz 256MB 128-bit DDR2 16MX16 DUAL-VGA
1	0000	600-10527-0000-000	G72 400/400MHz 256MB 128BIT DDR2 16MX16 DUAL VGA
2	<UNDEFI NED>	<UNDEFI NED>	<UNDEFI NED>
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# 16X PCIe Interface

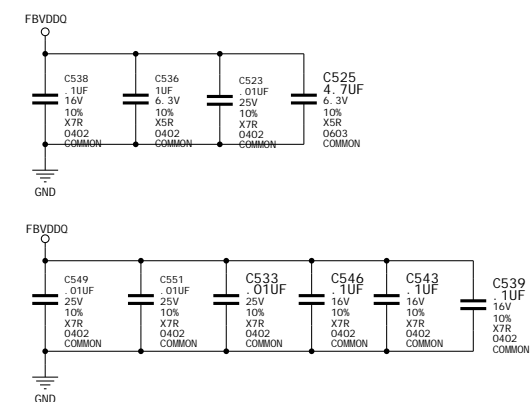
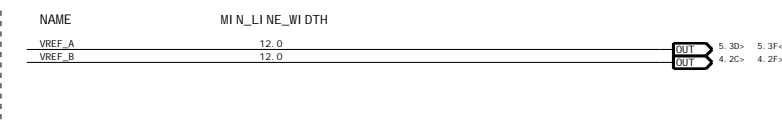





PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

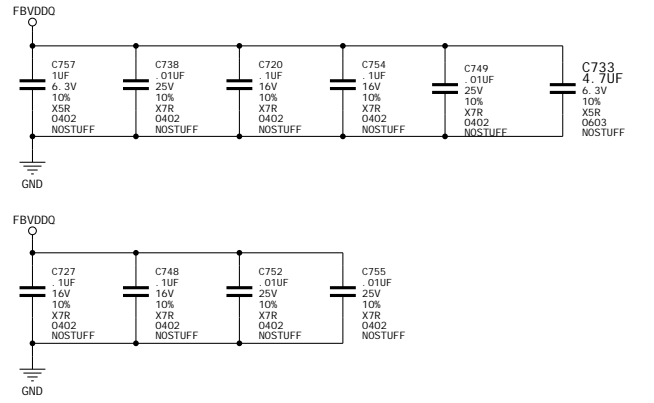
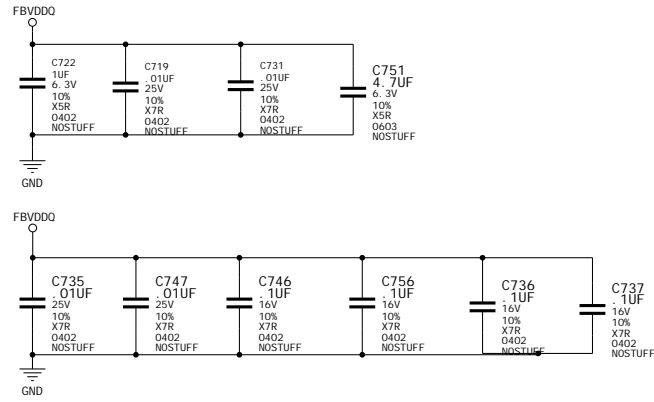



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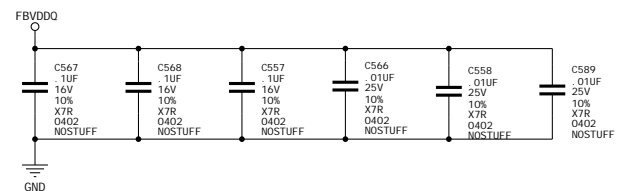
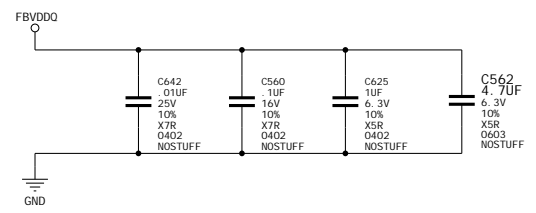
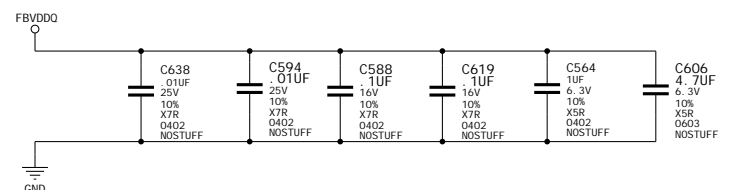
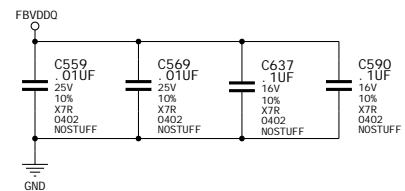
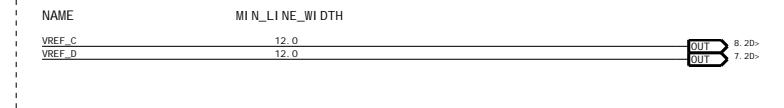
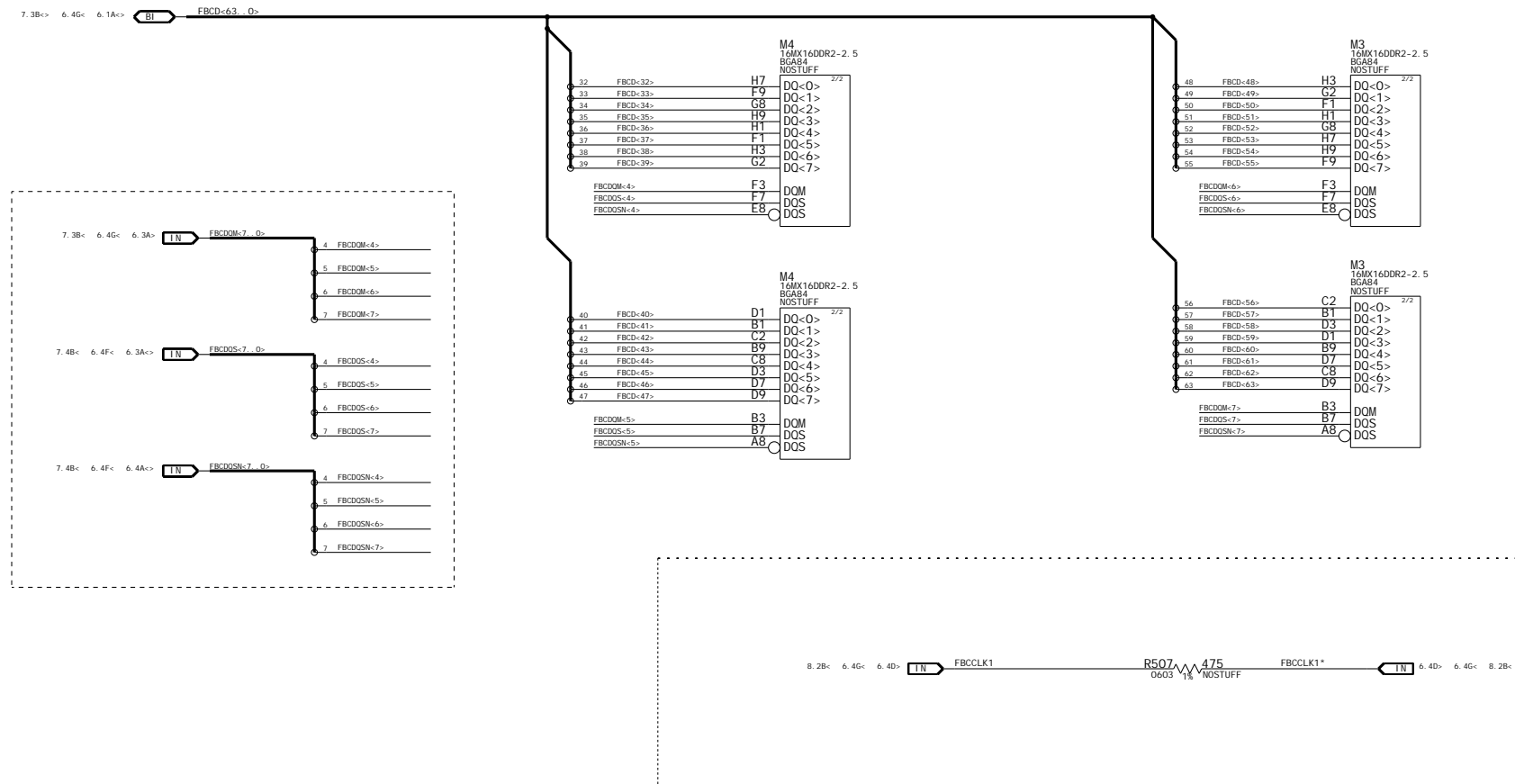
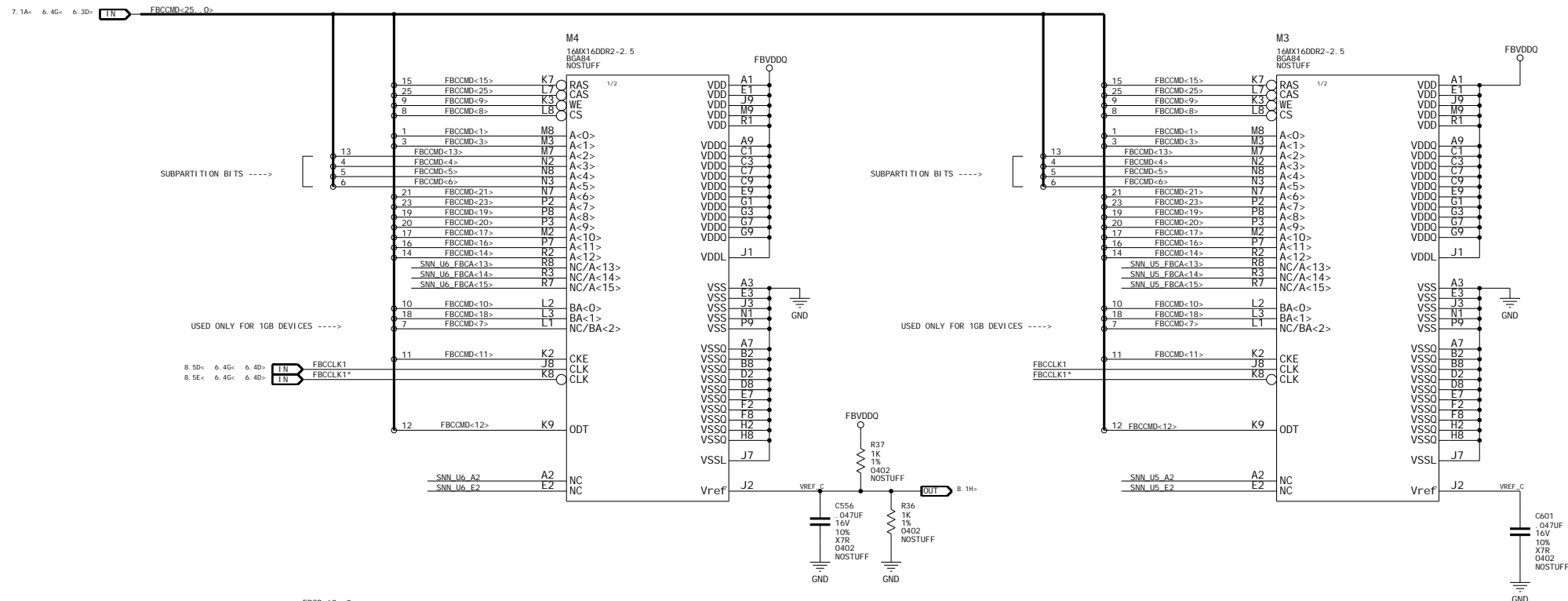
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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FBC MEMORY 2nd bank 32..63  
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



ALL COMPONENTS HERE ON FOR G73 ONLY

ASSEMBLY	G72 400/400MHz 256MB 128-bit DDR2 16MX16 DUAL-VGA
PAGE DETAIL	FBC 16Mx16 DDR2 MEMORIES, 2ND BANK 32..63

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ID p527 PAGE 8 OF 23

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DACA NET RULES

NET NV\_CRITICAL NV\_IMPEDANCE DIFFPAIR

IN	DACA_RED	1	600HM
IN	DACA_GREEN	1	600HM
IN	DACA_BLUE	1	600HM

14.2E< 9.4F>	IN	DACA_RED_C	1	600HM
14.2C< 9.4F>	IN	DACA_GREEN_C	1	600HM
14.2E< 9.5F>	IN	DACA_BLUE_C	1	600HM

IN	DACA_HSYNC	2	500HM
IN	DACA_VSYNC	2	500HM
IN	AVB	2	500HM
IN	AHB	2	500HM
IN	DACA_HSYNC_BUF	2	500HM
IN	DACA_VSYNC_BUF	2	500HM

14.3C< 9.3F>	IN	DACA_HSYNC_C	2	500HM
14.2C< 9.3F>	IN	DACA_VSYNC_C	2	500HM

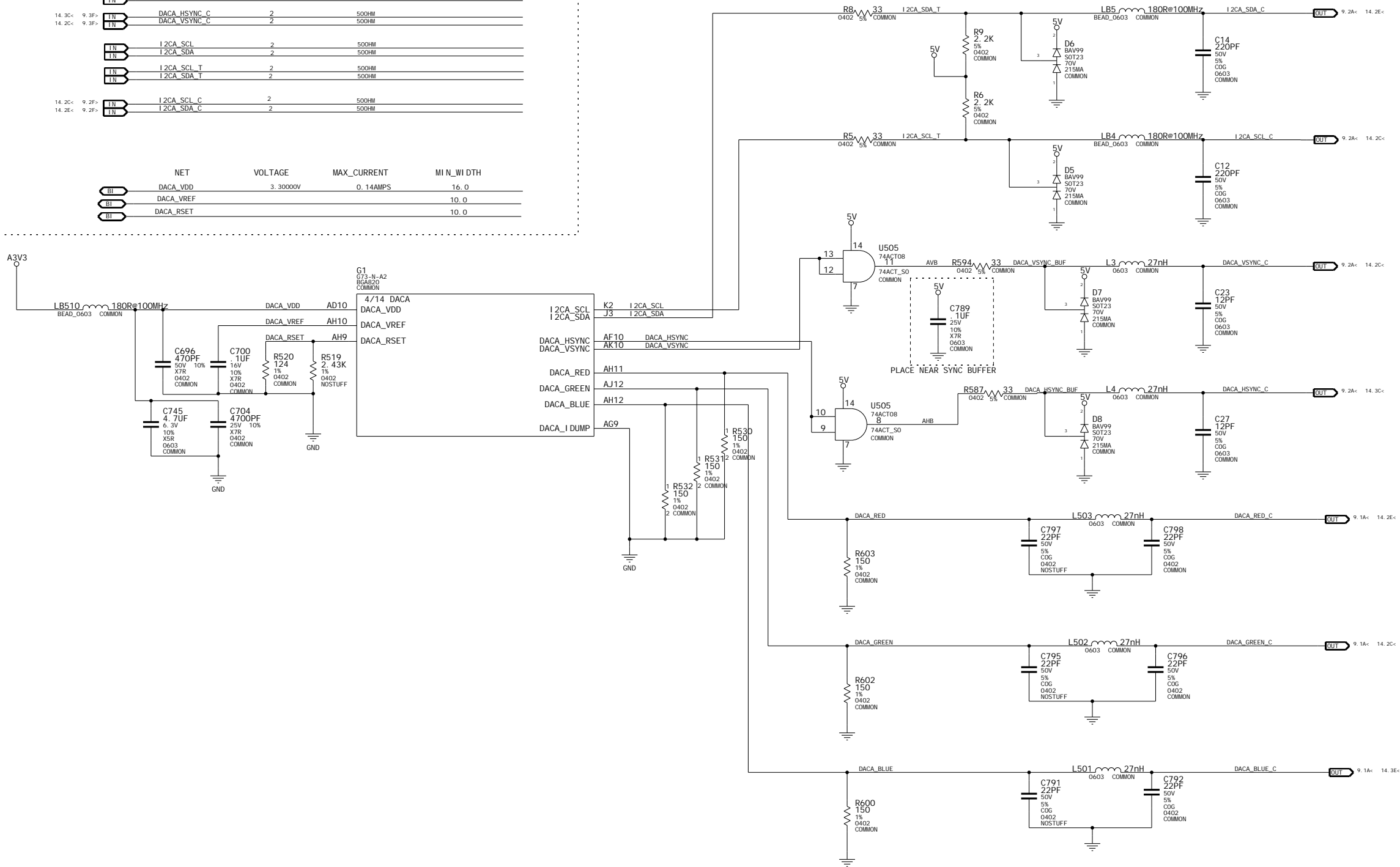
IN	I2CA_SCL	2	500HM
IN	I2CA_SDA	2	500HM
IN	I2CA_SCL_T	2	500HM
IN	I2CA_SDA_T	2	500HM

14.2C< 9.2F>	IN	I2CA_SCL_C	2	500HM
14.2E< 9.2F>	IN	I2CA_SDA_C	2	500HM

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACA_VDD	3.30000V	0.14AMPS	16.0
DACA_VREF			10.0
DACA_RSET			10.0

Primary Display (DACA)

DACA RGB-FILTER



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ID p527 PAGE 9 OF 23

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ASSEMBLY G72 400/400MHz 256MB 128-bit DDR2 16MX16 DUAL-VGA

PAGE DETAIL DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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DACC NET RULES

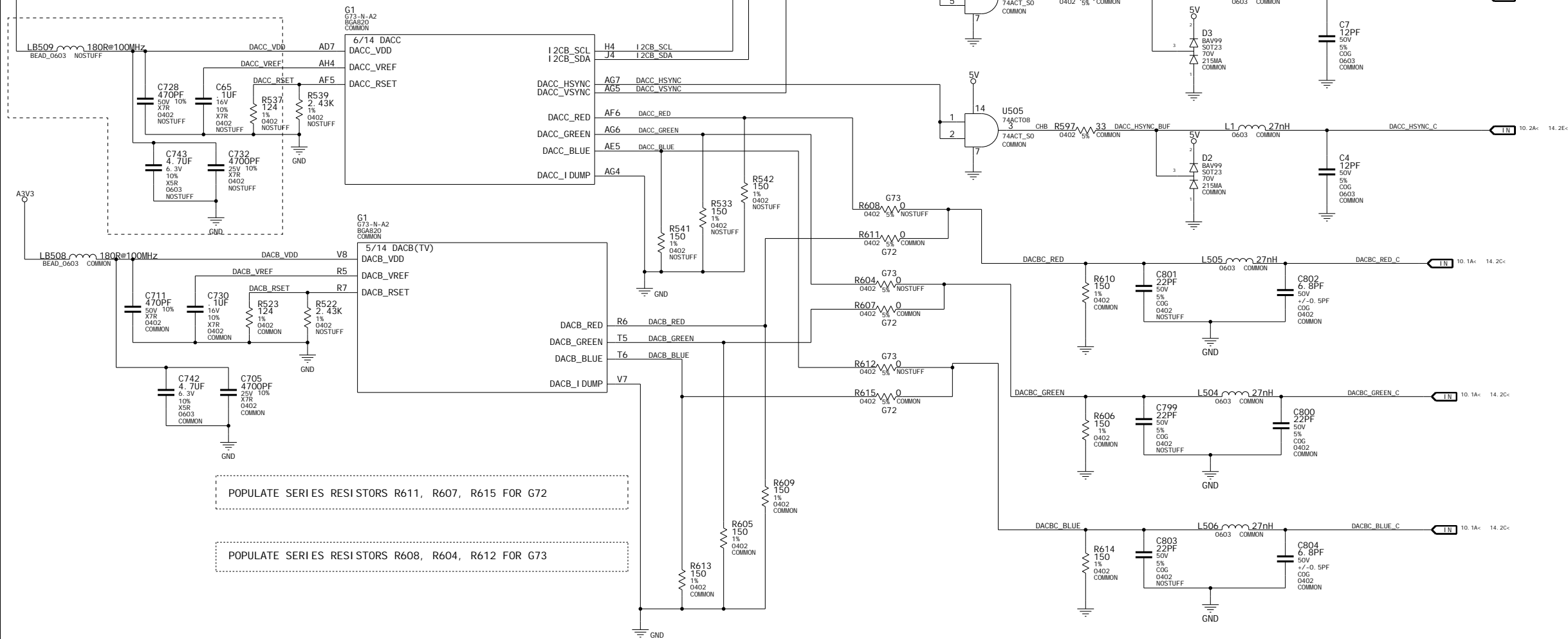
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1N	DACC_GREEN	1	600HM
1N	DACC_BLUE	1	600HM
1N	DACBC_RED	1	600HM
1N	DACBC_GREEN	1	600HM
1N	DACBC_BLUE	1	600HM
1N	DACB_RED	1	600HM
1N	DACB_GREEN	1	600HM
1N	DACB_BLUE	1	600HM
14.2C<	DACBC_RED_C	1	600HM
14.2C<	DACBC_GREEN_C	1	600HM
14.2C<	DACBC_BLUE_C	1	600HM
1N	DACC_HSYNC	2	500HM
1N	DACC_VSYNC	2	500HM
1N	CVB	2	500HM
1N	CHB	2	500HM
1N	DACC_HSYNC_BUF	2	500HM
1N	DACC_VSYNC_BUF	2	500HM
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14.2E<	DACC_VSYNC_C	2	500HM
1N	I2CB_SCL	2	500HM
1N	I2CB_SDA	2	500HM
1N	I2CB_SCL_T	2	500HM
1N	I2CB_SDA_T	2	500HM
14.2C<	I2CB_SCL_C	2	500HM
14.2C<	I2CB_SDA_C	2	500HM
NET VOLTAGE MAX_CURRENT MINWIDTH			
BI	DACC_VDD	3.30000V	0.14AMPS
BI	DACC_VREF		10.0
BI	DACC_RSET		10.0
BI	DACC_VDD	3.30000V	0.14AMPS
BI	DACC_VREF		10.0
BI	DACC_RSET		10.0

Secondary Display (DACC)

DACB/DACC RGB-FILTER

POPULATE ALL DACC FILTERS FOR G73 ONLY



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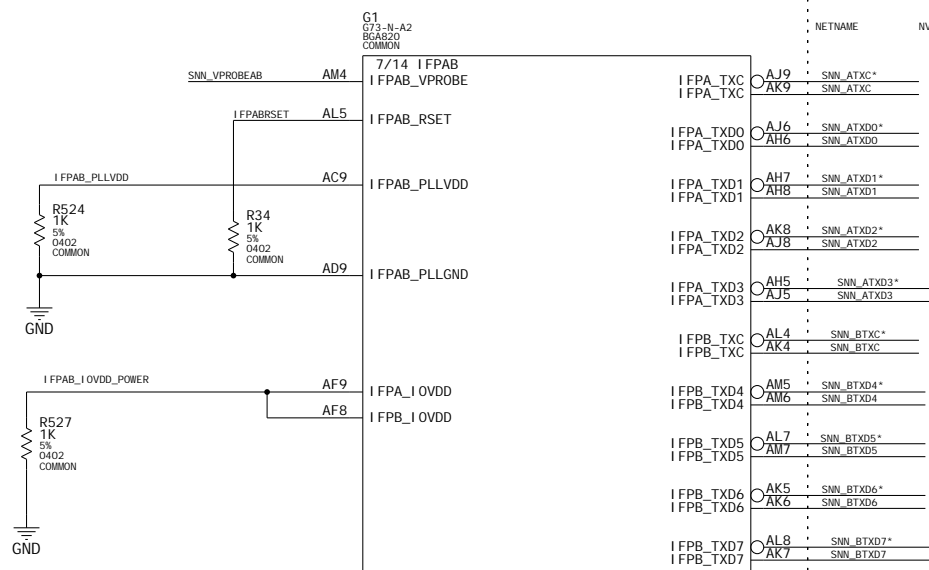
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## INTERNAL TMDS .. LINK A &amp; B


## I FPAB NET RULES

	NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAR R
	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	I FPAB_PLLVDD	2.50000V	0.04AMPS	16.0
IN	I FPABRSET			12.0



ASSEMBLY	G72 400/400MHz 256MB 128-bit DDR2 16MX16 DUAL-VGA
PAGE DETAIL	TMDS LINK A & PU'S, DVI CONNECTOR SOUTH

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## INTERNAL TMDS .. LINK C &amp; D

## I FPAB NET RULES

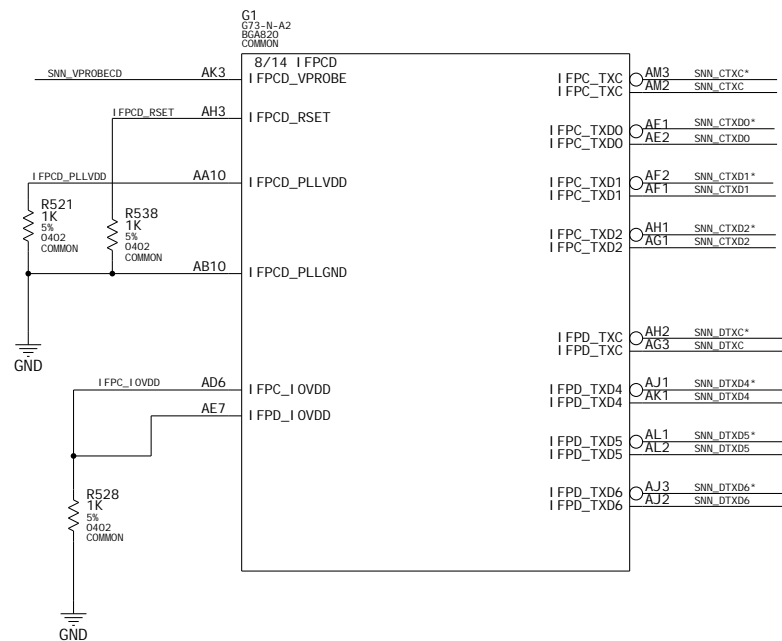
NET

MI N\_WIDTH

---

I FPCD\_RSET

12.0



ASSEMBLY	G72 400/400MHz 256MB 128-bit DDR2 16MX16 DUAL-VGA
PAGE DETAIL	TMDS LINK C

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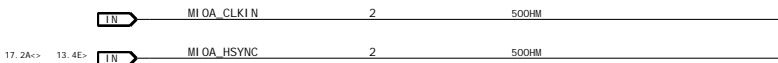
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ID	p527	PAGE	12 OF 23
NAME	epierre	DATE	27-NOV-2006

# MI OA & MI OB INTERFACES

## MIO NET RULES

NET NV\_CRI TICAL NV\_IMPEDANCE



### G3 MI OB

### G3 MI OA

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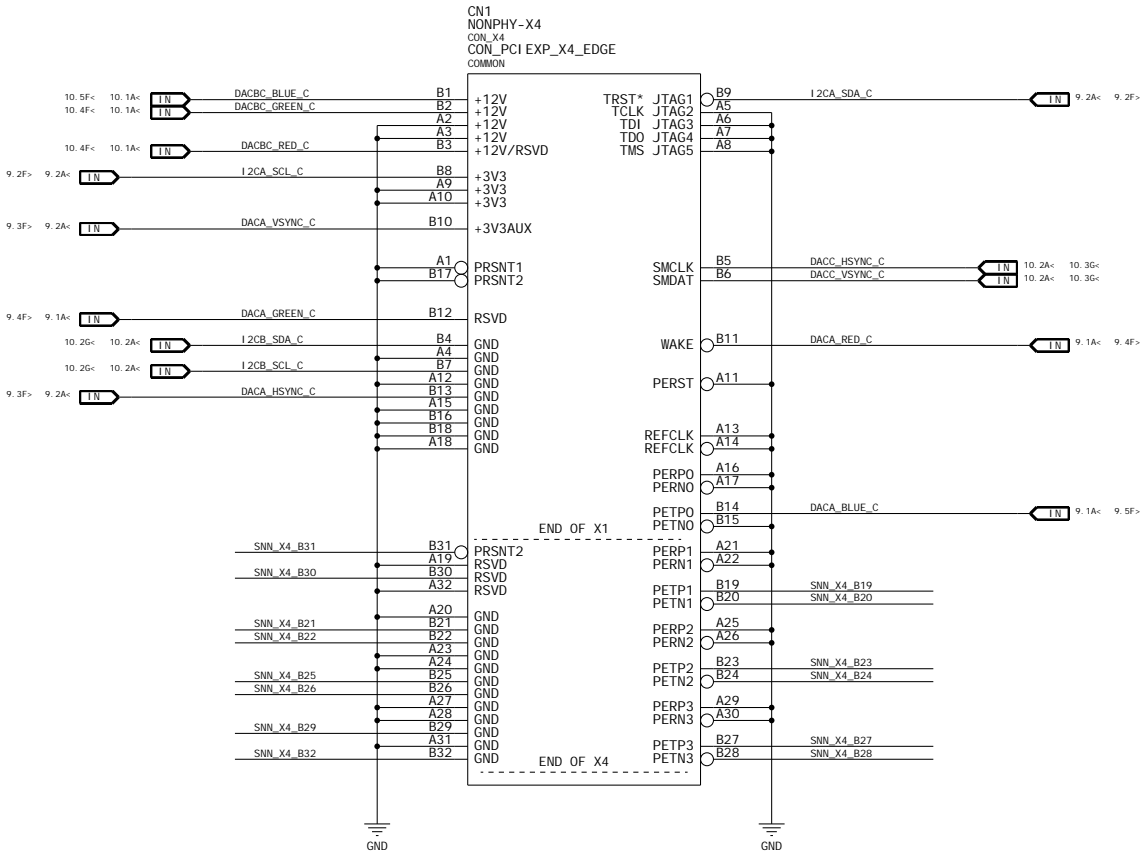
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ID	p527	PAGE	13 OF 23
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CUSTOM VGA PASS THRU x4PCI e EDGE CONNECTOR



VGA BLOCKS SWAPPED

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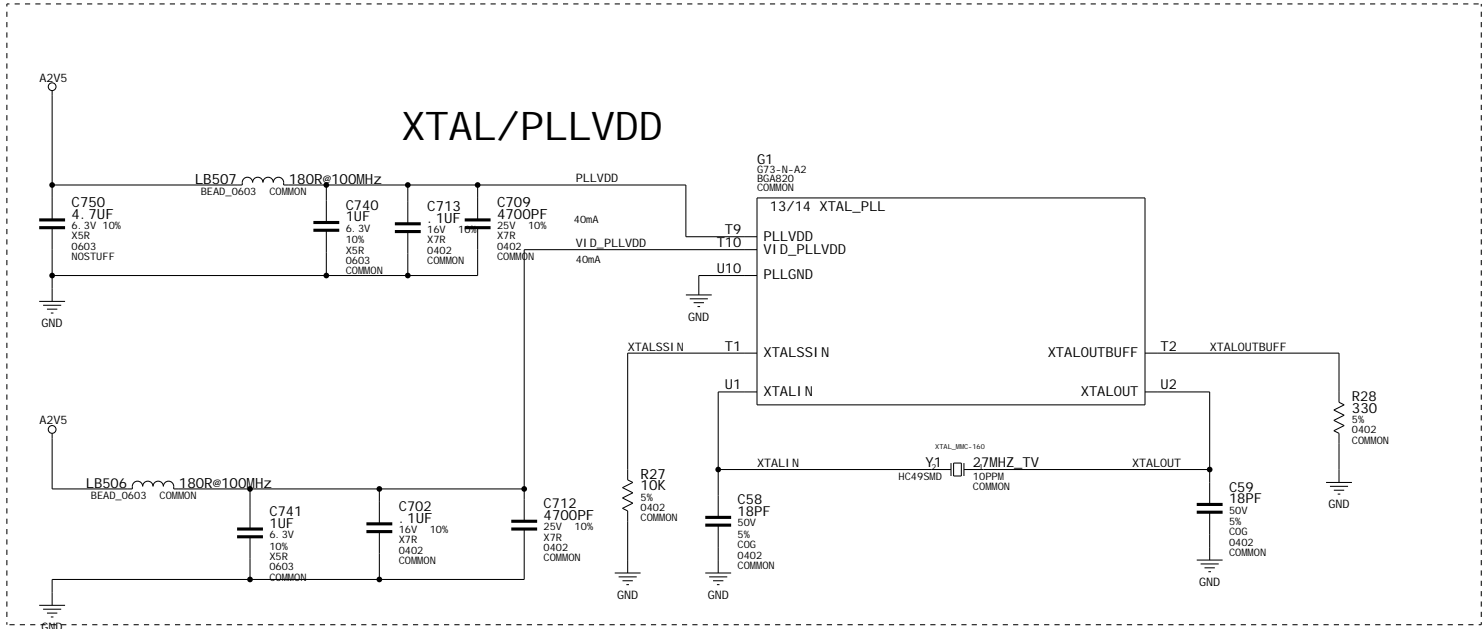
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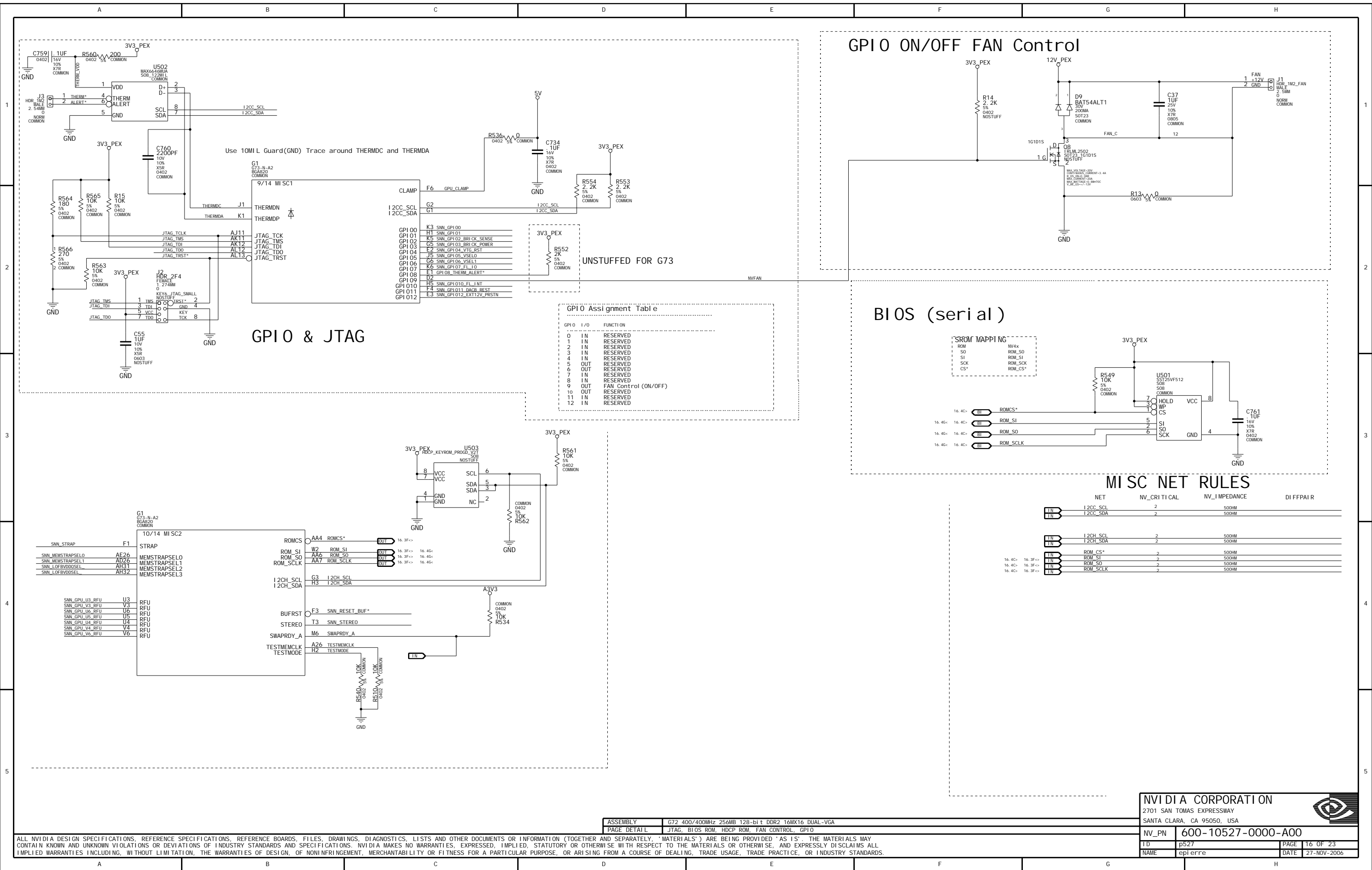
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ID	p527	PAGE	14 OF 23
NAME	epierre	DATE	27-NOV-2006



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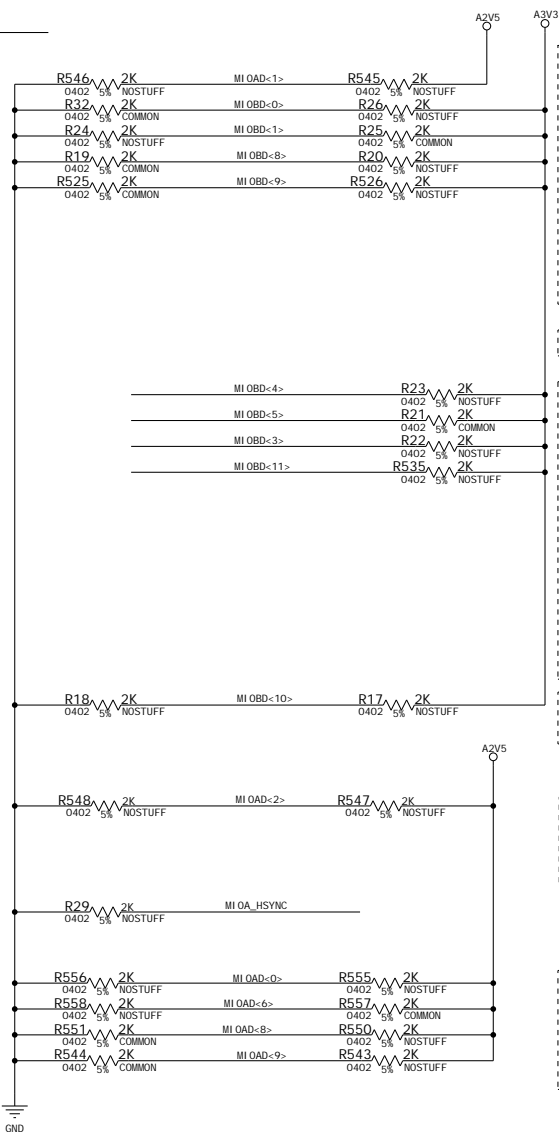
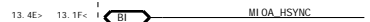
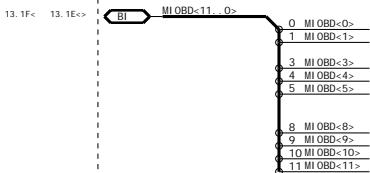
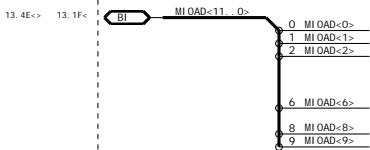


# BI OS, Straps, Mi sc

## Straps

Assembly: BIOS

## Mechanical parts



REG: NV\_PEXTDEV\_BOOT\_0

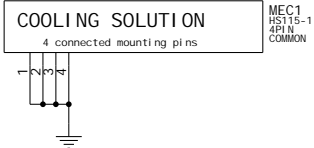
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01	SUB_VENDOR	SUB_VENDOR	0 NO BIOS 1 Read from BIOS
02	RAM_CFG_0	RAM_CFG[3:0]	0000 8Mx16 DDR2 128BIT 0001 RFU 1000 8Mx16 DDR2 64BIT 1001 RFU 1010 16Mx16 DDR2 128BIT 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 32Mx16 DDR2 64BIT
03	RAM_CFG_1		
04	RAM_CFG_2		
05	RAM_CFG_3		
06	CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz 01 14.31818 Mhz 10 27.000 Mhz 11 UNKNOWN
22	CRYSTAL_1		
07	TV_MODE_0	TV_MODE[1:0]	00 SECAM 01 NTSC 10 PAL 11 CRT
08	TV_MODE_1		
09	AGP8xEnabled	AGP_8x	0 AGP8x enabled 1 AGP8x disabled
10	AGP_SBA	AGP_SBA[0]	0 SBA enabled 1 SBA disabled
11	AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled
12	PCI_DEVID_0	PCI_DEVID[3:0]	0000 0x140 ... 1111 0x014F 0000 (default 0x140) 0101 (0x145)
13	PCI_DEVID_1		
20	PCI_DEVID_2		
21	PCI_DEVID_3		
14	BUS_TYPE	BUS_TYPE[0]	0 PCI 1 AGP
15	FP_FACE	FP_FACE[0]	0 24BIT 1 128BIT (DEFAULT)
23	FB_0	FB[1:0]	00 64M 01 128M 10 256M (DEFAULT) 11 512M
24	FB_1		
25	BR	BR[0]	0 BRIDGE disabled 1 BRIDGE enabled
26	BR_128M		BR bits are ignored if BRIDGE is disabled
27	BR_AGP		
28	BR_10		
29	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F 10 Serial_SST49VF 11 RFU
30	ROM_TYPE_1		

16	USER_0	STRAP_USER[3:0]	0000 (default)
17	USER_1		
18	USER_2		
19	USER_3		

31: SLOT\_CLOCK\_CFG 0 COMMON PCIe REF CLK enabled  
1 COMMON PCIe REF CLK disabled

REG: NV\_STRAP\_1

Bit	Signal	VALUE_ID	VALUES
11	PEX_PLL_EN_TERM100		0 (default -- internal term on)
12	3GI0_PADCFG_LUT_ADR[0]		
13	3GI0_PADCFG_LUT_ADR[1]		001 FOR G72M
14	3GI0_PADCFG_LUT_ADR[2]		



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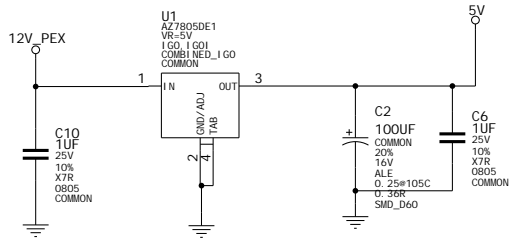
NV\_PN 600-10527-0000-A00

ID	p527	PAGE	17 OF 23
NAME	epierre	DATE	27-NOV-2006

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Power Supply 1 : 5V A3V3

5V



NETNAME	MAX_CURRENT	MIN_LENGTH	VOLTAGE
5V	0.3AMPS	12.0	
A3V3	1.5AMPS	30.0	3.30000V
GND		35.0	0.000000V

A3V3 Power Supply



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ID	p527	PAGE	18 OF 23
NAME	epierre	DATE	27-NOV-2006

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PowerSupply II: NVVDD, A2V5

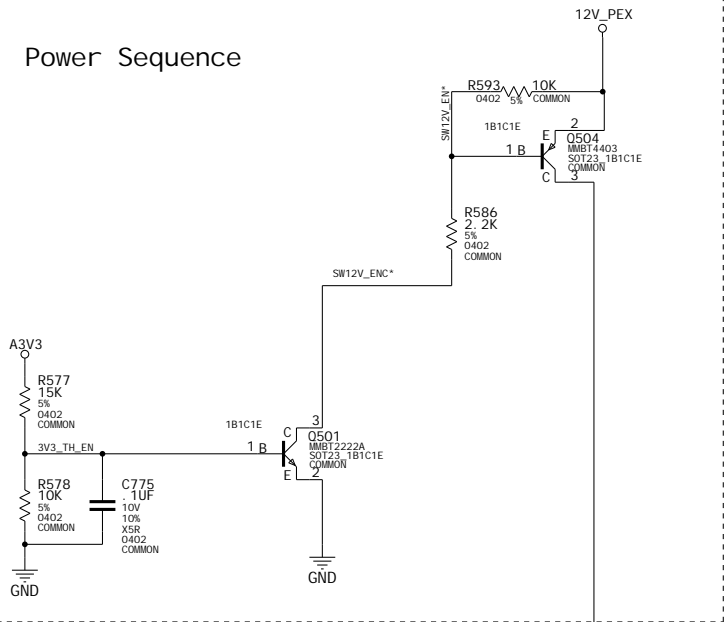
Net Name LINE\_WIDTH Current Voltage

NVVDD NVVDD 36MIL 15AMPS 1.2V

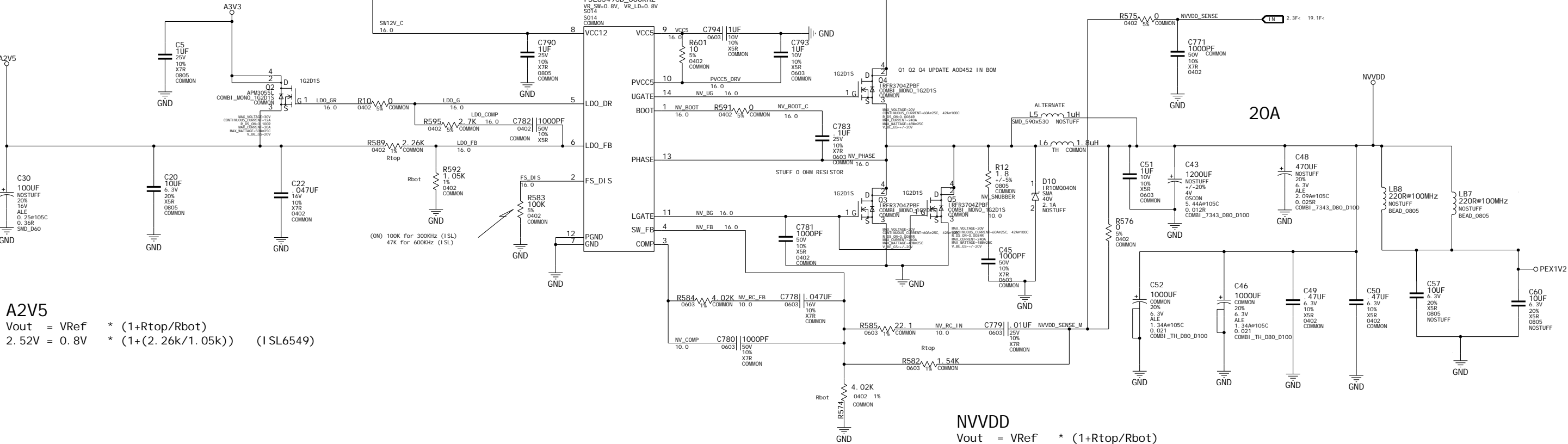
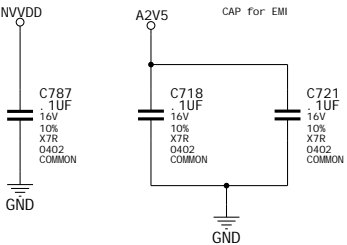
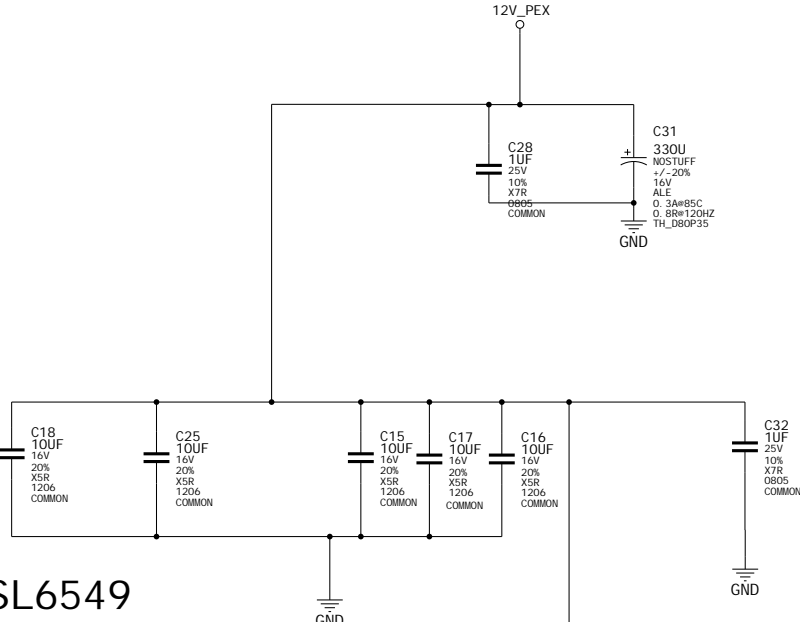
NVVDD\_SENSE NVVDD\_SENSE\_M 16MIL 0.5AMPS 1.2V

A2V5 A2V5 16MIL 0.8AMPS 2.5V

Power Sequence



ISL6549



A2V5

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$
$$2.52V = 0.8V * (1 + (2.26k/1.05k)) \quad (ISL6549)$$

NVVDD

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$
$$1.1V = 0.8V * (1 + (1.54k/4.02k)) \quad (ISL6549)$$
$$1.2V = 0.8V * (1 + (1.54k/3.09k)) \quad (ISL6549)$$

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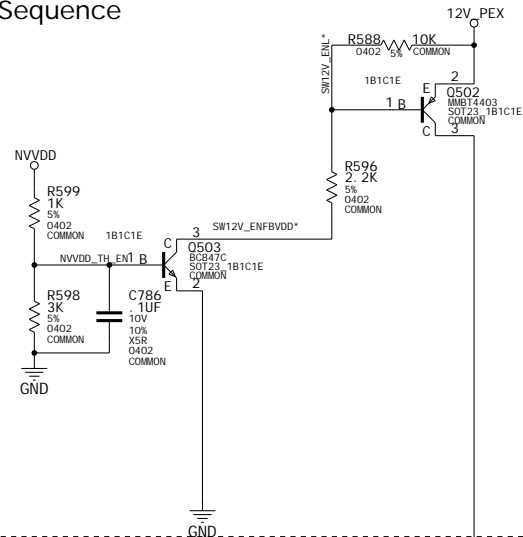


NV\_PN 600-10527-0000-A00

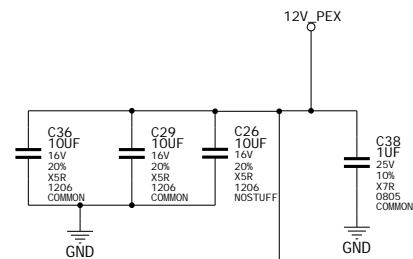
ID p527 PAGE 19 OF 23  
NAME epierre DATE 27-NOV-2006

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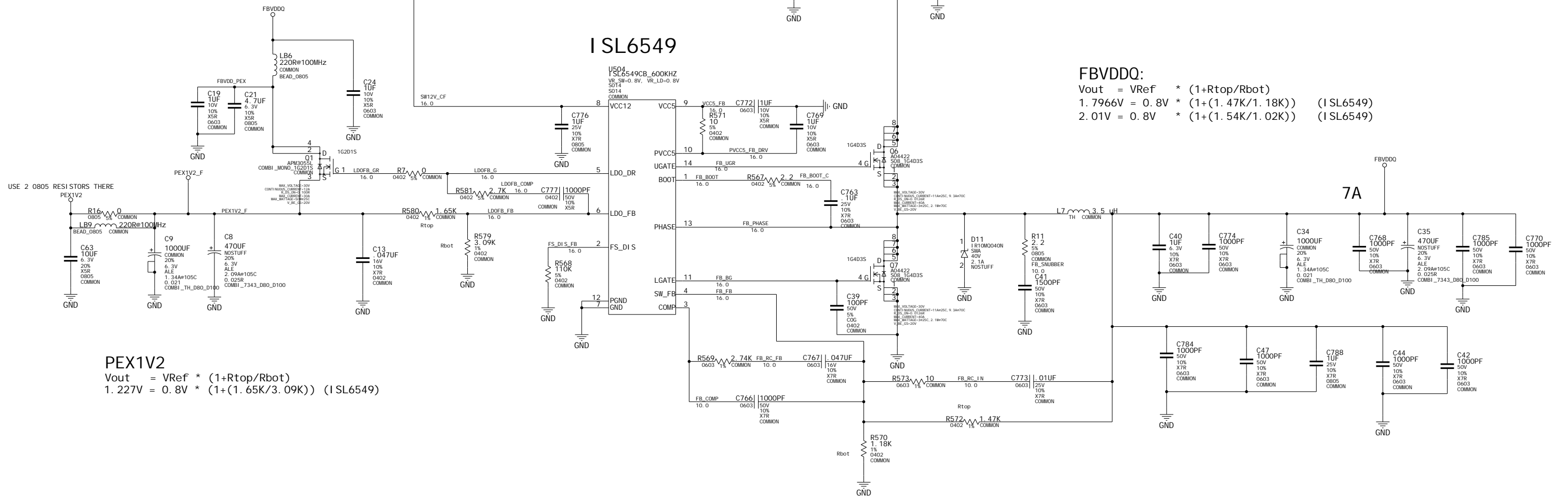
PowerSupply III: FbVDDQ, PEX1V2



Net	Name	LI NE_WI DTH	CURRENT	Vol tage
FBVDD0	FBVDD0	12MIL		1.8V
PEX1V2_F	PEX1V2_F	24MIL	1.5AMPS	1.2V
PEX1V2	PEX1V2	24MIL	1.5AMPS	1.2V



I SL6549



PEX1V2

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

$$1.227V = 0.8V * (1 + (1.65K/3.09K)) \quad (I\ SL6549)$$

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NV_PN	600-10527-0000-A00		
ID	p527	PAGE	20 OF 23
NAME	epi erre	DATE	27-NOV-2006

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A		B		C		D		E		F		G		H			
1	Title: Basenet Report Desi gn: p527 Date: Nov 20 13:20:52 2006																
	Base nets and synonyms for p527_a00.lib. P527(ep527_a00.lib.p527(sch_1))																
2	Base Si gnal	Location([Zone][di r])															
	3V3AUX	2.5G															
3	3V3_PEX	2.5G															
	3V3_TH_EN	19.2A															
4	5V	18.1G															
	12V_PEX	2.5G															
5	A2V5	19.1F															
	A3V3	18.1G															
6	AHB	9.1A< 9.3E															
	ALERT*	16.1A															
7	AVB	9.1A< 9.3E															
	CHB	10.1A< 10.3E															
8	CVB	10.1A< 10.3E															
	DACA_BLUE	9.1A< 9.5D															
9	DACA_BLUE_C	9.1A< 9.5F> 14.3E<															
	DACA_GREEN	9.1A< 9.4D															
10	DACA_GREEN_C	9.1A< 9.4F> 14.2C<															
	DACA_HSYNC	9.1A< 9.3C															
11	DACA_HSYNC_BUF	9.1A< 9.3E															
	DACA_HSYNC_C	9.2A< 9.3F> 14.3C<															
12	DACA_RED	9.1A< 9.4D															
	DACA_RED_C	9.1A< 9.4F> 14.2E<															
13	DACA_RSET	9.2A<> 9.3B															
	DACA_VDD	9.2A<> 9.3B															
14	DACA_VREF	9.1A< 9.3C															
	DACA_VSYNC	9.1A< 9.3C															
15	DACA_VSYNC_BUF	9.2A< 9.3E															
	DACA_VSYNC_C	9.2A< 9.3F> 14.2C<															
16	DACBC_BLUE	10.1A< 10.5E															
	DACBC_BLUE_C	10.1A< 10.5F< 14.2C<															
17	DACBC_GREEN	10.1A< 10.4E															
	DACBC_GREEN_C	10.1A< 10.4F< 14.2C<															
18	DACBC_RED	10.1A< 10.4E															
	DACBC_RED_C	10.1A< 10.4F< 14.2C<															
19	DACB_BLUE	10.1A< 10.4C															
	DACB_GREEN	10.1A< 10.4C															
20	DACB_RED	10.1A< 10.4C															
	DACB_RSET	10.2A<> 10.4A															
21	DACB_VDD	10.2A<> 10.4B															
	DACB_VREF	10.2A<> 10.4A															
22	DACC_BLUE	10.1A< 10.3C															
	DACC_GREEN	10.1A< 10.3C															
23	DACC_HSYNC	10.1A< 10.3C															
	DACC_HSYNC_BUF	10.2A< 10.3E															
24	DACC_HSYNC_C	10.2A< 10.3G< 14.2E<															
	DACC_RED	10.1A< 10.3C															
25	DACC_RSET	10.2A<> 10.3B															
	DACC_VDD	10.2A<> 10.3A															
26	DACC_VREF	10.2A<> 10.3A															
	DACC_VSYNC	10.1A< 10.3C															
27	DACC_VSYNC_BUF	10.2A< 10.3E															
	DACC_VSYNC_C	10.2A< 10.3G< 14.2E<															
28	FAN_C	16.1G															
	FBACLK0	3.3D> 3.3F< 4.2A<															
29		4.2D 4.5C<															
	FBACLK0*	3.3F< 3.4D> 4.2A<															
30		4.2D 4.5E<															
	FBACLK1	3.3F< 3.4D> 5.2A<															
31		5.2D 5.5D<															
	FBACLK1*	3.3F< 3.4D> 5.2A<															
32		5.2D 5.5E<															
	FBACMD<0>	3.2C 3.2F 4.1B 4.1D															
33		FBACMD<25_..0>	3.2D> 3.4F< 4.1A<														
		5.1A<															
34		FBACMD<1>	3.1F 3.3C 4.1B 4.1D														
		5.1B 5.1D															
35		FBACMD<2>	3.2G 3.3C 4.1B 4.1D														
		FBACMD<3>	3.1F 3.3C 4.1B 4.1D														
36		FBACMD<4>	3.1G 3.3C 5.1B 5.1D														
		FBACMD<5>	3.1F 3.3C 5.1B 5.1D														
37		FBACMD<6>	3.1G 3.3C 5.2B 5.2D														
		FBACMD<7>	3.2G 3.3C 4.2B 4.2D														
38		FBACMD<8>	5.2B 5.2D														
			3.1G 3.3C 4.1B 4.1D														
39		FBACMD<9>	5.1B 5.1D														
			3.1F 3.3C 4.1B 4.1D														
40		FBACMD<10>	5.1B 5.1D														
			3.2F 3.3C 4.2B 4.2D														
41		FBACMD<11>	5.2B 5.2D														
			3.3C 3.3D 4.2B 4.2D														
42		FBACMD<12>	5.2B 5.2D														
			3.3E 4.2B 4.2D 5.2B 5.2D														
43		FBACMD<13>	3.1G 3.3C 5.1B 5.1D														
		FBACMD<14>	3.2F 3.3C 4.2B 4.2D														
44		FBACMD<15>	5.2B 5.2D														
			3.1G 3.3C 4.1B 4.1D														



ASSEMBLY	G72 400/400MHz 256MB 128-bit DDR2 16MX16 DUAL-VGA
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NV_PN	600-10527-0000-A00		
ID	p527	PAGE	21 OF 23
NAME	epi erre	DATE	27-NOV-2006

A		B		C		D		E		F		G		H	
1															
2															
3															
4															
5															

SNN\_MI\_OA\_VREF 13. 4B  
SNN\_MI\_OA\_VSYNC 13. 5D  
SNN\_MI\_OBCAL\_PU\_GND 13. 2B  
SNN\_MI\_OBD<2> 13. 2D  
SNN\_MI\_OBD<6> 13. 2D  
SNN\_MI\_OBD<7> 13. 2D  
SNN\_MI\_OBD<12> 13. 2D  
SNN\_MI\_OBD<13> 13. 2D  
SNN\_MI\_OBD<14> 13. 2D  
SNN\_MI\_OBD<15> 13. 2D  
SNN\_MI\_OB\_CLKOUT 13. 2D  
SNN\_MI\_OB\_CLKOUT\* 13. 3D  
SNN\_MI\_OB\_CTL3 13. 2D  
SNN\_MI\_OB\_VREF 13. 2B  
SNN\_PEXCALPD\_GND 2. 2C  
SNN\_PEXCAPD\_VDDQ 2. 2C  
SNN\_PEX\_SMCLK 2. 1B  
SNN\_PEX\_SMDAT 2. 1B  
SNN\_PEX\_WAKE\* 2. 2B  
SNN\_PE\_PRSNT2\_A 2. 1A  
SNN\_PE\_PRSNT2\_B 2. 2A  
SNN\_PE\_PRSNT2\_C 2. 3A  
SNN\_PE\_RSVD2 2. 2A  
SNN\_PE\_RSVD3 2. 2A  
SNN\_PE\_RSVD4 2. 2A  
SNN\_PE\_RSVD5 2. 2A  
SNN\_PE\_RSVD6 2. 3A  
SNN\_PE\_RSVD7 2. 4A  
SNN\_PE\_RSVD8 2. 4A  
SNN\_RESET\_BUF\* 16. 4B  
SNN\_SPDI\_F 2. 5E  
SNN\_STEREO 16. 4B  
SNN\_STRAP 16. 4A  
SNN\_U2\_A2 7. 2B  
SNN\_U2\_E2 7. 2B  
SNN\_U2\_FBCA<13> 7. 2B  
SNN\_U2\_FBCA<14> 7. 2B  
SNN\_U2\_FBCA<15> 7. 2B  
SNN\_U3\_A2 7. 2E  
SNN\_U3\_E2 7. 2E  
SNN\_U3\_FBCA<13> 7. 2E  
SNN\_U3\_FBCA<14> 7. 2E  
SNN\_U3\_FBCA<15> 7. 2E  
SNN\_U5\_A2 8. 2D  
SNN\_U5\_E2 8. 2D  
SNN\_U5\_FBCA<13> 8. 2D  
SNN\_U5\_FBCA<14> 8. 2D  
SNN\_U5\_FBCA<15> 8. 2D  
SNN\_U6\_A2 8. 2B  
SNN\_U6\_E2 8. 2B  
SNN\_U6\_FBCA<13> 8. 2B  
SNN\_U6\_FBCA<14> 8. 2B  
SNN\_U6\_FBCA<15> 8. 2B  
SNN\_U7\_A2 4. 2D  
SNN\_U7\_E2 4. 2D  
SNN\_U7\_FBAA<13> 4. 2D  
SNN\_U7\_FBAA<14> 4. 2D  
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SNN\_U8\_E2 4. 2B  
SNN\_U8\_FBAA<13> 4. 2B  
SNN\_U8\_FBAA<14> 4. 2B  
SNN\_U8\_FBAA<15> 4. 2B  
SNN\_U9\_A2 5. 2D  
SNN\_U9\_E2 5. 3D  
SNN\_U9\_FBAA<13> 5. 2D  
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SNN\_U10\_FBAA<13> 5. 2B  
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SNN\_U10\_FBAA<15> 5. 2B  
SNN\_V1PHAD<4> 13. 2D  
SNN\_V1PHAD<5> 13. 2D  
SNN\_V1PHAD<6> 13. 2D  
SNN\_V1PHAD<7> 13. 2D  
SNN\_V1PHCLK 13. 2D  
SNN\_V1PHCTL 13. 2D  
SNN\_V1PPCLK 13. 2D  
SNN\_VPROBEAB 11. 2B  
SNN\_VPROBECD 12. 2B  
SNN\_X4\_B19 14. 3E  
SNN\_X4\_B20 14. 3E  
SNN\_X4\_B21 14. 3C  
SNN\_X4\_B22 14. 3C  
SNN\_X4\_B23 14. 3E  
SNN\_X4\_B24 14. 3E  
SNN\_X4\_B25 14. 3C  
SNN\_X4\_B26 14. 3C  
SNN\_X4\_B27 14. 3E  
SNN\_X4\_B28 14. 3E  
SNN\_X4\_B29 14. 3C  
SNN\_X4\_B30 14. 3C  
SNN\_X4\_B31 14. 3C  
SNN\_X4\_B32 14. 3C

SNN\_\_MI\_OBCAL\_PD\_VD 13. 2B  
DQ  
SW12V\_C 19. 3C  
SW12V\_CF 20. 3C  
SW12V\_EN\* 19. 1B  
SW12V\_ENC\* 19. 2B  
SW12V\_ENFBVDD\* 20. 2B  
SW12V\_ENL\* 20. 1B  
SWAPRDY\_A 16. 4C<  
TESTMEMCLK 16. 4B  
TESTMODE 16. 4B  
THERM\* 16. 1A  
THERMDA 16. 2B  
THERMDC 16. 2B  
THERM\_VDD 16. 1A  
VCC5 19. 3D  
VCC5\_FB 20. 3D  
VDD33 2. 3E  
VID\_PLLVDD 15. 2E 15. 5F<  
VREF\_A 5. 1H> 5. 3D> 5. 3F<  
VREF\_B 4. 2C> 4. 2F> 5. 1H>  
VREF\_C 8. 1H> 8. 2D> 8. 2F  
VREF\_D 7. 2D> 7. 2F 8. 1H>  
XTALI\_N 15. 3F 15. 4F<  
XTALOUT 15. 3G 15. 4F<  
XTALOUTBUFF 15. 2G  
XTALSSIN 15. 2E

ASSEMBLYG72 400/400MHz 256MB 128-bit DDR2 16MX16 DUAL-VGA  
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NAMEepierre

PAGE22 OF 23  
DATE27-NOV-2006

A		B		C		D		E		F		G		H	
Title: Cref Part Report Desi gn: p527 Date: Nov 20 13: 20: 52 2006		C519 [4. 3G] C520 [5. 2G] C521 [4. 4G] C522 [5. 2G] C523 [5. 4G] C524 [5. 2H] C525 [5. 4G] C526 [4. 1G] C527 [4. 3G] C528 [5. 2G] C529 [4. 3G] C530 [4. 2G] C531 [4. 1G] C532 [4. 3G] C533 [5. 4G] C534 [5. 2G] C535 [5. 2H] C536 [5. 4G] C537 [5. 2G] C538 [5. 4G] C539 [5. 4H] C540 [4. 3H] C541 [4. 3G] C542 [4. 1G] C543 [5. 4H] C544 [5. 2H] C545 [4. 3G] C546 [5. 4G] C547 [4. 2H] C548 [4. 2G] C549 [5. 4G] C550 [5. 2G] C551 [5. 4G] C552 [5. 2G] C553 [4. 1H] C554 [4. 2G] C555 [3. 5A] C556 [8. 3C] C557 [8. 4G] C558 [8. 4H] C559 [8. 1F] C560 [8. 3G] C561 [4. 5G] C562 [8. 3H] C563 [2. 5C] C564 [8. 2H] C565 [2. 5C] C566 [8. 4G] C567 [8. 4F] C568 [8. 4G] C569 [8. 1G] C570 [2. 5C] C571 [3. 2E] C572 [2. 5C] C573 [3. 1E] C574 [3. 2D] C575 [3. 1D] C576 [3. 2D] C577 [3. 2D] C578 [3. 2E] C579 [3. 1D] C580 [3. 2E] C581 [2. 5C] C582 [2. 4C] C583 [2. 5C] C584 [2. 4C] C585 [2. 4C] C586 [2. 4C] C587 [2. 4C] C588 [8. 2G] C589 [8. 4H] C590 [8. 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ID	p527	PAGE	23 OF 23
NAME	epierre	DATE	27-NOV-2006

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