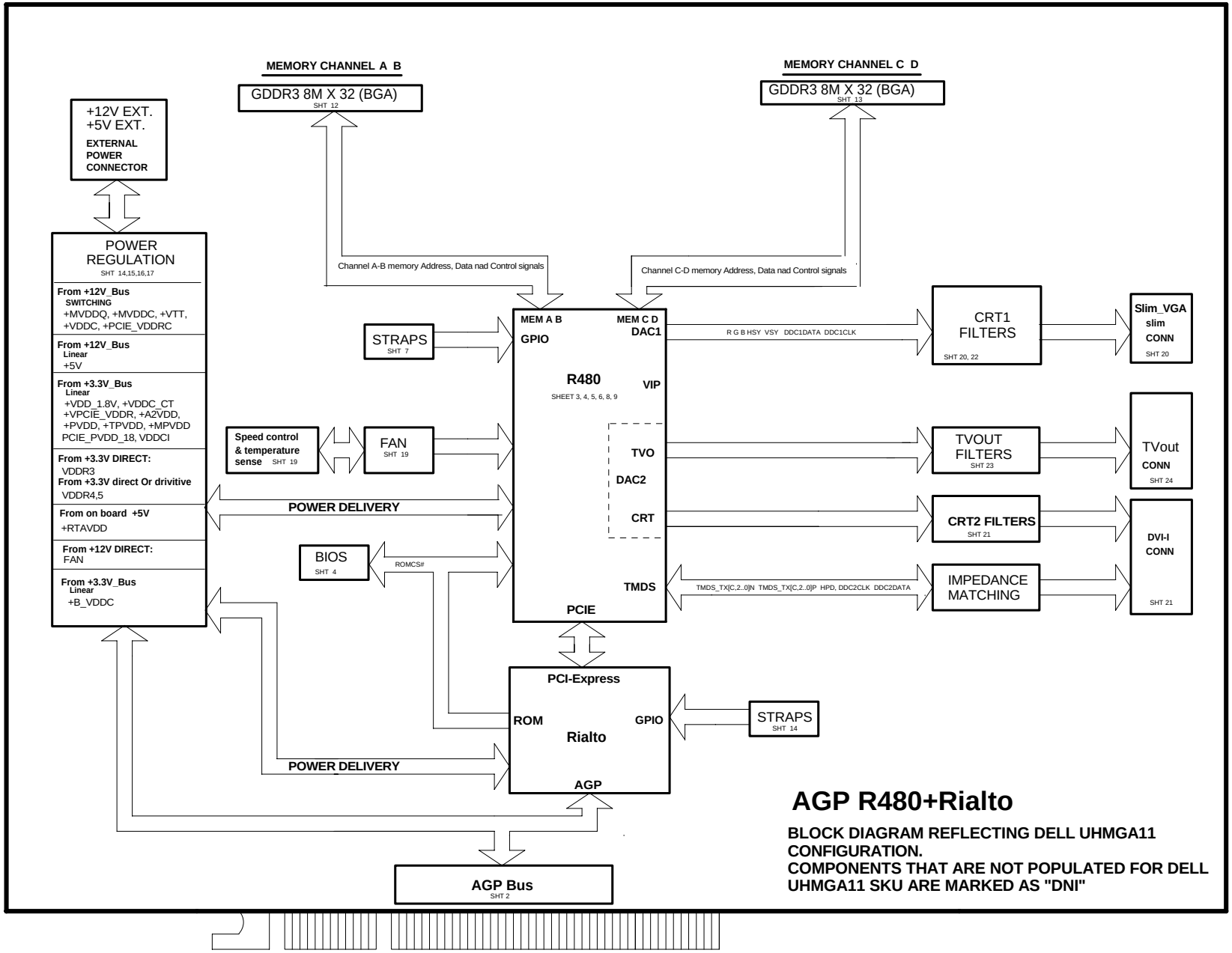
<Variant Name>

Title	Schematic No.	Date:
AGP R480+Rialto 256MB BGA DVII DVII VIVO	105-A49000-00A	**Friday, January 28, 2005**

REVISION HISTORY

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/07/04	Initial revision of the schematic based on 105-A474xx-00



AGP R480+Rialto

BLOCK DIAGRAM REFLECTING DELL UHMGA11 CONFIGURATION.
COMPONENTS THAT ARE NOT POPULATED FOR DELL UHMGA11 SKU ARE MARKED AS "DNI"

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LAYOUT NOTE: SOME OF THE CAPS BELOW MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

+12V_BUS — C12 10uF_20V
+5V_BUS — C5 47uF_6.3V
+3.3V_BUS — C10 47uF_6.3V
+VDDQ_BUS — C4 330uF_2.5V

Use 47uF Tant. 16V 20% D size (P/N 4230047600), 800mR Max. ESR and Max. ripple 430mA @ 100kHz
or
100uF, Alum. 6.3V 20% 6.3mm dia (P/N 4261010700), 440mR Max. ESR and Max. ripple 230mA @ 100kHz
or
47uF, Alum. 6.3V 20% 5mm dia (P/N 4262047600), 760mR Max. ESR and Max. ripple 150mA @ 100kHz

Place C2 on left side of AGP connector

4X/8X AGP BUS

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

(7) VDDC_PGOOD — R1833 0R — DNI

AGP_C/BE#[3..0] — AGP_C/BE#[3..0] (23)
AGP_AD[31..0] — AGP_AD[31..0] (23)
AGP_SBA[7..0] — AGP_SBA[7..0] (23)
AGP_ST[2..0] — AGP_ST[2..0] (23)

MAGP1

A1	12V	OVRCNT#	B1
A2	TYPEDET#	5.0V	B2
A3	GC_DET#/RESERVED	5.0V#B3	B3
A4	USB-	USB+	B4
A5	GND	GND#B5	B5
A6	INTA#	INTB#	B6
A7	RST#	CLK	B7
A8	GNT#	REQ#	B8
A9	VCC3.3	VCC3.3#B9	B9
A10	ST1	ST0	B10
A11	MB_DET#/RESERVED	ST2	B11
A12	DBI_HI/PIPE#	RBF#	B12
A13	GND#A13	GND#B13	B13
A14	WBF#	DBI_LO/RESERVED	B14
A15	SBA1	SBA0	B15
A16	VCC3.3#A16	VCC3.3#B16	B16
A17	SBA3	SBA2	B17
A18	SB_STB#	SB_STB	B18
A19	GND#A19	GND#B19	B19
A20	SBA5	SBA4	B20
A21	SBA7	SBA6	B21
A22	RESERVED	RESERVED#B22	B22
A23	GND#A23	GND#B23	B23
A24	RESERVED#A24	3.3VAUX	B24
A25	VCC3.3#A25	VCC3.3#B25	B25
A26	AD30	AD31	B26
A27	AD28	AD29	B27
A28	VCC3.3#A28	VCC3.3#B28	B28
A29	AD26	AD27	B29
A30	AD24	AD25	B30
A31	GND#A31	GND#B31	B31
A32	AD_STB1#	AD_STB1	B32
A33	C/BE3#	AD23	B33
A34	VDDQ1.5	VDDQ1.5#B34	B34
A35	AD22	AD21	B35
A36	AD20	AD19	B36
A37	GND#A37	GND#B37	B37
A38	AD18	AD17	B38
A39	AD16	C/BE2#	B39
A40	VDDQ1.5#A40	VDDQ1.5#B40	B40
A41	FRAME#	IRDY#	B41
A42	KEY	KEY#B42	B42
A43	KEY#A43	KEY#B43	B43
A44	KEY#A44	KEY#B44	B44
A45	KEY#A45	KEY#B45	B45
A46	TRDY#	DEVSEL#	B46
A47	STOP#	VDDQ1.5#B47	B47
A48	PME#	PERR#	B48
A49	GND#A49	GND#B49	B49
A50	PAR	SERR#	B50
A51	AD15	C/BE1#	B51
A52	VDDQ1.5#A52	VDDQ1.5#B52	B52
A53	AD13	AD14	B53
A54	AD11	AD12	B54
A55	GND#A55	GND#B55	B55
A56	AD9	AD10	B56
A57	C/BE0#	AD8	B57
A58	VDDQ1.5#A58	VDDQ1.5#B58	B58
A59	AD_STB0#	AD_STB0	B59
A60	AD6	AD7	B60
A61	GND#A61	GND#B61	B61
A62	AD4	AD5	B62
A63	AD2	AD3	B63
A64	VDDQ1.5#A64	VDDQ1.5#B64	B64
A65	AD0	AD1	B65
A66	VREFGC	VREFCG	B66

1.5V_AGP_BUS

AGP_TYPEDET# — AGP_GC_8X_DET# — AGP_CON_RESET# — AGP_ST1 — AGP_MB_8X_DET#_R — AGP_DBI_HI_R — AGP_SBA1 — AGP_SBA3 — AGP_SBA5 — AGP_SBA7 — AGP_AD30 — AGP_AD28 — AGP_AD26 — AGP_AD24 — AGP_C/BE#3 — AGP_AD22 — AGP_AD20 — AGP_AD18 — AGP_AD16 — AGP_PAR_R — AGP_AD15 — AGP_AD13 — AGP_AD11 — AGP_AD9 — AGP_C/BE#0 — AGP_AD6 — AGP_AD4 — AGP_AD2 — AGP_AD0 — AGP_VREFGC

(23) AGP_INTR# — (23) AGP_GNT# — (23) AGP_MB_8X_DET# — (23) AGP_DBI_HI — (23) AGP_WBF# — (23) AGP_SBSTB# — (23) AGP_ADSTB1# — (23) AGP_FRAME# — (23) AGP_TRDY# — (23) AGP_STOP# — (23) AGP_PAR — (23) AGP_ADSTB0#

R7 0R 402 — R9 0R 402 — R1 0R 402 — R5 0R 402 — R12 0R 402

AGP_AGPCLK (23) — AGP_REQ# (23) — AGP_RBF# (23) — AGP_DBI_LO (23) — AGP_SBSTB (23) — AGP_ADSTB1 (23) — AGP_IRDY# (23) — AGP_DEVSEL# (23) — AGP_ADSTB0 (23)

AGP_DBI_LO_R — R8 0R 402
AGP_SBSTB_R — R2 0R 402
AGP_ADSTB1_R — R10 0R 402
AGP_ADSTB0_R — R13 0R 402

AGP_AGPREF

+5V_BUS — R1834 10K — C972 100nF — U2A 74ACT08MTC — AGP_CON_RESET# — R1837 100R — AGP_RESET# (19,20,23) — R1838 180R

+12V_BUS — C22 100nF 402 — +5V_BUS — C25 100nF 402 — +3.3V_BUS — C24 100nF 402

Caps for EMI - install close to AGP connector

AGP_TYPEDET# — R19 5.1R — +12V, TYPEDET# short protection for OEM (5.1R)

AGP_GC_8X_DET# — R64 0R 402

UNIVERSAL VREFGC CIRCUIT (4X, 8X)

(23) AGP_MB_8X_DET# — AGP_MB_8X_DET# — R17 47K 402 — Q20 BSN20 — R6 20K 402 — TEST

+VDDQ_BUS — Q1 2N7002E — R20 324R 402 — AGP_VREFGC — R21 147R — R24 100R 402 — C6 10nF 402 — Close to ASIC

+5V_BUS — C3 100nF 402 — U4 TC7SZ08FU — R23 1K 402

May be placed far from connector -- place C3 FAR from connector, on left side!!

UNIVERSAL VREFCG CIRCUIT (4X, 8X)

AGP_AGPREF — +VDDQ_BUS — TEST — Q77 2N7002E — R72 147R — R75 324R 402 — DNI R73 0R 402 — AGP_AGPREFCG — AGP_AGPREFCG (23) — R74 100R 402 — C11 10nF 402 — Close to ASIC

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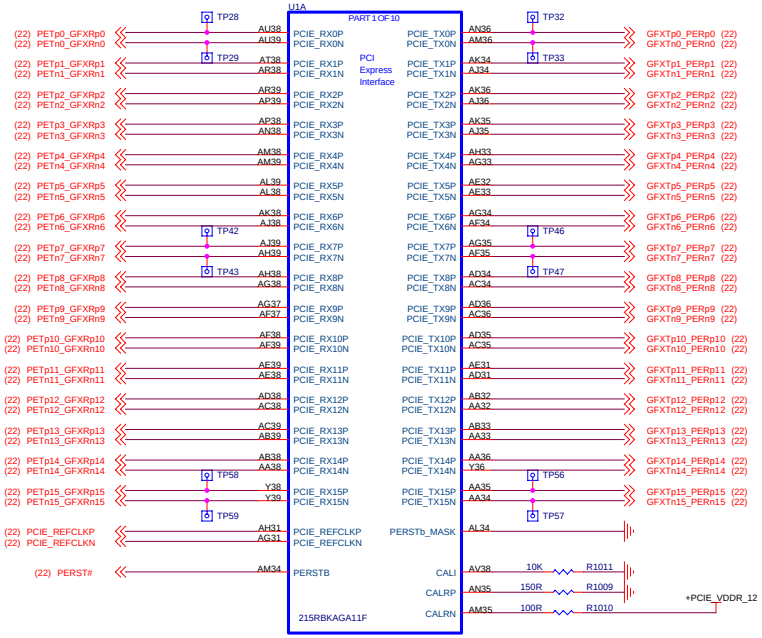
Place the Test Points close to U1

ATI PN# 215RBKAGA11F



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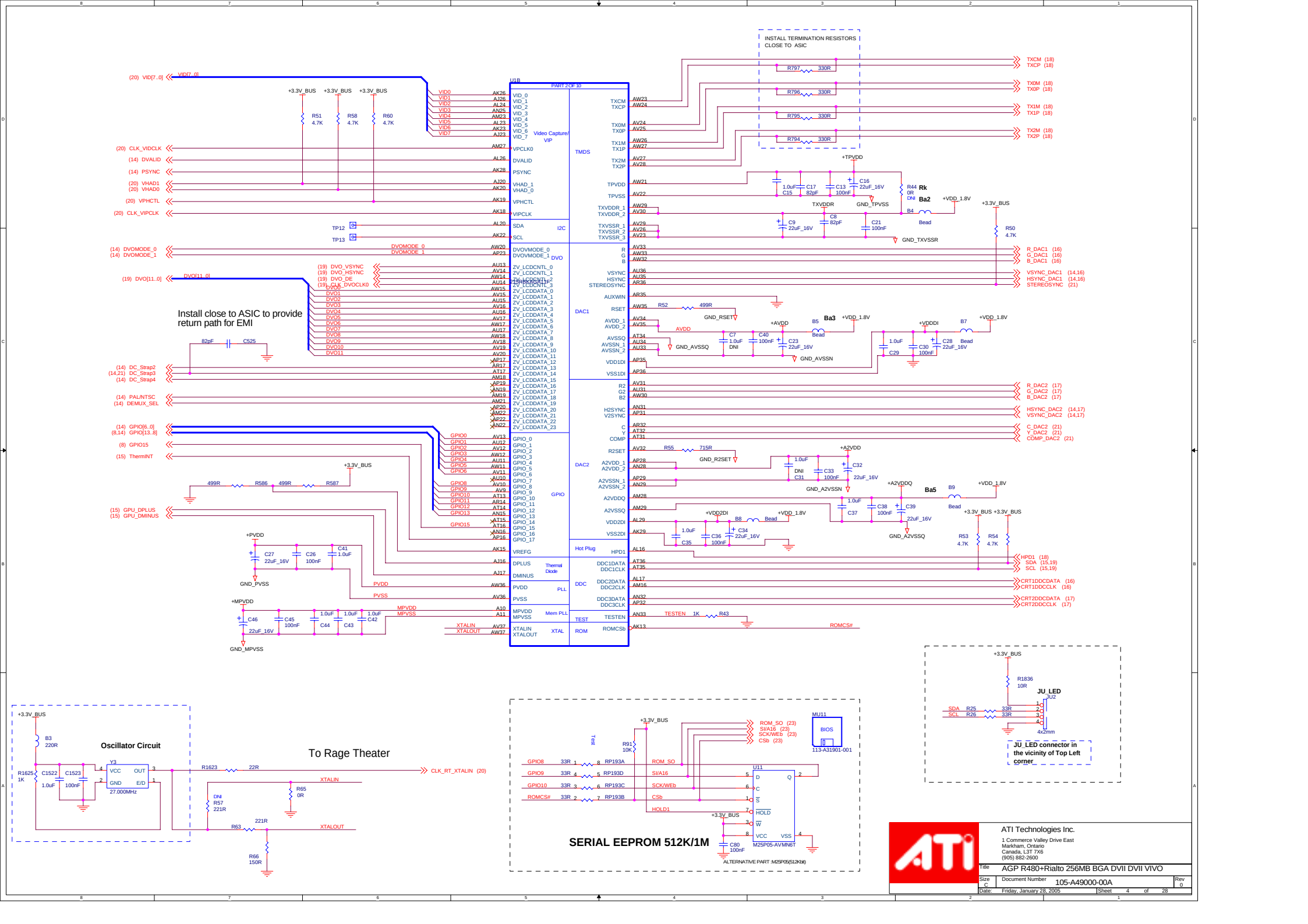
INSTALL TERMINATION RESISTORS CLOSE TO ASIC
U1B
PART 2 OF 10
Video Capture/ VIP
I2C
TMDS
DVO
DAC1
DAC2
GPIO
Hot Plug
HPD1
DDC
PLL
Mem PLL
TEST
TESTEN
XTAL
ROM
Thermal Diode
Install close to ASIC to provide return path for EMI
To Rage Theater
Oscillator Circuit
27.000MHz
SERIAL EEPROM 512K/1M
M25P05-AVMN6T
ALTERNATIVE PART: M25P05(512Kbit)
BIOS
113-A31901-001
JU_LED
JU2
JU_LED connector in the vicinity of Top Left corner
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AGP R480+Rialto 256MB BGA DVII DVII VIVO
105-A49000-00A
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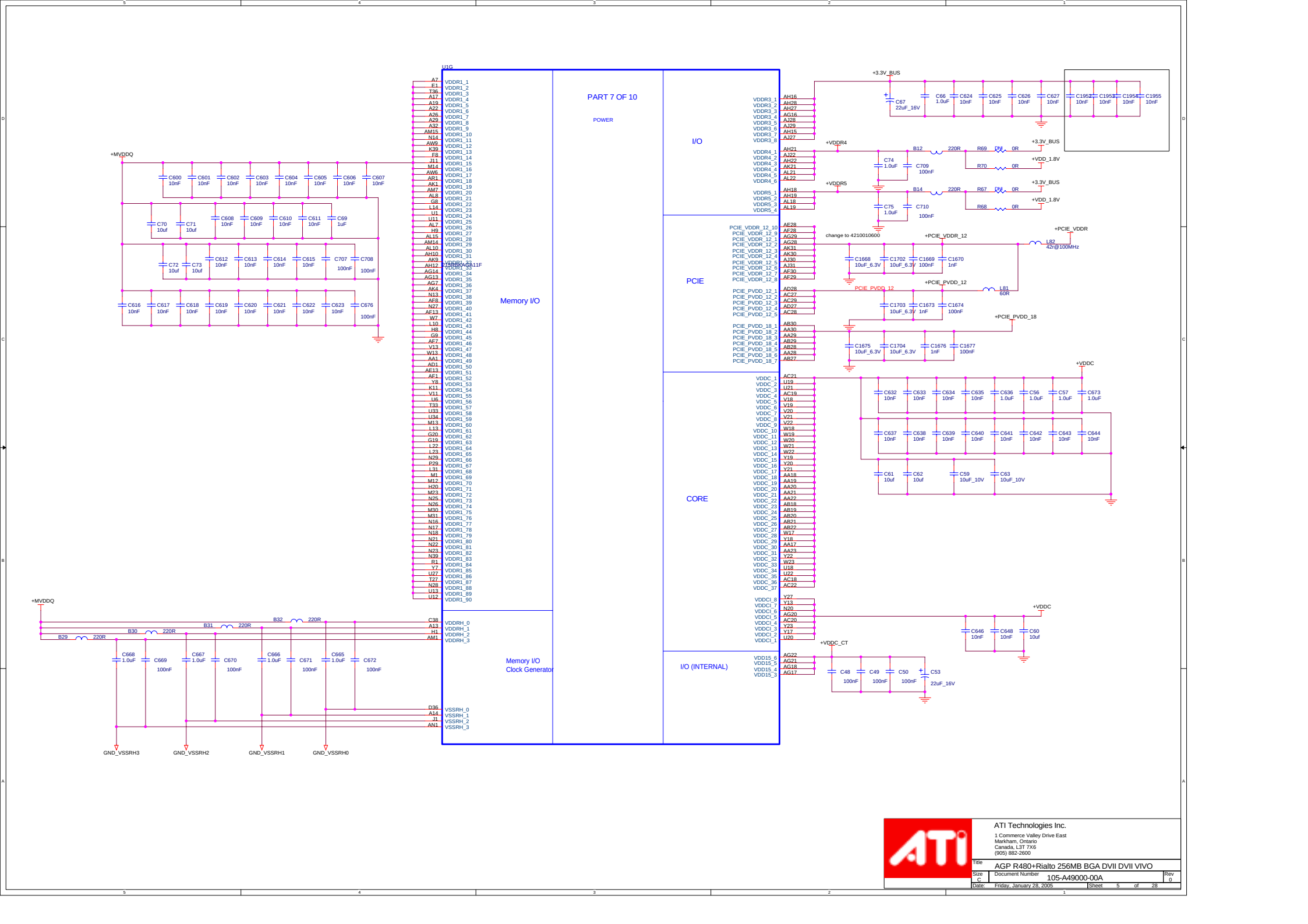

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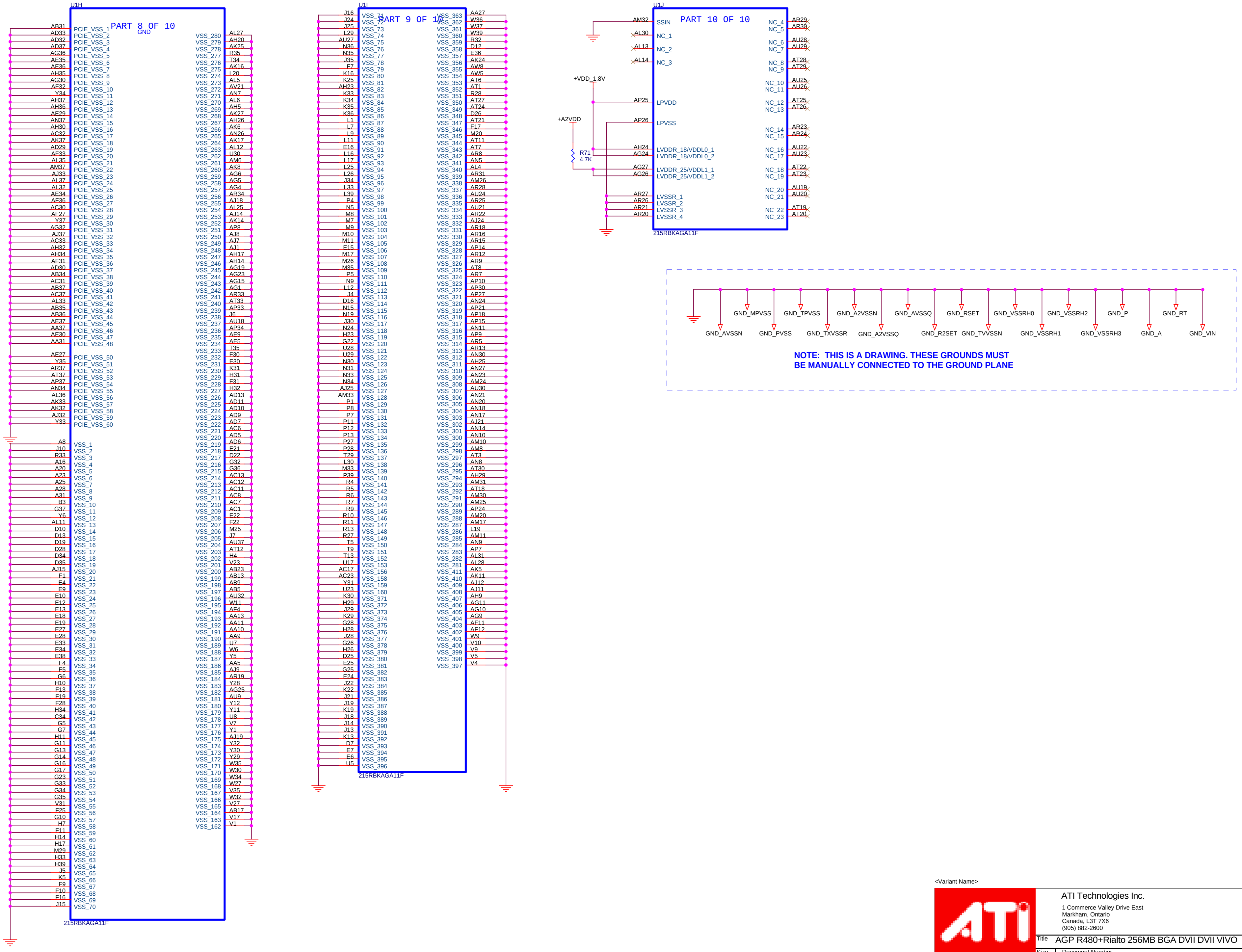

<Variant Name>

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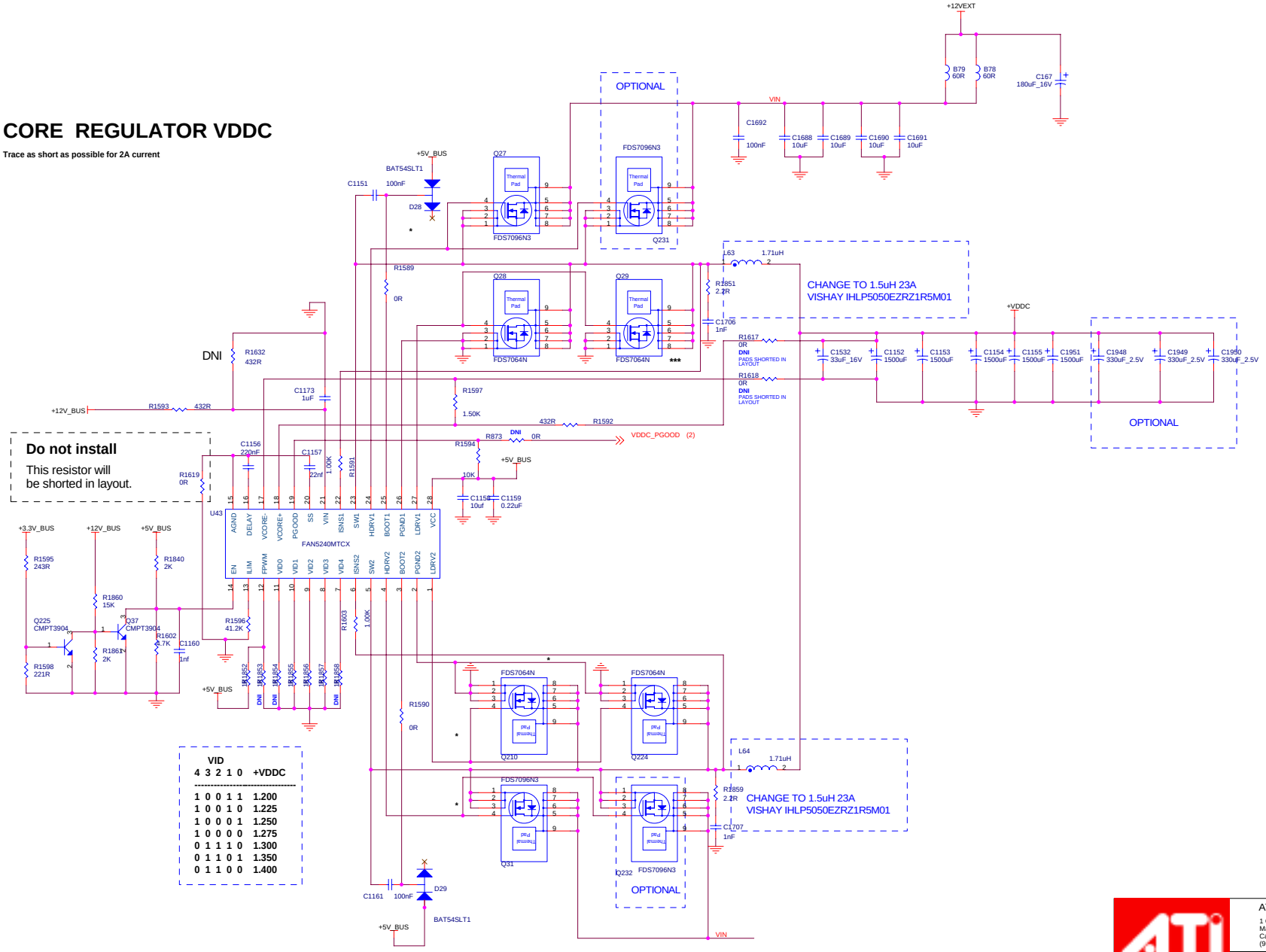
CORE REGULATOR VDDC

Trace as short as possible for 2A current



VID					
4	3	2	1	0	+VDDC
1	0	0	1	1	1.200
1	0	0	1	0	1.225
1	0	0	0	1	1.250
1	0	0	0	0	1.275
0	1	1	1	0	1.300
0	1	1	0	1	1.350
0	1	1	0	0	1.400

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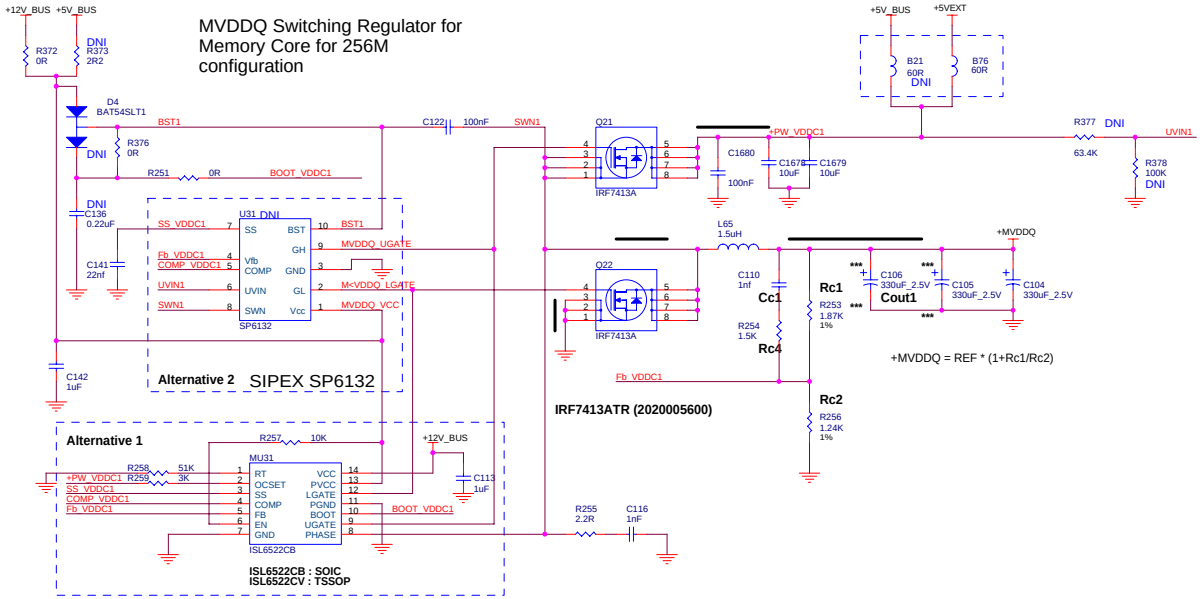
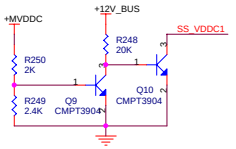
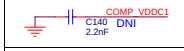


POWER SEQUENCING CIRCUIT:

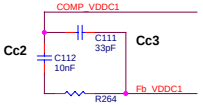


DESIGN NOTES:

Add this Capacitor for SP6132

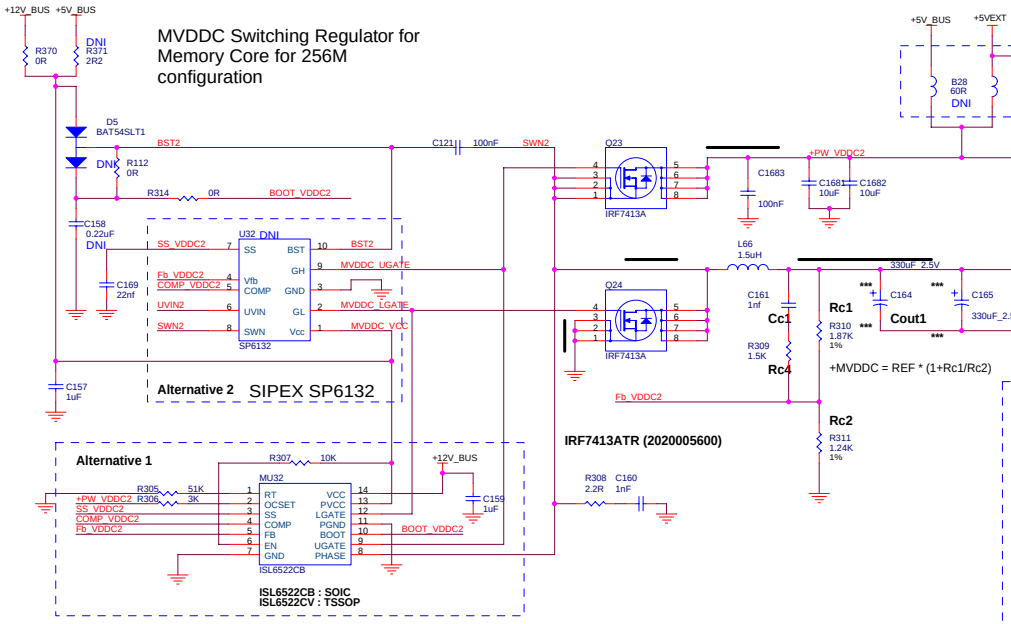


Compensation Circuit

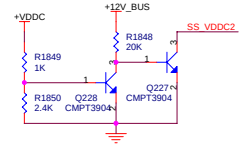


FOR ALTERNATE #2

Change C142 for 10uF
Change C122 for 1uF
Replace R251 with a bead
Swap Rc4 with Cc1



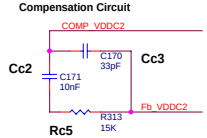
POWER SEQUENCING CIRCUIT:



DESIGN NOTES:

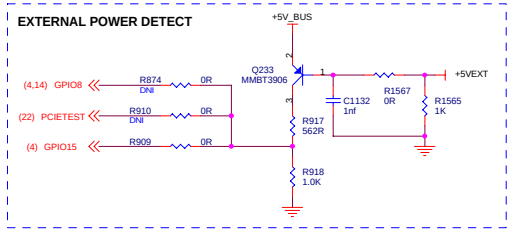
Add this Capacitor for SP6132

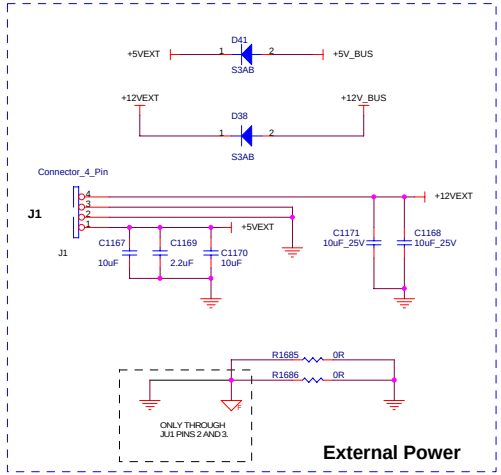
Compensation Circuit



FOR ALTERNATE #2

Change C157 for 10 uF
Change C121 for 1 uF
Replace C764 by 0 Ohm resistor
Remove R954
Replace R314 with a bead
Swap Rc4 with Cc1





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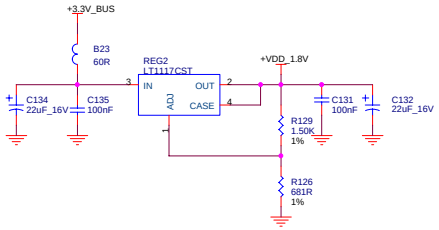
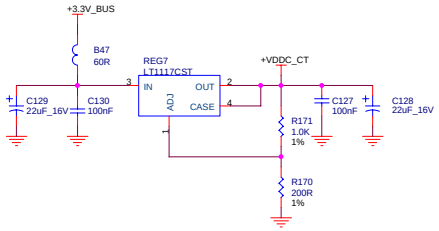
+1.8V Regulator for analog power supplies

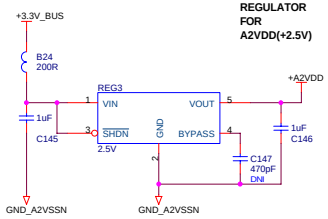


Max 400 mA if all 1.8 V analog power supplies are connected

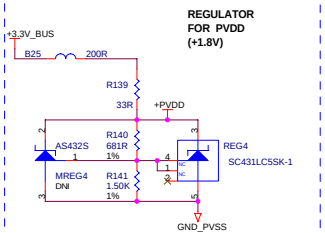
+1.5V Regulator for VDDC_CT (VDD15)



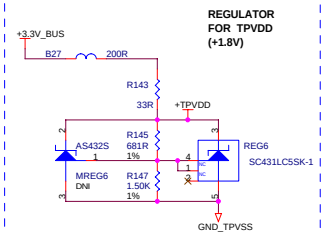
REGULATOR FOR A2VDD(+2.5V)



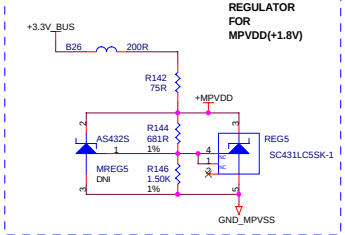
REGULATOR FOR PVDD (+1.8V)



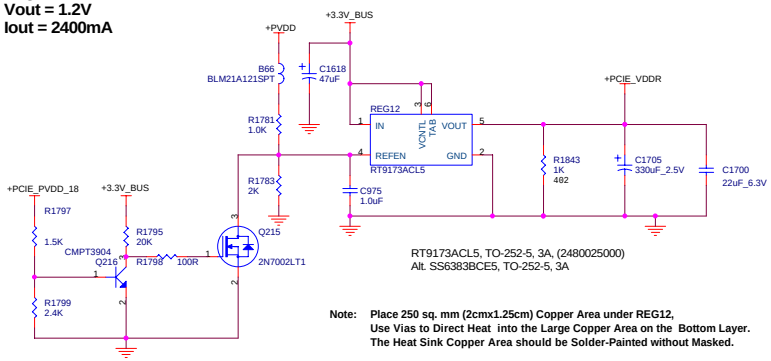
REGULATOR FOR TPVDD (+1.8V)



REGULATOR FOR MPVDD(+1.8V)



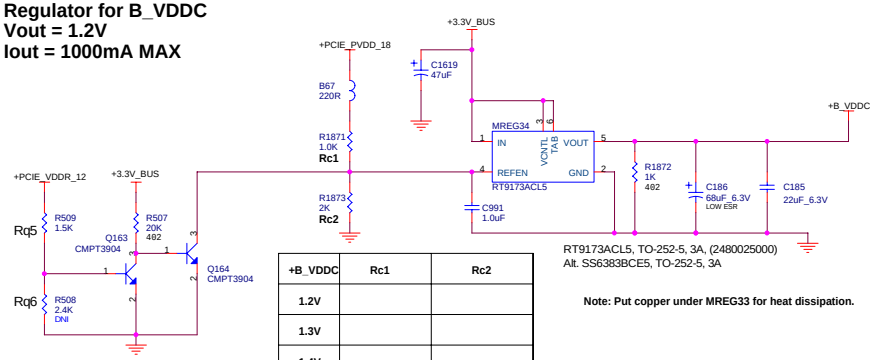
Regulator for PCIE_VDDR
Vout = 1.2V
Iout = 2400mA



RT9173ACL5, TO-252-5, 3A, (2480025000)
Alt. SS6383BCE5, TO-252-5, 3A

Note: Place 250 sq. mm (2cmx1.25cm) Copper Area under REG12, Use Vias to Direct Heat into the Large Copper Area on the Bottom Layer. The Heat Sink Copper Area should be Solder-Painted without Masked.

Regulator for B_VDDC
Vout = 1.2V
Iout = 1000mA MAX

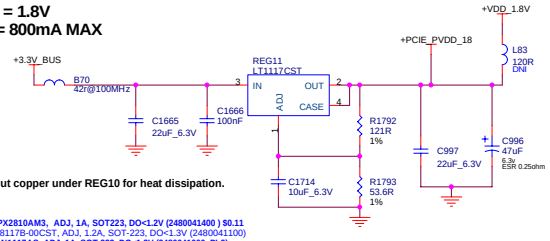


+B_VDDC	Rc1	Rc2
1.2V		
1.3V		
1.4V		

RT9173ACL5, TO-252-5, 3A, (2480025000)
Alt. SS6383BCE5, TO-252-5, 3A

Note: Put copper under MREG33 for heat dissipation.

Regulator for PCIE_PVDD_18
Vout = 1.8V
Iout = 800mA MAX



Put copper under REG10 for heat dissipation.

C996 can use 4231068600, CAP TANT 68UF 6.3V 20% LOW ESR B CASE

Use SPX2810AM3, ADJ, 1A, SOT223, DO<1.2V (2480041400) $0.11
Alt. LX8117B-00CST, ADJ, 1.2A, SOT-223, DO<1.3V (2480041100)
Alt. FAN1117AS, ADJ, 1A, SOT-223, DO<1.2V (2480041000, PL9)
Alt. FAN1117AS-1.8V, 1A, SOT-223, DO<1.2V (2480020000, PL4), $0.13
Alt. LX8117A-00CST, ADJ, 1A, SOT-223, DO<1.3V (2480002100, PL1), $0.25
Alt. AP1117, ADJ, 1A, SOT-223, DO<1.4V, Use +5V_BUS Input Only, $0.10

* R1792, 3160121000, 121R, 1%, 402
R1793, 3160537600, 53.6R, 1%, 402

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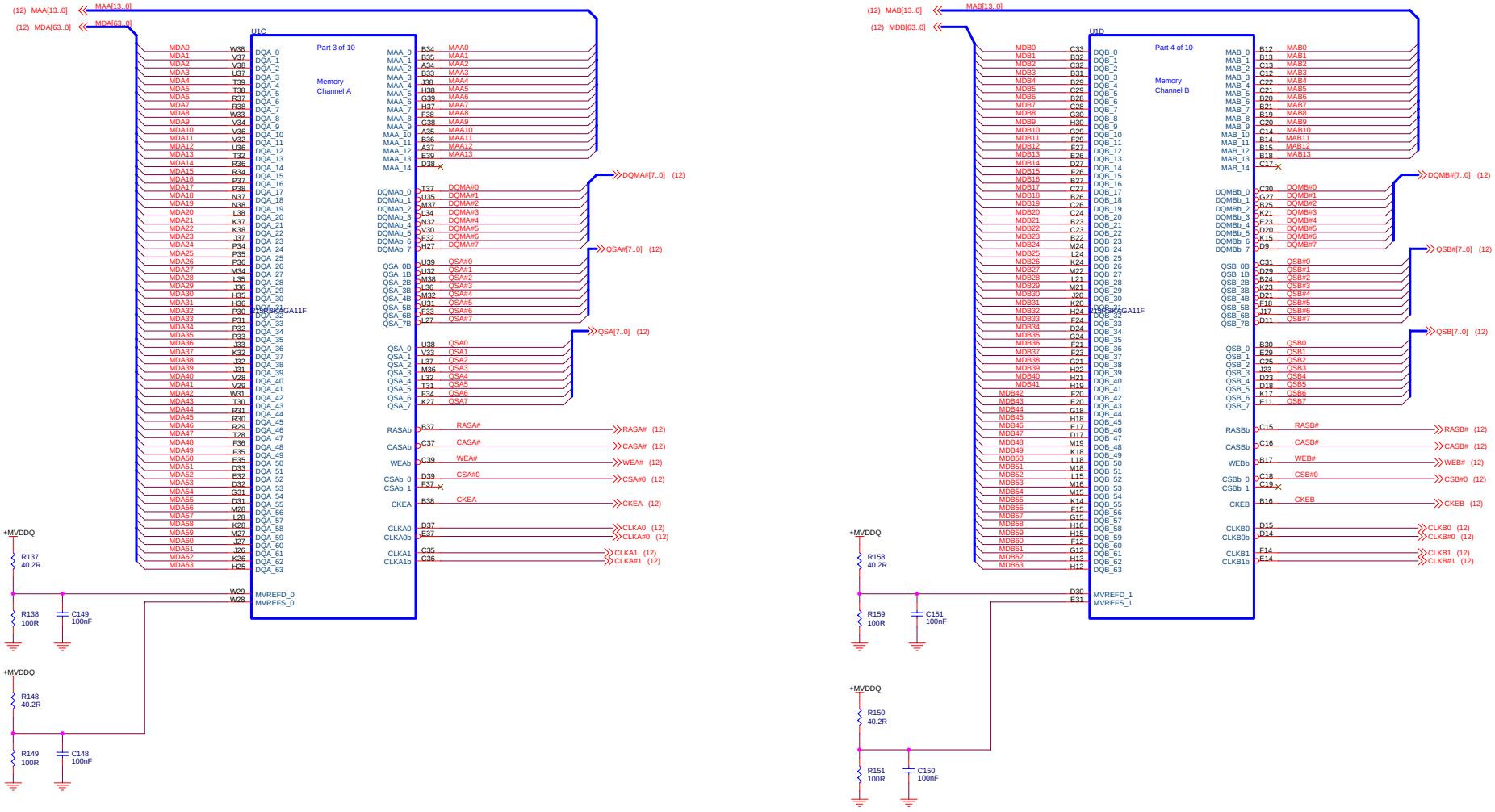
R423 MEMORY CHANNELS A and B



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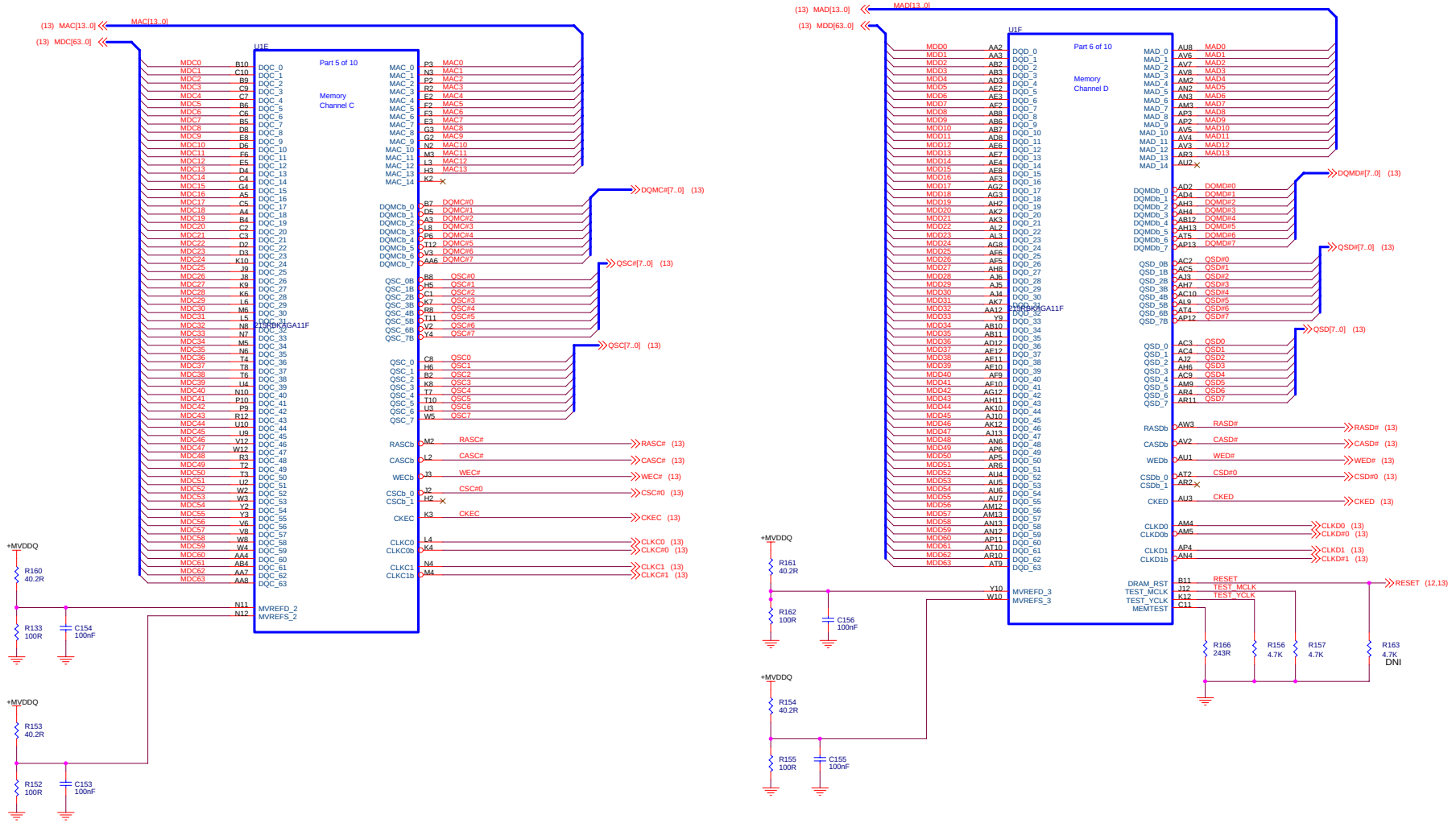
R-420 MEMORY CHANNELS C and D



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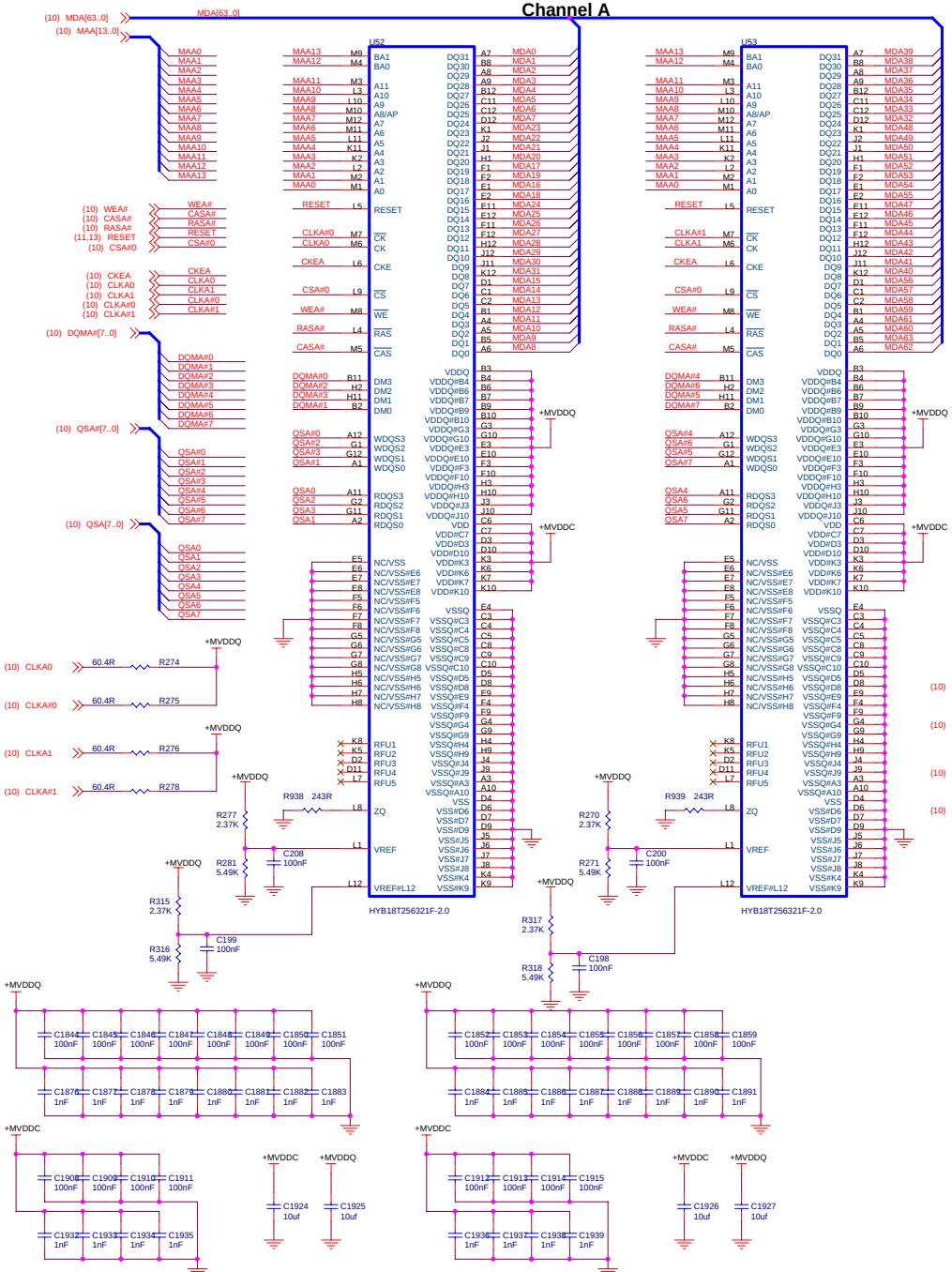
256 Mbit GDDRIII Channels A and B

Channel A



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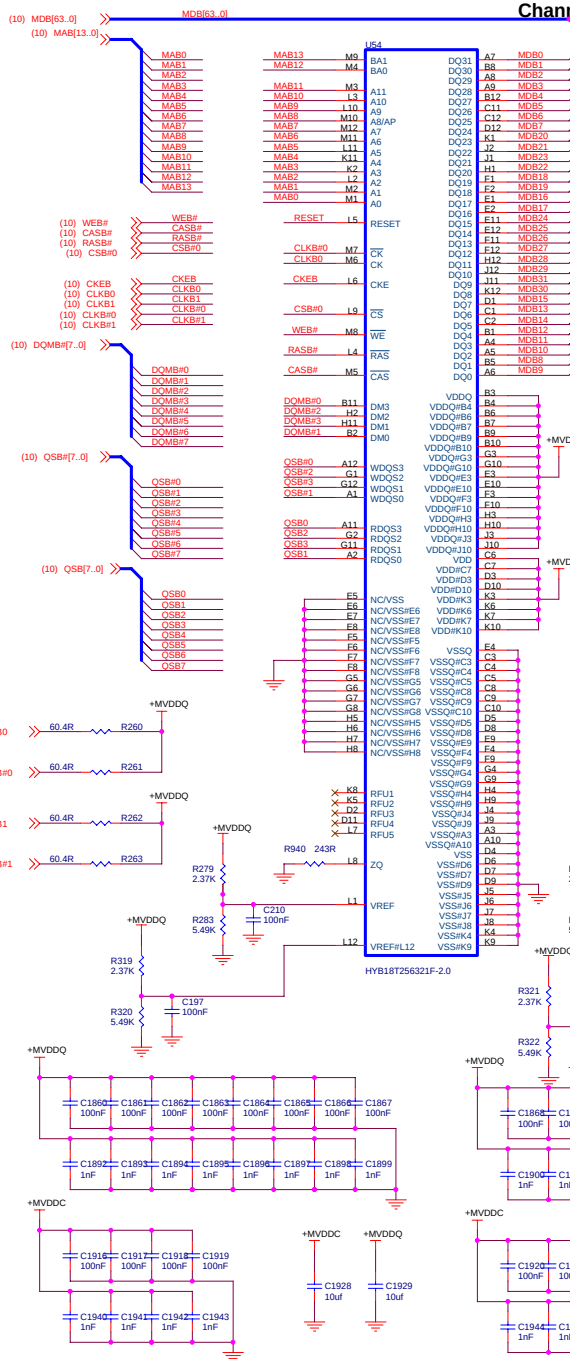

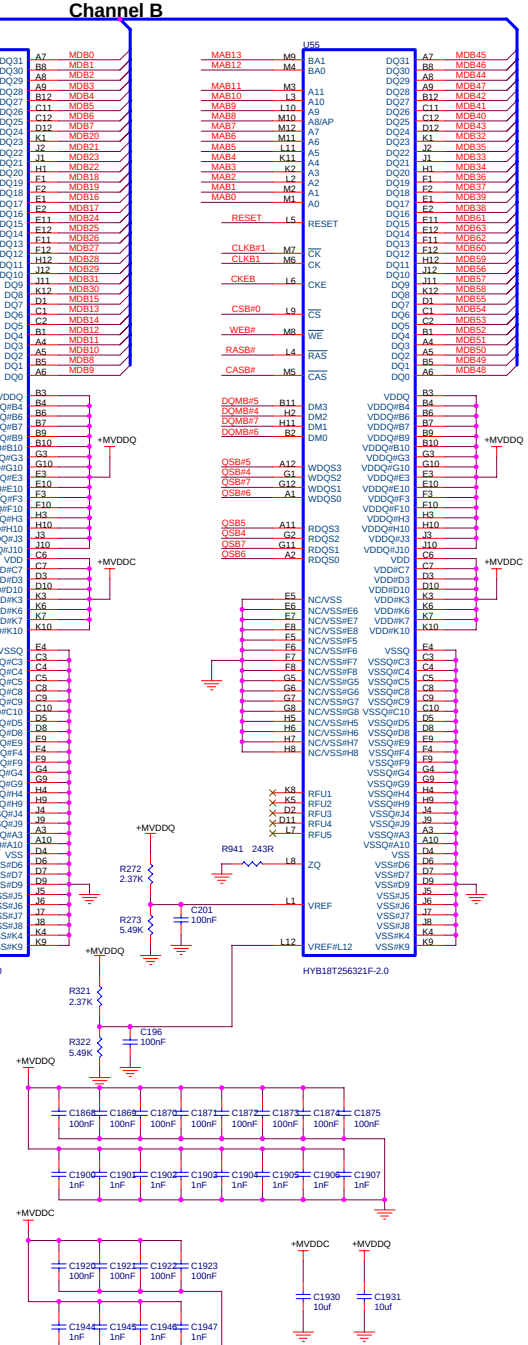

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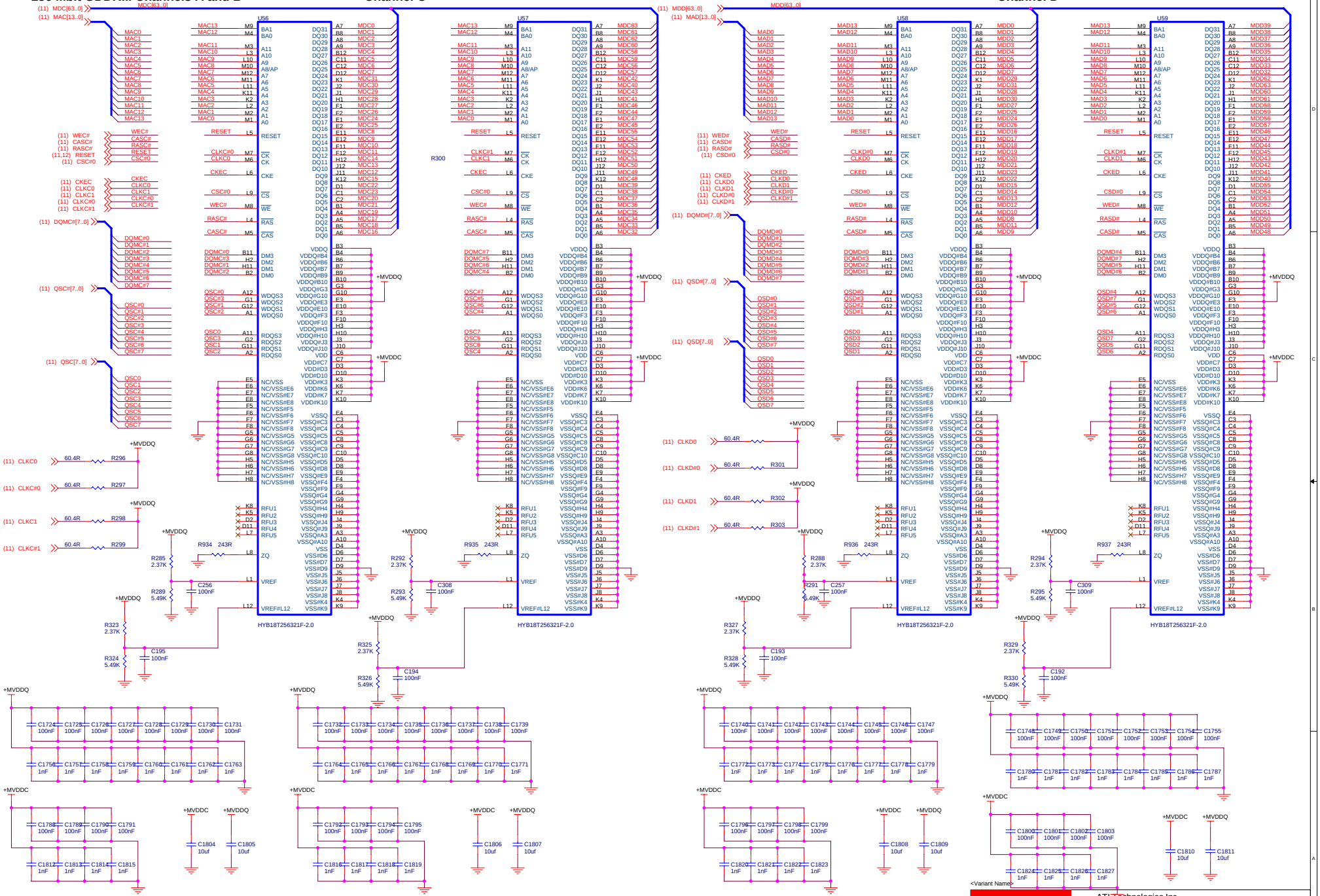
256 Mbit GDDRIII Channels A and B

Channel C

Channel D



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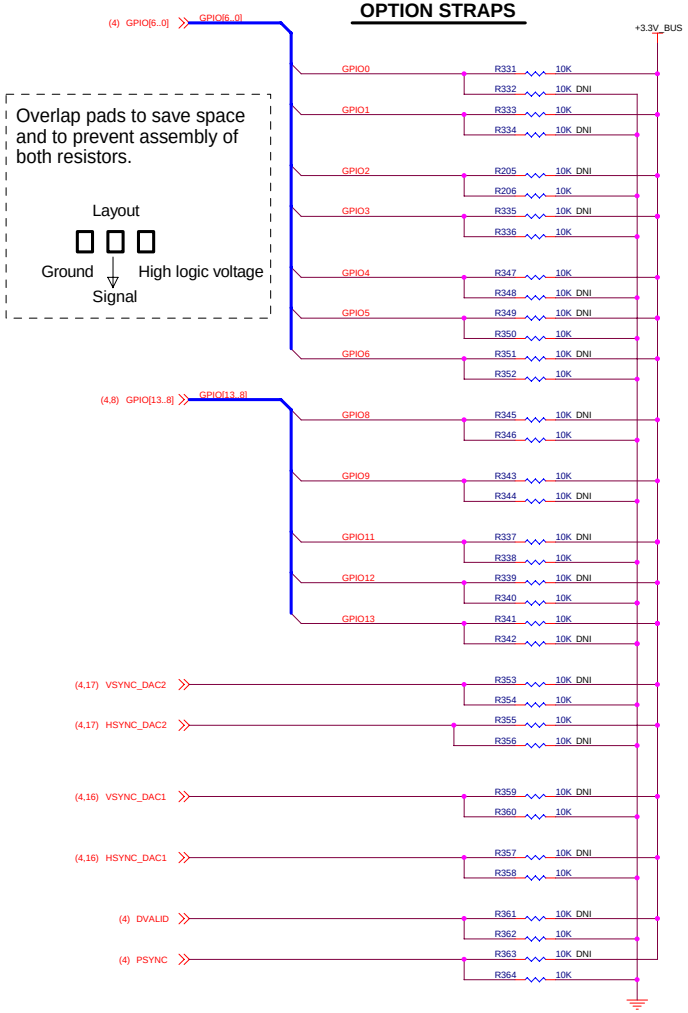
OPTION STRAPS



Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground — High logic voltage

Signal

R423 Shared Straps — REV. 0.0

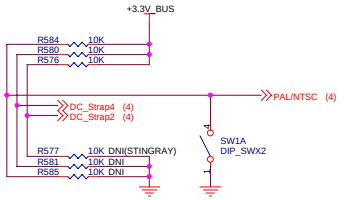
STRAPS	PIN	DESCRIPTION	DEFAULT
MOBILE_FEATURE0	GPIO(0)	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Desktop must have an external pullup)	0
MOBILE_FEATURE1	GPIO(1)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Desktop must have an external pullup)	0
PCIE_MODE (ATI Internal)	GPIO(3:2)	PCIE mode: 00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: Short-circuit internal loopback and PCI Express 1.0A mode	00
TX_IEXT	GPIO(4)	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
FORCE _COMPLIANCE	GPIO(5)	Force chip to get to compliance state quickly for Tester purposes 0: Normal operation 1: Force to compliance state	0
PLL_BW (ATI Internal)	GPIO(6)	0: Full PLL Bandwidth 1: Reduced PLL bandwidth	0
DEBUG_ACCESS	GPIO(8)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible 0: Disable debug access 1: Enable debug access	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type. GPIO[9,13,12,11] 000x - No ROM,CHG_ID=00 001x - No ROM, CHG_ID=01 010x - No ROM, CHG_ID=10 011x - No ROM, CHG_ID=11 1001 - 1M Serial AT25F1024 ROM (Atmel) 1010 - 1M Serial AT45DB011 ROM (Atmel) 1011 - 1M Serial M25P10 ROM (ST) 1100 - 512K Serial M25P05 ROM (ST) 1101 - 1M Serial SST45LF010 ROM (SST) 1M Serial W45B512 ROM (WinBond) 512K Serial W45B012 ROM (WinBond) 1110 - 1M Serial SST25VF010 ROM (SST) 512K Serial SST25VF512 ROM (SST) 1111 - 1M NX25F011B ROM (NexFlash) **Chip IDs:** Chip ID is based on substrate fuses and CHG_ID strap (which comes from ROM if used, or pin straps if no ROM is connected): CHG_ID = ROMIDCFG[2:1] = GPIO[13:12]	1100
MULTIFUNC(1:0)	H2SYNC, V2SYNC	Multi-function device select 00 - single function device. 01 - two function device. 10 - two function device. 11 - two function device.	10
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present 1 - No slave VIP host port devices reporting presence during reset	1
RFU	HSYNC	RFU 0 - Normal 1 - Not used	0

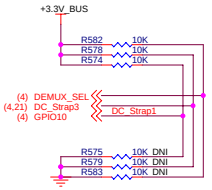
R423 Dedicated Straps — REV. 0.0

ZV_VOLTAGE_SEL0	DVOVMODE_0	DVOVMODE_0 is for ZV_LCDCNTL and ZV_LCDDATA(11:0). 0 - 3.3 V signaling 1 - 1.8 V signaling	0
ZV_VOLTAGE_SEL1	DVOVMODE_1	DVOVMODE_1 is for ZV_LCDDATA(23:12) 0 - 3.3 V signaling 1 - 1.8 V signaling	0

Board Straps — REV. 0.0

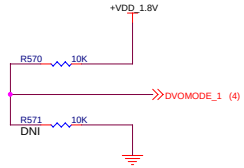
STRAPS	PIN	DESCRIPTION	DEFAULT
MEMTYPE(1:0)	DVALID, PSYNC.	Memory connected to R420 identification for BIOS 00 - Samsung GDDR 3 memory 144 Ball BGA package 01 - TBD 10 - TBD 11 - TBD	000
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled 1 - Enabled	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled 0 - Disabled 1 - Enabled	0
DC_Strap3	LCDDATA(14)	Not defined	0
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 -NTSC (on board resistor pull-up)	1
EXT_PWR	GPIO15	External power cable detect 0 - Cable is properly connected 1 - Cable is not properly connected. Software should prevent the board from booting, should display a warning at screen and should decrease engine and memory clock speed.	NA

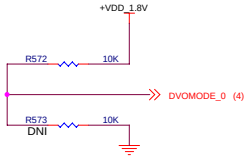




WARNING

Some of those straps must be connected to +VDD_1.8V if ZV_LCDATA bus is set to 1.8 V.





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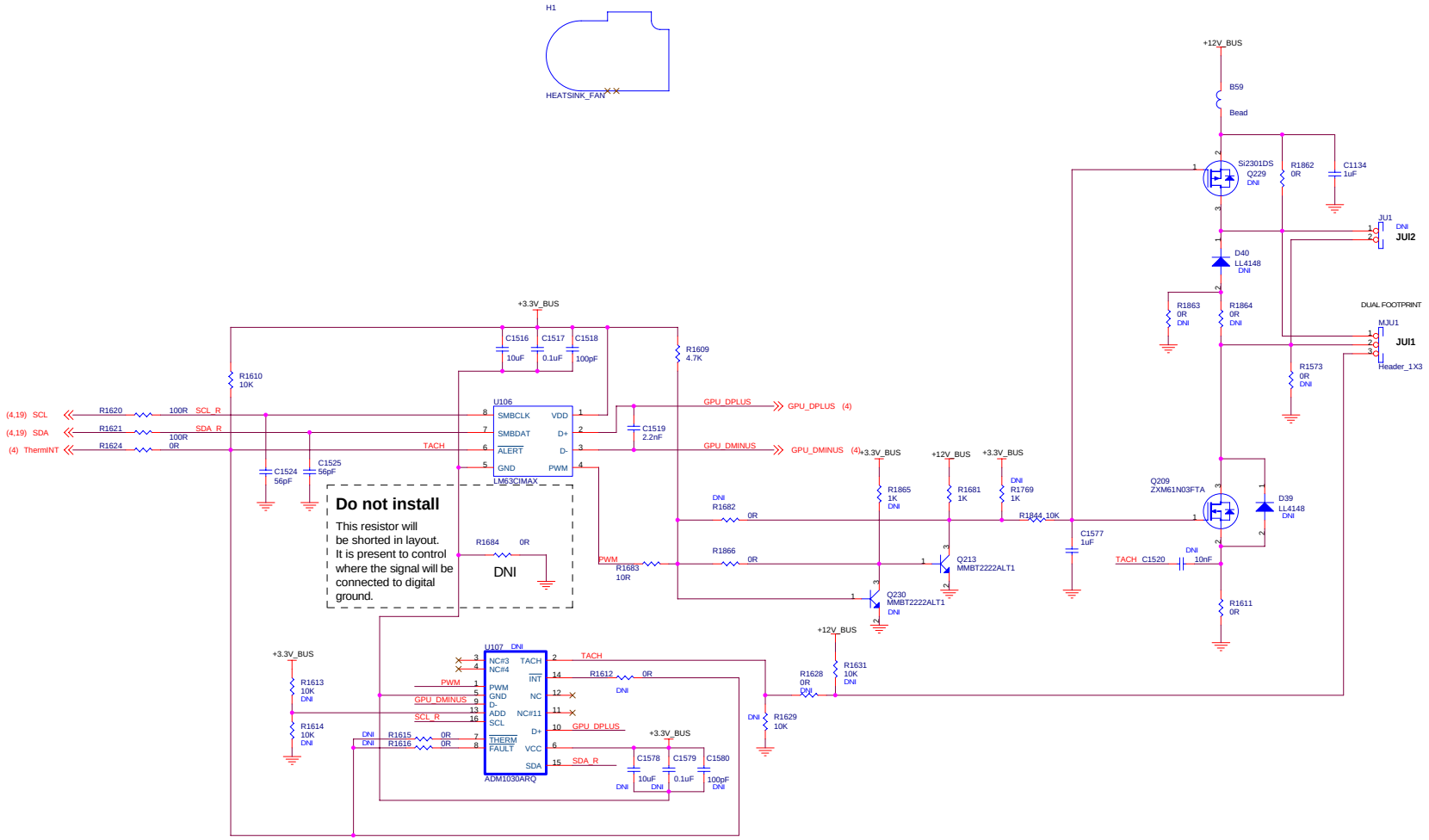
TEMPERATURE SENSE AND SPEED CONTROLLED FAN



Change to Maxim part

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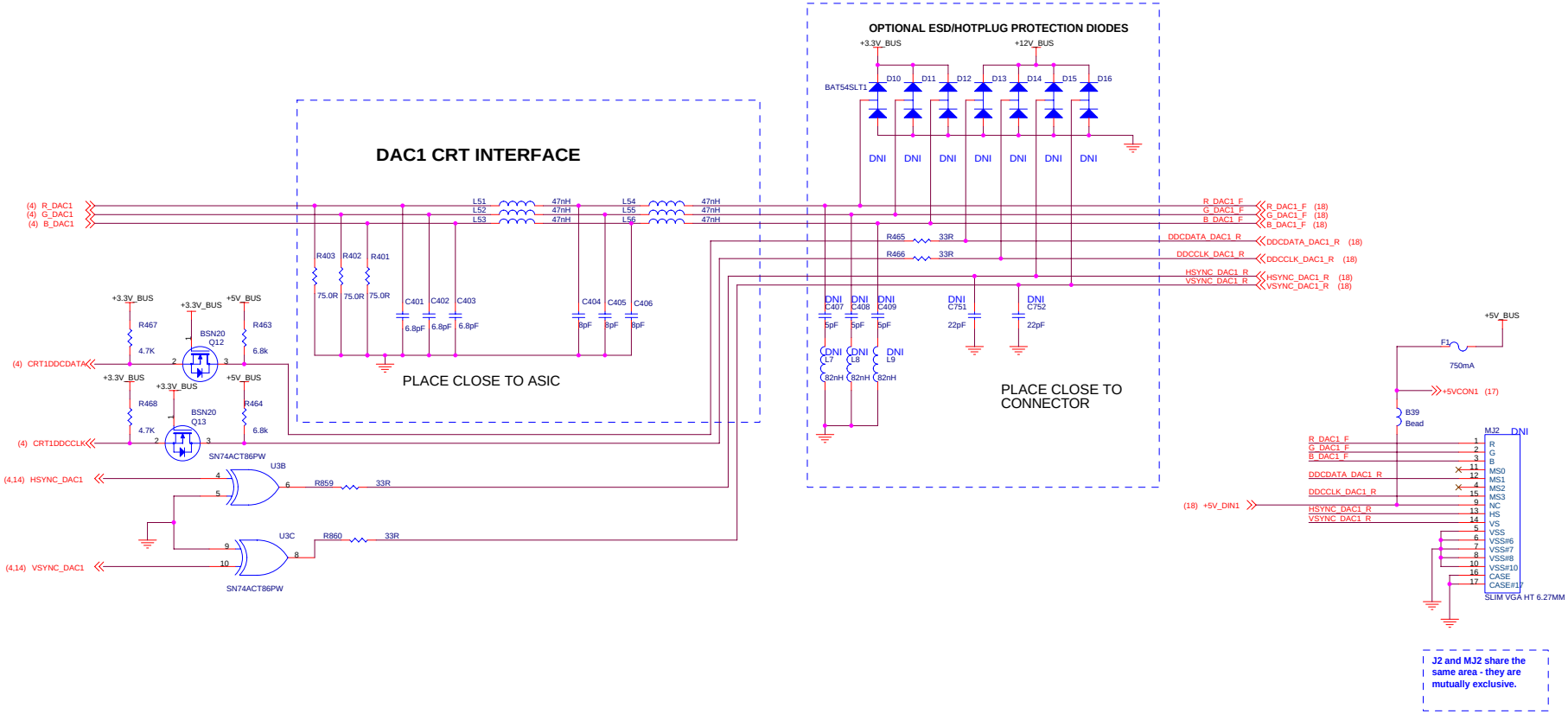

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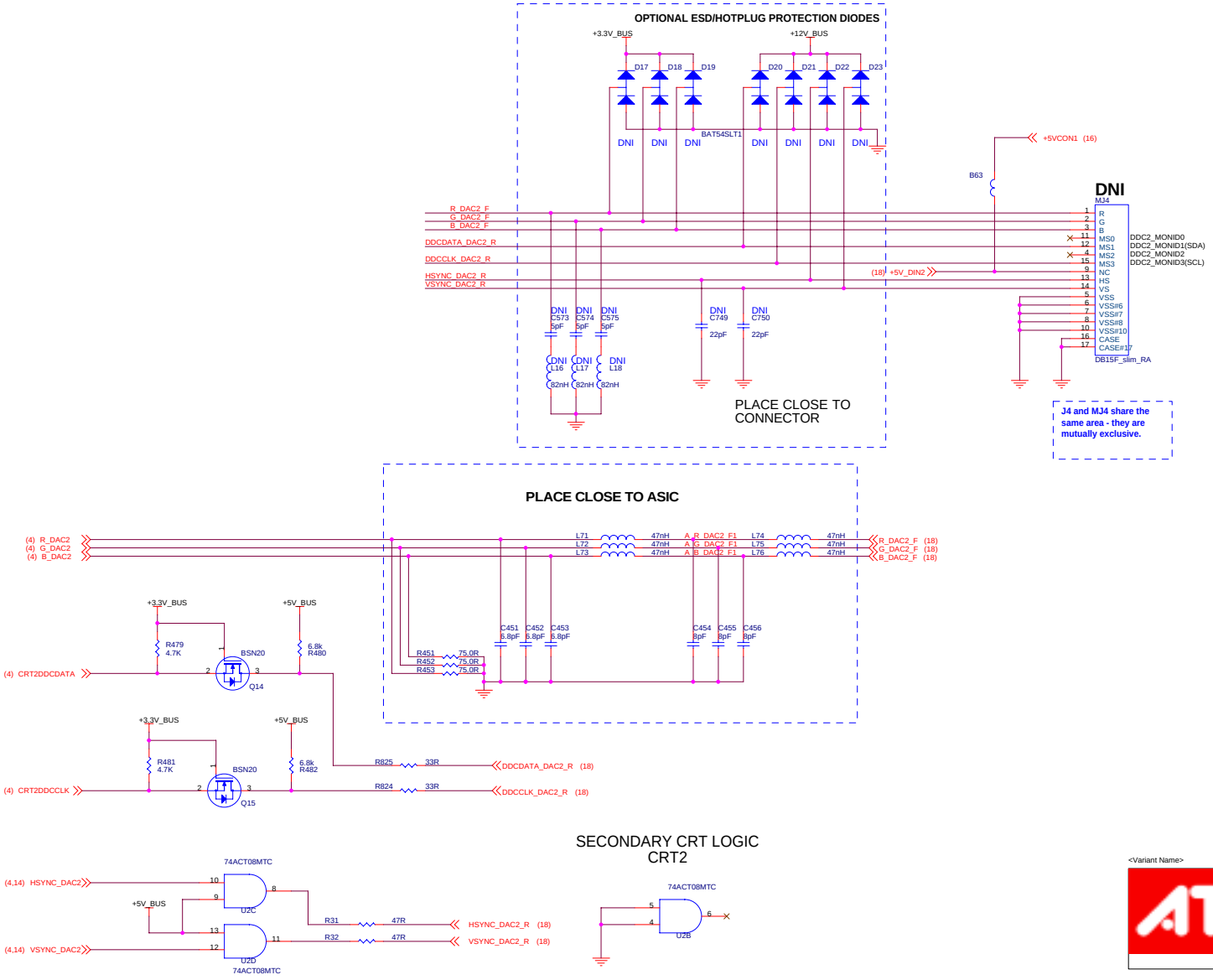

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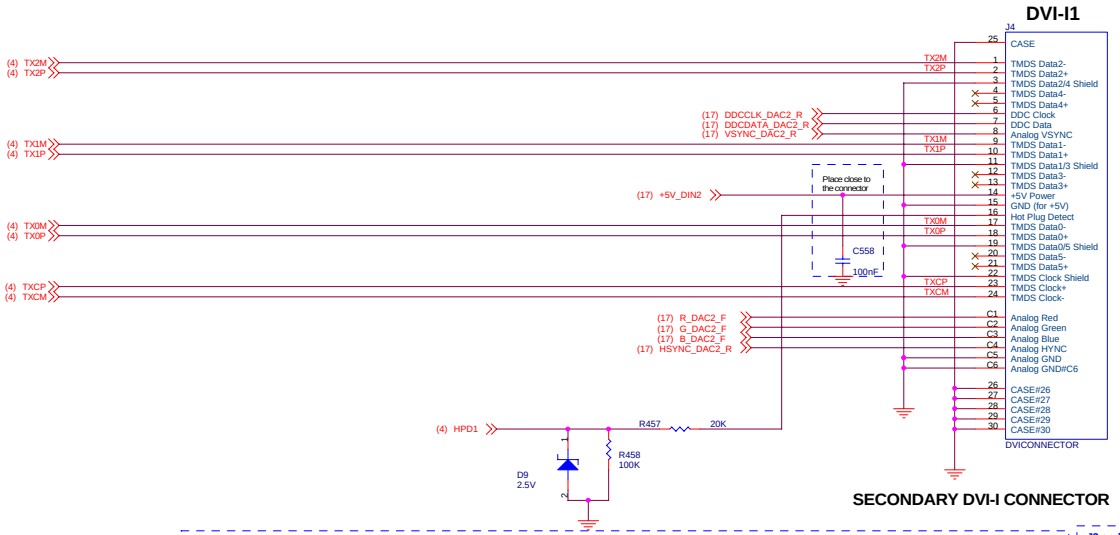
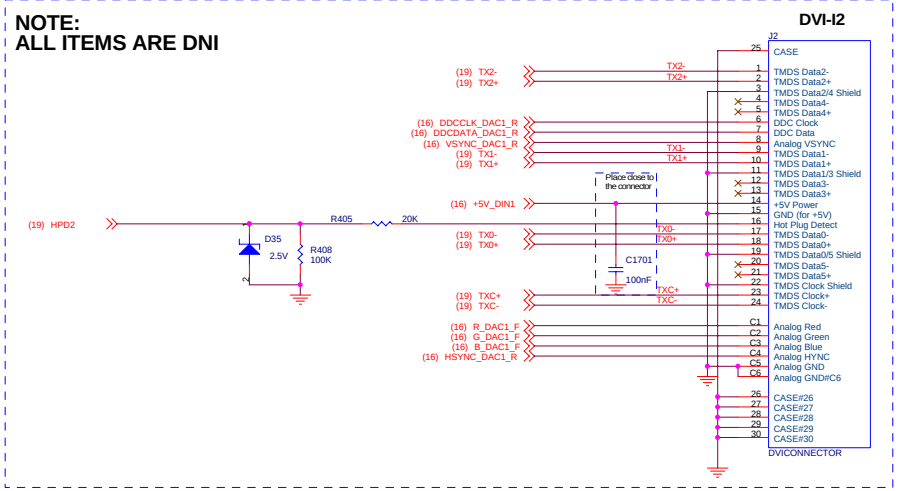
PRIMARY DVI-I CONNECTOR (DVI-I1)



SECONDARY DVI-I CONNECTOR

NOTE:
ALL ITEMS ARE DNI

J2 and MJ2 share the same area - they are mutually exclusive.



<variant_name>

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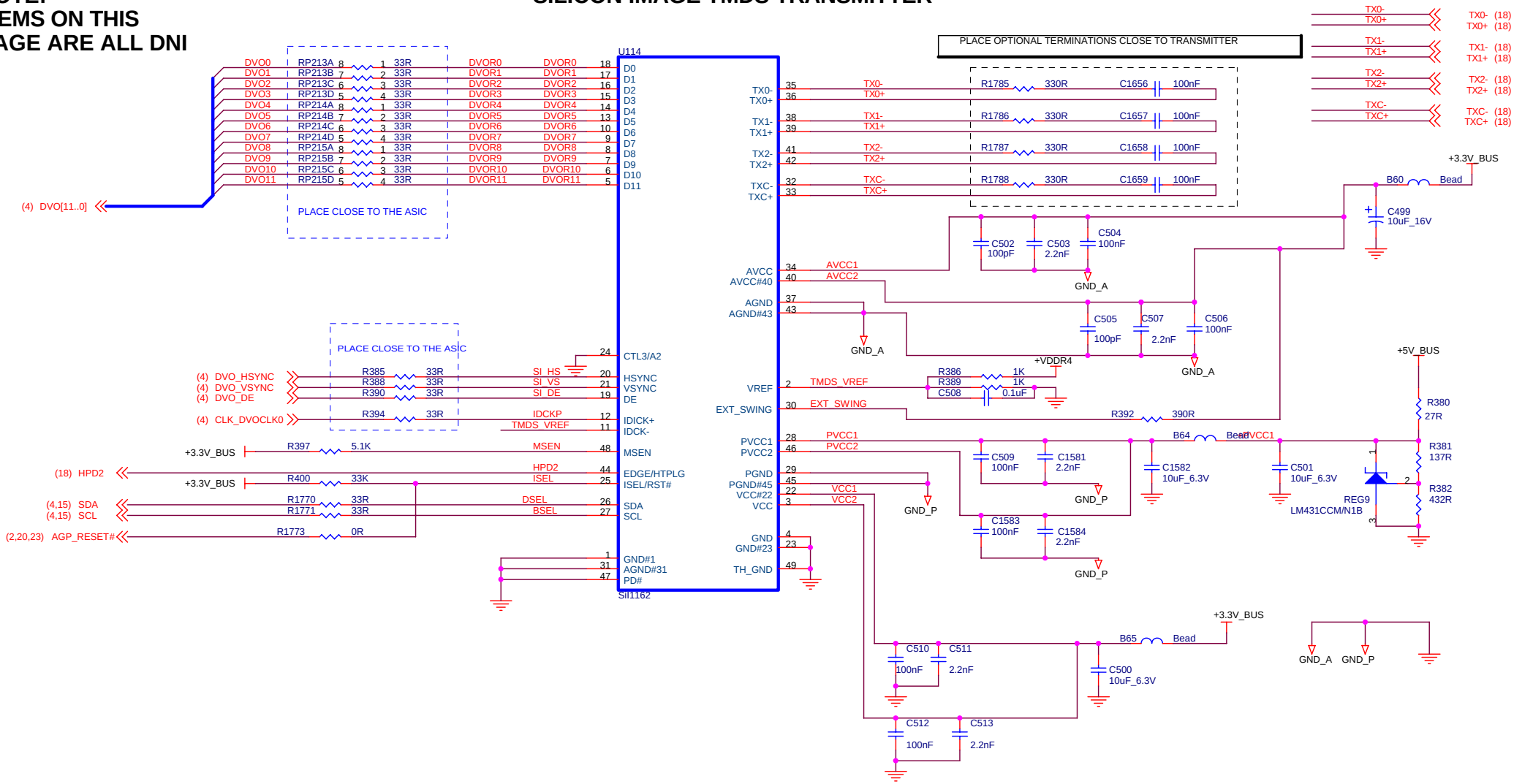
NOTE:
ITEMS ON THIS
PAGE ARE ALL DNI

SILICON IMAGE TMDS TRANSMITTER



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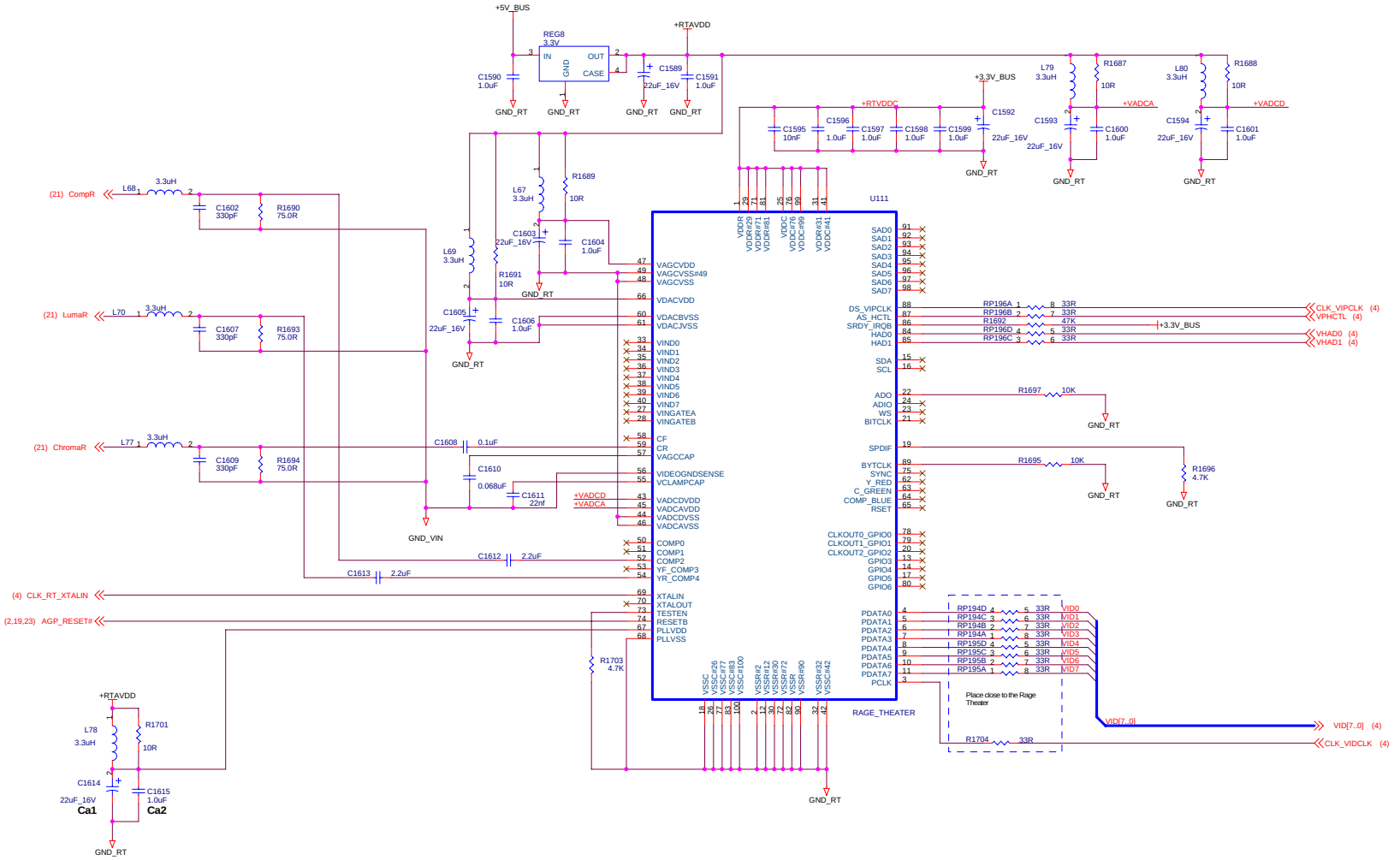
NOTE:
ITEMS ON THIS
PAGE ARE ALL DNI



Layout Guide line of THEATER

#1 : Ca1 and Ca2 have to be placed as close as possible to the respective pins of Rage THEATER

#2 : GND_VIN should be seperated from Digital or Chassis Ground and have no loops

#3 : GND_VIN should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

IMPORTANT

Put 2D line as close as possible to pin 56 of Rage Theater

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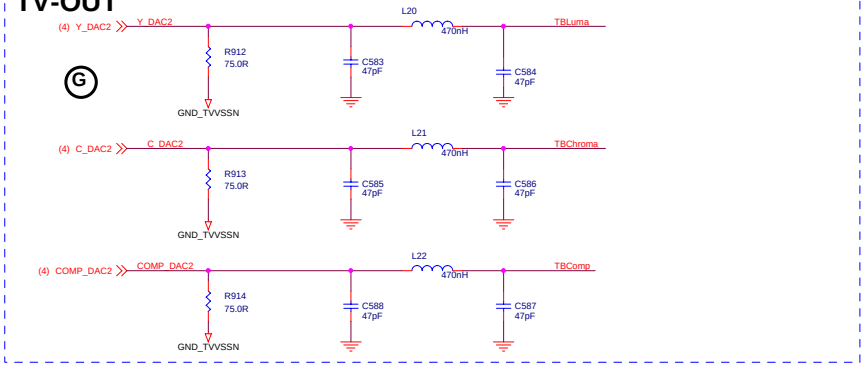
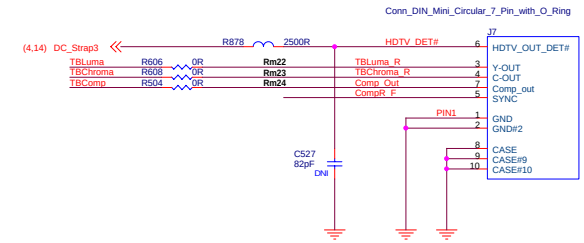
TV-OUT



Footprint - M1

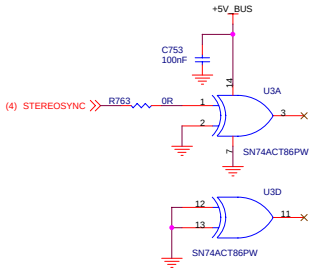
TV Out (SVHS) MiniDIN 7-pin

Jm1



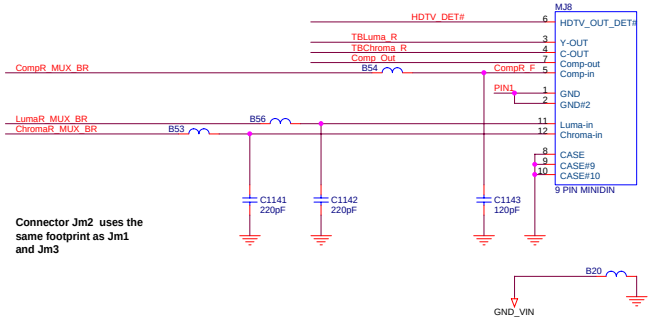
A

Connector Jm1 uses the same footprint as Jm2 and Jm3



NOTE: ALL ITEMS ARE DNI

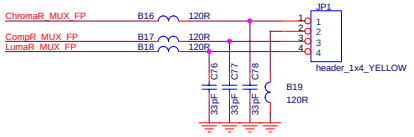
Jm2



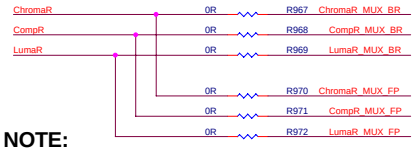
C

Connector Jm2 uses the same footprint as Jm1 and Jm3

NOTE: ALL ITEMS ARE DNI



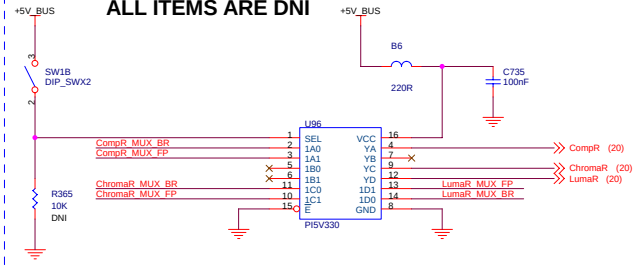
VI MUX BYPASS DNI



NOTE: ALL ITEMS ARE DNI

VI MUX

NOTE: ALL ITEMS ARE DNI



	Install	DNI
TV-OUT 7-PIN MiniDIN **102-00302-00** **102-00305-00**	(A) (B) (E)	(C)
VIVO 9-PIN MiniDIN **102-00303-00** **102-00306-00**	(C)	(A) (B) (E)
No Options (Just DB15)		(A) (B) (C) (E)

(A) (C) share the same footprint

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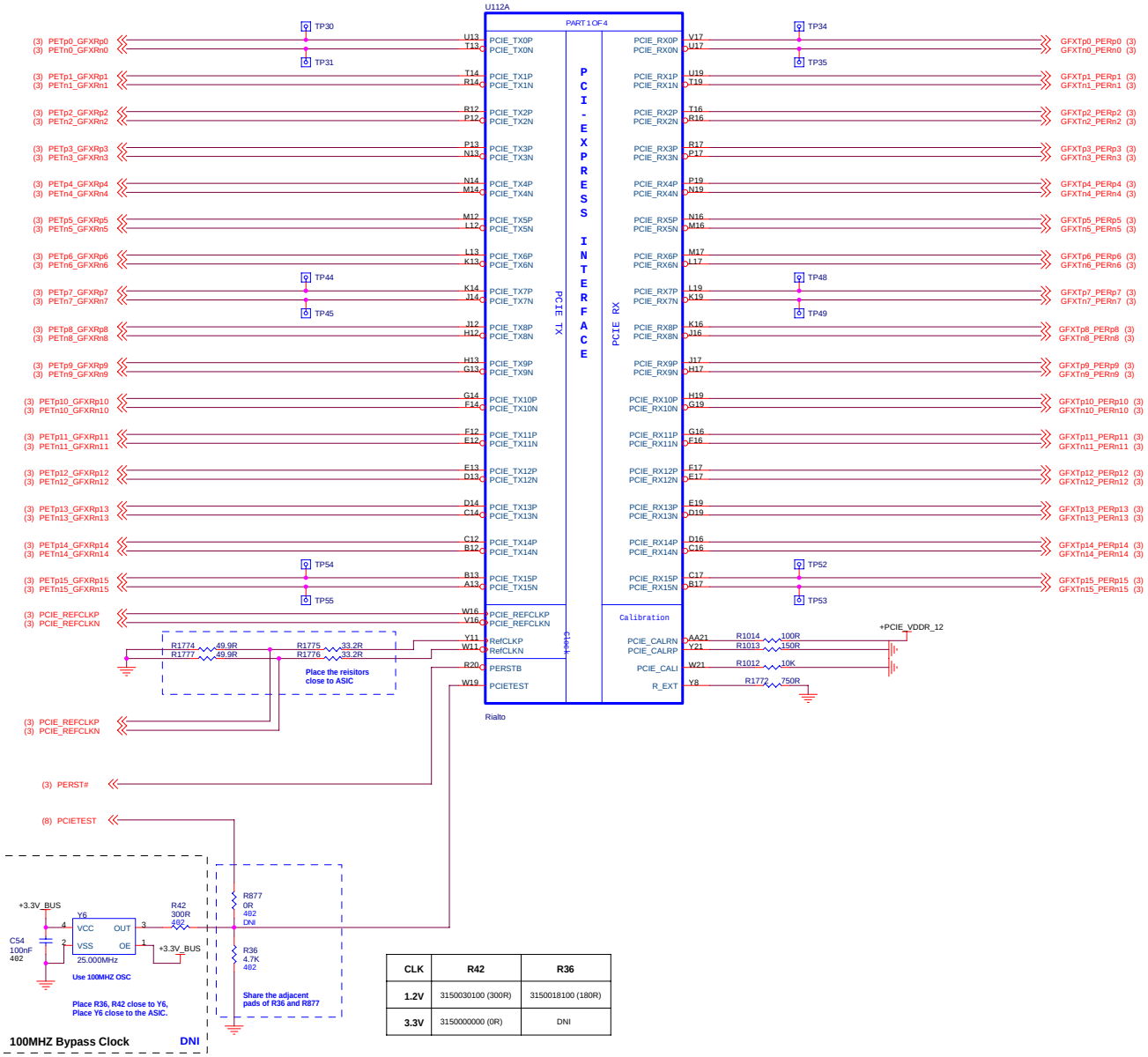
Place the Test Points close to U112

Rialto ASIC p/n is: 218BAPAGA11F



CLK	R42	R36
1.2V	3150030100 (300R)	3150018100 (180R)
3.3V	3150000000 (0R)	DNI

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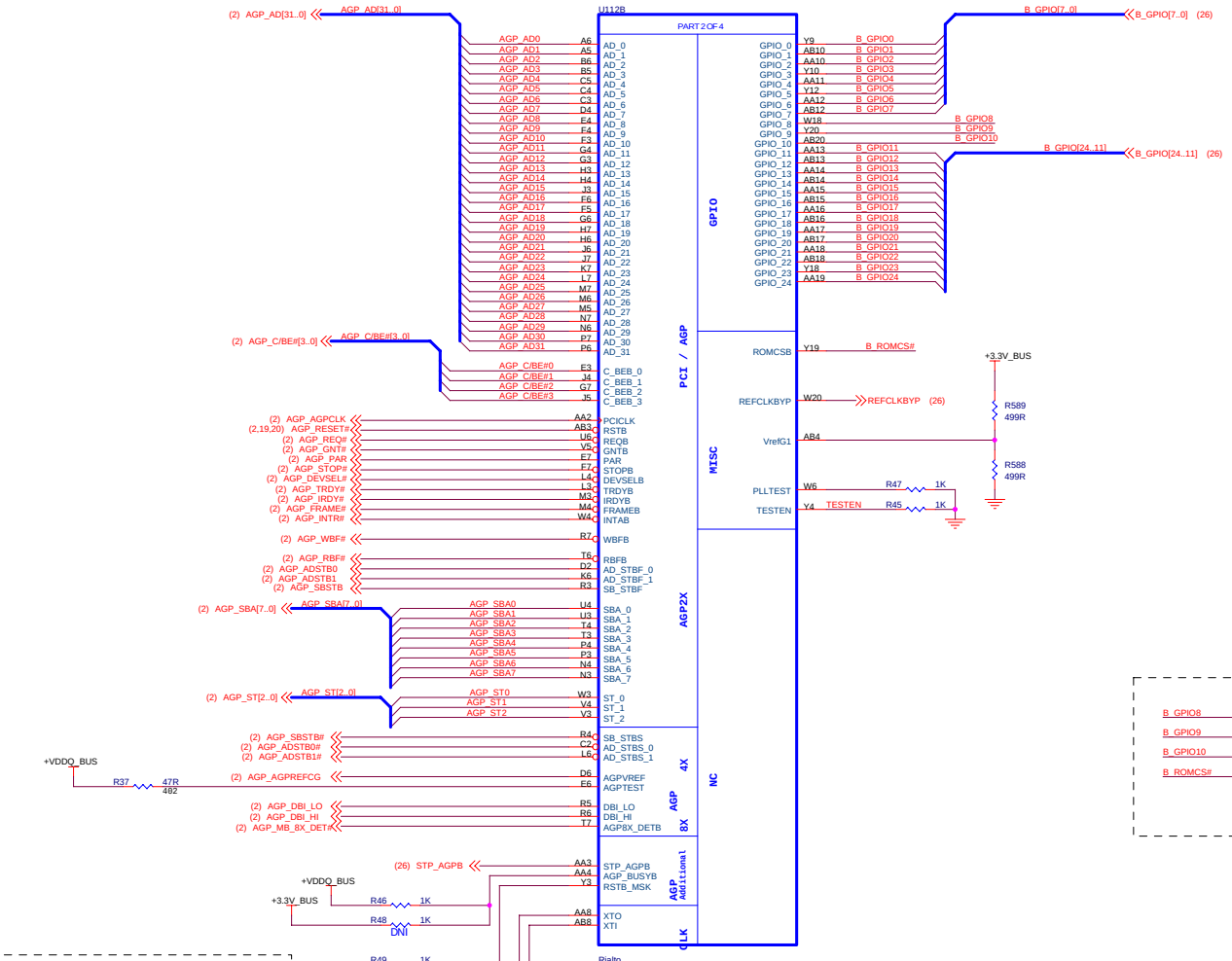

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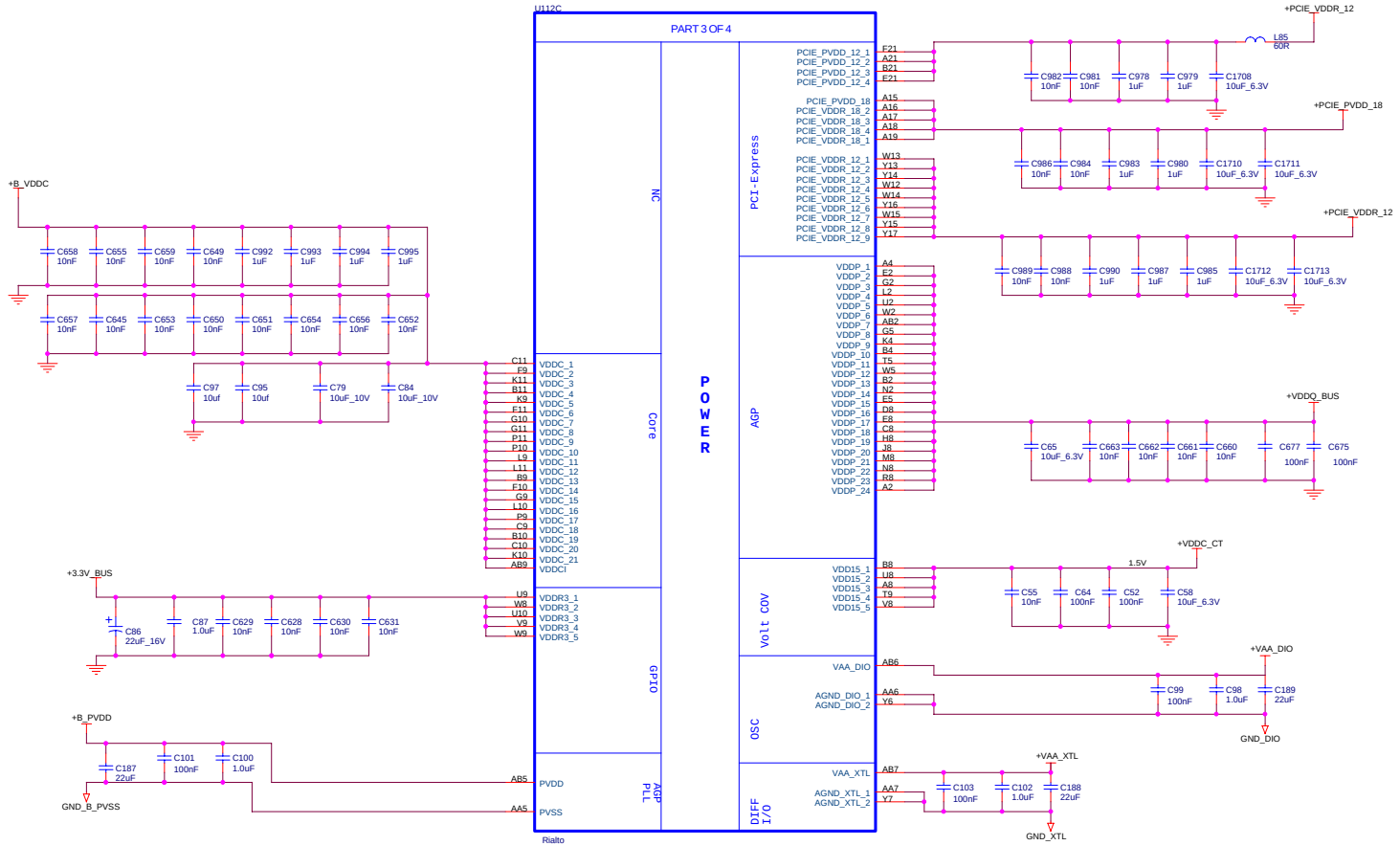
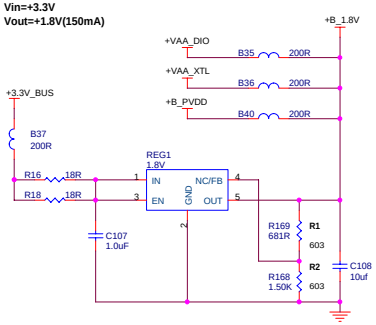


NOTE: Place REG1 close to ASIC.

REGULATOR FOR B_1.8V
Vin=+3.3V
Vout=+1.8V(150mA)



Use SP6201EM5-ADJ, 200mA, SOT23-5, DO<500mV (2480041200) $0.11
Alt. TI TPS76301, ADJ, 150mA, DO<300mV, SOT23 (2480040800)
Alt. TI TPS76318, 1.8V, 150MA, DO<300mV, SOT23 (2480003900)

	SP6201EM5-ADJ Vo=1.25 (1+R1/R2)	TPS76301, ADJ Vo=1.186 (1+R1/R2)
R1	3240681000, 681R, 1%	3240787000, 787R, 1%
R2	3240150100, 1.50K, 1%	3240150100, 1.50K, 1%

GND_B_PVSS GND_DIO GND_XTL

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

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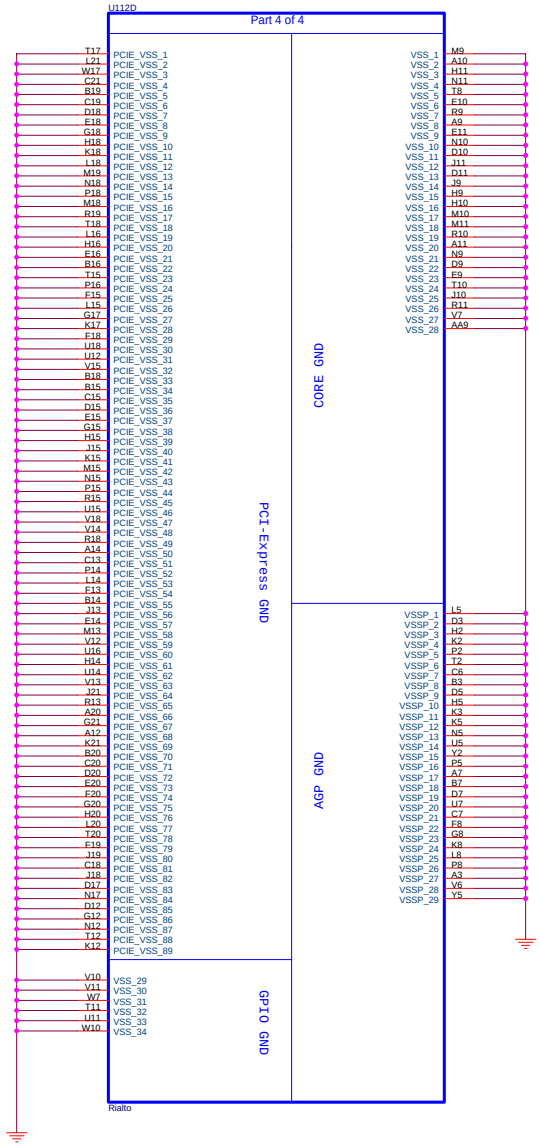

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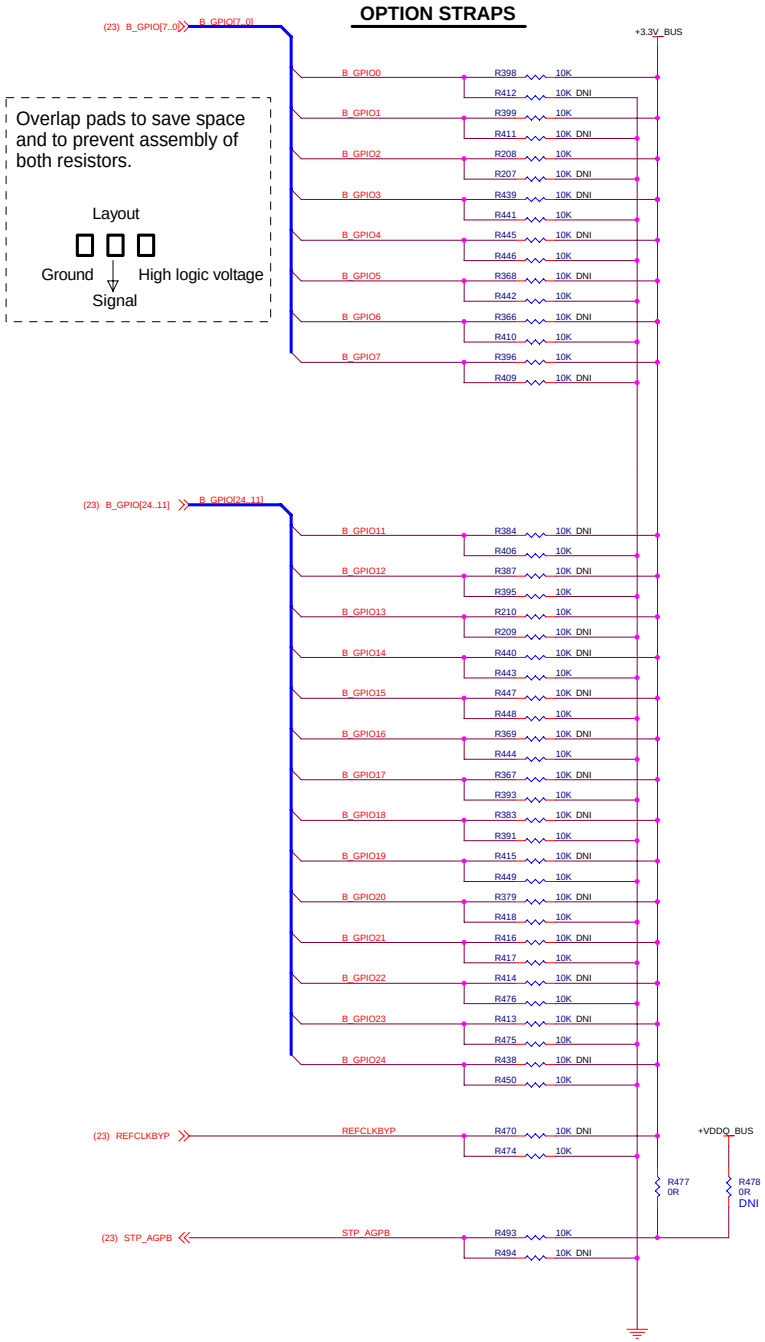

PCIE_AGP_Bridge Shared Straps

STRAPS	PIN	DESCRIPTION	DEFAULT
PCIE_PTX_PWRS_ENB	GPIO(0)	PCI Express transmitter power-saving enable bar 0 - 50% Tx output swing for mobile applications 1 - Full output swing	1
PCIE_PTX_DEEMPH_EN	GPIO(1)	PCI Express transmitter de-emphasis enable 0 - de-emphasis disenable 1 - de-emphasis enable	1
PCIE_ICP (1:0)	GPIO(3:2)	Charge pump current setting 00 - 5.0uA 01 - 10.0uA **10 - 15.0uA** 11 - 20.0uA	01
PCIE_PTX_IEXT	GPIO(4)	PCI Express transmitter extra ouptput current 0 - no extra current 1 - extra current in output stage	0
PCIE_PRX_IDLE_MODE	GPIO(5)	Controls sensitivity of the electrical idle detectors 0 - normal idle detect 1 - improve idle detect	0
PCIE_PPLL_BW	GPIO(6)	PCI Express PLL bandwidth setting 0 - Full PLL bandwidth 1 - Reduces PLL bandwidth	0
PCIE_REVERSE_ALL	GPIO(7)	0 - Don't reverse physical PCIE lanes 1 - Reverse physical PCIE lanes	1
PCI_RETRY_ENb	GPIO(8)	0 - Enable all PCI read/write retry, retry cycle 0x3 1 - Disable PCI read/write retry	0
	GPIO(9)		0
DEBUG_ACCESS	GPIO(10)	1 - Set the debug bus muxes to bring out debug signals even if registers are inaccessable	0
ROMIDCFG(2:0)	GPIO(13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 000 - No ROM, CHG_ID=0 001 - 512Kb Serial AT25F512 ROM (Atmel) 010 - Reserved 011 - 1M Serial M25P10A ROM (ST) **100 - 512K Serial M25P05A ROM (ST)** 101 - 1M Serial SST45LF010 ROM (SST) 1M Serial W45B012 ROM (WinBond) 512K Serial W45B512 ROM (WindBond) 110 - 1M Serial SST25VF010 ROM (SST) 512K Serial SST25VF512 ROM (SST) 111 - Reserved	100
VGA_MONO_MODE(1:0)	GPIO(24, 14)	00 - only VGA controller 01 - only MONO controller 10 - neither VGA/MONO controller 11 - both VGA/MONO controller	00
MEM_AP_SIZE	GPIO(15)	Used only there is no valid ROM 0 - 128Mb(2x64Mb) 1 - 256Mb(2x128Mb)	0
MULTIFUNC	GPIO(16)	For MULTIFUNC, when TESTEN(pin)=0, 0 = 00 - Single function device 1 = 01 - Two function device. No AGP in either function	0
PCIE_FORCE_COMPLIANCE		For PCIE_FORCE_COMPLIANCE, when TESTEN(pin)=1, 0 - Normal operation 1 - Force LC into compliance mode	0
AGPFBSKEW(1:0)	GPIO(18:17)	AGP 1xclock feedback phase adjustment wrt refclk(cpuclk) 00 - refclk slightly earlier than feedback 01 - refclk 1 tap later than feedback 10 - refclk 1 tap earlier than feedback 11 - refclk 2 tap earlier than feedback clock	00 internal pulldown
X1CLK_SKEW(1:0)	GPIO(20:19)	Clock phase adjustment between x1clk and x2clk 00 - 0 tap delay 01 - 1 tap delay 10 - 2 tap delay 11 - 3 tap delay	00 internal pulldown
BUSCFG	GPIO(21)	Control BUS type, CLK PLL select	0 internal pulldown
AGP_ONLY	GPIO(22)	0 - normal operation, assume VPU is working 1 - for debugging, shut off VPU so the bridge is working in AGP only mode	0
PCIE_LINK_TIMEOUT_OVERRIDE	GPIO(23)	0 - Timeout is active 1 - Timeout is disabled	0
MOBILE_EN	REFCLKBYP		0
BUS_PCI_CFG_RETRY_Enb	STP_AGPB	when internal MOBILE_EN=0 STRAP_BUS_PCI_CFG_RETRY_Enb	1

<Variant Name>

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

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DVI SCREWS

ASSY1
SCREW
JACKSCREW
ASSY

ASSY3
SCREW
JACKSCREW
ASSY

ASSY5
SCREW
PAN_HEAD

DVI SCREWS

ASSY2
SCREW
JACKSCREW
ASSY

ASSY4
SCREW
JACKSCREW
ASSY

MISC. BOARD PARTS

ASSY7
BLANK
LABEL
1.50W_X_0.50H
ASSY

ASSY8
ANTISTATIC
BAG
6_X_11
ASSY

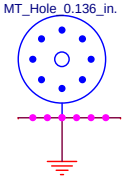
REF2
PCB
109-A31900-00C

REF3
ATI LOGO
LABEL
ATI_LOGO_LABEL

ASSY6
BRACKET
VGA, VID OUT, DVI

ASSY10
BRACKET
DUAL
DUAL, VGA, DIN, DVI

MT1
MT_Hole_0.136_in.



ASSY11
BRACKET
80200365A0

<Variant Name>

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