P892-A04: GT200/NVI 02

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Γ	SKU	VARI ANT	NVPN	ASSEMBLY
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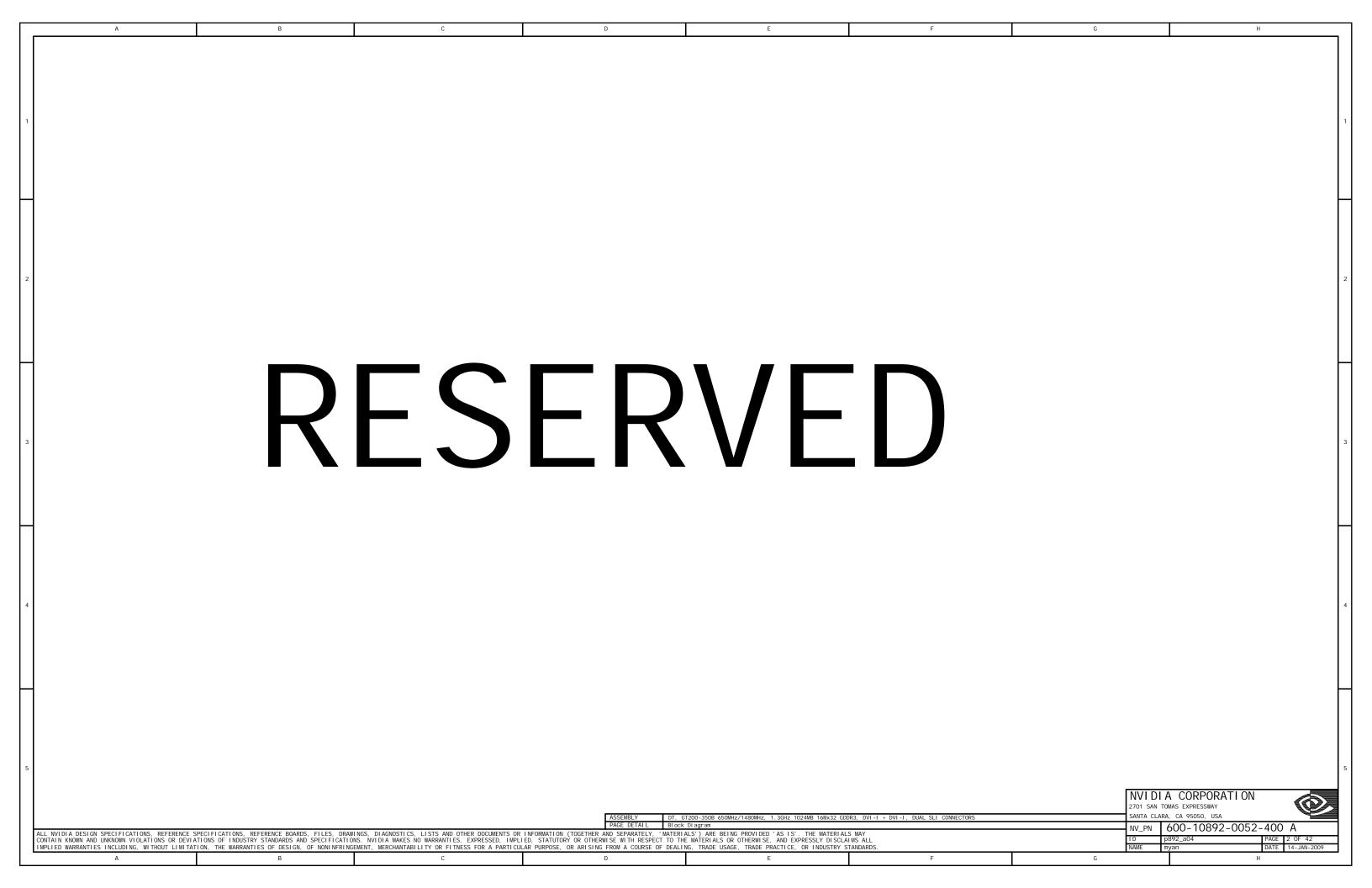
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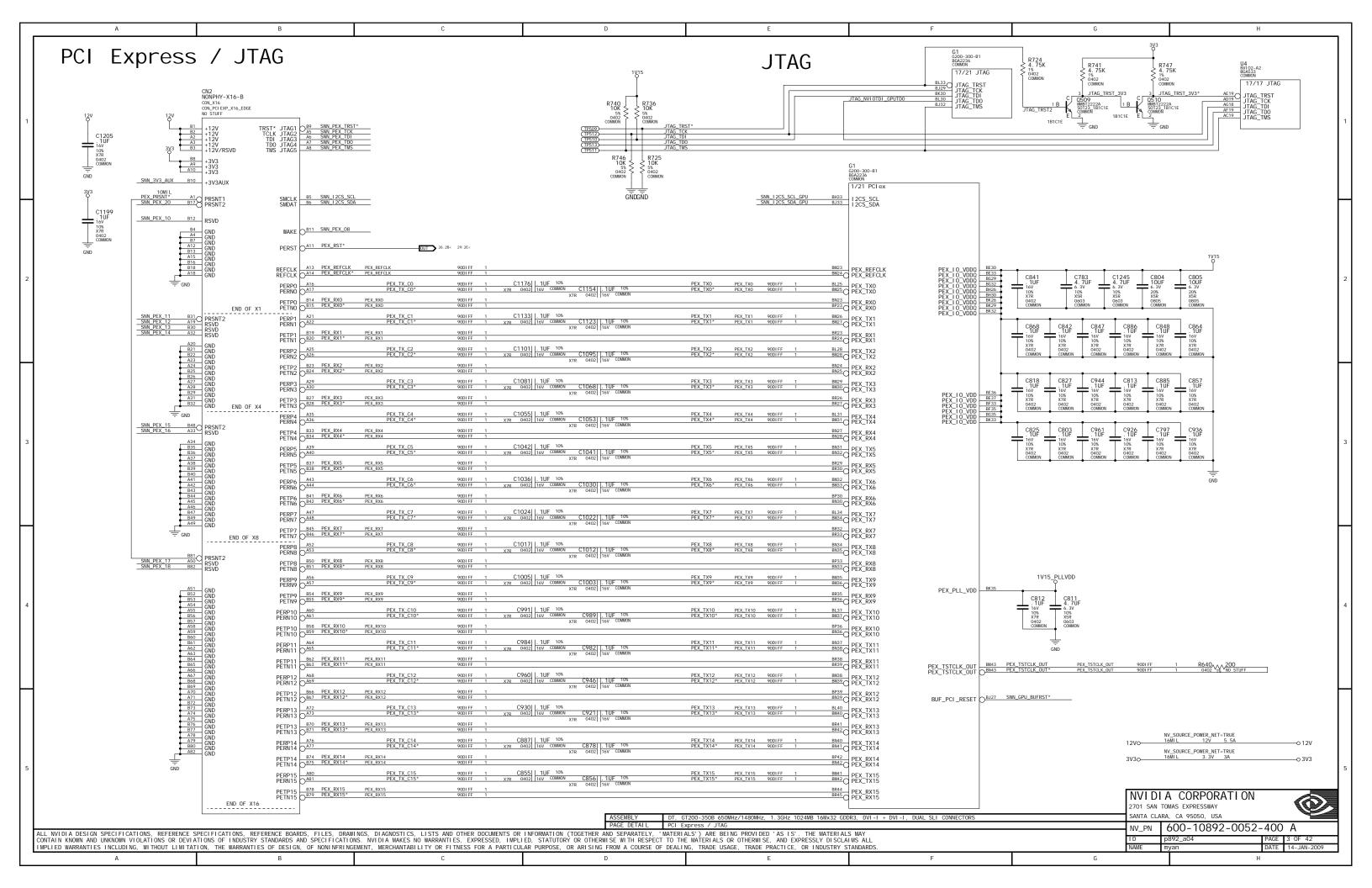
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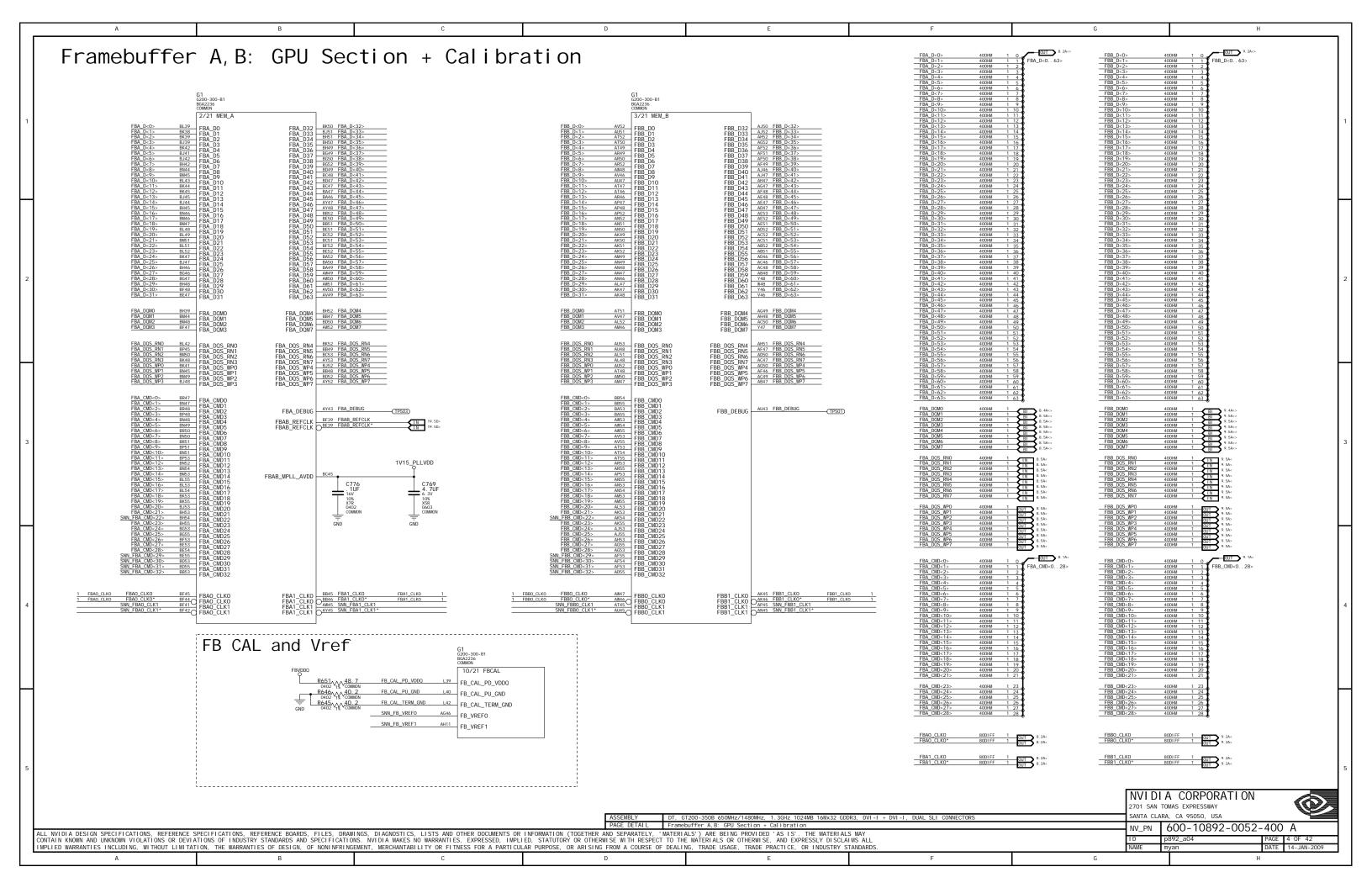
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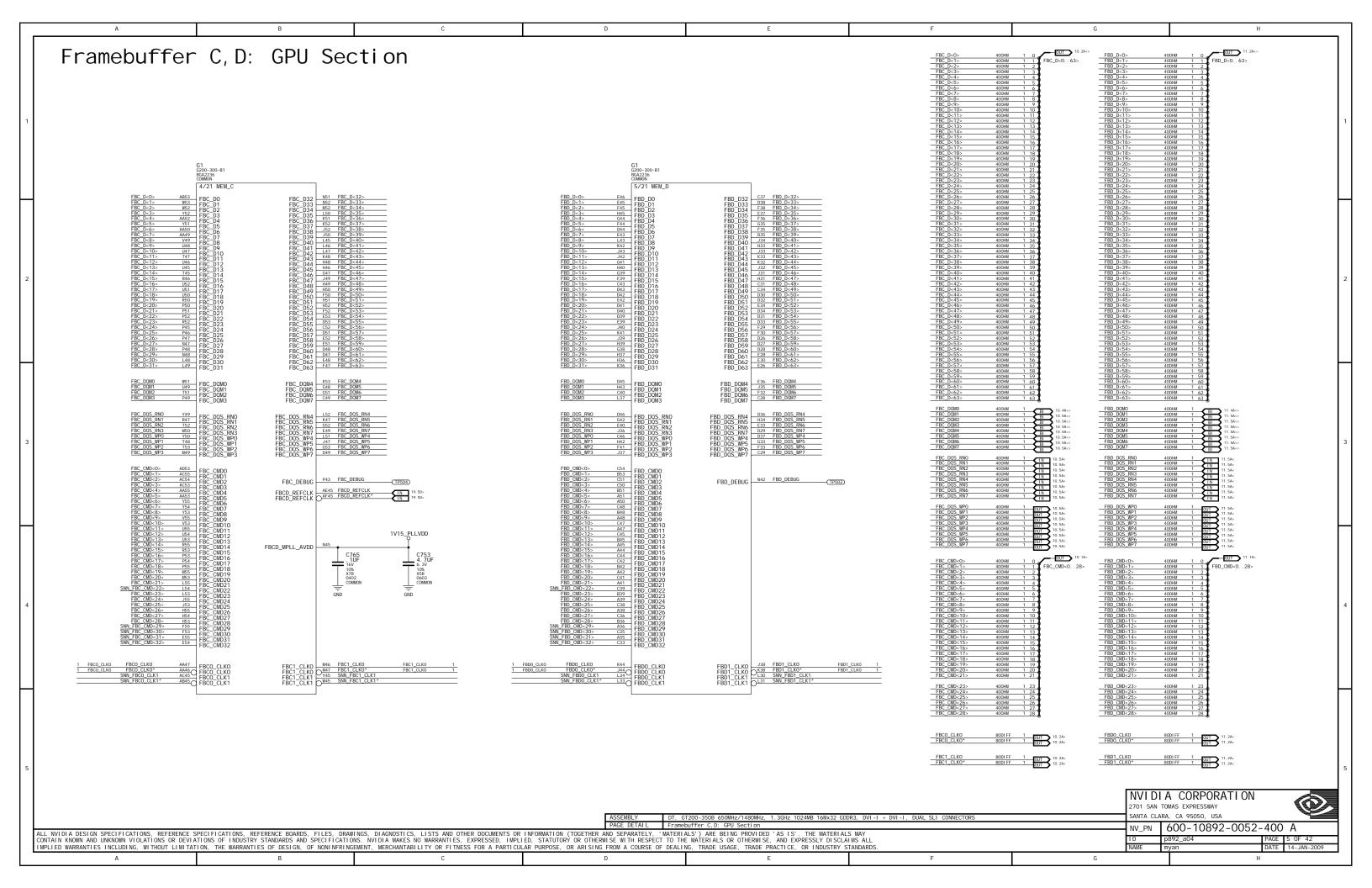
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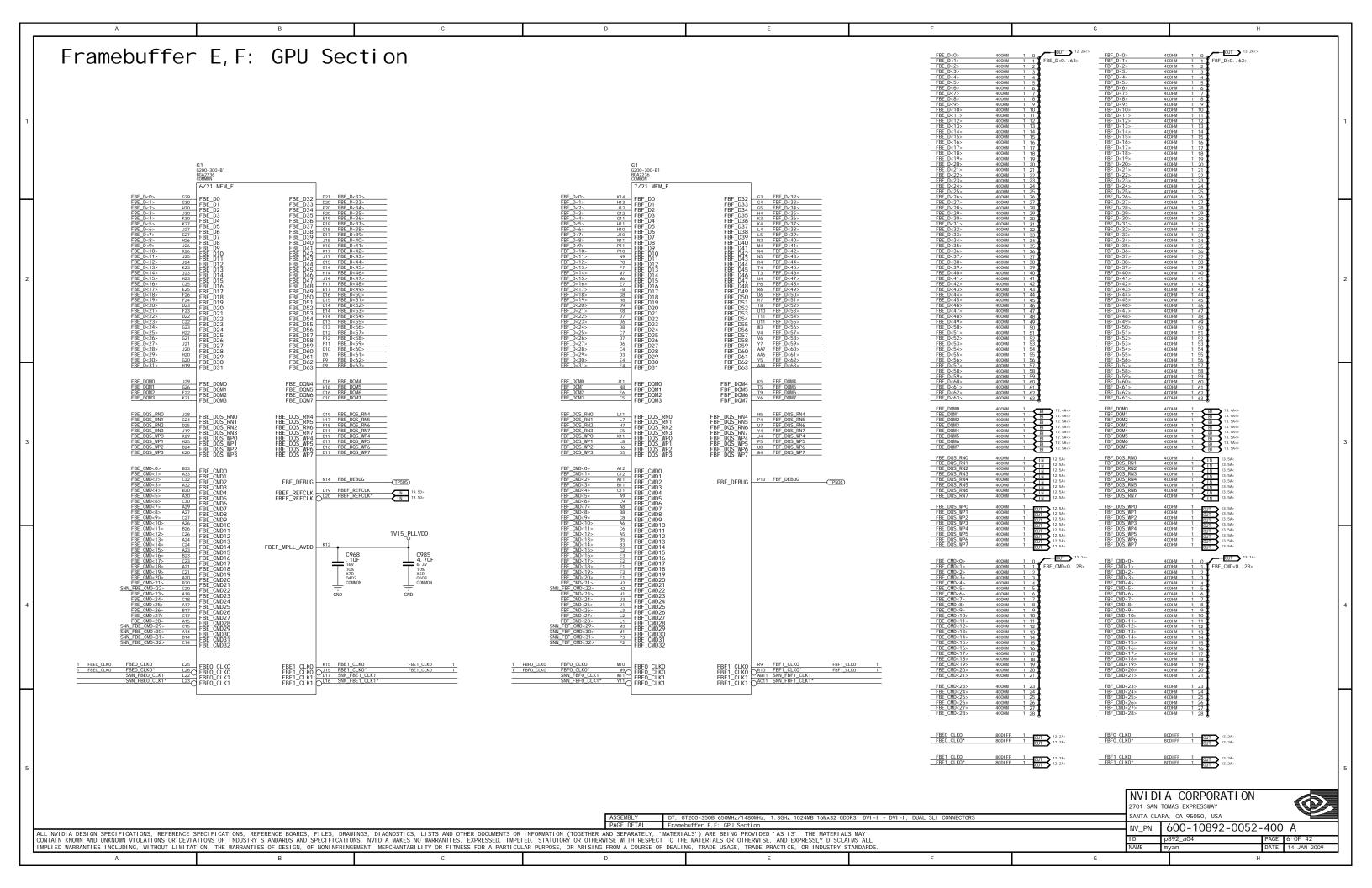
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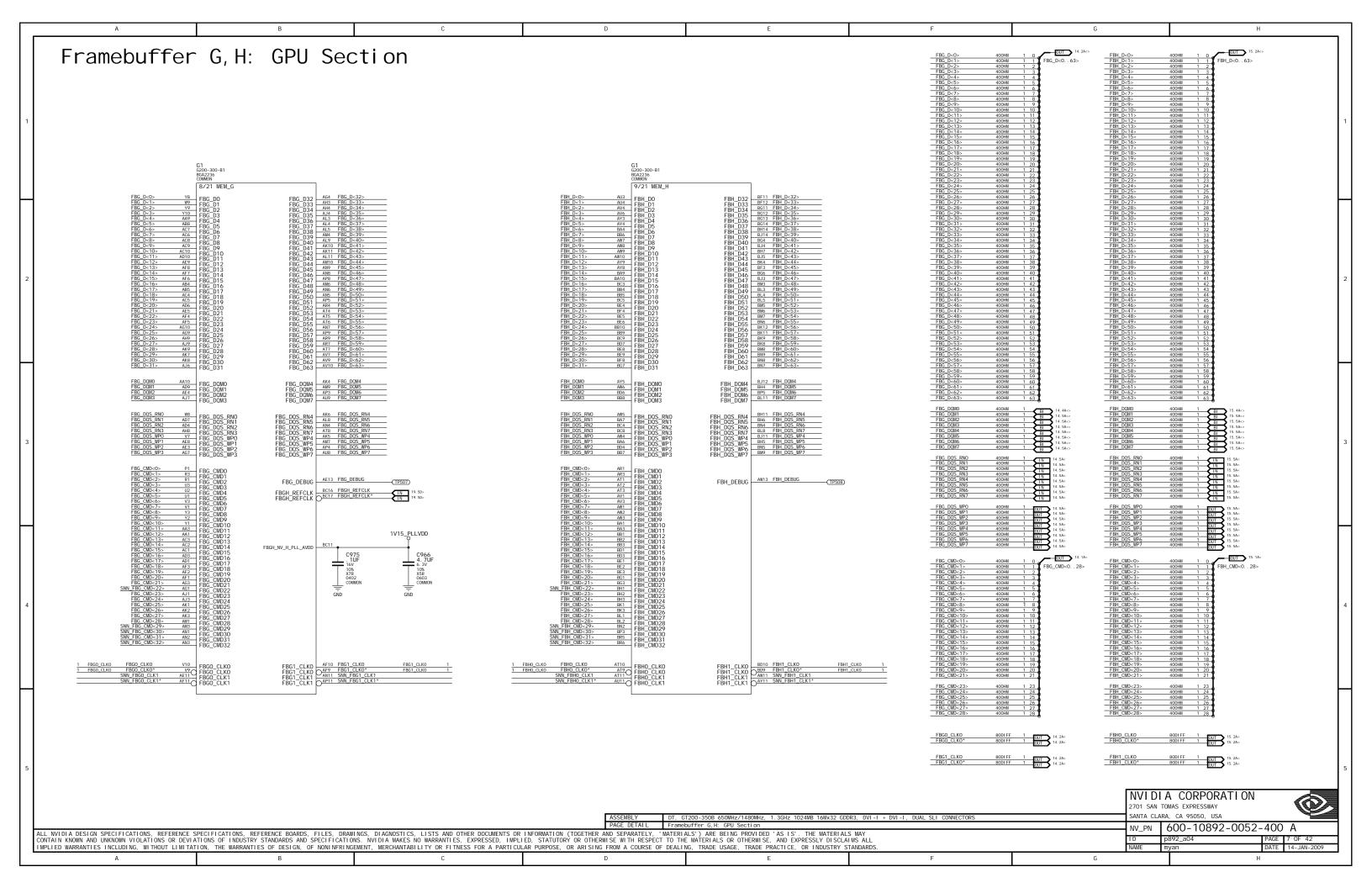


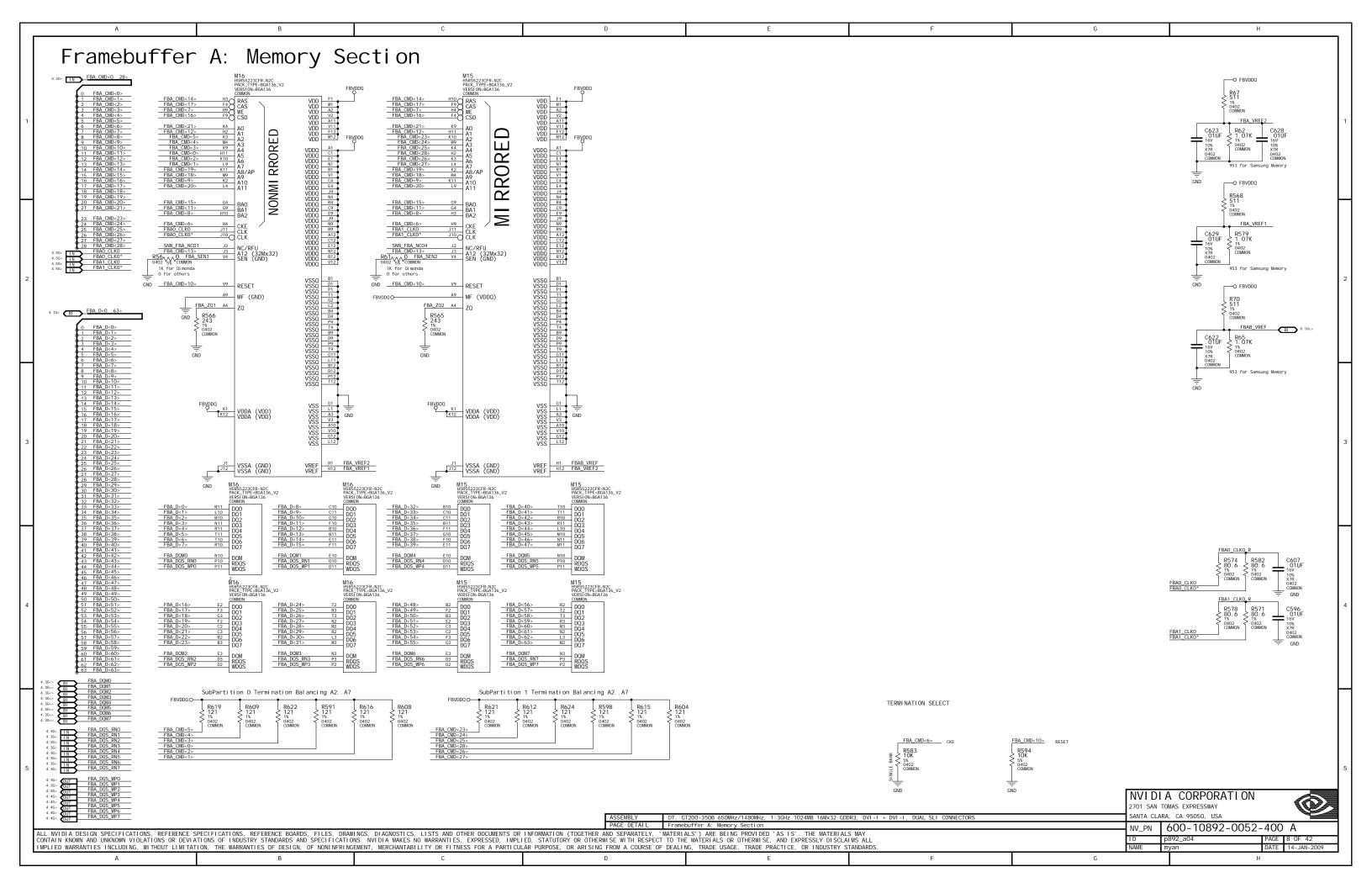


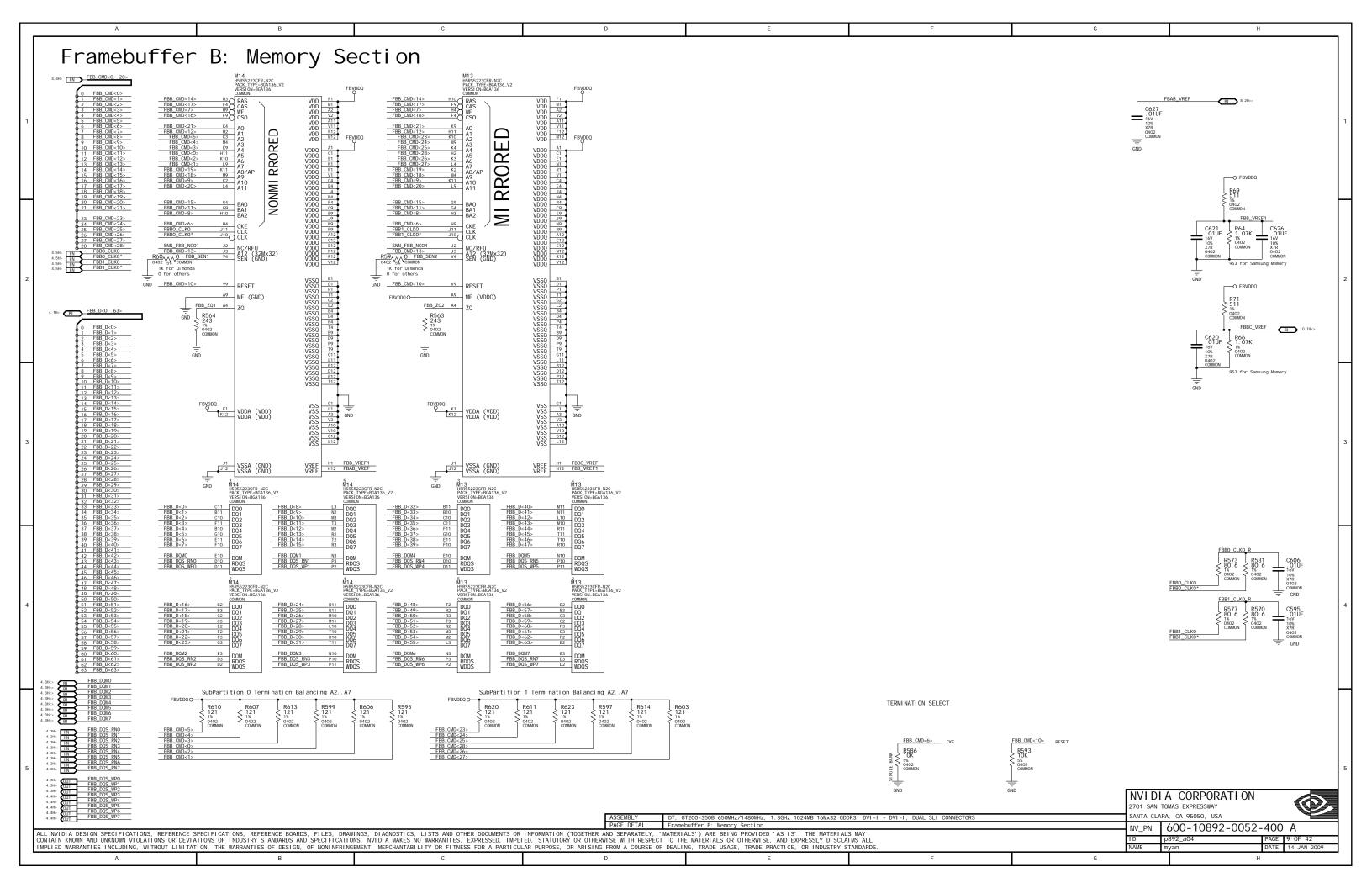


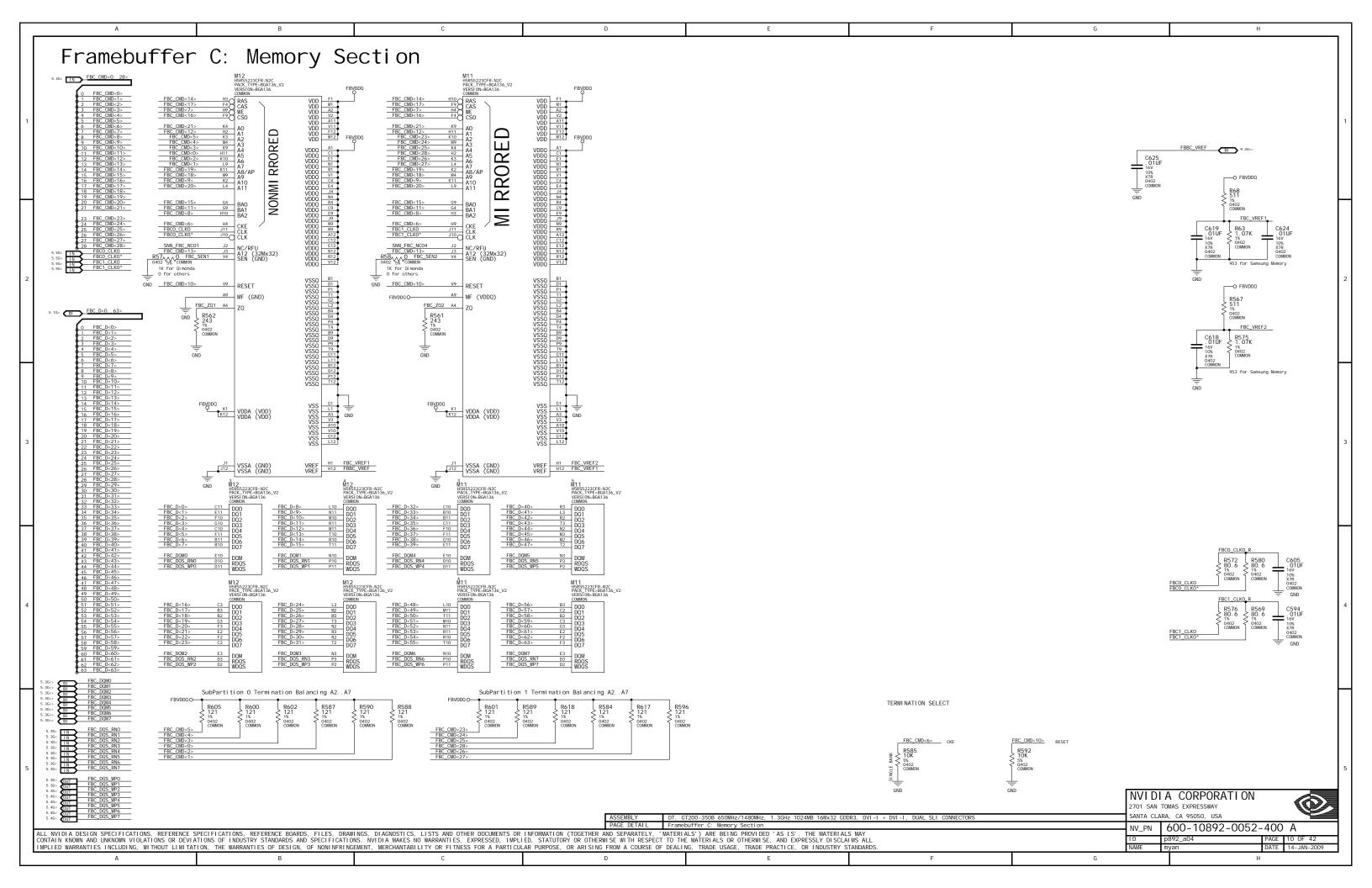


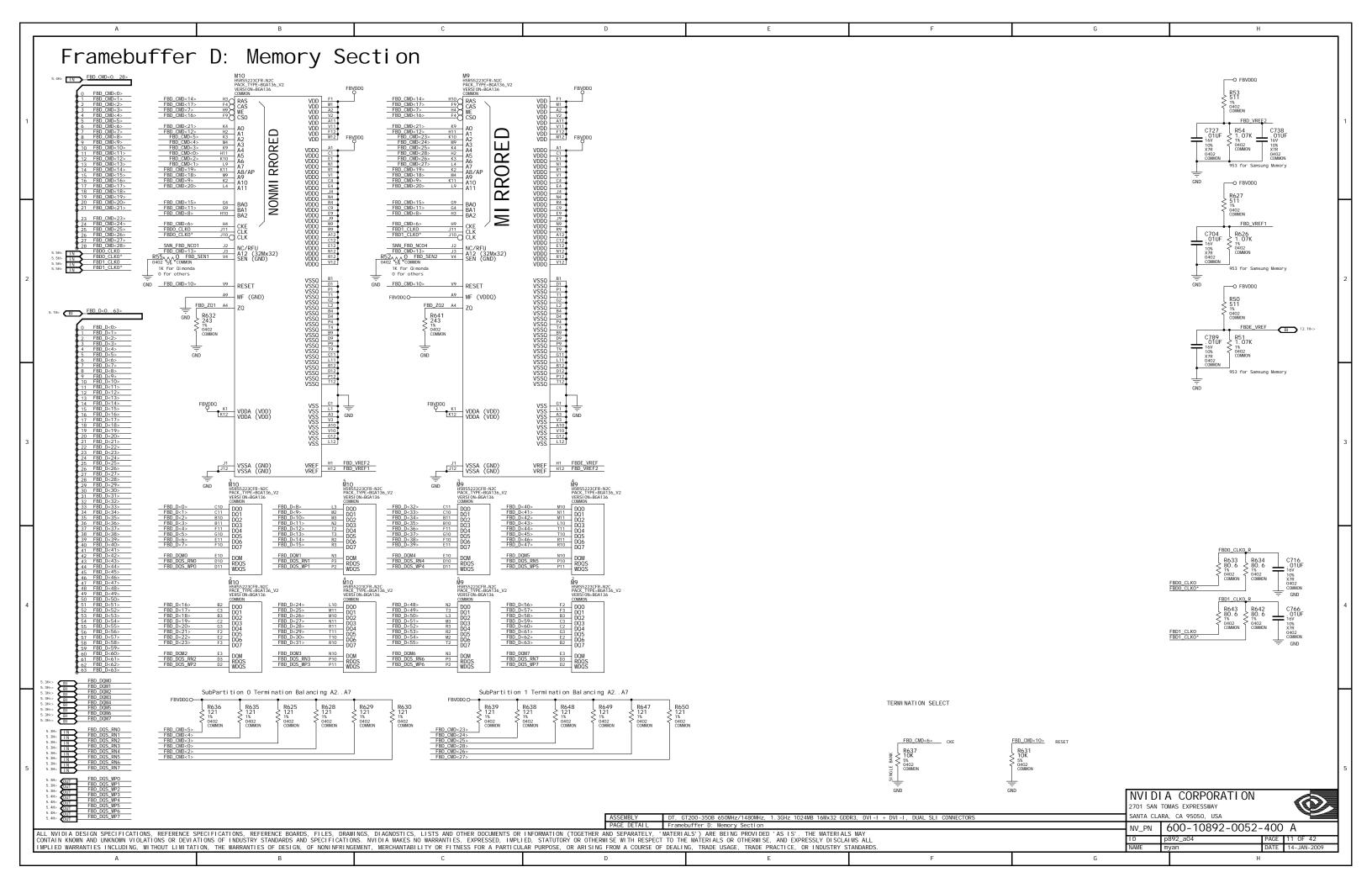


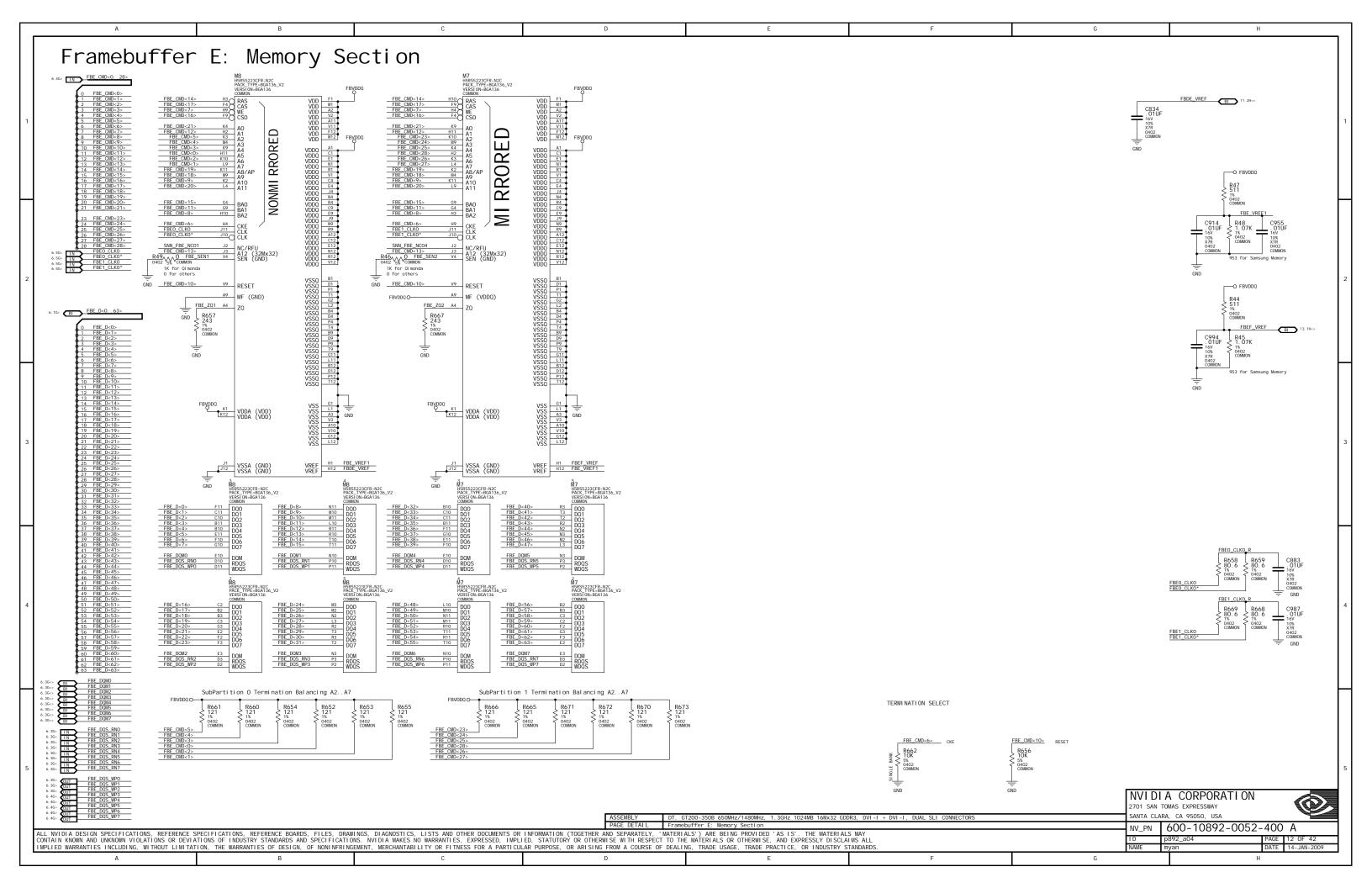


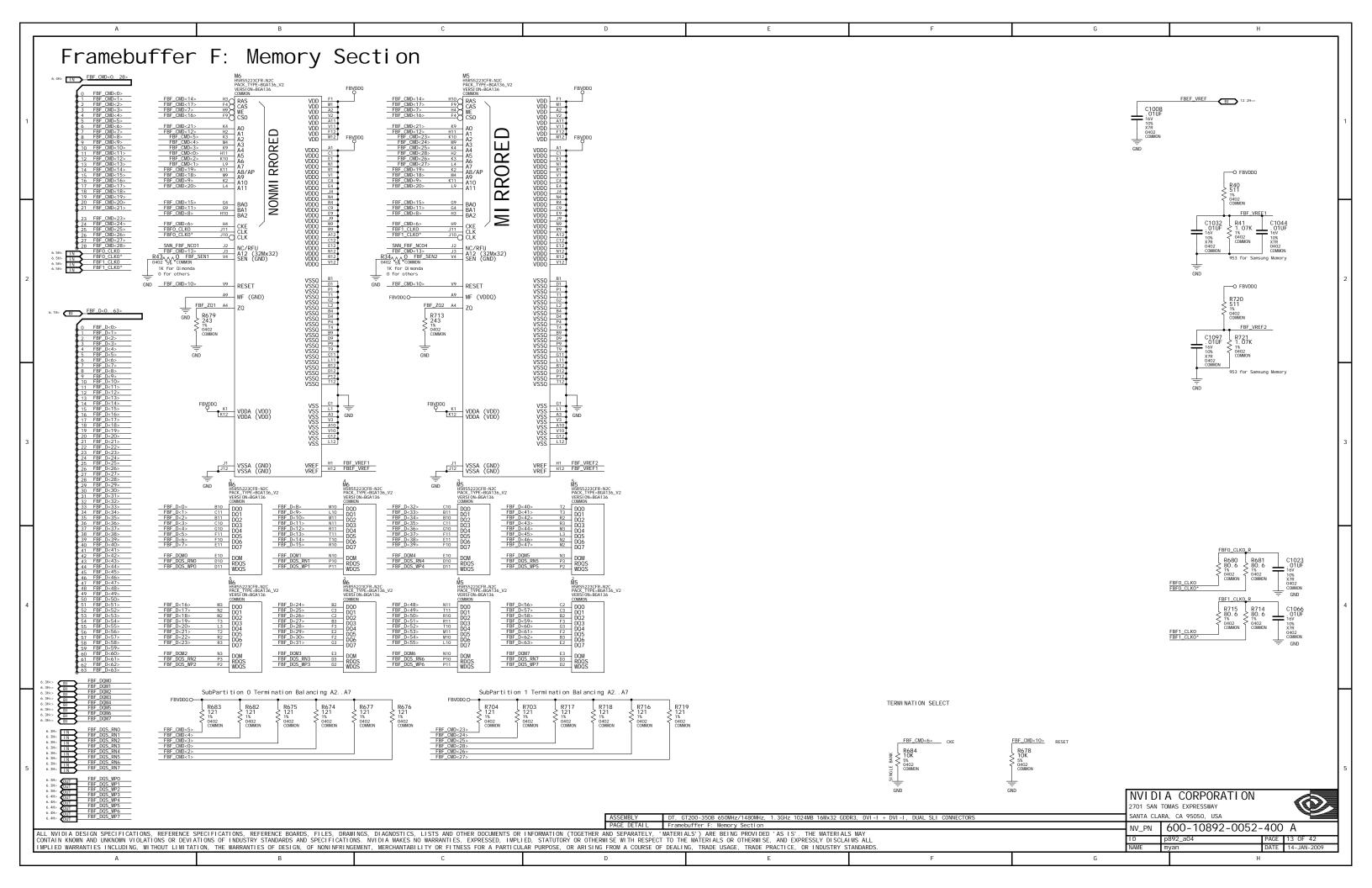


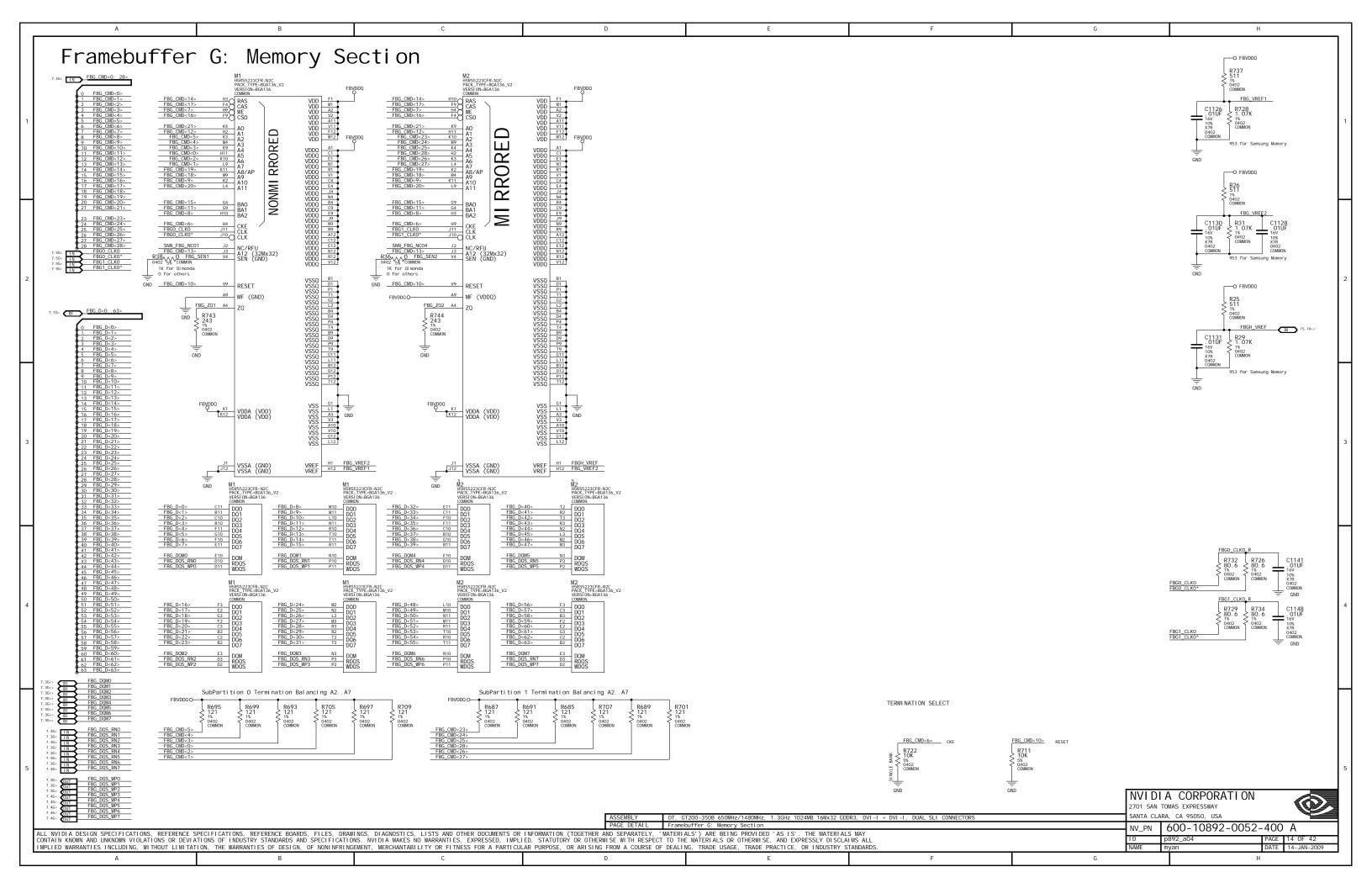


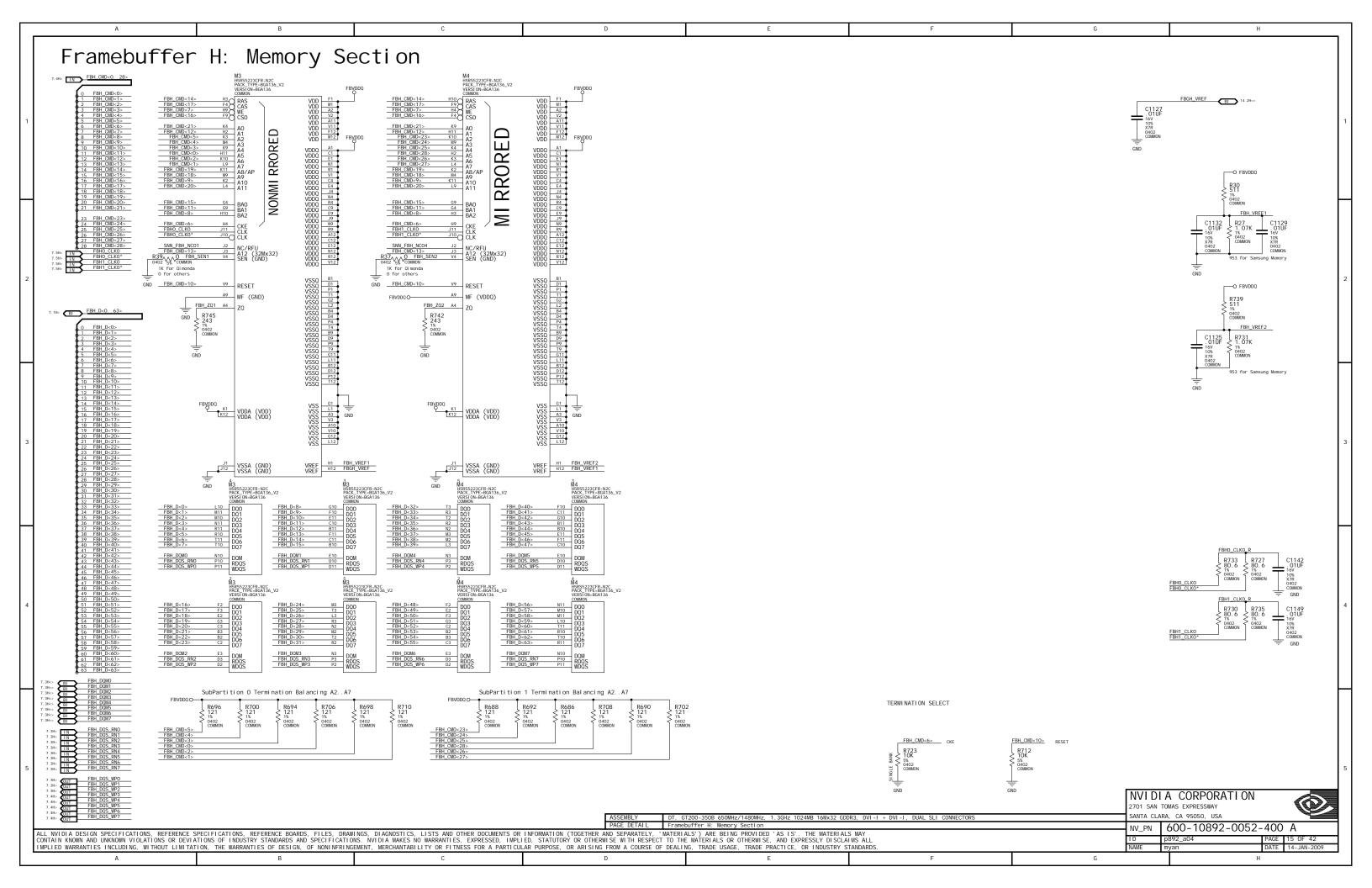


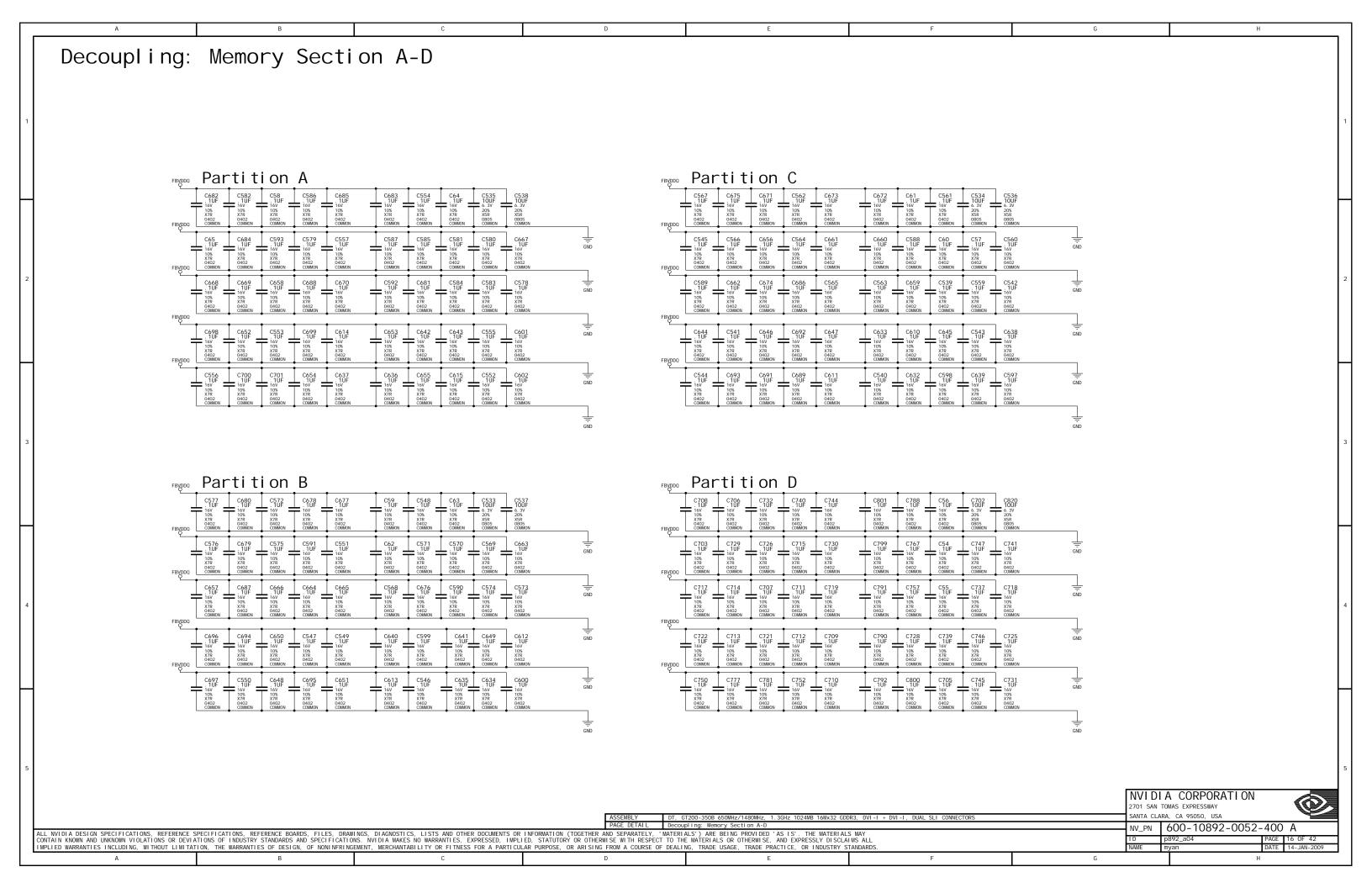


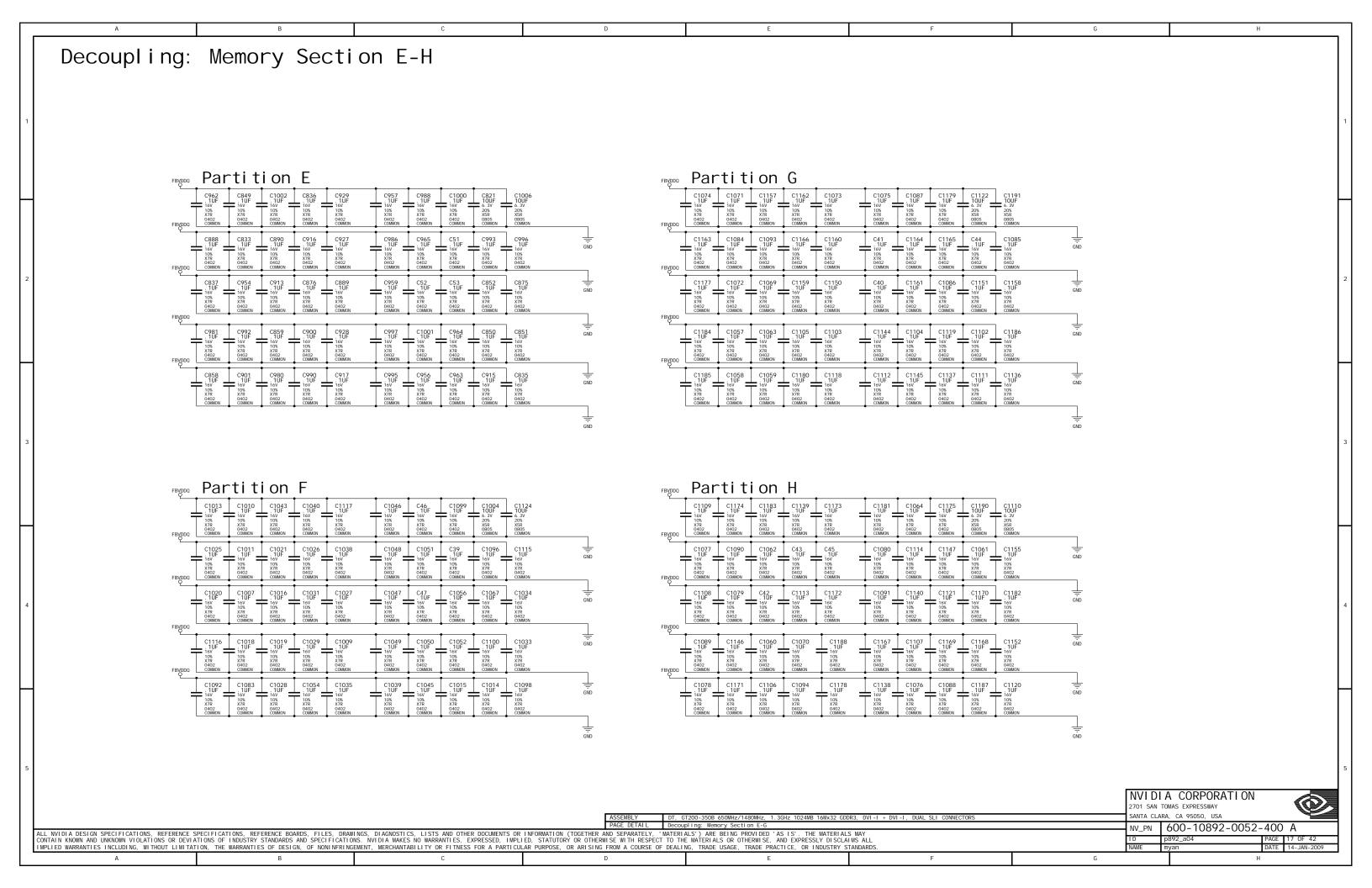


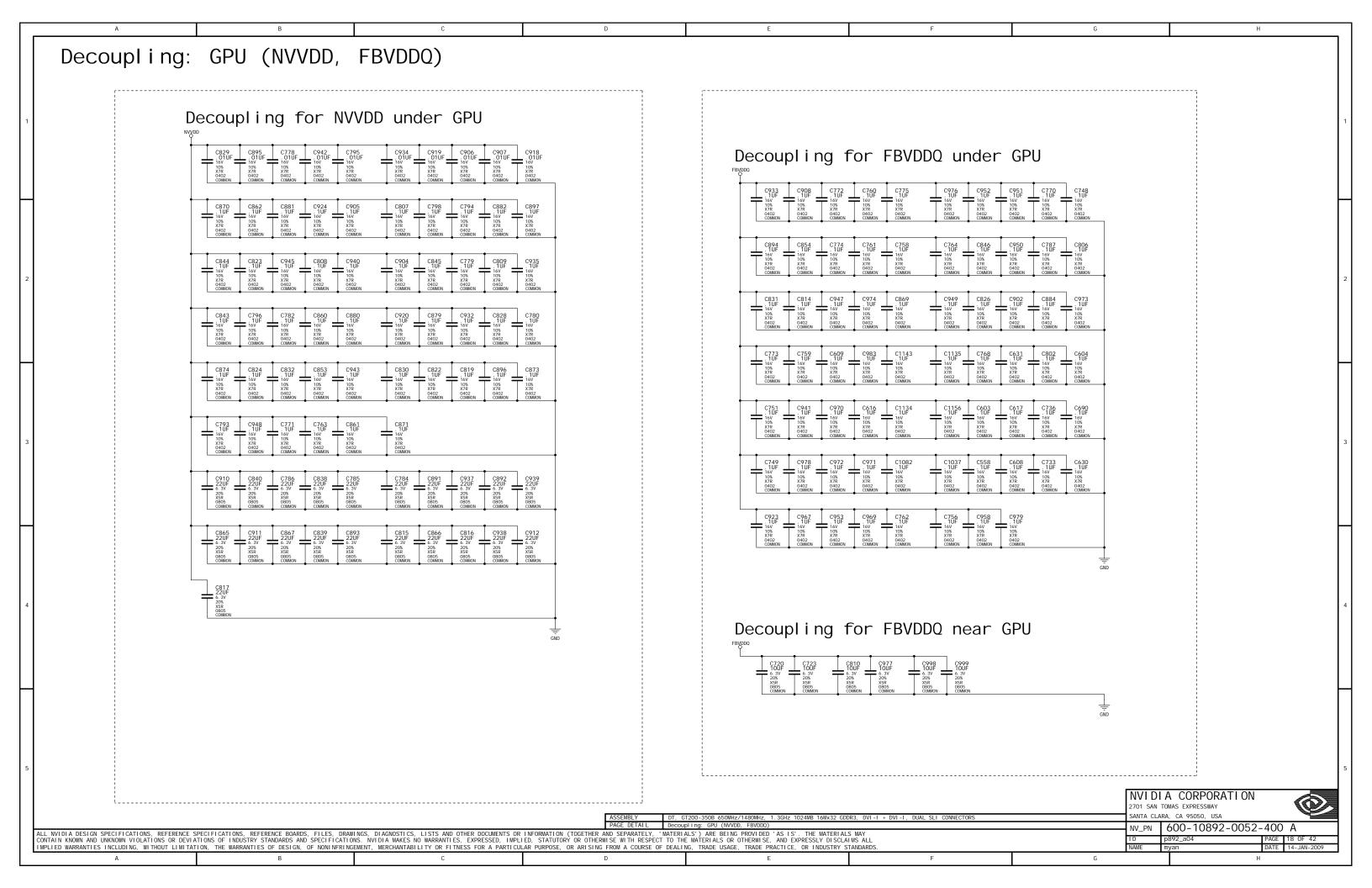


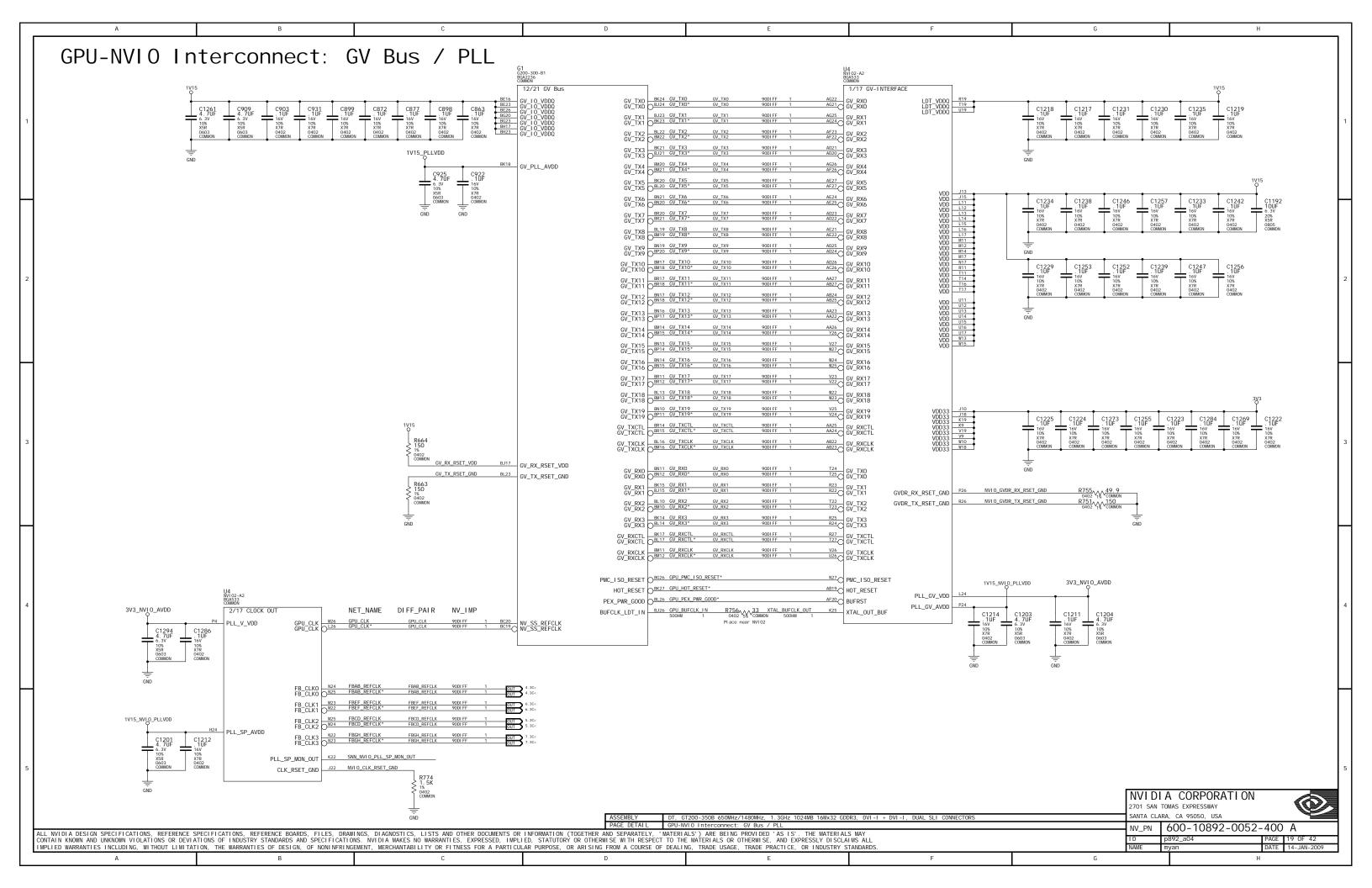


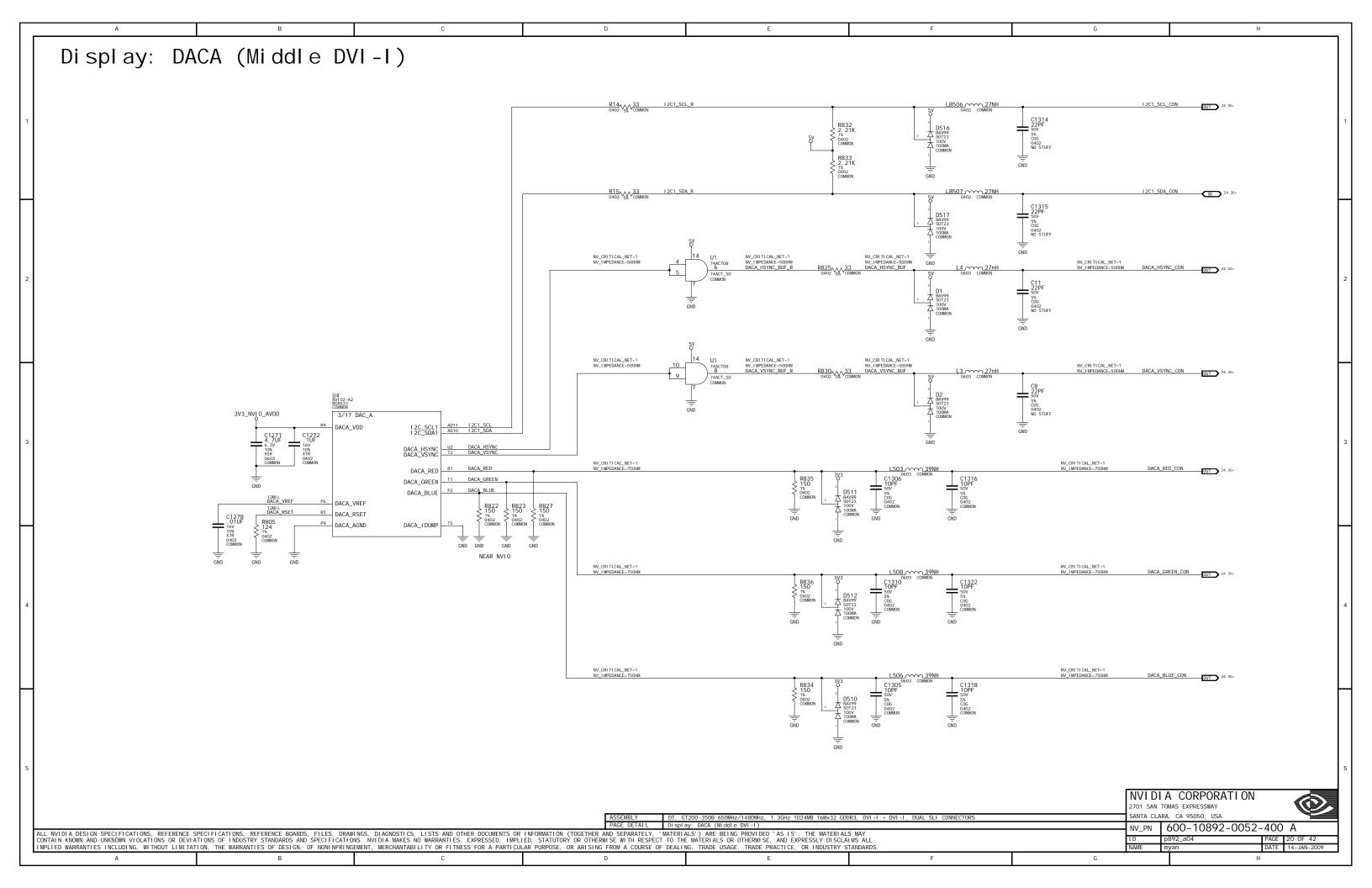


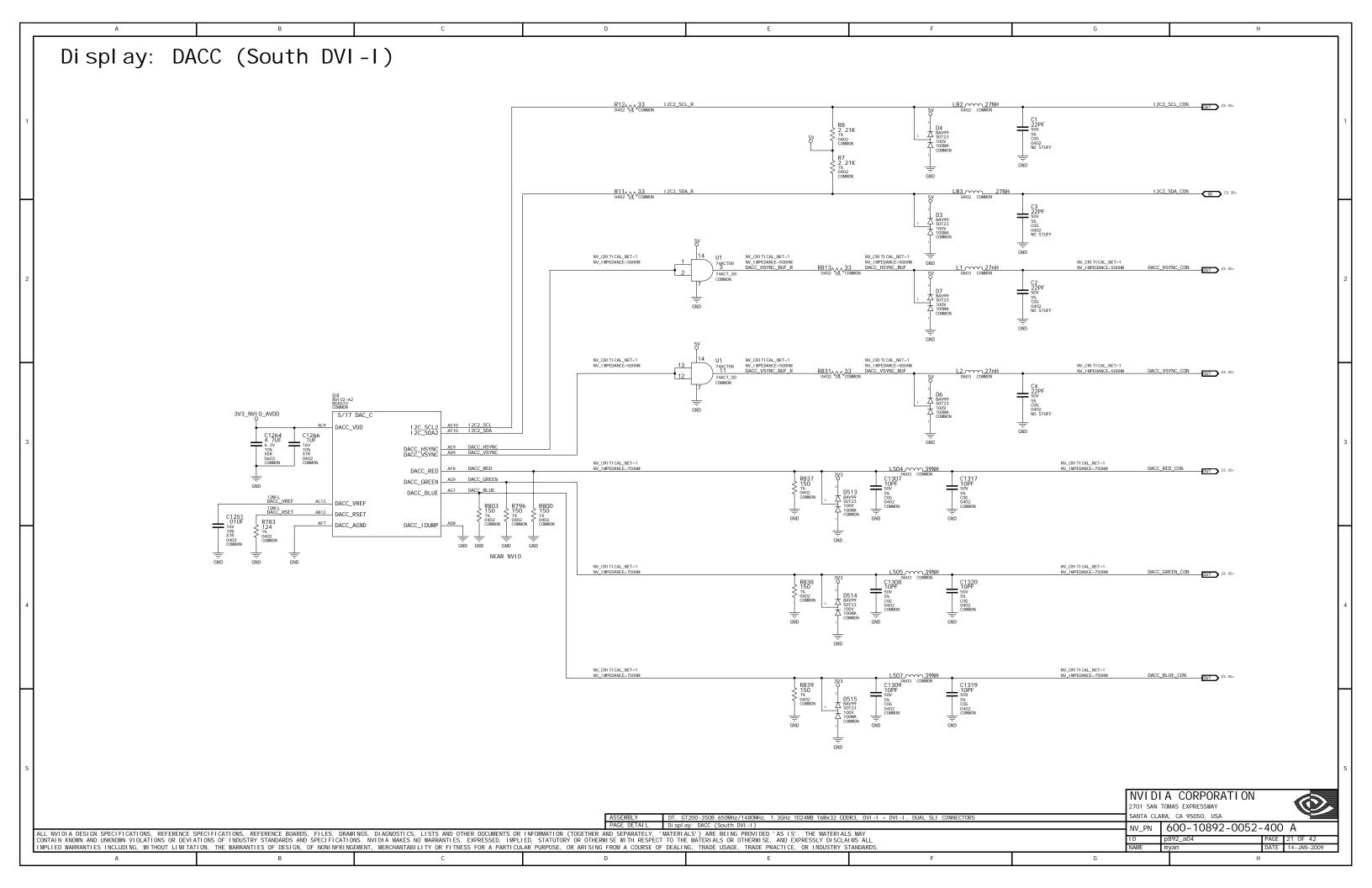


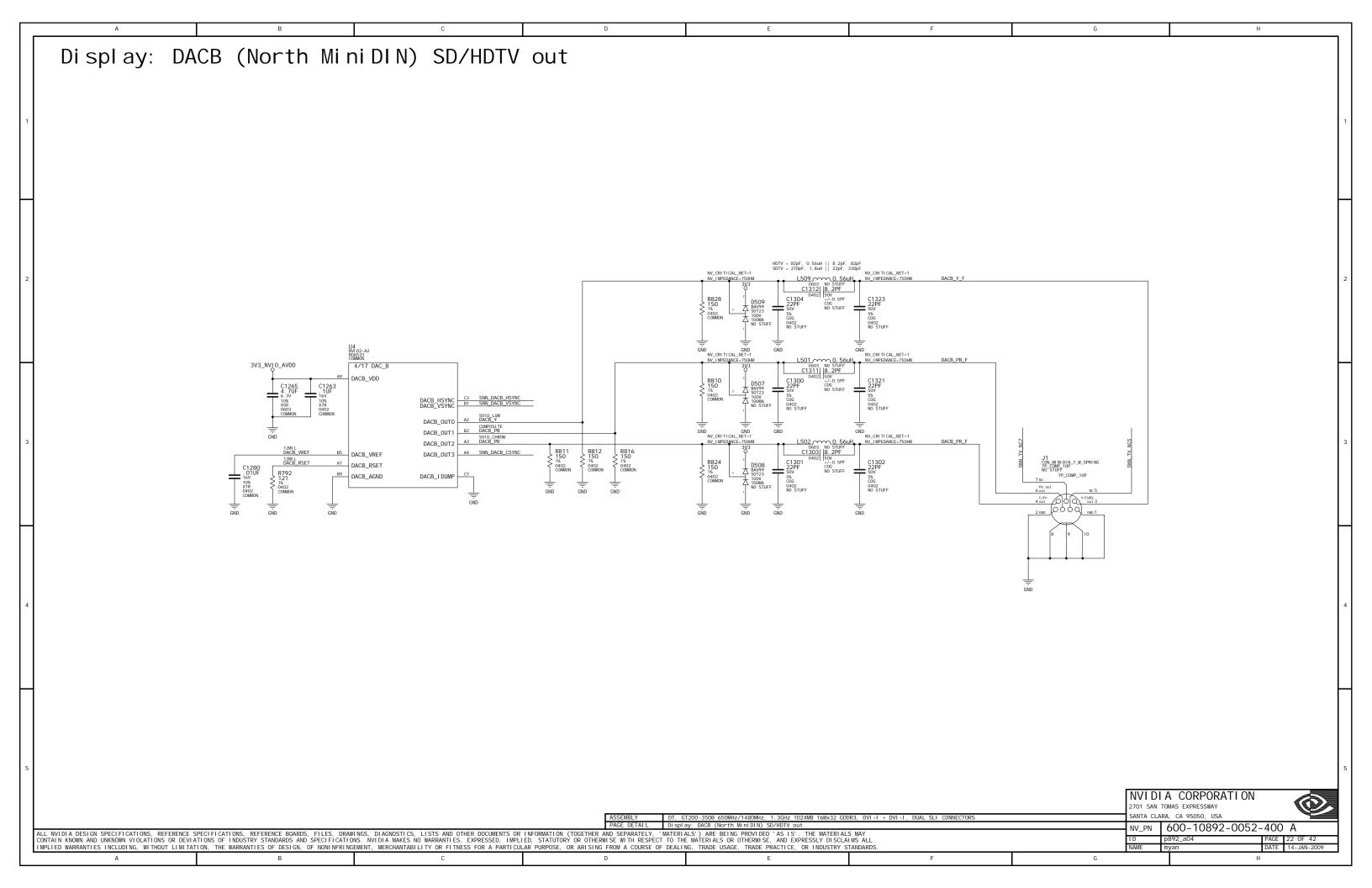


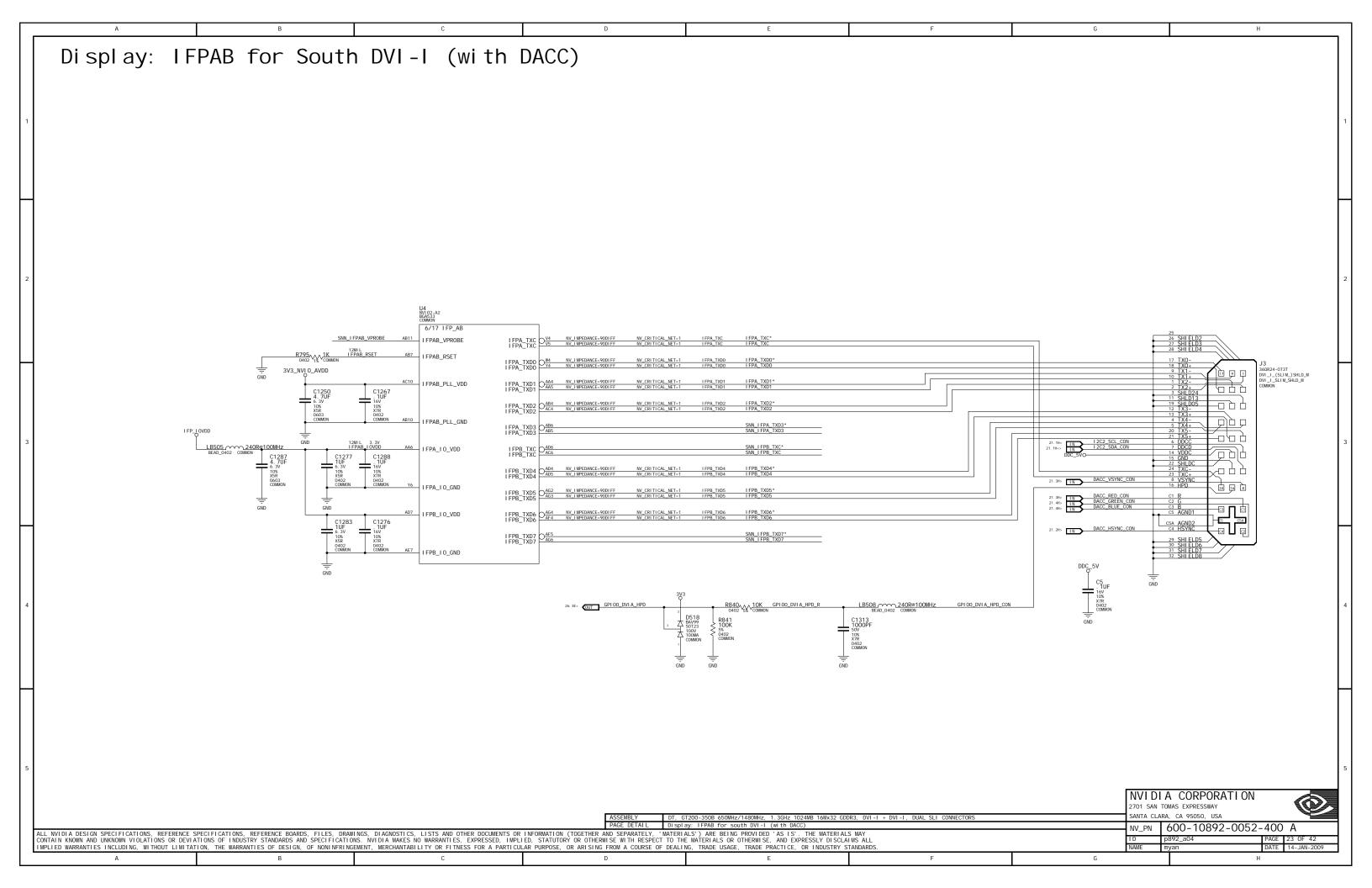


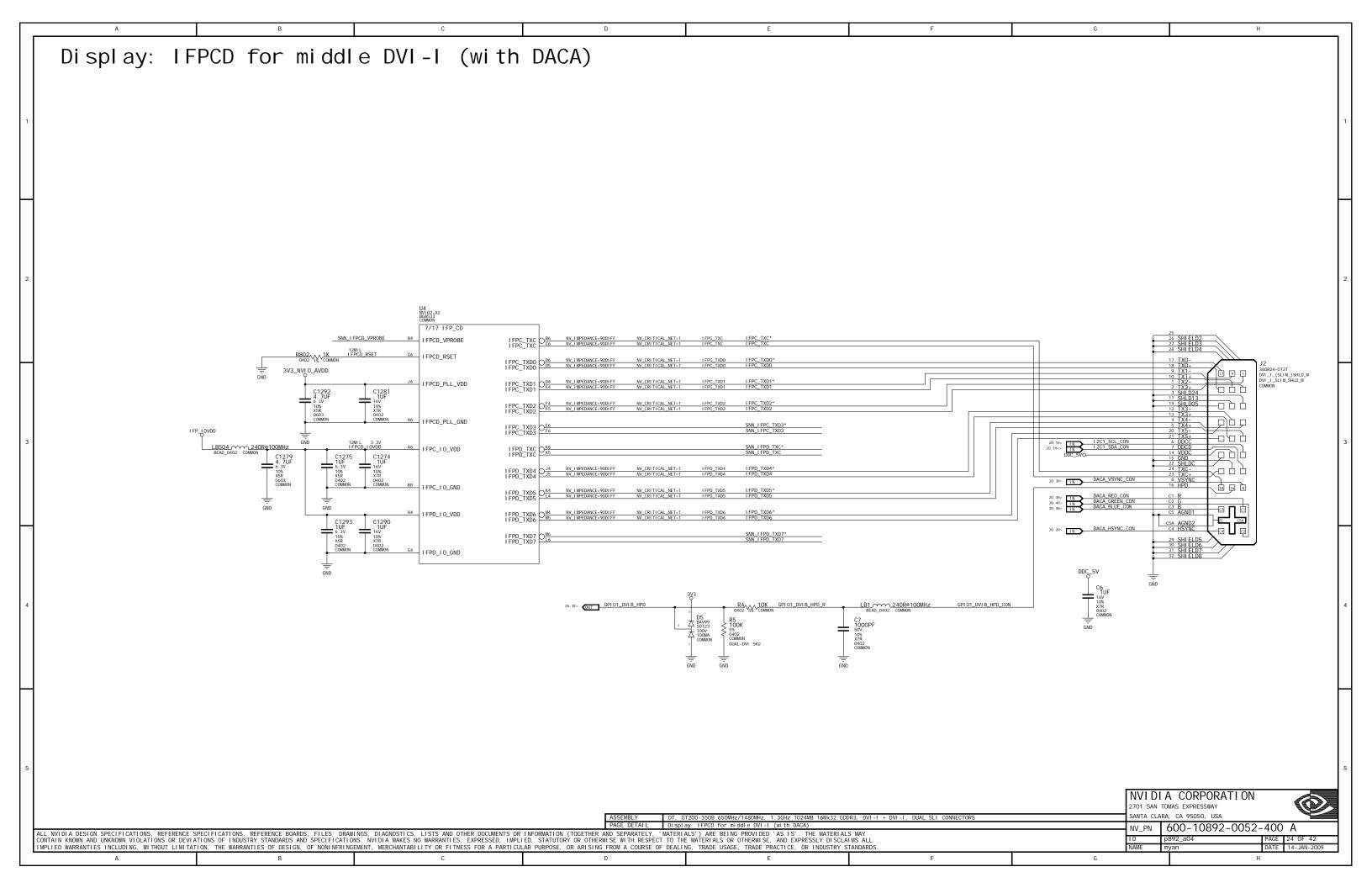


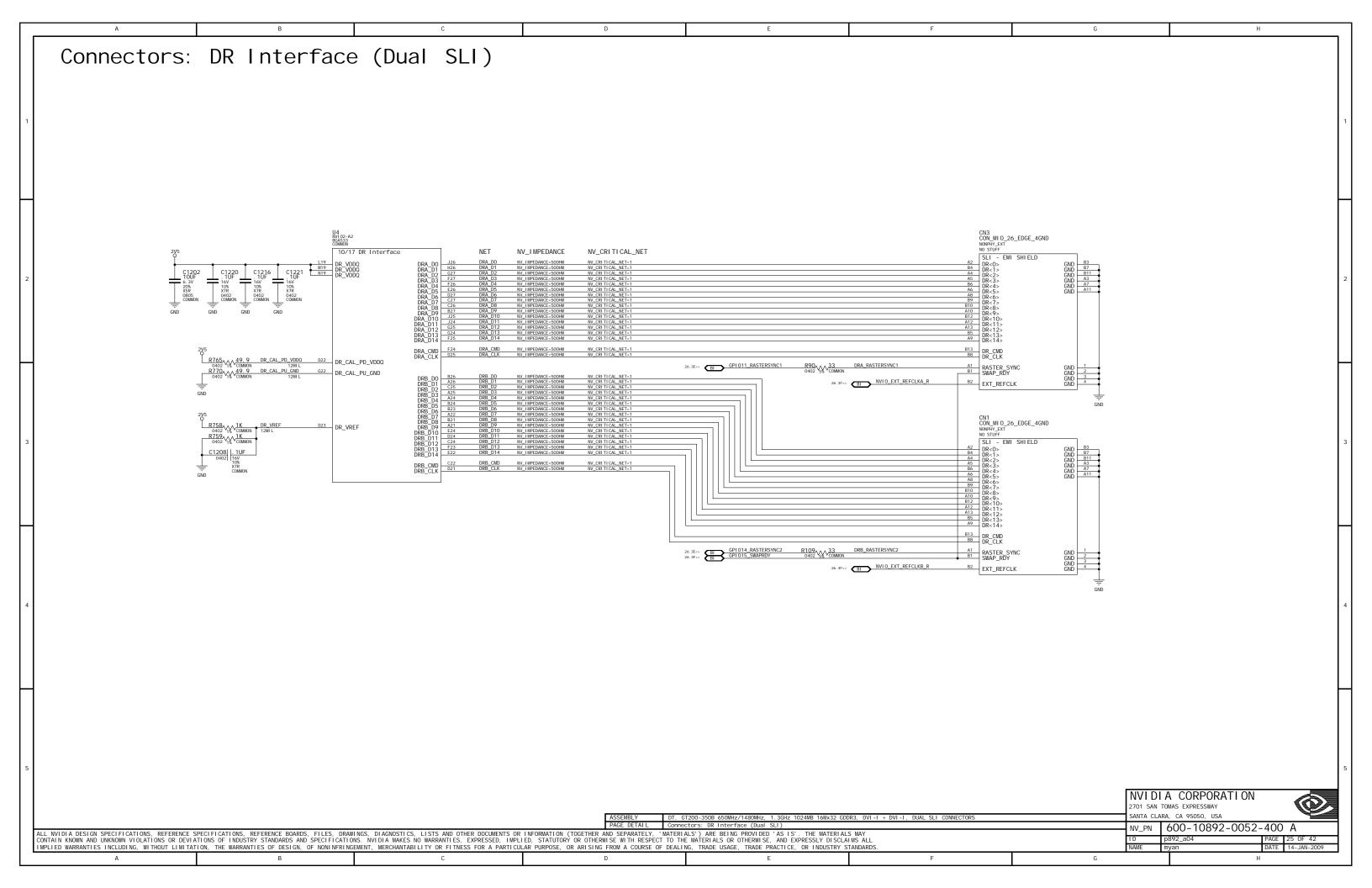


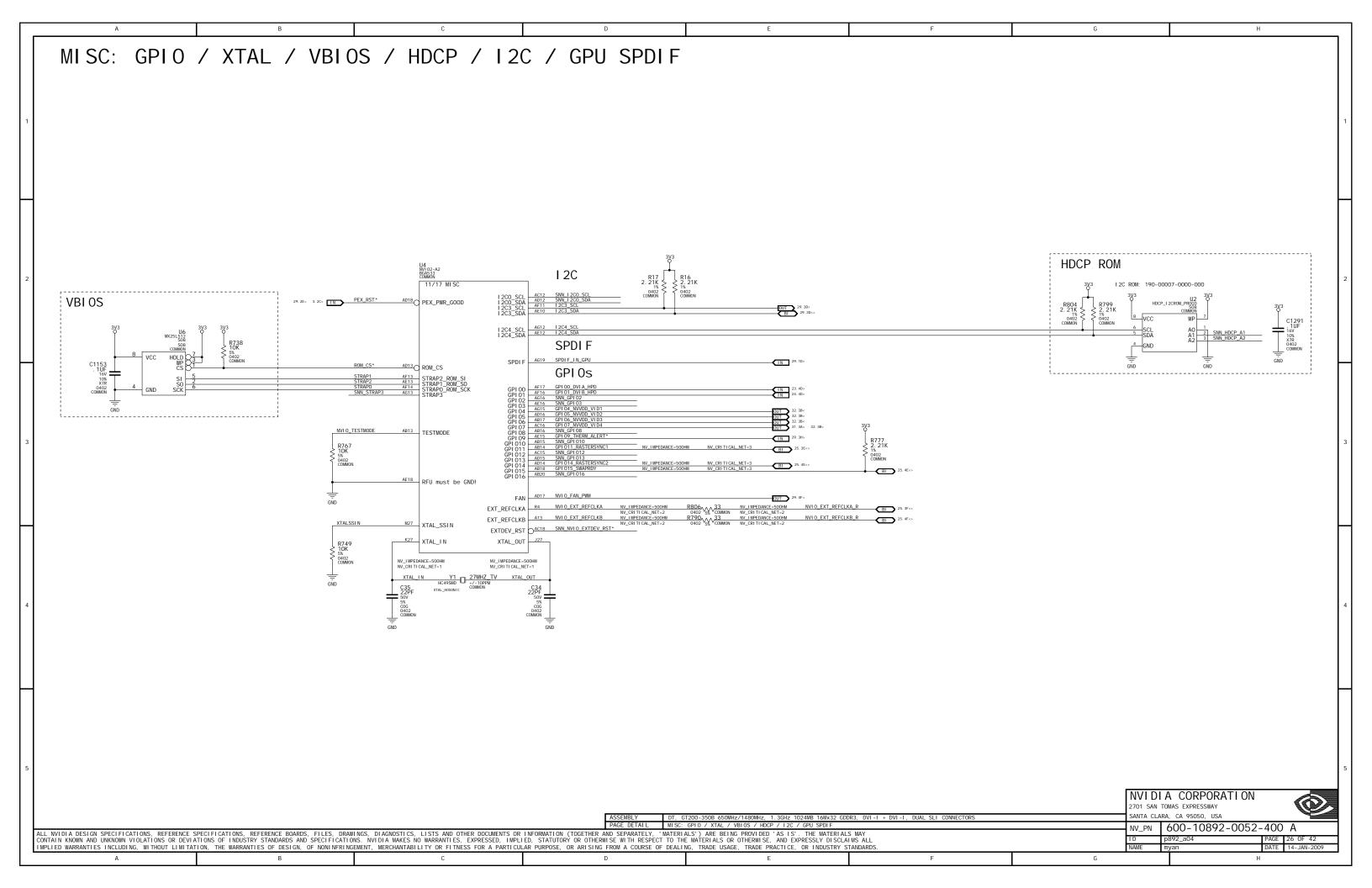


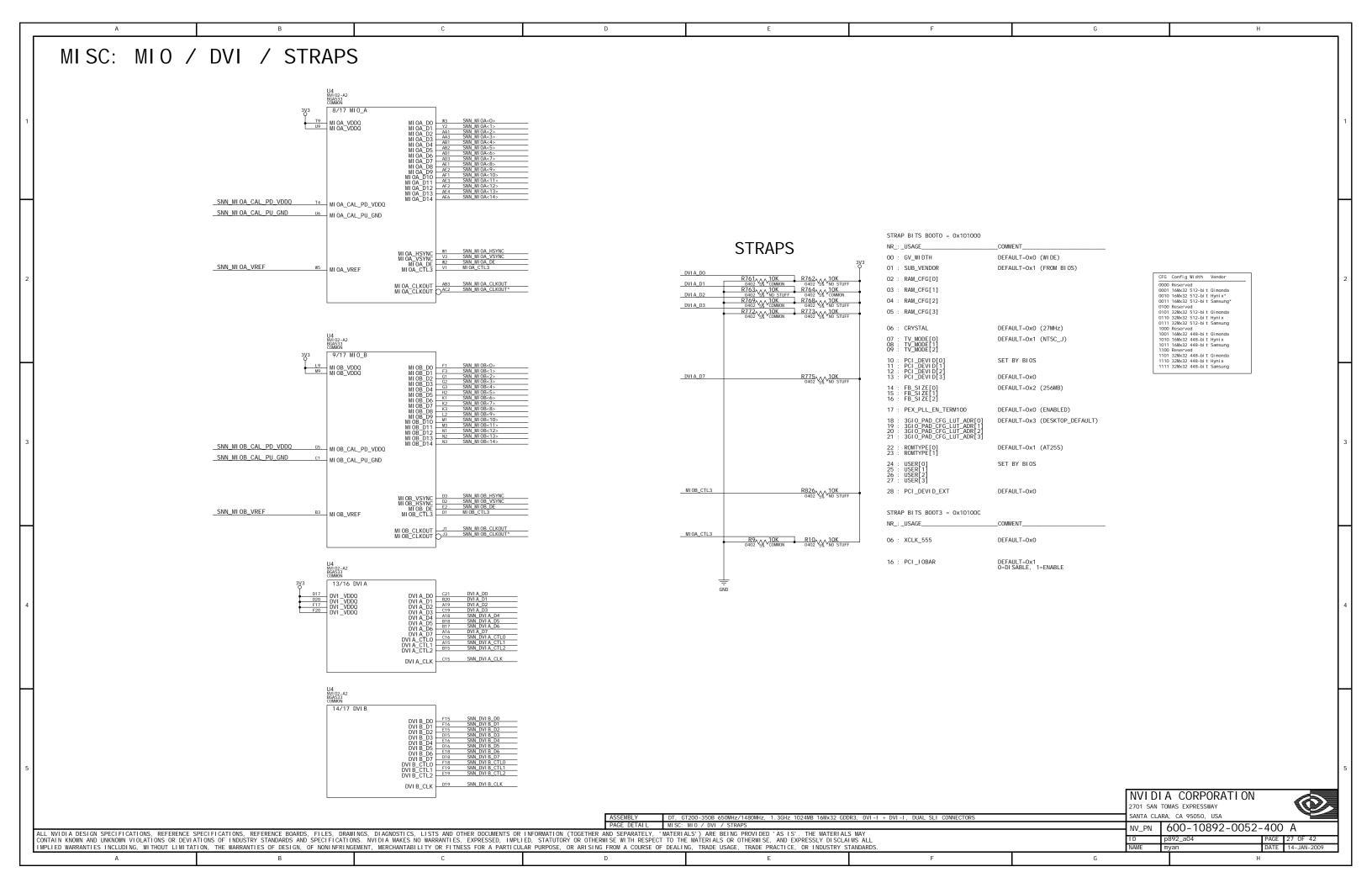


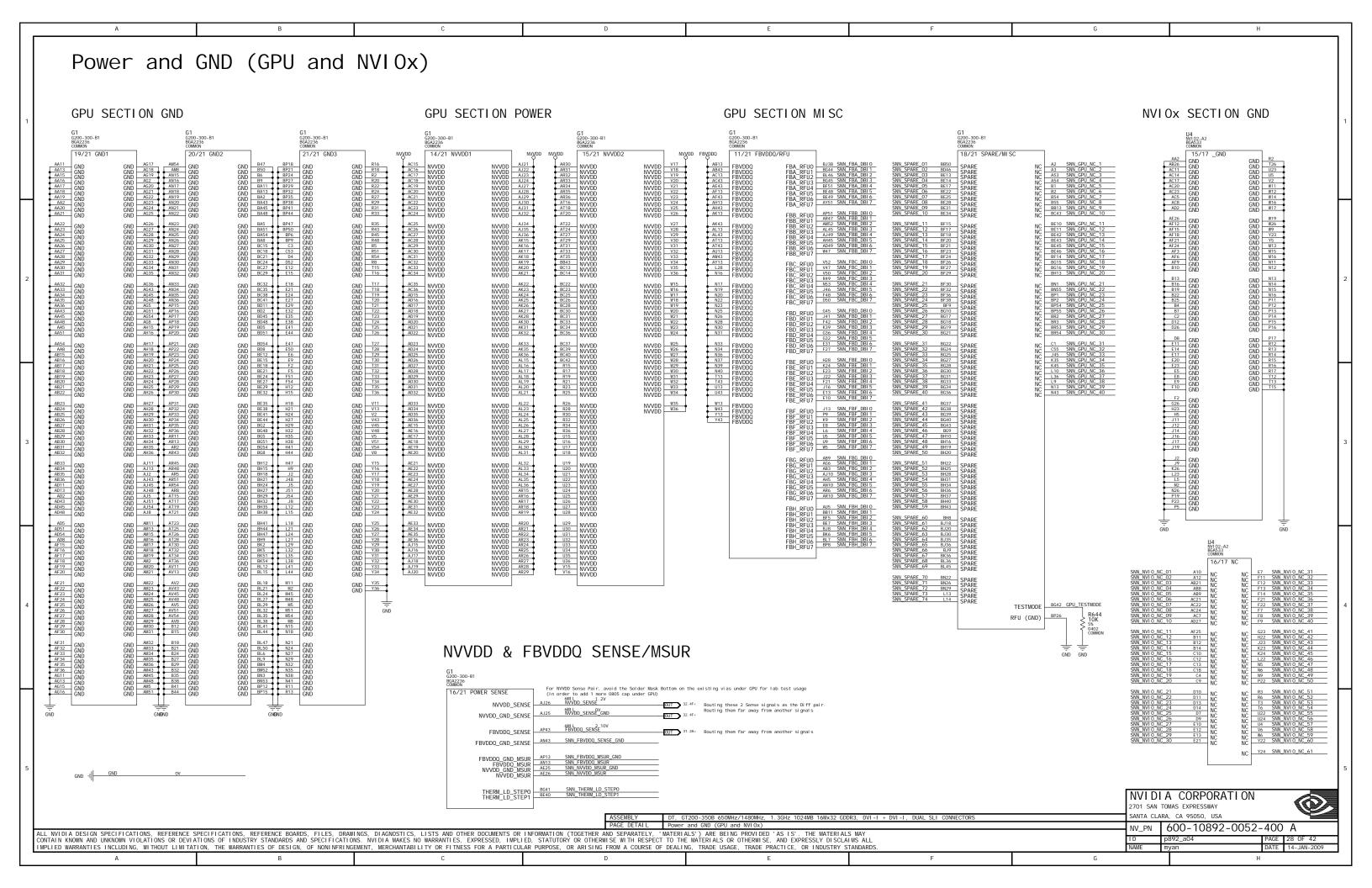


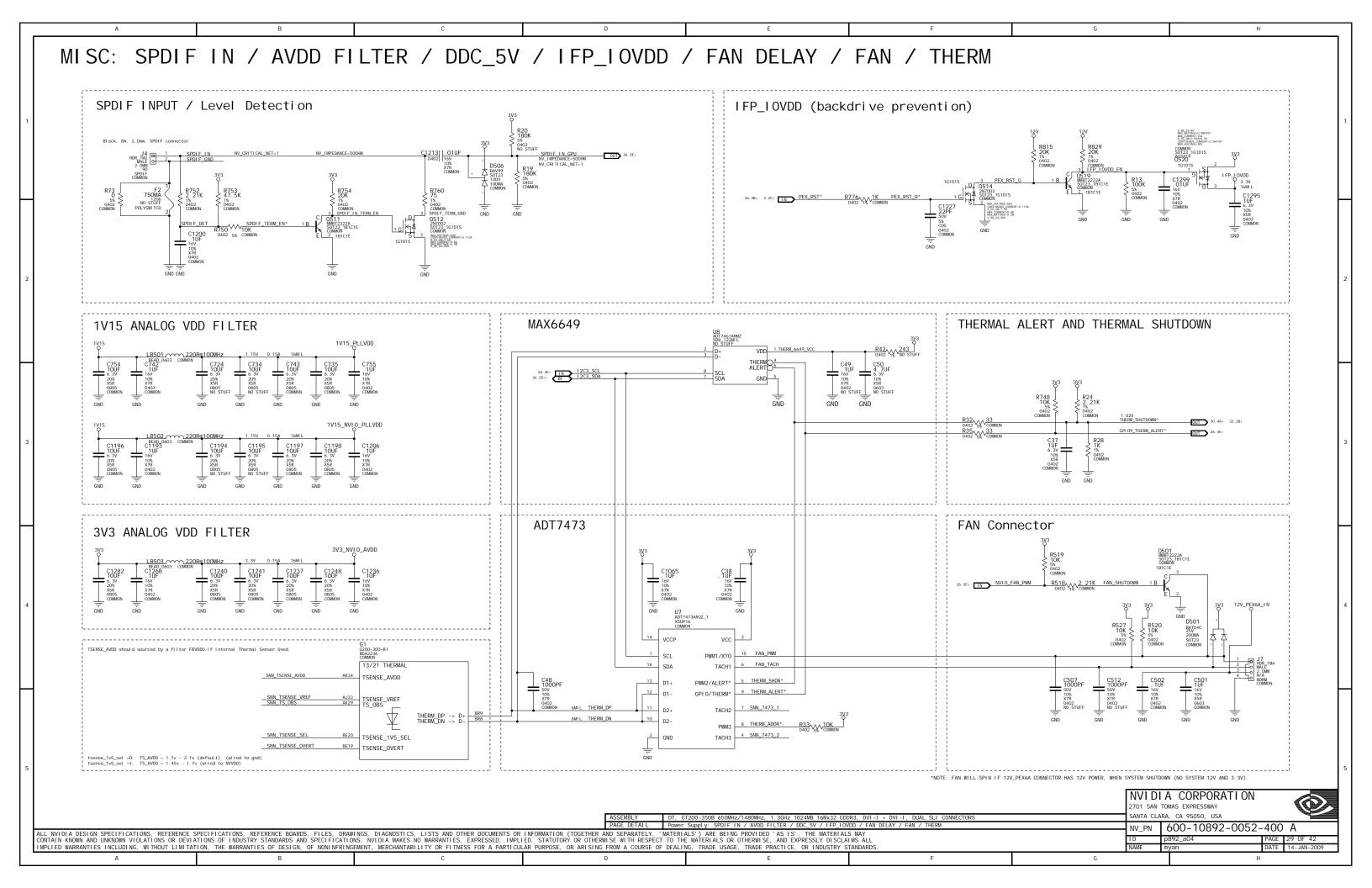


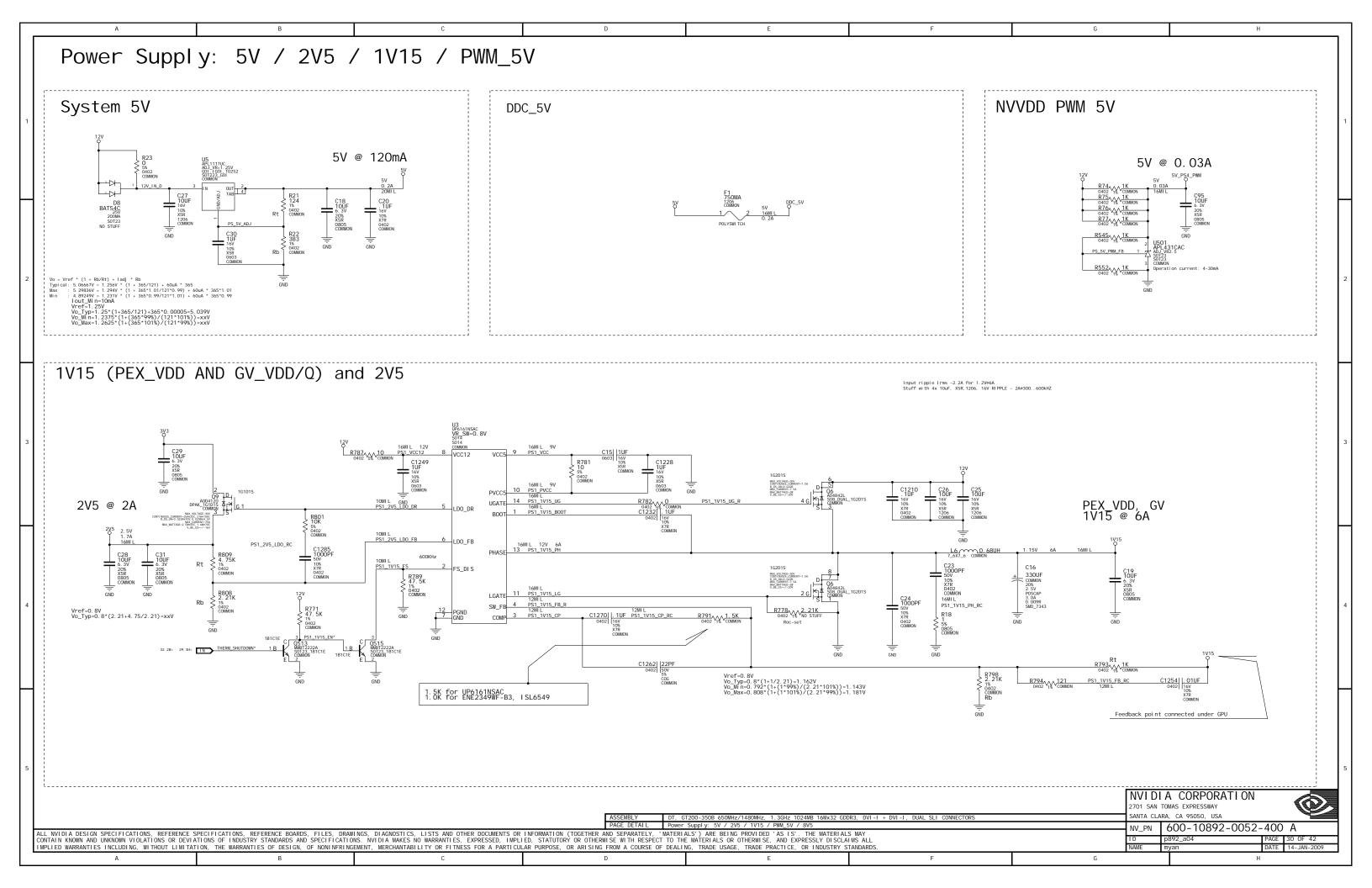


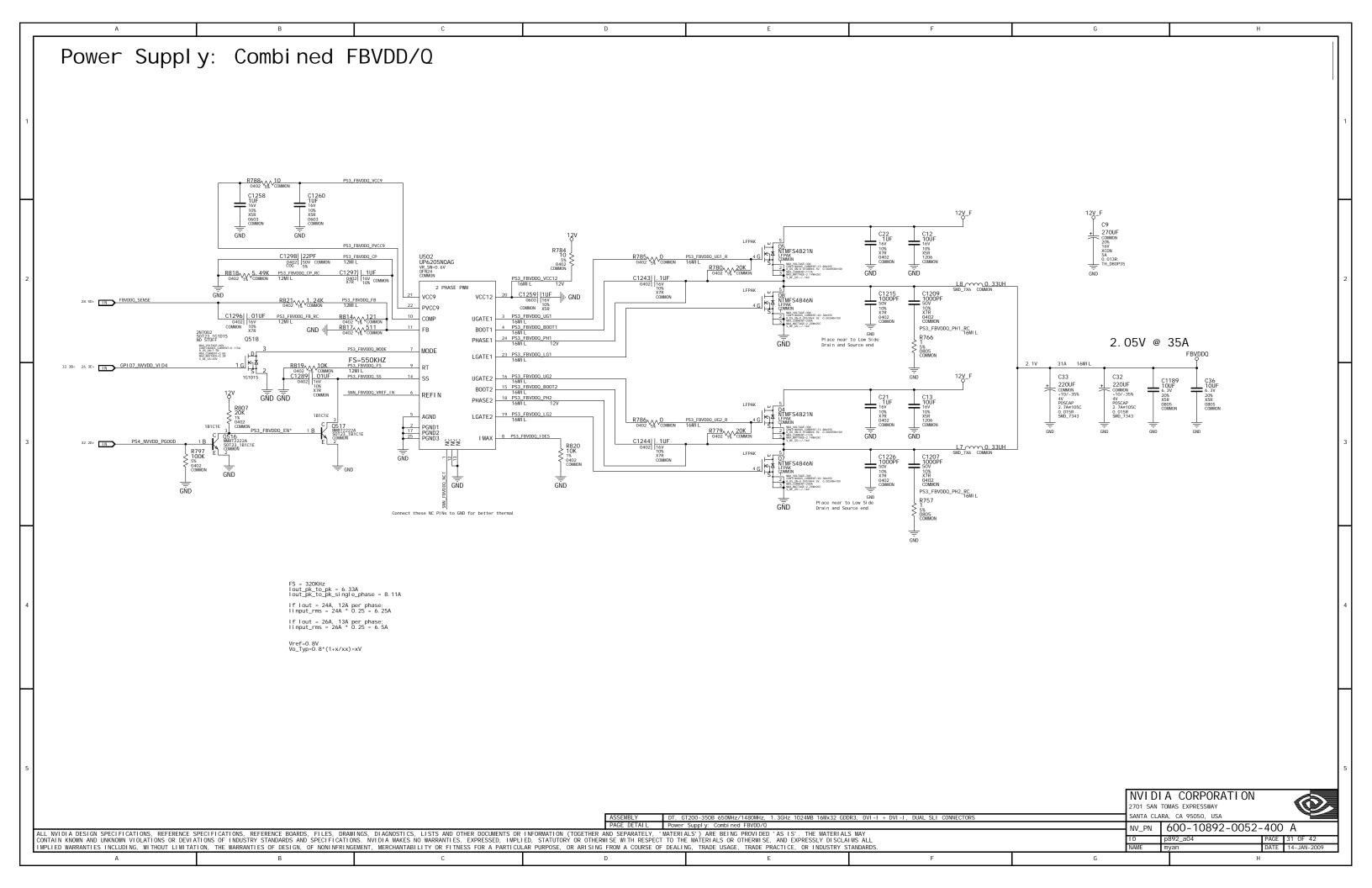


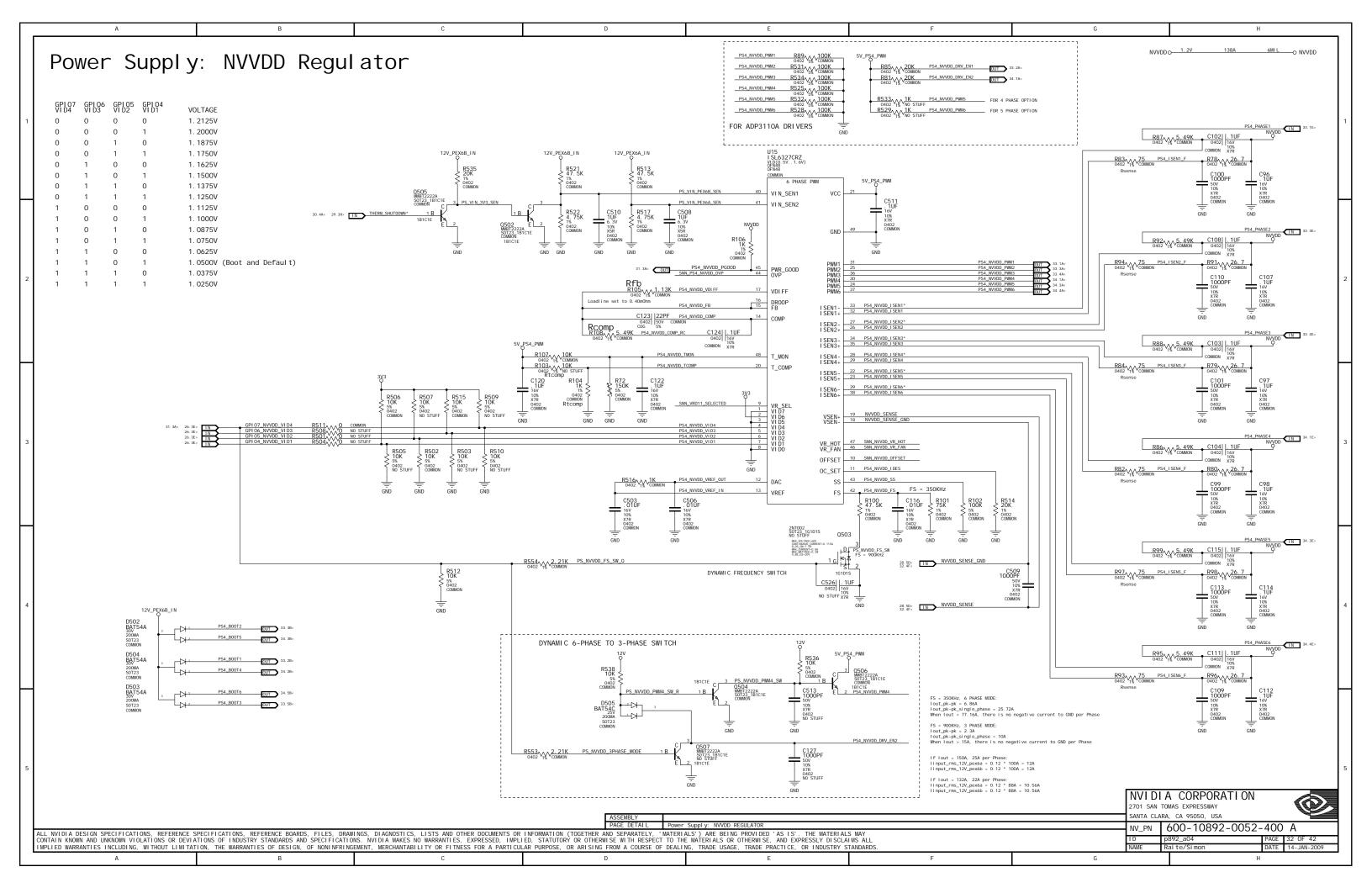


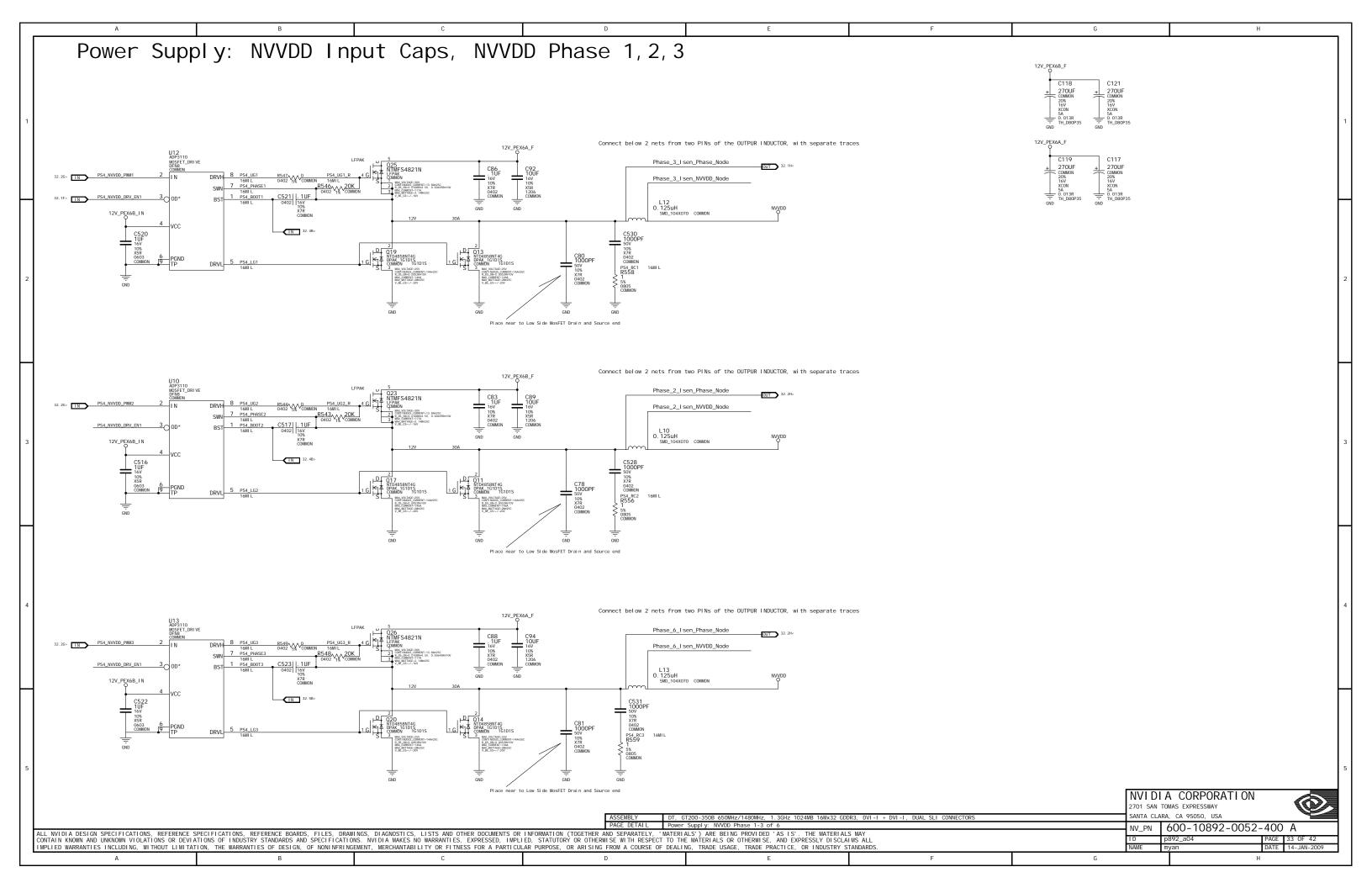


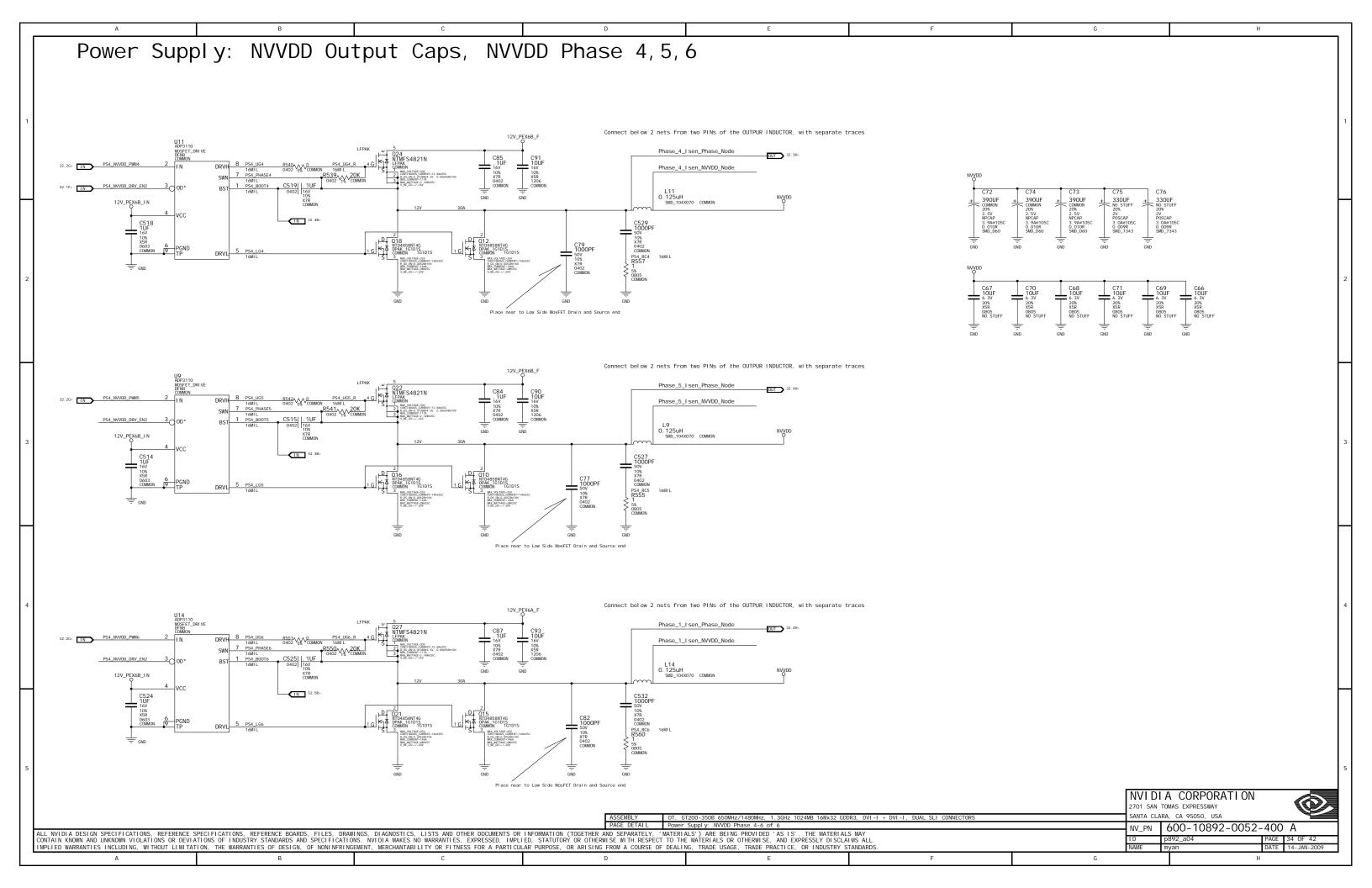


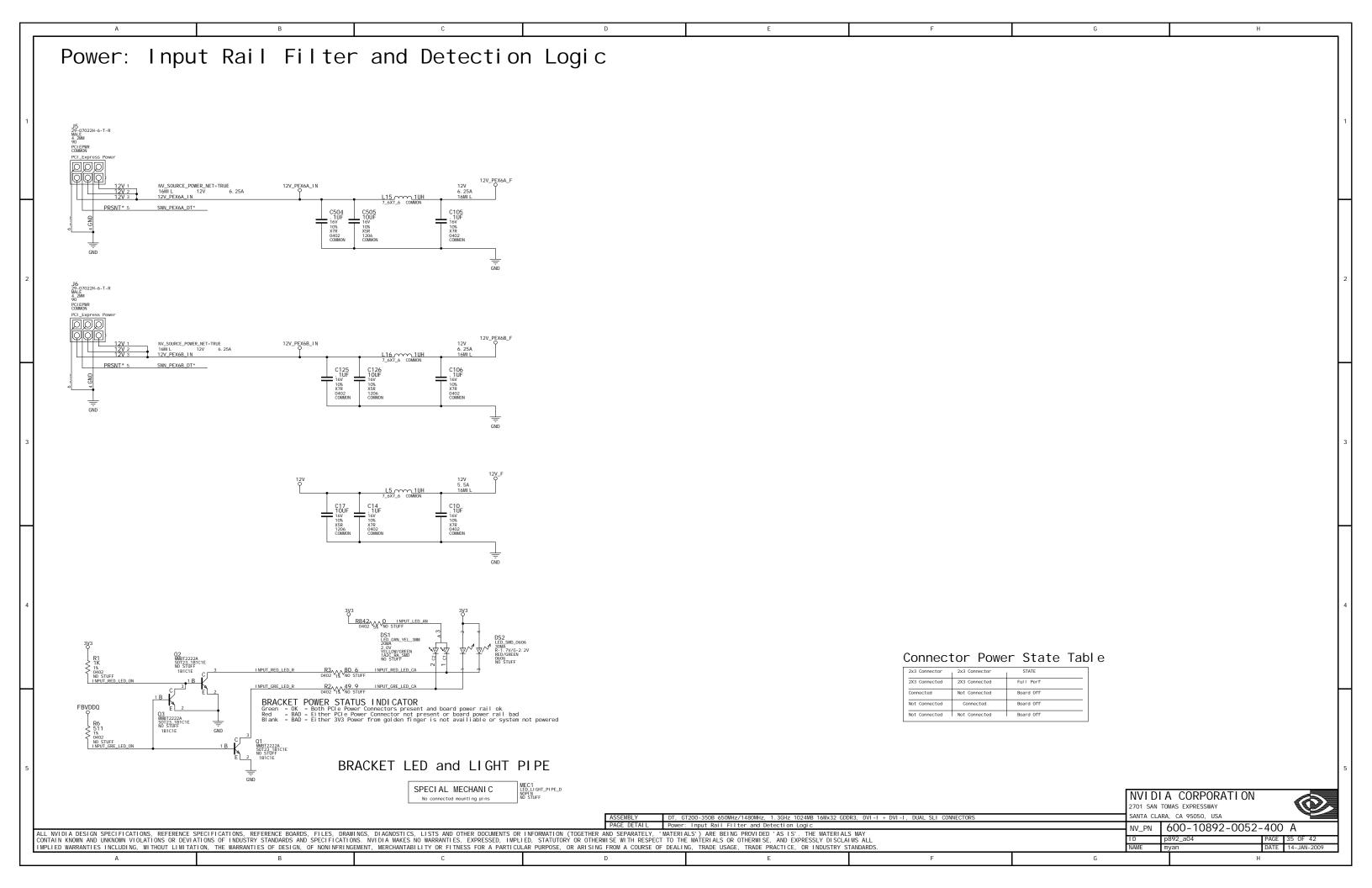




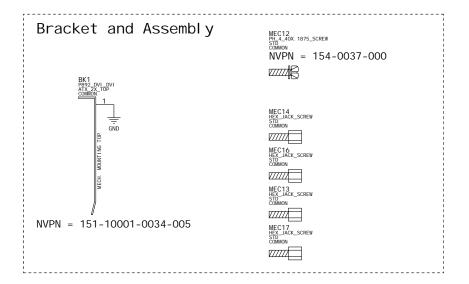


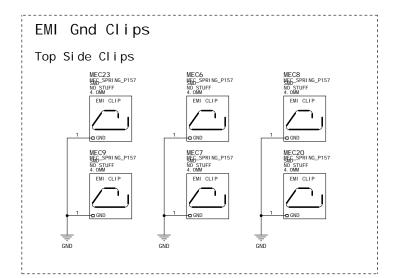


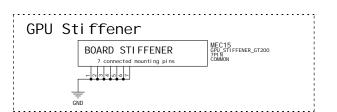


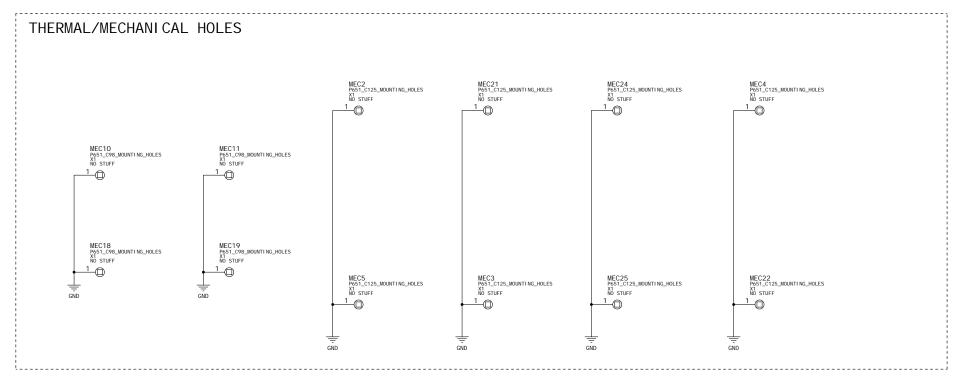












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						NVI DI A CORPORATI ON 2701 SAN TOMAS EXPRESSWAY	
				1480MHz, 1.3GHz 1024MB 16Mx32 GDDR3, DVI-I + DVI-I, D	UAL SLI CONNECTORS	SANTA CLARA, CA 95050, USA	
		DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION		PROVIDED 'AS IS'. THE MATERIALS MAY		NV_PN 600-10892-0052	
	TIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. I	NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTO	RY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR O	THERWISE, AND EXPRESSLY DISCLAIMS ALL		ID p892_a04	PAGE 37 OF 42
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	А		В	С		D		E		F	G		Н	
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	11. 5C		11. 5A<	FBE_D<0>	6. 1A 6. 1F 12. 2A 12. 3A	FBE_DQS_RN7	6. 3B 6. 3G< 12. 4C	FBF_D<5>	6. 1G 6. 2D 13. 2A 13. 4A	FBF_DQS_WP2	6. 3D 6. 3H> 13. 4A	FBG_D<6>	7. 1F 7. 2A 14. 2A 14. 4A	
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)_D<42> )_D<43>	5. 2E 5. 2G 11. 3C 11. 4A 5. 2E 5. 2G 11. 3C 11. 4A	FBE_CMD<2>	6. 3A 6. 4F 12. 1A 12. 1A 12. 5A	FBE_D<43> FBE_D<44>	6. 2B 6. 2F 12. 3C 12. 4A 6. 2B 6. 2F 12. 4A 12. 4C		6. 3D 6. 4G 13. 1A 13. 1A 13. 5A	FBF_D<49> FBF_D<50>	6. 2E 6. 2G 13. 4A 13. 4C 6. 2E 6. 2G 13. 4A 13. 4C	FBG_CMD<6>	14. 5A 7. 3A 7. 4F 14. 1A 14. 2A	FBG_D<50> FBG_D<51>	7. 2B 7. 2F 14. 4A 14. 4C 7. 2B 7. 2F 14. 4A 14. 4C	
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	5. 2E 5. 2G 11. 4A 11. 4C 5. 2E 5. 2G 11. 4A 11. 4C	FBE_CMD<7>	6. 3A 6. 4F 12. 1A 12. 1A 12. 1C	FBE_D<53> FBE_D<54>	6. 2B 6. 2F 12. 4A 12. 4C 6. 2B 6. 2F 12. 4A 12. 4C	FBF_CMD<10>	6. 3D 6. 4G 13. 1A 13. 2A 13. 2C 13. 5F	FBF_D<59> FBF_D<60>	6. 2E 6. 3G 13. 4A 13. 4C 6. 2E 6. 3G 13. 4A 13. 4C	FBG_CMD<11>	14. 2C 14. 5F 7. 4A 7. 4F 14. 1A 14. 2A	FBG_D<60> FBG_D<61>	7. 2B 7. 3F 14. 4A 14. 4C 7. 2B 7. 3F 14. 4A 14. 4C	
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													CORPORATI ON	
						ASSEMBL		550MHz/1480MHz, 1.3GHz 1024MB 1	16Mx32 GDDR3, DVI-I + DVI-I, I	DUAL SLI CONNECTORS		SANTA CLARA,	S EXPRESSWAY CA 95050, USA	- P
/IDIA DESIGN	SPECIFICATIONS. REFERENCE SE	PECIFICATIONS. REFEREN	ICE BOARDS: FILES DRAWLING	S. DIAGNOSTICS. LISTS AND	OTHER DOCUMENTS OR IN	PAGE DE NFORMATION (TOGETHER AND SEPAR	TAIL <edit here="" in<br="" to="">ATELY, 'MATERIALS') ARE</edit>		MATERIALS MAY			NV_PN 6	00-10892-0052-40	
N KNOWN AND	UNKNOWN VIOLATIONS OR DEVIA	TIONS OF INDUSTRY STAM	DARDS AND SPECIFICATIONS.	NVIDIA MAKES NO WARRANTI	ES, EXPRESSED, IMPLIED	D, STATUTORY OR OTHERWISE WITH	RESPECT TO THE MATERIAL	S OR OTHERWISE, AND EXPRESSL	Y DISCLAIMS ALL				PAG	GE 38 OF 4
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	А				U		F	п
FBG_DQM3	7. 3A 7. 3G<> 14. 4B		15. 1C	15. 5A<>	GV_TX7* 19. 2D	MI OA_CTL3 27. 2C 27. 4D	PEX_TX_C4* 3. 3C	PS4_NVVDD_I SEN3 32.2F
	14. 5A<>	FBH_CMD<19>	7. 4D 7. 4G 15. 1A 15. 1A	FBH_DQM6 7. 3E 7. 3H<> 15. 4C	GV_TX8 19. 2D	MI OB_CTL3 27. 3C 27. 3D	PEX_TX_C5 3. 3C	PS4_NVVDD_I SEN3* 32. 2F
FBG_DQM4	7. 3B 7. 3G<> 14. 4C 14. 5A<>	FBH_CMD<20>	15. 1C 7. 4D 7. 4G 15. 1A 15. 1C	15. 5A<> FBH_DOM7 7. 3E 7. 3H<> 15. 4C	GV_TX8* 19. 2D GV_TX9 19. 2D	NVI O_CLK_RSET_GND 19.5B NVI O_EXT_REFCLKA 26.3D	PEX_TX_C5* 3.3C PEX_TX_C6 3.3C	PS4_NVVDD_I SEN4 32. 2F PS4_NVVDD_I SEN4* 32. 2F
FBG_DQM5	7. 3B 7. 3G<> 14. 4C 14. 5A<>	FBH_CMD<21>	15. 2A 7. 4D 7. 4G 15. 1A 15. 1C	15. 5A<> FBH_DOS_RNO 7. 3D 7. 3H< 15. 4A	GV_TX9* 19. 2D GV_TX10 19. 2D	NVI O_EXT_REFCLKA_R 25. 3F<> 26. 3F<> NVI O_EXT_REFCLKB 26. 3D	PEX_TX_C6* 3.3C PEX_TX_C7 3.3C	PS4_NVVDD_I SEN5 32. 3F PS4_NVVDD_I SEN5* 32. 3F
FBG_DQM6	7. 3B 7. 3G<> 14. 4C		15. 2A	15. 5A<	GV_TX10* 19. 2D	NVI 0_EXT_REFCLKB_R 25. 4F<> 26. 3F<>	PEX_TX_C7* 3. 3C	PS4_NVVDD_I SEN6 32. 3F
FBG_DQM7	14. 5A<> 7. 3B 7. 3G<> 14. 4C	FBH_CMD<23>	7. 4D 7. 4G 15. 1C 15. 2A 15. 5C	FBH_DQS_RN1 7. 3D 7. 3H< 15. 4B 15. 5A<	GV_TX11 19. 2D GV_TX11* 19. 2D	NVI O_FAN_PWM 26. 3E> 29. 4F< NVI O_GVDR_RX_RSET_ 19. 3F	PEX_TX_C8 3. 4C PEX_TX_C8* 3. 4C	PS4_NVVDD_I SEN6* 32. 3F PS4_NVVDD_PG00D 31. 3A< 32. 2D>
	14. 5A<>	FBH_CMD<24>	7. 4D 7. 5G 15. 1C 15. 2A	FBH_DQS_RN2 7. 3D 7. 3H< 15. 4A	GV_TX12 19. 2D	GND	PEX_TX_C9 3. 4C	PS4_NVVDD_PWM1 32.1E 32.2G> 33.1A<
	7. 3A 7. 3G< 14. 4A 14. 5A<	FBH_CMD<25>	15. 5C 7. 4D 7. 5G 15. 1C 15. 2A	15. 5A FBH_DQS_RN3 7. 3D 7. 3H FBH_DQS_RN3 7. 3D	GV_TX12* 19. 2D GV_TX13 19. 2D	NVI O_GVDR_TX_RSET_ 19. 3F GND	PEX_TX_C9* 3. 4C PEX_TX_C10 3. 4C	PS4_NVVDD_PWM2 32.1E 32.2G> 33.3A< PS4_NVVDD_PWM3 32.1E 32.2G> 33.4A<
FBG_DQS_RN1	7. 3A 7. 3G< 14. 4B 14. 5A<	FBH_CMD<26>	15. 5C 7. 4D 7. 5G 15. 1C 15. 2A	15. 5A< FBH_DOS_RN4 7. 3E 7. 3H< 15. 4C	GV_TX13* 19. 2D GV_TX14 19. 2D	NVI 0_TESTMODE 26. 3B NVVDD_SENSE 28. 5D> 32. 4F< 32. 4F<	PEX_TX_C10* 3. 4C PEX_TX_C11 3. 4C	PS4_NVVDD_PWM4 32. 1E 32. 2G> 32. 5F 34. 1A<
FBG_DQS_RN2	7. 3A 7. 3G< 14. 4A		15. 5C	15. 5A<	GV_TX14* 19. 2D	NVVDD_SENSE_GND 28. 5D> 32. 4F< 32. 4F<	PEX_TX_C11* 3. 4C	PS4_NVVDD_PWM5 32.1E 32.1F 32.2G>
FBG_DQS_RN3	14. 5A< 7. 3A 7. 3G< 14. 4B	FBH_CMD<27>	7. 4D 7. 5G 15. 1C 15. 2A 15. 5C	FBH_DQS_RN5 7. 3E 7. 3H< 15. 4C 15. 5A<	GV_TX15 19. 2D GV_TX15* 19. 2D	PEX_PRSNT* 3. 1A PEX_REFCLK 3. 2B	PEX_TX_C12 3. 4C PEX_TX_C12* 3. 4C	34. 3A< PS4_NVVDD_PWM6 32. 1E 32. 1F 32. 2G>
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	14. 5A<	FBH_D<0>	7. 1D 7. 1G 15. 2A 15. 3A	FBH_DQS_RN7 7. 3E 7. 3H< 15. 4C	GV_TX17 19. 3D	PEX_RST_0 29.1F	PEX_TX_C14 3.5C	PS4_NVVDD_TCOMP 32. 3D
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FBG_DQS_WPO	14. 5A< 7. 3A 7. 3G> 14. 4A	FBH_D<5> FBH_D<6>	7. 1G 7. 2D 15. 2A 15. 4A 7. 1G 7. 2D 15. 2A 15. 4A	FBH_DQS_WP2 7. 3D 7. 3H> 15. 4A 15. 5A>	GV_TXCLK 19. 3D GV_TXCLK* 19. 3D	PEX_RX2 3.3B PEX_RX2* 3.3B	PS1_1V15_CP_RC 30. 4D PS1_1V15_EN* 30. 4B	PS4_NVVDD_VI D4 32. 3D PS4_NVVDD_VREF_I N 32. 3D
	14. 5A>	FBH_D<7>	7. 1G 7. 2D 15. 3A 15. 4A	FBH_DQS_WP3 7. 3D 7. 4H> 15. 4B	GV_TXCTL 19. 3D	PEX_RX3 3. 3B	PS1_1V15_FB_R 30. 4D	PS4_NVVDD_VREF_OUT 32. 3D
FBG_DQS_WP1	7. 3A 7. 3G> 14. 4B 14. 5A>	FBH_D<8> FBH_D<9>	7. 1G 7. 2D 15. 3A 15. 3B 7. 1G 7. 2D 15. 3A 15. 3B	15. 5A> FBH_DOS_WP4 7. 3E 7. 4H> 15. 4C	GV_TXCTL* 19.3D GV_TX_RSET_GND 19.3C	PEX_RX3* 3. 3B PEX_RX4 3. 3B	PS1_1V15_FB_RC 30. 4G PS1_1V15_FS 30. 4C	PS4_PHASE1 32. 1H< 33. 1E> PS4_PHASE2 32. 2H< 33. 3E>
FBG_DQS_WP2	7. 3A 7. 3G> 14. 4A	FBH_D<10>	7. 1G 7. 2D 15. 3A 15. 3B	15. 5A>	I 2C1_SCL 20. 3C	PEX_RX4* 3. 3B	PS1_1V15_LG 30. 4D	PS4_PHASE3 32. 2H< 33. 4E>
FBG_DQS_WP3	14. 5A> 7. 3A 7. 4G> 14. 4B	FBH_D<11> FBH_D<12>	7. 1G 7. 2D 15. 3A 15. 3B 7. 1G 7. 2D 15. 3A 15. 4B	FBH_DQS_WP5 7. 3E 7. 4H> 15. 4C 15. 5A>	12C1_SCL_CON	PEX_RX5 3. 3B PEX_RX5* 3. 3B	PS1_1V15_PH 30. 4D PS1_1V15_PH_RC 30. 4F	PS4_PHASE4 32. 3H< 34. 1E> PS4_PHASE5 32. 4H< 34. 3E>
FBG_DQS_WP4	14. 5A> 7. 3B 7. 4G> 14. 4C	FBH_D<13> FBH_D<14>	7. 1G 7. 2D 15. 3A 15. 4B 7. 1G 7. 2D 15. 3A 15. 4B	FBH_DOS_WP6 7. 3E 7. 4H> 15. 4C 15. 5A>	12C1_SDA	PEX_RX6 3.3B PEX_RX6* 3.3B	PS1_1V15_UG 30. 3D PS1_1V15_UG_R 30. 3E	PS4_PHASE6 32. 4H< 34. 4E> PS4_RC1 33. 2D
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FBG_DQS_WP5	7. 3B 7. 4G> 14. 4C 14. 5A>	FBH_D<16> FBH_D<17>	7. 1G 7. 2D 15. 3A 15. 4A 7. 1G 7. 2D 15. 3A 15. 4A	15. 5A> FBH_SEN1 15. 2A	12C2_SCL	PEX_RX7* 3. 4B PEX_RX8 3. 4B	PS1_2V5_LD0_FB 30. 4C PS1_2V5_LD0_RC 30. 4B	PS4_RC3 33.5D PS4_RC4 34.2D
FBG_DQS_WP6	7. 3B 7. 4G> 14. 4C 14. 5A>	FBH_D<18> FBH_D<19>	7. 1G 7. 2D 15. 3A 15. 4A 7. 1G 7. 2D 15. 3A 15. 4A	FBH_SEN2 15. 2C FBH_VREF1 15. 2H 15. 3B 15. 3D	12C2_SCL_R	PEX_RX8* 3.4B PEX_RX9 3.4B	PS1_PVCC 30. 3D PS1_VCC 30. 3D	PS4_RC5 34.3D PS4_RC6 34.5D
FBG_DQS_WP7	7. 3B 7. 4G> 14. 4C	FBH_D<20>	7. 1G 7. 2D 15. 3A 15. 4A	FBH_VREF2 15. 2H 15. 3D	I 2C2_SDA_CON 21. 1H<> 23. 3G<	PEX_RX9* 3. 4B	PS1_VCC12 30. 3C	PS4_UG1 33. 1B
FBG_SEN1	14. 5A> 14. 2A	FBH_D<21> FBH_D<22>	7. 1G 7. 2D 15. 3A 15. 4A 7. 1G 7. 2D 15. 3A 15. 4A	FBH_Z01 15. 2A FBH_Z02 15. 2C	I 2C2_SDA_R	PEX_RX10 3. 4B PEX_RX10* 3. 4B	PS3_FBVDDQ_B00T1 31. 2C PS3_FBVDDQ_B00T2 31. 3C	PS4_UG1_R 33.1B PS4_UG2 33.3B
FBG_SEN2	14. 2C	FBH_D<23>	7. 1G 7. 2D 15. 3A 15. 4A	FBVDDQ_SENSE 28.5D> 31.2A<	I 2C3_SDA 26. 2E<> 29. 3D<>	PEX_RX11 3. 4B	PS3_FBVDDQ_CP 31. 2B	PS4_UG2_R 33. 3B
FBG_VREF1 FBG_VREF2	14. 1H 14. 3B 14. 2H 14. 3B 14. 3D	FBH_D<24> FBH_D<25>	7. 1G 7. 2D 15. 3A 15. 4B 7. 1G 7. 2D 15. 3A 15. 4B	FB_CAL_PD_VDDQ	12C4_SCL 26. 2D 12C4_SDA 26. 2D	PEX_RX11* 3. 4B PEX_RX12 3. 5B	PS3_FBVDDQ_CP_RC 31. 2B PS3_FBVDDQ_EN* 31. 3B	PS4_UG3 33.4B PS4_UG3_R 33.4B
FBG_ZQ1 FBG_ZQ2	14. 2A 14. 2C	FBH_D<26> FBH_D<27>	7. 1G 7. 2D 15. 3A 15. 4B 7. 2D 7. 2G 15. 3A 15. 4B	FB_CAL_TERM_GND		PEX_RX12* 3.5B PEX_RX13 3.5B	PS3_FBVDDQ_FB	PS4_UG4 34. 1B PS4_UG4_R 34. 1B
_	7. 4D 7. 5H> 15. 2A	FBH_D<28>	7. 2D 7. 2G 15. 3A 15. 4B	GPI 00_DVI A_HPD_CON 23. 4F	I FPA_TXC 23. 2E	PEX_RX13* 3.5B	PS3_FBVDD0_FS 31.3B	PS4_UG5 34. 3B
FBHO_CLKO*	15. 2A< 15. 4G 7. 4D 7. 5H> 15. 2A	FBH_D<29> FBH_D<30>	7. 2D 7. 2G 15. 3A 15. 4B 7. 2D 7. 2G 15. 3A 15. 4B	GPI 00_DVI A_HPD_R 23. 4E GPI 01_DVI B_HPD 24. 4D> 26. 3E<	I FPA_TXC*	PEX_RX14 3.5B PEX_RX14* 3.5B	PS3_FBVDDQ_I DES	PS4_UG5_R 34.3B PS4_UG6 34.4B
FBHO_CLKO_R	15. 2A< 15. 4G	FBH_D<31>	7. 2G 7. 3D 15. 3A 15. 4B	GPI 01_DVI B_HPD_CON 24. 4F GPI 01_DVI B_HPD_R 24. 4E	I FPA_TXDO* 23. 2E	PEX_RX15 3.5B PEX_RX15* 3.5B	PS3_FBVDDQ_LG2 31.3C	PS4_UG6_R 34. 4B
FBH0_CLK0_R FBH1_CLK0	15. 4H 7. 4E 7. 5H> 15. 2A<	FBH_D<32> FBH_D<33>	7. 1E 7. 2G 15. 3A 15. 3C 7. 2E 7. 2G 15. 3A 15. 3C	GPI 04_NVVDD_VI D1 26. 3E> 32. 3B<	I FPA_TXD1	PEX_TSTCLK_OUT 3. 4F	PS3_FBVDD0_MODE 31. 2B PS3_FBVDD0_PH1 31. 2C	PS_5V_ADJ 30. 2B PS_5V_PWM_FB 30. 2G
FBH1_CLKO*	15. 2C 15. 4G 7. 4E 7. 5H> 15. 2A<	FBH_D<34> FBH_D<35>	7. 2E 7. 2G 15. 3A 15. 3C 7. 2E 7. 2G 15. 3A 15. 3C	GPI 05_NVVDD_VI D2 26. 3E> 32. 3B< GPI 06_NVVDD_VI D3 26. 3E> 32. 3B<	I FPA_TXD2	PEX_TSTCLK_OUT* 3. 4F PEX_TX0 3. 2E	PS3_FBVDD0_PH1_RC 31.2F PS3_FBVDD0_PH2 31.3C	PS_NVVDD_3PHASE_MO 32.5D DE
_	15. 2C 15. 4G	FBH_D<36>	7. 2E 7. 2G 15. 3A 15. 4C	GPI 07_NVVDD_VI D4 26. 3E> 31. 3A< 32. 3B<	I FPB_TXD4 23. 3E	PEX_TX0* 3. 2E	PS3_FBVDDQ_PH2_RC 31.3F	PS_NVVDD_FS_SW 32.4F
FBH1_CLKO_R FBH_CMD<0>	15. 4H 7. 3D 7. 4G 15. 1A 15. 1A	FBH_D<37> FBH_D<38>	7. 2E 7. 2G 15. 4A 15. 4C 7. 2E 7. 2G 15. 4A 15. 4C	GPI 09_THERM_ALERT* 26. 3E< 29. 3H> GPI 011_RASTERSYNC1 25. 3E<> 26. 3E<>	I FPB_TXD4*	PEX_TX1 3. 2E PEX_TX1* 3. 2E	PS3_FBVDD0_PVCC9 31. 2B PS3_FBVDD0_SS 31. 3B	PS_NVVDD_FS_SW_Q 32.4D PS_NVVDD_PWM4_SW 32.4E
FBH_CMD<028>	15. 5A 7. 4H> 15. 1A<	FBH_D<39> FBH_D<40>	7. 2E 7. 2G 15. 4A 15. 4C 7. 2E 7. 2G 15. 3C 15. 4A	GPI 014_RASTERSYNC2 25. 4E<> 26. 3E<> GPI 015_SWAPRDY 25. 4E<> 26. 3F<>	I FPB_TXD5*	PEX_TX2 3. 2E PEX_TX2* 3. 2E	PS3_FBVDDQ_UG1	PS_NVVDD_PWM4_SW_R 32.5D PS_VI N_3V3_SEN 32.2C
FBH_CMD<1>	7. 3D 7. 4G 15. 1A 15. 1A	FBH_D<41>	7. 2E 7. 2G 15. 3C 15. 4A	GPU_BUFCLK_I N 19. 4D	I FPB_TXD6* 23. 3E	PEX_TX3 3. 3E	PS3_FBVDDQ_UG2 31.3C	PS_VI N_PEX6A_SEN 32. 2D
FBH_CMD<2>	15. 5A 7. 3D 7. 4G 15. 1A 15. 1A	FBH_D<42> FBH_D<43>	7. 2E 7. 2G 15. 3C 15. 4A 7. 2E 7. 2G 15. 3C 15. 4A	GPU_CLK 19. 4B GPU_CLK* 19. 4B	I FPCD_I OVDD	PEX_TX3* 3. 3E PEX_TX4 3. 3E	PS3_FBVDDQ_UG2_R 31. 3D PS3_FBVDDQ_VCC9 31. 1B	PS_VI N_PEX6B_SEN 32. 1D ROM_CS* 26. 3B
	15. 5A	FBH_D<44>	7. 2E 7. 2G 15. 4A 15. 4C	GPU_HOT_RESET* 19. 4D	I FPC_TXC 24. 2E	PEX_TX4* 3. 3E	PS3_FBVDDQ_VCC12 31.2C	SNN_3V3_AUX 3. 1A
	7. 3D 7. 4G 15. 1A 15. 1A 15. 5A	FBH_D<45> FBH_D<46>	7. 2E 7. 2G 15. 4A 15. 4C 7. 2E 7. 2G 15. 4A 15. 4C	GPU_PEX_PWR_GOOD* 19.4D GPU_PMC_I SO_RESET* 19.4D		PEX_TX5 3. 3E PEX_TX5* 3. 3E	PS4_B00T1 32. 4B> 33. 2B< PS4_B00T2 32. 4B> 33. 3B<	SNN_7473_1 29. 5E SNN_7473_2 29. 5E
FBH_CMD<4>	7. 3D 7. 4G 15. 1A 15. 1A 15. 5A	FBH_D<47> FBH_D<48>	7. 2E 7. 2G 15. 4A 15. 4C 7. 2E 7. 2G 15. 4A 15. 4C	GPU_TESTMODE 28.4G GV_RXO 19.3D	I FPC_TXDO*	PEX_TX6 3. 3E PEX_TX6* 3. 3E	PS4_B00T3	SNN_DACB_CSYNC 22.3C SNN_DACB_HSYNC 22.3C
FBH_CMD<5>	7. 3D 7. 4G 15. 1A 15. 1A	FBH_D<49>	7. 2E 7. 2G 15. 4A 15. 4C	GV_RXO* 19.3D	I FPC_TXD1* 24. 3E	PEX_TX7 3. 3E	PS4_B00T5 32.4B> 34.3B<	SNN_DACB_VSYNC 22.3C
FBH_CMD<6>	15. 5A 7. 3D 7. 4G 15. 1A 15. 2A	FBH_D<50> FBH_D<51>	7. 2E 7. 2G 15. 4A 15. 4C 7. 2E 7. 2G 15. 4A 15. 4C	GV_RX1 19. 3D GV_RX1* 19. 3D	I FPC_TXD2	PEX_TX7* 3. 3E PEX_TX8 3. 4E	PS4_B00T6 32.5B> 34.5B< PS4_I SEN1_F 32.1G	SNN_DVI A_CLK
	15. 2C 15. 5F 7. 3D 7. 4G 15. 1A 15. 1A	FBH_D<52>	7. 2E 7. 2G 15. 4A 15. 4C 7. 2E 7. 2G 15. 4A 15. 4C	GV_RX2 19. 3D	I FPD_TXD4 24. 3E	PEX_TX8* 3. 4E	PS4_I SEN2_F 32. 2G PS4_I SEN3_F 32. 3G	SNN_DVI A_CTL1 27. 4C
	15. 1C	FBH_D<53> FBH_D<54>	7. 2E 7. 2G 15. 4A 15. 4C	GV_RX3 19.3D	I FPD_TXD4*	PEX_TX9* 3. 4E	PS4_I SEN4_F 32. 3G	SNN_DVI A_D4 27. 4C
FBH_CMD<8>	7. 3D 7. 4G 15. 1A 15. 2A 15. 2C	FBH_D<55> FBH_D<56>	7. 2E 7. 2G 15. 4A 15. 4C 7. 2E 7. 2G 15. 4A 15. 4C	GV_RX3* 19. 3D GV_RXCLK 19. 4D	I FPD_TXD5*	PEX_TX10 3.4E PEX_TX10* 3.4E	PS4_I SEN5_F 32. 4G PS4_I SEN6_F 32. 4G	SNN_DVI A_D5
FBH_CMD<9>	7. 3D 7. 4G 15. 1A 15. 1A	FBH_D<57>	7. 2E 7. 3G 15. 4A 15. 4C	GV_RXCLK* 19. 4D	I FPD_TXD6* 24. 3E	PEX_TX11 3. 4E	PS4_LG1 33. 2B	SNN_DVI B_CLK 27. 5C
FBH_CMD<10>	15. 1C 7. 3D 7. 4G 15. 1A 15. 2A	FBH_D<58> FBH_D<59>	7. 2E 7. 3G 15. 4A 15. 4C 7. 2E 7. 3G 15. 4A 15. 4C	GV_RXCTL 19. 4D GV_RXCTL* 19. 4D	IFP_IOVDD_EN	PEX_TX11* 3. 4E PEX_TX12 3. 4E	PS4_LG2 33. 3B PS4_LG3 33. 5B	SNN_DVI B_CTL0
	15. 2C 15. 5F 7. 4D 7. 4G 15. 1A 15. 2A	FBH_D<60> FBH_D<61>	7. 2E 7. 3G 15. 4A 15. 4C 7. 2E 7. 3G 15. 4A 15. 4C	GV_RX_RSET_VDD 19.3C	INPUT_GRE_LED_ON 35.5A INPUT_GRE_LED_R 35.4B	PEX_TX12* 3. 4E PEX_TX13 3. 5E	PS4_LG4 34. 2B	SNN_DVIB_CTL2
	15. 2C	FBH_D<62>	7. 2E 7. 3G 15. 4A 15. 4C	GV_TXO* 19.1D	I NPUT_LED_AN 35. 4C	PEX_TX13* 3. 5E	PS4_LG6 34.5B	SNN_DVI B_D1 27. 5C
FBH_CMD<12>	7. 4D 7. 4G 15. 1A 15. 1A 15. 1C	FBH_D<63> FBH_DEBUG	7. 3E 7. 3G 15. 4A 15. 4C 7. 3E	GV_TX1 19.1D GV_TX1* 19.1D	I NPUT_RED_LED_CA 35. 4C I NPUT_RED_LED_ON 35. 4A	PEX_TX14 3. 5E PEX_TX14* 3. 5E	PS4_NVVDD_COMP 32. 2D PS4_NVVDD_COMP_RC 32. 2D	SNN_DVI B_D2 27. 5C SNN_DVI B_D3 27. 5C
FBH_CMD<13>	7. 4D 7. 4G 15. 1A 15. 2A	FBH_DOMO	7. 3D 7. 3H<> 15. 4A	GV_TX2 19. 1D	I NPUT_RED_LED_R 35. 4B	PEX_TX15 3. 5E	PS4_NVVDD_DRV_EN1 32.1F> 33.2A< 33.3A	SNN_DVI B_D4 27. 5C
FBH_CMD<14>	15. 2C 7. 4D 7. 4G 15. 1A 15. 1A	FBH_DQM1	15. 4A<> 7. 3D 7. 3H<> 15. 4B	GV_TX2* 19. 1D GV_TX3 19. 1D	JTAG_NVI OTDI _GPUTD 3. 1E	PEX_TX15* 3. 5E PEX_TX_CO 3. 2C	33. 4A PS4_NVVDD_DRV_EN2 32. 1F> 32. 5F 34. 1A<	SNN_DVI B_D5
	15. 1C 7. 4D 7. 4G 15. 1A 15. 2A	FBH_DQM2	15. 5A<> 7. 3D 7. 3H<> 15. 4A	GV_TX3* 19.1D GV_TX4 19.1D	JTAG_TCK 3. 1D JTAG_TDI 3. 1D	PEX_TX_C0* 3. 2C PEX_TX_C1 3. 2C	34. 3A 34. 4A	SNN_DVI B_D7 27. 5C
	15. 2C		15. 5A<>	GV_TX4* 19. 1D	JTAG_TDO 3. 1D	PEX_TX_C1* 3. 2C	PS4_NVVDD_FS 32. 3F	SNN_FBAO_CLK1
FBH_CMD<16>	7. 4D 7. 4G 15. 1A 15. 1A 15. 1C	FBH_DQM3	7. 3D 7. 3H<> 15. 4B 15. 5A<>	GV_TX5 19.1D GV_TX5* 19.1D	JTAG_TMS 3.1D  JTAG_TRST* 3.1D	PEX_TX_C2 3.2C PEX_TX_C2* 3.2C	PS4_NVVDD_I DES 32. 3F PS4_NVVDD_I SEN1 32. 2F	SNN_FBA1_CLK1
FBH_CMD<17>	7. 4D 7. 4G 15. 1A 15. 1A	FBH_DQM4	7. 3E 7. 3H<> 15. 4C	GV_TX6 19. 1D	JTAG_TRST2 3. 1G	PEX_TX_C3 3. 3C	PS4_NVVDD_I SEN1* 32. 2F	SNN_FBA_CMD<22> 4.3A
FBH_CMD<18>	15. 1C 7. 4D 7. 4G 15. 1A 15. 1A	FBH_DQM5	15. 5A<> 7. 3E 7. 3H<> 15. 4C	GV_TX6* 19. 2D GV_TX7 19. 2D	JTAG_TRST_3V3 3. 1G JTAG_TRST_3V3* 3. 1G	PEX_TX_C3* 3. 3C PEX_TX_C4 3. 3C	PS4_NVVDD_L SEN2 32. 2F PS4_NVVDD_L SEN2* 32. 2F	SNN_FBA_CMD<29> 4.4A SNN_FBA_CMD<30> 4.4A
								NVI DI A. CODDODATI ON
								NVI DI A CORPORATI ON 2701 SAN TOMAS EXPRESSWAY
						z/1480MHz, 1.3GHz 1024MB 16Mx32 GDDR3, DVI-I + DVI-I, DUA	AL SLI CONNECTORS	SANTA CLARA, CA 95050, USA
MAIDLA BETTE	ODEOLEI ONTLONO DESERVICE	UELOATIONS STORY	E BOADDO ELLEO TELIMINA	DIAGNOSTI CO. LI CTO. MIC. OTUES COCCUTATION OF COLUMN	PAGE DETAIL <edit here="" insert<="" td="" to=""><td>page detail&gt;</td><td></td><td>NV_PN 600-10892-0052-400 A</td></edit>	page detail>		NV_PN 600-10892-0052-400 A
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А	В	С	D	E F	G	Н
MA 21 \ A AA	SNN FRE CND-22> 4 4D	SNN CDI NC 21 29 20	SNN NVIO NC 12 20 40	SNN_SPARE_22 28. 2F		
D<31> 4. 4A D<32> 4. 4A	SNN_FBF_CMD<32> 6.4D   SNN_FBF_DBI0 28.3E	SNN_GPU_NC_31 28. 2G SNN_GPU_NC_32 28. 2G	SNN_NVI 0_NC_13 28. 4G SNN_NVI 0_NC_14 28. 4G	SNN_SPARE_23 28. 2F		
0BI 0 28. 1E	SNN_FBF_DBI 1 28.3E	SNN_GPU_NC_33	SNN_NVI 0_NC_15 28. 4G	SNN_SPARE_24 28. 2F		
BI 1 28. 1E BI 2 28. 1E	SNN_FBF_DBI 2	SNN_GPU_NC_34 28. 2G SNN_GPU_NC_35 28. 3G	SNN_NVI O_NC_16 28. 4G SNN_NVI O_NC_17 28. 4G	SNN_SPARE_25 28. 2F SNN_SPARE_26 28. 2F		
DBI 3 28. 1E	SNN_FBF_DBI 4 28. 3E	SNN_GPU_NC_36 28.3G	SNN_NVI 0_NC_18 28. 4G	SNN_SPARE_27 28. 2F		
DBI 4 28. 1E DBI 5 28. 1E	SNN_FBF_DBI 5	SNN_GPU_NC_37 28. 3G SNN_GPU_NC_38 28. 3G	SNN_NVI 0_NC_19 28. 4G SNN_NVI 0_NC_20 28. 4G	SNN_SPARE_28 28. 2F SNN_SPARE_29 28. 2F		
DBI 6 28. 1E	SNN_FBF_DBI 7 28. 3E	SNN_GPU_NC_39 28. 3G	SNN_NVI O_NC_21 28. 5G	SNN_SPARE_30 28. 2F		
A_DBI 7 28. 2E	SNN_FBF_NC01 13. 2A	SNN_GPU_NC_40 28.3G	SNN_NVI 0_NC_22 28. 5G	SNN_SPARE_31 28. 2F		
A_NCO1 8. 2A A_NCO4 8. 2C	SNN_FBF_NCO4	SNN_HDCP_A1	SNN_NVI 0_NC_23 28. 5G SNN_NVI 0_NC_24 28. 5G	SNN_SPARE_32 28. 2F SNN_SPARE_33 28. 2F		
30_CLK1 4. 4D	SNN_FBGO_CLK1* 7.4A	SNN_I 2CO_SCL 26. 2D	SNN_NVI 0_NC_25	SNN_SPARE_34 28. 2F		
BO_CLK1*	SNN_FBG1_CLK1	SNN_1 2CO_SDA	SNN_NVI 0_NC_26 28. 5G SNN_NVI 0_NC_27 28. 5G	SNN_SPARE_35 28.3F SNN_SPARE_36 28.3F		
B1_CLK1* 4. 4E	SNN_FBG_CMD<22> 7.4A	SNN_I 2CS_SCL_GPU 3. 1E	SNN_NVI 0_NC_28 28. 5G	SNN_SPARE_37 28. 3F		
BB_CMD<22> 4. 3D BB_CMD<29> 4. 4D	SNN_FBG_CMD<29> 7.4A   SNN_FBG_CMD<30> 7.4A	SNN_I 2CS_SDA 3. 2B SNN_I 2CS_SDA_GPU 3. 2E	SNN_NVI 0_NC_29 28. 5G SNN_NVI 0_NC_30 28. 5G	SNN_SPARE_38 28.3F SNN_SPARE_39 28.3F		
B_CMD<30> 4.4D	SNN_FBG_CMD<31> 7.4A	SNN_I FPAB_VPROBE 23. 2B	SNN_NVI O_NC_31 28. 4H	SNN_SPARE_40 28. 3F		
B_CMD<31> 4.4D B_CMD<32> 4.4D	SNN_FBG_CMD<32> 7.4A   SNN_FBG_DBI 0 28.3E	SNN_I FPA_TXD3	SNN_NVI 0_NC_32 28. 4H SNN_NVI 0_NC_33 28. 4H	SNN_SPARE_41 28.3F SNN_SPARE_42 28.3F		
B_DBI 0 28. 2E	SNN_FBG_DBI 1 28. 3E	SNN_I FPB_TXC 23. 3E	SNN_NVI O_NC_34 28. 4H	SNN_SPARE_43 28. 3F		
B_DBI 1 28. 2E	SNN_FBG_DBI 2 28. 3E	SNN_I FPB_TXC* 23. 3E	SNN_NVI O_NC_35 28. 4H	SNN_SPARE_44 28. 3F SNN_SPARE_45 28. 3F		
B_DBI 2 28. 2E B_DBI 3 28. 2E	SNN_FBG_DBI 3	SNN_I FPB_TXD7	SNN_NVI 0_NC_36 28. 4H SNN_NVI 0_NC_37 28. 4H	SNN_SPARE_45		
B_DBI 4 28. 2E	SNN_FBG_DBI 5 28. 3E	SNN_I FPCD_VPROBE 24.2B	SNN_NVI O_NC_38 28. 4H	SNN_SPARE_47 28. 3F		
B_DBI 5 28. 2E B_DBI 6 28. 2E	SNN_FBG_DBI 6	SNN_I FPC_TXD3 24. 3E SNN_I FPC_TXD3* 24. 3E	SNN_NVI 0_NC_39 28. 4H SNN_NVI 0_NC_40 28. 4H	SNN_SPARE_48 28.3F SNN_SPARE_49 28.3F		
B_DBI 7 28. 2E	SNN_FBG_NC01 14. 2A	SNN_I FPD_TXC 24. 3E	SNN_NVI O_NC_41 28. 4H	SNN_SPARE_50 28. 3F		
B_NC01 9. 2A B_NC04 9. 2C	SNN_FBG_NCO4	SNN_I FPD_TXC* 24. 3E SNN_I FPD_TXD7 24. 4E	SNN_NVI 0_NC_42 28. 4H SNN_NVI 0_NC_43 28. 4H	SNN_SPARE_51 28. 3F SNN_SPARE_52 28. 3F		
CO_CLK1 5. 4A	SNN_FBHO_CLK1* 7.4D	SNN_I FPD_TXD7* 24.4E	SNN_NVI 0_NC_44 28. 4H	SNN_SPARE_53 28. 3F		
CO_CLK1* 5. 4A	SNN_FBH1_CLK1 7. 4E	SNN_MI 0A<0> 27. 1C	SNN_NVI O_NC_45 28. 4H	SNN_SPARE_54 28.3F		
C1_CLK1 5. 4B C1_CLK1* 5. 4B	SNN_FBH1_CLK1* 7. 4E   SNN_FBH_CMD<22> 7. 4D	SNN_MI OA<1> 27. 1C   SNN_MI OA<2> 27. 1C	SNN_NVI 0_NC_46 28. 4H SNN_NVI 0_NC_47 28. 4H	SNN_SPARE_55		
C_CMD<22> 5.4A	SNN_FBH_CMD<29> 7.4D	SNN_MI 0A<3> 27. 1C	SNN_NVI 0_NC_48 28. 4H	SNN_SPARE_57 28. 3F		
C_CMD<29> 5.4A C_CMD<30> 5.4A	SNN_FBH_CMD<30> 7.4D   SNN_FBH_CMD<31> 7.4D	SNN_MI OA<4> 27. 1C SNN_MI OA<5> 27. 1C	SNN_NVI O_NC_49 28. 4H SNN_NVI O_NC_50 28. 4H	SNN_SPARE_58 28.3F SNN_SPARE_59 28.3F		
C_CMD<31> 5.4A	SNN_FBH_CMD<32> 7.4D	SNN_MI OA<6> 27. 1C	SNN_NVI 0_NC_51 28. 5H	SNN_SPARE_60 28. 3F		
C_CMD<32> 5. 4A C_DBI 0 28. 2E	SNN_FBH_DBI 0	SNN_MI OA<7> 27. 1C   SNN_MI OA<8> 27. 1C	SNN_NVI 0_NC_52 28. 5H SNN_NVI 0_NC_53 28. 5H	SNN_SPARE_61 28.3F SNN_SPARE_62 28.4F		
C_DBI 1 28. 2E	SNN_FBH_DBI 2 28. 3E	SNN_MI OA<9> 27.10	SNN_NVI 0_NC_54 28. 5H	SNN_SPARE_63 28. 4F		
C_DBI 2 28. 2E	SNN_FBH_DBI 3 28. 3E	SNN_MI OA<10> 27. 1C	SNN_NVI O_NC_55 28. 5H	SNN_SPARE_64 28. 4F		
C_DBI 3 28. 2E C_DBI 4 28. 2E	SNN_FBH_DBI 4	SNN_MI 0A<11> 27. 1C   SNN_MI 0A<12> 27. 1C	SNN_NVI 0_NC_56 28. 5H SNN_NVI 0_NC_57 28. 5H	SNN_SPARE_65 28.4F SNN_SPARE_66 28.4F		
C_DBI 5 28. 2E	SNN_FBH_DBI 6 28. 4E	SNN_MI OA<13> 27. 1C	SNN_NVI O_NC_58 28. 5H	SNN_SPARE_67 28. 4F		
C_DBI 6 28. 2E C_DBI 7 28. 2E	SNN_FBH_DBI 7 28. 4E   SNN_FBH_NC01 15. 2A	SNN_MI OA<14> 27. 1C   SNN_MI OA_CAL_PD_VD 27. 2B	SNN_NVI 0_NC_59 28. 5H SNN_NVI 0_NC_60 28. 5H	SNN_SPARE_68 28.4F SNN_SPARE_69 28.4F		
C_NC01 10. 2A	SNN_FBH_NCO4 15. 2C	DQ	SNN_NVI O_NC_61 28. 5H	SNN_SPARE_70 28. 4F		
3C_NC04 10. 2C 3DO_CLK1 5. 4D	SNN_FBVDDQ_MSUR 28.5D SNN_FBVDDQ_MSUR_GN 28.5D	SNN_MI OA_CAL_PU_GN 27. 2B	SNN_NVIO_PLL_SP_MO 19.5B N_OUT	SNN_SPARE_71 28. 4F SNN_SPARE_72 28. 4F		
BDO_CLK1* 5. 4D	D	SNN_MI OA_CLKOUT 27. 2C	SNN_NVVDD_MSUR 28.5D	SNN_SPARE_73 28. 4F		
BD1_CLK1 5. 4E	SNN_FBVDDQ_NC1 31.3C	SNN_MI OA_CLKOUT* 27. 2C	SNN_NVVDD_MSUR_GND 28.5D	SNN_SPARE_74 28. 4F		
BD1_CLK1* 5. 4E BD_CMD<22> 5. 4D	SNN_FBVDDQ_SENSE_G 28.5D ND	SNN_MI OA_DE	SNN_NVVDD_OFFSET 32.3F SNN_NVVDD_VR_FAN 32.3F	SNN_STRAP3		
	SNN_FBVDDQ_VREF_I N 31.3B	SNN_MI OA_VREF 27. 2B	SNN_NVVDD_VR_HOT 32.3F	SNN_THERM_LD_STEP1 28.5D		
BD_CMD<30> 5. 4D BD_CMD<31> 5. 4D	SNN_FB_VREFO	SNN_MI OA_VSYNC	SNN_PEX6A_DT* 35. 2A SNN_PEX6B_DT* 35. 3A	SNN_TSENSE_AVDD 29.4B SNN_TSENSE_OVERT 29.5B		
D_CMD<32> 5. 4D	SNN_GPI 02 26. 3D	SNN_MI 0B<1> 27. 3C	SNN_PEX_08 3. 2B	SNN_TSENSE_SEL 29.5B		
8D_DBI 0 28. 2E 8D_DBI 1 28. 2E	SNN_GPI 03 26. 3D   SNN_GPI 08 26. 3D	SNN_MI OB<2> 27. 3C SNN_MI OB<3> 27. 3C	SNN_PEX_10 3. 2A SNN_PEX_11 3. 2A	SNN_TSENSE_VREF		
D_DBI 2 28. 2E	SNN_GPI 010 26. 3D	SNN_MI OB<4> 27. 3C	SNN_PEX_12 3. 2A	SNN_TV_NC5 22. 3G		
D_DBI 3 28. 2E	SNN_GPI 012 26. 3D	SNN_MI OB<5> 27. 3C	SNN_PEX_13 3. 2A	SNN_TV_NC7 22. 3G		
D_DBI 4 28. 2E D_DBI 5 28. 2E	SNN_GPI 013	SNN_MI 0B<6> 27. 3C   SNN_MI 0B<7> 27. 3C	SNN_PEX_14 3. 2A SNN_PEX_15 3. 3A	SNN_VRD11_SELECTED 32.3D   SPDIF_DET 29.2A		
D_DBI 6 28. 2E	SNN_GPU_BUFRST* 3.5F	SNN_MI OB<8> 27. 3C	SNN_PEX_16 3. 3A	SPDI F_GND 29. 1A		
D_DBI 7 28. 2E D_NCO1 11. 2A	SNN_GPU_NC_1 28.1G SNN_GPU_NC_2 28.1G	SNN_MI 0B<9> 27. 3C   SNN_MI 0B<10> 27. 3C	SNN_PEX_17 3.4A SNN_PEX_18 3.4A	SPDI F_I N 29. 1A   SPDI F_I N_GPU 26. 3E< 29. 1D>		
D_NC04 11. 2C	SNN_GPU_NC_3 28. 1G	SNN_MI OB<11> 27. 3C	SNN_PEX_20 3. 2A	SPDIF_IN_TERM_EN 29. 2B		
EO_CLK1 6. 4A EO CLK1* 6. 4A	SNN_GPU_NC_4 28.1G SNN GPU NC 5 28.1G	SNN_MI OB<12> 27. 3C SNN_MI OB<13> 27. 3C	SNN_PEX_TCK	SPDI F_TERM_EN*		
EO_CLK1* 6. 4A E1_CLK1 6. 4B	SNN_GPU_NC_5	SNN_MI 0B<13> 27. 3C SNN_MI 0B<14> 27. 3C	SNN_PEX_IDI	SPDIF_TERM_GND		
E1_CLK1* 6. 4B	SNN_GPU_NC_7 28.1G	SNN_MI OB_CAL_PD_VD 27. 3B	SNN_PEX_TMS 3.1B	STRAP1 26. 3B		
E_CMD<22> 6.4A E_CMD<29> 6.4A	SNN_GPU_NC_8 28. 2G SNN_GPU_NC_9 28. 2G	DQ SNN_MI OB_CAL_PU_GN 27. 3B	SNN_PEX_TRST* 3.1B SNN_PS4_NVVDD_OVP 32.2D	STRAP2 26. 3B THERM_6649_VCC 29. 2E		
E_CMD<30> 6.4A	SNN_GPU_NC_10 28. 2G	D	SNN_SPARE_01 28.1F	THERM_ADDR* 29. 5E		
E_CMD<31> 6.4A E_CMD<32> 6.4A	SNN_GPU_NC_11 28. 2G SNN_GPU_NC_12 28. 2G	SNN_MI OB_CLKOUT	SNN_SPARE_02 28.1F SNN_SPARE_03 28.1F	THERM_ALERT* 29. 5E   THERM_DN 29. 5D		
_DBI 0 28. 2E	SNN_GPU_NC_13 28. 2G	SNN_MI OB_DE 27. 3C	SNN_SPARE_04 28.1F	THERM_DP 29. 5D		
_DBI 1 28. 3E	SNN_GPU_NC_14 28. 2G	SNN_MI OB_HSYNC 27.3C	SNN_SPARE_05 28.1F	THERM_SHDN* 29. 4E		
_DBI 2 28. 3E _DBI 3 28. 3E	SNN_GPU_NC_15 28. 2G SNN_GPU_NC_16 28. 2G	SNN_MI OB_VREF	SNN_SPARE_06 28.1F SNN_SPARE_07 28.1F	THERM_SHUTDOWN* 29. 3H> 30. 4A< 32. 2B		
_DBI 4 28. 3E	SNN_GPU_NC_17 28. 2G	SNN_NVI O_EXTDEV_RS 26. 4D	SNN_SPARE_08 28. 2F	XTAL_BUFCLK_OUT 19. 4E		
E_DBI 5 28. 3E E_DBI 6 28. 3E	SNN_GPU_NC_18 28. 2G SNN_GPU_NC_19 28. 2G	T* SNN_NVI 0_NC_01 28. 4G	SNN_SPARE_09 28.2F SNN_SPARE_10 28.2F	XTAL_I N 26. 4C XTAL_OUT 26. 4C		
E_DBI 7 28. 3E	SNN_GPU_NC_20 28. 2G	SNN_NVI 0_NC_02 28. 4G	SNN_SPARE_11 28. 2F	20.70		
E_NC01 12. 2A	SNN_GPU_NC_21 28. 2G	SNN_NVI 0_NC_03 28. 4G	SNN_SPARE_12 28.2F			
E_NCO4 12. 2C FO_CLK1 6. 4D	SNN_GPU_NC_22 28. 2G SNN_GPU_NC_23 28. 2G	SNN_NVI 0_NC_04 28. 4G SNN_NVI 0_NC_05 28. 4G	SNN_SPARE_13 28. 2F SNN_SPARE_14 28. 2F			
FO_CLK1* 6. 4D	SNN_GPU_NC_24 28. 2G	SNN_NVI 0_NC_06 28. 4G	SNN_SPARE_15 28. 2F			
F1_CLK1 6. 4E F1_CLK1* 6. 4E	SNN_GPU_NC_25 28. 2G SNN_GPU_NC_26 28. 2G	SNN_NVI 0_NC_07	SNN_SPARE_16 28.2F SNN_SPARE_17 28.2F			
F_CMD<22> 6.4D	SNN_GPU_NC_27 28. 2G	SNN_NVI 0_NC_09 28. 4G	SNN_SPARE_18 28. 2F			
F_CMD<29> 6.4D F_CMD<30> 6.4D	SNN_GPU_NC_28	SNN_NVI 0_NC_10 28. 4G SNN_NVI 0_NC_11 28. 4G	SNN_SPARE_19 28. 2F SNN_SPARE_20 28. 2F			
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