電子類元件 零件承認書文件 CHECK LIST

零件廠商：UPI **品名規格：PWM uP1965PDD8 UPI**

技嘉料號：10TA1-601965-01R

項次	文件項目
Data Sheet 檢核項目	
1	DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2**
8	零件樣品 20PCS(Chipset 等高單價，至少 1PCS)
9	**電子零件承認基本調查表。註 3**
10	以上資料電子檔為 PDF 檔，且是同 1 個 File
GSCM 綠色產品管理系統-物料管制文件檢核清單	
物料管制文件 1	GSCM 綠色產品管理系統：零件照片
物料管制文件 2	GSCM 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4**
物料管制文件 3	GSCM 綠色產品管理系統：Data Sheet
GSCM 綠色產品管理系統-MCD 表格	
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
其他文件 (僅適用電阻、電容類之系列元件)	
附件 1	危害物質測試報告 Test Report of Hazardous Substances。**註 5**
附件 2	元件調查表 Component Composition Table

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等

※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)

2.1. 基本需符合 JEDEC 規範

2.2. Ambient Temp. (Reflow Temp endurace): >225℃, 70 sec. 零件塑膠材質需 PA9T(含)等級以上

2.3. PASTE IN HOLE 零件塑膠材質需 PA9T(含)等級以上

※ **3. 電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G*,11T***

非 IC 類：10C*,11C*,10L*,11L*,10X*,11X*,10R*,11B*

※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”

※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

電子零件承認基本調查表

一、原物料規格/來源

項次	部位名稱/規格	材質	原物料來源產地
1	CHIP	金屬	Taiwan
2	DIE ATTACH	EPOXY	Japan
3	LEAD FRAME	金屬	Japan
4	BONDING WIRE	金屬	Korea
5	MOLDING COMPOUND	EPOXY	Taiwan
6	PLATING	鍍錫	Taiwan

二、晶圓廠(非 IC 類免填)

項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	Maxchip Electronics Corp	TW	8	80	外包

三、封裝廠(IC 類)；成品之生產製造工廠(非 IC 類)

項次	工廠名稱	生產產地	投產比率(%)	自有/外包
1	GTK(超豐電子)	TW	85	外包
2	TongFu Microelectronics Co.,Ltd.	Nantong	15	外包
3				

四、產能

總產能(月/PCS)	可供技嘉產能(月/PCS)
NA	NA

※ 1. IC 類之晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 2. 非 IC 類零件之成品生產製造工廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 3. 以上資訊欄位若有不足，可自行增加行數

5V MOSFET Driver with Output Disable for Single Phase Synchronous-Rectified Buck Converter

General Description

The uP1965 is 5V MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous rectified buck converter for mobile computing application. This part has integrated bootstrap diode to eliminate external component count. The resistor commonly placed between MOSFET gate and source for discharge is also integrated, making external component minimal. This device combined with uPI multi-phase buck PWM controller forms a complete core voltage regulator for advanced microprocessors.

The uP1965 supports enable/disable function that reduces the power consumption to prolong battery life. Both gate drives are turned off by pulling low EN pin or high-impedance at PWM pin, preventing rapid output capacitor discharge during system shutdown. This device also supports three PWM input states that along with PWM controller to provide a complete power solution.

The uP1965 implements anti-shoot-through protection that prevents cross-conduction of the external MOSFET while maintains minimum deadtime for optimized efficiency. This device also supports supply input under voltage lockout. The uP1965 is available in thermally enhanced WDFN3x3-8L and WDFN2x2-8L packages.

Ordering Information

Order Number	Package	Remark
uP1965PDD8	WDFN3x3 - 8L	
uP1965QDN8	WDFN2x2 - 8L	

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

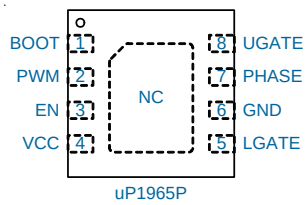
Features

- **Single 5V Driving Voltage Output**
- **Integrated Bootstrap Diode**
- **Integrated Gate-to-Source Discharge Resistors**
- **Enable/Disable Control**
- **Allow PWM Pin as Multi-Function Setting Application**
- **Three PWM Input States: High, Low and Tri-State**
- **Tri-State Input for Bridge Shutdown**
- **Anti-Shoot-Through Protection Circuitry**
- **Under Voltage Lockout for Supply Input**
- **WDFN3x3-8L and WDFN2x2-8L Packages**
- **RoHS Compliant and Halogen Free**

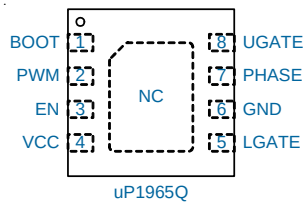
Applications

- **Desktop/Laptop CPU/GPU Core Voltage Regulators**
- **High Frequency Low Profile DC/DC Converter**
- **High Current Low Voltage DC/DC Converter**

Pin Configuration

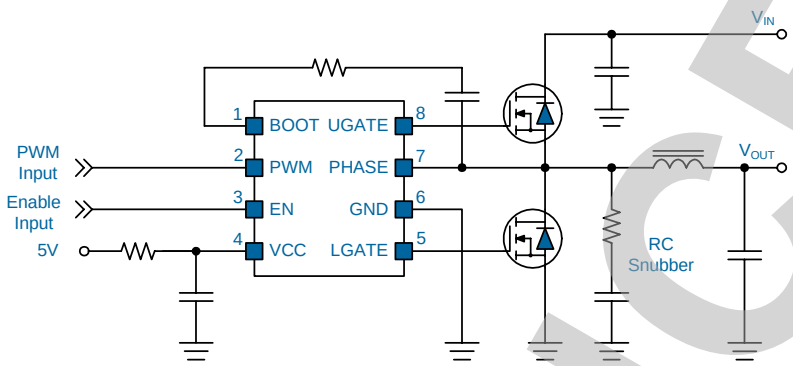


uP1965P

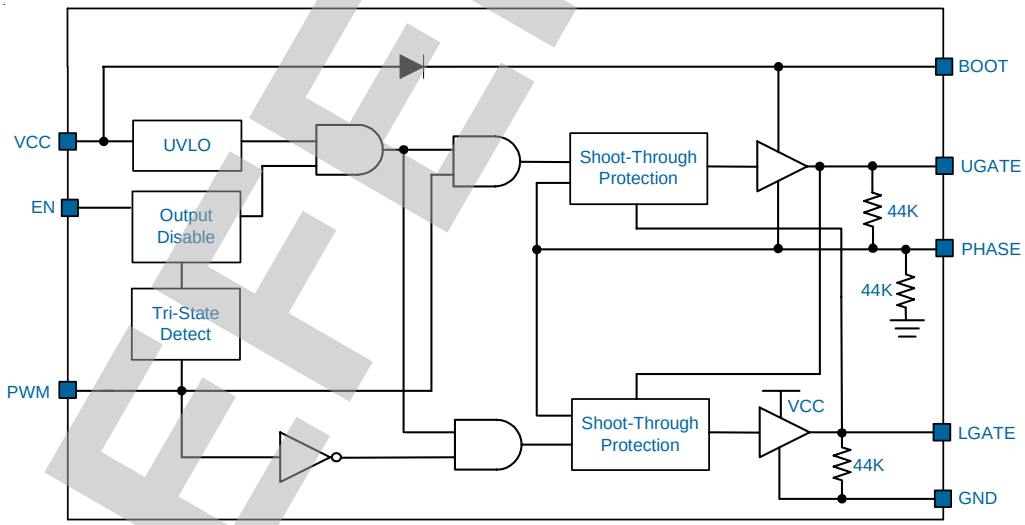


uP1965Q

Typical Application Circuit



Functional Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	**Bootstrap Supply.** For the floating upper gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Make sure that C_{BOOT} is placed near the IC.
2	PWM	**PWM Input.** This pin receives logic level input and controls the driver outputs. The PWM pin is in high input impedance state if EN input is low. When EN input is high, the PWM pin voltage will be pulled to tri-state by internal circuit. The resistor connected from PWM pin to GND for PWM controller function setting must be greater than 15kΩ.
3	EN	**Enable Control.** This pin disables normal operation and forces both UGATE and LGATE off when it is pulled low. This pin also controls the state of PWM pin. When the EN pin is pulled low, the PWM pin is in high-input impedance state. There is no internal pull-up or pull-low mechanism to this pin.
4	VCC	**Supply Voltage for the IC.** This pin provides bias voltage for the IC. Connect this pin to 5V voltage source and bypass it with an R/C filter.
5	LGATE	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when the lower MOSFET has been turned off.
6	GND	**Ground for the IC.** All voltage levels are measured with respect to this pin.
7	PHASE	**PHASE Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the return path for the UGATE driver. This pin is also monitored by the shoot-through protection circuitry to determine when the upper MOSFET has been turned off.
8	UGATE	**Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when the upper MOSFET has been turned off.
Exposed Pad	NC	**Not Internally Connected.** Although the exposed pad of uP1965P/Q is not electrically connected to GND. It is still highly recommended to connect the exposed pad to GND plane for maximum heat dissipation.

Functional Description

Enable Control

The EN pin controls PWM pin state and the MOSFET gate driver output state. Logic input low to EN pin disables the gate drivers. Both UGATE and LGATE will be kept low, and PWM pin will be in high input impedance state. Logic input high to EN pin enables the gate drivers after a delay time T_{PDHDEN} as shown in Figure 1. During this time period the PWM pin stays at high input impedance state, both UGATE and LGATE outputs are kept low, and the internal control circuit does not respond to the PWM input voltage. After T_{PDHDEN} expires, both UGATE and LGATE begin to respond to the PWM input. This mechanism is specifically designed for uPI's PWM controller, which uses its PWM pin as a multi-functional pin.

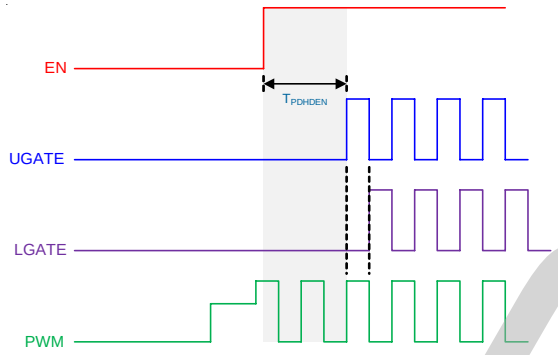


Figure 1. Enable Control, EN

PWM Input

The PWM pin is a tri-state input. Logic high turns on the high-side gate driver and turns off the low-side gate driver once the POR of VCC is granted and EN is kept high. Logic low turns off the high-side gate driver and turns on the low-side gate driver. High impedance input at PWM pin will keep both high-side and low-side gate drivers low and turns off both MOSFETs. The PWM pin voltage is kept around 1.6V by internal bias circuit when floating.

Refer to Figure 1, during T_{PDHDEN}, both UGATE and LGATE are kept low, the PWM pin is in high-input impedance state, and the PWM input will be ignored. For the PWM controller uses its PWM pin as a multi-functional pin, a resistor will be connected from PWM pin to GND to set parameter. Note that this resistor must be greater than 15kΩ. Lower resistor value will cause incorrect PWM voltage level at the PWM pin when the PWM controller output is in tri-state (high-impedance state).

Low-Side Driver

The low-side driver is designed to drive a ground referenced N-channel MOSFET. The bias to the low-side driver is internally connected to VCC supply and GND. The low-side driver output is out of phase with the PWM input when it is enabled. The low side driver is held low if the EN pin is pulled low or high-impedance at PWM pin.

High-Side Driver

The high-side driver is designed to drive a floating N-channel MOSFET. The bias voltage to the high-side driver is internally connected to BOOT and PHASE pins. An integrated bootstrap switch that is connected between BOOT and VCC pins provides the bias current for the high side gate driver.

The bootstrap capacitor C_{BOOT} is charged to V_{CC} when PHASE pin is grounded by turning on the low-side MOSFET. The PHASE rises to V_{IN} when the high-side MOSFET is turned on, forcing the BOOT pin voltage to V_{IN} + V_{CC} that provides voltage to hold the high-side MOSFET on.

The high-side gate driver output is in phase with the PWM input when it is enabled. The high-side driver is held low if the EN pin is pulled low or high-impedance at PWM pin.

Shoot Through Protection

The shoot-through circuit prevents the high-side and low-side MOSFETs from being turned on simultaneously and conducting destructive large current. It is done by turning on one MOSFET only after the other MOSFET is off already with adequate delay time.

At the high-side off edge, UGATE and PHASE voltages are monitored for anti-shoot-through protection. The low-side driver will not begin to output high until both (V_{UGATE} - V_{PHASE}) and V_{PHASE} are lower than 1.2V, making sure the high-side MOSFET is turned off completely.

At the low-side off edge, LGATE voltage is monitored for anti-shoot-through protection. The high-side driver will not begin to output high until V_{LGATE} is lower than 1.2V, making sure the low-side MOSFET is turned off completely.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC ---------- -0.3V to +6V
BOOT to PHASE ---------- -0.3V to +6V
PHASE to GND
- DC ---------- -0.7V to +30V
- < 200ns ---------- -8V to +36V

BOOT to GND
- DC ---------- -0.3V to (VCC +36V)
- < 200ns ---------- -0.3V to +42V

UGATE to PHASE
- DC ---------- -0.3V to (BOOT - PHASE +0.3V)
- < 200ns ---------- -5V to (BOOT - PHASE +0.3V)

LGATE to GND
- DC ---------- -0.3V to (VCC +0.3V)
- < 200ns ---------- -5V to (VCC +0.3V)

PWM ---------- -0.3V to +6V
EN ---------- -0.3V to (VCC +0.3V)
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- WDFN2x2 - 8L θ_{JA} ---------- 155°C/W
- WDFN2x2 - 8L θ_{JC} ---------- 20°C/W
- WDFN3x3 - 8L θ_{JA} ---------- 68°C/W
- WDFN3x3 - 8L θ_{JC} ---------- 6°C/W

Power Dissipation, P_D @ T_A = 25°C
- WDFN2x2 - 8L ---------- 0.65W
- WDFN3x3 - 8L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- 10.8V to 13.2V
Power Stage Input Voltage, V_{IN} ---------- +4.5V to 28V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

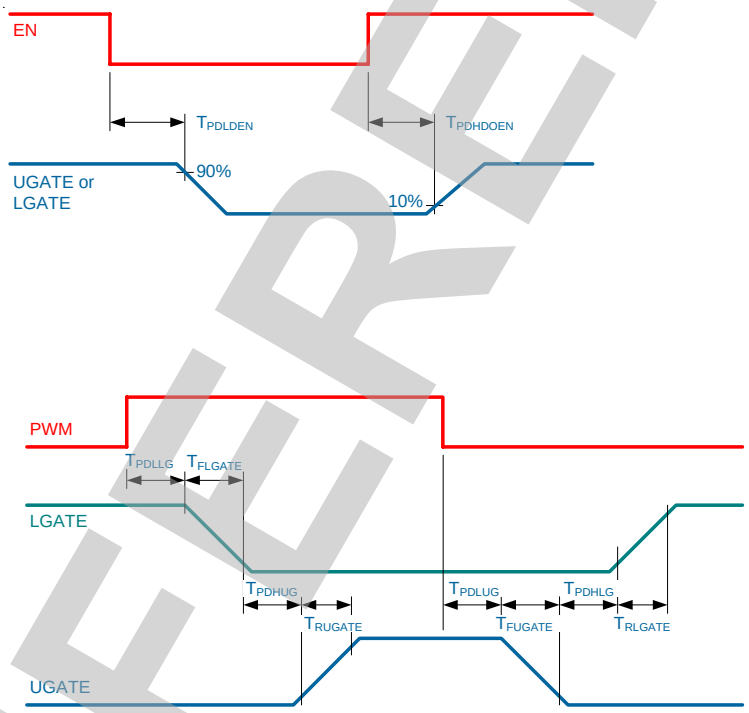
Electrical Characteristics

(VCC = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Current	I_{CC}	EN = 0V	--	10	20	uA
VCC POR Rising Threshold	V_{CCRTH}	V_{CC} Rising	3.8	4.0	4.4	V
VCC POR Hysteresis	V_{CCHYS}		--	0.2	--	V
PWM Input						
Input High Level	PWM_H		2.9	--	--	V
Input Low Level	PWM_L		--	--	0.4	V
PWM Floating Voltage	PWM_{FLT}		--	1.6	--	V
PWM Input Current	I_{PWM}	PWM = 0V	-520	-300	-200	uA
		PWM = 3.3V	0.5	1	1.6	mA
		PWM = 5V	1	2	2.6	mA
Tris-State Shutdown Hold-Off Time			70	130	220	ns
Enable Control						
Input High	EN_H		2	--	--	V
Input Low	EN_L		--	--	0.6	V
Propagation Delay Time	T_{PDHDEN}		1	6	10	us
	T_{PDLDEN}		--	--	600	ns
Bootstrap Diode						
Forward Voltage			--	0.33	--	V
High Side Driver						
Output Resistance, Sourcing	R_{H_SRC}	V_{BOOT} - V_{PHASE} = 5V, I_{UGATE} = -80mA	--	0.7	1.4	Ω
Output Resistance, Sinking	R_{H_SNK}	V_{BOOT} - V_{PHASE} = 5V, I_{UGATE} = -80mA	--	0.4	0.8	Ω
Output Rising Time	T_{RUGATE}	V_{BOOT} - V_{PHASE} = 5V, C_{LOAD} = 3nF	--	20	--	ns
Output Falling Time	T_{FUGATE}	V_{BOOT} - V_{PHASE} = 5V, C_{LOAD} = 3nF	--	10	--	ns
Propagation Delay Time	T_{PDHUG}	V_{BOOT} - V_{PHASE} = 5V	--	30	45	ns
	T_{PDLUG}	V_{BOOT} - V_{PHASE} = 5V	--	20	30	ns

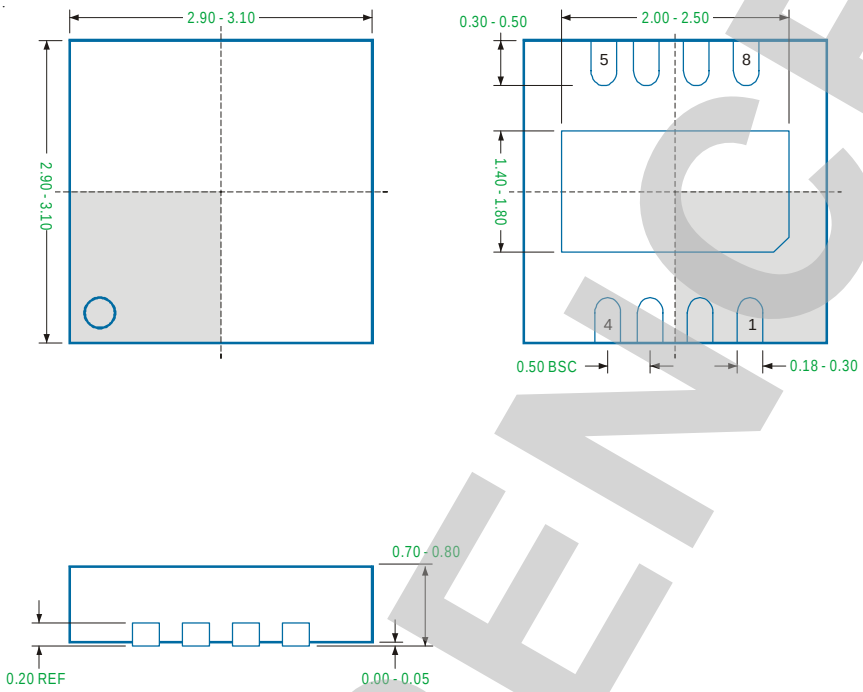
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low Side Driver						
Output Resistance, Sourcing	R_{L_SRC}	V_{CC} = 5V, I_{LGATE} = -80mA	--	0.7	1.4	Ω
Output Resistance, Sinking	R_{L_SNK}	V_{CC} = 5V, I_{LGATE} = -80mA	--	0.3	0.7	Ω
Output Rising Time	T_{RLGATE}	V_{CC} = 5V, C_{LOAD} = 3nF	--	20	--	ns
Output Falling Time	T_{FLGATE}	V_{CC} = 5V, C_{LOAD} = 3nF	--	10	--	ns
Propagation Delay Time	T_{PDHLG}	V_{CC} = 5V	--	30	45	ns
	T_{PDLLG}	V_{CC} = 5V	--	20	30	ns



Package Information

WDFN3x3 - 8L

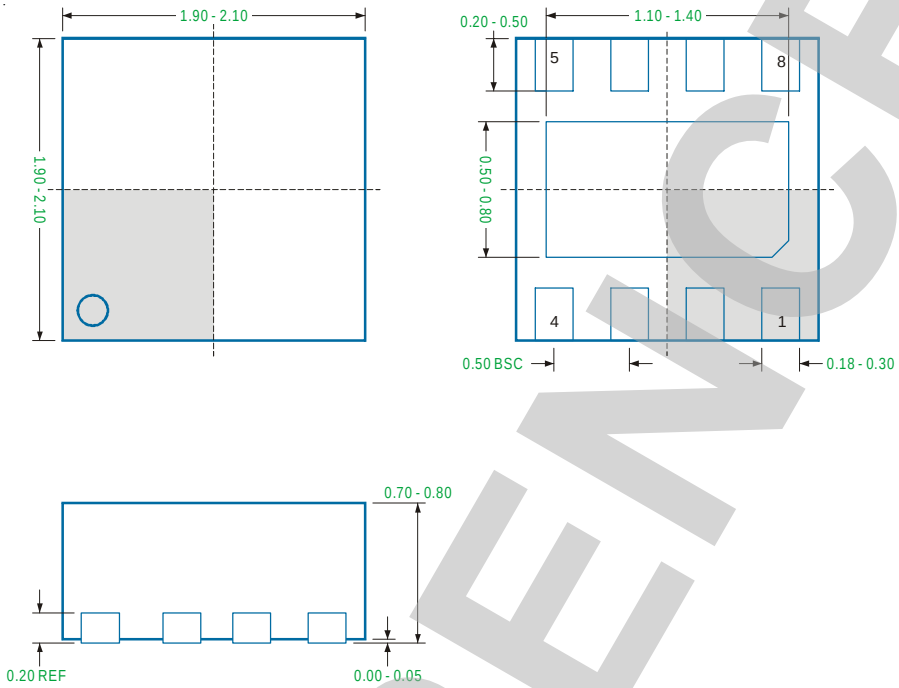


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

WDFN2x2 - 8L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

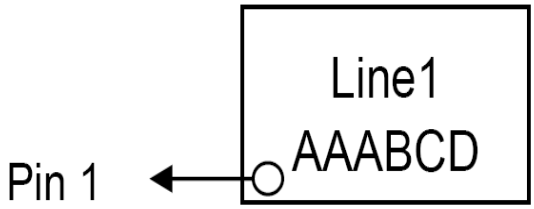
uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the taerms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use or application of any product or circuit; nor for any infringements of patents or other rights of third parties which may result from its use or application, including but not limited to any consequential or incidental damages. No uPI components are designed, intended or authorized for use in military, aerospace, automotive applications nor in systems for surgical implantation or life-sustaining. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

uPI Semiconductor Corp.
Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064

Top Marking Rule



Line 1 : Product Code

Part No.	Product Code
UP1965PDD8	uP1965P

Line 2 :
AAA - uPI internal trace code
BCD - Date Code, rules as below:

B：Last one of western calendar year (0~9), ex. 2007=7, 2008=8

C：Month

Month	Code	Month	Code	Month	Code	Month	Code
Jan	1	Apr	4	Jul	7	Oct	A
Feb	2	May	5	Aug	8	Nov	B
Mar	3	Jun	6	Sep	9	Dec	C

D：Date

Date	Code	Date	Code	Date	Code	Date	Code
1	1	9	9	17	H	25	S
2	2	10	A	18	J	26	T
3	3	11	B	19	K	27	U
4	4	12	C	20	L	28	V
5	5	13	D	21	M	29	W
6	6	14	E	22	N	30	X
7	7	15	F	23	P	31	Y
8	8	16	G	24	R		

WDFN3x3 Package

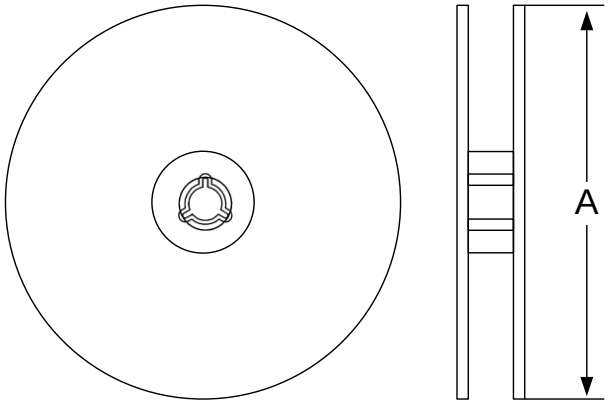
Definition:

DFN = Dual Flat No Lead

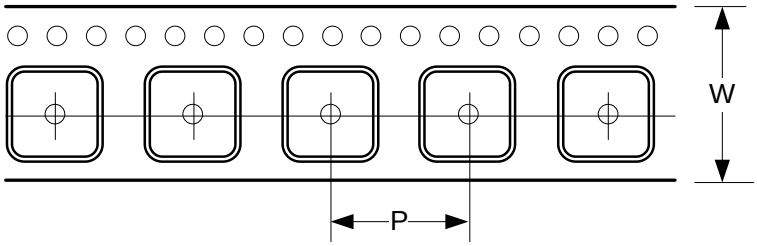
W Type= Very Very Thin Package(Thickness = 0.75 ± 0.05mm)

Tape & Reel Drawing

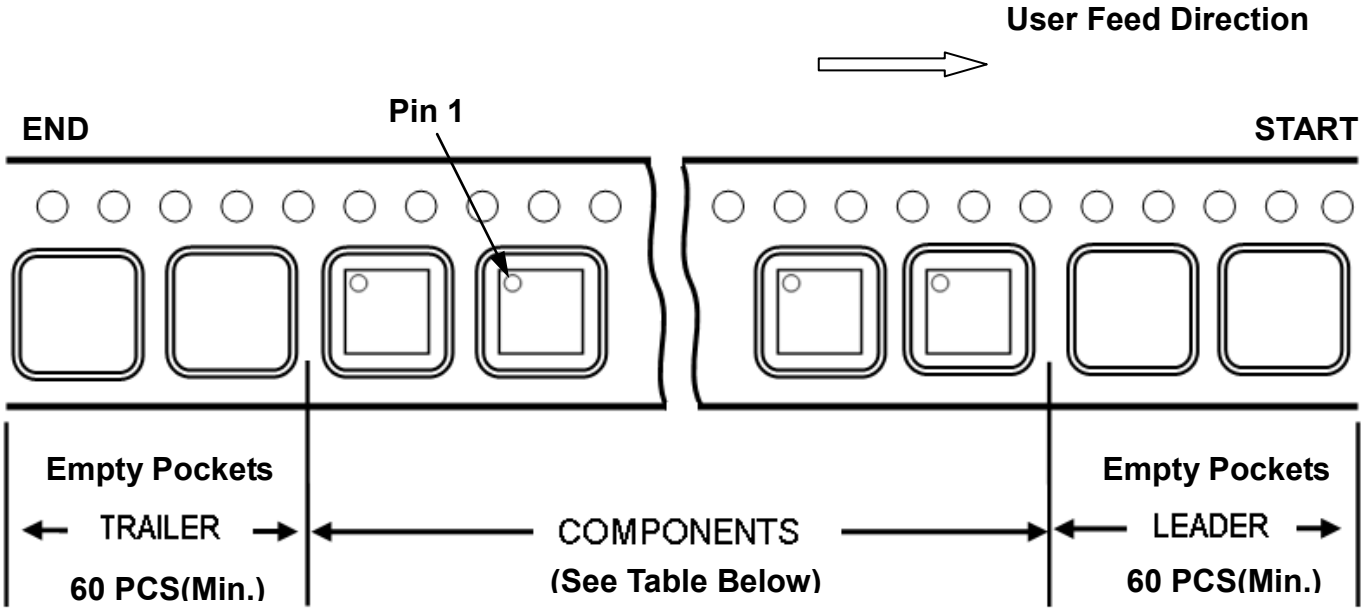
Lock Reel



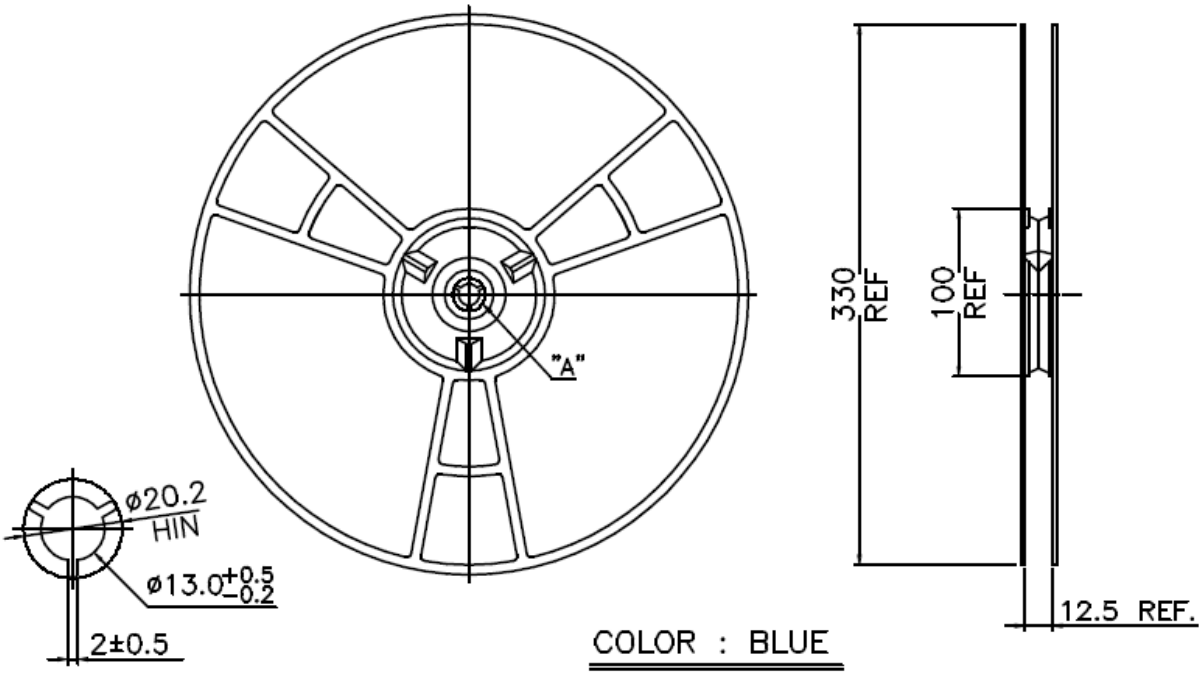
Carrier Tape

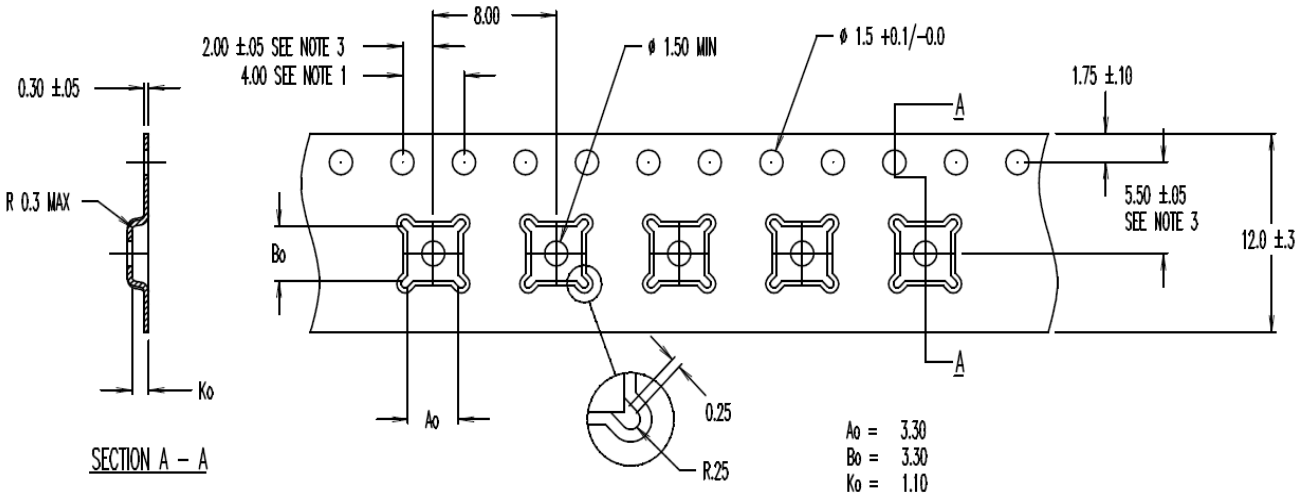


Packing Illustration



Carrier Tape Drawing





Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Cover Tape width 9.3±0.1mm.

Packing Quantity List

PKG Type Body Size	Reel Diameter(A) (inch/mm)	Carrier Width(W) (mm)	Carrier Pitch(P) (mm)	Reel Quantity (pcs)	Remark
WDFN 3x3	13 / 330	12	8	2500	

Packaging Drawing

Barcode Label – Apply for Reel/Al Bag/Inner Box and Outer Carton

P/N：uPI Part Number

LOT：Wafer Lot Number

QTY：Packing Quantity

D/C：Manufacturing Date Code

DATE：Packing Date

Note：For Internal Use Only

Inner Box

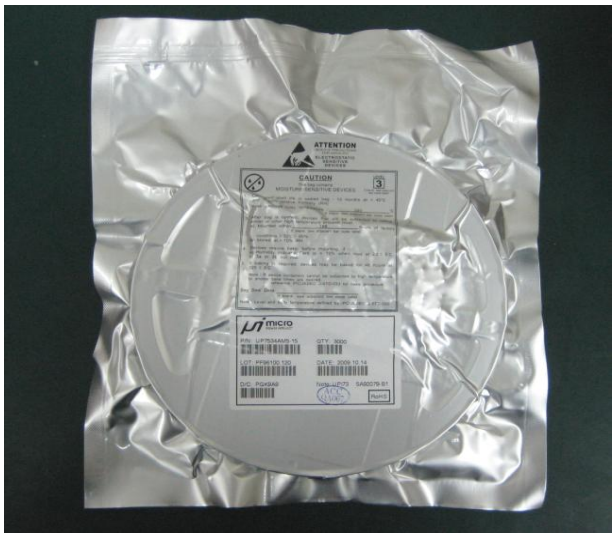
Box (13” Reel 355 x338 x 50 mm)

Outer Carton

Carton A (382 x 283 x390 mm)

Package Storage Condition:

- Vacuum Sealed into Moisture Barrier Bag and Meet MSL Level 3 requests.
- Comply with J-STD-033 standard.



- Storage Condition

  Vacuum Sealed : 12 months at <40℃ and 90%RH

  Bag Opened : Within 168 hrs at < 30℃ / 60%RH

- Baking Condition

  Re-Backing @ 125℃ +/- 5 ℃, 9hrs for IC only;

  Floor life begins counting at time =0 after Re-Backing.

  The times of Re-Backing: 2 times, Max.

Halogen-Free Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 -2000	Volume mm^3 > 2000
< 1.6 mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6 mm - 2.5 mm	260 +0 °C	250 +0 °C	245 +0 °C
≧ 2.5 mm	250 +0 °C	245 +0 °C	245 +0 °C

IR Reflow Profile

Profile Feature	Halogen-Free Assembly
Average Ramp-uP Rate (TS_{max} to Tp)	3 °C/second max.
Preheat - Temperature Min (TS_{min}) - Temperature Max (TS_{max}) - Time (TS_{min} to TS_{max})	 150 °C 200 °C 60-180 Seconds
Time Maintained above - Temperature (TL) - Time (tL)	 217 °C 60-150 Seconds
Peak/Classification Temperature (Tp)	<=260 °C
Time Within 5 °C of actual Peak Temperature (tp)	20-40 seconds
Ramp-Down Rate	6 °C/second max.
Time 25 °C to Peak Temperature	8 minutes max.