

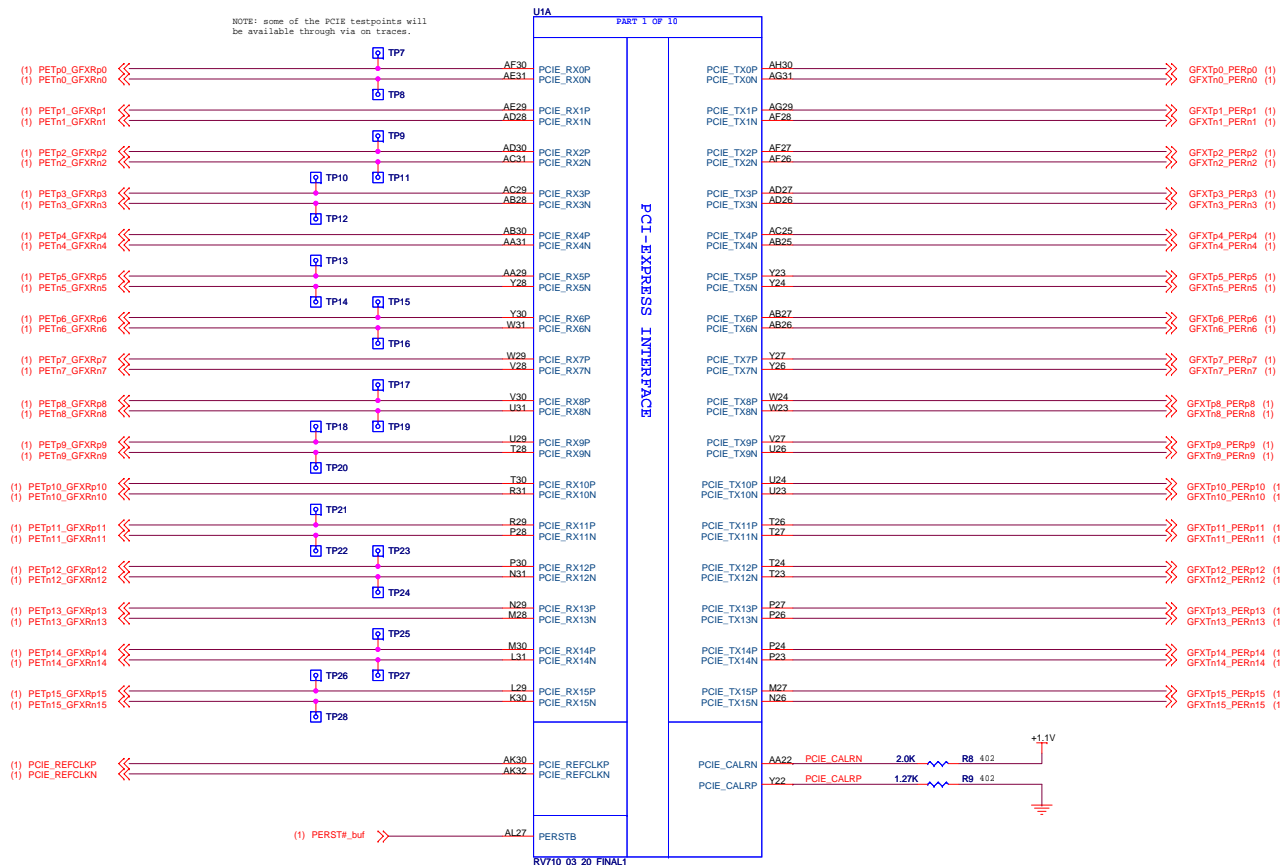
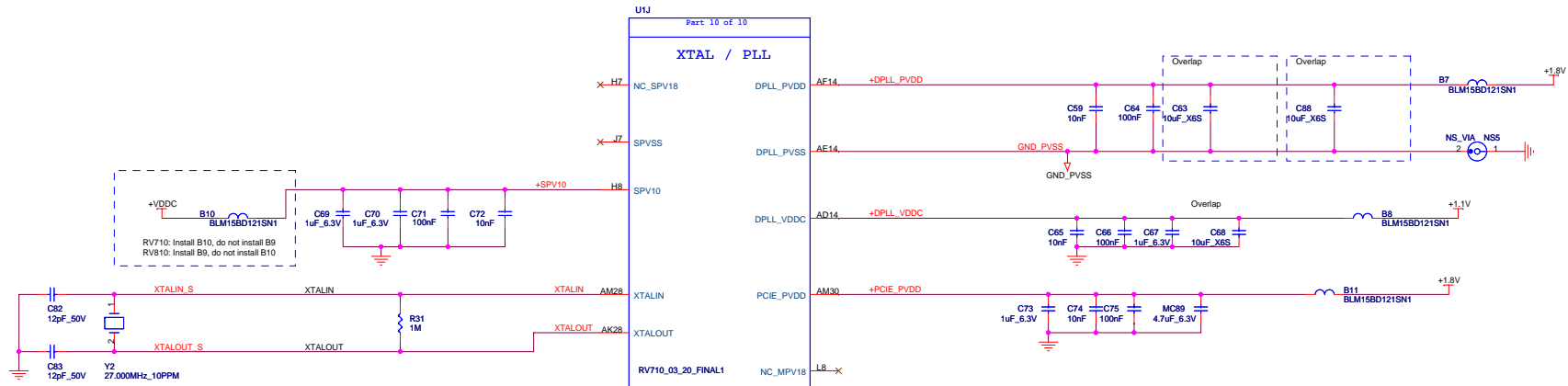


| SYMBOL LEGEND   |                |
|---|----------------|
| DNI   | DO NOT INSTALL |
| #   | ACTIVE LOW     |
|  | DIGITAL GROUND |
|  | ANALOG GROUND  |





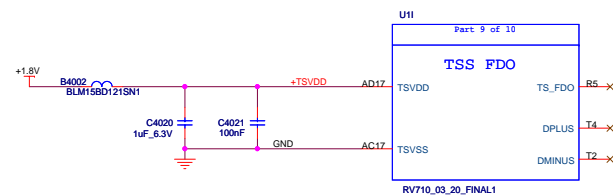
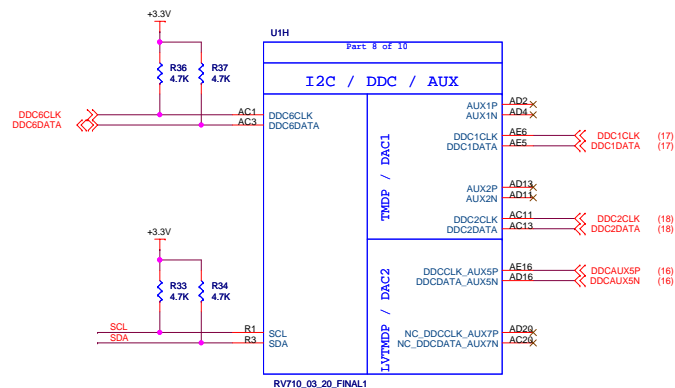


DDC6 BUS:

| I2C Address | Function                           | Device |
|-------------|------------------------------------|--------|
| 0x90        | I2C VDDC Control                   | DS4402 |
| 0x98        | LM63 - External Temperature Sensor | LM63   |

SCL / SDA BUS:

| I2C Address | Function | Device |
|-------------|----------|--------|
| N/A         | N/A      | N/A    |



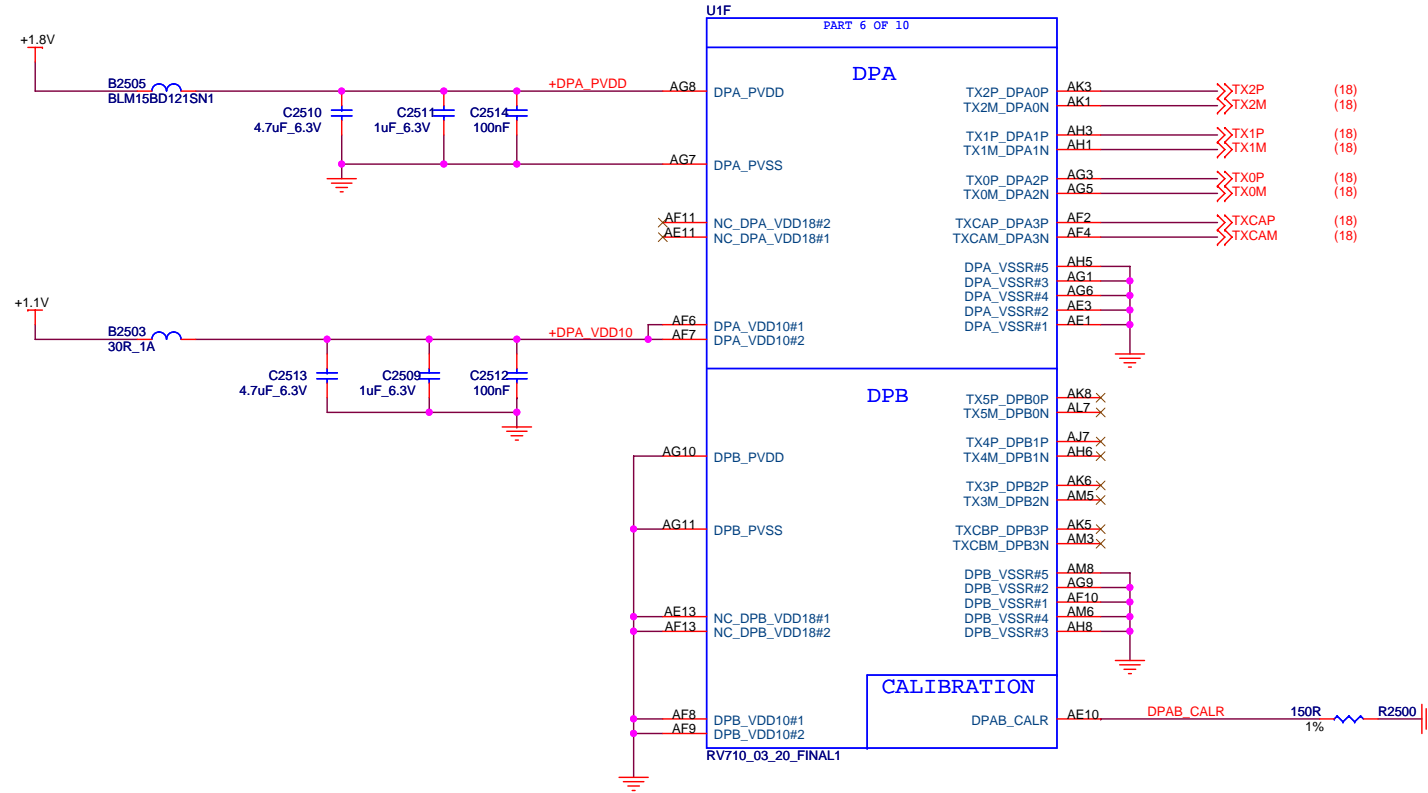
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Sheet 4 of 22

Title RH LP RV710 DDR2 VGA (header) TVO DVI Doc No. 105-B750XX-00A

# TMDP INTERFACE



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Title RH LP RV710 DDR2 VGA (header) TVO DVI

**LVTMDP INTERFACE**

The diagram illustrates the LVTMDP interface for the RV710 GPU. It shows the connection of the GPU's DPF and DPE blocks to various power and signal pins. Power planes are shown for +1.8V and +1.1V, with decoupling capacitors (C1500-C1508) and inductors (B1500, B1501, B1502). Signal pins are connected to the GPU's DPF and DPE blocks, which are then connected to the board's pins (AK24, AL23, AH22, etc.). A calibration section shows the connection of the DPEF\_CALR pin to a 150R resistor and a 1% tolerance resistor R1500.

**Power and Signal Connections:**

- +1.8V:** B1500, BLM15BD121SN1, C1500 (4.7uF\_6.3V), C1501 (1uF\_6.3V), C1509 (1uF\_6.3V), C1502 (100nF).
- +1.8V:** B1501, BLM15BD121SN1, C1503 (4.7uF\_6.3V), C1504 (1uF\_6.3V), C1510 (1uF\_6.3V), C1508 (100nF).
- +1.1V:** B1502, 30R 1A, C1506 (4.7uF\_6.3V), C1507 (1uF\_6.3V), C1511 (1uF\_6.3V), C1508 (100nF).

**GPU Blocks and Pins:**

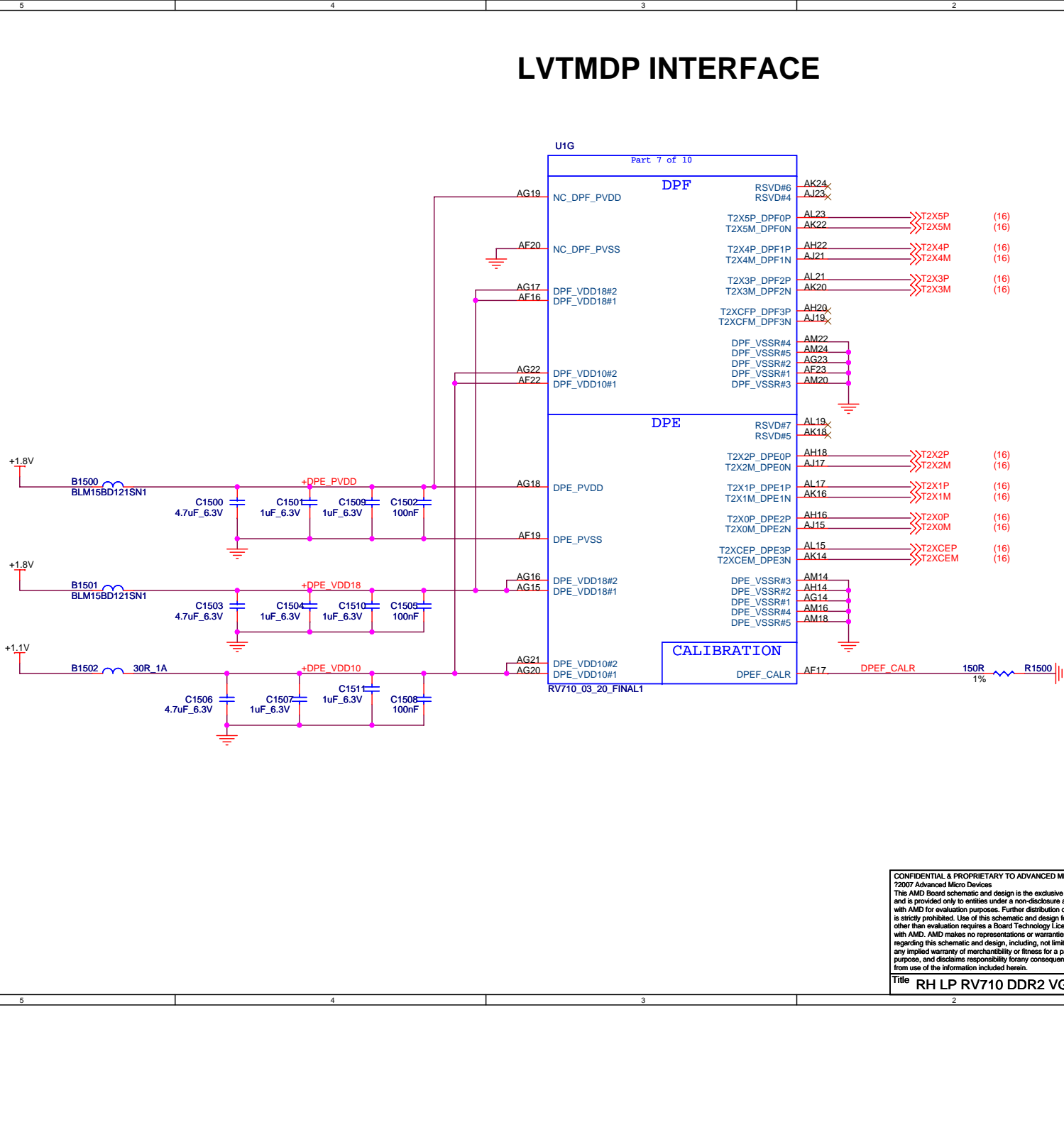
- DPF:** NC\_DPF\_PVDD (AG19), NC\_DPF\_PVSS (AF20), DPF\_VDD18#2 (AG17), DPF\_VDD18#1 (AF16), DPF\_VDD10#2 (AG22), DPF\_VDD10#1 (AF22), DPE\_VDD (AG18), DPE\_PVSS (AF19), DPE\_VDD18#2 (AG16), DPE\_VDD18#1 (AG15), DPE\_VDD10#2 (AG21), DPE\_VDD10#1 (AG20).
- DPE:** RSVD#7, RSVD#5, T2X2P\_DPE0P, T2X2M\_DPE0N, T2X1P\_DPE1P, T2X1M\_DPE1N, T2X0P\_DPE2P, T2X0M\_DPE2N, T2XCEP\_DPE3P, T2XCEM\_DPE3N, DPE\_VSSR#3, DPE\_VSSR#2, DPE\_VSSR#1, DPE\_VSSR#4, DPE\_VSSR#5.
- CALIBRATION:** DPEF\_CALR (AF17).

**Board Pins and Connections:**

- AK24, AJ23, AL23, AK22, AH22, AJ21, AL21, AK20, AH20, AJ19, AM22, AM24, AG23, AF23, AM20, AL19, AK18, AH18, AJ17, AL17, AK16, AH16, AJ15, AL15, AK14, AM14, AH14, AG14, AM16, AM18, AF17.
- T2X5P, T2X5M, T2X4P, T2X4M, T2X3P, T2X3M, T2X2P, T2X2M, T2X1P, T2X1M, T2X0P, T2X0M, T2XCEP, T2XCEM.

**Resistors and Capacitors:**

- Resistors: B1500, B1501, B1502, 30R 1A, 150R, R1500 (1%).
- Capacitors: C1500, C1501, C1502, C1503, C1504, C1506, C1507, C1508, C1509, C1510, C1511.



|  |                              |       |  |
|--|------------------------------|-------|--|
|  |                              | 2     |  |
|  |                              |       |  |
| >>T2X5P  | (16)                         |       |  |
| >>T2X5M  | (16)                         |       |  |
| >>T2X4P  | (16)                         |       |  |
| >>T2X4M  | (16)                         |       |  |
| >>T2X3P  | (16)                         |       |  |
| >>T2X3M  | (16)                         |       |  |
|  |                              |       |  |
| >>T2X2P  | (16)                         |       |  |
| >>T2X2M  | (16)                         |       |  |
| >>T2X1P  | (16)                         |       |  |
| >>T2X1M  | (16)                         |       |  |
| >>T2X0P  | (16)                         |       |  |
| >>T2X0M  | (16)                         |       |  |
| >>T2XCPE   | (16)                         |       |  |
| >>T2XCEM   | (16)                         |       |  |
|  |                              |       |  |
| F CALR   | 150R<br>1%                   | R1500 |  |
|  |                              |       |  |
|  |                              |       |  |
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|  | 2                            |       |  |

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| Sheet       | 6 of 22   |
| er) TVO DVI |   |

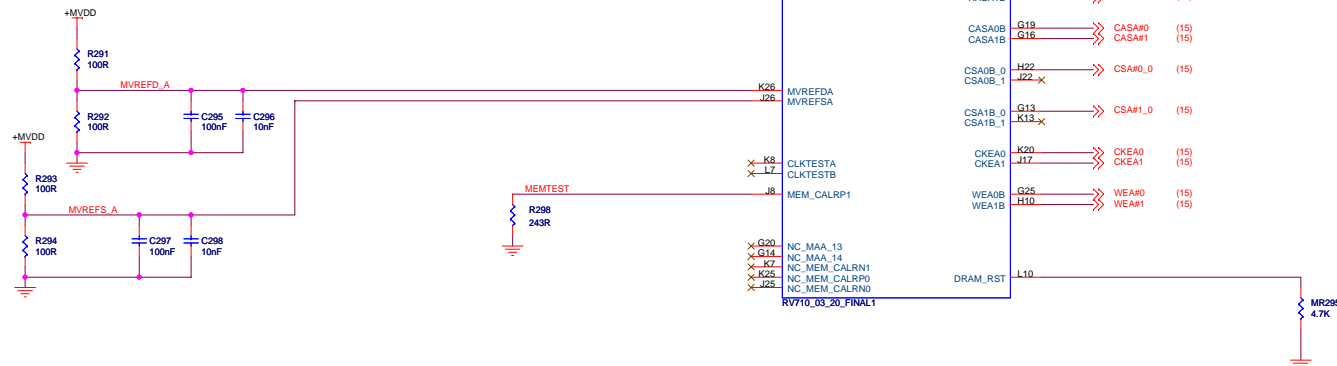
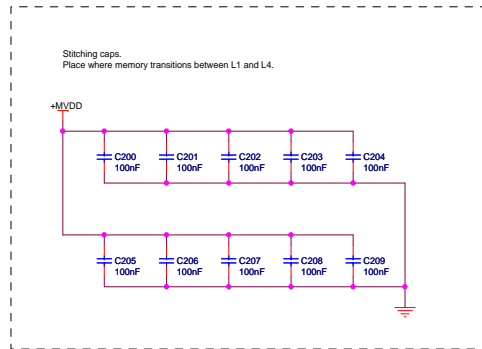


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| er) TVO DVI   | Doc No. 105-B750XX-00A |
| 1   |                        |

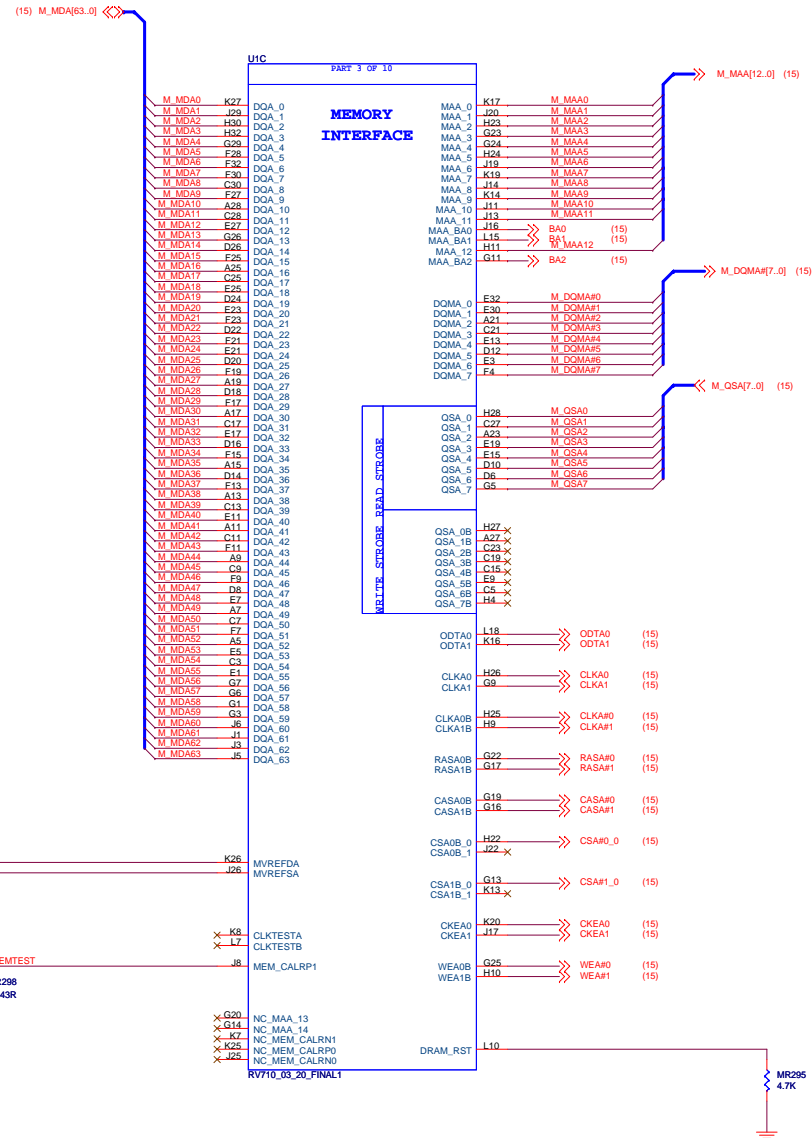
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| Title RH LP RV710 DDR2 VGA (header) TVO DVI      | Doc No. 105-B750XX-00A |

## MEMORY INTERFACE



|                   |      |
|-------------------|------|
| DIVIDER RESISTORS | DDR2 |
| MVREF TO 1.8V     | 100R |
| MVREF TO GND      | 100R |

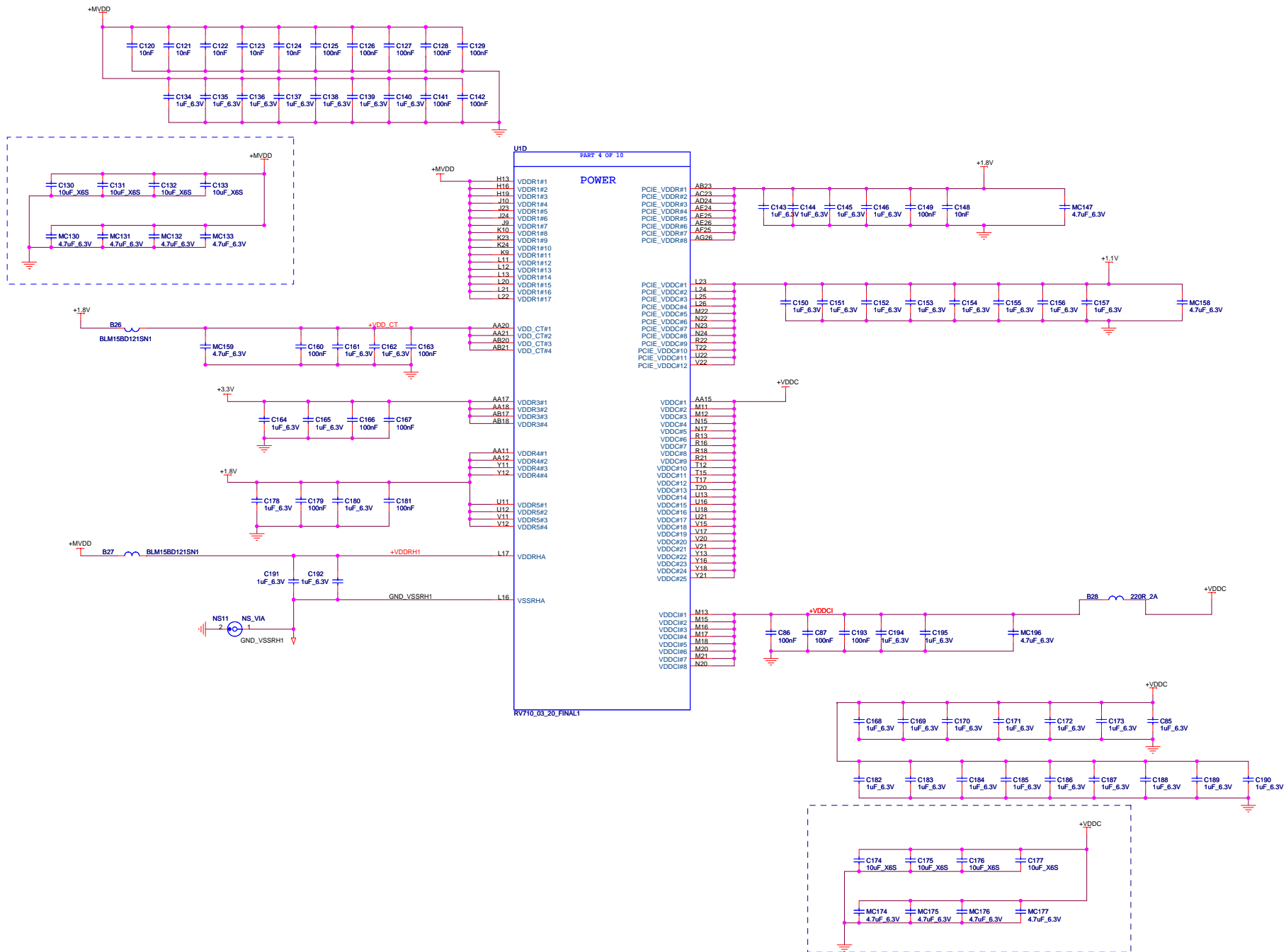


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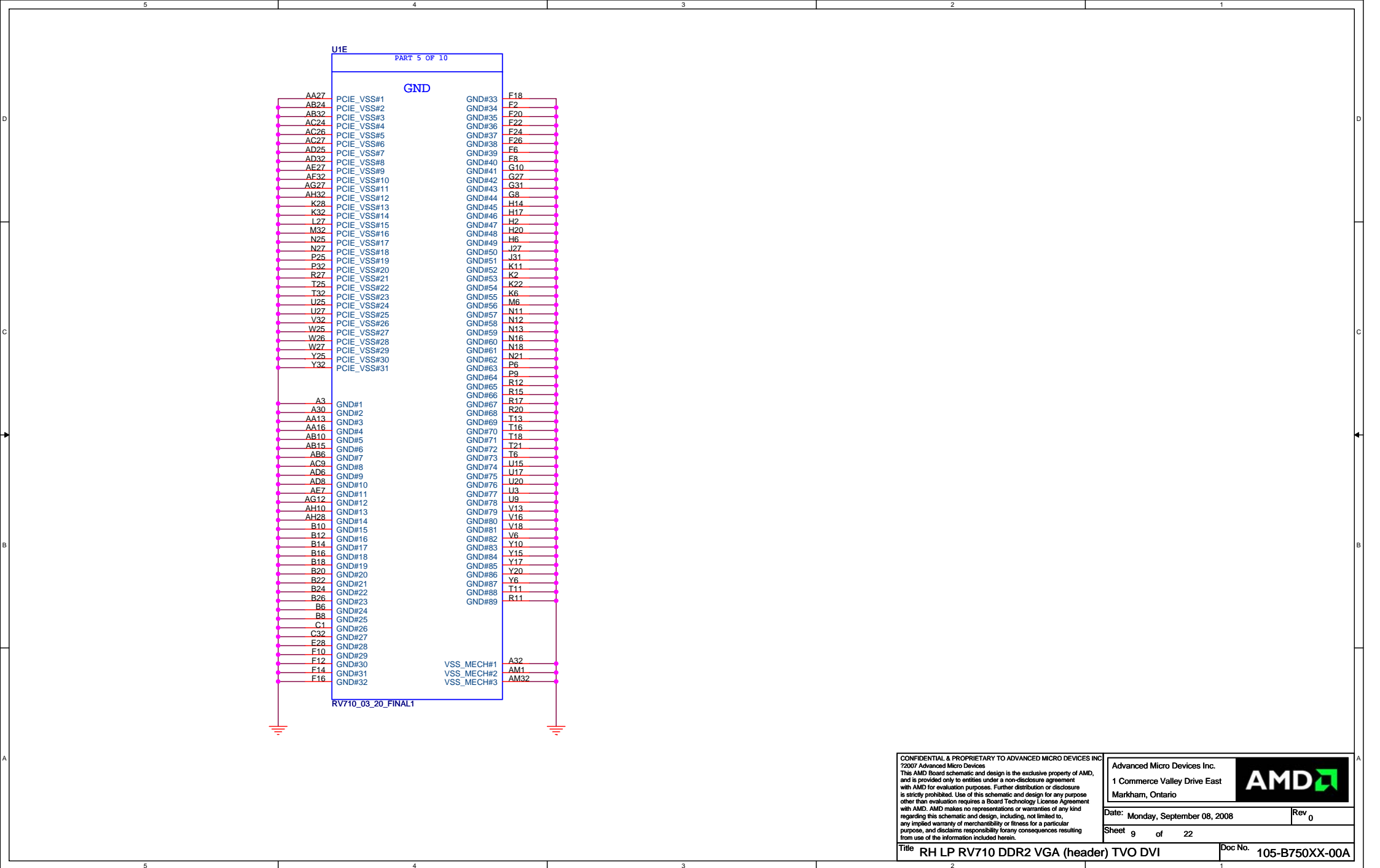
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|-------|--|---------------------------------------|--|---------|--|----------------|--|







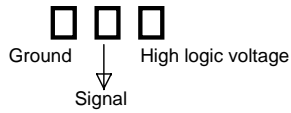
## PIN BASED STRAPS

Pull-Down Resistors are for BU until built-in pull-downs are verified.

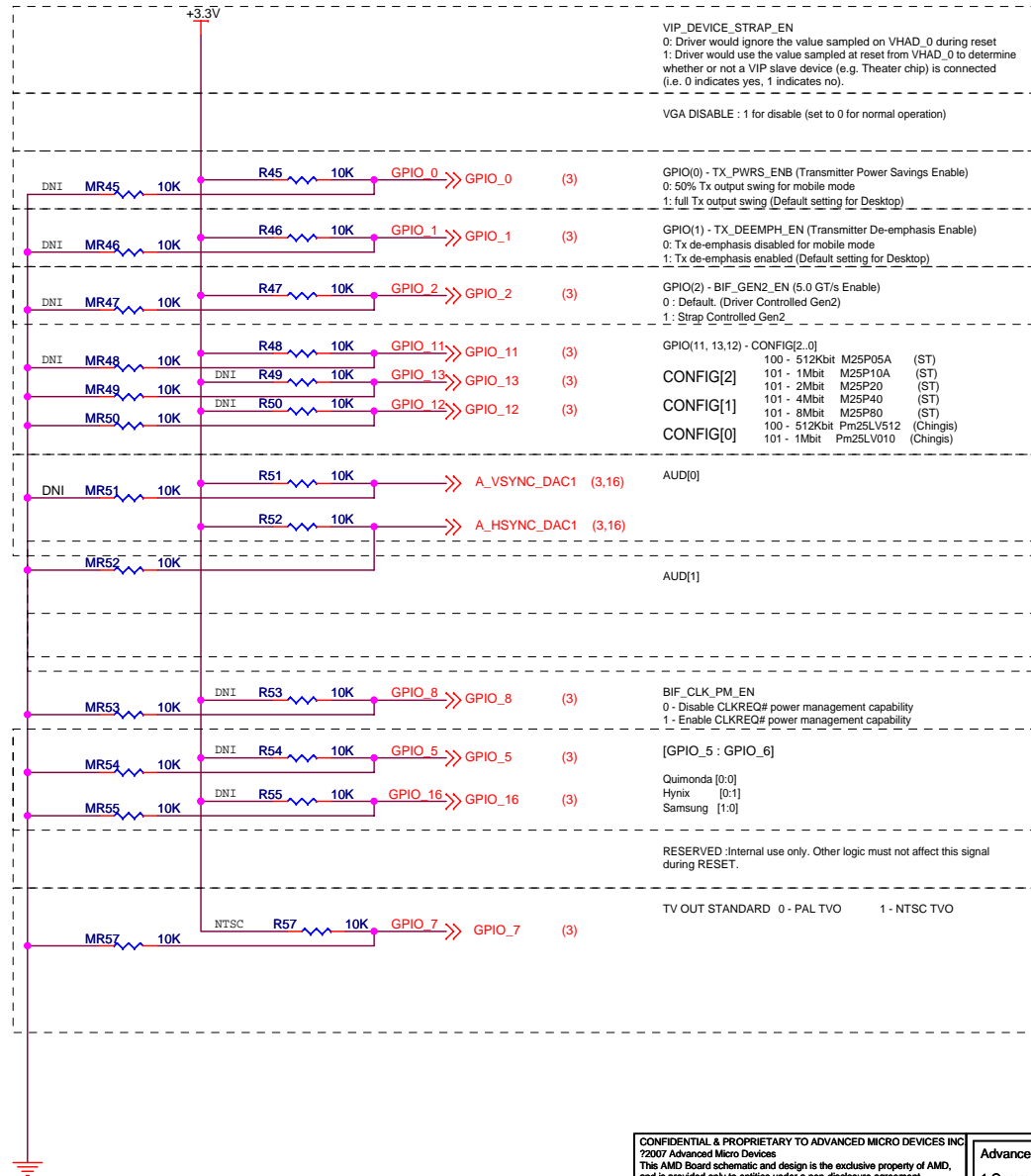


Overlap pads to save space  
and to prevent assembly of  
both resistors.

Layout



## PIN BASED STRAPS



VIP\_DEVICE\_STRAP\_EN  
0: Driver would ignore the value sampled on VHAD\_0 during reset  
1: Driver would use the value sampled at reset from VHAD\_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no).

VGA\_DISABLE : 1 for disable (set to 0 for normal operation)

GPIO(0) - TX\_PWRS\_ENB (Transmitter Power Savings Enable)  
0: 50% Tx output swing for mobile mode  
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX\_DEEMPH\_EN (Transmitter De-emphasis Enable)  
0: Tx de-emphasis disabled for mobile mode  
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF\_GEN2\_EN (5.0 GT/s Enable)  
0: Default. (Driver Controlled Gen2)  
1: Strap Controlled Gen2

GPIO(11, 13, 12) - CONFIG[2..0]  
100 - 512Kbit M25P05A (ST)  
101 - 1Mbit M25P10A (ST)  
101 - 2Mbit M25P20 (ST)  
101 - 4Mbit M25P40 (ST)  
101 - 8Mbit M25P80 (ST)  
100 - 512Kbit Pm25LV512 (Chingis)  
101 - 1Mbit Pm25LV010 (Chingis)

AUD[0]

A\_VSYNC\_DAC1 (3,16)

A\_HSYNC\_DAC1 (3,16)

AUD[1]

BIF\_CLK\_PM\_EN  
0 - Disable CLKREQ# power management capability  
1 - Enable CLKREQ# power management capability

[GPIO\_5 : GPIO\_6]

Quimonda [0:0]  
Hynix [0:1]  
Samsung [1:0]

RESERVED :Internal use only. Other logic must not affect this signal during RESET.

TV OUT STANDARD 0 - PAL TVO 1 - NTSC TVO

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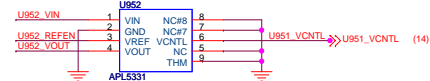
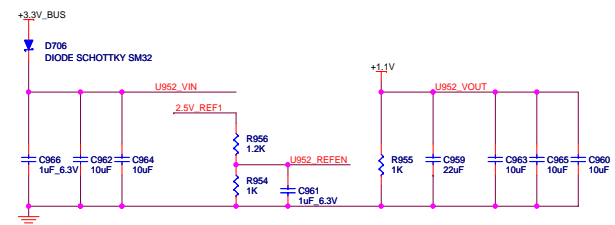
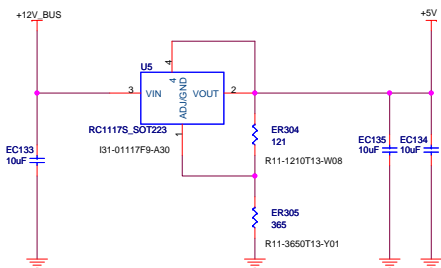
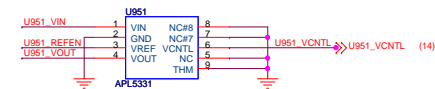
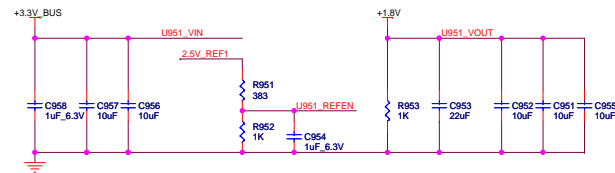
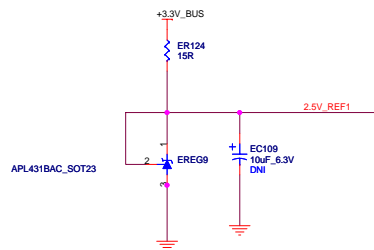
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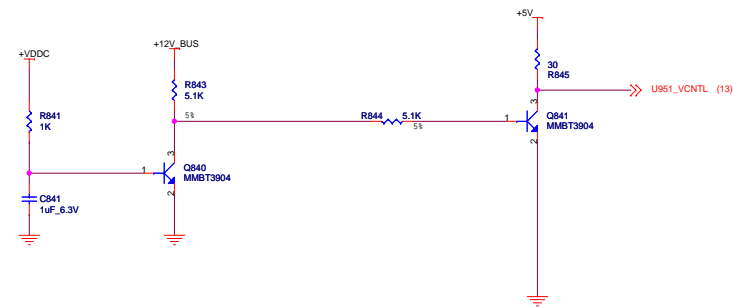
Memory Power Seq

$+MVDD = 0.8 * ( 1 + ( ER12 / ER13 ) )$



$$V_{out} = 1.25V \cdot \left[ 1 + \left( \frac{ER305}{ER304} \right) \right]$$





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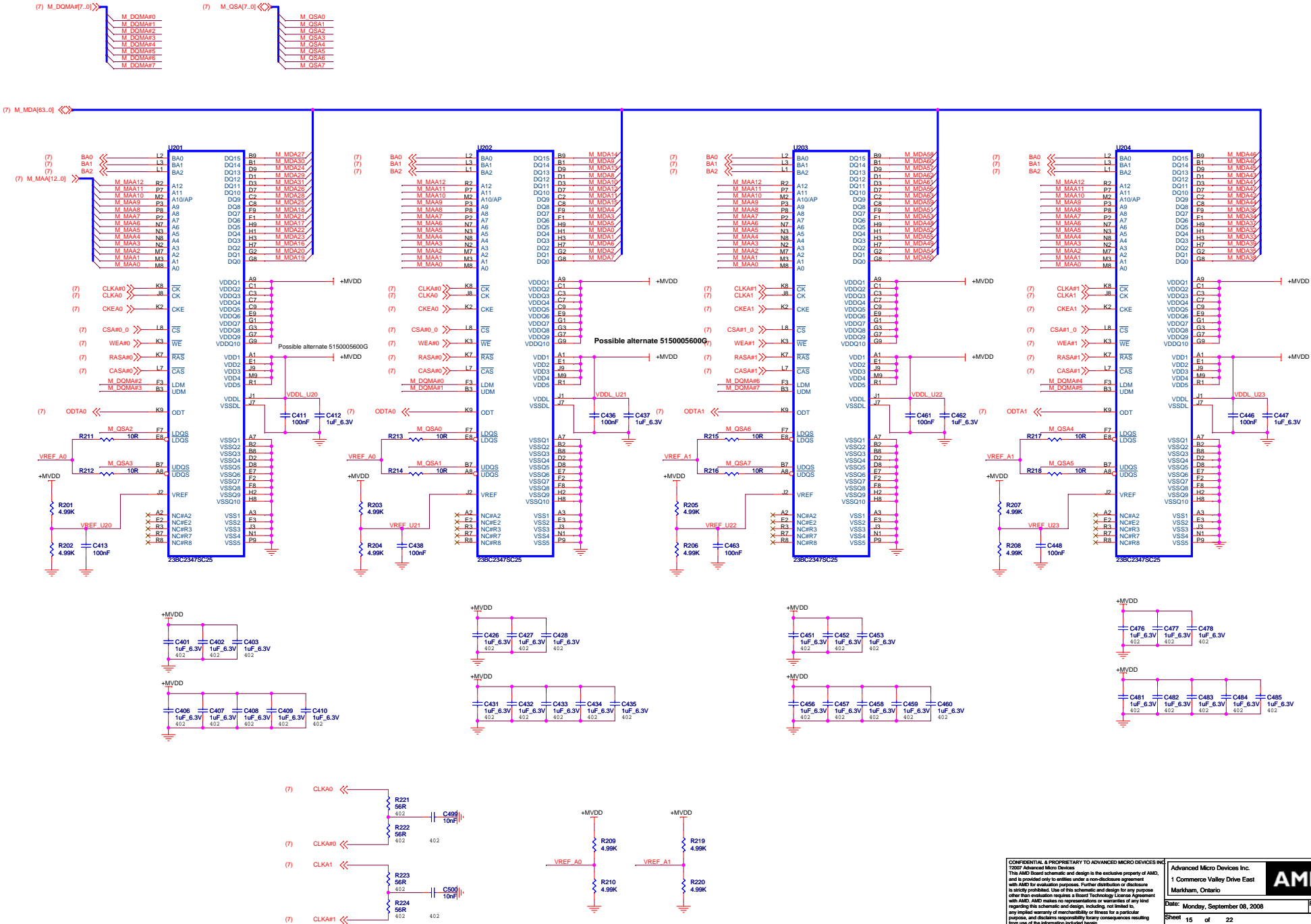
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# CHANNEL A: RANK 0 512MB DDR2

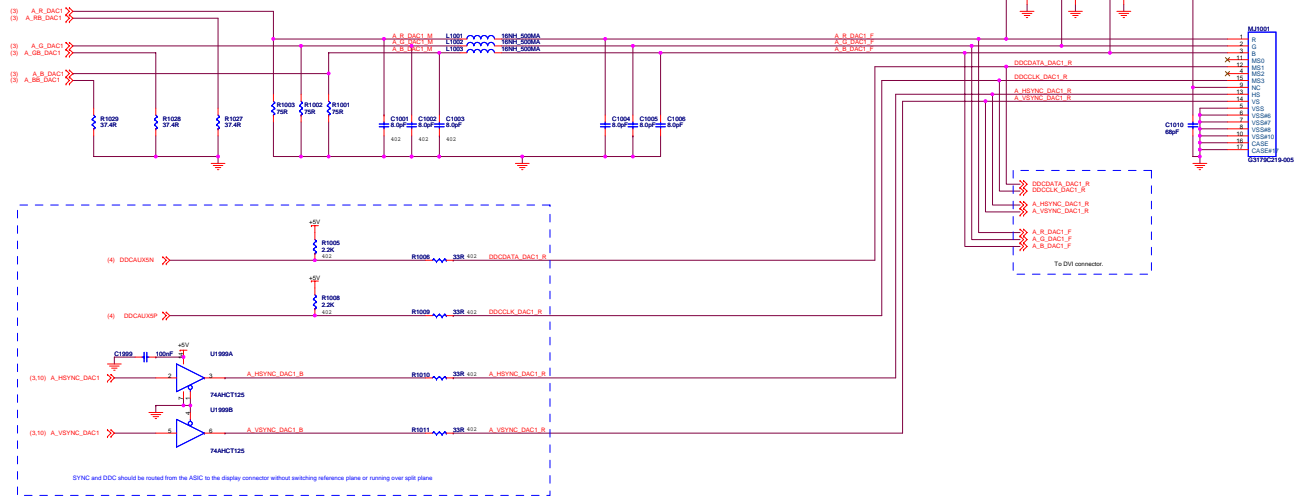
MAX DENSITY: 64Mx16



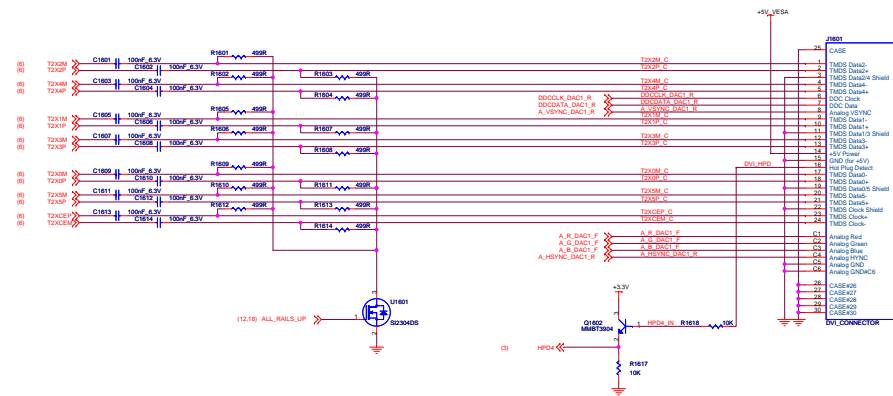
## DAC 1 OUTPUT



Place close to Connector  
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane  
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)

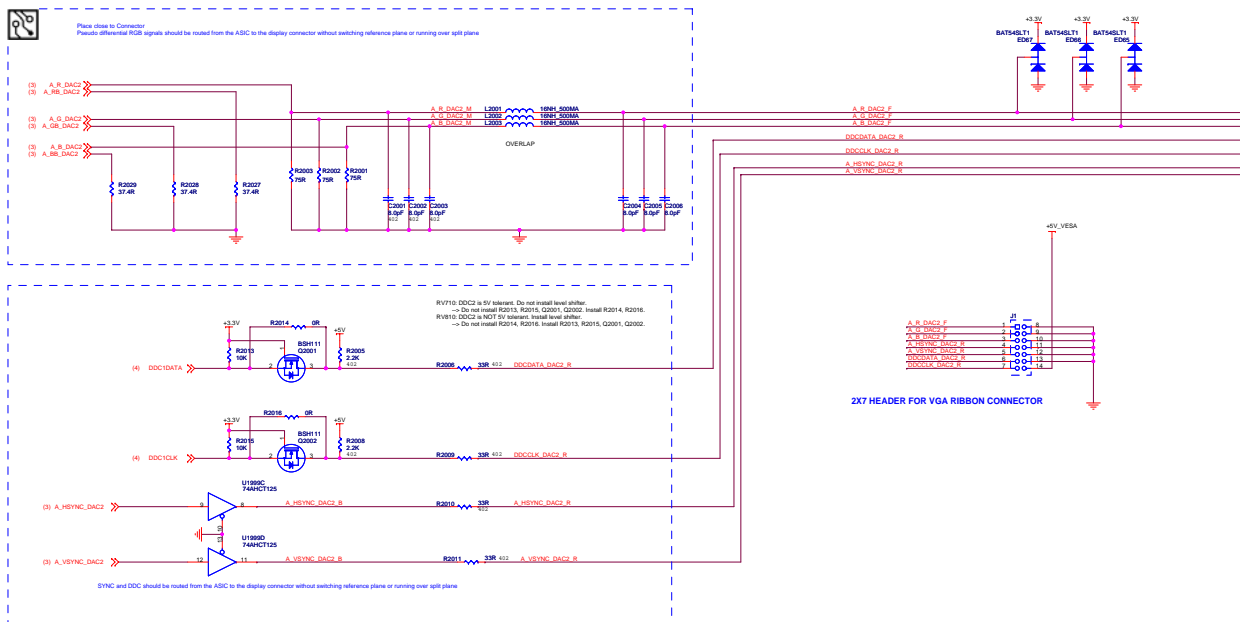


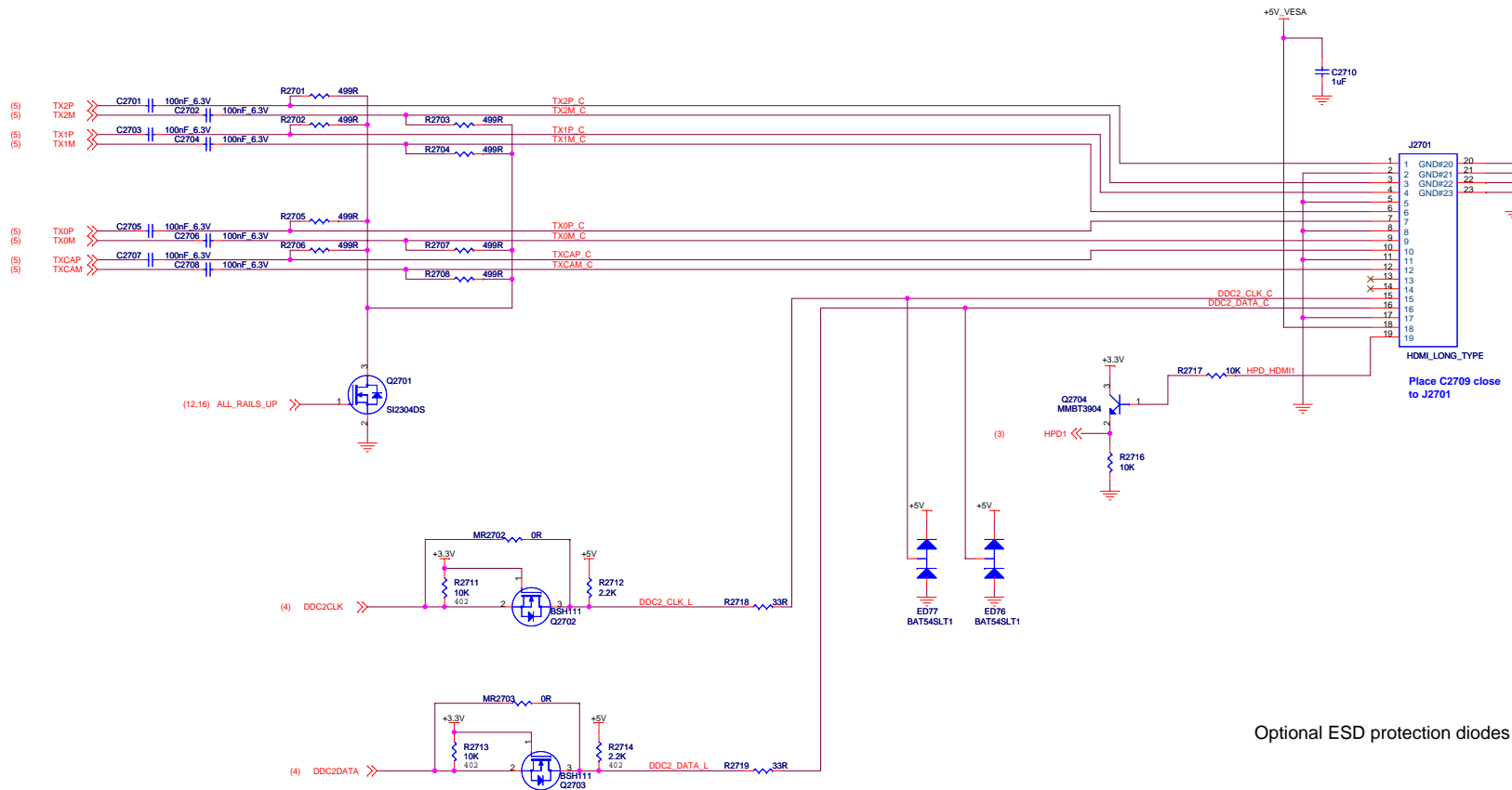
## DPE / DPF OUTPUT





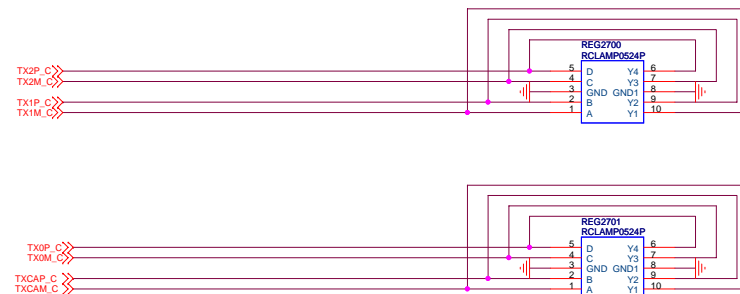
## DAC 2 OUTPUT





HDMI

Optional ESD protection diodes



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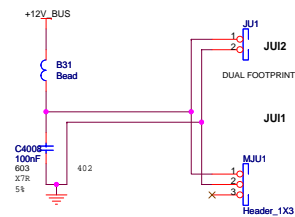
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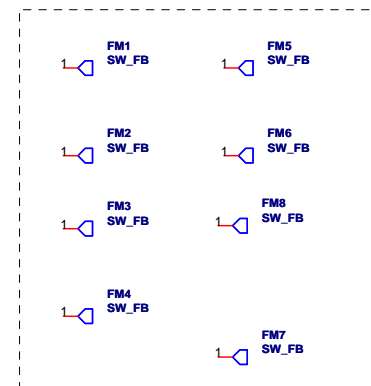
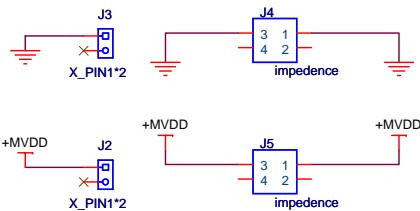
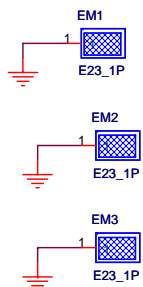
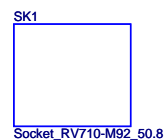
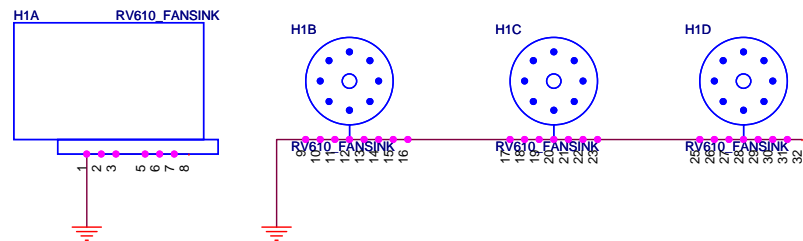
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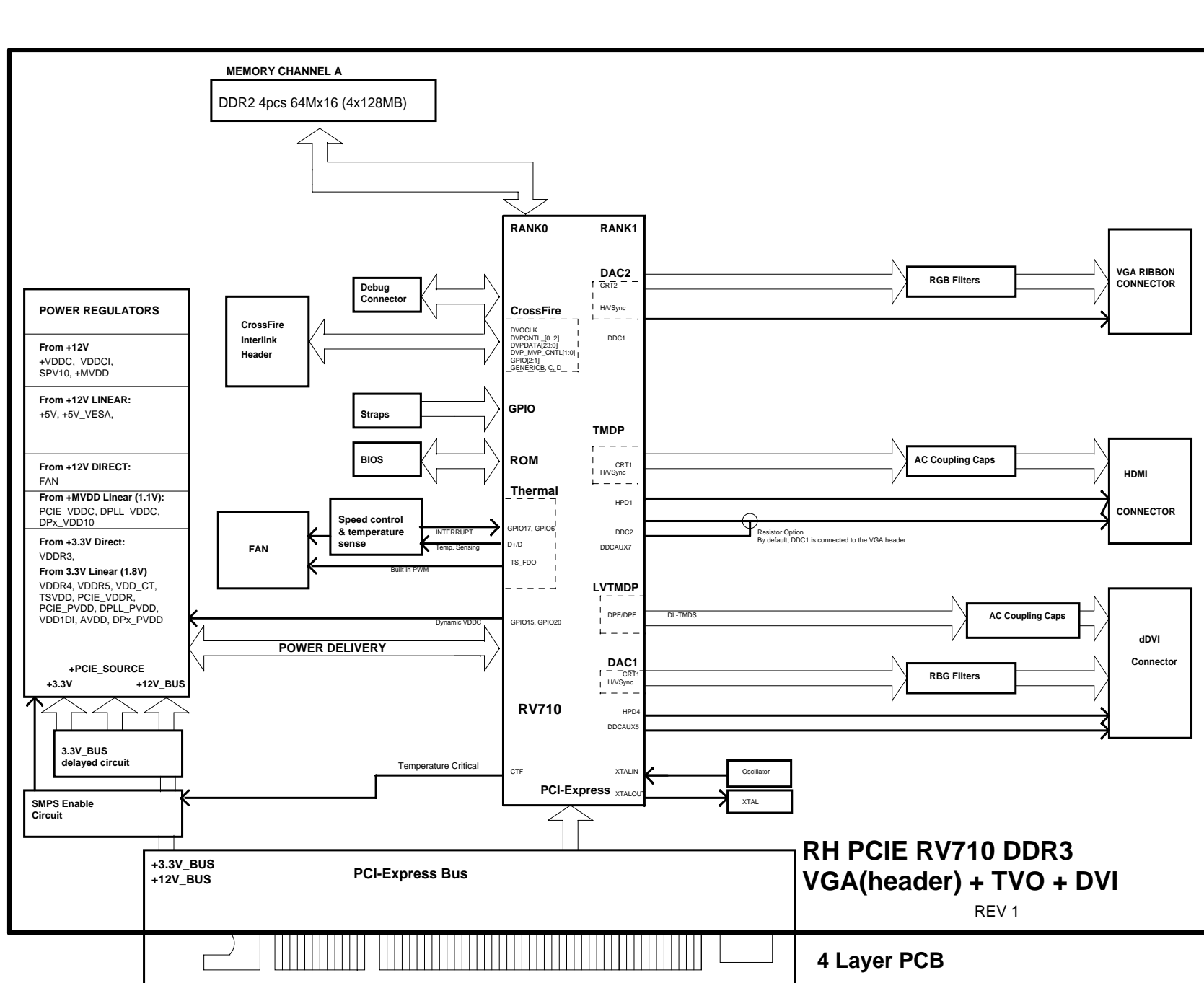


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5

4

3

2

1

AMD

Title

RH LP RV710 DDR2 VGA (header) TVO DVI

Schematic No.

105-B750XX-00A

Date:

Monday, September 08, 2008

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.  
For Stuffing options (component values, DNI , ? please consult the product specific BOM.  
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev

0

Sch Rev

PCB Rev

Date

RV710 ENGINEERING BOARD

REVISION DESCRIPTION

01

00A

2008.04.02

INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.

D

D

C

C

B

B

A

A

