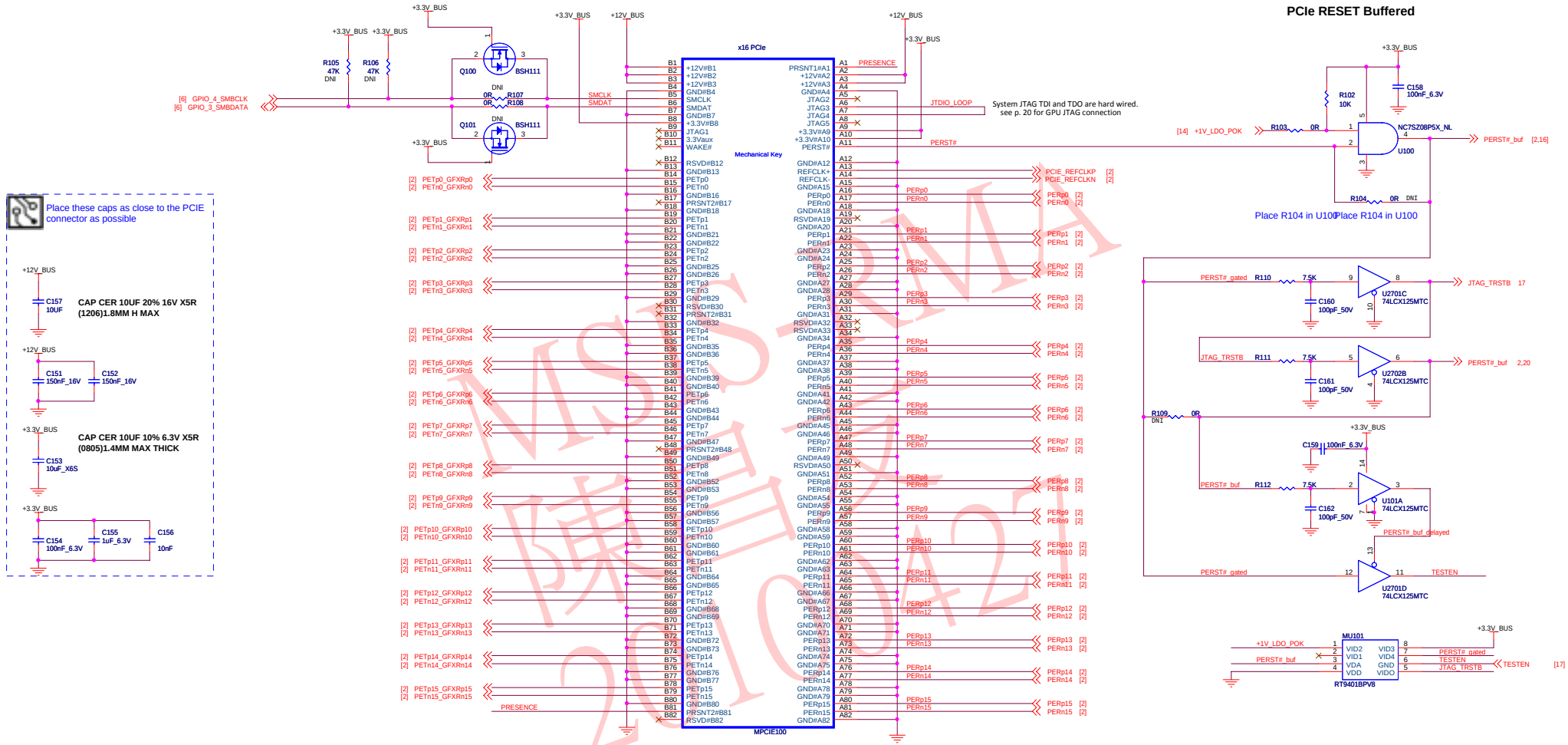
PCI-EXPRESS EDGE CONNECTOR

REDWOOD WOLVERINE



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(2) REDWOOD PCIe Interface

NOTE: Some of the PCIE testpoints will be available through vias on traces.

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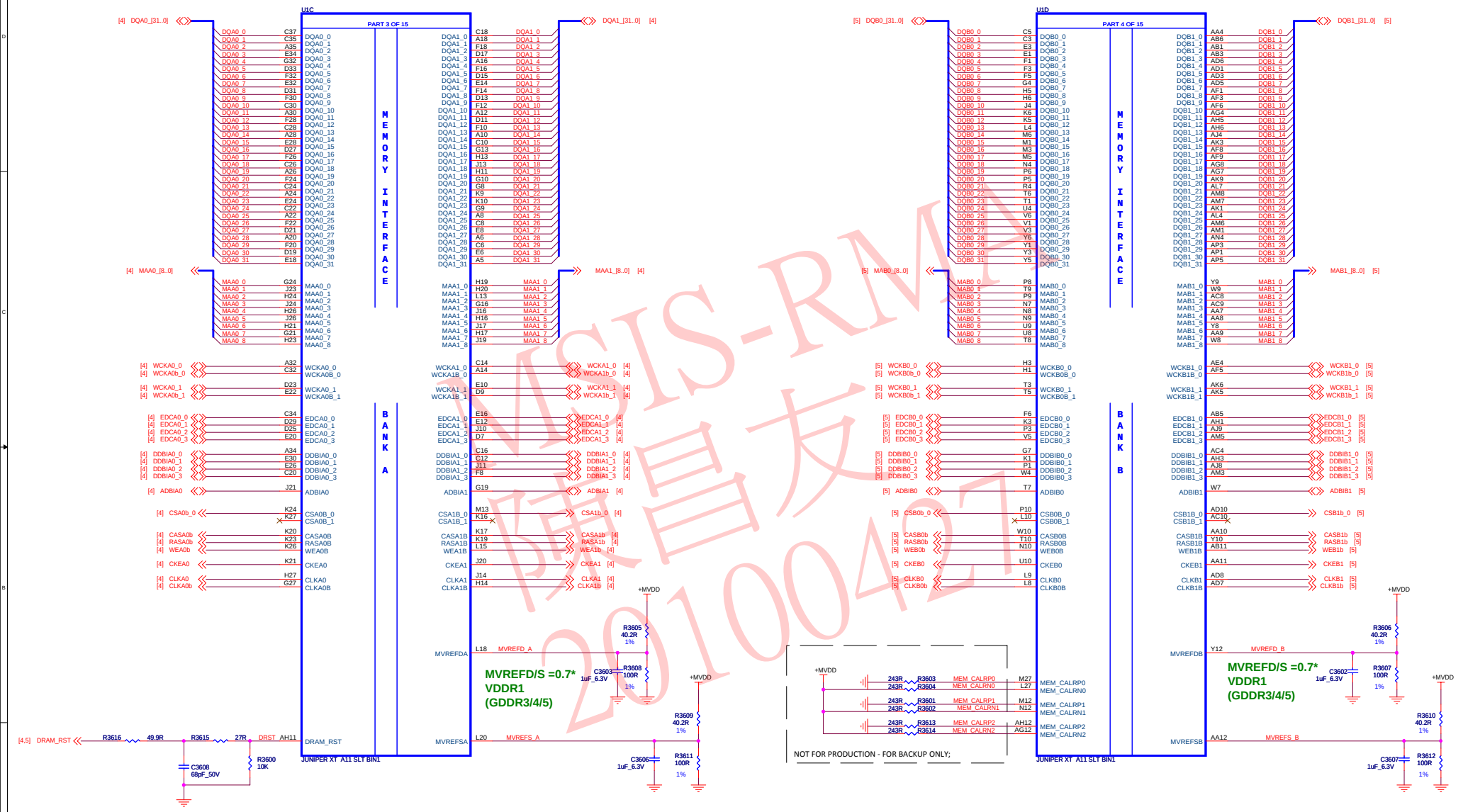
(3) REDWOOD MEM Interface Ch A&B



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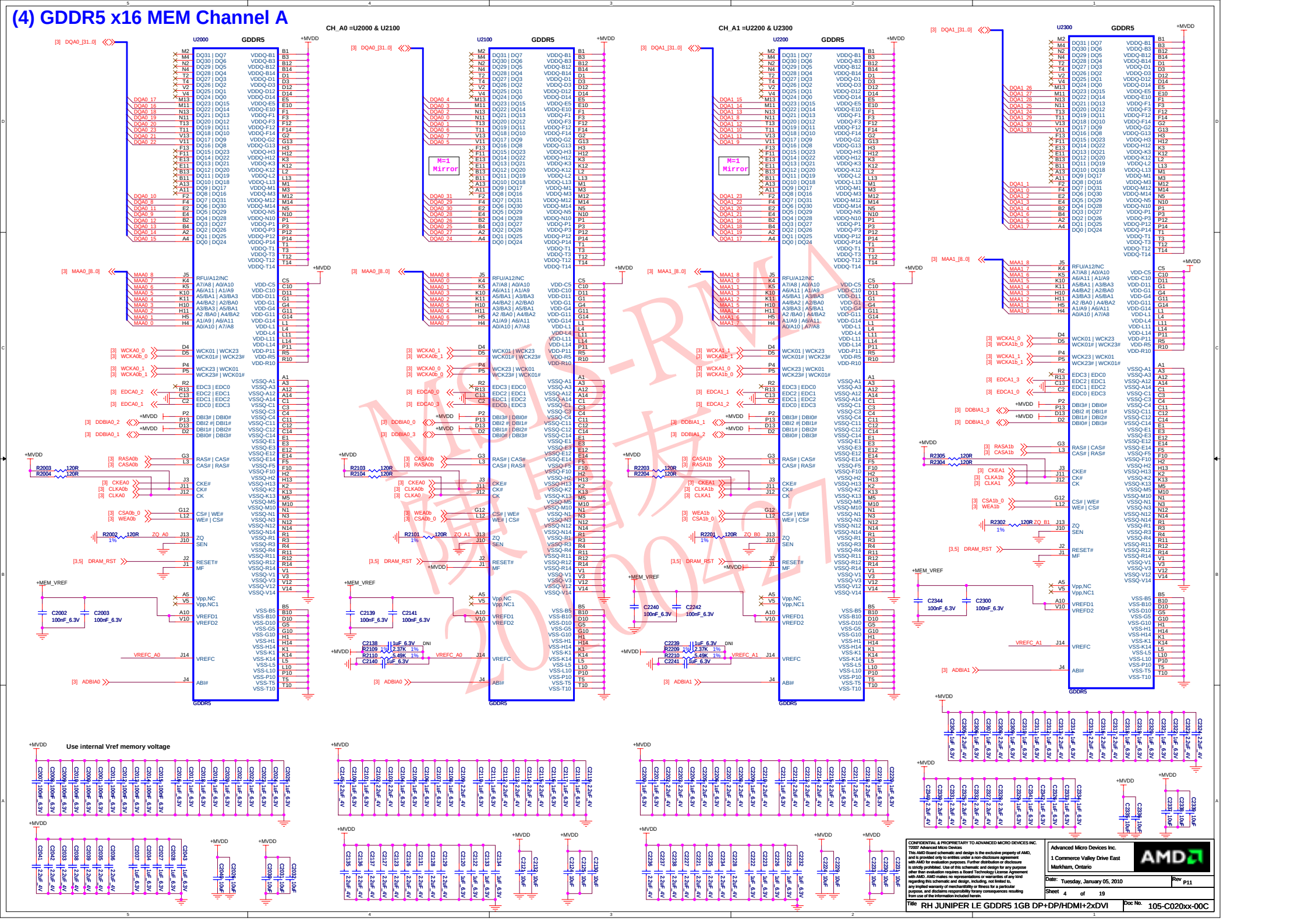
(4) GDDR5 x16 MEM Channel A



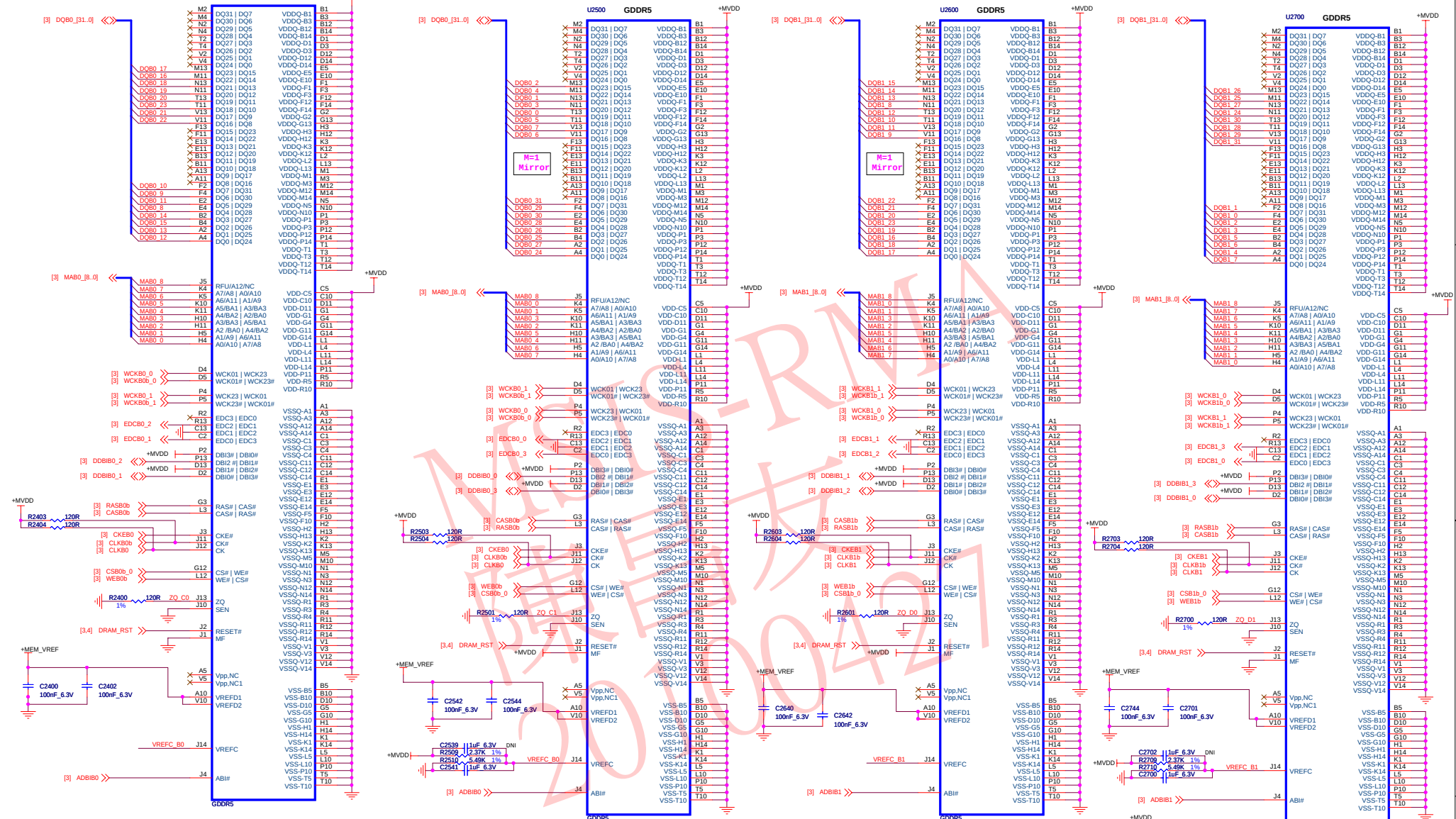
(5) GDDR5 x16 MEM Channel B

CH_B0 =U2400 & U2500

CH_B1 =U2600 & U2700

BOTTOM

TOP



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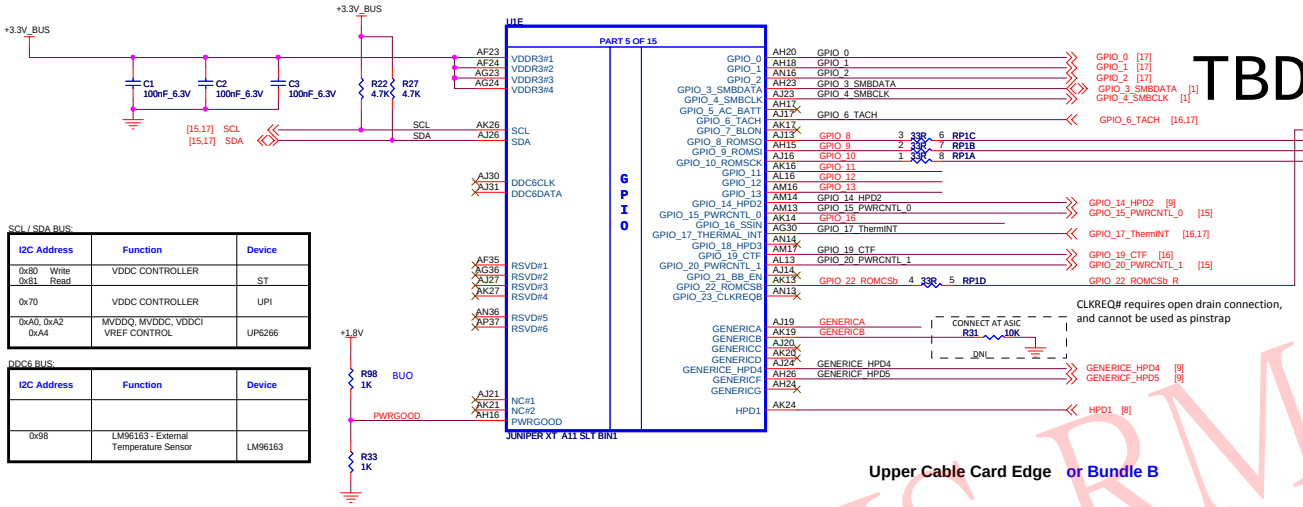
(06) REDWOOD GPIOs Strap CF XTAL OSC



SCL / SDA BUS:

I2C Address	Function	Device
0x80 Write 0x81 Read	VDDC CONTROLLER	ST
0x70	VDDC CONTROLLER	UPI
0xA0, 0xA2 0xA4	MVDDQ, MVDDC, VDDCI VREF CONTROL	UP6266

DDC6 BUS:

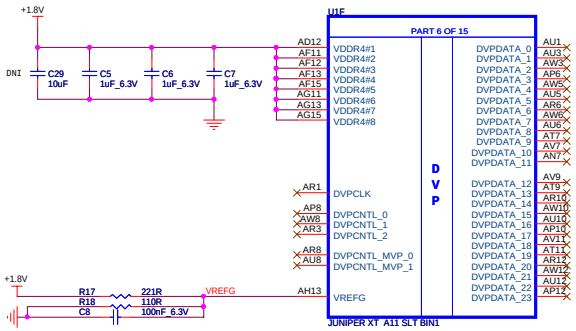
I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

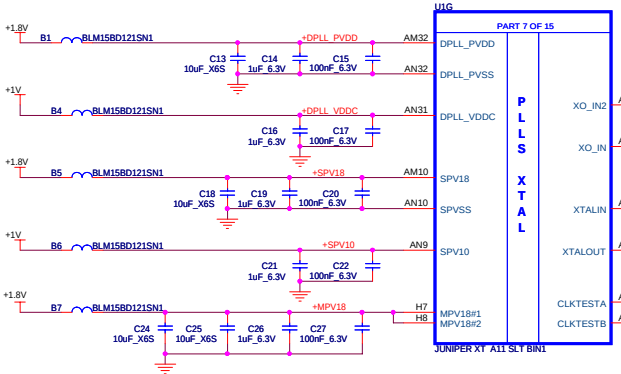
TBD

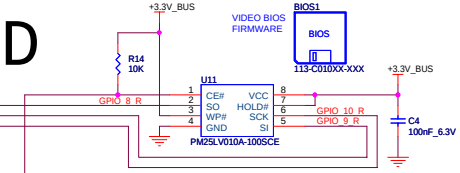
CLKREQ# requires open drain connection, and cannot be used as pinstrap

Upper Cable Card Edge or Bundle B

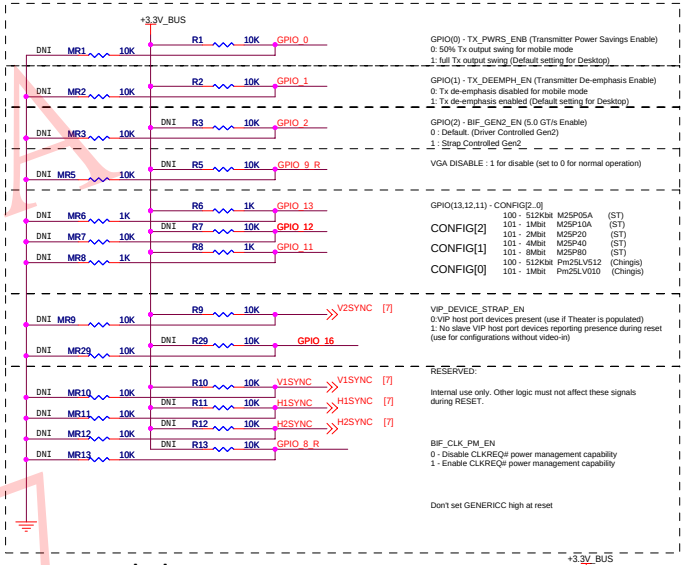
CrossFire Card-Edge

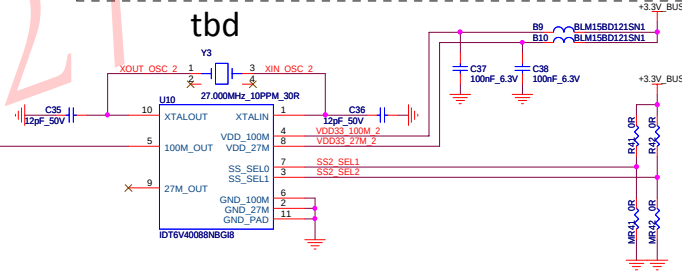


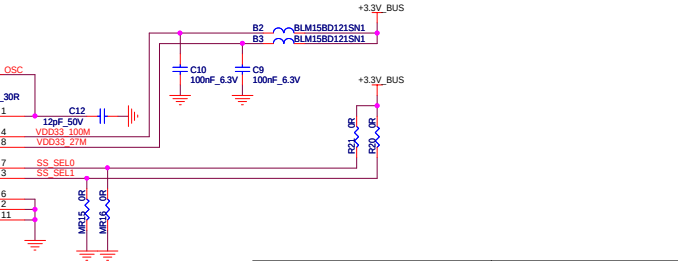




PIN BASED STRAPS







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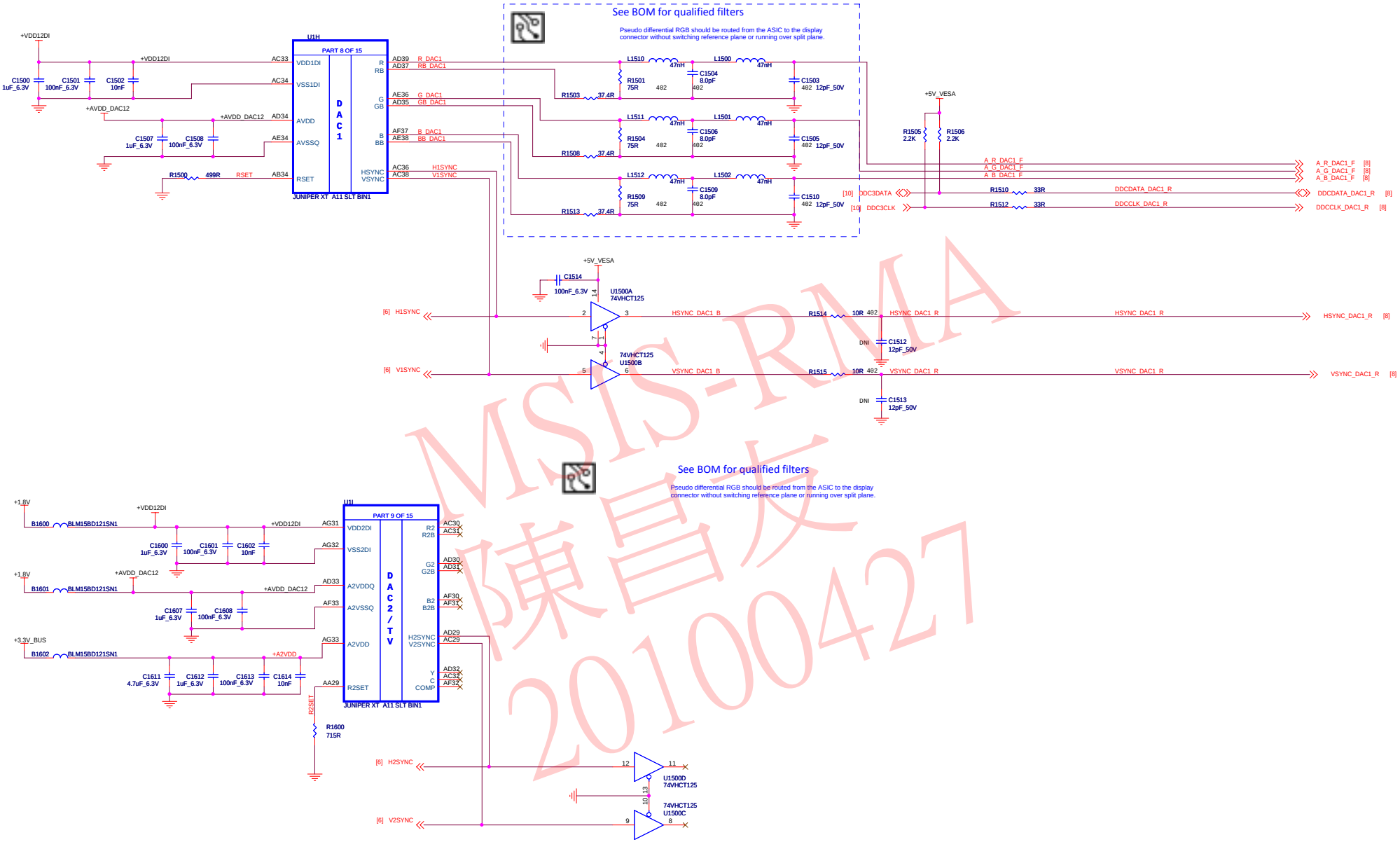
(07) REDWOOD DAC1 and DAC2



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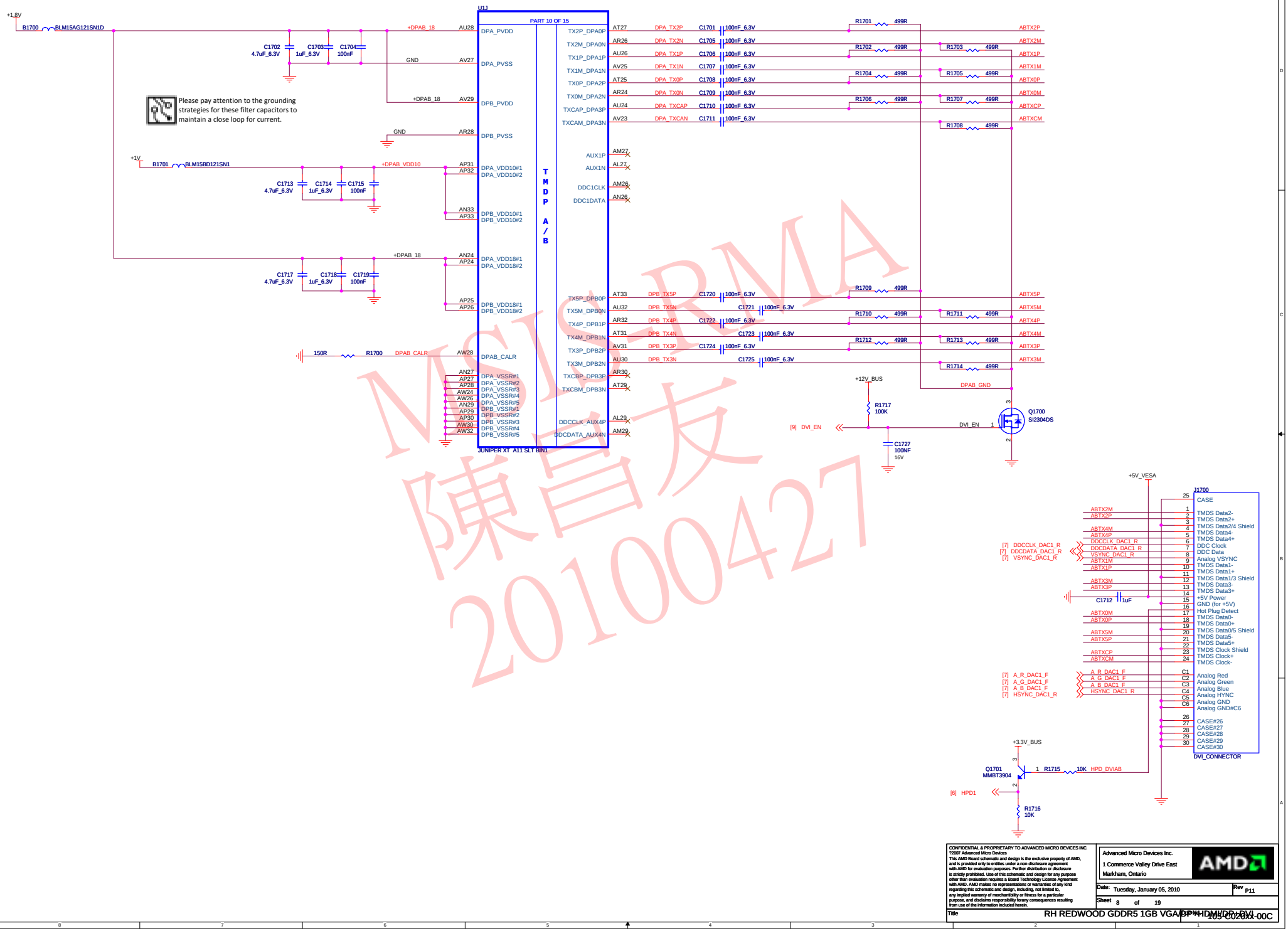
(08) REDWOOD TMDP A&B dDVI-I TOP



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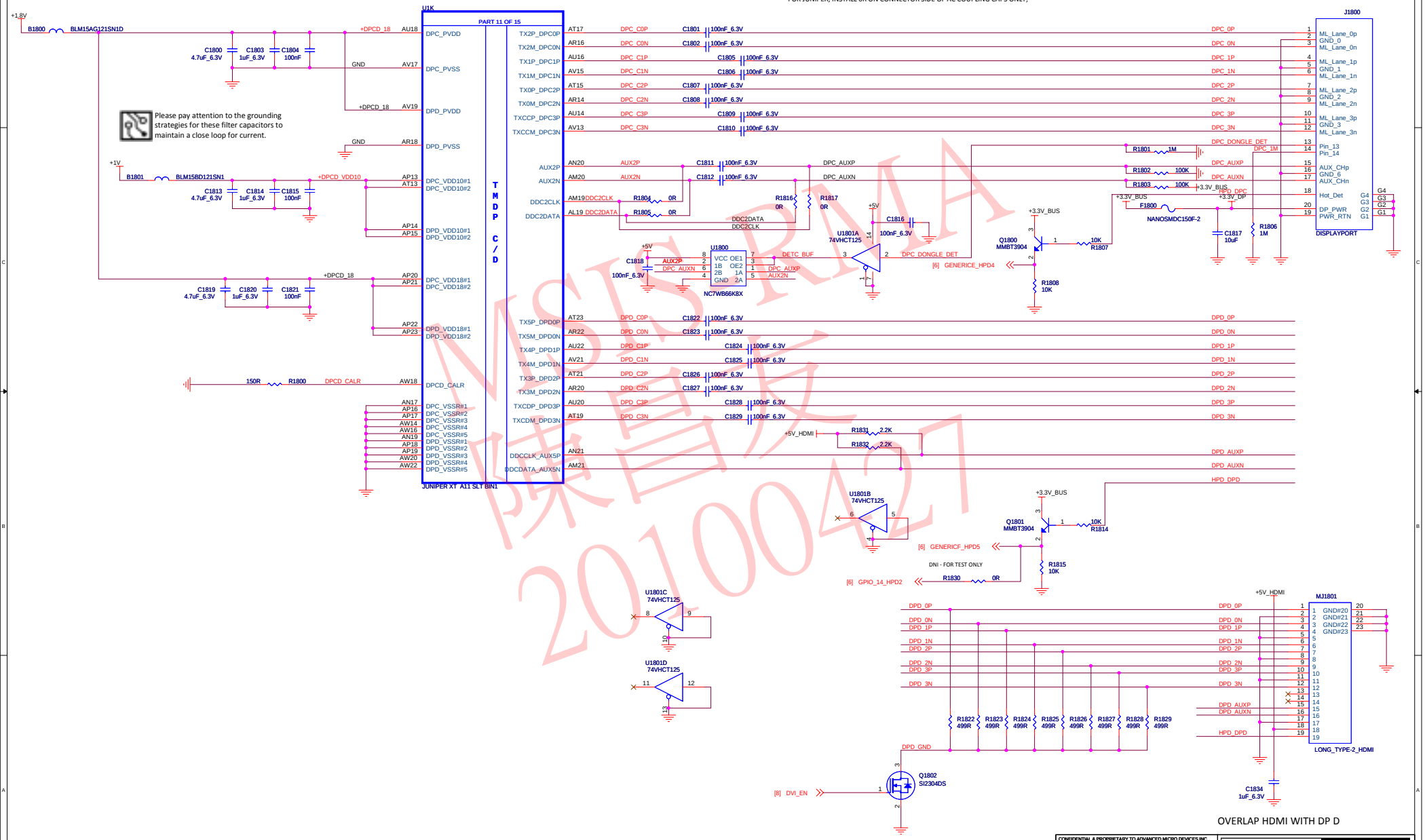
(09) REDWOOD Display Port C & Display Port/HDMI D



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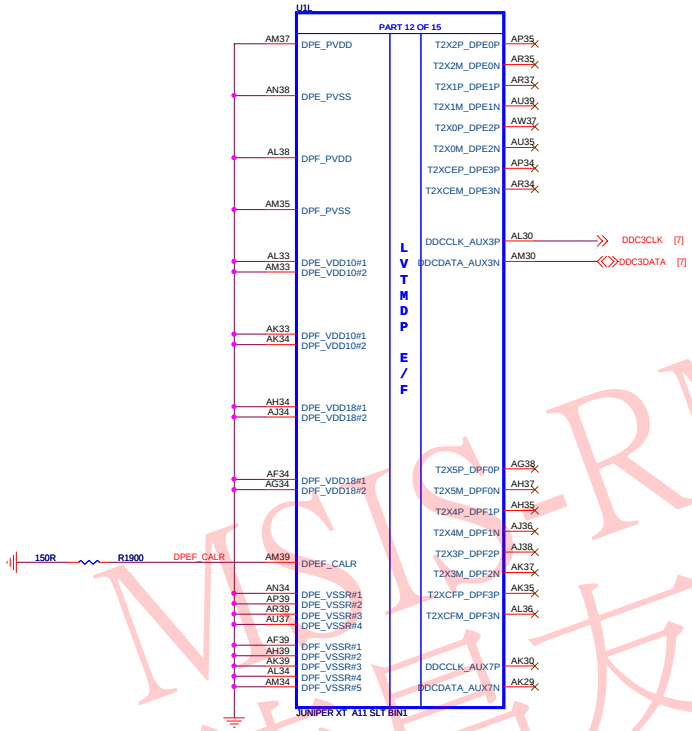
(10) REDWOOD LVTMDP E&F



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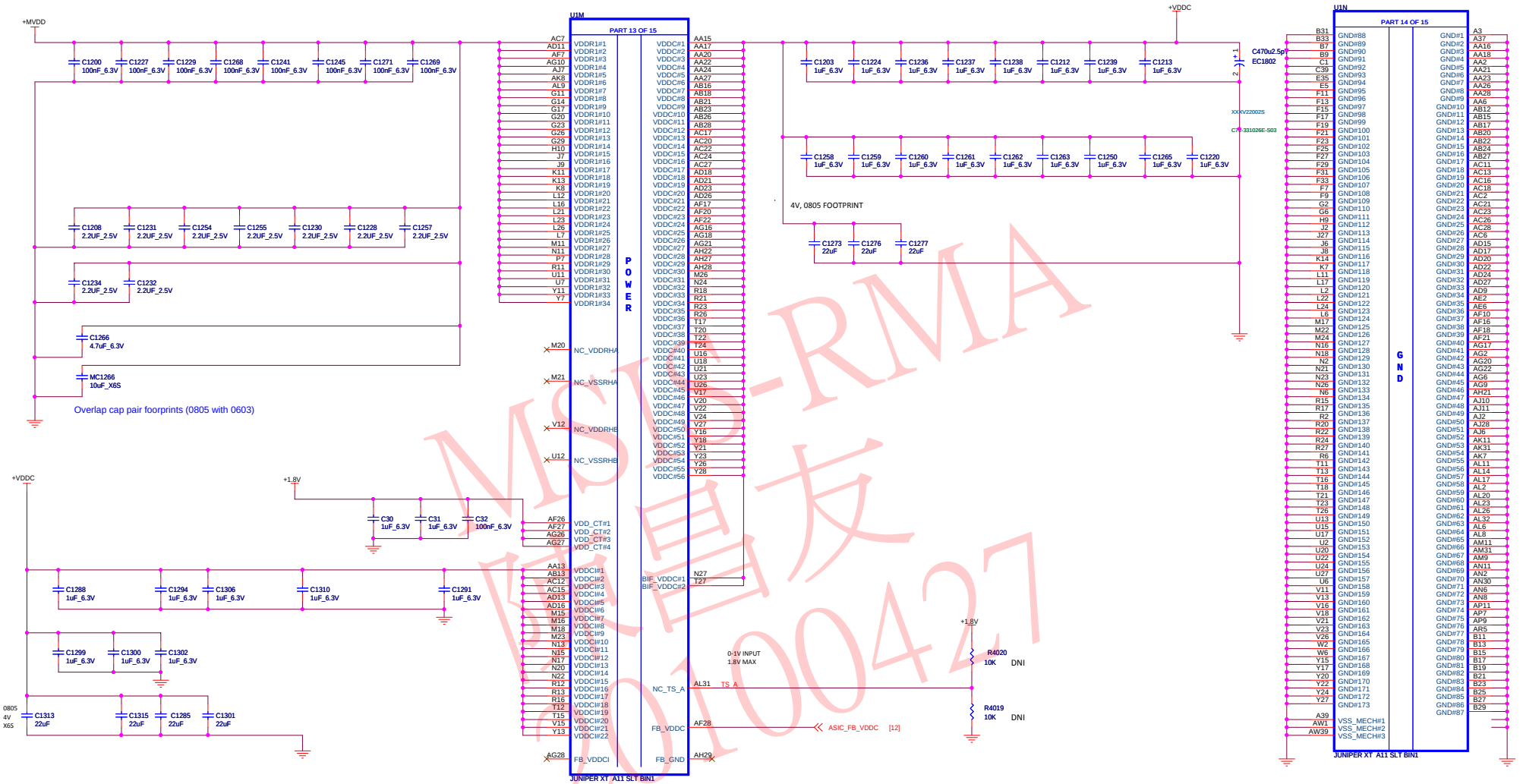
(11) REDWOOD Power & GND



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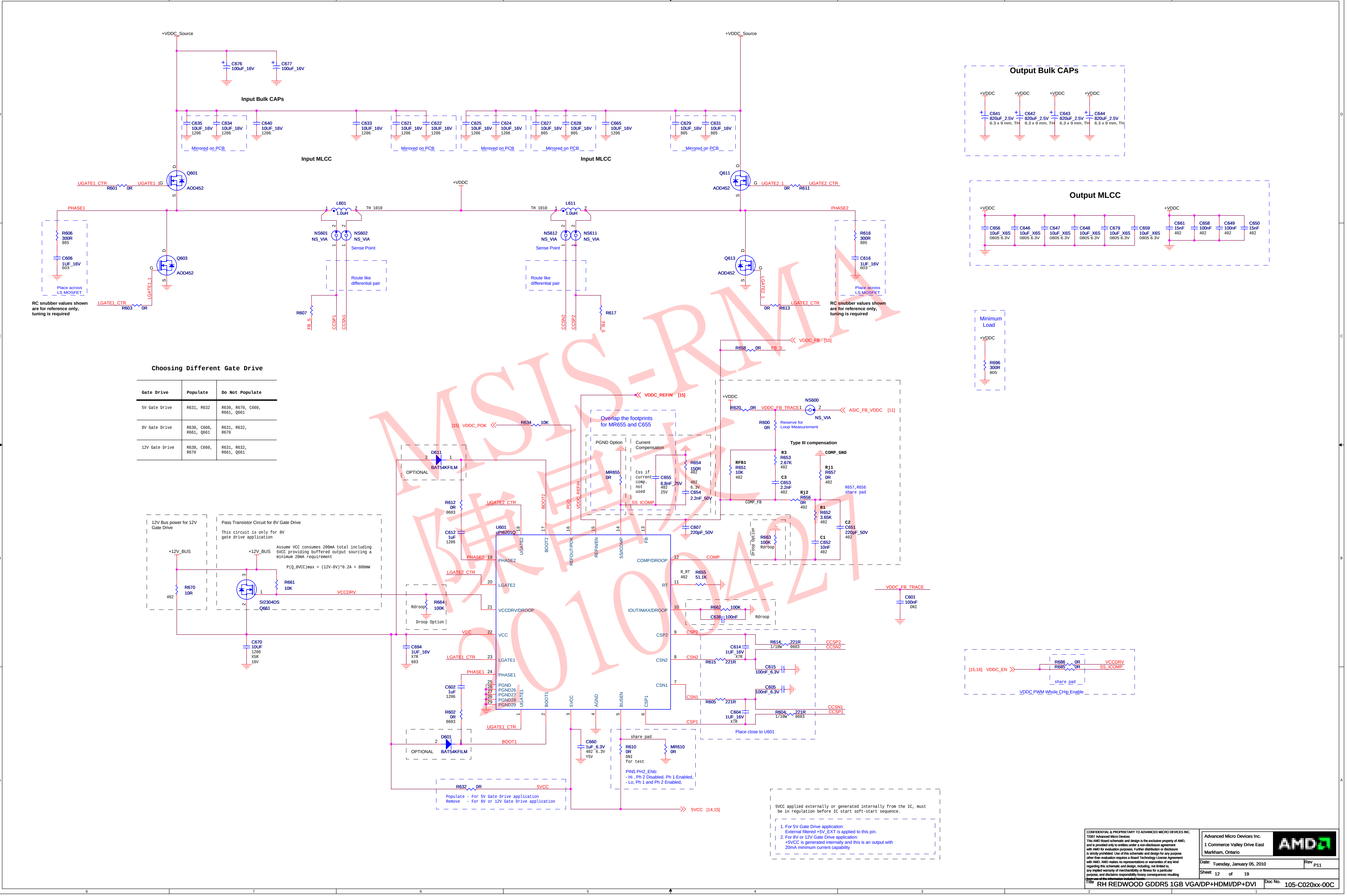

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661

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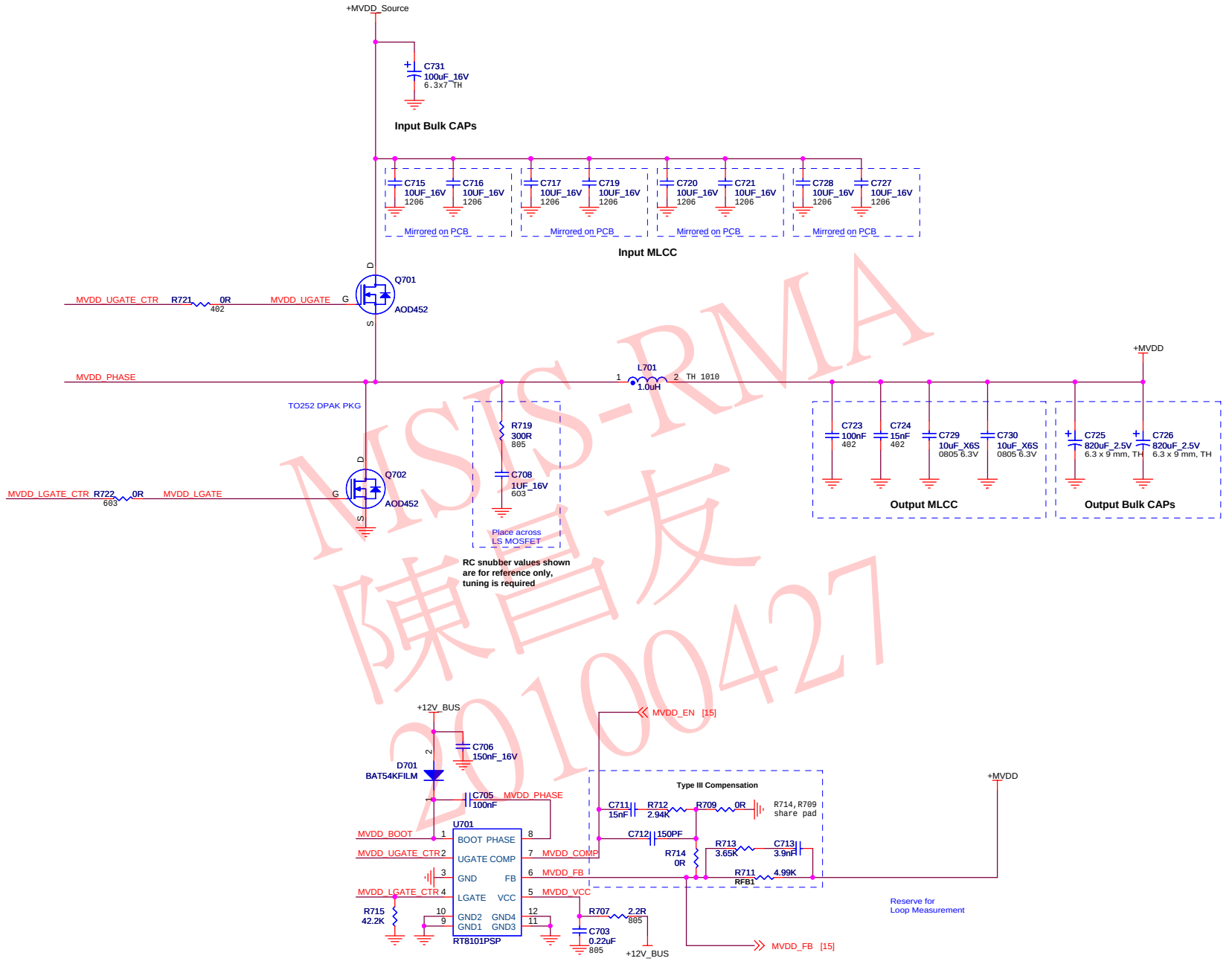

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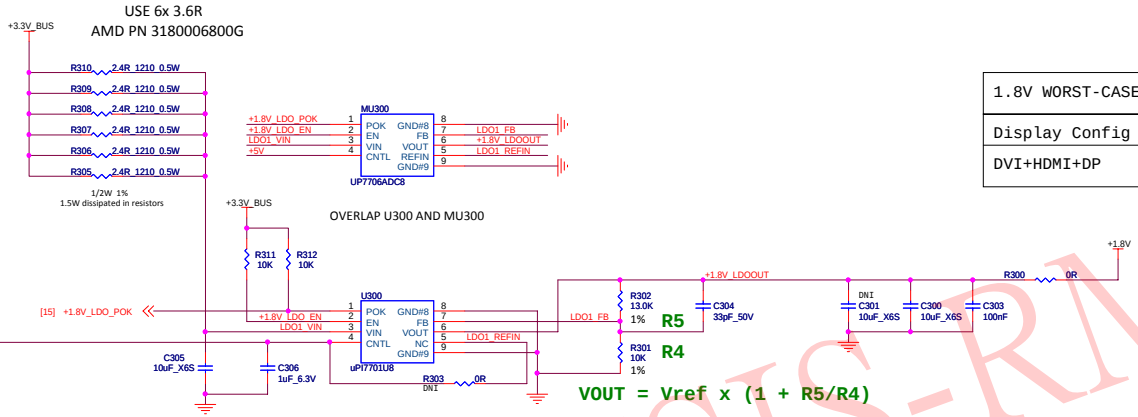
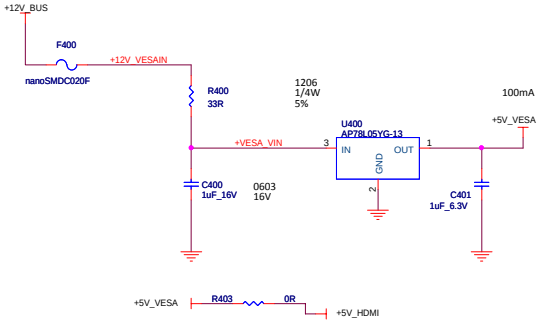
(15) Linear Regulators

Regulators for +5V, +5V_VESA and +5V_HDMI

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

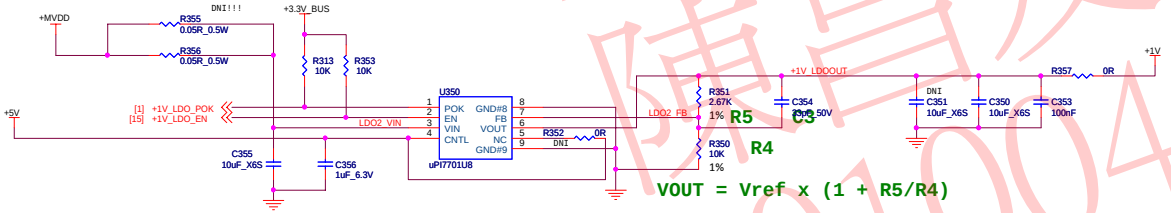


1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

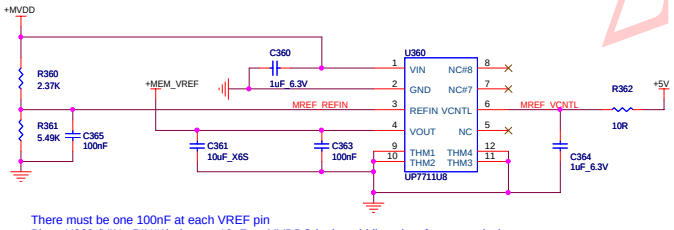


LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

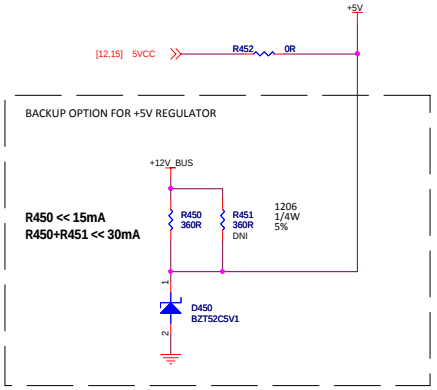
1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA



Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ



There must be one 100nF at each VREF pin
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices



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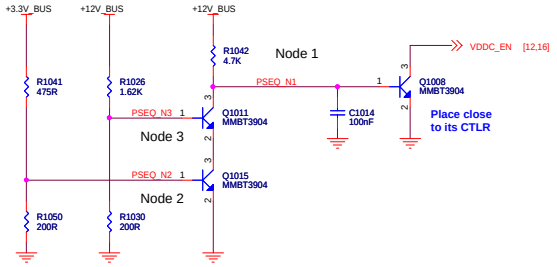
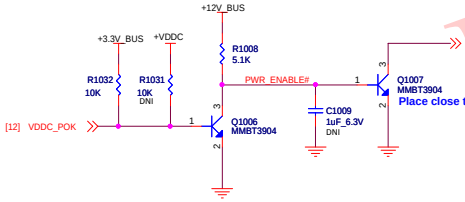
(16) Power Management - Power Gating and Dynamic Voltage Control

12V_BUS & 3V3_BUS POWER SEQUENCING



POWER SEQUENCING CIRCUIT

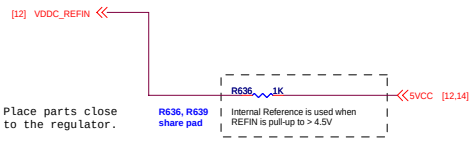


VDDC Reference Voltage Selection

VDDC Vref Mode Selection

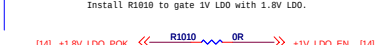
Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

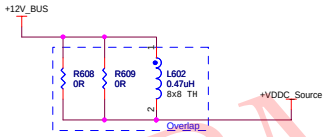
I2C VOLTAGE REFERENCE FOR VDDC (not for production)

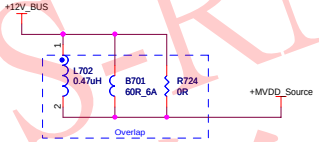


I2C ADDRESS: A4

Install R1010 to gate 1V LDO with 1.8V LDO.





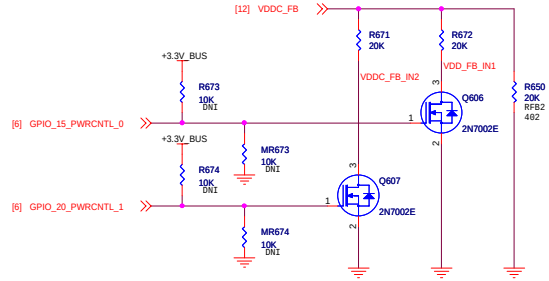


MVDD Low Side Divider

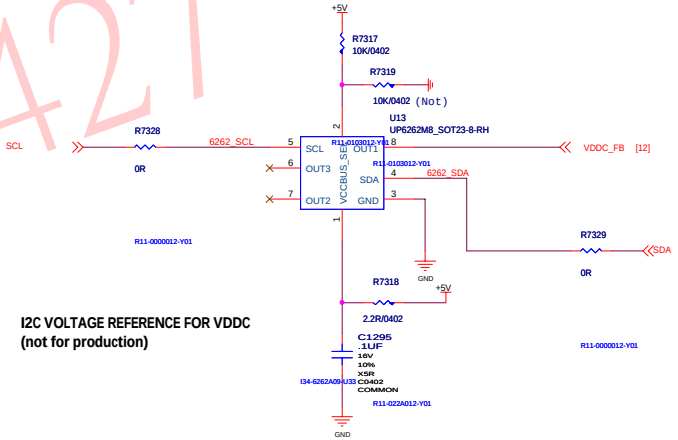
VDDC Low Side Divider

R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.

- Hi-Side Divider R651 is Fixed to 5.11K
- Vo = Vref * (1 + R651 / R650)
- Vref = 0.6V



I2C VOLTAGE REFERENCE FOR VDDC (not for production)



I2C ADDRESS: A4

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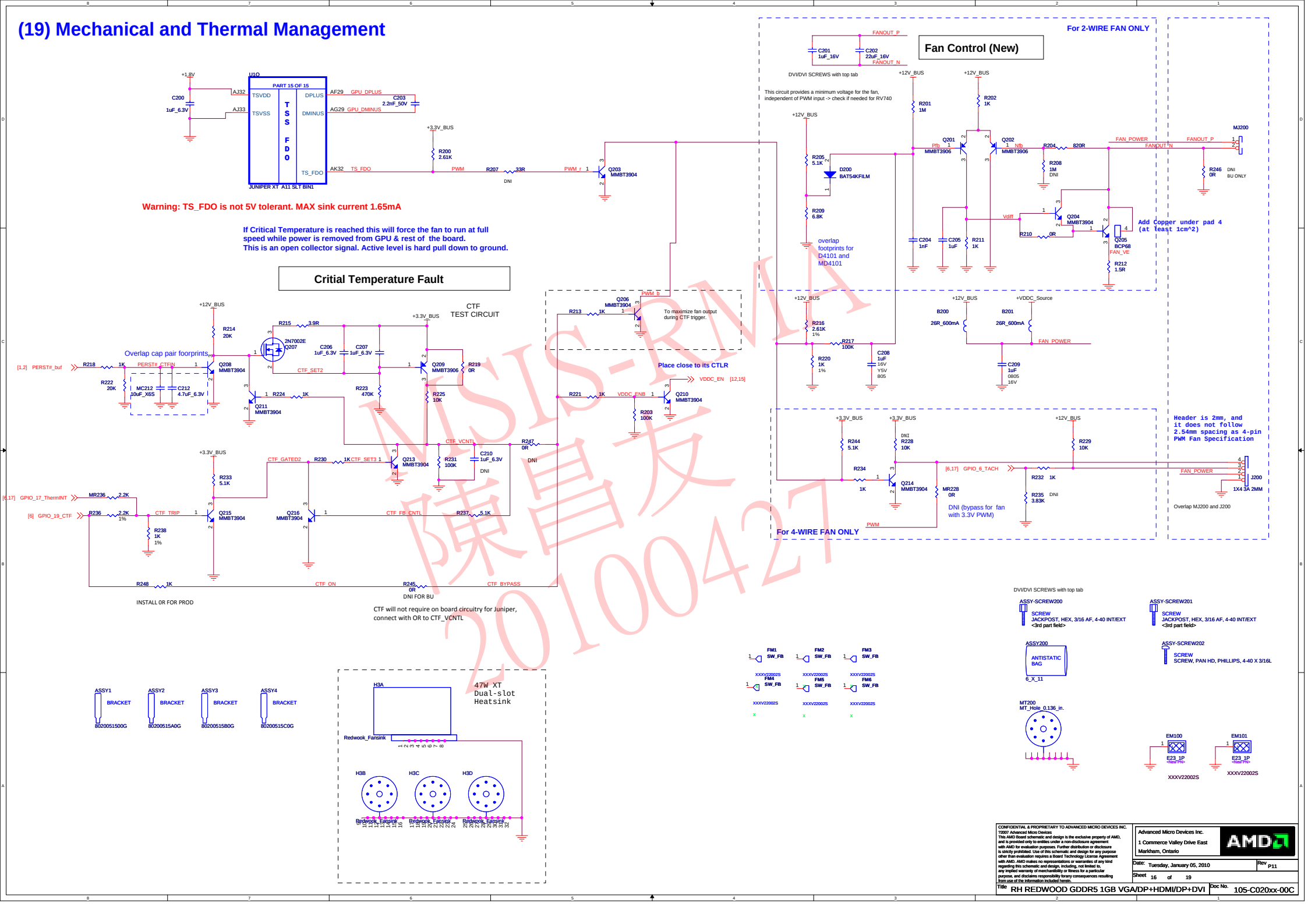
(19) Mechanical and Thermal Management



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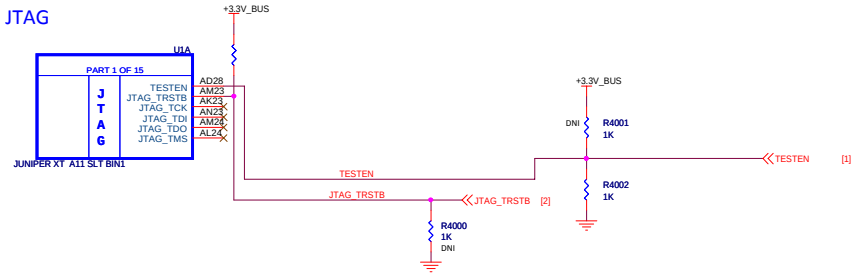
(19) Debug Circuits



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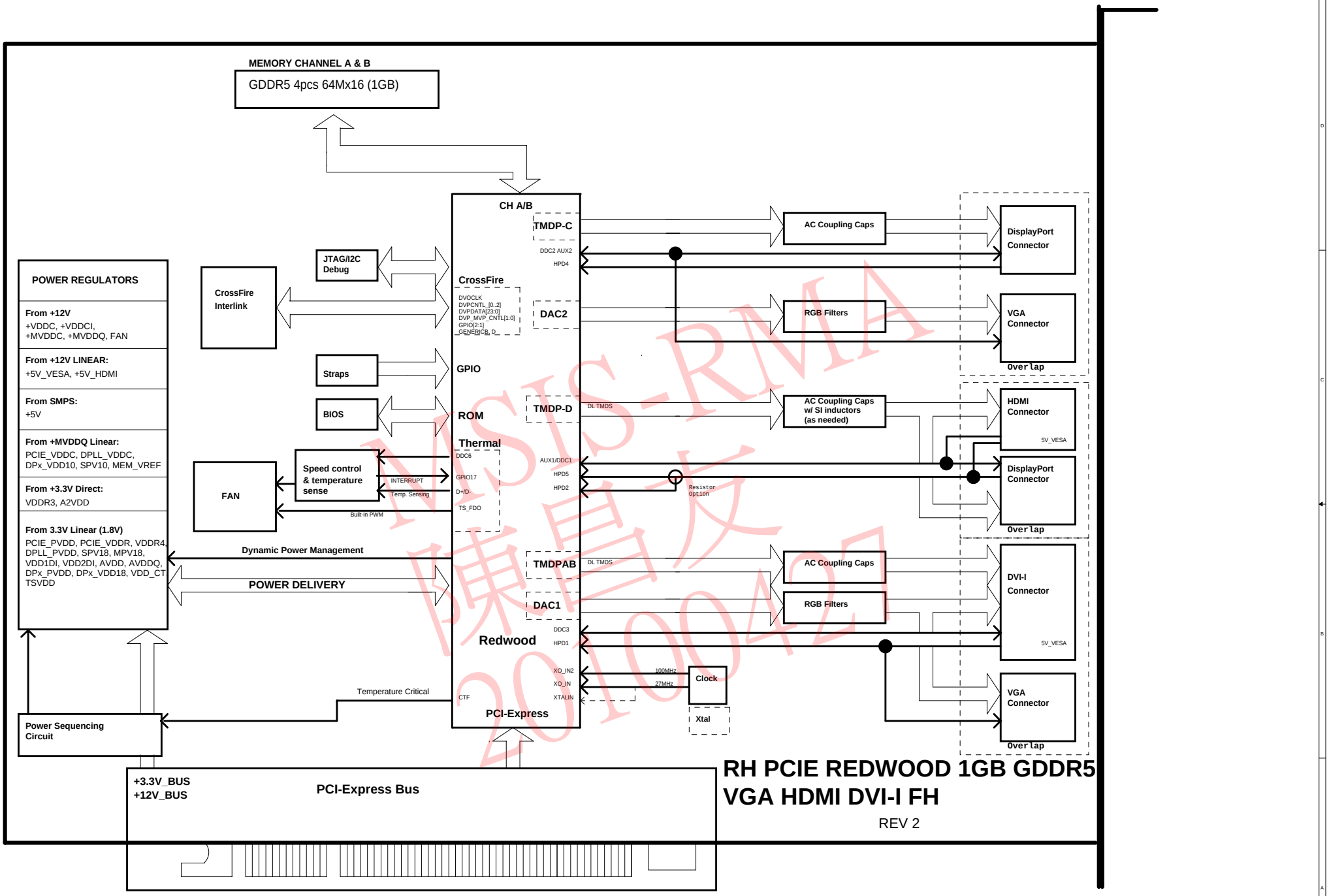

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Title	Schematic No.	Date:
RH REDWOOD GDDR5 1GB VGA/DP+HDMI/DP+DVI	105-C020xx-00C	Thursday, December 17, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev P11

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/05/08	
01	00B	2009/08/20	
02	00C	2009/09/28	REDWOOD XT GDDR5 1GB - Initial Release