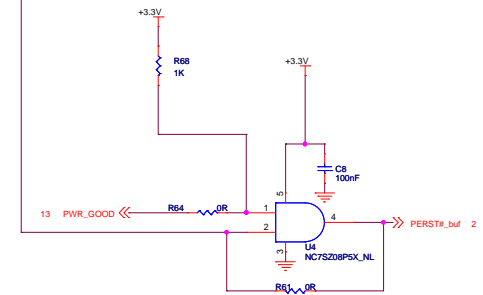
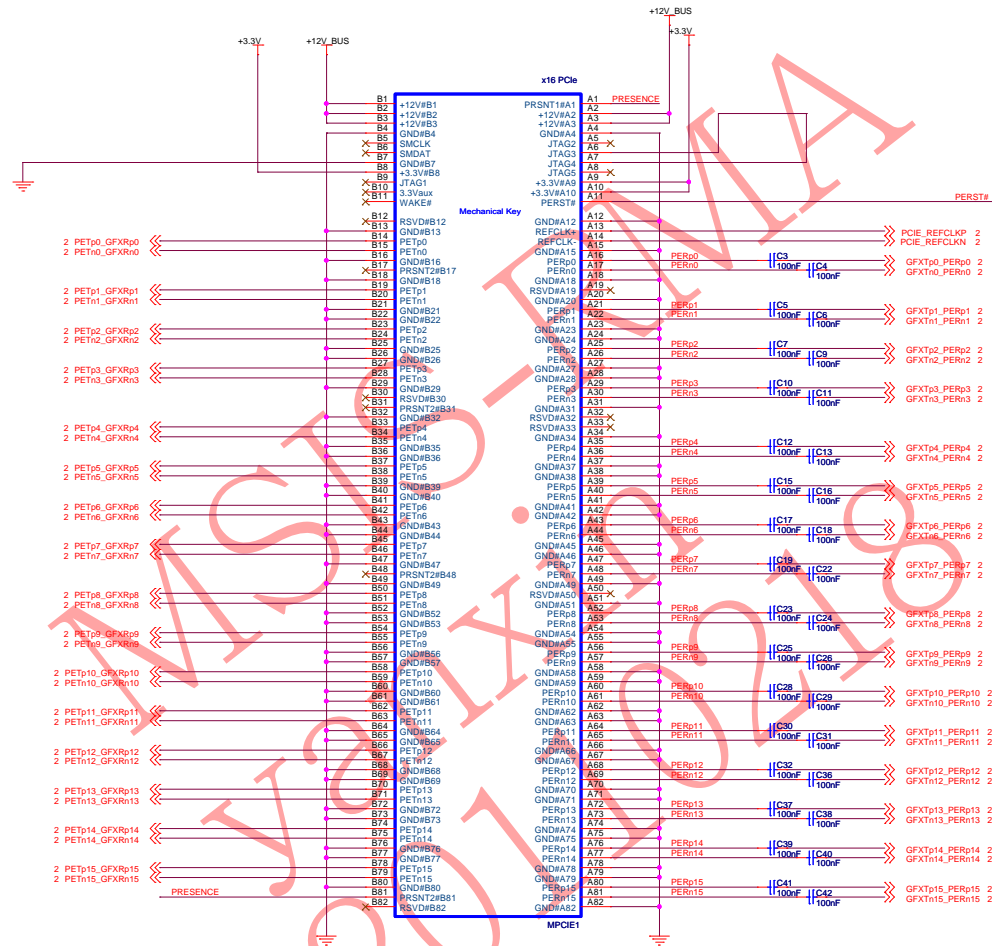
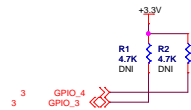


## PCI-EXPRESS EDGE CONNECTOR

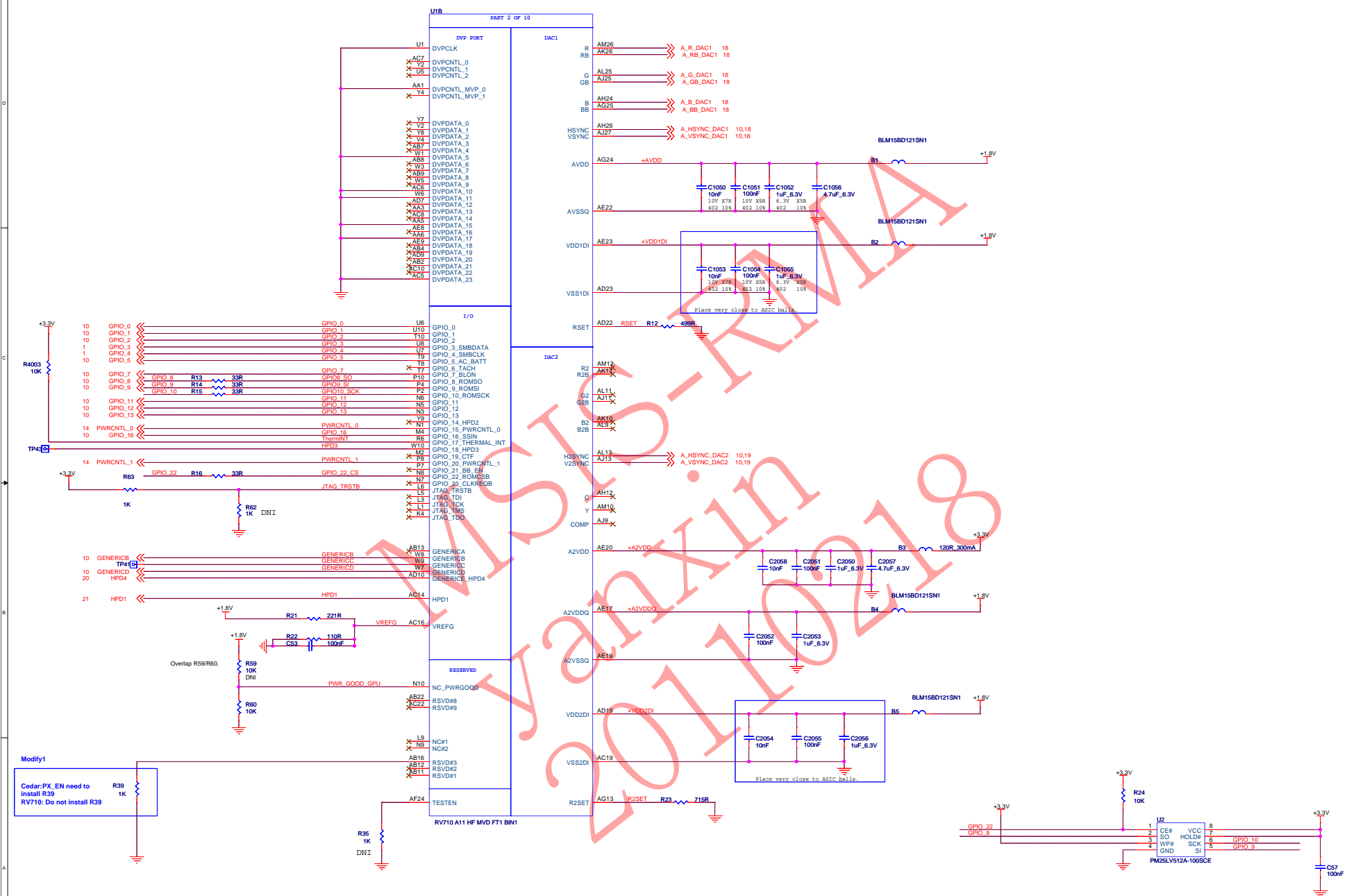



| SYMBOL LEGEND |                |
|---------------|----------------|
| DNI           | DO NOT INSTALL |
| #             | ACTIVE LOW     |
|               | DIGITAL GROUND |
|               | ANALOG GROUND  |

## (2) RV710 PCIe Interface

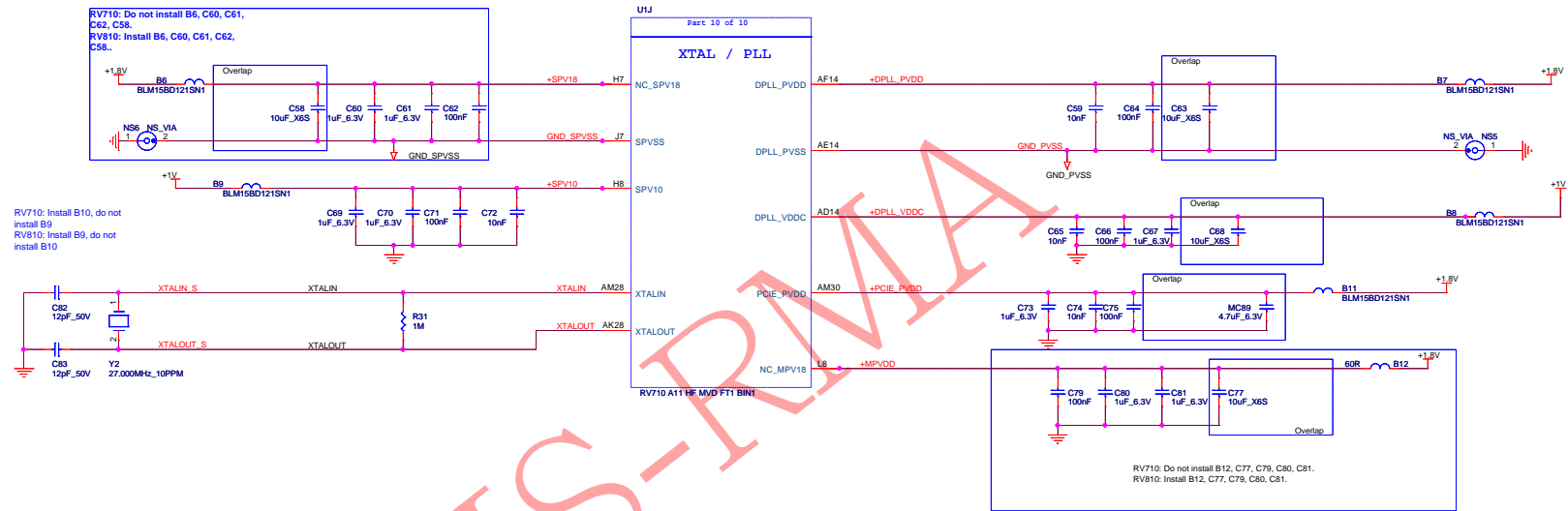


**(3) RV710 Main**



|  |  |   |  |   |  |
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| Sheet <u>3</u> of <u>25</u>  |  |   |  |   |  |
| Title <u>RH LP RV710 DDR3 QVA (header) HDMI DVI</u>  |  | Juc No. <u>105-B890X-X-00B</u>  |  |   |  |

# (04) RV710 GPIOs CF XTAL

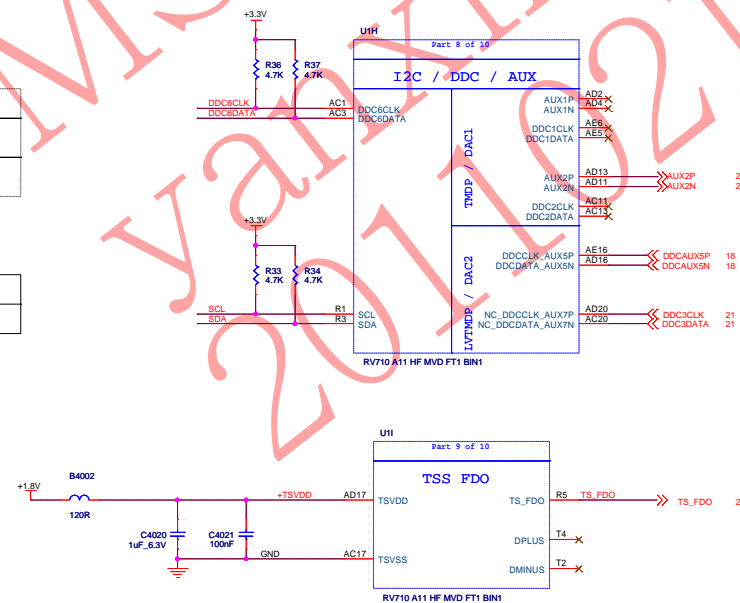


DDC6 BUS:

| I2C Address | Function                           | Device |
|-------------|------------------------------------|--------|
| 0x90        | I2C VDDC Control                   | DS4402 |
| 0x98        | LM63 - External Temperature Sensor | LM63   |

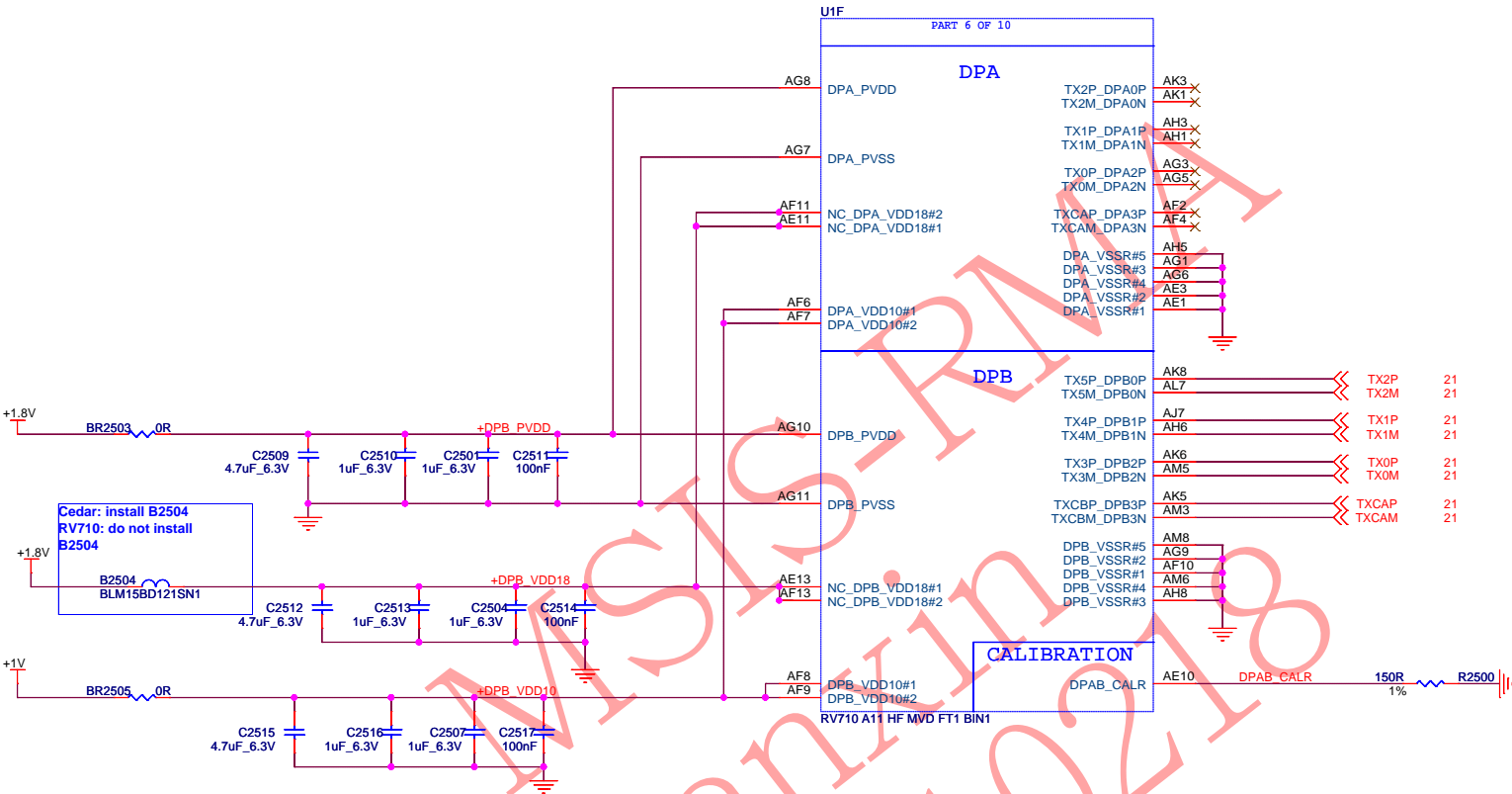
SCL / SDA BUS:

| I2C Address | Function | Device |
|-------------|----------|--------|
| N/A         | N/A      | N/A    |

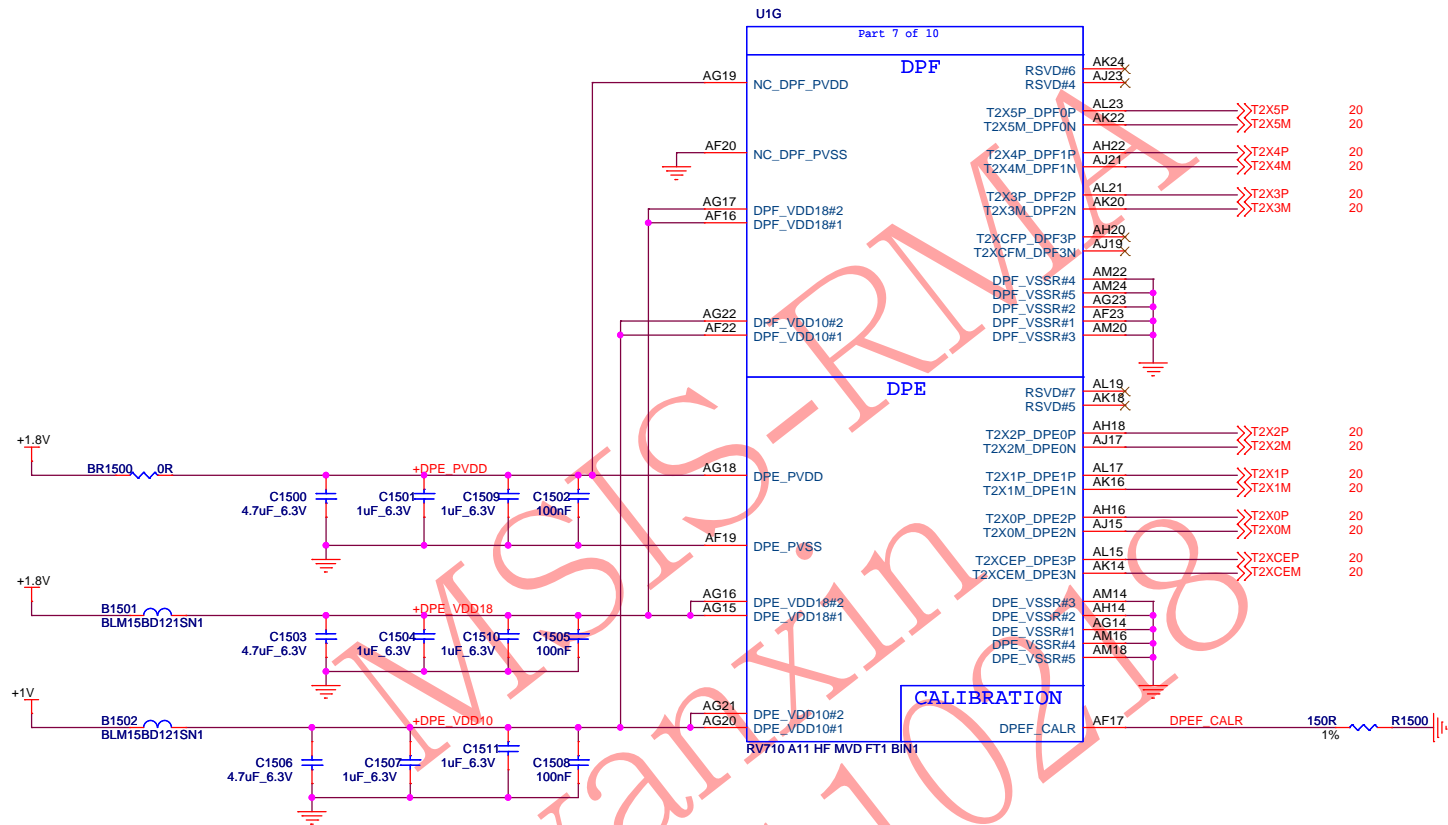


(05) RV710 TMDP A&B

TMDP INTERFACE

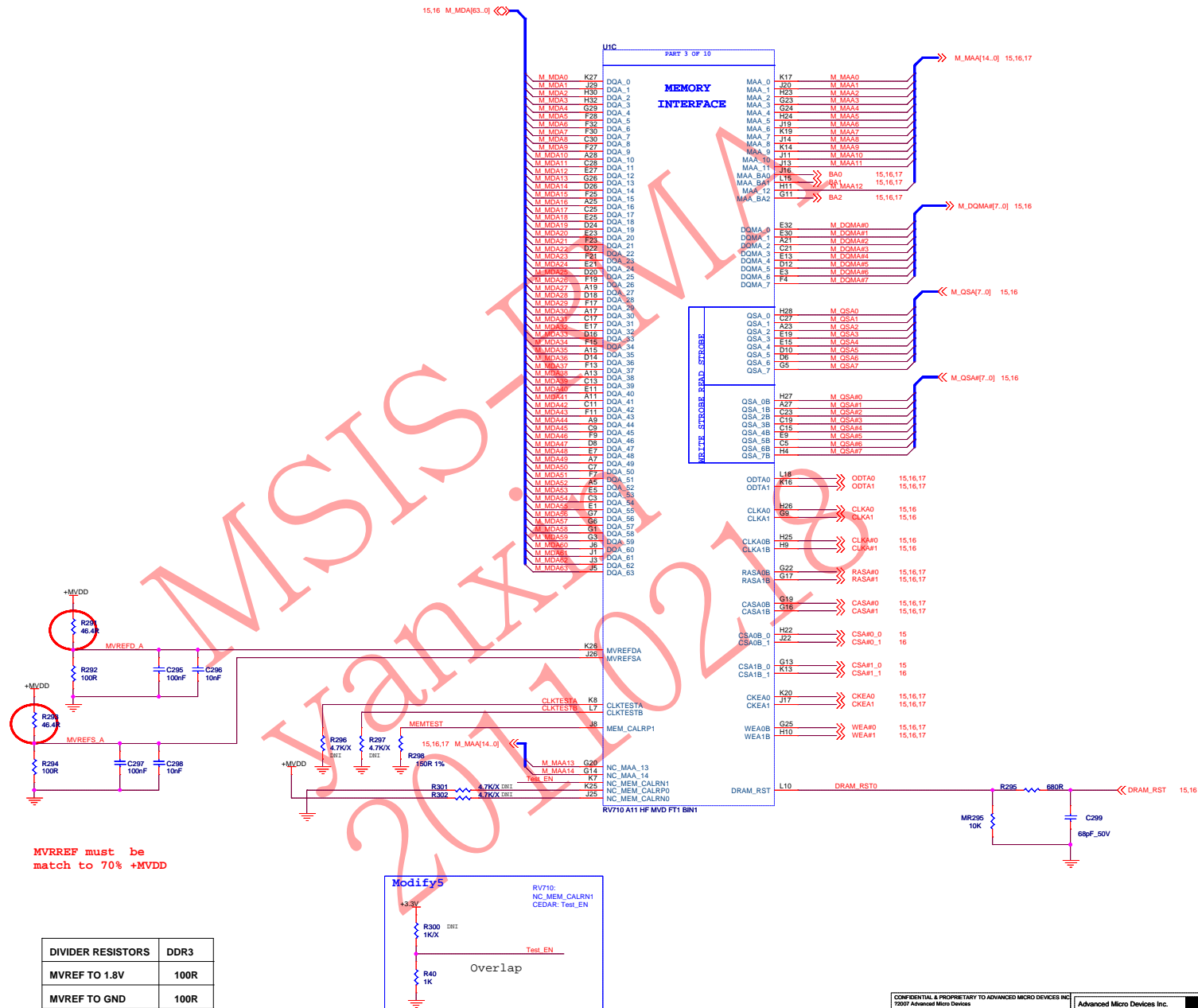


LVTMDP INTERFACE



### (07) RV710 MEM Interface Ch A

## MEMORY INTERFACE



|                   |      |
|-------------------|------|
| DIVIDER RESISTORS | DDR3 |
| MVREF TO 1.8V     | 100R |
| MVREF TO GND      | 100R |

Modify5

RV710:  
NC\_MEM\_CALRN1  
CEDAR: Test\_EN

+3.3V

R300 1KΩ

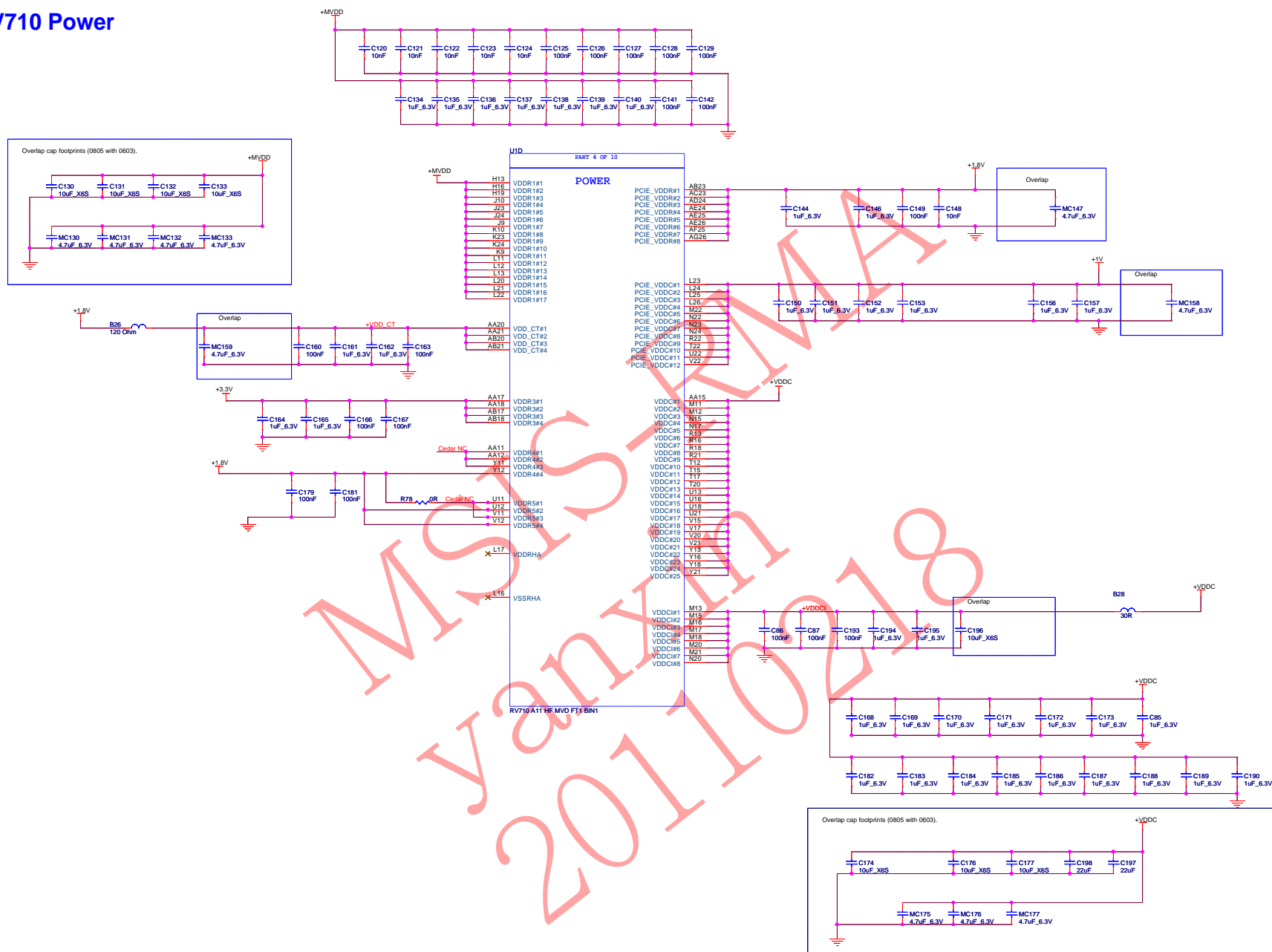
R40 1K

Test\_EN

Overlap

|  |  |
|--|--|
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### (08) RV710 Power

[illegible]



(09) RV710 GND

U1E  
PART 5 OF 10

GND

AA27 PCIE\_VSS#1  
AB24 PCIE\_VSS#2  
AC24 PCIE\_VSS#3  
AC26 PCIE\_VSS#4  
AC27 PCIE\_VSS#5  
AD25 PCIE\_VSS#6  
AD32 PCIE\_VSS#7  
AE27 PCIE\_VSS#8  
AF32 PCIE\_VSS#9  
AG27 PCIE\_VSS#10  
AH32 PCIE\_VSS#11  
K28 PCIE\_VSS#12  
K32 PCIE\_VSS#13  
L27 PCIE\_VSS#14  
M32 PCIE\_VSS#15  
N25 PCIE\_VSS#16  
N27 PCIE\_VSS#17  
P25 PCIE\_VSS#18  
P32 PCIE\_VSS#19  
R27 PCIE\_VSS#20  
T25 PCIE\_VSS#21  
T32 PCIE\_VSS#22  
U25 PCIE\_VSS#23  
U27 PCIE\_VSS#24  
V32 PCIE\_VSS#25  
W25 PCIE\_VSS#26  
W26 PCIE\_VSS#27  
W27 PCIE\_VSS#28  
Y25 PCIE\_VSS#29  
Y32 PCIE\_VSS#30  
Y32 PCIE\_VSS#31

A3 GND#1  
A30 GND#2  
AA13 GND#3  
AA16 GND#4  
AB10 GND#5  
AB15 GND#6  
AB6 GND#7  
AC9 GND#8  
AD6 GND#9  
AD8 GND#10  
AE7 GND#11  
AG12 GND#12  
AH10 GND#13  
AH28 GND#14  
B10 GND#15  
B12 GND#16  
B14 GND#17  
B16 GND#18  
B18 GND#19  
B20 GND#20  
B22 GND#21  
B24 GND#22  
B26 GND#23  
B6 GND#24  
B8 GND#25  
C1 GND#26  
C32 GND#27  
E28 GND#28  
F10 GND#29  
F12 GND#30  
F14 GND#31  
F16 GND#32

GND#33  
GND#34  
GND#35  
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GND#86  
GND#87  
GND#88  
GND#89

F18  
F2  
F20  
F22  
F24  
F26  
F6  
F8  
G10  
G27  
G31  
G8  
H14  
H17  
H2  
H20  
H6  
J27  
J31  
K11  
K2  
K22  
K6  
M6  
N11  
N12  
N13  
N16  
N18  
N21  
P6  
P9  
R12  
R15  
R17  
R20  
T13  
T16  
T18  
T21  
T6  
U15  
U17  
U20  
U3  
U9  
V13  
V16  
V18  
V6  
Y10  
Y15  
Y17  
Y20  
Y6  
T11  
R11

A32  
AM1  
AM32

VSS\_MECH#1  
VSS\_MECH#2  
VSS\_MECH#3

RV710 A11 HF MVD FT1 BIN1

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Sheet g of 25

Title RH LP RV710 DDR3 VGA (header) HDMI DVI  
Doc No. 105-B890XX-00B

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| Sheet <sub>g</sub> of <sub>25</sub>   |  |   |  |
| (r) HDMI DVI  |  | Doc No. 105-B890XX-00E  |  |

(10) RV710 STRAPS

PIN BASED STRAPS

|     |       |     |     |     |              |      |  |
|-----|-------|-----|-----|-----|--------------|------|--|
| DNI | +3.3V | DNI | R43 | 10K | A_VSYNC_DAC2 | 3,19 | VIP_DEVICE_STRAP_EN<br>0: Driver would ignore the value sampled on VHAD_0 during reset<br>1: Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no). |
|     |       | DNI | R44 | 10K | GPIO_9       | 3    | VGA DISABLE : 1 for disable (set to 0 for normal operation)  |
| DNI |       |     | R45 | 10K | GPIO_0       | 3    | GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)<br>0 : 50% Tx output swing for mobile mode<br>1: full Tx output swing (Default setting for Desktop)   |
| DNI |       |     | R46 | 10K | GPIO_1       | 3    | GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)<br>0: Tx de-emphasis disabled for mobile mode<br>1: Tx de-emphasis enabled (Default setting for Desktop)   |
| DNI |       |     | R47 | 10K | GPIO_2       | 3    | GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)<br>0 : Default. (Driver Controlled Gen2)<br>1 : Strap Controlled Gen2  |
| DNI |       |     | R48 | 10K | GPIO_11      | 3    | GPIO(13, 12, 11) - CONFIG[2..0]<br>100 - 512Kbit M25P05A (ST)<br>101 - 1Mbit M25P10A (ST)<br>101 - 2Mbit M25P20 (ST)<br>101 - 4Mbit M25P40 (ST)<br>101 - 8Mbit M25P80 (ST)<br>100 - 512Kbit Pm25LV512 (Chingis)<br>101 - 1Mbit Pm25LV010 (Chingis)                           |
| DNI |       | DNI | R49 | 10K | GPIO_13      | 3    |  |
| DNI |       | DNI | R50 | 10K | GPIO_12      | 3    |  |
|     |       |     |     |     |              |      |  |
| DNI |       |     | R51 | 10K | A_VSYNC_DAC1 | 3,18 | AUD[0]   |
|     |       |     | R52 | 10K | A_HSYNC_DAC1 | 3,18 | AUD[1]   |
|     |       | DNI | R53 | 10K | GPIO_8       | 3    | BIF_CLK_PM_EN<br>0 - Disable CLKREQ# power management capability<br>1 - Enable CLKREQ# power management capability   |
|     |       |     | R54 | 10K | GPIO_5       | 3    | GPIO_5 : GPIO_16]  |
|     |       | DNI | R55 | 10K | GPIO_16      | 3    | Quimonda [0:0]<br>Hynix [0:1]<br>Samsung [1:0]   |
|     |       | DNI | R56 | 10K | A_HSYNC_DAC2 | 3,19 | RESERVED :Internal use only. Other logic must not affect this signal during RESET.   |
|     | NTSC  |     | R57 | 10K | GPIO_7       | 3    | TV OUT STANDARD 0 - PAL TVO 1 - NTSC TVO   |
| DNI |       |     | R70 | 10K | GENERICB     | 3    | GenericB and GenericD will be used for additional memory vendor straps.  |
| DNI |       |     | R71 | 10K | GENERICD     | 3    |  |

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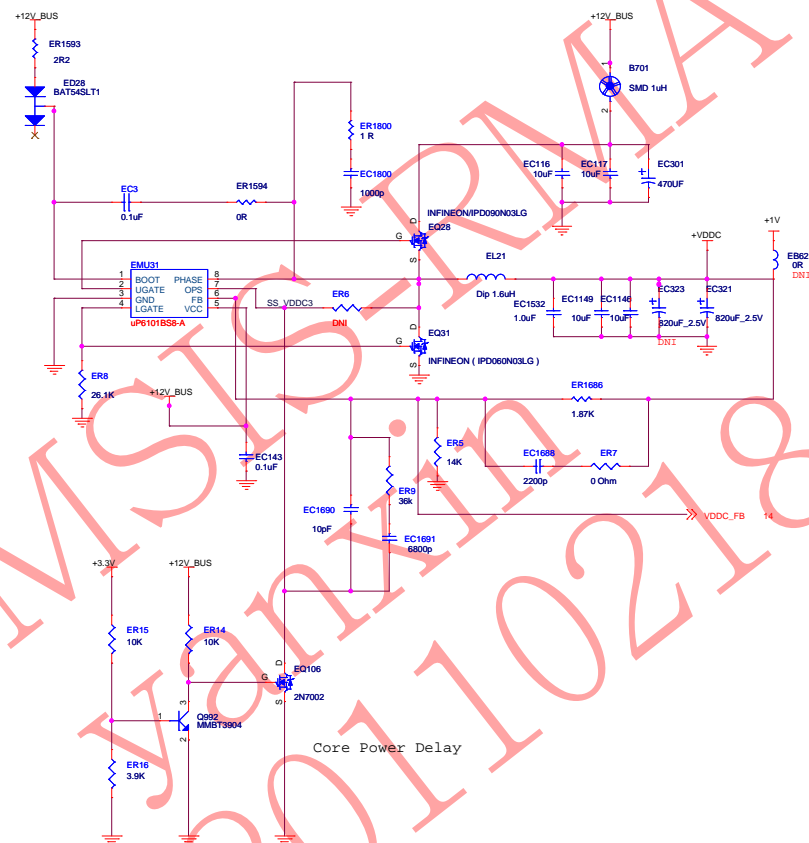
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Sheet 10 of 25

Doc No. 105-B890XX-00B

**(11) VDDC**



Core Power Delay

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Sheet 11 of 25

|         |                |
|---------|----------------|
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|---------|----------------|

Title RH LP RV710 DDR3 VGA (header) HDMI DVI

(12) MVDD

+12V\_BUS

Vin I rms = 5.8A @ 1.8V/15A

Vout Irripple = 5.3A @ 300kHz

$$+MVDD = 0.8 * \left( 1 + \left( \frac{ER12}{ER13} \right) \right)$$

Memory Power Seq

|  |  |   |  |
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| Title: RH LP RV710 DDR3 VGA (header) HDMI DVI  |  | Doc No.: 105-B890XX-00B   |  |

**(12) MVDD**

+12V\_BUS

ER1596  
2R2  
R11-02A014-W08

ED2  
BAT54S  
D01-BAT54S-P15

ER1801  
1R  
R11-0010034-W08

EC1801  
1000pF  
C11-4021013-S02

ER1596  
R11-000034-Y01  
OR

EC124  
0.1uF  
C11-1042813-W08  
ER307  
OR

EMJ42  
1 2 3 4 5 6 7 8  
BOOT UGATE OPS FB LGATE VCC

UG\_M  
UG\_R\_M  
PHASE\_M  
OPS\_M  
LG\_R\_M  
FB\_M

INFINEON (IPD090N03LG)  
D03-90N031B-H14

EL64  
Dip 1.8uH

EQ40  
EQ41

INFINTEON (IPD090N03LG)  
D03-90N031B-H14

ER10  
R11-154713-W08  
DNI

ER20  
10K  
R11-0103T13-W08

Rimp

+12V\_BUS

EC168  
0.1uF  
C11-1042013-W08

GND

ER13  
1.78K  
R11-1781T13-W08

ER12  
1.82K  
R11-821T23-Y01

EC7  
2200pF  
C11-222023-W08

ER11  
5.0K  
R11-086CT13-W08

DNI DNI

EC164  
10uF  
C11-1063047-W08

EC159  
10uF  
C11-1067517-S02

EC169  
10uF  
C11-1063027-Y01

EC346  
10uF  
C11-1063027-Y01

EC347  
10uF  
C11-1063027-Y01

EC348  
10uF  
C11-1063027-Y01

EC184  
1000pF  
C04-1000E1-A07

C1034  
100pF  
C11-1011512-W08

C1035  
100pF  
C11-1011512-W08

C1036  
100pF  
C11-1011512-W08

C1038  
1000pF  
C11-1022082-W08

C1039  
1000pF  
C11-1022082-W08

C1040  
1000pF  
C11-1022082-W08

C1042  
10nF  
C11-1032082-W08

C1043  
10nF  
C11-1032082-W08

C1044  
10nF  
C11-1032082-W08

GND

Vin Irms = 5.8A @ 1.8V/15A

+MVDD

Vout Irripple = 5.3A @ 300kHz

+VDDC

ER19  
1K  
DNI

ER17  
10K  
DNI

EQ107  
2N7002

DNI

C993  
MMST3904

ER18  
10K  
DNI

Memory Power Seq

$$+MVDD = 0.8 * ( 1 + ( ER12 / ER13 ) )$$

+3.3V

C995  
10uF

C996  
10uF

C997  
10uF

+3.3V

C1012  
100pF

C1014  
100pF

C1015  
100pF

+3.3V

C998  
1000 pF

C999  
1000 pF

C1000  
1000 pF

+3.3V

C1017  
10nF

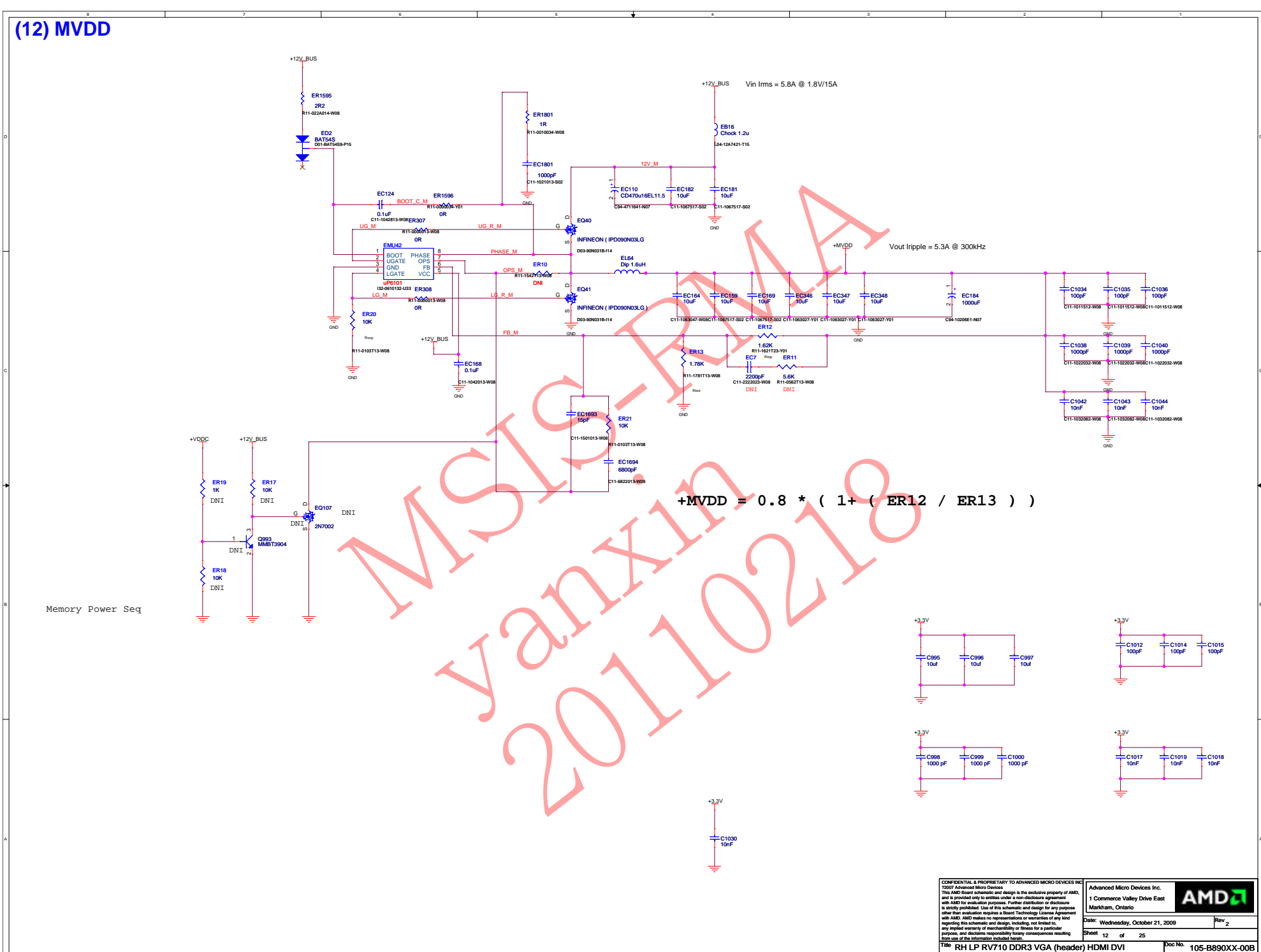
C1019  
10nF

C1018  
10nF

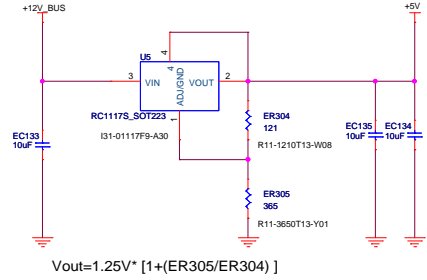
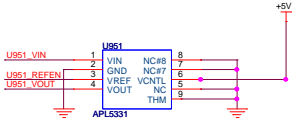
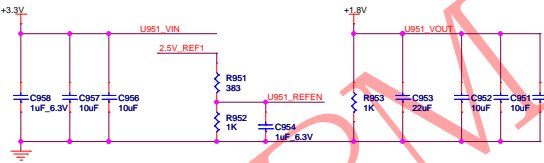
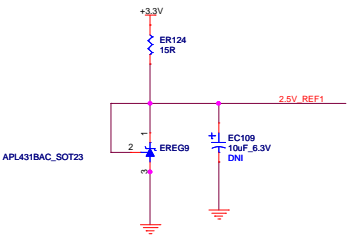
+3.3V

C1030  
10nF

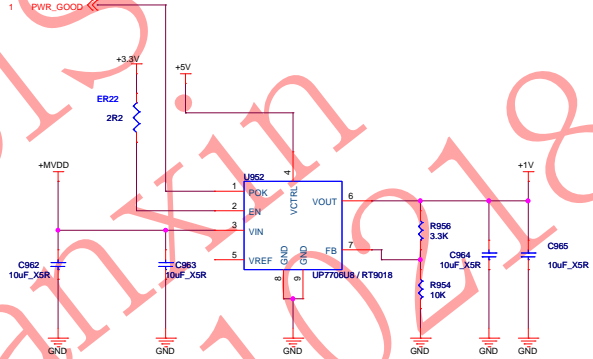
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| Sheet:   | 12 of 25                    | Title   |   | RH LP RV710 DDR3 VGA (header) HDMI DVI |  |
| Doc No.  |                             | 105-B890XX-00B  |   |  |  |

[illegible]

(13) Linear Regulators

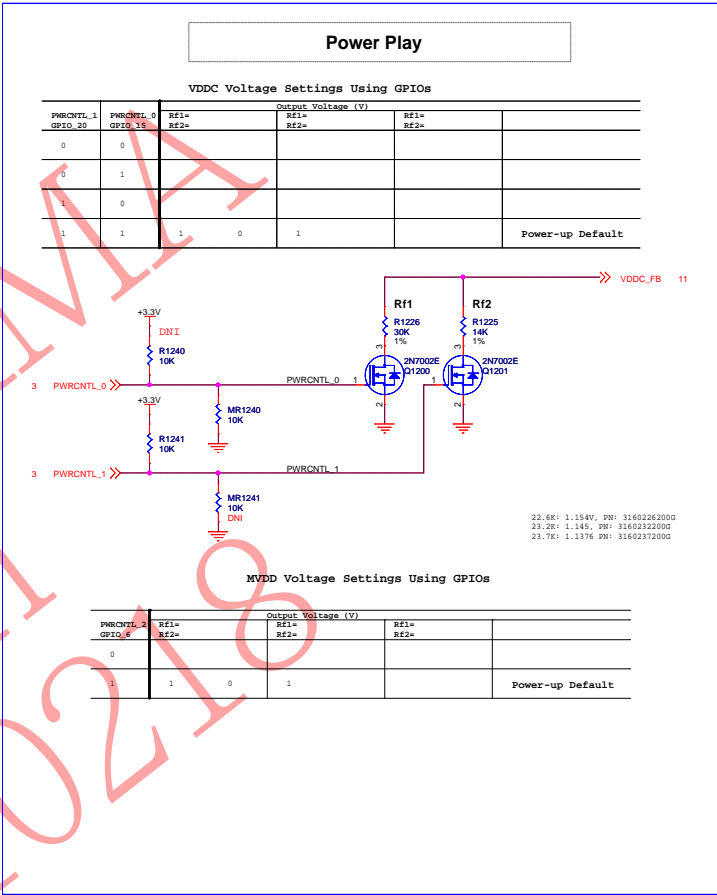
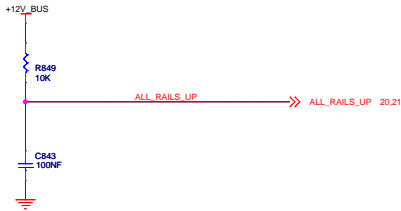


$$V_{out} = 1.25V * [1 + (ER305/ER304)]$$

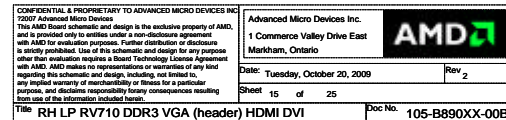


$$V_{out} = 0.8V * (1 + R956 / R954)$$

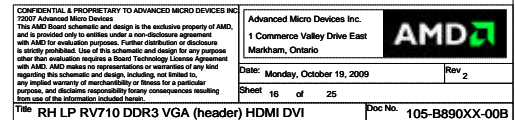
(14) Power Management



**RANK1: 256MB/512MB DDR3**

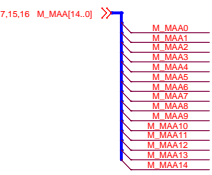
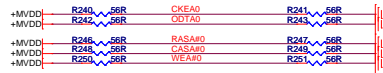


**RANK2: 256MB/512MB DDR3**





(17) DDR3 Termination

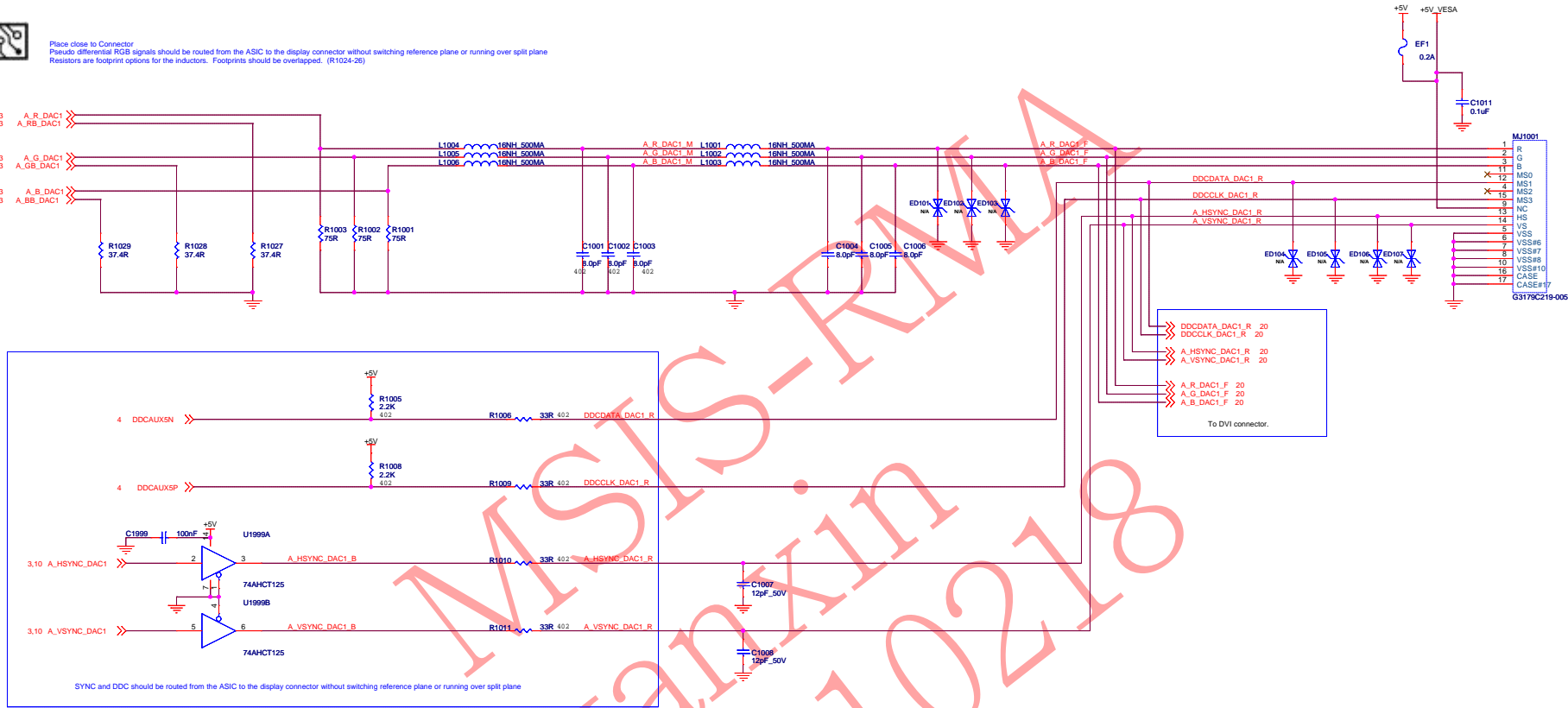


(18) DAC1 OUTPUT

DAC 1 OUTPUT



Place close to Connector  
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane  
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)



(19) DAC2 OUTPUT

DAC 2 OUTPUT

Optional ESD Protection Diodes

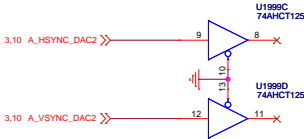
Place near D2002, D2003, D2004, D2005



Place close to Connector  
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane

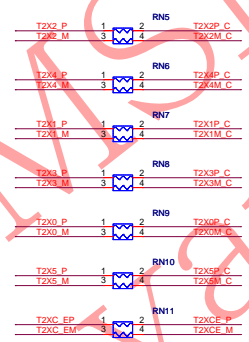
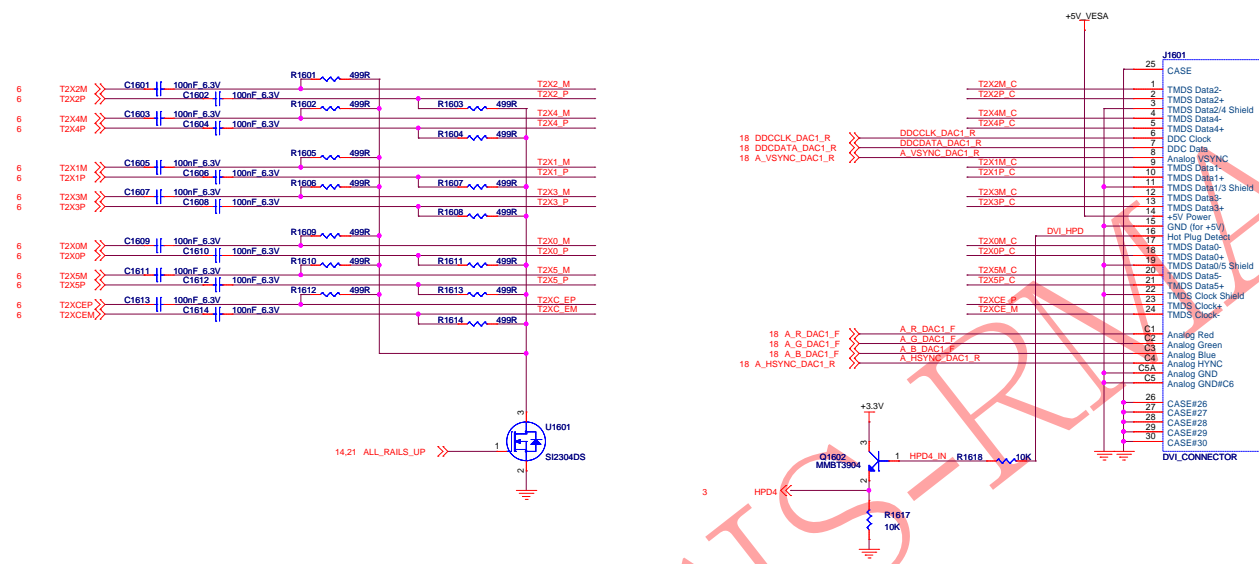
RV710: DDC2 is 5V tolerant. Do not install level shifter.  
--> Do not install R2013, R2015, Q2001, Q2002. Install R2014, R2016.  
RV810: DDC2 is NOT 5V tolerant. Install level shifter.  
--> Do not install R2014, R2016. Install R2013, R2015, Q2001, Q2002.

Remove VGA RIBBON CONNECTOR  
2009/09/23



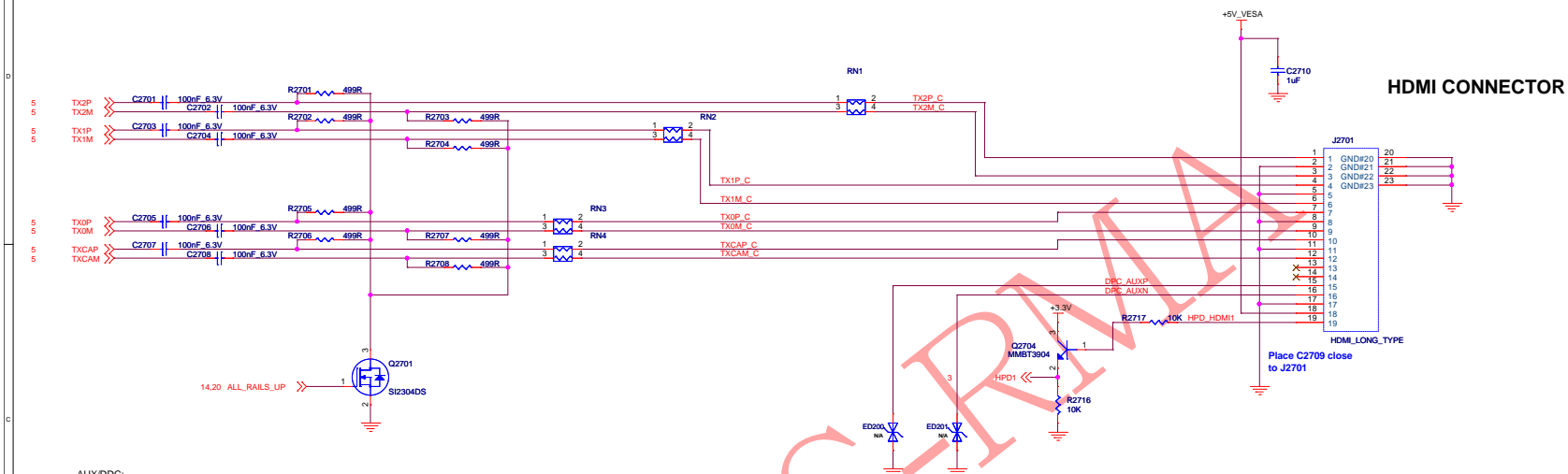
(20) DVI OUTPUT

DPE / DPF OUTPUT



**(21) HDMI OUTPUT**

## TMDP-B OUTPUT

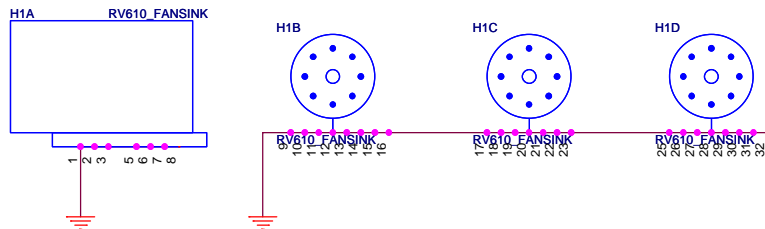


AUX/DDC:  
FOR 740/730, INSTALL OR ON ASIC-SIDE OF AC COUPLING CAPS ONLY;  
FOR JUNIPER, INSTALL OR ON CONNECTOR SIDE OF AC COUPLING CAPS ONLY;

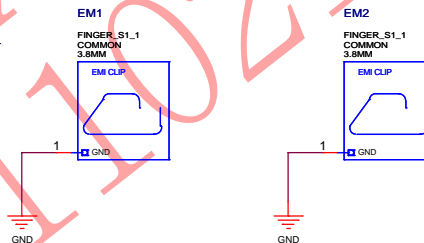
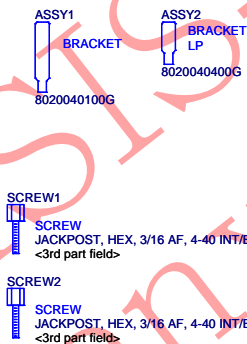
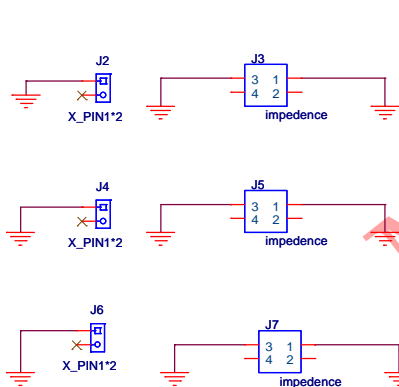
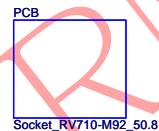
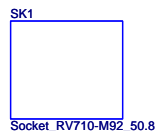


Optional ESD protection diodes





7120036200G



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 Markham, Ontario



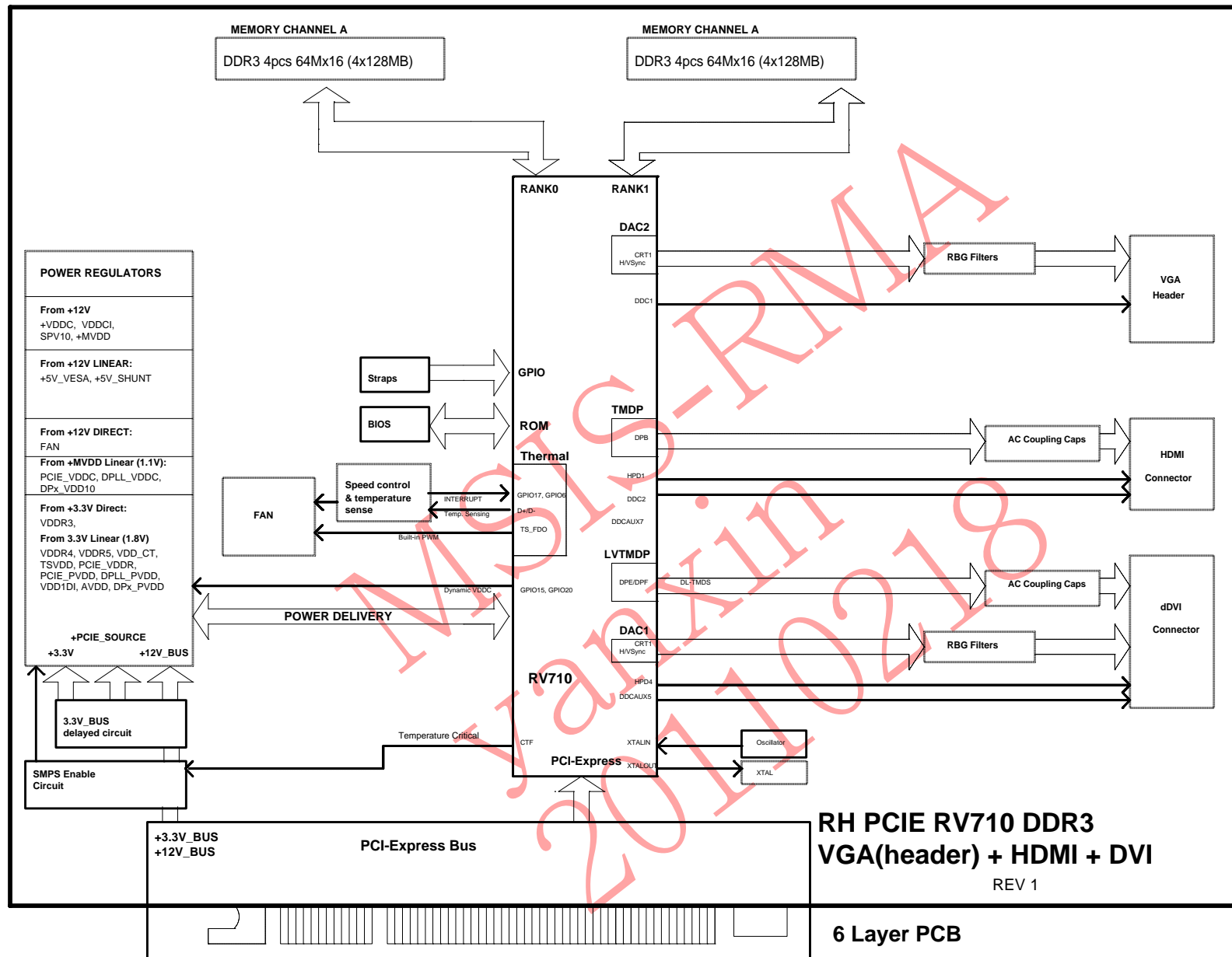
Date: Tuesday, October 20, 2009

Rev 2

Sheet 23 of 25

Title RH LP RV710 DDR3 VGA (header) HDMI DVI


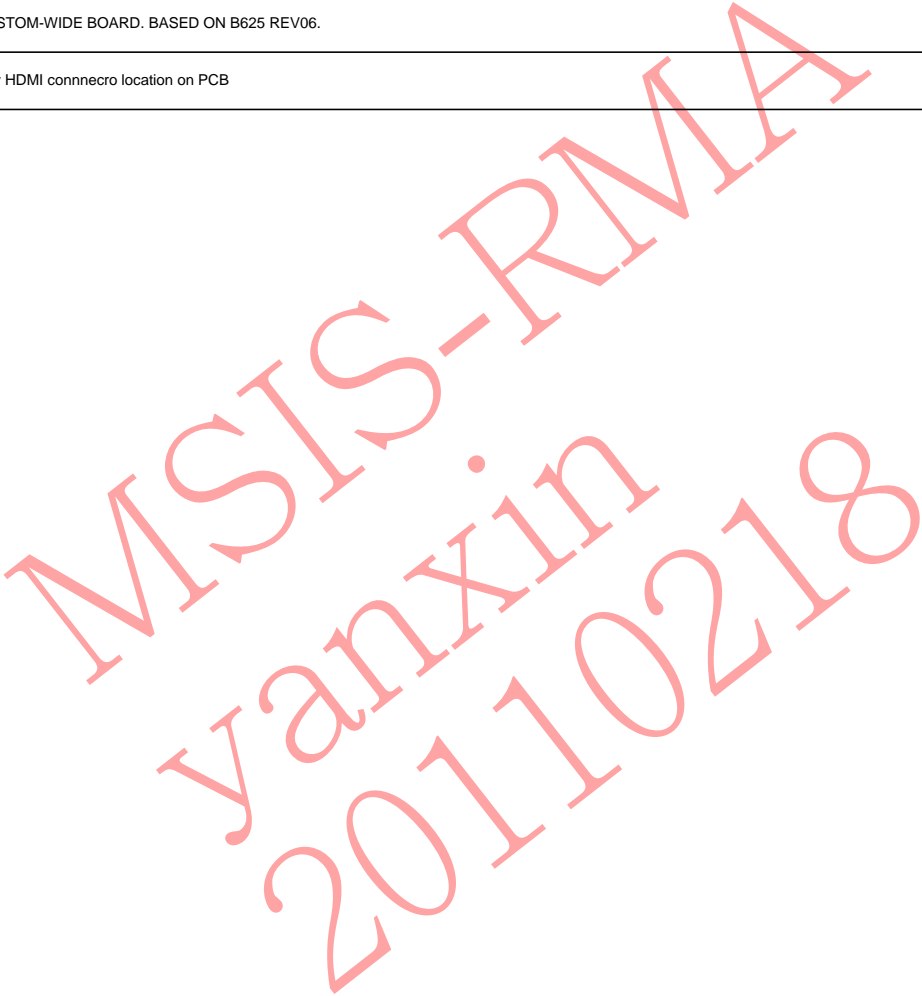
Doc No. 105-B890XX-00B



**RH PCIE RV710 DDR3  
VGA(header) + HDMI + DVI**  
REV 1

**6 Layer PCB**



|  |   |         |   |  |   |  |  |  |                                   |  |   |  |  |  |  |  |  |  |  |  |   |
|--|---|---------|---|--|---|--|--|--|-----------------------------------|--|---|--|--|--|--|--|--|--|--|--|---|
| 5  |   |         | 4   |  | 3 |  | 2  |  | 1                                 |  |   |  |  |  |  |  |  |  |  |  |   |
|  |   |         | Title<br>RH LP RV710 DDR3 VGA (header) HDMI DVI |  |   |  | Schematic No.<br>105-B890XX-00B  |  | Date:<br>Monday, October 19, 2009 |  |   |  |  |  |  |  |  |  |  |  |   |
|  |   |         | REVISION HISTORY                                |  |   |  | NOTE: This schematic represents the PCB, it does not represent any specific SKU.<br>For Stuffing options (component values, DNI  s? please consult the product specific BOM.<br>Please contact AMD representative to obtain latest BOM closest to the application desired. |  | Rev 2                             |  |   |  |  |  |  |  |  |  |  |  |   |
| D  | Sch Rev   | PCB Rev | Date  | RV710 ENGINEERING BOARD REVISION DESCRIPTION               |   |  |  |  |                                   |  | D |  |  |  |  |  |  |  |  |  |   |
|  | 0   | 00A     | 2008.12.30                                      | INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06. |   |  |  |  |                                   |  |   |  |  |  |  |  |  |  |  |  |   |
|  | 1   | 00B     | 2009.01.22                                      | Sch no change. just modify HDMI connnecro location on PCB  |   |  |  |  |                                   |  |   |  |  |  |  |  |  |  |  |  |   |
| C  |  |         |   |  |   |  |  |  |                                   |  | C |  |  |  |  |  |  |  |  |  |   |
| B  |   |         |   |  |   |  |  |  |                                   |  |   |  |  |  |  |  |  |  |  |  | B |
| A  |   |         |   |  |   |  |  |  |                                   |  |   |  |  |  |  |  |  |  |  |  | A |
| 5  |   |         | 4   |  | 3 |  | 2  |  | 1                                 |  |   |  |  |  |  |  |  |  |  |  |   |