

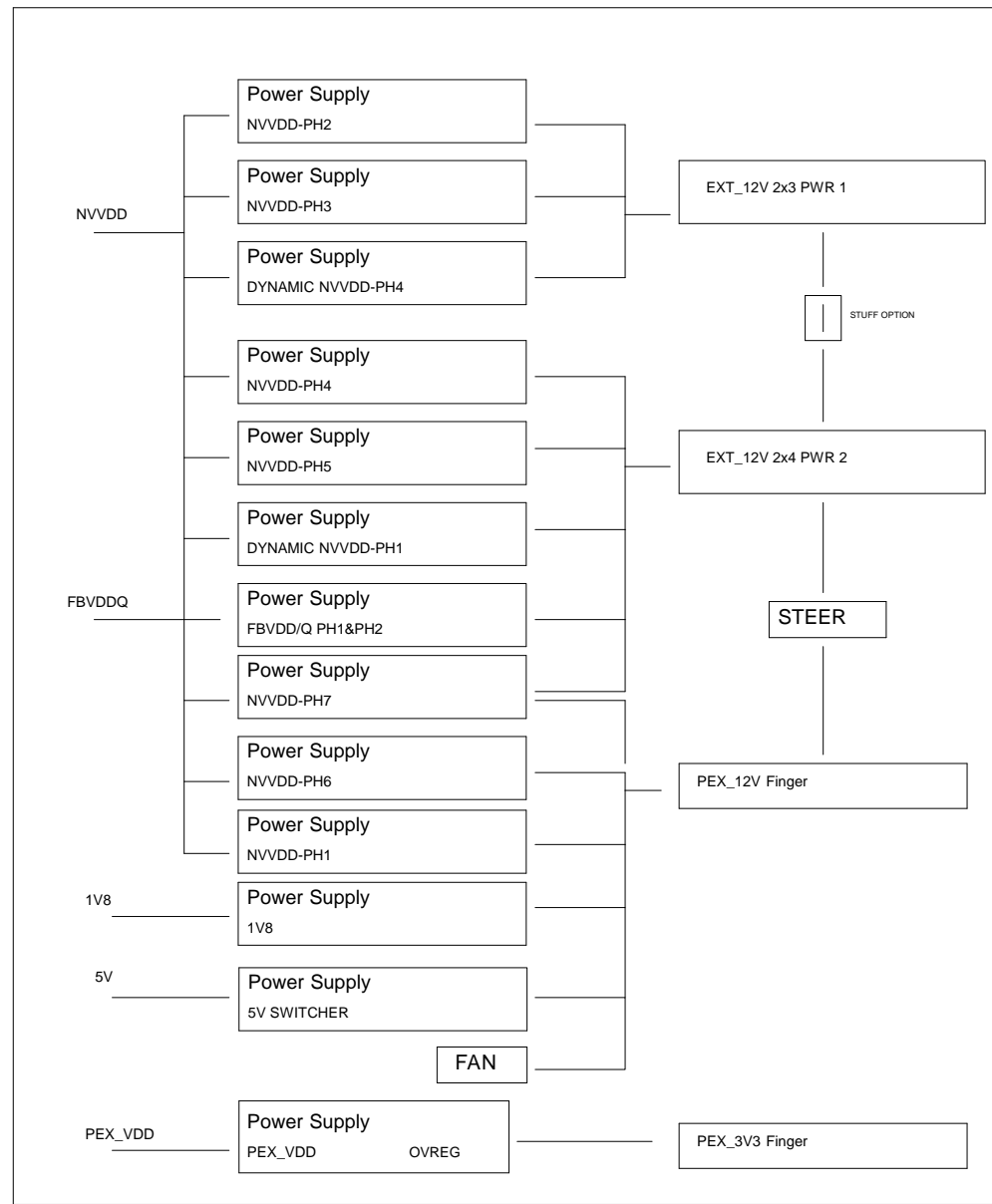
PG611 A00

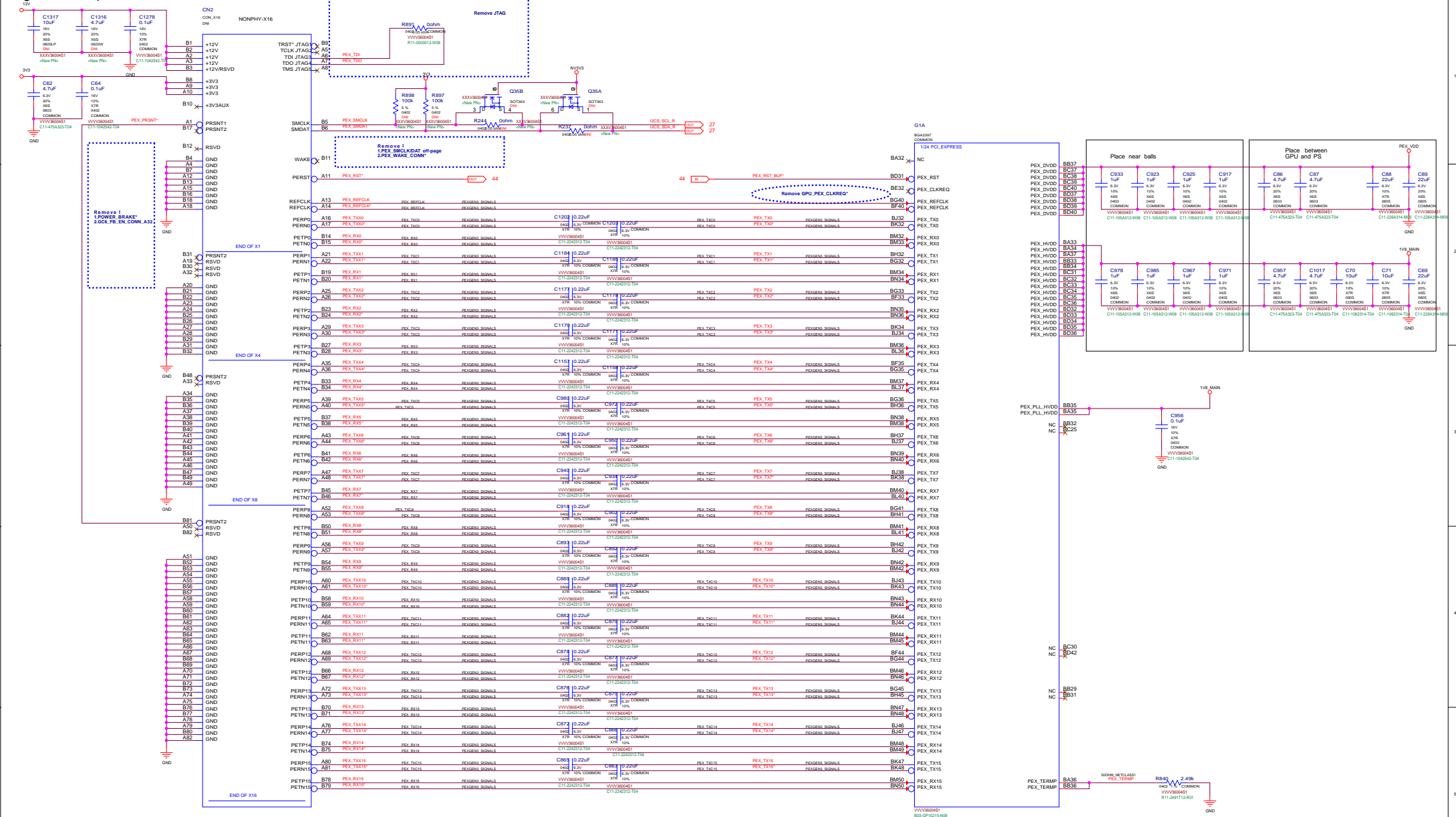
12GB GDDR5X, 384b, 256Mx32

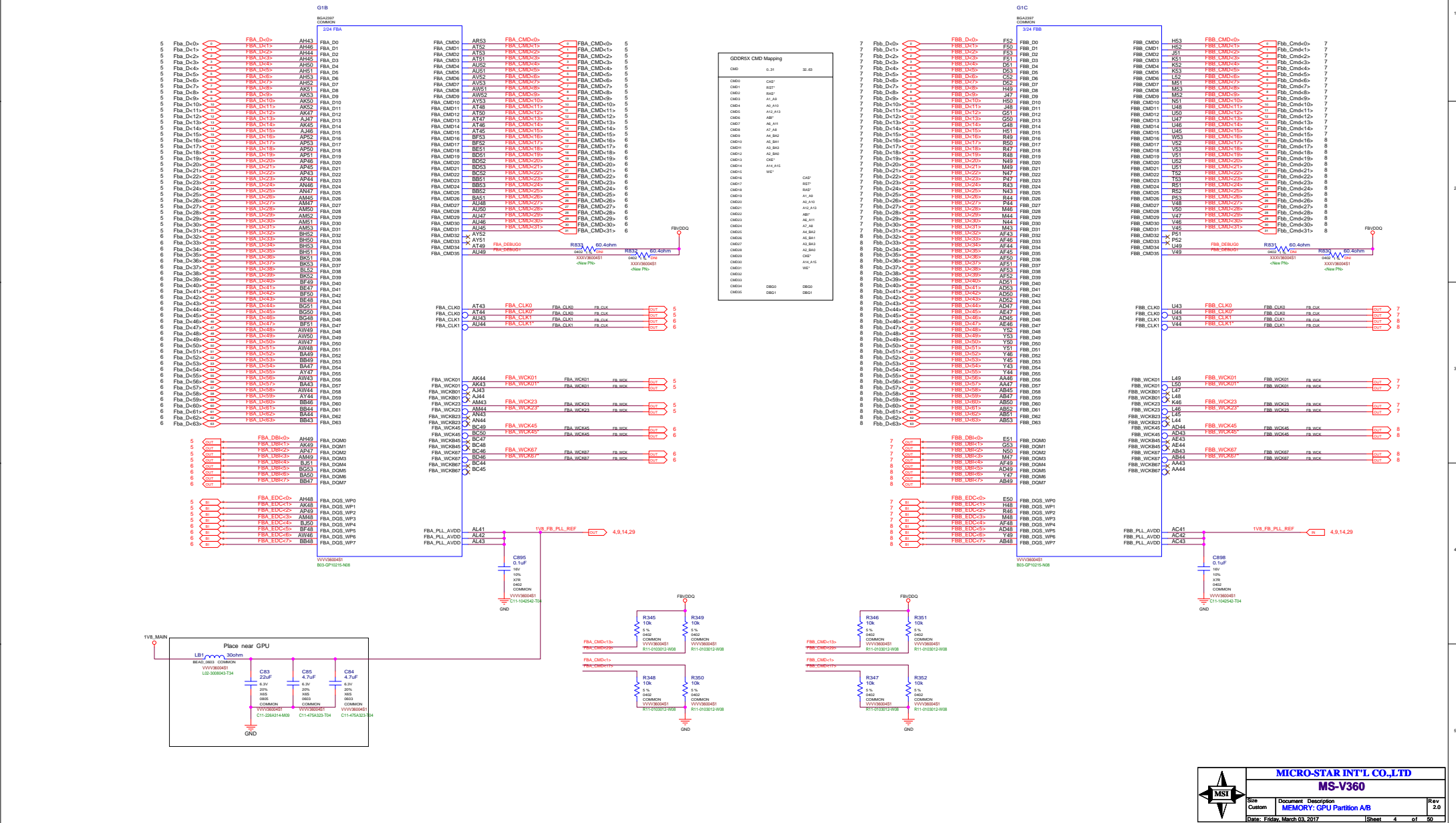
TALL DVI-D + DP + DP + HDMI/DP + DP

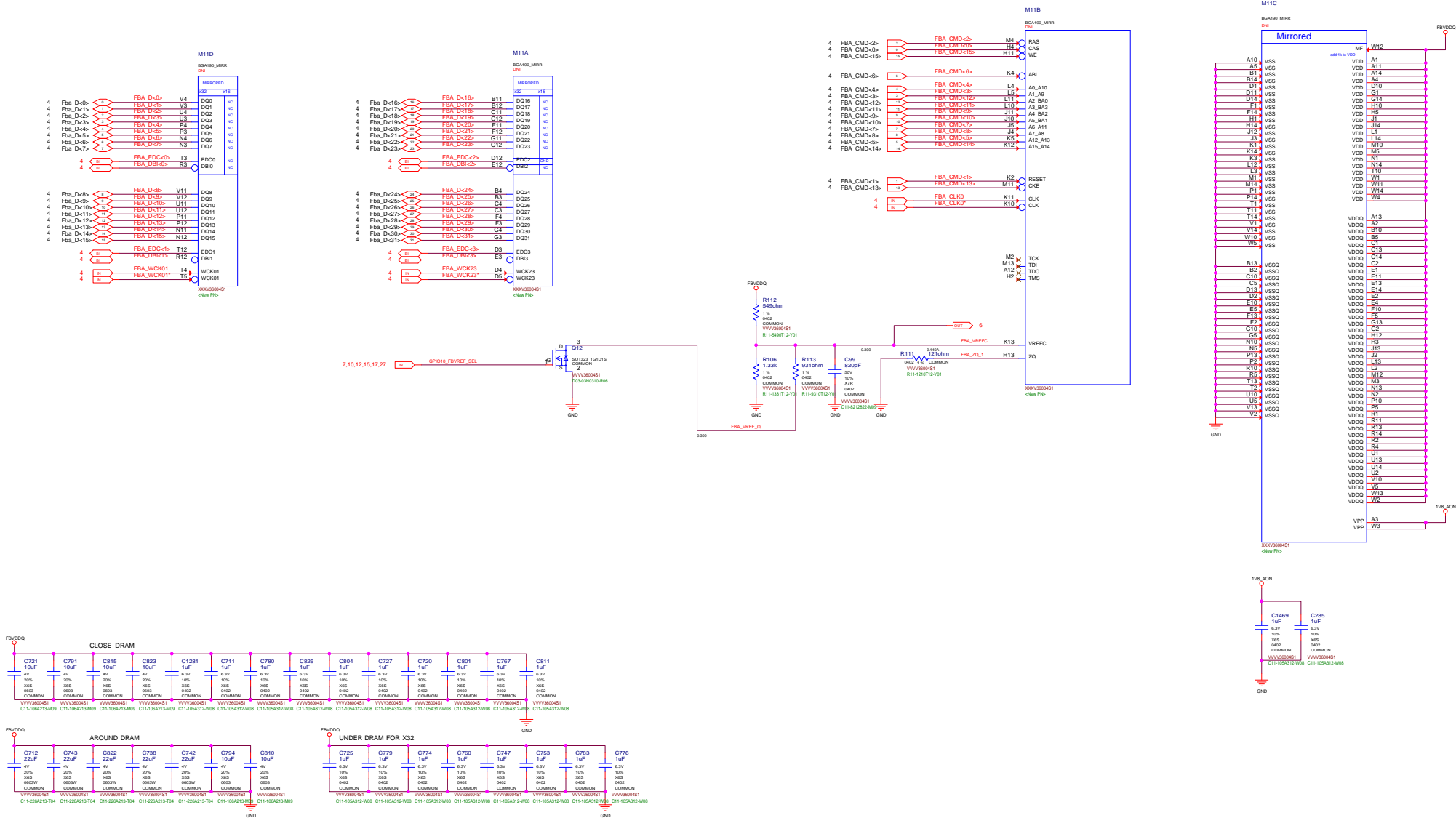
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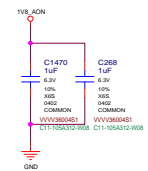
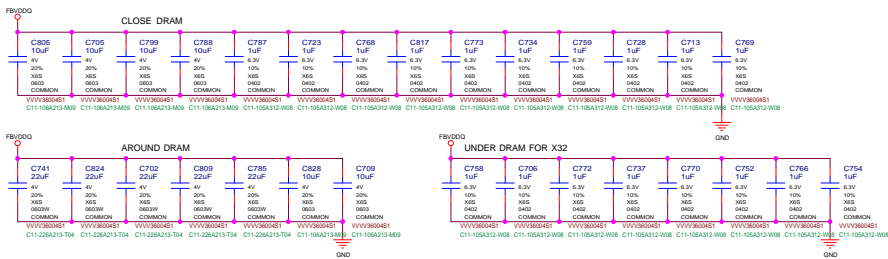
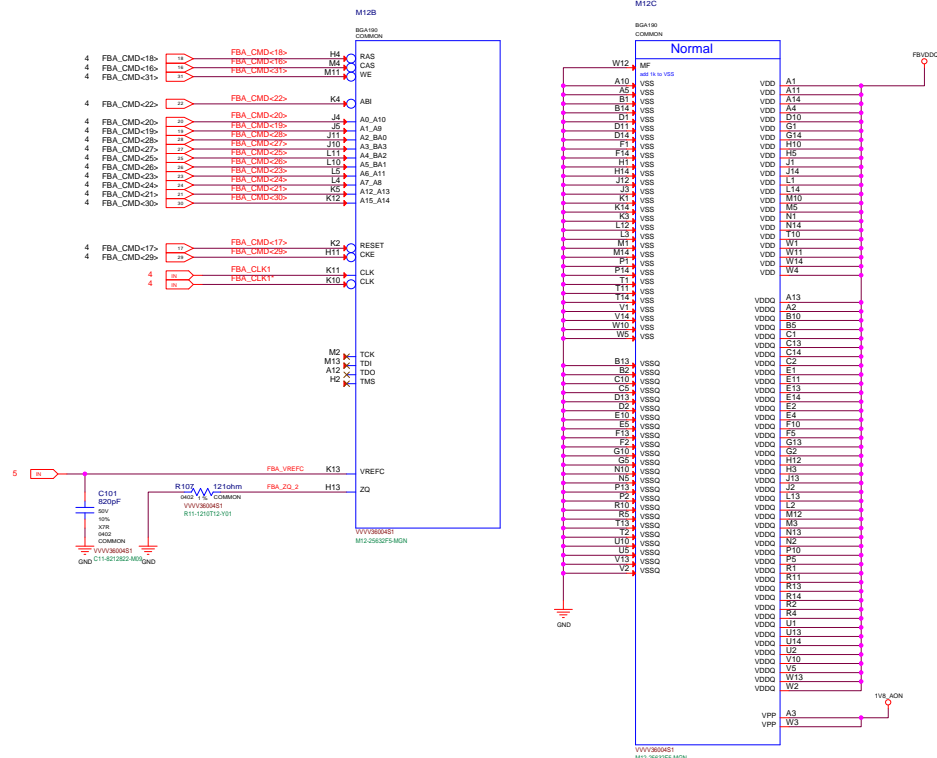
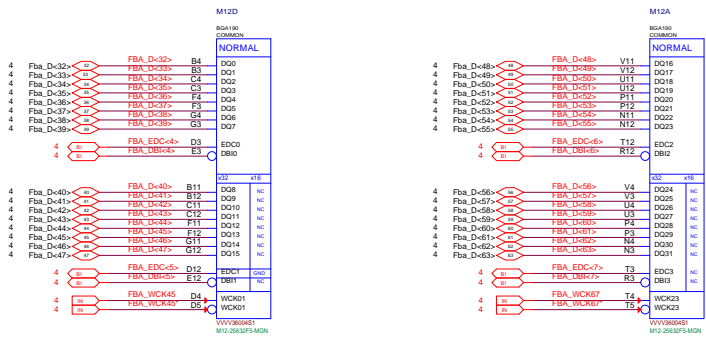
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| 24 | IFPC HDMI/DP | 49 | VR Thermal Protection |
| 25 | IFPD DP | | |

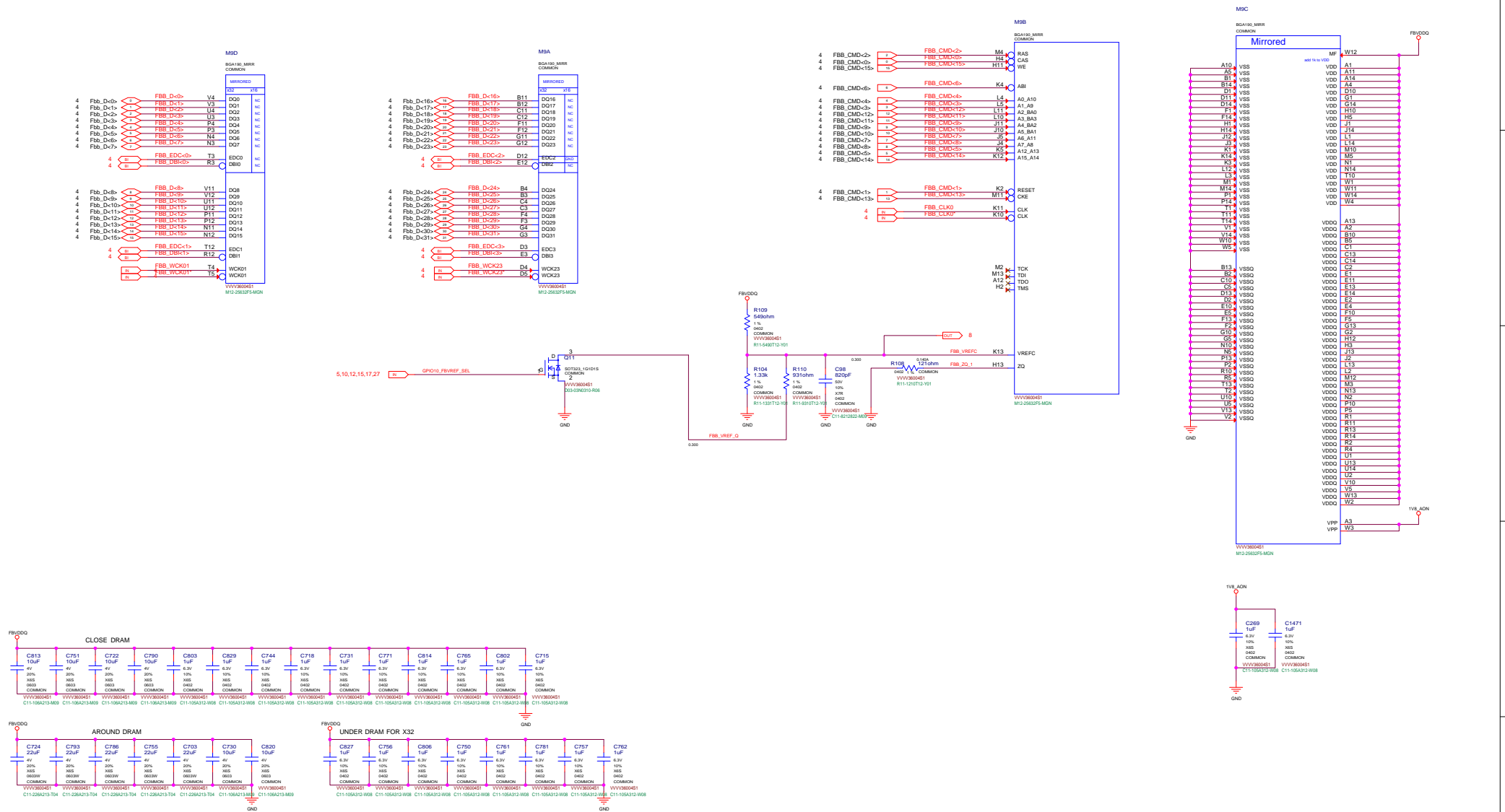


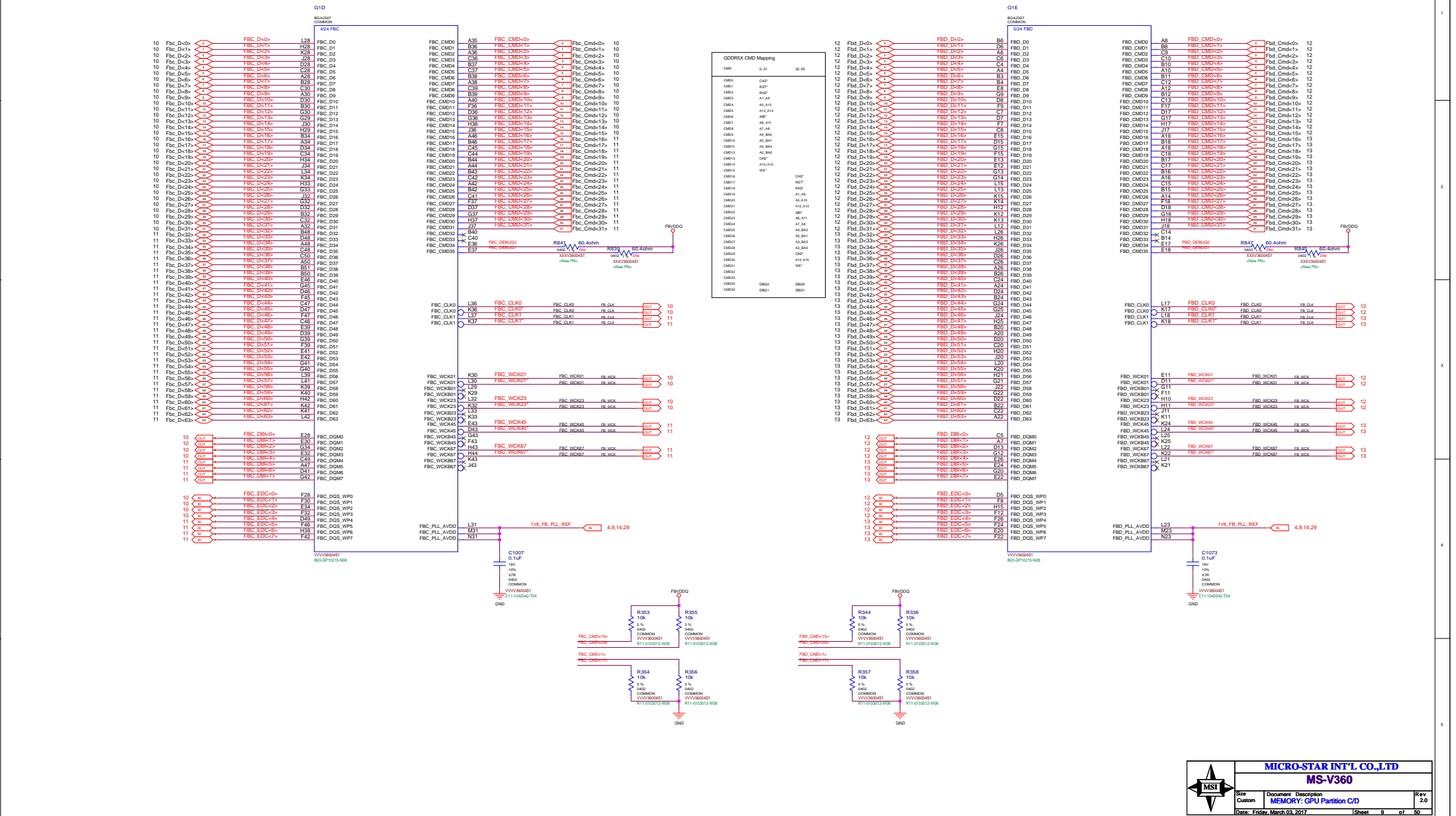


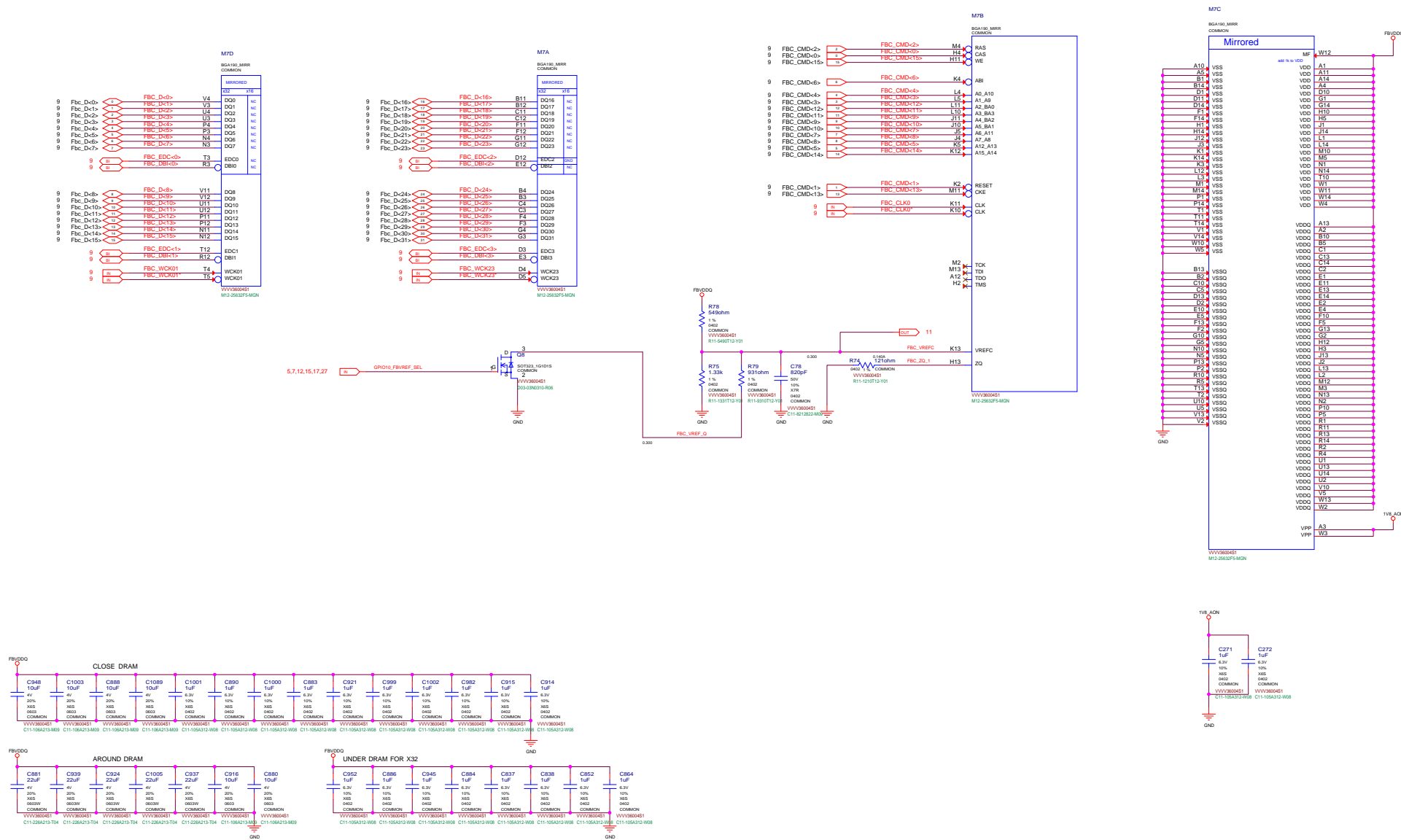


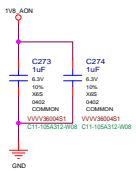
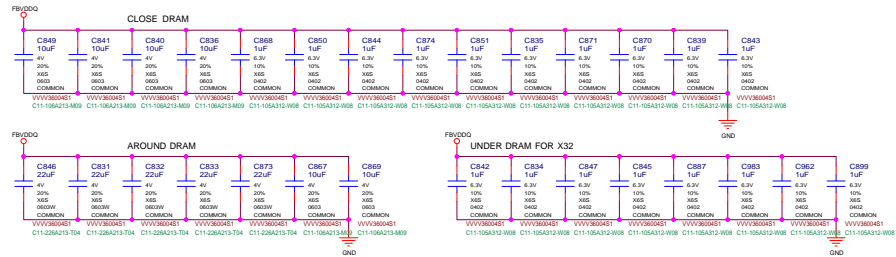
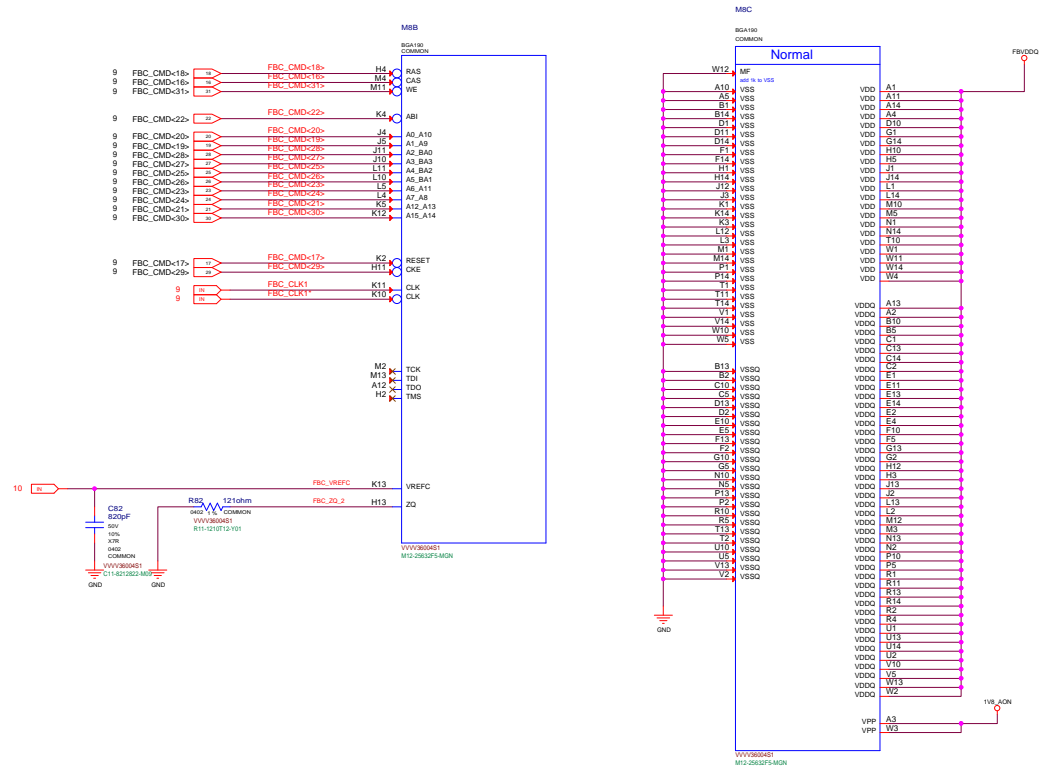
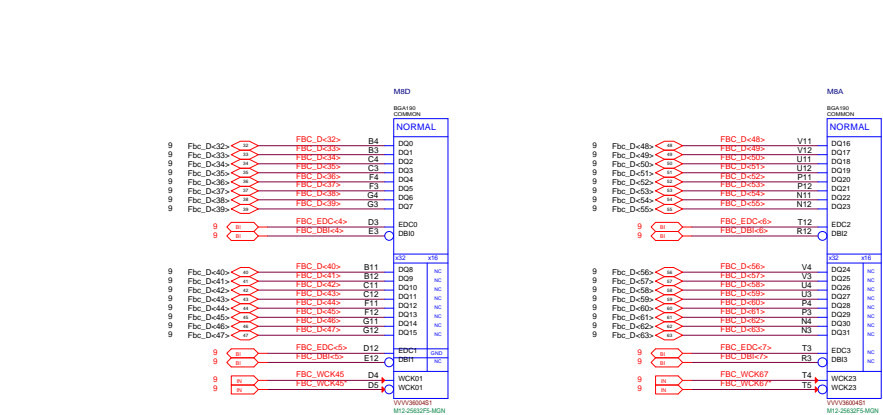






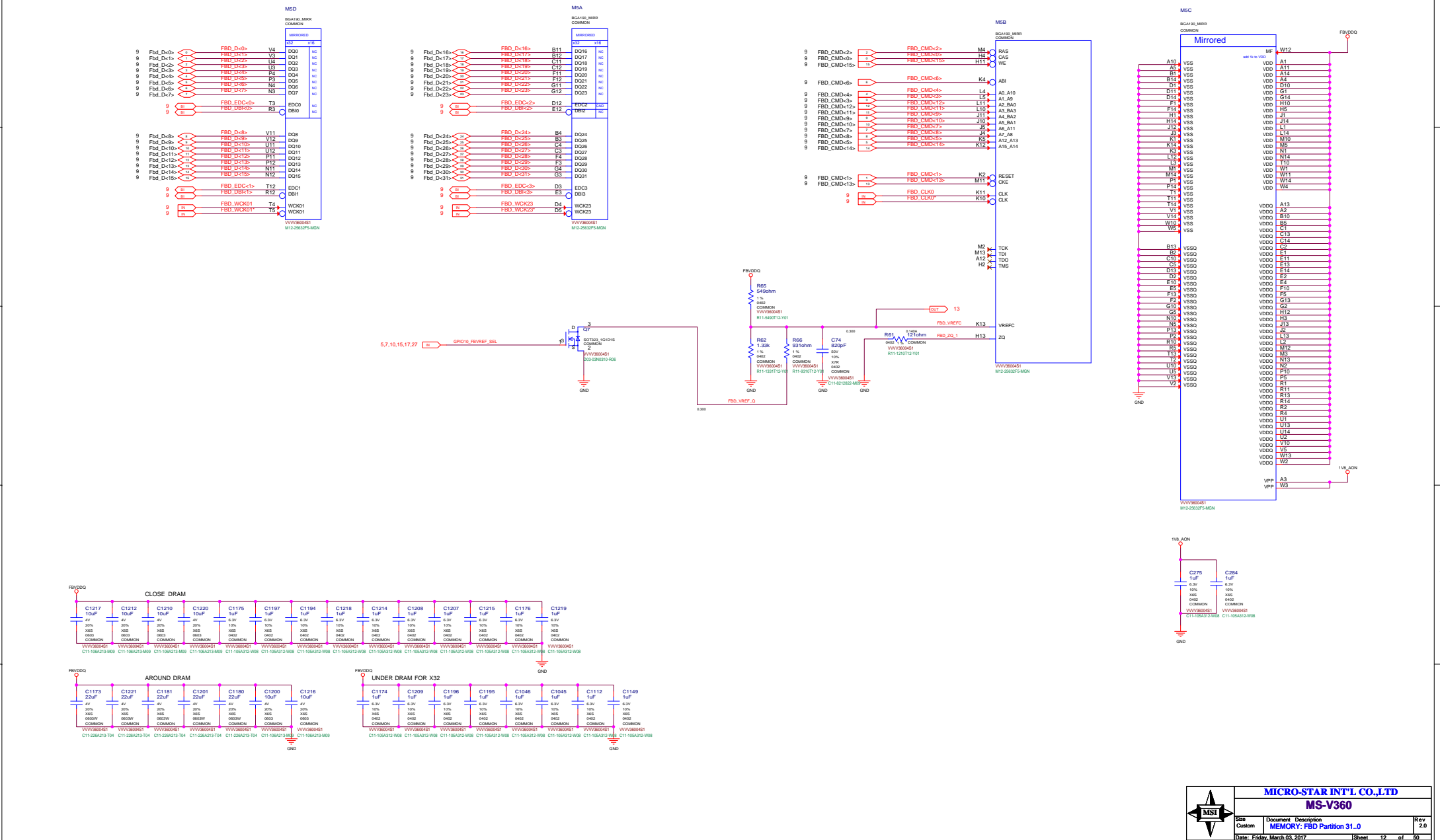


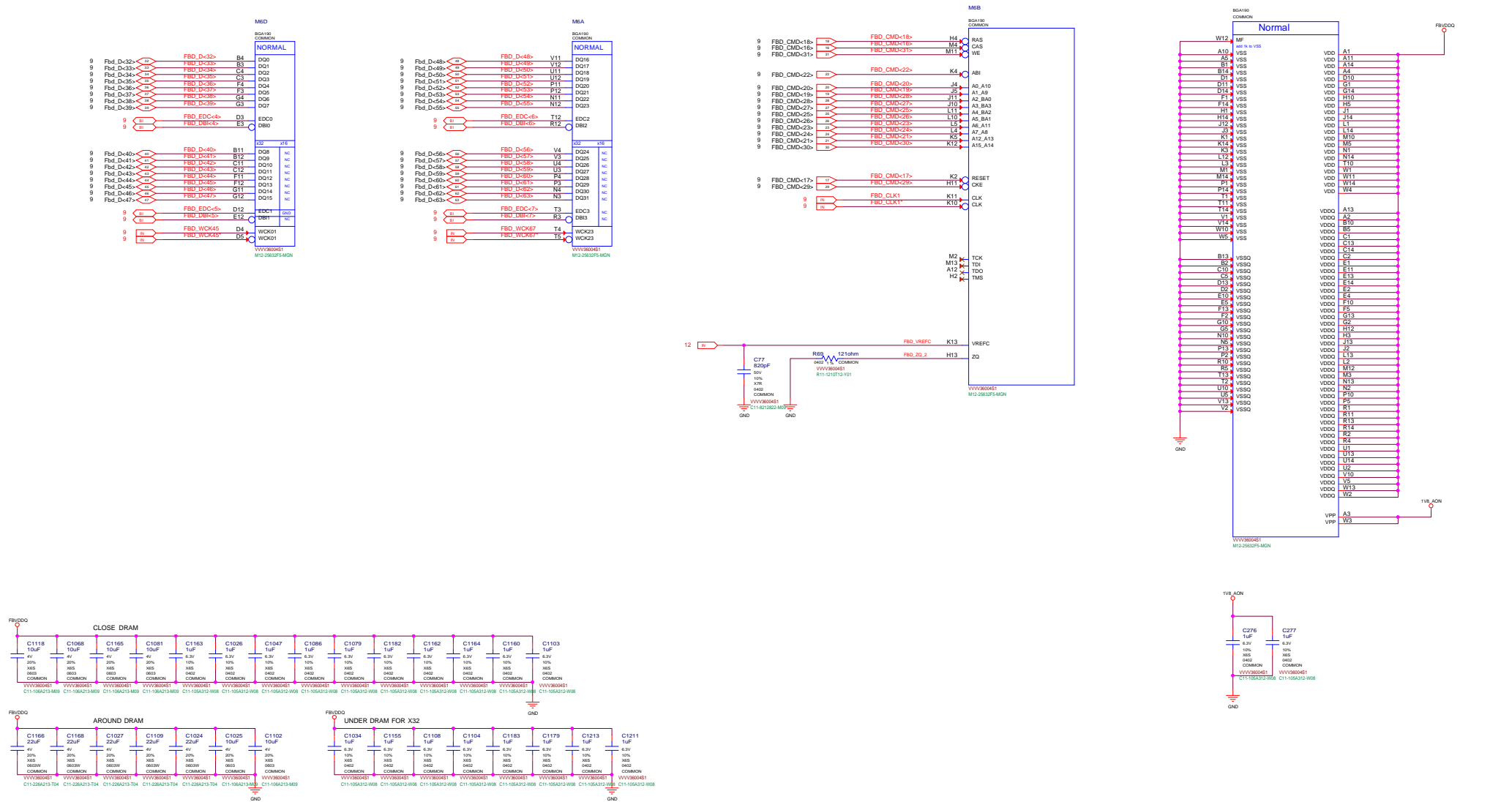


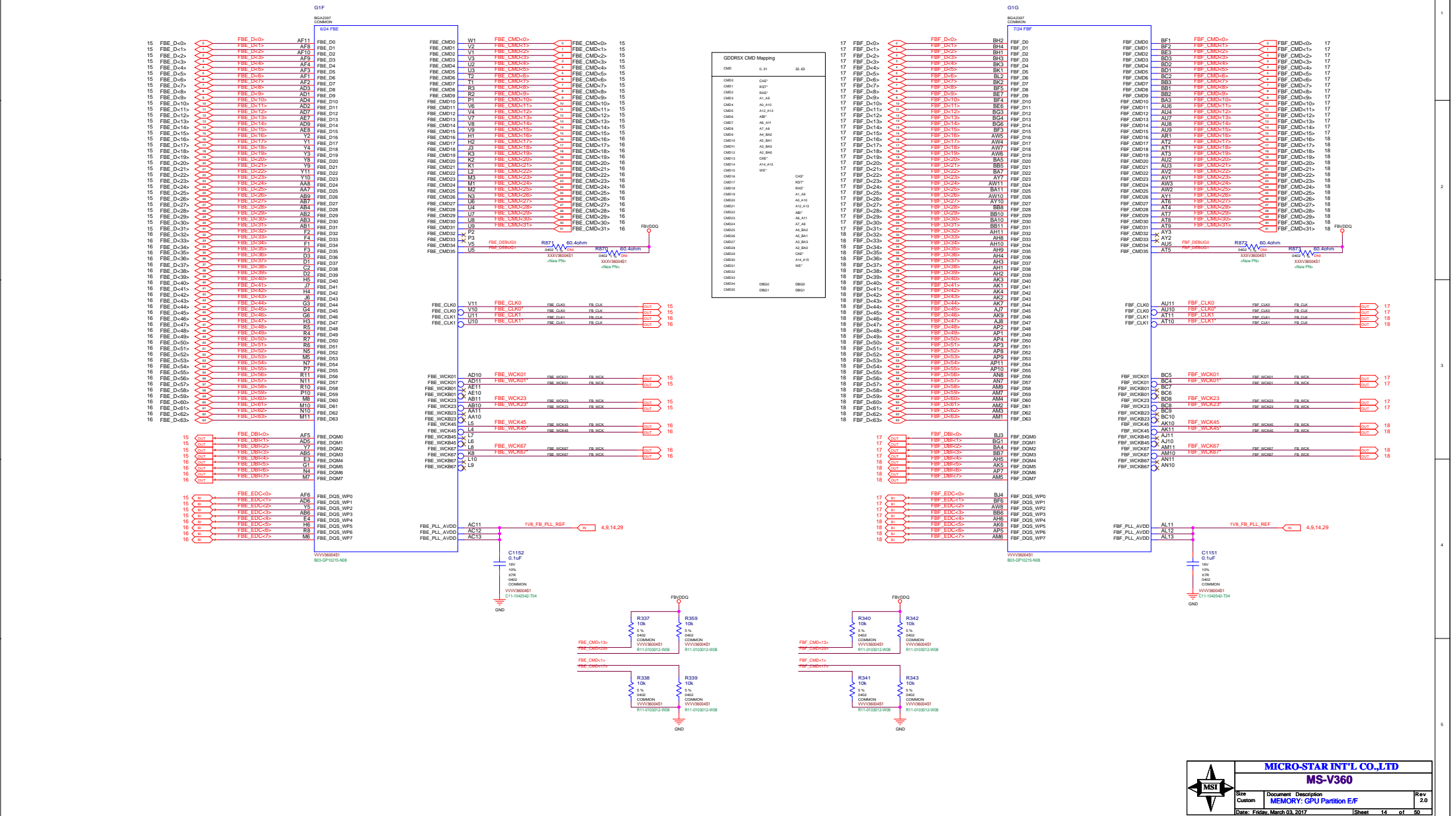


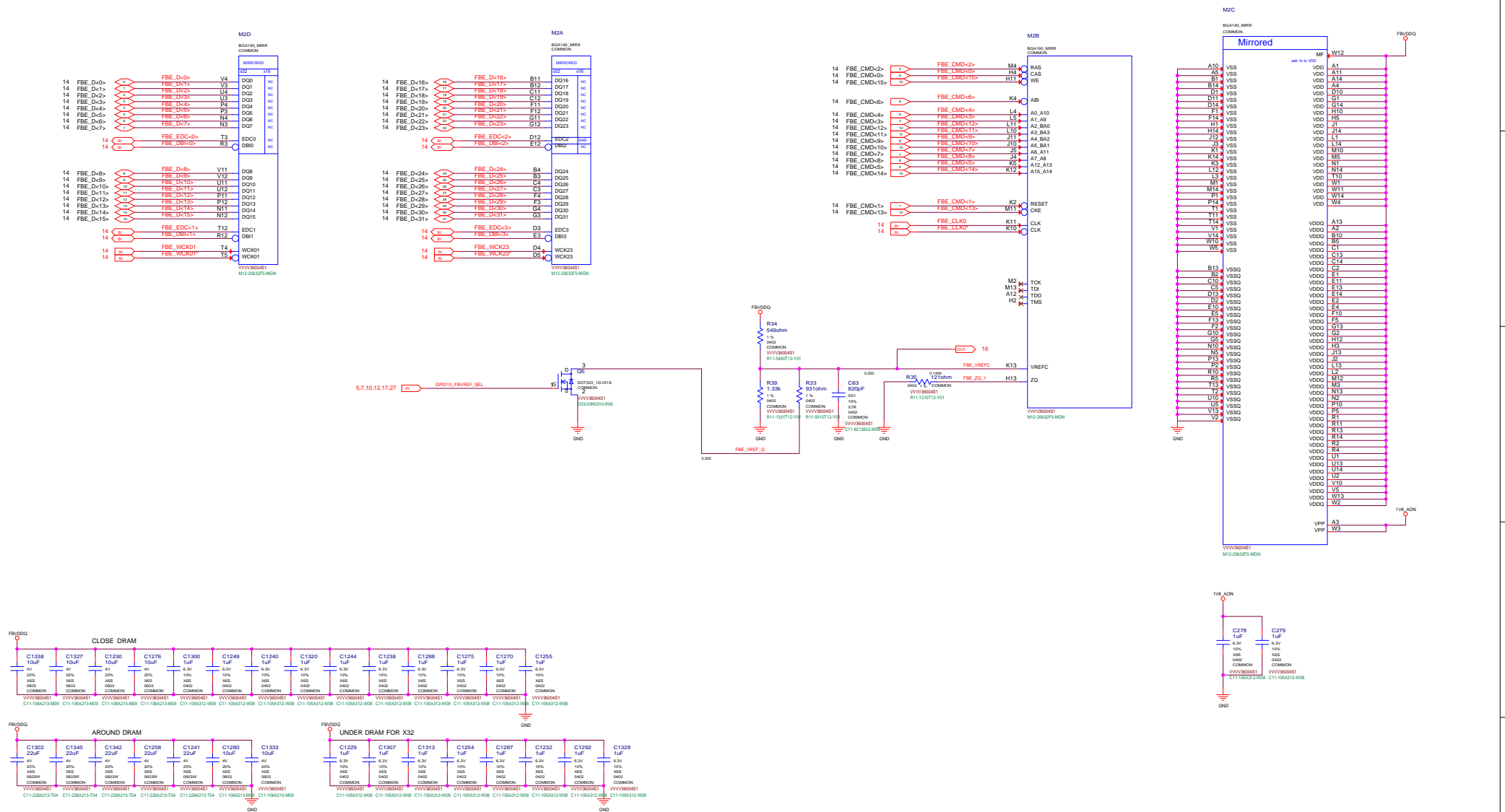
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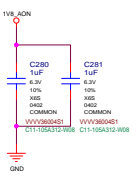
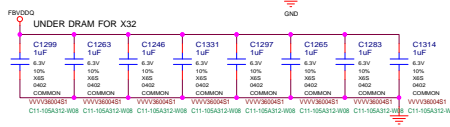
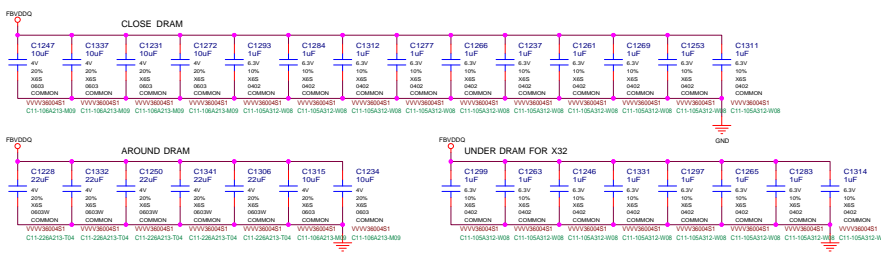
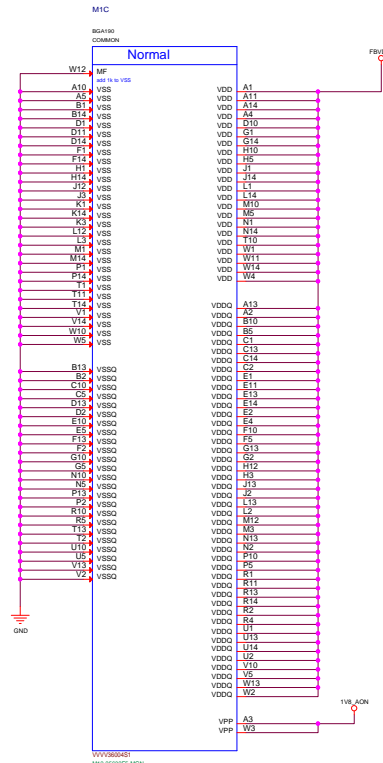
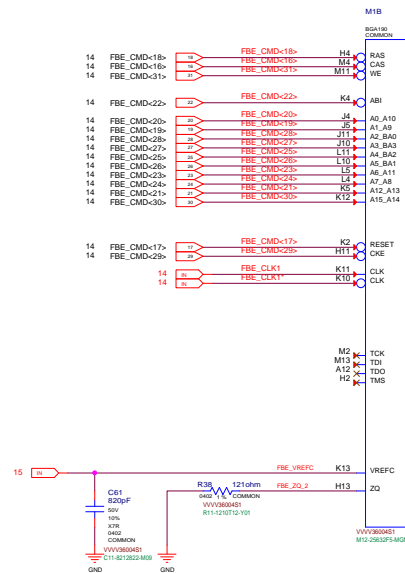
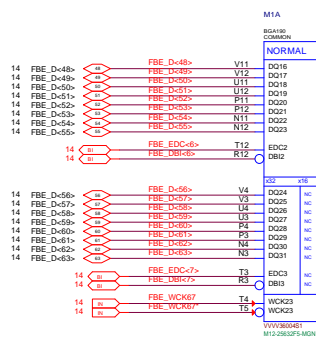
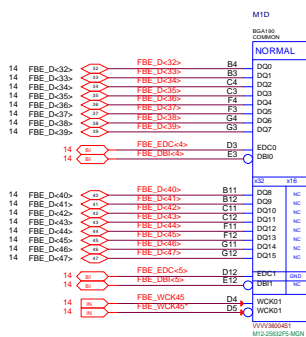
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| Size Custom | Document Description MEMORY: FBC Partition 63..32 | Rev 2.0 |
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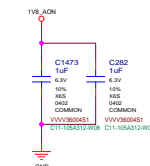
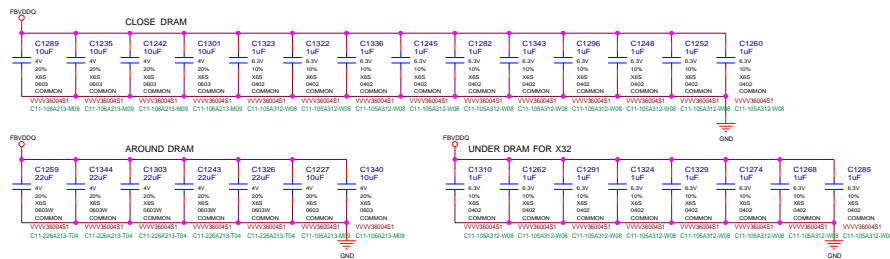
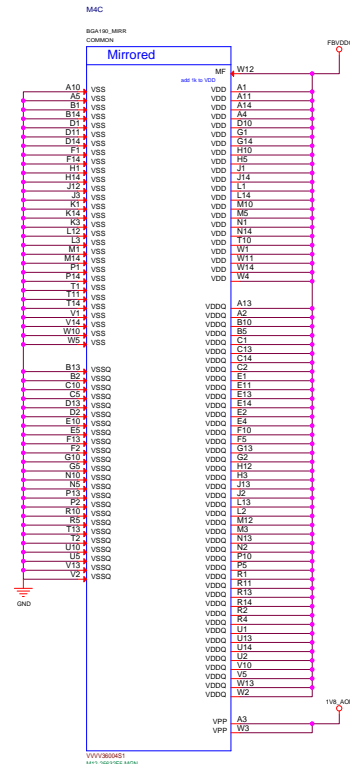
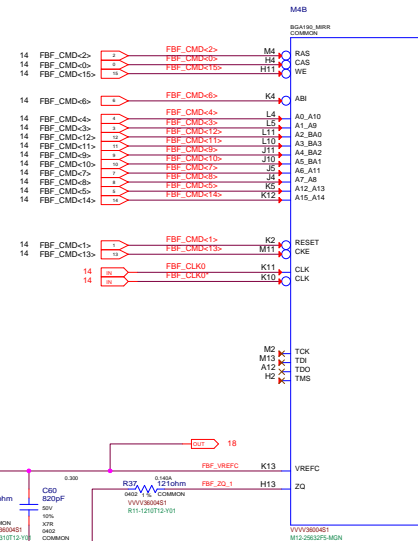
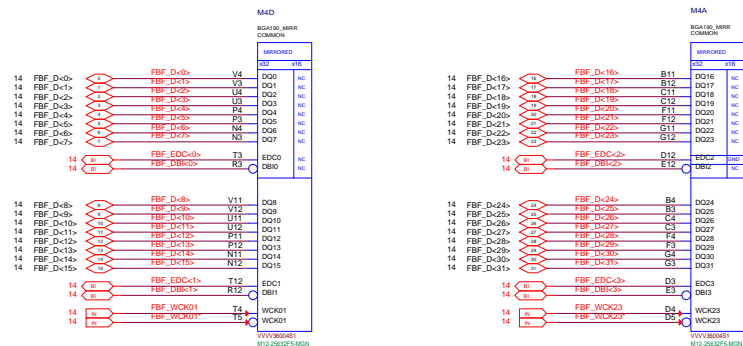


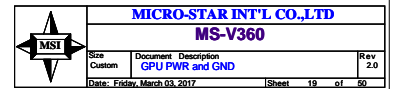
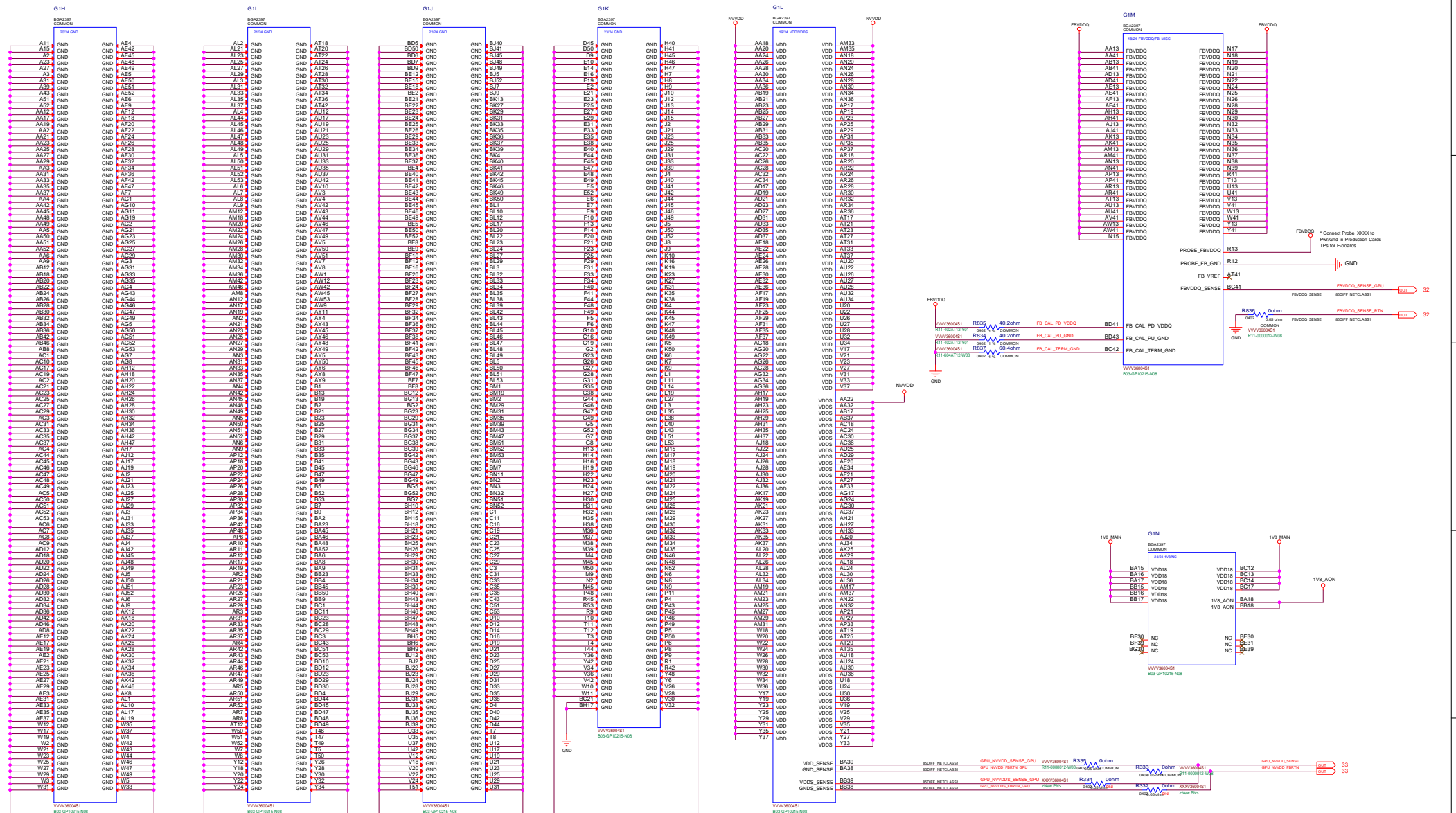


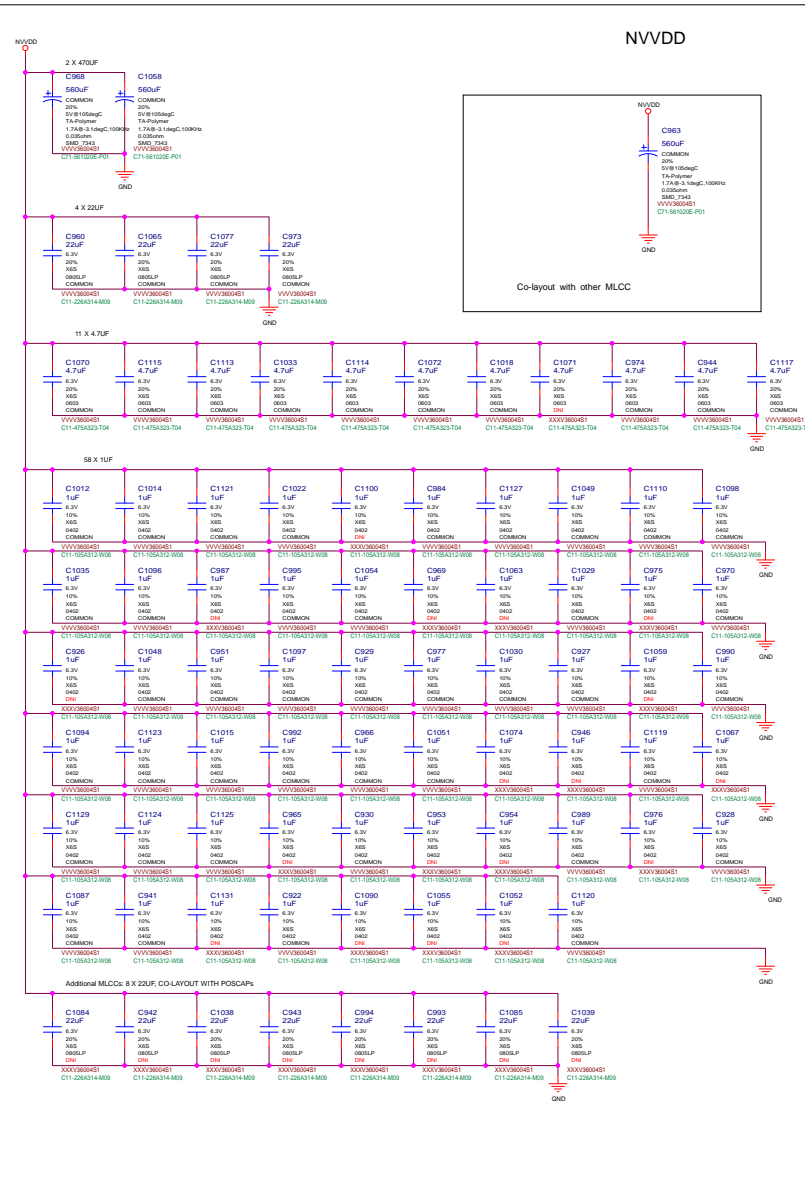
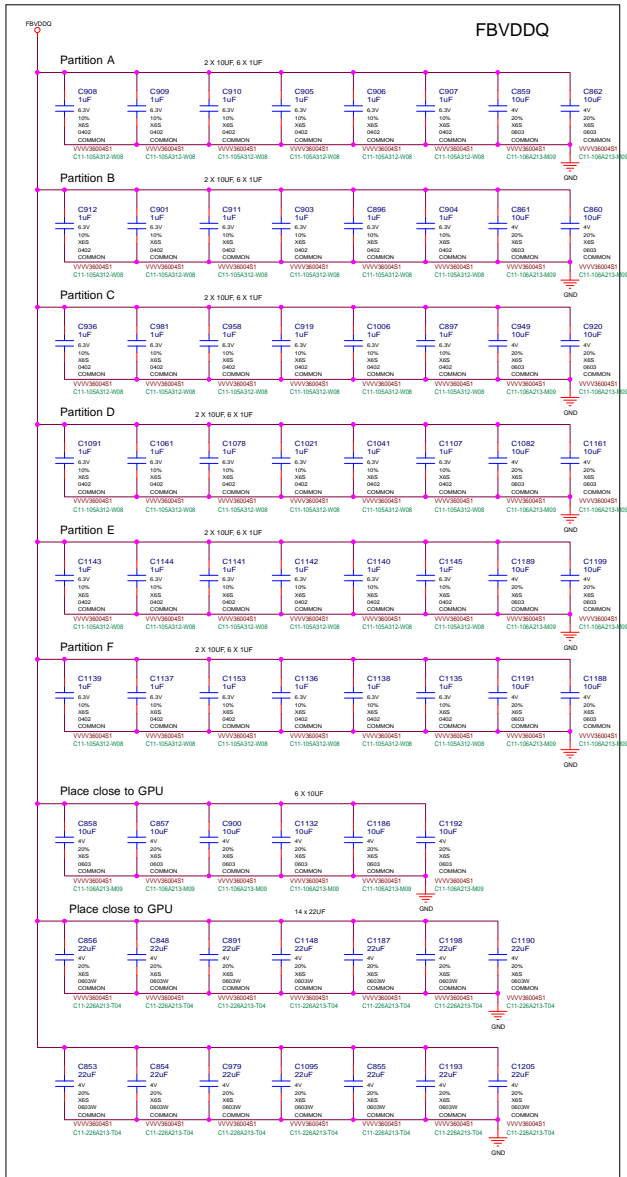


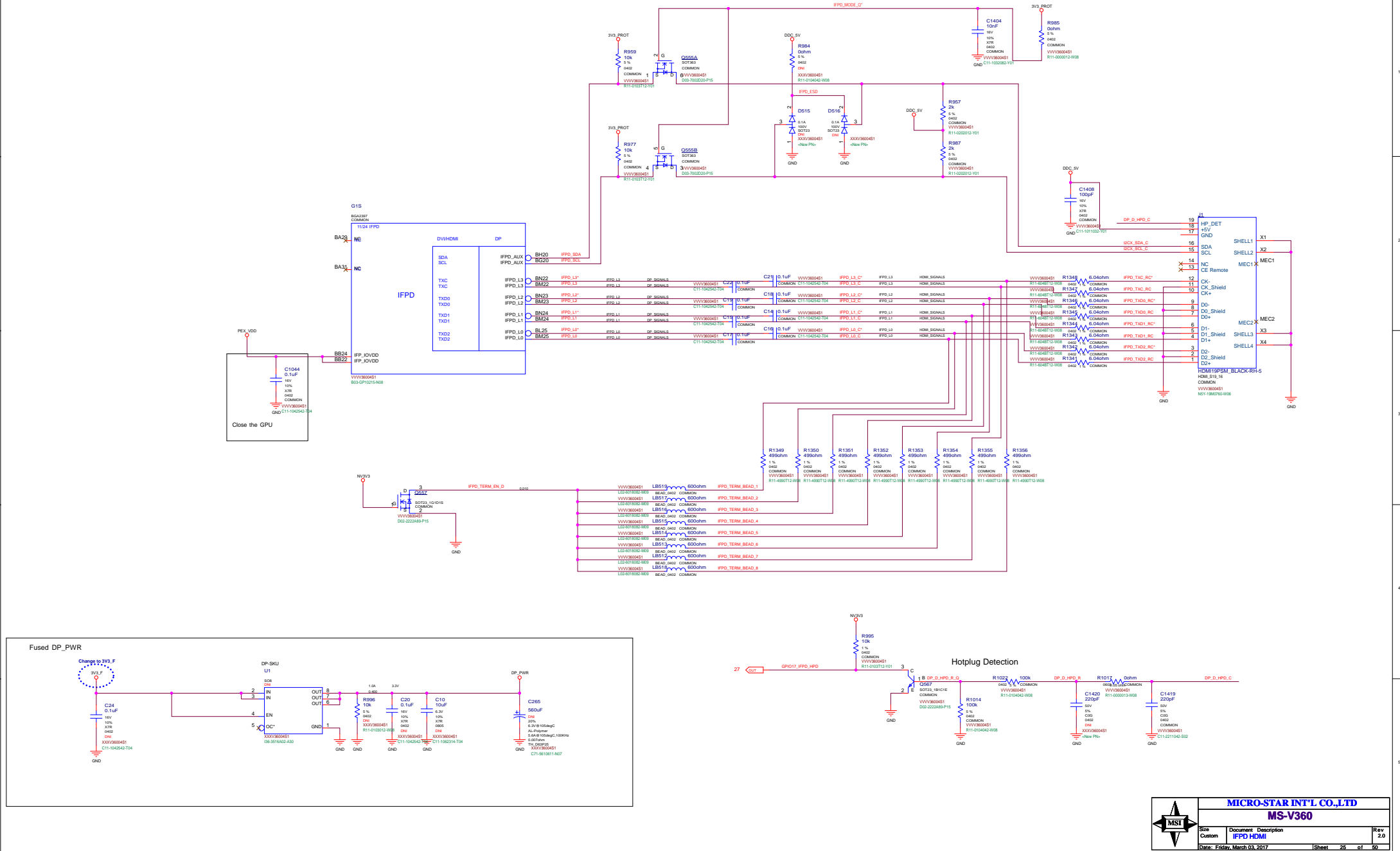
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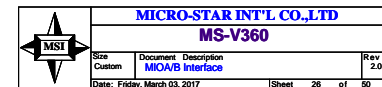
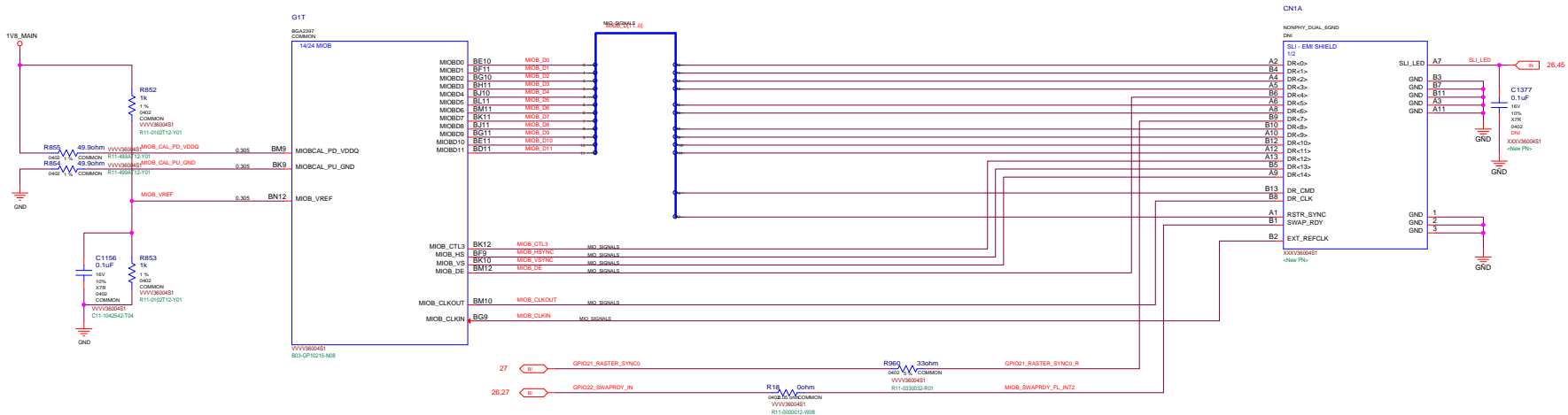
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| Size Custom | Document Description MEMORY: FBE Partition 63...32 | Rev 2.0 |
| Date: Friday, March 03, 2017 | | Sheet 16 of 50 |

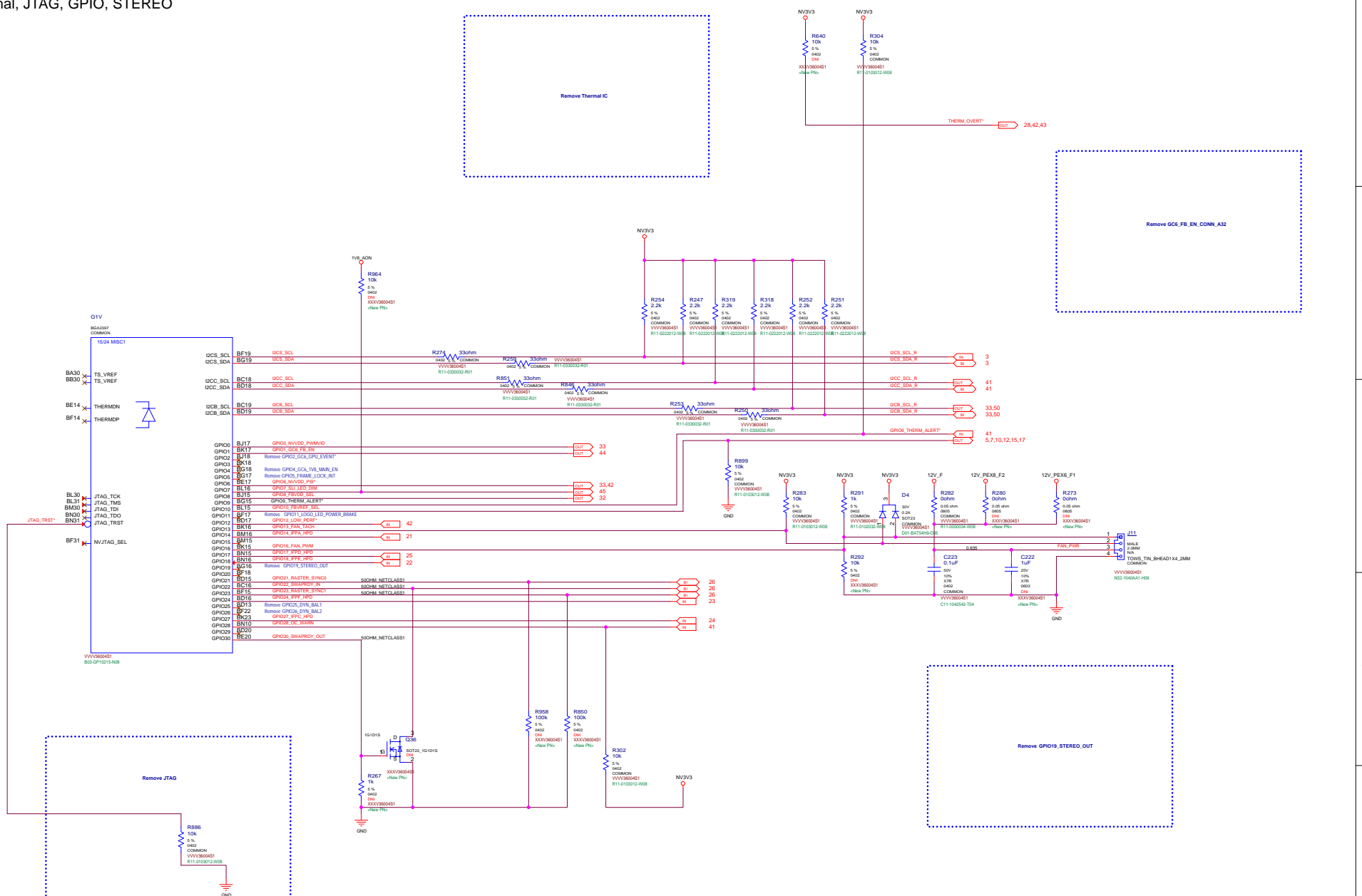












| STRAP2 | STRAP1 | STRAP0 | RAMCFG[4:0] | |
|--------|--------|----------|------------------|--------------------|
| L | L | L | 00000 | |
| L | H | L | 00010 | |
| L | H | H | 00011 | |
| H | H | L | 00110 | |
| H | H | H | 00111 | |
| ROM_SO | ROM_SI | ROM_SCLK | SOR_EXPOSED[3:0] | 1:ENABLE 0:DISABLE |
| L | L | L | 1111 DEFAULT | SOR0/1/2/3 ENABLE |
| L | L | H | 1110 | |
| L | H | L | 1101 | |
| L | H | H | 1100 | |
| H | L | L | 1011 | |
| H | L | H | 1010 | |
| H | H | L | 1001 | |
| H | H | H | 1000 | |
| L | L | M | 0111 | |
| L | M | L | 0110 | |
| L | M | H | 0101 | |
| L | H | M | 0100 | |
| H | L | M | 0011 | |
| H | M | L | 0010 | |
| H | M | H | 0001 | |
| H | H | M | 0000 | |

| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |
|--------|--------|--------|--------------|-----------|----------|------------|
| M | H | H | 1 | 1 | 1 | 1 |
| M | H | L | 1 | 1 | 1 | 0 |
| M | L | H | 1 | 1 | 0 | 1 |
| M | L | L | 1 | 1 | 0 | 0 |
| L | H | M | 1 | 0 | 1 | 1 |
| L | M | H | 1 | 0 | 1 | 0 |
| L | M | L | 1 | 0 | 0 | 1 |
| L | L | M | 1 | 0 | 0 | 0 |
| H | H | H | 0 | 1 | 1 | 1 |
| H | H | L | 0 | 1 | 1 | 0 |
| H | L | H | 0 | 1 | 0 | 1 |
| H | L | L | 0 | 1 | 0 | 0 |
| L | H | H | 0 | 0 | 1 | 1 |
| L | H | L | 0 | 0 | 1 | 0 |
| L | L | H | 0 | 0 | 0 | 1 DEFAULT |
| L | L | L | 0 | 0 | 0 | 0 |

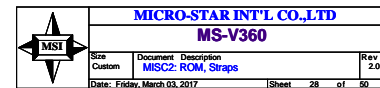
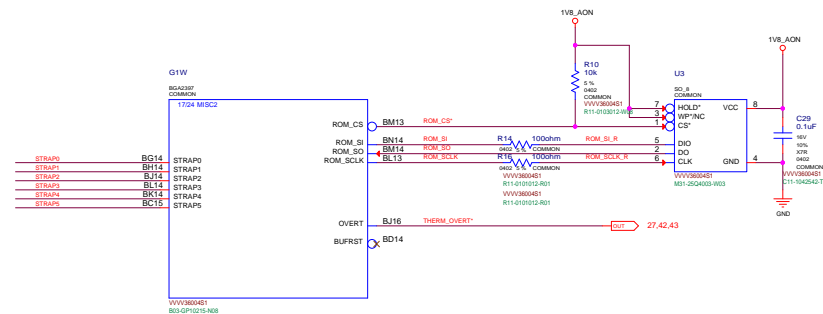
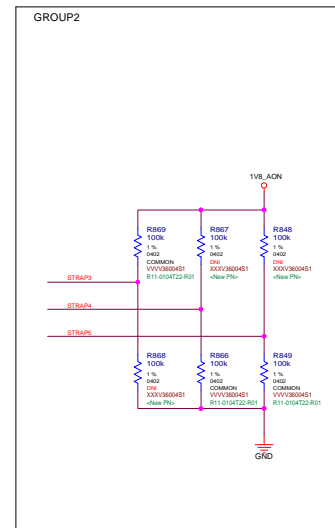
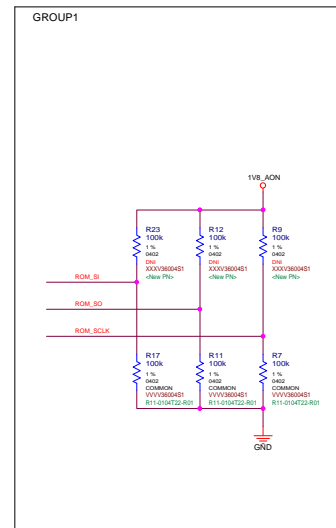
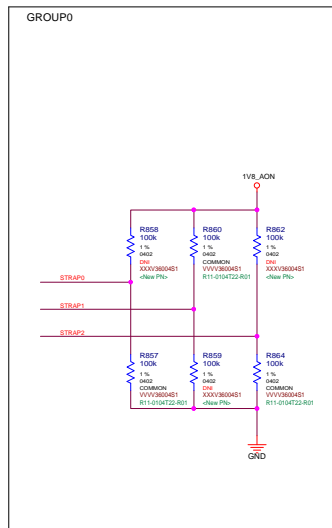
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

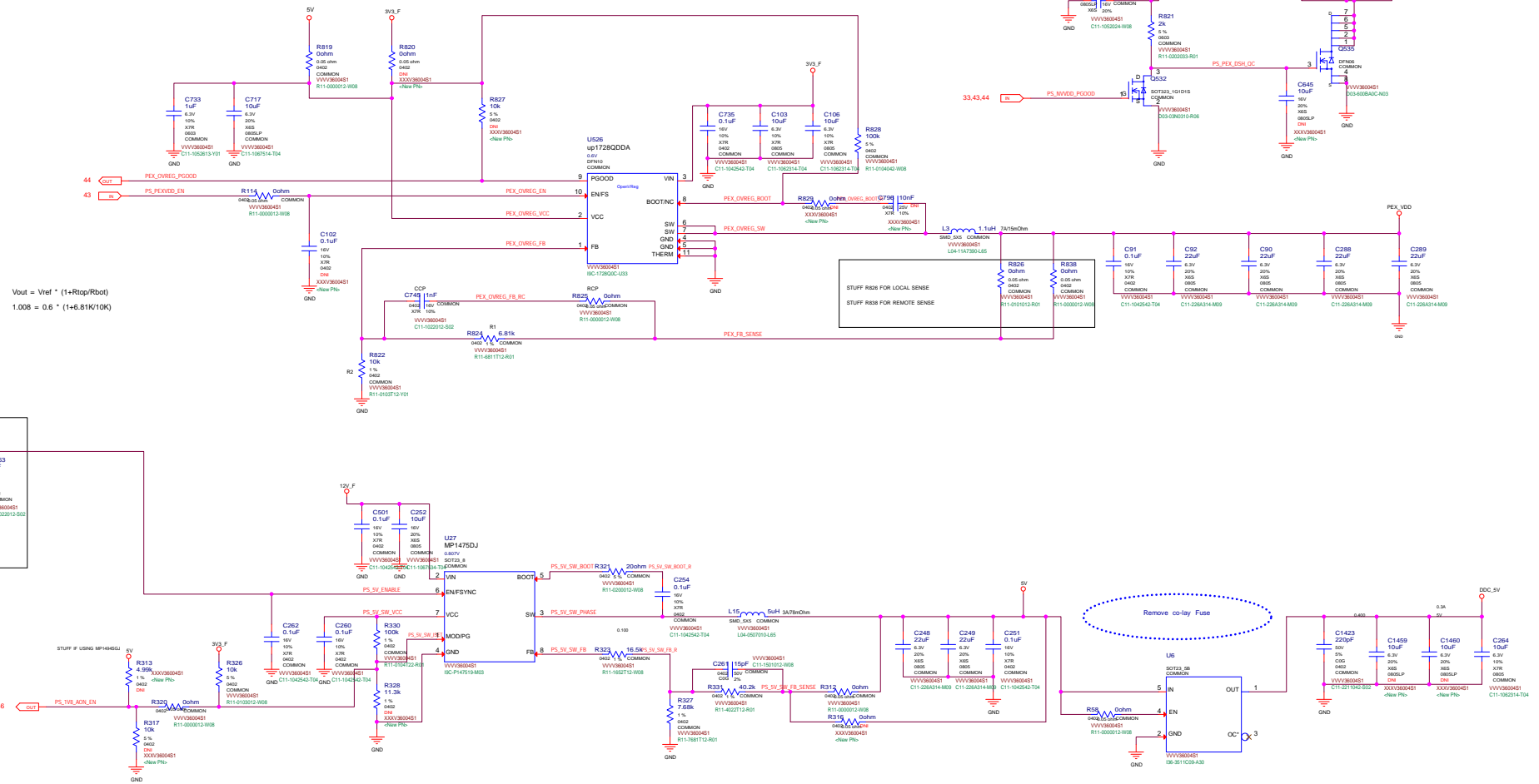
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

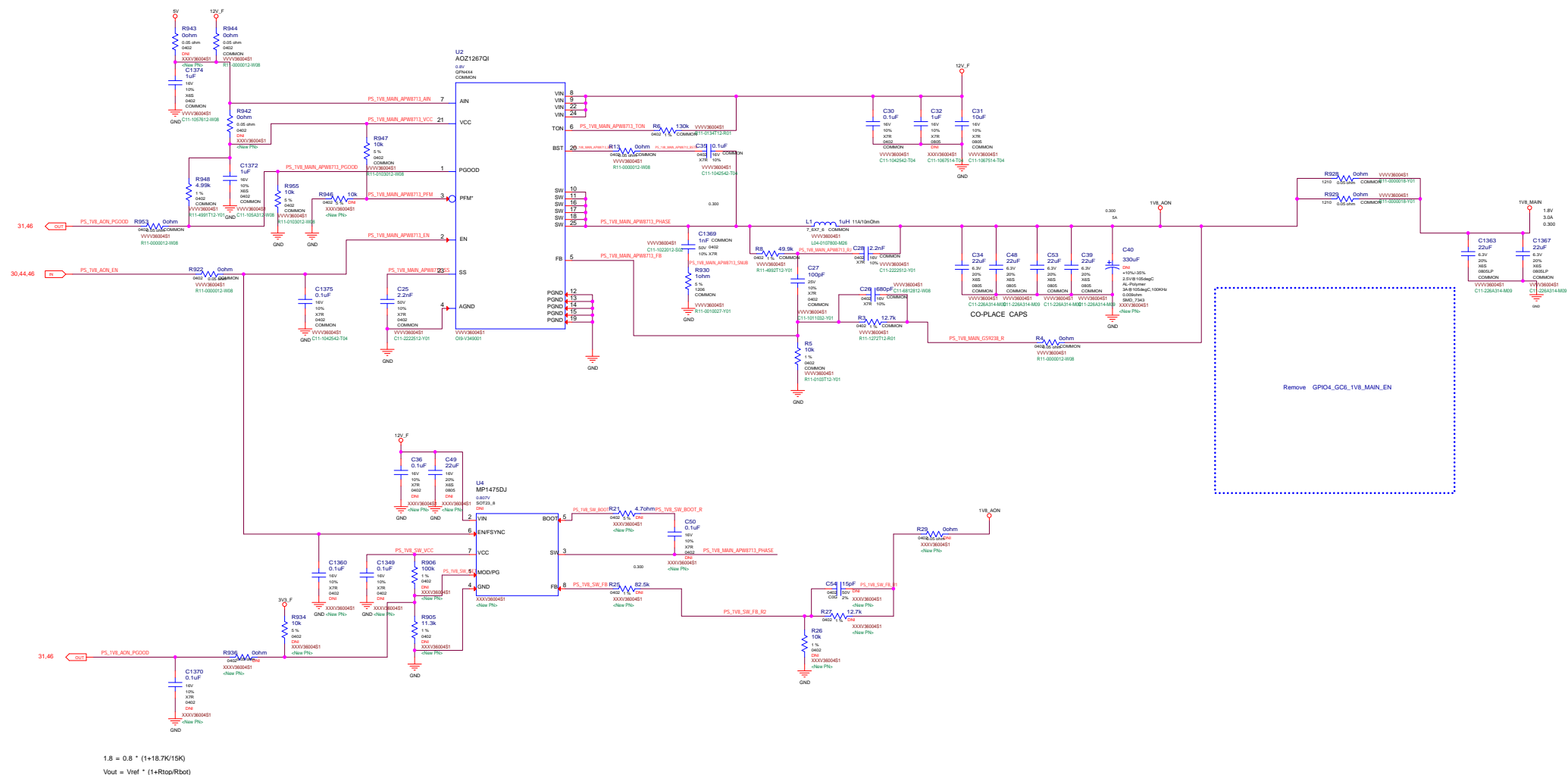
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

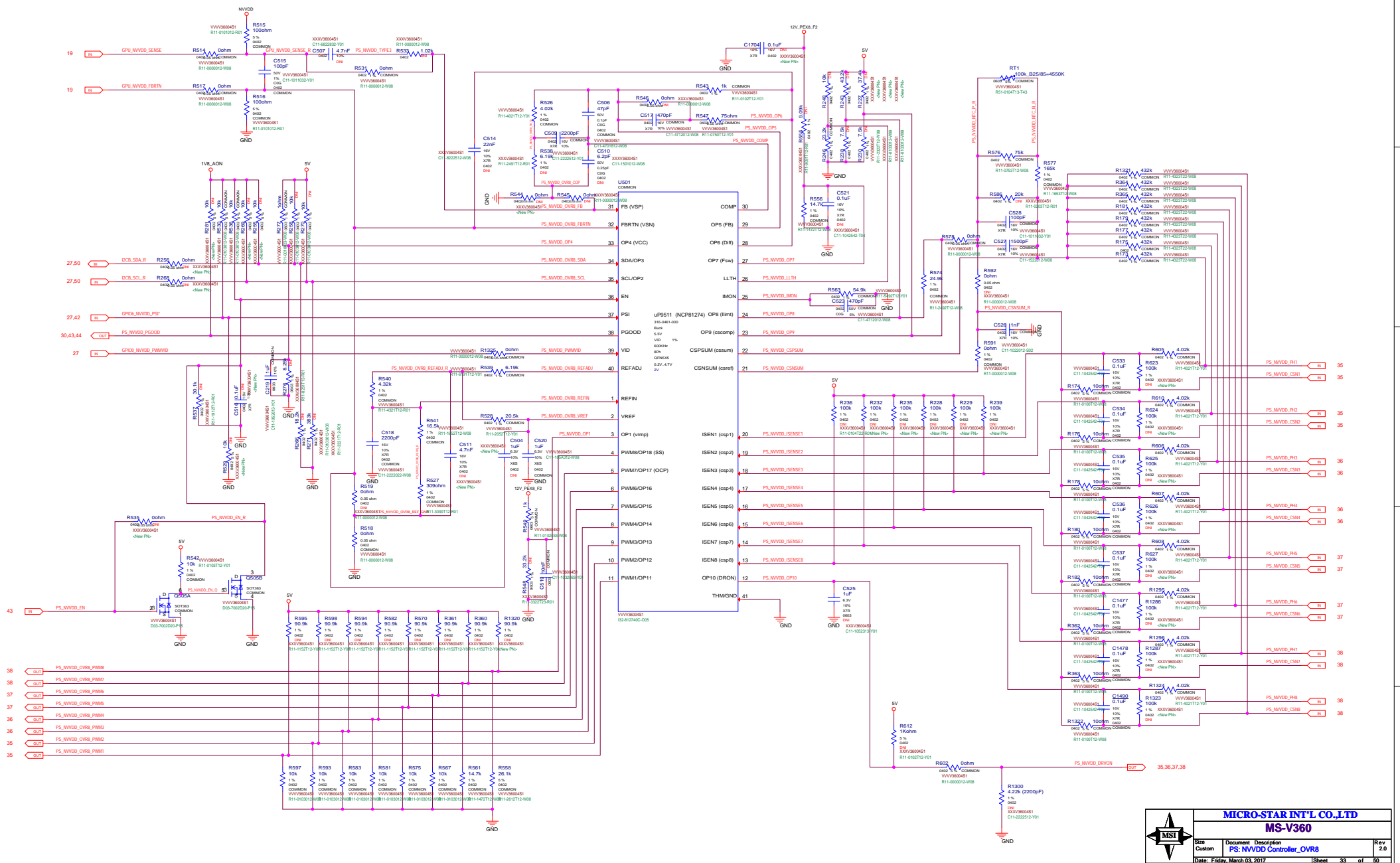
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



PEX PLL Switcher





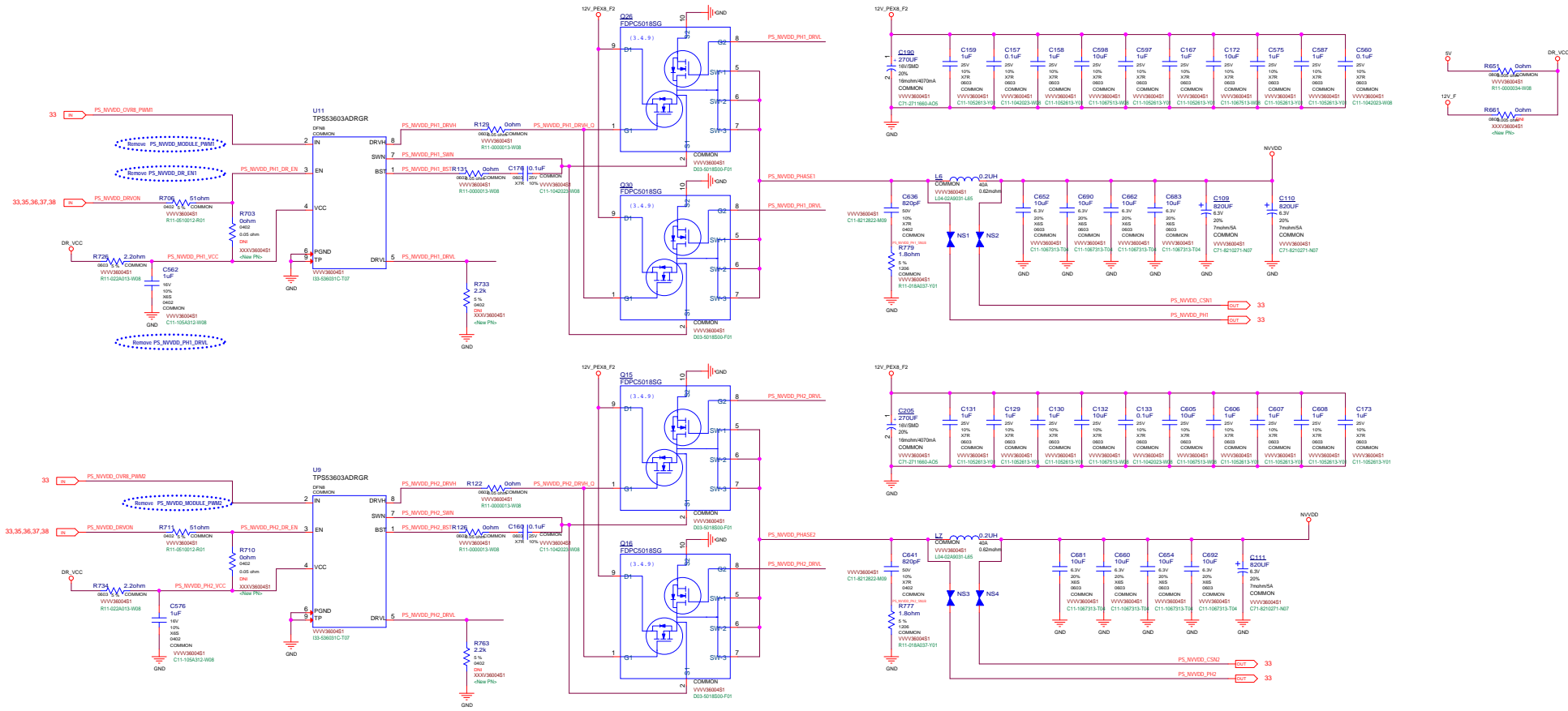


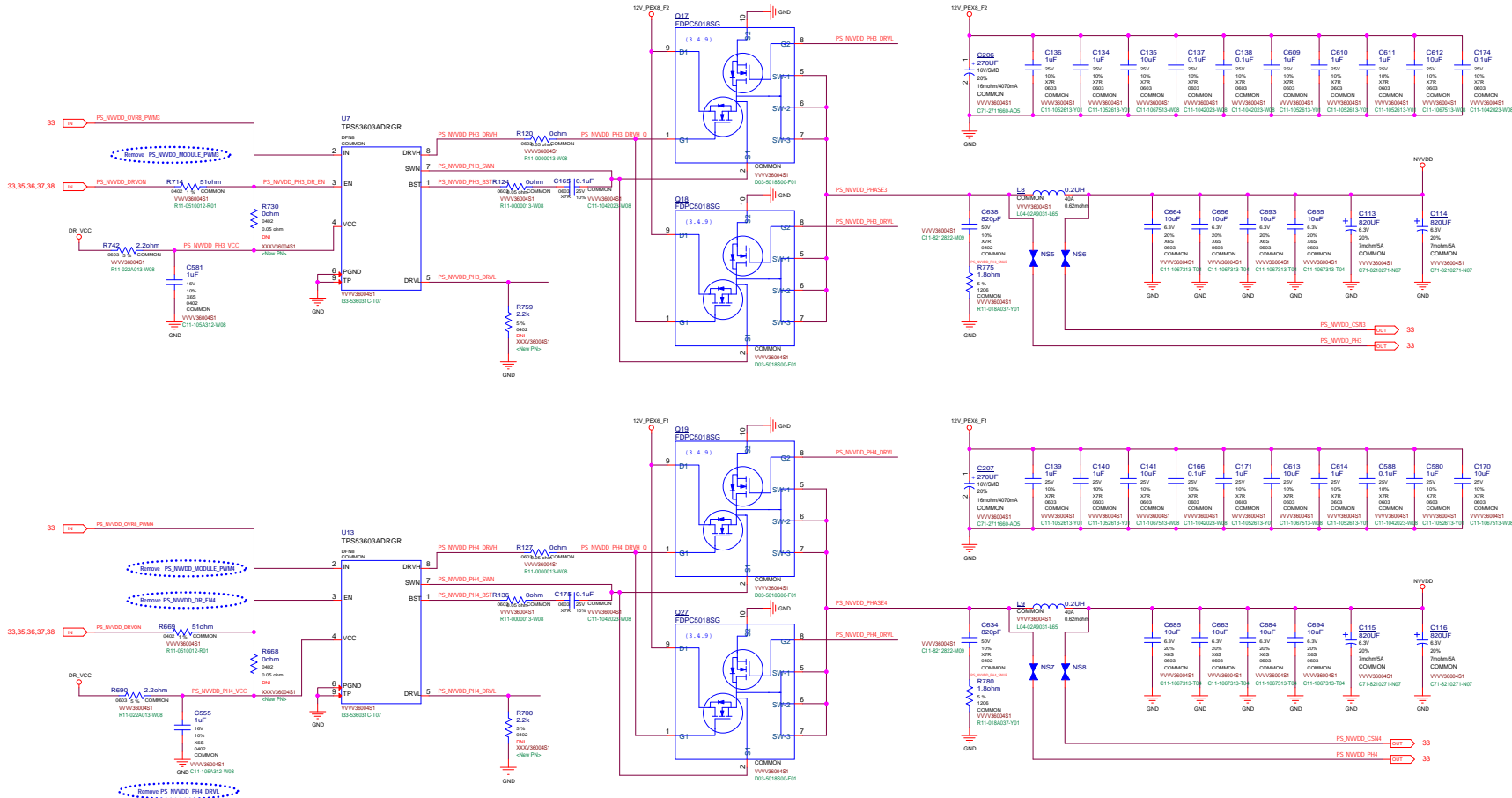


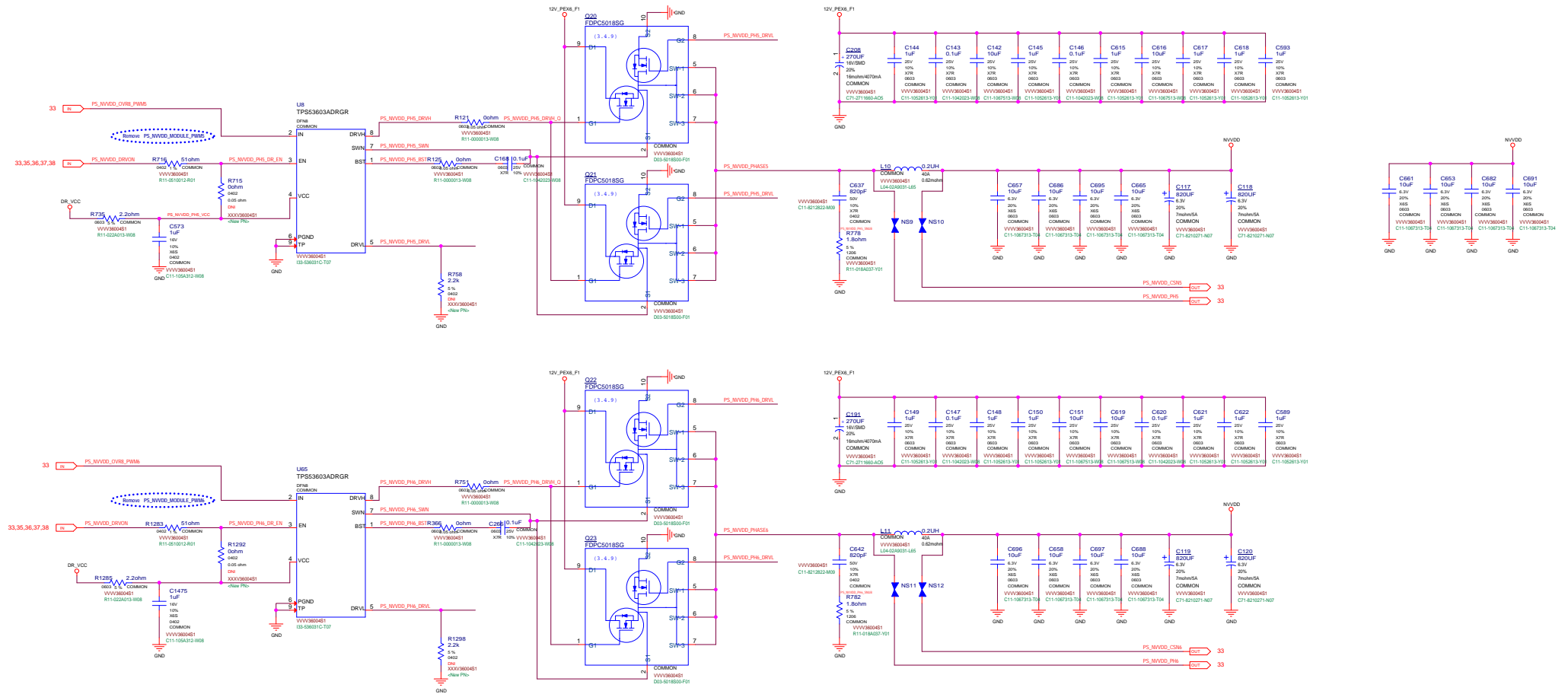
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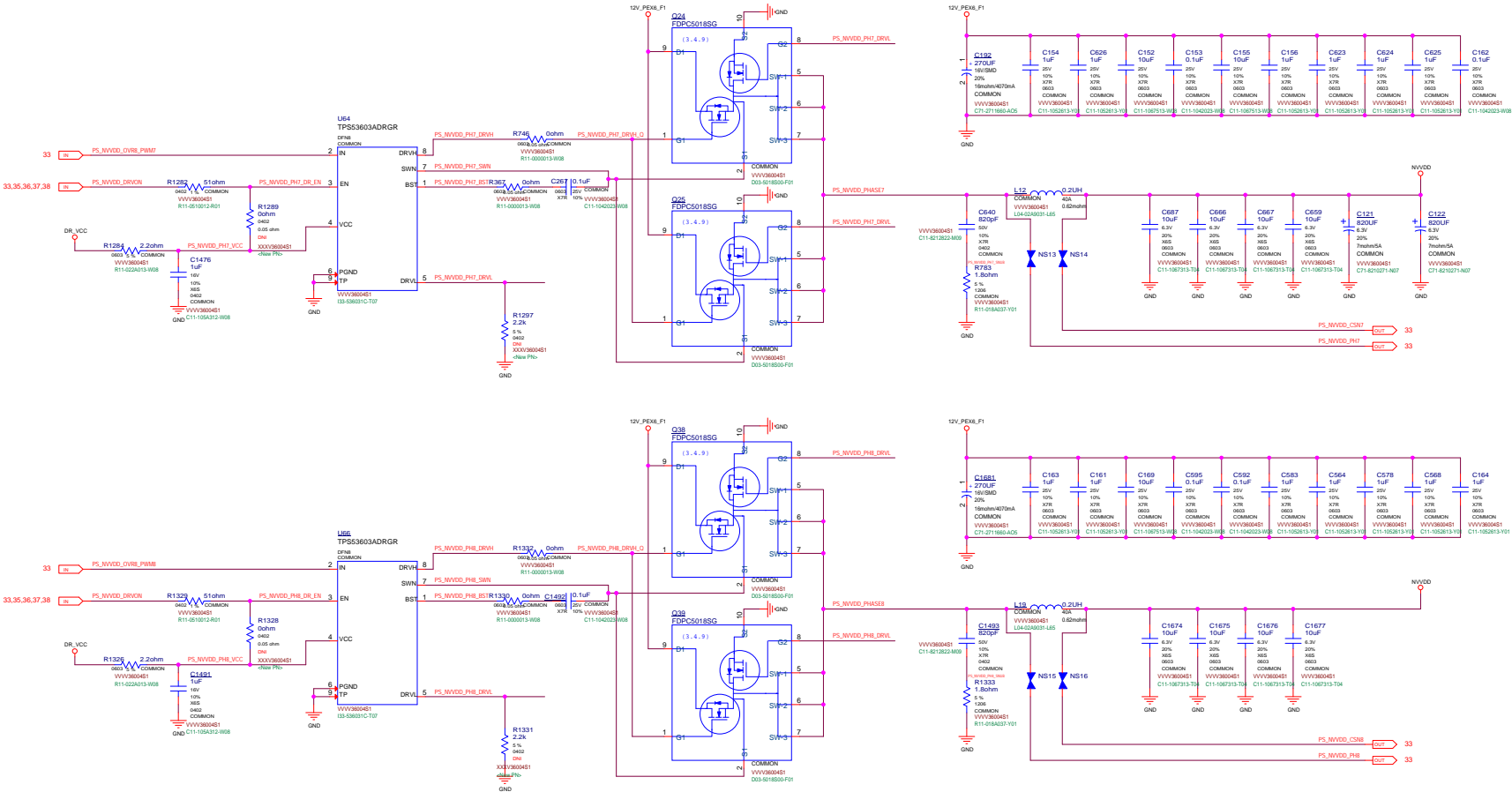
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| Size | Document | Description | Rev |
| Custom | PS: NVVDD CONTROLLER_PWR-MODULE | | 2.0 |
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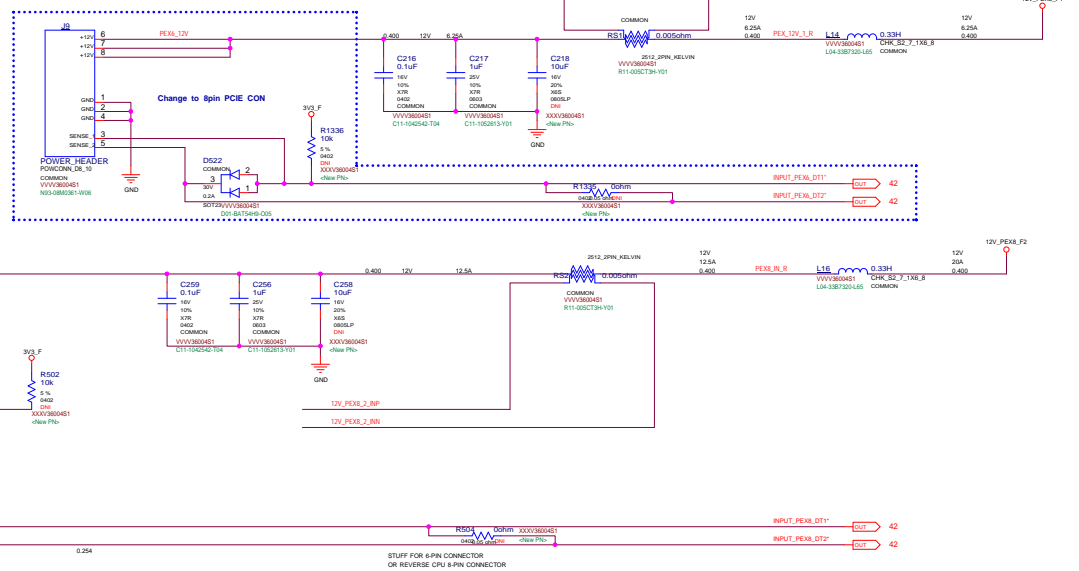
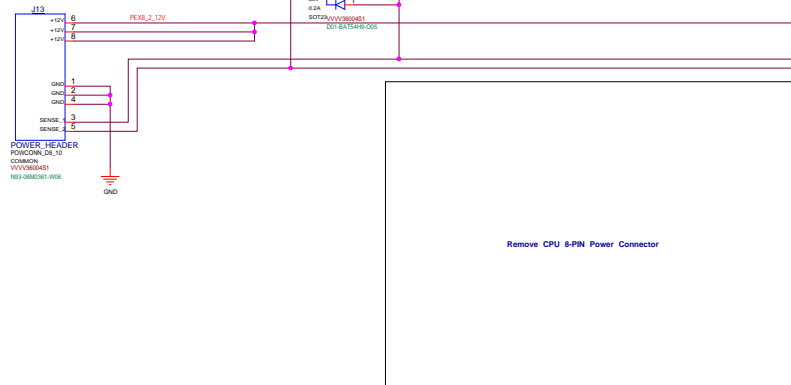
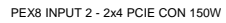
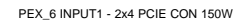
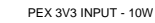
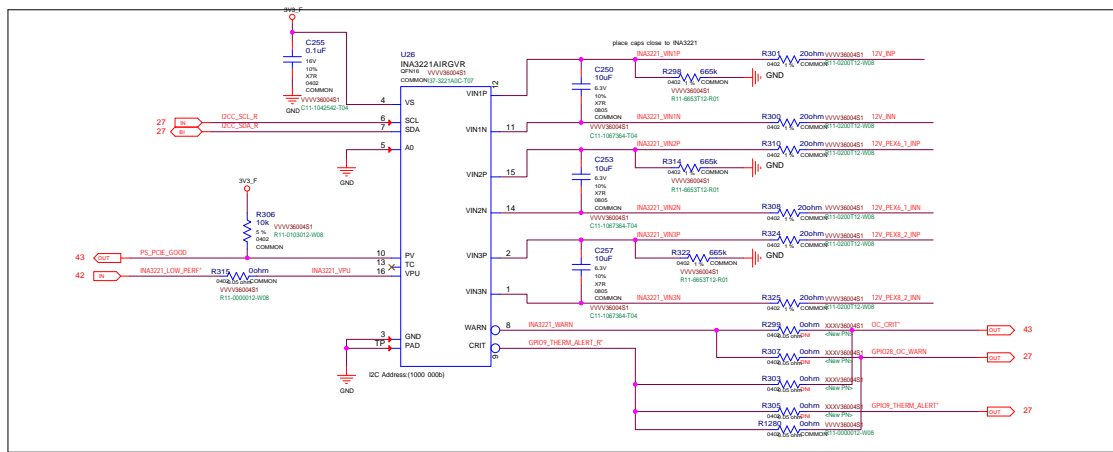




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| MICRO-STAR INT'L CO.,LTD | | | |
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| Size | Document | Description | Rev |
| Custom | Dynamic Power Balance Phases | | 2.0 |
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| | | |
|------------------------------|---------------------------------|----------------|
| MICRO-STAR INT'L CO.,LTD | | |
| MS-V360 | | |
| Size | Document Description | Rev |
| Custom | PS: Dynamic Power Balance Logic | 2.0 |
| Date: Friday, March 03, 2017 | | Sheet 40 of 50 |

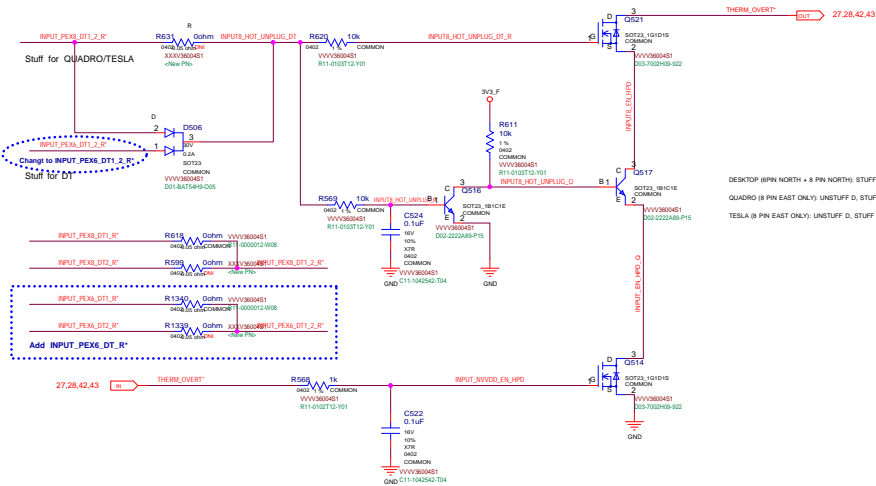
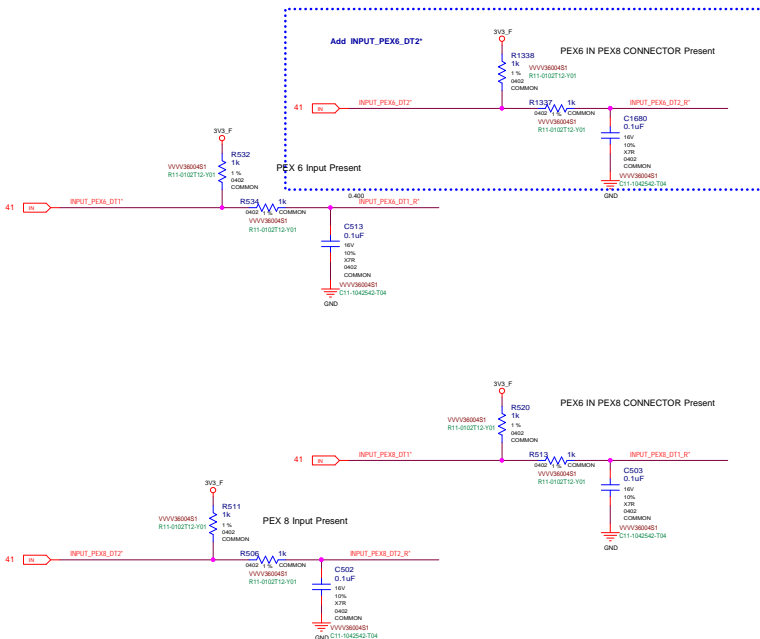
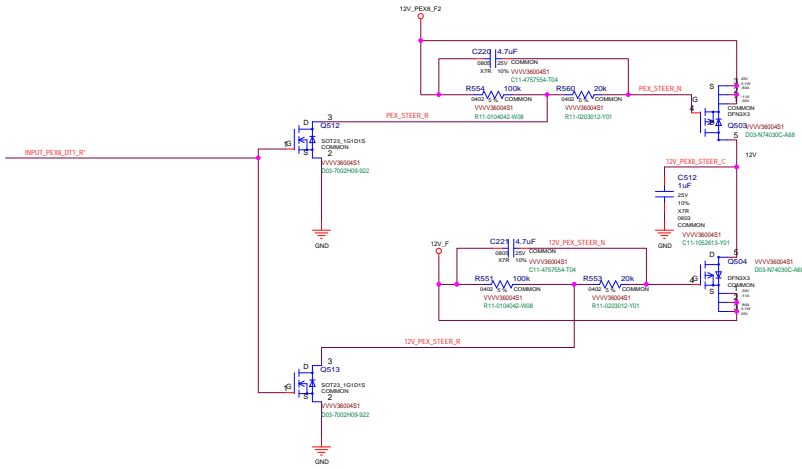


QUADRO/TESLA:

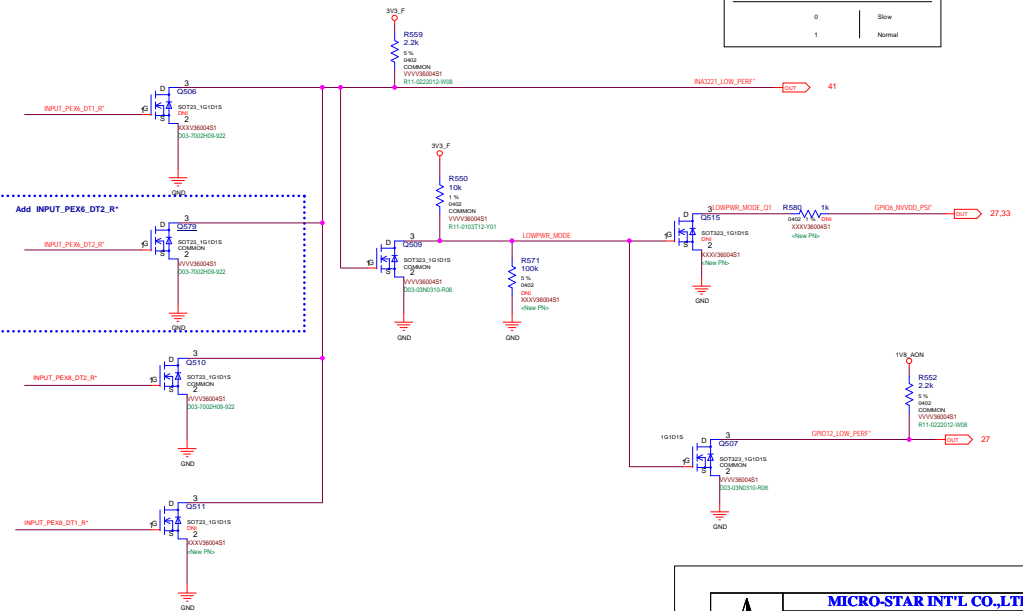
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVeg Type4 + Phase Doubler, 2 phase PSI mode



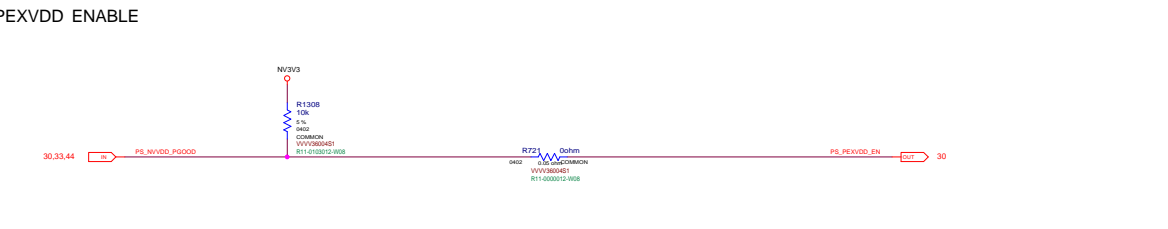
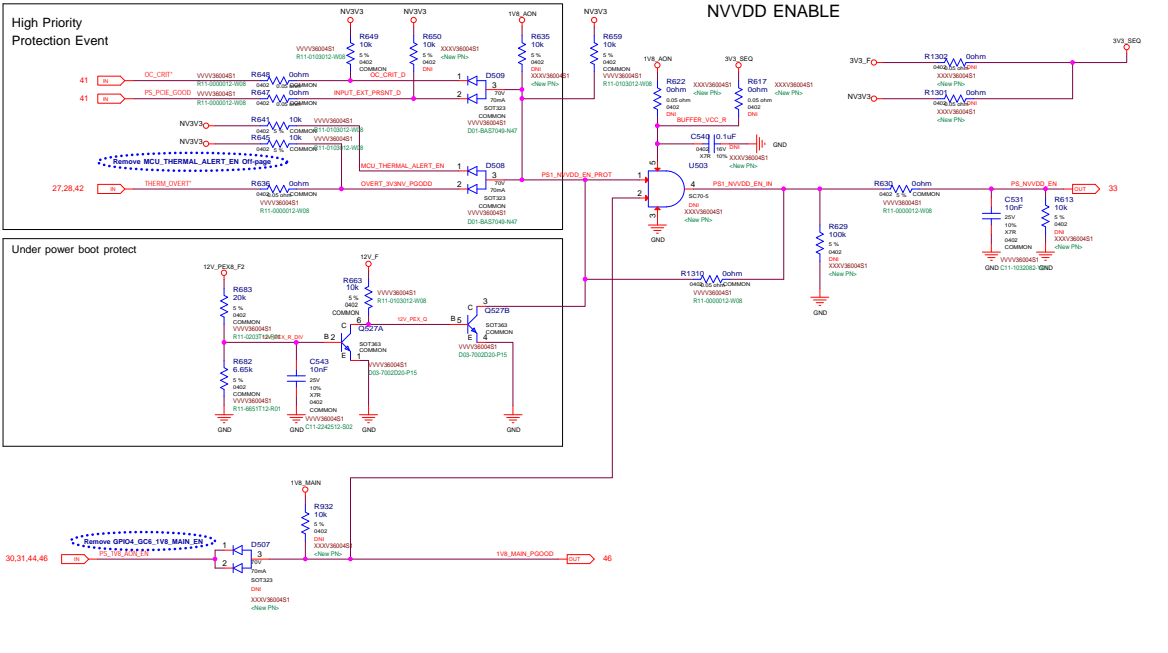
PEX Input - Under Power Boot Controls



A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

| GPU12_LOW_PERF* | GPU SPEED |
|-----------------|-----------|
| 0 | Slow |
| 1 | Normal |

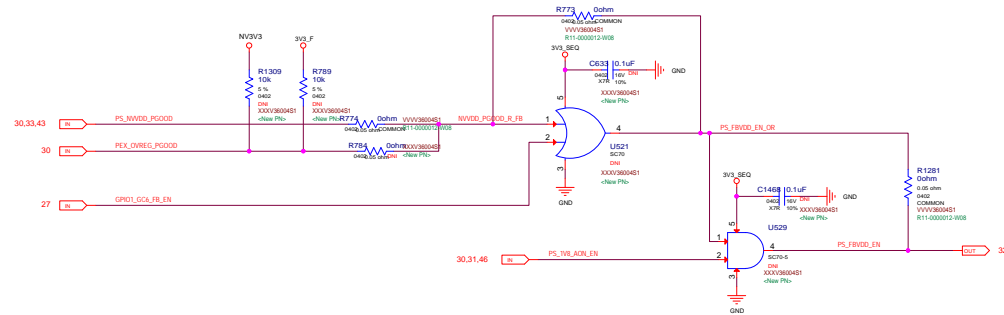
| MICRO-STAR INT'L CO.,LTD | | | |
|------------------------------|----------|--|-------|
| MS-V360 | | | |
| Size | Document | Description | Rev |
| Custom | Document | PS: 12V Current Steering & Hot Unplug Detect | 2.0 |
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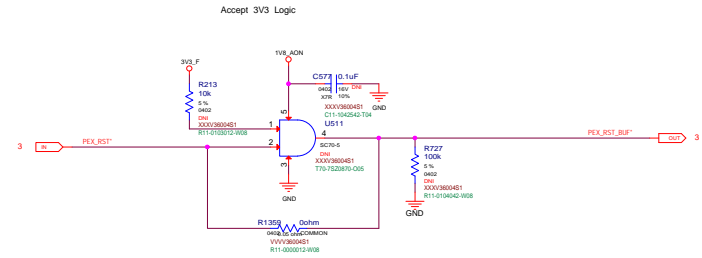
Remove PEX_CLKREQ*

Remove GPU_EVENT*

FBVDD/Q ENABLE

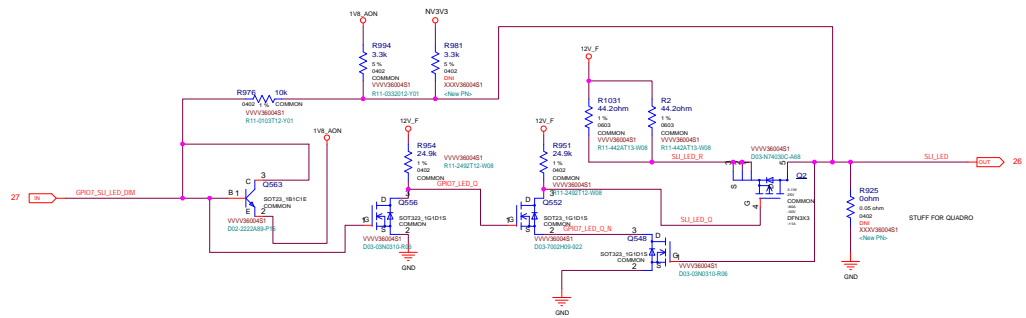


PEX_RST# LOGIC

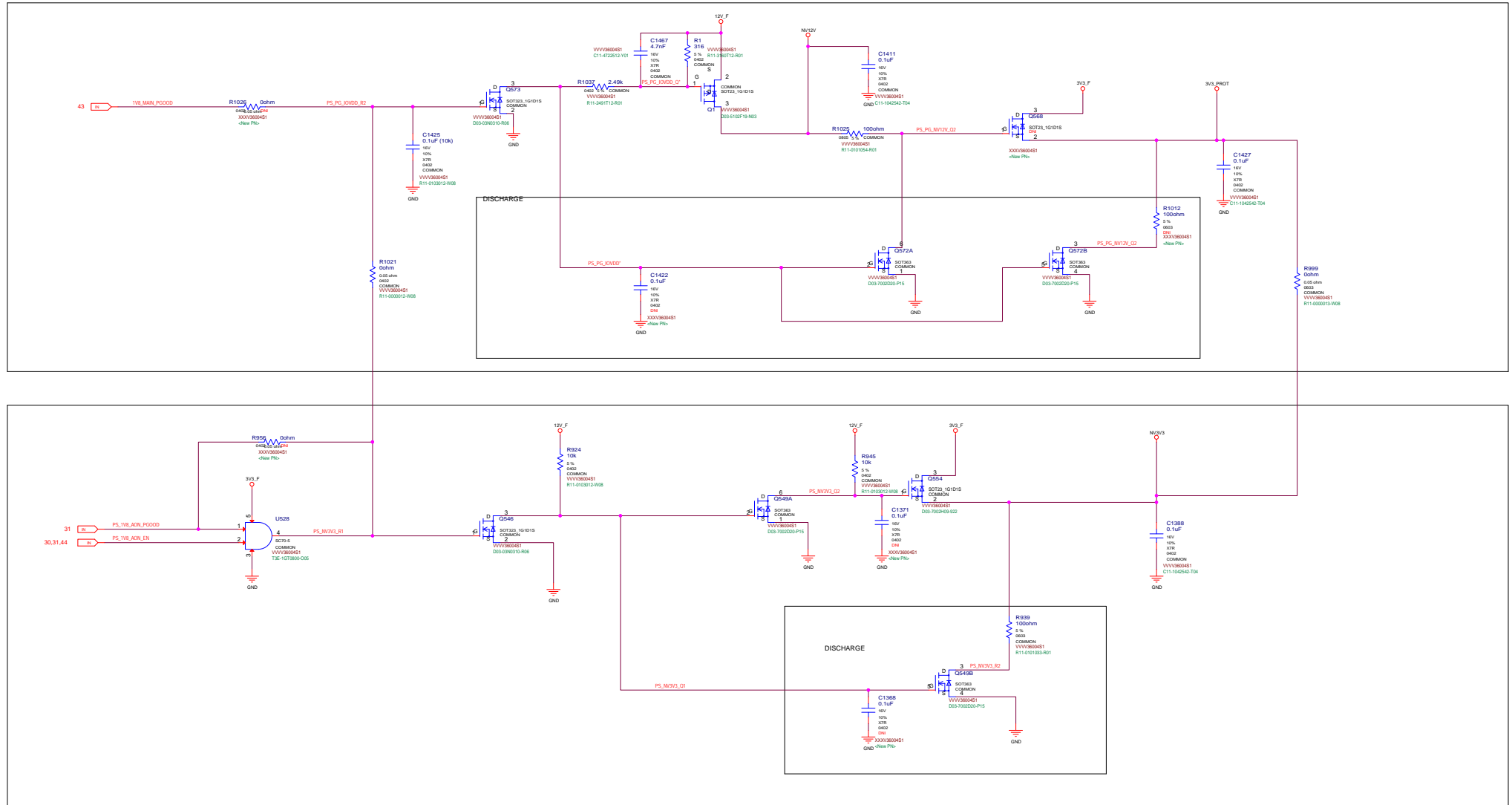


Remove LED HEADER(GEFORCE ONLY)

SLI LED (GEFORCE ONLY)



| | | | |
|---|---------------------------------|-----------------------|-----|
|  | MICRO-STAR INT'L CO.,LTD | | |
| | MS-V360 | | |
| | Size | Document Description | Rev |
| | Custom | GEFORCE LED & SLI LED | 2.0 |
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| | | |
|------------------------------|--------------------------------------|----------------|
| Size Custom | Document Description NV3V3, NV12V | Rev 2.0 |
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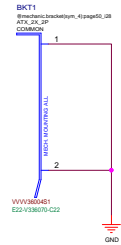


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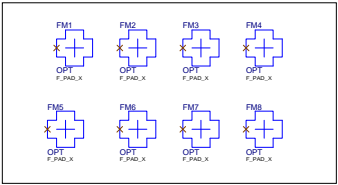
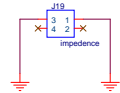
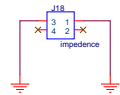
MS-V360

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|------------------------------|----------|-------------|----------------|
| Size | Document | Description | Rev |
| Custom | MCU | | 2.0 |
| Date: Friday, March 03, 2017 | | | Sheet 47 of 50 |

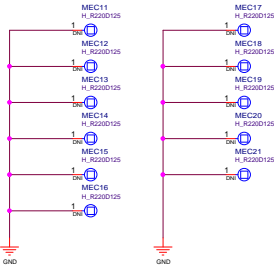
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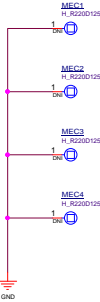
Screw



Mechanical Holes Symbol



GPU HOLES SYMBOL





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| MS-V360 | | | |
| Size | Document | Description | Rev |
| Custom | VR THERMAL PROTECTION | | 2.0 |
| Date: Friday, March 03, 2017 | | Sheet | 49 of 50 |

