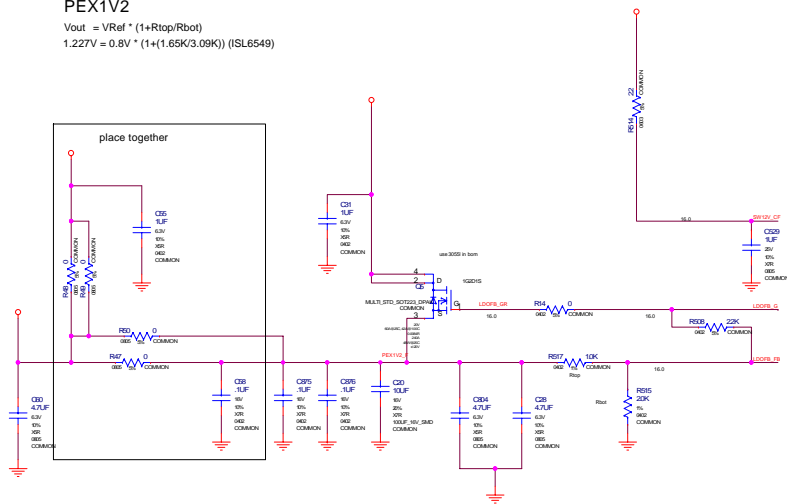


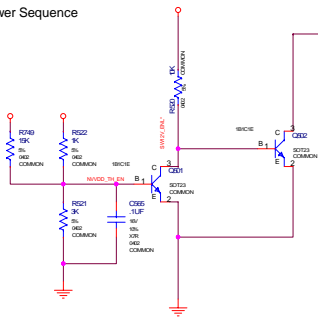
PowerSupplyIII: FBVDDQ, PEX1V2

PEX1V2

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

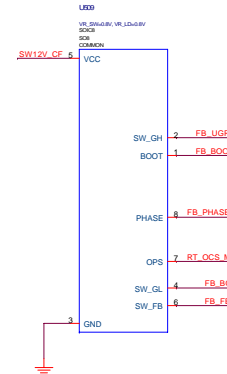
$$1.227V = 0.8V * (1 + (1.65K/3.09K)) \text{ (ISL6549)}$$


Power Sequence



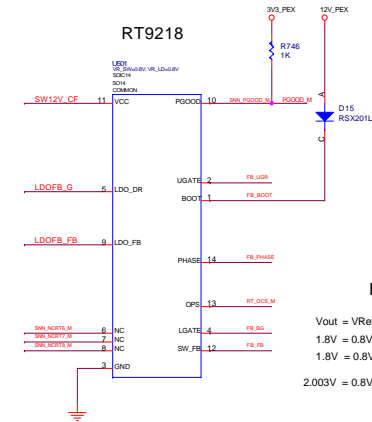
Power down option
A3V3 Rtop 15K Rbot 10K
NVDD Rtop 1K Rbot 3K

APW7120 / RT9214



FBVDDQ & PEX1V2

RT9218



FBVDDQ:-RT9218

Vout = VRef * (1+Rtop/Rbot)

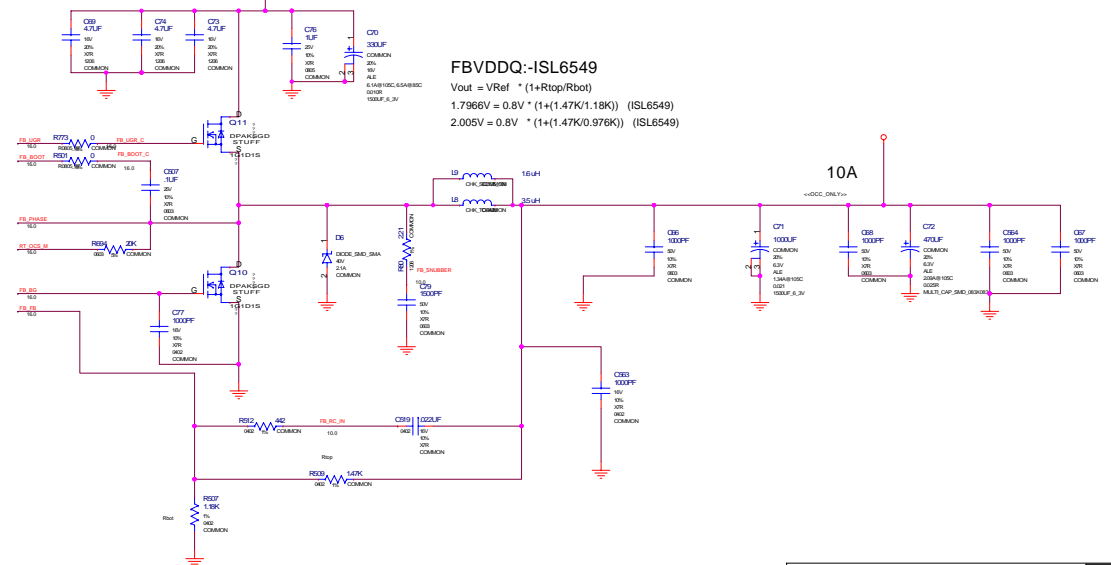
1.8V = 0.8V * (1+(5k/4k)) (RT9218)

1.8V = 0.8V * (1+(200/160)) (RT9218) Samsung MEM

2.003V = 0.8V * (1+(200/133)) (RT9218) Infineon MEM default

Net Name	LINE_WIDTH	CURRENT	Voltage
FBVDDQ	12MIL		1.8V

FBVDDQ:-ISL6549

$$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$$
$$1.7966V = 0.8V * (1 + (1.47K/1.18K)) \quad (ISL6549)$$
$$2.005V = 0.8V * (1 + (1.47K/0.976K)) \quad (ISL6549)$$


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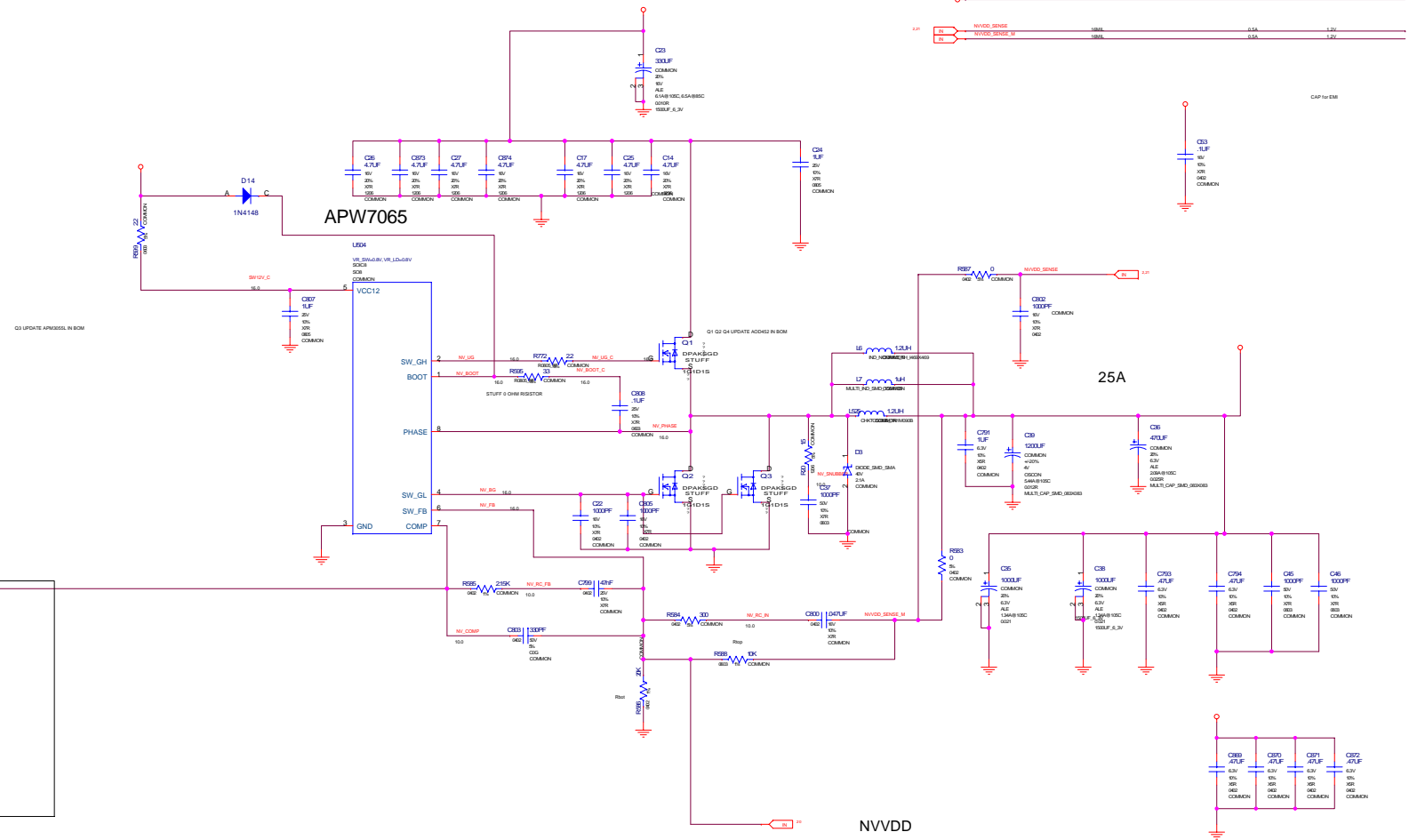
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PowerSupplyIR: FBVDDQ, PLLVDD

PowerSupplyII: NVVDD




NVDD

$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$

$1.1V = 0.8V * (1 + (1.54k/4.02k))$ (ISL6549)

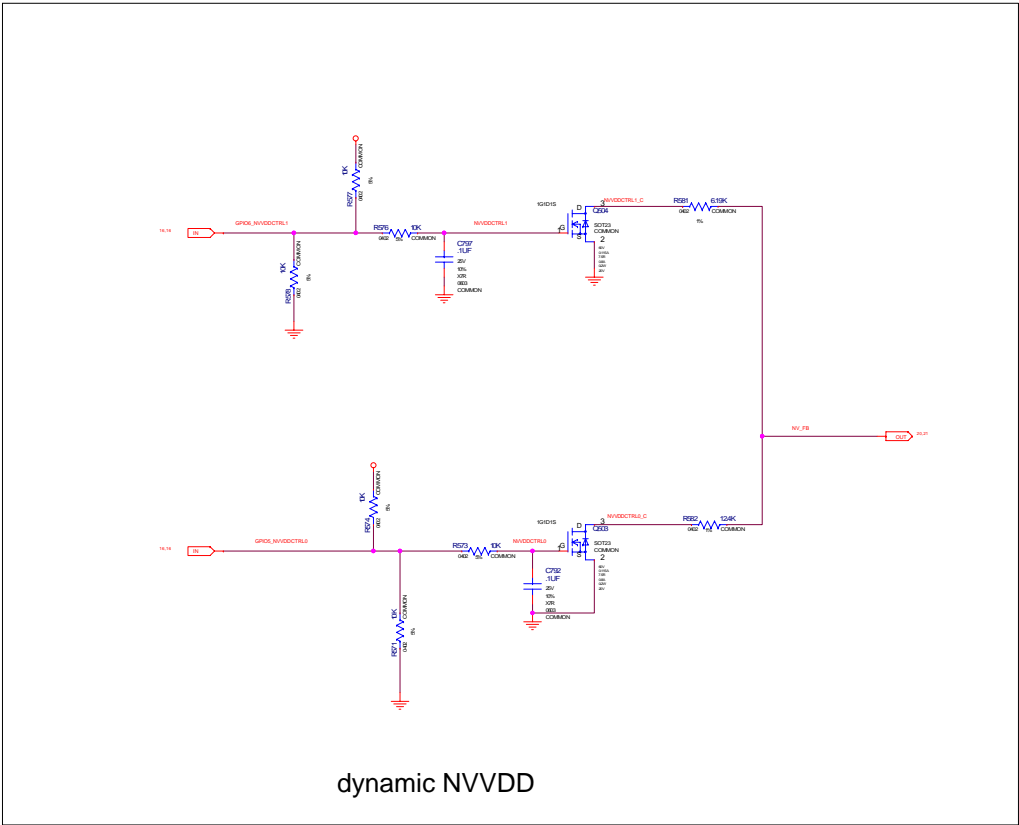
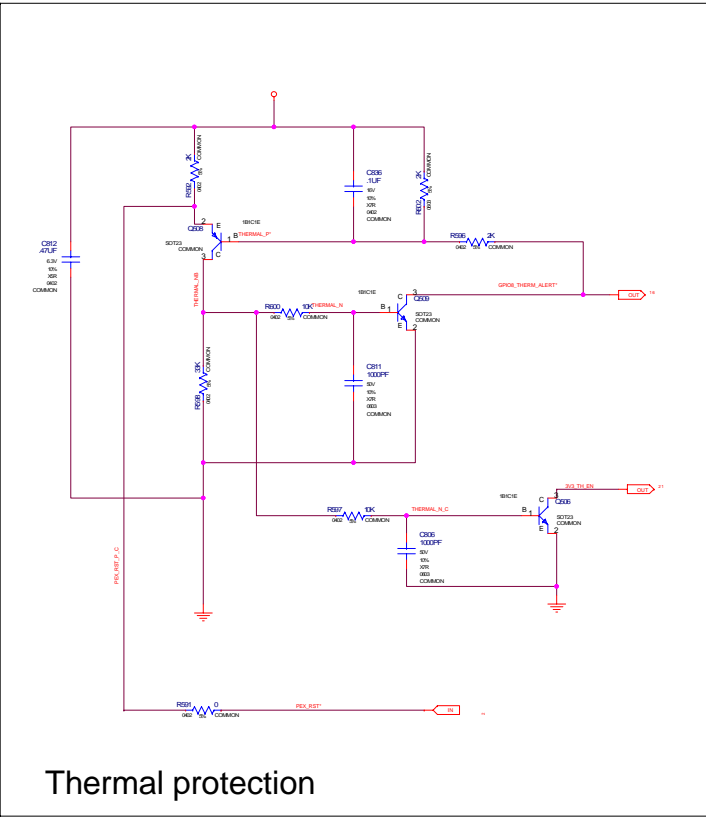
$1.2V = 0.8V * (1 + (1.54k/3.09k))$ (ISL6549)

$1.2V = 0.8V * (1 + (10k/20k))$ (APW7065)

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thermal protection and dynamic NVVDD



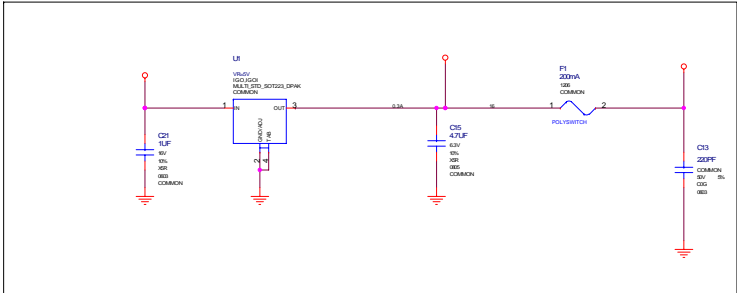
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal protection and dynamic NVVDD

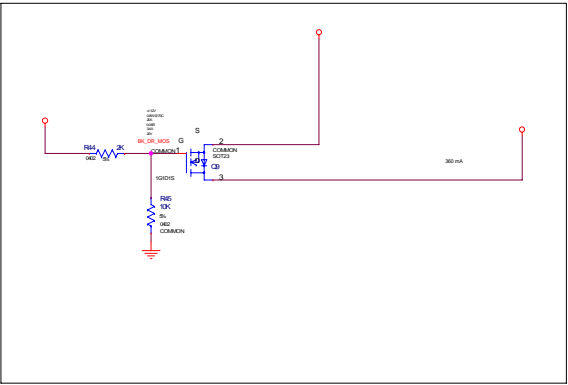
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NAME	DATE 12-JAN-2007

Power SupplyI:TMD5_IOVDD A3V3 DDC_5V IFF_PLLVDD

DDC 5V

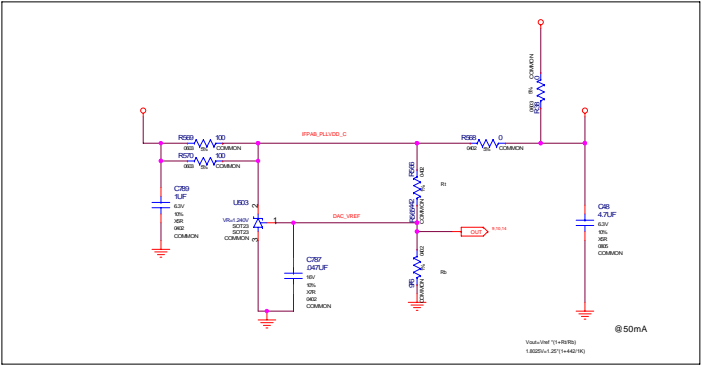


TMD5 IO SUPPLY WITH BACKDRIVE PROTECTION

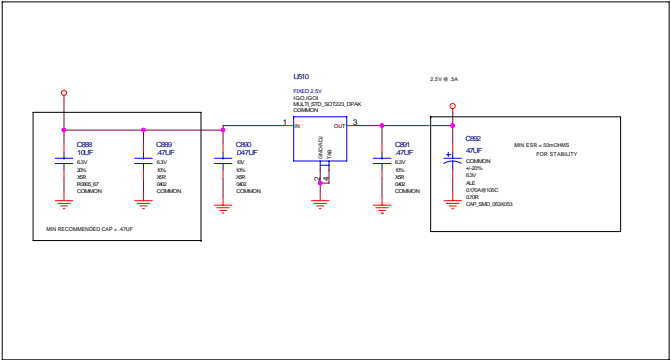


NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	0.1A	120	5.00000V
A3V3	1.5A	30.0	3.30000V
IFFAB_OVDD	0.3A	16	3.30000V
GND		30.0	0.000000V
IFF_PLLVDD	0.3A	16	1.80000V
MIOA_VDDQ	1A	1200	2.50V

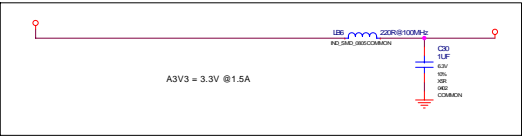
IFF_PLL SUPPLY



MIOA_VDDQ

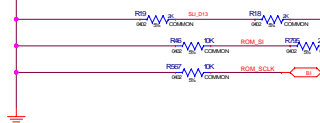


A3V3 Power Supply

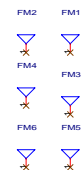


Straps

Mechanical parts

[illegible]

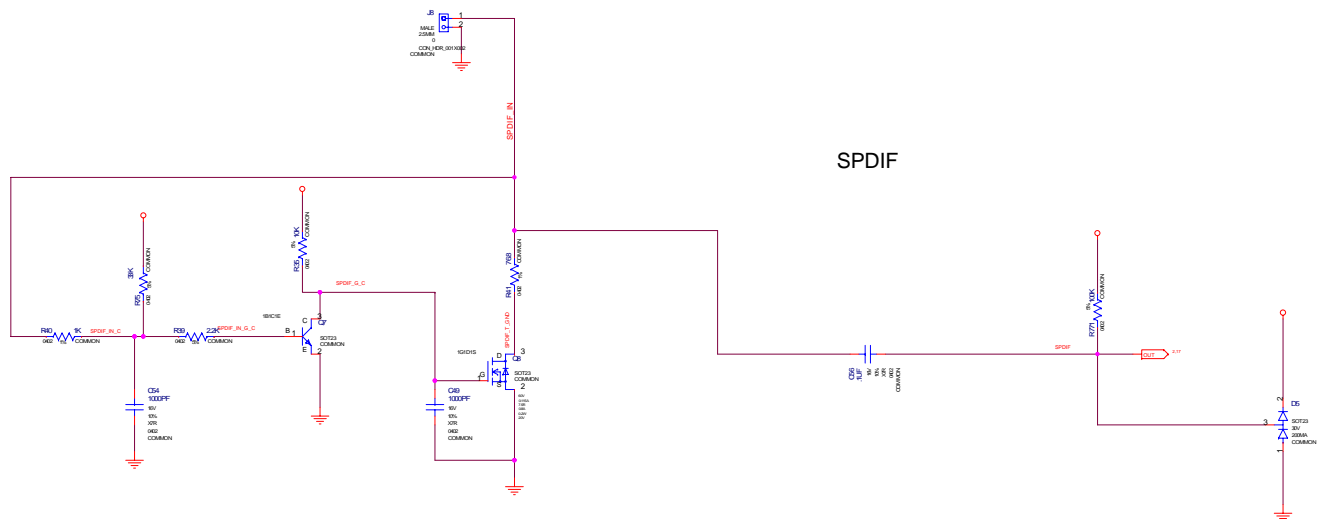
31: StrapOnTime per SW		
REG: NW_STRAP_1		
Bit Signal	VALUE_ID	VALUES
15: Set Clock Configuration		0:Disable 1:Enable
		0:2.5V 1:2.2V
12: MD_EN_33V_0	MDC_VDDO Voltage	0:2.5V 1:2.2V
13: MD_EN_33V_1	MDIO_VDDO Voltage	0:2.5V 1:2.2V
16: FCI_I2C0R		0:Disable 1:Enable



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Signal	Direction	Source	Destination
SPCKF	Input	SPCKF_IN	SPCKF
SPCKF	Output	SPCKF_OUT	SPCKF



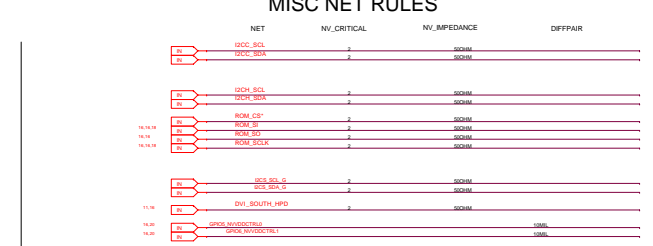
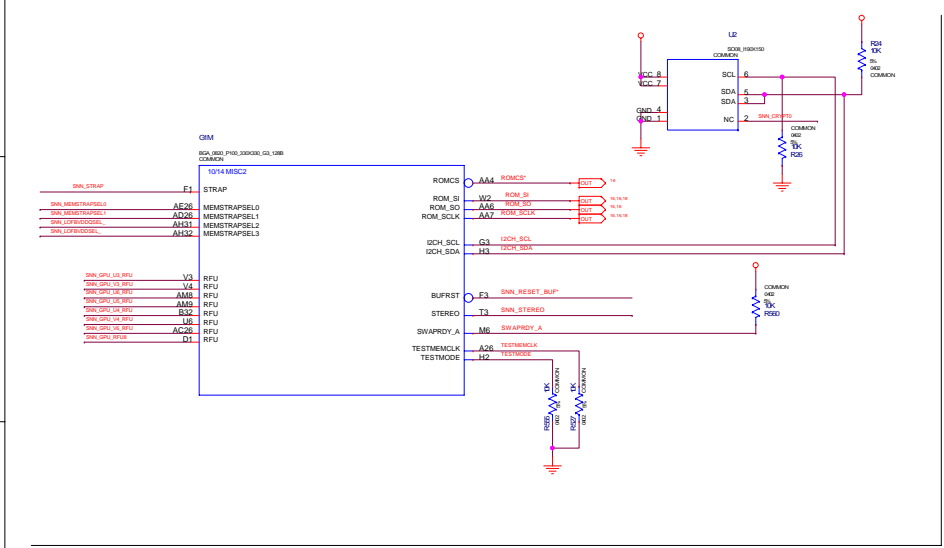
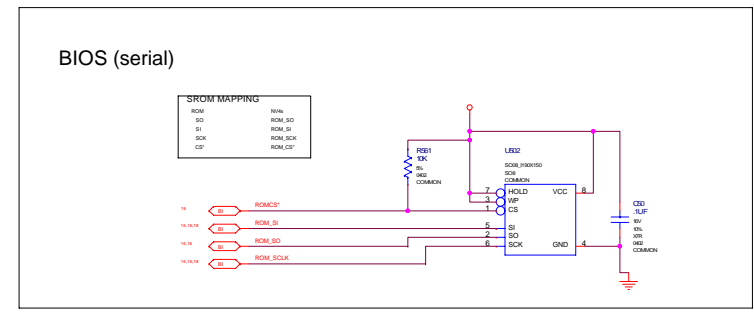
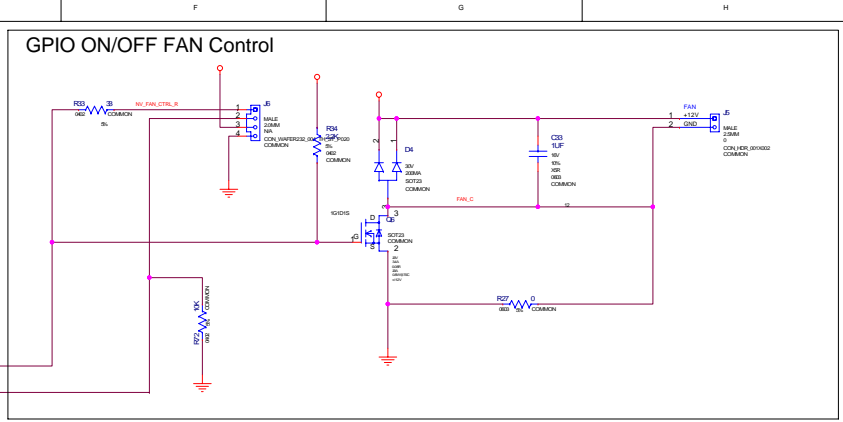
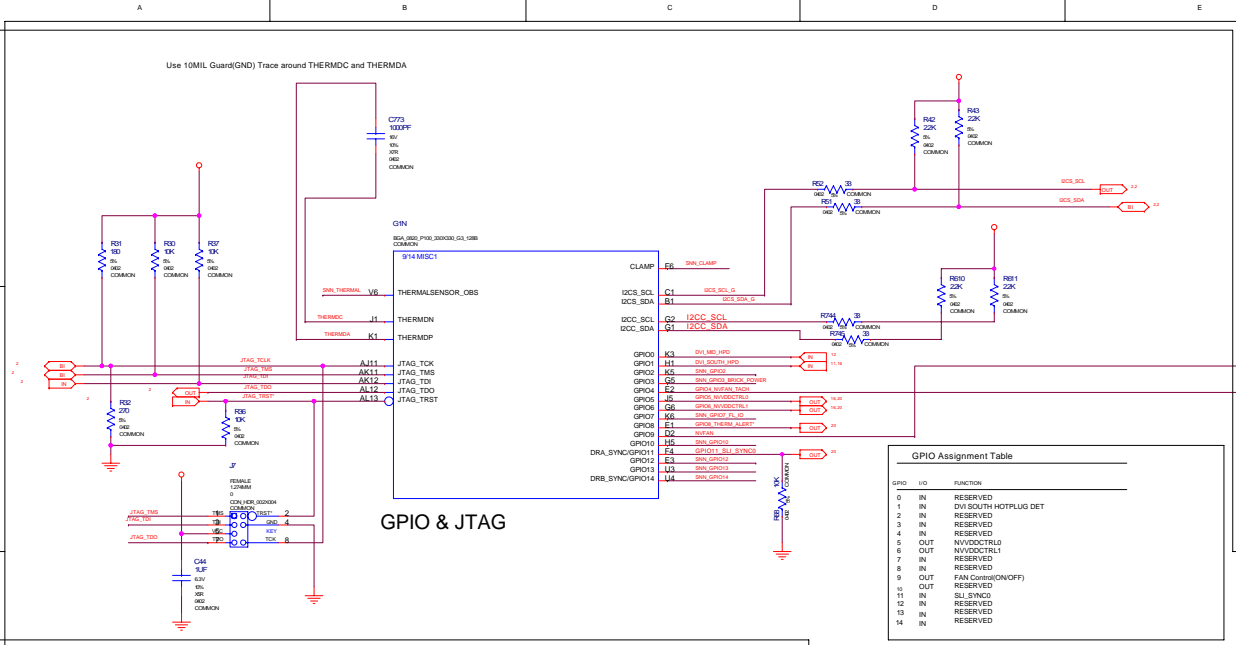
place close to GPU

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF

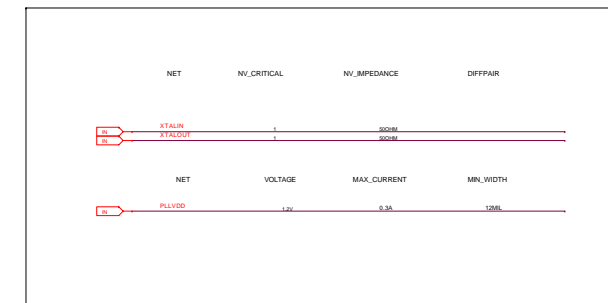
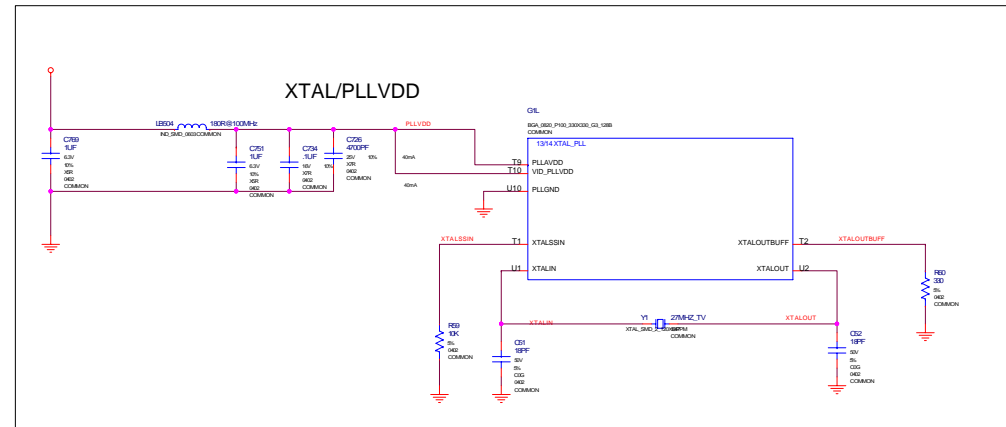
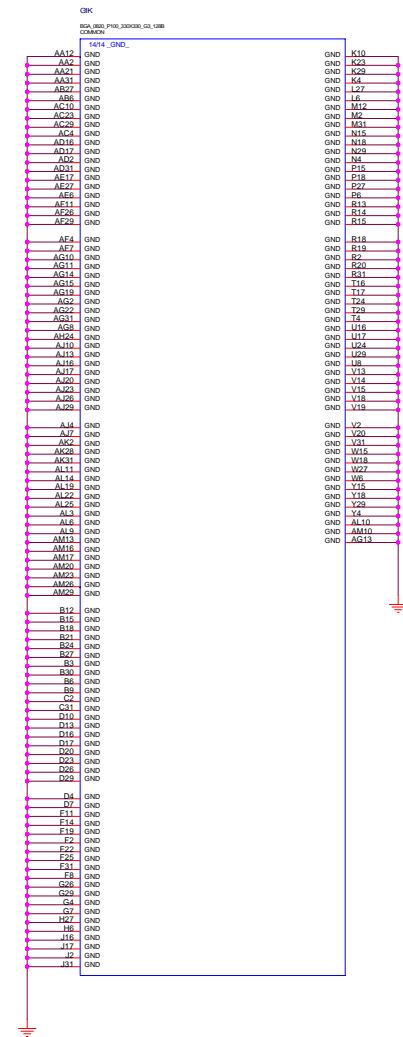
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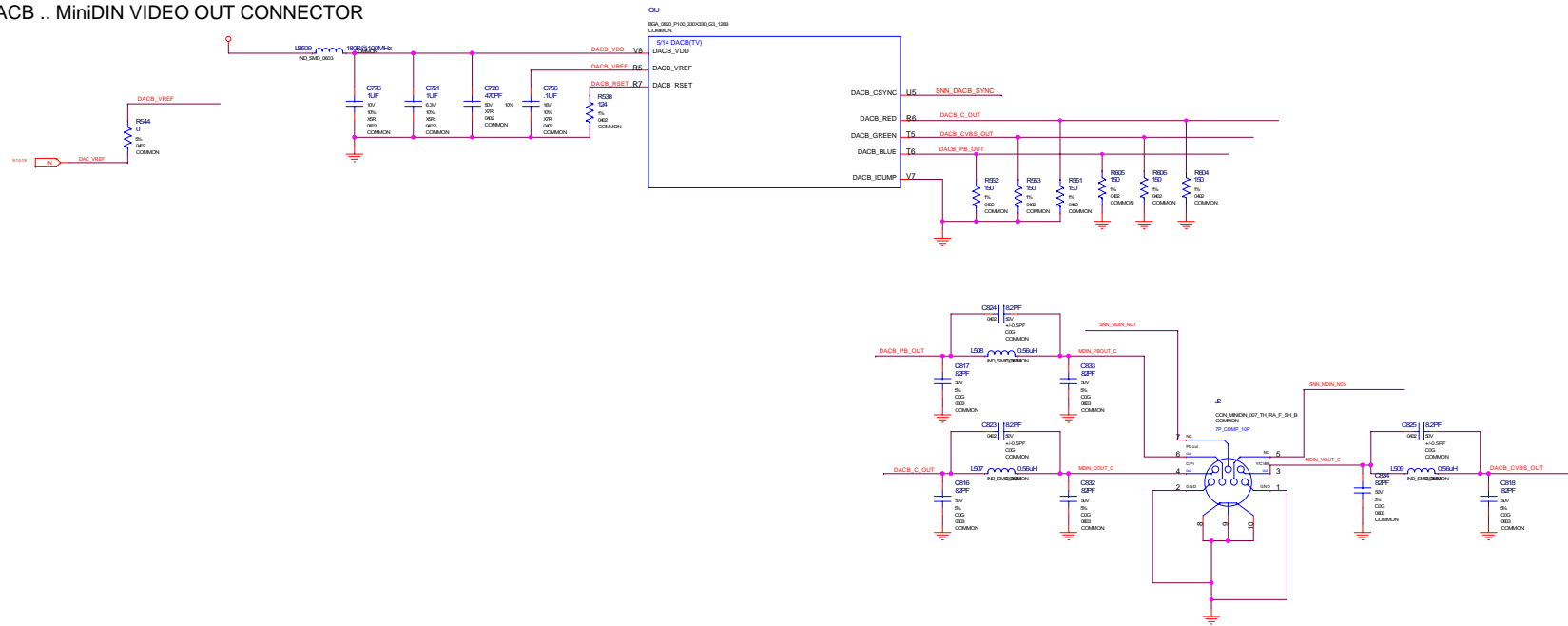
GPU GND CONNECTION, XTAL



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DACB .. MiniDIN VIDEO OUT CONNECTOR



DACB NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	TV_OHIO_F	1	500M	
IN	MON_YCOUT_C	1	500M	
IN	TV_LUMA_F	1	500M	
IN	MON_YDOUT_C	1	500M	
IN	TV_CVBS_F	1	500M	
IN	MON_PROUT_C	1	500M	

Signal	Direction	Width	Unit
MDIN_SCL_C	Input	2	500UM
MDIN_SDA_C	Input	2	500UM

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN DACS_VDD	3.30000V	0.07A	16.0
IN DACS_VREF			16.0
IN DACS_RSET			16.0

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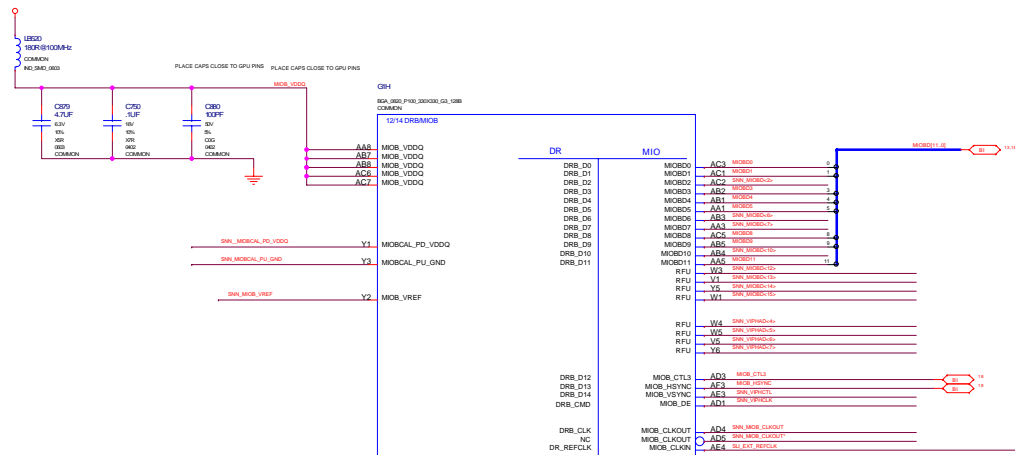
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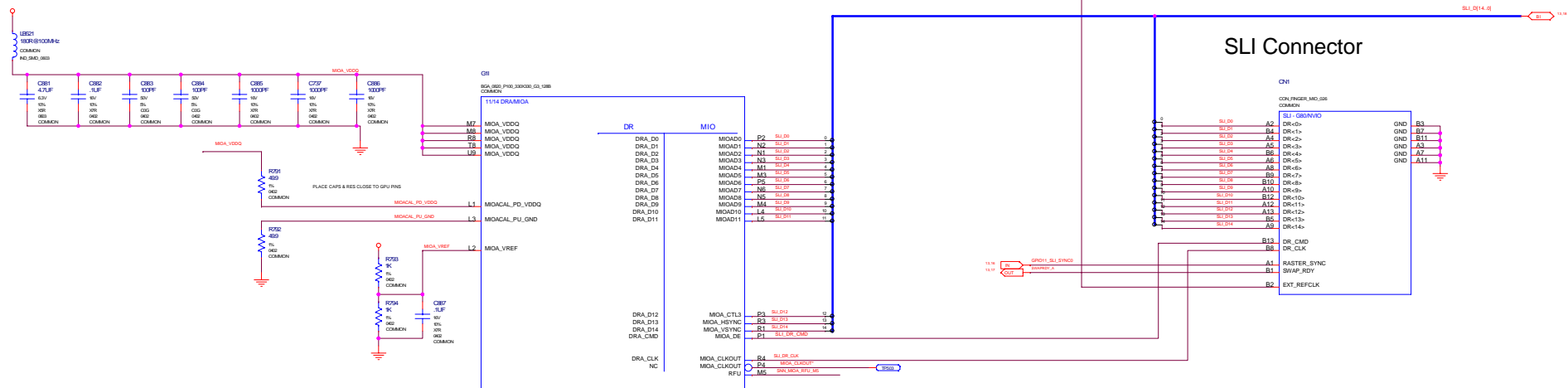
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, SYNC STRIPPER, MINIDIN CONNECTOR NORTH, HDTV HEADER

G3 VIP/MIOB

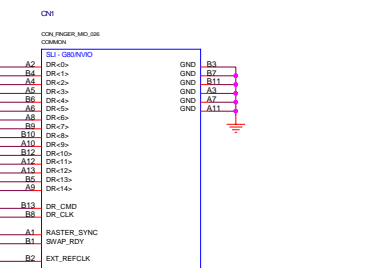


G3 MIOA



MIO NET RULES

SLI Connector



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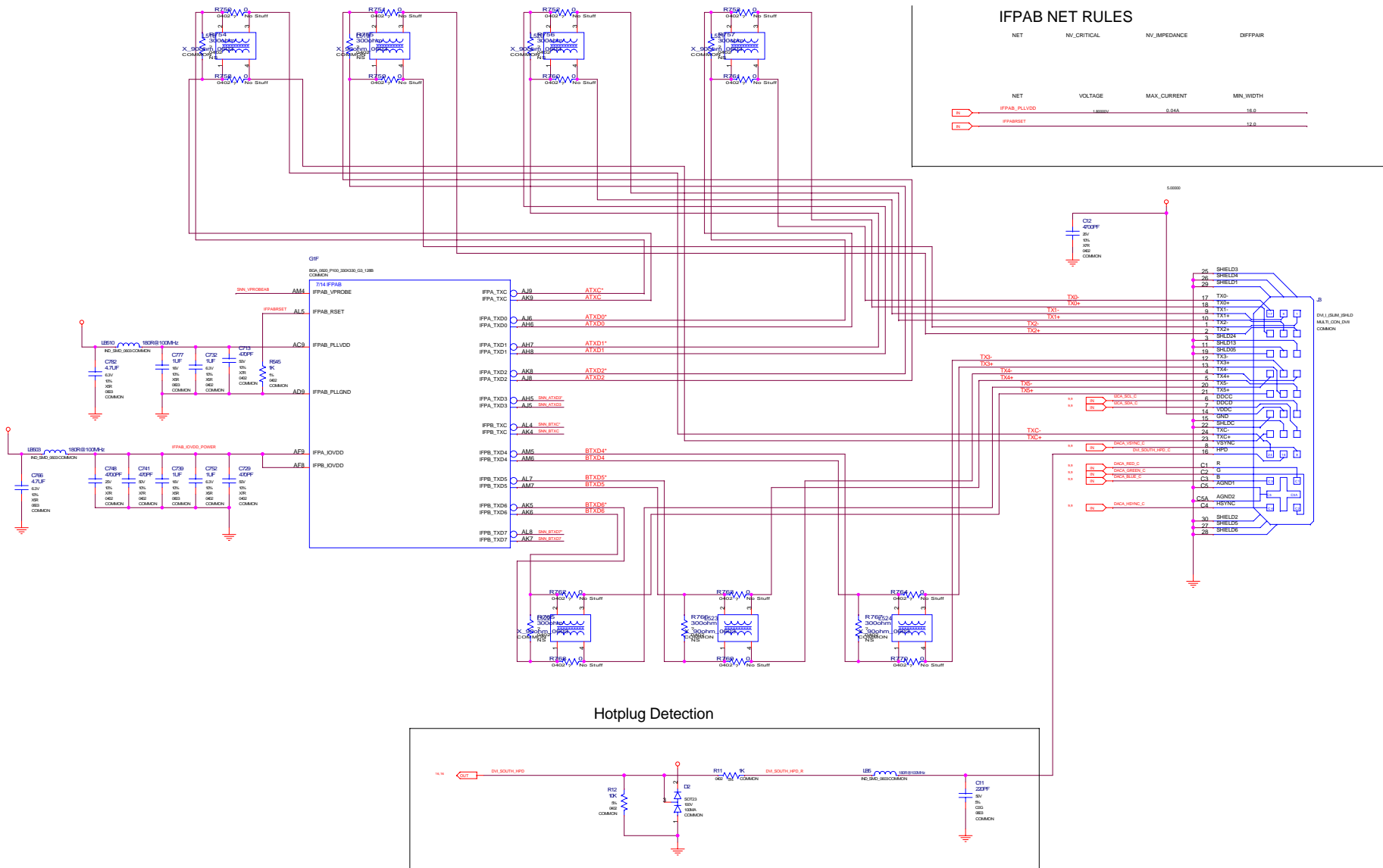
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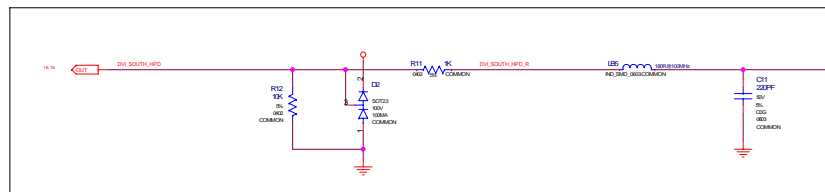
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PAGE DETAIL	MOA & MOB

INTERNAL TMDS .. LINK A & B



Hotplug Detection



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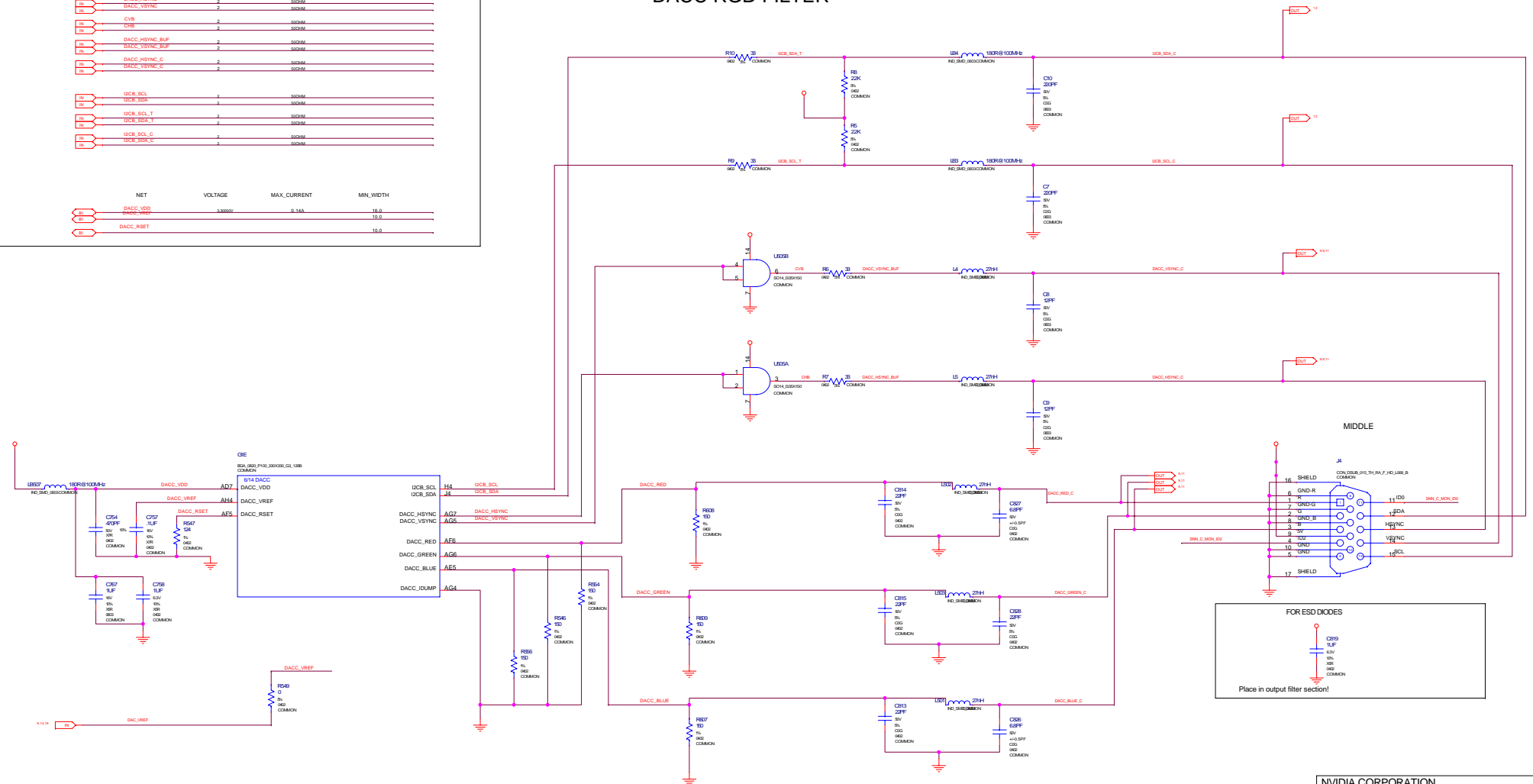
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DACC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACC_RED	1	50OHM	
DACC_GREEN	1	50OHM	
DACC_BLUE	1	50OHM	
DACC_RED_C	1	50OHM	
DACC_GREEN_C	1	50OHM	
DACC_BLUE_C	1	50OHM	
DACC_HSYNC	2	50OHM	
DACC_VSYNC	2	50OHM	
CVR	2	50OHM	
CVR	2	50OHM	
DACC_HSYNC_BUF	2	50OHM	
DACC_VSYNC_BUF	2	50OHM	
DACC_HSYNC_C	2	50OHM	
DACC_VSYNC_C	2	50OHM	
DCC_SCL	2	50OHM	
DCC_SDA	2	50OHM	
DCC_SCL_T	2	50OHM	
DCC_SDA_T	2	50OHM	
DCC_SCL_C	2	50OHM	
DCC_SDA_C	2	50OHM	
DACC_VDD	3.3000V	0.16A	18.0
DACC_VREF			18.0
DACC_RSET			18.0

Secondary Display (DACC), DB15

DACC RGB-FILTER



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PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID

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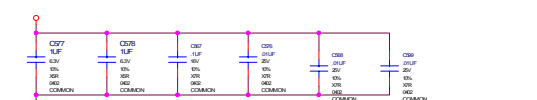
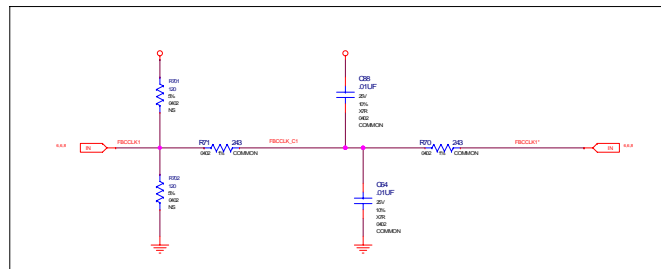
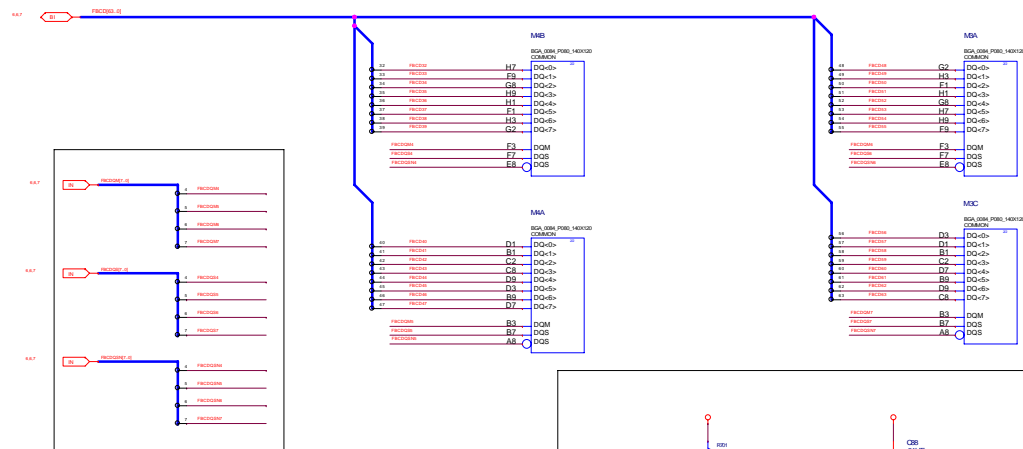
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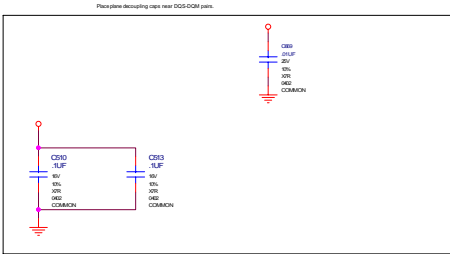
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PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



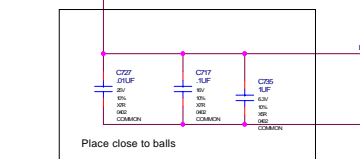
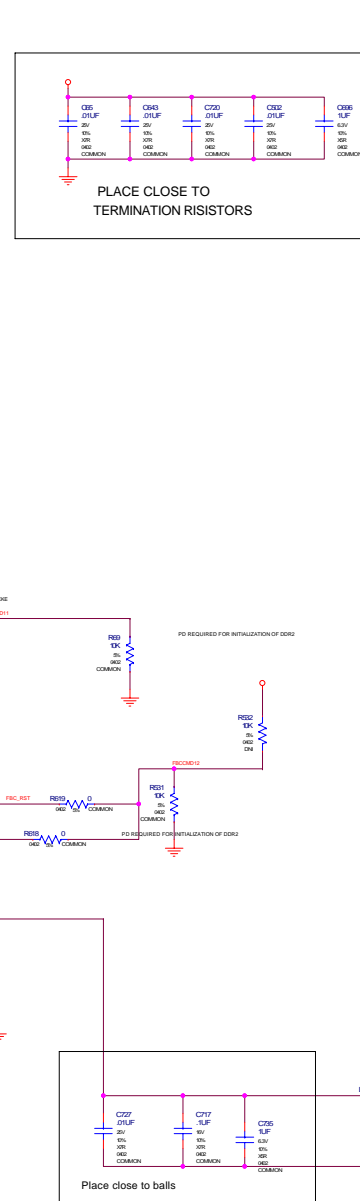
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16MX16 DDR2 MEMORIES, 2ND BANK 0.31

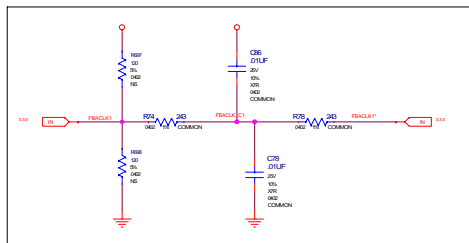
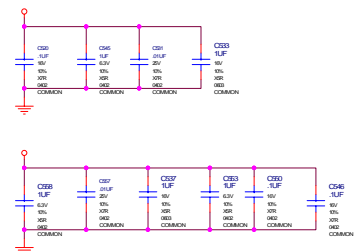
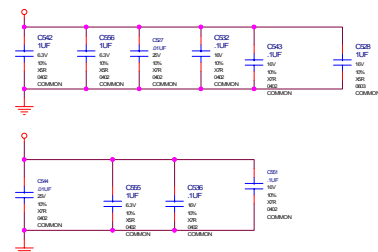
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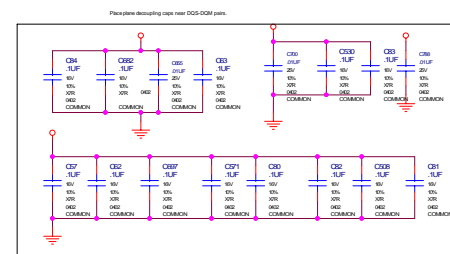
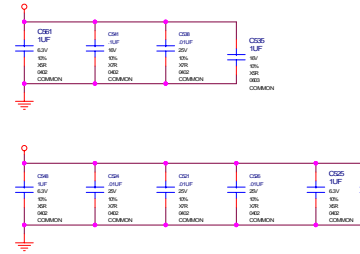
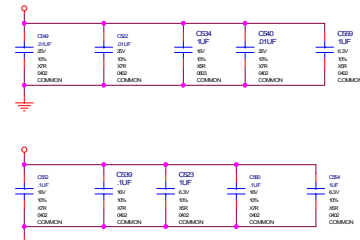
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

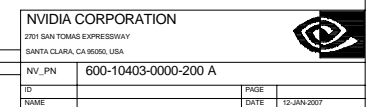


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16Mx16 DDR2 MEMORIES, BANK 0..31

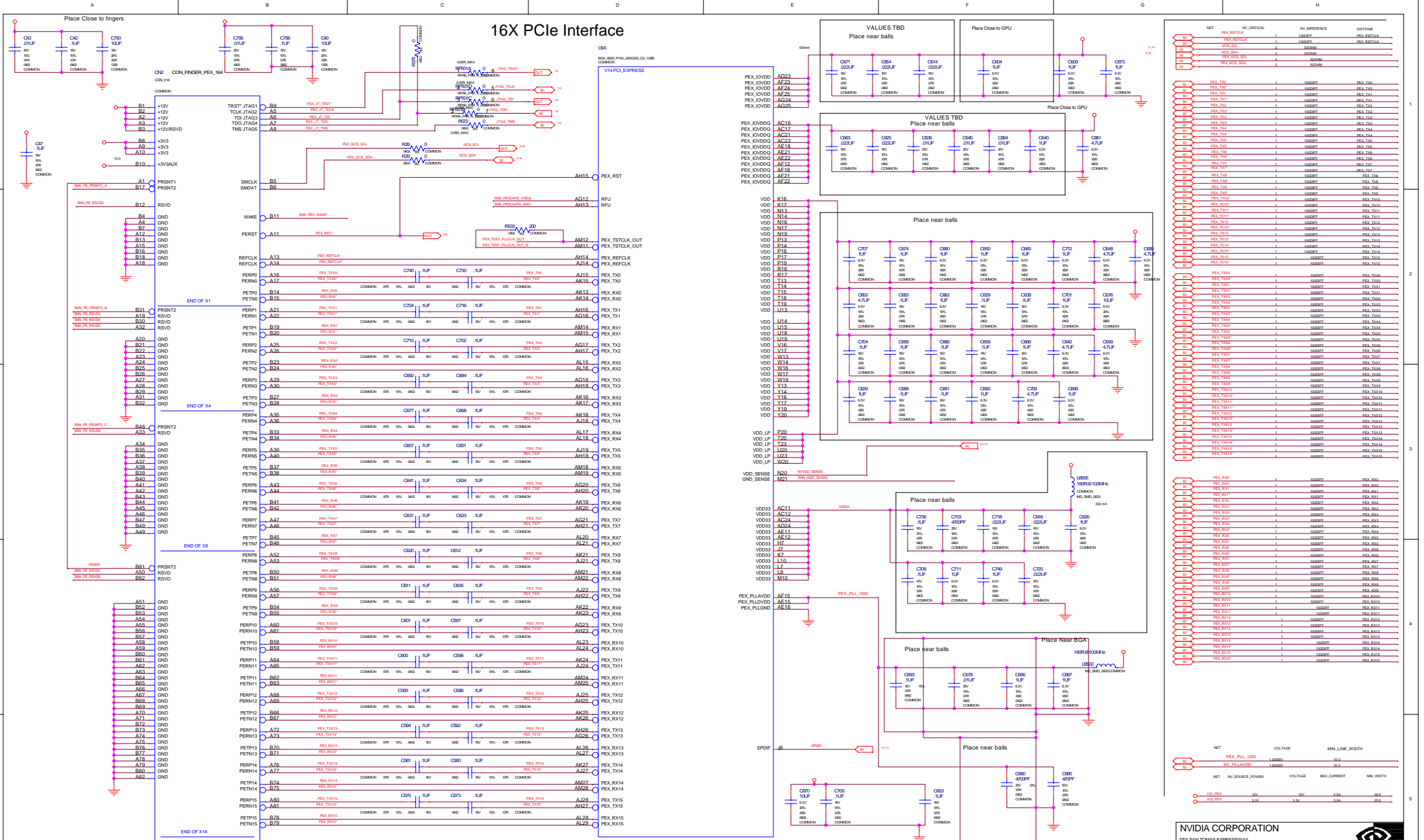


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	NET	NV_CRITICAL	NV_PREFERENCE	DIFFPBR
B1	PEX_REFCLK	1	1000T	PEX_REFCLK
B1	PEX_REFCLK	1	1000T	PEX_REFCLK
B1	WCS_SCL	2	5000M	
B1	WCS_GDA	2	5000M	
B1	PEX_WCS_SCL	2	5000M	
B1	PEX_WCS_GDA	2	5000M	

FE1	FE1-106	+	1000000	FE1-206
FE2	FE2-107	+	1000000	FE2-207
FE3	FE3-108	+	1000000	FE3-208
FE4	FE4-109	+	1000000	FE4-209
FE5	FE5-110	+	1000000	FE5-210
FE6	FE6-111	+	1000000	FE6-211
FE7	FE7-112	+	1000000	FE7-212
FE8	FE8-113	+	1000000	FE8-213
FE9	FE9-114	+	1000000	FE9-214
FE10	FE10-115	+	1000000	FE10-215
FE11	FE11-116	+	1000000	FE11-216
FE12	FE12-117	+	1000000	FE12-217
FE13	FE13-118	+	1000000	FE13-218
FE14	FE14-119	+	1000000	FE14-219
FE15	FE15-120	+	1000000	FE15-220
FE16	FE16-121	+	1000000	FE16-221
FE17	FE17-122	+	1000000	FE17-222
FE18	FE18-123	+	1000000	FE18-223
FE19	FE19-124	+	1000000	FE19-224
FE20	FE20-125	+	1000000	FE20-225
FE21	FE21-126	+	1000000	FE21-226
FE22	FE22-127	+	1000000	FE22-227
FE23	FE23-128	+	1000000	FE23-228
FE24	FE24-129	+	1000000	FE24-229
FE25	FE25-130	+	1000000	FE25-230
FE26	FE26-131	+	1000000	FE26-231
FE27	FE27-132	+	1000000	FE27-232
FE28	FE28-133	+	1000000	FE28-233
FE29	FE29-134	+	1000000	FE29-234
FE30	FE30-135	+	1000000	FE30-235
FE31	FE31-136	+	1000000	FE31-236
FE32	FE32-137	+	1000000	FE32-237
FE33	FE33-138	+	1000000	FE33-238
FE34	FE34-139	+	1000000	FE34-239
FE35	FE35-140	+	1000000	FE35-240
FE36	FE36-141	+	1000000	FE36-241
FE37	FE37-142	+	1000000	FE37-242
FE38	FE38-143	+	1000000	FE38-243
FE39	FE39-144	+	1000000	FE39-244
FE40	FE40-145	+	1000000	FE40-245
FE41	FE41-146	+	1000000	FE41-246
FE42	FE42-147	+	1000000	FE42-247
FE43	FE43-148	+	1000000	FE43-248
FE44	FE44-149	+	1000000	FE44-249
FE45	FE45-150	+	1000000	FE45-250
FE46	FE46-151	+	1000000	FE46-251
FE47	FE47-152	+	1000000	FE47-252
FE48	FE48-153	+	1000000	FE48-253
FE49	FE49-154	+	1000000	FE49-254
FE50	FE50-155	+	1000000	FE50-255
FE51	FE51-156	+	1000000	FE51-256
FE52	FE52-157	+	1000000	FE52-257
FE53	FE53-158	+	1000000	FE53-258
FE54	FE54-159	+	1000000	FE54-259
FE55	FE55-160	+	1000000	FE55-260
FE56	FE56-161	+	1000000	FE56-261
FE57	FE57-162	+	1000000	FE57-262
FE58	FE58-163	+	1000000	FE58-263
FE59	FE59-164	+	1000000	FE59-264
FE60	FE60-165	+	1000000	FE60-265
FE61	FE61-166	+	1000000	FE61-266
FE62	FE62-167	+	1000000	FE62-267
FE63	FE63-168	+	1000000	FE63-268
FE64	FE64-169	+	1000000	FE64-269
FE65	FE65-170	+	1000000	FE65-270
FE66	FE66-171	+	1000000	FE66-271
FE67	FE67-172	+	1000000	FE67-272
FE68	FE68-173	+	1000000	FE68-273
FE69	FE69-174	+	1000000	FE69-274
FE70	FE70-175	+	1000000	FE70-275
FE71	FE71-176	+	1000000	FE71-276
FE72	FE72-177	+	1000000	FE72-277
FE73	FE73-178	+	1000000	FE73-278
FE74	FE74-179	+	1000000	FE74-279
FE75	FE75-180	+	1000000	FE75-280
FE76	FE76-181	+	1000000	FE76-281
FE77	FE77-182	+	1000000	FE77-282
FE78	FE78-183	+	1000000	FE78-283
FE79	FE79-184	+	1000000	FE79-284
FE80	FE80-185	+	1000000	FE80-285
FE81	FE81-186	+	1000000	FE81-286
FE82	FE82-187	+	1000000	FE82-287
FE83	FE83-188	+	1000000	FE83-288
FE84	FE84-189	+	1000000	FE84-289
FE85	FE85-190	+	1000000	FE85-290
FE86	FE86-191	+	1000000	FE86-291
FE87	FE87-192	+	1000000	FE87-292
FE88	FE88-193	+	1000000	FE88-293
FE89	FE89-194	+	1000000	FE89-294
FE90	FE90-195	+	1000000	FE90-295
FE91	FE91-196	+	1000000	FE91-296
FE92	FE92-197	+	1000000	FE92-297
FE93	FE93-198	+	1000000	FE93-298
FE94	FE94-199	+	1000000	FE94-299
FE95	FE95-200	+	1000000	FE95-300

01	PEX_R00	+	UNOFF	PEX_R00
02	PEX_R01	+	UNOFF	PEX_R01
03	PEX_R02	+	UNOFF	PEX_R02
04	PEX_R03	+	UNOFF	PEX_R03
05	PEX_R04	+	UNOFF	PEX_R04
06	PEX_R05	+	UNOFF	PEX_R05
07	PEX_R06	+	UNOFF	PEX_R06
08	PEX_R07	+	UNOFF	PEX_R07
09	PEX_R08	+	UNOFF	PEX_R08
0A	PEX_R09	+	UNOFF	PEX_R09
0B	PEX_R0A	+	UNOFF	PEX_R0A
0C	PEX_R0B	+	UNOFF	PEX_R0B
0D	PEX_R0C	+	UNOFF	PEX_R0C
0E	PEX_R0D	+	UNOFF	PEX_R0D
0F	PEX_R0E	+	UNOFF	PEX_R0E
10	PEX_R0F	+	UNOFF	PEX_R0F
11	PEX_R10	+	UNOFF	PEX_R10
12	PEX_R11	+	UNOFF	PEX_R11
13	PEX_R12	+	UNOFF	PEX_R12
14	PEX_R13	+	UNOFF	PEX_R13
15	PEX_R14	+	UNOFF	PEX_R14
16	PEX_R15	+	UNOFF	PEX_R15
17	PEX_R16	+	UNOFF	PEX_R16
18	PEX_R17	+	UNOFF	PEX_R17
19	PEX_R18	+	UNOFF	PEX_R18
1A	PEX_R19	+	UNOFF	PEX_R19
1B	PEX_R1A	+	UNOFF	PEX_R1A
1C	PEX_R1B	+	UNOFF	PEX_R1B
1D	PEX_R1C	+	UNOFF	PEX_R1C
1E	PEX_R1D	+	UNOFF	PEX_R1D
1F	PEX_R1E	+	UNOFF	PEX_R1E
20	PEX_R1F	+	UNOFF	PEX_R1F
21	PEX_R20	+	UNOFF	PEX_R20
22	PEX_R21	+	UNOFF	PEX_R21
23	PEX_R22	+	UNOFF	PEX_R22
24	PEX_R23	+	UNOFF	PEX_R23
25	PEX_R24	+	UNOFF	PEX_R24
26	PEX_R25	+	UNOFF	PEX_R25
27	PEX_R26	+	UNOFF	PEX_R26
28	PEX_R27	+	UNOFF	PEX_R27
29	PEX_R28	+	UNOFF	PEX_R28
2A	PEX_R29	+	UNOFF	PEX_R29
2B	PEX_R2A	+	UNOFF	PEX_R2A
2C	PEX_R2B	+	UNOFF	PEX_R2B
2D	PEX_R2C	+	UNOFF	PEX_R2C
2E	PEX_R2D	+	UNOFF	PEX_R2D
2F	PEX_R2E	+	UNOFF	PEX_R2E
30	PEX_R2F	+	UNOFF	PEX_R2F
31	PEX_R30	+	UNOFF	PEX_R30
32	PEX_R31	+	UNOFF	PEX_R31
33	PEX_R32	+	UNOFF	PEX_R32
34	PEX_R33	+	UNOFF	PEX_R33
35	PEX_R34	+	UNOFF	PEX_R34
36	PEX_R35	+	UNOFF	PEX_R35
37	PEX_R36	+	UNOFF	PEX_R36
38	PEX_R37	+	UNOFF	PEX_R37
39	PEX_R38	+	UNOFF	PEX_R38
3A	PEX_R39	+	UNOFF	PEX_R39
3B	PEX_R3A	+	UNOFF	PEX_R3A
3C	PEX_R3B	+	UNOFF	PEX_R3B
3D	PEX_R3C	+	UNOFF	PEX_R3C
3E	PEX_R3D	+	UNOFF	PEX_R3D
3F	PEX_R3E	+	UNOFF	PEX_R3E
40	PEX_R3F	+	UNOFF	PEX_R3F
41	PEX_R40	+	UNOFF	PEX_R40
42	PEX_R41	+	UNOFF	PEX_R41
43	PEX_R42	+	UNOFF	PEX_R42
44	PEX_R43	+	UNOFF	PEX_R43
45	PEX_R44	+	UNOFF	PEX_R44
46	PEX_R45	+	UNOFF	PEX_R45
47	PEX_R46	+	UNOFF	PEX_R46
48	PEX_R47	+	UNOFF	PEX_R47
49	PEX_R48	+	UNOFF	PEX_R48
4A	PEX_R49	+	UNOFF	PEX_R49
4B	PEX_R4A	+	UNOFF	PEX_R4A
4C	PEX_R4B	+	UNOFF	PEX_R4B
4D	PEX_R4C	+	UNOFF	PEX_R4C
4E	PEX_R4D	+	UNOFF	PEX_R4D
4F	PEX_R4E	+	UNOFF	PEX_R4E
50	PEX_R4F	+	UNOFF	PEX_R4F
51	PEX_R50	+	UNOFF	PEX_R50
52	PEX_R51	+	UNOFF	PEX_R51
53	PEX_R52	+	UNOFF	PEX_R52
54	PEX_R53	+	UNOFF	PEX_R53
55	PEX_R54	+	UNOFF	PEX_R54
56	PEX_R55	+	UNOFF	PEX_R55
57	PEX_R56	+	UNOFF	PEX_R56
58	PEX_R57	+	UNOFF	PEX_R57
59	PEX_R58	+	UNOFF	PEX_R58
5A	PEX_R59	+	UNOFF	PEX_R59
5B	PEX_R5A	+	UNOFF	PEX_R5A
5C	PEX_R5B	+	UNOFF	PEX_R5B
5D	PEX_R5C	+	UNOFF	PEX_R5C</

Timing diagram for the PEX PLL VDD signal. The diagram shows a square wave signal labeled "PEX_PLL_VDD" with a period of 1.000000 and a high level of 3.0. The signal is connected to the "NV_PLAVDD" pin of the "NET" block. The "NET" block also has inputs for "NV_SOURCE_POWER" (3.0V), "VOLTAGE" (3.0V), "MNU_CURRENT" (5.0A), and "MNU_WIDTH" (3.0). The "NET" block is connected to a "100_PEX4" block, which has inputs for "100_PEX4" (3.0V), "100_PEX4" (3.0V), "100_PEX4" (3.0V), and "100_PEX4" (3.0V).



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PAGE DETAIL	PCI EXPRESS 16X, NVDD DECOUPLING CAPS, PEX, IOVDD DECOUPLING CAPS

	PAGE DETAIL
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P403-B00 DESIGN -- G84-200, 256 MB DDR2,DVI-I, VGA, HDTV

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REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10403-0000-200	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SK0000	600-10403-0000-200	P403 B00 G84-200 459400MHz 256MB 16Mx16 BG484 GDDR2 DVI-I DL+VGA+HDTV-Out
2	SK0001	600-10403-0001-200	P403 B00 G84-200 459400MHz 256MB 16Mx16 BG484 GDDR2 DVI-I DL+VGA+HDTV-Out
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