

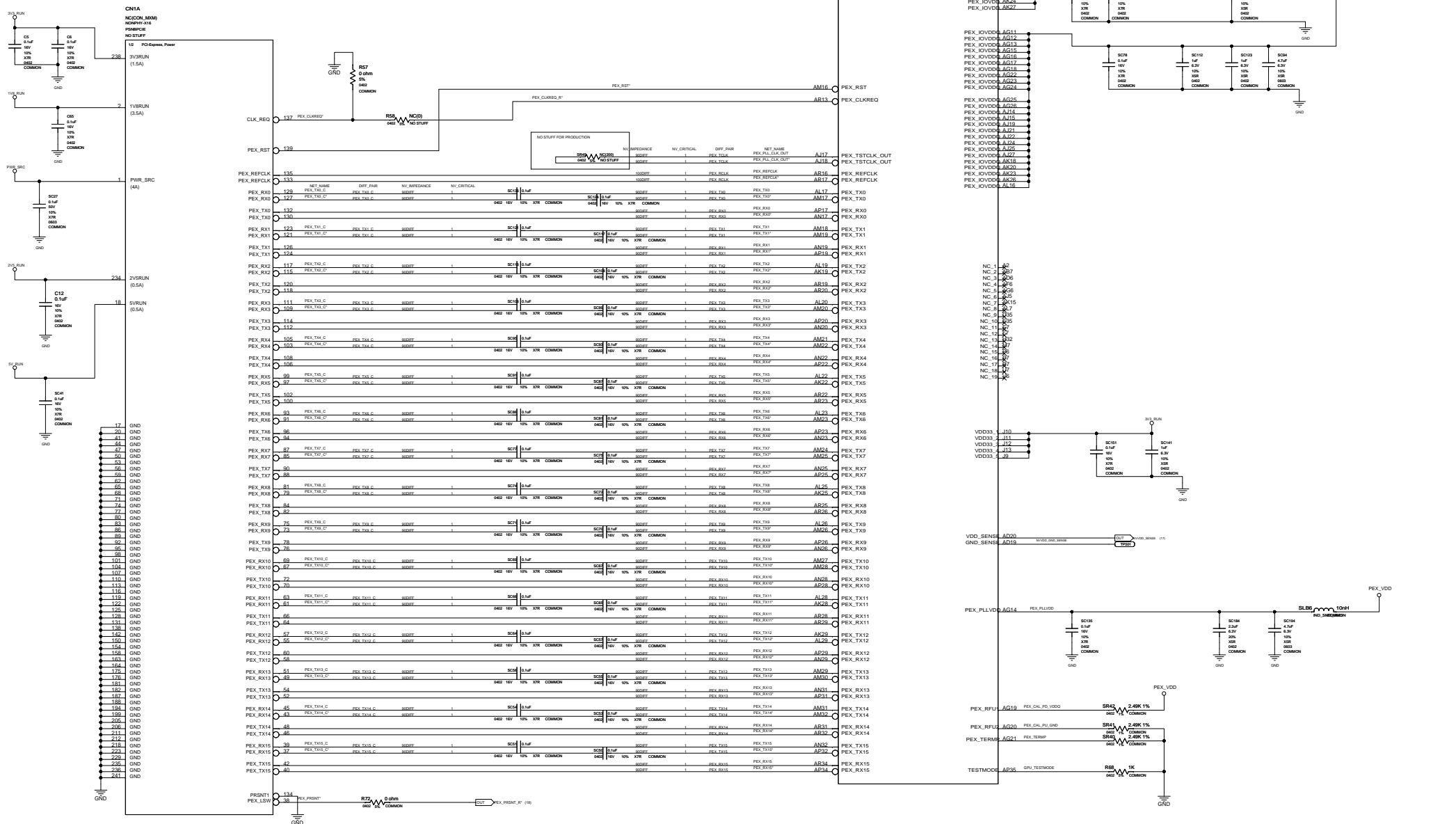
P601 REV:1.2 : G96-GS/GE2-128, MXM-II, 512/256MB DDR2 (32/16Mx16)
LVDS, DP-A/B, DVI-A/B/C, TV_OUT, VGA, HD AUDIO, SPDIF
MXM 2.1a SPECIFICATION COMPLIANT

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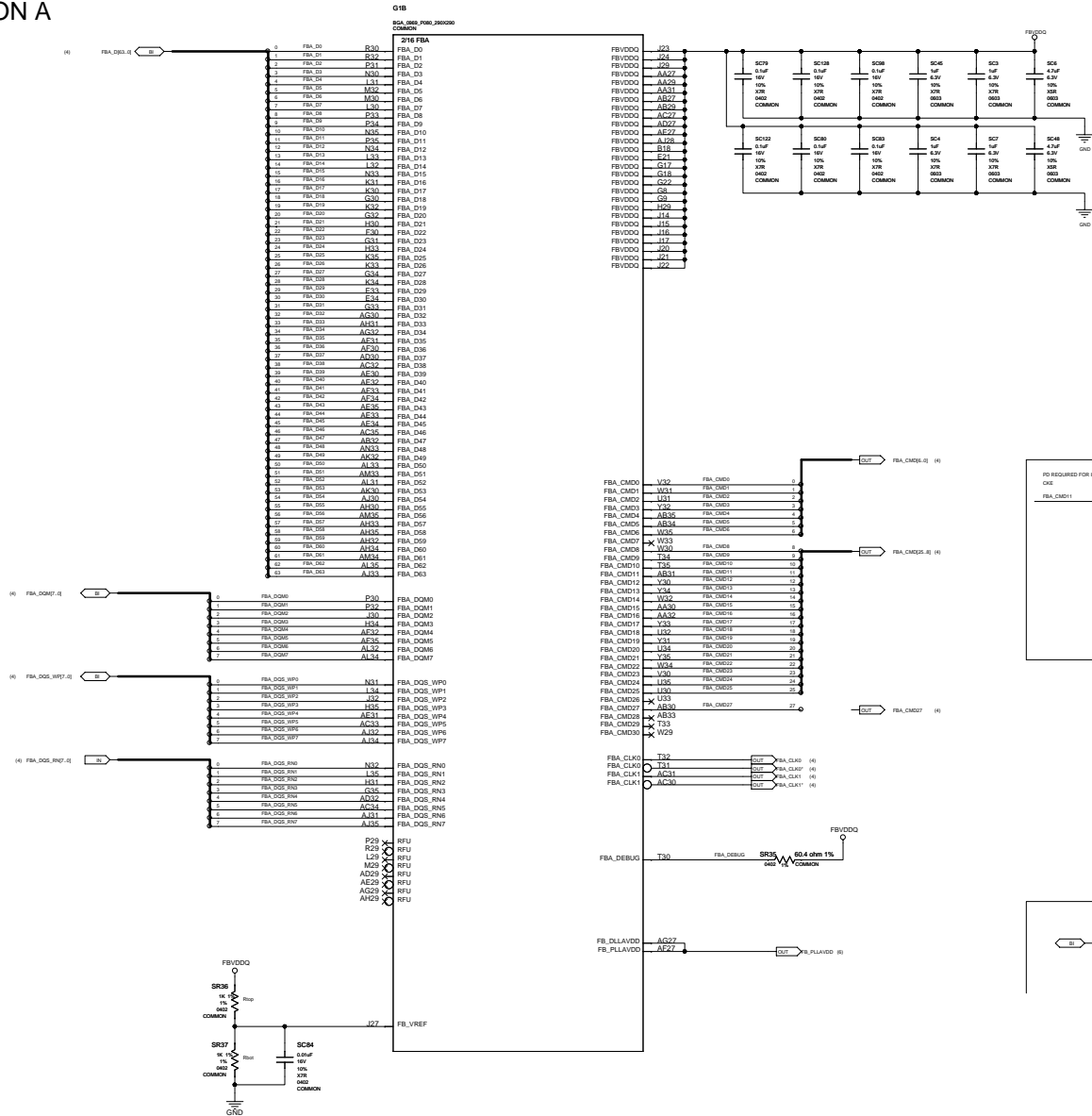
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REVISION HISTORY			
Sch Rev	PCB Rev	DATE	REVISION DESCRIPTION
1.0	1.0	2008-04-16	Base NV P616-A03 design. Change GDDR3 to DDR2
1.0	1.0	2008-05-07	Model name change to P601 V1.0
1.1	1.1	2008-05-26	Add D3, D4, D7, SD2, SD4 ESD diodes for I2C bus.
1.2	1.2	2008-06-02	Modify PCB layout. Down impedance of NVVDD plane

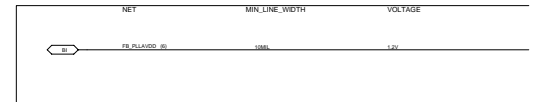
PCI EXPRESS



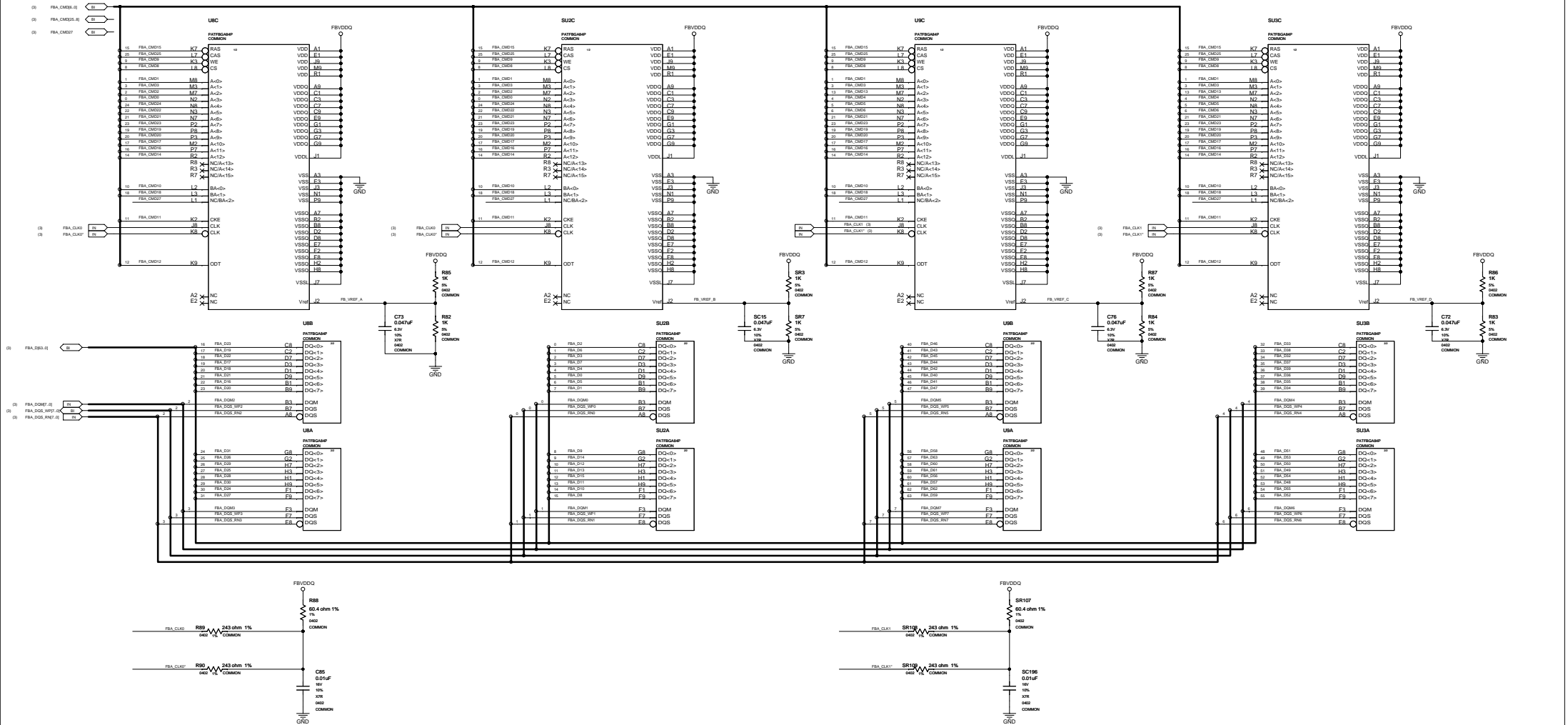
GPU MEMORY INTERFACE: PARTITION A



CMD-Addr Map			
BSGAR +31..26	BSGAR +25..20	ADDR	
CMD01	CMD1	Addr0	
CMD02	CMD3	Addr1	
CMD03	CMD4	Addr2	
CMD04	CMD5	Addr3	
CMD05	CMD6	Addr4	
CMD06	CMD7	Addr5	
CMD07	CMD8	Addr6	
CMD08	CMD9	Addr7	
CMD09	CMD10	Addr8	
CMD10	CMD11	Addr9	
CMD11	CMD12	Addr10	
CMD12	CMD13	Addr11	
CMD13	CMD14	Addr12	
CMD14	CMD15	Addr13	
CMD15	CMD16	Addr14	
CMD16	CMD17	Addr15	
CMD17	CMD18	Addr16	
CMD18	CMD19	Addr17	
CMD19	CMD20	Addr18	
CMD20	CMD21	Addr19	
CMD21	CMD22	Addr20	
CMD22	CMD23	Addr21	
CMD23	CMD24	Addr22	
CMD24	CMD25	Addr23	
CMD25	CMD26	Addr24	
CMD26	CMD27	Addr25	
CMD27	CMD28	Addr26	
CMD28	CMD29	Addr27	
CMD29	CMD30	Addr28	
CMD30	CMD31	Addr29	
CMD31	CMD32	Addr30	
CMD32	CMD33	Addr31	
CMD33	CMD34	Addr32	
CMD34	CMD35	Addr33	
CMD35	CMD36	Addr34	
CMD36	CMD37	Addr35	
CMD37	CMD38	Addr36	
CMD38	CMD39	Addr37	
CMD39	CMD40	Addr38	
CMD40	CMD41	Addr39	
CMD41	CMD42	Addr40	
CMD42	CMD43	Addr41	
CMD43	CMD44	Addr42	
CMD44	CMD45	Addr43	
CMD45	CMD46	Addr44	
CMD46	CMD47	Addr45	
CMD47	CMD48	Addr46	
CMD48	CMD49	Addr47	
CMD49	CMD50	Addr48	
CMD50	CMD51	Addr49	
CMD51	CMD52	Addr50	
CMD52	CMD53	Addr51	
CMD53	CMD54	Addr52	
CMD54	CMD55	Addr53	
CMD55	CMD56	Addr54	
CMD56	CMD57	Addr55	
CMD57	CMD58	Addr56	
CMD58	CMD59	Addr57	
CMD59	CMD60	Addr58	
CMD60	CMD61	Addr59	
CMD61	CMD62	Addr60	
CMD62	CMD63	Addr61	
CMD63	CMD64	Addr62	
CMD64	CMD65	Addr63	
CMD65	CMD66	Addr64	
CMD66	CMD67	Addr65	
CMD67	CMD68	Addr66	
CMD68	CMD69	Addr67	
CMD69	CMD70	Addr68	
CMD70	CMD71	Addr69	
CMD71	CMD72	Addr70	
CMD72	CMD73	Addr71	
CMD73	CMD74	Addr72	
CMD74	CMD75	Addr73	
CMD75	CMD76	Addr74	
CMD76	CMD77	Addr75	
CMD77	CMD78	Addr76	
CMD78	CMD79	Addr77	
CMD79	CMD80	Addr78	
CMD80	CMD81	Addr79	
CMD81	CMD82	Addr80	
CMD82	CMD83	Addr81	
CMD83	CMD84	Addr82	
CMD84	CMD85	Addr83	
CMD85	CMD86	Addr84	
CMD86	CMD87	Addr85	
CMD87	CMD88	Addr86	
CMD88	CMD89	Addr87	
CMD89	CMD90	Addr88	
CMD90	CMD91	Addr89	
CMD91	CMD92	Addr90	
CMD92	CMD93	Addr91	
CMD93	CMD94	Addr92	
CMD94	CMD95	Addr93	
CMD95	CMD96	Addr94	
CMD96	CMD97	Addr95	
CMD97	CMD98	Addr96	
CMD98	CMD99	Addr97	
CMD99	CMD100	Addr98	
CMD100	CMD101	Addr99	
CMD101	CMD102	Addr100	
CMD102	CMD103	Addr101	
CMD103	CMD104	Addr102	

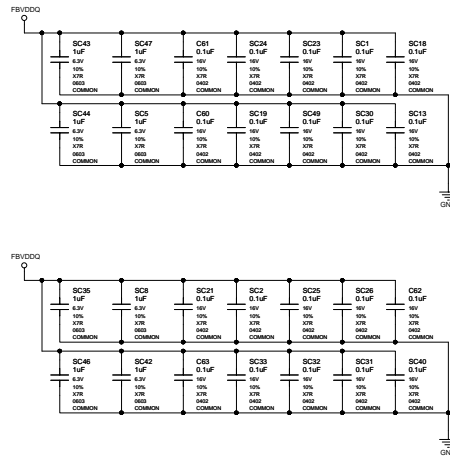


Partition A Memories



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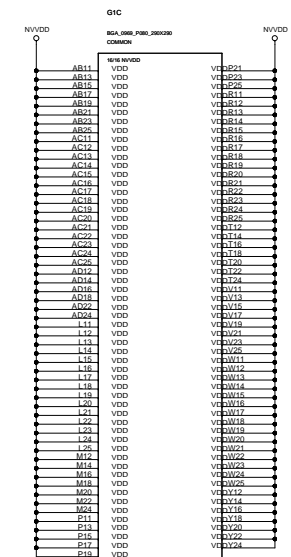
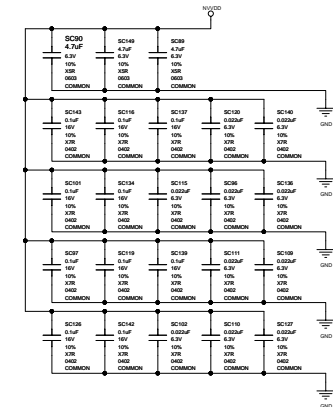
FRAME BUFFER: PARTITION A DECOUPLING



Decoupling for
FBA North Side
Memory Device.

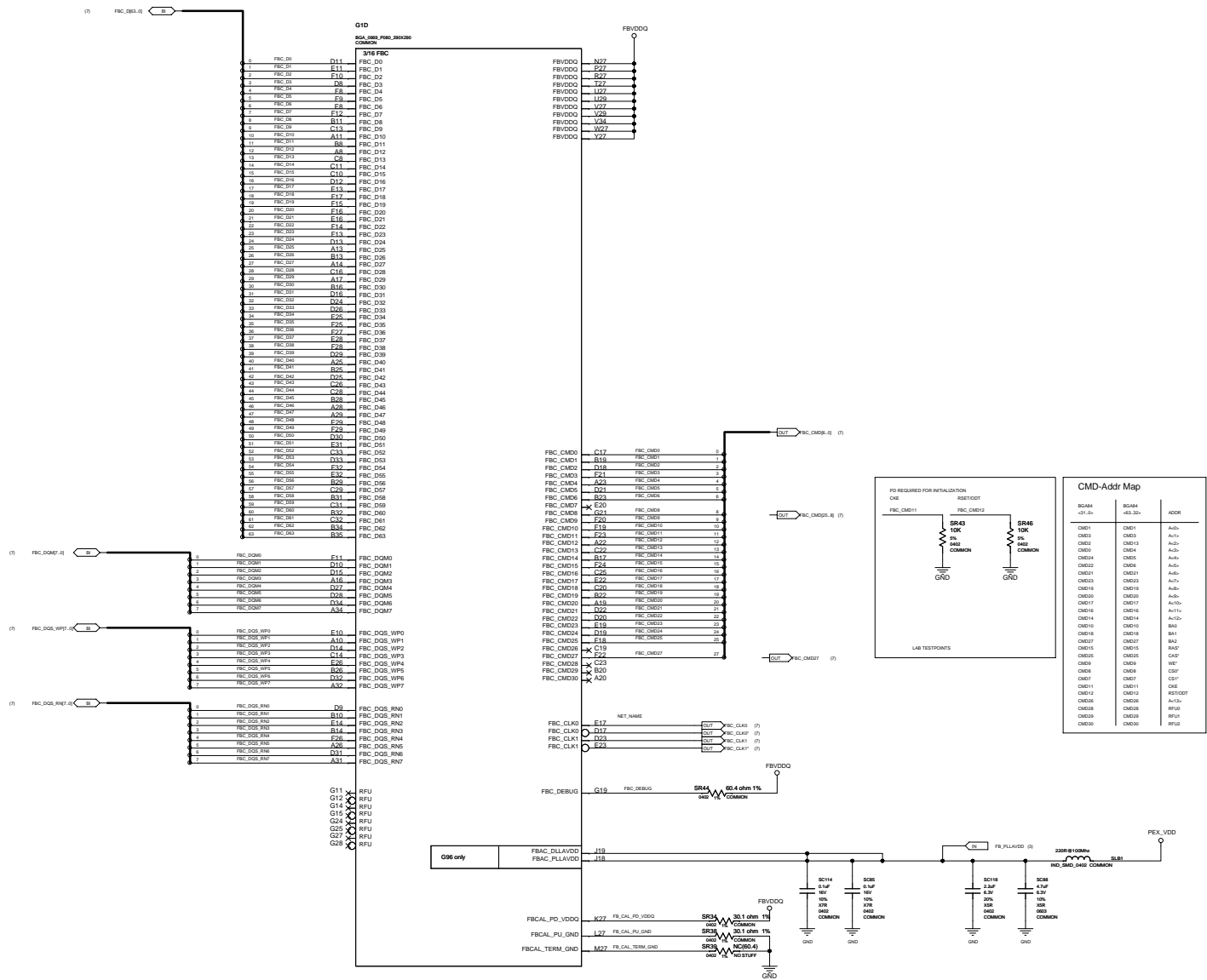
Decoupling for
FBA South Side
Memory Device.

NVVDD POWER AND DECOUPLING

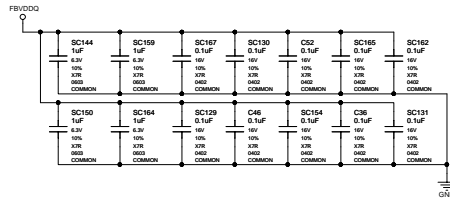


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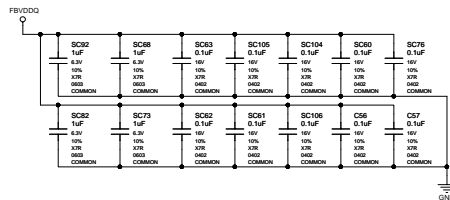
GPU MEMORY INTERFACE: PARTITION C



FRAMEBUFFER: PARTITION C DECOUPLING

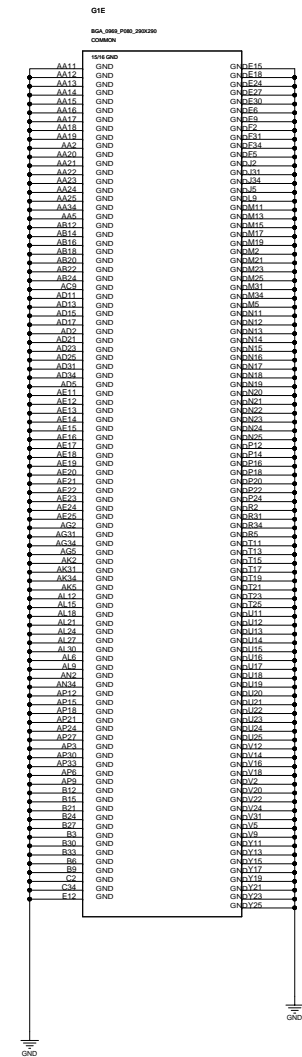


Decoupling for
FBC West Side
Memory Device.



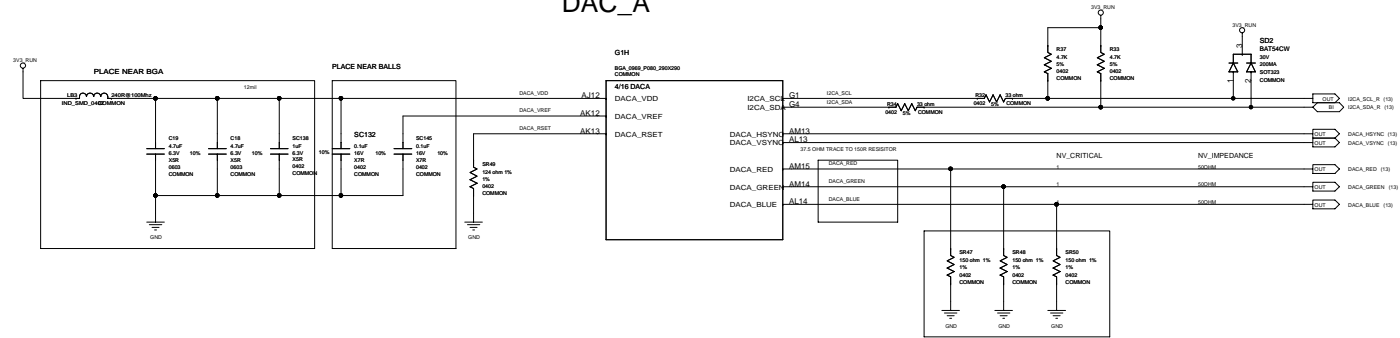
Decoupling for
FBC East Side
Memory Device.

NVVDD GROUND

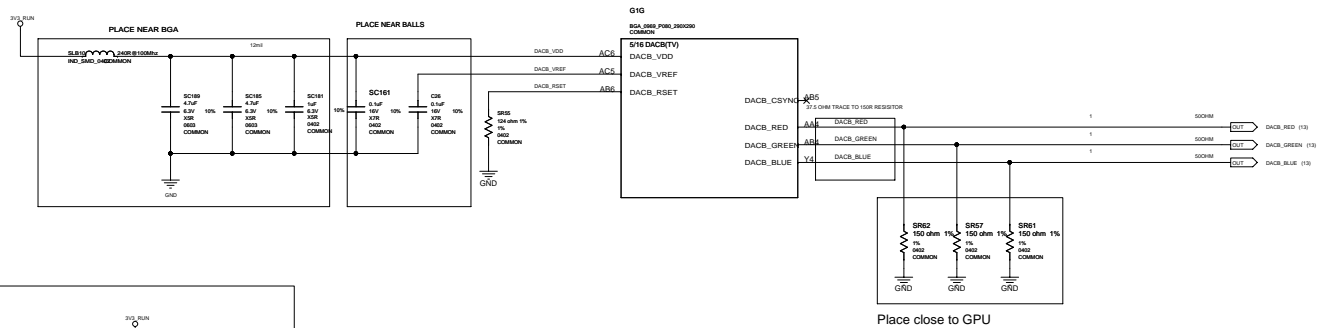


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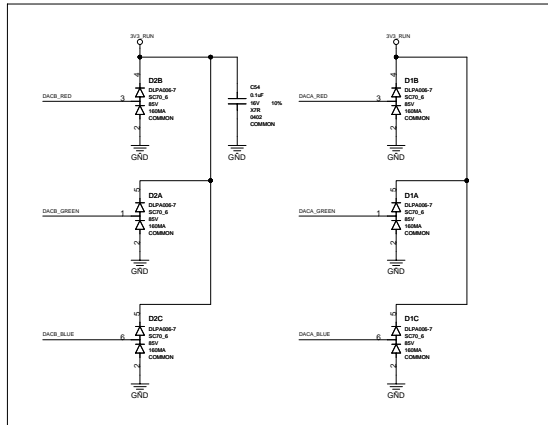
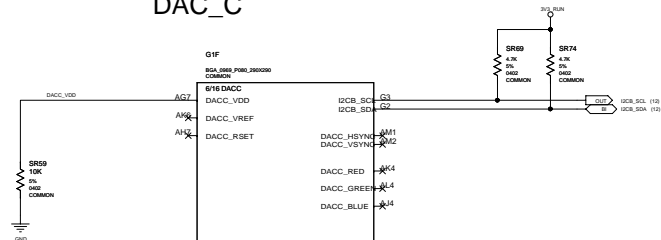
DAC_A



DAC_B



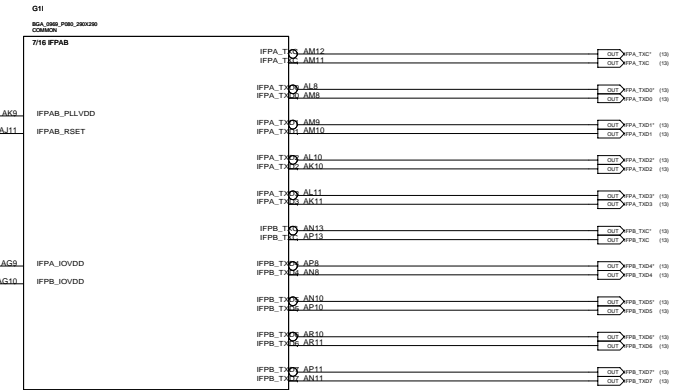
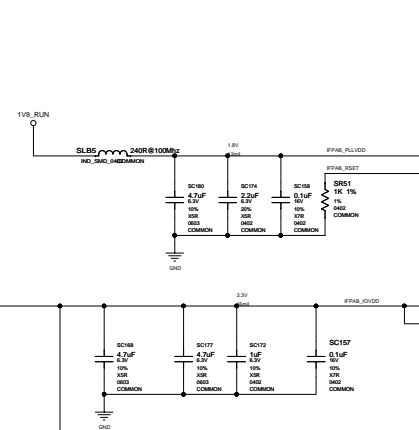
DAC_C



TV DAC ESD PROTECTION

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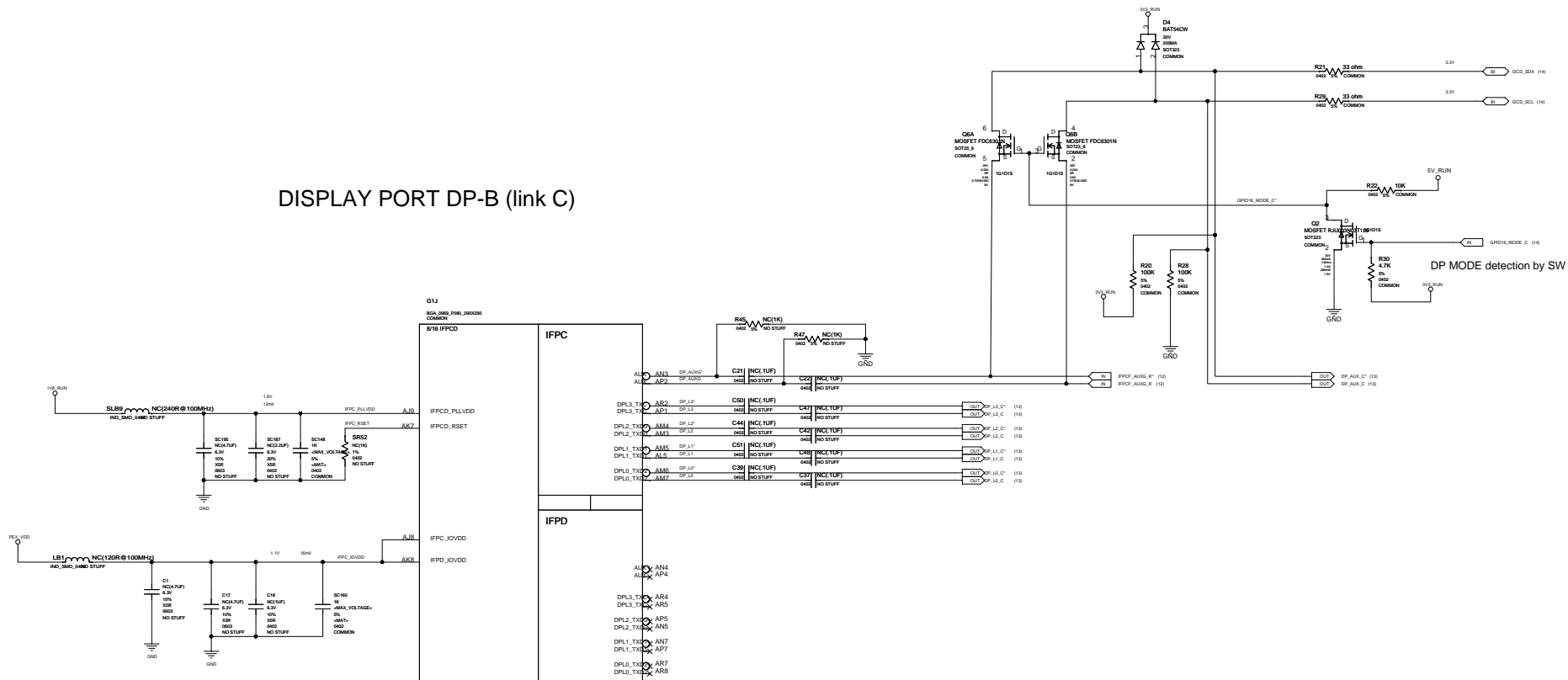
Option #1) IFPAB outputs to LVDS only.
Option #2) IFPAB outputs to DVI-C only.
Option #3) Controlled with GPIO9, IFPAB dynamically outputs to LVDS or DVI-C.



G96-630-A

[illegible][illegible]

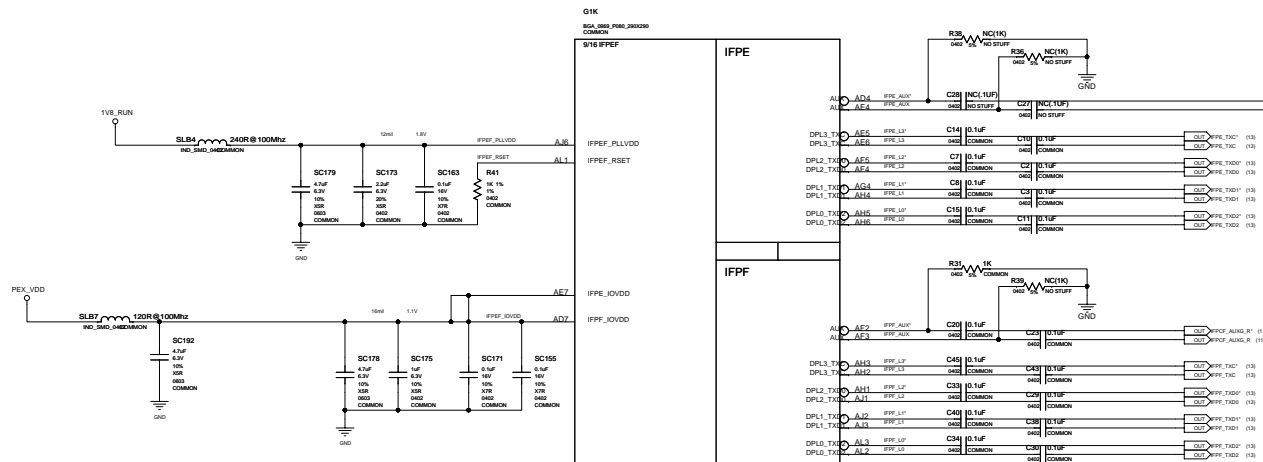
DISPLAY PORT DP-B (link C)



(DP CONSTRAINTS)

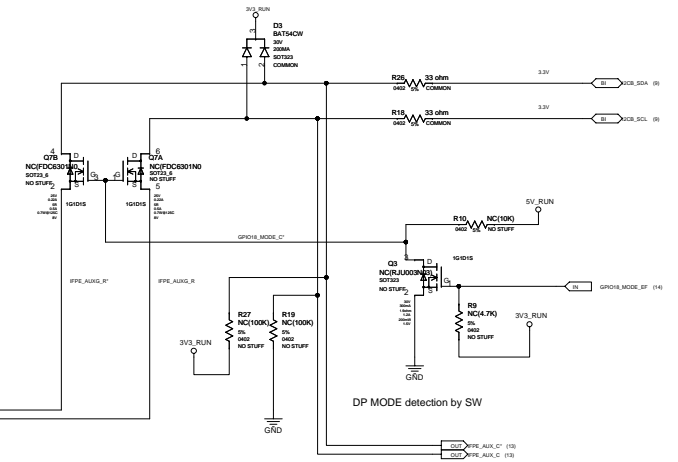
NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
(1) DP_AUX_C	DP_AUX	1	1000EF
(2) DP_AUX_C	DP_AUX	1	1000EF
(3) DP_I3_C	DP_I3	1	1000EF
(4) DP_I3_C	DP_I3	1	1000EF
(5) DP_I3_C	DP_I3	1	1000EF
(6) DP_I3_C	DP_I3	1	1000EF
(7) DP_I3_C	DP_I3	1	1000EF
(8) DP_I3_C	DP_I3	1	1000EF
(9) DP_I3_C	DP_I3	1	1000EF
(10) DP_I3_C	DP_I3	1	1000EF

DVI-A HDMI (LINK E)
OPTIONAL DP-C FOR OEM SPECIAL SKU

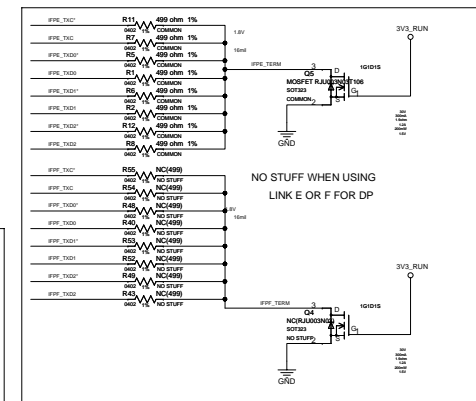


DISPLAY PORT DP-A (LINK F)
OPTIONAL DVI-B TMDS SL OR DL W/ DVI-A

(TMDS/HDMI/DP OPTION CONSTRAINTS)

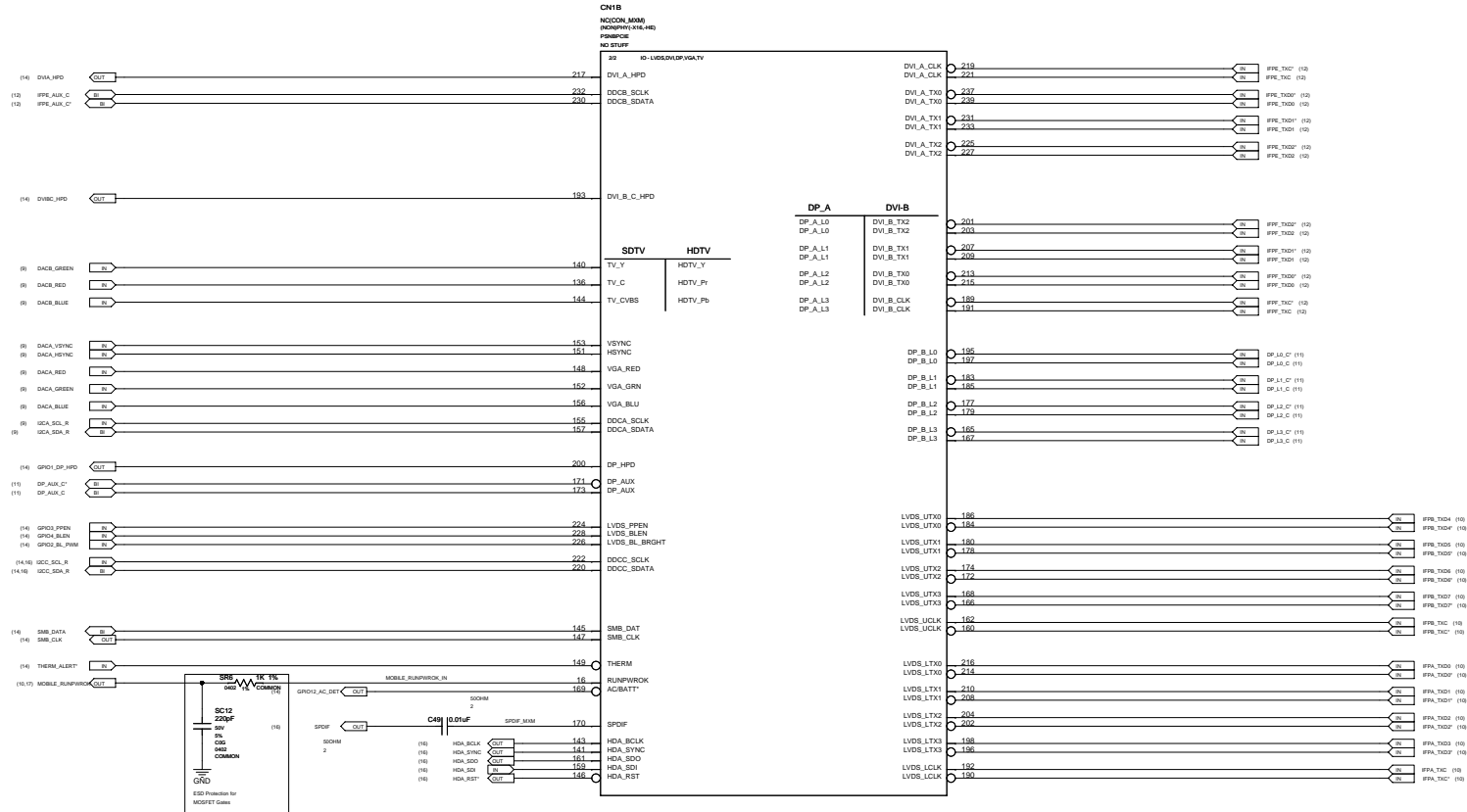
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LinkE/F BIAS

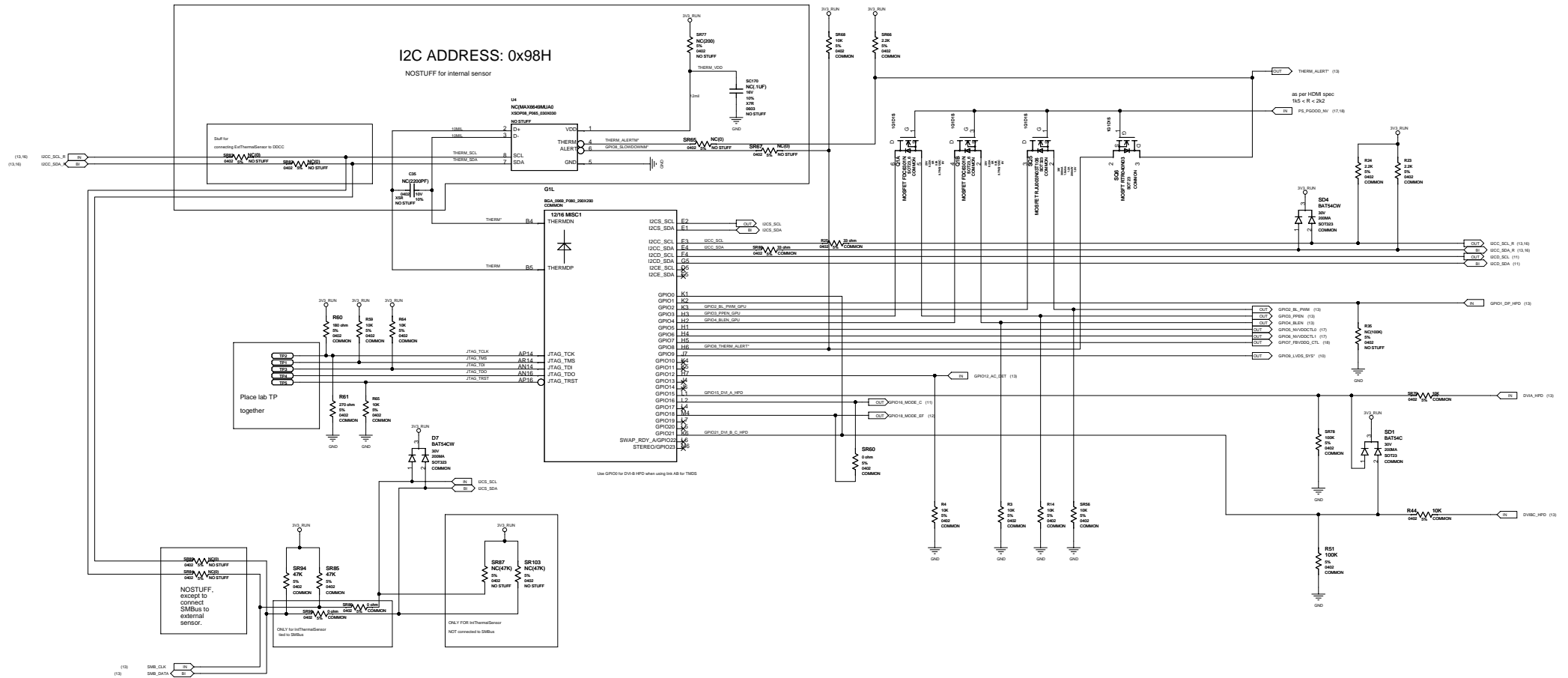


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MXM CONNECTOR

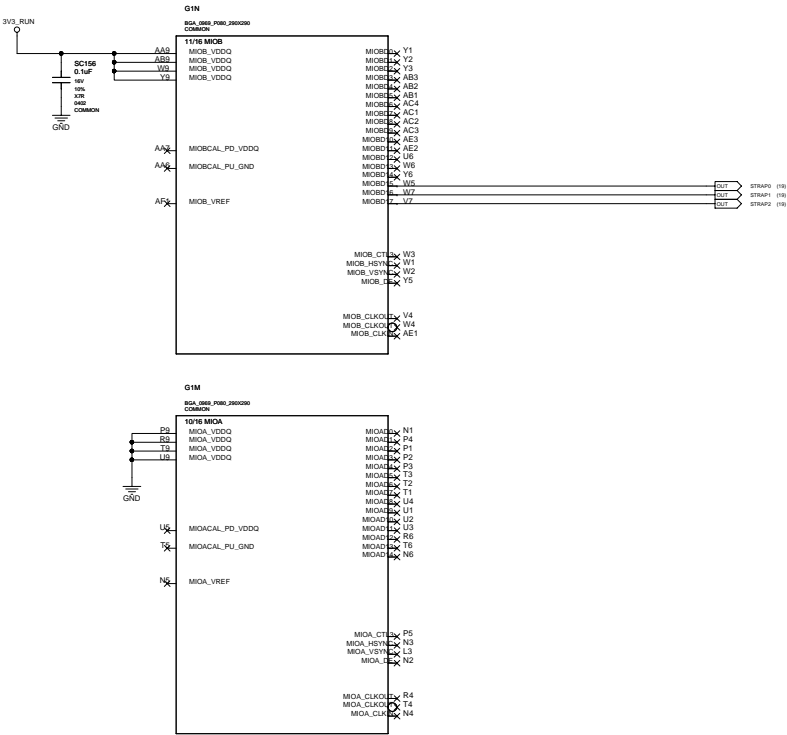


GPIO, TEMP SENSOR, JTAG



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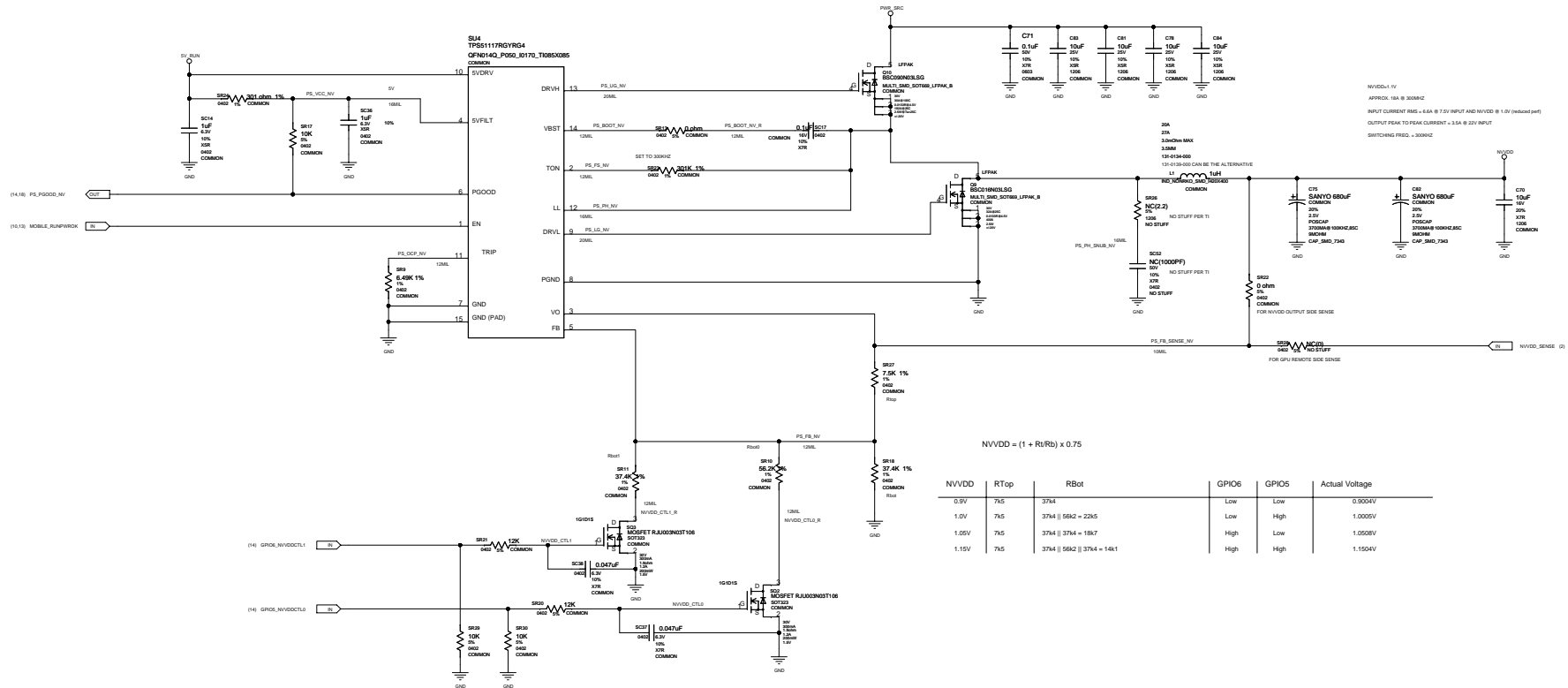
MIOA/B



NVVDD POWER SUPPLY

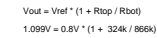


NVVDD SWITCHER POWER SUPPLY



NVVDD	RTop	RBot	GPI06	GPI05	Actual Voltage
0.9V	7K5	37k4	Low	Low	0.9004V
1.0V	7K5	37k4 56k2 = 22K5	Low	High	1.0005V
1.05V	7K5	37k4 37k4 = 18k7	High	Low	1.0508V
1.15V	7K5	37k4 56k2 37k4 = 14k1	High	High	1.1504V

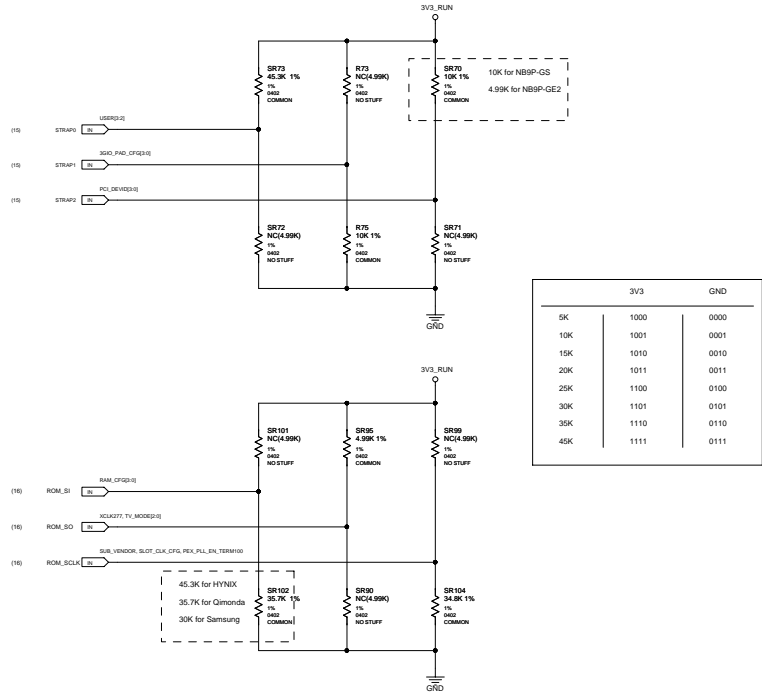
FBVDDQ SWITCHER


$$FBVDDQ = (1 + R_t/R_b) \times 0.80$$

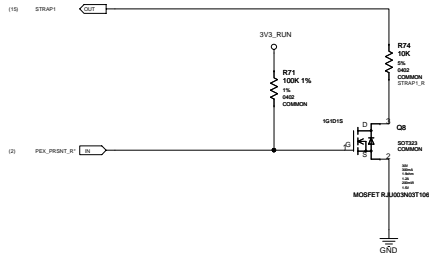
FBVDDQ	R _{Top}	R _{Bot}	GPIO7	Actual Voltage
1.55V	49KΩ	53KΩ	Low	1.5448V
1.8V	49KΩ	53KΩ 156K	High	1.7975V

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STRAPPING OPTIONS



PEX SWING LEVEL



PEX_PRST2_R	R_STRAP1	3_GIO_PADCFG_LUT<3.0>
GND	10k	0x1 MOBILE_DEFAULT
FLOAT	5k (10k 10k)	0x0 DESKTOP_DEFAULT

STRAP0

USER_BIT0 0xF: 45K PU (unused)
USER_BIT1
USER_BIT2
USER_BIT3

STRAP1

3GIO_PADCFG_LUT_ADR0
3GIO_PADCFG_LUT_ADR1 0x0: Desktop default (normal swing) - 5k PD
3GIO_PADCFG_LUT_ADR2 0x1: Mobile default (low swing) - 10k PD
3GIO_PADCFG_LUT_ADR3 acc. to /hw/tesla_g98b/manuals/dev_ext_devices.ref

STRAP2

PCI_DEVID_0 all 4 bits set by HW strapping
PCI_DEVID_1 0x0649: 10K PU (NB9P-GS)
PCI_DEVID_2 0x0648: 5K PU (NB9P-GE2)
PCI_DEVID_3 0x065C: 25K PU (NB9P-GLM2)

ROM_SO

TV_MODE_BIT0 0x0: NTSC-M
TV_MODE_BIT1 5K PU
TV_MODE_BIT2
XCLK_277 1: PCI-E GEN2

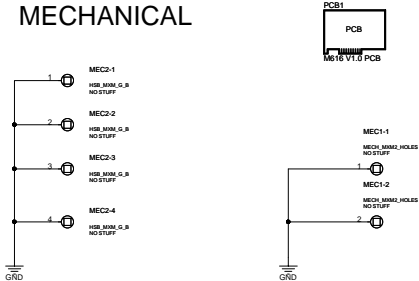
ROM_SI

RAM_CFG_0 256 MB (4pcs. 16Mx32) 512 MB (4pcs. 32Mx32)
RAM_CFG_1 RAM_CFG[3:0] Definitions RAM_CFG[3:0] Definitions
RAM_CFG_2 0000 Reserved 0100 25k PD Reserved
0001 Qimonda 0101 30k PD Qimonda
0010 Hynix 0110 35k PD Hynix
0011 Samsung 0111 45k PD Samsung
RAM_CFG_3

ROM_SCLK

PEX_PLL_EN_TERM100 0:
SLOT_CLK_CONFIG 1: GPU/MCH SHARE COM REF CLK 35K PD
SUB_VENDOR 1: SUB_VENDOR BIOS
PCI_DEVID_EXT 0: TERM100 DISABLED

MECHANICAL



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