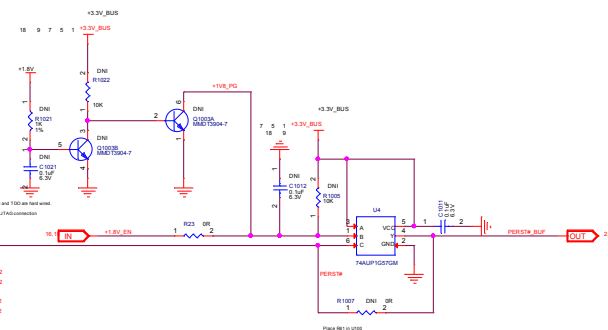
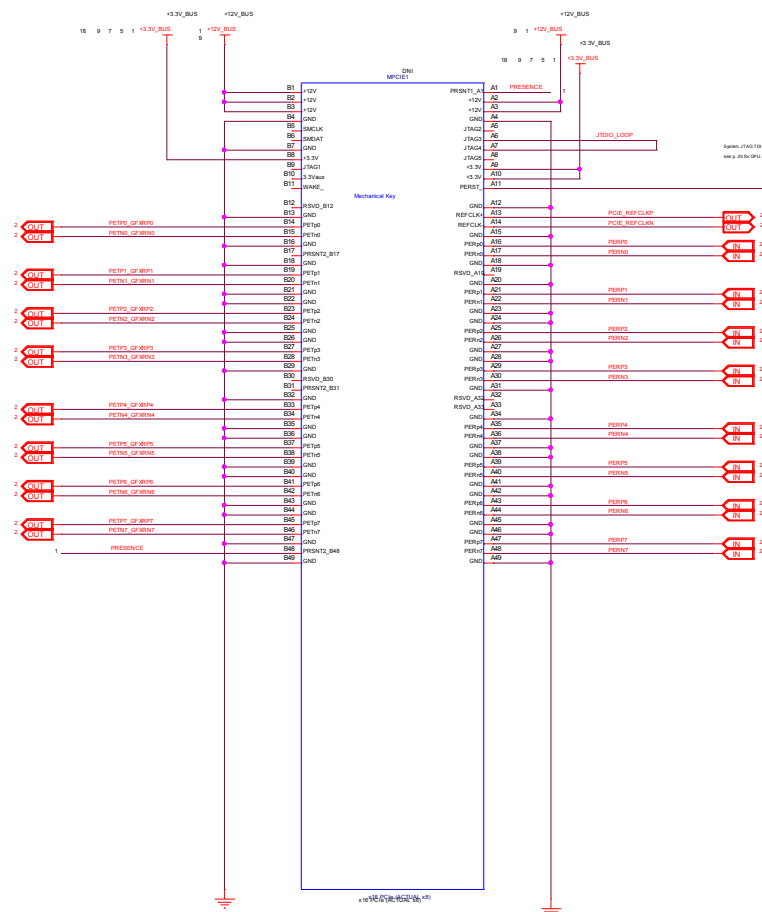
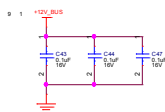
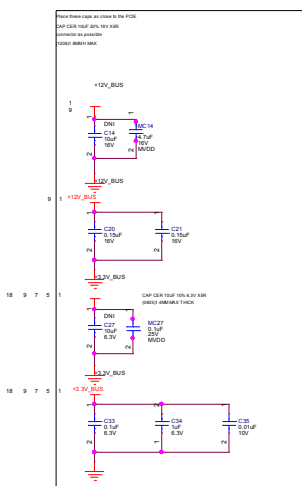
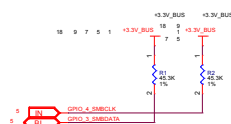




## PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BOD	BOND UP ONLY

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#46, No.1387, ZHANGDONG ROAD  
SHANGHAI, CHINA 201203

SHEET: PCIe Edge Connector

DATE: Wed Aug 29 03:27:33 2018

REV: P00

SHEET NUMBER: 1 OF 20

DOCUMENT NUMBER: 105\_d12900\_00A

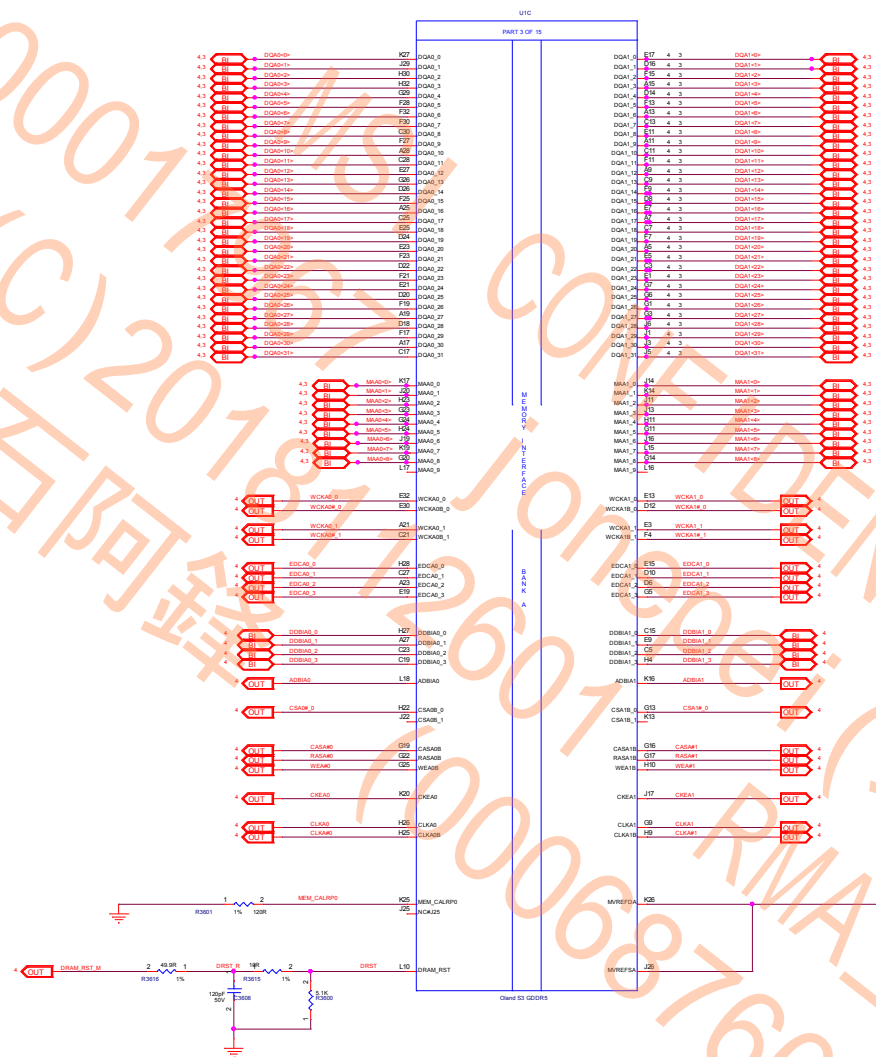
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
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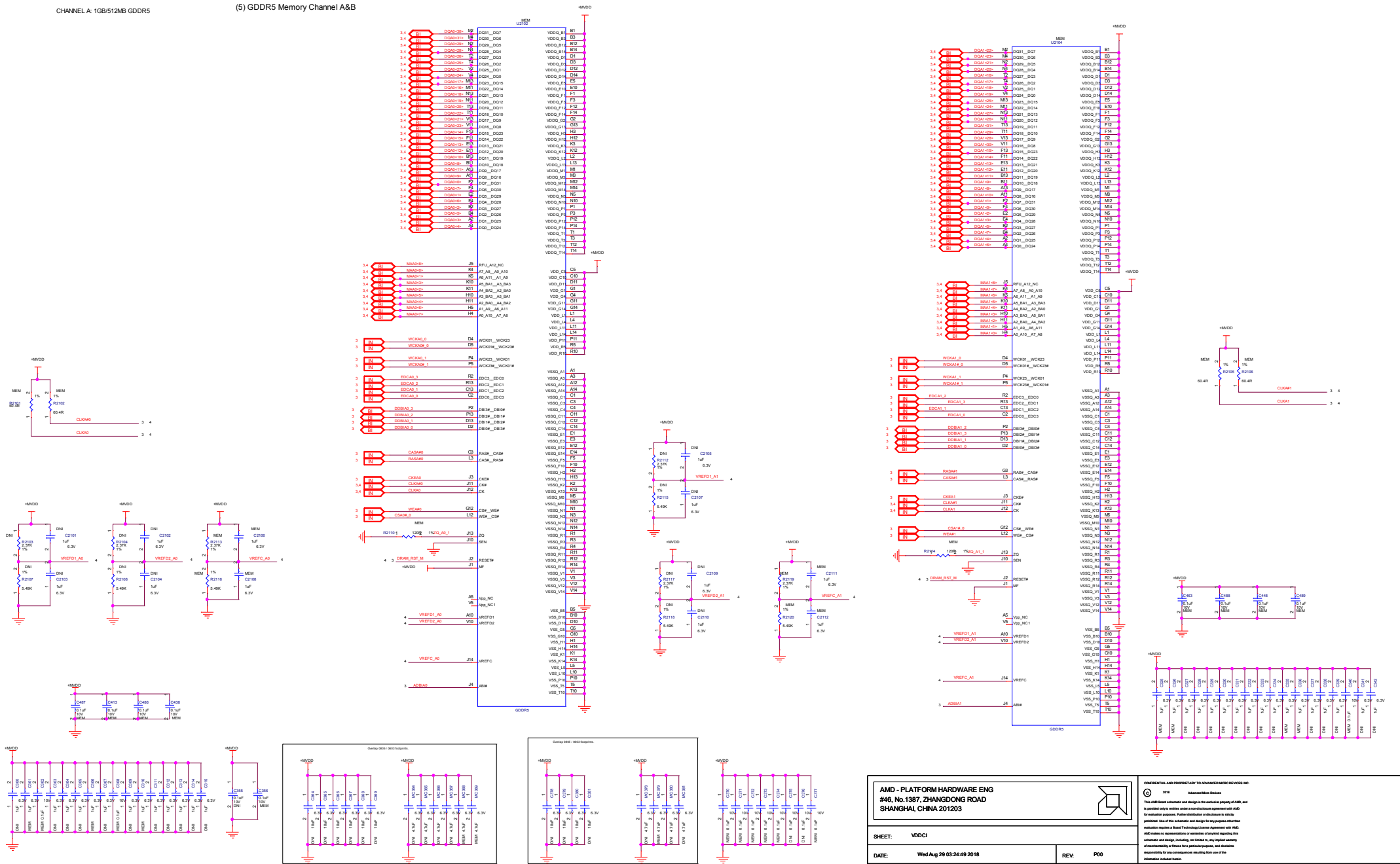
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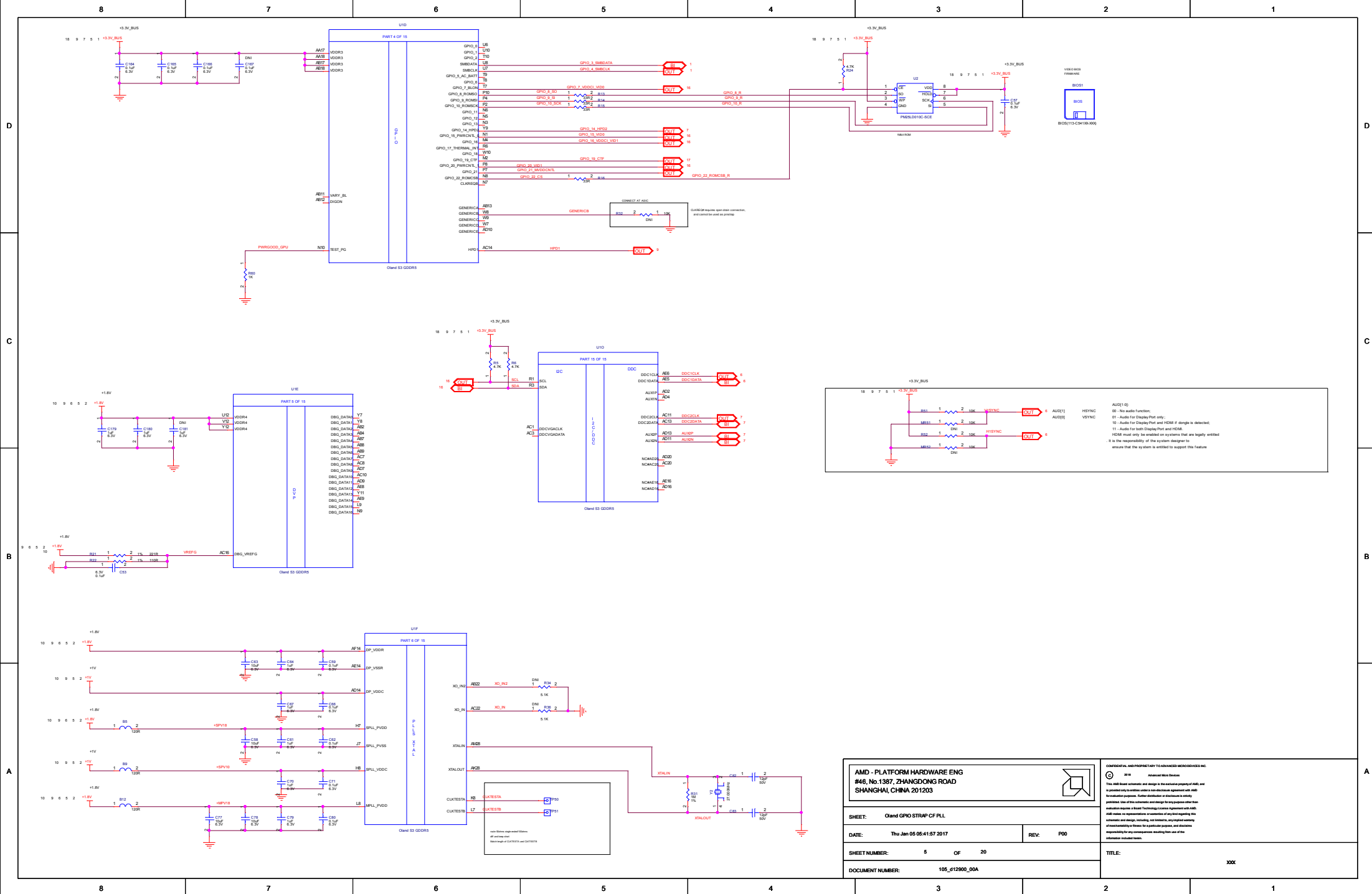
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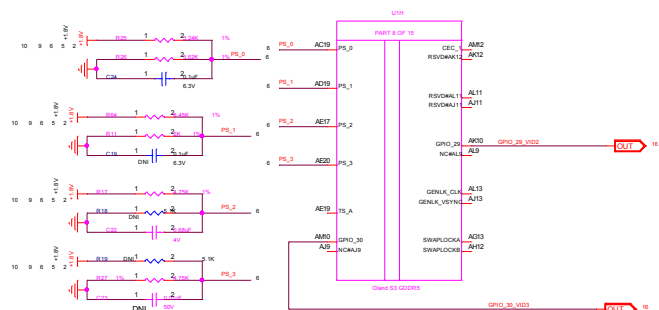
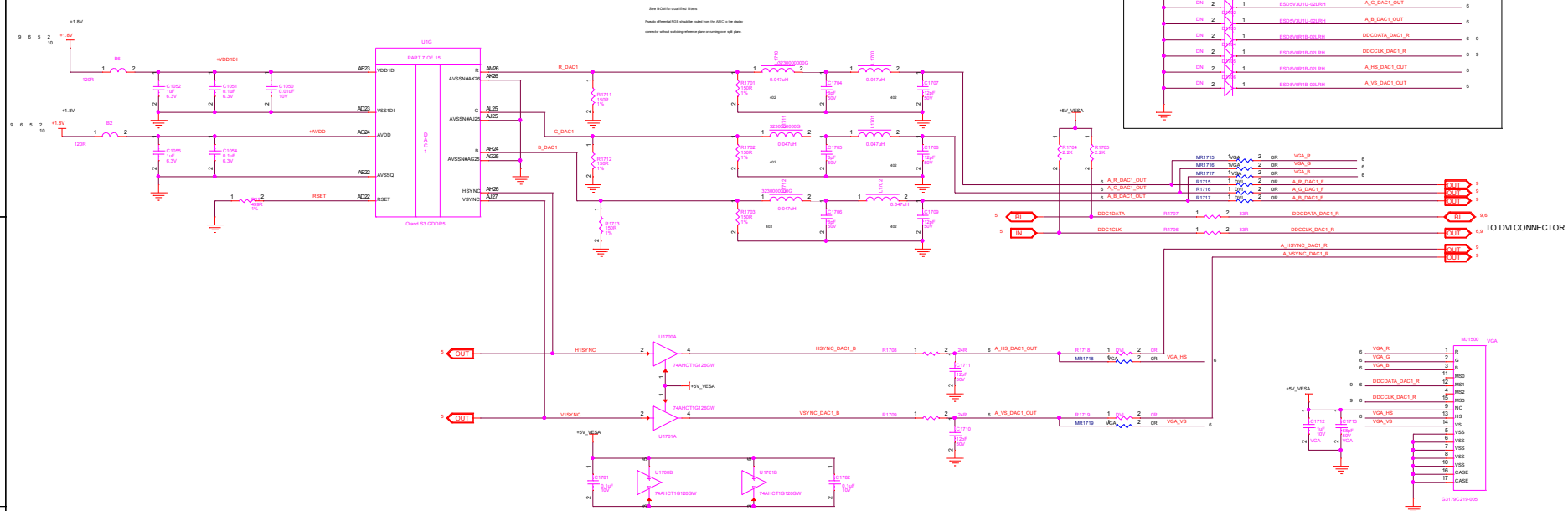



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SHEET: VDDCI		REV: P00			
DATE: Wed Aug 29 03:24:49 2018					
SHEET NUMBER: 3 OF 20				TITLE: XXX	
DOCUMENT NUMBER: 105_012900_00A					
NOTES: NOTE					



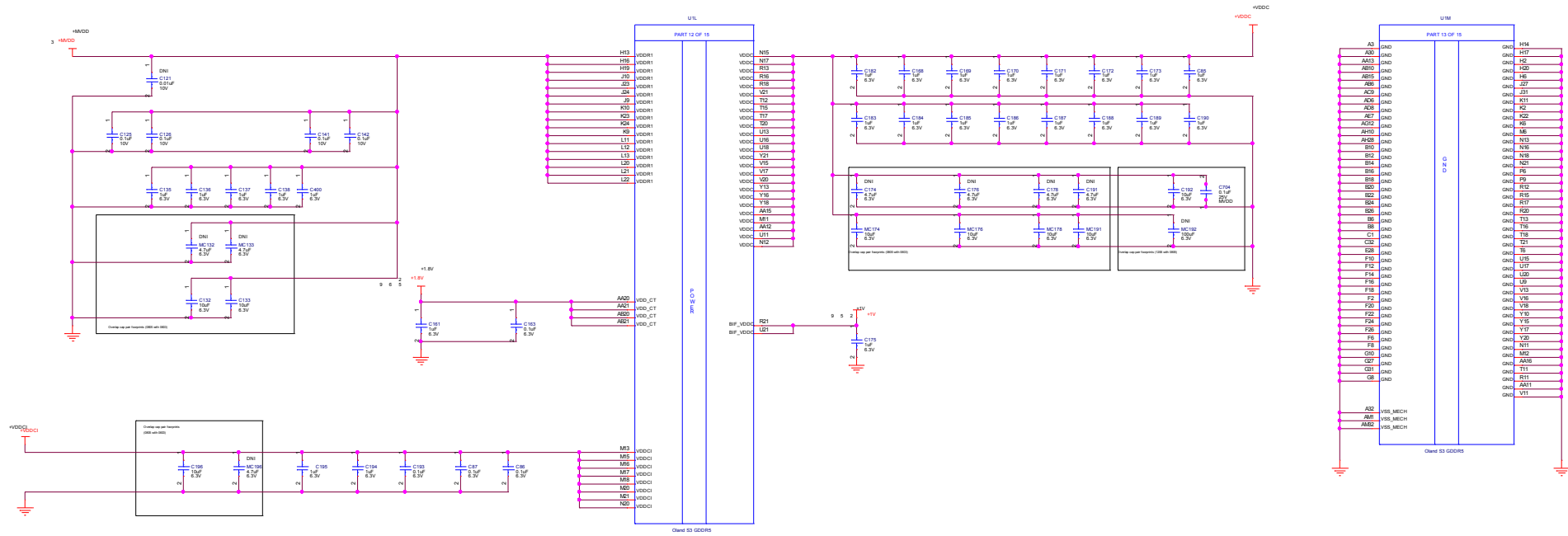



## Oland DAC1

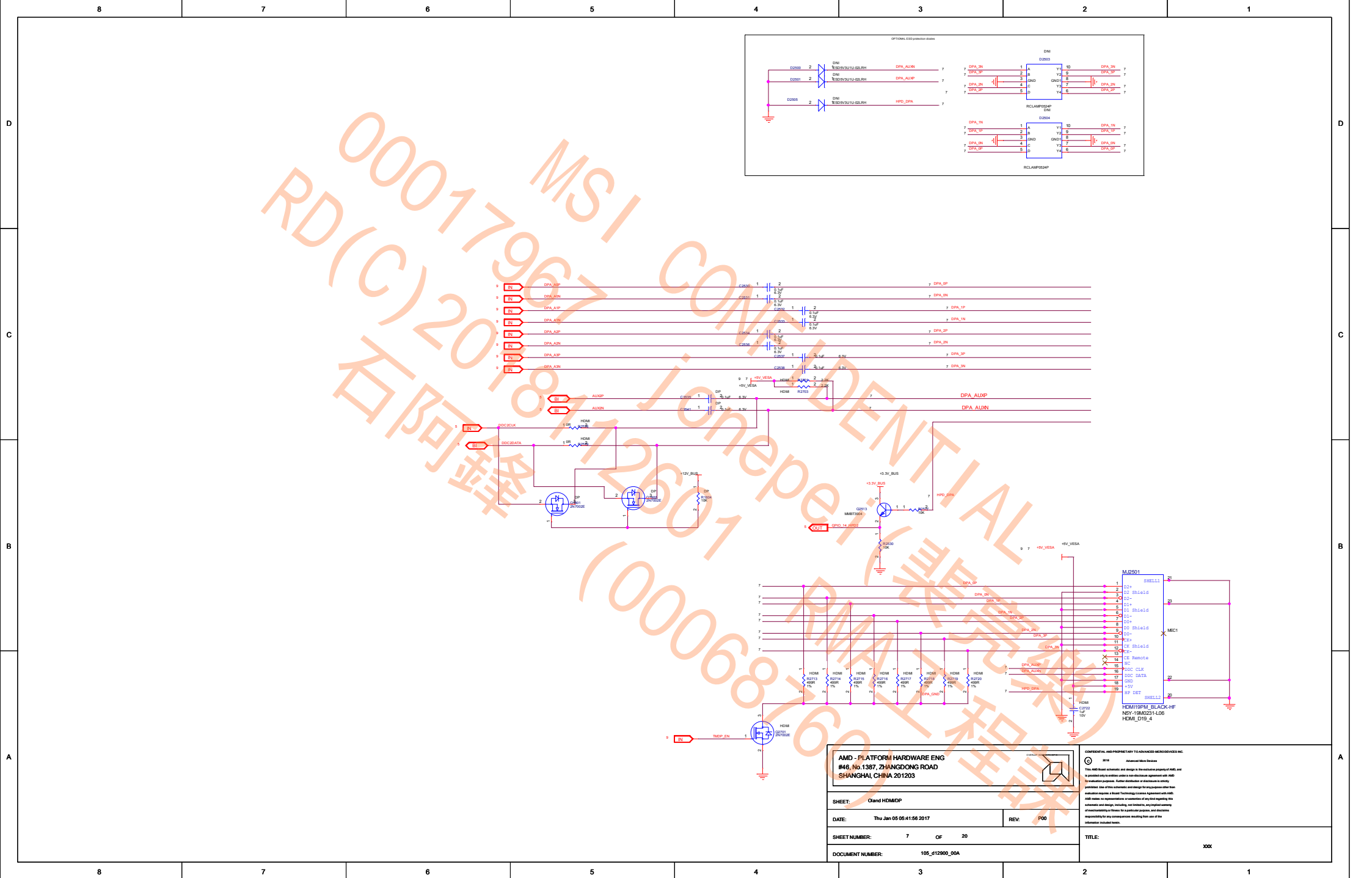


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<p>SHEET:      Grand DAC</p> <p>DATE:         Thu Jan 05 09:41:56 2017</p>	<p>REV:          P00</p>
<p>SHEET NUMBER:           6           OF           20</p>	<p>TITLE:</p>
<p>DOCUMENT NUMBER:       105_#12900_00A</p>	<p>XXX</p>

## OLAND S3 Power & GND

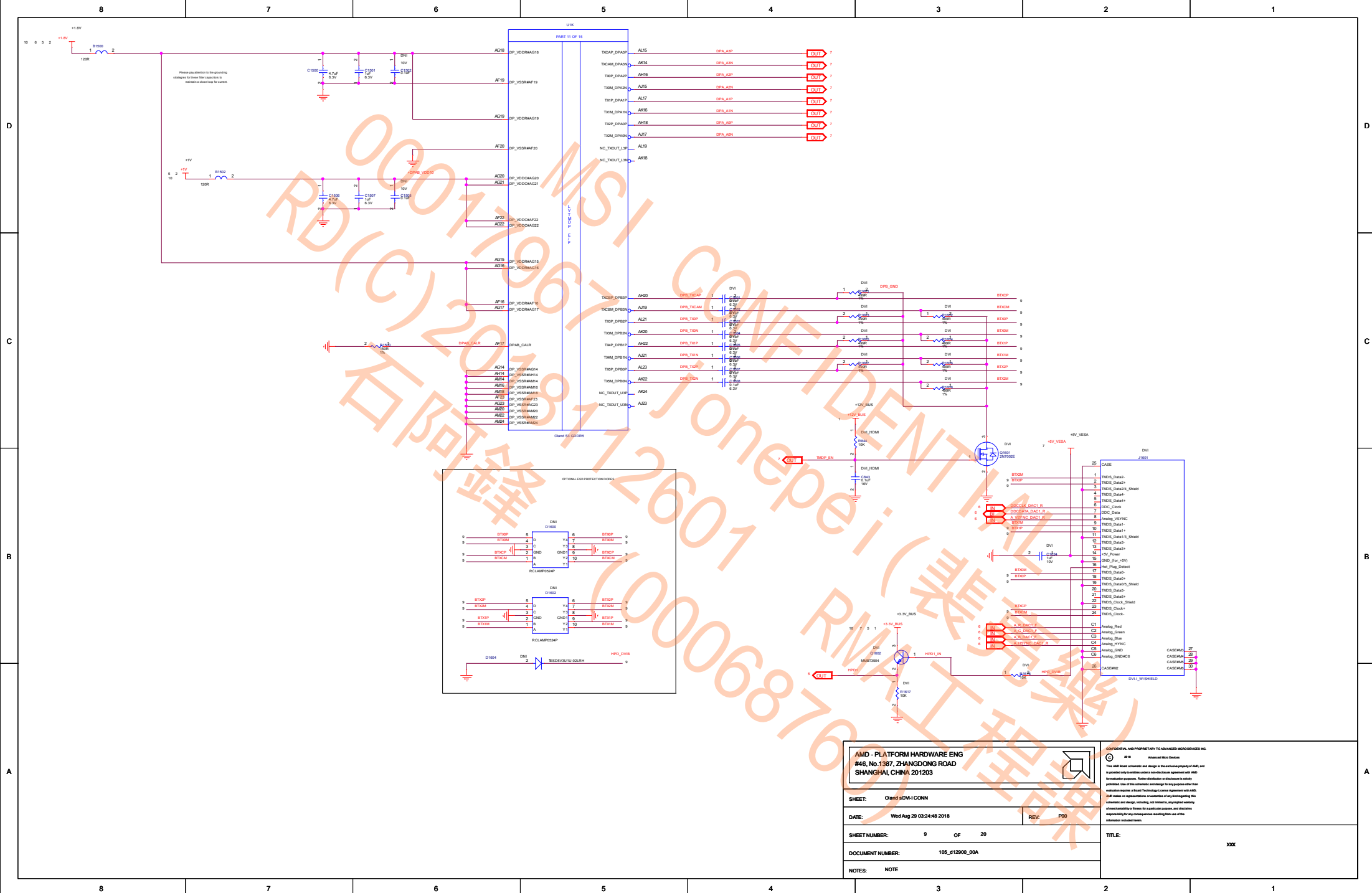


<b>AMD - PLATFORM HARDWARE ENG</b> <b>#46: NO.1387, ZHANGDONG ROAD</b> <b>SHANGHAI, CHINA 201203</b>			
<b>SHEET: VDDCI</b>		<b>DATE: 2018</b> <b>Added: Alex Boudet</b>	
<b>DATE: Wed Aug 29 03:24:49 2018</b>		<b>REV: P00</b>	
<b>SHEET NUMBER: 10 OF 20</b>		<b>TITLE:</b>	
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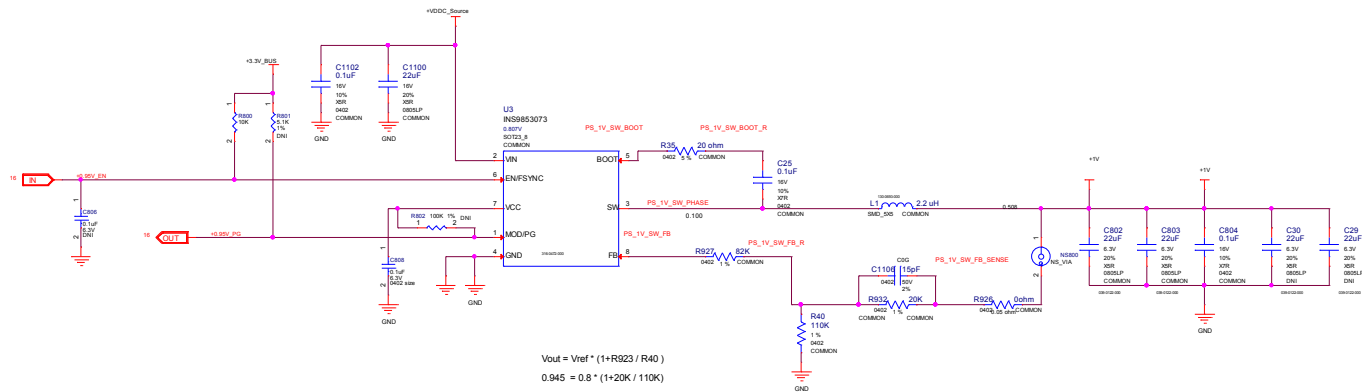





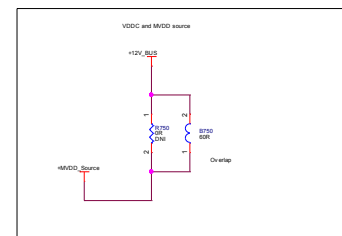


LDO #1:                      Vin = +1.5V +/-2%                      Vout = +0.95V +/-2%                      Iout = 1.44A (TYP)RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



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SHEET: VDDCI				
DATE: Wed Aug 29 03:24:49 2018	REV: P00			
SHEET NUMBER: 11 OF 20		TITLE:		
DOCUMENT NUMBER: 105_012900_00A		XXX		
NOTES: NOTE				



REV: P00

REV: P00

**TITLE:**

xxx

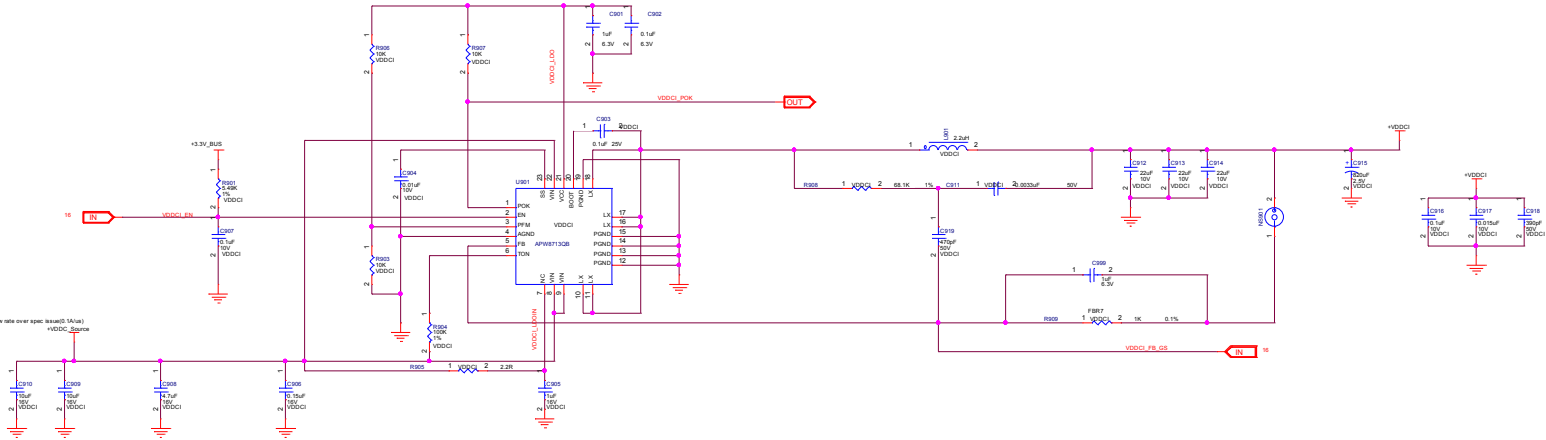
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Register for MVD

Use rVDDC\_Source to share L801 to eliminate PCIe 12V current slew rate over spec issue(0.1A/us)  
rVDDC\_Source



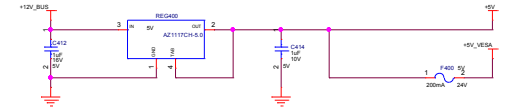
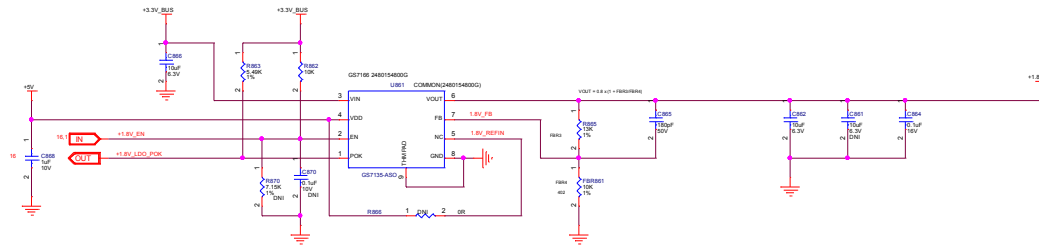
AMD - PLATFORM HARDWARE ENG #46, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: VDDC1	
DATE: Wed Aug 29 03:24:49 2018	REV: P00
SHEET NUMBER: 13 OF 20	
DOCUMENT NUMBER: 105_012900_00A	
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## Linear Regulators

LD0 #2: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TbV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling



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SHEET: Linear Regulators

DATE: Thu Jan 05 05:41:58 2017

REV: P00

SHEET NUMBER: 15 OF 20

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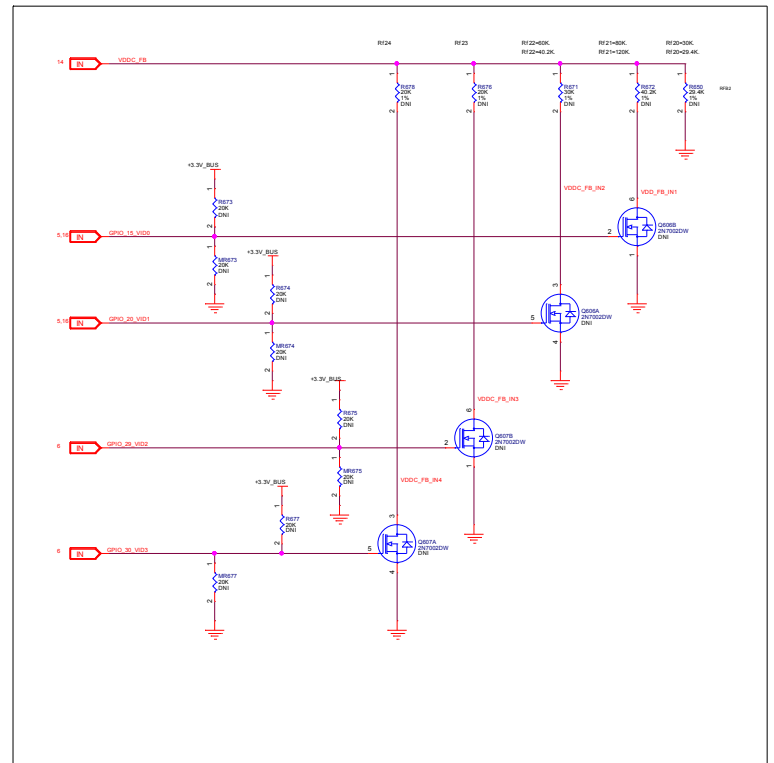
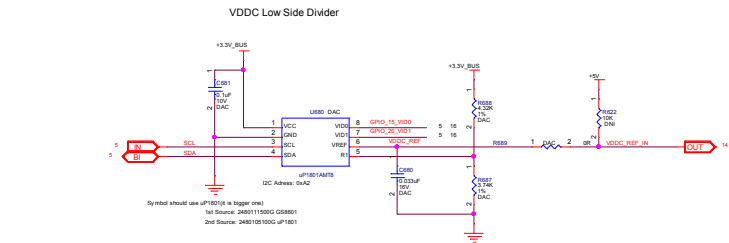
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xxx

POWER SEQUENCE  
+1.8V-2.8ms->AVDD-3.4ms->0.95V-4.3ms->VDDC  
0.95V must ramp up before VDDC

Don't support BACO
Support CTF(Internal)



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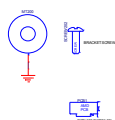
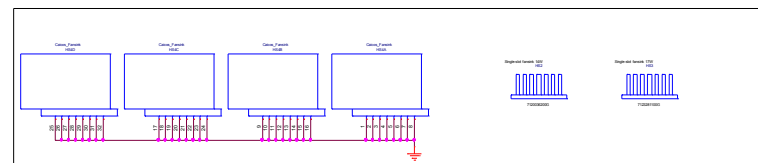
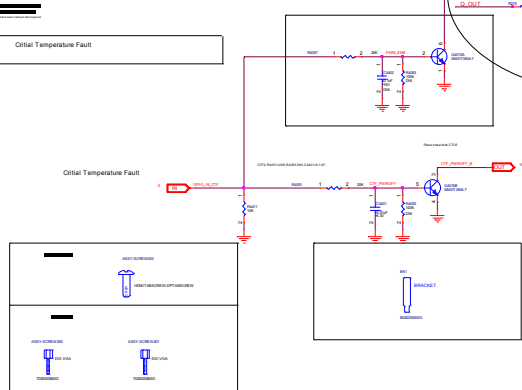
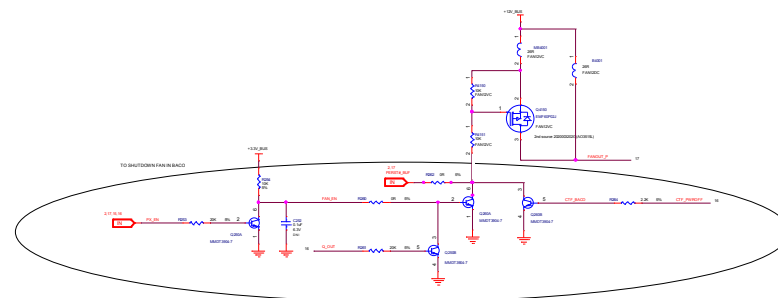
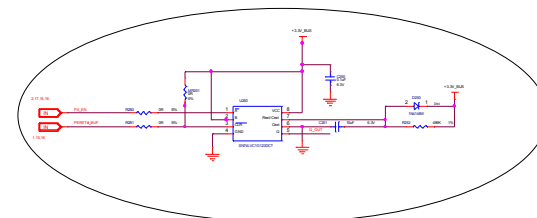
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DATE: Wed Aug 29 03:24:49 2018	REV: P00
SHEET NUMBER: 16 OF 20	
DOCUMENT NUMBER: 105_g12900_00A	
NOTES: NOTE	

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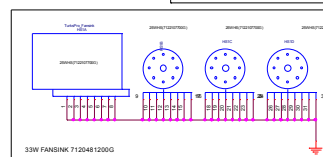
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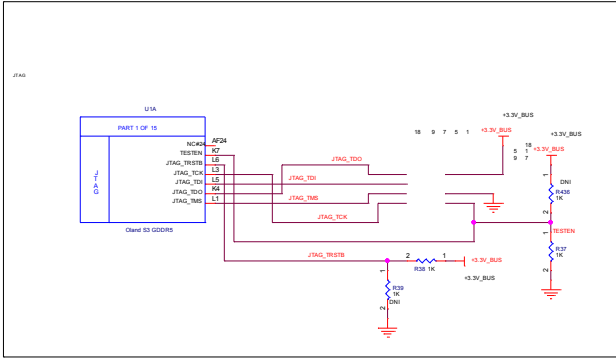
The schematic diagram shows a 24VDC power source connected to a relay. The relay has two outputs, FANOUT\_1 and FANOUT\_2, which are connected to a 12V source. A box labeled 'Fan Control' is connected to the relay.

[illegible]

Bracket, VGA, HDMI, DVI	802005200G
Bracket, VGA, DP (sbs), DVI	802005240G
Bracket, LP, DP (sbs), DVI	802005300G
Bracket, LP, HDMI, DVI	802005340G



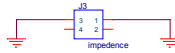
AMD - PLATFORM HARDWARE ENG #60, No.1367, ZHANGJIE ROAD SHANGHAI, CHINA 201203			
SHEET: VEDGO		004                             	
DATE: Wed Aug 30 22:48:2018	REV: 000	TITLE: XXX	
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DOCUMENT NUMBER: HW_P000_00A		TITLE: XXX	
NOTES: NONE		TITLE: XXX	



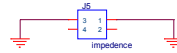
TOP  
Single end  
Memory data  
45 ohm +/- 5 ohm  
5.12 mils



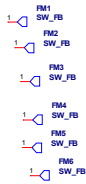
Bottom  
Single end  
Address trunk  
45 ohm +/- 5 ohm  
5.12 mils



TOP  
Different  
TMDS  
85 ohm +/- 10 %  
4.33 mils / 5.51 mils



Bottom  
Different  
PEX\_PCIE  
85 ohm +/- 10 %  
4.33 mils / 5.51 mils




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SHEET: Debug		REV: P00		TITLE:	
DATE: Thu Jan 05 05:41:58 2017				XXX	
SHEET NUMBER: 18 OF 20					
DOCUMENT NUMBER: 105_d12900_00A					



	8	7	6	5	4	3	2	1	
D			TITLE		SCHEMATIC NO.		DATE		
			Client ID: Q20RS 1GB HBM2P+4DVI-IVGA		105-012900-00A				
	REVISION HISTORY		NOTE: THIS DOCUMENT REPRESENTS THE NDA. IT DOES NOT REPRESENT ANY SPECIFIC DATA. FOR INTERNAL OFFICE USE ONLY. NO PARTS SHOULD BE REPRODUCED OR COPIED. PLEASE CONTACT THE REPRESENTATIVE TO OBTAIN THE NDA DOCUMENT TO THE APPLICATION BOARD.					REV	
								POD	
	SCH REV		PCB REV		DATE		REVISION DESCRIPTION		
10		001		2017-01-18		Initial Board/PCB schematic based on Q20RS 1GB			
C									
B									
A									

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SHEET: History

DATE: Thu Jan 05 05:41:18 2017

REV: P00

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DOCUMENT NUMBER: 105\_012900\_00A

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