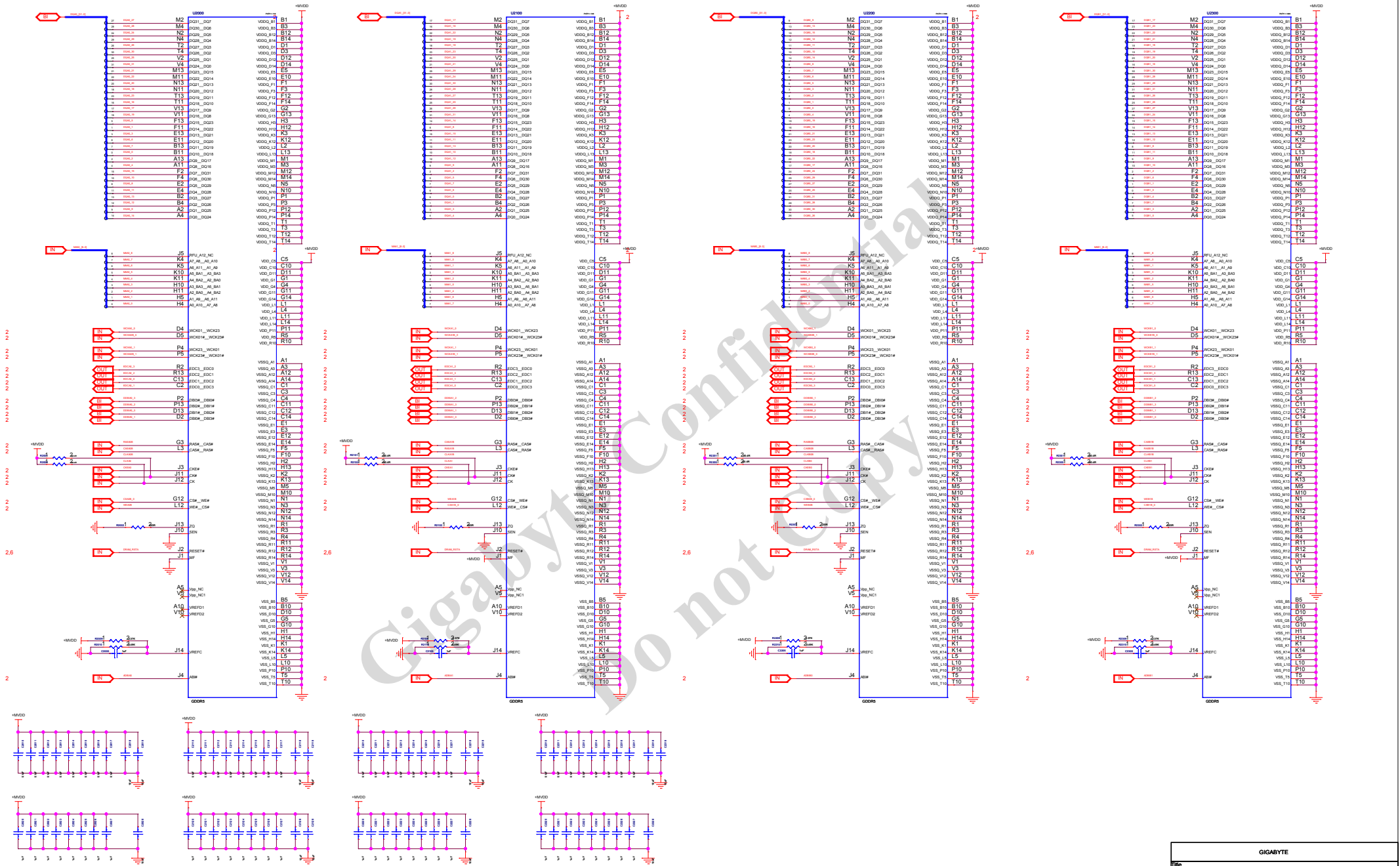


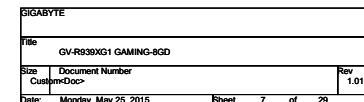
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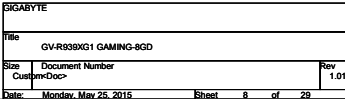
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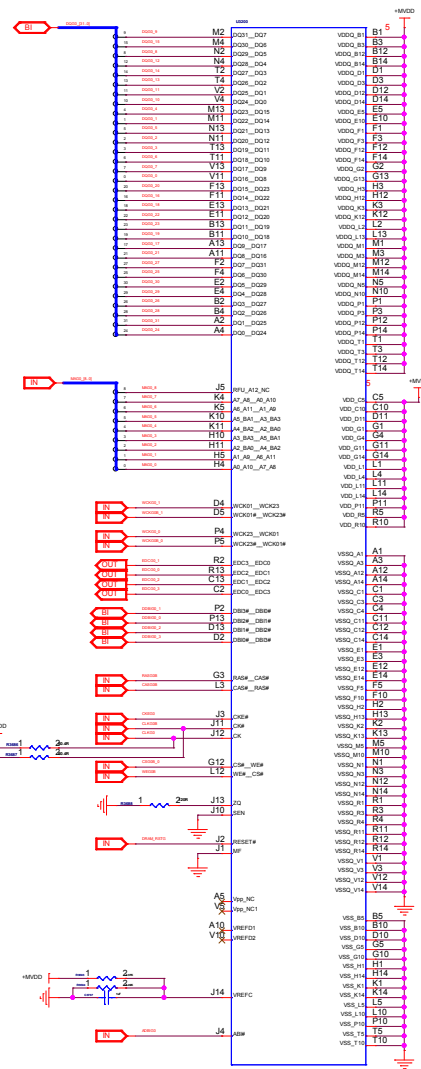


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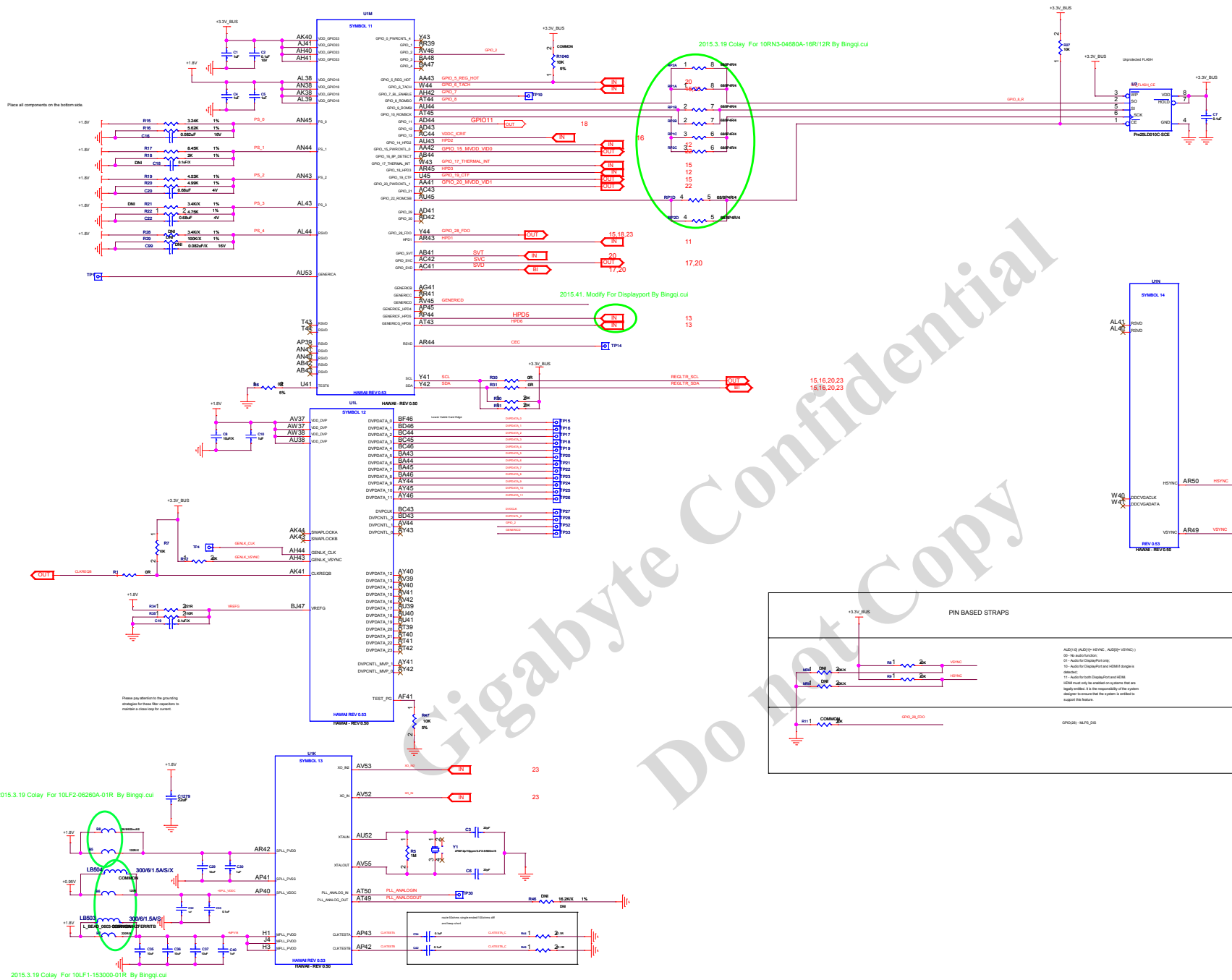
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2.9

5

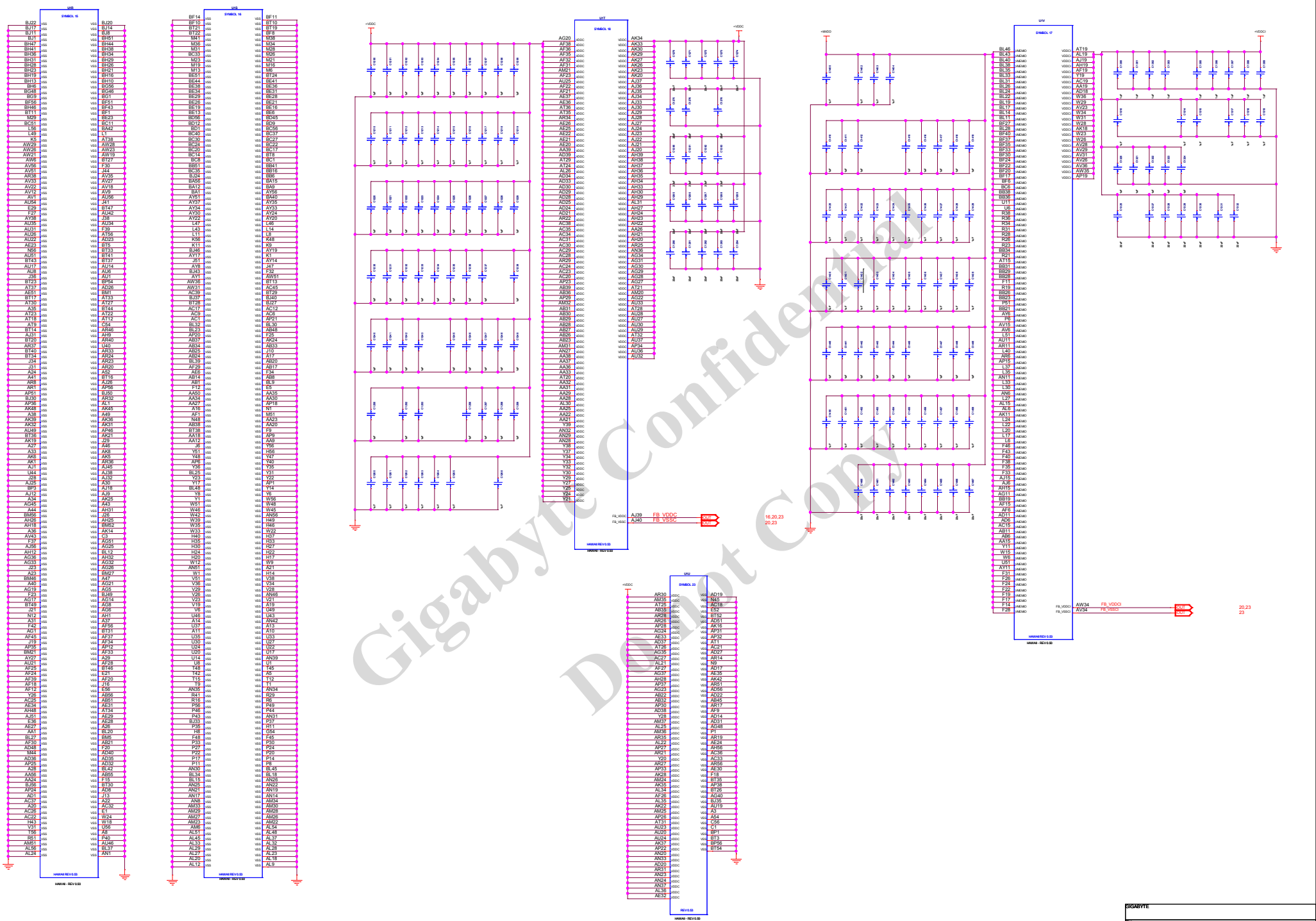


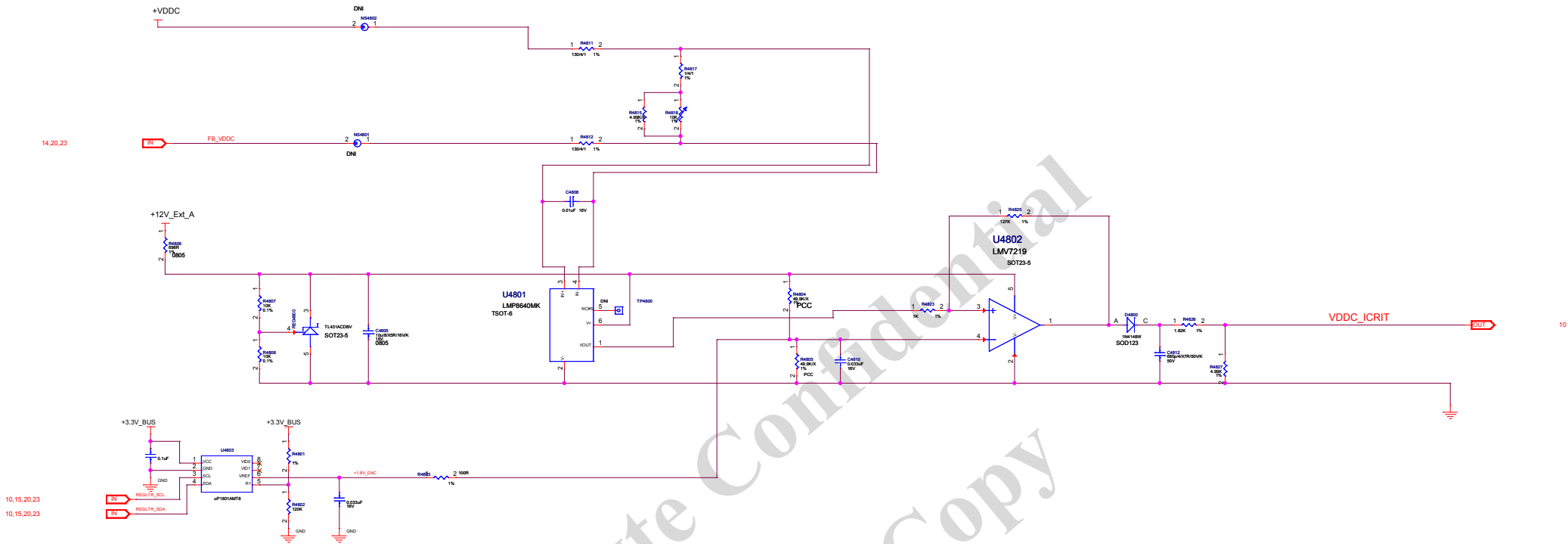
Place all components on the bottom side.

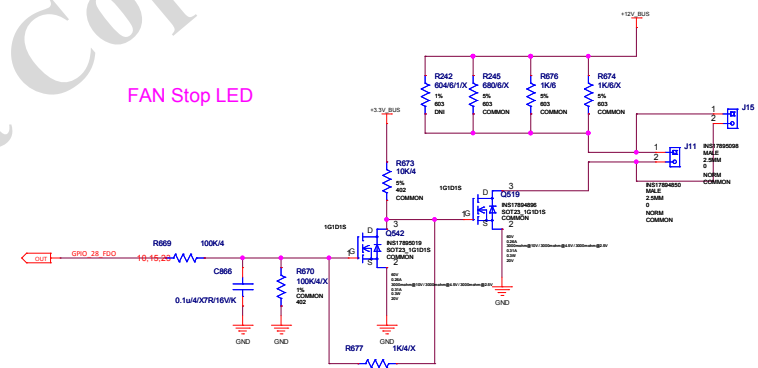
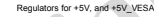


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Date:	Monday, May 25, 2015	Sheet 10 of 29

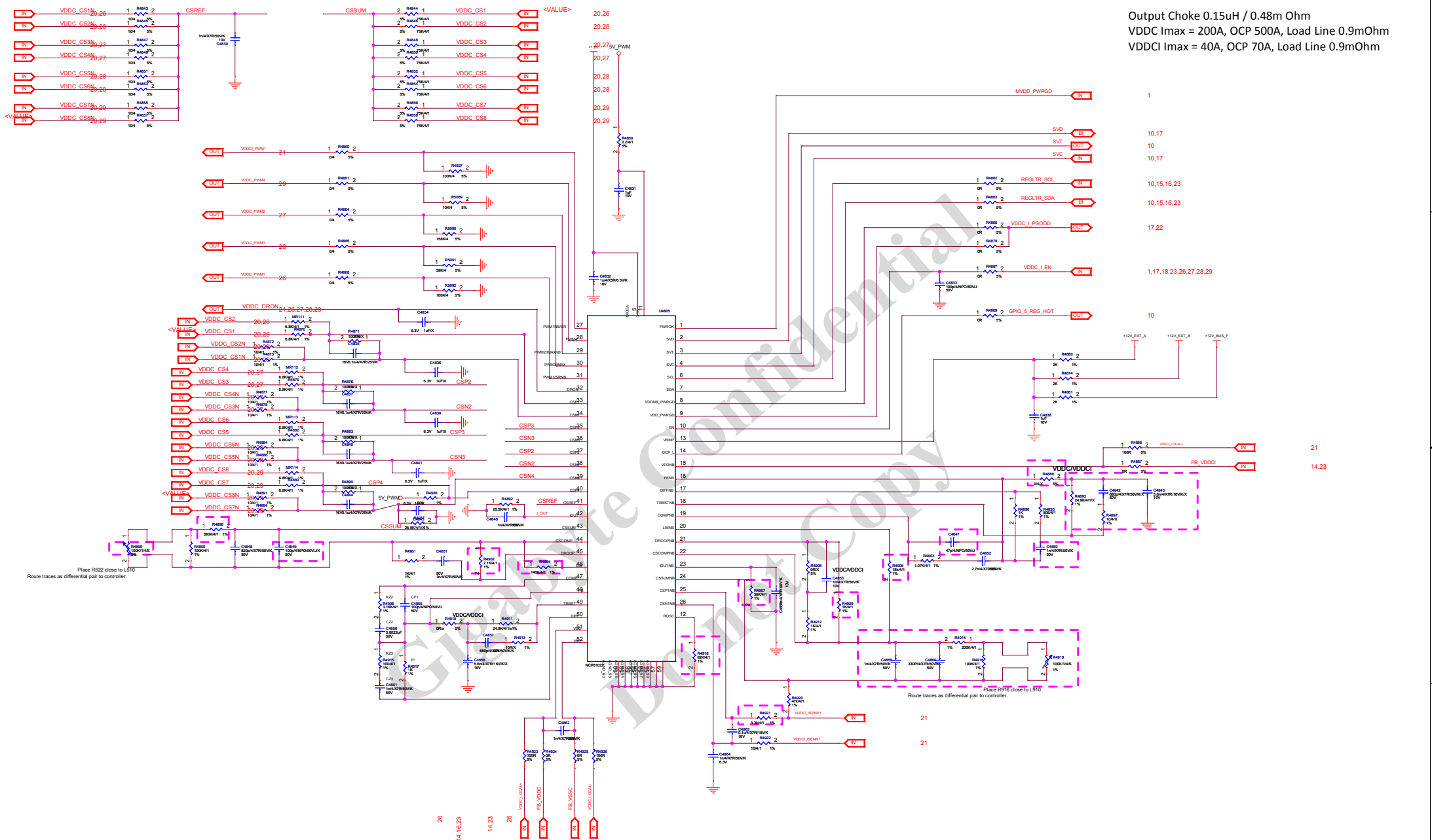
The schematic diagram illustrates the DPFE_CalR board, which is designed for signal processing. It features two identical channels, U2 and U4, each processing a set of input signals (AP53, ARS2, ARS4, ARS5, ARS3, AT52, AT54, AU55, AU56) and outputting DP_FPA1 and DP_FPA2 signals. The board includes a power supply section with +5V_VESA and +3.3V_BUS rails, and a connector for DP_FPA1 and DP_FPA2. The board is labeled '16096 REV 5.30'.





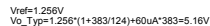


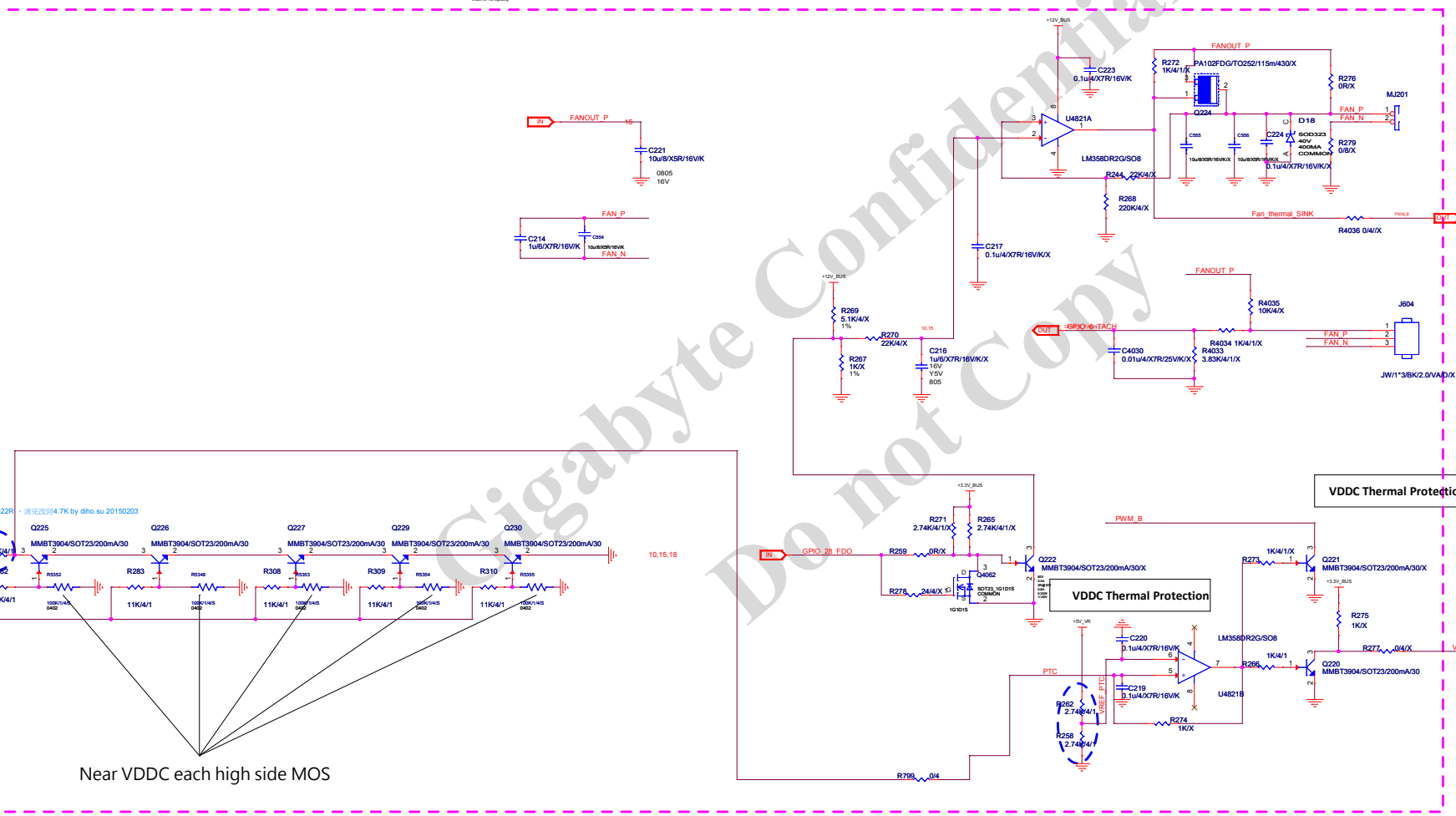
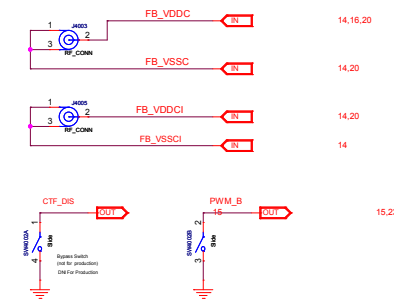
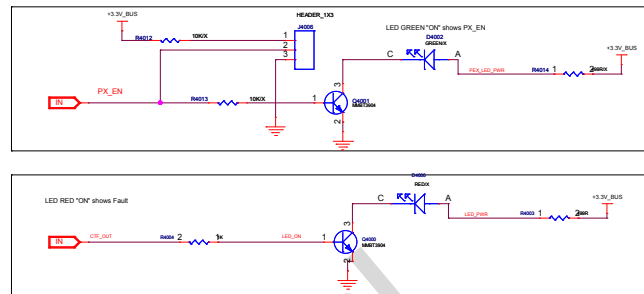
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Date:	Monday, May 25, 2015	Sheet	18 of 29



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Date	Monday, May 26, 2015	Sheet 20 of 29

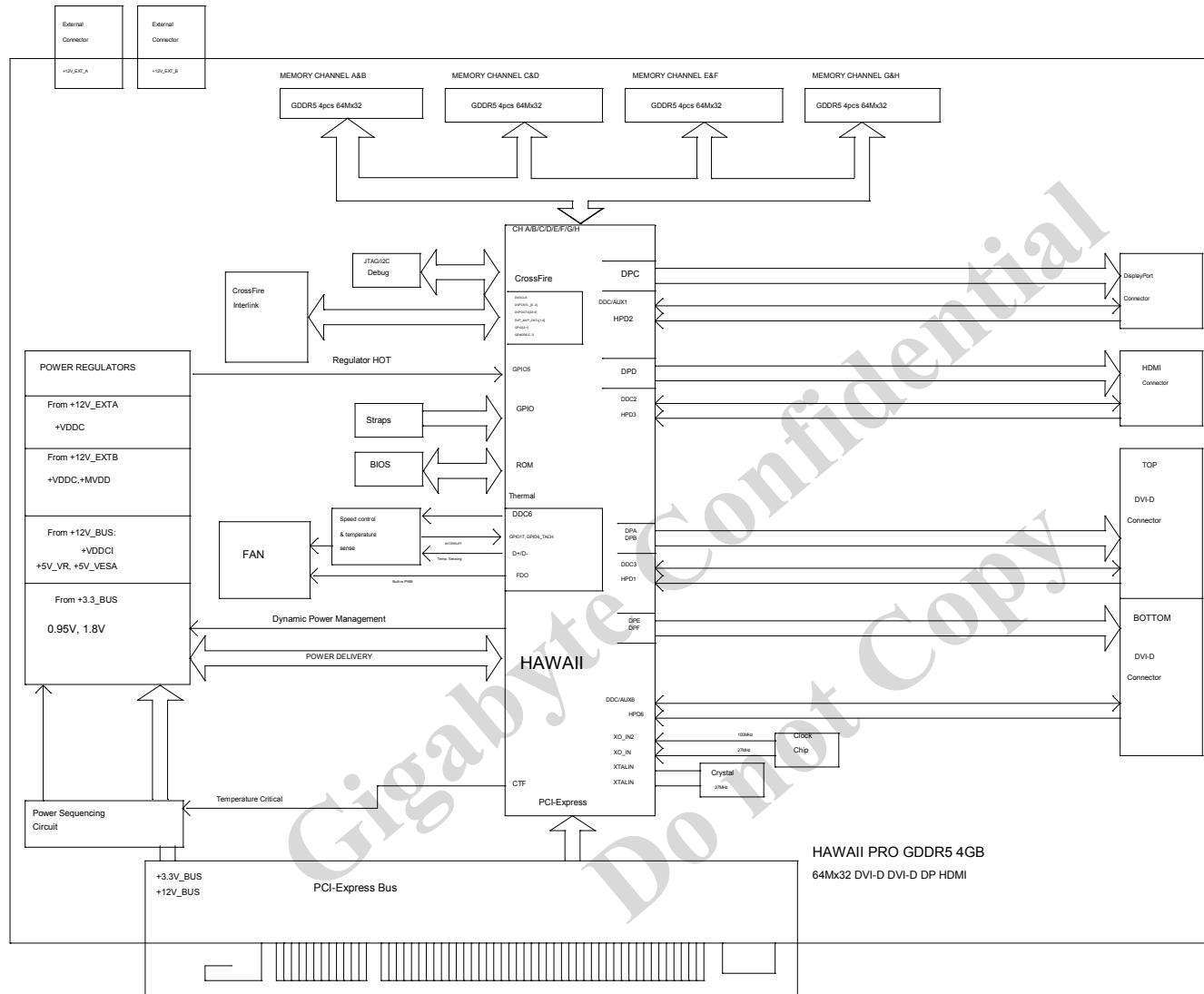
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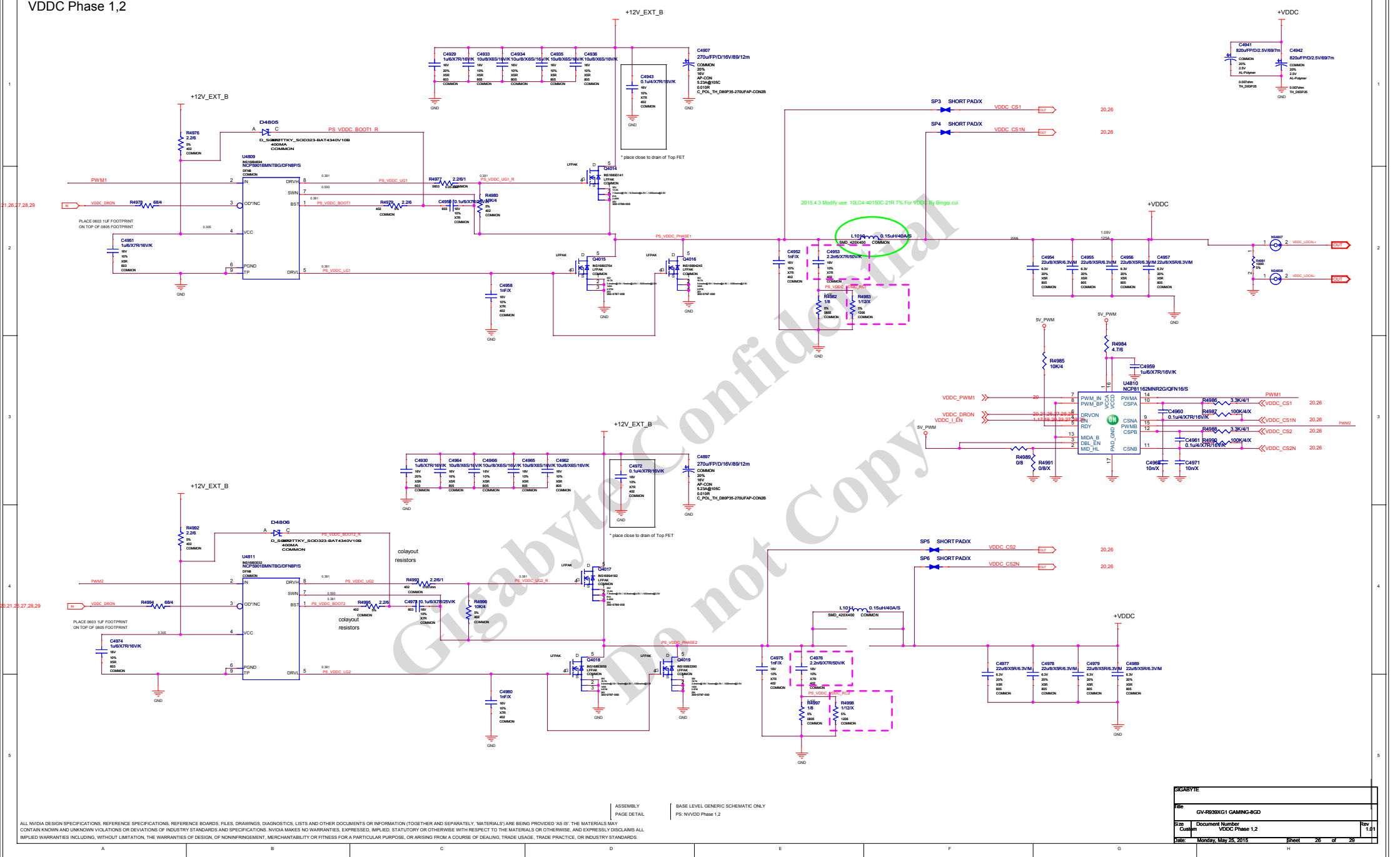
Near VDDC each high side MOS

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Date:	Monday, May 25, 2015	Sheet	23 of 29



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AMD				TITLE: Hawaii XT CR		DOCUMENT NUMBER: 105-C87900-008		DATE: Mon Jan 13 03:07:00 2014		SHEET NUMBER: 26 OF 26		REV: 1.0			
REVISION HISTORY				ENGINEER: Anatoly FRidman		NOTES: NOTE		<div>CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding the schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.</div> <div>C 2013 Advanced Micro Devices</div>				AMD - GRAPHICS 1 COMMERCE VALLEY MARKHAM, ONTARIO, L3T 7X6			
SCH Rev	PCB Rev	Date	REVISION DESCRIPTION												
1	00A	Oct 03 2013	1) Based on C872. 2) VDDC/VDDCI regulator changed to C871 solution. 3) VR_HOT circuitry deleted and used C871 solution.												
<div>Gigabyte Confidential</div> <div>Do not Copy</div>															
8		7		6		5		4		3		2		1	

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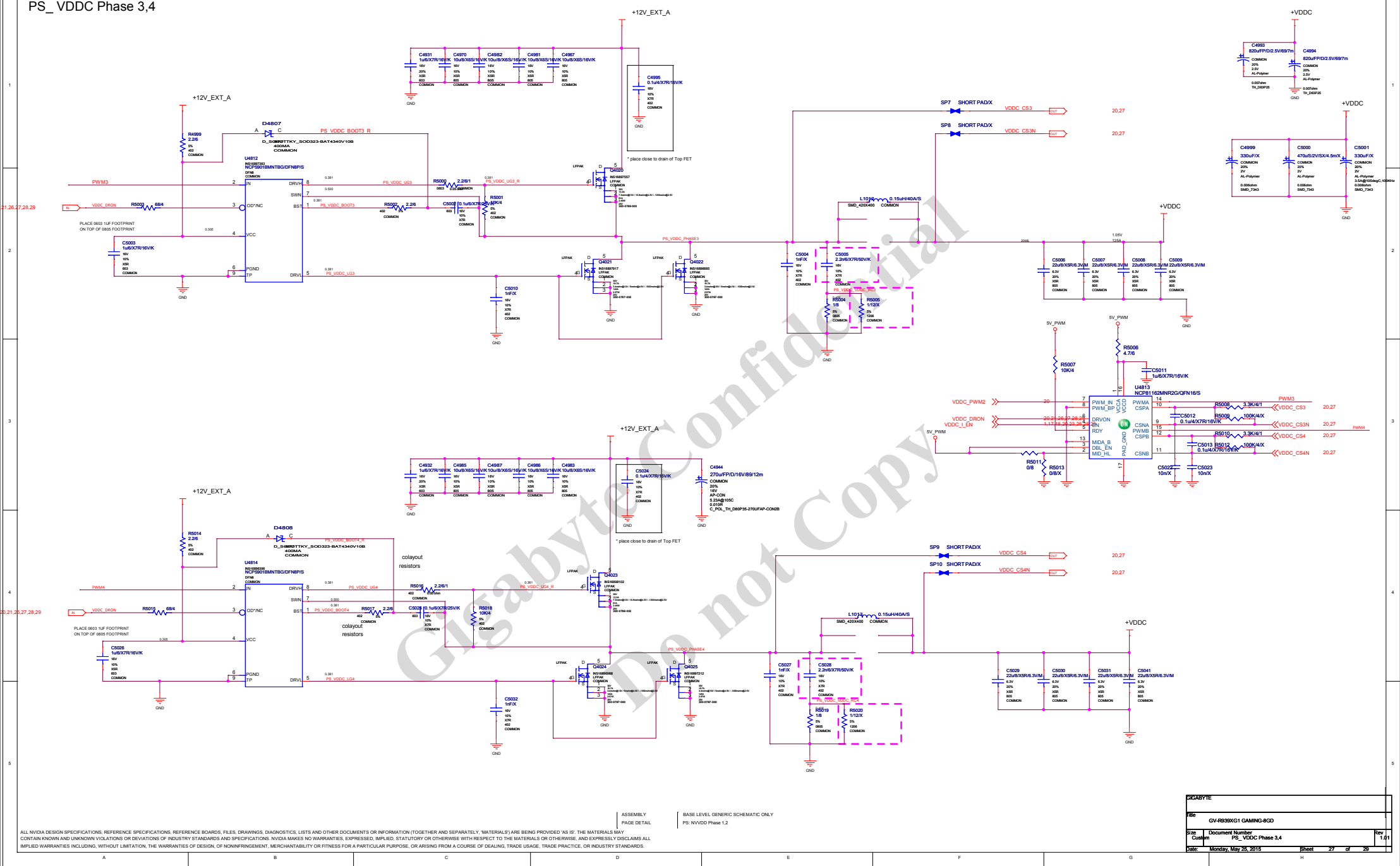


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Date	Monday, May 25, 2015	Sheet	26 of 28

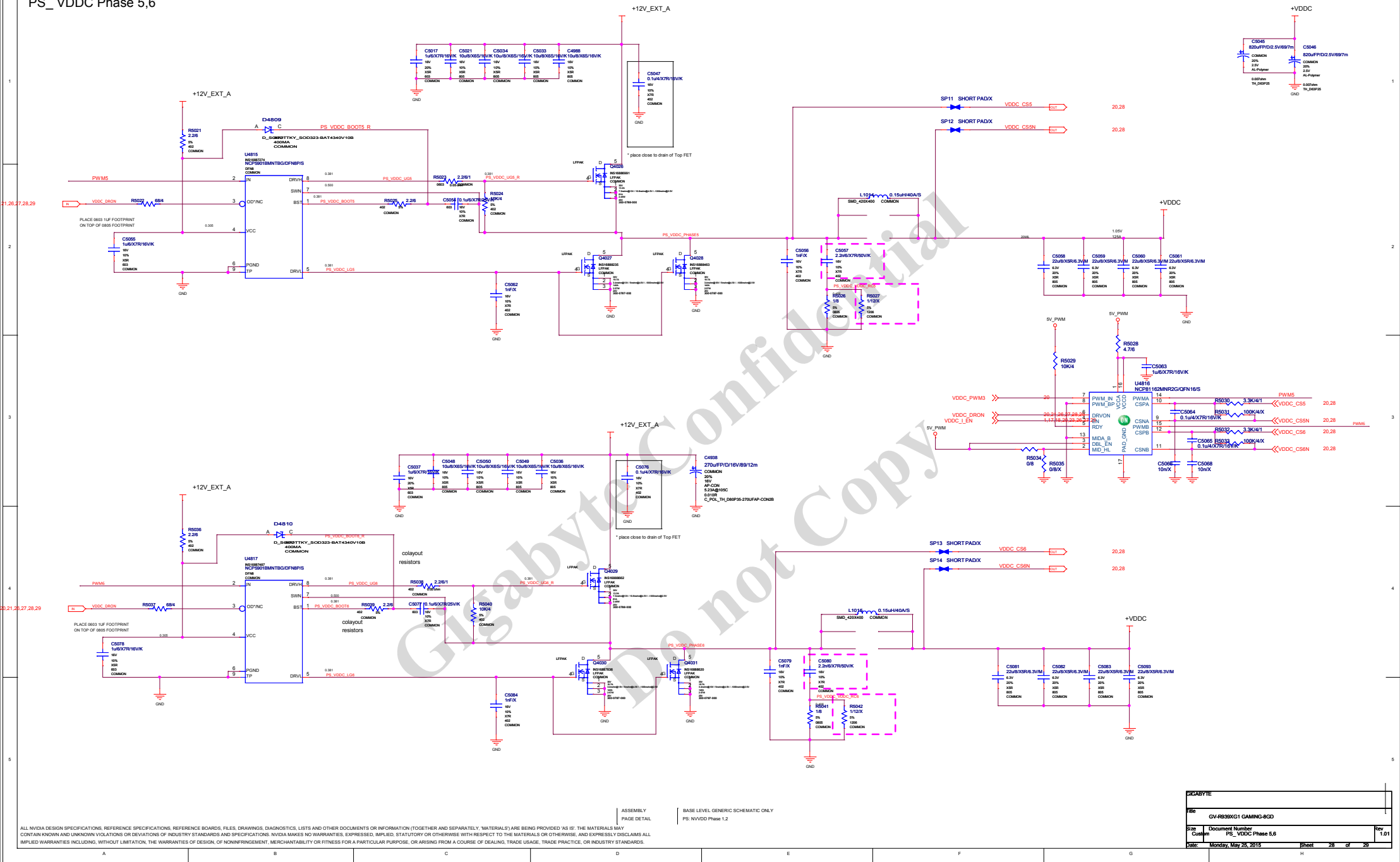
PS_ VDDC Phase 3,4



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Notes	Monday, Mar 28, 2011	Printed	39	of 90



PS_VDDC Phase 7,8

