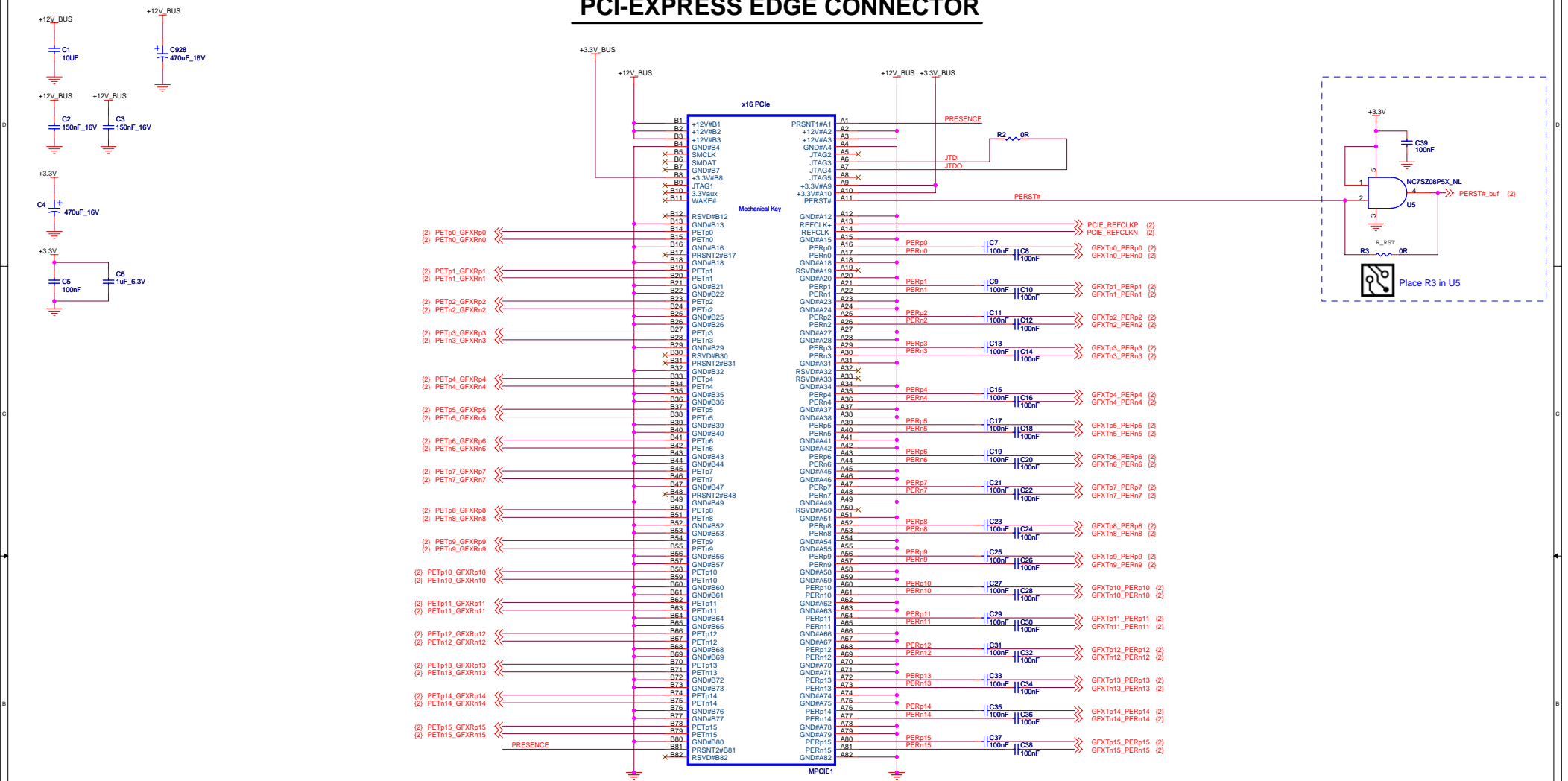


PCI-EXPRESS EDGE CONNECTOR

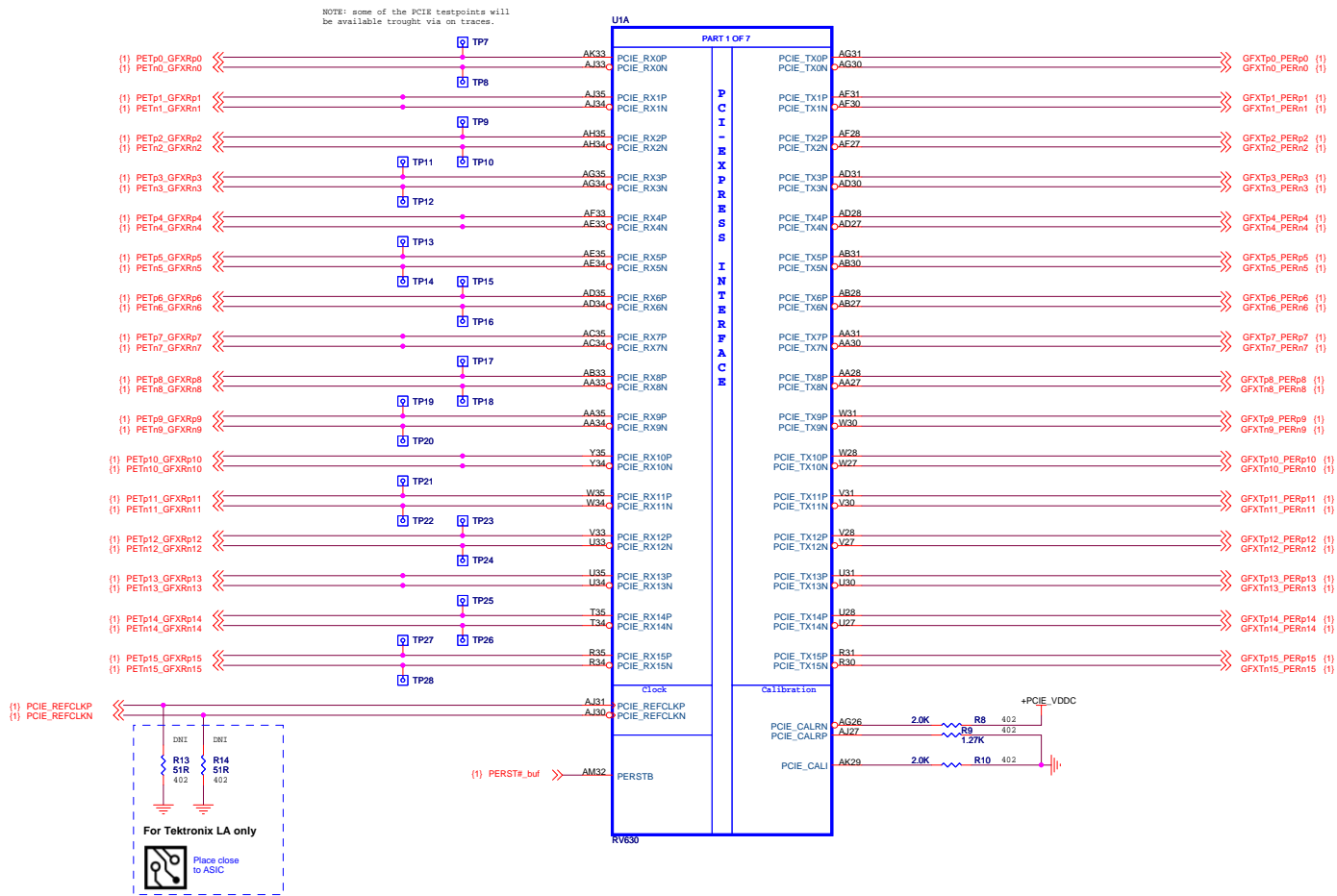


SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BLUO	BRING UP ONLY



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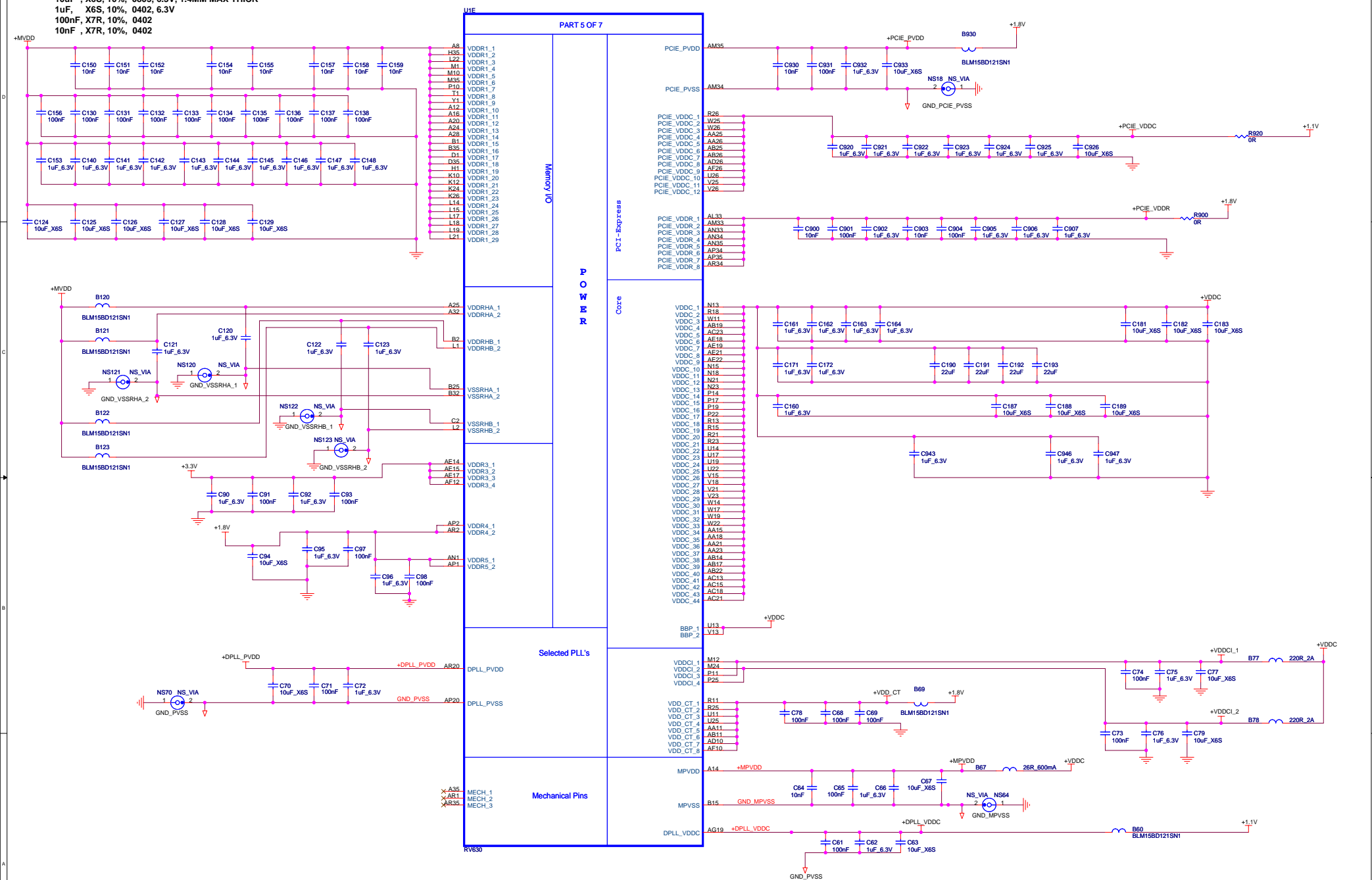
Title	RV630 GDDR3 - PCI-E Edge Connector		
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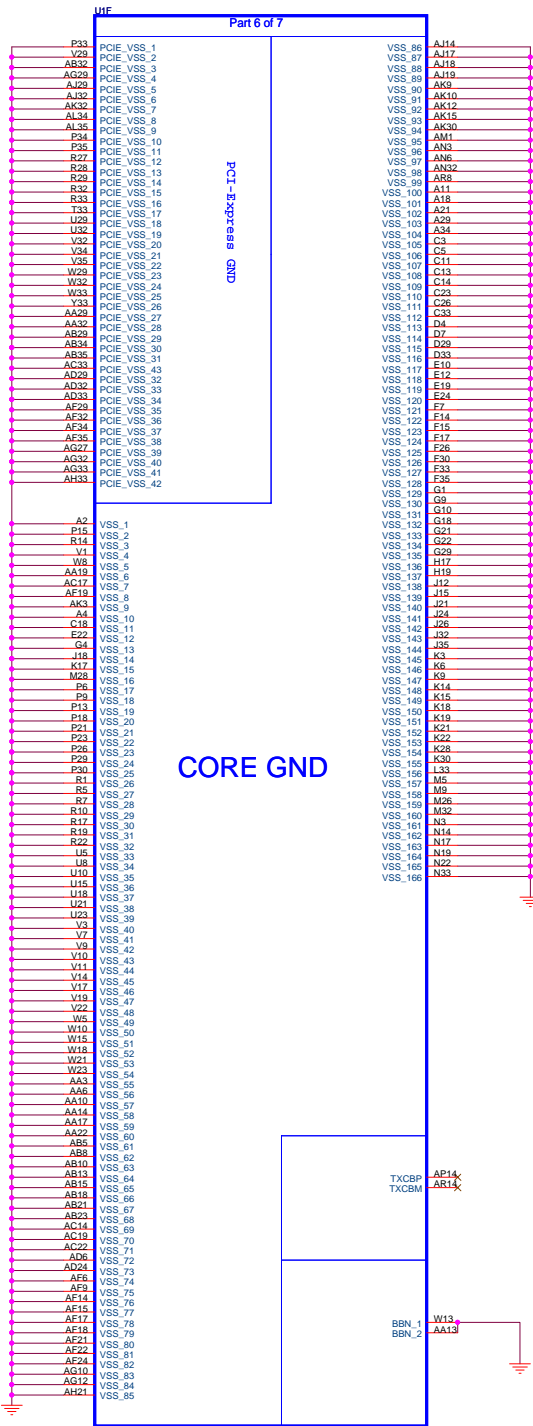
Title		RV630 GDDR3 - ASIC PCIe Interface	
Size	Document Number	105-B148xx-00A	Rev
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Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402



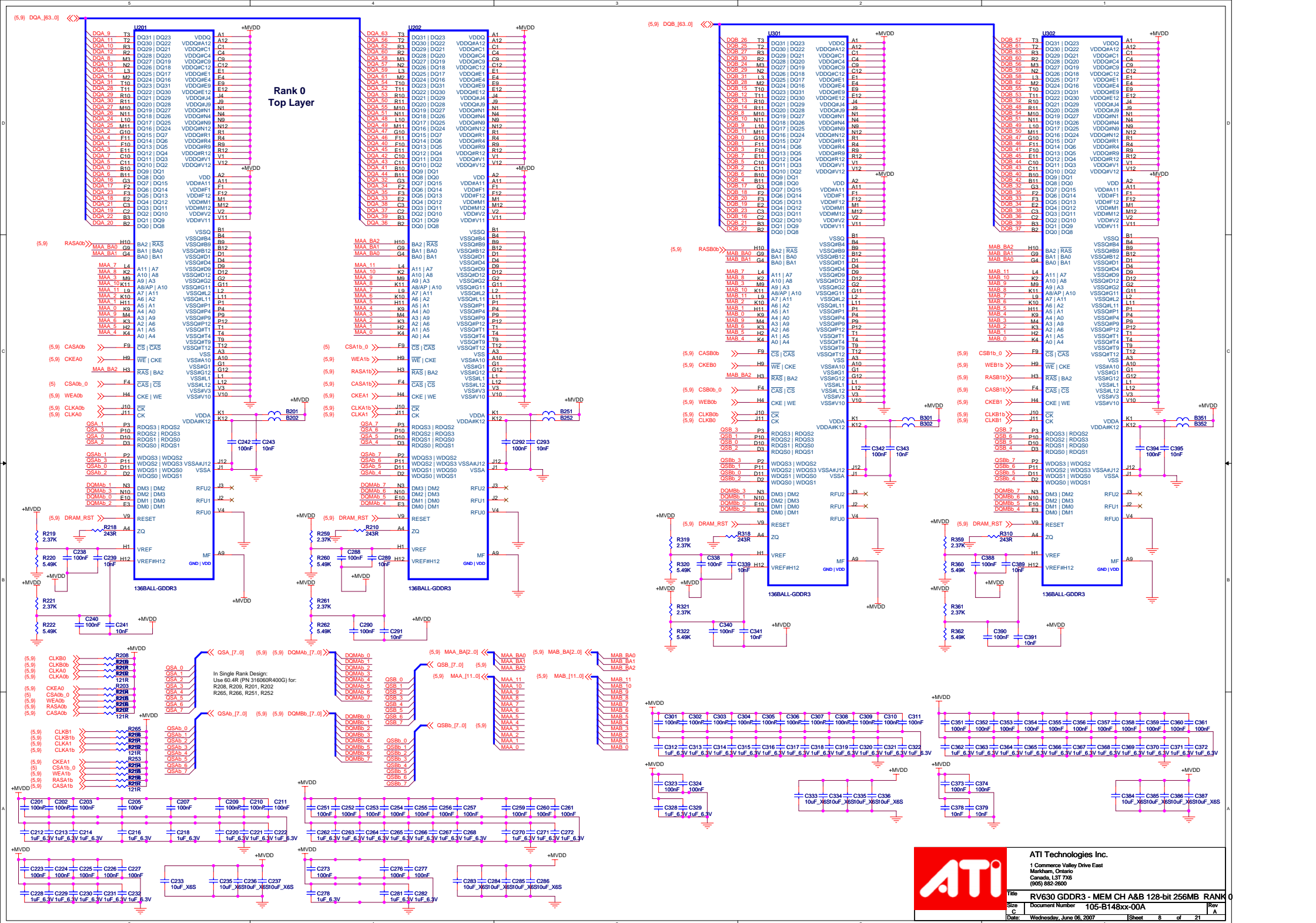
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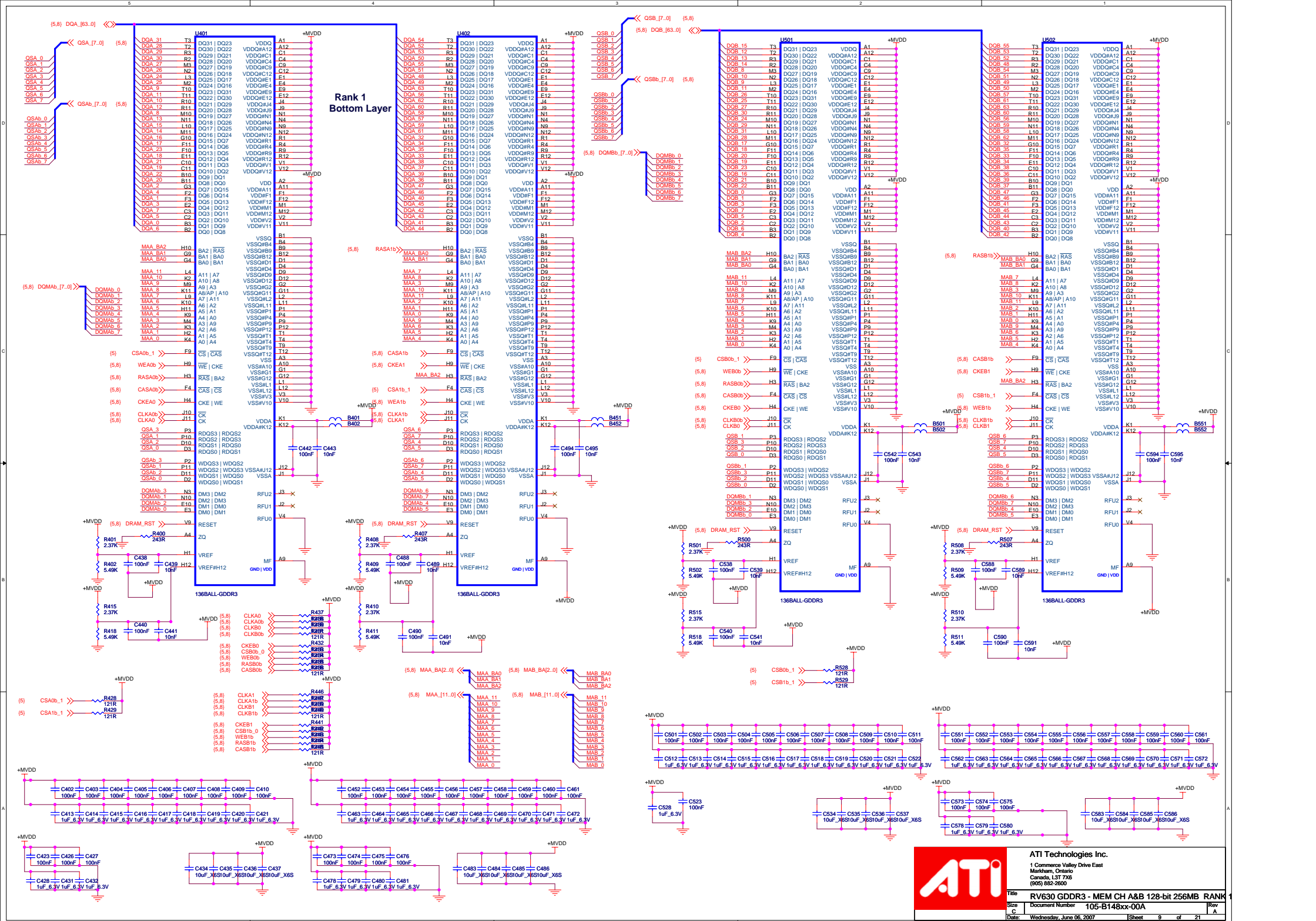
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Size	Document Number	105-B148xx-00A	
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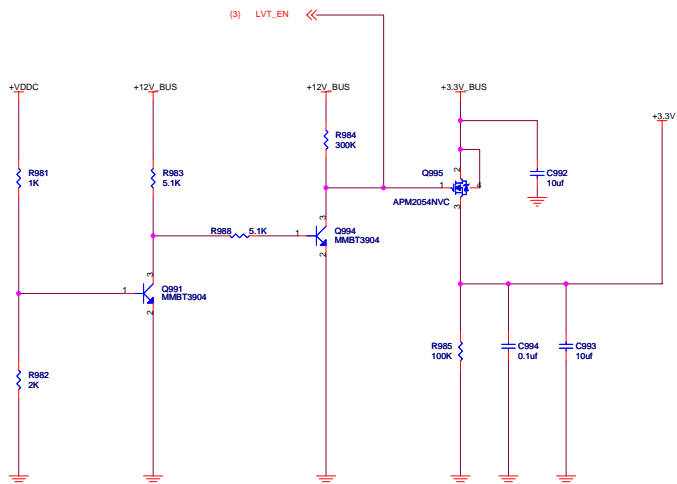


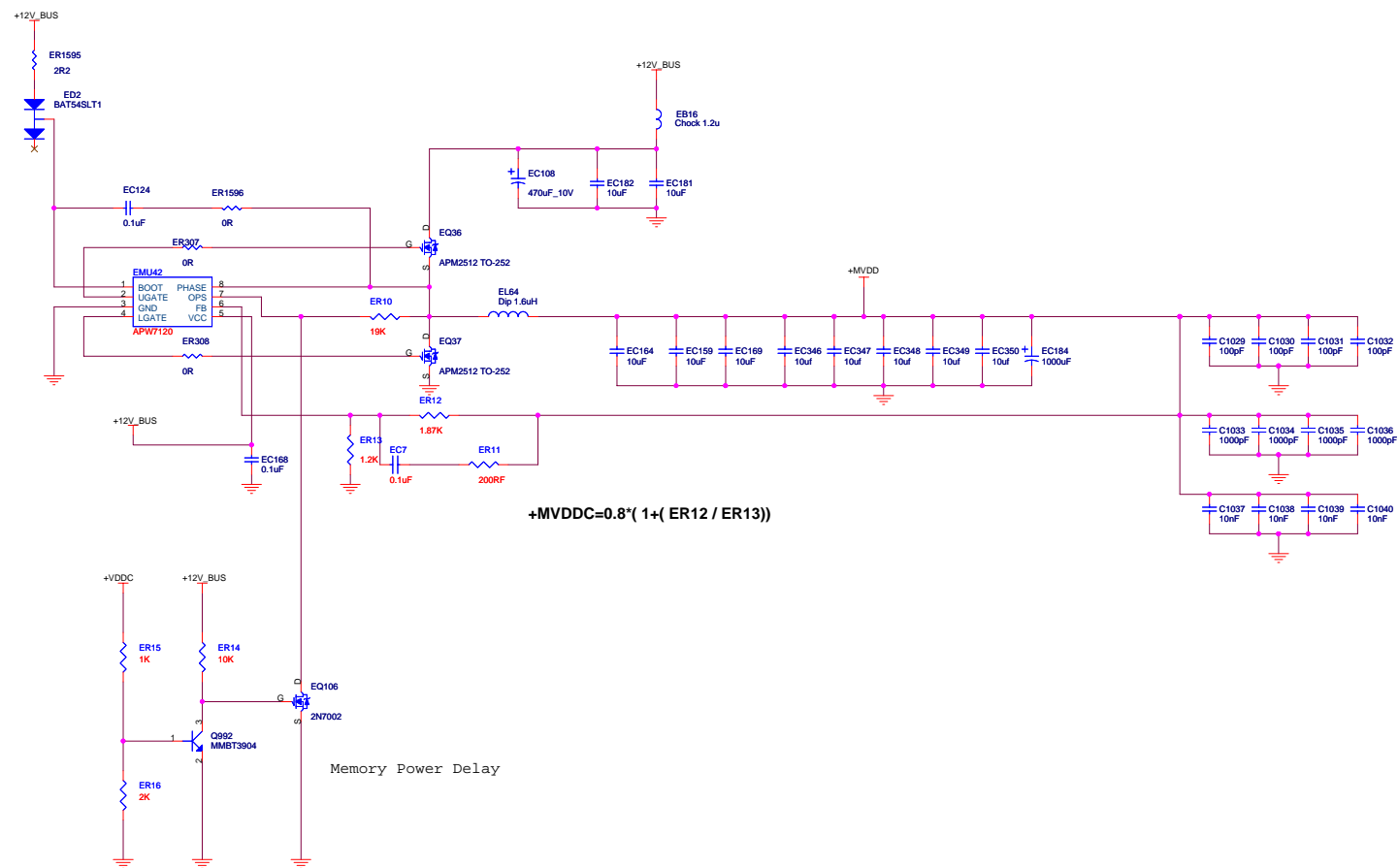
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Title		RV630 GDDR3 - ASIC Grounds	
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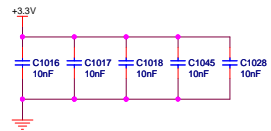
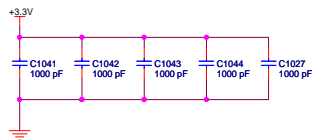
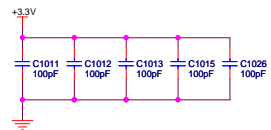
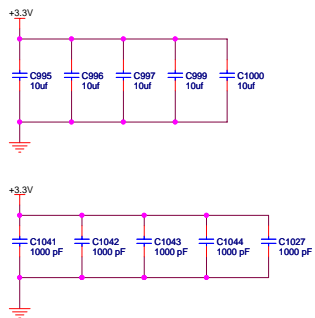


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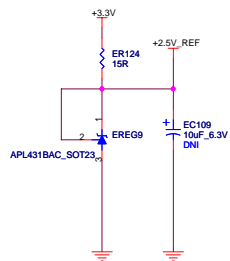
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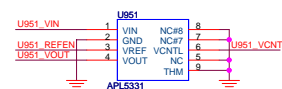
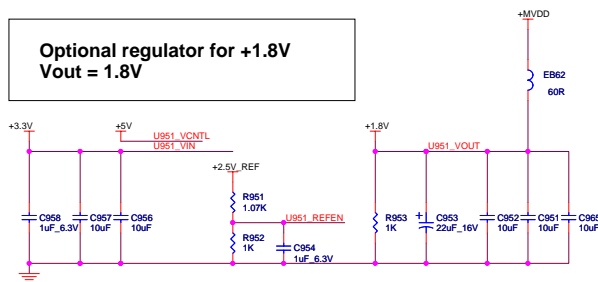


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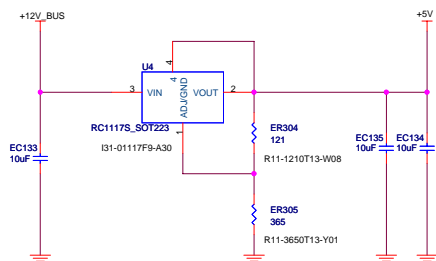
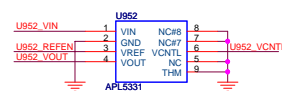
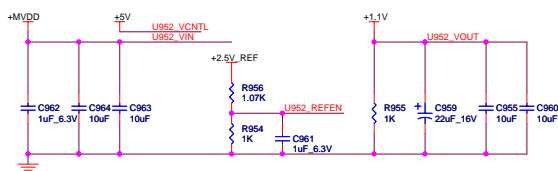
Title		RV630 GDDR3 - Power Management	
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Optional regulator for +1.8V Vout = 1.8V



Optional regulator for +1.1V Vout = 1.1V



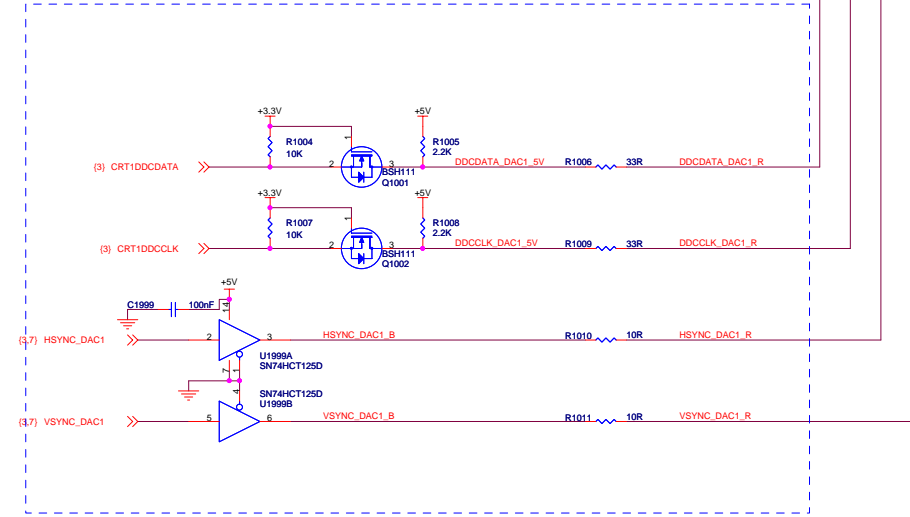
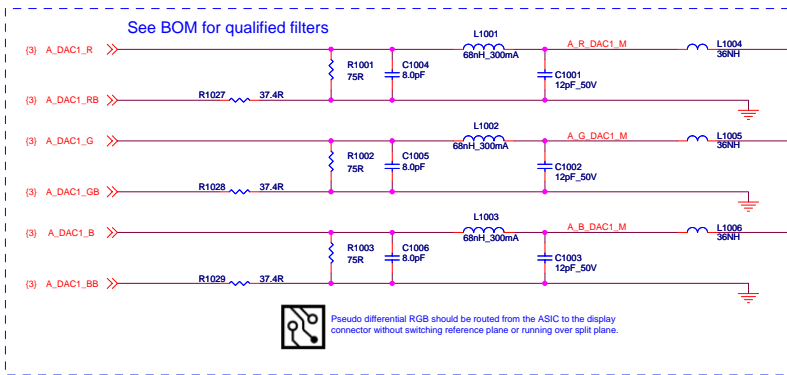
$$V_{out} = 1.25V \times \left[1 + \left(\frac{R_{305}}{R_{304}} \right) \right]$$

Shared Power Rails

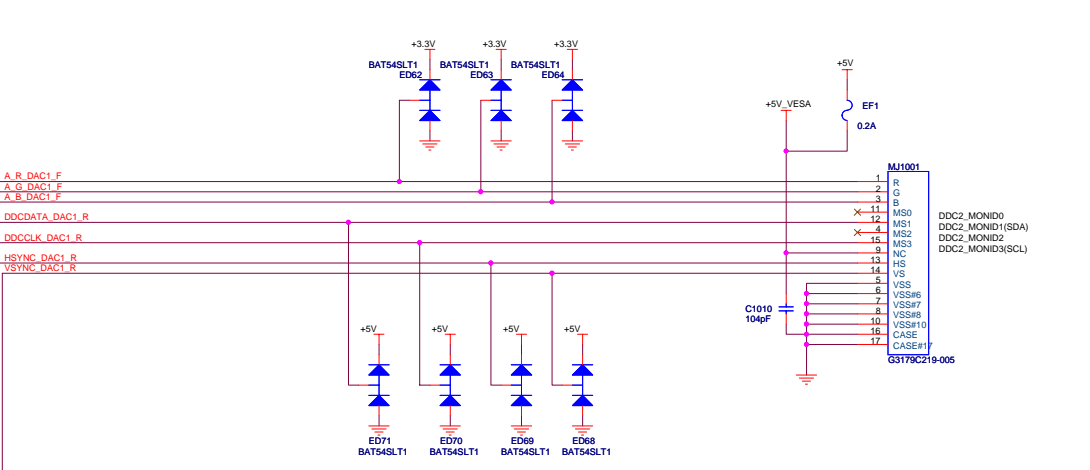
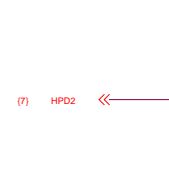


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Title	RV630 GDDR3 - Linear Regulators	Rev	A
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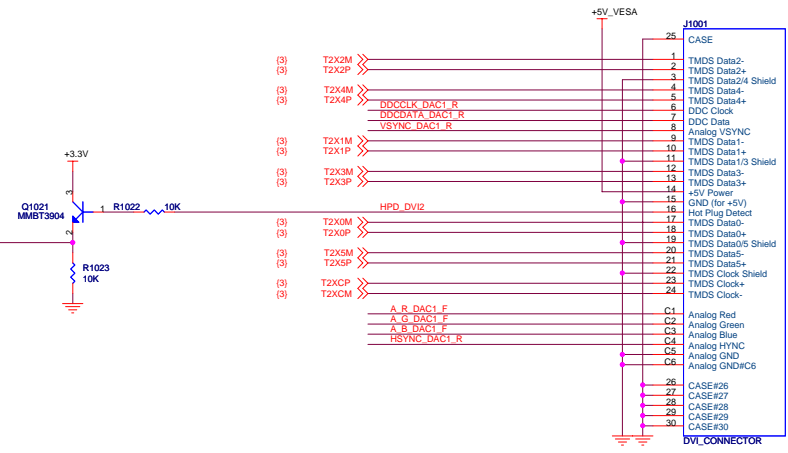


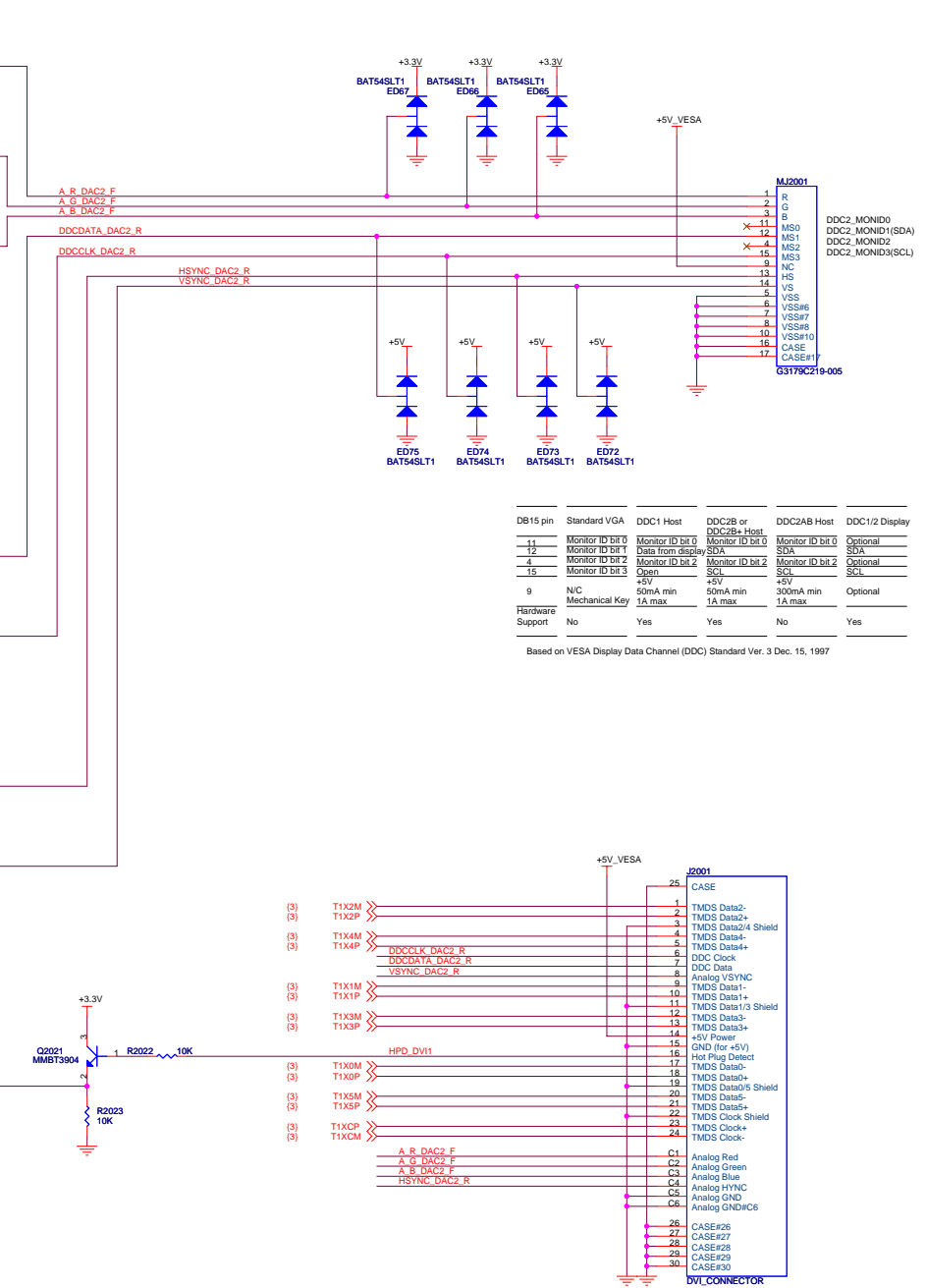
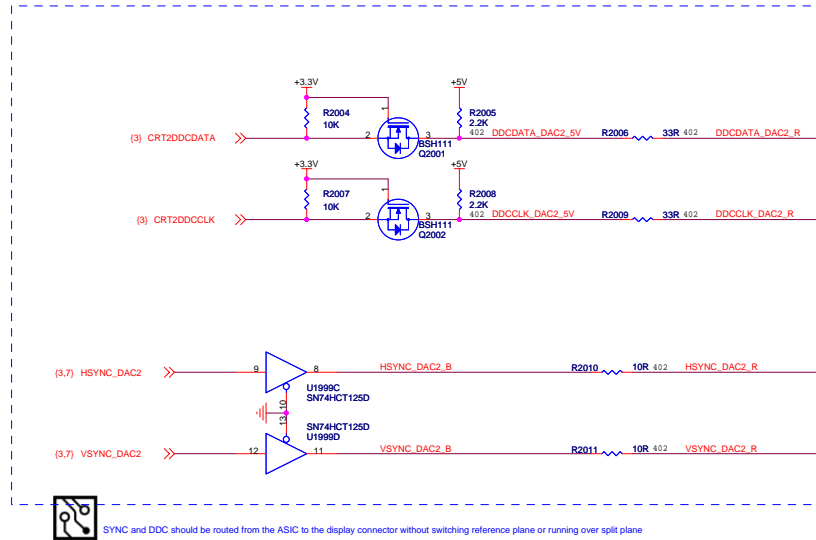
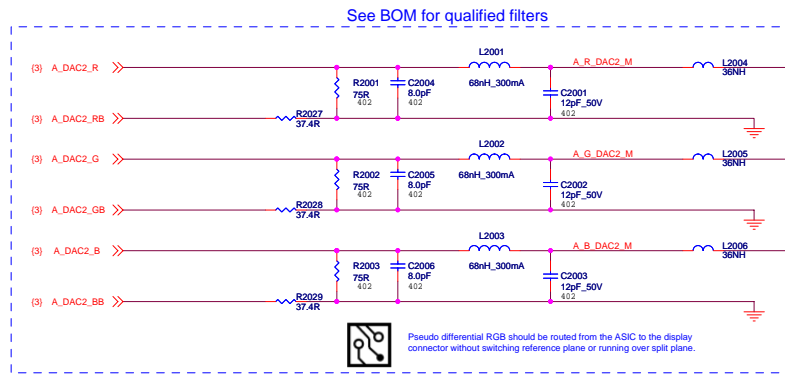
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

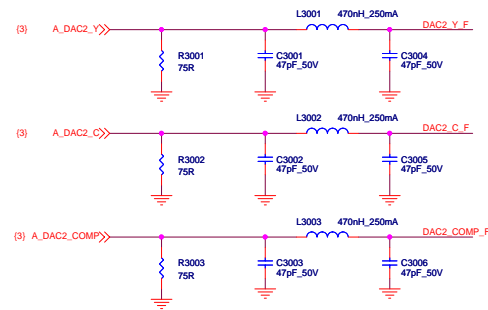


DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display SDA	SDA	SDA	Optional
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	Open	Open	Optional
9	N/C	+5V	+5V	+5V	Optional
Support	No	Yes	Yes	No	Yes

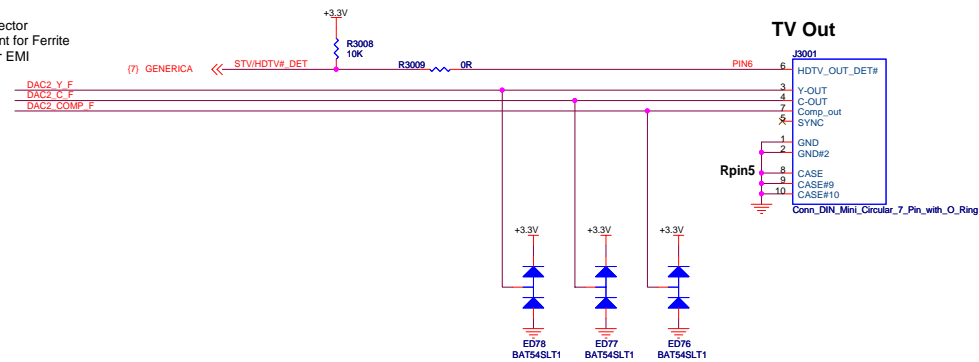
Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





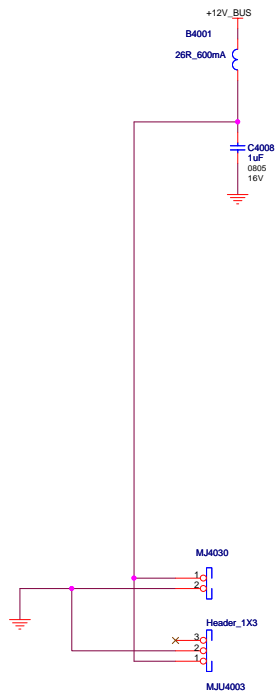


Place near connector
OR leaves footprint for Ferrite
Beads if req'd for EMI



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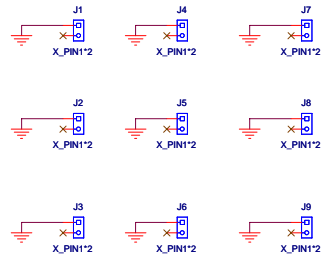
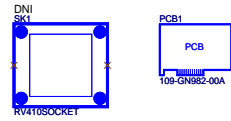
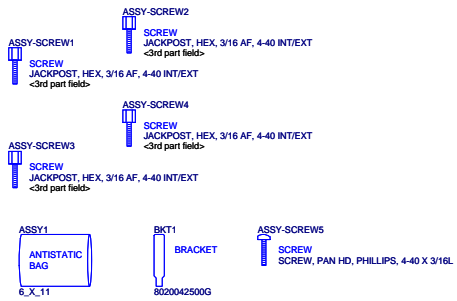
Title		RV630 GDDR3 - TVO	
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DVI/DVI SCREWS with top tab



<Variant Name>

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Title: RV630 GDDR3- Mechanical			
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Title

RH PCIE RV630 2x256MB GDDR3 DUAL DL-DVI-I VIVO FH

Schematic No.

105-B148xx-00A

Date:

Wednesday, May 30, 2007

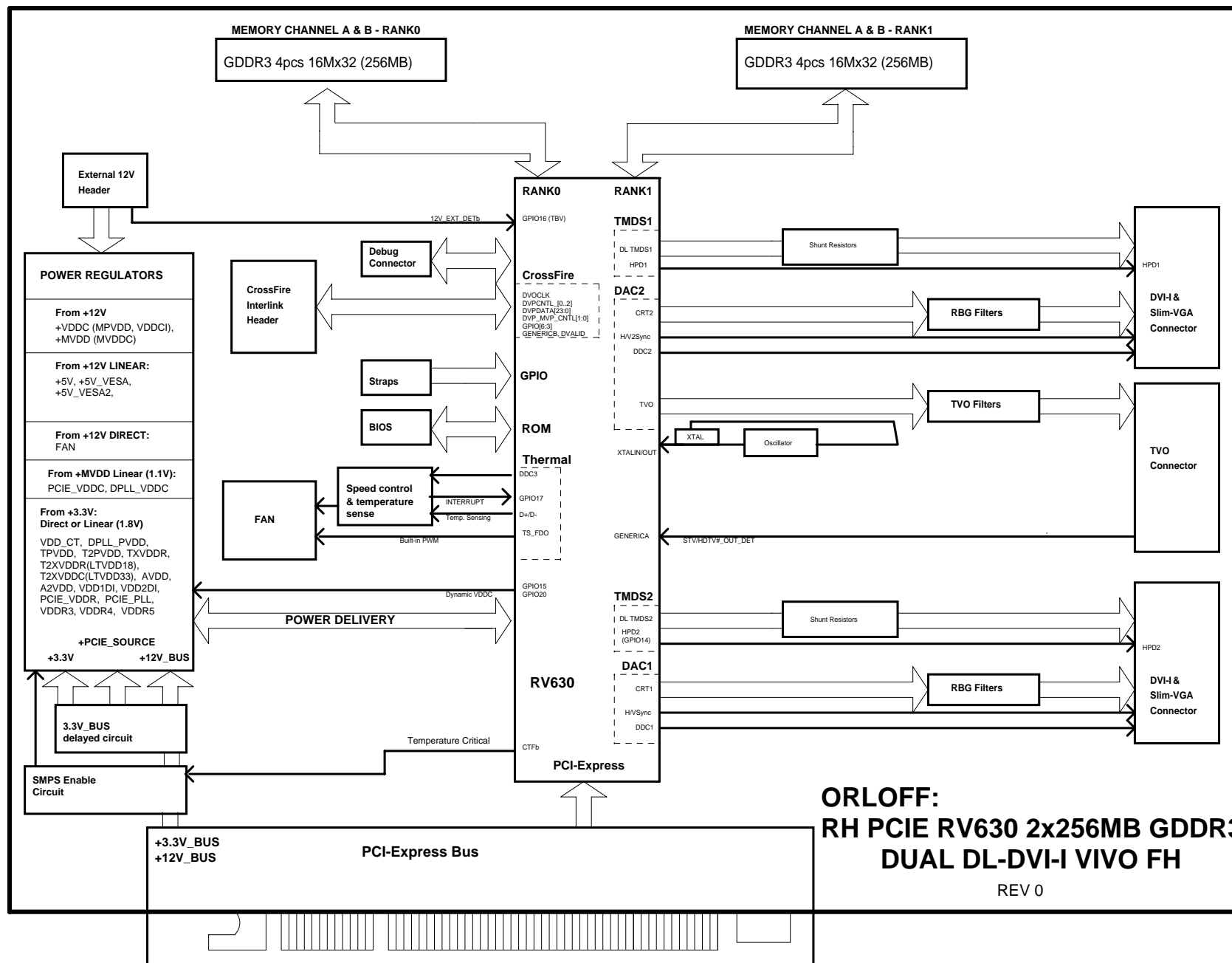
REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.

Rev

A

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/02/06	Initial design for RV630 GDDR3



ORLOFF:
RH PCIE RV630 2x256MB GDDR3
DUAL DL-DVI-I VIVO FH

REV 0



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Title RV630 GDDR3 - BLOCK DIAGRAM

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