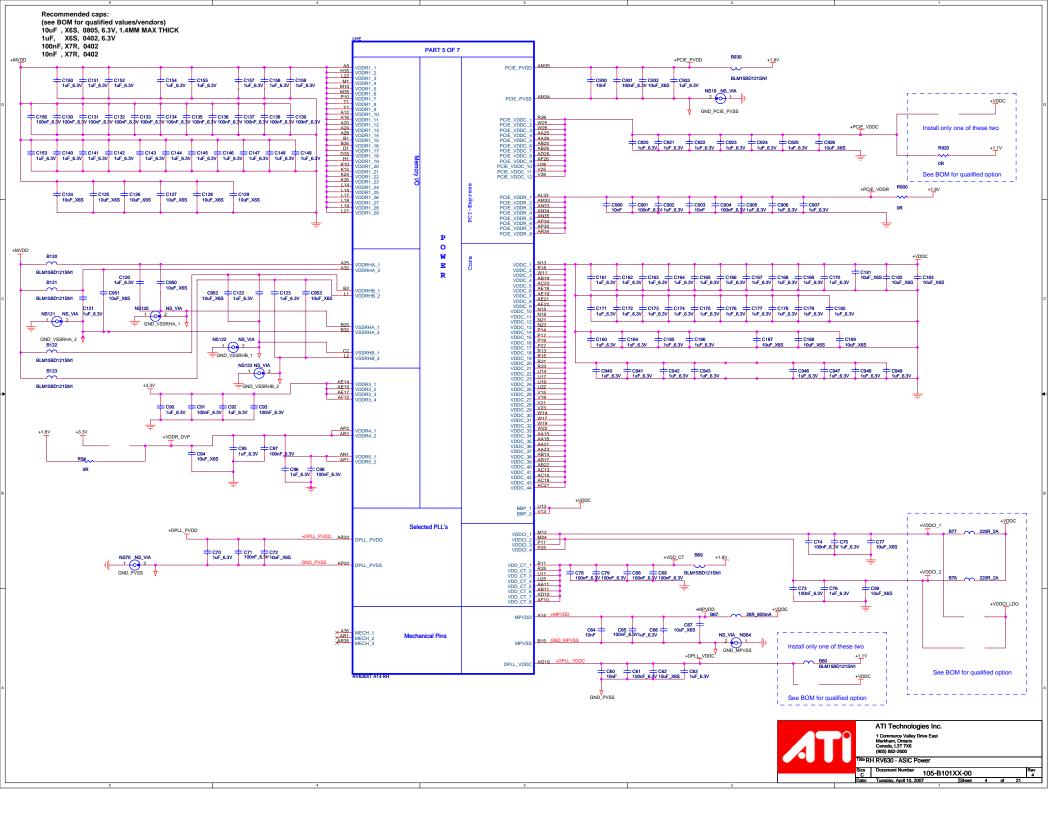


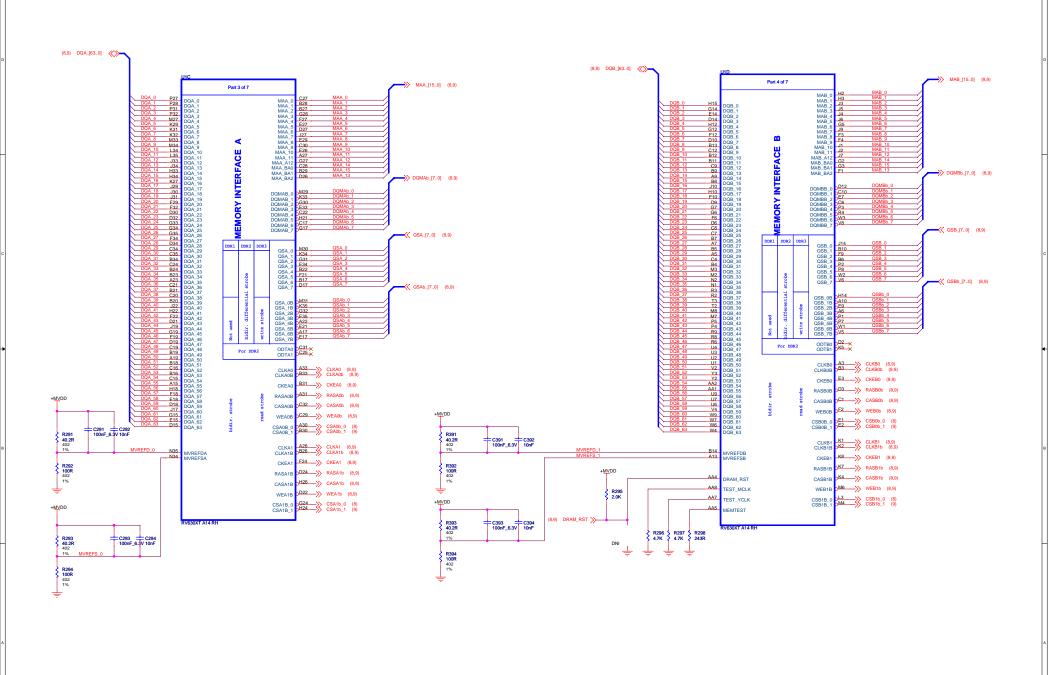


Recommended caps: (see BOM for qualified values/vendors) 10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK 1uF, X6S, 0402, 6.3V 100nF, X7R, 0402 10nF, X7R, 0402 Place close to ASIC Place close to ASIC PART 2 OF 7 (15) T2XCM (15) T2XCR TXCAM TXCAP R110 182R R100 _____100F TX0M TX0P R101 _____ 100F AR23 AP23 R102 _____100I AR24 AR12 (15) T2X2M(-(15) T2X2R(-T2X2M T2X2P TX2M TX2P AP24 AP12 R103 100R AR25 TX3M TX3P R104 100R +1.8V T2X4M T2X4P TX4M TX4P R105 _____ 100 Q100 SI2304DS +12V_BUS TX5M AR17 TX5P AP17 AR27 Γ2X5M Γ2X5P TPVDD AM14 TPVSS AL14 AL22 AK22 +T2PVDD +TPVDD I M E D NS110 NS_VIA C101 = 100nF_6.3V C110 + C111 + C112 10nF 100nF 1uF_6.3V C100 = C102 = 10uF_X6S 1uF_6.3V C113 10uF_X6S AK27 AL27 T2XVDDC_1 T2XVDDC 2 TXVDDR_2 TXVDDR_3 TXVDDR_4 TXVDDR_5 GND_T2PVSS V GND_TPVSS +LTVDD18 TXVDDR_4 TXVDDR_5 +TXVDDR B100 AJ26 AH26 C116 = C117 1uF_6.3V 10uF_X6S TXVSSR_1 TXVSSR_3 TXVSSR_4 TXVSSR_5 TXVSSR_6 TXVSSR_6 AN11 AN12 AN13 AN14 AN15 AN16 AN17 AN18 C103 -C108 C109 _____ 100nF_6.3V C114 10nF 10uF_X6S +<u>3.3</u>V 1uF_6.3V T2XVSSR_1 T2XVSSR_2 T2XVSSR_3 AN21 AN24 AN25 AN28 MR109 0R 2XVSSR_4 2XVSSR_5 TXVSSR_ TXVSSR_ AR18 AP21 AP26 Share one pad I TXVSSR 1 T2XVSSR_6 T2XVSSR_7 T2XVSSR_8 T2XVSSR_9 T2XVSSR_10 T2XVSSR_11 T2XVSSR_11 T2XVSSR_12 T2XVSSR_13 T2XVSSR_14 +LTVDD33 乖 A_DAC1_R (15) A_DAC1_RB (15) AR21 AR26 AM22 AM22 AM24 AM26 AM27 A 2101 A_DAC1_G (15) A_DAC1_GB (15) DAC/CRT C106 : 1uF_6.3V C105 = 100nF_6.3V BSH111 AR29 ----->> HSYNC1_TRST (1) (1) DDC1DATA_TDI →>> HSYNC_DAC1 (7,15) →>> VSYNC_DAC1 (7,15) HSYNC VSYNC +3.3V (15) CRT1DDCDATA (15) CRT1DDCCLK AL29 +AVDD 12C DEVICE ADDRESS' ON DDC3 AN31 RSET R1030 499R GND_AVSSQ ->> VSYNC1_TCK (1) R40 R41 4.7K 4.7K 402 402 DDC2DATA AR32 AVDD C1020 + C1021 + C1022 100F 1000F_6.3V 1uF_6.3V NS1020 NS_VIA 2 0 1 || I BUO 402 402 DDC3DATA Monitor DDC3CLK Interface AP32 (11,13,18) DDC3DATA (11,13,18) DDC3CLK AVSSQ +VDD1DI DDC4DATA DDC4CLK AR28 VDD1DI C1023 — C1024 — C1025 10nF 100nF_6.3V1uF_6.3V NS1021 NS_VIA AP28 VSS1DI (16) HPD1 >> IPD1 (1) DDC3CLK_TDO <<-GND_VSS1DI A_DAC2_R (16) A_DAC2_RB (16) (1) DDC1CLK_TMS <<-(7) SDA (7) SCL MMI2C DAC2 (TV/CRT2) G2 A_DAC2_G (16) A_DAC2_GB (16) G2B A_DAC2_B (16)
A_DAC2_BB (16) AM4 AG21 → HSYNC_DAC2 (7,16) VSYNC_DAC2 (7,16) H2SYNC TP42 PLL TEST TEST_EN PLLTEST TESTEN COMP (1) TEST_EN_R (R2SET R2030 715R GND_A2VSSQ AJ21 R2SET +A2VDDQ A2VDDQ Share one PAD R43 221R VREFG C2021 100nF_6.3V DNI A2VSSQ R44 110R C46 100nF_6.3V ΔH22 VDD2DI +VDD2DI GND_A2VSSQ AG22 AR33 AP33 VSS2DI XTALOUT_S is done for ease of layout (17) RTCLK >>-A2VDD +3.3V_BUS +A2VDD GND VSS2DI B2030 0R +3.3V B80 BLM15BD121SN1 Y81 XTALOUT S 4 VCC OUT

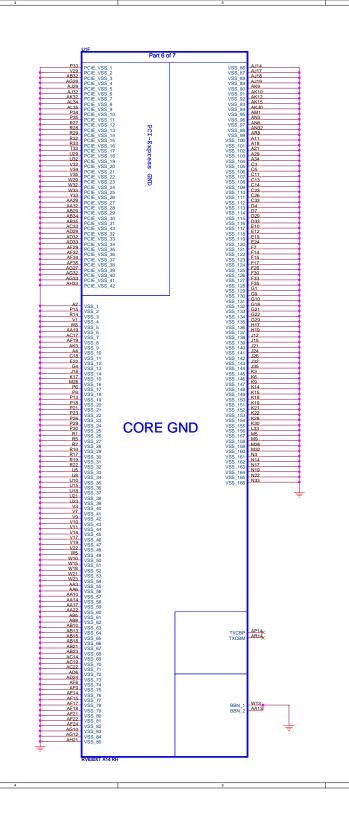
C80 2 GND E/D

100nF_6.3V 27.000MHz C2030 + C2031 + C2032 + C2033 10nF 100nF_6.3V 1uF_6.3V 10uF_X6S R81 182R R82 221R \mathscr{T} OSC EN ✓ OSC_EN (14,17) ->>> RTXTALIN (17) ATI Technologies Inc. R_RTCLK 1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600 XTALOUT ->> RTXTALOUT (17) Place R_RTCLK close to XTAL so the main clock line has shortest stub Title RH RV630 - ASIC MAIN 105-B101XX-00

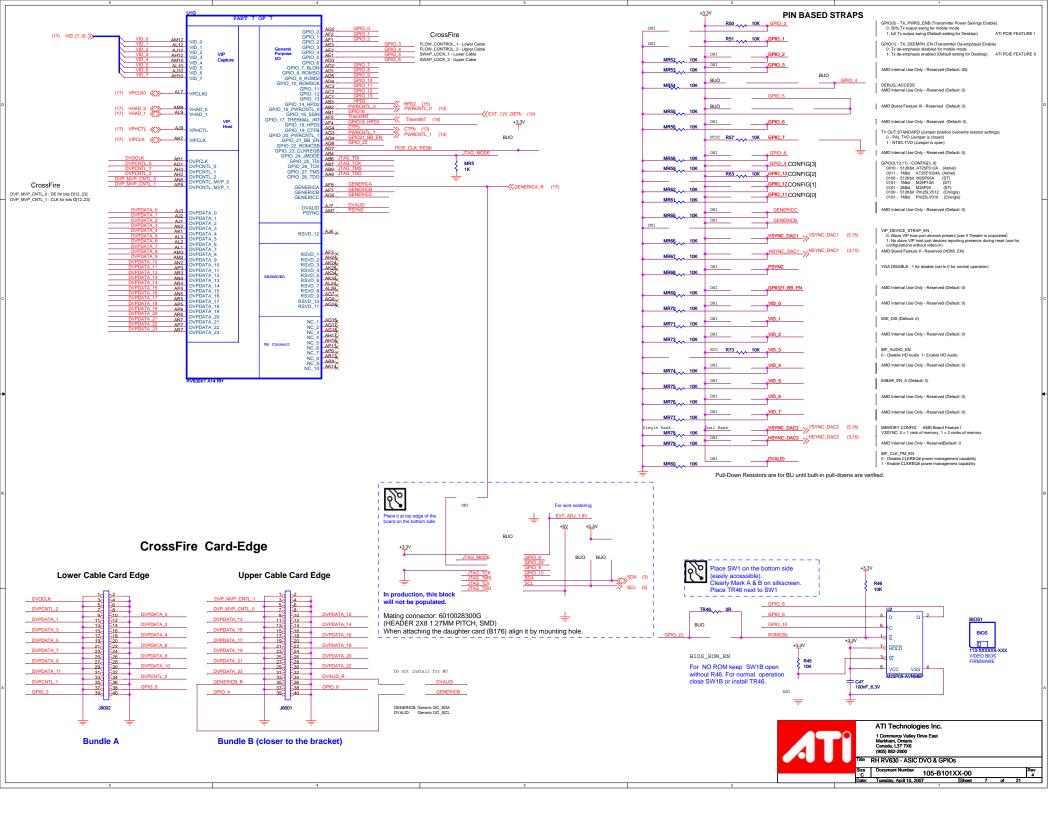


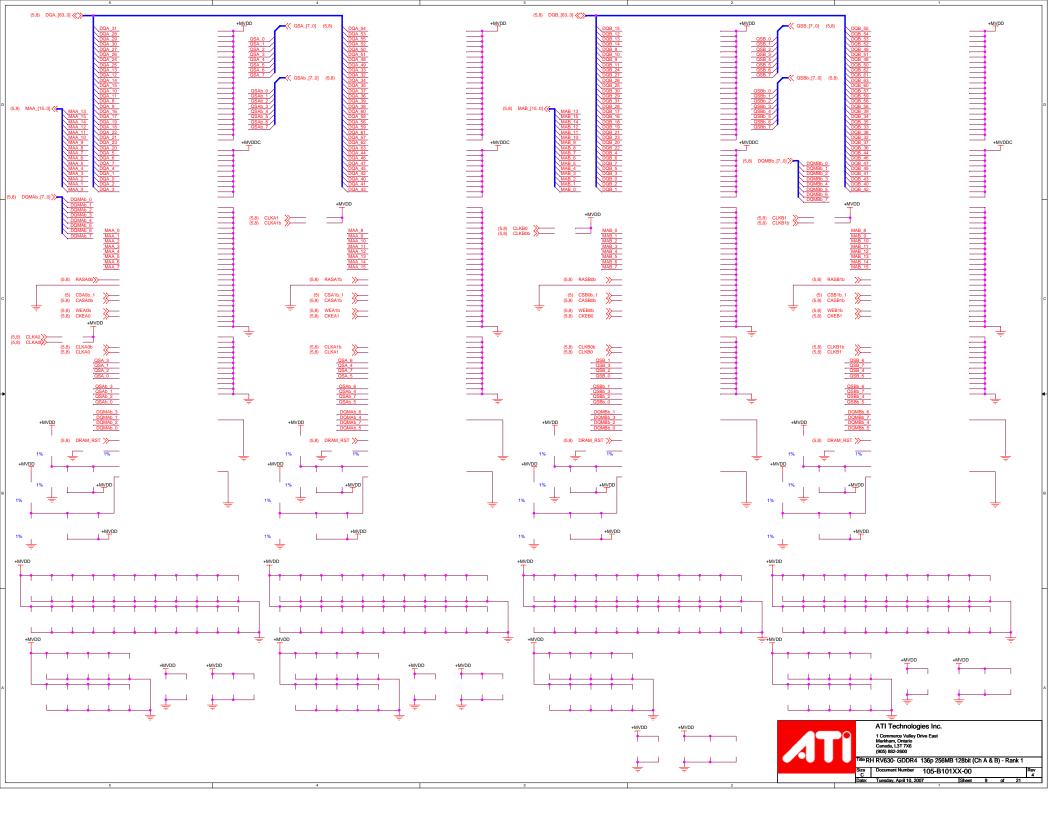


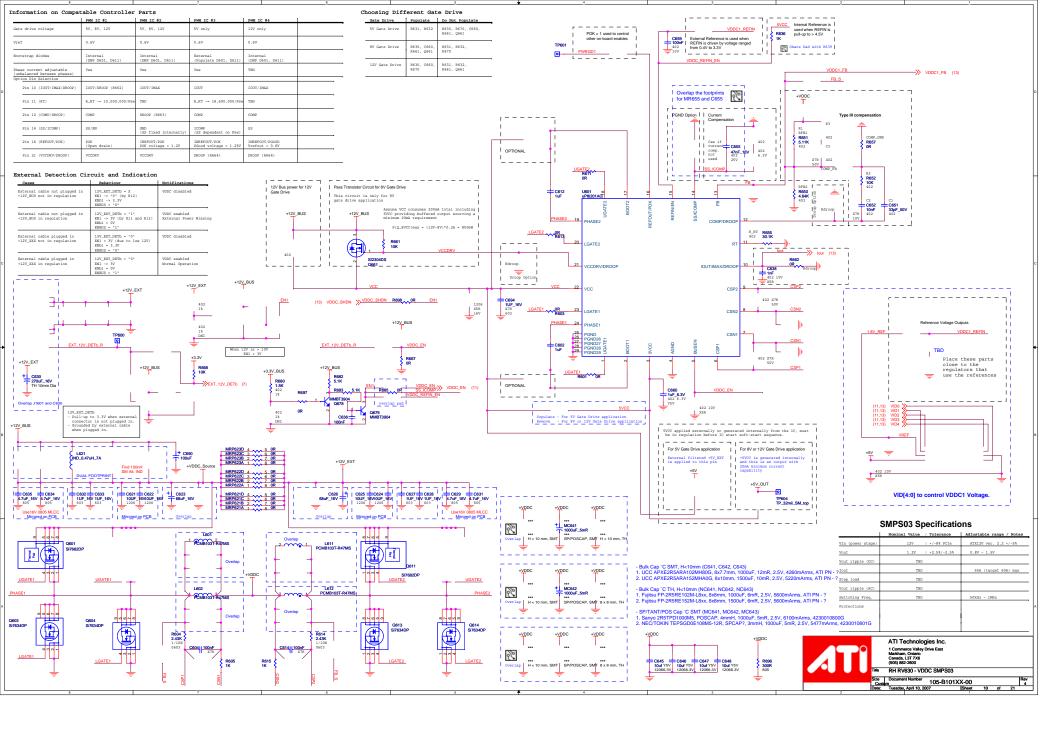


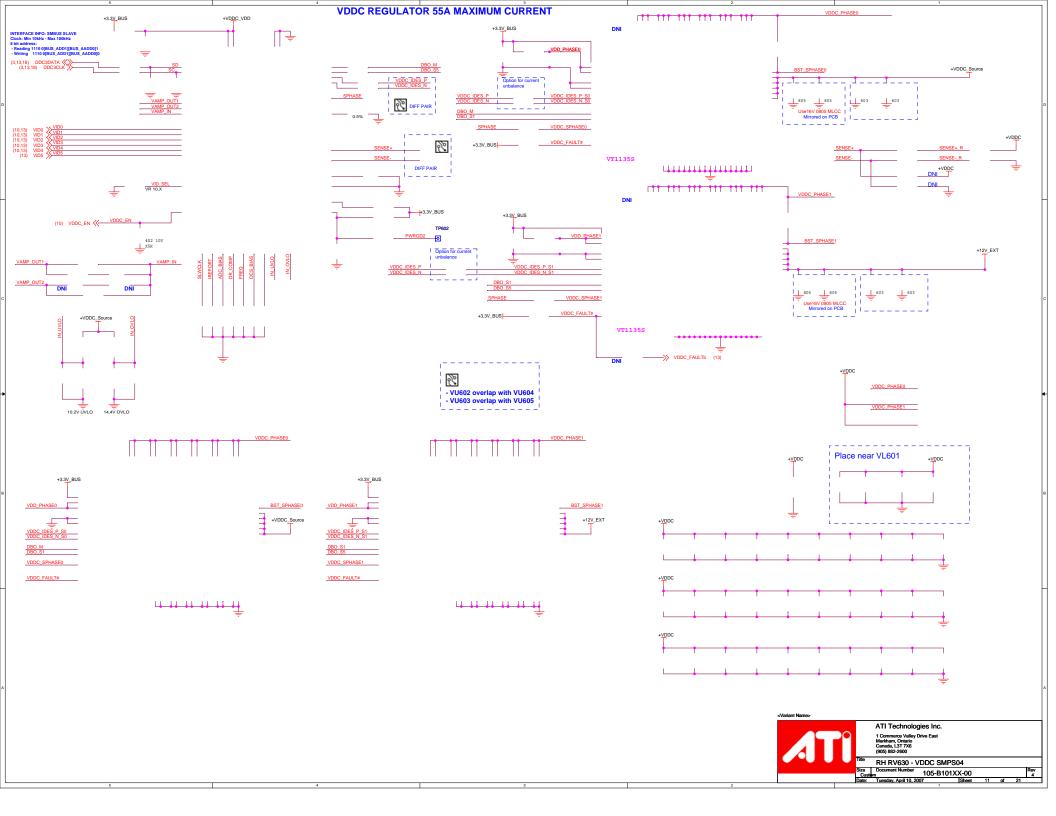


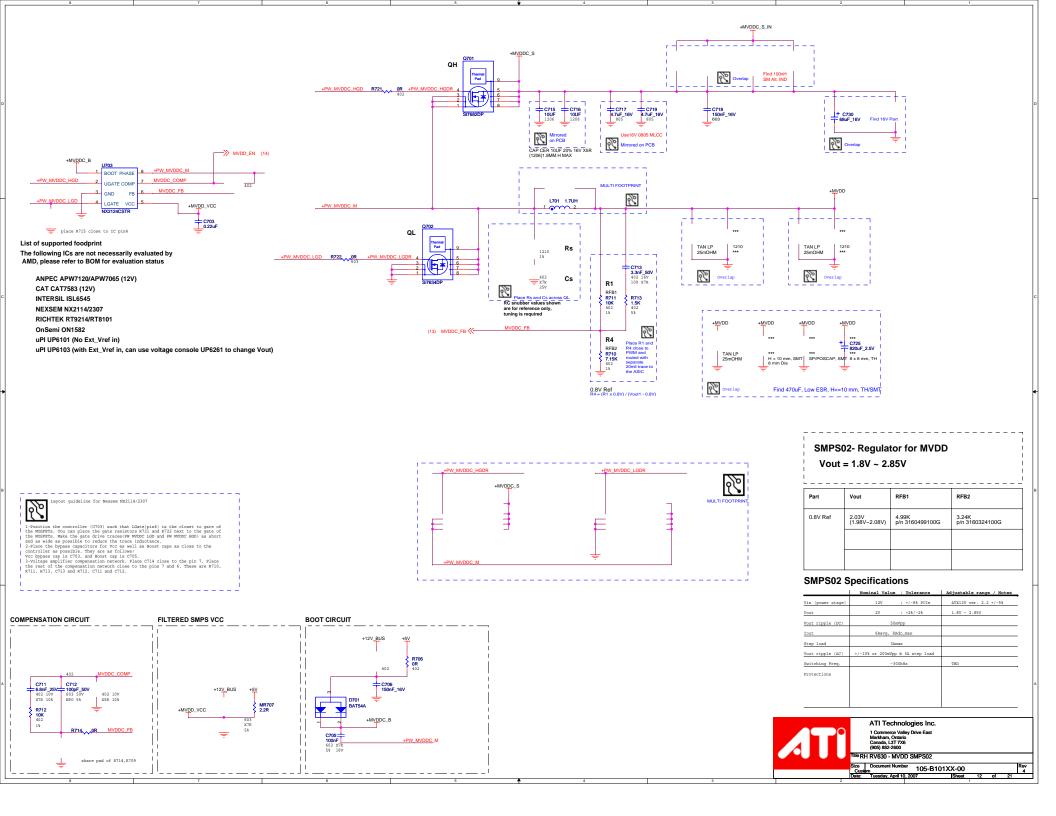


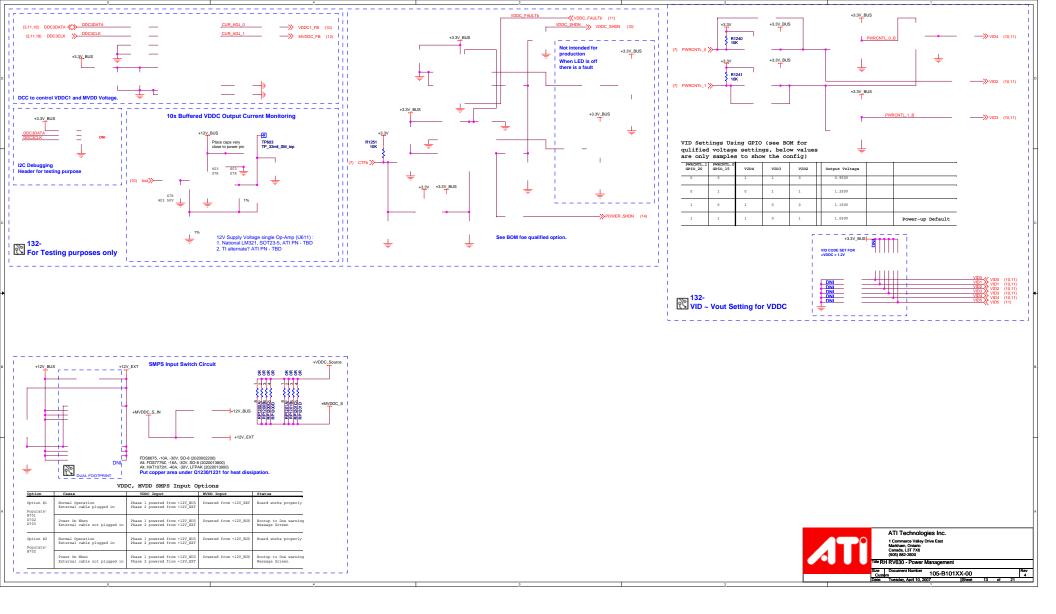


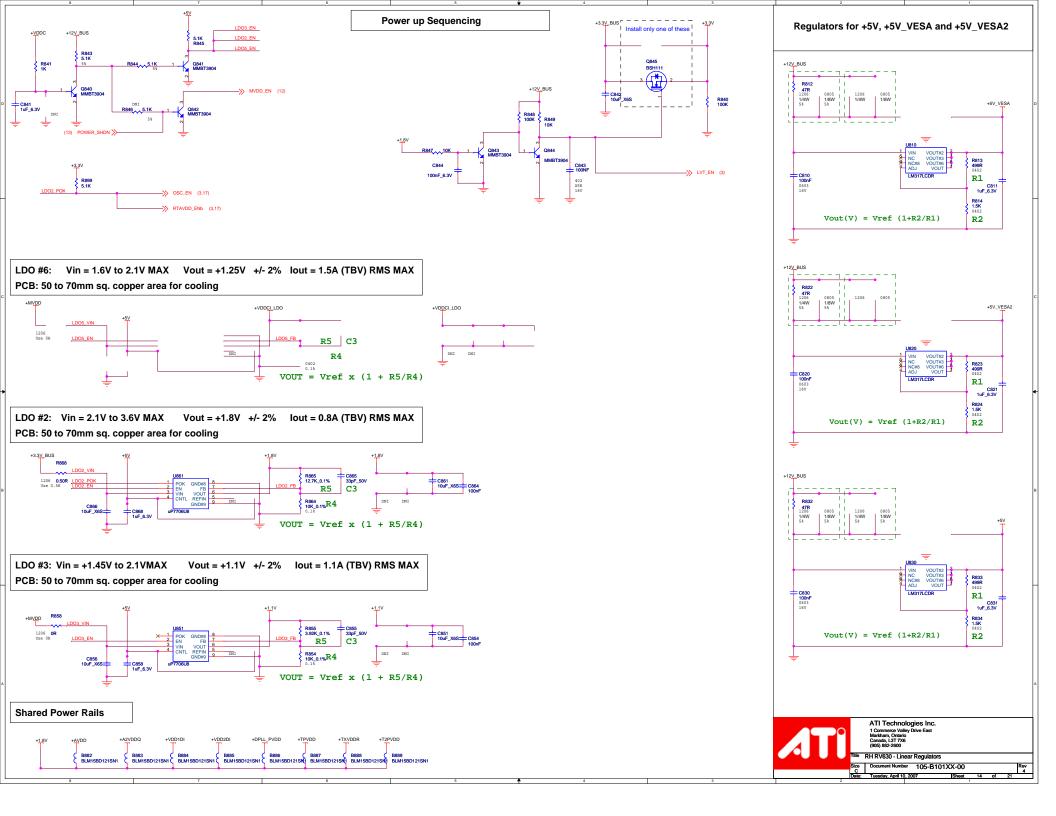


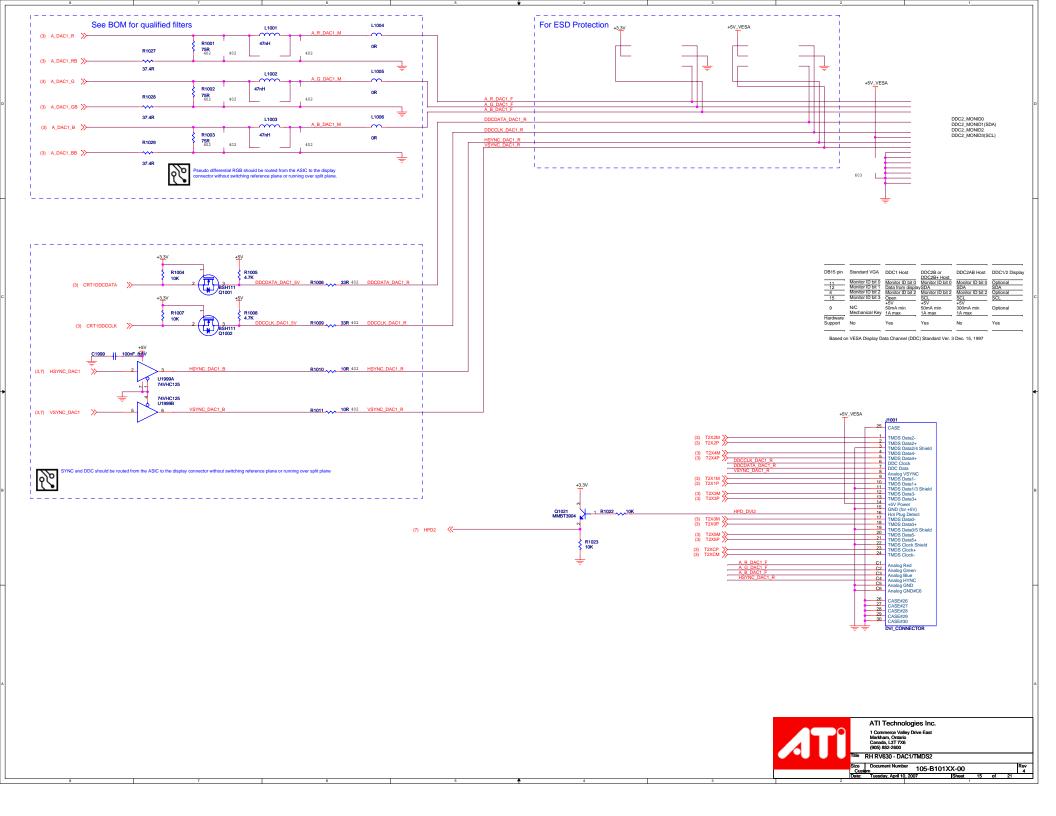


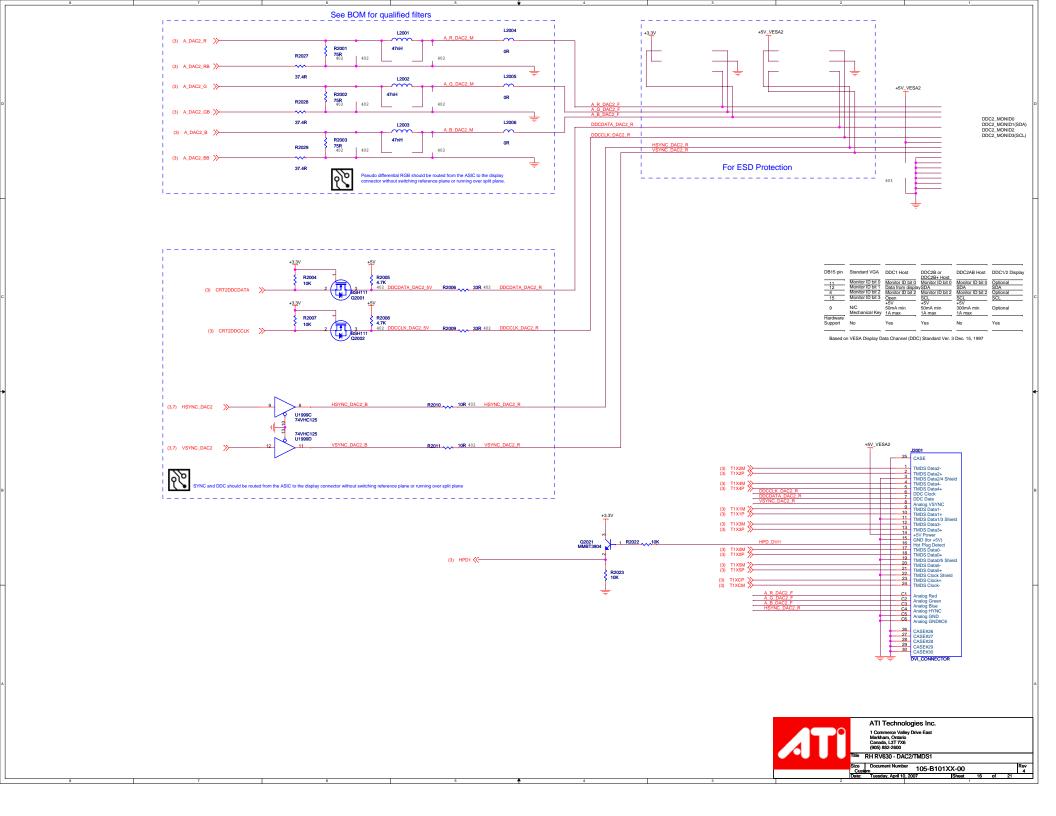


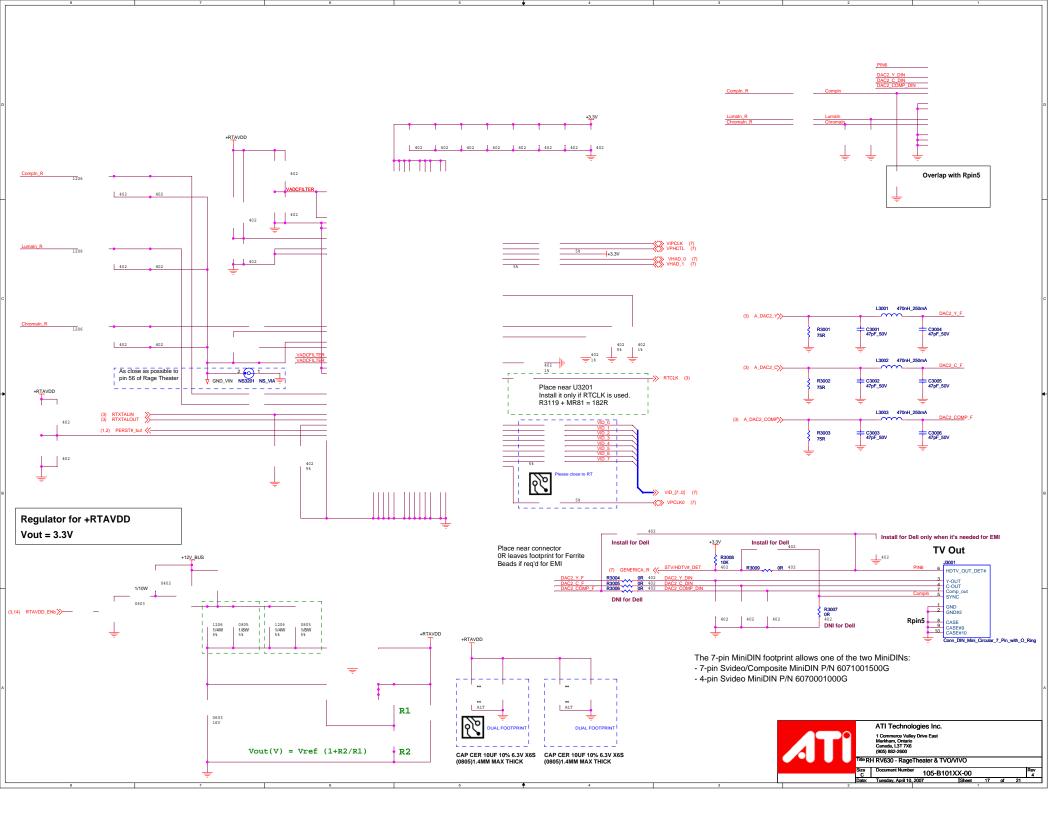


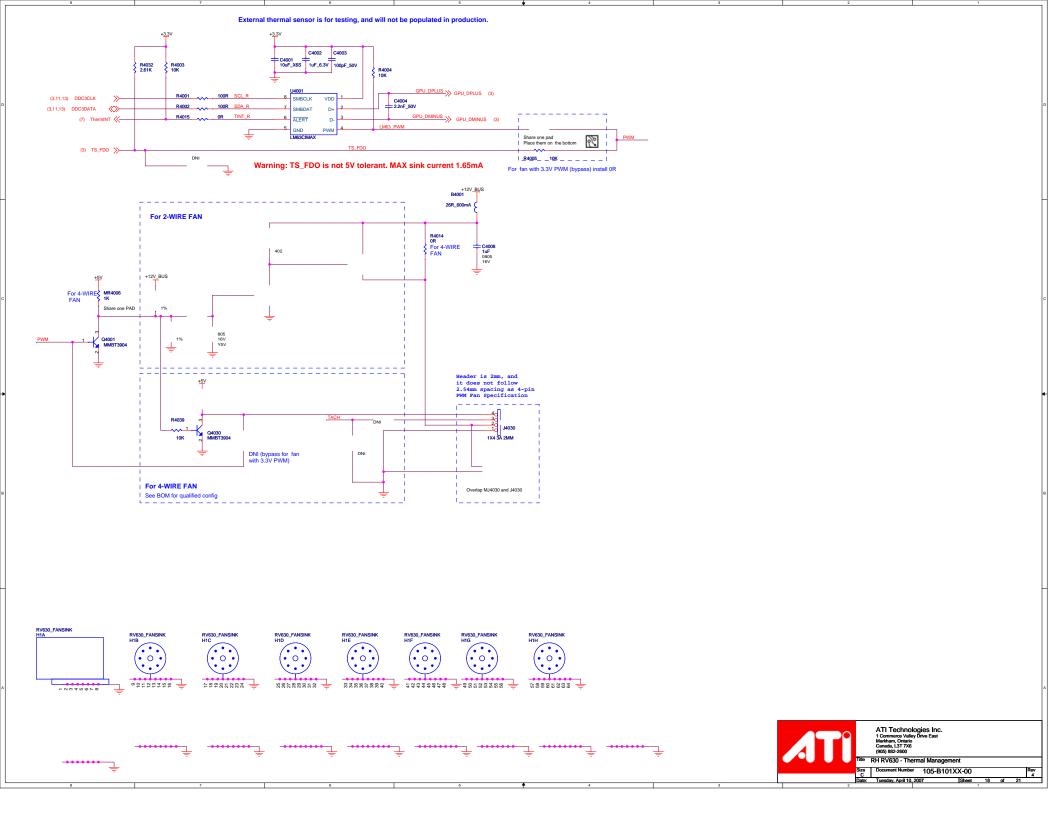


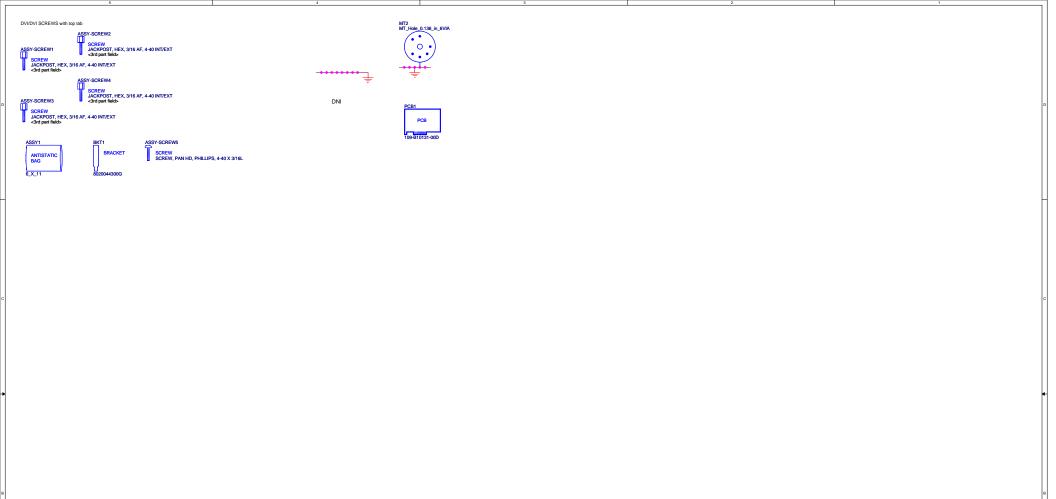












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RH RV630 - Mechanical 105-B101XX-00 007 Sheet

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ATI			Po	Title RH PCIE RV630 2x256MB GDDR4 DUAL DL-DVI-I VIVO) FH	Schematic No. 105-B101XX-00	Date: Tuesday, April 10, 2	ite: esday, April 10, 2007	
D _			JU	REVISION HISTORY NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's,) please consult the product specific BOM. Please contact ATI representative to obtain latest BOM closest to the application desired.							Rev 4
	Sch Rev	PCB Rev	Date	REVISION DESCRIPTION							
	0	A00	06/11/08	Initial design for RV630 pipe cleaner							
	1	00B 06/11/18 Regrouping of parts (Cosmetic) Power-up sequecning updated VID control and EXT detection are updated VDDC SMPS updated									
	2 00C 06/12/08 (pg 05) Re-assignment of MAA_13, MAA_14, MAA_15, MAB_13, MAB_14, and MAB_15 (pg 10) SMPS updated (pg 11) SMPS updated (pg 12) SMPS updated - Adding +5V option (pg 14) Adding R891 (pg 18) Adding Heatsink symbols H1 and H2 (pg 49) Adding MT1 (Layout) Heatsink mounting holes modified and one added.										
+	3	00D	07/02/06	Removing some of test featuers (pg 14) Renaming LDO1 to LDO5 and for connecting to VDDCI if needed (pg 18) Merging 2-wire and 4-wire fan buffer circuitry (pg 3, 4) Adding 10uF caps to VDDRH, VDDCI, T2XVDDR, T2PVDD, and PLL rails (pg 10) Adding buffer for EXT_DETECT line, R1229 and C630 (pg 13) Adding option to control shut down circuitry for critical temperature (pg 14) Removing R891 (pg 7) Adding DIP switch to GPIO7 and GPIO5 (pg 1, 3) Adding TR10 to TR15 to support legacy JTAG for internal testing.							
	4	00	00 03/09/07 Release to production.								
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