MS-V041 VER 30

NV43-PCIE NV43 256MB/128bit, BGA 16MX16 DDR2,VGA,DVI-I,TV-OUT(HT-10)

P295-A00 DESIGN NV43 300/267MHZ 128MB/256MB/512MB DDR2 84-FBGA

PAGE SUMMARY: **DDR2 84-FBGA Clock setting 350MHZ**

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	602-10295-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	602-10295-0000-000	GF-6600-A04 GEN 300/267MHZ 256MB 84-FBGA DDR2 16MX16 VGA+DVI-I+HDTV
2	SKU001	602-10295-0001-000	GF-6600-A04 GEN 300/267MHZ 128MB 84-FBGA DDR2 8MX16 VGA+DVI-I+HDTV
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

REV HISTORY

A00

-08/04/2005:

1.Page18: change power solution to RT9218 for NVVDD & FBVDDQ

10S

-08/04/2005:

1.Page18: Move C913~C916 out form C910,C911 & Move C930,C931 out form C929

2.Page19: Add C940 near C36

3.Page19: Remove C16, C35, C55

B00

-12/06/2005:

1.ADD G73 circuit

C00

-04/26/2006:

1.Remove NV43 reserve circuit

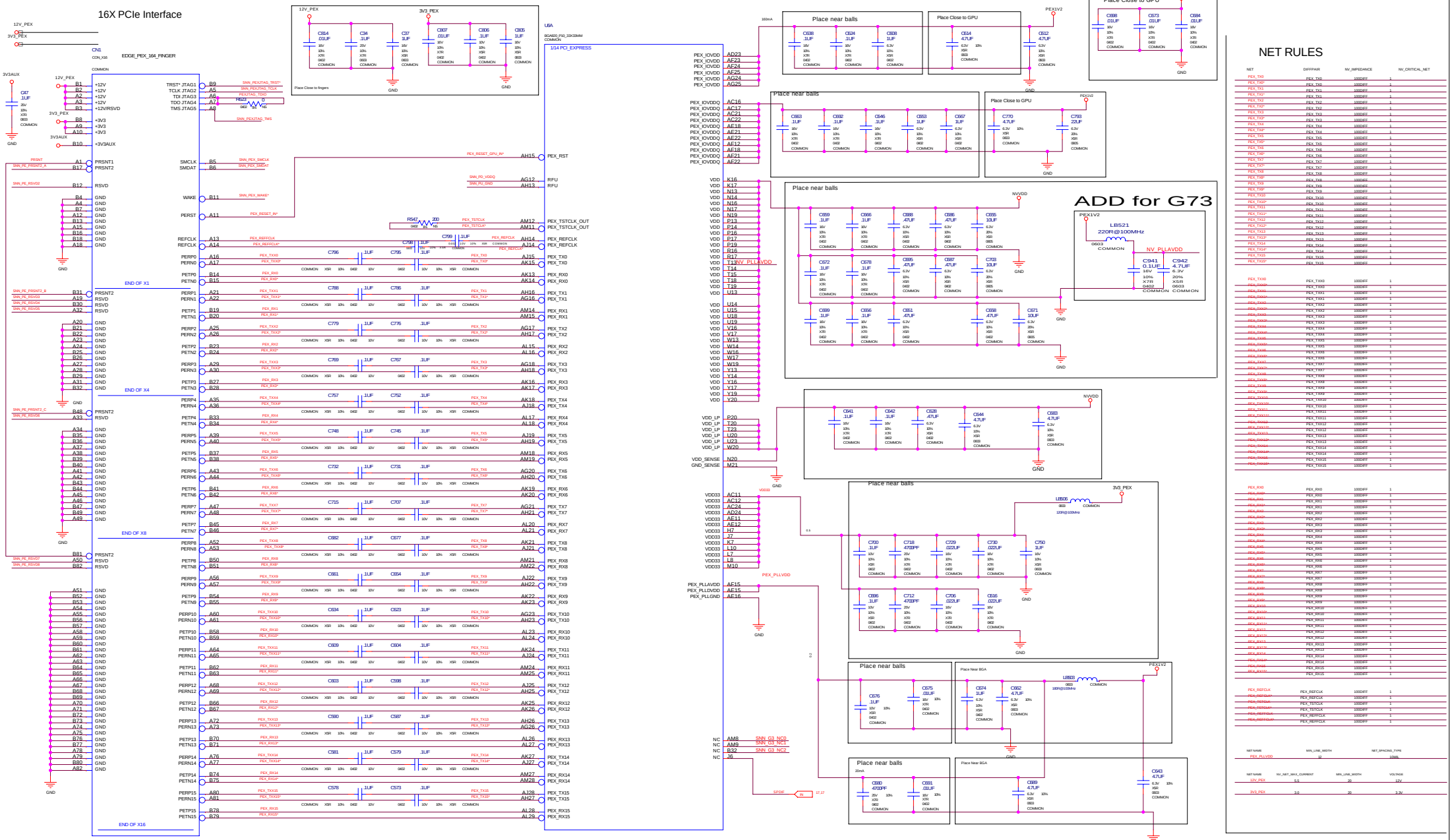
2.Page14: Add SPDIF circuit

3.Page15: Add TMDS Dual_Link A/B

4.Page17: Add MIOA Feature SLI CON

5.Page18,19: Modify Power solution same as P345

02 PCI EXPRESS, NVVDD, VDD33



NET RULES

NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
PEX_TX0	PEX_TX0	100DIFF	1
PEX_TX0*	PEX_TX0	100DIFF	1
PEX_TX1	PEX_TX1	100DIFF	1
PEX_TX1*	PEX_TX1	100DIFF	1
PEX_TX2	PEX_TX2	100DIFF	1
PEX_TX2*	PEX_TX2	100DIFF	1
PEX_TX3	PEX_TX3	100DIFF	1
PEX_TX3*	PEX_TX3	100DIFF	1
PEX_TX4	PEX_TX4	100DIFF	1
PEX_TX4*	PEX_TX4	100DIFF	1
PEX_TX5	PEX_TX5	100DIFF	1
PEX_TX5*	PEX_TX5	100DIFF	1
PEX_TX6	PEX_TX6	100DIFF	1
PEX_TX6*	PEX_TX6	100DIFF	1
PEX_TX7	PEX_TX7	100DIFF	1
PEX_TX7*	PEX_TX7	100DIFF	1
PEX_TX8	PEX_TX8	100DIFF	1
PEX_TX8*	PEX_TX8	100DIFF	1
PEX_TX9	PEX_TX9	100DIFF	1
PEX_TX9*	PEX_TX9	100DIFF	1
PEX_TX10	PEX_TX10	100DIFF	1
PEX_TX10*	PEX_TX10	100DIFF	1
PEX_TX11	PEX_TX11	100DIFF	1
PEX_TX11*	PEX_TX11	100DIFF	1
PEX_TX12	PEX_TX12	100DIFF	1
PEX_TX12*	PEX_TX12	100DIFF	1
PEX_TX13	PEX_TX13	100DIFF	1
PEX_TX13*	PEX_TX13	100DIFF	1
PEX_TX14	PEX_TX14	100DIFF	1
PEX_TX14*	PEX_TX14	100DIFF	1
PEX_TX15	PEX_TX15	100DIFF	1
PEX_TX15*	PEX_TX15	100DIFF	1
PEX_TX0	PEX_TX0	100DIFF	1
PEX_TX0*	PEX_TX0	100DIFF	1
PEX_TX1	PEX_TX1	100DIFF	1
PEX_TX1*	PEX_TX1	100DIFF	1
PEX_TX2	PEX_TX2	100DIFF	1
PEX_TX2*	PEX_TX2	100DIFF	1
PEX_TX3	PEX_TX3	100DIFF	1
PEX_TX3*	PEX_TX3	100DIFF	1
PEX_TX4	PEX_TX4	100DIFF	1
PEX_TX4*	PEX_TX4	100DIFF	1
PEX_TX5	PEX_TX5	100DIFF	1
PEX_TX5*	PEX_TX5	100DIFF	1
PEX_TX6	PEX_TX6	100DIFF	1
PEX_TX6*	PEX_TX6	100DIFF	1
PEX_TX7	PEX_TX7	100DIFF	1
PEX_TX7*	PEX_TX7	100DIFF	1
PEX_TX8	PEX_TX8	100DIFF	1
PEX_TX8*	PEX_TX8	100DIFF	1
PEX_TX9	PEX_TX9	100DIFF	1
PEX_TX9*	PEX_TX9	100DIFF	1
PEX_TX10	PEX_TX10	100DIFF	1
PEX_TX10*	PEX_TX10	100DIFF	1
PEX_TX11	PEX_TX11	100DIFF	1
PEX_TX11*	PEX_TX11	100DIFF	1
PEX_TX12	PEX_TX12	100DIFF	1
PEX_TX12*	PEX_TX12	100DIFF	1
PEX_TX13	PEX_TX13	100DIFF	1
PEX_TX13*	PEX_TX13	100DIFF	1
PEX_TX14	PEX_TX14	100DIFF	1
PEX_TX14*	PEX_TX14	100DIFF	1
PEX_TX15	PEX_TX15	100DIFF	1
PEX_TX15*	PEX_TX15	100DIFF	1
PEX_RX0	PEX_RX0	100DIFF	1
PEX_RX0*	PEX_RX0	100DIFF	1
PEX_RX1	PEX_RX1	100DIFF	1
PEX_RX1*	PEX_RX1	100DIFF	1
PEX_RX2	PEX_RX2	100DIFF	1
PEX_RX2*	PEX_RX2	100DIFF	1
PEX_RX3	PEX_RX3	100DIFF	1
PEX_RX3*	PEX_RX3	100DIFF	1
PEX_RX4	PEX_RX4	100DIFF	1
PEX_RX4*	PEX_RX4	100DIFF	1
PEX_RX5	PEX_RX5	100DIFF	1
PEX_RX5*	PEX_RX5	100DIFF	1
PEX_RX6	PEX_RX6	100DIFF	1
PEX_RX6*	PEX_RX6	100DIFF	1
PEX_RX7	PEX_RX7	100DIFF	1
PEX_RX7*	PEX_RX7	100DIFF	1
PEX_RX8	PEX_RX8	100DIFF	1
PEX_RX8*	PEX_RX8	100DIFF	1
PEX_RX9	PEX_RX9	100DIFF	1
PEX_RX9*	PEX_RX9	100DIFF	1
PEX_RX10	PEX_RX10	100DIFF	1
PEX_RX10*	PEX_RX10	100DIFF	1
PEX_RX11	PEX_RX11	100DIFF	1
PEX_RX11*	PEX_RX11	100DIFF	1
PEX_RX12	PEX_RX12	100DIFF	1
PEX_RX12*	PEX_RX12	100DIFF	1
PEX_RX13	PEX_RX13	100DIFF	1
PEX_RX13*	PEX_RX13	100DIFF	1
PEX_RX14	PEX_RX14	100DIFF	1
PEX_RX14*	PEX_RX14	100DIFF	1
PEX_RX15	PEX_RX15	100DIFF	1
PEX_RX15*	PEX_RX15	100DIFF	1
PEX_REFCLK	PEX_REFCLK	100DIFF	1
PEX_REFCLK*	PEX_REFCLK	100DIFF	1
PEX_TSTCLK	PEX_TSTCLK	100DIFF	1
PEX_TSTCLK*	PEX_TSTCLK	100DIFF	1
PEX_REFCLK	PEX_REFCLK	100DIFF	1
PEX_REFCLK*	PEX_REFCLK	100DIFF	1

NET NAME	MIN_LINE_WIDTH	NET_SPACING_TYPE
PEX_PLLVDD	12	10MIL

NET NAME	NV_NET_MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
12V_PEX	5.5	20	12V
3V3_PEX	3.0	20	3.3V

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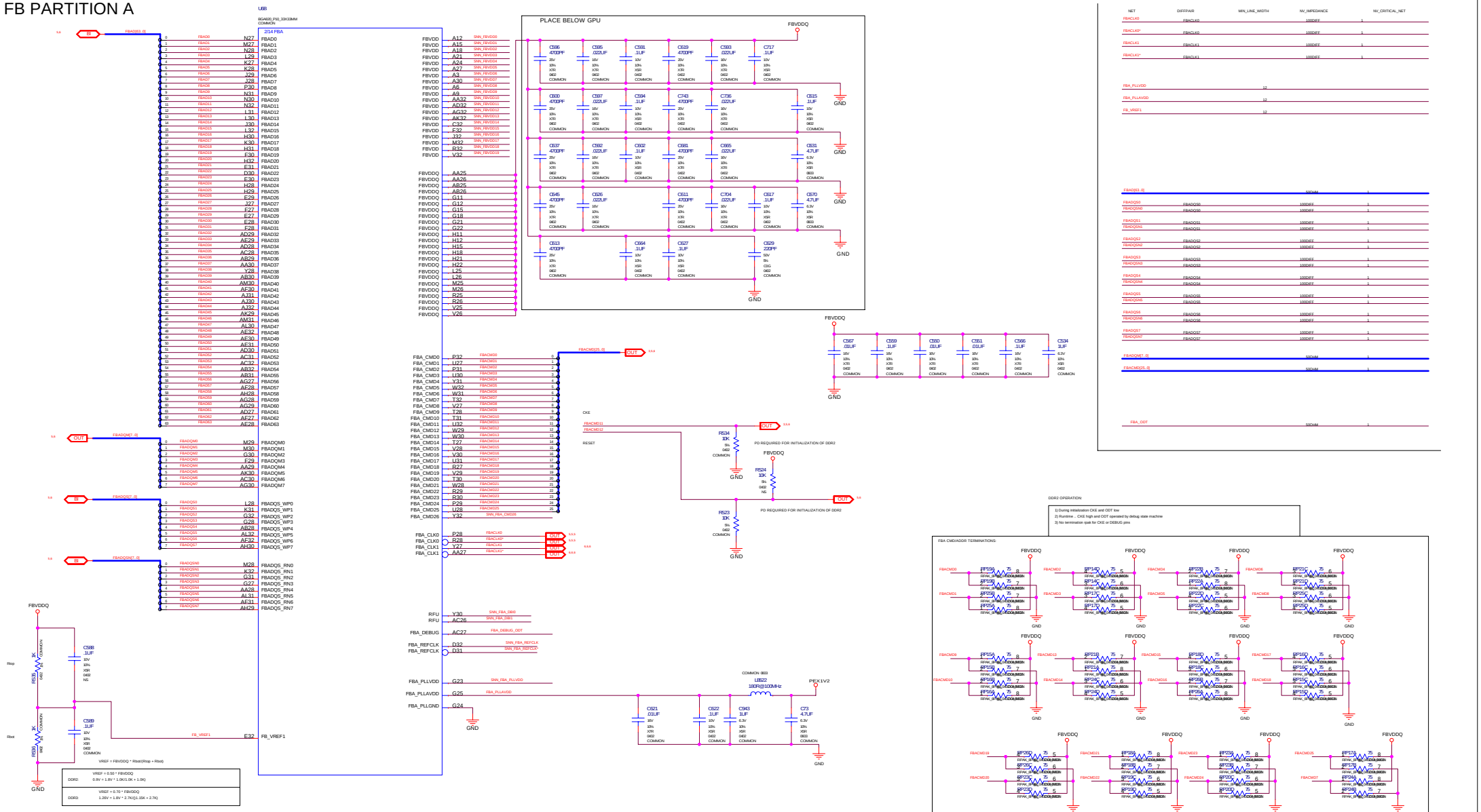
03 FB BANK A, FBVDDQ DECOUPLING

FB PARTITION A



NET	DIFFPAIR	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
FBACLK0	FBACLK0		100DIFF	1
FBACLK0*	FBACLK0		100DIFF	1
FBACLK1	FBACLK1		100DIFF	1
FBACLK1*	FBACLK1		100DIFF	1
FBA_PLLVDD		12		
FBA_PLLAVDD		12		
FB_VREF1		12		
FBADQS3..0]			50OHM	1
FBADQS0	FBADQS0		100DIFF	1
FBADQSN0	FBADQS0		100DIFF	1
FBADQS1	FBADQS1		100DIFF	1
FBADQSN1	FBADQS1		100DIFF	1
FBADQS2	FBADQS2		100DIFF	1
FBADQSN2	FBADQS2		100DIFF	1
FBADQS3	FBADQS3		100DIFF	1
FBADQSN3	FBADQS3		100DIFF	1
FBADQS4	FBADQS4		100DIFF	1
FBADQSN4	FBADQS4		100DIFF	1
FBADQS5	FBADQS5		100DIFF	1
FBADQSN5	FBADQS5		100DIFF	1
FBADQS6	FBADQS6		100DIFF	1
FBADQSN6	FBADQS6		100DIFF	1
FBADQS7	FBADQS7		100DIFF	1
FBADQSN7	FBADQS7		100DIFF	1
FBADQM7..0]			50OHM	1
FBACMD25..0]			50OHM	1
FBA_ODT			50OHM	1

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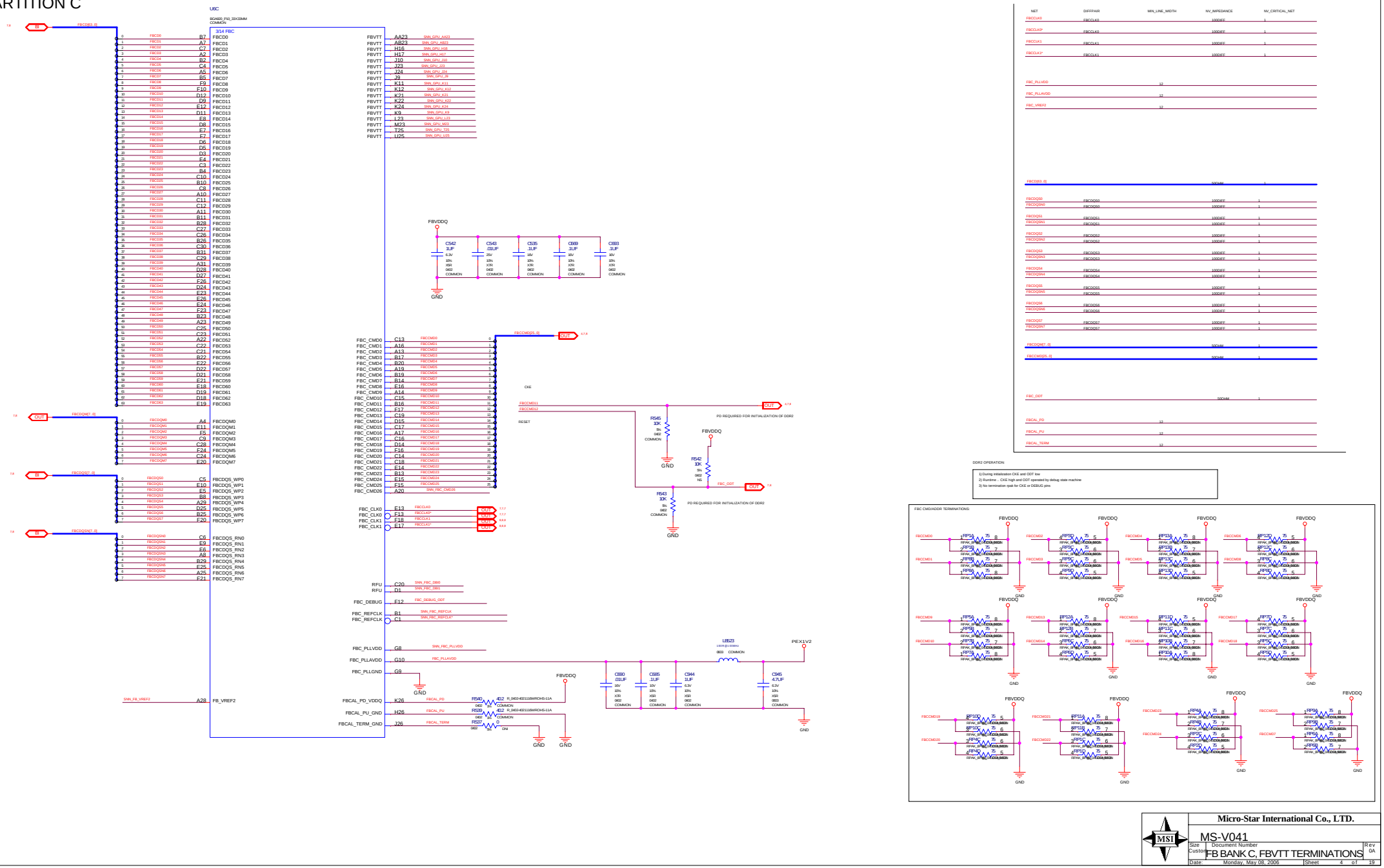
04 FB BANK C, FBVTT TERMINATIONS

FB PARTITION C



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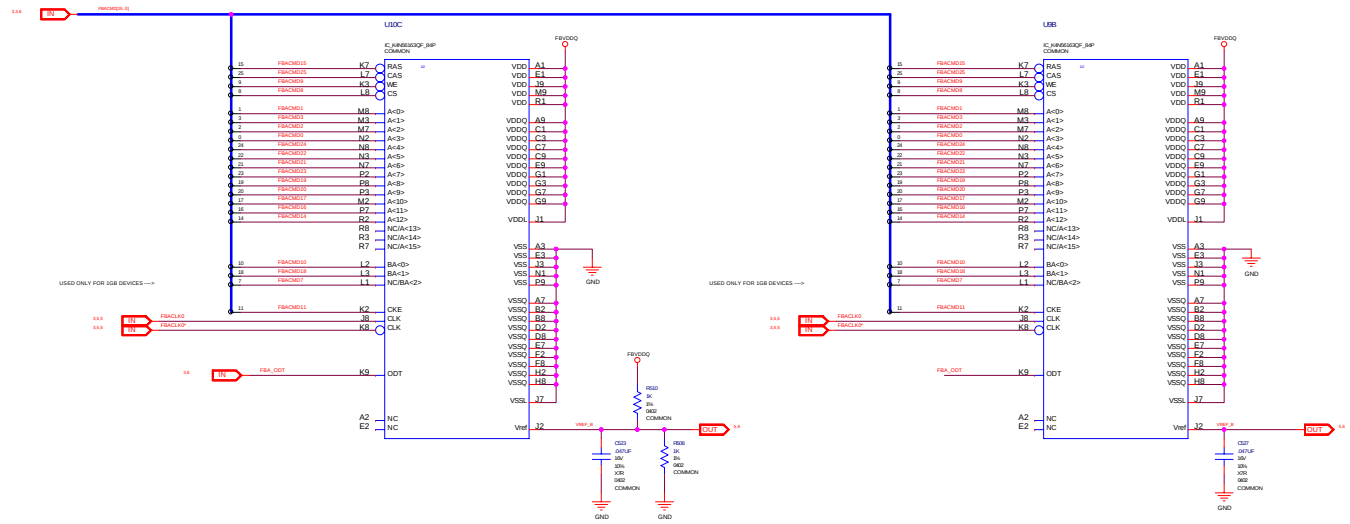
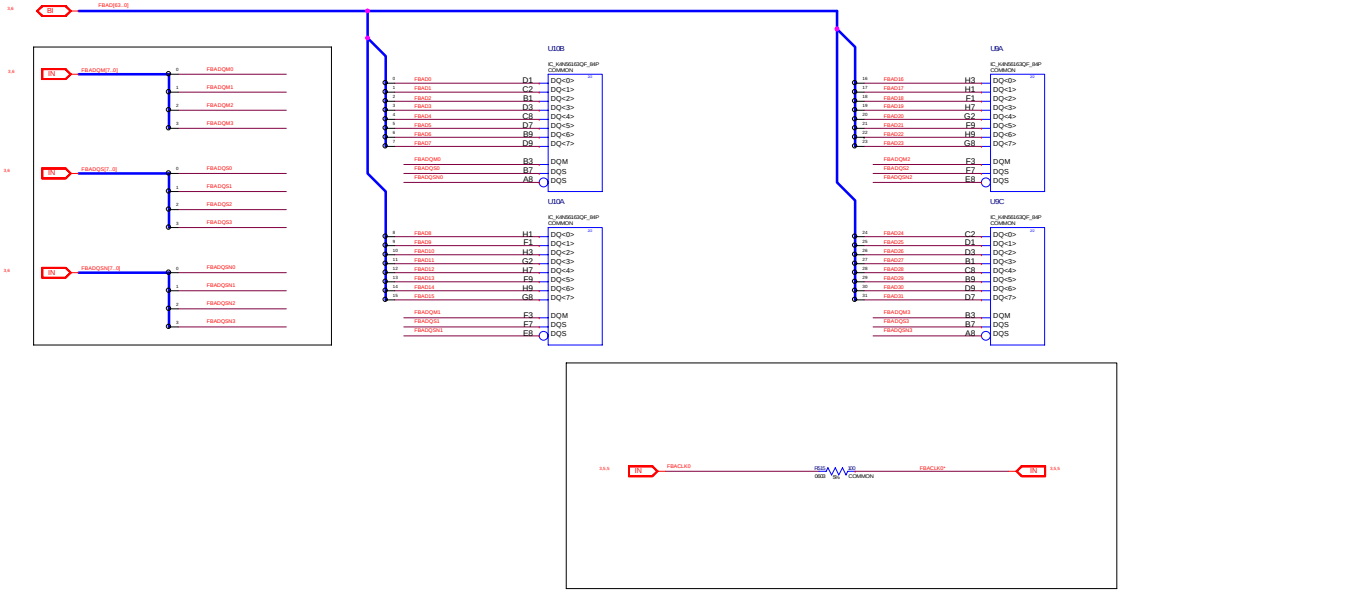
05 MEMORY PARTITION A 0..31

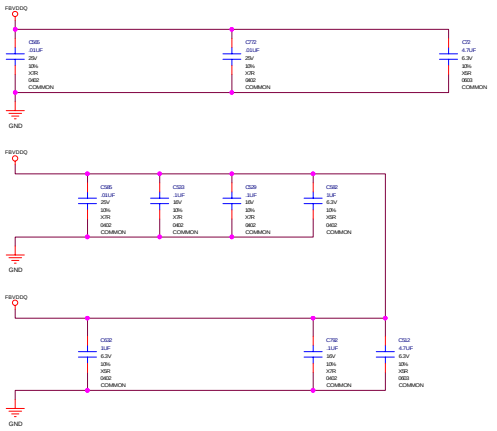
FBA MEMORY 1st bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY





16x power/gnd pin pairs per mem
3x 0.022uF - 5.3 to 1
6x 4700uF - 2.7 to 1
5x 220pF - 3.2 to 1
2x 0.047uF - 8 to 1
2x 4.7uF - 8 to 1



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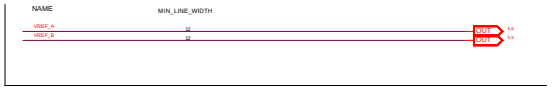
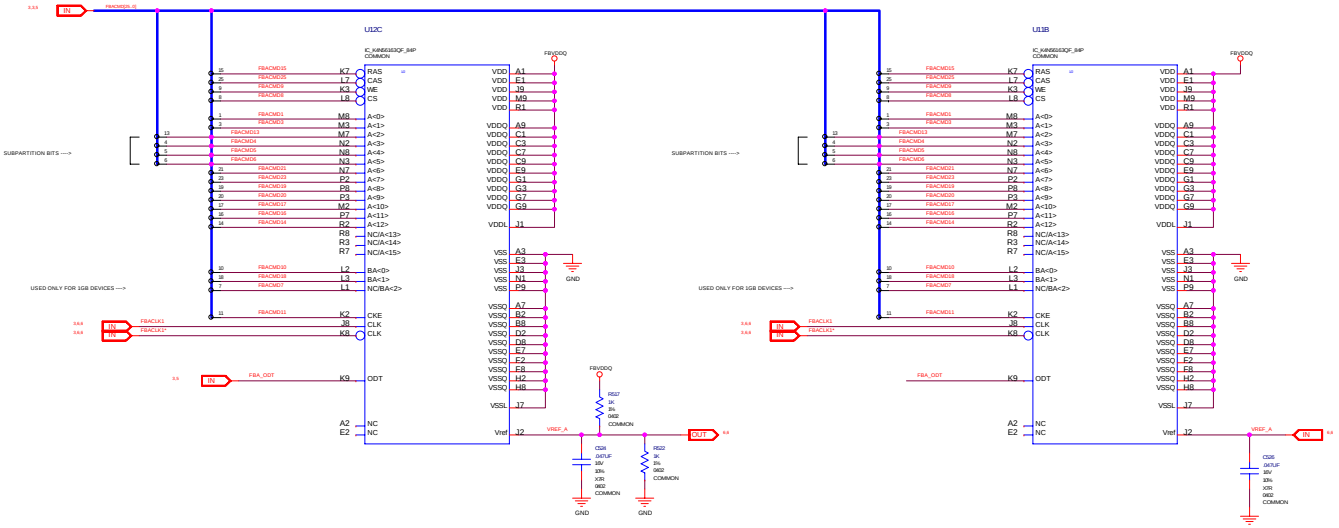
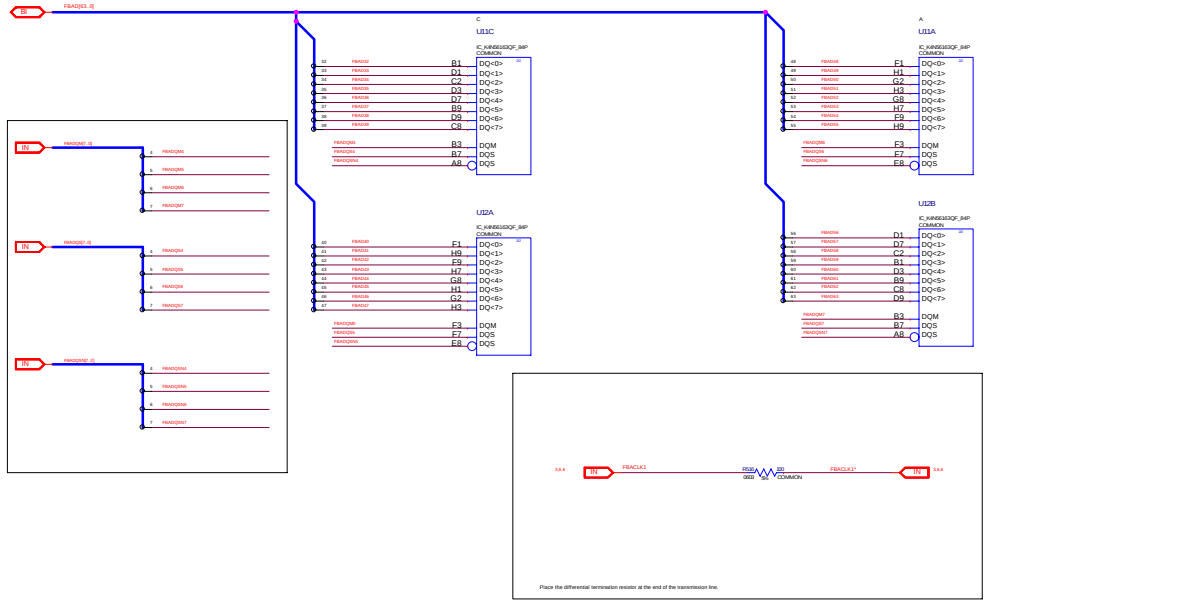
06 MEMORY PARTITION A 32..63

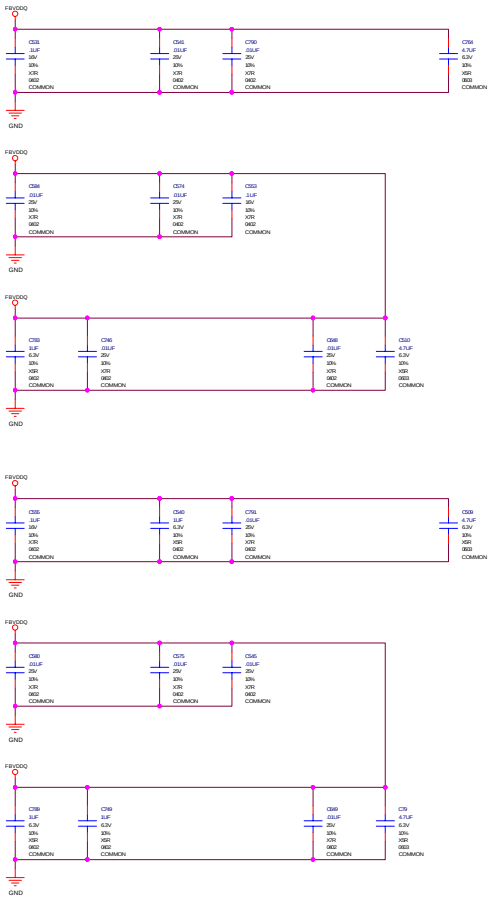
FBA MEMORY 1st bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY









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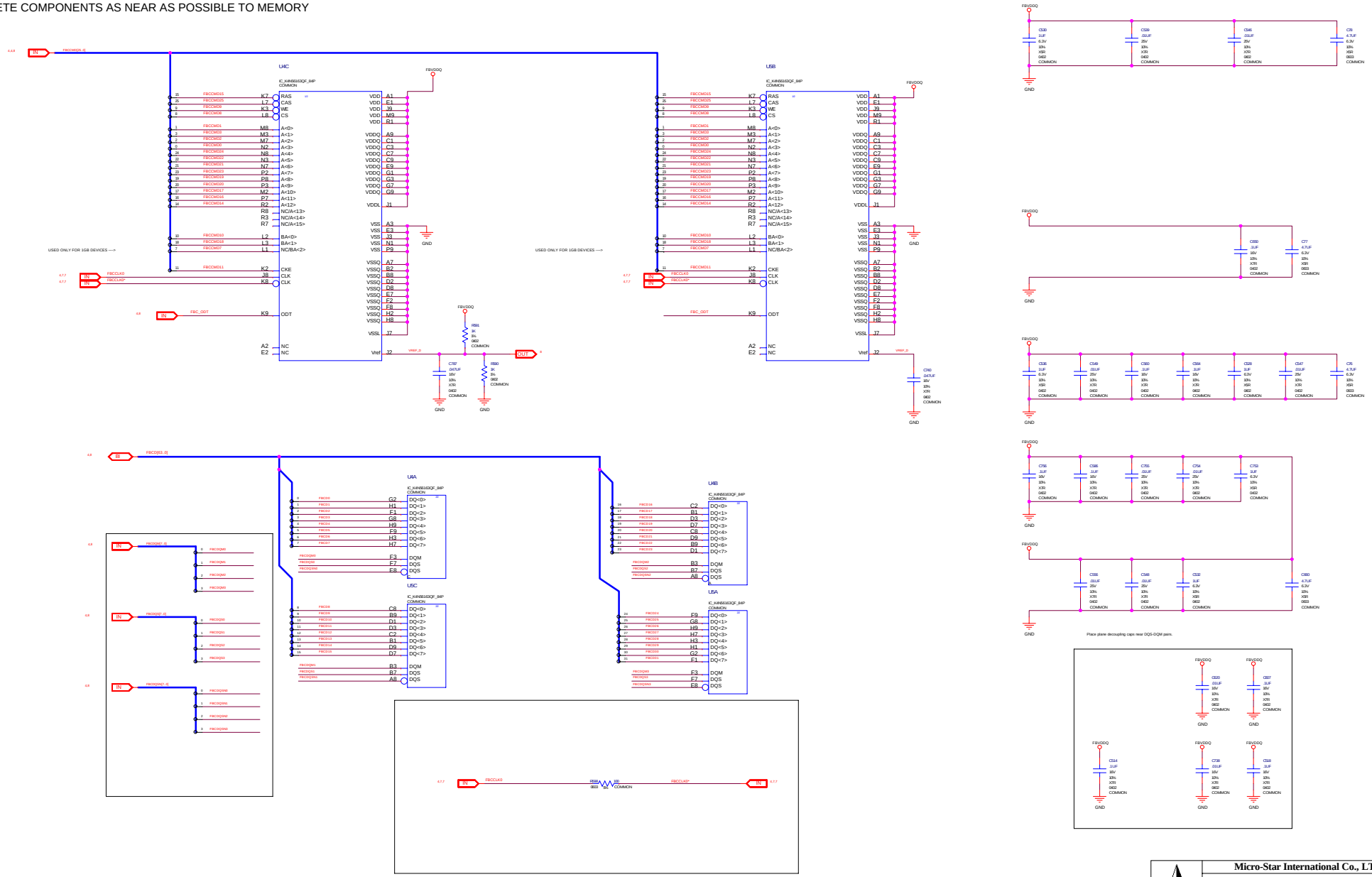
07 MEMORY PARTITION C 0..31

FBC MEMORY 2nd bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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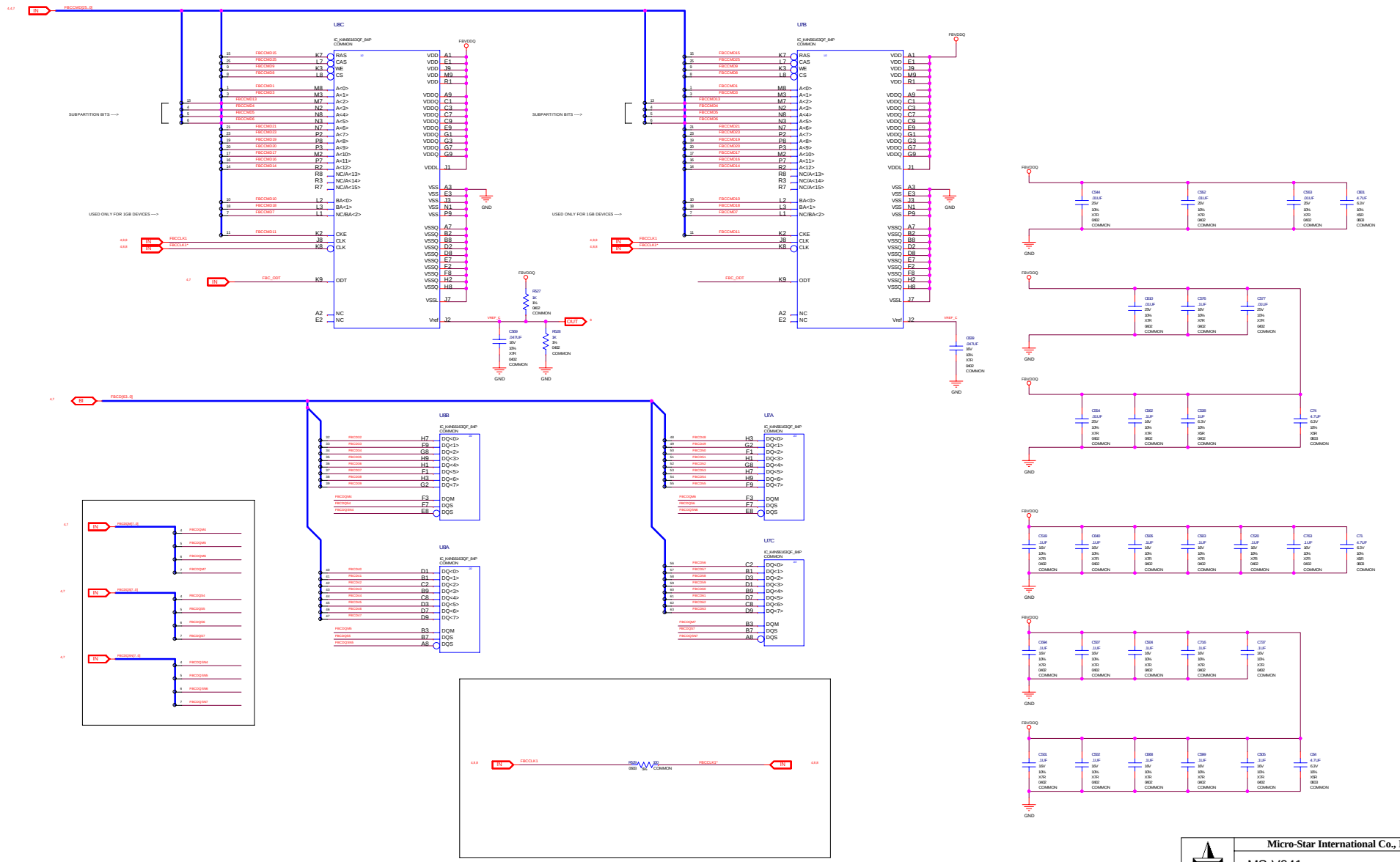
08 MEMORY PARTITION C 32..63

FBC MEMORY 2nd bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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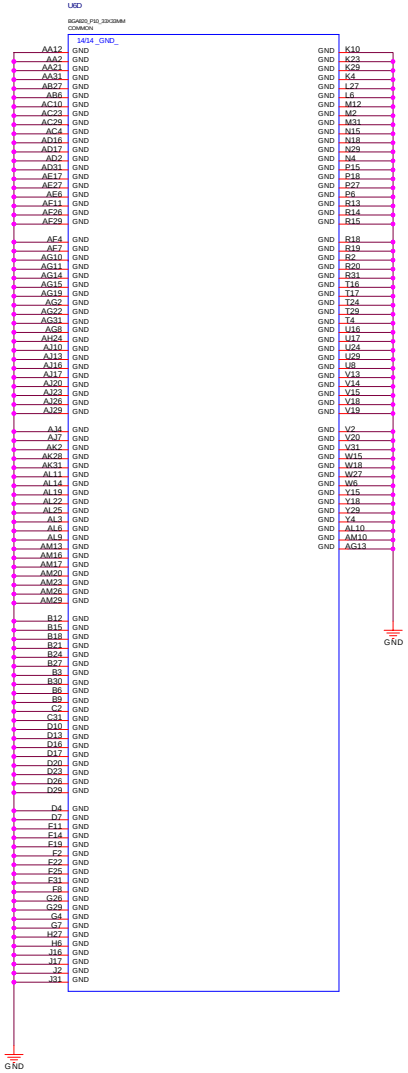
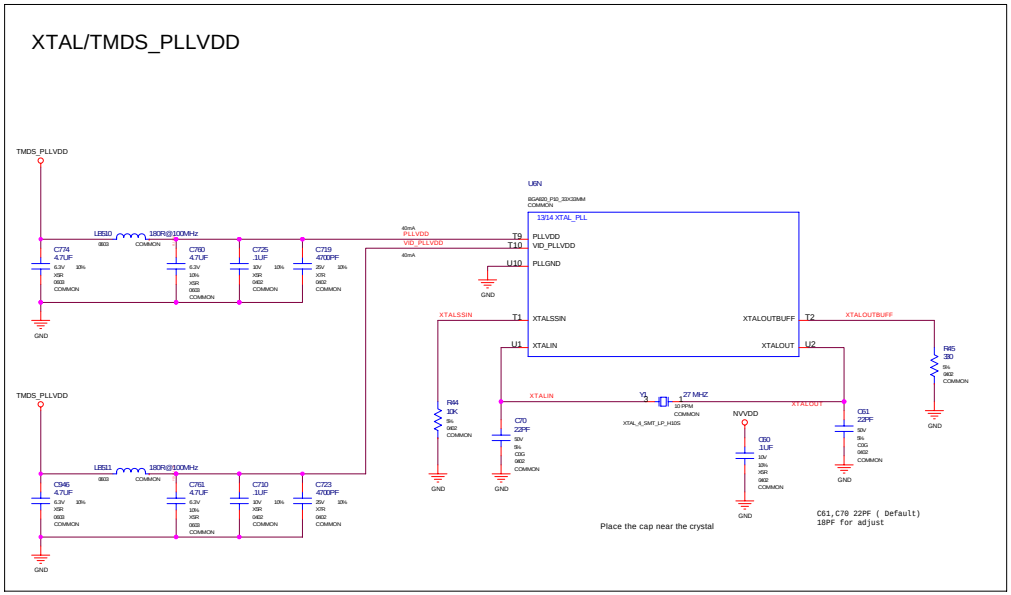
09 GPU GND / TMDS_PLLVDD





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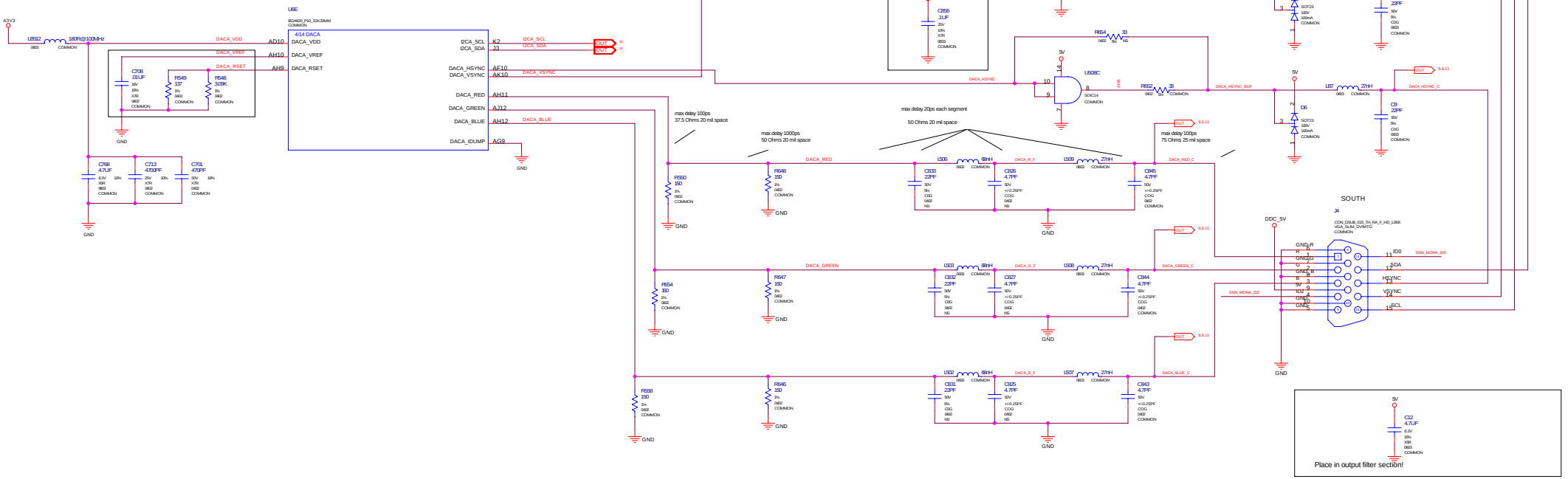
10 DACA - VGA

NET_NAME	MIN_LINE_WIDTH	NV_CRITICAL_NET	NV_IMPEDANCE
I2CA_SCL			
I2CA_SDA			
DACA_HSYNC		2	50OHM
DACA_VSYNC		2	50OHM
DACA_HSYNC_BUF		2	50OHM
DACA_VSYNC_BUF		2	50OHM
DACA_VSYNC_C		2	50OHM
DACA_HSYNC_C		2	50OHM
AVB		2	50OHM
A VB		2	50OHM
DACA_RED		1	50OHM
DACA_GREEN		1	50OHM
DACA_BLUE		1	50OHM
DACA_G_F		1	50OHM
DACA_R_F		1	50OHM
DACA_RED_C		1	50OHM
DACA_GREEN_C		1	50OHM
DACA_BLUE_C		1	50OHM
DACA_VDD	12		
DACA_VREF	12		
DACA_RSET	12		

Note that this impedance is the highest one on the x-net for a 4-layer stackup

Change for G73

C708 0.1u
R549 124ohm
R548 1.78Kohm



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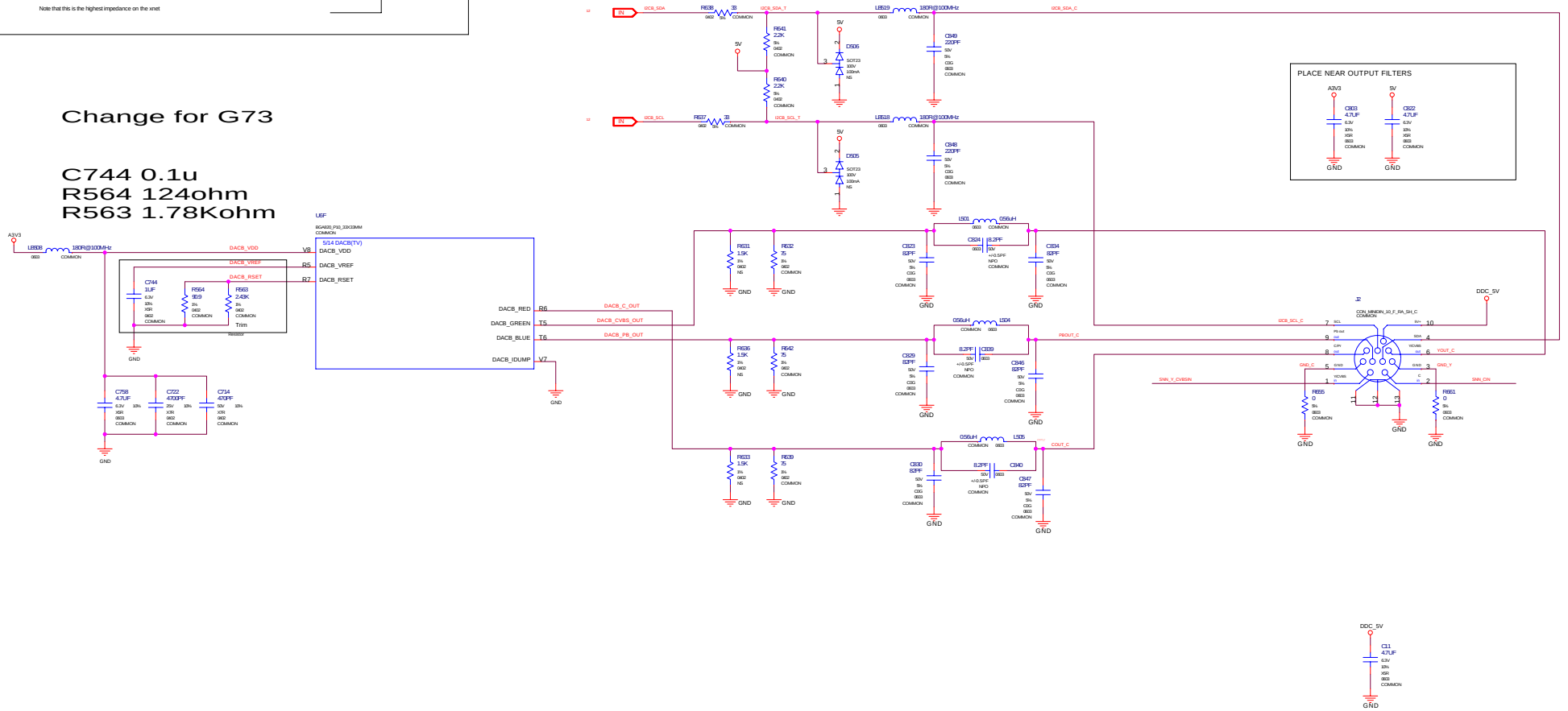
11 DACB - TVOUT, VIDEO IN

NET_NAME	MIN_LINE_WIDTH	NV_CRITICAL_NET	NV_IMPEDANCE
DACB_C_OUT		1	56OHM
DACB_CVBS_OUT		1	56OHM
DACB_PB_OUT		1	56OHM
COUT_C		1	56OHM
YOUT_C		1	56OHM
PBOUT_C		1	56OHM
DACB_VDD	12		
DACB_VREF	12		
DACB_RSET	12		
TVRSET	12		
GND_C	12		
GND_Y	12		

Note that this is the highest impedance on the xnet

Change for G73

C744 0.1u
R564 124ohm
R563 1.78Kohm



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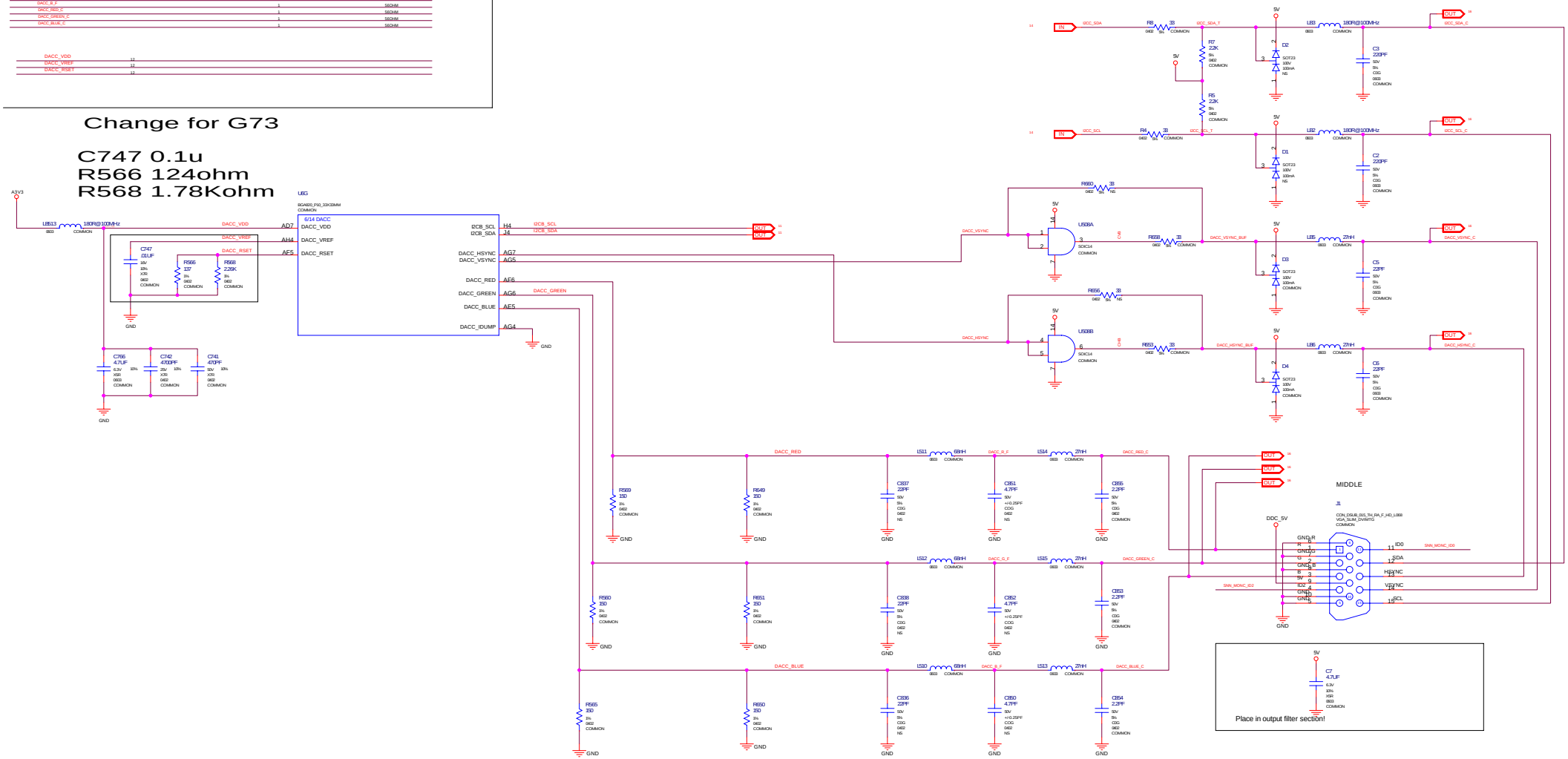
12 DACC - VGA

NET_NAME	MIN_LINE_WIDTH	NET_SPACING_RULE	NV_CRITICAL_NET	NV_IMPEDANCE
I2CB_SCL				
I2CB_SDA				
DACC_HSYNC		2		50OHM
DACC_VSYNC		2		50OHM
DACC_HSYNC_BUF		2		50OHM
DACC_VSYNC_BUF		2		50OHM
DACC_VSYNC_C		2		50OHM
DACC_HSYNC_C		2		50OHM
CHB		2		50OHM
CVB		2		50OHM
DACC_RED		1		50OHM
DACC_GREEN		1		50OHM
DACC_BLUE		1		50OHM
DACC_R_F		1		50OHM
DACC_G_F		1		50OHM
DACC_B_F		1		50OHM
DACC_RED_C		1		50OHM
DACC_GREEN_C		1		50OHM
DACC_BLUE_C		1		50OHM
DACC_VDD		12		
DACC_VREF		12		
DACC_RSET		12		

Change for G73

C747 0.1u
R566 124ohm
R568 1.78Kohm



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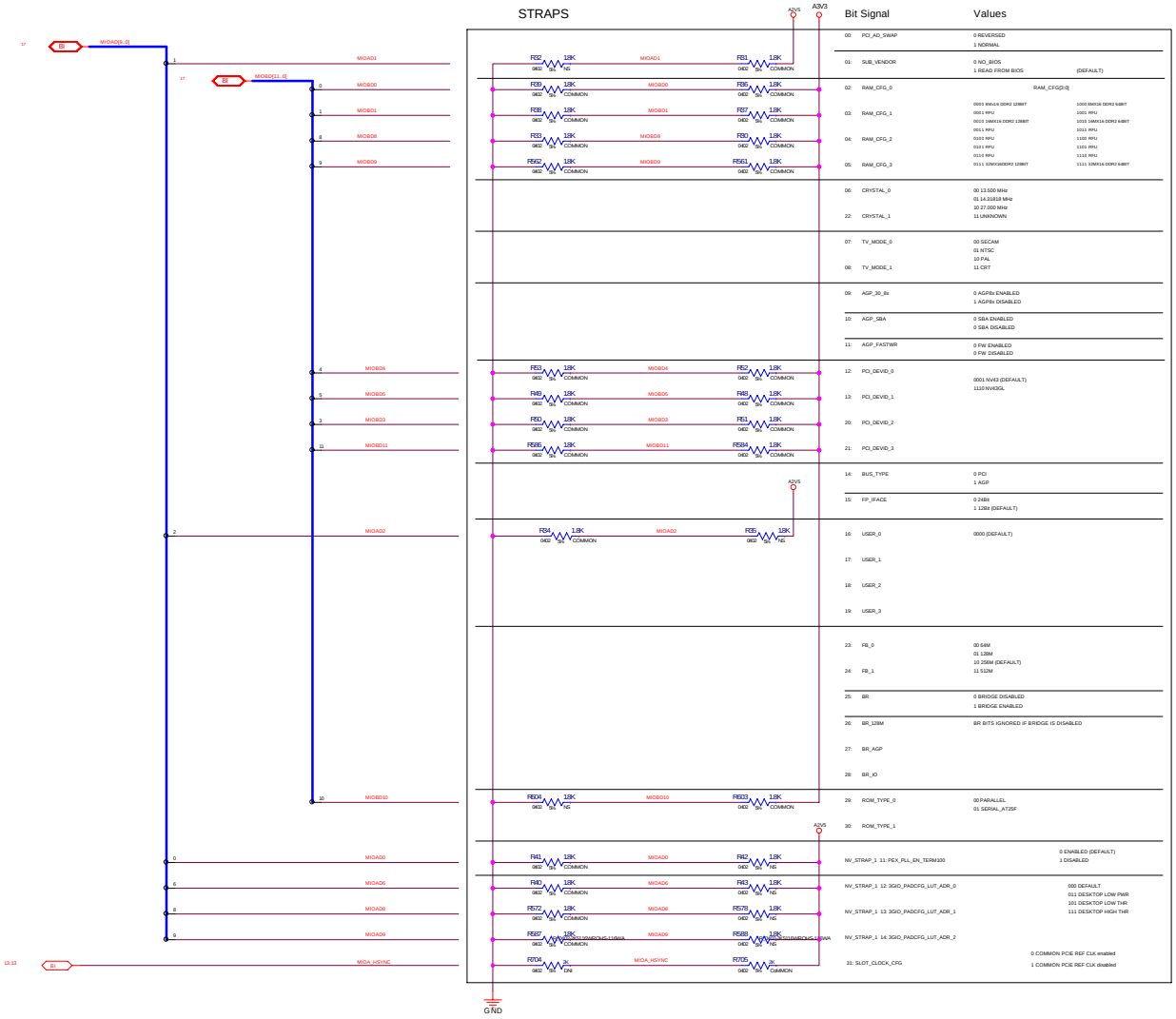
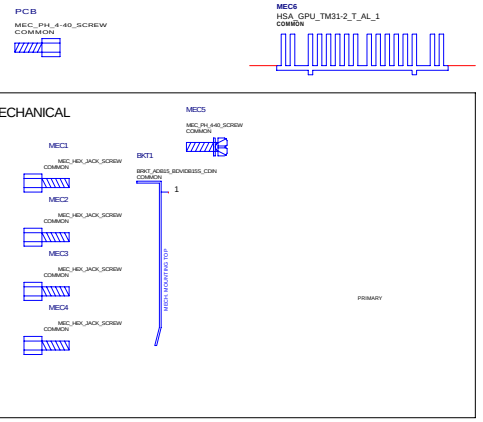
13 STRAPS, FANSINK, MECHANICALS

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground — Signal — High logic voltage





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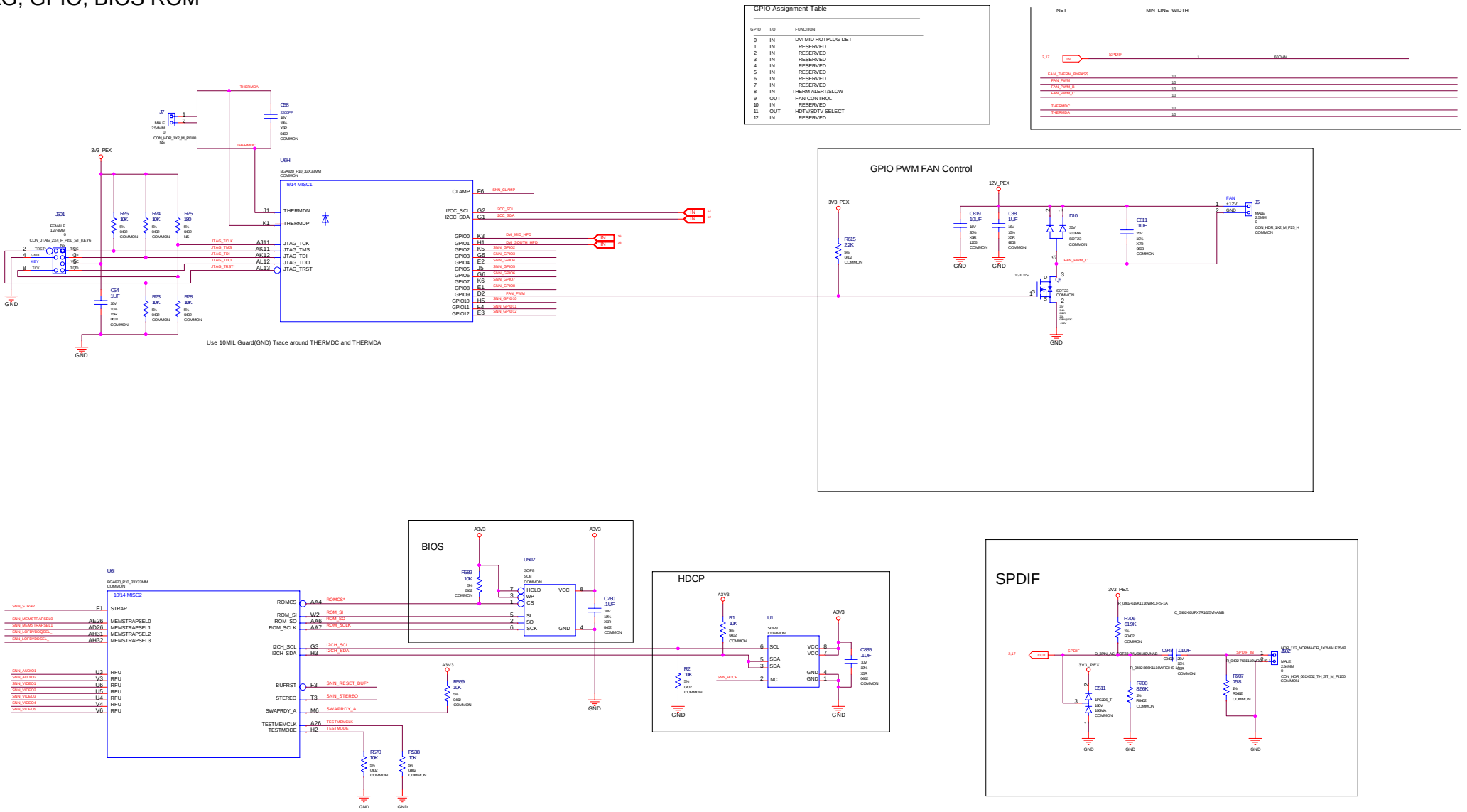
14 GPIO, HDCP, VBIOS, FAN CON

JTAG, GPIO, BIOS ROM



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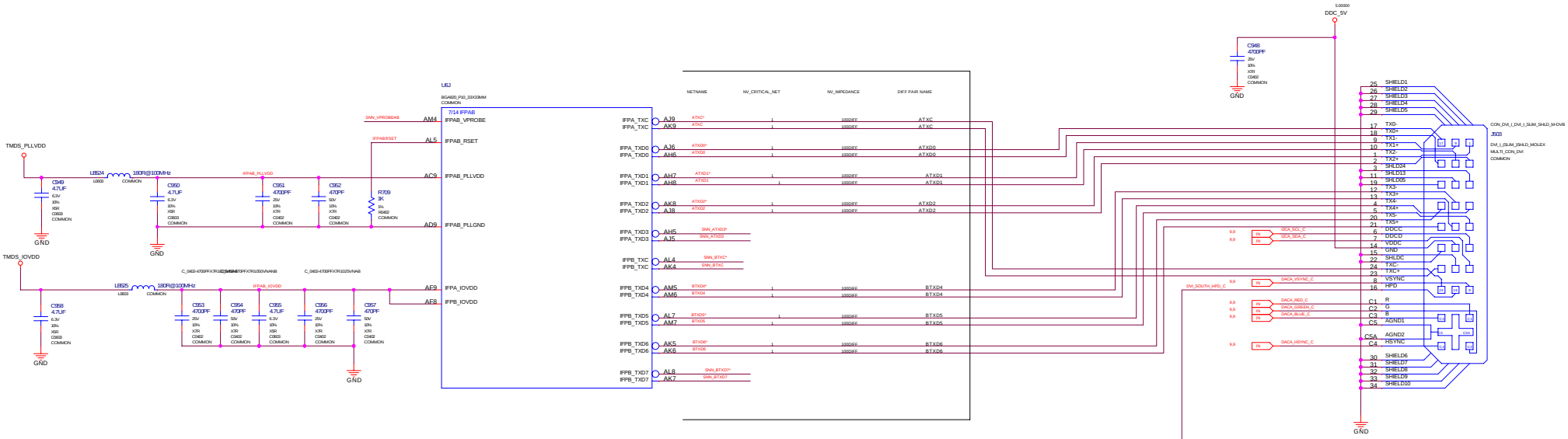
15 INTERNAL TMDS LINK A/B

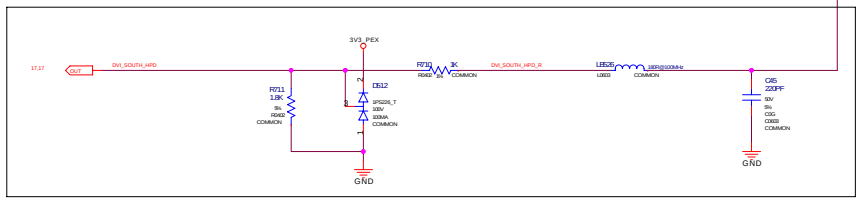
IFPAB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RSET	1	50OHM	
DVI_SOUTH_HPD_C	1	50OHM	
DVI_SOUTH_HPD_R	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLLVDD	3.30000	0.04	16.0
IFPAB_IOVDD	3.30000	0.24	16.0



Hotplug Detection



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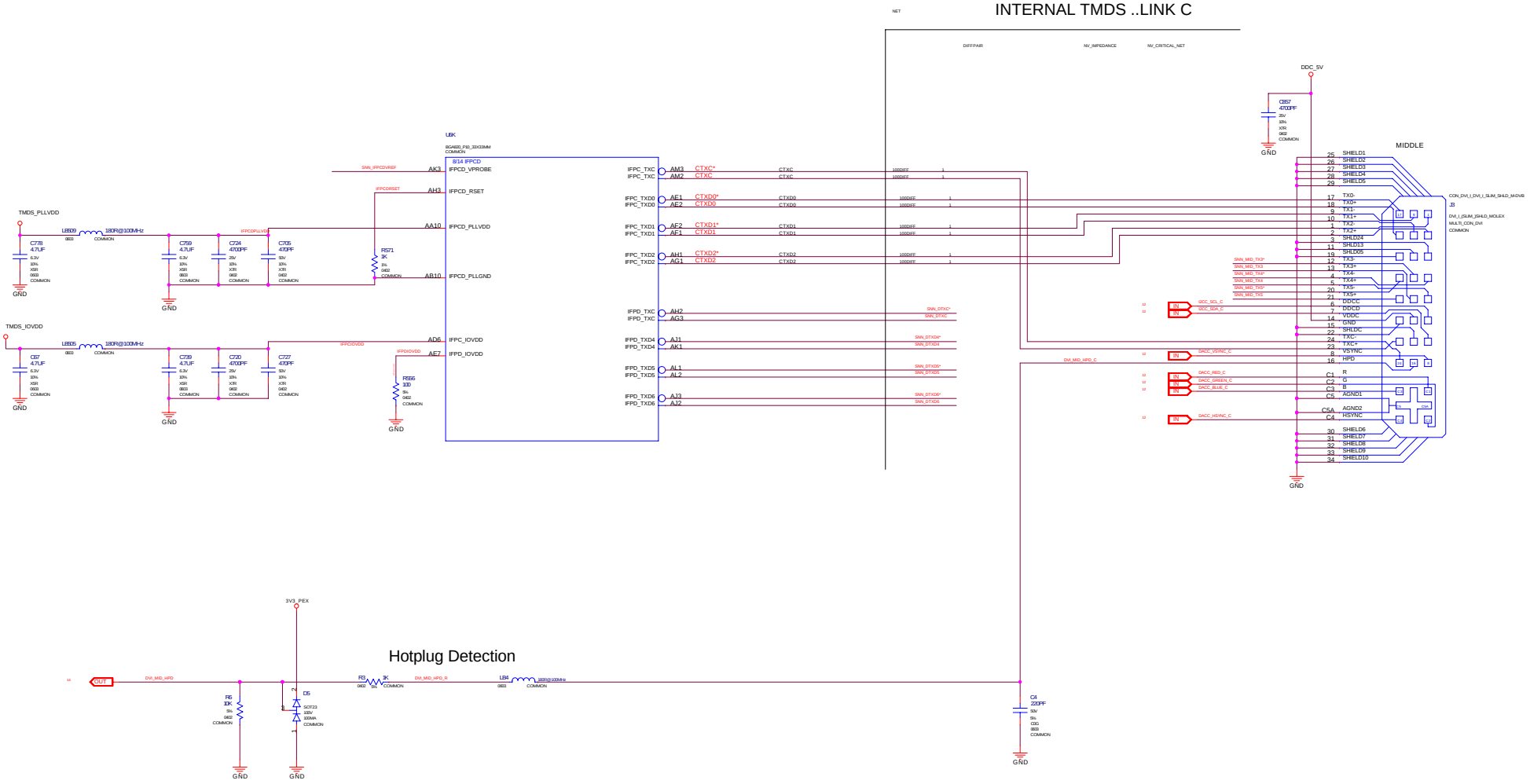
16 INTERNAL TMDS LINK C/D

NET	MIN_LINE_WIDTH	VOLTAGE
IFPCDVREF	12	3.3V
IFPCDPLLVDD	12	3.3V
IFPCIOVDD	12	3.3V
IFPIOVDD	12	3.3V
IFPCDRSET	12	

INTERNAL TMDS ..LINK C

Hotplug Detection



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17 MIOA, MIOB, NVPLL

MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
MIOAD[11..0]	2	50OHM	
MIOA_CLKIN	2	50OHM	
MIOA_CLKOUT	2	50OHM	
MIOA_DE	2	50OHM	
MIOA_VSYNC	2	50OHM	
MIOA_VSYNC	2	50OHM	
MIOBD[11..0]	2	50OHM	
VIPPCLK	2	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VDDQ	2.50000	0.8	12.0
MIOA_VREF	1.25000		12.0
MIOACAL_PD_VDDQ	2.50000		12.0
MIOACAL_PU_GND	0.000000		12.0
MIOB_VDDQ	3.30000	0.05	12.0
MIOB_VREF	1.65000		12.0
MIOBCAL_PD_VDDQ	3.30000		12.0
MIOBCAL_PU_GND	0.000000		12.0

Feature Connector

MIOA

MIOB

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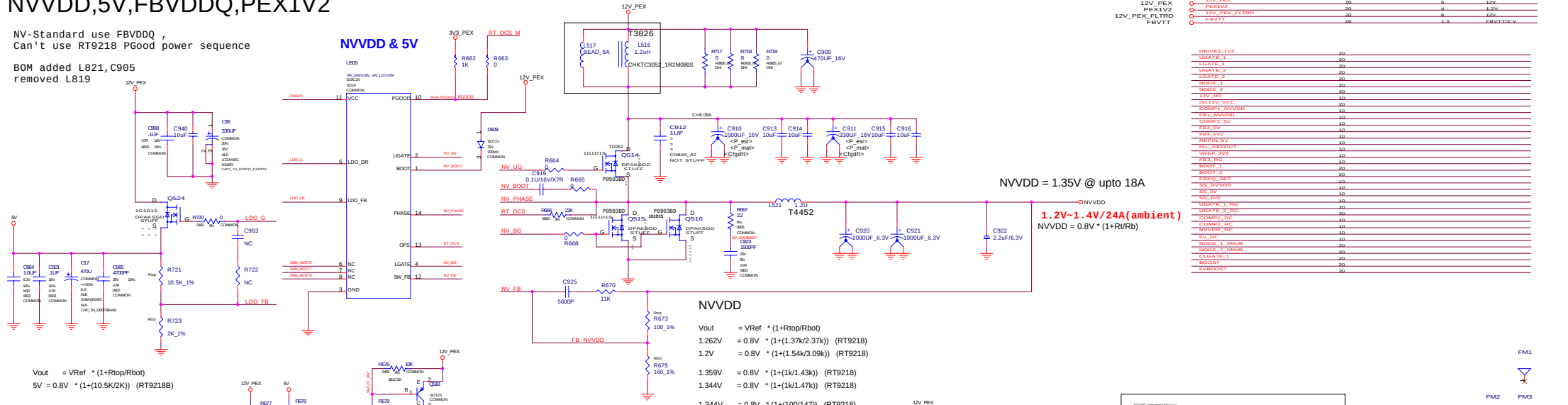
18 Power Supply (RT9218)
NVVDD,5V,FBVDDQ,PEX1V2

NV-Standard use FBVDDQ ,
Can't use RT9218 PGood power sequence

BOM added L821,C905
removed L819

NVVDD & 5V



NVVDD

Vout = VRef * (1+Rtop/Rbot)

1.262V = 0.8V * (1+(1.37k/2.37k)) (RT9218)

1.2V = 0.8V * (1+(1.54k/3.09k)) (RT9218)

1.359V = 0.8V * (1+(1k/1.43k)) (RT9218)

1.344V = 0.8V * (1+(1k/1.47k)) (RT9218)

1.344V = 0.8V * (1+(100/147)) (RT9218)

1.3V = 0.8V * (1+(100/160)) (RT9218) default

Vout = VRef * (1+Rtop/Rbot)

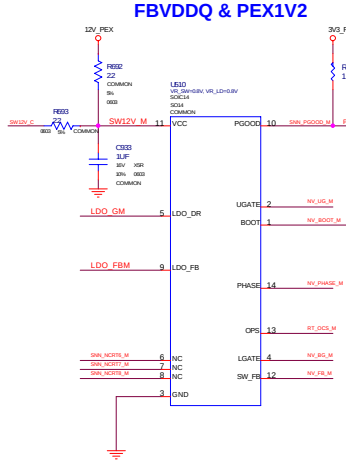
5V = 0.8V * (1+(10.5K/2K)) (RT9218B)

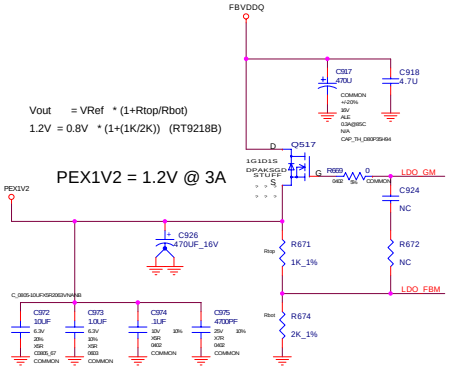
FBVDDQ & PEX1V2

Choose RT9218 PGood power sequence

Added BOM R883,R904

Removed R905





Vout = VRef * (1+Rtop/Rbot)

1.2V = 0.8V * (1+(1K/2K)) (RT9218B)

PEX1V2 = 1.2V @ 3A

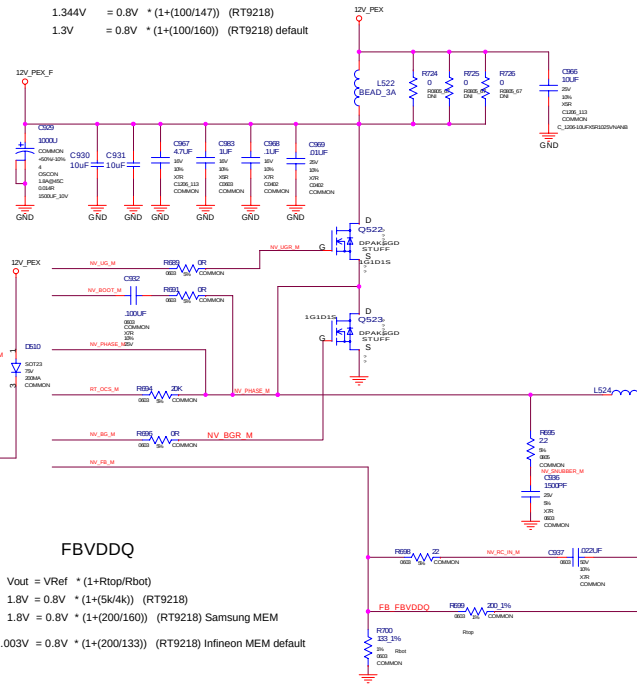
FBVDDQ

Vout = VRef * (1+Rtop/Rbot)

1.8V = 0.8V * (1+(5k/4k)) (RT9218)

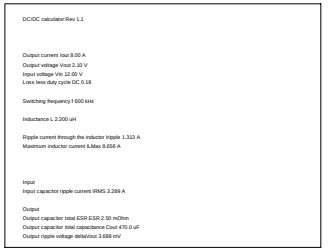
1.8V = 0.8V * (1+(200/160)) (RT9218) Samsung MEM

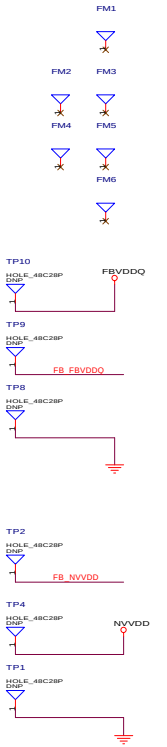
2.003V = 0.8V * (1+(200/133)) (RT9218) Infineon MEM default



FBVDDQ = 1.8V @ upto 5A

1.8V/5.0A





Net Name	MIN_LINE_WIDTH		VOLTAGE
5V	16	3	5V
NVVDD	16	20	1.35V
12V_PEX	20	6	12V
PEX1V2	20	4	1.2V
12V_PEX_FLTRD	20	6	12V
FBVTT	20	1.5	FBVTT/2 V

DRIVE3_1V2	20
UGATE_1	20
LGATE_1	20
UGATE_2	20
LGATE_2	20
NODE_1	20
NODE_2	20
12V_RR	10
ISL12V_VCC	20
COMP1_NVVDD	10
FB1_NVVDD	10
COMP2_5V	10
FB2_5V	10
FB3_1V2	10
REFIN_5V	10
ISL_REFOUT	10
VREF_3V3	10
FB3_RC	10
BOOT_1	20
BOOT_2	20
FREQ_SET	10
SS_NVVDD	10
SS_5V	10
SS_1V2	10
UGATE_1_RG	20
UGATE_2_RG	20
COMP1_RC	10
COMP2_RC	10
NVVDD_RC	10
5V_RC	10
NODE_1_SNUB	20
NODE_2_SNUB	20
CLGATE_1	20
BOOST	20
5VBOOST	20

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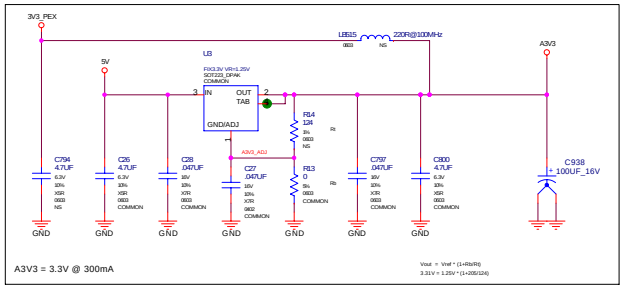
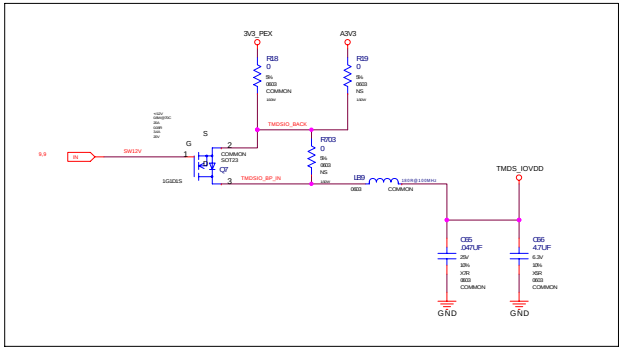
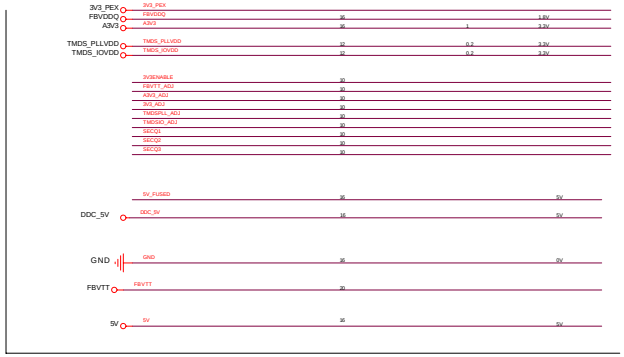
19 Others Power Supply (Linears)
A3V3,A2V5,TMDS_PLLVDD,TMDS_IOVDD

A3V3

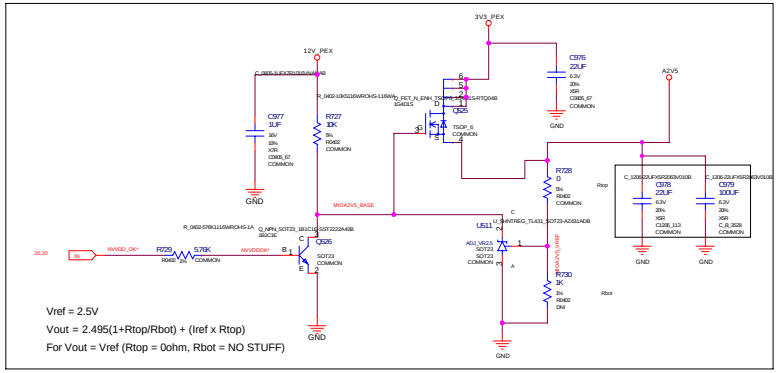


TMDS IO SUPPLY WITH BACKDRIVE PROTECTION

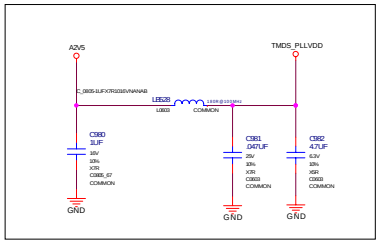




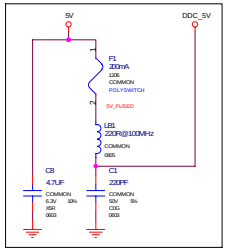
A2V5



TMDS PLL Supply



DDC 5V



Power Sequencing for FBVDDQ & A2V5