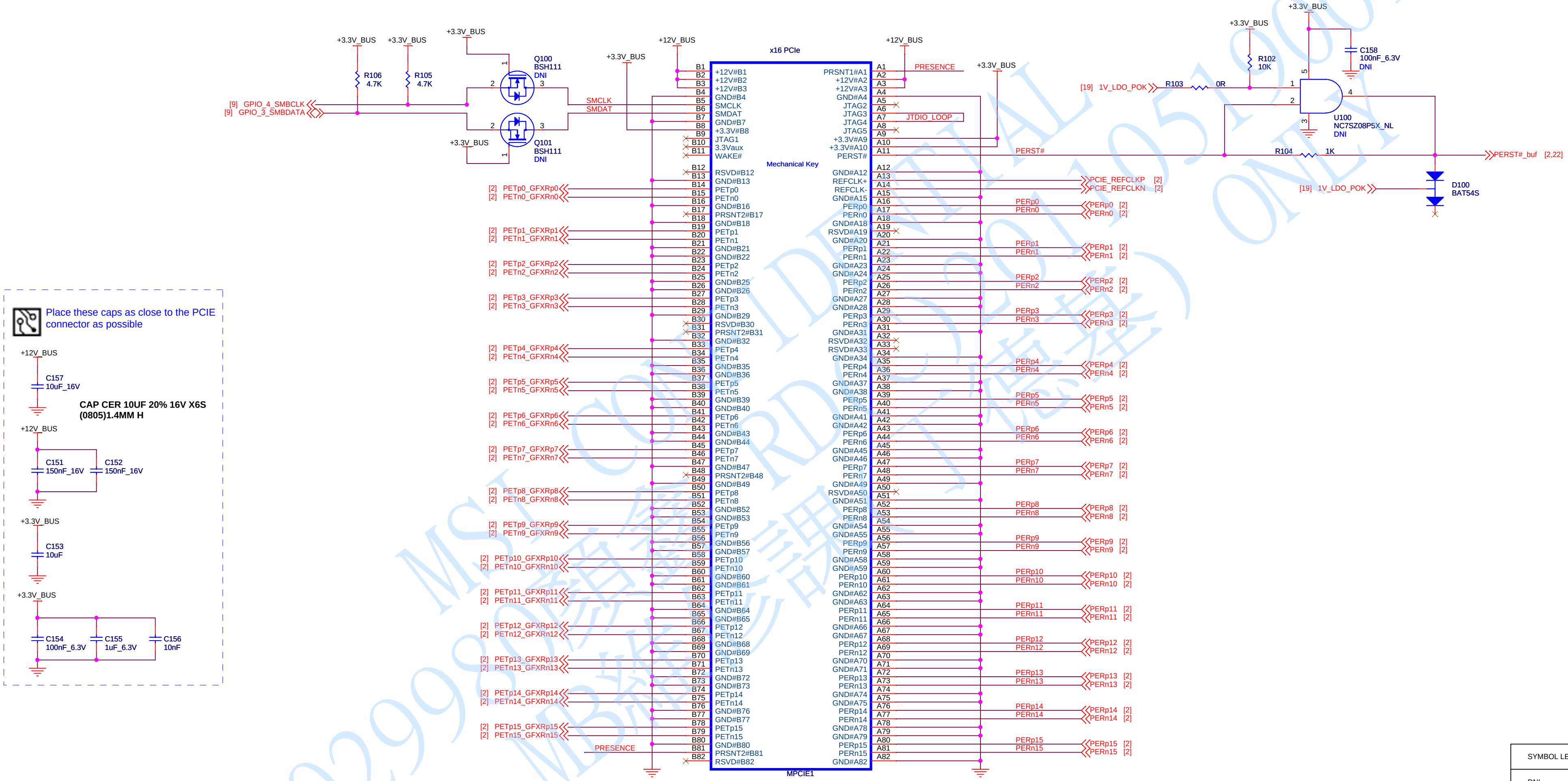
PCI-EXPRESS EDGE CONNECTOR

PCIe RESET Buffered



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
(symbol)	DIGITAL GROUND
(symbol)	ANALOG GROUND
BUO	BRING UP ONLY

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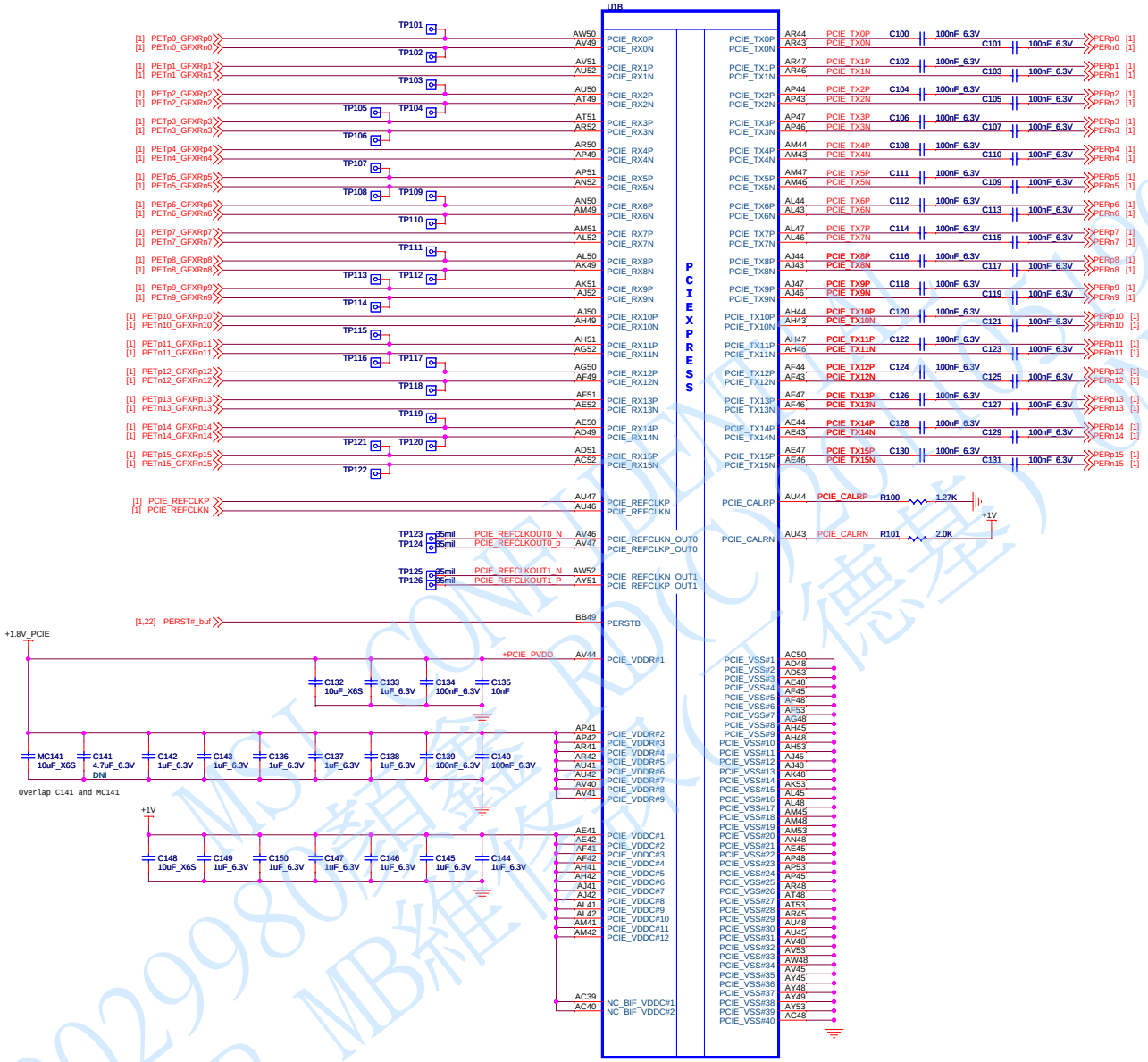
Title: PCIE EDGE CONNECTOR | Doc No. 105-C205XX-00A

(2) CAMEN PCIE Interface



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Title	ASIC PCIE Interface
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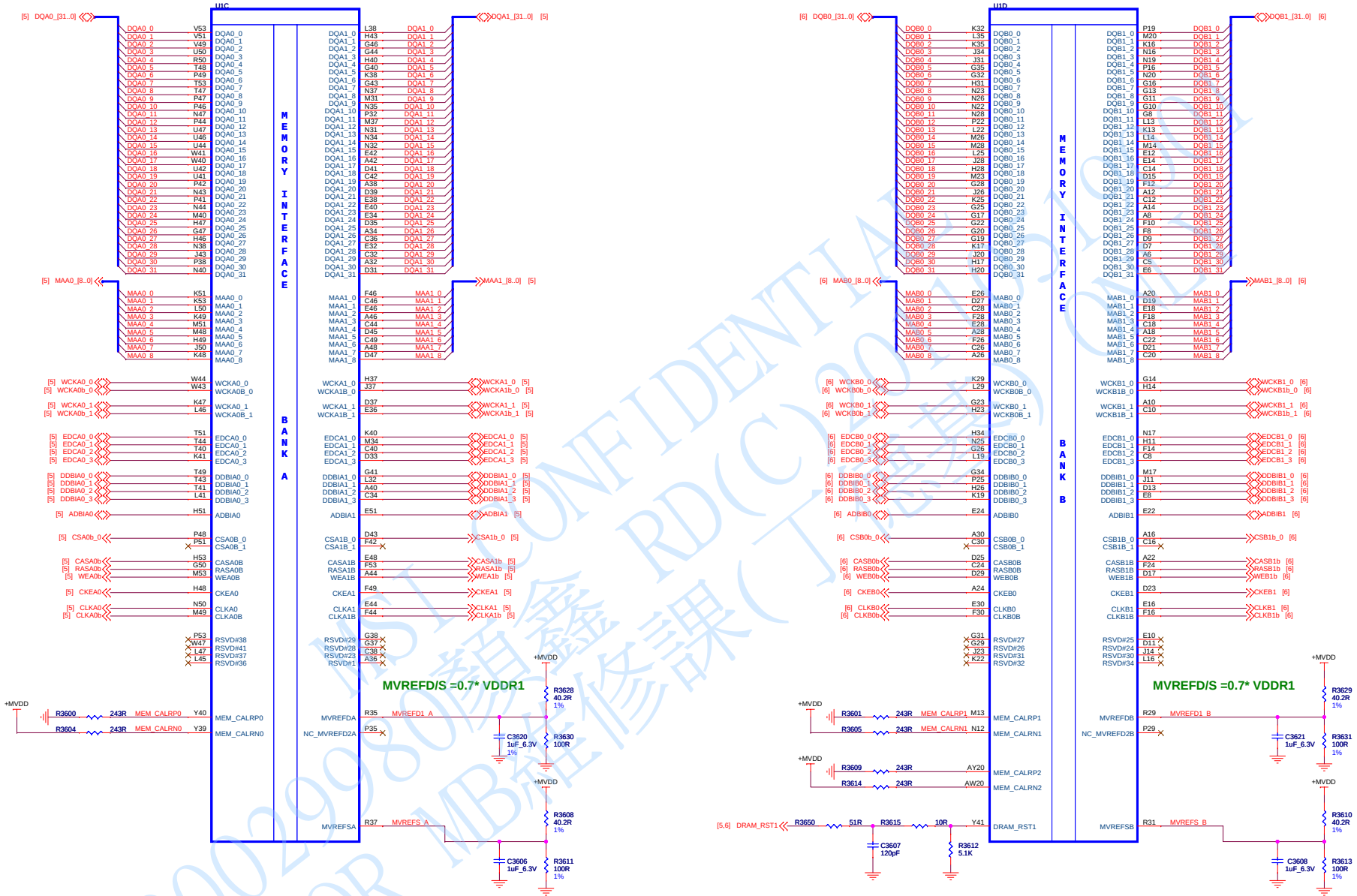
(3) CAYMEN MEM Interface Ch A&B



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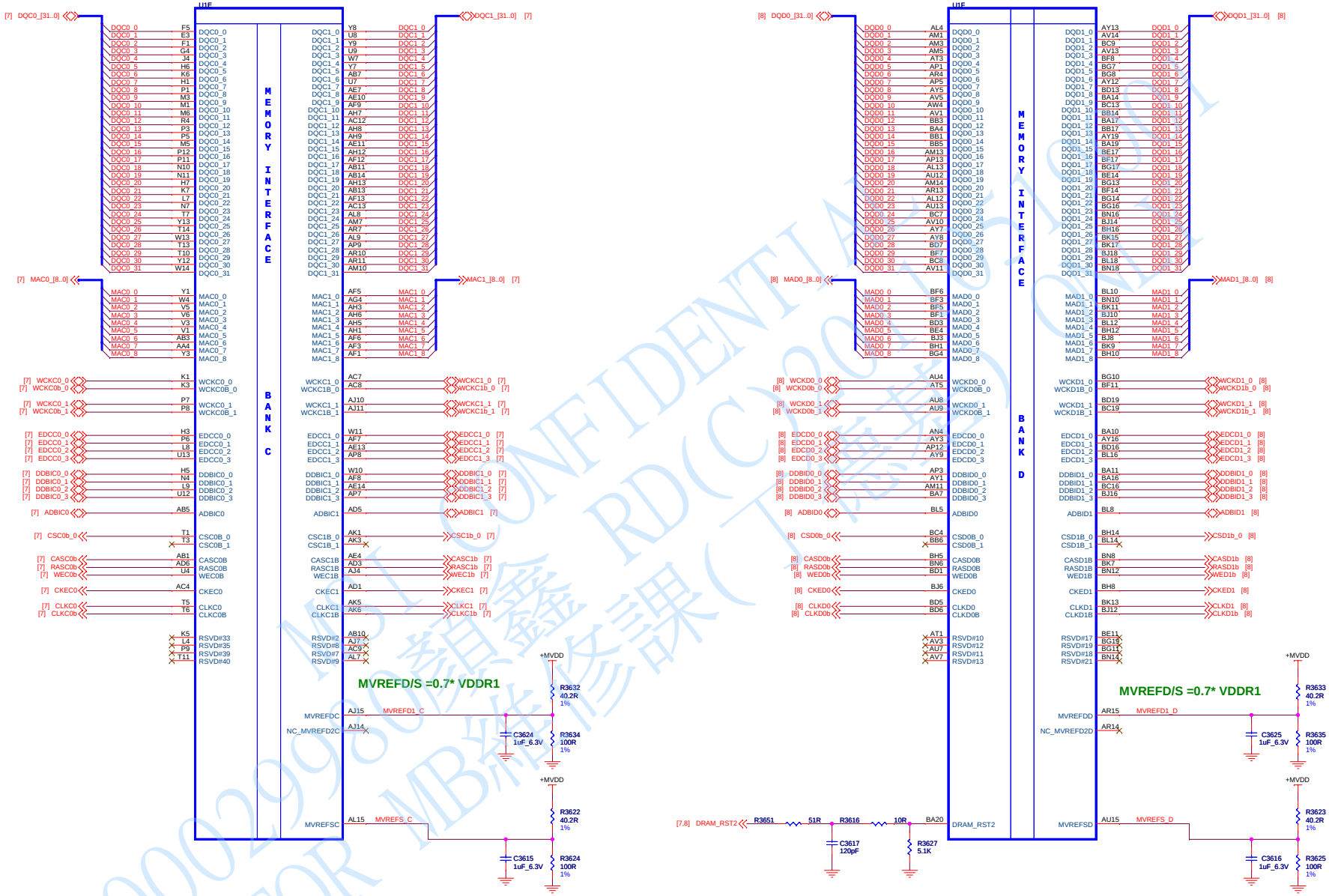
(4) CAYMEN MEM Interface Ch C&D



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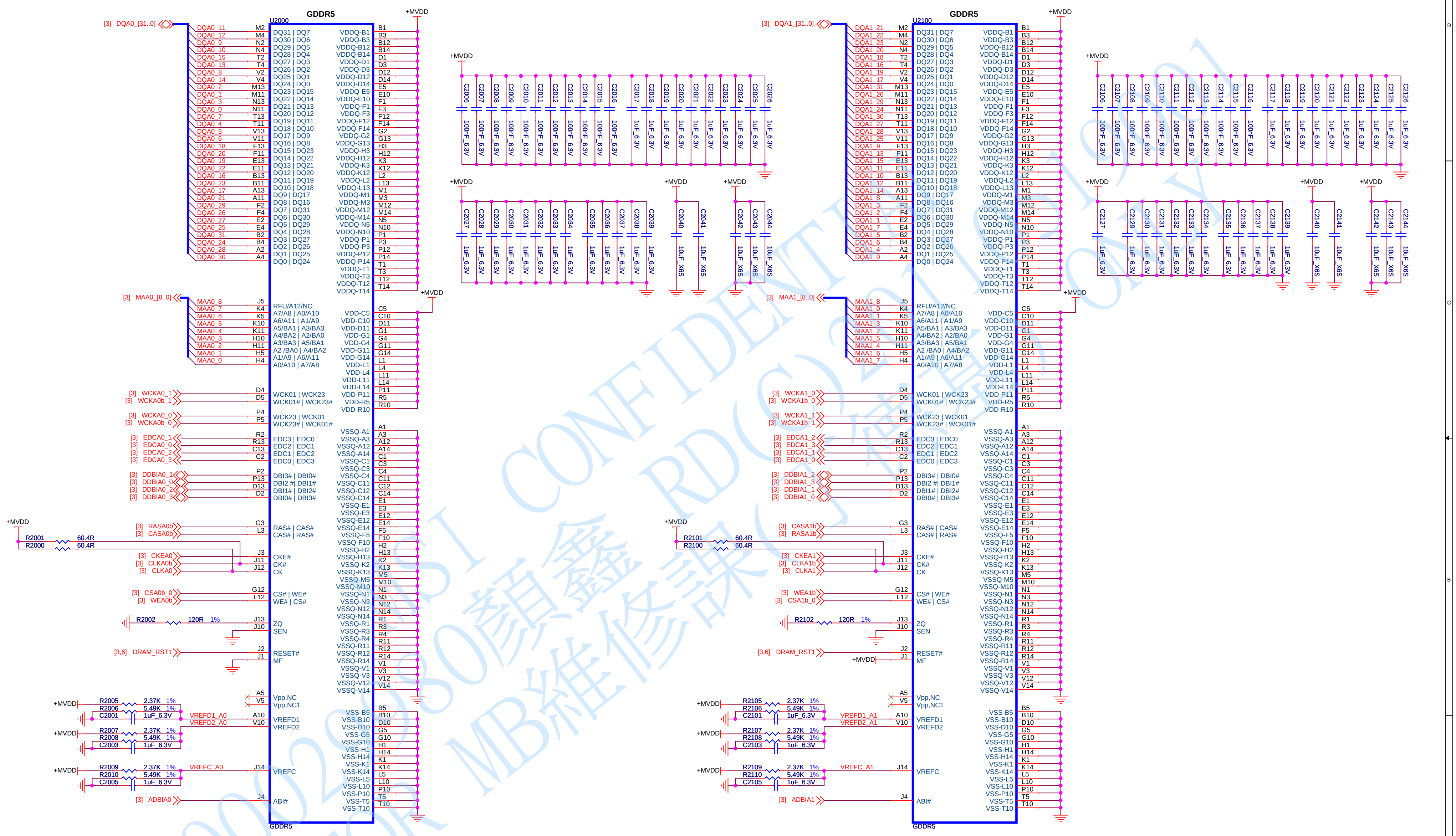
(5) GDDR5 Memory Channel A



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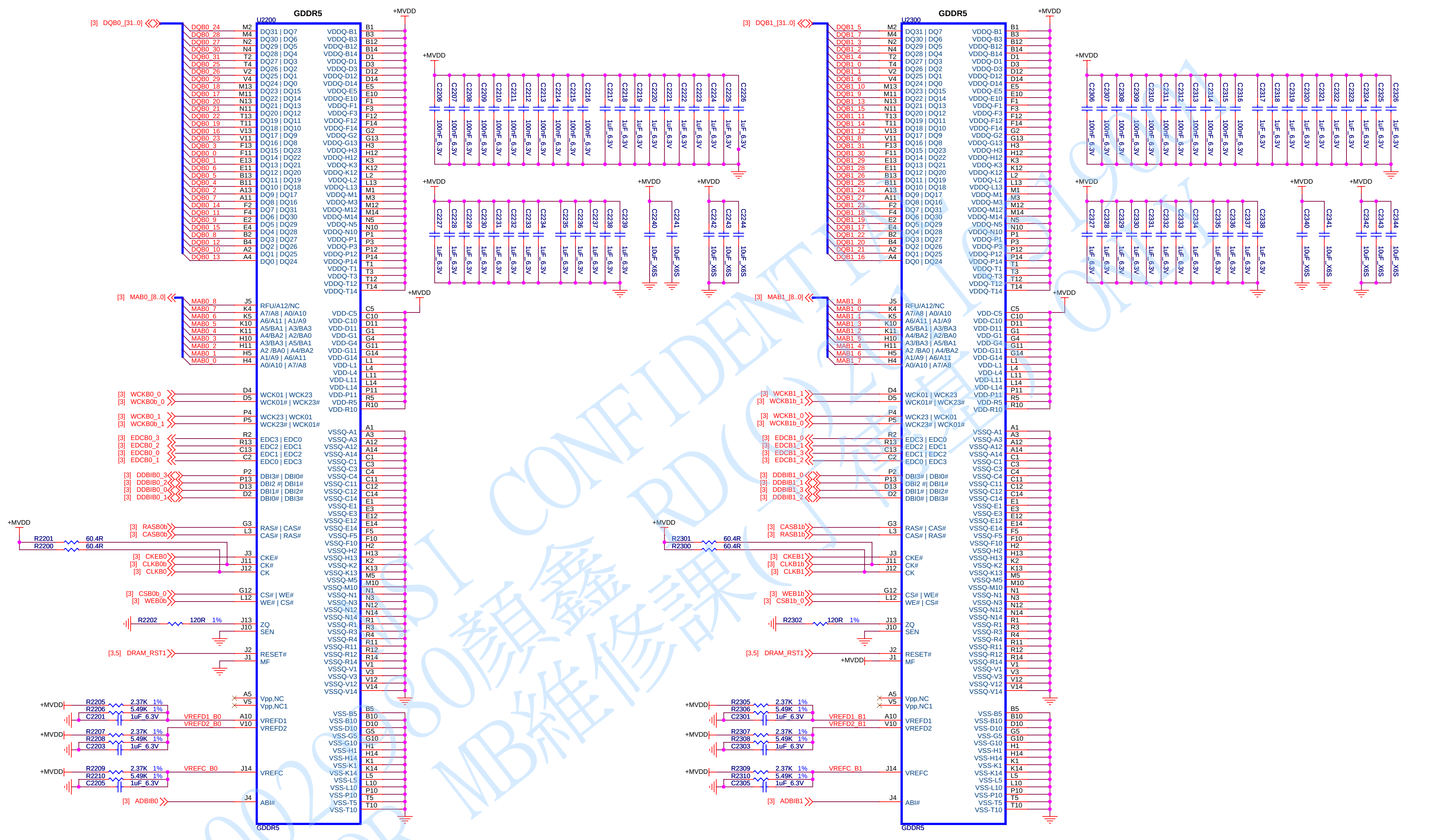
Title GDDR5 Ch A | Doc No. 105-C205XX-00A

(6) GDDR5 Memory Channel B



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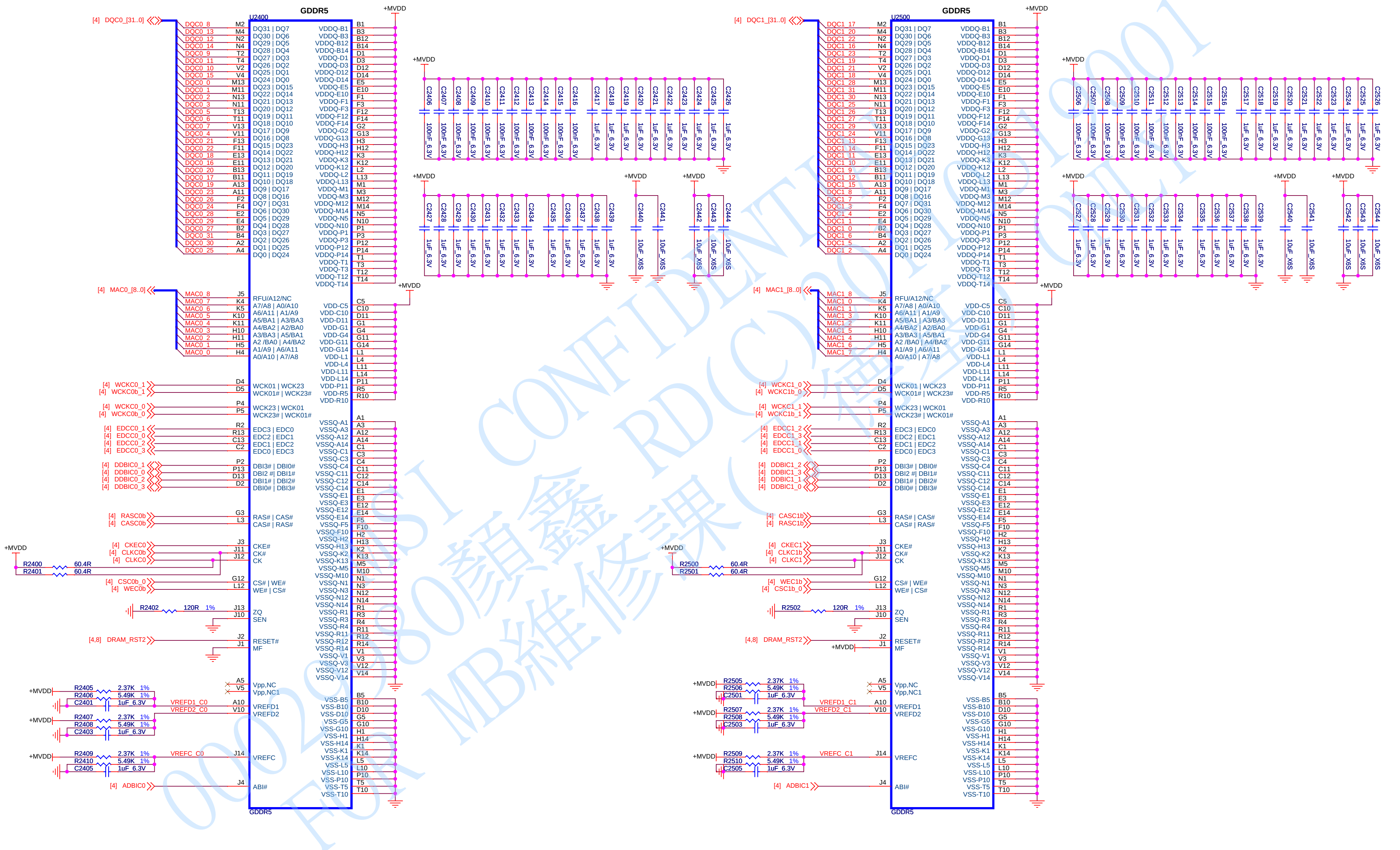
(7) GDDR5 Memory Channel C



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Title GDDR5 Ch C
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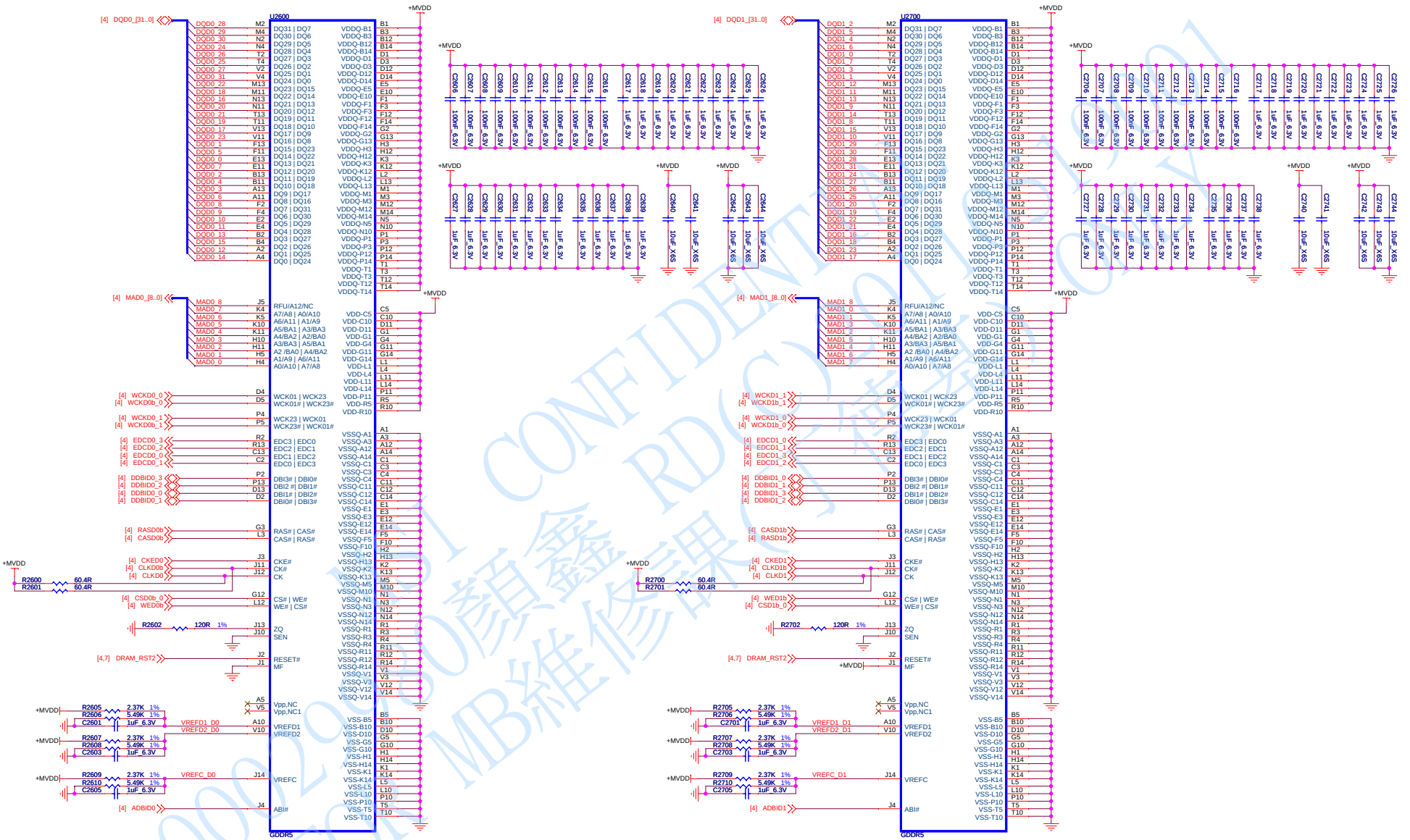
(8) GDDR5 Memory Channel D



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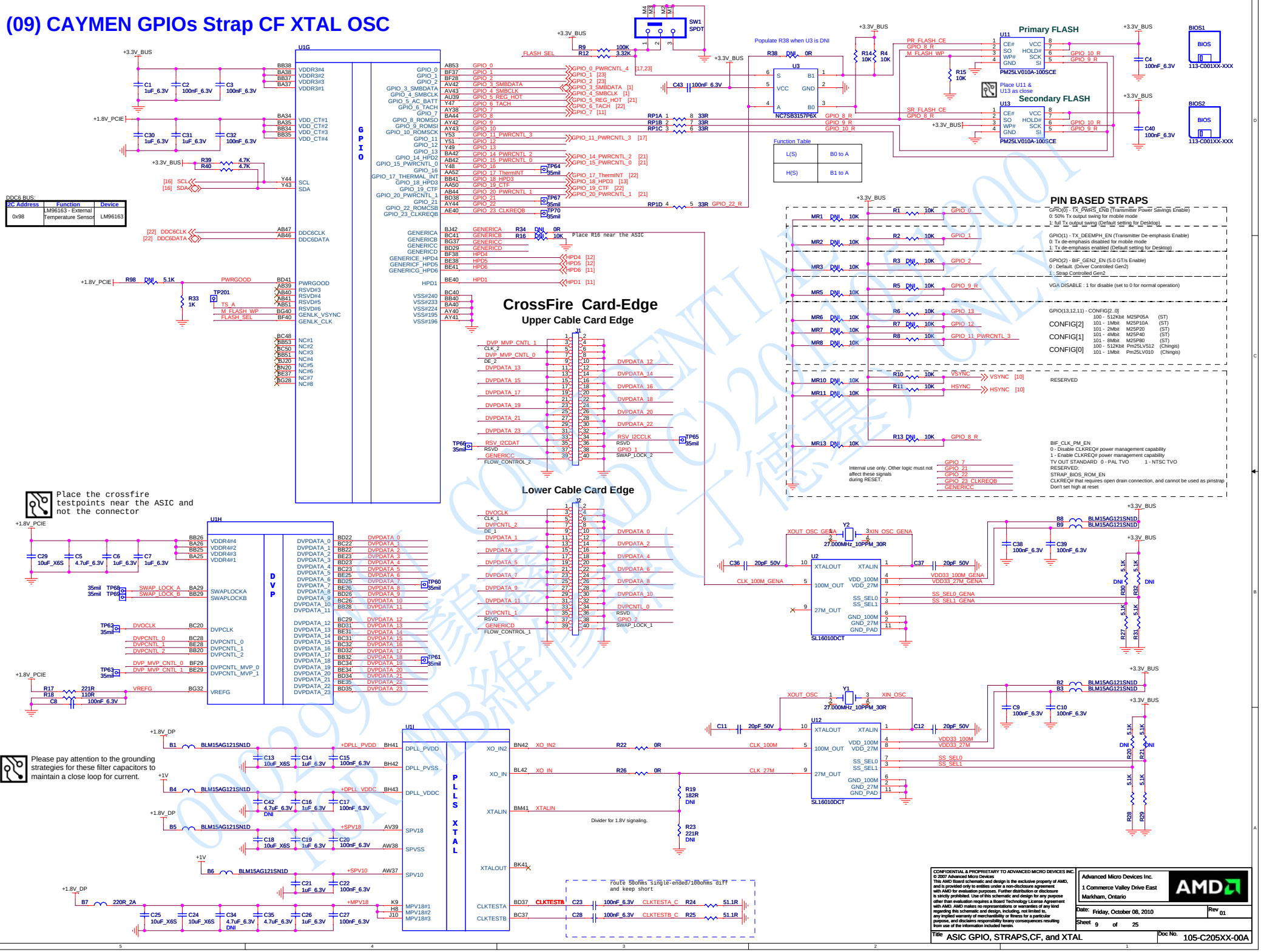
(09) CAYMEN GPIOs Strap CF XTAL OSC



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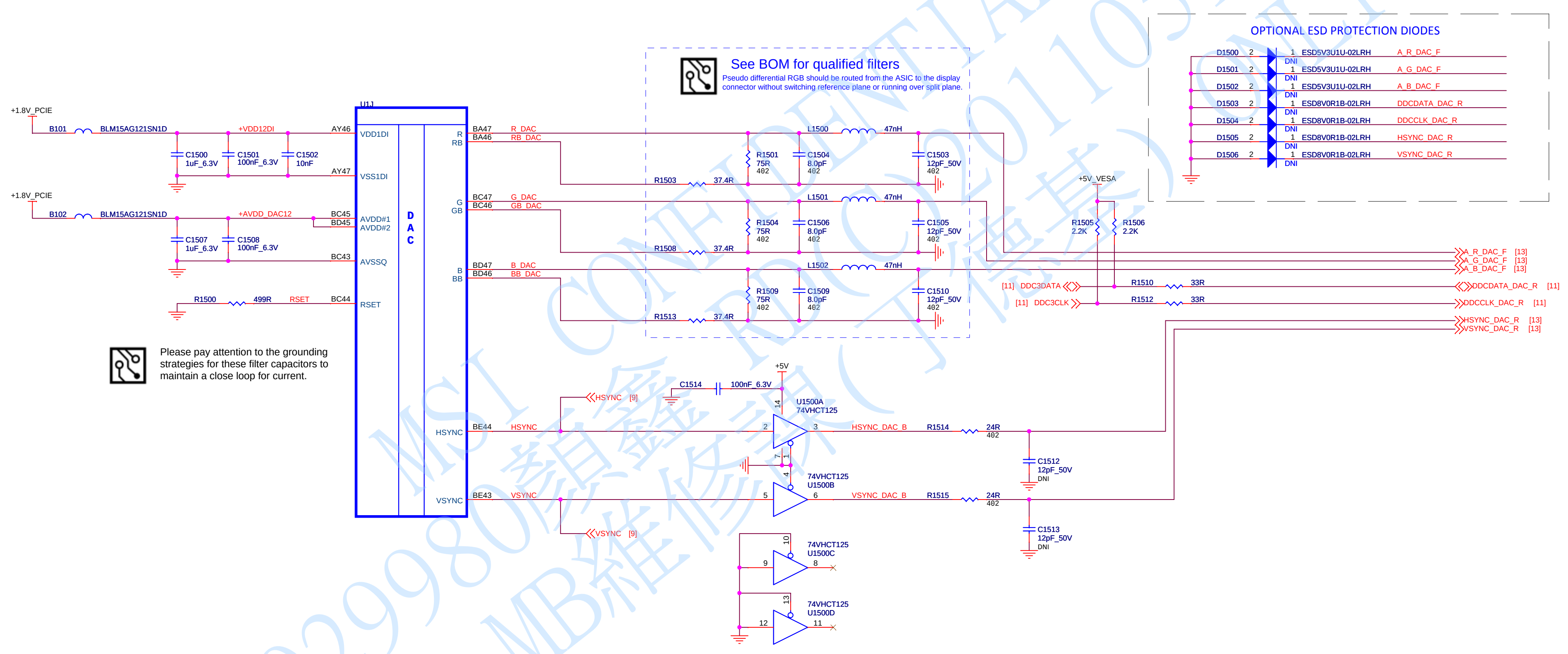
Title ASIC GPIO, STRAPS,CF, and XTAL	Doc No. 105-C205XX-00A

(10) CAYMEN DAC



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Title ASIC DAC1 & DAC2
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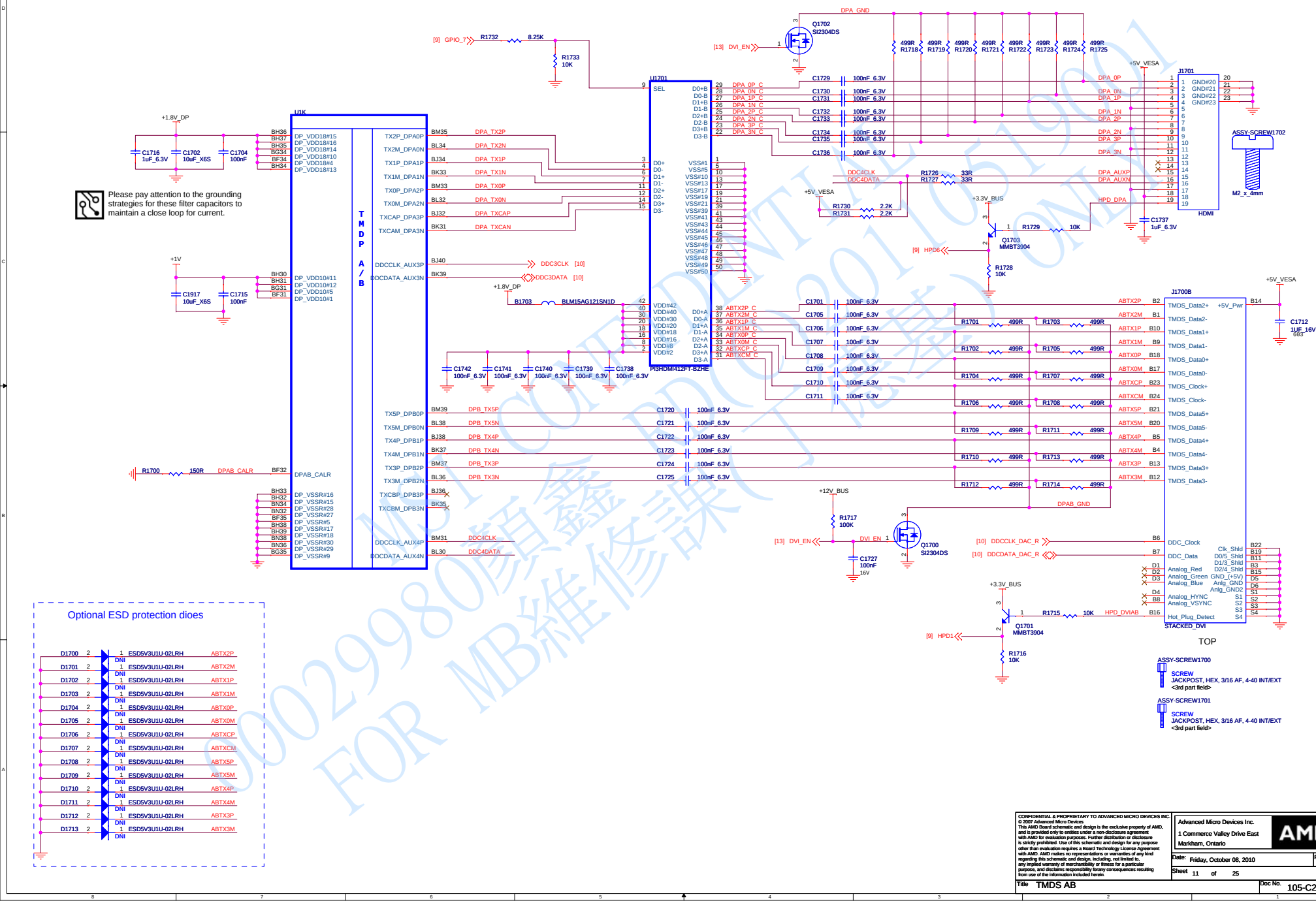
(11) CAYMEN TMDS A&B



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Title	TMDS AB
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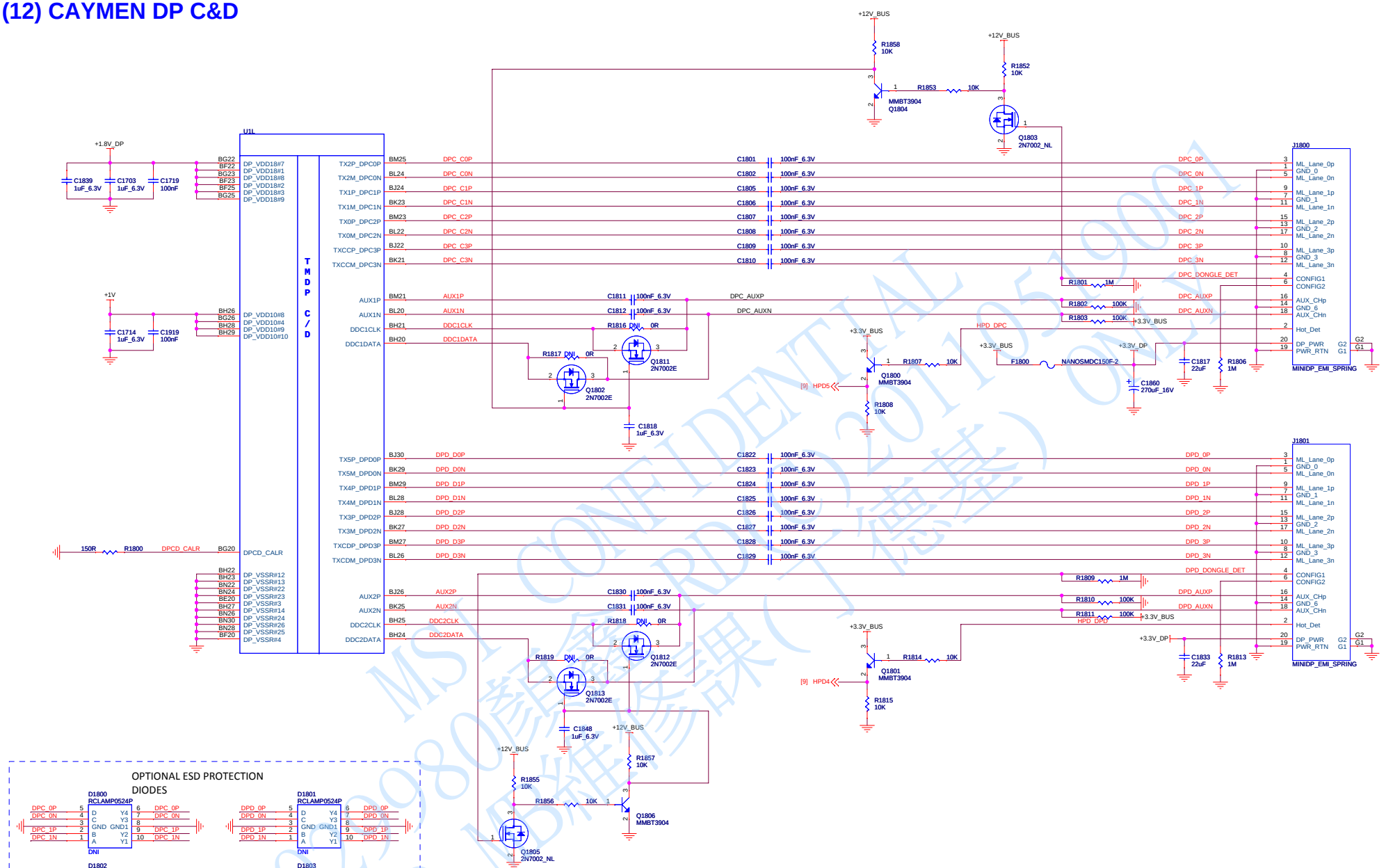
(12) CAYMEN DP C&D



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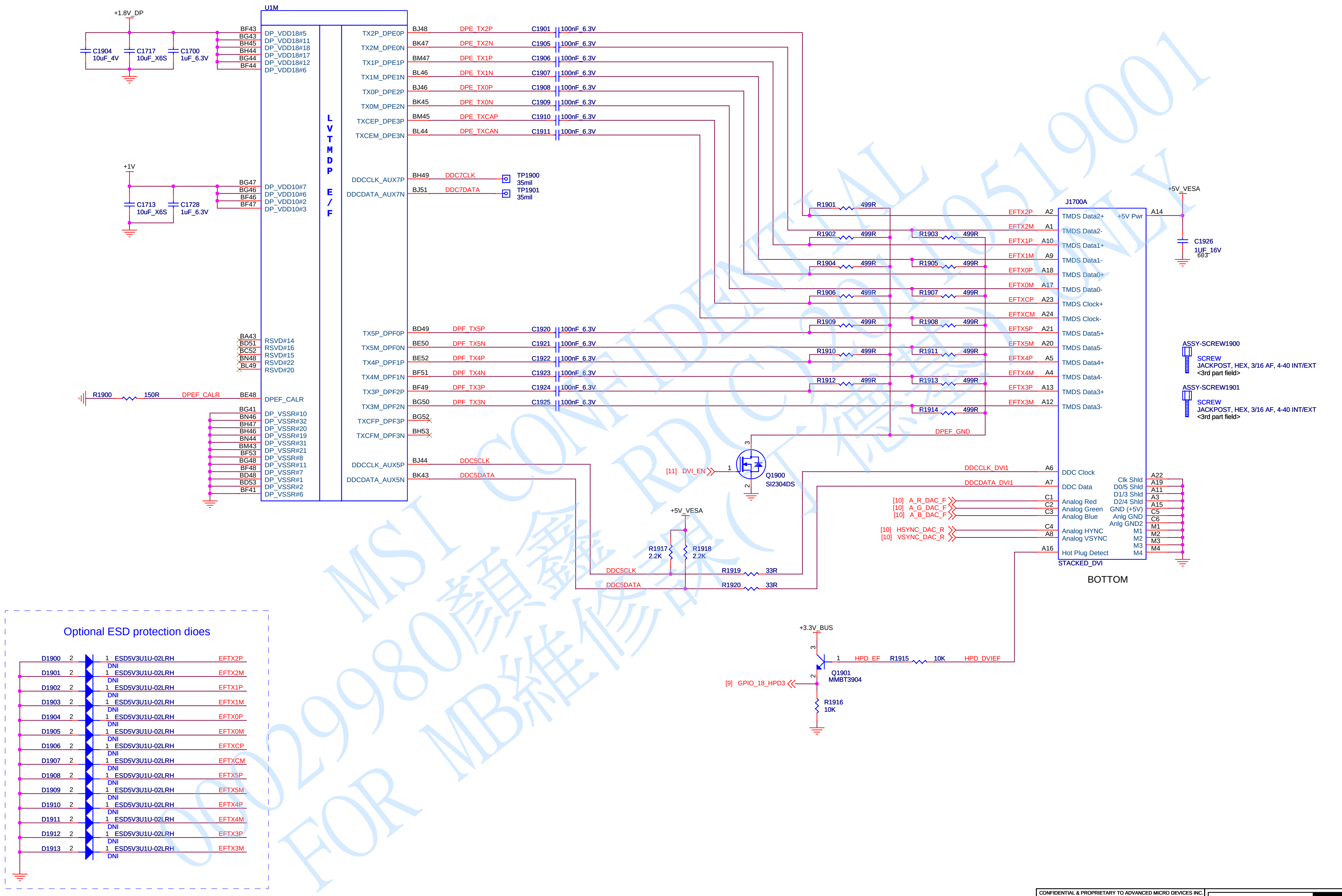
(13) CAYMEN LVTMDP E&F



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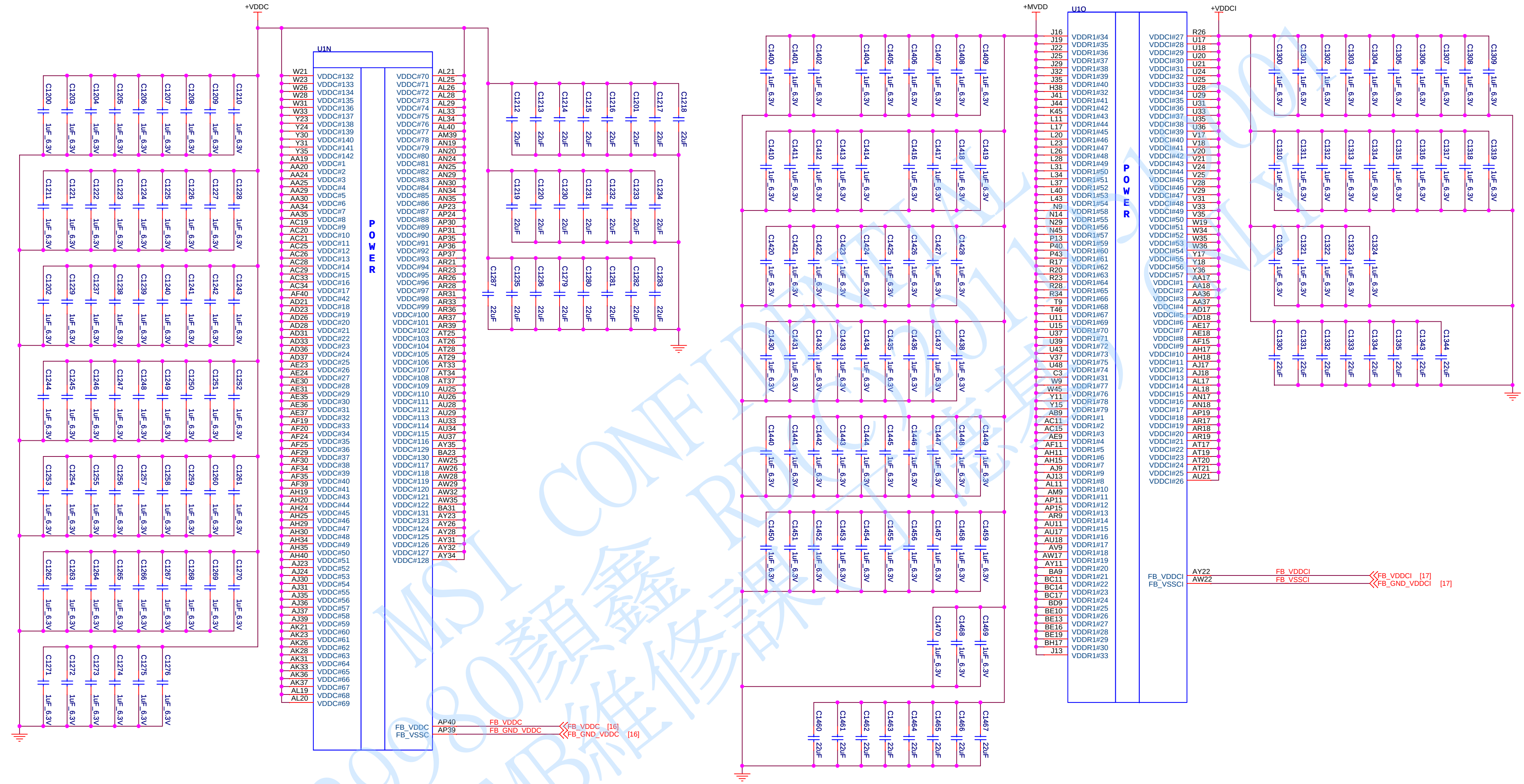
Title TMDS EF	Doc No. 105-C205XX-00A

(14) CAYMEN Power



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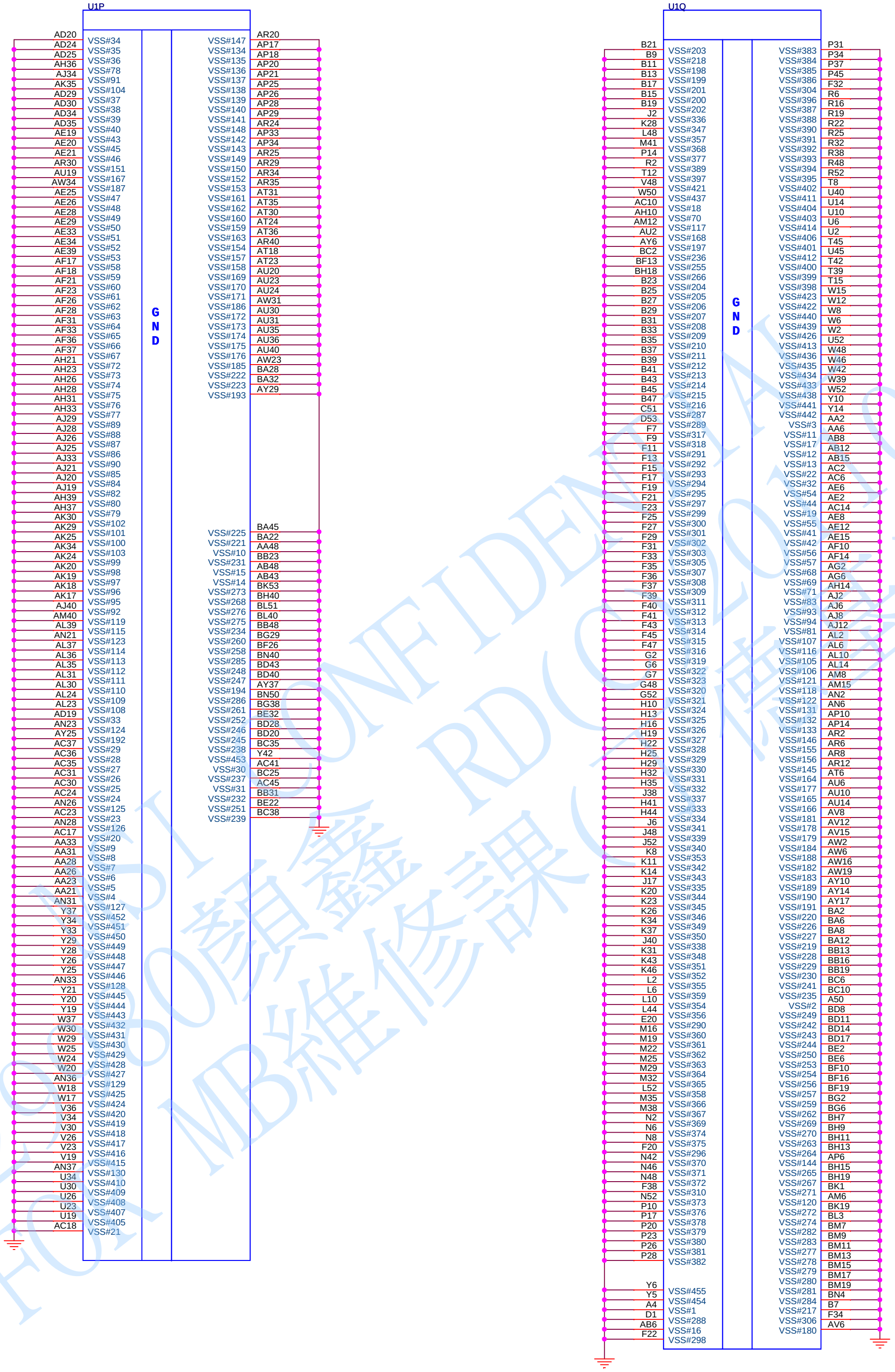
(15) CAYMEN GND



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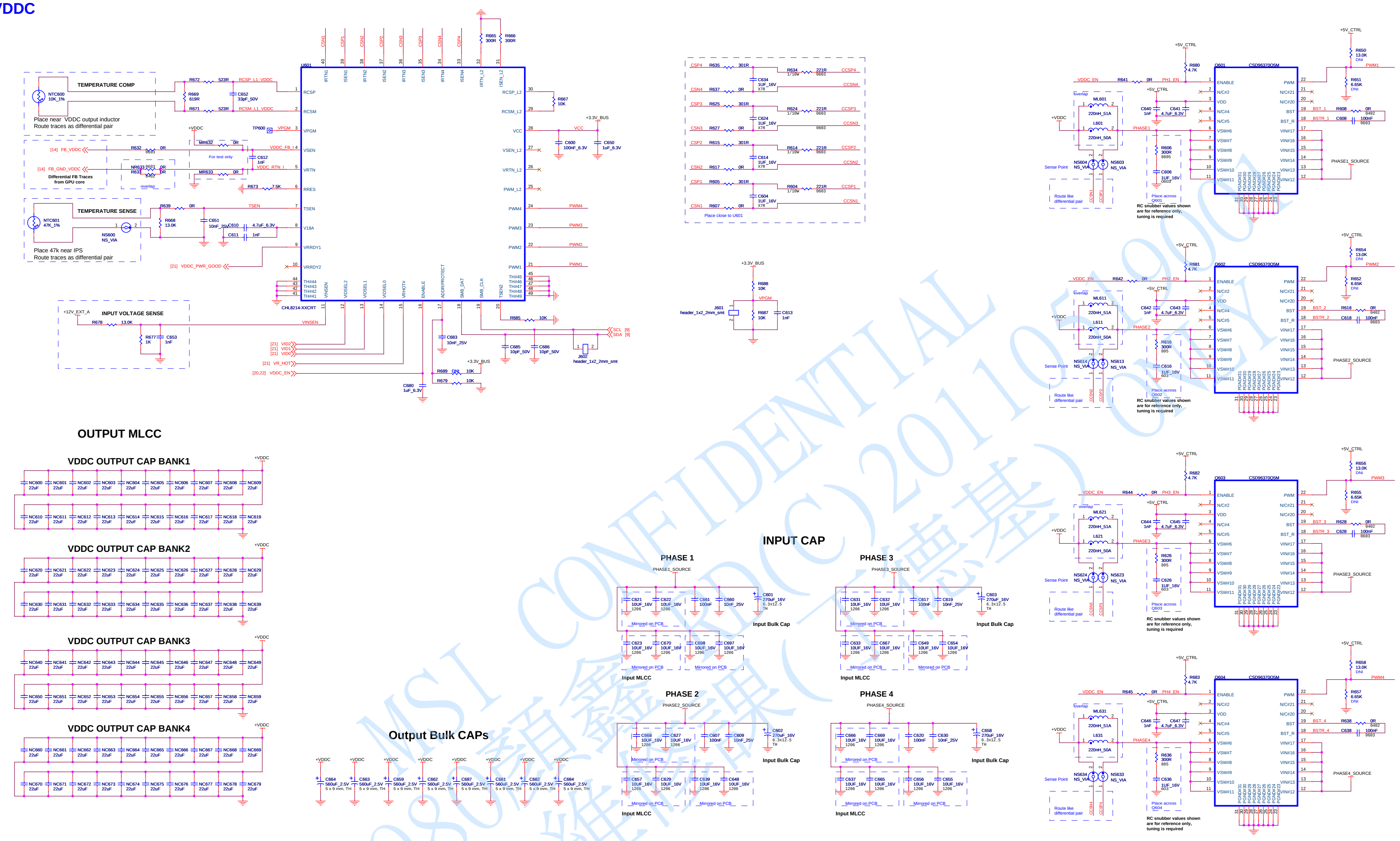
(16) VDDC



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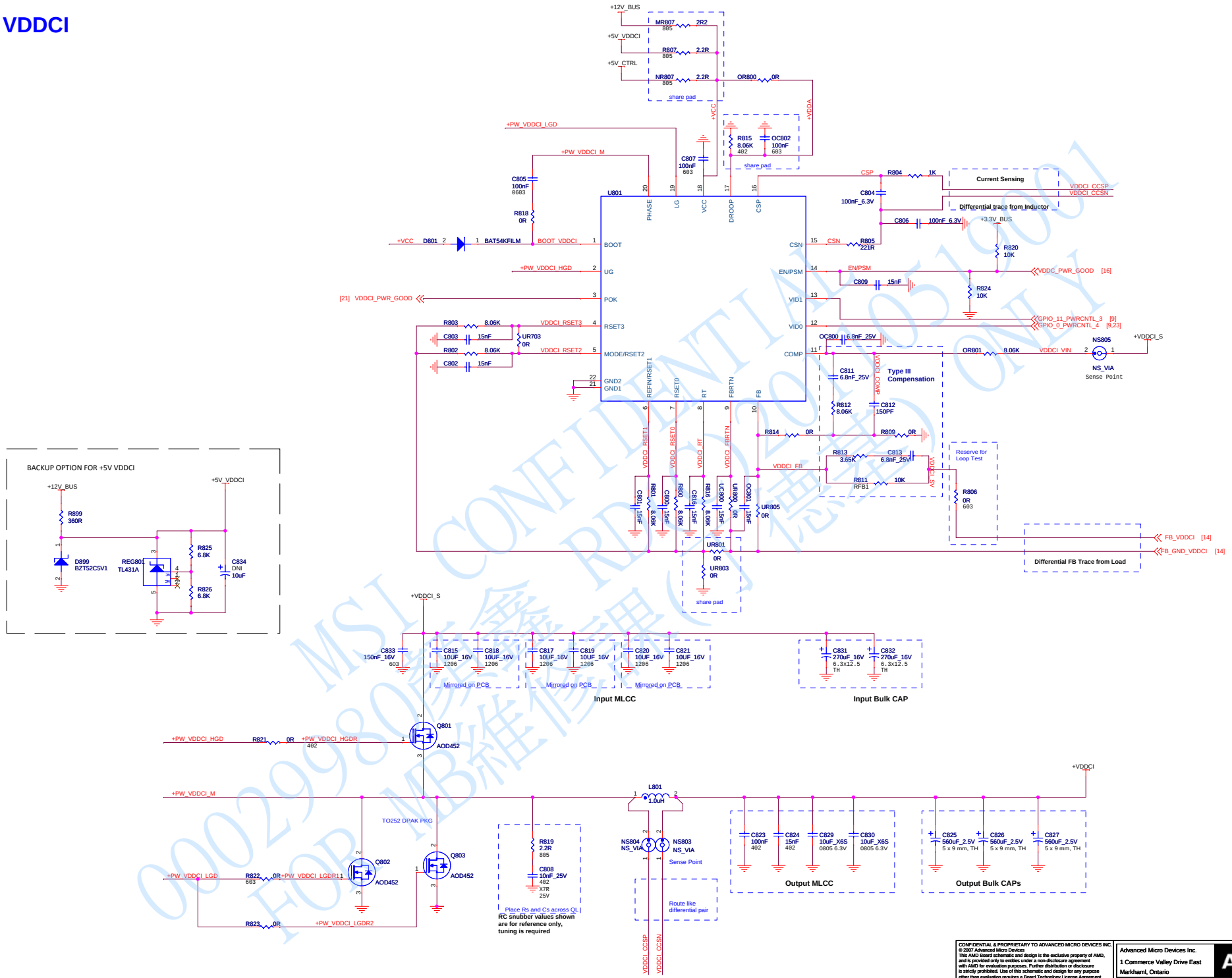
(17) VDDCI



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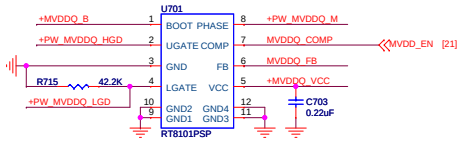
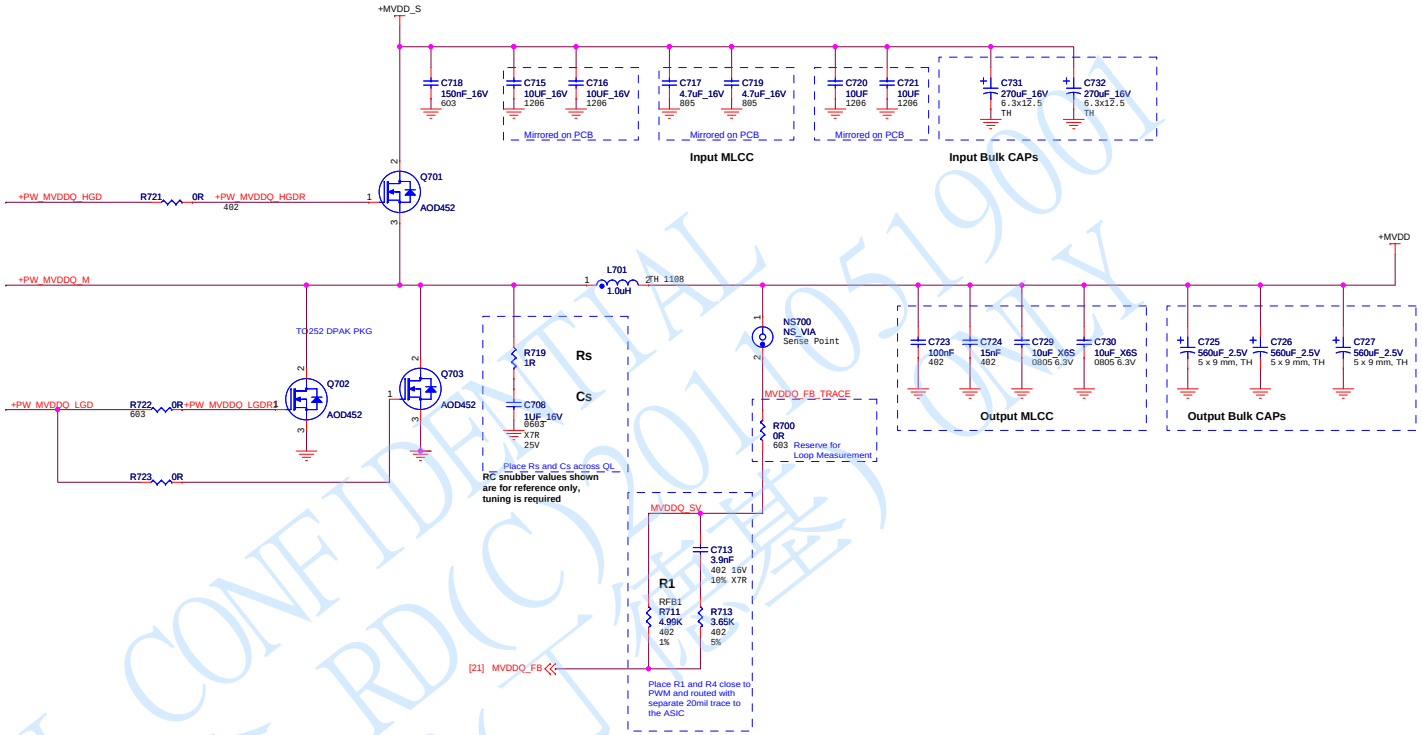
(18) MVDD

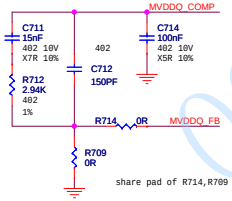




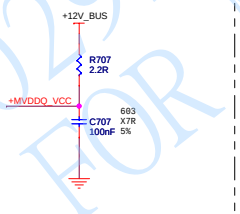
Layout guideline

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

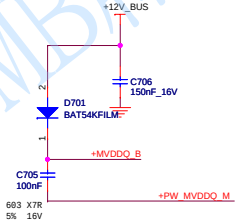
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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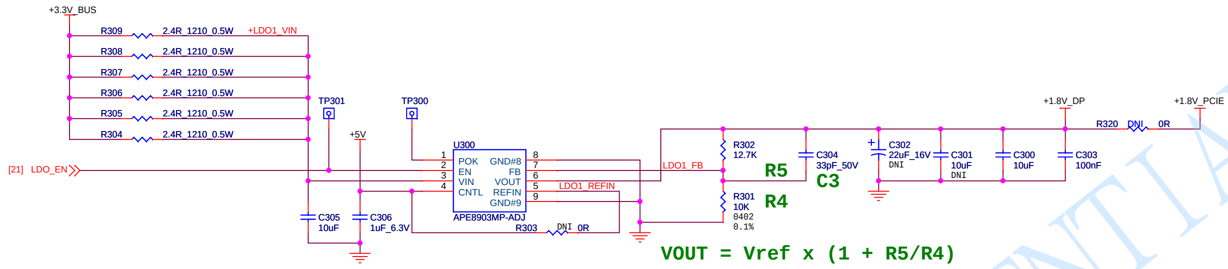
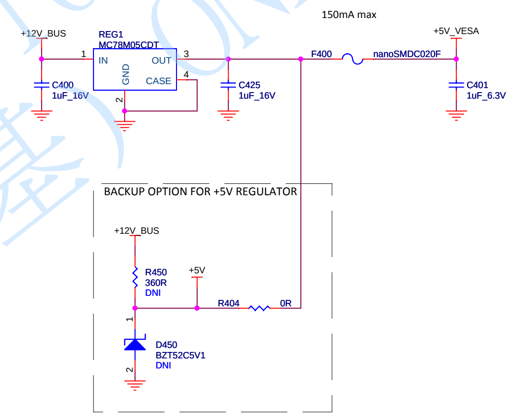
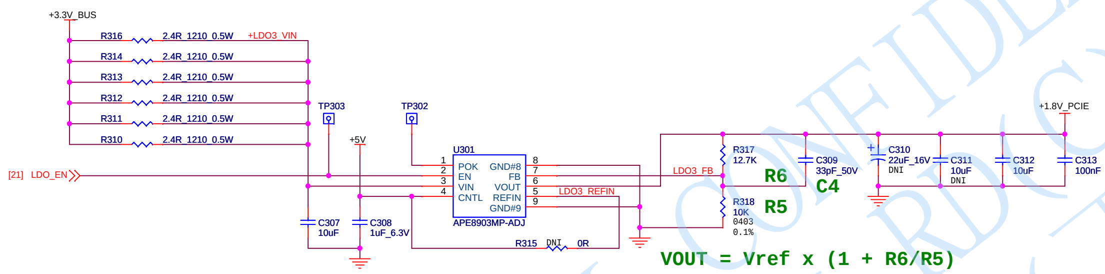
(19) CAYMEN Small Rail Regulators

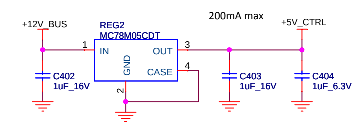
LDO #1: Vin = 2.3V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.0A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



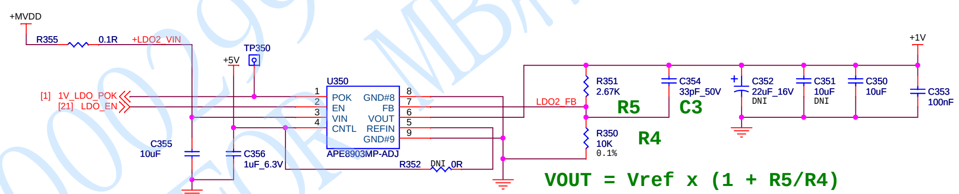
Regulators for +5V, +5V_VESA and +5V_HDMI
Iout max = 150mA (DVI+HDMI)







LDO #2: Vin = +1.40V to 1.8VMAX Vout = +1V +/- 2% Iout = 1.5A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



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Title Small Rail Regulators
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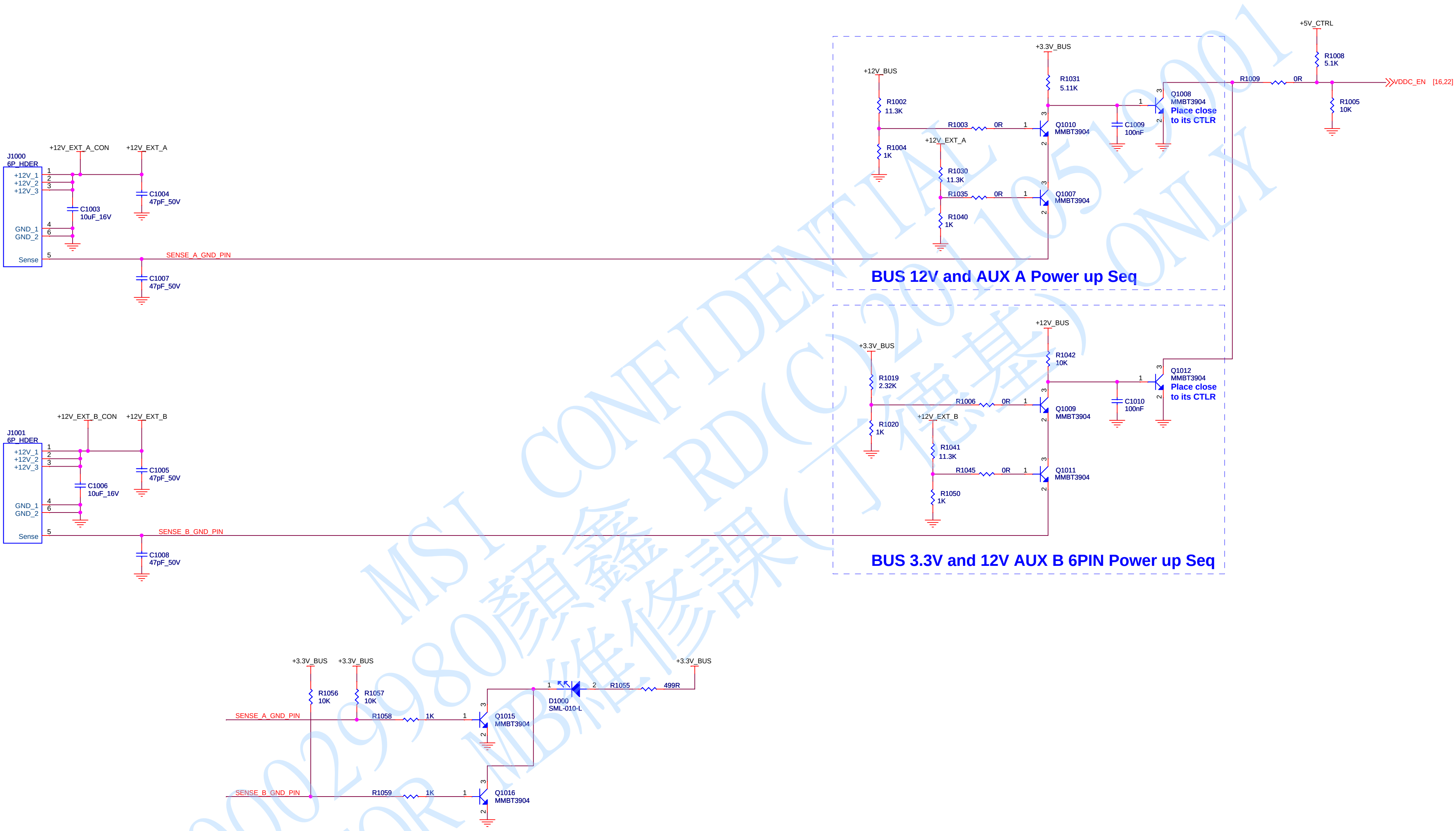
(20) CAYMEN POWER MGMNT



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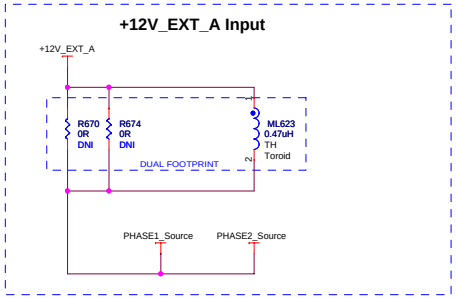
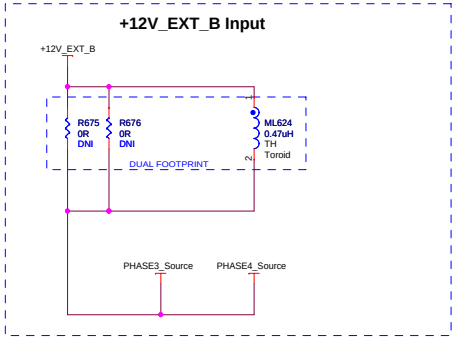
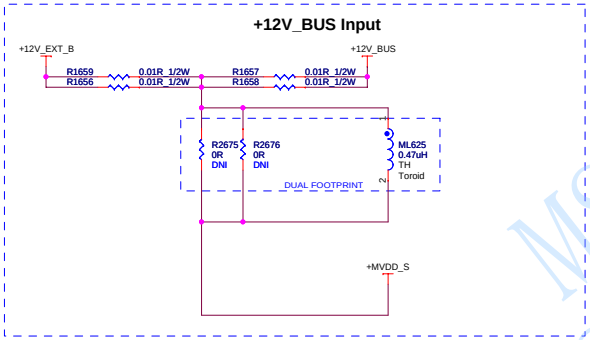
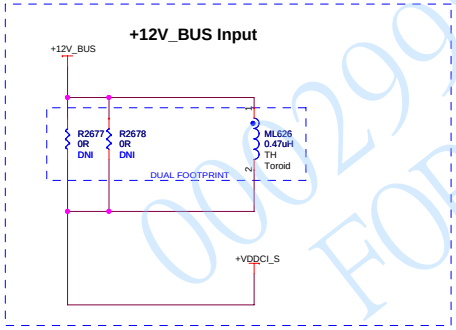
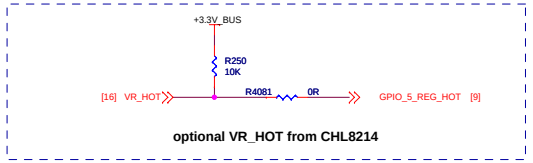
(21) CAYMEN POWER MANAGEMENT 2



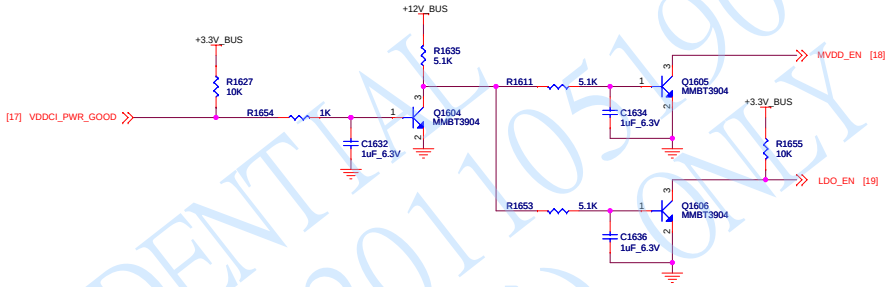


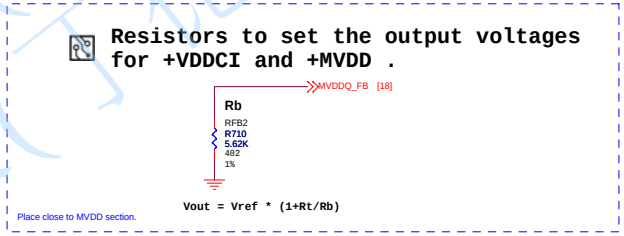


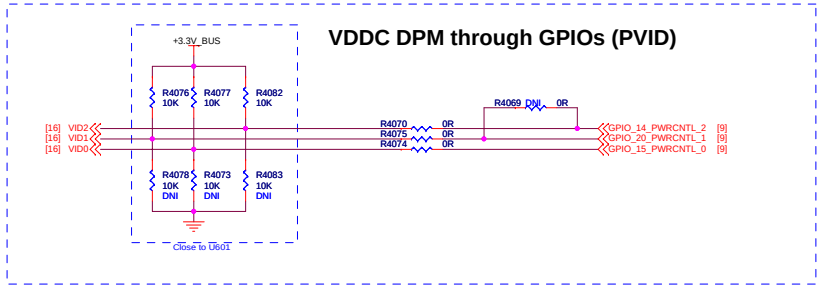




Power up Sequencing







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(22) CAYMEN Mechanical and Thermal Management

Use Q203 20200023006, R200, R215, D1719 and C3609 for cheaper fan controller. Requires big change in fan table.

Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.

Critial Temperature Fault

For one time CTF use R223 47k.
For resetable CTF use R223 2k.

CTF By-pass

To maximize fan output during CTF trigger.

Place close to its CTLR

This circuit provides a minimum voltage for the fan, independent of PWM input

For 4-WIRE FAN ONLY

For 2-WIRE FAN ONLY

Cheaper 2 wires fan control

Overlap MJ200 and J200

Header is 2mm, and it does not follow 2.54mm spacing as 4-pin PWM Fan Specification

MOSFET Heatsink MT

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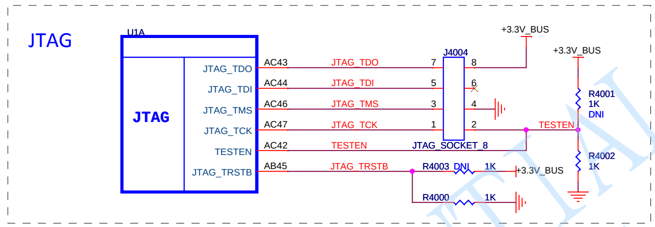
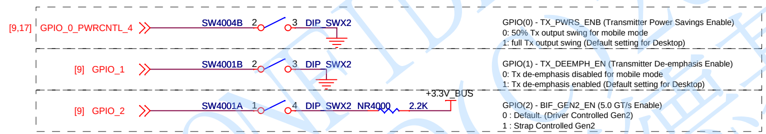
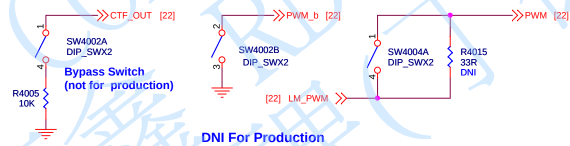
(23) CAYMEN Debug Circuits

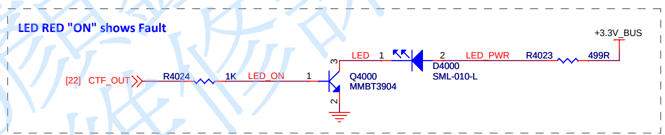


SWITCH CONNECTIONS TO PINSTRAPS





DNI For Production



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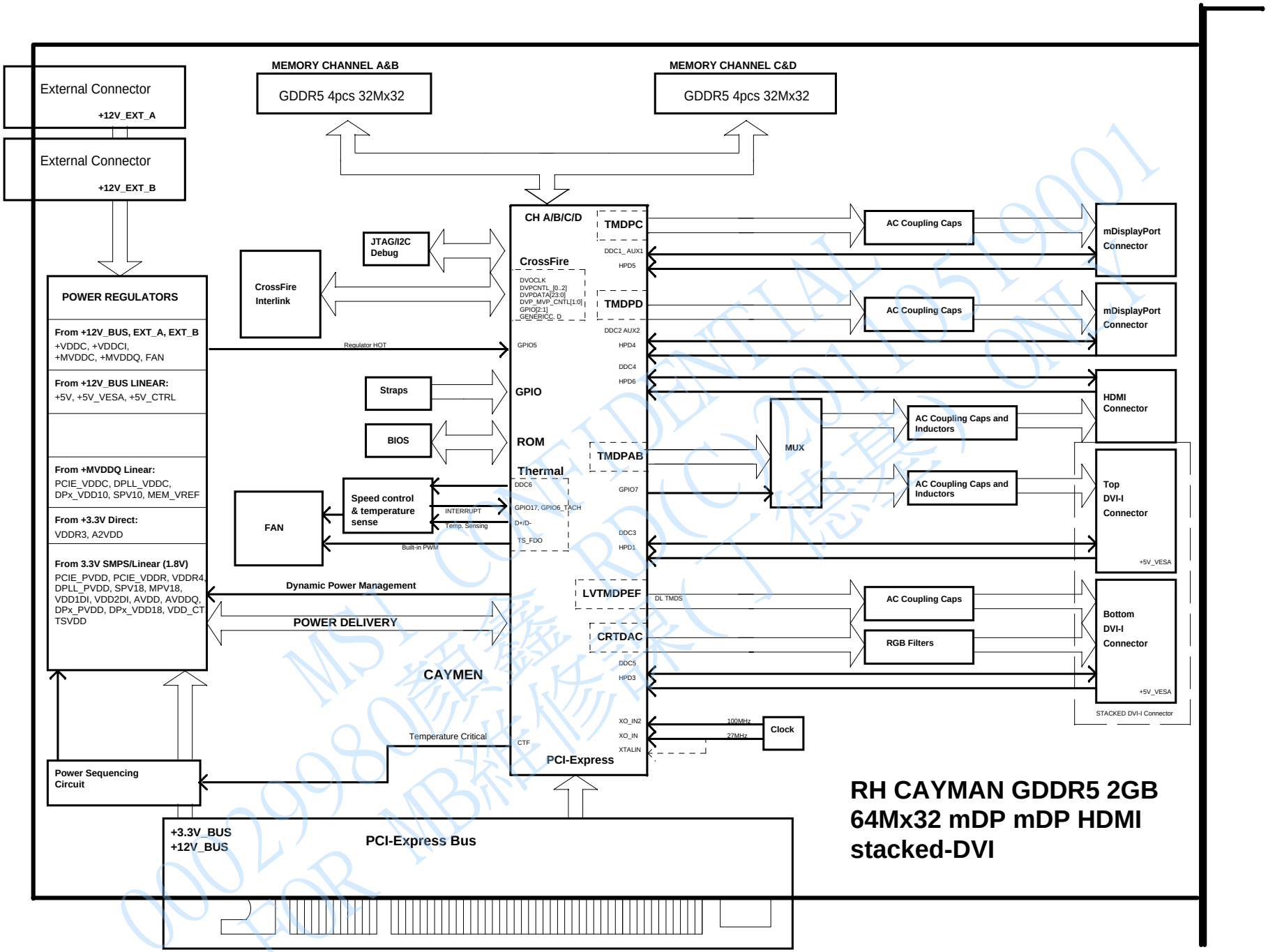

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Title	Block Diagram
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Title	Schematic No.	Date:
RH CAYMAN GDDR5 2GB 64Mx32 mDP mDP HDMI stacked-DVI	105-C205XX-00A	Friday, October 08, 2010

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 01

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION