# 電子類元件 零件承認書文件 CHECK LIST

零件廠商：UPI　　品名規格：US5650QQKI　UPI

技嘉料號：10TA1-085650-01R

| 項次 | 文件項目 |
|---|---|
| **Data Sheet 檢核項目** | |
| 1 | DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**) |
| 2 | 零件 Making 文字面說明 |
| 3 | 零件 Part Number 說明 |
| 4 | 零件 Qualification Test Report |
| 5 | 料件包裝方式及包裝 Label 之零件 Part number 說明 |
| 6 | UL Safety Report (If Request ) |
| 7 | 零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2** |
| 8 | 零件樣品 20PCS(Chipset 等高單價，至少 1PCS) |
| **9** | **電子零件承認基本調查表。註 3** |
| 10 | 以上資料電子檔為 PDF 檔，且是同 1 個 File |
| **GSCM 綠色產品管理系統-物料管制文件檢核清單** | |
| 物料管制文件 1 | GSCM 綠色產品管理系統：零件照片 |
| 物料管制文件 2 | GSCM 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4** |
| 物料管制文件 3 | GSCM 綠色產品管理系統：Data Sheet |
| **GSCM 綠色產品管理系統-MCD 表格** | |
| MCD 表格 | 物質內容宣告表格 (Material Content Declaration, MCD) |
| **其他文件 (僅適用電阻、電容類之系列元件)** | |
| 附件 1 | 危害物質測試報告 Test Report of Hazardous Substances。**註 5** |
| 附件 2 | 元件調查表 Component Composition Table |

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等

※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)

2.1. 基本需符合 JEDEC 規範

2.2. Ambient Temp. (Reflow Temp endurace): >225℃, 70 sec. 零件塑膠材質需 PA9T(含)等級以上

2.3. PASTE IN HOLE 零件塑膠材質需 PA9T(含)等級以上

※ **3. 電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G*,11T***

**非 IC 類：10C*,11C*,10L*,11L*,10X*,11X*,10R*,11B***

※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”

※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

# 電子零件承認基本調查表

**一、原物料規格/來源**

| 項次 | 部位名稱/規格 | 材質 | 原物料來源產地 |
|---|---|---|---|
| 1 | CHIP | 金屬 | TAIWAN |
| 2 | DIE ATTACH | EPOXY | JAPAN |
| 3 | LEAD FRAME | 金屬 | JAPAN |
| 4 | BONDING WIRE | 金屬 | JAPAN |
| 5 | MOLDING COMPOUND | EPOXY | TAIWAN |
| 6 | PLATING | 鍍錫 | TAIWAN |

**二、晶圓廠(非 IC 類免填)**

| 項次 | 工廠名稱 | 生產產地 | Wafer (吋) | 投產率(%) | 自有/外包 |
|---|---|---|---|---|---|
| 1 | VIS(世界先進) | TW | 8 | 40 | 外包 |

**三、封裝廠(IC 類)；成品之生產製造工廠(非 IC 類)**

| 項次 | 工廠名稱 | 生產產地 | 投產比率(%) | 自有/外包 |
|---|---|---|---|---|
| 1 | GTK (超豐) | TW | 50 | 外包 |
| 2 | ASE-KS(日月光) | KS | 50 | 外包 |
| 3 | | | | |

**四、產能**

| 總產能(月/PCS) | 可供技嘉產能(月/PCS) |
|---|---|
| NA | NA |

※ 1. IC 類之晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 2. 非 IC 類零件之成品生產製造工廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 3. 以上資訊欄位若有不足，可自行增加行數

# ADC Prefilter with Analog Multiplexer

## General Description

The uS5650Q is a 4-Channel Analog prefilter and Multiplexer. This 4 channel device is intended to condition single and differential signals at bus voltages to a range appropriate for sampling with a low voltage ADC. Power supply operates from 2.8V to 3.8V.

## Ordering Information

| Order Number | Package | Remark |
|---|---|---|
| uS5650QQKI | WQFN4x4-32L | |

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

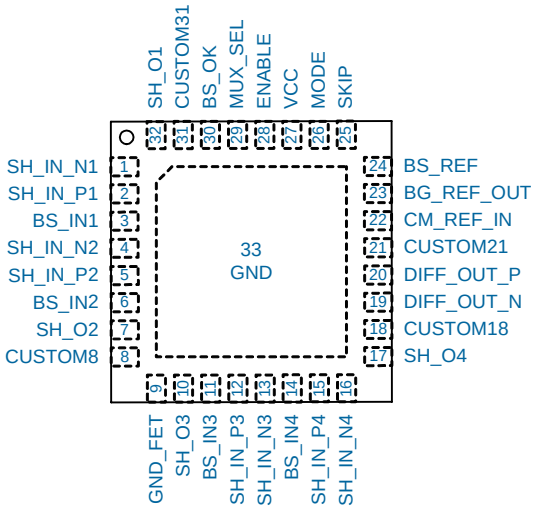
## Applications

- **Computers**
- **Power Management**
- **Telecom Equipment**
- **Battery Chargers**
- **Power Supplies**
- **Test Equipment**

## Features

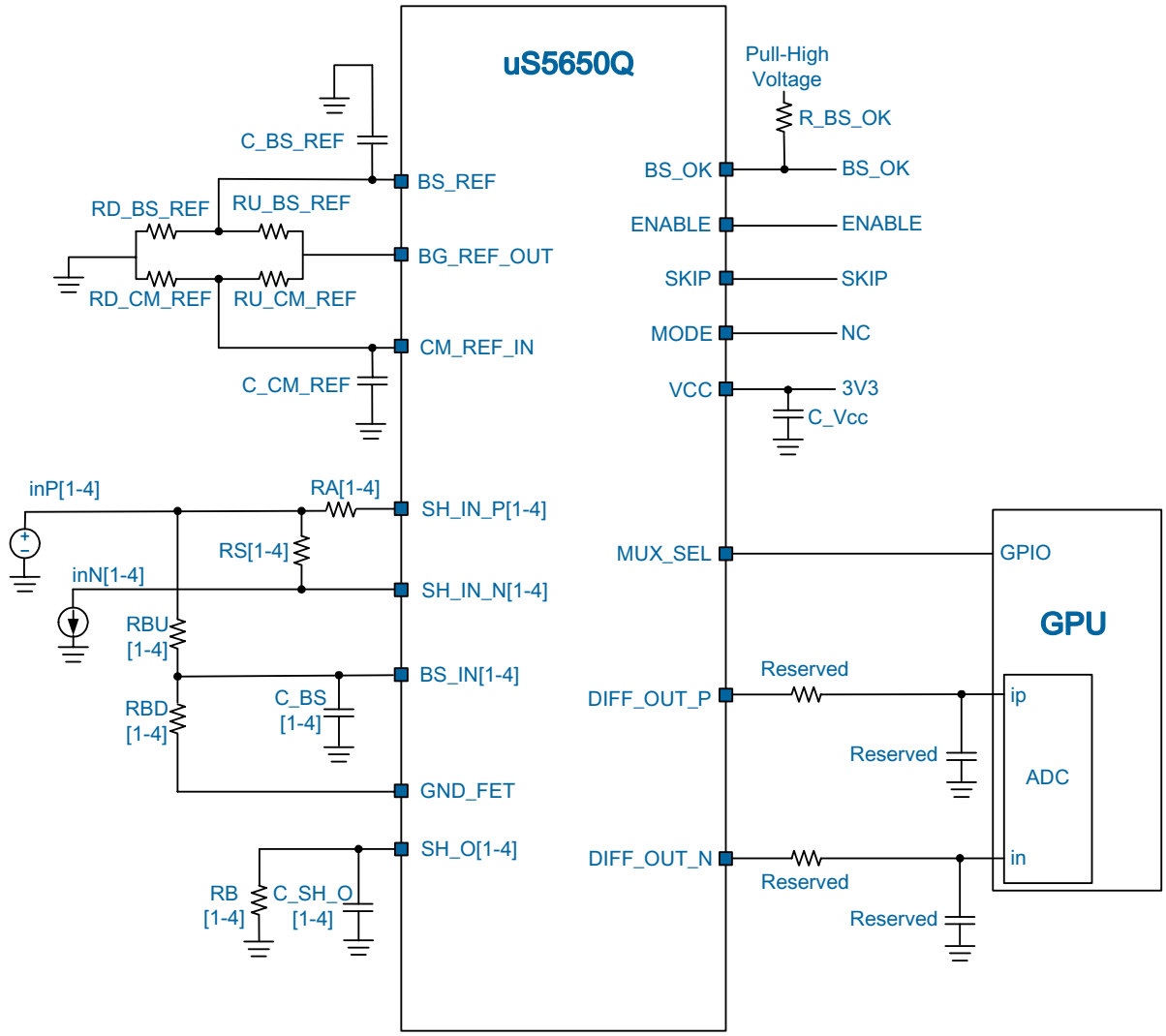
- **4 Differential to Single-Ended Trans-Conductance Amplifier**
- **2*4-to-1 (1 for Bus, 1 for Shunt) Analog Multiplexer with Single Bit for MUX Select**
- **Single-Ended to Differential Converter with Buffered Input Reference Voltages**
- **Strap Selectable to Operate the Device by Itself or in a Pair**
- **Enable Input that Enables Active Devices and Controls an Internal FET to Ground**
- **Operating Shunt Voltage: 5V to 30V**
- **Max Bus Voltage: 30V**
- **Power Supply Operation: 2.8V to 3.8V**

## Pin Configuration



## Typical Application Circuit

4-Channel Application Circuit (Stand-Alone Mode)

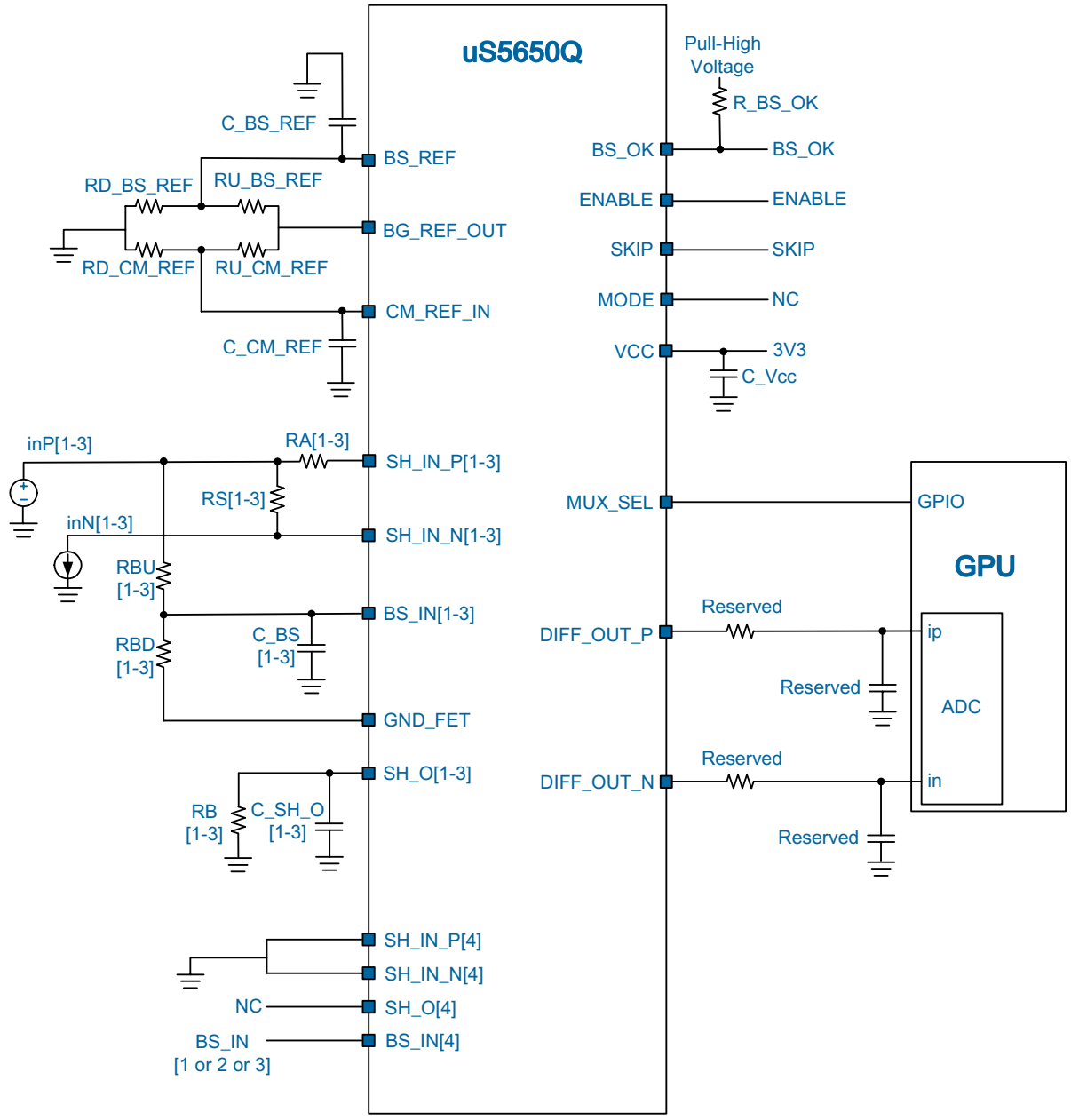



Note:

There are two differential output reserved resistance(0.86Ω~8.6Ω) and capacitance(22pF~82pF) which appears as a series RC with lumped equivalent.

## Typical Application Circuit

3-Channel Application Circuit (Stand-Alone Mode)



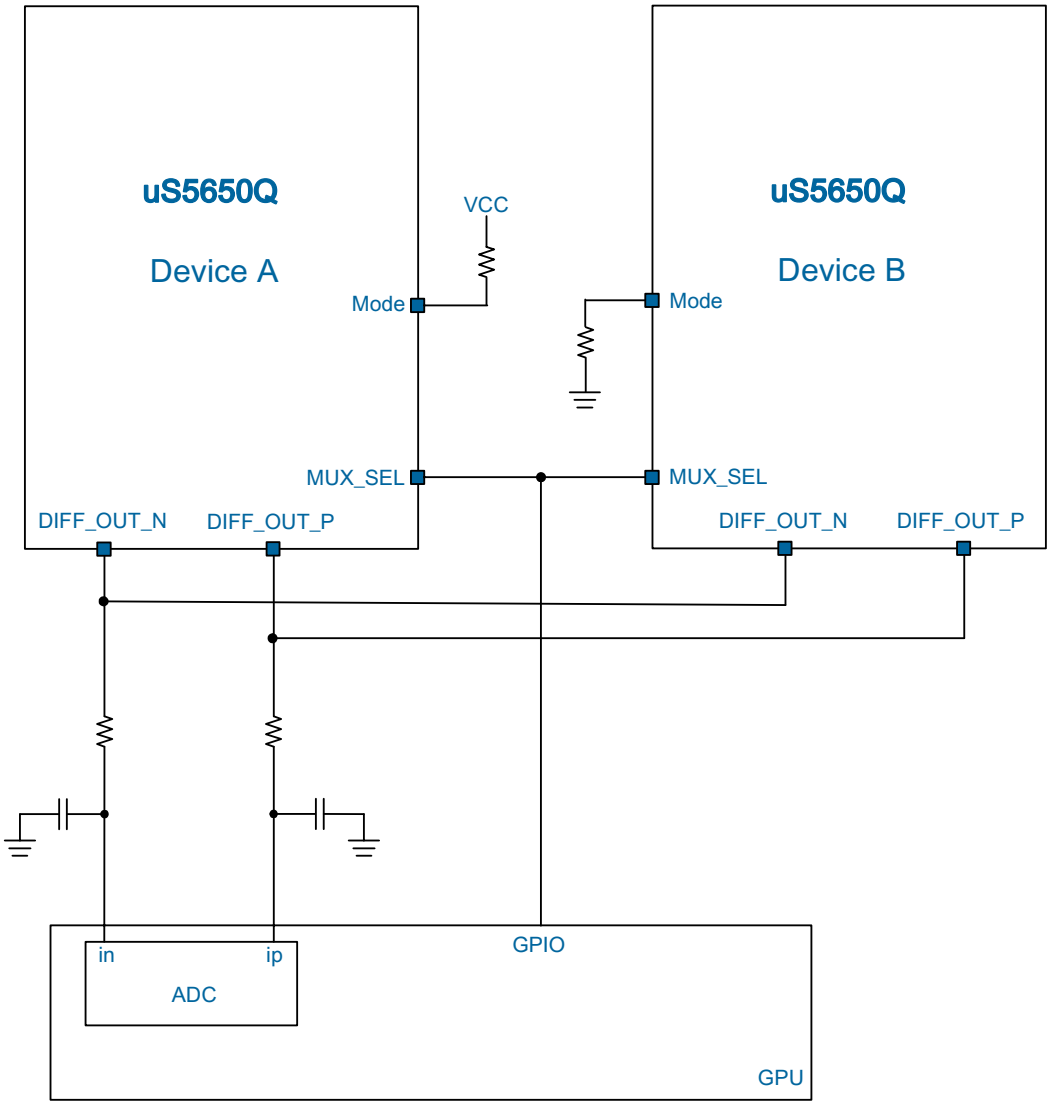

Note:

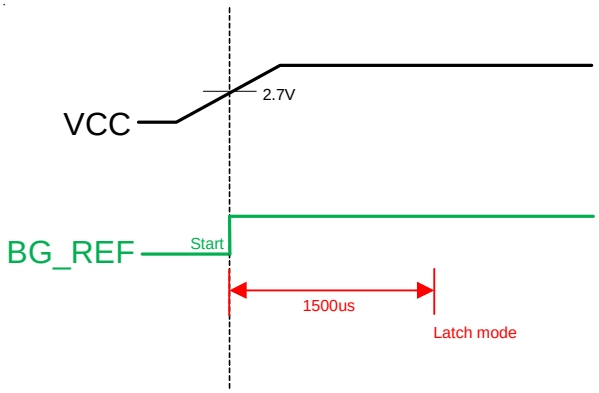
uS5650Q needs to incorporate at least 2 channels. Channel-reduction needs to start from channel 4.

If channel reduction is used in parallel mode, both devices will operate the same number of channels.

## Typical Application Circuit

Two Device Application Circuit




EN is individual related to the GPU signal instead of Mode and Vcc

## Functional Pin Description

| Pin No. | Pin Name | I/O | Pin Function |
|---|---|---|---|
| 1 | SH_IN_N1 | AI | **Negative Side of Shunt Input.** High impedance, high voltage, avoid floating. |
| 2 | SH_IN_P1 | AI | **Positive Side of Shunt Input.** High impedance, high voltage, avoid floating. |
| 3 | BS_IN1 | AI | **Analog Input for Bus Voltage Multiplexer.** Avoid floating. |
| 4 | SH_IN_N2 | AI | **Negative Side of Shunt Input.** High impedance, high voltage, avoid floating. |
| 5 | SH_IN_P2 | AI | **Positive Side of Shunt Input.** High impedance, high voltage, avoid floating. |
| 6 | BS_IN2 | AI | **Analog Input for Bus Voltage Multiplexer.** Avoid floating. |
| 7 | SH_O2 | AO | **Current Source Proportional to Shunt Voltage.** Low Voltage. |
| 8 | CUSTOM8 | -- | **NC.** For custom functions. |
| 9 | GND_FET | AI | **Ground to FET.** It can be connected to internal FET to short to GND. |
| 10 | SH_O3 | AO | **Current Source Proportional to Shunt Voltage.** Low Voltage |
| 11 | BS_IN3 | AI | **Analog Input for Bus Voltage Multiplexer.** Avoid Floating. |
| 12 | SH_IN_P3 | AI | **Positive Side of Shunt Input.** High impedance, high voltage, avoid floating. |
| 13 | SH_IN_N3 | AI | **Negative Side of Shunt Input.** High impedance, high voltage, avoid floating |
| 14 | BS_IN4 | AI | **Analog Input for Bus Voltage Multiplexer.** Avoid Floating. |
| 15 | SH_IN_P4 | AI | **Positive Side of Shunt Input.** High impedance, high voltage, avoid floating |
| 16 | SH_IN_N4 | AI | **Negative Side of Shunt Input.** High impedance, high voltage, avoid floating |
| 17 | SH_O4 | AO | **Current Source Proportional to Shunt Voltage.** Low Voltage |
| 18 | CUSTOM18 | -- | **NC.** For custom functions. |
| 19 | DIFF_OUT_N | AO | **Differential Output.** Negative Terminal. |
| 20 | DIFF_OUT_P | AO | **Differential Output.** Positive Terminal. |
| 21 | CUSTOM21 | -- | **NC.** For custom functions. |
| 22 | CM_REF_IN | AI | **Common Mode Reference.** |
| 23 | BG_REF_OUT | AO | **Bandgap Analog Out.** |
| 24 | BS_REF | AI | **Reference Input for the Bus Ready Comparator.** |
| 25 | SKIP | AI | **Mask for BS_OK.** |
| 26 | MODE | DI | **Mode Selection for stand-alone. As device-A, or as device-B** |
| 27 | VCC | AI | **VCC of device.** |
| 28 | ENABLE | DI | **Enable.** It takes device out of sleep and opens GNDFET. |
| 29 | MUX_SEL | DI | **Multiplexer Selection.** |
| 30 | BS_OK | DO | **Open Drain Digital Output.** Indicating the bus is OK. |
| 31 | CUSTOM31 | -- | **NC.** For custom functions. |
| 32 | SH_O1 | AO | **Current Source Proportional to Shunt Voltage.** Low Voltage. |
| EP | GROUND [1] | -- | **Power GND of Device.** |

## Functional Block Diagram

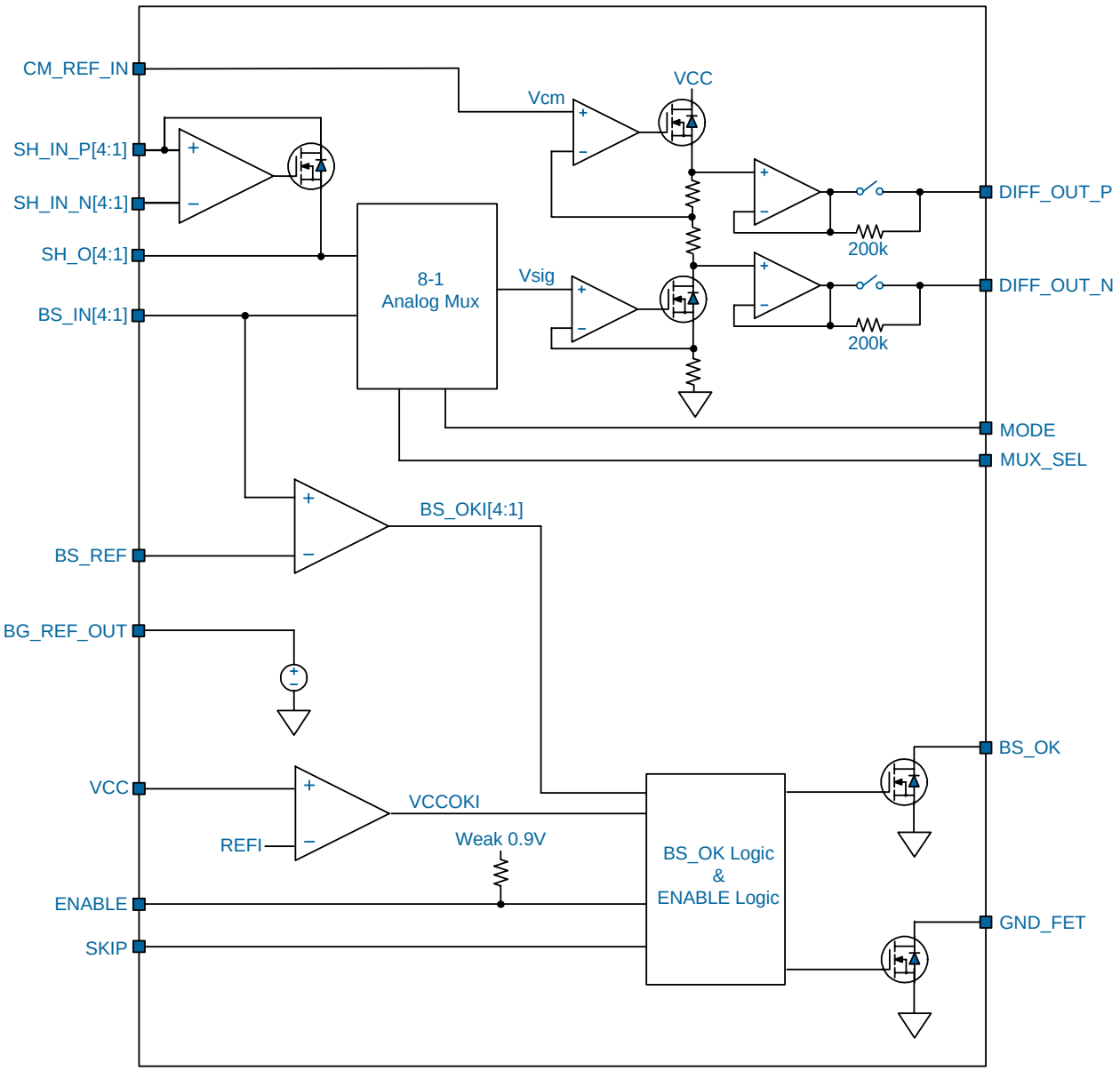



Diagram of device in use with passives and GPU. Circuits drawn inside the device are representative of its function; implementation can differ. Values are provided for approximate reference only and will change based on exact application (see Inputs, Analog Multiplexer, and Differential Output ) or uPI's choice in certain device parameters.

### Inputs, Analog Multiplexer, and Differential Output

For a 4-channel device, there will be 4 shunt inputs and 4 bus inputs. The shunt input is a transconductance architecture of which SH_IN_P and SH_IN_N are positive and negative terminals respectively. SH_O is the output of the transconductance which allows the gain to be set. This pin also internally connects to the multiplexer input. BS_IN is a straight connection to the multiplexer input.

The output of the multiplexer will feed a single to differential stage that drives the GPU. A common mode is provided by CM_REF_IN. DIFF_OUT_P and DIFF_OUT_N drives Vcm+4/3*Vsig and Vcm-4/3*Vsig respectively where Vsig is the output of the multiplexer which can be the voltage on either SH_O or BS_IN. It can also be different between the shunt and bus inputs. Note that since Vsig will always be positive, DIFF_OUT_P will always be equal or higher potential than DIFF_OUT_N.

The load that DIFF_OUT needs to drive is dominated by board and GPU package traces and will have a lump equivalent fall in this range:

R: 860~8600mΩ

C: 22~82pF

### Shunt Configuration

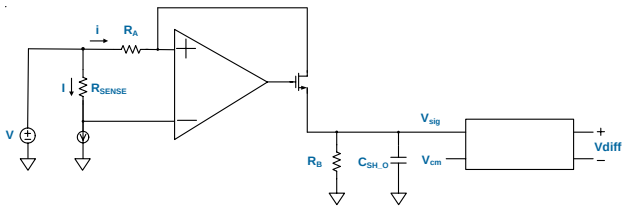



Figure 1. Shunt Configuration

$V_{diff} = 8/3V_{SIG}$

$$V_{SIG} = \frac{R_B}{R_A} \times R_{SENSE} \times I$$

$$\text{Shunt Gain} = \frac{V_{SIG}}{R_{SENSE} \times I} = \frac{R_B}{R_A}$$

If Full Range $V_{SIG}$ = 0.3V, $R_B$ = 1020, $R_A$ = 340,

$R_{SENSE}$ = 1mΩ

=>Shunt Gain = 3

=> Full Range Shunt Voltage(V)

$$= V_{SENSE\_FULL} = \frac{0.3}{3} \cong 0.1(V)$$

Full Range Current(A) =

$$\frac{V_{SENSE\_FULL}}{R_{SENSE}} = \frac{0.1}{1m} \cong 100\ (A)$$

### Bus Configuration

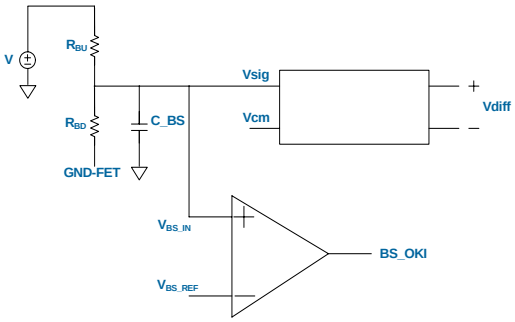



Figure 2. Bus Configuration

$V_{diff} = 8/3V_{SIG}$

$$V_{SIG} = \frac{R_{BD}}{R_{BU} + R_{BD}} \times V$$

$$BusGain = \frac{V_{SIG}}{V} = \frac{R_{BD}}{R_{BU} + R_{BD}}$$

$$\frac{1}{BusGain} = \frac{R_{BU} + R_{BD}}{R_{BD}}$$

If Full Range $V_{SIG}$ = 0.3V, $R_{BD}$ = 200, $R_{BU}$ = 15.8k,

$$\Rightarrow \frac{1}{BusGain} = \frac{200 + 15.8k}{200} = 80$$

=>Full Range Bus Voltage(V) = 80 x 0.3 = 24(V)

### Multiplexer Select Operation

The multiplexer selection is done through a single bit digital input clocked. The device will monitor the input and cycle through the different op-amps in a fixed sequence. The sequence that the multiplexer must follow starts with the bus of the first enumerated before altering to its shunt. It then cycles likewise through the bus/shunt pairs in order of enumeration repeating itself after the shunt of the last active channel has been passed through the multiplexer. The multiplexer will repeat the cycle indefinitely until either a timeout condition is detected or a disable is asserted.

Devices can be configured to work in one three modes of operation: stand-alone, as device-A, or as device-B using the MODE pin. In stand-alone operation, the device will cycle through op-amps all clock cycles. As device-A, the device will respond to the first set of clock cycle and go into high impedance while device-B responds to the subsequent clocks. Two devices, one configured as device-A and another as device-B will share MUX_SEL and DIFF_OUT lines on the PCB.

Devices can also be configured to work in reduced channel count. By floating a given SH_O, channels of equal and higher enumeration will remain unused. Unused channels will behave as if they do not exist and be skipped over by the multiplexer. uS5650Q needs to corporate at least 2 channels. Channel-reduction needs to start from channel 4. If channel reduction is used in parallel mode, both devices will operate the same number of channels. Reducing the channel count of multiplexer will NOT impact Bus Comparator operation.

The Diff Output is VCM when ENABLE pin pulls low and MUX_SEL not start up. Stopping MUX_SEL over 35us will let Diff Output to VCM. Rising edge of MUX_SEL to when DIFF_OUT achieve 6mV error is within 250ns

Table 1.

| Mode Pin Connection | Operation Mode |
|---|---|
| Pull high to VCC with R < 10kΩ (Mode > 2V) | Device-A |
| Pull low to GND with R < 10kΩ (Mode < 0.6V) | Device-B |
| Floating | Stand-Alone |

Table 2.

| 4-Channel Stand-Alone Mode | |
|---|---|
| **Clock Cycle** | **Diff Output** |
| 0 | VCM |
| 1 | Ch1 Bus |
| 2 | Ch1 Shunt |
| 3 | Ch2 Bus |
| 4 | Ch2 Shunt |
| 5 | Ch3 Bus |
| 6 | Ch3 Shunt |
| 7 | Ch4 Bus |
| 8 | Ch4 Shunt |
| 9 | Ch1 Bus |

Table 3.

| 6-Channel Parallel Mode | | |
|---|---|---|
| **Clock Cycle** | **Diff Output (Dev A)** | **Diff Output (Dev B)** |
| 0 | VCM | VCM |
| 1 | Ch1 Bus | VCM |
| 2 | Ch1 Shunt | VCM |
| 3 | Ch2 Bus | VCM |
| 4 | Ch2 Shunt | VCM |
| 5 | Ch3 Bus | VCM |
| 6 | Ch3 Shunt | VCM |
| 7 | VCM | Ch1 Bus |
| 8 | VCM | Ch1 Shunt |
| 9 | VCM | Ch2 Bus |
| 10 | VCM | Ch2 Shunt |
| 11 | VCM | Ch3 Bus |
| 12 | VCM | Ch3 Shunt |
| 13 | Ch1 Bus | VCM |

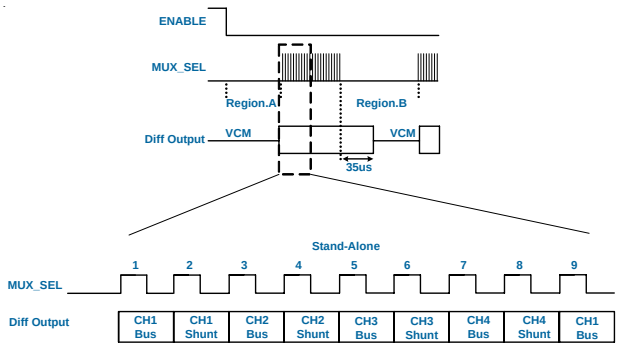



Figure 3.

### Bus Comparator

Operating independently from the multiplexer, the device will also have comparators for each bus inputs and Vcc. If the BS_IN of all active channels compare positively against a reference on BS_REF, Vcc compares positively against an internally generated reference and the SKIP pin is not

being asserted low, it will release an open drain output BS_OK. As much as feasible, BS_OK should remain low impedance logic low even when Vcc goes below operating threshold. SKIP needs to be high voltage tolerant and can be used to power BS_OK pull down in cases where Vcc becomes low.

### Bandgap Reference

BG_REF_OUT provides a high accuracy bandgap reference from which BS_REF and CM_REF_IN can be derived.

### Ground FET

GND_FET is a switch that connects the bus divider to ground that can be disconnected to break any leakage path between input power and ground.

### Enable

Three logic levels and their behavior defined as follows. Note that enable logic levels are defined differently from expected convention.

Table 4.

| Enable State | Description |
|---|---|
| Low | Fully Functional |
| Tri-state | Limited Function.<br>Only BG_REF_OUT, GND_FET, BS_OK are functional . All other biasing should be minimized. In this state, DIFF_OUT will always be high impedance and MUX_SEL logic will be ignored. |
| High | Standby.<br>In addition to saving features of Limited Function, GND_FET will be disconnected and additional power saving where possible. |

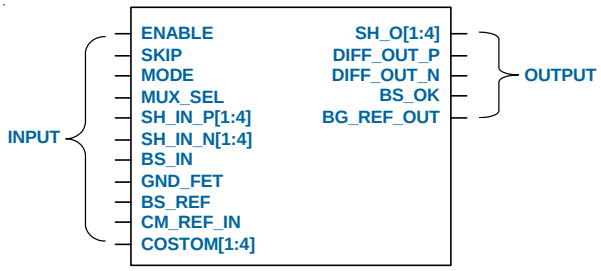



Figure 4.

Complete logic table of ENABLE, SKIP and BS_IN is as follows,

Table 5.

| ENABLE | OTP | VCC | BS_IN | SKIP | BS_OK |
|---|---|---|---|---|---|
| X | H | X | | H | L |
| H | L | X | | | |
| T/L | | L | X | | |
| | | X | L | | |
| | | H | | | H (open drain) |
| X | | | | L | |

Table 6.

| State | SH_O[1:4] | DIFF_OUT_P/N | BS_OK | BG_REF_OUT | T/O Counter |
|---|---|---|---|---|---|
| UVLO | Low by Ext Resistor | High Z | See Table 5 | Low | Reset |
| OTP | Low by Ext Resistor | High Z | See Table 5 | Keep | Reset |

### $V_{cc}$ and GND

The device has a VCC pin and GND will use the thermal pad. When the device reaches its Vcc threshold, there can be a delay during before Full Function operation is expected and MUX_SEL will not toggle. It is expected that MODE and channel determination will happen during this delay.

### Customization

Those pins should be floated in production use.

## Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC ---------- 2.8V to 6V
Safety Temperature ---------- -40°C to 125°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
CDM (Charged Device Mode) ---------- 1kV

## Thermal Information

Package Thermal Resistance (Note 3)
WQFN4x4-32L $\theta_{JA}$ ---------- 37°C/W
WQFN4x4-32 $\theta_{JC}$ ---------- 20°C/W
Power Dissipation, $P_D$ @ $T_A$ = 25°C
WQFN4x4-32 L ---------- 1W

## Recommended Operation Conditions

(Note 4)

Supply Input Voltage, VCC ---------- 2.8V to 3.8V
Safety Temperature ---------- -40°C to 105°C
Operating Junction Temperature Range ---------- -40°C to +105°C
Operating Ambient Temperature Range ---------- -40°C to +85°C

**Note 1.** Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.** $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Safe Voltage (SH_IN_P, SH_IN_N) | | | -- | -- | 30 | V |
| Operating Voltage (SH_IN_P, SH_IN_N) | | | 5 | -- | 30 | V |
| Operating Voltage (SH_O) | | | -- | -- | 0.3 | V |
| Current Capability (SH_O) | | | 1 | -- | -- | mA |
| Valid Load [1] (SH_O) | | | -- | -- | 2k | Ω |
| SH_O Floating Detection Resistance | | | 10k | -- | -- | Ω |
| Capacitance Load (SH_O_C) | | | 2.2 | -- | 100 | nF |
| Safe Voltage (BS_IN) | | | -- | -- | 30 | V |
| Reference Voltage for the Bus (BS_REF) | | | -- | -- | 1 | V |
| Comparator Offset Voltage | | | -3 | -- | 3 | mV |
| Supported CM_REF_IN | | | 565 | 850 | 885 | mV |
| DIFF_LOAD Capacitive Load Drive Strength [2][3] | | | 22 | -- | 82 | pF |
| DIFF_OUT Safety Voltage | | | -- | -- | 1.8 | V |
| Mux_Sel VIH | | | 1.4 | -- | -- | V |
| Mux_Sel VIL | | | -- | -- | 0.4 | V |
| Mux_Sel High/Low Duration | | | 50 | -- | -- | ns |
| Mux_Sel Valid Period | | | 0.185 | -- | 11 | us |
| Mux_Sel Timeout Reset | | | 35 | -- | -- | us |
| BS_OK Logic Low Impedance | | | -- | -- | 100 | Ω |
| Bandgap Level [4] | | | 1.274 | 1.300 | 1.326 | V |
| Safe Voltage (GND_FET) | | | -- | -- | 30 | V |
| Tristate Input Impedance | | | 100k | -- | -- | Ω |
| Enable/SKIP VIH [7] | | | 1.4 | -- | -- | V |
| Enable/SKIP VIL [7] | | | -- | -- | 0.4 | V |
| SKIP Operating Voltage | | | -- | -- | 5 | V |
| Vcc to Full Function Delay | | | -- | -- | 2 | ms |
| Standby or Limited Function to Full Function | | | -- | -- | 40 | us |
| GNDFET On-resistance | | | -- | -- | 10 | Ω |

## Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Device IDDQ Fully Functional | | | -- | 1.6 | -- | mA |
| Device IDDQ Limited Function | | | -- | 0.25 | -- | mA |
| Device IDDQ Disabled | | | -- | 0.25 | -- | mA |
| Vcc Threshold Reference for BS_OK Input [5] | | | 2.6 | -- | 2.8 | V |
| Vcc for BS_OK Low Impedance [6] | | | 1.0 [8] | -- | 3.8 | V |
| Vcc Hysteresis for BS_OK Input | | | 100 | 150 | 200 | mV |
| BS_OK Comparator Hysteresis | | | 15 | 20 | 25 | mV |

[1] Impedances larger than this range can be considered floating for channel count selection

[2] Referenced to Ground. Both pins DIFF_OUT pins need to be able to individually drive this load

[3] In parallel mode, this will include the stub leading to the other output but not its output impedance

[4] Exact values can be defined manufacturer by should fit within a +/-2% tolerance of some nominal

[5] Vcc detection for BS_OK must trip in this trip. Device can be either operational or not in this range

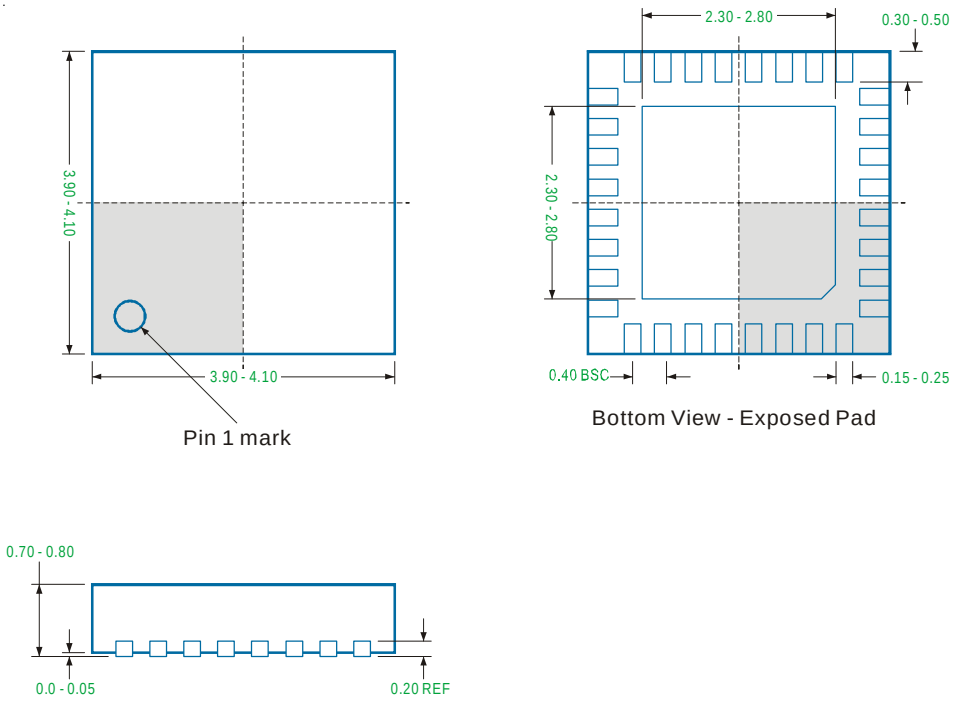
[6] Vcc range where BS_OK can maintain logic low impedance

[7] Enable driving capability should greater than 2 uA

[8] Only when SKIP voltage exceeds 2.8V, the minimum is 1.0V.

## Package Information

WQFN4x4 - 32L




Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

## Important Notice

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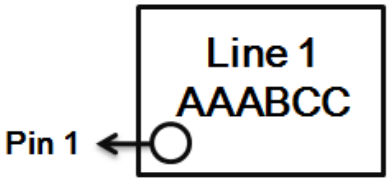
# Top Marking Rule




Line 1 : Product Code

| Part No. | Product Code |
|---|---|
| US5650QQKI | uS5650Q |

Line 2 :

AAA - uPI internal trace code

BCC - Date Code, rules as below:

B：Last one of western calendar year (0~9), ex. 2017=7, 2018=8

CC：weekly:

First half of the week : Sunday ~ Wednesday

Second half of the week : Thursday ~ Saturday

| First half of the week | Second half of the week | First half of the week | Second half of the week | First half of the week | Second half of the week |
|---|---|---|---|---|---|
| 01 | AA | 19 | AU | 37 | BN |
| 02 | AB | 20 | AV | 38 | BP |
| 03 | AC | 21 | AW | 39 | BQ |
| 04 | AD | 22 | AX | 40 | BR |
| 05 | AE | 23 | AY | 41 | BS |
| 06 | AF | 24 | AZ | 42 | BT |
| 07 | AG | 25 | BA | 43 | BU |
| 08 | AH | 26 | BB | 44 | BV |
| 09 | AJ | 27 | BC | 45 | BW |
| 10 | AK | 28 | BD | 46 | BX |
| 11 | AL | 29 | BE | 47 | BY |
| 12 | AM | 30 | BF | 48 | BZ |
| 13 | AN | 31 | BG | 49 | CA |
| 14 | AP | 32 | BH | 50 | CB |
| 15 | AQ | 33 | BJ | 51 | CC |
| 16 | AR | 34 | BK | 52 | CD |
| 17 | AS | 35 | BL | | |
| 18 | AT | 36 | BM | | |

# WQFN4x4 Package

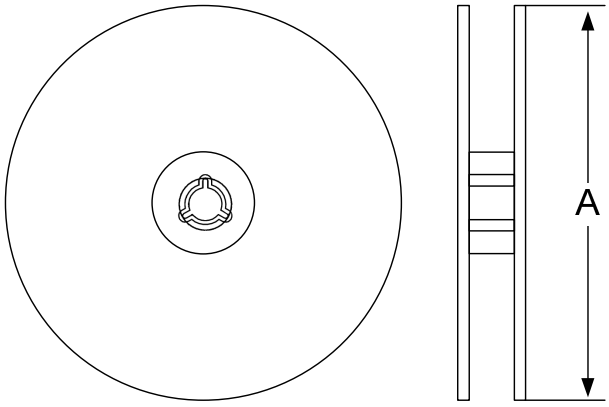
***Definition:***

***QFN = Quad Flat No Lead***

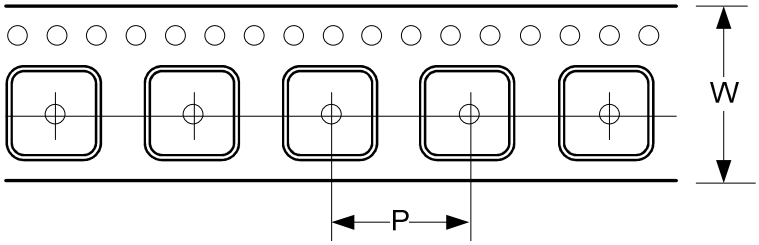
*W Type= Very Very Thin Package(Thickness = 0.75 ± 0.05mm)*

## *Tape & Reel Drawing*

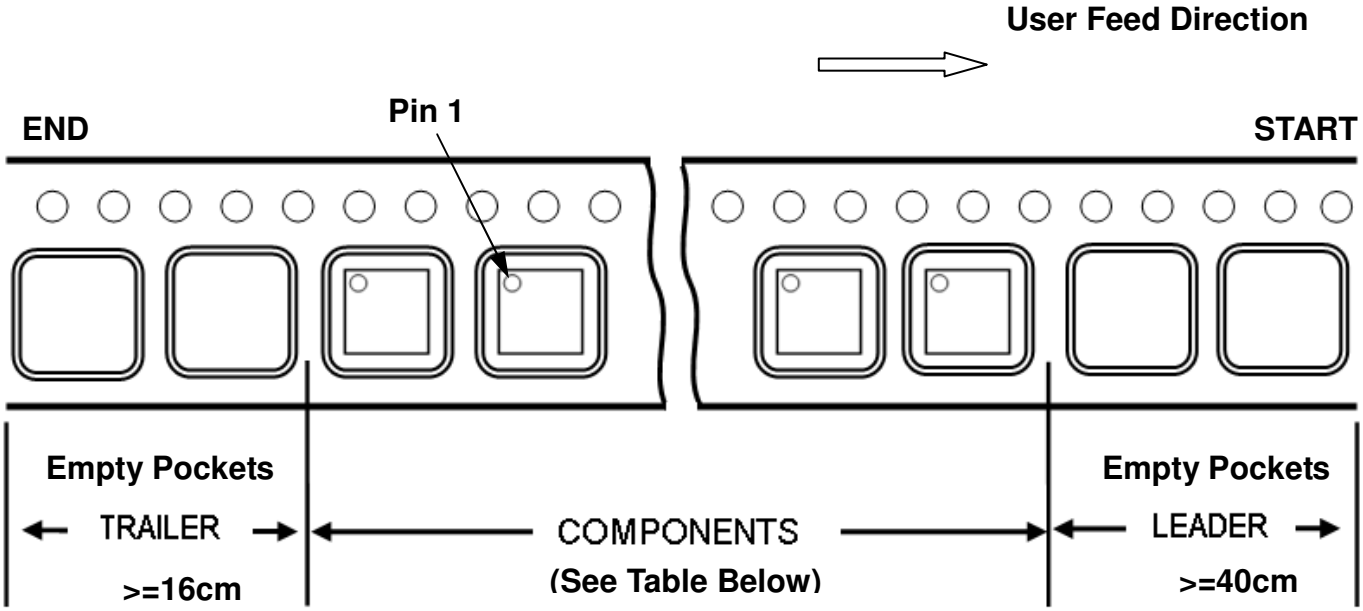
### Lock Reel



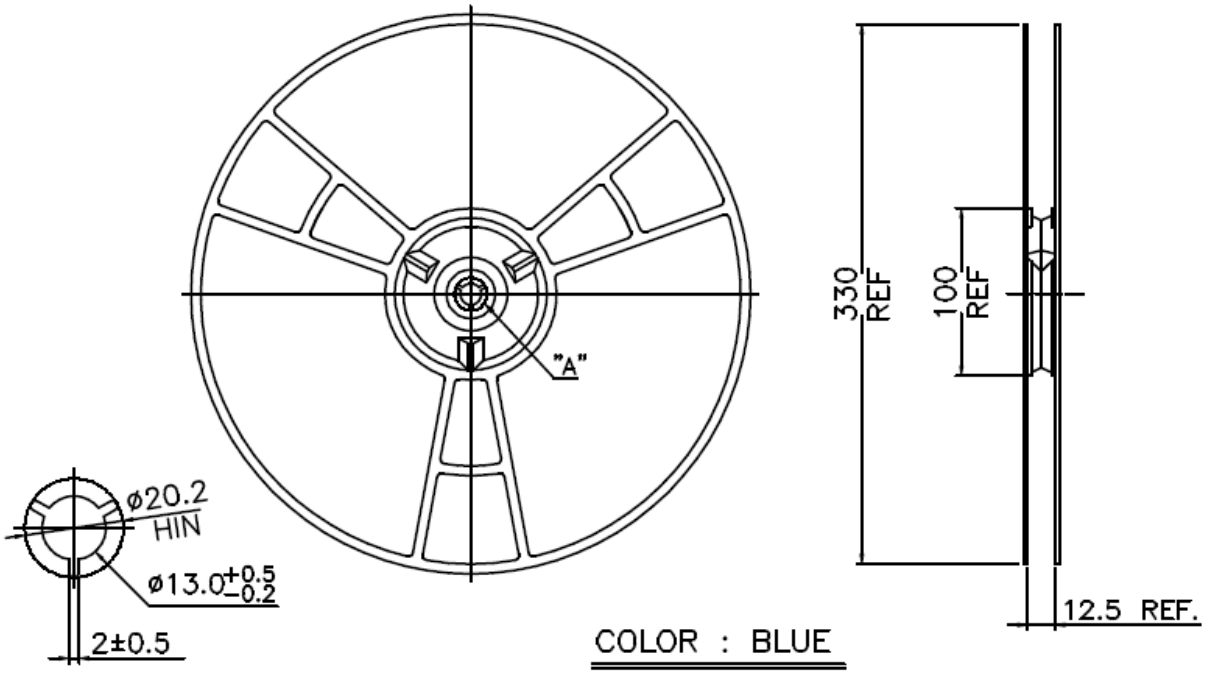

### Carrier Tape

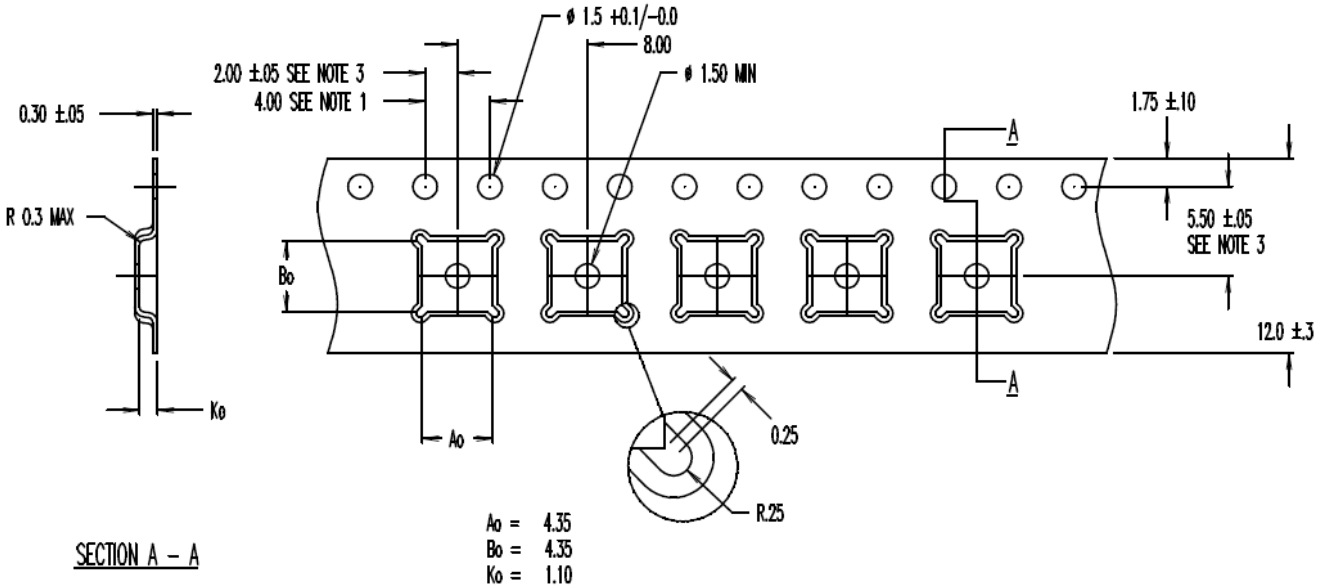



### Packing Illustration



## Carrier Tape Drawing



## Packing Quantity List

| PKG Type<br>Body Size | Reel Diameter(A)<br>(inch/mm) | Carrier Width(W)<br>(mm) | Carrier Pitch(P)<br>(mm) | Reel Quantity<br>(pcs) | Remark |
|---|---|---|---|---|---|
| WQFN 4x4 | 13 / 330 | 12 | 8 | 2500 | |

## *Packaging Drawing*

### Barcode Label – Apply for Reel/Al Bag/Inner Box and Outer Carton


P/N：uPI Part Number

LOT：Wafer Lot Number

QTY：Packing Quantity

D/C：Manufacturing Date Code

DATE：Packing Date

Note：For Internal Use Only

### Inner Box

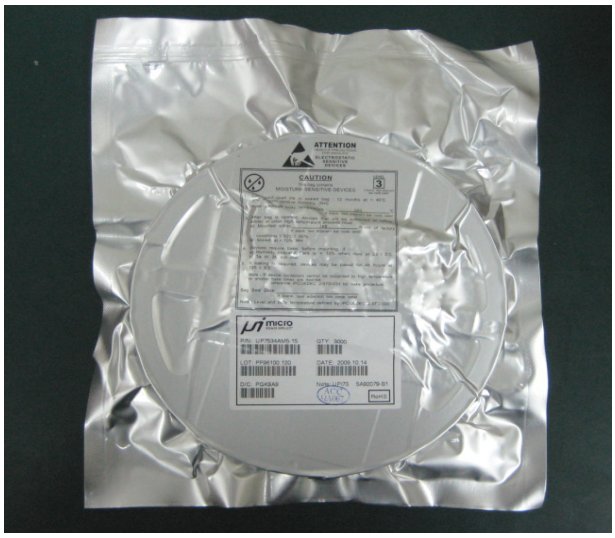
Box (13” Reel 355 x338 x 50 mm)

### Outer Carton

Carton A (382 x 283 x390 mm )

## Package Storage Condition:

- Vacuum Sealed into Moisture Barrier Bag and Meet MSL Level 3 requests.
- Comply with J-STD-033 standard.




- Storage Condition

  Vacuum Sealed : 12 months at <40℃ and 90%RH

  Bag Opened : Within 168 hrs at < 30℃ / 60%RH

- Baking Condition

  Re-Baking @ 125℃ +/- 5 ℃, 48hrs for IC only;

  Floor life begins counting at time =0 after Re-Baking.

  The times of Re-Baking: 2 times, Max.

## *Halogen-Free Package Peak Reflow Temperatures*

| Package Thickness | Volume $mm^3$ < 350 | Volume $mm^3$ 350 -2000 | Volume $mm^3$ > 2000 |
|---|---|---|---|
| < 1.6 mm | 260 +0 °C | 260 +0 °C | 260 +0 °C |
| 1.6 mm - 2.5 mm | 260 +0 °C | 250 +0 °C | 245 +0 °C |
| ≧ 2.5 mm | 250 +0 °C | 245 +0 °C | 245 +0 °C |

## *IR Reflow Profile*

| Profile Feature | Halogen-Free Assembly |
|---|---|
| Average Ramp-uP Rate ($TS_{max}$ to Tp) | 3 °C/second max. |
| Preheat<br>- Temperature Min ($TS_{min}$)<br>- Temperature Max ($TS_{max}$)<br>- Time ($TS_{min}$ to $TS_{max}$) | <br>150 °C<br>200 °C<br>60-180 Seconds |
| Time Maintained above<br>- Temperature (TL)<br>- Time (tL) | <br>217 °C<br>60-150 Seconds |
| Peak/Classification Temperature (Tp) | <=260 °C |
| Time Within 5 °C of actual Peak Temperature (tp) | 20-40 seconds |
| Ramp-Down Rate | 6 °C/second max. |
| Time 25 °C to Peak Temperature | 8 minutes max. |