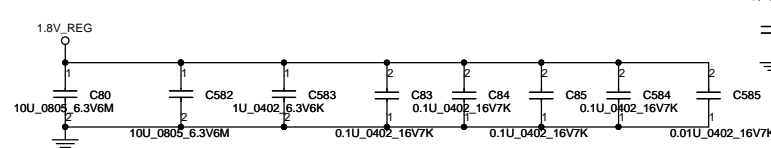
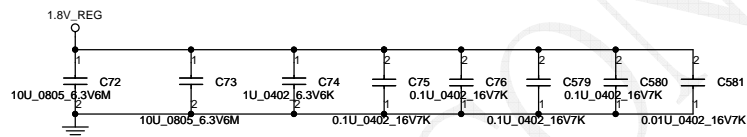
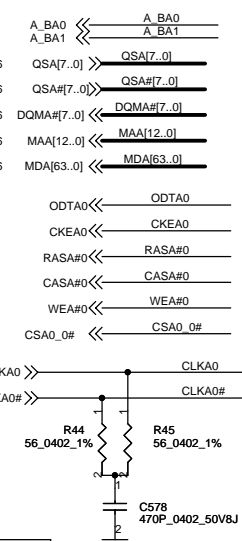
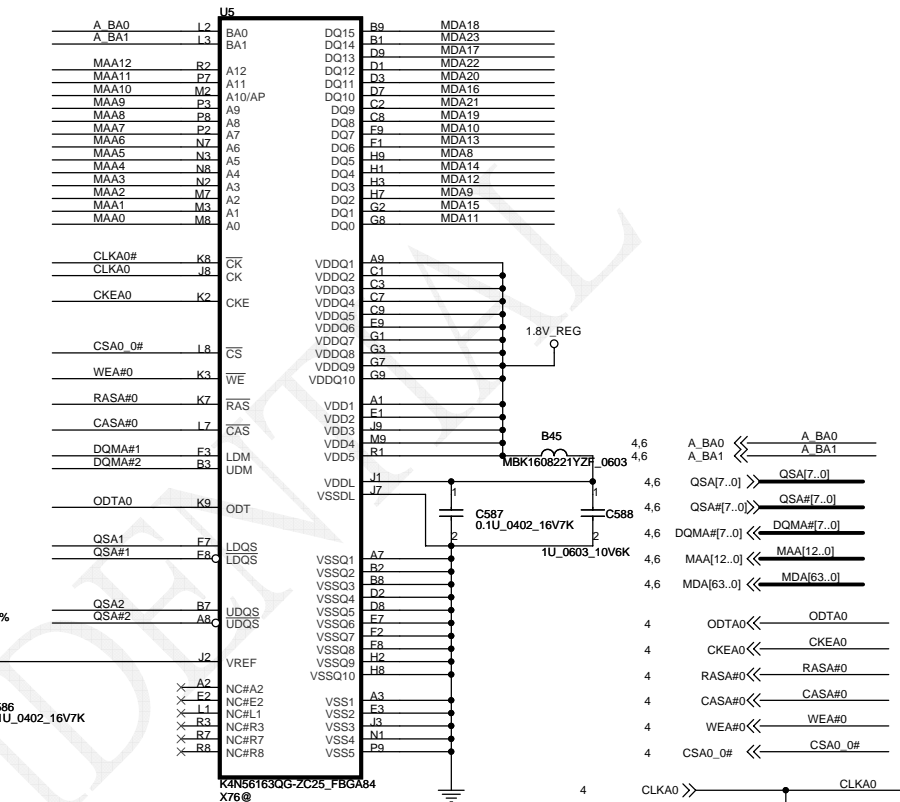
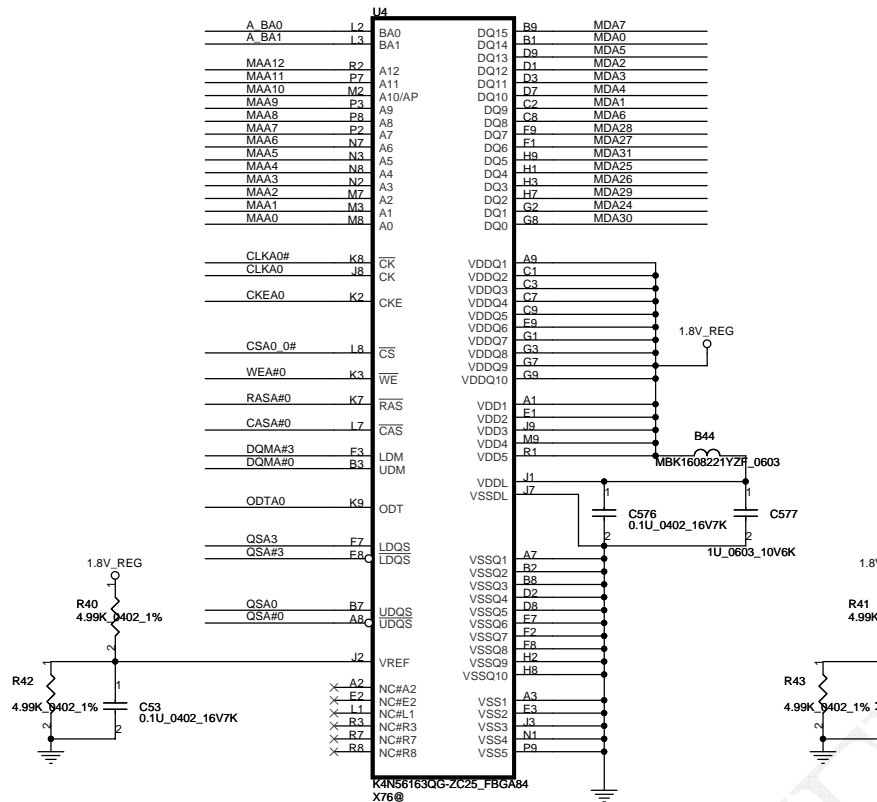


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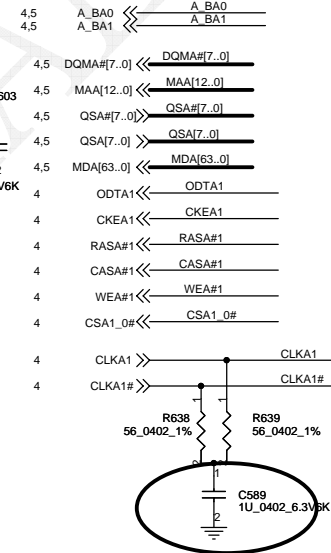
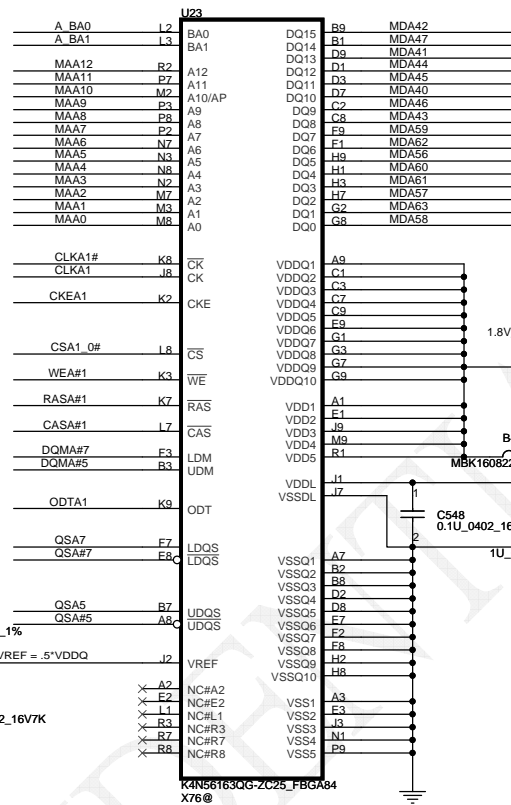
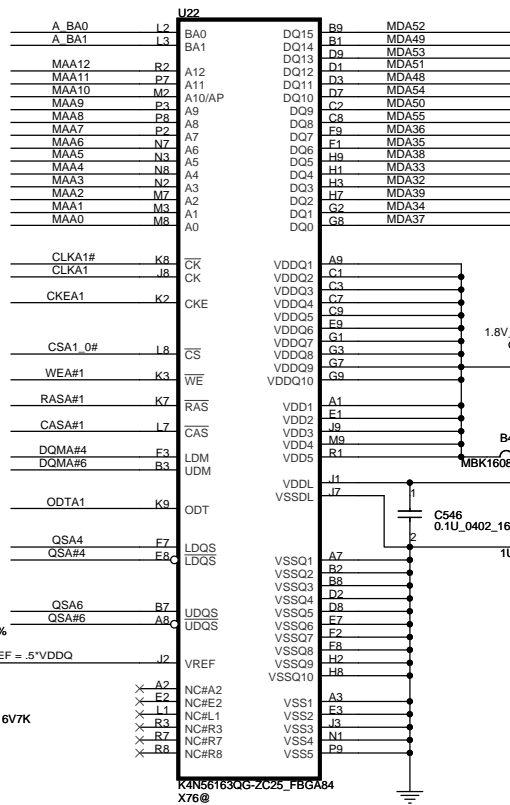
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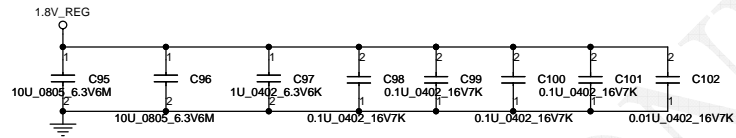
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	Title: SCHEMATIC, VGA/B LS-355BP Size: Custom Date: Wednesday, September 26, 2007		
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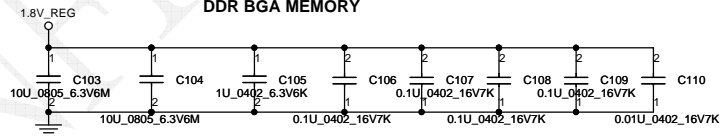
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DDR2 BGA MEMORY



DDR BGA MEMORY



CHAN B RANK 0 DDR2 BGA MEMORY

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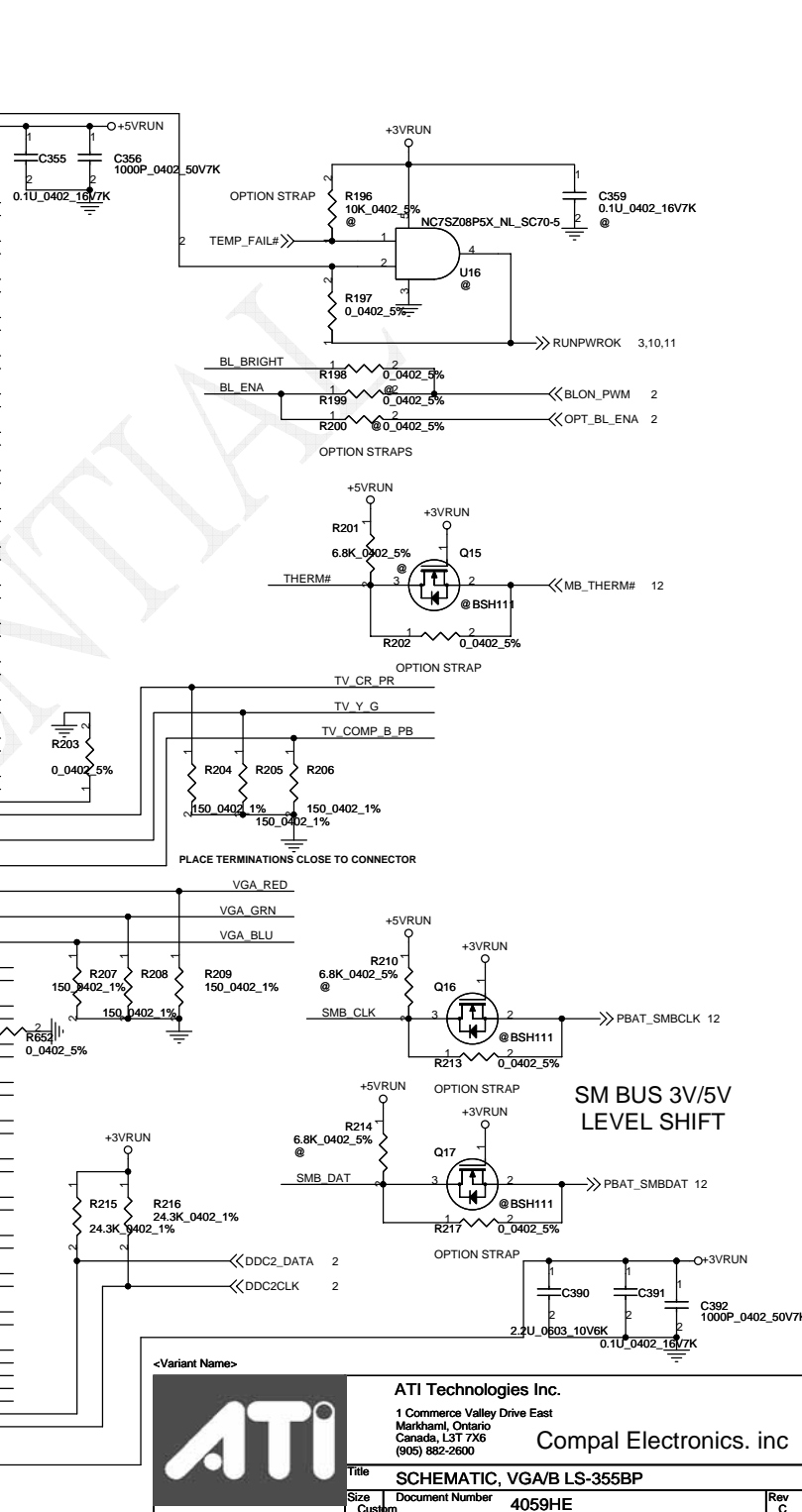
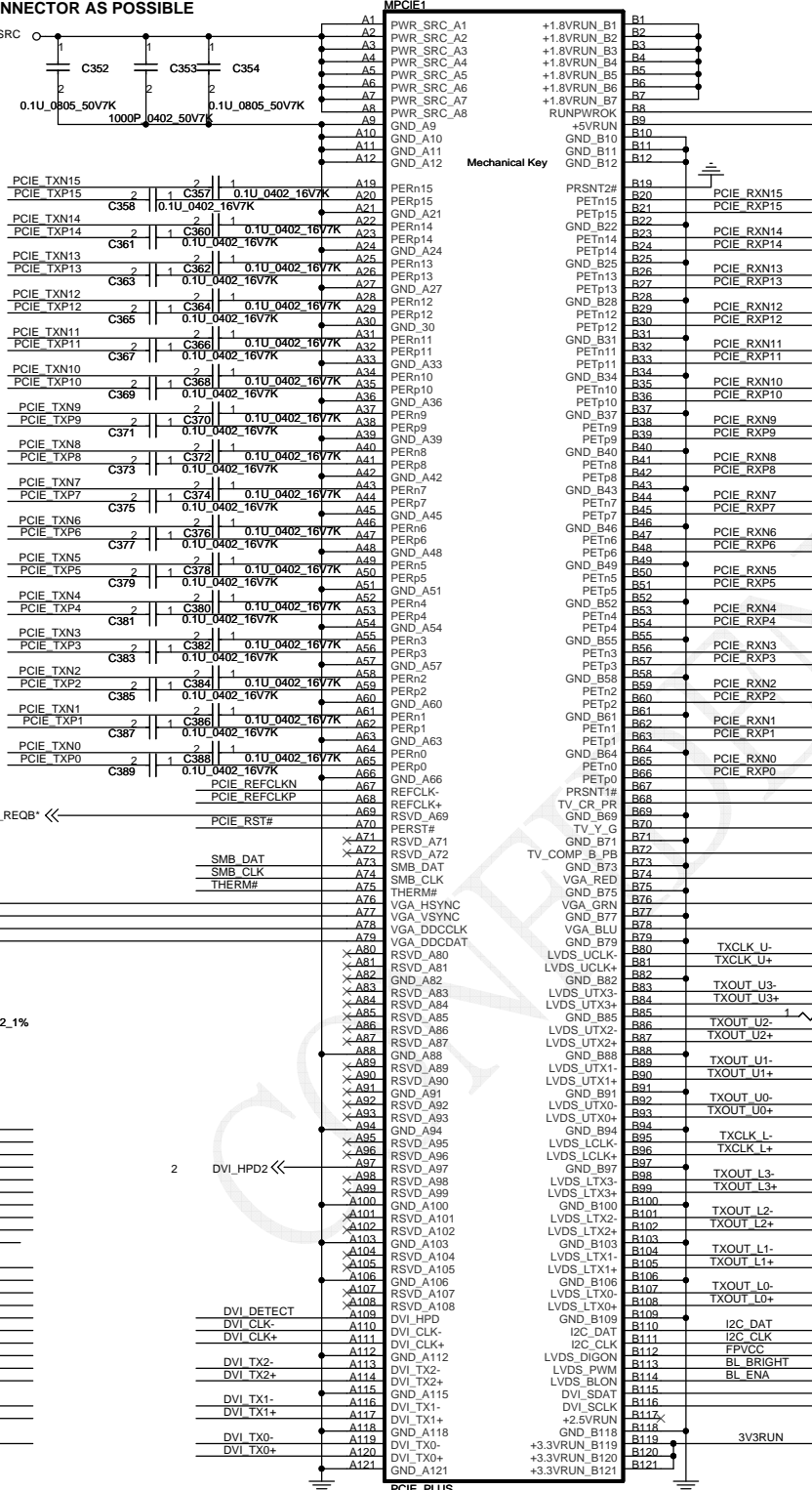
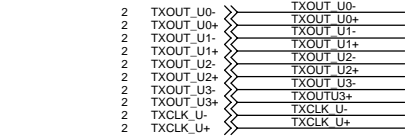
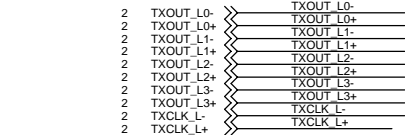
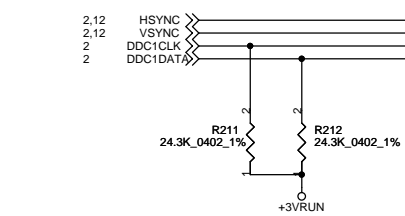
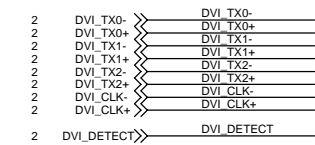
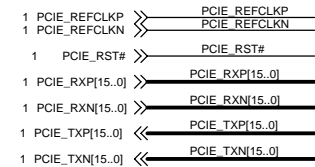
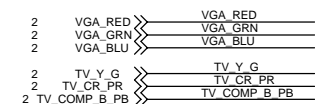
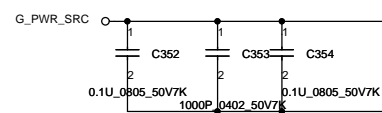
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PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE



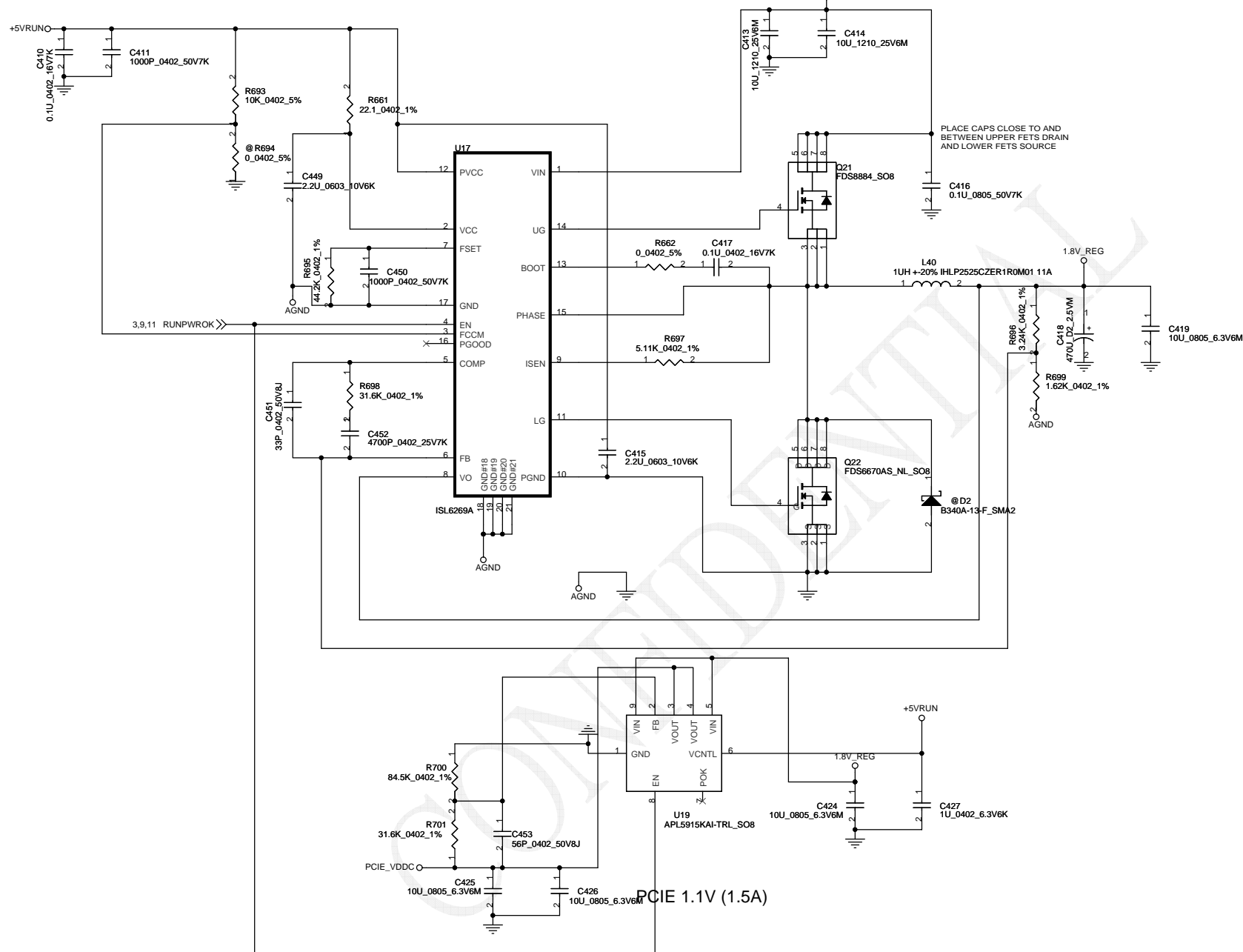
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IO REGULATOR 1.8V @ 10A



<Variant Name>



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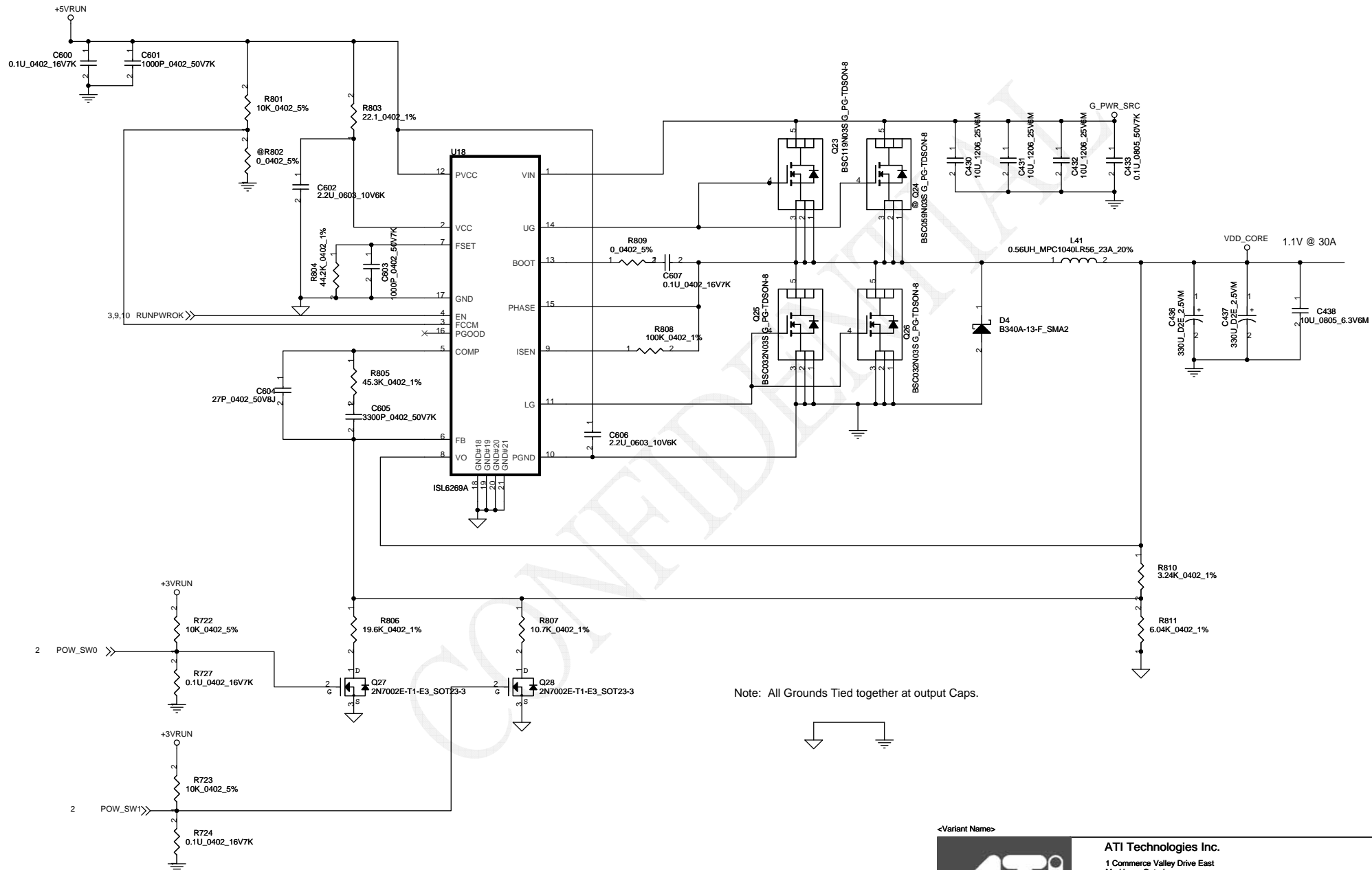
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CORE PWM REGULATOR .95V - 1.1V @ 30A



Note: All Grounds Tied together at output Caps.

<Variant Name>



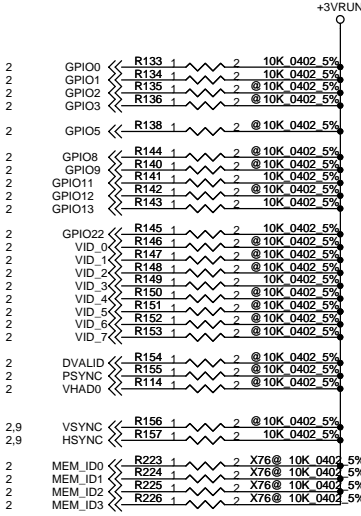
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ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

ATI RESERVED CONFIGURATION STRAPS	
0x00000000	0x00000000
0x00000001	0x00000000
0x00000002	0x00000000
0x00000003	0x00000000
0x00000004	0x00000000
0x00000005	0x00000000
0x00000006	0x00000000
0x00000007	0x00000000
0x00000008	0x00000000
0x00000009	0x00000000
0x0000000A	0x00000000
0x0000000B	0x00000000
0x0000000C	0x00000000
0x0000000D	0x00000000
0x0000000E	0x00000000
0x0000000F	0x00000000
0x00000010	0x00000000
0x00000011	0x00000000
0x00000012	0x00000000
0x00000013	0x00000000
0x00000014	0x00000000
0x00000015	0x00000000
0x00000016	0x00000000
0x00000017	0x00000000
0x00000018	0x00000000
0x00000019	0x00000000
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0x0000001B	0x00000000
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0x0000002C	0x00000000
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0x0000002E	0x00000000
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0x00000038	0x00000000
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0x0000005D	0x00000000
0x0000005E	0x00000000
0x0000005F	0x00000000
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0x00000061	0x00000000
0x00000062	0x00000000
0x00000063	0x00000000
0x00000064	0x00000000
0x00000065	0x00000000
0x00000066	0x00000000
0x00000067	0x00000000

VID0	VID2	VID3	VID4	VID6	VID7	HSYNC	DVALID	GPI02	GPI03	GPI05	GPI06	GPI08	VHAD0
<p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>													
GPI0_28_TDO	GENERICC	GPI021_BB_EN	GPI0_23_CLKREQB (DRIVES LOW DURING RESET)					H2SYNC	V2SYNC				

The schematic diagram shows the M25P10-AV1M6P memory device connected to a +3V3V supply. The device is a 16Kbit (2K x 8) SPI memory. The circuit includes a HOLD pin (pin 7) connected to a 3V3V supply through a 10k resistor. The VSS pin (pin 4) is connected to ground. The data bus (pins 2, 3, 4) is connected to a 3V3V supply. The chip select (pin 1) is connected to a 3V3V supply through a 10k resistor. The device is labeled 'M25P10-AV1M6P' and 'TYPE 1'.

	Vedio Memory Config. (GPU Internal PD)							
	R224	R223	R225	R226	MEM	Size	Vendor	Chips
M74	0	0	0	0	128MB	16Mx16	Samsung	x4
	0	0	0	1	256MB	32Mx16	Samsung	x4
	0	0	1	0	128MB	16Mx16	Hynix	x4
	0	0	1	1	256MB	32Mx16	Hynix	x4
	0	1	0	0	128MB	16Mx16	Infineon	x4
	0	1	0	1	256MB	32Mx16	Infineon	x4
M76	0	0	0	0	256MB	16Mx16	Samsung	x8
	0	0	0	1	512MB	32Mx16	Samsung	x8
	0	0	1	0	256MB	16Mx16	Hynix	x8
	0	0	1	1	512MB	32Mx16	Hynix	x8
	0	1	0	0	256MB	16Mx16	Infineon	x8
	0	1	0	1	512MB	32Mx16	Infineon	x8



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Schematic No.
4059HE

Date:
Wednesday, September 26, 2007

REVISION HISTORY

Rev C

Sch Rev	PCB Rev	Date
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REVISION DESCRIPTION

0	00A	04/10/06	PROTOTYPE BASED ON 105-B17831-00A
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