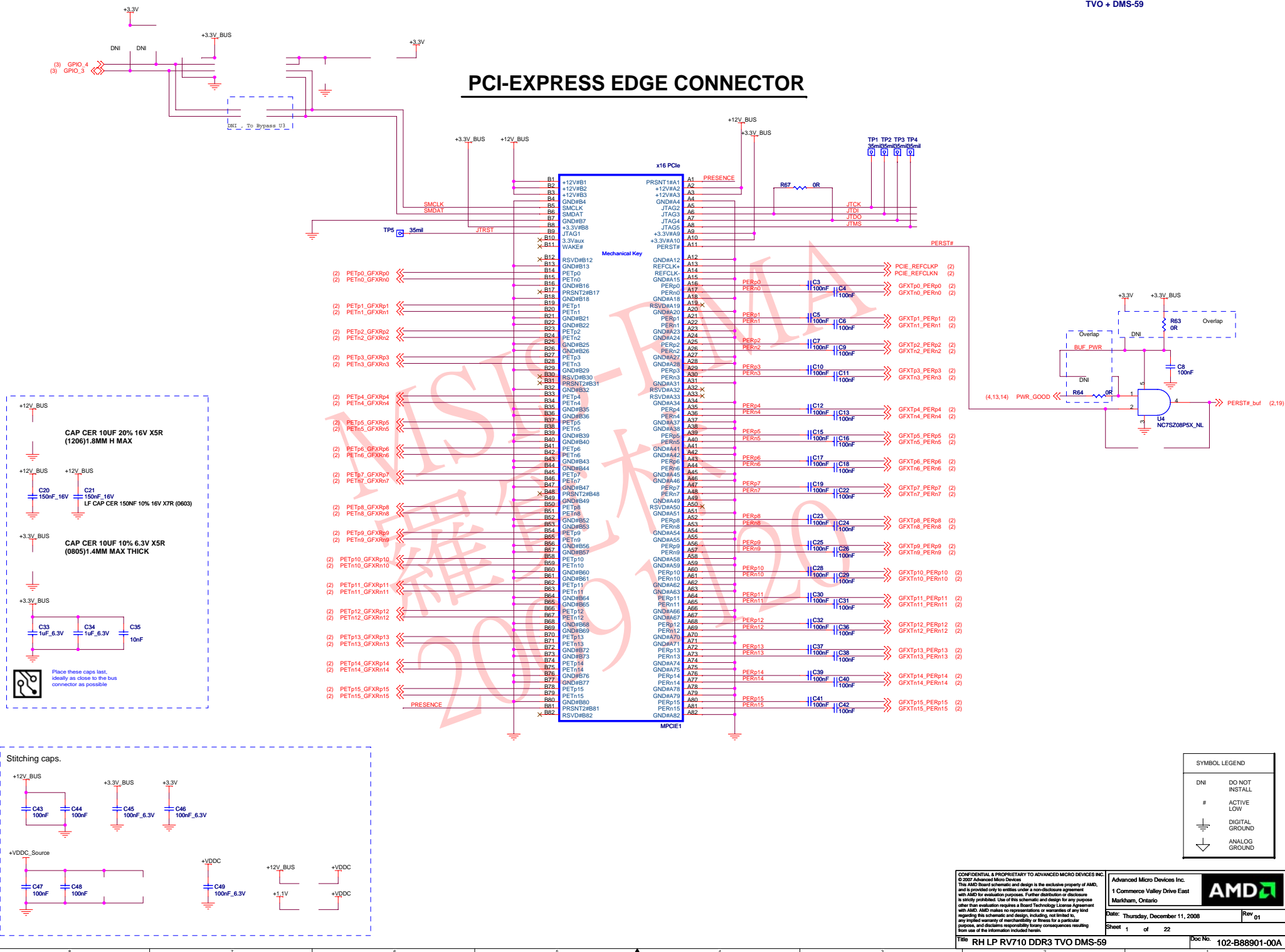
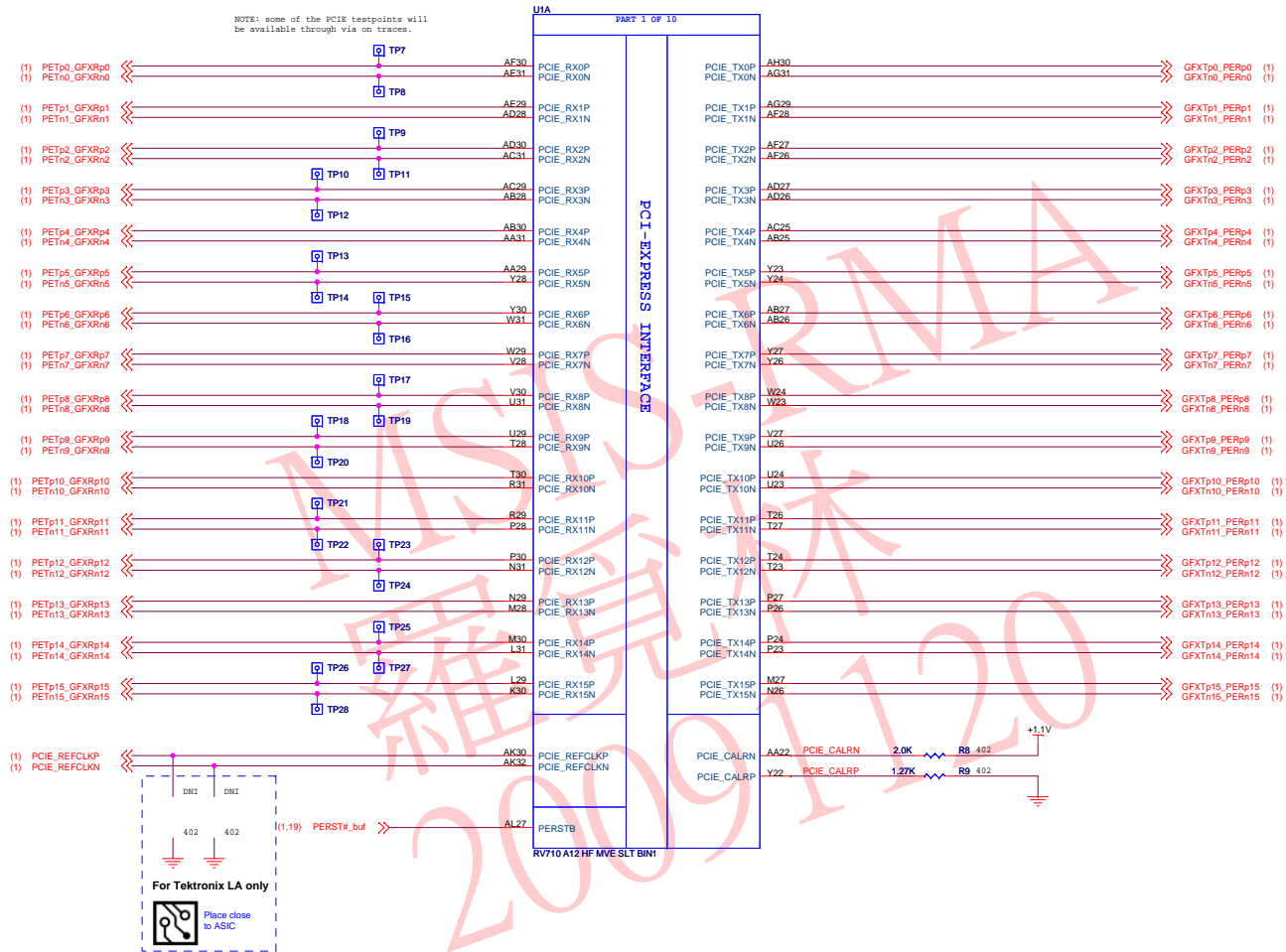
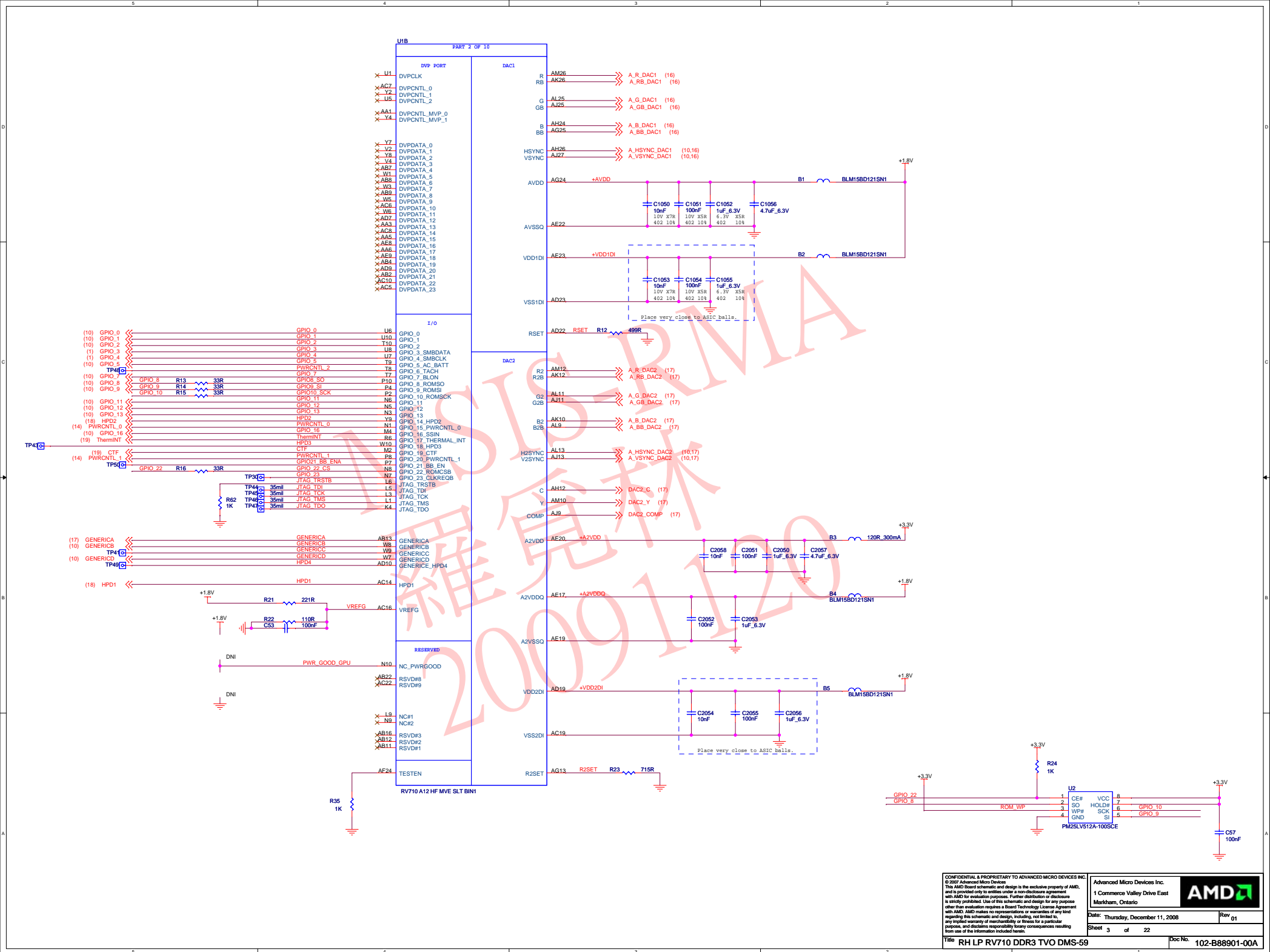
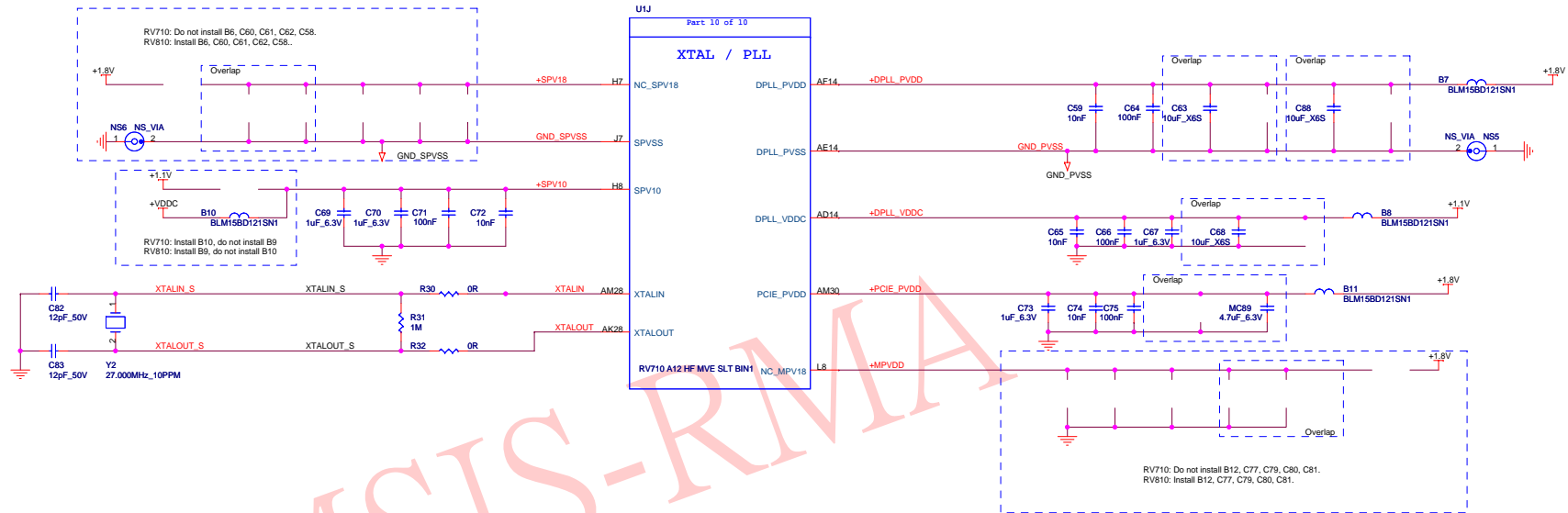


PCI-EXPRESS EDGE CONNECTOR







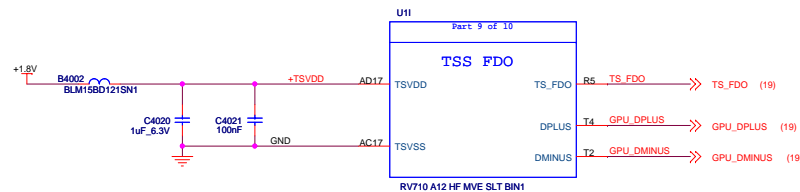
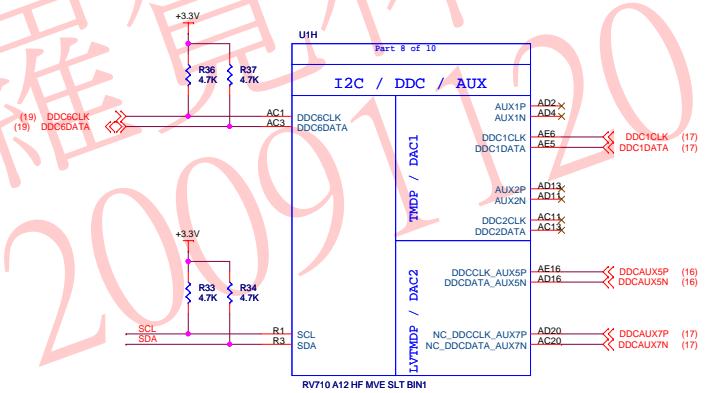


DDC6 BUS:

I2C Address	Function	Device
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A



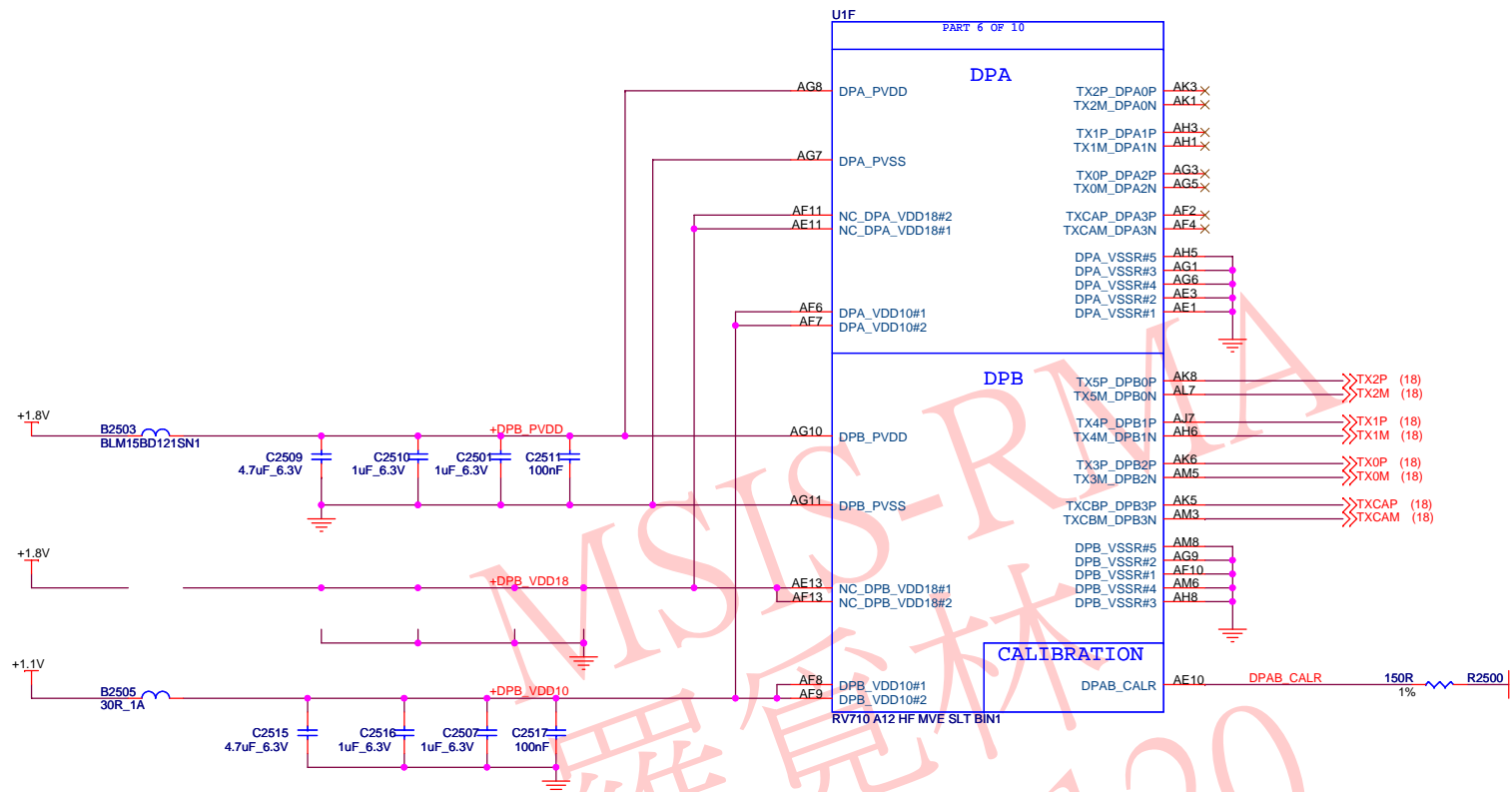
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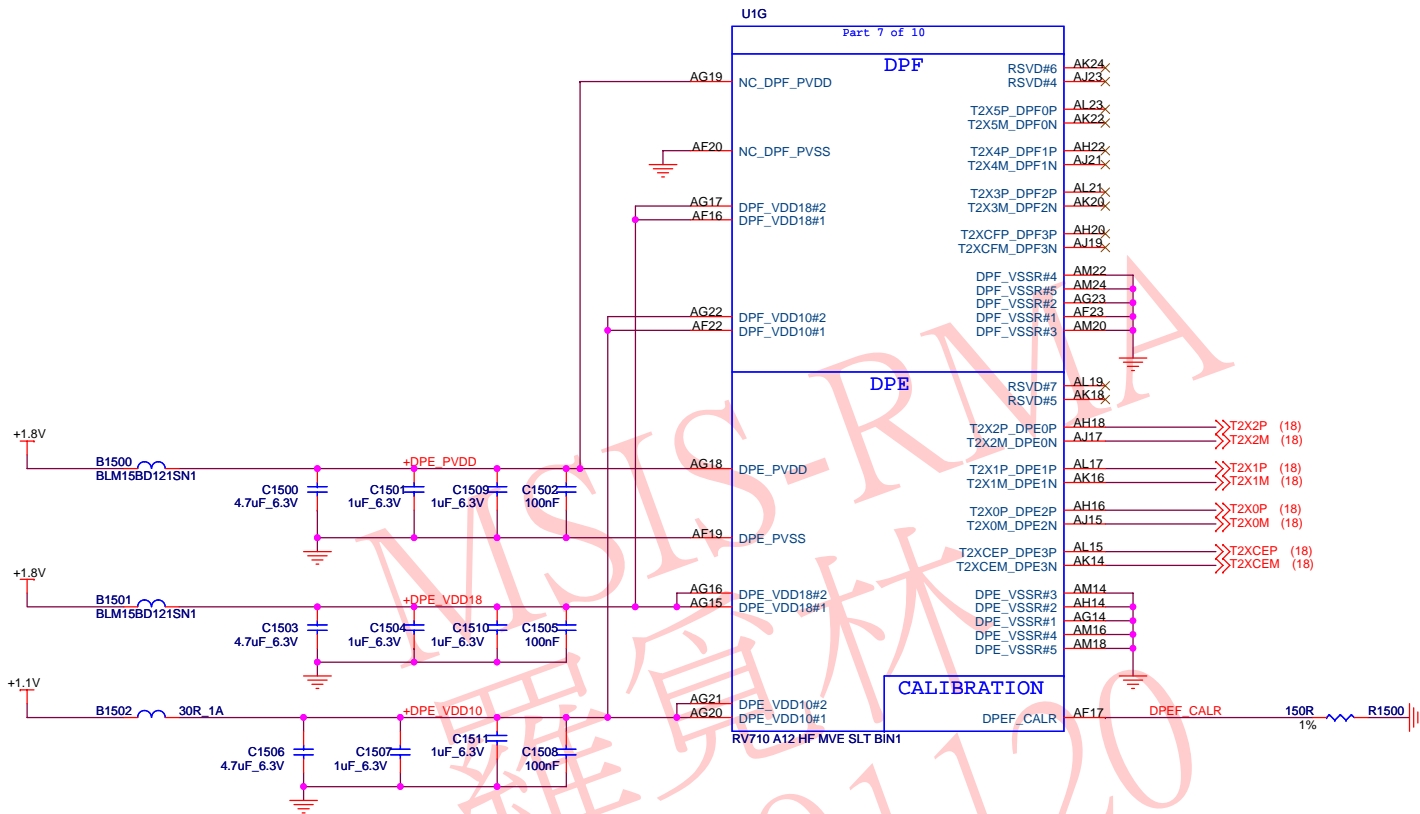
Title: RH LP RV710 DDR3 TWO DMS-59

Doc No: 102-B88901-00A

TMDP INTERFACE



LVTMDP INTERFACE



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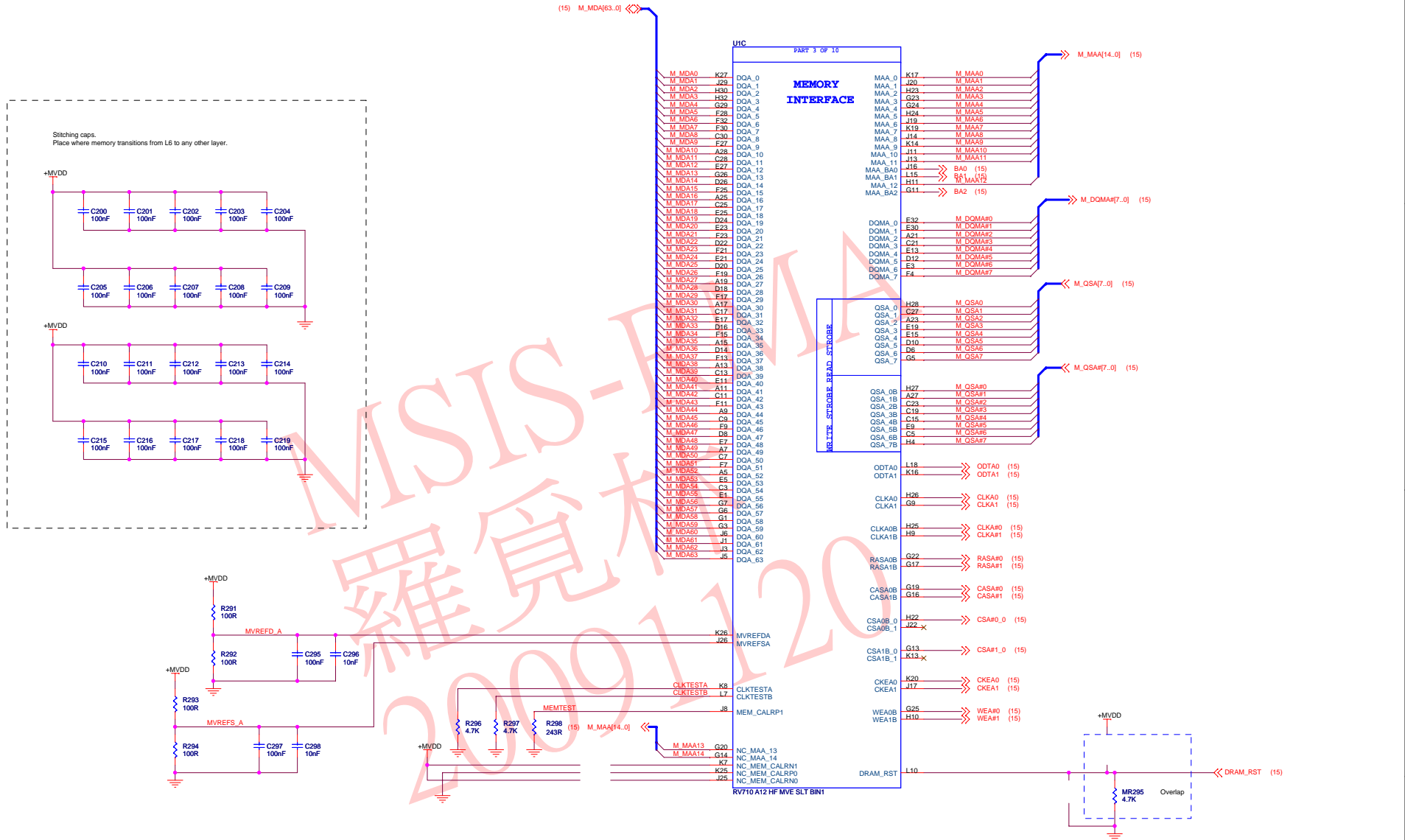
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Title RH LP RV710 DDR3 TVO DMS-59

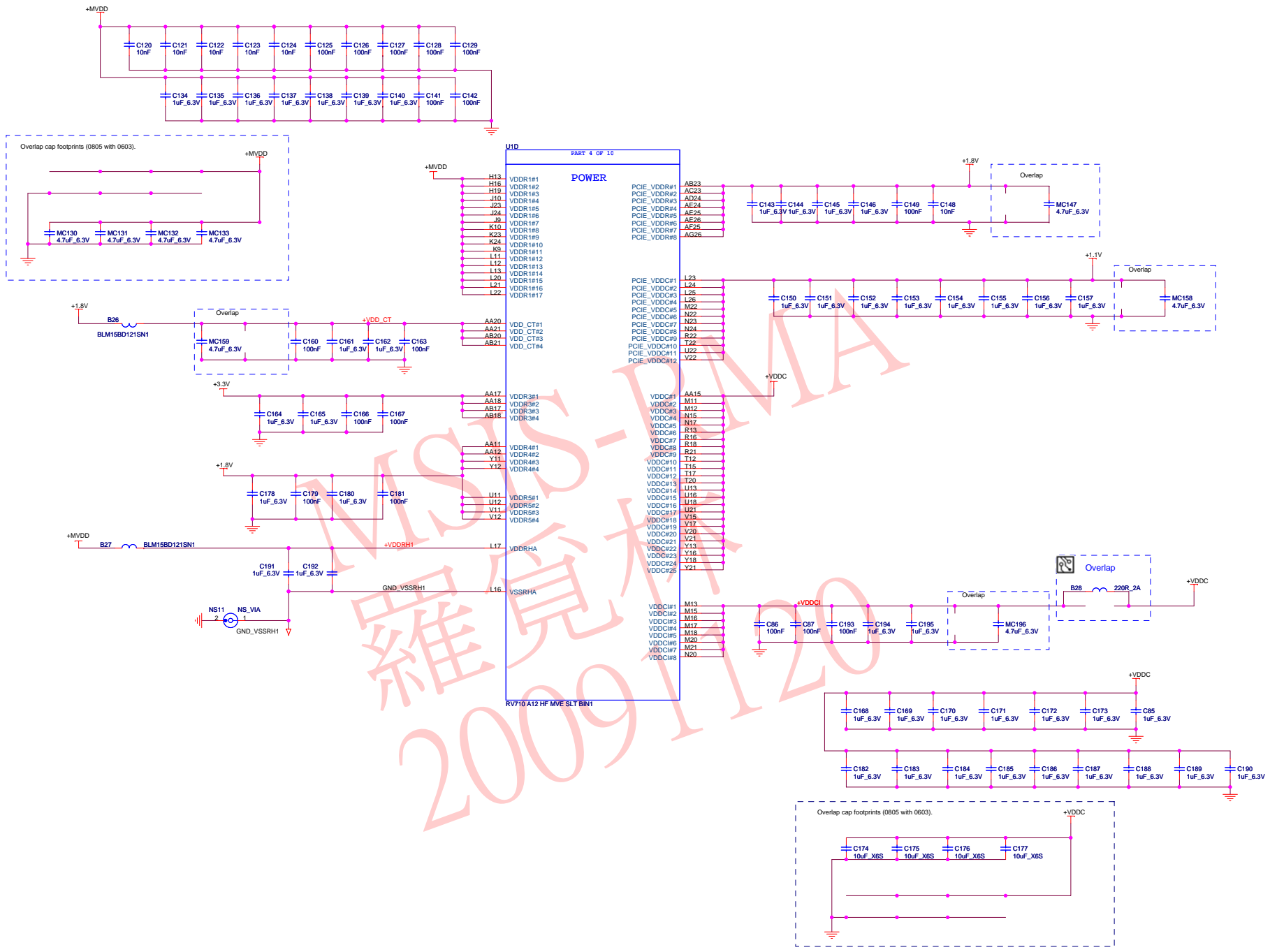
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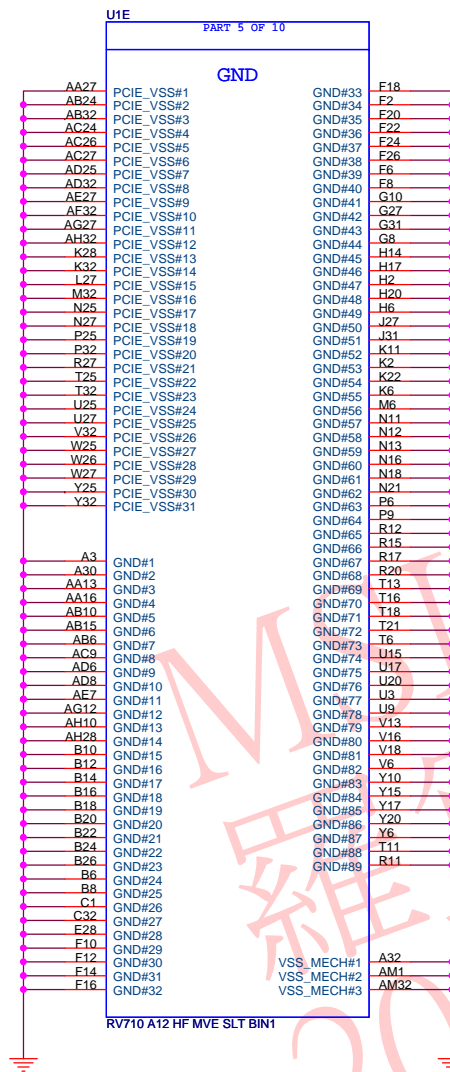
MEMORY INTERFACE



DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R

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Title RH LP RV710 DDR3 TOS DMS-5		Date: Thursday, December 11, 2008	Rev 01
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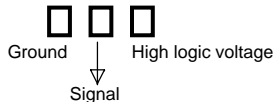
PIN BASED STRAPS

Pull-Down Resistors are for BU until built-in pull-downs are verified.



Overlap pads to save space
and to prevent assembly of
both resistors.

Layout



PIN BASED STRAPS



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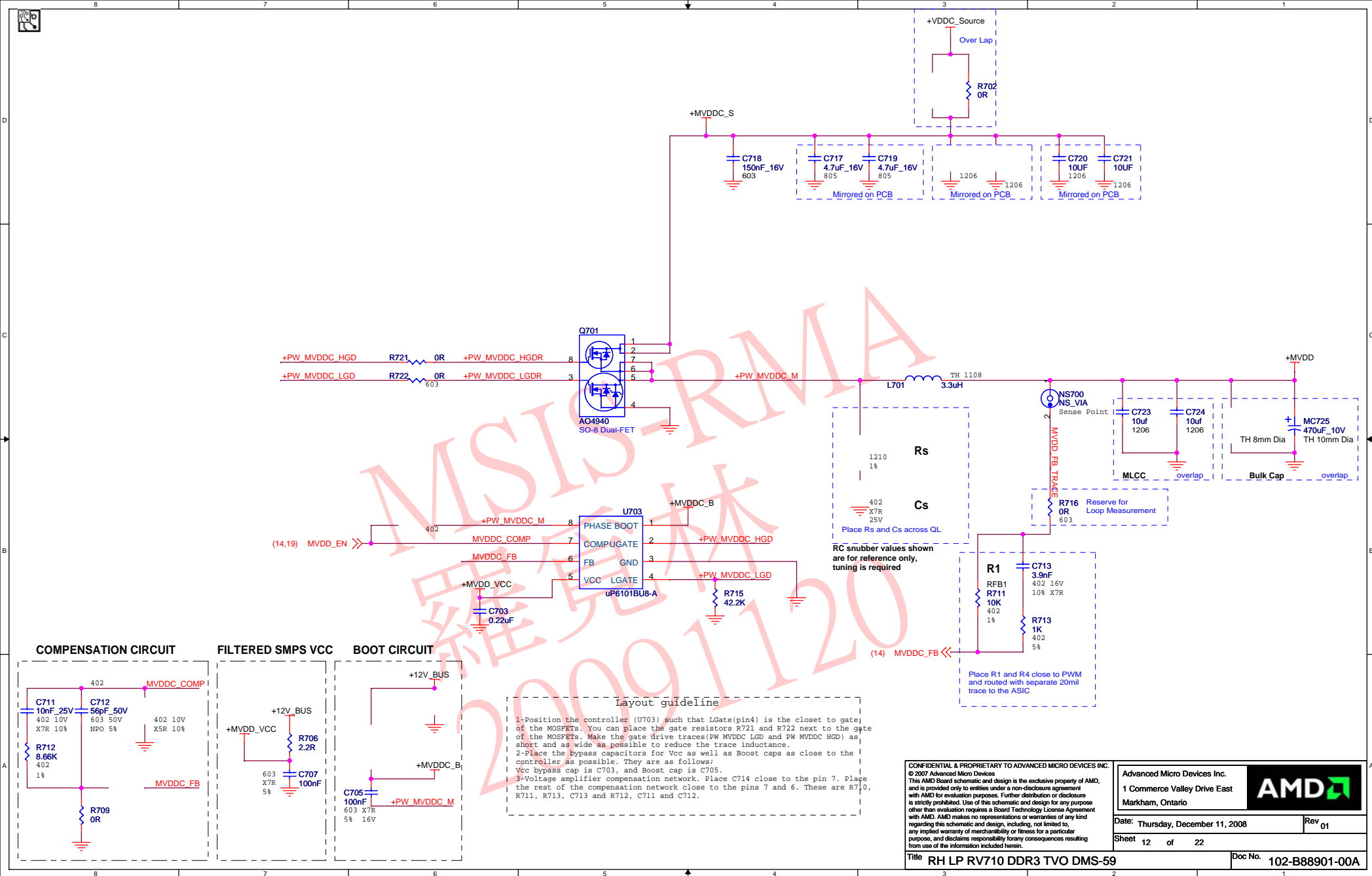
Date: Thursday, December 11, 2008

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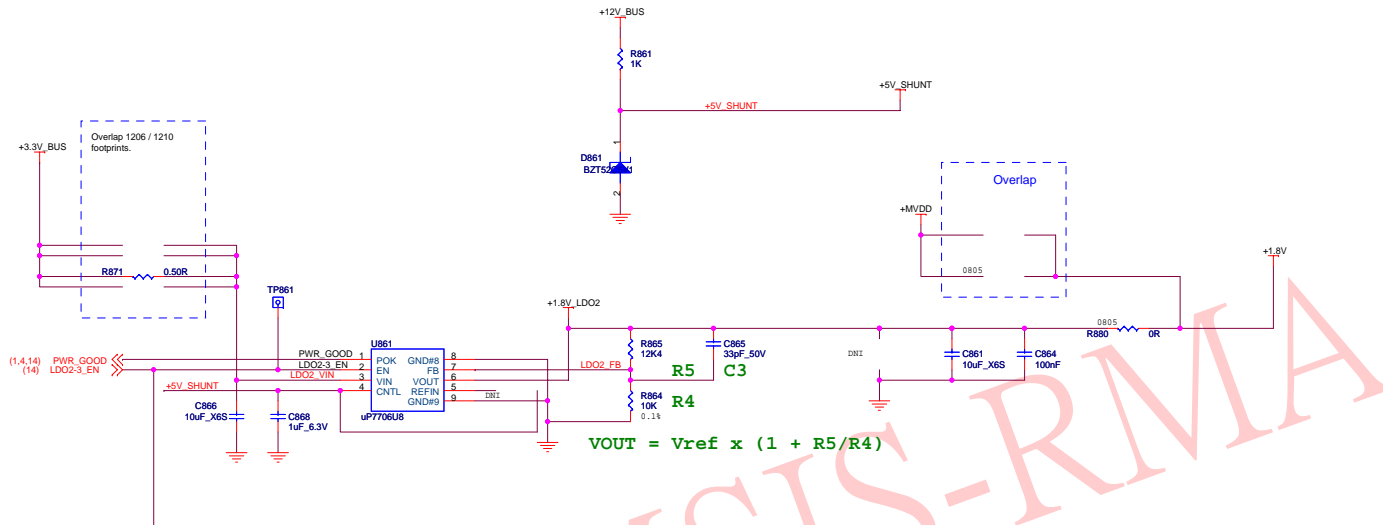
Title RH LP RV710 DDR3 TVO DMS-59

Doc No. 102-B88901-00A



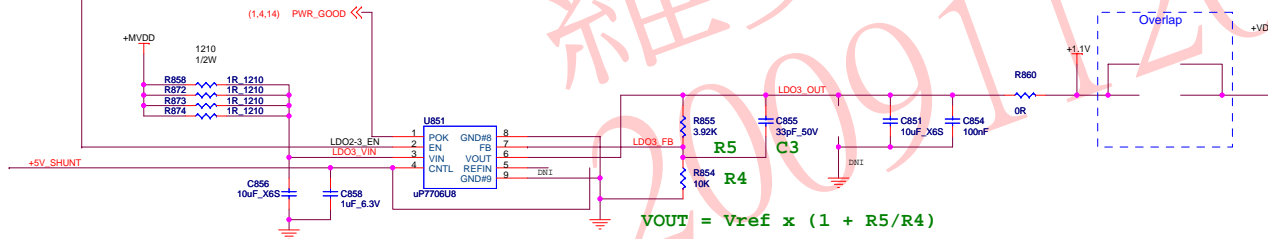


LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



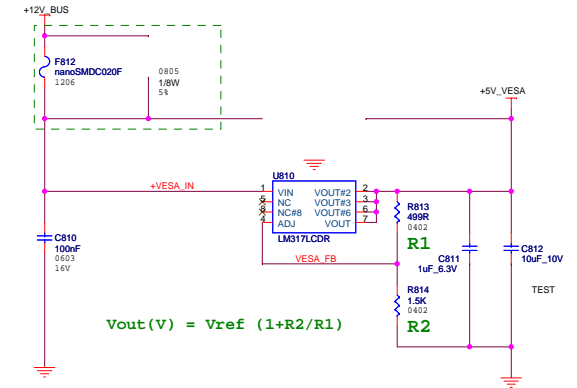
$$V_{OUT} = V_{ref} \times (1 + R5/R4)$$

LDO #3: Vin = +1.4V to 2.087V MAX Vout = +1.1V +/- 2.5% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



$$V_{OUT} = V_{ref} \times (1 + R5/R4)$$

Regulators for +5V_VESA



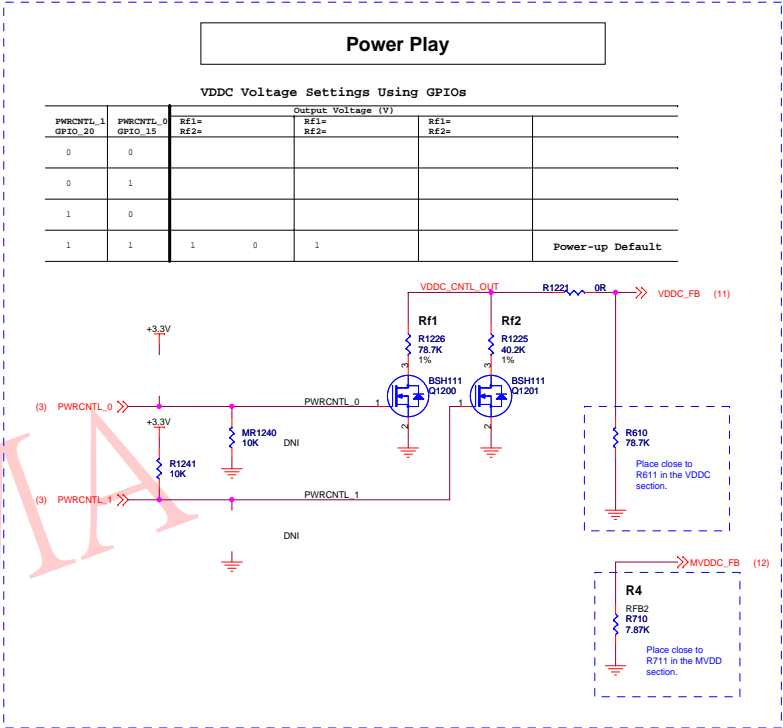
$$V_{out}(V) = V_{ref} (1 + R2/R1)$$

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Power up/down Sequencing



PBCTRL1_1 GPIO_20	PBCTRL1_5 GPIO_15	Output Voltage (V)			
		R1= R2=	R1= R2=	R1= R2=	
0	0				
0	1				
1	0				
1	1	1	0	1	Power-up Default

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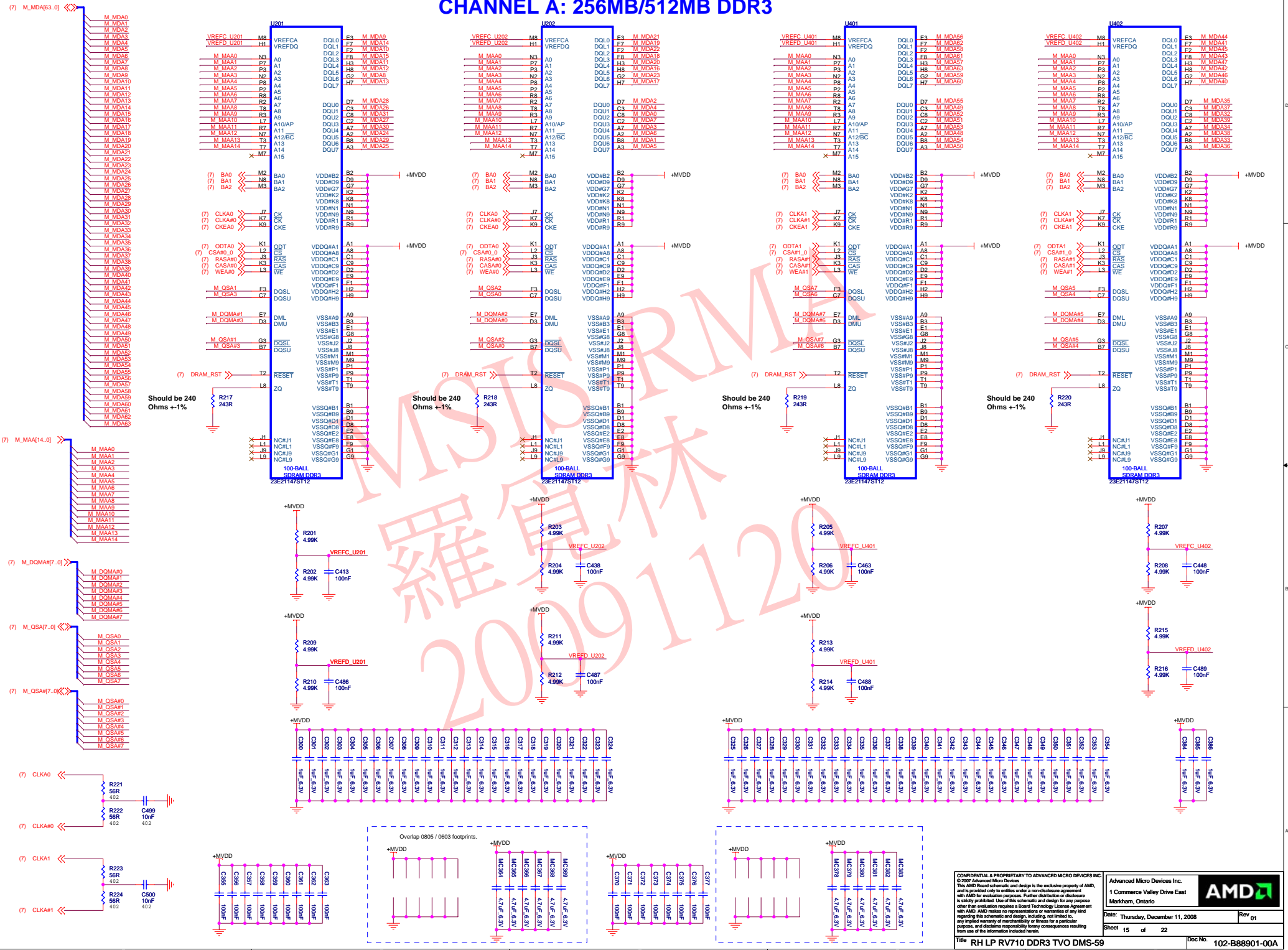
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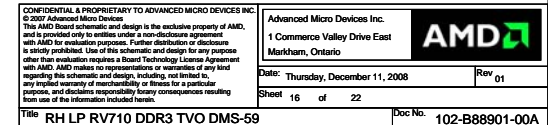
9

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CHANNEL A: 256MB/512MB DDR3

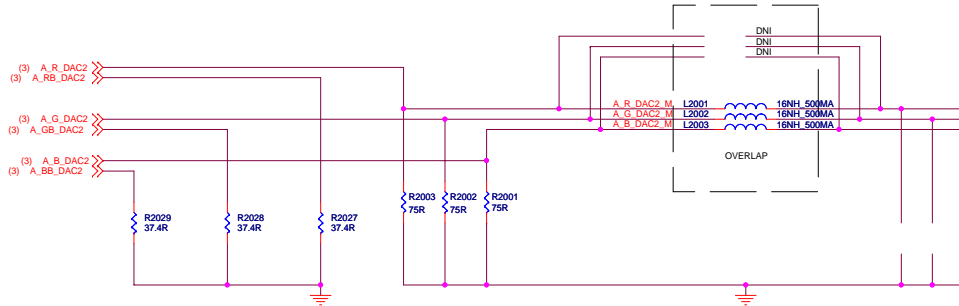




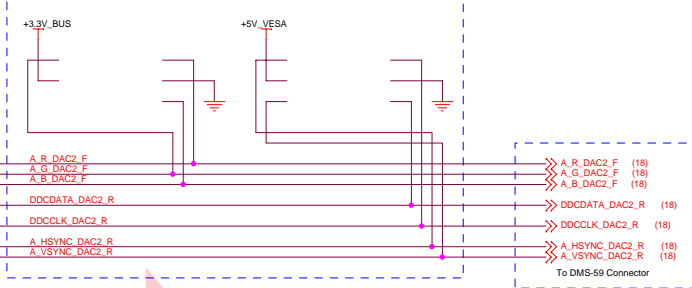
DAC 2 OUTPUT



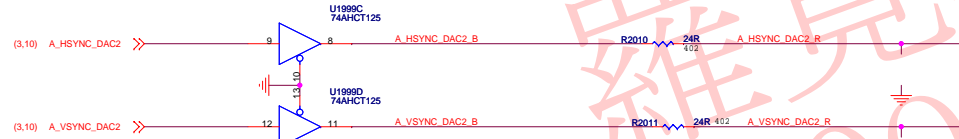
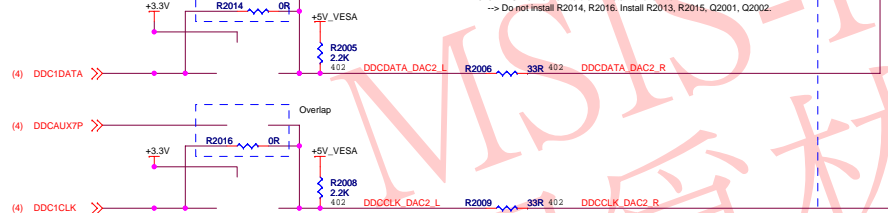
Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane



Optional ESD Protection Diodes Place close to Connector
ALLOW FOR A LOW INDUCTANCE PATH TO PIN 5

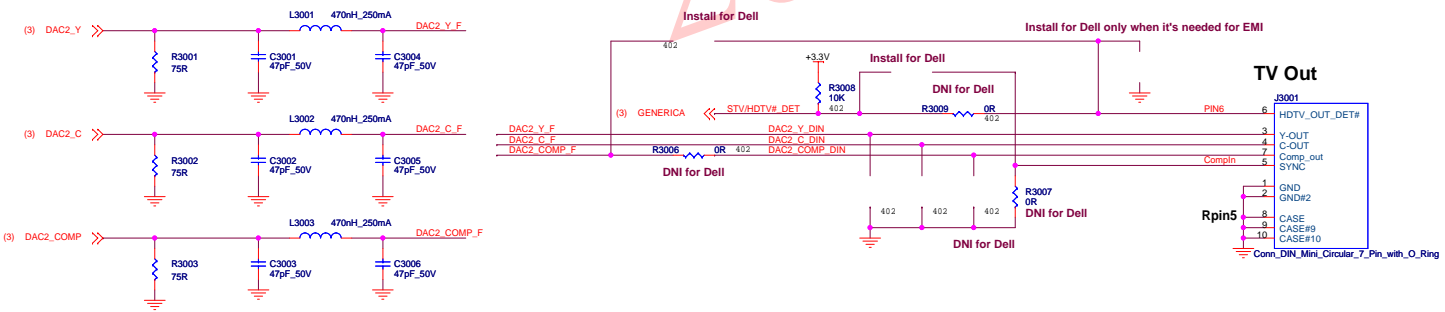


RV710: DDC1 is 5V tolerant. Do not install level shifter.
-> Do not install R2013, R2015, Q2001, Q2002. Install R2014, R2016.
RV810: DDC1 is NOT 5V tolerant. Install level shifter.
-> Do not install R2014, R2016. Install R2013, R2015, Q2001, Q2002.

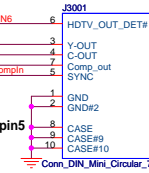


SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

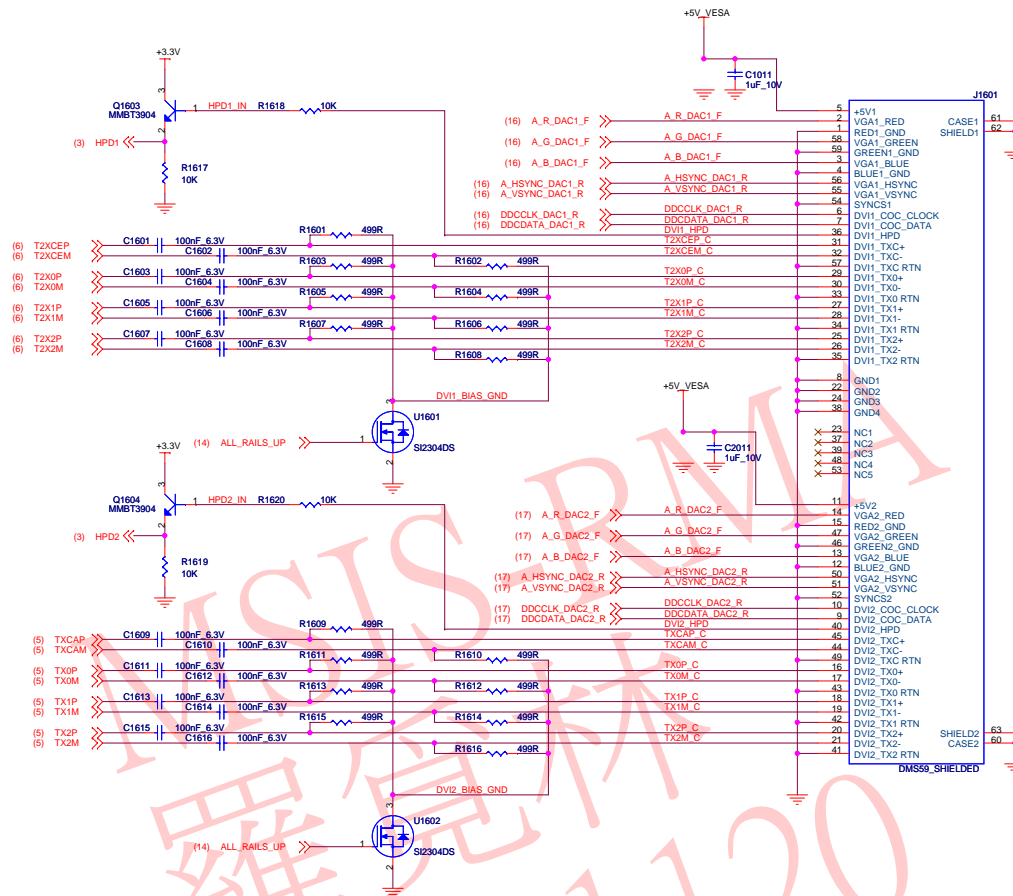
TVO



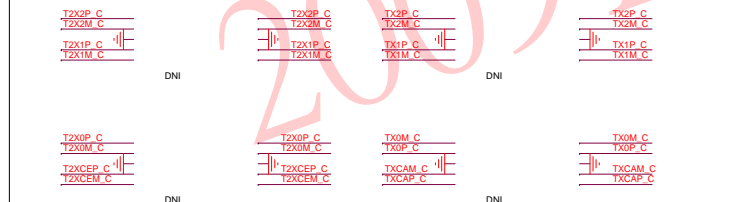
TV Out



DMS-59 DPB / DPE OUTPUT



Optional ESD protection diodes



Connector 1	
Signals	Mapping
VGA:	DAC1
DVI:	Internal TMDS2
HPD:	HPD1
DDC:	DDC1
5V:	+5V_VESA

Connector 2	
Signals	Mapping
VGA:	DAC2 (TVDAC)
DVI:	Internal LVTMS1
HPD:	HPD2
DDC:	DDC5
5V:	+5V_VESA

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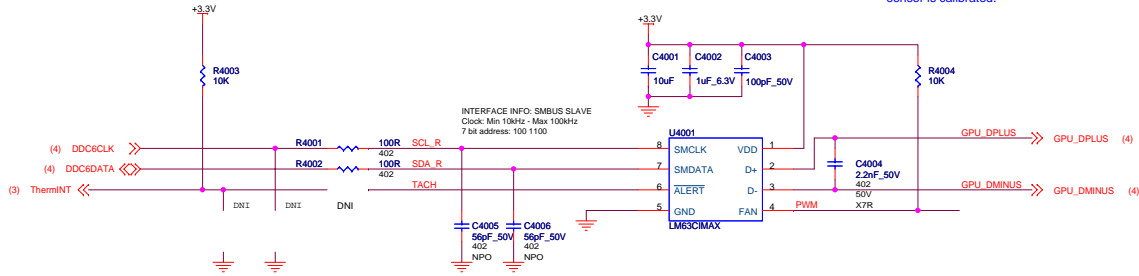
Title: RH LP RV710 DDR3 TWO DMS-59

Doc No: 102-B88901-00A

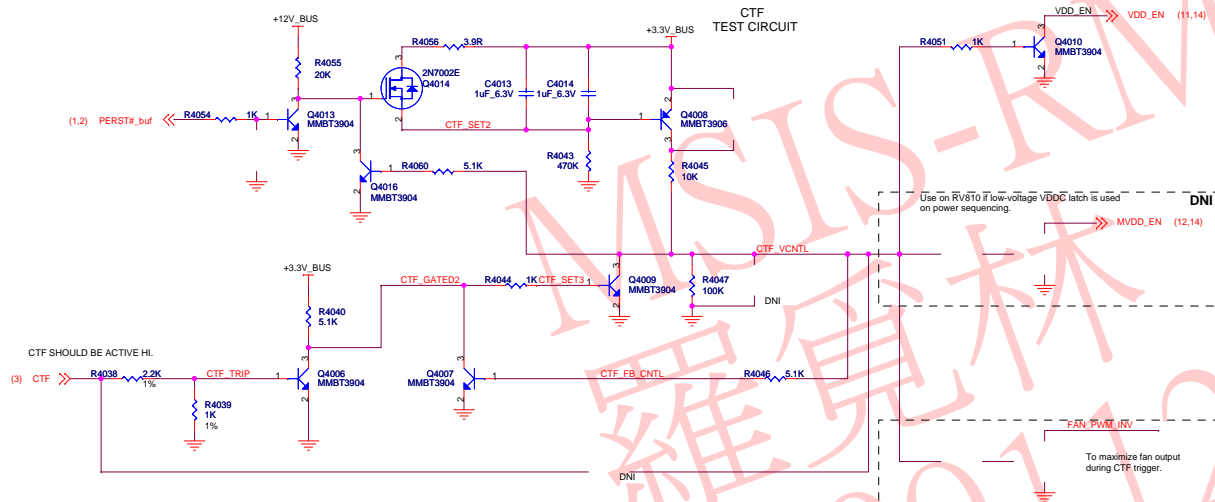
THERMAL MANAGEMENT



Remote diode temp sensor is for RV710 BU, until internal thermal sensor is calibrated.



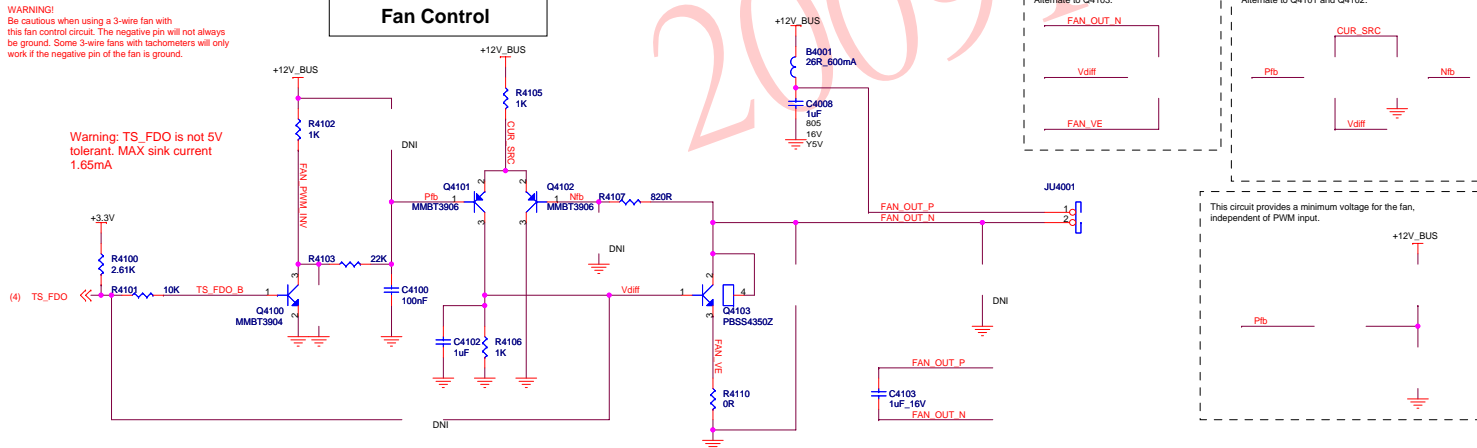
Critical Temperature Fault



Fan Control

WARNING!
Be cautious when using a 3-wire fan with this fan control circuit. The negative pin will not always be ground. Some 3-wire fans with tachometers will only work if the negative pin of the fan is ground.

Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA



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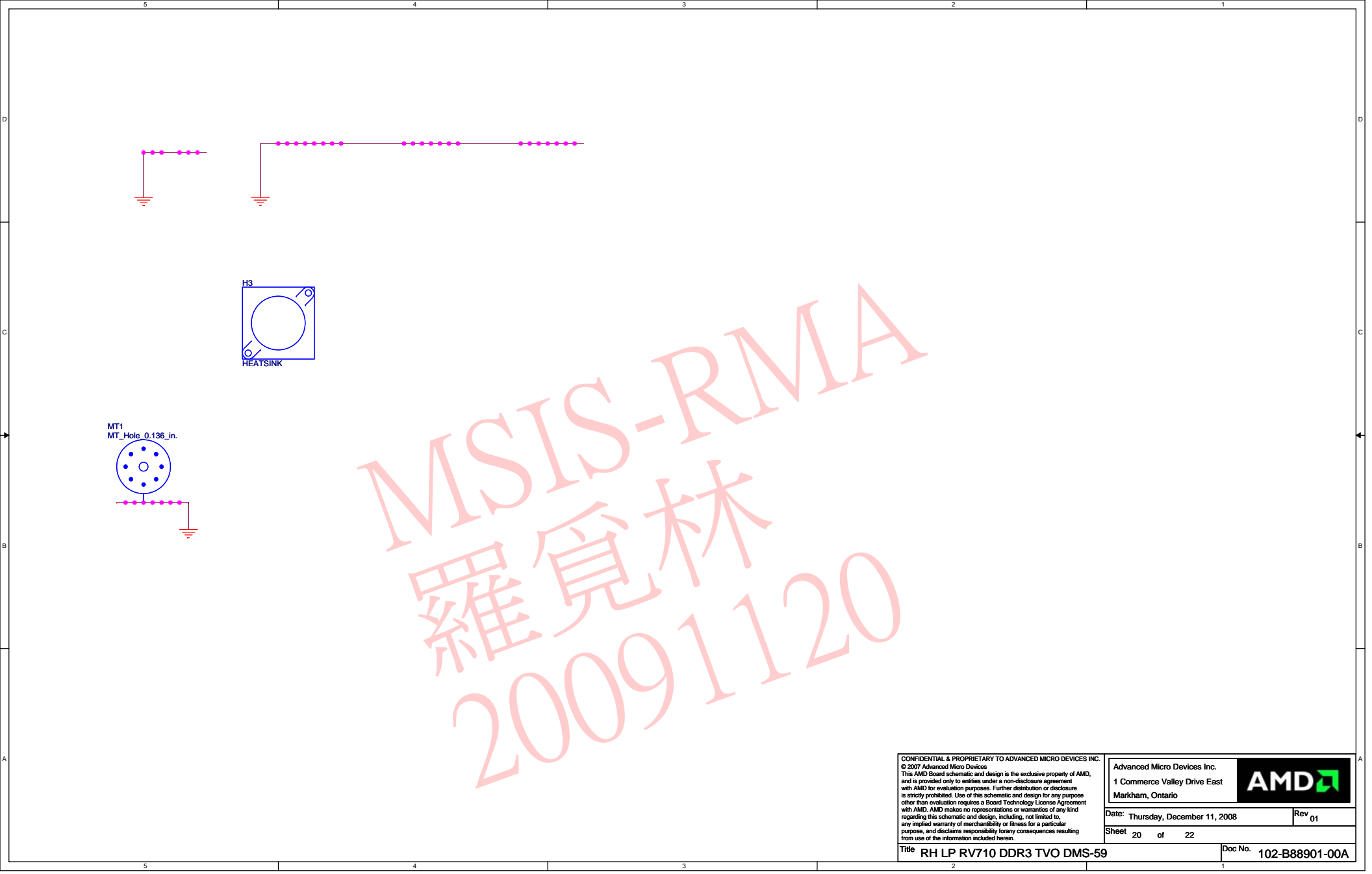
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<div>AMD</div>			Title			Schematic No.		Date:	
			RH LP RV710 DDR3 TVO DMS-59			102-B88901-00A		Thursday, December 11, 2008	
			REVISION HISTORY					NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.	
Sch Rev	PCB Rev	Date	RV710 REVISION DESCRIPTION						
01	00A	2008.11.11	INITIAL RELEASE OF B889 BOARD. BASED ON B754 Rev 90.						
02	00A	2008.11.12	ADD R67 AS OPTION TO SHORT JTAG IO						
03	00A	2008.11.13	REMOVE MT2						
04	00A	2008.11.19	REMOVE MVDD GPIO VOLTAGE CONTROL OPTION						
05	00A	2008.11.19	REMOVE LED AND PWR_GOOD CONNECTIONS TO CTF CIRCUIT						
06	00A	2008.11.19	REMOVE MC625, PL601, NL601, ML601, R58 AND PROVIDE OPTION TO SHORT CTF TO CTF_VCNTL BY R4062						
07	00A	2008.11.24	CHANGE DAC INDUCTORS TO 0603 PART, REMOVE C1001-C1003 and C2001-C2003						
08	00A	2008.11.25	REMOVE R26, CHANGE MVDD FET SYMBOL						
09	00A	2008.12.01	CHANGE PIN ASSIGNMENT OF D2001 AND REG1603 FOR LAYOUT						

MSIS-RMA
羅覓林
20091120