

P410: G3-128, 128/256MB, 128-bit, 8/16Mx32 DDR2
LVDS, TV_OUT, VGA

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HISTORY:

A00: INITIAL VERSION

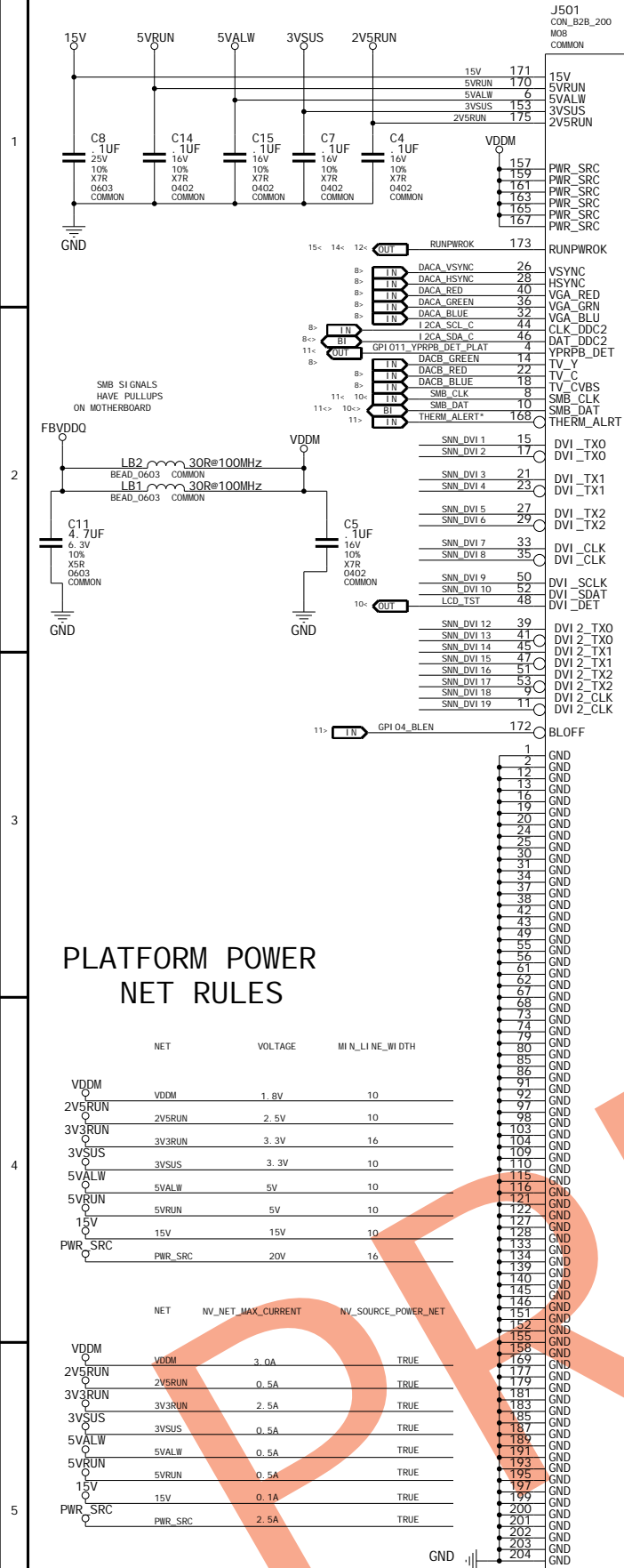
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview

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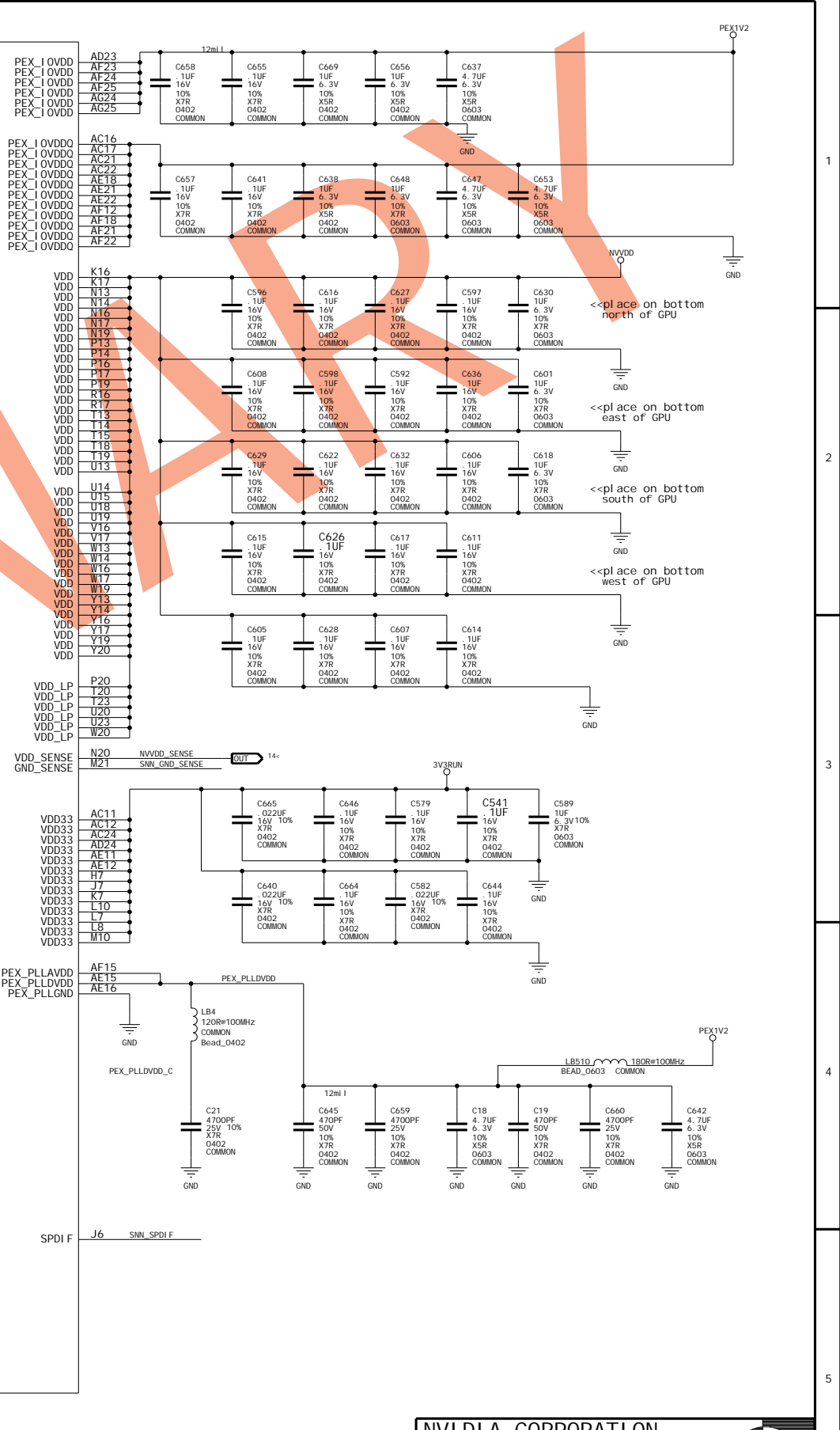
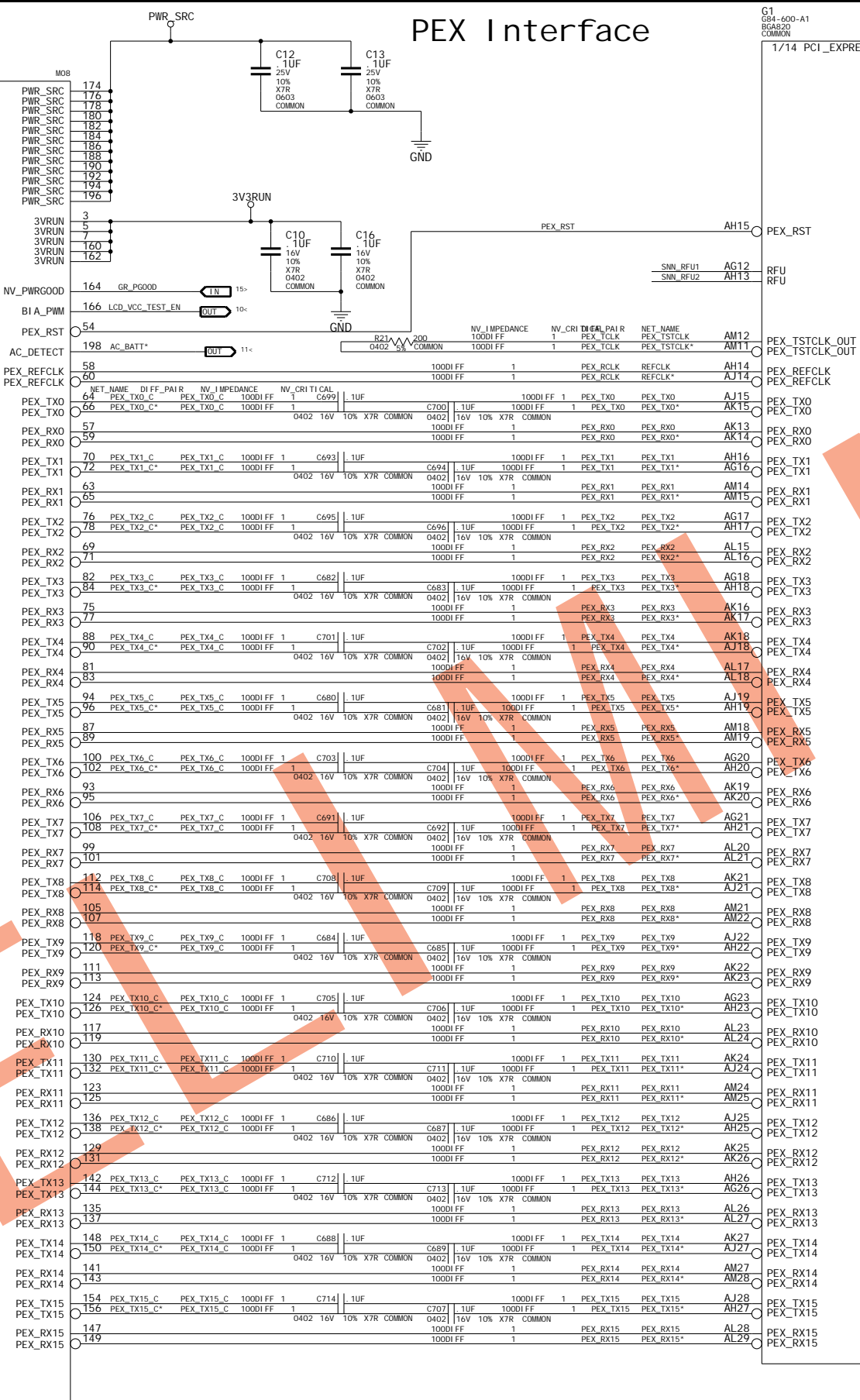
MOTHERBOARD CONNECTOR



PLATFORM POWER NET RULES

NET	VOLTAGE	MIN_LENGTH_WIDTH
VDDM	VDDM	1.8V 10
2V5RUN	2V5RUN	2.5V 10
3V3RUN	3V3RUN	3.3V 16
3VSUS	3VSUS	3.3V 10
5VALW	5VALW	5V 10
5VRUN	5VRUN	5V 10
15V	15V	15V 10
PWR_SRC	PWR_SRC	20V 16
NET	NV_NET_MAX_CURRENT	NV_SOURCE_POWER_NET
VDDM	3.0A	TRUE
2V5RUN	0.5A	TRUE
3V3RUN	2.5A	TRUE
3VSUS	0.5A	TRUE
5VALW	0.5A	TRUE
5VRUN	0.5A	TRUE
15V	0.1A	TRUE
PWR_SRC	2.5A	TRUE

PEX Interface



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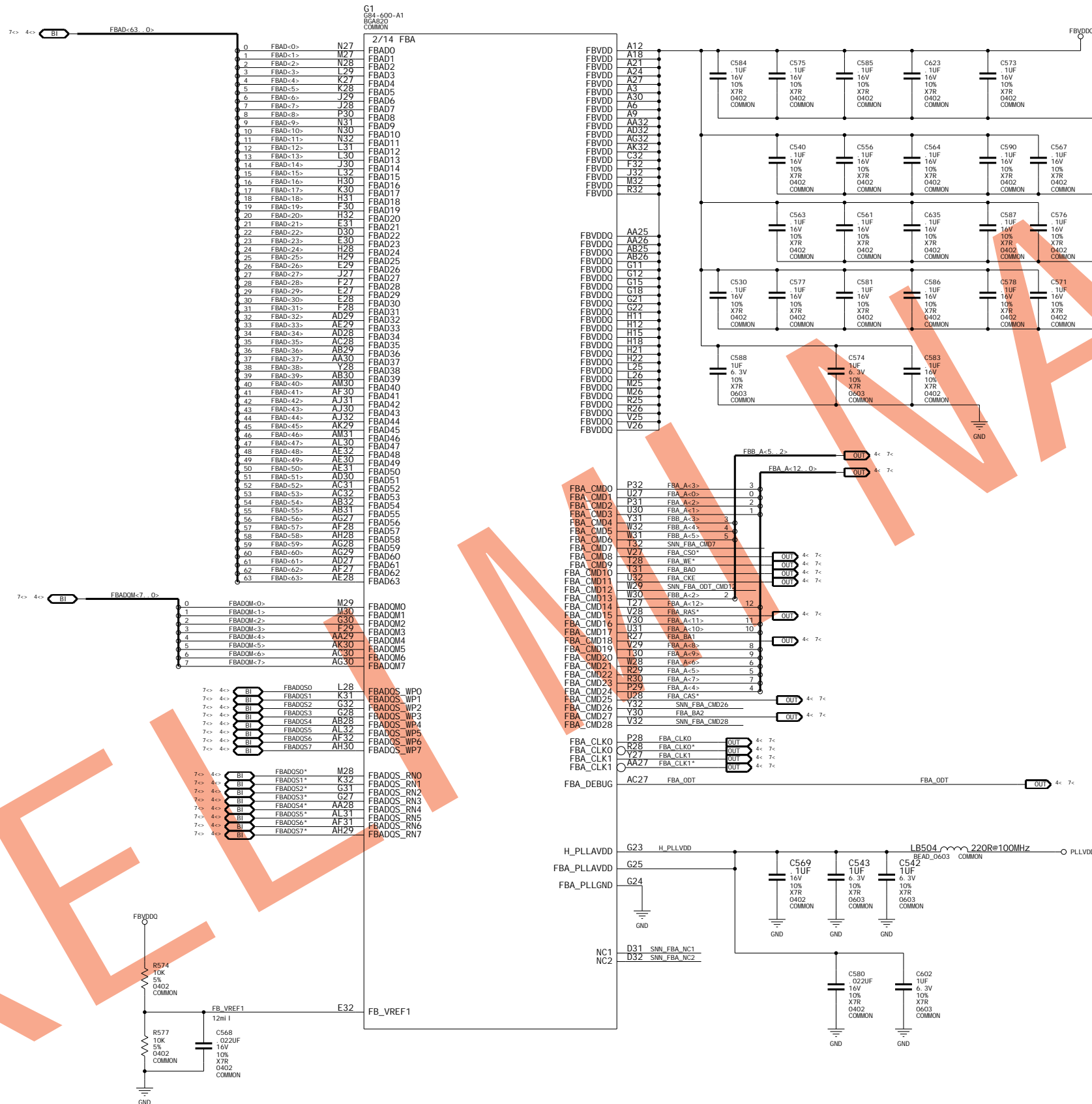


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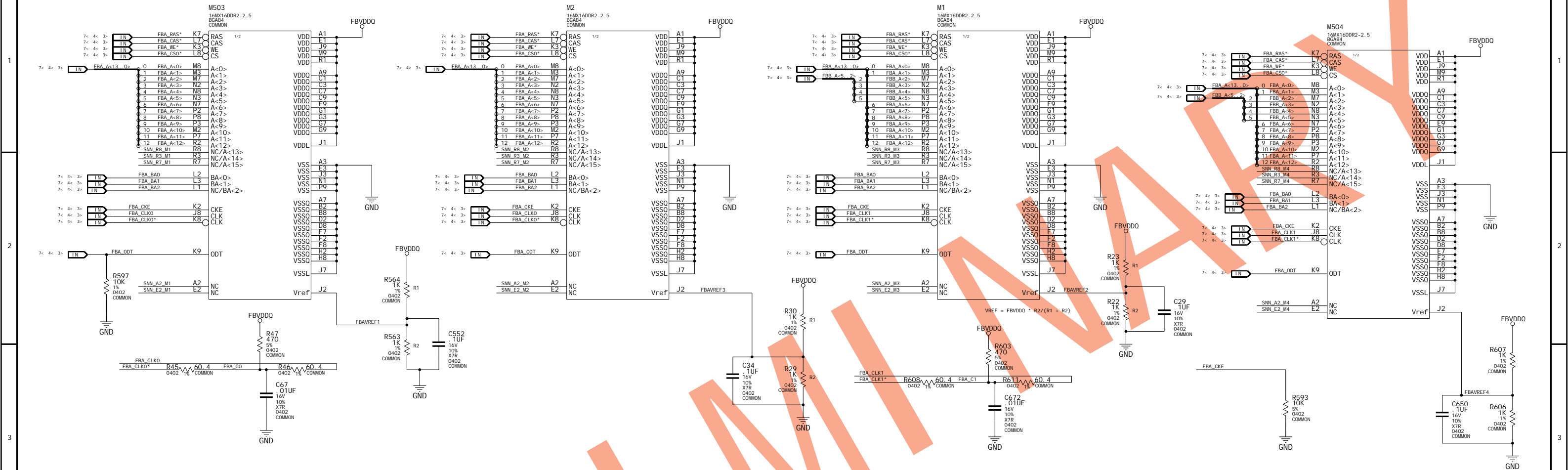
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PAGE DETAIL	PCI EXPRESS Interface

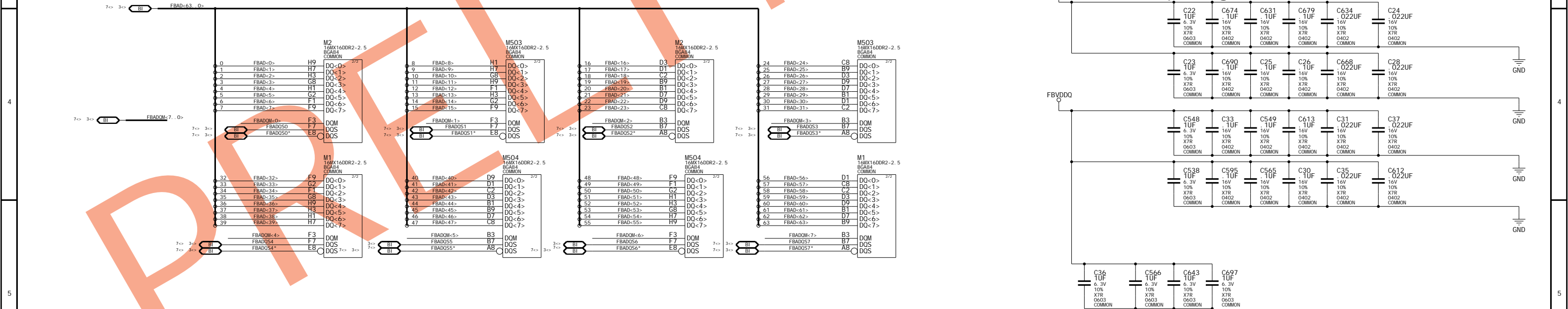
Frame Buffer A GPU



PAGE 4) MEMORY PARTITION A



Decoupling for FBA 0..31



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PAGE DETAIL Frame Buffer A Memories

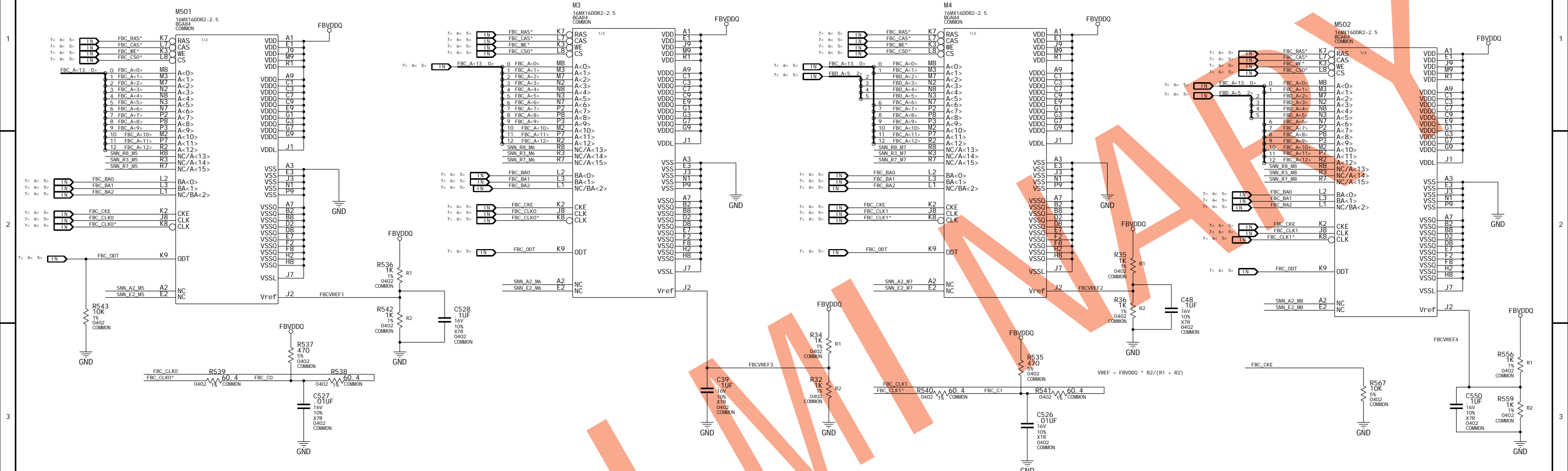
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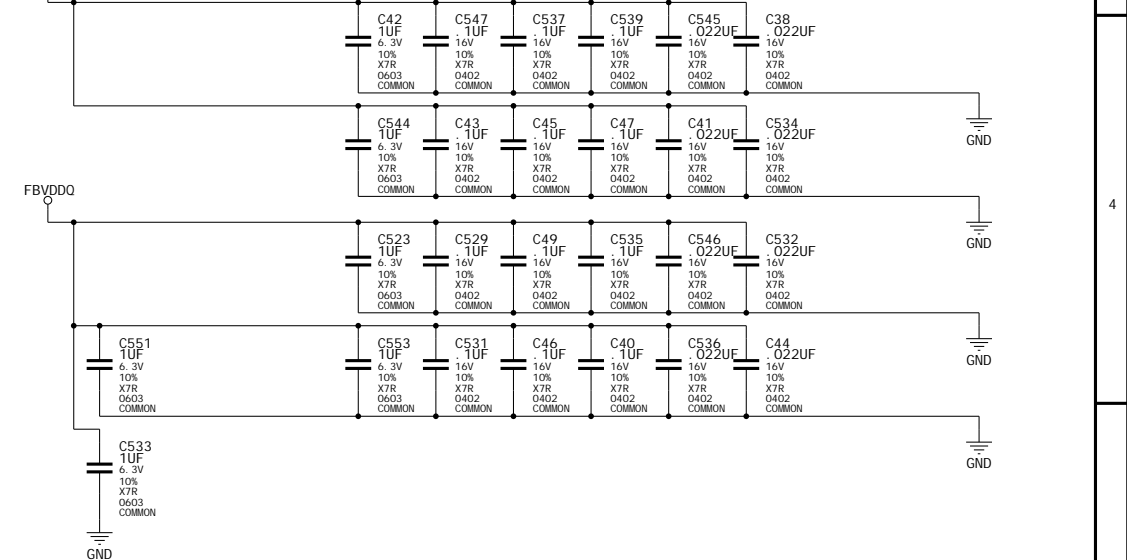
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PAGE 5) MEMORY PARTITION C





































Decoupling for FBC 0..31





































FrameBuffer Net Rules

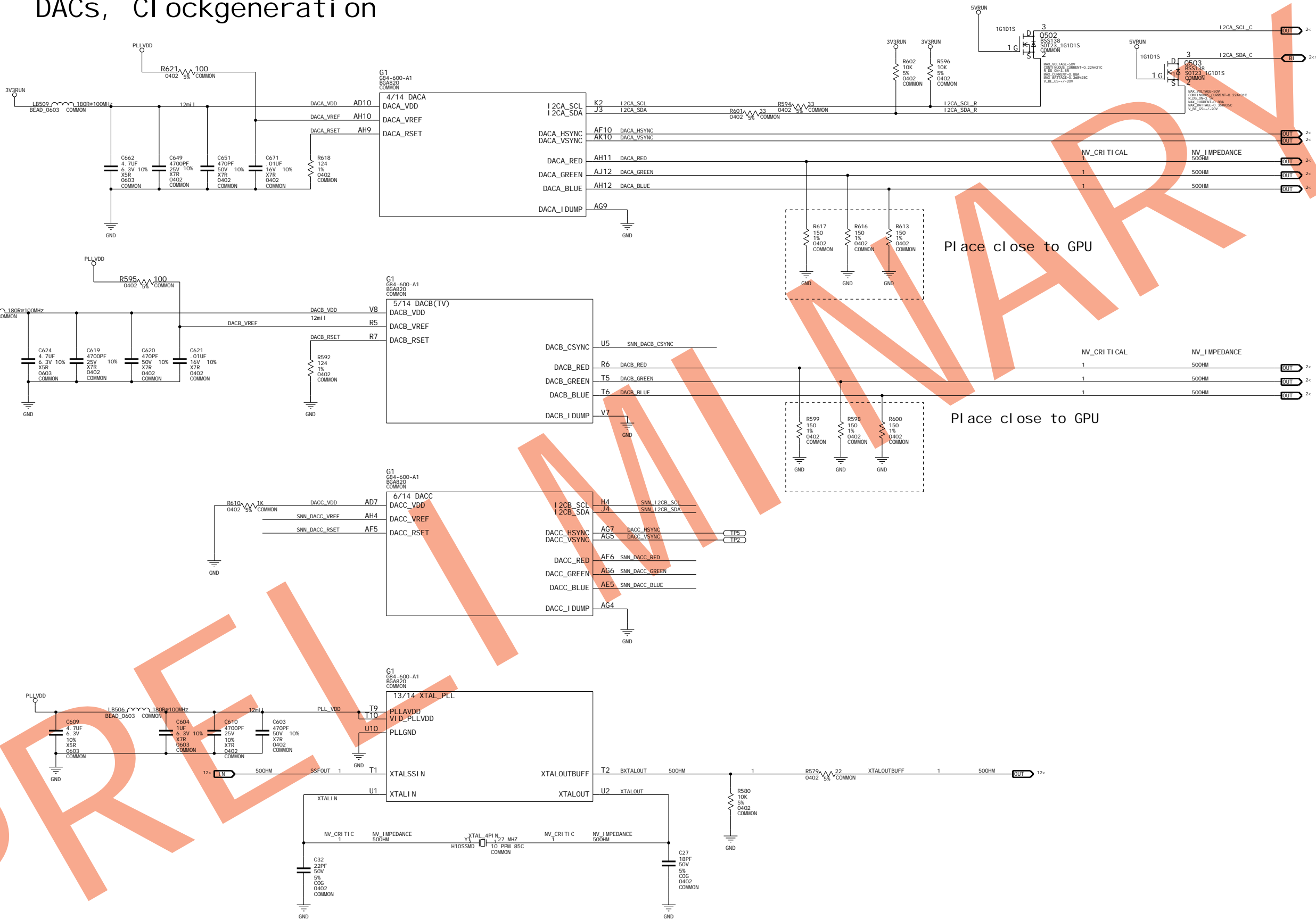
NET RULES for FrameBuffer A

	NET	DIFFPAIR	CRITICAL	IMPEDANCE
4< 3>	 FBA_CLK0	FBA_CLK0	1	100DIE
4< 3>	 FBA_CLK0*	FBA_CLK0	1	100DIE
4< 3>	 FBA_CLK1	FBA_CLK1	1	100DIE
4< 3>	 FBA_CLK1*	FBA_CLK1	1	100DIE
4< 3>	 FBAD0S0	FBAD0S0	1	100DIE
4< 3>	 FBAD0S0*	FBAD0S0	1	100DIE
4< 3>	 FBAD0S1	FBAD0S1	1	100DIE
4< 3>	 FBAD0S1*	FBAD0S1	1	100DIE
4< 3>	 FBAD0S2	FBAD0S2	1	100DIE
4< 3>	 FBAD0S2*	FBAD0S2	1	100DIE
4< 3>	 FBAD0S3	FBAD0S3	1	100DIE
4< 3>	 FBAD0S3*	FBAD0S3	1	100DIE
4< 3>	 FBAD0S4	FBAD0S4	1	100DIE
4< 3>	 FBAD0S4*	FBAD0S4	1	100DIE
4< 3>	 FBAD0S5	FBAD0S5	1	100DIE
4< 3>	 FBAD0S5*	FBAD0S5	1	100DIE
4< 3>	 FBAD0S6	FBAD0S6	1	100DIE
4< 3>	 FBAD0S6*	FBAD0S6	1	100DIE
4< 3>	 FBAD0S7	FBAD0S7	1	100DIE
4< 3>	 FBAD0S7*	FBAD0S7	1	100DIE
4< 3>	 FBA_A<12..0>		2	500HM
4< 3>	 FBA_A<5..2>		2	500HM
4< 3>	 FBA_BA0		2	500HM
4< 3>	 FBA_BA1		2	500HM
4< 3>	 FBA_CKE		2	500HM
4< 3>	 FBA_BA2		2	500HM
4< 3>	 FBA_RAS*		2	500HM
4< 3>	 FBA_CAS*		2	500HM
4< 3>	 FBA_WE*		2	500HM
4< 3>	 FBA_CS0*		2	500HM
4< 3>	 FBA_CS1*		2	500HM
4< 3>	 FBAD<63..0>		2	500HM
4< 3>	 FBAD<63..0>		2	500HM
4< 3>	 FBA_ODT		2	500HM

NET RULES for FrameBuffer C

	NET	DIFFPAIR	CRITICAL	IMPEDANCE
6< 5>	 FBC_CLK0	FBC_CLK0	1	100DIE
6< 5>	 FBC_CLK0*	FBC_CLK0	1	100DIE
6< 5>	 FBC_CLK1	FBC_CLK1	1	100DIE
6< 5>	 FBC_CLK1*	FBC_CLK1	1	100DIE
6< 5>	 FBAD0S0	FBAD0S0	1	100DIE
6< 5>	 FBAD0S0*	FBAD0S0	1	100DIE
6< 5>	 FBAD0S1	FBAD0S1	1	100DIE
6< 5>	 FBAD0S1*	FBAD0S1	1	100DIE
6< 5>	 FBAD0S2	FBAD0S2	1	100DIE
6< 5>	 FBAD0S2*	FBAD0S2	1	100DIE
6< 5>	 FBAD0S3	FBAD0S3	1	100DIE
6< 5>	 FBAD0S3*	FBAD0S3	1	100DIE
6< 5>	 FBAD0S4	FBAD0S4	1	100DIE
6< 5>	 FBAD0S4*	FBAD0S4	1	100DIE
6< 5>	 FBAD0S5	FBAD0S5	1	100DIE
6< 5>	 FBAD0S5*	FBAD0S5	1	100DIE
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6< 5>	 FBAD0S6*	FBAD0S6	1	100DIE
6< 5>	 FBAD0S7	FBAD0S7	1	100DIE
6< 5>	 FBAD0S7*	FBAD0S7	1	100DIE
6< 5>	 FBC_A<12..0>		2	500HM
6< 5>	 FBC_A<5..2>		2	500HM
6< 5>	 FBC_BA0		2	500HM
6< 5>	 FBC_BA1		2	500HM
6< 5>	 FBC_CKE		2	500HM
6< 5>	 FBC_BA2		2	500HM
6< 5>	 FBC_RAS*		2	500HM
6< 5>	 FBC_CAS*		2	500HM
6< 5>	 FBC_WE*		2	500HM
6< 5>	 FBC_CS0*		2	500HM
6< 5>	 FBC_CS1*		2	500HM
6< 5>	 FBAD<63..0>		2	500HM
6< 5>	 FBAD<63..0>		2	500HM
6< 5>	 FBC_ODT		2	500HM

DACs, Clockgenerati on



Place close to GPU

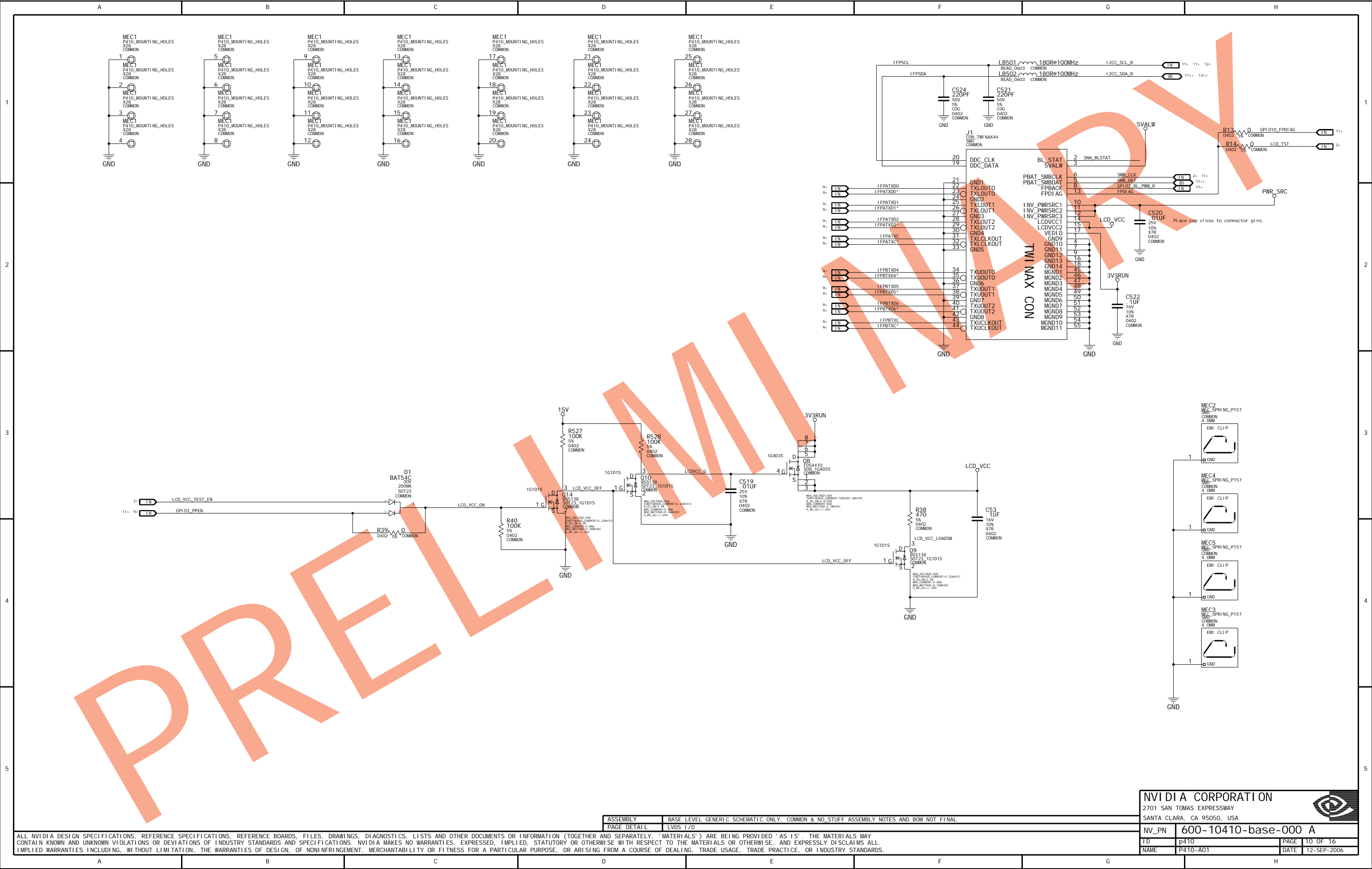
Place close to GPU

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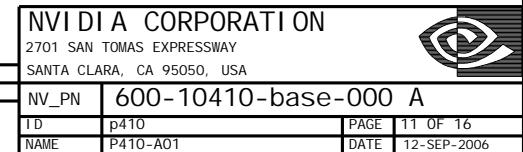
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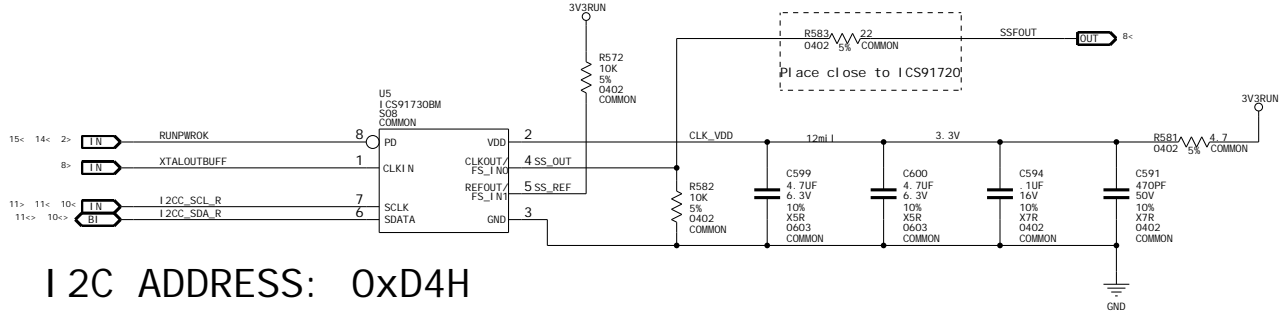


I 2C ADDRESS: 0x98H



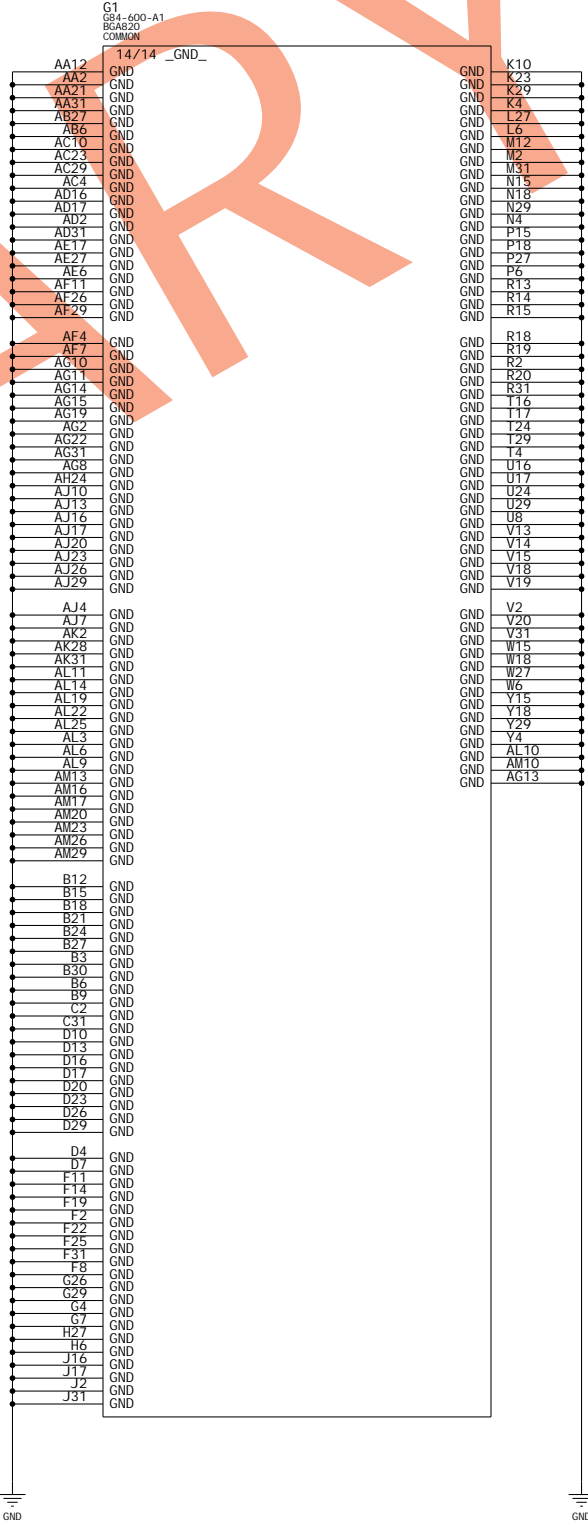
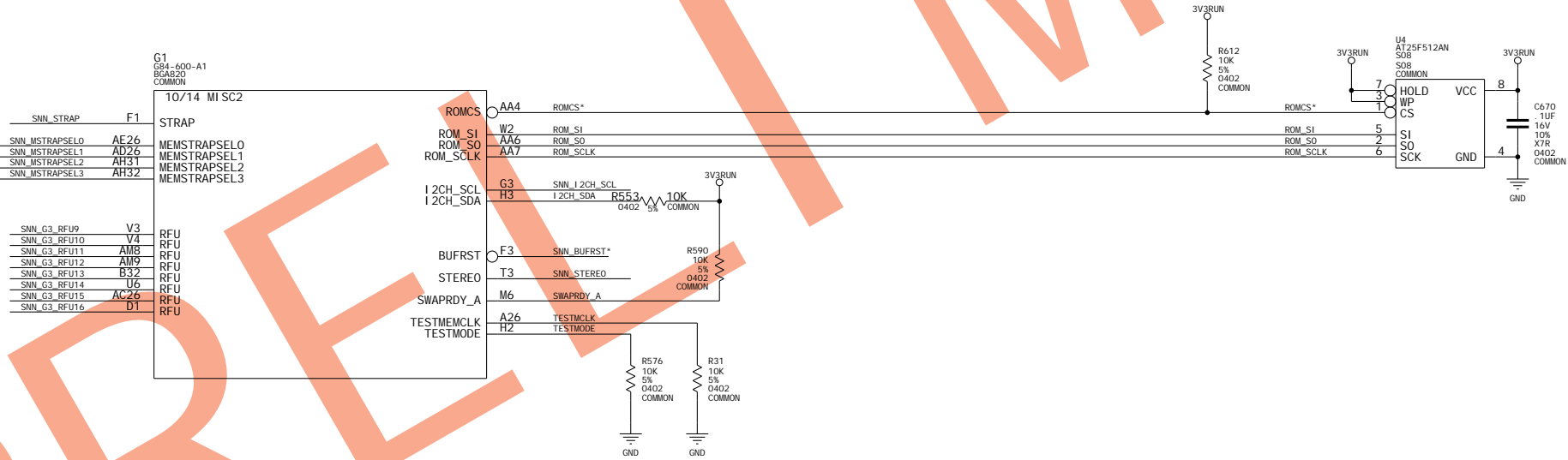
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SPREAD SPECTRUM CLOCK

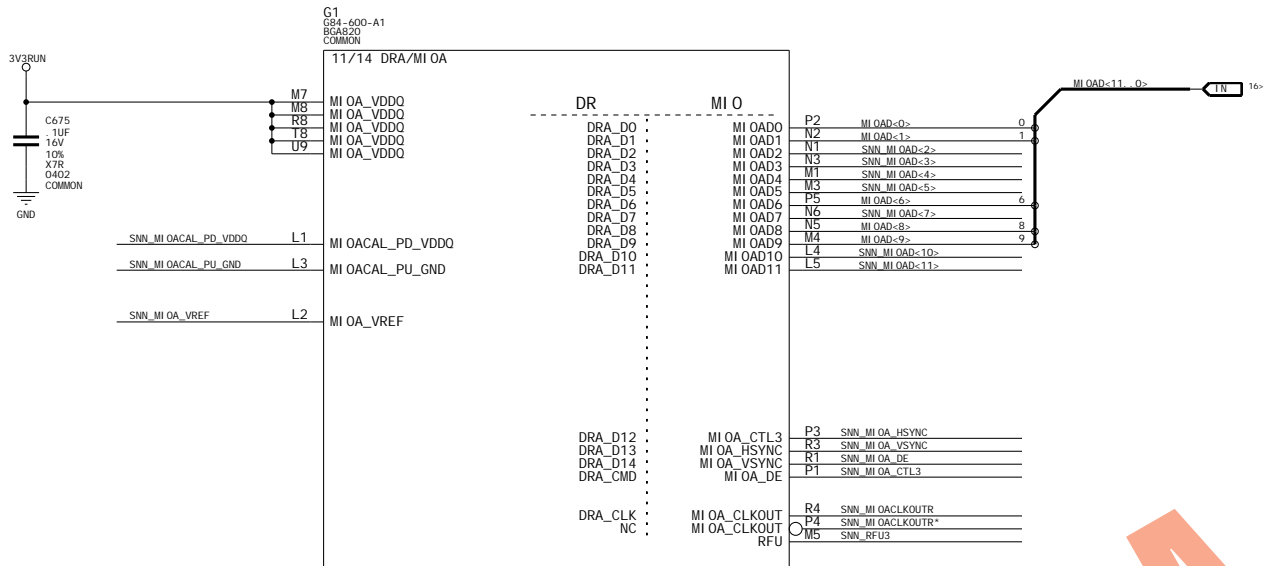


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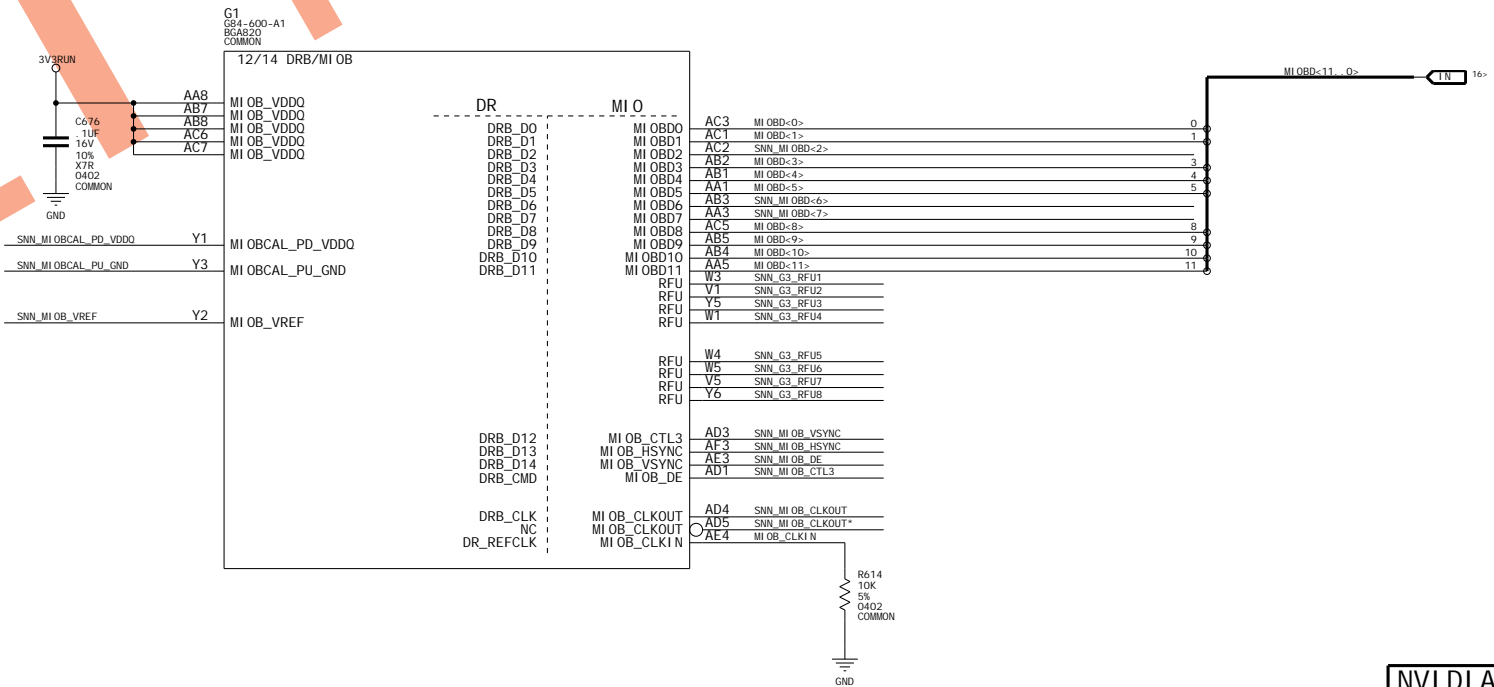
ROM Interface



MI OA



MI OB



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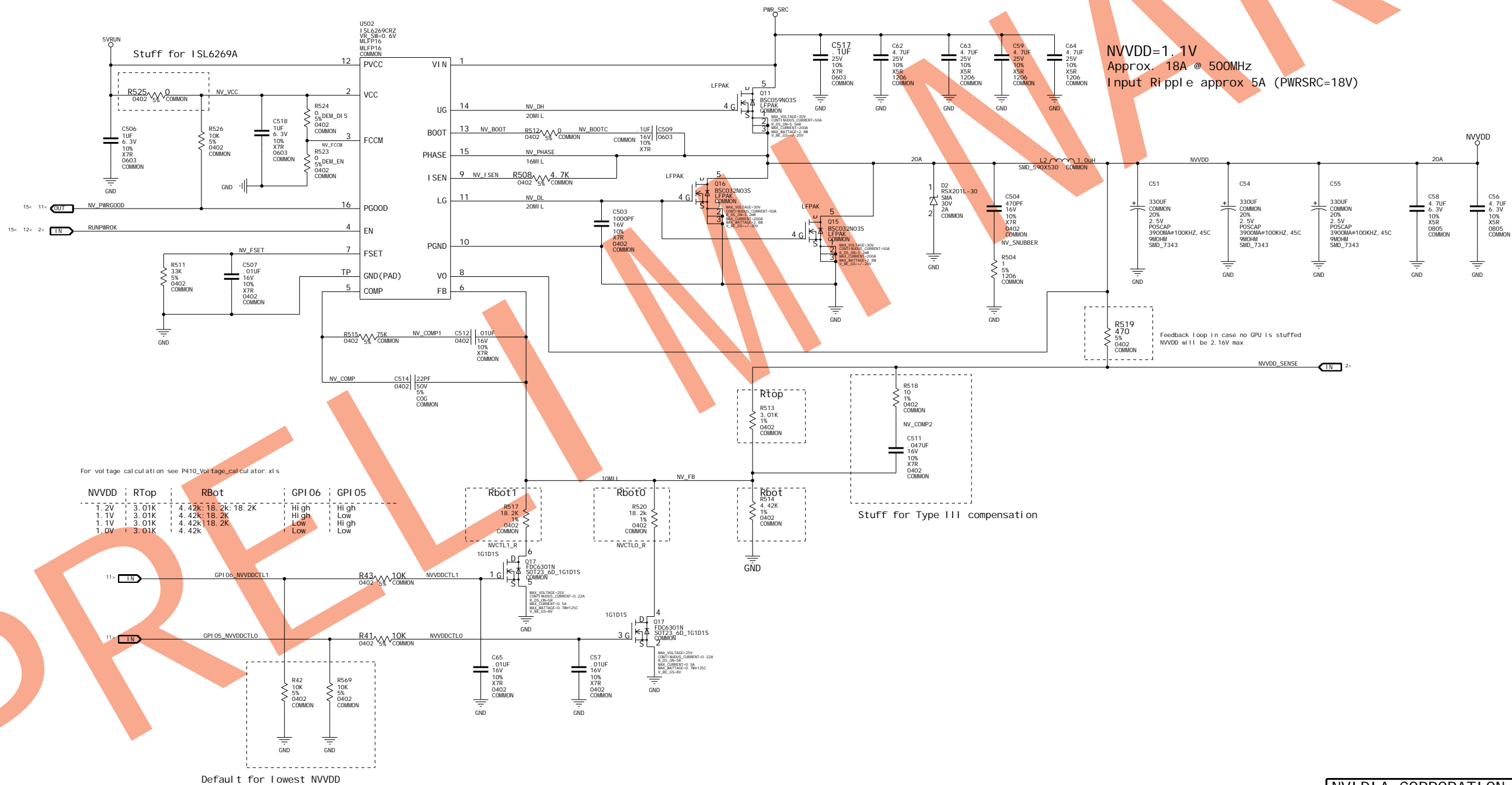
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NVVDD SUPPLY

NET	M I N _ L I N E _ W I D T H	VOLTAGE
FBVDDO	12MIL	1.8V
NVDD	12MIL	1.2V



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[illegible]

The circuit diagram shows the APL5913 (U1) configured as a precision current source. The input voltage is 5V, and the output current is 2.0A. The feedback network consists of a 470pF capacitor (C3) and a 511 Ohm resistor (R1). The load resistor is 0.02K (R2). The output voltage is 1.2V.

Component values and connections:


- U1: APL5913, SOP8, COMMON
- VCNTL: 6
- VI N: 5
- VI N: 9
- EN POK: 8
- POK: 7
- GND: 4
- VOUT VOUT: 3
- PEX1V2_FB: 2
- C2: 100nF, 6.3V, 10%, X7R, 0603, COMMON
- C3: 470pF, 16V, 10%, X7R, 0402, COMMON
- R1: 511 Ohm, 1%, 0402, COMMON
- R2: 0.02K, 1%, 0402, COMMON
- Rtop: 2.0A
- Rbot: 0.02K
- C1: 4.7uF, 6.3V, 10%, X5R, 0603, COMMON
- PEX1V2: 1.2V

Formula for output voltage:

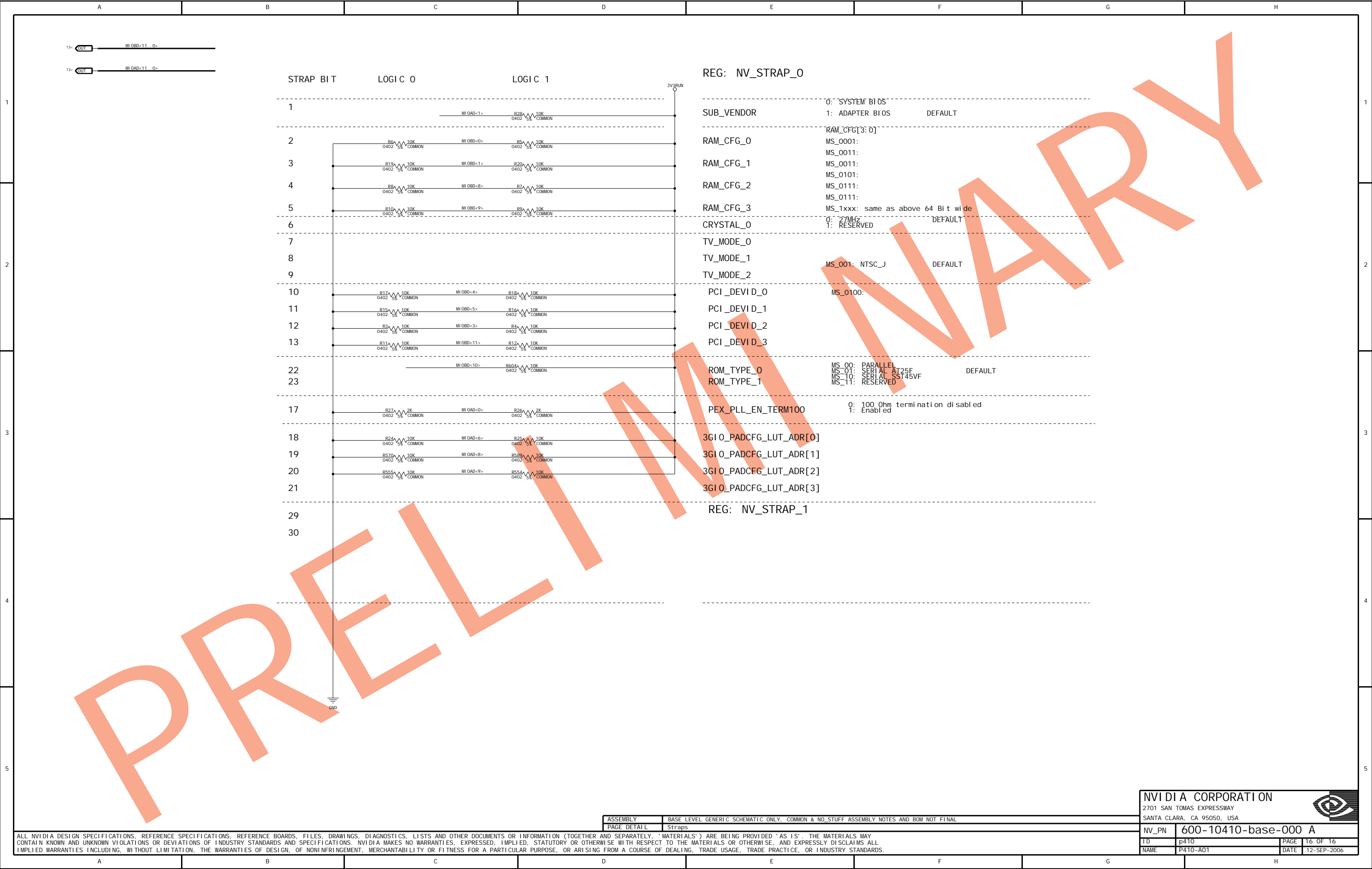
$$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$$

Calculation:

$$1.2V = 0.8V * (1 + 511 / 1.02K)$$
[illegible]

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REG: NV_STRAP_0

	0: SYSTEM BIOS	
SUB_VENDOR	1: ADAPTER BIOS	DEFAULT
	RAM_CFG[3:0]	
RAM_CFG_0	MS_0001:	
RAM_CFG_1	MS_0011:	
RAM_CFG_2	MS_0101:	
RAM_CFG_3	MS_0111:	
	MS_1xxx: same as above 64 Bit wide	
CRYSTAL_0	0: 27MHz	DEFAULT
	1: RESERVED	
TV_MODE_0		
TV_MODE_1	MS_001: NTSC_J	DEFAULT
TV_MODE_2		
PCI_DEVID_0	MS_0100:	
PCI_DEVID_1		
PCI_DEVID_2		
PCI_DEVID_3		
	MS_00: PARALLEL	
ROM_TYPE_0	MS_01: SERIAL AT25F	DEFAULT
ROM_TYPE_1	MS_10: SERIAL SST45Vf	
	MS_11: RESERVED	

PEX_PLL_EN_TERM100 0: 100 Ohm termination disabled
1: Enabled

3GIO_PADCFG_LUT_ADR[0]
3GIO_PADCFG_LUT_ADR[1]
3GIO_PADCFG_LUT_ADR[2]
3GIO_PADCFG_LUT_ADR[3]

REG: NV_STRAP_1