電子類元件 零件承認書文件 CHECK LIST

零件廠商： **AOS** **品名規格：** DR MOS AOZ5036QI-01 60A AOS

技嘉料號： 10IFD-605036-01R

項次	文件項目
	Data Sheet 檢核項目
1	DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2**
8	零件樣品 20PCS(Chipset 等高單價，至少 1PCS)
9	**電子零件承認基本調查表。註 3**
10	以上資料電子檔為 PDF 檔，且是同 1 個 File
	GSCM 綠色產品管理系統-物料管制文件檢核清單
物料管制文件 1	GSCM 綠色產品管理系統：零件照片
物料管制文件 2	GSCM 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4**
物料管制文件 3	GSCM 綠色產品管理系統：Data Sheet
	GSCM 綠色產品管理系統-MCD 表格
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
	其他文件 (僅適用電阻、電容類之系列元件)
附件 1	危害物質測試報告 Test Report of Hazardous Substances。**註 5**
附件 2	元件調查表 Component Composition Table

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等

※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)

2.1. 基本需符合 JEDEC 規範

2.2. Ambient Temp. (Reflow Temp endurace): >225℃, 70 sec. 零件塑膠材質需 PA9T(含)等級以上

2.3. PASTE IN HOLE 零件塑膠材質需 PA9T(含)等級以上

※ **3. 電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G*,11T***

非 IC 類：10C*,11C*,10L*,11L*,10X*,11X*,10R*,11B*

※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”

※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

電子零件承認基本調查表

一、原物料規格/來源			
項次	部位名稱/規格	材質	原物料來源產地
1	BONDING WIRE	Metal	SINGAPORE,PANDAN CRESCENT
2	DIE ATTACH_1	Adhesives	CALIFORNIA,USA
3	DIE ATTACH_2	Adhesives	SUZHOU,CHINA
4	CHIP	WAFER	HILLSBORO,USA HAEMEK,ISRAEL
5	LEADFRAME	Metal	YINZHOU,CHINA
6	LEADFINISH	Metal materials plating layer	SHANGHAI,CHINA
7	MOLD COMPOUND	Epoxy Resin	SUZHOU,CHINA

二、晶圓廠(非 IC 類免填)					
項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	JIREH	USA,OR	8	100	自有
2	TOWRJAZZ	USA,CA	6	100	外包
3					

三、封裝廠(IC 類)；成品之生產製造工廠(非 IC 類)				
項次	工廠名稱	生產產地	投產比率(%)	自有/外包
1	AOS	CHINA	100	自有
2				
3				

四、產能	
總產能(月/PCS)	可供技嘉產能(月/PCS)
200K	200K

※ 1. IC 類之晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 2. 非 IC 類零件之成品生產製造工廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 3. 以上資訊欄位若有不足，可自行增加行數

承認書

SPECIFICATION APPROVAL FORM

廠　　商：技嘉科技股份有限公司

承認書編號：

品　　名：**AOZ5036QI-01**

規　　格：QFN-40L

數　　量：

承 辦 人：**Daniel Liu**

日　　期：**2017/7/24**

用　　途：

公 司 承 認 章	廠 商 承 認 章
	志遠電子股份有限公司 代理專用章 TEL:8226-7698 FAX:2225-8960 TECHMOSA INTERNATIONAL INC.

志遠電子股份有限公司

TECHMOSA INTERNATIONAL INC.

台北縣中和市立德街 118 號 6F

TEL: (02) 8226-7698　　FAX: (02) 2651-3280

AOZ5036

60A DrMOS Power Module

General Description

The AOZ5036 is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The high side MOSFET has low capacitance and gate charge for fast switching with low duty cycle operation. The low side MOSFET has ultra low $R_{DS(ON)}$ to minimize conduction losses.

The AOZ5036 is available with two PWM options. AOZ5036QI is intended for use with TTL compatible PWM inputs. AOZ5036QI-01 has lower thresholds on the PWM signal and can operate with 3V inputs. All other parameters are identical for the two versions. Both versions are tri-state compatible that allows both power MOSFETs to be turned off.

A number of features are provided making the AOZ5036 a highly versatile power module. The boot supply diode is integrated in the driver. The low side MOSFET can be driven into diode emulation mode to provide asynchronous operation when required. The pinout is optimized for low inductance routing of the converter keeping the parasitics and their effects to the minimum.

Features

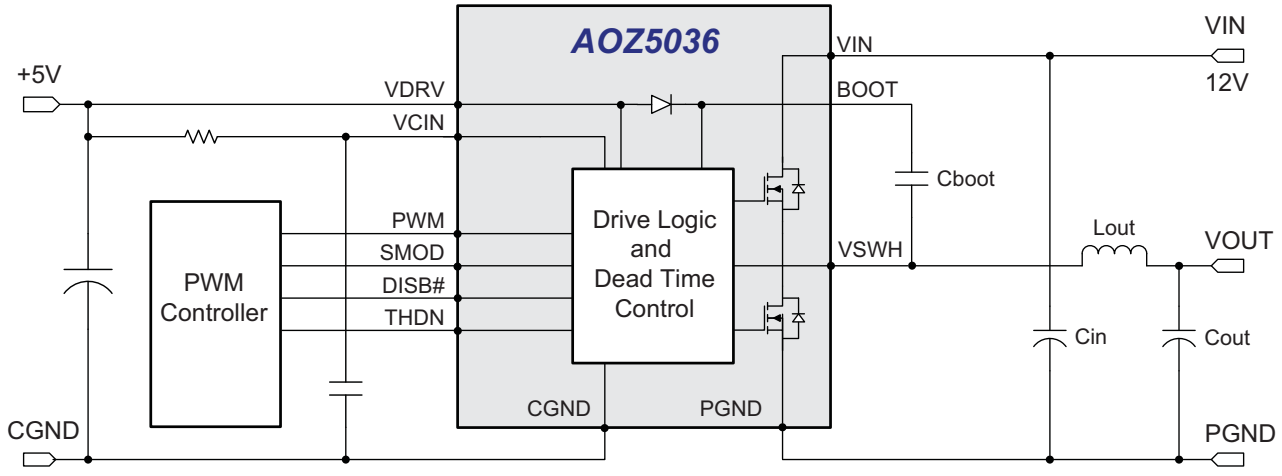
- Fully complies with Intel DrMOS Rev 4.0 specifications
- 4.5V to 16V input voltage range
- 4.5V to 5.5V driver supply range
- Up to 60A output current
- Up to 1MHz PWM operation
- Tri state PWM input
- Undervoltage protection
- Integrated boot supply diode
- Diode Emulation mode of operation
- Thermal shutdown alarm with flag
- Small 6x6 QFN-40L package

Applications

- Servers
- VRMs for motherboards
- Point of load DC/DC converters
- Memory and graphic cards
- Video gaming consoles

Green Product

Typical Application Circuit

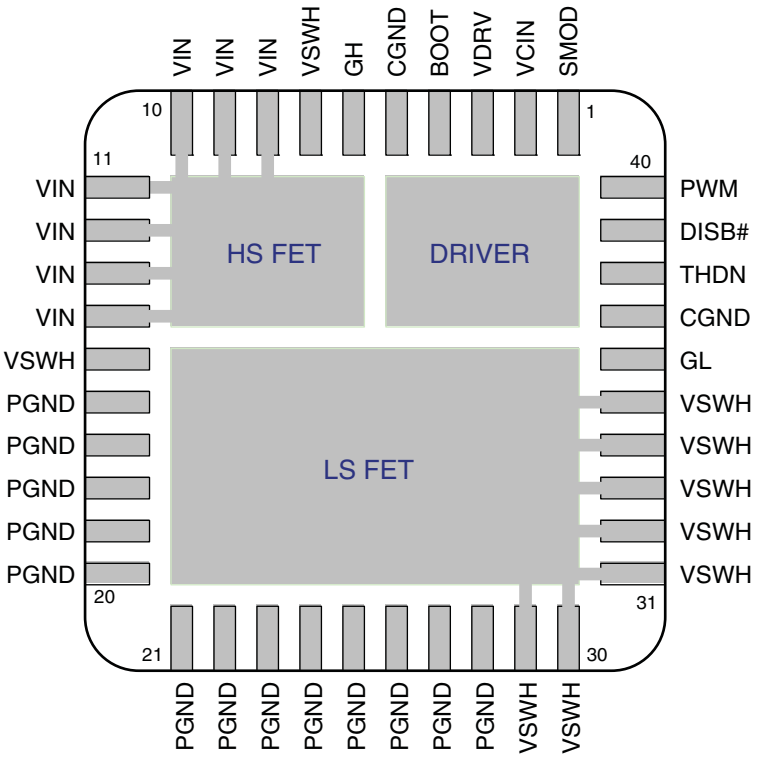


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5036QI*	-40°C to +85°C	6x6 QFN-40L	Green Product
AOZ5036QI-01			

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.
* Contact factory for availability.

Pin Configuration

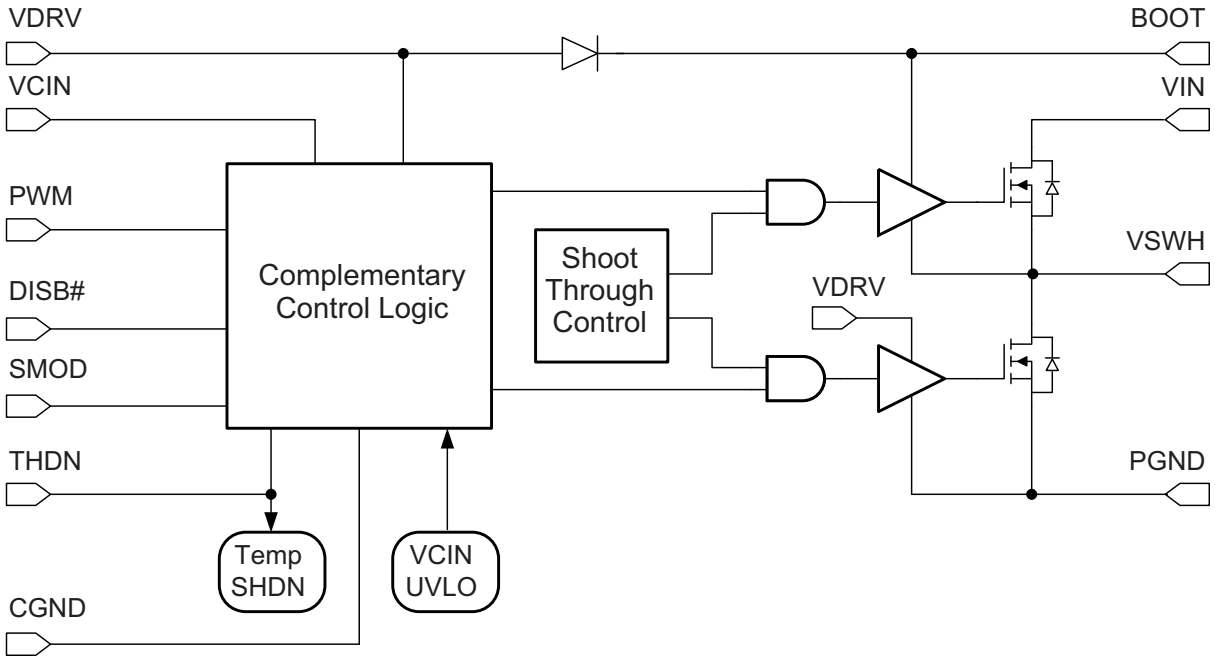


6x6 QFN-40
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	SMOD	Skip Mode input. When the pin is held active low, Diode Emulation or Skip Mode is enabled for the LS FET.
2	VCIN	Control supply input. Nominal 5V. Can be derived from the gate drive supply VDRV with an RC filter for noise bypass.
3	VDRV	Gate drive supply input. Nominal 5V.
4	BOOT	Gate drive supply for the HS FET. Nominal 5V. The bootstrap diode is internal to the module. Connect a 0.1µF or higher ceramic capacitor between VSWH node at pin 7.
5, 37	CGND	Control or analog ground for return of control signals and bypass capacitors. Attached to exposed pad in the driver section.
6	GH	Gate of the HS FET. Used for module testing during production. No user connections.
7	VSWH	Switching or the phase node for bootstrap capacitor connection.
8 to 14	VIN	Power input to the switching MOSFETs. Attached to the HS FET drain tab.
15	VSWH	Switching or the phase node pin. Not for power connections.
16 to 28	PGND	Power ground. Internally connected to control GND of pin 37.
29 to 35	VSWH	Switching or phase node connected to source of high side MOSFET and drain of the low side MOSFET. Electrically attached to the LS FET drain tab.
36	GL	Gate of the LS FET. Used for module testing during production. No user connections.
38	THDN	Open drain output of the thermal shutdown circuit. Active low.
39	DISB#	Disable pin for the controller. Both gates are held active low when DISB# is grounded.
40	PWM	Pulse Width Modulated Tri State input from external controller.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (VIN)	-0.3V to 25V
Switch Node Voltage (VSWH) (1)	-8V to 25V
Bootstrap Voltage (VBOOT)	-0.3V to 25V
VBOOT Voltage Transient (1)	36V
Supply and Gate Drive Voltages {VCIN, VDRV, (VBOOT – VSWH)}	-0.3V to 7V
Control Inputs (PWM, SMOD, DISB#)	-0.3V to VCIN+0.3 V
Storage Temperature (T_S)	-65°C to +150°C
Junction Temperature (T_J)	+150°C
ESD Rating(2)	2kV

Notes:

1. Peak voltages can be applied for 100nS per switching cycle.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (VIN)	4.5V to 16V
Supply and Gate Drive Voltages {VCIN, VDRV, (VBOOT – VSWH)}	4.5V to 5.5V
Control Inputs (PWM, SMOD, DISB#)	0V to VCIN – 0.3V
Operating Frequency	200kHz to 1MHz

Electrical Characteristics(3)

T_A = 25°C, V_{IN} = 12V, VDRV = VCIN = 5V unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIN	Operating Voltage		4.5		16	V
VCIN		VDRV Tied to VCIN	4.5		5.5	V
$R_{\theta JC}$(4)	Thermal Resistance	PCB Temp = 100°C		5.0		°C / W
$R_{\theta JA}$ (4)				50		°C / W
INPUT SUPPLY AND UVLO						
V_{CINON}	Undervoltage Lockout	V_{CIN} Rising		3.5	3.9	V
$V_{CINHYST}$		V_{CIN} Falling		550		mV
I_{VCIN}	Control Circuit Bias Current	DISB# = 0, VCIN = 5V		50	75	µA
		DISB# = High, V_{PWM} = Open		350	500	µA
		DISB# = High, V_{PWM} = 0V		650		µA
I_{VDRV}	Drive Circuit Operating Current	DISB# = High, V_{PWM} = 300kHz @ 50%		46		mA
		DISB# = High, V_{PWM} = 1MHz @ 50%		152		mA
PWM INPUT (AOZ5036QI)*						
V_{PWMH}	PWM Input High Threshold	V_{PWM} Rising, VCIN = 5V	3.6	3.9	4.1	V
V_{PWML}	PWM Input Low Threshold	V_{PWM} Falling, VCIN = 5V	0.8	1.0	1.2	V
I_{PWM}	PWM Pin Input Current	Source or Sink, V_{PWM} = 0V to 5V		±250		µA
V_{TRIH}	PWM Input Tri State Threshold	V_{PWM} Rising, VCIN = 5V	1.0	1.3	1.6	V
V_{TRIL}		V_{PWM} Falling, VCIN = 5V	3.4	3.7	4.0	V
V_{TRRH}	Tri State Threshold Hysteresis	V_{PWM} Rising, VCIN = 5V		280		mV
V_{TRFH}		V_{PWM} Falling, VCIN = 5V		170		mV

* Contact factory for availability.

Electrical Characteristics[3] (Continued)

T_A = 25°C, V_{IN} = 12V, VDRV = VCIN = 5V unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PWM INPUT (AOZ5036QI-01)						
V_{PWMH}	PWM Input High Threshold	V_{PWM} Rising, VCIN = 5V	1.8	2.0	2.2	V
V_{PWML}	PWM Input Low Threshold	V_{PWM} Falling, VCIN = 5V	0.8	1.0	1.2	V
I_{PWM}	PWM Pin Input Current	Source or Sink, V_{PWM} = 0V to 3V		±10		µA
V_{TRIH}	PWM Input Tri State Threshold	V_{PWM} Rising, VCIN = 5V	1.15	1.3	1.45	V
V_{TRIL}		V_{PWM} Falling, VCIN = 5V	1.65	1.75	1.9	V
V_{TRRH}	Tri State Threshold Hysteresis	V_{PWM} Rising, VCIN = 5V		300		mV
V_{TRFH}		V_{PWM} Falling, VCIN = 5V		300		mV
DISB# INPUT						
V_{DISBON}	Outputs Enable Threshold	VCIN = 5V	2.0			V
$V_{DISBOFF}$	Outputs Disable Threshold	VCIN = 5V			0.8	V
I_{DISB}	DISB# pin input current	Source or Sink		±10		µA
SMOD INPUT						
V_{SMODH}	SMOD Enable Threshold	VCIN = 5V	2.0			V
V_{SMODL}	SMOD Disable Threshold	VCIN = 5V			0.8	V
I_{SMOD}	SMOD Pin Input Current	Source or Sink		±10		µA
GATE DRIVER TIMINGS						
t_{PDLU}	PWM to HS Gate	PWM H → L, GH H → L		20		ns
t_{PDLL}	PWM to LS Gate	PWM L → H, GL H → L		35		ns
t_{PDHU}	LS to HS Gate Deadtime	GL H → L, GH L → H		16		ns
t_{PDHL}	HS to LS Gate Deadtime	GH H → L, GL L → H		17		ns
t_{TSSHD}	Tri State Shutdown Delay			170		ns
t_{PTS}	Tri State Propagation Delay			35		ns
THERMAL SHUTDOWN[5]						
T_{JTHDN}	Shutdown Threshold			150		°C
T_{JHYST}	Hysteresis			15		°C
V_{THDNL}	THDN Pin Output Low	5kΩ pull up resistor to VCIN		0.06		V
R_{THDNL}	THDN Pull Down Resistance			60		Ω
MOSFET RATINGS[6]						
V_{DS}	Voltage Rating		25			V
R_{DSHS}	Drain Source On Resistance	High Side MOSFET		6		mΩ
R_{DSLS}		Low Side MOSFET		1.6		mΩ

Notes:

3. All voltages are specified with respect to the corresponding GND pin
4. Characterisation value. Not tested in production.
5. Temperature sensed on the driver pad
6. Values given for reference only.

Typical Performance Characteristics

Unless otherwise noted, VIN = 12V, VDRV = VCIN = 5V, F_{sw} = 670kHz, L_{out} = 470nH, V_{out} = 1.2V.
Loss and efficiency measured on AOS evaluation board at T_A = 25°C. No forced air for module loss < 7W.
Module loss includes power MOSFET loss plus drive circuit loss.
Power train consists of AOZ5036 power module plus output inductor IHLP6767GZERR47M01.
Power train efficiency does not include other losses in the test board.

Fig 1. Module Loss vs. Load Current

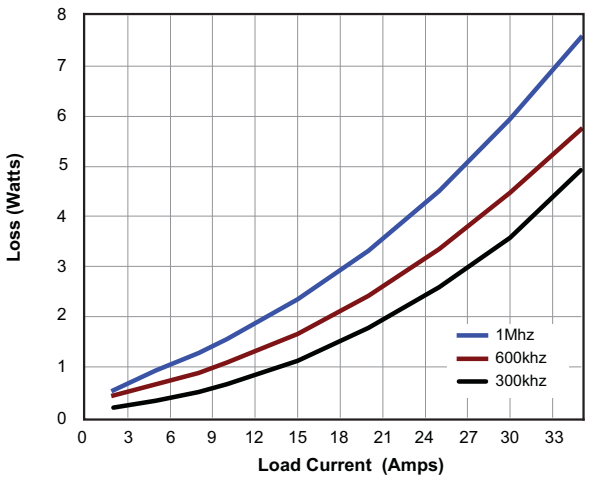


Fig 2. Power Train Efficiency vs. Load Current

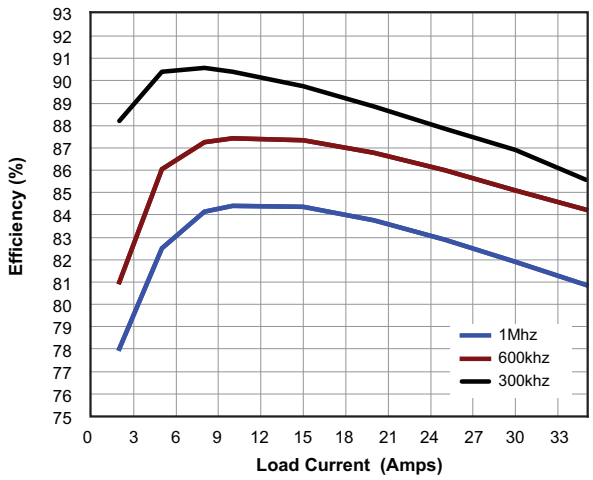


Fig 3. Normalised Module Loss and Power Train Efficiency vs. Drive Voltage

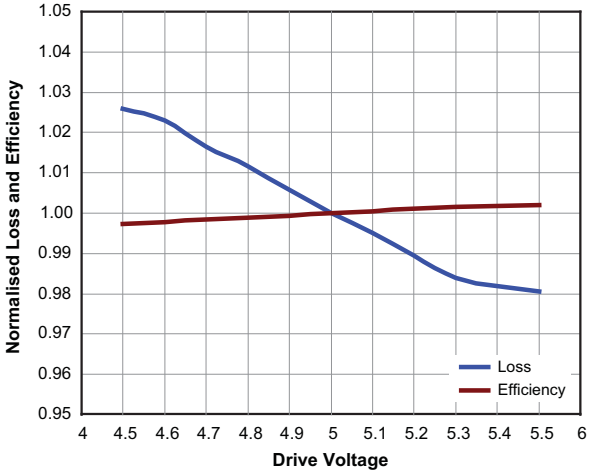
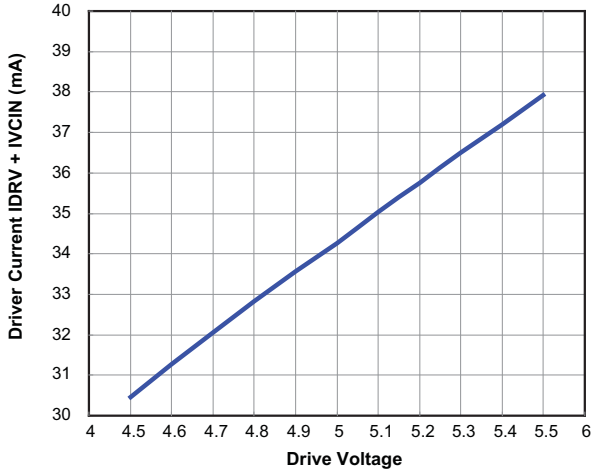


Fig 4. I_{DRV} + I_{VCIN} vs. Drive Voltage



Typical Performance Characteristics (Continued)

Fig 5. Normalised I_{DRV} + I_{VCIN} vs. Operating Frequency

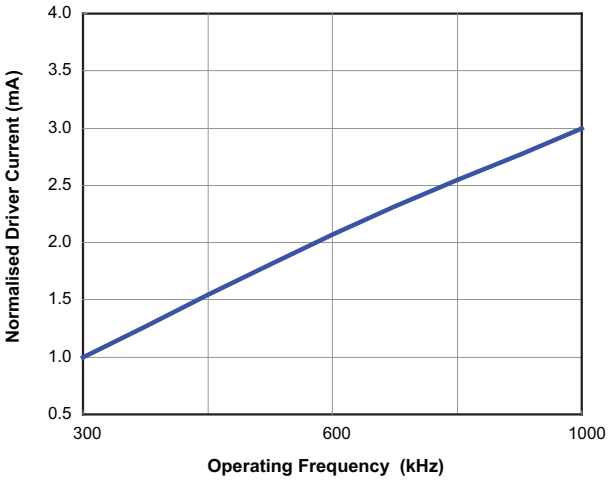


Fig 6. I_{DRV} + I_{VCIN} vs. Temperature

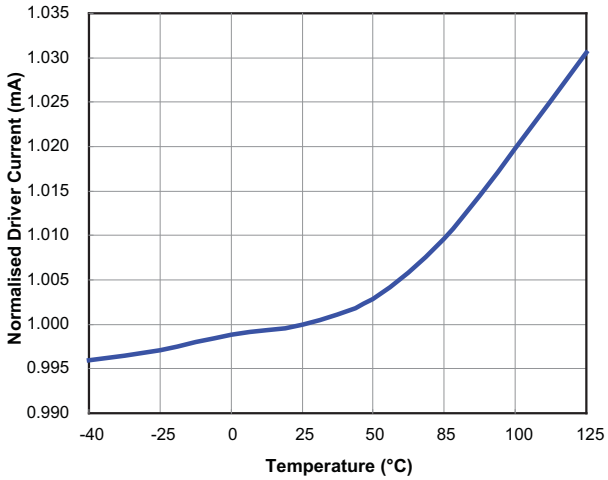


Fig 7. VDRV UVLO Threshold vs. Temperature

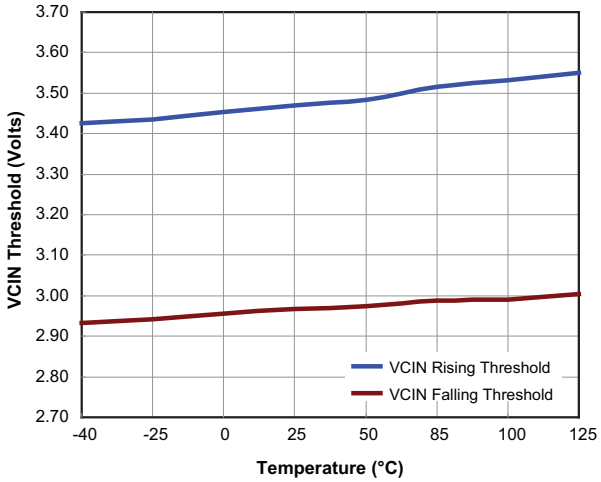


Fig 8. PWM Input Threshold vs. Temperature

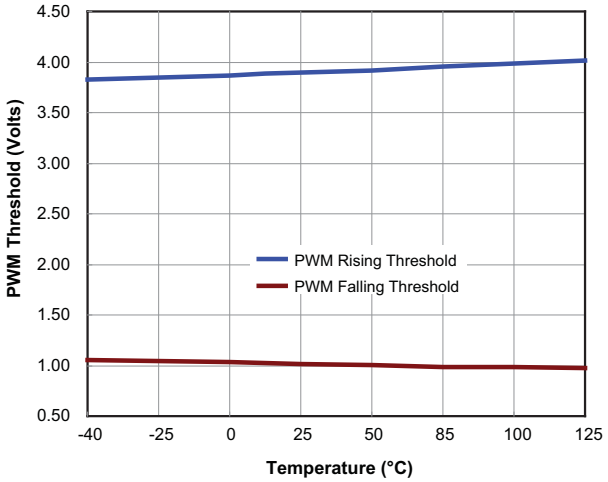


Fig 9. PWM Input Tristate Threshold vs. Temperature

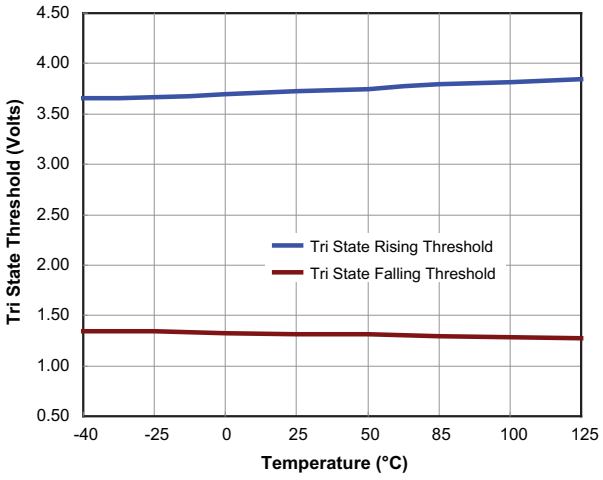
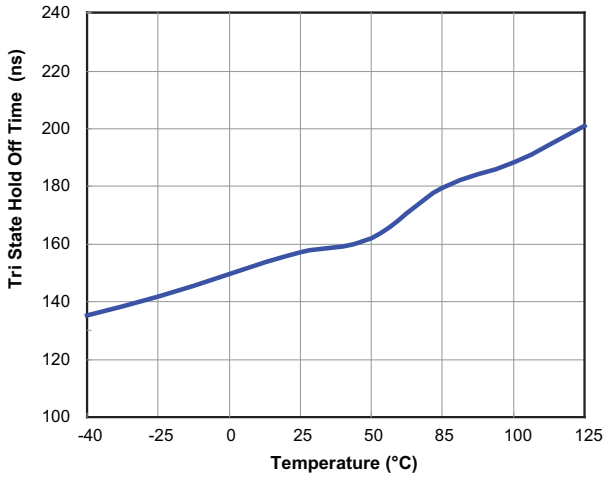


Fig 10. PWM Input Tri State Hold Off Time vs. Temperature



Typical Performance Characteristics (Continued)

Fig 11. DISB# Input Threshold vs. Temperature

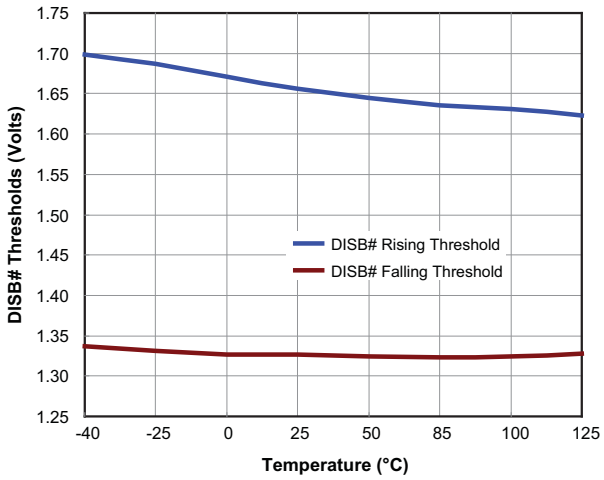
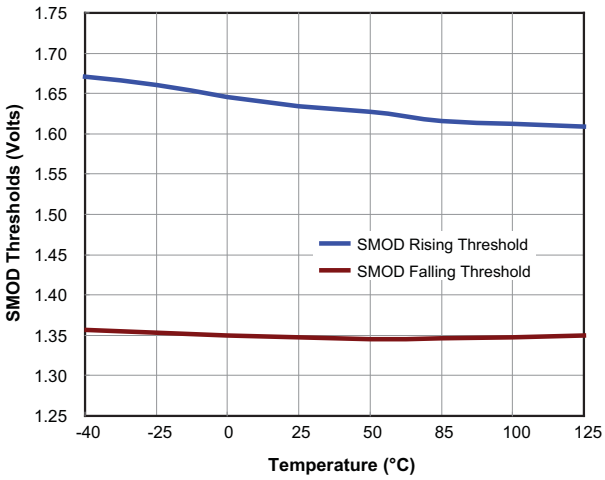


Fig 12. SMOD Input Threshold vs. Temperature



Timing Diagram

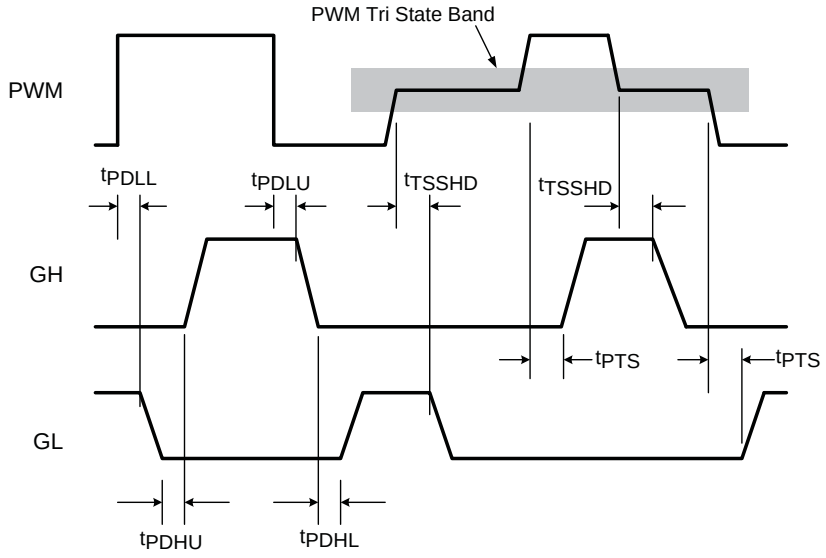


Figure 13. Timing Diagram

Application Information

AOZ5036QI and AOZ5036QI-01 are fully integrated power modules designed to work over an input voltage range of 4.5V to 16V with 5V supplies for gate drive and internal control circuits. A number of features are provided making the AOZ5036QI a highly versatile power module. High side and low side power MOSFETs are combined in one package with the pin outs optimized for power routing with minimum parasitic inductances. The MOSFETs are individually tailored for efficient operation as either high side or low side switches in a low duty cycle synchronous buck converter. A high current driver is also included in the package which minimizes the gate drive loop and results in extremely fast switching. The modules are fully compatible with Intel DrMOS specification Rev 4.0 in form fit and function.

Powering the Module and the Gate Drives

An external supply VDRV of 5V is required for driving the MOSFETs. The MOSFETs are designed with low gate thresholds so that lower drive voltage can be used to reduce the switching and drive losses without compromising the conduction losses. The control logic supply VCIN can be derived from the gate drive supply VDRV through an RC filter to bypass the switching noise. See Figure 14 for recommended gate drive supply connections. The gate driver is capable of supplying several amperes of peak current into the LS FET to achieve extremely fast switching. A ceramic bypass capacitor of 1μF or higher is recommended from VDRV to CGND.

The boost supply for driving the high side MOSFET is generated by connecting a small capacitor between BOOT pin and the switching node VSWH. It is recommended that this capacitor Cboot be connected as close as possible to the device across pins 4 and 7. Boost diode is integrated into the package. Rboot is an optional resistor used by designers to slow down the turn on speed of the high side MOSFET. The value is a compromise between the need to keep both the switching time and VSWH node spikes as low as possible and is typically 1Ω to 5Ω.

Undervoltage Lockout and Enable

VCIN is monitored for UVLO conditions and both outputs are actively held low unless adequate gate supply is available. The undervoltage lockout is set at 3.5V with a 550mV hysteresis. Since the PWM control signals are provided typically from an external controller or a digital processor extra care must be taken during start up. The AOZ5036QI must be powered up and enabled before the PWM input is applied. It should be ensured that PWM signal goes through a proper soft start sequence to minimise inrush current in the converter during start up. Powering the module with a full duty cycle PWM signal already applied may lead to a number of undesirable consequences as explained below.

Outputs can also be turned off through the DISB# pin. When this input is grounded the drivers are disabled and held active low. The module is in standby mode with low quiescent current of less than 75μA.

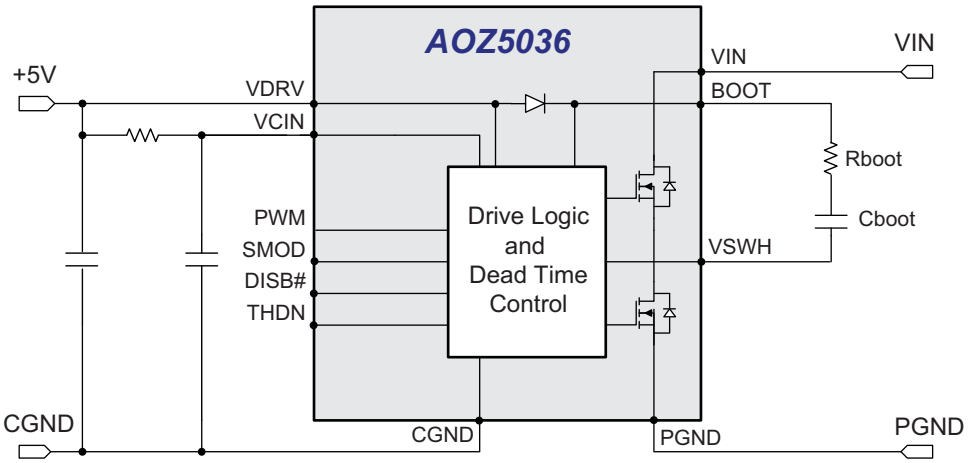


Figure 14. Applying VDRV and Generating BOOT Supply

IMPORTANT: If the DISB# is used it is necessary to ensure proper coordination with soft start and enable features of the external PWM controller in the system. Every time AOZ5036QI is disabled through DISB# there will be no output and the external controller may enter into open loop and put out a PWM signal with maximum duty ratio possible. If the AOZ5036QI is re-enabled by taking DSBL# high, there will be extremely large inrush currents while the output voltage builds up again which may drive the system into current limit. There might be undesirable consequences such as inductor saturation, overloading of the input or even a catastrophic failure of the device. It is recommended that the PWM controller be disabled when AOZ5036QI is disabled or non operational because of UVLO. The PWM controller should always be enabled with a soft start to minimise stresses on the converter.

In general it should be noted that AOZ5036QI is a combination of two MOSFETs with an unintelligent driver, all of which are optimized for switching at the highest efficiency. Other than UVLO and thermal protection, it does not have any monitoring or protection functions built in. The PWM controller should be designed in to perform these functions under all possible operating and transient conditions.

Input Voltage VIN

AOZ5036QI is rated to operate over a wide input range of 4.5V to 16V. As with any other synchronous buck converter, large pulse currents at high frequency and extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to bypass the input supply very close to package leads with X7R or X5R quality ceramic capacitors.

The high side MOSFET in AOZ5036QI is optimized for fast switching with low duty ratios. It has ultra low gate charges which have been achieved as a trade off with higher $R_{DS(ON)}$ value. When the module is operated at low VIN the duty ratio will be higher and conduction losses in the HS FET will also be correspondingly higher. This will be compensated to some extent by reduced switching losses. The total power loss in the module may appear to be low even though in reality the HS MOSFET losses may be disproportionately high. Since the two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation, the HS FET may be much hotter than the LS FET. It is recommended that worst case junction temperature be measured and ensured to be within safe limits when the module is operated with high duty ratios.

PWM Input

AOZ5036QI is offered in two versions which can be interfaced with PWM logic compatible with either 5V (TTL) or 3V (CMOS). Refer to Figure 13 for the timing and propagation delays between the PWM input and the gate drives. The PWM is also a tri state compatible input. When the input is high impedance or unconnected both the gate drives will be off and the gates are held active low. The PWM Threshold Table (Table 1) lists the thresholds for high and low level transitions as well as tri state operation. As shown in Figure 13, there is a hold off delay between the time PWM signal enters the tri state window and the corresponding gate drive is pulled low. This delay is typically 170ns and intended to prevent spurious triggering of the tri state mode which may be caused either by noise induced glitches in the PWM waveform or slow rise and fall times.

Table 1. PWM Input and Tri State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5036QI	3.9V	1.0V	1.3V	3.7V
AOZ5036QI-01	2V	1V	1.3V	1.75V

Note: See Figure 13 for propagation delays and tri state window.

Diode Mode Emulation of Low Side MOSFET (SMOD)

AOZ5036QI can be operated in the diode emulation or skip mode using the SMOD pin. This is useful if the converter has to operate in asynchronous mode during start up, light load or under pre bias conditions. If SMOD is taken high, the controller will use the PWM signal as reference and generate both the high and low side complementary gate drive outputs with the minimal delays necessary to avoid cross conduction. When the pin is taken low the HS FET drive is not affected but diode emulation mode is activated for the LS FET. See Table 2 for a comprehensive view of all logic inputs and corresponding drive conditions.

Table 2. Control Logic Truth Table

DISB#	SMOD	PWM	GH	GL
L	X	X	L	L
H	L	H	H	L
H	L	L	L	See Note
H	H	Tri State	L	L
H	H	H	H	L
H	H	L	L	H

Note: Diode emulation mode is activated when SMOD pin is held low.

Gate Drives

AOZ5036QI has an internal high current high speed driver that generates the floating gate drive for the HS FET and a complementary drive for the LS FET. Propagation delays between transitions of the PWM waveform and corresponding gate drives are kept to the minimum. An internal shoot through protection scheme ensures that neither MOSFET turns on while the other one is still conducting, thereby preventing shoot through condition of the input current. When the PWM signal makes a transition from H → L or L → H, the corresponding gate drive GH or GL begins to turn off. The adaptive timing circuit monitors the falling edge of the gate voltage and when the level goes below 1V, the complementary gate driver is turned on. The dead time between the two switches is minimized, at the same time preventing cross conduction across the input bus. The adaptive circuit also monitors the switching node VSWH and ensures that transition from one MOSFET to another always takes place without cross conduction, even under transient and abnormal conditions of operation.

The gate pins GH and GL are brought out on pins 6 and 36 respectively. However these connections are not made directly to MOSFET gate pads and their voltage measurement may not reflect the actual gate voltage applied inside the package. The gate connections are primarily for functional tests during manufacturing and no connections should be made to them in the application.

Thermal Shutdown

The module temperature is internally sensed and an alarm is asserted if it exceeds 150°C. The alarm is reset when the temperature cools down to 135°C. The THDN is an open drain pin that is pulled to CGND to indicate an overtemperature condition. It may be pulled up to VCIN through a resistor for monitoring purposes.

PCB Layout Guidelines

AOZ5036 is a high current module rated for operation up to 1MHz. This requires extremely fast switching speeds to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package helps to minimise the driver-to-MOSFET gate pad connections without involving the parasitics of the package or PCB traces. While excellent switching speeds are achieved, correspondingly high levels of dv/dt and di/dt will be observed throughout the power train which requires careful attention to PCB layout to minimise voltage spikes and other transients. As with any synchronous buck converter layout the critical requirement is to minimise the area of the primary switching current loop, formed by the HS FET, LS FET and the input bypass capacitor C_{in}. The PCB design is somewhat simplified because of the optimized pin out in AOZ5036QI. The bulk of VIN and PGND pins are located adjacent to each other and the input bypass capacitors should be placed as close as possible to these pins. The area of the secondary switching loop, formed by LS FET, output inductor and output capacitor C_{out} is the next critical parameter. The ground plane should be extended and the negative pins of C_{out} should be returned to it, again as close as possible to the device pins.

While AOZ5036QI is extremely efficient it can still dissipate up to 6W of heat which requires attention to thermal design. MOSFETs in the package are directly attached to individual exposed pads to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal reliefs should be avoided to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the 12V system input, is desirable and vias should be provided near the device to connect the VIN

copper pour to the power plane. Though ground does not form a part of any device tabs, significant amount of heat is dissipated though multiple PGND pins. A large copper pour connected to PGND pins and further to the system ground plane through vias will further improve thermal management of the system.

Figure 15 illustrates the various copper pours and bypass capacitor locations.

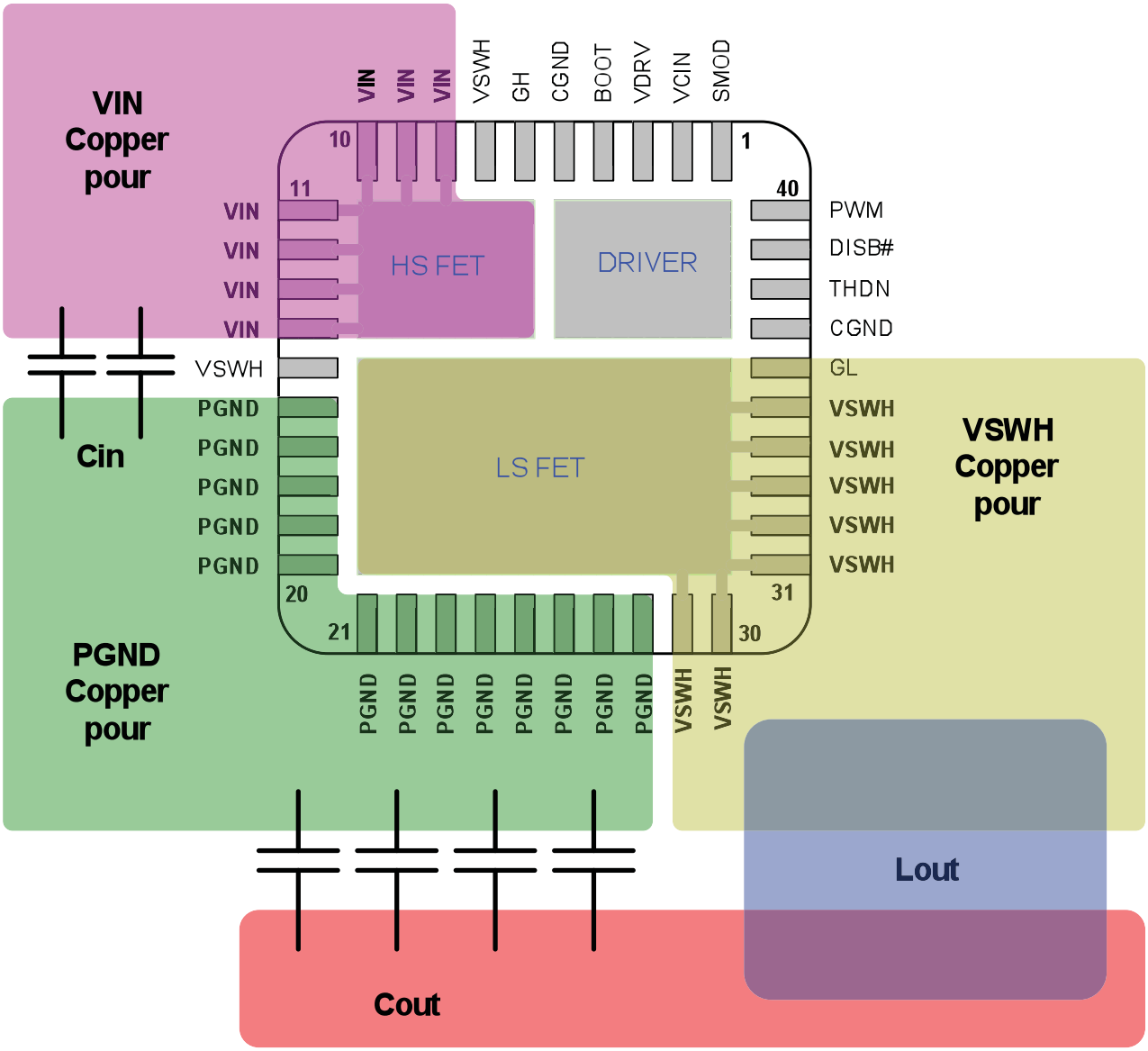
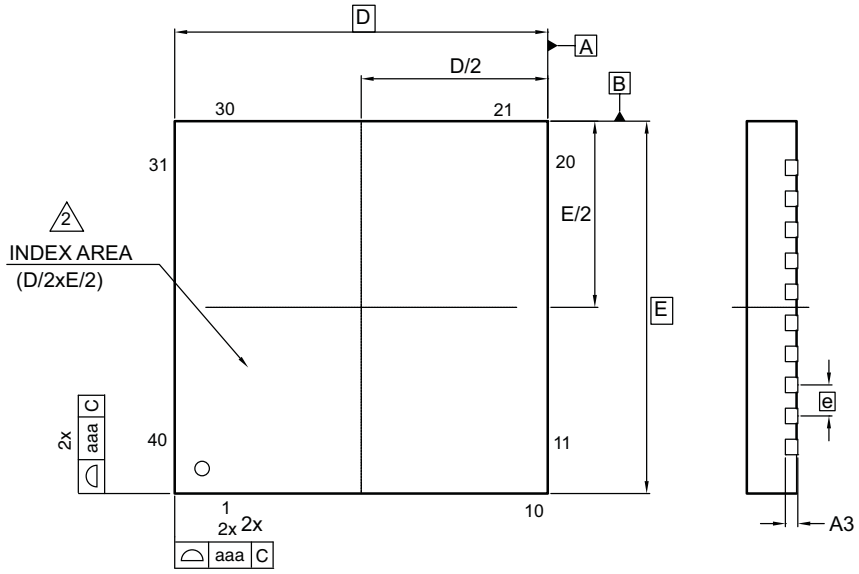
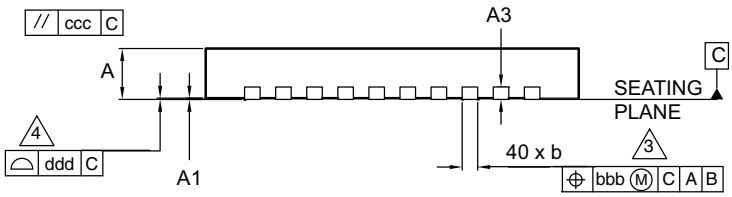


Figure 15. PCB Layout Illustration for Minimizing Current Loops

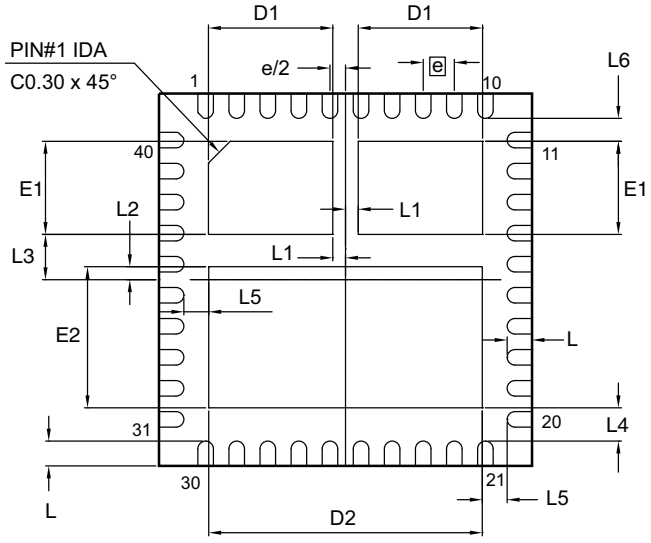
Package Dimensions, 6x6 QFN-40 EP3_S



TOP VIEW



SIDE VIEW

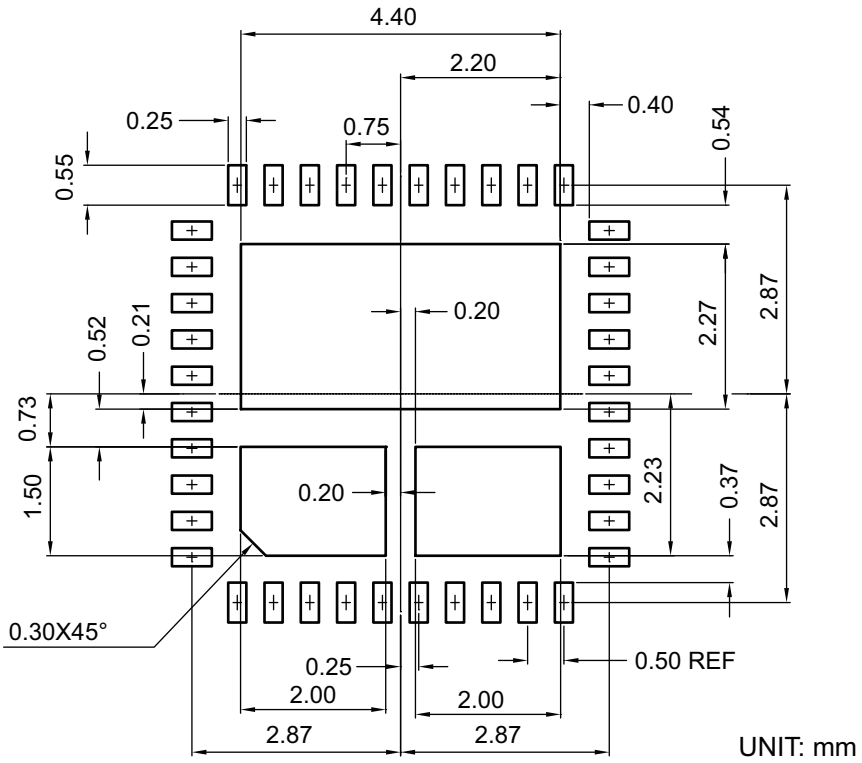


BOTTOM VIEW

Notes:

1. All dimensions are in millimeters.
2. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.
3. Dimension b applies to metallized terminal and is measured between 0.20mm and 0.35mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
4. Coplanarity applies to the terminals and all other bottom surface metalization.

Package Dimensions, 6x6 QFN-40 EP3_S (Continued)



RECOMMENDED LAND PATTERN

Dimensions in millimeters

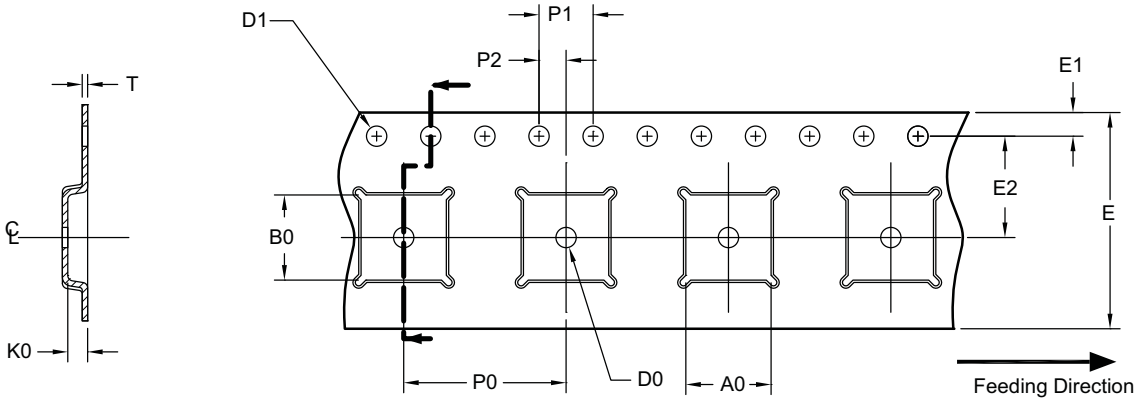
Symbols	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.35
D		6.00 BSC	
D1	1.90	2.00	2.10
D2	4.30	4.40	4.50
E		6.00 BSC	
E1	1.40	1.50	1.60
E2	2.17	2.27	2.37
e		0.50 BSC	
L	0.30	0.40	0.50
L1	0.15	0.20	0.25
L2	0.15	0.21	0.26
L3	0.63	0.73	0.83
L4	0.44	0.54	0.64
L5	0.30	0.40	0.50
L6	0.27	0.37	0.47
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.08	

Dimensions in inches

Symbols	Min.	Typ.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.008	0.010	0.014
D		0.236 BSC	
D1	0.075	0.079	0.083
D2	0.169	0.173	0.177
E		0.236 BSC	
E1	0.055	0.059	0.063
E2	0.085	0.089	0.093
e		0.020 BSC	
L	0.012	0.016	0.020
L1	0.006	0.008	0.010
L2	0.006	0.008	0.010
L3	0.024	0.028	0.032
L4	0.017	0.021	0.025
L5	0.012	0.016	0.020
L6	0.011	0.015	0.019
aaa		0.006	
bbb		0.004	
ccc		0.004	
ddd		0.003	

Tape and Reel Dimensions, 6x6 QFN

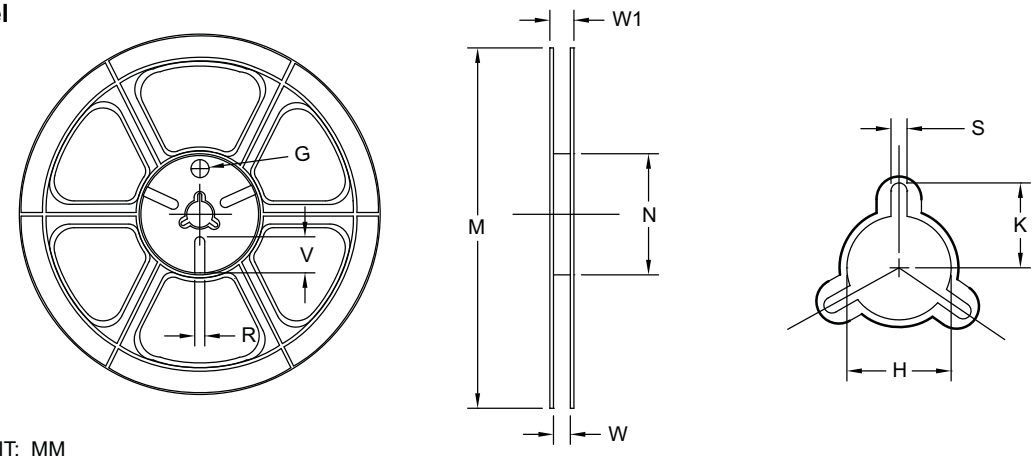
Carrier Tape



UNIT: MM

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN6x6 (16mm)	6.30 ±0.20	6.30 ±0.20	1.10 ±0.20	1.50 MIN.	1.50 +0.1 -0.0	16.0 ±0.3	1.75 ±0.10	7.5 ±0.1	12.00 ±0.20	4.00 ±0.20	2.00 ±0.10	0.30 ±0.05

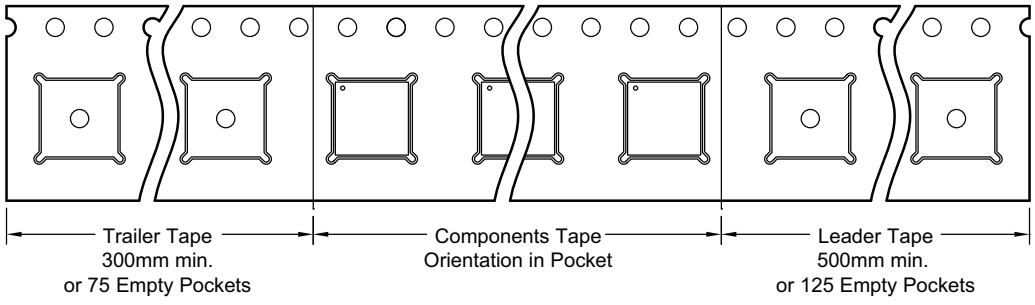
Reel



UNIT: MM

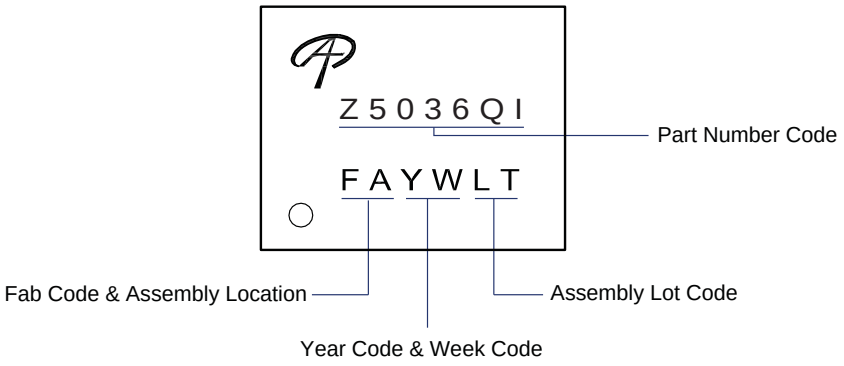
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
16mm	Ø330	Ø330 Max.	Ø100 Min.	16.4 +2.0 -0.0	22.4 Max.	Ø13.0 +0.5 -0.2	10.1 Min.	1.5 Min.	---	---	---

Leader/Trailer and Orientation



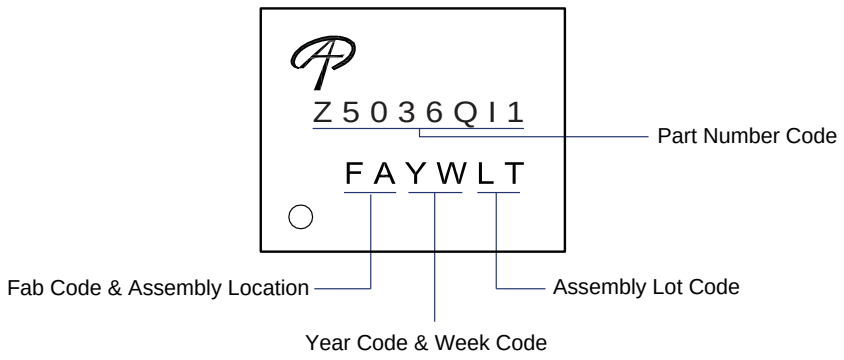
Part Marking

AOZ5036QI*
(6.0 x 6.0 QFN)



** Contact factory for availability*

AOZ5036QI-01
(6.0 x 6.0 QFN)



ALPHA & OMEGA SEMICONDUCTOR

Document No.	PO-00099
Version	B

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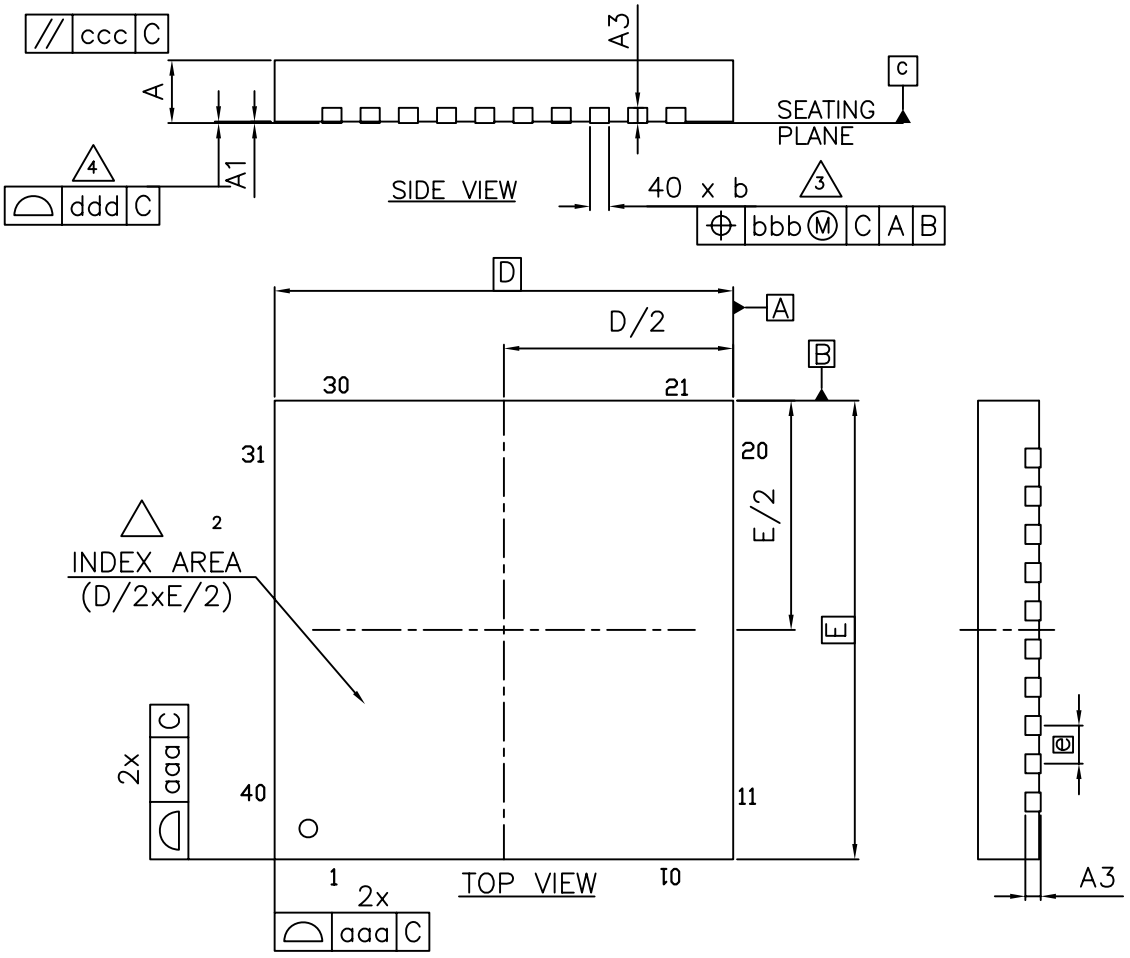
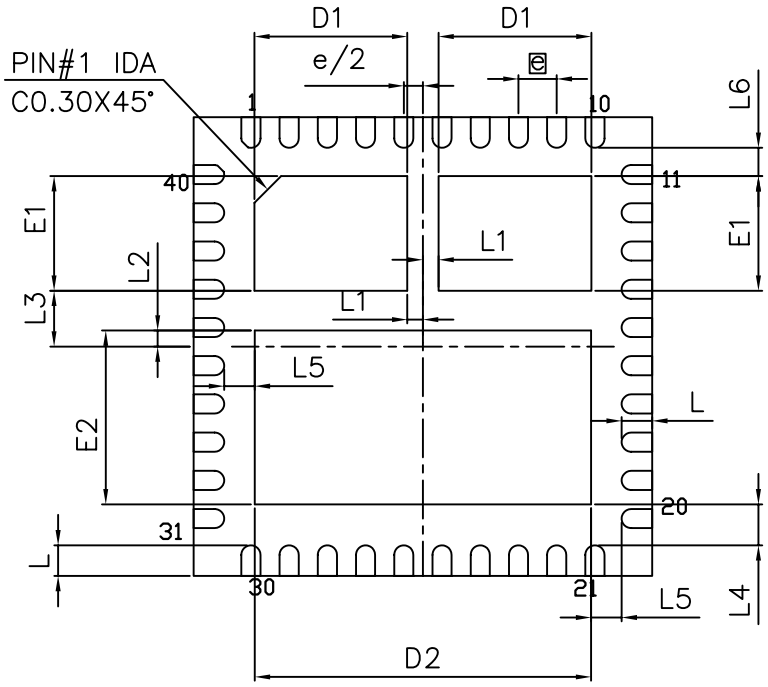
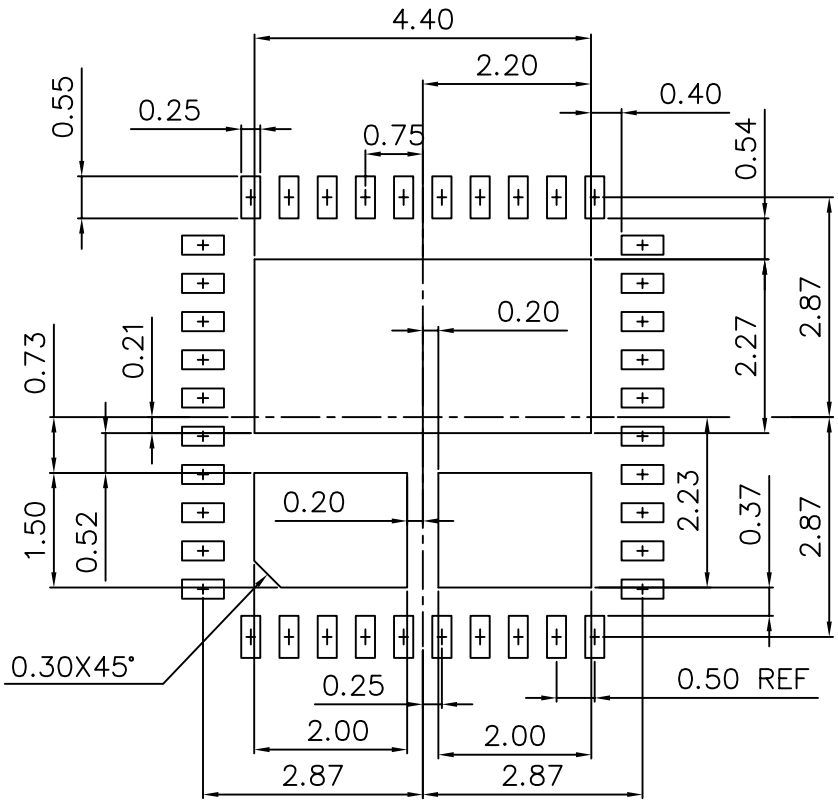




BOTTOM VIEW

QFN6x6_40L_EP3_S PACKAGE OUTLINE

RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.20	0.25	0.35	0.008	0.010	0.014
D	6.00 BSC			0.236 BSC		
D1	1.90	2.00	2.10	0.075	0.079	0.083
D2	4.30	4.40	4.50	0.169	0.173	0.177
E	6.00 BSC			0.236 BSC		
E1	1.40	1.50	1.60	0.055	0.059	0.063
E2	2.17	2.27	2.37	0.085	0.089	0.093
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.15	0.20	0.25	0.006	0.008	0.010
L2	0.15	0.21	0.26	0.006	0.008	0.010
L3	0.63	0.73	0.83	0.024	0.028	0.032
L4	0.44	0.54	0.64	0.017	0.021	0.025
L5	0.30	0.40	0.50	0.012	0.016	0.020
L6	0.27	0.37	0.47	0.011	0.015	0.019
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.08			0.003		

Note:

1. All dimensions are in millimeters.

2. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.

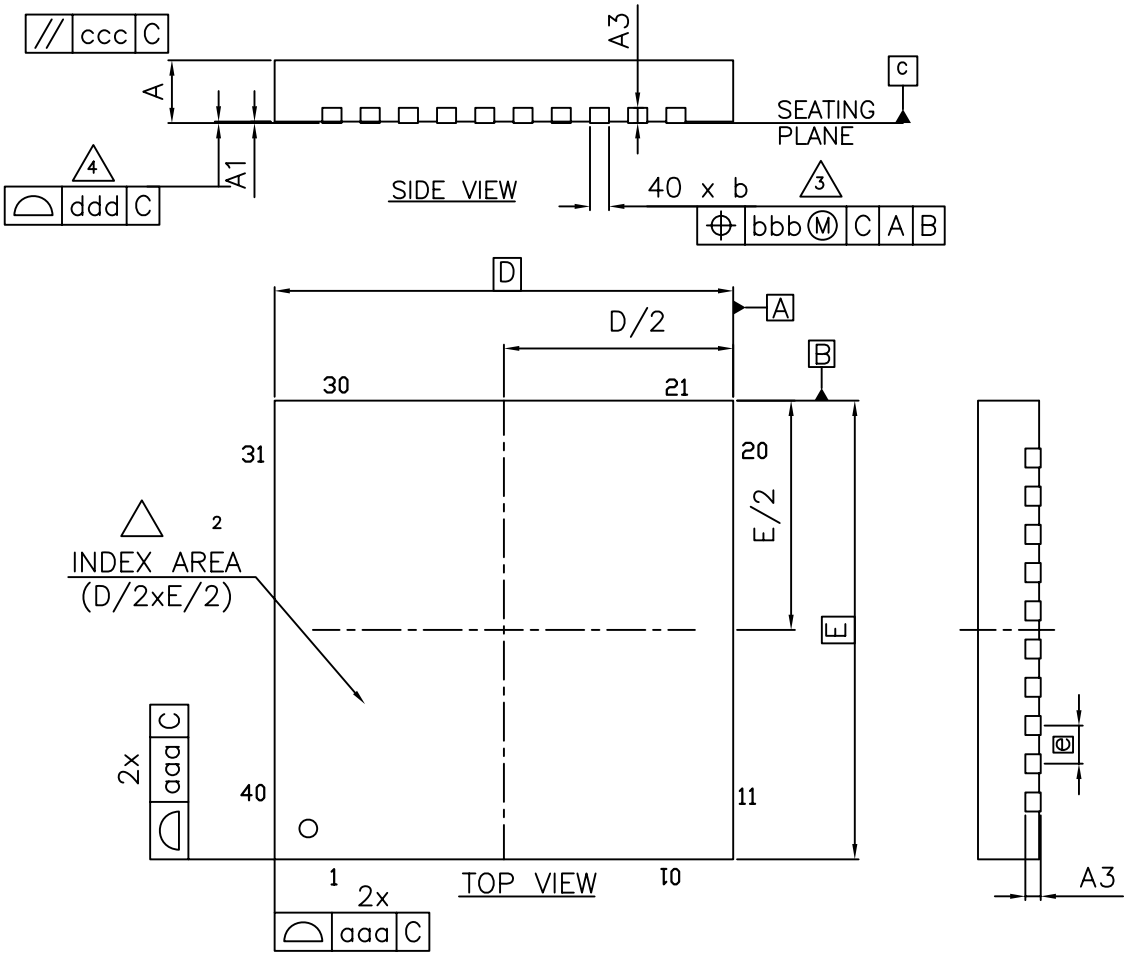
3. Dimension b applies to metallized terminal and is measured between 0.20mm and 0.35mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.

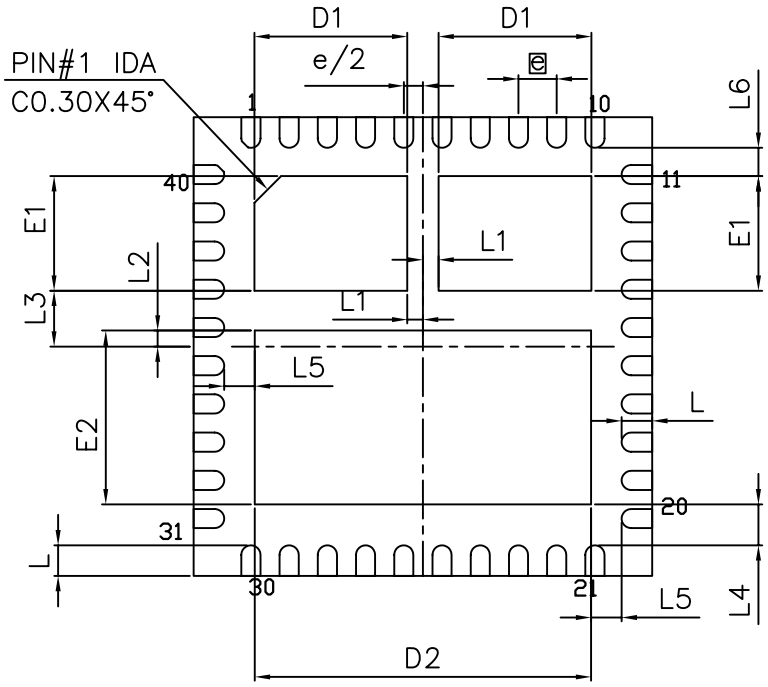
4. Coplanarity applies to the terminals and all other bottom surface metallization.

ALPHA & OMEGA SEMICONDUCTOR

Document No.	PO-00099
Version	B

QFN6x6_40L_EP3_S PACKAGE OUTLINE

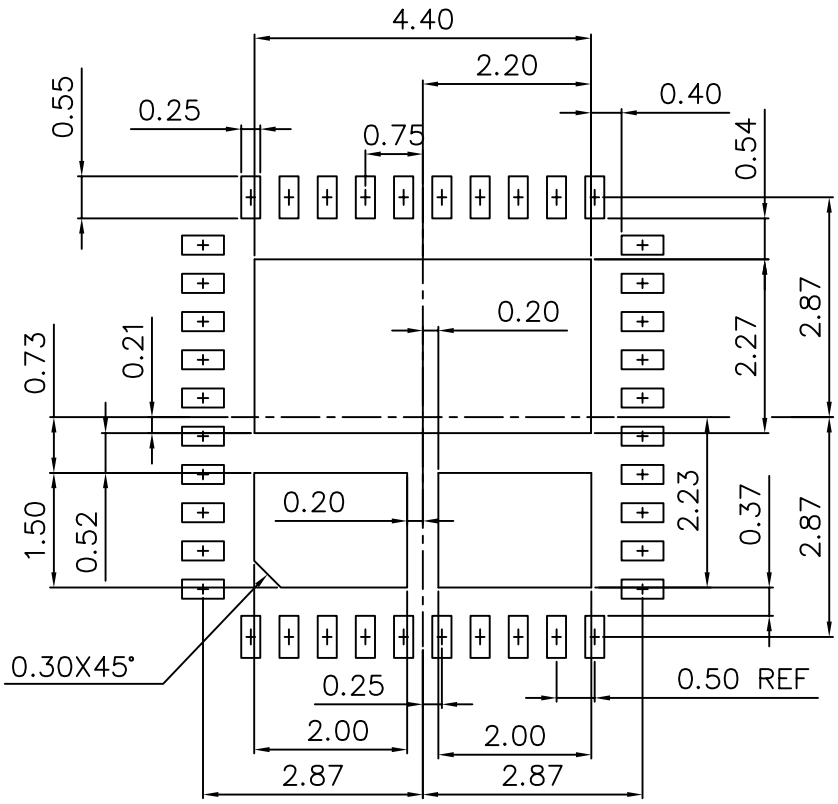




BOTTOM VIEW

QFN6x6_40L_EP3_S PACKAGE OUTLINE

RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
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A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.20	0.25	0.35	0.008	0.010	0.014
D	6.00 BSC			0.236 BSC		
D1	1.90	2.00	2.10	0.075	0.079	0.083
D2	4.30	4.40	4.50	0.169	0.173	0.177
E	6.00 BSC			0.236 BSC		
E1	1.40	1.50	1.60	0.055	0.059	0.063
E2	2.17	2.27	2.37	0.085	0.089	0.093
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.15	0.20	0.25	0.006	0.008	0.010
L2	0.15	0.21	0.26	0.006	0.008	0.010
L3	0.63	0.73	0.83	0.024	0.028	0.032
L4	0.44	0.54	0.64	0.017	0.021	0.025
L5	0.30	0.40	0.50	0.012	0.016	0.020
L6	0.27	0.37	0.47	0.011	0.015	0.019
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.08			0.003		

Note:

1. All dimensions are in millimeters.

2. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.

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4. Coplanarity applies to the terminals and all other bottom surface metallization.

ALPHA & OMEGA SEMICONDUCTOR

PAC-005

Recommended Temperature Profile For Soldering AOS Product With Lead Free Solder

For AOS internal reliability precondition profile see Appendix A

TITLE: Soldering Temperature Profile of AOS Product with Lead free solder

1 PURPOSE

This document defines the recommendation of soldering temperature profiles for all the Alpha & Omega Semiconductor (AOS) products. Using temperature and time duration not to exceed these conditions will prevent damage to the parts during the mounting processes, and also help to ensure the quality and reliability of AOS parts.

2 SCOPE

This procedure is applicable to all of AOS product/packages that are required to perform soldering on to PCB (Printed circuit board)

3 REFERENCE DOCUMENTS

JESD22-A113，Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

IPC/JEDEC J-STD-020D ， Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

4 GENERAL

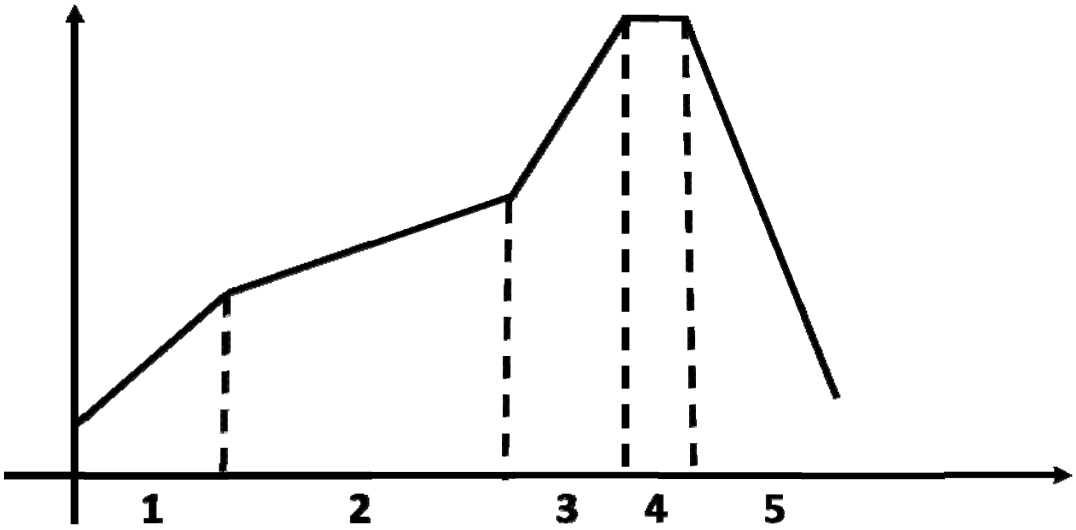
Soldering profile is used in PCB assembly. Since different system, different components and different solder are used by different customer, the optimum soldering condition to insure the solder integrity and reliability can only be determined by user (customer).

The recommended soldering profiles reflect the common range used by PCB assembly process which has less thermal stresses than our reliability qualification precondition. This will insure the long term reliability of usage of AOS parts.

During the reliability qualification, AOS parts are subject to very severe condition in accordance with the IPC/JEDEC J-STD-20D document (see profile in Appendix A), which involves one week moisture absorption in 85 ºC and 85% relative humidity follow by three solder reflows simulation for >=30 sec at peak temperature between 255 ºC and 260 ºC. By using temperature and time duration not to exceed these recommended conditions will be obviously not damage AOS parts.

5 Recommended Soldering Profile

5.1 Reflow Soldering Profile:



Profile Feature	Requirement
1. Ramp up	1-4 ºC/second
2. Soak	150 ºC~200 ºC 60-180 seconds
3. Ramp up to peak	1-4ºC/second
4. Peak soak *	245~260 ºC 10 seconds max
5. Ramp-down Rate	1~6 ºC/second max.

* Maximum thermal excursion allowed during the reflow assembly is as follow:

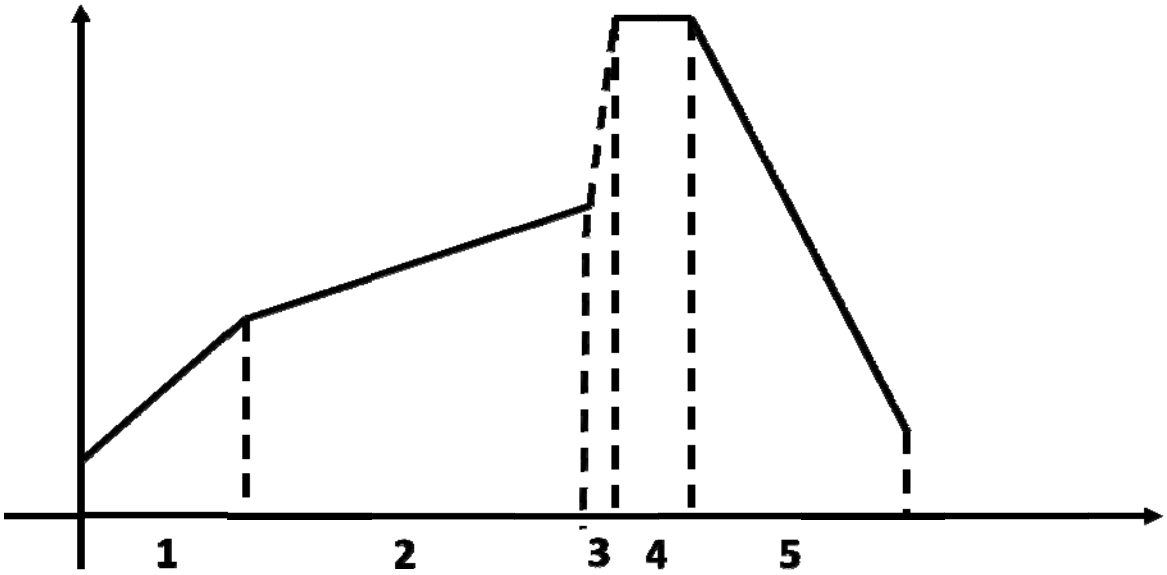
Temperature: 255 ºC ~ 260 ºC

Duration at peak soak: 30 sec

Number of reflow: 3

5.2 Wave Soldering Profile:

5.2.1 Profile



Profile Feature	**Recommended Condition**
1. Preheat - Ramp up rate	 1-7 ºC/second
2. Soak - Temprature: - Time:	 110ºC ramp to 140ºC 60-120 seconds
3.Ramp up -Ramp up rate	 ~150 ºC/sec
4. Peak - Peak package body temperature - Time	 245 ºC to 260 ºC 10 seconds max. For dual wave also
5. Ramp down: - Ramp down rate:	 1-7 ºC/second

5.2.2 Leadless Device Assembled on the back side of PCB

By and large wave soldering is for through hole device assemble. Leadless device is not recommended to be assemble on the backside of the PCB, however if customer has needs to do so, care needs to be exercised. Then the thermal stress from this wave solder profile is allowed.

If the device is to be attached by surface mount reflow first on the backside, then the special holding fixture needs to be used to prevent the device from falling into the wave soldering bath.

If the device is attached on the backside with adhesive it is customer's responsibility to insure that it will not dropped during the wave soldering process.

Device with heat sink on the backside, it is recommended that no more than 50% of the area will be blocked by adhesive. It is customer's responsibility to do the thermal and electrical characterization to insure the system integrity.

5.3Hand Soldering:

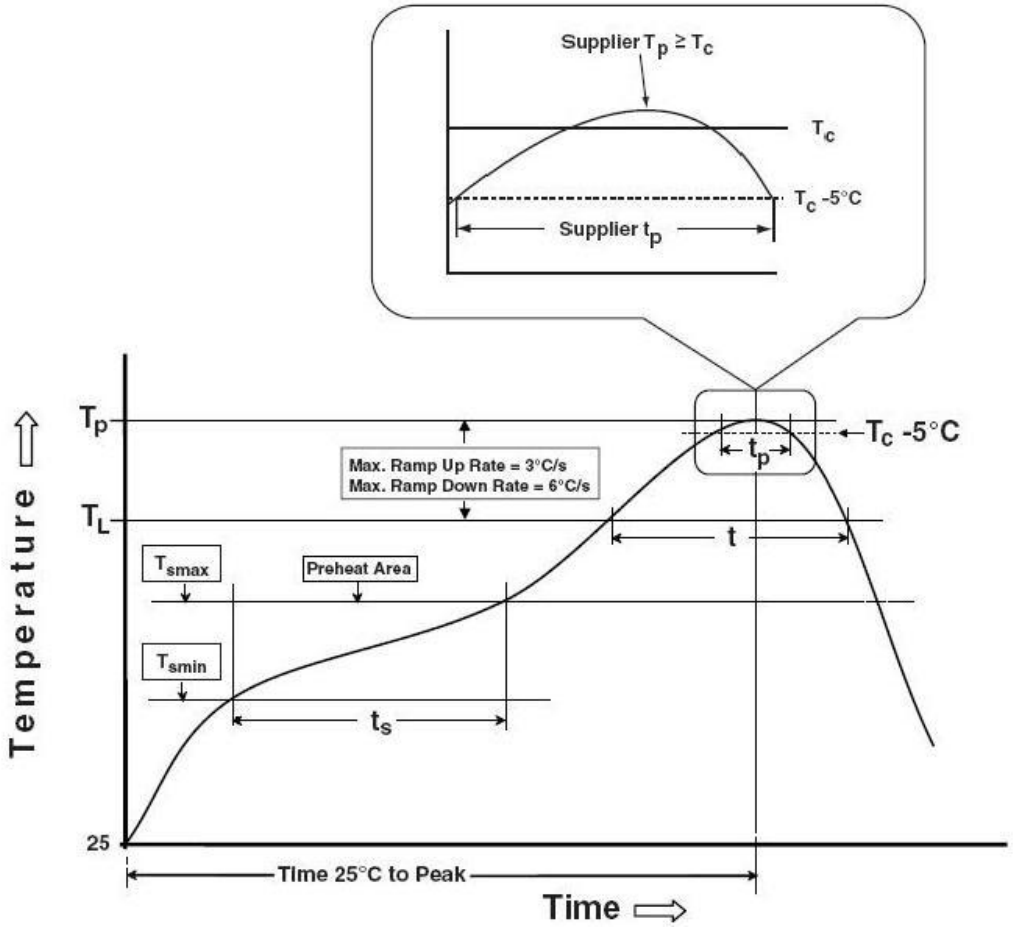
Not recommended for mass production, for engineering project or re-work it is allowed. It should be used with cautious.

Parameters	**Recommended Condition**
Tip Temperature	350 ±10 ºC
Time*	3 seconds

*Maximum duration is 5 seconds

Appendix A

AOS internal reflow profile for reliability test precondition is as follow:



Profile Feature	**Condition**
Preheat & Soak - Temperature Min ($T_{S(min)}$): - Temperature Max ($T_{S(min)}$): - Time (min to max)(ts):	 150 ºC 200 ºC 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 ºC/second max
Liquidous Temperature (T_L): Time (t_L):	217 ºC 60-150 seconds
Peak Package body Temperature(T_p)*: See IPC/JEDEC J-STD-020 for detail	Tp must equal to or exceed the Classification Temperature. Typically Tp = 260 ºC
Time t_p within 5ºC of specified classification temperature (T_C):	30 seconds min.
Ramp-down Rate (T_p to T_{smax}) :	6 ºC/second max.
Time 25 ºC to Peak Temp. :	8 minutes max