

PG611 C00

12GB GDDR5X, 384b, 256Mx32

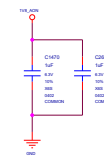
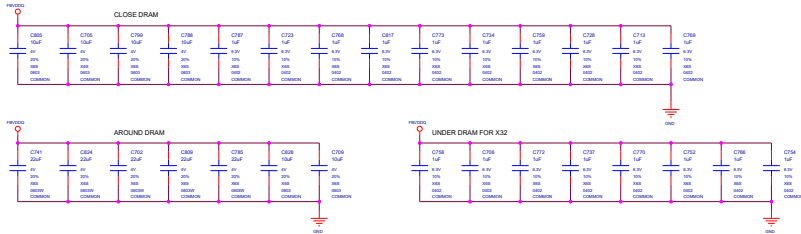
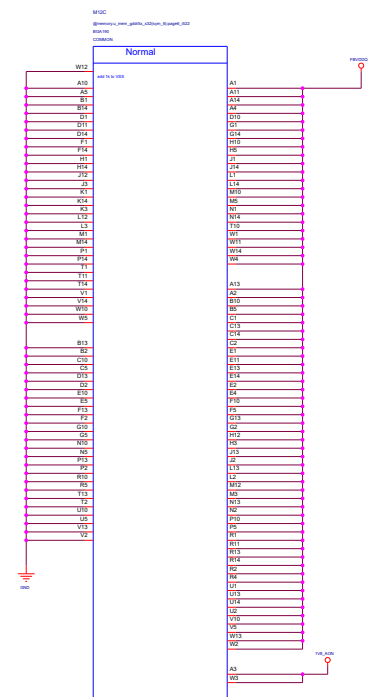
TALL DVI-D + DP + DP + HDMI/DP + DP

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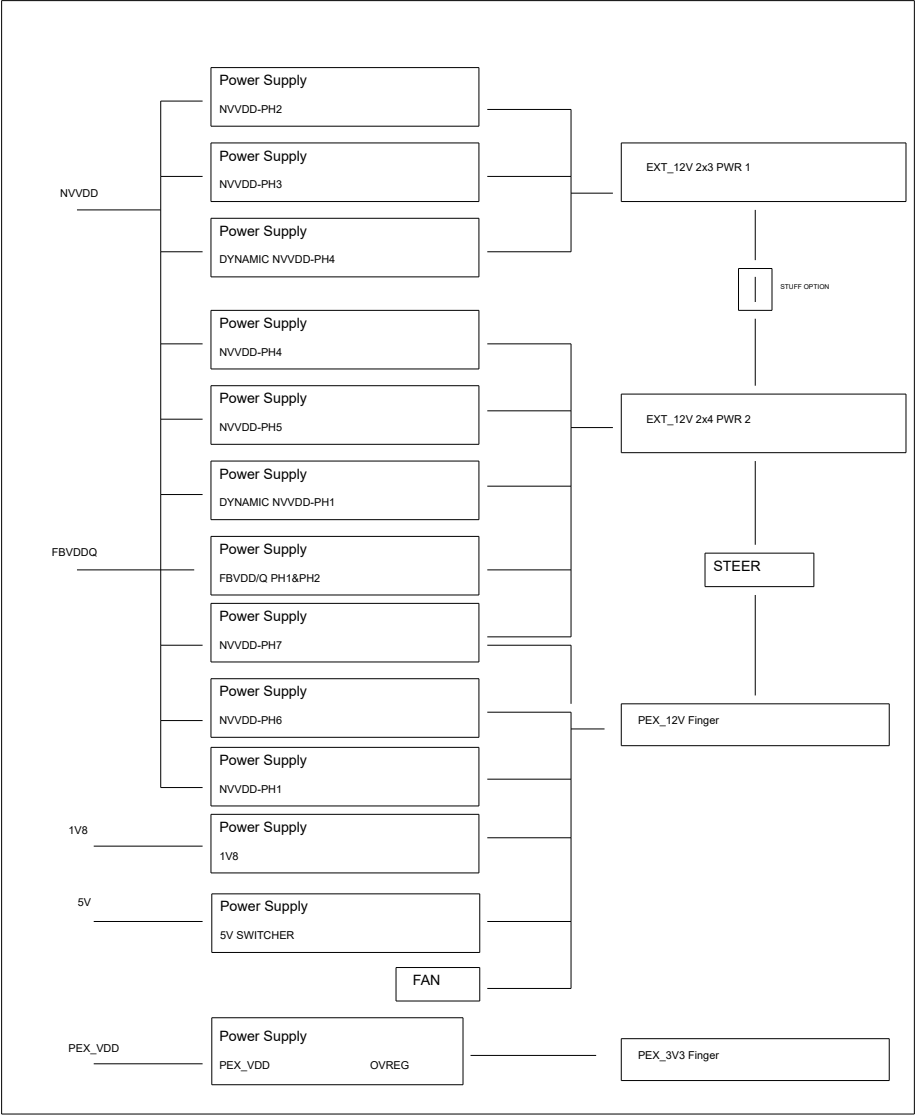
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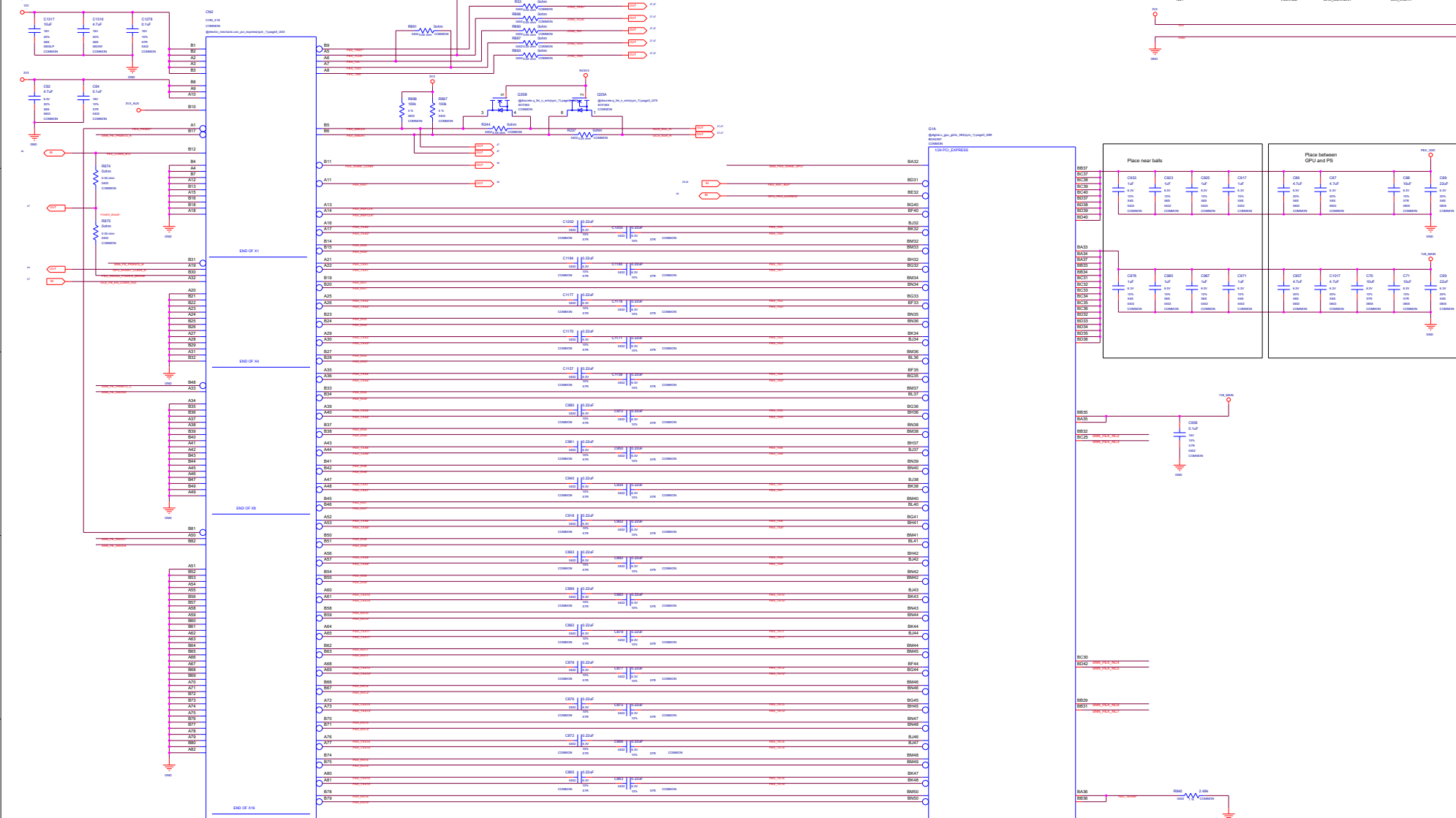
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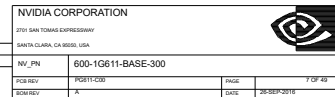


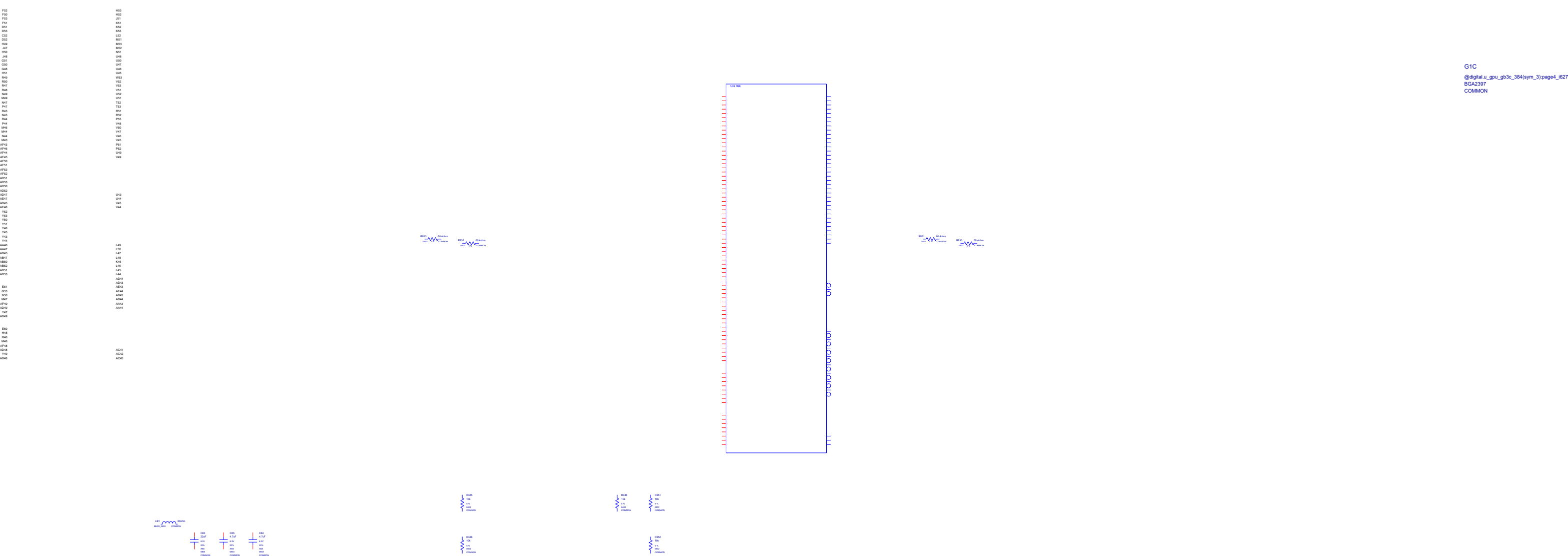
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PCB DESIGN	PCB DESIGN

NVIDIA CORPORATION			
3701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
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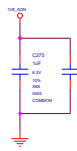


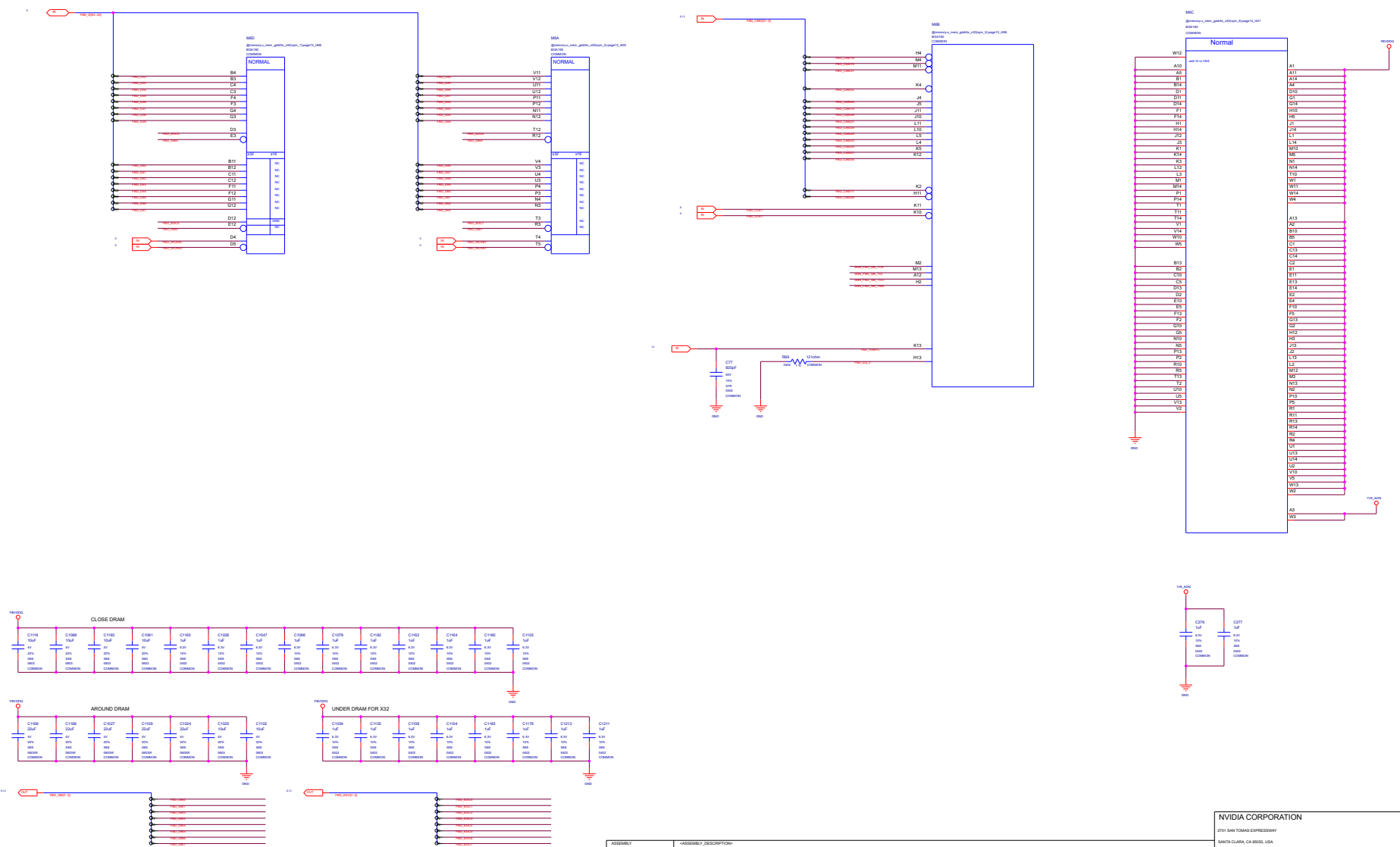
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BGA2397

COMMON

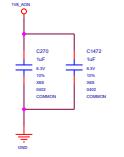
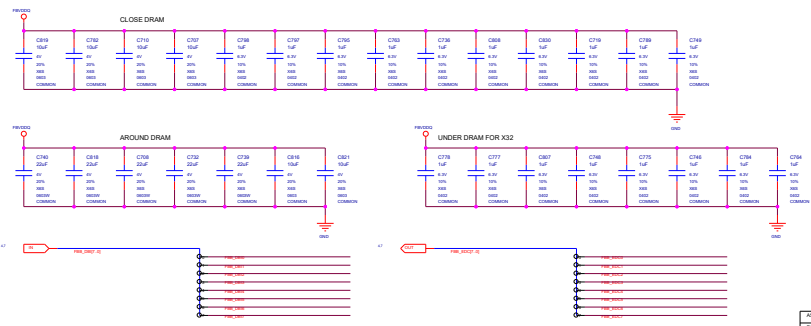
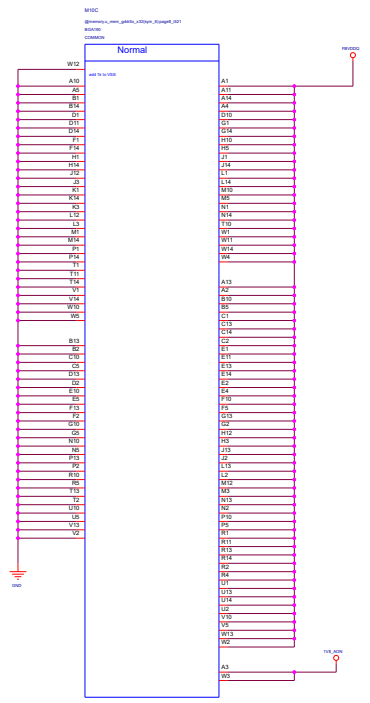
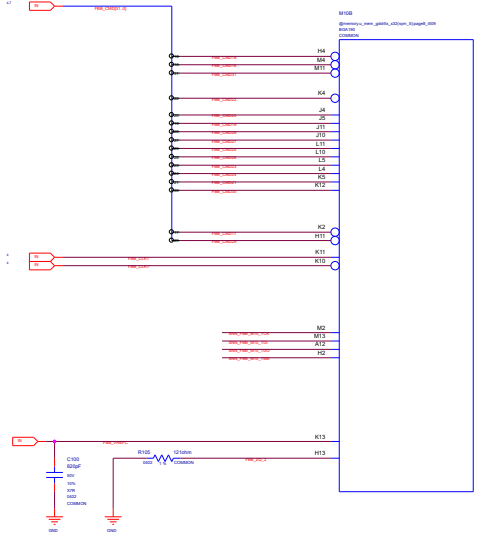
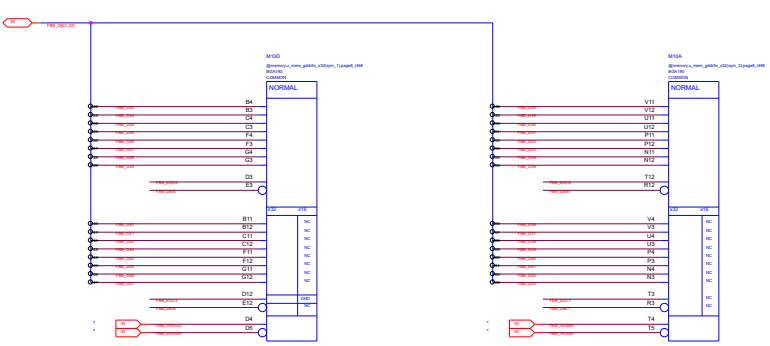




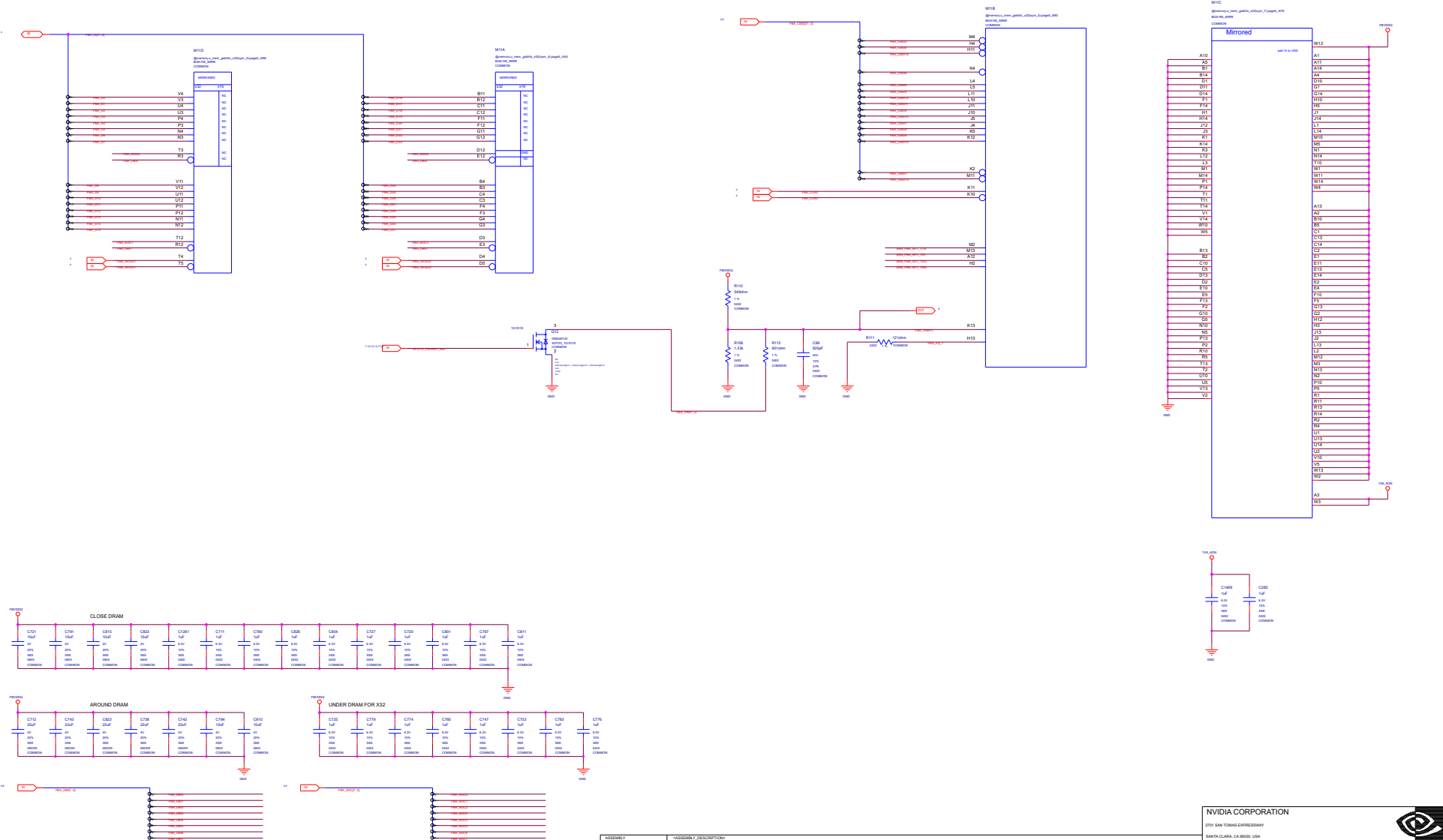




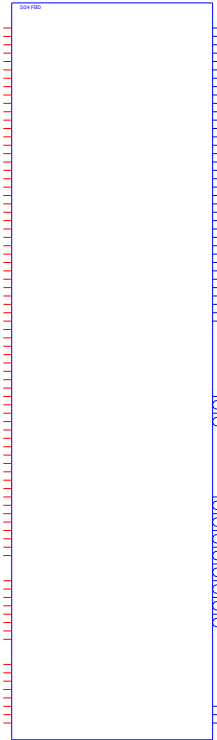
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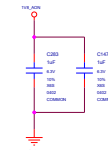
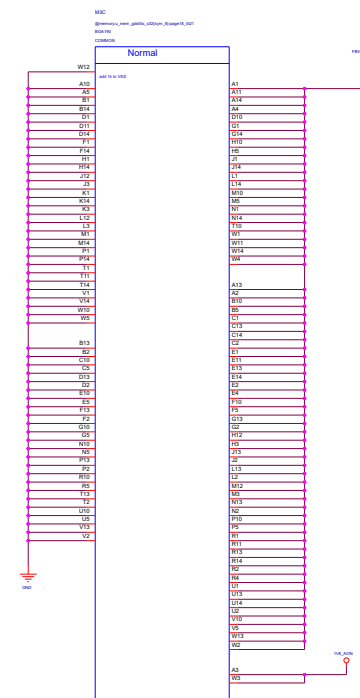
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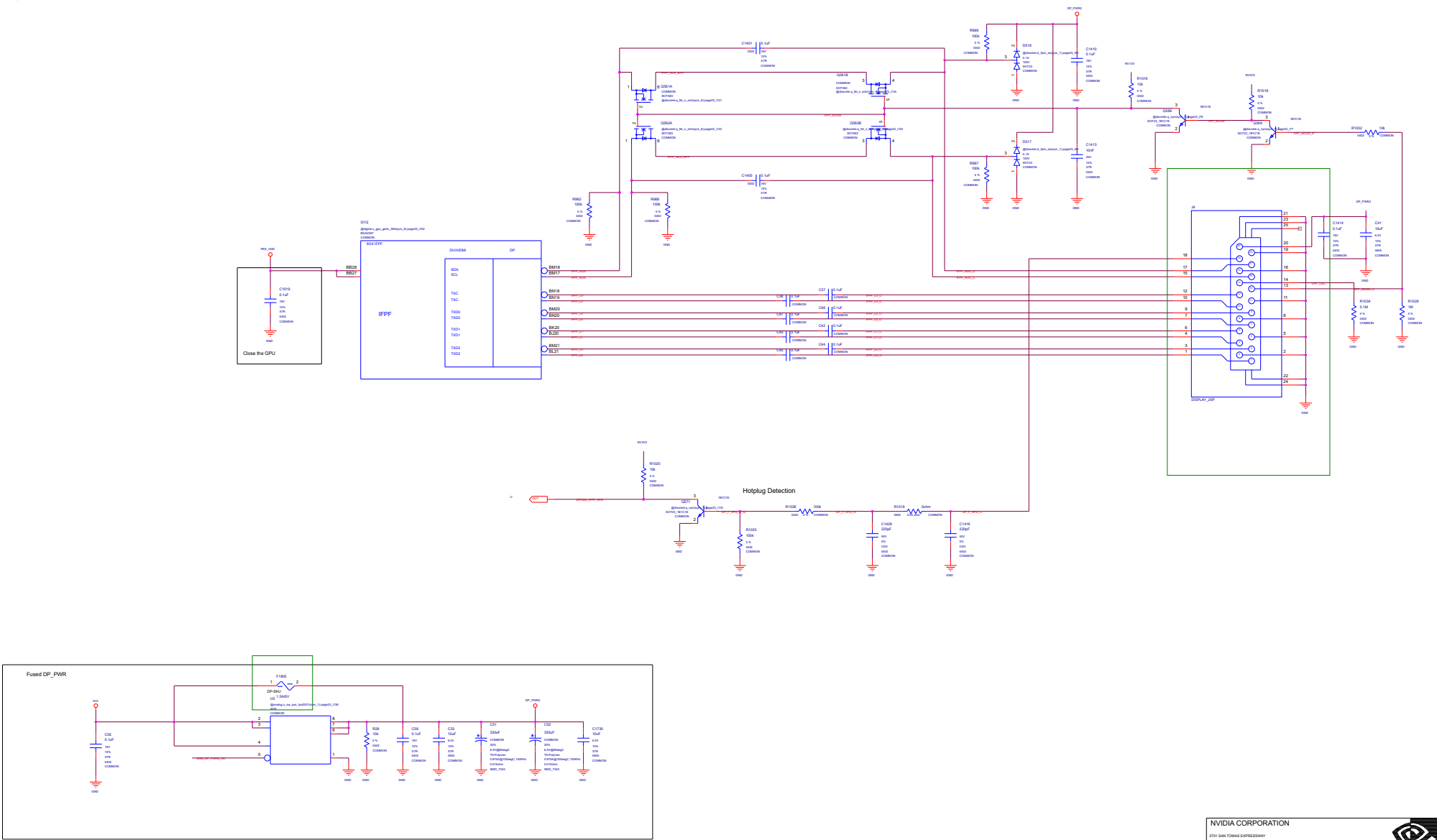
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BGA2397
COMMON





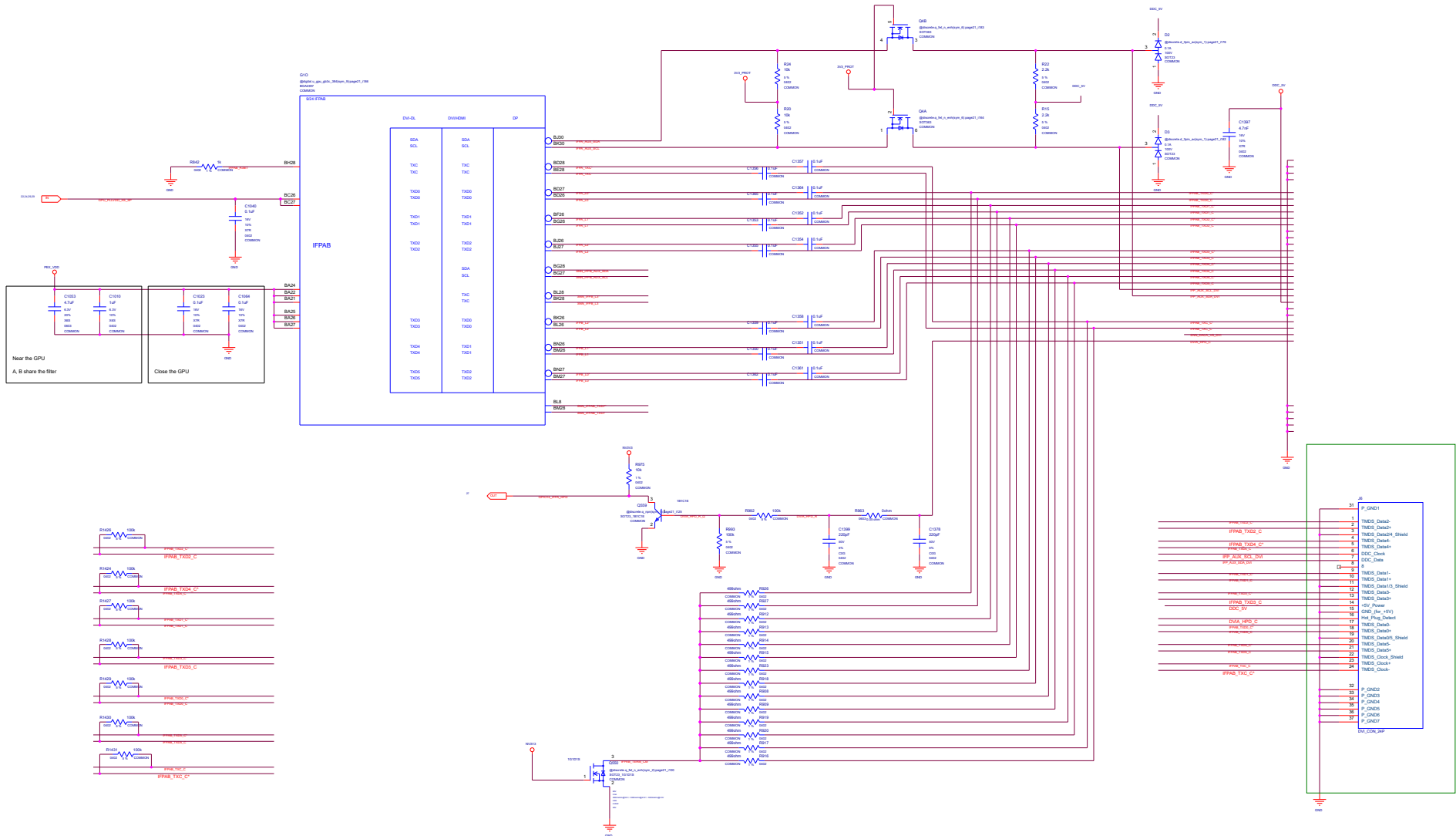




ASSEMBLY	ASSEMBLY DESCRIPTION
IFPF DP	IFPF DP

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-10611-BASE-300		
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ASSEMBLY	ASSEMBLY DESCRIPTION
FRAME SERIAL	MIOA/B INTERFACE & FRAME LOCK

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SAN JOSE, CALIFORNIA, CA 95134, USA

NV_P/N

600-10611-BASE-300

PCB REV

7081TCSW

BOARD REV


A

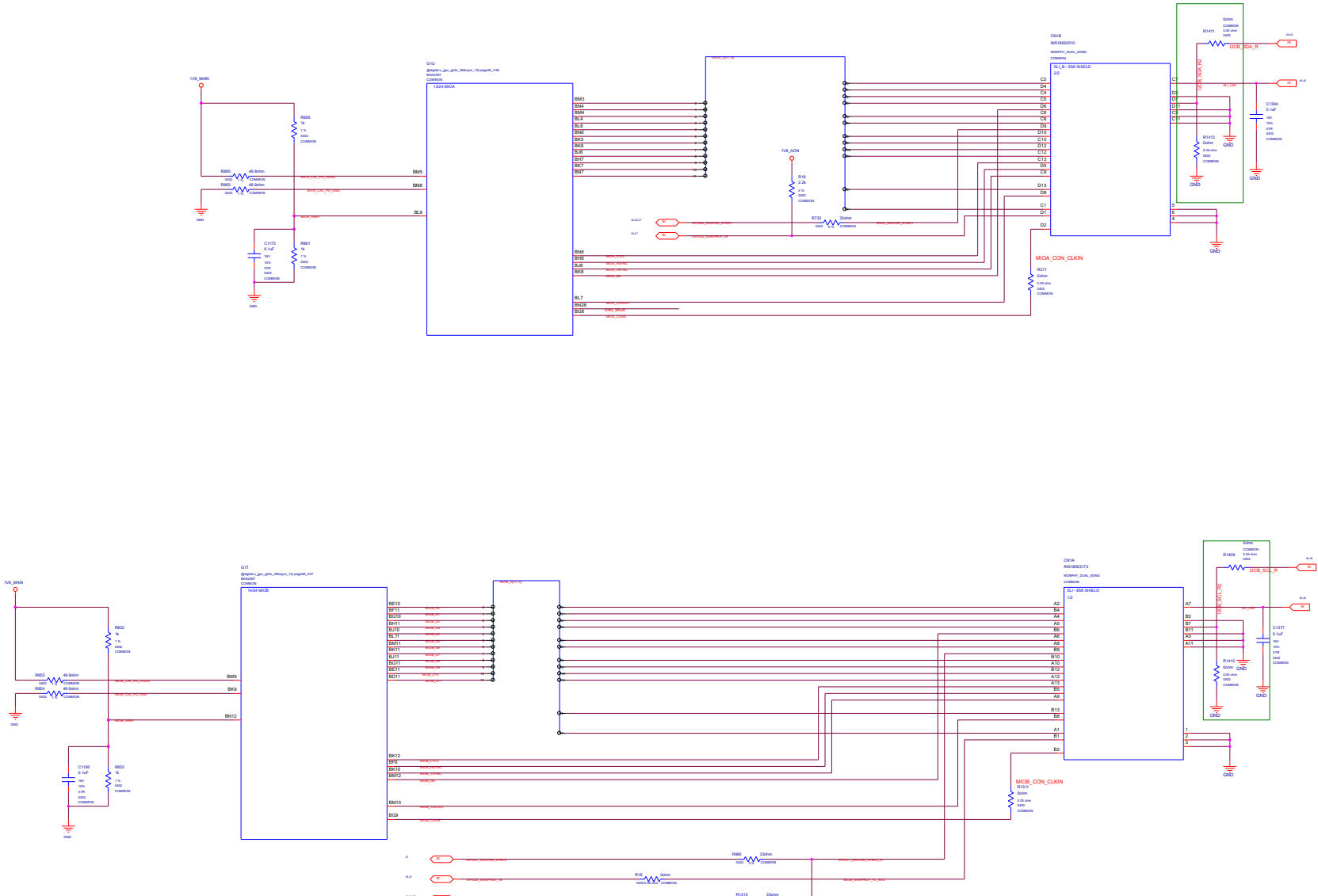
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DATE

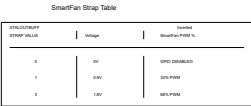
26 SEP 2016







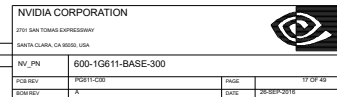
NVIDIA CORPORATION			
3701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-1G611-BASE-300		
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STRAP OUTPUT STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPO DISABLED
1	0.9V	33% PWM
3	1.8V	66% PWM



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STRAP2	STRAP1	STRAP0	RAMCFG(4:0)	
L	L	L	00000	
L	L	H	00001	
L	H	L	00010	MICRON 12Gbps REV.B
L	H	H	00011	
H	L	L	00100	
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED(3:0)	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

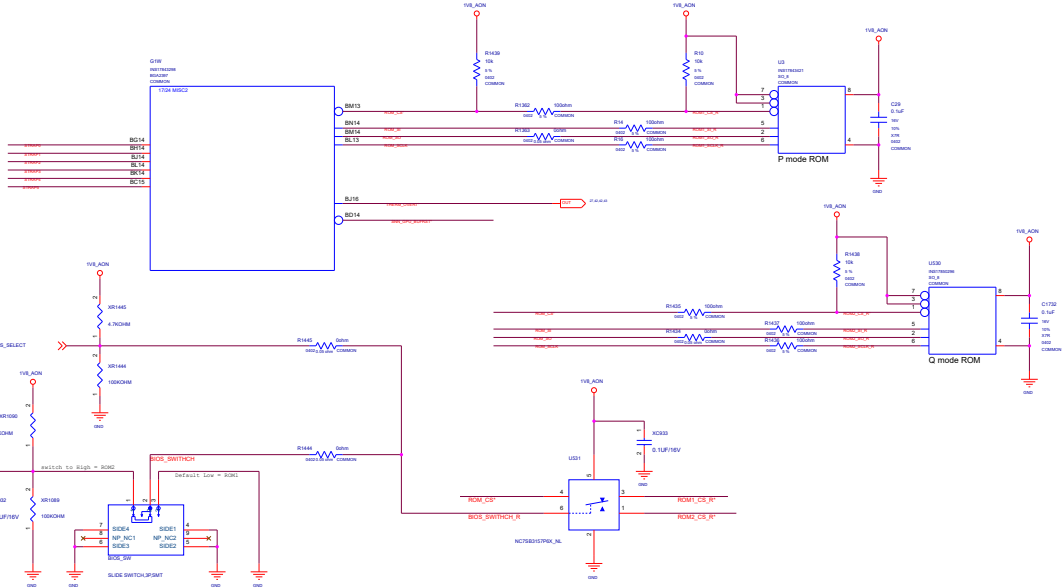
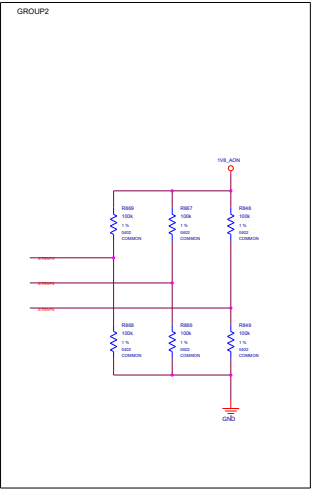
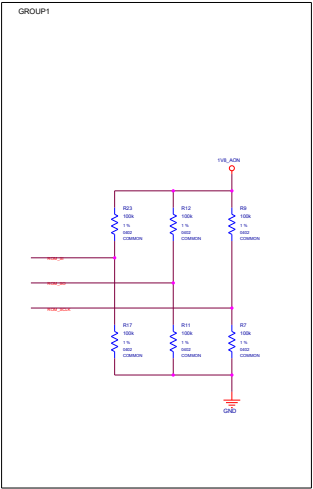
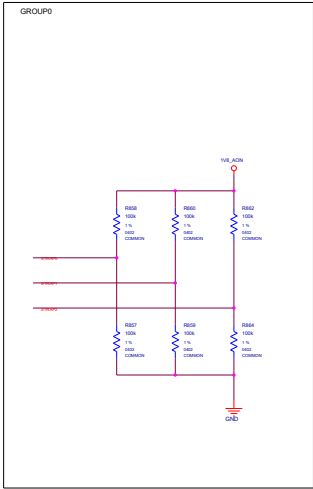
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

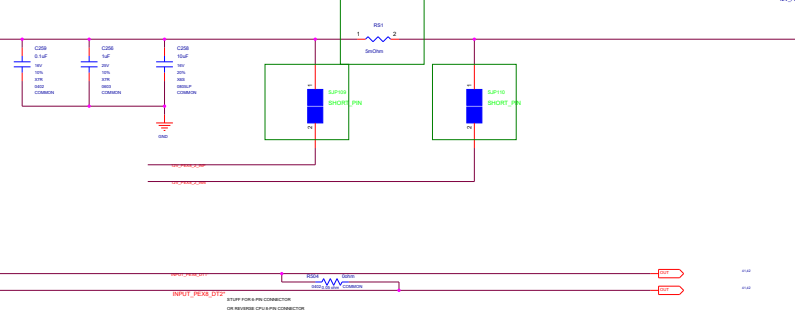
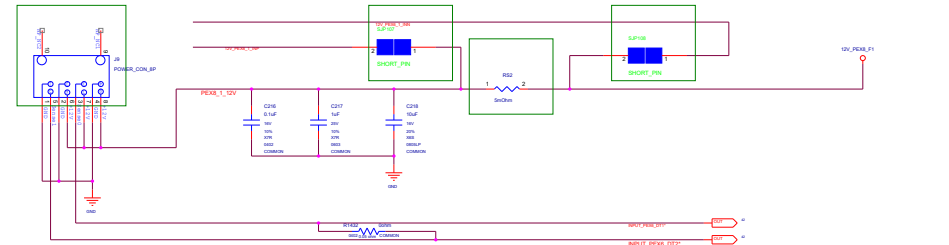
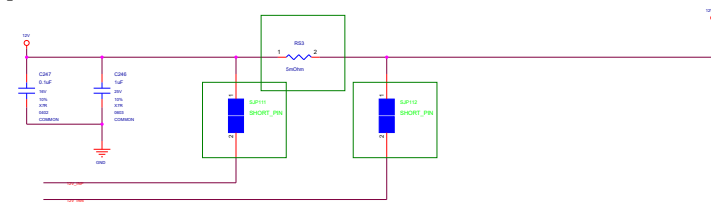
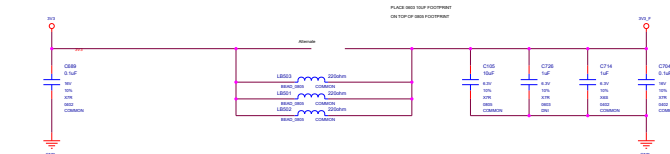
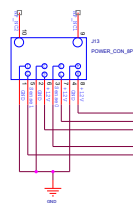
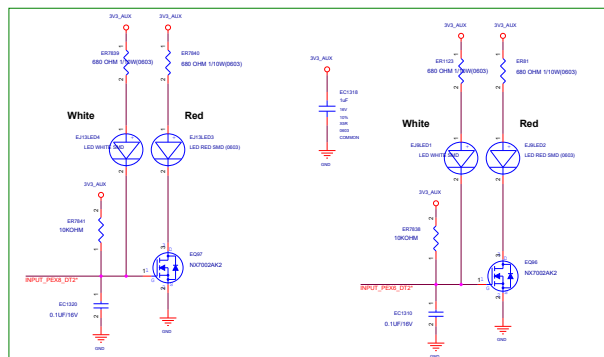
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





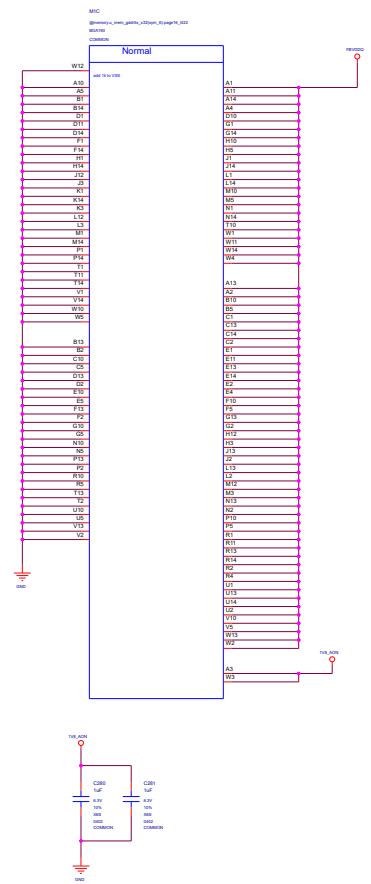
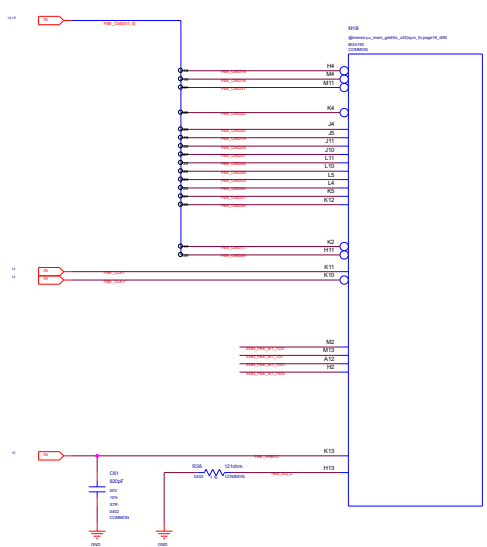
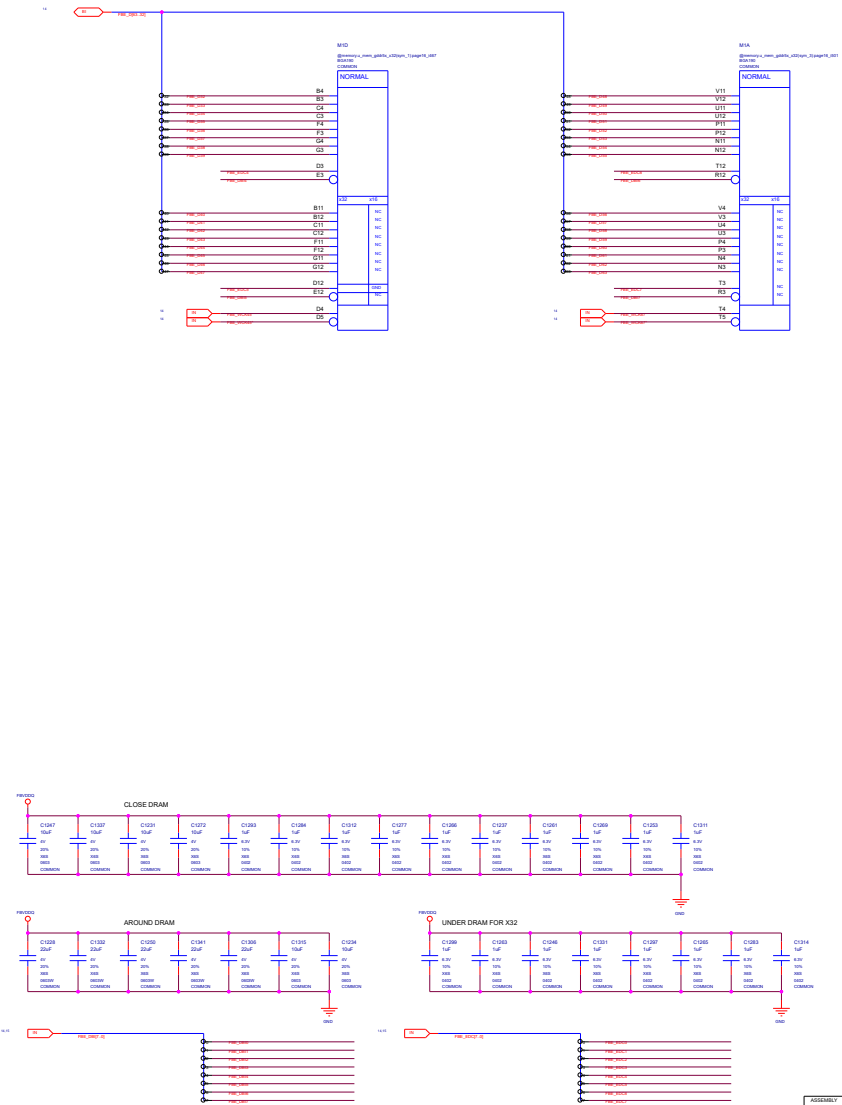
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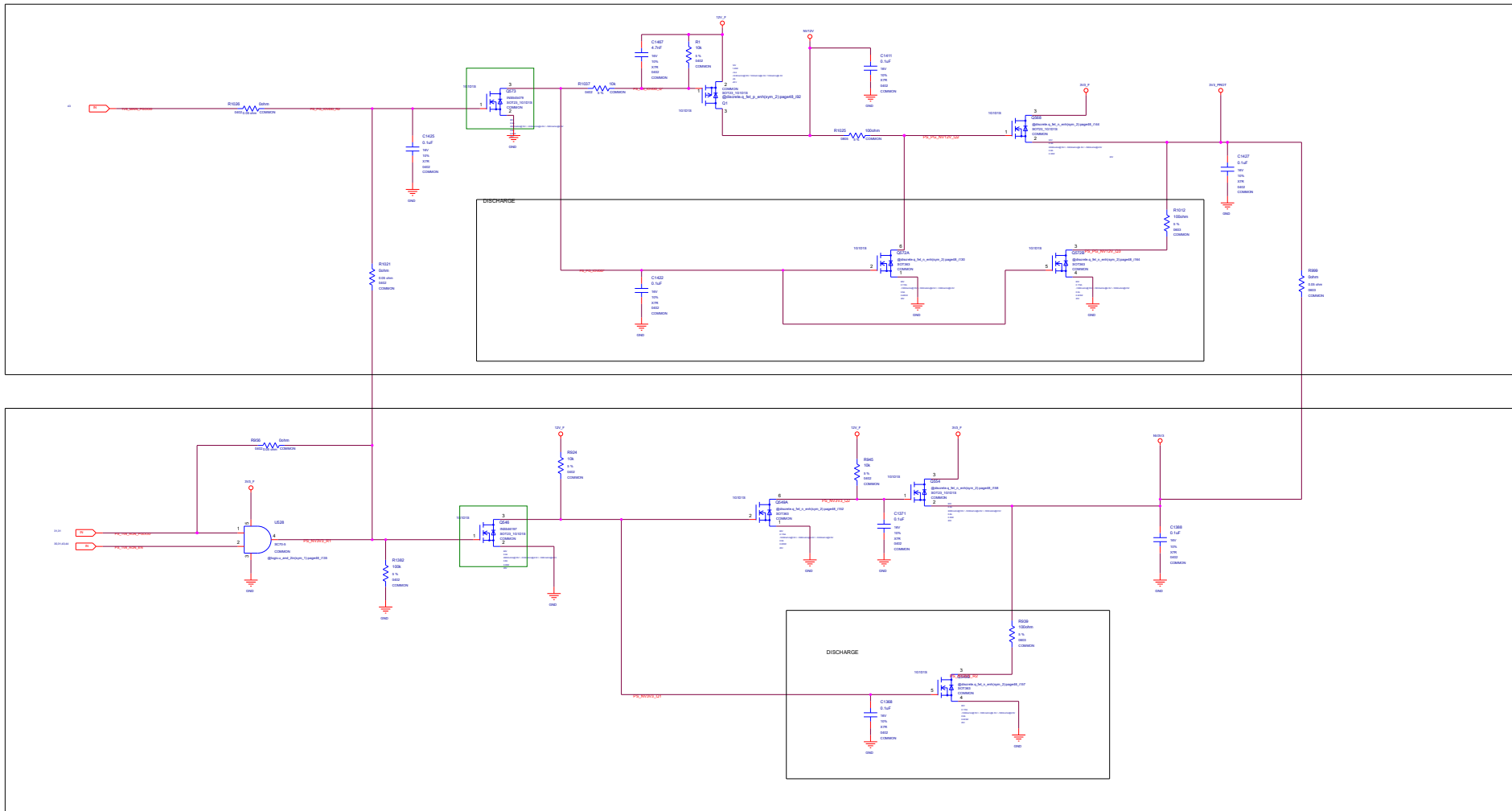
NV_PN	600-1G611-BASE-300		
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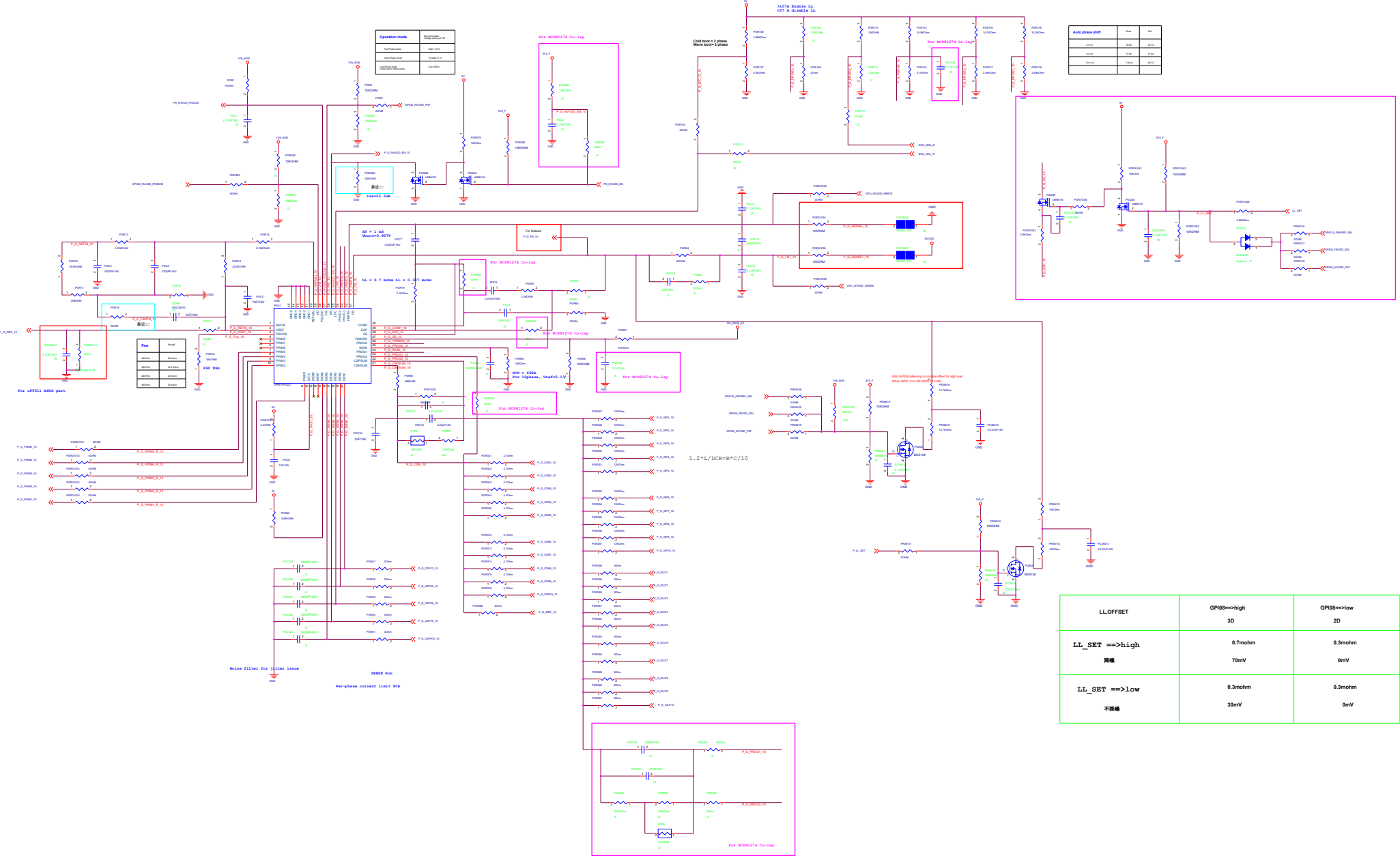
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB SERIAL	PCB NV3V3, NV12V

NVIDIA CORPORATION			
3701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95051, USA			
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BOARD REV	A		

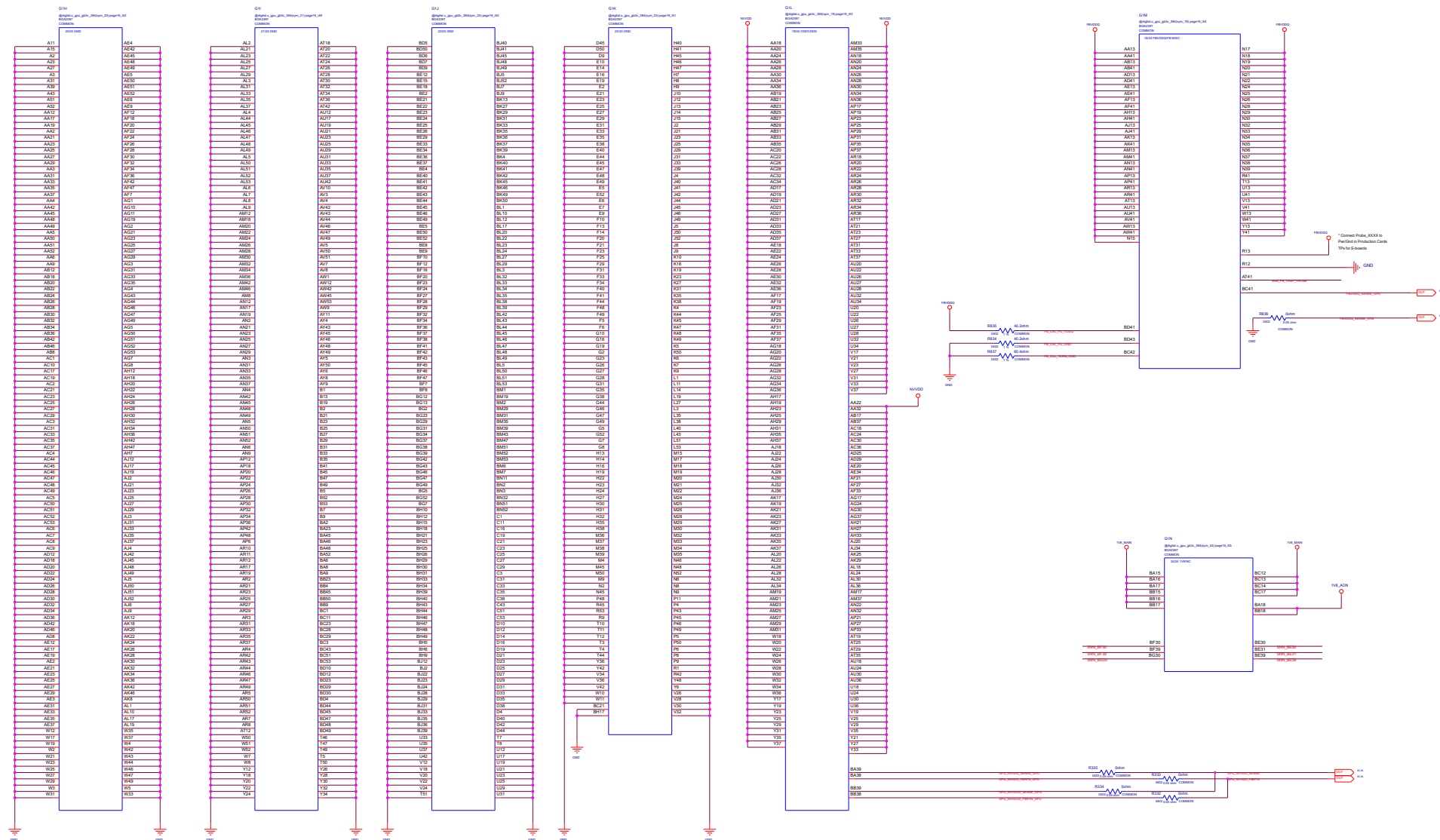


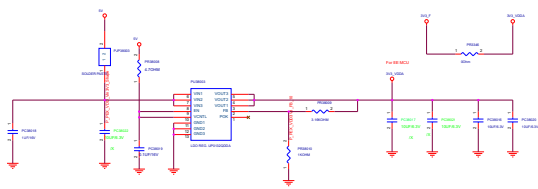


Operation mode	Motor driver
Auto phase shift	Auto phase shift
LL_SET ==>high	LL_SET ==>high
LL_SET ==>low	LL_SET ==>low

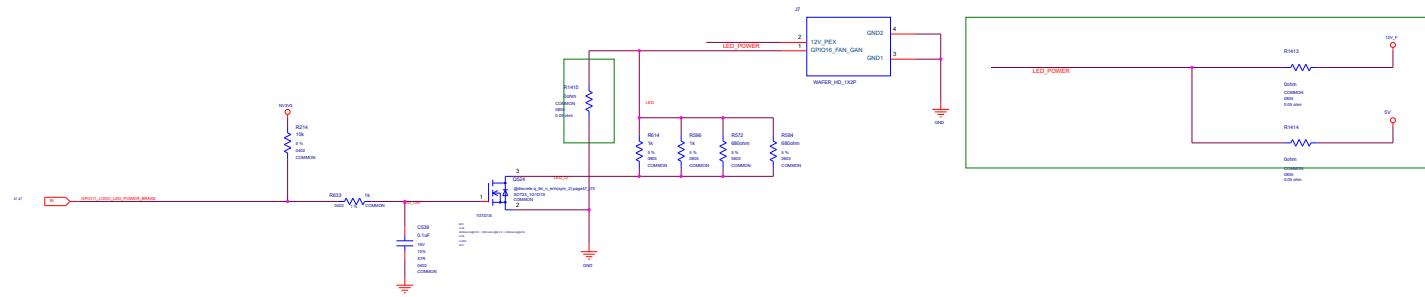
Auto phase shift	LL_SET ==>high	LL_SET ==>low
Auto phase shift	LL_SET ==>high	LL_SET ==>low
Auto phase shift	LL_SET ==>high	LL_SET ==>low
Auto phase shift	LL_SET ==>high	LL_SET ==>low

LLOFFSET	GPIO8==>high	GPIO8==>low
LL_OFFSET	GPIO8==>high	GPIO8==>low
LL_OFFSET	GPIO8==>high	GPIO8==>low
LL_OFFSET	GPIO8==>high	GPIO8==>low

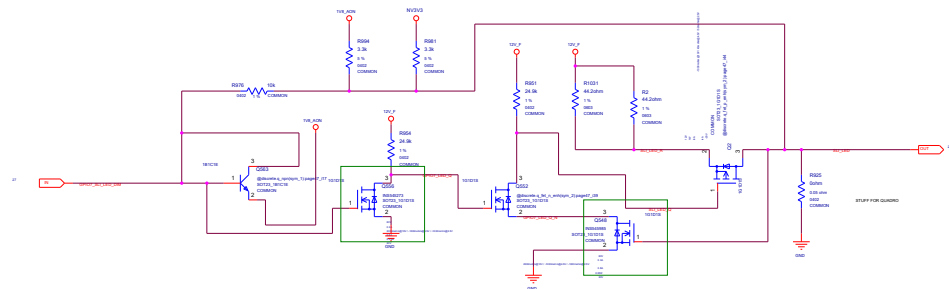




$$V_o = 0.8V(1 + R_{top}/R_{bot})$$
$$= 0.8V * (1 + 3.16K/1K) = 3.3V$$



SLI LED (GEFORCE ONLY)



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GEFORCE LEO AND SIL LEO

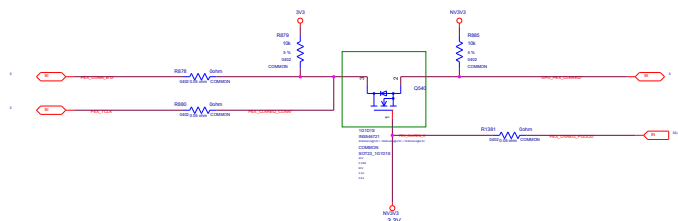
NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

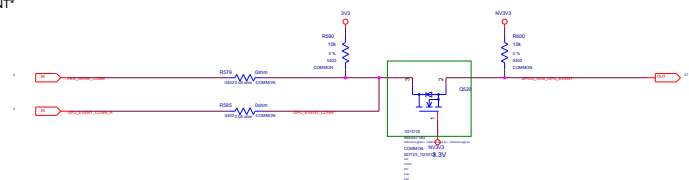


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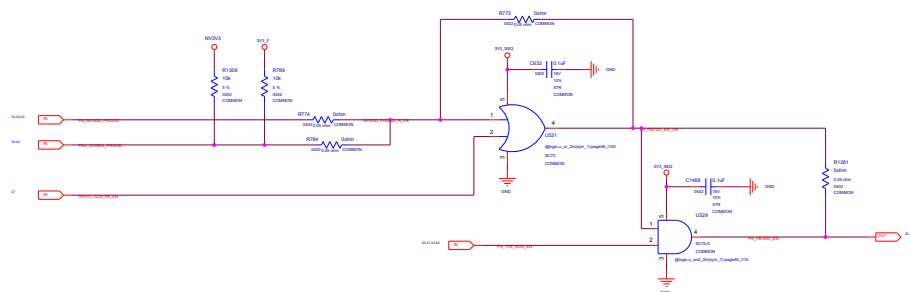
PEX CLKREQ#



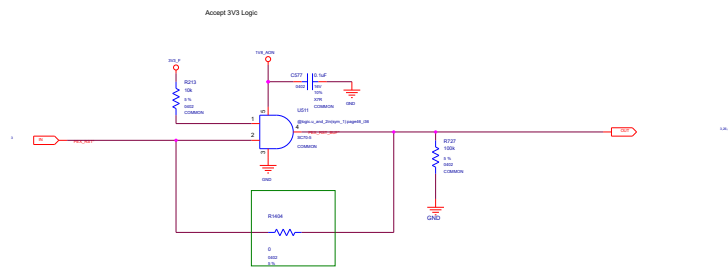
GPU EVENT*




FRVDD/Q FNARI F



PFX_RST# LOGIC



ASSEMBLY		ASSEMBLY DESCRIPTION		SANTA CLARA, CA 95050, USA	
PAGE DETAIL		PR: GCR MAG			
				NY_PN 600-10611-BASE-300	
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BOM: REV		A		DATE: 24-SEP-2016	

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SANTA CLARA, CA 95050, USA



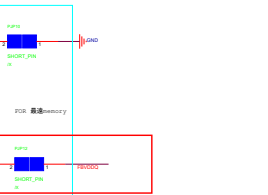
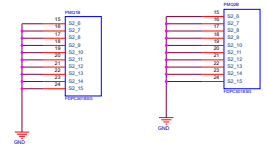
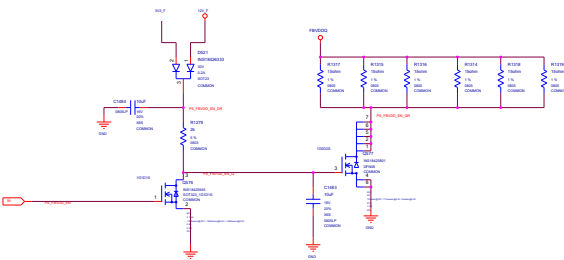
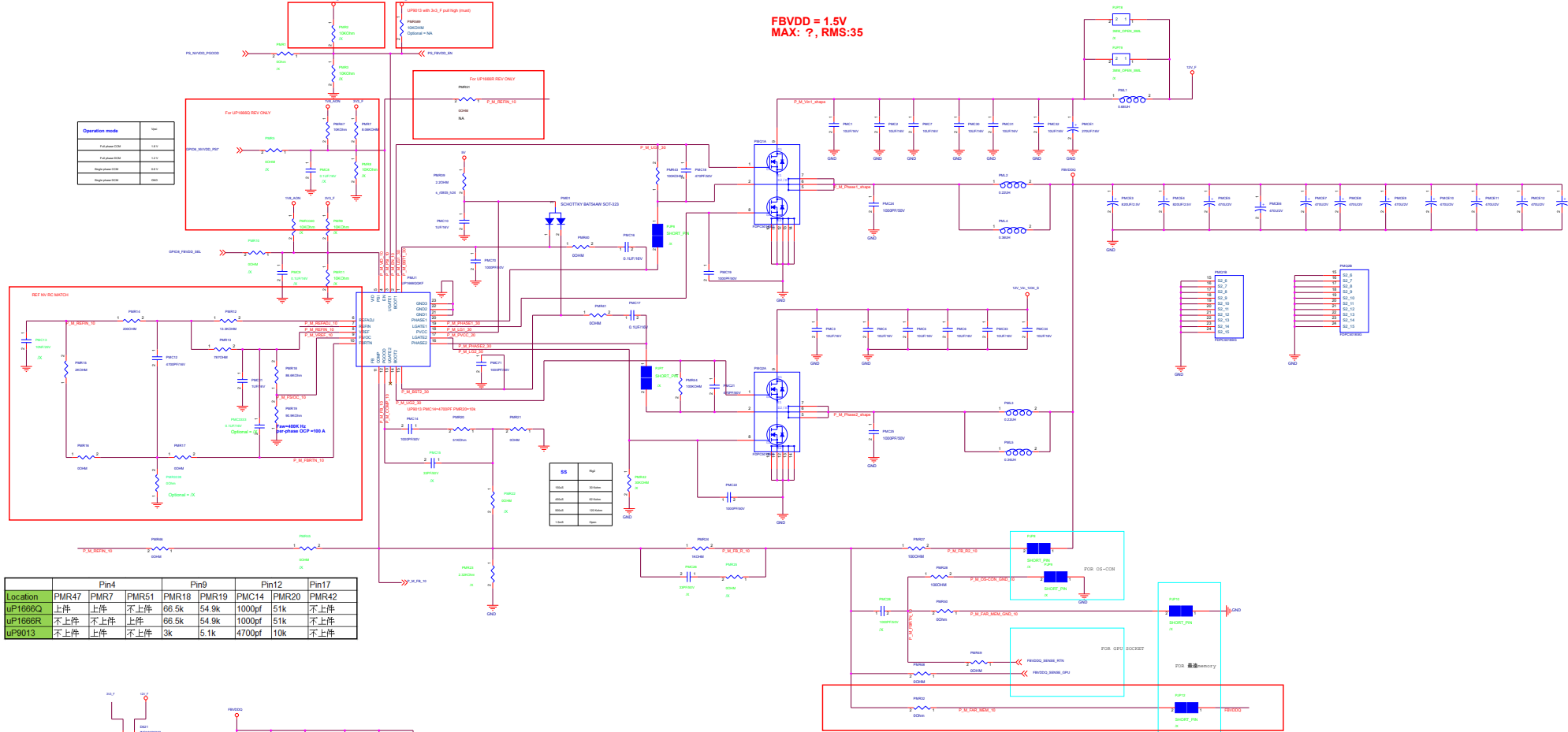
NV_PN	600-1G611-BASE-300
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SOM REV	A	DATE	26-SEP-2016

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FBVDD = 1.5V
MAX: ?, RMS:35

Operation mode	Test
Full power ON	100
Full power OFF	100
Standby ON	100
Standby OFF	100



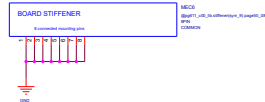
Brackets:



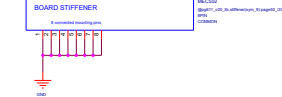
Bracket Screw



GPU Stiffener (BRING-UP COOLER)



QUAL COOLER STIFFENER



GPU HEATLINK



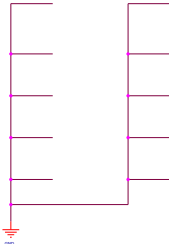
STIFFENER



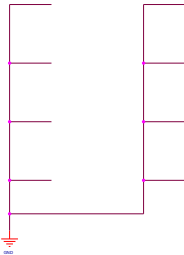
BOARD BACK PLATE

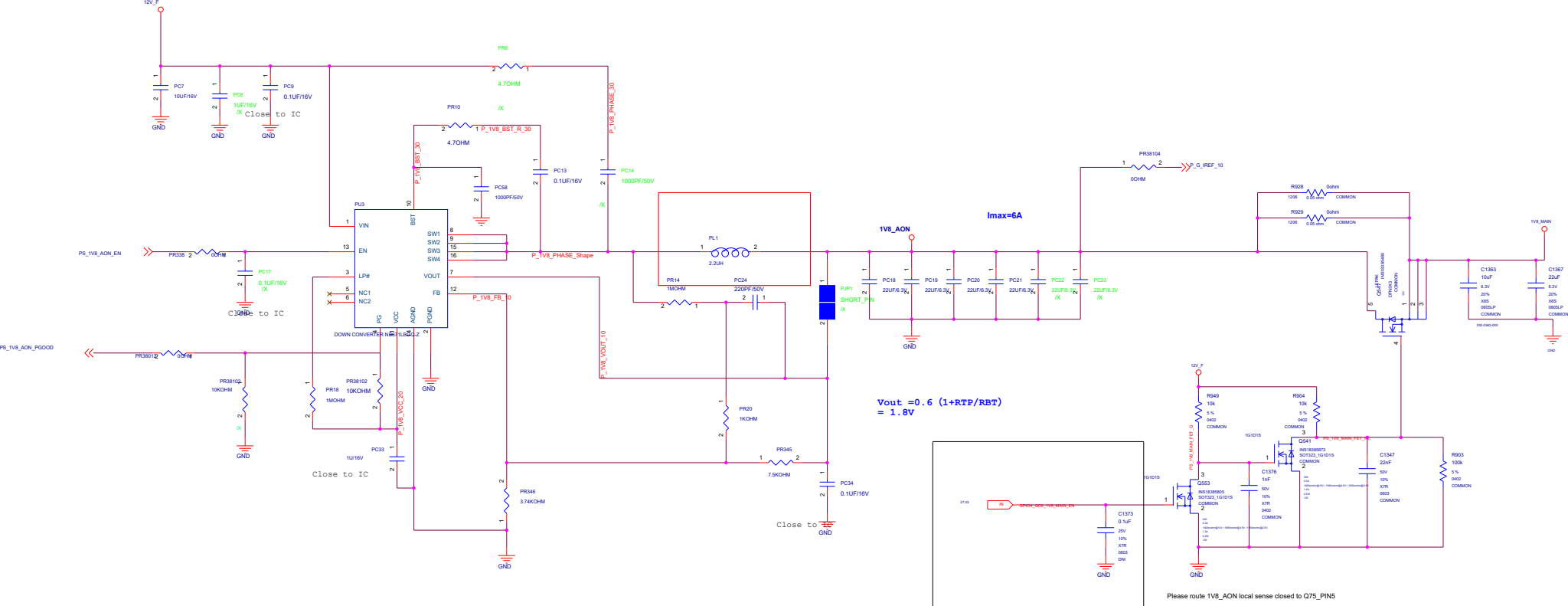


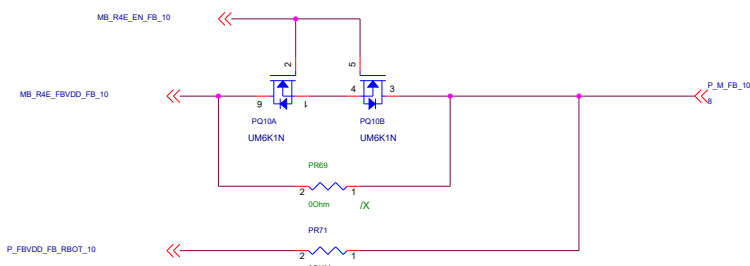
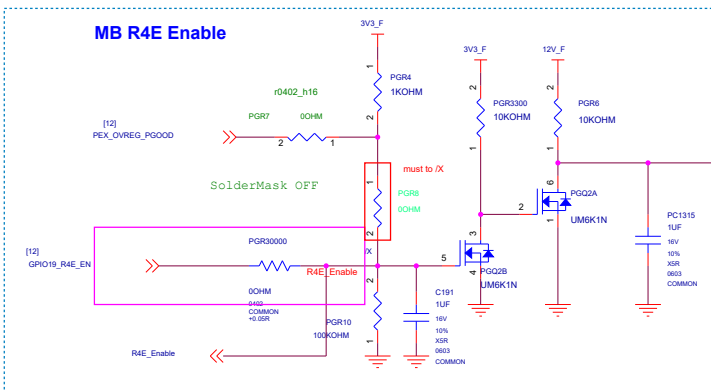
Mechanical Holes Symbol



GPU HOLES SYMBOL







MB_R4E_EN_FB_10
17,18,21

MB_R4E_NVDD_FB_10
13

Note:change to FB for超壓

P_NVDD_ADJ_RBOT_10_10
90

00hm PGR2394

1 2

10k12 10hm

1 2 3 4

PGR2393 PGR2394

UM8K1N UM8K1N

00hm

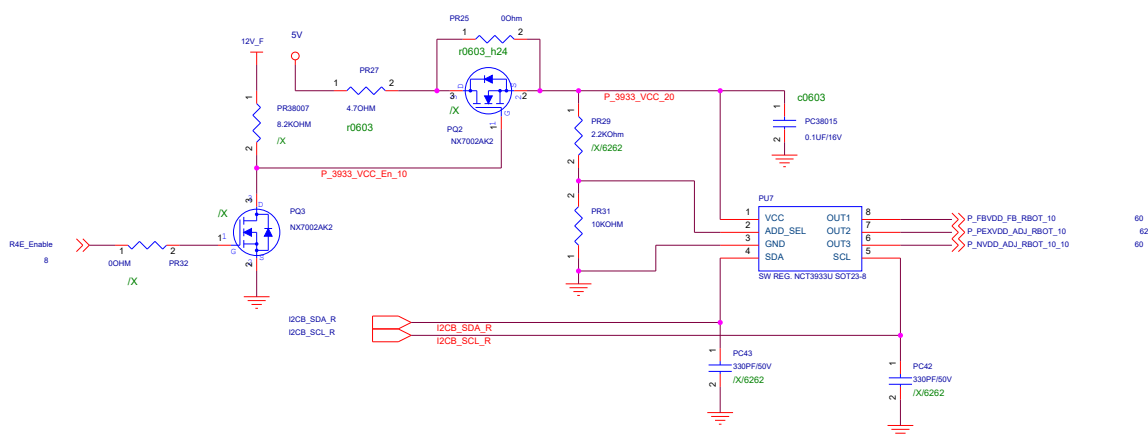
r0402_h16 /X

P_G_FB_10
8

1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V

1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPIO tri-state
VID[5:1]=11000 to set 0.9125V

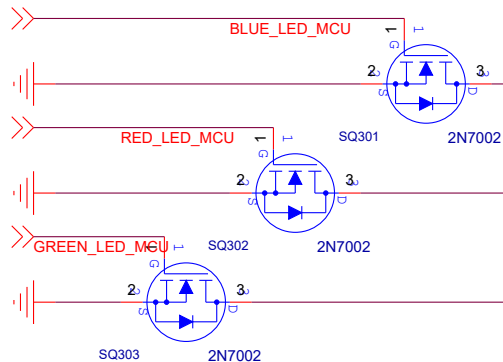
Address : 0x2A



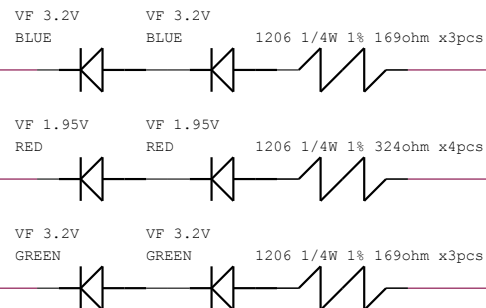
BLUE_LED_MCU

RED_LED_MCU

GREEN_LED_MCU



LED BOARD



BLUE_LED_MCU

RED_LED_MCU

GREEN_LED_MCU

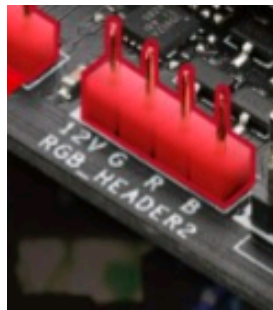
TO S0001 IT8915

+12V_LED

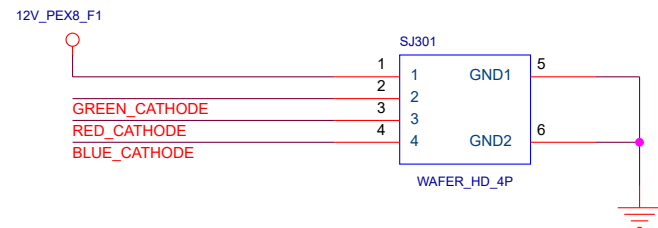
TO Power, Max 300mA

COVER LED線路

示意圖

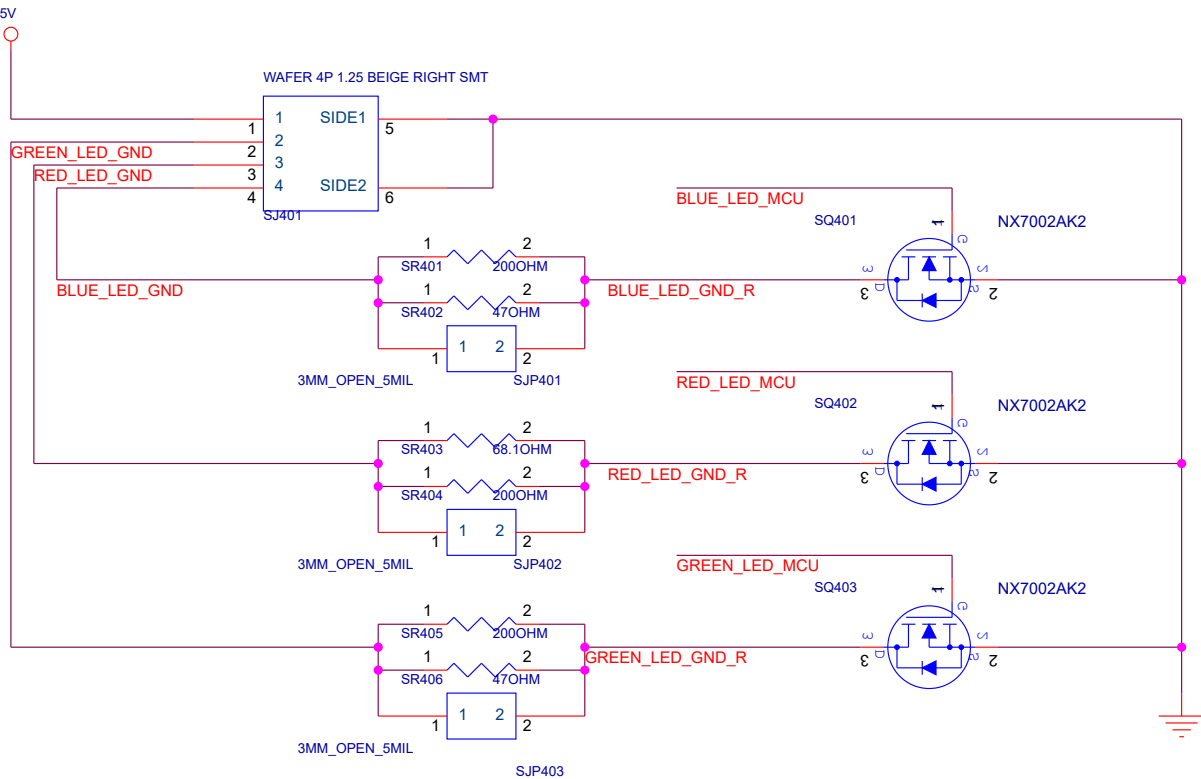
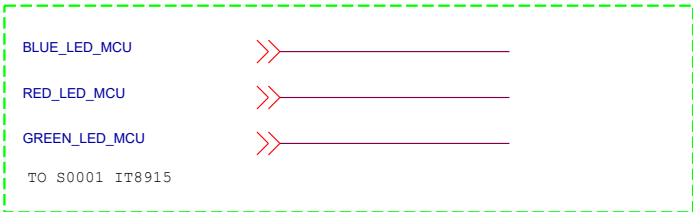
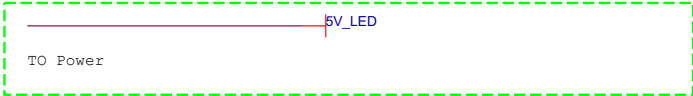


連接座旁請註明 12V G R B

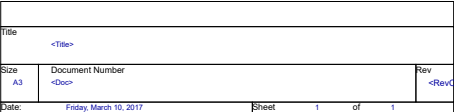


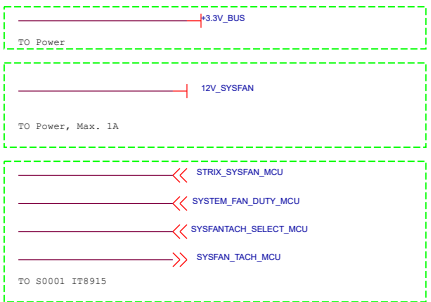
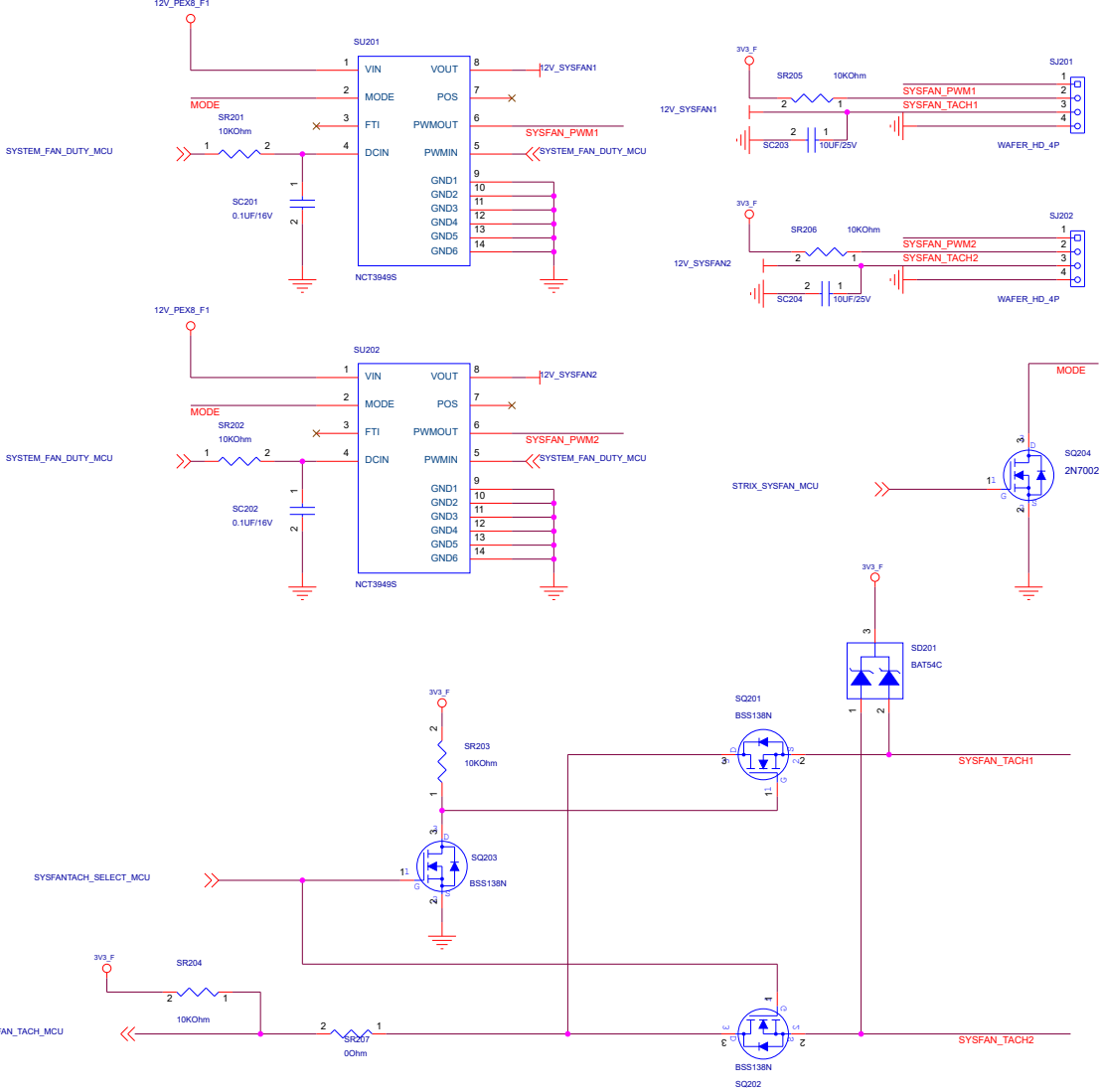
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Date:	Friday, March 10, 2017	Sheet 1 of 1

背板ROG LED線路



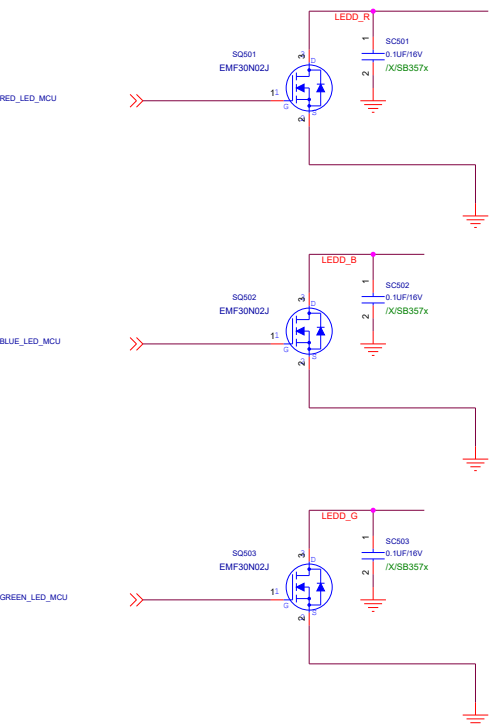
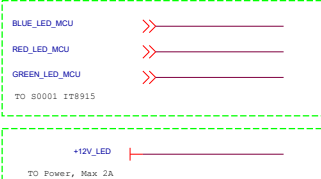
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Size	Document Number		Rev
A	<Doc>		<RevCode>
Date:	Friday, March 10, 2017	Sheet 1 of 1	





STRIX_SYSFAN_MCU	Mode
L	NORMAL
H(Default)	STRIX

SYSFANTACH_SELECT_MCU	Mode
L	SYSFAN_TACH1
H(Default)	SYSFAN_TACH2



示意圖



連接座旁請註明 12V G R B
RGB Header

