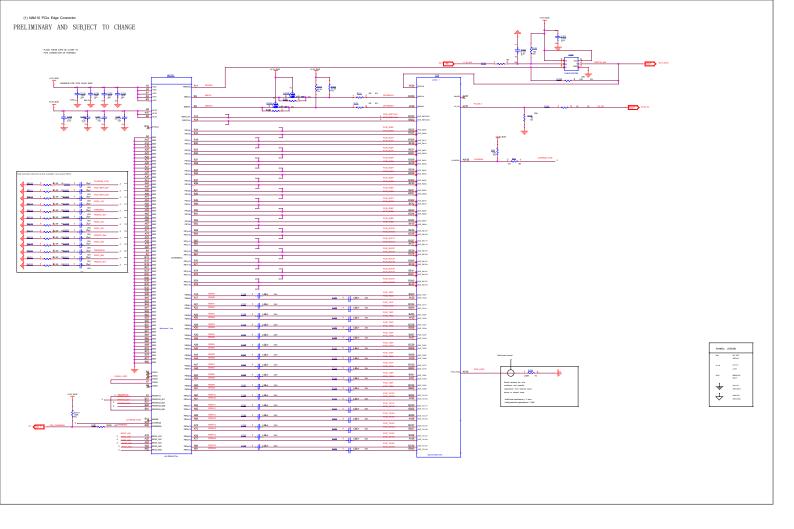
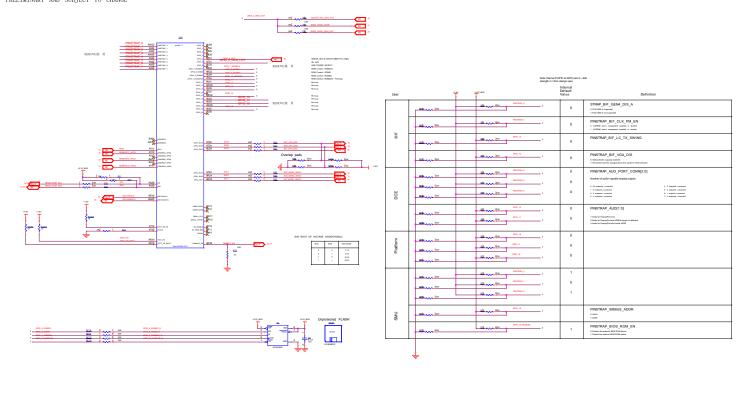
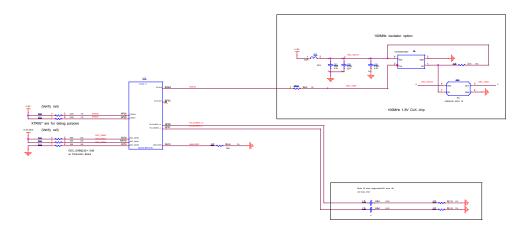
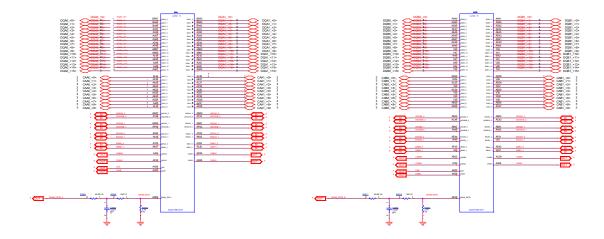
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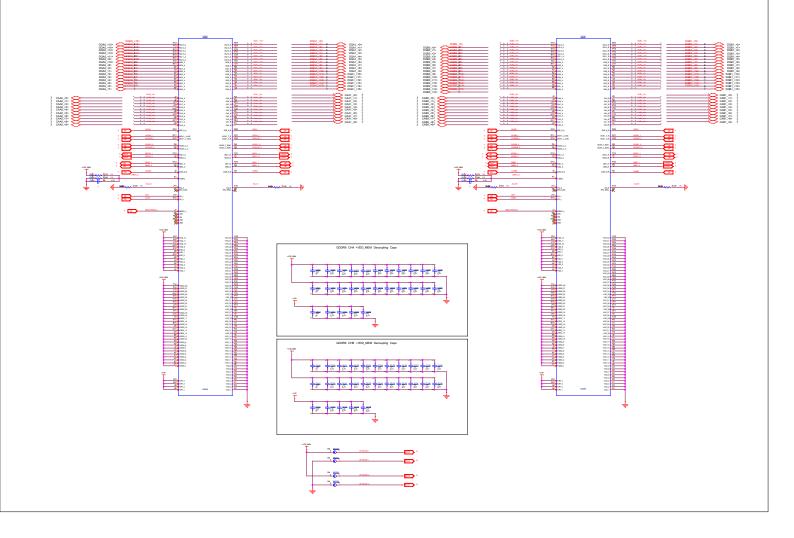
SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	SMALL RAL REGULATORS
2	NAM10 PCIs Interface	27	NAVIIO DECAPS
3	NAM10 GPIOs	28	NAVIO POWER
4	NAM10 XTAL	29	NAVIO GND
5	NAVIO MEM CHAB	30	POWER MANAGEMENT
6	NAMID MEM CHCD	31	SV2 & BAMACO
7	NAM10 MEM CHEF	32	MECHANICAL & THERMAL
8	NAMID MEM CHGH	33	DEBUG
9	GDDRS MEM CHAB	34	BLOCK DIAGRAM
10	GDDRS MEM CHCD	35	REVISION HISTORY
11	GDDRS MEM CHEF		
12	GDDRS MEM CHGH		
13	NAMIO TMDPA - DP		
14	NAM10 TMDPC - HDMI		
15	NAMIO TMOPEF - DP DP		
16	GFX & SOC CONTROLLER		
17	VDDCR_GFX PHASES 2 and 5		
18	VDDCR_GFX PHASES 1 and 4		
19	VDDCR_GFX PHASES 3 and 7		
20	VDDCR_GFX PHASES 6 and VDDCR_SDC		
21	MVDD_VDDCI CONTROLLER		
22	REG MVDD		
23	REG VODCI		
24	REG 0.79V		
25	REG 1.8V		

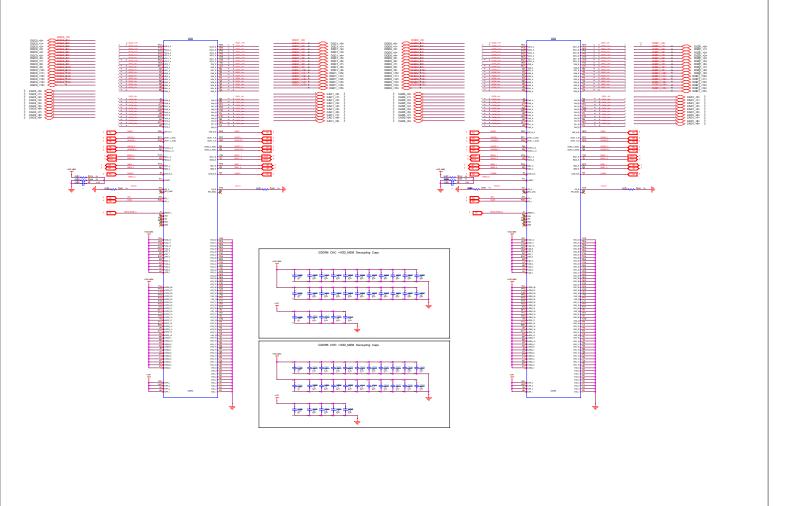


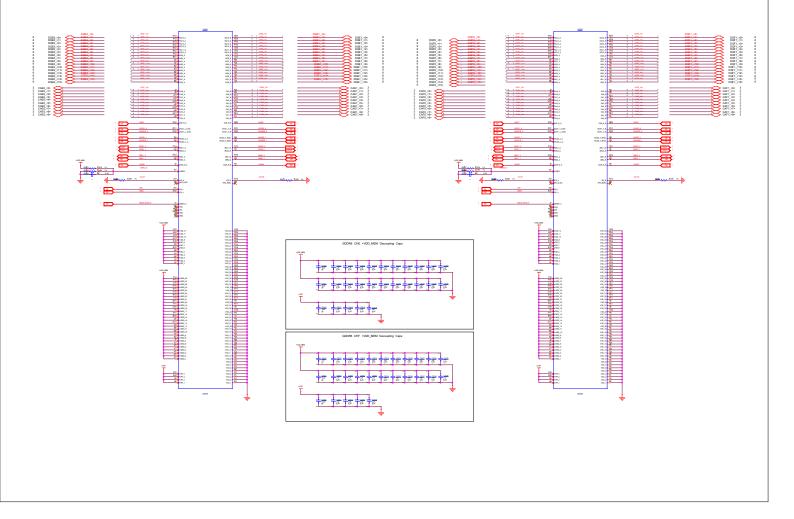




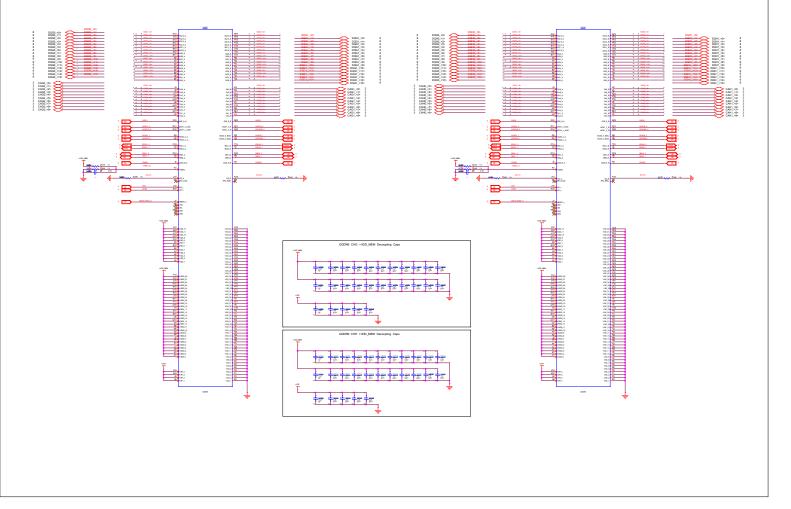






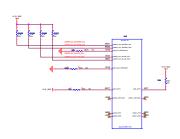


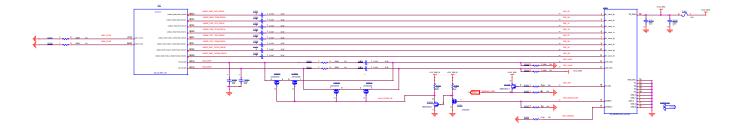


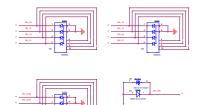


NAVI10 TMDP A/B



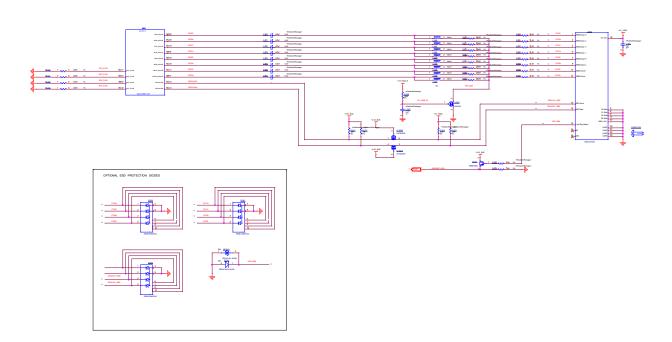




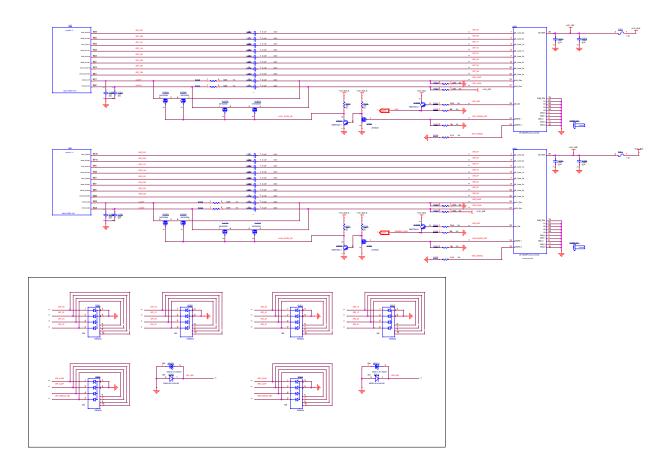


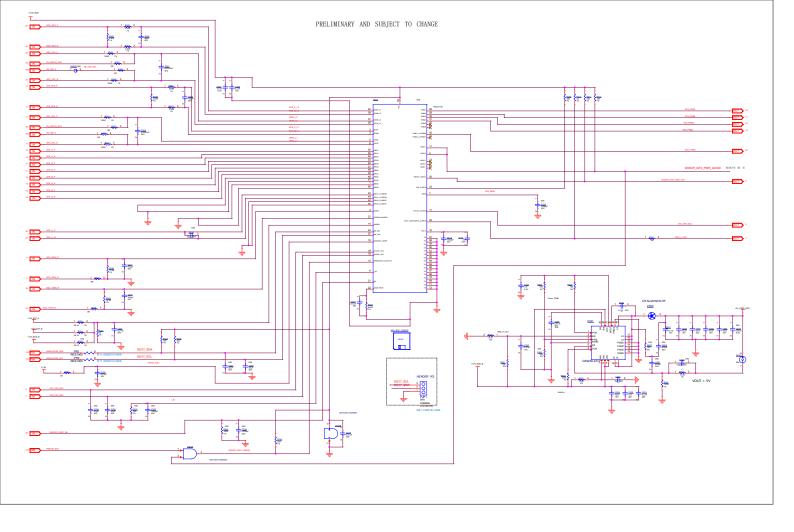
NAVI10 TMDP C/D

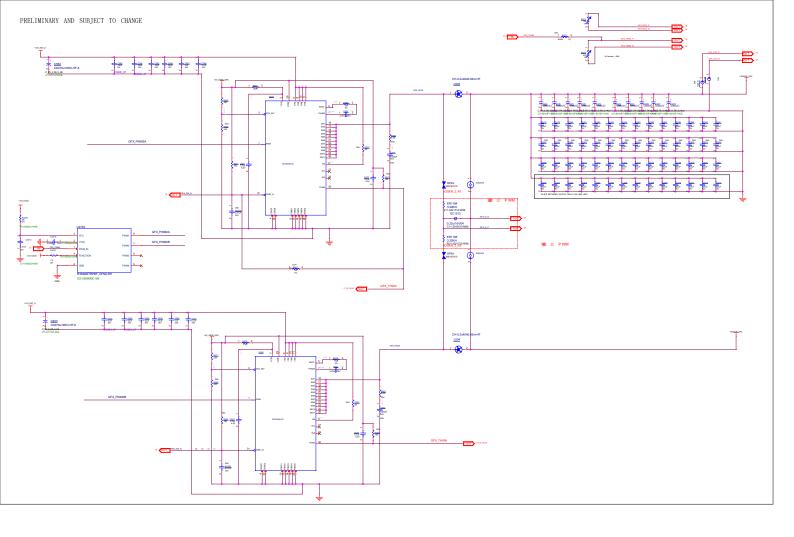


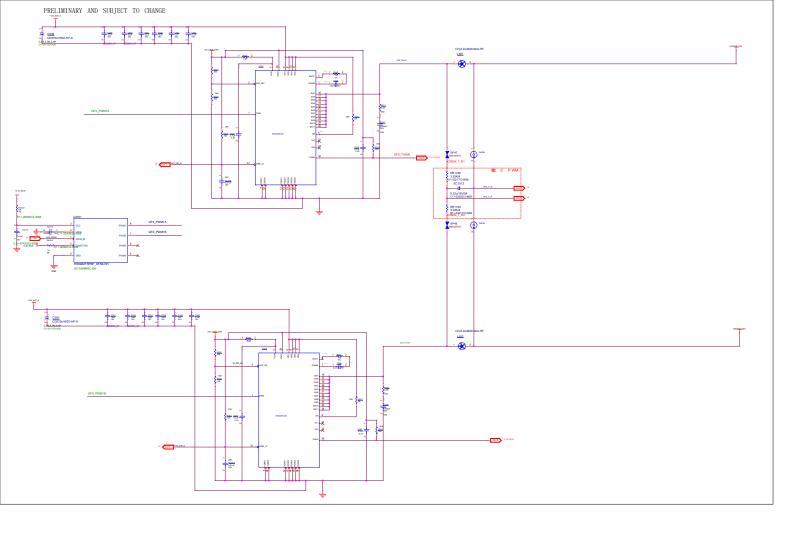


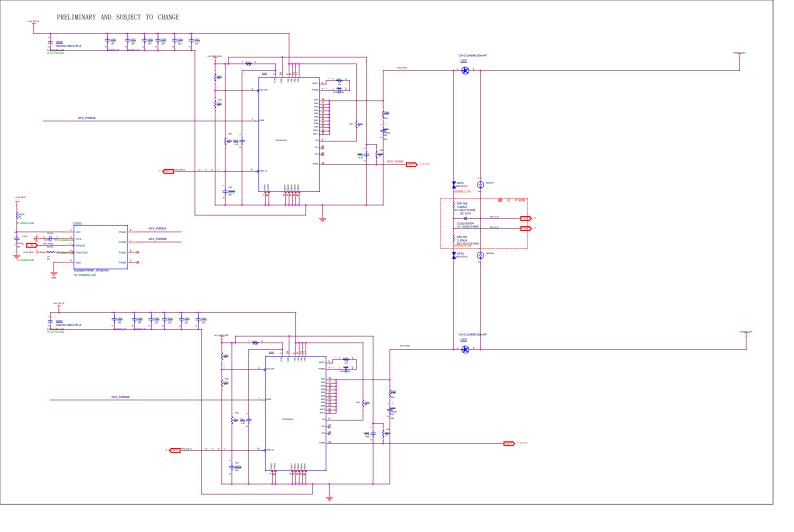
(9) NAVI10 TMDP E/F

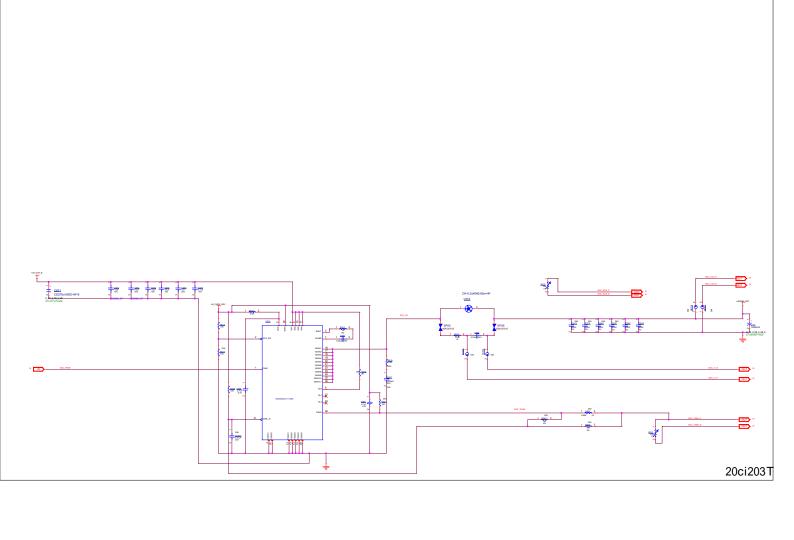


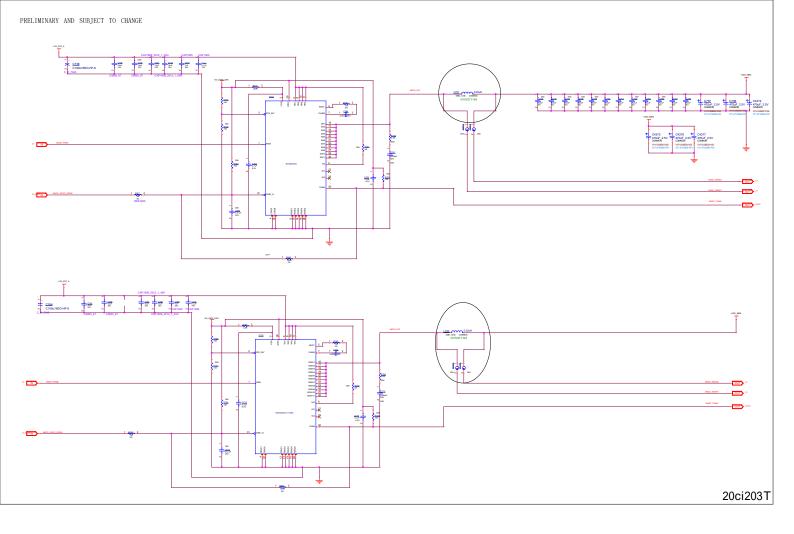


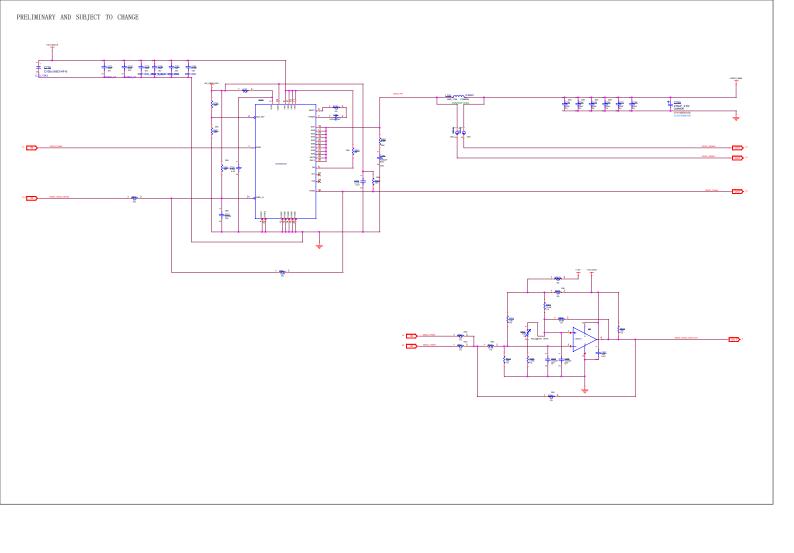


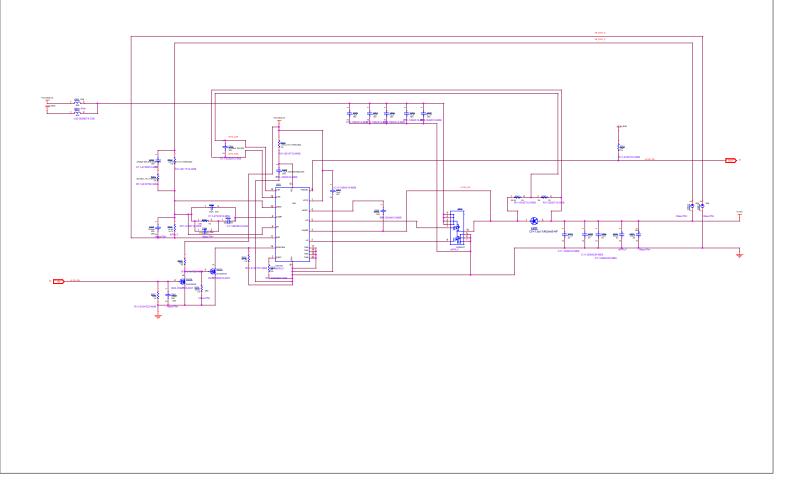


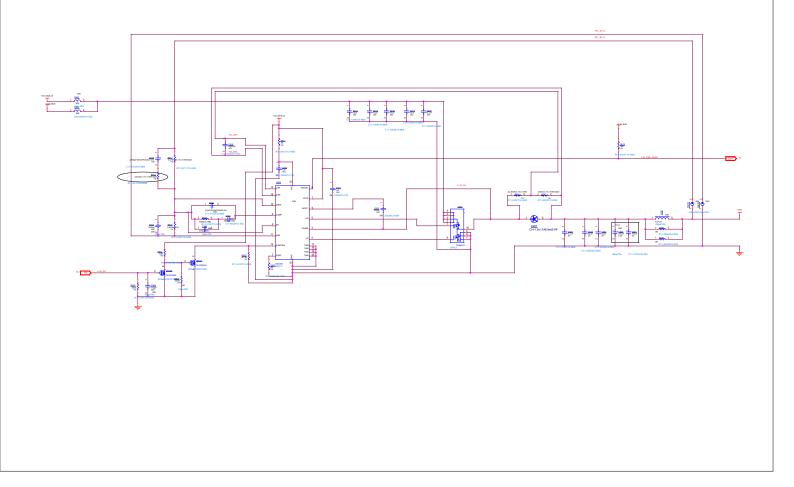


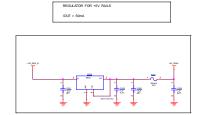


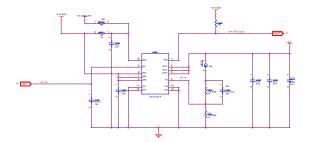


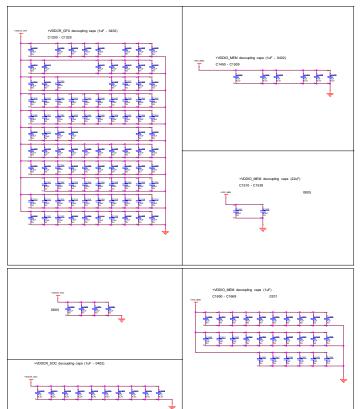


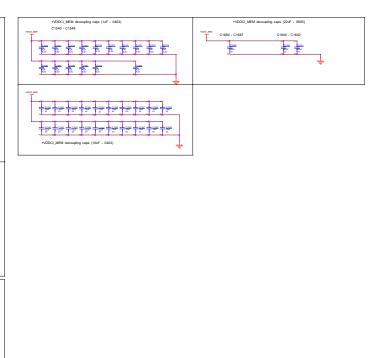


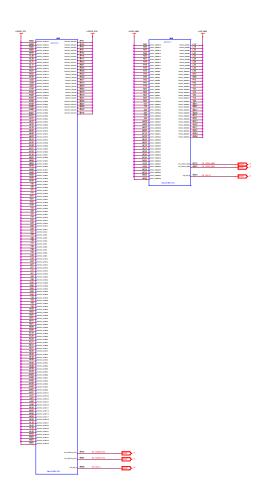


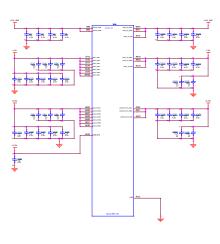




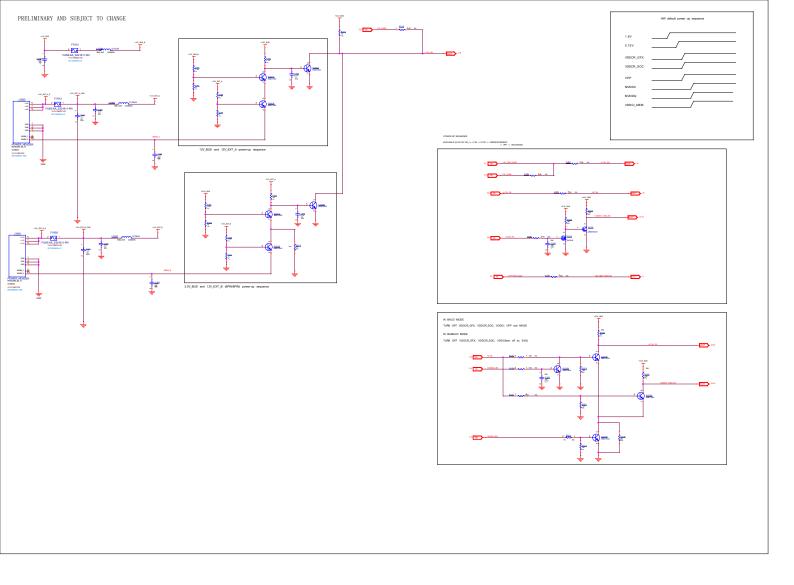


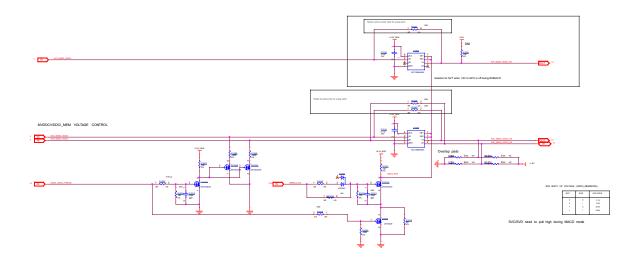


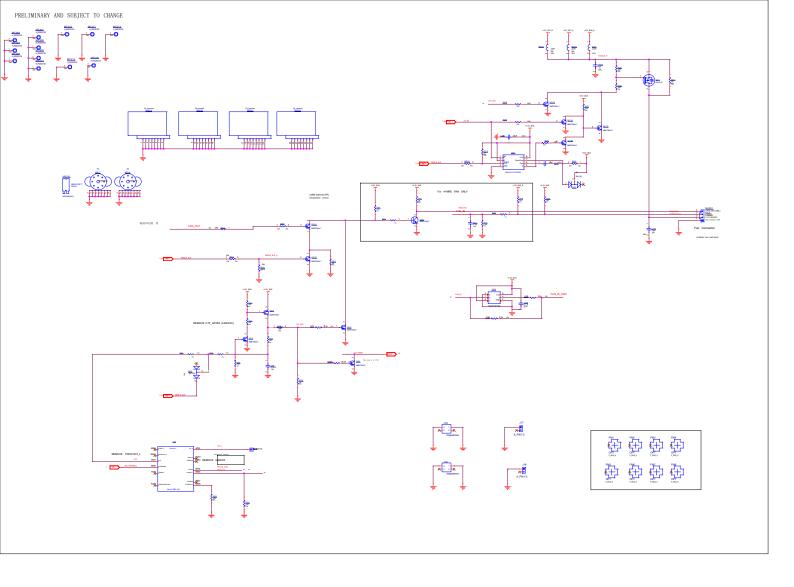


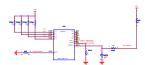




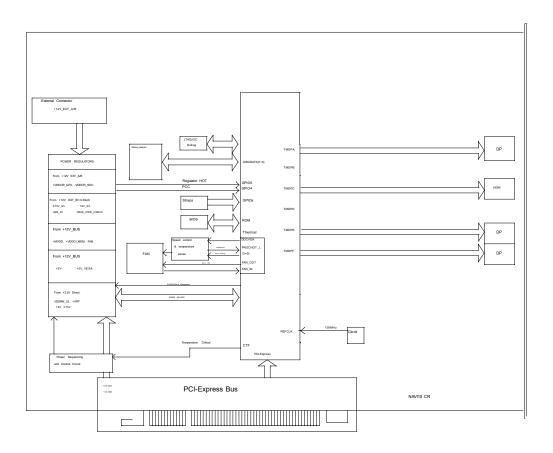


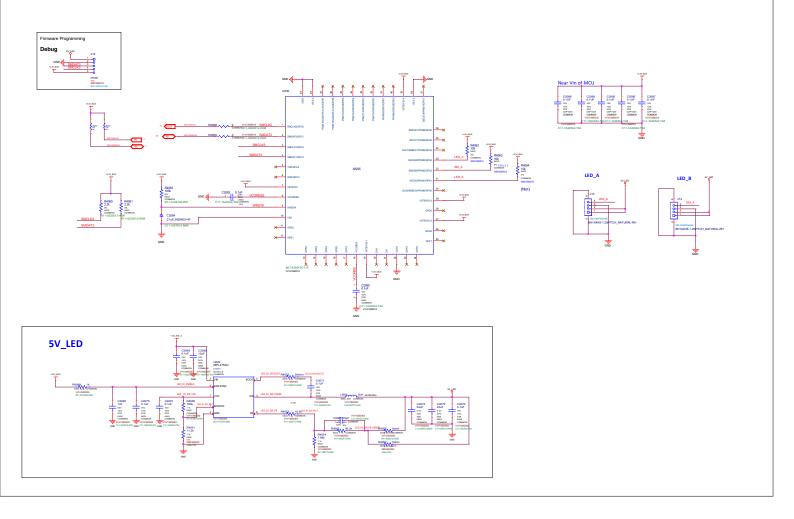


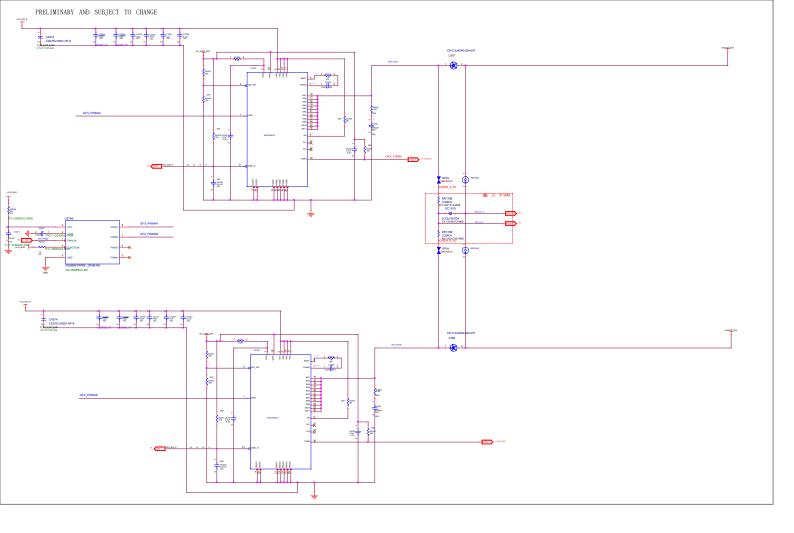


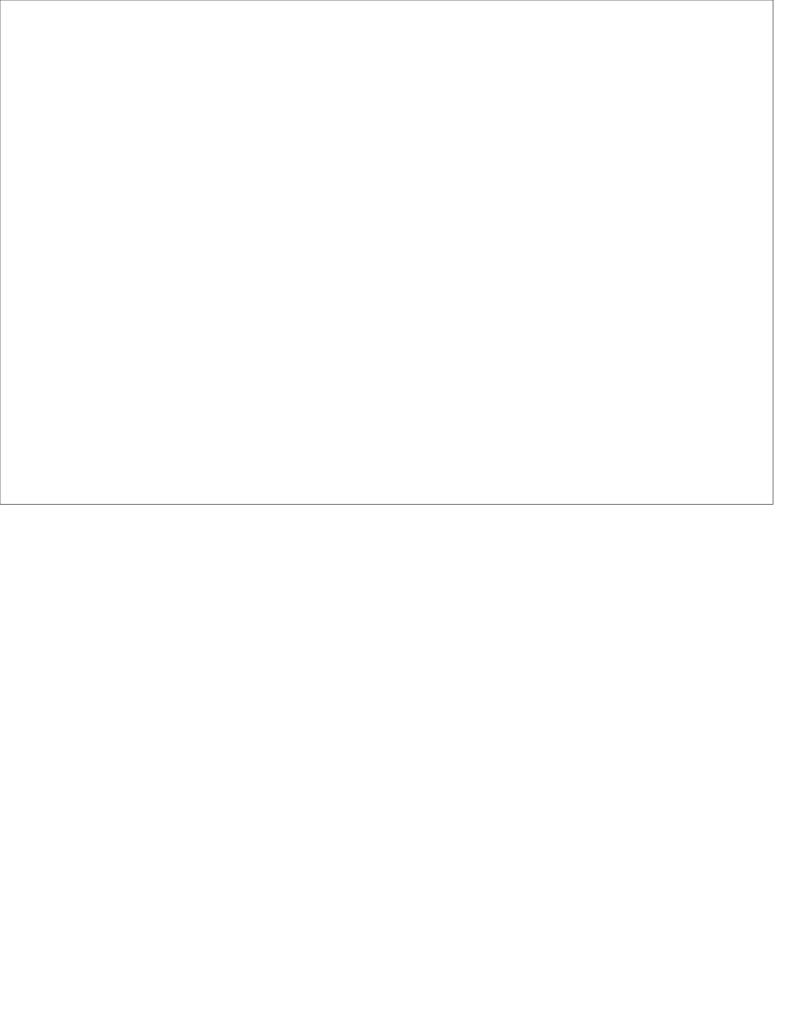


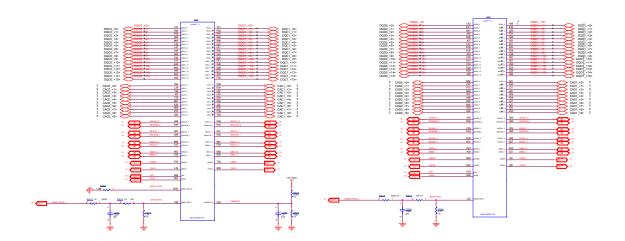
RACECN Lighter beader	



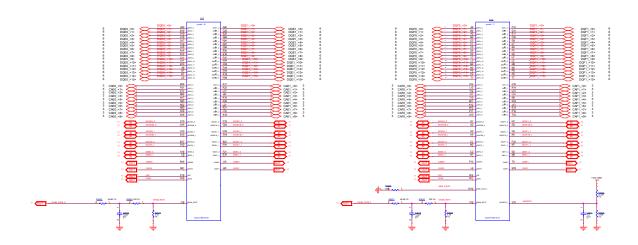














NAVI 10 MEM INTERFACE CH G/H

