

G94-P545-A01 - GDDR3, DVI/VGA + DVI/VGA + Display port + HDMI

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10545-000-100	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SRU0100	600-10545-0100-100	G94-400 650MHz/1000MHz 512MB 16MA32 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out (Bring Up SRU)
2	SRU0200	600-10545-0200-100	G94-400 650MHz/1000MHz 512MB 16MA32 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out
3	SRU0310	600-10545-0310-100	G94-300 500MHz/800MHz 512MB 16MA32 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out
4	SRU0320	600-10545-0320-100	G94-300 500MHz/800MHz 384MB 16MA32 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out
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V145-0A Base on V135-100 and P545


- 1.PAGE21: Remove HD Audio circuit.
- 2.PAGE19: Remove DACB HDTV circuit.
- 3.PAGE18: Modify DP_Power circuit and AUX channel circuit
- 4.PAGE 27:Phase adjustment by loading circuit
- 5.PAGE15: Remove DACC D-Sub connector
- 6.PAGE16,17: Add J5 Dual DVI connector
- 7.PAGE 25 add Optical Spidf in connector.
- 8.PAGE 28 Change FBVDD power solution to UP6205 and PEX_VDD to UP7706
- 9.PAGE 29 add Winbond W83L786G Hardware monitor
- 10.PAGE 30 Change NVVDD power solution to ISL6334

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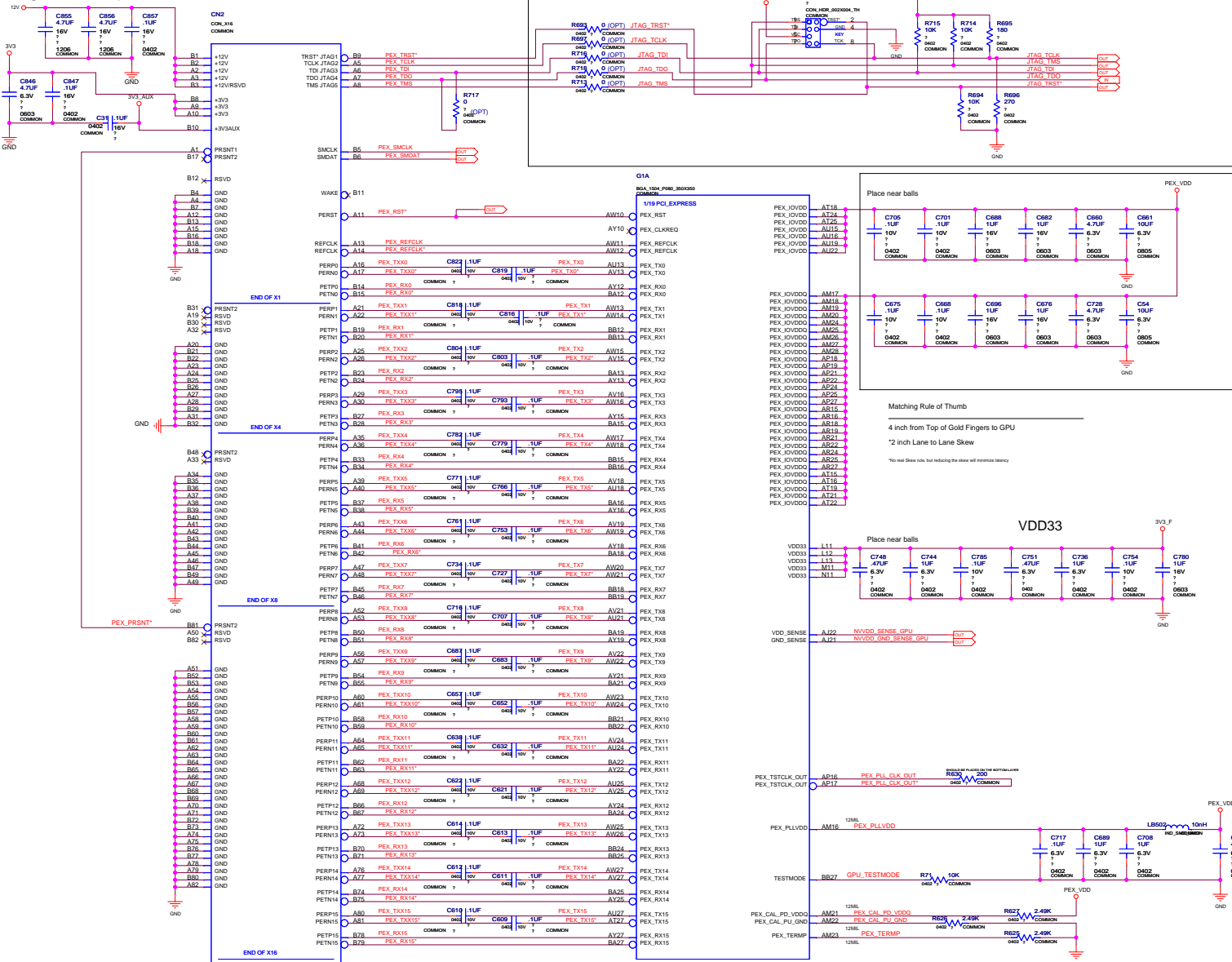
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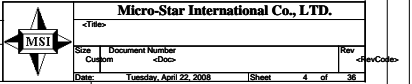
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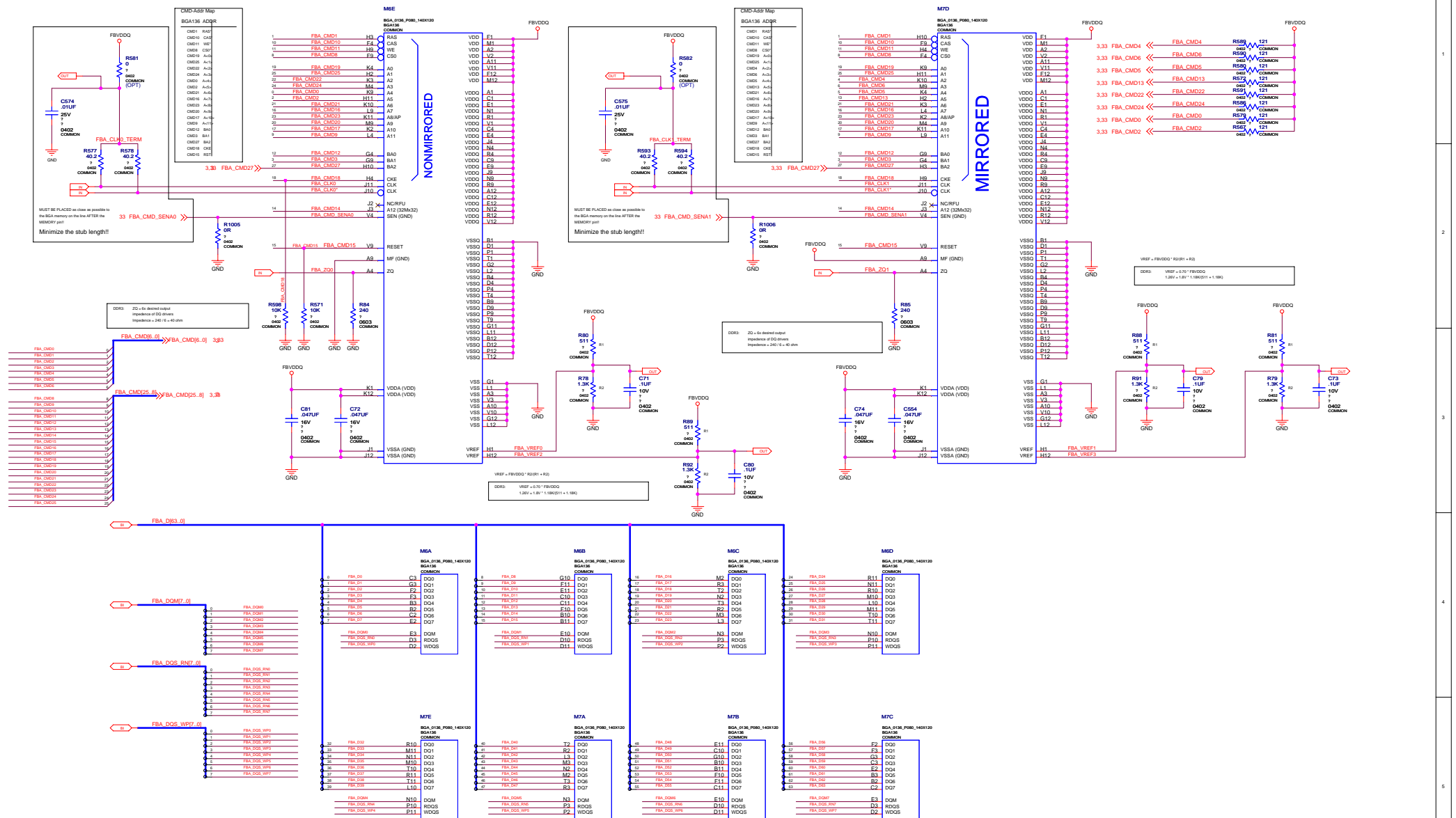


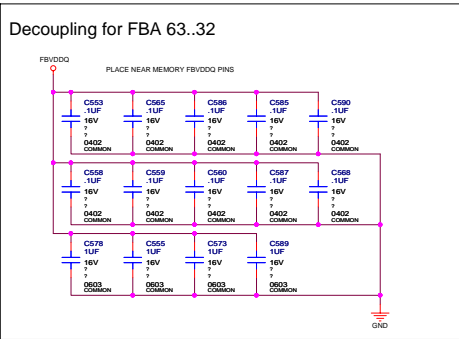
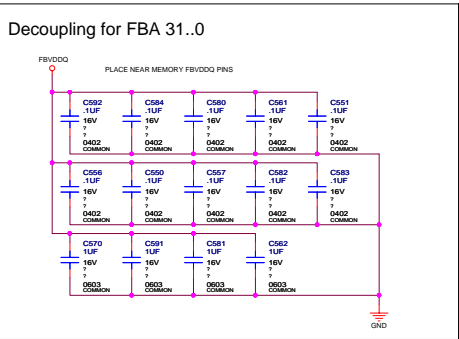
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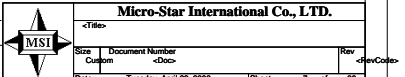
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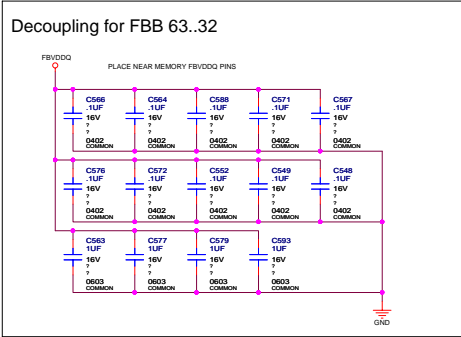
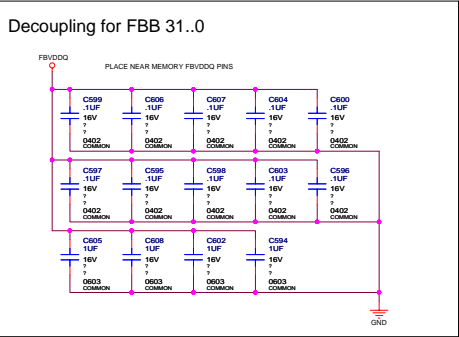


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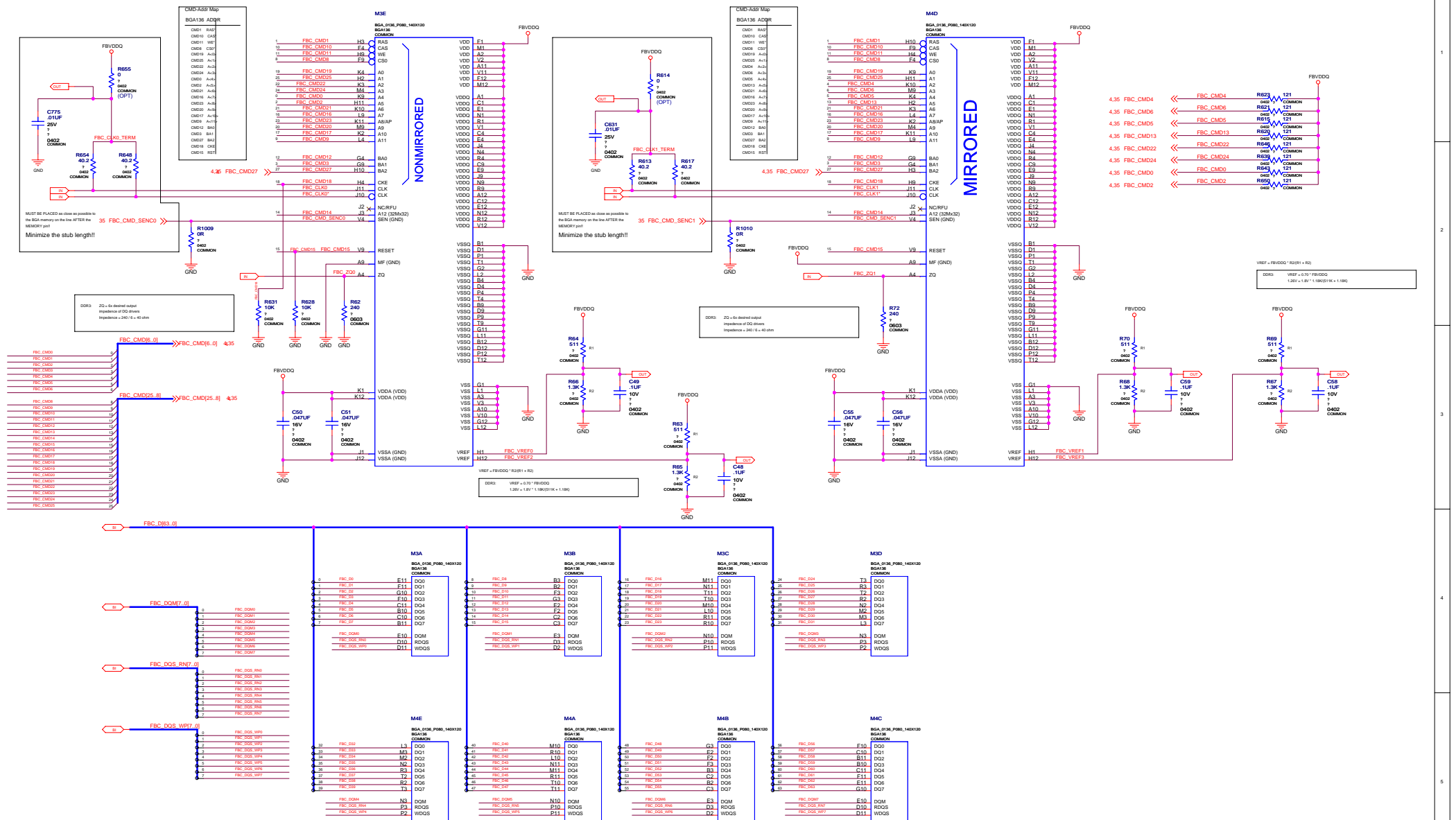
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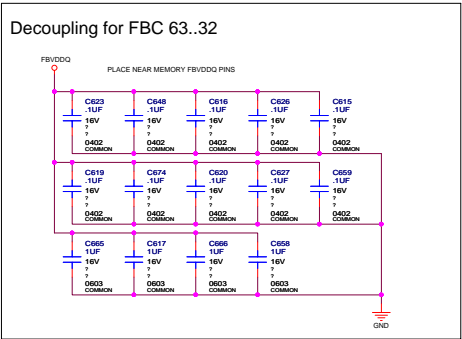
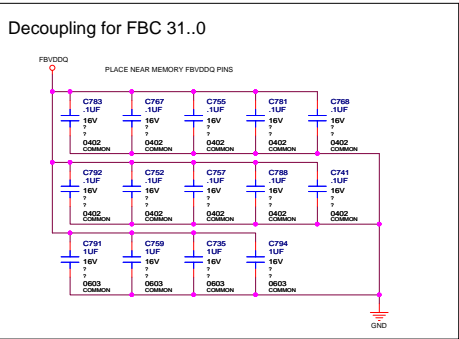


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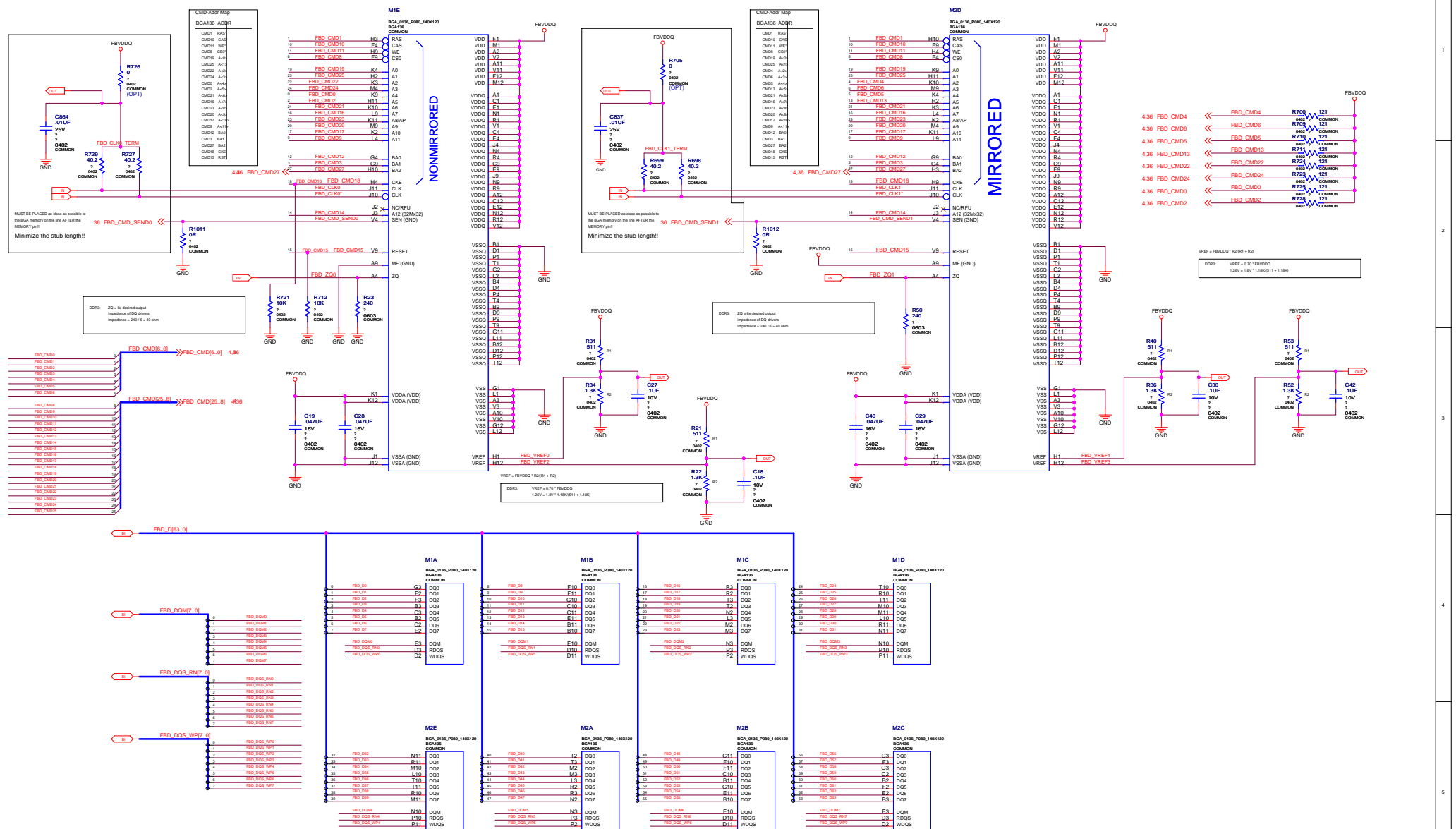
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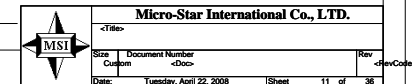


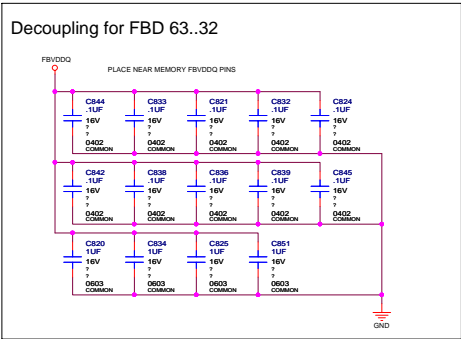
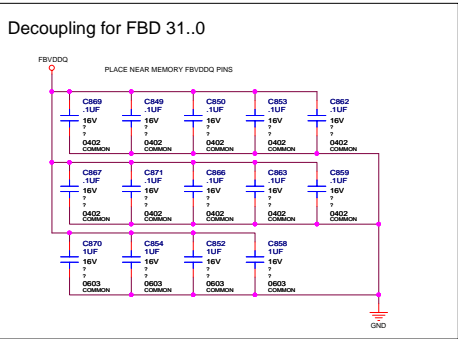
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OUT	FBA_CLK0	1	500F	FBA_CLK0
OUT	FBA_CLK0*	1	500F	FBA_CLK0
OUT	FBA_CLK0_TERM	1	600M	
OUT				
OUT	FBA_CLK1	1	500F	FBA_CLK1
OUT	FBA_CLK1*	1	500F	FBA_CLK1
OUT	FBA_CLK1_TERM	1	600M	

NET	NV_CRITICAL_NET	IMPEDANCE
OUT	FBA_DG5_W9P7_0	1
IN	FBA_DG5_W9P7_0	1
OUT	FBA_DG4P7_0	1
IN	FBA_DG4P7_0	1

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
OUT FSB_CLK0	1	NOFF	FSB_CLK0
OUT FSB_CLK0*	1	NOFF	FSB_CLK0
OUT FSB_CLK0_TERM	1	NOFF	FSB_CLK0
OUT	1	NOFF	
OUT FSB_CLK1	1	NOFF	FSB_CLK1
OUT FSB_CLK1*	1	NOFF	FSB_CLK1
OUT FSB_CLK1_TPHSM	1	NOFF	FSB_CLK1

	NET	NV_CRITICAL_NET	IMPEDANCE
OUT	F88_DQ5_WF07_0	1	400M
IN	F88_DQ5_WF07_0	1	400M
OUT	F88_DQ6_WF7_0	1	400M
IN	F88_DQ6_0	1	400M

	NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
6	FB_PLAUC00	120%	1.1V	0.00A
6	FB_VREF	120%	1.20V	0.00A
6	FBA_VREF0	120%	1.20V	0.00A
6	FBA_VREF1	120%	1.20V	0.00A
6	FBC_VREF2	120%	1.20V	0.00A
6	FBA_VREF3	120%	1.20V	0.00A
6	FBA_ZD0	120%	1.20V	0.00A
6	FBC_ZD1	120%	1.20V	0.00A
6	FBA_VREF0	120%	1.20V	0.00A
6	FBC_VREF1	120%	1.20V	0.00A
6	FBA_VREF2	120%	1.20V	0.00A
6	FBC_VREF3	120%	1.20V	0.00A
6	FBA_ZD0	120%	1.20V	0.00A
6	FBC_ZD1	120%	1.20V	0.00A

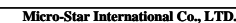
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OUT	FBC_CLK0*	1	500FT	FBC_CLK0
OUT	FBC_CLK0_TERM	1	600M	
OUT				
OUT	FBC_CLK1	1	500FT	FBC_CLK1
OUT	FBC_CLK1*	1	500FT	FBC_CLK1
OUT	FBC_CLK1_TERM	1	600M	

NET	NV_CRITICAL_NET	IMPEDANCE
OUT	FBC_DQ5_WP07_0	400UM
IN	FBC_DQ5_WP07_0	400UM
OUT	FBC_DQ047_0	400UM
IN	FBC_DQ047_0	400UM

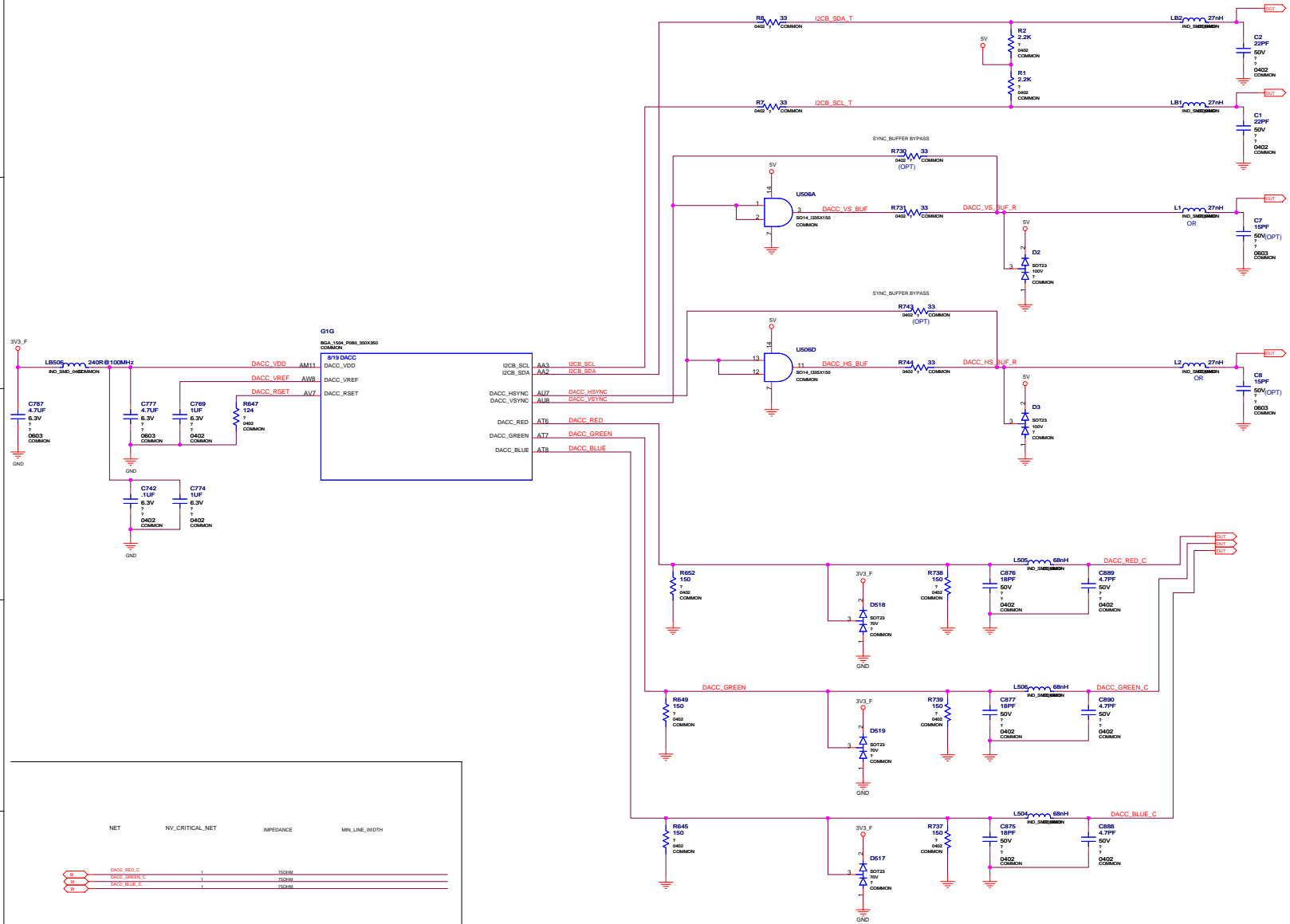
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OUT F8D_CLK0	1	NOFFT	F8D_CLK0
OUT F8D_CLK0*	1	NOFFT	F8D_CLK0
OUT F8D_CLK0_TERM	1	ACSHM	
OUT F8D_CLK1	1	NOFFT	F8D_CLK1
OUT F8D_CLK1*	1	NOFFT	F8D_CLK1
OUT F8D_CLK1_TFHM	1	NOFFT	F8D_CLK1

	NET	NV_CRITICAL_NET	IMPEDANCE
OUT	F8D_DQS_WRP[7:0]	1	400M
IN	F8D_DQS_WRP[5]	1	400M
OUT	F8D_DQM[7:0]	1	400M
IN	F8D_DQM[5]	1	400M

	NET	MIN_LINE_WIDTH	VOLTAGE	NV.NET_MAX_CURRENT
0	FB_PLAU001	120%	1.1V	0.04A
0	FBC_VREF0	120%	1.80V	0.03A
0	FBC_VREF1	120%	1.80V	0.03A
0	FBC_VREF2	120%	1.80V	0.03A
0	FBC_VREF3	120%	1.80V	0.03A
0	FBC_Z00	120%	1.80V	0.03A
0	FBC_Z01	120%	1.80V	0.03A
0	FBD_VREF0	120%	1.80V	0.03A
0	FBD_VREF1	120%	1.80V	0.03A
0	FBD_VREF2	120%	1.80V	0.03A
0	FBD_VREF3	120%	1.80V	0.03A
0	FBD_Z00	120%	1.80V	0.03A
0	FBD_Z01	120%	1.80V	0.03A




DACC RGB-FILTER



NET	INV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACC_RED_C	1	120OHM	
DACC_GREEN_C	1	120OHM	
DACC_BLUE_C	1	120OHM	
DACC_RED_C	2	120OHM	
DACC_GREEN_C	2	120OHM	
DACC_BLUE_C	2	120OHM	

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DACC Interface



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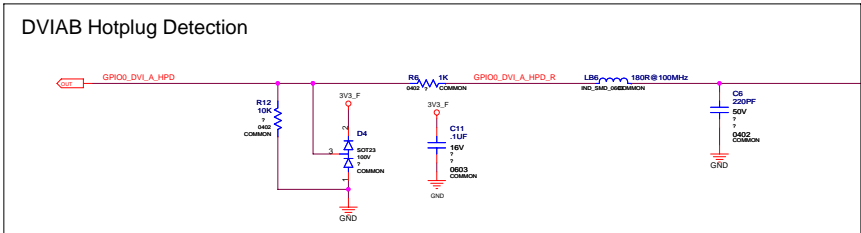
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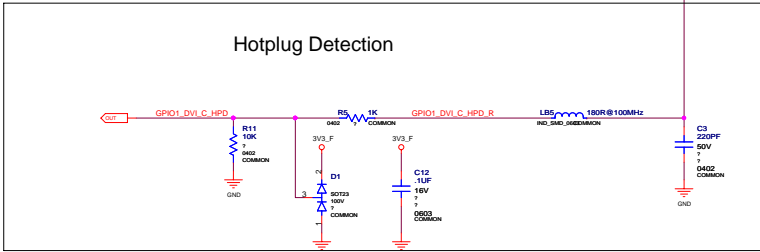
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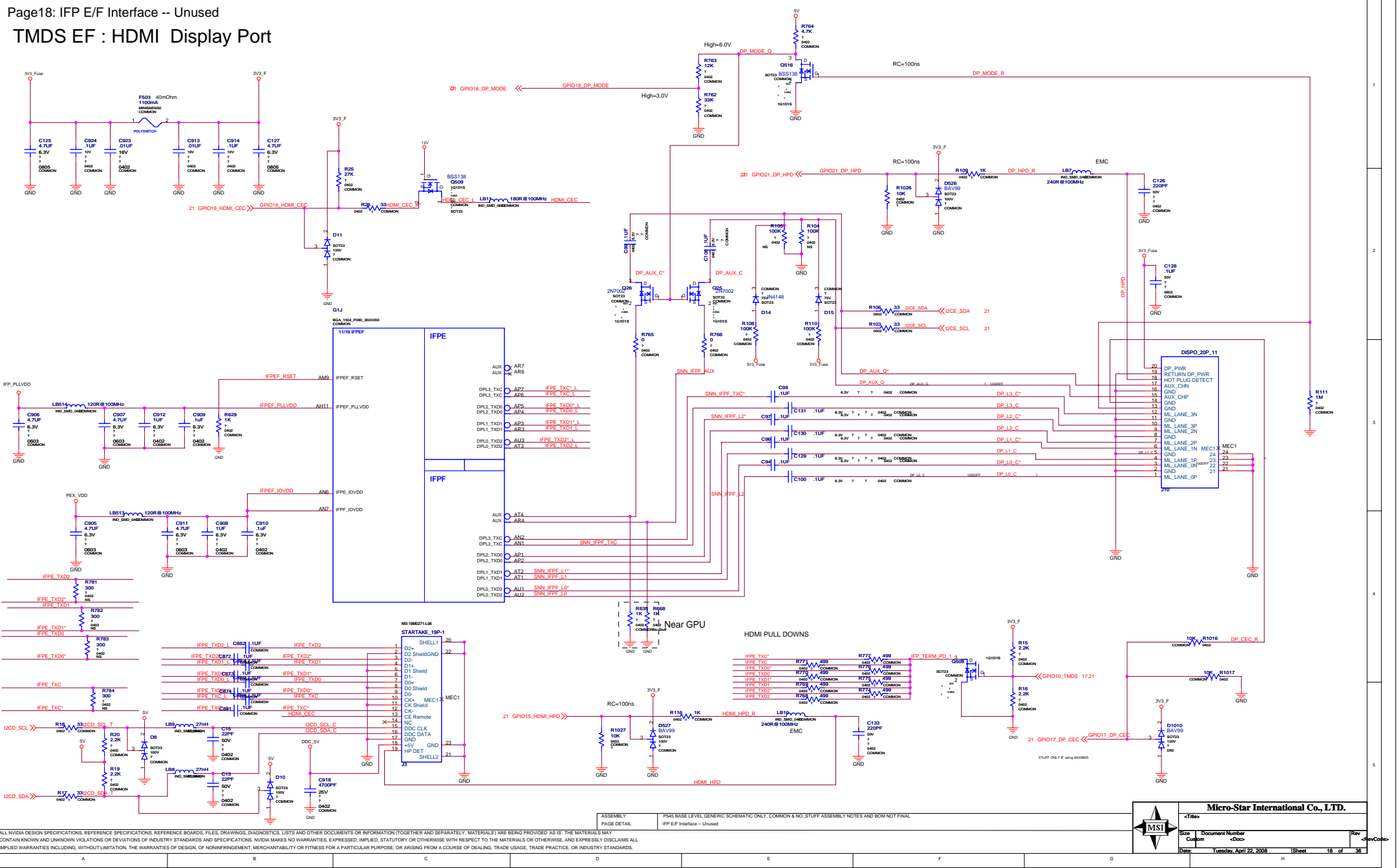


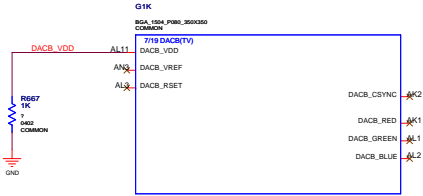
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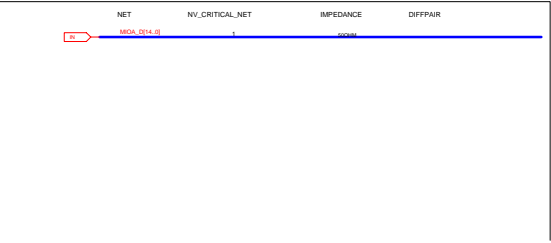
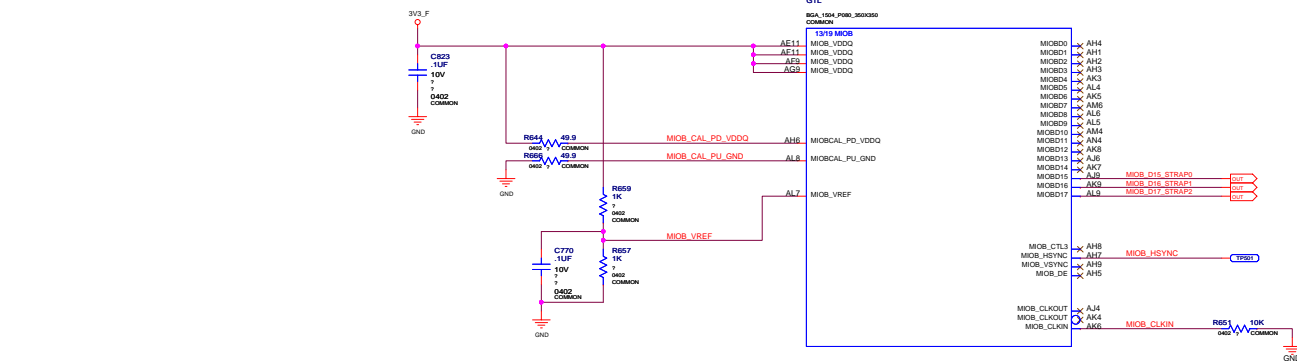
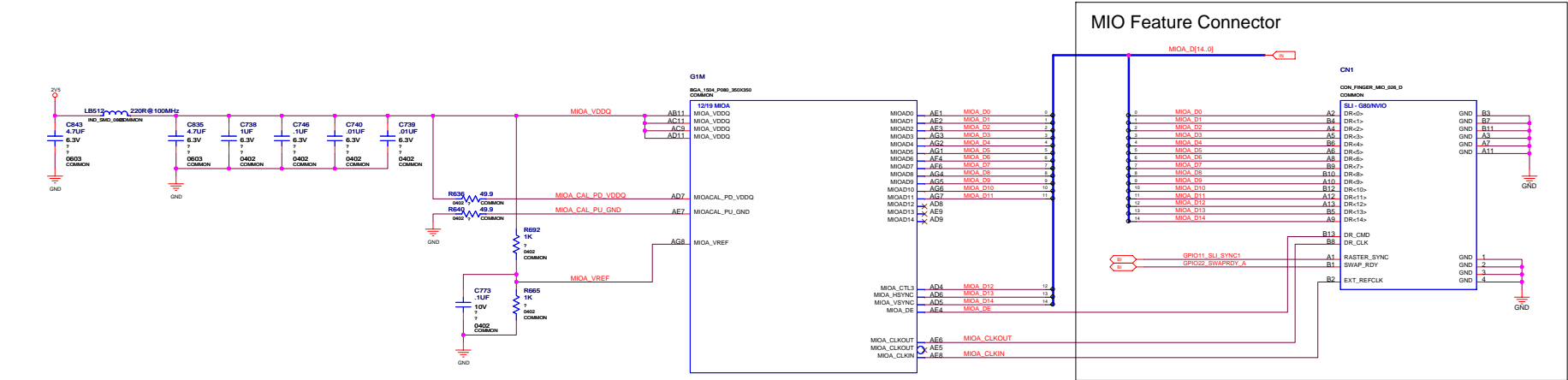
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ASSEMBLY PAGE DETAIL
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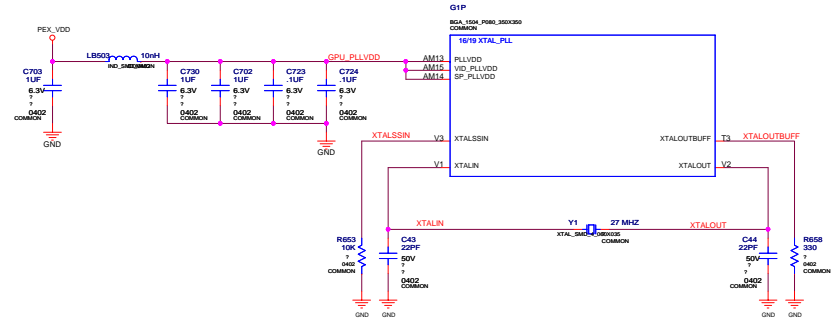
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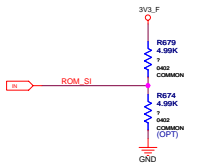
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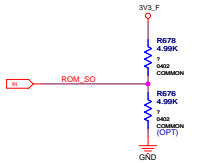
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	Date: Tuesday, April 22, 2008	Sheet 21 of 36	



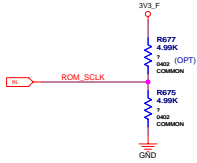


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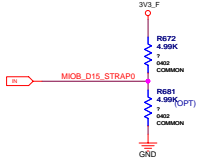
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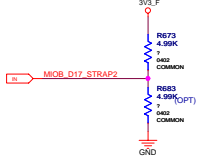
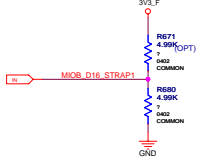
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ROM_SO	SLOT_CLK_CFG	



STRAP PIN	STRAP NAME	
ROM_SCLK	PCI_DEVID[3]	




STRAP PIN	STRAP NAME	
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STRAP1	RAMCFG1	
STRAP2	RAMCFG2	



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ACM6	NC
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ASSEMBLY PAGE DETAIL
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Strap Configuration



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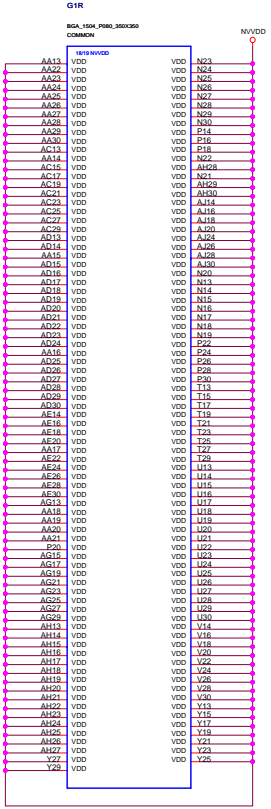
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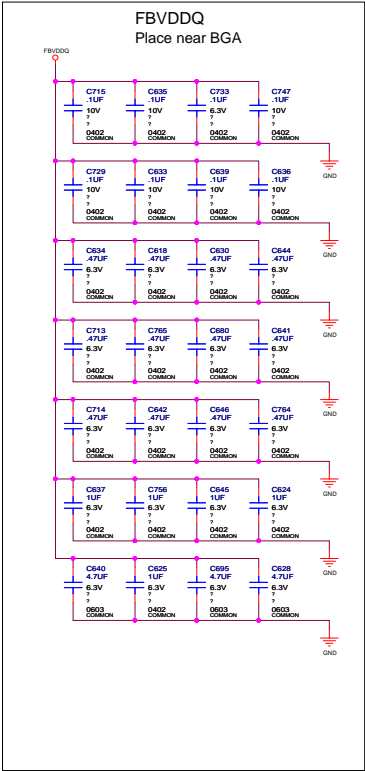
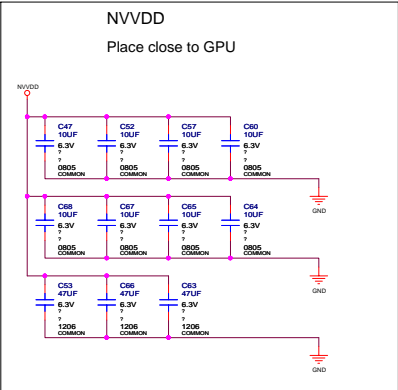
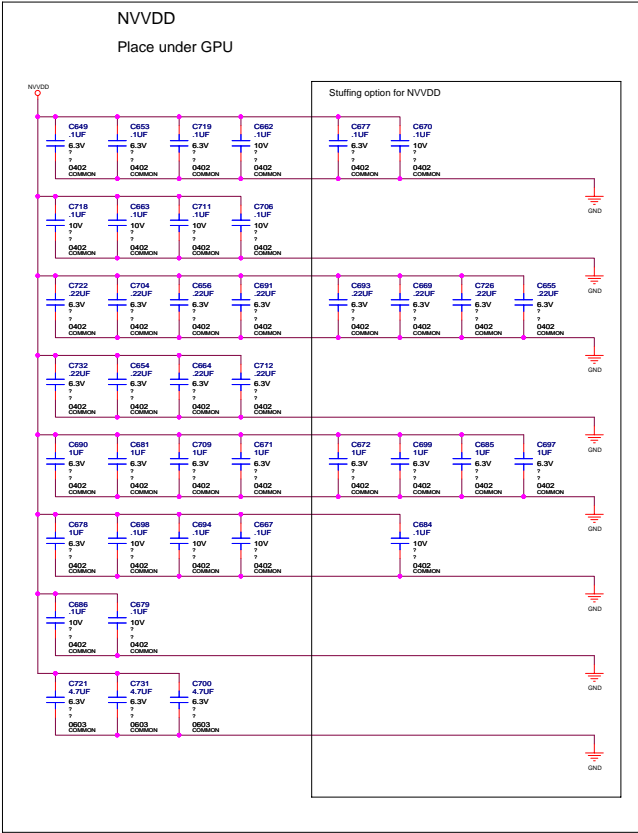
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Rev <Rev Code>





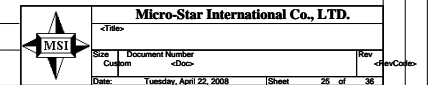
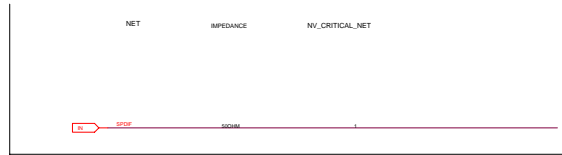
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ASSEMBLY
PAGE DETAIL
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NVVDD and FBVDDQ Decoupling

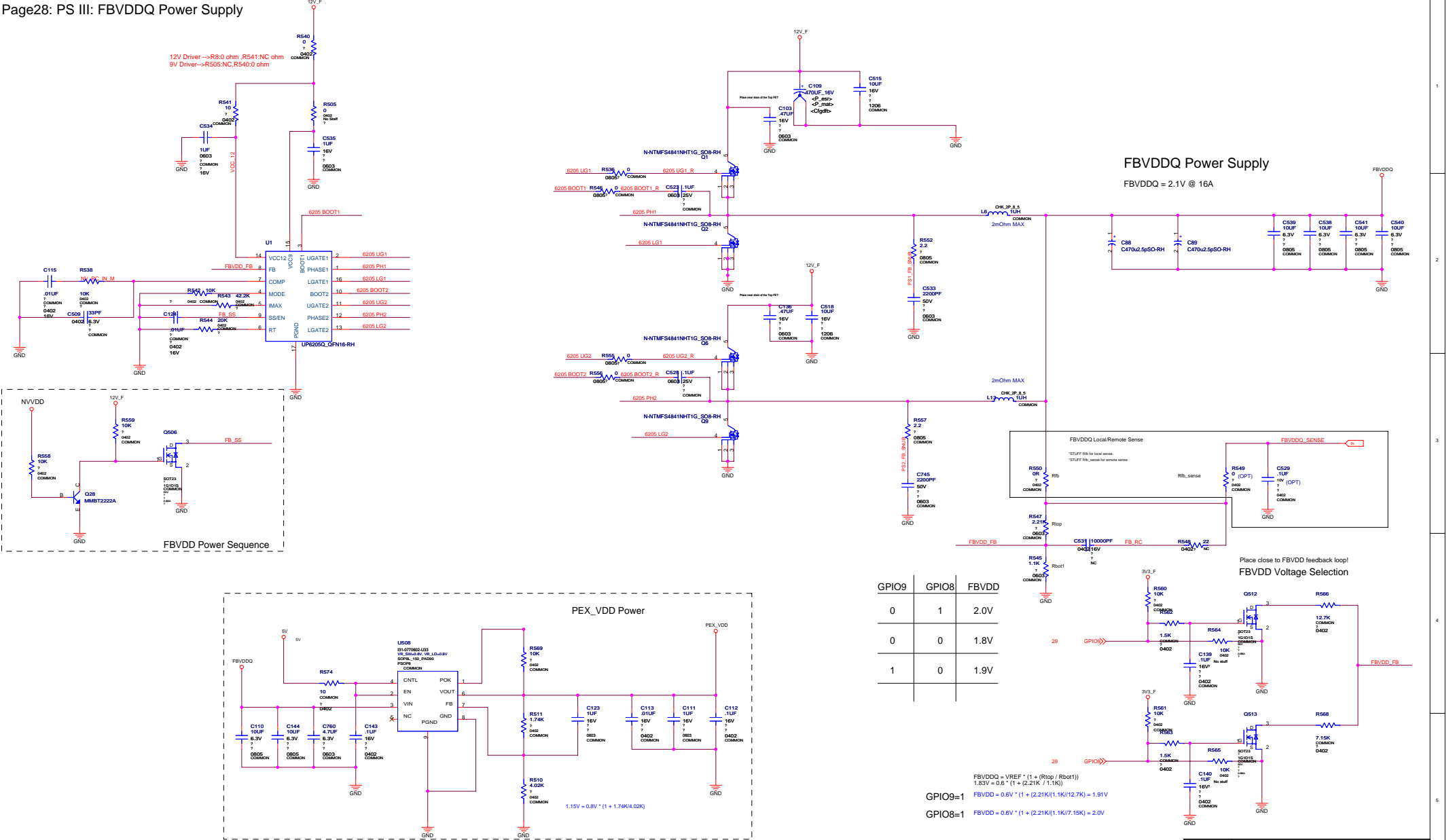


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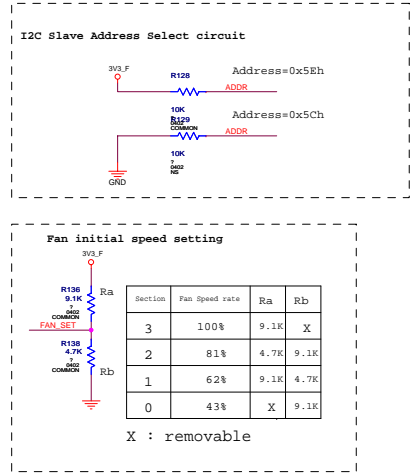
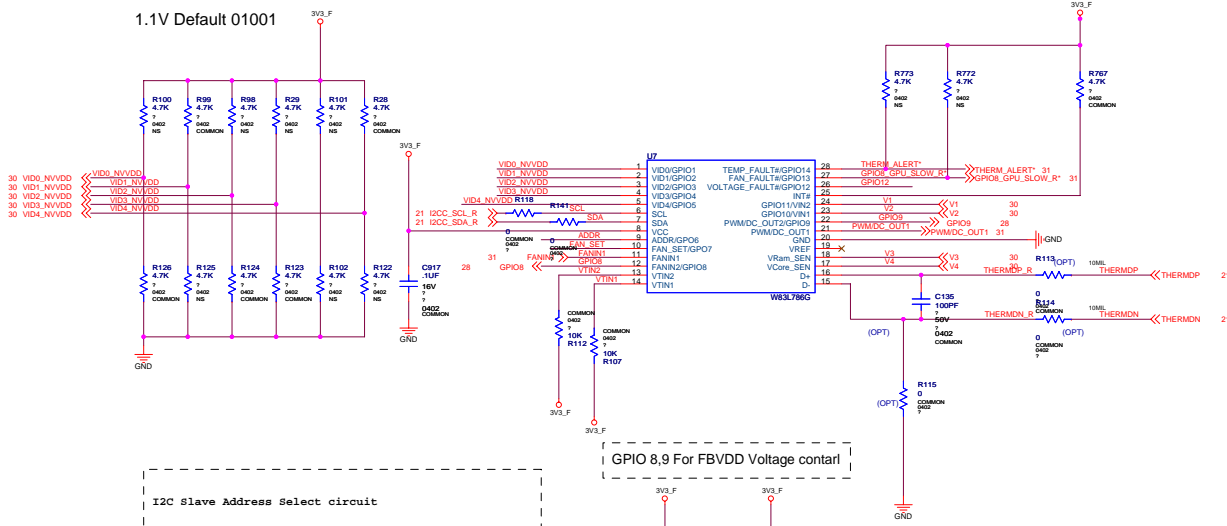
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Date: Tuesday, April 22, 2008 1 Sheet 24 of 38



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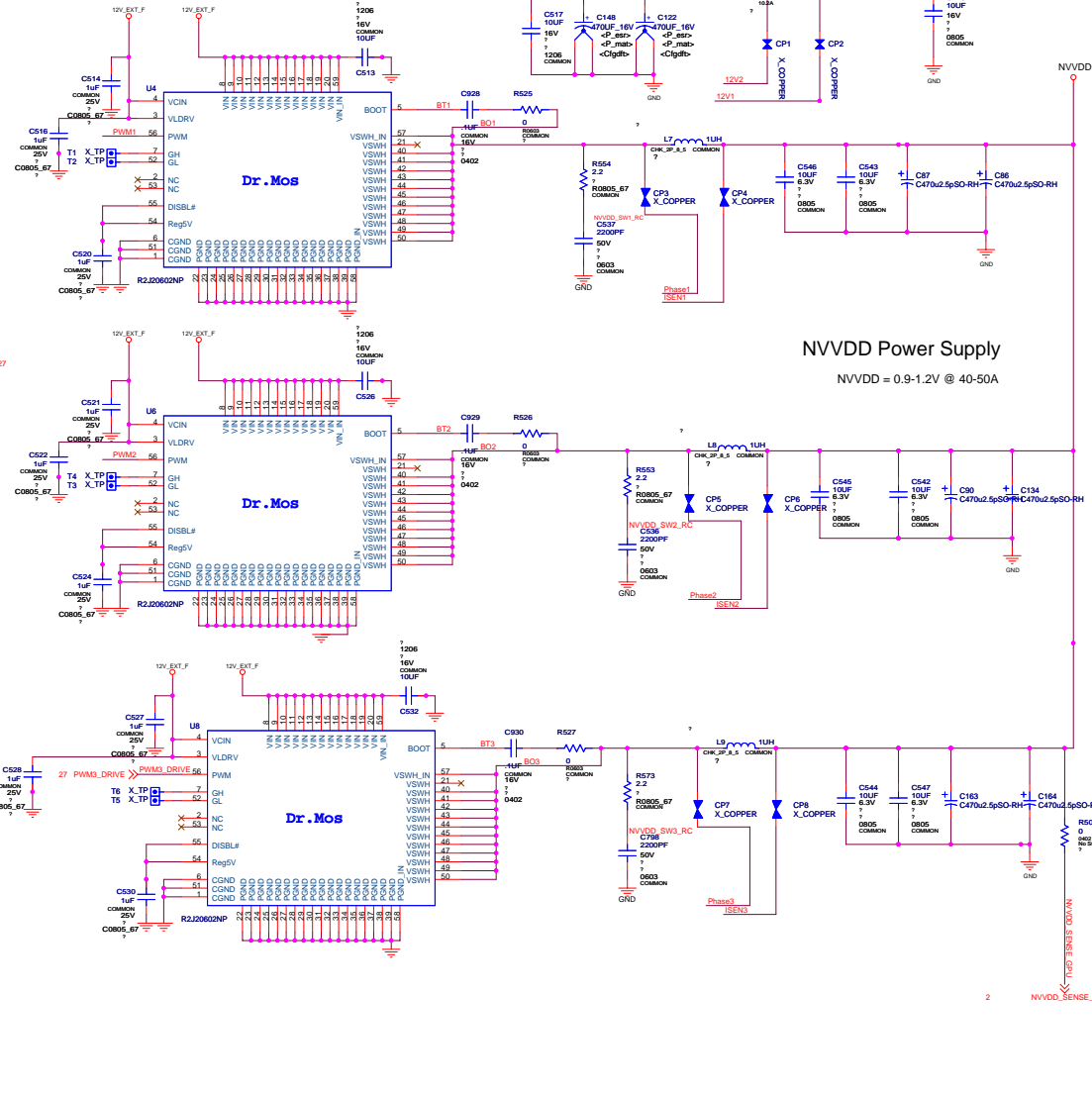
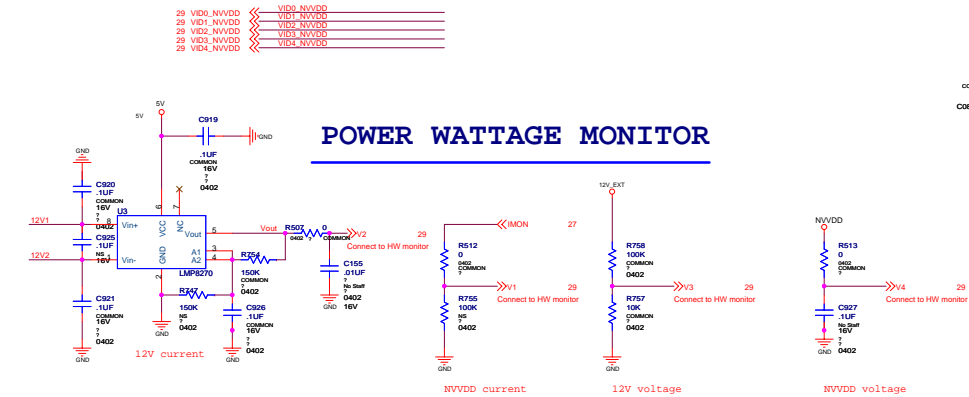
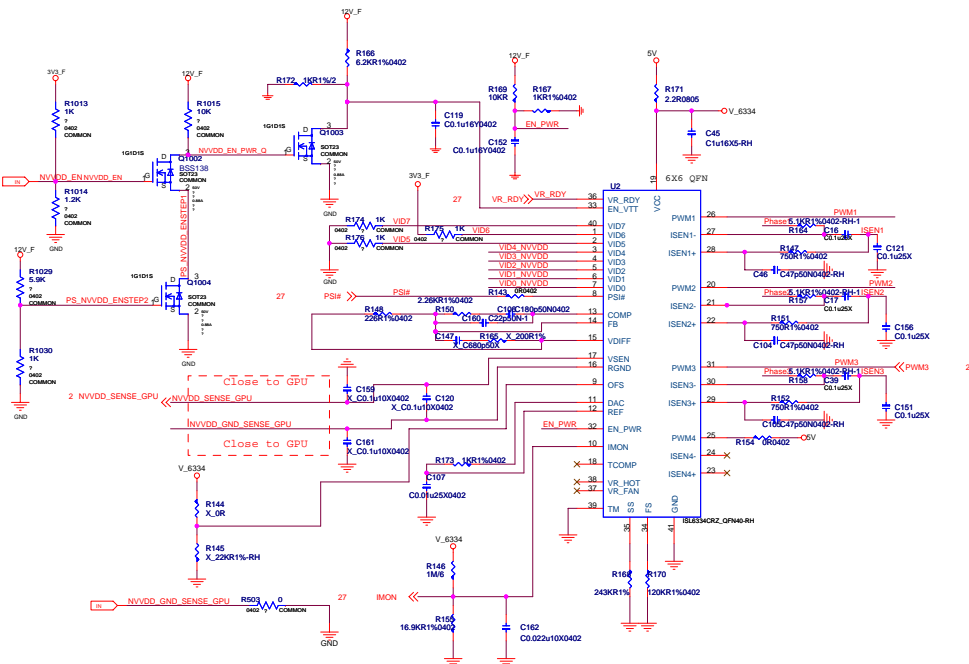
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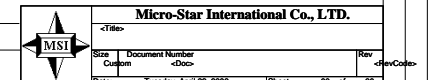
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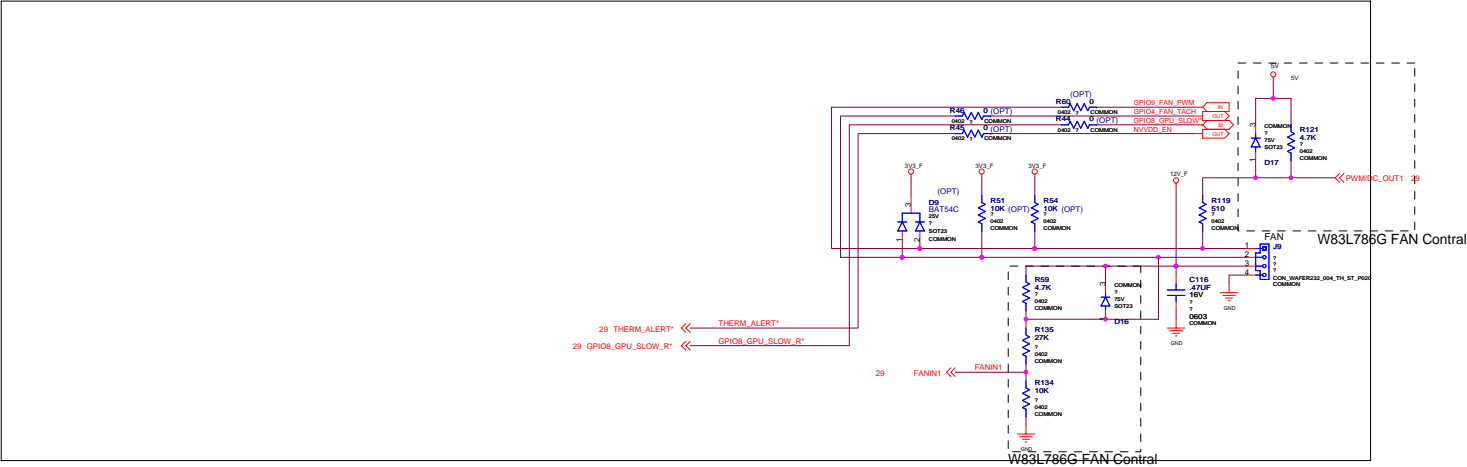


12V1, 12V2 trace length不可拉太長,
LMV772MAX放在near PWM IC

ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS V: NVDD Power Supply



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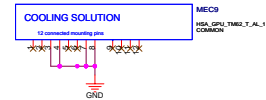
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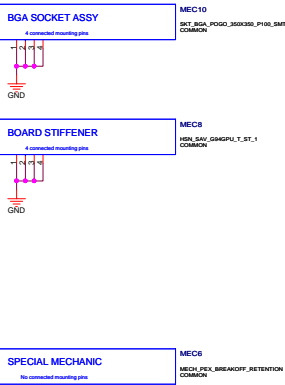
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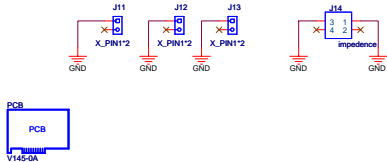
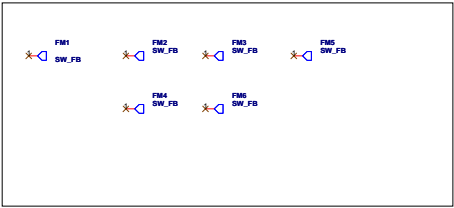
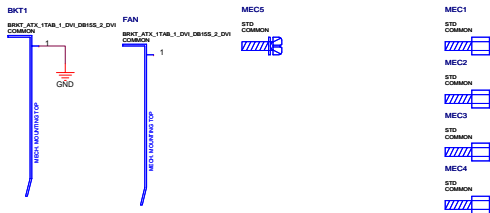
Thermal



Mechanical



Bracket



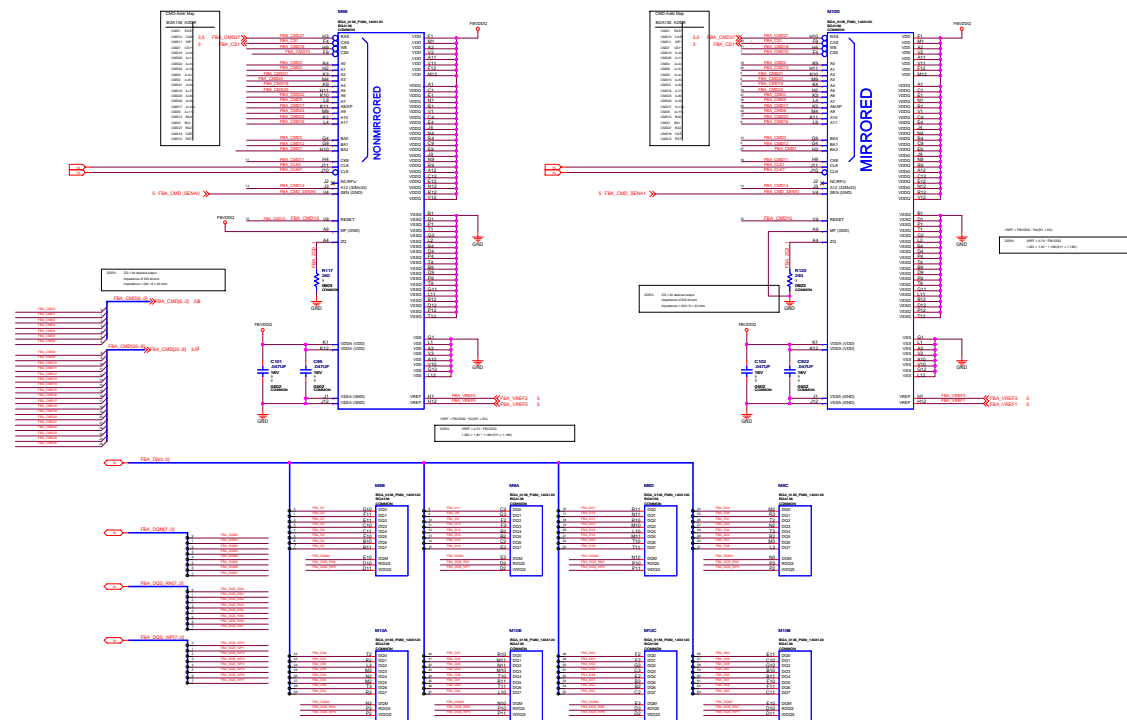
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ASSEMBLY
PAGE DETAIL
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Thermal, Mechanical, and Bracket

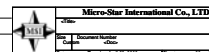
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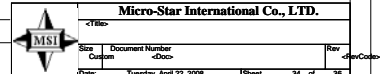
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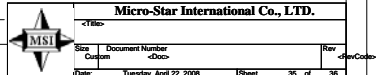
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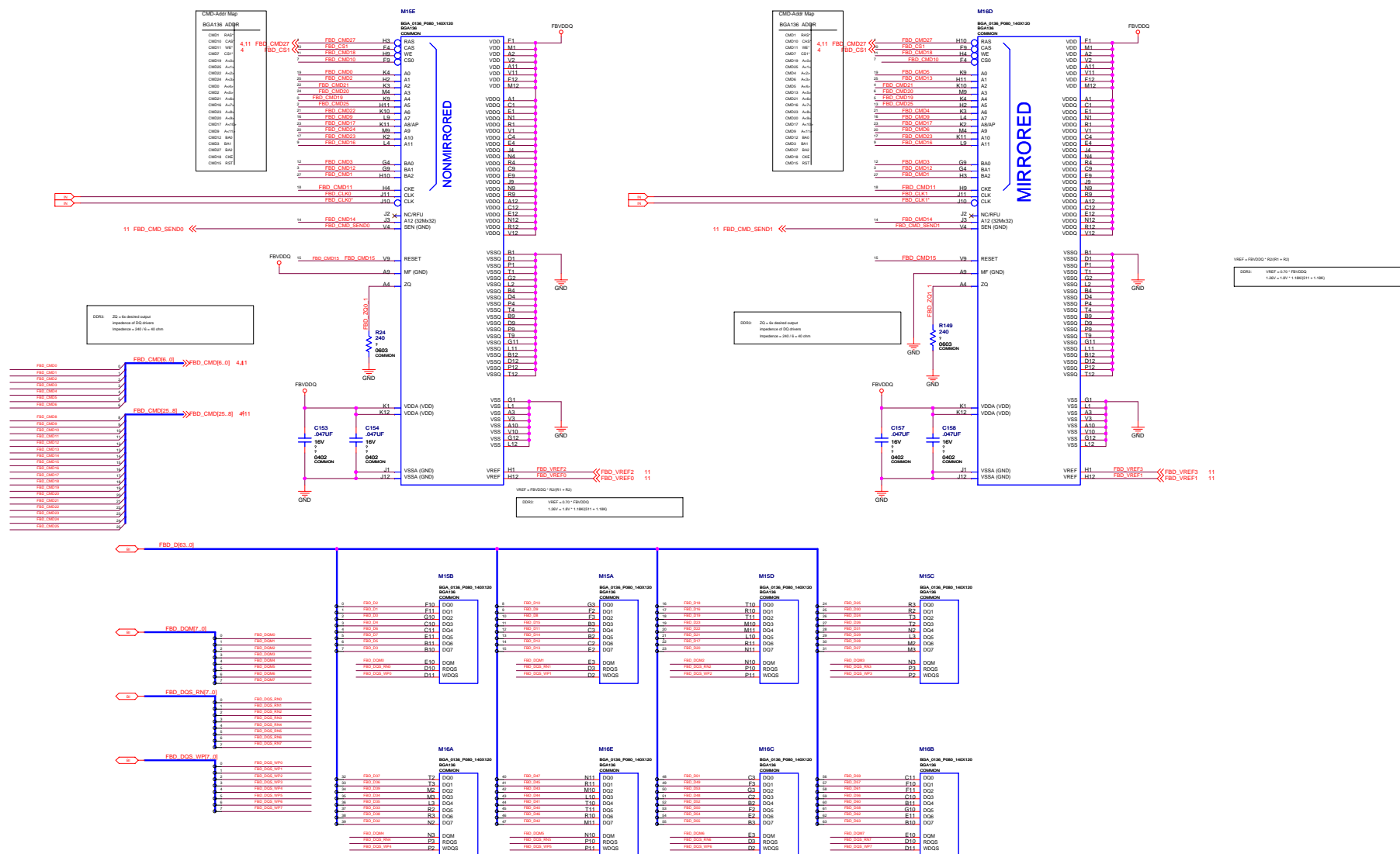


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ASSEMBLY	PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBO Partition



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