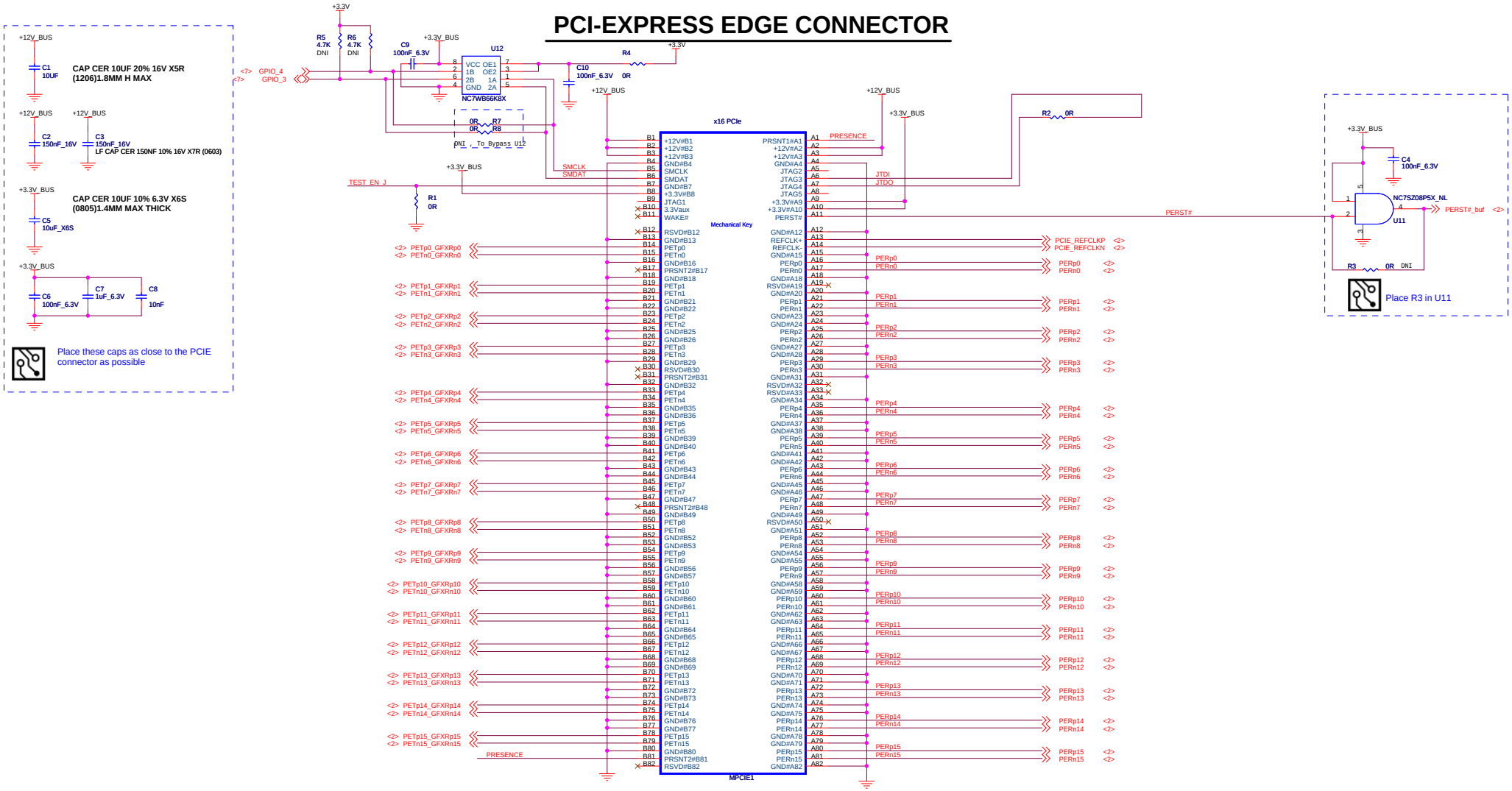
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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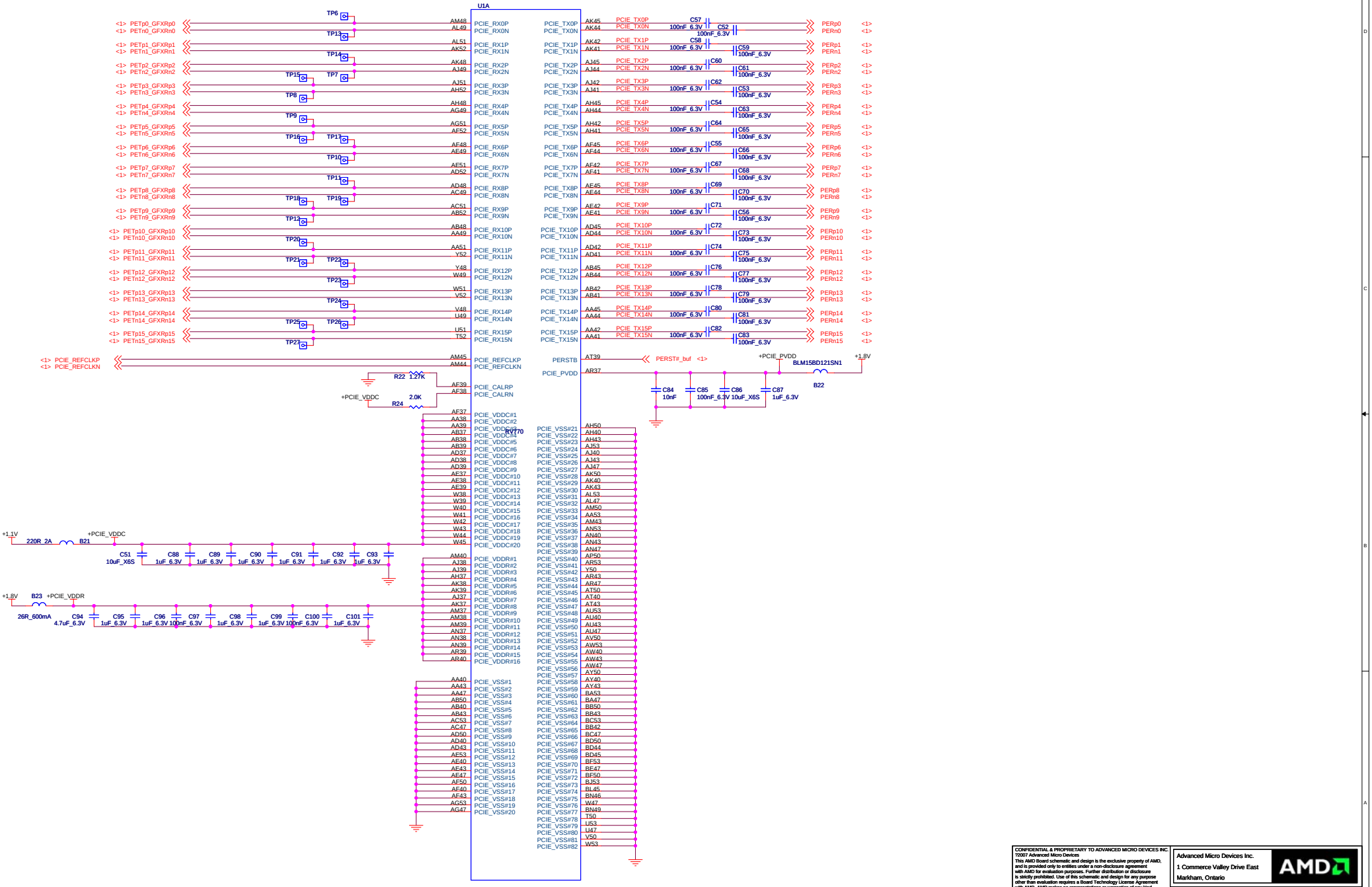
NOTE: some of the PCIE testpoints will
be available trought via on traces.



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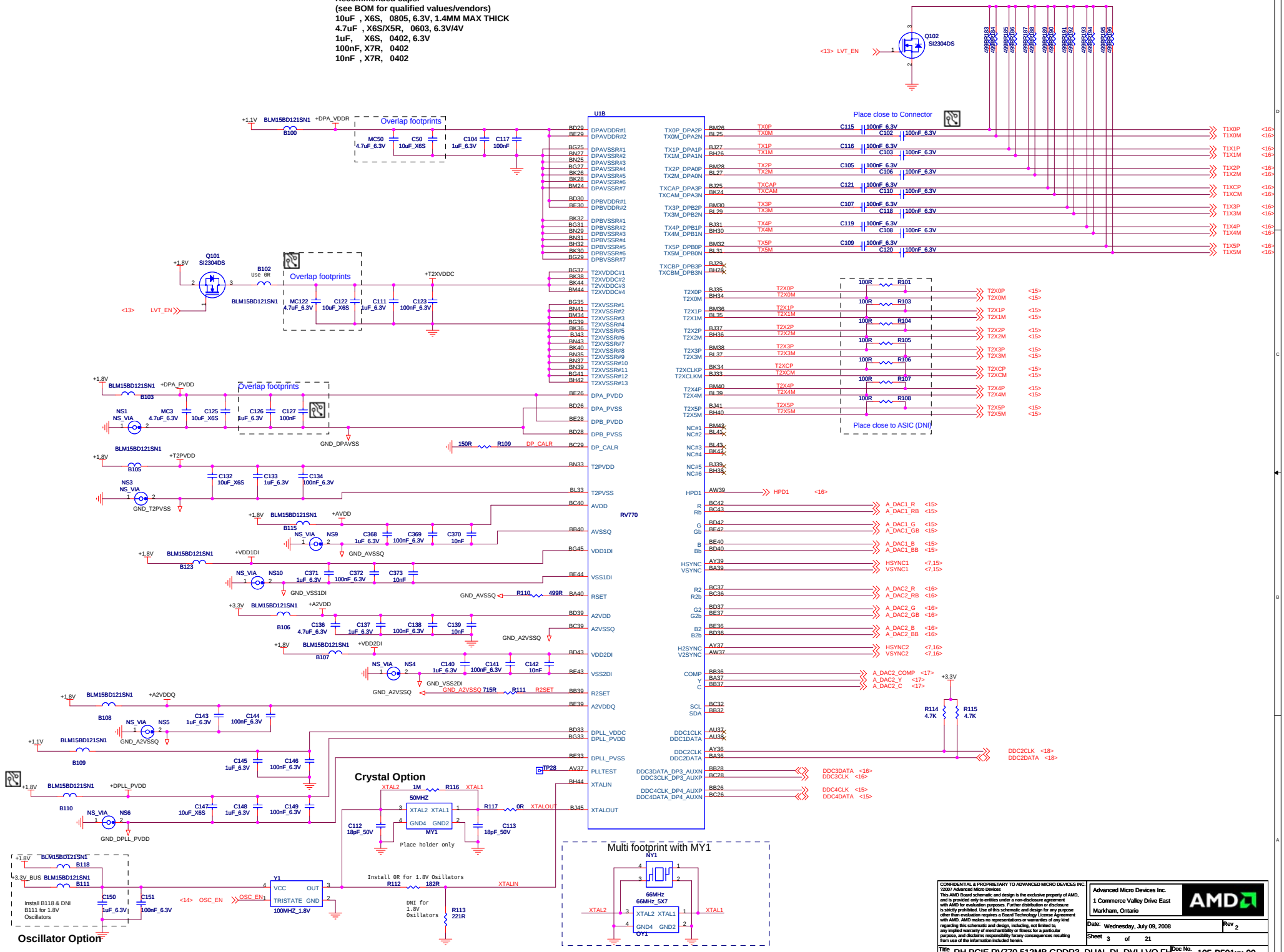
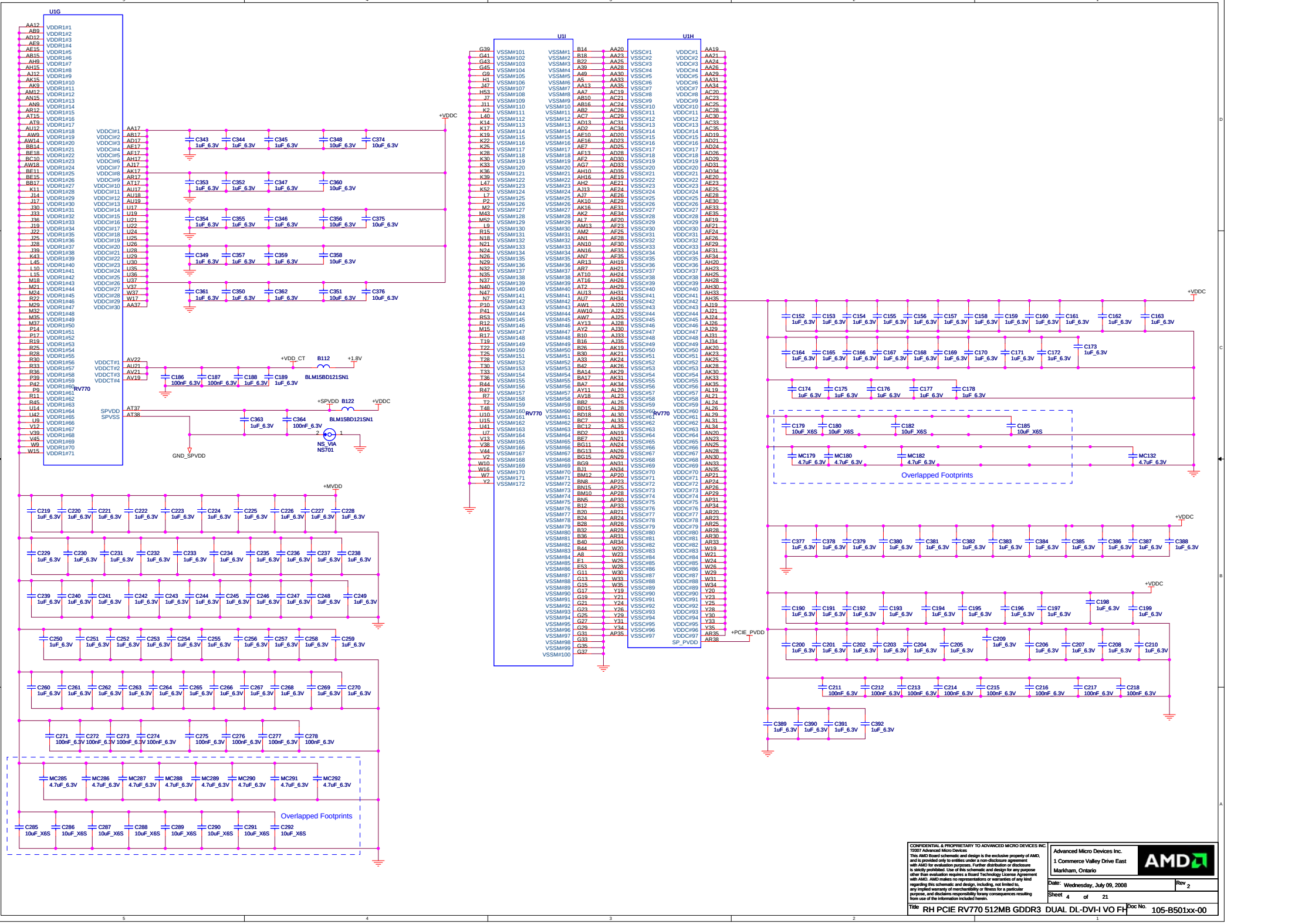
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402





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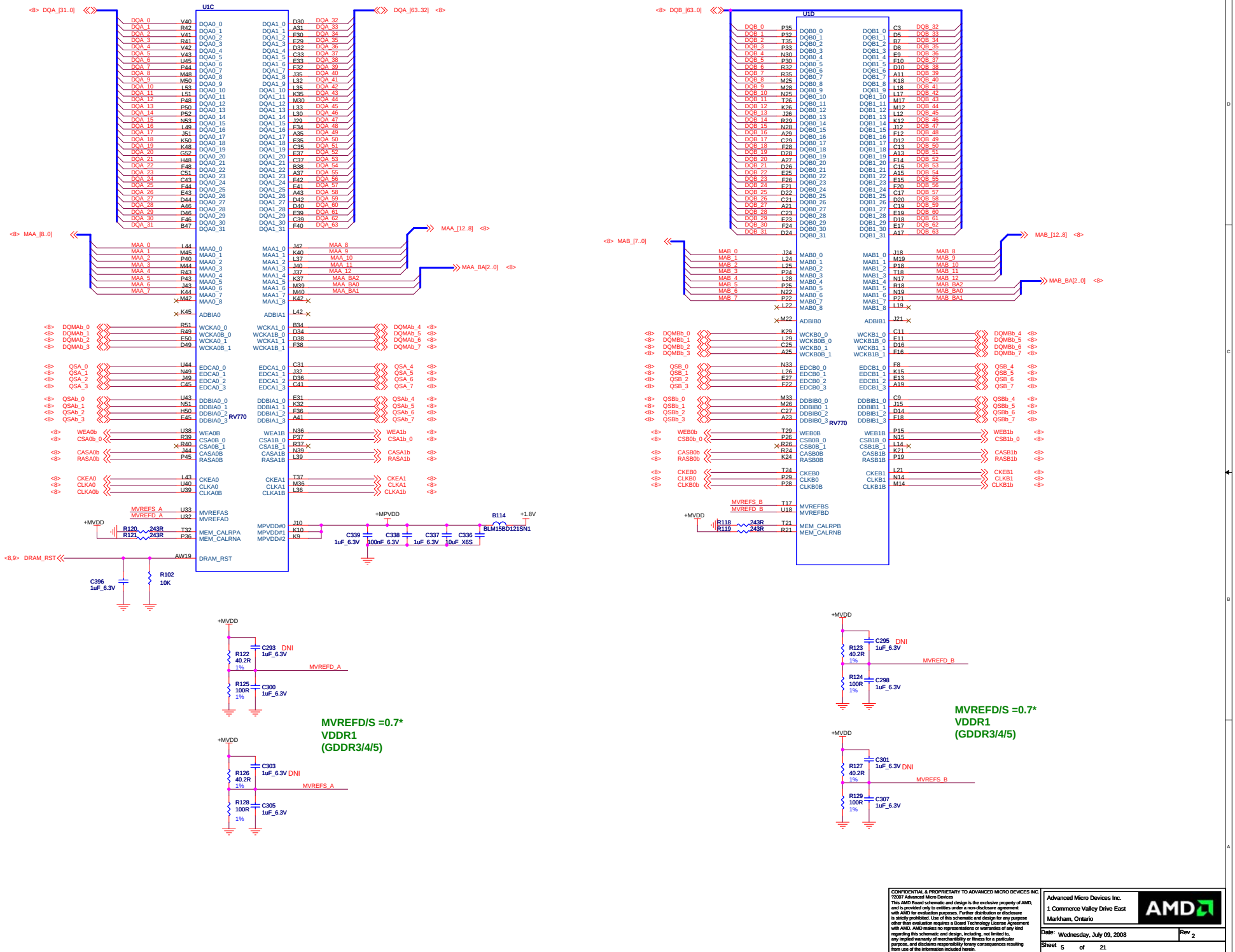

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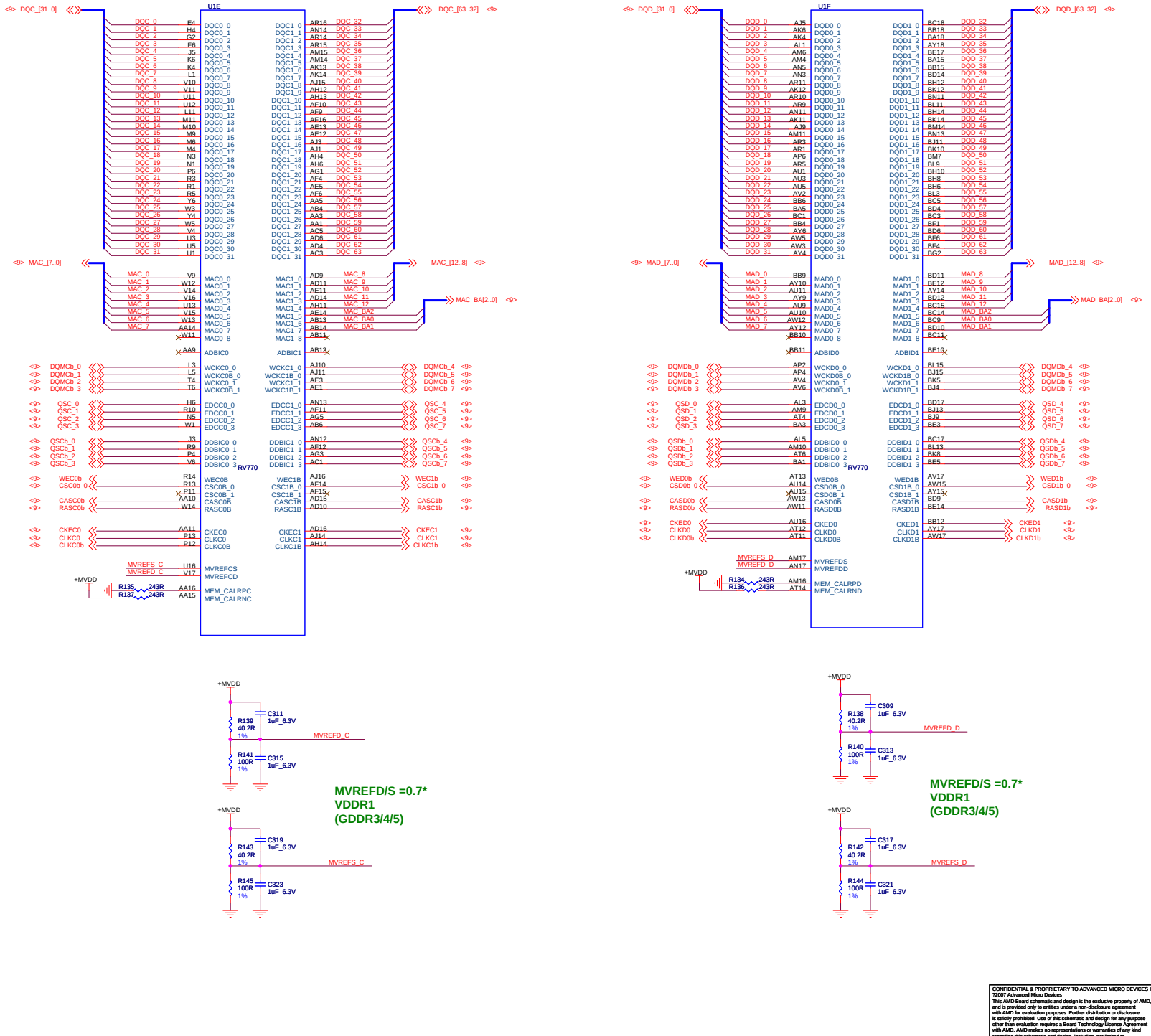

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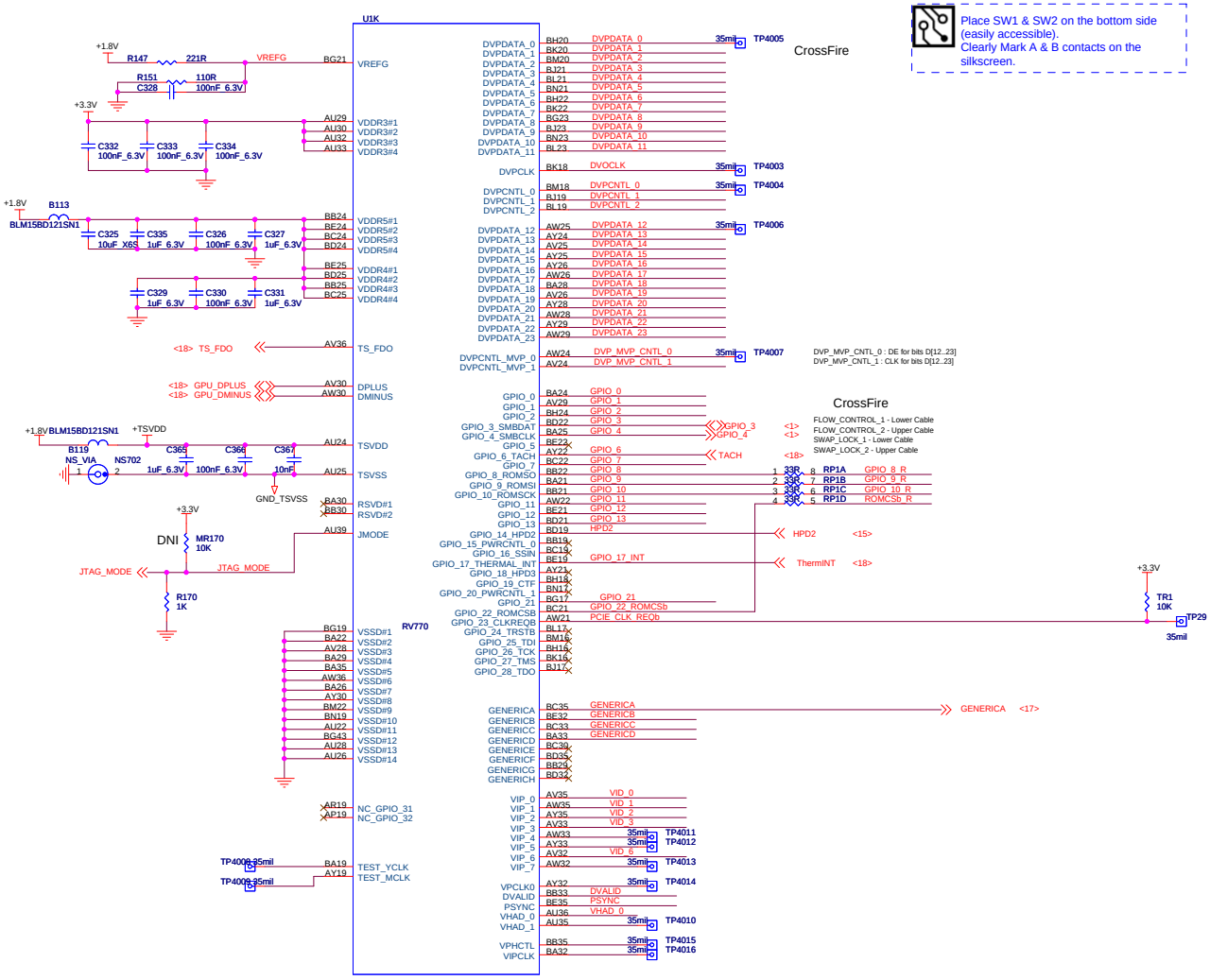
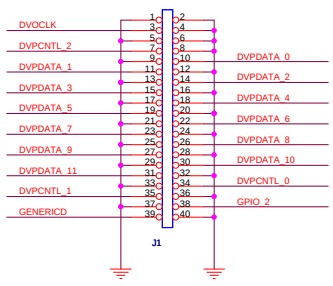
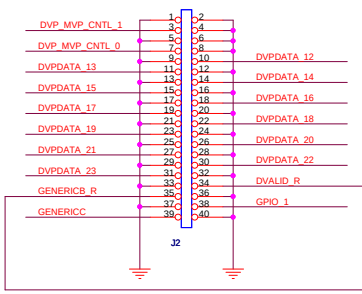


CrossFire Card-Edge

Lower Cable Card Edge



Upper Cable Card Edge



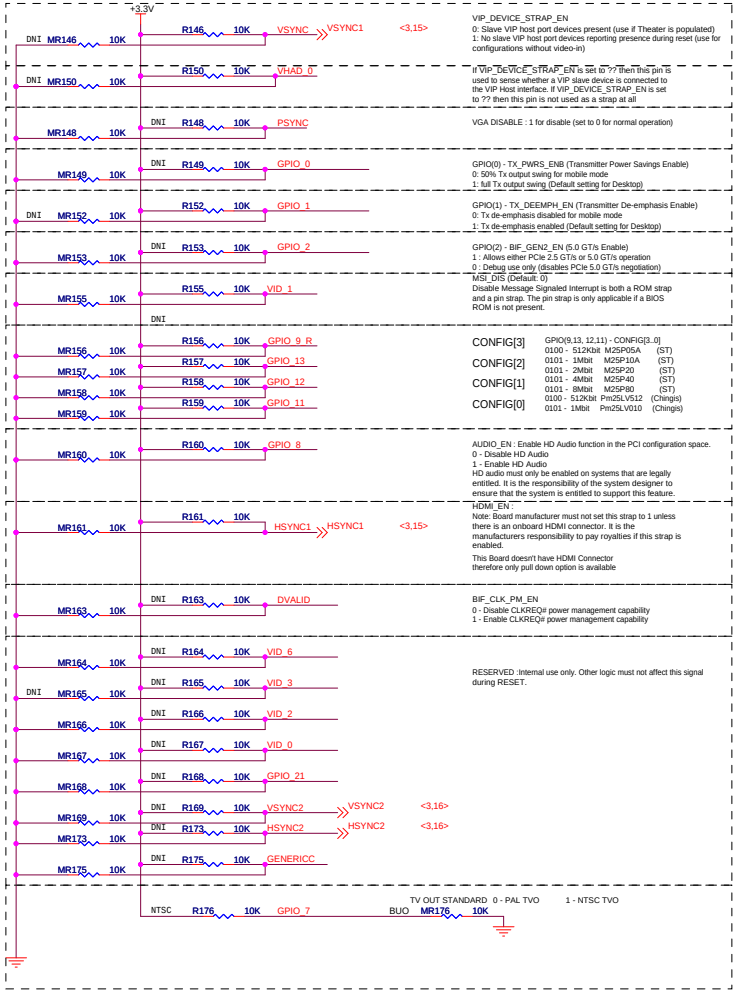
Bundle B

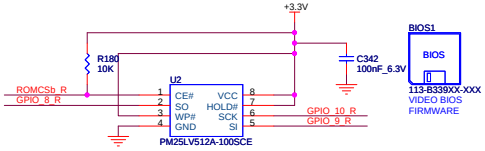
Bundle A (closer to the bracket)

DNI
R181 0R DVALID
R182 0R GENERICB

GENERICB: Generic I2C_SDA
DVALID: Generic I2C_SCL

PIN BASED STRAPS





PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

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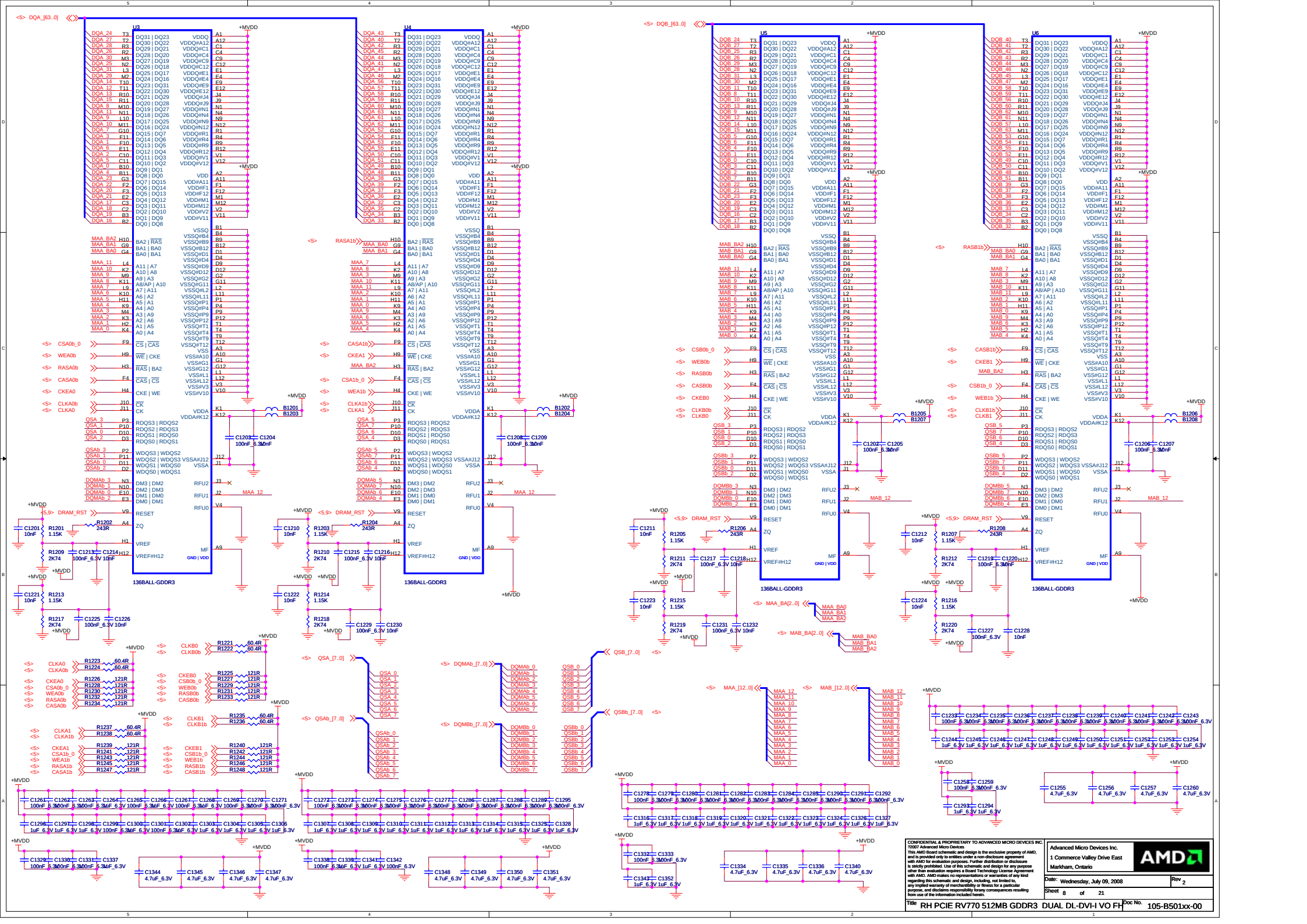
U3
U4
U5
U6
136BALL-GDDR3
DQA_24 DQA_27 DQA_28 DQA_26 DQA_30 DQA_25 DQA_31 DQA_29 DQA_26 DQA_25 DQA_24 DQA_23 DQA_22 DQA_15 DQA_8 DQA_11 DQA_9 DQA_10 DQA_7 DQA_3 DQA_54 DQA_1 DQA_6 DQA_2 DQA_5 DQA_0 DQA_4 DQA_23 DQA_22 DQA_20 DQA_21 DQA_17 DQA_18 DQA_19 DQA_16
DQA_43 DQA_40 DQA_42 DQA_45 DQA_44 DQA_41 DQA_47 DQA_46 DQA_56 DQA_57 DQA_58 DQA_59 DQA_60 DQA_63 DQA_61 DQA_62 DQA_52 DQA_53 DQA_55 DQA_50 DQA_51 DQA_49 DQA_48 DQA_38 DQA_39 DQA_37 DQA_36 DQA_32 DQA_35 DQA_34 DQA_33
DQB_24 DQB_27 DQB_25 DQB_26 DQB_28 DQB_31 DQB_30 DQB_29 DQB_8 DQB_10 DQB_13 DQB_9 DQB_12 DQB_14 DQB_15 DQB_6 DQB_5 DQB_4 DQB_1 DQB_0 DQB_3 DQB_2 DQB_21 DQB_23 DQB_20 DQB_19 DQB_16 DQB_17 DQB_18
DQB_40 DQB_41 DQB_42 DQB_43 DQB_44 DQB_46 DQB_45 DQB_47 DQB_58 DQB_59 DQB_56 DQB_60 DQB_61 DQB_57 DQB_63 DQB_53 DQB_54 DQB_55 DQB_52 DQB_49 DQB_50 DQB_48 DQB_51 DQB_39 DQB_37 DQB_38 DQB_36 DQB_33 DQB_34 DQB_35 DQB_32
MAA_BA2 MAA_BA1 MAA_BA0 MAA_11 MAA_10 MAA_9 MAA_8 MAA_7 MAA_6 MAA_5 MAA_4 MAA_3 MAA_2 MAA_1 MAA_0
MAB_BA2 MAB_BA1 MAB_BA0 MAB_11 MAB_10 MAB_9 MAB_8 MAB_7 MAB_6 MAB_5 MAB_4 MAB_3 MAB_2 MAB_1 MAB_0
CSA0b_0 WEA0b RASA0b CASA0b CKEA0 CLKA0b CLKA0
CSB0b_0 WEB0b RASB0b CASB0b CKEB0 CLKB0b CLKB0
CASA1b CKEA1 CSA1b_0 WEA1b CLKA1b CLKA1
CASB1b CKEB1 CSB1b_0 WEB1b CLKB1b CLKB1
QSA_3 QSA_1 QSA_0 QSA_2 QSA_7 QSA_6 QSA_4 QSA_5
QSB_3 QSB_1 QSB_0 QSB_2 QSB_5 QSB_7 QSB_6 QSB_4
QSAb_3 QSAb_1 QSAb_0 QSAb_2 QSAb_7 QSAb_6 QSAb_4 QSAb_5
QSBb_3 QSBb_1 QSBb_0 QSBb_2 QSBb_5 QSBb_7 QSBb_6 QSBb_4
DQMA_3 DQMA_1 DQMA_0 DQMA_2 DQMA_7 DQMA_6 DQMA_4 DQMA_5
DQMB_3 DQMB_1 DQMB_0 DQMB_2 DQMB_5 DQMB_7 DQMB_6 DQMB_4
DRAM_RST
MAA_12 MAA_[12..0] MAA_[2..0]
MAB_12 MAB_[12..0] MAB_[2..0]
DQA_[63..0] DQB_[63..0]
QSA_[7..0] QSAb_[7..0] QSB_[7..0] QSBb_[7..0]
DQMA_[7..0] DQMAb_[7..0] DQMB_[7..0] DQMBb_[7..0]
+MVDD
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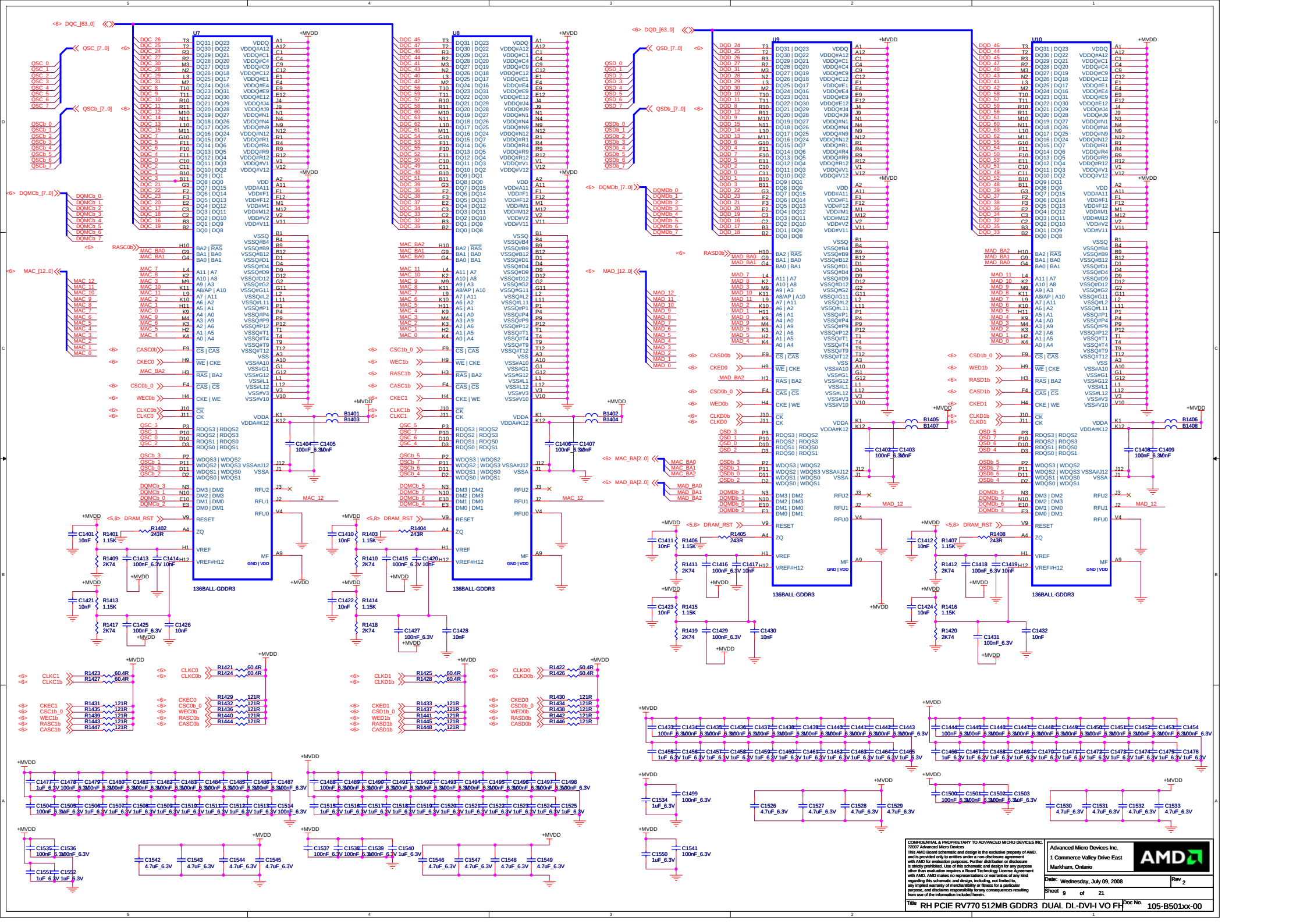
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U8
U9
U10
136BALL-GDDR3
DQC_[63..0]
QSC_[7..0]
QSCb_[7..0]
DQMC_[7..0]
MAC_[12..0]
DQD_[63..0]
QSD_[7..0]
QSDb_[7..0]
DQMD_[7..0]
MAD_[12..0]
+MVDD
DRAM_RST
RASC0b
CASC0b
CKEC0
WEC0b
CLKC0b
CLKC0
RASD0b
CASD0b
CKED0
WED0b
CLKD0b
CLKD0
RASC1b
CASC1b
CKEC1
WEC1b
CLKC1b
CLKC1
RASD1b
CASD1b
CKED1
WED1b
CLKD1b
CLKD1
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MAD_BA[2..0]
MAC_12
MAD_12
B1401
B1402
B1403
B1404
B1405
B1406
B1407
B1408
C1401
C1402
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R1443
R1444
R1445
R1446
R1447
R1448
243R
1.15K
2K74
60.4R
121R
10nF
100nF_6.3V
1uF_6.3V
4.7uF_6.3V
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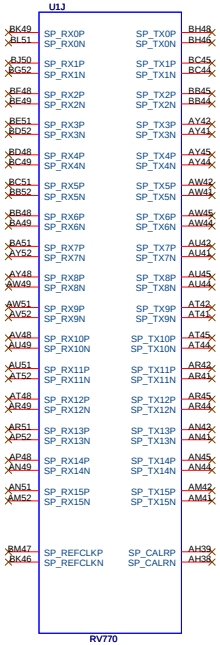

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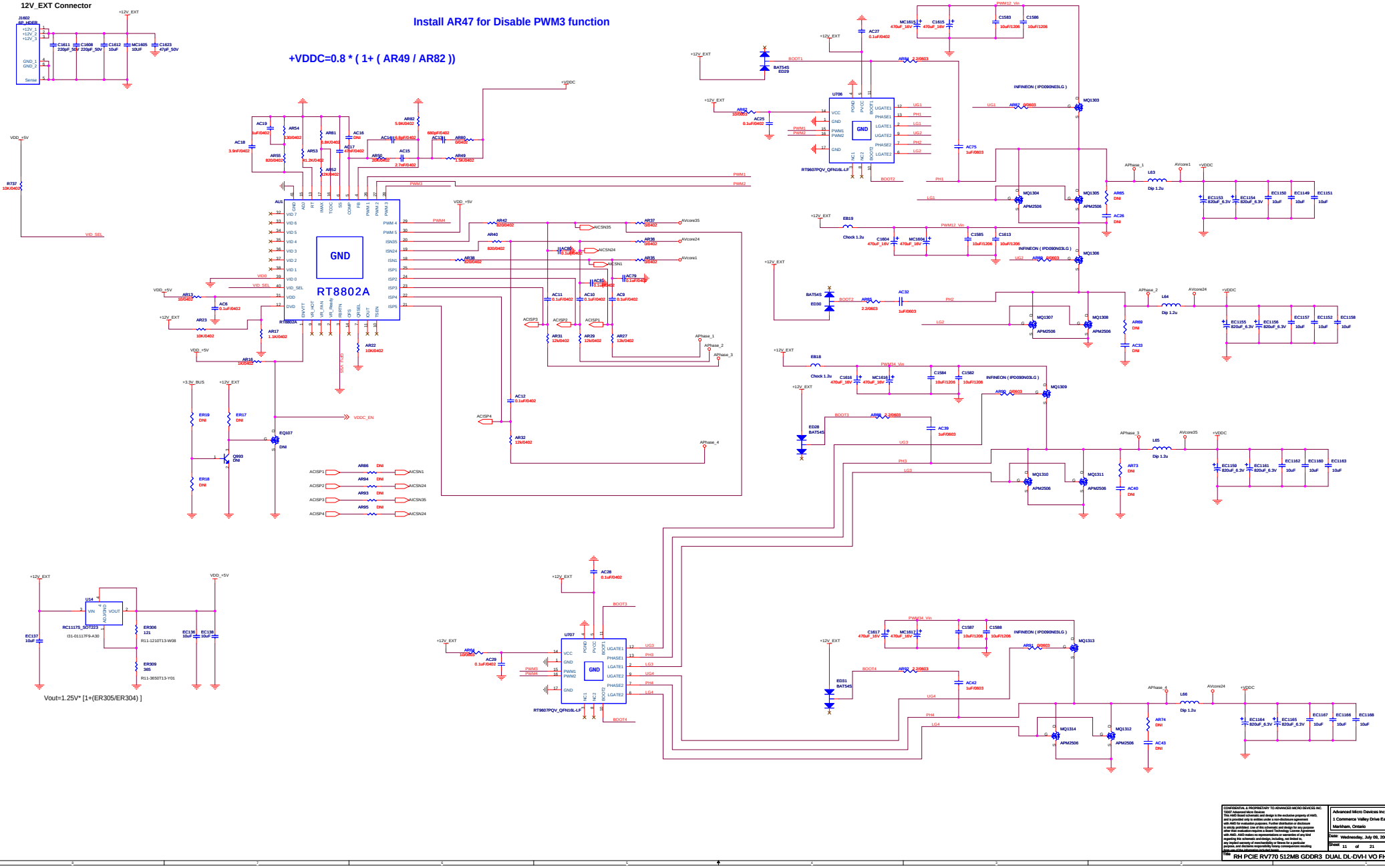
12V_EXT Connector

Install AR47 for Disable PWM3 function

+VDDC=0.8 * (1+ (AR49 / AR82))



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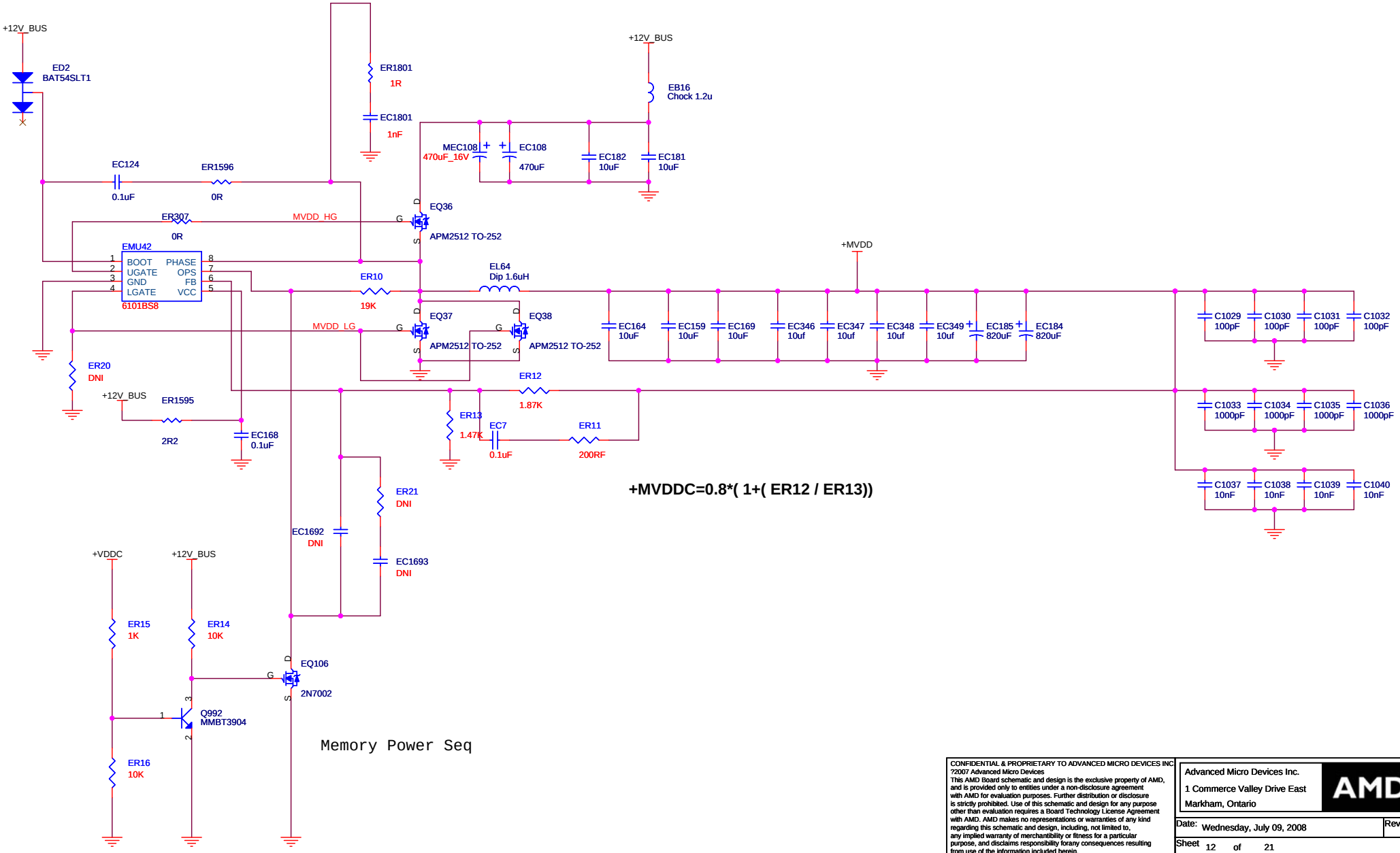

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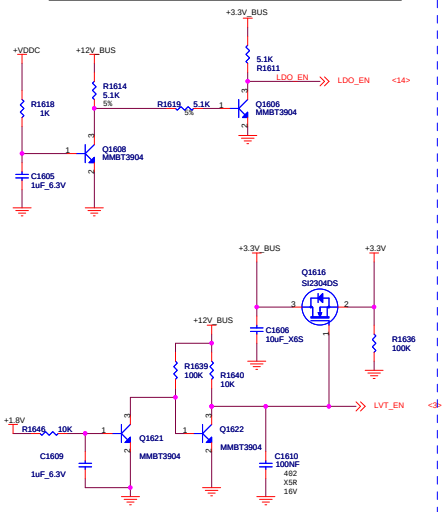
Power up Sequencing



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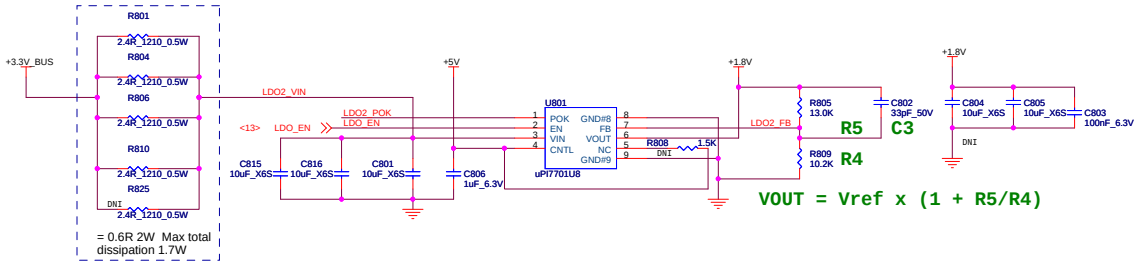
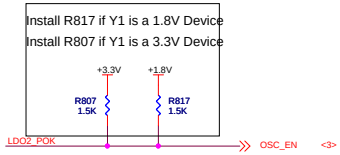
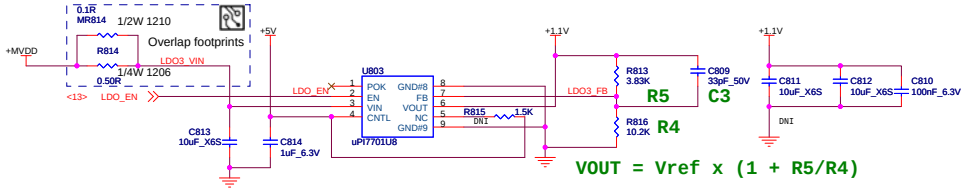
Regulators for +5V

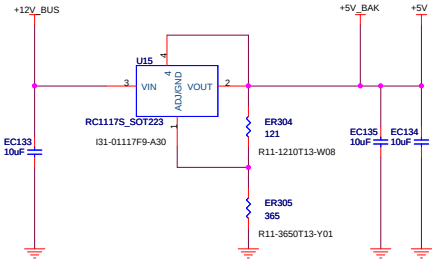
LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 1.7A (TBV) RMS MAX
PCB: Min 70mm sq. copper area for cooling



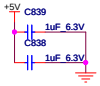


LDO #3: Vin = +1.50V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX
PCB: Min 70mm sq. copper area for cooling





Vout=1.25V* [1+(ER305/ER304)]



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See BOM for qualified filters

<3> A_DAC1_R — R1001 75R 402 — C1004 8.0pF 402 — L1001 47nH / ML1001 36NH — C1001 12pF_50V 402
R1027 37.4R
<3> A_DAC1_RB
<3> A_DAC1_G — R1002 75R 402 — C1005 8.0pF 402 — L1002 47nH / ML1002 36NH — C1002 12pF_50V 402
R1028 37.4R
<3> A_DAC1_GB
<3> A_DAC1_B — R1003 75R 402 — C1006 8.0pF 402 — L1003 47nH / ML1003 36NH — C1003 12pF_50V 402
R1029 37.4R
<3> A_DAC1_BB

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

L100x and ML100x footprints are overlapped

For ESD Protection

D1001 CM1213-04 (+3.3V) — D1002 CM1213-04 (+5V_VESA)

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

+5V_VESA2 — +5V_VESA — +5V — EF1 0.2A

C1010 68pF 603

MJ1001 G3179C219-005

MJ1001	
1	R
2	G
3	B
11	MS0
12	MS1
4	MS2
15	MS3
9	NC
13	HS
14	VS
5	VSS
6	VSS#6
7	VSS#7
8	VSS#8
10	VSS#10
16	CASE
17	CASE#17

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

<3> DDC4DATA — +5V — R1005 2.2K — DDCDATA_DAC1_5V — R1006 33R 402 — DDCDATA_DAC1_R
<3> DDC4CLK — +5V — R1008 2.2K — DDCCLK_DAC1_5V — R1009 33R 402 — DDCCLK_DAC1_R

<3,7> HSYNC1 — C1999 100nF 6.3V — U1999A 74VHC125 — HSYNC_DAC1_B — R1010 10R 402 — HSYNC_DAC1_R
<3,7> VSYNC1 — 74VHC125 U1999B — VSYNC_DAC1_B — R1011 10R 402 — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

+3.3V — Q1021 MMBT3904 — R1022 10K — HPD_DVI2 — <7> HPD2 — R1023 10K

+5V_VESA — J1001 DVI_CONNECTOR

J1001			
25	CASE		
1	TMDS Data2-	<3>	T2X2M
2	TMDS Data2+	<3>	T2X2P
3	TMDS Data2/4 Shield		
4	TMDS Data4-	<3>	T2X4M
5	TMDS Data4+	<3>	T2X4P
6	DDC Clock	DDCCLK_DAC1_R	
7	DDC Data	DDCDATA_DAC1_R	
8	Analog VSYNC	VSYNC_DAC1_R	
9	TMDS Data1-	<3>	T2X1M
10	TMDS Data1+	<3>	T2X1P
11	TMDS Data1/3 Shield		
12	TMDS Data3-	<3>	T2X3M
13	TMDS Data3+	<3>	T2X3P
14	+5V Power		
15	GND (for +5V)		
16	Hot Plug Detect	HPD_DVI2	
17	TMDS Data0-	<3>	T2X0M
18	TMDS Data0+	<3>	T2X0P
19	TMDS Data0/5 Shield		
20	TMDS Data5-	<3>	T2X5M
21	TMDS Data5+	<3>	T2X5P
22	TMDS Clock Shield		
23	TMDS Clock+	<3>	T2XCP
24	TMDS Clock-	<3>	T2XCM
C1	Analog Red	A_R_DAC1_F	
C2	Analog Green	A_G_DAC1_F	
C3	Analog Blue	A_B_DAC1_F	
C4	Analog HYNC	HSYNC_DAC1_R	
C5	Analog GND		
C6	Analog GND#C6		
26	CASE#26		
27	CASE#27		
28	CASE#28		
29	CASE#29		
30	CASE#30		

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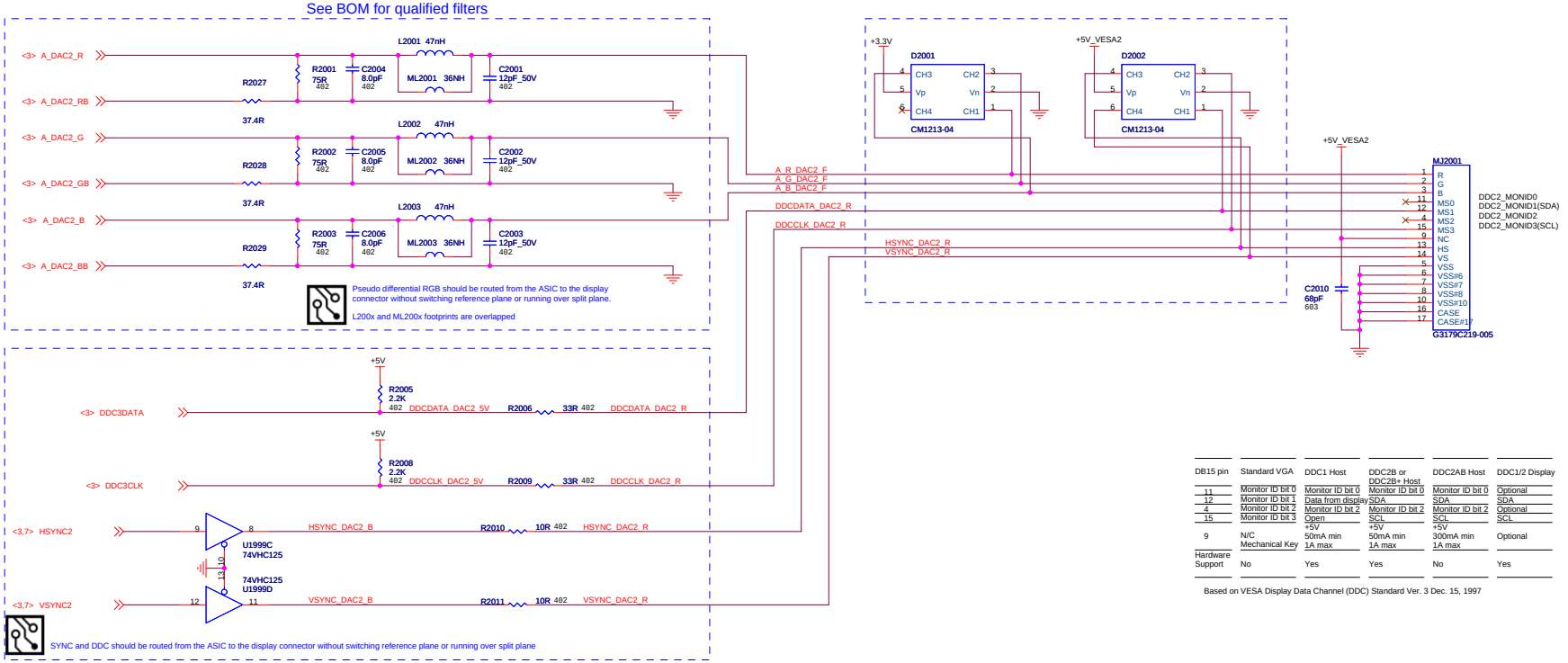
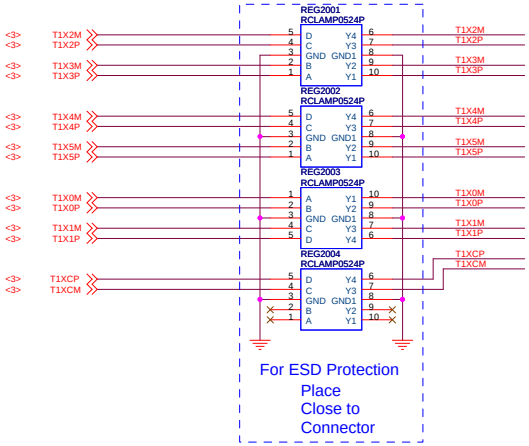
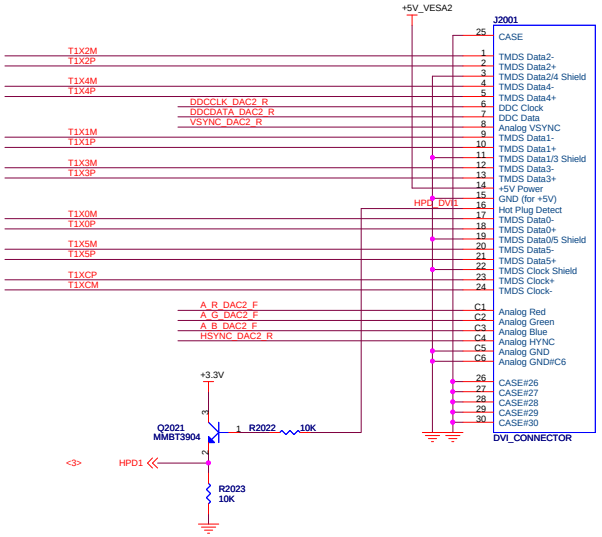
See BOM for qualified filters



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





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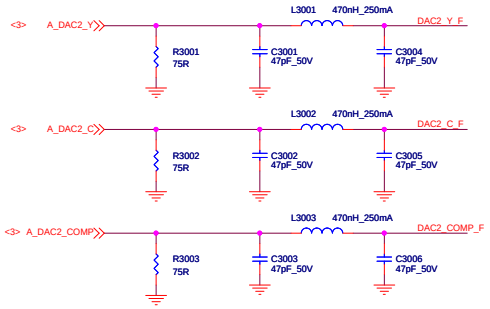

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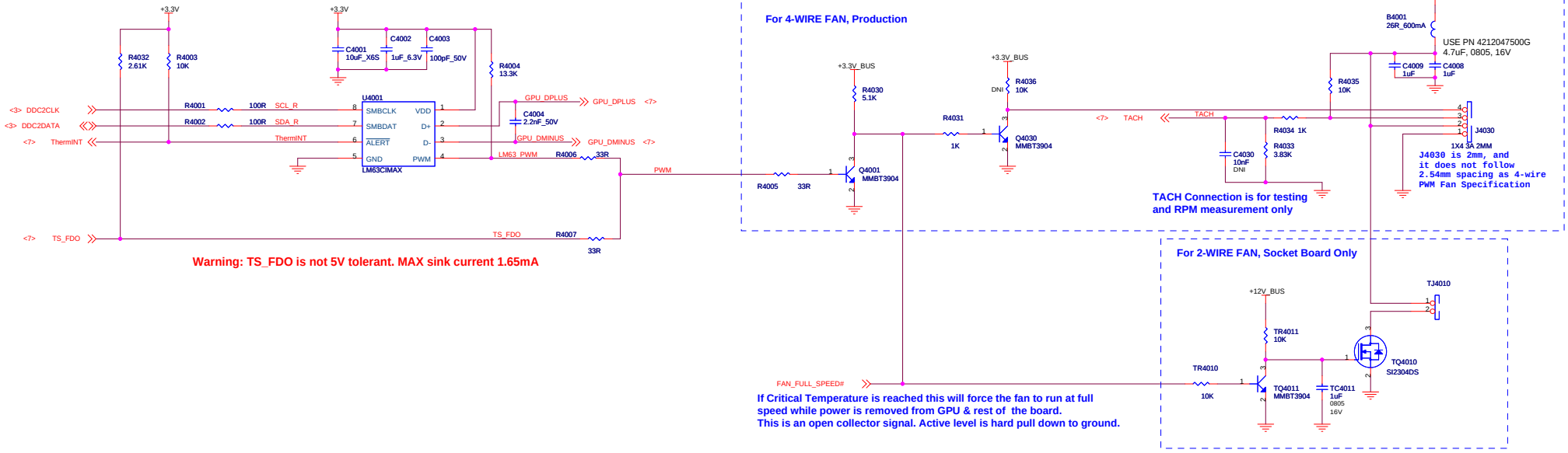

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ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

MT1
MT_Hole_0.136 TM 5.5 BM 7.0

PCB1
PCB
109-B33931-00A

ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET
80200386B0G

ASSY-SCREW5
SCREW
SCREW

BKT1: DS, DVI - DIN - DVI

BKT2
BRACKET
8020038600G

SK1
Socket_RV770

PCIE 12V/3.3V Power up Bonding support

VDDC1

MVDD1

TPC1

IOT1

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM4 SW_FB
FM5 SW_FB
FM6 SW_FB

J7 3 1 4 2 impedence

J4 3 1 4 2 impedence

J5 3 1 4 2 impedence

J8 3 1 4 2 impedence

J3 X_PIN1*2

J6 X_PIN1*2

J9 X_PIN1*2

J11 X_PIN1*2

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Title	Schematic No.	Date:
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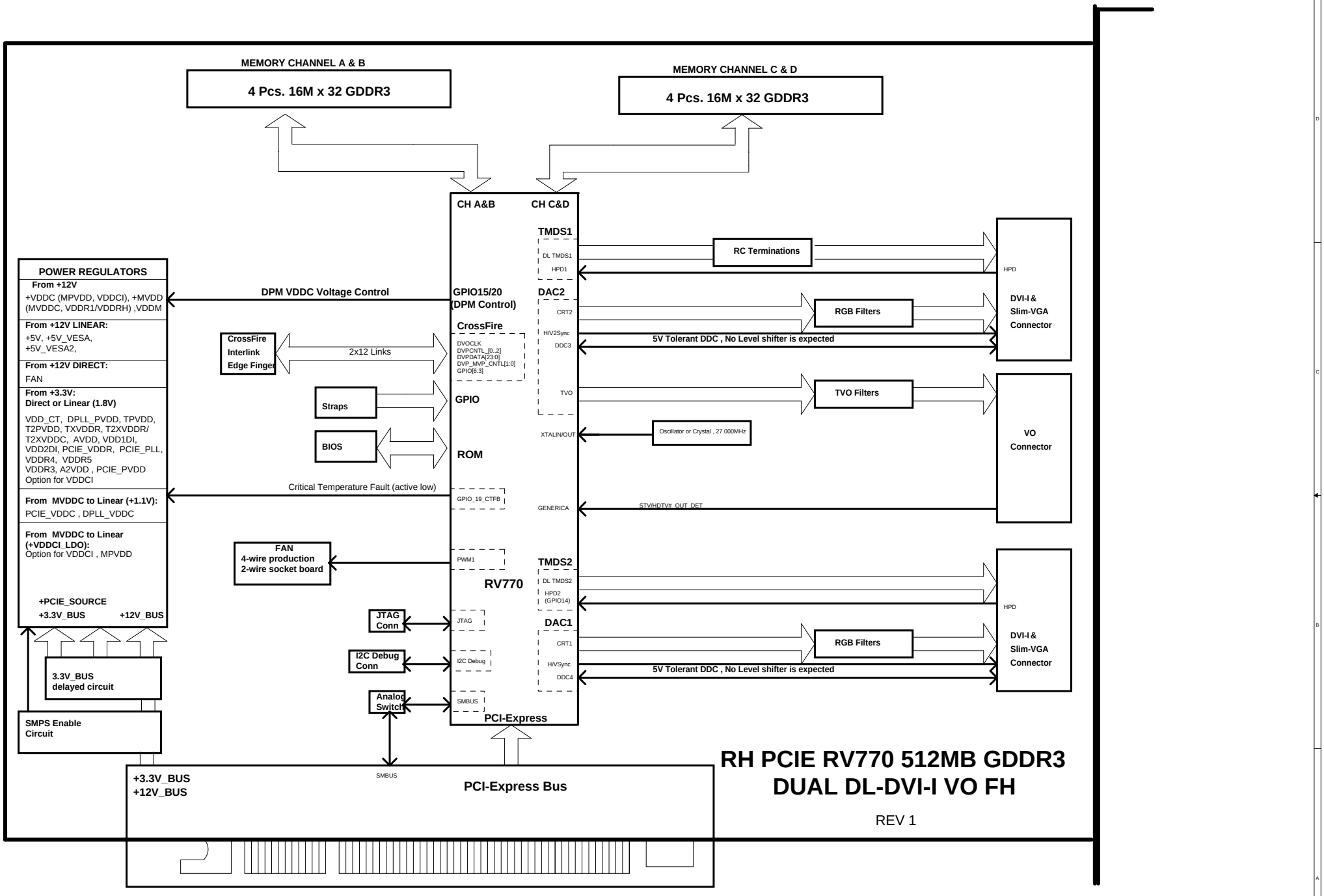
REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/10/11	Initial design for RV770 GDDR3
1	00B	08/02/25	Improvement: 1) Add 1 uF CAP on memory reset, Pg5 2) MVDDC current leakage board workaround; Pg13 3) MVDD Themal Protection, Pg 13 4) Improvement on Hot Plug protection Pg13 5) 12V_BUS & 12V_EXT Input Switch Circuit Page 13
2	00	08/03/27	1.Correct PTC comparator power connection. 2. Add Fuse NF1200 on page 13



RH PCIE RV770 512MB GDDR3
DUAL DL-DVI-I VO FH

REV 1

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