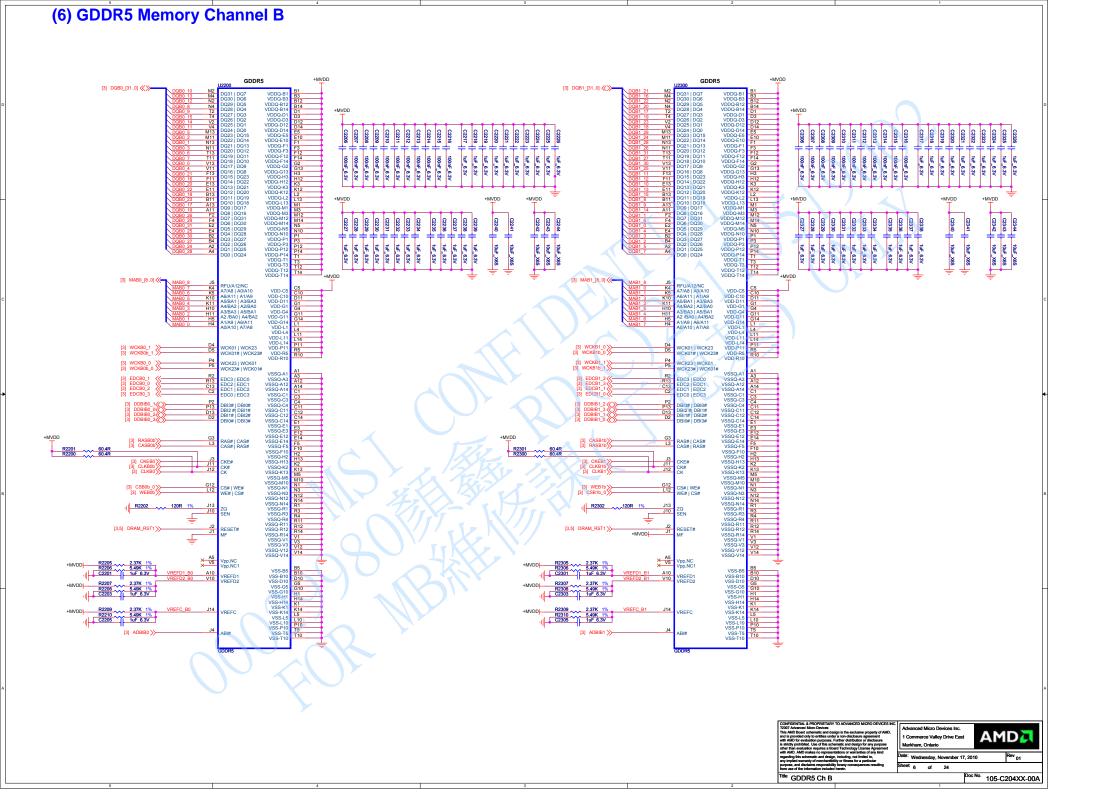
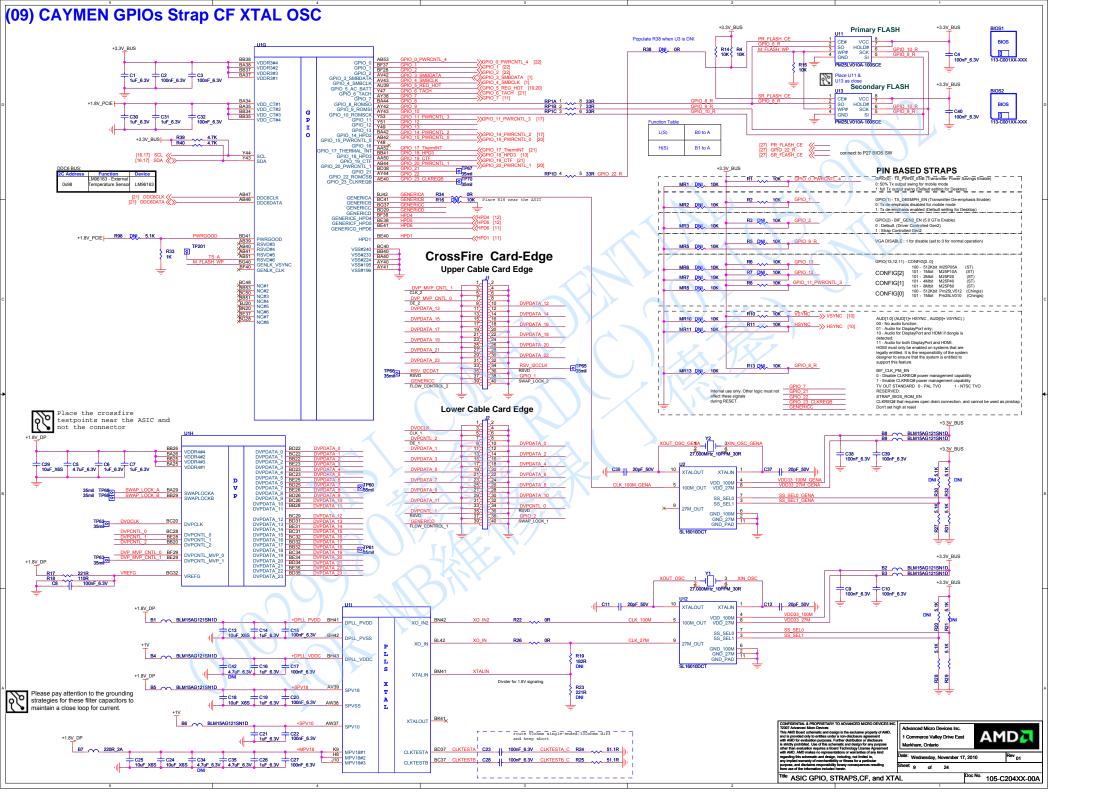


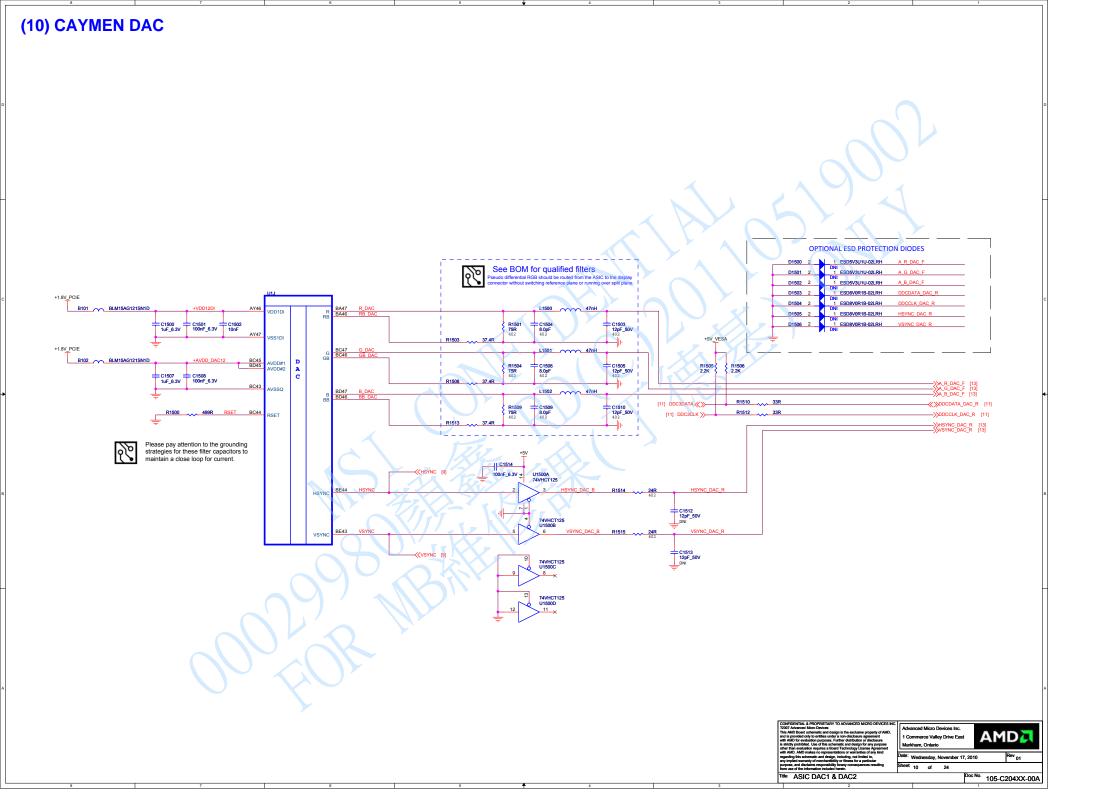
(5) GDDR5 Memory Channel A GDDR5 GDDR5 D030 | D06 D029 | D05 D029 | D05 D029 | D05 D029 | D05 D027 | D03 D026 | D02 D027 | D03 D026 | D02 D025 | D01 D024 | D00 D025 | D01 D024 | D00 D025 | D01 D024 | D00 D021 | D013 D020 | D012 D013 | D016 D021 | D013 D020 | D017 D030 | D016 D017 | D031 | D026 D017 | D031 | D026 D031 | D027 | D026 D031 | D027 | D026 D031 | D027 | D026 D031 | D026 VDDQ-E VDQ-E VDDQ-D: VDDQ-D: VDDQ-D: VDDQ-D: VDDQ-D: VDDQ-F: VDDQ-F: VDDQ-F: VDDQ-F: VDDQ-F: VDDQ-F: VDDQ-H: VDDQ-M: VDDQ-M 1uF_6.3V C2134 | 10E_63V C2133 | 10E_63V C2132 | 10E_63V C2131 | 10E_63V C2129 | 10E_63V C2040 | 10uF_X6S 10F_63V 10F_63V 10F_63V 10F_63V [3] MAA0_[8..0] << RFU/A12/NC A7/A8 | A0/A10 A6/A11 | A1/A9 A5/BA1 | A3/BA3 A4/BA2 | A2/BA0 A3/BA3 | A5/BA1 A2 /BA0 | A4/BA2 RFU/A12/NC A7/A8 | A0/A10 A6/A11 | A1/A9 A5/BA1 | A3/BA3 A4/BA2 | A2/BA0 A3/BA3 | A5/BA1 A2 /BA0 | A4/BA2 VDD-C5 VDD-C10 VDD-D1 VDD-G1 VDD-G1 VDD-C1 VDD-D1 VDD-G VDD-G VDD-G1 A1/A9 | A6/A11 A0/A10 | A7/A8 VDD-G1-VDD-L VDD-L A1/A9 | A6/A11 A0/A10 | A7/A8 WCK01 | WCK23 WCK01# | WCK23# WCK01 | WCK23 WCK01# | WCK23# VDD-R VSSQ-A1 VSSQ-A1 VSSQ-A1 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-E1 VSSQ-H1 VSSQ-H VSSQ-A1 VSSQ-A3 VSSQ-A2 VSSQ-C1 VSSQ-C3 VSSQ-C3 VSSQ-C3 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-M1 VSSQ-M DBI3# | DBI0# DBI2 #| DBI1# DBI1# | DBI2# DBI0# | DBI3# DBI3# | DBI0# DBI2 #| DBI1# DBI1# | DBI2# DBI0# | DBI3# RAS# | CAS# CAS# | RAS# RAS# | CAS# CAS# | RAS# CKE# CK# CKE# CK# CK CS#|WE# WE#|CS# +MVDD R2105 2.37K 1% R2106 5.49K 1% C2101 1uF 6.3V VSS-B5 VSS-B10 VSS-D10 VSS-G5 VSS-G10 VSS-H14 VSS-K14 VSS-K15 VSS-L10 VSS-P10 VSS-T5 VSS-T10 R2109 2.37K 1% R2110 5.49K 1% C2105 1uF 6.3V R2009 2.37K 1% R2010 5.49K 1% C2005 1uF 6.3V **AMD** Commerce Valley Drive East ets of 24 Doc No. 105-C204XX-00A itle GDDR5 Ch A

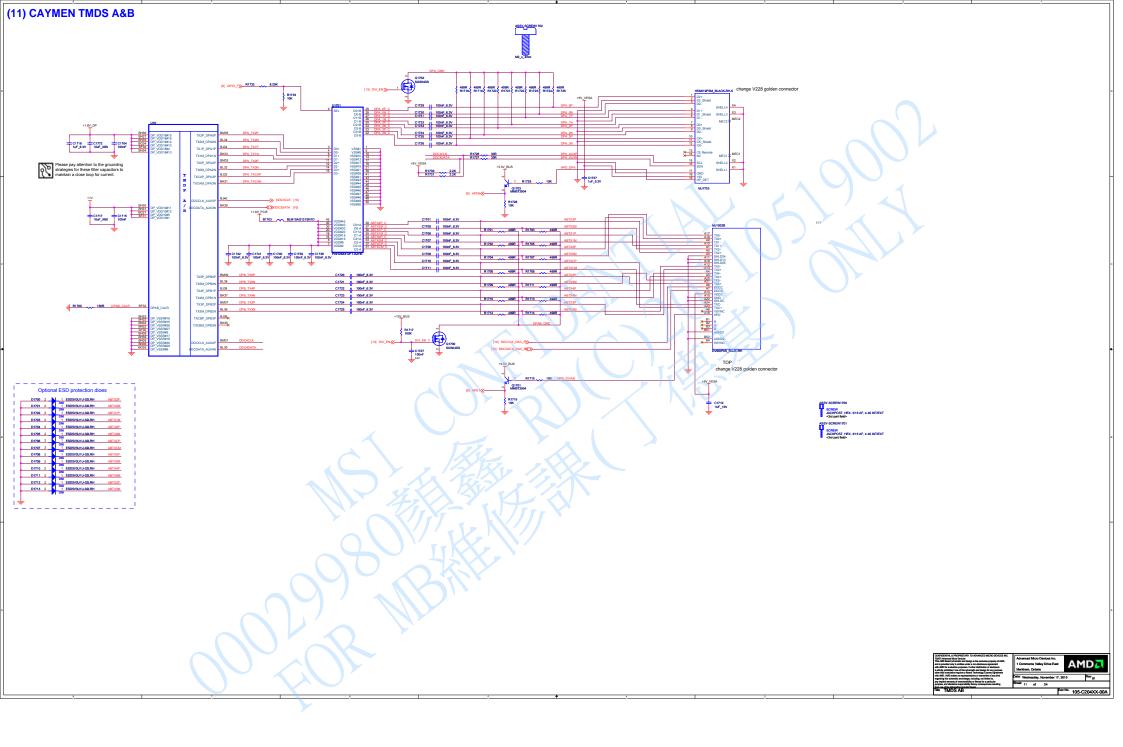


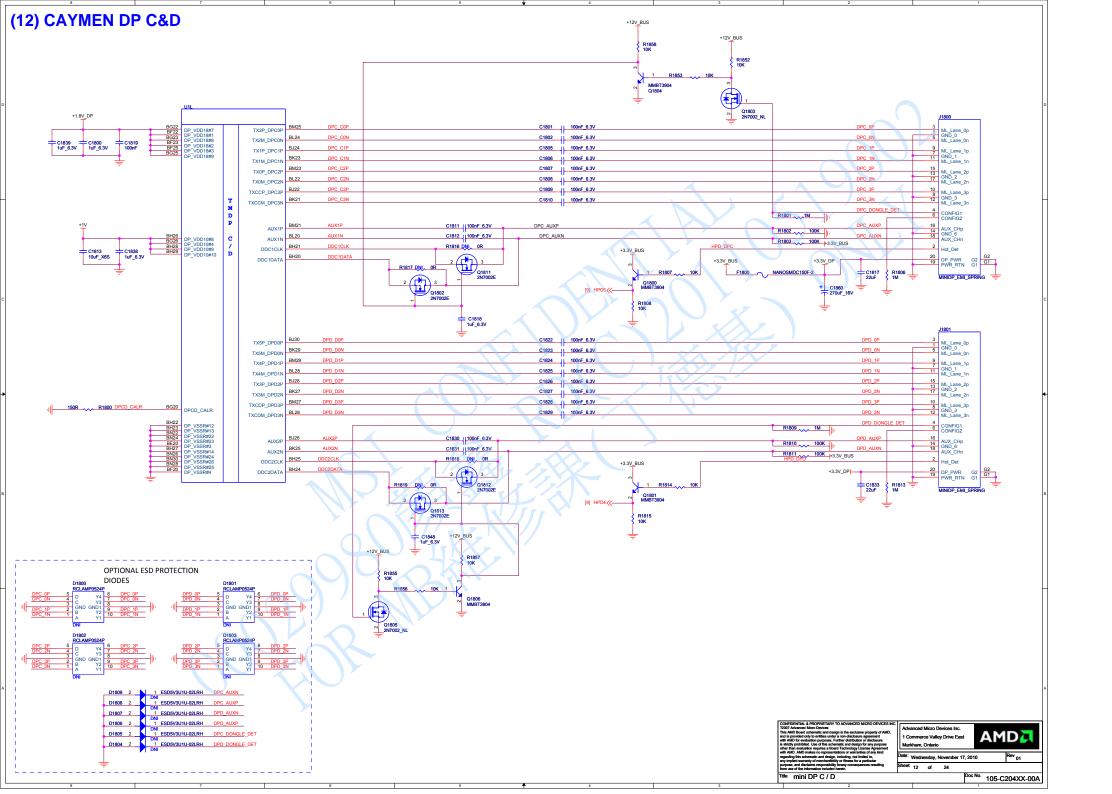
(7) GDDR5 Memory Channel C GDDR5 GDDR5 D031 | D07 D030 | D06 D029 | D05 D028 | D04 D028 | D04 D028 | D04 D026 | D02 D026 | D02 D026 | D02 D024 | D00 D023 | D01 D024 | D00 D023 | D01 D022 | D01 D022 | D01 D022 | D01 D019 | D019 | D019 D VDDQ-B VDDQ-B1 VDDQ-B1 VDDQ-D1 VDDQ-D1 VDDQ-D1 VDDQ-D1 VDDQ-E1 VDDQ-E1 VDDQ-E2 VDDQ-E1 VDQ-E1 VDQ VDDQ-B: VDDQ-B: VDDQ-B: VDDQ-B: VDDQ-B: VDDQ-D: VDDQ-D: VDDQ-D: VDDQ-D: VDDQ-B: VDDQ-P: VDQQ-P: VDQQ-P DQ12 | DQ20 DQ11 | DQ19 DQ10 | DQ18 DQ9 | DQ17 DQ8 | DQ16 DQ7 | DQ31 DQ6 | DQ30 DQ5 | DQ29 DQ4 | DQ28 DQ3 | DQ27 DQ2 | DQ26 DQ1 | DQ25 DQ1 | DQ25 +MVDD C2544 10uF_X6S C2543 10uF_X6S C2542 10uF_X6S C2538 1 10F_6.3V C2538 1 10F_6.3V C2537 1 10F_6.3V C2536 1 10F_6.3V C2535 1 10F_6.3V C2440 | 10uF_X6S | 10F_63V 10F_63V 10F_63V 10F_63V 10F_63V 10F_63V 10F_63V 10uF_X6S 10F_6.3V 10F_6.3V 10F_6.3V 10F_6.3V 10F_6.3V 10F_6.3V 1uF_6.3V [4] MAC0 [8..0] (RFU/A12/NC A7/A8 | A0/A10 A6/A11 | A1/A9 A5/BA1 | A3/BA3 A4/BA2 | A2/BA0 A3/BA3 | A5/BA1 A2 /BA0 | A4/BA2 41/A9 | A6/A11 RFU/A12/NC A7/A8 | A0/A10 A6/A11 | A1/A9 A5/BA1 | A3/BA3 A4/BA2 | A2/BA0 A3/BA3 | A5/BA1 A2/BA0 | A4/BA2 A1/A9 | A6/A11 A0/A10 | A7/A8 VDD-C5 VDD-C10 VDD-D1* VDD-G* VDD-G4 VDD-C VDD-C1 VDD-D1 VDD-G VDD-G1 VDD-G1 1/A9 | A6/A11 0/A10 | A7/A8 VDD-L VDD-L VDD-L WCK01 | WCK23 WCK01# | WCK23# WCK01 | WCK23 WCK01# | WCK23# VSSQ-A VSSQ-A VSSQ-A VSSQ-C VSSQ-C VSSQ-C VSSQ-C VSSQ-C VSSQ-E VS EDC3 | EDC0 EDC2 | EDC1 EDC1 | EDC2 EDC0 | EDC3 DBI3# | DBI0# DBI2 #| DBI1# DBI1# | DBI2# DBI0# | DBI3# DRIS# I DRIN# DBI2#| DBI1# DBI1# | DBI2# DBI0# | DBI3# VSSQ-E12 VSSQ-E14 VSSQ-F14 VSSQ-F14 VSSQ-M12 VSSQ-M12 VSSQ-M12 VSSQ-M12 VSSQ-M12 VSSQ-M12 VSSQ-M12 VSSQ-M12 VSSQ-R14 VSSQ-V12 VSS RAS# | CAS# CAS# | RAS# RAS# | CAS# CAS# | RAS# +MVDD /pp,NC /pp,NC1 VSS-B5 VSS-B10 VSS-D10 VSS-G10 VSS-G10 VSS-H11 VSS-H14 VSS-K14 VSS-K14 VSS-L5 VSS-L10 VSS-P10 VSS-T5 VSS-T10 VSS-B5 VSS-B10 VSS-D10 VSS-G10 VSS-G10 VSS-H1 VSS-H14 VSS-K14 VSS-L1 VSS-L1 VSS-L1 VSS-P1(VSS-T1 VREFD1 VREFD2 **AMD** Commerce Valley Drive East Markham, Ontario et 7 of 24 Doc No. 105-C204XX-00A itle GDDR5 Ch C

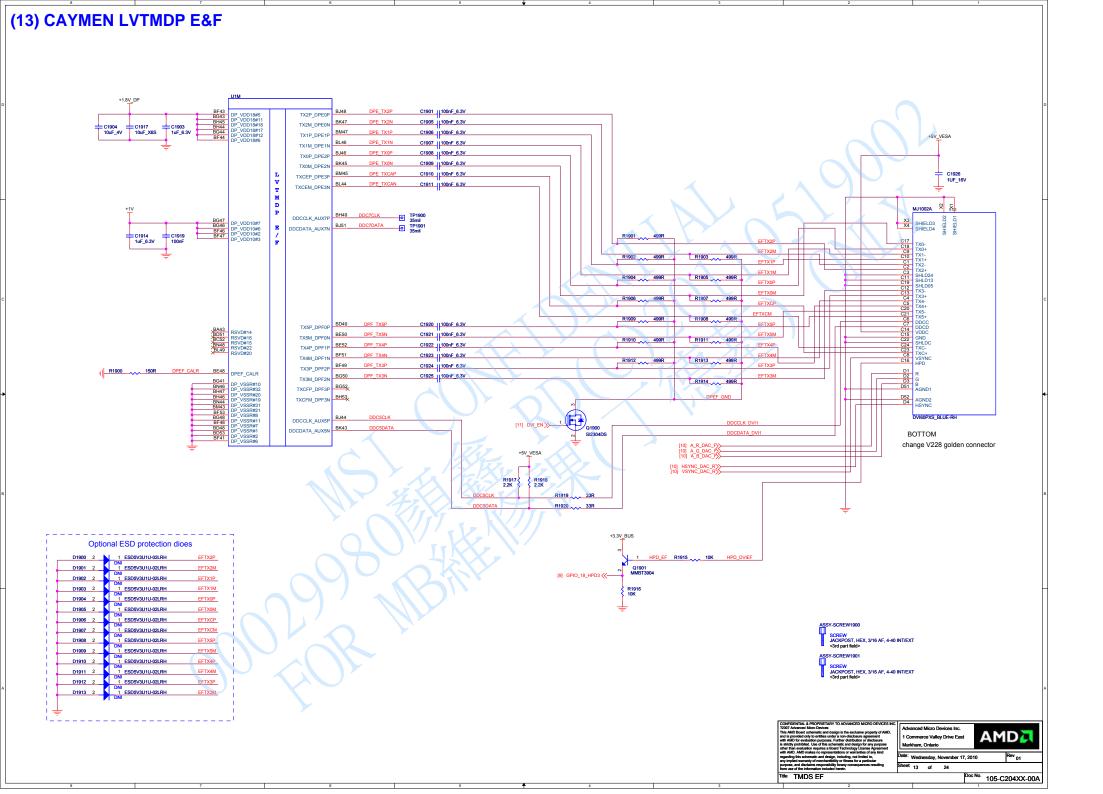
(8) GDDR5 Memory Channel D VDDQ-B: VDDQ-B: VDDQ-B: VDDQ-B: VDDQ-B: VDDQ-D: VDDQ-D: VDDQ-D: VDDQ-E: VDDQ-F: VDDQ-F: VDDQ-F: VDDQ-F: VDDQ-B: VDDQ-P: VDDQ-T: VDDQ-T VDDQ-812 VDDQ-814 VDDQ-51 VDDQ-51 VDDQ-51 VDDQ-51 VDDQ-51 VDDQ-61 VDDQ-71 VDQ-71 V C2716 C2715 C2714 C2713 C2711 10F_63V 10uF_X6S 10uF_X6S 1uF_6.3V 1uF_6.3V 1uF_6.3V [4] MADO_[8..0] <<-RFU/A12/NC A7/A8 | A0/A10 A6/A11 | A1/A9 A5/BA1 | A3/BA3 A4/BA2 | A2/BA0 A3/BA3 | A5/BA1 A2 /BA0 | A4/BA2 A1/A9 | A6/A11 VDD-C1 VDD-D1 VDD-G1 VDD-G1 VDD-G1 VDD-G1 VDD-L1 VDD-L2 VDD-C5 VDD-C10 VDD-D11 VDD-G1 VDD-G4 VDD-G11 VDD-G14 A3/BA3 | A5/BA1 A2 /BA0 | A4/BA2 A1/A9 | A6/A11 A0/A10 | A7/A8 WCK01 | WCK23 WCK01# | WCK23# WCK23 | WCK01 WCK23# | WCK01# WCK23 | WCK01 WCK23# | WCK01# VSSQ-A1 VSSQ-A2 VSSQ-A1 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-E1 VSSQ-M1 VSSQ-M VSSQ-A1 VSSQ-A3 VSSQ-A3 VSSQ-A12 VSSQ-A14 VSSQ-C14 VSSQ-C14 VSSQ-C14 VSSQ-C14 VSSQ-C14 VSSQ-C14 VSSQ-E15 VSSQ-E15 VSSQ-E16 VSSQ-E16 VSSQ-E17 VSSQ-E17 VSSQ-E17 VSSQ-M14 VSSQ-M DBI3# | DBI0# DBI2 #| DBI1# DBI1# | DBI2# DBI0# | DBI3# RAS# | CAS# CAS# | RAS# RAS# | CAS# CAS# | RAS# CKE# CK# CK [4.7] DRAM RST2 \> RESET# +MVDD VSS-B1 VSS-D1 VSS-G1 VSS-G1 VSS-H1 VSS-K1 VSS-L1 VSS-L1 VSS-L1 VSS-P10 VSS-T1 VSS-B5 VSS-B10 VSS-D10 VSS-G5 VSS-G10 VSS-H14 VSS-K14 VSS-K14 VSS-L5 VSS-L10 VSS-P10 VSS-T5 VSS-T50 +MVDD **AMD** Commerce Valley Drive East Markham, Ontario Doc No. 105-C204XX-00A itle GDDR5 Ch D

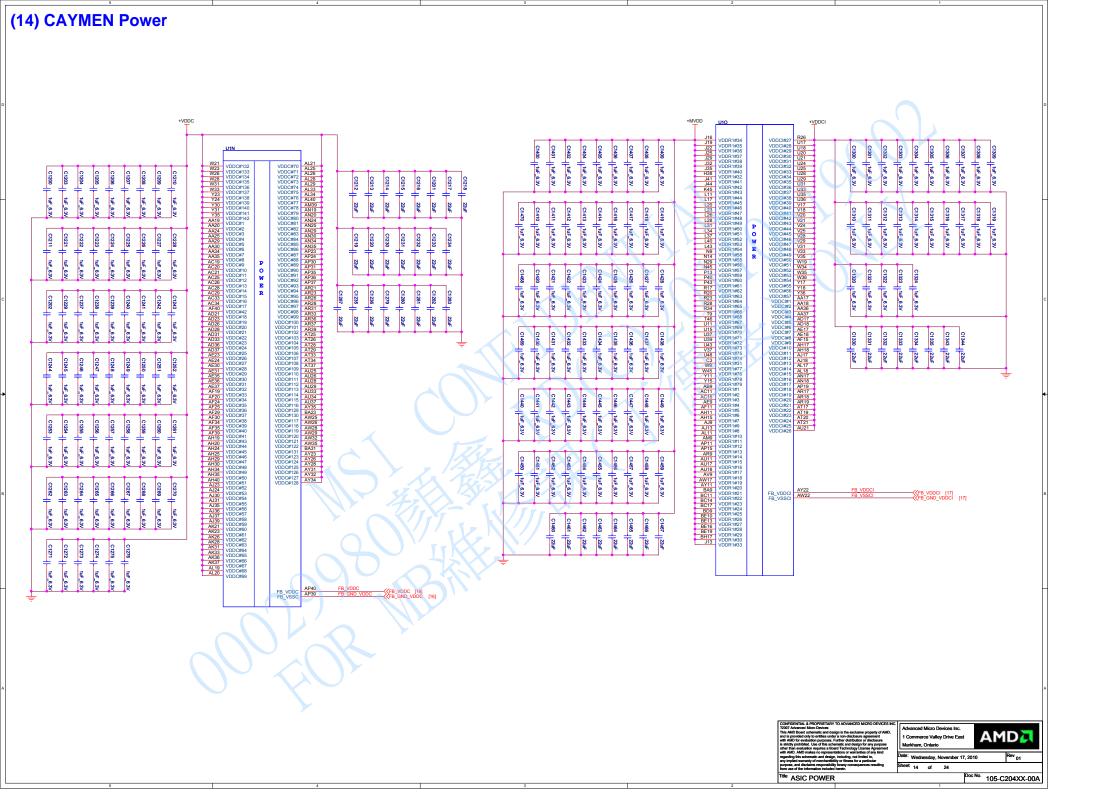


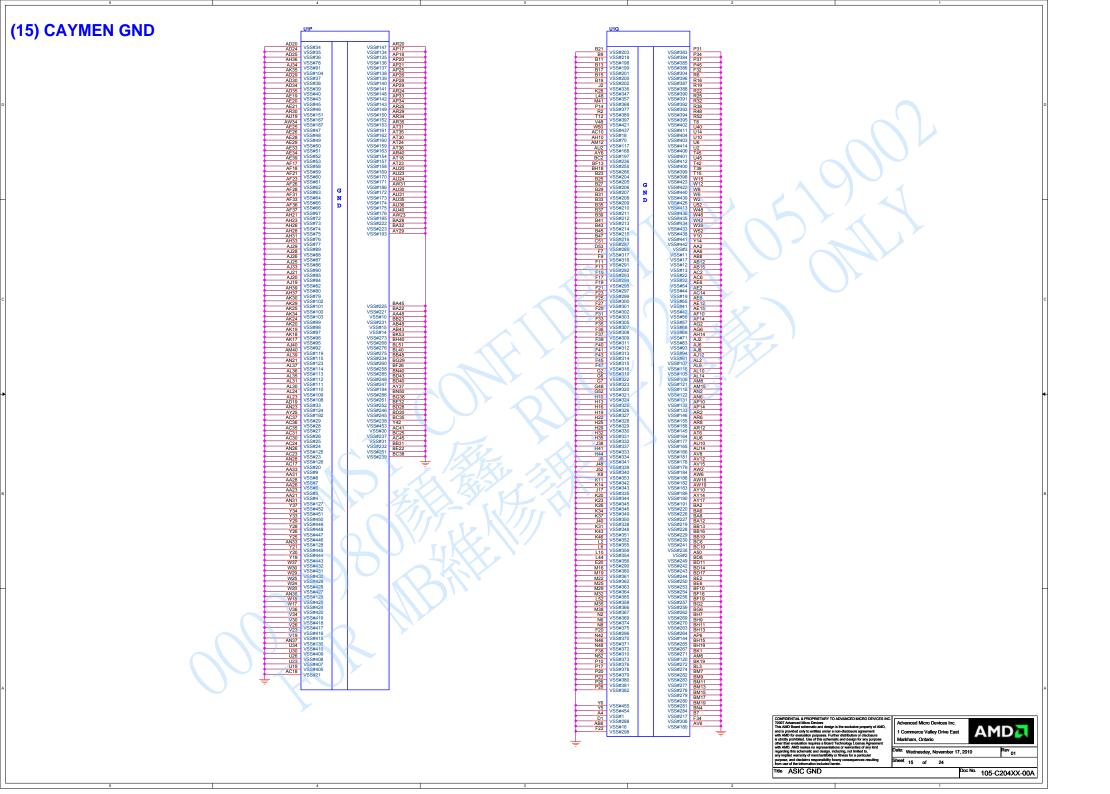


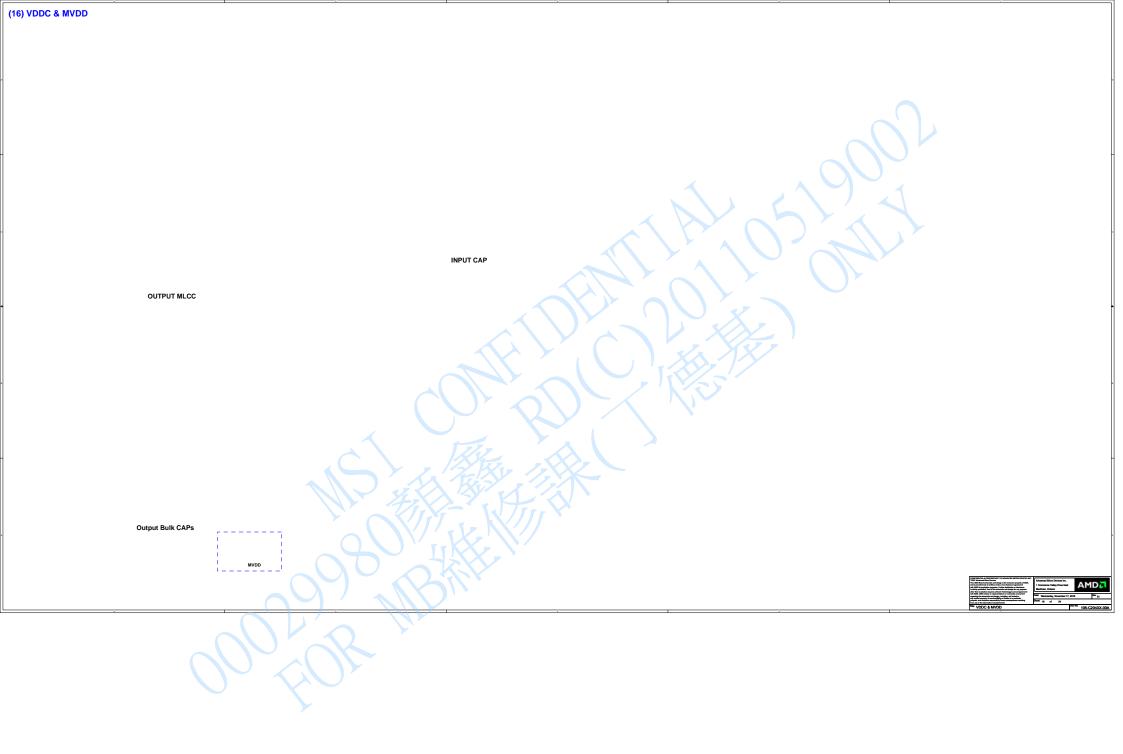


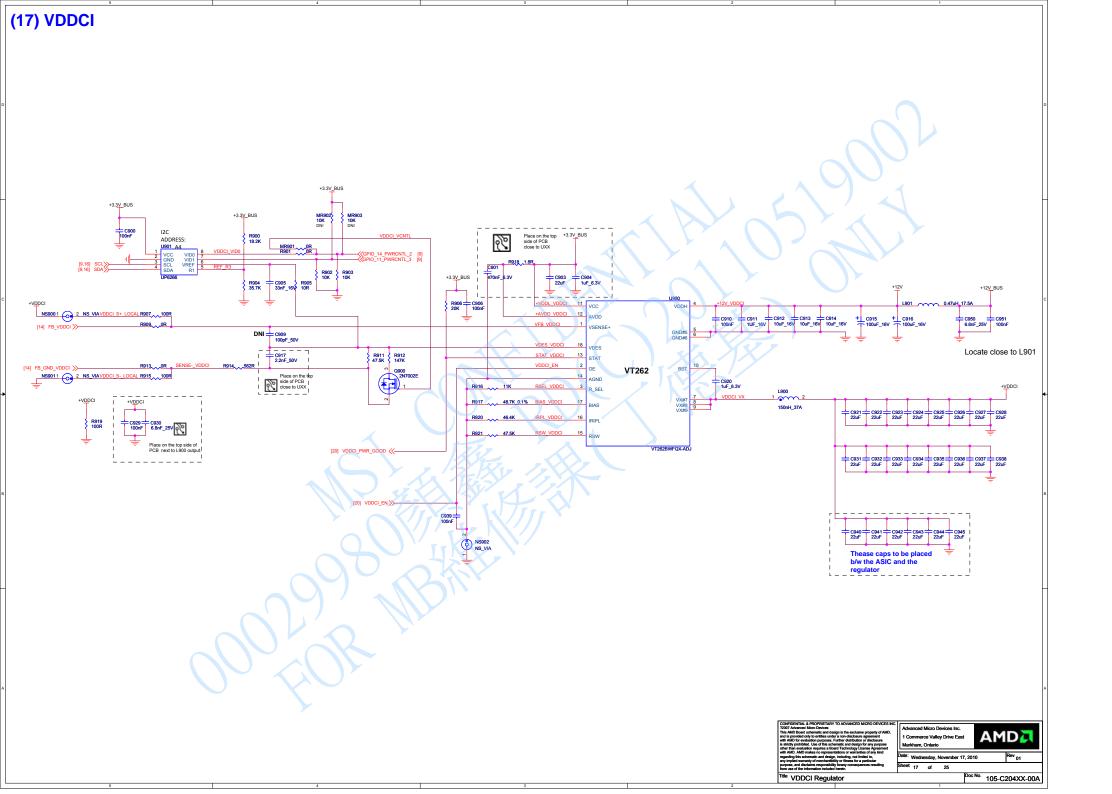






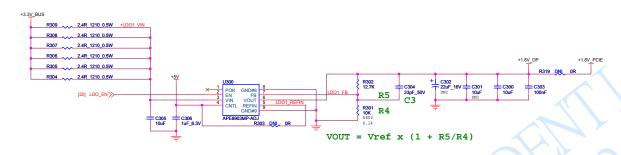


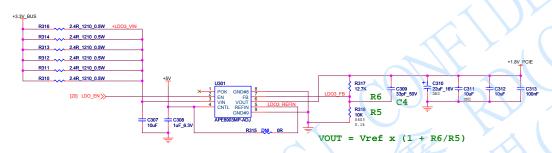




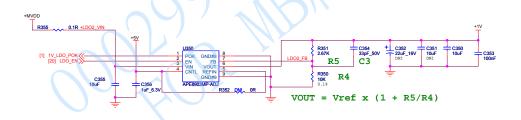
(18) CAYMEN Small Rail Regulators

LDO #1: Vin = 2.3V to 3.6V MAX Vout = +1.8V +/- 2% lout = 2.0A (TBV) RMS MAX PCB: 50 to 70mm sq. copper area for cooling

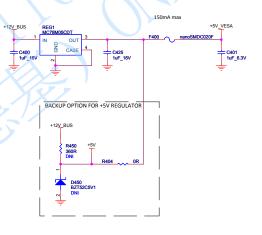


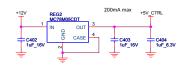


LDO #2: Vin = +1.40V to 1.8VMAX Vout = +1V +/- 2% lout = 1.5A (TBV) RMS MAX PCB: 50 to 70mm sq. copper area for cooling

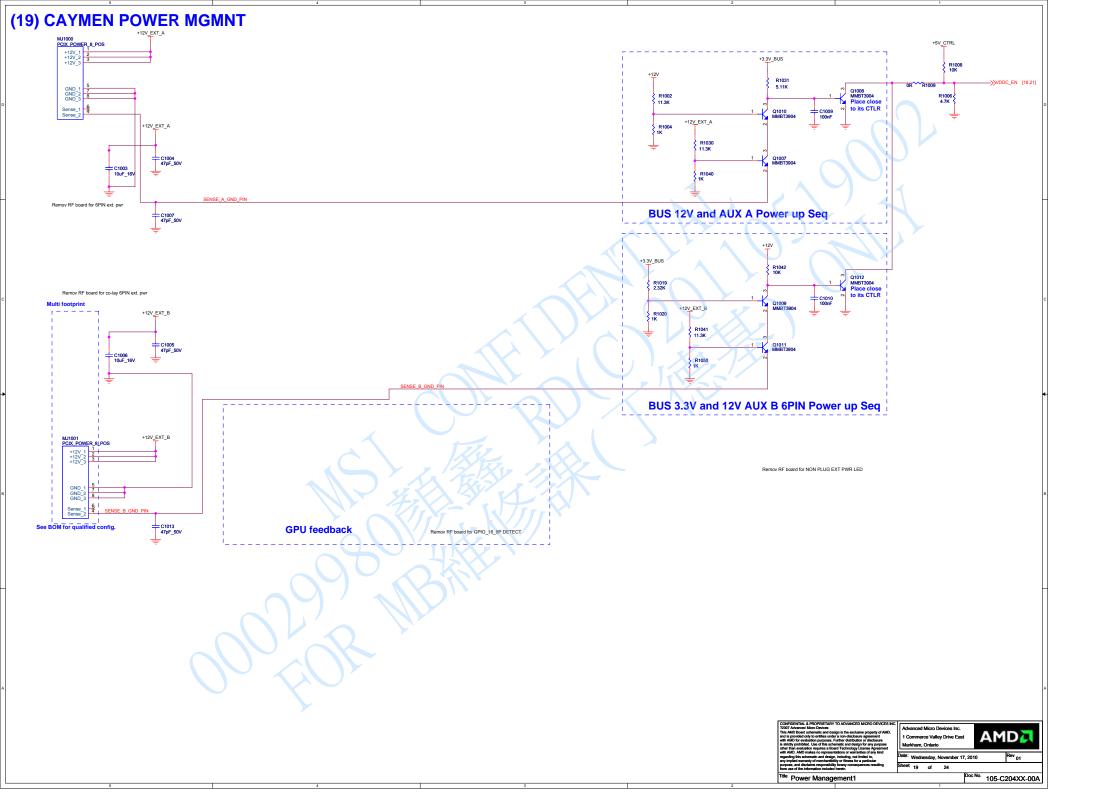


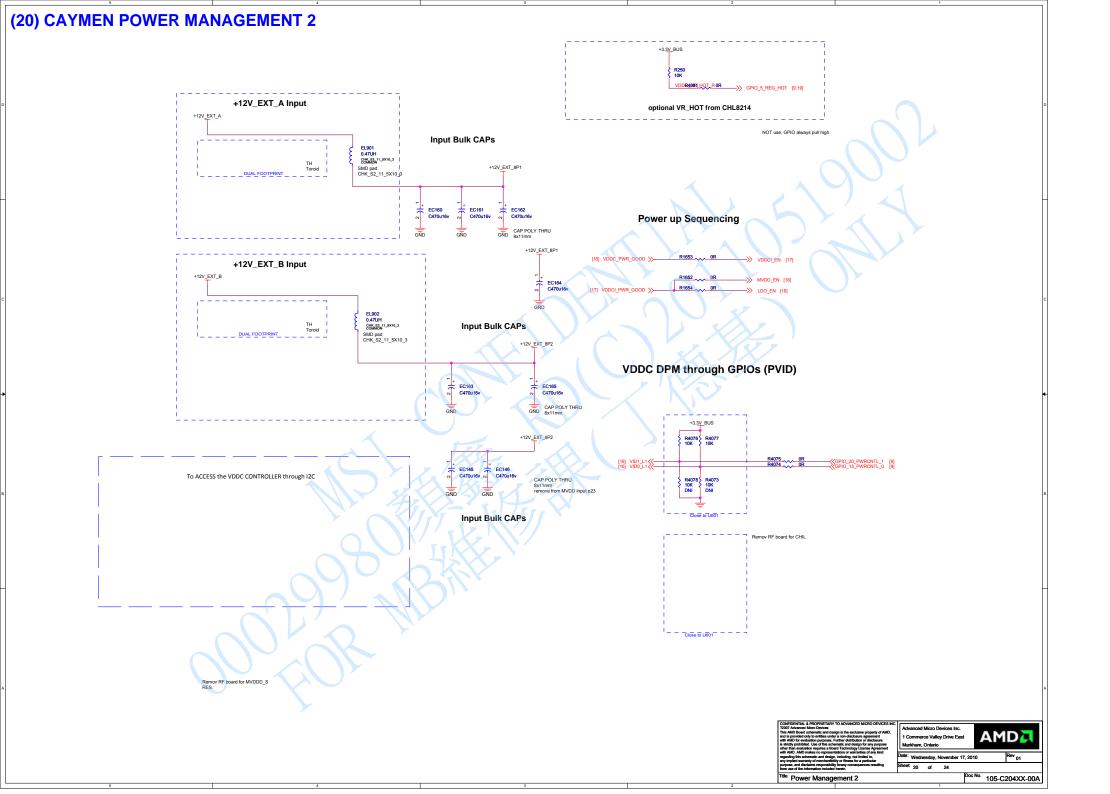
Regulators for +5V, +5V_VESA and +5V_HDMI lout max = 150mA (DVI+HDMI)

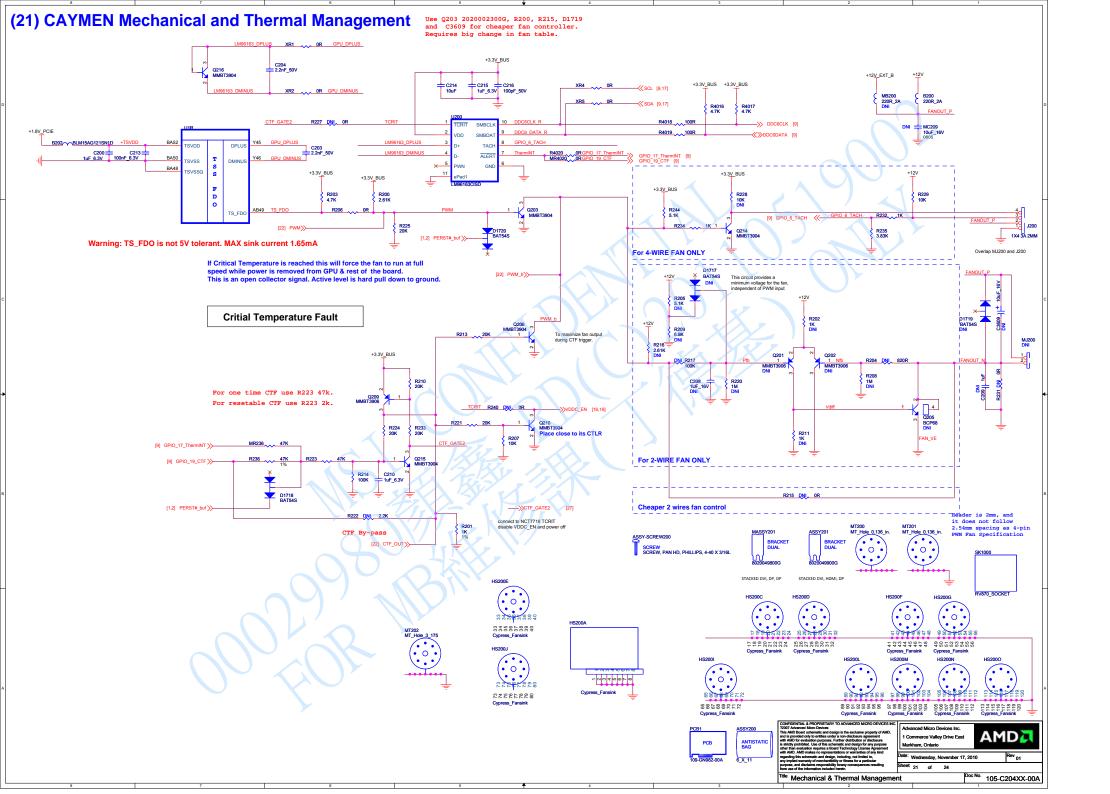


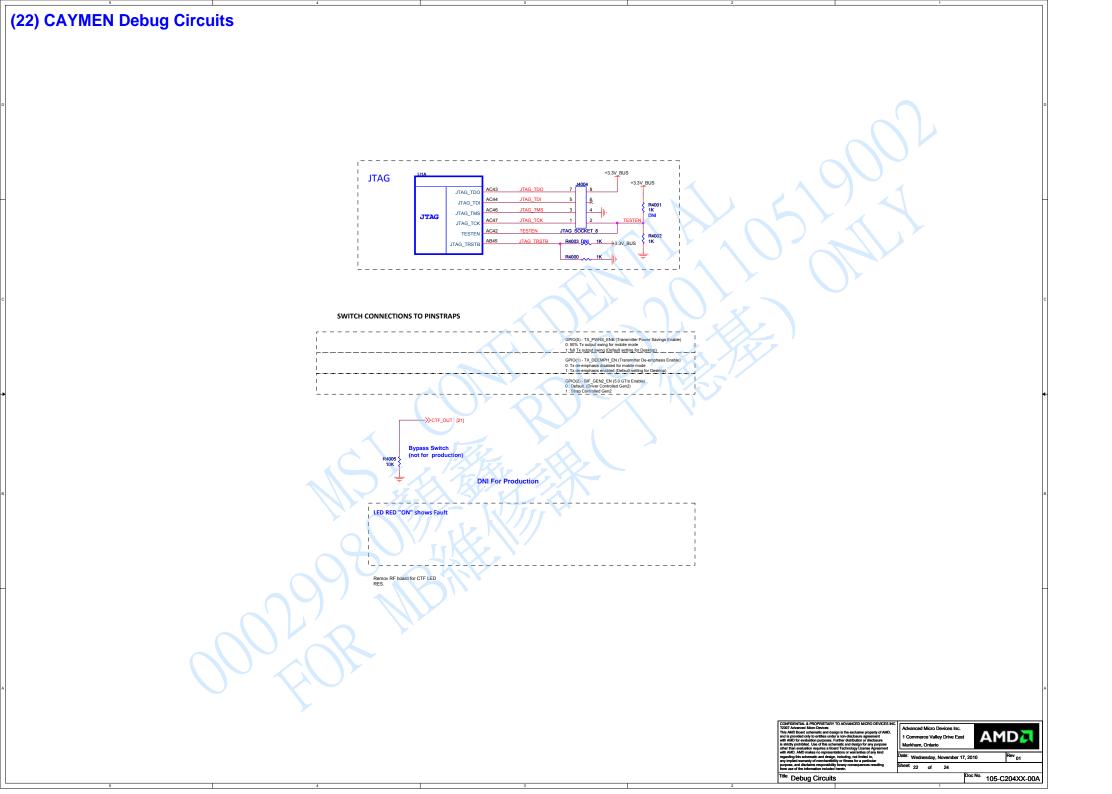


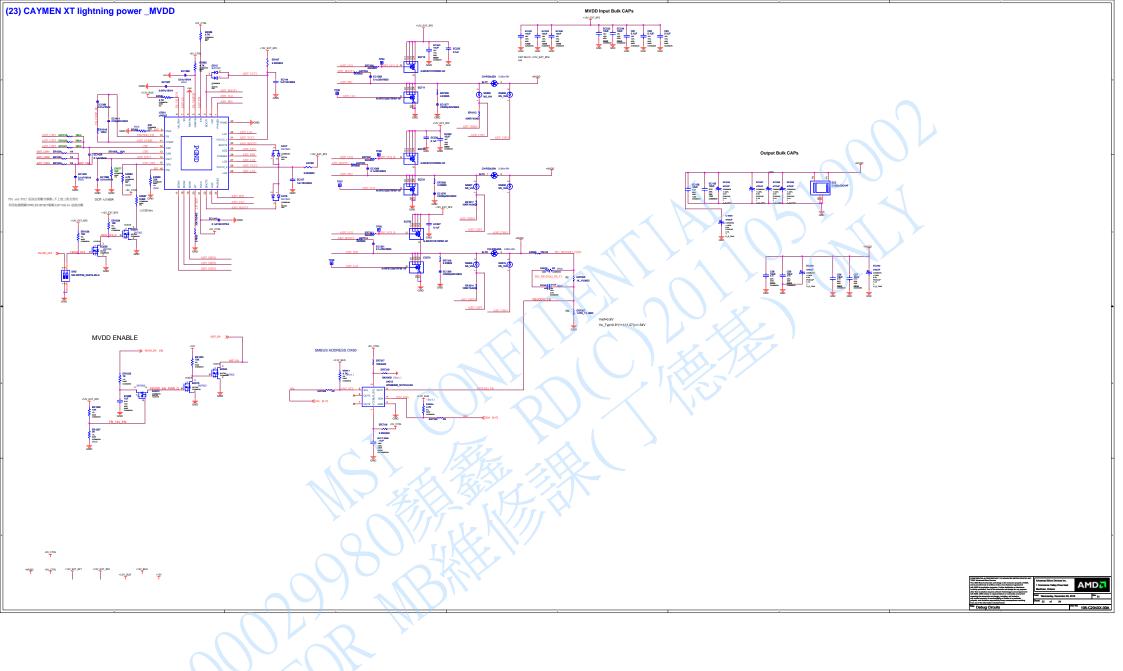
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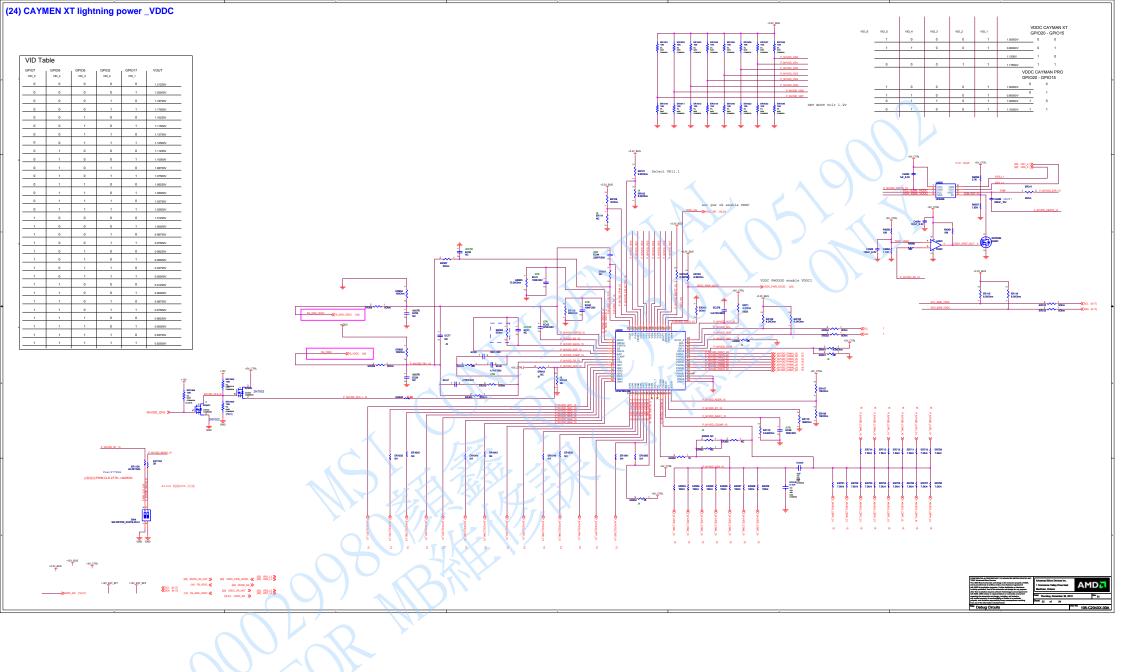


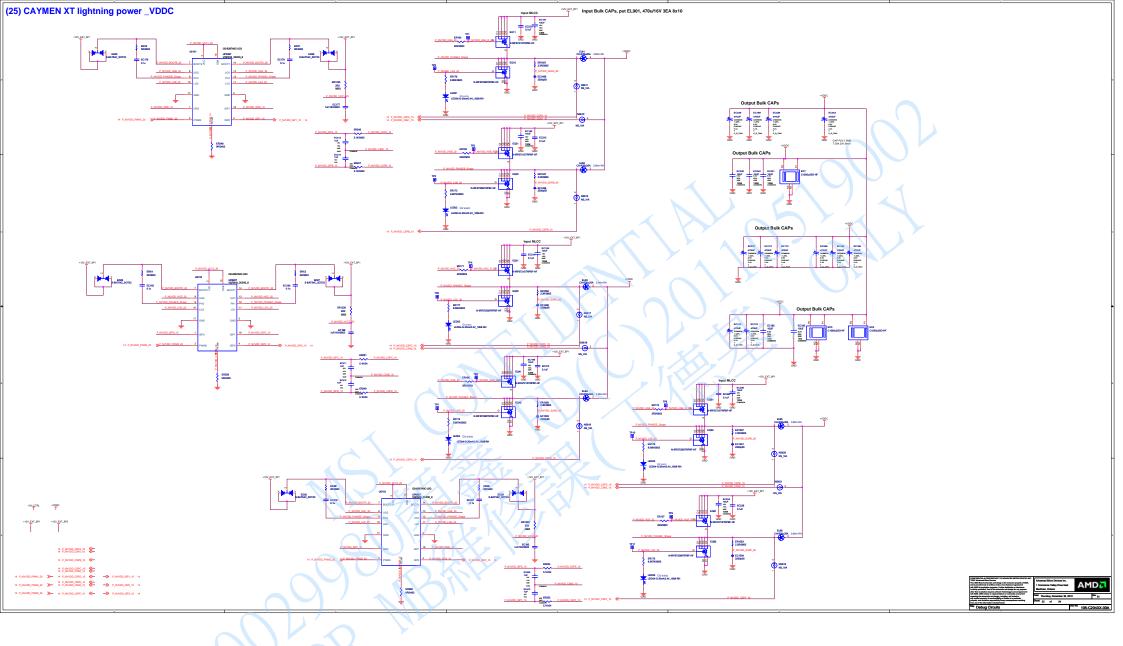


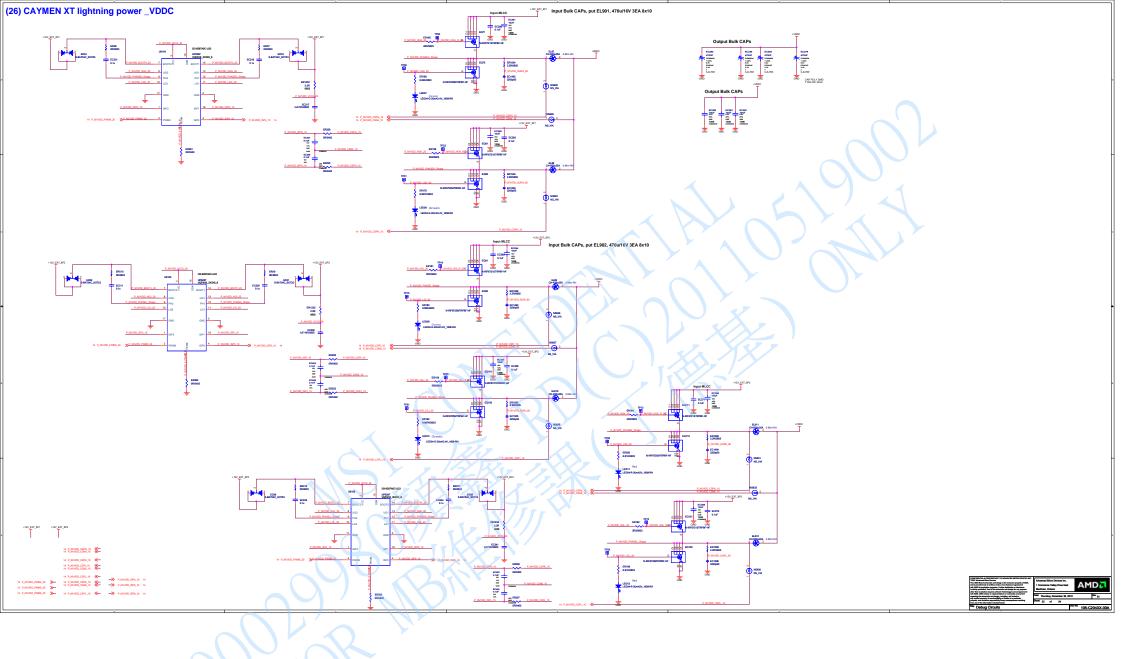


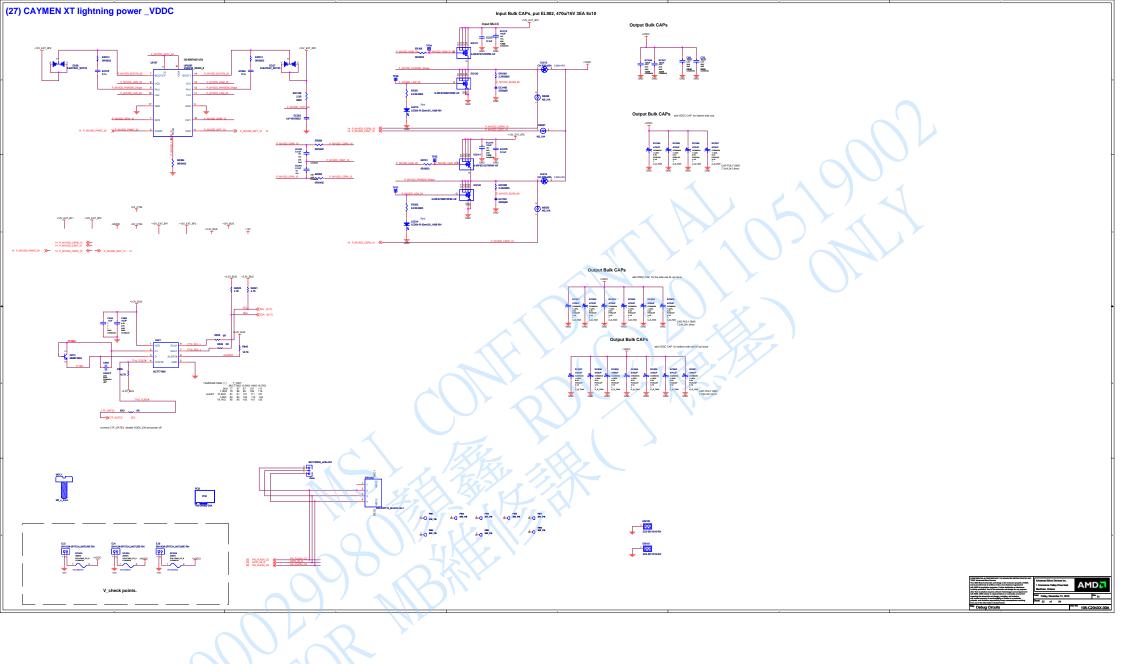


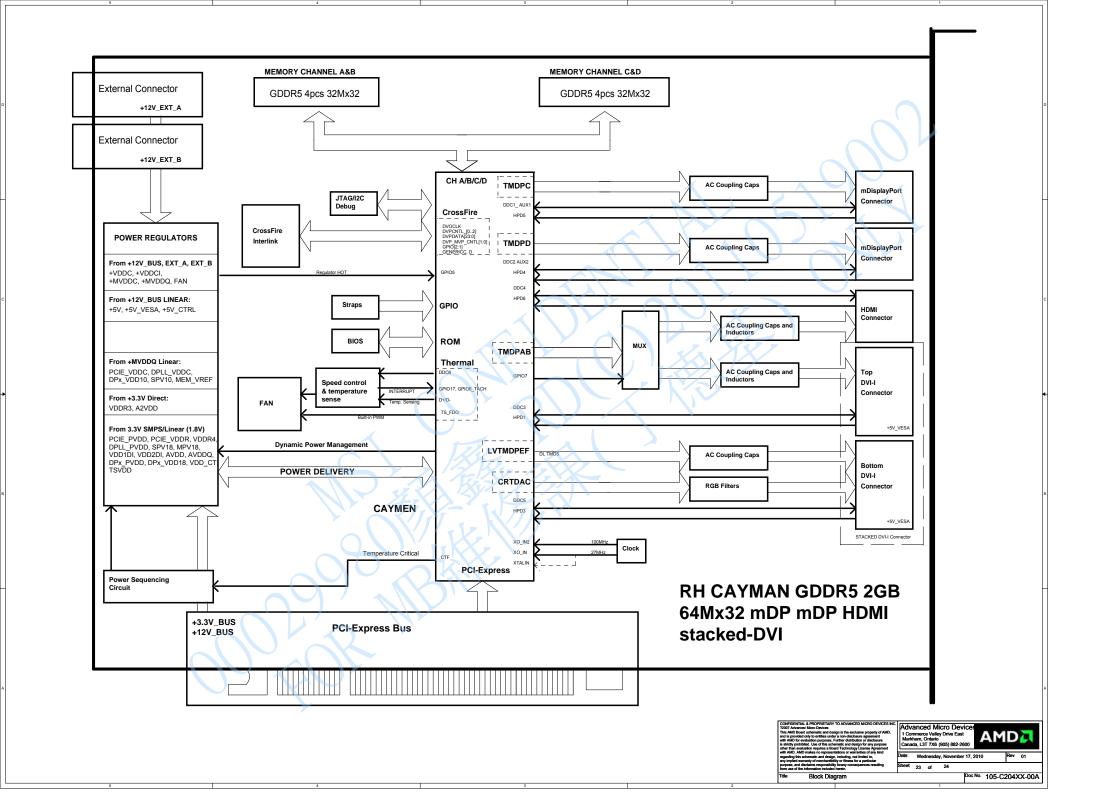












AMD			Title RH CAYMAN GDDR5 2GB 64Mx32 mDP mDP HDMI stacked-DVI	Schematic No. 105-C204XX-00A	Date: Wednesday, November 17, 2010	
			REVISION HISTORY NOTE: This schematic re For Stuffing option Please contact All	presents the PCB, it does not represent any specifi ns (component values, DNI , ? please consult the ID representative to obtain latest BOM closest to th	c SKU. product specific BOM. le application desired.	
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