PG161-B00

TU106 8GB GDDR6, 192b, X16
DVI-D + DP + HDMI

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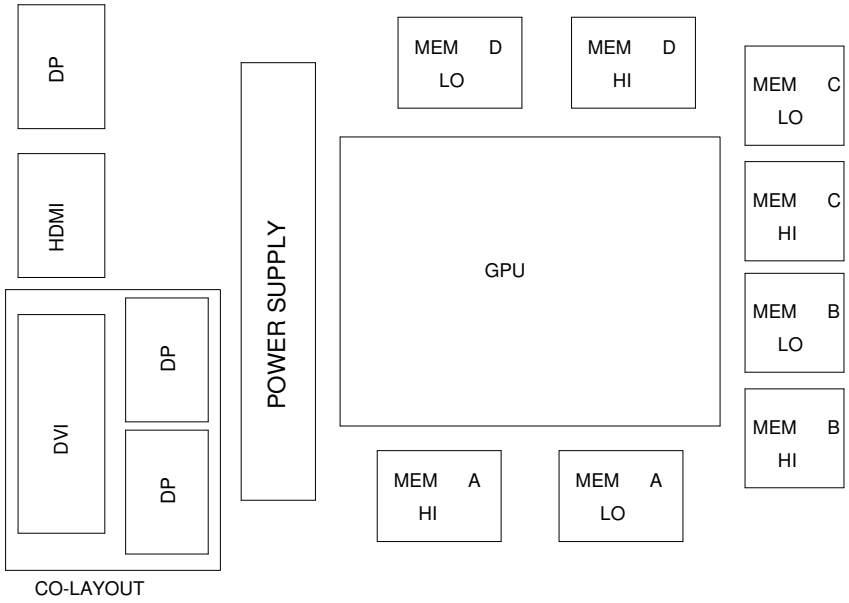
Page2: Block Diagram



Power Supply:

- Power Supply NVVDD-PH6
- Power Supply NVVDD-PH5
- Power Supply NVVDD-PH4
- Power Supply NVVDD-PH3
- Power Supply NVVDD-PH2
- Power Supply NVVDD-PH1
- Power Supply FBVDDQ-PH2
- Power Supply FBVDDQ-PH1
- Power Supply 5V
- PEX_VDD
- 1V8
- Fan
- DP_PWR

→ EXT_12V 8PIN PWR

→ PEX_12V Finger

→ PEX_3V3 FINGER

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Block Diagram

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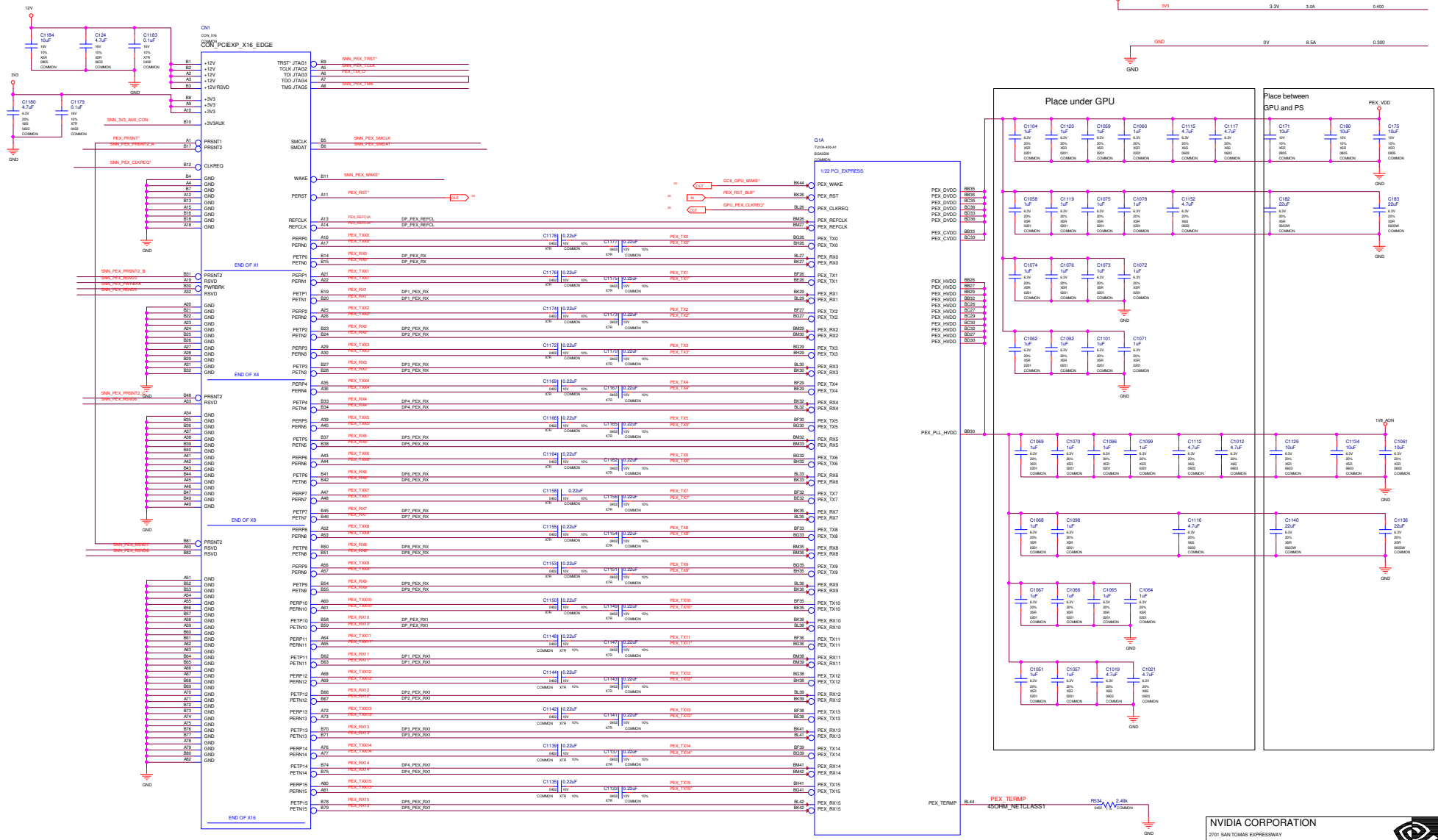
Page3: PCI Express



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.406
3V3	3.3V	3.0A	0.400
GND	0V	8.5A	0.300

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI Express

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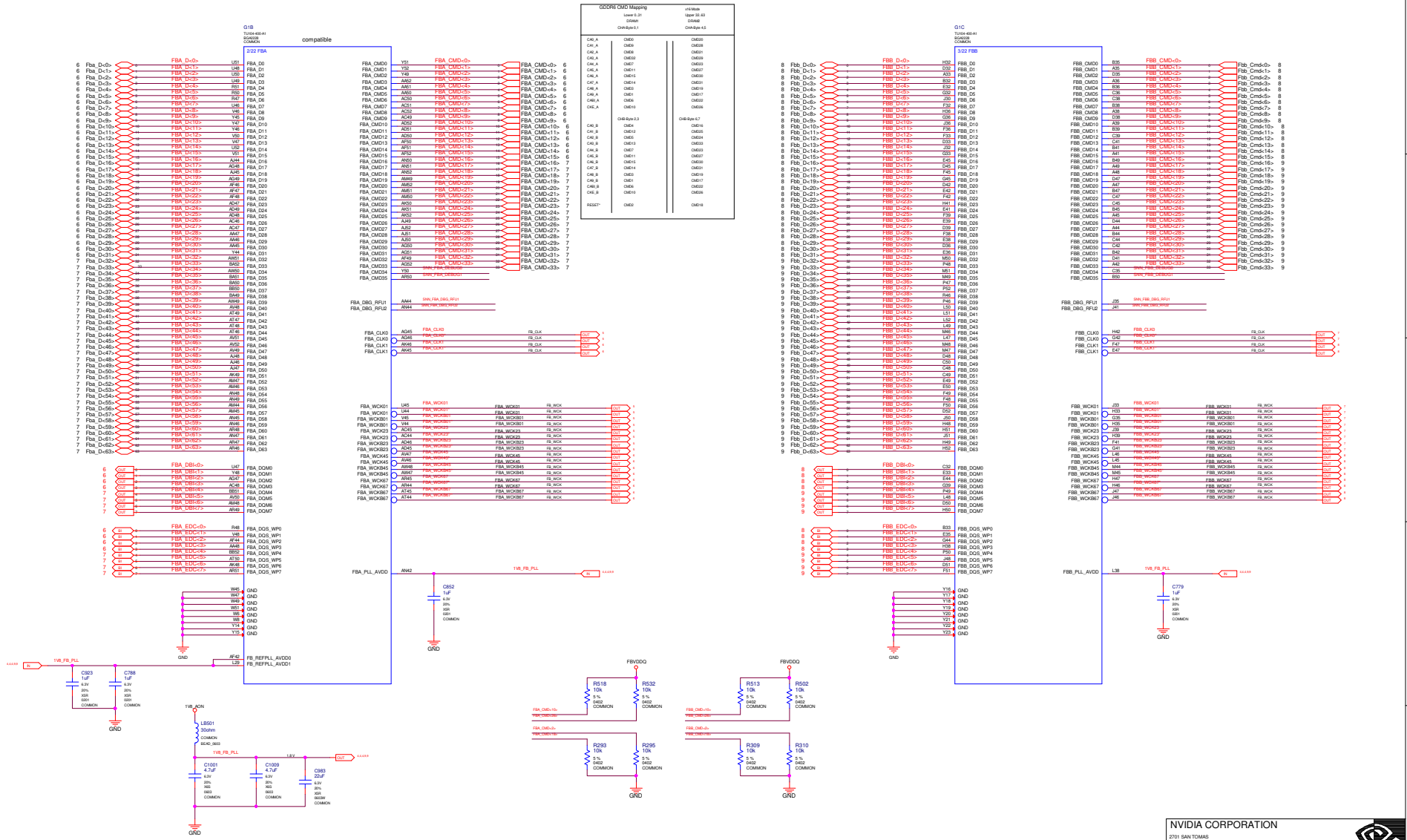
Page4: MEMORY: GPU Partition A/B



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PAGE DETAIL	MEMORY: GPU FB_AB

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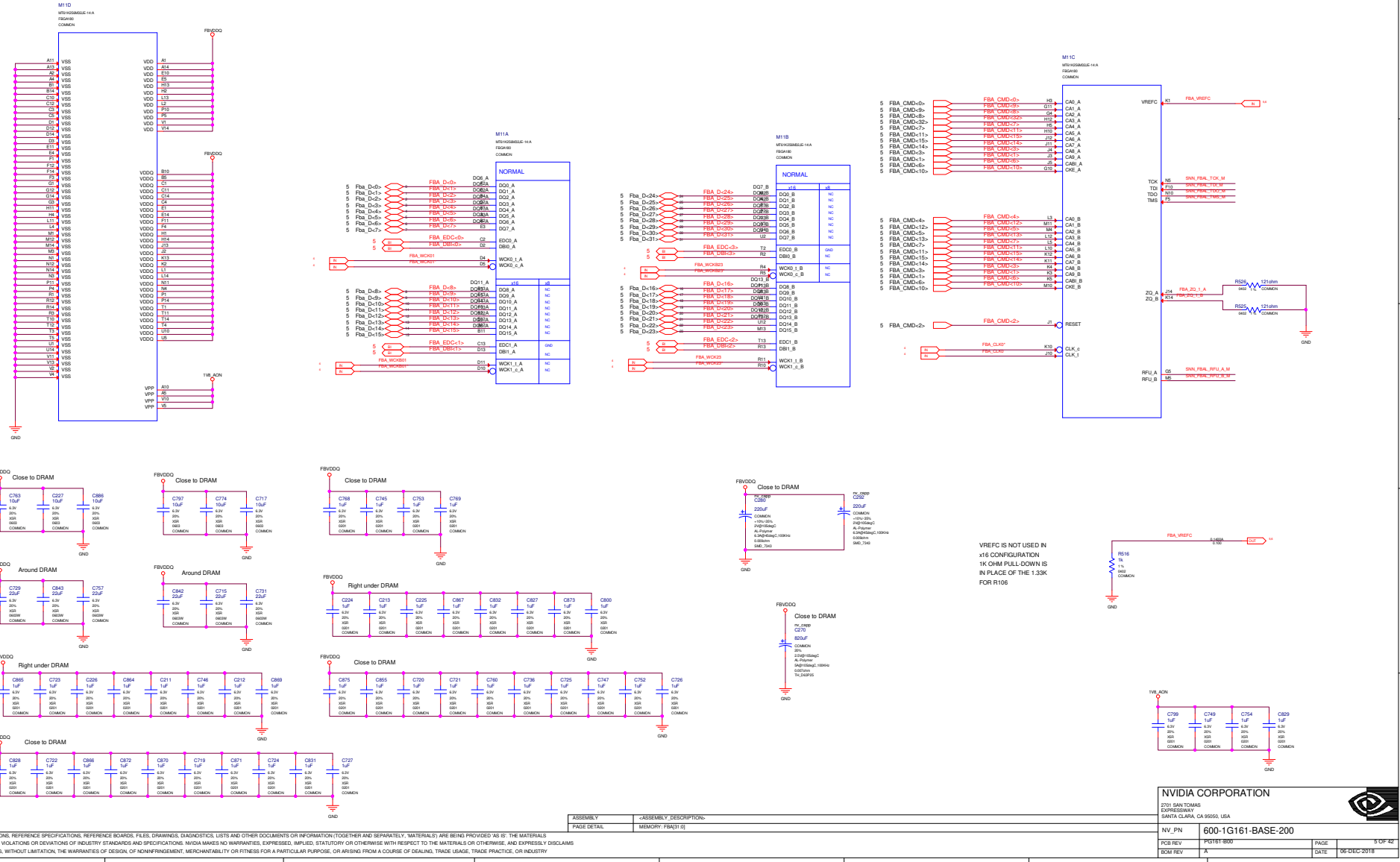
Page5: MEMORY: FBA Partition 31..0



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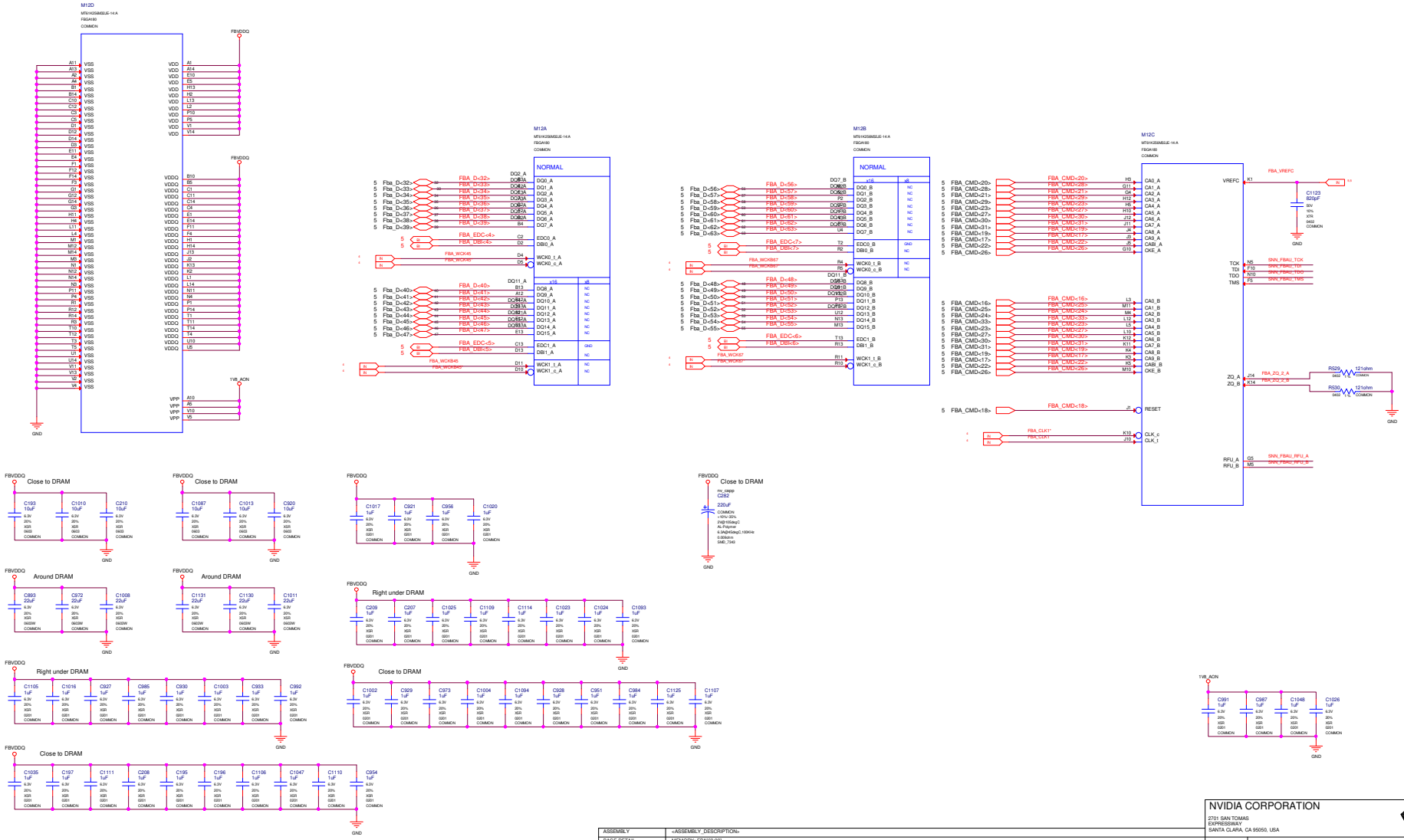
Page6: MEMORY: FBA Partition 63..32



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PAGE DETAIL	MEMORY: FBA[63:32]

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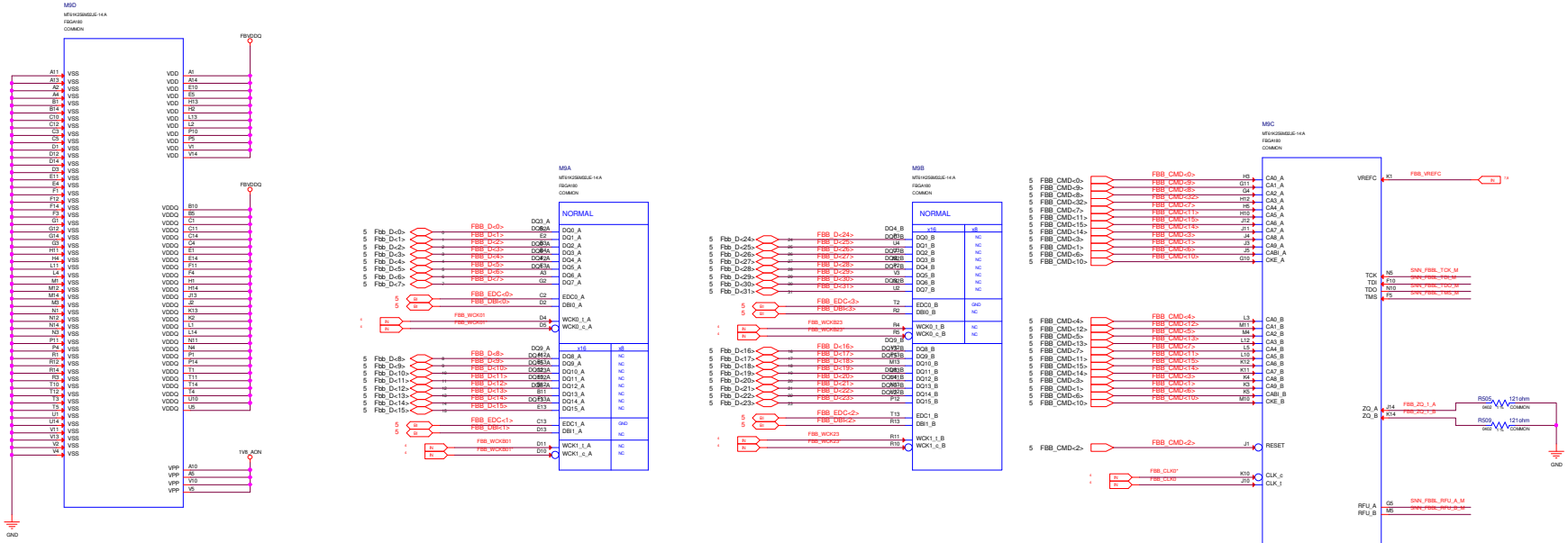
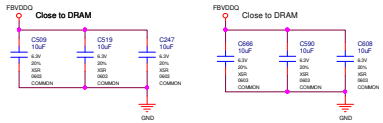
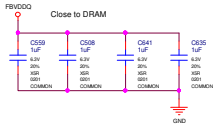
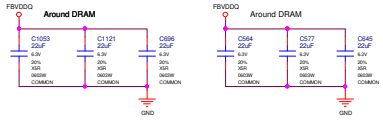
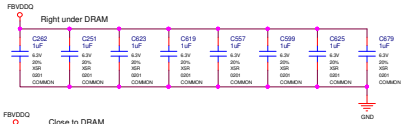
Page7: MEMORY: FBB Partition 31..0

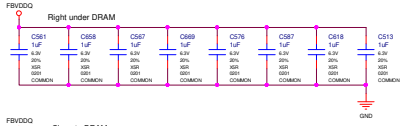


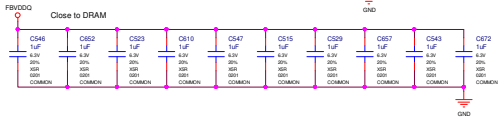


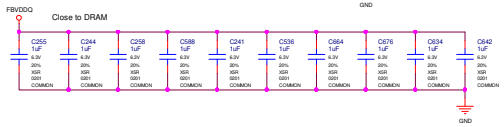




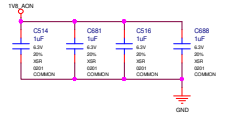








VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R104



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PAGE DETAIL	MEMORY: FBB[31:0]

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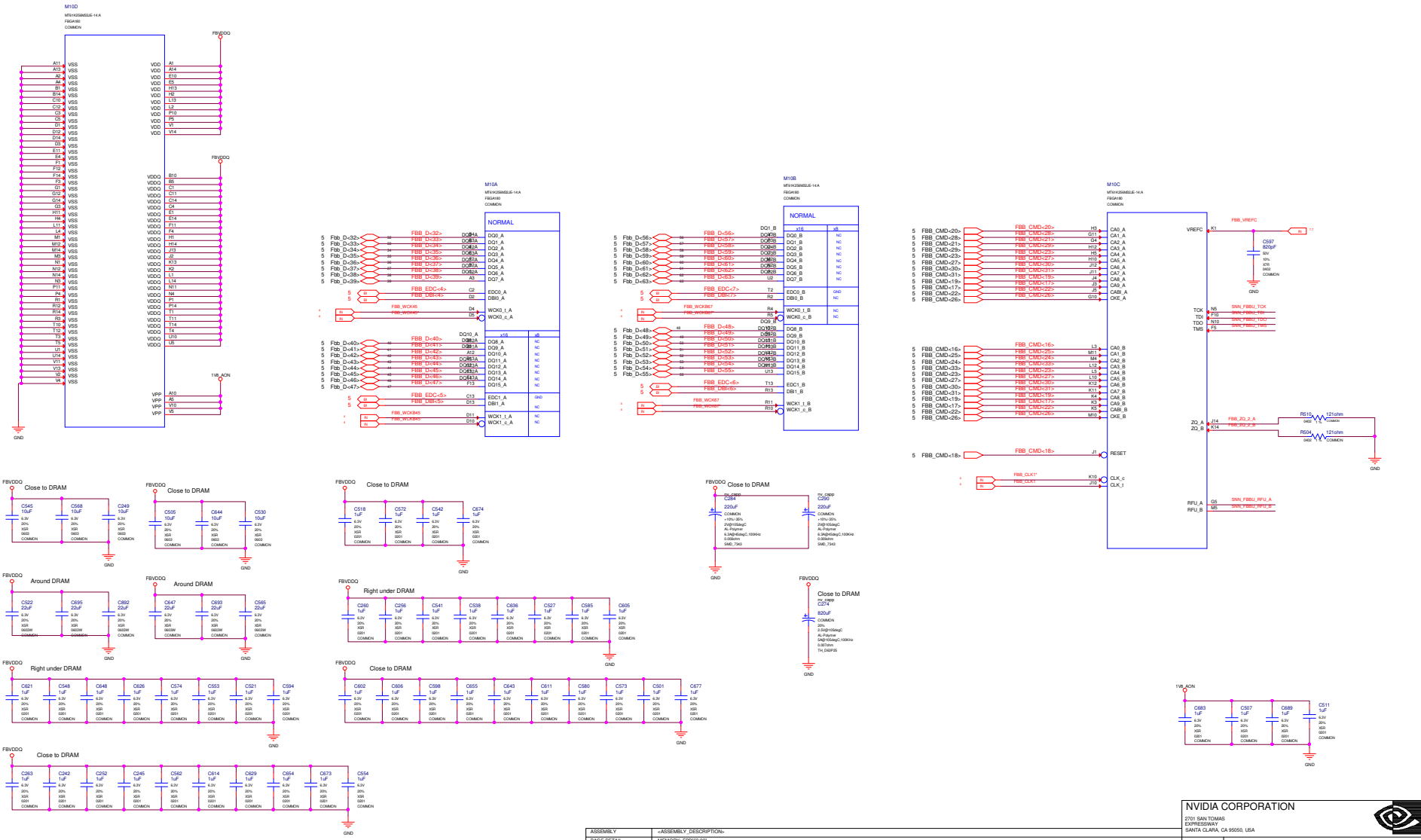
Page8: MEMORY: FBB Partition 63..32



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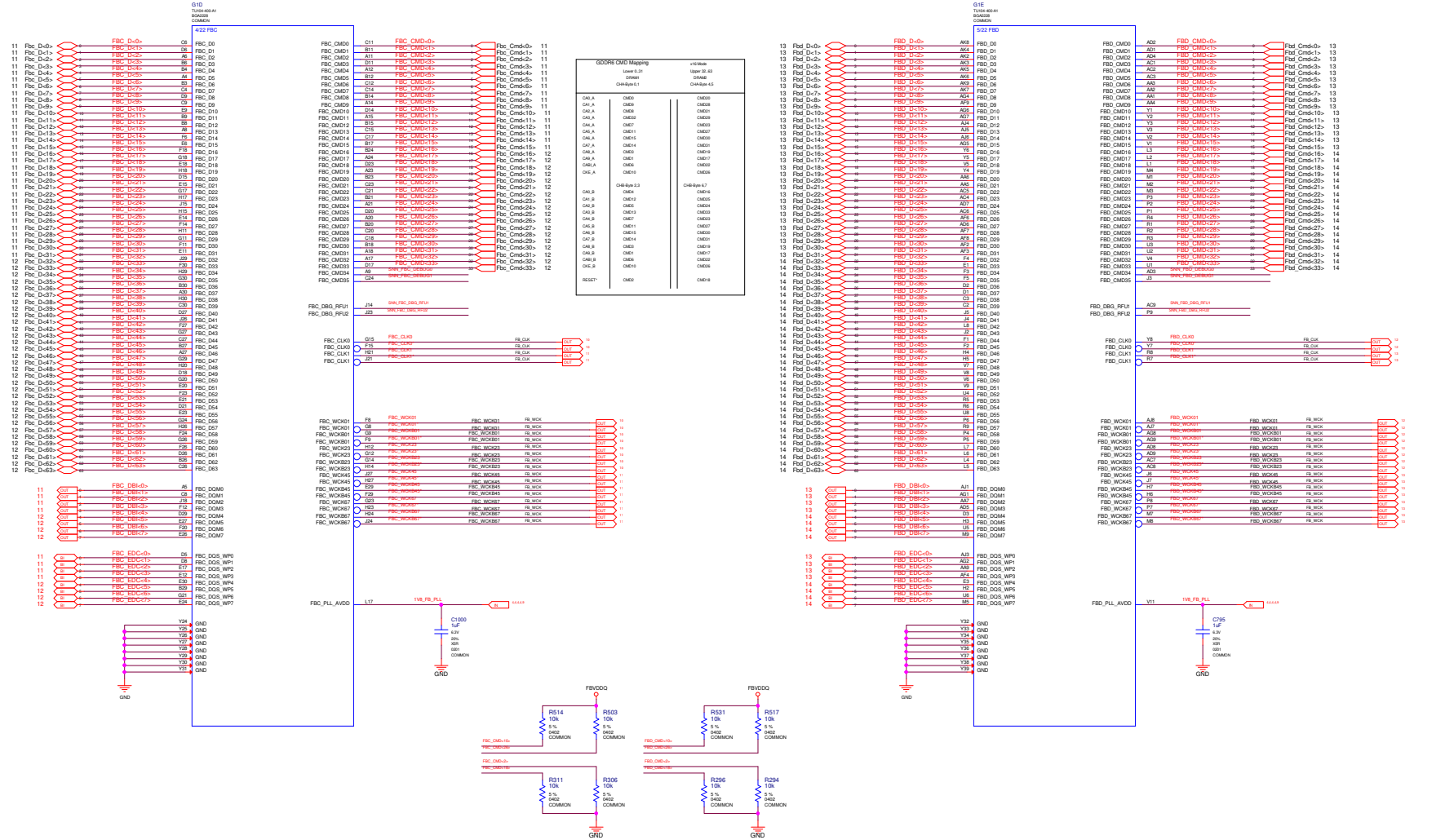
Page9: MEMORY: GPU Partition C/D



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PAGE DETAIL	MEMORY: GPU FB_CD

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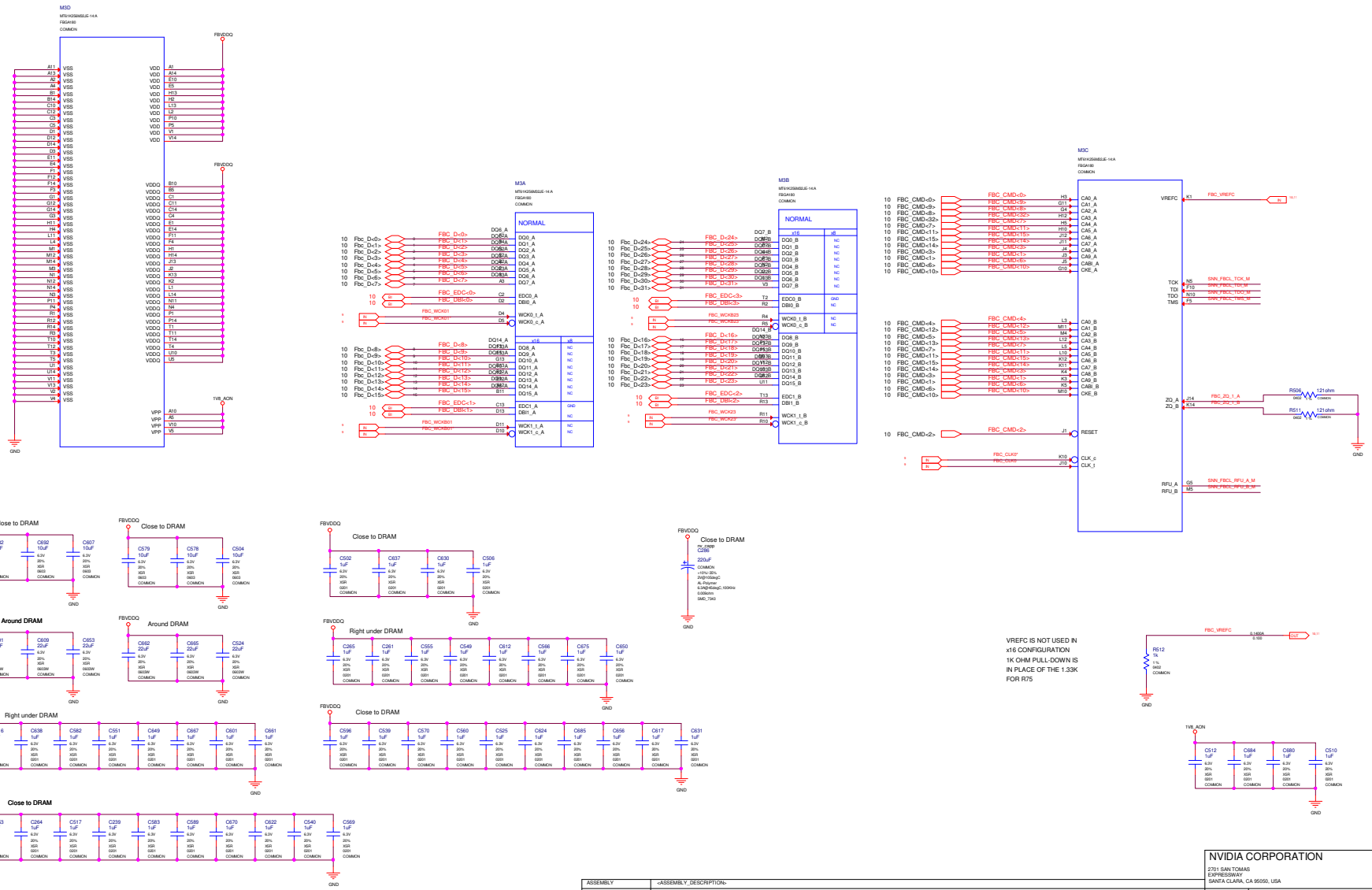
Page10: MEMORY: FBC Partition 31..0



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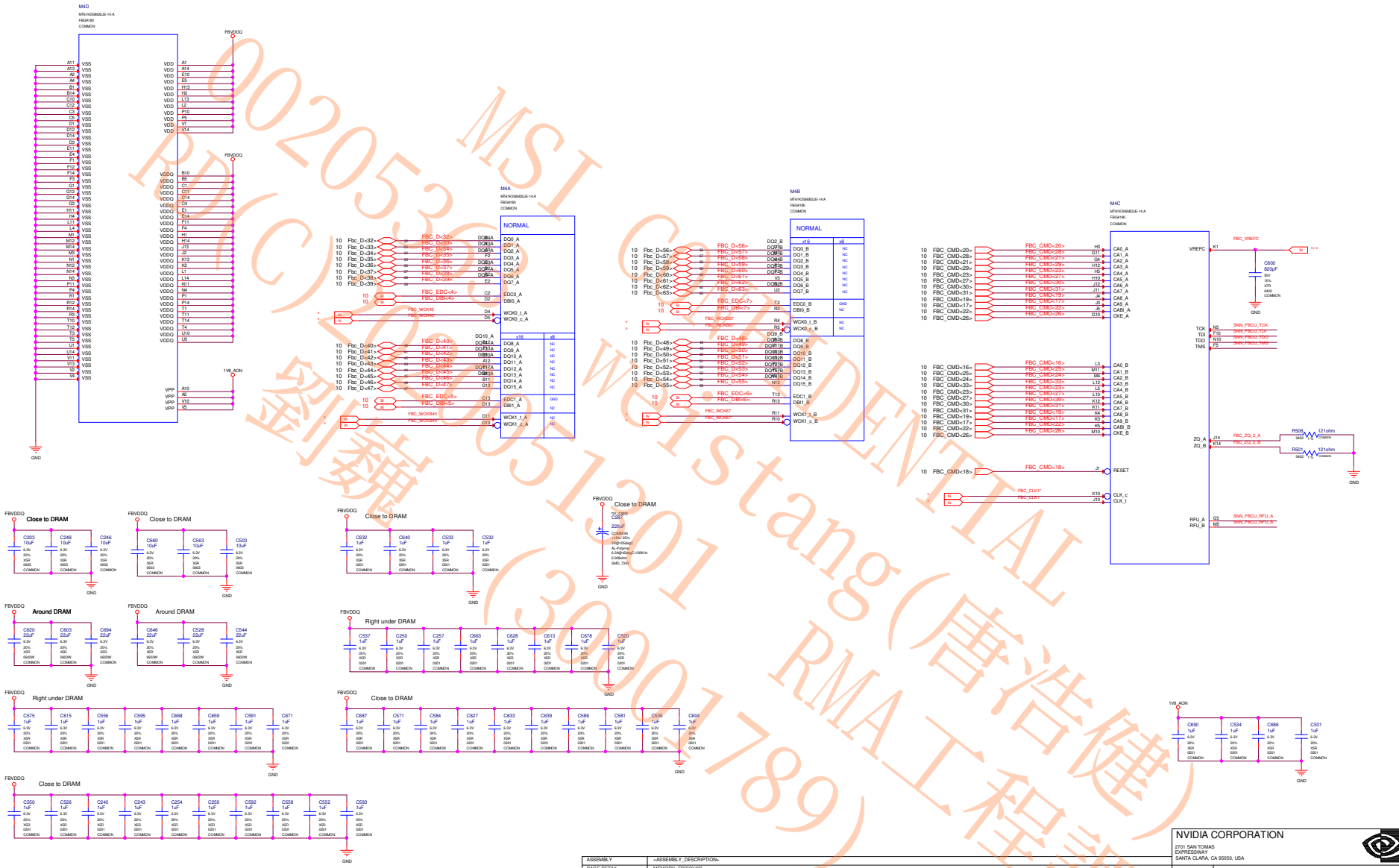
Page11: MEMORY: FBC Partition 63..32



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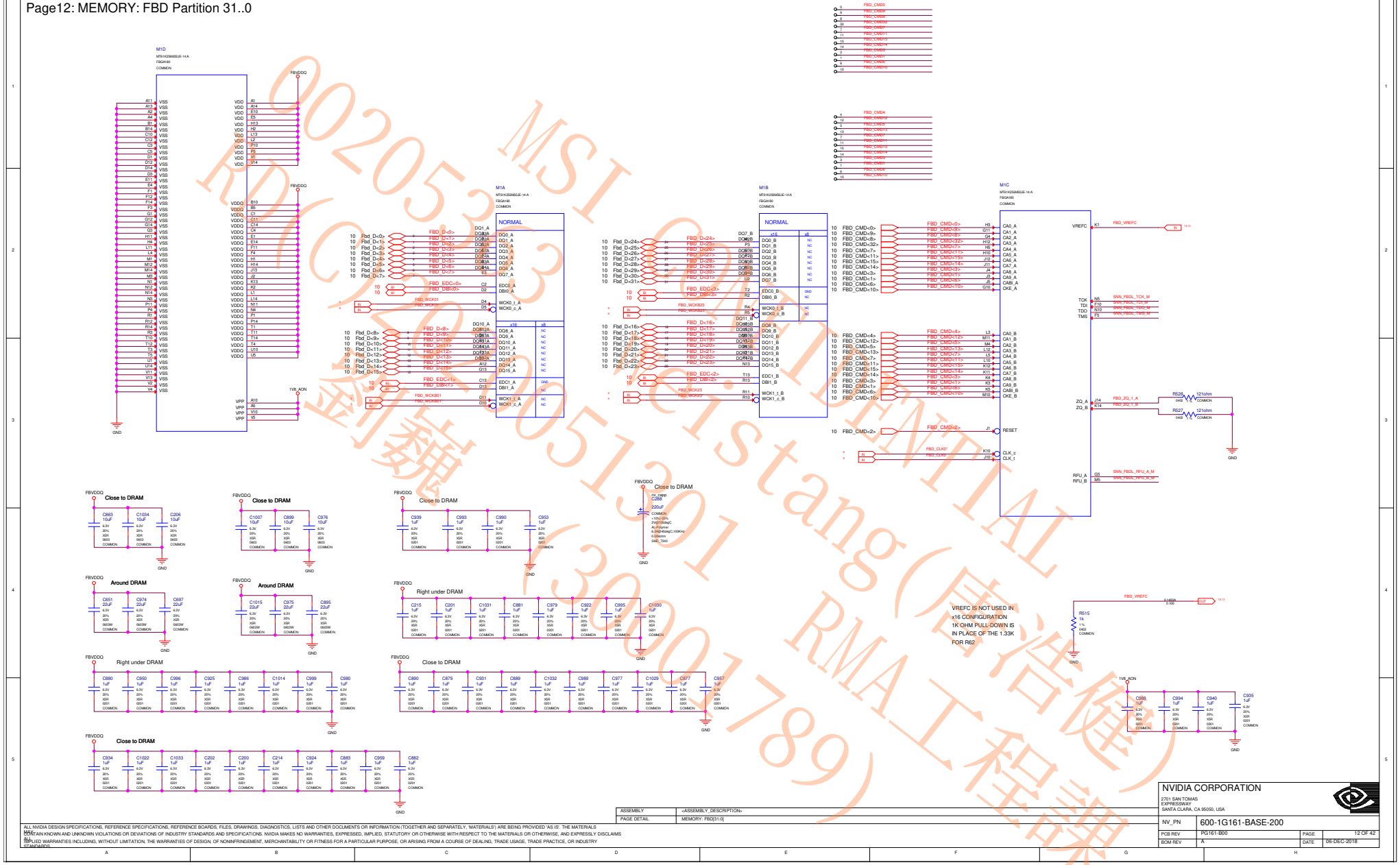
RDC(02)(2001)(3000178)
RMA工程課
劉建 (3000178)

Page12: MEMORY: FBD Partition 31..0



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
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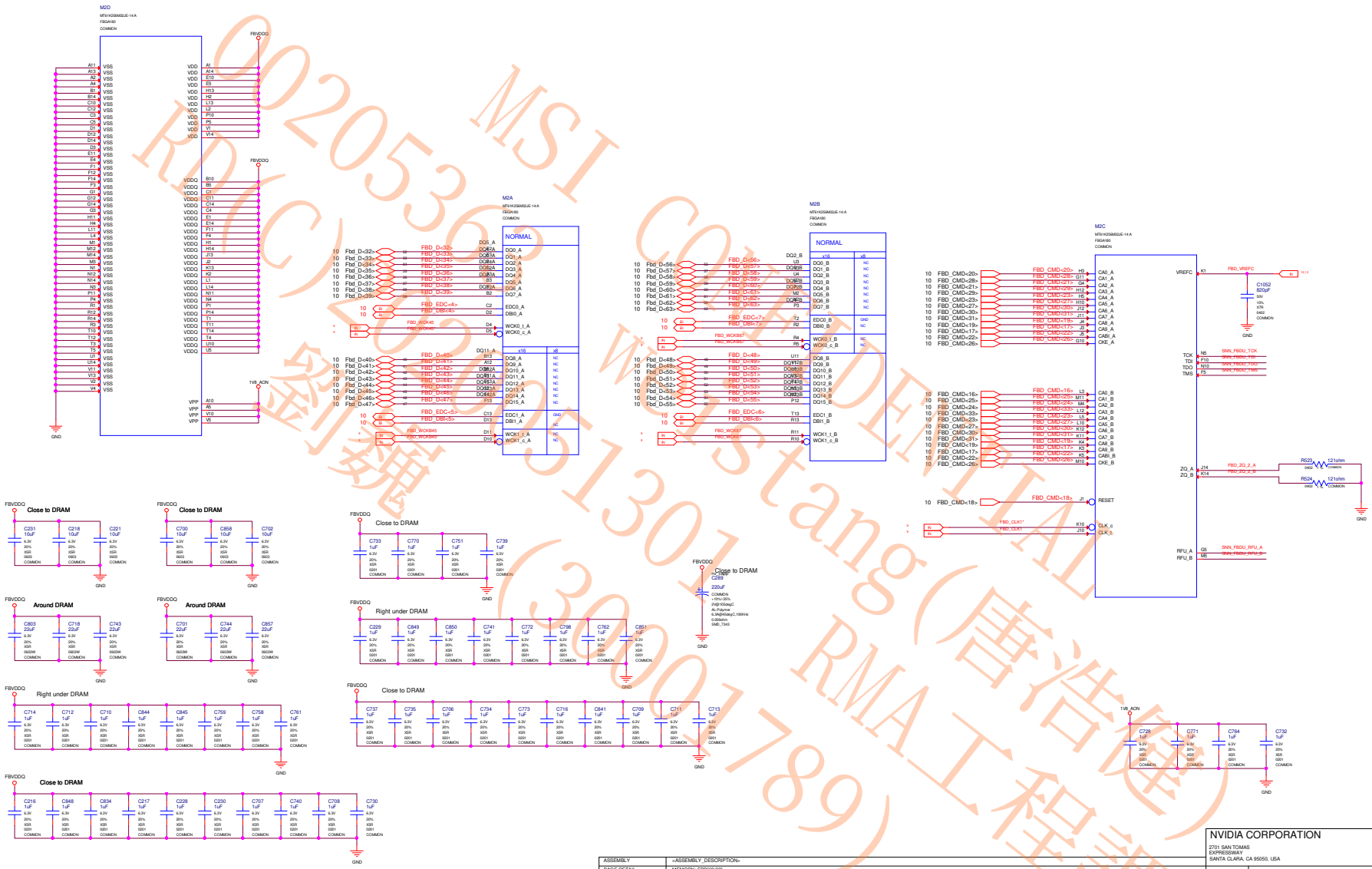
RD(Christang(唐治隆)
0205301 13001789)
刘辅(RMA工程师)

Page13: MEMORY: FBD Partition 63..32



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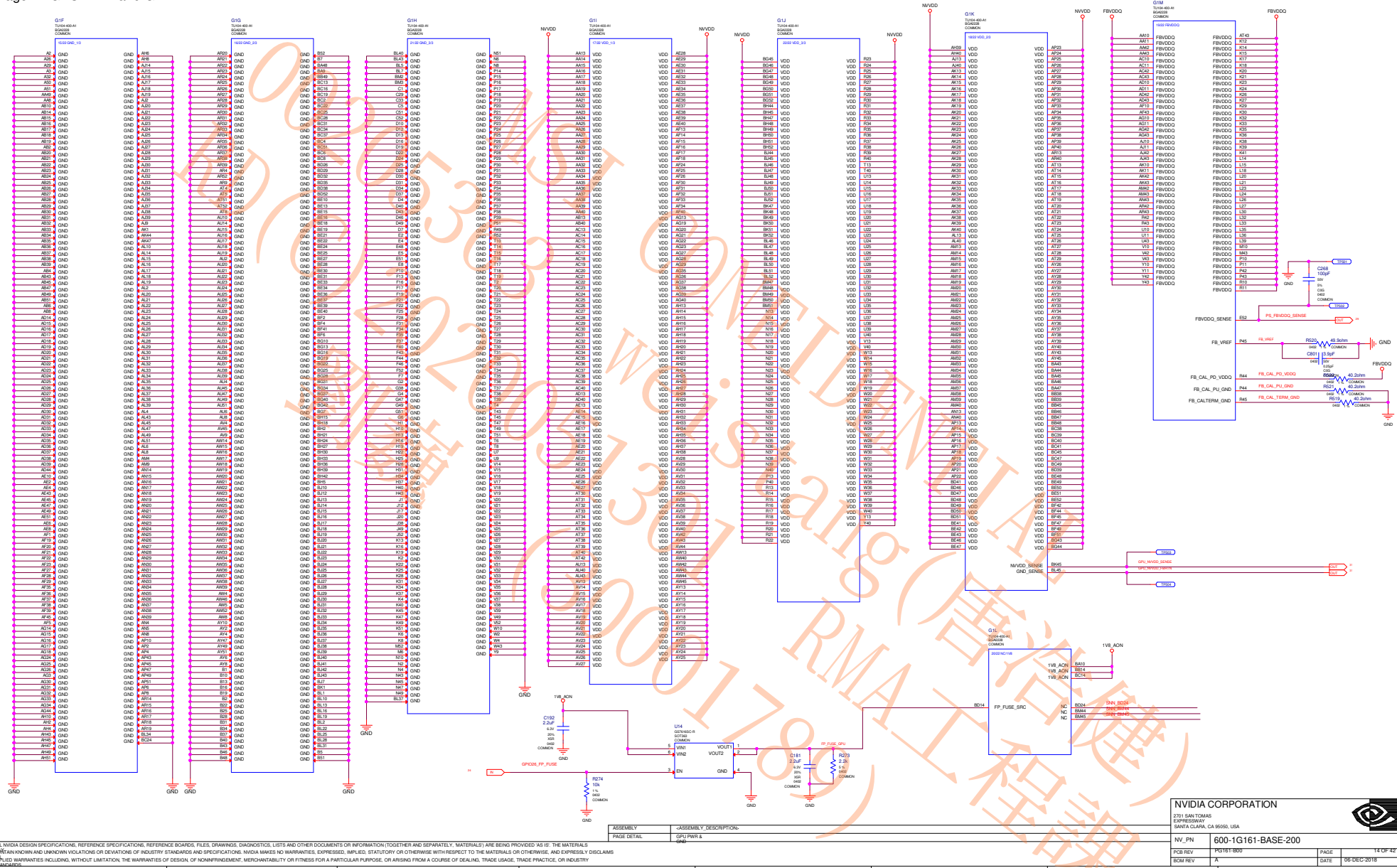
RDC (Dongguan) Mustang (Dongguan)
RMA工程課
(300017789)
00205361301
副本

Page14: GPU PWR and GND



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND

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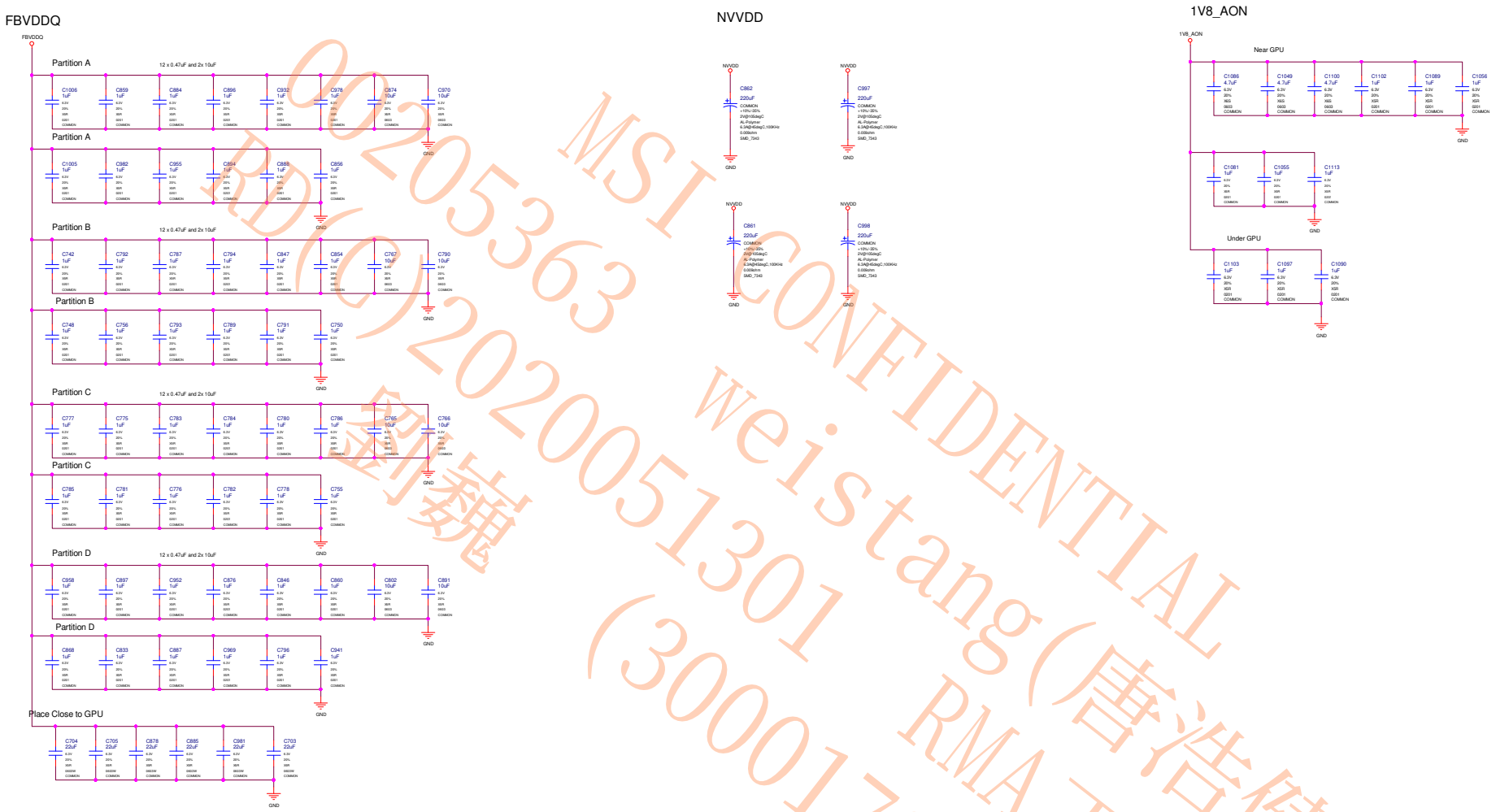
Page15: GPU DECOUPLING 1



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING 1

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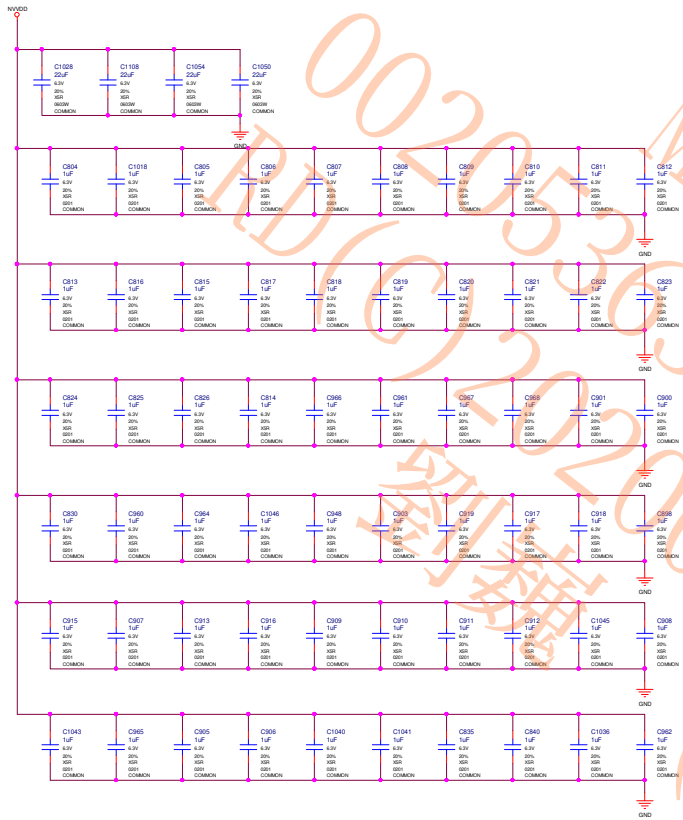
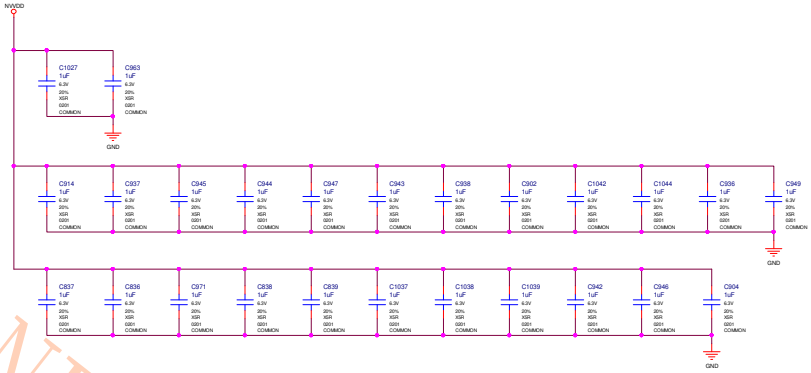
Page16: GPU DECOUPLING 2

NVVDD





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PAGE DETAIL	GPU DECOUPLING 2

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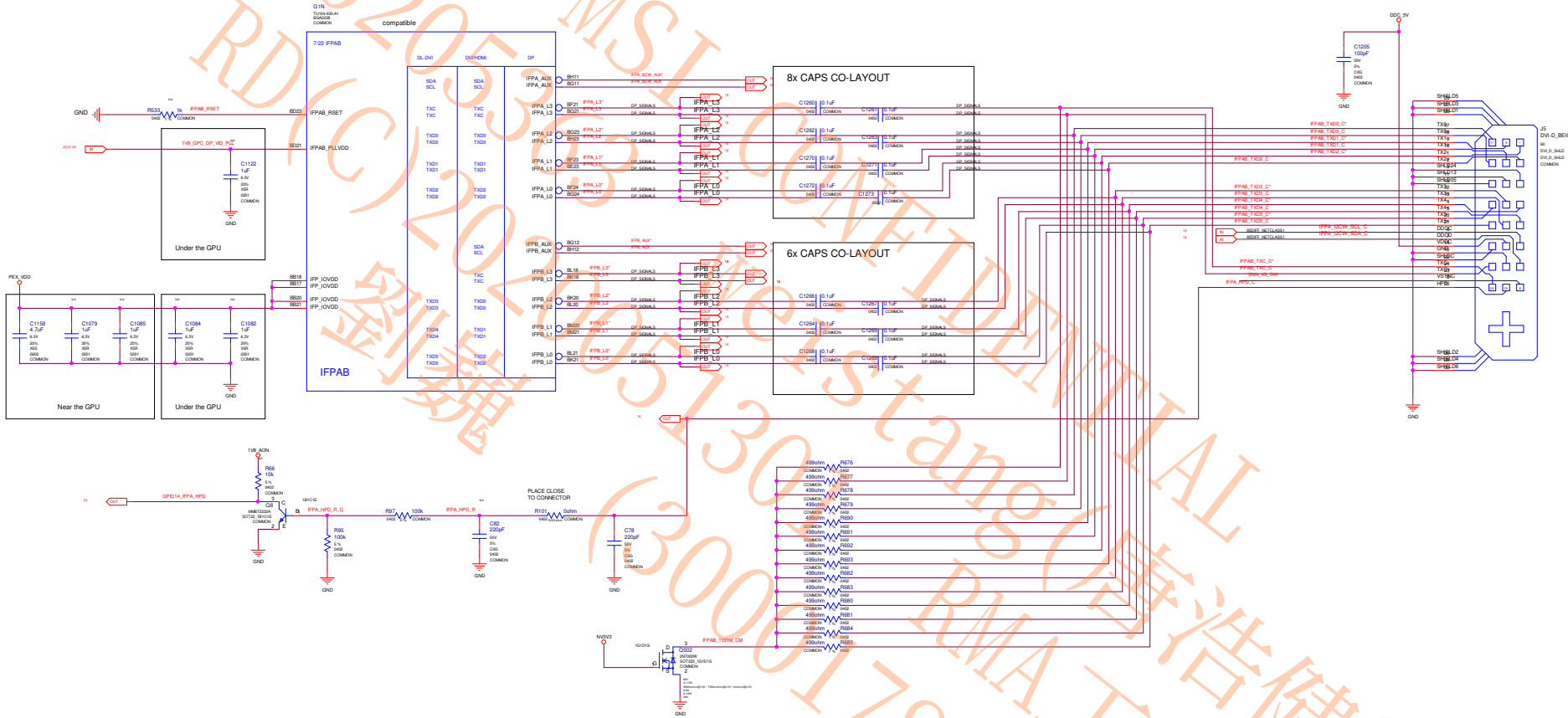
Page17: IFPAB DVI-D-DL



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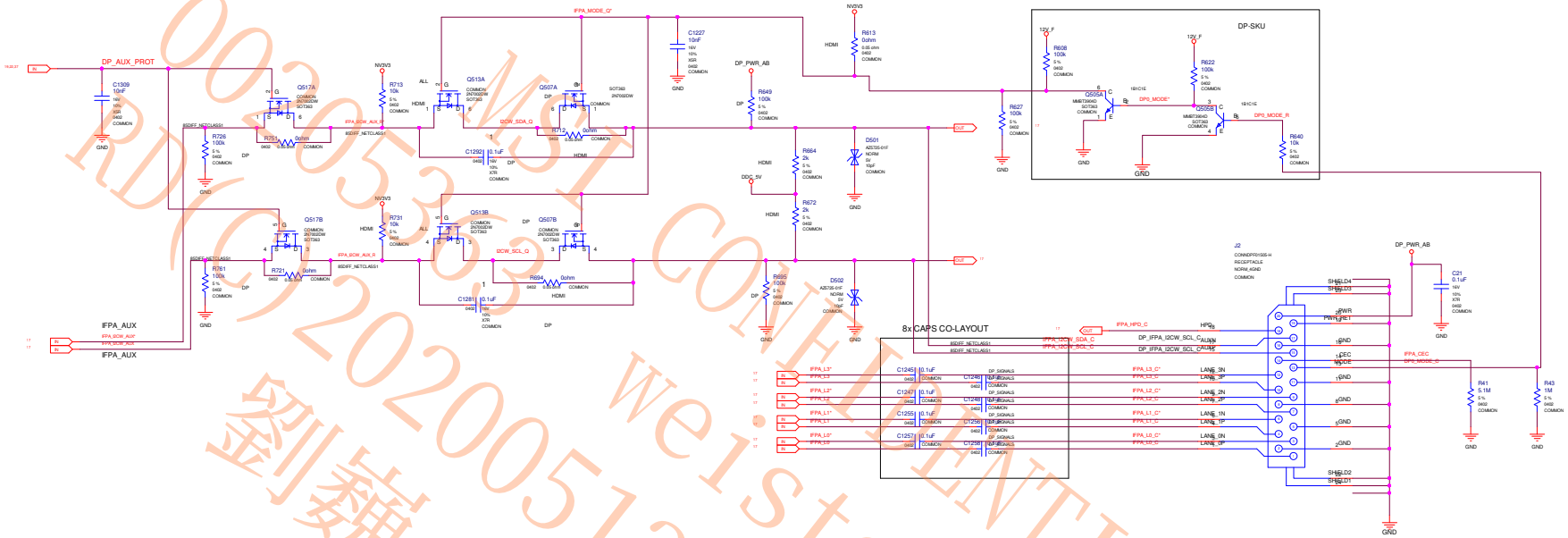
Page18: IFPA DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPA DP

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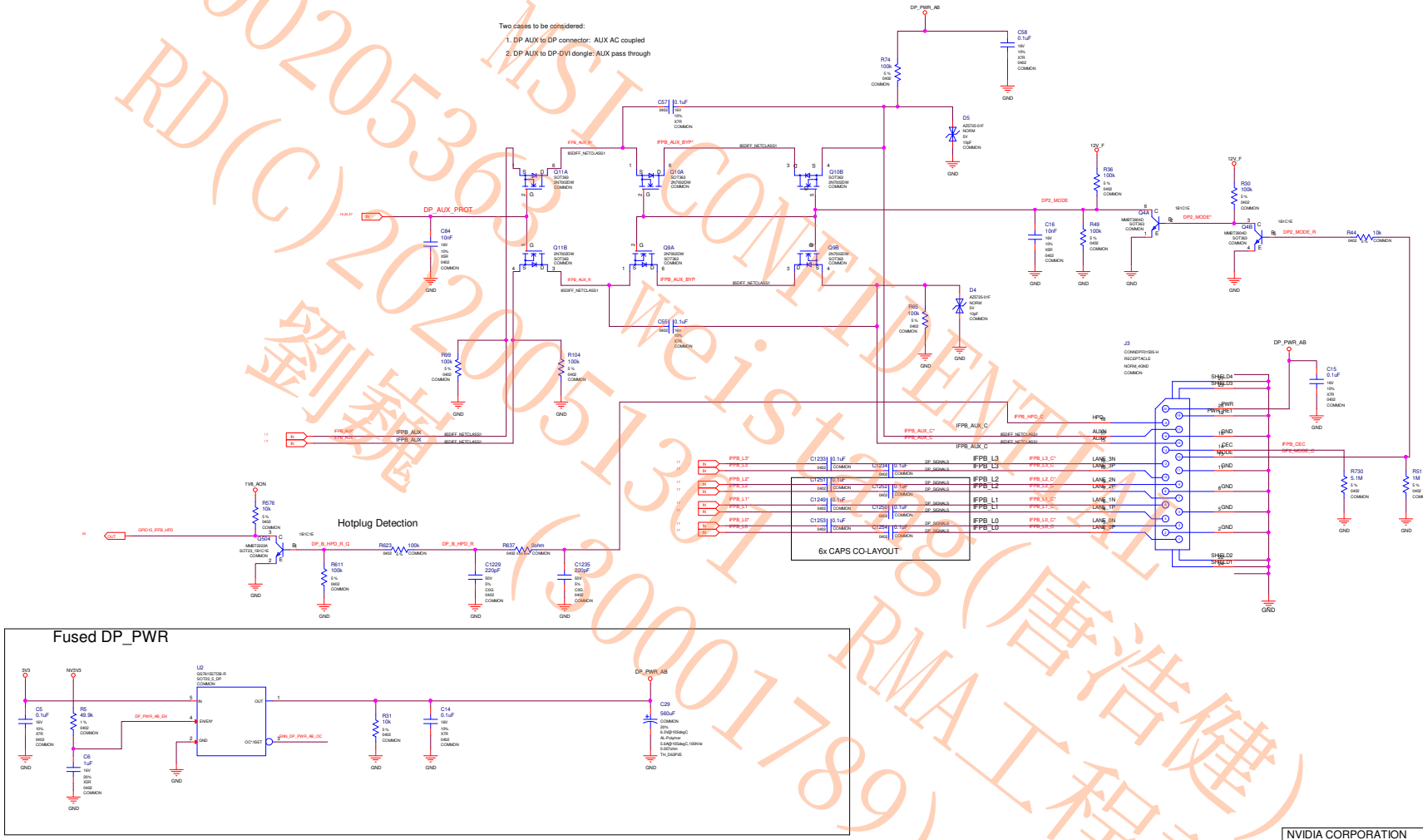
Page19: IFPB DP



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PAGE DETAIL	IO: IFPB DP

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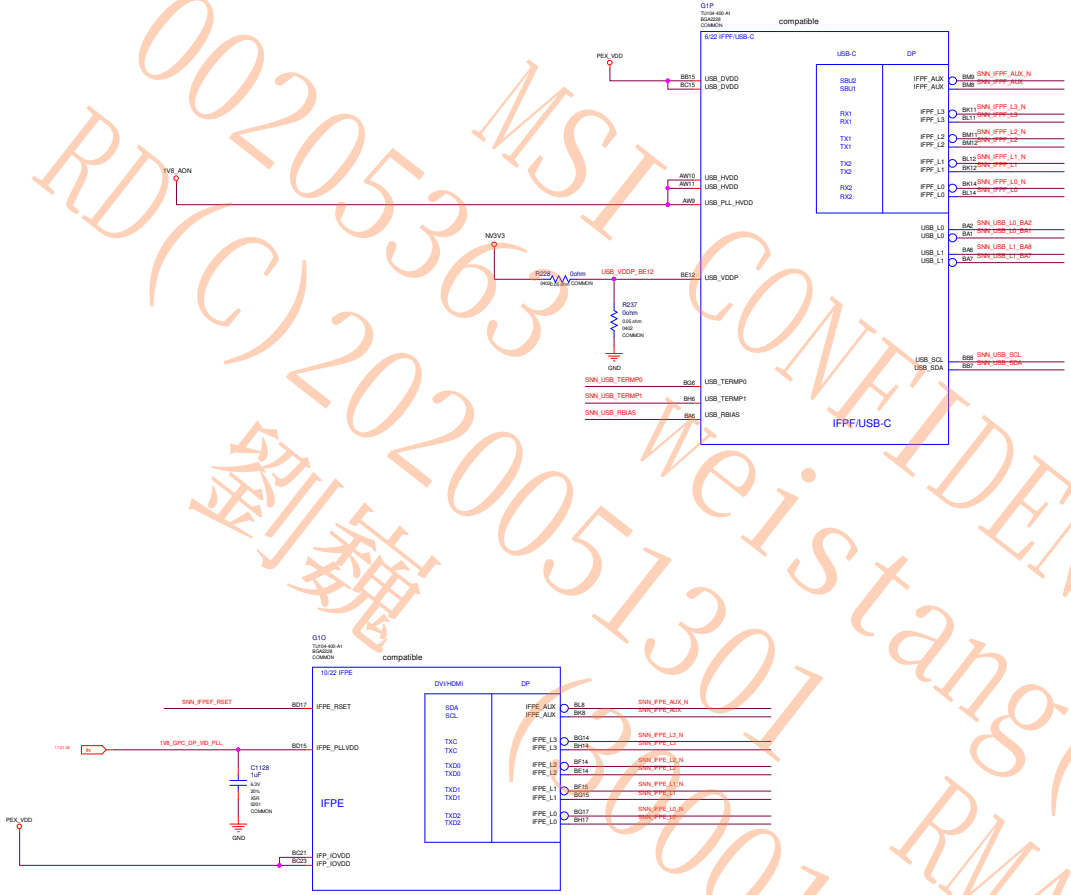
Page20: IFPE & IFPF NC



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IO: IFPE & IFPF NC

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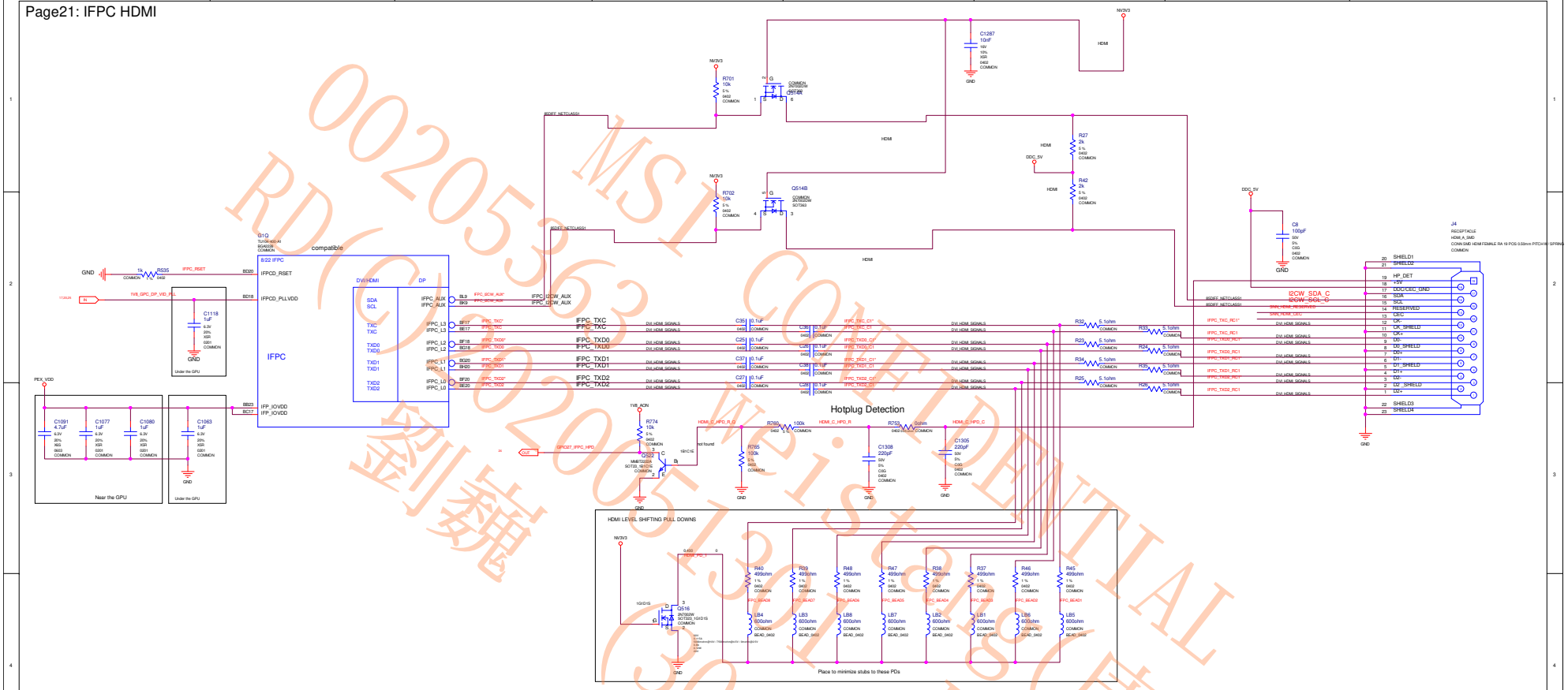
Page21: IFPC HDMI



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPC HDMI

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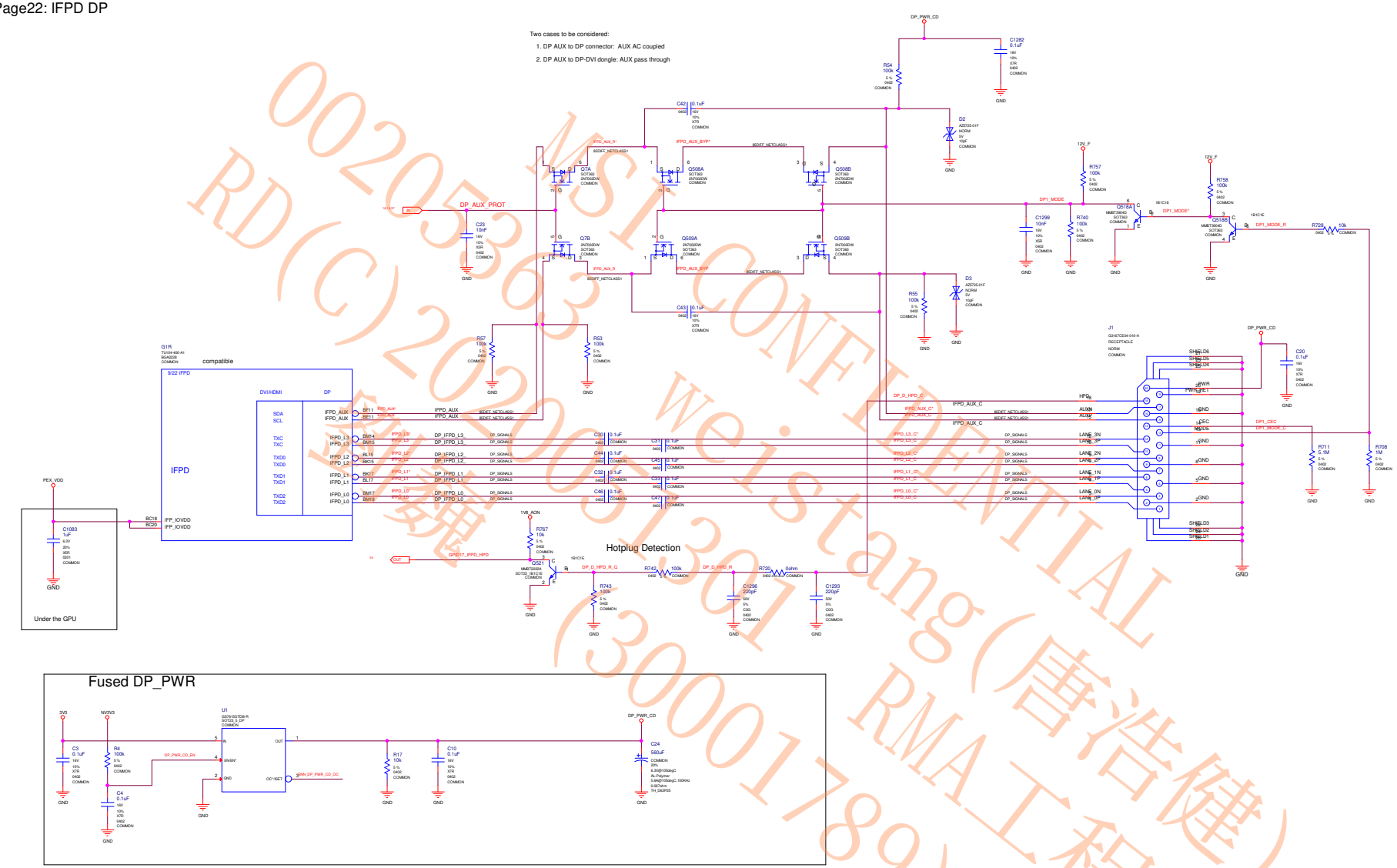
Page22: IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPD DP

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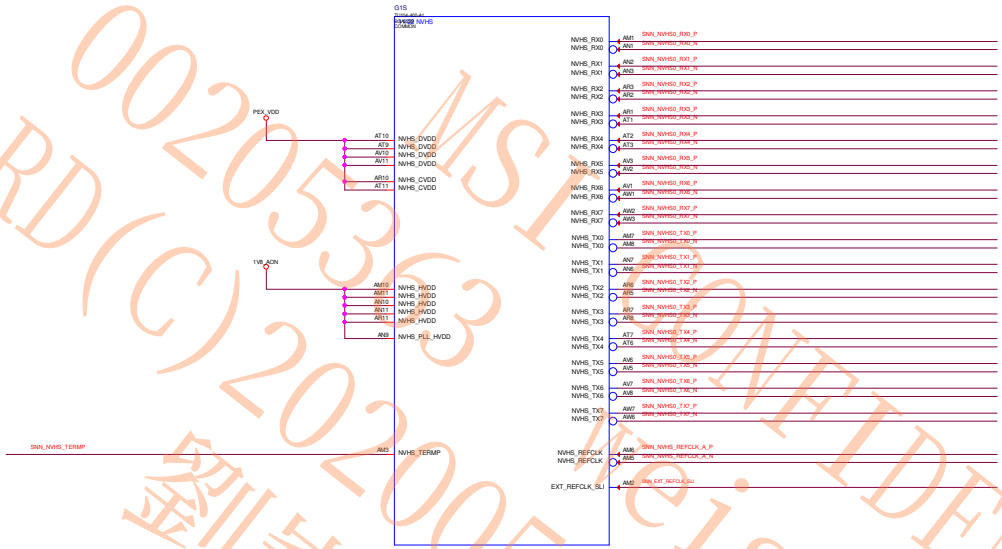
Page23: NVHS INTERFACE AND FRAME LOCK



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: NVHS INTERFACE AND FRAME LOCK

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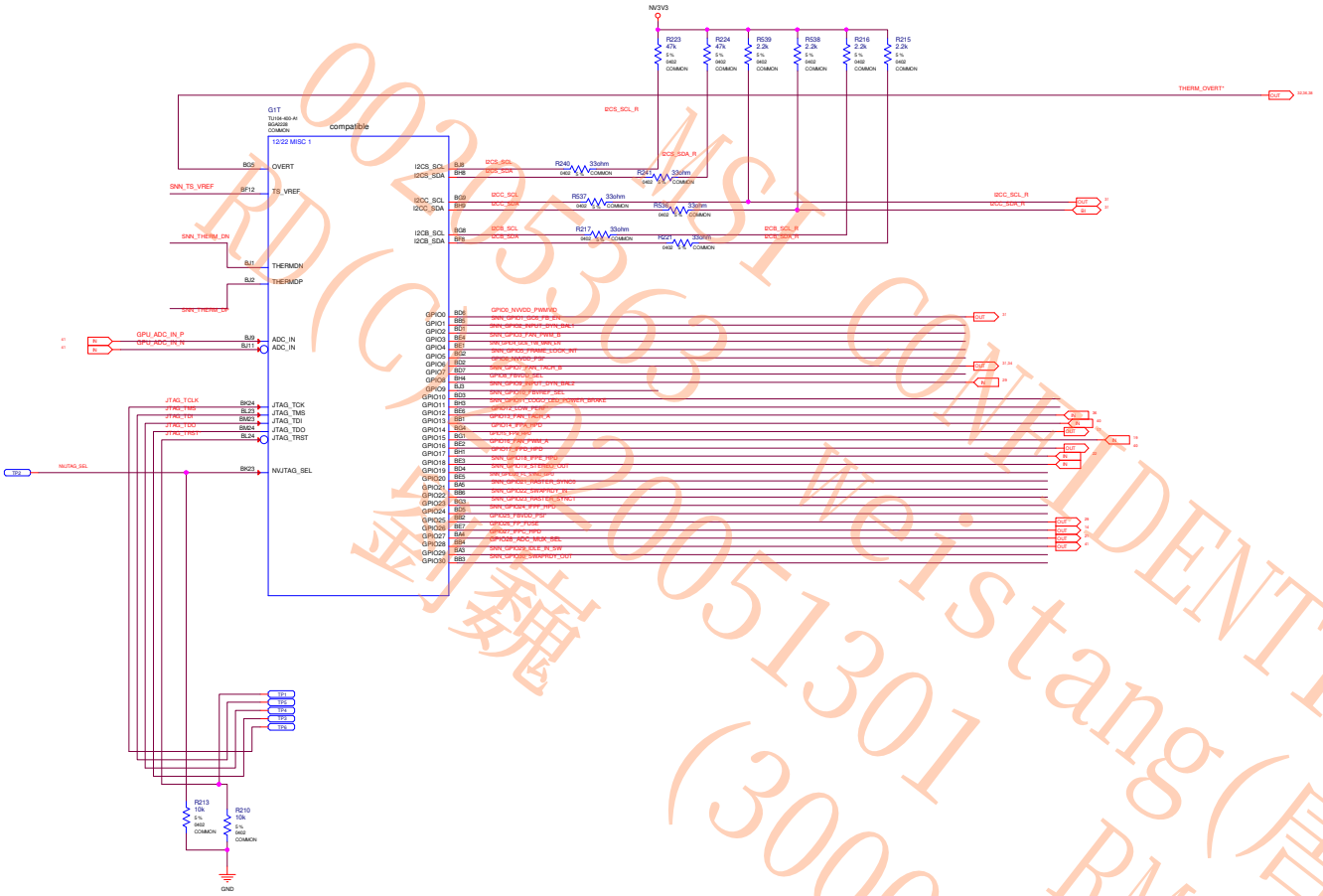
Page24: MISC1: JTAG, GPIO, ADC, I2C, OVERT



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: JTAG,GPIO,ADC,I2C,OVERT

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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]FS_OVERT	1:ENABLE 0:DISABLE	DEFAULT
L	L	L	XXX1	FS_OVERT ENABLE	
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

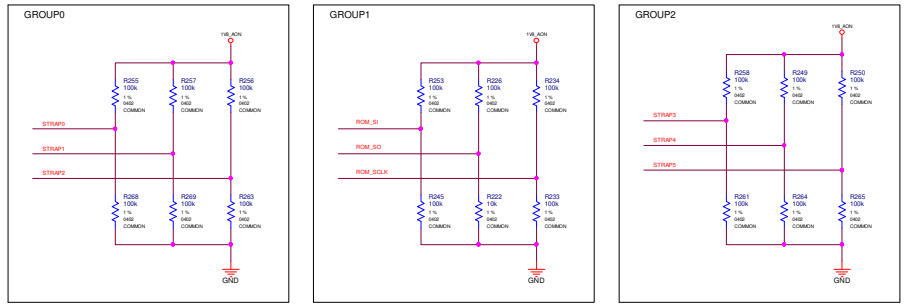
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

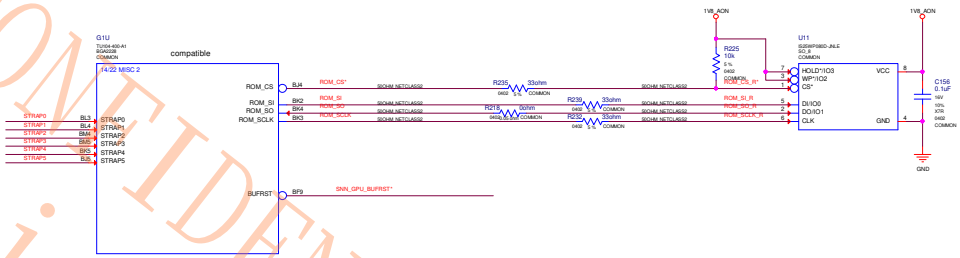
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

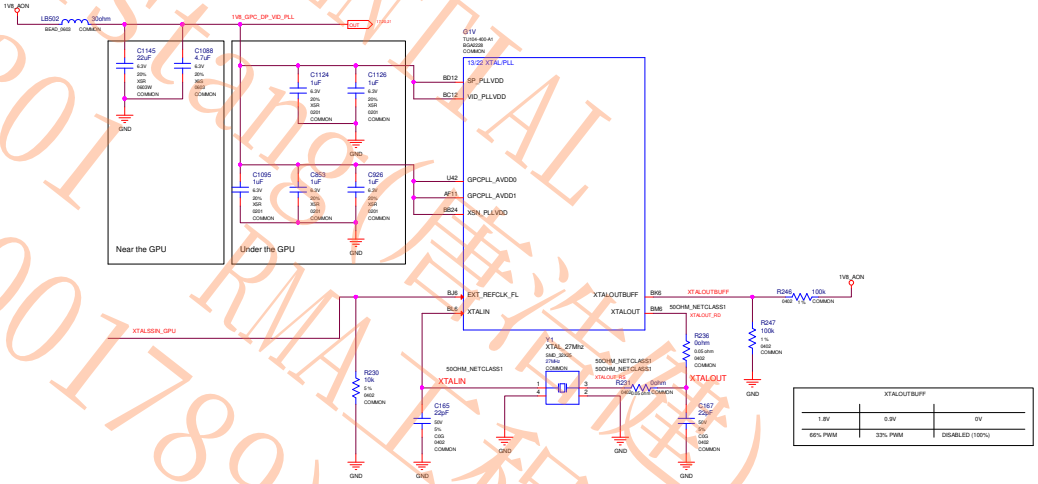
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL,STRAPS

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(3000178)
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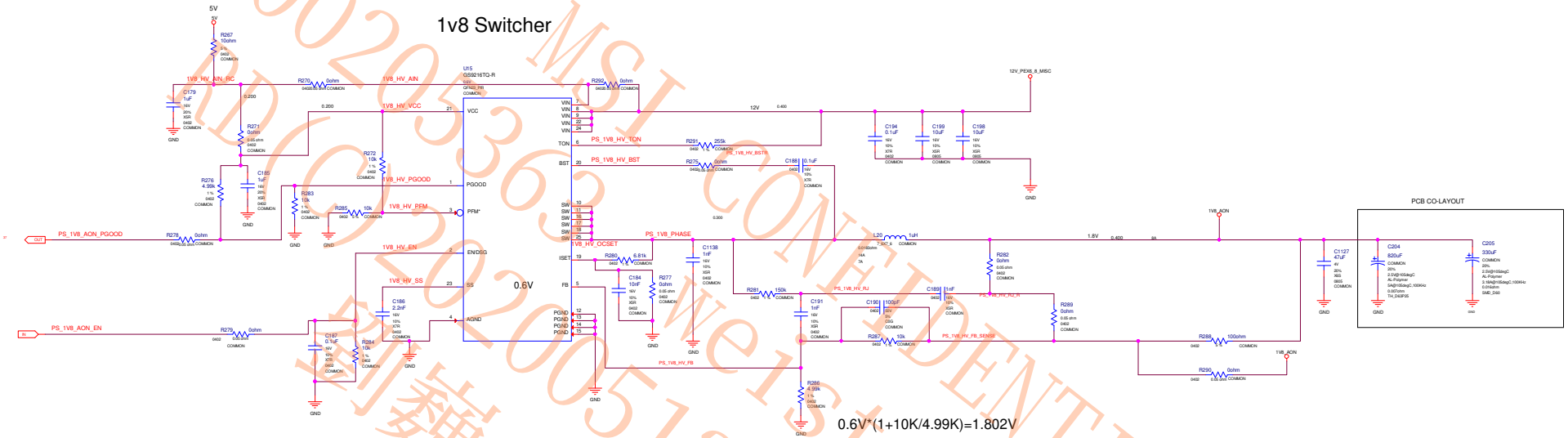
Page26: PS: 1V8_AON



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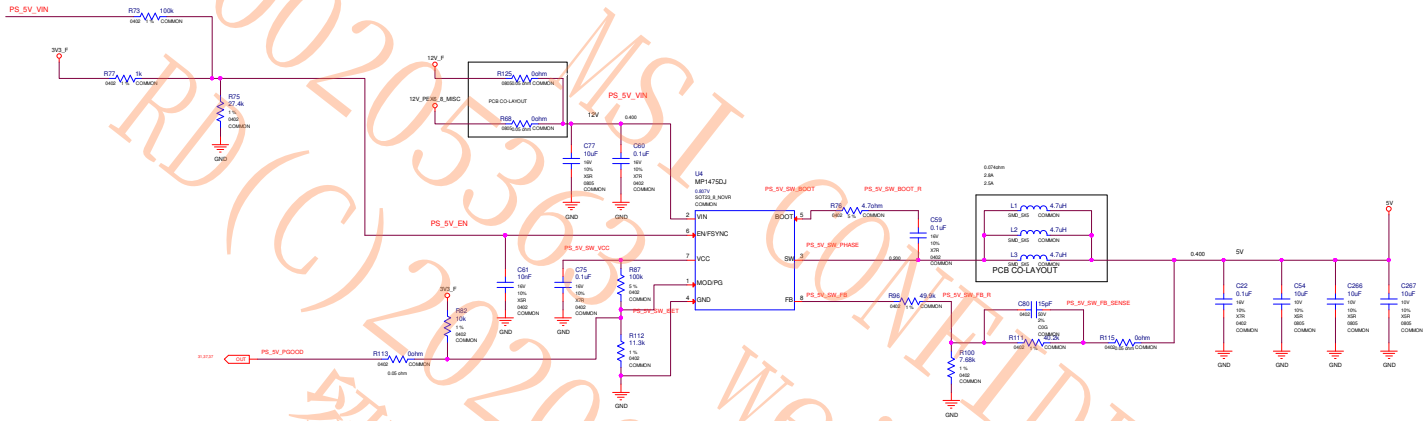
Page27: PS: 5V



0.8V*(1+40.2K/7.68K)=4.9875V

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 5V

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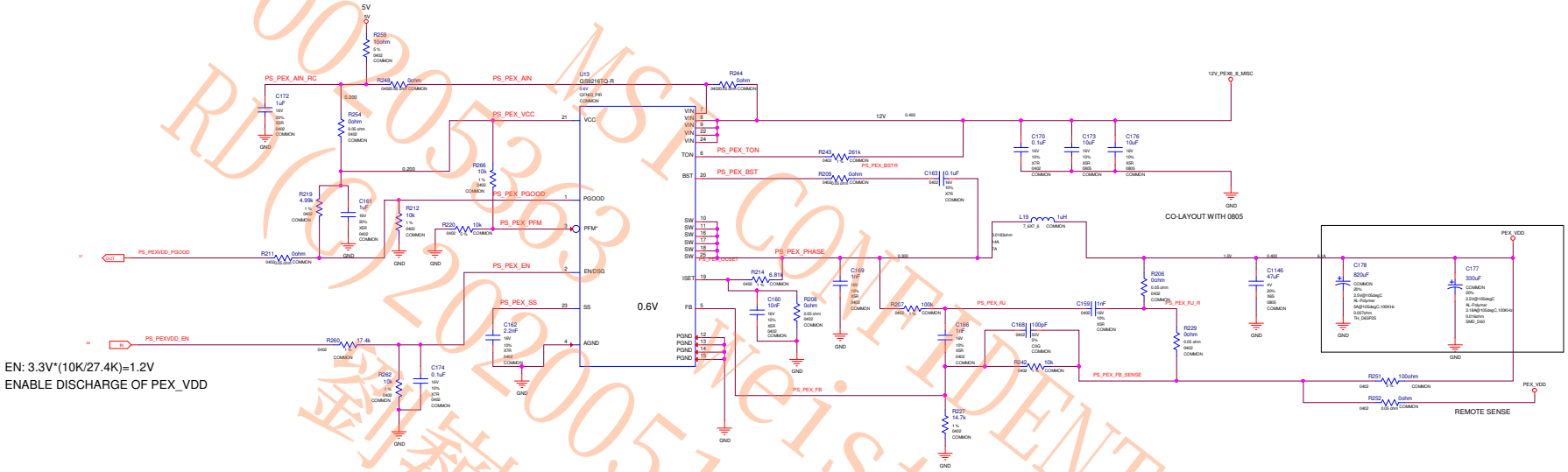
BOM REV	A	DATE	06-DEC-2018

Page28: PS: PEXVDD



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEXVDD

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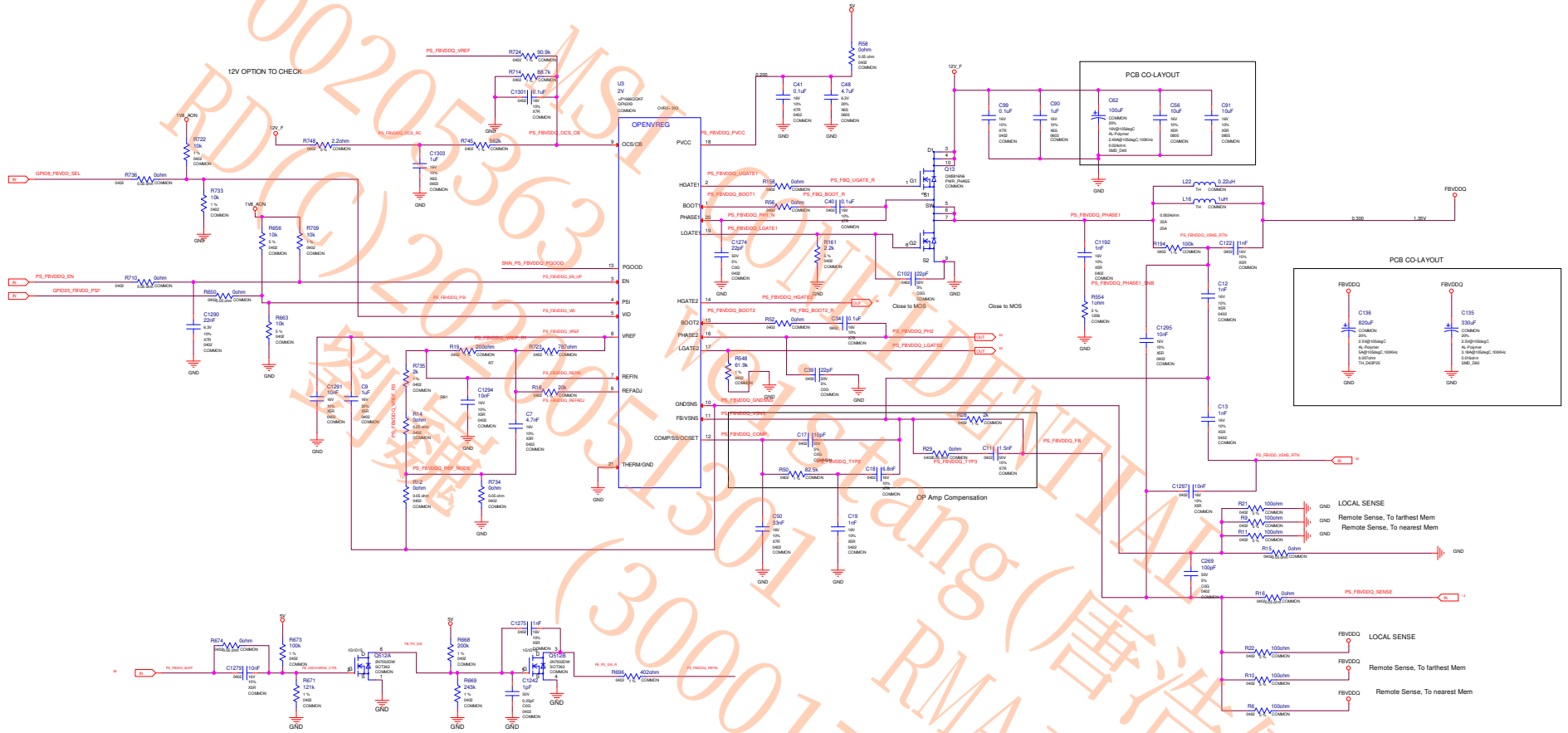
Page29: PS: FBVDDQ



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PAGE DETAIL	PS: FBVDDQ

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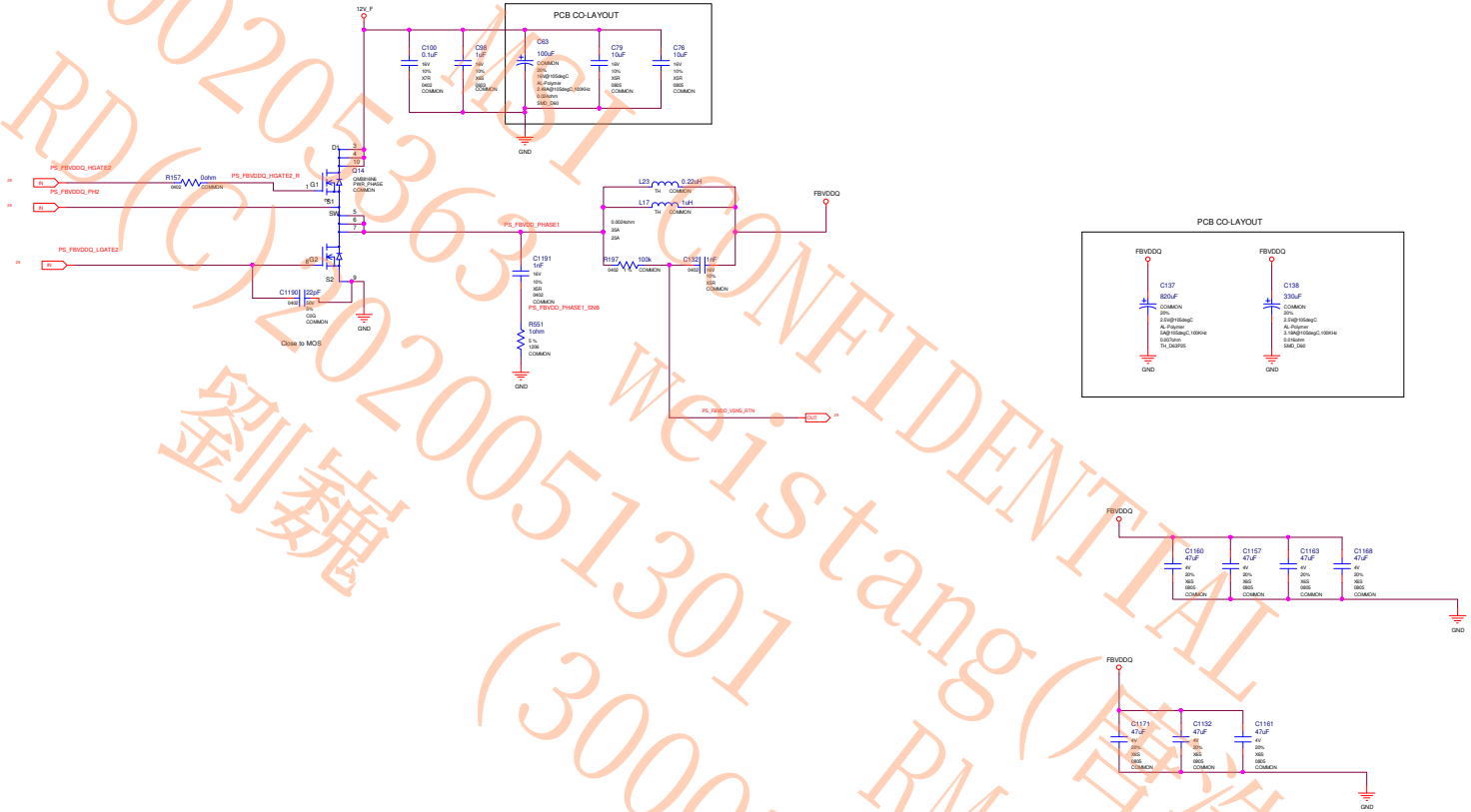
Page30: PS: FBVDDQ PH2



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDDQ PH2

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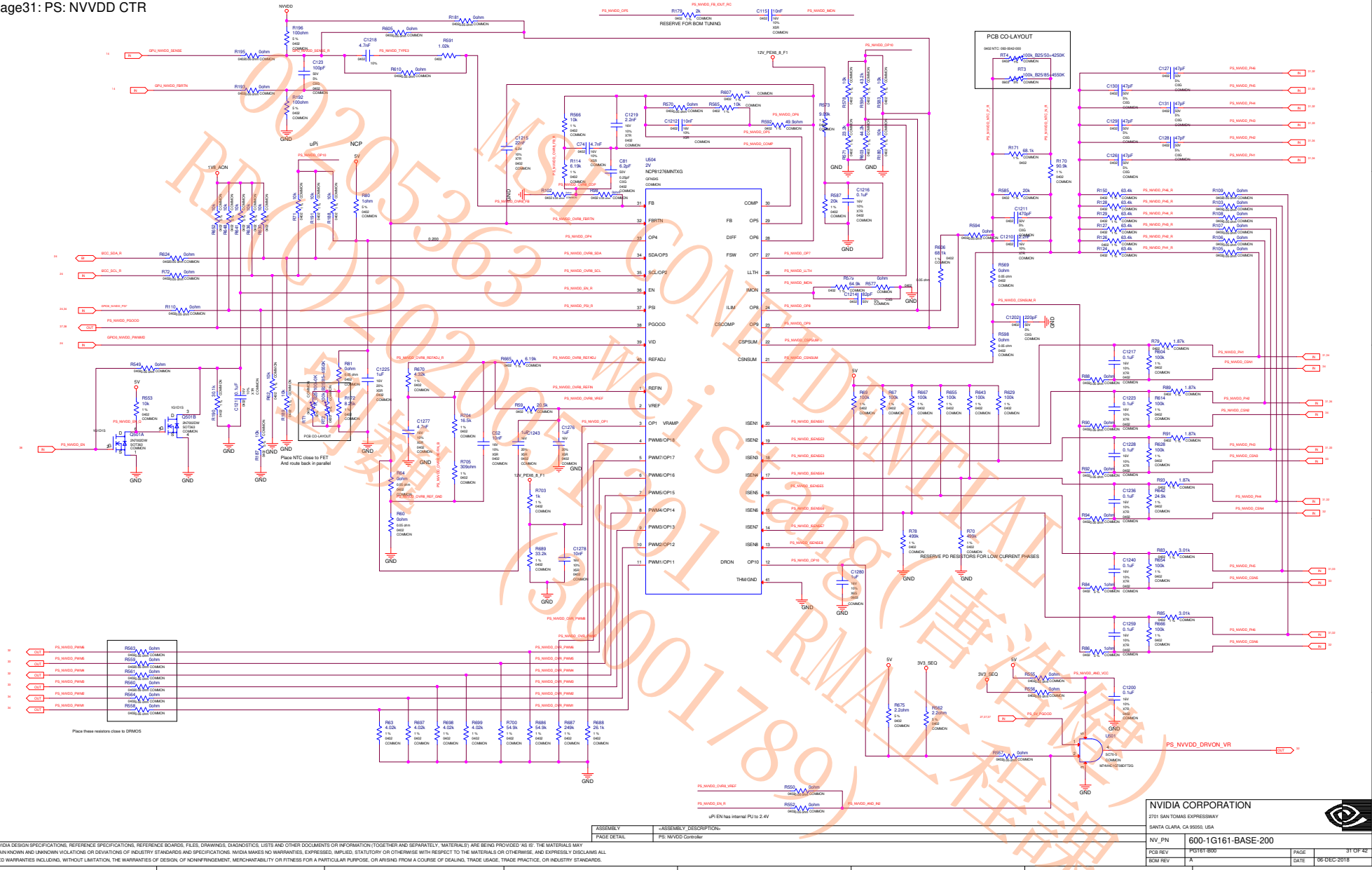
Page31: PS: NVVDD CTR



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PAGE DETAIL	PS: NVDD Controller

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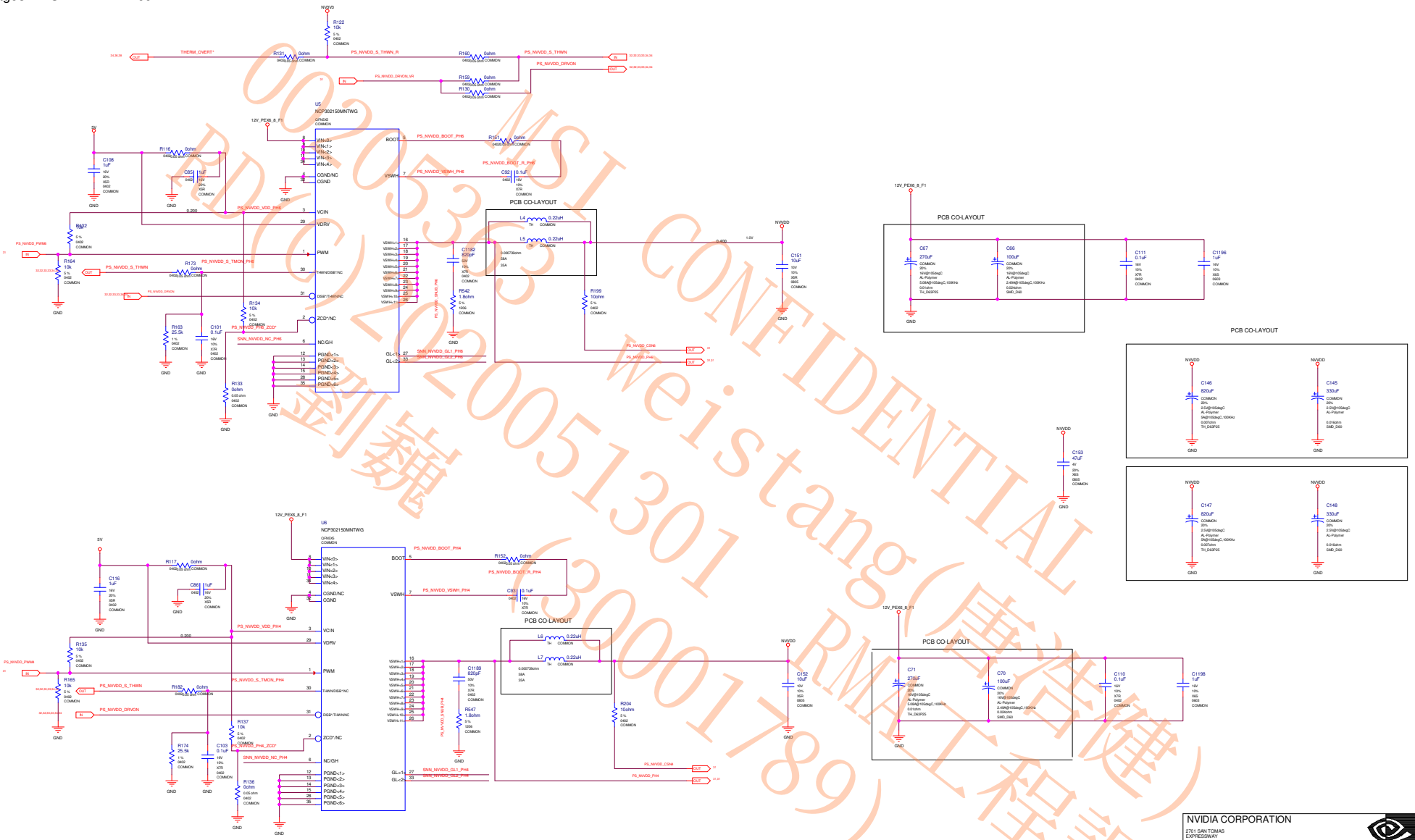
Page32: PS: NVVDD PH6&4



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PAGE DETAIL	PS: NVVDD Phase 6,4

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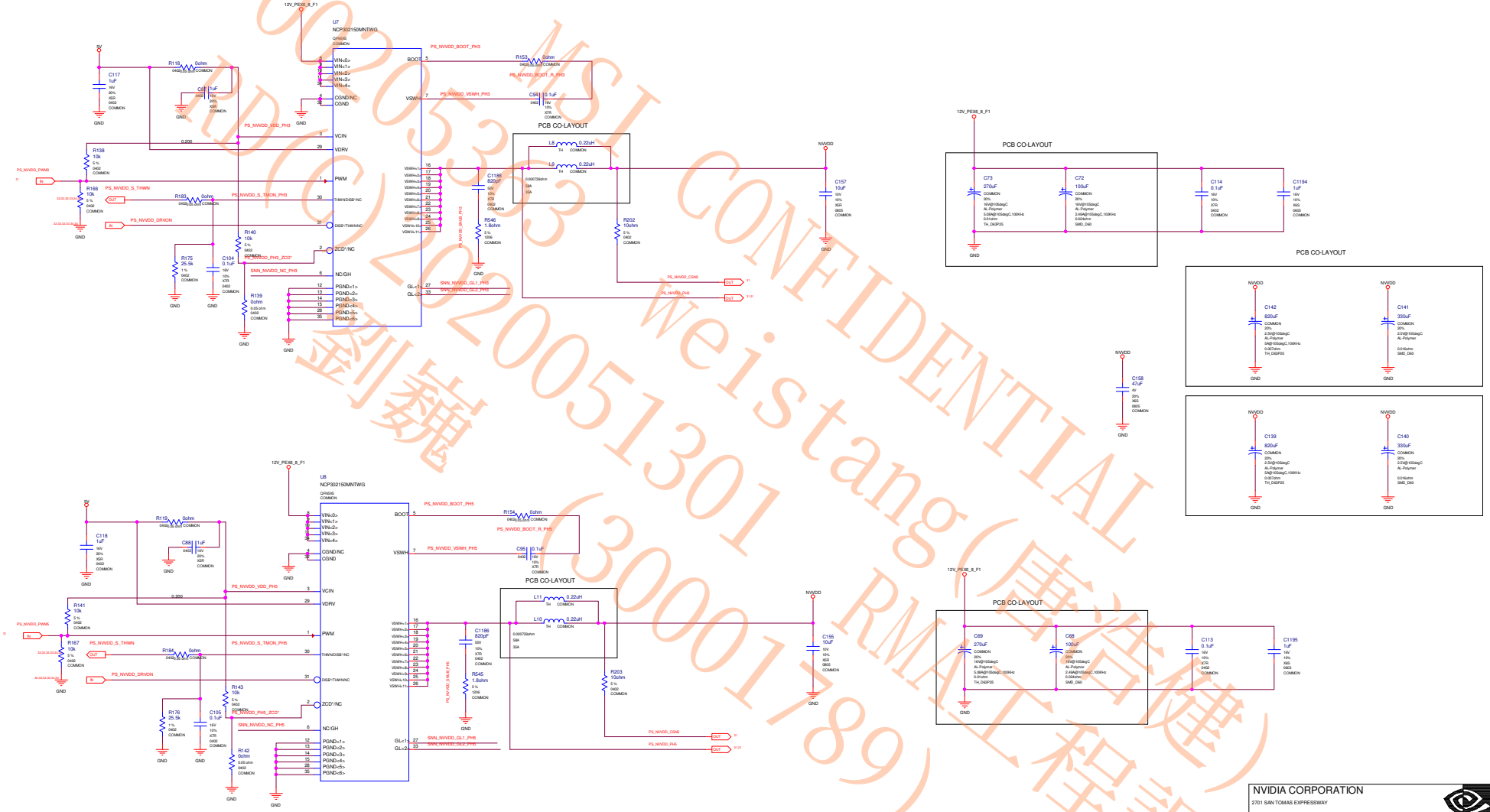
0605335 2020051301 (3000178)

Page33: PS: NVVDD PH3&5



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00053323
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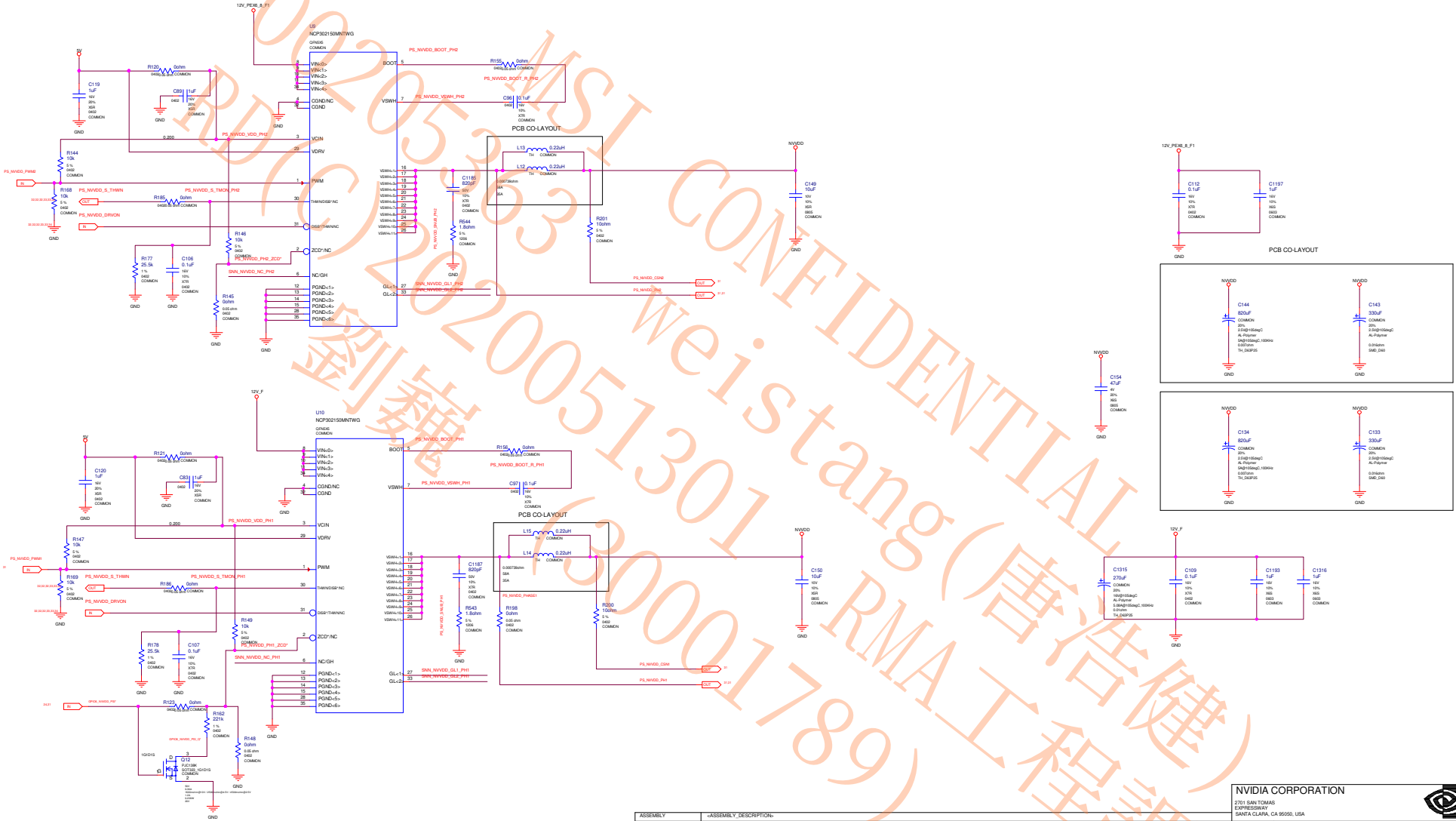
劉豬

Page34: PS: NVVDD PH2&1



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0205363 0200051301 (9000001789)
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 2,1

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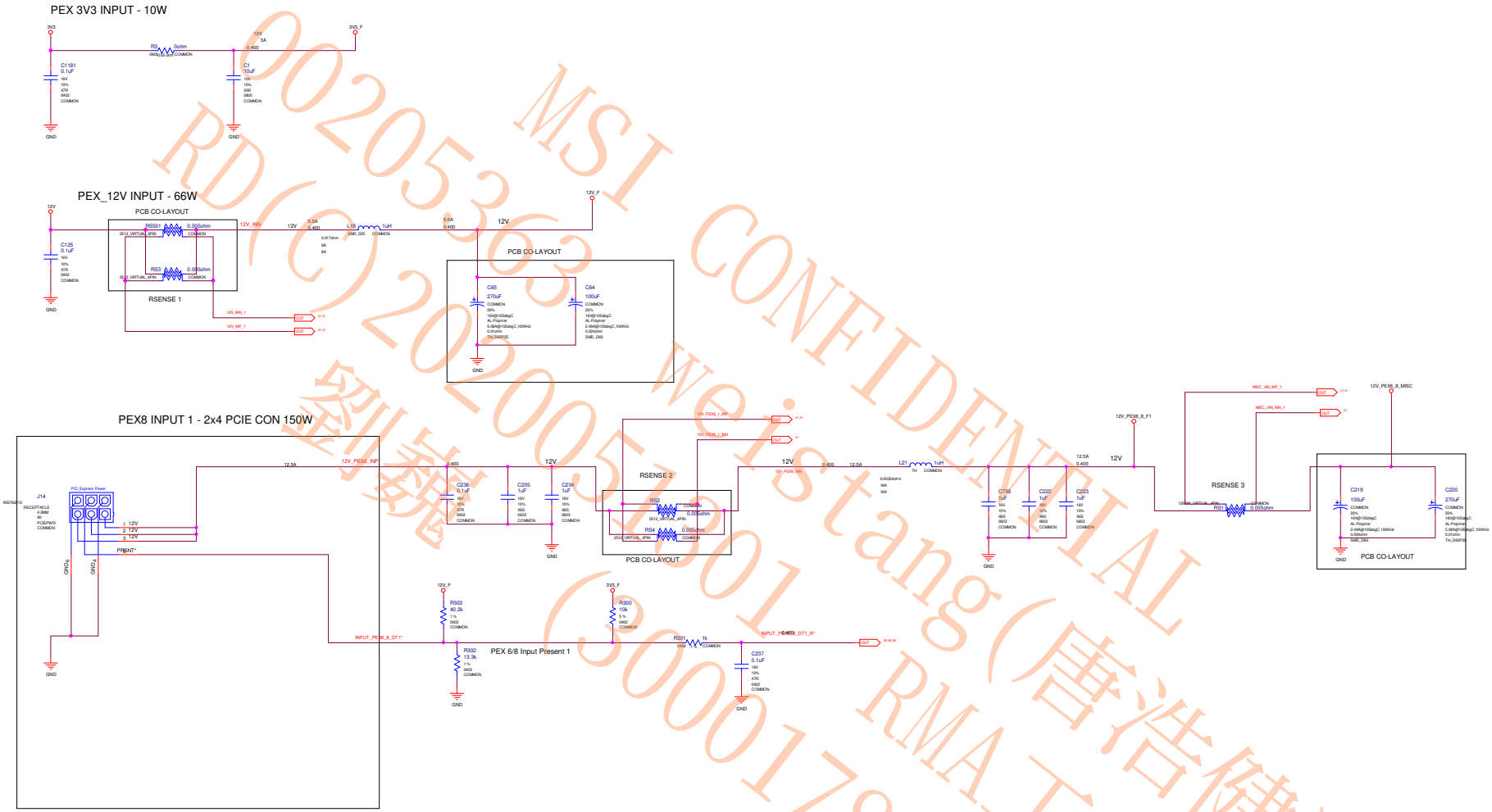
Page35: PS: PEX_INPUT, 12V_EXT_INPUT, FILTERING



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RD(C)20200529001
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEX_INPUT, 12V_EXT_INPUT, FILTERING

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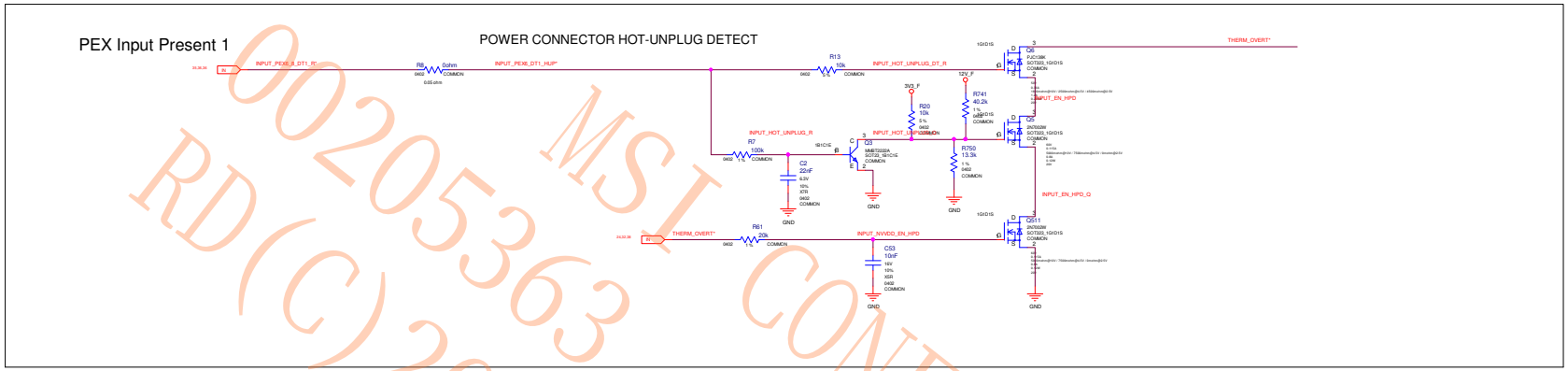
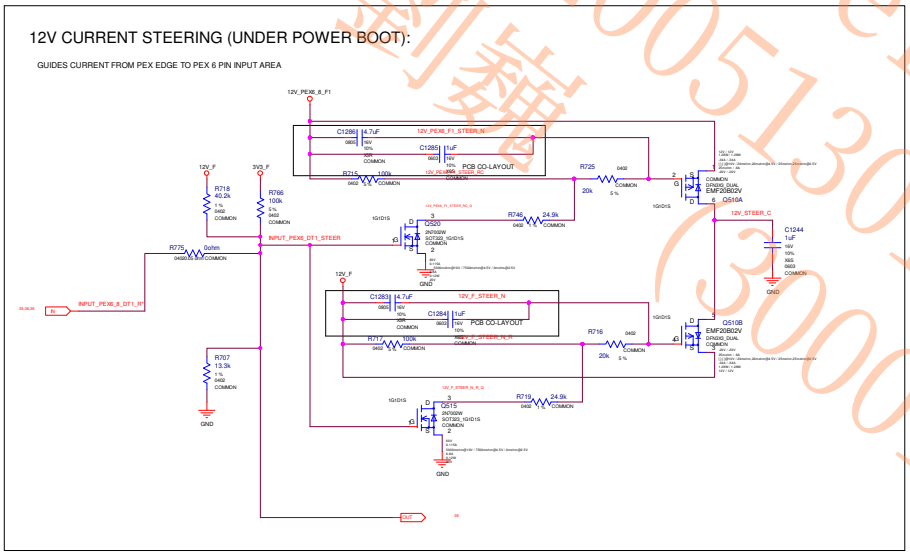
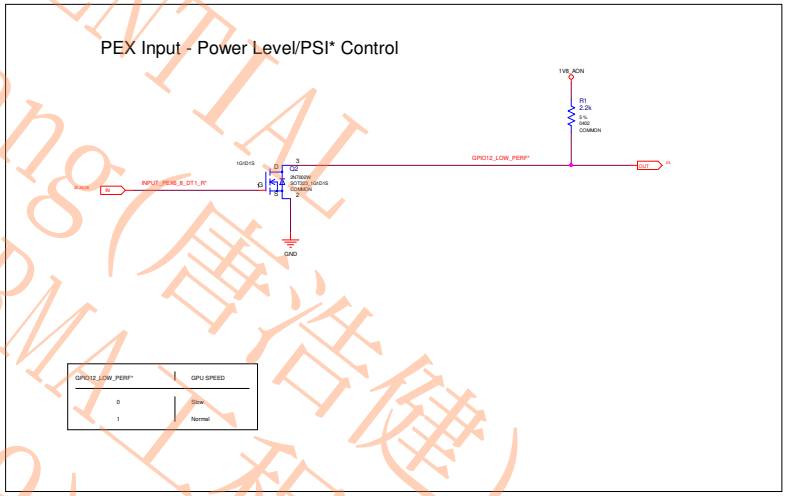
Page36: PS: CURRENT STEERING, UNDER POWER BOOT, HOT-UNPLUG







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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: CURRENT STEERING,UPB,HOT-UNPLUG

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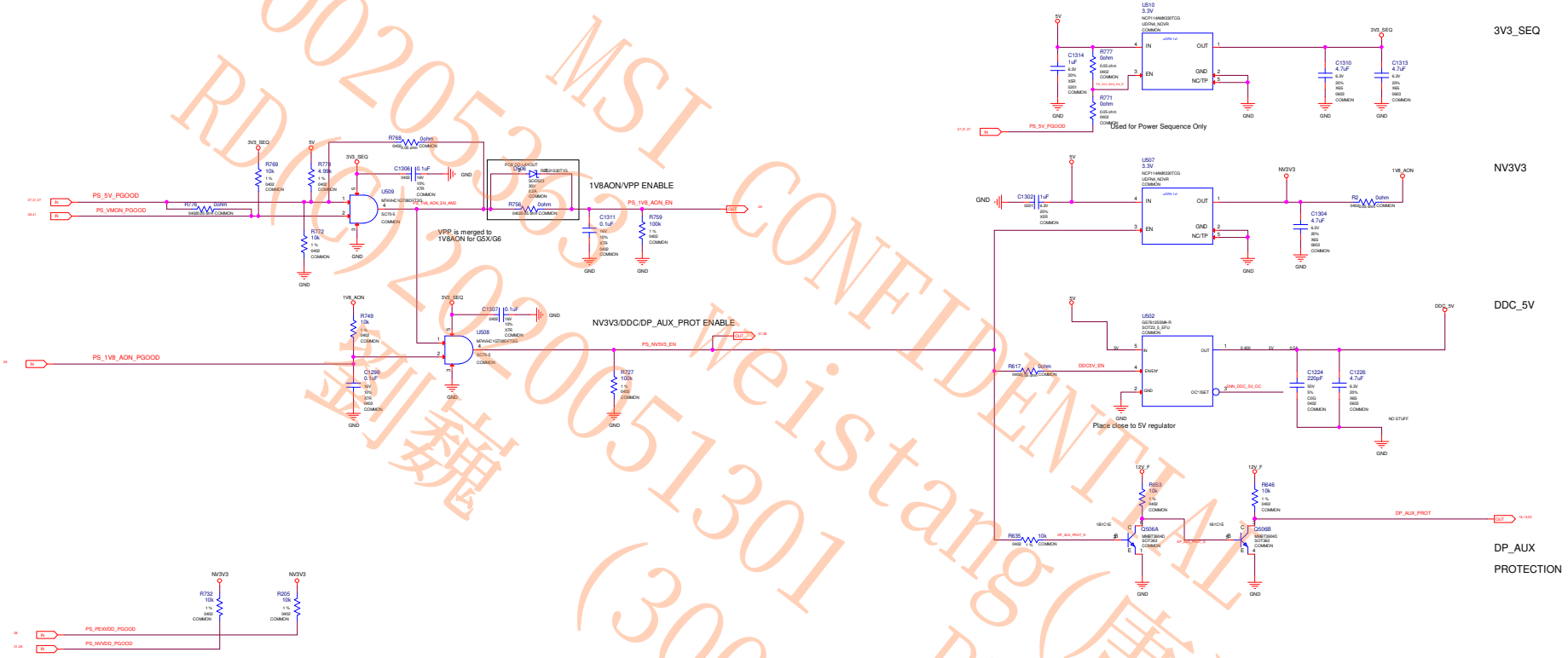
Page37: SEQ:1V8_AON, 3V3_SEQ, NV3V3, DDC_5V, DP_AUX_PROT



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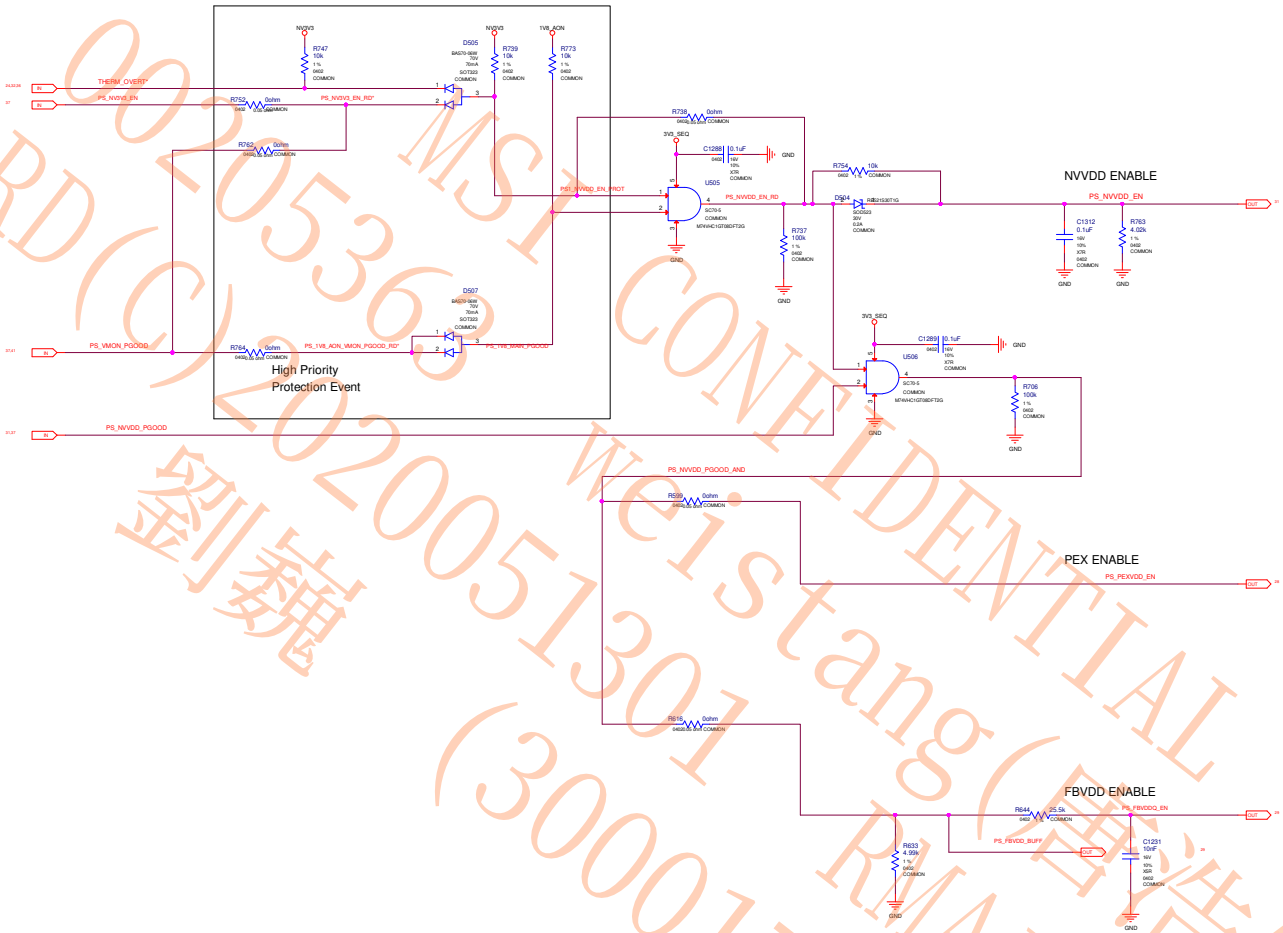
Page38: SEQ:NVVDD, PEX, FBVDDQ ENABLE



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NVVDD, PEX, FBVDDQ ENABLE

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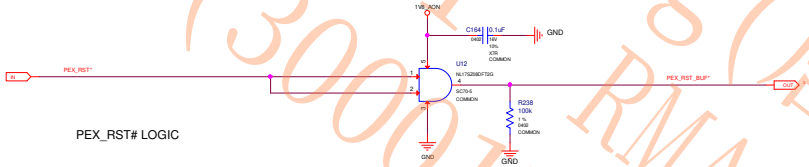
Page39: SEQ:MISC

PU ON GPU SIDE
NC ON GOLD FINGER SIDE

PU ON GPU SIDE
NC ON GOLD FINGER SIDE



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PAGE DETAIL	SEQ: MISC

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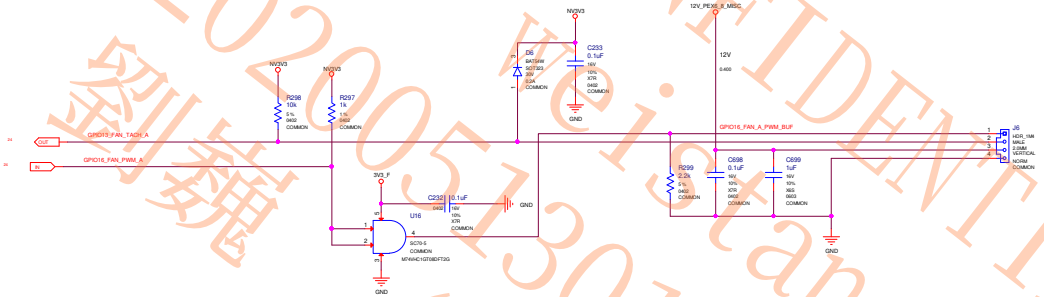
Page40: FAN



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	FAN

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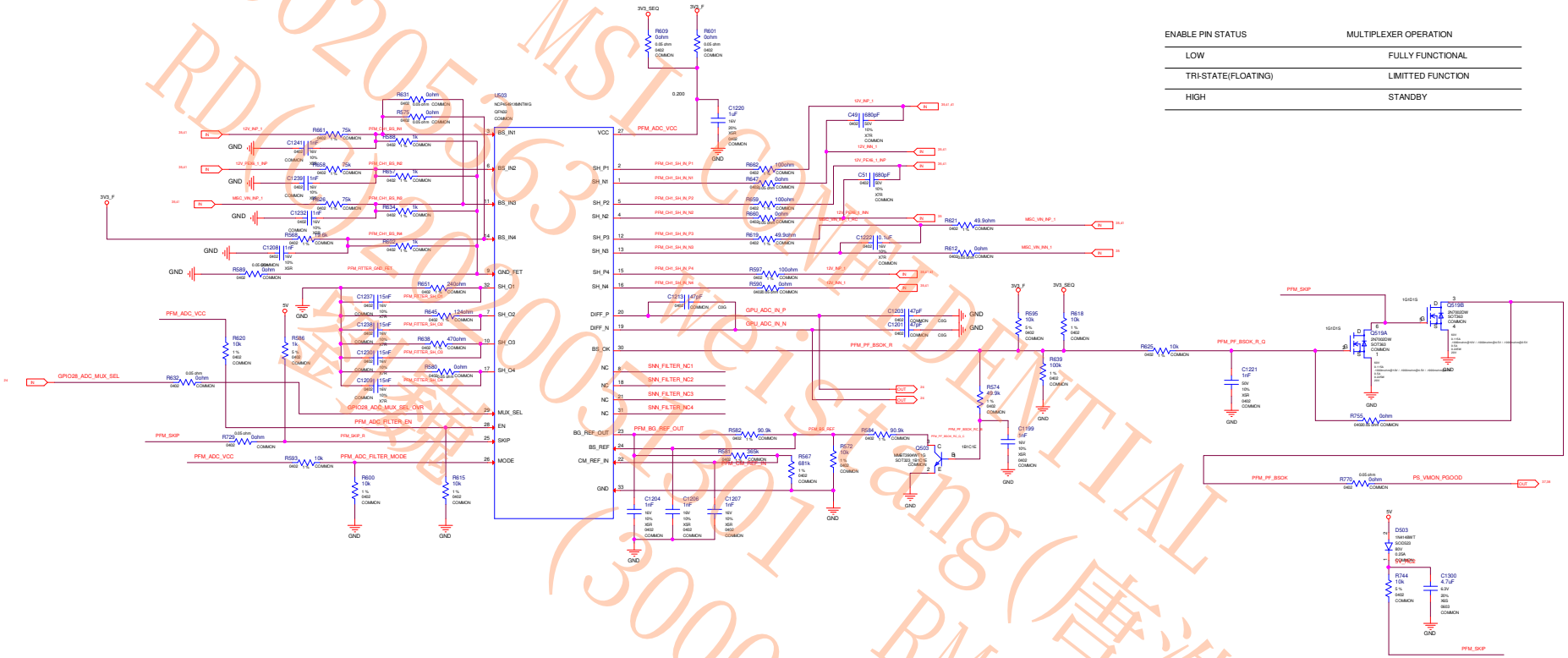
Page41: OVRM_PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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PAGE DETAIL	PS: OVRM_PWR SENSE

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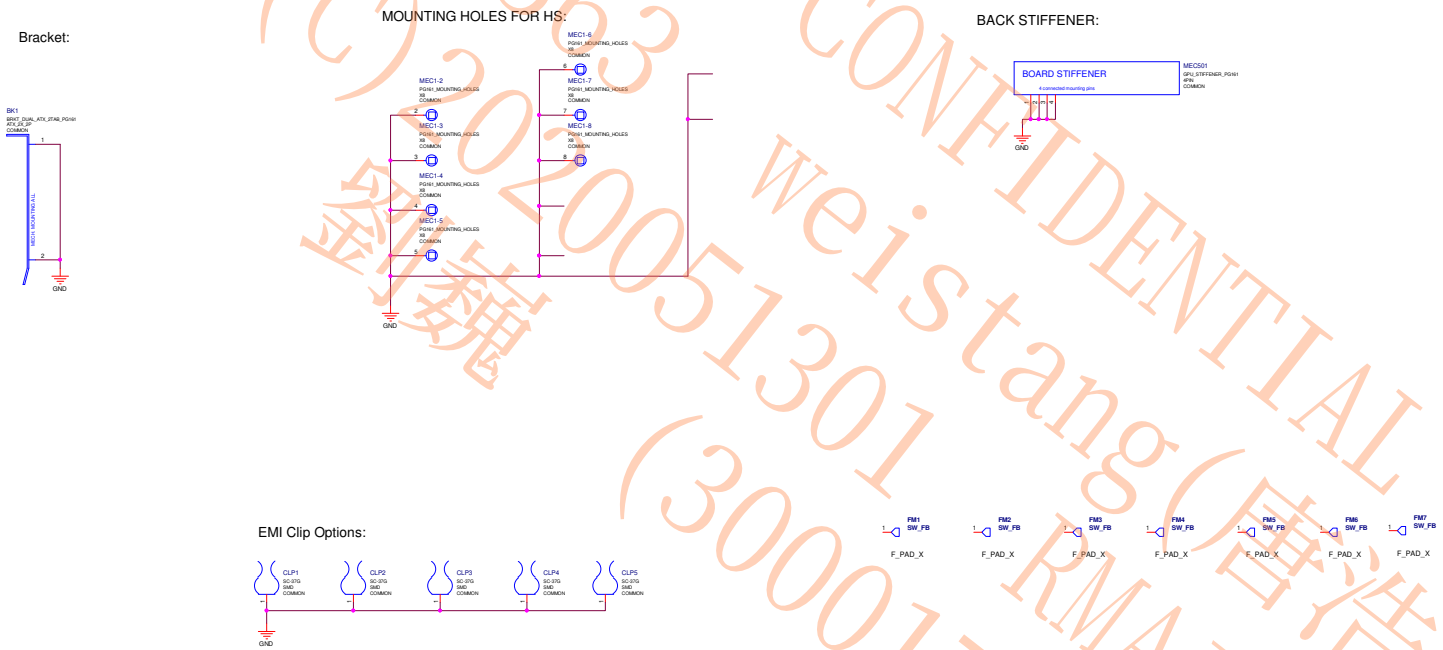
Page42: MECH



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