

V056: G72, DDR2 MEMORY 16Mx16


base on P381 A02  
add PMW circute for FBVDDQ.

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REV	VARIANT	NVPN	ASSEMBLY
0	BASE	60010381-xxxx-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU01	60010381-0000-100	P381: G72G34A, 32 BIT DDR2 MEMORY, VGA+SOTV
2	SKU01	60010381-0001-100	P381: G72G34A, 64 BIT DDR2 MEMORY, VGA+SOTV
3	SKU02	60010381-0002-100	P381: G72G34A, 32 BIT DDR2 MEMORY, DVH+SOTV
4	SKU03	60010381-0003-100	P381: G72G34A, 64 BIT DDR2 MEMORY, DVH+SOTV
5	SKU04	60010381-0004-100	P381: G72G34A, 64 BIT DDR2 MEMORY, VGA+DVH+SOTV
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P381 Overview



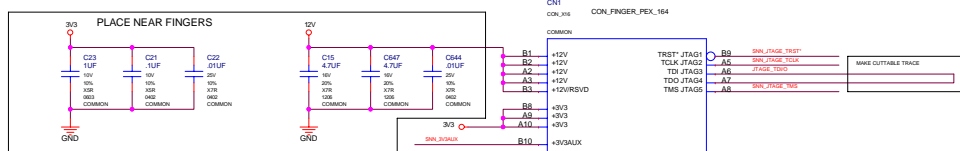
Micro-Star International Co., LTD.

V056-0A

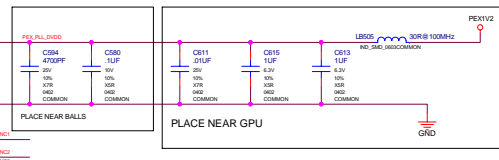
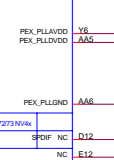
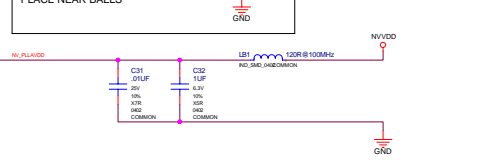
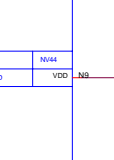
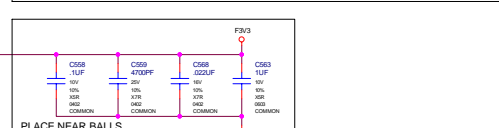
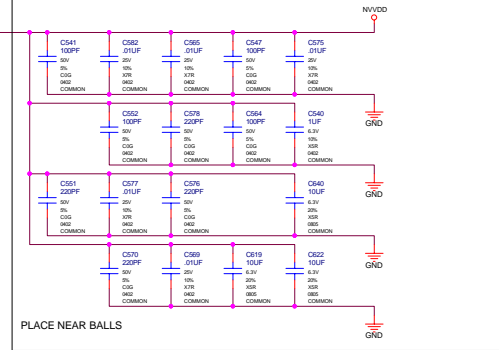
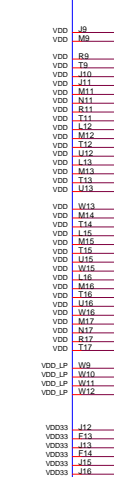
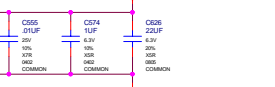
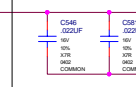
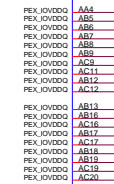
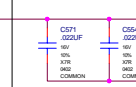
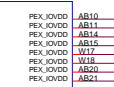
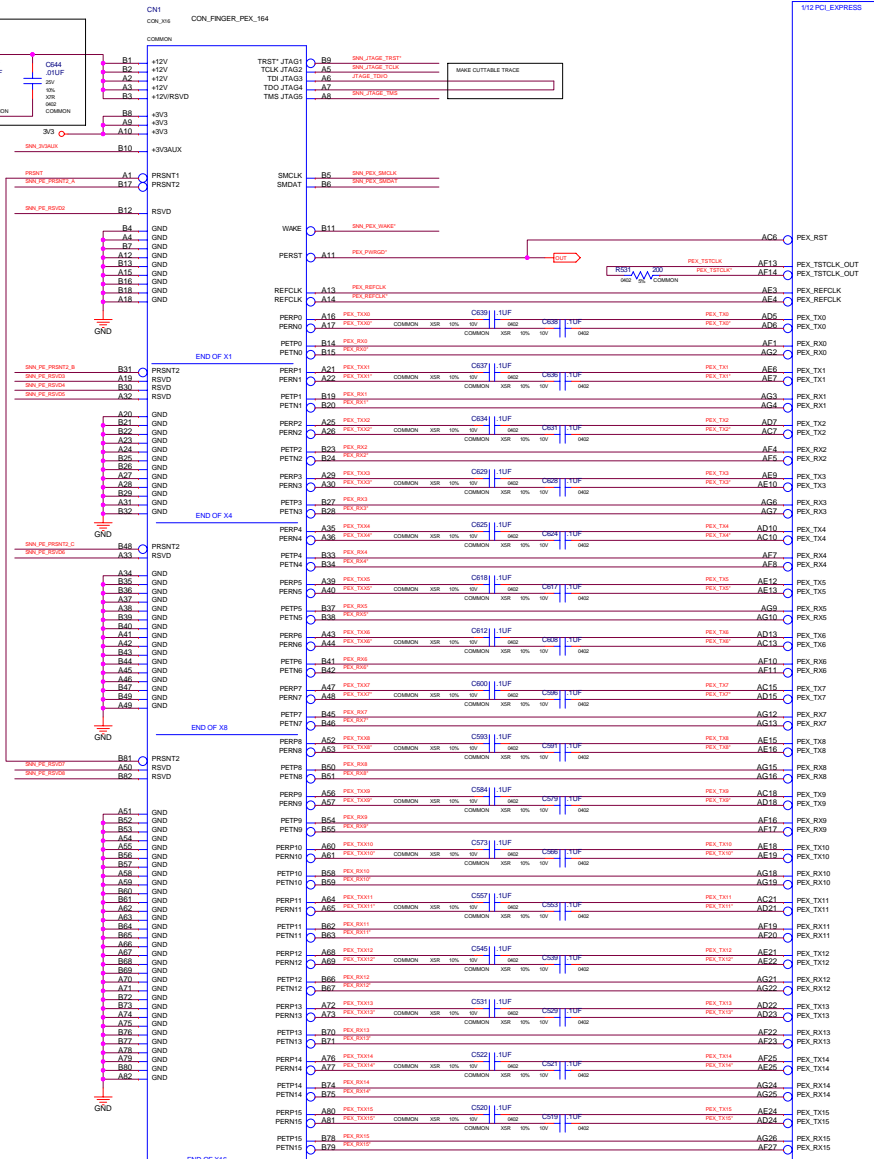
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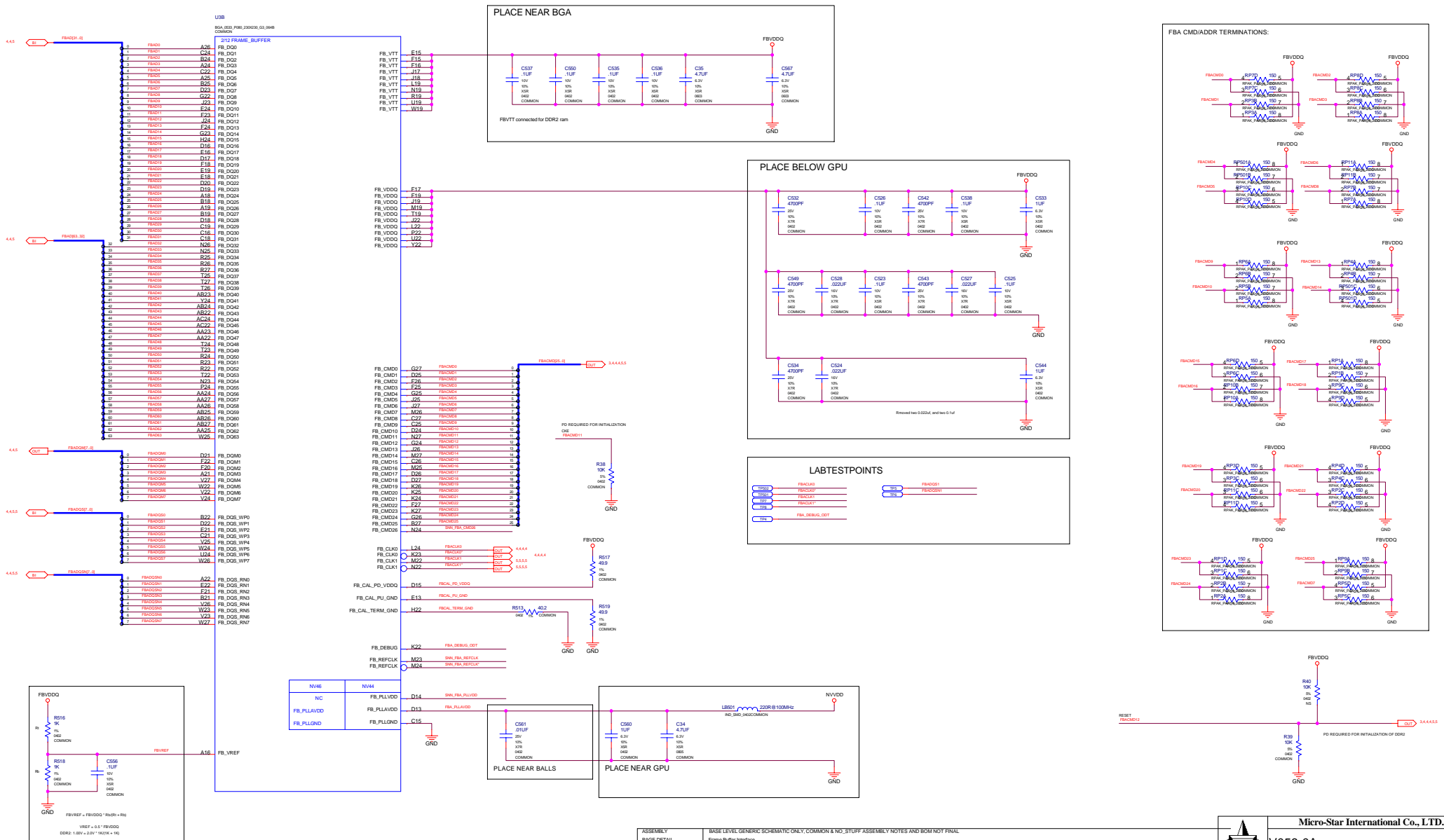
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IN	PEL_R99	PEL_R99	+	1000F
IN	PEL_R99P	PEL_R99P	+	1000F
IN	PEL_R			



## GPU: FB-Interface



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Frame Buffer Interface



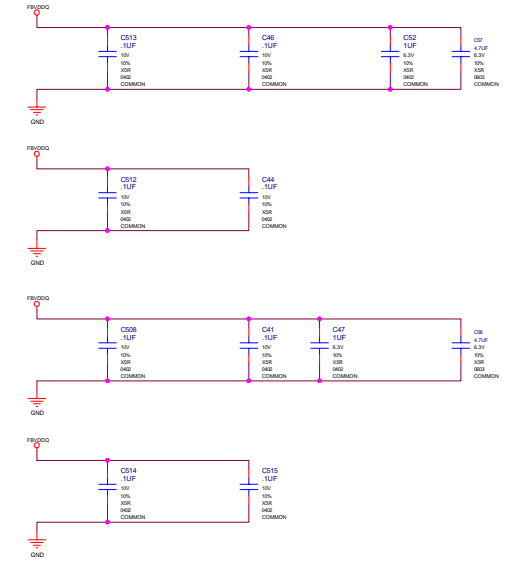
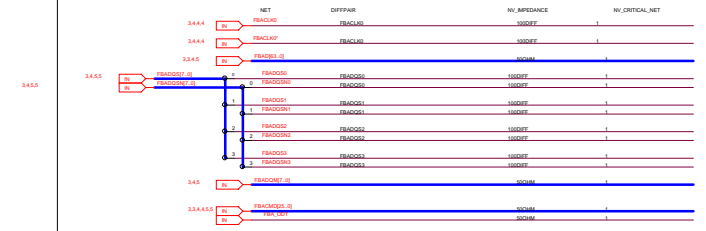
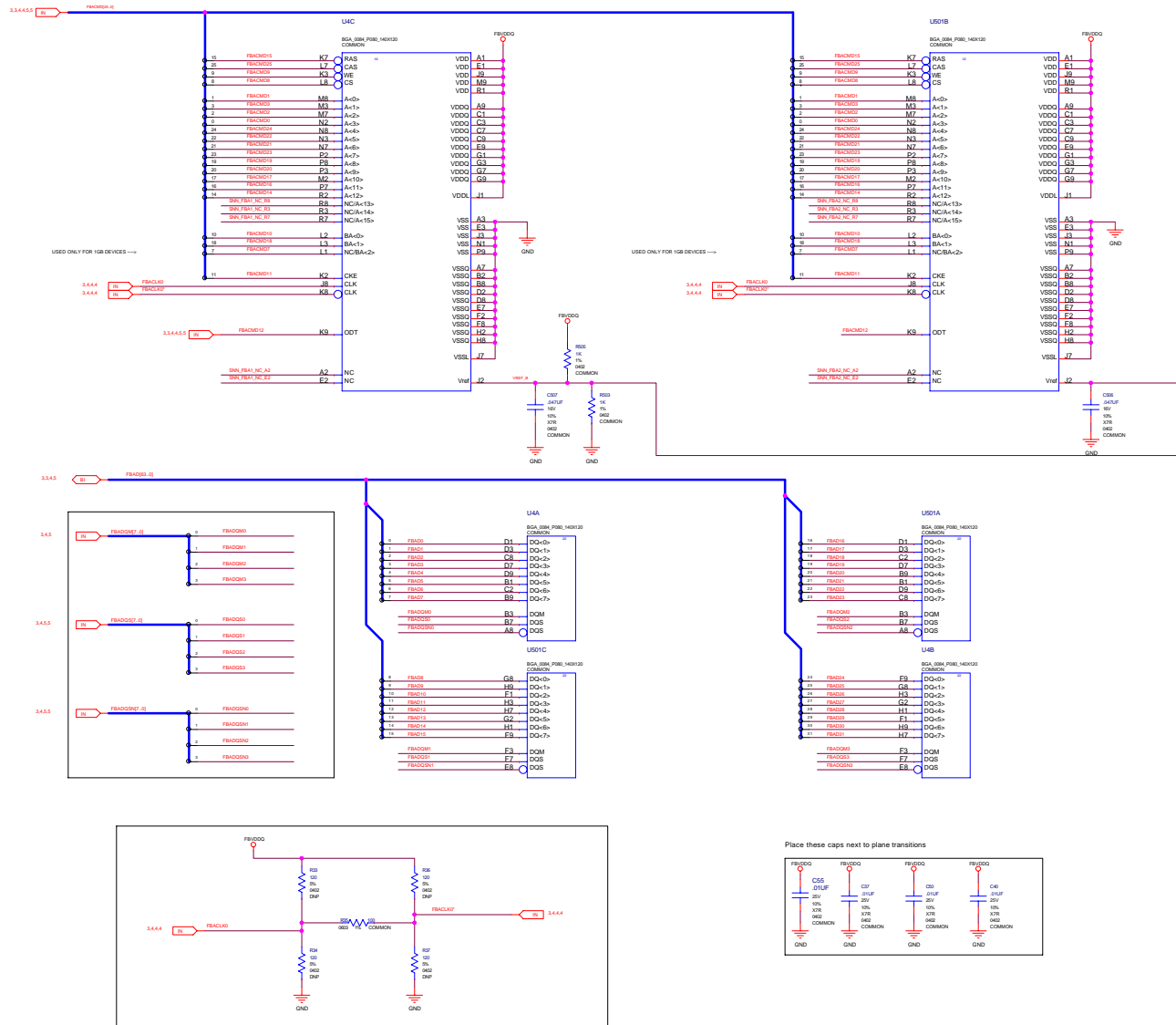
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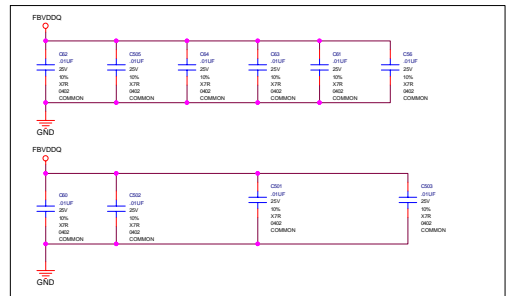
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# Memory Bit 0..31

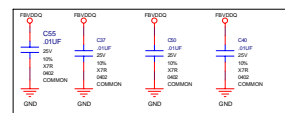
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



X-cap for CMD



Place these caps next to plane transitions

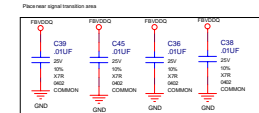
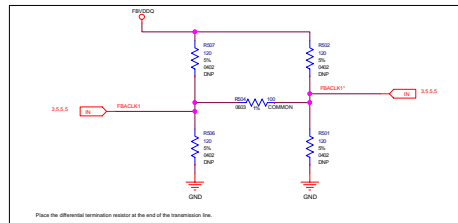
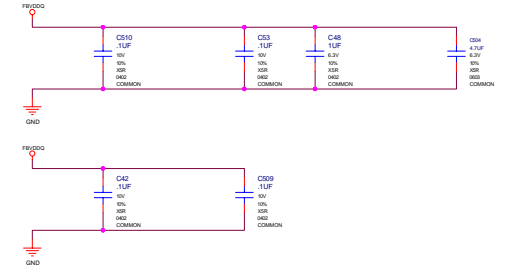
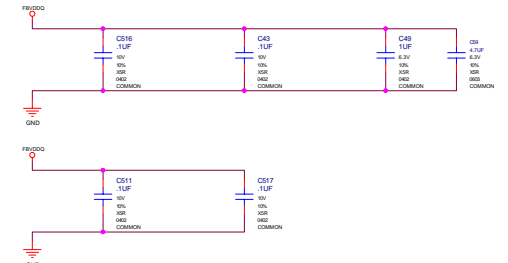
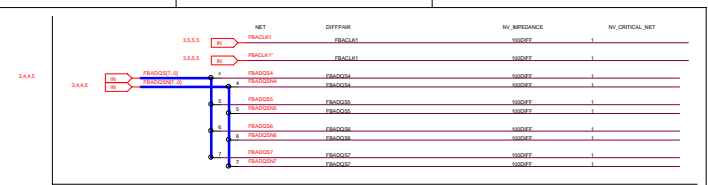
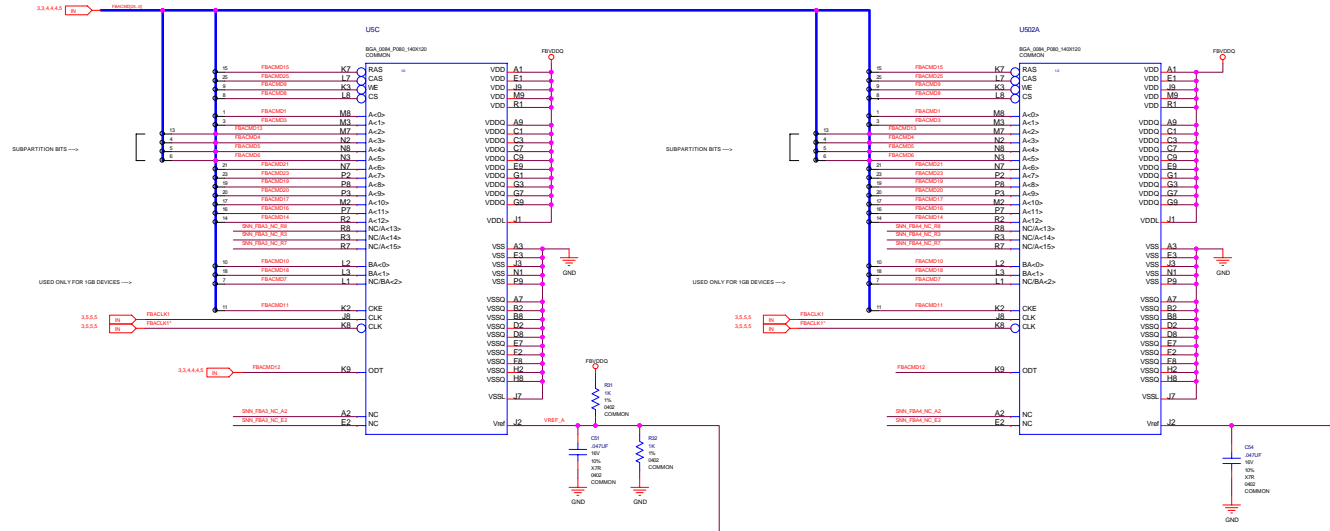


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ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO\_STUFF ASSEMBLY NOTES AND BOM NOT FINAL Memory bit bank 0..31

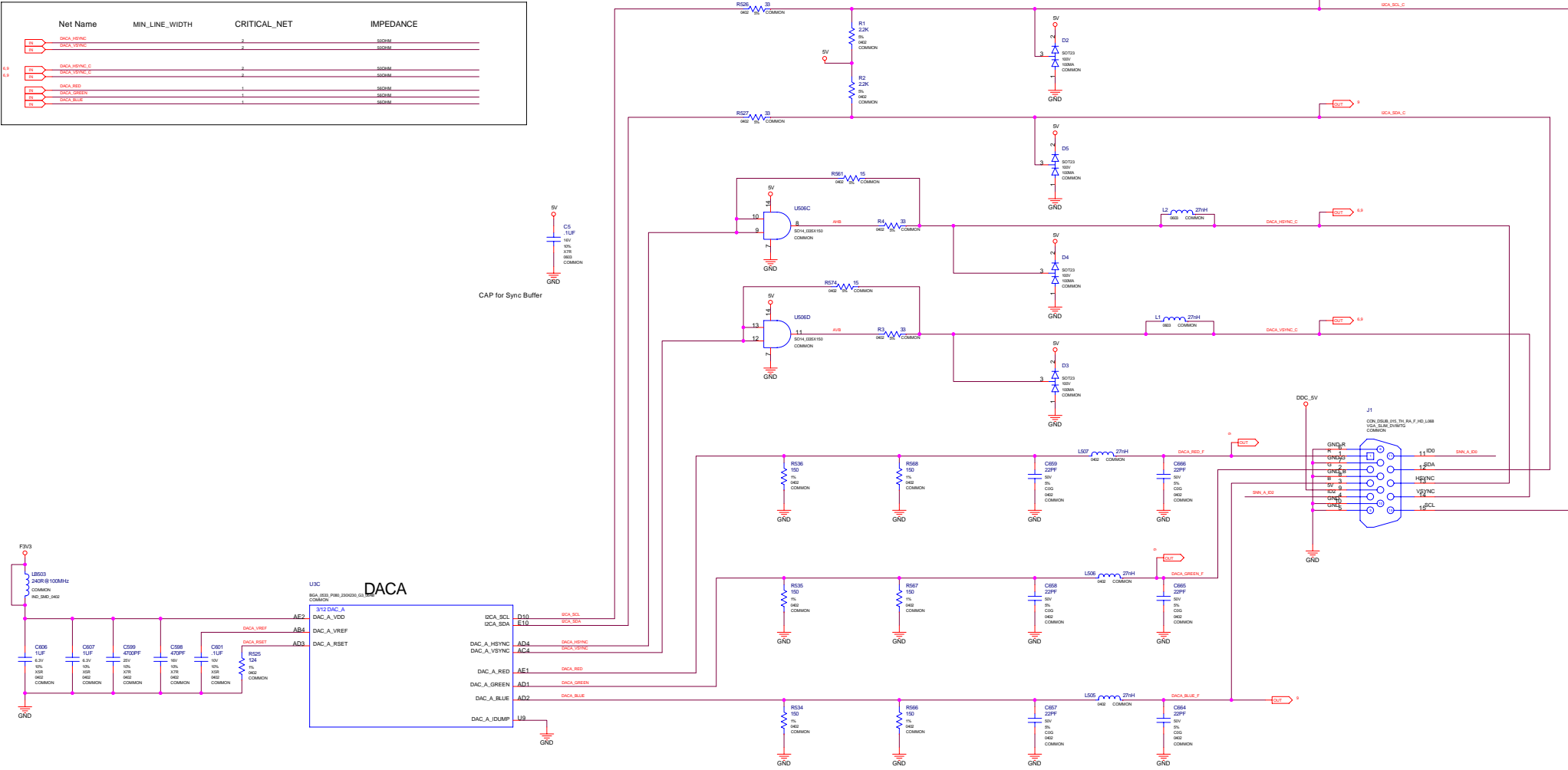
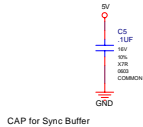
# Memory Bit 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

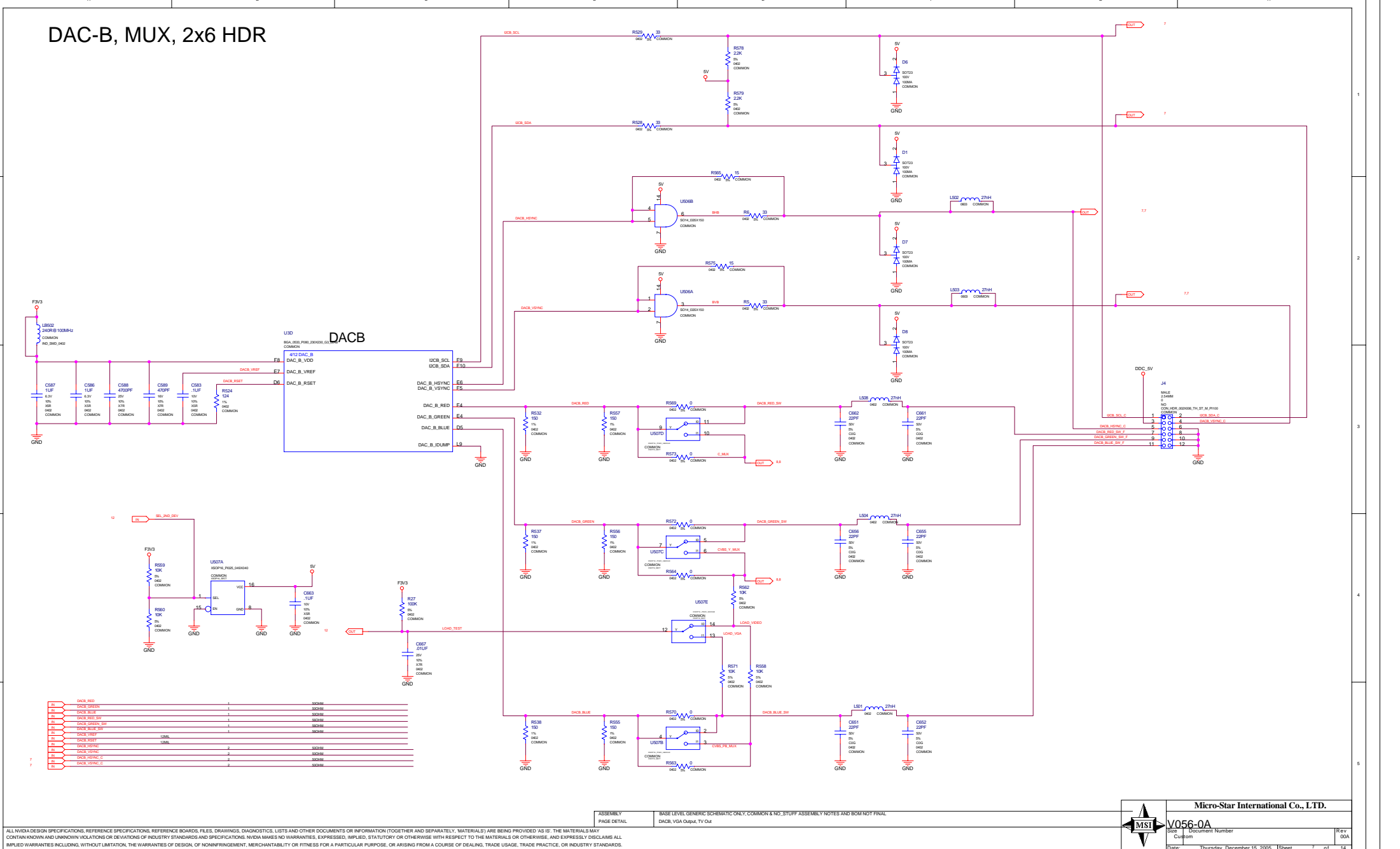


DAC-A, DB15 Connector

Net Name	MIN_LINE_WIDTH	CRITICAL_NET	IMPEDANCE
DACA_VREF	2		50OHM
DACA_VREF_C	2		50OHM
DACA_VREF_F	2		50OHM
DACA_RED	1		50OHM
DACA_GREEN	1		50OHM
DACA_BLUE	1		50OHM

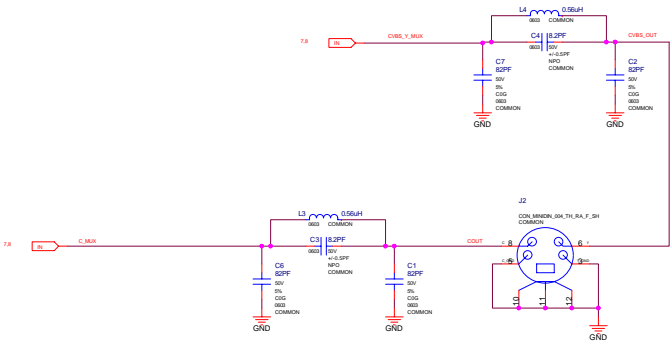


DAC-B, MUX, 2x6 HDR



VIDEO CONNECTORS: MiniDIN

	Name	LINE_WIDTH	CRITICAL	IMPEDANCE
7.8	C_MIX		A	50OHM
7.8	CINEL_Y_MIX		A	50OHM
7.8	COUT		A	50OHM
7.8	COUT_OUT		A	50OHM



Replace MiniDin with Compupack Part

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ASSEMBLY PAGE DETAIL  
BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL  
VIDEO CONNECTORS: MiniDIN, 2x6 HDR

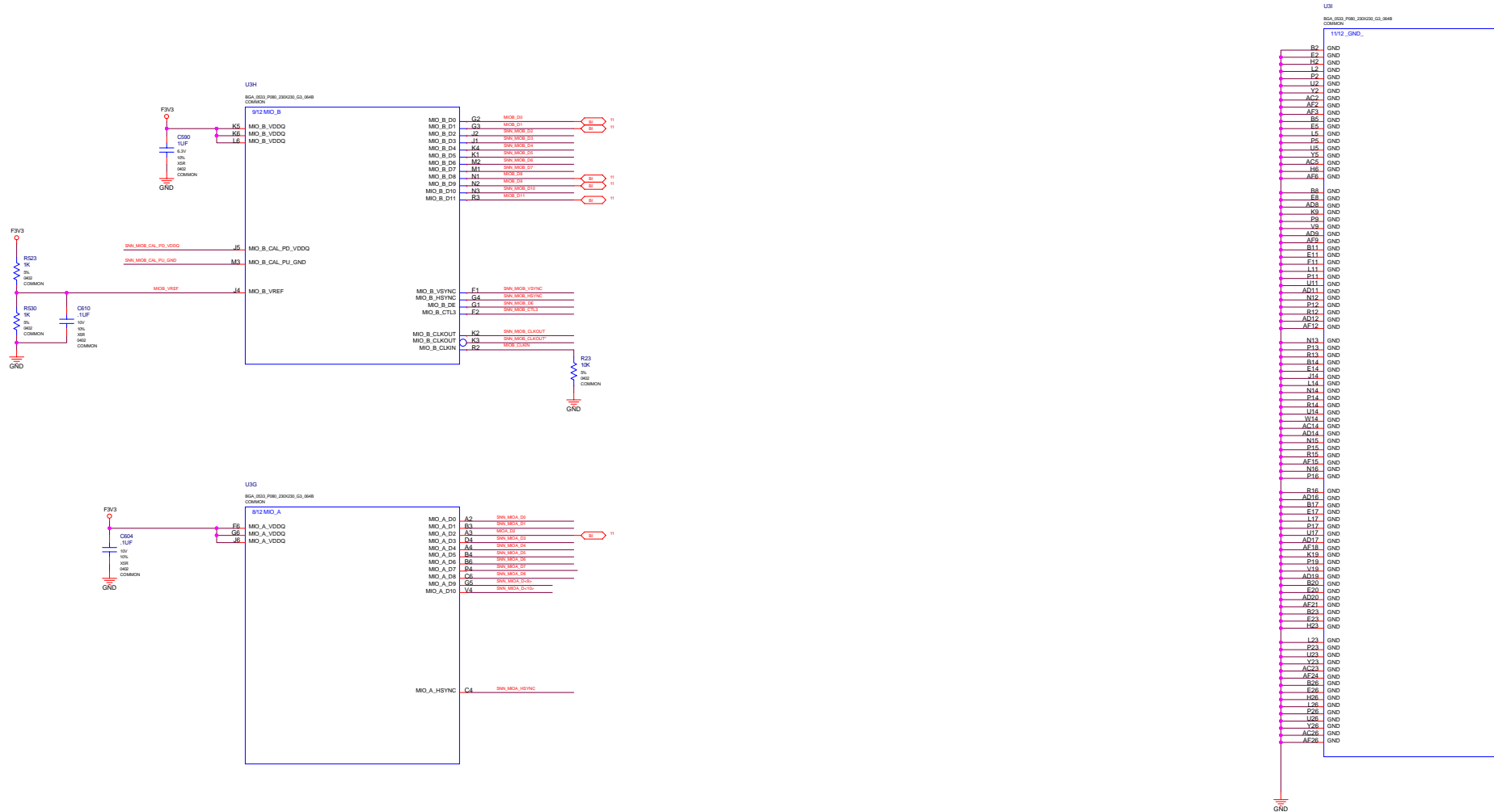


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MIOA, MIOB Interface



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ASSEMBLY PAGE DETAIL  
BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL  
MIOA, MIOB Interface, LPC-ROM



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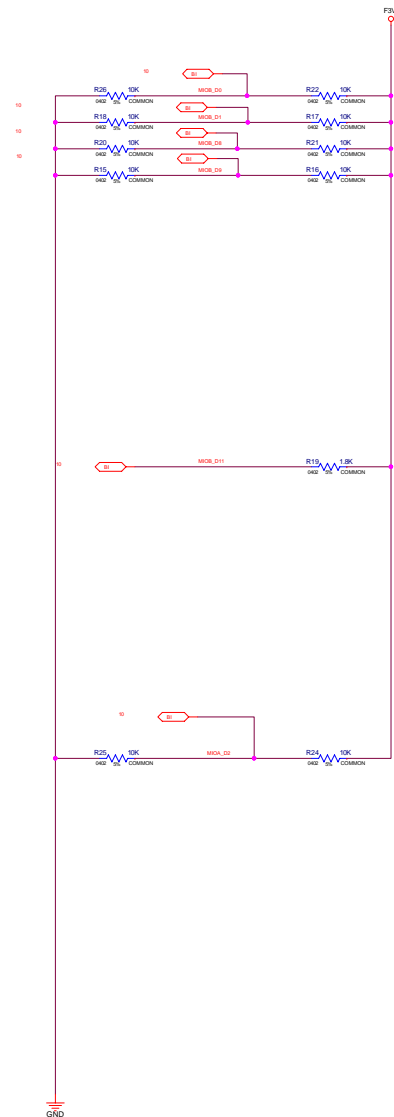
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Date: Thursday, December 16, 2005

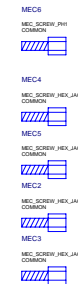
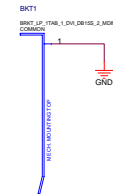
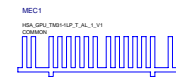
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## STRAPS, Mechanical Parts

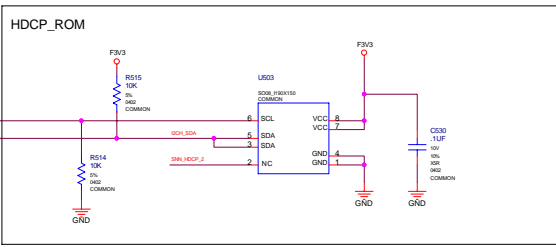
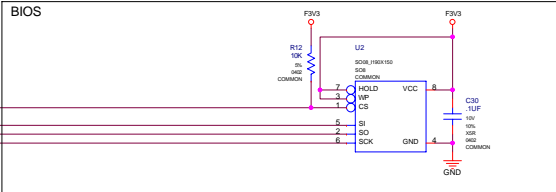
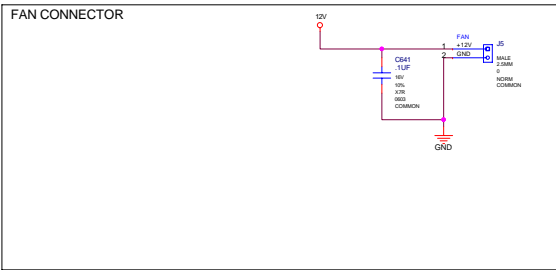
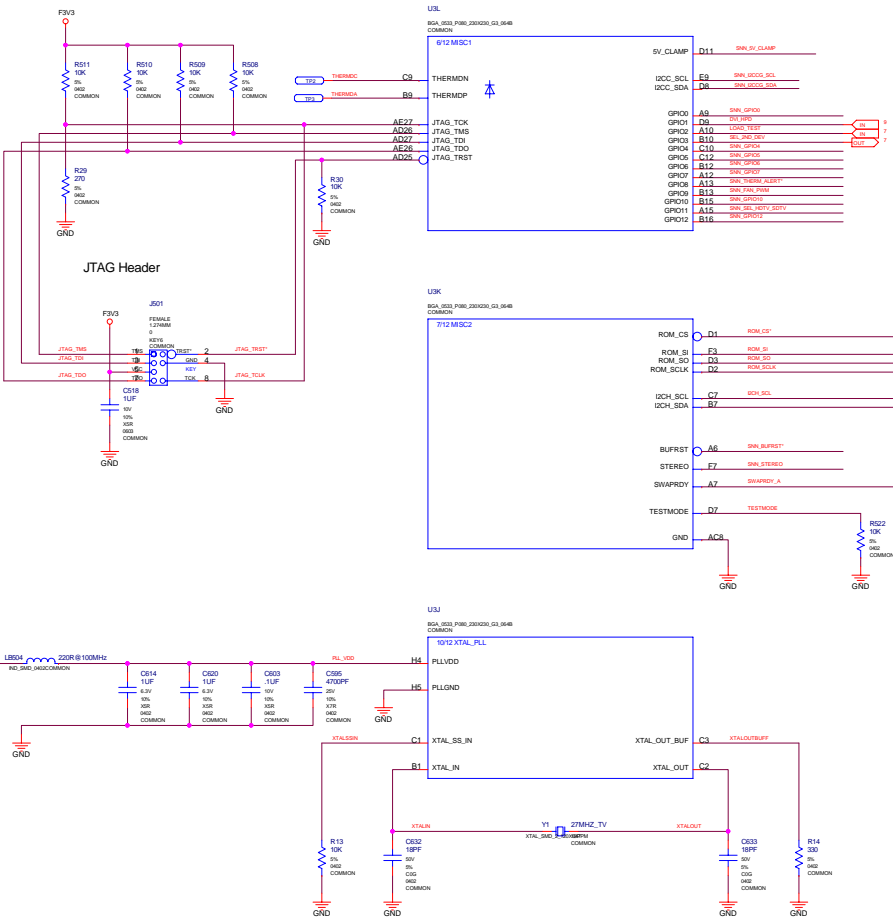


Bit Signal		Values
00	PCI_AD_VENDOR	0 REVERSED 1 LOCAL
01	SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS
02	RAM_CTL_0	000 8M(HDDR2.64M) 001 8M(U) 010 16M(HDDR2.64M) 011 8M(U) 100 8M(U) 101 8M(U) 110 8M(U) 111 16M(HDDR2.64M)
03	RAM_CTL_1	000 8M(U) 001 8M(U) 010 8M(U) 011 8M(U) 100 8M(U) 101 8M(U) 110 8M(U) 111 16M(HDDR2.64M)
04	RAM_CTL_2	000 8M(U) 001 8M(U) 010 8M(U) 011 8M(U) 100 8M(U) 101 8M(U) 110 8M(U) 111 16M(HDDR2.64M)
05	RAM_CTL_3	000 8M(U) 001 8M(U) 010 8M(U) 011 8M(U) 100 8M(U) 101 8M(U) 110 8M(U) 111 16M(HDDR2.64M)
06	CRISTA_0	00 15.000 MHz 01 14.318 MHz 10 7.159 MHz 11 UNKNOWN
07	CRISTA_1	00 15.000 MHz 01 14.318 MHz 10 7.159 MHz 11 UNKNOWN
08	TV_MODE_0	00 BTCCM 01 NTSC 10 PAL 11 DET
09	TV_MODE_1	00 BTCCM 01 NTSC 10 PAL 11 DET
10	ASP_3A	0 ASP0 DISABLED 1 ASP0 DISABLED
11	ASP_3BA	0 ASP1 DISABLED 1 ASP1 DISABLED
12	ASP_1AST008	0 P/F0 ENABLED 1 P/F0 DISABLED
13	PCI_DEV_0	100 (unused (N/A))
14	PCI_DEV_1	
20	PCI_DEV_2	
21	PCI_DEV_3	
16	BUS_TYPE	0 PCI 1 AGP
17	FP_FACE	0 0MHz 1 100MHz (DEFAULT)
22	FR_0	0 66MHz 01 100MHz 10 133MHz (DEFAULT) 11 50MHz
23	BR	00 BR0 DISABLED 1 BRIDGE ENABLED
24	BR_0BR	00 BR0 DISABLED 1 BRIDGE ENABLED
25	BR_1BR	00 BR1 DISABLED 1 BRIDGE ENABLED
26	BR_2BR	00 BR2 DISABLED 1 BRIDGE ENABLED
27	BR_3BR	00 BR3 DISABLED 1 BRIDGE ENABLED
28	BR_4BR	00 BR4 DISABLED 1 BRIDGE ENABLED
29	RCM_TYPE_0	00 0MHz 01 80MHz 10 100MHz 11 133MHz
30	RCM_TYPE_1	00 0MHz 01 80MHz 10 100MHz 11 133MHz
15	USER_0	000 (DEFAULT)
16	USER_1	
17	USER_2	
18	USER_3	
19	USER_4	
PCI_PLA_EN_TERR100		
XGR_PACING_LUT_ADDR[0]		
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XGR_PACING_LUT_ADDR[2]		
XGR_PACING_LUT_ADDR[3]		
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XGR_PACING_LUT_ADDR[112]		
XGR_PACING_LUT_ADDR[113]</		




XTAL, GPIO, BIOS, FAN, JTAG, THERMAL

Net Name	LINE_WIDTH	Voltage
PLL_VDD	1.2MM	3.3V
XTALIN	1	3.3V
XTALOUT	1	3.3V
Net Name	LINE_WIDTH	Voltage
CRITICAL_NET	1	3.3V
IMPEDANCE	1	3.3V



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PowerSupplyII: 5V, DDC5V, F3V3, FBVDDQ

