NV25, P83, DUAL DAC/TMDS, 128MB 4MX32 BGA DDR, TV IN/OUT, GOGGLES, AGP

A00-X02: Combined CX and SA power filters. Connected memory PS bootstrap to 12V. XOR Hotplugs to GPIO1. Isolated PLL VDD from 3.3VL to get rid of 350mV stray voltage. Combined GND, AGND and Chassis GND A00-X03 Changed both TMDS digital powers from 3.3V to 3.3VL. Added a resistor to base transistor PLL_VDD sequencer. Added 2nd fan connector. Added various placement and routing notes. P83-A00: TERMINATED DESIGN Changed memory series resistors to (56R to VTT) terminated design. Swapping.... Sync up with P81 changes Modified PS to support terminated design. Design Review: Deleted PU resistor from SII_DVOCLK_IN_PRI Added PDs resistors on SII_DVOCLK_IN_PRI and SII_DVOCLK_IN_SEC More cleanup on Assembly properties. Moved TMDS parallel termination resistors to DVI connector page. Added C1567 (0.1uF) near Stereo connector pin 1. Removed bootstrap from SC1102. Moved R1197.2 to AGND. P83-A00: X RELEASE P83-A01: Add two 5-3.0 VR for DVOA and B BUS power supply and change Flash Rom power to DVOA_PWR (3.0V) on Page 5.1 Change the decoupling cap. C1349,C1350,C1351,C1362,C907 connect to DVOA_PWR from 3.3V on page 5.1 Change the decoupling cap. C1443,C1444,C1445,C1446,C920, connect to DVOA_PWR from 3.3V on page 5.1 Change series P-ROM U505 power to DVOA_PWR (3.0V) on page 5.2V Change GPU pin AH1, AD1, AC7 connect to DVOA_PWR and change GPU pin AH15, AP8, AP12 connect to DVOB_PWR on Page 6.0. Connect AGND to GND symbol on page 3.1 Remove R1183,R1184,R1179,R1180,R1198,R1199, P83-A01 X RELEASE A01-000 Fix the cap property errors to match the BOM. P83-A02: A02-X00 Put NO_STUUF for C1123, C1126, C1129, C304, C307, C310 Replace C303, C306, C309, C1122, C1125, C1128 with CAP NPO 0603 15PF 16V 5% (035-20150-0006-000) Replace L715, L717, L719, L300, L305, L309 with IND 0805 MTLR 5% 0.068UH (130-30680-0006-000) Replace L716, L718, L720, L302, L306, L310 with IND 0603 MTLR 5% 0.068UH (130-20680-0006-000) Change C29, C30 value from 33PF to 27PF to improve the color burst stability for conexent and philips TV chip

Change R1072 res value from 665 Ohm to 1.5K to allow use other MOSFET with 11mOhm Rdson, like IRF7811.

P83 P-RELEASE

P80-A00: Based on P53-A00.

Populate R1034 with 0.01 Ohm Populate 68R parallel terminations on FBCLK/CLK#

A00-X01: Isolated GND, AGND and Chassis GND Corrected Multichip Strap Changed sync buffers inputs from pin 2 to pin 1 for easy probing. Corrected PWRGD_FBVDD on memory PS

COMMON -- ALL

NO_STUFF - NOT_STUFFED

PRI_VGA - Primary VGA Support

PRI_DVI - Primary DVI-D (Digital) Support

PRI_DVI I - Primary DVI-I (Digital & Analog) Support

SEC_DVI I - Secondary DVI-I (Digital & Analog) Support

PRI_PROT - Primary DVI-VGA protection diodes.

SEC_PROT - Secondary DVI-I protection diodes

MEMI28 - 128MB EXTENDED MEMORY

NO_STUFF FOR FIRST BUILD ROM_SER - Serial ROM used ROM_PAR - Parallel ROM used.

STEREO - USED FOR STEREO GOOGLES
STEREOSYNC1 - USED FOR STEREO GOOGLES
STEREOSYNC2 - USED FOR STEREO GOOGLES
STEREOSYNC3 - USED FOR STEREO SINC BUFFERS
SAA8 - PHILIPS ENCODER DECODER SAA7108
CX - CONEXENT ENCODER CX25571

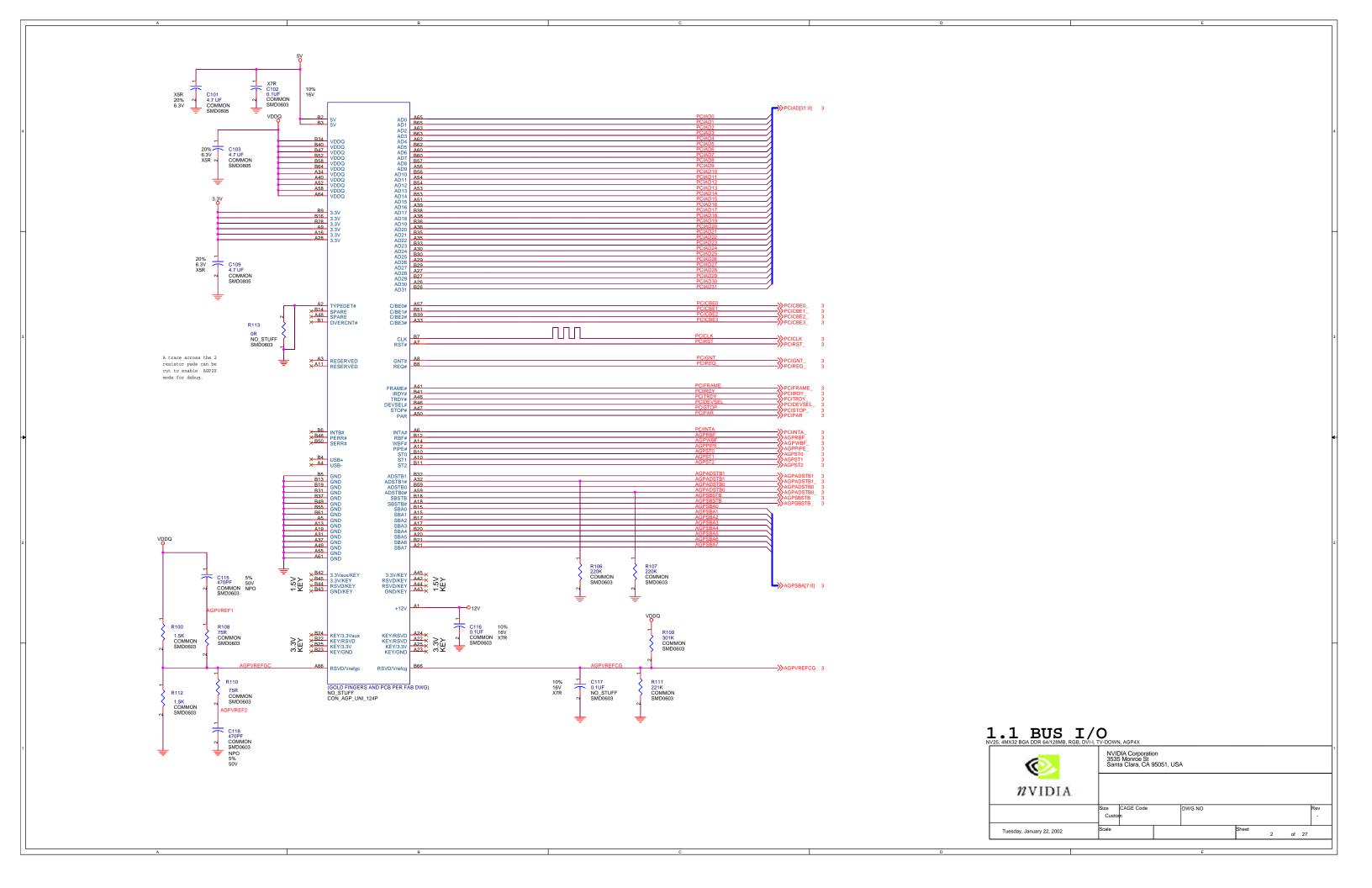
NO_STUFF FOR FIRST BUILD

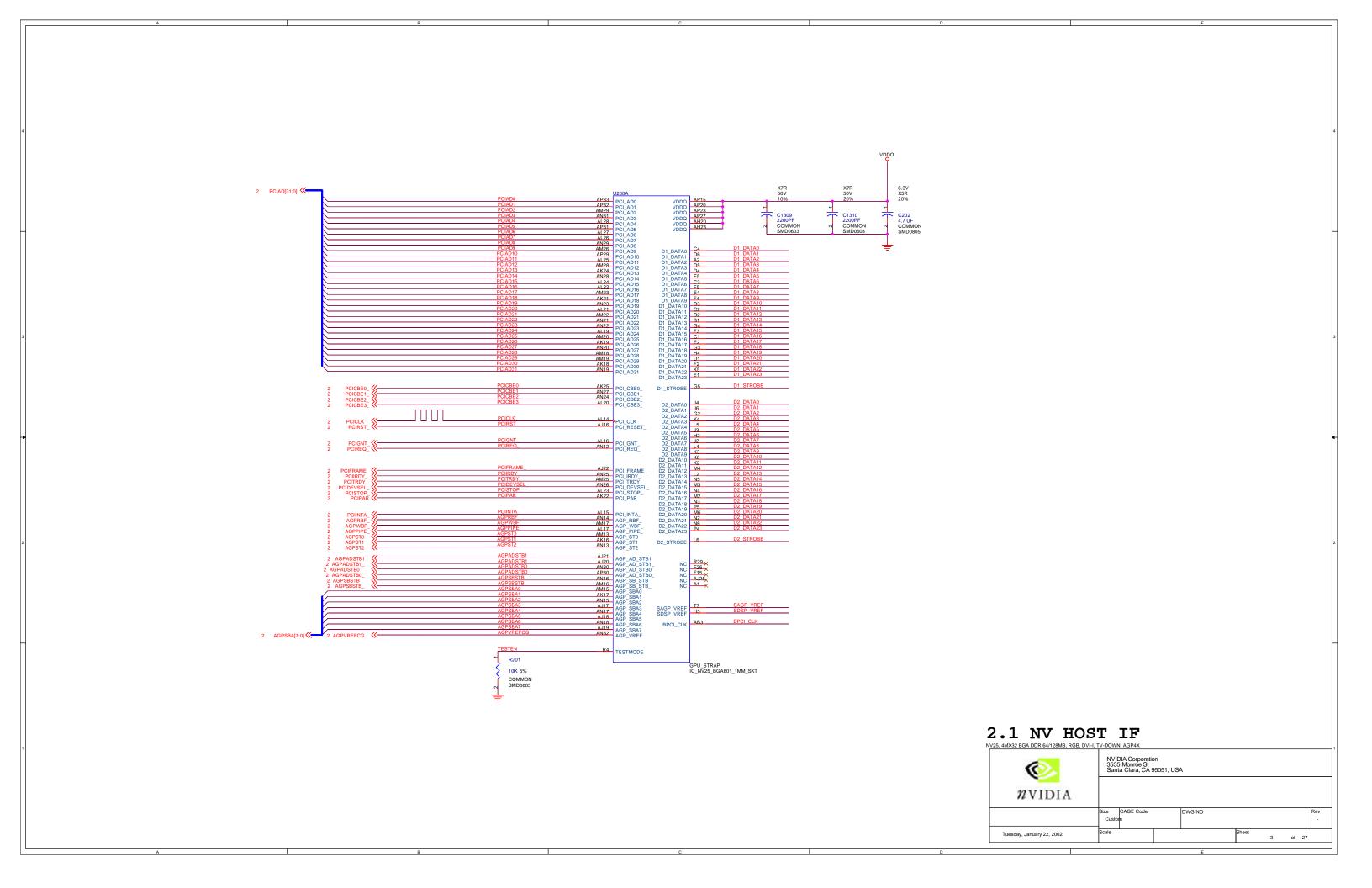
SC1102 - USED TO REGULATE FBVDD FROM 12V - SWITCHER SC1565 - USED TO REGULATE 3.3VI FROM 3.3V - LINEAR SC1175 - USED TO REGULATE NVVDD FROM 3.3V AND 5V - SWITCHER

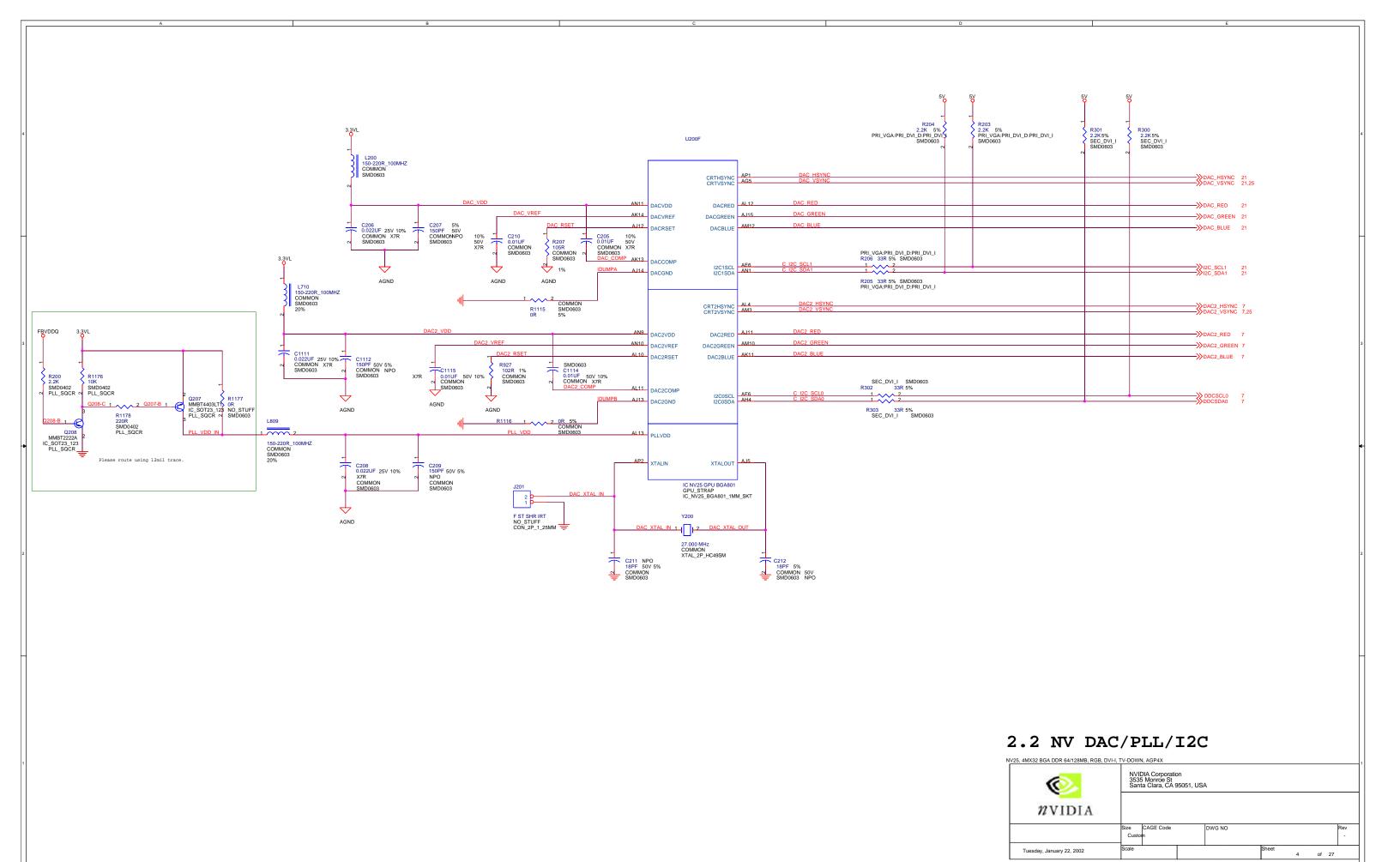
VGA-TV-DVI - Used for Primary VGA / TV / Secondary DVI VGA-DVI - Used for Primary VGA / Secodary DVI only VGA-TV - Used for Primary VGA / TV VGA - Used for Primary VGA only DVI-TV-DVI - Used for Primary DVI / TV / Secondary DVI DVI-DVI - Used for Primary DVI / Secondary DVI DVI-TV - Used for Primary DVI / TV DVI - Used for Primary DVI / TV DVI - Used for Secondary DVI DVI - Used for Secondary DVI DVI - Used for Passive heat sink FAN_HS - Used for Fan heat Sink SOCKET - PARTS REMOVED WHEN USING A SOCKET

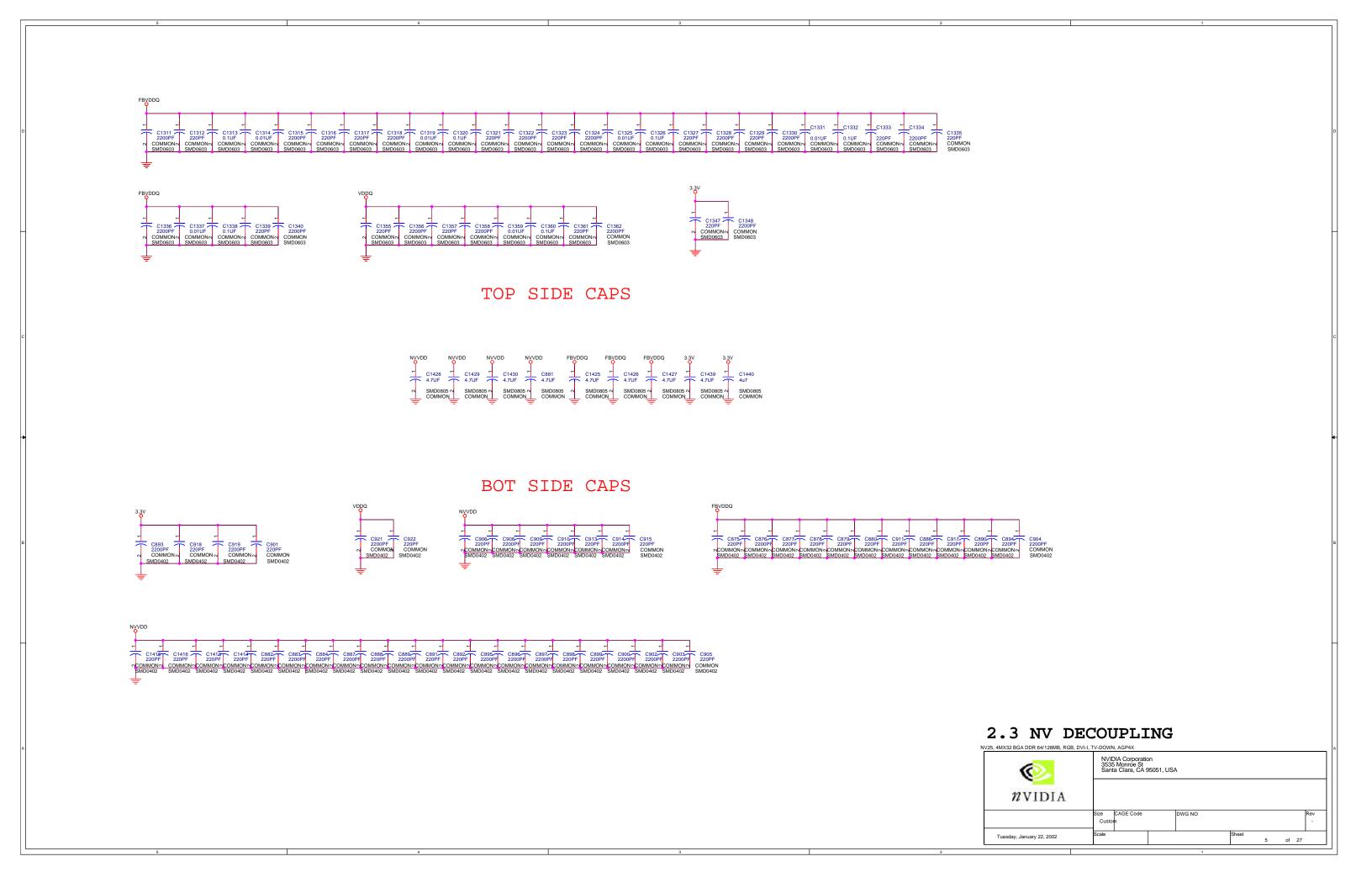
O. TOP PAGE NV25_4MX32_RGA_DDR_64/128MB_RGB_DVI-I_TV-DOW











17,20 DVOBD[23:0] >> 6,17,24 VIP_VID[15:0] >> BOOT_0_STRAP 17,18 DVOD21

17.18.23.24 DVOD8

17,18,23,24 DVOD9

15,17,24 VIP_VID7

15,17 VIP_VID8

10

14

0 = REVERSED 1 = NORMAL R929 1 2 10k 5% COMMON SMD0402

R931 1 2 10k 5% COMMON SMD0402 0 = System BIOS 1 = Adapter BIOS RAM_CFG_0 [3..0] - RAM_CFG - Frame buffer RAM R932 1 2 10k 5% MFM STRAP SMD0402 R933 1 2 10k 5% NO STUFF SMD0402 17,18 DVOD22 R934 1 2 10k 5% MEM_STRAP SMD0402 R935 1 2 10k 5% NO STUFF SMD0402 17,18 DVOD23 *//*---

 $_{\mathtt{RAM_CFG_1}}$ type configuration 1100 = SS Terminated 4MX32 BGA RAM_CFG_2 DQS PER BYTE.

R940 1 2 10k 5% COMMON SMD0402 R941 1 2 10k 5% NO STUFF SMD0402 R942 1 2 10k 5% NO STUFF SMD0402 R943 1 2 10k 5% COMMON SMD0402 15,17 VIP_HAD0 **~**—

R936 1 2 10k 5% NO_STUFF SMD0402

R938 1 2 10k 5% NO_STUFF SMD0402

[1..0] - TVMODE

0 = Enabled
1 = Disabled

R944 1 2 10k 5% NO_STUFF SMD0402 R945 1 2 10k 5% COMMON SMD0402 17.18.23.24 DVOD11 R946 1 2 10k 5% COMMON SMD0402 R947 1 2 10k 5% NO_STUFF SMD0402 15,17,24 VIP_VID6

R950 1 2 10k 5% COMMON SMD0402

R948 1 2 10k 5% VIP VID7 R949 1 2 10k 5% SMD0402 NO_STUFF SMD0402

R937 1 2 10k 5% MEM STRAP SMD0402

R939 1 2 10k 5% MEM_STRAP SMD0402

R951 1 2 10k 5% NO_STUFF SMD0402 0 = Enabled
1 = Disabled

R952 1 2 10k 5% VIP VID9 R953 1 2 10k 5% COMMON SMD0402 NO STUFF SMD0402 0 = Enabled
1 = Disabled

VIP VID12 R955 1 2 10k 5% AGP COMMON SMD0402

BOOT_0_STRAP PCI_DEVID_0 [3..0] - PCI_DEVID - PCI DEVICE ID CODE 12 R956 1 2 10k 5% GPU_STRAP SMD0402 R957 1 2 10k 5% NO_STUFF SMD0402 13 R959 1 2 10k 5% NO_STUFF SMD0402 R958 1 2 10k 5% GPU STRAP 2 10k 5% 15,17 VIP_VID11 R961 1 2 10k 5%

NO_STUFF SMD0402

R963 1 2 10k 5%

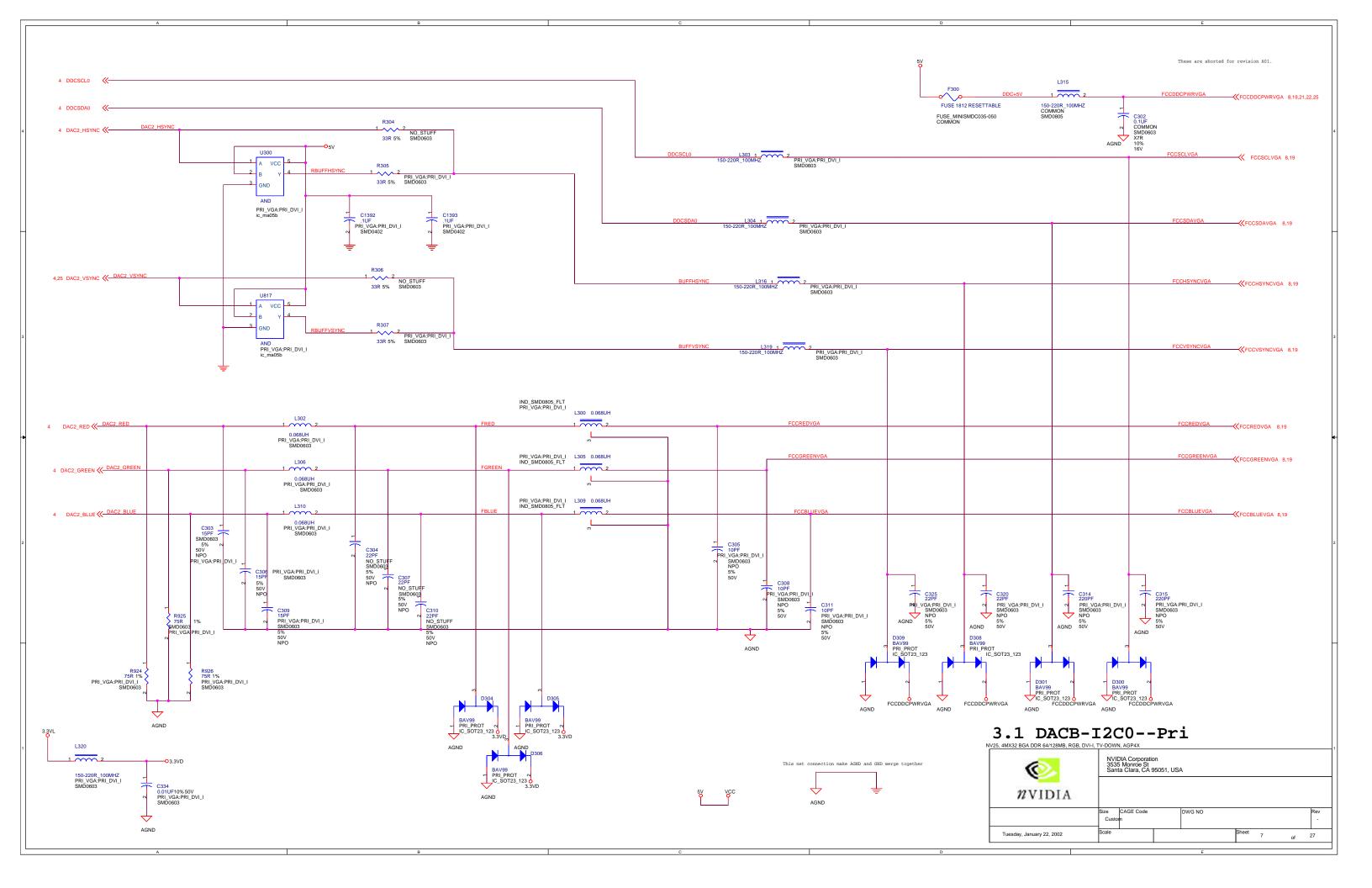
NO_STUFF SMD0402

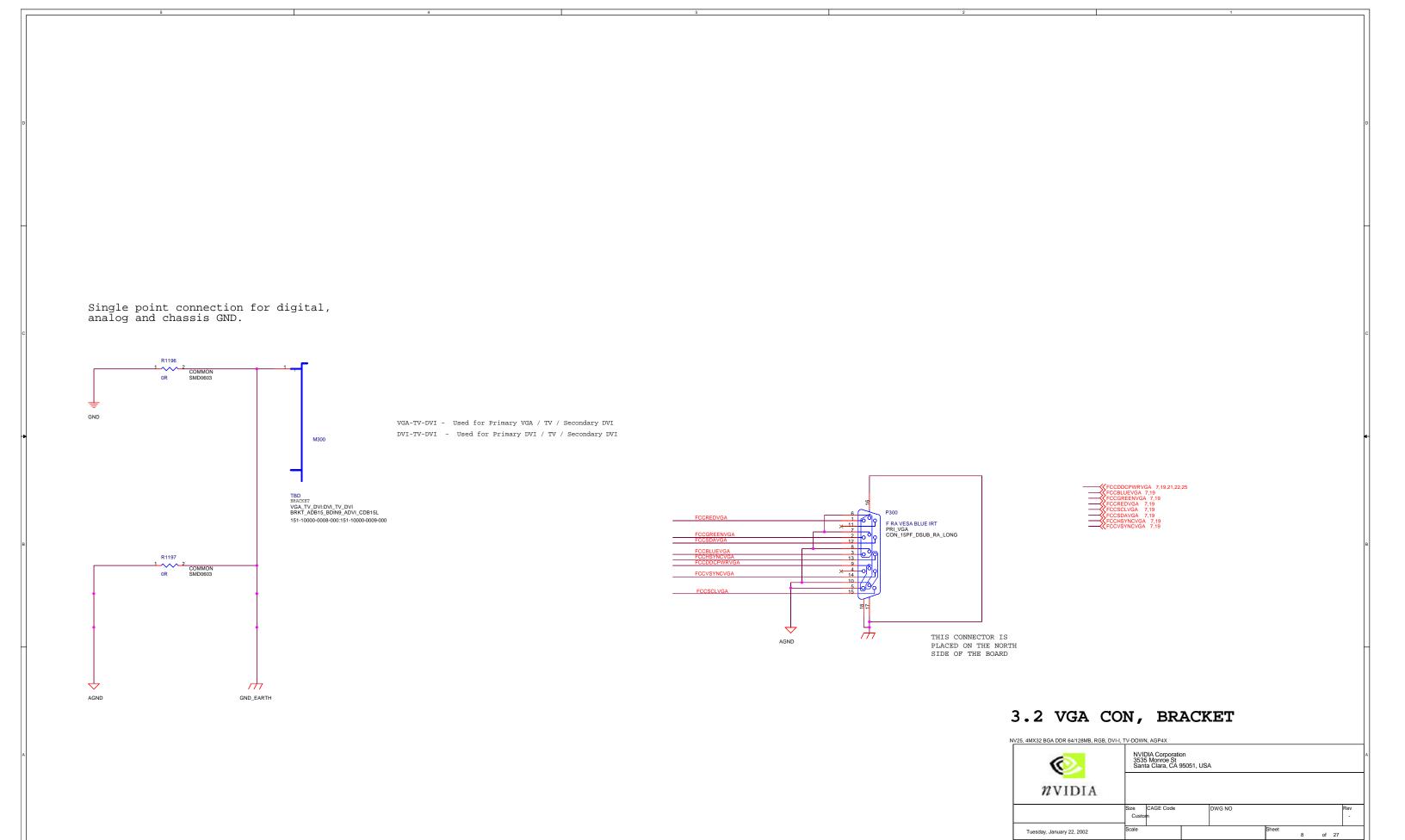
SMD0402 20 R960 1 2 10k 5% GPU STRAP SMD0402 PCI_DEVID_2 17,18 DVOD19 PCI_DEVID_3 R962 1 2 10k 5% GPU_STRAP SMD0402 17.18 DVOD20 R964 1 2 10k 5% COMMON SMD0402 R965 1 2 10k 5% NO STUFF SMD0402 R966 1 2 10k 5% VIP VID15
COMMON SMD0402 17 R967 1 2 10k 5% NO STUFF SMD0402 15,17 VIP_VID15 **~**— [1..0] - STRAP_FB - Frame Buffer type selection R972 1 2 10k 5% NO_STUFF SMD0402 R973 1 2 10k 5% COMMON SMD0402 17 VIP_HAD1 STRAP_FB_1 24 R974 1 2 10k 5% COMMON SMD0402 R975 1 2 10k 5% NO_STUFF SMD0402 17 VIP HADS 15 R976 1 2 10k 5% VIP_VID13

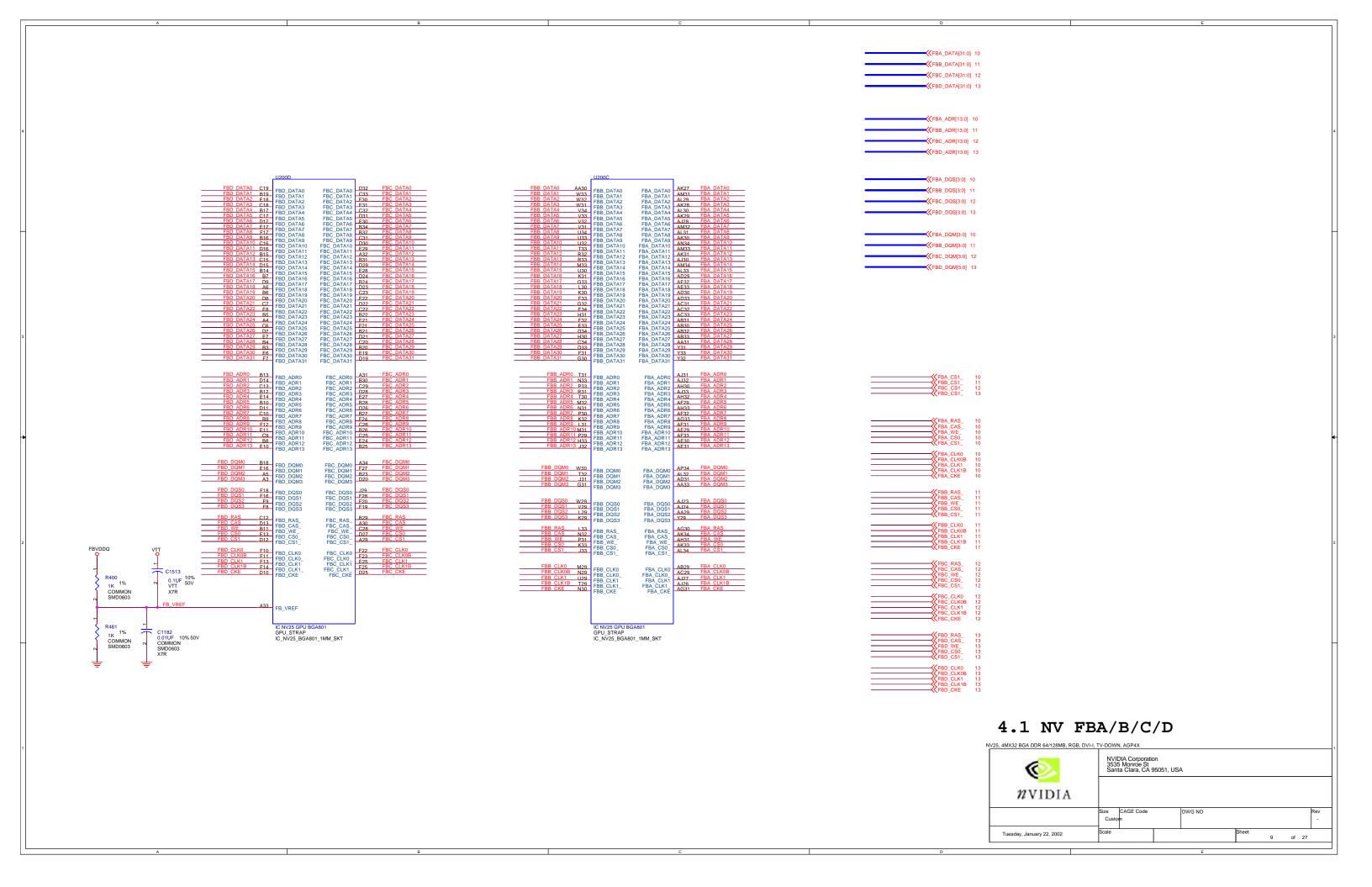
COMMON SMD0402 R977 1 2 10k 5% NO STUFF SMD0402 0 = 24 bit Flat Panel Interfave
1 = 12 bit Flat Panel Interfave 15.17 VIP VID13 R978 1 2 10k 5% VIP HAD6 R979 1 2 10k 5% SMD0402 NO STUFF SMD0402 0 = Disabled 15,17 VIP_HAD6 R980 1 2 10k 5% VIP HAD7
COMMON SMD0402 R981 1 2 10k 5% NO STUFF SMD0402 0 = Disabled 15,17 VIP_HAD7 27 R982 1 2 10k 5% DVOBD12 R983 1 2 10k 5% SMD0402 COMMON SMD0402 STRAP_MULTICHIP_AGP_DEV 1 = 0 = Disabled 1 = 0 Enabled 17,20 DVOBD12 R984 1 2 10k 5% DVOBD13 NO_STUFF SMD0402 R985 1 2 10k 5% COMMON SMD0402 STRAP_MULTICHIP_IO_DEV 1 0 = Disabled 1 = Enabled 17,20 DVOBD13 < R986 1 2 10k 5% DVOD14
COMMON SMD0402 [1..0] - STRAP_ROM 00 = PARALLEL 01 = SERIAL AT25F R987 1 2 10k 5% NO_STUFF SMD0402 STRAP_ROM_0 17.18 DVOD14 30 17,18 DVOD15 R988 1 2 10k 5% COMMON SMD0402

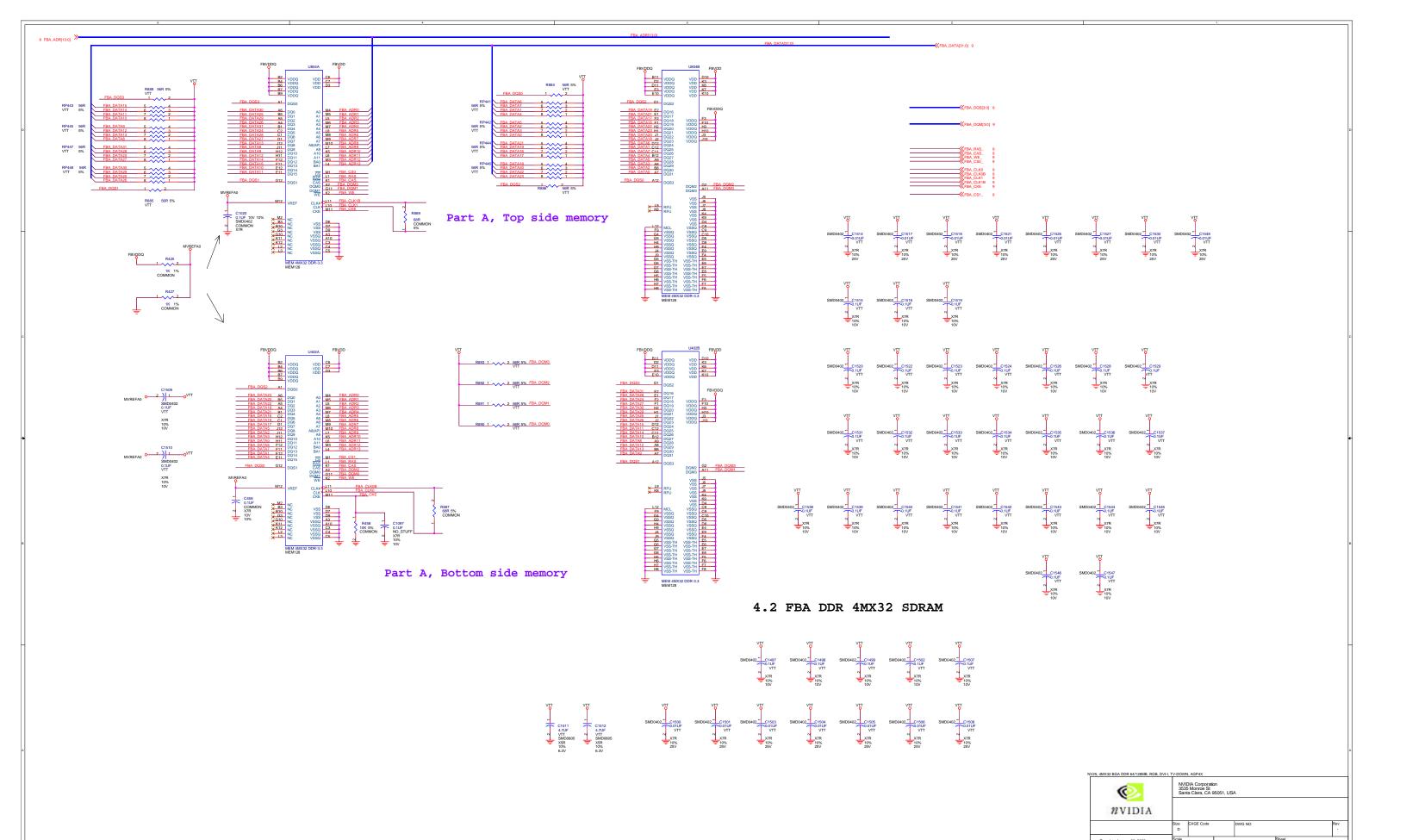
3.0 NV STRAP

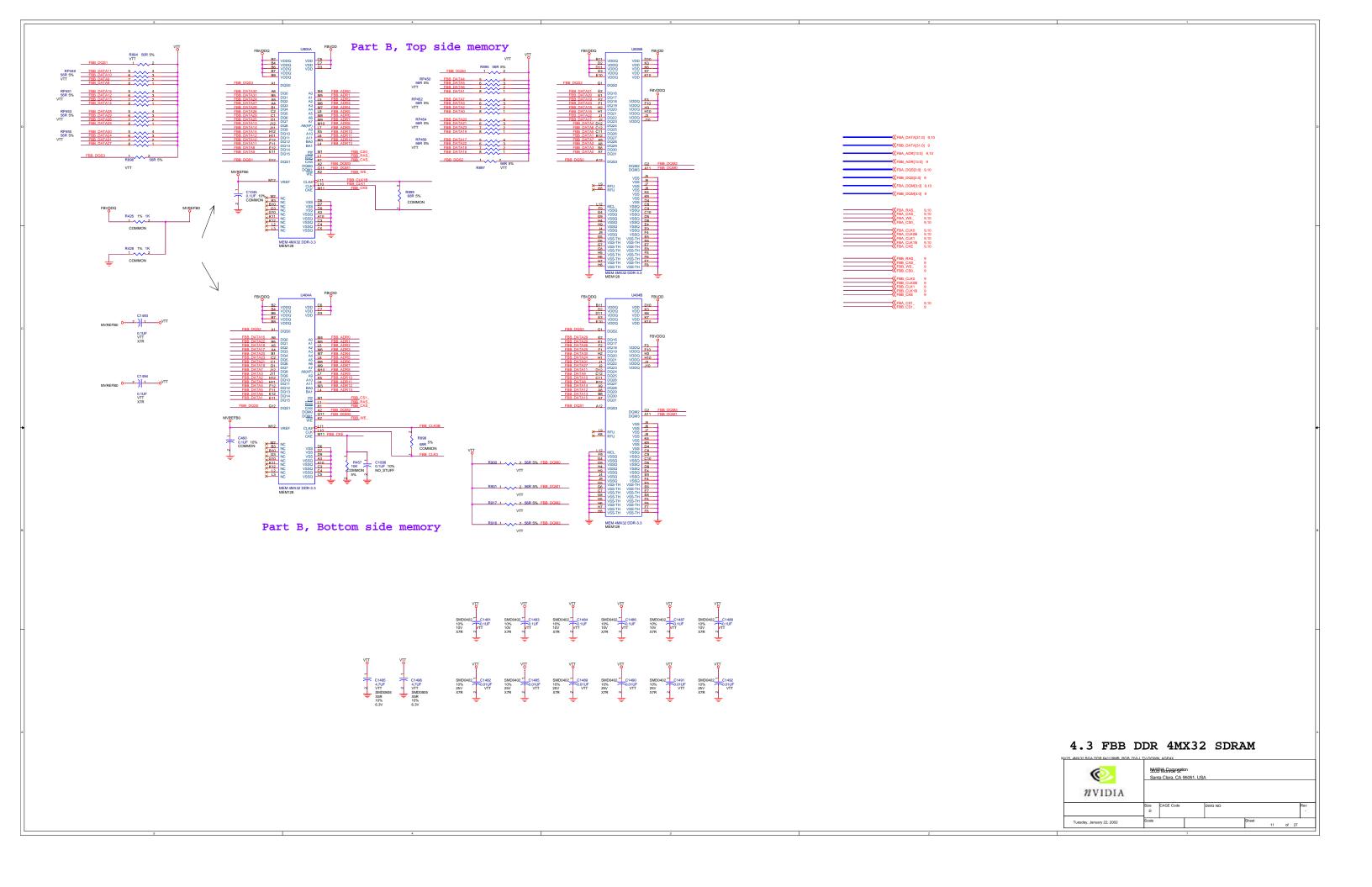
NVIDIA Corporation 3535 Monroe St Santa Clara, CA 95051, USA **@** NVIDIA Tuesday, January 22, 2002

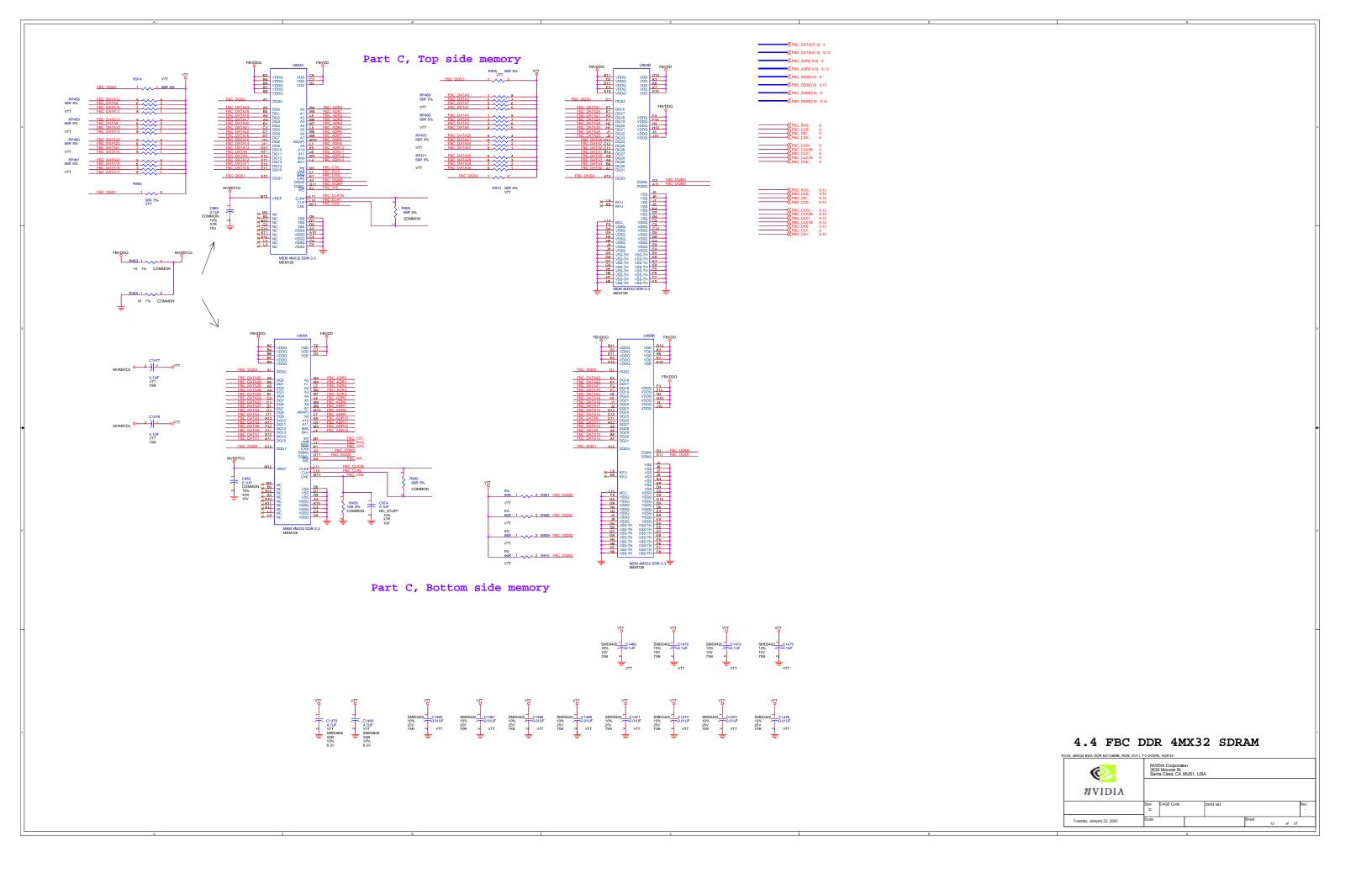


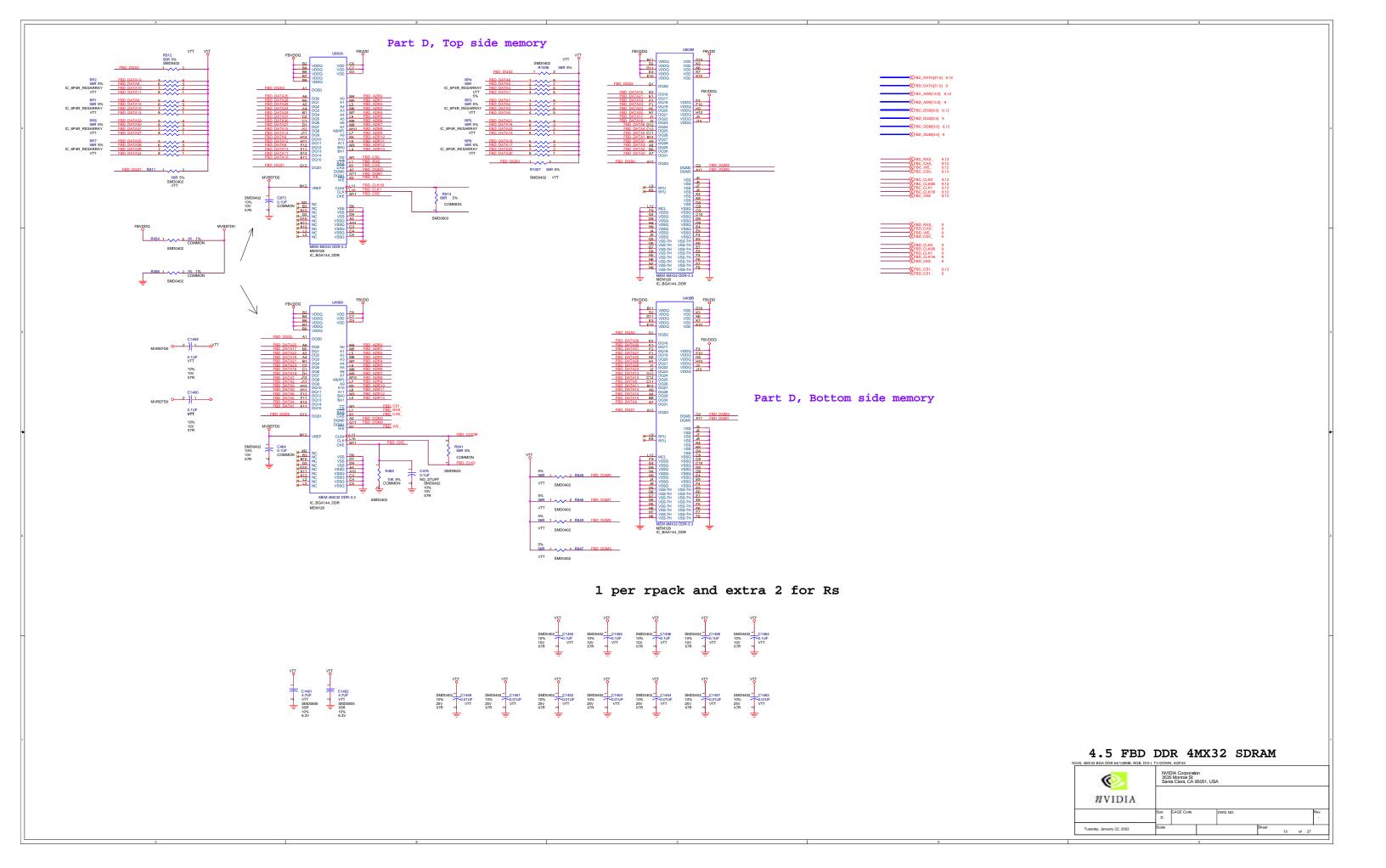








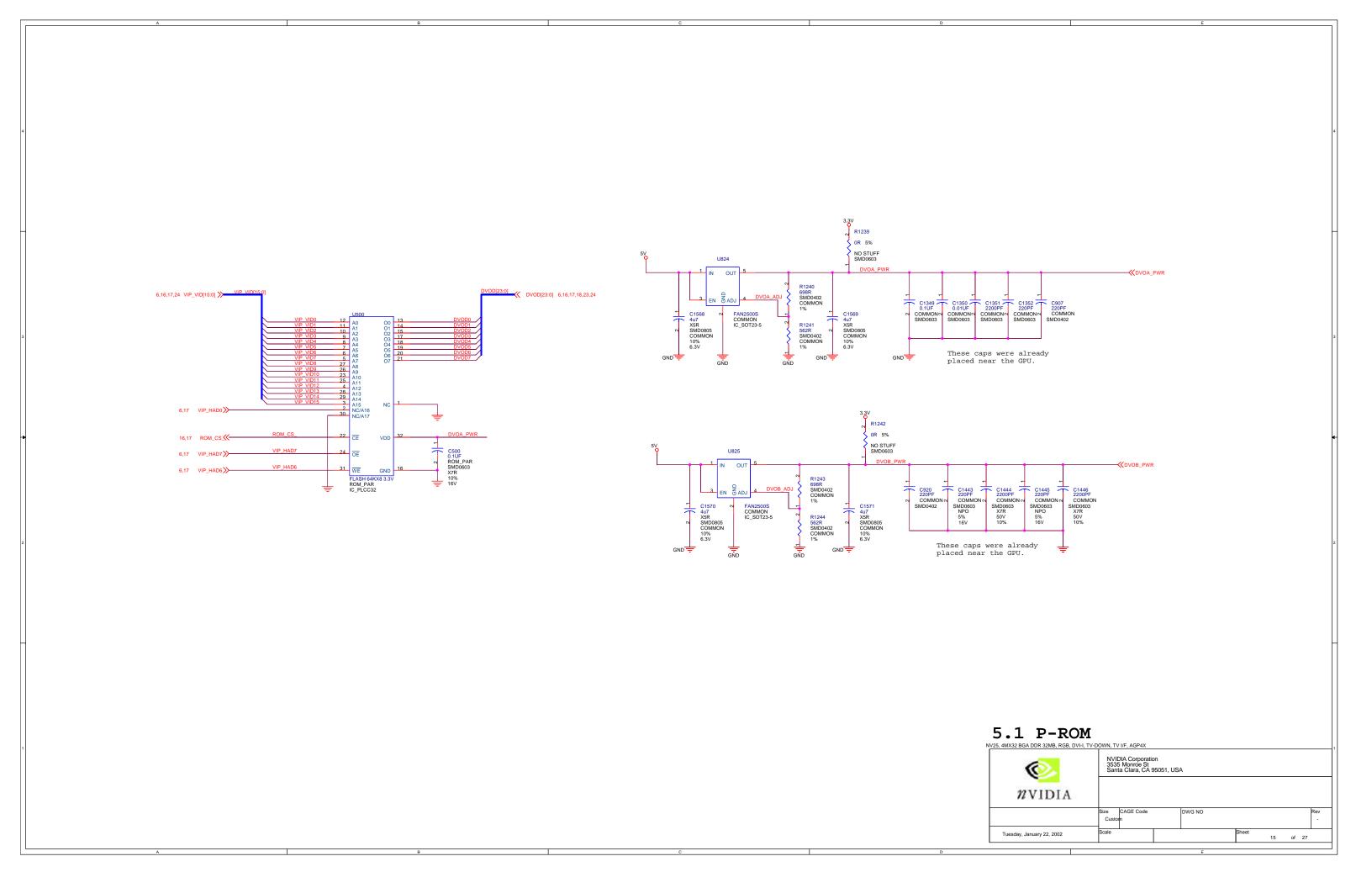


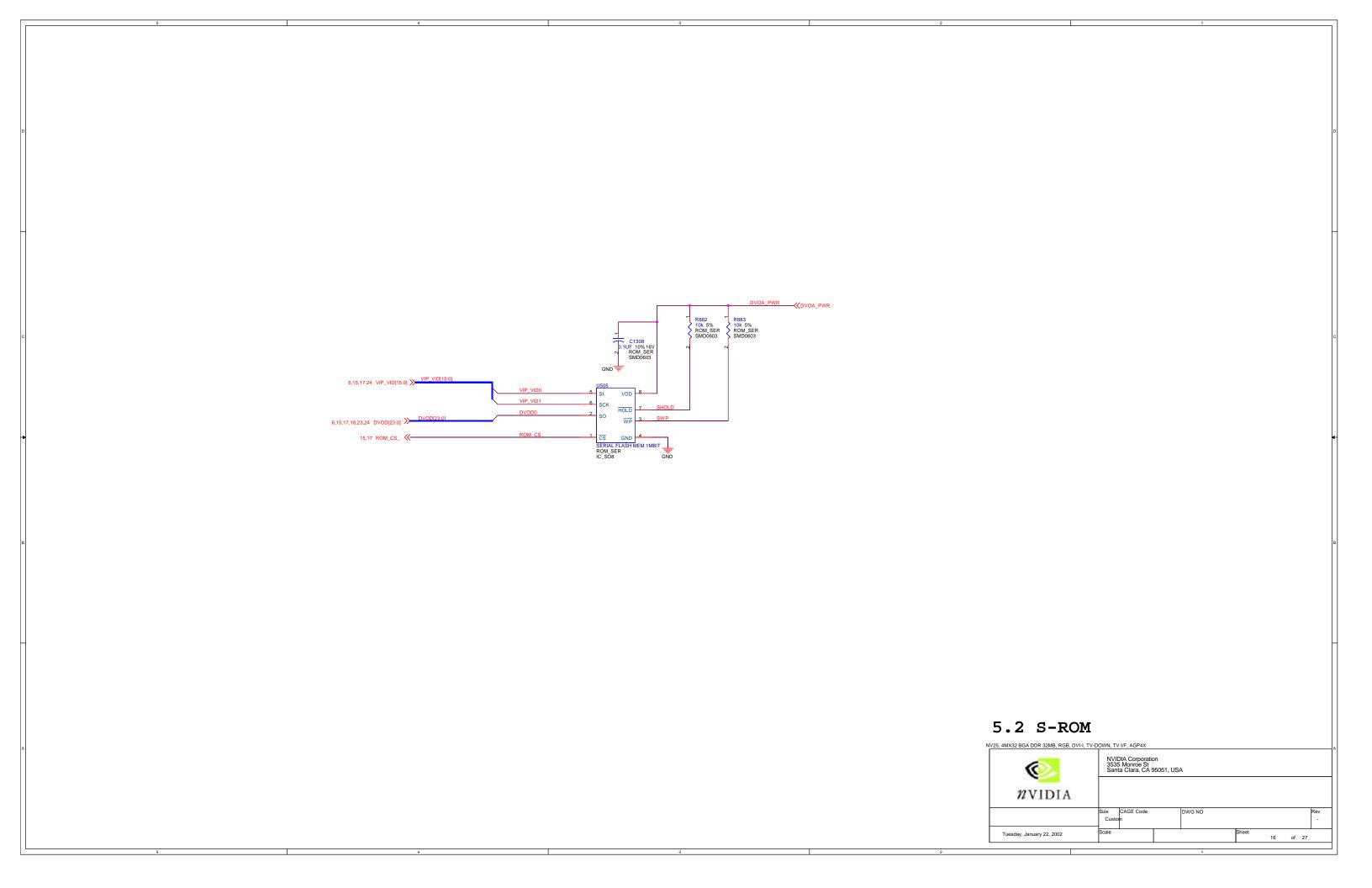


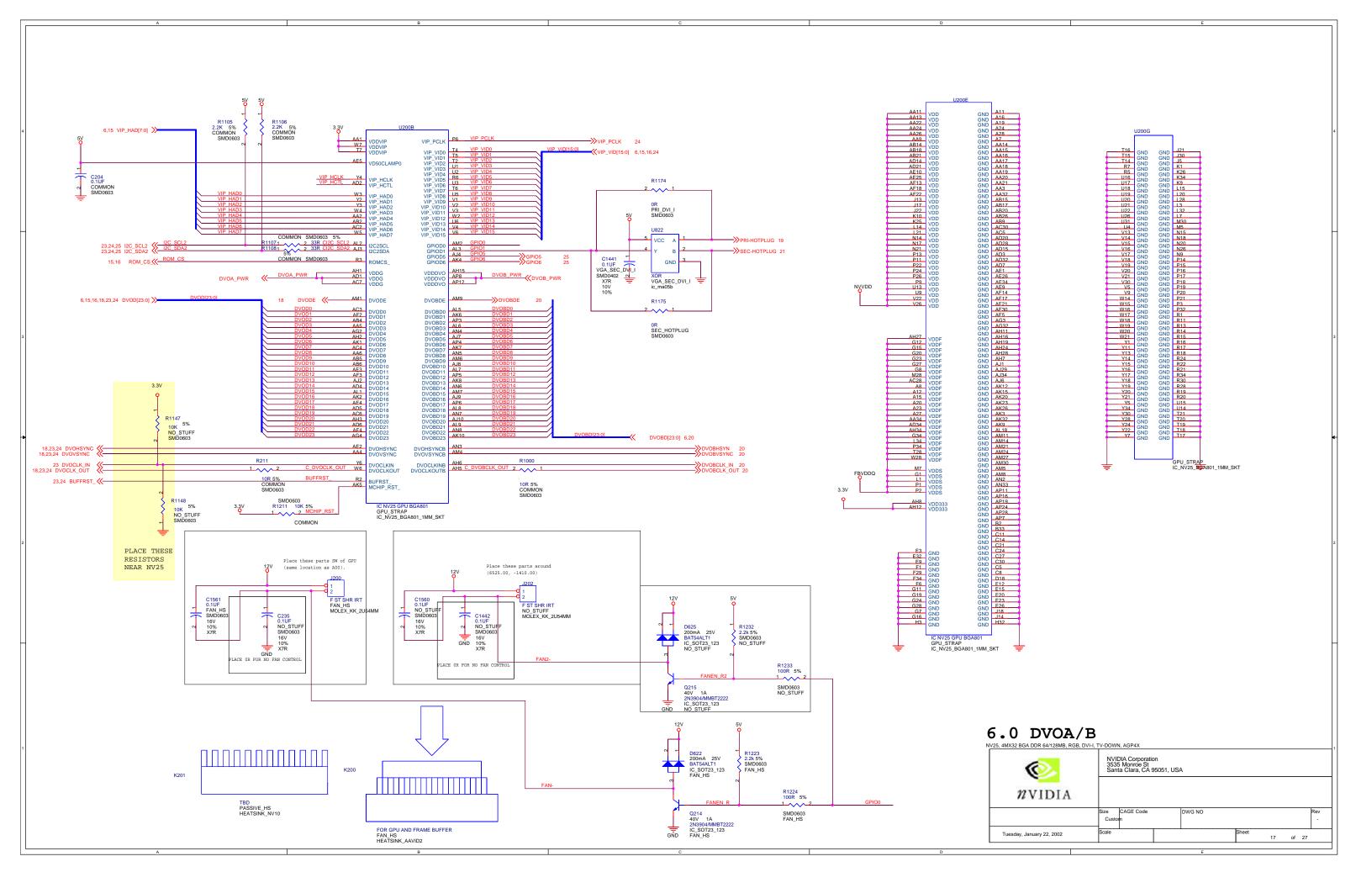


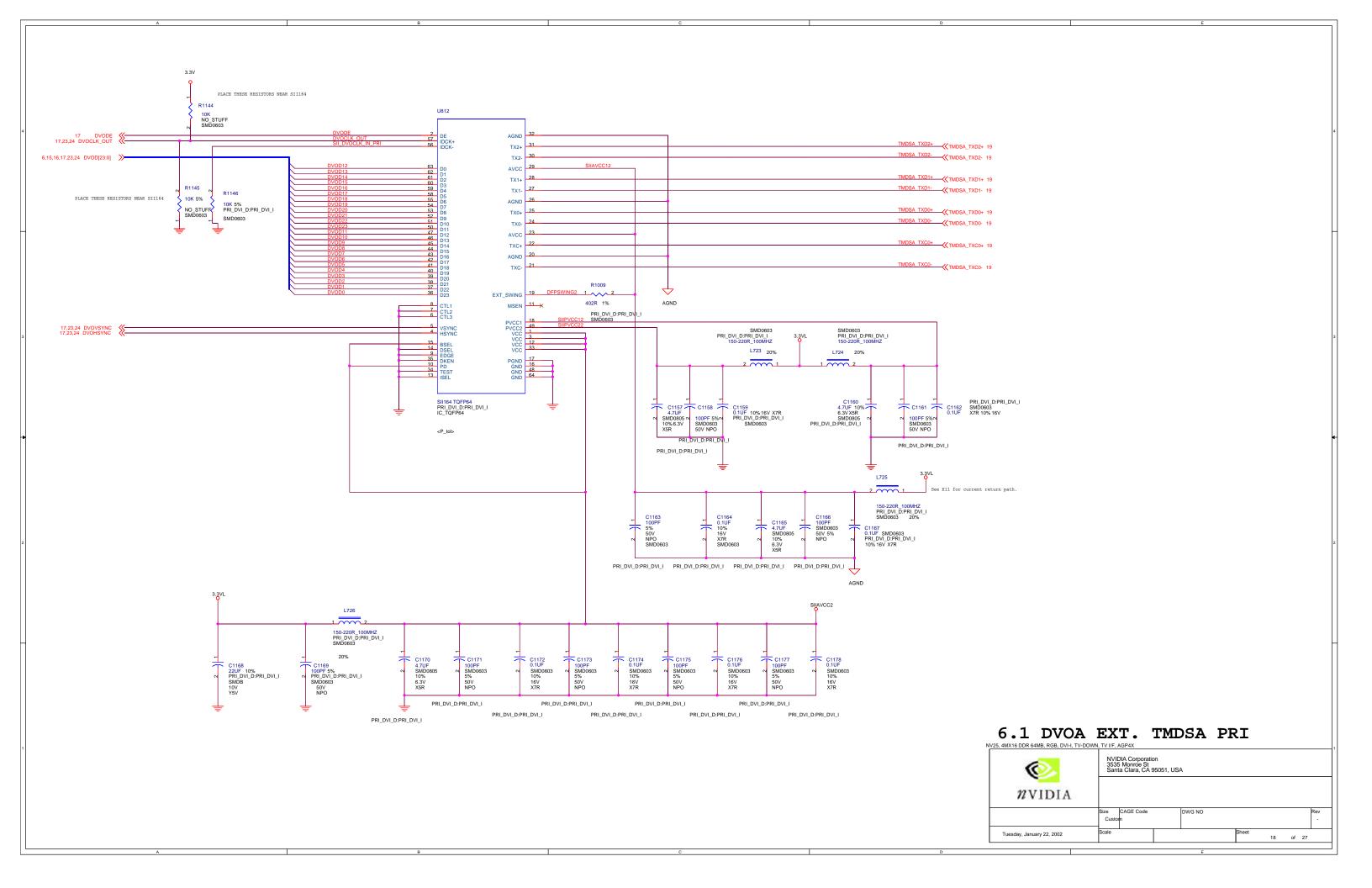
4.6 BGA MEMORY DECOUPLING

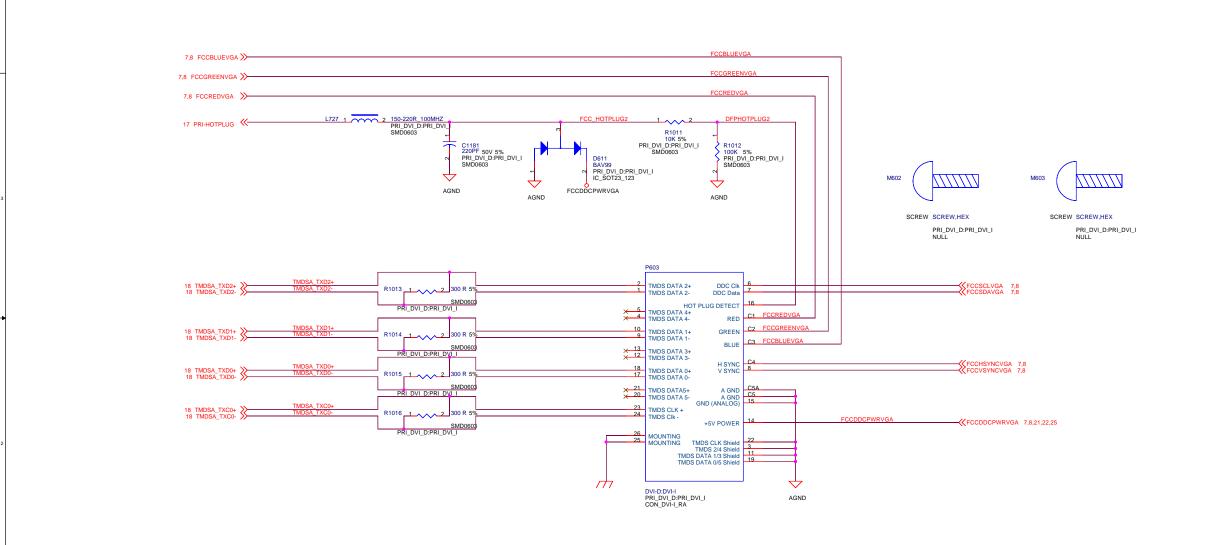
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nvidia										
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Tuesday, January 22, 2002	Scale				Sheet	14	of	27		





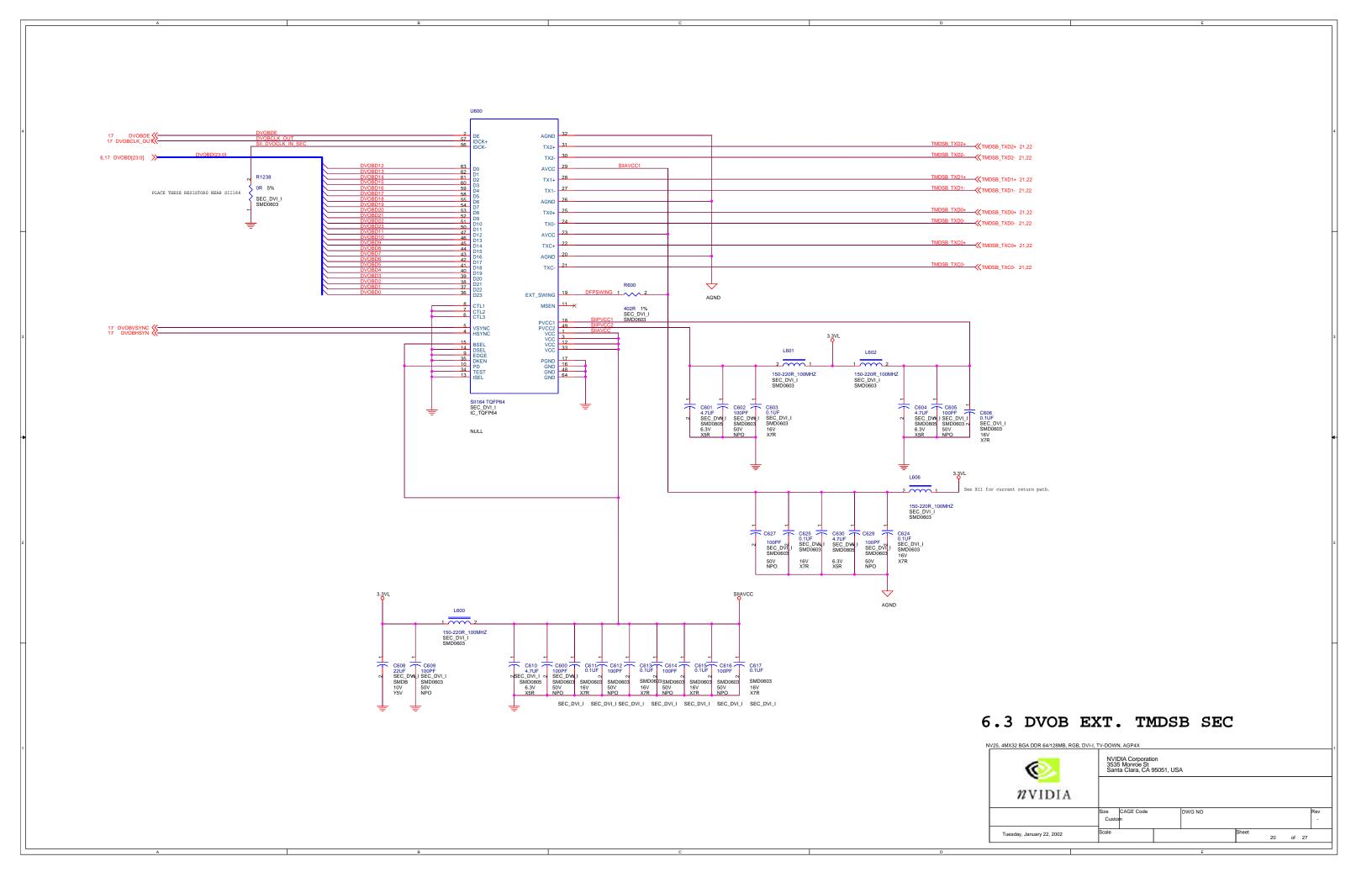


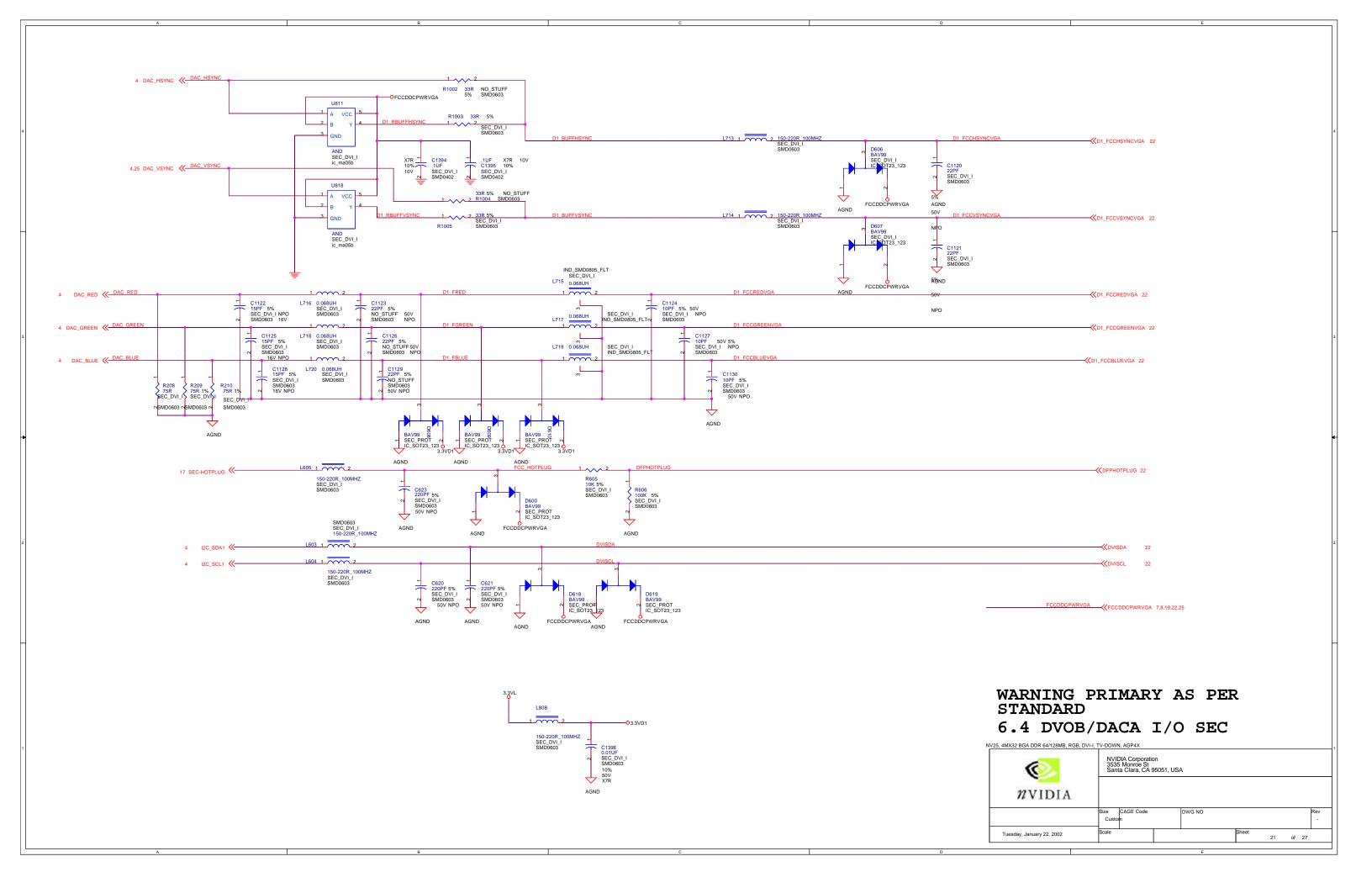


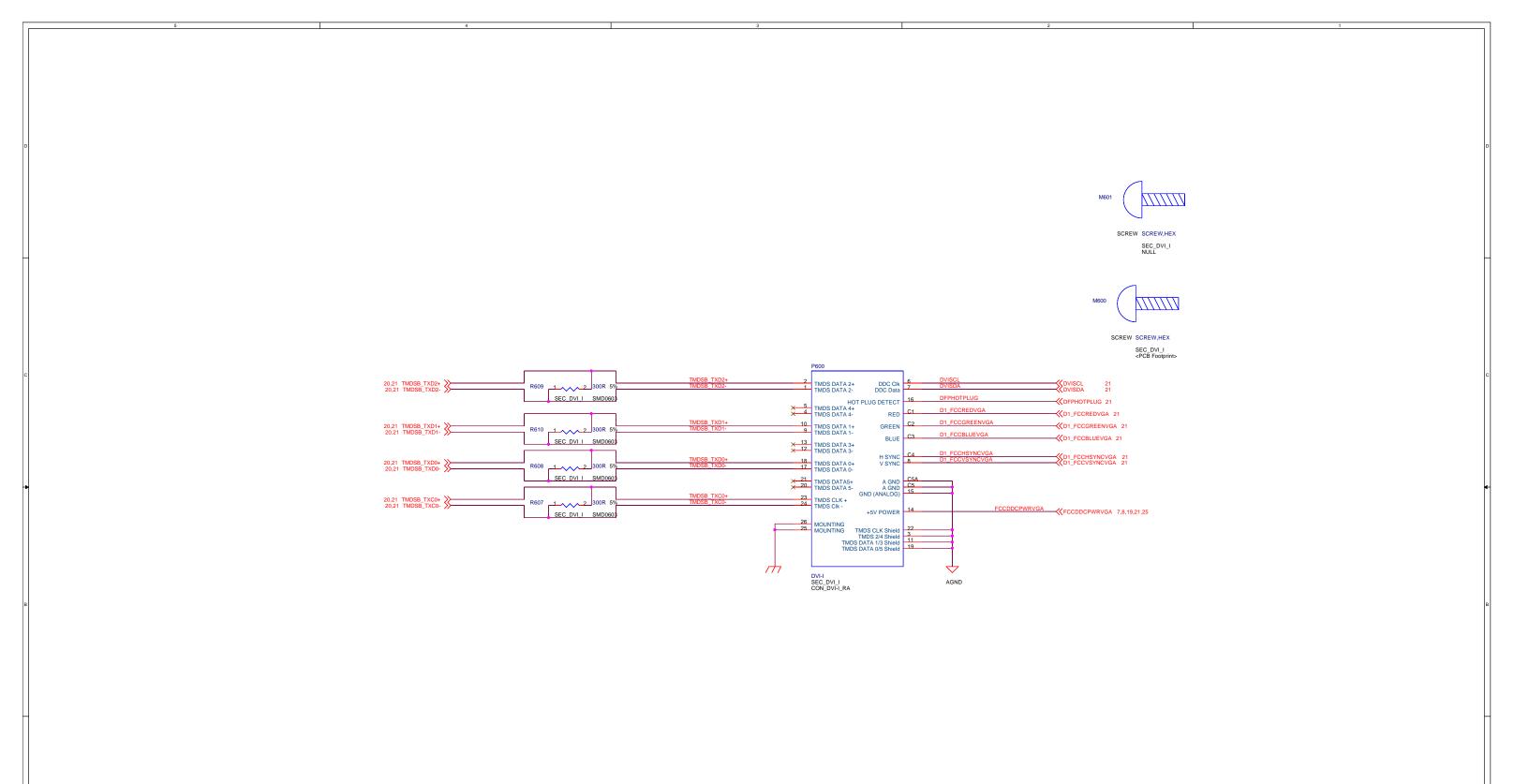


6.2 DVOA EXT. TMDSA I/O PRI

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, I	NVIDIA Corporation 3535 Monroe St Santa Clara, CA 95051, USA								
nvidia									
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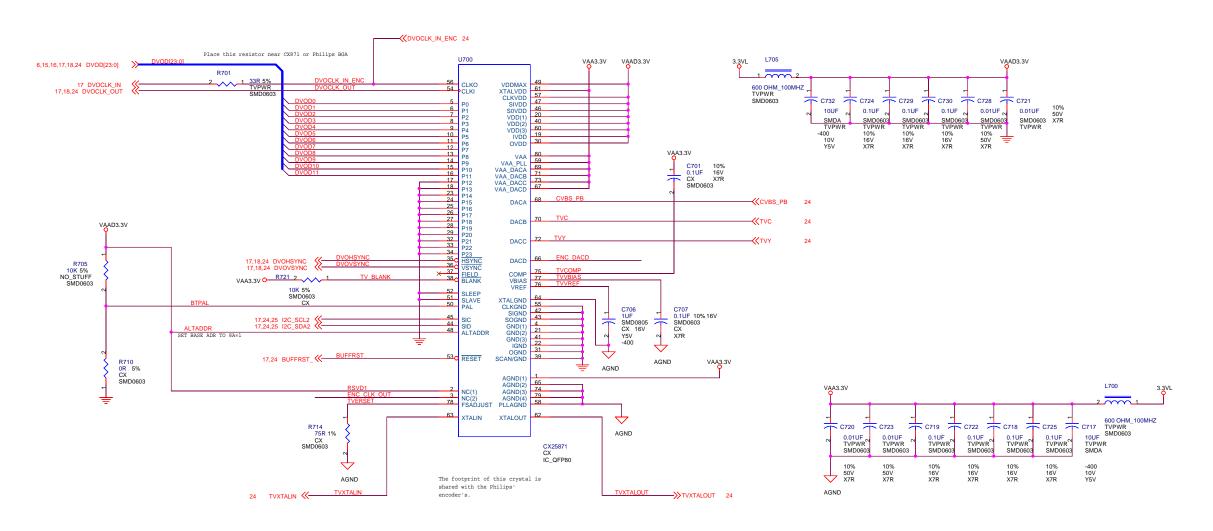






6.5 DVOB/DACA CONNECTOR

NV25, 4MA32 BGA DDR 64/128MB, RGB, DVI-I,	NVIDIA Corporation 3535 Monroe St Santa Clara, CA 95051, USA								
nvidia									
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IC CX DIGITAL VIDEO ENCODER CX25871

7.1 TV-CX ENCODER

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X											
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nvidia											
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Tuesday, January 22, 2002	Scale				Sheet	23	of	27			

