

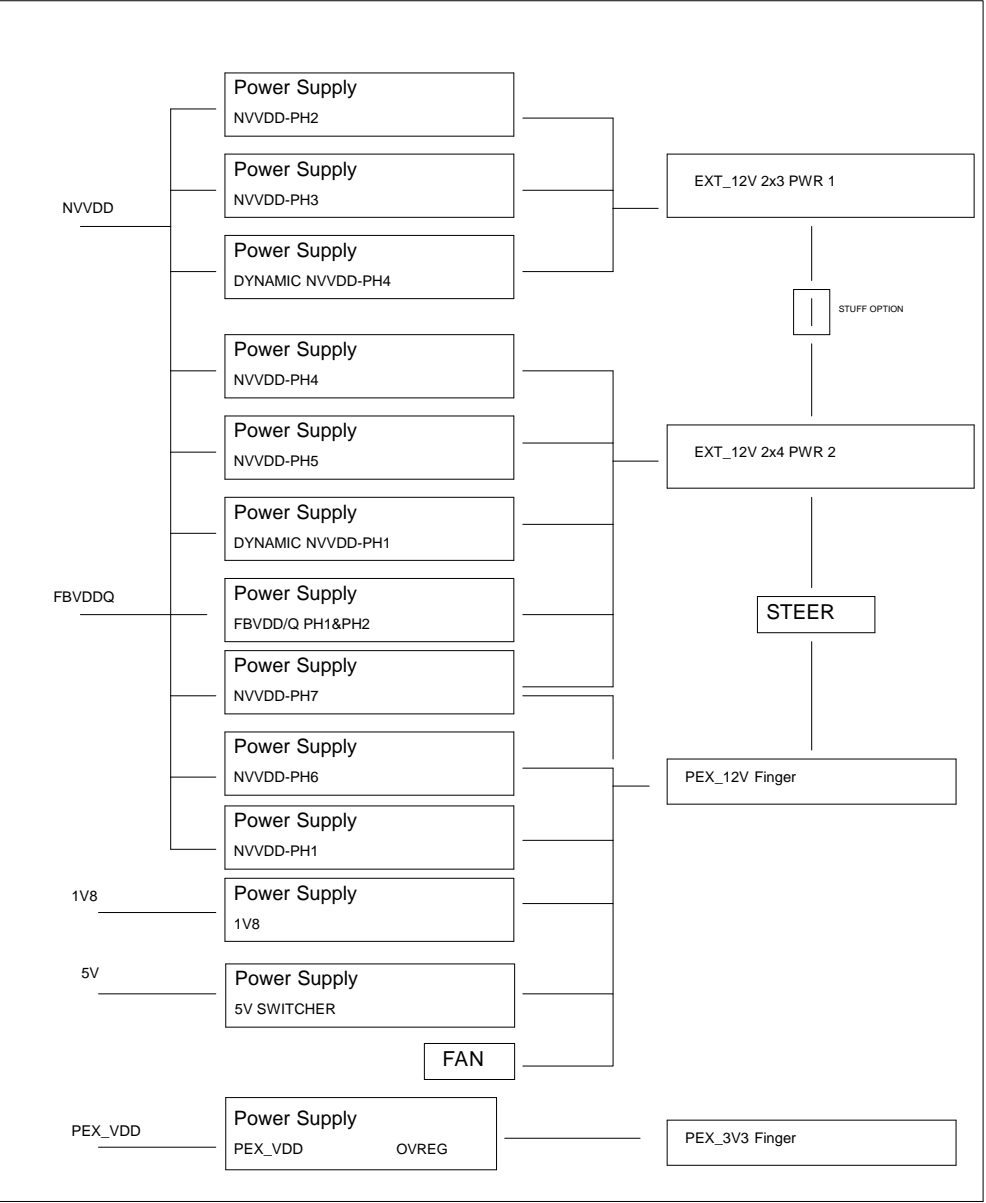
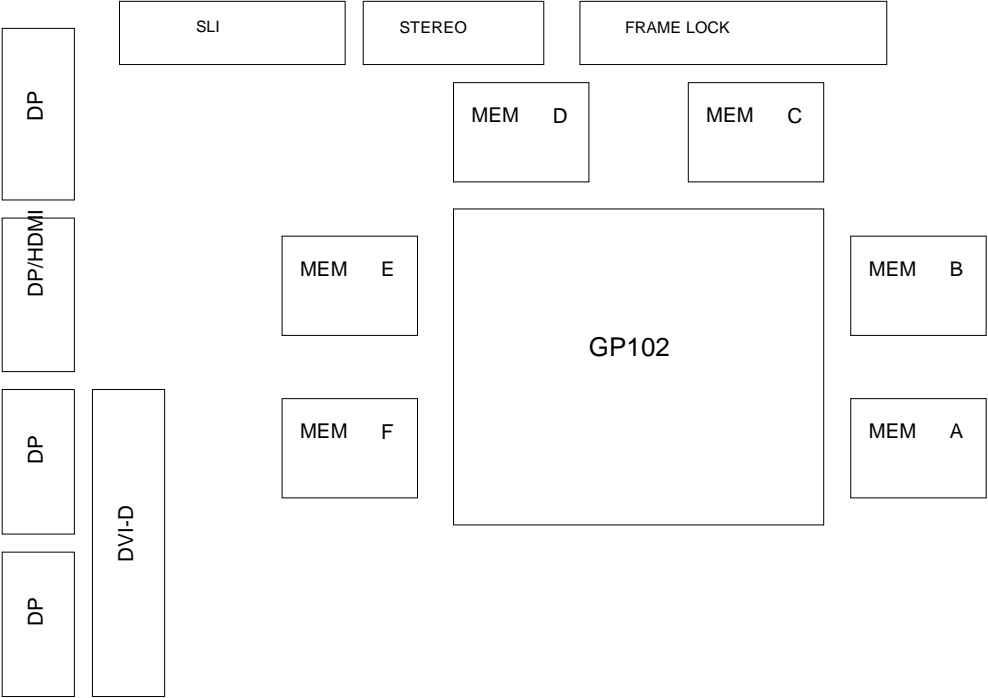
PG611 A00

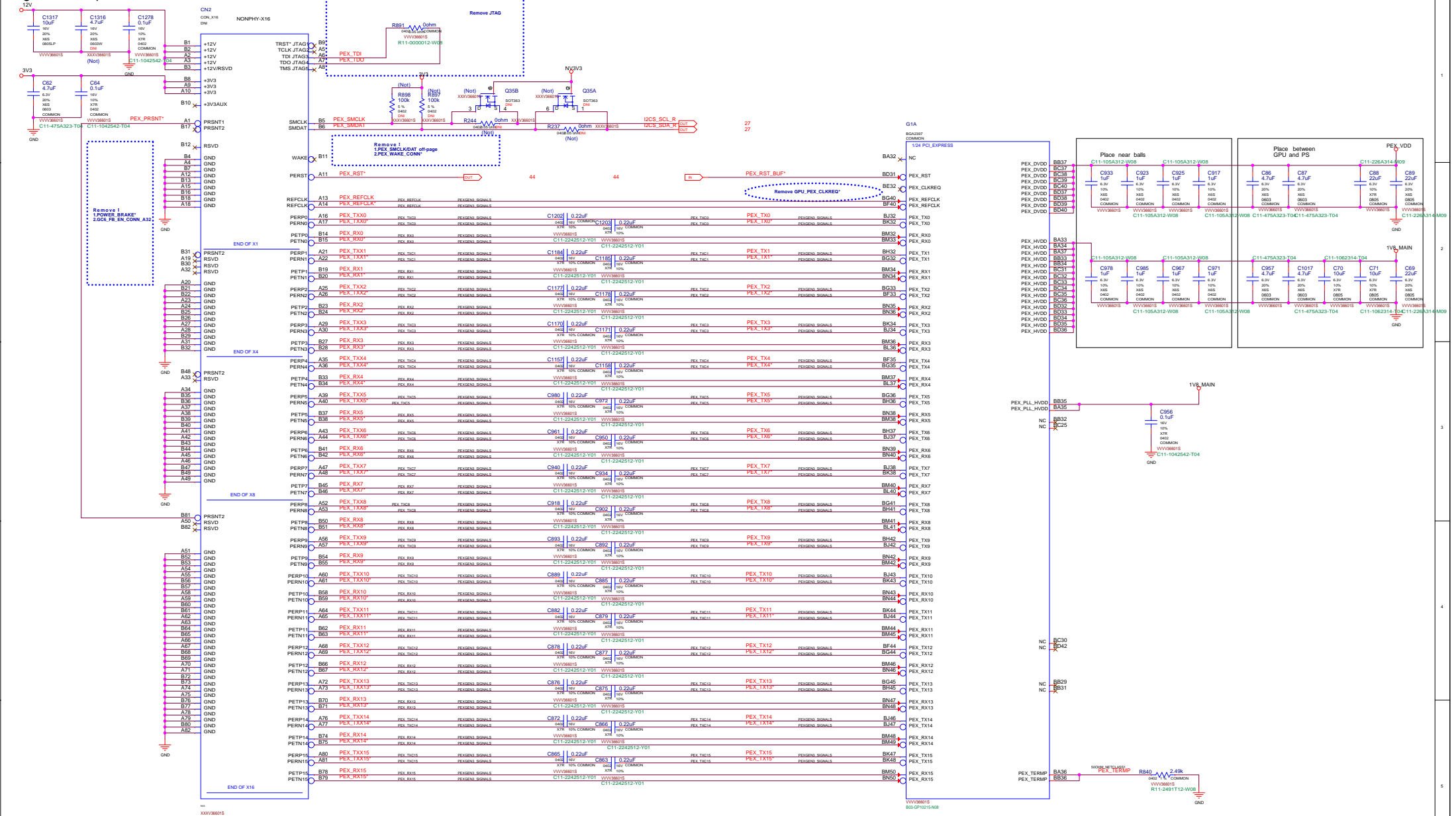
12GB GDDR5X, 384b, 256Mx32

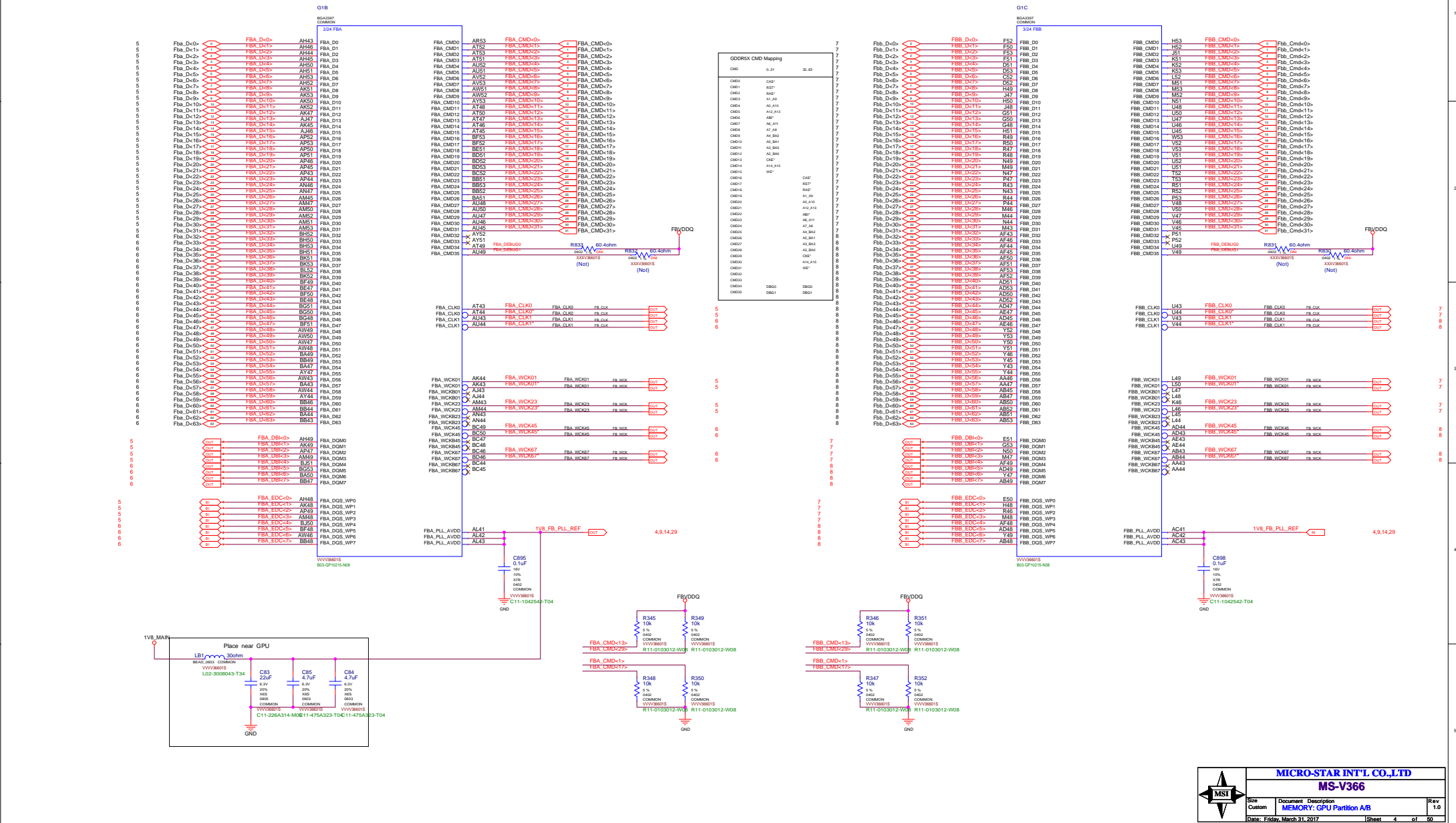
TALL DVI-D + DP + DP + HDMI/DP + DP

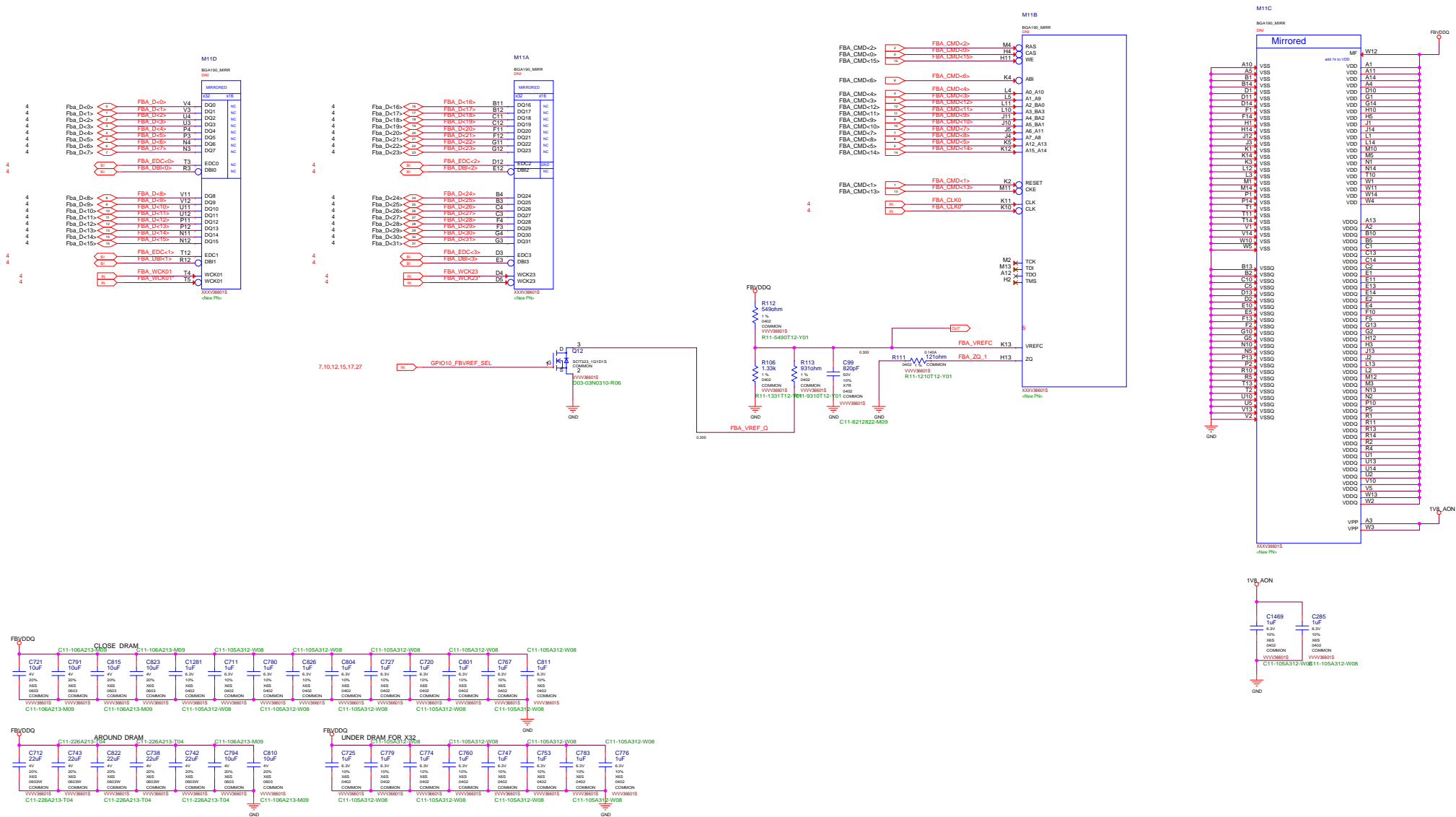
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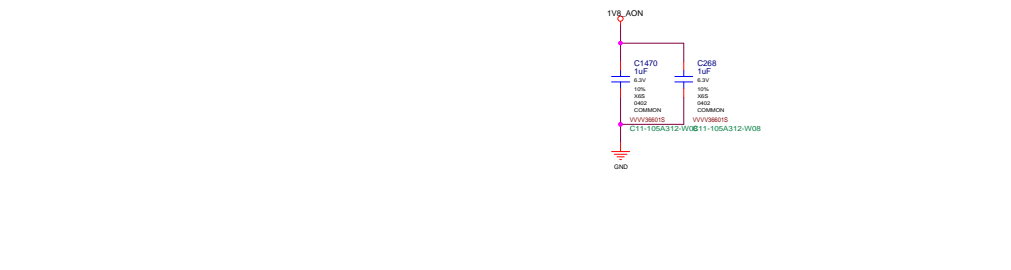
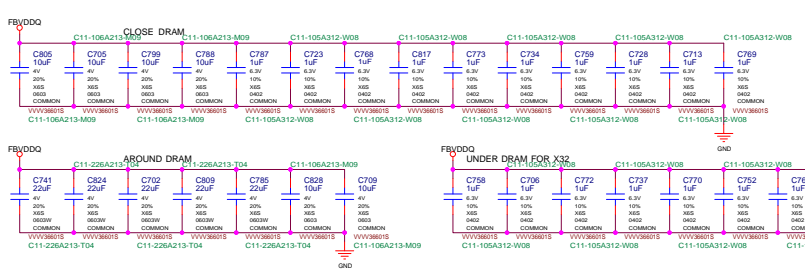
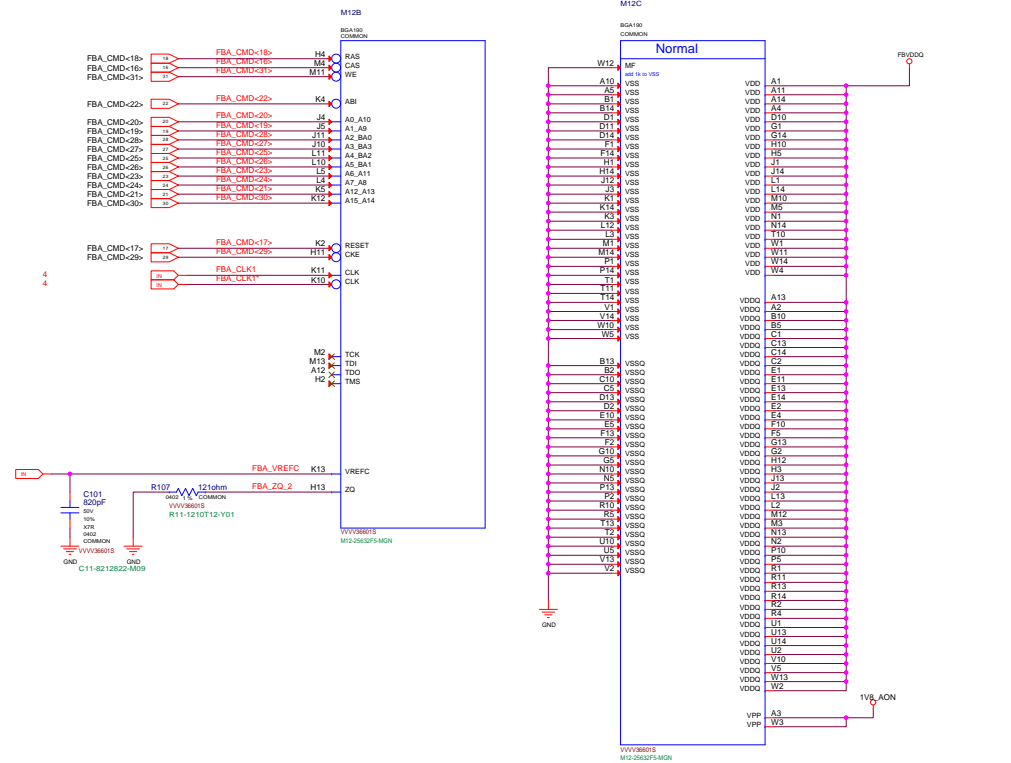
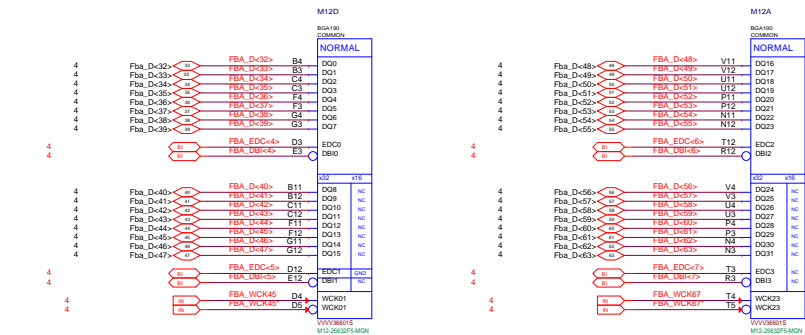
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22	IFPE DP	47	PS: MCU
23	IFPF DP	48	MECH
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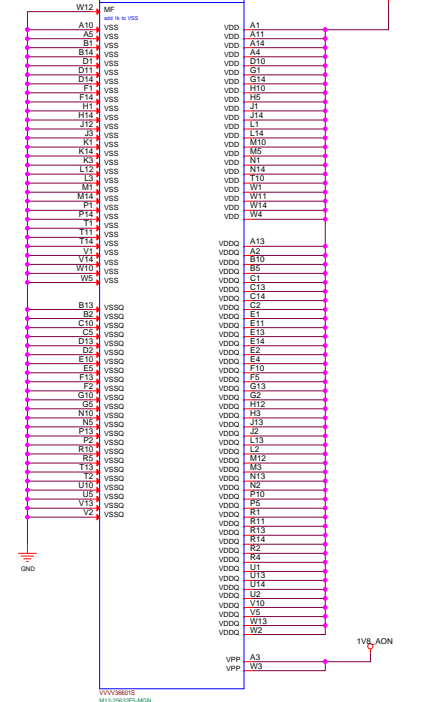
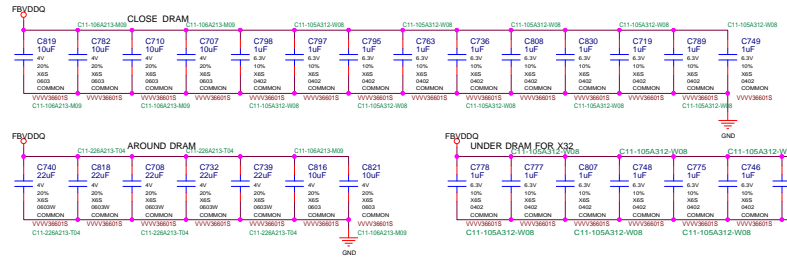
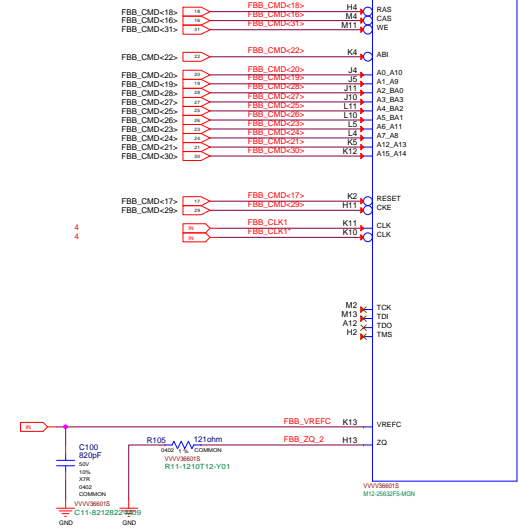
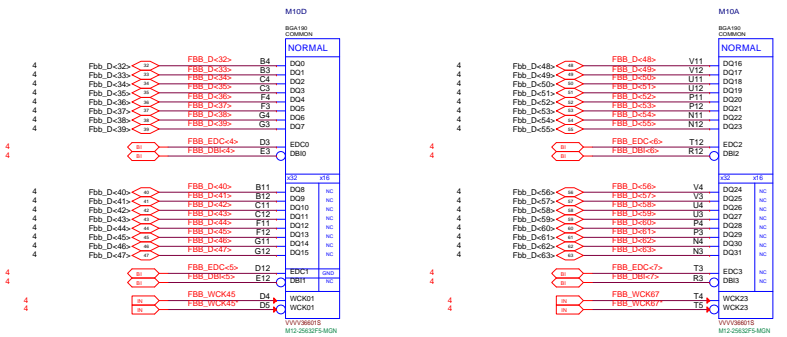


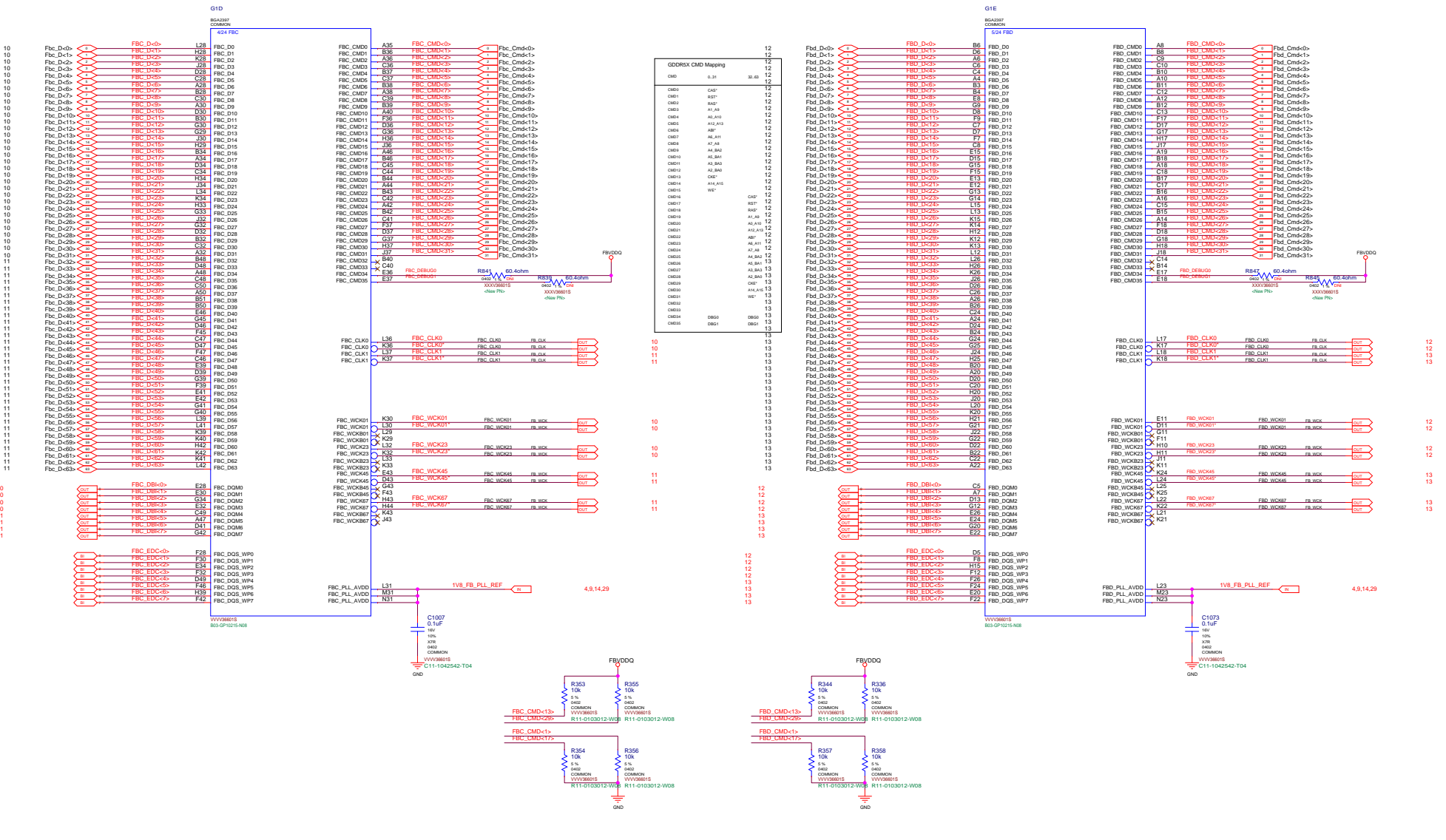


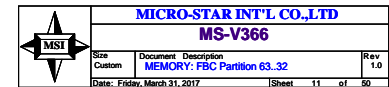
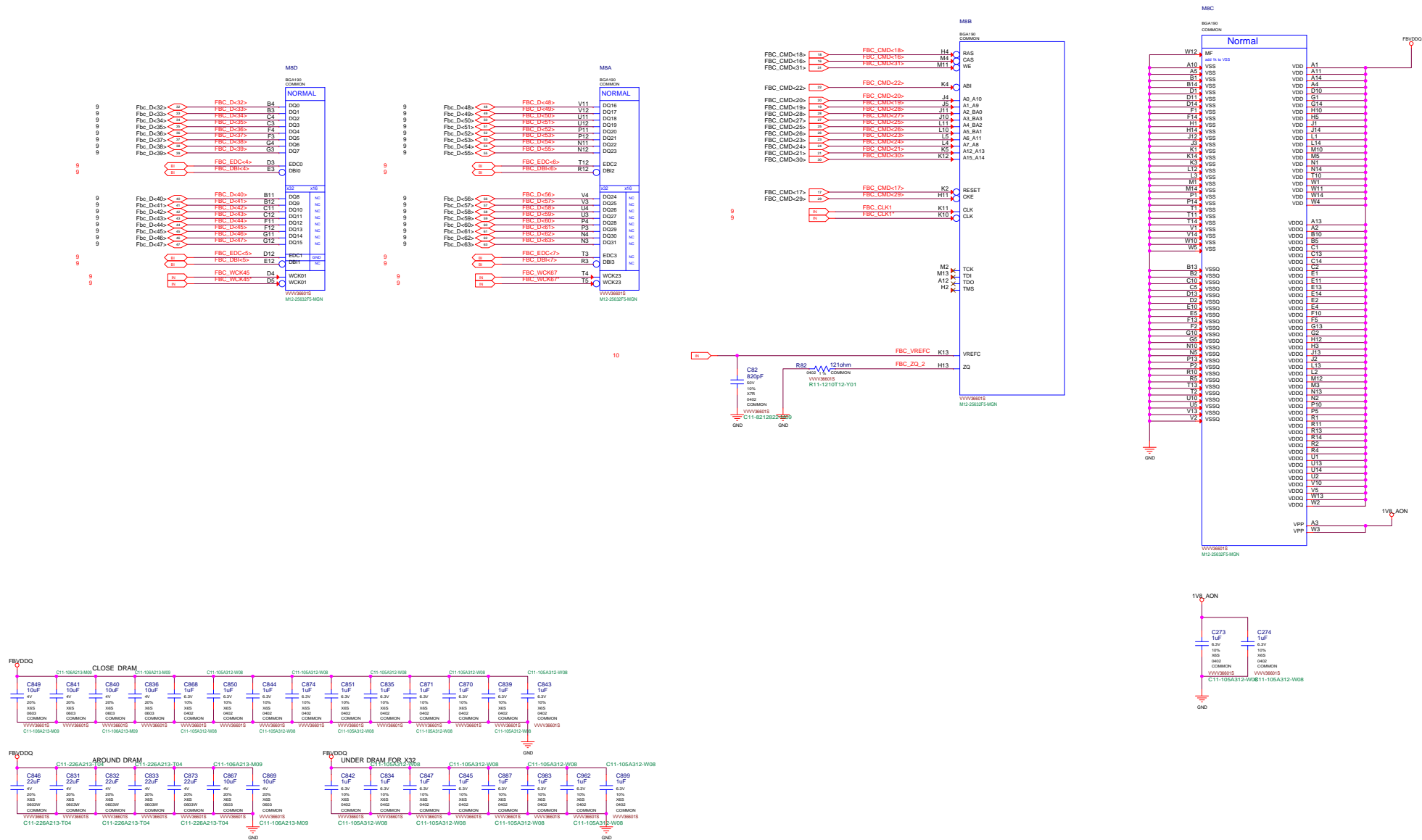


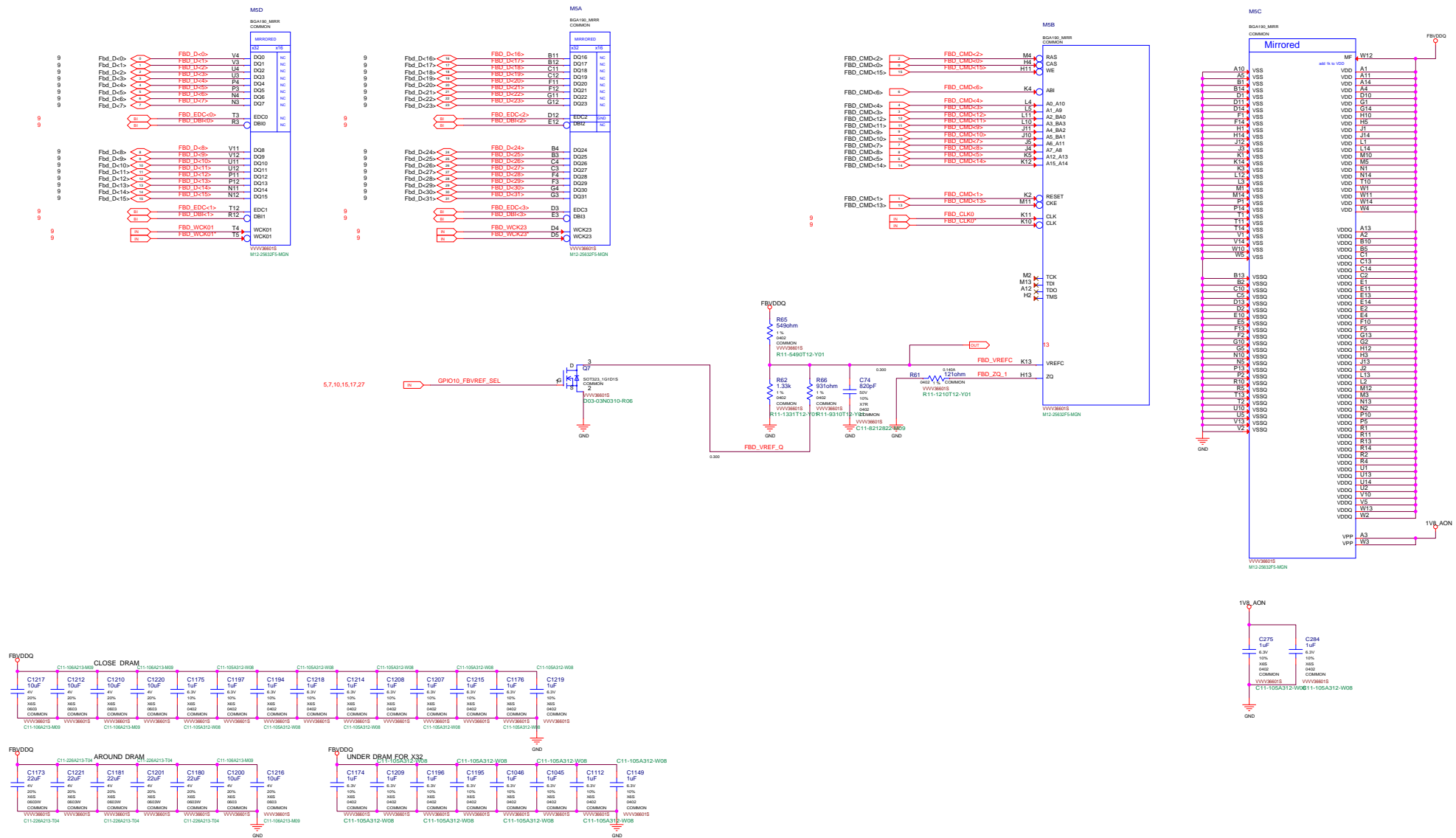


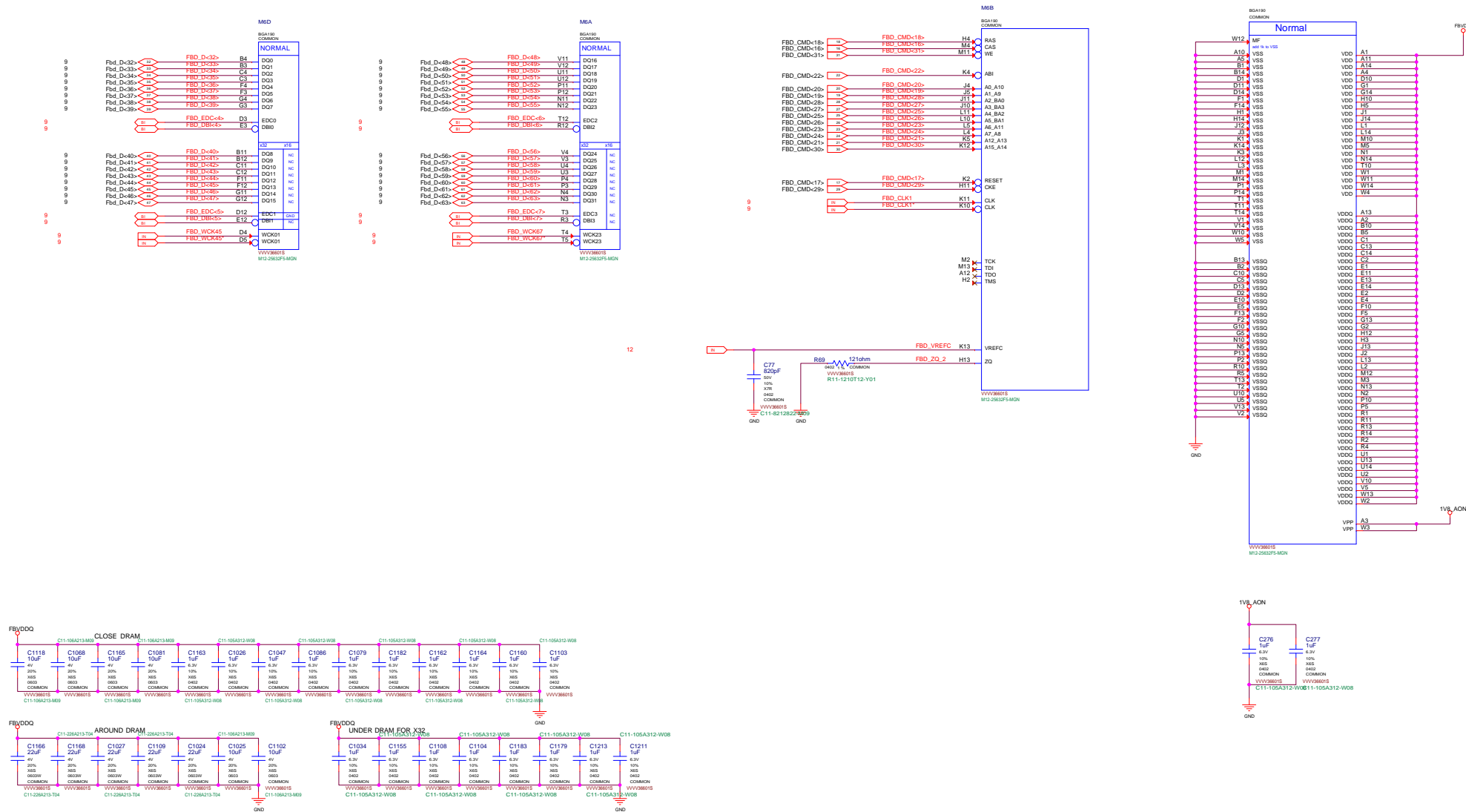


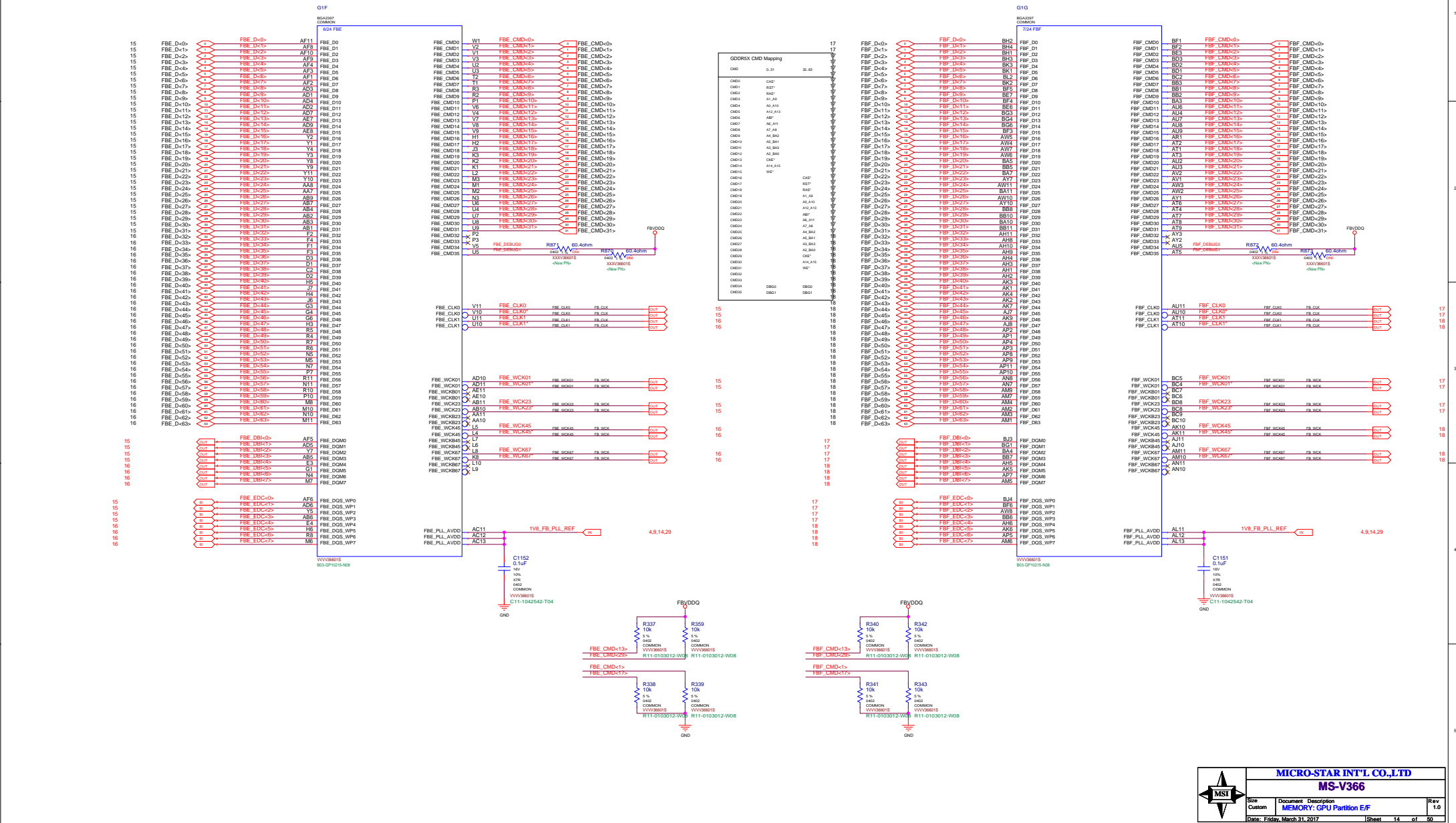


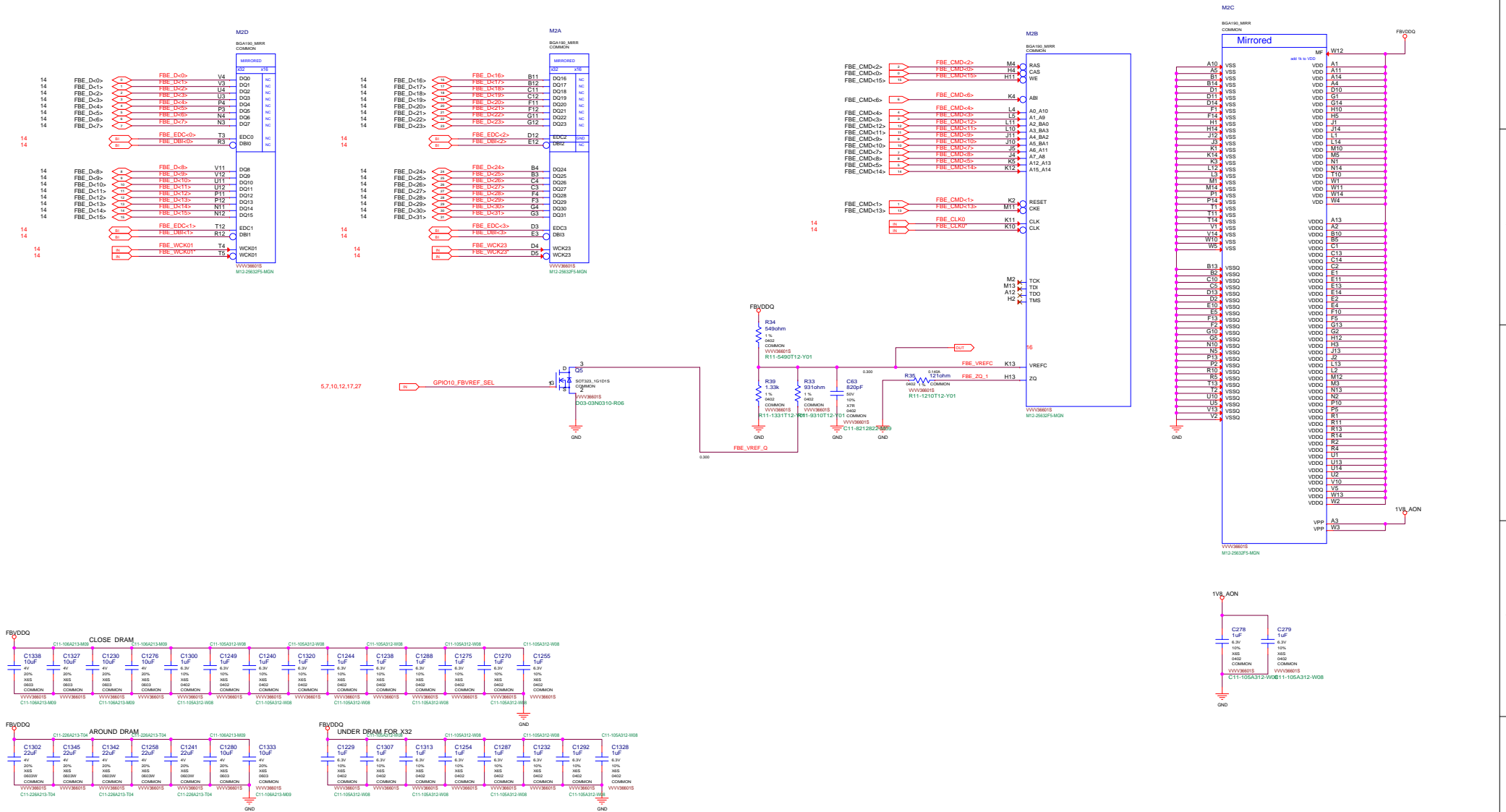


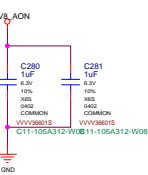
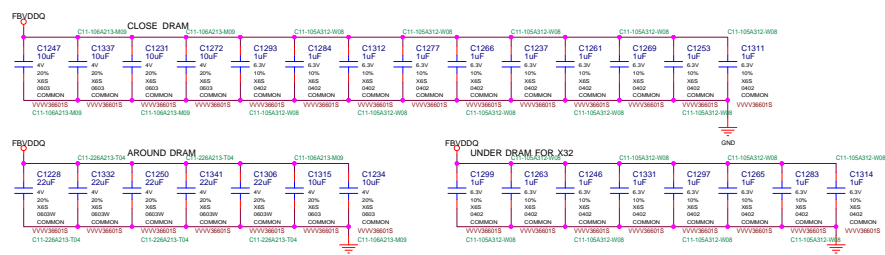
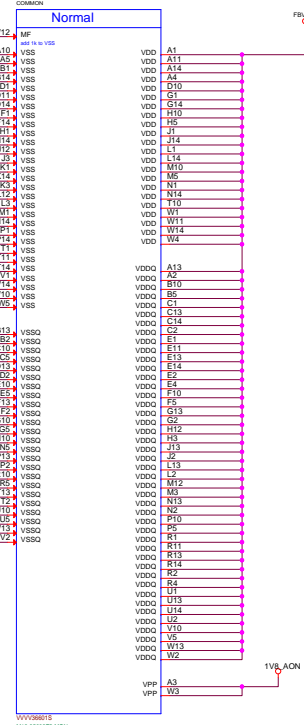
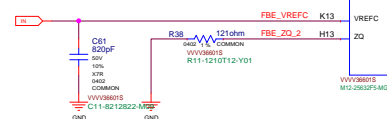
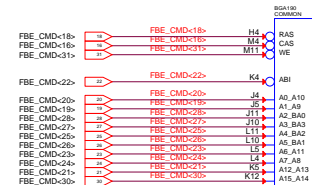
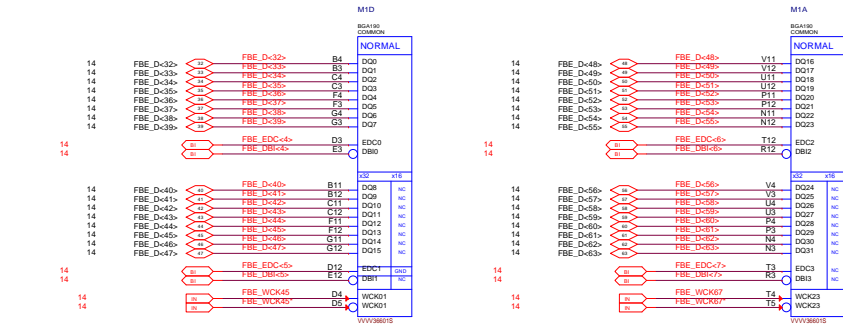






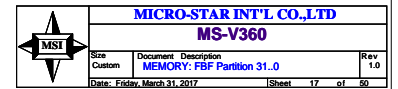
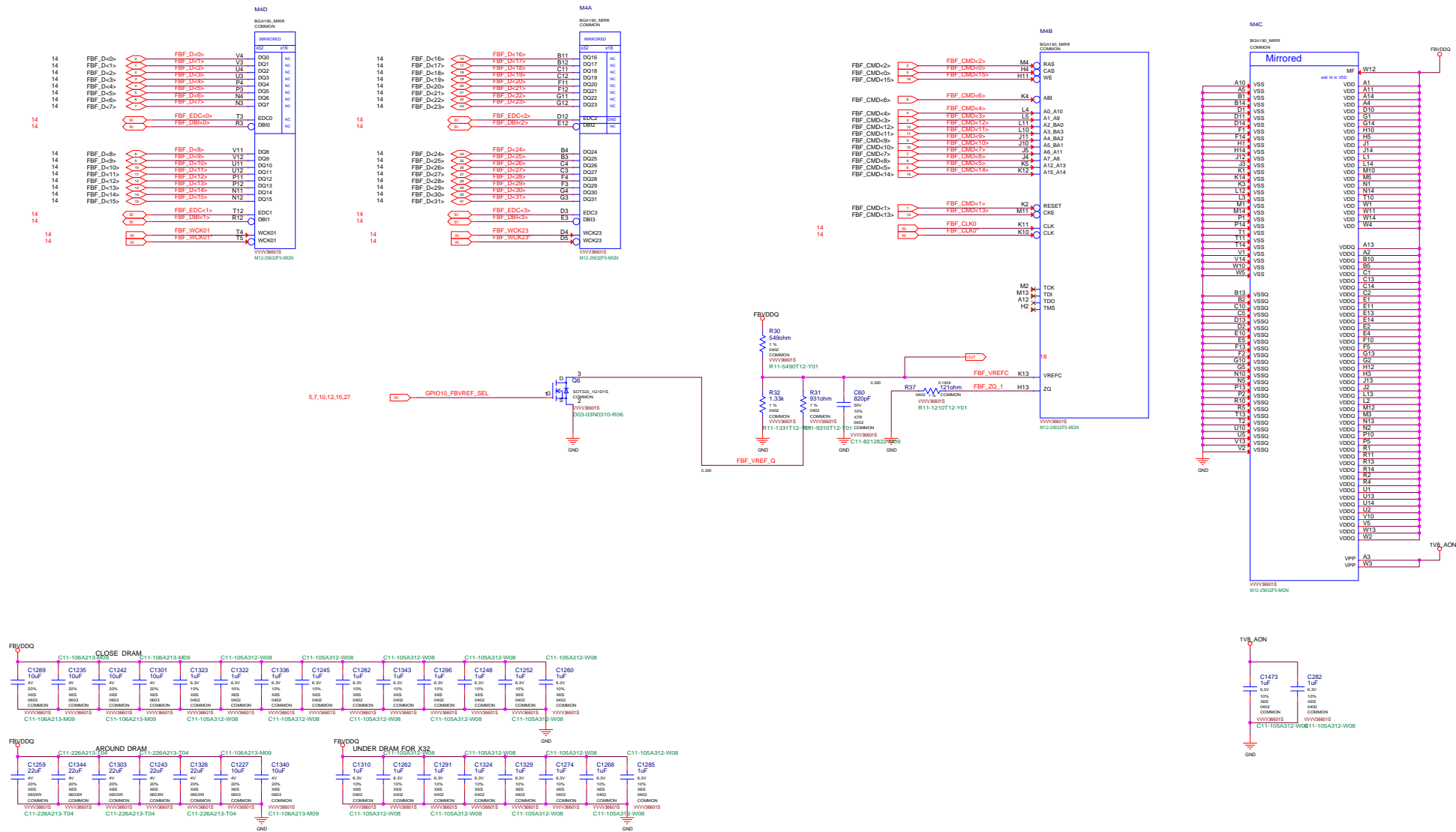


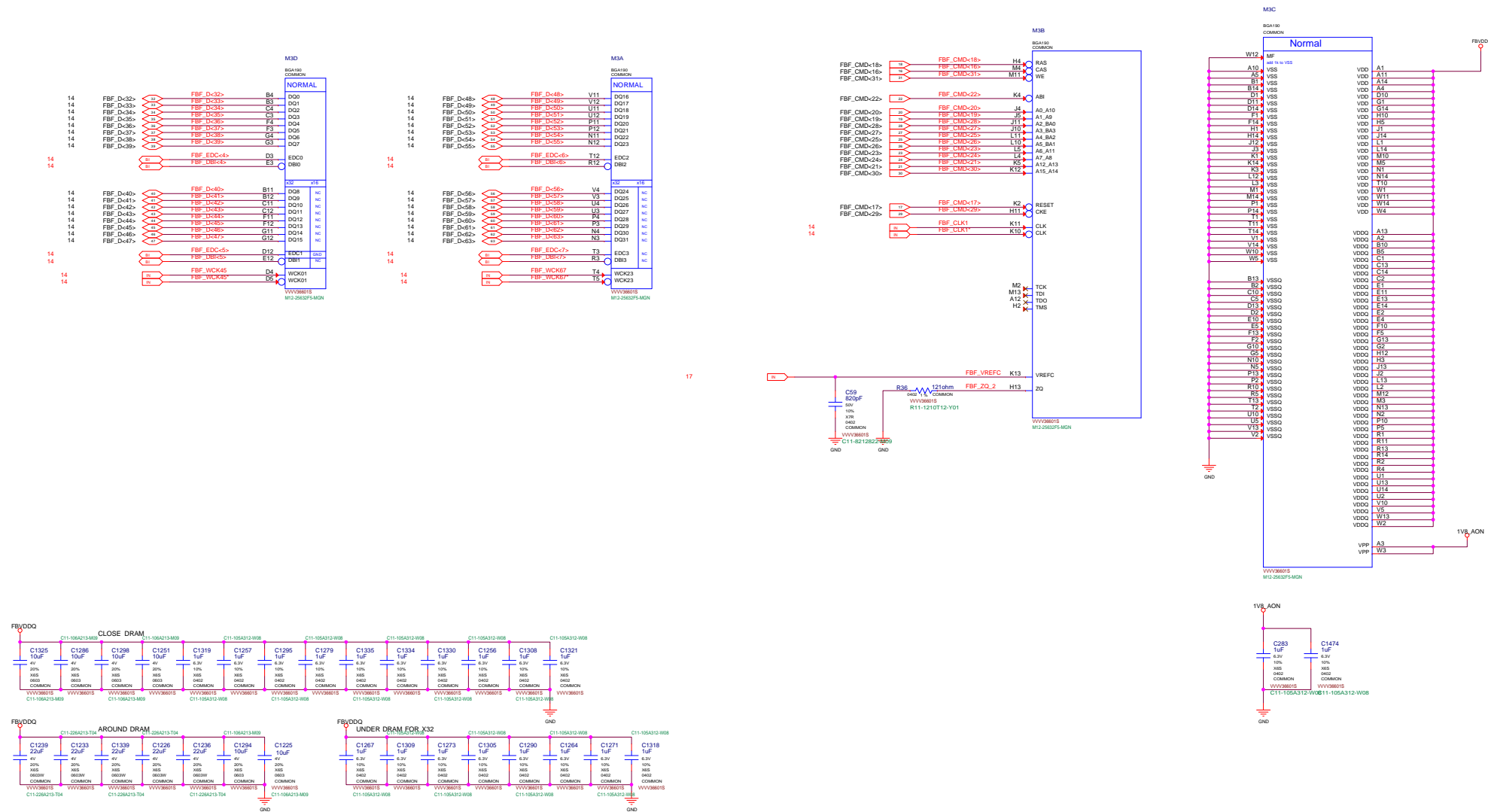


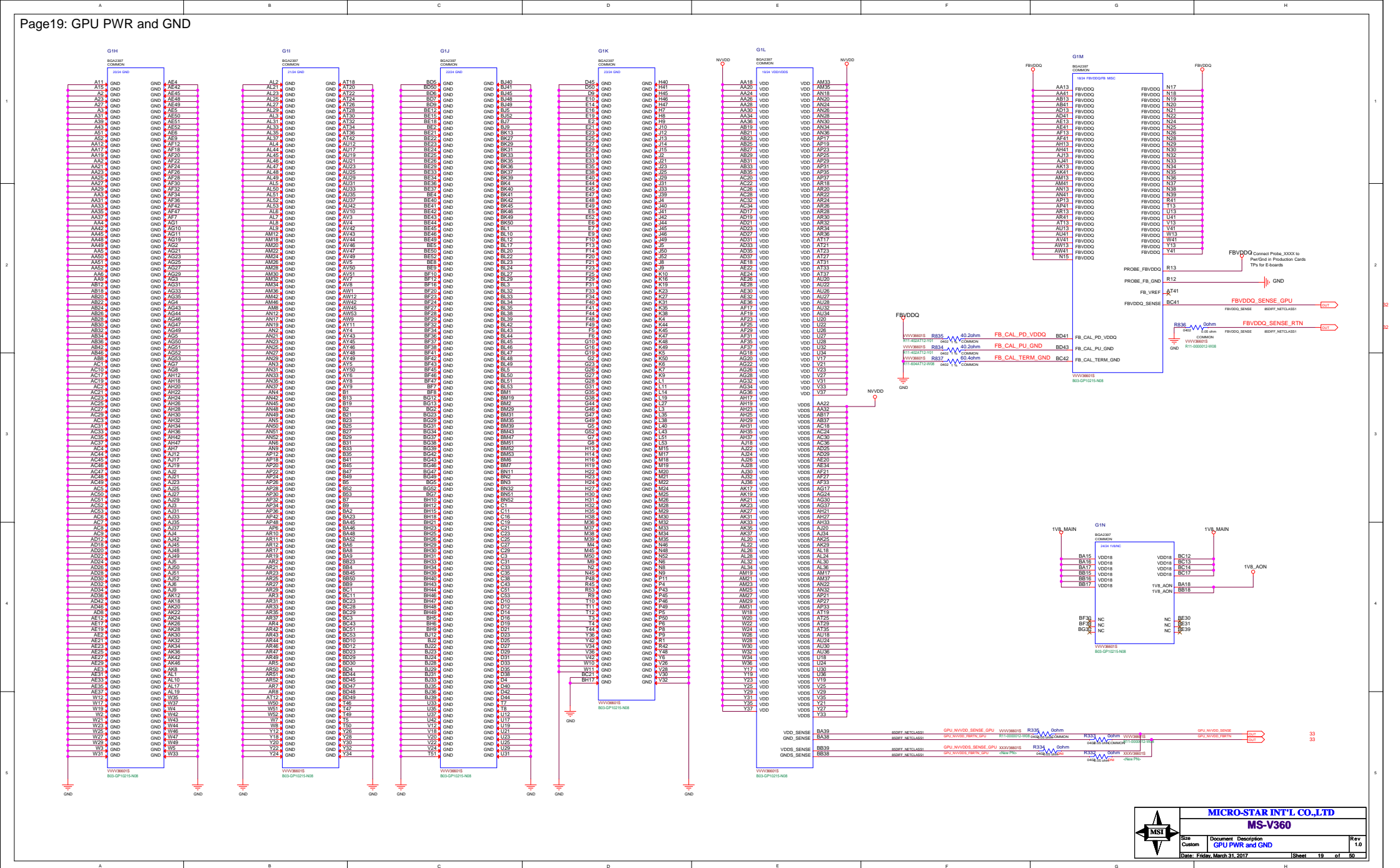


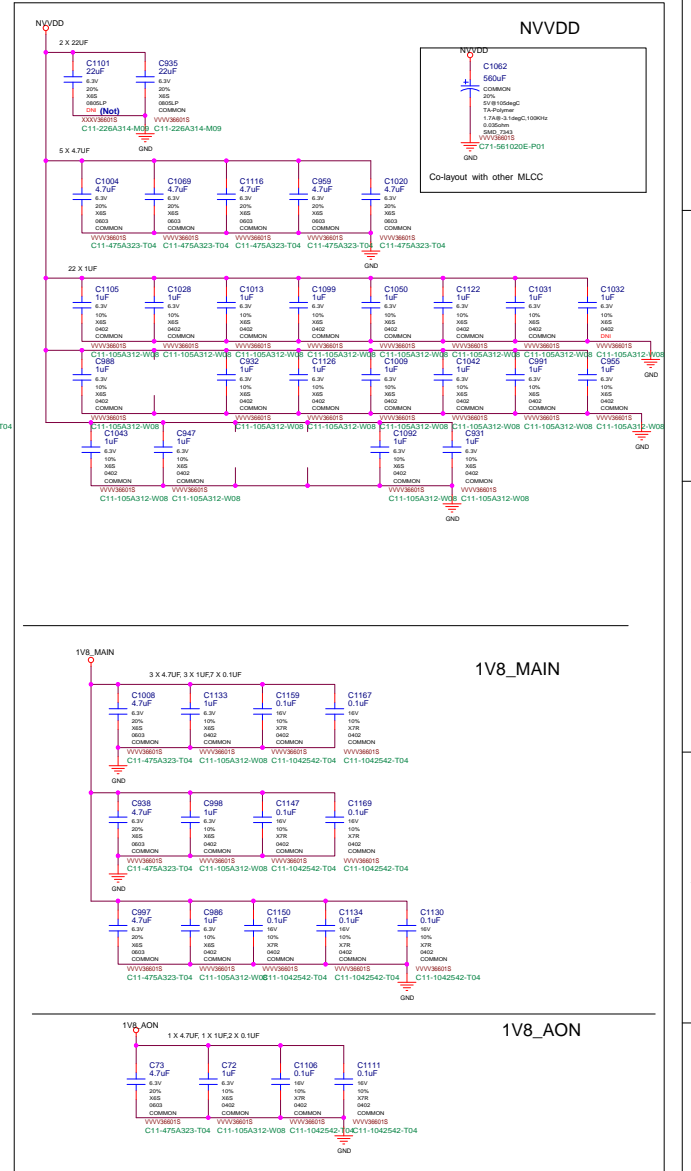
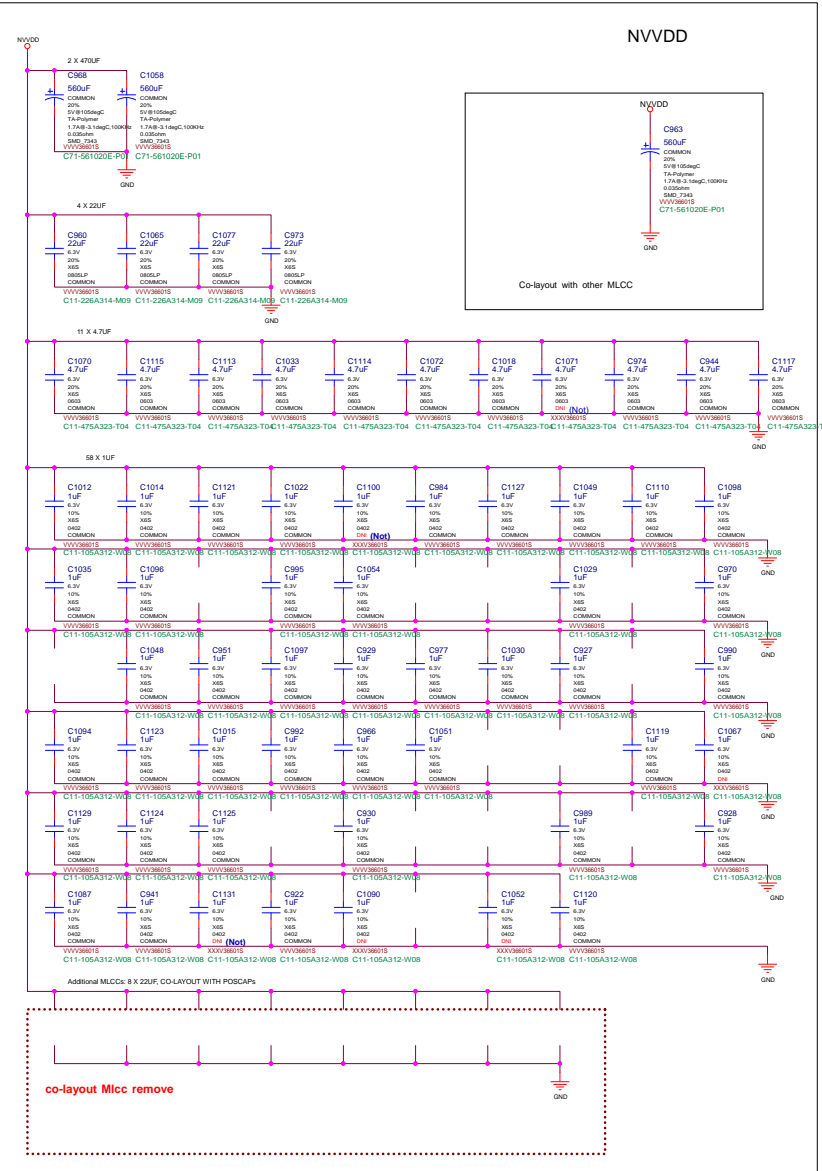
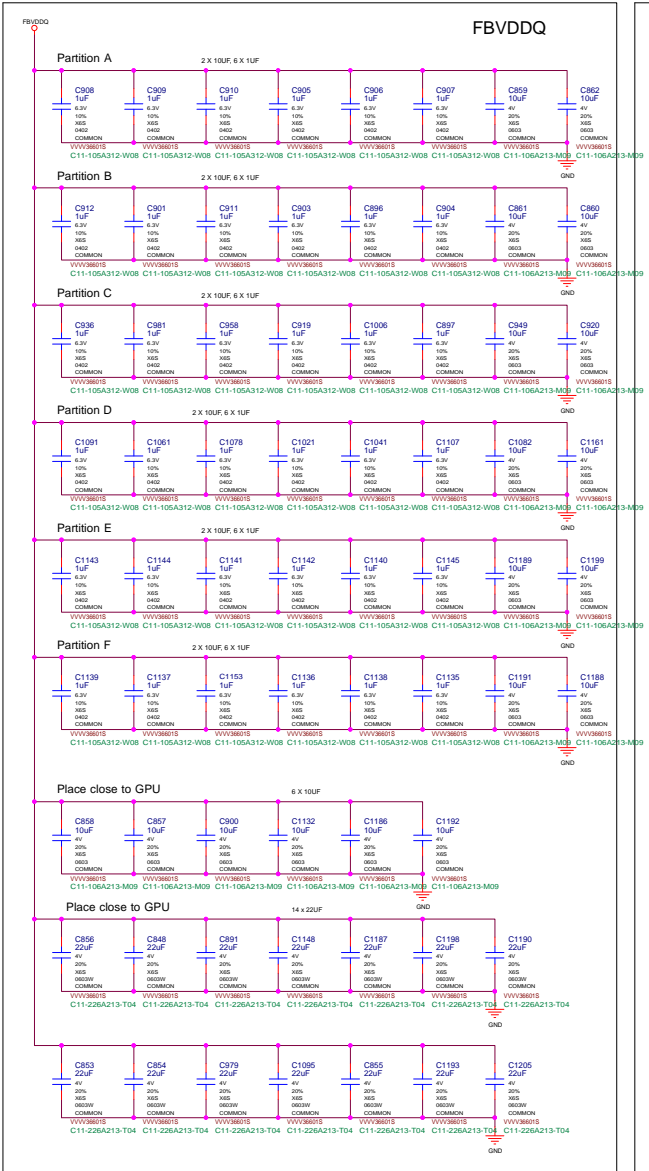
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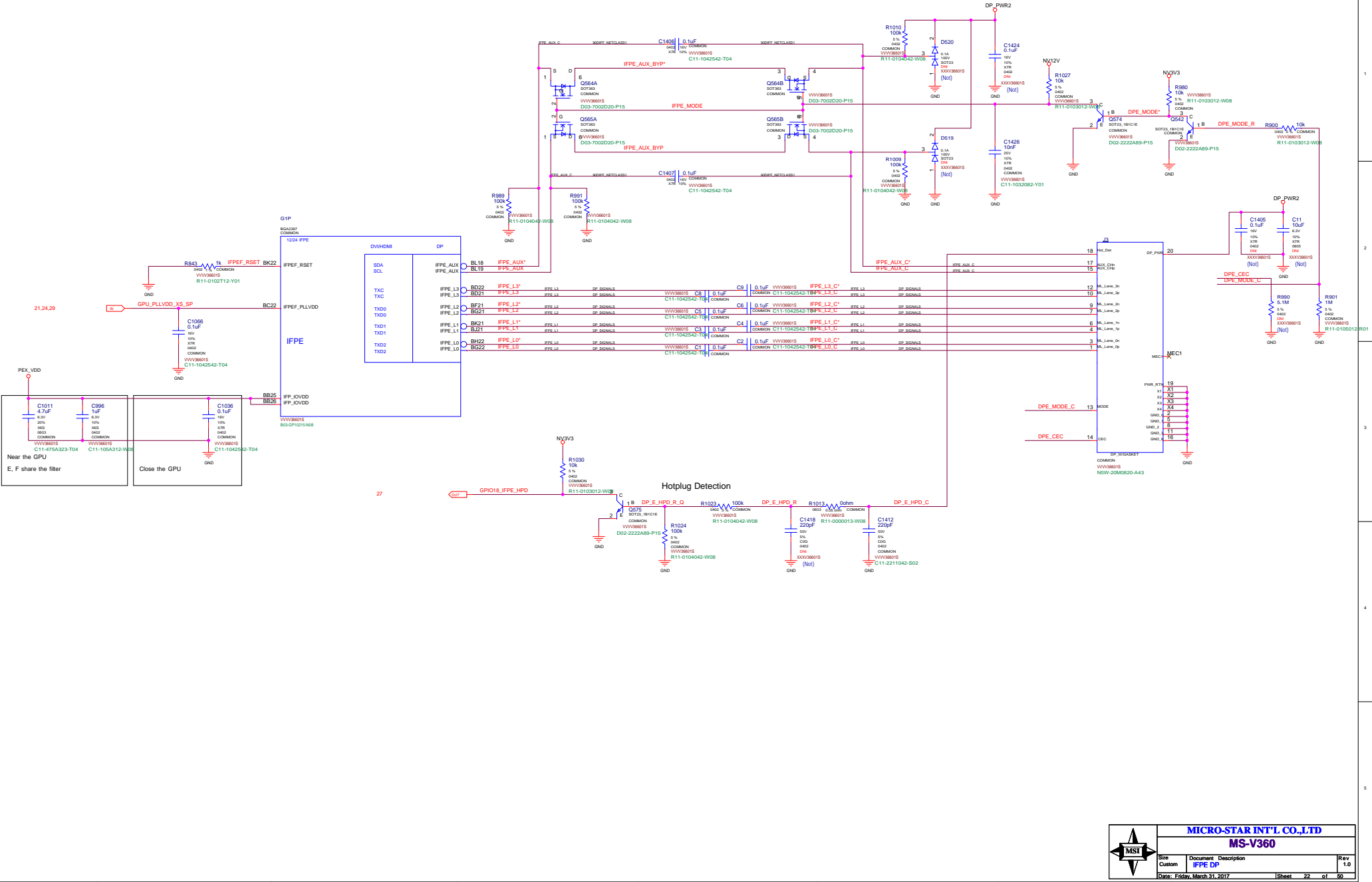
Size Custom	Document Description MEMORY: FBE Partition 63..32	Rev 1.0
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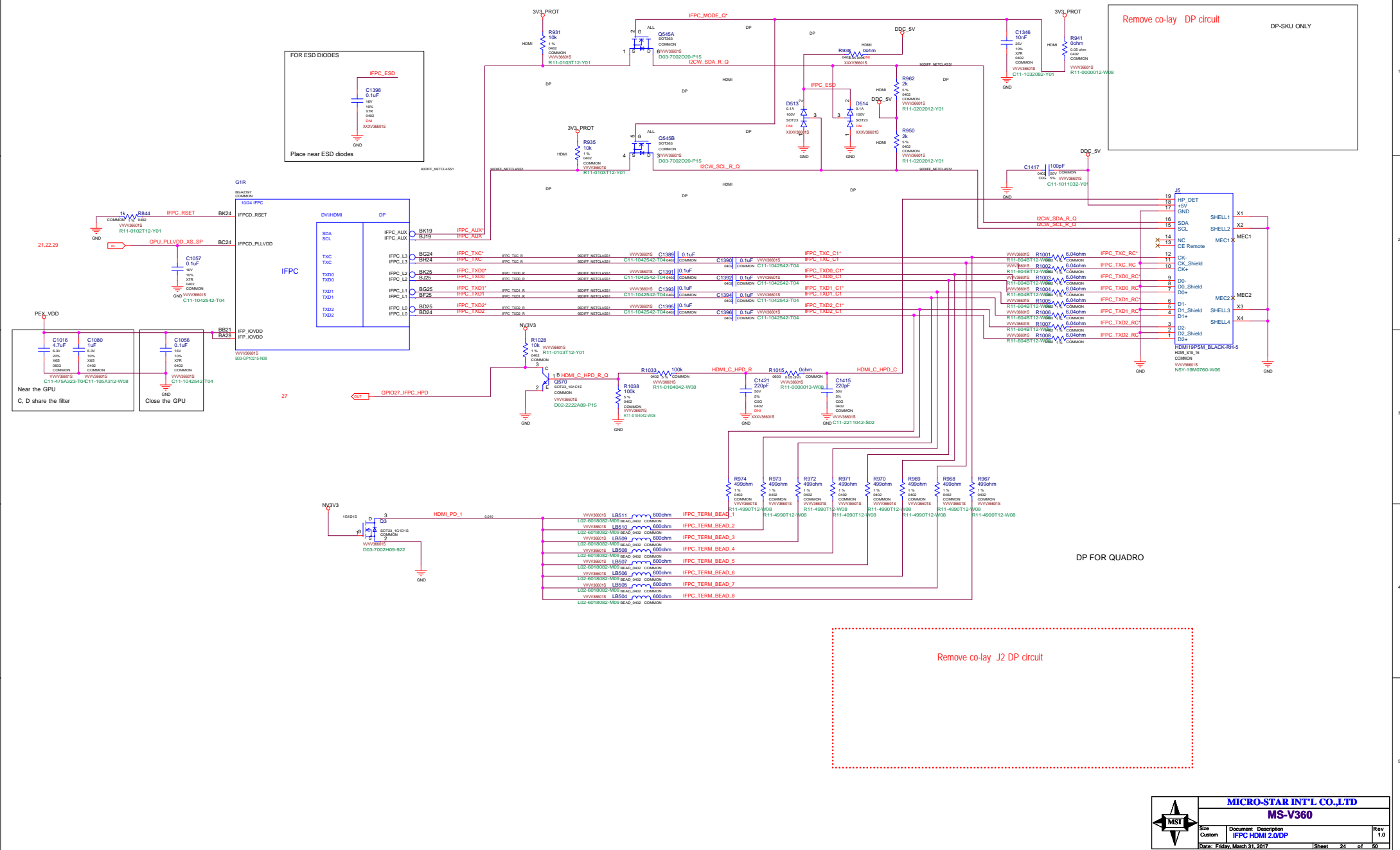


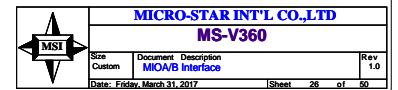
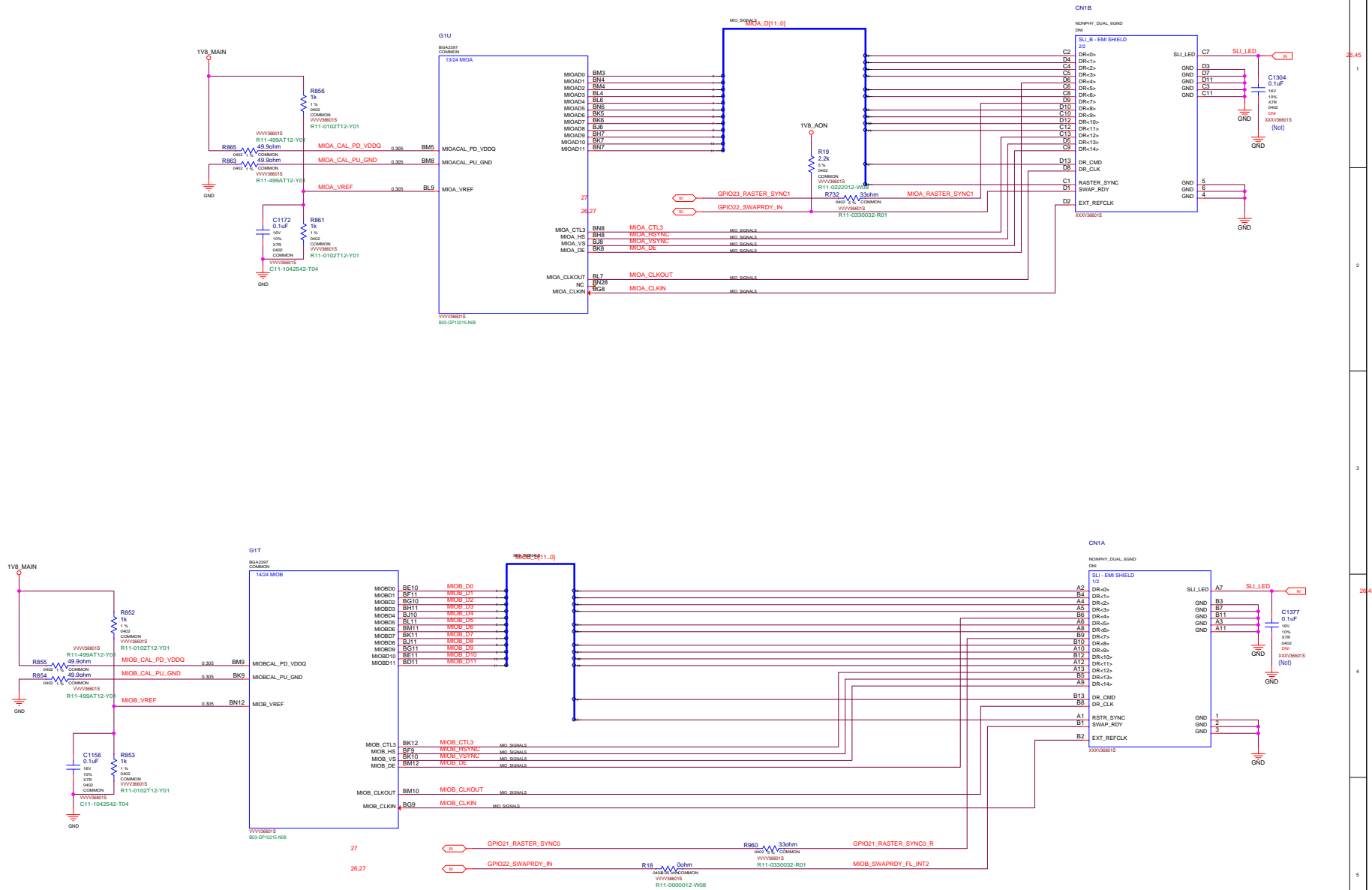












STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0] 1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT SOR0/1/2/3 ENABLE
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

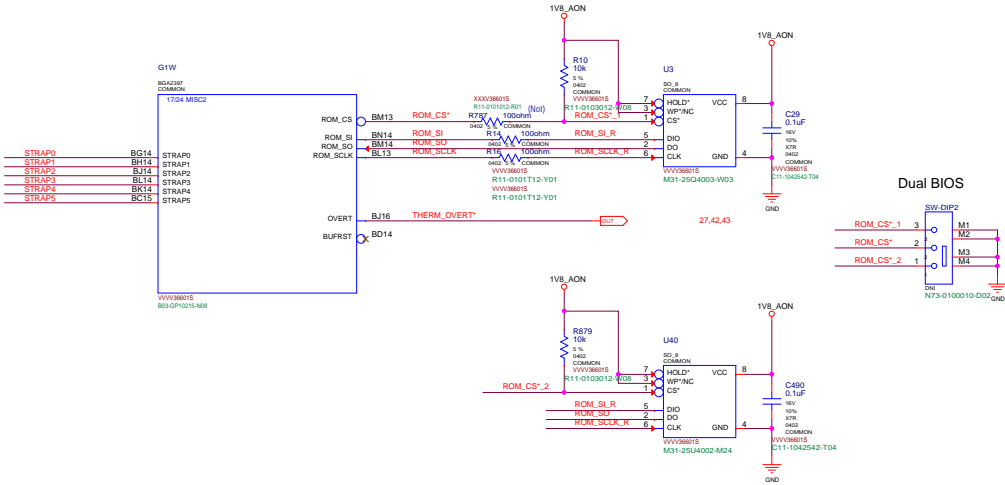
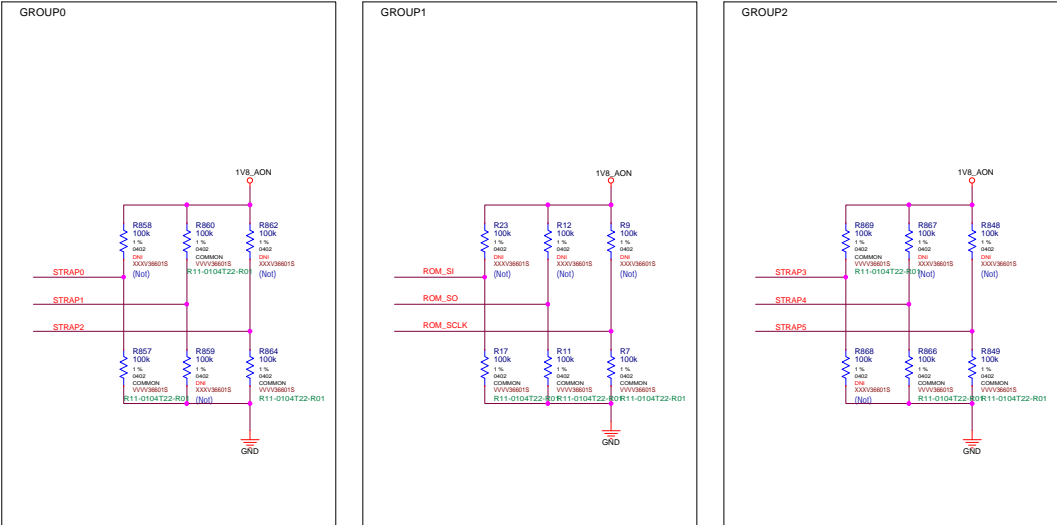
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

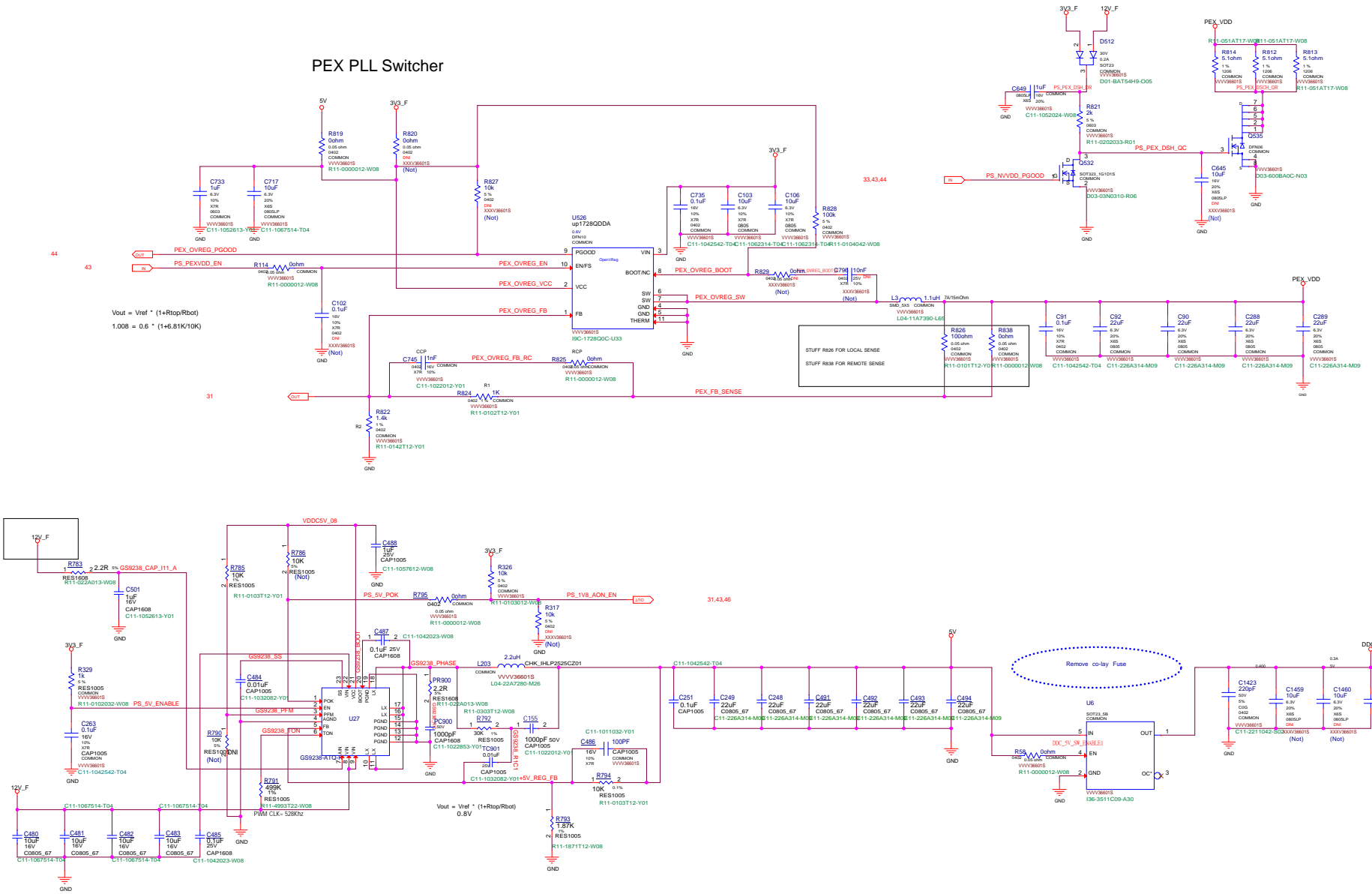
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

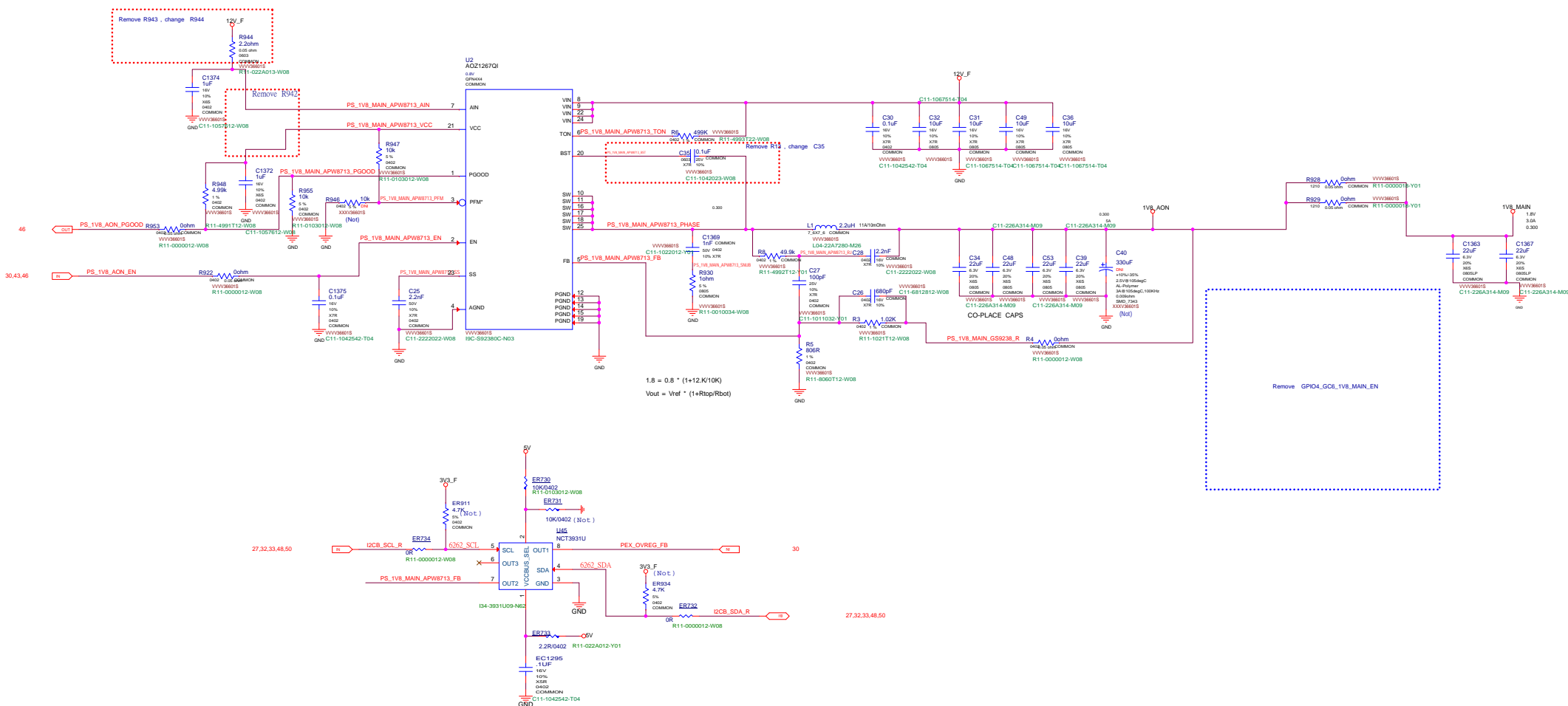


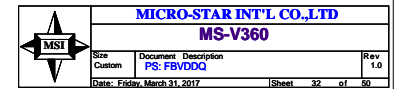
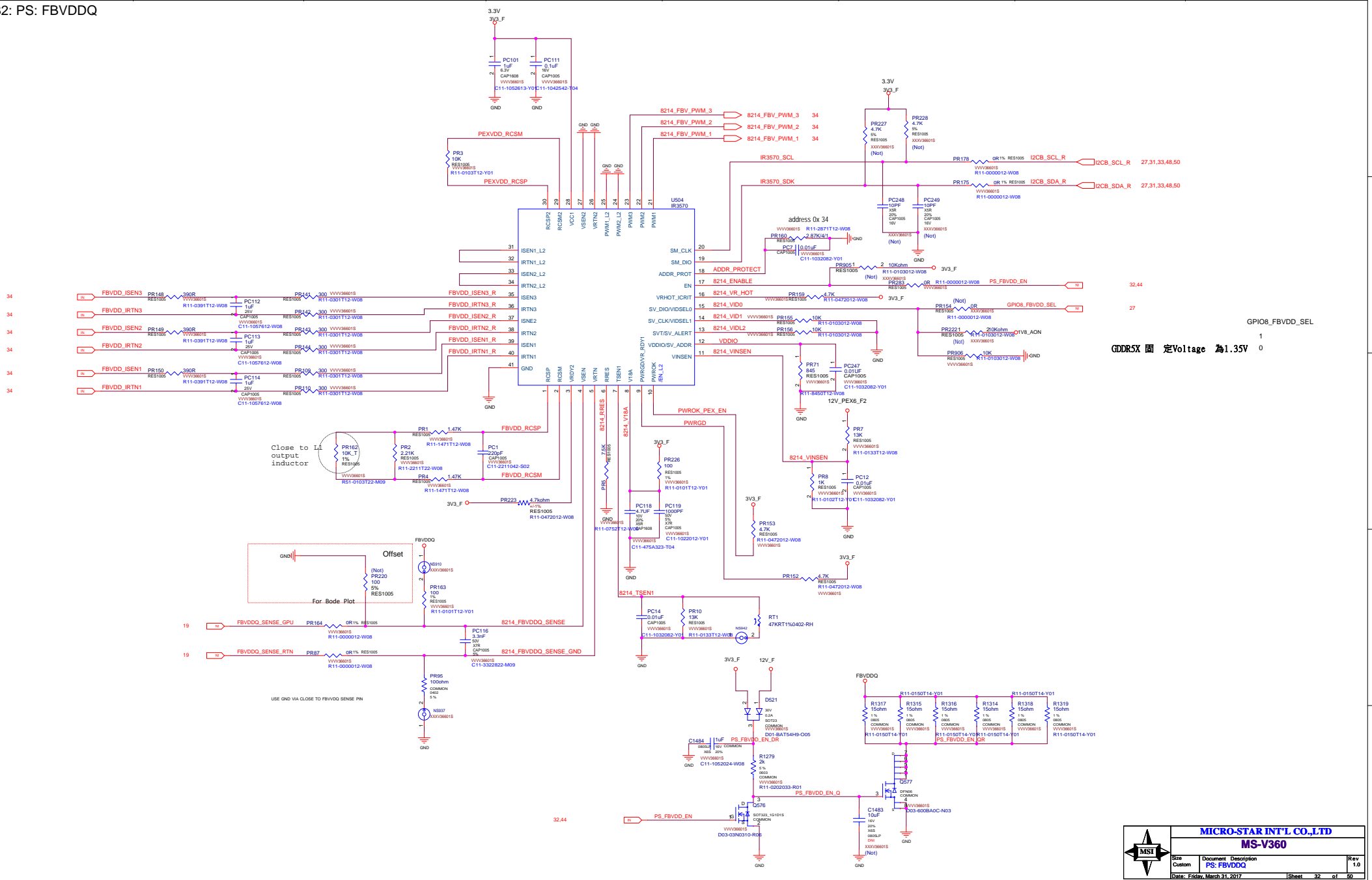
PEX PLL Switcher

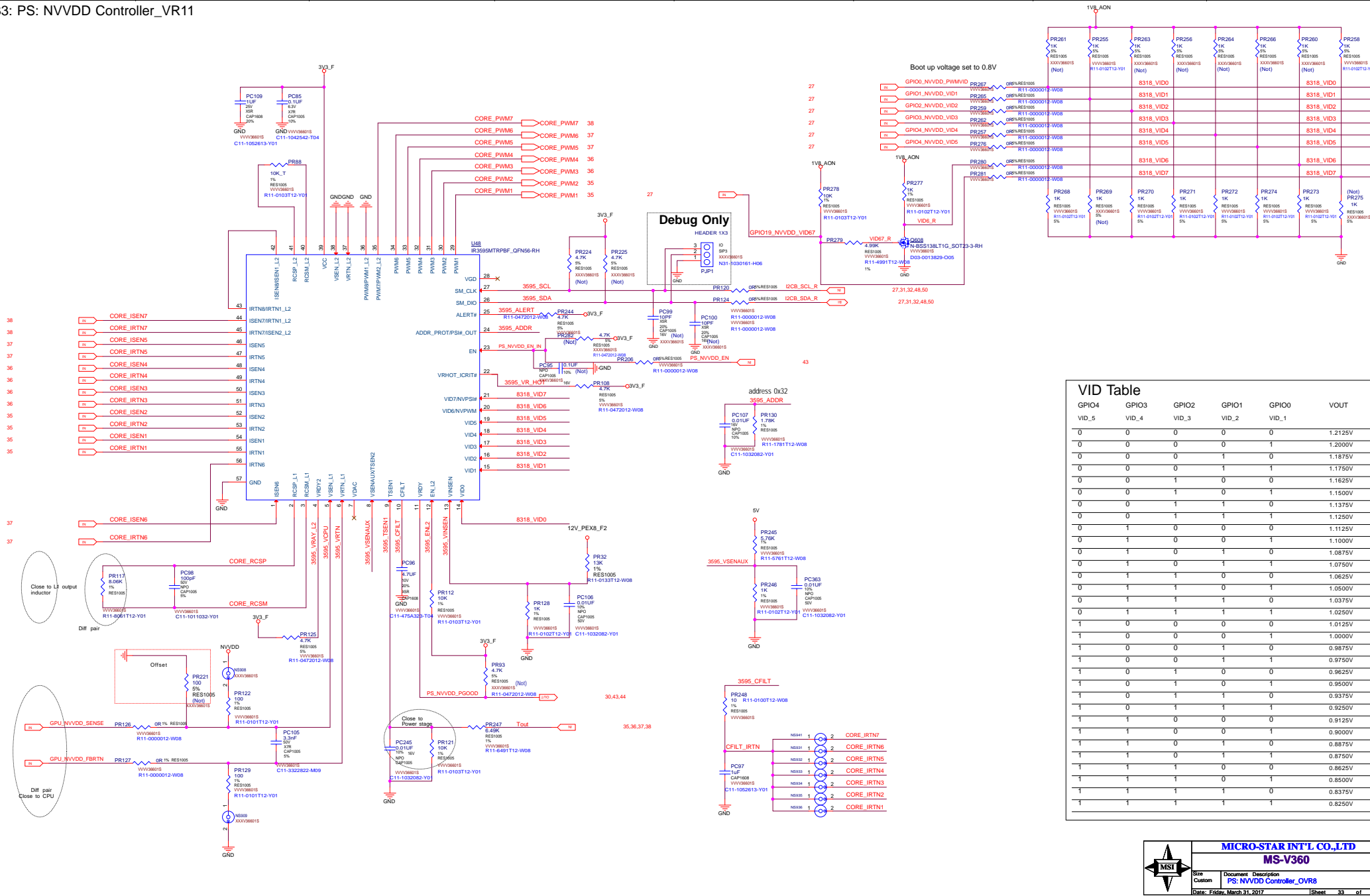


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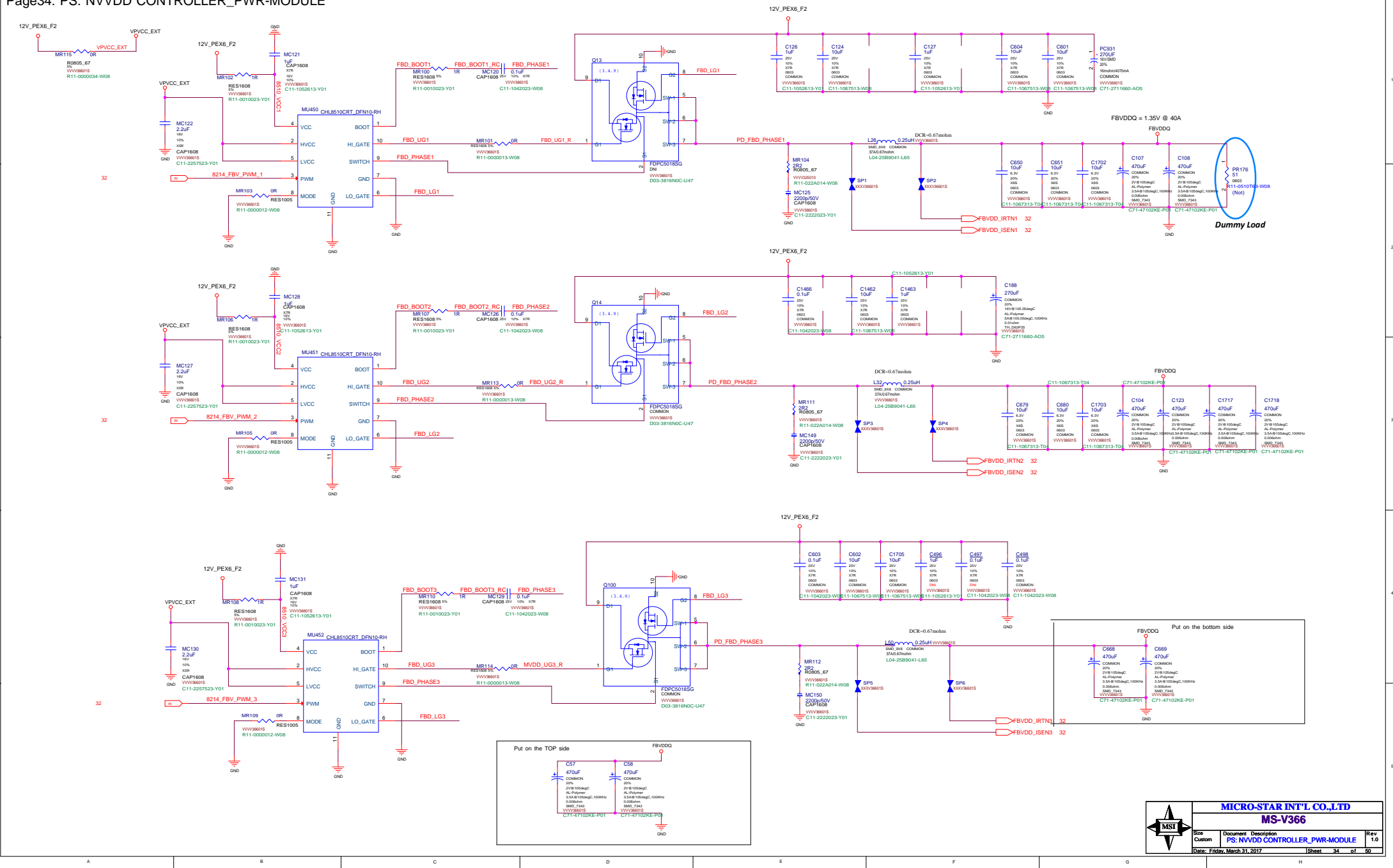
Size Custom	Document Description PS: 5V, PEX_VDD	Rev 1.0
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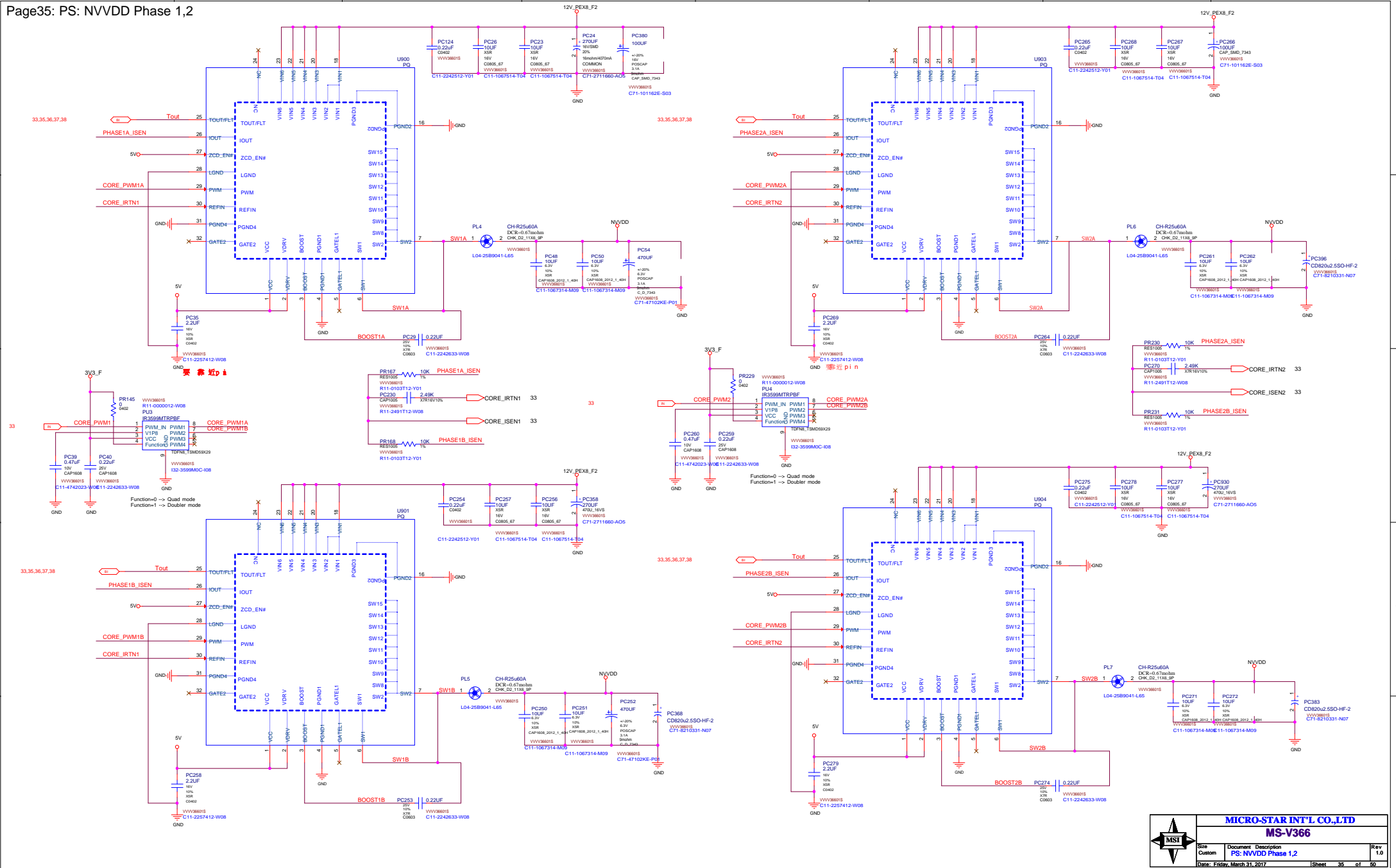


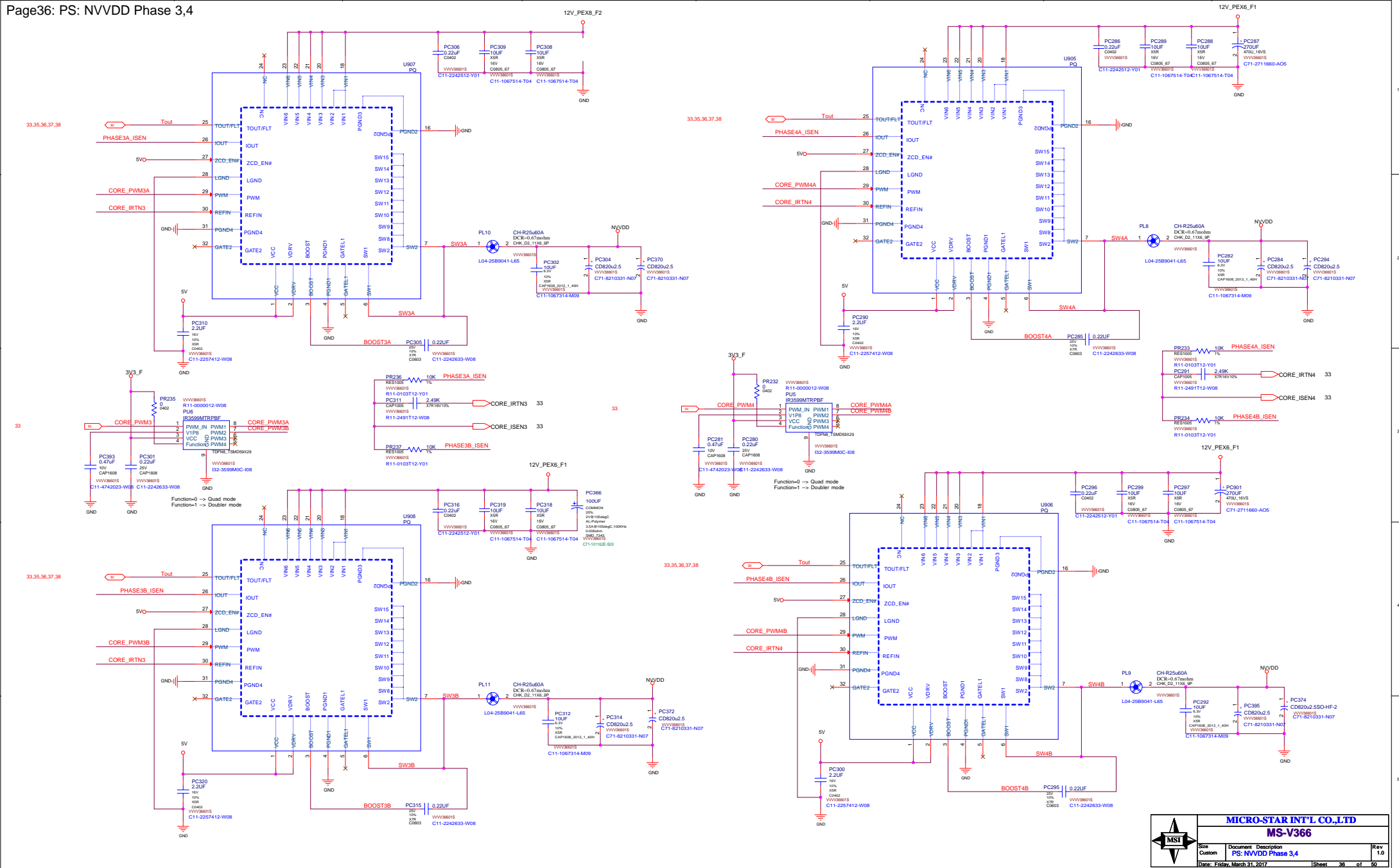


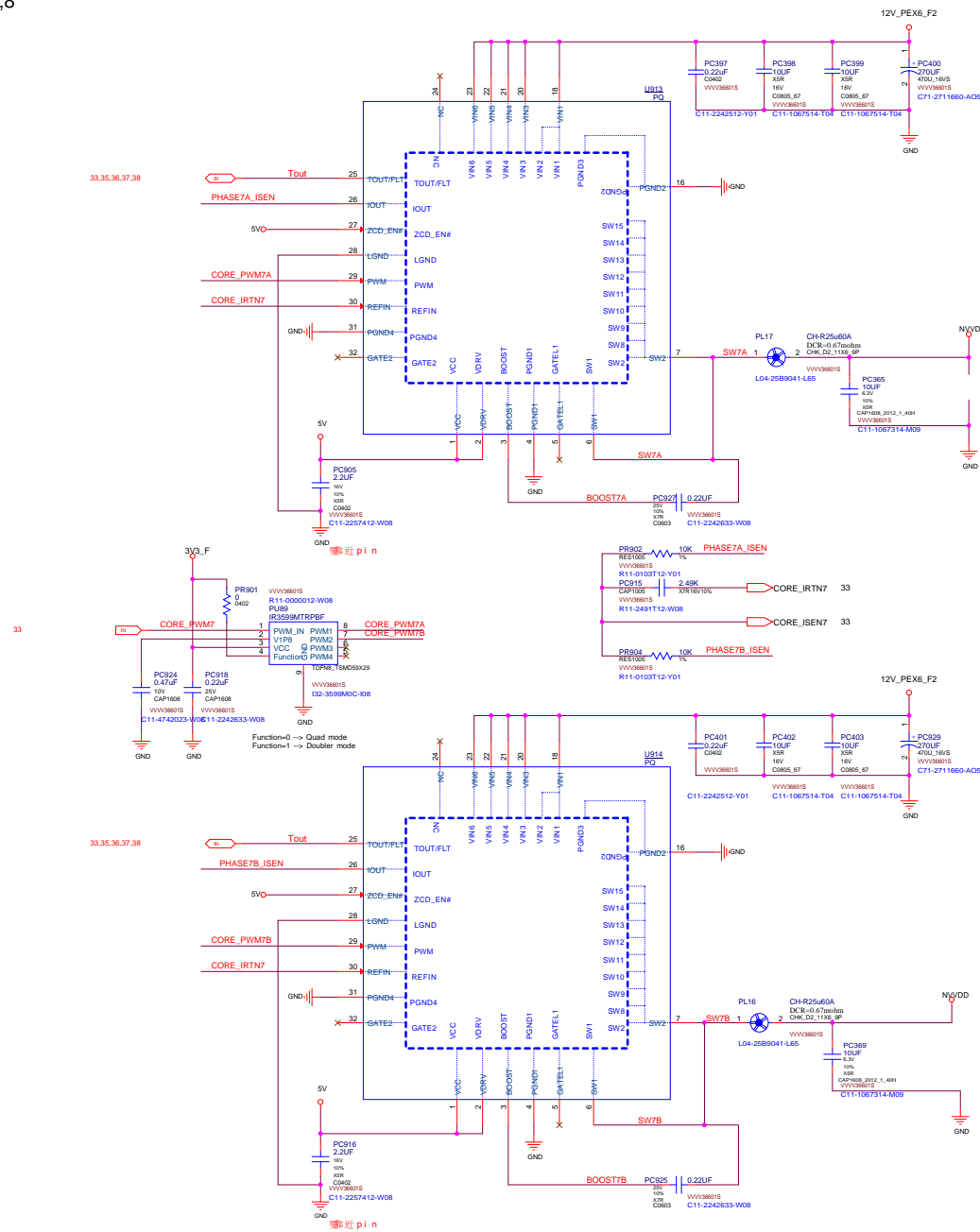


VID Table					
GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
1	0	0	0	0	1.0250V
1	0	0	0	1	1.0125V
1	0	0	1	0	1.0000V
1	0	0	1	1	0.9875V
1	0	1	0	0	0.9750V
1	0	1	0	1	0.9625V
1	0	1	1	0	0.9500V
1	0	1	1	1	0.9375V
1	1	0	0	0	0.9250V
1	1	0	0	1	0.9125V
1	1	0	1	0	0.9000V
1	1	0	1	1	0.8875V
1	1	1	0	0	0.8750V
1	1	1	0	1	0.8625V
1	1	1	1	0	0.8500V
1	1	1	1	1	0.8375V
1	1	1	1	1	0.8250V










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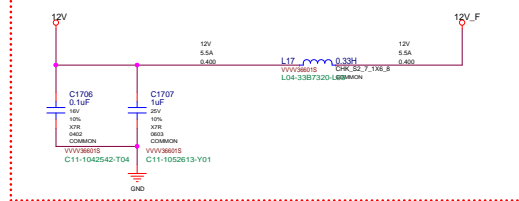
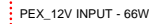
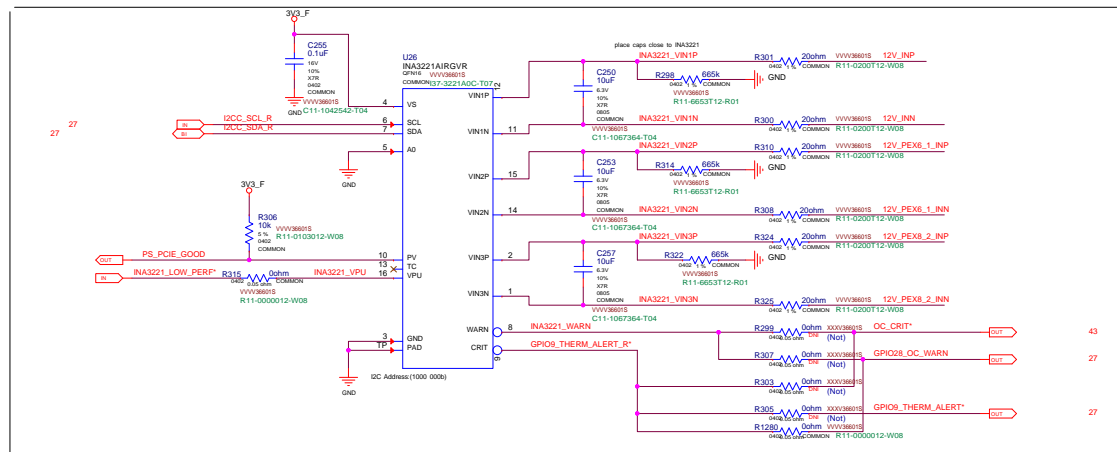
Size Custom	Document Description PS:NWDD Phase 6,7	Rev 1.0
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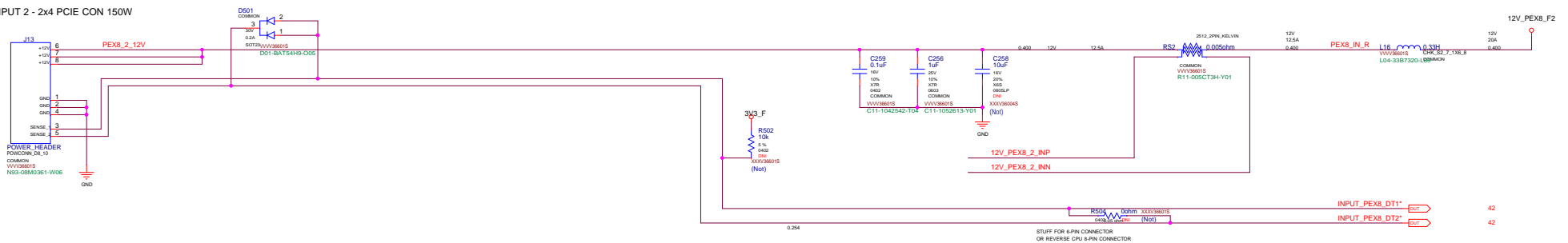
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MS-V366			
Size	Document	Description	Rev
Custom	Dynamic Power Balance Phases		1.0
Date: Wednesday, March 29, 2017		Sheet	39 of 50



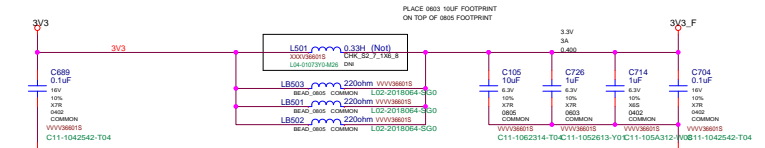
MICRO-STAR INT'L CO.,LTD			
MS-V366			
Size	Document Description		Rev
Custom	PS: Dynamic Power Balance Logic		1.0
Date: Wednesday, March 29, 2017		Sheet	40 of 50



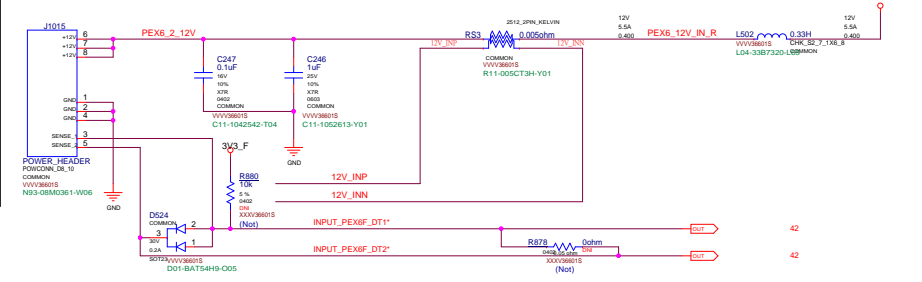
PEX8 INPUT 2 - 2x4 PCIE CON 150W



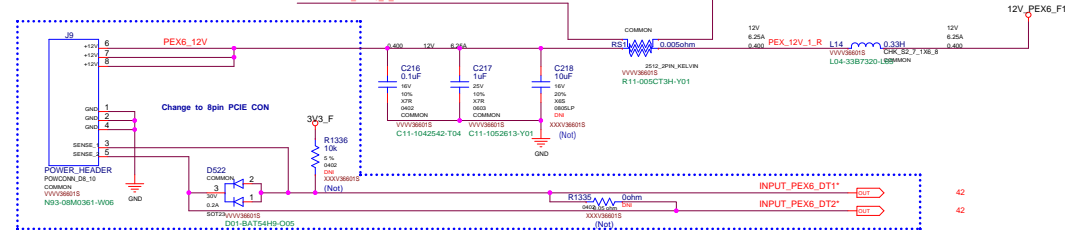
PEX 3V3 INPUT - 10W



PEX_6 INPUT1 - 2x4 PCIE CON 150W



PEX_6 INPUT1 - 2x4 PCIE CON 150W



STUFF FOR 6-PIN CONNECTOR
OR REVERSE CPU 8-PIN CONNECTOR

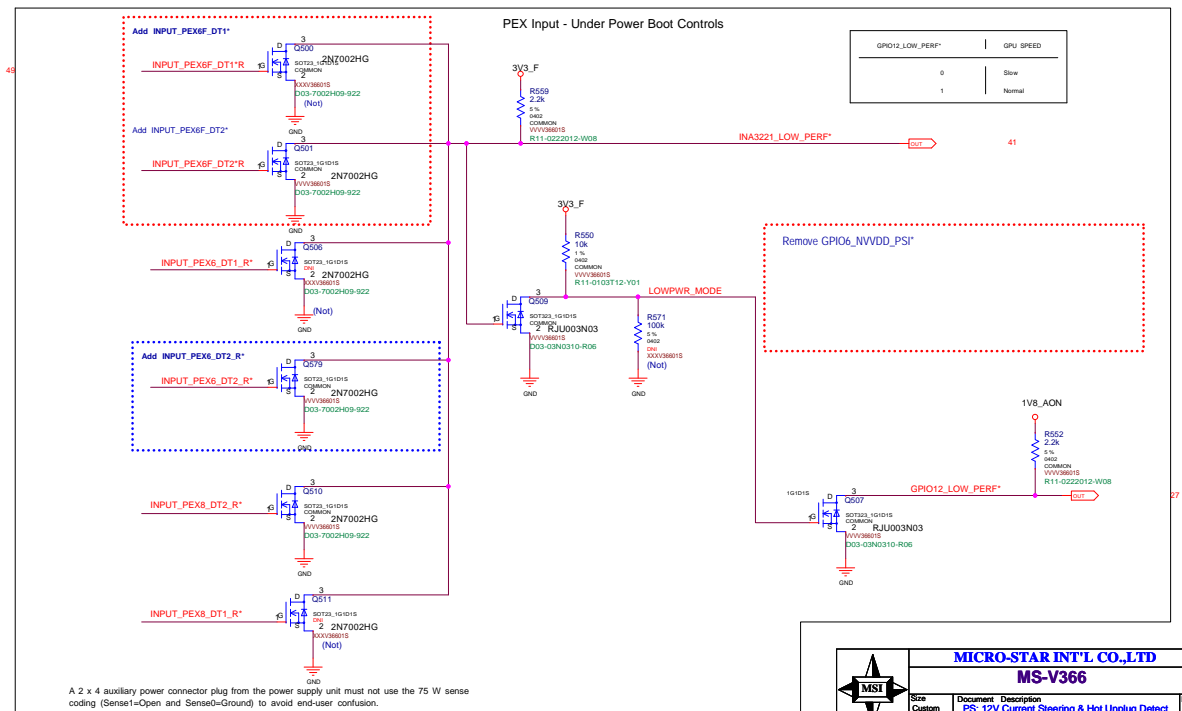
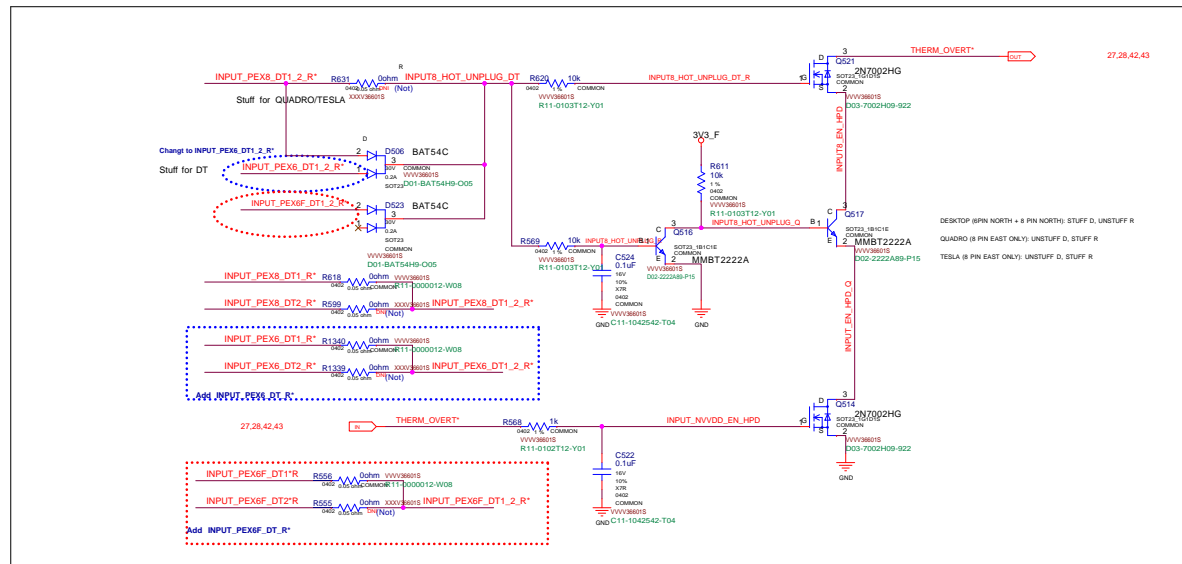
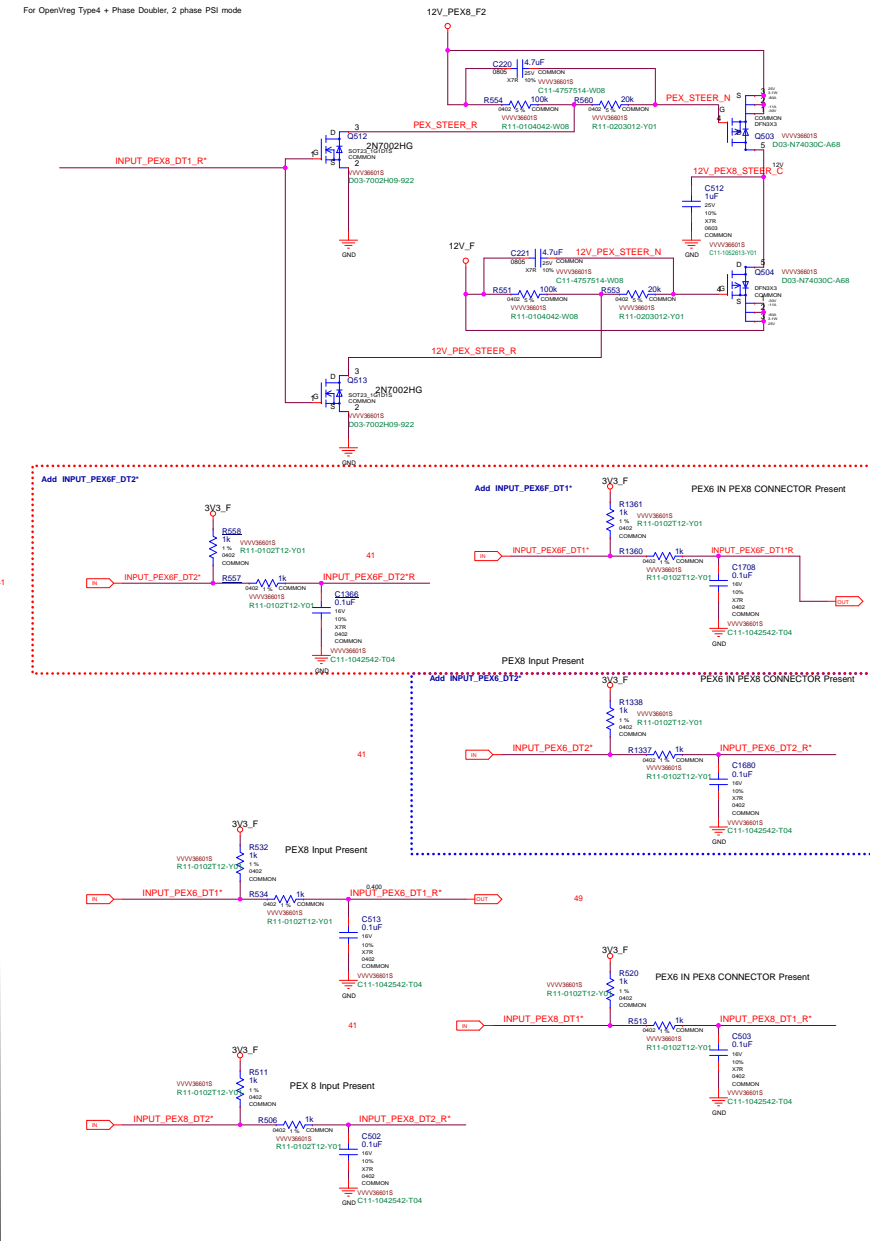


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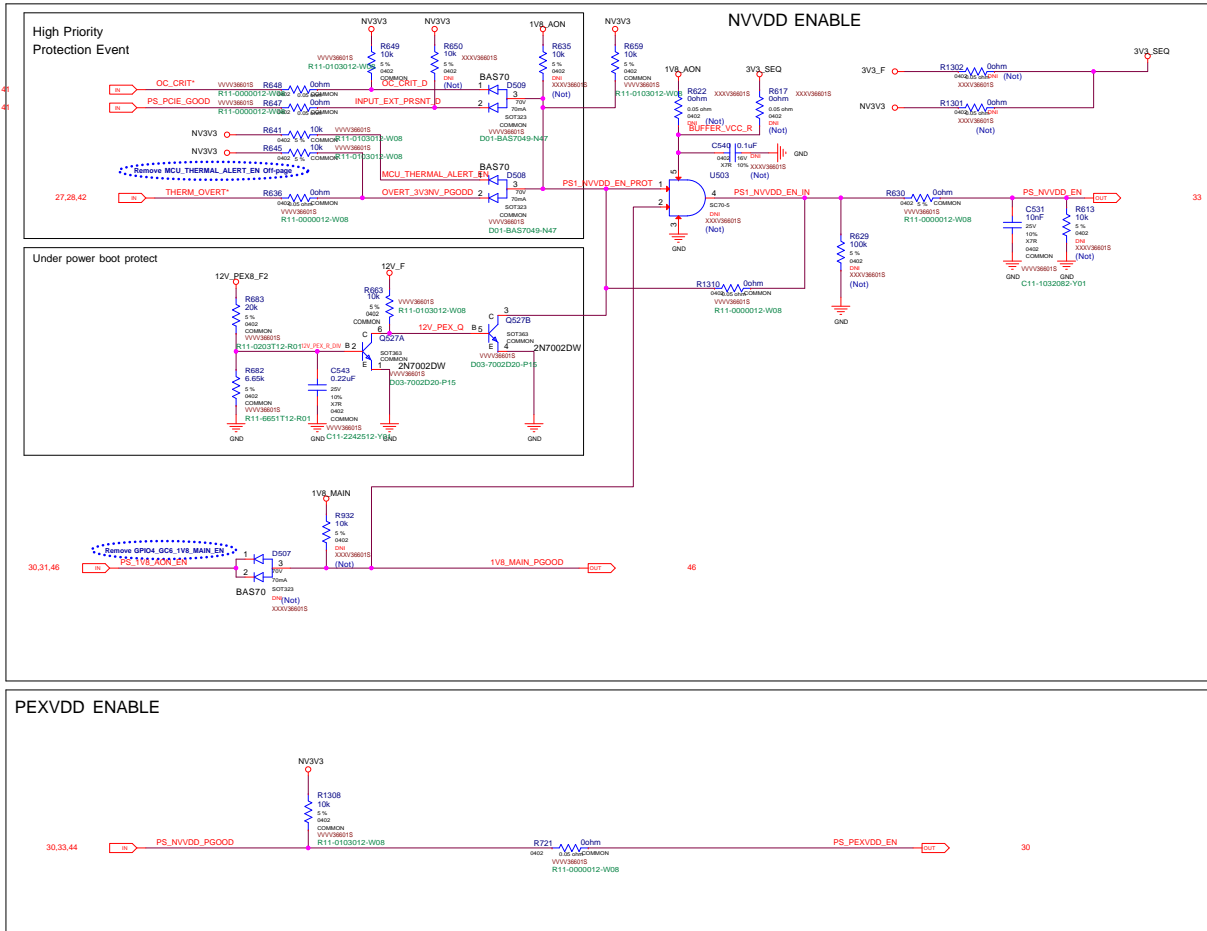
Size Custom	Document Description PS: Inputs, Filtering, and Monitoring	Rev 1.0
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GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.



Remove GPU_EVENT*

The diagram shows the PS_FBVDD_EN signal path. The signal is generated by the PS_NVDD_PGOOD pin (pin 18) through a network of inverters and resistors. The signal path includes a 74VHC125 buffer (U10) and a 74VHC125 buffer (U11). The signal is then connected to the PS_FBVDD_EN pin (pin 18) through a 10k resistor (R1281). The signal is also connected to the PS_FBVDD_EN pin (pin 18) through a 10k resistor (R1281). The signal is also connected to the PS_FBVDD_EN pin (pin 18) through a 10k resistor (R1281).

Accept 3V3 Logic

3V3_F

10k

5%

0.1uF

3V3_AON

74VHC123

100k

5%

0.1uF

3V3_AON

100k

5%

0.1uF

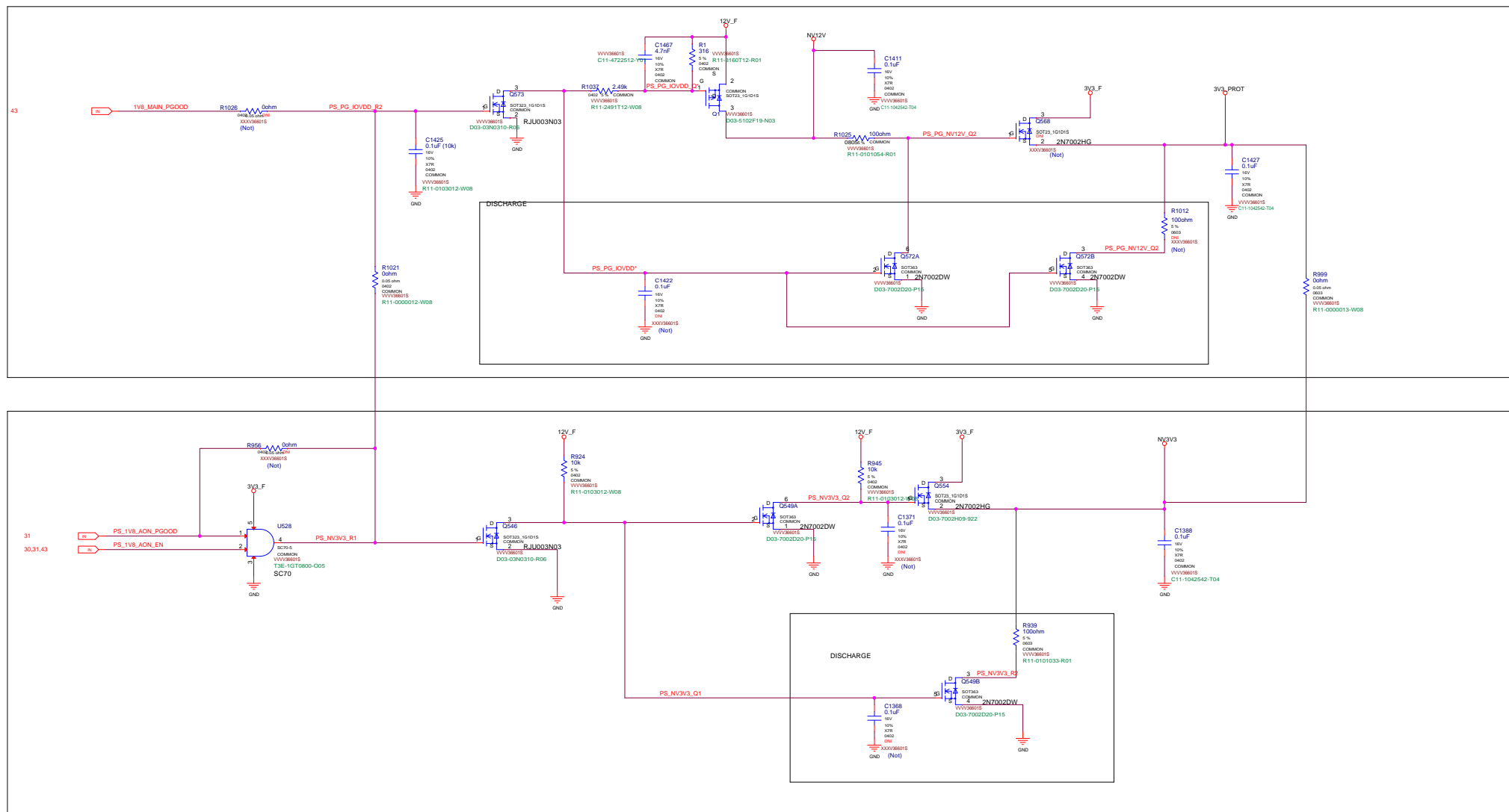
3V3_AON

PEX_RST*

3V3_AON

Remove LED HEADER(GEFORCE ONLY)



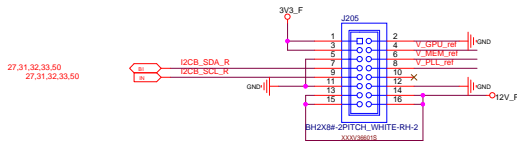
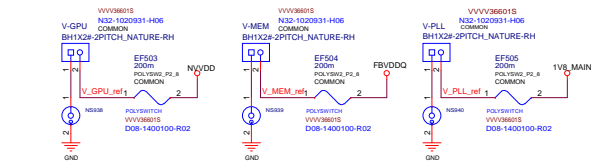


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MS-V366

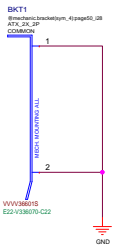
Size Custom	Document Description NV3V3, NV12V	Re 1
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Please refer datasheet
TCRIT_SET Table
If floating,shutdown temp. set to 65°C

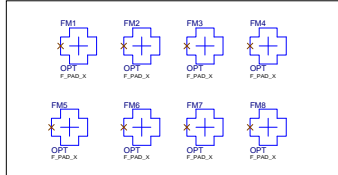
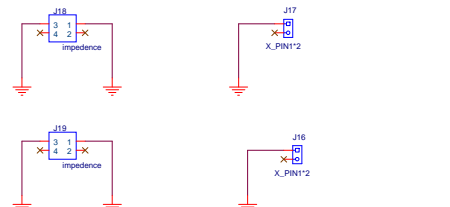
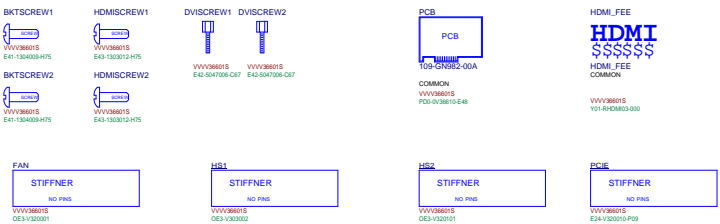




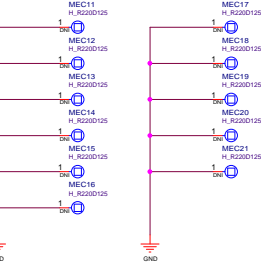
Brackets:



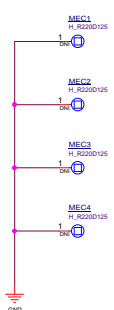
Screw

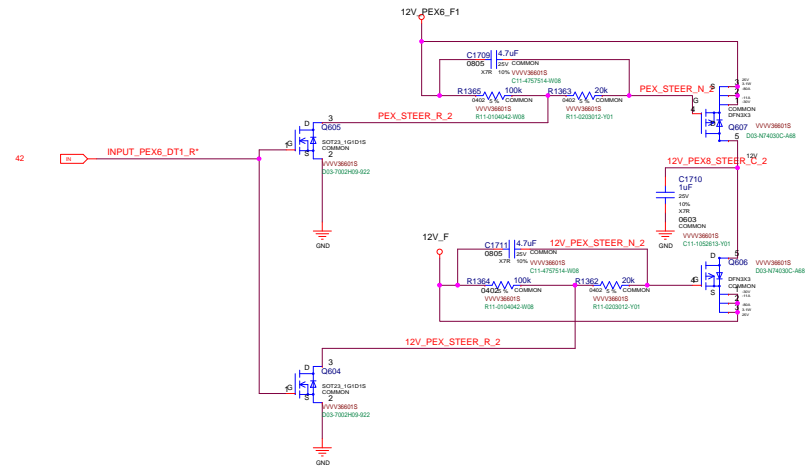
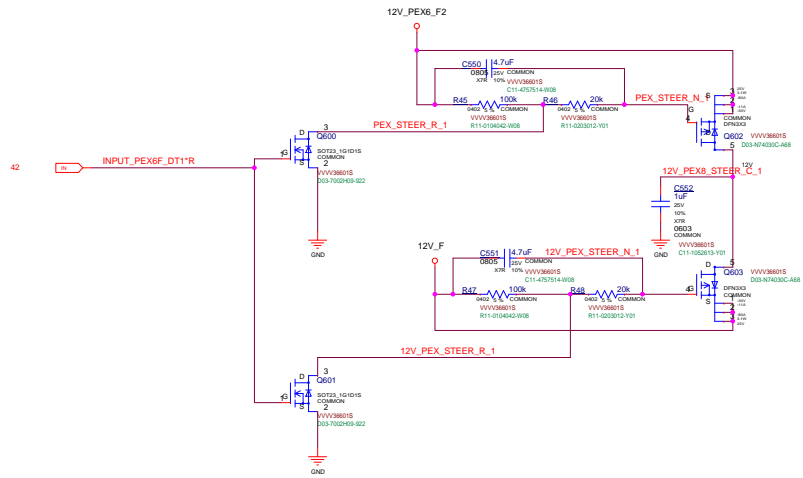


Mechanical Holes Symbol



GPU HOLES SYMBOL





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