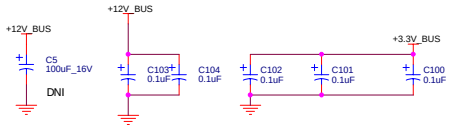
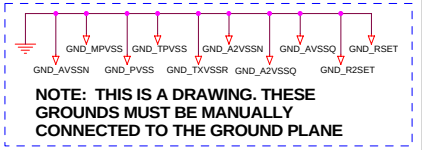
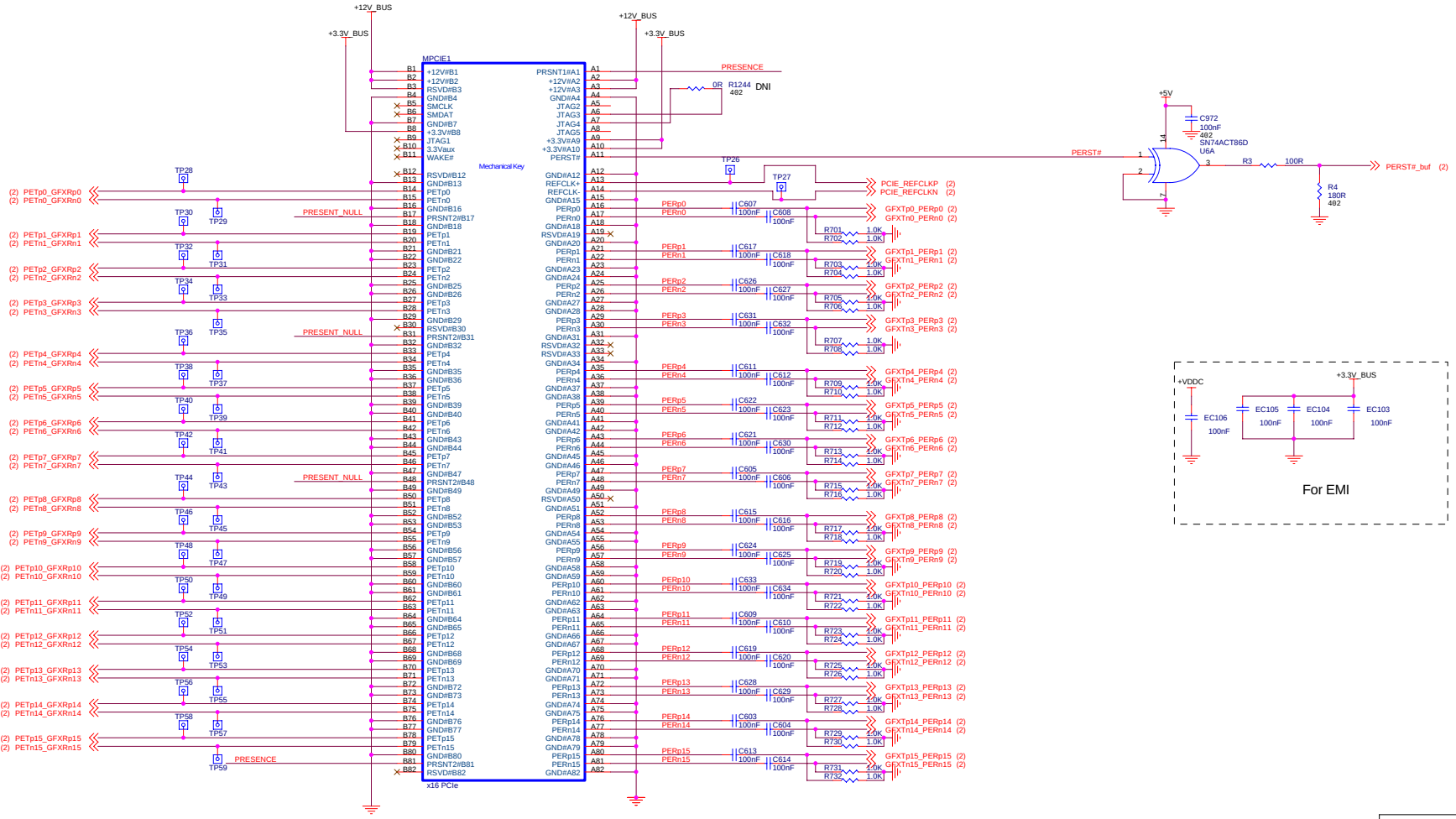
PCI-EXPRESS EDGE CONNECTOR







SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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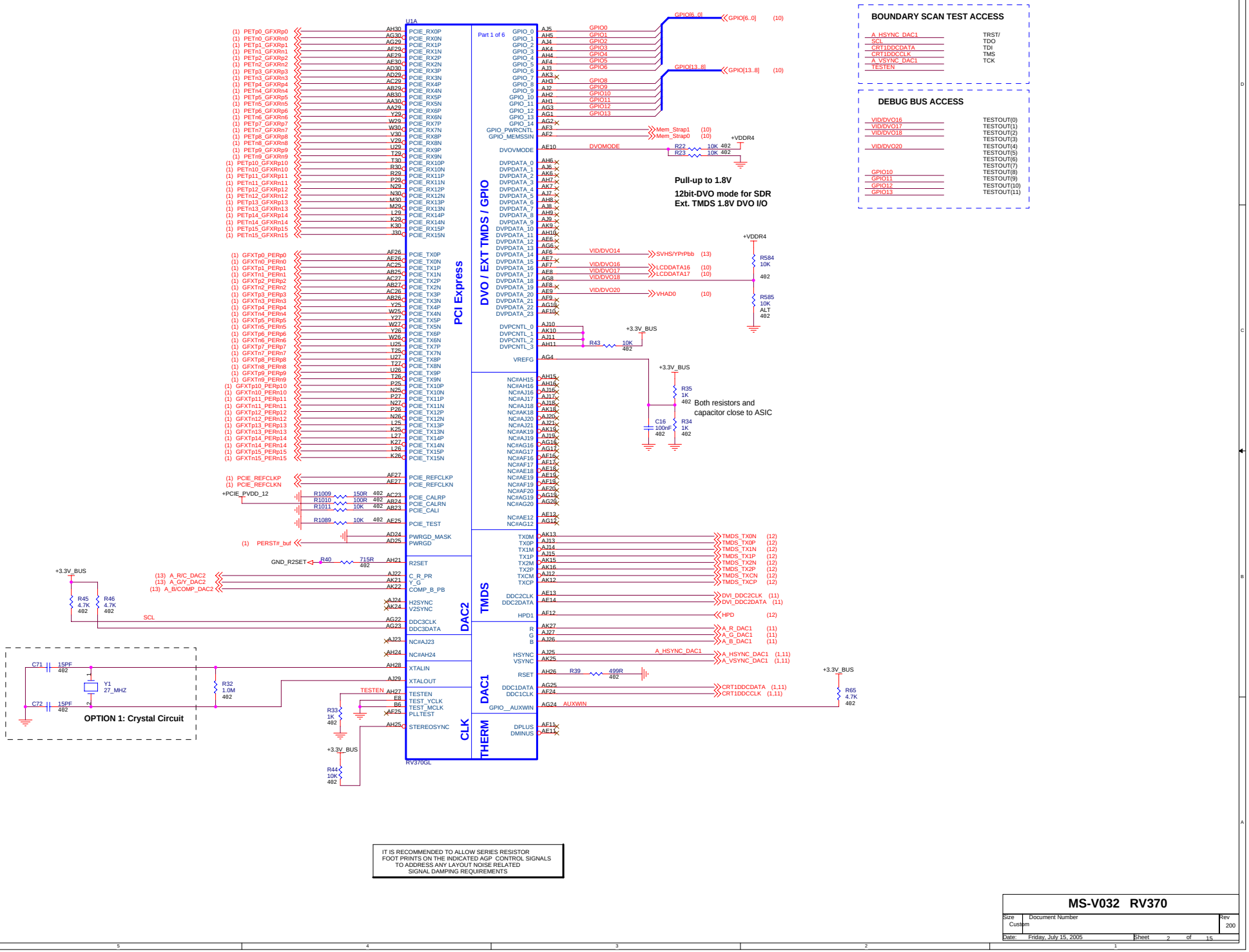

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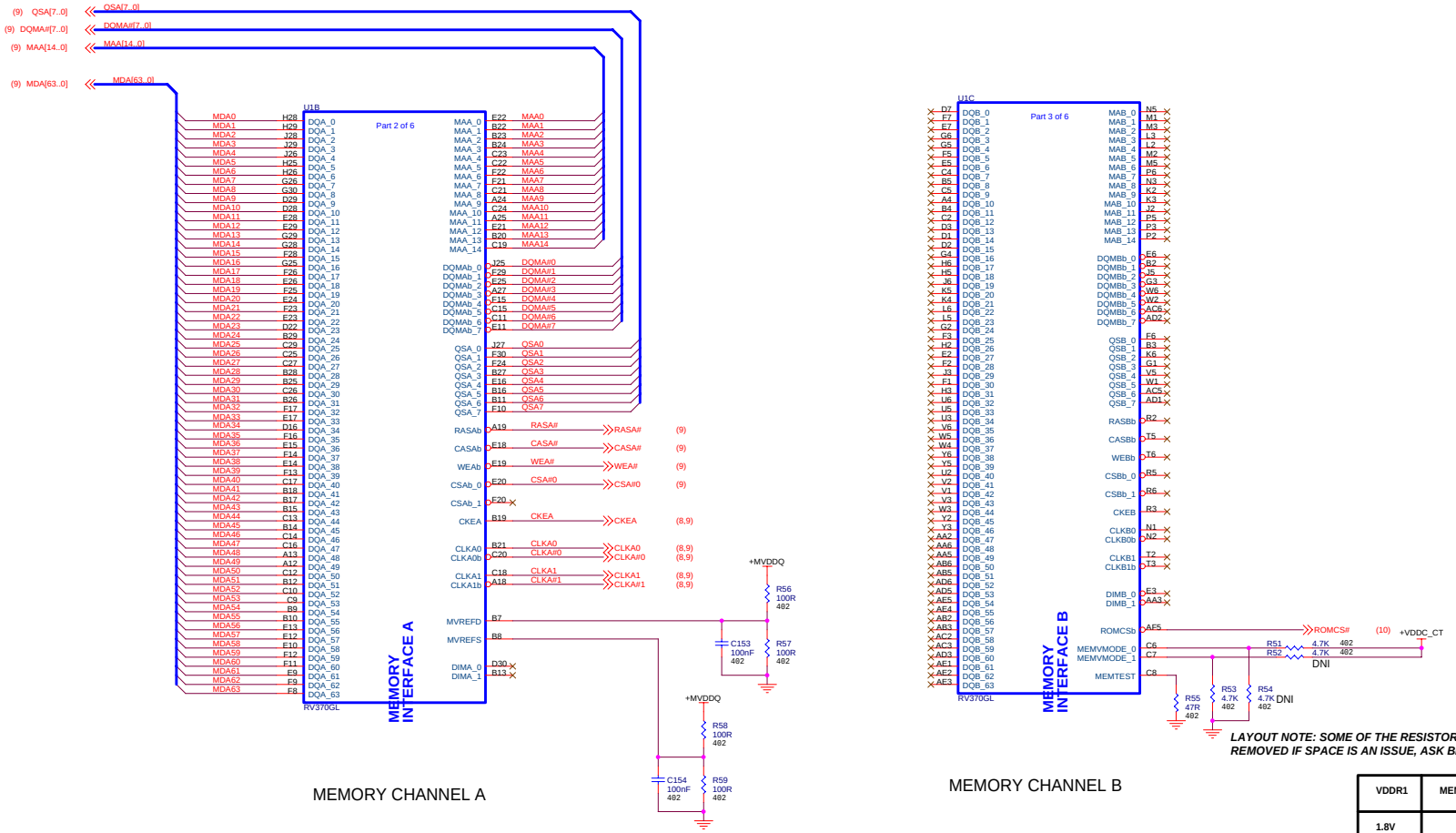

MEMORY CHANNEL A

MEMORY CHANNEL B

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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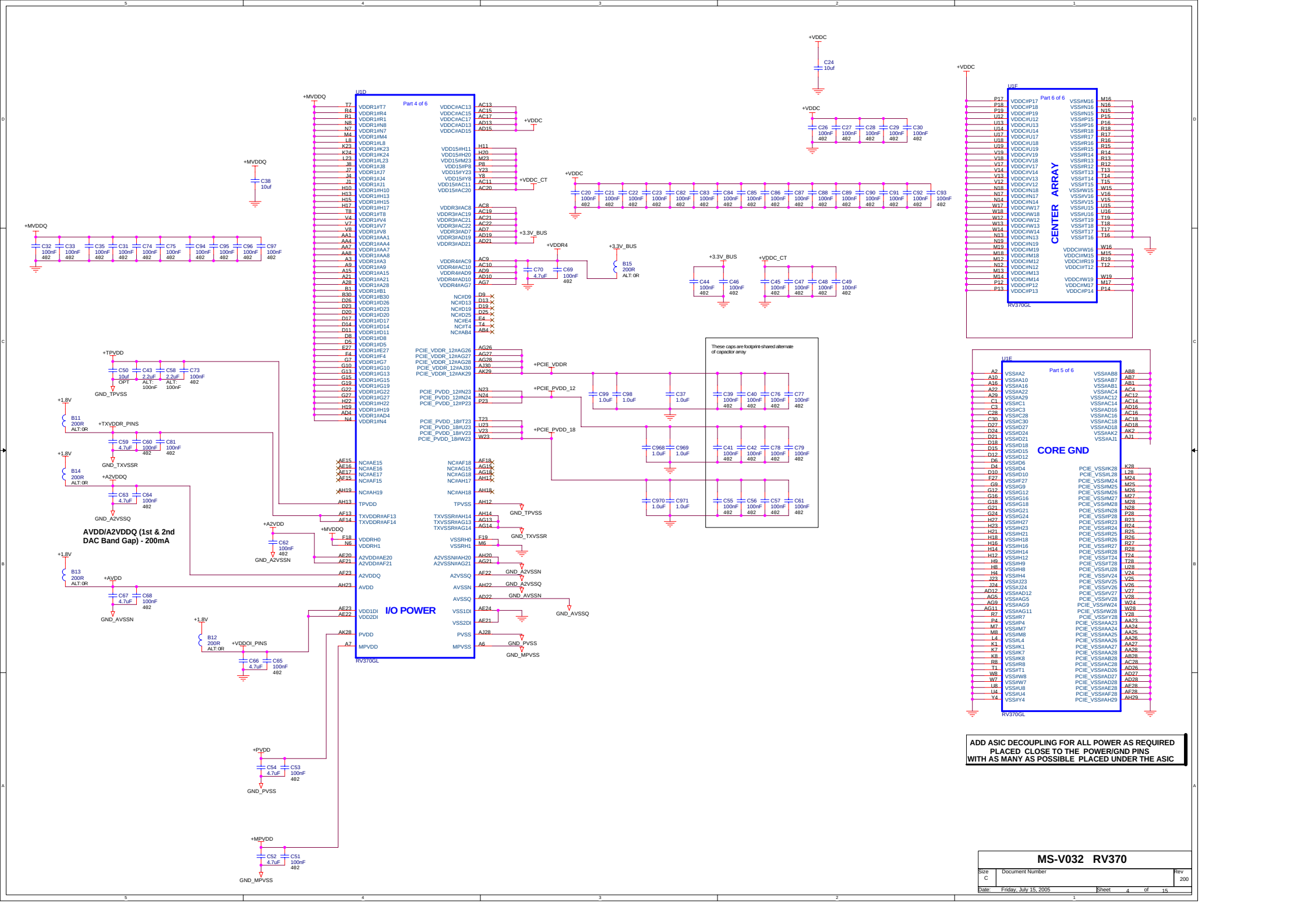
U1D
Part 4 of 6
RV370GL
I/O POWER
U1E
Part 5 of 6
CORE GND
U1F
Part 6 of 6
CENTER ARRAY
These caps are footprint-shared alternate of capacitor array
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
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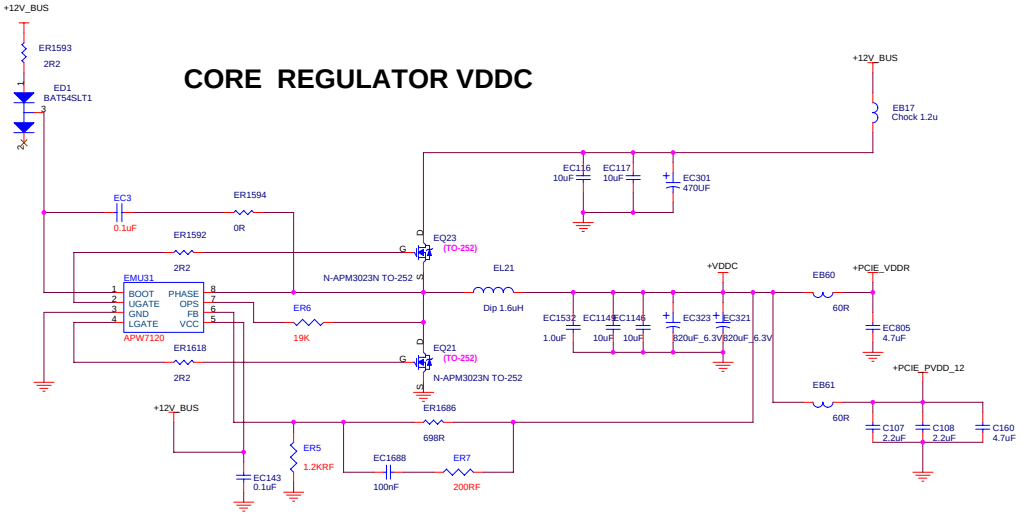
CORE REGULATOR VDDC



+VDDC=1.26V

APW7120 Application Circuit

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+MVDDQ +MVDDC

APW7120 Application Circuit

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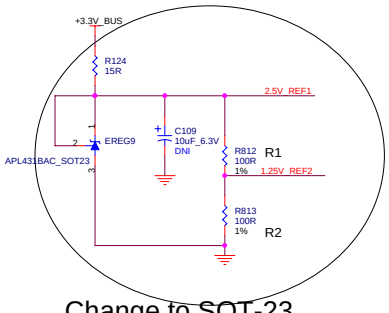
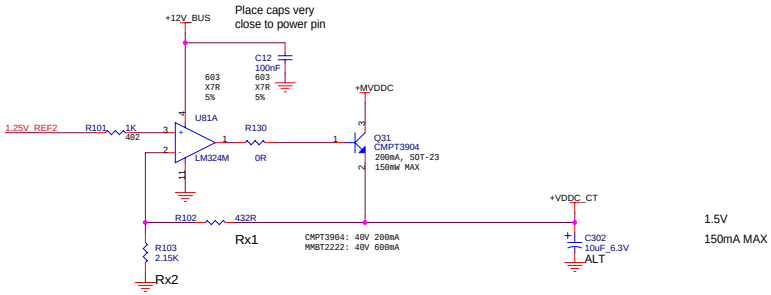
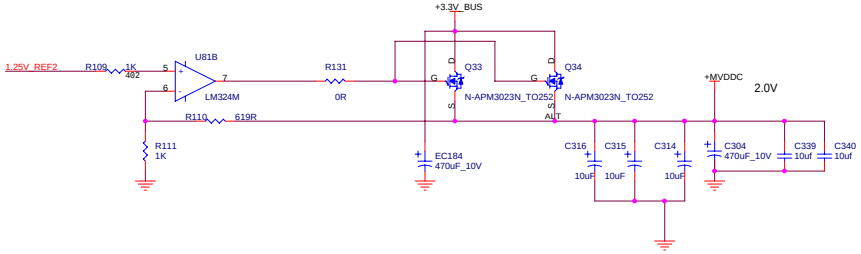
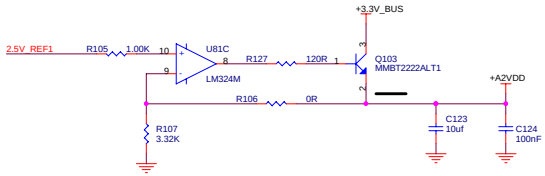
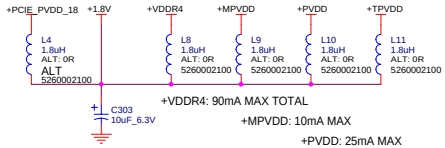


Change to SOT-23









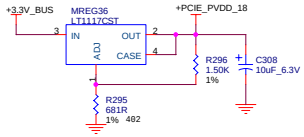
+VDDR4: 90mA MAX TOTAL

+MPVDD: 10mA MAX

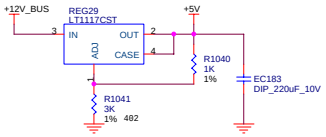
+PVDD: 25mA MAX

+TPVDD: 50mA MAX

Alt. regulator for PCIE_PVDD_18
Vout = 1.85V
Iout = 500mA MAX



Regulator for +5V
Vout = 5V
Iout = 20mA MAX



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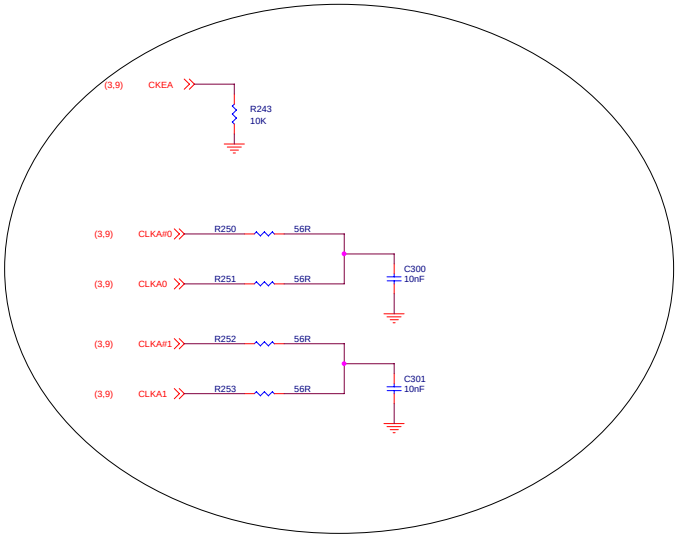

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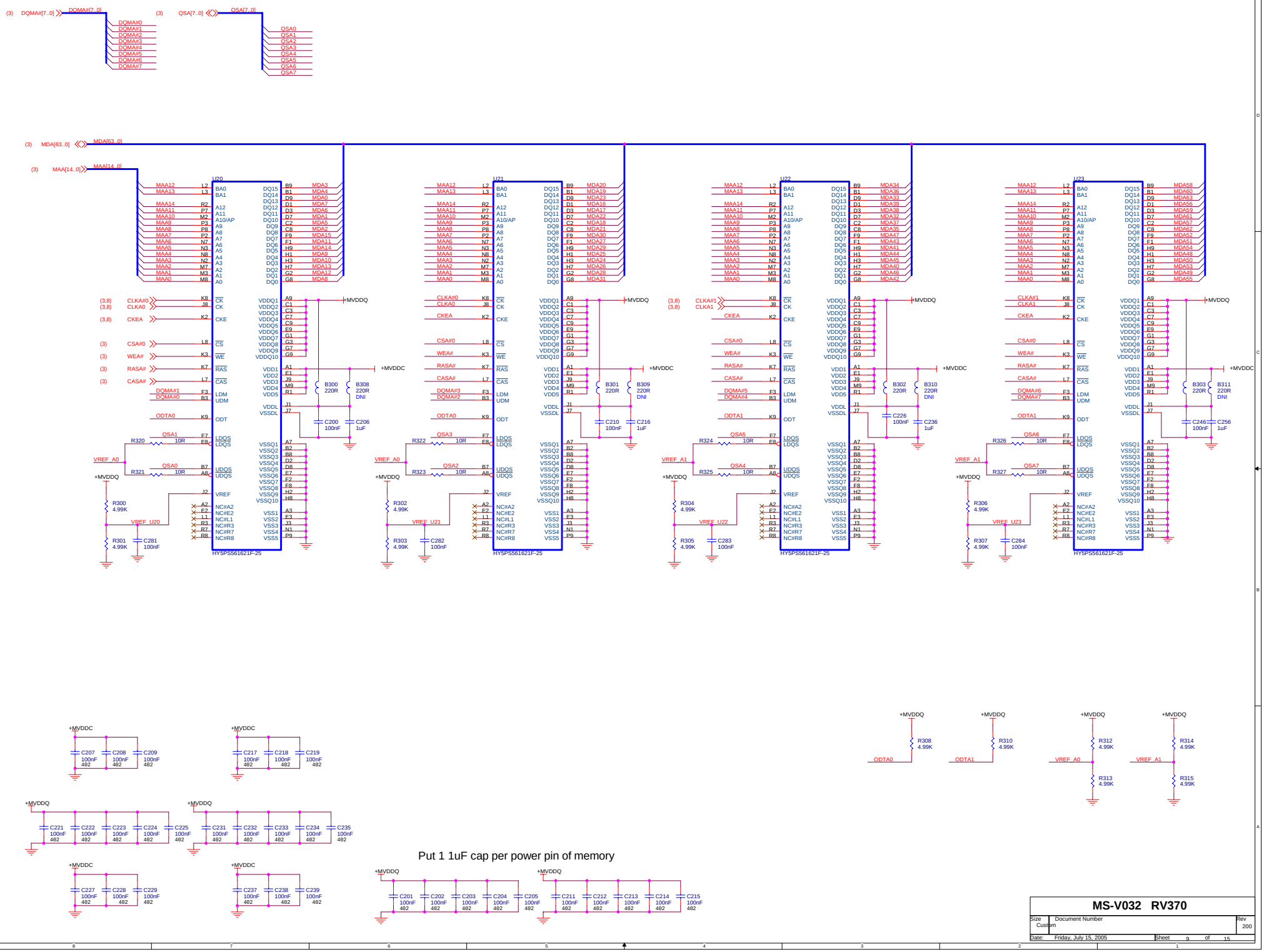
(3) DQMA#[7..0]
DQMA#[7..0]
DQMA#0
DQMA#1
DQMA#2
DQMA#3
DQMA#4
DQMA#5
DQMA#6
DQMA#7
(3) QSA[7..0]
QSA[7..0]
QSA0
QSA1
QSA2
QSA3
QSA4
QSA5
QSA6
QSA7
(3) MDA[63..0]
MDA[63..0]
(3) MAA[14..0]
MAA[14..0]
U20
U21
U22
U23
HY5PS561621F-25
+MVDDQ
+MVDDC
VREF_A0
VREF_A1
VREF_U20
VREF_U21
VREF_U22
VREF_U23
Put 1 1uF cap per power pin of memory
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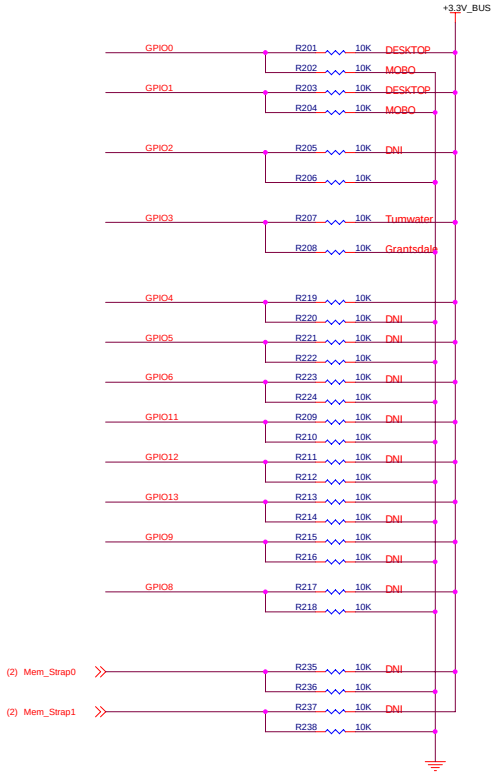
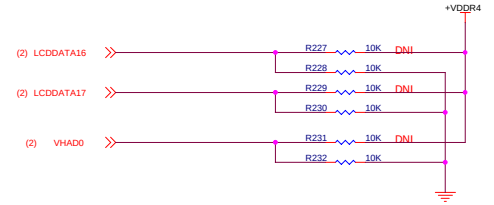
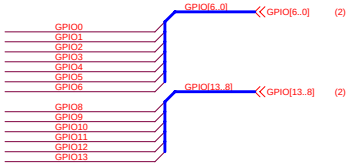
OPTION STRAPS





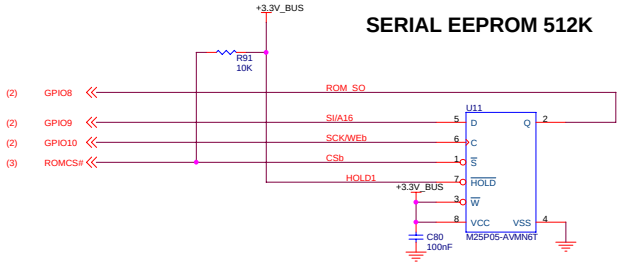


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDs. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDs from ROM 1011 - Serial M25P10 ROM (ST), chip IDs from ROM **1100 - Serial M25P05 ROM (ST), chip IDs from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDs from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K



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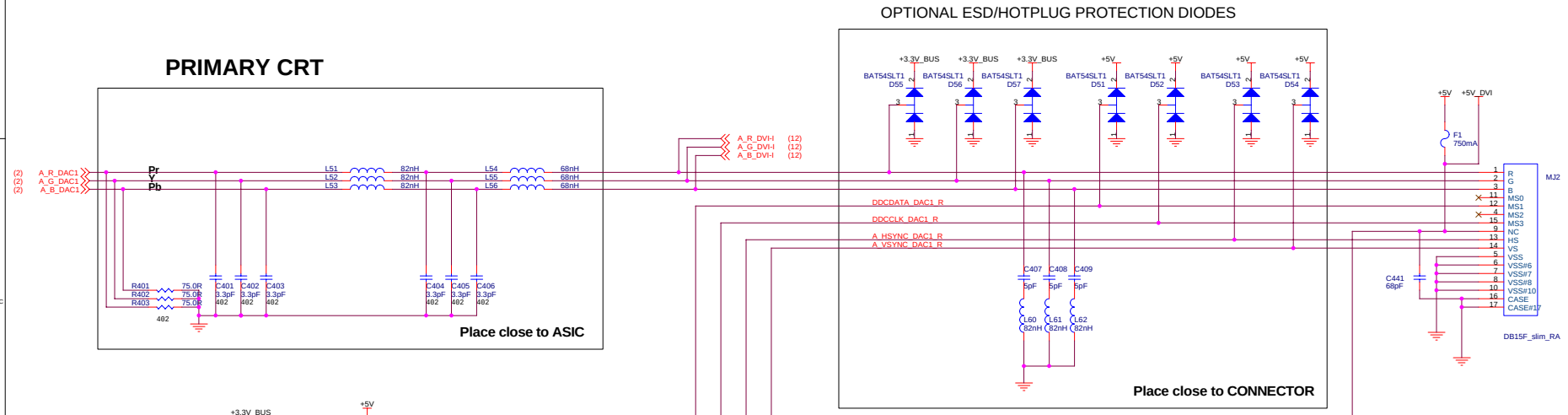
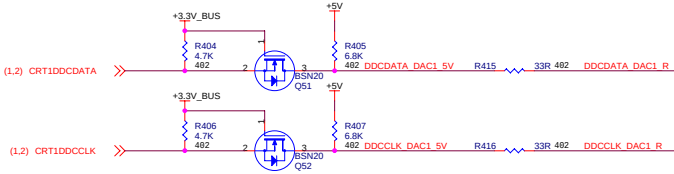
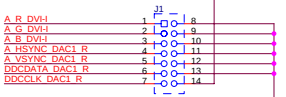
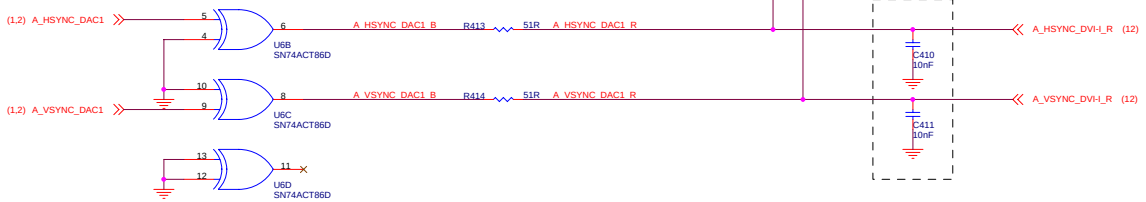
PRIMARY CRT

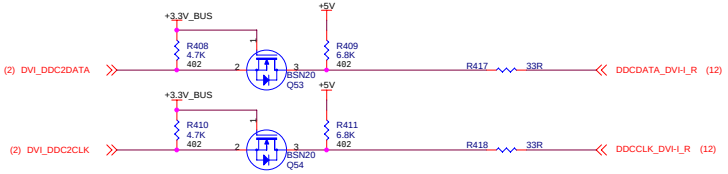


OPTIONAL ESD/HOTPLUG PROTECTION DIODES









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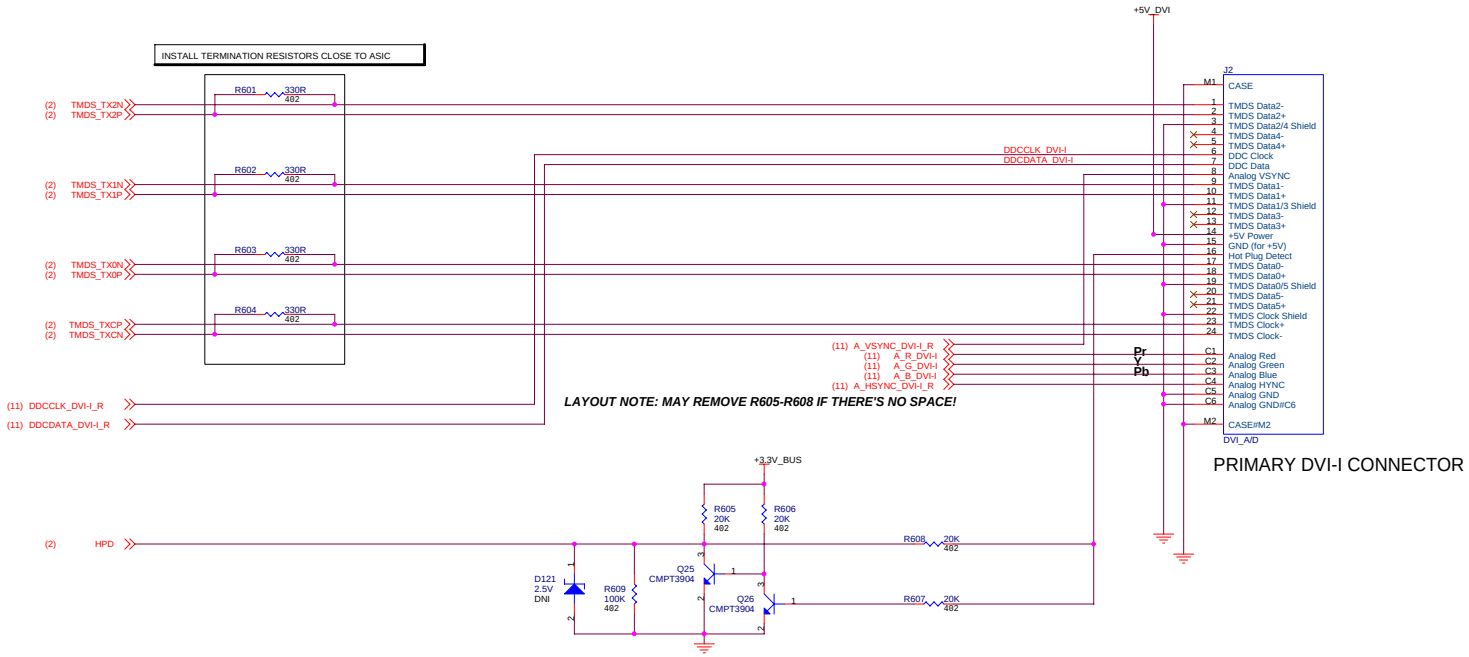

PRIMARY DVI-I CONNECTOR

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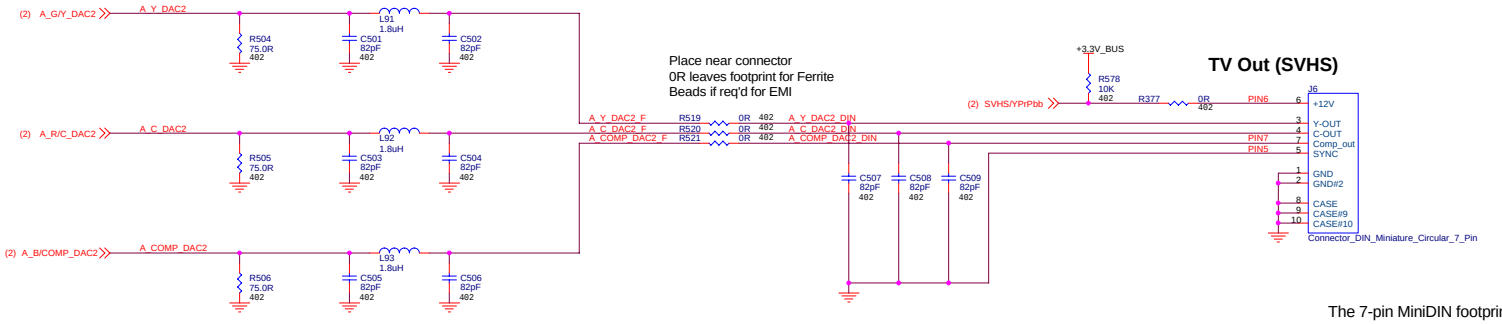
Place Resistors close to ASIC.



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500
- 4-pin Svideo MiniDIN P/N 6070001000

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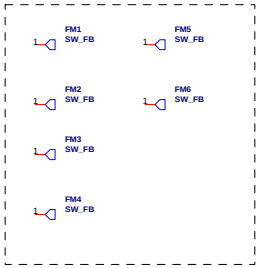

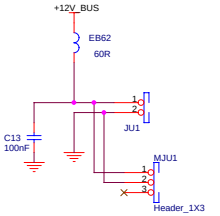

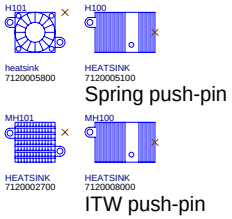

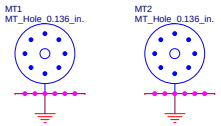

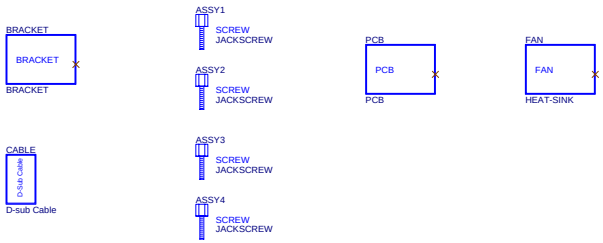

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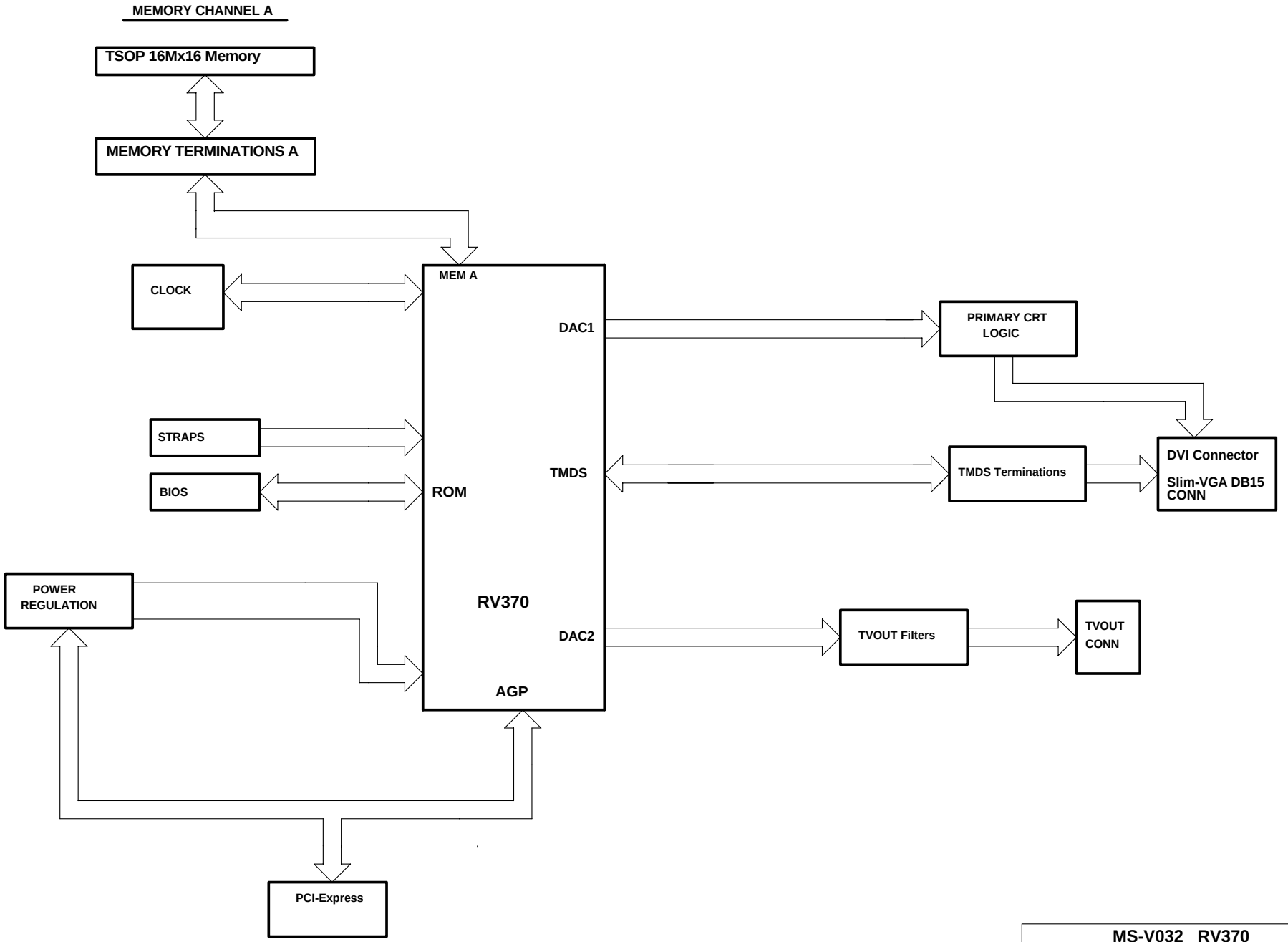

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