<Variant Name>

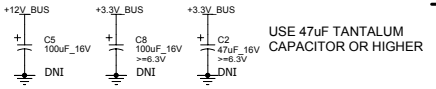
Title	Schematic No.	Date:
PCI-E RV380/370 128M TSOP VO-DMS59	105-A259xx-00C	**Tuesday, July 06, 2004**

REVISION HISTORY

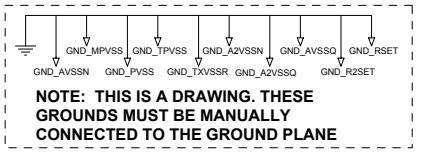
Rev 2

Sch Rev		Date	REVISION DESCRIPTION
0	00A	2003-09-10	PRELIMINARY BASED ON 105-A181xx-00A and 105-A200xx-00 - Use 402 R and C footprints as preferred - (pg1) Add 0R bypass for PERST#, and use XOR spared gate for buffer - (pg1) Keep only 1 100uF decoupling for +12V_BUS - (pg1) Connect B3 of edge connector directly to +12V_BUS - (pg2) Remove oscillator and change crystal to surface mount - (pg2) Hard pull-down on TEST_Y/MCLK - (pg2) Remove thermal interrupt, no provision for speed controlled fan - (pg2) Remove redundant TPs - (pg2) Pull-up on DVPCNTL_[3:0], remove RageTheater capture ports (VID/DVO[7:0]) - (pg2) DVOMode pull-up to 1.8V, set to 12-bit DVO (1.8V DVO I/O signalling) - (pg3) Memory interface based on A198, remove Channel B - (pg4) Remove power-up diodes - (pg5, 6, 7) Redesigned power regulators - (pg8, 9) Channel A only Series-Terminated TSOP interface (based on A200) - (pg11, 12, 13) Front-end based on Low-Profile VGA/DVI + VO design (based on A200)
		2003-09-22	- (pg5) Add RC snubber circuit on switching regulator - (pg7) Add R124 for power dissipation
		2004-01-13	- (Layout) Change to 6 layer - (pg2) Add series resistor for SI1162 DVO and control bus - (pg4) Add C98 and C99 on PCIE_VDDR, remove C980 - (pg5) Remove +Vout_Switcher, add power sequence circuit, remove +A2VDD pull-up on bottom MOSFET - (pg6) Remove MQ31, L12 - (pg6) Replace Q32 with CMPT3904 and add R1044, R1045 for +5V regulator - (pg6) Add R1043 and R1046 for +5V_DDC power and add preferred option of +5V from Opamp regulator, add R146 for PCIE_PVDD18 power sequence - (pg7) Add L4 for +PCIE_PVDD18 to +1.8V - (pg7) Remove Opamp regulator circuits - (pg12) Swapping HPD pins, add +5V_DDC power option - (pg12) Remove TVO signals from DMS-59 connector - (pg14) Change SI164 ext TMDS chip to SI1162
		2004-01-28	- (pg4) Remove C979, C981, C982, C983, C984 and C985 - (pg13) Change one set of filter capacitor to digital GND - (pg02, 10) Change +VDD_DVO to +VDDR4
1	00B	2004-04-15	- (pg04) Remove CP2, CP3, CP4, CP5, CP6, CP8, CP9, CP10 and CP11, dual-footprint - (pg05) Add MR357 for power sequencing - (pg06) Remove R6, +5V reg is not required for VESA compliance - (pg06) Remove C986, C987, C988, C989, C990, C991, C992 and C993, dual-footprint - (pg06) Add C800 for stability - (pg07) Remove MC306 and MC308 - (pg11, 12, 13) Remove R991, R992, R993, R997, R998 and R999 for joined ground - (pg12 and 14) Correct R318 and R606 short for HPD - (pg12) Add +5V_VESA and +5V_VESA2 power regulator, remove B21 and F1, add C442 - (pg13) Delete R513 and R514 for EMI, connect TVO shield directly to Chassis GND
2	00C	2004-06-10	- (Layout) EMI changes Remove int. TMDS ground guard Move ext. TMDS to inner layer Move DVO bus from layer 3 to layer 4 - (pg6) change +VDDC_CT source from +3.3V_BUS - (pg6) change +PCIE_VDDR optional regulator reference from +3.3V_BUS to +PCIE_PVDD18 - (pg14) change TMDS differential pairs termination resistors and capacitors to 402 footprint - (pg14) change AVCC, PVDD, VCC decoupling caps to 402 footprint and add 10uF filtering, spearate PVCC1, PVCC2, AVCC1 and AVCC2. - (pg14) remove R319, R320, R620 and R625 redundant straps

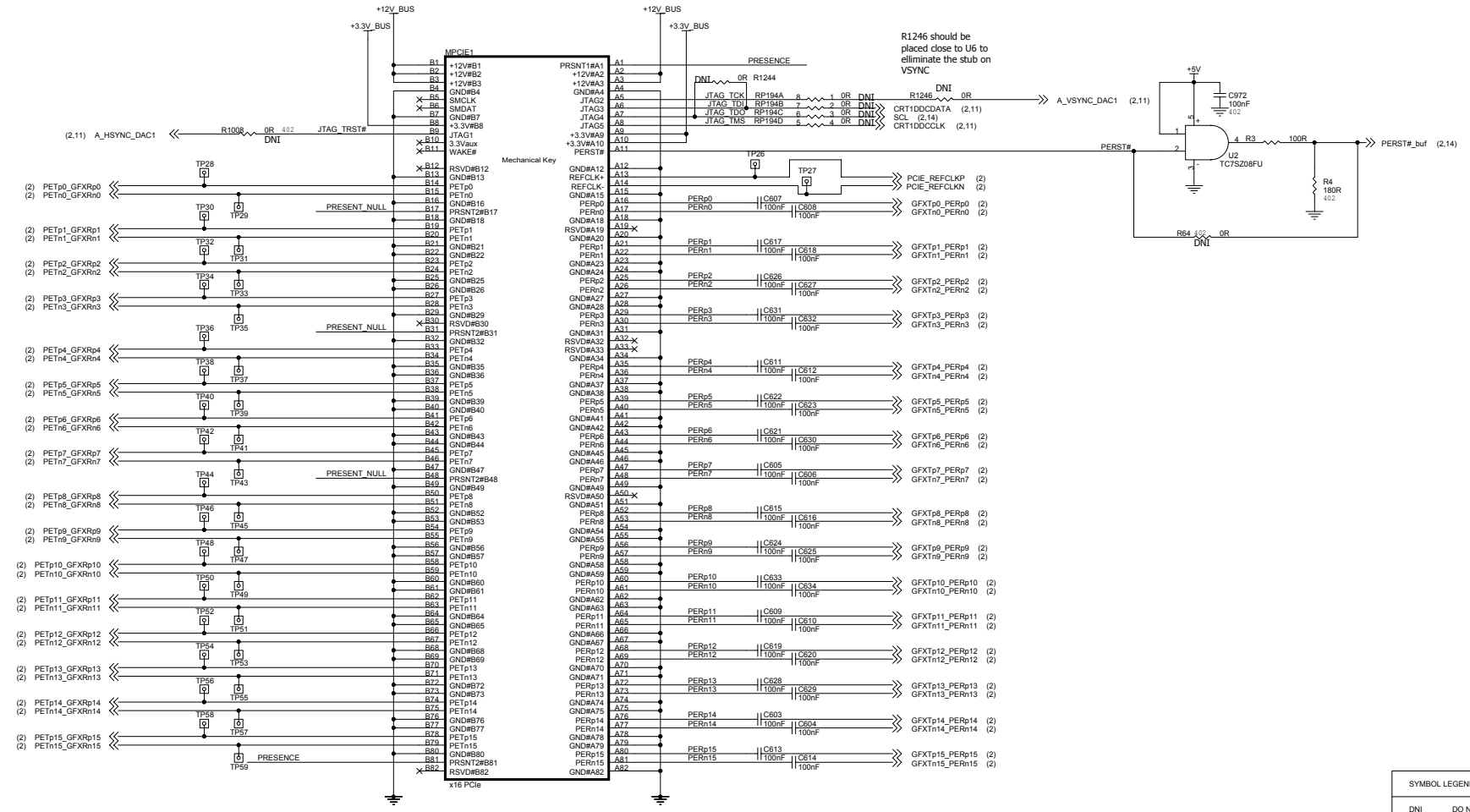
PCI-EXPRESS EDGE CONNECTOR



USE 47uF TANTALUM CAPACITOR OR HIGHER



NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

<Variant Name>

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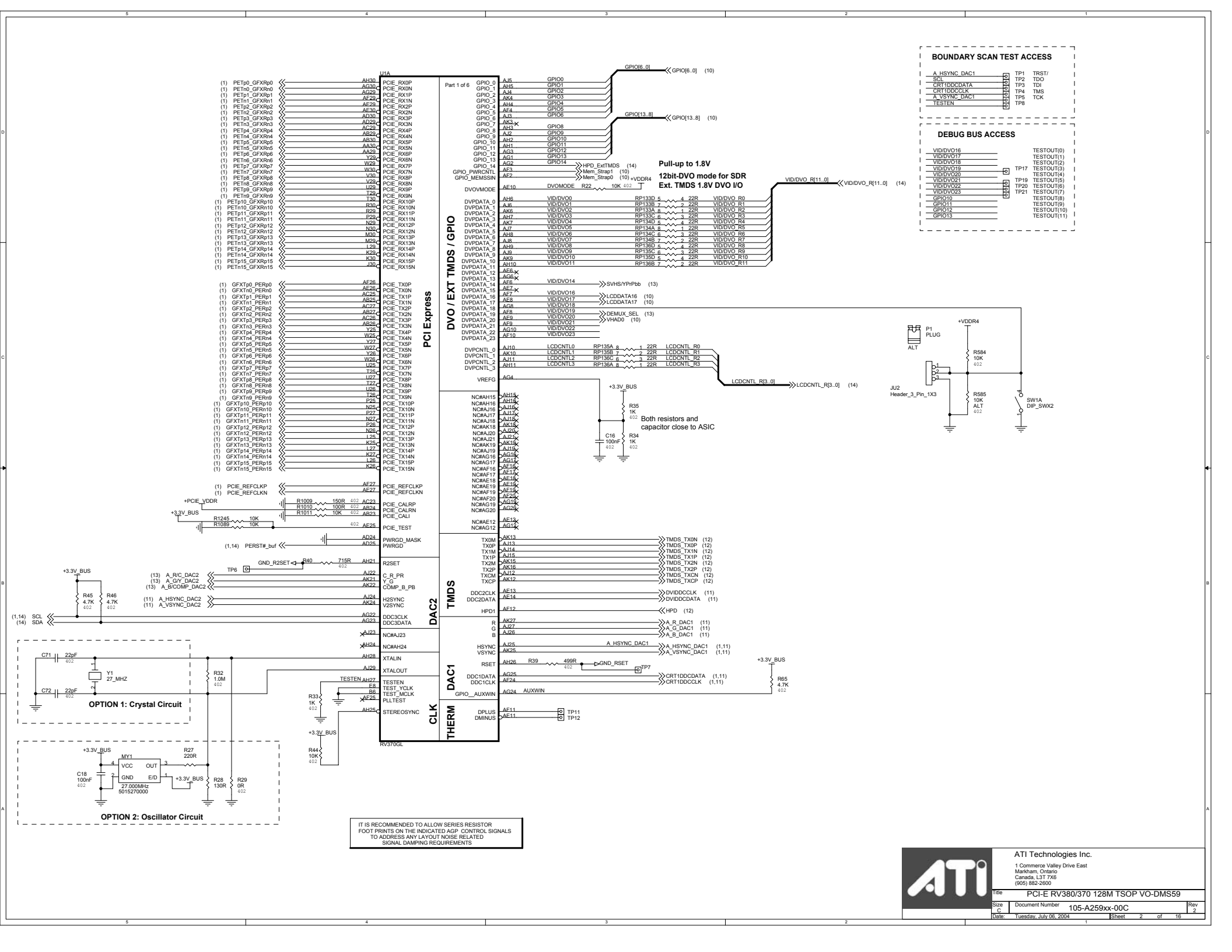
BOUNDARY SCAN TEST ACCESS
A_HSYNC_DAC1
SCL
CRT1DDCDATA
CRT1DDCCLK
A_VSYNC_DAC1
TESTEN
TP1 TRST/
TP2 TDO
TP3 TDI
TP4 TMS
TP5 TCK
TP8
DEBUG BUS ACCESS
VID/DVO16
VID/DVO17
VID/DVO18
VID/DVO19
VID/DVO20
VID/DVO21
VID/DVO22
VID/DVO23
GPIO10
GPIO11
GPIO12
GPIO13
TP17
TP19
TP20
TP21
TESTOUT(0)
TESTOUT(1)
TESTOUT(2)
TESTOUT(3)
TESTOUT(4)
TESTOUT(5)
TESTOUT(6)
TESTOUT(7)
TESTOUT(8)
TESTOUT(9)
TESTOUT(10)
TESTOUT(11)
U1A
Part 1 of 6
PCI Express
DVO / EXT TMDS / GPIO
TMDS
DAC2
DAC1
CLK
THERM
RV370GL
Pull-up to 1.8V
12bit-DVO mode for SDR
Ext. TMDS 1.8V DVO I/O
Both resistors and capacitor close to ASIC
OPTION 1: Crystal Circuit
OPTION 2: Oscillator Circuit
IT IS RECOMMENDED TO ALLOW SERIES RESISTOR FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS TO ADDRESS ANY LAYOUT NOISE RELATED SIGNAL DAMPING REQUIREMENTS
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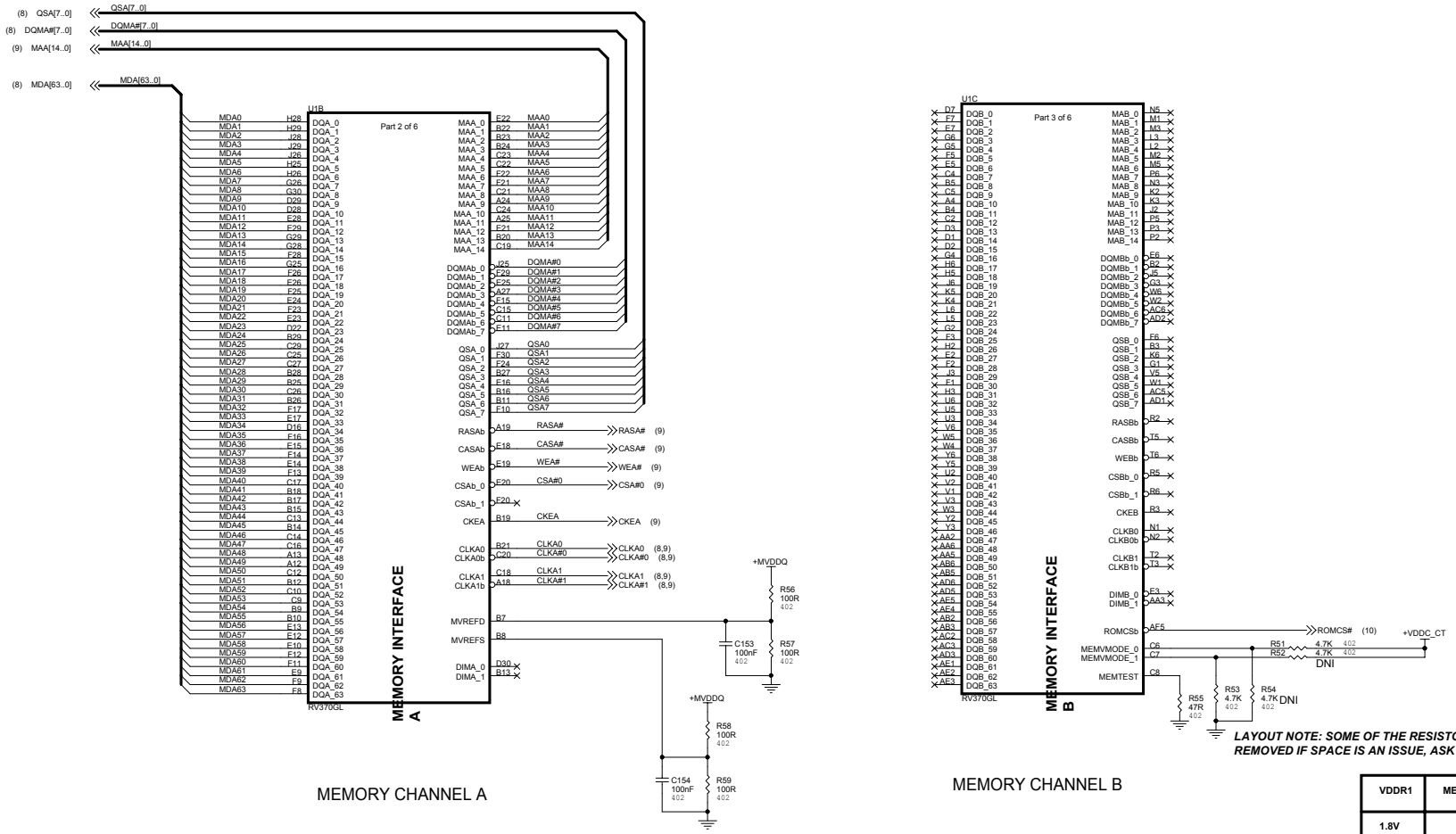

MEMORY CHANNEL A

PLACE C351/152 VERY CLOSE TO ASIC
R56/57/58/59 CLOSE TO ASIC AS WELL

MEMORY CHANNEL B

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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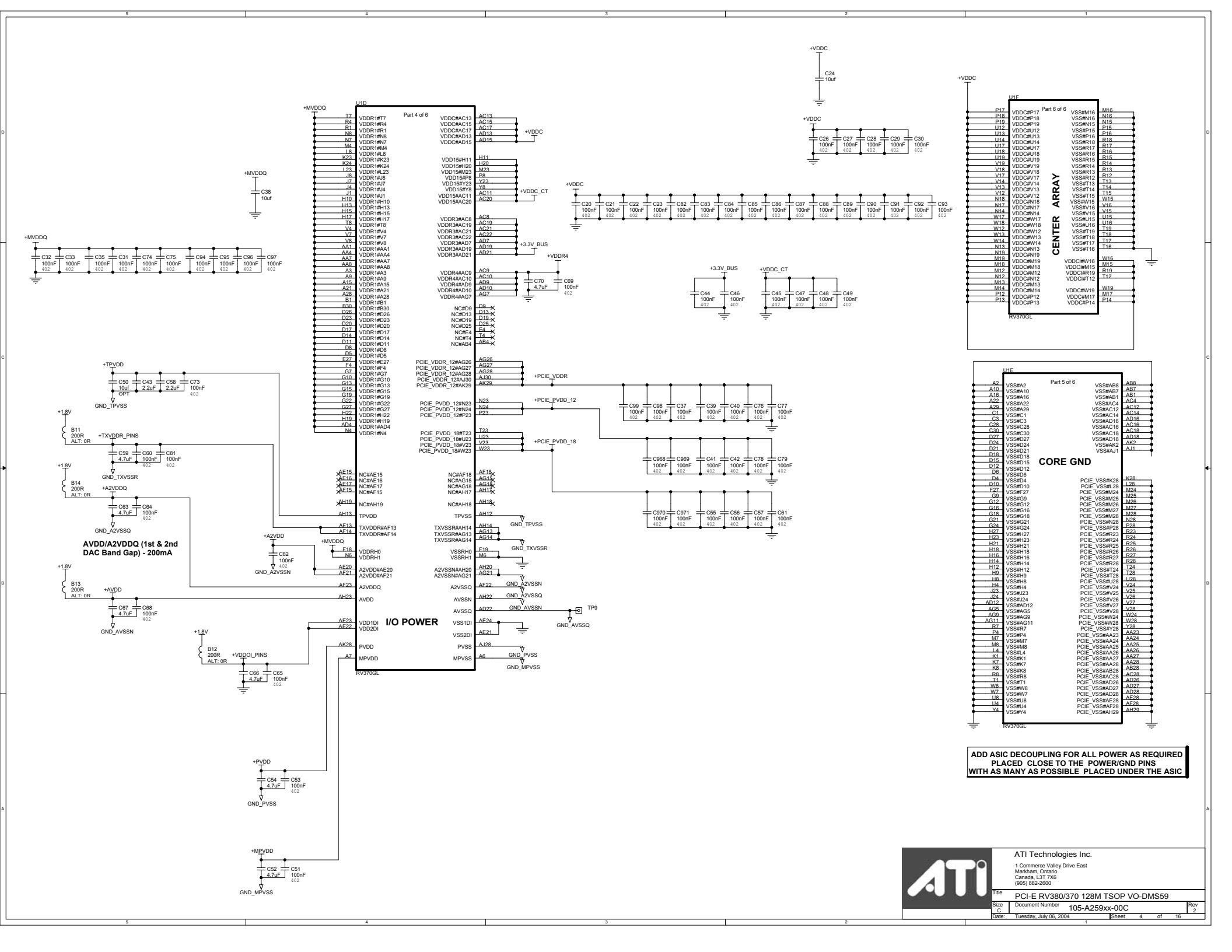
U1D
Part 4 of 6
RV370GL
I/O POWER
+MVDDQ
+VDDC
+VDDC_CT
+3.3V_BUS
+VDDR4
+PCIE_VDDR
+PCIE_PVDD_12
+PCIE_PVDD_18
+TPVDD
+1.8V
+A2VDDQ
+AVDD
+VDDOI_PINS
+PVDD
+MPVDD
GND_TPVSS
GND_TXVSSR
GND_A2VSSQ
GND_A2VSSN
GND_TPVSS
GND_TXVSSR
GND_A2VSSN
GND_A2VSSQ
GND_AVSSN
GND_AVSSQ
GND_PVSS
GND_MPVSS
TP9
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
U1E
Part 5 of 6
CORE GND
U1F
Part 6 of 6
CENTER ARRAY
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
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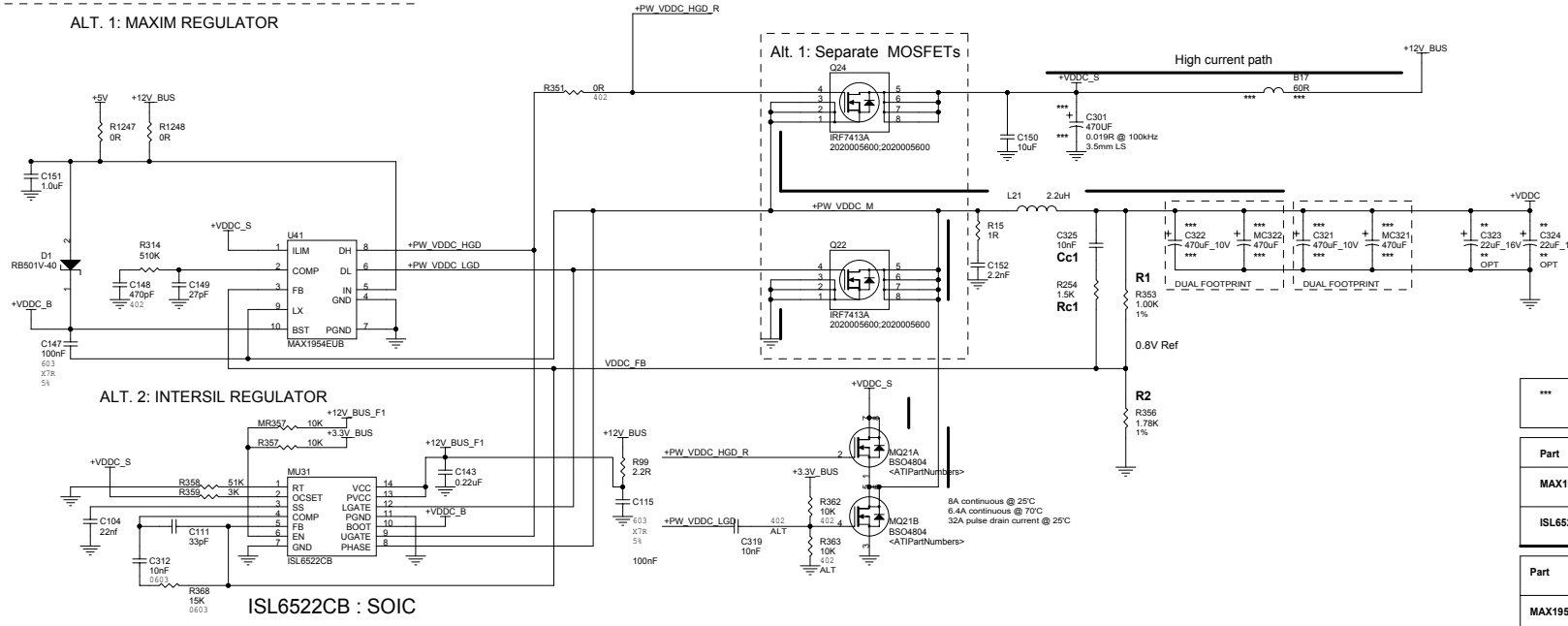
Regulator for VDDC (ASIC Core)

Vout = 1.2V ~ 1.3V

ALT. 1: MAXIM REGULATOR

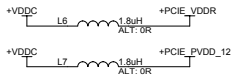


ISL6522CB : SOIC

*** Indicate number of power via required for the connection

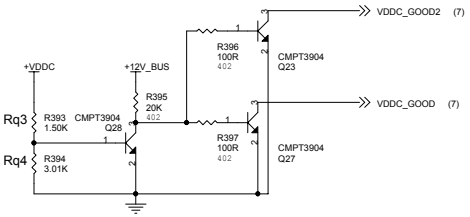
Part	NOTES
MAX1954	Do not install Cc1, Rc1
ISL6522	Install Cc1, Rc1

Part	Vout	R1	R2
MAX1954 ISL6522	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
0.8V Ref	1.25V	1.00K 1% ATI P/N 3240100100	1.78K 1% ATI P/N 3240178100
0.8V Ref	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100



Circuit to hold PCI-E voltage low and wait for +VDDC for proper power sequence

+VDDC	Rq3	Rq4
+1.3V	1.5K	2.4K
+1.2V	1.5K	3K



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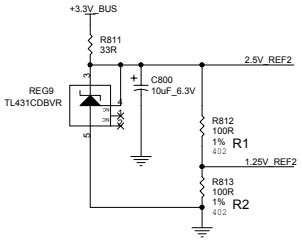
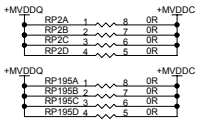
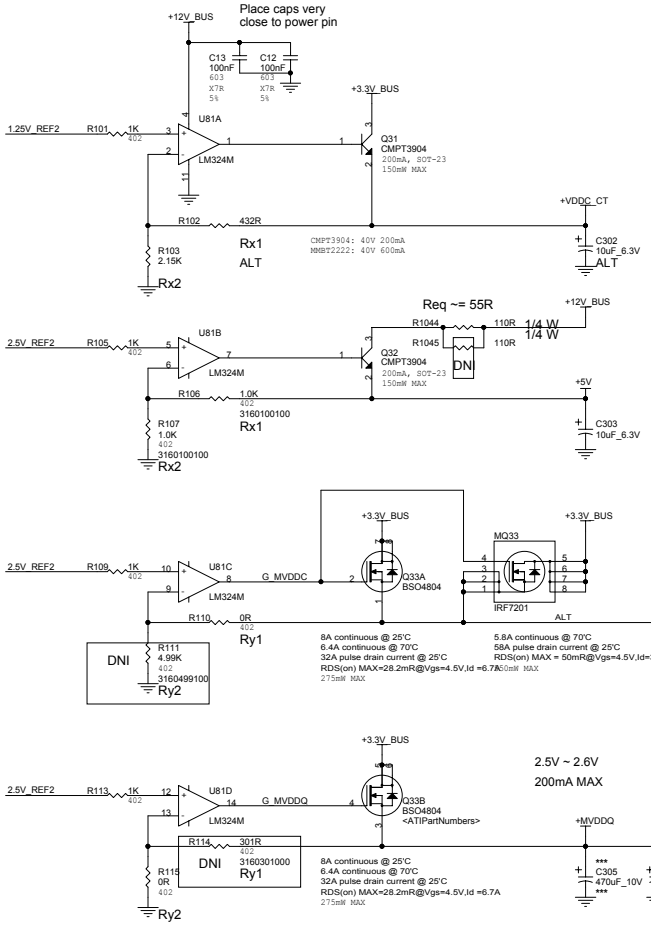


Voltage Req.	R1	R2
0.8V	150R P/N 3160150000 402	71.5R P/N 324075R500
1.25V	100R P/N 3160100000 402	100R P/N 3160100000 402
1.5V	100R P/N 3160100000 402	150R P/N 3160150000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

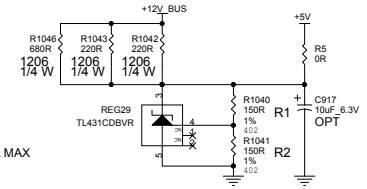
Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.55	475R (402, 1%) P/N 3160475000	2K (402, 1%) P/N 3160200100
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240015200

Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.61V	221R (402, 1%) P/N 3160221000	4.99K (402, 1%) P/N 3160499100
2.5V	0R P/N 3230000000 603 P/N 3150000000 402	DNI



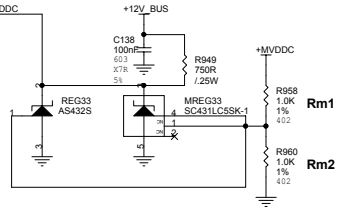


Alt regulator for +5V
Vout = 5V
Iout = 10mA MAX (+5V)



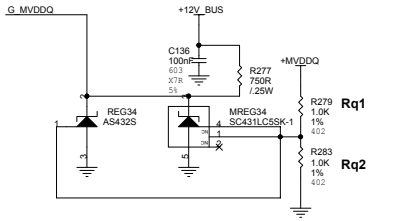
Alt. regulator for +MVDDC
Vout = 2.5V ~ 2.6V
Iout = 500mA MAX

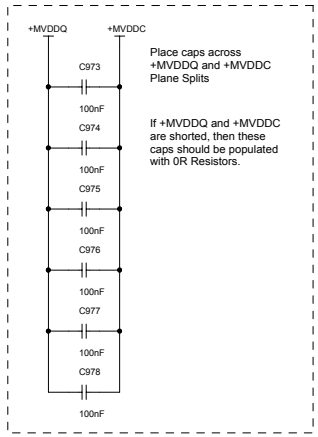
Voltage Req.	Rm1	Rm2
3.34V [-0.04V/+0.04V]	4.32K	2.55K
3.45V [-0.04V/+0.04V]	4.32K	2.43K
2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100



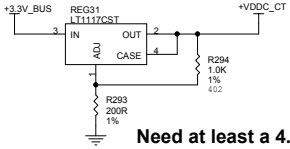
Alt regulator for +MVDDQ
Vout = 2.5V ~ 2.6V
Iout = 200mA MAX

Voltage Req.	Rq1	Rq2
1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
2.5V	1K 3240100100	1K 3240100100
2.6V	4.75K 3240475100	4.32K 3240432100



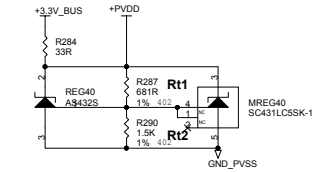


Alt regulator for +VDDC_CT
Vout = 1.5V
Iout = 150mA MAX

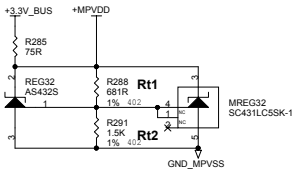


Need at least a 4.7uF output cap for stability

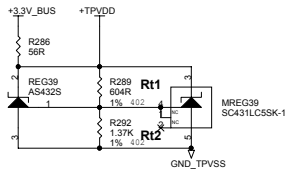
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



Alt regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX



Alt. regulator for +TPVDD
Vout = 1.65V ~ 1.85V
Iout = 20mA MAX



	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100

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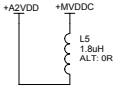
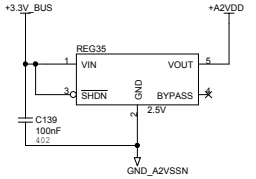
Alt. regulator for +A2VDD
Vout = 2.5V
Iout = 120mA MAX

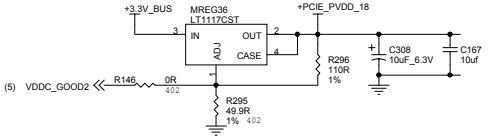
2.5V
120mA





+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.

Alt. regulator for PCIE_PVDD_18
Vout = 1.82V
Iout = 500mA MAX



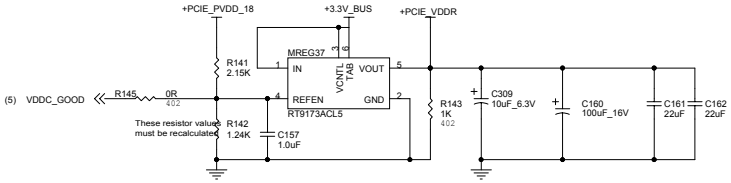
Need at least a 10uF Tant. output cap for stability
Min. Load Current: 10mA

Optional when +Vout_Switcher is above 1.2V

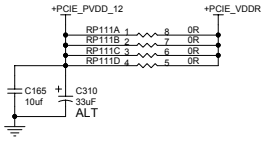
+VDDR4: 90mA MAX TOTAL
+MPVDD: 10mA MAX
+PVDD: 25mA MAX
+TPVDD: 50mA MAX

Rails derived from +VDDR4
+AVDD: 10mA MAX
+A2VDDQ: 20mA MAX
+VDDOI_PINS: 20mA MAX
+TXVDDR_PINS: 20mA MAX

+PCIE_VDDR: 1.2V 1300mA MAX



+PCIE_PVDD_12: 1.2V 250mA MAX



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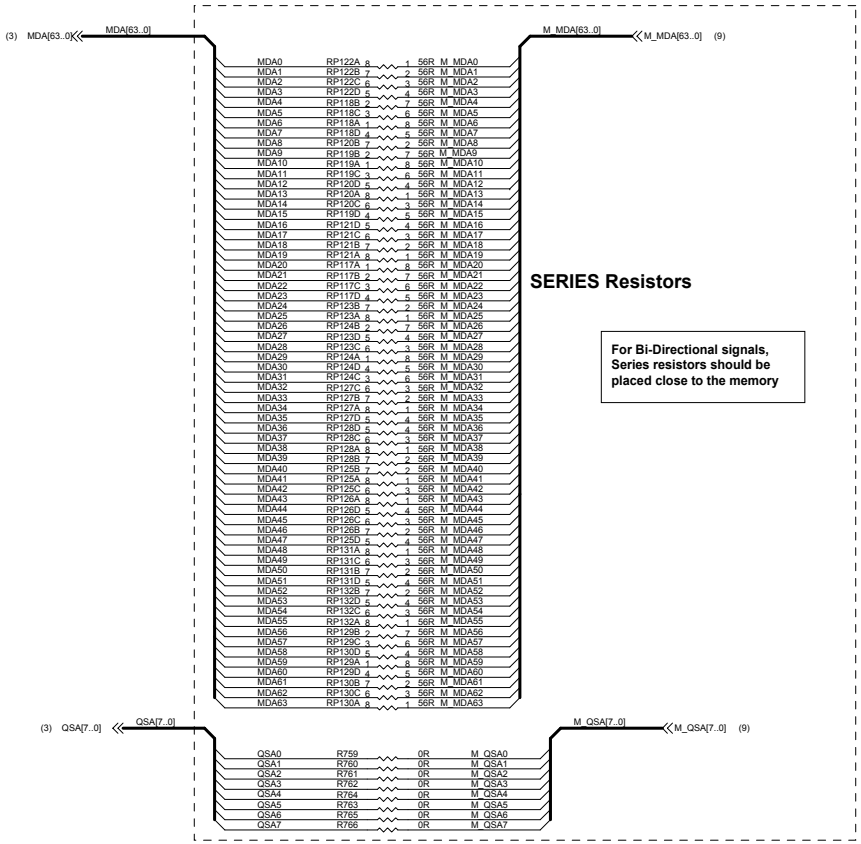

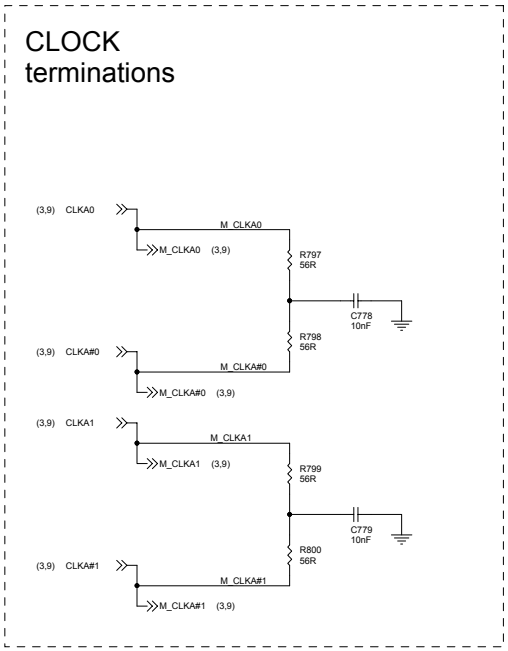

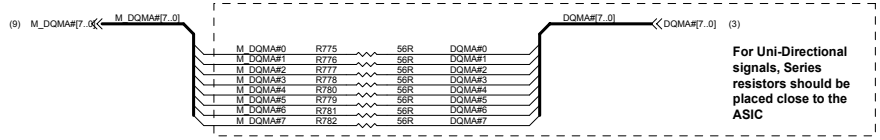

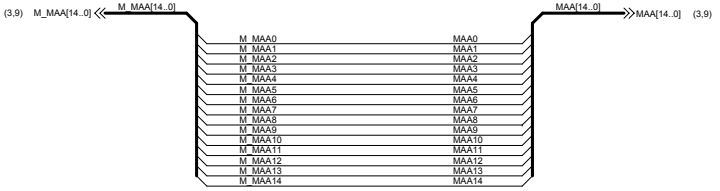

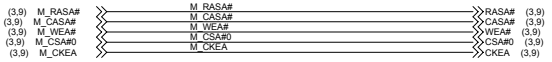

<Variant Name>

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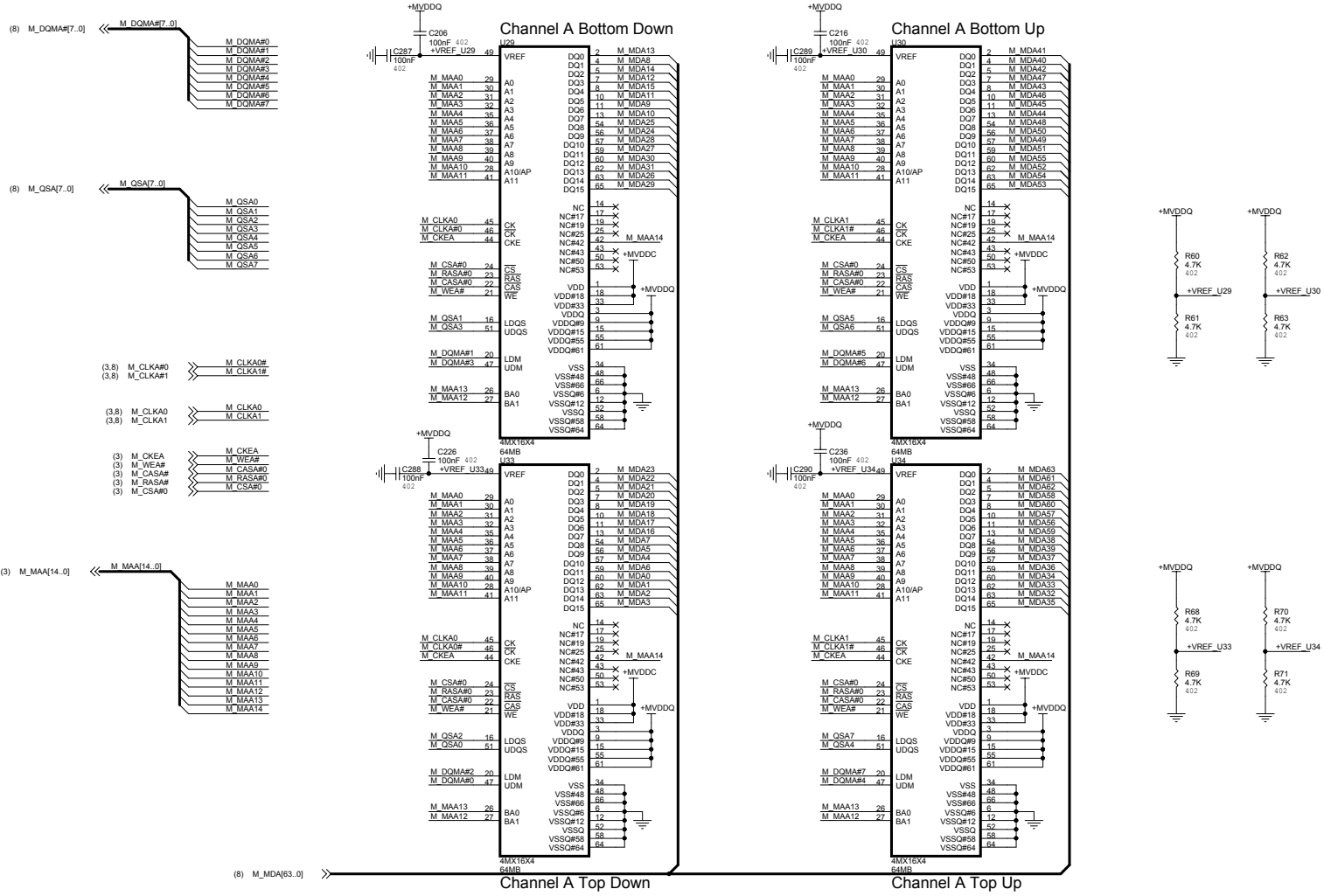
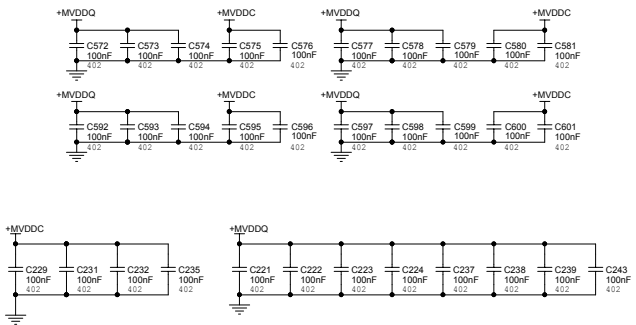


Put 1 1uF cap per power pin of memory



DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

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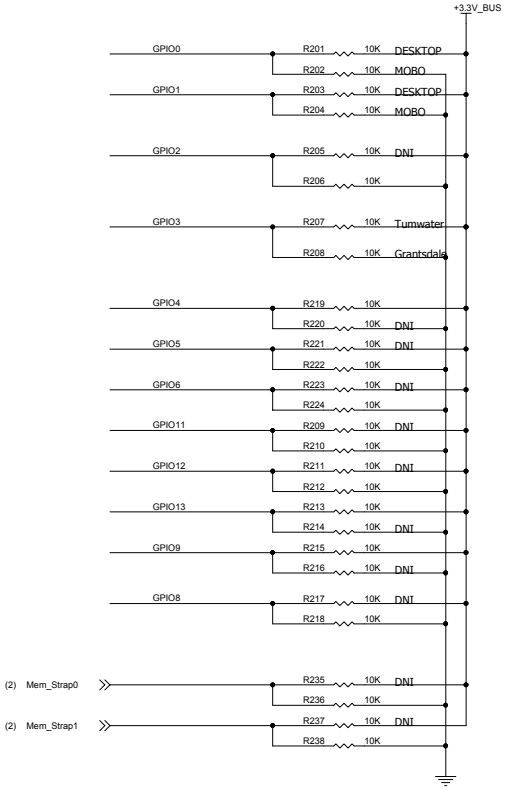
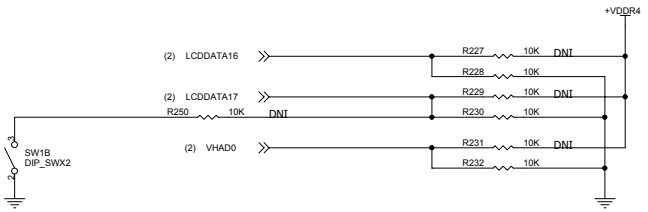
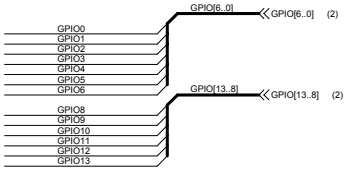
OPTION STRAPS





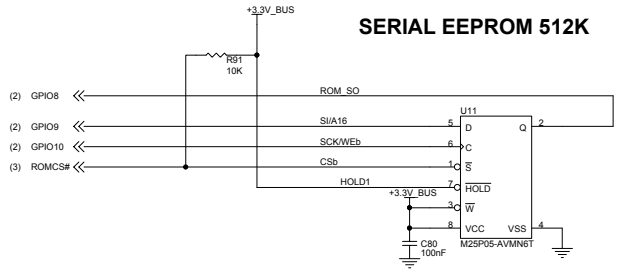


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K



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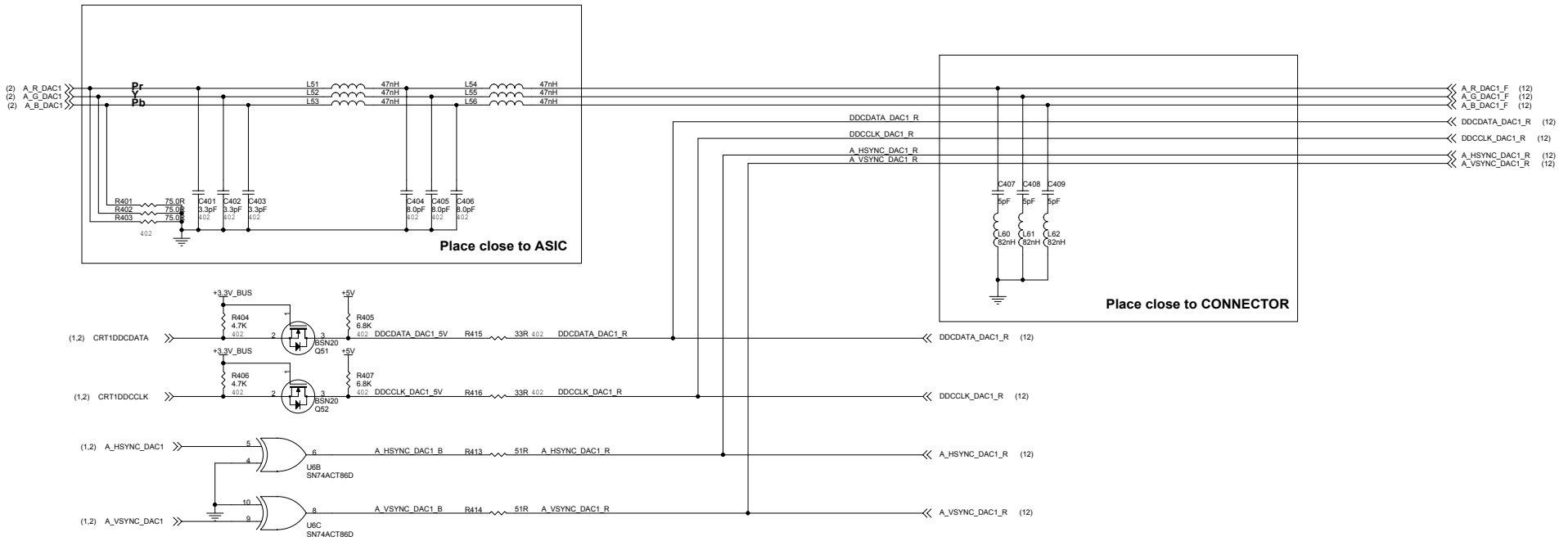
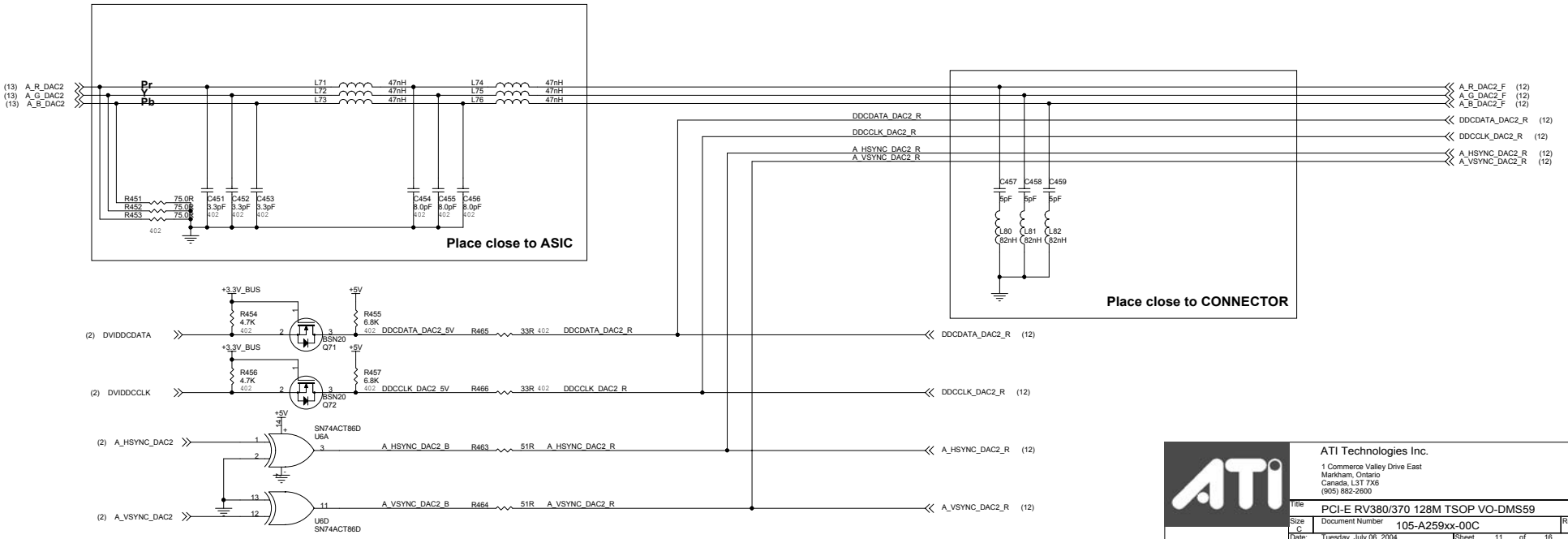
PRIMARY CRT



2nd CRT



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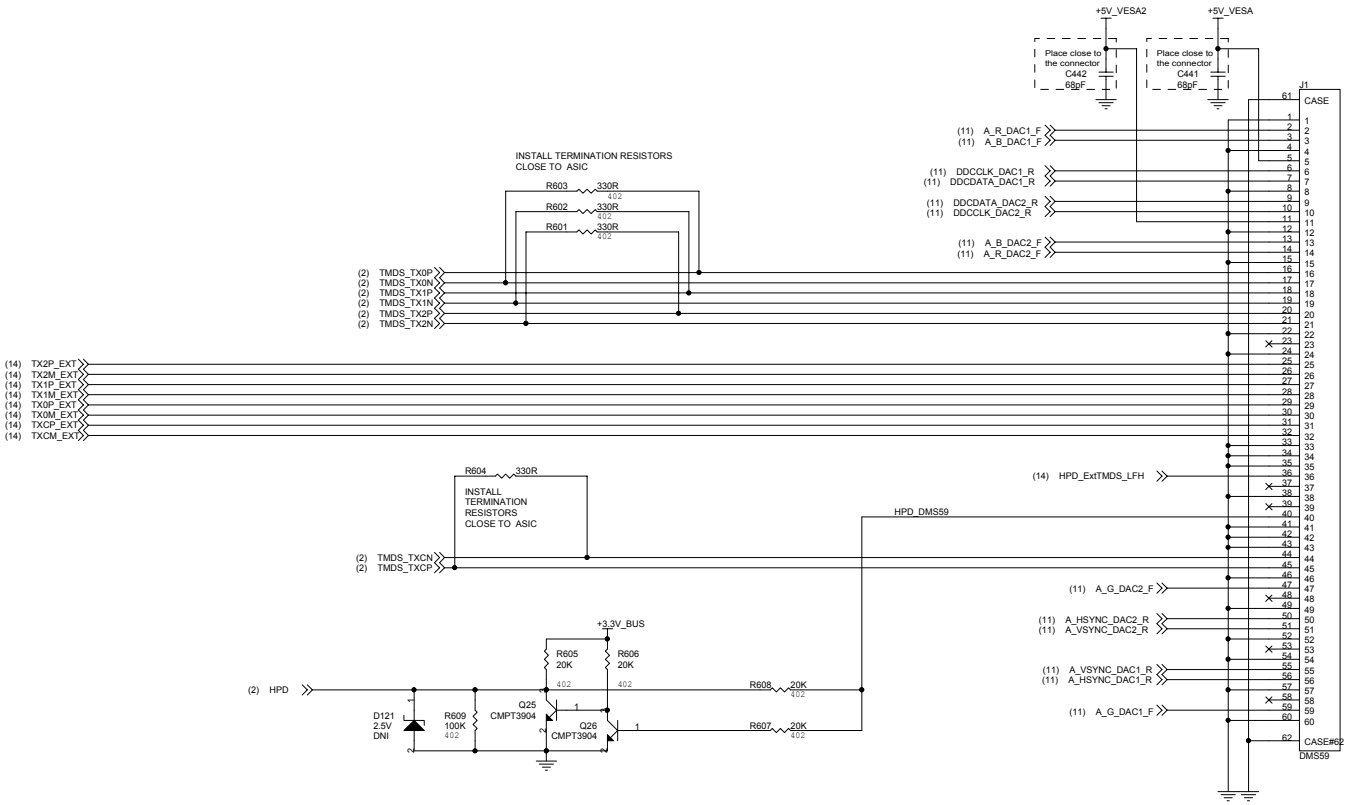
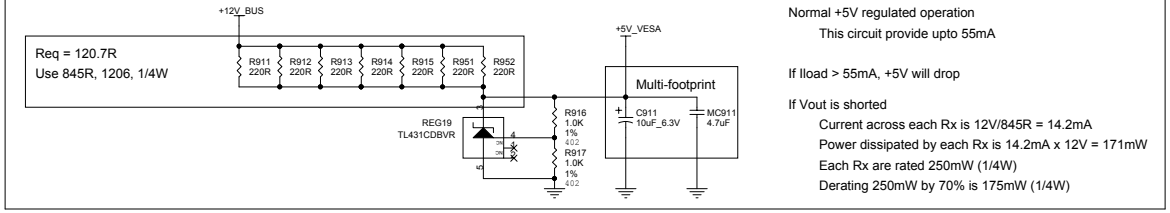
VESA Multi-Display Interface DMS-59 Connector



Connector 1	
Signals	Mapping
VGA:	DAC1
DVI:	External TMDS
HPD:	External TMDS HPD
DDC:	CRT1 DDC
5V:	+5V_VESA

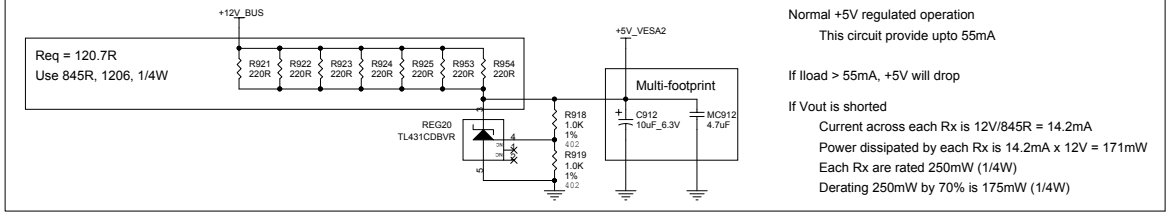
Connector 2	
Signals	Mapping
VGA:	DAC2 (TVDAC)
DVI:	Internal/Integrated TMDS
HPD:	Internal/Integrated TMDS HPD
DDC:	DVI DDC
5V:	+5V_VESA2



Normal +5V regulated operation
This circuit provide upto 55mA

If Iload > 55mA, +5V will drop

If Vout is shorted
Current across each Rx is 12V/845R = 14.2mA
Power dissipated by each Rx is 14.2mA x 12V = 171mW
Each Rx are rated 250mW (1/4W)
Derating 250mW by 70% is 175mW (1/4W)



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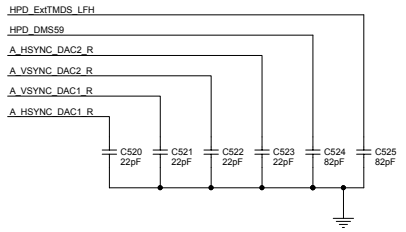

EMI Capacitors, place close to connector

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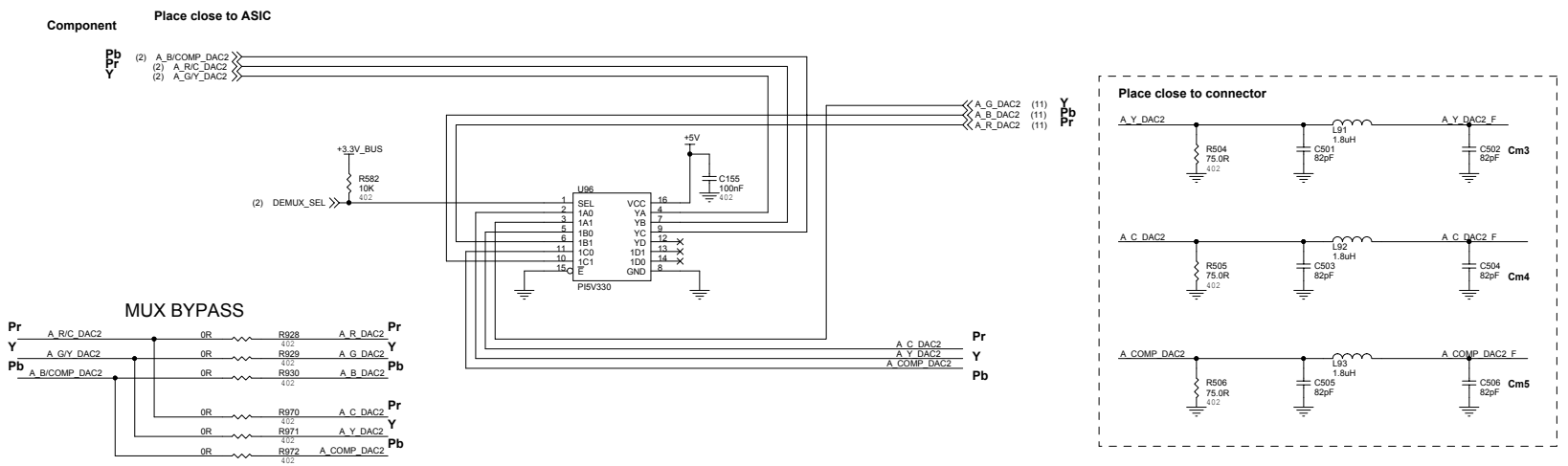
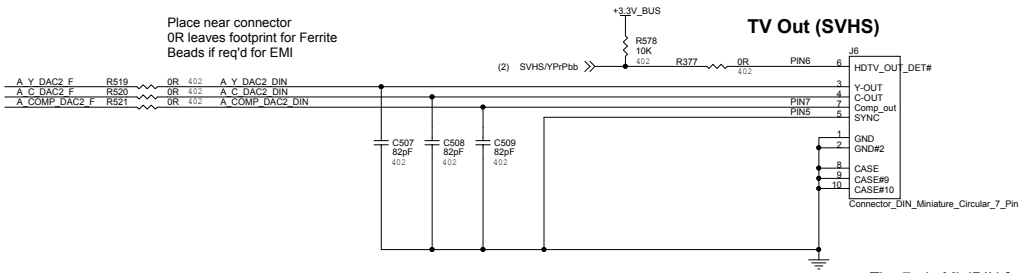
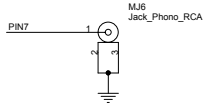




The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500
- 4-pin Svideo MiniDIN P/N 6070001000



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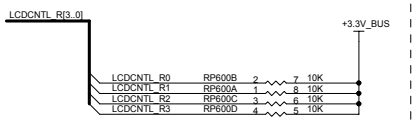
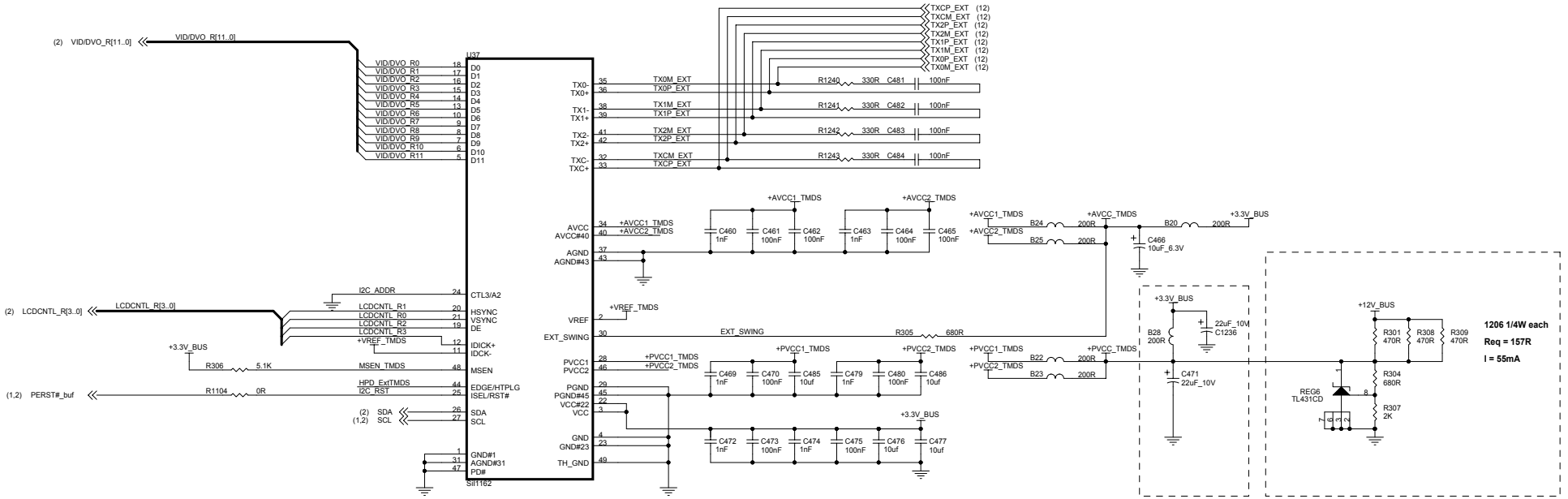
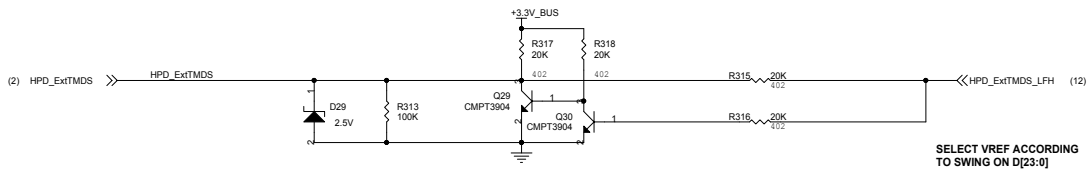
MUST BE INSTALLED IF NO
TMDS IS INSTALLED



Place close to TMDS





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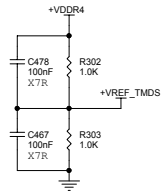
TO SWING ON D[23:0]



SELECT VREF ACCORDING
TO SWING ON D[23:0]

<Variant Name>

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DVI/VGA SCREWS

ASSY1
SCREW

ASSY2
SCREW

MISC. BOARD PARTS

ASSY7
ANTISTATIC BAG
6_X_11

ASSY5
ATI LOGO LABEL
ATI_LOGO_LABEL

ASSY-PCB1
ATI LOGO LABEL

ASSY8
BLANK LABEL
1.5W_X_0.50H
9050005900;9050005900

ASSY6
SCREW
PAN_HEAD

MH101
HEATSINK
7120002700

H101
HEATSINK
7120008000

MT1
MT_Hole_0.136_in.

H102
heatsink

+12V_BUS
JU1
COMMON

LP brackets

ASSY3
BRACKET
LP, NO TABS, Dual DVI
80200326B0

ASSY4
BRACKET
LP, TOP TAB, DIN, Dual DVI
80200327F0

ATX brackets

ASSY10
BRACKET
DUAL, NO TABS, Slim VGA, DIN, DVI

ASSY9
BRACKET
TOP TAB (LP), DIN, Dual DVI

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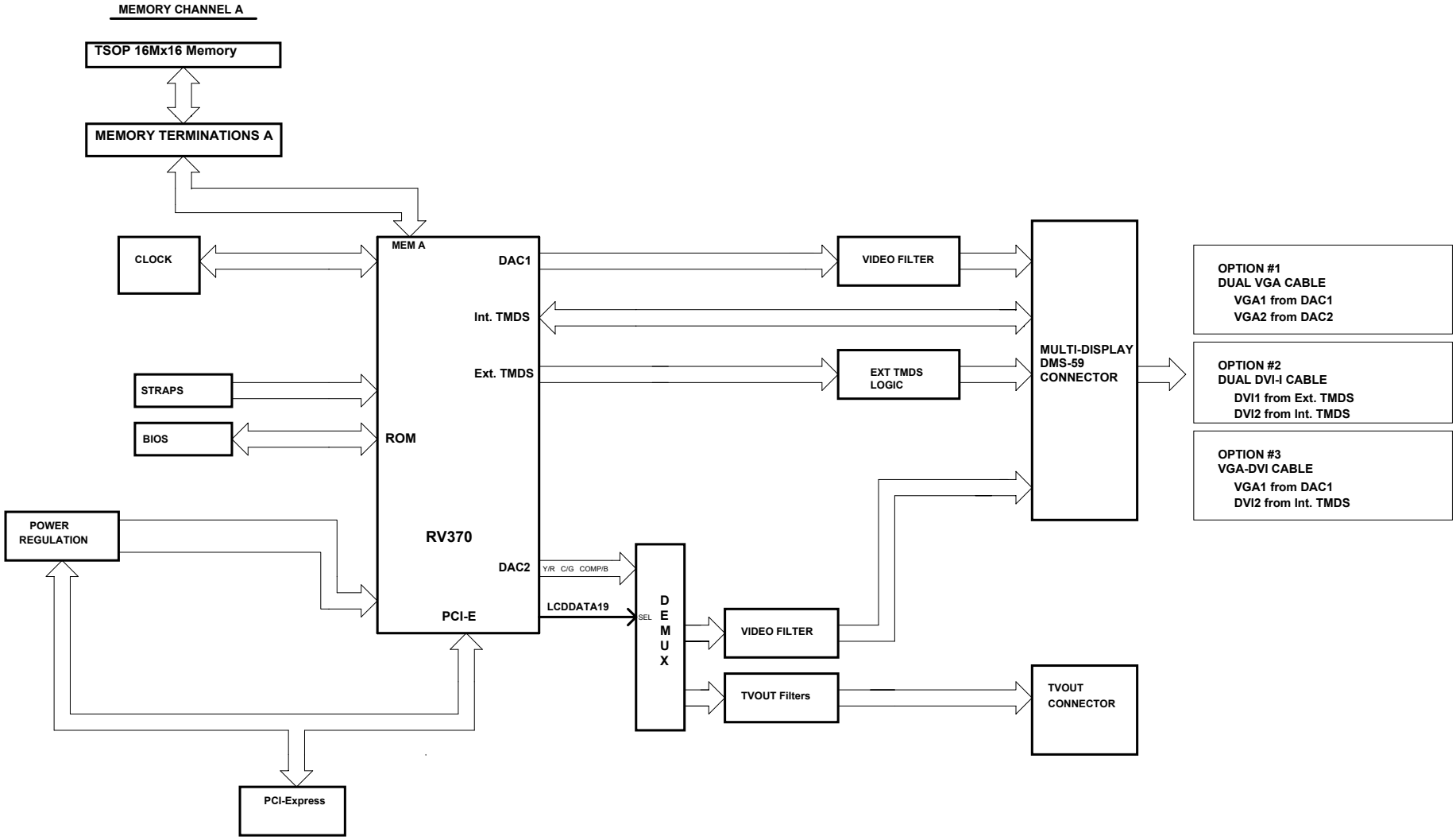

<Variant Name>

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