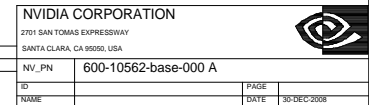
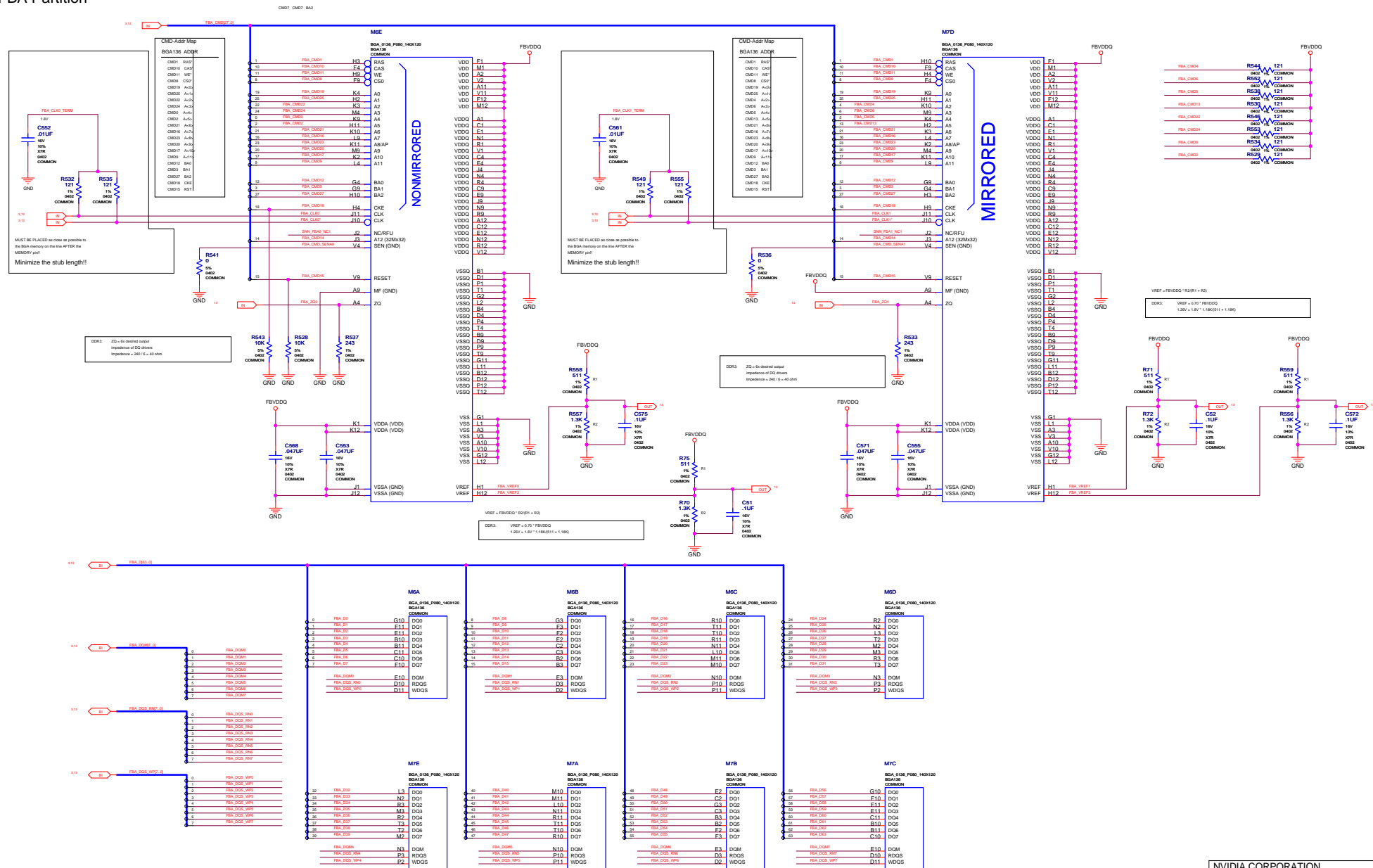




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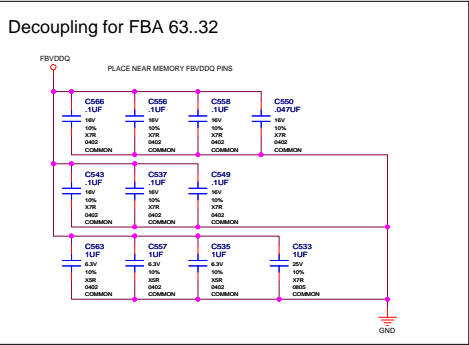
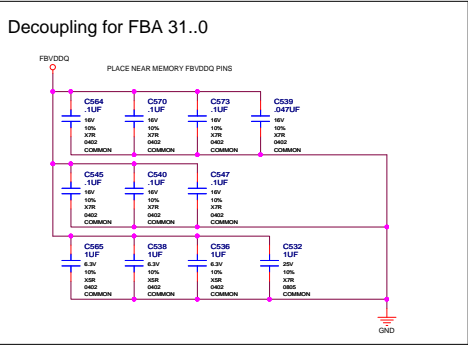


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PAGE DETAIL	FBA Partition

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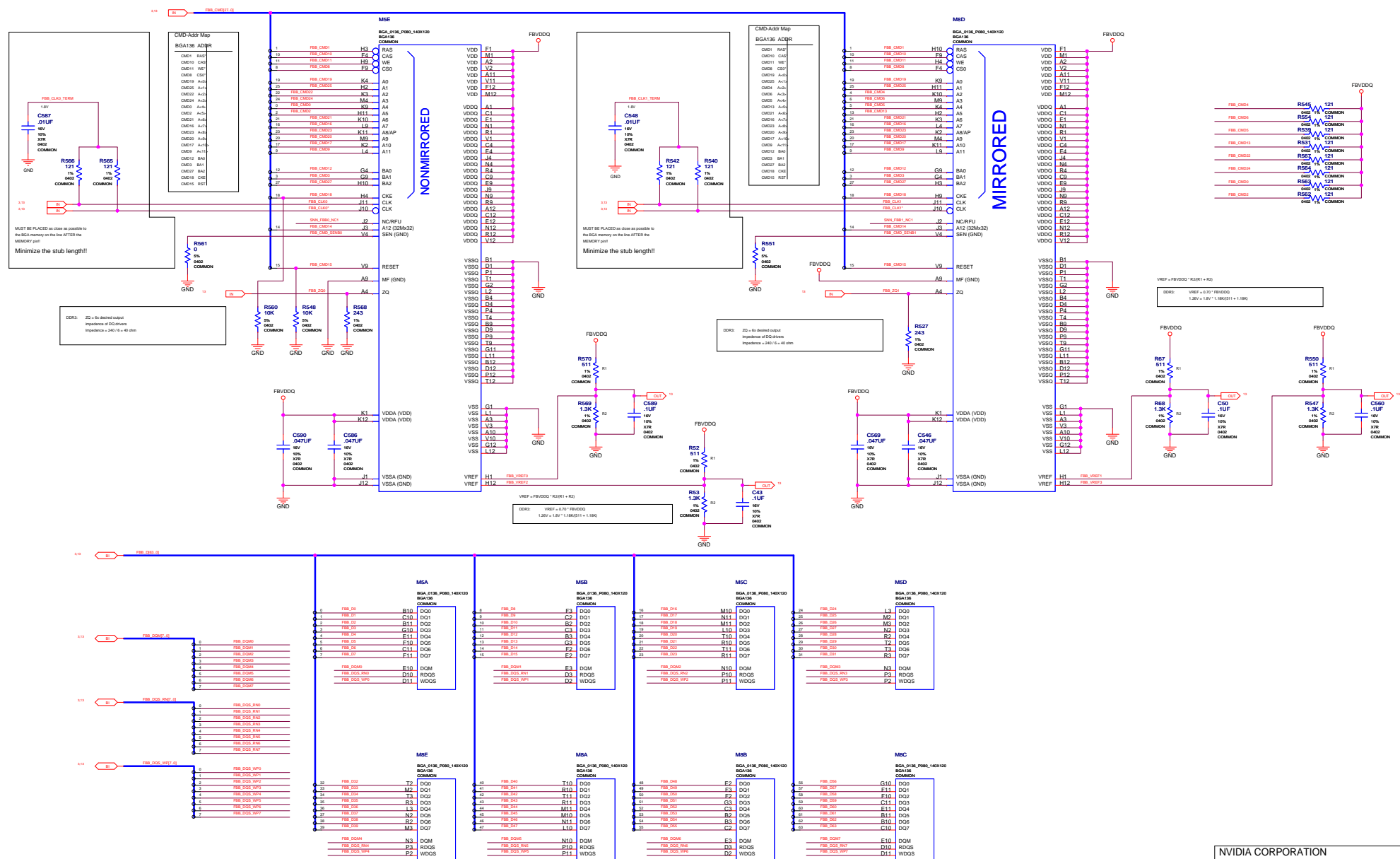




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PAGE DETAIL	FBA Partition Decoupling

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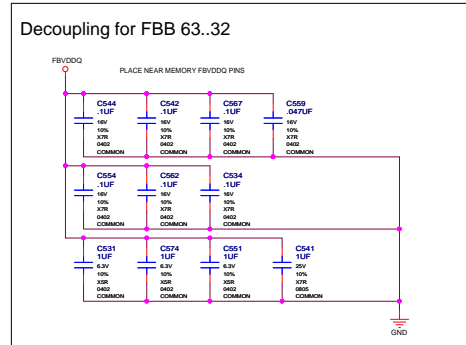


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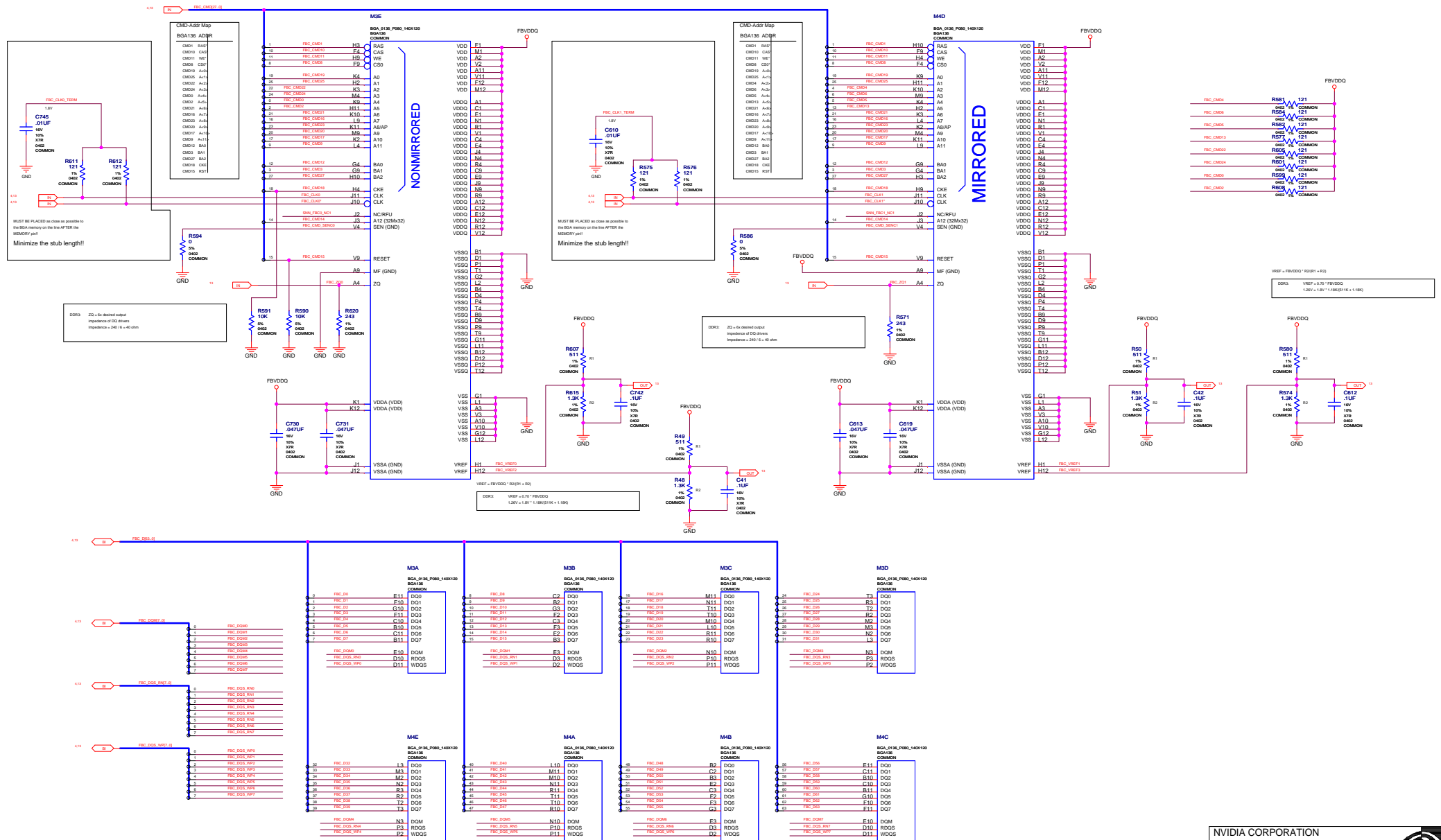


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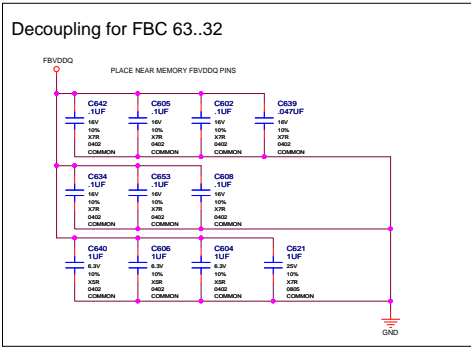
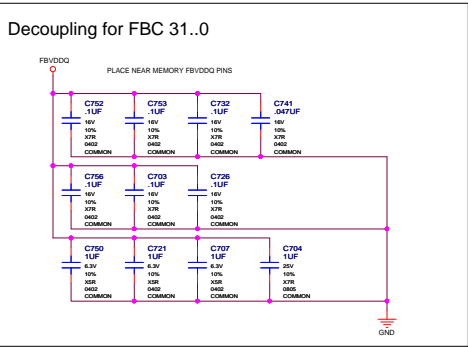


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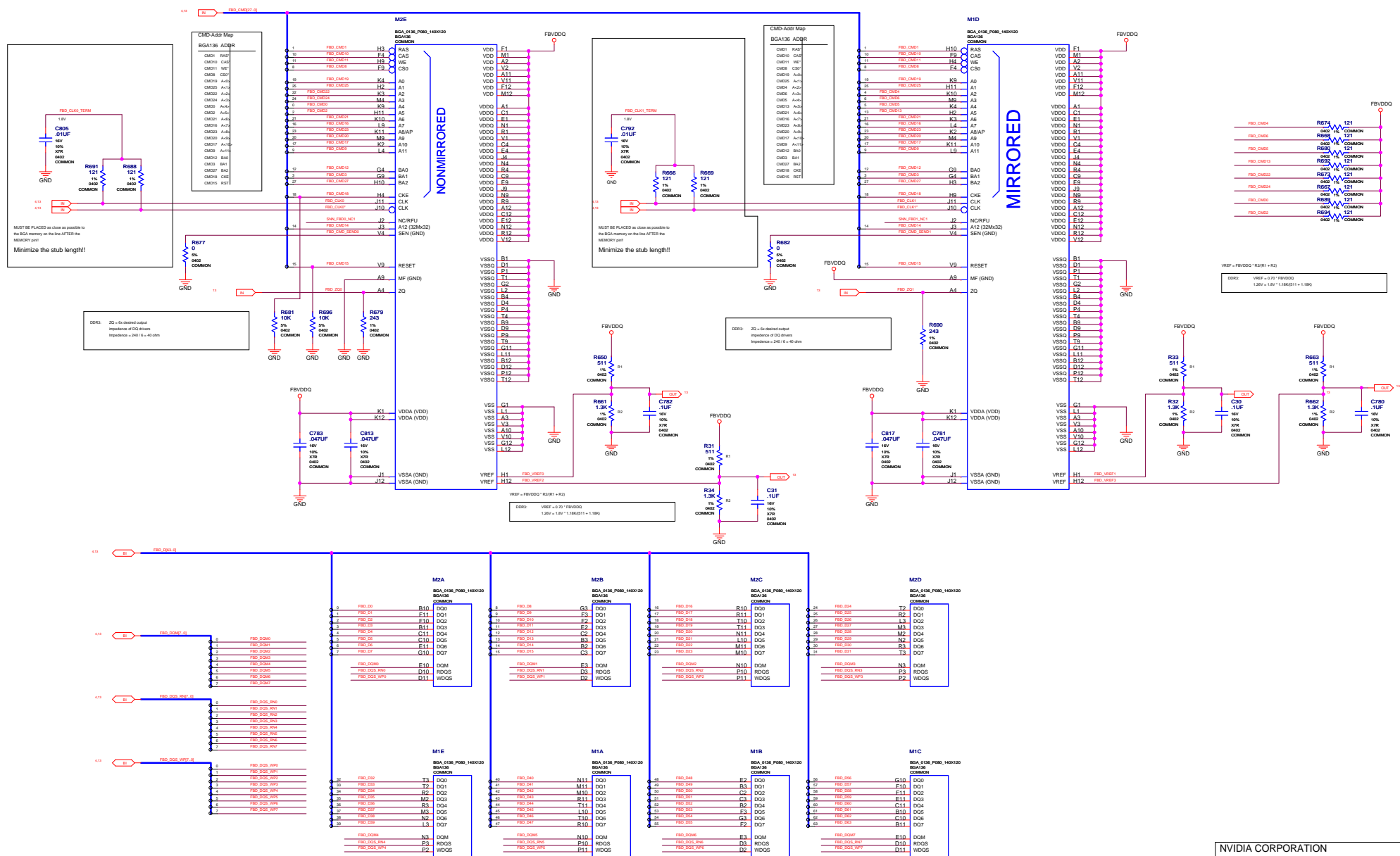
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PAGE DETAIL	FBC Partition Decoupling

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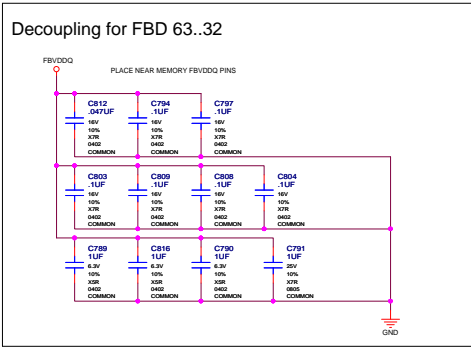
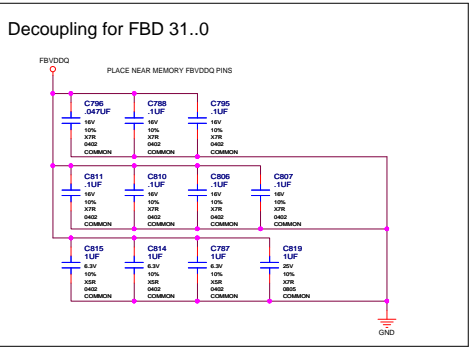


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PAGE DETAIL	FBD Partition

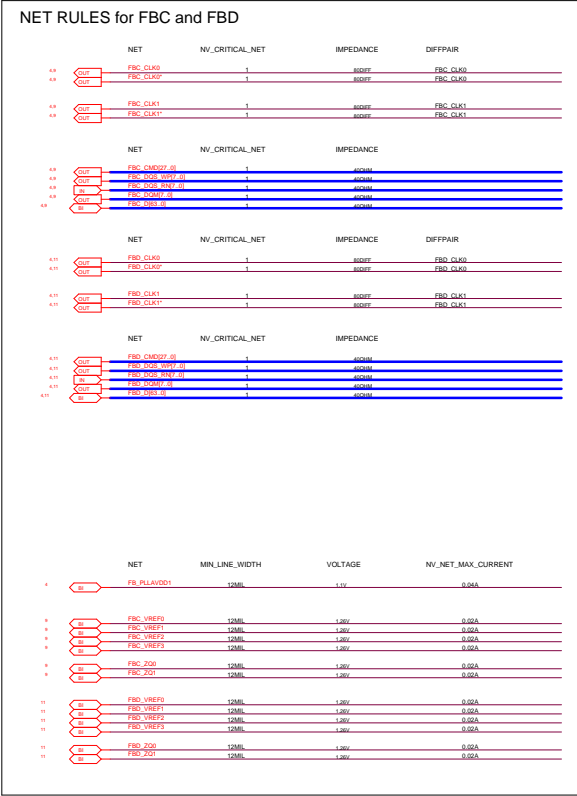
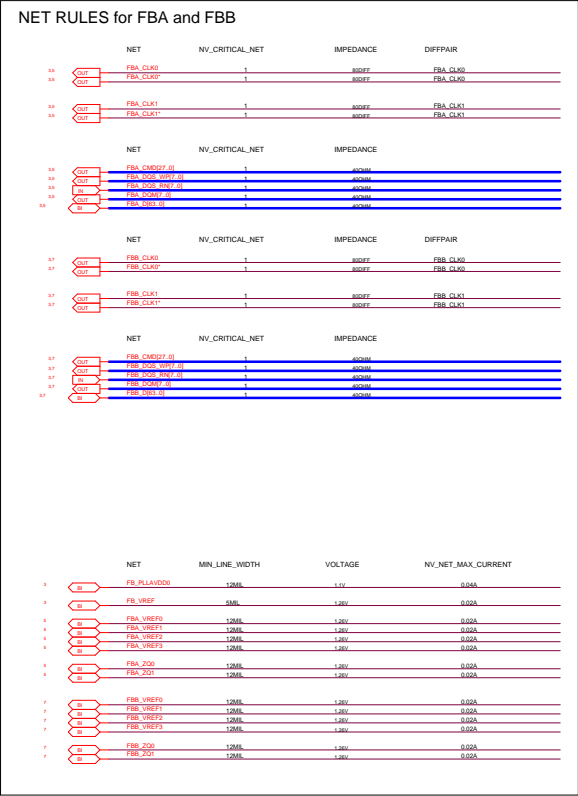


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PAGE DETAIL	FB Net Properties

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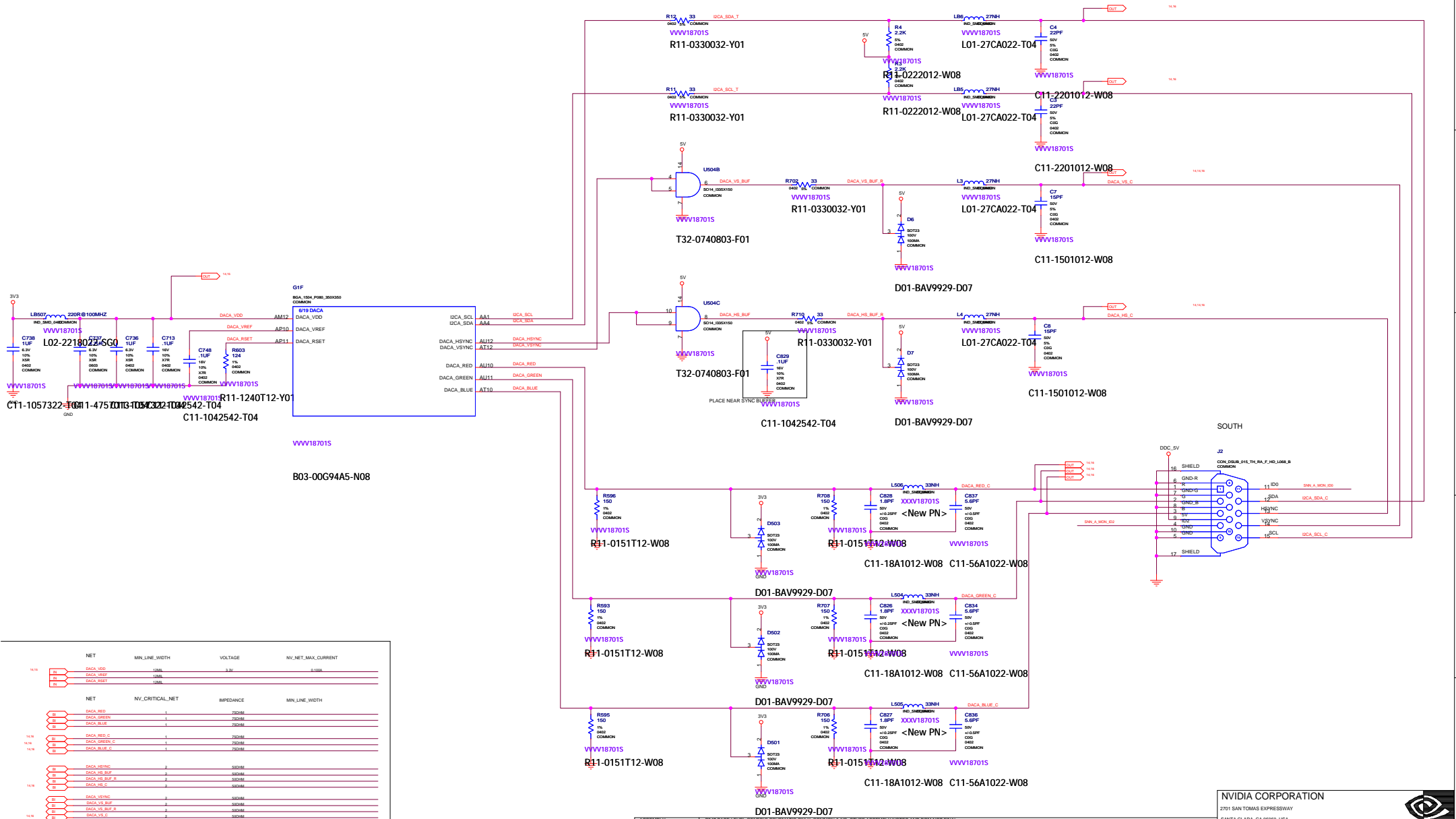
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DACA RGB-FILTER



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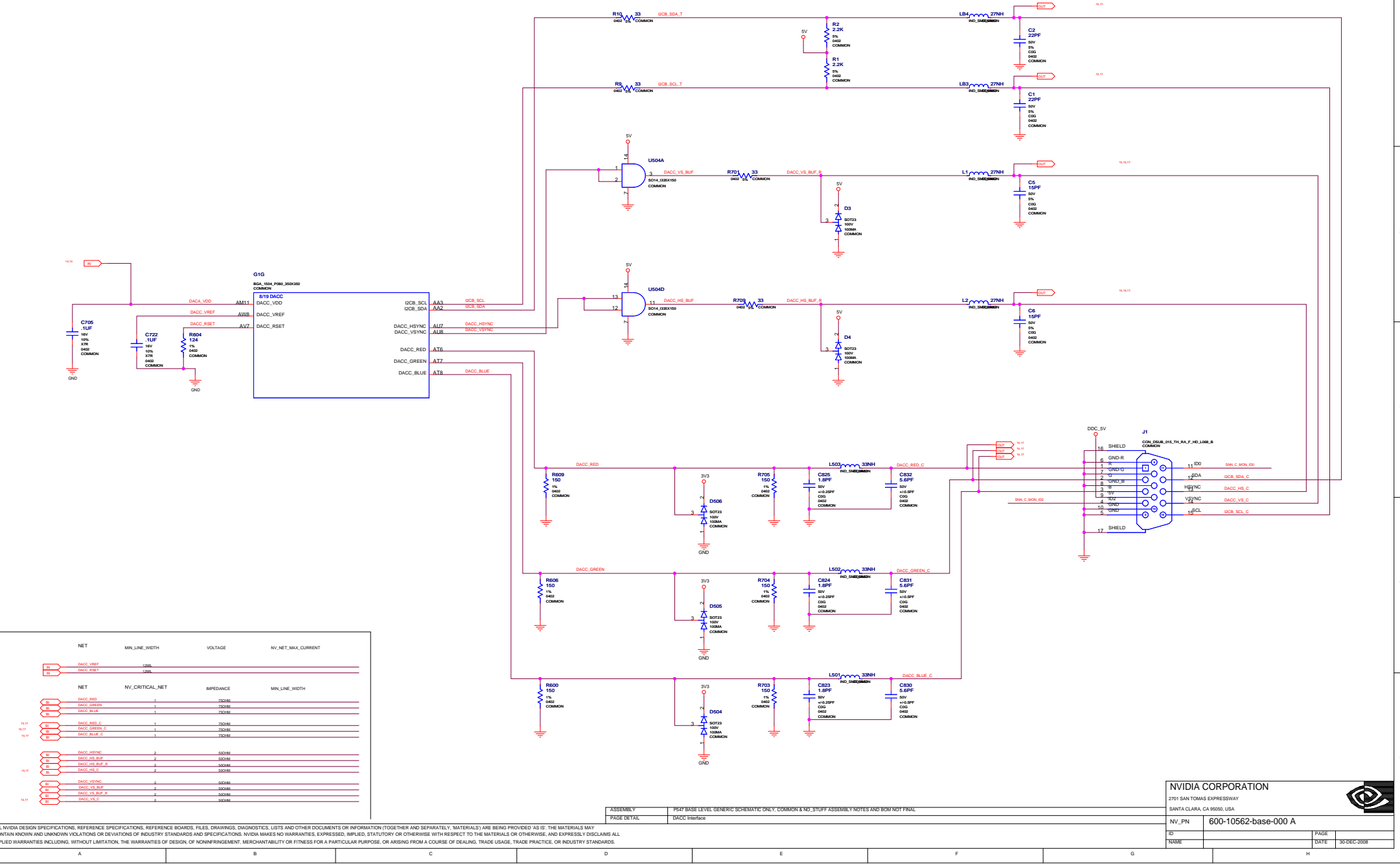
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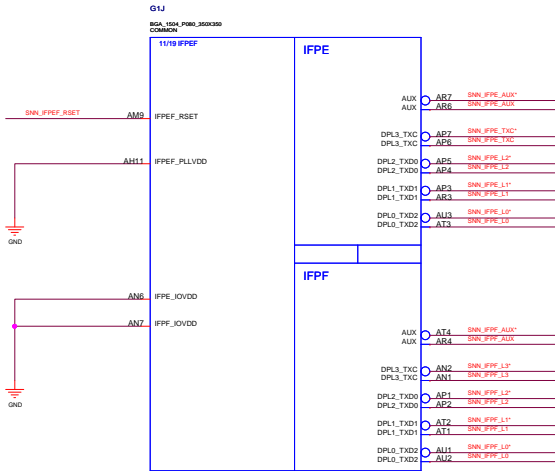
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ASSEMBLY P547 BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 31UPF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL DACA Interface

DACC RGB-FILTER





NET	MIN_LINE_WIDTH	VOLTAGE	IV_NET_MAX_CURRENT


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ASSEMBLY	PG47 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP E/F Interface - Unisys

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ASSEMBLY	PG17 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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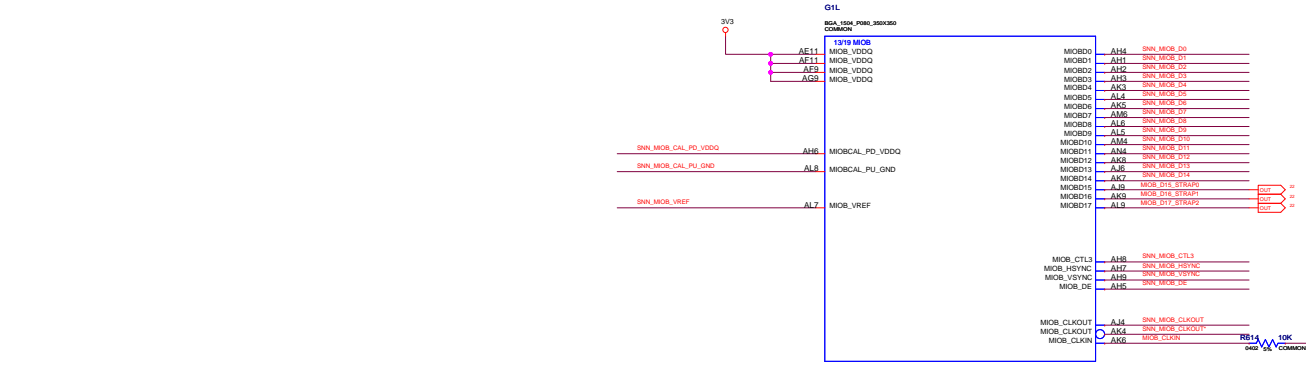
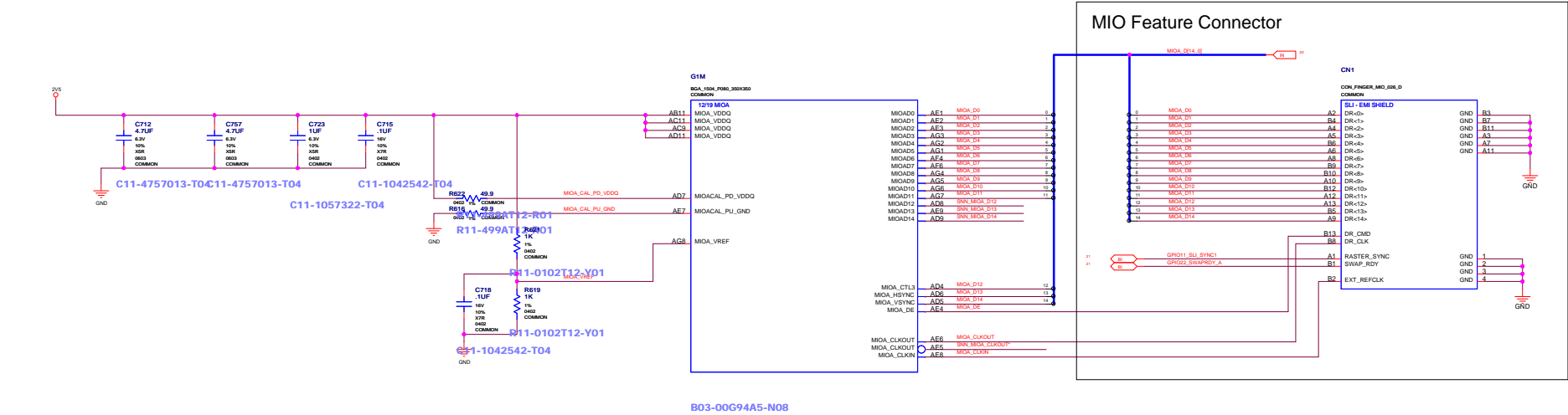
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B3	MIOA_D14_0	1	500mV
B3	MIOA_CLKIN	1	500mV
B3	MIOA_CLKOUT	1	500mV
B3	MIOA_DE	1	500mV
NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
B3	MIOA_VREF	2MIL	1.6V
B3	MIOA_CAL_PD_VDDO	12MIL	2.5V
B3	MIOA_CAL_PD_GND	12MIL	0.5V

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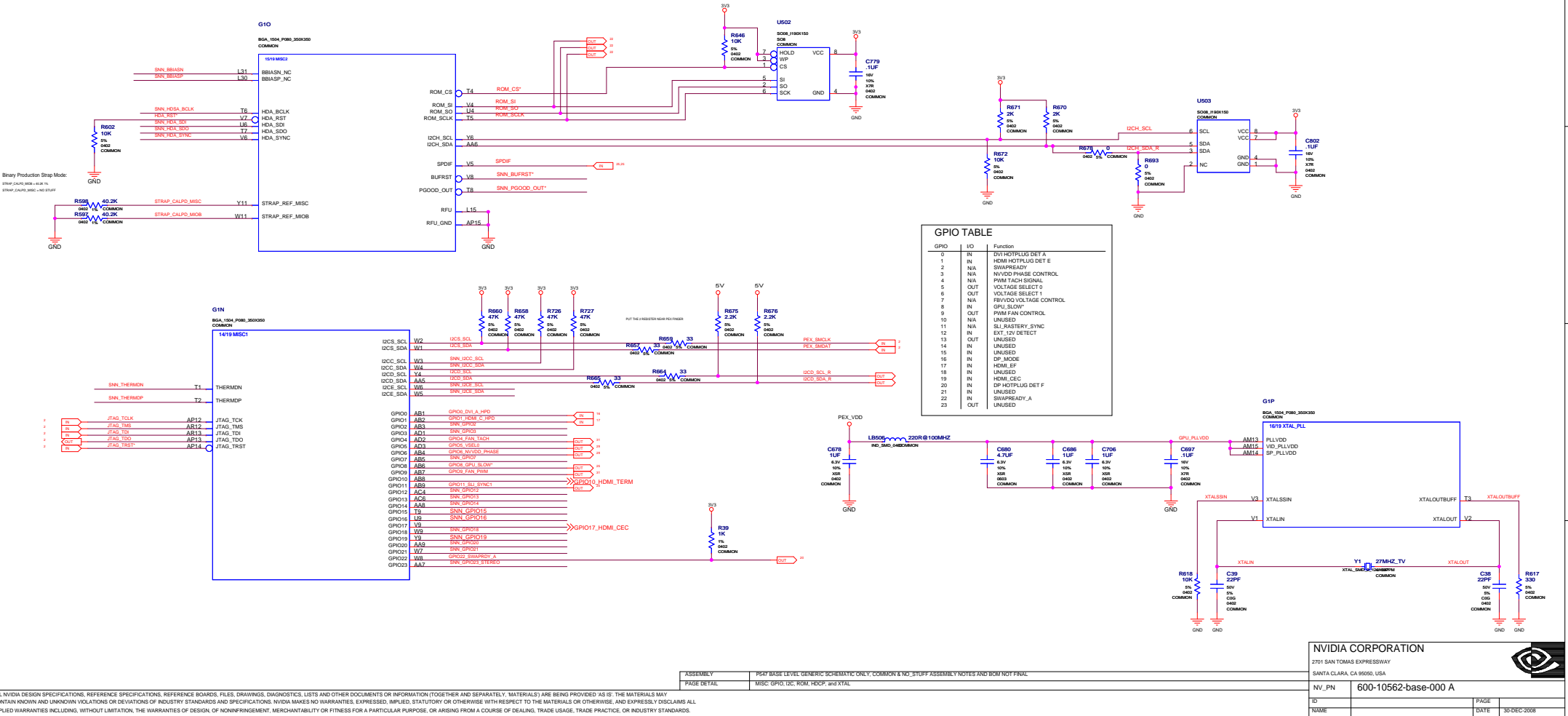
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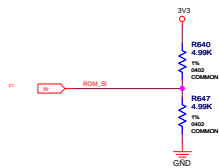
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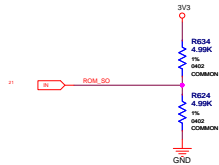


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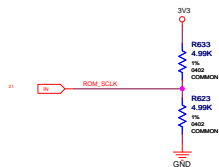


STRAP PIN	STRAP NAME
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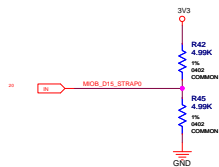
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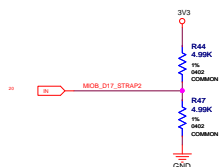
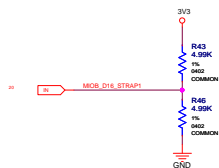
STRAP PIN	STRAP NAME
ROM_SO	SLOT_CLK_CFG



STRAP PIN	STRAP NAME
ROM_SCLK	PCI_DEVID[3]



STRAP PIN	STRAP NAME	
STRAP0	RAMCFG0	
STRAP1	RAMCFG1	<div><div>* RAMCFG[2:0]</div><div>256MB (8Mx32)<div>101 --- 256-bit Qimonda 110 --- 256-bit Hynix 111 --- 256-bit Samsung</div></div><div>512MB (16Mx32)<div>001 --- 256-bit Qimonda 010 --- 256-bit Hynix 011 --- 256-bit Samsung</div></div><div>1024MB (32Mx32)<div>101 --- 256-bit Hynix 110 --- 256-bit Hynix 111 --- 256-bit Samsung</div></div></div>
STRAP2	RAMCFG2	



GPIO	GPIO
GPIO1	GPIO1
GPIO2	GPIO2
GPIO3	GPIO3
GPIO4	GPIO4
GPIO5	GPIO5
GPIO6	GPIO6
GPIO7	GPIO7
GPIO8	GPIO8
GPIO9	GPIO9
GPIO10	GPIO10
GPIO11	GPIO11
GPIO12	GPIO12
GPIO13	GPIO13
GPIO14	GPIO14
GPIO15	GPIO15
GPIO16	GPIO16
GPIO17	GPIO17
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GPIO19	GPIO19
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GPIO26	GPIO26
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GPIO98	GPIO98
GPIO99	GPIO99

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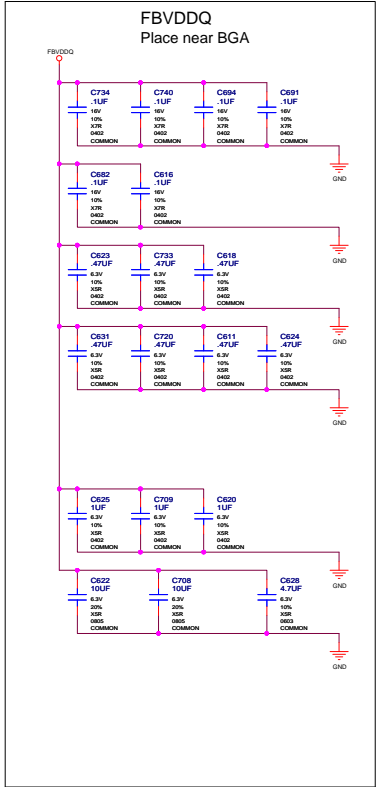
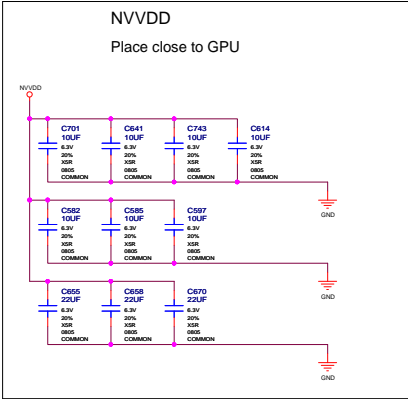
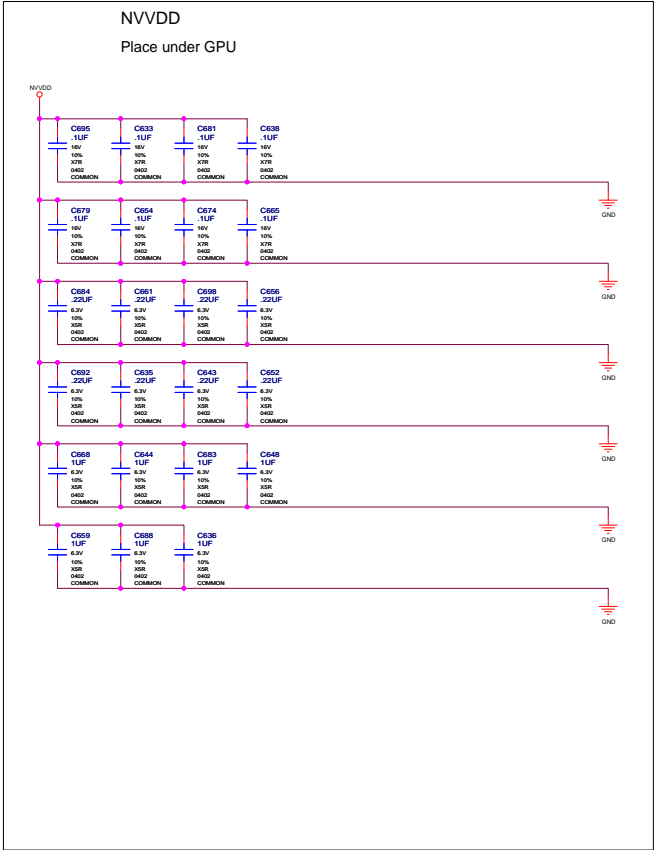
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ASSEMBLY	PG47 BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	NVVDD and FBVDDQ Decoupling

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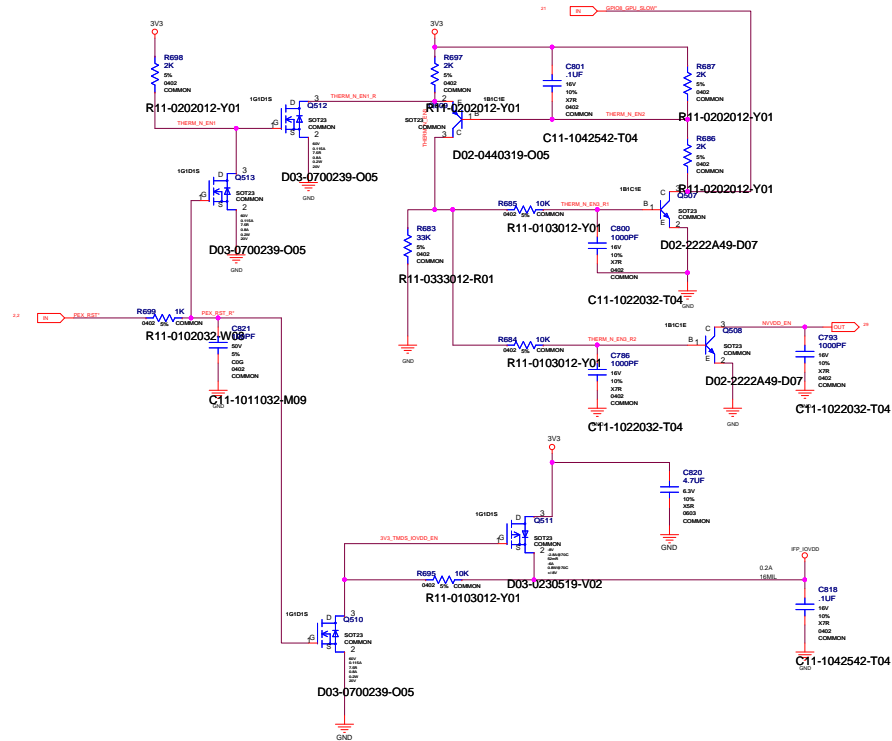
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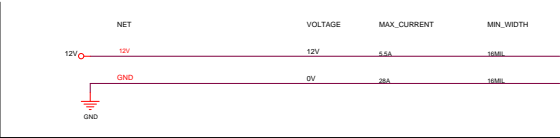
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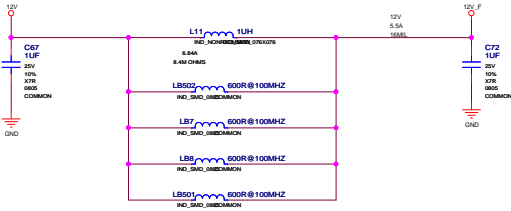
IFP_IOVDD Backdrive Prevention

[illegible]



12V Power Supply Filter

12V_F = 12V @ 5.5A




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ASSEMBLY	PSI7 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS I: 3V3, 12V, and 12V_EXT Power Supply Filter

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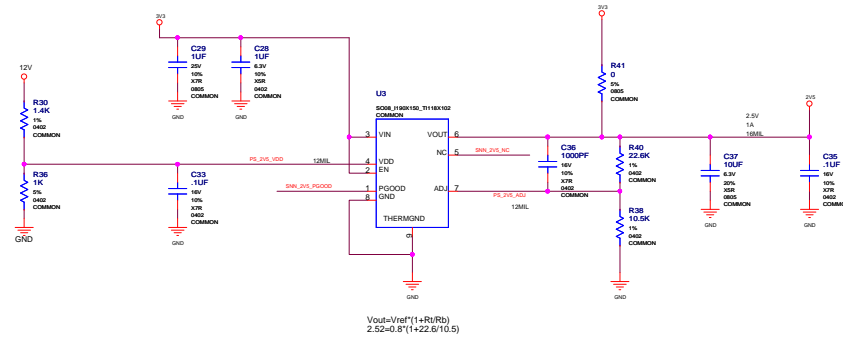
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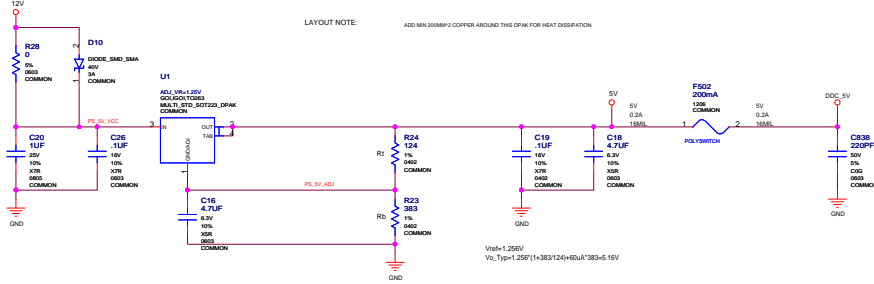
2V5 Power Supply



5V and DDC_5V Power Supply

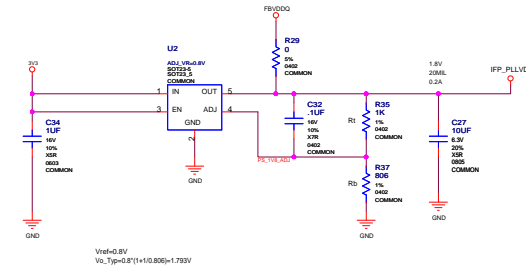
DDC_5V = 5V @ 200mA

LAYOUT NOTE: ADD 1MM 200MM² COPPER AROUND THIS DPAK FOR HEAT DISSIPATION



IFP_PLLVDD Power Supply

IFP_PLLVDD = 1.8V @ 200mA



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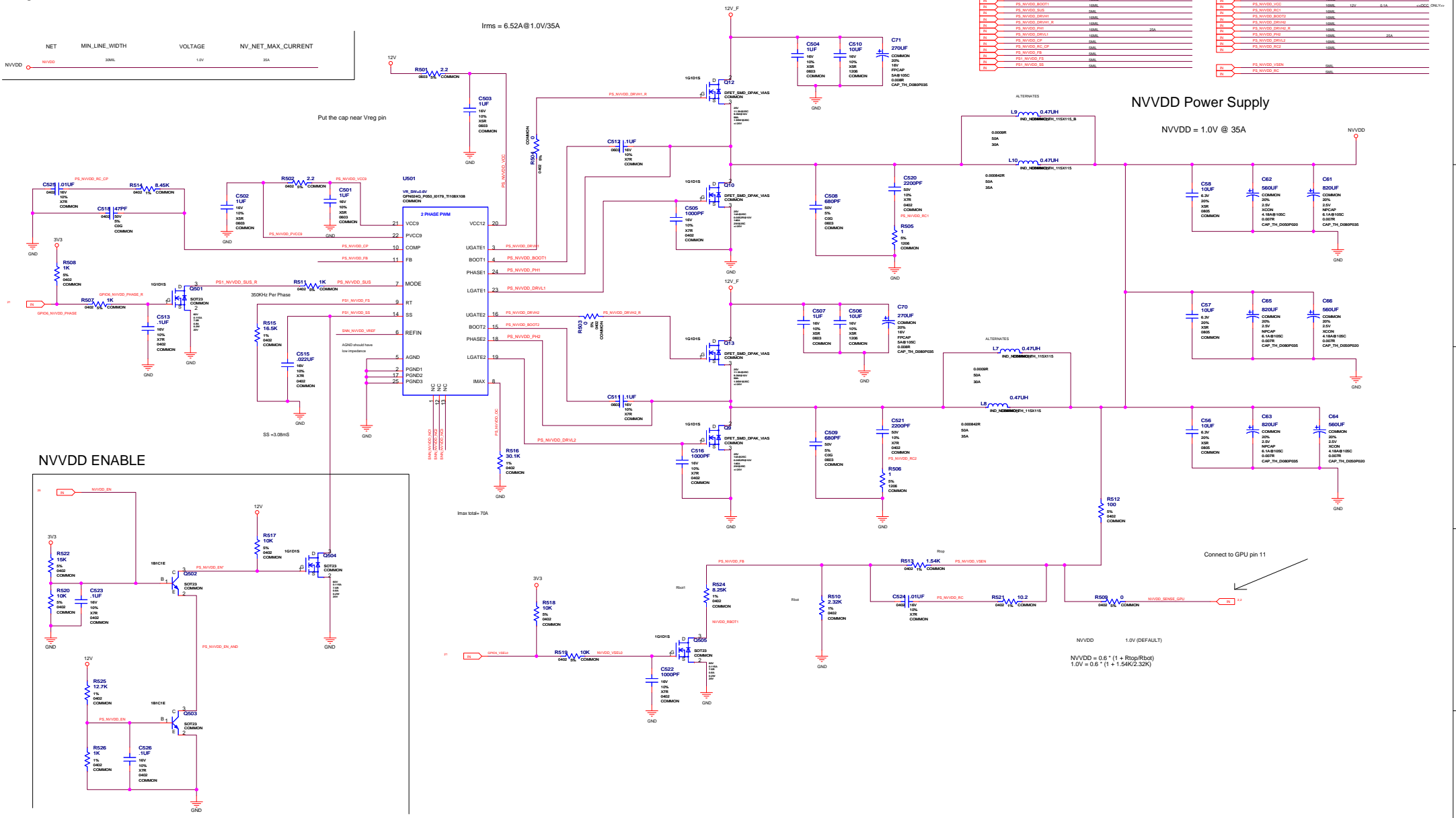


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ASSEMBLY	PSII BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO 3V/5V ASSEMBLY NOTES AND BOM NOT FINAL
PAGE/DETAIL	PS II: IFP_PLLVDD, 2V5, 5V, and DDC_5V Power Supply



ASSEMBLY	PS47 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS IV: NVVDDV

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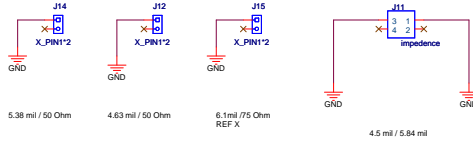
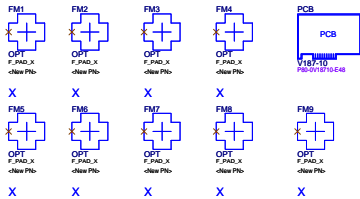
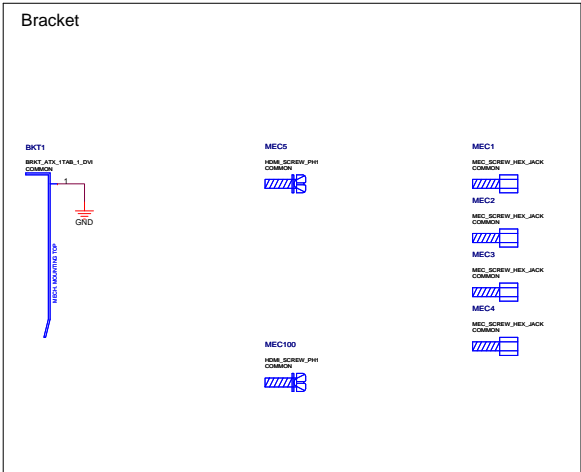
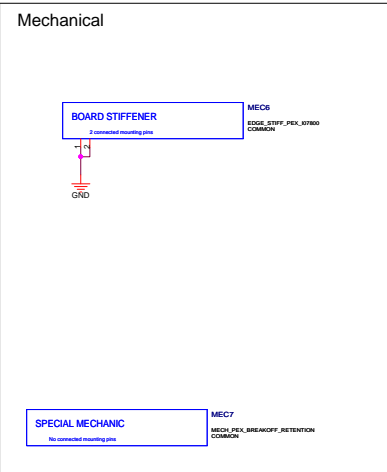
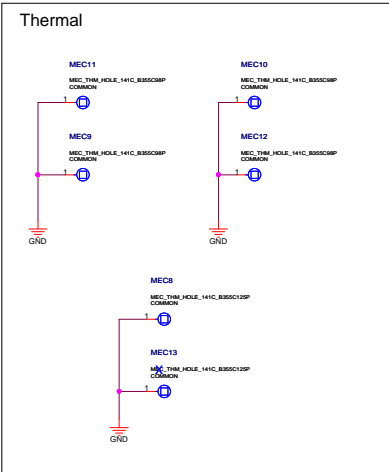


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PAGE DETAIL	Thermal, Mechanical, and Bracket

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A		B		C		D		E		F		G		H	
Title: Netlistpage Report Design: j9562_400 Date: Dec 24 11:53:24 2008		PEX_RK14* 2:30> 2:58 PEX_RK14* 2:30> 2:58 PEX_RK15 2:30> 2:58 PEX_RK15P 2:30> 2:58 PEX_RK15P 2:30> 2:58 PEX_SMD07 2:10> 21:2E< GPU_TESTMODE 2:5D 2:5G> GPU_TESTMODE 2:5D 2:5G> JTAD_TCLK 2:1F> 2:1F> 21:3A< JTAD_TCLK 2:1F> 2:1F> 21:3A< JTAD_TDI 2:1F> 2:1F> 21:3A< JTAD_TDI 2:1F> 2:1F> 21:3A< JTAD_TDO 2:1F> 2:1F> 21:3A< JTAD_TDO 2:1F> 2:1F> 21:3A< JTAD_TMS 2:1F> 2:1F> 21:3A< JTAD_TMS 2:1F> 2:1F> 21:3A< JTAD_TBST1 2:1F> 2:1F> 21:3A< JTAD_TBST1 2:1F> 2:1F> 21:3A< NVIO0_BSENSE_GPU 2:4E> 2:5G> 29:4G> NVIO0_BSENSE_GPU 2:4E> 2:5G> 29:4G> PEX_CAL_PU_VDDQ 2:5D PEX_CAL_PU_GND 2:5D PEX_PLVUD0 2:4D 2:5G> PEX_PLVUD0 2:4D 2:5G> PEX_PUL_CLK_OUT1 2:4D 2:4G> PEX_PUL_CLK_OUT1 2:4D 2:4G> PEX_PUL_CLK_OUT2 2:4D 2:4G> PEX_PUL_CLK_OUT2 2:4D 2:4G> PEX_PSRBT1 2:1A 2:2 4A 2:4G> PEX_PSRBT1 2:1A 2:2 4A 2:4G> PEX_PSRBT1 2:1A 2:2 4A 2:4G> PEX_PSRBT1 2:1A 2:2 4A 2:4G> PEX_REFCLK 2:10> 2:28 													

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