P2002

2GB GDDR5, 256b, 64Mx32

Stacked DVI-I/DVI-D + HDMI + DP

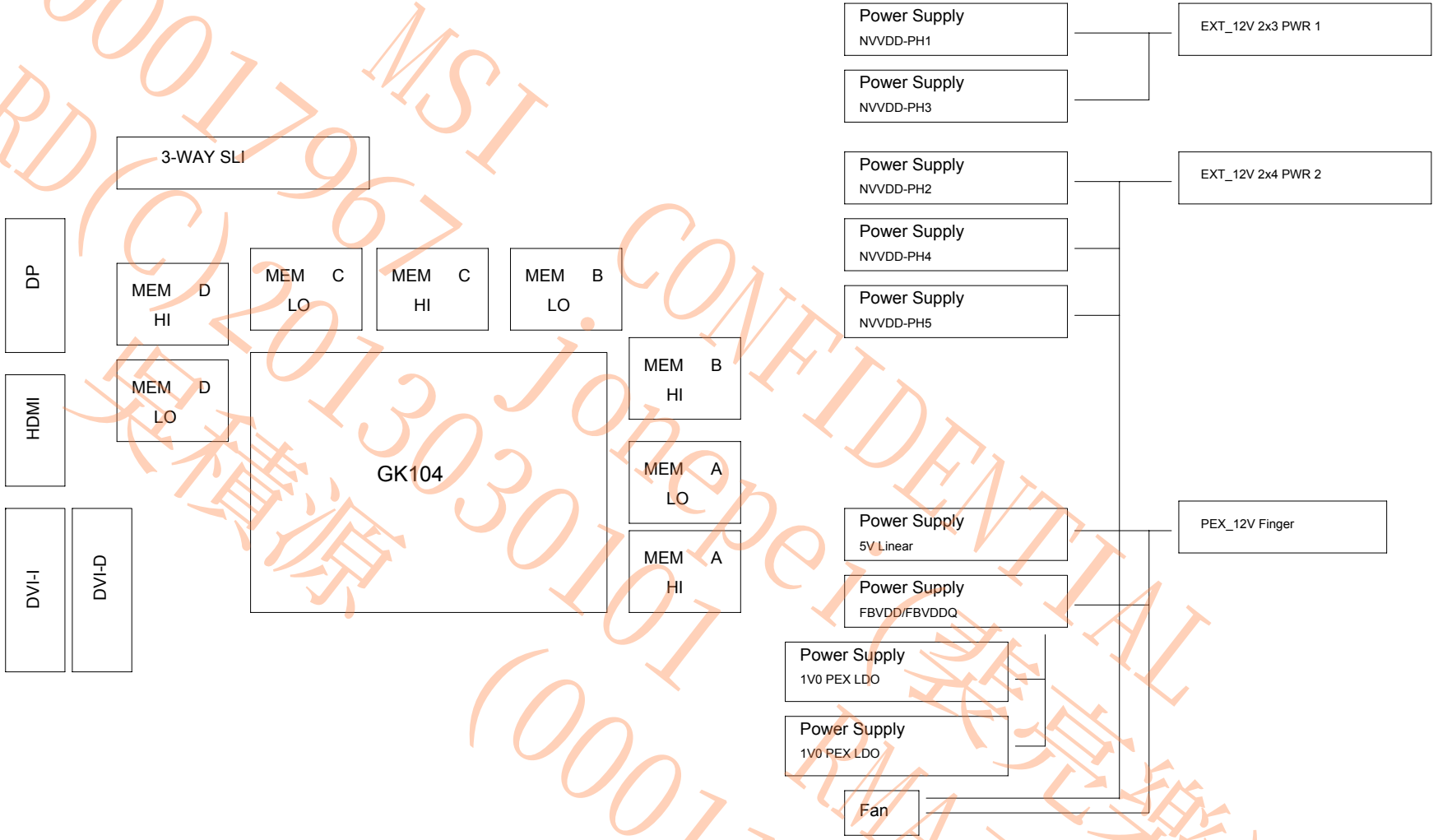
TABLE OF CONTENTS

2012/02/17 MS-V283-1.0 changed list

Page	Description
3	1.Add 12V_Bus Fuse
17	1. Modify DUAL STACK DVI library
18	1. Modify DUAL STACK DVI library 2. IFPEF_IOVDD change to PEX_VDD
19	1. Modify HDMI library 2. IFPCD_IOVDD change to PEX_VDD
20	1. Modify DP library
22	1. Add Thermal IC circuit 2. Add I2CB to 8318 / 7718 / 6262 3. Remove GPIO19/GPIO20
23	1. Add Dual BIOS circuit
24	1. Modify U2 footprint 2. PEX_VDD change to 1-phase PWM
25	1. FBVDD used UPI/1612
26	1. NVVDD used CHIL/8318
27/28	1. Driver IC used IR/3598 2. MOS used IRF8327 / 8304 3. Choke used Trio R17 (Golden)
30	1. Remove U502 INA3221 circuit 2. Modify 12V/PEX_12V current sensor IC circuit
32	1. Remove GeForce Logo LED circuit

MICRO-STAR INT'L CO.,LTD
MS-V283
Size: Custom | Document Description: Table of Contents | Rev: 1.0
Date: Friday, April 20, 2012 | Sheet 1 of 33

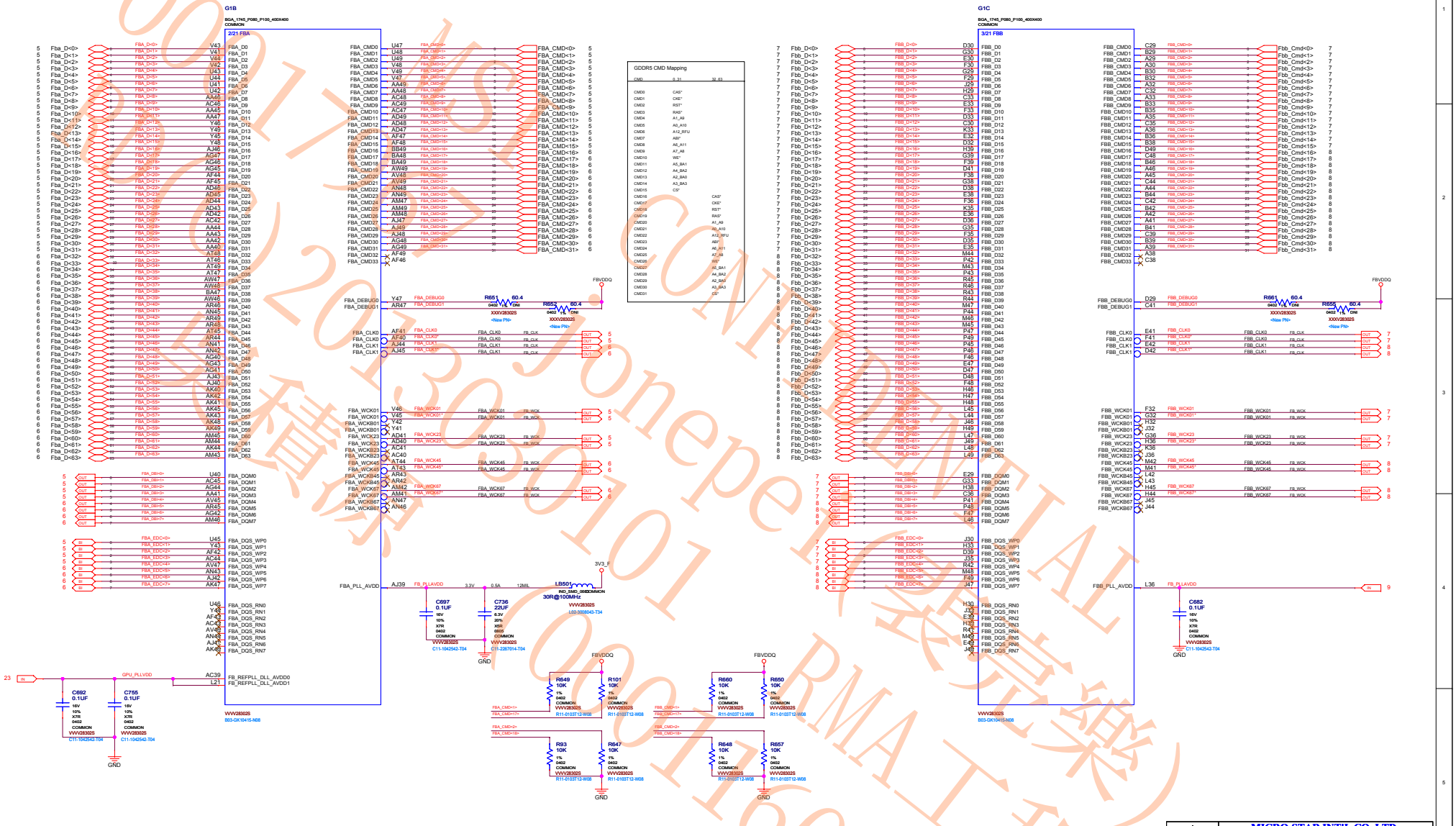
Page2: Block Diagram



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V283	
Size: Custom	Document Description: Block Diagram	Rev: 1.0
Date: Friday, April 20, 2012	Sheet 2 of 33	

Page3: PCI Express

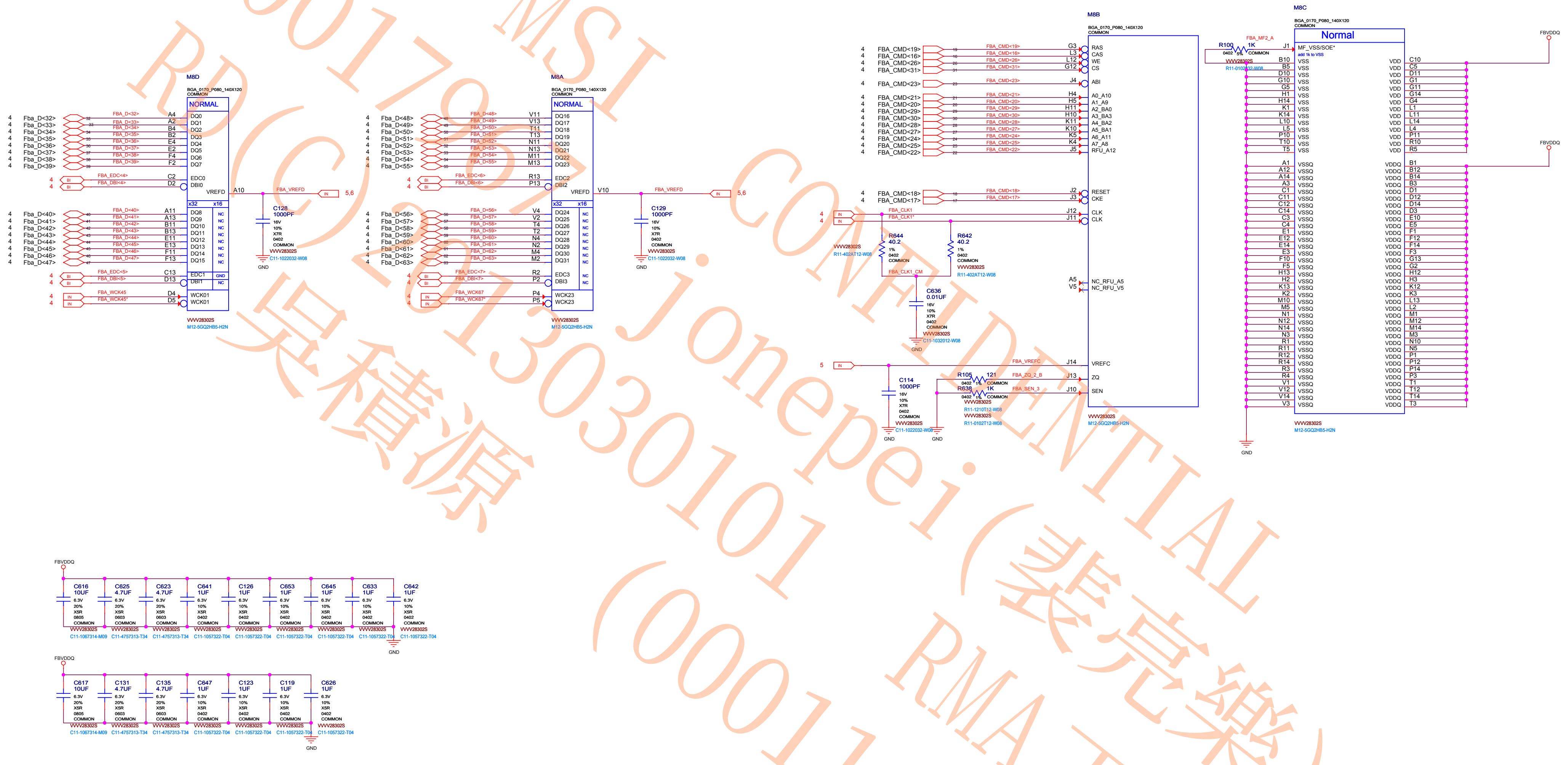
Page4: MEMORY: GPU Partition A/B



Page5: MEMORY: FBA Partition 31..0

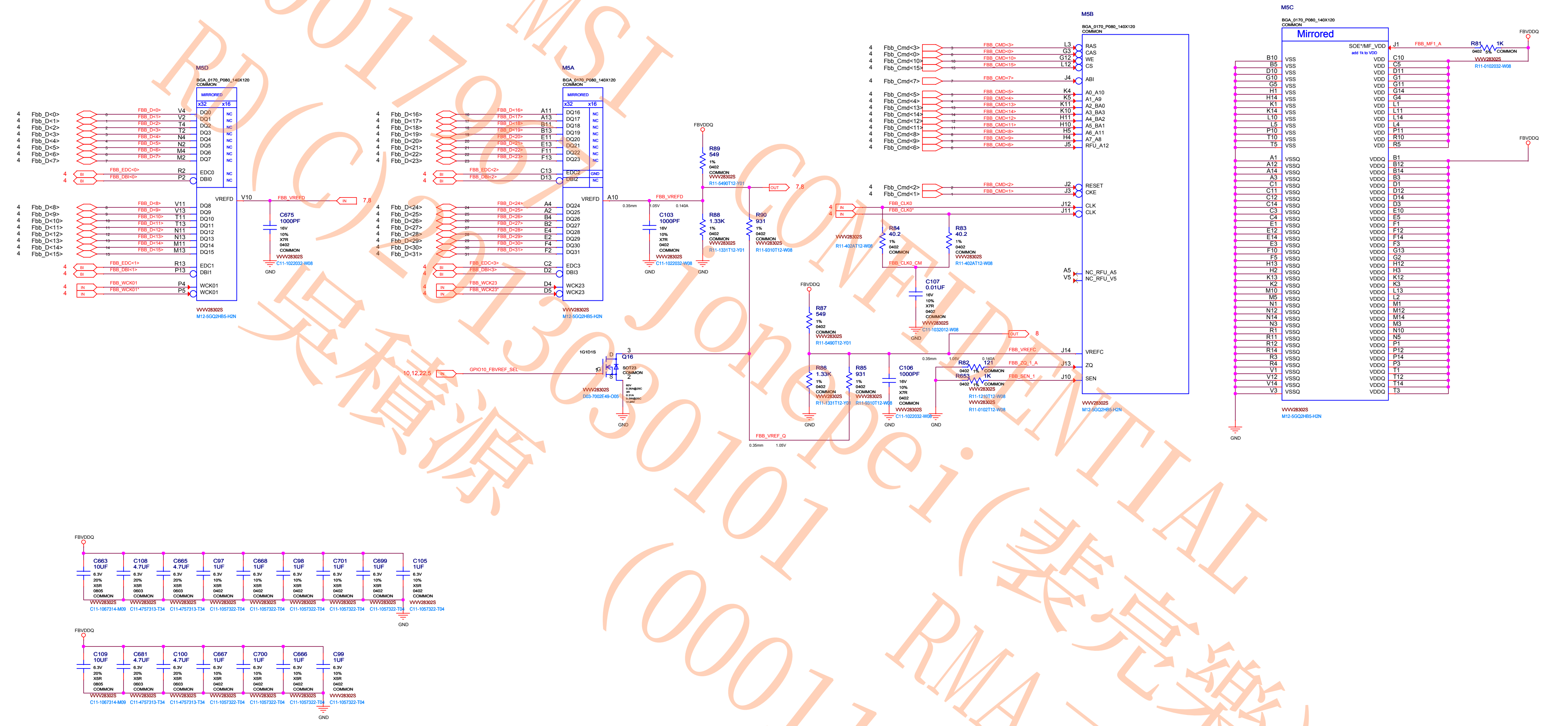
MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size: Custom	Document Description: MEMORY_ FBA[31_0]	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 5 of 33	

Page6: MEMORY: FBA Partition 63..32



MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size: Custom	Document Description: MEMORY_ FBA[63_32]	Rev 1.0
Date: Monday, April 23, 2012	Sheet 6 of 33	

Page7: MEMORY: FBB Partition 31..0



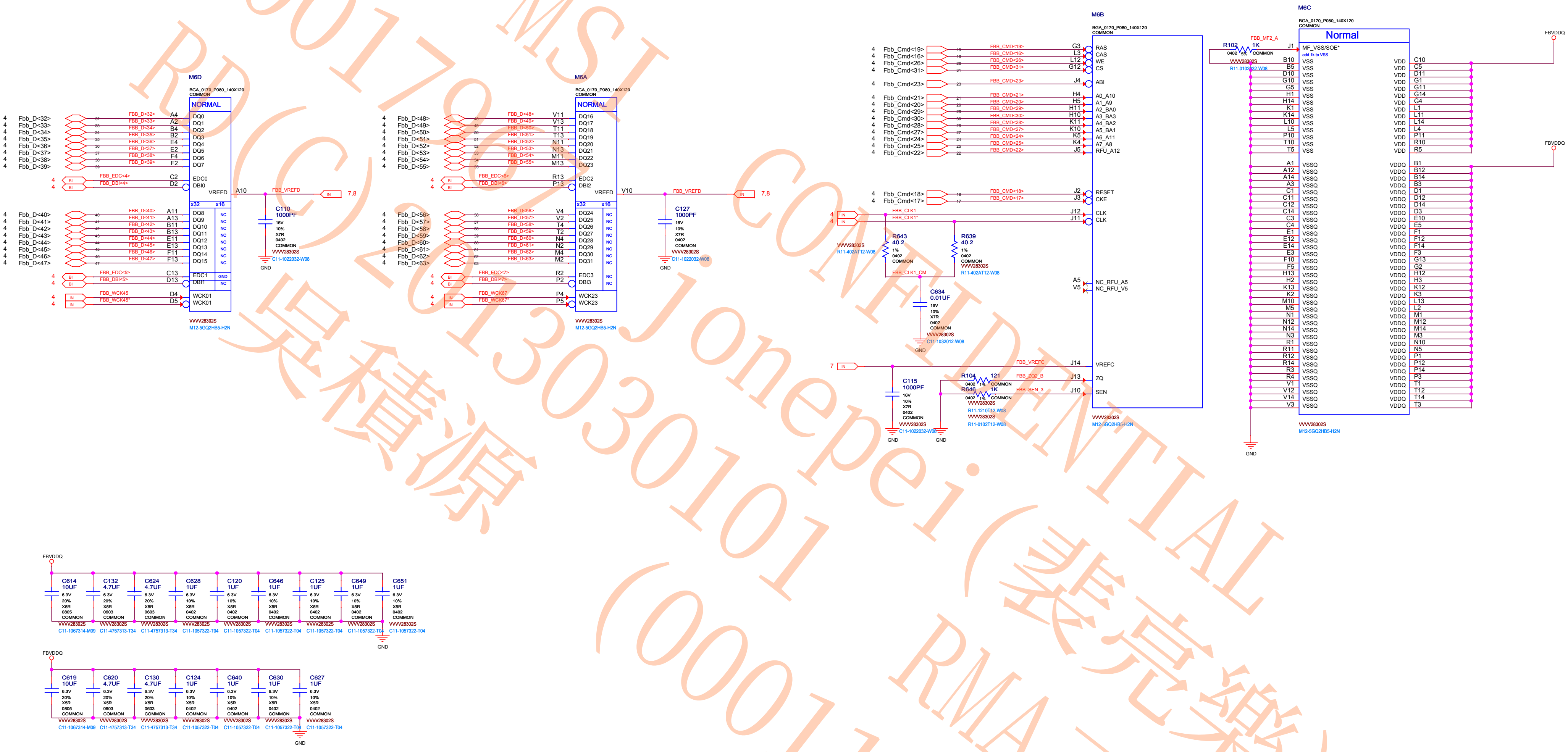
MICRO-STAR INT'L CO.,LTD

MS-V283

Size	Document Description	Rev
Custom	MEMORY_ FBB[31_0]	1.0

Date: Monday, April 23, 2012 Sheet 7 of 33

Page8: MEMORY: FBB Partition 63..32



MICRO-STAR INT'L CO.,LTD

MS-V283

Size: Custom

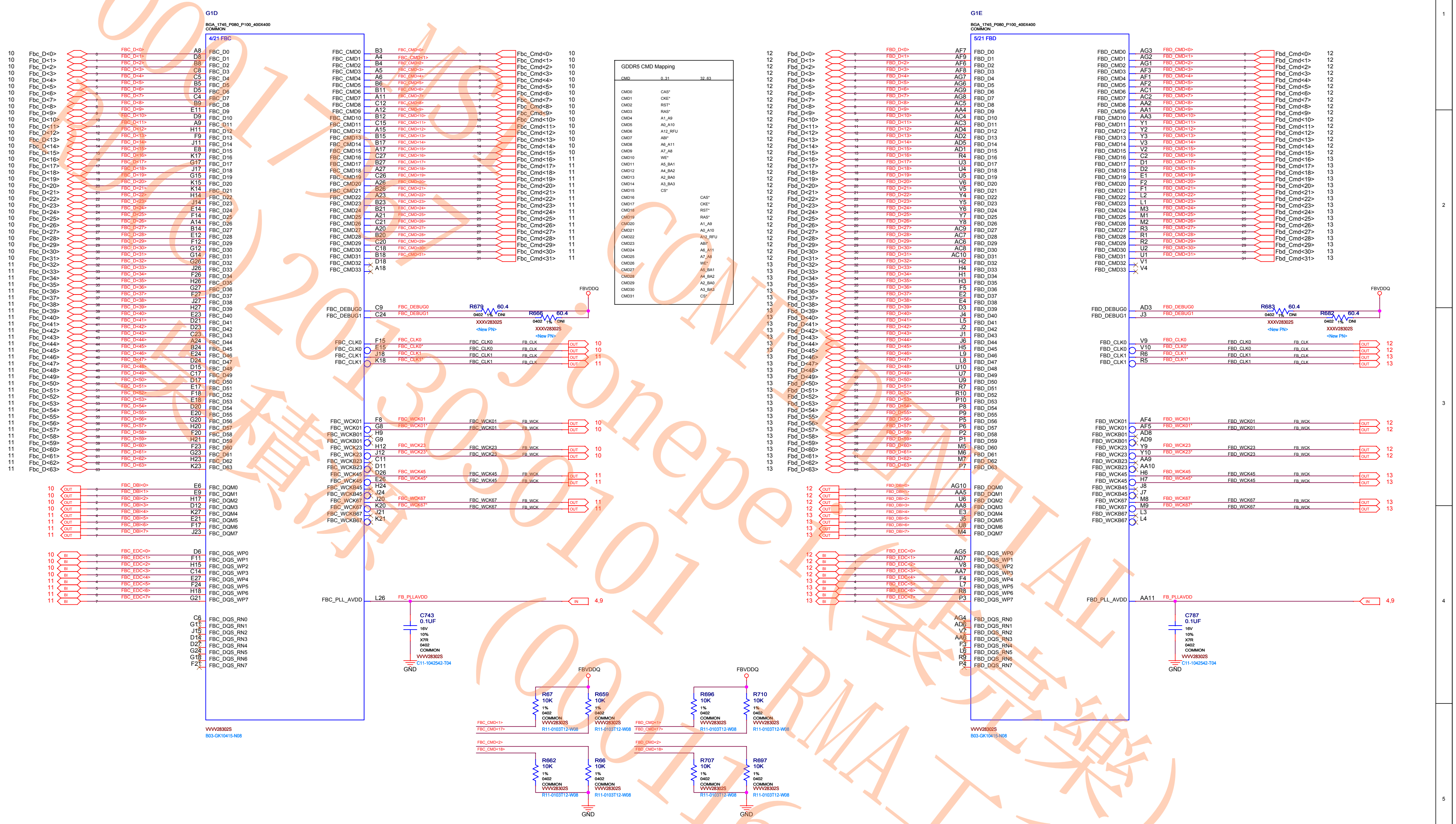
Document Description: MEMORY_ FBB[63_32]

Rev: 1.0

Date: Monday, April 23, 2012

Sheet 8 of 33

Page9: MEMORY: GPU Partition C/D



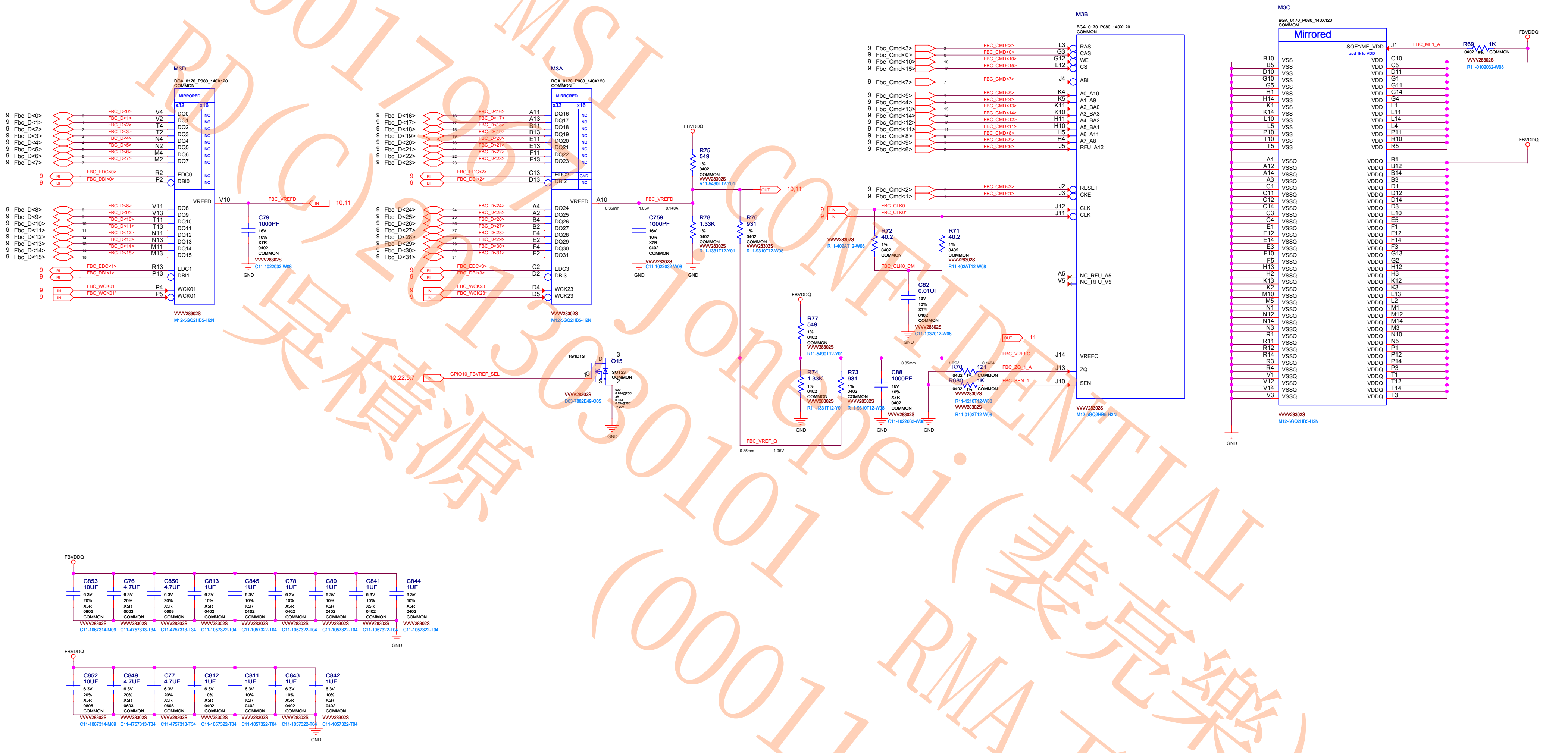
MICRO-STAR INT'L CO.,LTD

MS-V283

Size	Document Description	Rev
Custom	MEMORY_ GPU Partition C_D	1.0

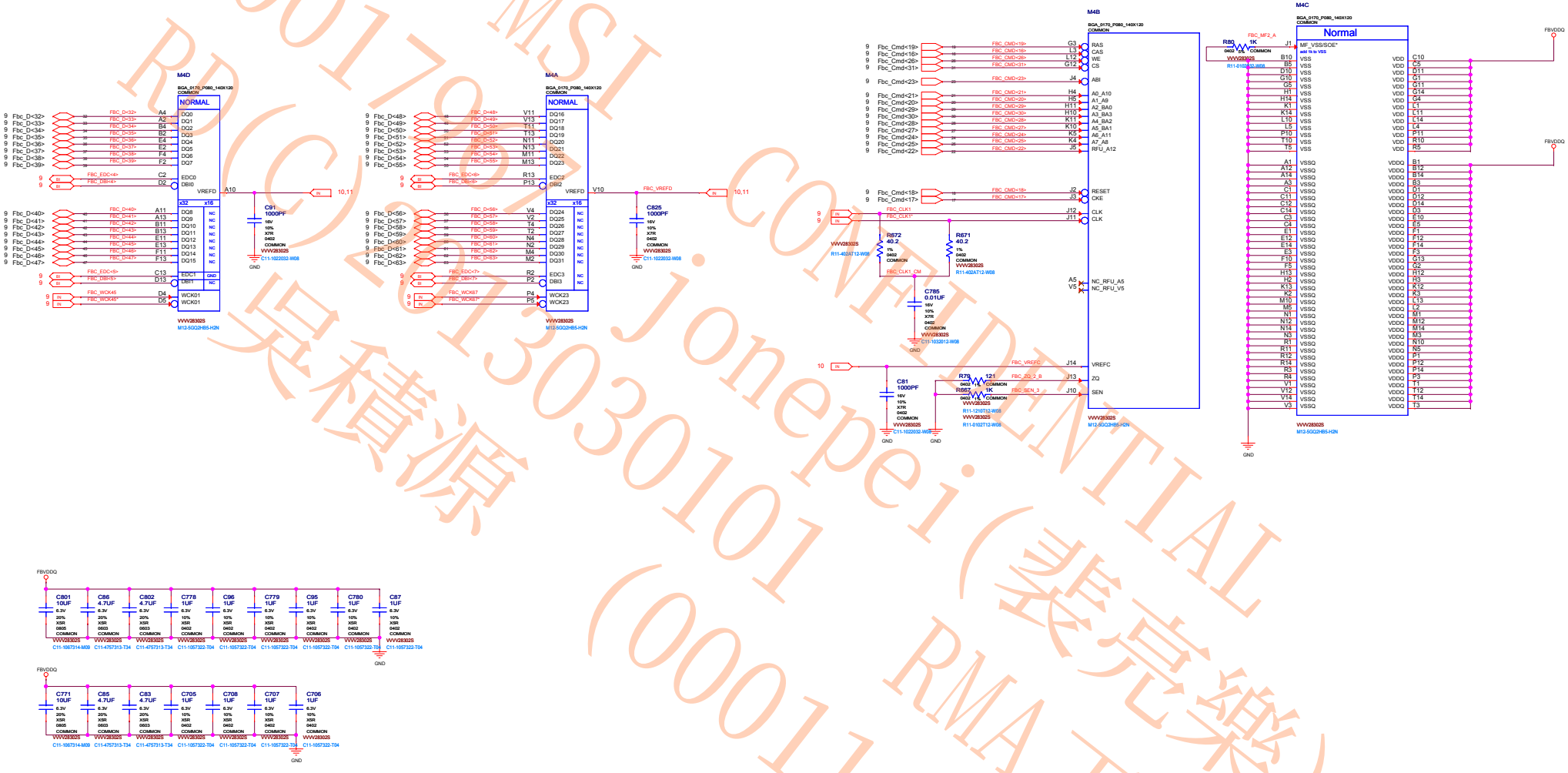
Date: Monday, April 23, 2012 Sheet 9 of 33

Page10: MEMORY: FBC Partition 31..0



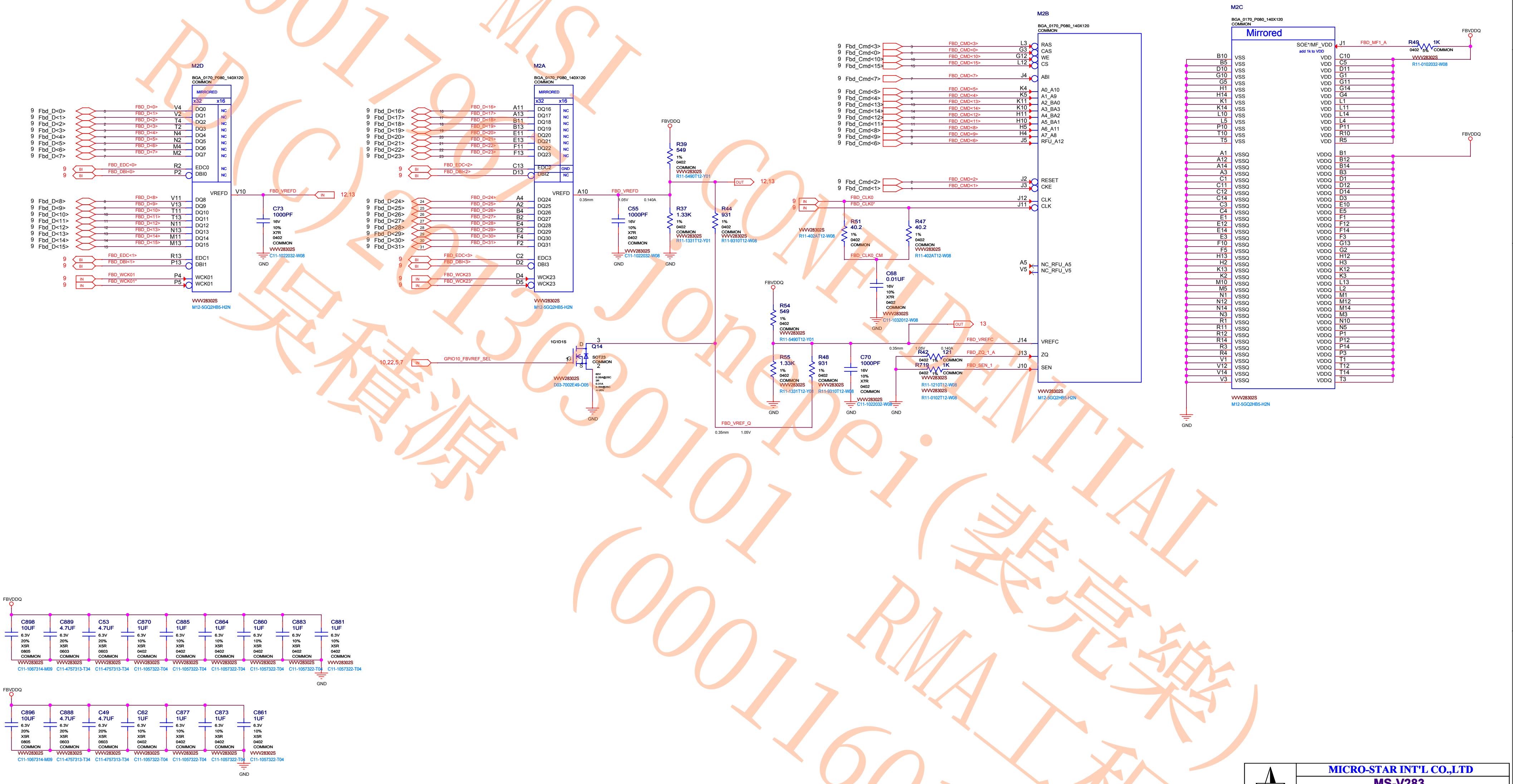
MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size: Custom	Document Description: MEMORY_ FBC[31_0]	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 10 of 33	

Page11: MEMORY: FBC Partition 63..32



MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size: Custom	Document Description: MEMORY_ FBC[63_32]	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 11 of 33	

Page12: MEMORY: FBD Partition 31..0



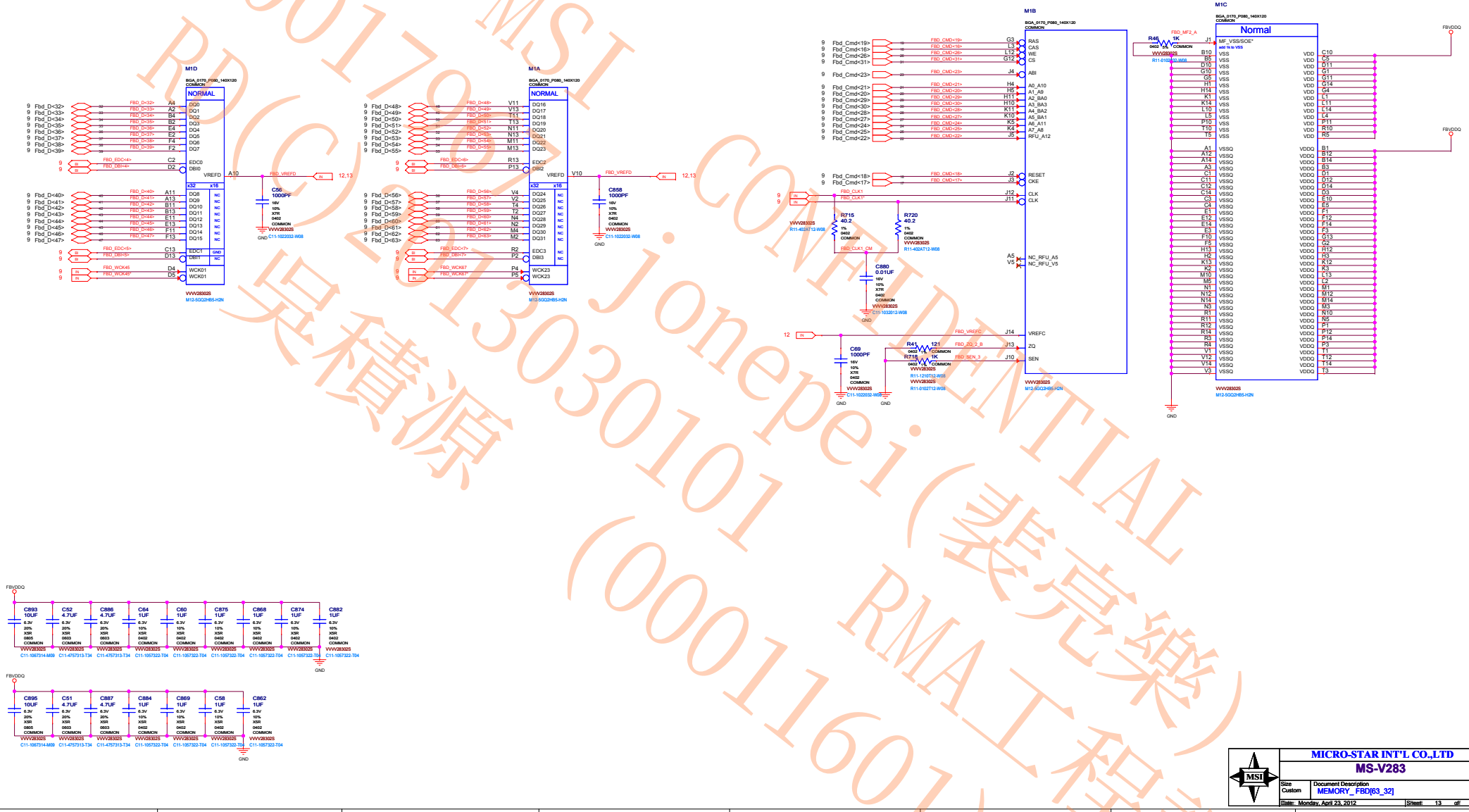
MICRO-STAR INT'L CO.,LTD

MS-V283

Size	Document Description	Rev
Custom	MEMORY_ FBD[31_0]	1.0

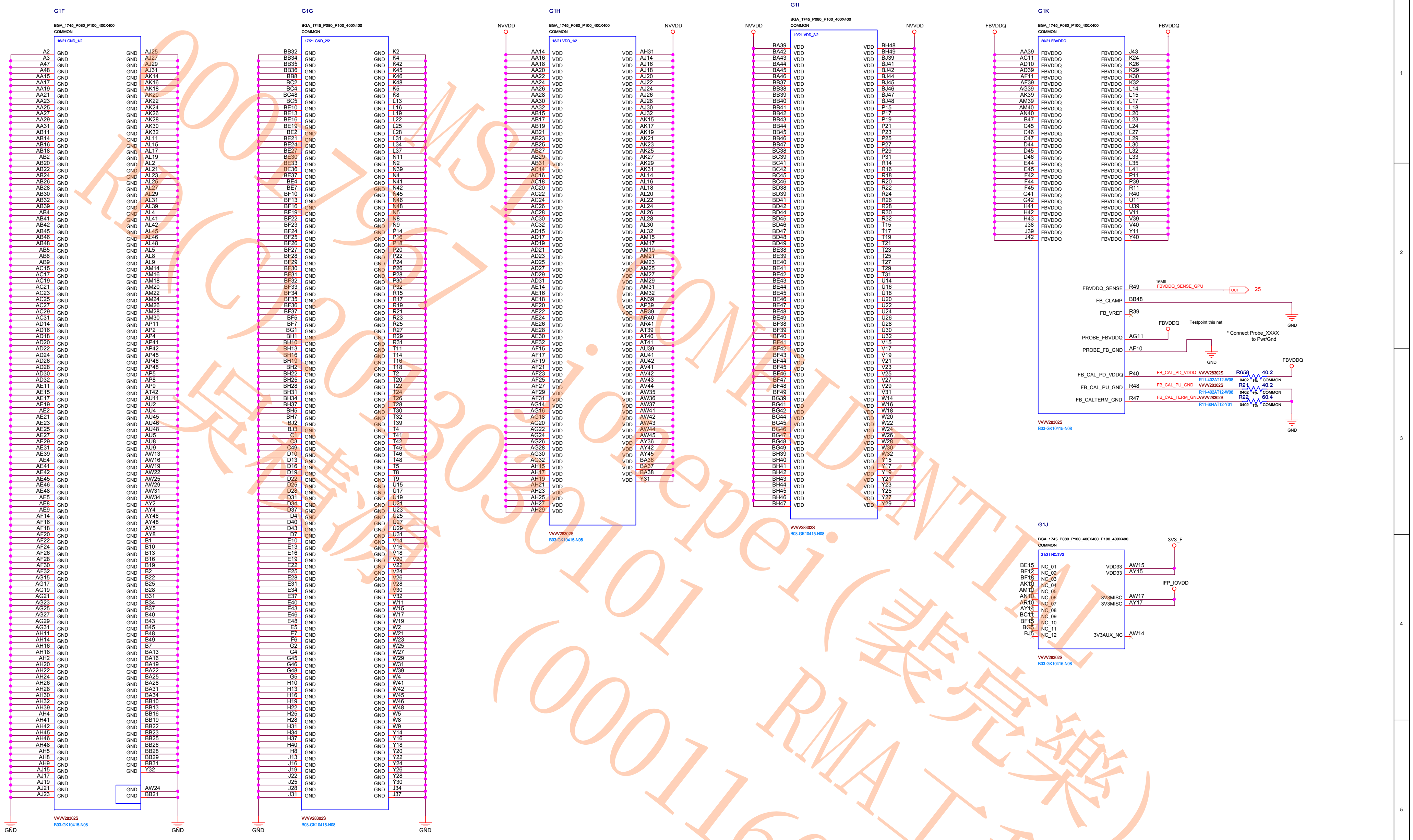
Date: Monday, April 23, 2012 | Sheet 12 of 33

Page13: MEMORY: FBD Partition 63..32



MICRO-STAR INT'L CO.,LTD	
MS-V283	
Size: Custom	Document Description: MEMORY_ FBD[63_32]
Rev: 1.0	
Date: Monday, April 23, 2012	Sheet: 13 of 33

Page14: GPU PWR and GND



MICRO-STAR INT'L CO.,LTD

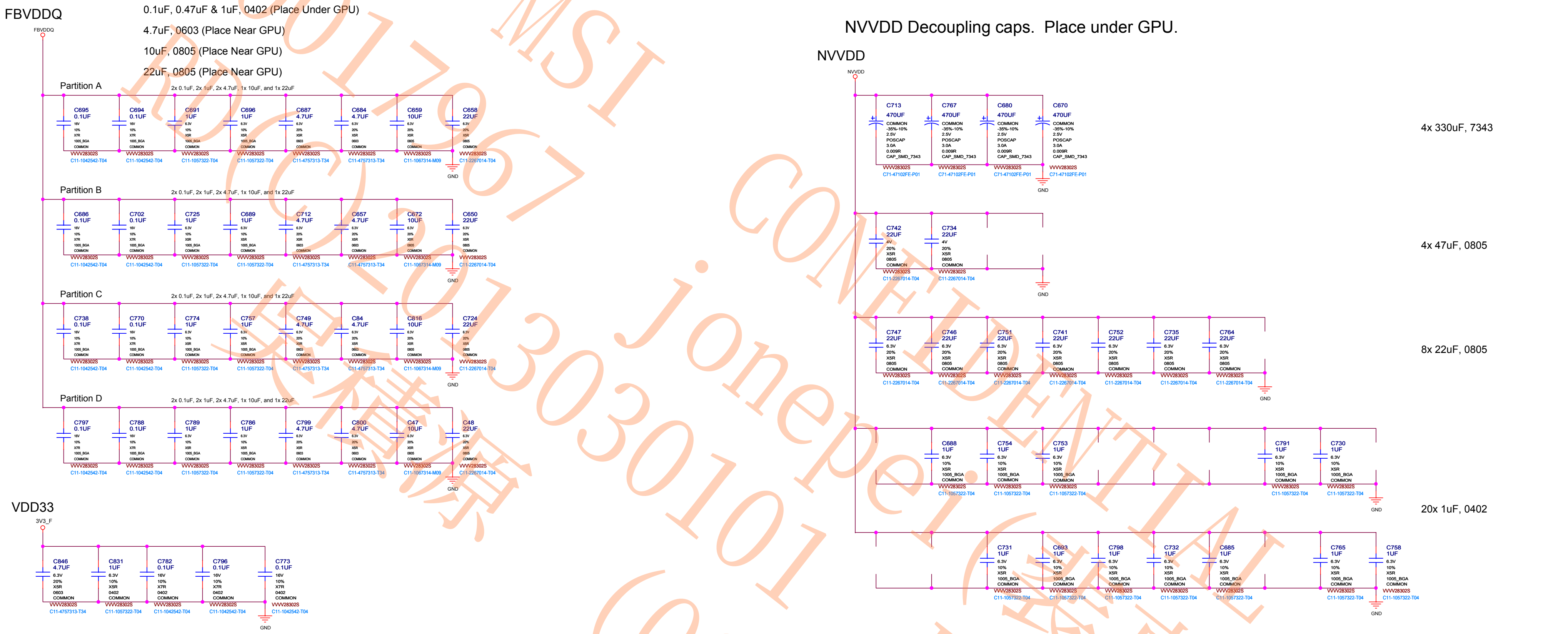
MS-V283

Size	Document Description	Rev
Custom	GPU PWR and GND	1.0

Date: Monday, April 23, 2012 Sheet 14 of 33

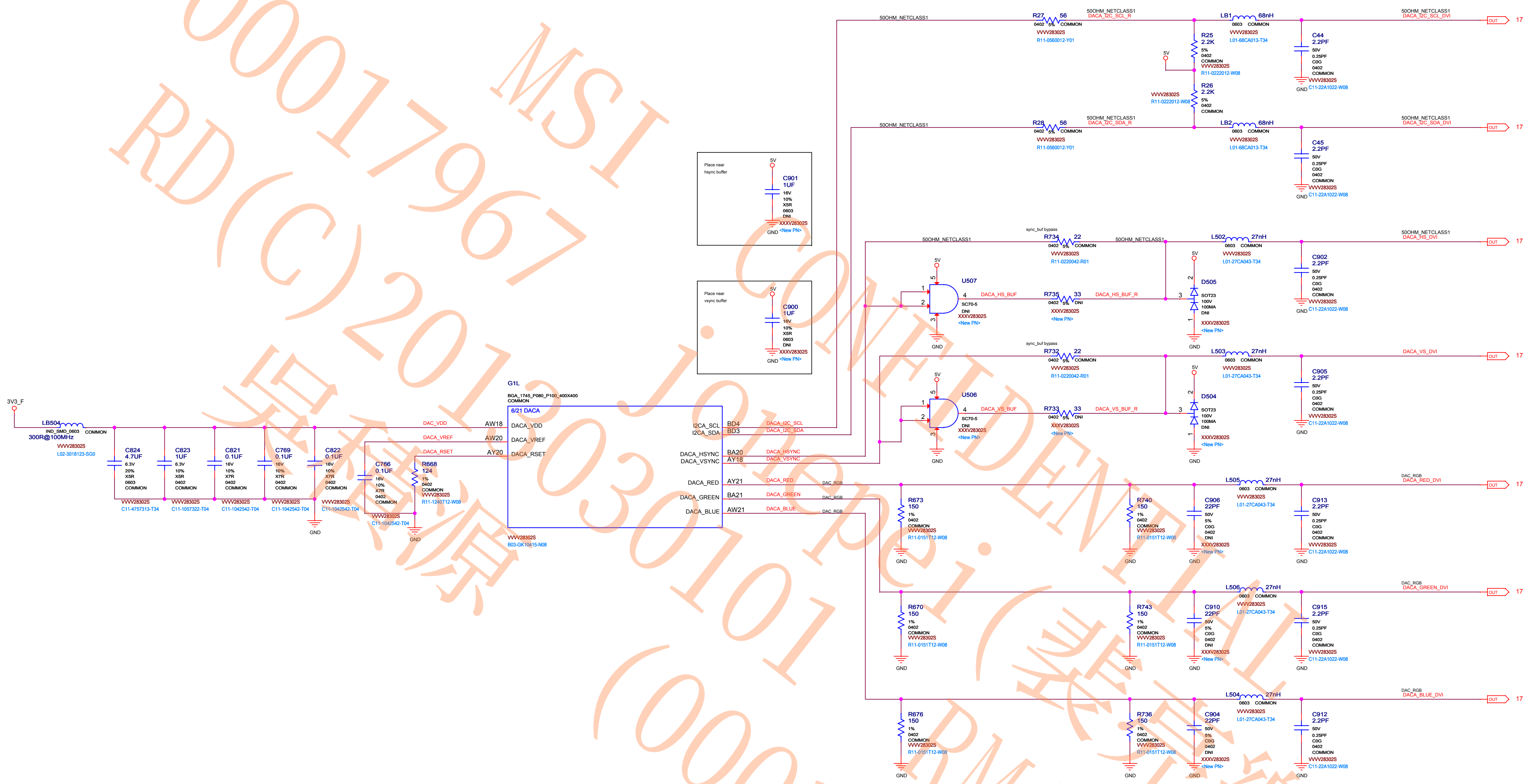
Page15: GPU Decoupling

Based on GB2-X GDDR5 FBVDDQ Decap Guideline



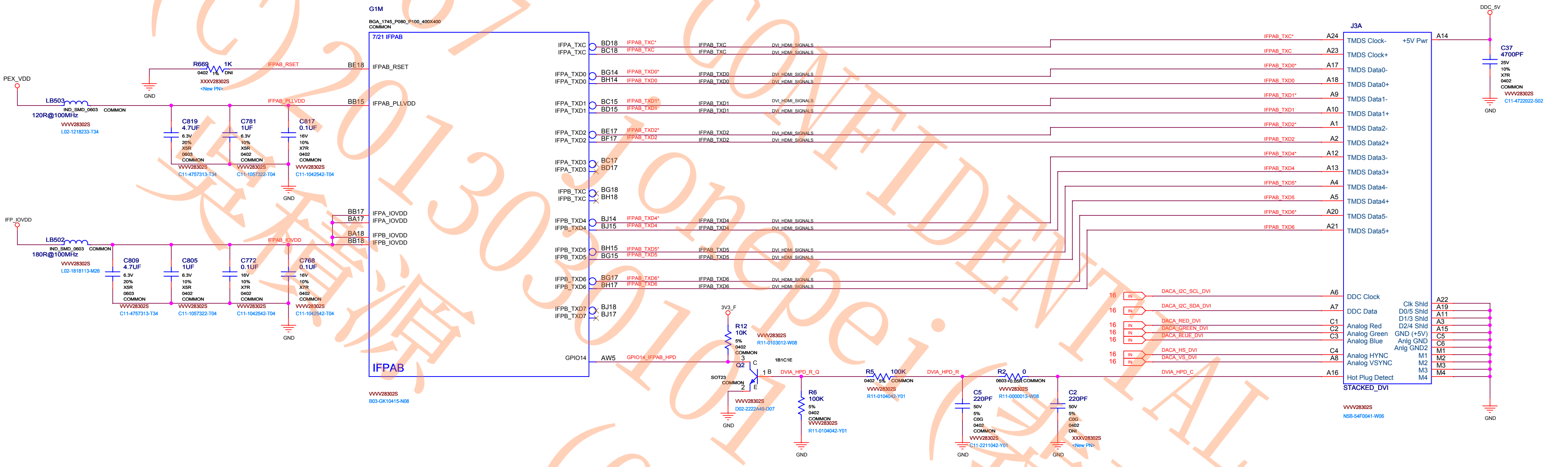
MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size: Custom	Document Description: GPU Decoupling	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 15 of 33	

Page16: DACA Interface



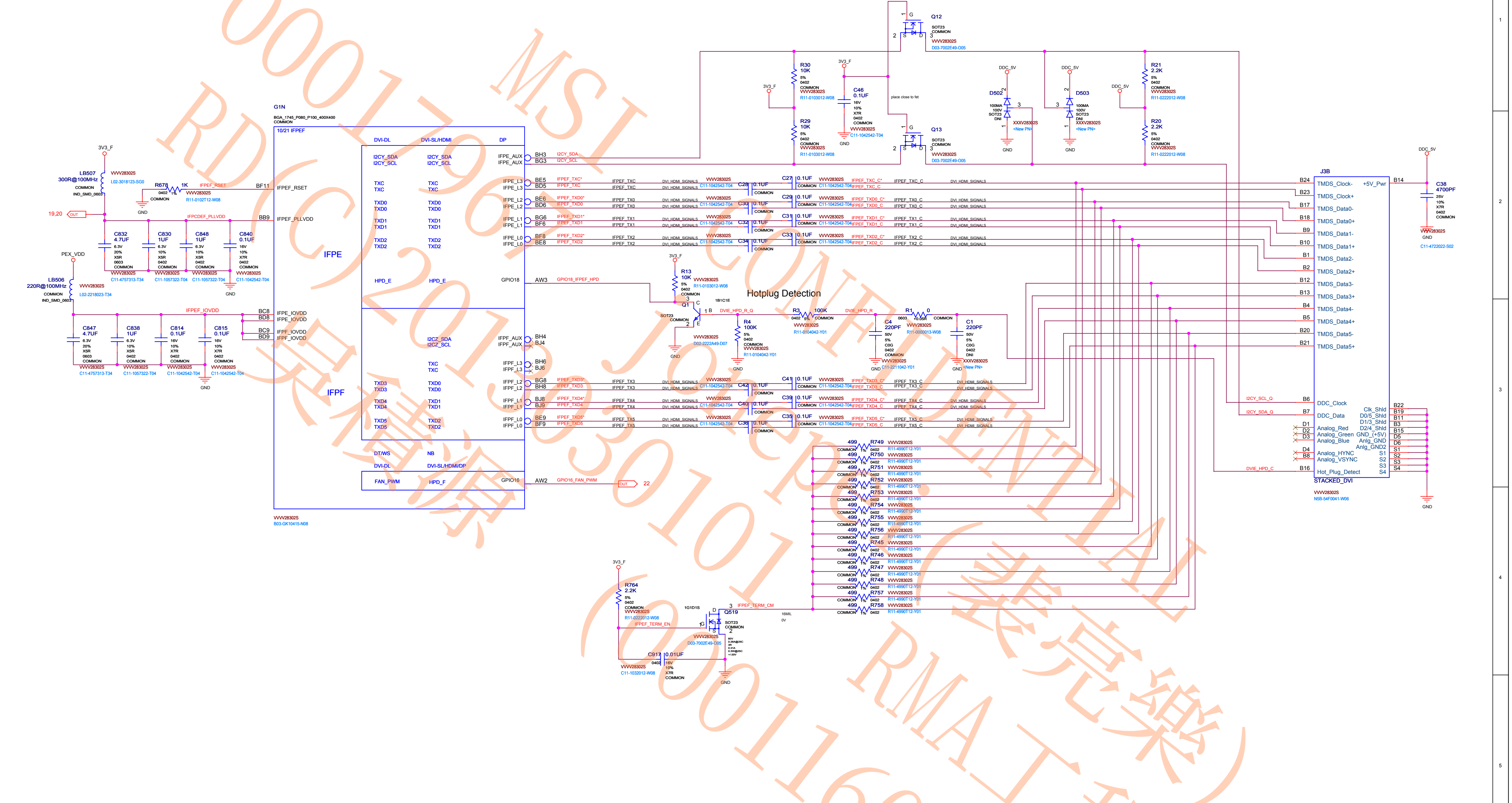
MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size Custom	Document Description DACA Interface	Rev 1.0
Date: Monday, April 23, 2012	Sheet 16 of 33	

Page17: IFPAB DVI-I-DL



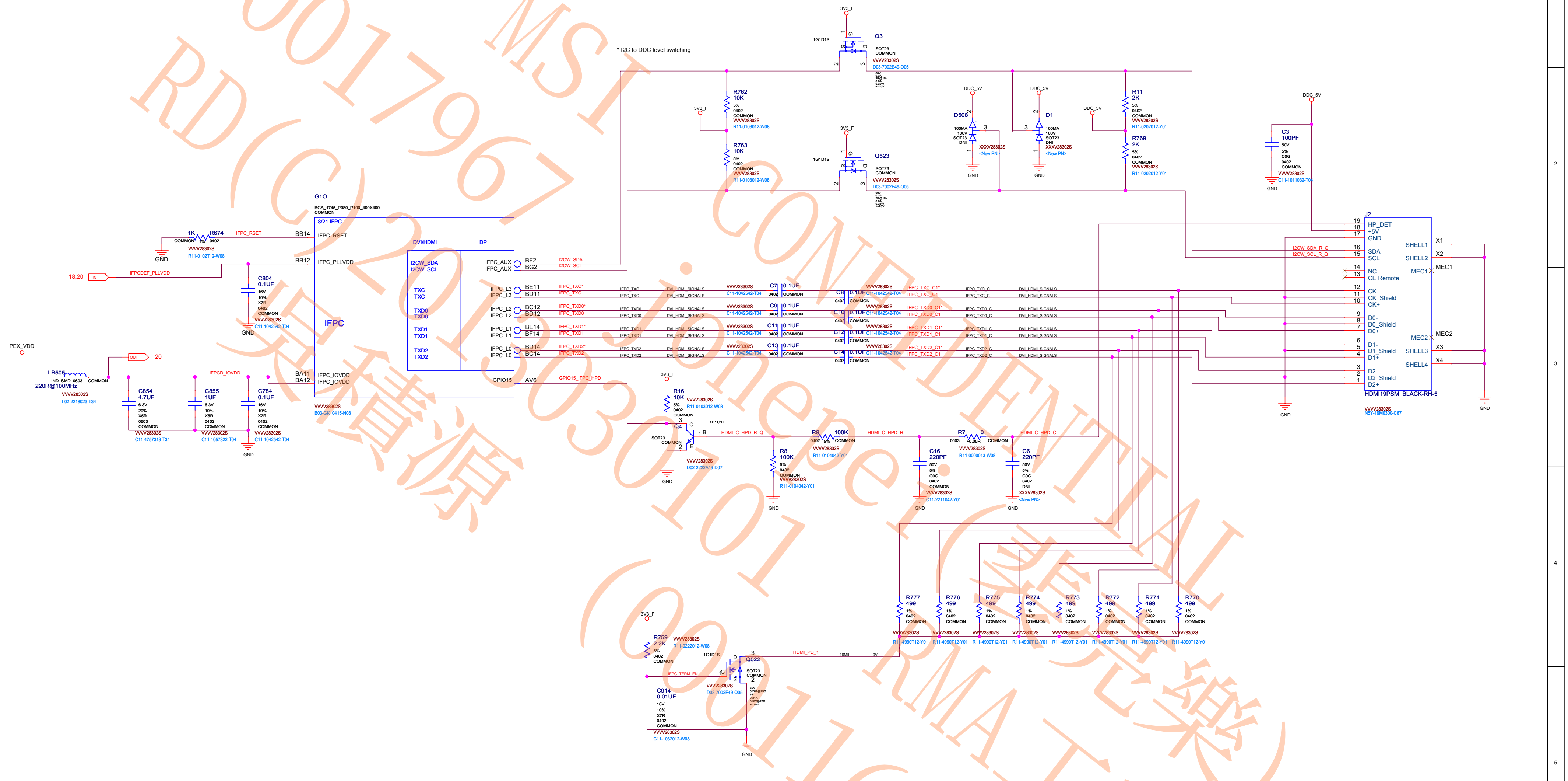
MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size: Custom	Document Description: IFPAB DVI-I-DL	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 17 of 33	

Page18: IFPEF DVI-D-DL



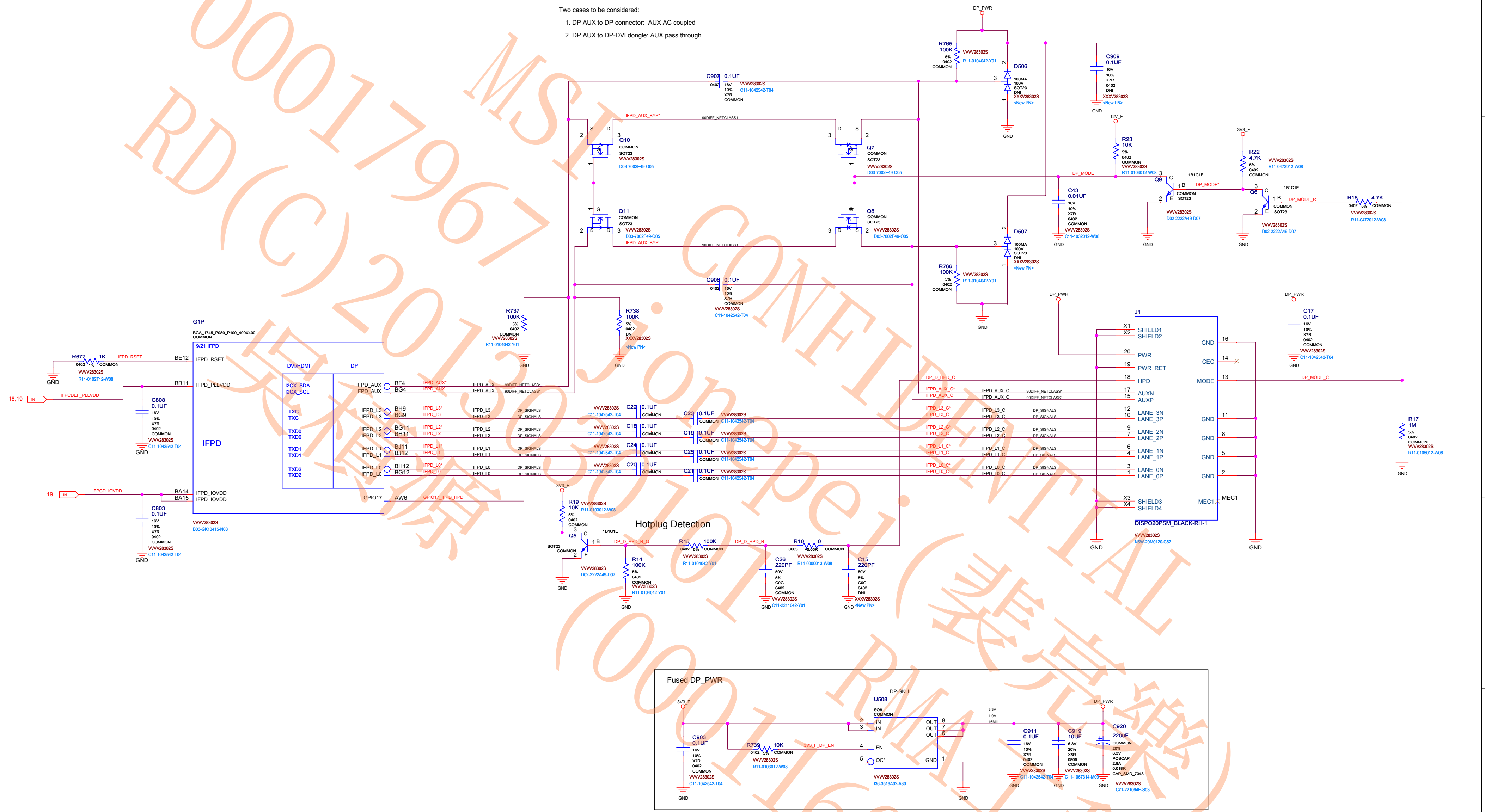
MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size: Custom	Document Description: IFPEF DVI-D-DL	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 18 of 33	

Page19: IFPC HDMI



MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size: Custom	Document Description: IFPC HDMI	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 19 of 33	

Page20: IFPD DP



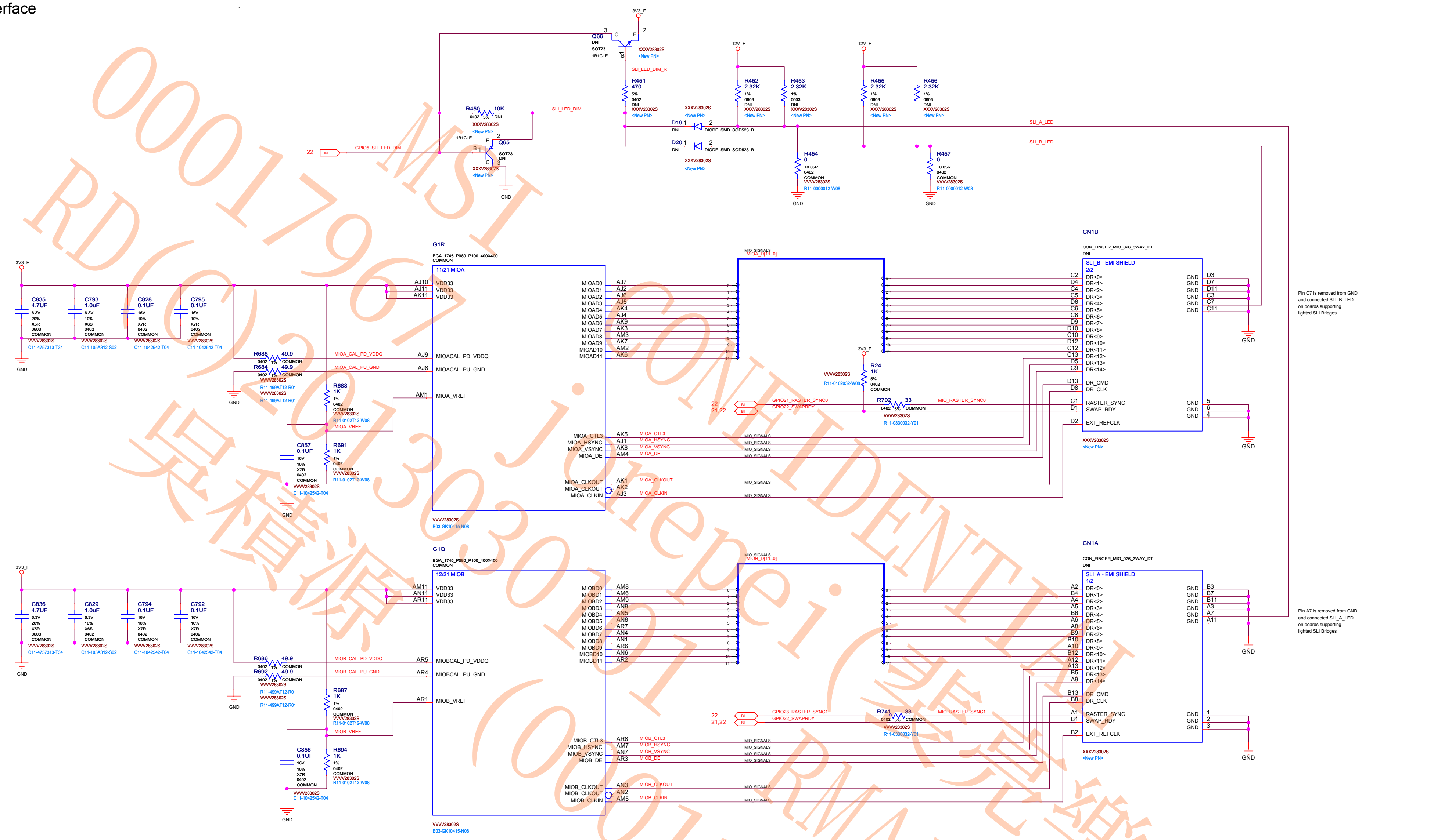
MICRO-STAR INT'L CO.,LTD

MS-V283

Size	Document Description	Rev
Custom	IFPD DP	1.0

Date: Monday, April 23, 2012 | Sheet 20 of 33

Page21: MIOA/B Interface



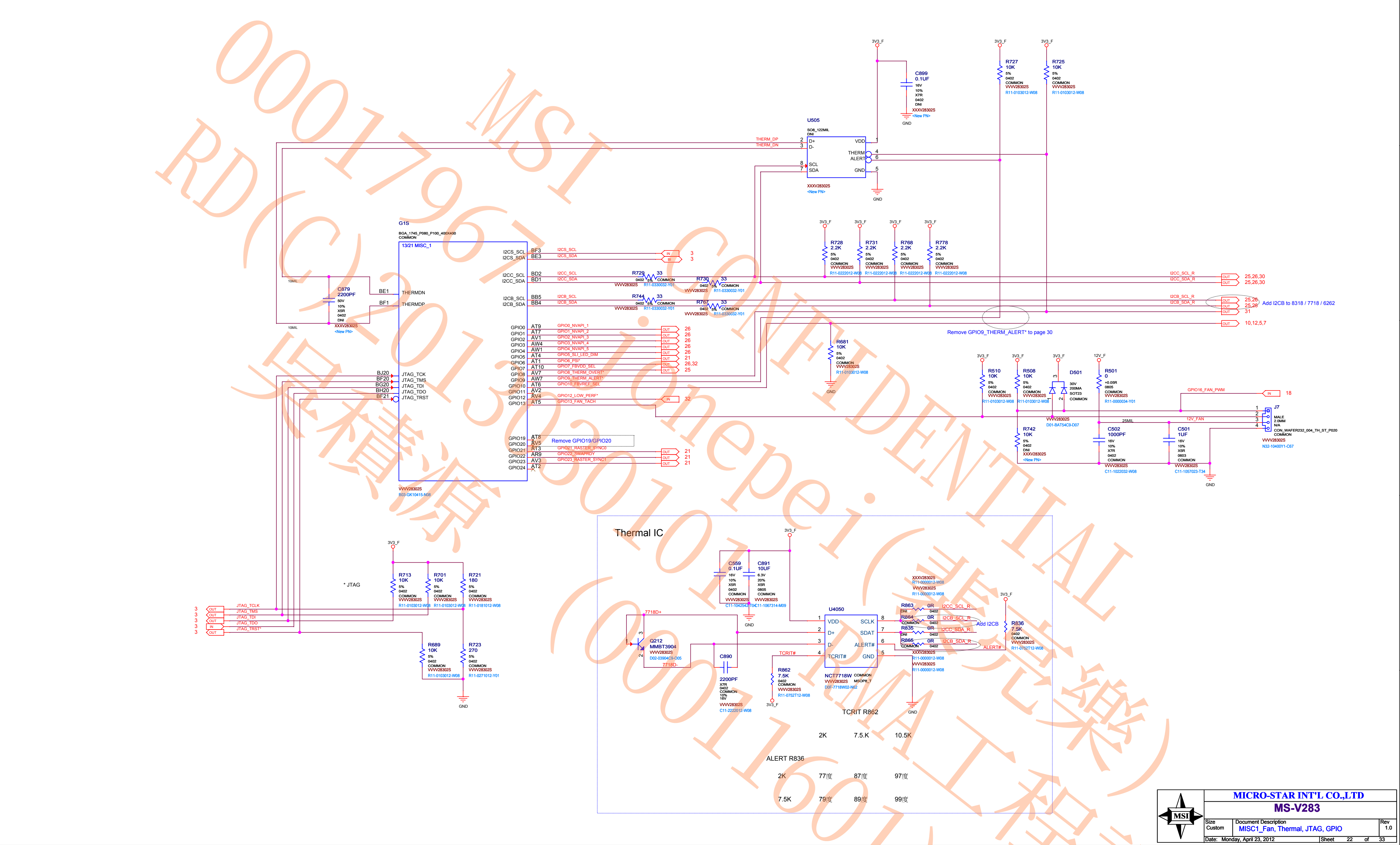
MICRO-STAR INT'L CO.,LTD

MS-V283

Size	Document Description	Rev
Custom	MIOA_B Interface	1.0

Date: Monday, April 23, 2012 Sheet 21 of 33

Page22: MISC1: Fan, Thermal, JTAG, GPIO



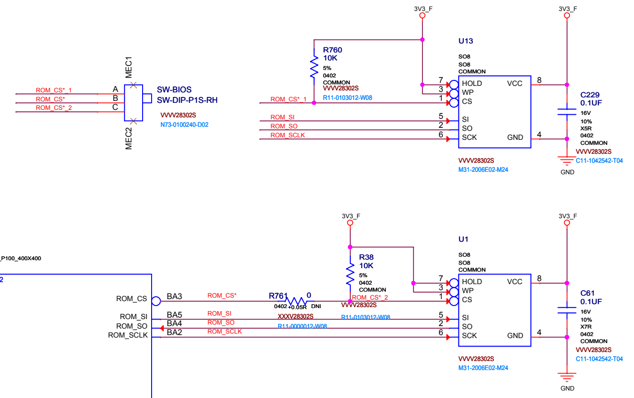
Page23: MISC2: ROM, XTAL, Straps

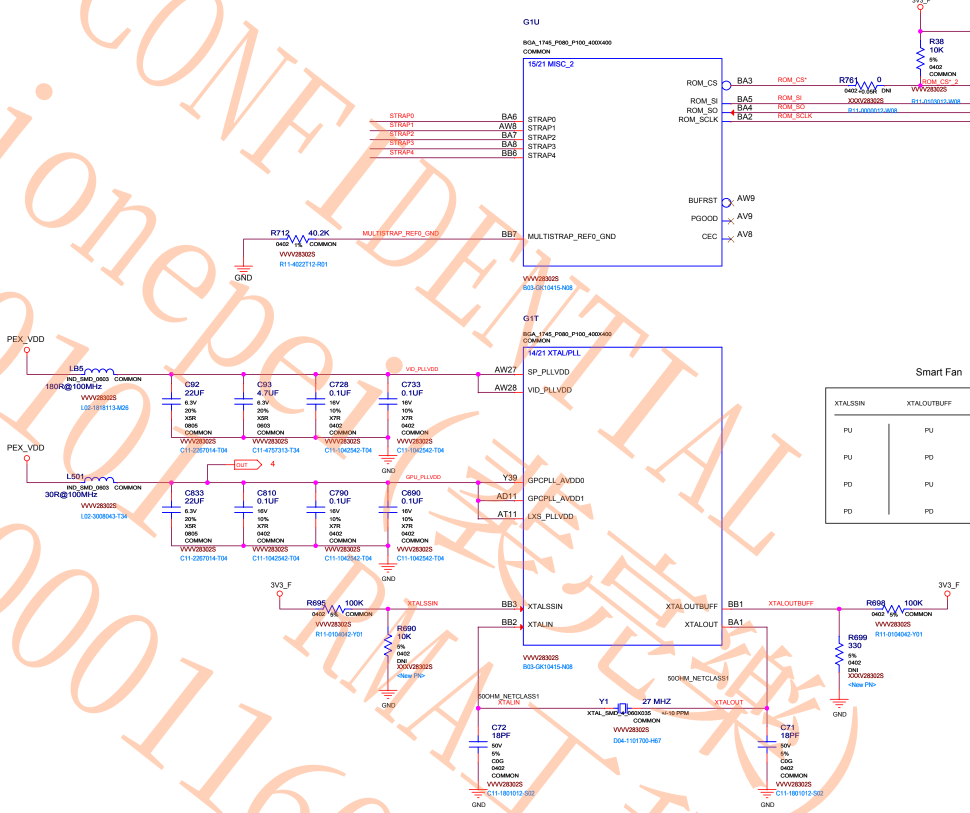
STRAP0	USER_BIT [3:0]*	0000*		5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*		5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0000 - (0x1180)*		5K PD -400 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*		45K PU*
STRAP4	DP_PLL_VDD_33V*	1*	FOR 3_3V*	45K PD*
	PEX_MAX_SPEED*	1*	FOR GEN2/3*	
	PEX_SPD_CHANGE_GEN3*	1*	ENABLED*	
	*			
ROM_SI	RAMCFG[0]*	0*		35K PD* (0110 for 64Mx32 256 bit Hynix for SKU 0 primary memory)
	RAMCFG[1]*	1*		
	RAMCFG[2]*	1*		
	RAMCFG[3]*	0*		
ROM_SO	VGA_DEVICE*	1*		10K PU*
	SMB_ALT_ADDR*	0*		
	FB[0]_APERTURE_SIZE*	0*	For 256MB*	
	FB[1]_APERTURE_SIZE*	1*	For 256MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0*	DISABLED*	25K PD*
	PCI_DEVID_EXT[5]*	0*	For 0x1180*	
	SUB_VENDOR*	1*	Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0*	For 0x1180*	

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

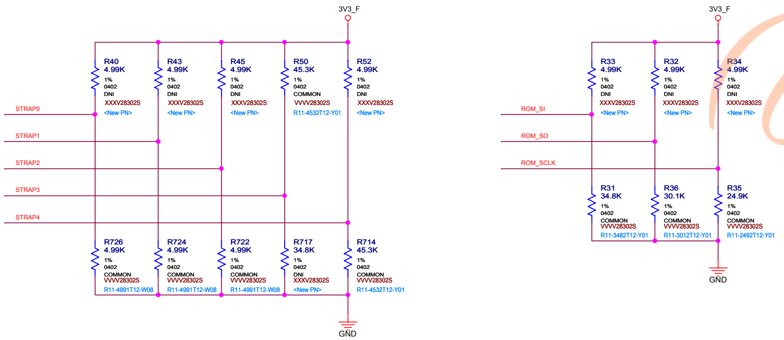
CFG[3:0]	Config Width Vendor
0000	Reserved
0001	32Mx32 256-bit Elpida
0010	32Mx32 256-bit Hynix
0011	32Mx32 256-bit Samsung
0100	Reserved
0101	64Mx32 256-bit Elpida
0110	64Mx32 256-bit Hynix
0111	64Mx32 256-bit Samsung
1000	Reserved
1001	32Mx32 192-bit Elpida
1010	32Mx32 192-bit Hynix
1011	32Mx32 192-bit Samsung
1100	Reserved
1101	64Mx32 192-bit Elpida
1110	64Mx32 192-bit Hynix
1111	64Mx32 192-bit Samsung

Dual BIOS





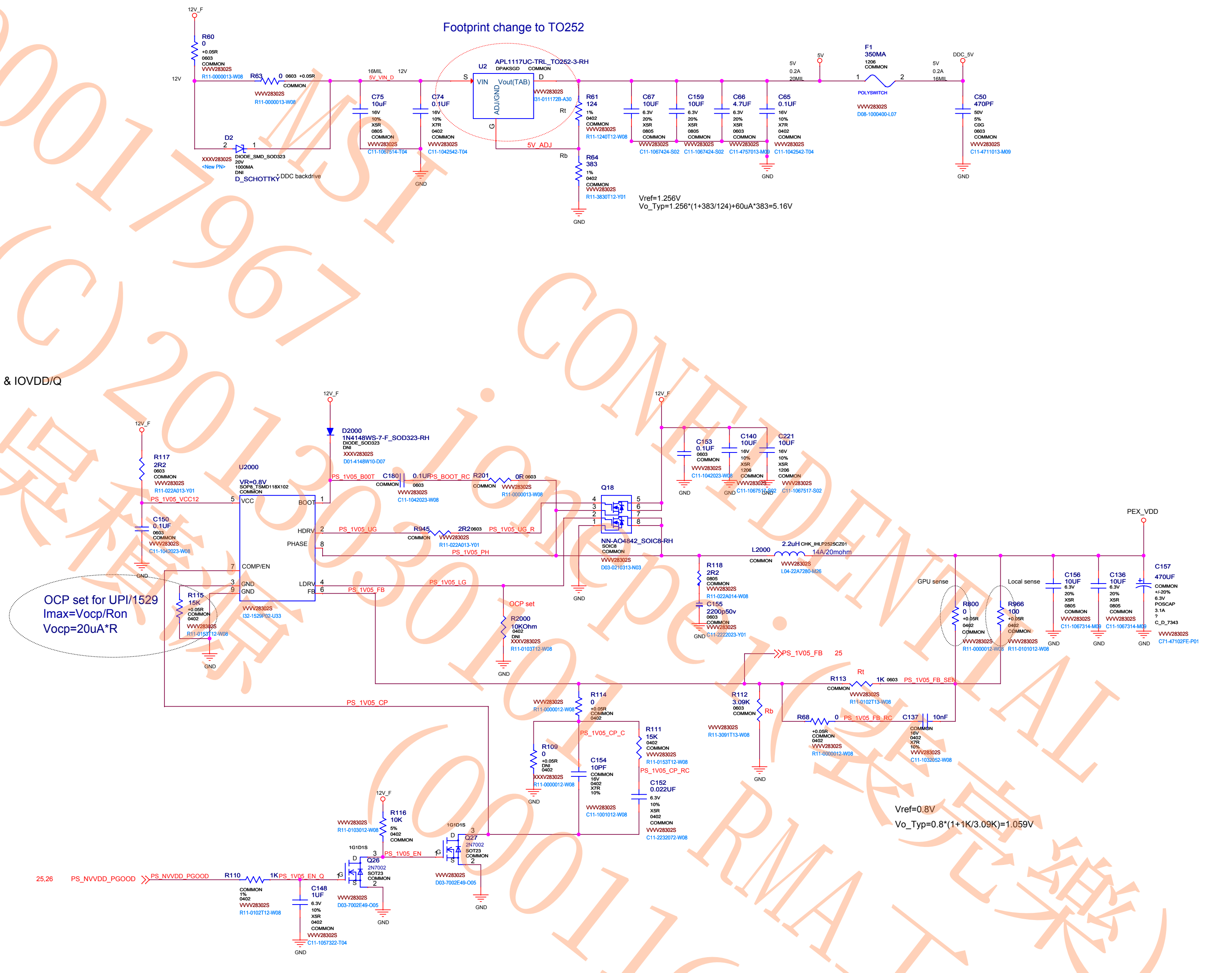
	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND



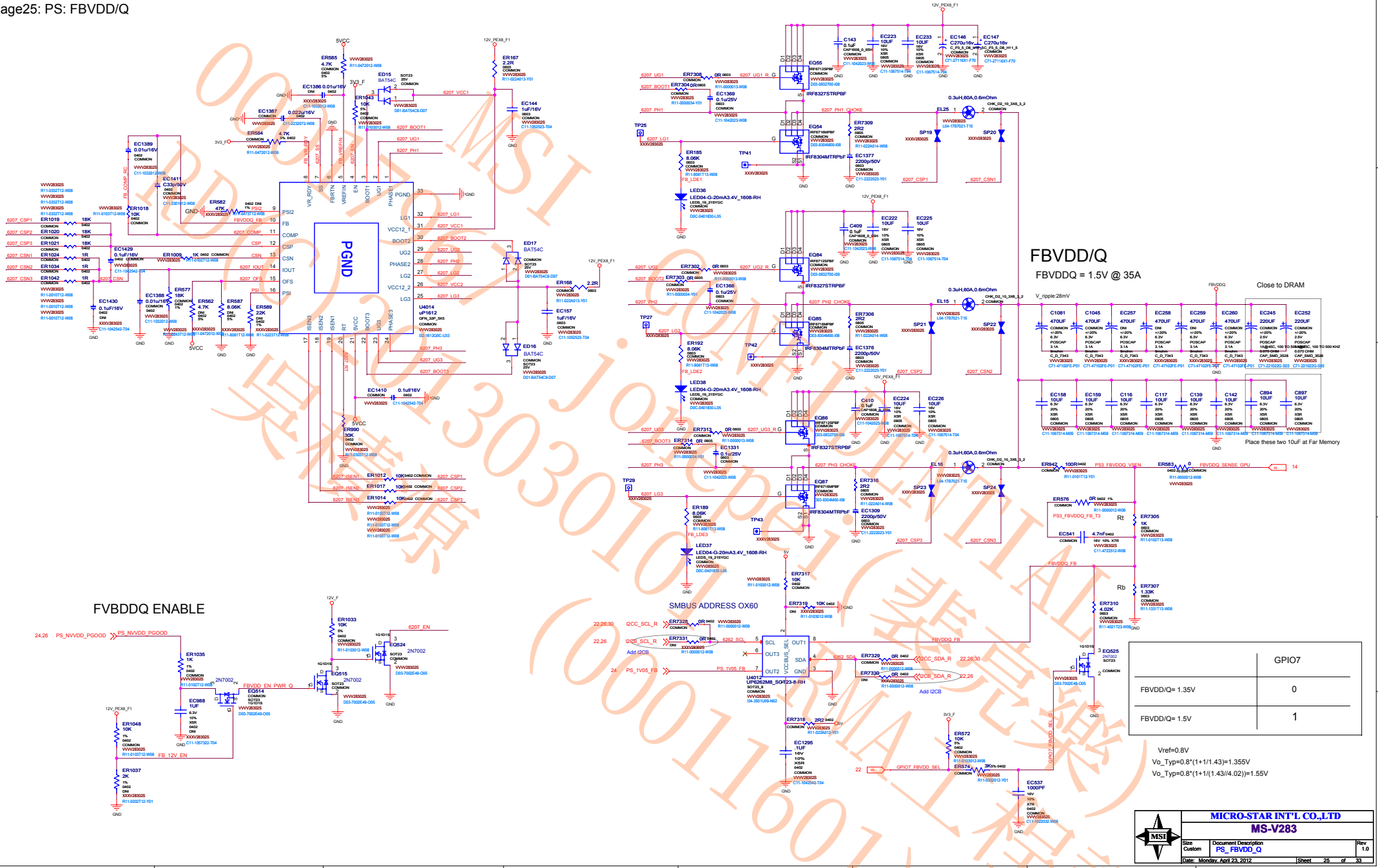
Smart Fan

XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

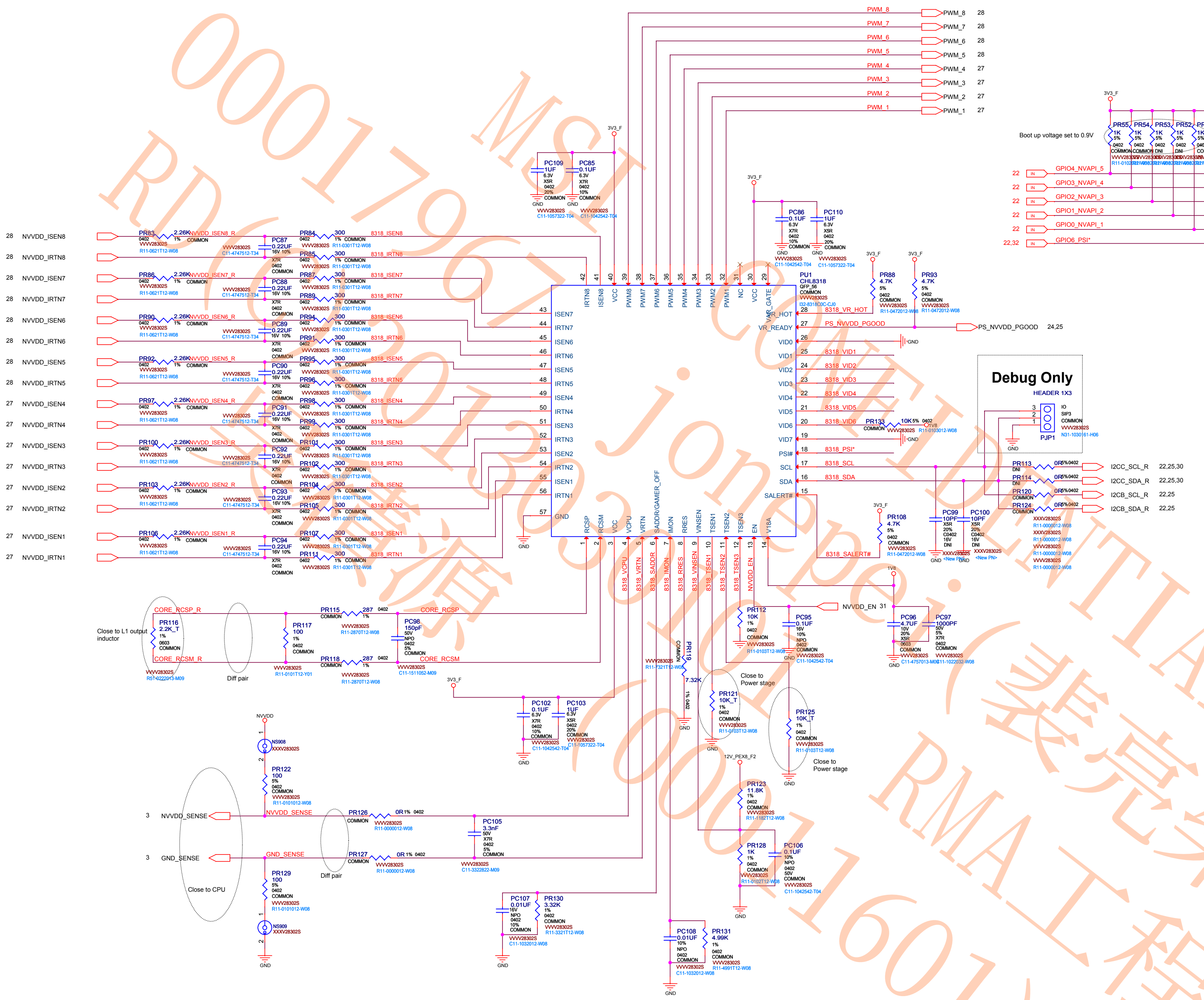
Page24: PS: 5V, PEX_VDD



MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size: Custom	Document Description: PS_5V, PEX_VDD	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 24 of 33	


FBVDD/Q
FBVDDQ = 1.5V @ 35A
V_ripple:28mV
Close to DRAM
Place these two 10uF at Far Memory
FVBDDQ ENABLE
SMBUS ADDRESS OX60
PGND
GPIO7
FBVDD/Q= 1.35V
0
FBVDD/Q= 1.5V
1
Vref=0.8V
Vo_Typ=0.8*(1+1/1.43)=1.355V
Vo_Typ=0.8*(1+1/(1.43//4.02))=1.55V
MICRO-STAR INT'L CO.,LTD
MS-V283
PS_FBVDD_Q
Rev 1.0
Monday, April 23, 2012
Sheet 25 of 33

Page26: PS: NVVDD Controller (CHIL 8318)



SOFT START (VR11)

1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPIO tri-state
   VID[5:1]=11000 to set 0.9125V

P-STATE VOLTAGES

1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V

VID Table

GPIO7	GPIO6	GPIO5	GPIO2	GPIO17	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

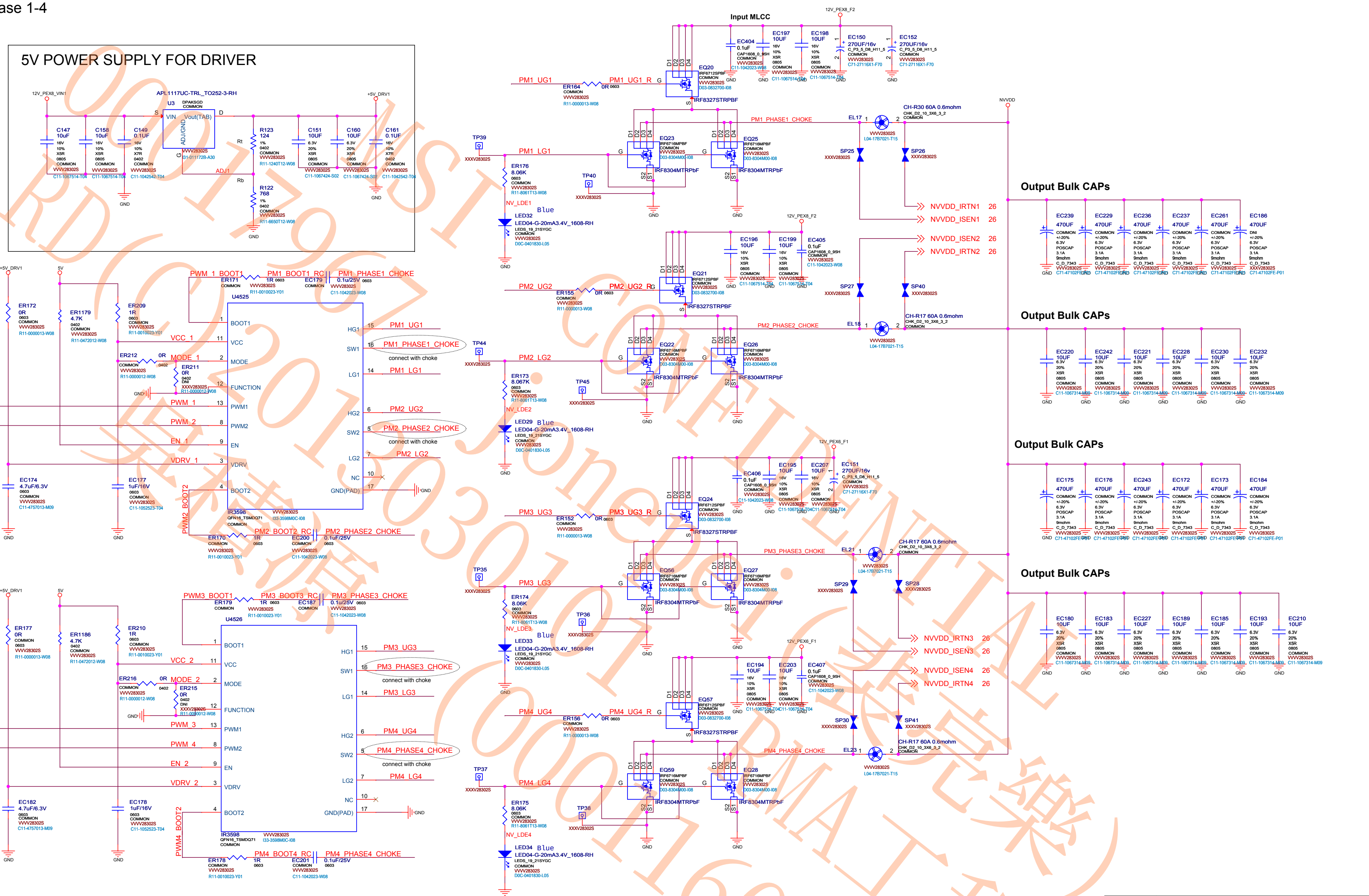
MICRO-STAR INT'L CO.,LTD
MS-V283

Size: Custom | Document Description: PS_ NVVDD Controller | Rev: 1.0

Date: Monday, April 23, 2012 | Sheet 26 of 33

Page27: PS: NVVDD Phase 1-4

Function	Mode	PWM Mode	Phase Mode
0	1	IR ATL	Dual
1	1	IR ATL	Doublar
0	0	tri-state	Dual
1	0	tri-state	Doublar

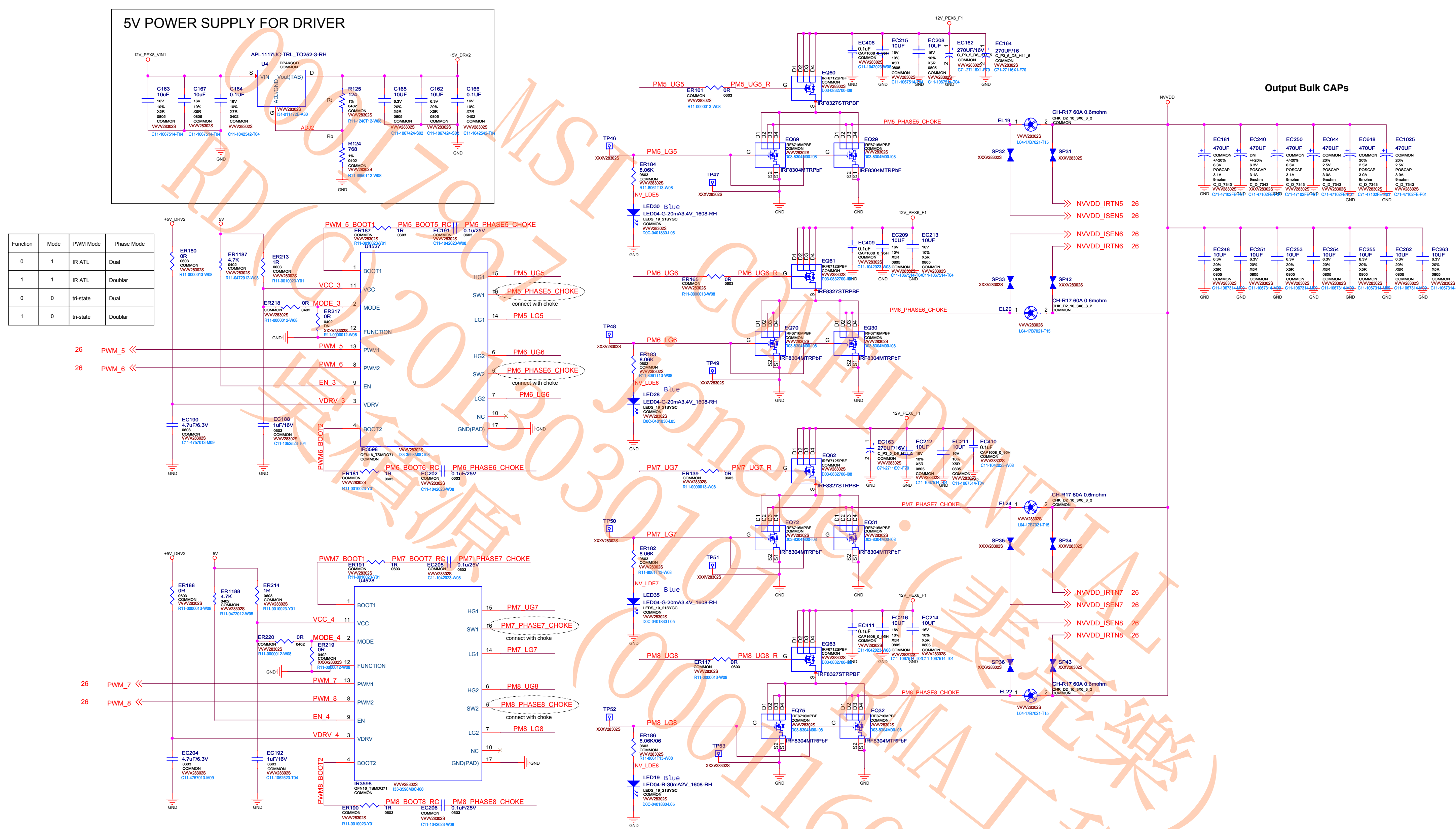


MICRO-STAR INT'L CO.,LTD
MS-V283

Size	Document Description	Rev
Custom	PS_ NVVDD Phase 1-4	1.0

Date: Monday, April 23, 2012 Sheet 27 of 33

Page28: PS: NVVDD Phase 5-8



Function	Mode	PWM Mode	Phase Mode
0	1	IR ATL	Dual
1	1	IR ATL	Doublar
0	0	tri-state	Dual
1	0	tri-state	Doublar

MICRO-STAR INT'L CO.,LTD

MS-V283

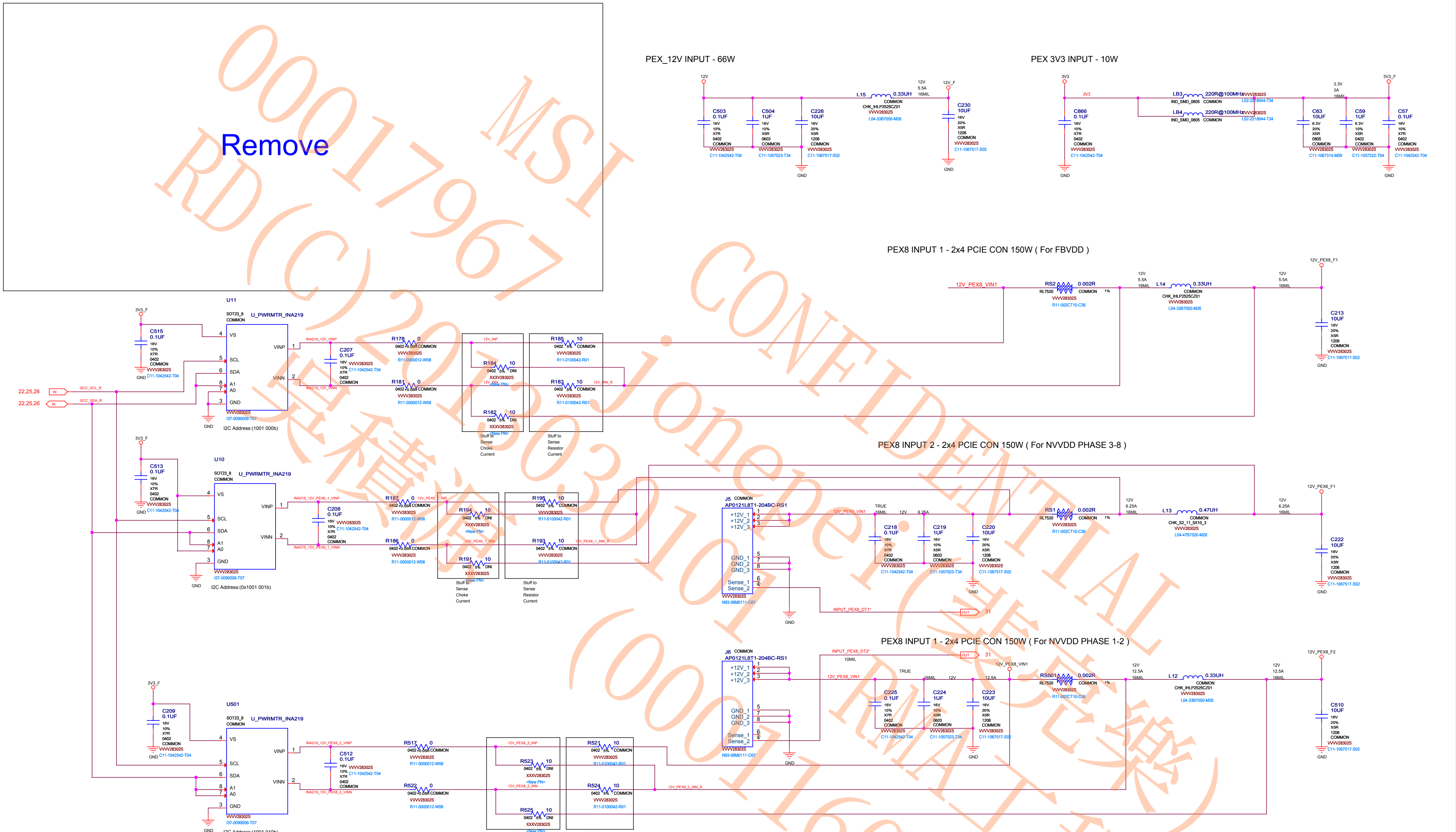
Size: Custom | Document Description: PS_ NVVDD Phase 5-8 | Rev: 1.0

Date: Monday, April 23, 2012 | Sheet 28 of 33

Page29: PS: NVVDD Phase 9-10 (N/A)

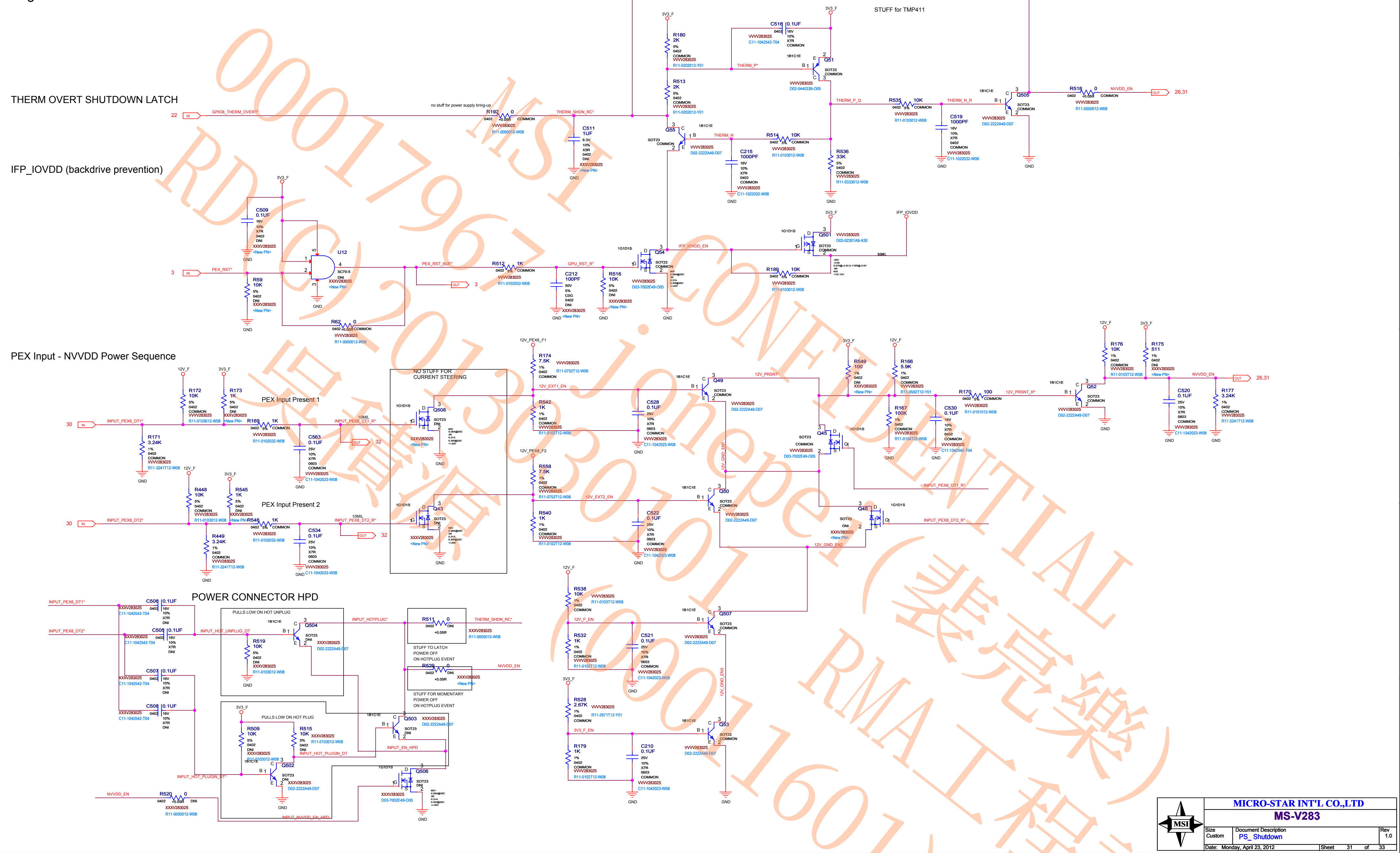
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V283	
Size: Custom	Document Description: PS_ NVVDD Phase 9-10	Rev: 1.0
Date: Friday, April 20, 2012	Sheet 29 of 33	

Page30: PS: Inputs, Filtering, and Monitoring

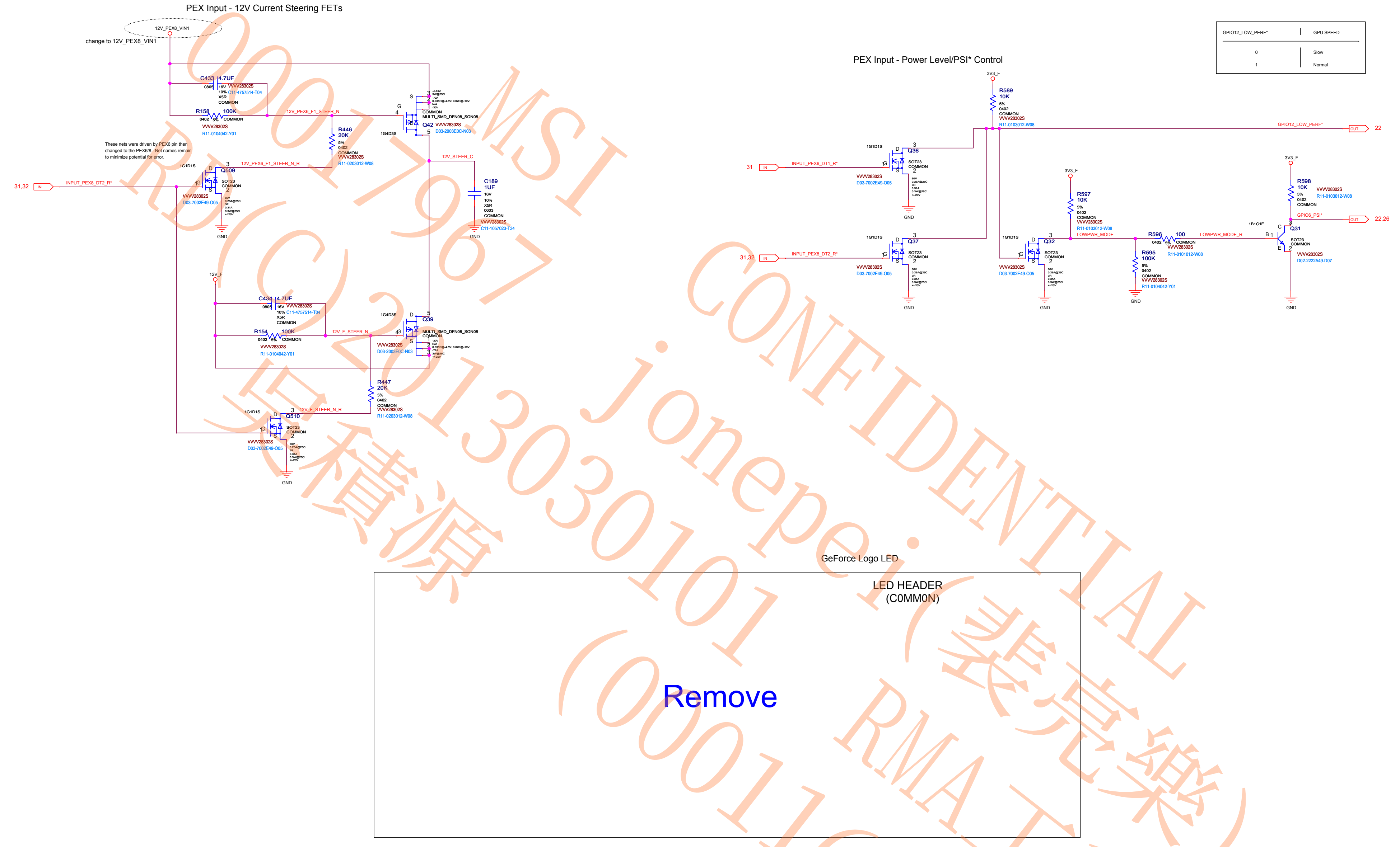


MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size: Custom	Document Description: PS_ Inputs, Filtering, and Monitoring	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 30 of 33	

Page31: PS: Shutdown



Page32: PS: 12V Current Steering, PSI Control, and LED



MICRO-STAR INT'L CO.,LTD		
MS-V283		
Size: Custom	Document Description: PS_ 12V Current Steering P	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 32 of 33	

Page33: Mechanical: Bracket/Thermal Solution