

GF110-P1261

P1261-A00 GF110, GDDR5 384Bi t
DVI -I -DL, DVI -I -DL/DP, Mi ni -HDMI

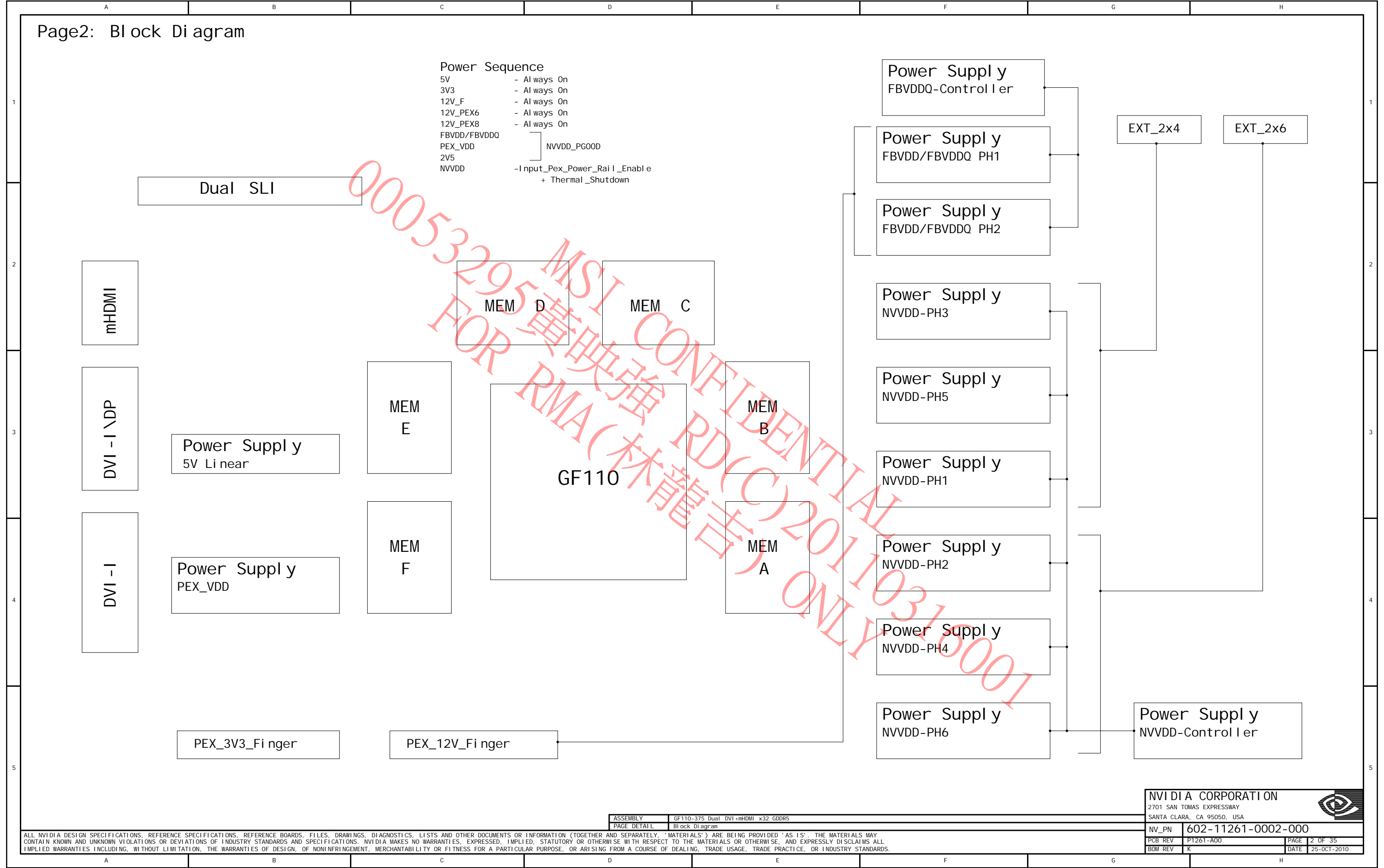
TABLE OF CONTENTS

Page	Descripti on
1	Table of Contents
2	Block Diagram
3	PCI Express 2.0
4	MEMORY: GPU Partition A/B
5	FBA Partition
6	FBB Partition
7	MEMORY: GPU Partition C/D
8	FBC Partition
9	FBD Partition
10	MEMORY: GPU Partition E/F
11	FBE Partition
12	FBF Partition
13	GDDR5 Memory Decoupling
14	GPU Decoupling
15	DAC_A for South DVI -I
16	DAC_B for Mid DVI -I
17	I FP A/B Interface (South DVI)
18	I FP E/F Interface(Middle DVI)
19	I FP D Interface/Mid DP
20	I FP C Interface (North mHDMI)
21	MI SC: GPIO, I2C, ROM, and XTAL
22	Mul ti -use IO(MI O) Interface
23	GPU POWER CONNECTIONS
24	Strapping Configurati on
25	MI SC: Thermal / BACKDRIVE

Page	Descripti on
26	Mechani cal
27	Power Supply: 5V, PEX_PLLVDD, 8V5
28	Power Supply: PEXVDD
29	Power Supply: FBVDDQ
30	Power Supply: NVVDD Controller
31	Power Supply: NVVDD Phase 1-2 of 6
32	Power Supply: NVVDD Phase 3 & 5 of 6
33	Power Supply: NVVDD Phase 4 & 6 of 6
34	Power Input and Load Monitoring, LED, Power Sequence
35	Power Supply: NVVDD Controller(Option)

sku	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11261-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-11261-0000-000	P1261 GF100-400 1536MB GDDR5 32x32M DVI -I +DVI -I +mHDMI
2	SKU0001	600-11261-0001-000	P1261 GF110-400 1536MB GDDR5 32x32M DVI -I +DP+mHDMI
3	SKU0090	600-11261-0090-000	P1261 GF110-400 1536MB GDDR5 32MX32 DVI -I +DVI -I +mHDMI ADT7473 ENGINEERING SKU
4	SKU9900	600-11261-9900-000	P1261 GF110-400 1536MB GDDR5 32MX32 DVI -I +DVI -I +mHDMI PRIMARY ENGINEERING SKU
5	SKU0002	600-11261-0002-000	P1261 GF110-375 1536MB GDDR5 32MX32 DVI -I +DVI -I +mHDMI
6	SKU0005	600-11261-0005-000	P1261 GF110-275 1280MB GDDR5 32MX32 DVI -I +DVI -I +mHDMI
7	SKU0003	600-11261-0003-000	P1261 GF110-375 1536MB GDDR5 32MX32 DVI -I +DP+mHDMI
8	SKU0022	600-11261-0022-000	P1261 GF110-375 CHRY 1536MB GDDR5 32MX32 DVI -I +DVI -I +mHDMI
9	SKU0025	600-11261-0025-000	P1261 GF110-275 CHRY 1280MB GDDR5 32MX32 DVI -I +DVI -I +mHDMI
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ASSEMBLY	GF110-375 Dual DVI+mHDMI x32 GDDR5
PAGE DETAIL	Block Diagram

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NV_PN	602-11261-0002-000	PAGE	2 OF 35
PCB REV	P1261-A00	DATE	25-OCT-2010
BOM REV	K		

12V O 12V 16MIL 5.5A NV SOURCE POWER_NET=TRUE C63 0.1UF 16V CN2 NONPHY-X16 CON_X16 CON_PCIEXP_X16_EDGE



Place near ball s

Matching Rule of Thumb

4 inch from Top of Gold Fingers to GPU
*2 inch Lane to Lane Skew

*No real Skew rule, but reducing the skew will minimize latency

ASSEMBLY	GF110-375 Dual DVI+mHDMI x32 GDDR5
PAGE DETAIL	PCI Express 2.0

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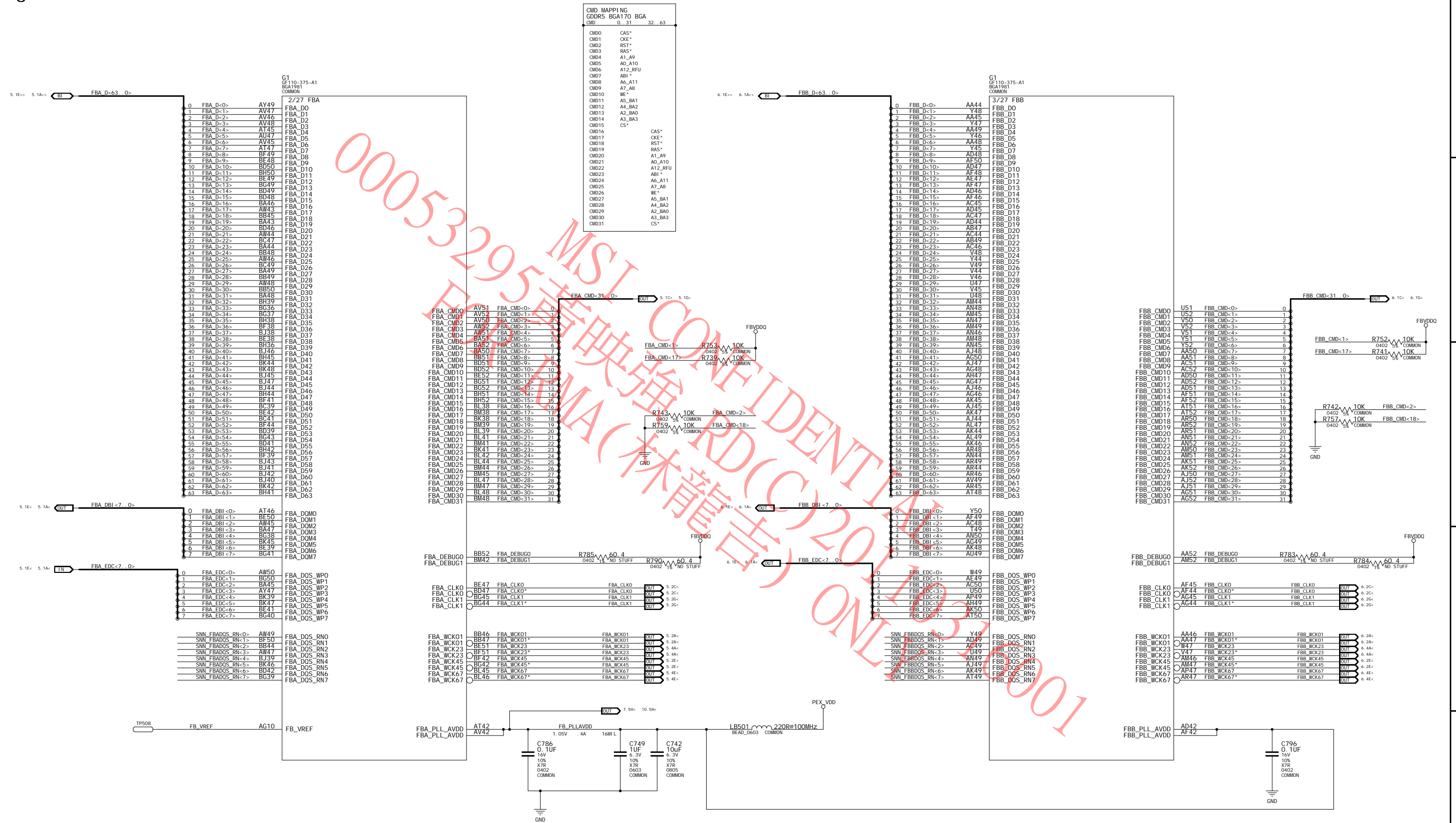
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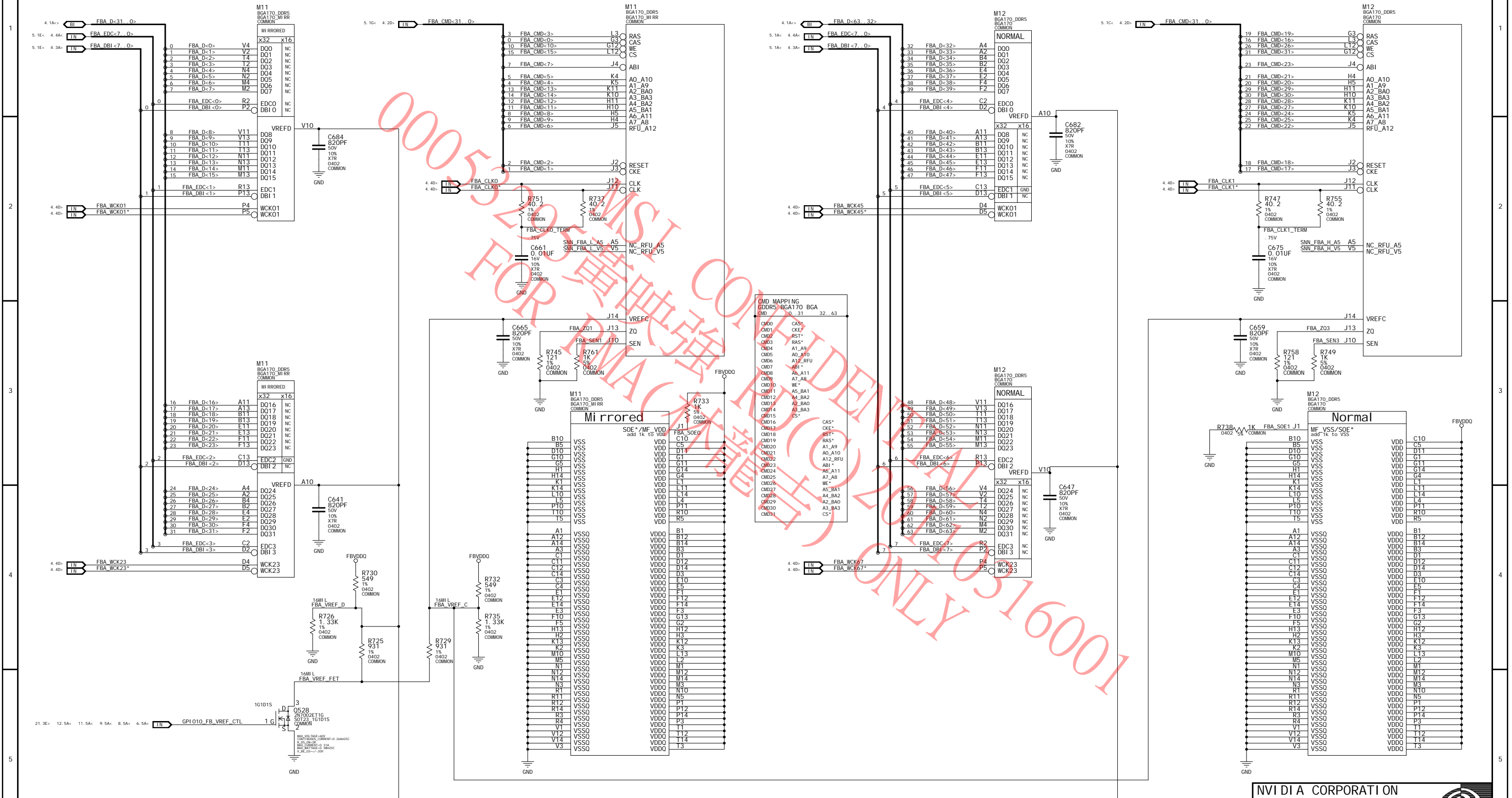
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PCB REV	P1261-A00	PAGE	3 OF 35
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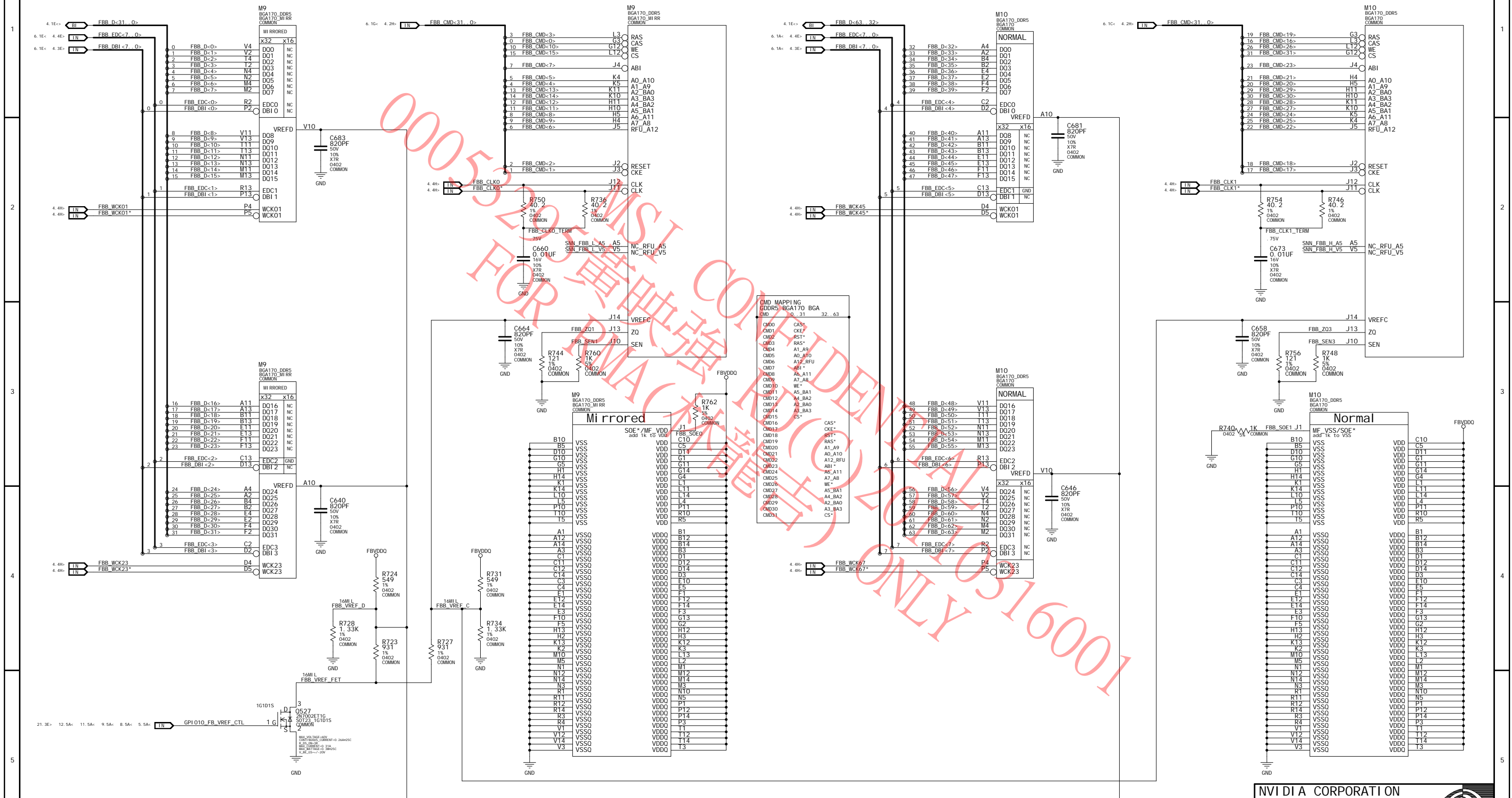


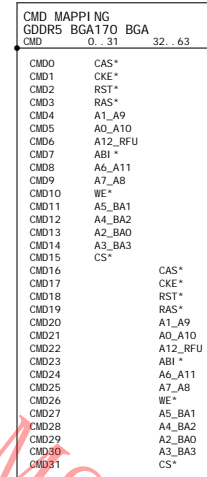


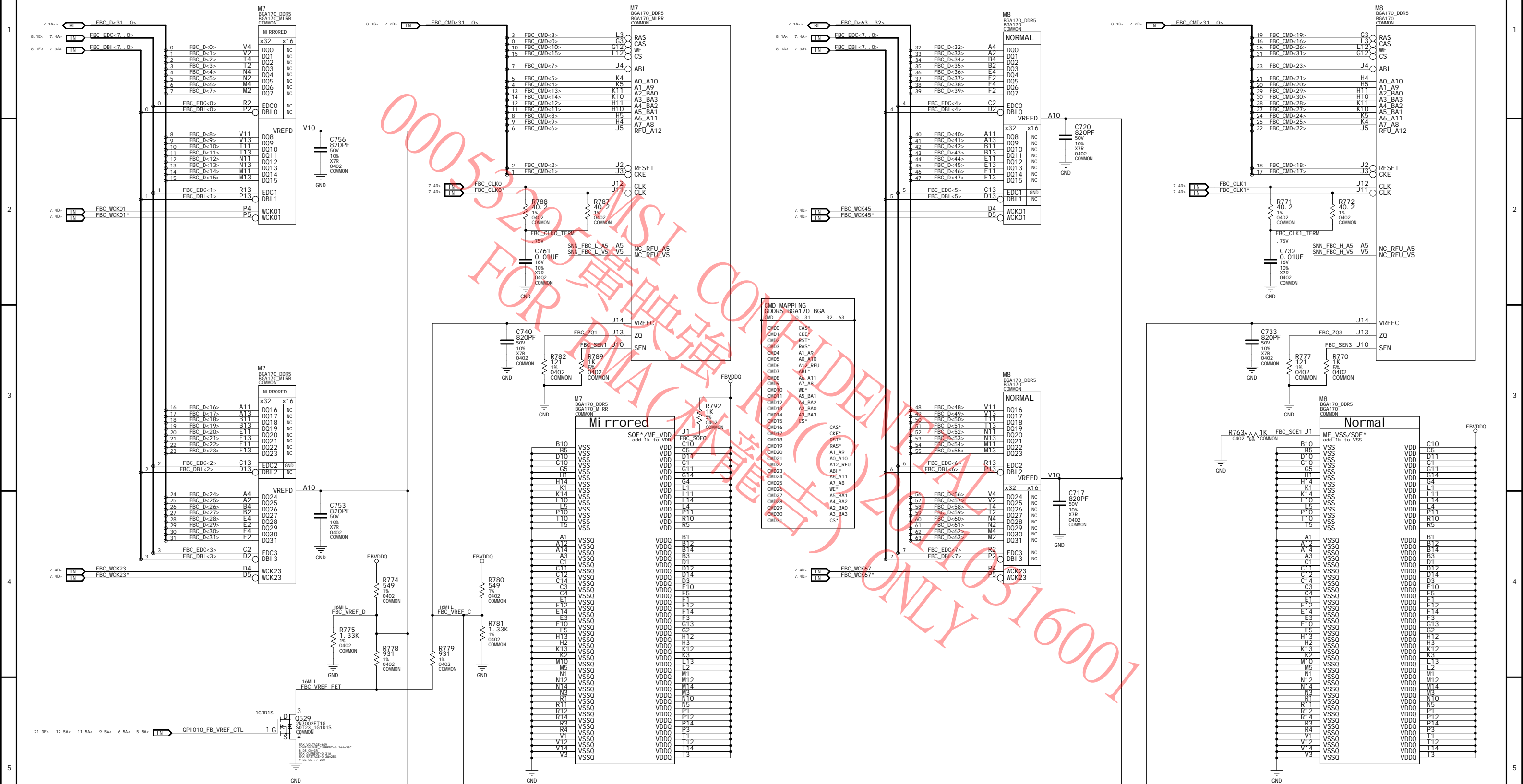
ASSEMBLY	GF110-375 Dual DVI +mHDMI x32 GDDR5
PAGE DETAIL	FBA Partition

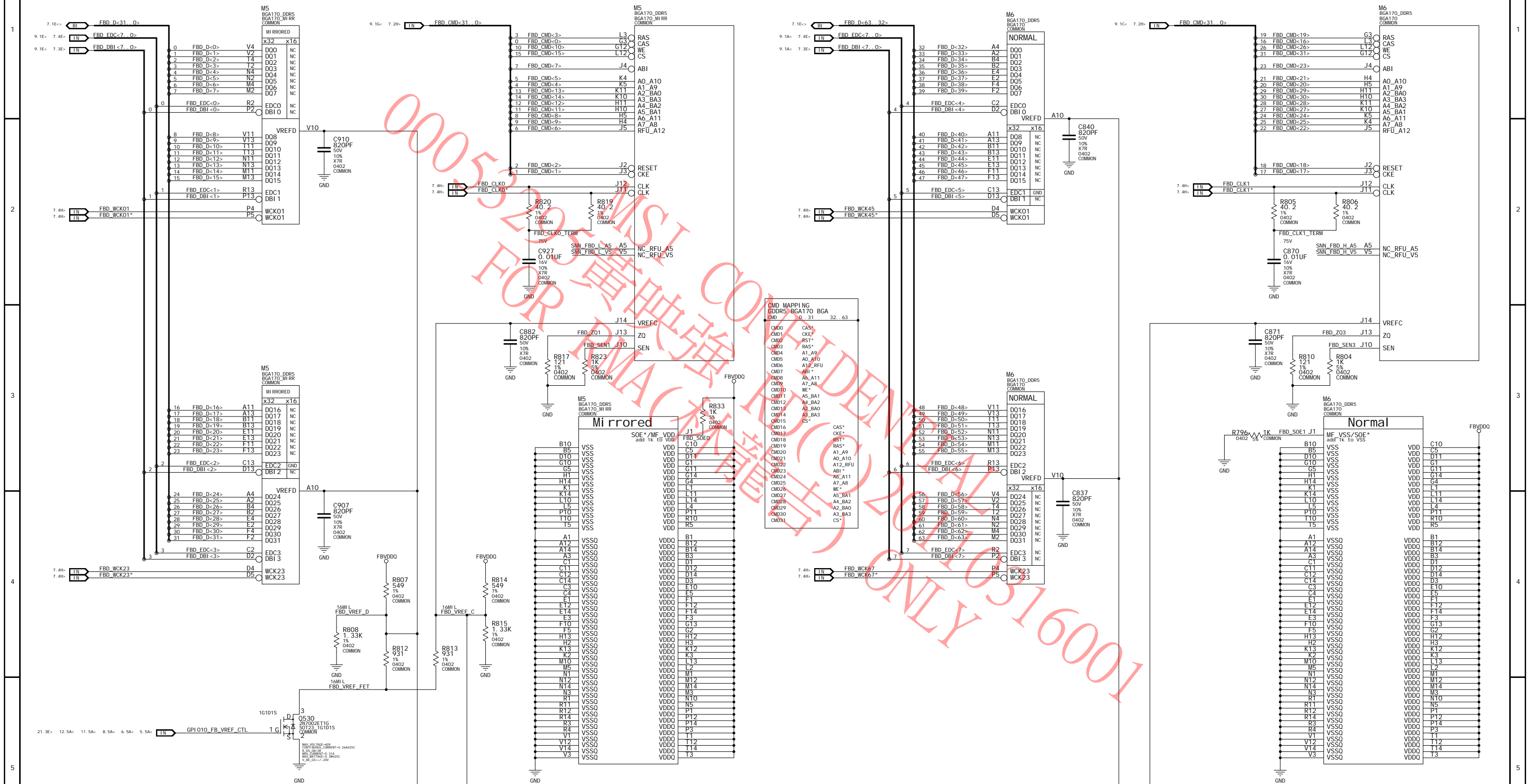
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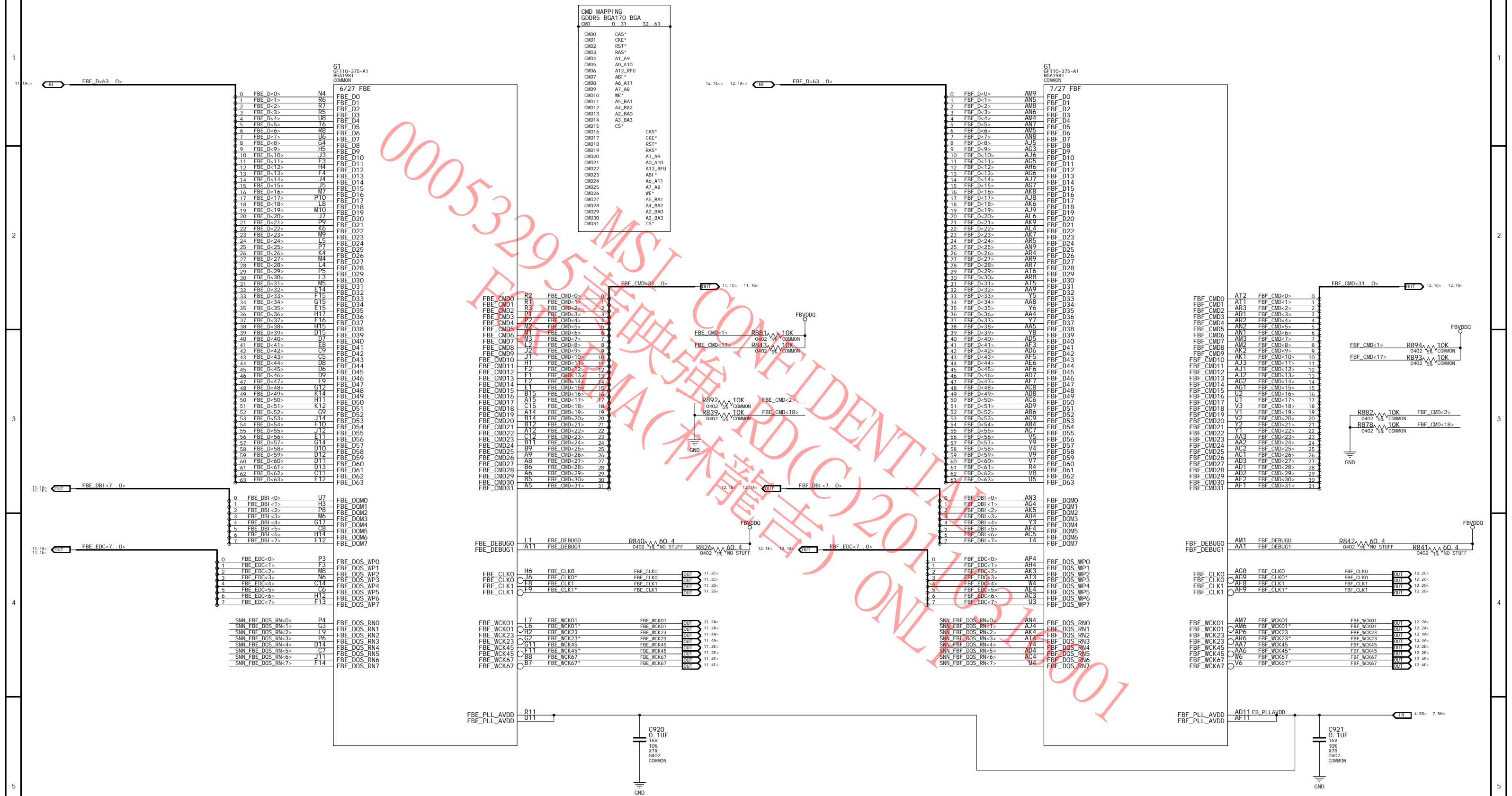
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PCB REV	P1261-A00	PAGE	5 OF 35
BOM REV	K	DATE	25-OCT-2010

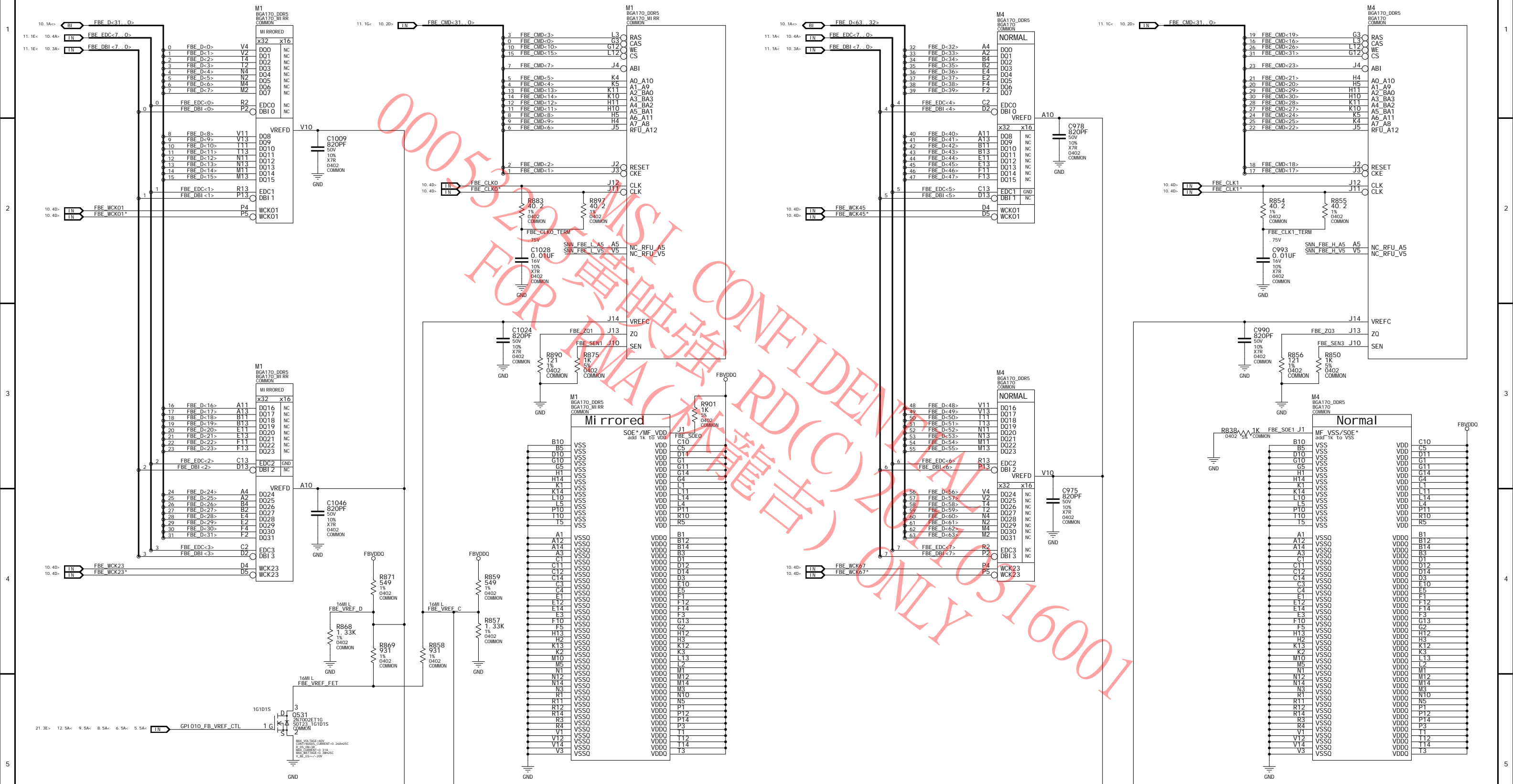


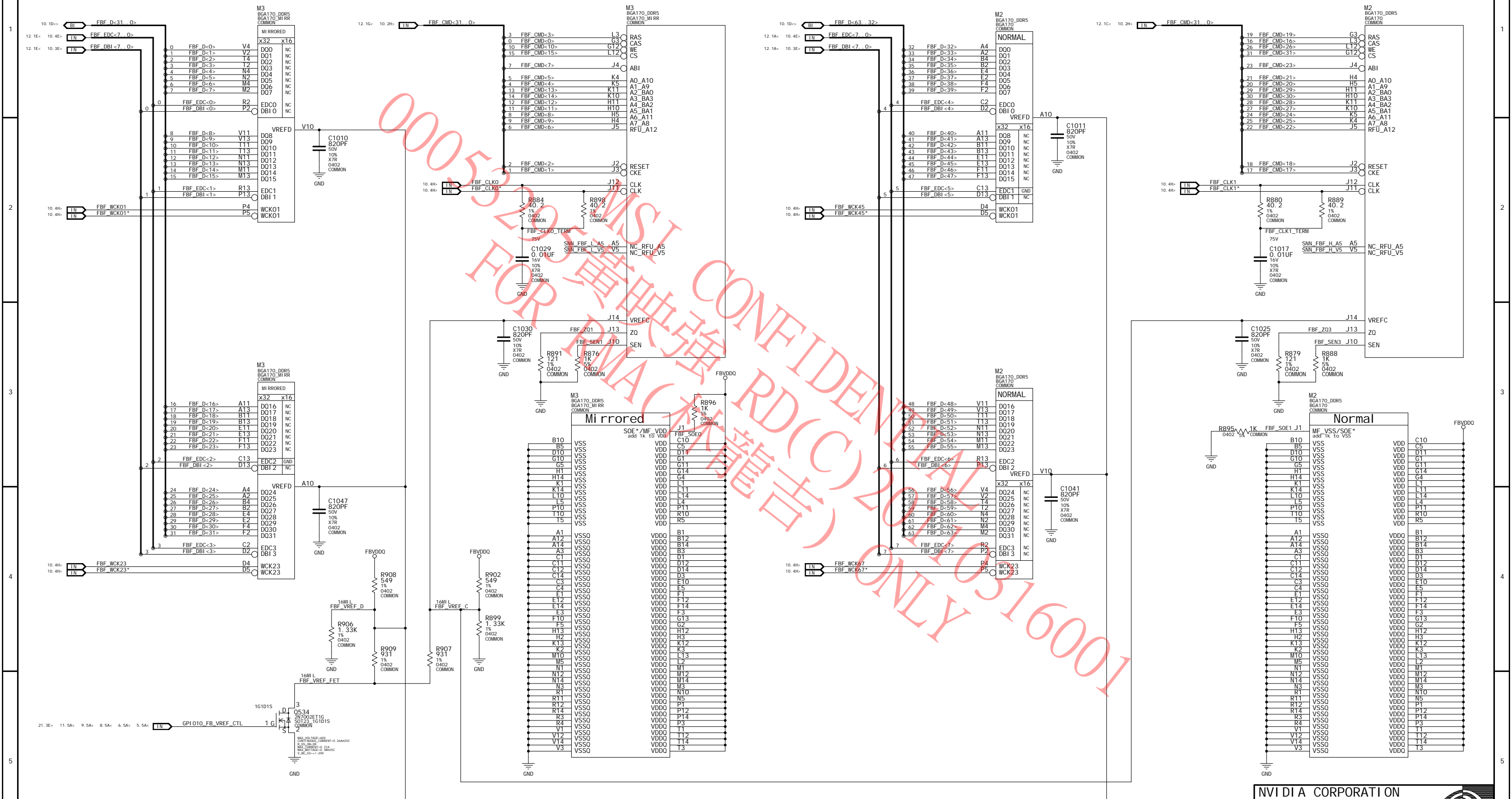




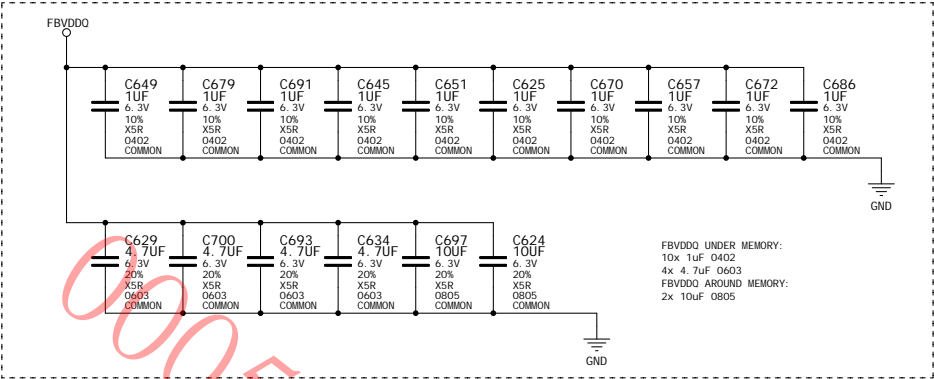




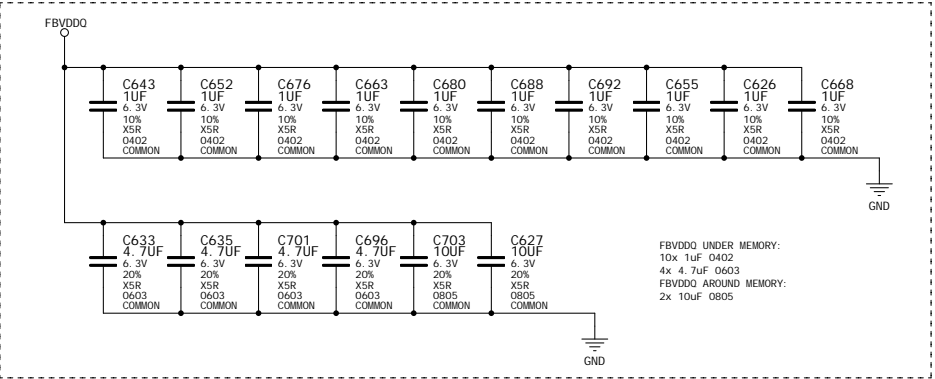




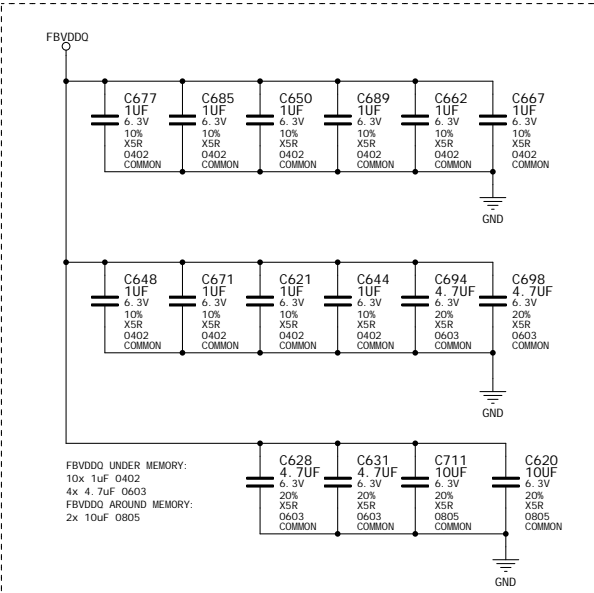
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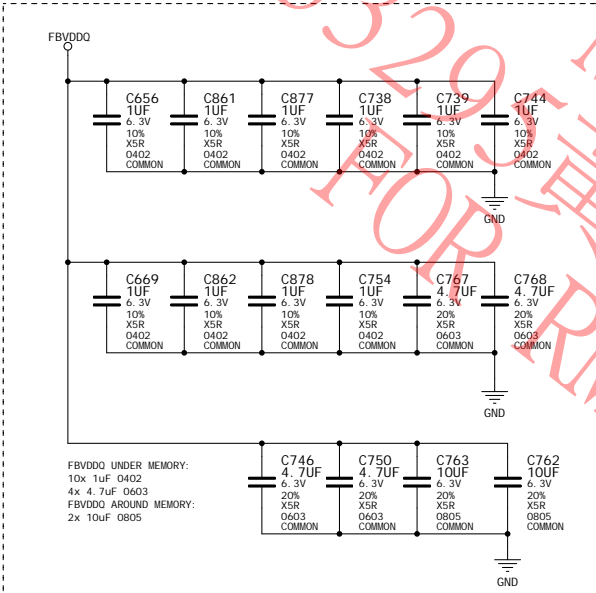
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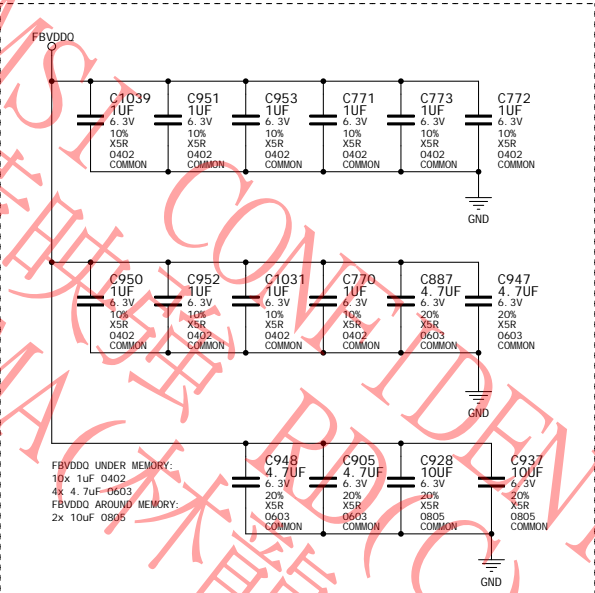
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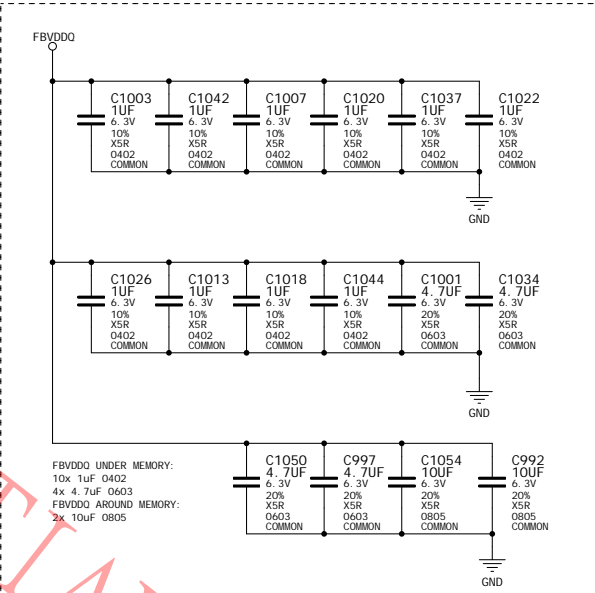
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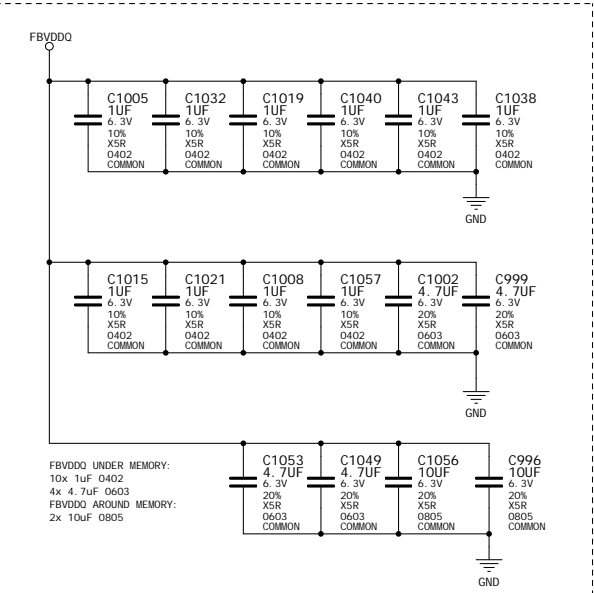
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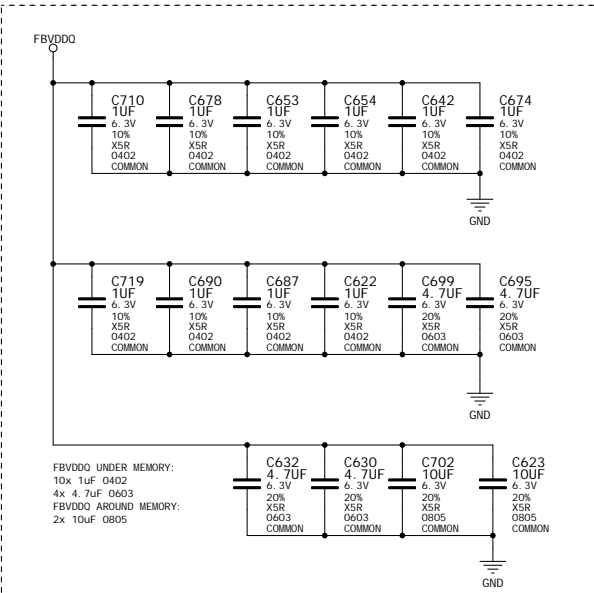
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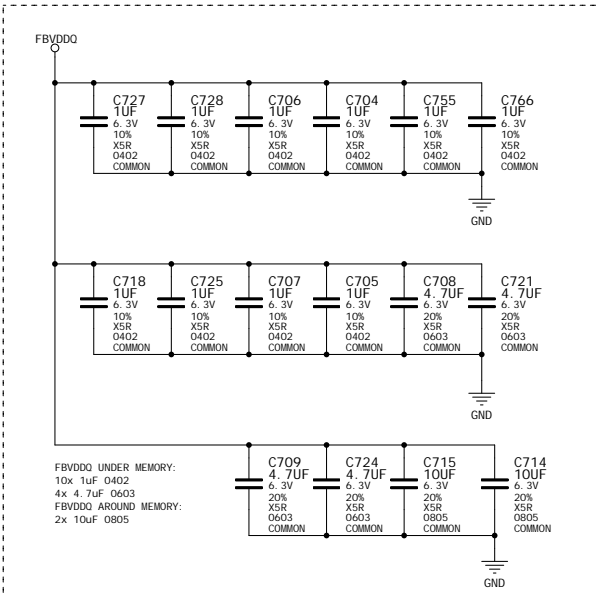
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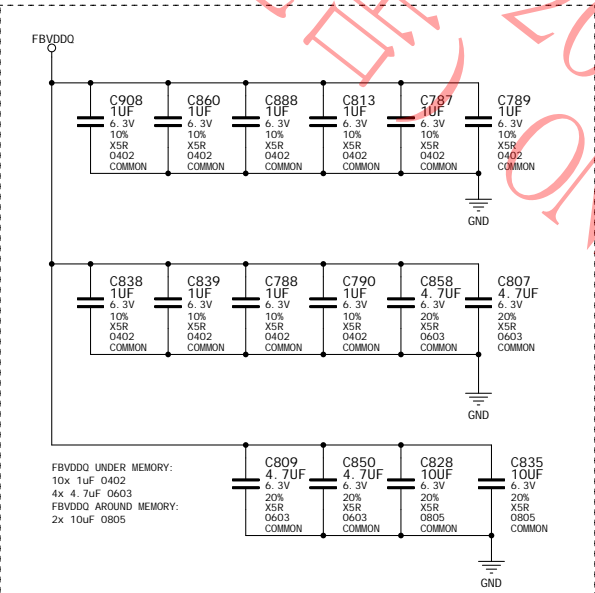
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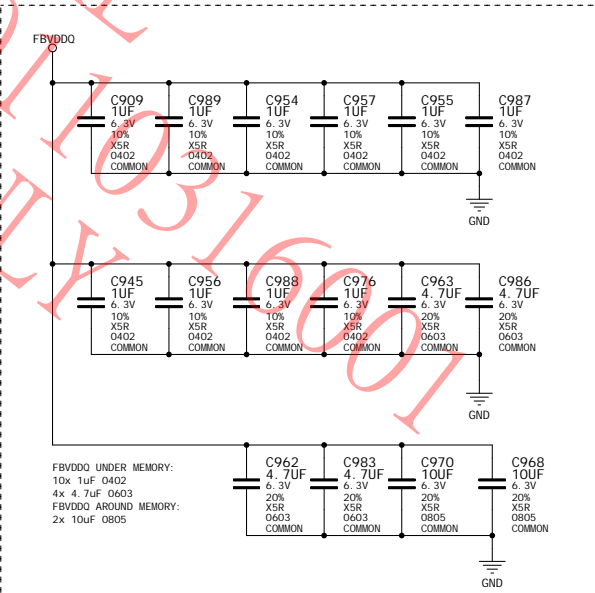
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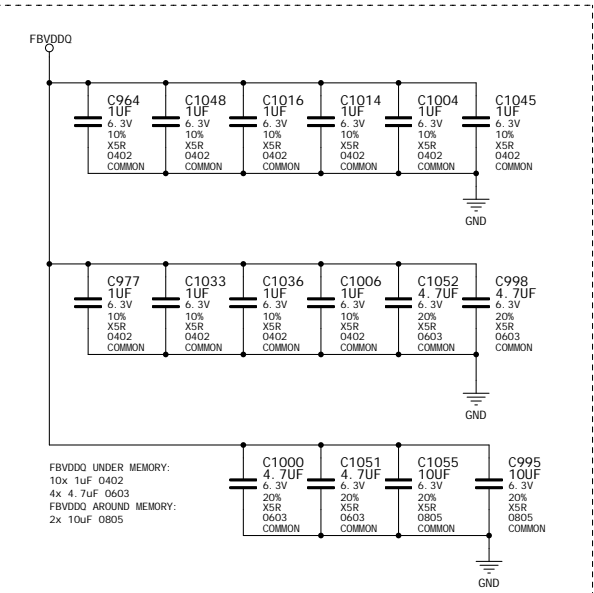
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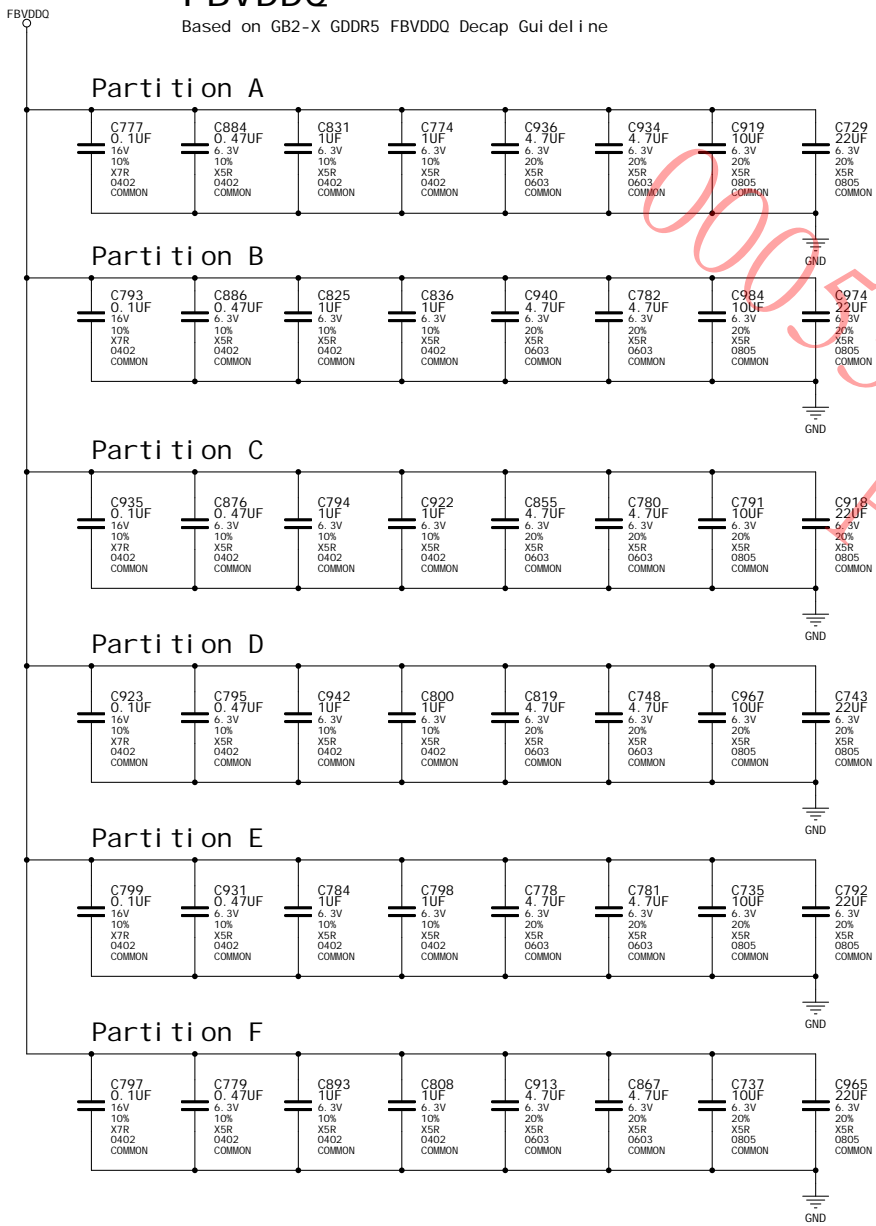


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ASSEMBLY	GF110-375 Dual DVI+mHDMI x32 GDDR5
PAGE DETAIL	GDDR5 Memory Decoupling

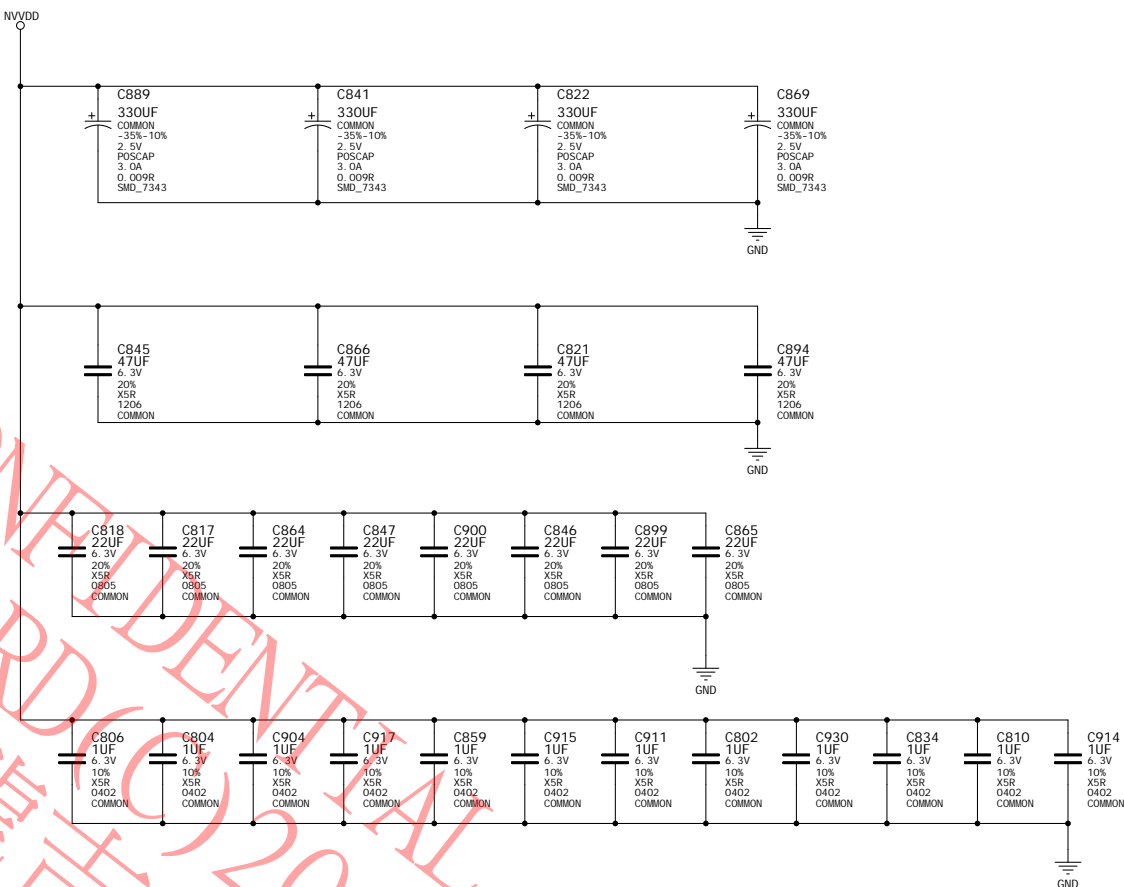
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PCB REV	P1261-A00
BOM REV	K
PAGE	13 OF 35
DATE	25-OCT-2010

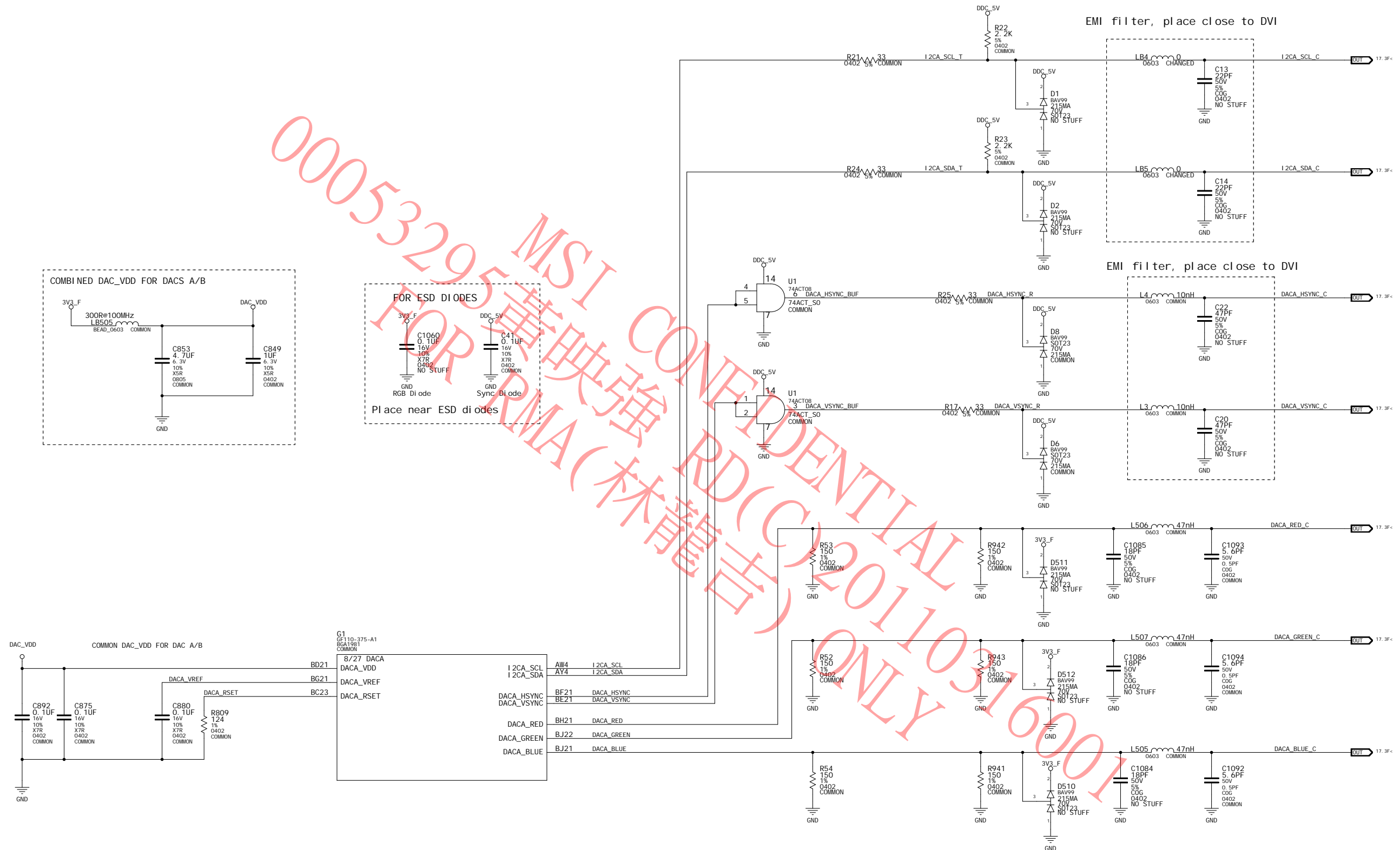
FBVDDQ
Based on GB2-X GDDR5 FBVDDQ Decap Gui del i ne

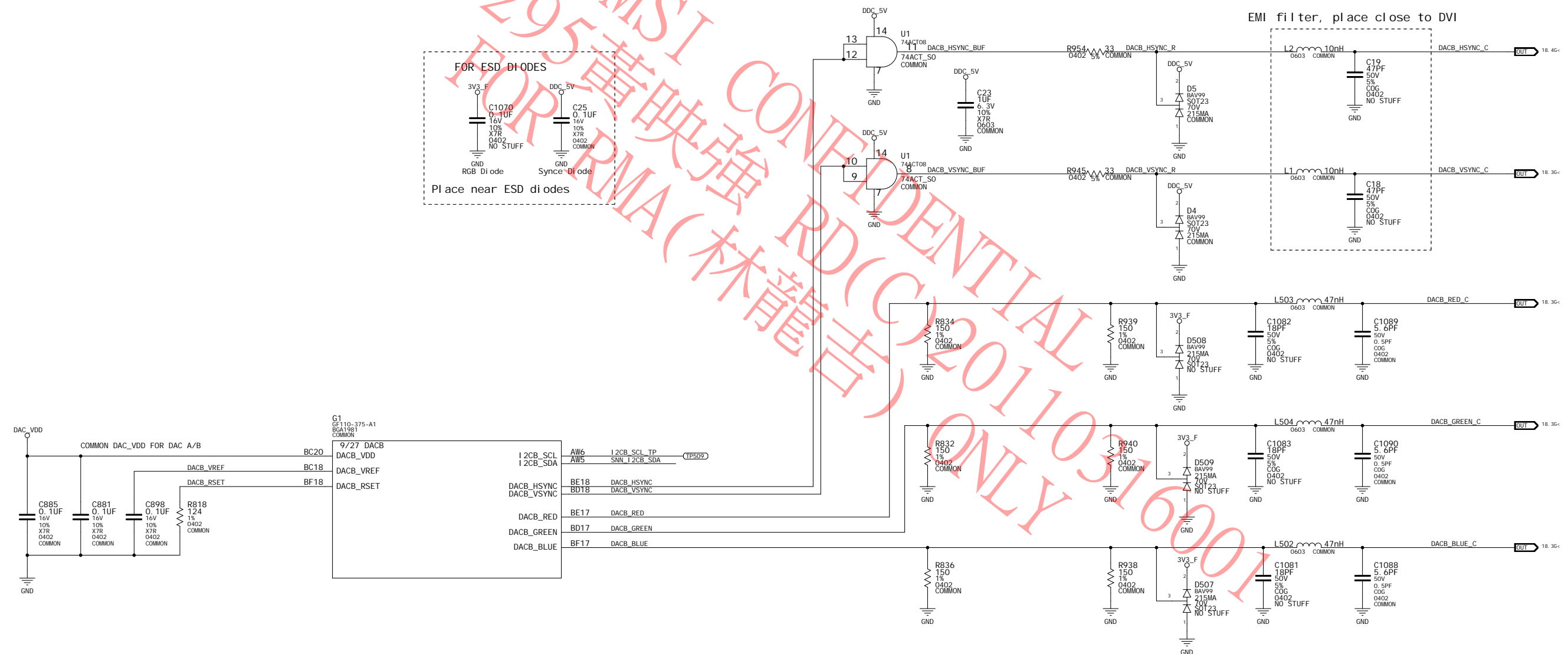


FBVDDQ under GPU
0.1uF 0402 X7R x6
0.47uF 0402 X5R x6
1uF 0402 X5R x12
FBVDDQ around GPU
4.7uF 0603 X5R x12
10uF 0805 X5R x6
22uF 0805 X5R x6

NVVDD decoupl i ng under GPU




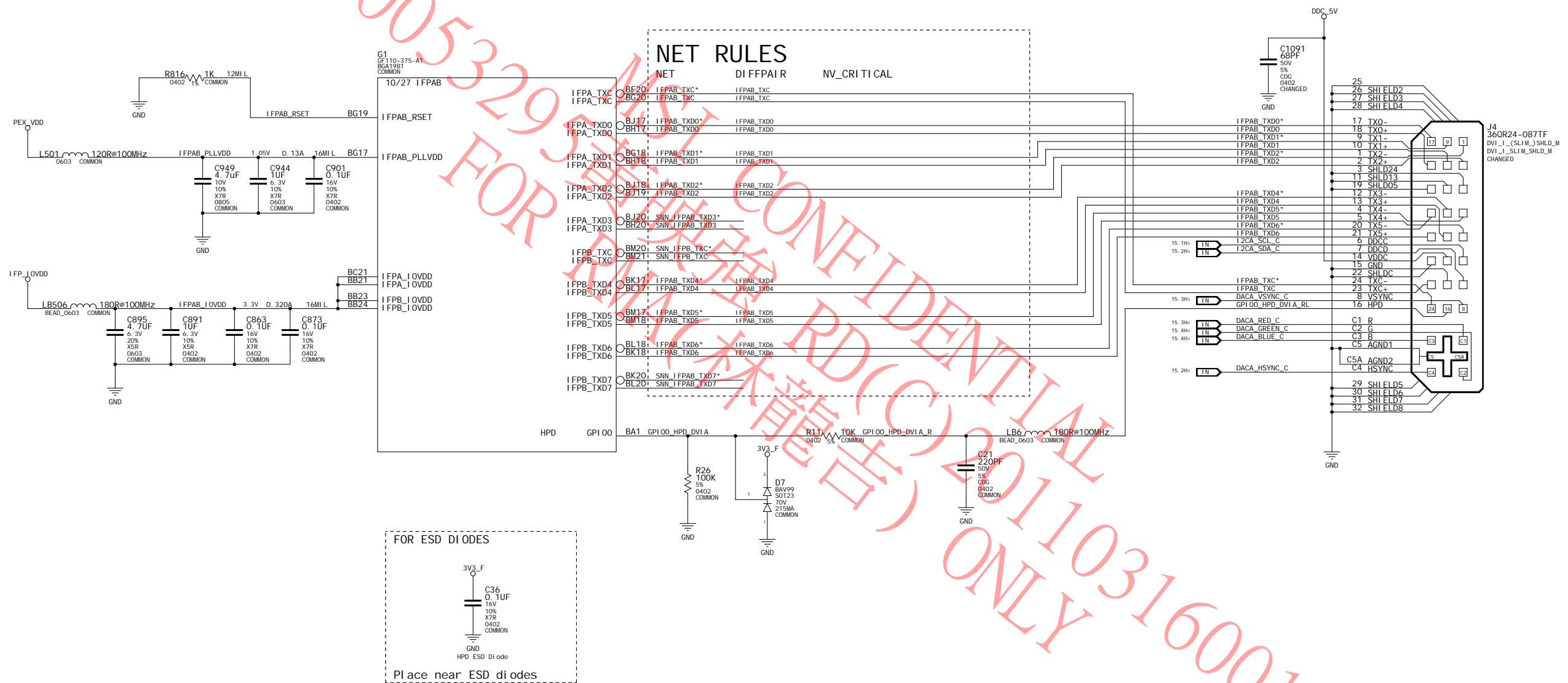


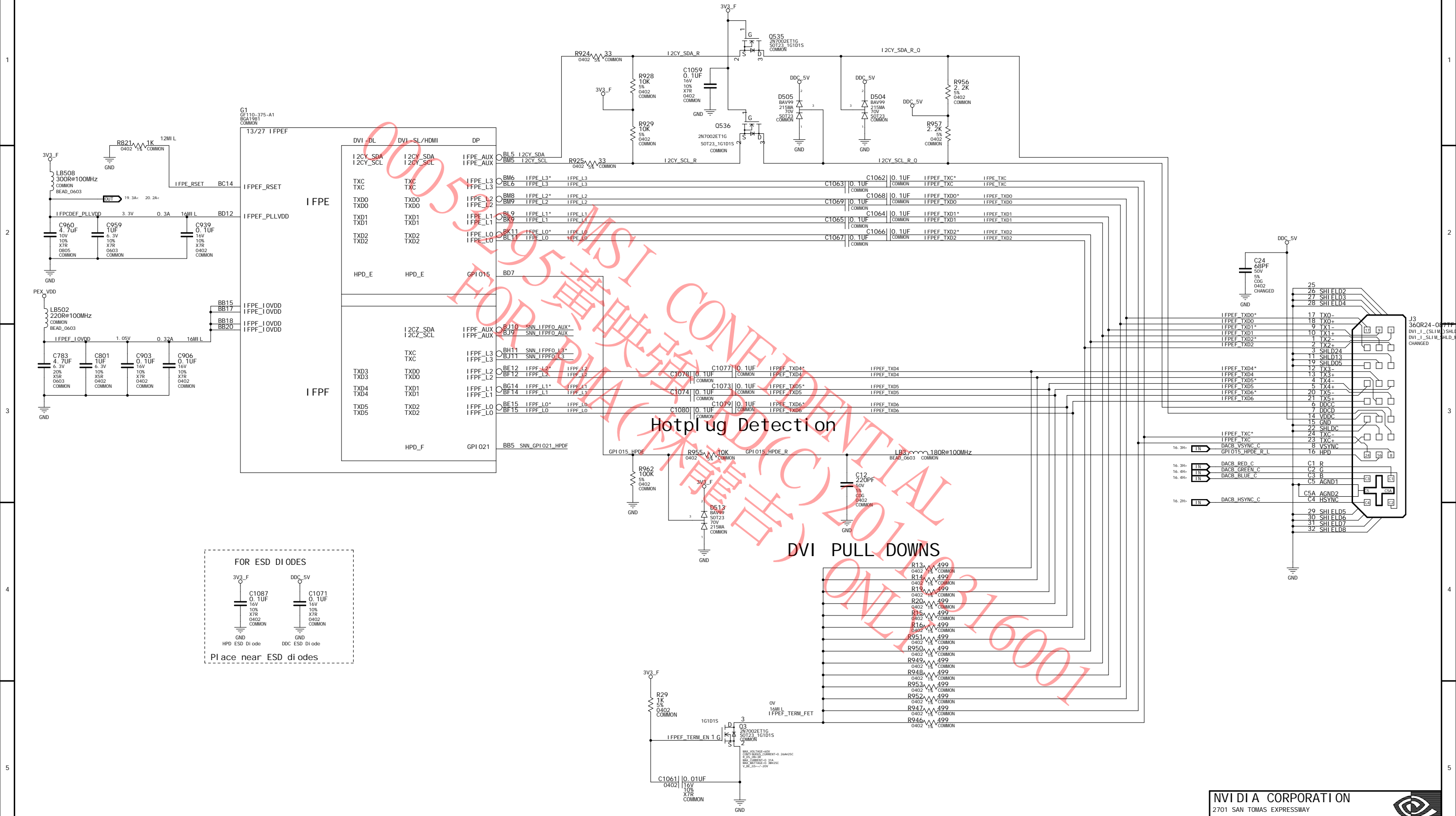


ASSEMBLY	GF110-375 Dual DVI +mHDMI x32 GDDR5
PAGE DETAIL	DAC_B for Mi d DVI-I

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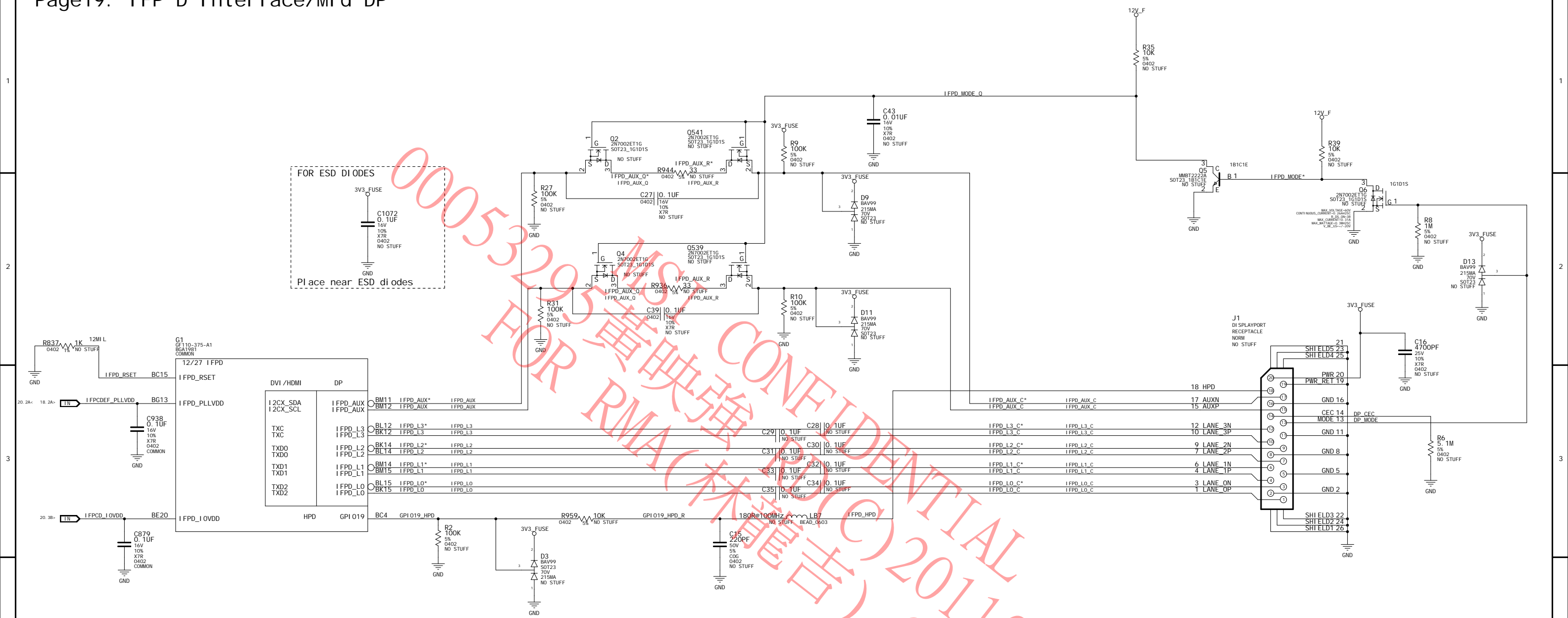
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PCB REV	T1261-A00	PAGE	16 OF 35
BOM REV	K	DATE	25-OCT-2010





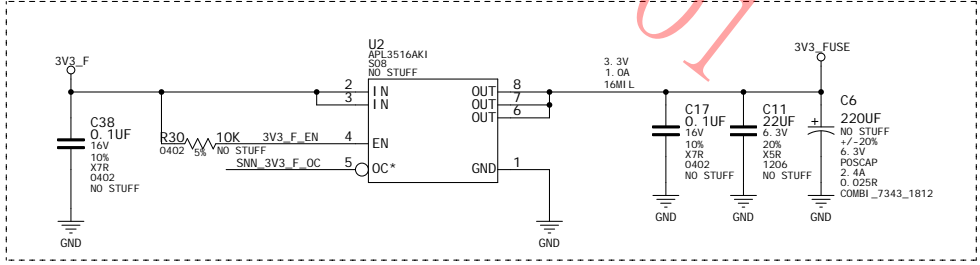
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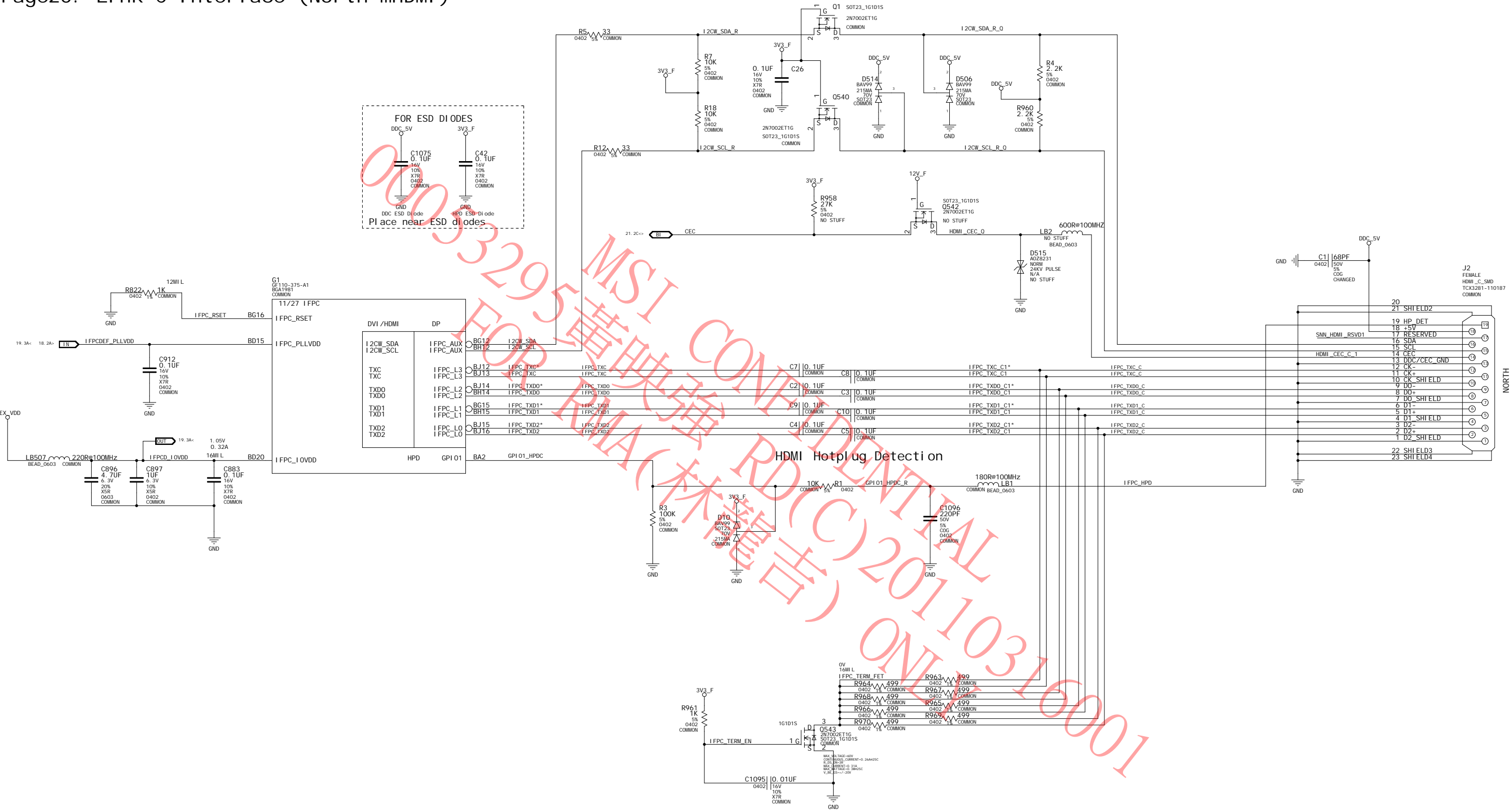
DP Hotplug Detection

3V3_DP_FUSE



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BOM REV	K	DATE	25-OCT-2010



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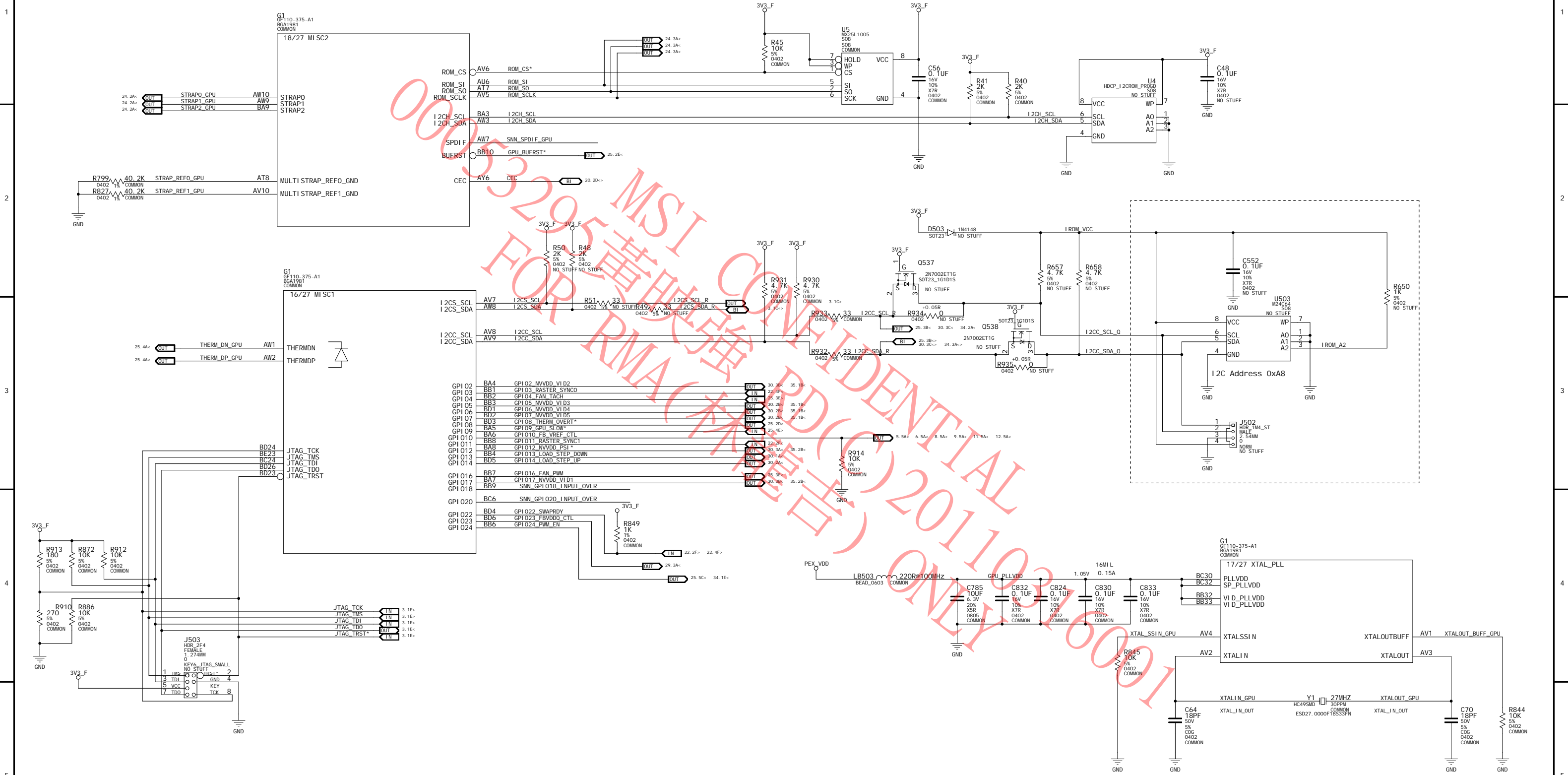
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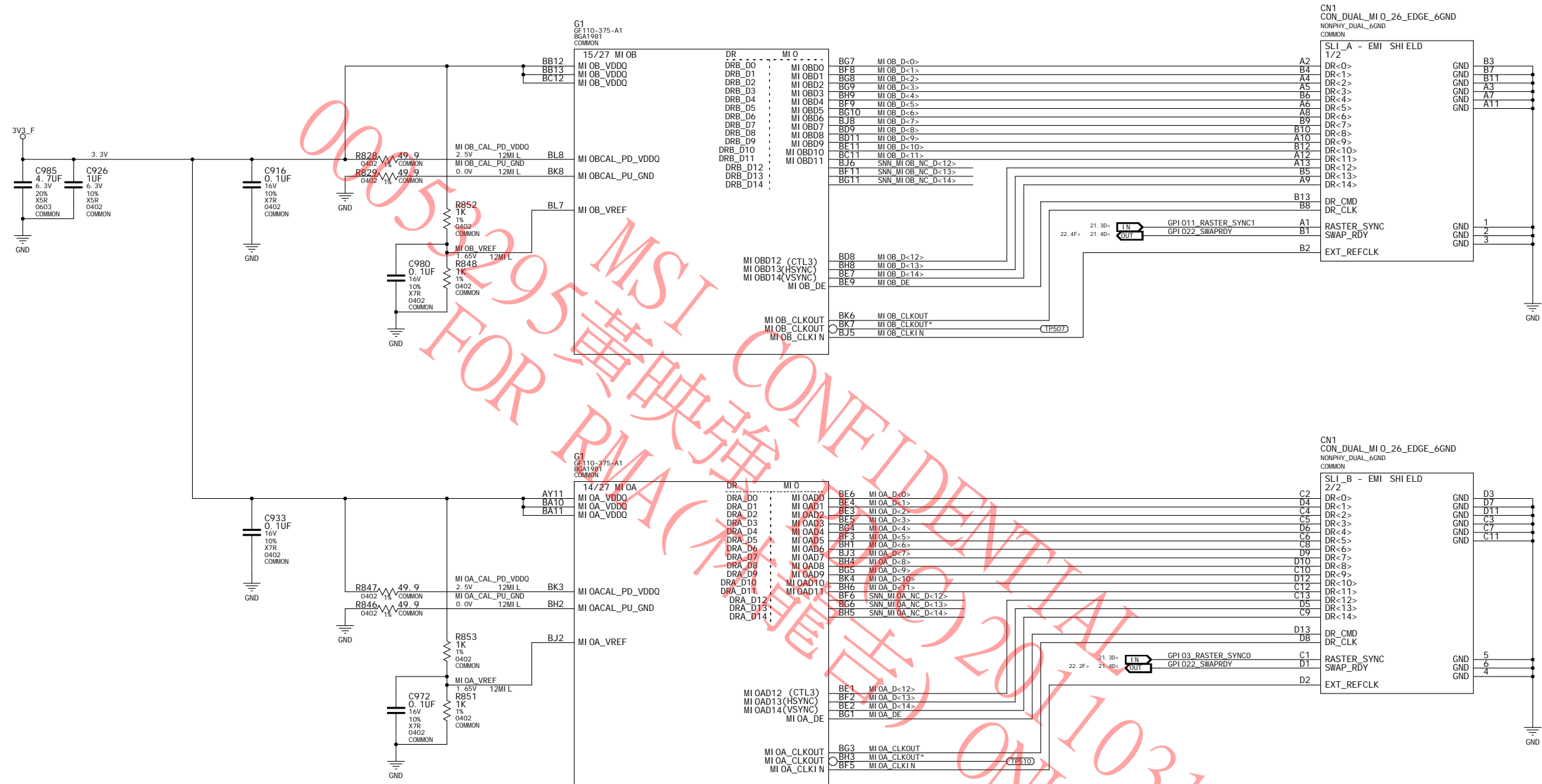


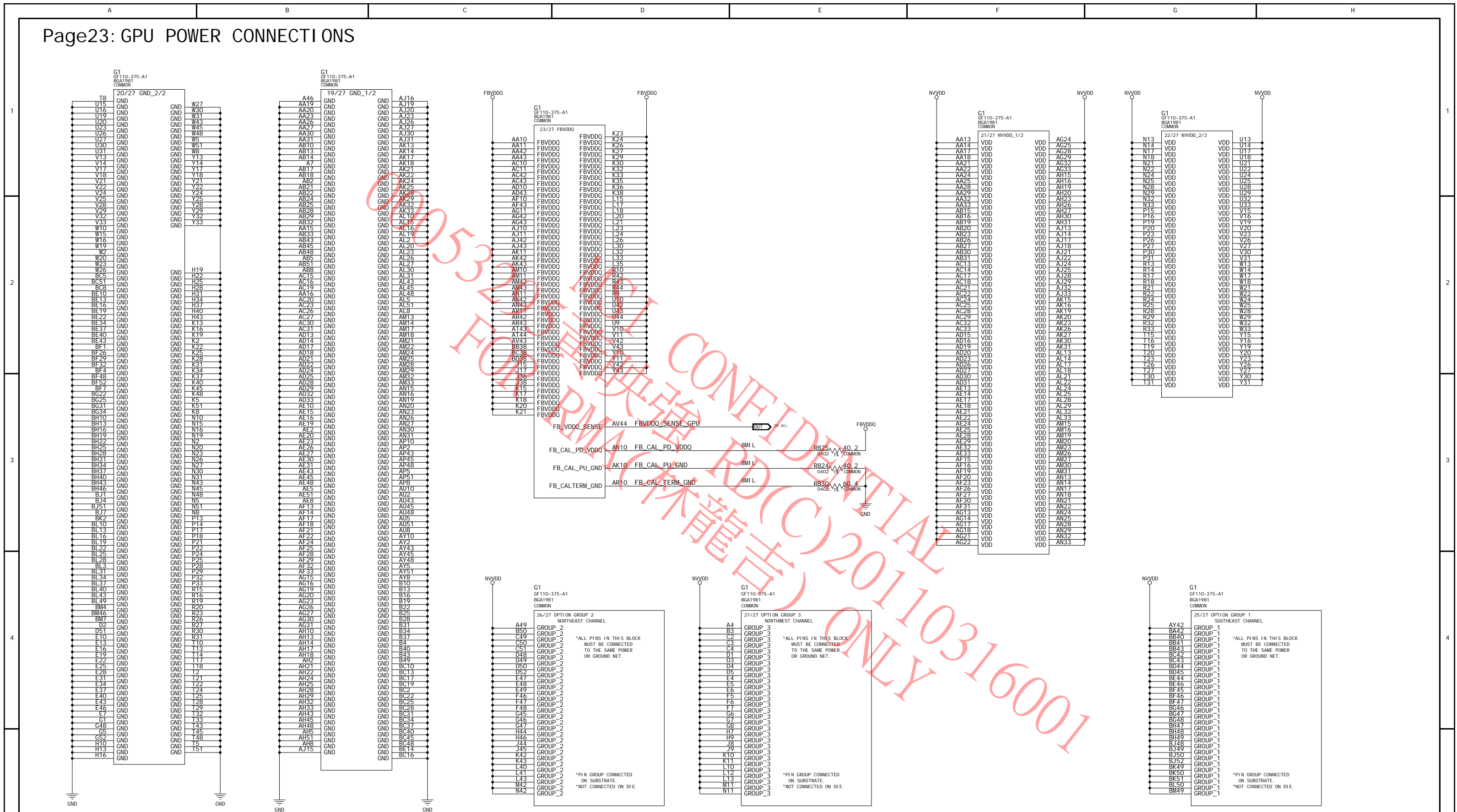
ASSEMBLY	GF110-375 Dual DVI+mHDMI x32 GDDR5
PAGE DETAIL	IFP C Interface (North mHDMI)

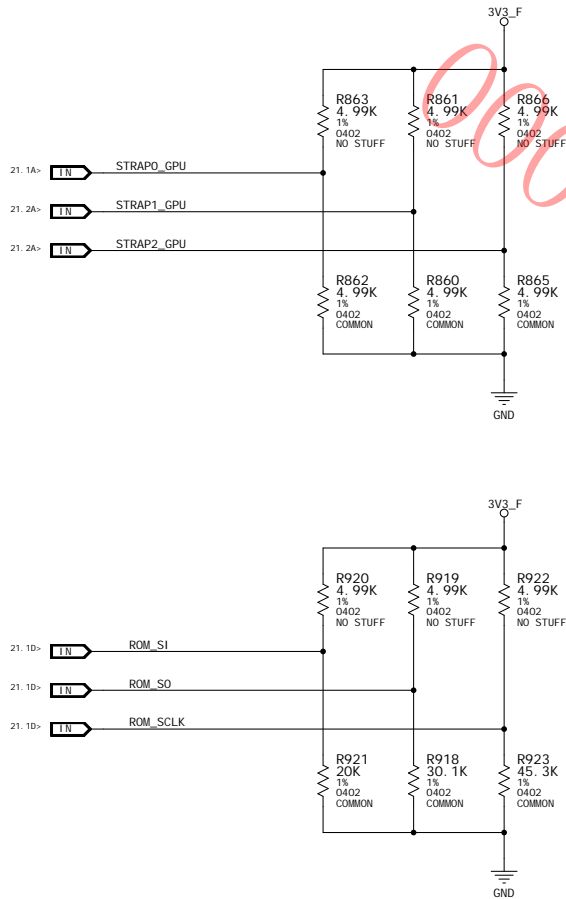
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PCB REV	P1261-A00	PAGE	20 OF 35
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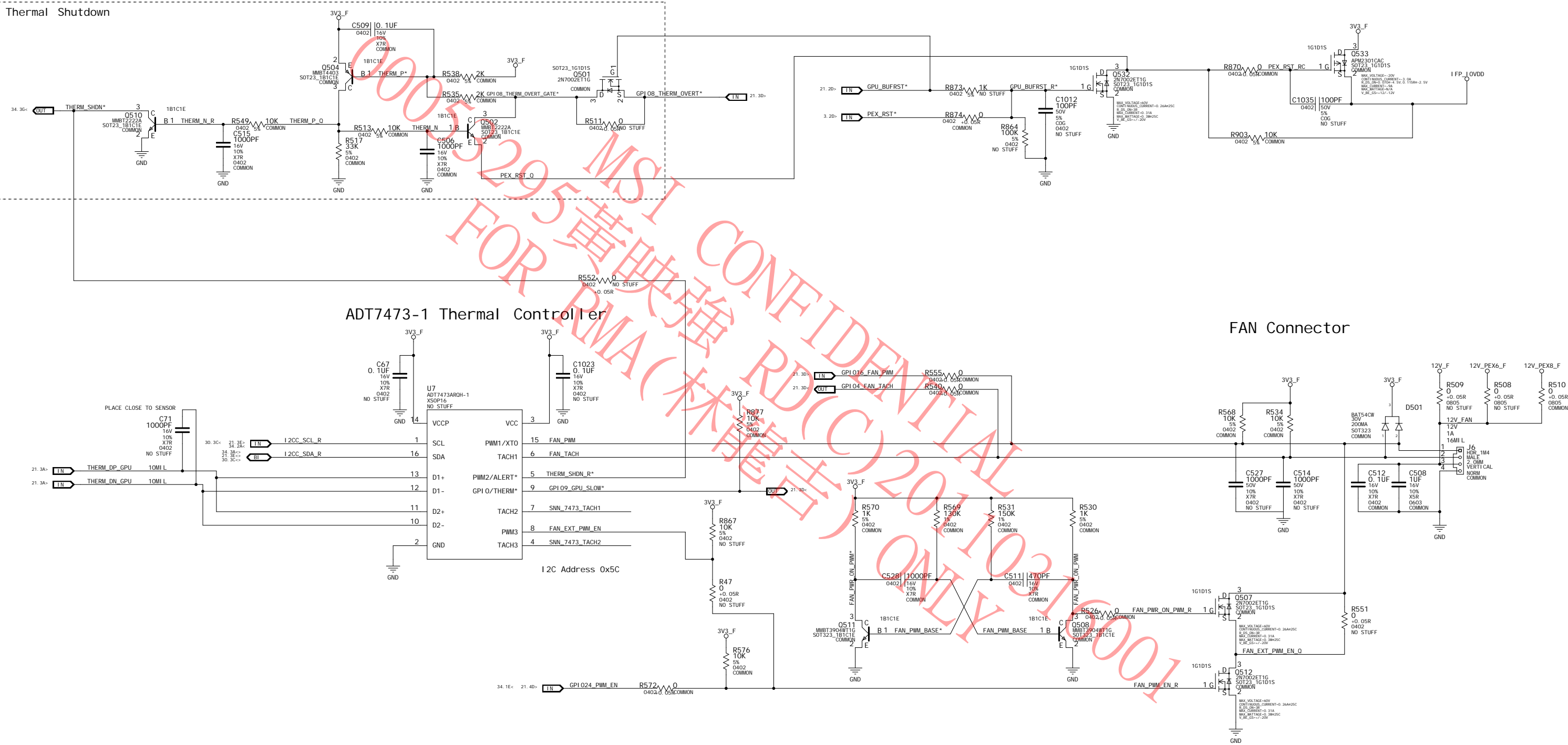




G1	
GF110-375-A1	
BGA1981	
COMMON	
24/27 NC/Spare	
SNN_G1_NC_1	BG2
SNN_G1_NC_2	BH7
SNN_G1_NC_3	BK5
SNN_G1_NC_4	BL4
SNN_G1_NC_5	BC35
SNN_G1_NC_6	BC33
SNN_G1_NC_7	BD14
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	NC_2
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	NC_5
	NC_6
	NC_7

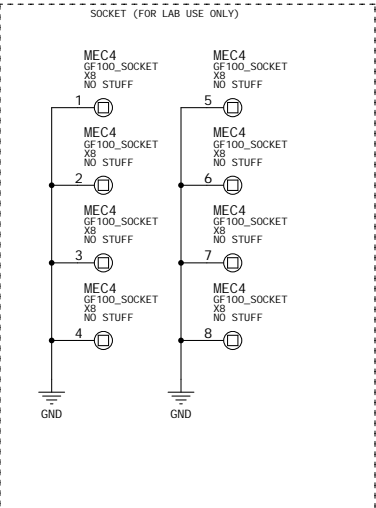
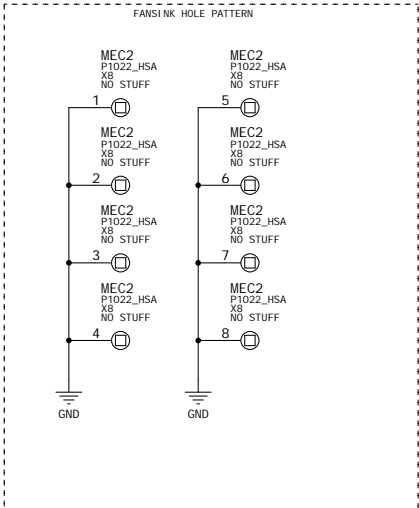
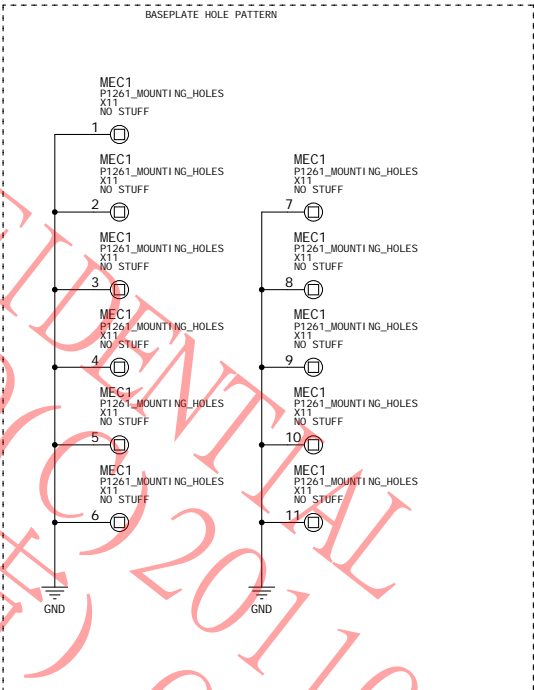
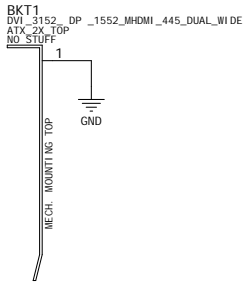
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STRAP1	3GIO_PADCFG_LUT_ADR	0000 : =>5K PD	0000 Desktop
STRAP2	PCI_DEVID [3:0]	0000 : =>5K PD	For 0x06C0
ROM_SI	RAMCFG[0]		0001 32Mx32 GDDR5 384-bit Qimonda 0010 32Mx32 GDDR5 384-bit Hynix 0011 32Mx32 GDDR5 384-bit Samsung
	RAMCFG[1]		
	RAMCFG[2]		0101 64Mx32 GDDR5 384-bit Qimonda 0110 64Mx32 GDDR5 384-bit Hynix 0111 64Mx32 GDDR5 384-bit Samsung
	RAMCFG[3]		
ROM_SO	VGA_DEVICE	1 FOR GPU0	
	SMB_ALT_ADDR	0	
	FB[0]_BAR_SIZE	1	
	XCLK_417	0	
ROM_SCLK	PEX_PLL_EN_TERM100	1 ENABLED	
	SLOT_CLK_CFG	1 ENABLED	45K PD
	SUB_VENDOR	1 Dedicated BIOS	
	PCI_DEVID_EXT	0 0xC	

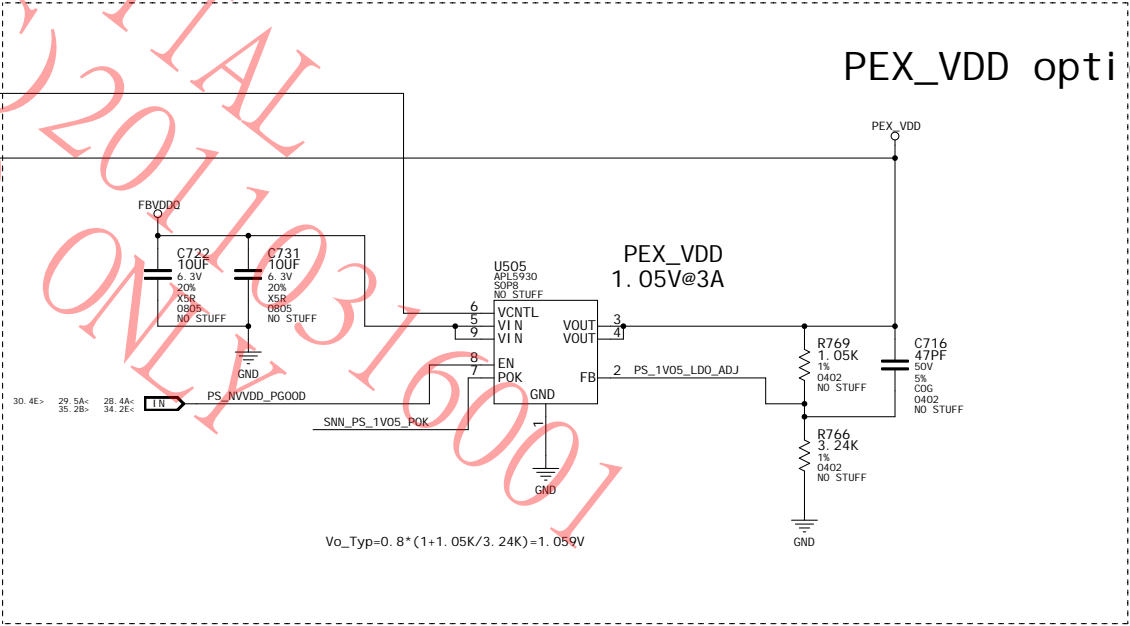
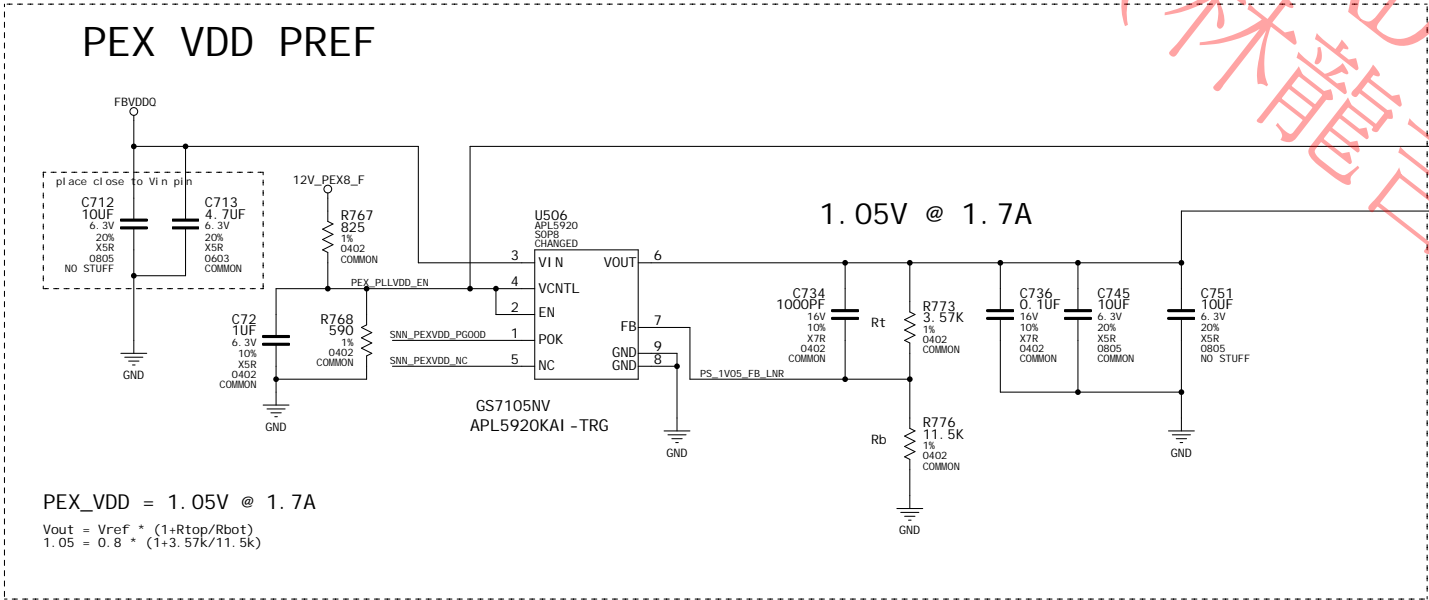
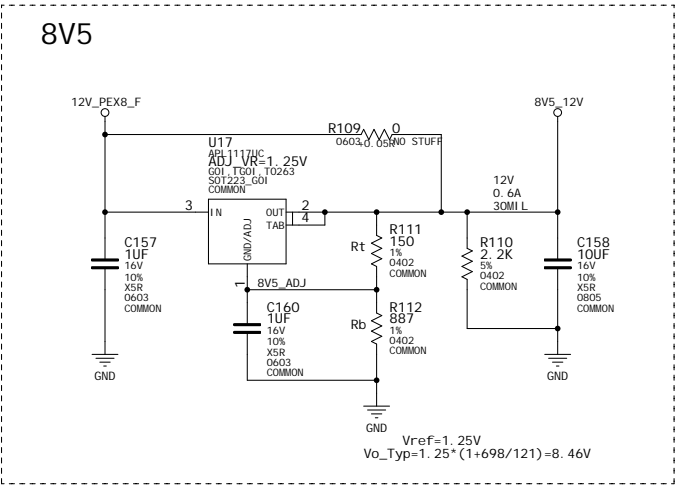
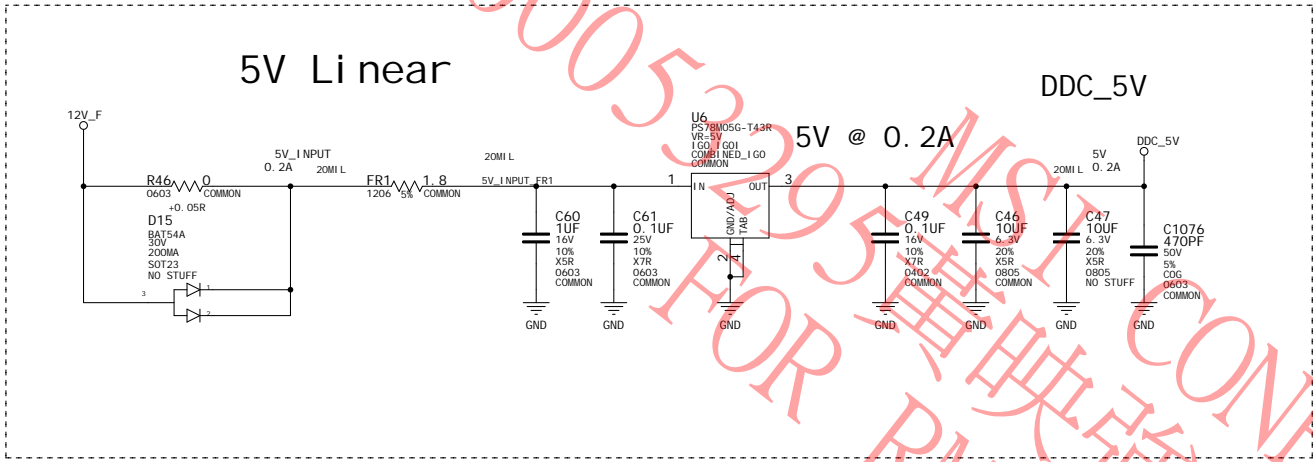
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

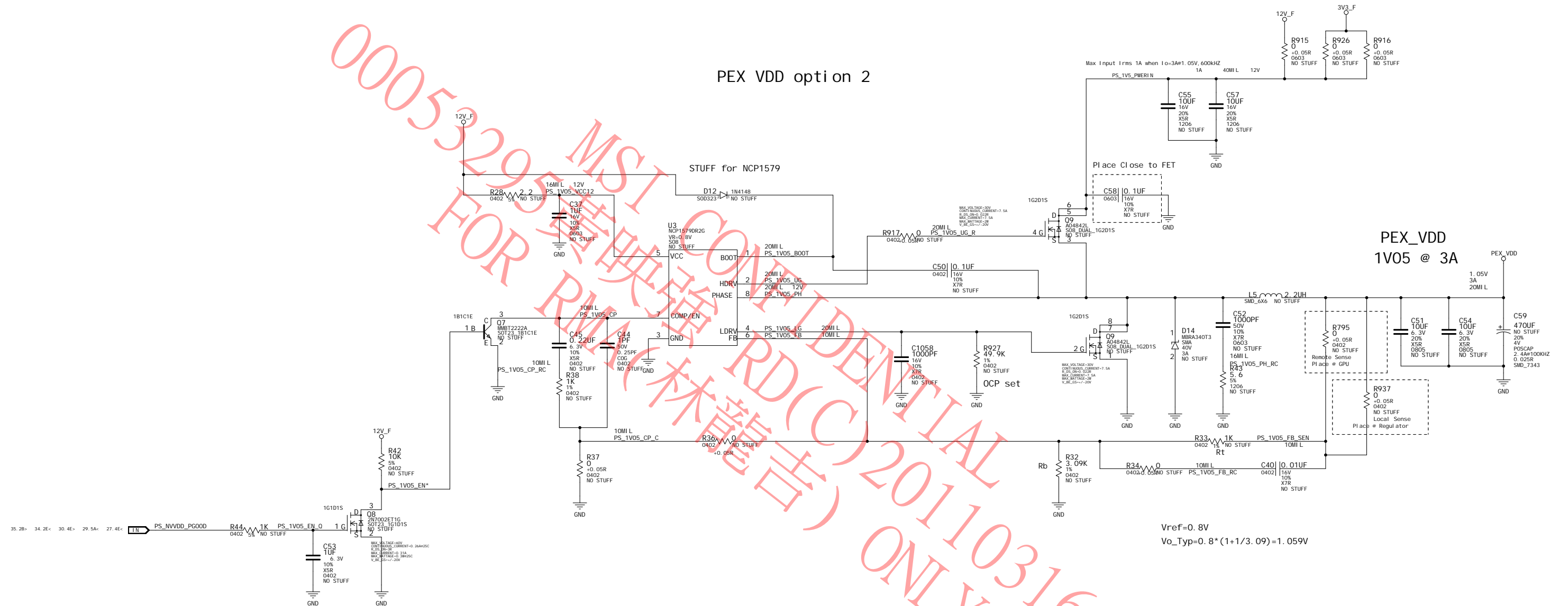


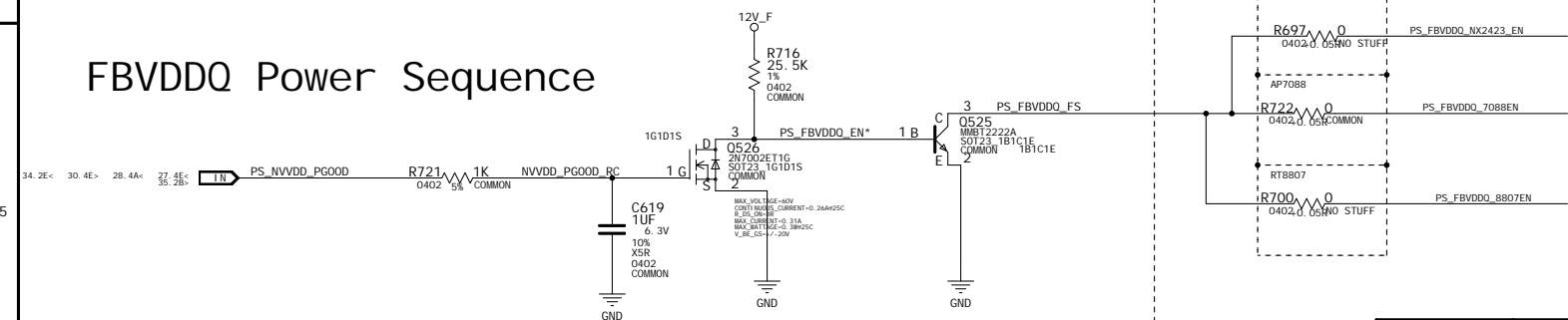
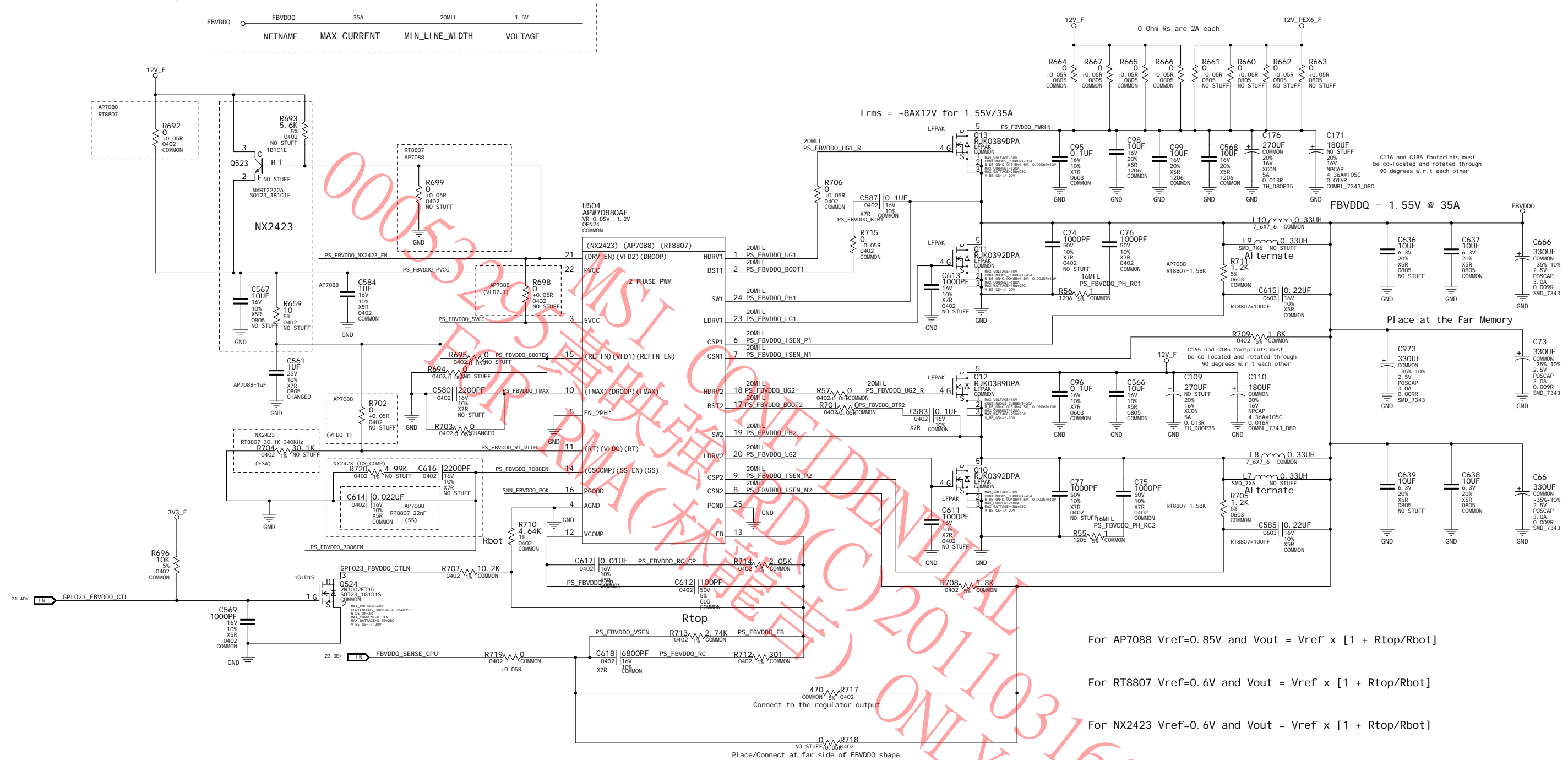
Brackets:

- 151-10001-0352-071 DVI , DVI , mHDMI
- 151-10001-0353-071 DVI , DP, mHDMI



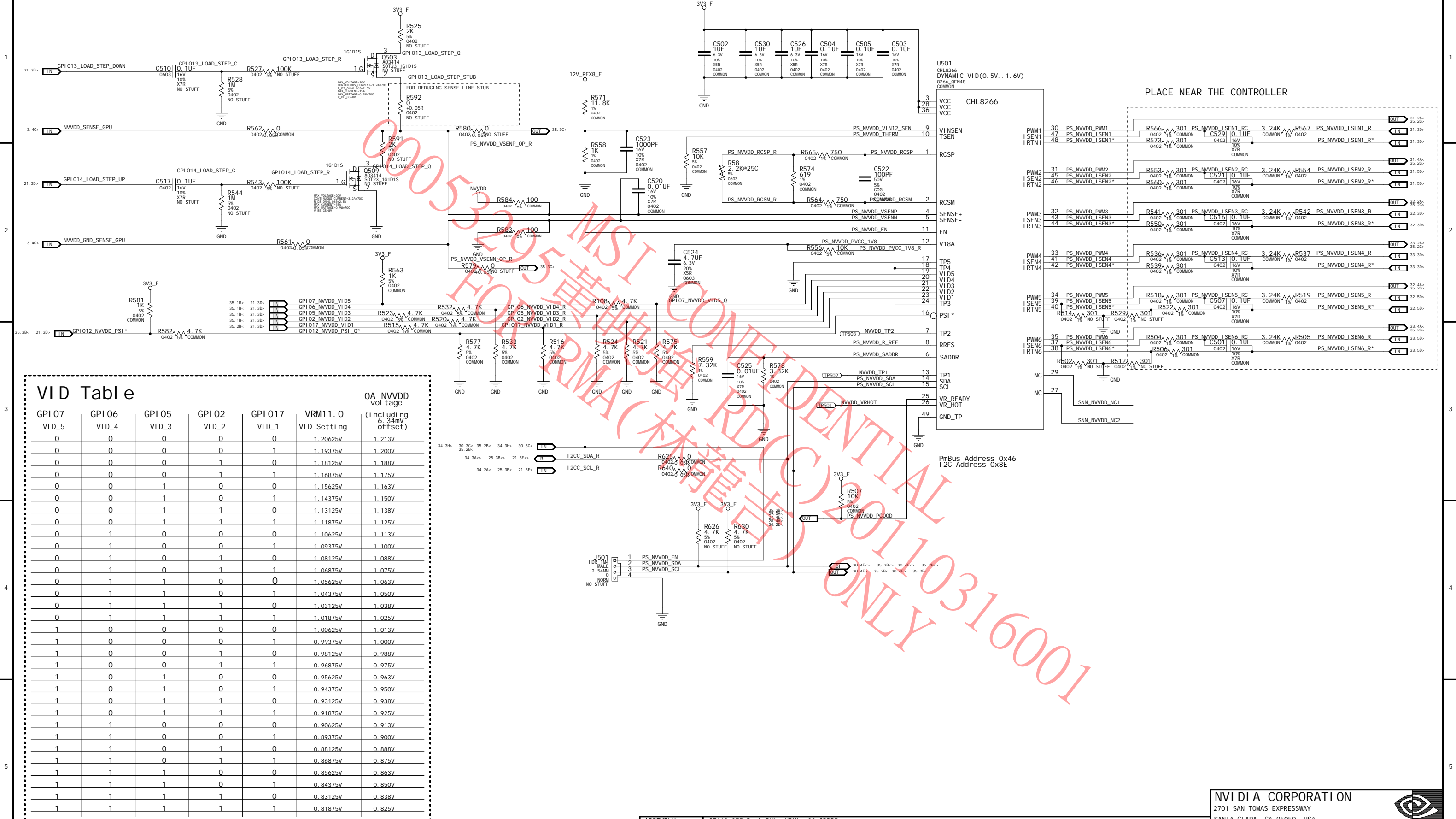






GPI 023	FBVDDQ Voltage Typical	FBVDDQ Calculation for AQP7088	1/Rbot = 1/4.64K + 1/10.2K = 3.19K
0	1.35V (Low perfmode)	$R_{bot} = 4.64K$ $R_{top} = 2.74K$ $FBVDDQ = 0.85V * [1 + 2.74K / 4.64] = 1.350V$	
1	1.58V (3D)	$R_{bot} = 4.64K 10.2K = 3.19K$ $R_{top} = 2.74K$ $FBVDDQ = 0.85V * [1 + 2.74K / 3.19K] = 1.580V$	

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PCB REV	P1261-A00	PAGE	29 OF 35
BOM REV	K	DATE	25-OCT-2010



VID Table

GPI 07 VID_5	GPI 06 VID_4	GPI 05 VID_3	GPI 02 VID_2	GPI 017 VID_1	VRM11.0 VID Setting	OA NVVDD voltage (including 6.34mV offset)
0	0	0	0	0	1.20625V	1.213V
0	0	0	0	1	1.19375V	1.200V
0	0	0	1	0	1.18125V	1.188V
0	0	0	1	1	1.16875V	1.175V
0	0	1	0	0	1.15625V	1.163V
0	0	1	0	1	1.14375V	1.150V
0	0	1	1	0	1.13125V	1.138V
0	0	1	1	1	1.11875V	1.125V
0	1	0	0	0	1.10625V	1.113V
0	1	0	0	1	1.09375V	1.100V
0	1	0	1	0	1.08125V	1.088V
0	1	0	1	1	1.06875V	1.075V
0	1	1	0	0	1.05625V	1.063V
0	1	1	0	1	1.04375V	1.050V
0	1	1	1	0	1.03125V	1.038V
0	1	1	1	1	1.01875V	1.025V
1	0	0	0	0	1.00625V	1.013V
1	0	0	0	1	0.99375V	1.000V
1	0	0	1	0	0.98125V	0.988V
1	0	0	1	1	0.96875V	0.975V
1	0	1	0	0	0.95625V	0.963V
1	0	1	0	1	0.94375V	0.950V
1	0	1	1	0	0.93125V	0.938V
1	0	1	1	1	0.91875V	0.925V
1	1	0	0	0	0.90625V	0.913V
1	1	0	0	1	0.89375V	0.900V
1	1	0	1	0	0.88125V	0.888V
1	1	0	1	1	0.86875V	0.875V
1	1	1	0	0	0.85625V	0.863V
1	1	1	0	1	0.84375V	0.850V
1	1	1	1	0	0.83125V	0.838V
1	1	1	1	1	0.81875V	0.825V

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ASSEMBLY	GF110-375 Dual DVI+mHDMI x32 GDDR5
PAGE DETAIL	Power Supply: NVVDD Controller

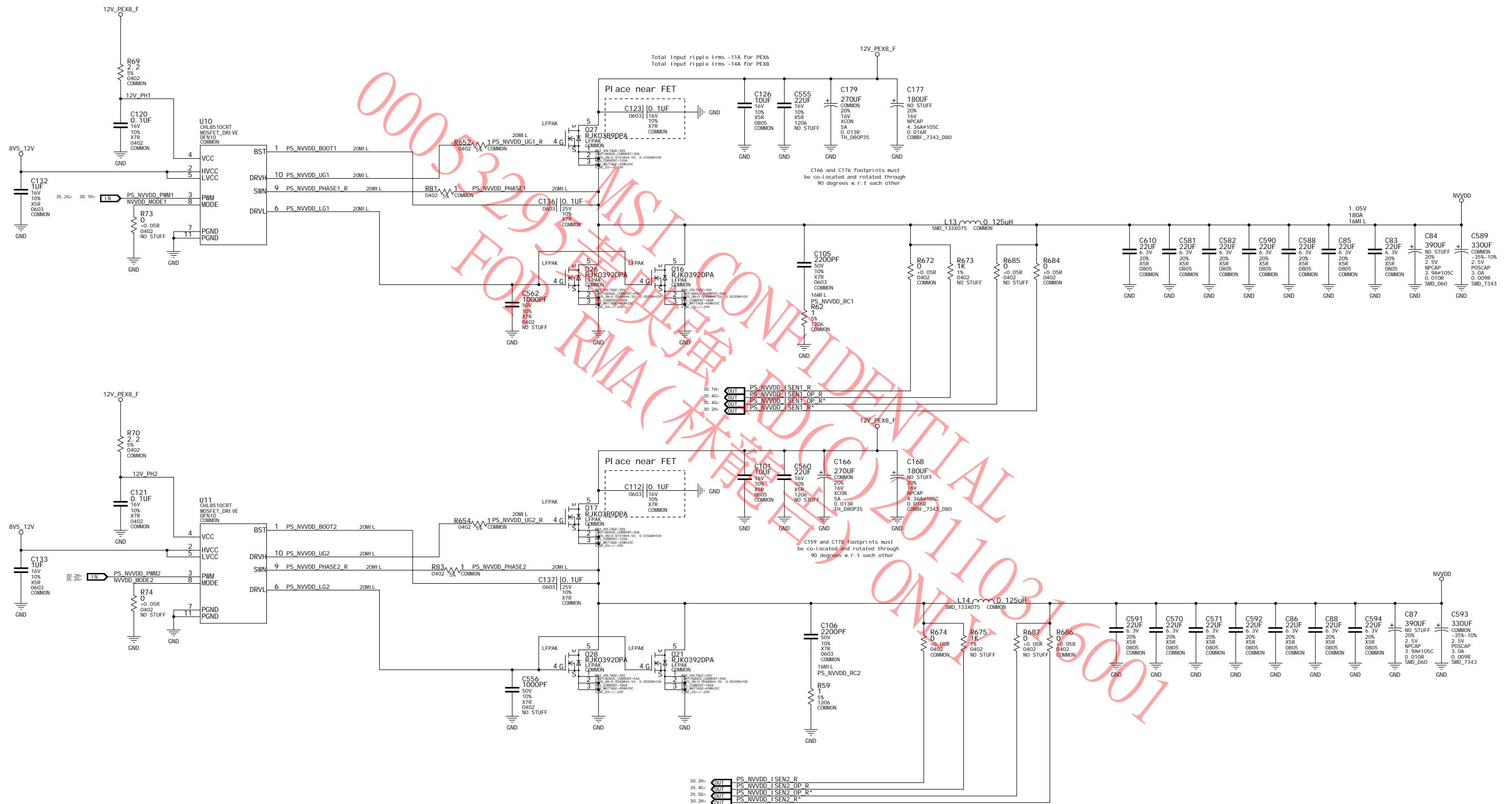
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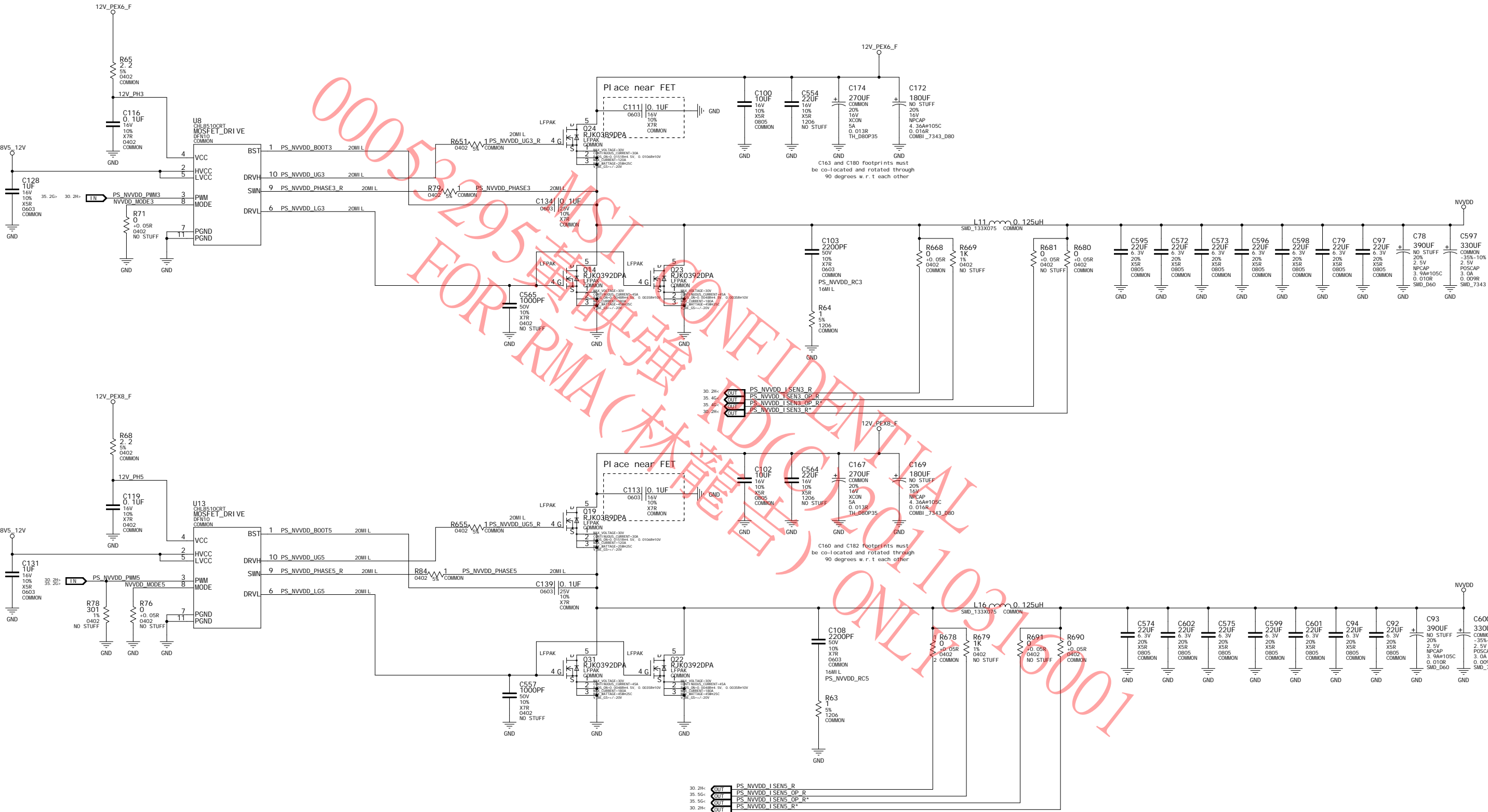
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PCB REV	P1261-A00	PAGE	30 OF 35
BOM REV	K	DATE	25-OCT-2010

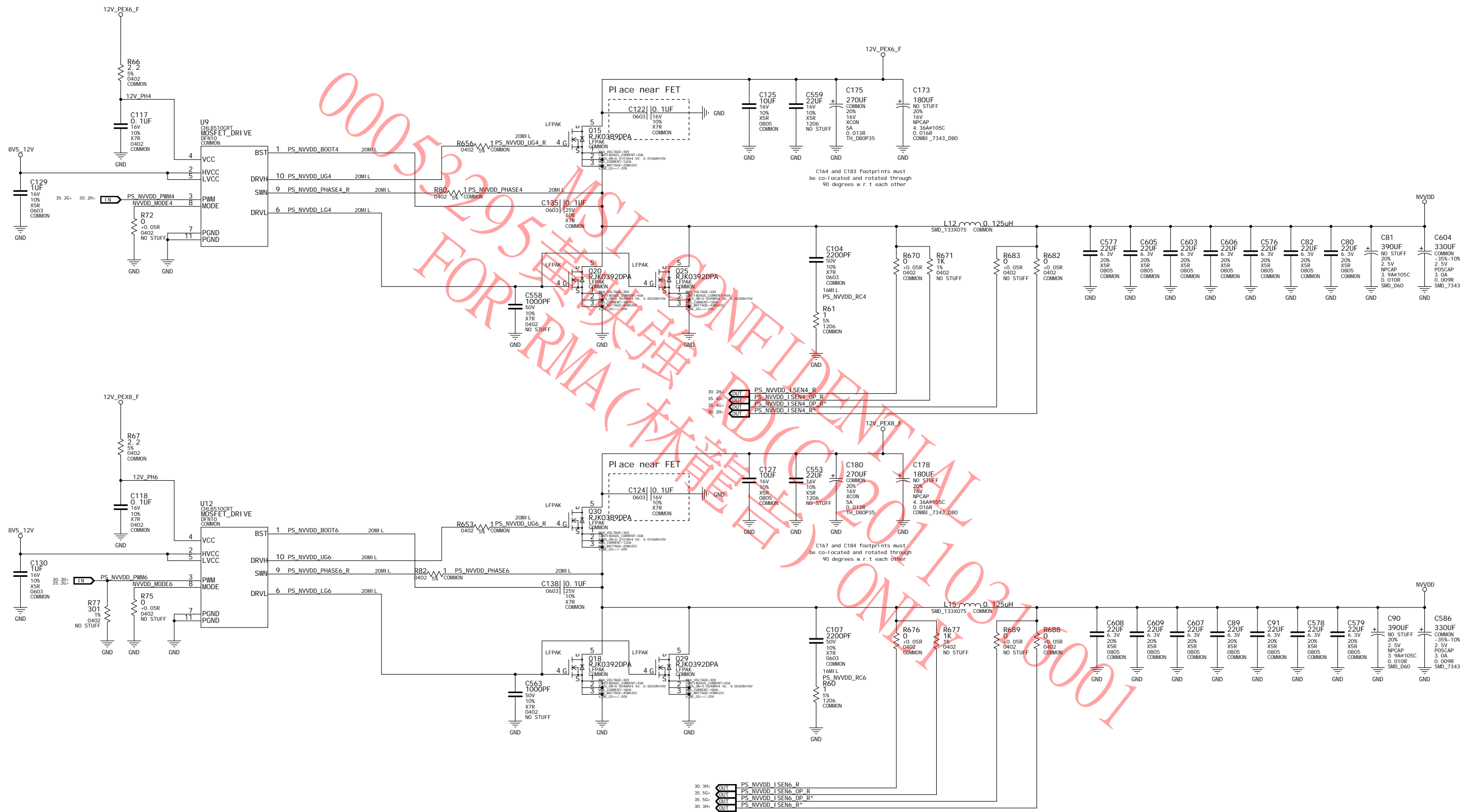




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ASSEMBLY	GF110-375 Dual DVI+mHDMI x32 GDDR5
PAGE DETAIL	Power Supply: NVVDD Phase 3 & 5 of 6

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BOM REV	Andy Stavros
PAGE	32 OF 35
DATE	25-OCT-2010



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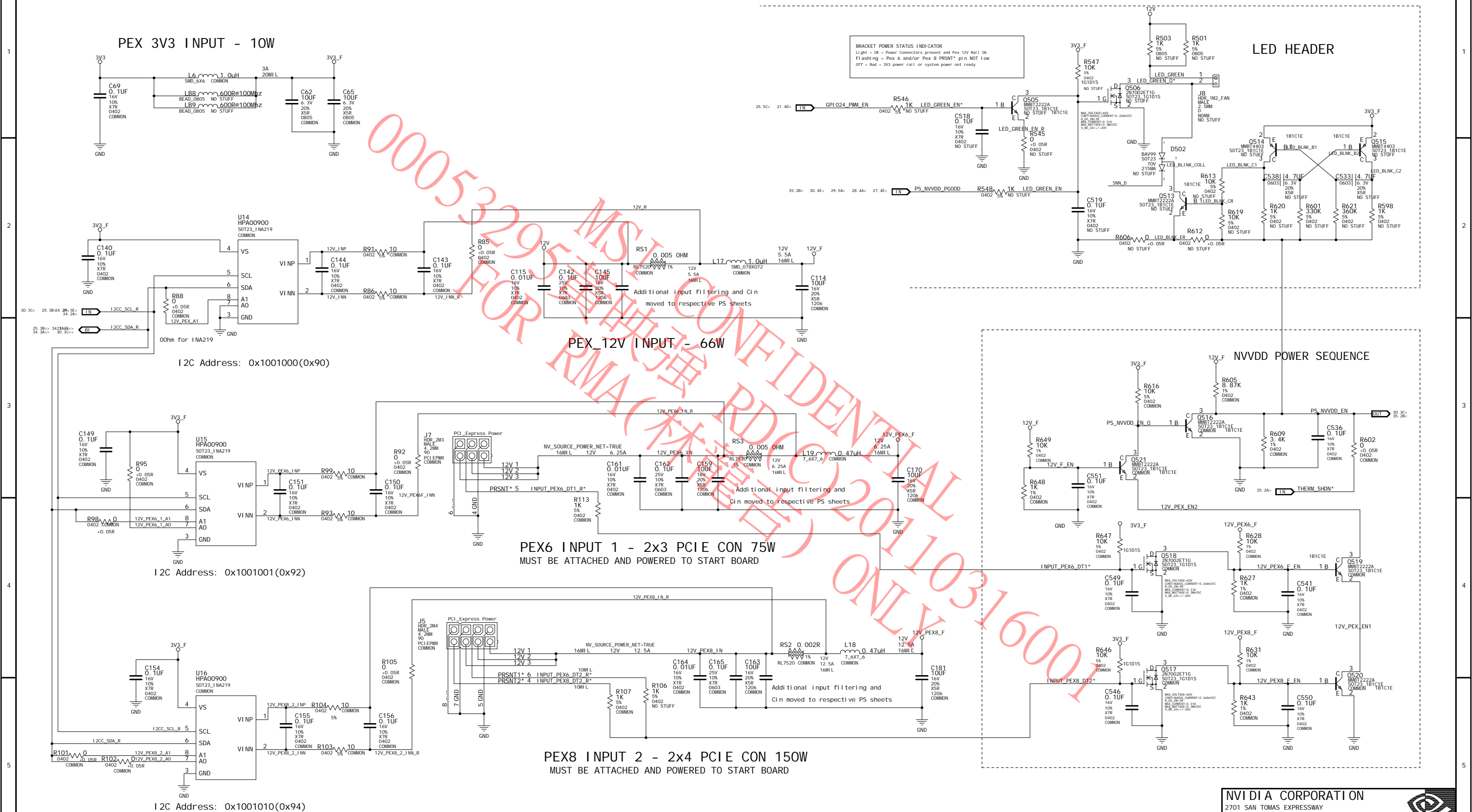
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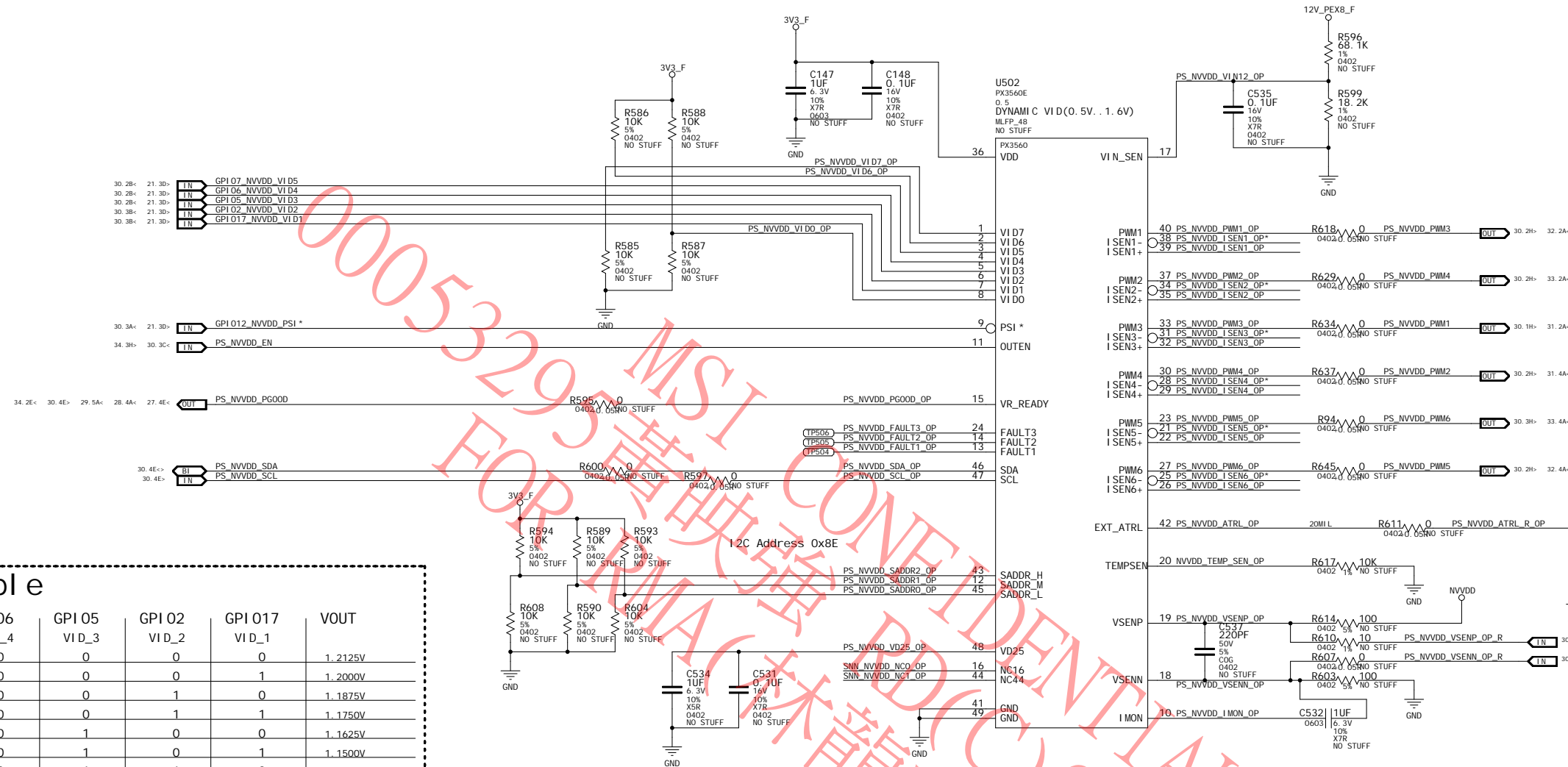
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BOM REV Andy Stavros

PAGE 33 OF 35

DATE 25-OCT-2010

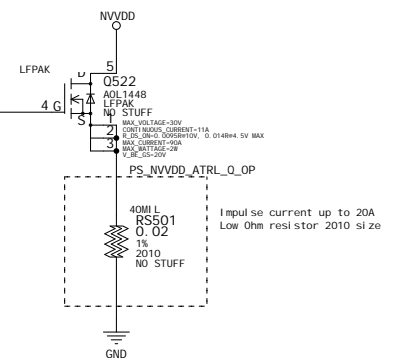




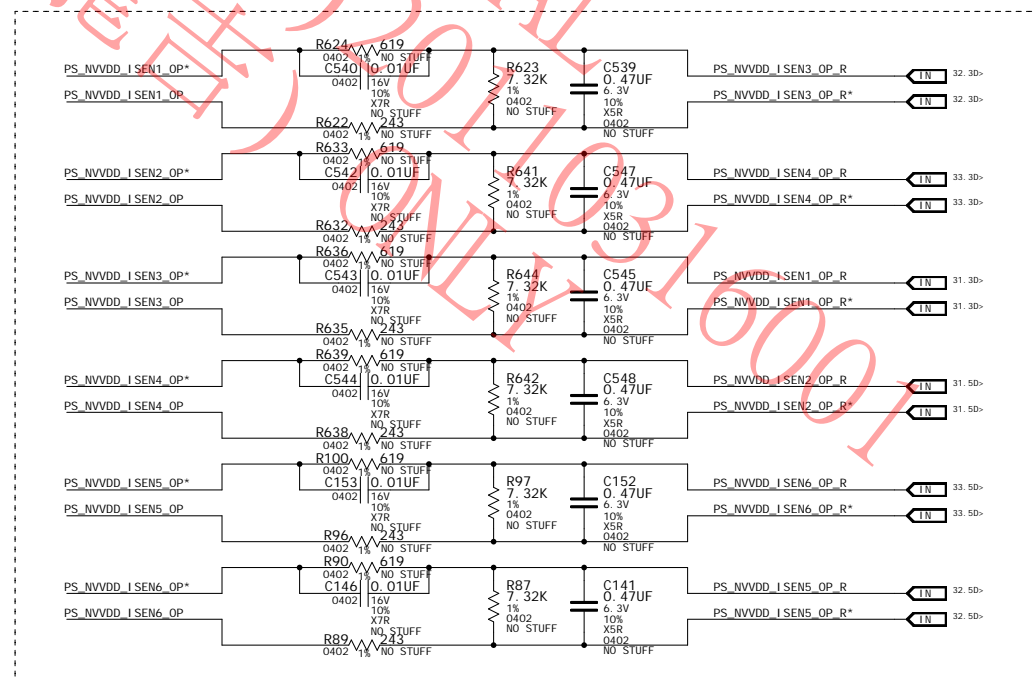
VI D Tabl e

GPI 07 VID_5	GPI 06 VID_4	GPI 05 VID_3	GPI 02 VID_2	GPI 017 VID_1	VOUT
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

EXTERNAL ATR CIRCUIT



PLACE FET AT THE POWER SUPPLY OUTPUT



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PCB REV	P1261-A00	PAGE	35 OF 35
BOM REV	K	DATE	25-OCT-2010

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