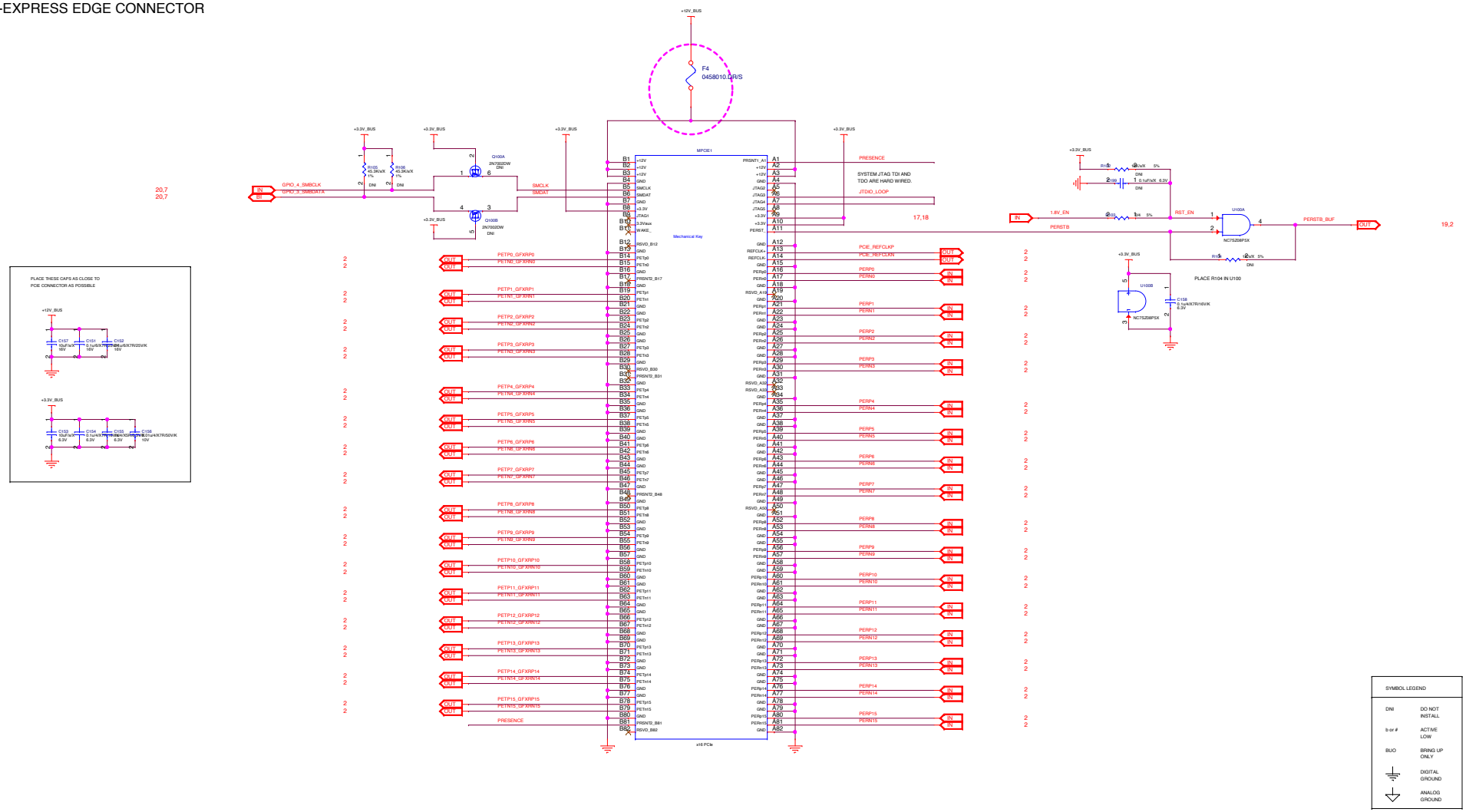
(1) PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
b or #	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

GIGABYTE		
PCIE EDGE CONNECTOR		
Size: Custom	Document Number: GV-R927XOC-2GD	Rev: 1.02
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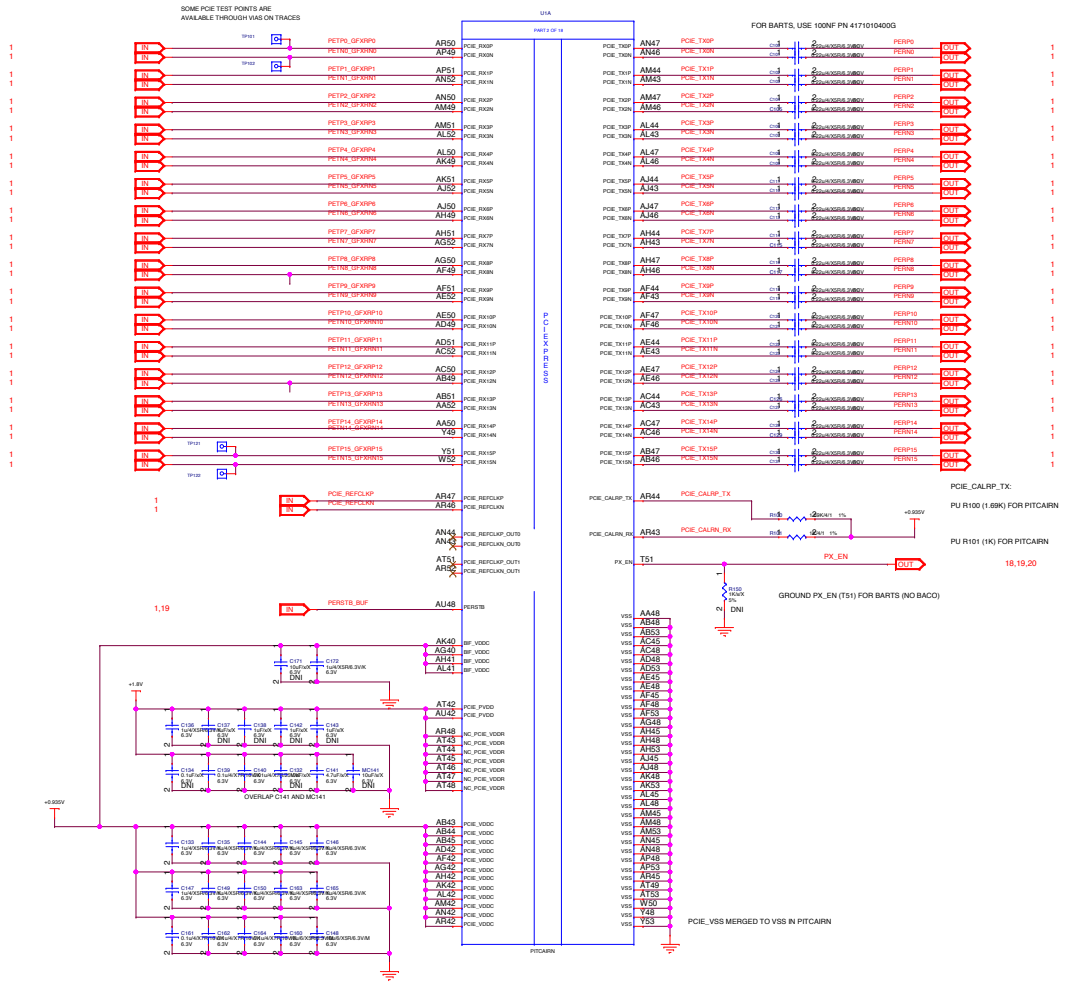
(2) CURACAO PCIE INTERFACE



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CURACAO PCIE INTERFACE

Size	Document Number	Rev
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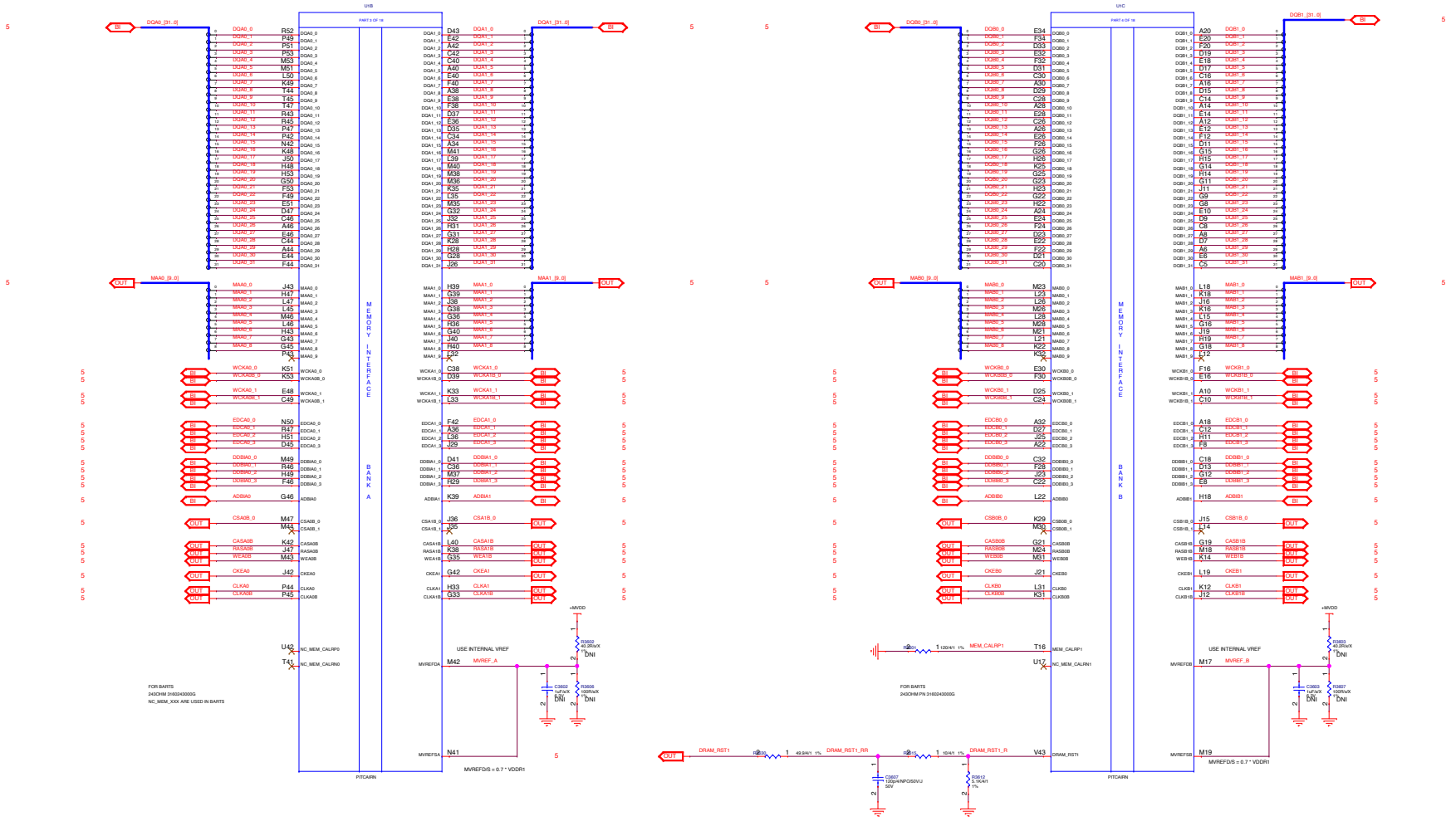
(3) CURACAO MEM INTERFACE CH AB



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CURACAO PITCAIRN MEM CH AB

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Custom	GV-R927XOC-2GD	1.02
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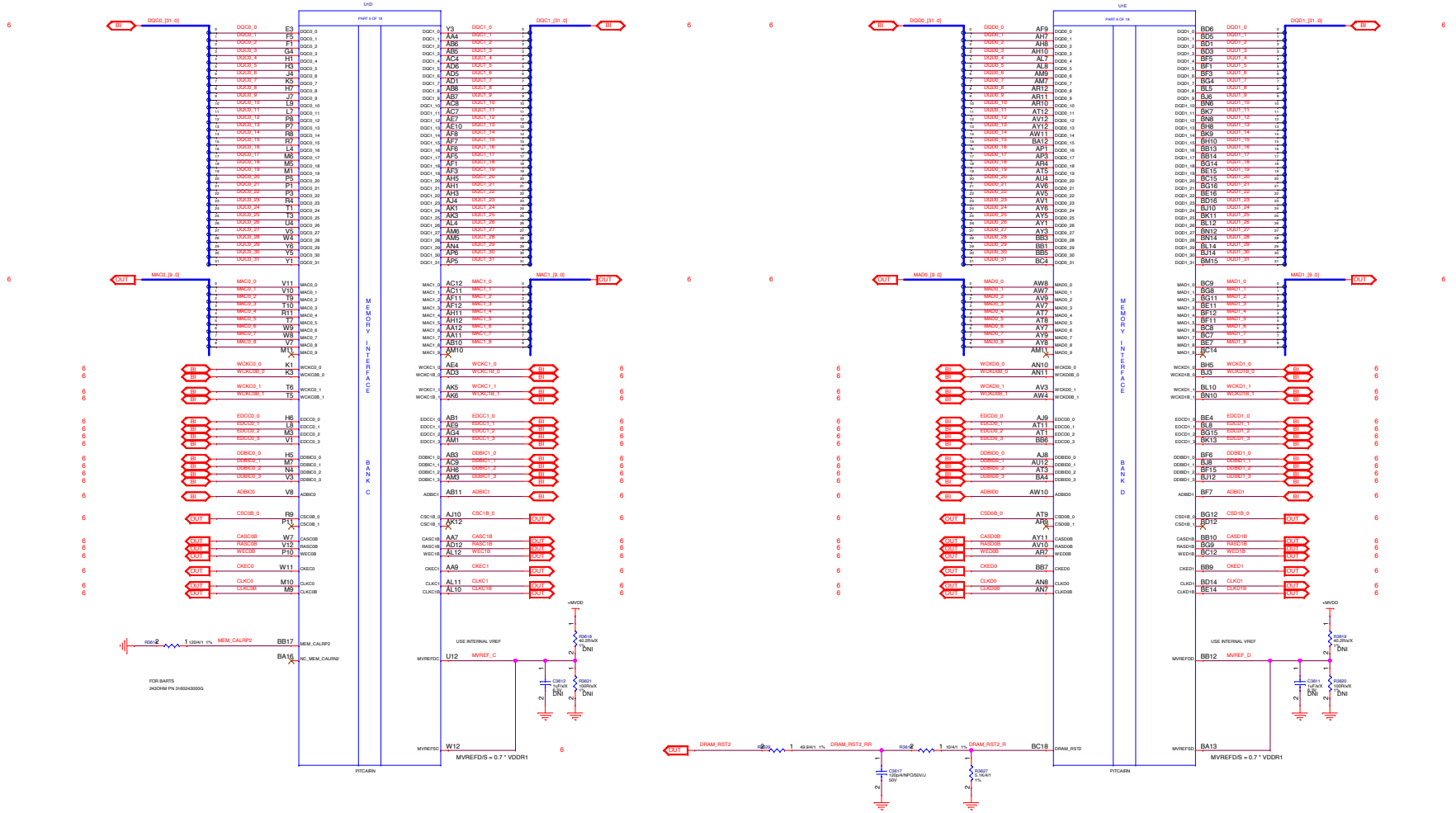
(4) CURACAO MEM INTERFACE CH CD



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CURACAO PITCAIRN MEM CH CD

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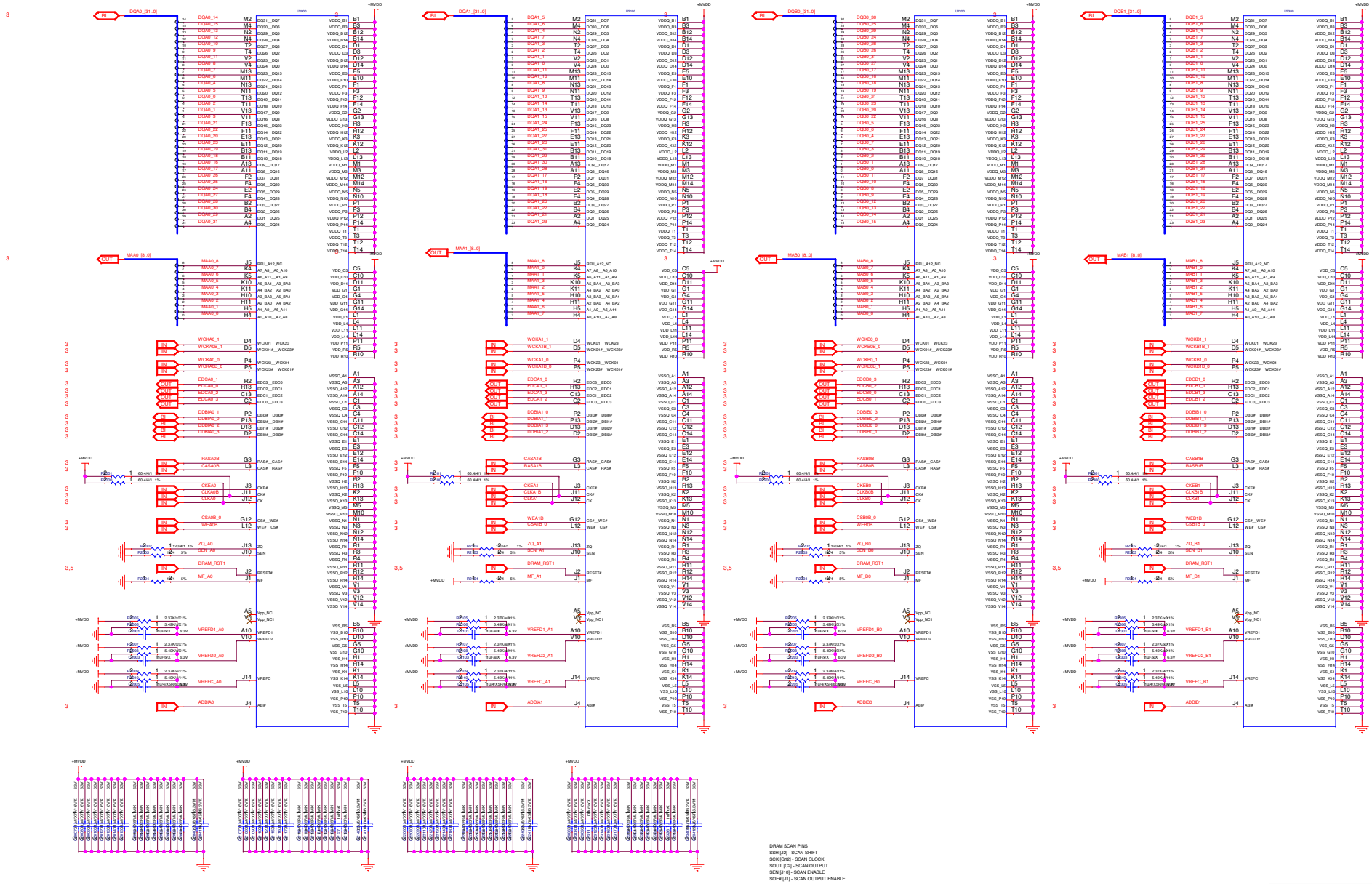
(5) GDDR5 MEM CH AB



DRAM SCAN PINS
SSH [J2] - SCAN SHIFT
SCK [G12] - SCAN CLOCK
SOUT [C2] - SCAN OUTPUT
SEN [J10] - SCAN ENABLE
SOE# [J1] - SCAN OUTPUT ENABLE

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GDDR5 MEM CH AB

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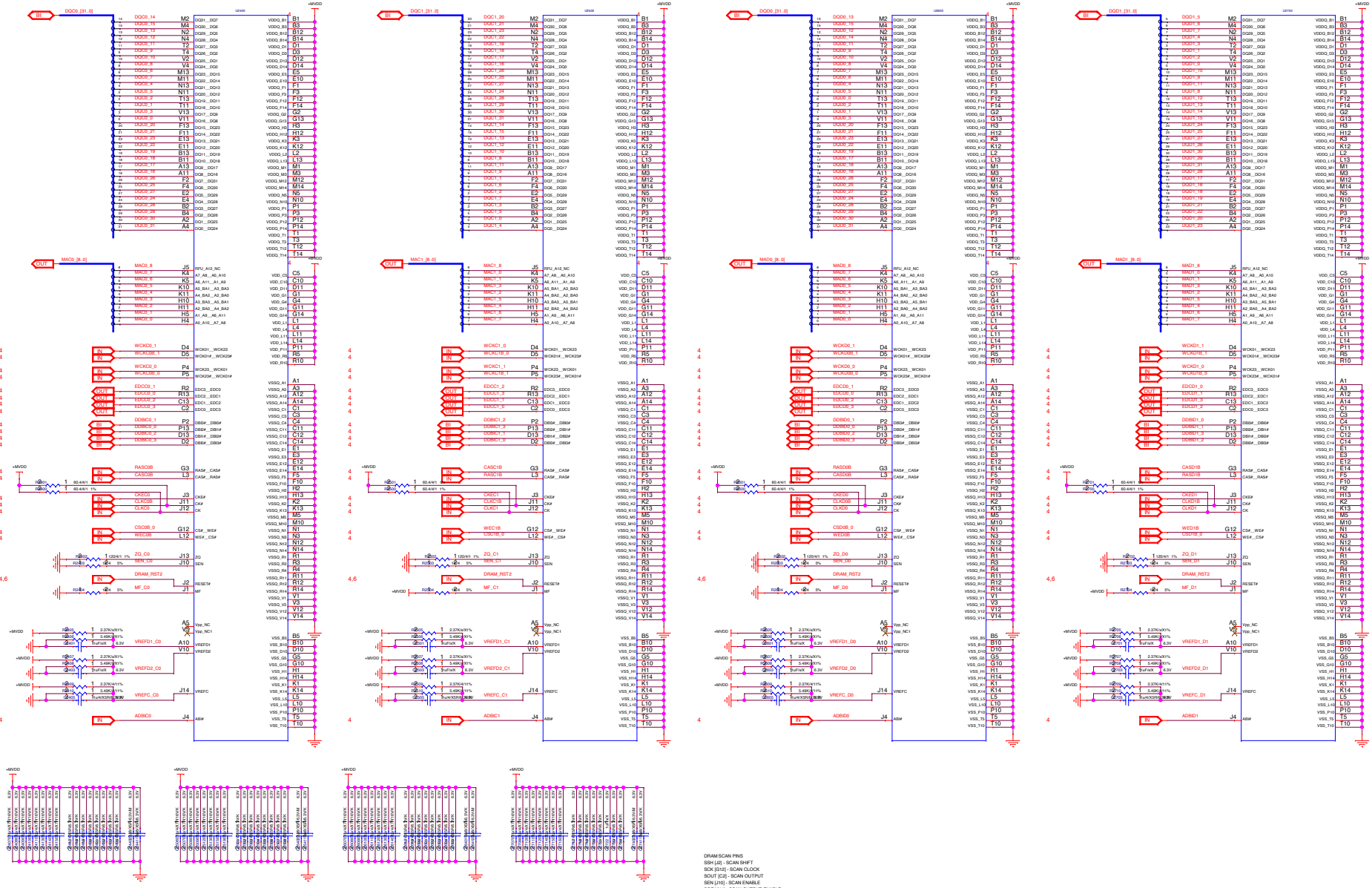
(6) GDDR5 MEM CH CD



DRAM SCAN PINS
SSH [J2] - SCAN SHIFT
SCK [G12] - SCAN CLOCK
SOUT [C2] - SCAN OUTPUT
SEN [J10] - SCAN ENABLE
SOE# [J1] - SCAN OUTPUT ENABLE

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GDDR5 MEM CH CD

Size	Document Number	Rev
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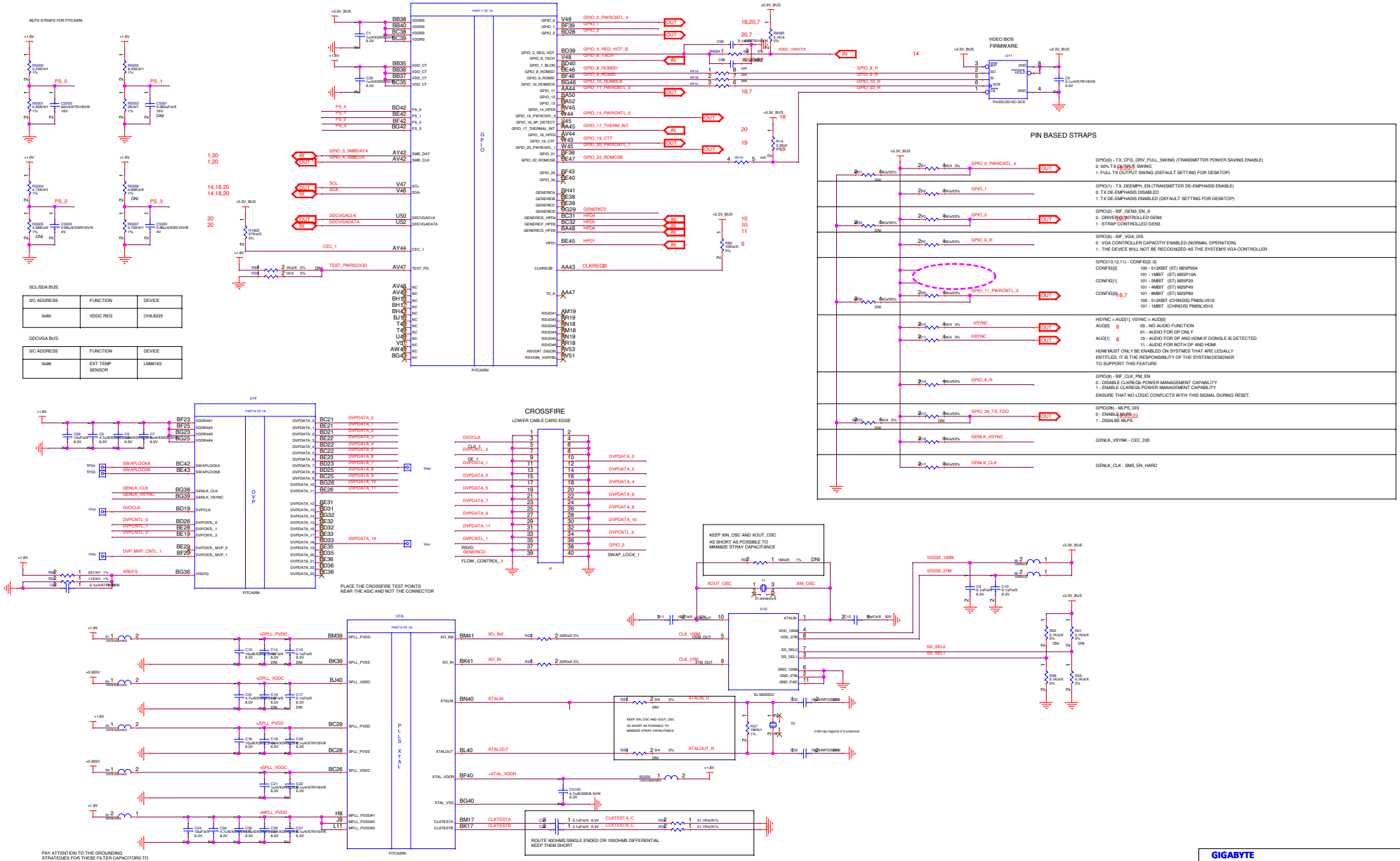
(7) CURACAO GPIO STRAP CF PLL XTAL



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CURACAO PITCAIRN GPIO STRAP

Size	Document Number	Rev
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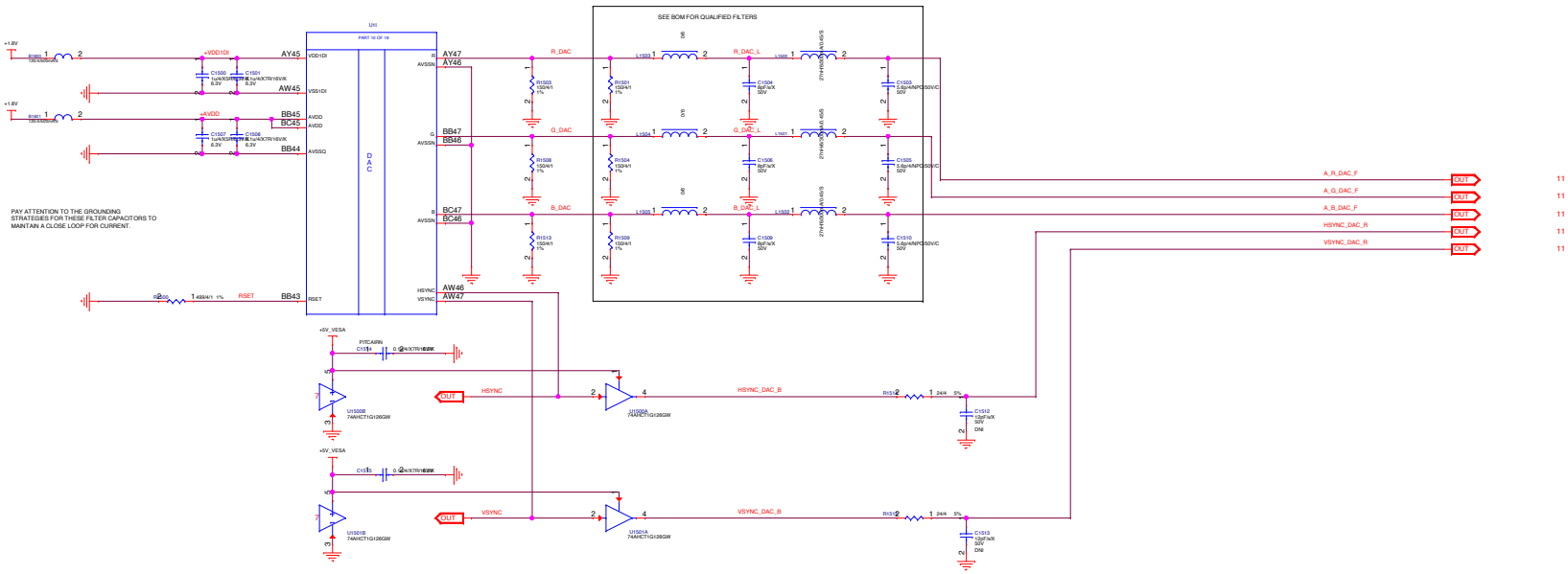
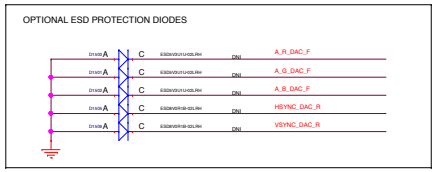
(8) CURACAO DAC





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CURACAO PITCAIRN DAC

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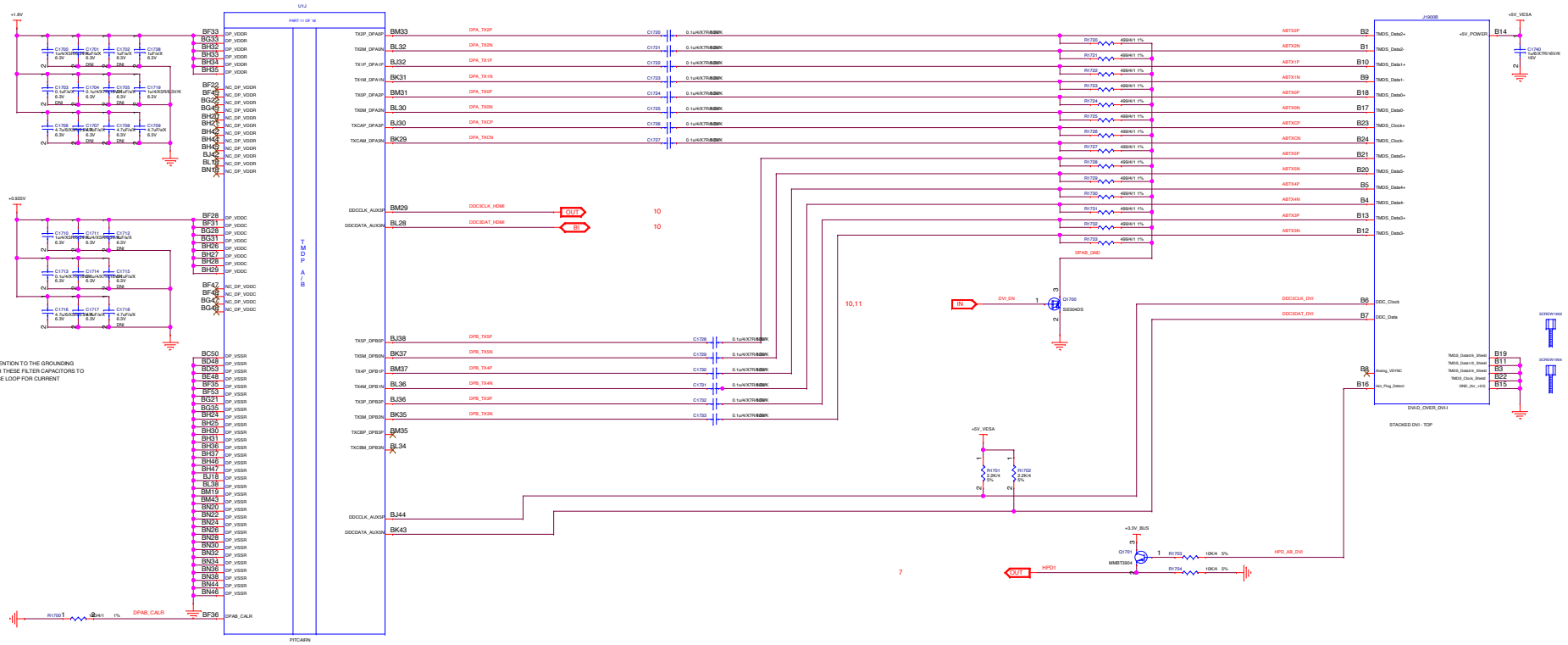
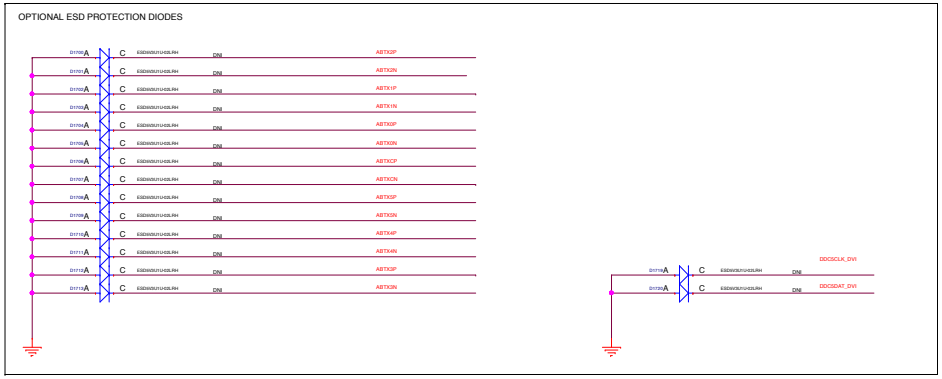
(9) CURACAO TMDPAB sDVI





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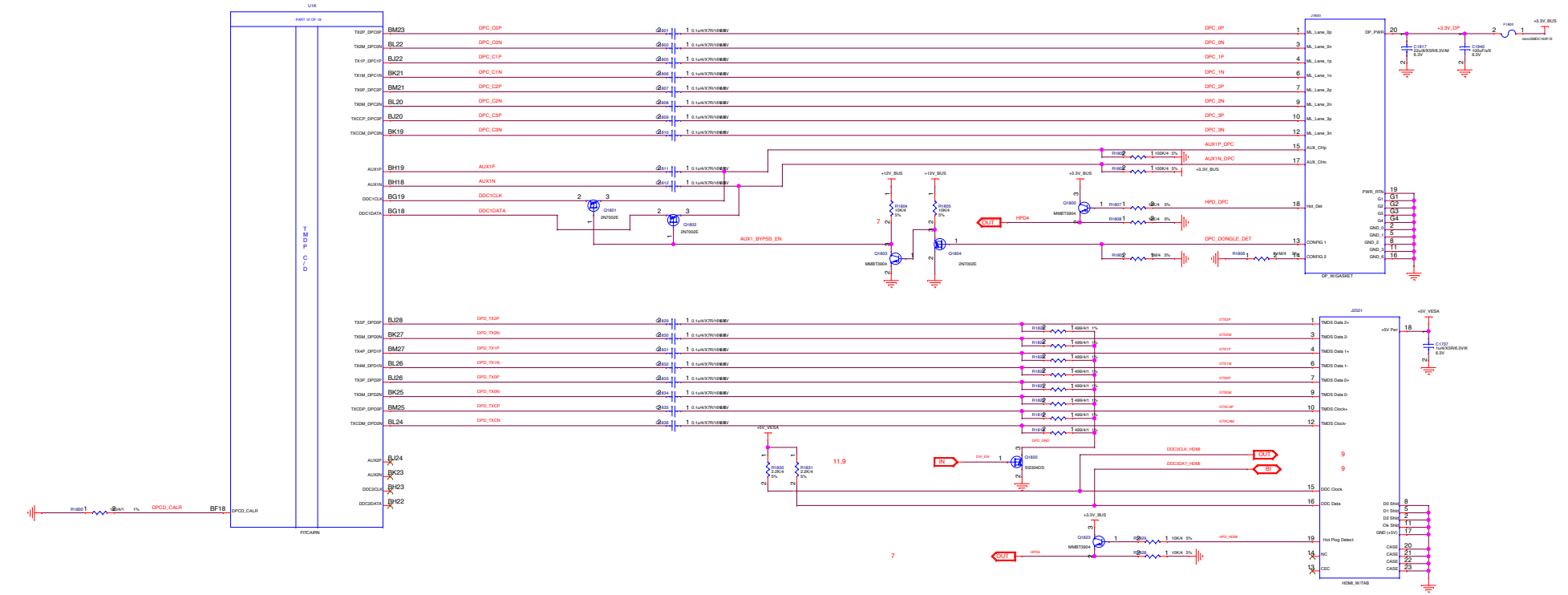
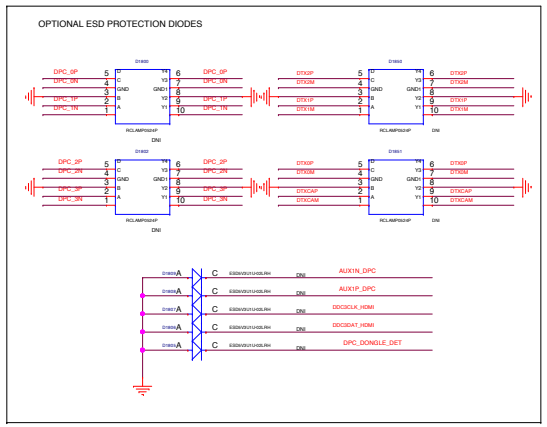
DATE: Wed Jul 17 02:26:13 2013	REV: 1.0
SHEET NUMBER: 9 OF 26	
DOCUMENT NUMBER: GV-R927XOC-2GD	TITLE: <TITLE>

(10) CURACAO TMDPCD DP HDMI





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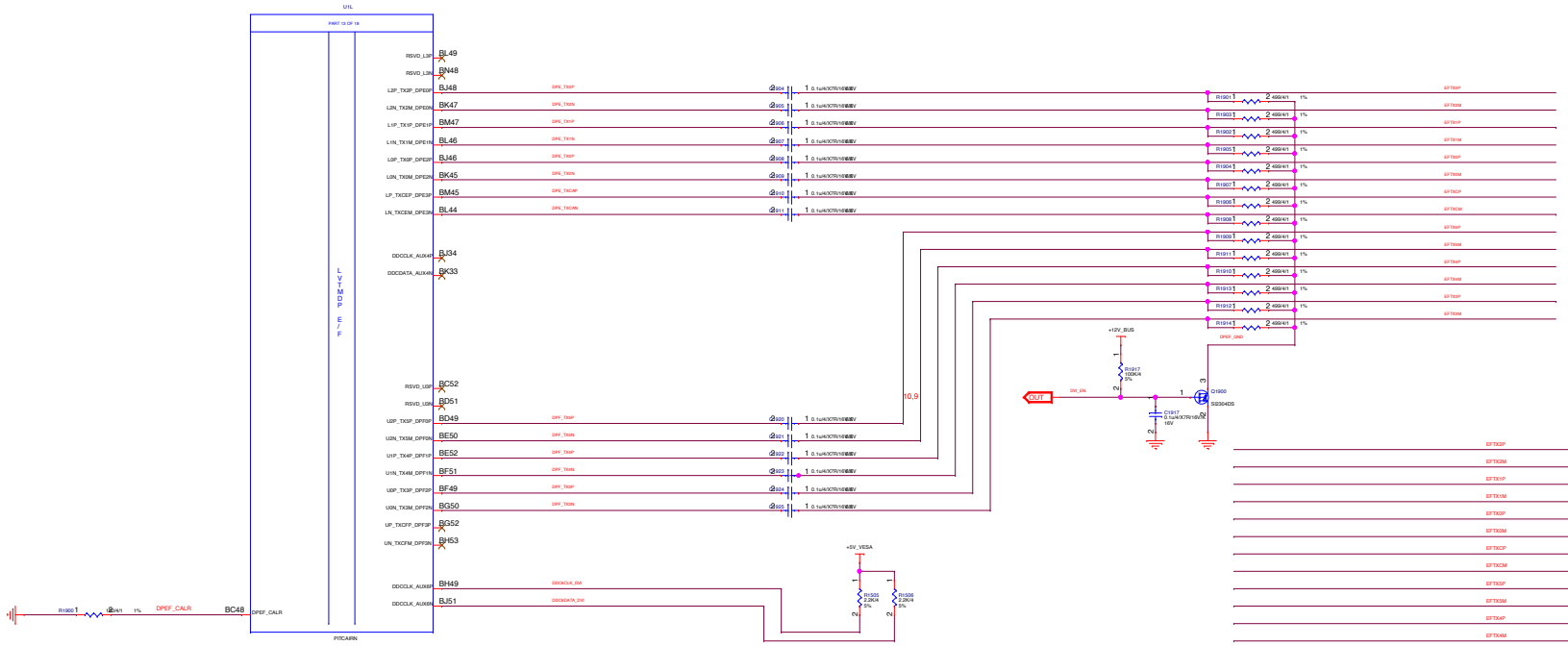
(11) CURACAO LVTMDPEF dDVI



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DOCUMENT NUMBER:	GV-R927XOC-2GD
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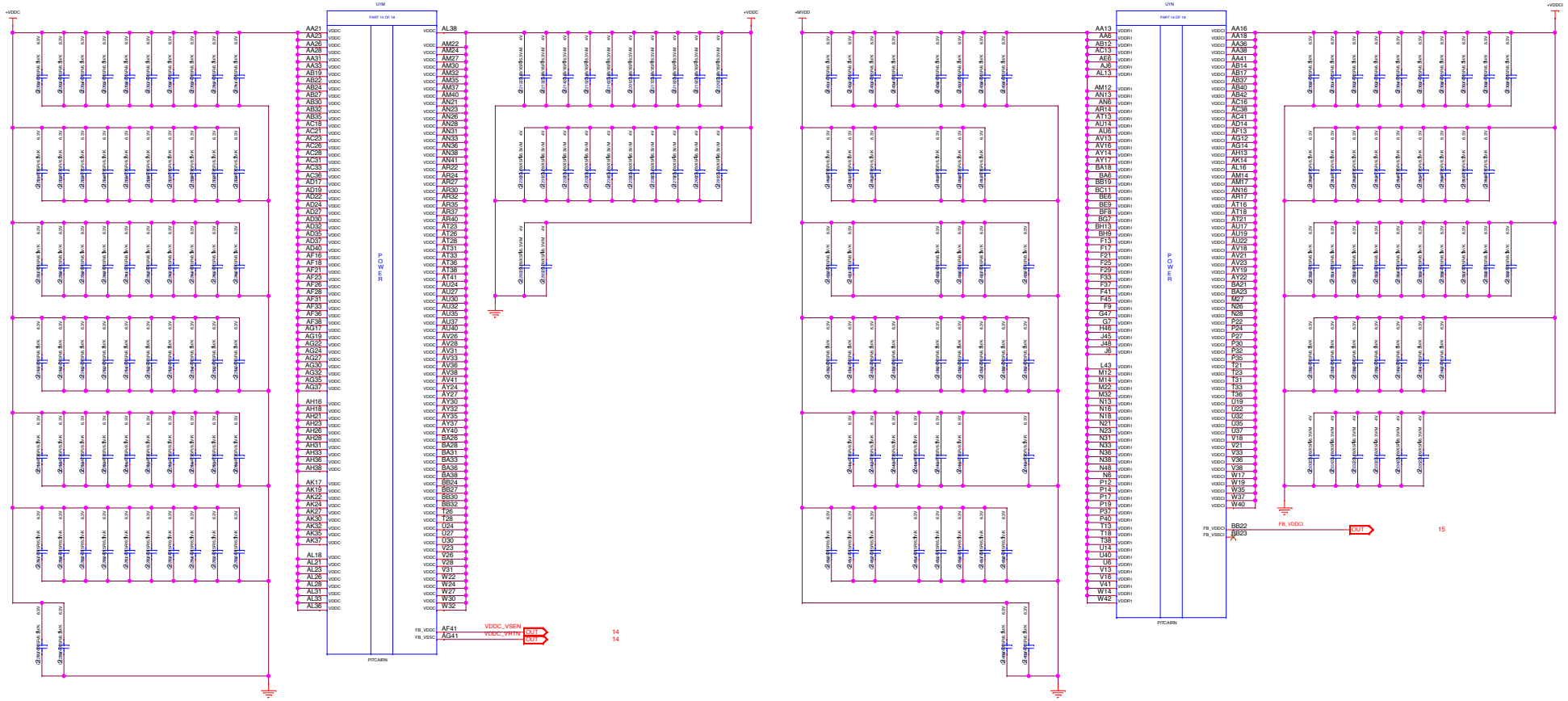
(12) CURACAO POWER



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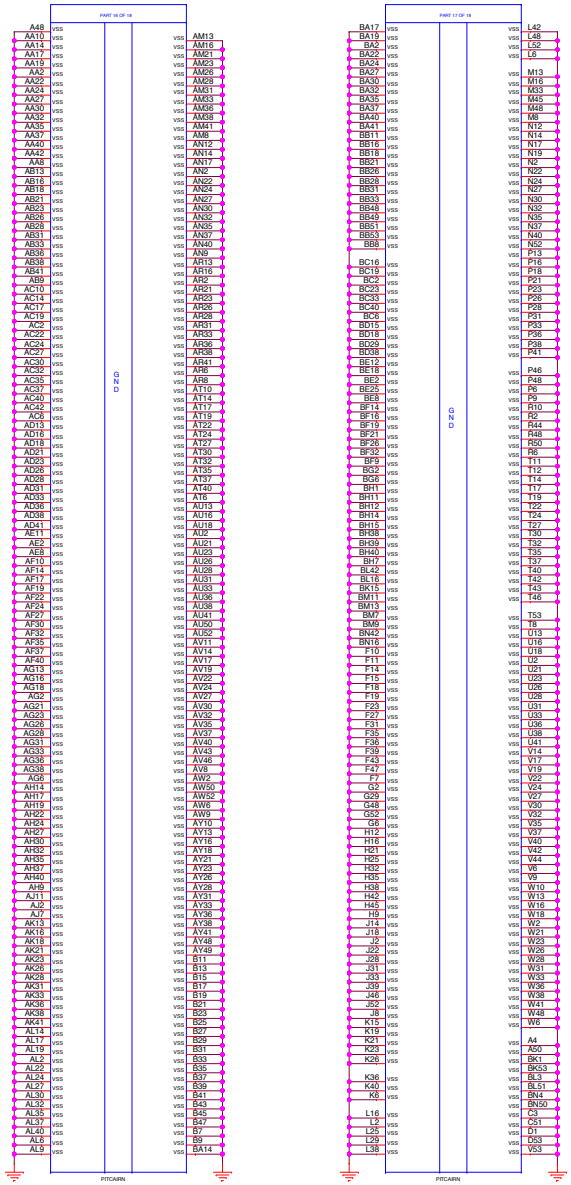
(13) CURACAO GND



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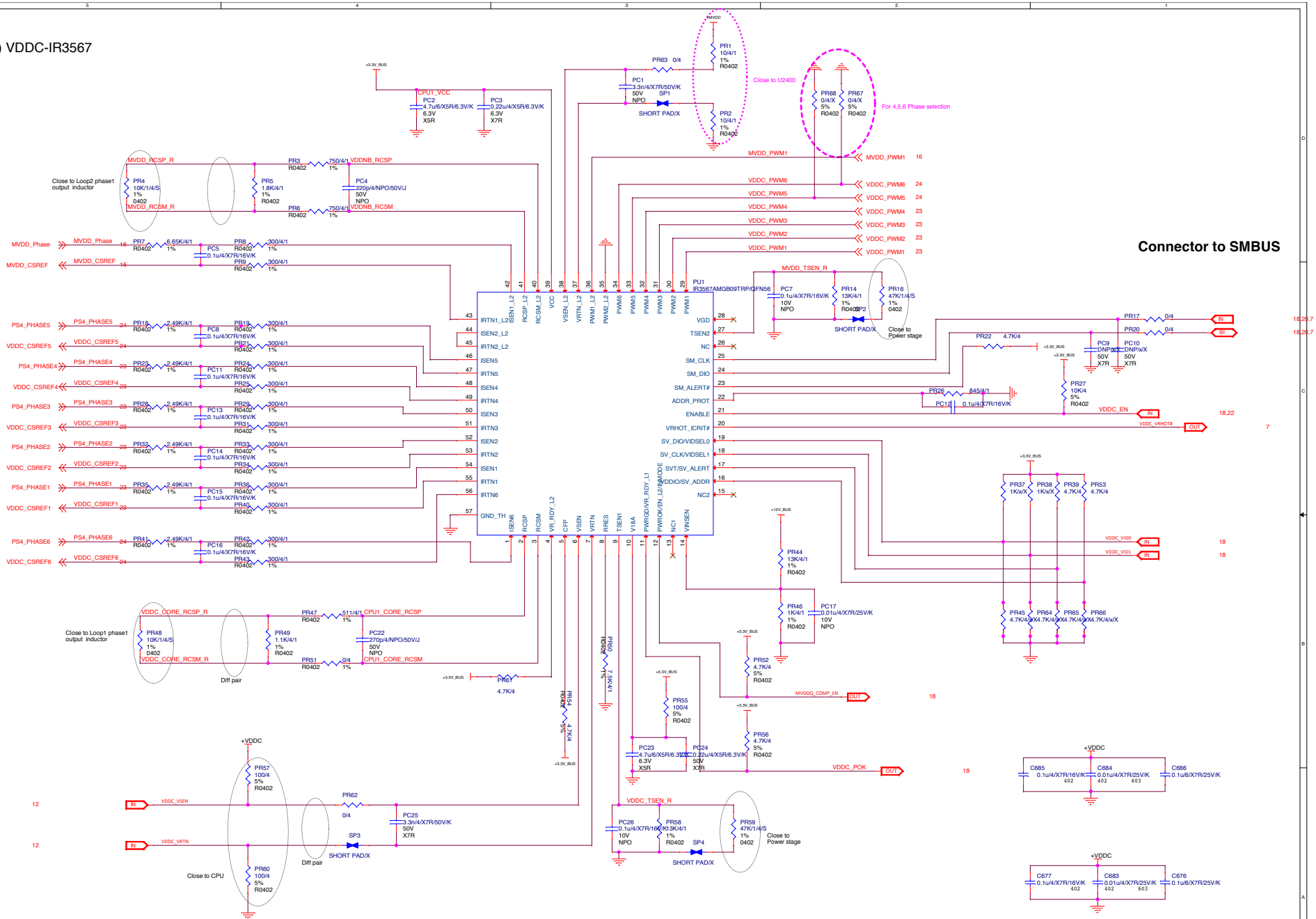
(14) VDDC-IR3567



GIGABYTE	
VDDC-IR3567	
Size C	Document Number GV-R927XOC-2GD Rev 1.02
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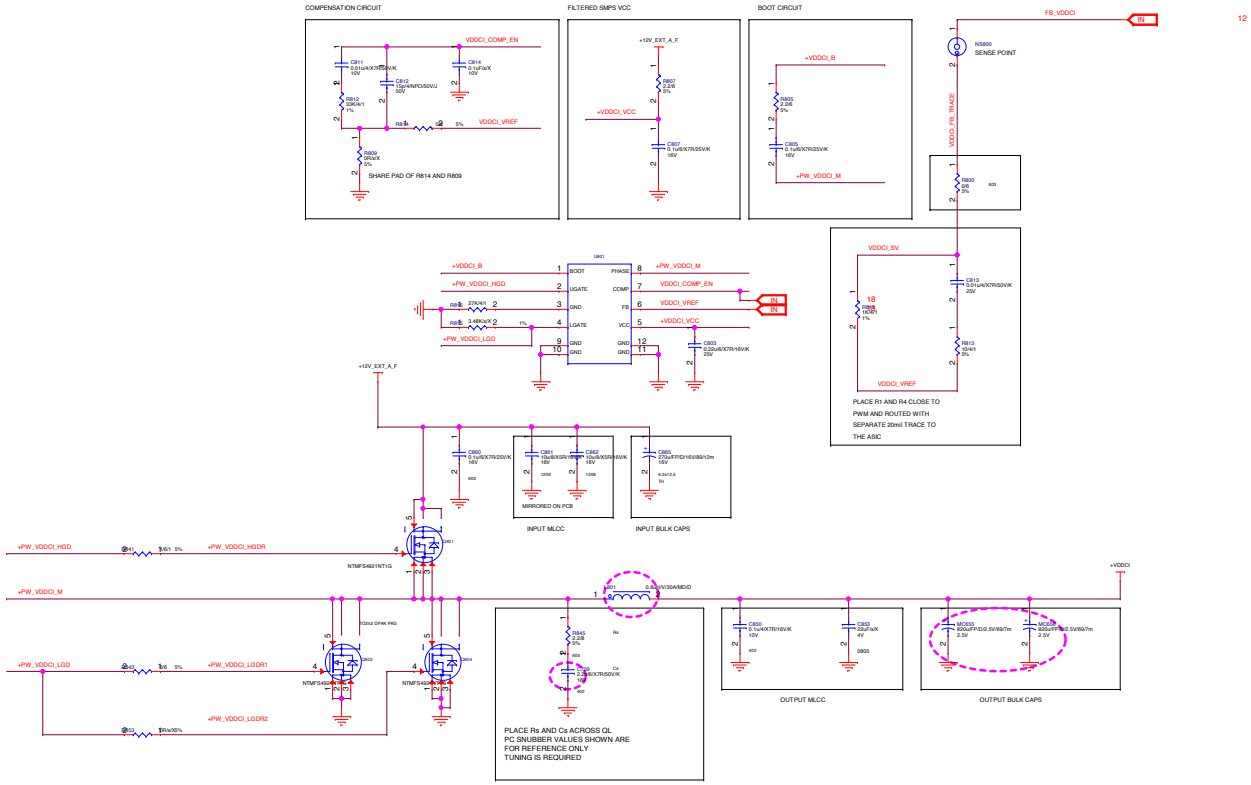
(15) VDDCI



GIGABYTE

VDDCI

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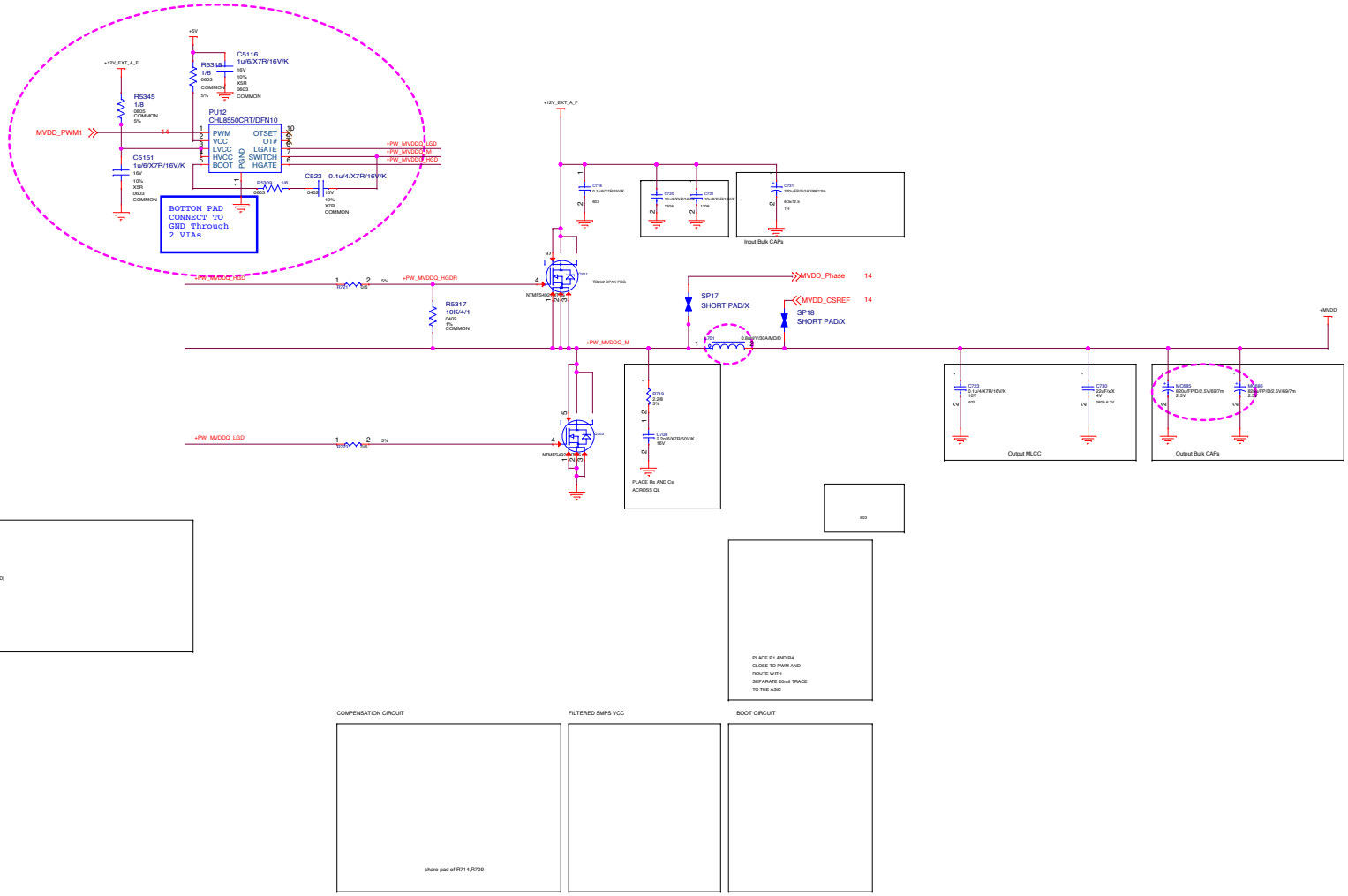
(16) MVDD



LAYOUT GUIDELINE

1. POSITION THE CONTROLLER (U703) SUCH THAT LGATE (PIN4) IS THE CLOSEST TO THE GATE OF THE MOSFETS. YOU CAN PLACE THE GATE RESISTORS R721 AND R722 NEXT TO THE GATE OF THE MOSFETS. MAKE THE GATE DRIVE TRACES (PW_MVDDQ_LGD/HGD) AS SHORT AS POSSIBLE TO REDUCE THE TRACE INDUCTANCE.
2. PLACE THE BYPASS CAPACITORS FOR VCC (C703) AS WELL AS BOOST CAPS (C705) AS CLOSE TO THE CONTROLLER AS POSSIBLE.
3. VOLTAGE AMPLIFIER COMPENSATION NETWORK: PLACE R714 CLOSE TO THE PIN 7. PLACE THE REST OF THE COMPENSATION NETWORK (R710, R711, R712, R713, C711, C712 AND C713) CLOSE TO THE PINS 7 AND 8.

GIGABYTE

MVDD

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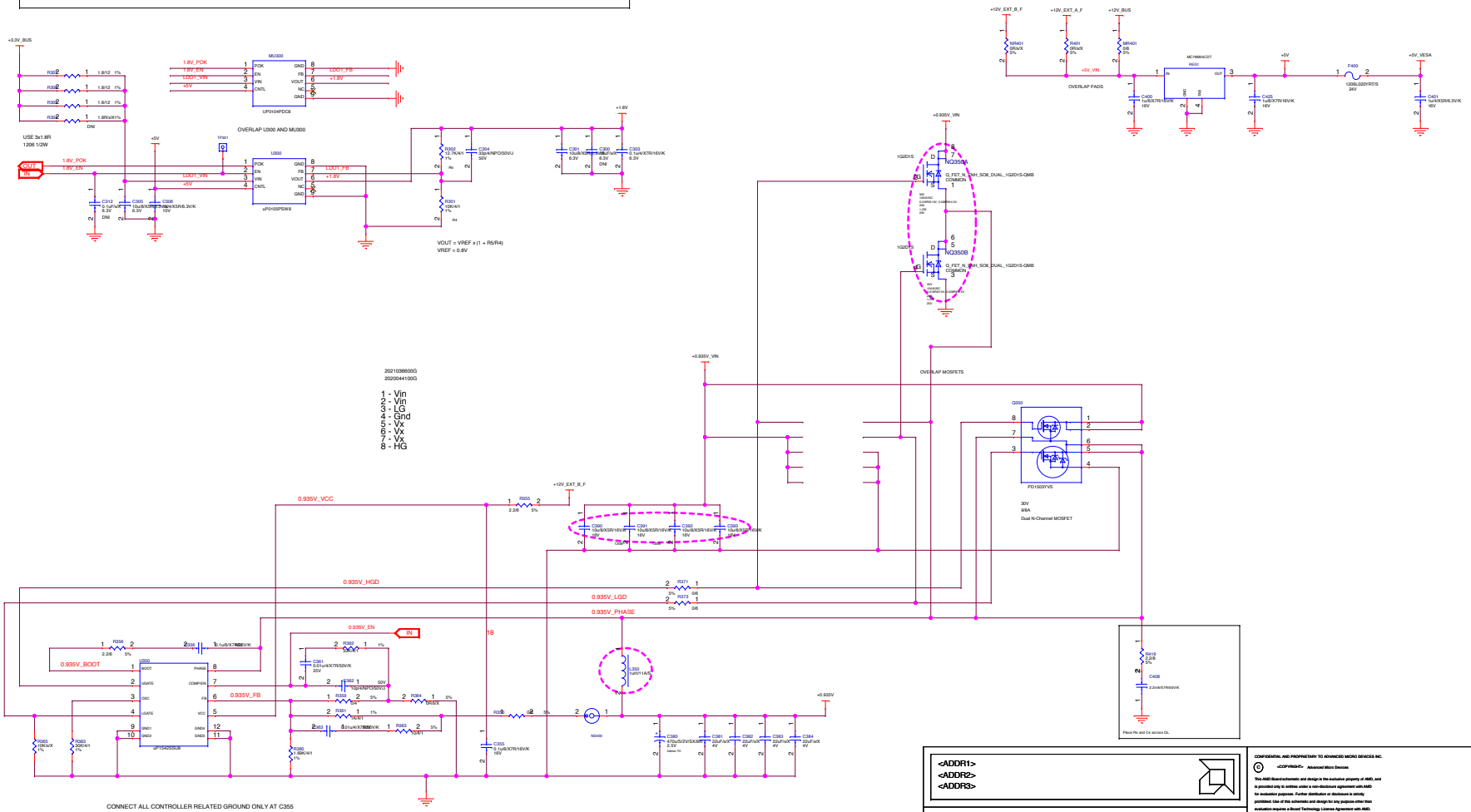
(17) SMALL RAIL REGULATOR

LDO #1: VIN = 3.0V TO 3.6V MAX VOUT = +1.8V +/- 2% IOUT = 1.3A RMS MAX

PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING

REGULATOR FOR +5V RAILS

IOUT MAX = 150mA



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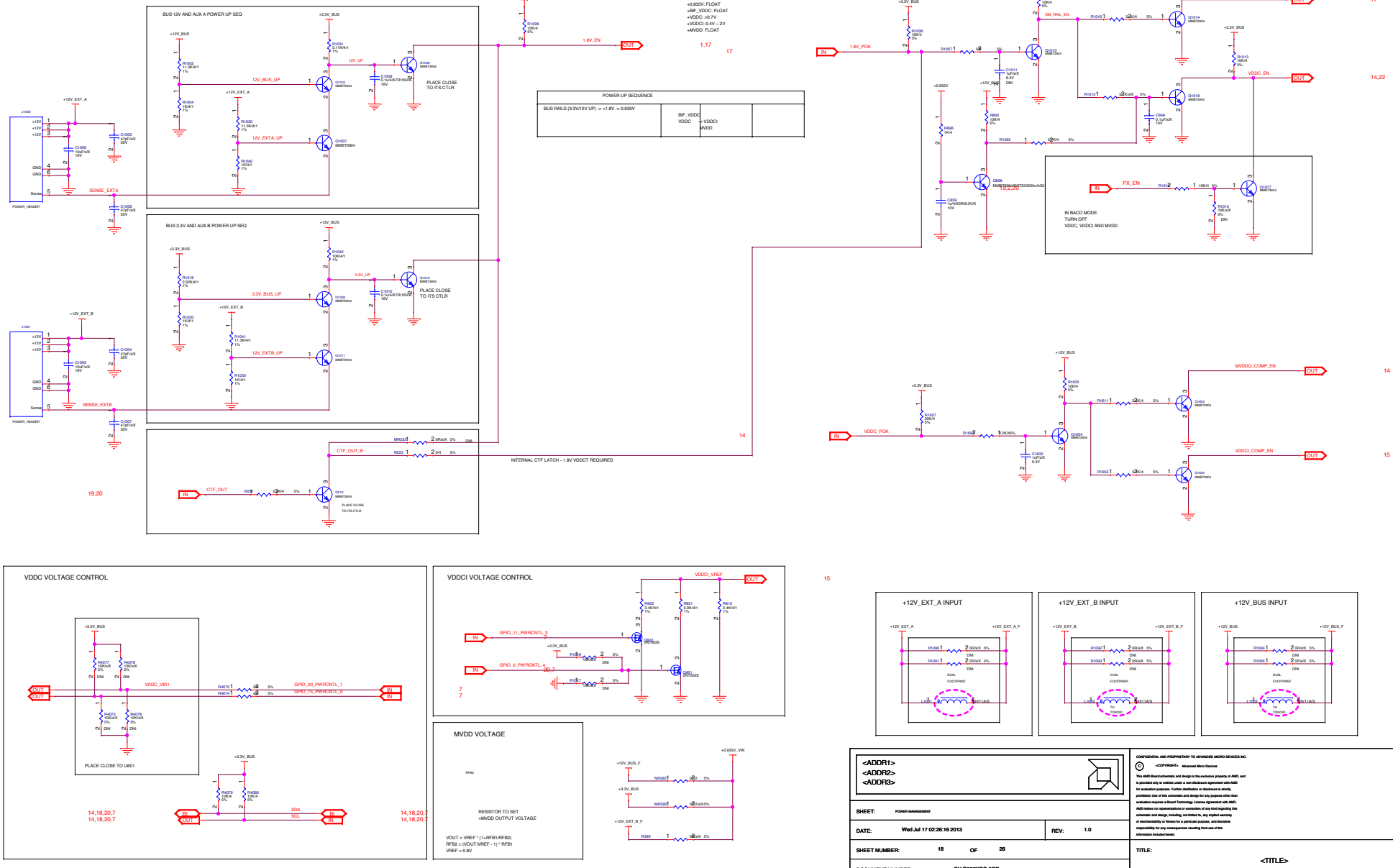
DATE:	Wed Jul 17 02:26:16 2013
REV:	1.0
SHEET NUMBER:	17 OF 26
DOCUMENT NUMBER:	GV-R927XOC-2GD
TITLE:	<TITLE>

(18) POWER MANAGEMENT



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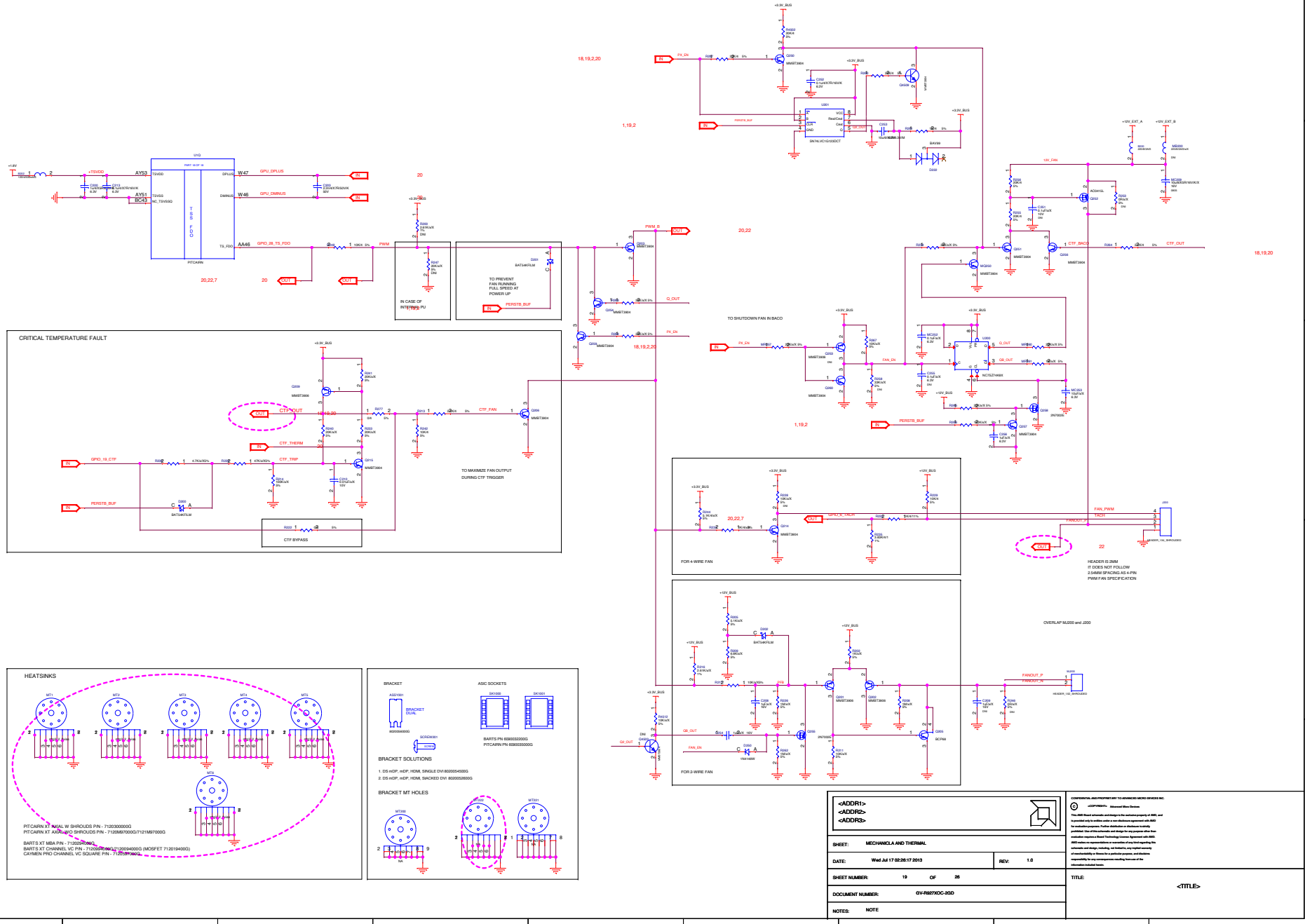
DATE: Wed Jul 17 02:26:16 2013	REV: 1.0
SHEET NUMBER: 18	OF 26
DOCUMENT NUMBER: GV-R927XOC-2GD	TITLE: <TITLE>

(19) MECH AND THERM MANAGEMENT



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DATE:	Wed Jul 17 02:26:17 2013
REV:	1.0
SHEET NUMBER:	19 OF 26
DOCUMENT NUMBER:	GV-R927XOC-3GD
NOTES:	NOTE
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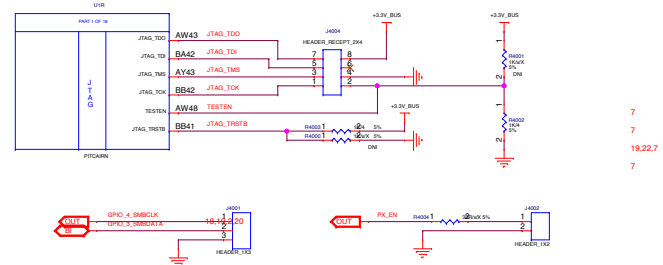
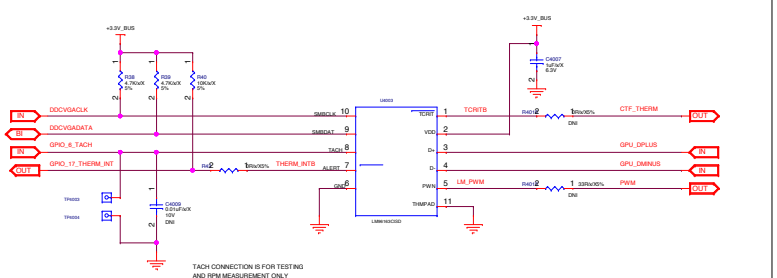
(20) DEBUG CIRCUIT

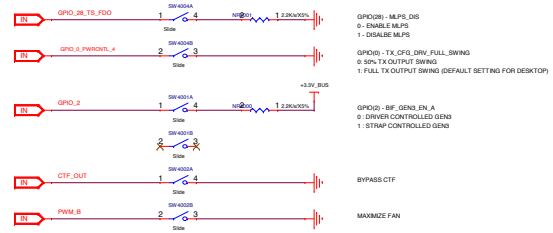
JTAG



LM96163 FOR BACKUP THERMAL CONTROL

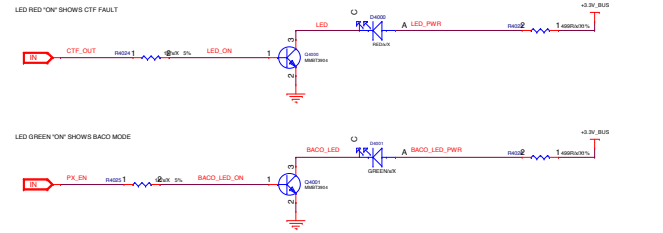


SWITCH CONNECTIONS TO PINSTRAPS



I2C ACCESS POINTS FOR VDDC CONTROLLER

LED LIGHTS



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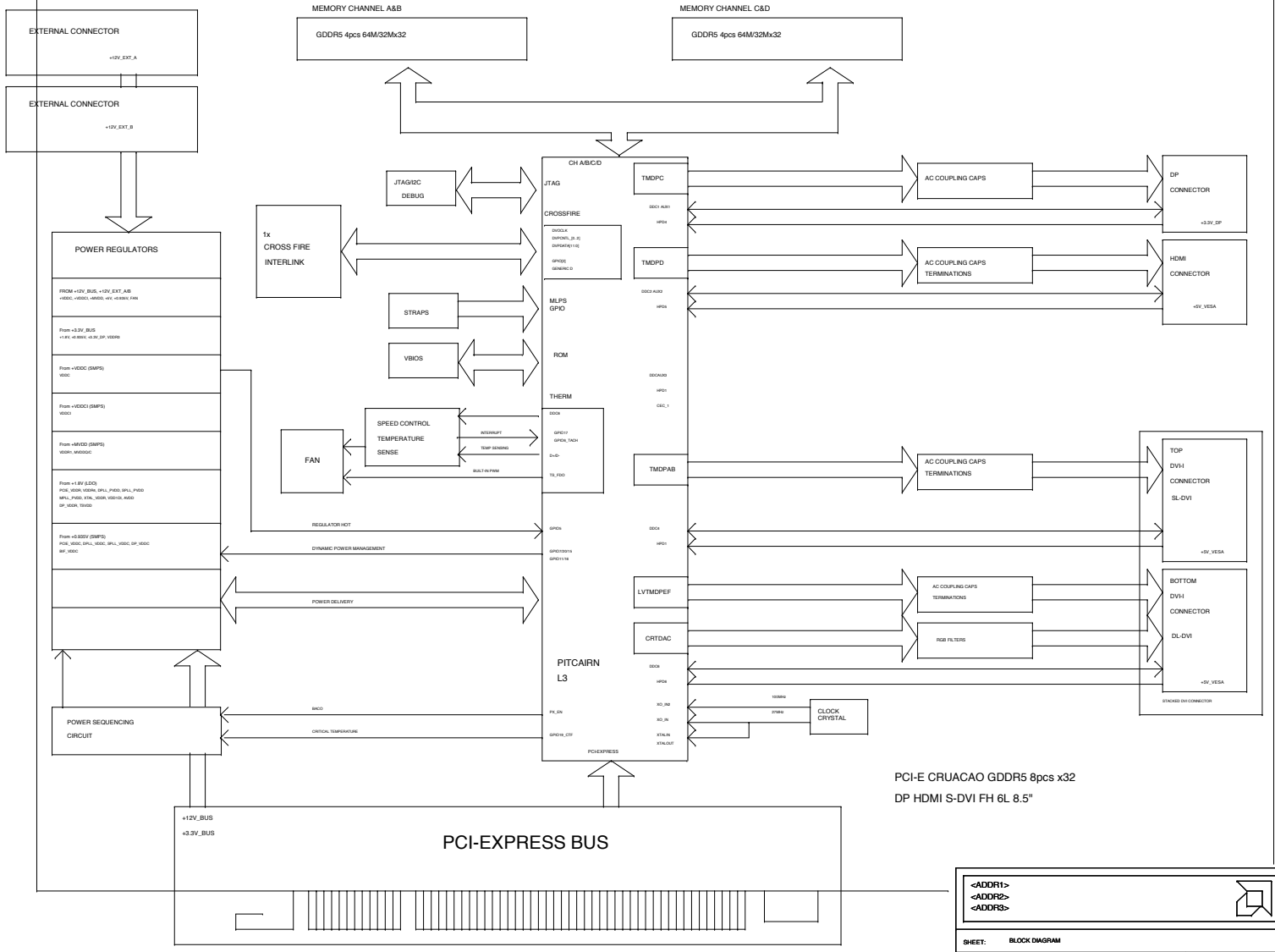

PCI-E CRUACAO GDDR5 8pcs x32

DP HDMI S-DVI FH 6L 8.5"

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DATE: Wed Jul 17 02:26:17 2013	REV: 1.0
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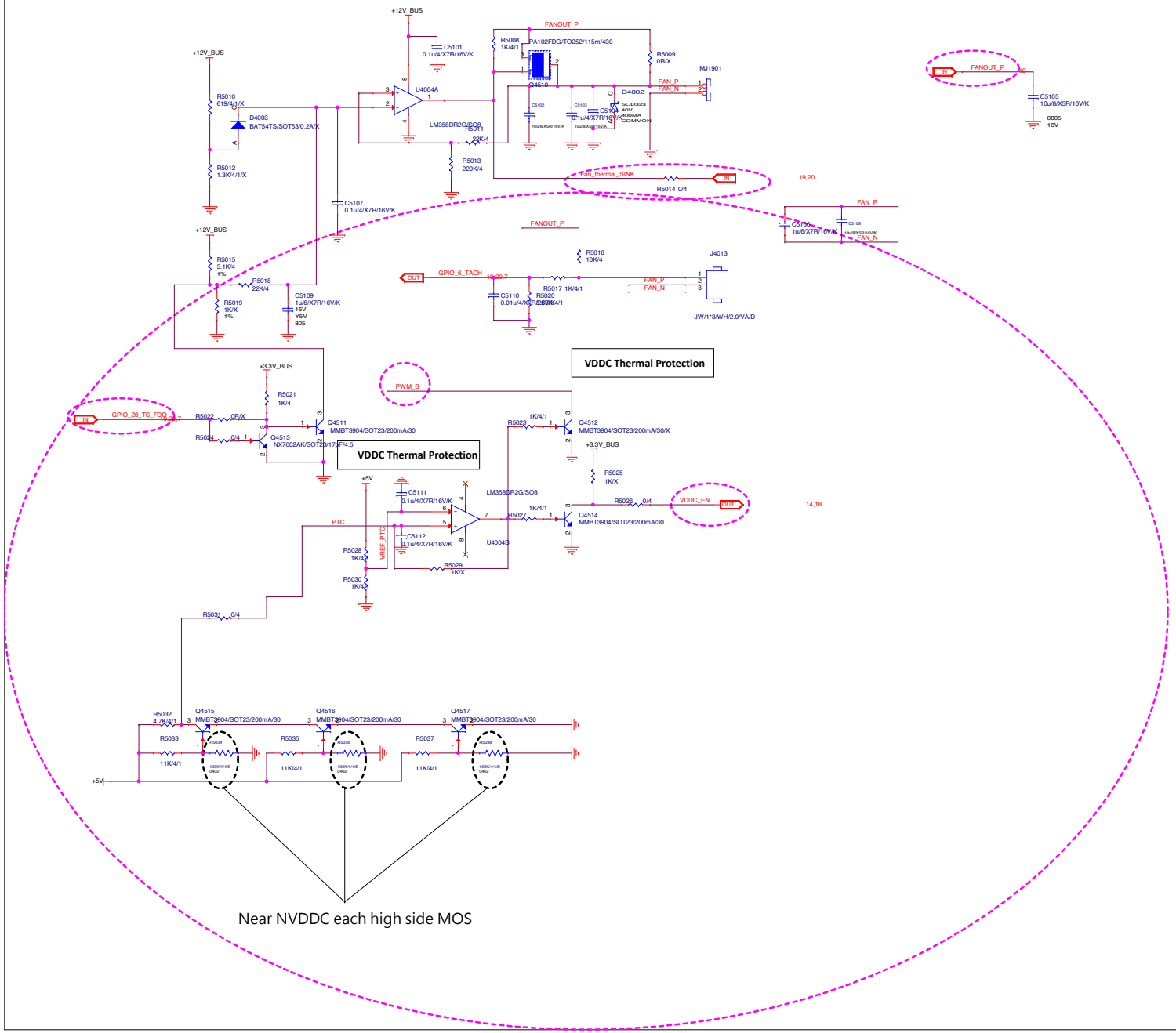
(22) 3 Pin Fan Control



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Title: Fan Control

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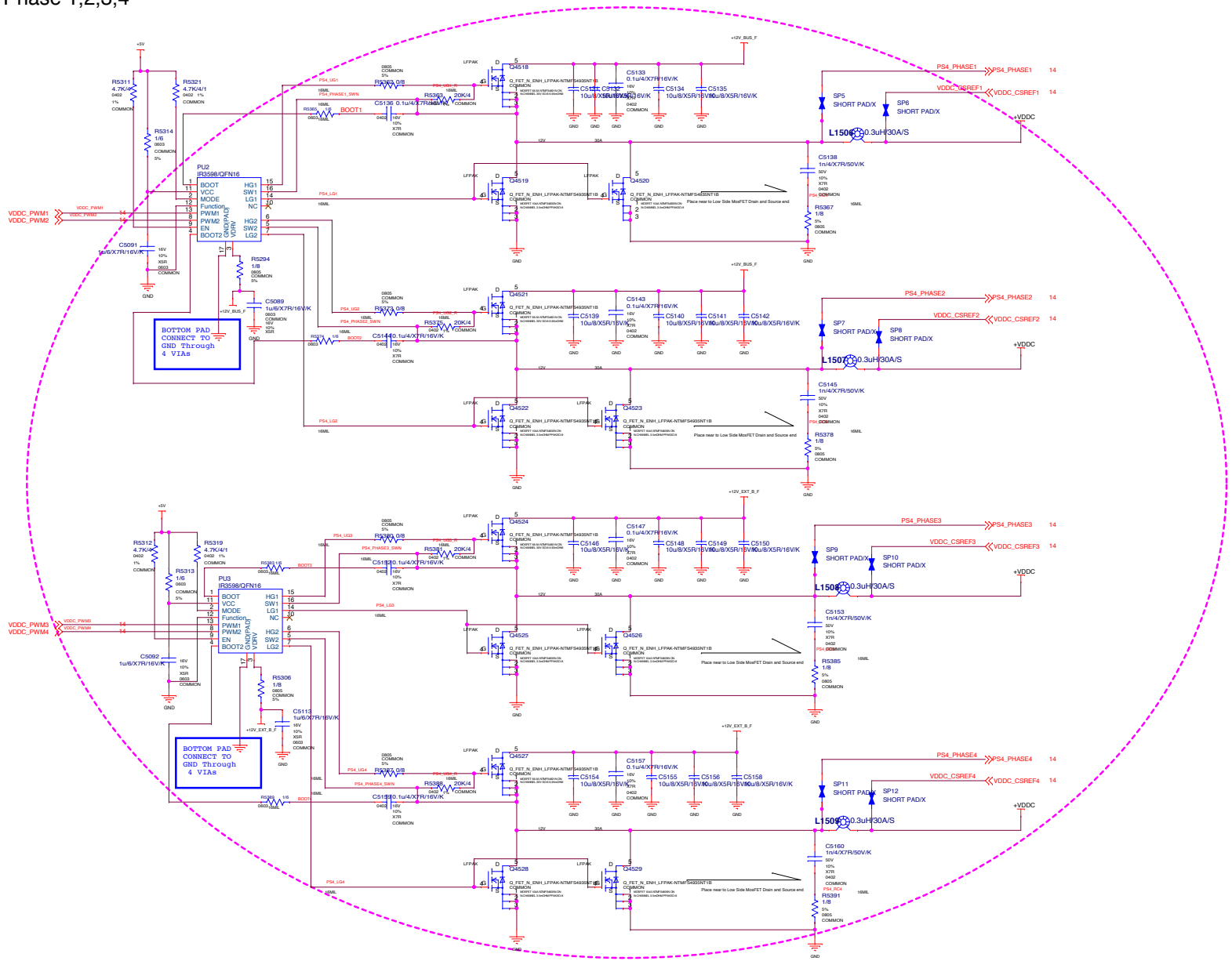
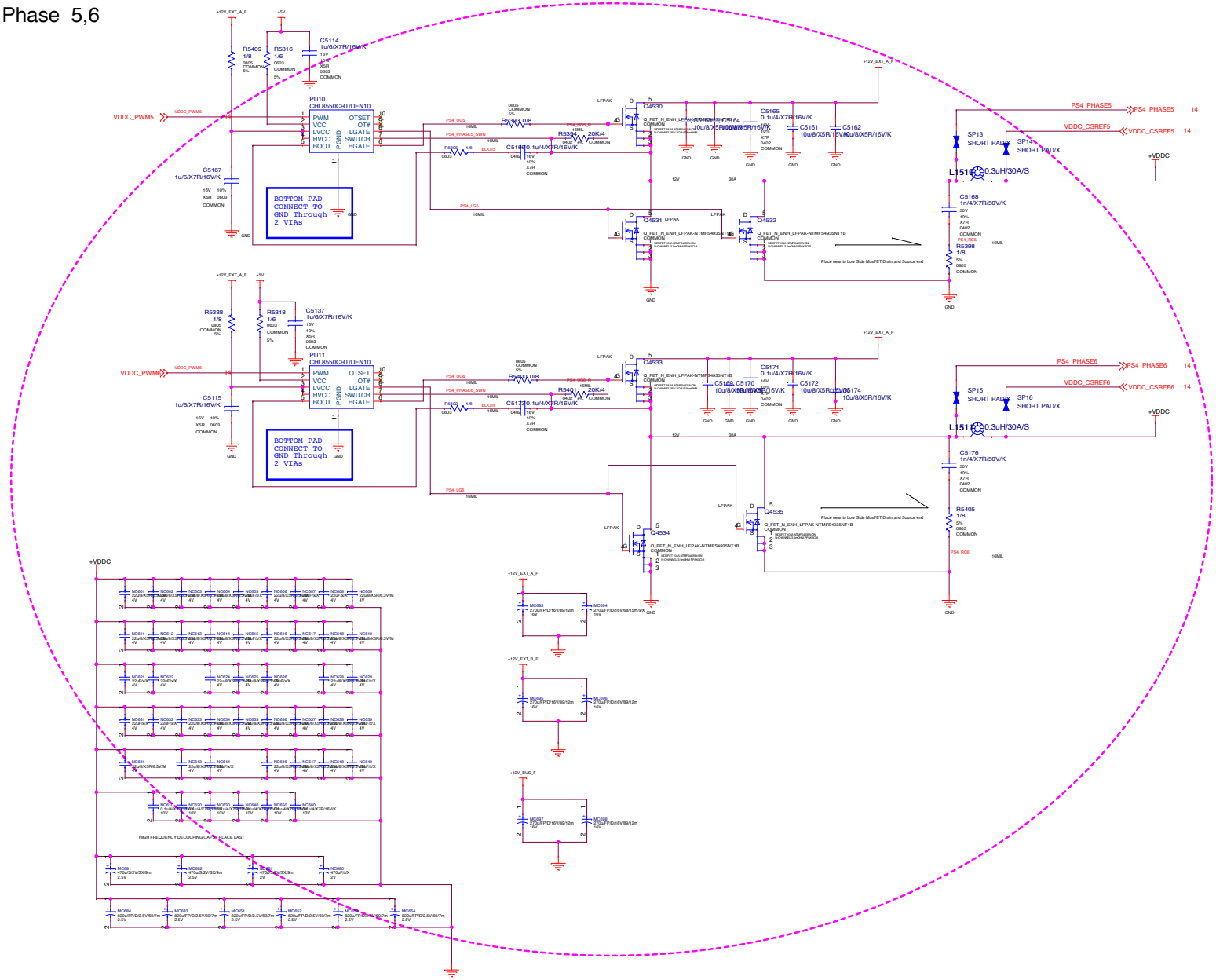
(23) VDDC Phase 1,2,3,4



Title	VDDC Phase 1,2,3		
Size: Custom	Document Number: GV-R927XOC-2GD		Rev: 1.02
Date: Thursday, July 31, 2014	Sheet 23 of 26		

(24) VDDC Phase 5,6



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Title	VDDC Phase 5,6	
Size: Custom	Document Number: GV-R927XOC-2GD	Rev: 1.02
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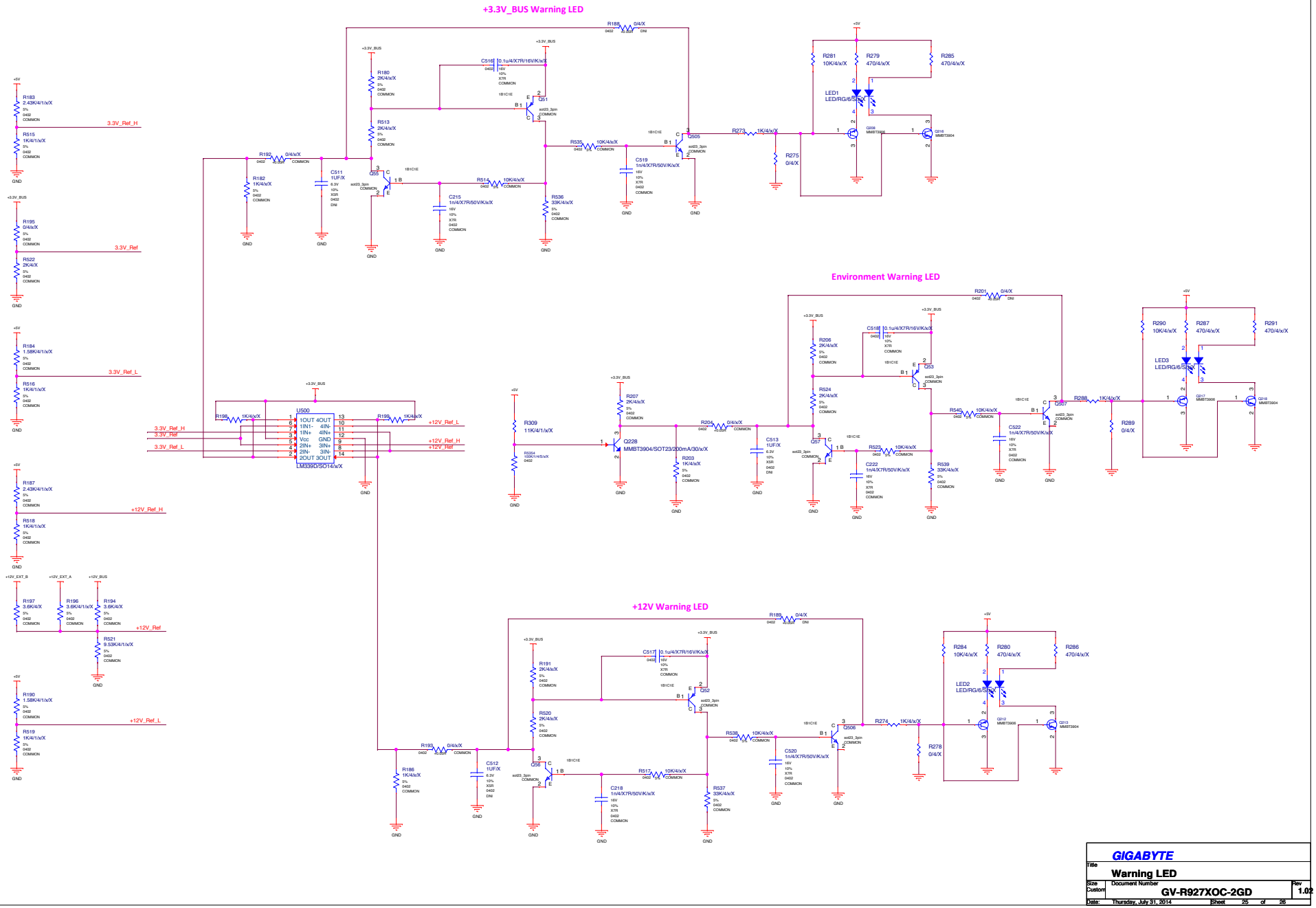
(25) Warning LED



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DOCUMENT NUMBER: 105_C631XX_00D

DATE: Wed Jul 17 02:26:17 2013

SHEET NUMBER: 22 OF 23

REV: <REV>

REVISION HISTORY

ENGINEER: <ENGINEER>

NOTES: NOTE

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SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
0	00A	02/01/2012	INITIAL SCHEMATIC BASED ON C600
1	00B	20/12/2012	add R668,C99,C89
1	00C	26/12/2012	remove L1720 ~L1723 remove NC pin for DP_VDDRGP_VDDC
	00D	10/05/2013	update power sequence to make 0.95V power up before vddc

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REVISION HISTORY
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Date: Thursday, July 31, 2014 Sheet 26 of 28