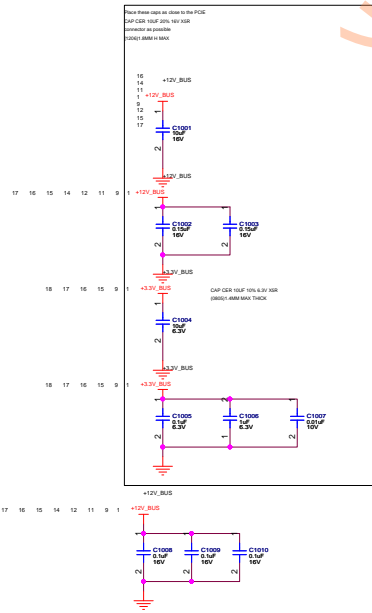
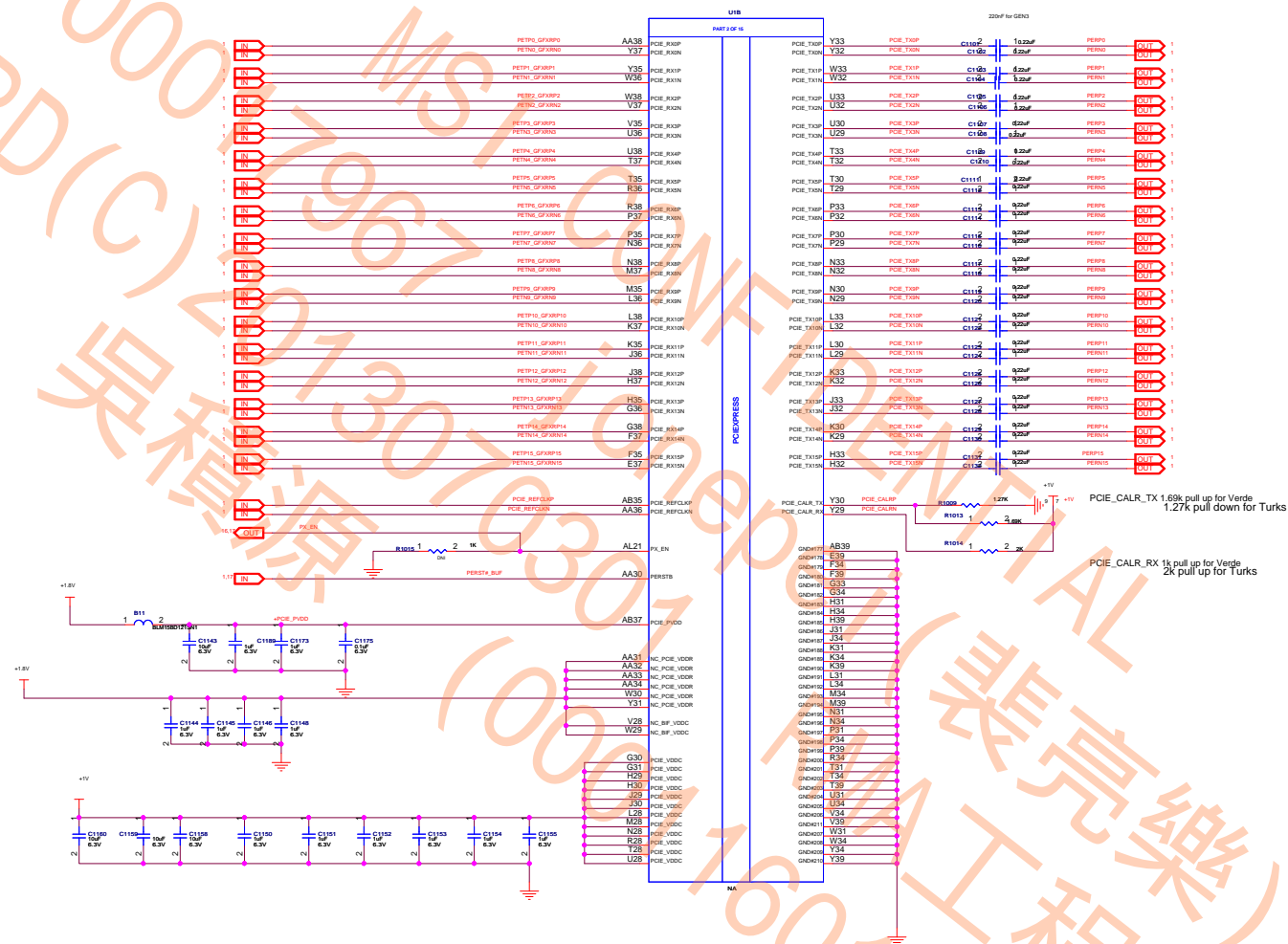
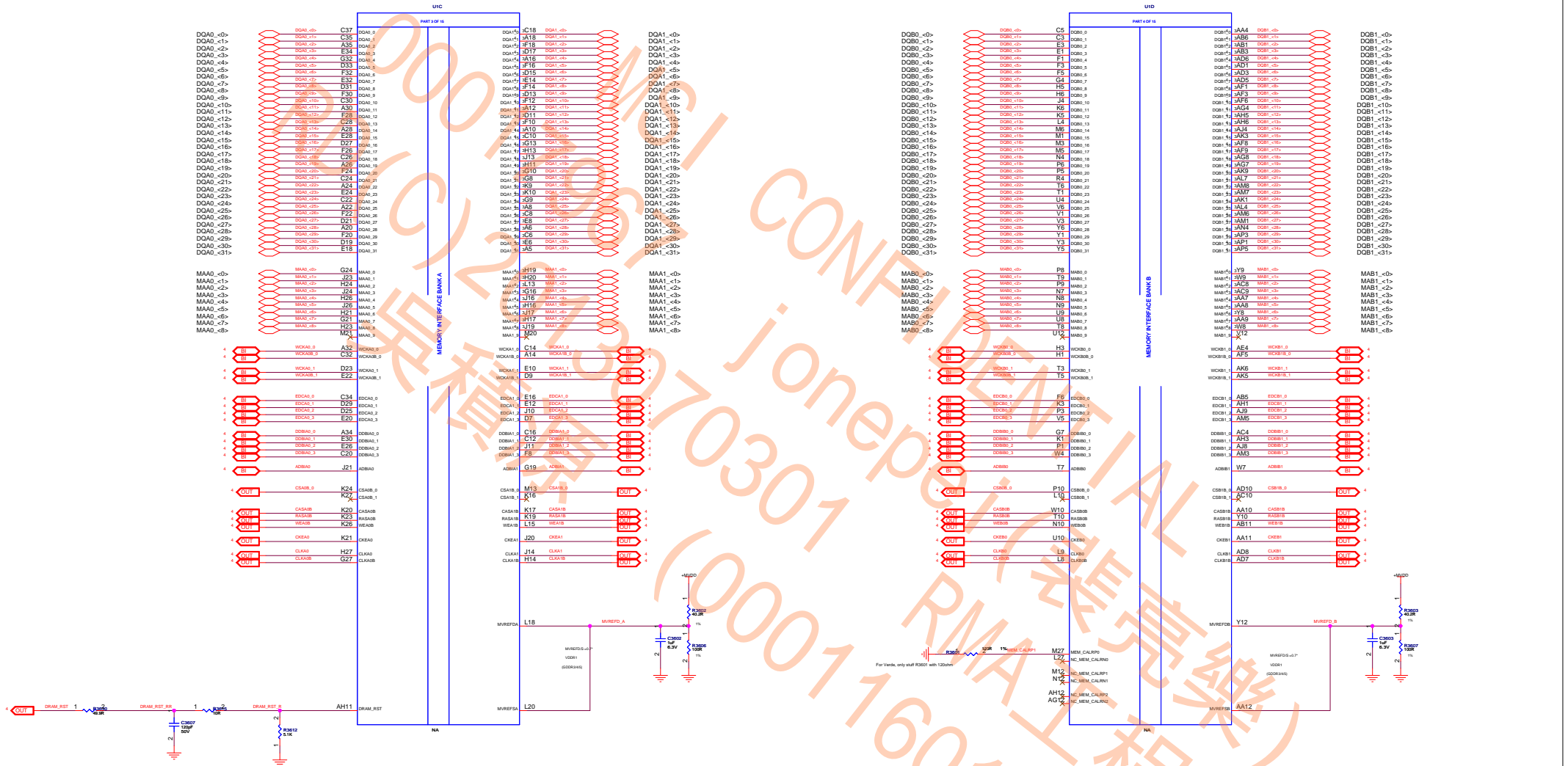


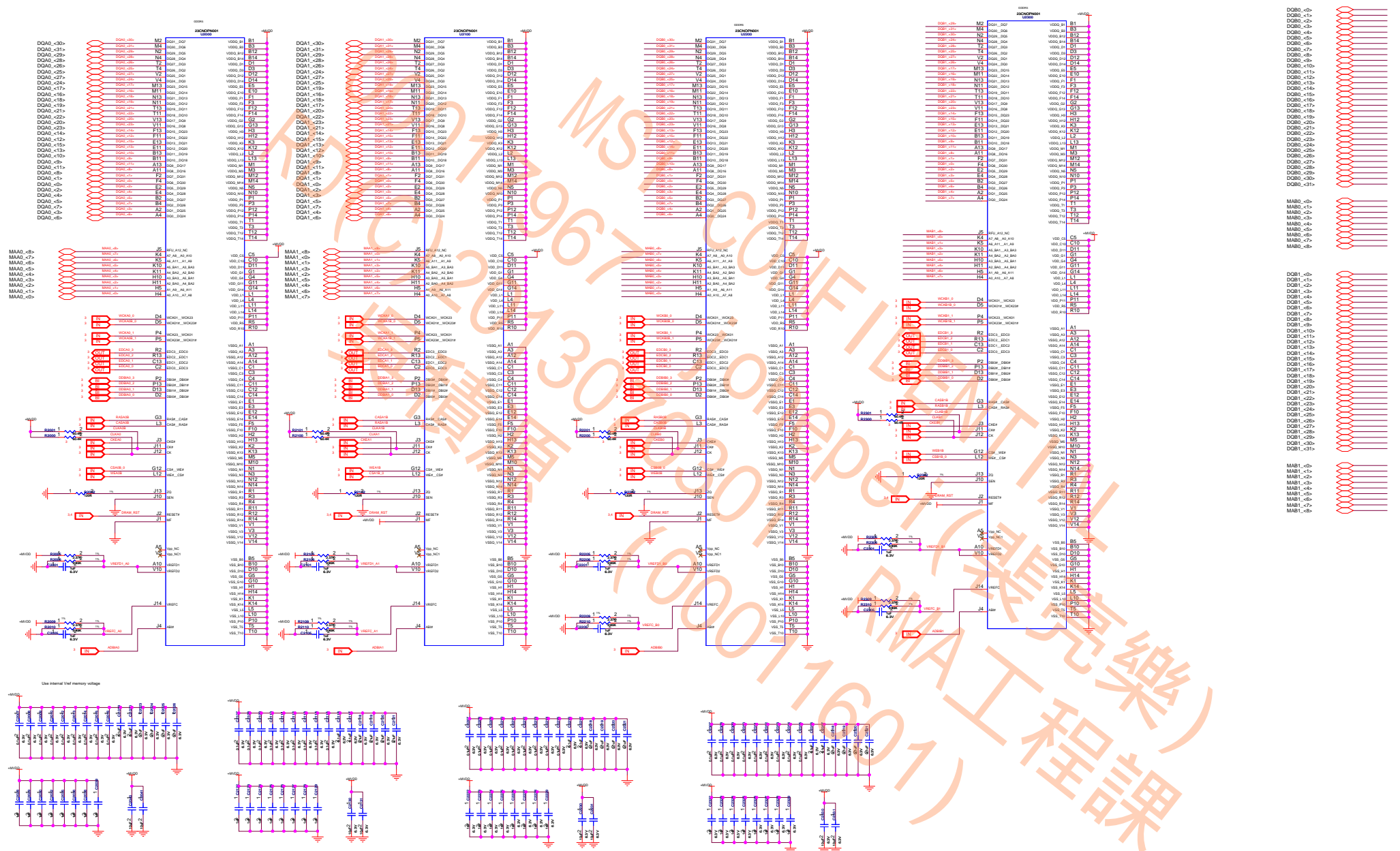
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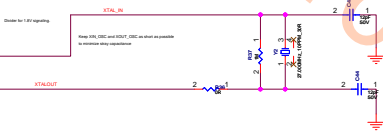
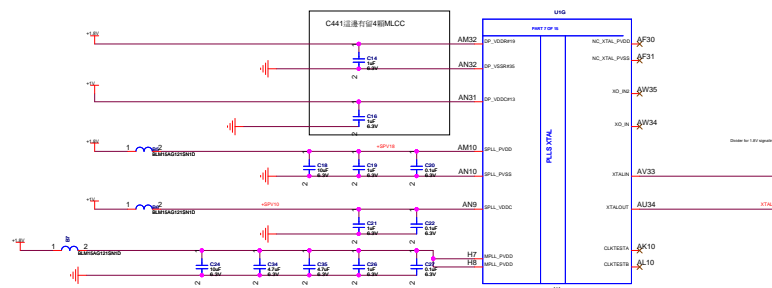
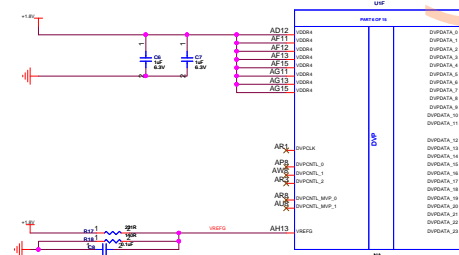
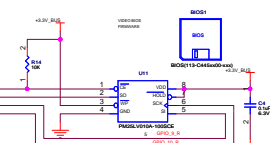
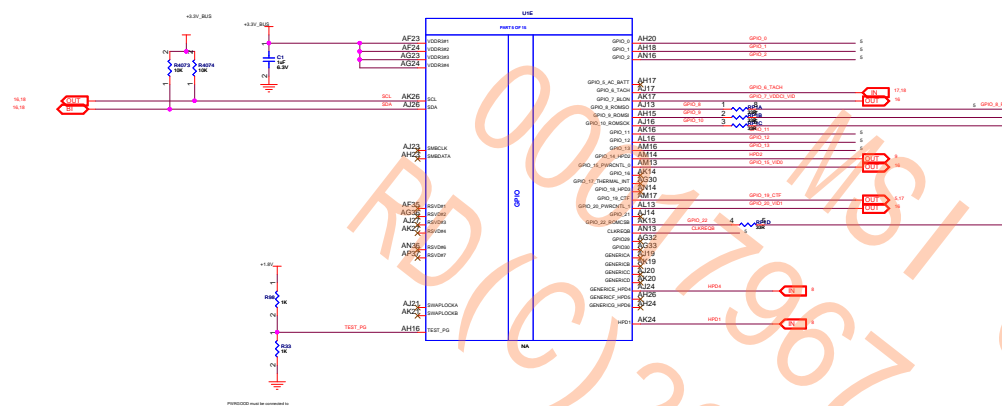
SYMBOL LEGEND	
DNI	DO NOT INSTALL
\neq	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

NOTE: Some of the PCIE testpoints will be available through vias on traces.

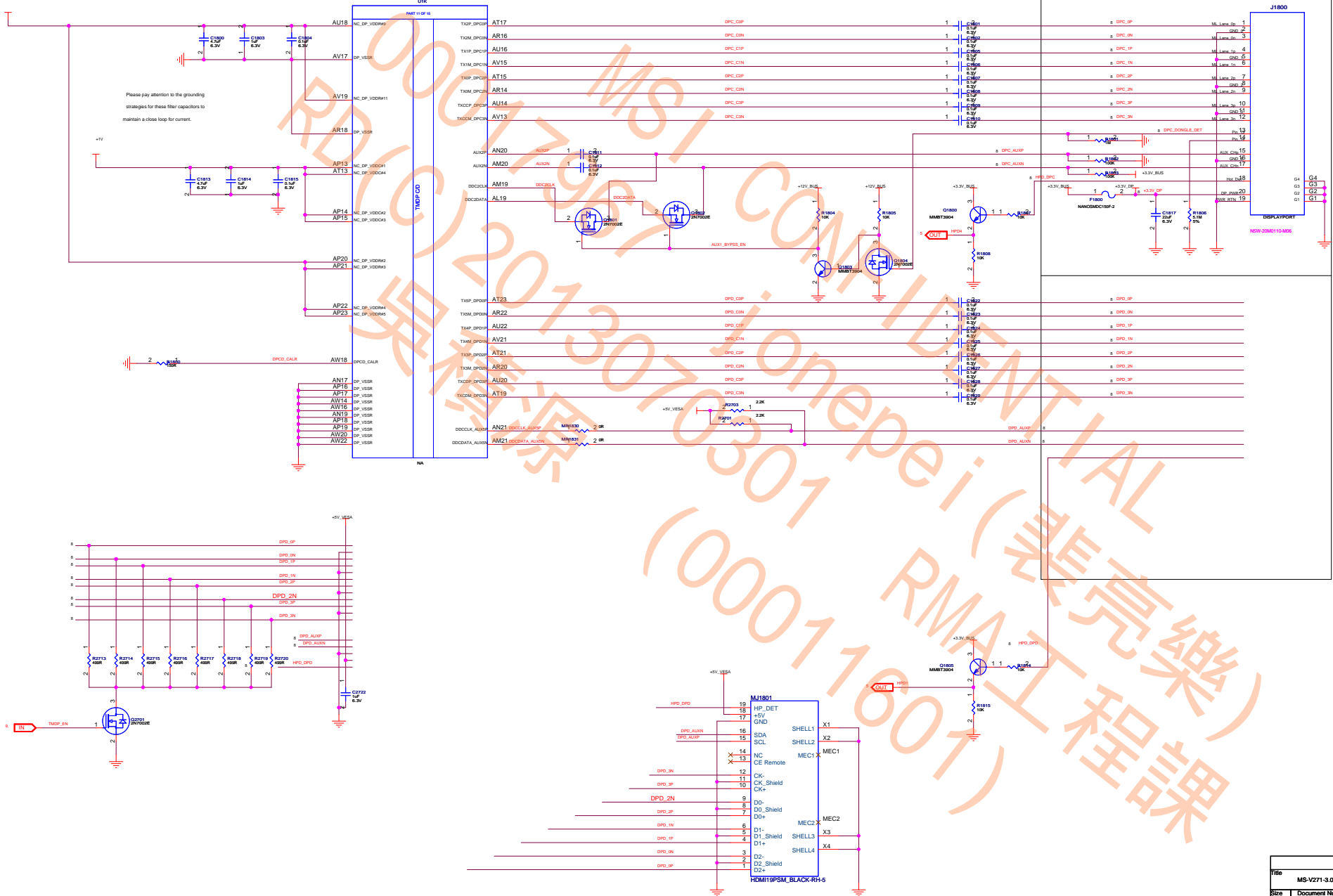




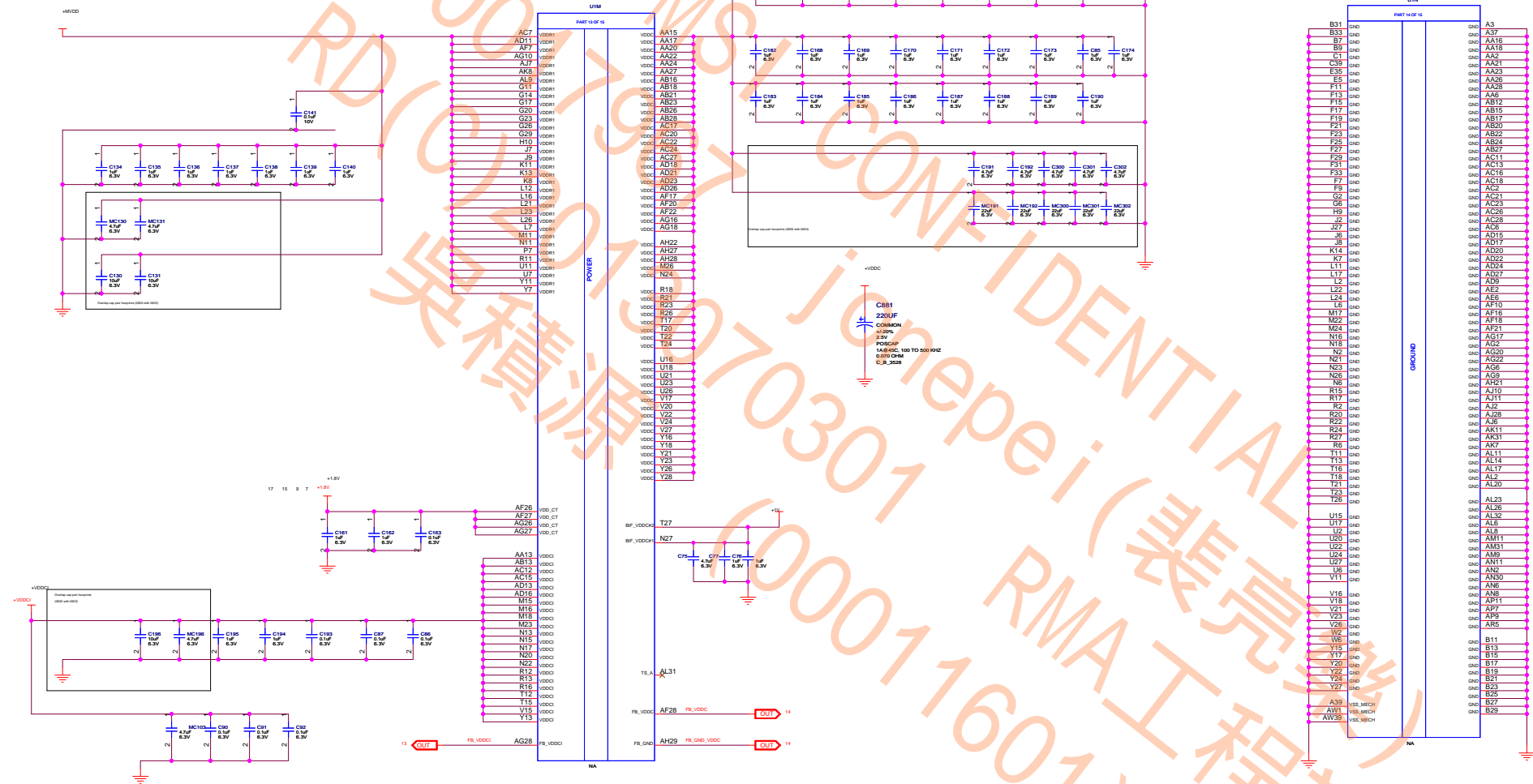




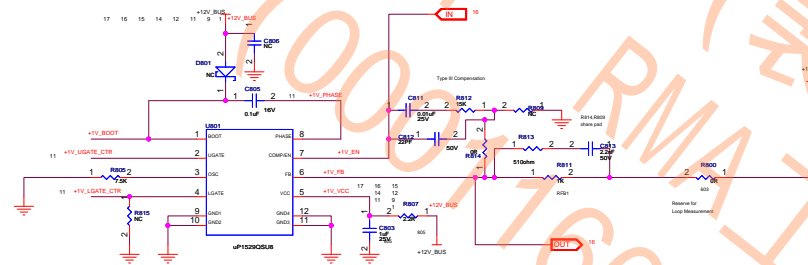
+1.8V



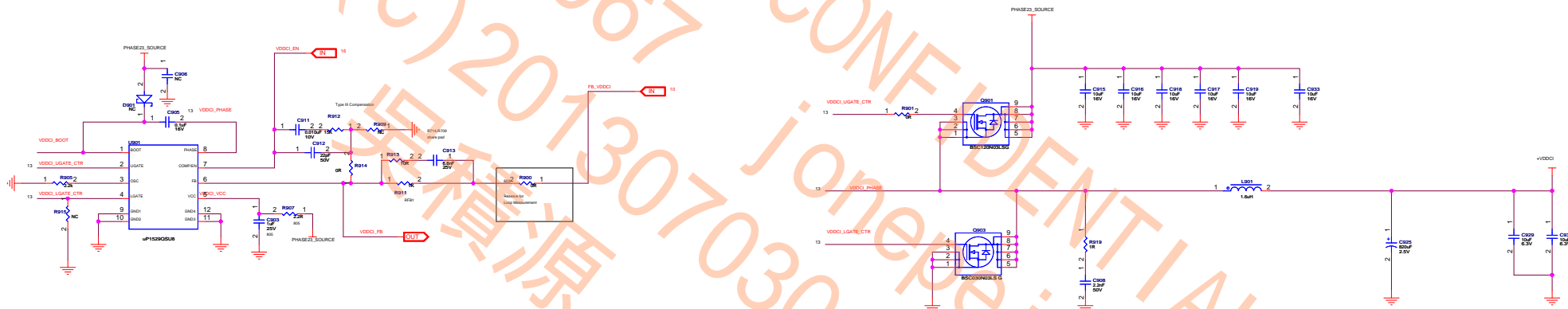
CAPE VERDE Power & GND



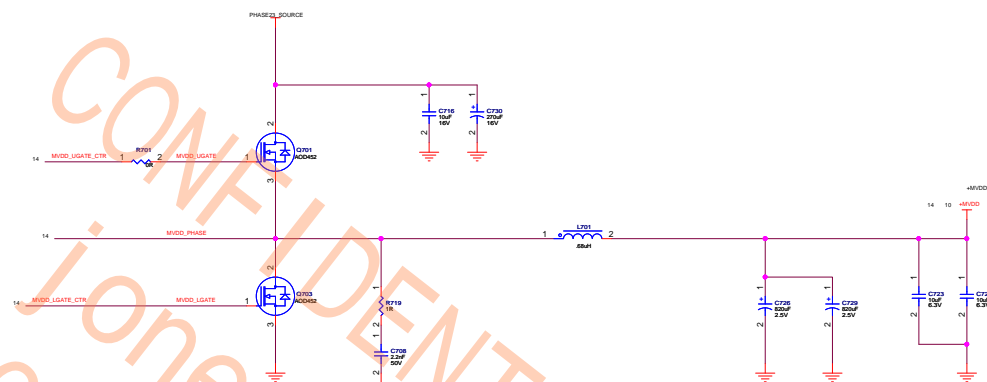
Title			
MS-V271-3.0 (AMD C445->C441)			
Size	Document Number	Rev	
Custom	2011-12-14-01	01	
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Title MS-V271-3.0 (AMD C445->C441)				
Size Custom	Document Number 2011-12-14-01			Rev 01
Date:	Friday, February 24, 2012	Sheet	11	of 21

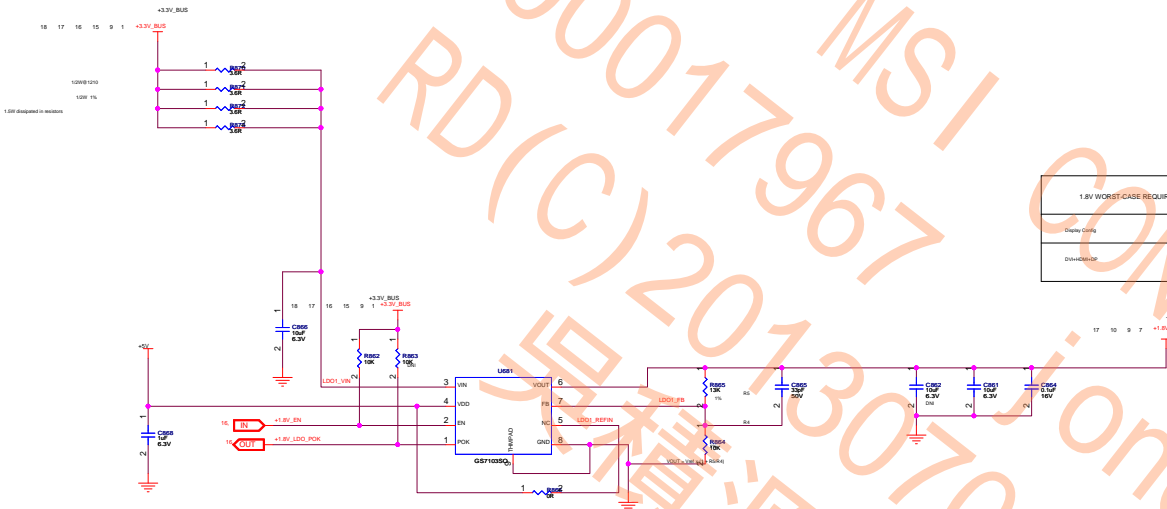


Title		
MS-V271-3.0 (AMD C445-C441)		
Size	Document Number	Rev
Customer	2011-12-14-01	01
Date:	Friday, February 24, 2012	Sheet 13 of 21



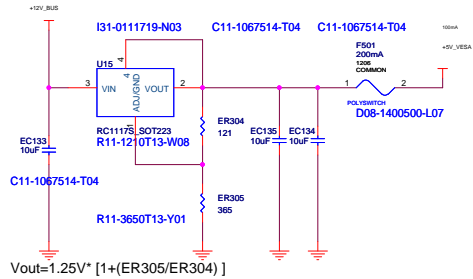
Linear Regulators

LDO #1:	Vin = 3.00V to 3.60V (3.3V ±1.5%)	Vout = +1.8V ±1.2%	Iout = 1.6A (TbV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling			

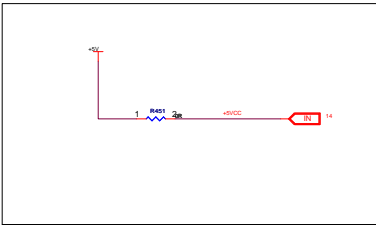


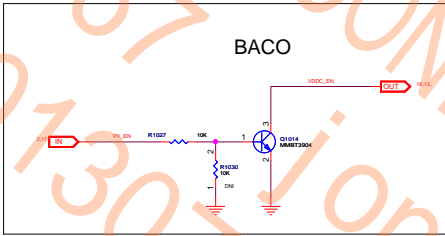
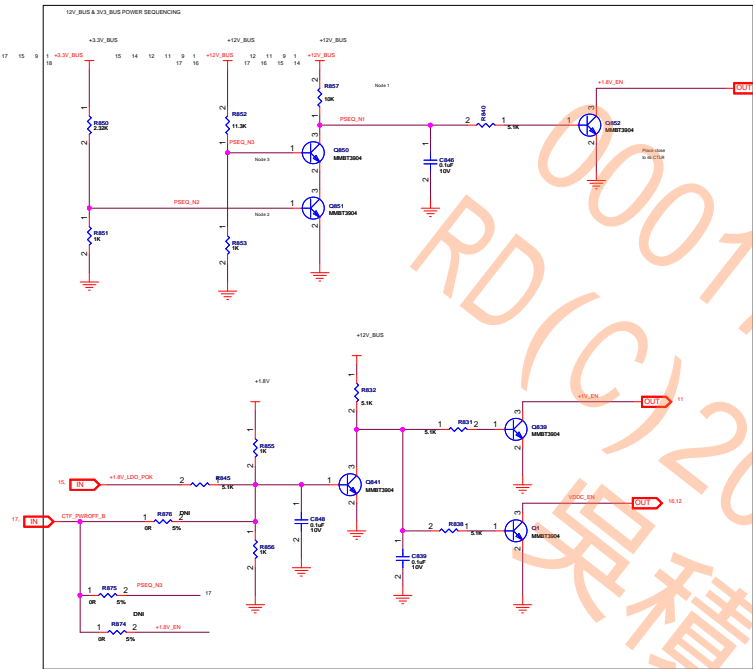
1.8V WORST CASE REQUIREMENT	
Output Current	Edi Current
Discharge Rate	Max

Regulators for +5V, +5V_VESA and +5V_VESA2
--

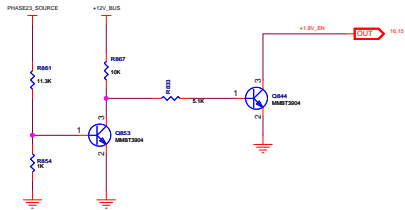
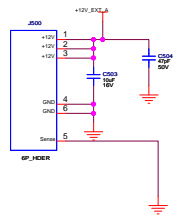
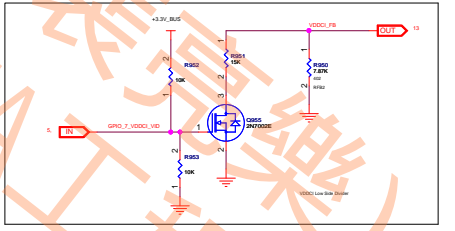
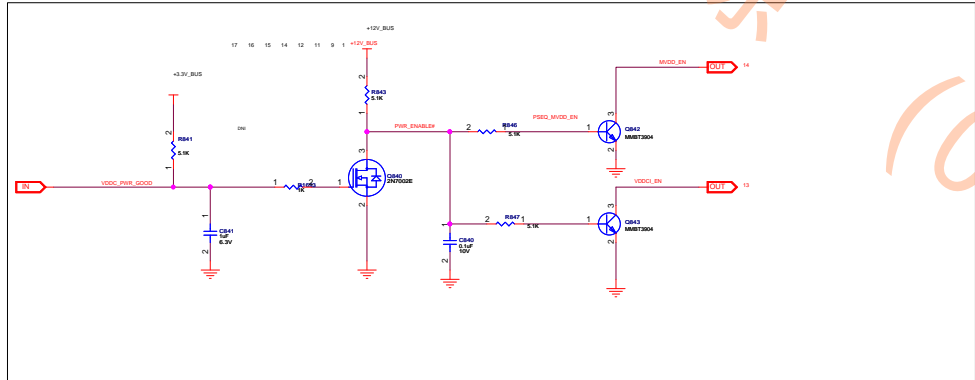


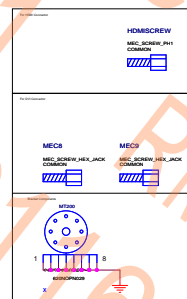
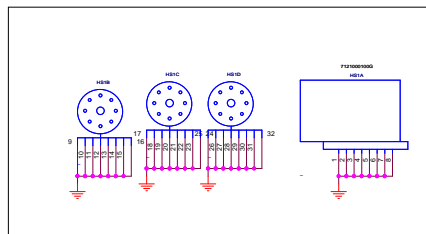
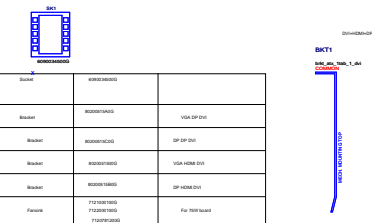
Change +5V REGULATOR to A1117
copy from MS-V208-5.0

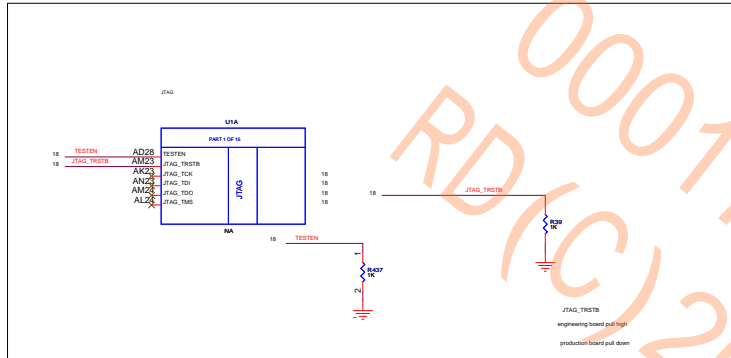


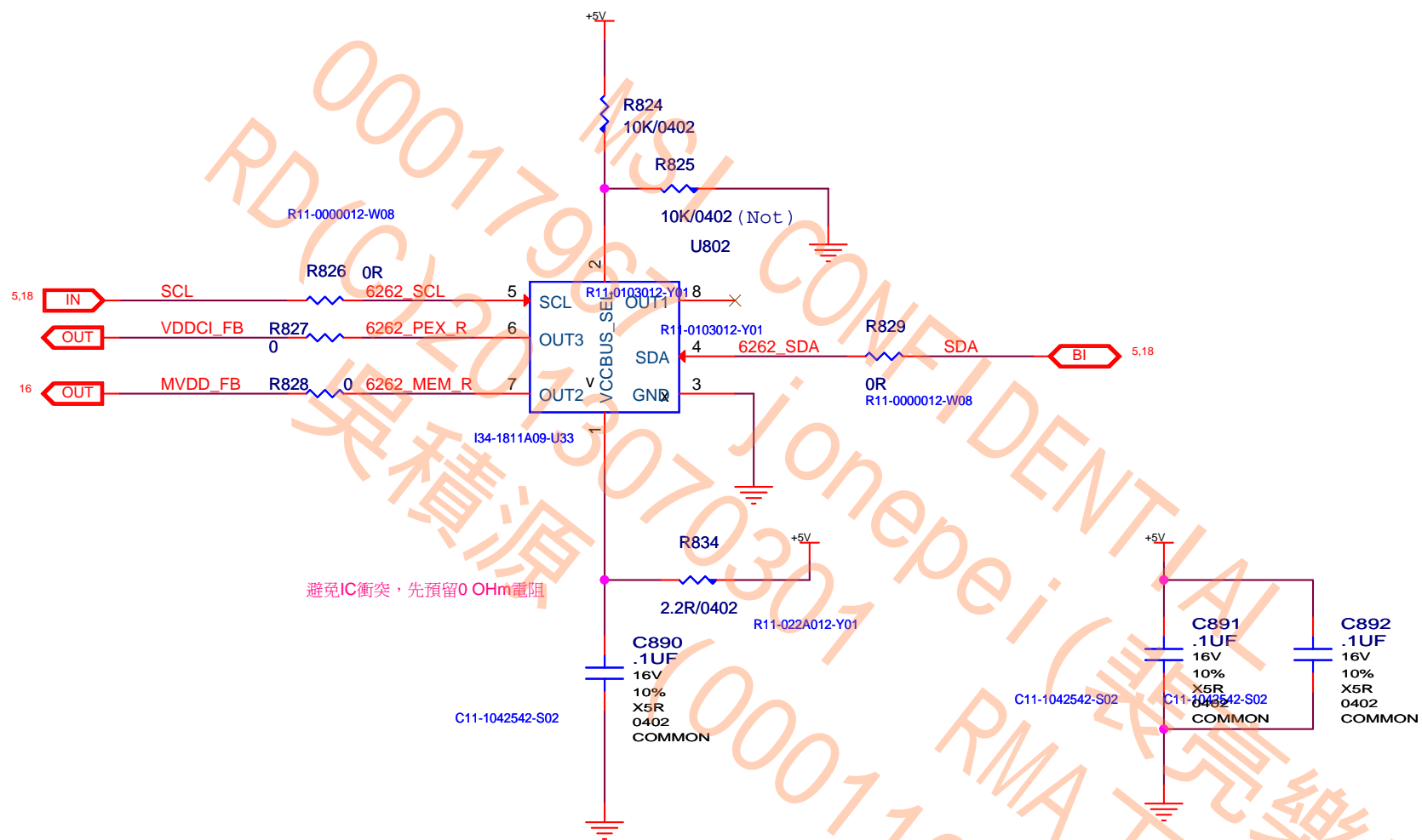


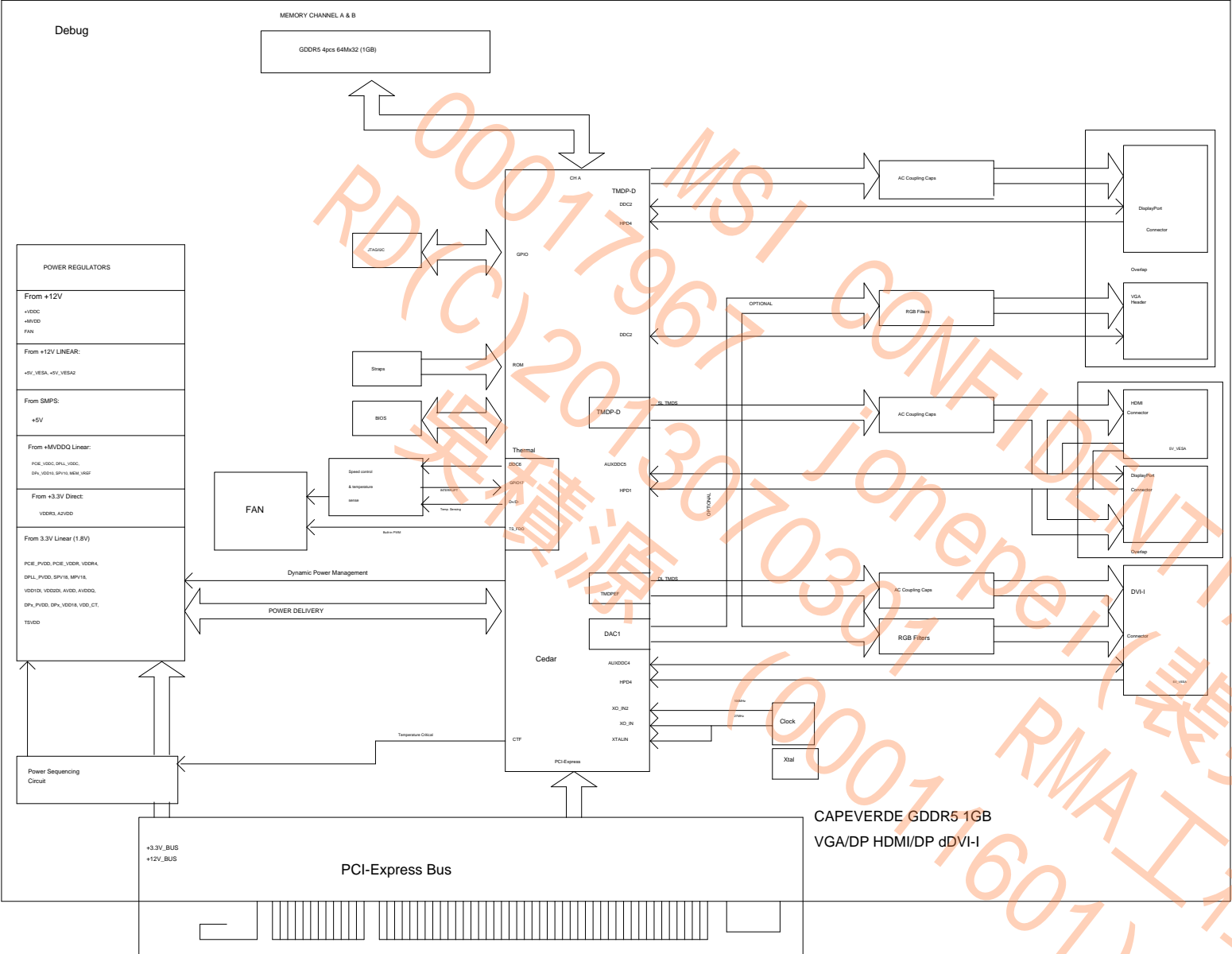
POWER SEQUENCING CIRCUIT











CAPEVERDE GDDR5 1GB
VGA/DP HDMI/DP dDVI-I

Title			MS-V271-3.0 (AMD C445->C441)
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Cus	0011-12-14-01	01	
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			TITLE	SCHEMATIC NO.	DATE
			CAPE VERDE PRO GD005 686A32 45V11H8M00P-0P1V0A	105-CH4500-00	
REVISION HISTORY			NOTE		
			THIS DOCUMENT REPRESENTS THE FINAL DESIGN. ANY CHANGES TO THE DESIGN SHALL BE MADE BY THE CUSTOMER. FOR FURTHER INFORMATION, PLEASE CONTACT THE PRODUCT SUPPORT TEAM. PLEASE CONTACT AND APPROVE ANY CHANGES TO THE DESIGN BEFORE IMPLEMENTING THEM IN THE APPLICATION DESIGN.		
SCN	PCB	DATE	REVISION DESCRIPTION		
REV	REV				
01	001	20110101	Initial CAPE VERDE schematic		
02	001	20110601	1. Update BOM of CAPE VERDE schematic 2. Add BOM of CAPE VERDE schematic 3. Add BOM of CAPE VERDE schematic 4. Add BOM of CAPE VERDE schematic		
03	001	20110601	1. Update BOM of CAPE VERDE schematic 2. Add BOM of CAPE VERDE schematic 3. Add BOM of CAPE VERDE schematic 4. Add BOM of CAPE VERDE schematic		
04	001	20110601	1. Update BOM of CAPE VERDE schematic 2. Add BOM of CAPE VERDE schematic 3. Add BOM of CAPE VERDE schematic 4. Add BOM of CAPE VERDE schematic		
05	001	20110601	1. Update BOM of CAPE VERDE schematic 2. Add BOM of CAPE VERDE schematic 3. Add BOM of CAPE VERDE schematic 4. Add BOM of CAPE VERDE schematic		
06	001	20110601	1. Update BOM of CAPE VERDE schematic 2. Add BOM of CAPE VERDE schematic 3. Add BOM of CAPE VERDE schematic 4. Add BOM of CAPE VERDE schematic		



Smart3D Changelog
Instruction: Please specify "PARTNER SCHEMATIC PART NUMBER:" on the following table and please insert a "X" in the "YES" "NO" "Not Applicable" column as appropriate. Please specify "AMD Ref schematic =" on the following table.

PARTNER SCHEMATIC CHANGE NOTE				
PARTNER SCHEMATIC PART NUMBER:				
AMD REFERENCE SCHEMATIC USED: C445_00.DSN reference schematics				
Partner schematic pages:	Content change description			
	YES	NO	Not Applicable	Comments
Page 1	X			1. Remove SMBus
Page 2		X		
Page 3		X		
Page 4		X		
Page 5	X			1. Delete SMBus 2. Add GPIO 5 & 6 3. Delete GPIO 17 & 29 330 4. Delete U12 & relation
Page 6	X			1. Delete J1501 & relation 2. Delete ESD DIODES 3. Short L1710 & L1711 & L1712
Page 7		X		
Page 8	X			1. Delete J1801 & relation 2. Delete ESD solution
Page 9	X			1. Delete ESD solution
Page 10	X			1. Connect net FB_VDDCI & FB_VDDC & FB_GND_VDDC 2. Add C881 3. Delete MC176 & MC178 4. Reserve CAP for BIF_VDDC#1 & BIF_VDDC#2
Page 11	X			1. Change MOSFET & Cin & Cout 2. Short NS800 via 3. Delete low side Gate Resistor 4. Delete Cout * 2
Page 12	X			1. Delete all content & copy UPI solution from C441 2. Change Cin & Cout 3. Short NS* via
Page 13	X			1. Short NS900 via 2. Feedback sense from net FB_VDDCI 3. Delete low side Gate Resistor 4. Delete Cout * 3 5. Add Cin 10UF * 1
Page 14	X			1. Change Lin & Cin 2. Short NS700 via 3. Delete low side Gate Resistor 4. Delete Cout * 3 5. Delete Cin 10UF * 1
Page 15	X			1. Delete Vin reservation 2. Change 5V solution to 1117 3. Delete D450 & relation
Page 16	X			1. Add 6 pin EXT_12V 2. Add +12V_EXT_A power up sequence for +1.8V_EN 3. Add input 12V_BUS & 12V_EXT choke for core PWM 4. upon setting 1..-3. are copy from C441 5. Delete U680 & relation 6. Delete Vcore Rbot & relation
Page 17	X			1. Delete 2 pin fan & relation 2. Copy C441 4 pin fan & relation 3. Delete net GPU_DPLUS & GPU_DMINUS 4. Add MR4104 for MLPS 5. Reserve R4100 & R4409
Page 18	X			1. Delete U4001 & relation 2. Delete J4004 & relation
Page 19		X		
Page 20		X		