

PG132-A02

370W, FH Std PCB, 384b, GDDR6x 2CH X16
DP + DP + DP + HDMI/DP

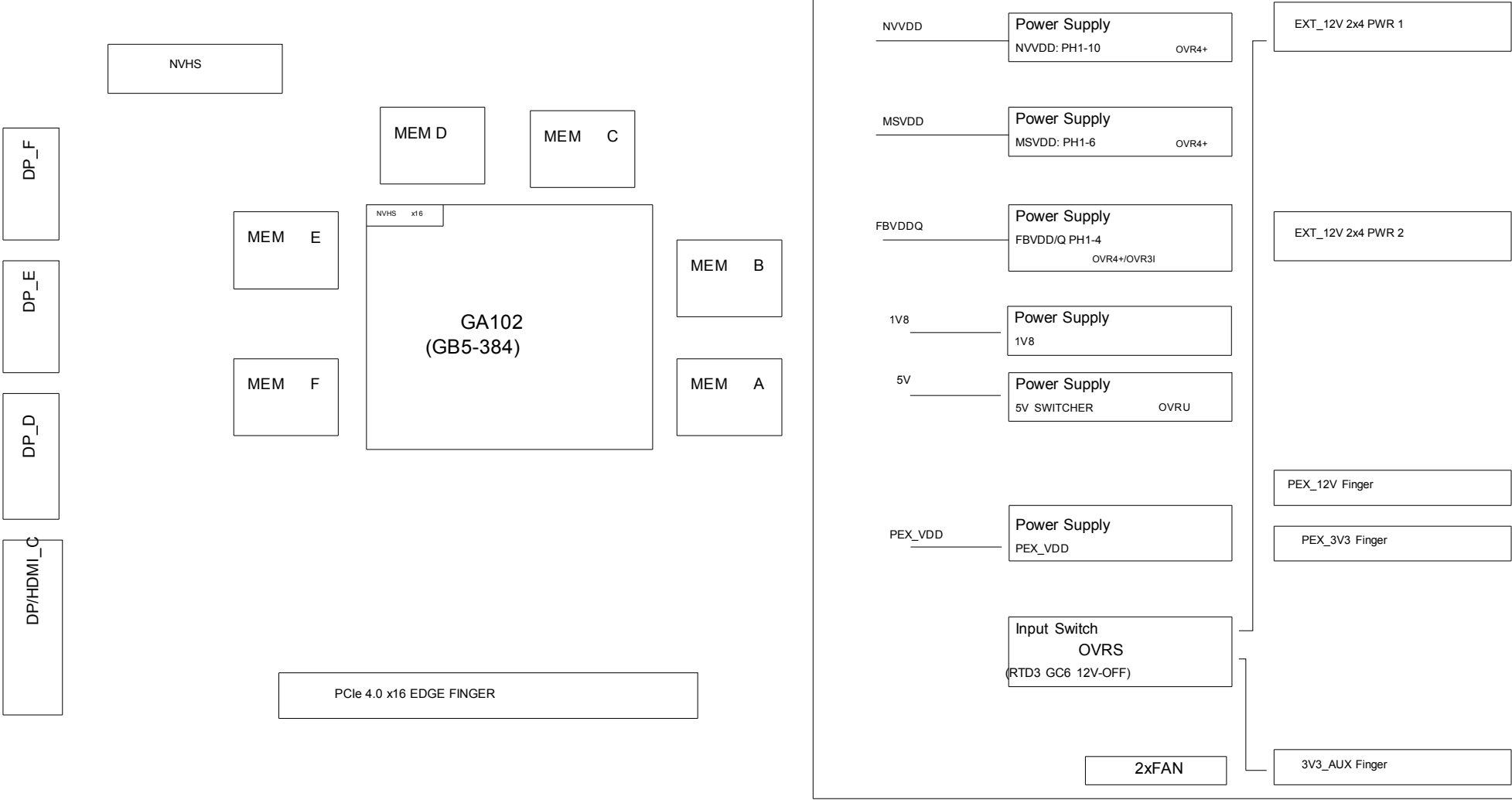
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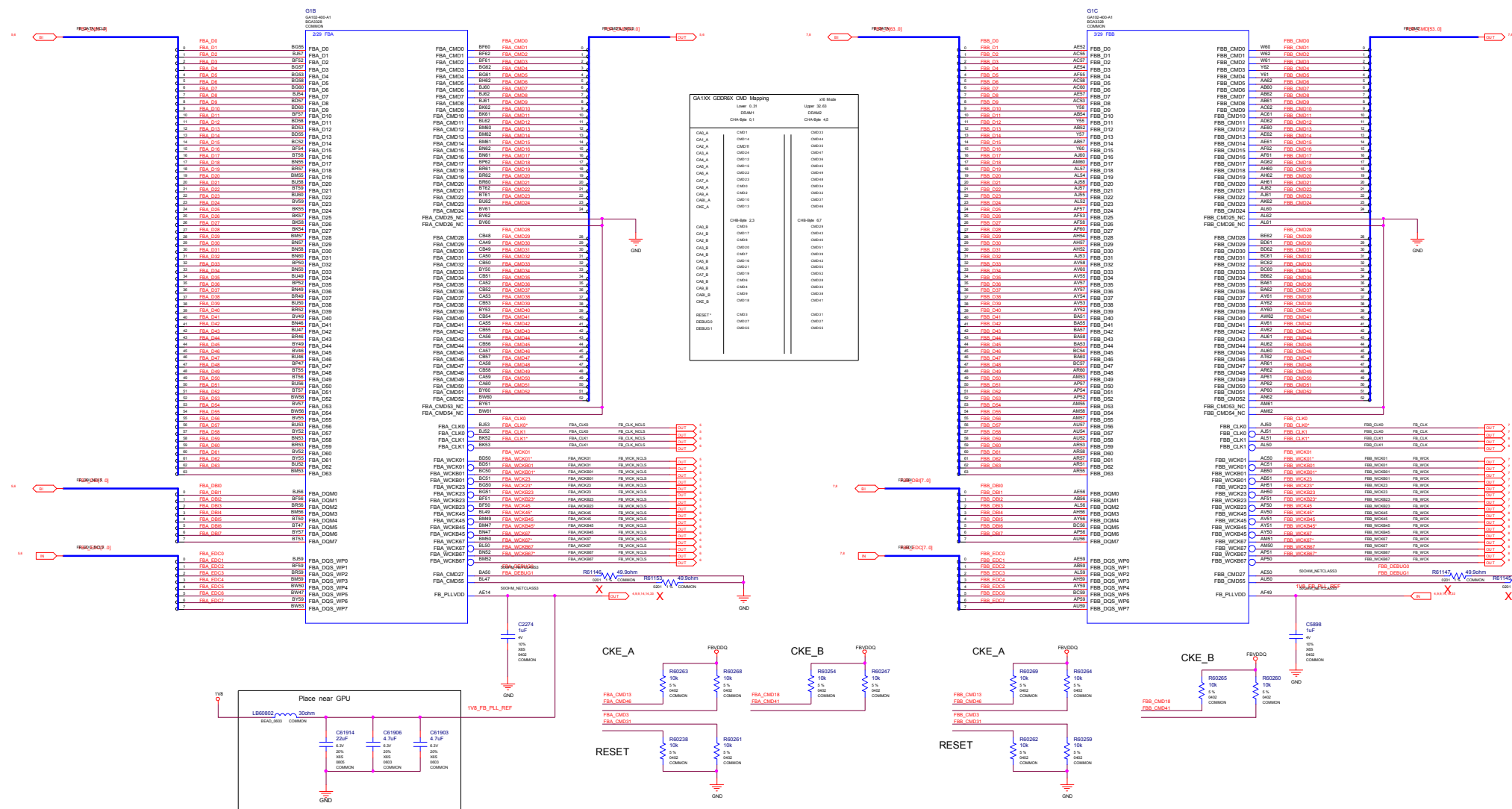
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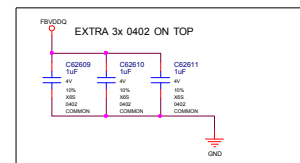
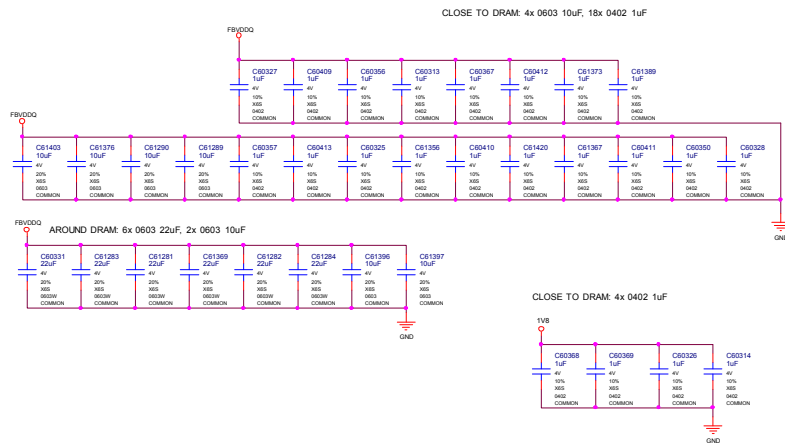
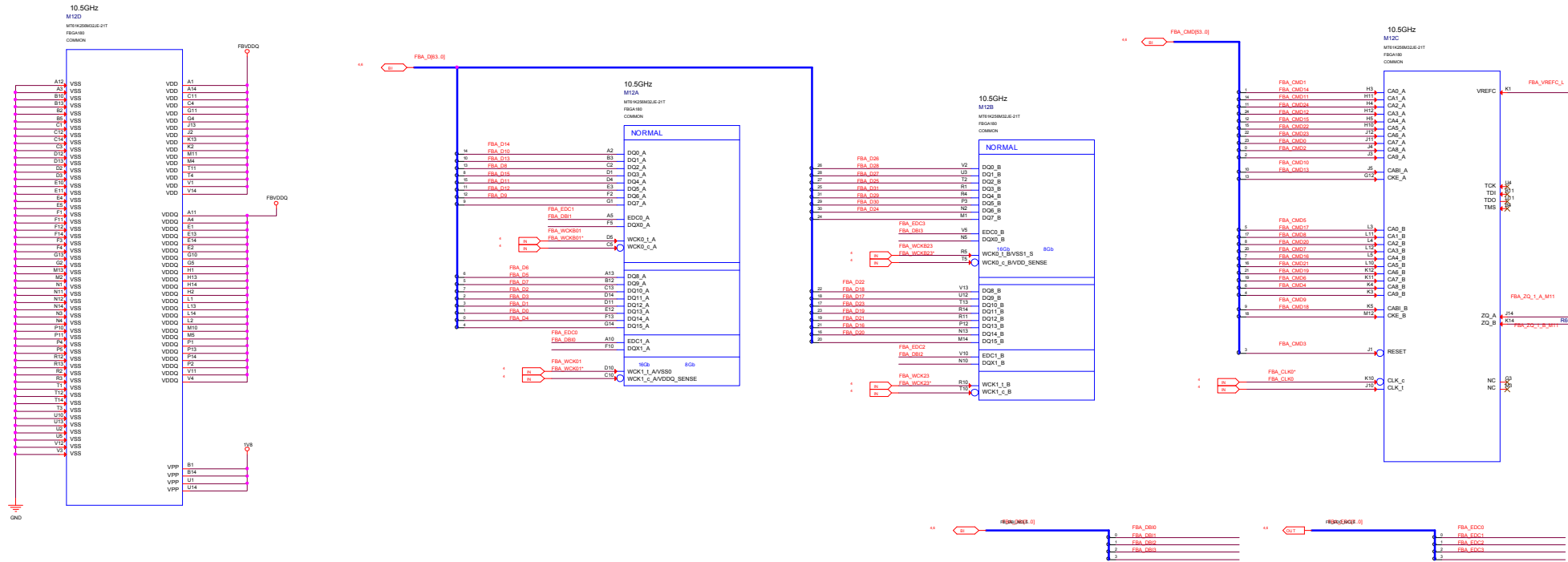
Block Diagram



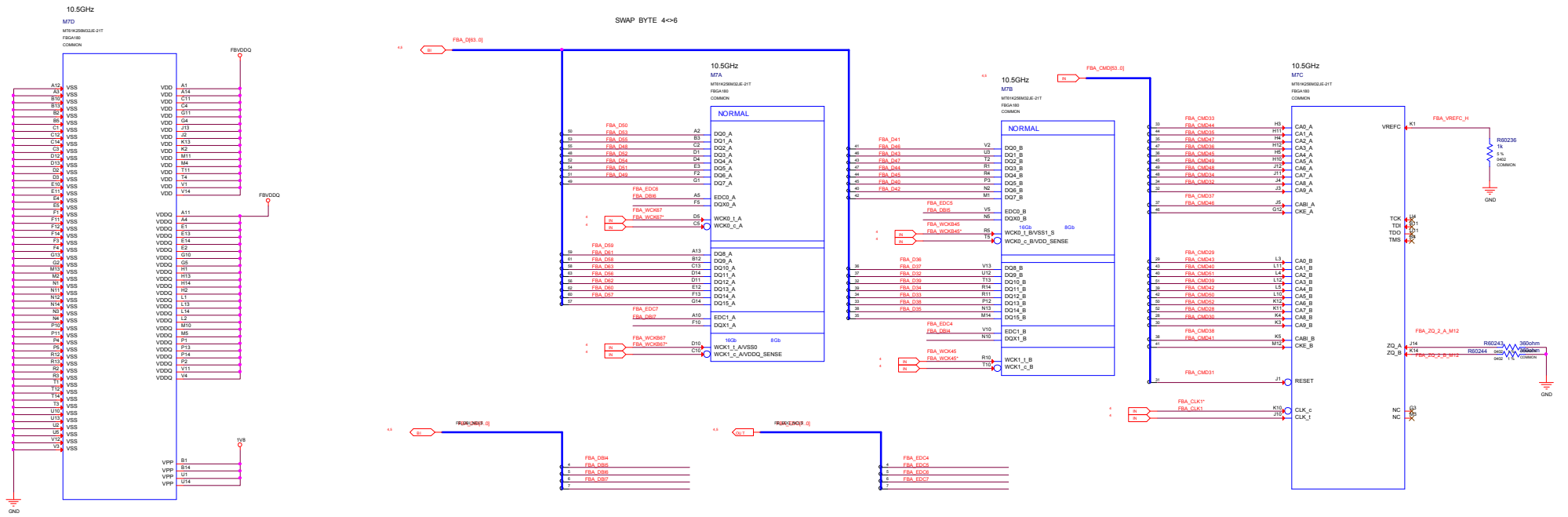
MEMORY: GPU Partition A/B



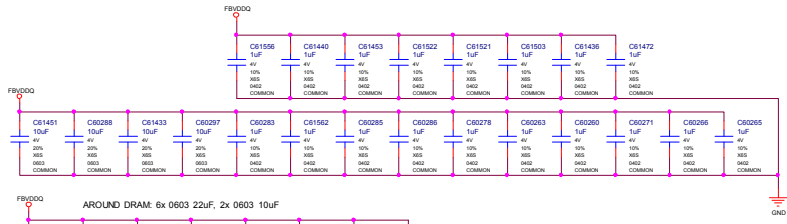
MEMORY: FBA Partition 31..0



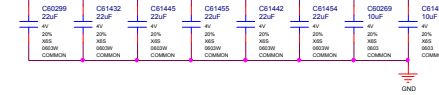
MEMORY: FBA Partition 63..32



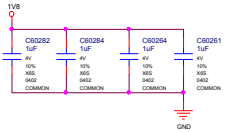
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



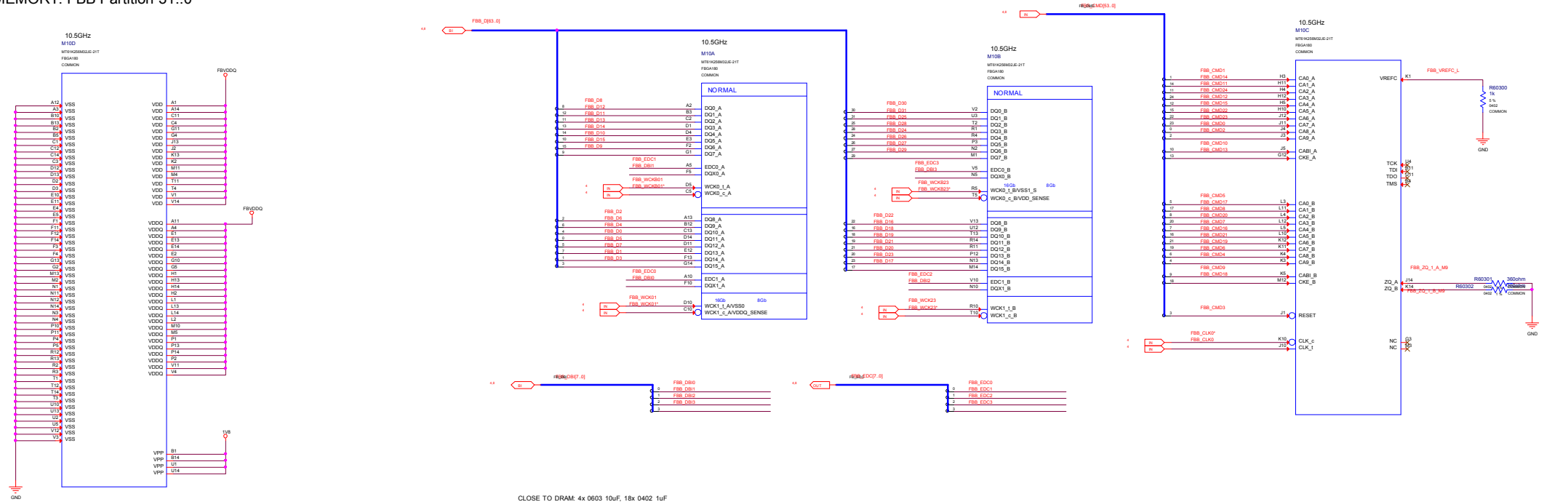
AROUND DRAM: 6x 0603 22uF, 2x 0603 10uF



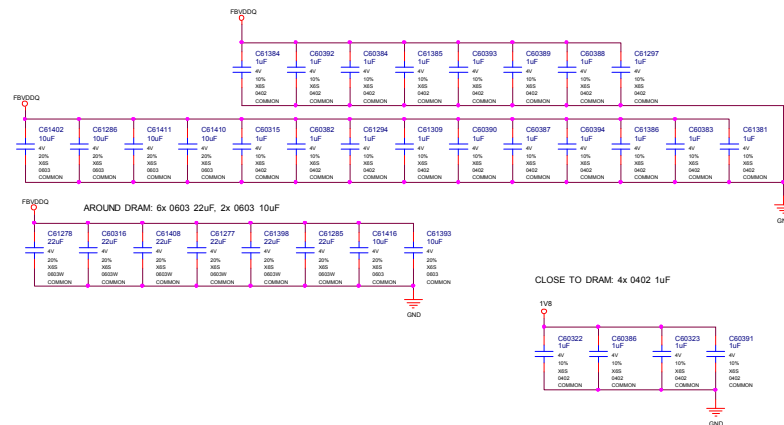
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MEMORY: FBB Partition 31..0

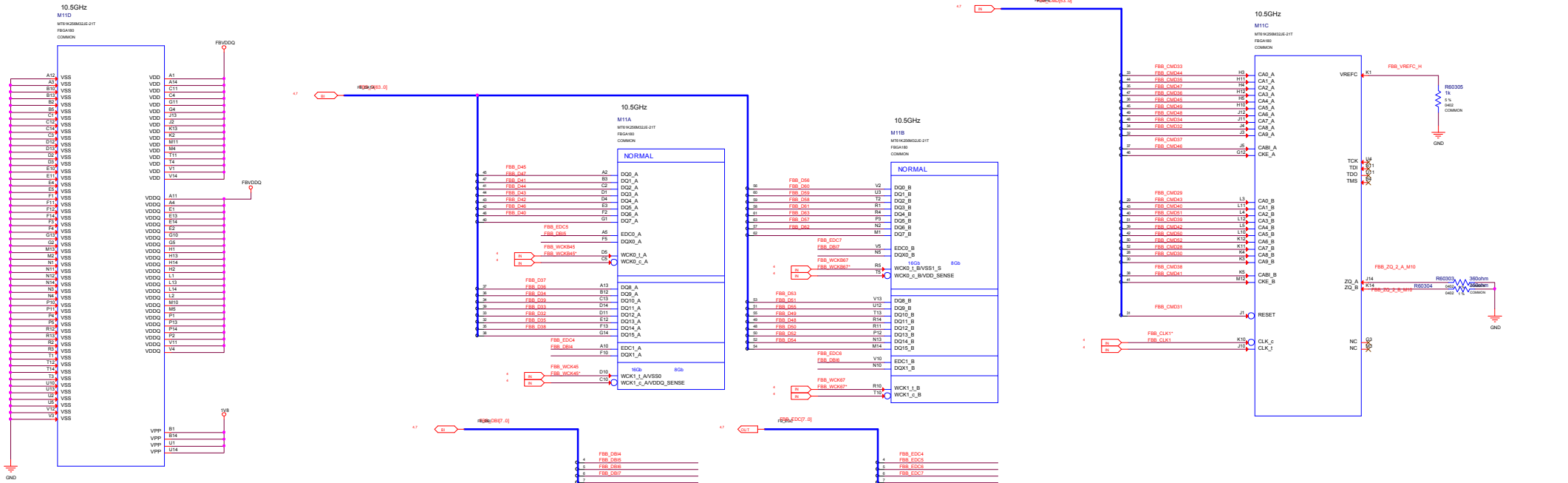


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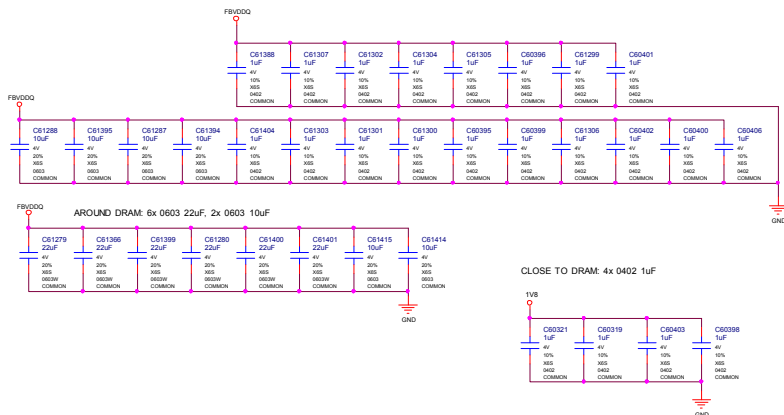


CLOSE TO DRAM: 4x 0402 1uF

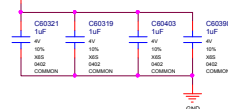
MEMORY: FBB Partition 63..32



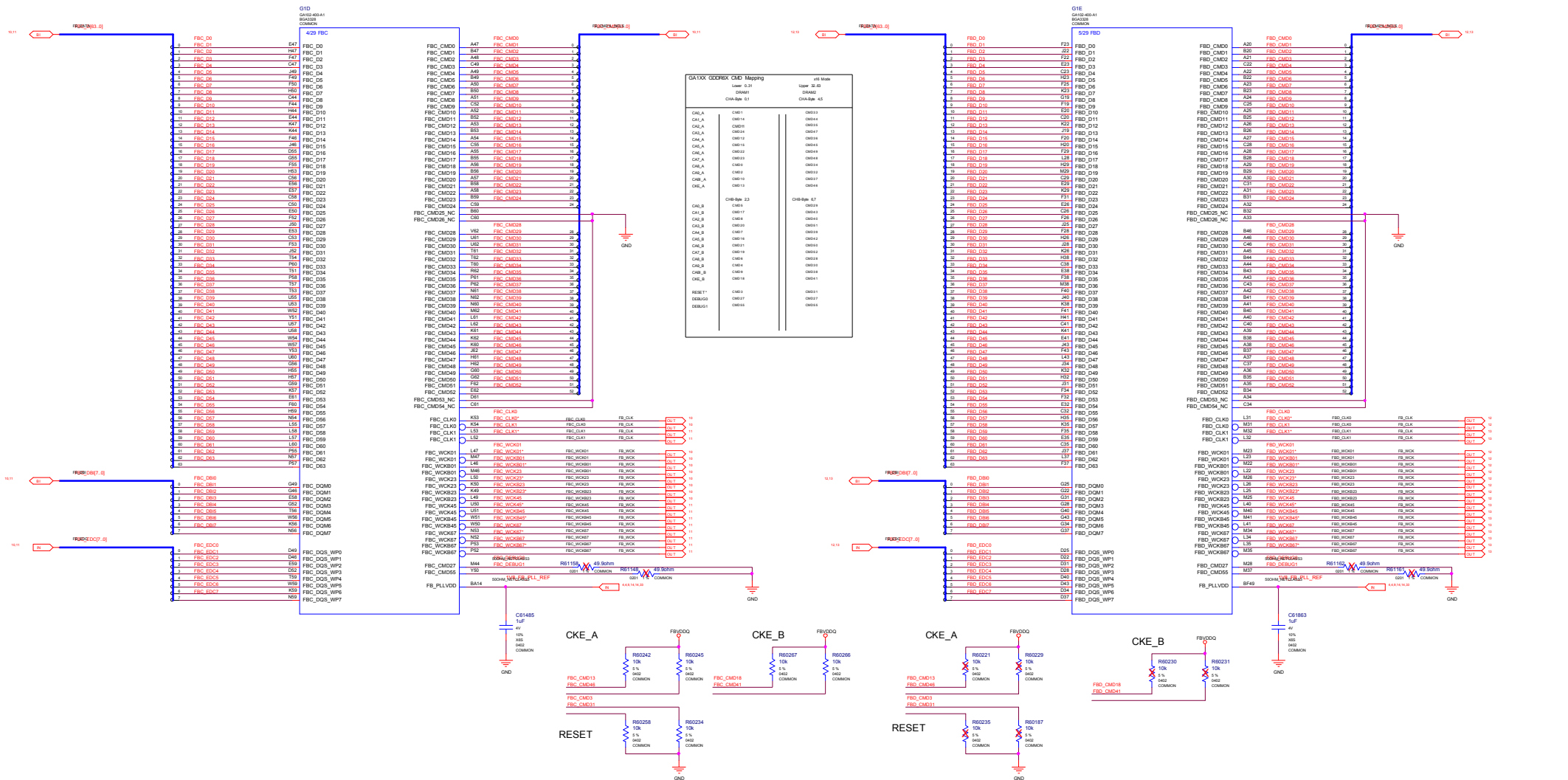
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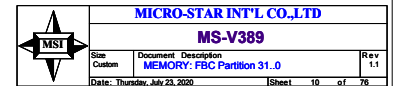
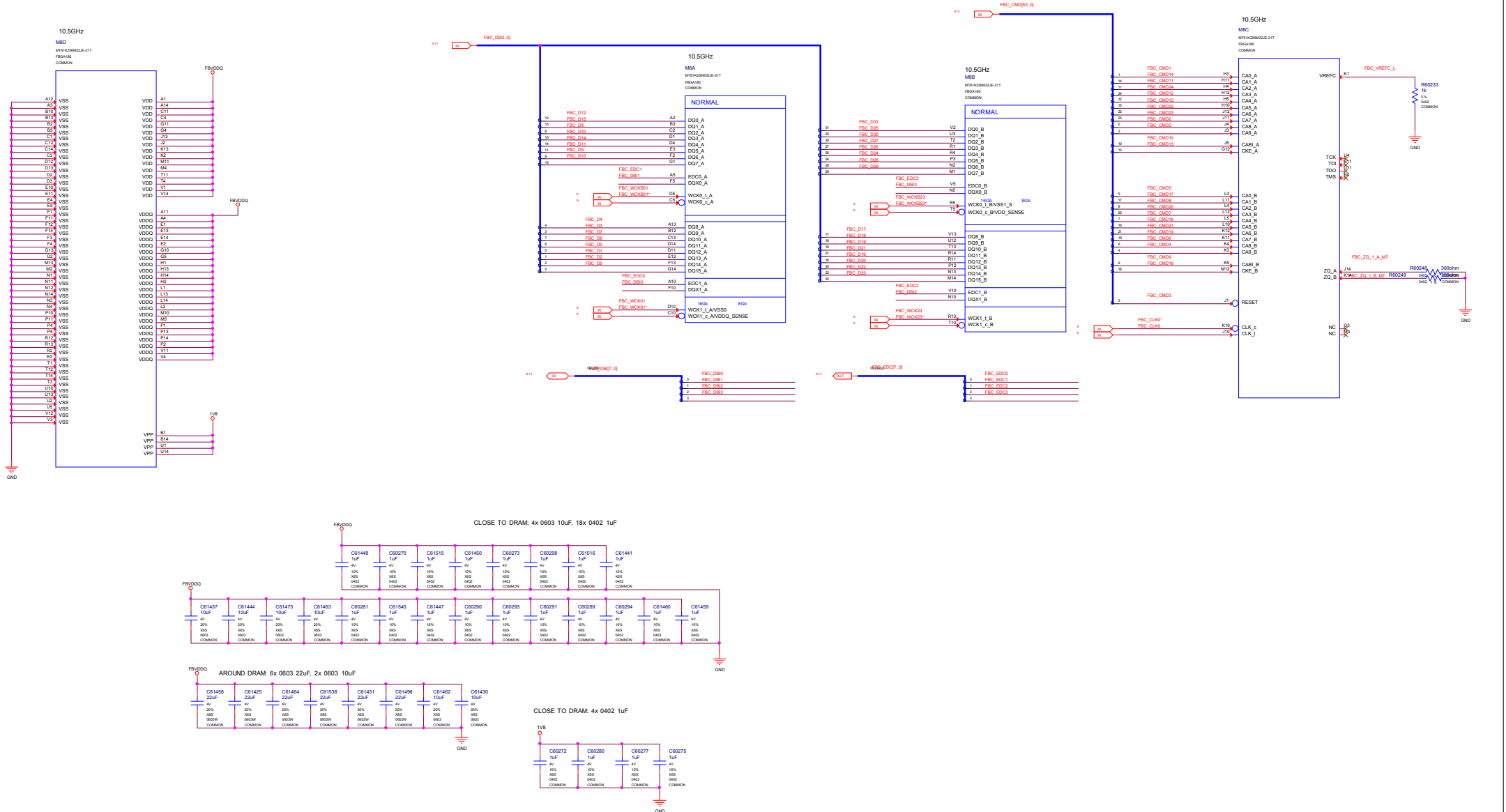
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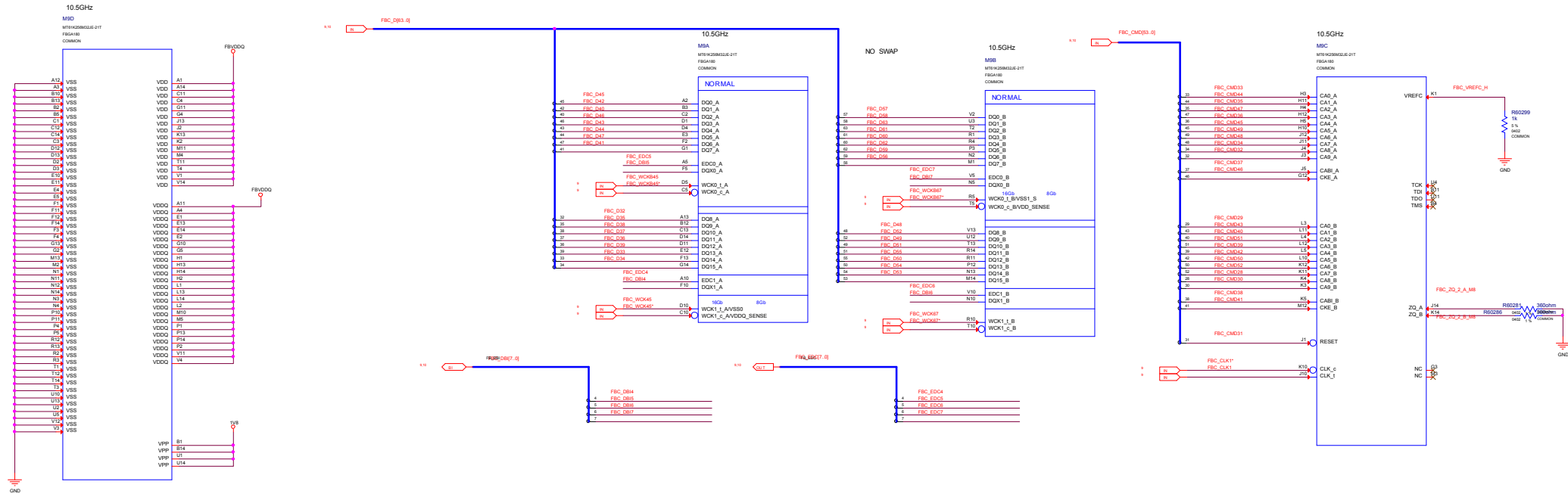
MEMORY: GPU Partition C/D



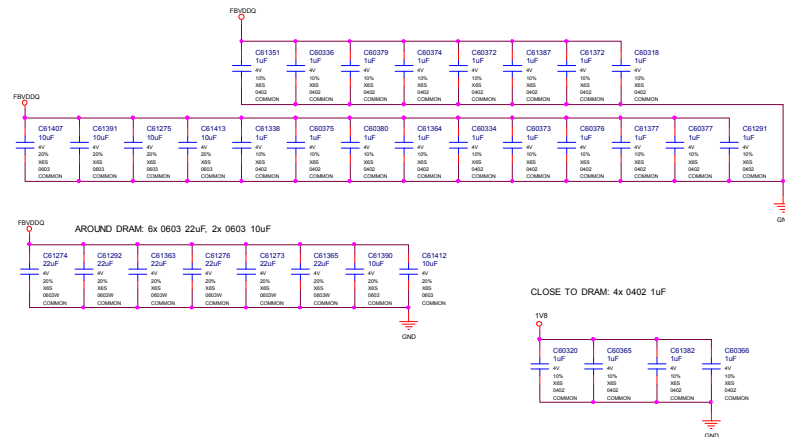
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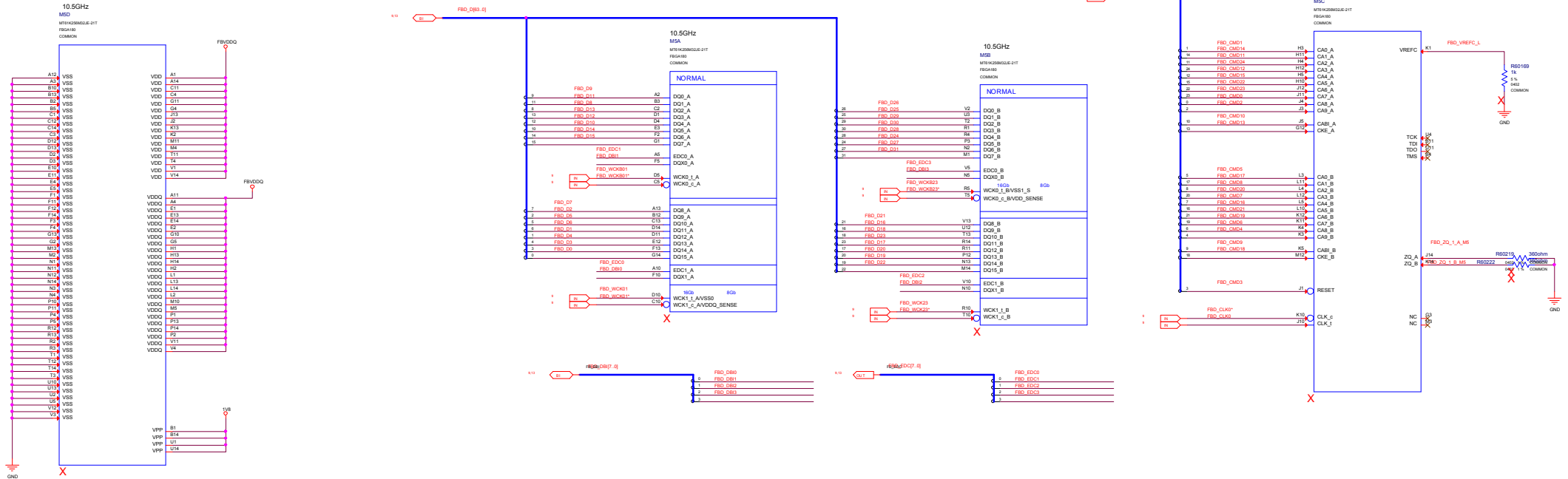
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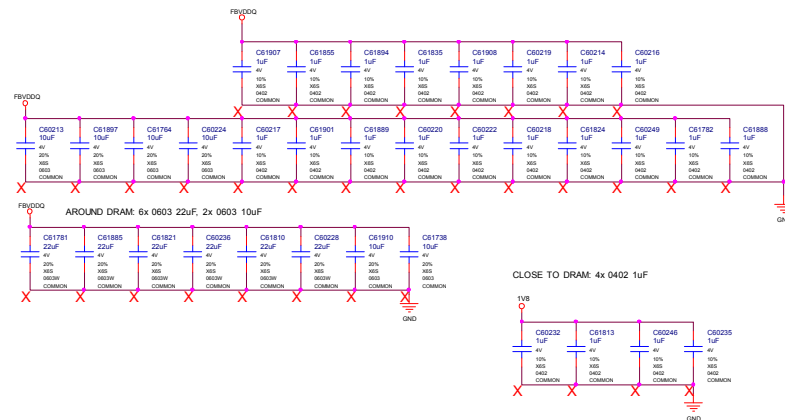
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MEMORY: FBD Partition 31..0

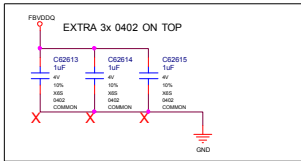
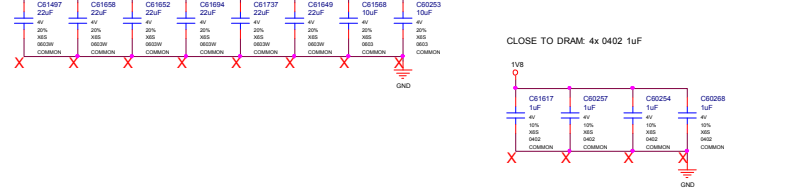
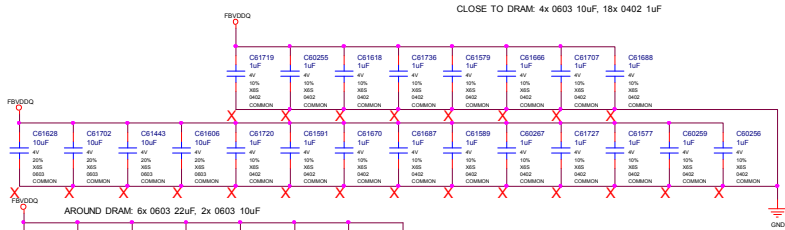
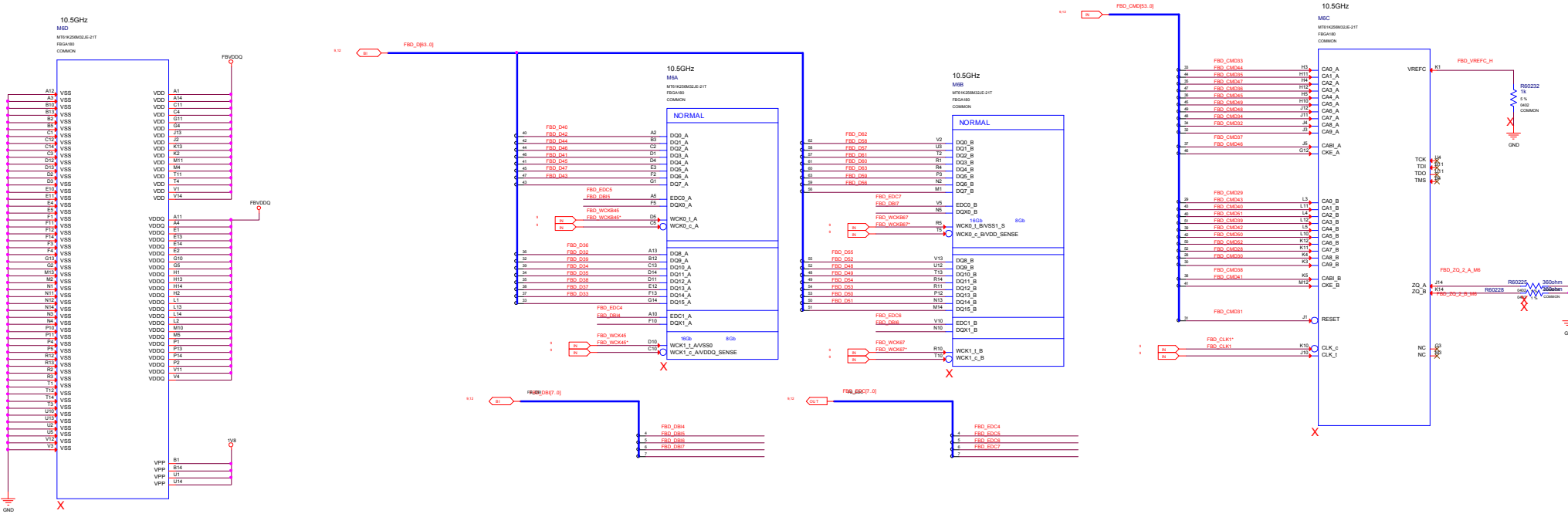


CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF

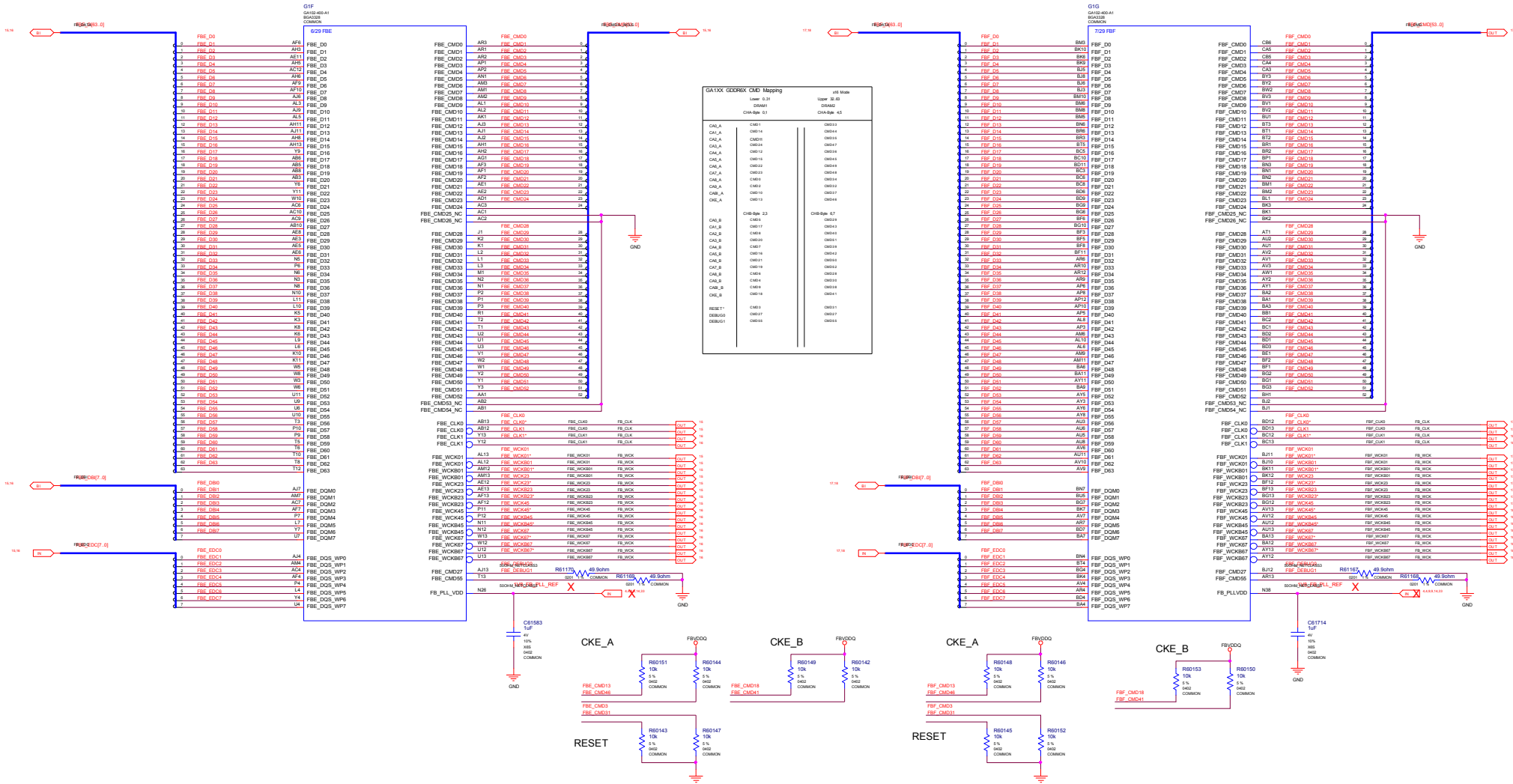


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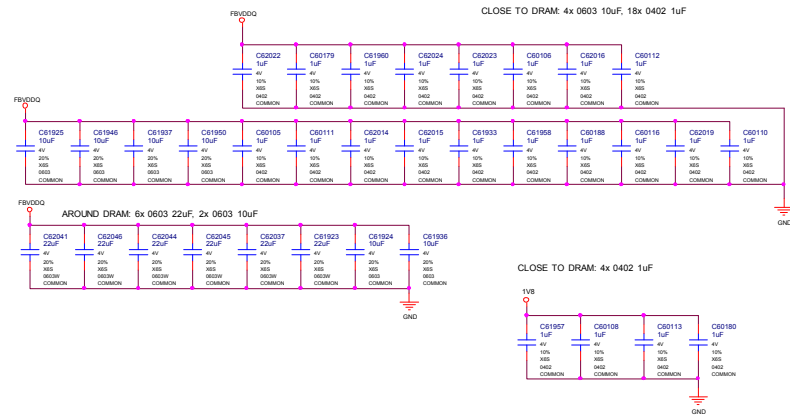
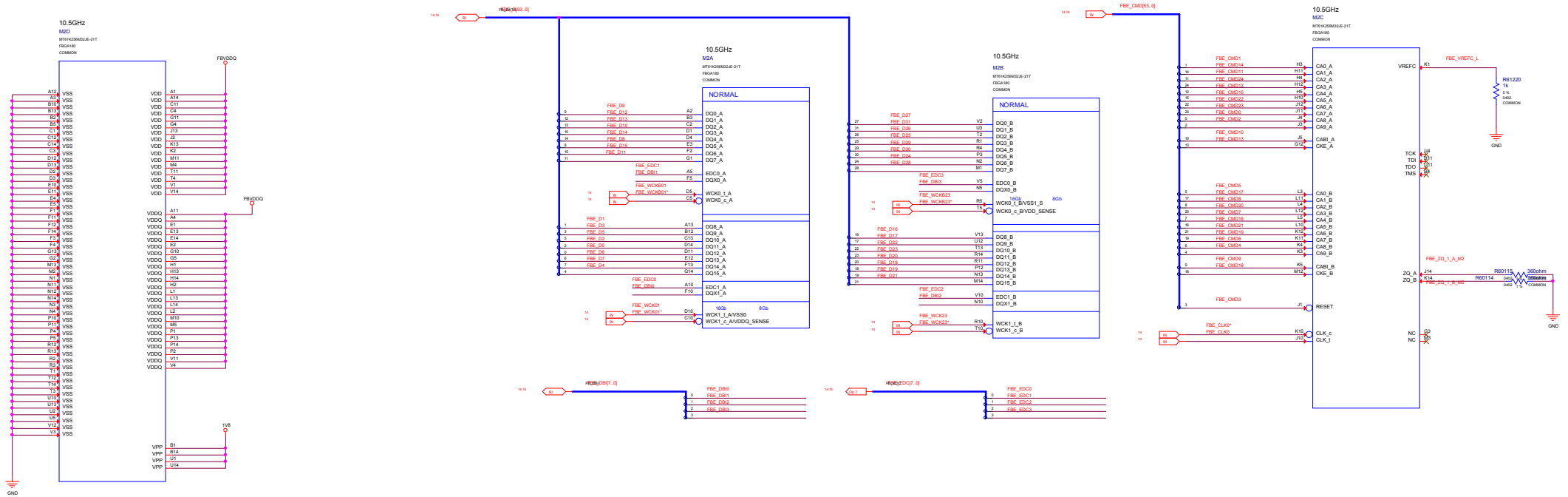
MEMORY: FBD Partition 63..32



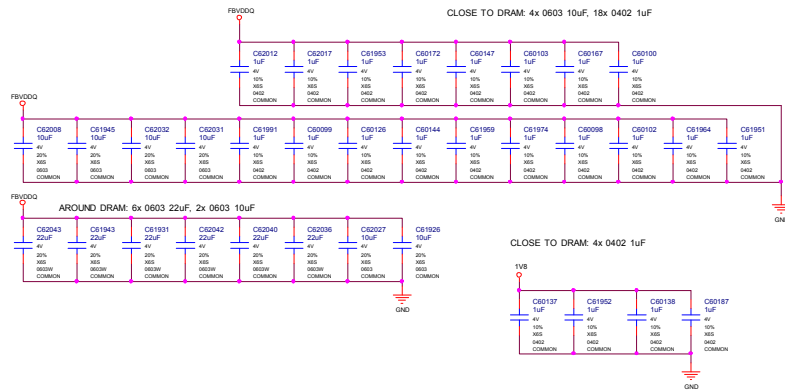
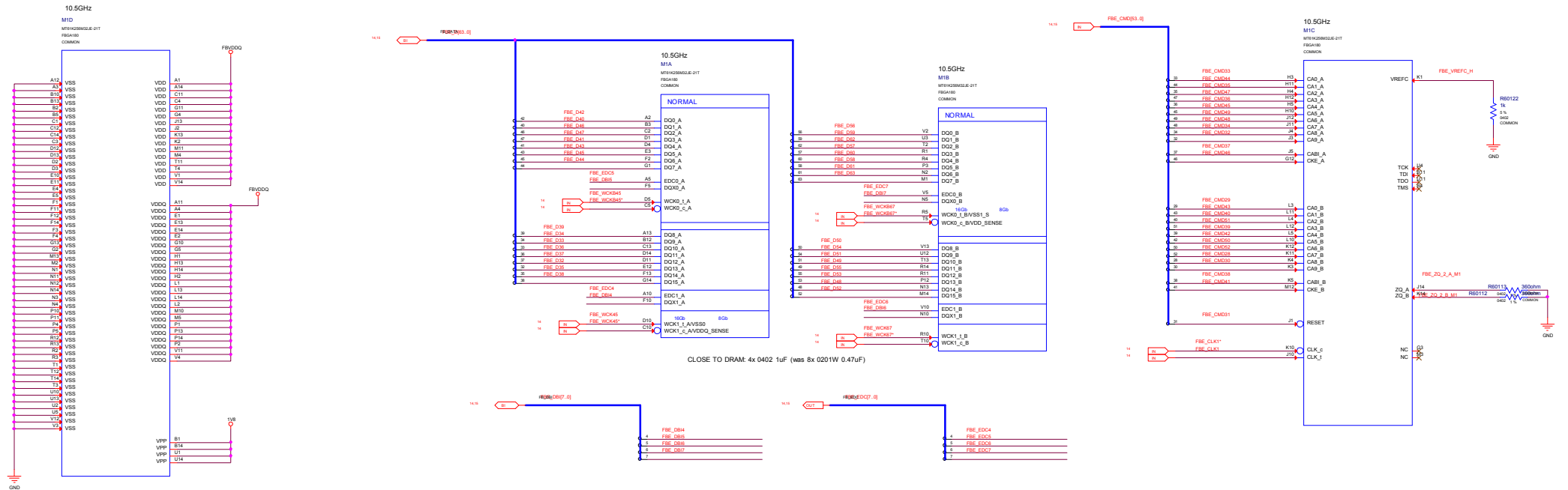
MEMORY: GPU Partition E/F



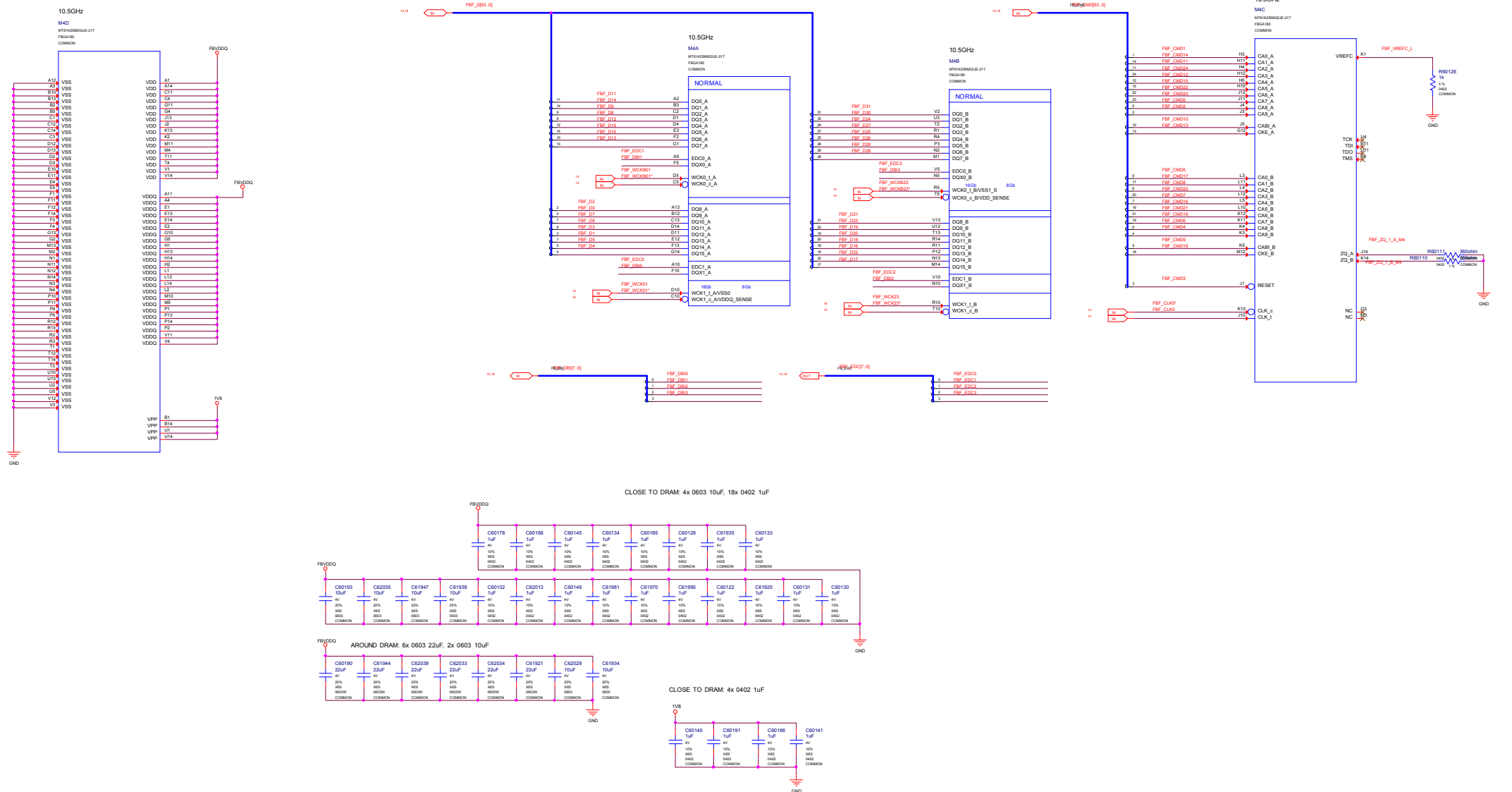
MEMORY: FBE Partition 31..0



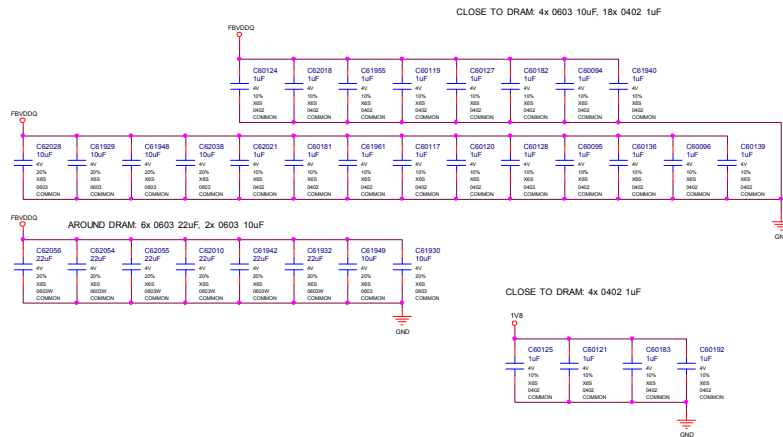
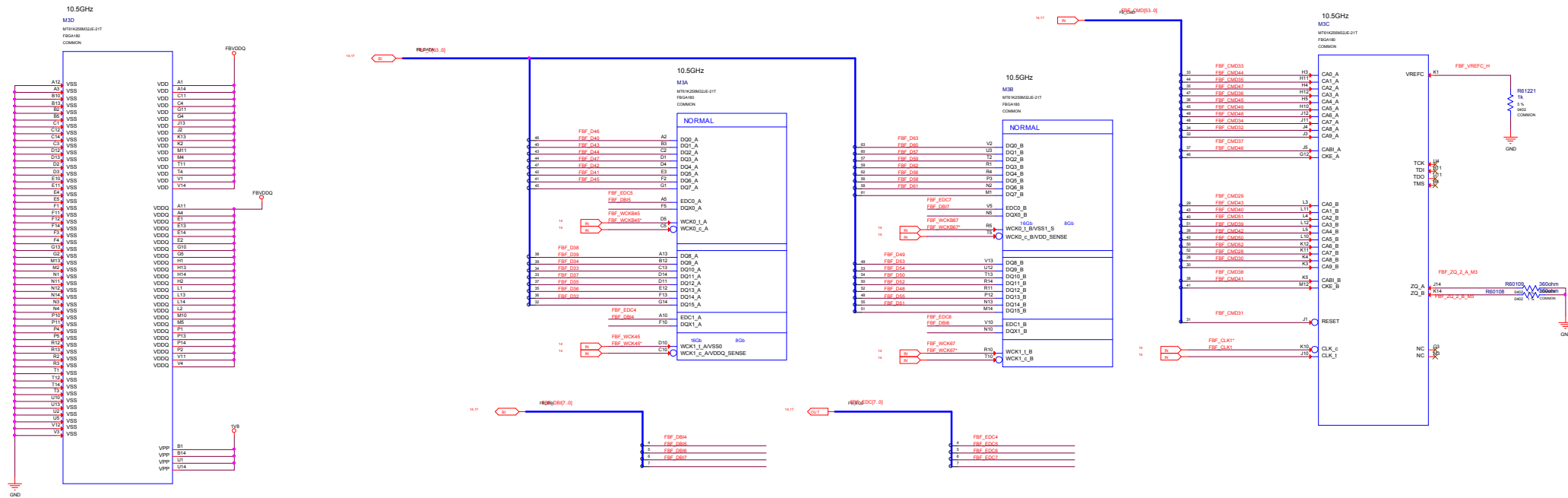
MEMORY: FBE Partition 63..32



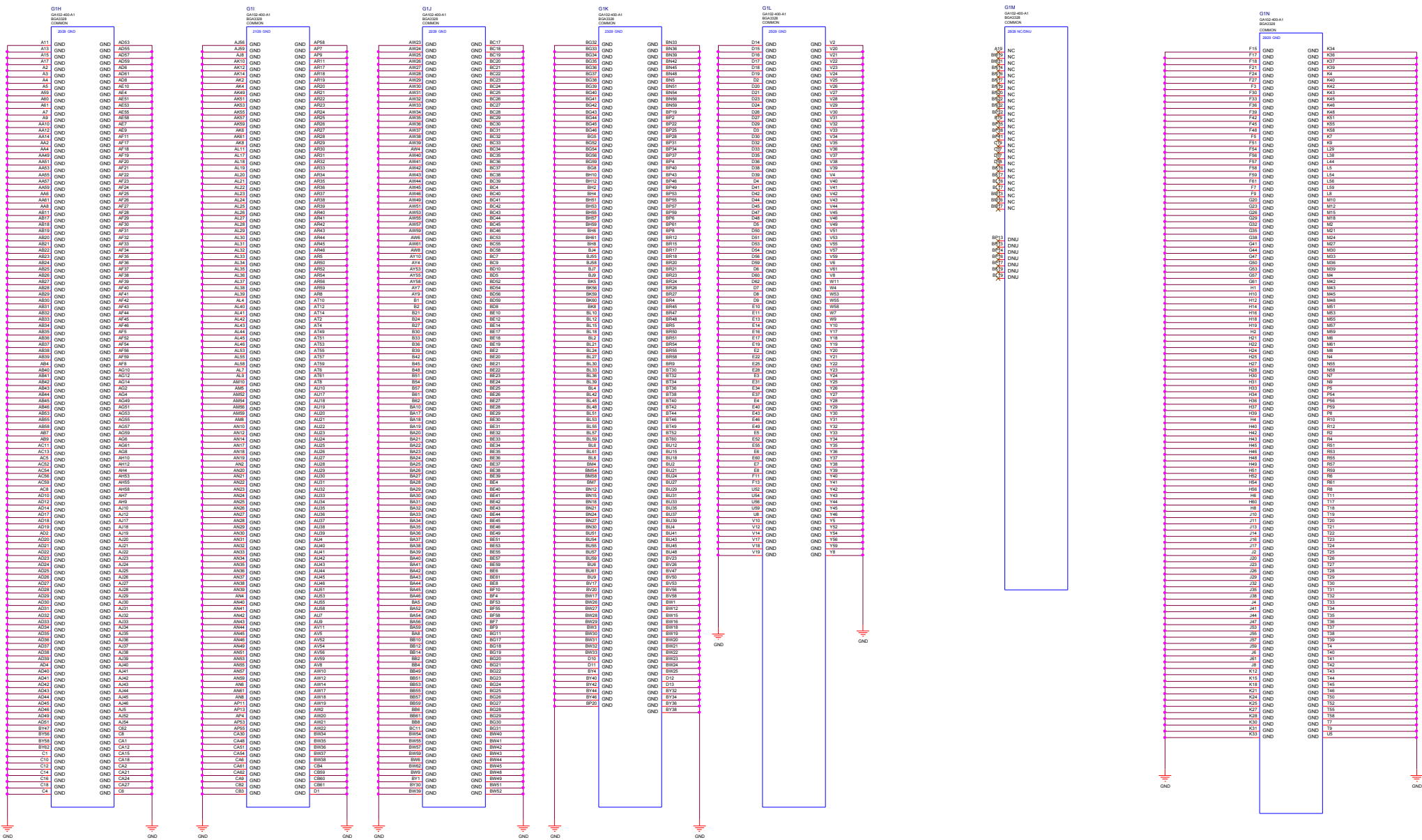
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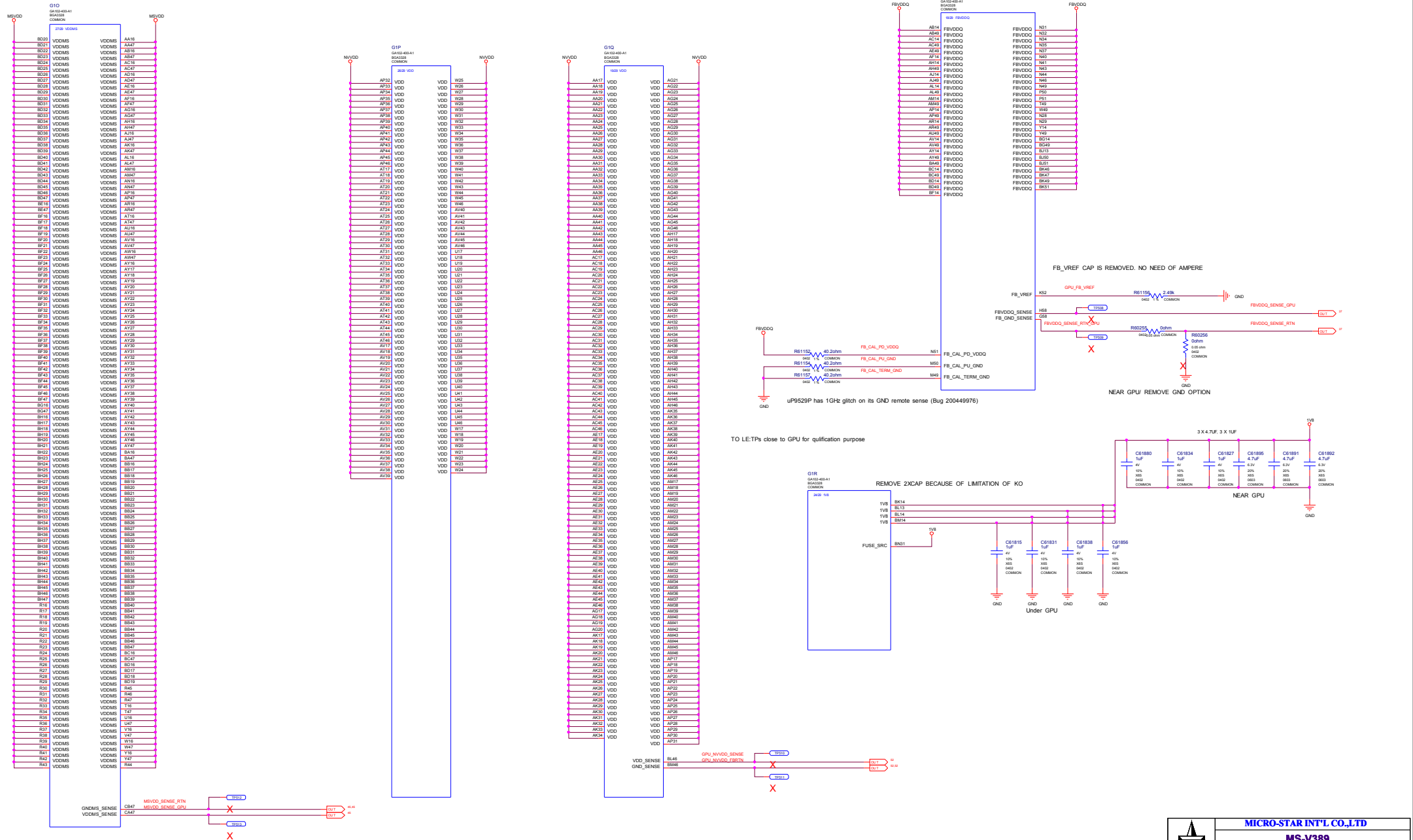
MEMORY: FBF Partition 63..32



GPU GND, RFUs & RSVD

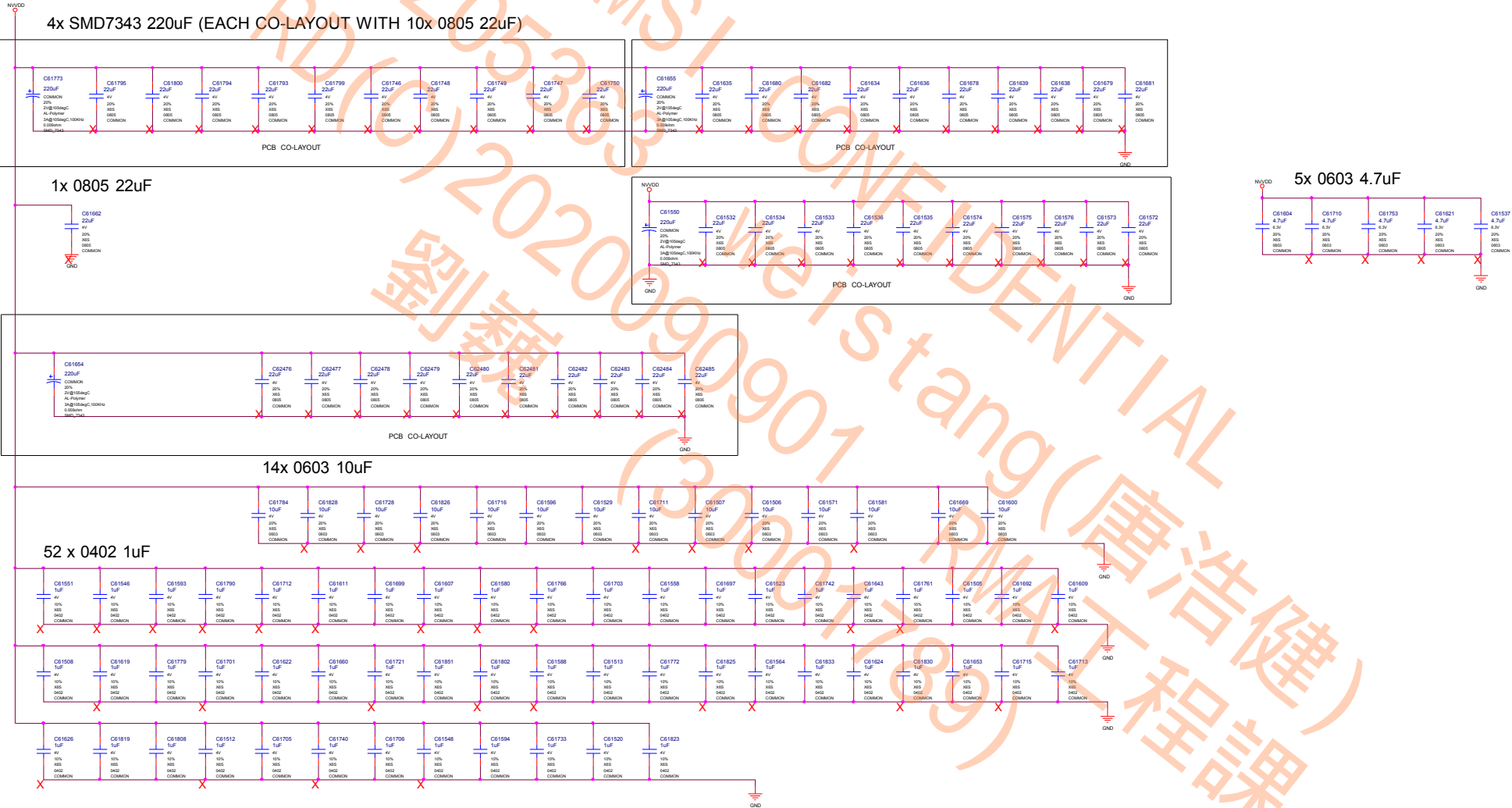


GPU PWR and GND

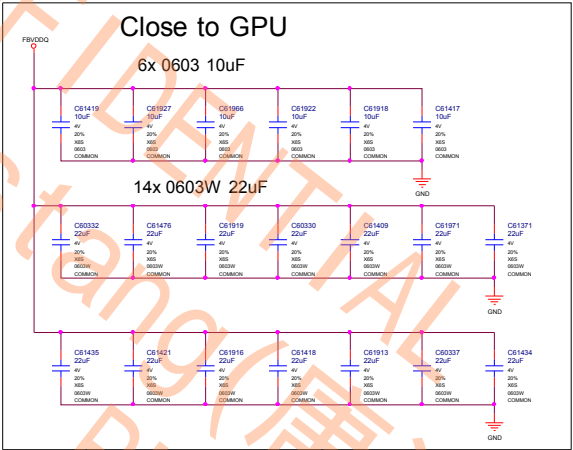


NVVDD

UNDER GPU

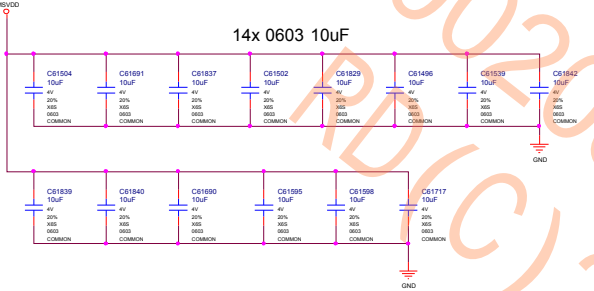


FBVDDQ

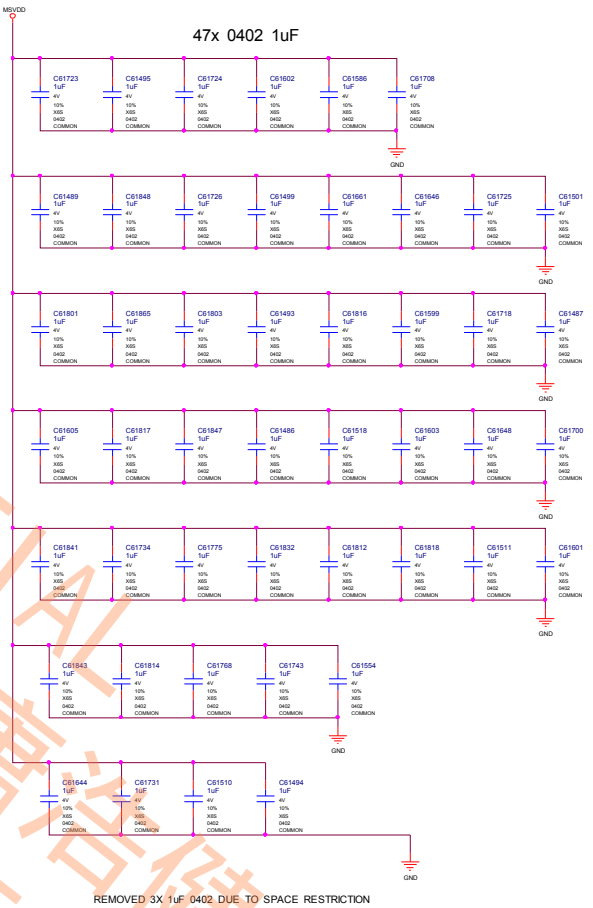
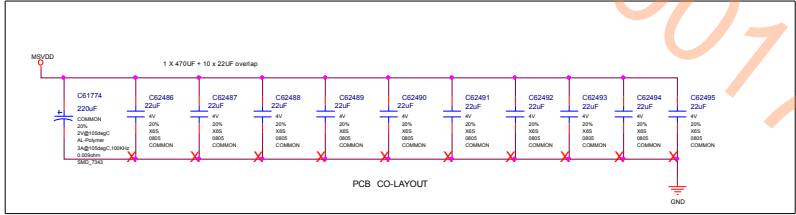
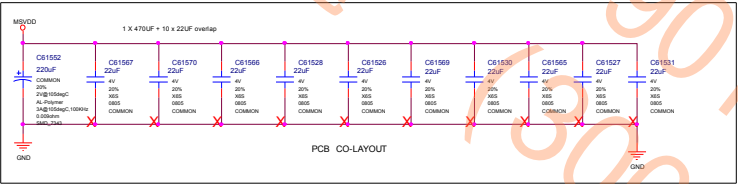


UNDER GPU

MSVDD



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

MSI CONFIDENTIAL
00205363
RD(C)2020090901
Weistang (唐浩健)
RMA工程課
(30001789)

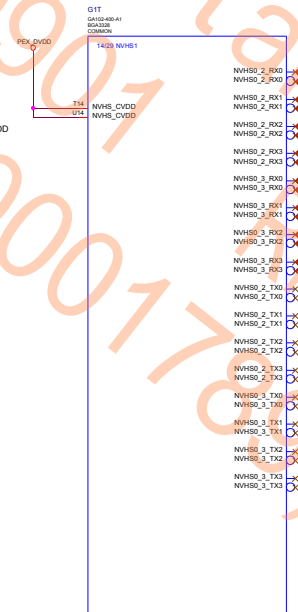
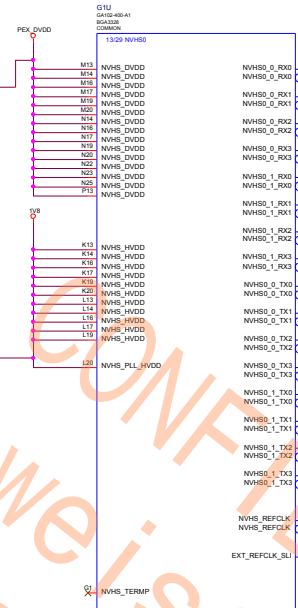
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The diagram illustrates the power distribution of the GPU, divided into two main sections: NEAR GPU and UNDER GPU. Each section contains a series of capacitors with their values and ESRs. Red 'X' marks indicate common ground connections for each capacitor.

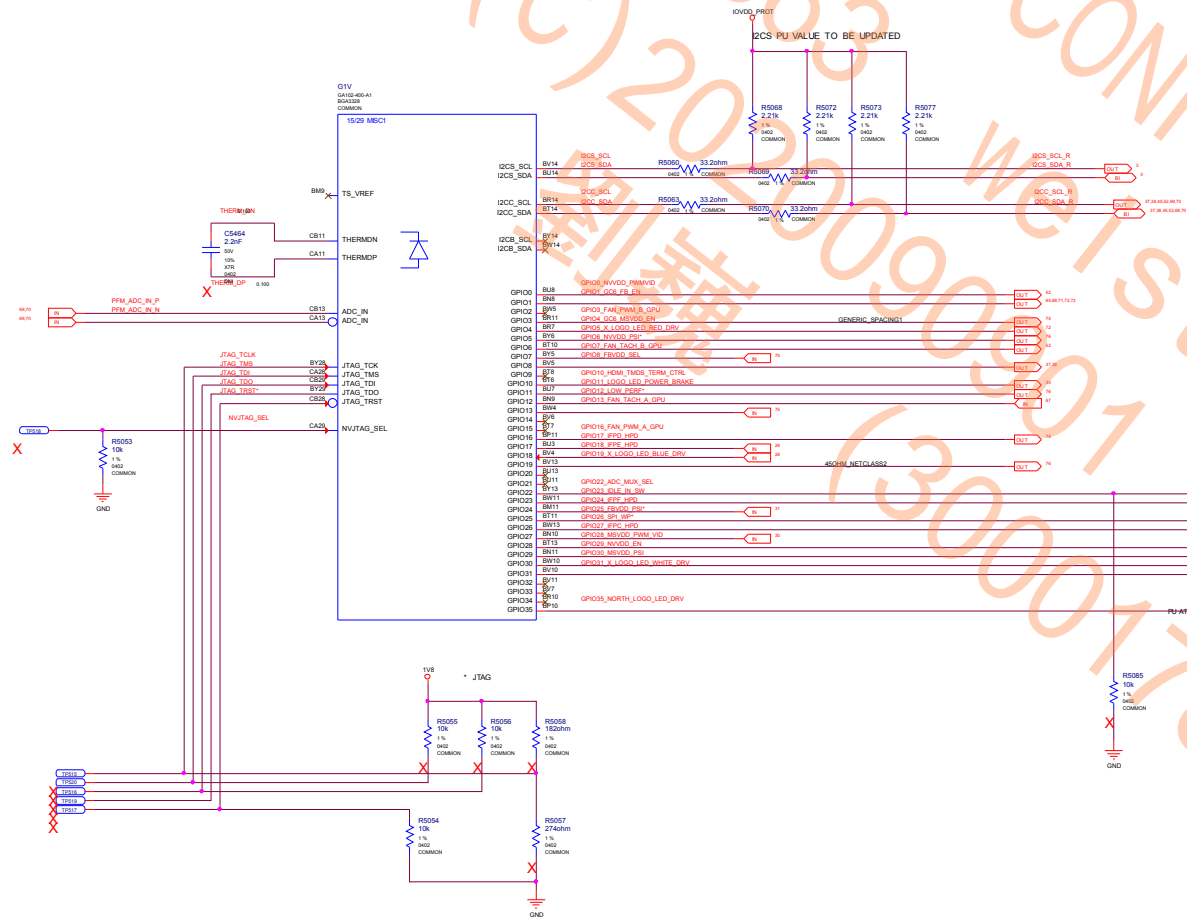
Section	Capacitor Value	ESR	Common Ground
NEAR GPU	C60169 22uF	4.37	COMMON
	C60092 22uF	4.37	COMMON
	C60160 10uF	10%	COMMON
	C60173 10uF	10%	COMMON
	C60175 10uF	10%	COMMON
UNDER GPU	C61797 4.7uF	4.37	COMMON
	C61798 4.7uF	4.37	COMMON
	C61763 4.7uF	4.37	COMMON
	C61876 1uF	10%	COMMON
	C61760 1uF	10%	COMMON
	C61878 1uF	10%	COMMON
	C61732 1uF	10%	COMMON
	C61776 1uF	10%	COMMON
	C61741 1uF	10%	COMMON
	C61777 1uF	10%	COMMON

ID ROM ->YES

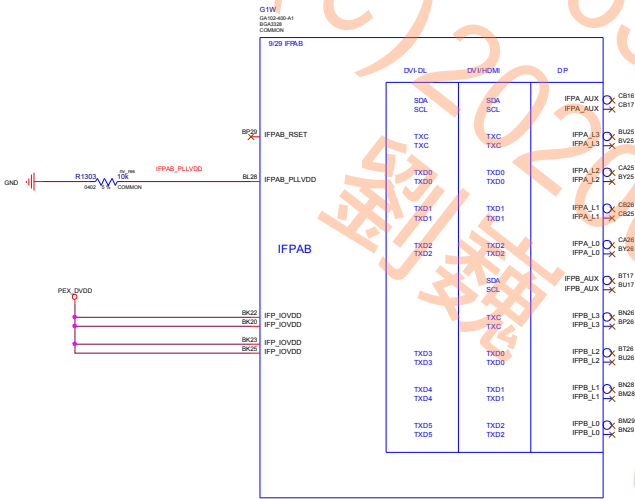
REMOVE ONE BECAUSE OF KO LIMITATION



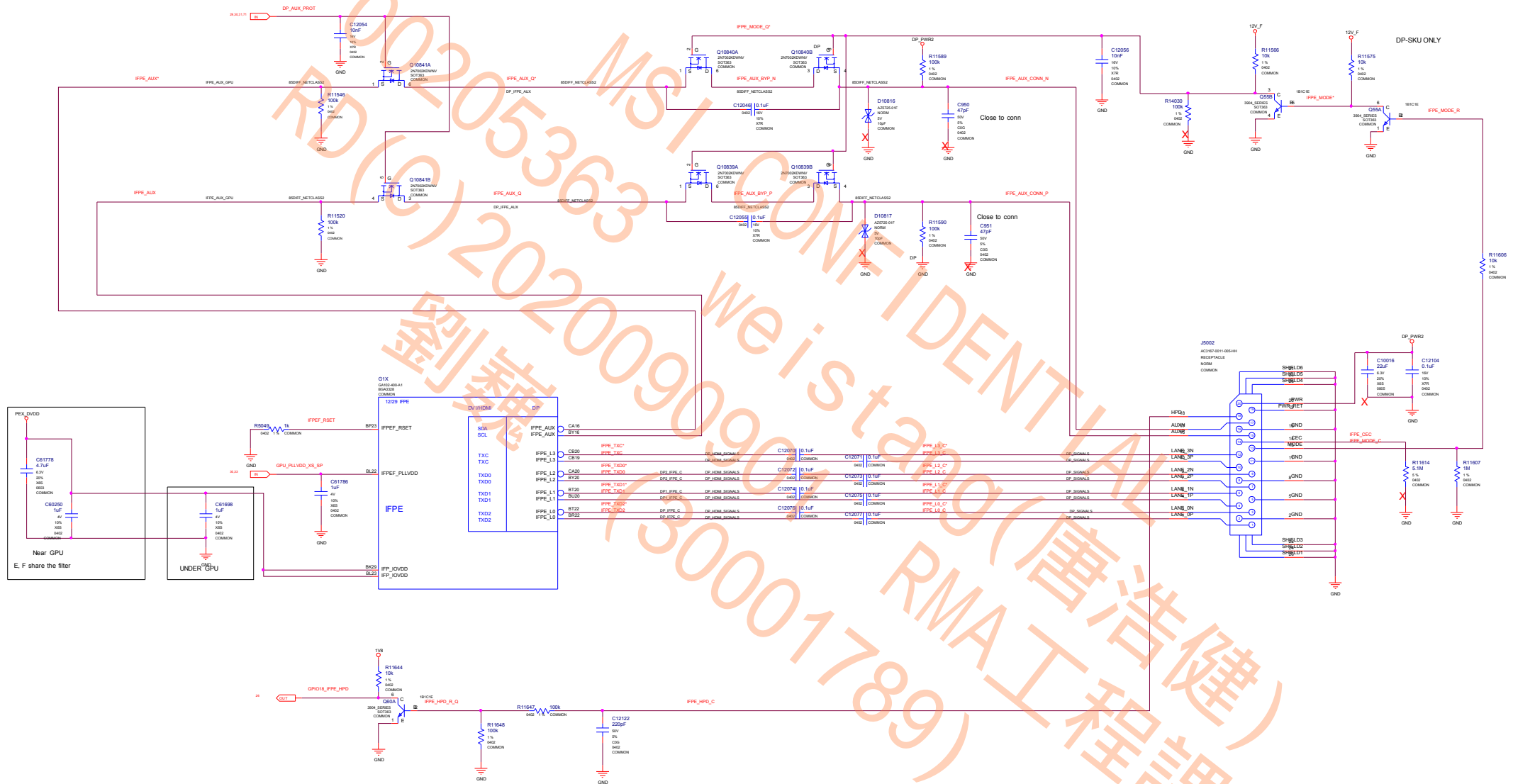
MISC1: Fan, Thermal, JTAG, GPIO, STEREO



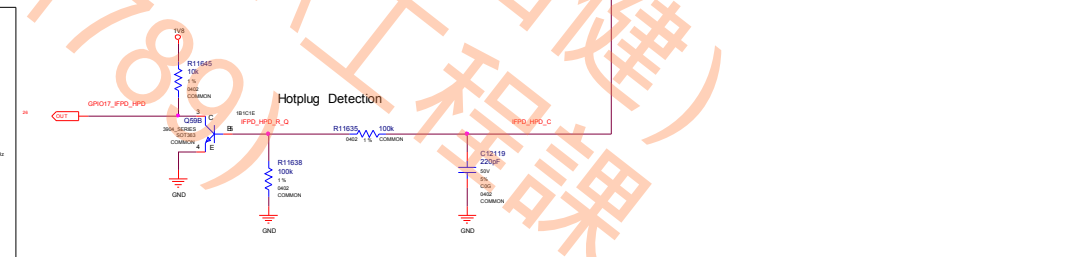
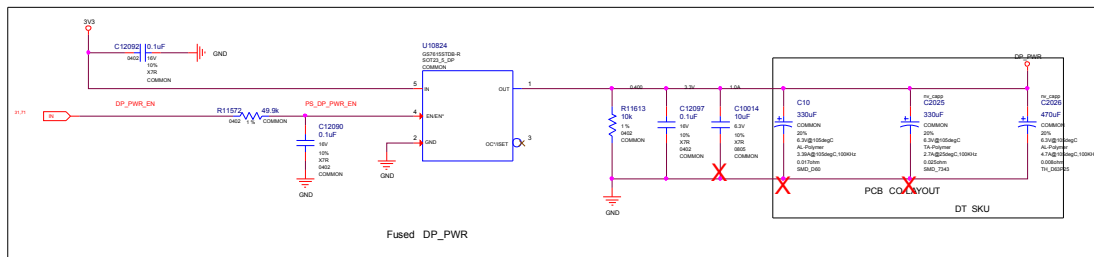
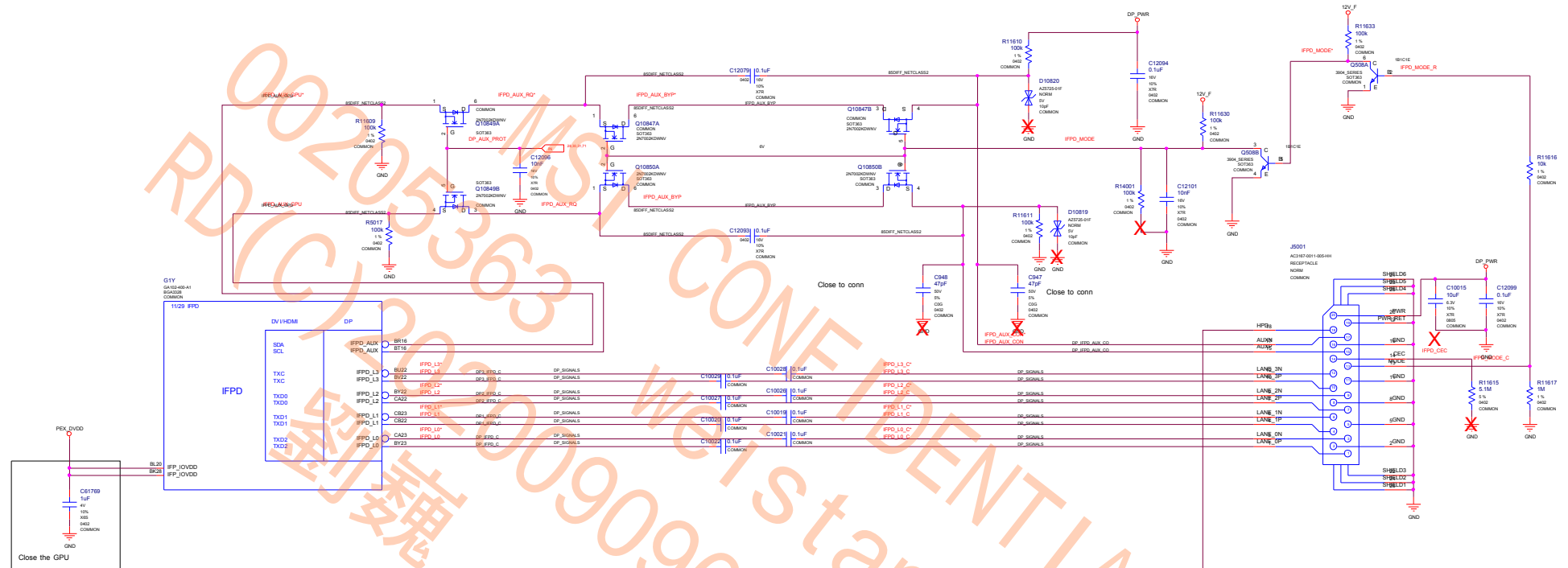
IFPA UNUSED, IFPB UNUSED



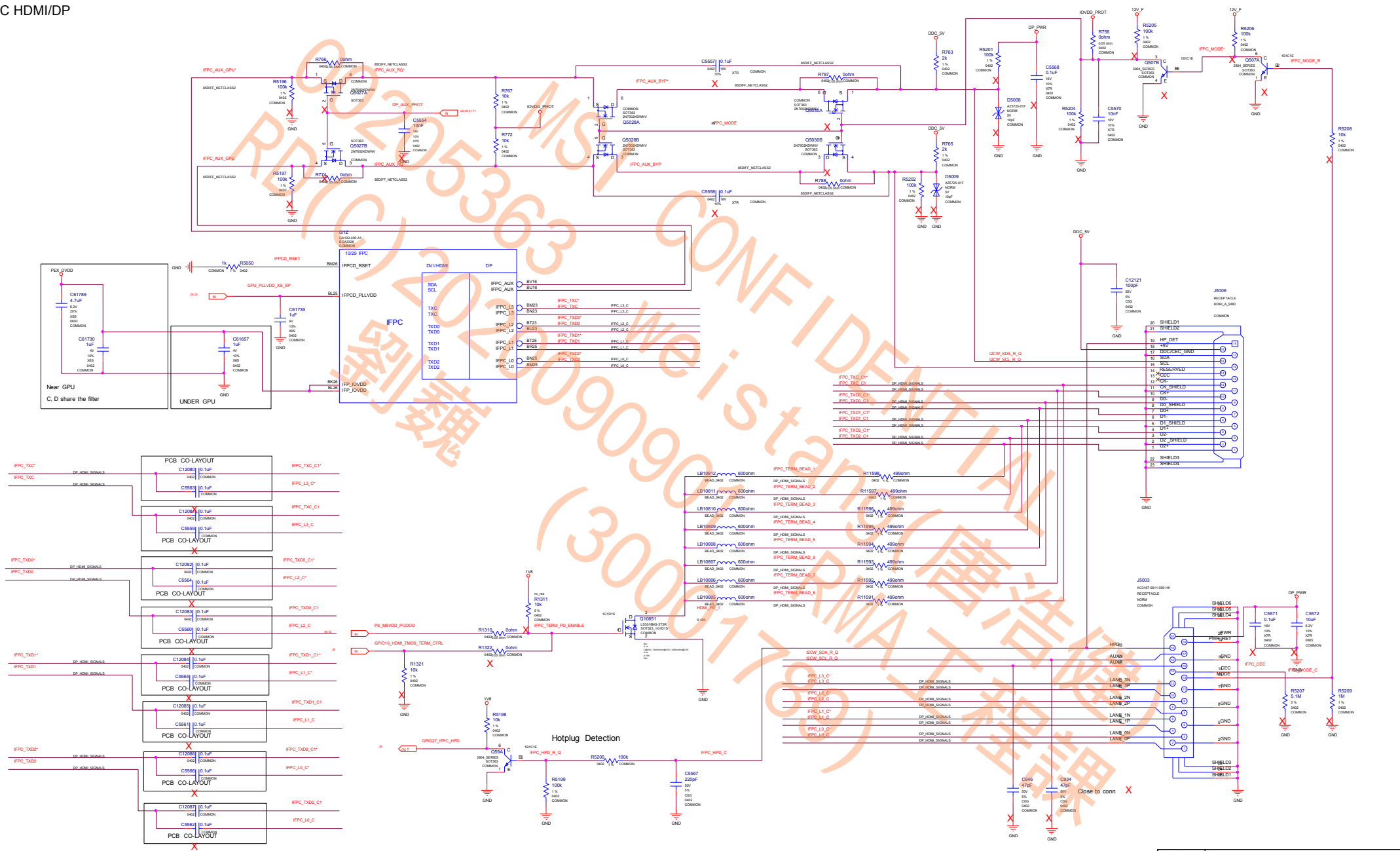
IFPE DP

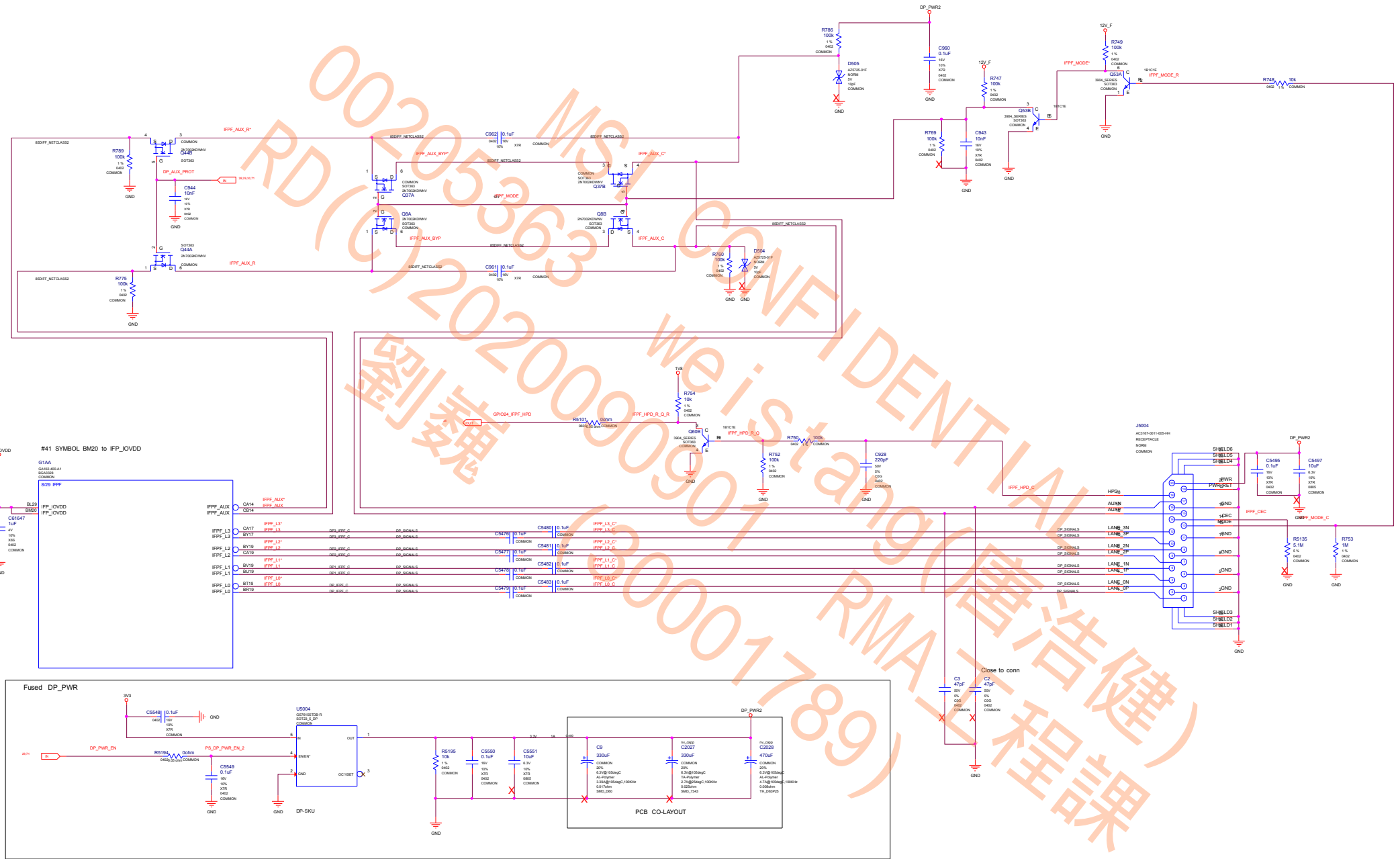


IFPD DP



IFPC HDMI/DP





MISC: ROM, Straps

GROUP0	STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
	L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
	H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
	H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
	L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
	L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
	L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE	DEFAULT
H	H	H	0111	FS_OVERT ENABLE	
L	L	L	0000	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	

Default

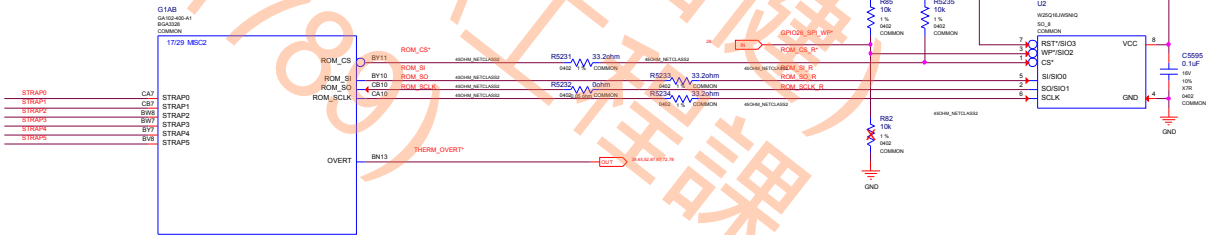
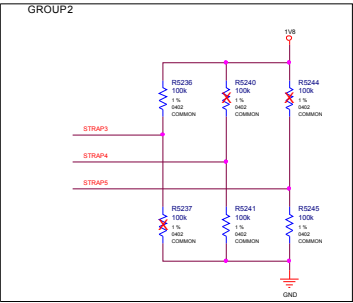
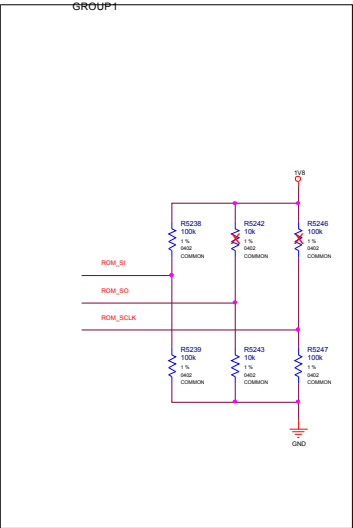
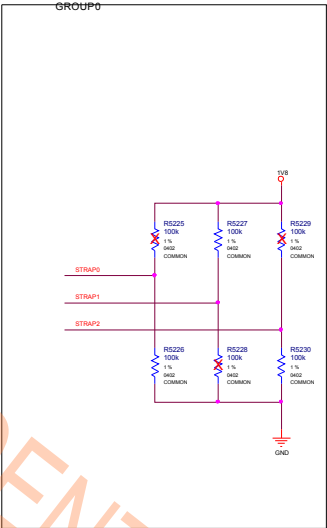
Default

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

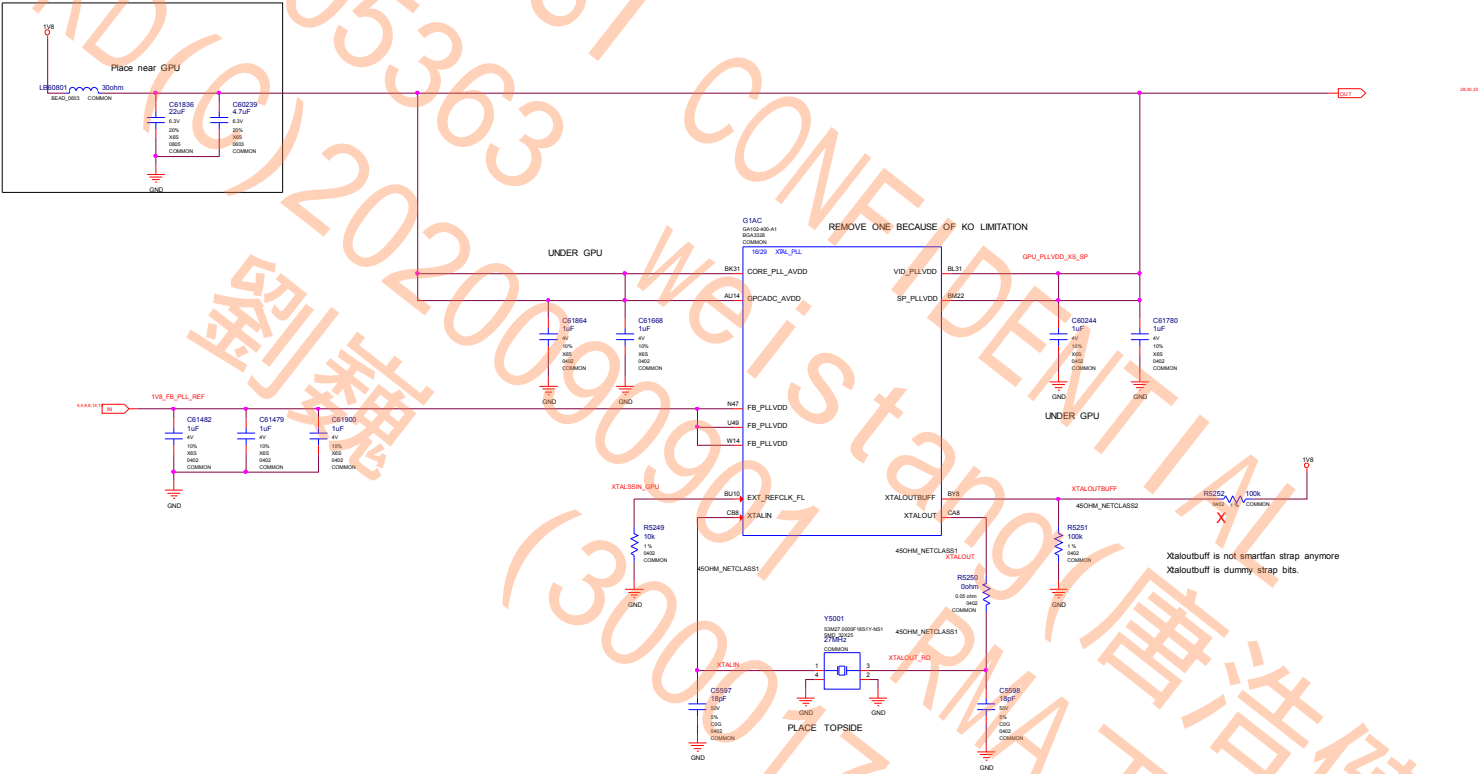
<A01 PCB

<OLD

<LATEST A02 PCB



MISC: XTAL. PLL

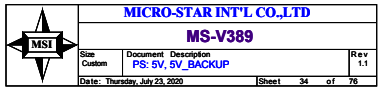


STUFF IF USING MP14040

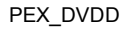
PS_SV_PG00D

34,38,45,52,60,63,71

OUT



PS: PEX_DVDD 1V8 Rail



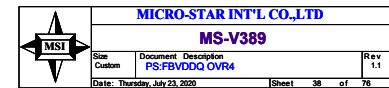
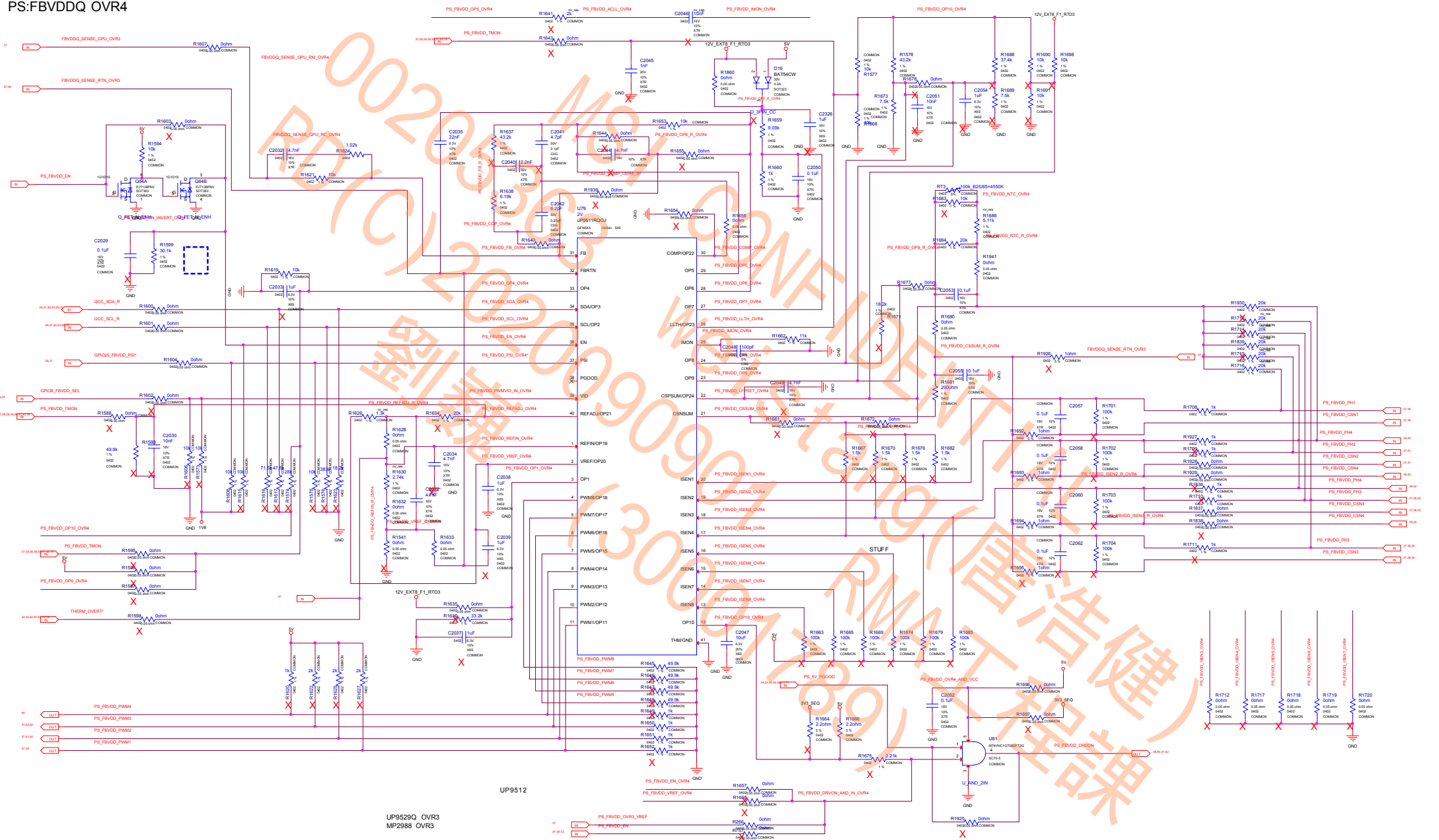
00205363
RD(C)2020-0901
MSI CONFIDENTIAL
Weistang (唐浩健)
RMA工程課
(30001789)

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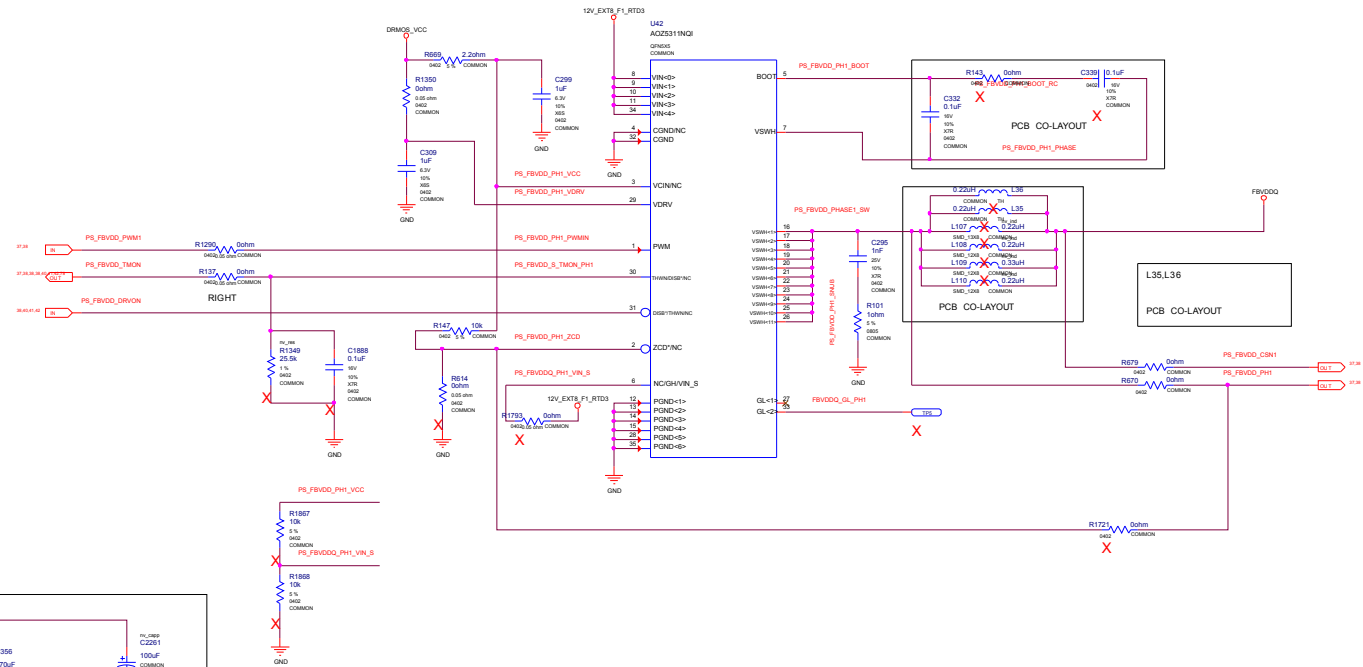
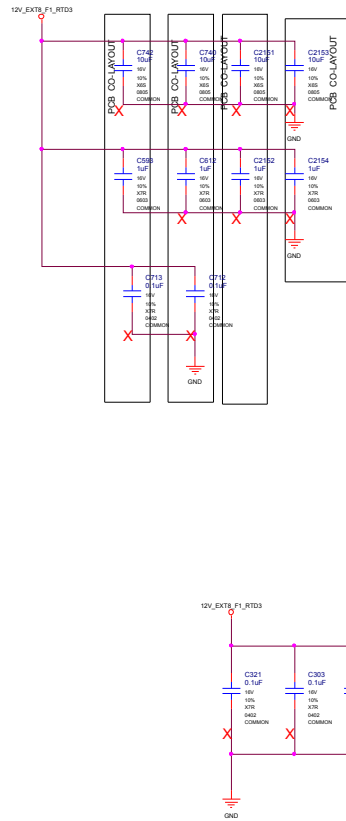
PIN12 MP2988 VIN SENSE 1/16 DIVIDER
PIN12 UP9529 REFOUT



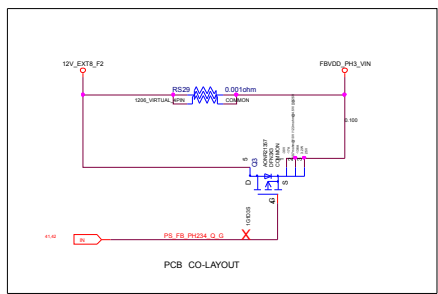
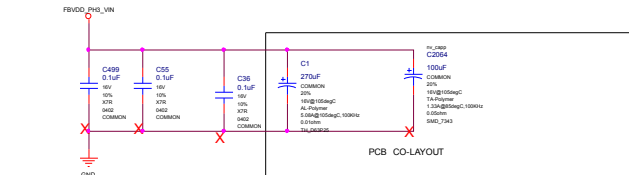
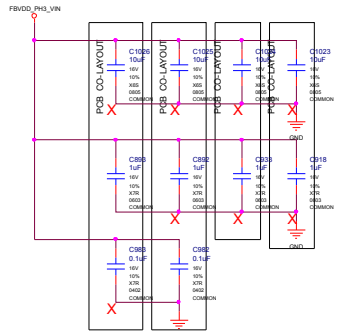
PS:FBVDDQ OVR4



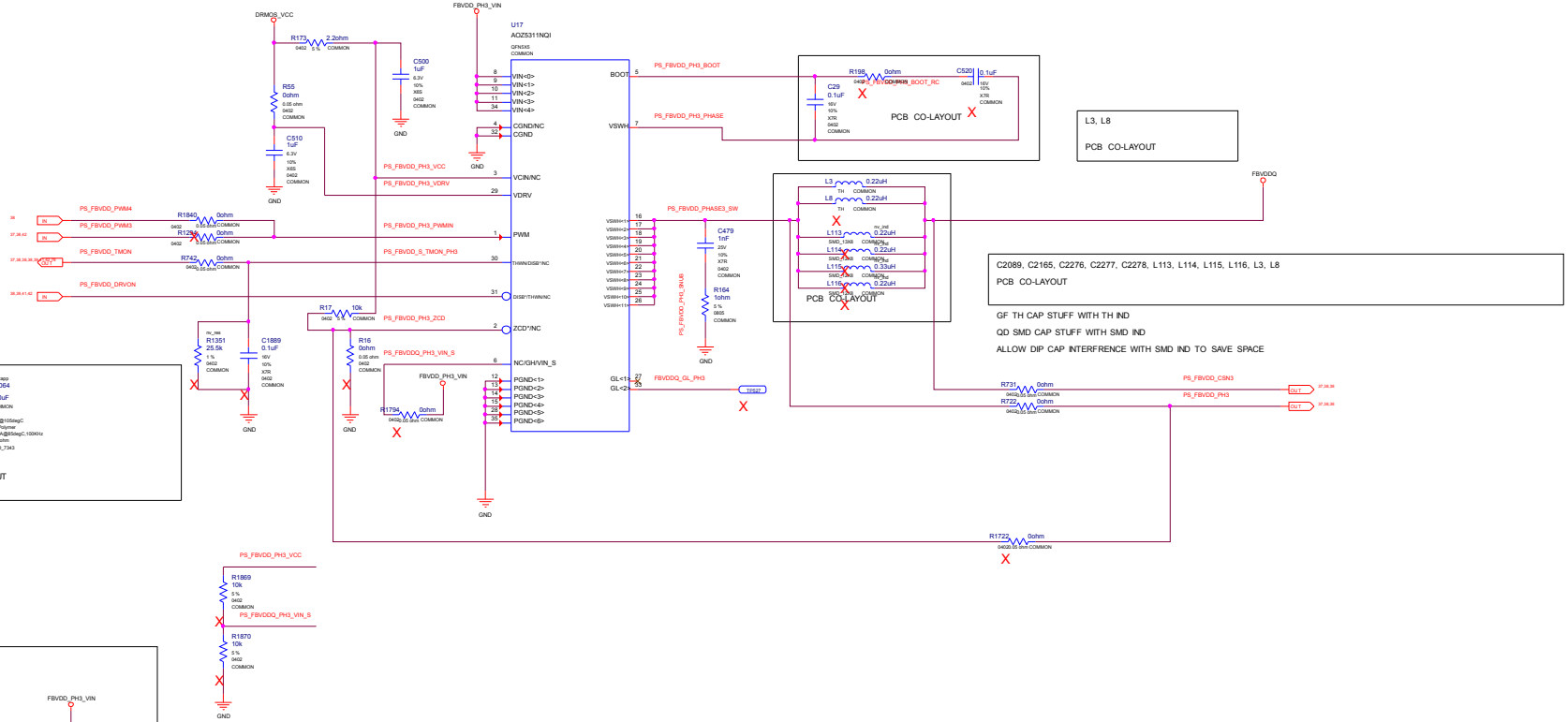
PS: FBVDD PH1



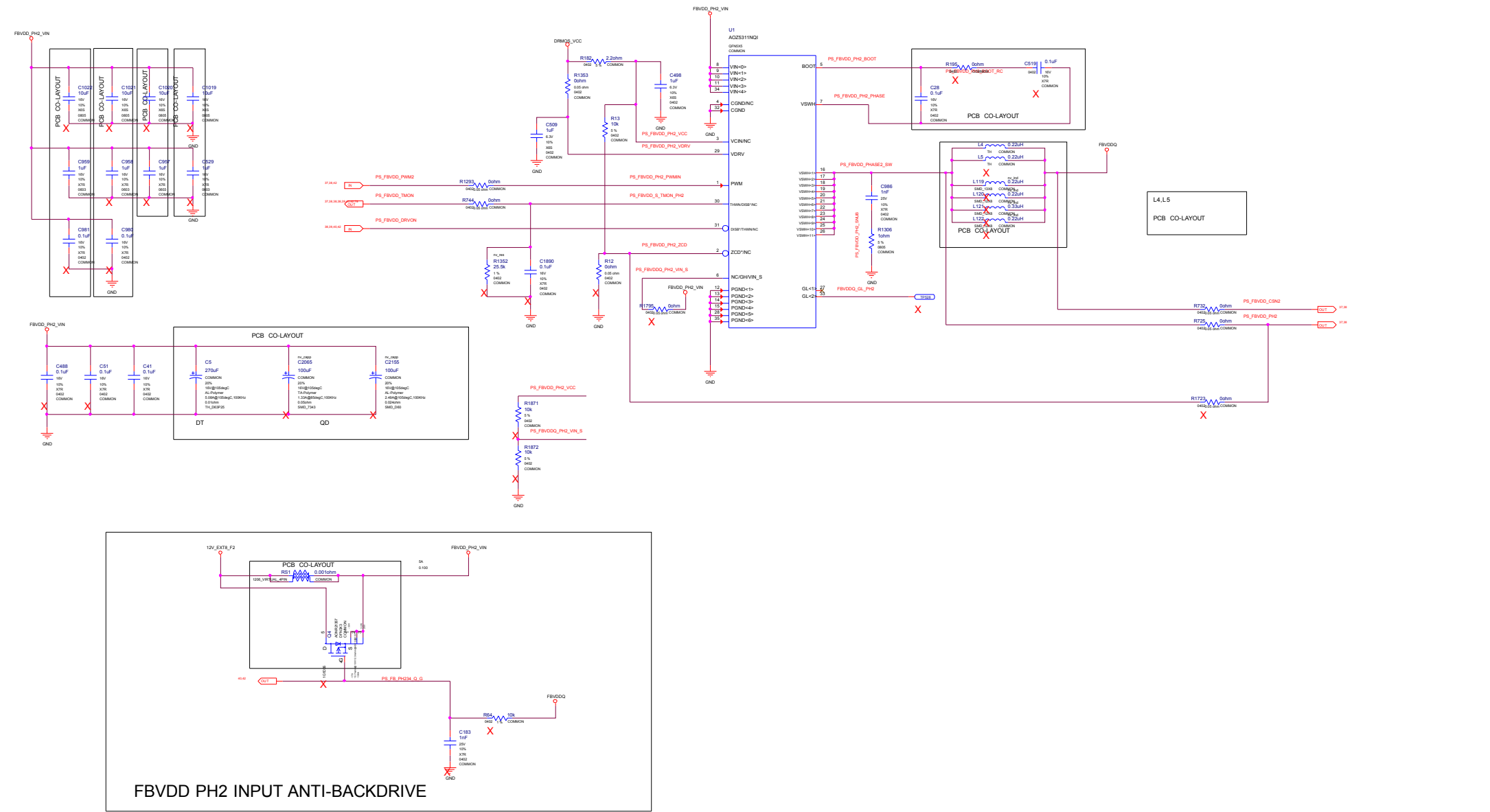
PS: FBVDD PH3



FBVDD PH3 INPUT ANTI-BACKDRIVE

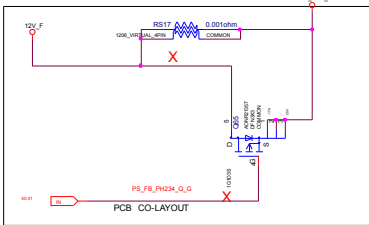
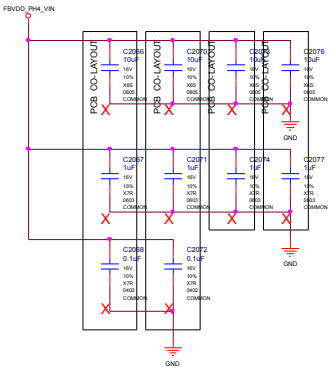


PS: FBVDD PH2

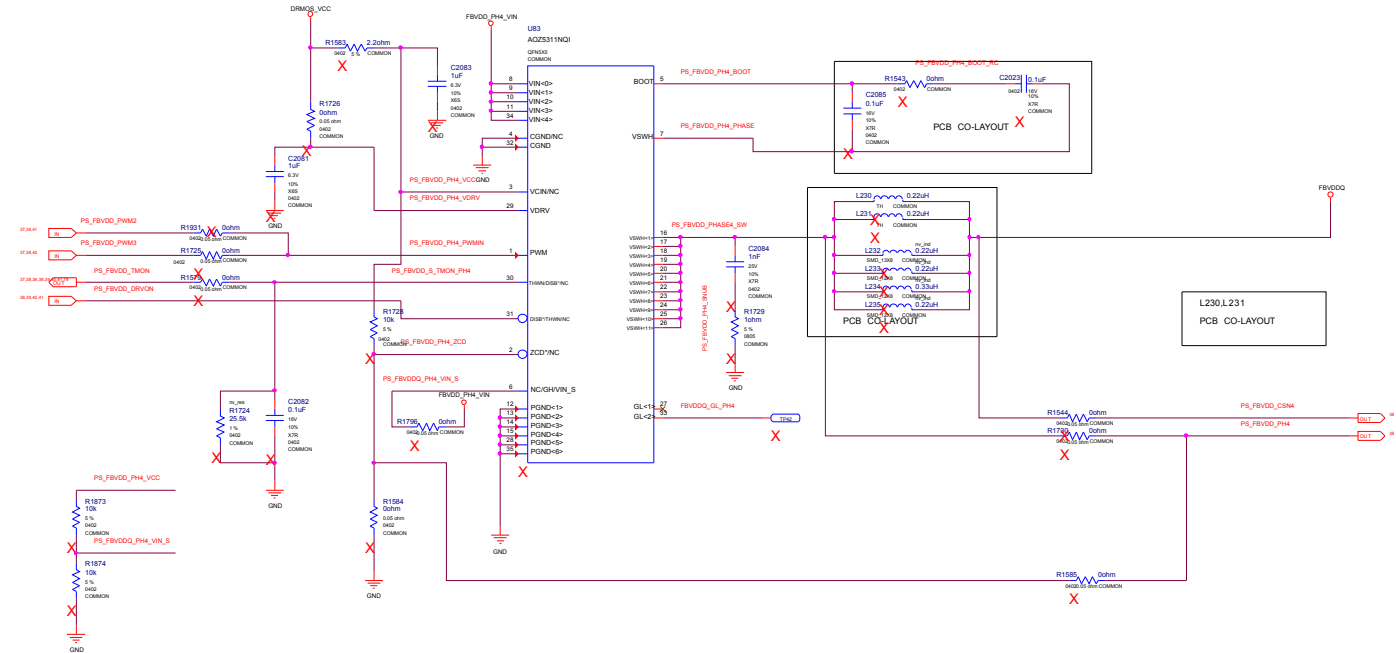
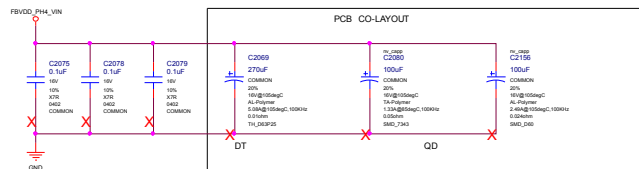


FBVDD PH2 INPUT ANTI-BACKDRIVE

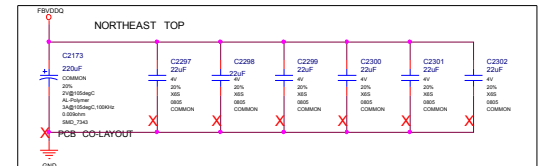
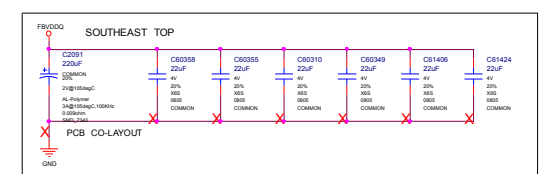
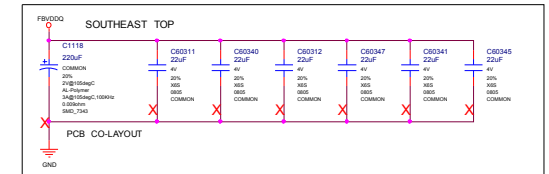
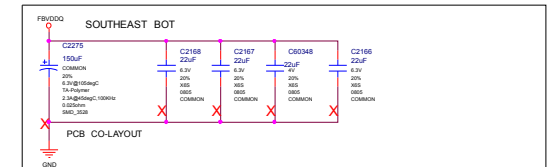
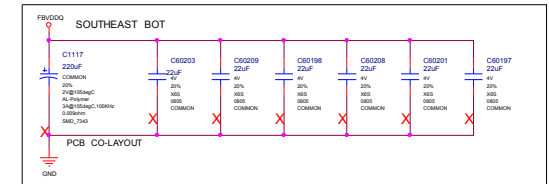
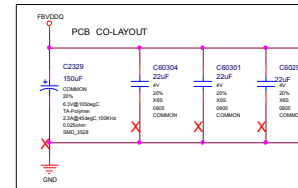
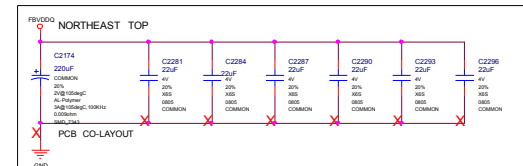
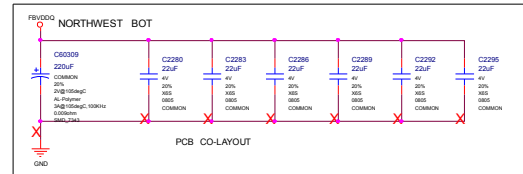
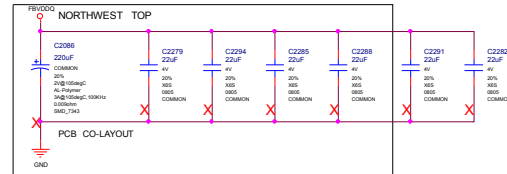
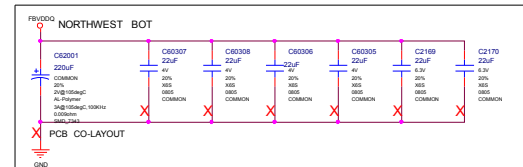
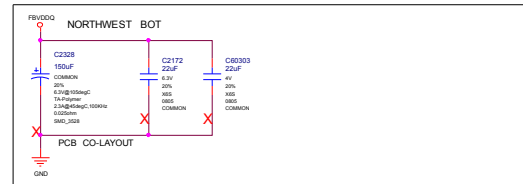
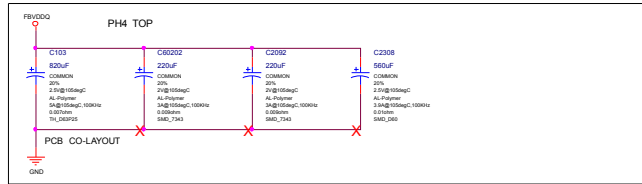
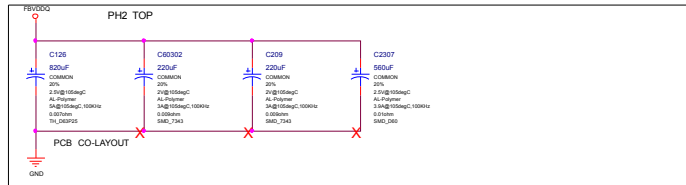
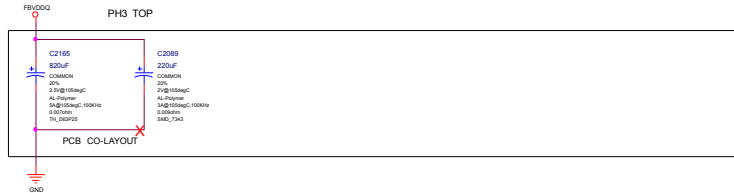
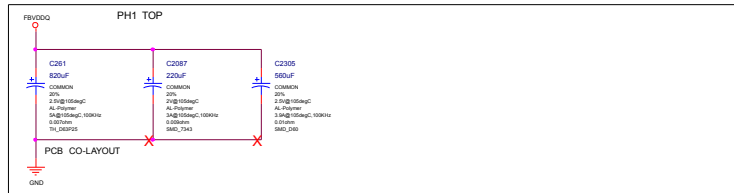
PS: FBVDD PH4



FBVDD PH3 INPUT ANTI-BACKDRIVE



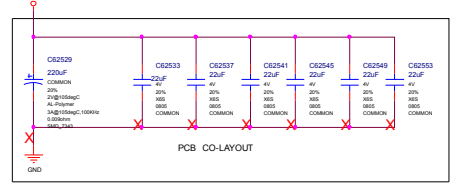
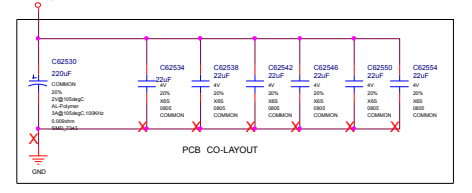
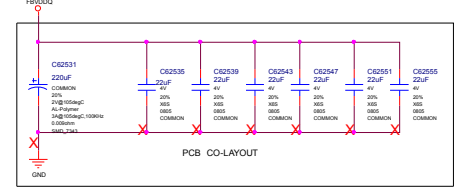
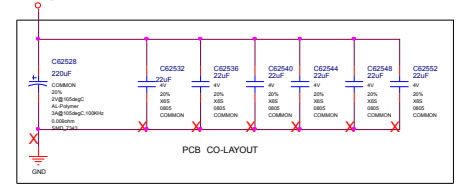
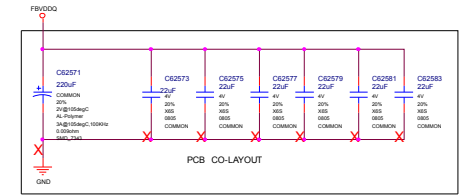
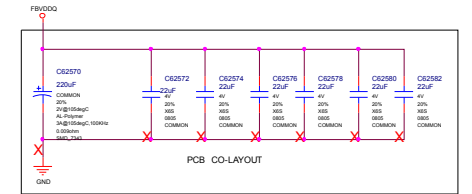
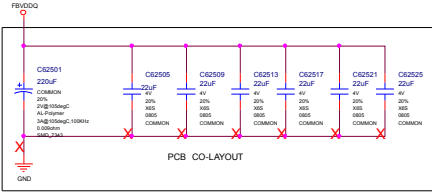
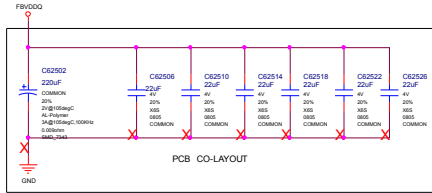
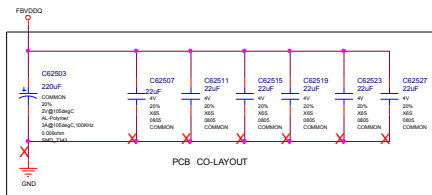
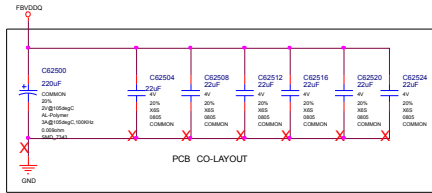
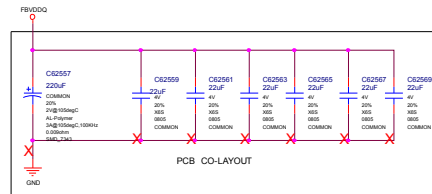
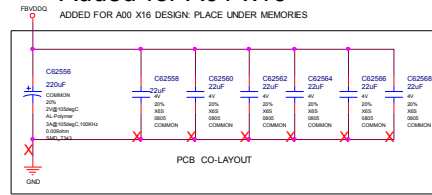
3x 820uF TH FBVDD OUTPUT BULK CAPS



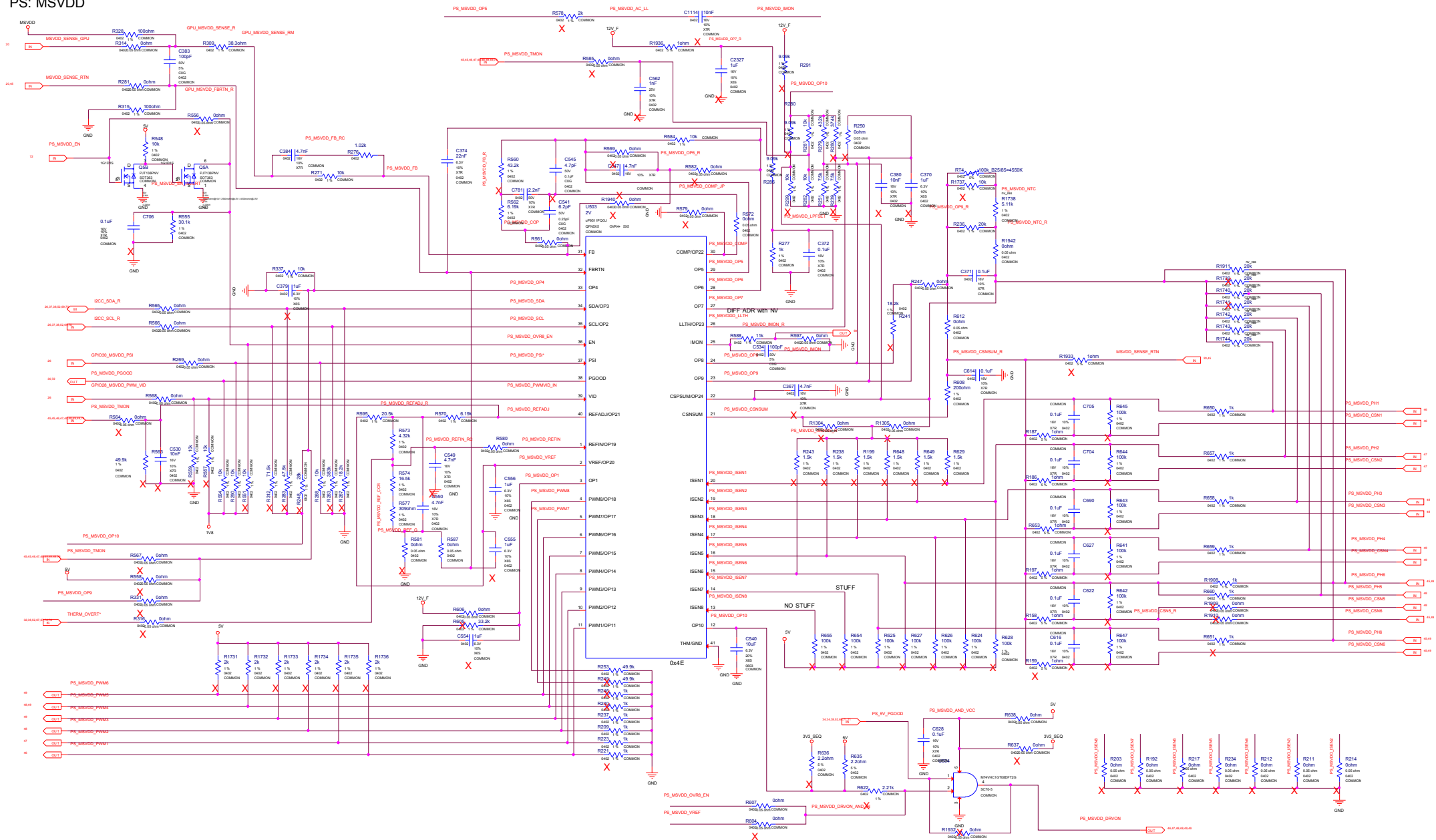
CLOSE TO FB PH3 OUTPUT STUFF

Added for A01 x16

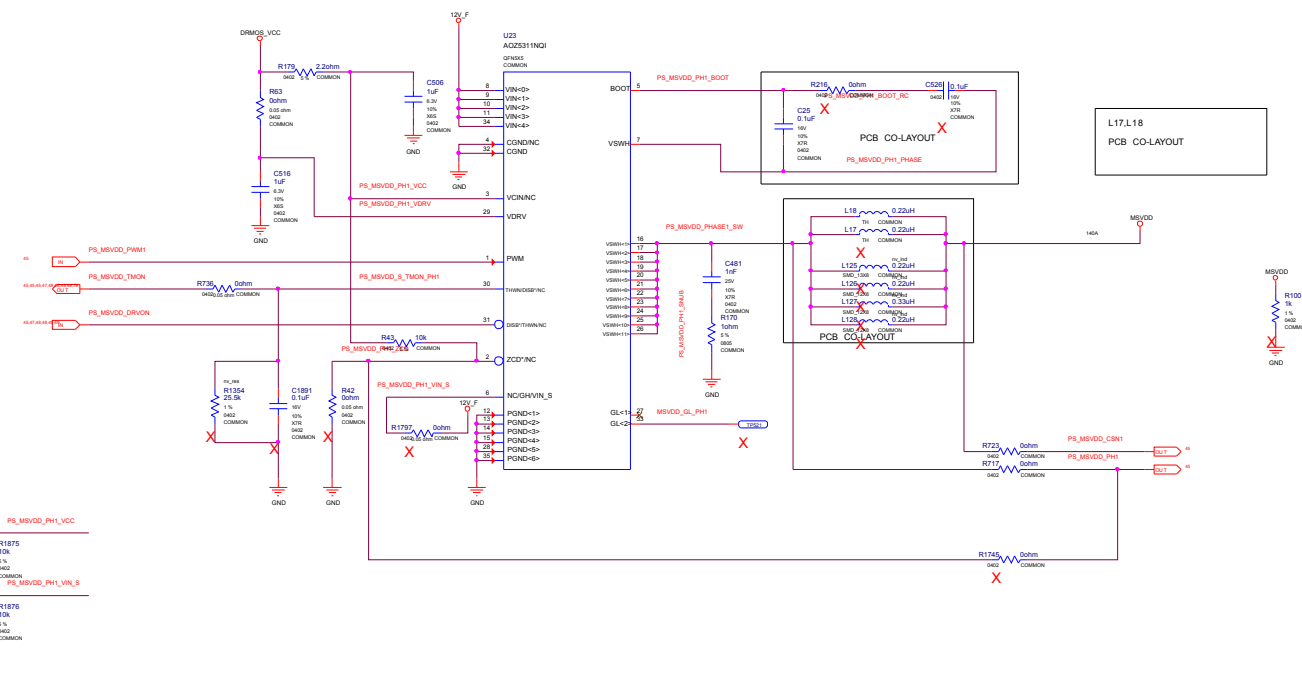
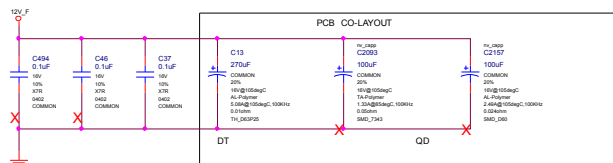
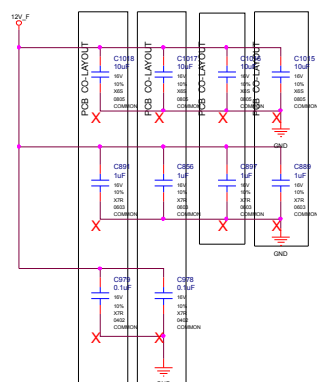
ADDED FOR A00 X16 DESIGN: PLACE UNDER MEMORIES



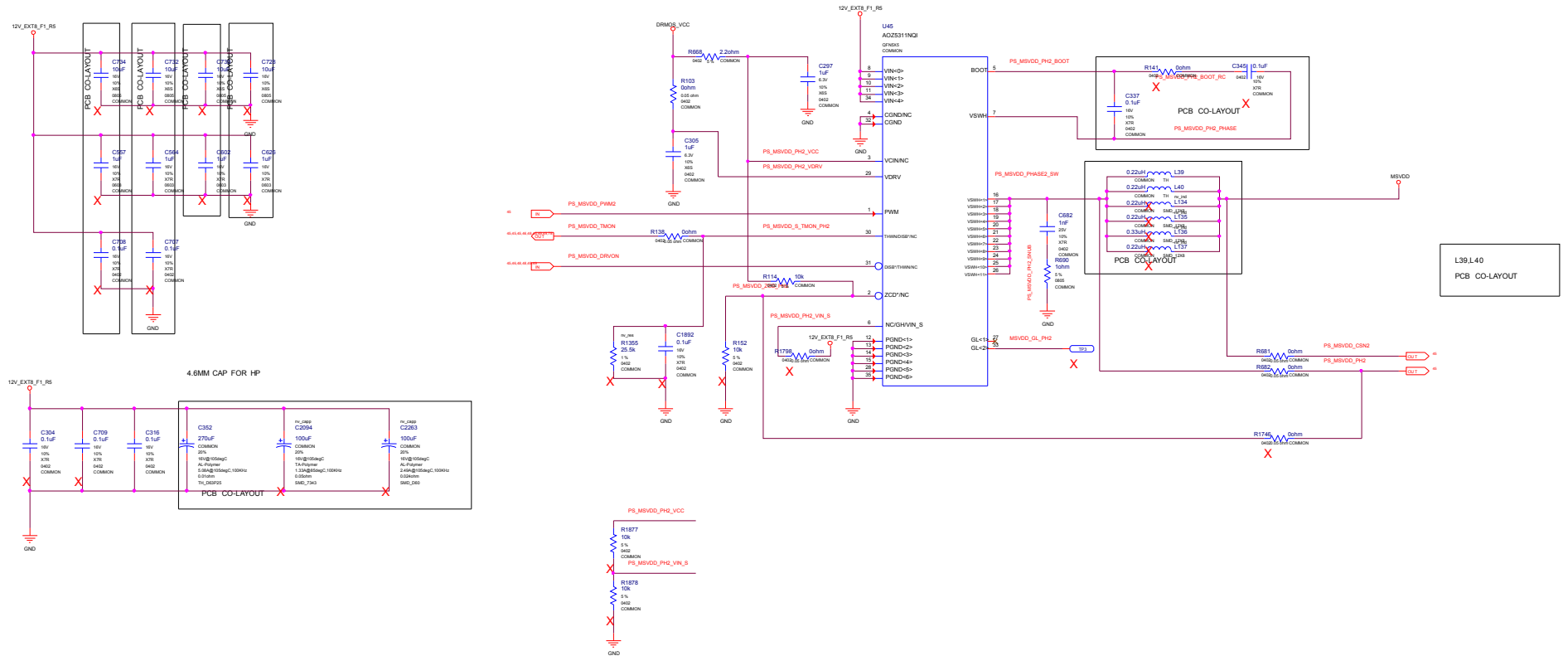
PS: MSVDD



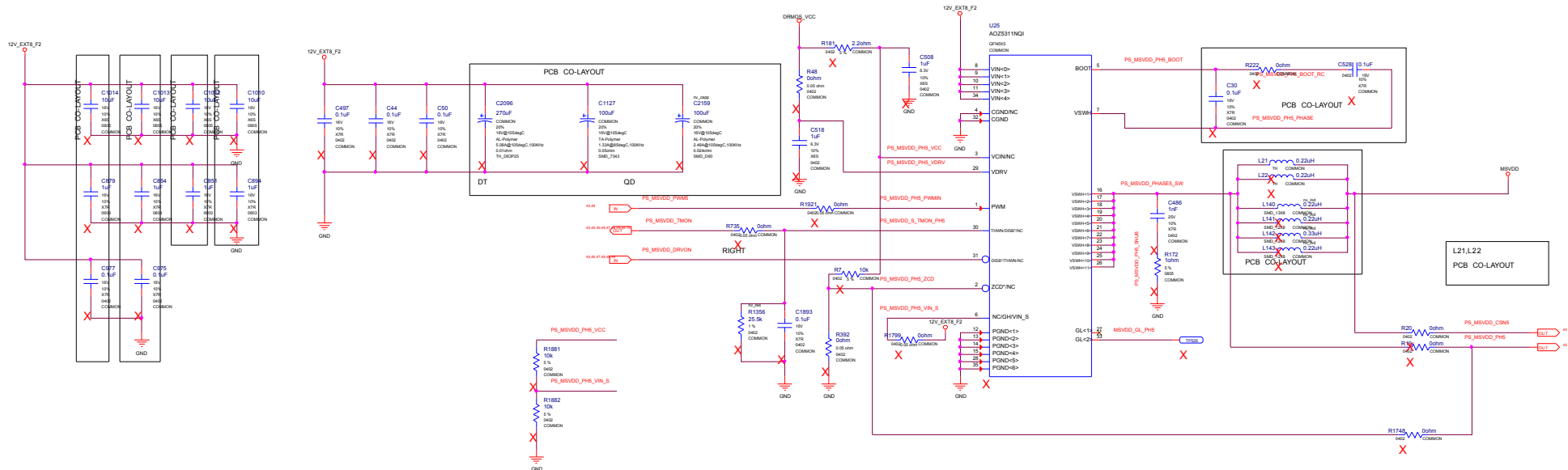
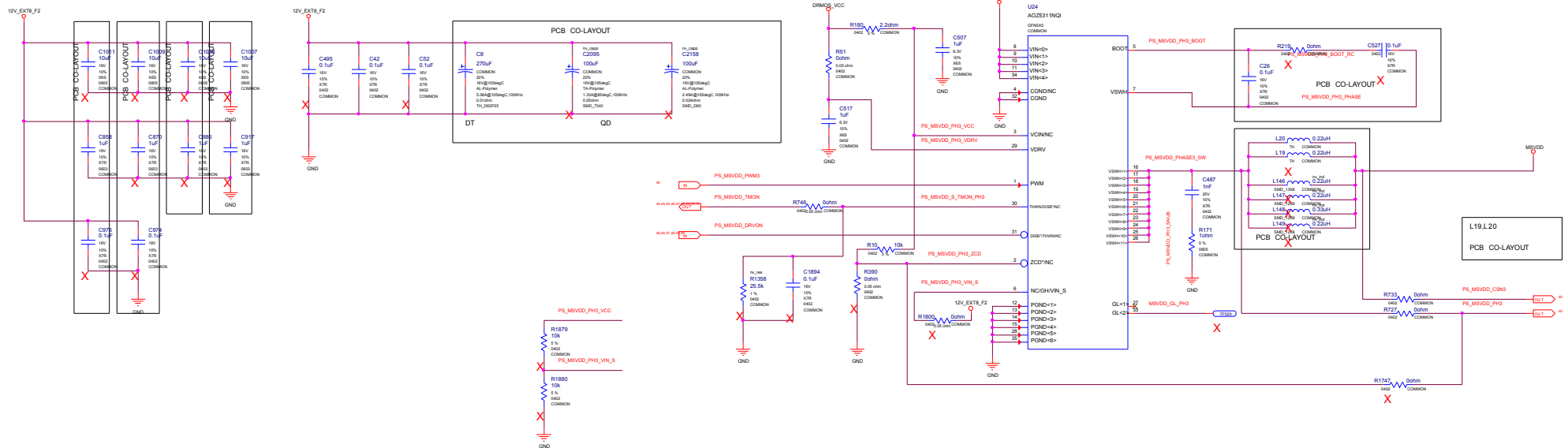
PS: MSVDD Phase 1



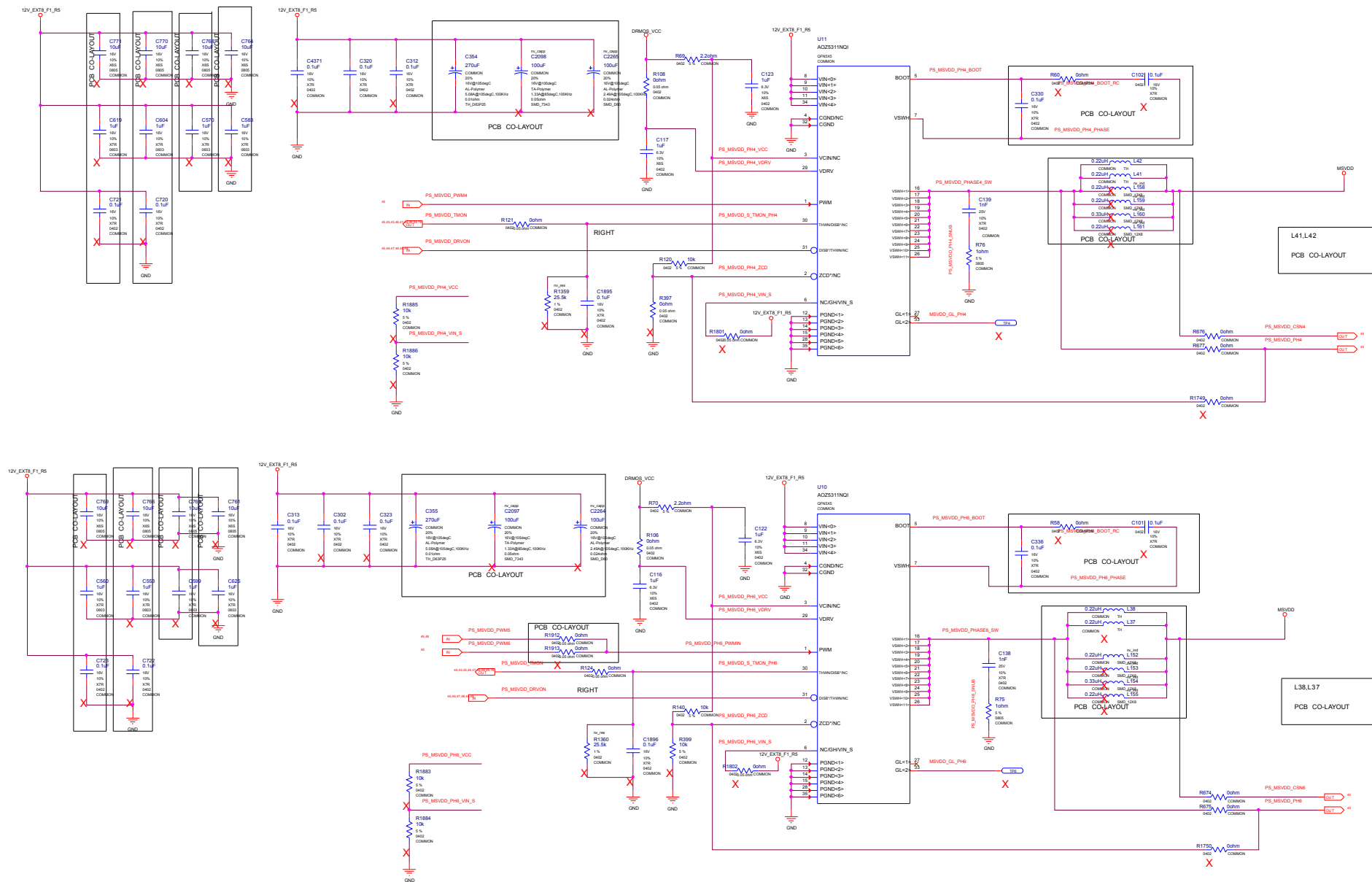
PS: MSVDD PH 2



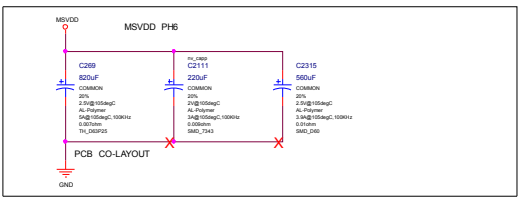
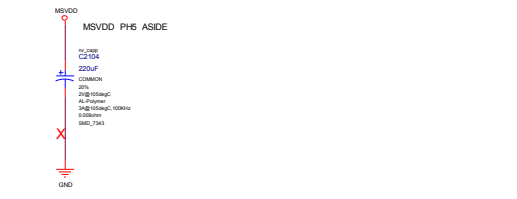
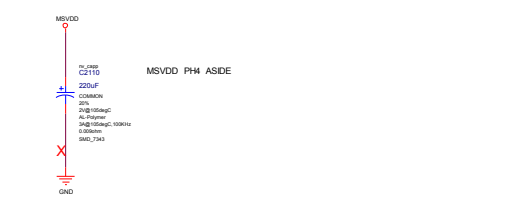
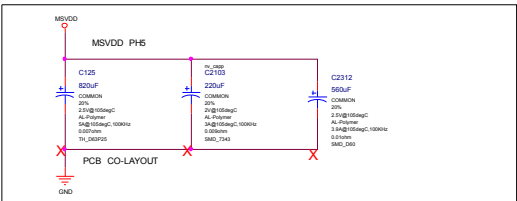
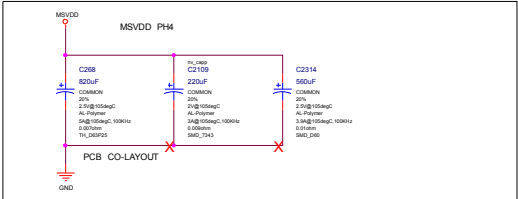
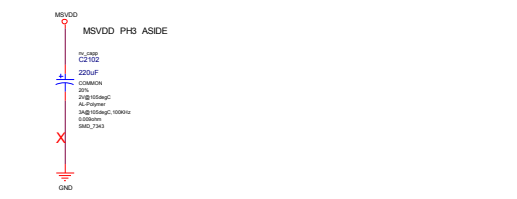
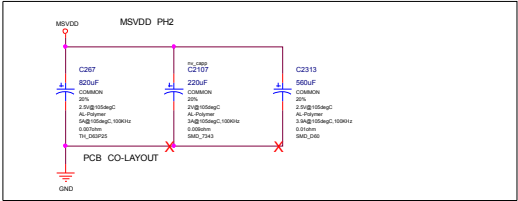
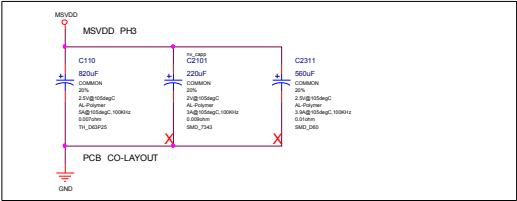
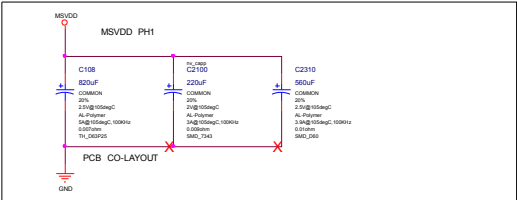
PS:MSVDD Phase 3, 5



PS: MSVDD PH 4,6

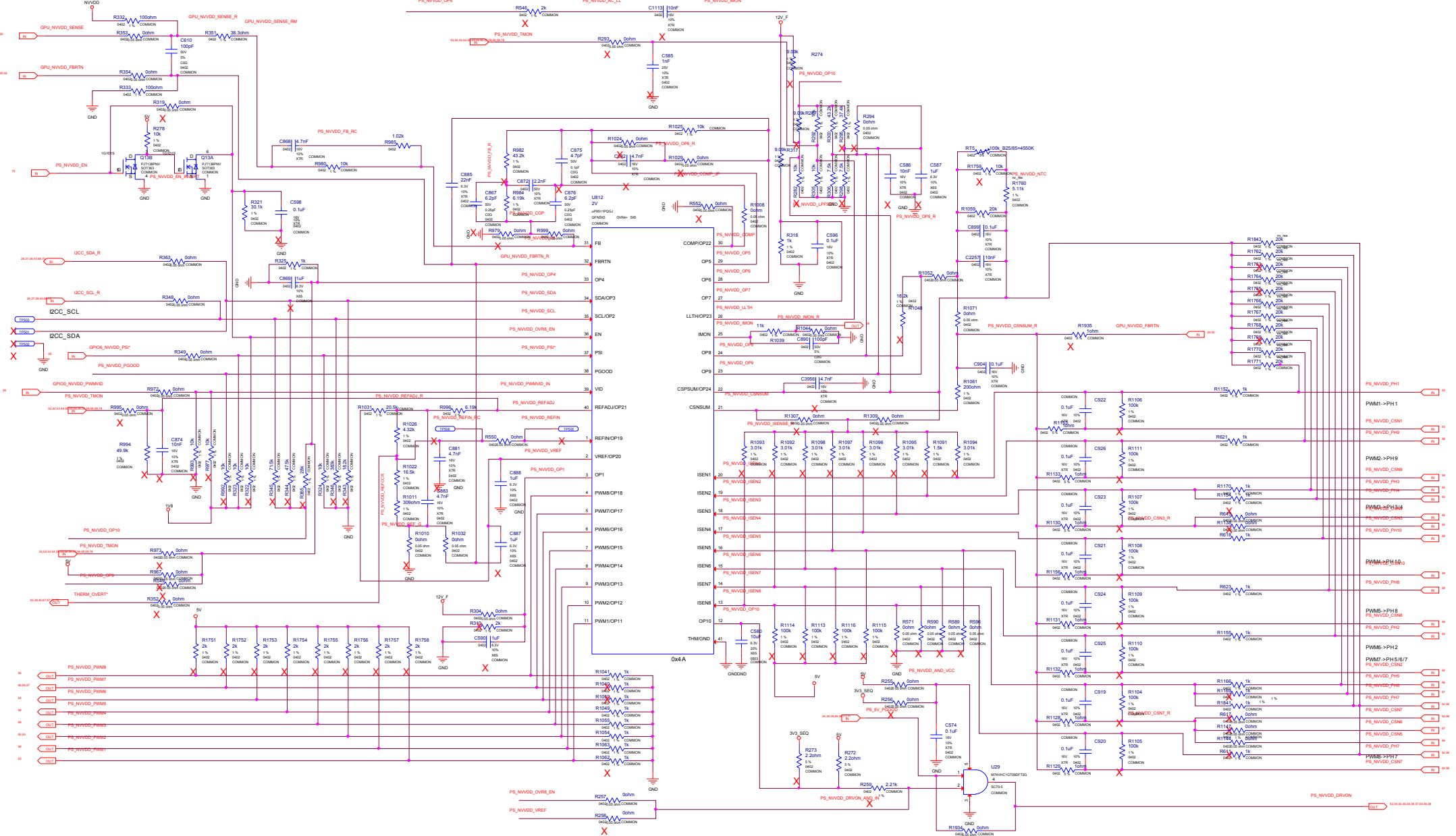


PS:MSVDD OUTPUT CAP (TOP)



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PS: NVVDD Controller_OVR8

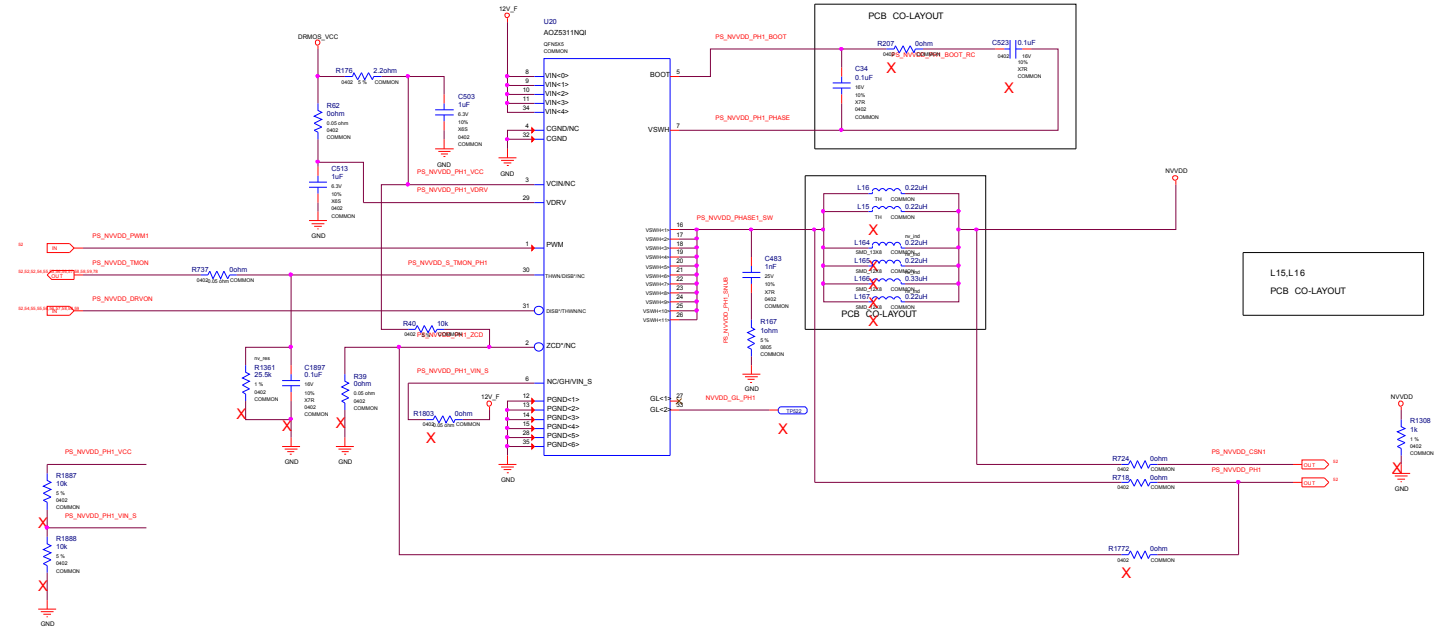
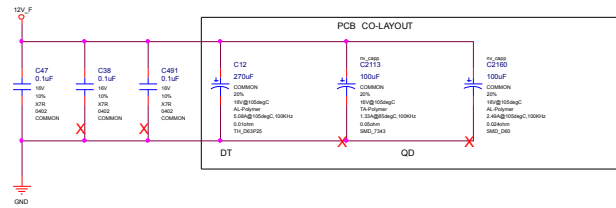
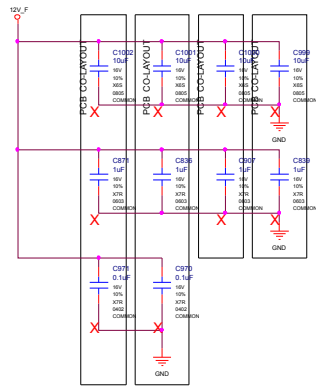


MICRO-STAR INT'L CO.,LTD

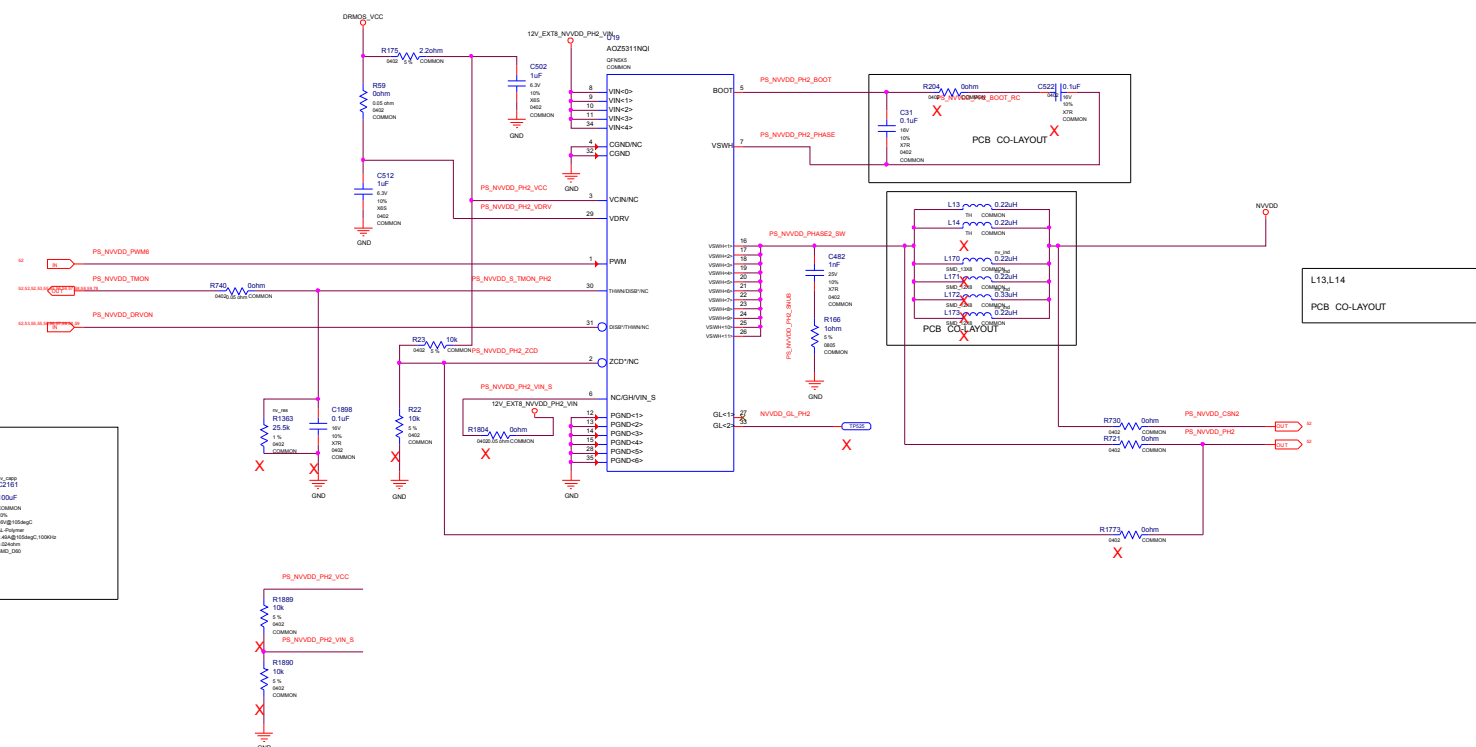
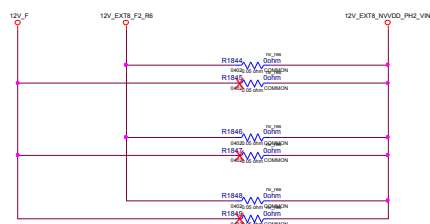
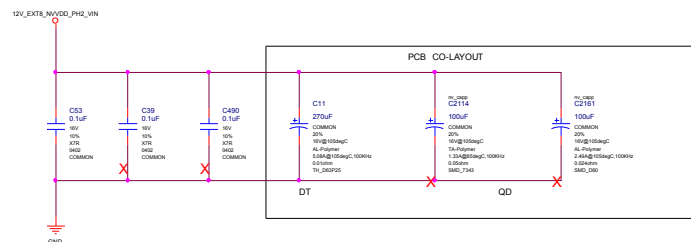
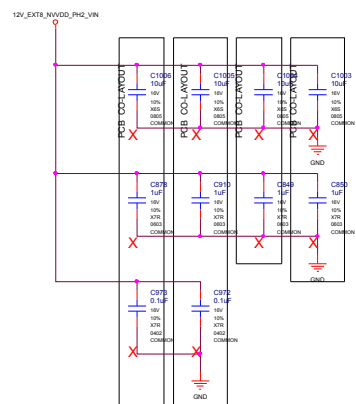
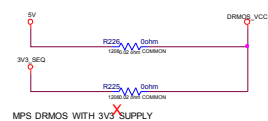
MS-V389

Size Custom	Document Description PS: NVDD Controller_OVR8	Rev 1.1
Date: Thursday, Jul 23, 2020		Sheet 63 of 72

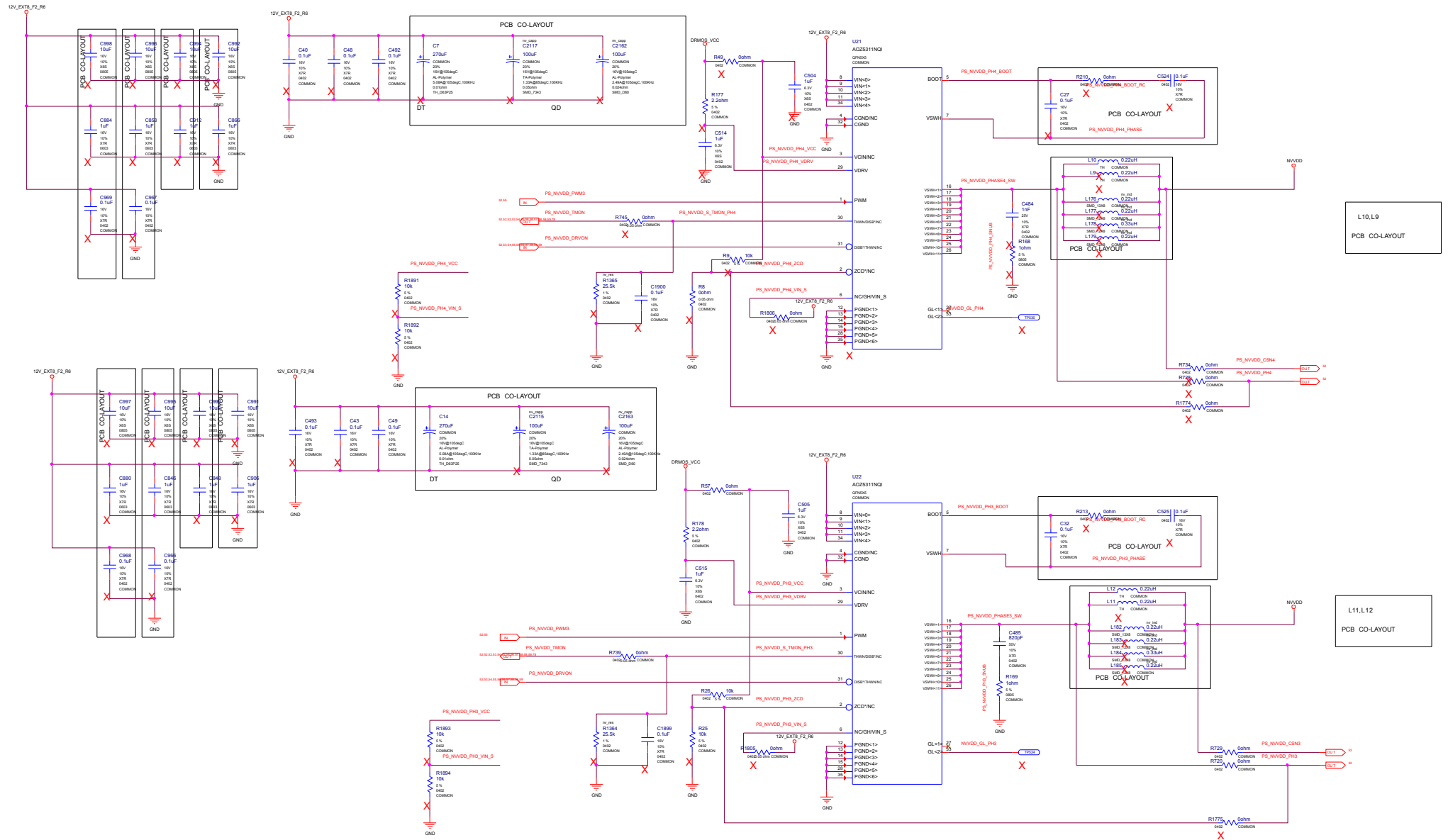
PS: NVVDD Phase 1



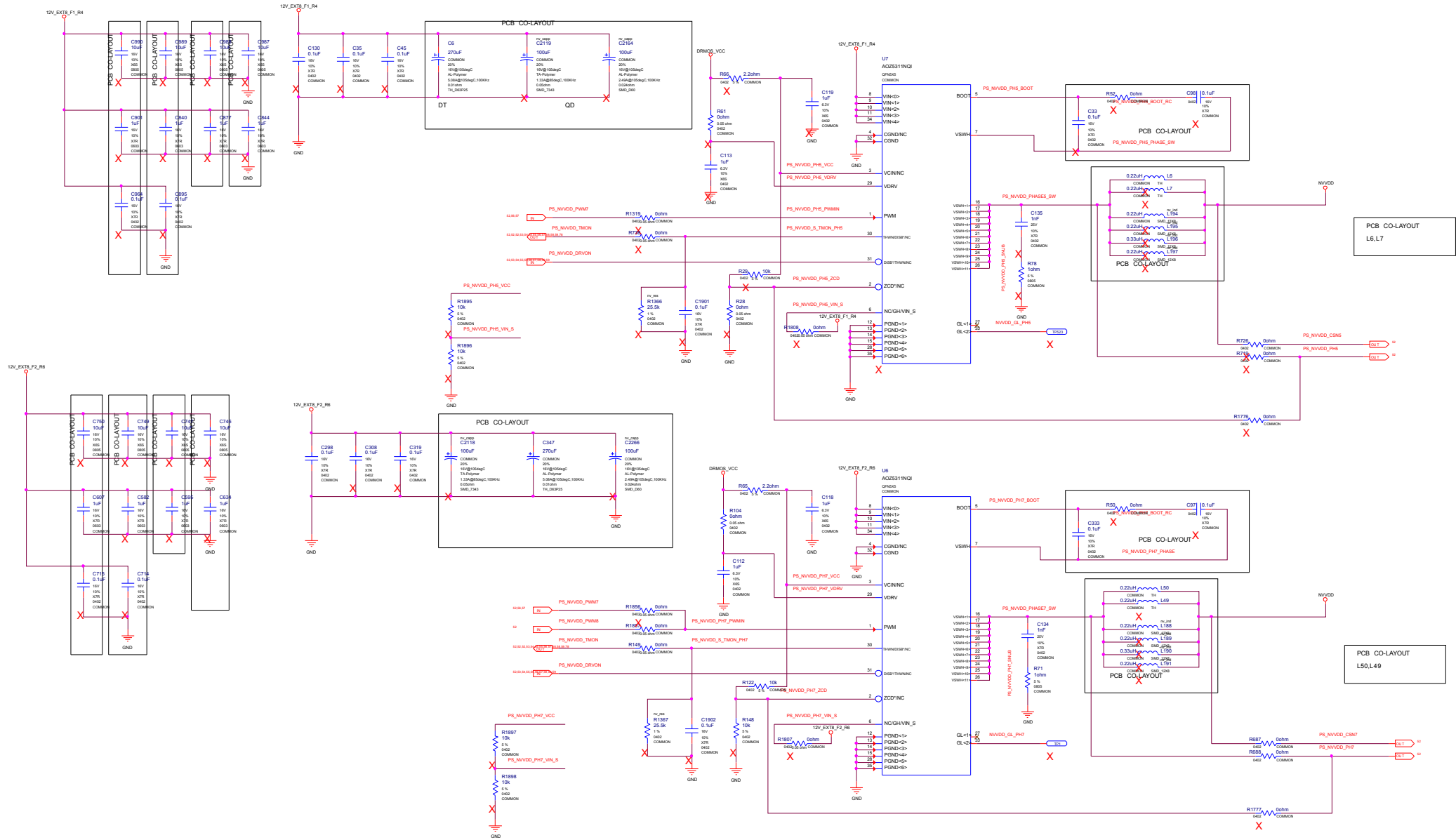
PS: NVVDD Phase 2



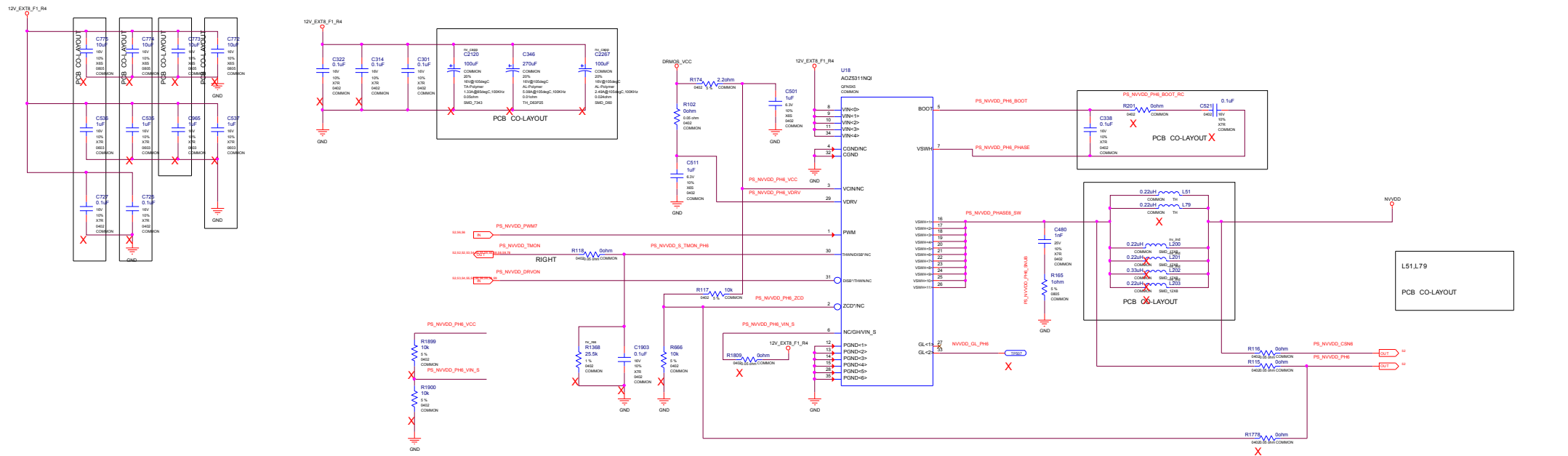
PS: NVVDD Phase 3 (PWM6), PHASE 4(PWM2)



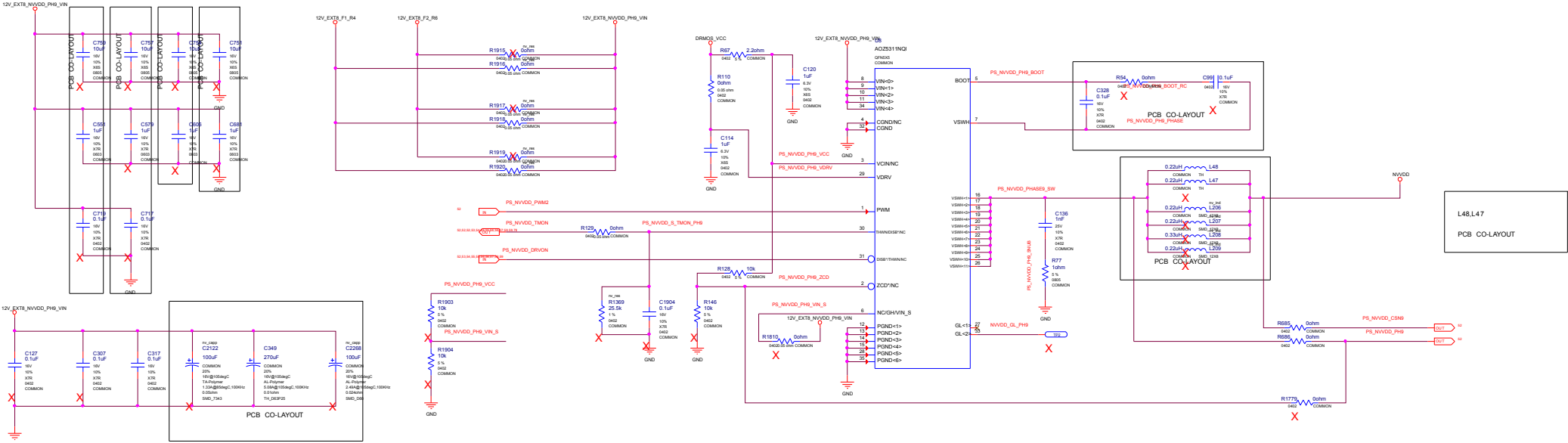
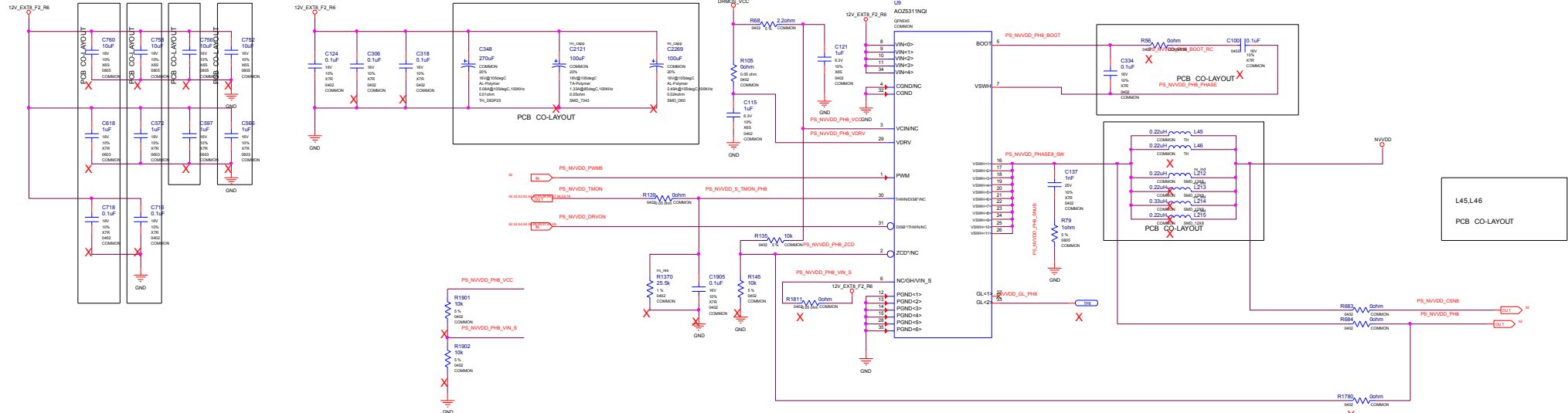
PS: NVDD PH 5(PWM2), PH7(PWM3)



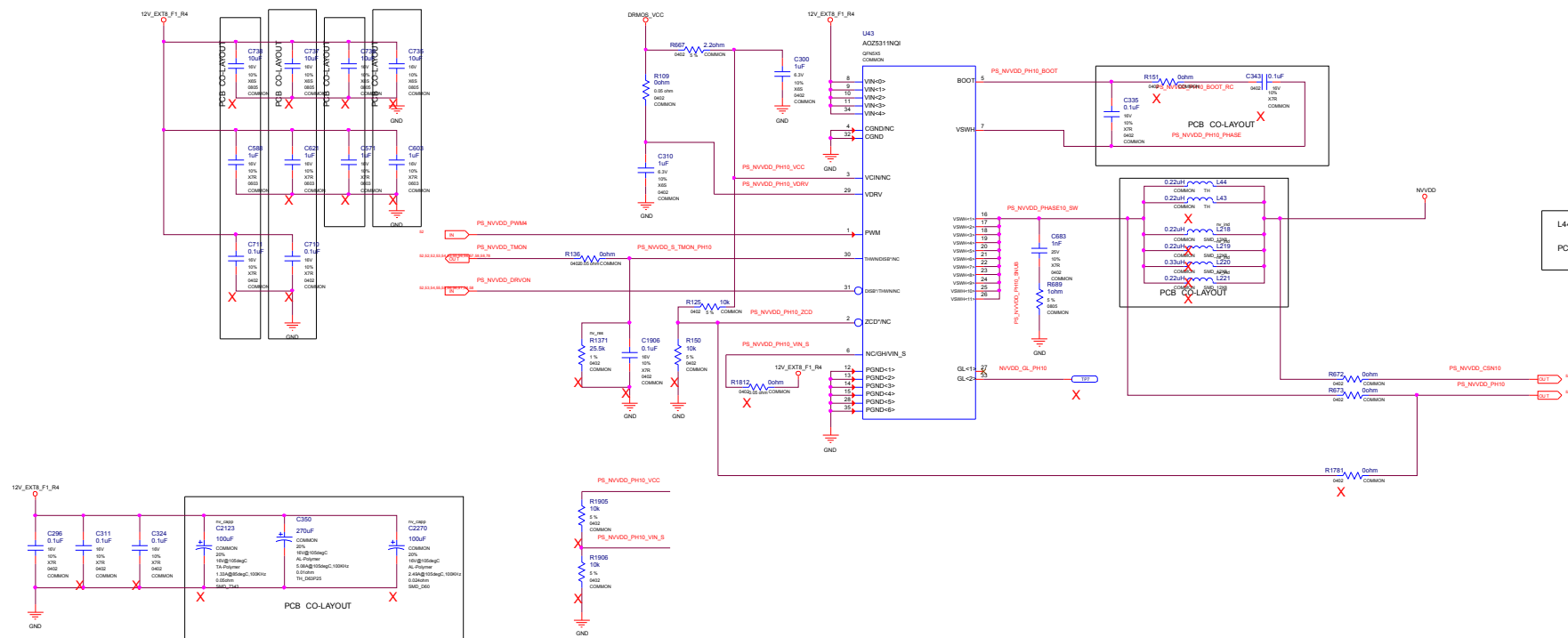
PS: NVVDD Phase 6(PWM7)



PS: NVVDD PH 8 (PWM5), PH 9(PWM8)



PS: NVVDD Phase 10 (PWM8)



PCB CO-LAYOUT
C131, C132, C133, C140, C141, C142, C2106, C2107, C2133, C2134, C2135, C2137, C264, C265, C266, C267, C61, C64, C65, C66, C67, C68, C69, C77, C80, C83, C88

PCB CO-LAYOUT
C103, C105, C106, C107, C108, C110, C1208, C125, C1254, C1256, C1267, C128, C144, C145, C146, C151, C152, C153, C154, C159, C160, C161, C162, C170, C173, C2092, C2100, C2101, C2102, C2103, C2104, C2138, C2139, C2140, C2141, C2142, C2143, C2144, C2272, C230, C231, C232, C233, C243, C245, C246, C248, C253, C254, C255, C256, C270, C274, C275, C276, C283, C289, C290, C291, C60202, C62004, C62005

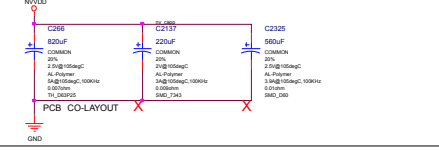
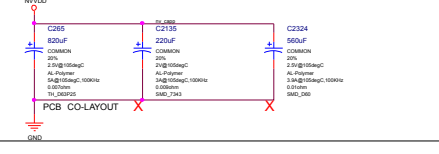
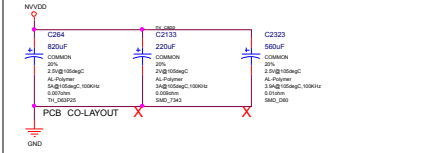
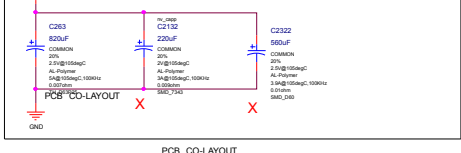
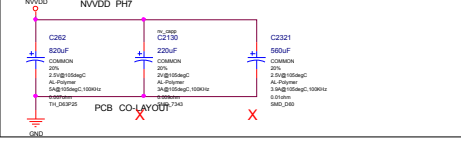
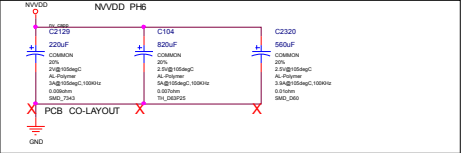
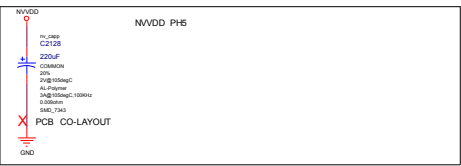
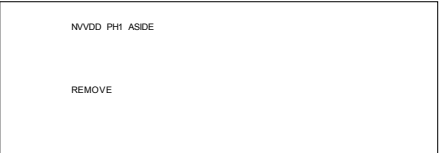
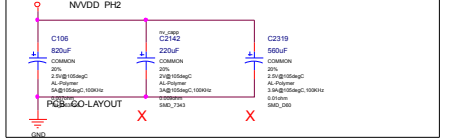
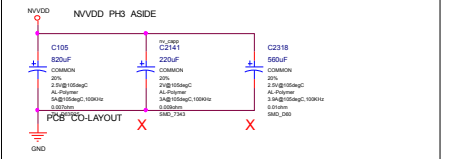
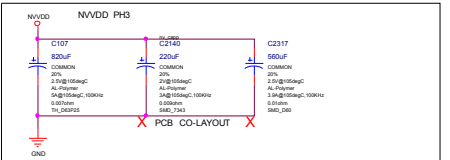
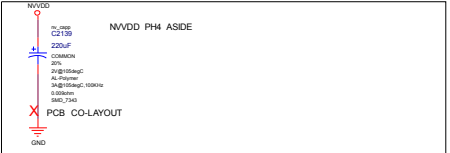
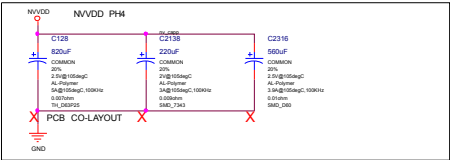
C163, C164, C166, C167, C2087, C2105, C2109, C2110, C2111, C224, C225, C261, C268, C269, C60354, C61428, C62, C63, C89, C91, C96

PCB CO-LAYOUT

2020_06_17

- 1.Fix J1,J2 to reverse 8 pins
- 2.Change L238,L52,L53 footprint

PS: NVDD OUTPUT CAP(TOP)

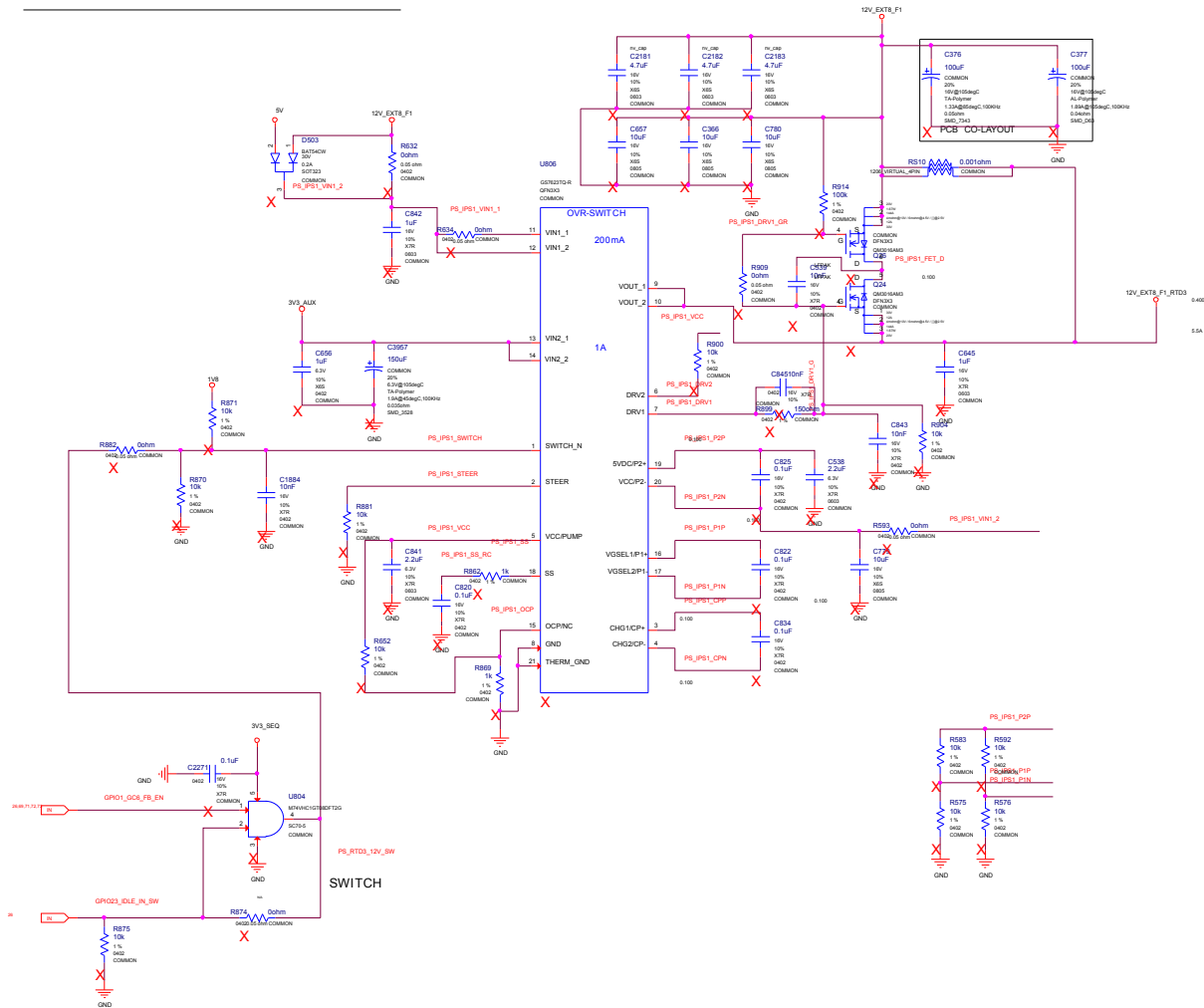


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PS: INPUT SWITCH RTD3

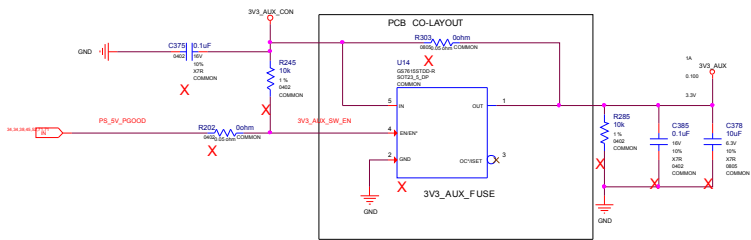
AND GATE LOGIC FOR P-BOARD

GPI01	GPI023	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

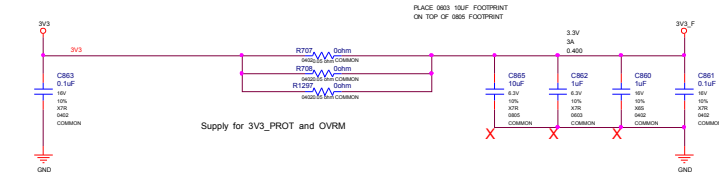


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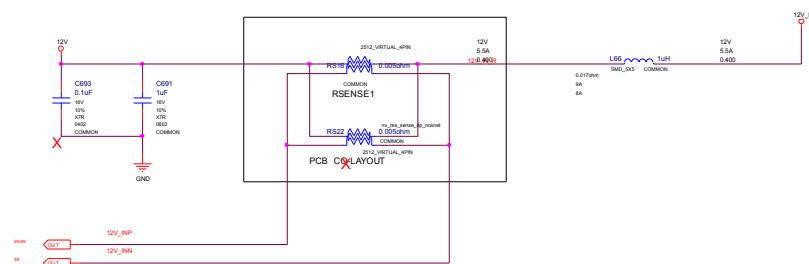
PS: Inputs, Filtering, and Monitoring



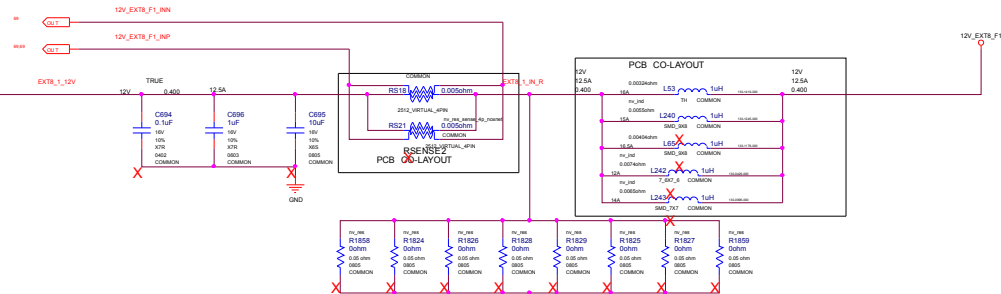
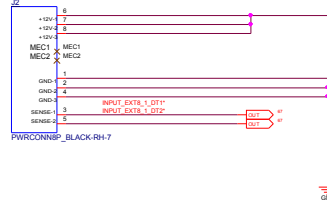
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W

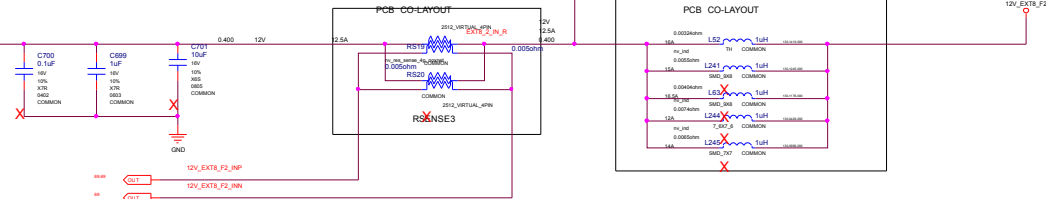
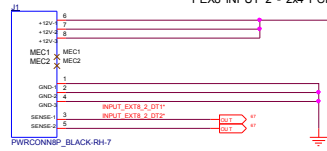


PEX8 INPUT 1 - 2x4 PCIE CON 150W

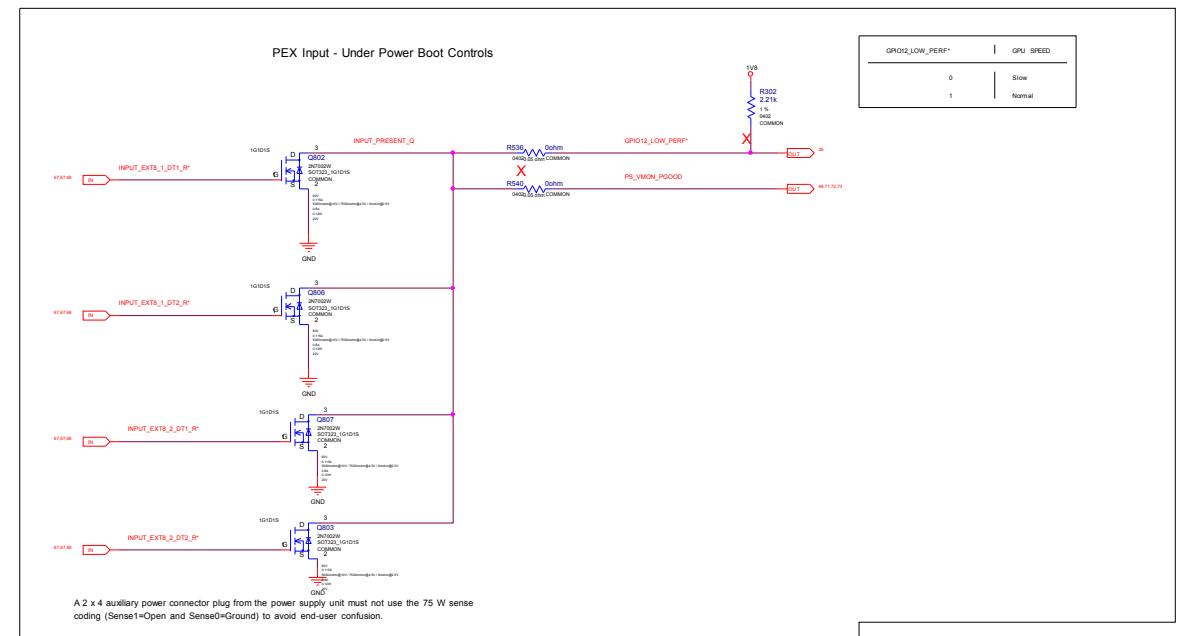
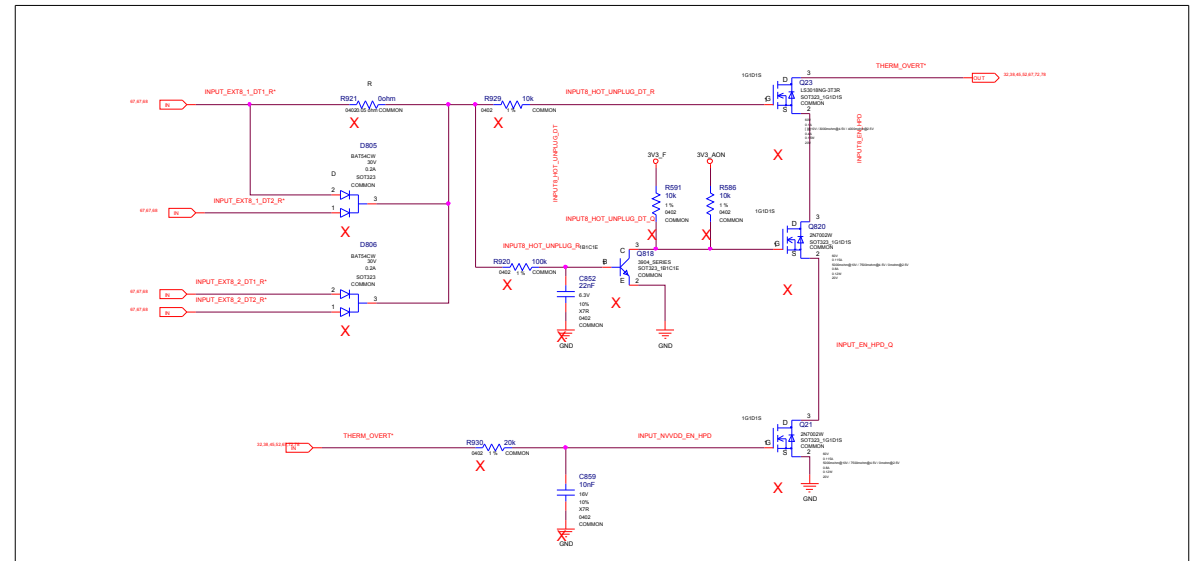
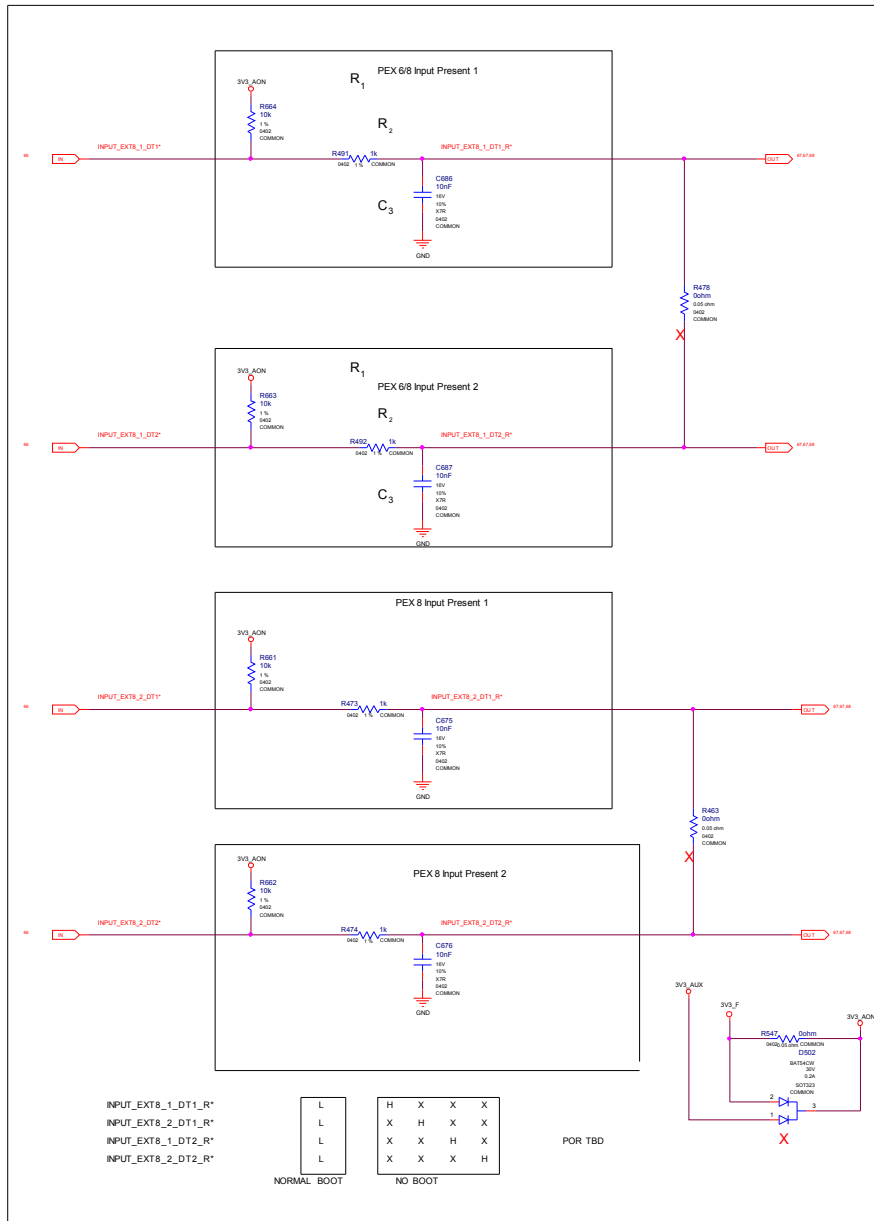


QD SKU CABLE

PEX8 INPUT 2 - 2x4 PCIE CON 150W



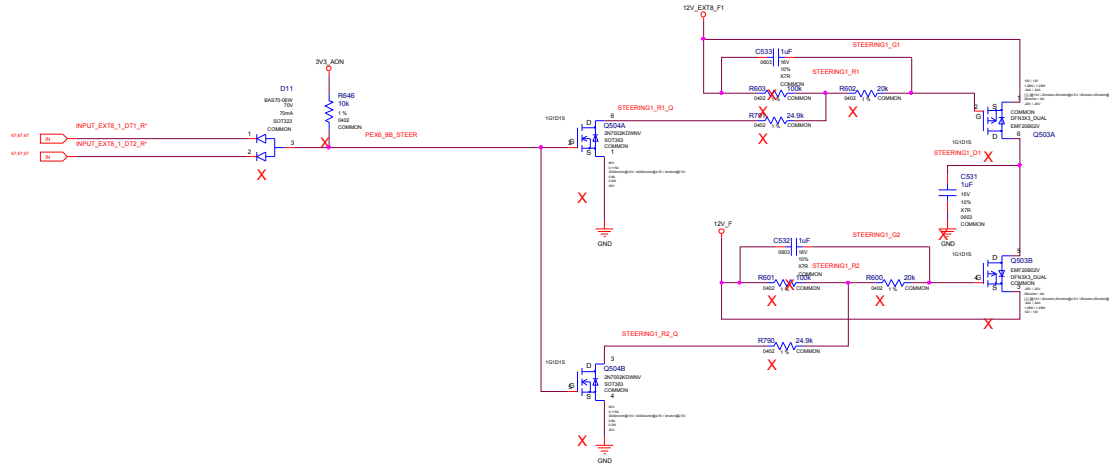
PS: 12V Current Steering & Hot Unplug Detect



PS: Discrete Steering

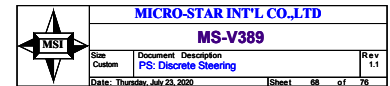
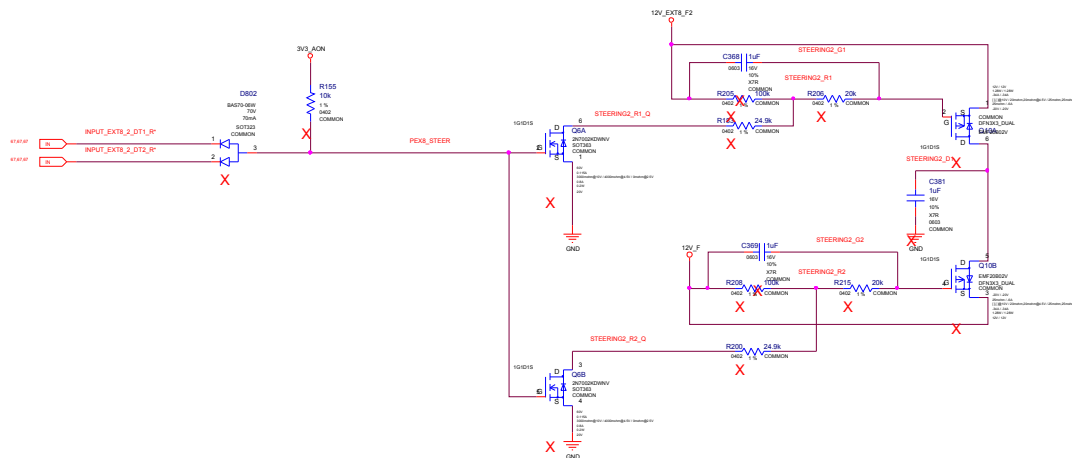
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1



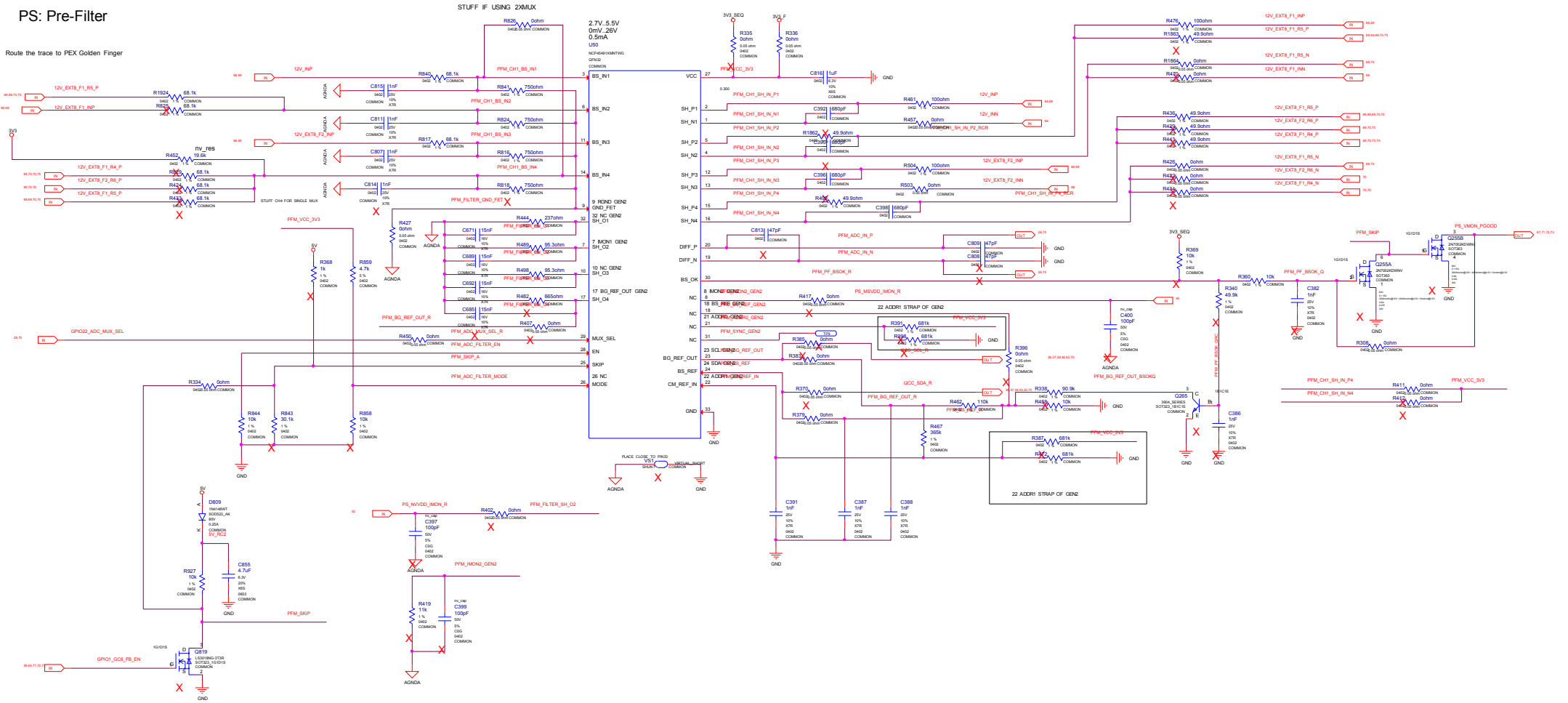
NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V_EXT8_F2

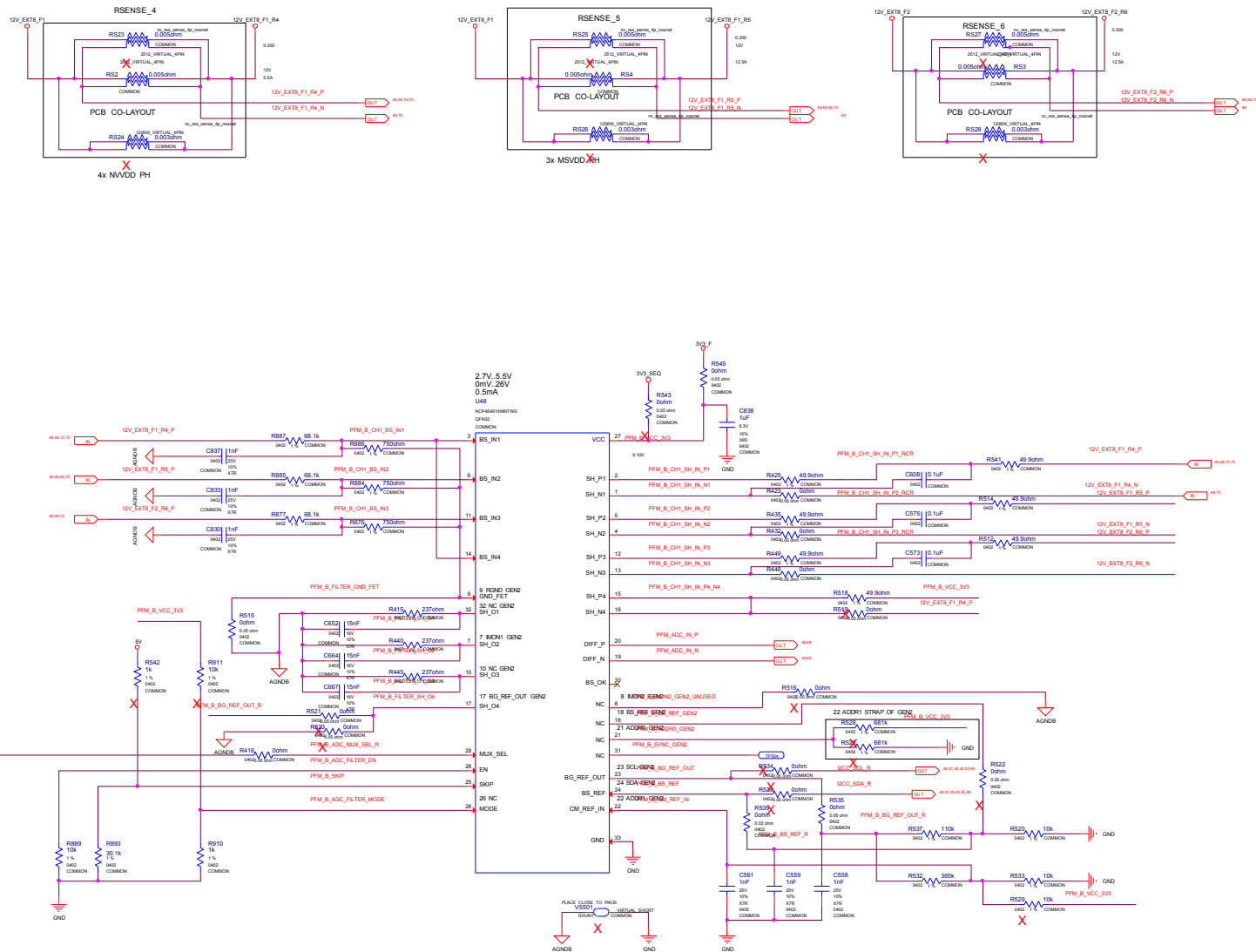


Route the trace to PEX Golden Finger

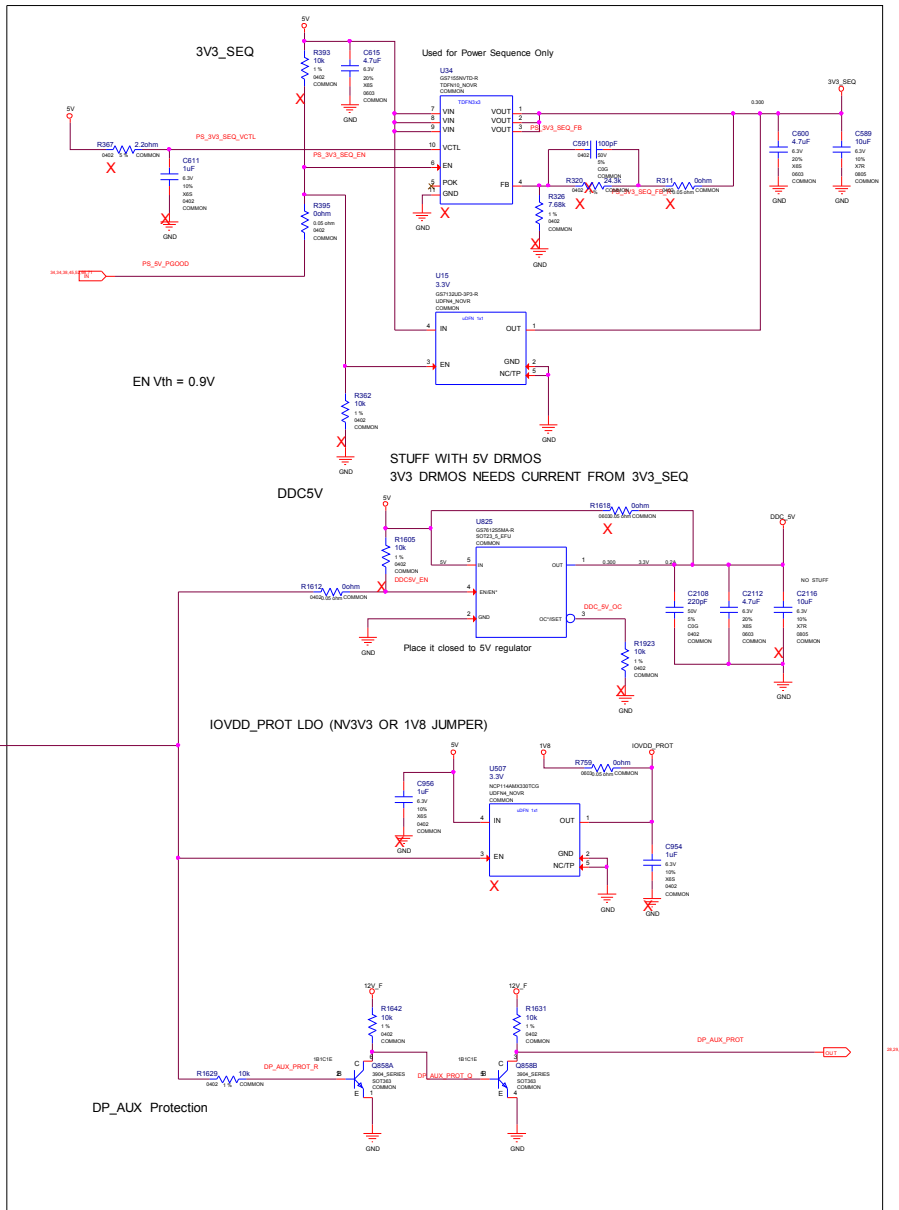
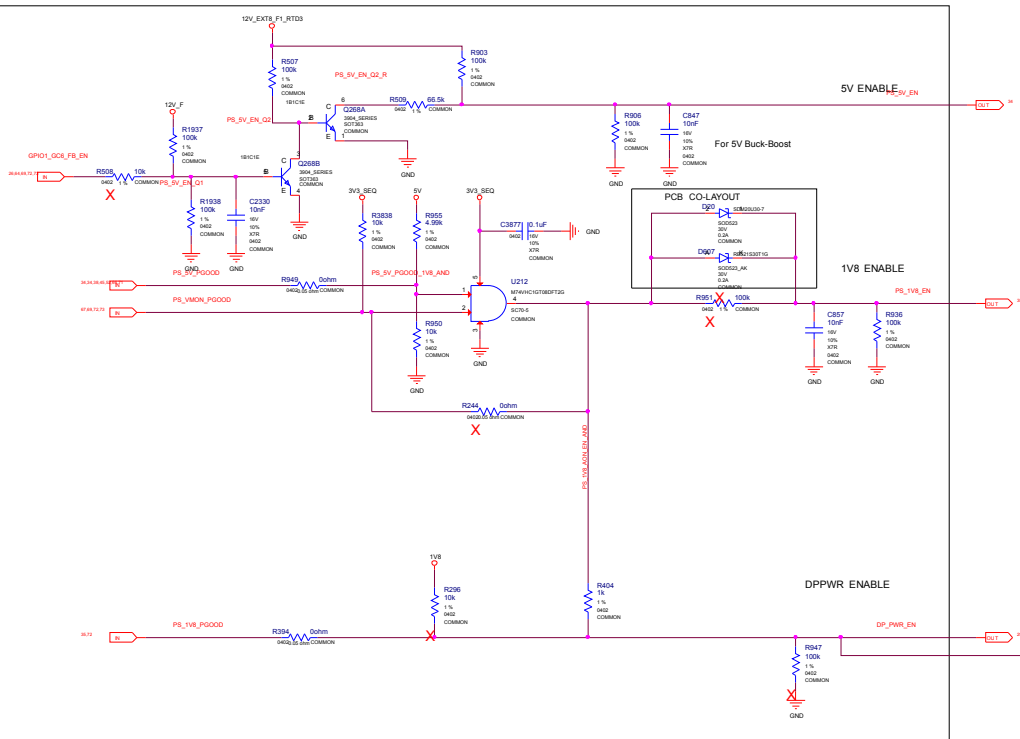
Route the trace to PEX Golden Finger



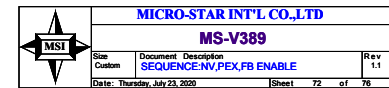
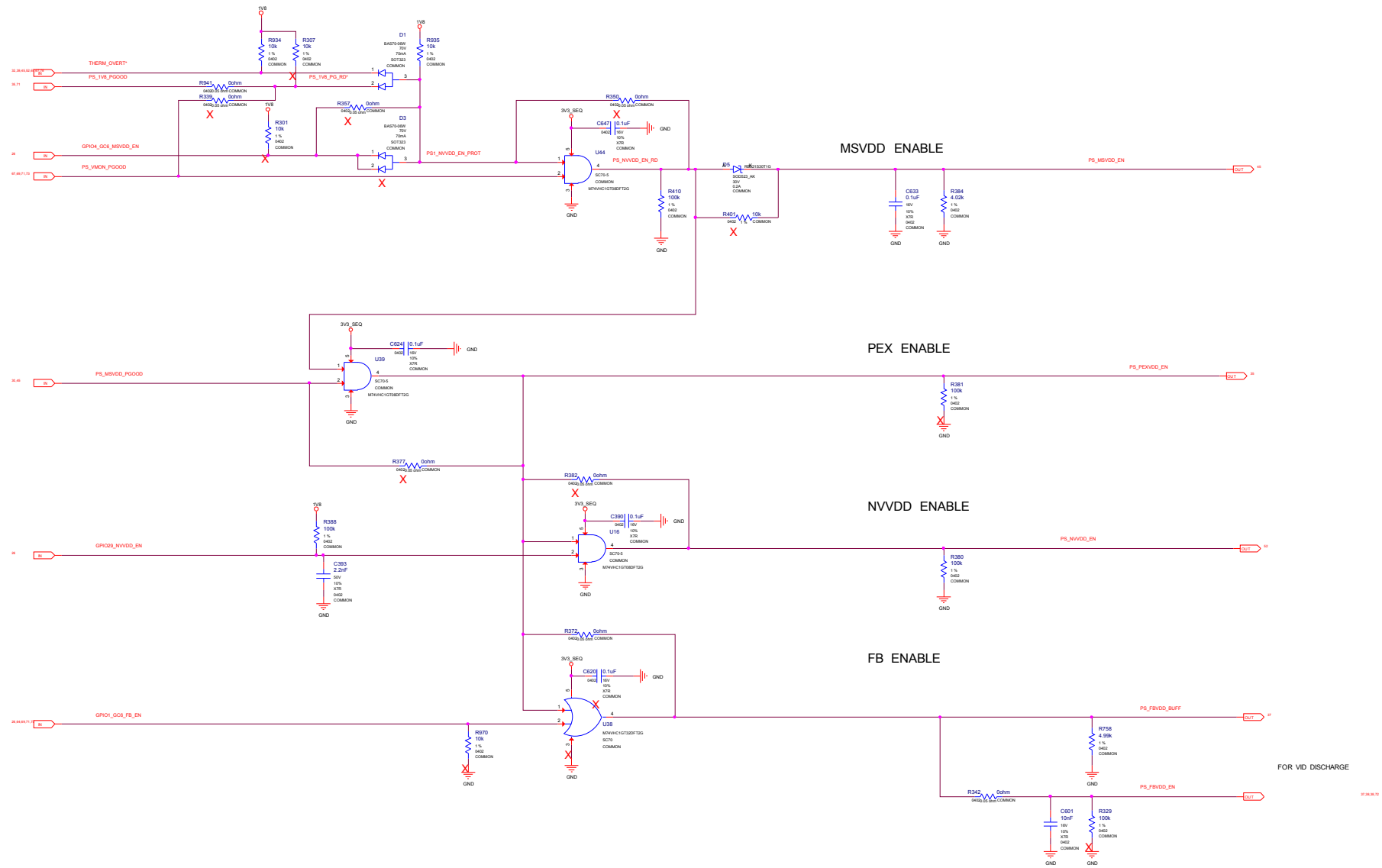
PS: Pre-Filter B

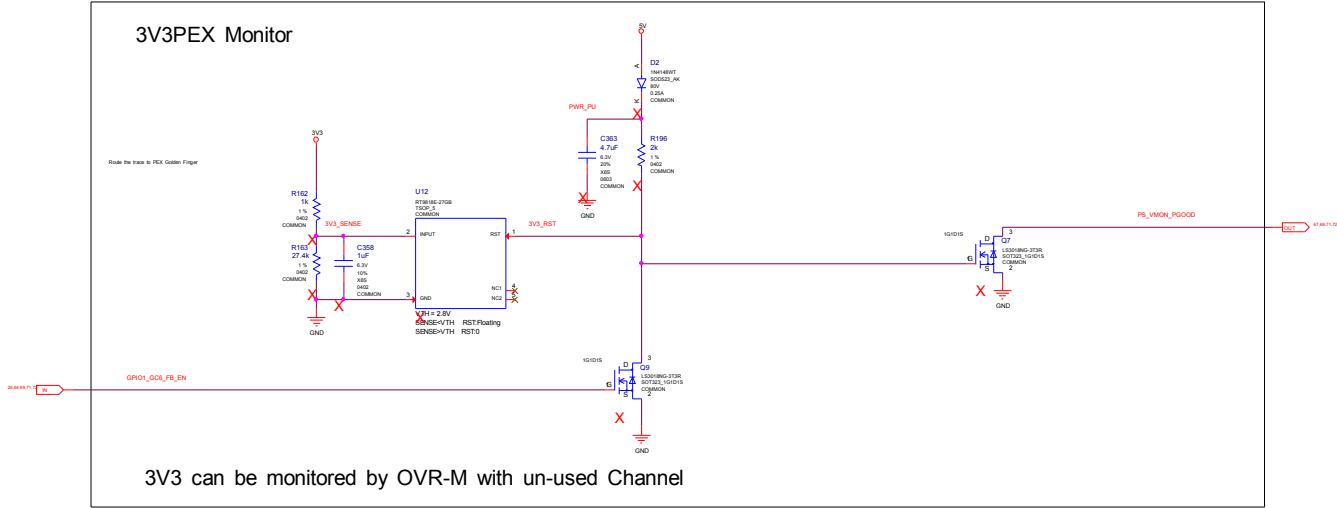


SEQUENCE:5V,1V8,3V3_SEQ ENABLE

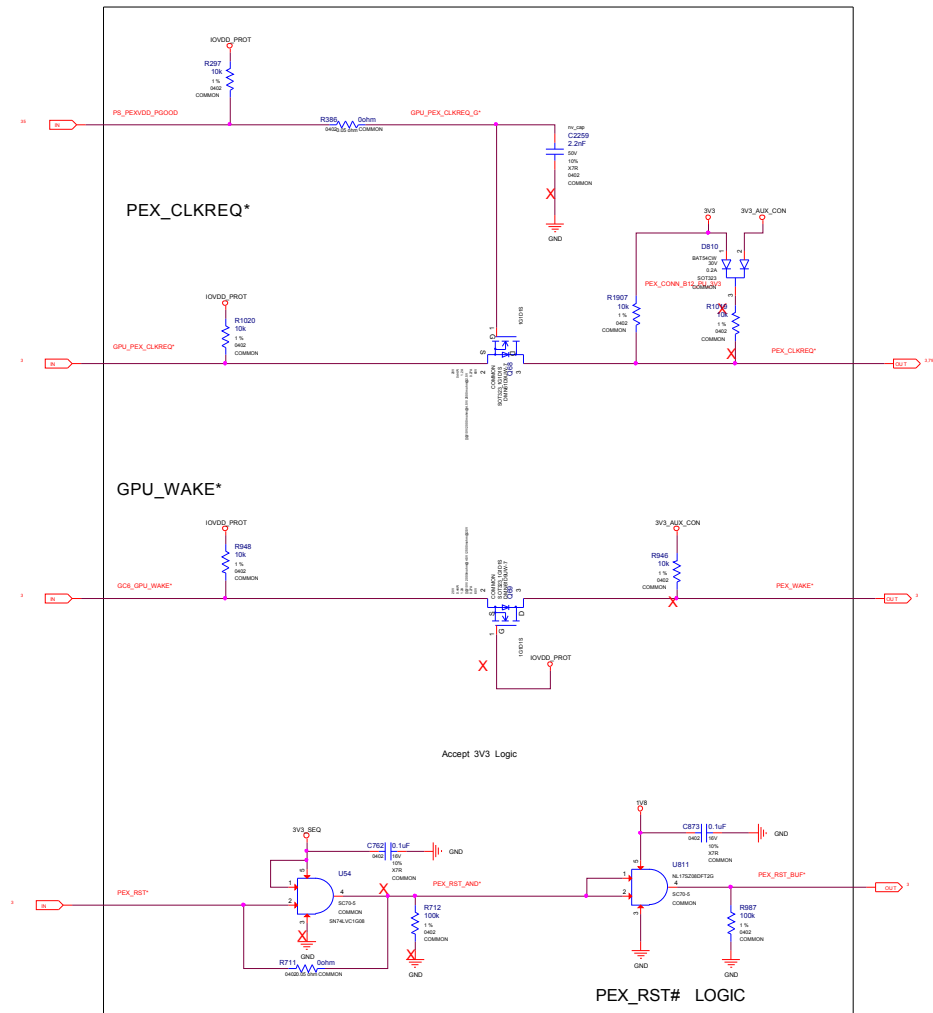


SEQUENCE:NV,PEX,FB ENABLE



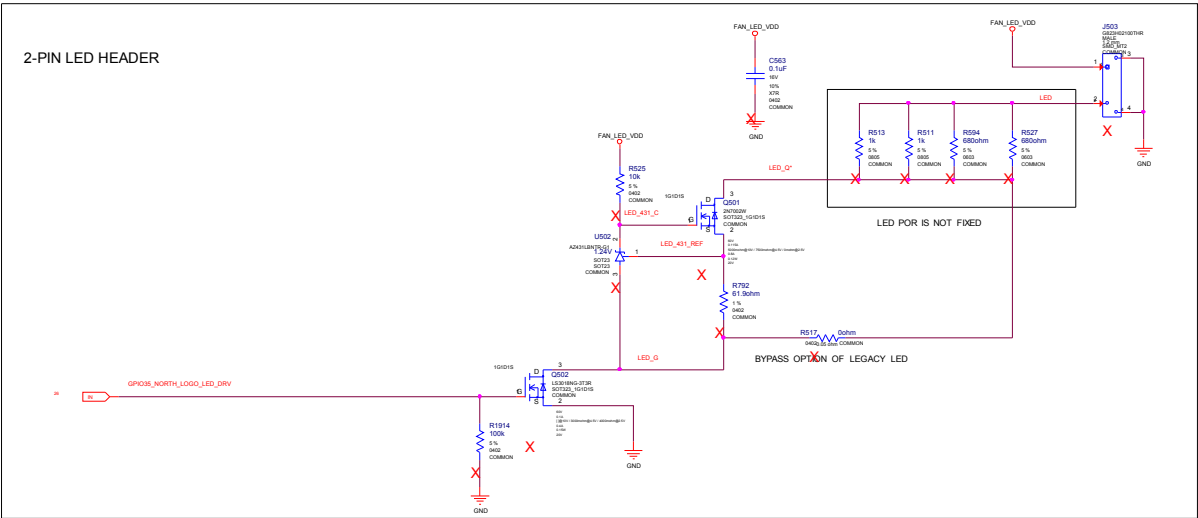


SEQUENCE:MISC

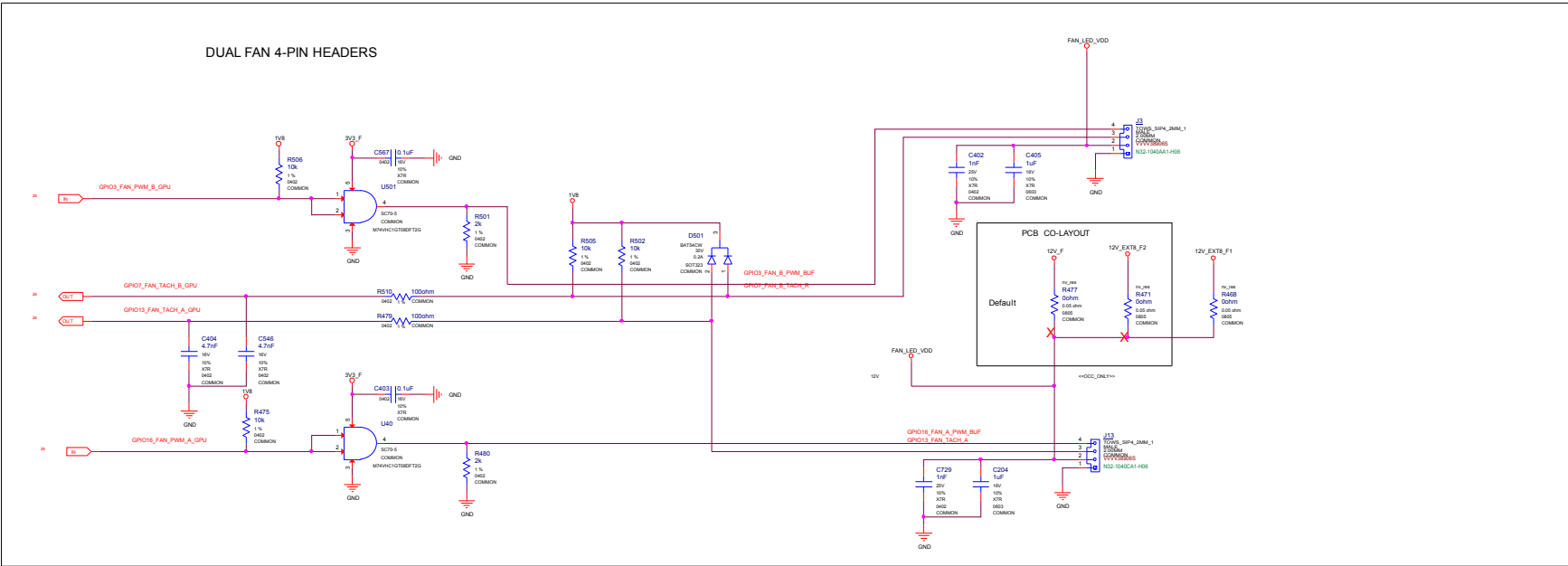


MISC: LED & FAN

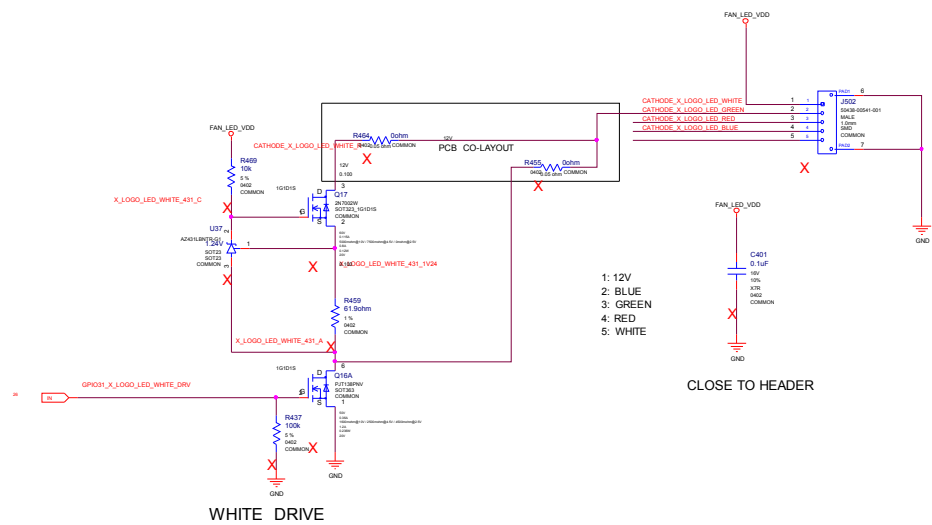
2-PIN LED HEADER



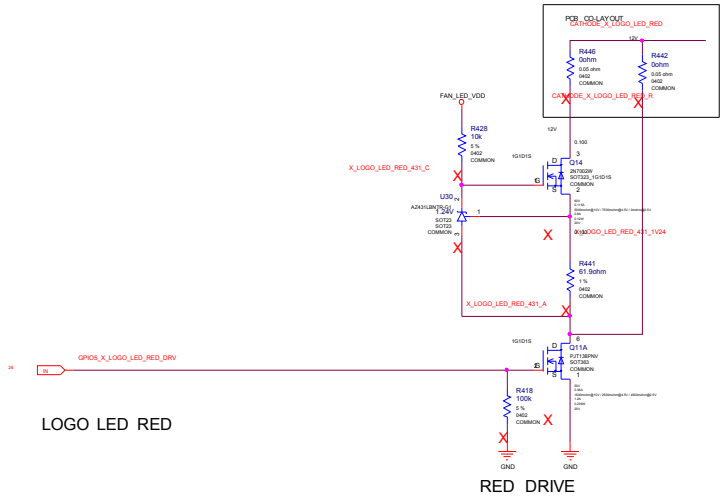
DUAL FAN 4-PIN HEADERS



MISC: RGBW LED REF

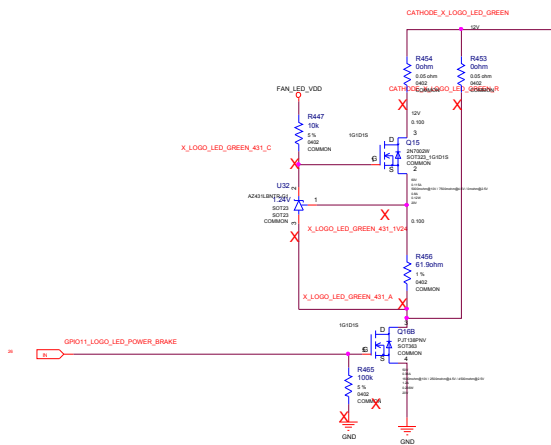


CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALINGN WITH PASH
IF ADDITIONAL POWER CONSUMPTION R
NEEDED, IT SHOULD BE ON LED MOD.

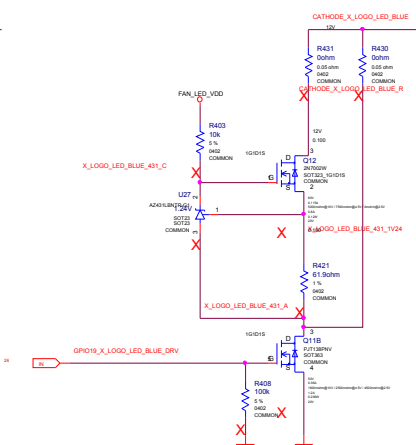


LOGO LED RED

RED DRIVE

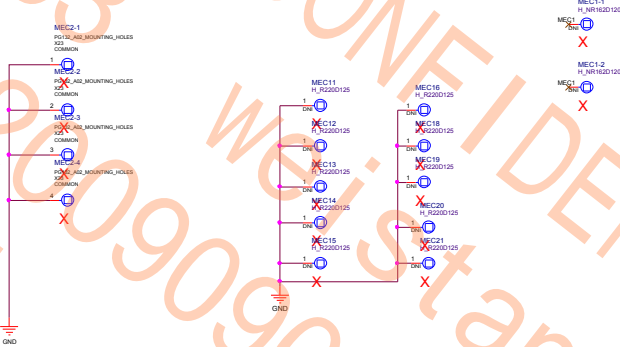
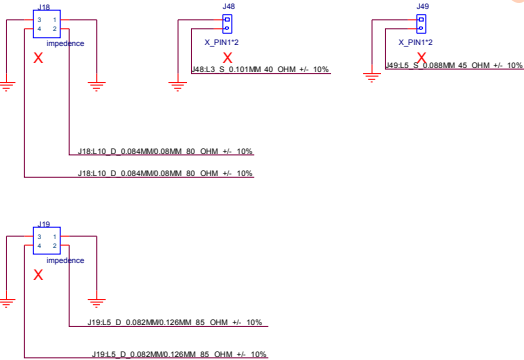
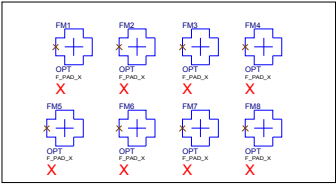


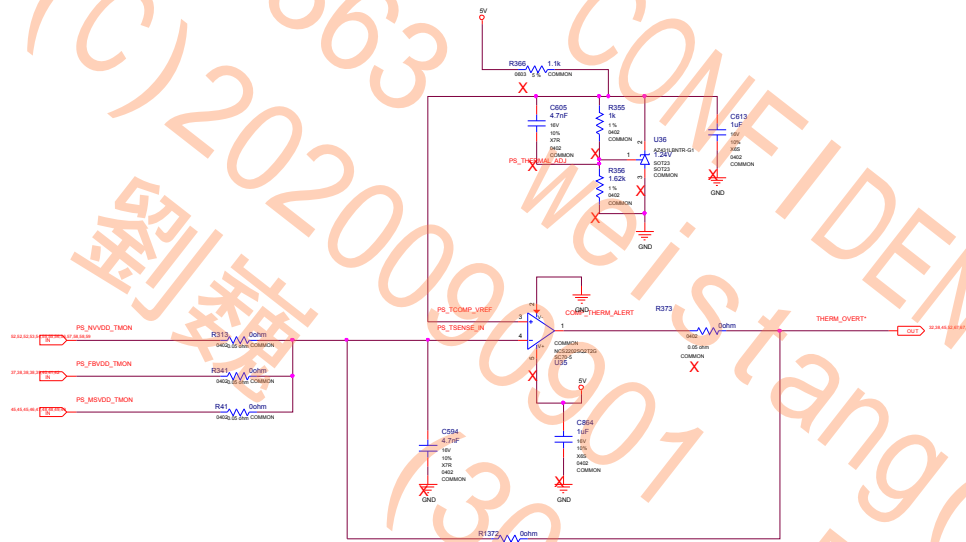
GREEN DRIVE



BLUE DRIVE

Mechanical: Mounting holes



[illegible]

PCI TERM

