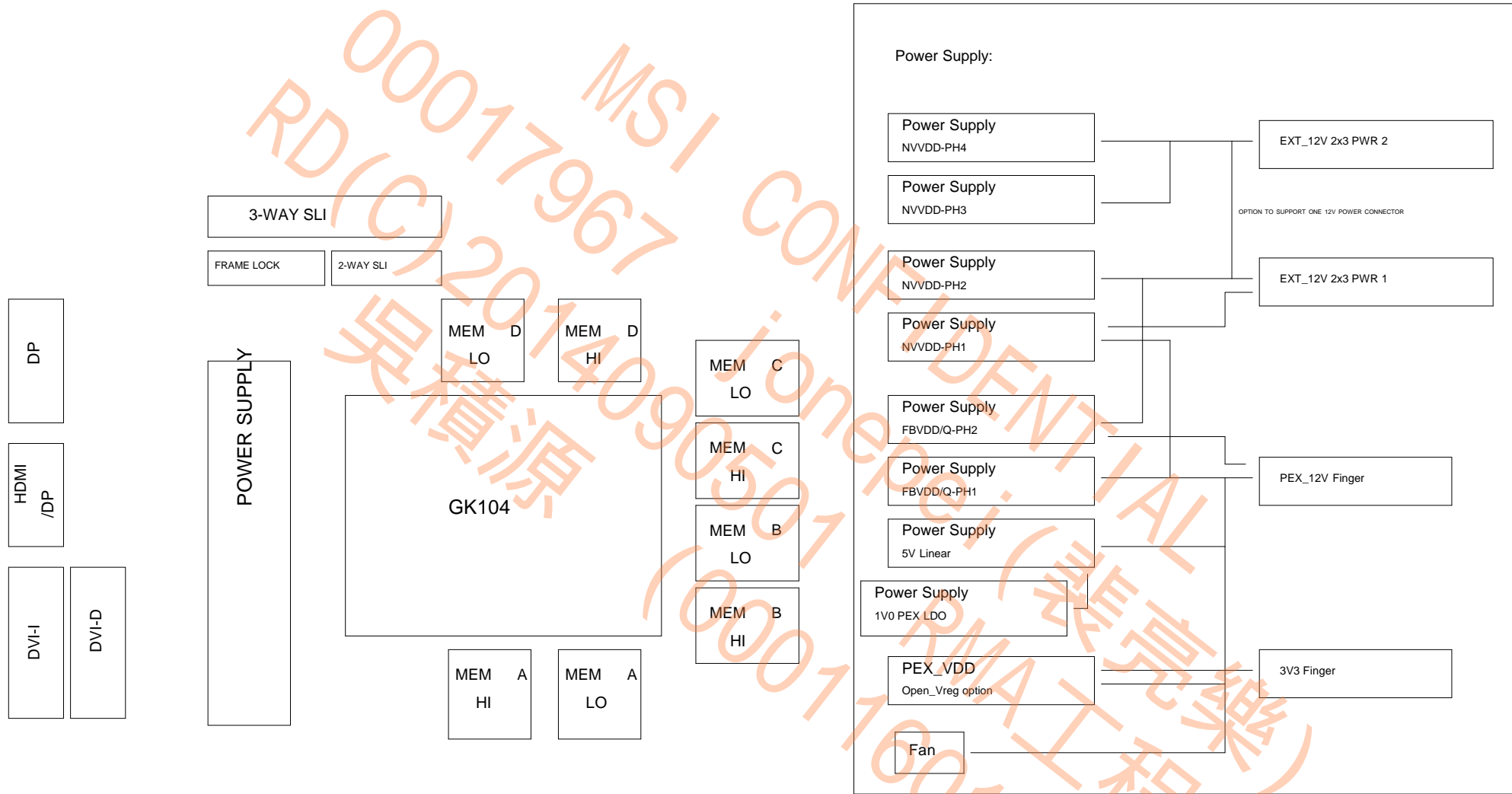


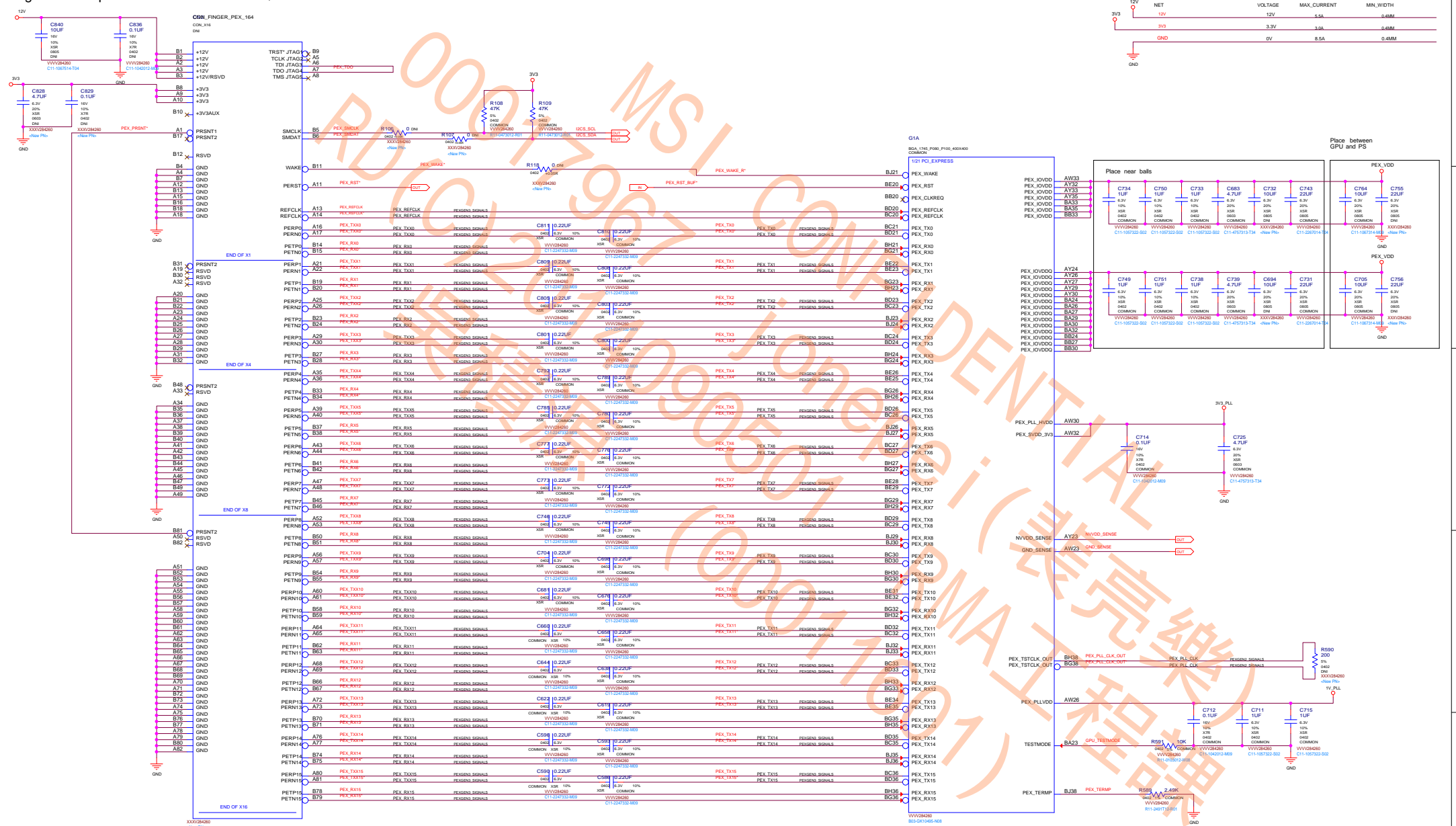
TABLE OF CONTENTS

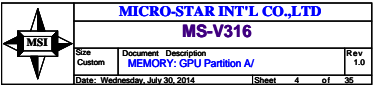
Page	Description
	Base on V284-81
P4~11	1. Del co-layout 16bit memory 2. Add FBVDDQ decoupling capacitor
P13	Add NVVDD decoupling capacitor
P15	1. Add ESD PROTECTION 2. Add AC Coupling capacitors
P16~18	Add ESD PROTECTION
P19	Change MIOA/B circuit
P21	Add 6-pin Fan connector
P25	PWM change to NCP81174
P26	Change to NCP81162 DOUBLERS
P27~28	Change to NCP81061
P29	Change to reverse 6 & 8-pin Power Connector
P32	Add NCT7511 FAN2
P33	Power Connector Hot unplug
P34	Add GeForce Logo LED & VID_PLL power

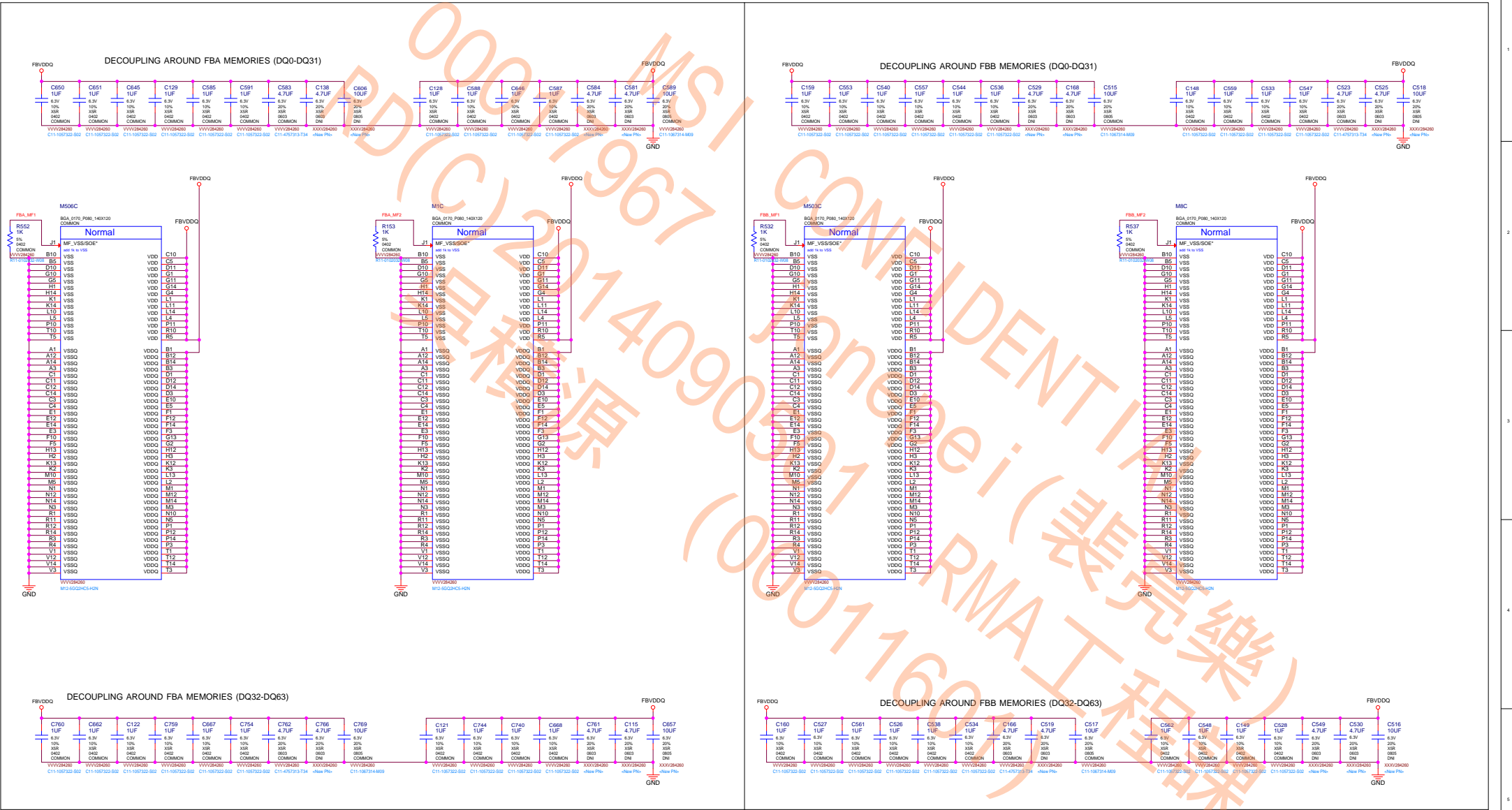
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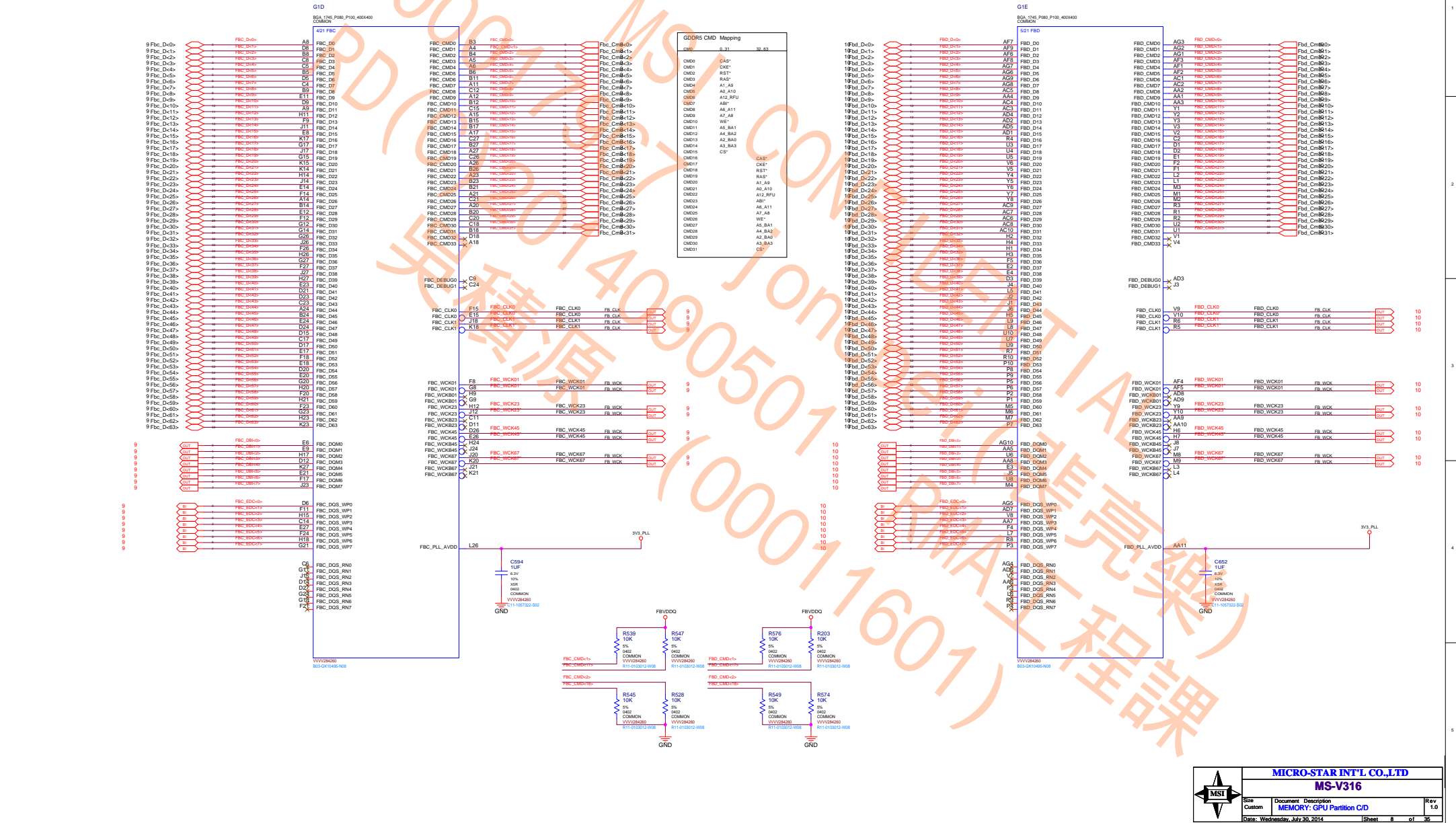
Page	Description
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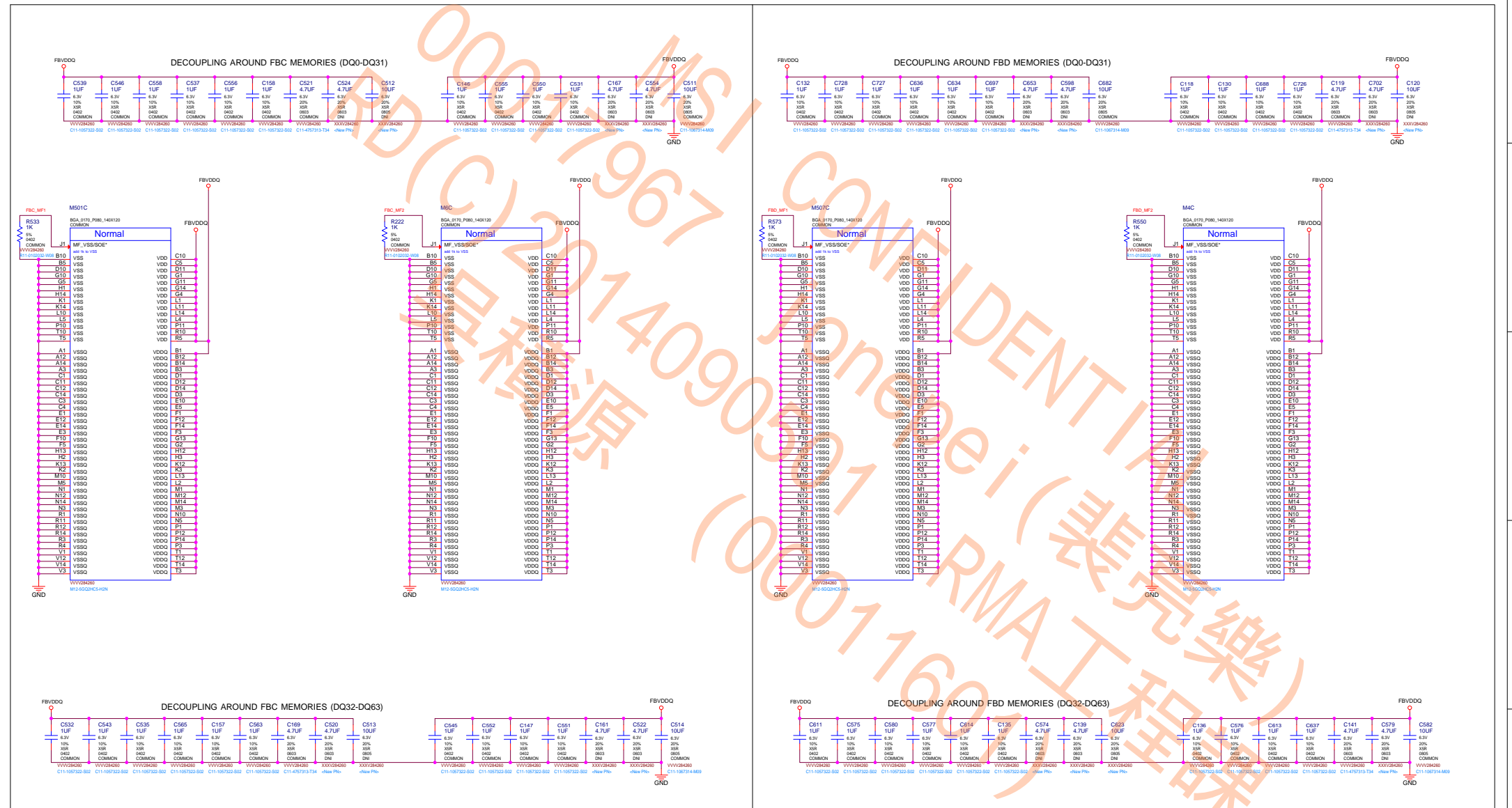


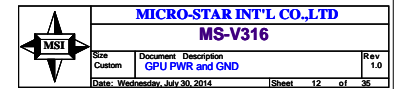


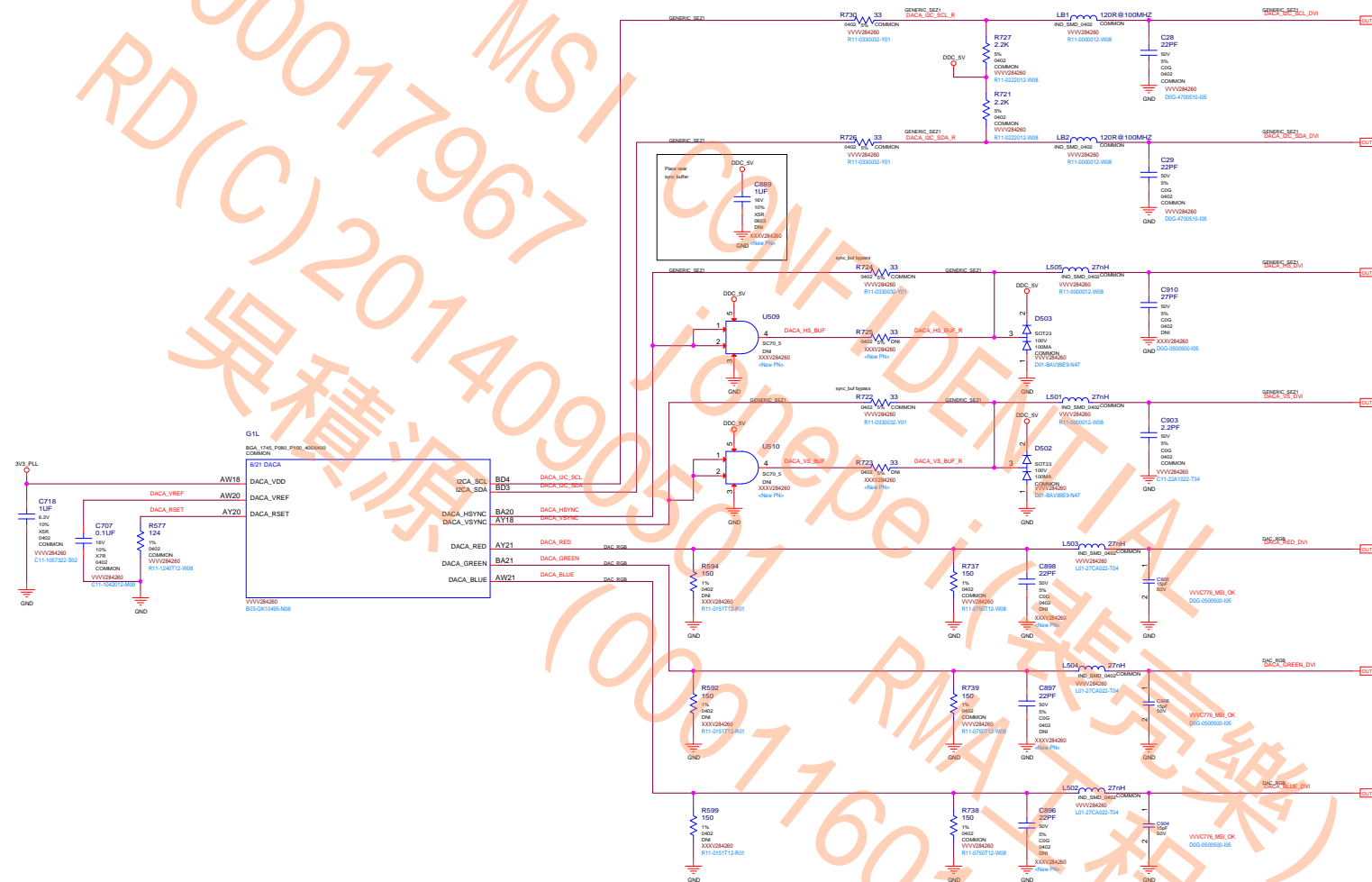


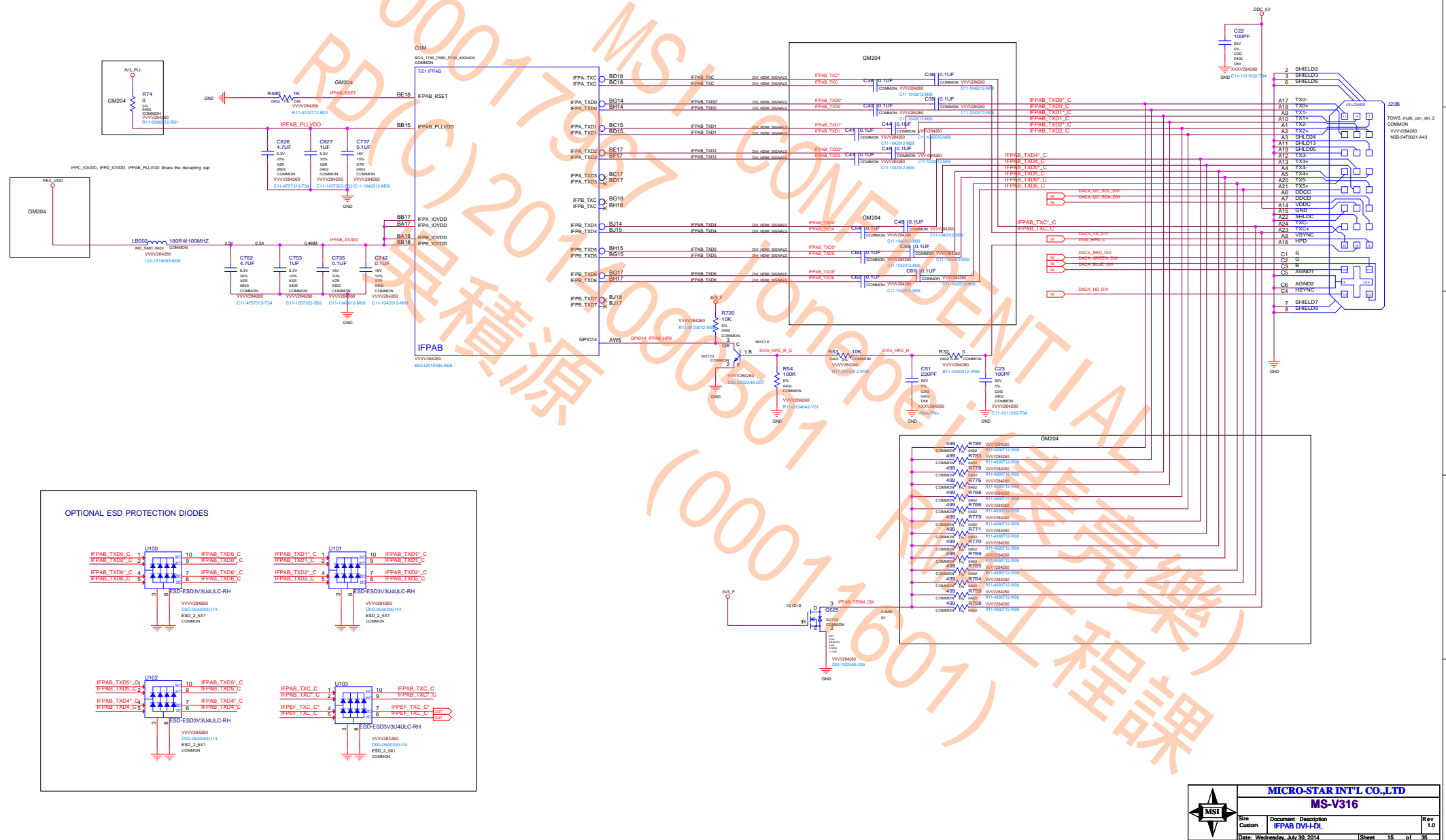








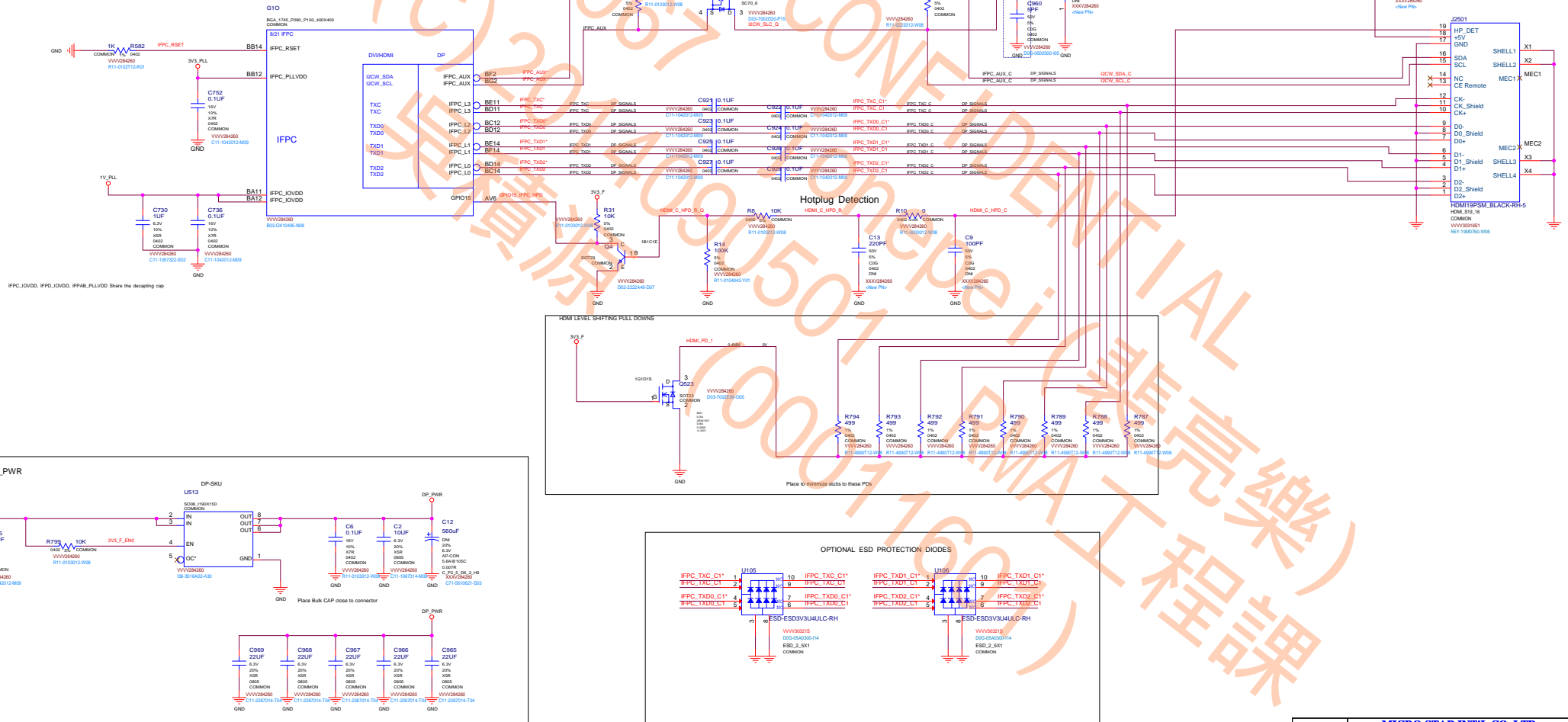




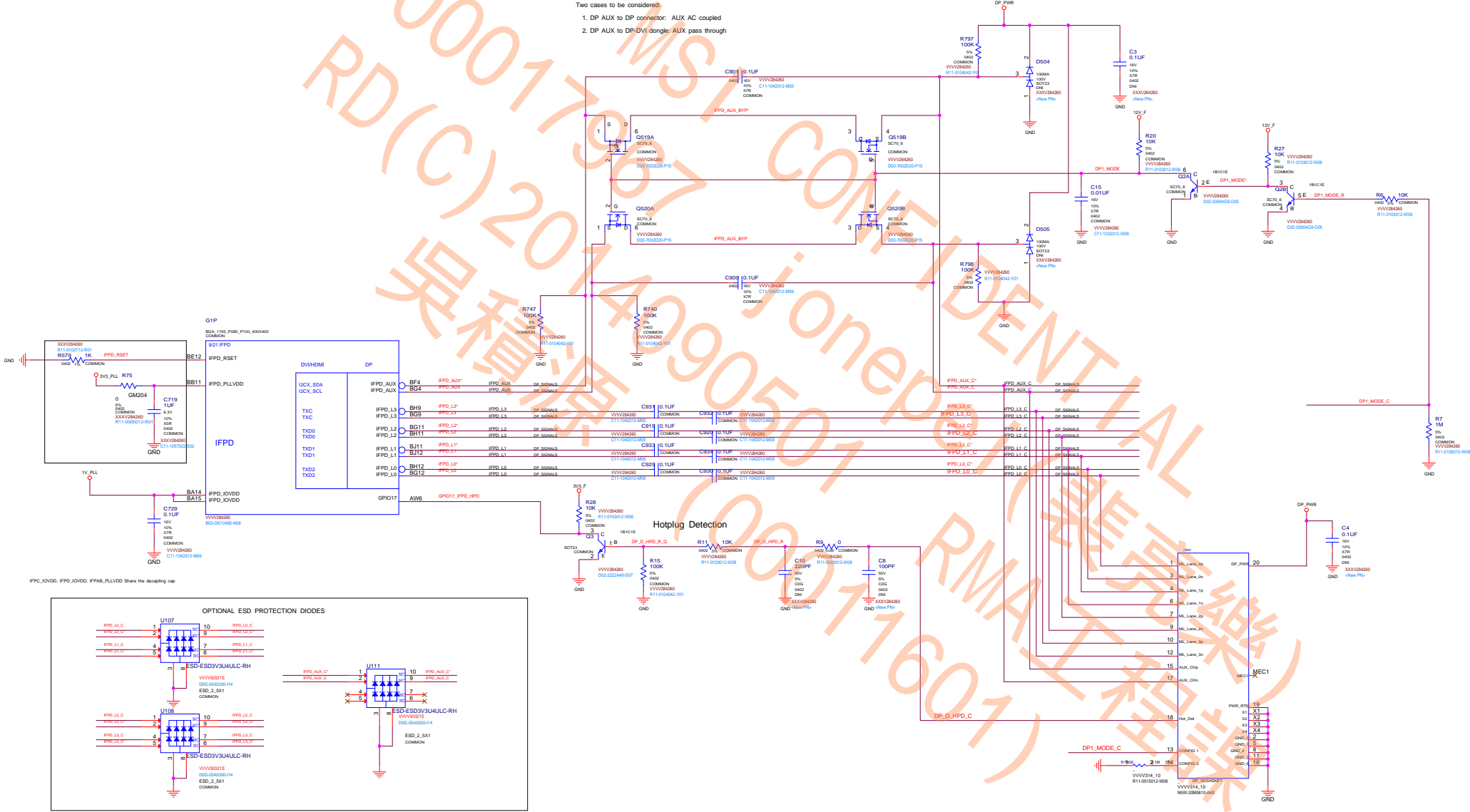
Two cases to be considered:

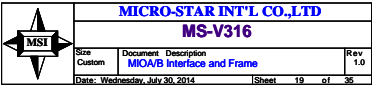
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

* I2C to DDC level switching



- Two cases to be considered:
- 1. DP AUX to DP connector: AUX AC coupled
 - 2. DP AUX to DP-DVI dongle: AUX pass through





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吳積源 (00011601)

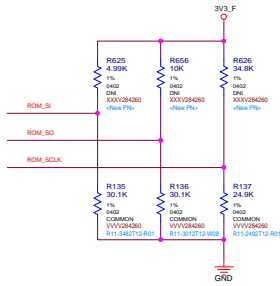
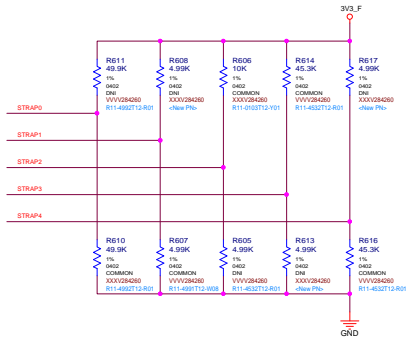
	MICRO-STAR INT'L CO.,LTD		
	MS-V316		
	Size	Document Description	Rev
	Custom	STEREO CONNECTOR	1.0
Date: Wednesday, July 30, 2014			Sheet 20 of 36

STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	1001 - (0x1189)*	10K PU -32S GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		
ROM_SI	RAMCFG[0]*	0*	
	RAMCFG[1]*	1*	64Mx32/32-bit type for SMC5 primary memory 35K PD*
	RAMCFG[2]*	1*	
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	30k PD*
	FB[0]_APERTURE_SIZE*	1* For 128MB*	
	FB[1]_APERTURE_SIZE*	0* For 128MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0* DISABLE*	
	PCI_DEVID_EXT[5]*	0* For 0x1189*	25K PD*
	SUB_VENDOR*	1* Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0* For 0x1189*	

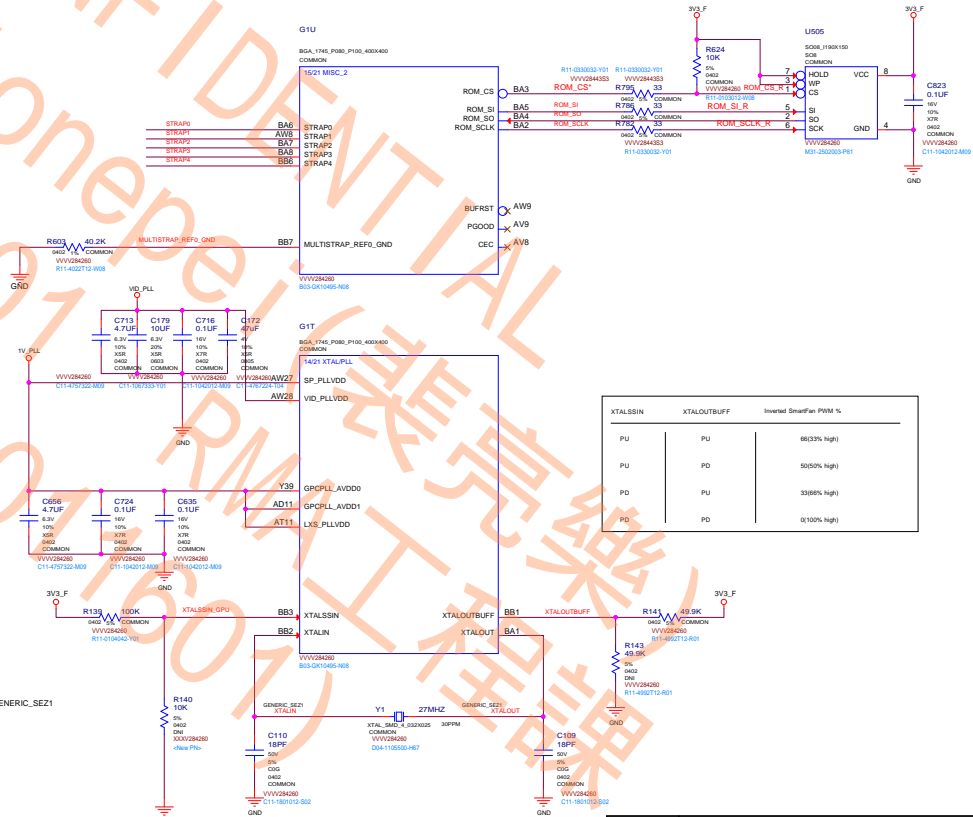
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit	Elpida
0010	32Mx32 256-bit	Hynix
0011	32Mx32 256-bit	Samsung
0100	Reserved	
0101	64Mx32 256-bit	Elpida
0110	64Mx32 256-bit	Hynix
0111	64Mx32 256-bit	Samsung

	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	NO
BINARY BRINGUP	NO
MULTI-LEVEL	40.3k 1% TO GND



remove XTALSSIN_GPU/GENERIC_SE21



XTALSSIN	XTALOUTBUFF	Inverted SmartFan PWM %
PU	PU	86(33% High)
PU	PD	50(50% High)
PD	PU	33(66% High)
PD	PD	0(100% High)



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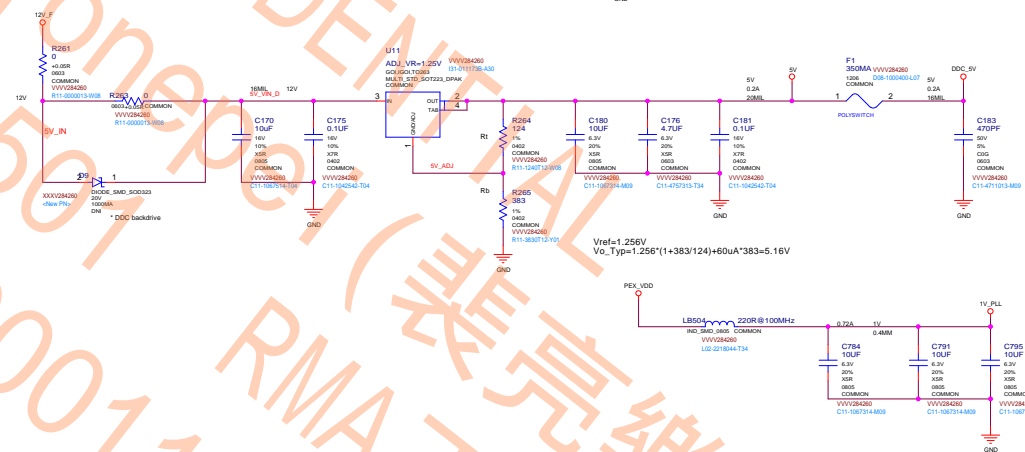
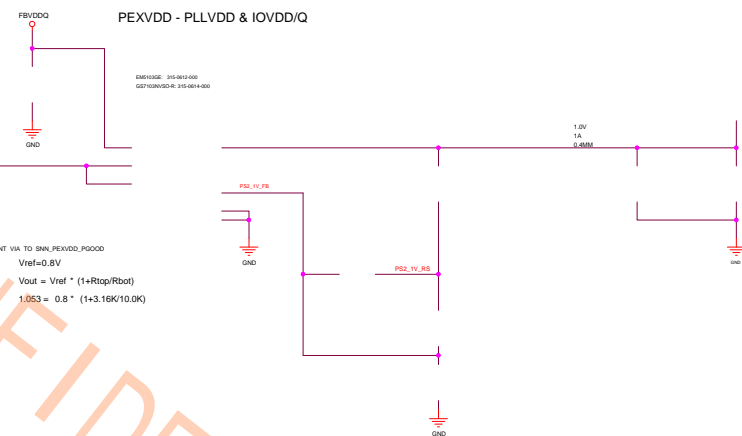
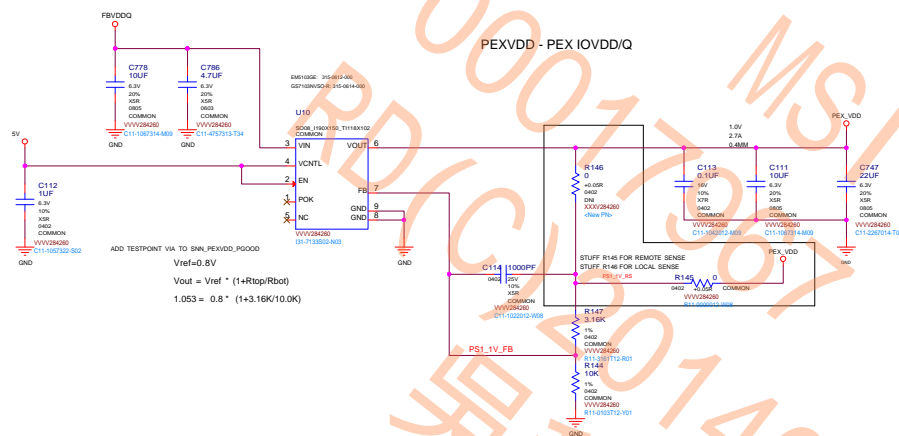
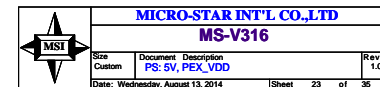
Size Custom

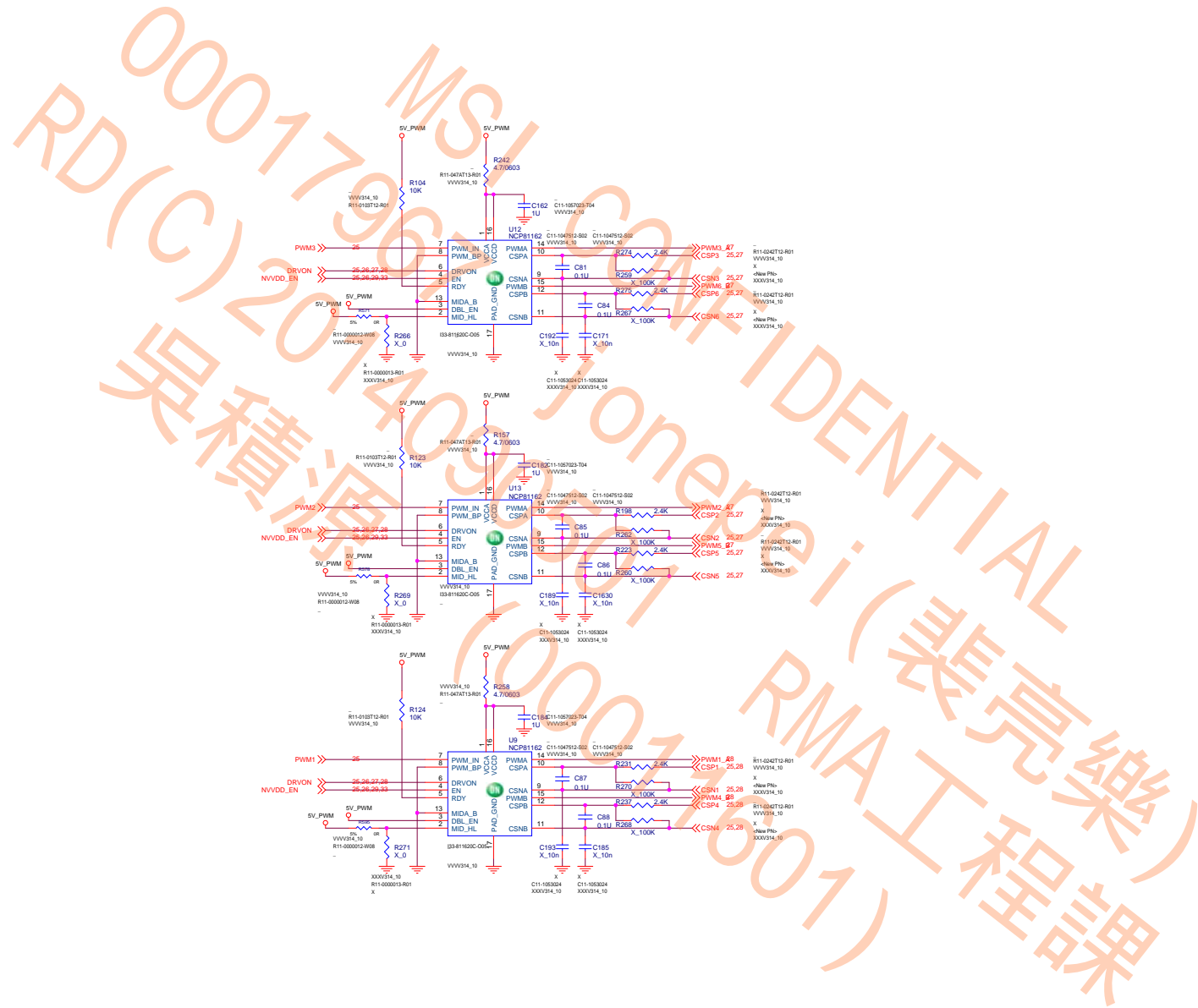
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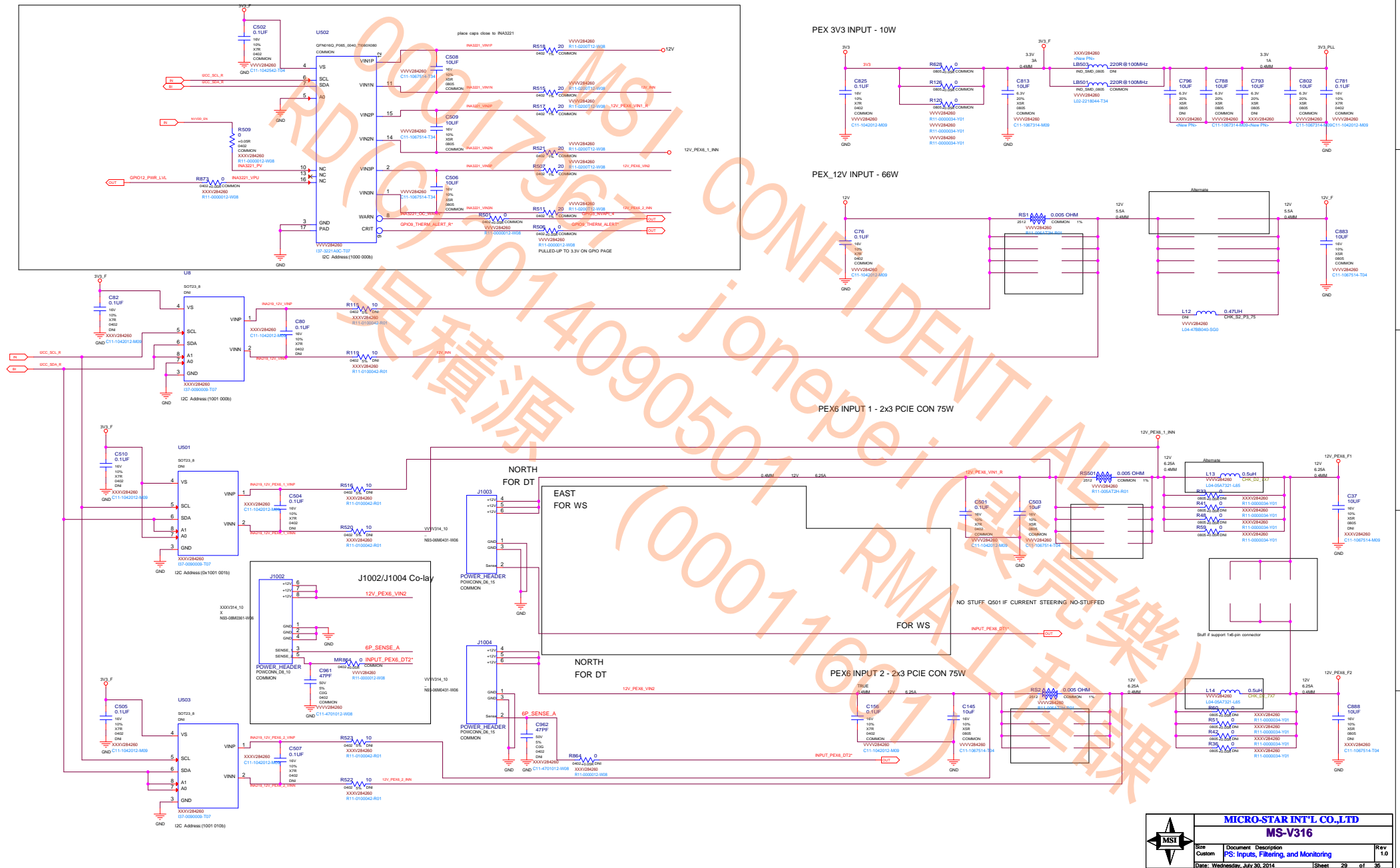
Rev 1.0

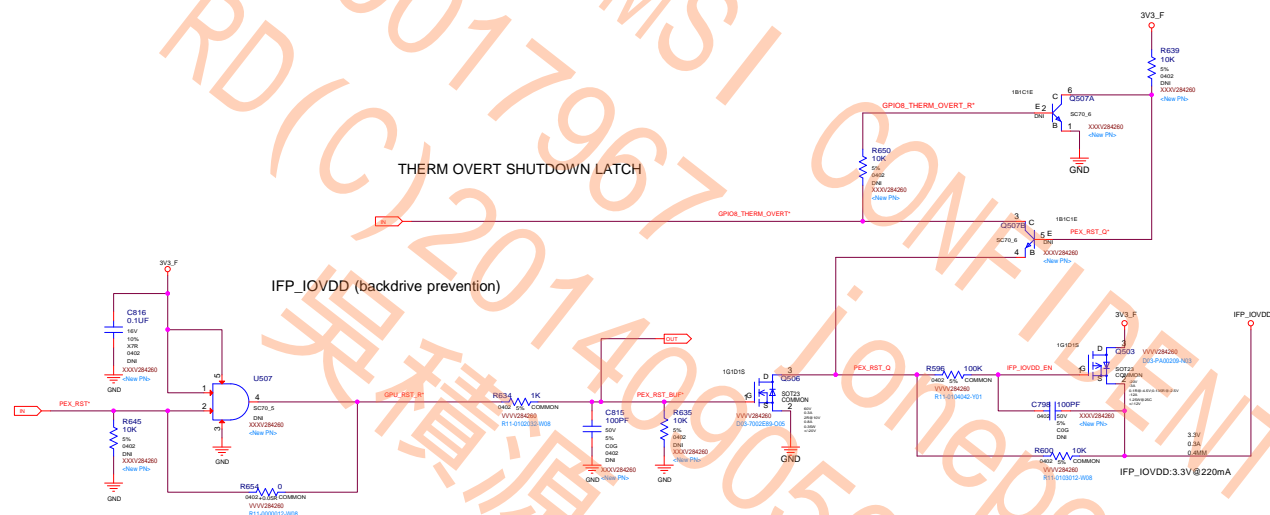
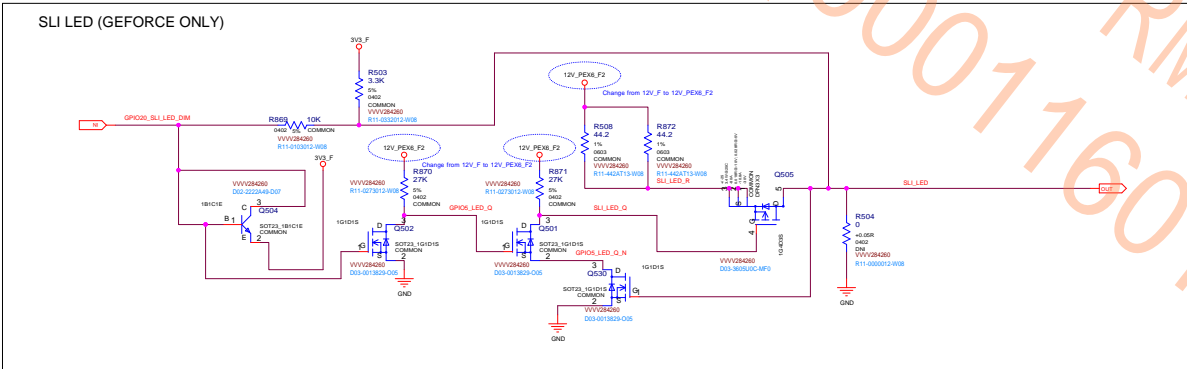
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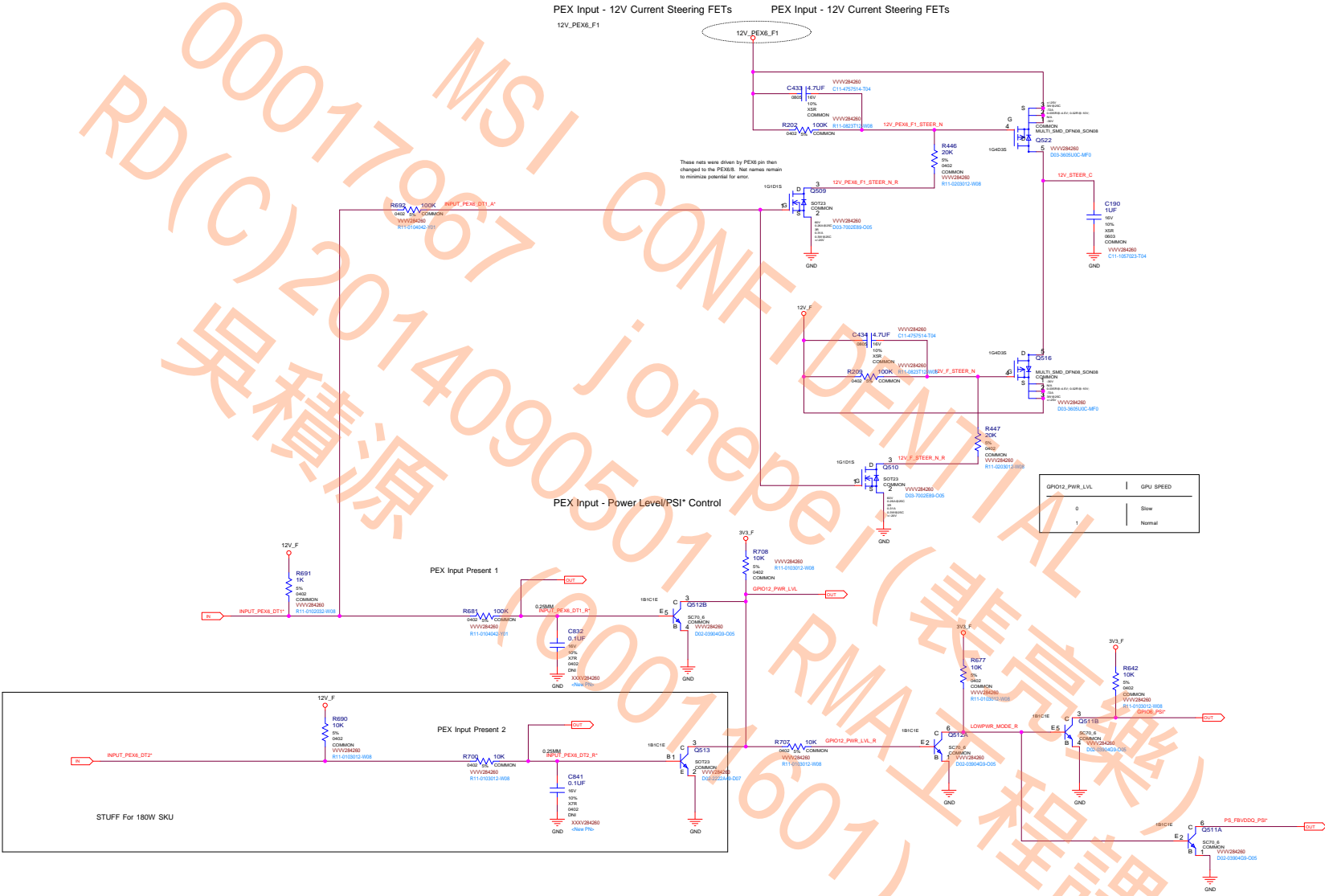

$$V_{o_Typ} = 0.8 \cdot (1 + 1K/3.09K) = 1.059V$$




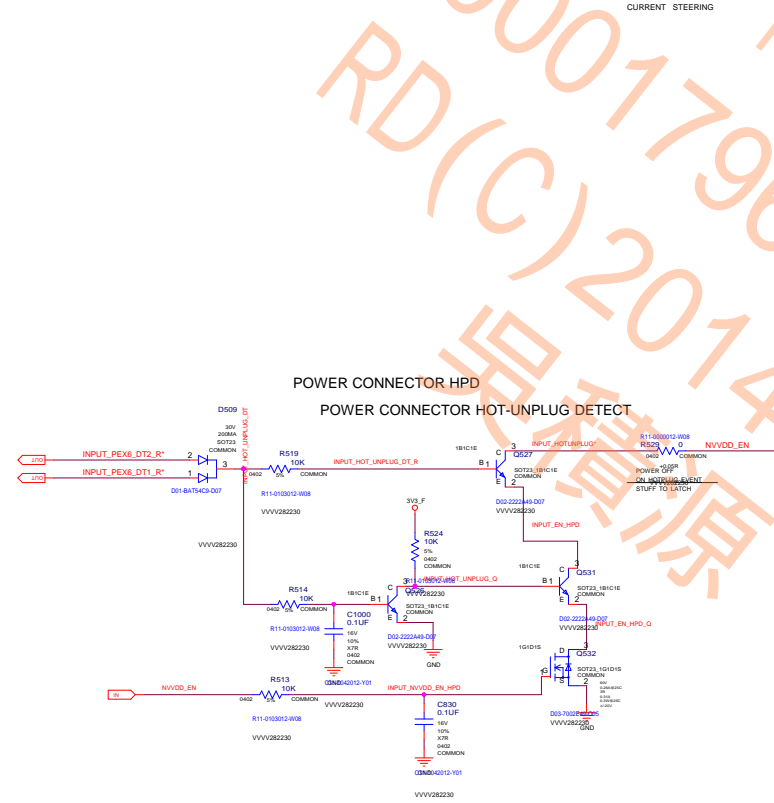


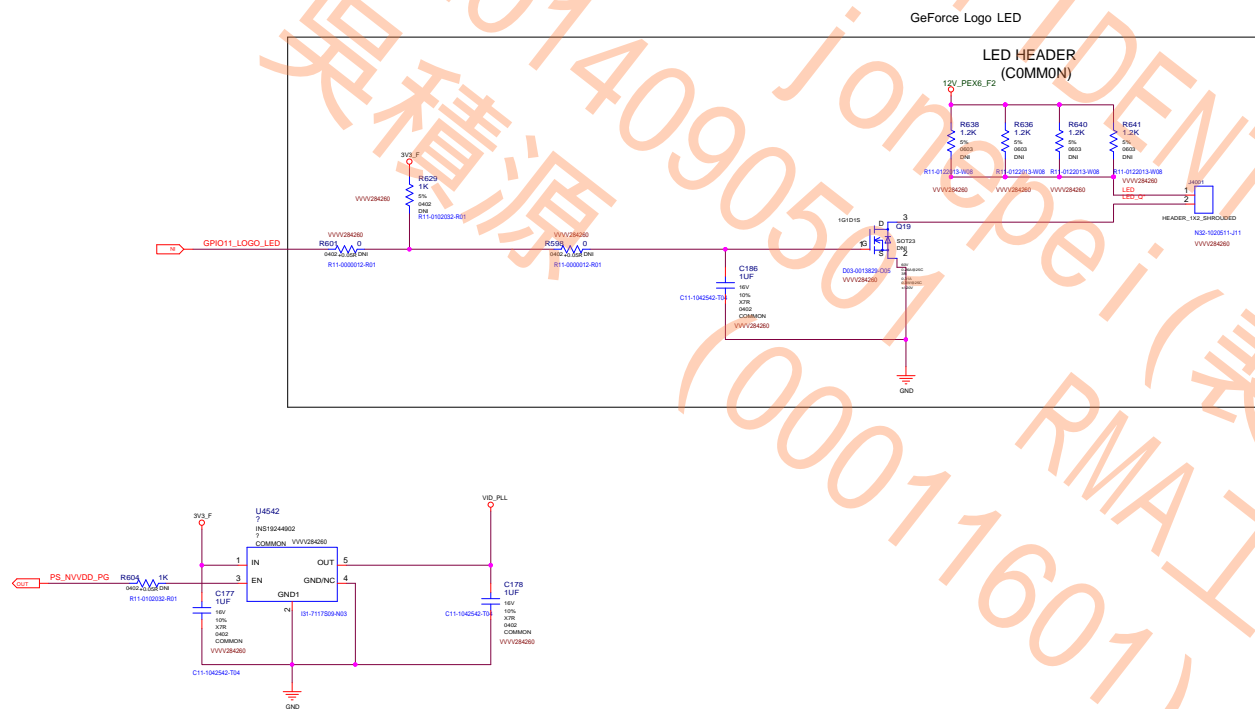


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	Size Custom	Document Description Thermal Shutdown & Light SLI	Rev 1.0
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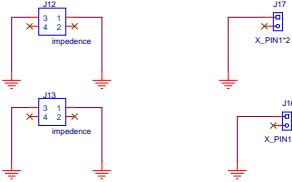
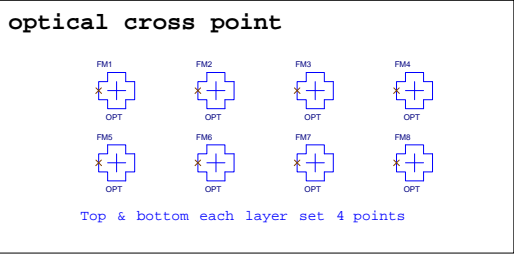
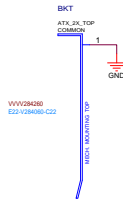


PEX Input - NVVDD Power Sequence

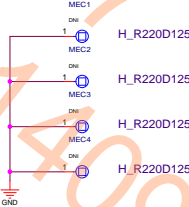




Brackets:



GPU Stiffener:



MOUNTING HOLES FOR HS:

