# MS-8854

## NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X

NVVDD SET TO: 1.67V
FBVDD SET TO: 3.63V
FBVDDQ SET TO: 2.59V

HISTORY REVISION:

X00: Based on P50-A06
- See change list in 149- file.
- Set FBVDDQ=2.59V

P50-A07-X01:

- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

P50-A08:

X04: - Delay PLL_VDD to come up after NVVDD.
X05: - Added 1UF accross R257.
X06: - Removed X04-5 above, added a switcher generated PLL delay option.
- SSENA cap for 2nd SW changed to 1UF.
- A05 Si, NVVDD=1.52V

P50-A09:

X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.
X03: - Added option to pull up power good to 12V
ECO1235: - Changed R841 PU to 10K (from 4.7K)

P50-A10: Removed unintended shorts between the analog ground and the digital ground (layout affected only).

P50-A11: Isolate analog and chassis GND from the main digital GND.
Generate clean 3.3V onboard (3.3VL), used on TV, TMDS and DAC/PLL.
Added 100R resistor on each of the lower FET in series with 680pf.
Removed Shunt Regulator TL431 used previously for external TMDS.
RGB filters are now back to P50-A09 style.
Removed SLI connector.
Added Linear bypass option resistor.
Reference PVCC1 and PVCC2 filtering caps to PGND pin (digital GND).
All plane bridge "X" components will be initially stuffed with 0R resistors.
Power Supply power sequencing to remain as P50-A09 style.
X76 is where A11 and B00 are brahced off.
B00 is official after Dell's review.

B00-X01: R241 and R242 silkscreens are swapped. The bd may look like R241=NOSTUFF and R242=STUFF (but it's the other way around: BOM is correct).

B00-X02:
Added diff pairs parallel terminations (Res, 0603, 300R)
Populated C897 with 150uF to lower DFP supply noise.

C00: Added 700mA circuit from 5V to 3.3V
No Stuff on 3.3V Power Patch.
Set FBVDD to 3.6V max.

C01 : 1. Added L804 to connect PLL_VDD_SW to FBVDD
2. Changed R259 and R261 connected to PLL_VDD_SW net created, was connected to 3.3VL
3. Added two more ground termination 0-ohm resistors X13 and X14.

**0. TOP PAGE**

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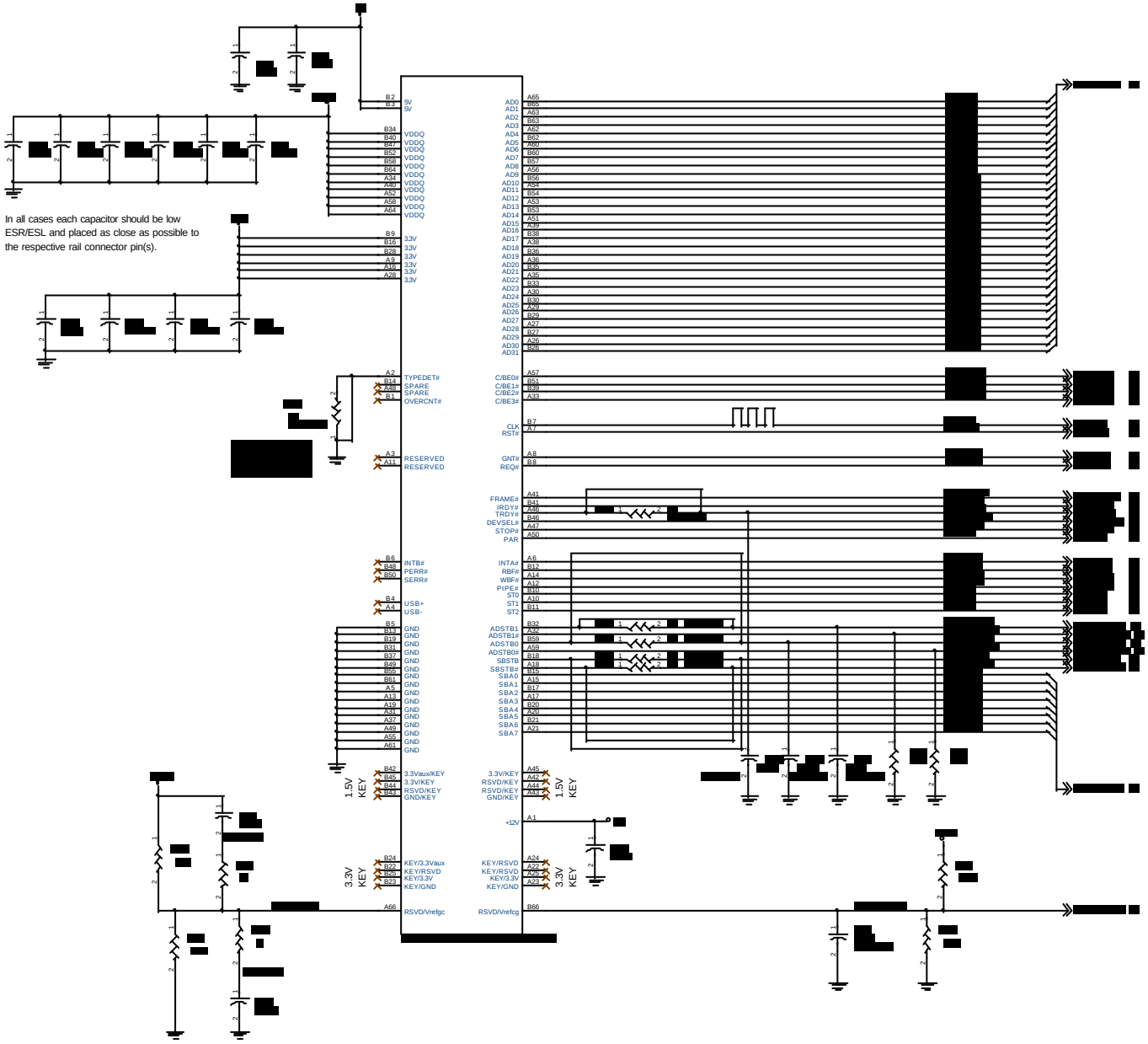
TOP PAGE




# 1.1 BUS I/O

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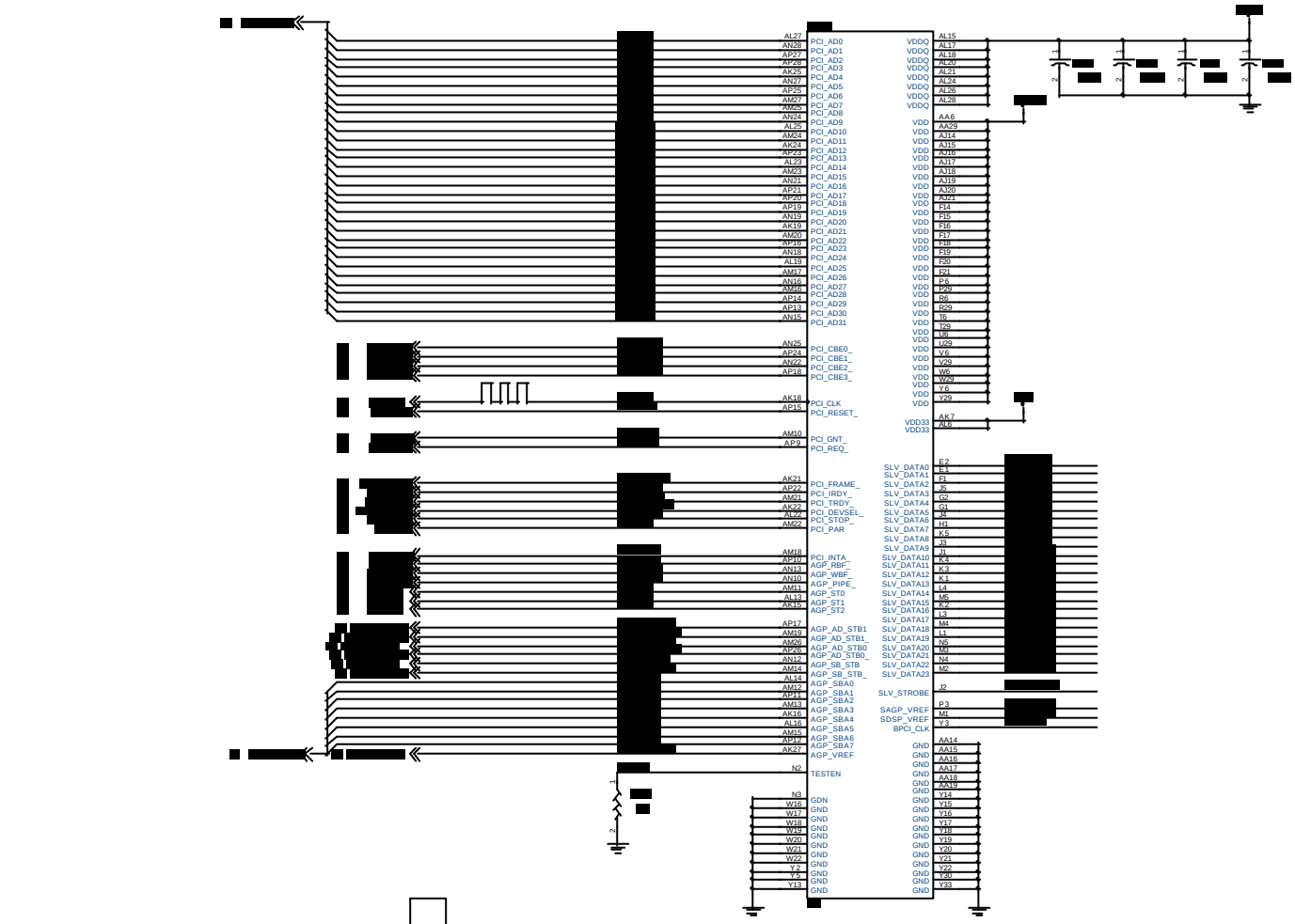
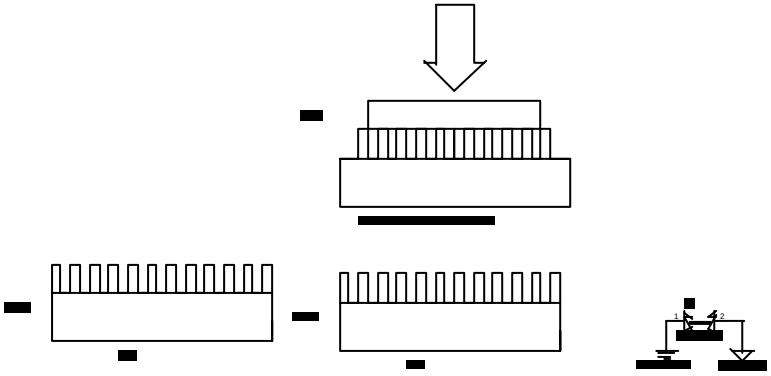
BUS I/0




ROUTE 12V THRU FERRITE PADS.



# 2.1 NV20 HOST

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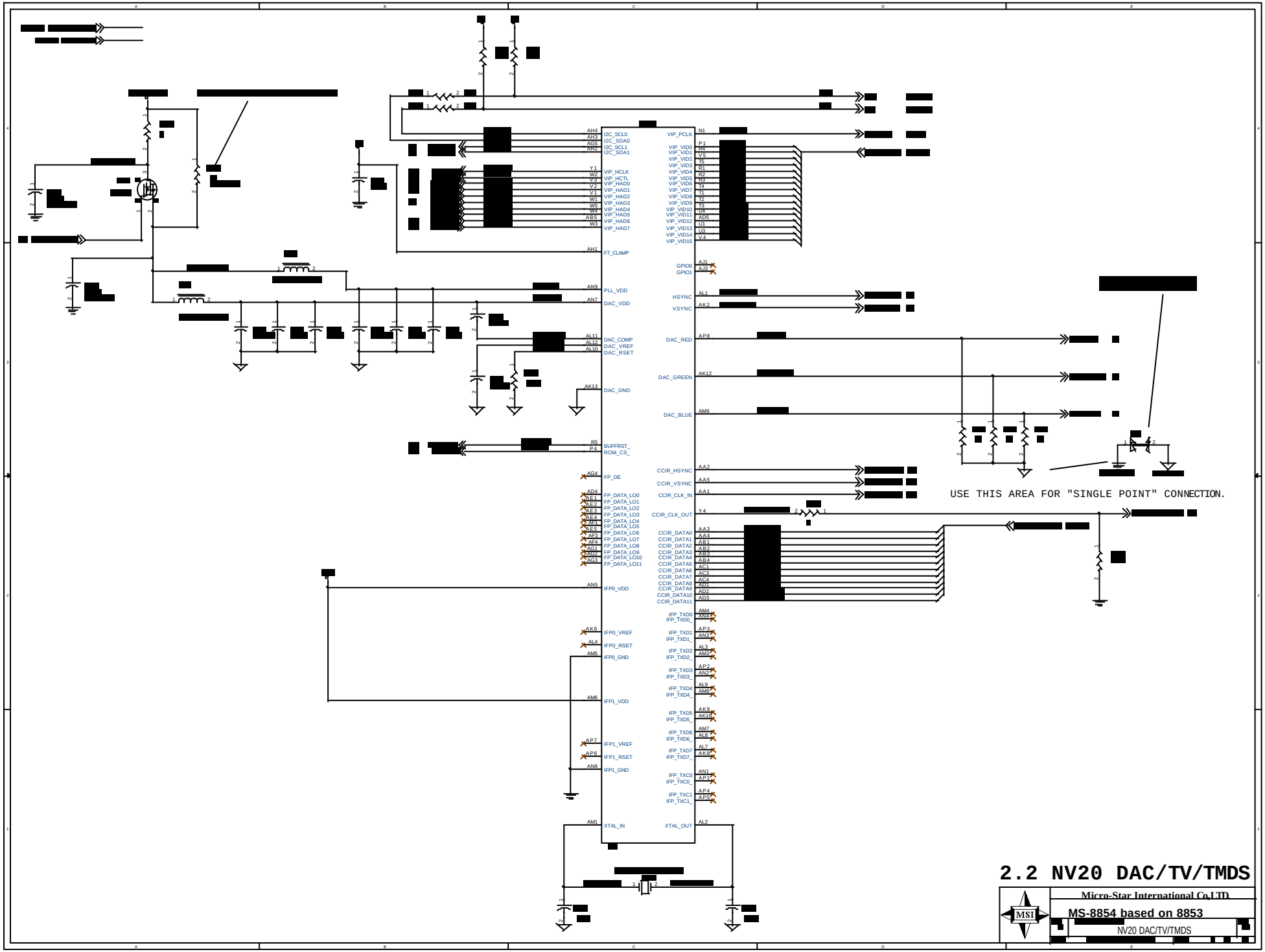
NV20 HOST




# 2.2 NV20 DAC/TV/TMDS

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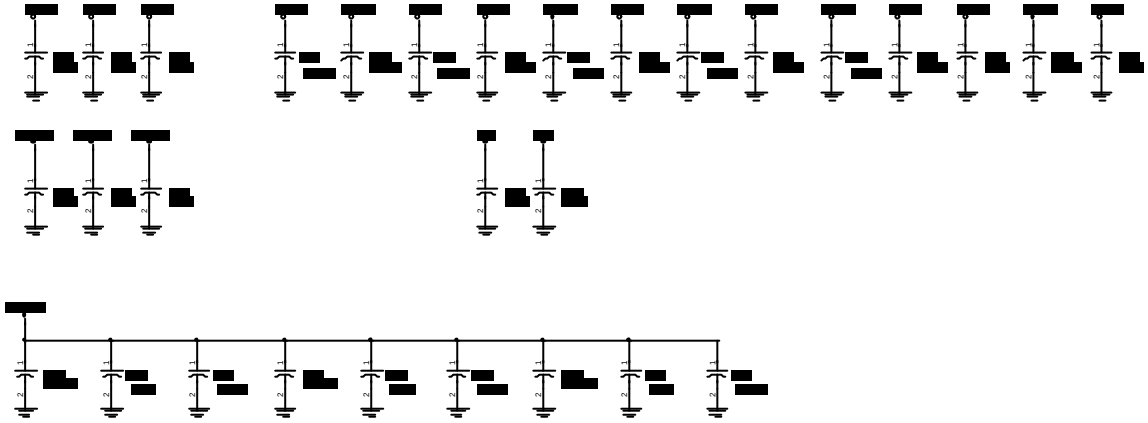
NV20 DAC/TV/TMDS

Use thick (non-impedance controlled) traces on XTALIN/OUT



## 2.3 NV20 DECOUPLING

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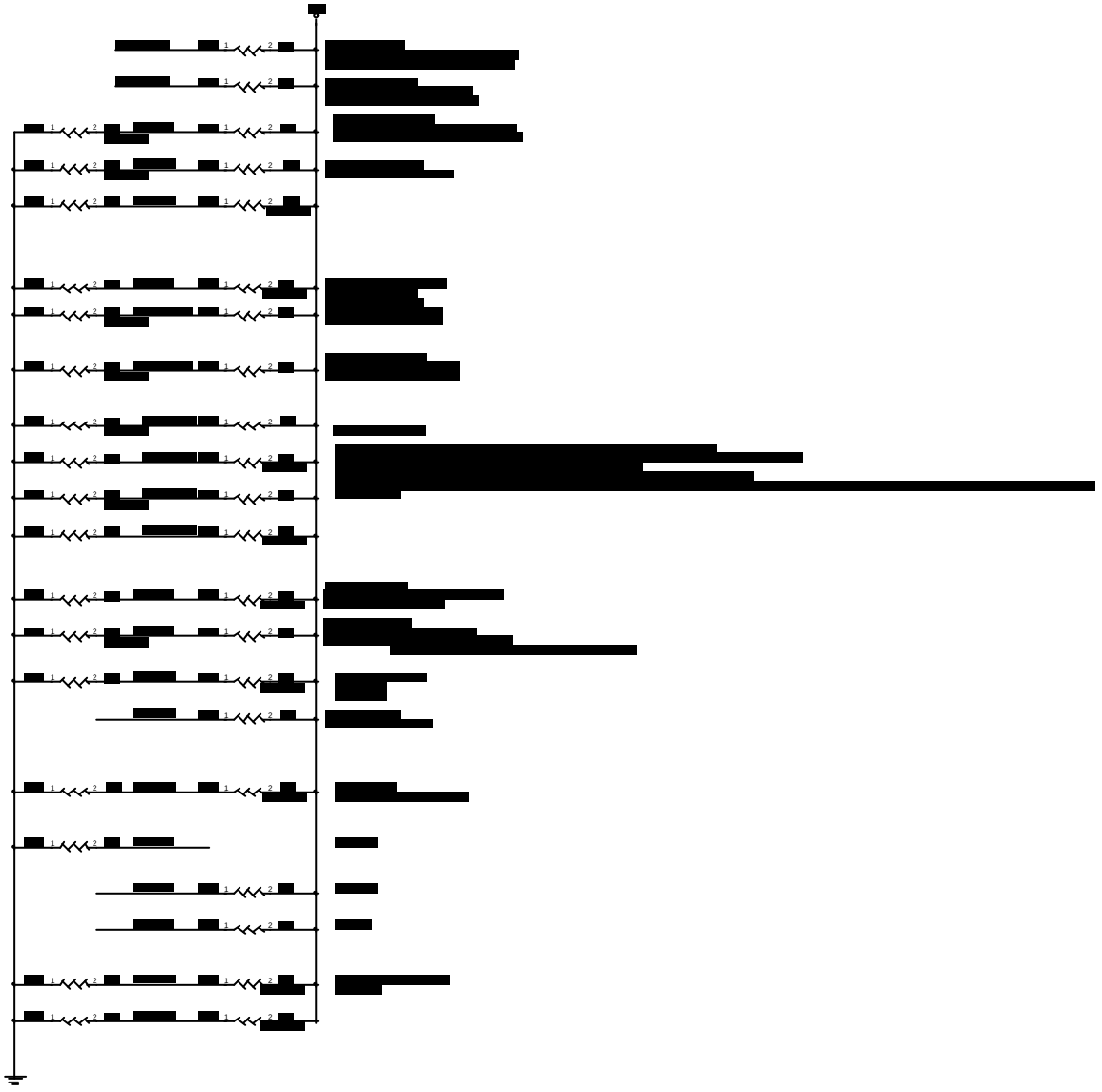
NV20 DECOUPLING



## 2.4 NV20 HOST STRAPS

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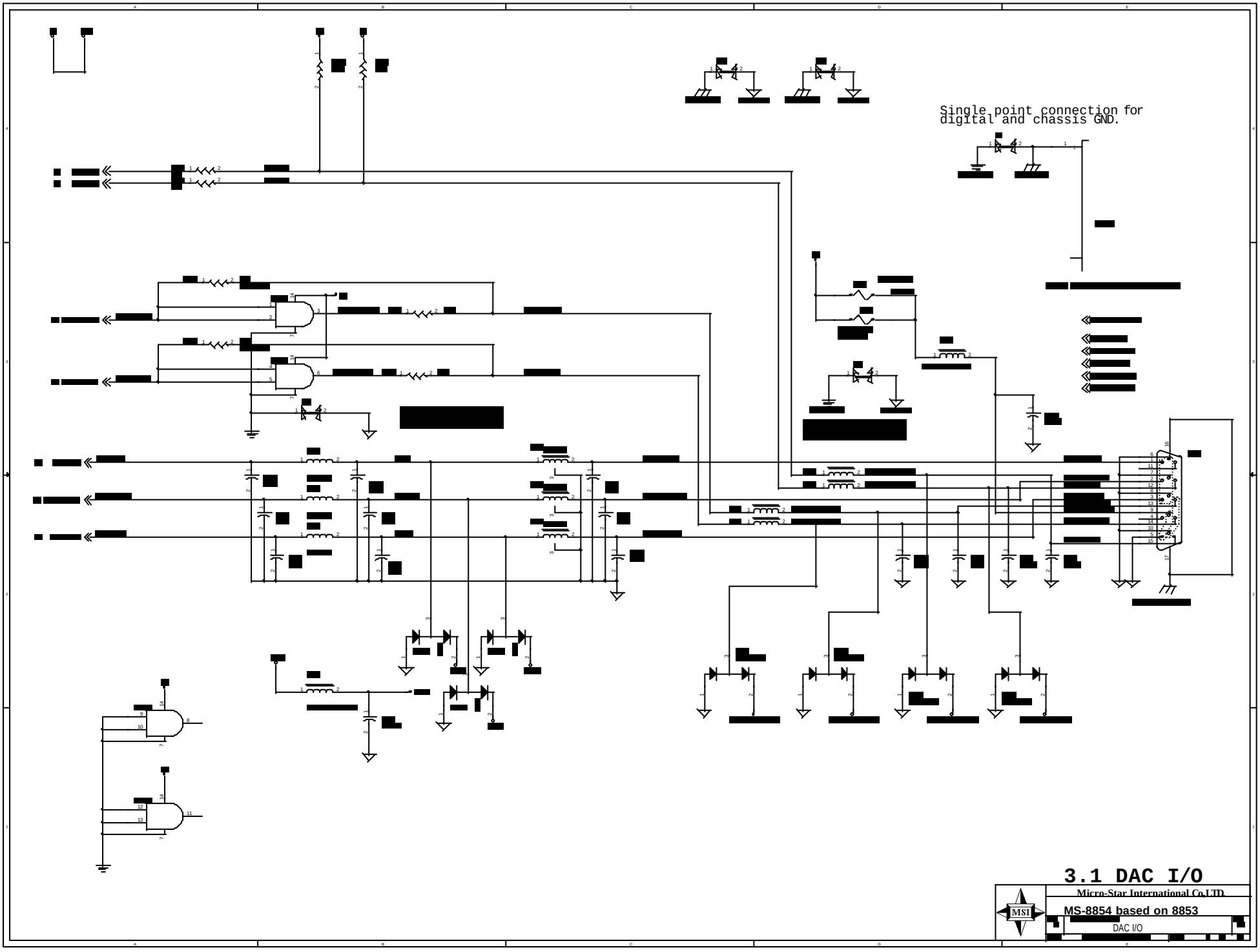
NV20 HOST STRAPS




# 3.1 DAC I/O

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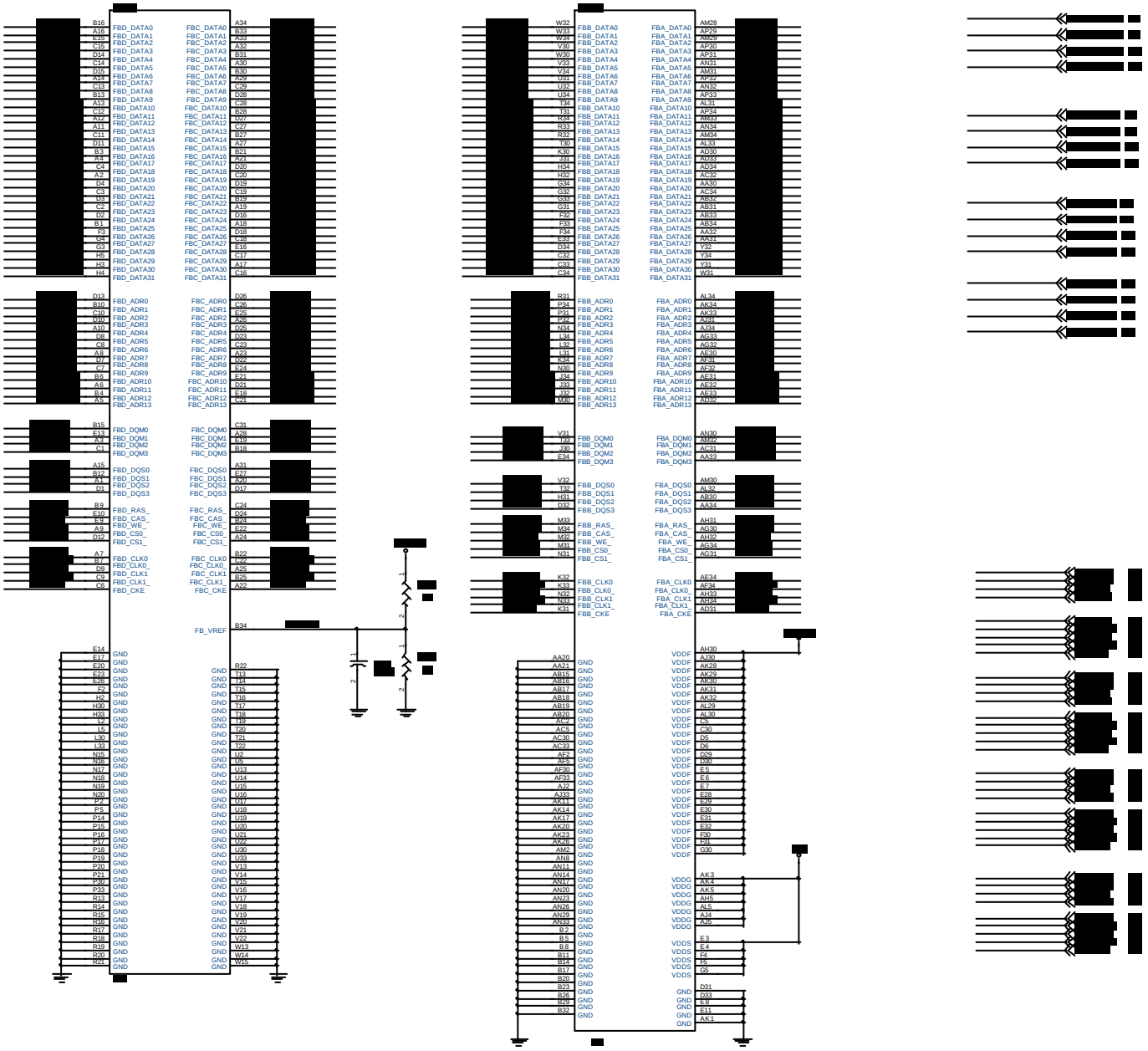
DAC I/O




# 4.1 NV20 FBA/B/C/D

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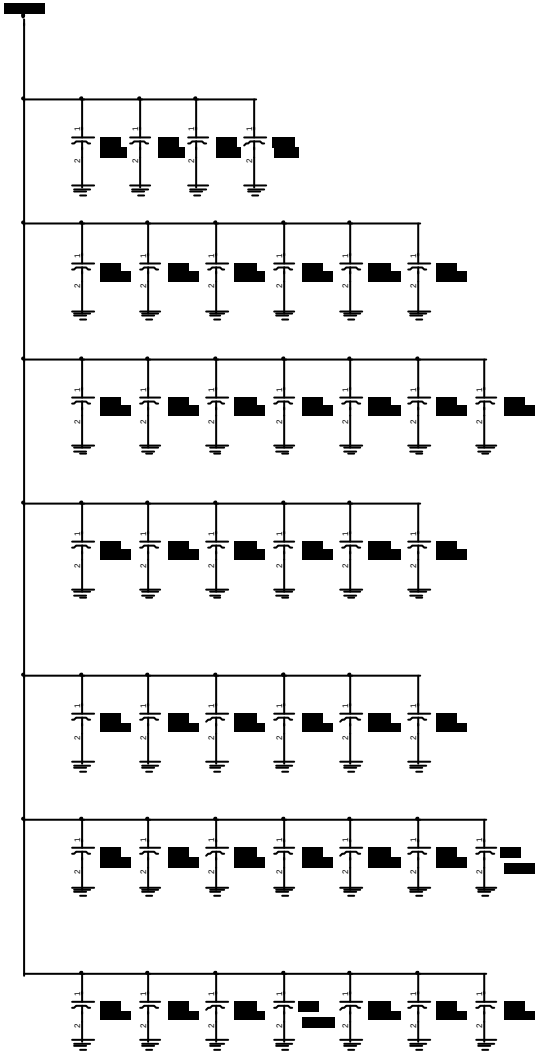
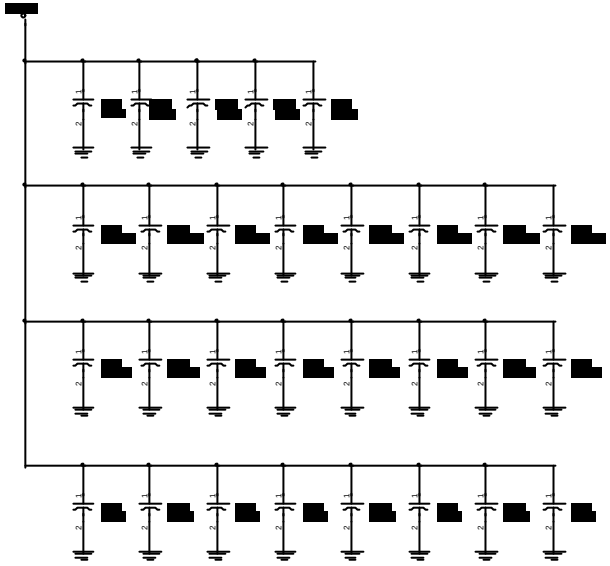
NV20 FBA/B/C/D





## 4.2 FB DECOUPLING 4MX16 SDRAM

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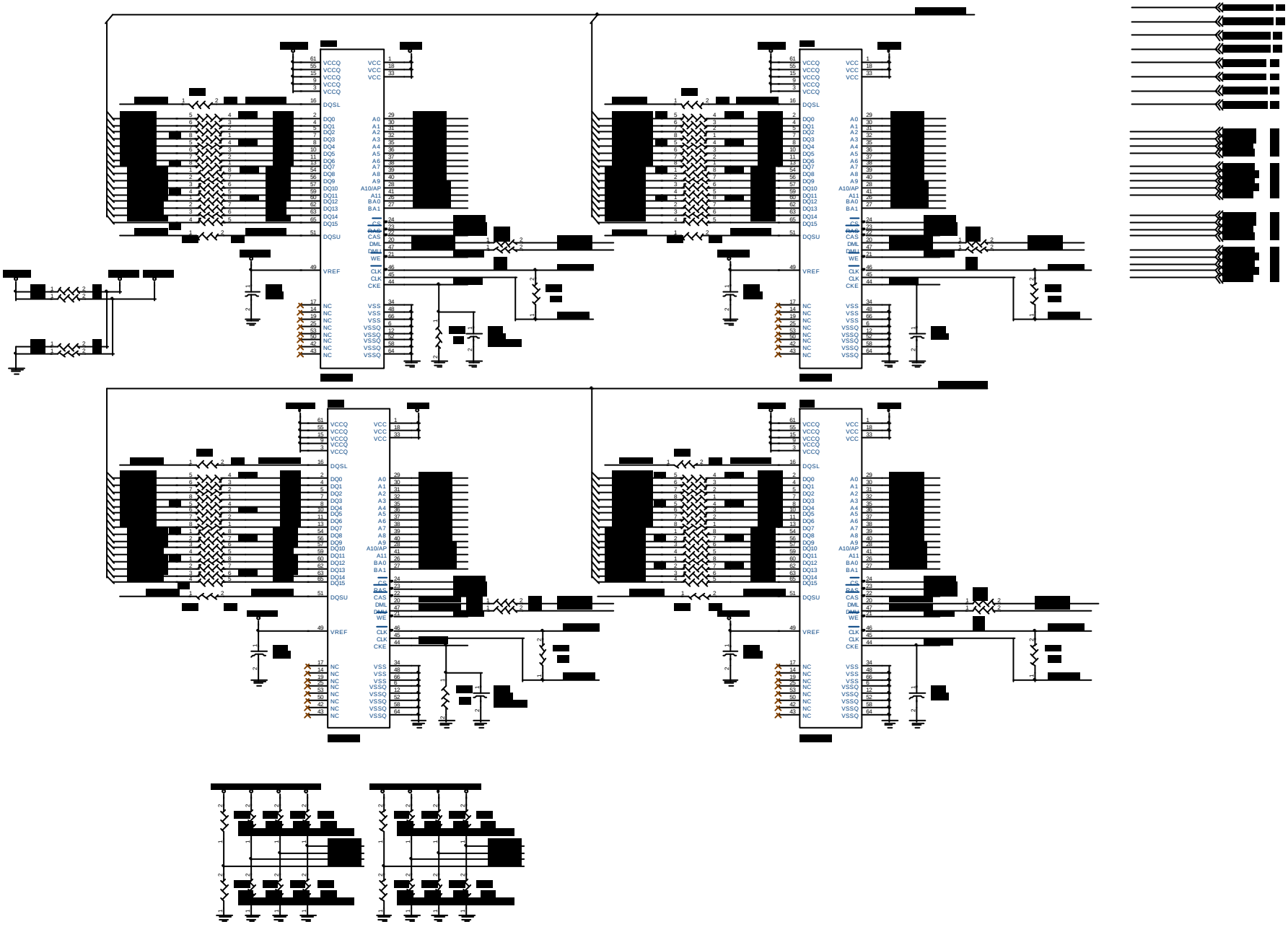
FB DECOUPLING 4MX16 SDRAM



# 4.3 FBA/B DDR 4MX16 SDRAM

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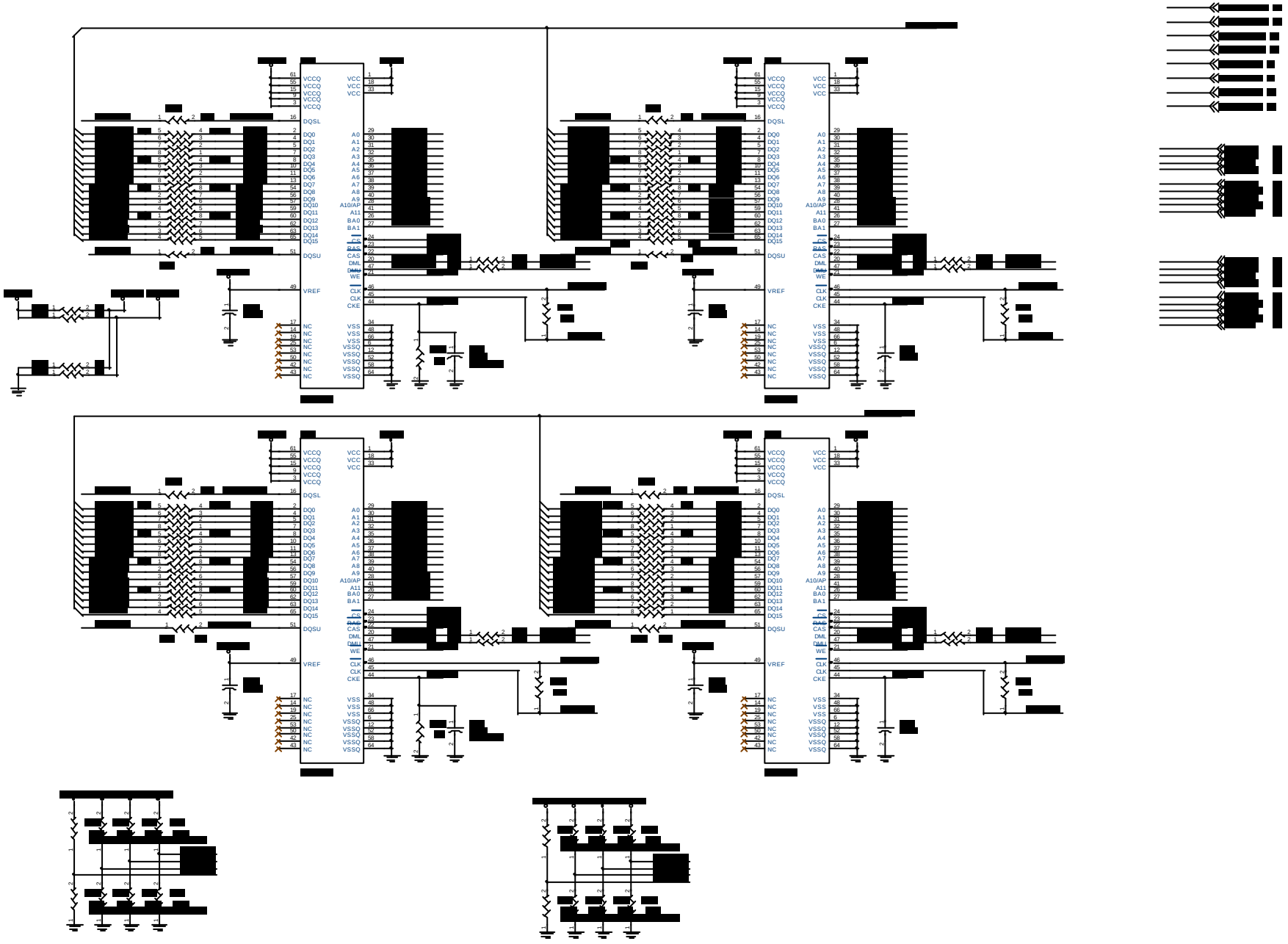
FBA/B DDR 4MX16 SDRAM



# 4.4 FBC/D DDR 4MX16 SDRAM

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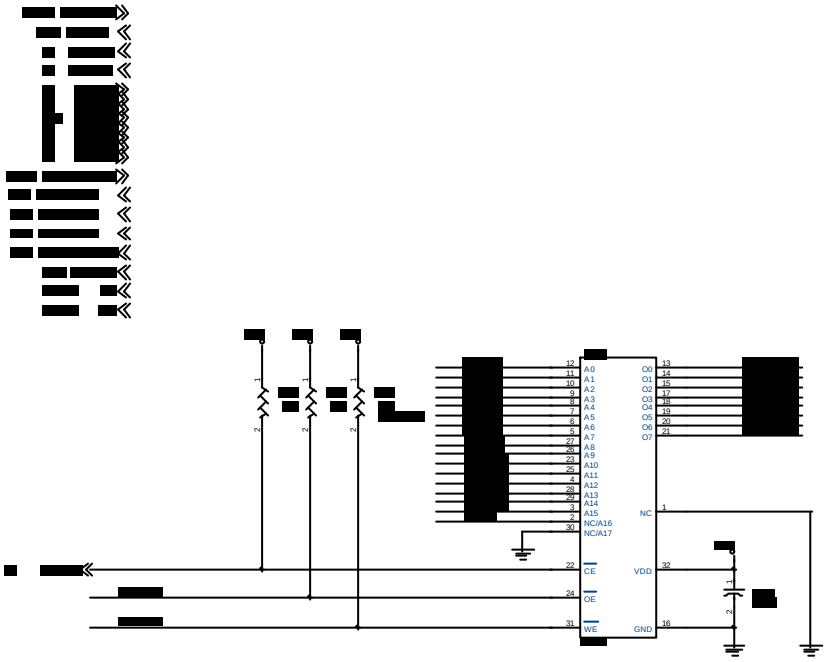
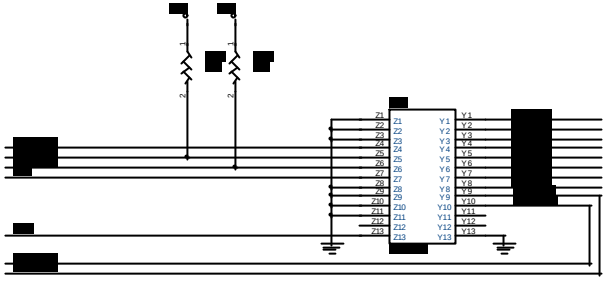
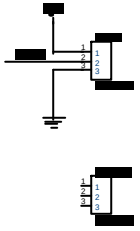
FBC/D DDR 4MX16 SDRAM



Twin BIOS



# 5.1 ROM VIP & VIDEO IF

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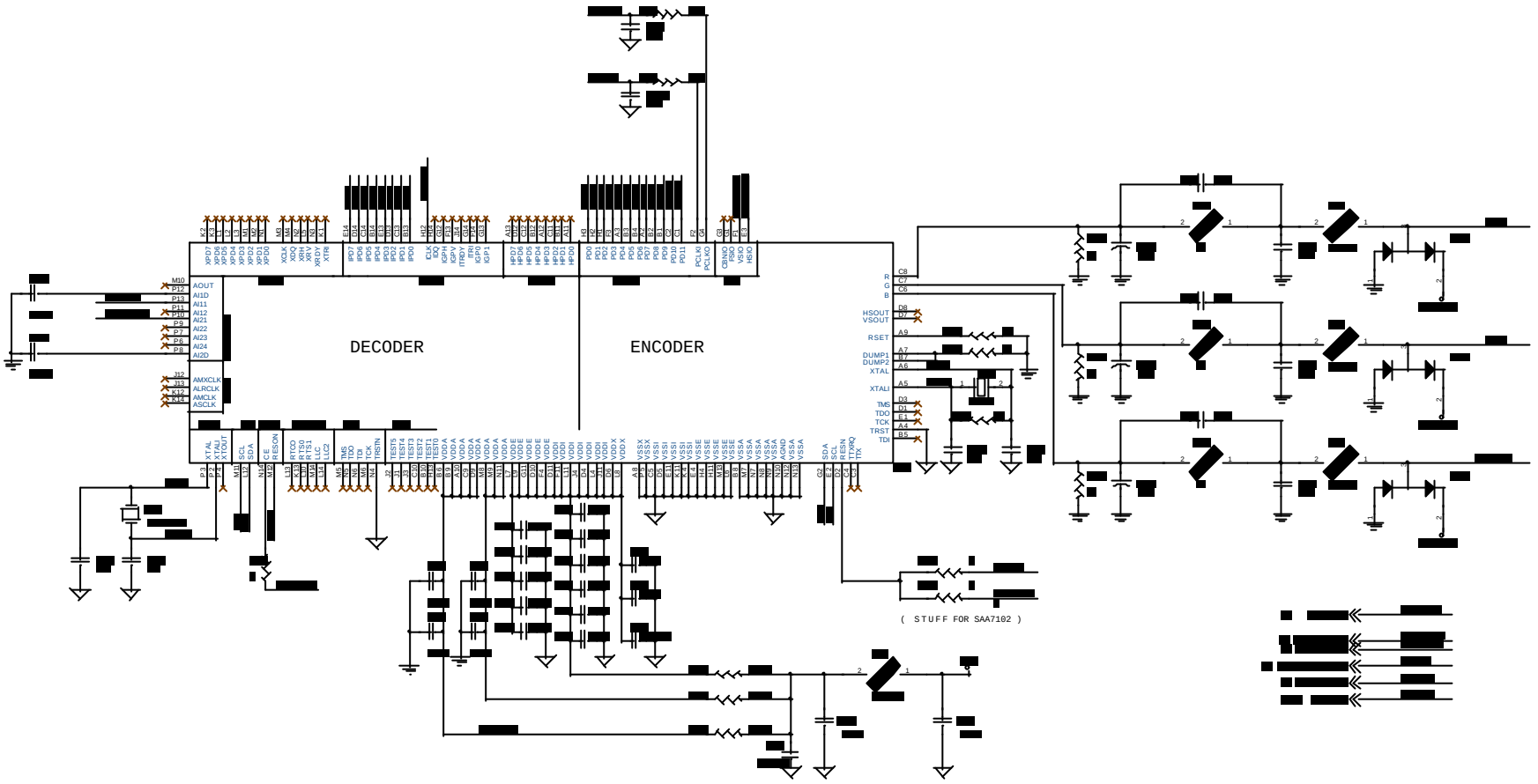
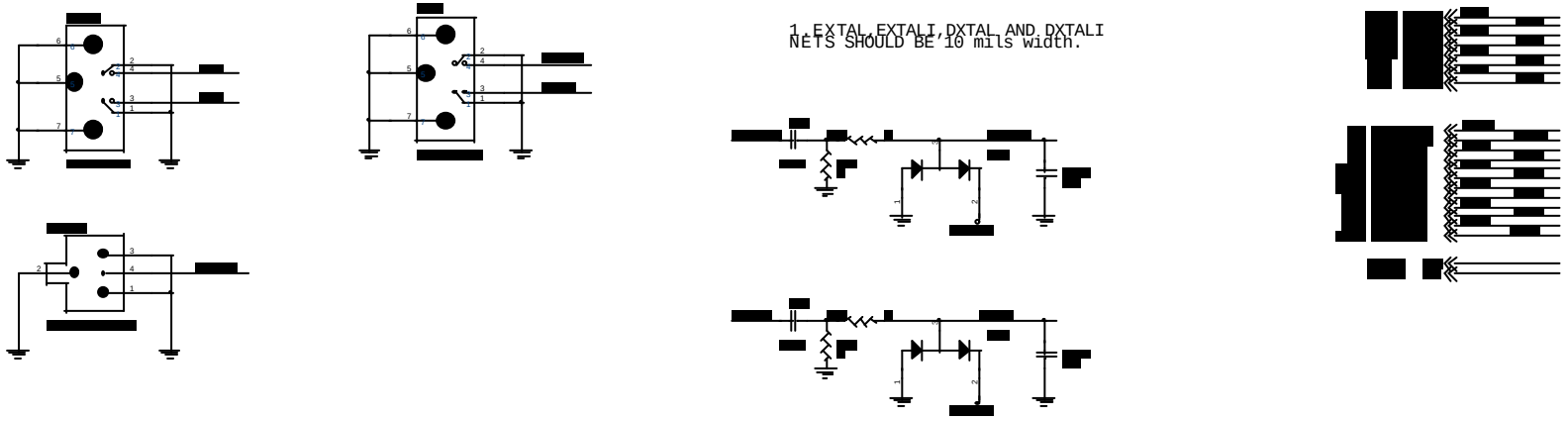
ROM & VIDEO IF




1.EXTAL,EXTALI,DXTAL AND DXTALI NETS SHOULD BE 10 mils width.



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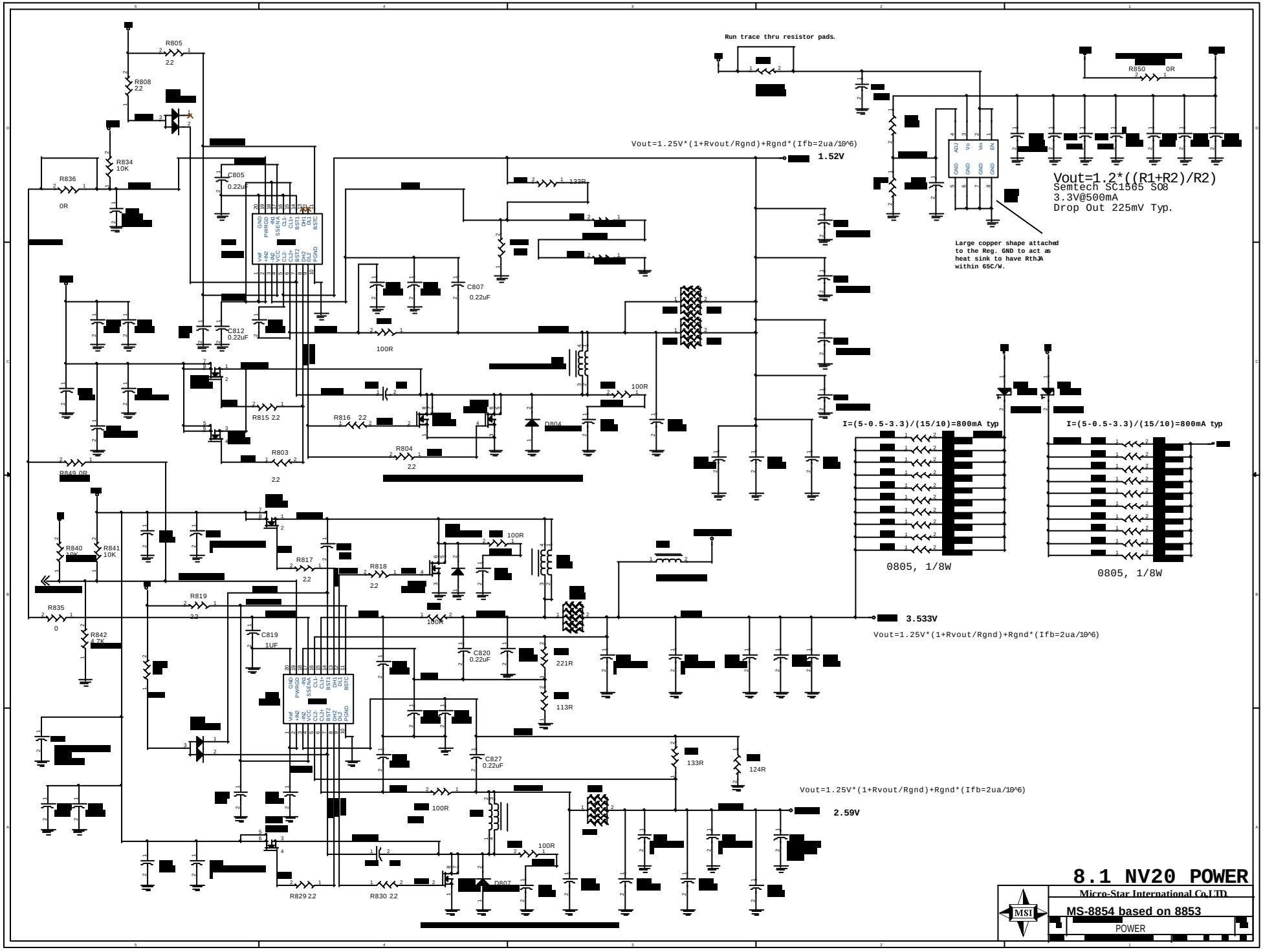
| TV OUT & VIDEO IN | |


Run trace thru resistor pads.
Vout=1.25V*(1+Rvout/Rgnd)+Rgnd*(Ifb=2ua/10^6)
1.52V
Vout=1.2*((R1+R2)/R2)
Semtech SC1565 SO8
3.3V@500mA
Drop Out 225mV Typ.
Large copper shape attached to the Reg. GND to act as heat sink to have RthJA within 65C/W.
I=(5-0.5-3.3)/(15/10)=800mA typ
0805, 1/8W
3.533V
Vout=1.25V*(1+Rvout/Rgnd)+Rgnd*(Ifb=2ua/10^6)
2.59V
8.1 NV20 POWER
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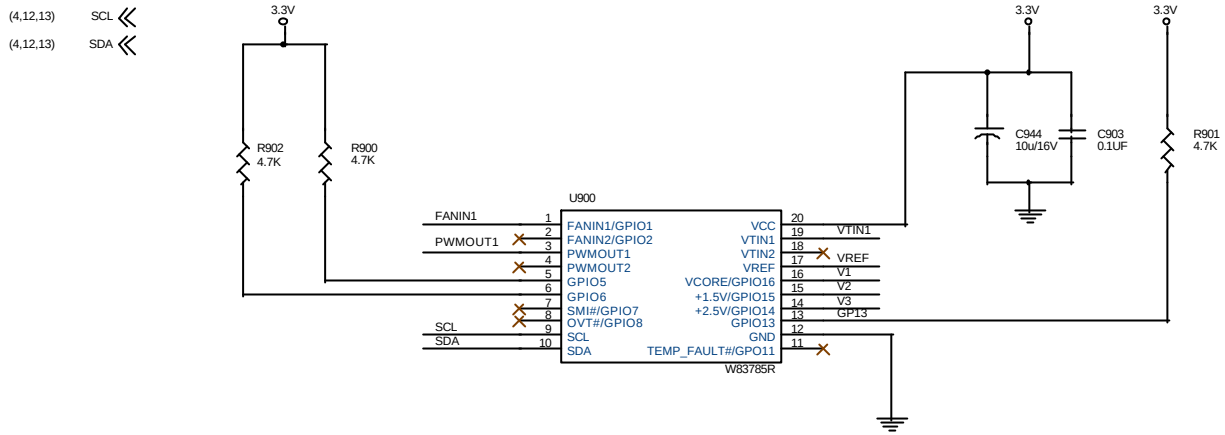
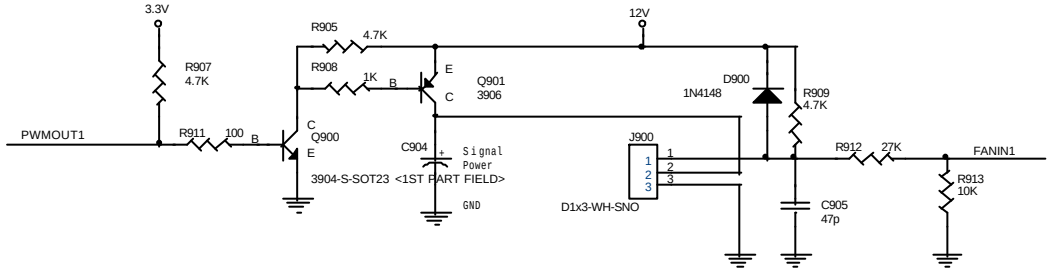
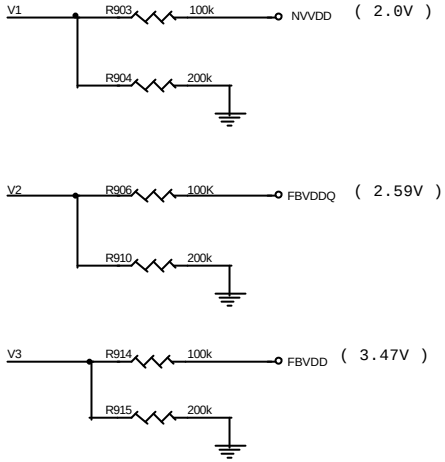
POWER



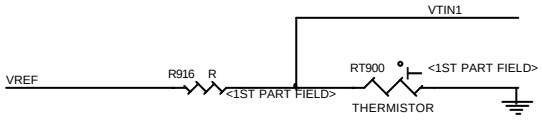




PWM1 Circuit for FAN1 speed Control

FOR 12V FAN




VOLTAGE SENSORING CIRCUIT




TEMPERATURE SENSORING CIRCUIT

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| Size B | Document Number H/W MONITOR | Rev 0A |
| Date: Sunday, October 28, 2001 | Sheet 15 of 15 | |