P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4X

PCI DEVICE ID 0X0=0X171 FOR NV17-128D.

HISTORY:

X00:
Adapted from E63

X39: 1) Show unused inverter U14F.
2) Connect GPIO2 to Backlight On

X49: 1) Show Stuff Option and explanation for GATEBS and GATE12V. Add R263 to GATEBS stuff option.

X55: 1) Disabled current limit circuits on SC1176. Removed C241, C244, R261, R267, and grounded U13.6 and U13.15
2) Corrected strap options to select 27MHz crystal
3) Corrected values for R248 and R250 to produce expected output voltage for U801
4) Corrected power supply name on J10.170 to +3.3VRUN
5) Corrected R262 value to 221 ohms 1%
6) Changed LP600 to RP600 10K resistor pack and changed connections for BP001 to PTDn signals
7) Removed USER STRAP option resistors R234-R41
8) Added SS3V:SS5V stuff option to power spread spectrum chip from 5VSUS
9) DAC2 Rset R315 changed to 63.4 ohms 1%
10) Corrected spread spectrum settings for 27 MHz operation

X56: 1) Corrected connection on C152 to +3.3VRUN

X59: 1) Changed footprint for spread spectrum part (U8) to be compatible with Cypress W245 part
2) Rewired spread spectrum part to use GPIOs 0 and 5
3) Added protection FETs to DDC lines

X61: 1) Unswapped I2CSCL and I2CSDAT
2) Changed to I2C2 for LCD EDID detection

X62: 1) Deleted R500-R503
2) Connected GPIO6 to SUS_STAT_L

X64: 1) Changed crystal load caps to 18 pF
2) Added R101 to optionally ground TYPEDET
3) Added D12 protection diode pair for CVBS.

X65: 1) Changed R400 to pullup to +3.3VSUS

X68: 1) Changed R300 and R302 to NO STUFF so I2C1 lines not pulled up

A02:

X71: 1) Swapped input rails for switcher U13.
2) Added R/C across L39 and L40 for improved stability.
3) NO-STUFF C242 and C243.
4) Changed clock terminators to 100 ohms.
5) Changed R891 to 820 ohms 1%

X73: 1) Added L406 to power IFP0PLLVDD from +3.3VRUN

X74: 1) Added inverter for SUS_STAT in NVVDD voltage switch

X76: 1) Connected crystal to GPU instead of SS chip

X78: 1)Grounded power supplies for IFP1

X79: 1) Replaced U16 with 2 discrete FETs, Q9 & Q10
2) Connected J1 pin 22 to 3.3VSUS.
3) Connected gate drive for Q4, Q7, and Q8 to 5VRUN

X80: 1) Add power switches for 5VSUS and 3.3VSUS
2) Relabeled J1 P22 as DDCPOWER

X82: 1) Changed decoupling caps at the AGP connector to the corresponding input rails 3.3VSUSIN and 5VSUSIN.
2) added EMI clip (M7)

X83: 1) Added decoupling caps around the MOSFETs to switch 3.3VSUSIN and 5VSUSIN (C905-C908).
2) Added decoupling cap for 3.3VSUS add J1 (C909).

X84: 1) Changed power switches Q101 and Q102 to P-channel. Remove R149, change R148 pullup to 5VSUSIN.
2) Changed drain connection for Q6 to 3.3VSUSIN.

X87: 1) Added Q103 to isolate NV17 AGPVDDQ rail from system AGPVDDQ rail
2) Added C20 and C556 EMI caps near clock terminators.
3) Added R153 and R154

X89: 1) Changed R400 to 3.3K, and R285 to 100 ohms and marked as NO_STUFF

A03:

X92: 1) Corrected connection of Q9 to FB2
2) Change value of R262 to 243 ohms 1% to set FBVDD to 2.58V

X01: 1) Added linear LDO regulators for suspend operation

X02: 1) Added R278 bypass option for Q11

X03: 1) Added R279-282 gate pull-down resistors for switcher FETs

X05: 1) Added C301 plane stitching cap for XTALIN/XTALOUT layer transition.

X06: 1) Changed voltage setting resistors (R262 R264) for FBVDD

PAGE OVERVIEW

	STUFF OPTION	MEANING
These 2 are mutually exclusive.	**C3STAT**	C3_STAT_L is the source of AGPSTOP_.
	SUSC3STAT	(SUS_STAT_L or C3_STAT_L) is the source of AGPSTOP_.
	TRIMVREFCG	On-board trim components for AGPVREFCG
	CLKTERM	Differential FB clock terminators.
	ALIN	Linear regulator U801 and associated components for analog 3.3V or GPU 2.8V.
These 2 are mutually exclusive.	**A33LIN**	U801 output to analog 3.3V
	A33SUS	Analog 3.3V derived directly from 3.3VSUS
	GPU33	GPU 3.3V derived directly from 3.3VSUS
	PID	Parallel Panel ID bits
	32MEG	32 Meg frame buffer
	64MEG	64 Meg frame buffer
These 2 are mutually exclusive.	**GATE12V**	Gate drive for high-side FETs set directly to 12V
	GATEBS	Gate drive for high-side FETs derived from bootstrap circuit
	ABIOS	Adapter BIOS
	SBIOS	System BIOS
These 2 are mutually exclusive.	**DESK**	Desktop GPU
	WKSTN	GL GPU

Item\tQty\tRefDes\tDescription\tAssembly\tNVPN\tNotes\tValue\tParam_voltage\tParam_material\tParam_tolerance\tParam_power\tParam_esr\tParam_ripple\tParam_current\tPCB Footprint
{Item}\t{Qty}\t{Reference}\t{Description}\t{Assembly}\t{NVPN}\t{Notes}\t{Value}\t{P_volt}\t{P_mat}\t{P_tol}\t{P_pow}\t{P_esr}\t{P_ripple}\t{P_current}\t{PCB Footprint}

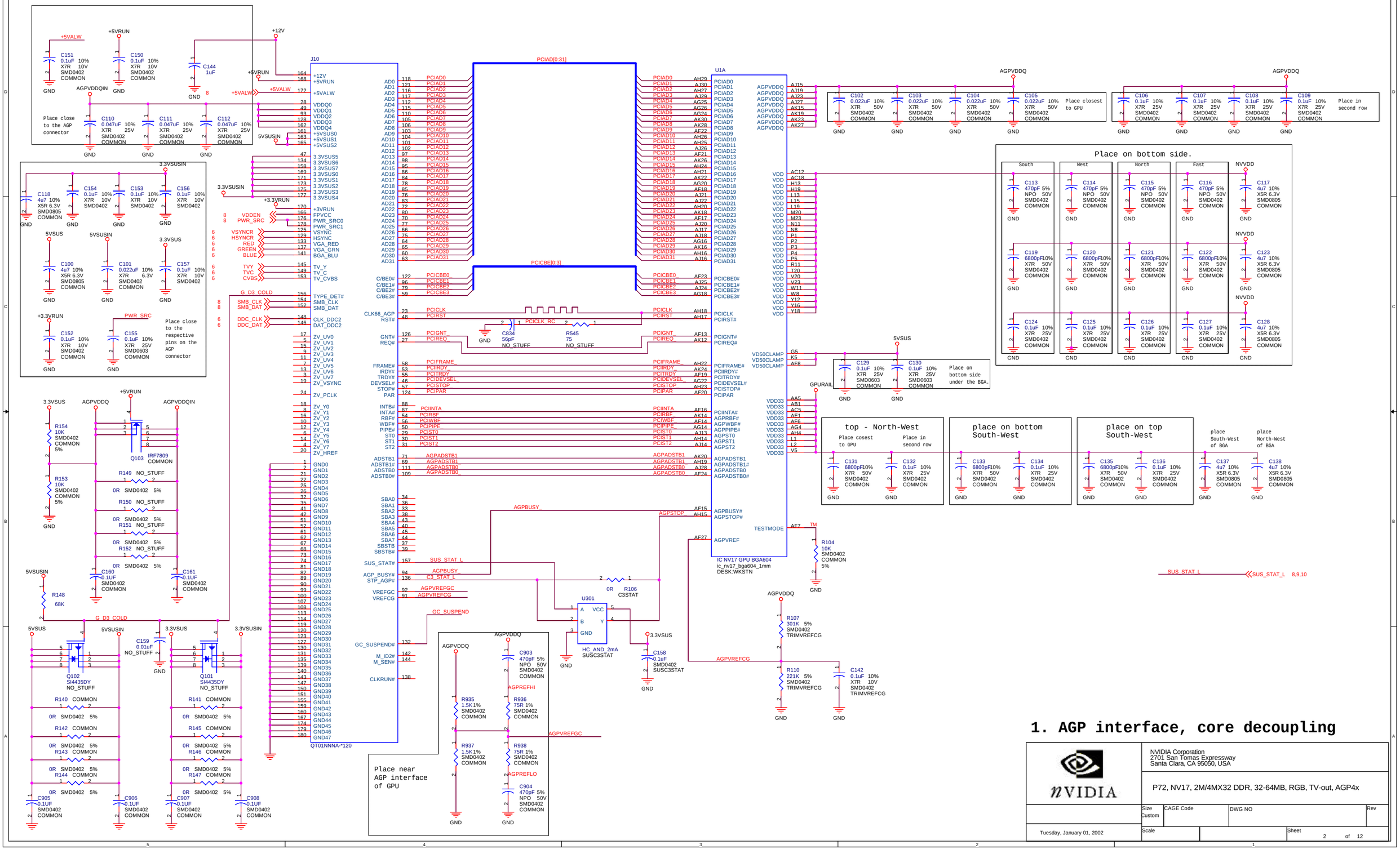
140-10072-0000-xxx
602-10072-0000-xxx

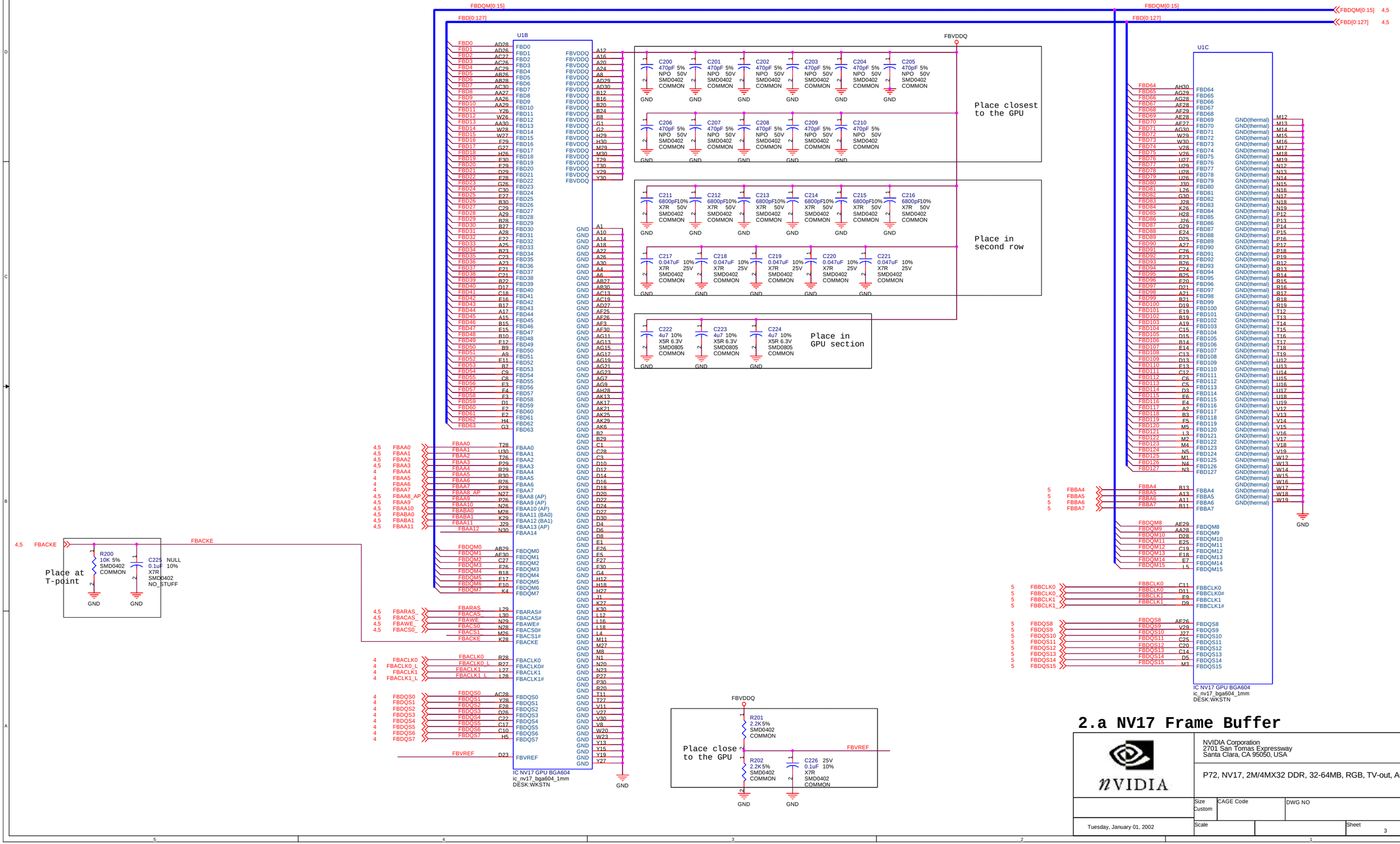
NVIDIA Corporation
3535 Monroe St
Santa Clara, CA 95051, USA

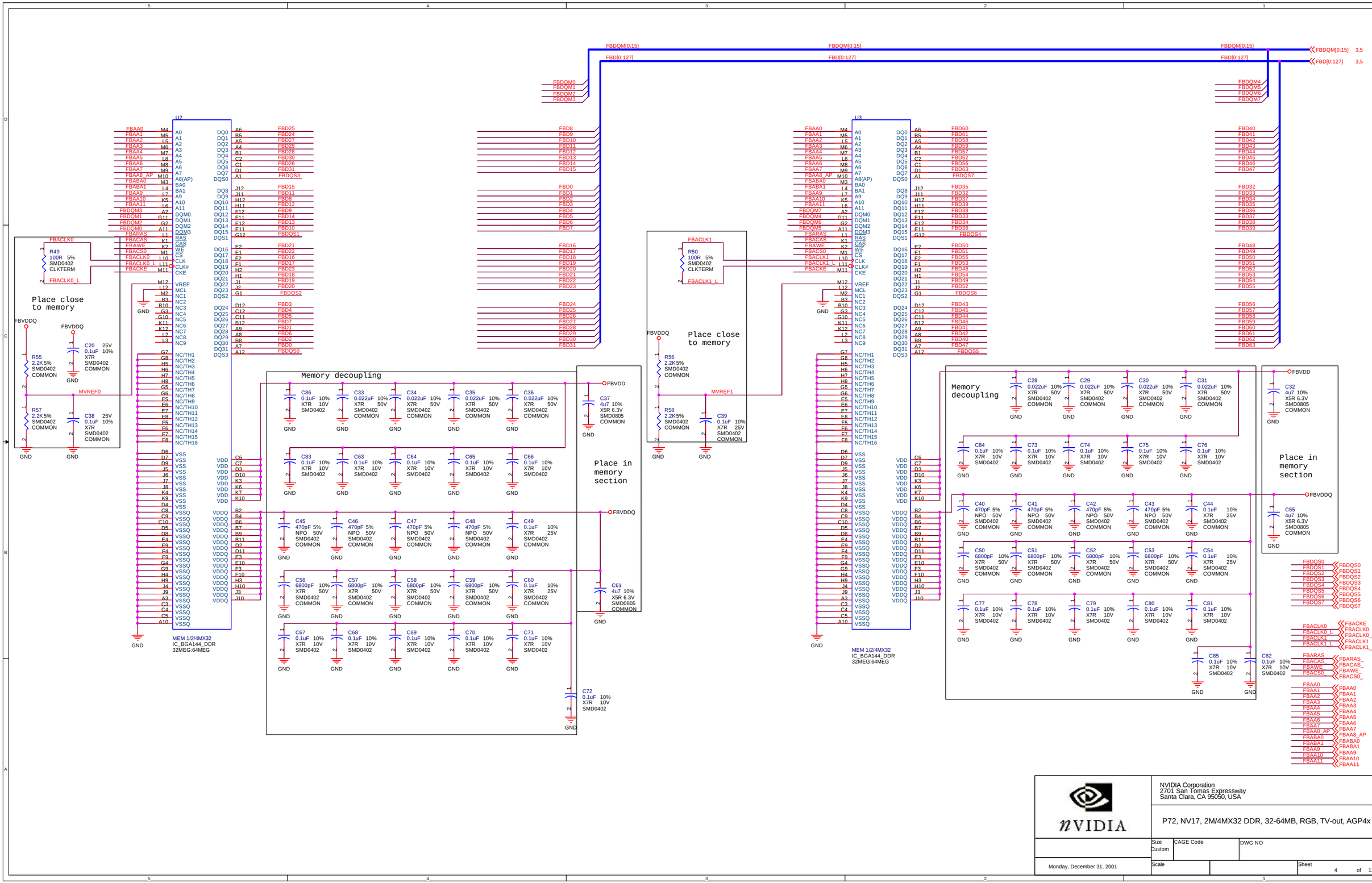
P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4x

Size	CAGE Code	DWG NO	Rev
Custom			

Monday, December 31, 2001 — Scale — Sheet 1 of 12


Place close to the AGP connector
Place close to the respective pins on the AGP connector
Place near AGP interface of GPU
Place on bottom side.
South
West
North
East
Place on bottom side under the BGA.
Place closest to GPU
Place in second row
top - North-West
Place cosest to GPU
Place in second row
place on bottom South-West
place on top South-West
place South-West of BGA
place North-West of BGA
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WKSTN
HC_AND_2mA
SUSC3STAT
QT01NNNA-*120
PCIAD[0:31]
PCICBE[0:3]
SUS_STAT_L
1. AGP interface, core decoupling
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4x
Size Custom
CAGE Code
DWG NO
Rev
Scale
Sheet 2 of 12
Tuesday, January 01, 2002


FBDQM[0:15]
FBD[0:127]
U1B
FBVDDQ
Place closest to the GPU
Place in second row
Place in GPU section
C200 470pF 5% NPO 50V SMD0402 COMMON
C201 470pF 5% NPO 50V SMD0402 COMMON
C202 470pF 5% NPO 50V SMD0402 COMMON
C203 470pF 5% NPO 50V SMD0402 COMMON
C204 470pF 5% NPO 50V SMD0402 COMMON
C205 470pF 5% NPO 50V SMD0402 COMMON
C206 470pF 5% NPO 50V SMD0402 COMMON
C207 470pF 5% NPO 50V SMD0402 COMMON
C208 470pF 5% NPO 50V SMD0402 COMMON
C209 470pF 5% NPO 50V SMD0402 COMMON
C210 470pF 5% NPO 50V SMD0402 COMMON
C211 6800pF 10% X7R 50V SMD0402 COMMON
C212 6800pF 10% X7R 50V SMD0402 COMMON
C213 6800pF 10% X7R 50V SMD0402 COMMON
C214 6800pF 10% X7R 50V SMD0402 COMMON
C215 6800pF 10% X7R 50V SMD0402 COMMON
C216 6800pF 10% X7R 50V SMD0402 COMMON
C217 0.047uF 10% X7R 25V SMD0402 COMMON
C218 0.047uF 10% X7R 25V SMD0402 COMMON
C219 0.047uF 10% X7R 25V SMD0402 COMMON
C220 0.047uF 10% X7R 25V SMD0402 COMMON
C221 0.047uF 10% X7R 25V SMD0402 COMMON
C222 4u7 10% X5R 6.3V SMD0805 COMMON
C223 4u7 10% X5R 6.3V SMD0805 COMMON
C224 4u7 10% X5R 6.3V SMD0805 COMMON
GND
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WKSTN
FBACKE
Place at T-point
R200 10K 5% SMD0402 COMMON
C225 NULL 0.1uF 10% X7R SMD0402 NO_STUFF
FBVDDQ
Place close to the GPU
R201 2.2K5% SMD0402 COMMON
R202 2.2K5% SMD0402 COMMON
C226 25V 0.1uF 10% X7R SMD0402 COMMON
FBVREF
U1C
GND(thermal)
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WKSTN
2.a NV17 Frame Buffer
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4x
Size Custom
CAGE Code
DWG NO
Rev
Tuesday, January 01, 2002
Scale
Sheet 3 of 12


FBDQM[0:15]
FBD[0:127]
U2
MEM 1/2/4MX32
IC_BGA144_DDR
32MEG:64MEG
U3
Place close to memory
Memory decoupling
Place in memory section
FBVDDQ
FBVDD
MVREF0
MVREF1
FBACLK0
FBACLK1
GND
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4x
Monday, December 31, 2001
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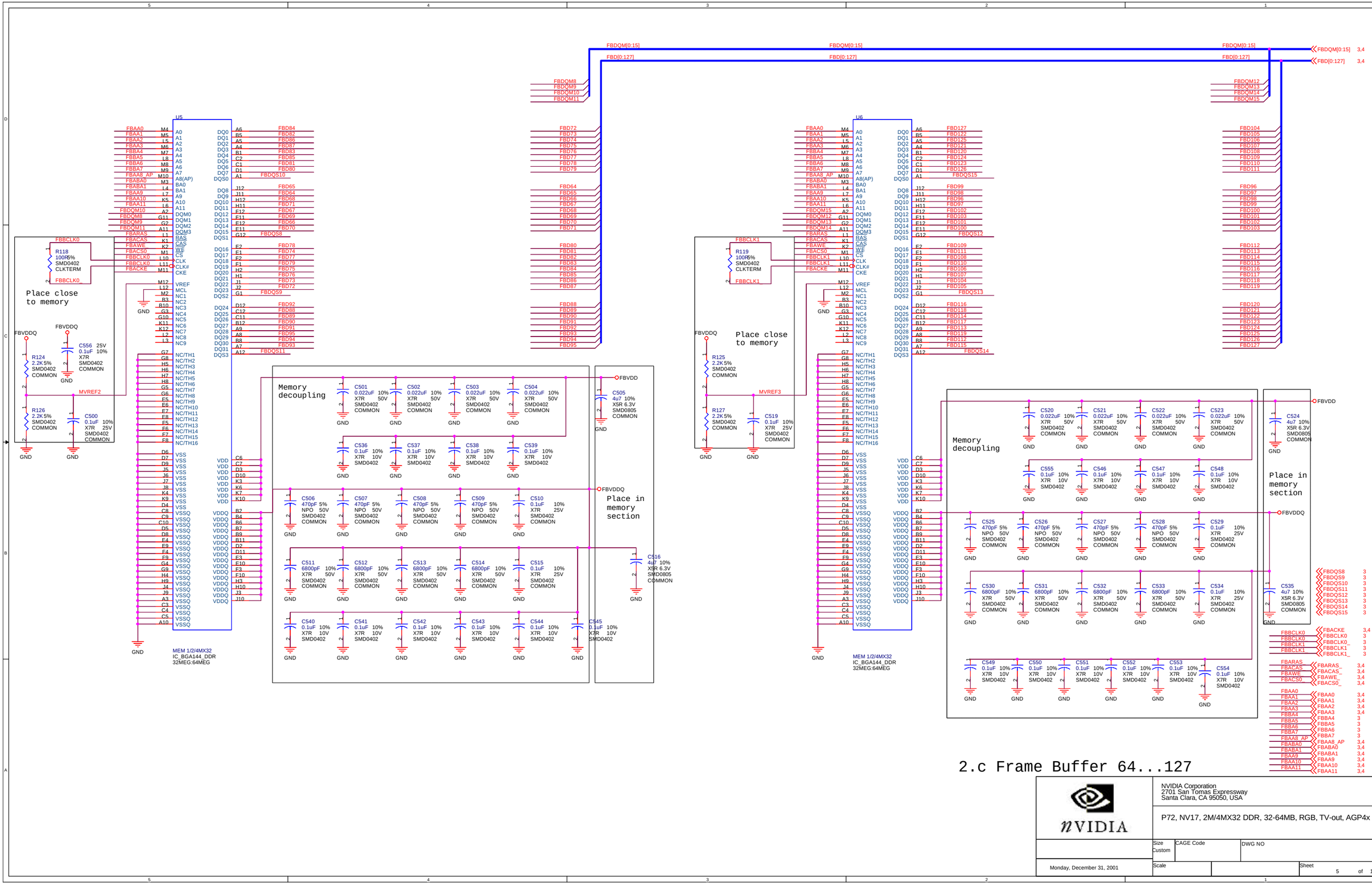
FBDQM[0:15]
FBD[0:127]
U5
MEM 1/2/4MX32
IC_BGA144_DDR
32MEG:64MEG
U6
MEM 1/2/4MX32
IC_BGA144_DDR
32MEG:64MEG
Place close to memory
Memory decoupling
Place in memory section
FBVDDQ
FBVDD
GND
MVREF2
MVREF3
2.c Frame Buffer 64...127
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4x
Monday, December 31, 2001
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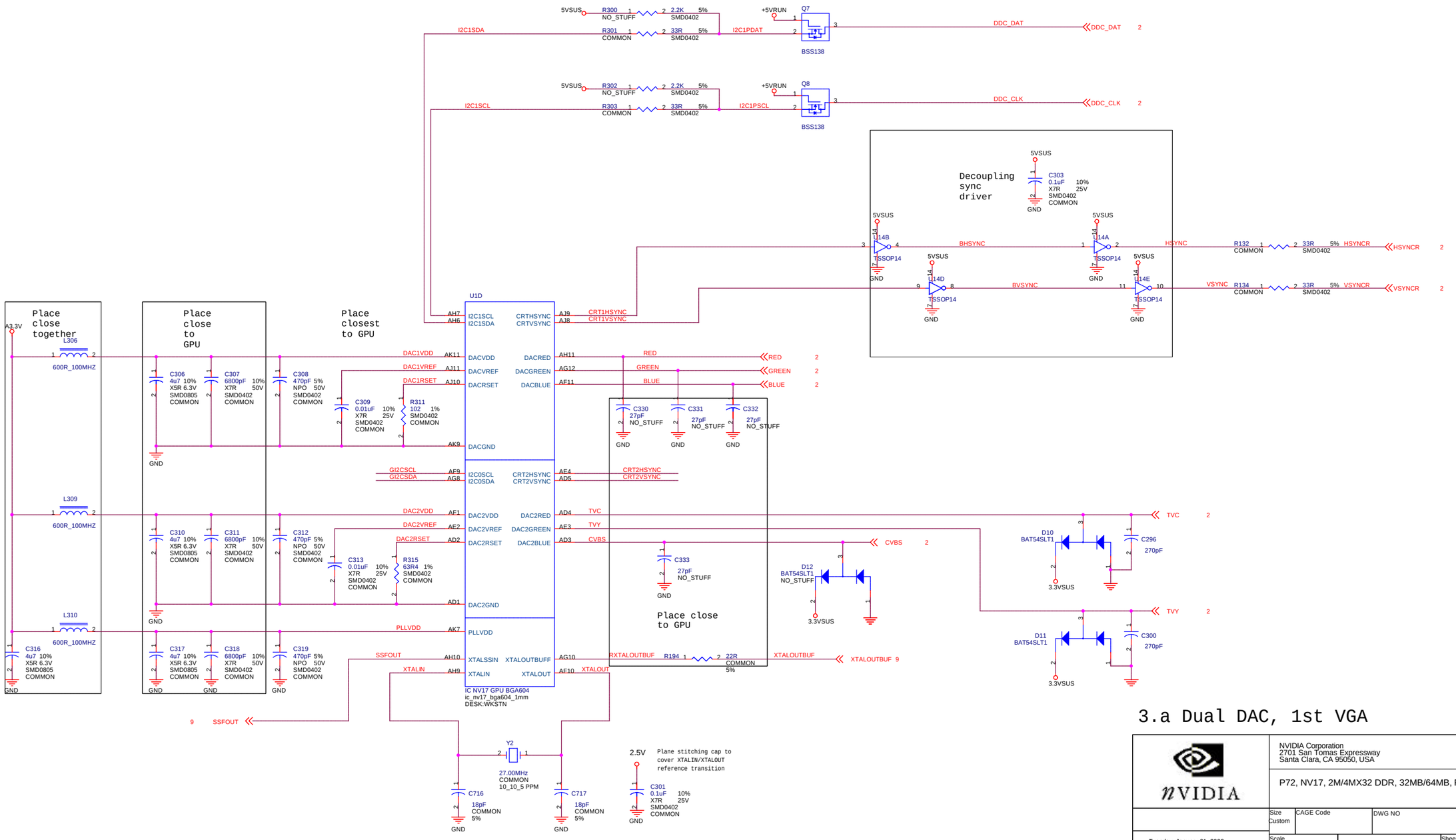

3.a Dual DAC, 1st VGA

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

P72, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, AGP4x

Size	CAGE Code	DWG NO	Rev
Custom			

Tuesday, January 01, 2002 — Scale — Sheet 6 of 12

3.b Dual DAC, 2nd VGA

NVIDIA Corporation
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P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4x

Size	CAGE Code	DWG NO	Rev
Custom			

Monday, December 31, 2001

Scale

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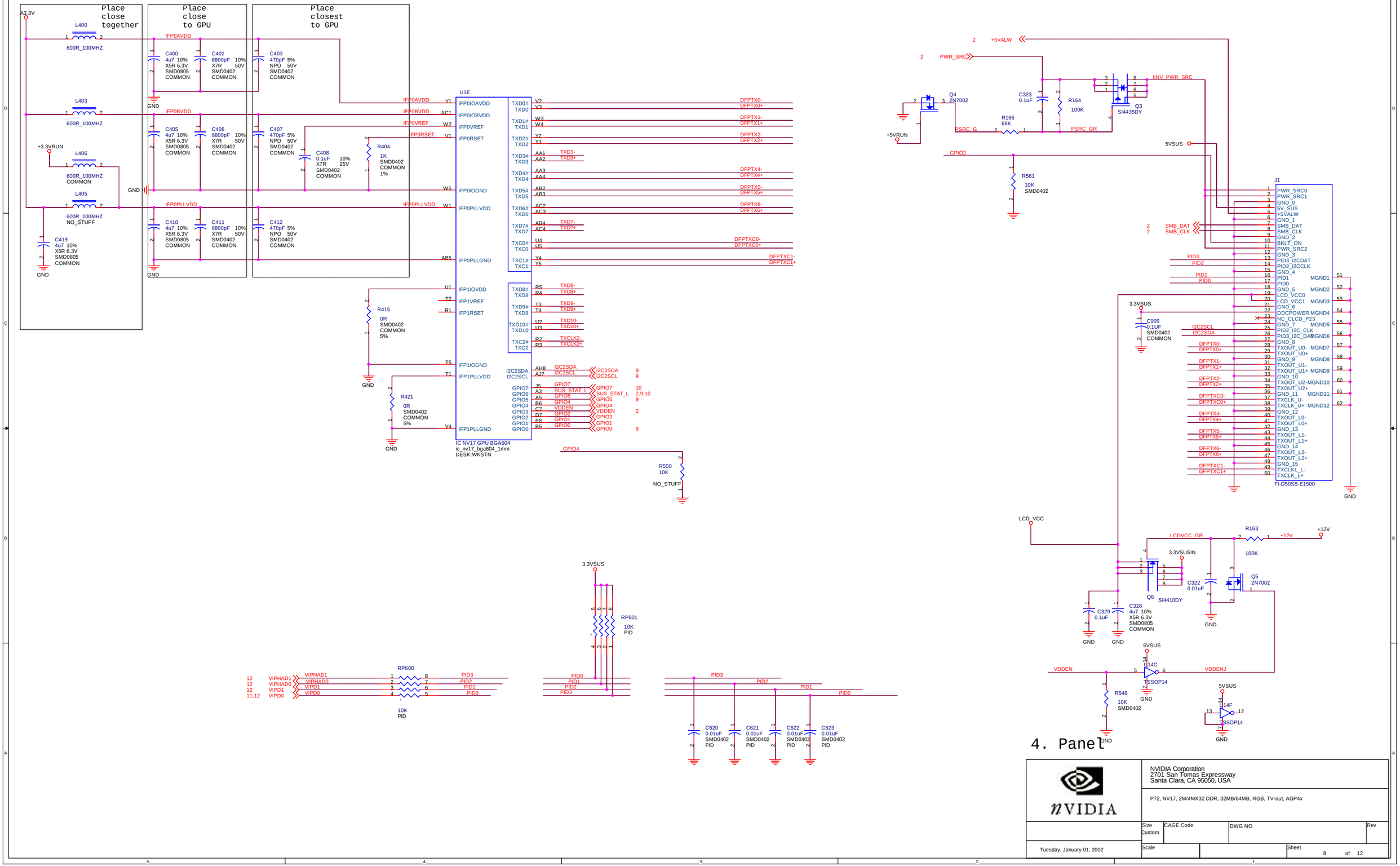
Place close together
Place close to GPU
Place closest to GPU
A3.3V
L400
600R_100MHZ
L403
600R_100MHZ
+3.3VRUN
L406
600R_100MHZ
COMMON
L405
600R_100MHZ
NO_STUFF
C419 4u7 10% X5R 6.3V SMD0805 COMMON
GND
IFP0AVDD
IFP0BVDD
IFP0PLLVDD
C400 4u7 10% X5R 6.3V SMD0805 COMMON
C402 6800pF 10% X7R 50V SMD0402 COMMON
C403 470pF 5% NPO 50V SMD0402 COMMON
C405 4u7 10% X5R 6.3V SMD0805 COMMON
C406 6800pF 10% X7R 50V SMD0402 COMMON
C407 470pF 5% NPO 50V SMD0402 COMMON
C408 0.1uF 10% X7R 25V SMD0402 COMMON
R404 1K SMD0402 COMMON 1%
C410 4u7 10% X5R 6.3V SMD0805 COMMON
C411 6800pF 10% X7R 50V SMD0402 COMMON
C412 470pF 5% NPO 50V SMD0402 COMMON
U1E
IFP0IOAVDD
IFP0IOBVDD
IFP0VREF
IFP0RSET
IFP0IOGND
IFP0PLLVDD
IFP0PLLGND
IFP1IOVDD
IFP1VREF
IFP1RSET
IFP1IOGND
IFP1PLLVDD
IFP1PLLGND
R415 0R SMD0402 COMMON 5%
R421 0R SMD0402 COMMON 5%
TXD0# TXD0
TXD1# TXD1
TXD2# TXD2
TXD3# TXD3
TXD4# TXD4
TXD5# TXD5
TXD6# TXD6
TXD7# TXD7
TXC0# TXC1#
TXD8# TXD8
TXD9# TXD9
TXD10# TXD10
TXC2# TXC2
DFPTX0- DFPTX0+
DFPTX1- DFPTX1+
DFPTX2- DFPTX2+
DFPTX3- DFPTX3+
DFPTX4- DFPTX4+
DFPTX5- DFPTX5+
DFPTX6- DFPTX6+
DFPTX7- DFPTX7+
DFPTXC0- DFPTXC0+
DFPTXC1- DFPTXC1+
DFPTX8- DFPTX8+
DFPTX9- DFPTX9+
DFPTX10- DFPTX10+
DFPTXCLK2- DFPTXCLK2+
I2C2SDA I2C2SCL
GPIO7 GPIO6 GPIO5 GPIO4 GPIO3 GPIO2 GPIO1 GPIO0
SUS_STAT_L VDDEN
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WKSTN
GPIO4
R550 10K NO_STUFF
RP600
VIPHAD1 VIPHAD0 VIPD1 VIPD0
PID3 PID2 PID1 PID0
10K PID
3.3VSUS
RP601 10K PID
C620 0.01uF SMD0402 PID
C621 0.01uF SMD0402 PID
C622 0.01uF SMD0402 PID
C623 0.01uF SMD0402 PID
+5VALW
PWR_SRC
Q4 2N7002
C323 0.1uF
R164 100K
R165 68K
Q3 SI4435DY
IINV_PWR_SRC
PSRC_G
PSRC_GR
+5VRUN
GPIO2
R561 10K SMD0402
5VSUS
J1
PWR_SRC0
PWR_SRC1
GND_0
5V_SUS
+5VALW
GND_1
SMB_DAT
SMB_CLK
GND_2
BKLT_ON
PWR_SRC2
GND_3
PID3_I2CDAT
PID2_I2CCLK
GND_4
PID1
PID0
GND_5
LCD_VCC0
LCD_VCC1
GND_6
DDCPOWER
NC_CLCD_P23
GND_7
PID2_I2C_CLK
PID3_I2C_DAT
GND_8
TXOUT_U0-
TXOUT_U0+
GND_9
TXOUT_U1-
TXOUT_U1+
GND_10
TXOUT_U2-
TXOUT_U2+
GND_11
TXCLK_U-
TXCLK_U+
GND_12
TXOUT_L0-
TXOUT_L0+
GND_13
TXOUT_L1-
TXOUT_L1+
GND_14
TXOUT_L2-
TXOUT_L2+
GND_15
TXCLKL_L-
TXCLK_L+
MGND1 MGND2 MGND3 MGND4 MGND5 MGND6 MGND7 MGND8 MGND9 MGND10 MGND11 MGND12
FI-D50SB-E1500
SMB_DAT
SMB_CLK
I2C2SCL
I2C2SDA
C909 0.1UF SMD0402 COMMON
3.3VSUS
LCD_VCC
LCDVCC_GR
R163 100K
+12V
3.3VSUSIN
Q6 SI4410DY
Q5 2N7002
C322 0.01uF
C328 4u7 10% X5R 6.3V SMD0805 COMMON
C329 0.1uF
VDDEN
VDDENJ
U14C
U14F
TSSOP14
R548 10K SMD0402
4. Panel
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P72, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, AGP4x
Size Custom
CAGE Code
DWG NO
Rev
Tuesday, January 01, 2002
Scale
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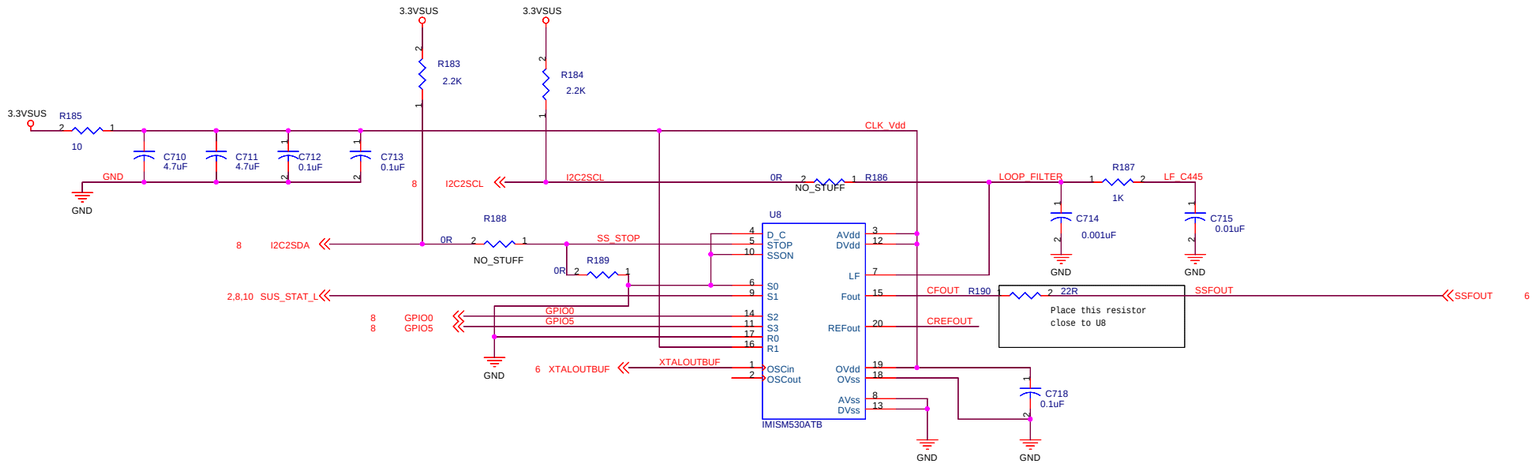

5.b Spread Spectrum Control

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4x

Size	CAGE Code	DWG NO	Rev
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Scale

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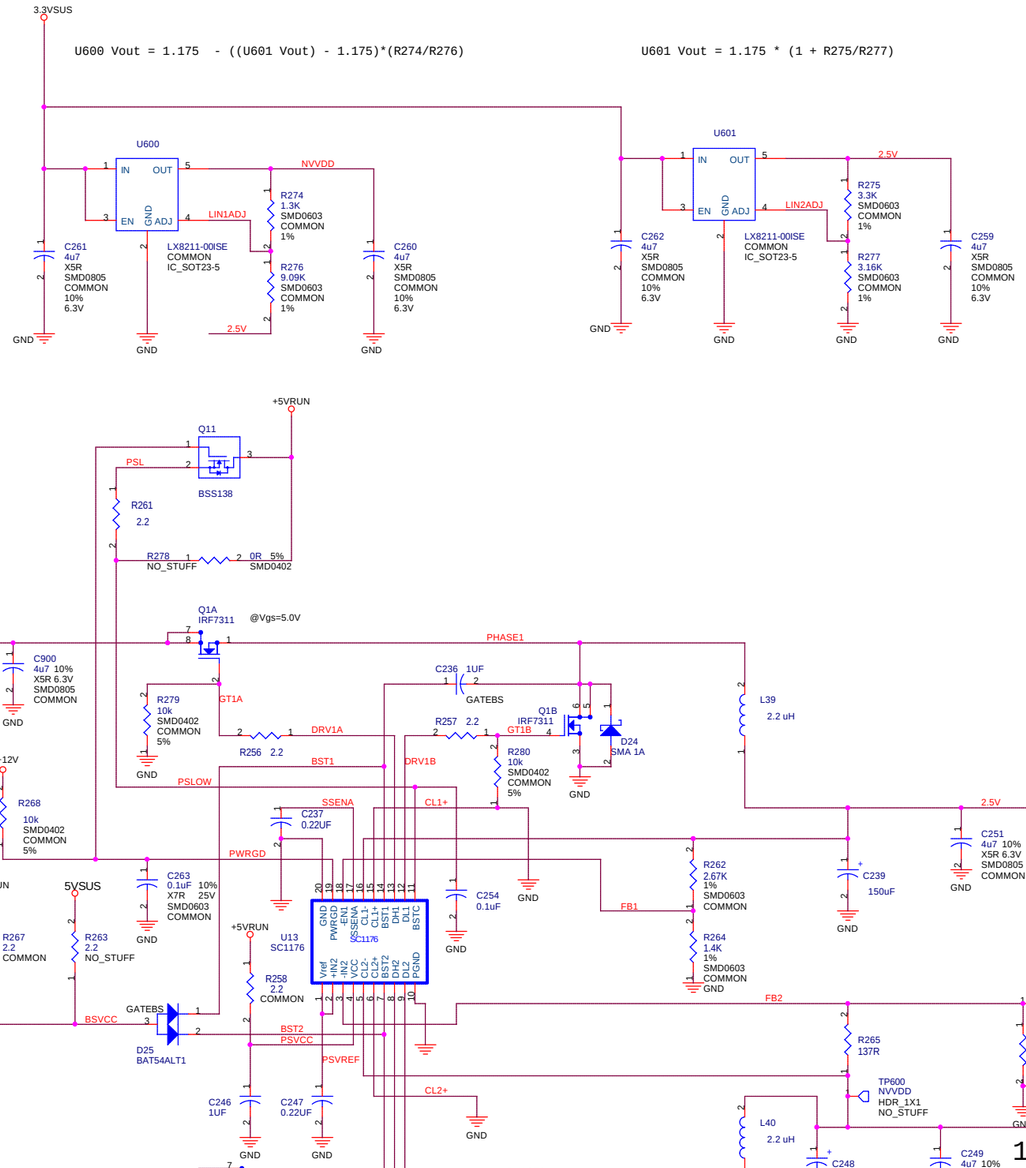
Analog 3.3V

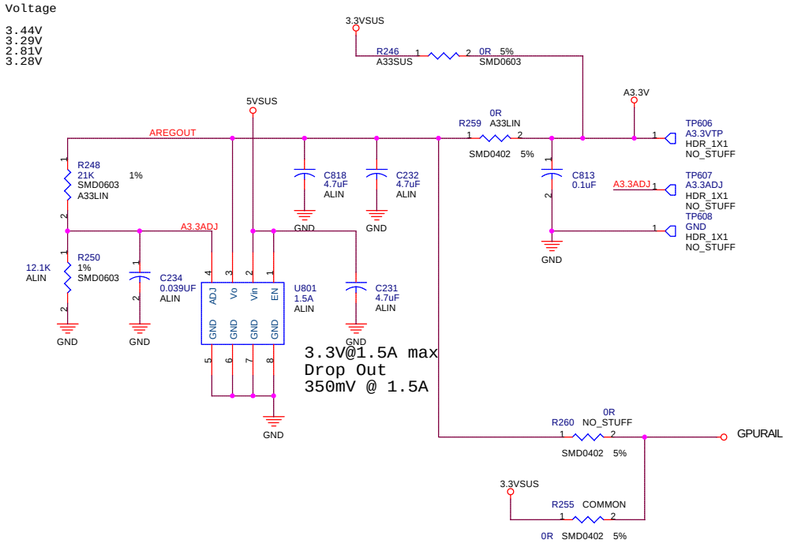
Vo=(1.20 * (R248 + R250)) / R250

R248	R250	Nominal Output Voltage
215R	115R	3.44V
200R	115R	3.29V
154R	115R	2.81V
21K	12.1K	3.28V

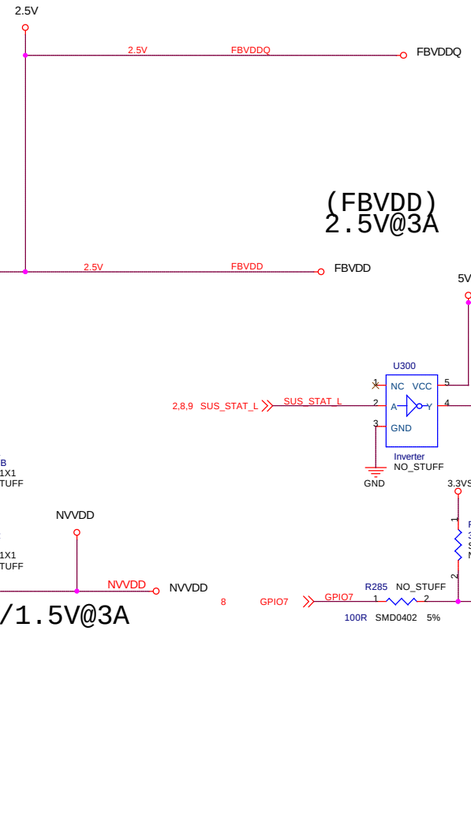
U600 Vout = 1.175 - ((U601 Vout) - 1.175)*(R274/R276)

U601 Vout = 1.175 * (1 + R275/R277)



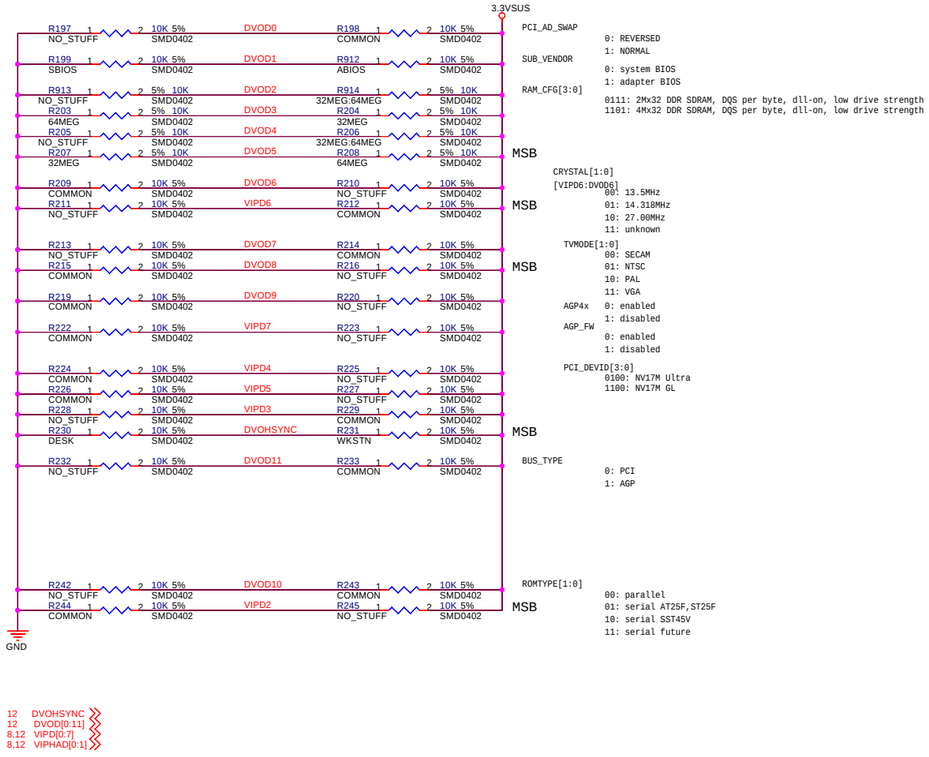


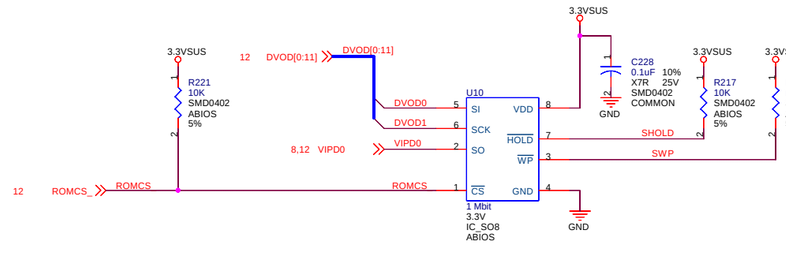
If installing R932 and R933 to use 12V for gate drive, remove R263 and/or D25 to prevent 5VSUS from driving 12V in the case 5VSUS comes up first. Also ensure high side FETs can tolerate 12V gate drive. IRF7311's shown are marginal at best.



NVVDD Switching	SUS_STAT =0	SUS_STAT = 1
GPIO7 = 0	NVVDD = 1.2V	NVVDD = 0.94V
GPIO7 = 1 or not driven	NVVDD = 1.35V	NVVDD = 0.96V

Title	P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4x	
Size: Custom<Doc>	Document Number	Rev: A
Date: Tuesday, January 01, 2002	Sheet 10 of 12	





7. BIOS, Strapping

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

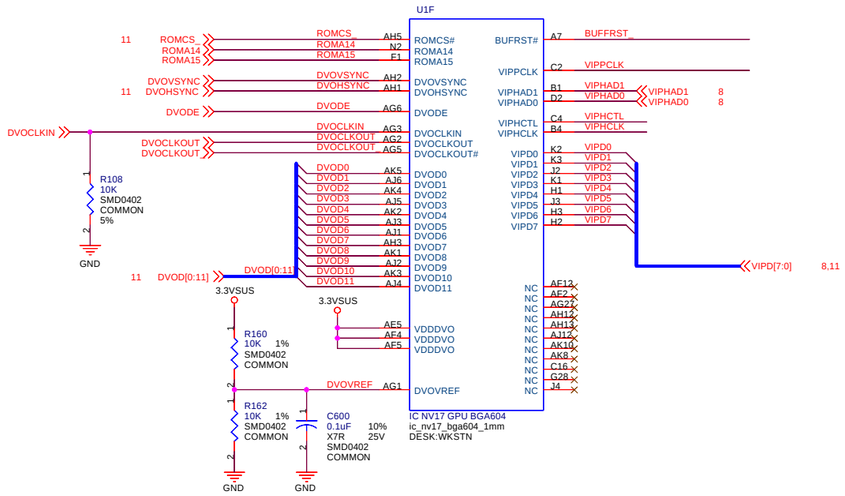
P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4x

Size	CAGE Code	DWG NO	Rev
Custom			

Tuesday, January 01, 2002

Scale

Sheet 11 of 12



5.a TV out,video capture,stereo

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4x

Size	CAGE Code	DWG NO	Rev
Custom			

Tuesday, January 01, 2002

Scale

Sheet 12 of 12