

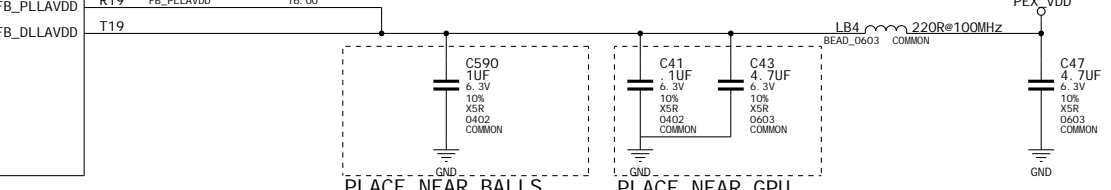
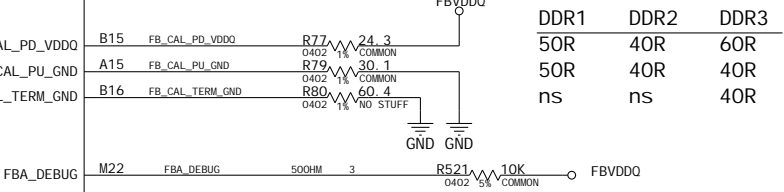
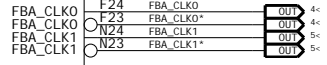
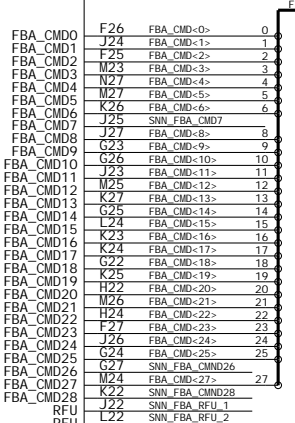
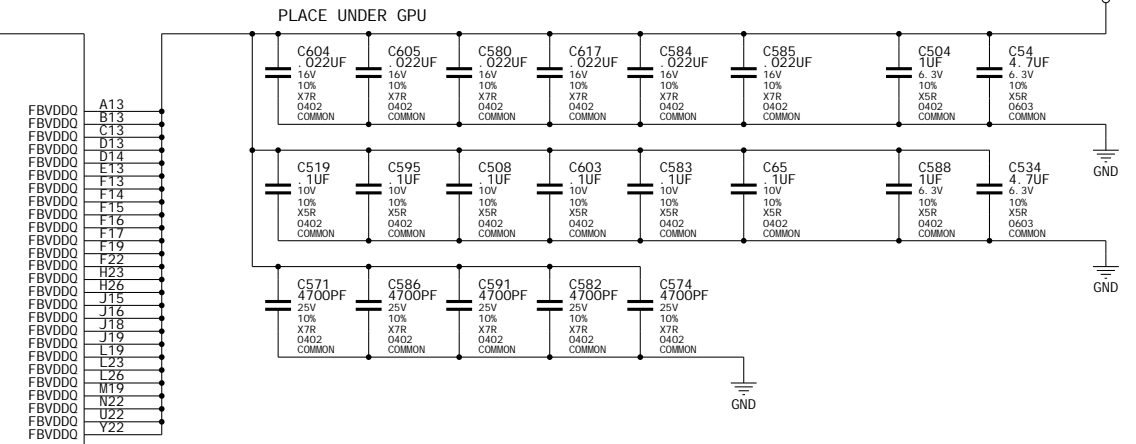
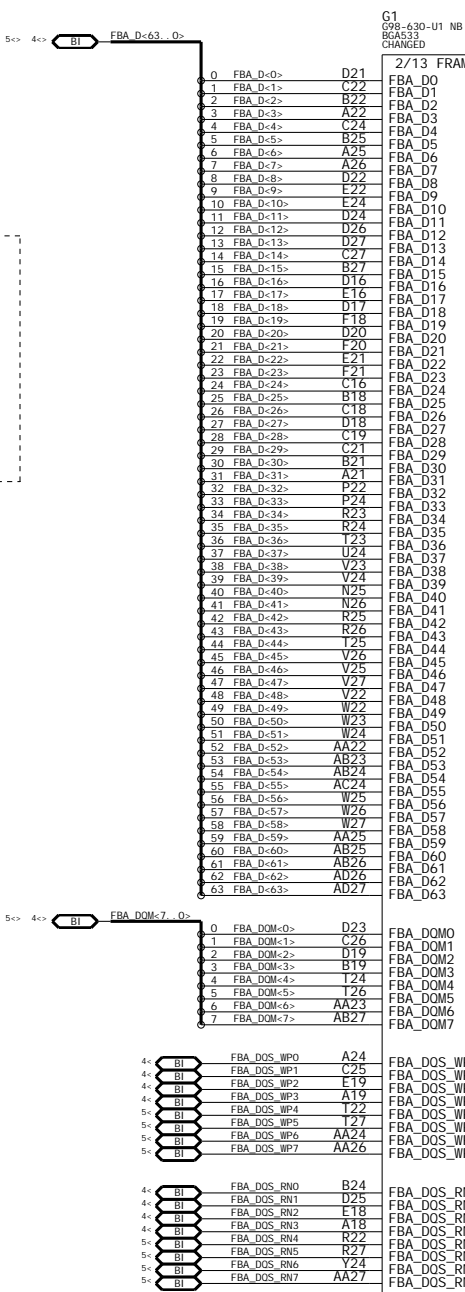
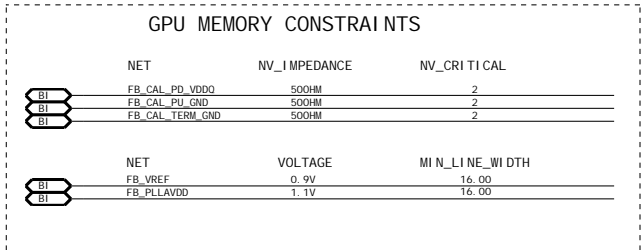
P621-A00: G98-GB1-64, MXM-I , 256/128MB GDDR2 (32M/16Mx16),
LVDS, HDMI , TV_OUT, VGA, HD Audi o, DP opti on

Table of Contents

Page 1: PAGE OVERVIEW
Page 2: PCI EXPRESS INTERFACE
Page 3: GPU MEMORY INTERFACE
Page 4: MEMORY LOWER SUB-PARTITION INTERFACE
Page 5: MEMORY UPPER SUB-PARTITION INTERFACE
Page 6: DAC A/B
Page 7: LVDS(LINK A/B), HD AUDIO
Page 8: HDMI , DP
Page 9: MXM CONNECTOR
Page 10: GPIO, JTAG, TEMP SENSOR
Page 11: VBIOS & HDCP ROM, XTAL, SPREAD SPECTRUM, SPDIF
Page 12: NVVDD POWER SUPPLY
Page 13: PEX, FBVDDQ POWER SUPPLY
Page 14: STRAPS
Page 15: Basenet Report
Page 16: Cref Part

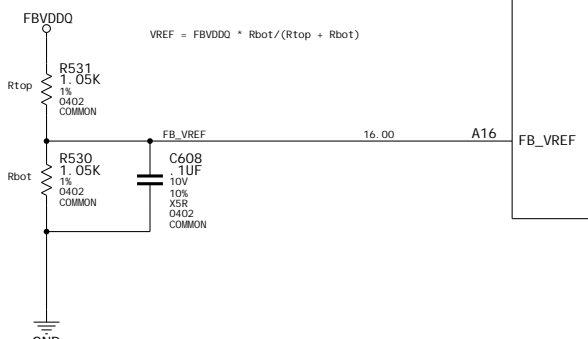
SKU	VARIANT	NVPN	ASSEMBLY
B	Base	600-10621-0000-000	BASE LEVEL GENERIC SCHEMATIC ONLY
1	SKU0001	600-10621-0001-000	NB9M-GS G98M ?/400MHz, 256MB(64bit) GDDR2 32Mx16 84FBGA, LVDS + HDMI + SD/HD(TV_OUT) + VGA
2	SKU0002	600-10621-0002-000	Cancelled 128MB version
3	SKU0003	600-10621-0003-000	NB9M-GE G98M ?/400MHz, 256MB(64bit) GDDR2 32Mx16 84FBGA, LVDS + HDMI + SD/HD(TV_OUT) + VGA
4	SKU9998	600-10621-9998-000	All components
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

GPU MEMORY INTERFACE

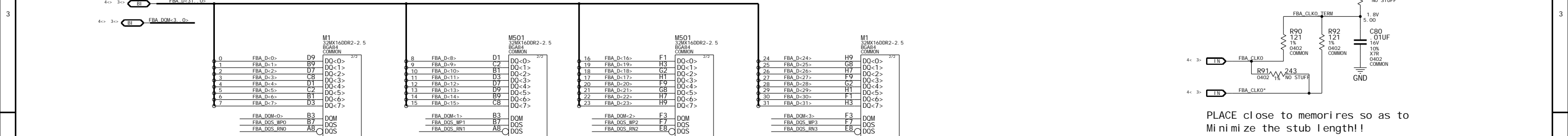
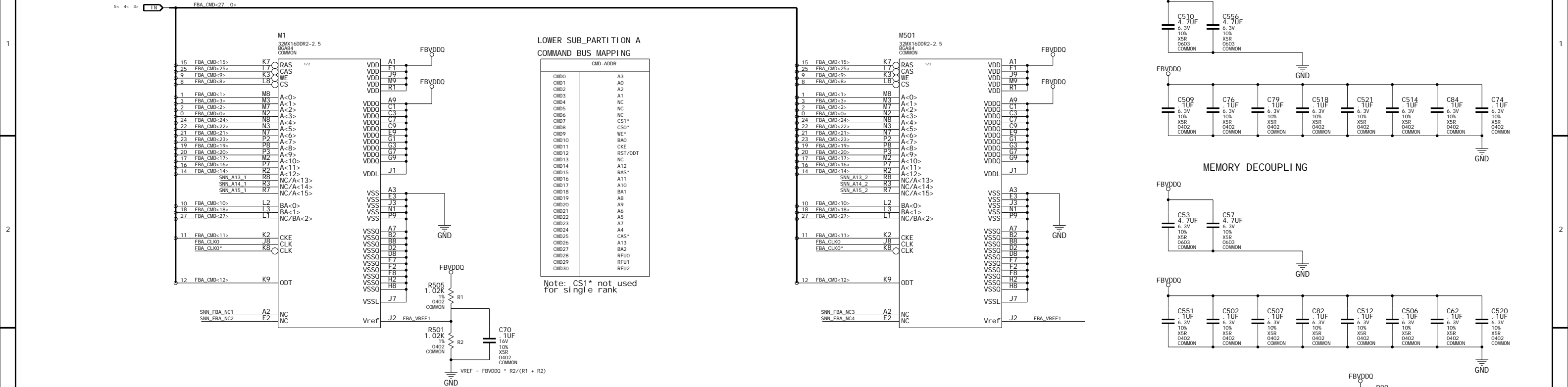


COMMAND BUS MAPPING DDR2-FBGA84

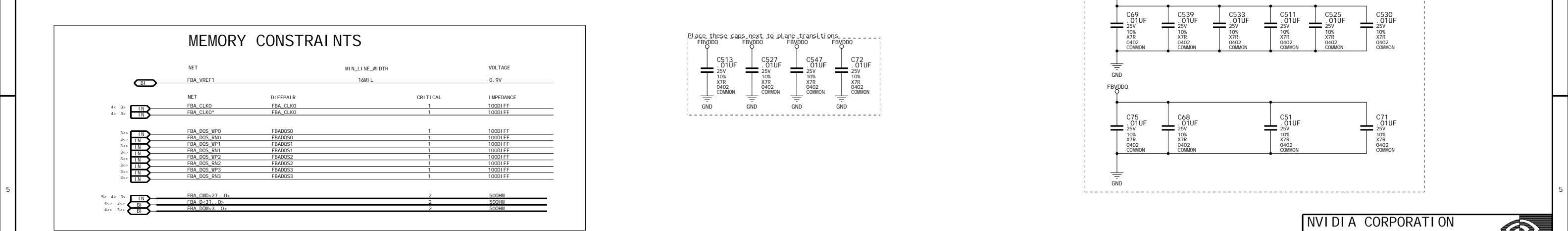
CMD	FB[31..0]	FB[63..32]	CMD	FB[31..0]	FB[63..32]
CMD0	A3	-	CMD16	A11	A11
CMD1	A0	A0	CMD17	A10	A10
CMD2	A2	-	CMD18	BA1	BA1
CMD3	A1	A1	CMD19	A8	A8
CMD4	-	A3	CMD20	A9	A9
CMD5	-	A4	CMD21	A6	A6
CMD6	-	A5	CMD22	A5	-
CMD7	CS1* (BA2)	CS1* (BA2)	CMD23	A7	A7
CMD8	CS0*	CS0*	CMD24	A4	-
CMD9	WE*	WE*	CMD25	CAS*	CAS*
CMD10	BA0	BA0	CMD26	A13	A13
CMD11	CKE	CKE	CMD27	BA2	BA2
CMD12	RST/ODT	RST/ODT	CMD28	RFU0	RFU0
CMD13	-	A2	CMD29	RFU1	RFU1
CMD14	A12	A12	CMD30	RFU2	RFU2
CMD15	RAS*	RAS*			



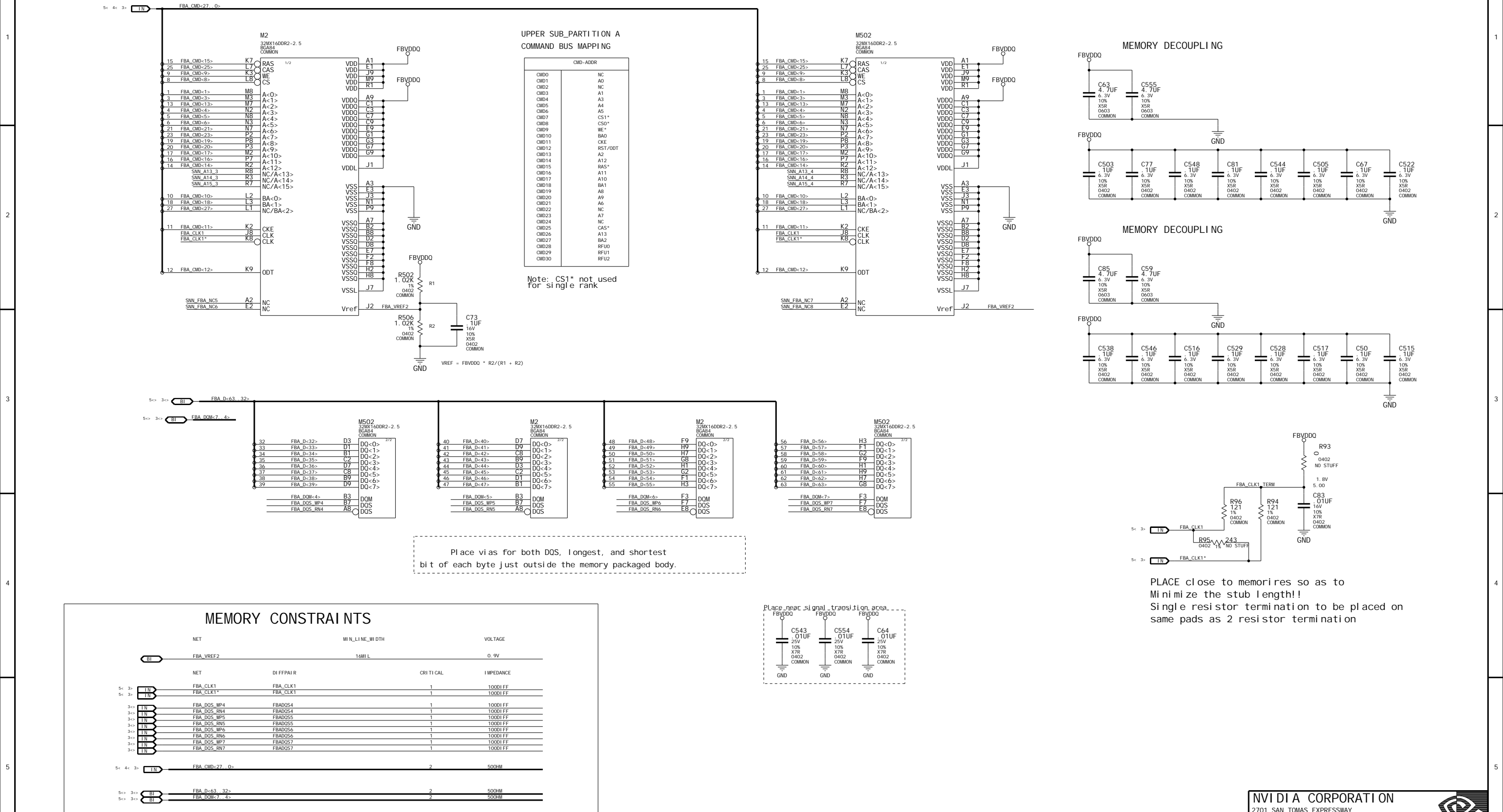
MEMORY LOWER SUB-PARTITION INTERFACE D<31..0>



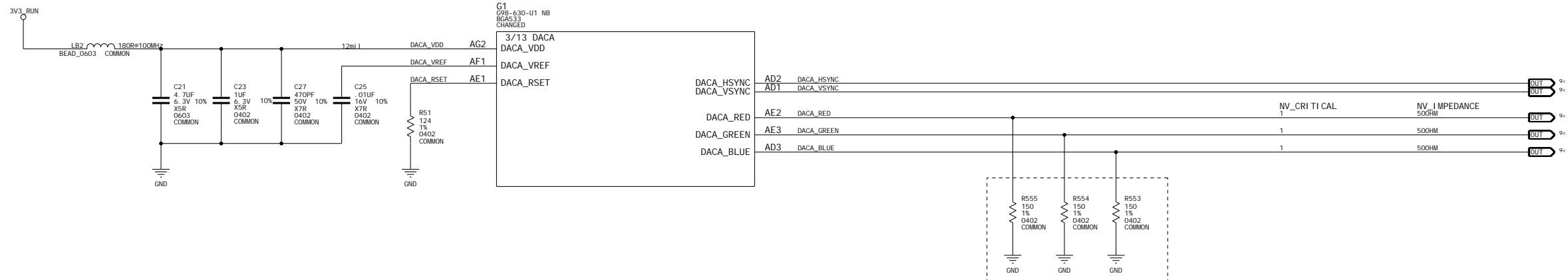
Place vias for both DQS, longest, and shortest bit of each byte just outside the memory packaged body.



MEMORY UPPER SUB-PARTITION INTERFACE D<63..32>

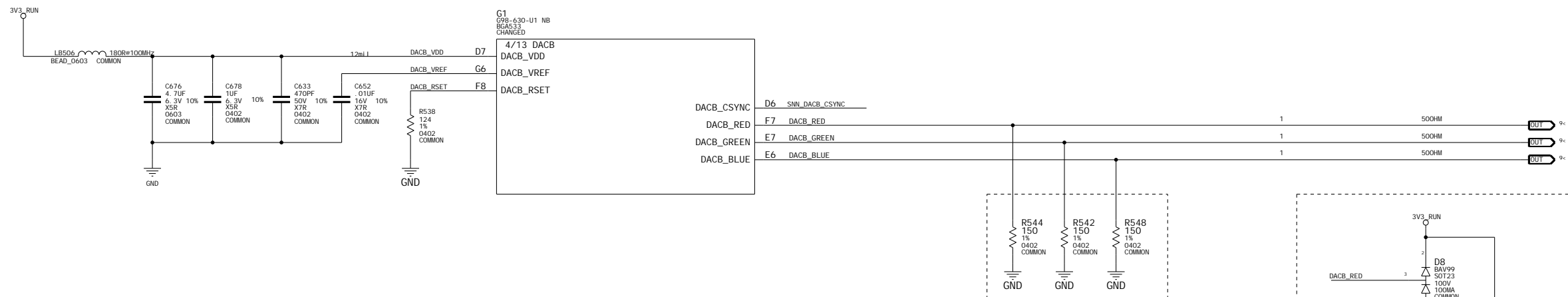


DAC_A



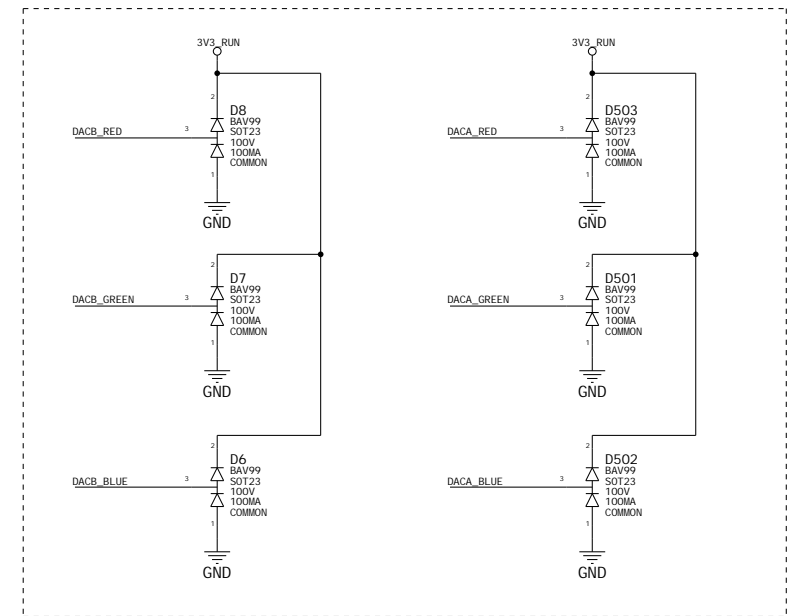
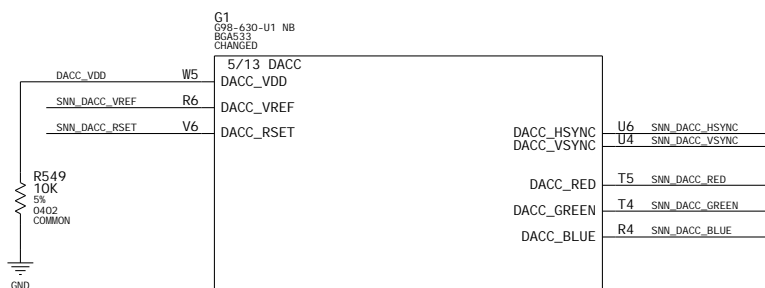
Place close to GPU

DAC_B



Place close to GPU


DAC_C



TV DAC ESD PROTECTION

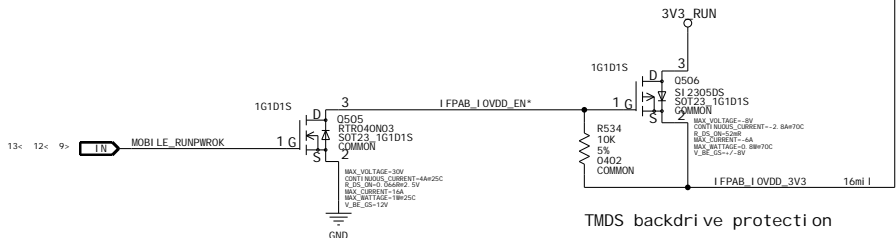
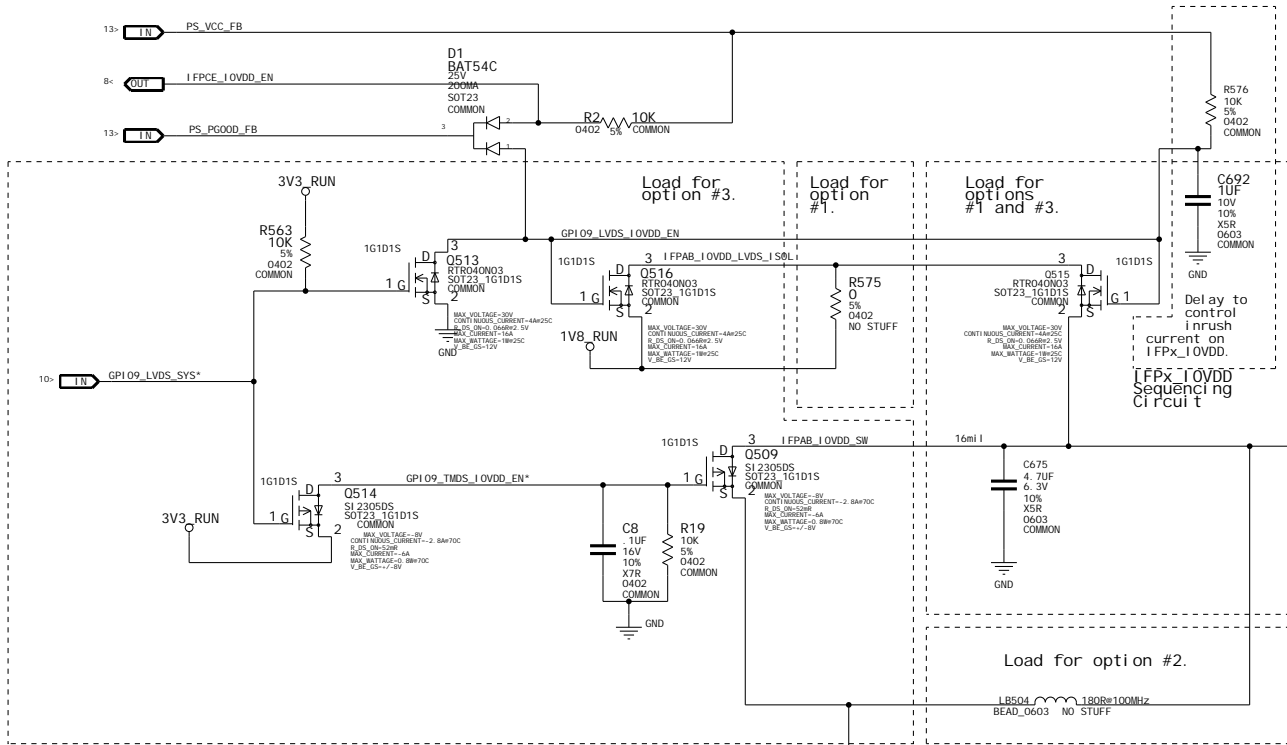
ASSEMBLY	
PAGE DETAIL	DAC A/B

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVI DI A CORPORATI ON			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-10621-0001-000 A		
ID	p621	PAGE	6 OF 16
NAME	Thorsten Freund	DATE	13-SEP-2007

Loading options for IFPAB outputs

- Option #1) IFPAB outputs to LVDS only.
Option #2) IFPAB outputs to DVI-C only.
Option #3) Controlled with GPI09, IFPAB dynamically outputs to LVDS or DVI -C.

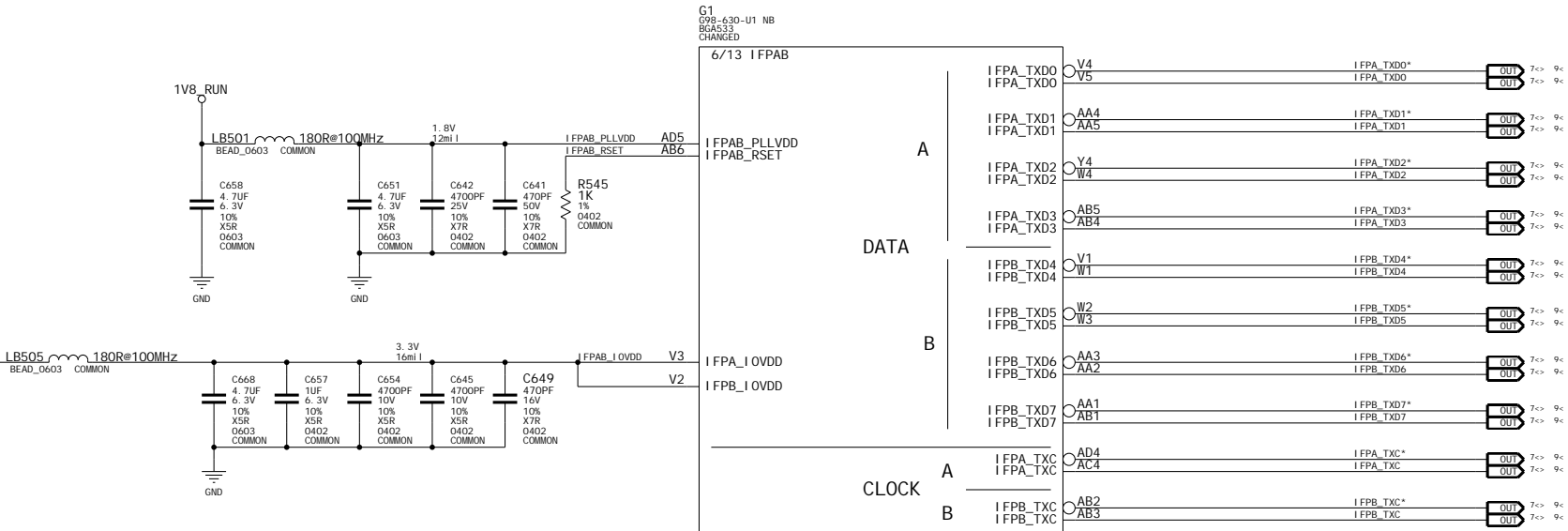


(LVDS & HD AUDIO CONSTRAINTS)

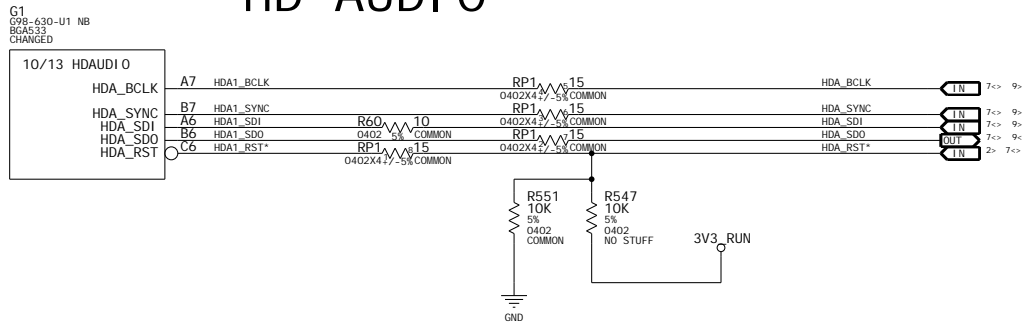
NET NAME	DIFFPAIR	NV_Critical_NET	NV_IMPEDANCE		
IFPA_TXD0*	IFPATXD0	1	100DFF	BI	7< 9<
IFPA_TXD0	IFPATXD0	1	100DFF	BI	7< 9<
IFPA_TXD1*	IFPATXD1	1	100DFF	BI	7< 9<
IFPA_TXD1	IFPATXD1	1	100DFF	BI	7< 9<
IFPA_TXD2*	IFPATXD2	1	100DFF	BI	7< 9<
IFPA_TXD2	IFPATXD2	1	100DFF	BI	7< 9<
IFPA_TXD3*	IFPATXD3	1	100DFF	BI	7< 9<
IFPA_TXD3	IFPATXD3	1	100DFF	BI	7< 9<
IFPB_TXD4*	IFPBTXD4	1	100DFF	BI	7< 9<
IFPB_TXD4	IFPBTXD4	1	100DFF	BI	7< 9<
IFPB_TXD5*	IFPBTXD5	1	100DFF	BI	7< 9<
IFPB_TXD5	IFPBTXD5	1	100DFF	BI	7< 9<
IFPB_TXD6*	IFPBTXD6	1	100DFF	BI	7< 9<
IFPB_TXD6	IFPBTXD6	1	100DFF	BI	7< 9<
IFPB_TXD7*	IFPBTXD7	1	100DFF	BI	7< 9<
IFPB_TXD7	IFPBTXD7	1	100DFF	BI	7< 9<
IFPA_TXC*	IFPATXC	1	100DFF	BI	7< 9<
IFPA_TXC	IFPATXC	1	100DFF	BI	7< 9<
IFPB_TXC*	IFPBTXC	1	100DFF	BI	7< 9<
IFPB_TXC	IFPBTXC	1	100DFF	BI	7< 9<

	NV_Critical_NET	NV_IMPEDANCE		
HDA1_BCLK	2	50OHM	BI	
HDA1_SYNC	2	50OHM	BI	
HDA1_SDI	2	50OHM	BI	
HDA1_SDO	2	50OHM	BI	
HDA1_RST*	2	50OHM	BI	
HDA_BCLK	2	50OHM	BI	7< 9<
HDA_SYNC	2	50OHM	BI	7< 9<
HDA_SDI	2	50OHM	BI	7< 9<
HDA_SDO	2	50OHM	BI	7< 9<
HDA_RST*	2	50OHM	BI	2< 7<

LVDS/TMDS(Link A&B)



HD AUDIO



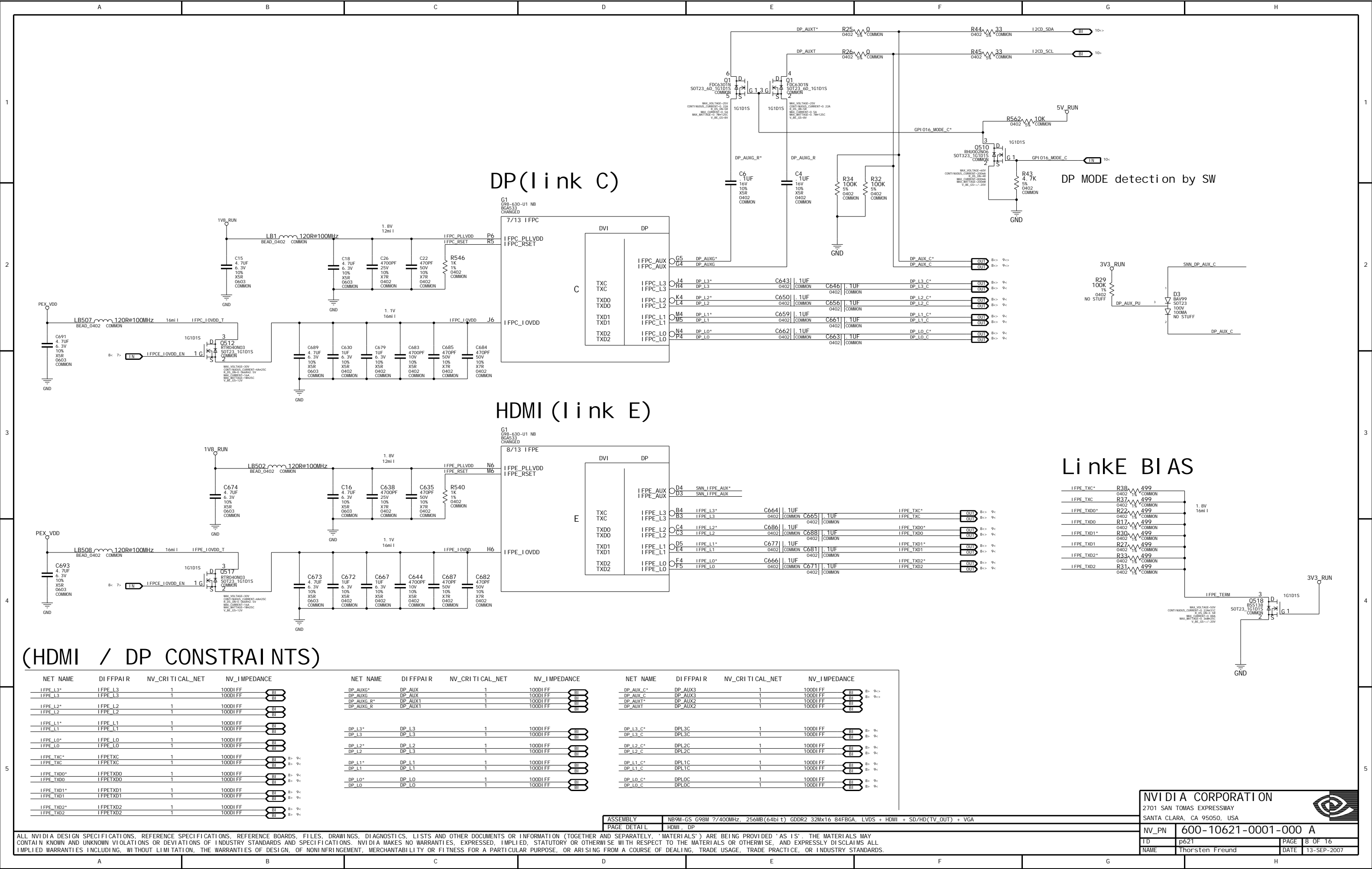
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

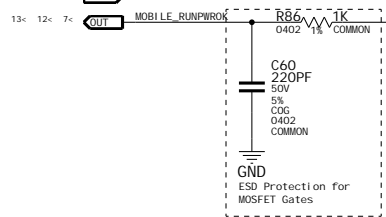
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



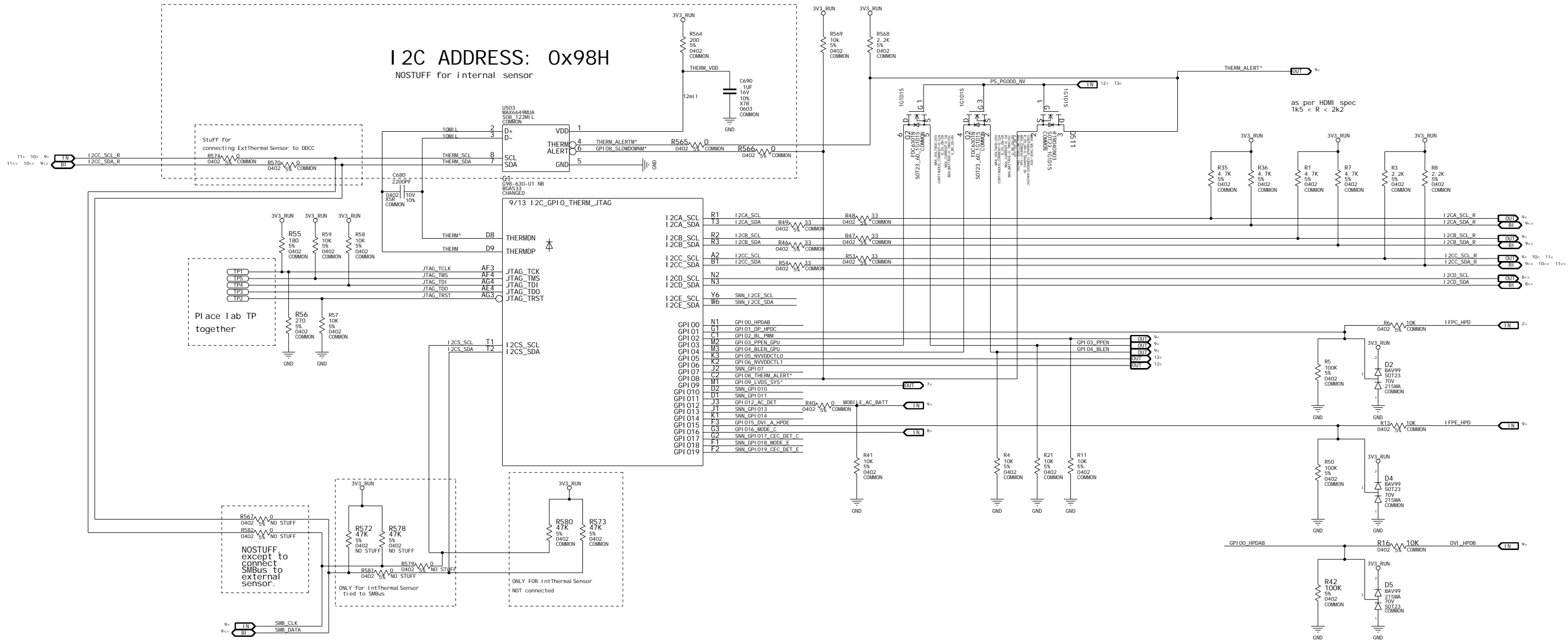
NV_PN	600-10621-0001-000 A		
ID	p621	PAGE	7 OF 16
NAME	Thorsten Freund	DATE	13-SEP-2007



CN1
CON_MXM_X16_EDGE
(N, NON)PHY(-X16, -HE)
NONPHY-X16
COMMON



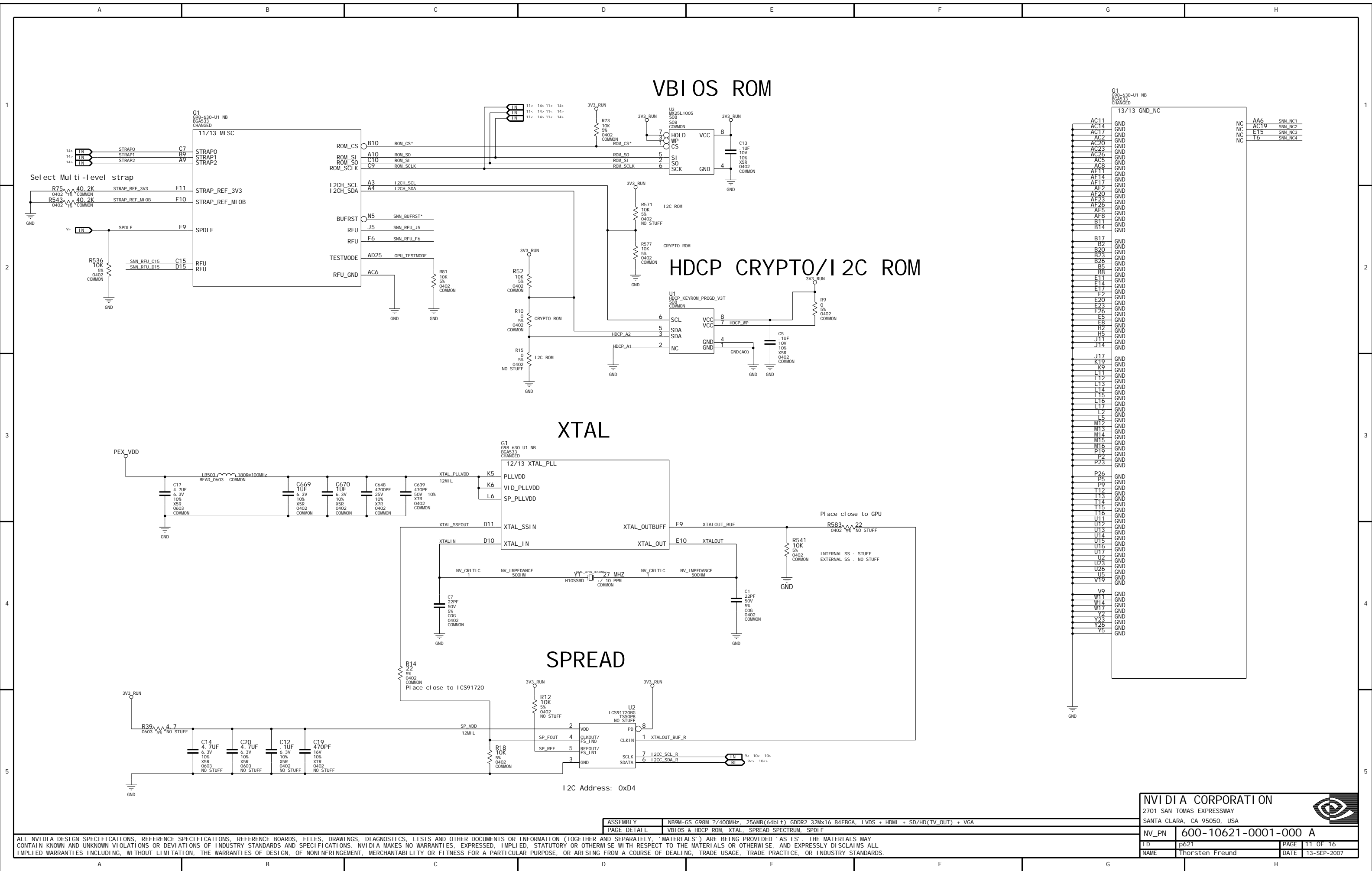
GPI 0, TEMP SENSOR, JTAG



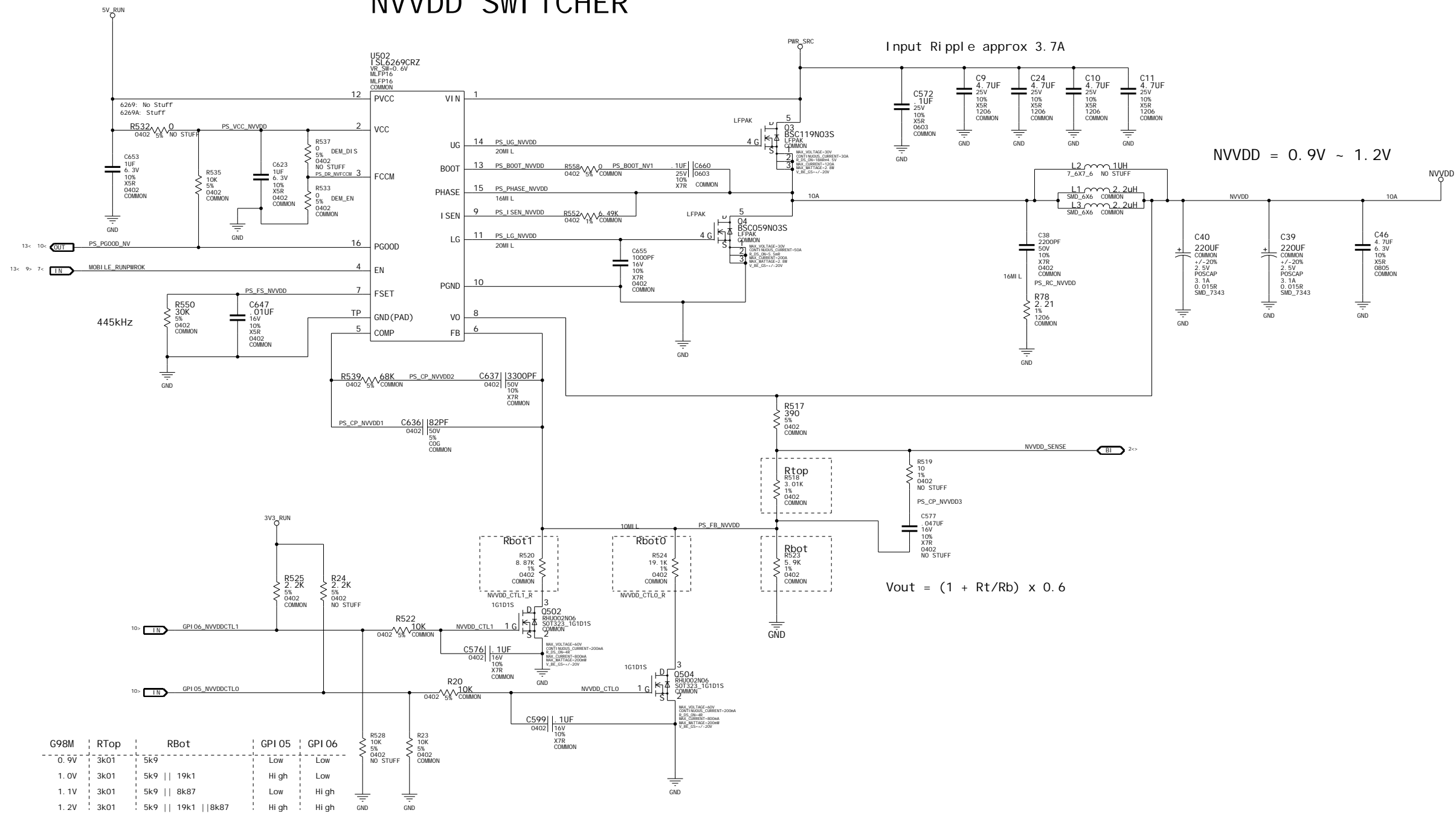
ASSEMBLY	NB9M-GS G98M ?/400MHz, 256MB(64bi t) GDDR2 32Mx16 84FBGA, LVDS + HDMI + SD/HD(TV_OUT) + VGA
PAGE DETAIL	GPIO, JTAG, TEMP SENSOR

NV_PN	600-10621-0001-000 A		
ID	p621	PAGE	10 OF 16
NAME	Thorsten Freund	DATE	13-SEP-2007

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

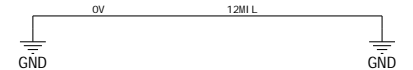


NVVDD SWITCHER



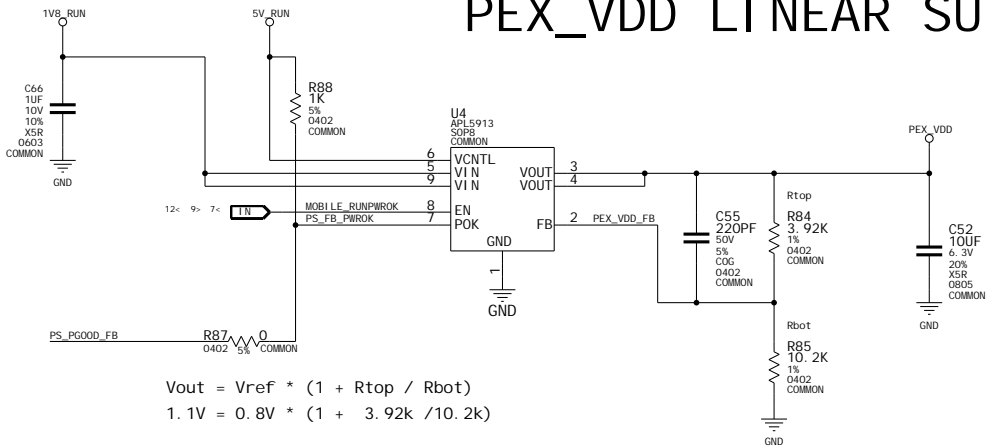
VOLTAGE NODE PROPERTIES

	VOLTAGE	SOURCE POWER NET	MIN LINE WIDTH	MAX. CURRENT	
3V3_RUN	3.3V	TRUE	12MIL	1.5A	3V3_RUN
1V8_RUN	1.8V	TRUE	16MIL	3.5A	1V8_RUN
5V_RUN	5.0V	TRUE	12MIL	0.5A	5V_RUN
PWR_SRC	22V	TRUE	30MIL	4A	PWR_SRC
NVVDD	1.2V		16MIL	10A	NVVDD
PEX_VDD	1.1V		16MIL	2.5A	PEX_VDD
FBVDDQ	1.8V		12MIL	5A	FBVDDQ



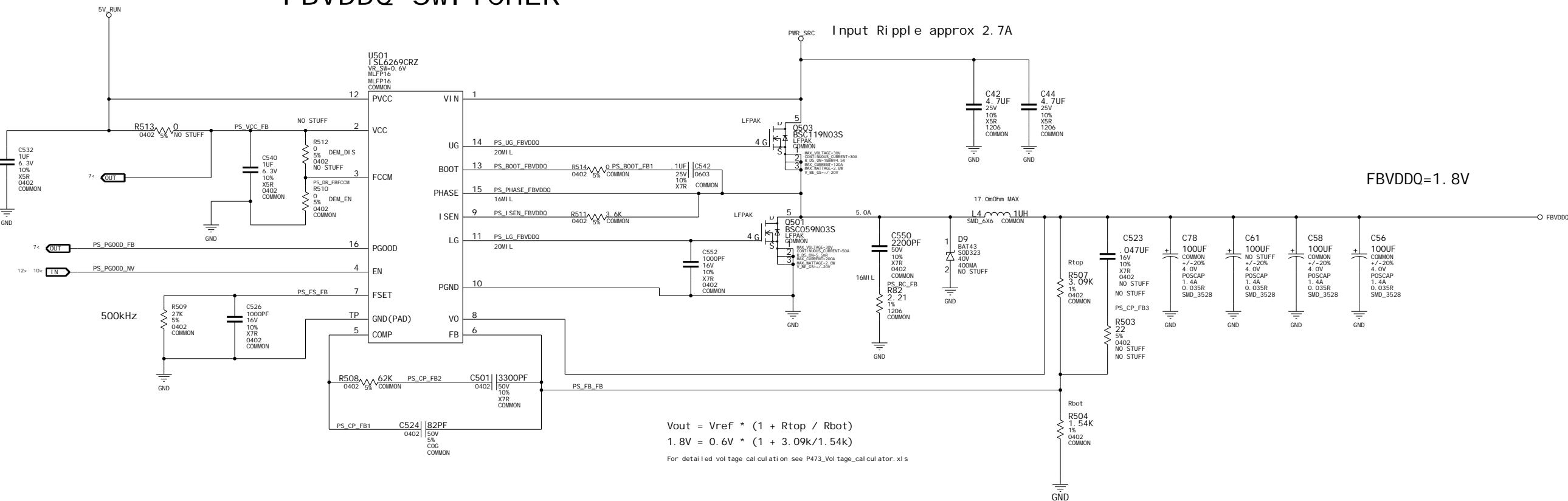
$$V_{out} = (1 + R_t/R_b) \times 0.6$$

PEX_VDD LINEAR SUPPLY



$$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$$
$$1.1V = 0.8V * (1 + 3.92k / 10.2k)$$

FBVDDQ SWITCHER



$$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$$
$$1.8V = 0.6V * (1 + 3.09k / 1.54k)$$

For detailed voltage calculation see P473_Voltage_calculator.xls

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

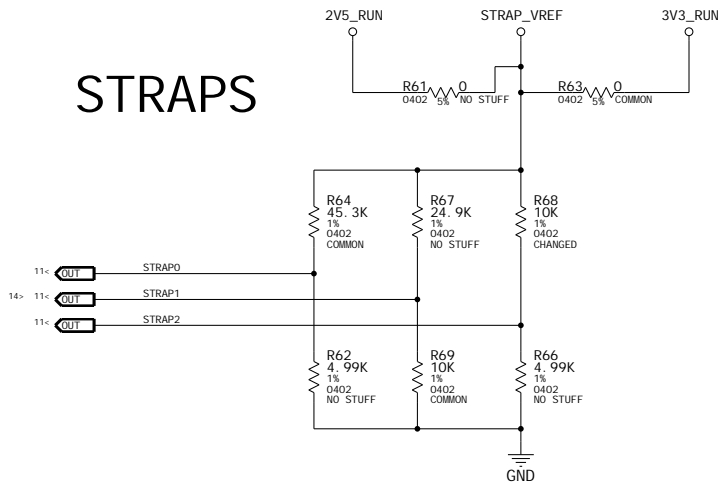


ASSEMBLY	NB9M-GS G98M 7/400MHz, 256MB(64bit) GDDR2 32Mx16 84FBGA, LVDS + HDMI + SD/HD(TV_OUT) + VGA
PAGE DETAIL	PEX_FBVDDQ POWER SUPPLY

NV_PN	600-10621-0001-000	A
ID	p621	PAGE 13 OF 16
NAME	Thorsten Freund	DATE 13-SEP-2007

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

STRAPS



STRAP0

STRAP1

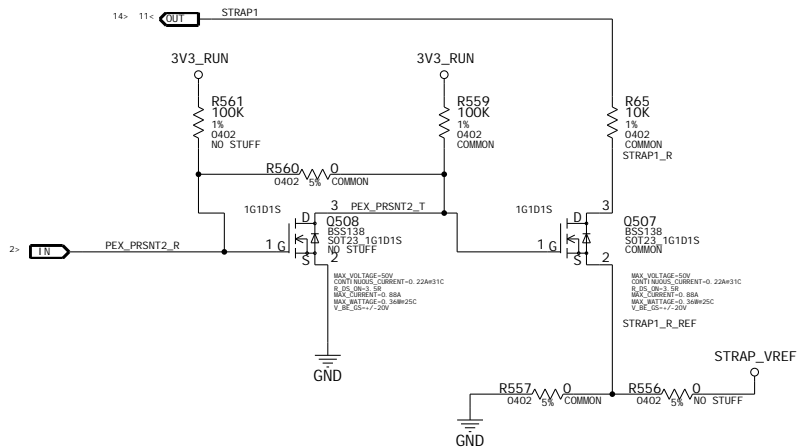
STRAP2

ROM_SO

ROM_SI

ROM_SCLK

PEX SWING LEVEL



PEX_PRST2_R	R_STRAP1	3_GI O_PADCFG_LUT<3..0>
GND	10k	0x1 MOBILE_DEFAULT
FLOAT	5k (10k 10k)	0x0 DESKTOP_DEFAULT

USER_BIT0 0xF: 45K PU (unused)
USER_BIT1
USER_BIT2
USER_BIT3

3GIO_PADCFG_LUT_ADR0
3GIO_PADCFG_LUT_ADR1 0x0: Desktop default t (normal swing) - 5k PD
3GIO_PADCFG_LUT_ADR2 0x1: Mobile default (low swing) - 10k PD
3GIO_PADCFG_LUT_ADR3 acc. to //hw/tesla_g98b/manuals/dev_ext_devices.ref

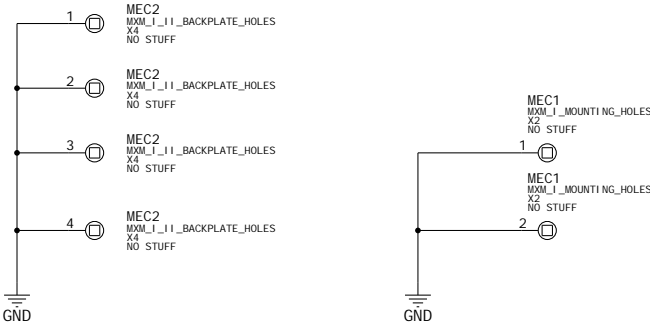
PCI_DEVID_0 all 4 bits set by HW strapping
PCI_DEVID_1 0x06E8: 5K PU (NB9M-GE)
PCI_DEVID_2 0x06E9: 10K PU (NB9M-GS)
PCI_DEVID_3

TV_MODE_BIT0 0x0: NTSC-M
TV_MODE_BIT1 5K PU
TV_MODE_BIT2
XCLK_277 1:

RAM_CFG_0	128 MB (4pcs. 16Mx16)	256 MB (4pcs. 32Mx16)
RAM_CFG_1	RAM_CFG[3:0] Definitions	RAM_CFG[3:0] Definitions
RAM_CFG_2	0000 Elpi da 0001 Samsung 0010 Qimonda 0011 Hynix 0100 Nanya	0100 25k PD Elpi da 0101 30k PD Samsung 0110 35k PD Qimonda 0111 45k PD Hynix
RAM_CFG_3		

PCI_DEVID_EXT 0:
SUB_VENDOR 1: SUB_VENDOR BIOS 25K PD
SLOT_CLK_CONFIG 0:
PEX_PLL_EN_TERM100 0: TERM100 DISABLED

MECHANICAL



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



NV_PN	600-10621-0001-000 A		
ID	p621	PAGE	14 OF 16
NAME	Thorsten Freund	DATE	13-SEP-2007

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

A		B		C		D		E		F		G		H	
<div>Title: Cref Part</div> <div>Report</div> <div>Desi gn: p621</div> <div>Date: Aug 27</div> <div>12: 32: 38 2007</div>		<div>C532 [13. 3D]</div> <div>C534 [13. 4D]</div> <div>C536 [2. 5C]</div> <div>C537 [2. 5D]</div> <div>C538 [2. 5C]</div> <div>C540 [2. 4D]</div> <div>C542 [2. 4C]</div> <div>C543 [2. 4D]</div> <div>C544 [2. 4C]</div> <div>C545 [2. 4D]</div> <div>C546 [2. 4C]</div> <div>C547 [2. 4D]</div> <div>C548 [2. 4C]</div> <div>C549 [2. 4D]</div> <div>C550 [12. 4C]</div> <div>C551 [2. 4C]</div> <div>C552 [2. 3D]</div> <div>C553 [2. 3C]</div> <div>C554 [2. 3D]</div> <div>C555 [12. 2D]</div> <div>C556 [2. 1H]</div> <div>C557 [2. 3C]</div> <div>C558 [2. 3D]</div> <div>C559 [2. 3C]</div> <div>C560 [2. 3D]</div> <div>C561 [2. 3C]</div> <div>C562 [2. 3D]</div> <div>C563 [12. 4D]</div> <div>C565 [2. 1H]</div> <div>C566 [2. 3C]</div> <div>C567 [2. 2G]</div> <div>C568 [2. 2H]</div> <div>C569 [2. 2D]</div> <div>C570 [2. 3G]</div> <div>C571 [2. 2C]</div> <div>C572 [2. 2D]</div> <div>C573 [2. 1G]</div> <div>C575 [2. 2H]</div> <div>C576 [2. 2H]</div> <div>C577 [2. 2C]</div> <div>C578 [2. 3G]</div> <div>C580 [2. 2D]</div> <div>C582 [2. 1G]</div> <div>C583 [12. 4C]</div> <div>C584 [2. 2C]</div> <div>C585 [2. 1G]</div> <div>C586 [2. 4G]</div> <div>C587 [2. 4G]</div> <div>C588 [2. 2D]</div> <div>C590 [12. 2B]</div> <div>C591 [2. 1G]</div> <div>C592 [2. 2C]</div> <div>C593 [2. 2G]</div> <div>C594 [2. 2G]</div> <div>C595 [2. 1G]</div> <div>C596 [2. 1G]</div> <div>C597 [2. 2G]</div> <div>C598 [6. 3B]</div> <div>C600 [2. 2G]</div> <div>C602 [2. 2G]</div> <div>C604 [2. 1G]</div> <div>C606 [6. 3B]</div> <div>C607 [2. 1G]</div> <div>C608 [2. 2G]</div> <div>C609 [12. 3B]</div> <div>C610 [12. 3C]</div> <div>C611 [2. 4G]</div> <div>C614 [12. 3B]</div> <div>C615 [12. 2C]</div> <div>C616 [12. 2A]</div> <div>C617 [7. 2E]</div> <div>C618 [8. 3C]</div> <div>C619 [8. 2C]</div> <div>C620 [6. 1B]</div> <div>C621 [6. 1B]</div> <div>C622 [12. 2D]</div> <div>C623 [7. 2E]</div> <div>C624 [11. 3C]</div> <div>C625 [8. 3C]</div> <div>C626 [8. 2C]</div> <div>C628 [6. 1B]</div> <div>C629 [6. 1B]</div> <div>C630 [11. 3C]</div> <div>C631 [8. 3B]</div> <div>C632 [7. 2E]</div> <div>C633 [2. 1H]</div> <div>C634 [7. 2E]</div> <div>C636 [6. 3B]</div> <div>C637 [8. 2B]</div> <div>C638 [7. 2E]</div> <div>C639 [7. 2E]</div> <div>C642 [11. 3A]</div> <div>C643 [2. 4H]</div> <div>C644 [6. 3B]</div> <div>C646 [7. 2E]</div> <div>C647 [10. 2D]</div>		<div>C648 [8. 3B]</div> <div>C649 [7. 2E]</div> <div>C650 [7. 2B]</div> <div>C651 [8. 2B]</div> <div>C652 [11. 4C]</div> <div>C654 [11. 4E]</div> <div>C656 [8. 2A]</div> <div>C657 [11. 2E]</div> <div>C1075 [3. 5C]</div> <div>C1077 [3. 5G]</div> <div>C1081 [4. 1G]</div> <div>C1082 [5. 4E]</div> <div>C1083 [5. 2G]</div> <div>C1084 [5. 1F]</div> <div>C1085 [5. 2F]</div> <div>C1086 [5. 2H]</div> <div>C1088 [5. 3H]</div> <div>C1089 [4. 1G]</div> <div>C1090 [4. 1G]</div> <div>C1091 [4. 2G]</div> <div>C1093 [4. 1G]</div> <div>C1094 [5. 2G]</div> <div>C1097 [5. 1G]</div> <div>C1098 [5. 3H]</div> <div>C1099 [5. 2G]</div> <div>C1101 [4. 1H]</div> <div>C1102 [4. 1H]</div> <div>C1103 [5. 2G]</div> <div>C1104 [5. 3C]</div> <div>C1105 [4. 4G]</div> <div>C1106 [4. 3H]</div> <div>C1107 [4. 5G]</div> <div>C1109 [5. 2H]</div> <div>C1110 [4. 5F]</div> <div>C1112 [4. 4H]</div> <div>C1113 [4. 4G]</div> <div>C1114 [4. 4F]</div> <div>C1116 [4. 4G]</div> <div>C1117 [4. 5G]</div> <div>C1118 [4. 5H]</div> <div>C1119 [4. 4E]</div> <div>C1120 [4. 2H]</div> <div>C1121 [4. 4E]</div> <div>C1122 [4. 4D]</div> <div>C1123 [4. 4D]</div> <div>C1124 [4. 4G]</div> <div>C1546 [4. 2H]</div> <div>C1548 [5. 4E]</div> <div>C1549 [5. 3H]</div> <div>C1550 [5. 2H]</div> <div>C1551 [5. 3G]</div> <div>C1552 [4. 2H]</div> <div>C1554 [4. 3C]</div> <div>C1555 [5. 4H]</div> <div>C1559 [5. 3G]</div> <div>C1560 [5. 4E]</div> <div>C1562 [4. 1G]</div> <div>C1563 [4. 2G]</div> <div>C1564 [4. 1G]</div> <div>C1565 [4. 1G]</div> <div>C1566 [4. 2G]</div> <div>C1567 [4. 2G]</div> <div>C1570 [4. 2G]</div> <div>C1571 [5. 2G]</div> <div>C1572 [5. 2F]</div> <div>C1573 [5. 3F]</div> <div>C1574 [4. 1H]</div> <div>C1576 [4. 2G]</div> <div>C1579 [4. 2G]</div> <div>C1581 [5. 3G]</div> <div>C1583 [5. 3G]</div> <div>C1591 [3. 5F]</div> <div>C1595 [3. 1E]</div> <div>C1596 [3. 1E]</div> <div>C1598 [3. 1F]</div> <div>C1602 [3. 1F]</div> <div>C1603 [3. 1G]</div> <div>C1607 [3. 1F]</div> <div>C1608 [3. 1F]</div> <div>C1609 [3. 1E]</div> <div>C1610 [3. 1E]</div> <div>C1612 [3. 5F]</div> <div>C1613 [3. 5F]</div> <div>C1616 [3. 1G]</div> <div>C1617 [3. 1F]</div> <div>C1618 [3. 1G]</div> <div>C1624 [3. 1E]</div> <div>C1633 [3. 1F]</div> <div>C1635 [3. 1G]</div> <div>C1636 [3. 1F]</div> <div>C1637 [3. 1F]</div> <div>C1640 [3. 1F]</div> <div>C1653 [3. 1F]</div> <div>CN1 [2. 3B]</div> <div>CN1 [9. 3D]</div> <div>D1 [10. 4G]</div>		<div>D2 [13. 4E]</div> <div>D3 [10. 4G]</div> <div>D4 [6. 3G]</div> <div>D5 [6. 4G]</div> <div>D6 [6. 4G]</div> <div>D7 [6. 3H]</div> <div>D8 [6. 4H]</div> <div>D9 [6. 4H]</div> <div>D10 [8. 2G]</div> <div>D11 [7. 1B]</div> <div>D502 [10. 3G]</div> <div>G1 [2. 3F]</div> <div>G1 [3. 3D]</div> <div>G1 [6. 4D 6. 1D 6. 3D]</div> <div>G1 [7. 4F 7. 2C]</div> <div>G1 [8. 4D 8. 2D]</div> <div>G1 [10. 3D]</div> <div>G1 [11. 2B 11. 3D 11. 3G]</div> <div>L1 [12. 2E]</div> <div>L2 [12. 2E]</div> <div>L3 [12. 2E]</div> <div>L4 [13. 4E]</div> <div>LB1 [7. 3C]</div> <div>LB2 [8. 4A]</div> <div>LB3 [8. 3B]</div> <div>LB502 [6. 1B]</div> <div>LB503 [11. 3B]</div> <div>LB504 [7. 1E]</div> <div>LB505 [8. 2B]</div> <div>LB506 [2. 4H]</div> <div>LB507 [6. 2A]</div> <div>LB508 [8. 2A]</div> <div>LB509 [7. 2D]</div> <div>LB1502 [3. 4G]</div> <div>M1001 [4. 3B 4. 3E 4. 2B]</div> <div>M1002 [5. 3D 5. 2B 5. 3C]</div> <div>M1501 [4. 3D 4. 3C 4. 2E]</div> <div>M1502 [5. 2E 5. 3B 5. 3E]</div> <div>MEC1 [14. 5F 14. 5F]</div> <div>MEC2 [14. 5D 14. 5D 14. 5D 14. 4D]</div> <div>O1 [7. 2D]</div> <div>O2 [7. 2C]</div> <div>O3 [12. 2D]</div> <div>O4 [12. 2D]</div> <div>O5 [8. 4H]</div> <div>O6 [8. 1E 8. 1E]</div> <div>O7 [8. 1F]</div> <div>O8 [14. 4B]</div> <div>O9 [14. 4B]</div> <div>O13 [8. 3B]</div> <div>O14 [8. 4B]</div> <div>O501 [13. 4D]</div> <div>O502 [12. 4C]</div> <div>O503 [13. 3D]</div> <div>O504 [12. 4C]</div> <div>O505 [10. 2E 10. 2E]</div> <div>O506 [10. 2F]</div> <div>O507 [7. 3B]</div> <div>O508 [7. 2B]</div> <div>O509 [7. 3A]</div> <div>O510 [7. 2A]</div> <div>O511 [7. 2B]</div> <div>R1 [7. 2C]</div> <div>R2 [2. 5G]</div> <div>R3 [7. 4G]</div> <div>R4 [7. 2B]</div> <div>R5 [11. 3D]</div> <div>R6 [7. 1D]</div> <div>R7 [12. 3D]</div> <div>R8 [11. 5A]</div> <div>R9 [11. 2D]</div> <div>R10 [11. 2D]</div> <div>R11 [11. 2D]</div> <div>R12 [11. 4C]</div> <div>R13 [11. 5C]</div> <div>R14 [11. 5D]</div> <div>R15 [11. 4E]</div> <div>R16 [8. 3C]</div> <div>R17 [8. 3G]</div> <div>R18 [13. 2C]</div> <div>R19 [13. 2C]</div> <div>R20 [8. 3G]</div> <div>R21 [11. 1D]</div> <div>R22 [8. 3G]</div> <div>R23 [8. 4G]</div> <div>R24 [8. 4G]</div> <div>R25 [6. 2E]</div> <div>R26 [6. 2E]</div> <div>R27 [6. 2E]</div>		<div>R28 [8. 4G]</div> <div>R29 [8. 2C]</div> <div>R30 [11. 4E]</div> <div>R31 [13. 2A]</div> <div>R32 [13. 1A]</div> <div>R33 [10. 4F]</div> <div>R34 [6. 4C]</div> <div>R35 [2. 5H]</div> <div>R36 [10. 3E]</div> <div>R37 [10. 4E]</div> <div>R38 [12. 3E]</div> <div>R39 [10. 3B]</div> <div>R40 [14. 4B]</div> <div>R41 [14. 5B]</div> <div>R42 [13. 4D]</div> <div>R43 [2. 5C]</div> <div>R44 [8. 4G]</div> <div>R45 [14. 5C]</div> <div>R46 [8. 4G]</div> <div>R47 [8. 1F]</div> <div>R48 [8. 1F]</div> <div>R49 [8. 2E]</div> <div>R50 [10. 2E]</div> <div>R51 [10. 3E]</div> <div>R52 [10. 2E]</div> <div>R53 [10. 3E]</div> <div>R54 [10. 2G]</div> <div>R55 [10. 2G]</div> <div>R56 [10. 2G]</div> <div>R57 [14. 1B]</div> <div>R58 [10. 2G]</div> <div>R59 [14. 1C]</div> <div>R60 [11. 2A]</div> <div>R61 [11. 2A]</div> <div>R62 [14. 1B]</div> <div>R63 [14. 2B]</div> <div>R64 [14. 2B]</div> <div>R65 [14. 3B]</div> <div>R66 [14. 1B]</div> <div>R67 [14. 2B]</div> <div>R68 [14. 2B]</div> <div>R69 [14. 3B]</div> <div>R70 [14. 1B]</div> <div>R71 [14. 2B]</div> <div>R72 [14. 2B]</div> <div>R73 [14. 3B]</div> <div>R74 [7. 4F]</div> <div>R75 [10. 4G]</div> <div>R76 [10. 4H]</div> <div>R77 [8. 1G]</div> <div>R78 [7. 1B]</div> <div>R79 [8. 2G]</div> <div>R80 [8. 1F]</div> <div>R81 [8. 1F]</div> <div>R82 [4. 3C]</div> <div>R83 [5. 4G]</div> <div>R84 [8. 2F]</div> <div>R86 [7. 4G]</div> <div>R87 [8. 2F]</div> <div>R89 [11. 2D]</div> <div>R90 [11. 2E]</div> <div>R93 [11. 2A]</div> <div>R94 [14. 4B]</div> <div>R95 [14. 4B]</div> <div>R96 [14. 4C]</div> <div>R504 [13. 4E]</div> <div>R505 [13. 4E]</div> <div>R506 [13. 5E]</div> <div>R507 [13. 4A]</div> <div>R509 [13. 4B]</div> <div>R511 [13. 4C]</div> <div>R513 [13. 4B]</div> <div>R514 [13. 3B]</div> <div>R515 [9. 4B]</div> <div>R516 [13. 3A]</div> <div>R517 [13. 3C]</div> <div>R521 [12. 4B]</div> <div>R522 [12. 5B]</div> <div>R523 [12. 4B]</div> <div>R524 [12. 4D]</div> <div>R525 [12. 3D]</div> <div>R529 [12. 4C]</div> <div>R530 [12. 4C]</div> <div>R531 [12. 3D]</div> <div>R532 [10. 4G]</div> <div>R534 [12. 2A]</div> <div>R535 [12. 2B]</div> <div>R536 [12. 5B]</div> <div>R538 [10. 3G]</div> <div>R539 [12. 2A]</div> <div>R540 [12. 4C]</div> <div>R541 [12. 2B]</div> <div>R542 [12. 4B]</div> <div>R543 [12. 3B]</div> <div>R545 [7. 2F]</div> <div>R549 [6. 3C]</div>		<div>R550 [12. 3A]</div> <div>R551 [6. 3E]</div> <div>R554 [12. 2C]</div> <div>R555 [6. 3E]</div> <div>R556 [10. 3B]</div> <div>R558 [6. 3E]</div> <div>R559 [10. 3H]</div> <div>R560 [6. 1C]</div> <div>R561 [10. 4F]</div> <div>R562 [12. 2C]</div> <div>R563 [10. 3B]</div> <div>R564 [10. 3B]</div> <div>R565 [10. 4F]</div> <div>R566 [10. 3B]</div> <div>R567 [10. 2E]</div> <div>R568 [7. 2A]</div> <div>R569 [10. 2D]</div> <div>R570 [10. 3H]</div> <div>R571 [11. 2C]</div> <div>R572 [7. 3B]</div> <div>R573 [10. 2D]</div> <div>R575 [10. 2E]</div> <div>R576 [10. 2H]</div> <div>R577 [10. 2H]</div> <div>R578 [10. 3E]</div> <div>R579 [10. 3E]</div> <div>R581 [10. 2D]</div> <div>R584 [10. 4C]</div> <div>R585 [10. 2B]</div> <div>R586 [10. 2B]</div> <div>R587 [10. 4C]</div> <div>R590 [10. 4B]</div> <div>R591 [10. 4B]</div> <div>R592 [10. 4C]</div> <div>R593 [10. 4B]</div> <div>R594 [10. 4C]</div> <div>R595 [10. 4D]</div> <div>R1077 [3. 4E]</div> <div>R1078 [3. 4E]</div> <div>R1079 [3. 4E]</div> <div>R1080 [3. 5B]</div> <div>R1081 [3. 5B]</div> <div>R1091 [4. 3H]</div> <div>R1092 [3. 3F]</div> <div>R1093 [5. 2C]</div> <div>R1095 [4. 3G]</div> <div>R1096 [4. 3G]</div> <div>R1097 [5. 3C]</div> <div>R1098 [3. 3F]</div> <div>R1587 [4. 3C]</div> <div>R1588 [5. 4G]</div> <div>R1589 [4. 2C]</div> <div>R1591 [5. 4G]</div> <div>R1592 [5. 3H]</div> <div>R1596 [3. 4F]</div> <div>RP1 [7. 4F 7. 4G 7. 4G 7. 4G]</div> <div>TP2 [2. 4G]</div> <div>TP4 [10. 3B]</div> <div>TP5 [10. 3B]</div> <div>TP6 [10. 3B]</div> <div>TP7 [10. 3B]</div> <div>TP8 [10. 3B]</div> <div>U1 [11. 1E]</div> <div>U2 [10. 2C]</div> <div>U3 [11. 2E]</div> <div>U4 [11. 5D]</div> <div>U5 [13. 2B]</div> <div>U501 [13. 4B]</div> <div>U502 [12. 2B]</div> <div>Y1 [11. 4D]</div>					
1		2		3		4		5							
2		3		4		5									
3		4		5											
4		5													
5															

ASSEMBLY

NB9M-GS G98M 77400MHz, 256MB(64bi t) GDDR2 32Mx16 84FBGA, LVDS + HDMI + SD/HD(TV_OUT) + VGA

PAGE DETAIL

<edit here to insert page detail>

NVidia Corporation

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV_PN

600-10621-0001-000 A

ID

p621

PAGE

16 Of 16

NAME

Thorsten Freund

DATE

13-SEP-2007

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

ASSEMBLY

NB9M-GS G98M 7/400MHz, 256MB(64bit) GDDR2 32Mx16 84FBGA, LVDS + HDMI + SD/HD(TV_OUT) + VGA

PAGE DETAIL

<edit here to insert page detail>

NV_PN

600-10621-0001-000 A

ID

p621

PAGE

16 OF 16

NAME

Thorsten Freund

DATE

13-SEP-2007