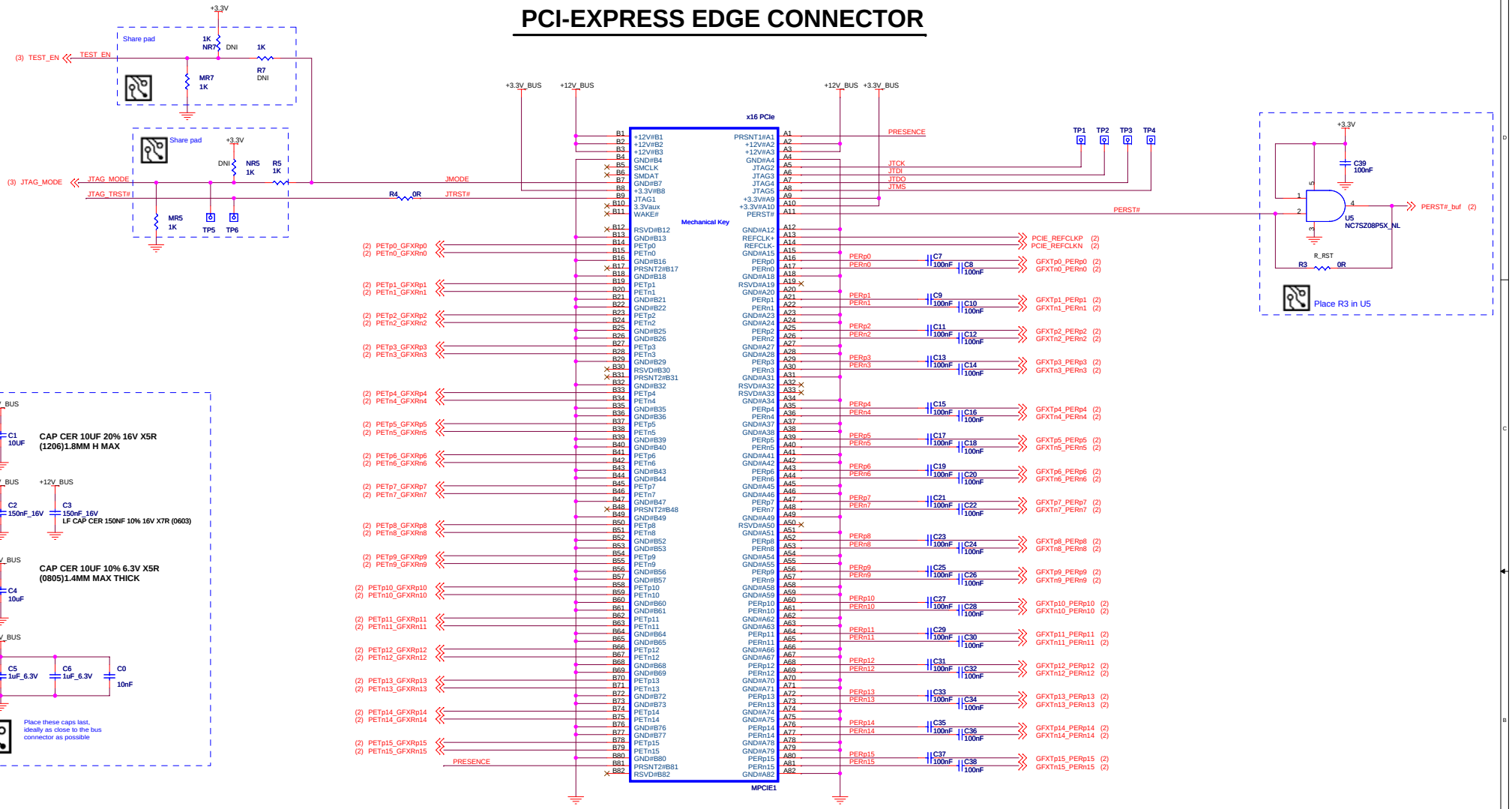
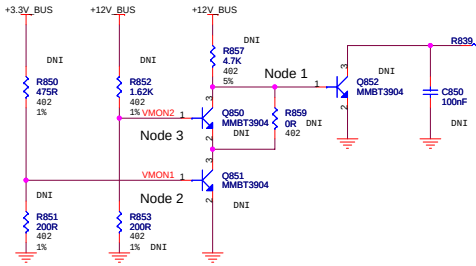
PCI-EXPRESS EDGE CONNECTOR





Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.

Node 1 When +12V_BUS ramps above min Vbe, SMPS_EN will be held low

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

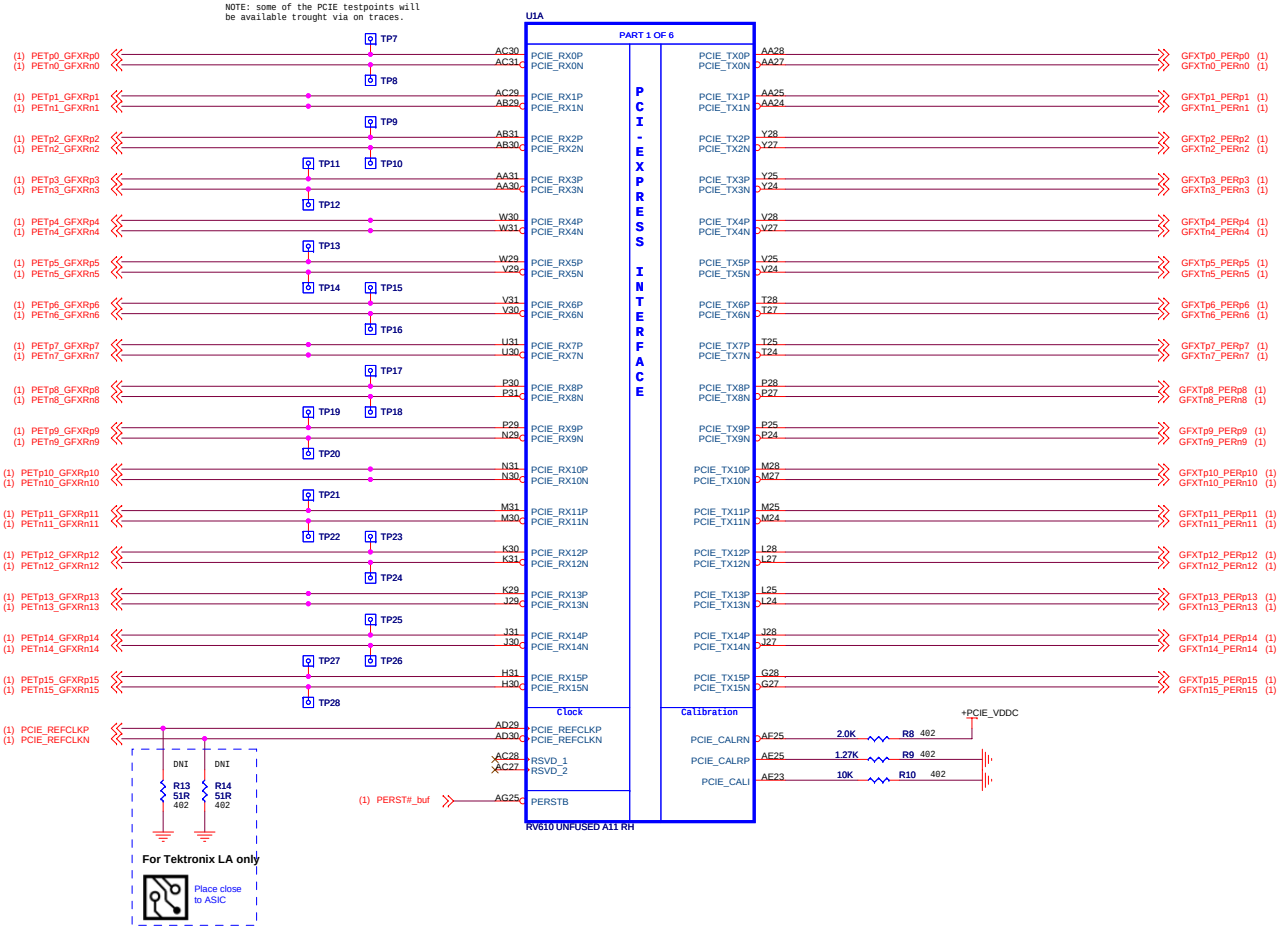
Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

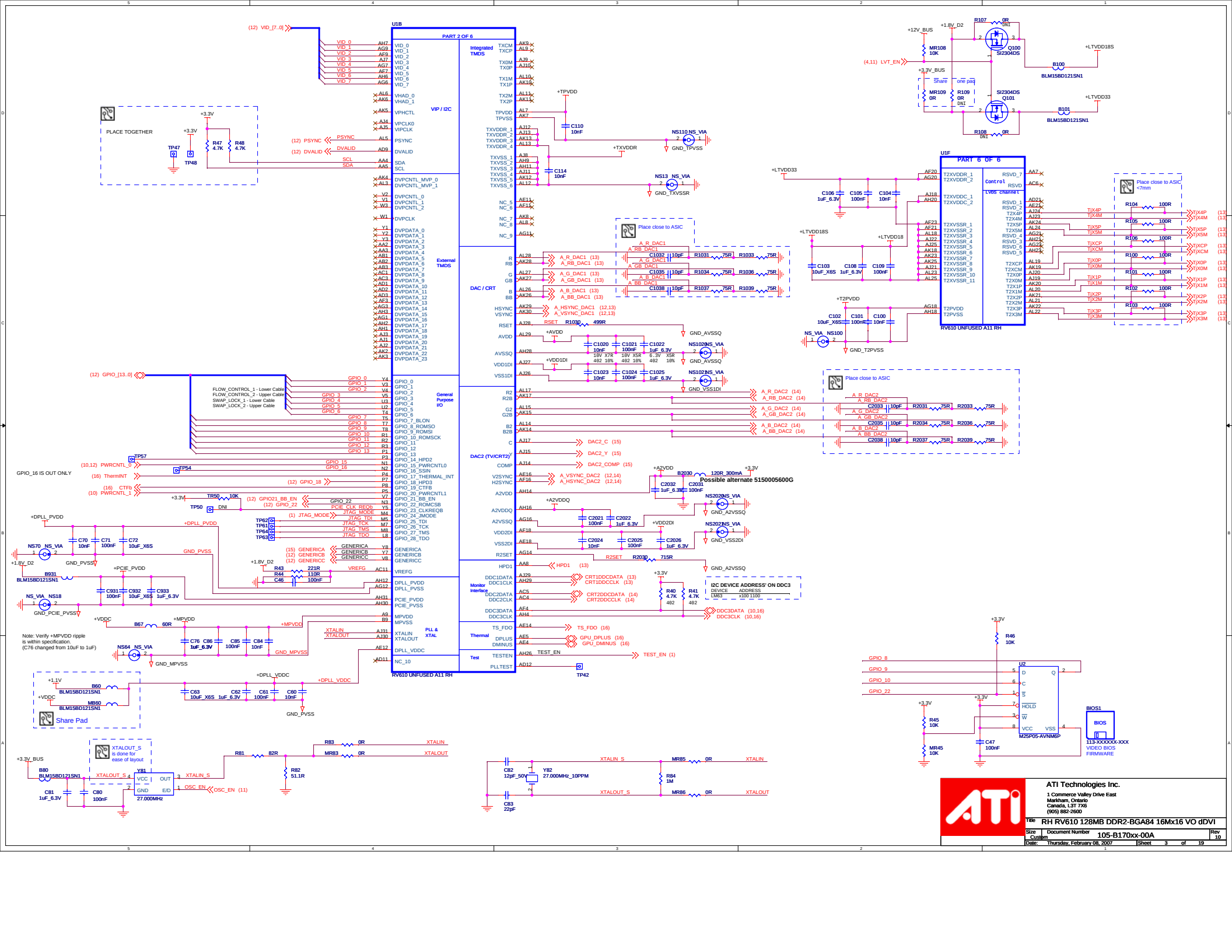
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

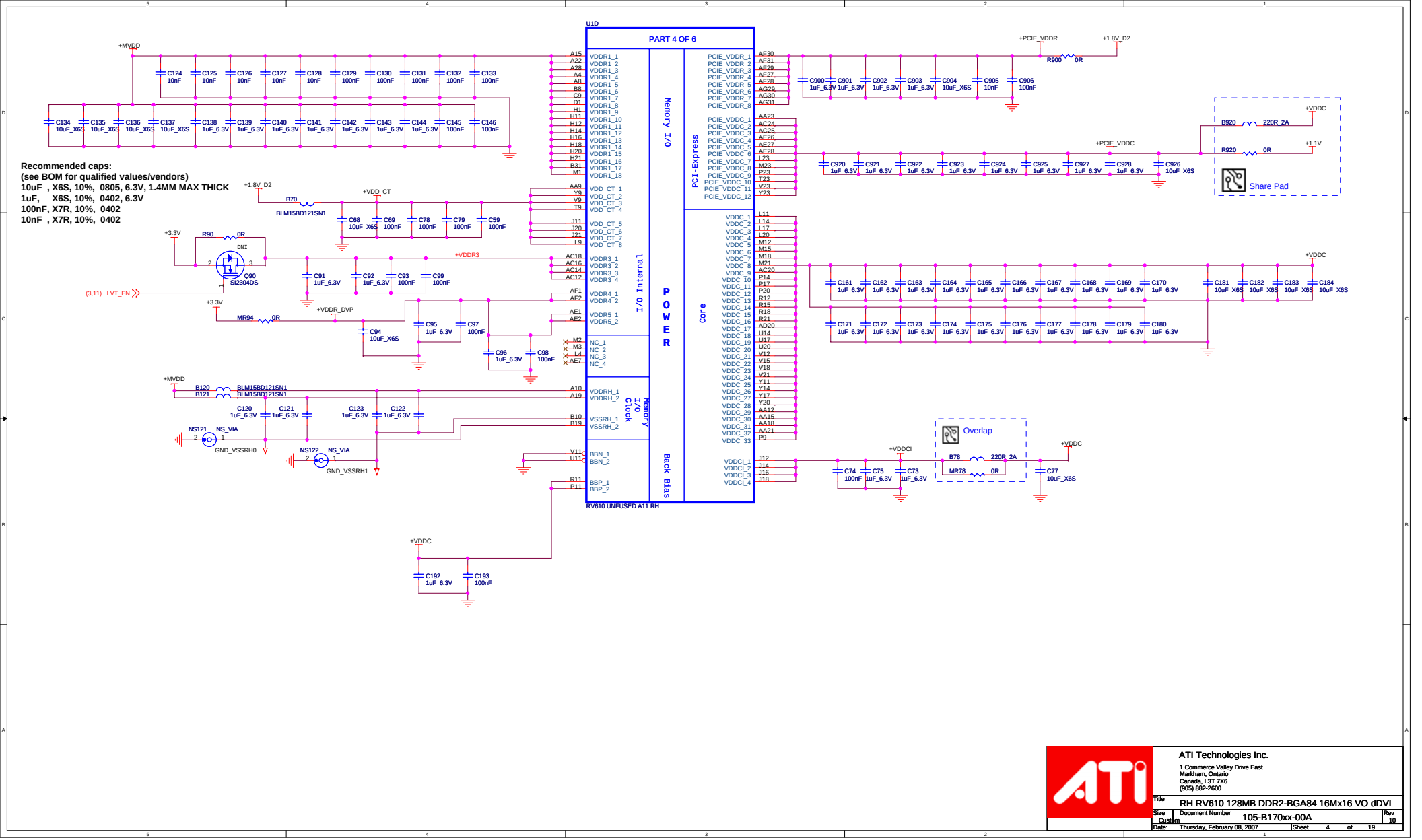
Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI		
Size C	Document Number 105-B170xx-00A		Rev 10
Date: Thursday, February 08, 2007		Sheet 1 of 19	



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

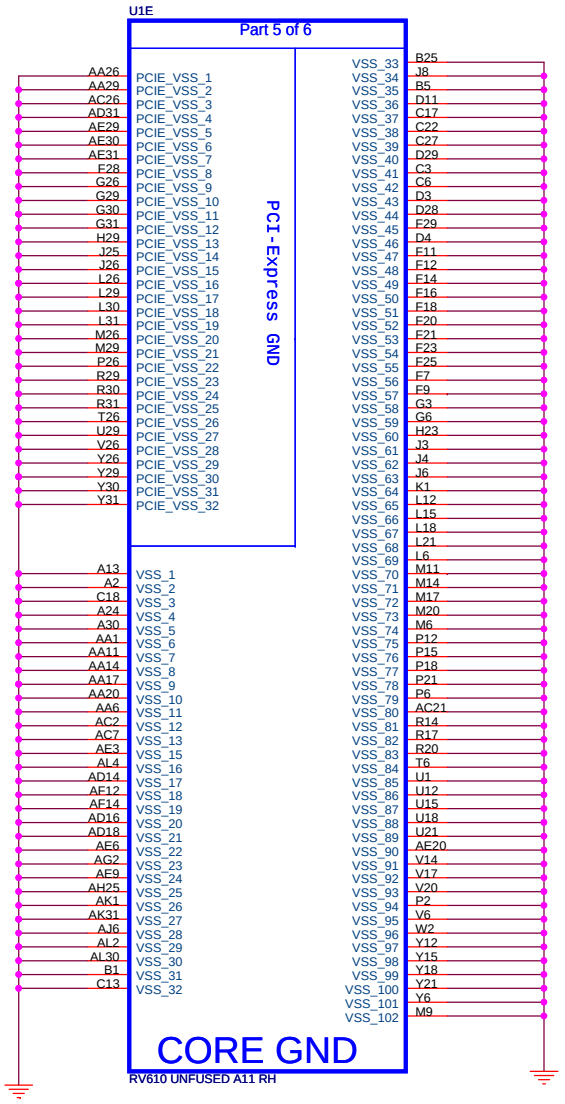
Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI		
Size C	Document Number 105-B170xx-00A		Rev 10
Date: Thursday, February 08, 2007	Sheet 2 of 19		


U1B
PART 2 OF 6
VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
VID_7
VIP / I2C
Integrated TMDS
External TMDS
DAC / CRT
DAC2 (TV/CRT2)
General Purpose I/O
Monitor Interface
Thermal
Test
PLL & XTAL
RV610 UNFUSED A11 RH
U1F
PART 6 OF 6
Control
LVDS channel
RV610 UNFUSED A11 RH
PLACE TOGETHER
Share Pad
Share one pad
I2C DEVICE ADDRESS' ON DDC3
Possible alternate 5150005600G
GPIO_16 IS OUT ONLY
Note: Verify +MPVDD ripple is within specification. (C76 changed from 10uF to 1uF)
XTALOUT_S is done for ease of layout
Place close to ASIC
Place close to ASIC <7mm
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600
RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI
105-B170xx-00A
Thursday, February 08, 2007
Sheet 3 of 19



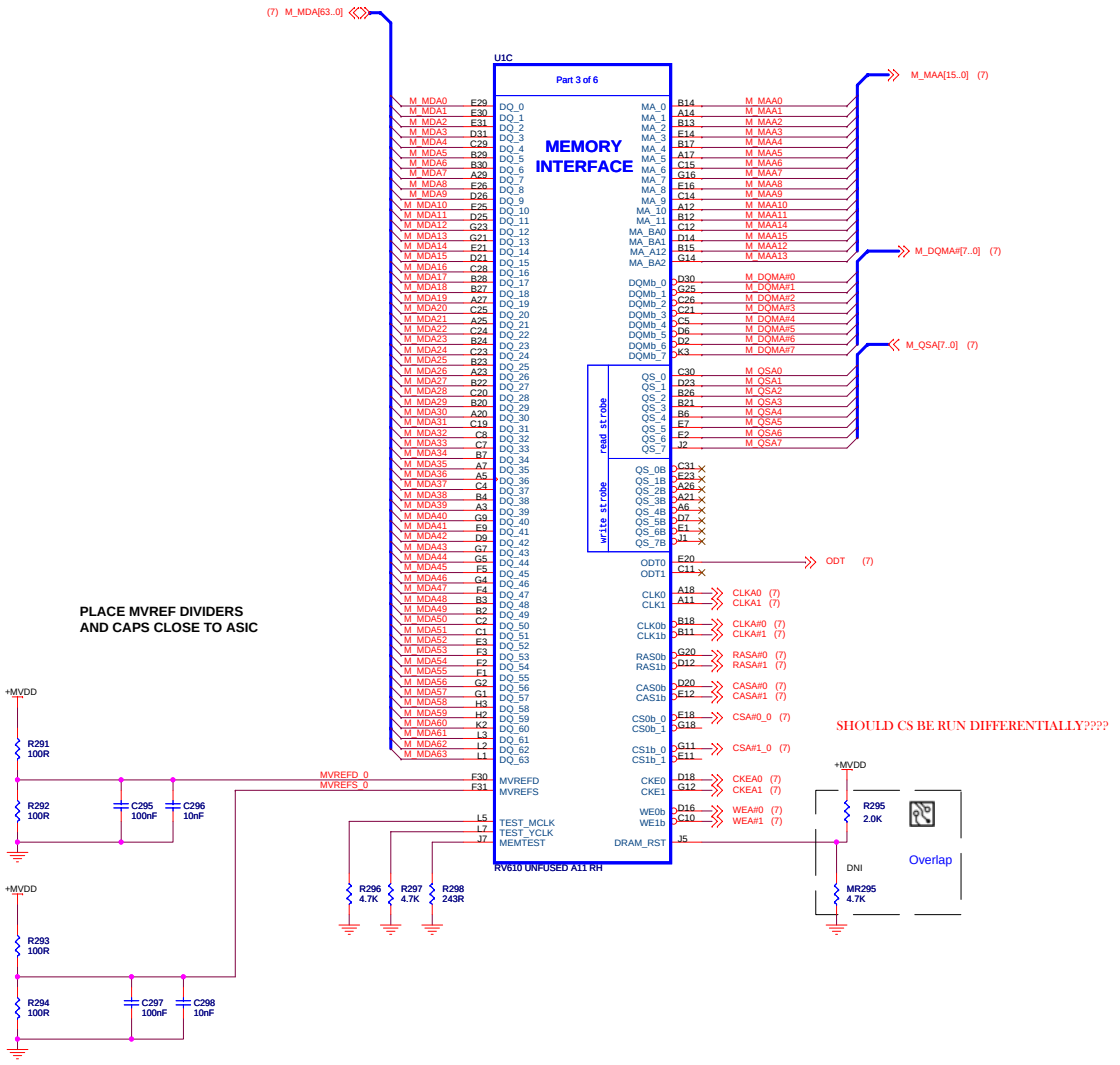
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI	
Size: Custom	Document Number: 105-B170xx-00A	Rev: 10
Date: Thursday, February 08, 2007	Sheet 4 of 19	



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI	
Size B	Document Number 105-B170xx-00A	Rev 10
Date: Thursday, February 08, 2007	Sheet 5 of 19	

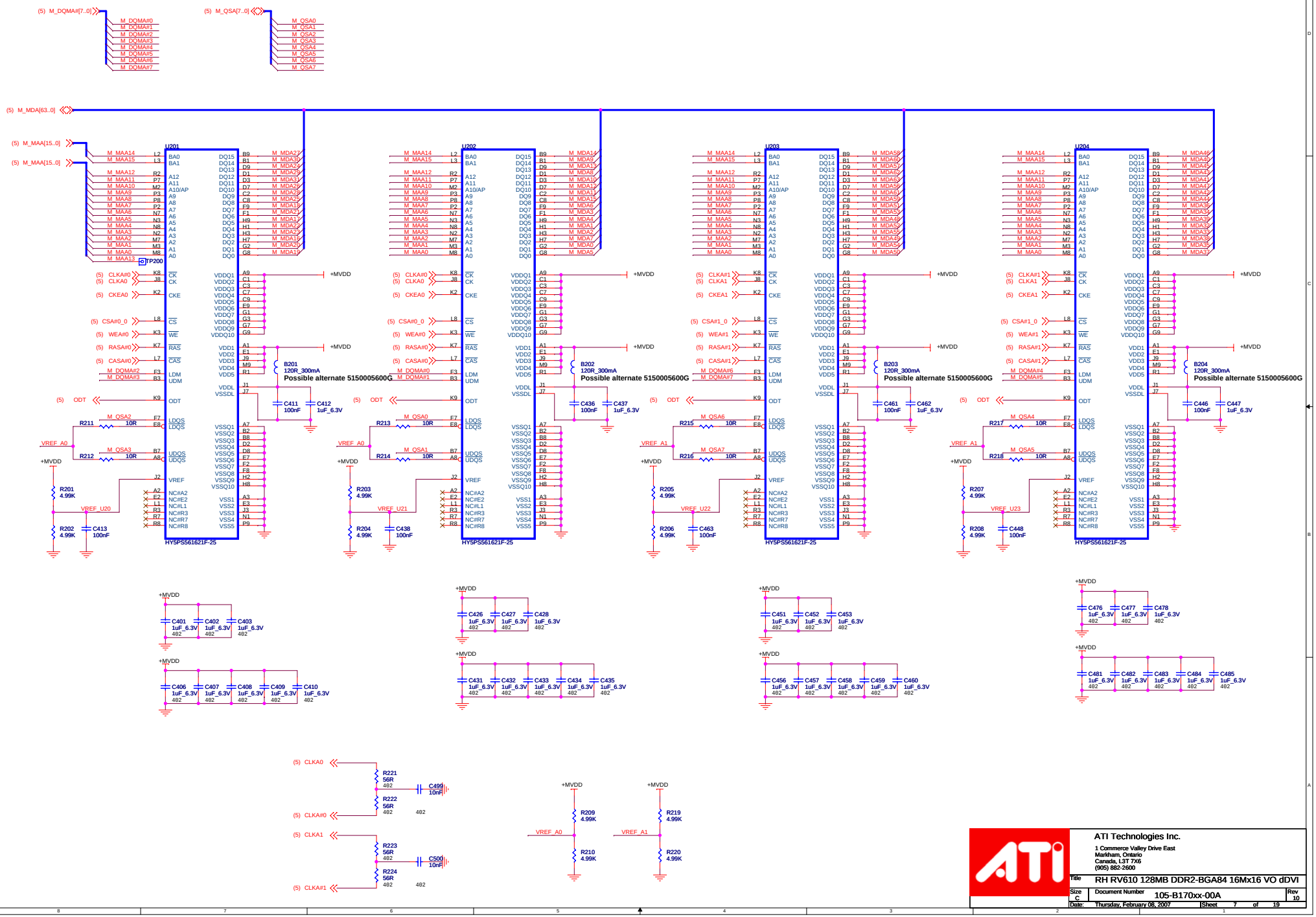


DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

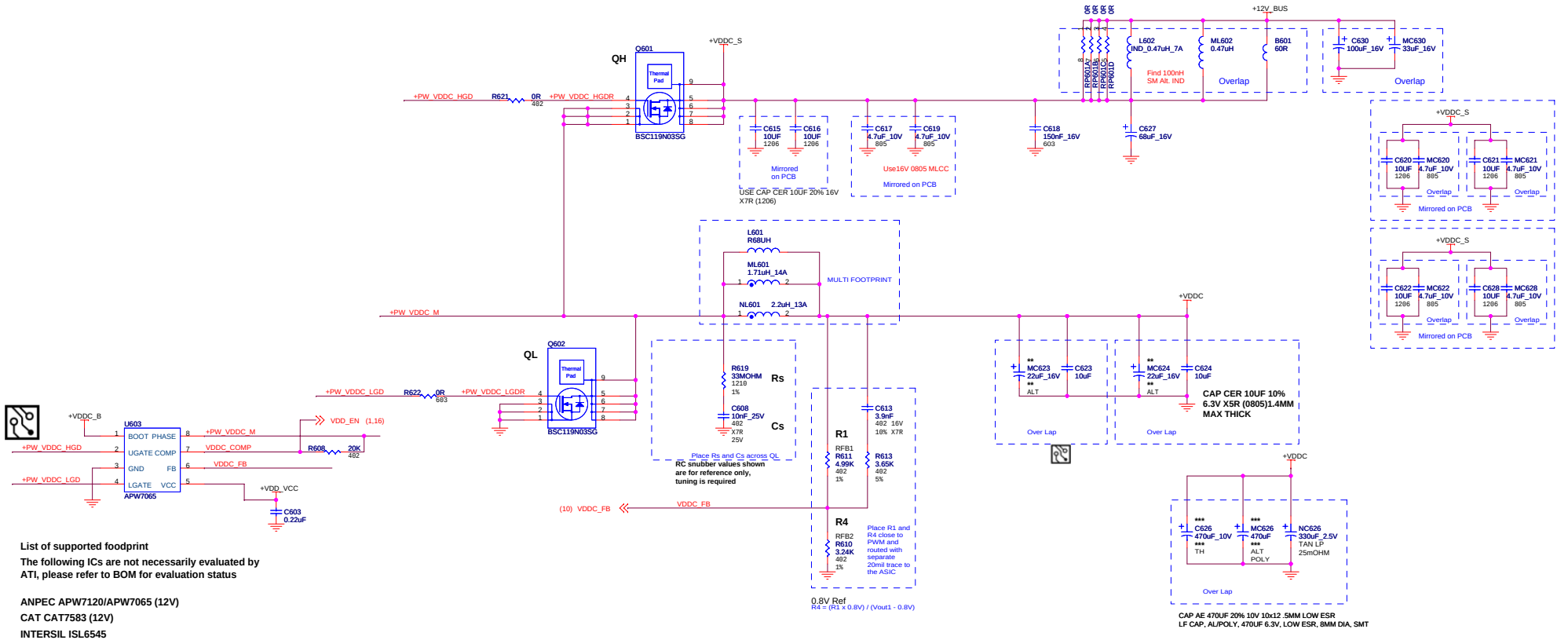
Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI		
Size C	Document Number 105-B170xx-00A		Rev 10
Date: Thursday, February 08, 2007	Sheet 6 of 19		

CHANNEL A: RANK 0 128MB DDR2



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI	
Size C	Document Number 105-B170xx-00A	Rev 10
Date: Thursday, February 08, 2007	Sheet 7 of 19	



List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7120/APW7065 (12V)
CAT CAT7583 (12V)
INTERSIL ISL6545
NEXSEM NX2114/2307
RICHTEK RT9214/RT8101
OnSemi ON1582
uPI UP6101 (No Ext_Vref in)

Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

SMPS02- Regulator for VDDC

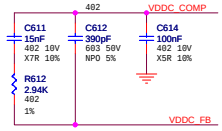
Vout = 0.9V ~ 1.1V

Part	Vout	RFB1	RFB2
0.8V Ref	1.1V (1.98V~2.08V)	200R p/n 3160200000G	511R p/n 3160511000G

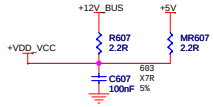
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

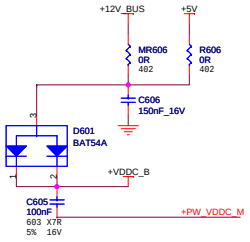
COMPENSATION CIRCUIT



FILTERED SMPS VCC

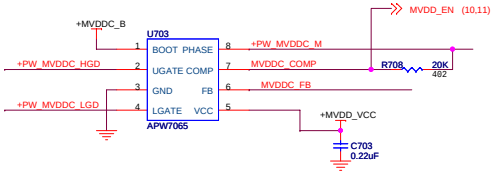


BOOT CIRCUIT



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title: RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI
Size: Custom | Document Number: 105-B170xx-00A | Rev: 10
Date: Thursday, February 08, 2007 | Sheet 8 of 19

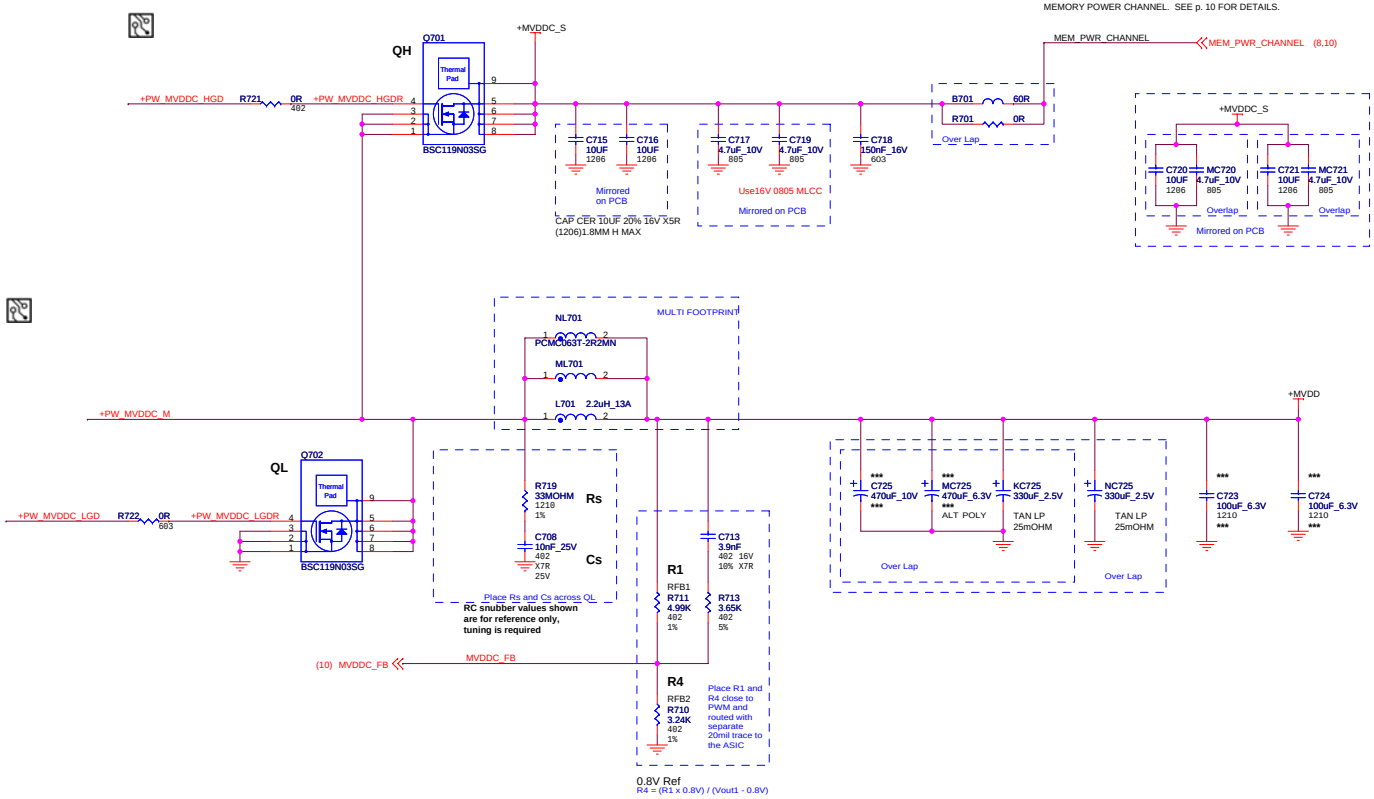


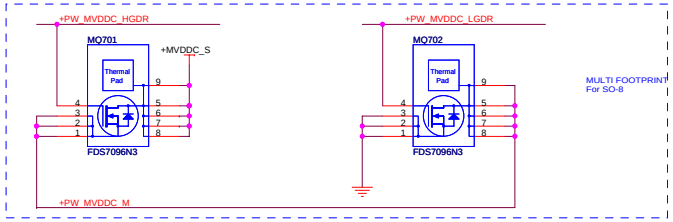
List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

- **ANPEC APW7120/APW7065 (12V)**
- **CAT CAT7583 (12V)**
- **INTERSIL ISL6545**
- **NEXSEM NX2114/2307**
- **RICHTEK RT9214/RT8101**
- **OnSemi ON1582**
- **uPI UP6101 (No Ext_Vref in)**
- **uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**

MEMORY POWER CHANNEL. SEE p. 10 FOR DETAILS.





SMPS02- Regulator for MVDD

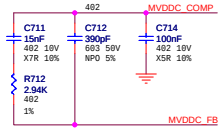
Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G
	1.8V (1.78V~1.86V)	4.99K p/n 3160499100G	3.92K p/n 3160392100G

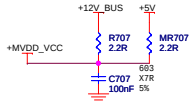
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

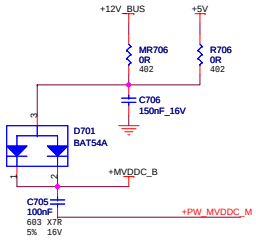
NSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

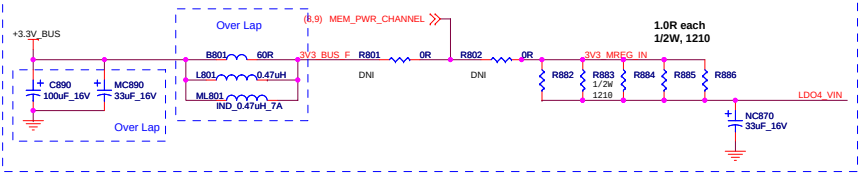
Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI	
Size: Custom	Document Number: 105-B170xx-00A	Rev: 10
Date: Thursday, February 08, 2007	Sheet 9 of 19	

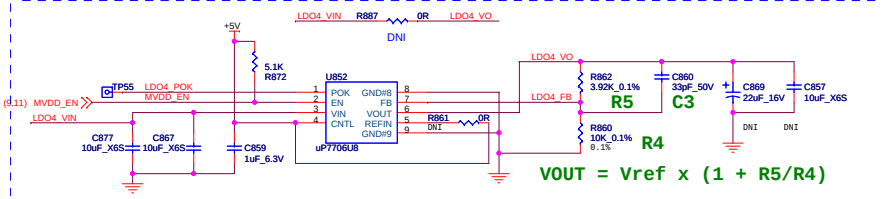
Linear Regulator for +MVDD
Vout = 1.8V ~ 2.1V
Iout = 2.75A MAX
P_REG = 1.35W
Tj(rise)max = 1.35Wx50C/W(50~70mm sq. Cu) = 67.5C

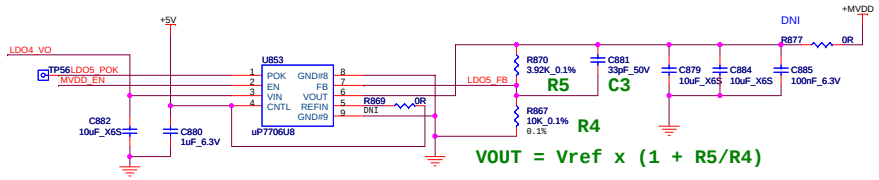
MEM PWR INPUT	INSTALL	DO NOT INSTALL
3.3V BUS (3V3_BUS_F)	R801 R802	R602 R701
12V (+VDDC_S)	R602 R701	R801 R802

Req = 1R/5 = 0.2R
P_Req = 0.2R * 2.75^2 = 1.5W
P_Reach = 1.5W/5 = 300mW < 500mW * 70%

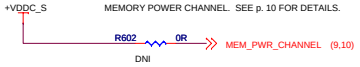
MEMORY POWER CHANNEL TO EASE LAYOUT CONGESTION OF LP BOARD. MEMORY POWER CHANNEL CAN BE USED TO DELIVER SOURCE VOLTAGE TO MVDD SMPS OR LINEAR REGULATORS (12V IN OR 3.3V IN)

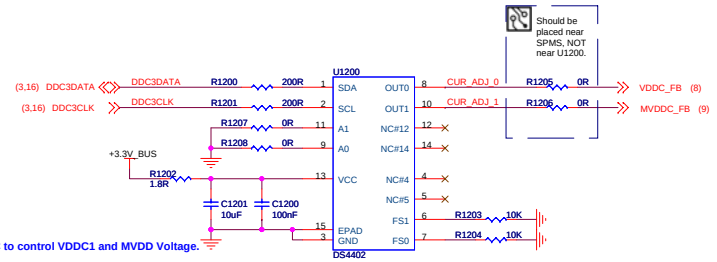






Memory Power Channel
Source Selection

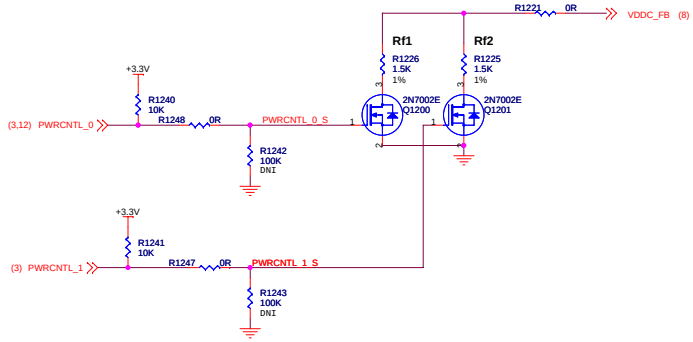




ASIC GPIO(x2) to control VDDC Voltage.

VDDC Voltage Settings Using GPIOs

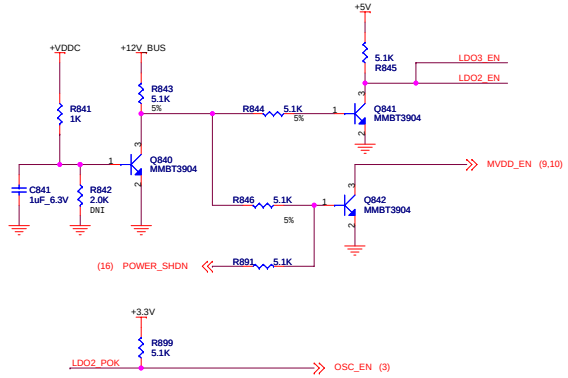
PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0	0				
0	1				
1	0				
1	1	1 0	1		Power-up Default

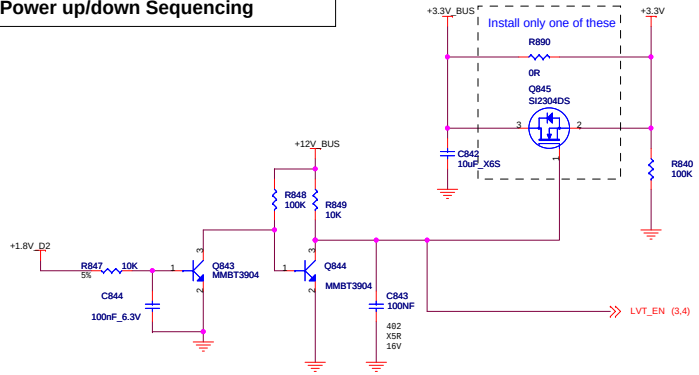


ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

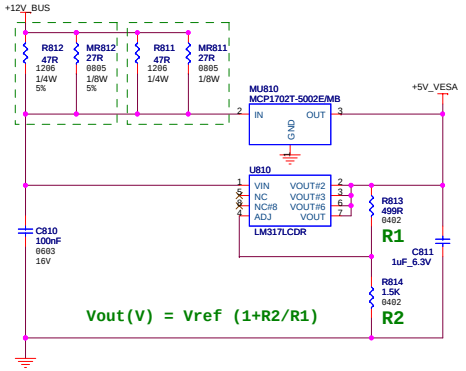
Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI	
Size: Custom	Document Number: 105-B170xx-00A	Rev: 10
Date: Thursday, February 08, 2007	Sheet 10 of 19	

Power up/down Sequencing



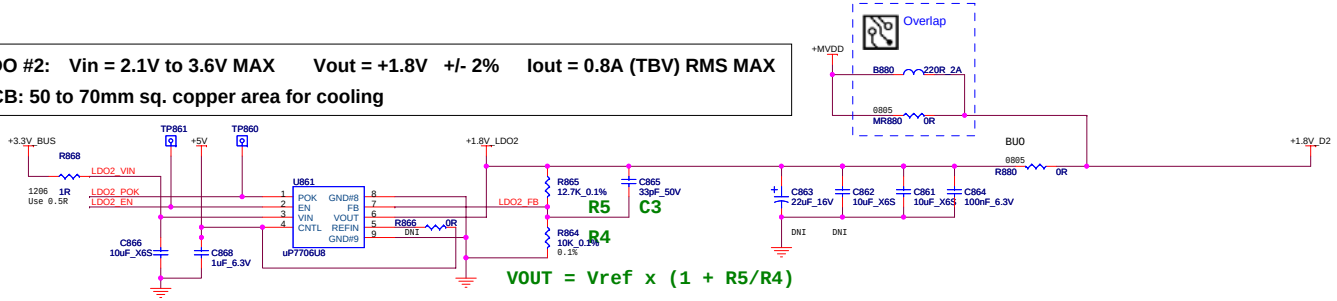


Regulators for +5V, +5V_VESA and +5V_VESA2



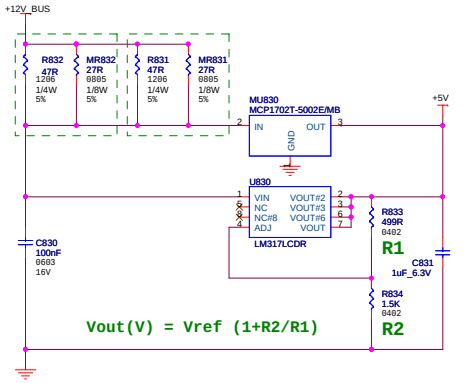
LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



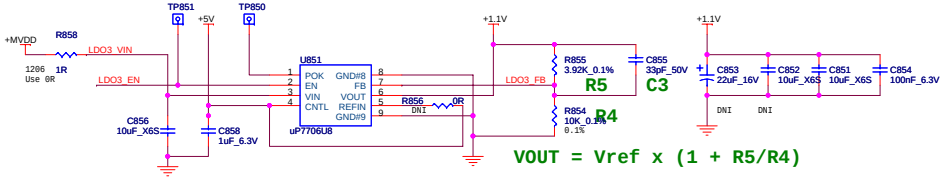
VOUT = Vref x (1 + R5/R4)

R868 (0.5R 1/2W or 0R 1206), R864, R865 & C865: To Be Verified



LDO #3: Vin = +1.45V to 2.1VMAX Vout = +1.1V +/- 2% Iout = 1.1A (TBV) RMS MAX

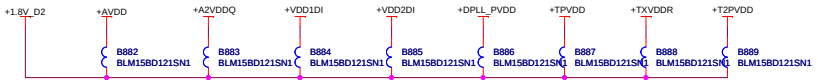
PCB: 50 to 70mm sq. copper area for cooling



VOUT = Vref x (1 + R5/R4)

R854, R855 (3.92K) & C855: To Be Verified

Shared Power Rails



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI	
Size C	Document Number 105-B170xx-00A	Rev 10
Date: Thursday, February 08, 2007	Sheet 11 of 19	

PIN BASED STRAPS

+3.3V

DNI	MR50	10K	R50	10K	GPIO_0	GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
DNI	MR51	10K	R51	10K	GPIO_1	GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)
DNI	MR52	10K	R52	10K	GPIO_2	
DNI	MR53	10K	R53	10K	GPIO_3	GPIO(3:2) - ATI Internal Use Only - Reserved (Default: 00)
DNI	MR54	10K	R54	10K	GPIO_4	GPIO(4) - DEBUG_ACCESS ATI Internal Use Only - Reserved (Default: 0)
DNI	MR55	10K	R55	10K	GPIO_5	GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)
DNI	MR56	10K	R56	10K	GPIO_6	GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)
NTSC	MR57	10K	R57	10K	GPIO_7	GPIO(7) - TV OUT STANDARD (Jumper position overwrite resistor settings) 0 - PAL TVO (Jumper is closed) 1 - NTSC TVO (Jumper is open)
DNI	MR58	10K	R58	10K	GPIO_8	GPIO(8) - ATI Internal Use Only - Reserved (Default: 0)
	MR59	10K	R59	10K	GPIO_9	GPIO(9,13:11) - CONFIG[3..0] IF BIOS_ROM_EN=1 [default] (GPIO_22) Atmel - AT25F512A (512 kbit)0010 AT25F1024A (1 Mbit)0011 ST Microelectronics- M25P05A (512 kbit) 0100 M25P10A (1 Mbit) 0101 M25P20 (2 Mbit) 0101 Chingis (formerly PMC) - Pm25LV512 (512 kbit) 0100 Pm25LV010 (1 Mbit) 0101 If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. (Config 3 = don't care). x000 128MB x001 256MB x010 64MB x011 32MB x100 512MB x101 1GB x110 2GB x111 4GB
	MR63	10K	R63	10K	GPIO_13	
	MR62	10K	R62	10K	GPIO_12	
	MR61	10K	R61	10K	GPIO_11	
DNI	MR65	10K	R65	10K	GENERICC	GENERICC, GENERICB - ATI Internal Use Only - Reserved (Default: 0)
DNI	MR64	10K	R64	10K	GENERICB	
	MR66	10K	R66	10K	A_VSYNC_DAC1	VSYNC - VIP_DEVICE_STRAP_EN 0: Slave VIP host port devices present (use if Theater is populated) 1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)
	MR67	10K	R67	10K	A_HSYNC_DAC1	HSYNC - ATI Internal Use Only - Reserved (Default 0)
DNI	MR68	10K	R68	10K	PSYNC	PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)
DNI	MR69	10K	R69	10K	GPIO21_BB_EN	GPIO_21 - ATI Internal Use Only - Reserved (Default: 0)
DNI	MR70	10K	R70	10K	VID_0	VID_0 - ATI Internal Use Only - Reserved (Default: 0)
DNI	MR71	10K	R71	10K	VID_1	VID_1 - MSI_DIS (Default: 0)
DNI	MR72	10K	R72	10K	VID_2	VID_2 - ATI Internal Use Only - Reserved (Default: 0)
DNI	MR73	10K	R73	10K	VID_3	VID_3 - BIF_AUDIO_EN 0 - Disable HD Audio 1- Enable HD Audio
DNI	MR74	10K	R74	10K	VID_4	VID_4 - ATI Internal Use Only - Reserved (Default: 0)
DNI	MR75	10K	R75	10K	VID_5	VID_5 - 64BAR_EN_A (Default: 0) Enable 64-bit BARS
DNI	MR76	10K	R76	10K	VID_6	VID_6:7 - ATI Internal Use Only - Reserved (Default: 00)
DNI	MR77	10K	R77	10K	VID_7	
DNI	MR80	10K	R80	10K	A_VSYNC_DAC2	VSYNC - MEMORY CONFIG ATI Board Feature I 0 = single rank memory, 1 = dual rank memory
DNI	MR79	10K	R79	10K	A_HSYNC_DAC2	HSYNC2 - ATI Internal Use Only - Reserved (Default: 0)
DNI	MR60	10K	R60	10K	DVALID	BIF_CLK_PM_EN 0 - Disable CLKREQ# power management capability 1 - Enable CLKREQ# power management capability
DNI	MR87	10K	R87	10K	PWRCNTL_0 (3,10)	GPIO_15 - FOR FUTURE EXPANSION
DNI	MR46	10K	GPIO_22		GPIO_22 (3)	GPIO_22_ROMCSb - Enable external BIOS ROM device (Default 1)
DNI	MR88	10K	R88	10K	GPIO_18 (3)	GPIO_18 - MEMORY CONFIG BANK SELECT 0 - 4 BANKS, 1 - 8 BANKS

PSYNC → PSYNC (3)
DVALID → DVALID (3)

(3) VID_[7..0]
VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
VID_7

(3) GPIO_[13..0]
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

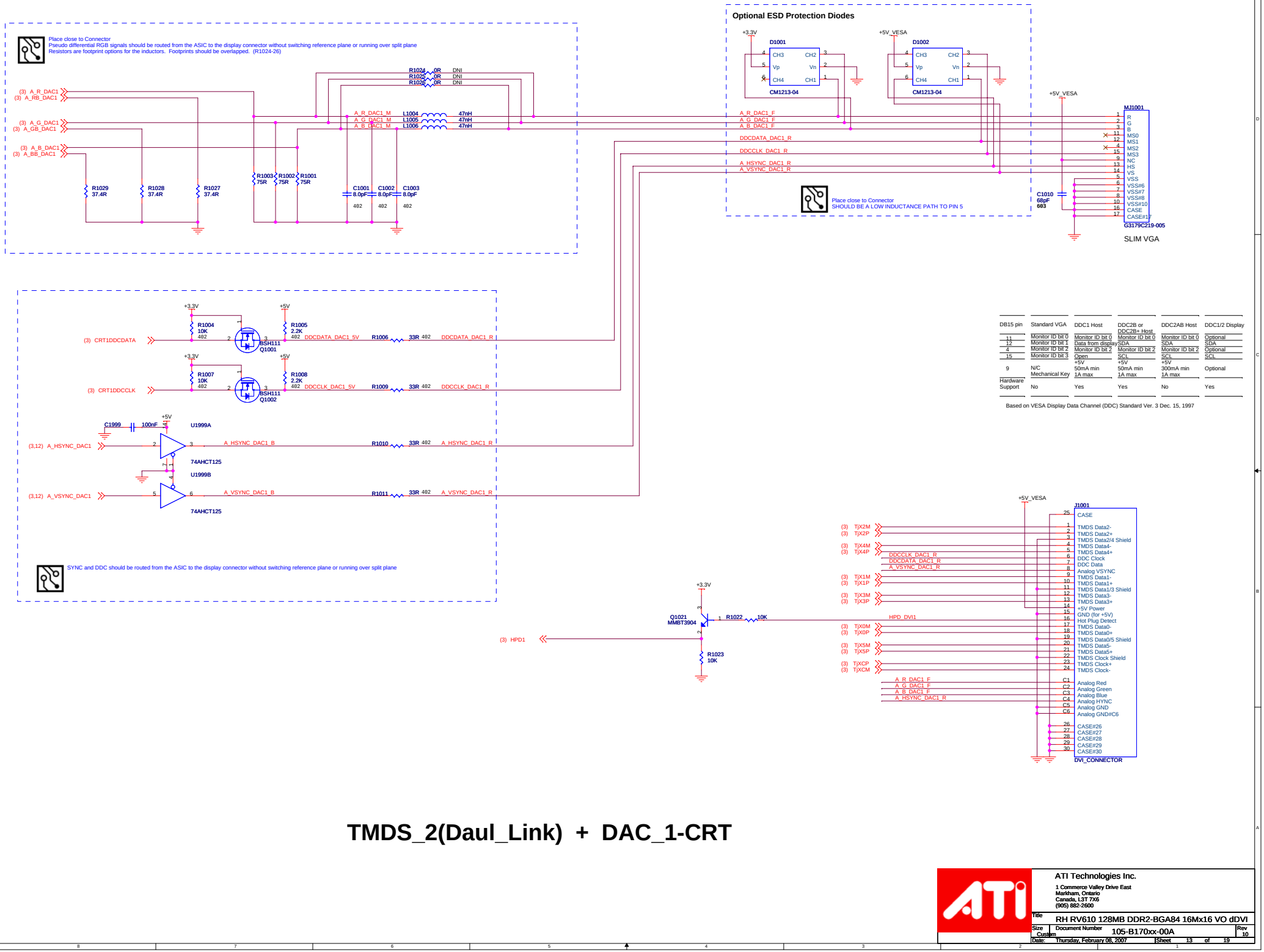
Layout

Ground — High logic voltage

Signal

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

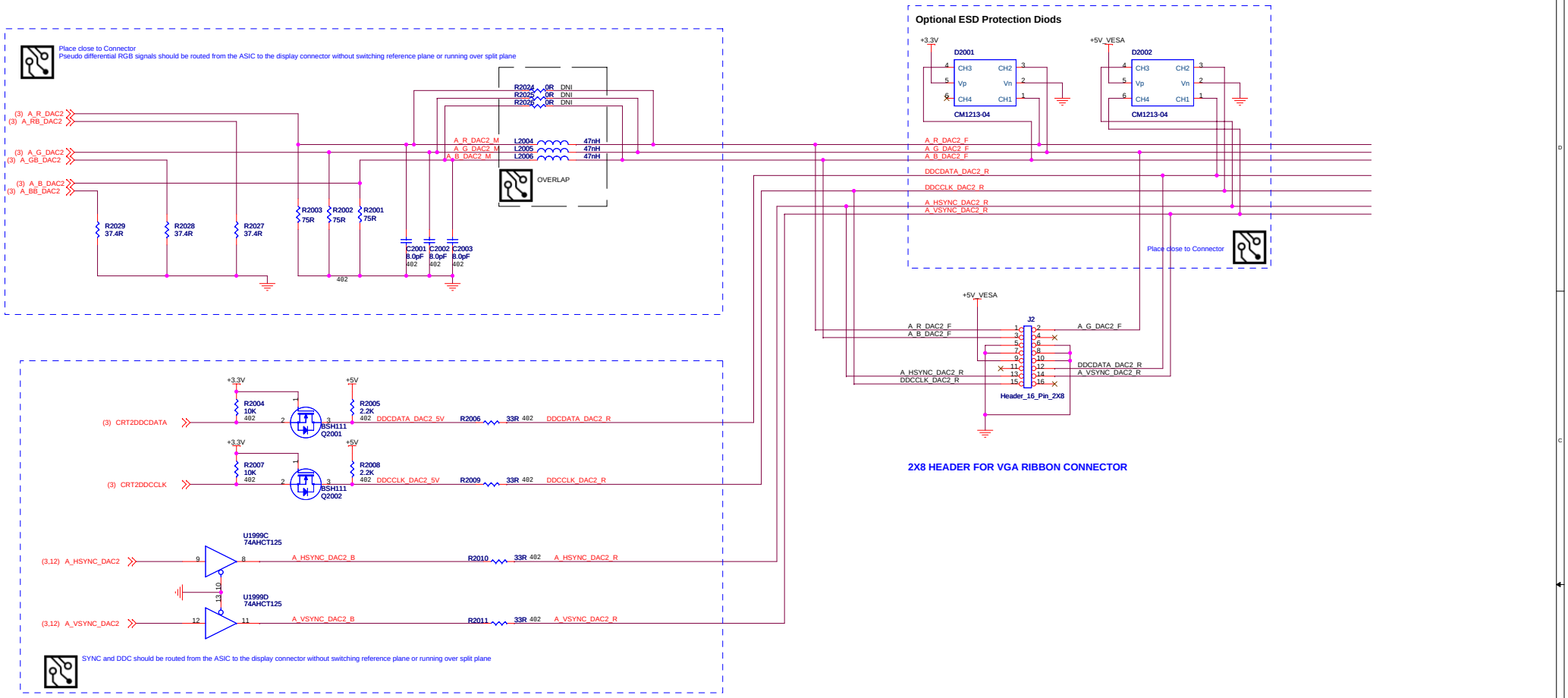
Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI		
Size: Custom	Document Number: 105-B170xx-00A		Rev: 10
Date: Thursday, February 08, 2007	Sheet 12 of 19		



TMDS_2(Daul_Link) + DAC_1-CRT

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

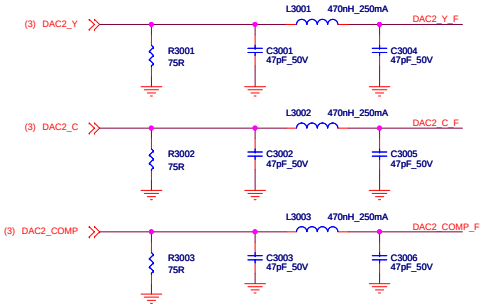
Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI	
Size: Custom	Document Number: 105-B170xx-00A	Rev: 10
Date: Thursday, February 08, 2007	Sheet 13 of 19	

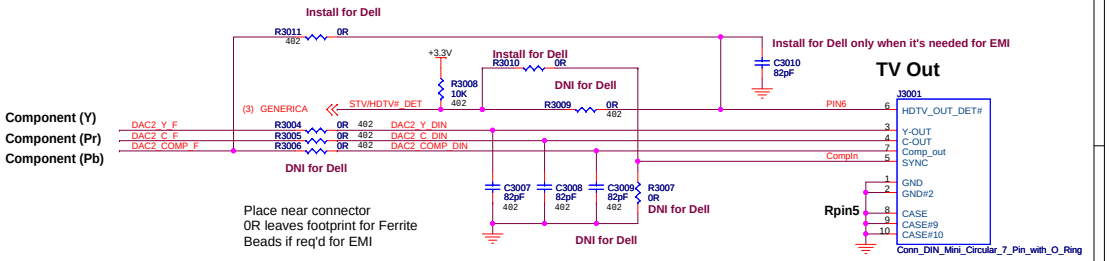


TMDS_1(Single_Link) + DAC_2-CRT

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI	
Size: Custom	Document Number: 105-B170xx-00A	Rev: 10
Date: Thursday, February 08, 2007	Sheet 14 of 19	



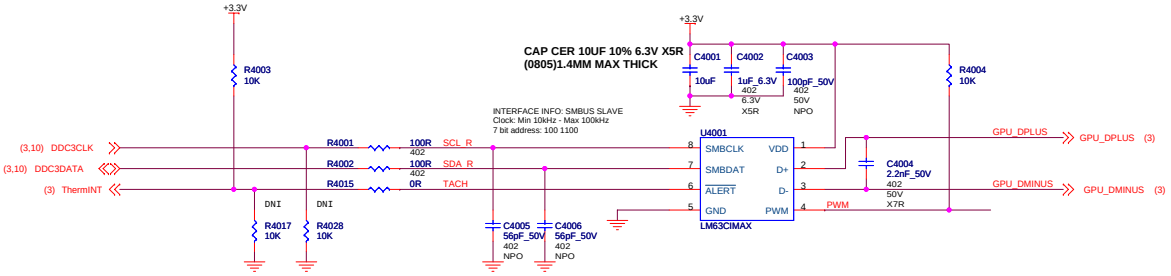


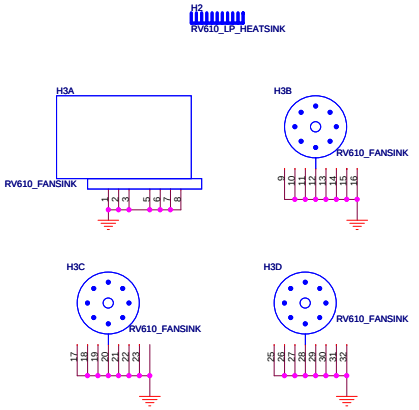
The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

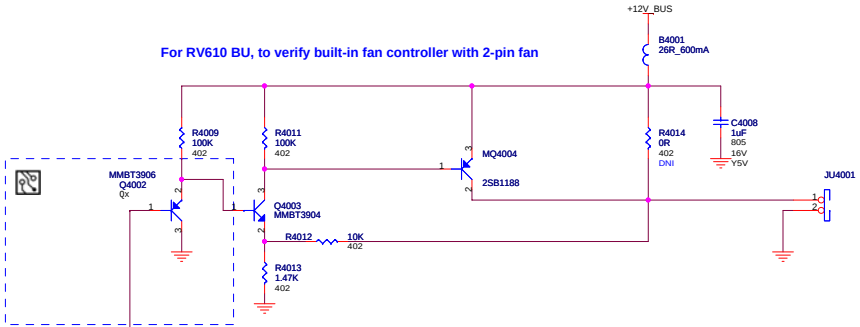
Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI	
Size C	Document Number 105-B170xx-00A	Rev 10
Date: Thursday, February 08, 2007	Sheet 15 of 19	

LM63 is for RV610 BU, until built-in fan controller is verified.

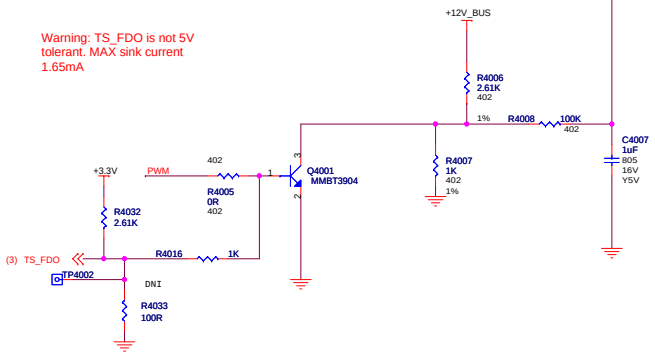




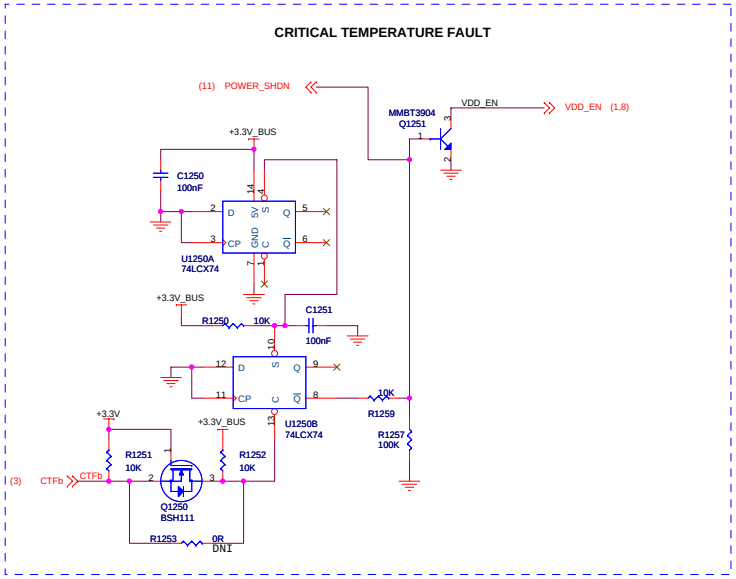
For RV610 BU, to verify built-in fan controller with 2-pin fan



Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA



CRITICAL TEMPERATURE FAULT



ATI Technologies Inc. 1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600			
Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI		
Size C	Document Number 105-B170xx-00A		Rev 10
Date: Thursday, February 08, 2007	Sheet 16 of 19		

DVI/VGA SCREWS

ASSY-SCREW1
SCREW
JACKSCREW
ASSY
7020000800G

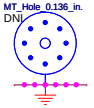
ASSY-SCREW2
SCREW
JACKSCREW
ASSY
7020000800G

ASSY-SCREW5
SCREW
PAN_HEAD
7020001700G

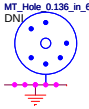
ASSY-SCREW3
SCREW
JACKSCREW
ASSY
7020000800G

ASSY-SCREW4
SCREW
JACKSCREW
ASSY
7020000800G

MT1
MT_Hole_0.136_in.
DNI



MT2
MT_Hole_0.136_in_6VIA
DNI



ASSY1
BRACKET
8020040100G

ASSY2
BRACKET
LP
8020040400G

<Variant Name>

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI	
Size C	Document Number 105-B170xx-00A	Rev 10
Date: Thursday, February 08, 2007	Sheet 17 of 19	

<variant Name>

Title

RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI

Schematic No.

105-B170xx-00A

Date:

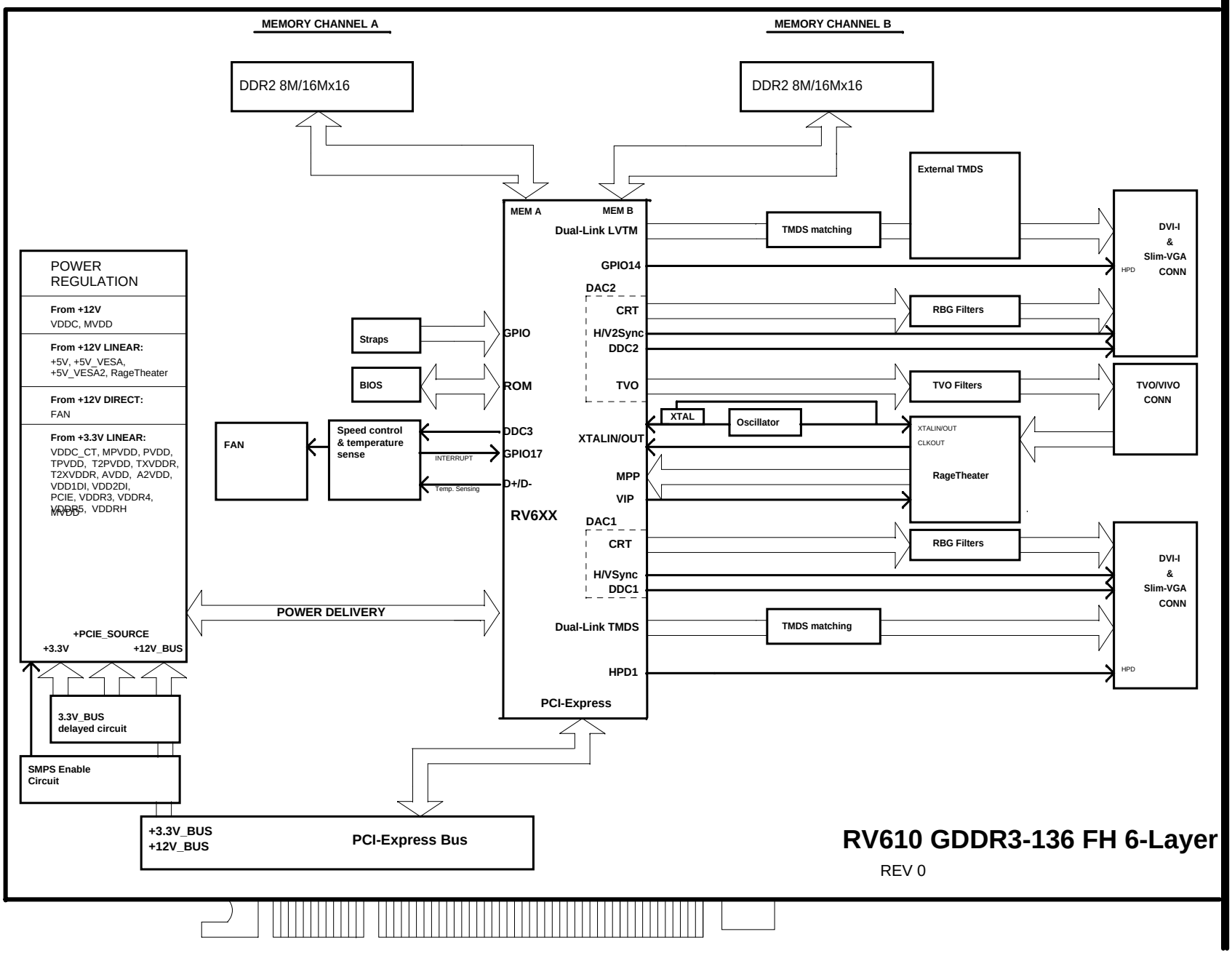
Thursday, February 08, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact ATI representative to obtain latest BOM closest to the application desired.**

Rev 10

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
01	00A	2007.01.08	INITIAL SCHEMATIC. B169 r37 USED AS BASE SCHEM.
02	00A	2007.01.09	SCHEM UPDATES.
03	00A	2007.01.10	RM LED, UPDATE HEATSINK P/N, RM SW1 & J57
04	00A	2007.01.15	RM NC627, MOVE MVDD CONN, RM BBIAS
05	00A	2007.01.24	RM JTAG, ADD TP FOR CONNECTIONS. RM SOME RGB FILTER COMPs
06	00A	2007.01.30	ADD MEMORY POWER CHANNEL
07	00A	2007.01.31	REMOVE LDO1, ADD BRACKET P/N
08	00A	2007.02.01	RM TR52-TR55, ADD HEATSINK
09	00A	2007.02.01	ADD Q90 FOR VDDDR3 LEAKAGE
010	00A	2007.02.01	HEATSINK GROUNDING
011	00A	2007.02.06	ADDED R891. CHANGED VDDC/MVDD NOTES.
012	00A	2007.02.07	MOVED R602 TO PG10. REMOVED MC627.
013	00A	2007.02.08	CHANGED REF DES C625 / MC625 / NC625 TO C626 / MC626 / NC626



RV610 GDDR3-136 FH 6-Layer

REV 0

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RH RV610 128MB DDR2-BGA84 16Mx16 VO dDVI	
Size C	Document Number 105-B170xx-00A	Rev 10
Date: Thursday, February 08, 2007	Sheet 19 of 19	