P681-A01 GT215/216 DESKTOP GB1-128 DDR3 PCI-EXPRESSx16 DL-DVI VGA HDMI

Ver. 0A

Page 1: P681-A01 OVERVIEW Page 2: PCI-EXPRESS INTERFACE Page 3: PARTITION A FRAME BUFFER INTERFACE Page 4: PARTITION A MEMORIES Page 5: FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS Page 6: PARTITION C FRAME BUFFER INTERFACE Page 7: PARTITION C MEMORIES Page 8: FBC DECOUPLING CAPS Page 9: DACA (SOUTH DVI-I) Page 10: DACB (MID VGA) Page 11: IFP AB (SOUTH DVI-I) Page 12: IFP C (NORTH HDMI) Page 13: IFP D (UNUSED) Page 14: IFP EF (UNUSED) Page 15: MIOA & MIOB

Page 16: XTAL, MECHANICALS, THERMALS Page 17: EXTERNAL THERMAL SENSOR, FAN CONTROL, GPIO, JTAG $^{05/11}$ Page 18: BIOS ROM, HDCP ROM, STRAPPING OPTIONS

Page 19: LINEAR POWER SUPPLIES Page 20: FBVDDQ/PEXVDD POWER SUPPLY

Page 21: NVVDD POWER SUPPLY

Page 01 1.Remove C690,C70 47uF Page 10 1.Remove J1 D-Sub Page 11 1.Remove R16.Q2 Page 12 1.Remove R1,Q1 Page 16 1.Change Crystal Footprint to 2-PIN SMD 2.Remove C71 47uF 05/08

Page 17 1.Remove Thermal Sensor Circuit Page 18 1.Remove U2,C54,R31,R30,D16 INFOROM circuit Page 19 1.Remove 3V3 to 1.8V circuit

2.Change 5V REGULATOR Circuit Page 20 1.Change L8 Footprint to 1.6uH 2. Change Footprint to multi cap for EL 1500uF

Page 21 1.Change NVVDD to UP6161 2.Change L12 footprint to 1.2uH

Page 05 1. Remove Decoupling for EMI cap Page 20 1. C84 change Footprint to multi cap

Page 21 1.Add C39 270uF 2.Add R922,R924 for APW7068 OCSET Page 16 1.Add XTALIN R566 Risister Add XTALOUT R573 Risister Page 02 1.Change C51 to 0805 1UF and ADD C54 0805 1UF

Page 03 1.C642,C666,C633 change to .01UF Page 05 1.Remove C516.C525.C549.C556.C541.C512 Remove C513,C546,C540,C528,C547,C507 Remove C544,C545,C520,C523,C532,C508 Remove C535, C526, C543, C553, C537, C88

Page 08 1.Remove C566,C567,C576,C578,C82,C564 Remove C619.C592.C586.C585.C622.C574 Remove C705, C706, C680, C729, C691, C683 Remove C742, C738, C731, C725, C743, C728

Page 20 1.Remove C86,C562,C563,C87

Page 17 1.Remove 4-PIN FAN Circuit Page 12 1.Change Q509 to Q513,Q514 SOT23 footprint

Page 16 1.Change FAN Screw hole Page 20 1.Add C102 820uF

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Page 21 1.Remove D94 scottky diode

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Page 11 1.Add EMI bridge Page 12 2.Add EMI bridge

Page 03 1.Add RP24 termination risister Page 06 2.Add RP23 termination risister

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SWAP CMD Page 03/06 RP5.1 , RP5.2 FBC_CMD10 , RP5.3 , RP5.4 FBC CMD22 RP4.1, RP4.2 FBC CMD18, RP4.3, RP4.4 FBC CMD7

RP24.1, RP24.2 FBA CMD30, RP24.3, RP24.4 FBA CMD7 RP20.1, RP20.2 FBA CMD14, RP20.3, RP20.4 FBA CMD18 RP14.1, RP14.2 FBA_CMD1, RP14.3, RP14.4 FBA_CMD20 RP12.3, RP12.4 FBA CMD29

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Page 05 1. Add Decoupling for EMI cap C80,C524,C517,C102

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Page 02 1.Remove JTAG Circuit

Page 09 1.Remove EMI filter, protection diode, C780, C775, C779 Page 10 1.Remove EMI filter,protection diode,C771,C772,C773

Page 12 1.IFP_PLLVDD change netname to 3V3

Page 15 1.Remove R545,C664,R554 of MIOA

Page 17 1.Remove JTAG Circuit 2 Remove FAN PWM Circuit

Page 18 1.Remove HDCP EEROM

Page 19 1.Remove U4 UP7703 Circuit

2.Change 5V Circuit SOT223-->SOT252

Page 20 1.Remove C86,C105,C90

2.Add R917 LMOS Gate risister 3.Add L10

4.Add L9.LB23.LB24 5.Add EL 680UF FootPrint

Page 21 1.Add L13

2.Remove APW7068 OCSET 3.Add GPIO 5,6 Circuit 4.Remove C927,C931

08/04

Page 21 1.Remove C933.C30.C31.C38 2.Change C39 FootPrint for 470uF 3.NVVDD Power Sequencing and PWM power change to 12V from 12V_F

Page 20 1.Add C86,C87,R26

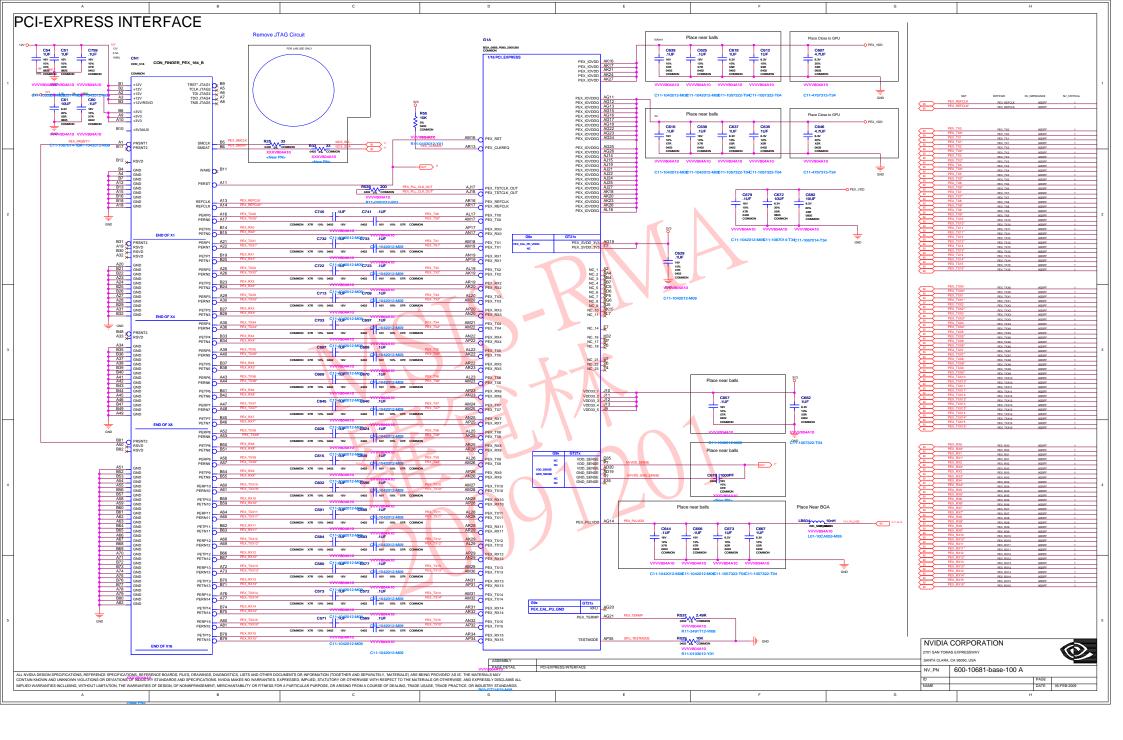
2.Remove C557

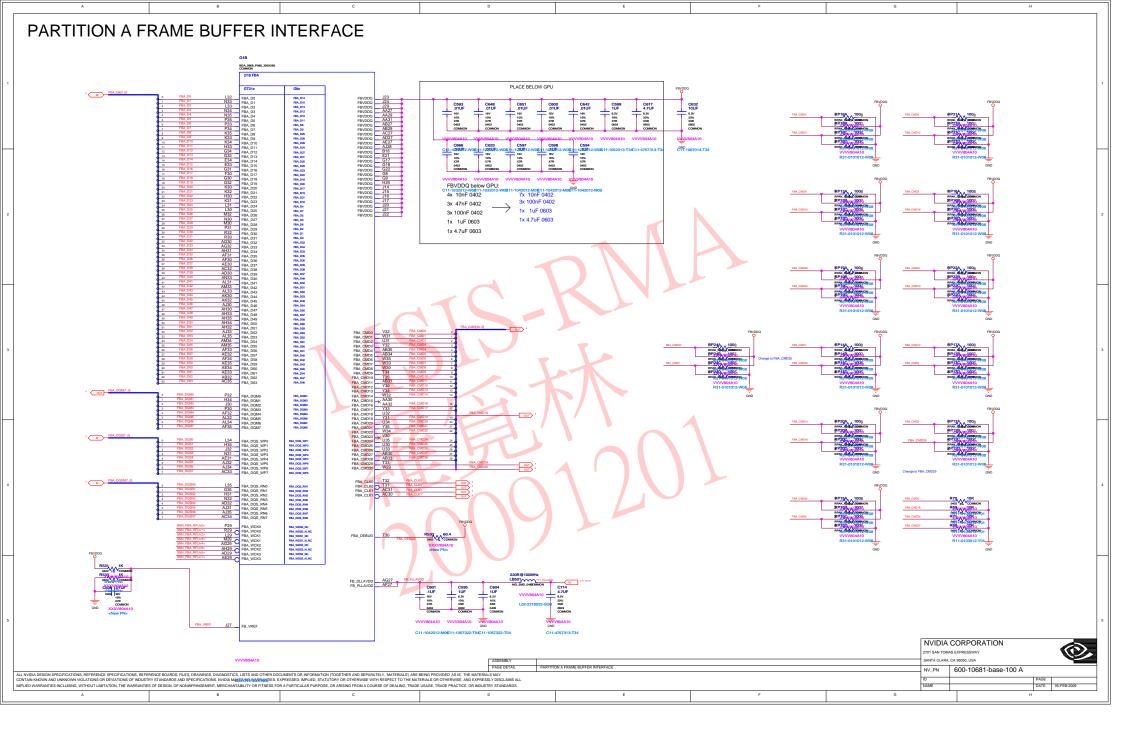
3. Power Sequencing and PWM power change to 12V from 12V_F

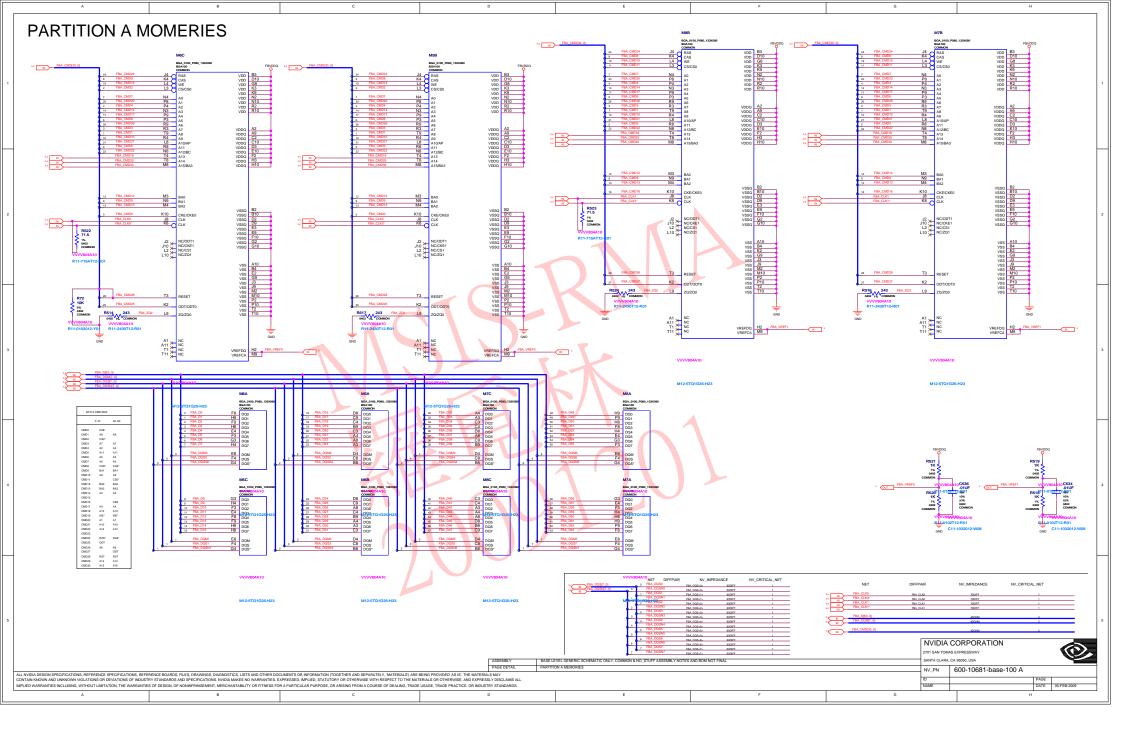
NVIDIA CORPORATION

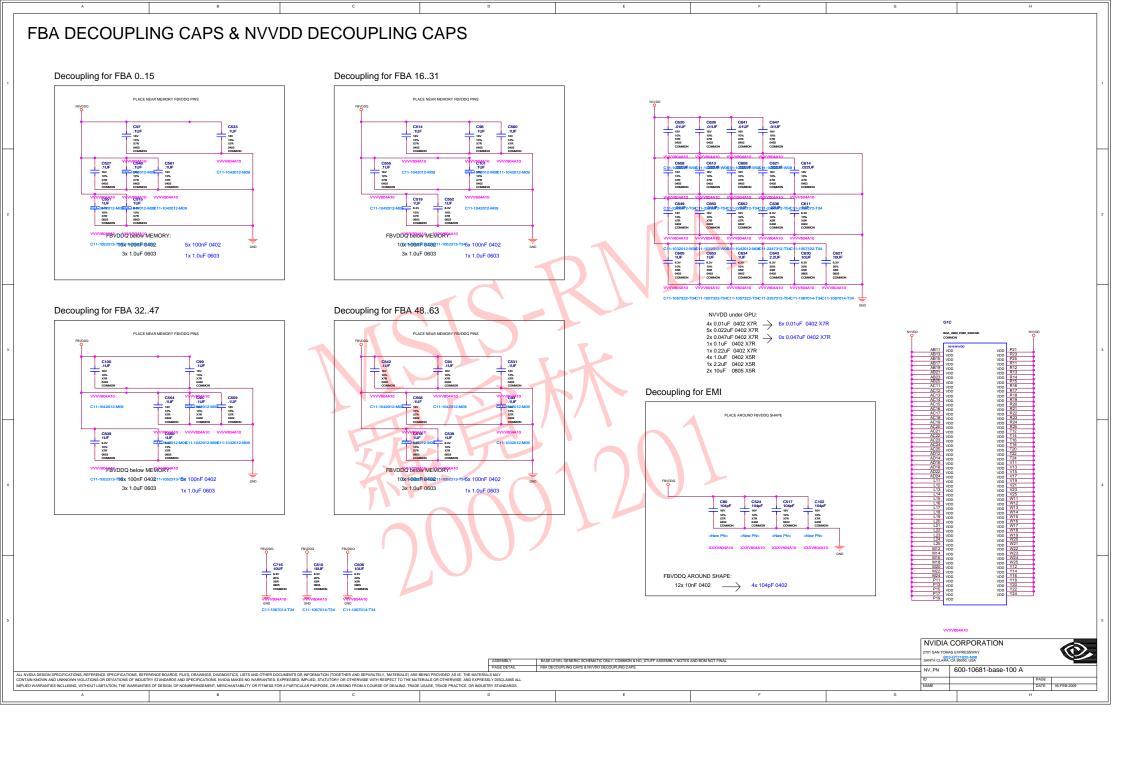
SHU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10681-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10681-0001-100	GT216-300 600/1500MHz 1024MB 64Mx16 BGA100 800MHz DDR3 DVI-I/VGA/HDMI
2	SKU0002	600-10681-0002-100.	GT216-300 600/1500MHz 1024MB 64Mx16 BGA100 1000MHz DDR3 DVI-I/VGA/HDMI
3	SKU0011	600-10681-0011-100	GT215-300 600/1500MHz 1024MB 64Mx16 BGA100 900MHz DDR3 DVI-I/VGA/HDMI
4	<undefined></undefined>	<undefined></undefined>	UNDEFINEDS
5	<undefined></undefined>	<undefined></undefined>	<undefined></undefined>
6	<undefined></undefined>	<undefined></undefined>	<undefined></undefined>
7	<undefined></undefined>	<undefined></undefined>	<undefined></undefined>
8	<undefined></undefined>	<undefined></undefined>	<undefined></undefined>
9	<undefined></undefined>	<undefined></undefined>	<undefined></undefined>
10	<undefined></undefined>	<undefined></undefined>	UNDEFINEDS
11	<undefined></undefined>	<undefined></undefined>	UNDEFINEDS
12	<undefined></undefined>	<undefined></undefined>	<undefined></undefined>
13	<undefined></undefined>	<undefined></undefined>	<undefined></undefined>
14	<undefined></undefined>	<undefined></undefined>	<undefined></undefined>
15	<undefined></undefined>	<undefined></undefined>	AUNDEFINED»

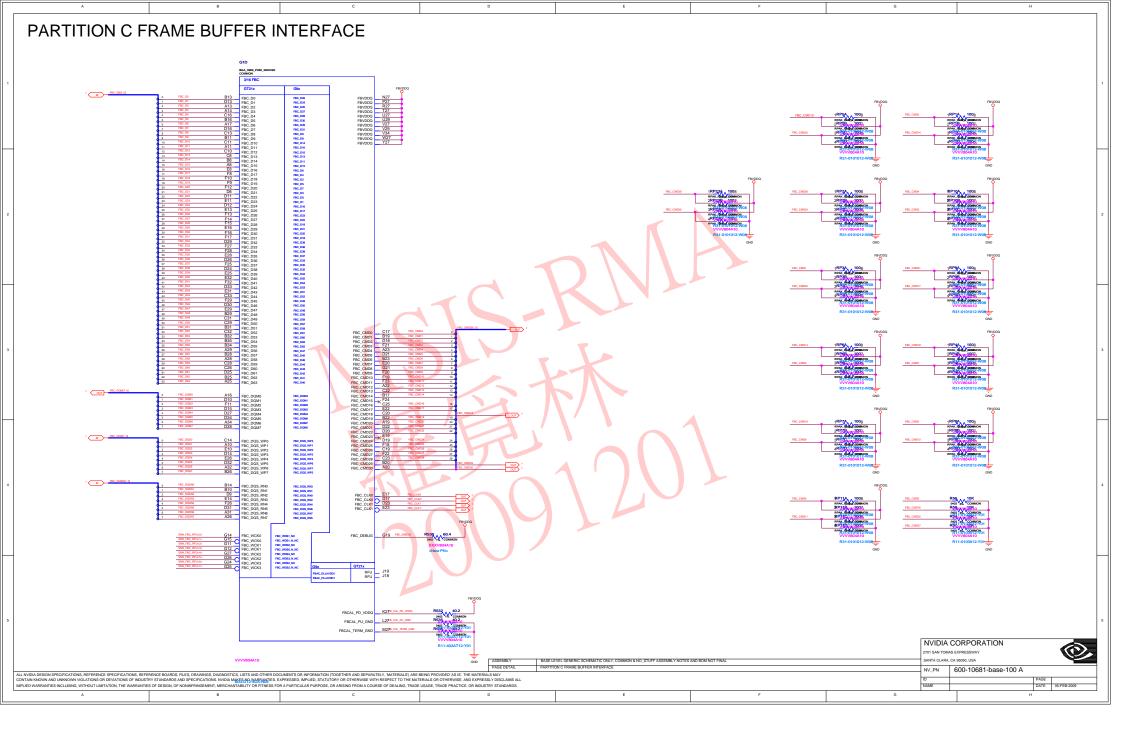
701 SAN TOMAS EXPRESSWA BASE LEVEL GENERAL SCHEMATIC ONLY COMMON & NO. STILES ASSEMBLY NOTES AND BOM NOT FIN ANTA CLARA, CA 95050, USA 600-10681-base-100 A NV_PN ALL INFOLD SEIGN SPECIPICATIONS, REFERENCE SPECIFICATIONS, REFERENCE SOURCE, FLES, DRAWNSS, DUGNOSTICS, LISTS AND OTHER DOCUMENTS OR INCROMATION (TOCETHER AND SEPARATELY, MATERIALS) ARE EIRN PROVIDED AS IS THE MATERIALS MAY CONTAIN INCOMINA AD LINKNOWN VIOLATIONS OR DEVIATIONS OF ROLUSTRY STANDARDS AND SPECIFICATIONS, NIVIDA MAKES NO WARRANTES, EXPRESSED, MPLED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY OR SOCIATIONS AND ADMINISTRATION OF THE PROVINCE, AND EXPRESSLY OR ADMINISTRATION APPROVED, OR ARBITING FROM A COURSE OF DEALMS, TANGE USINGE, TRADE PRACTICE, OR ROLUSTRY STANDARDS.

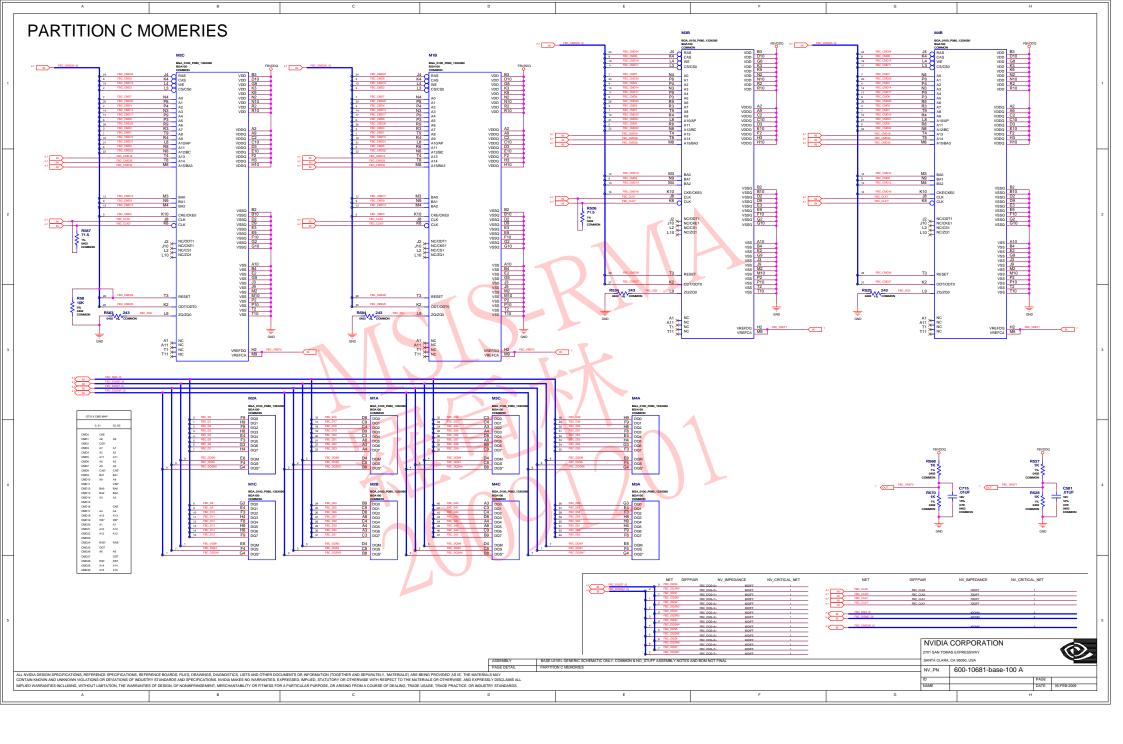


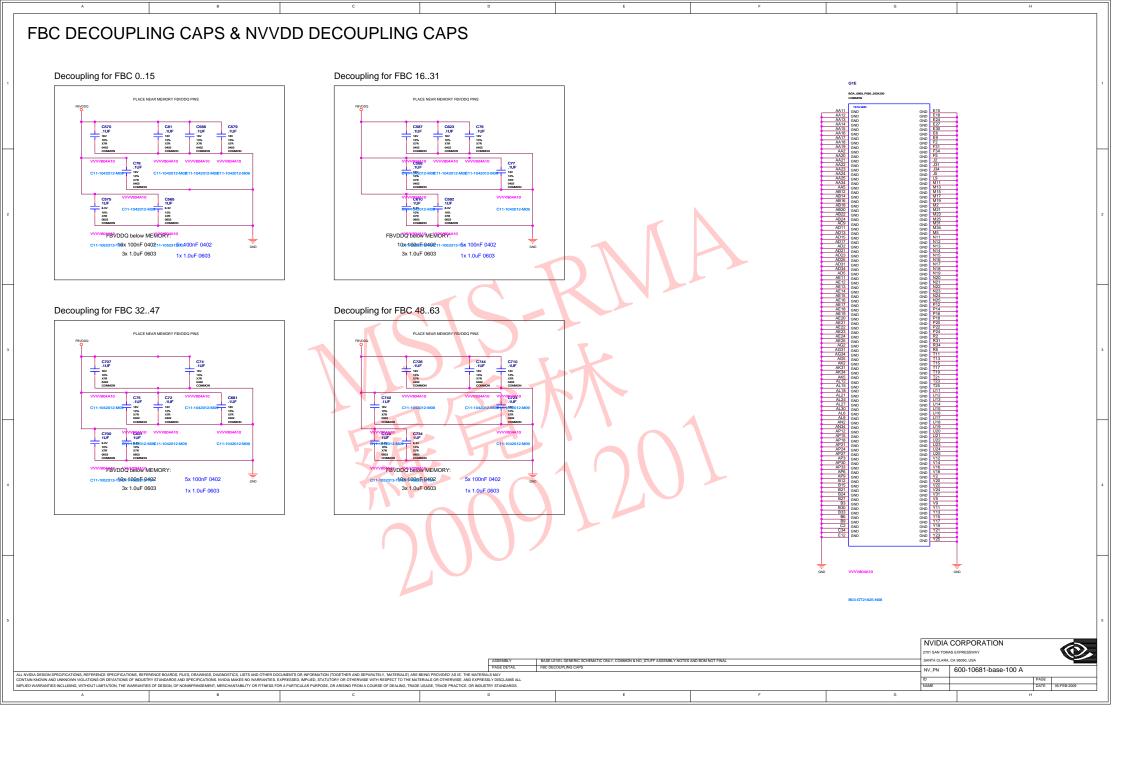


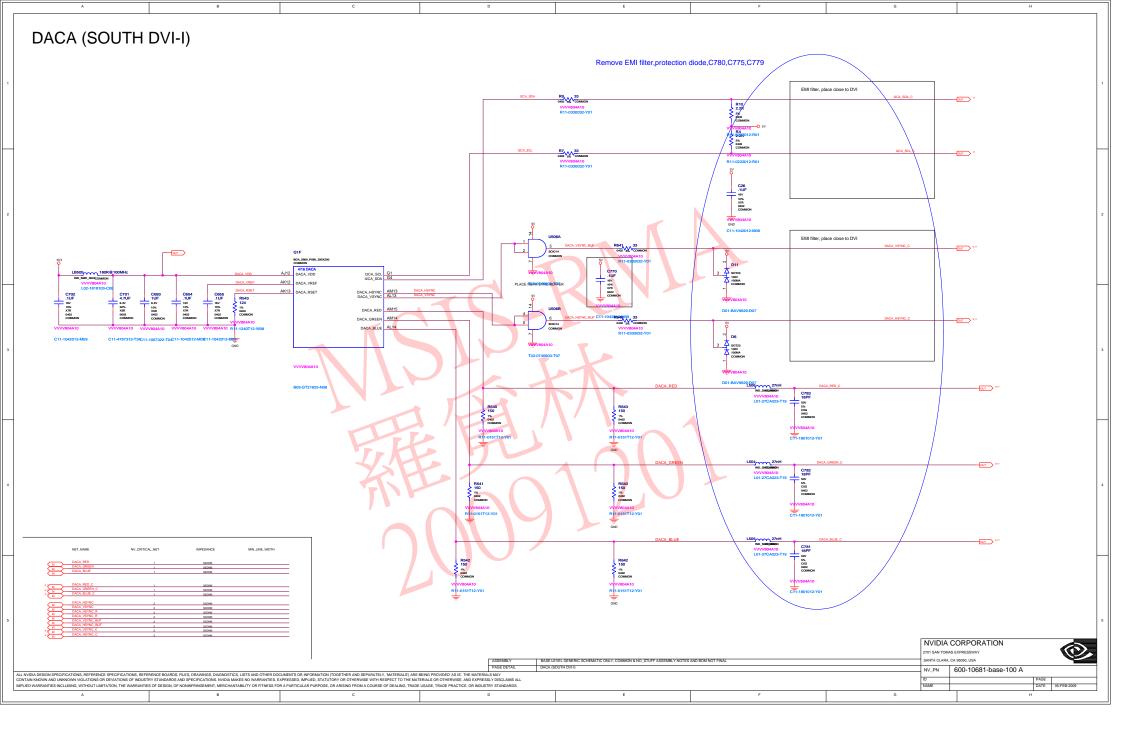


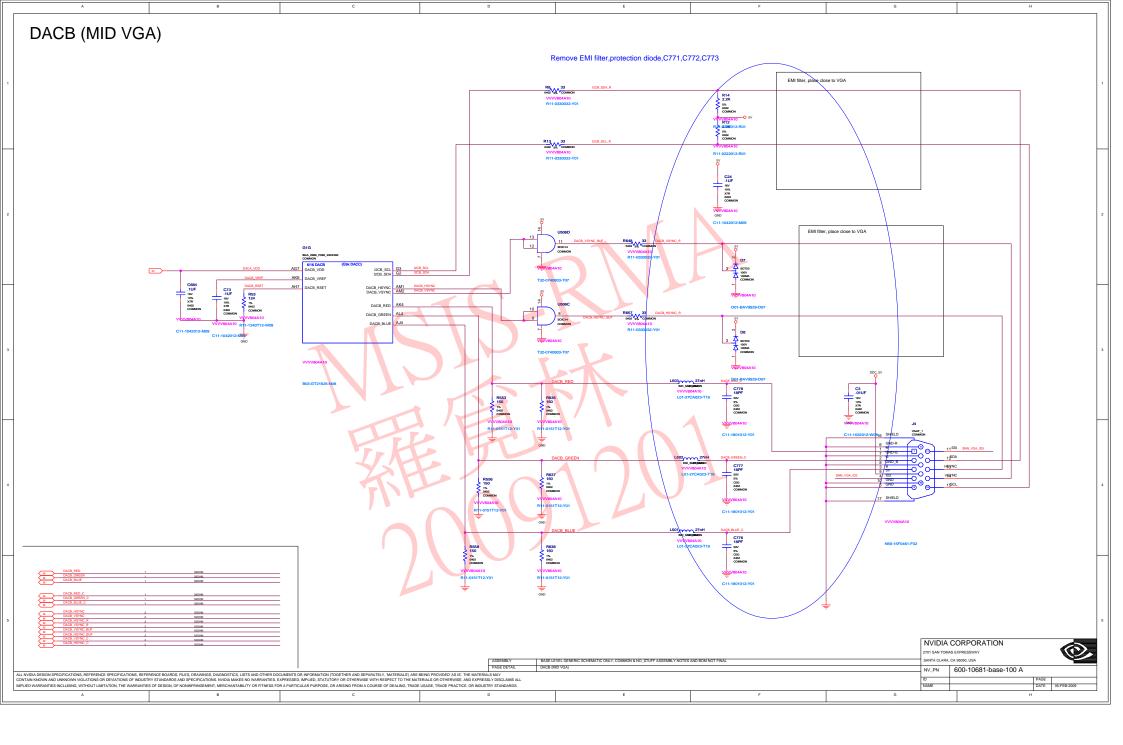


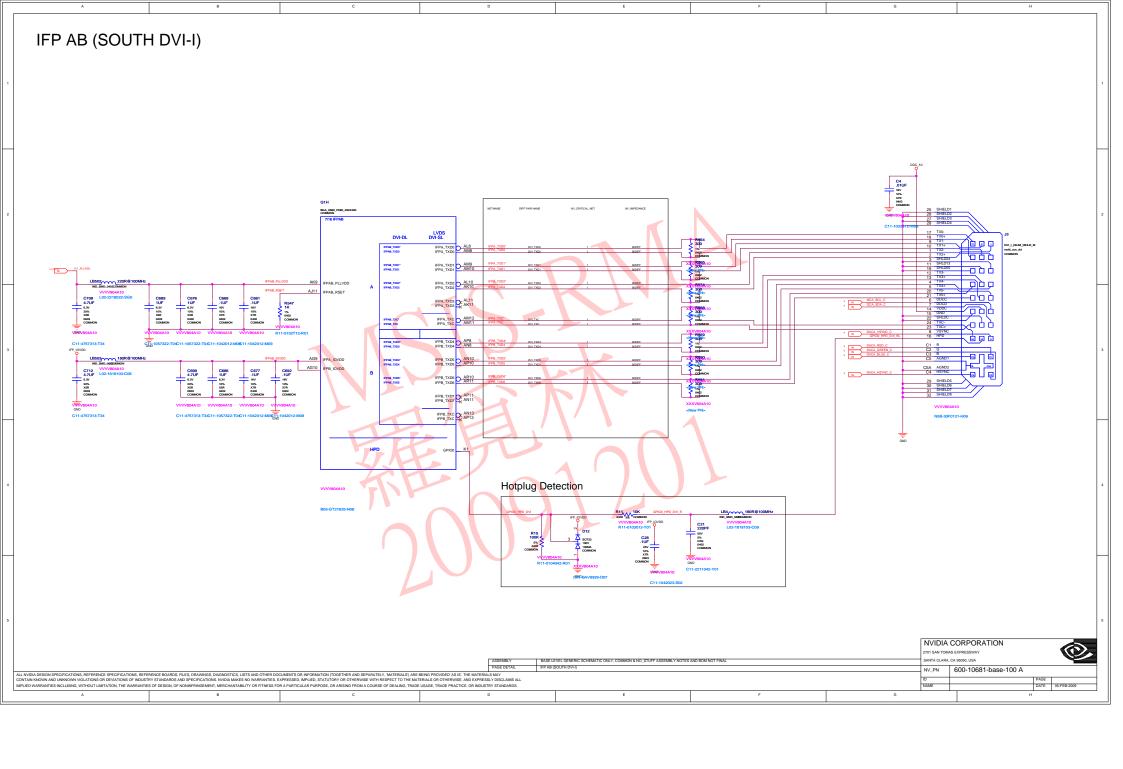


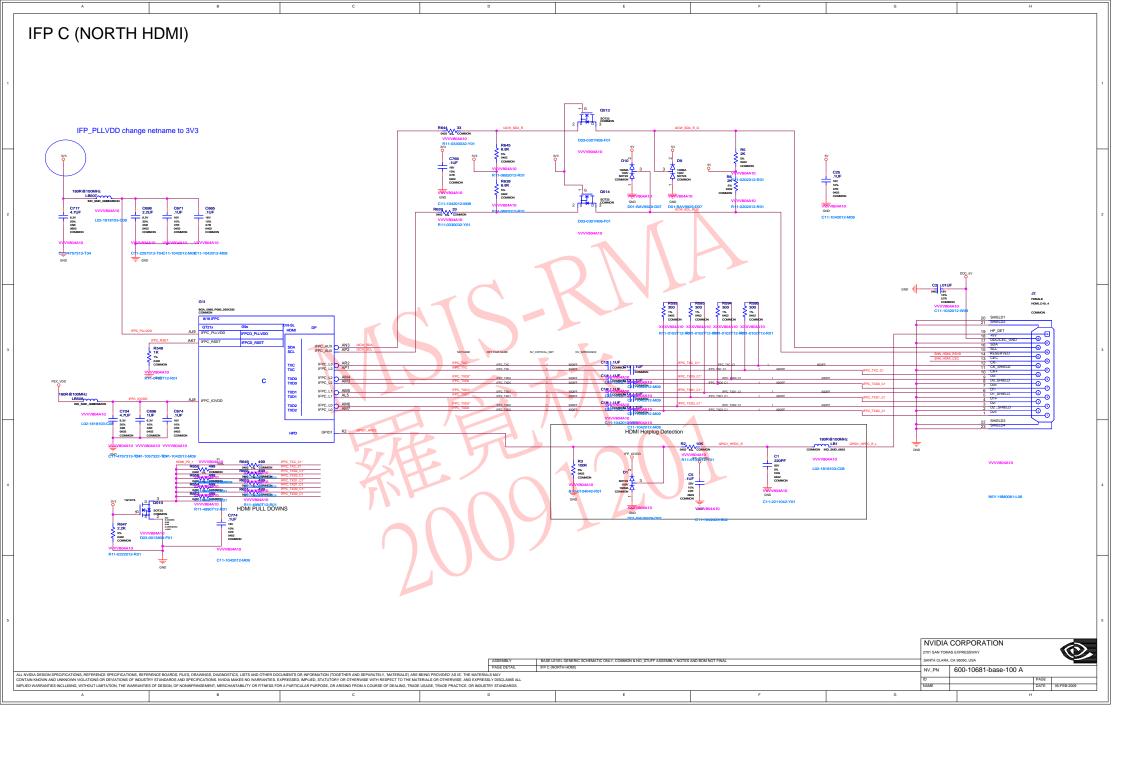


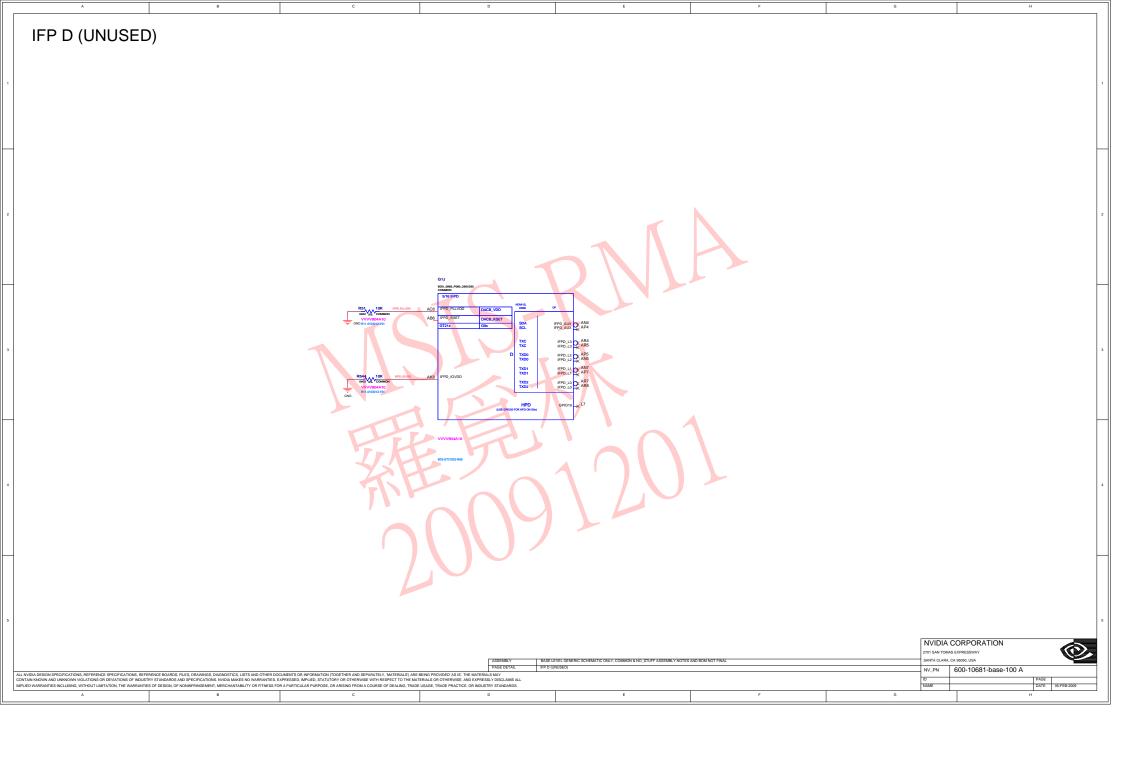


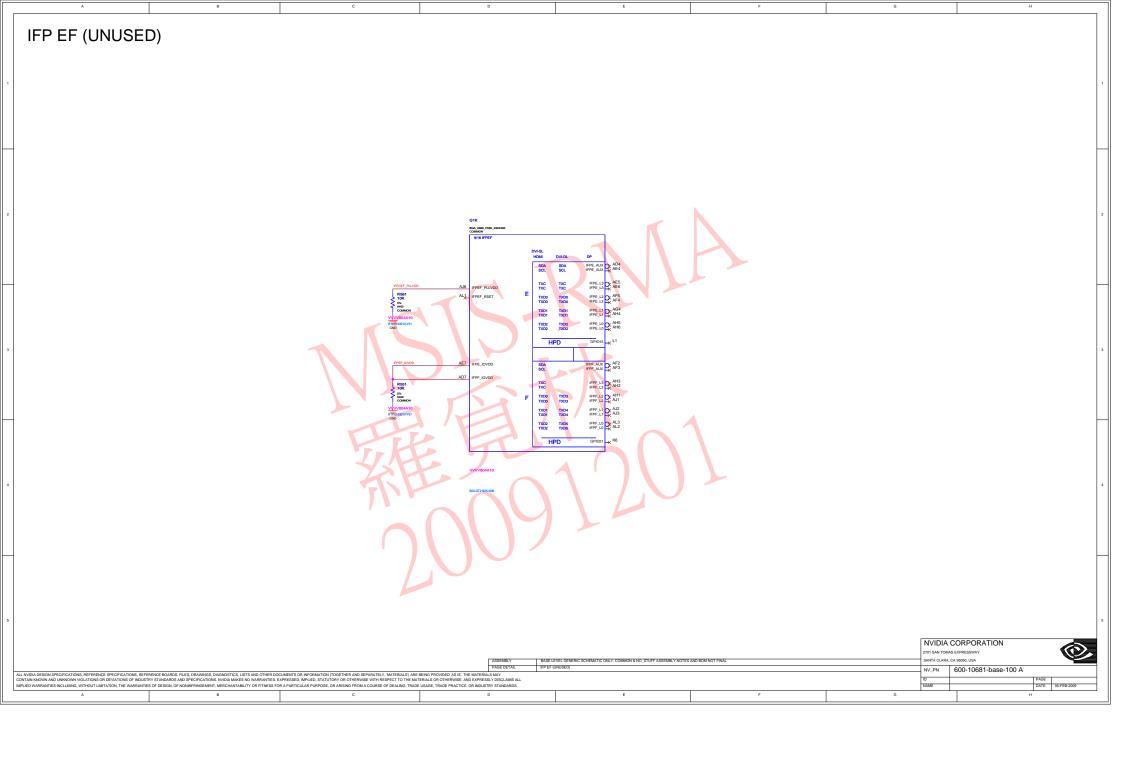


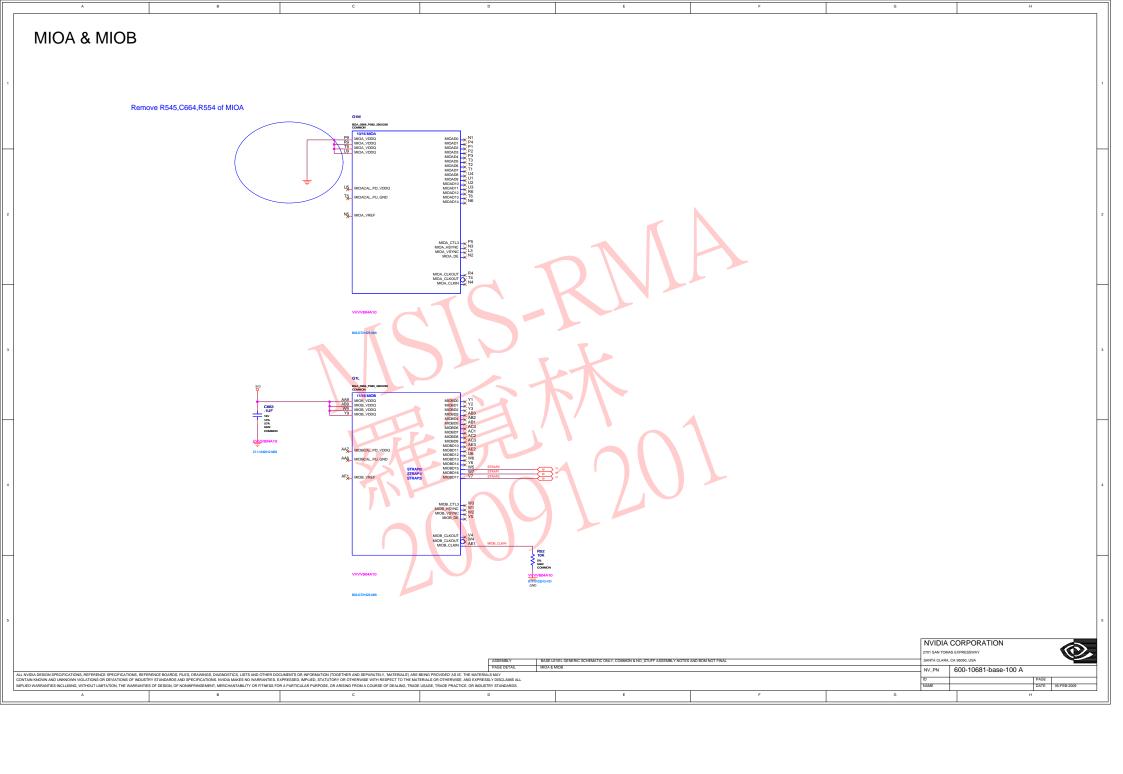


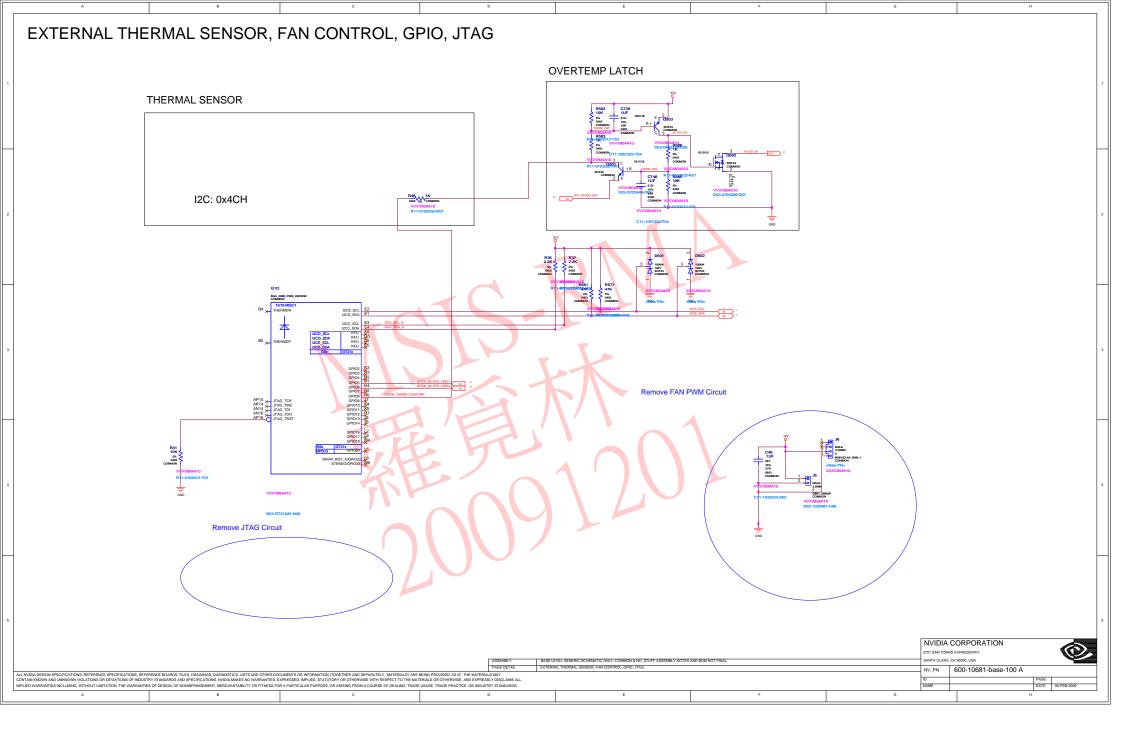


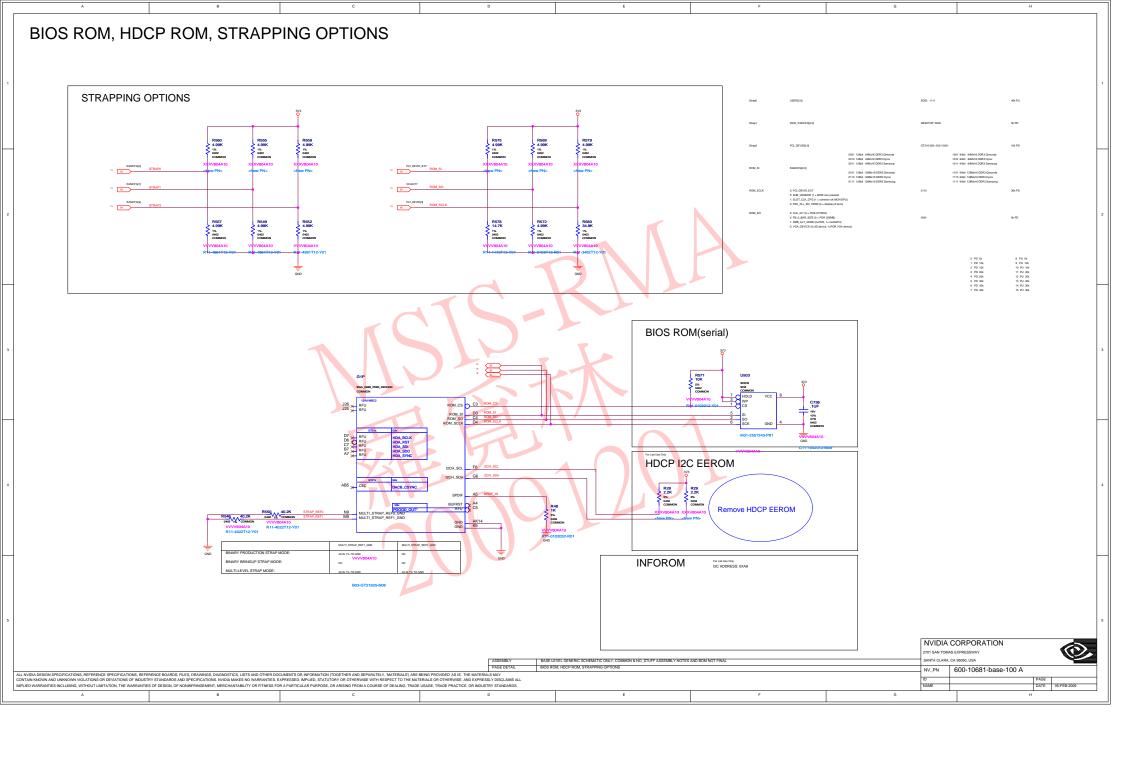


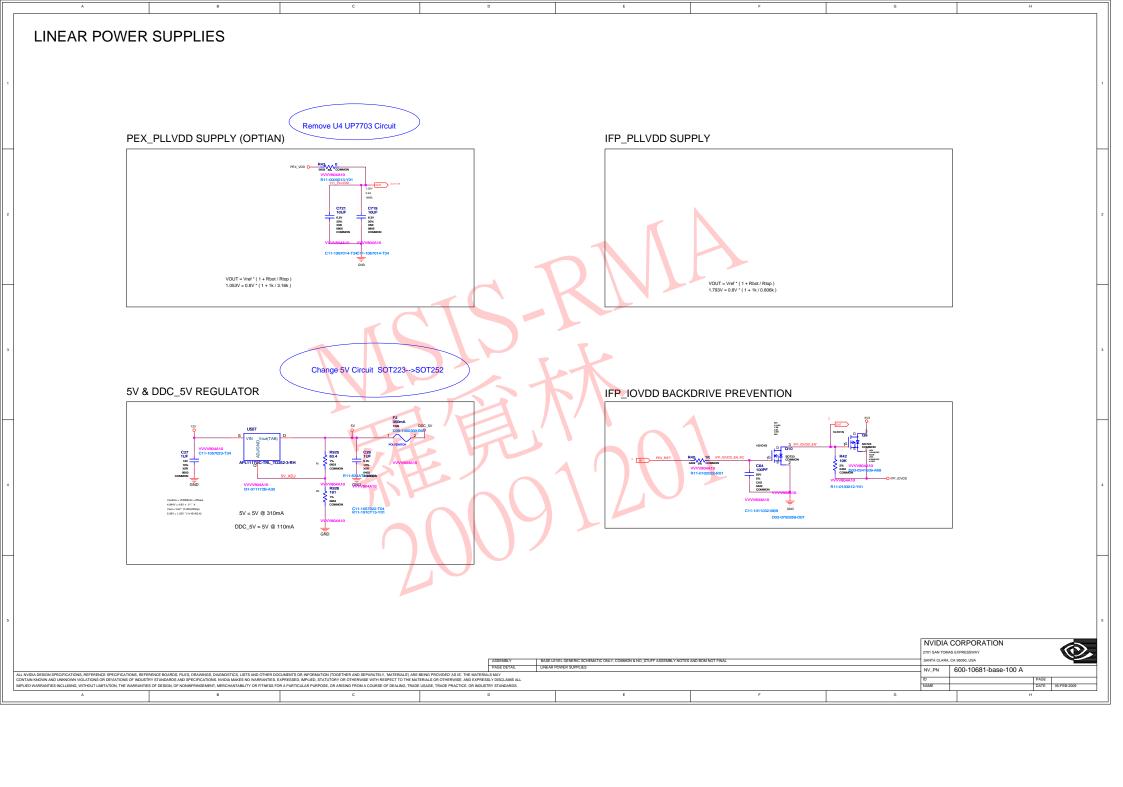


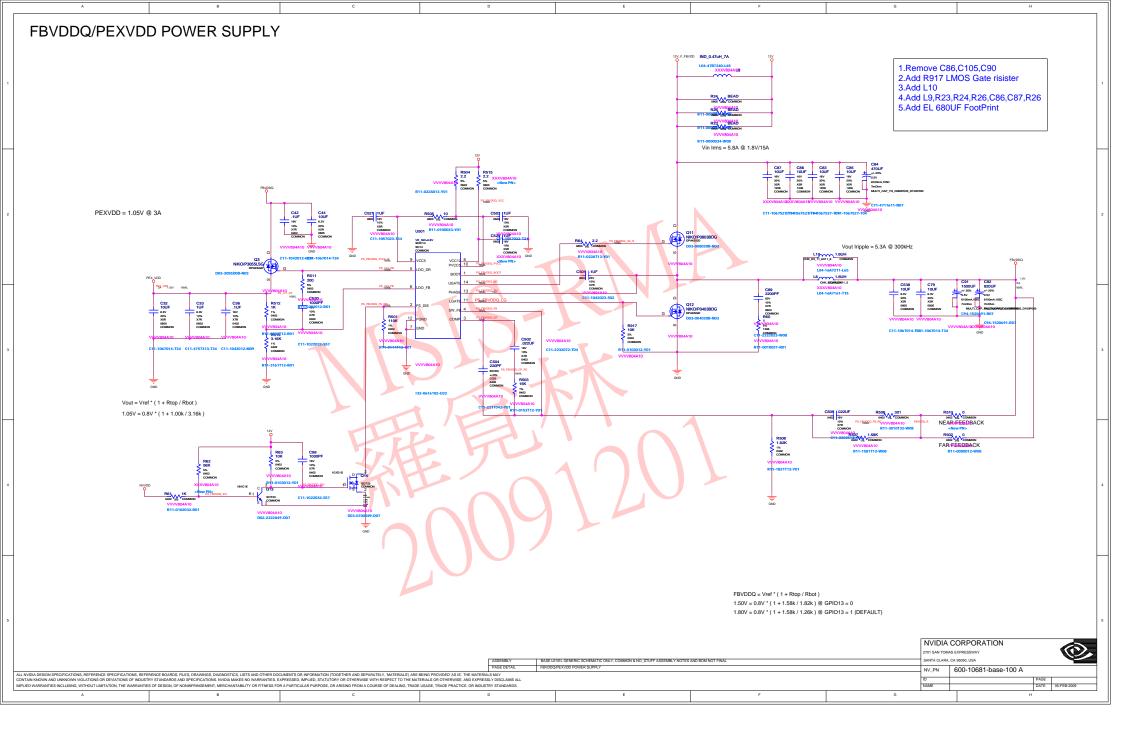


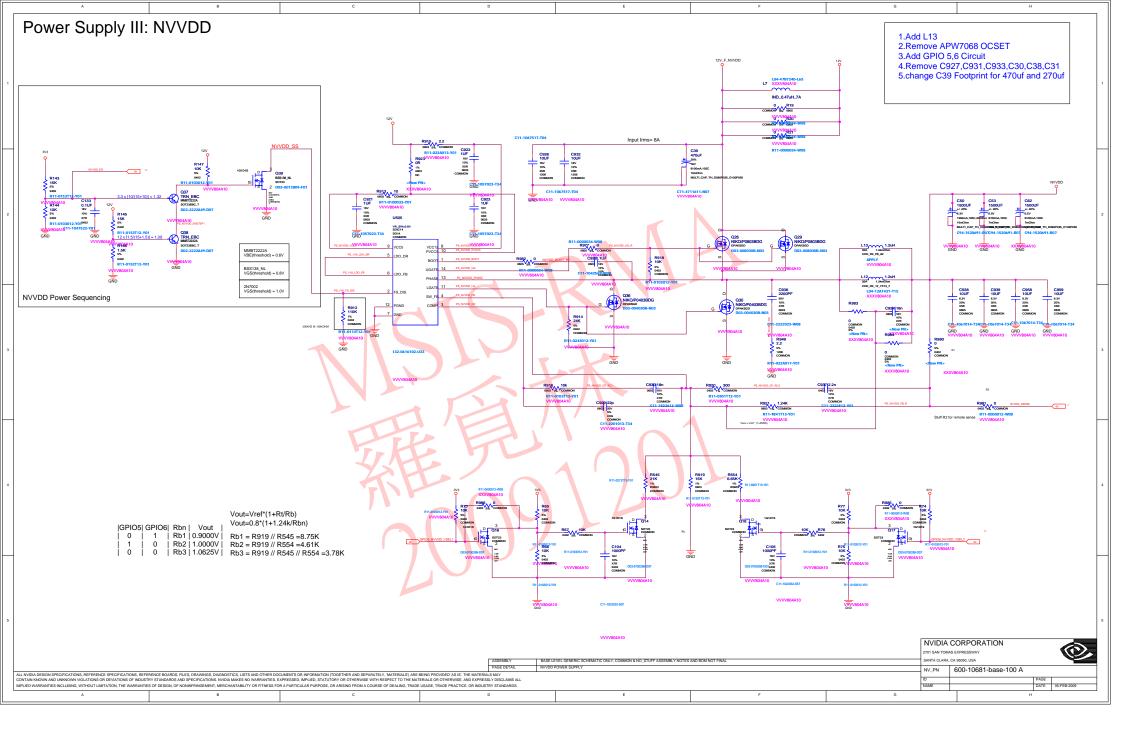










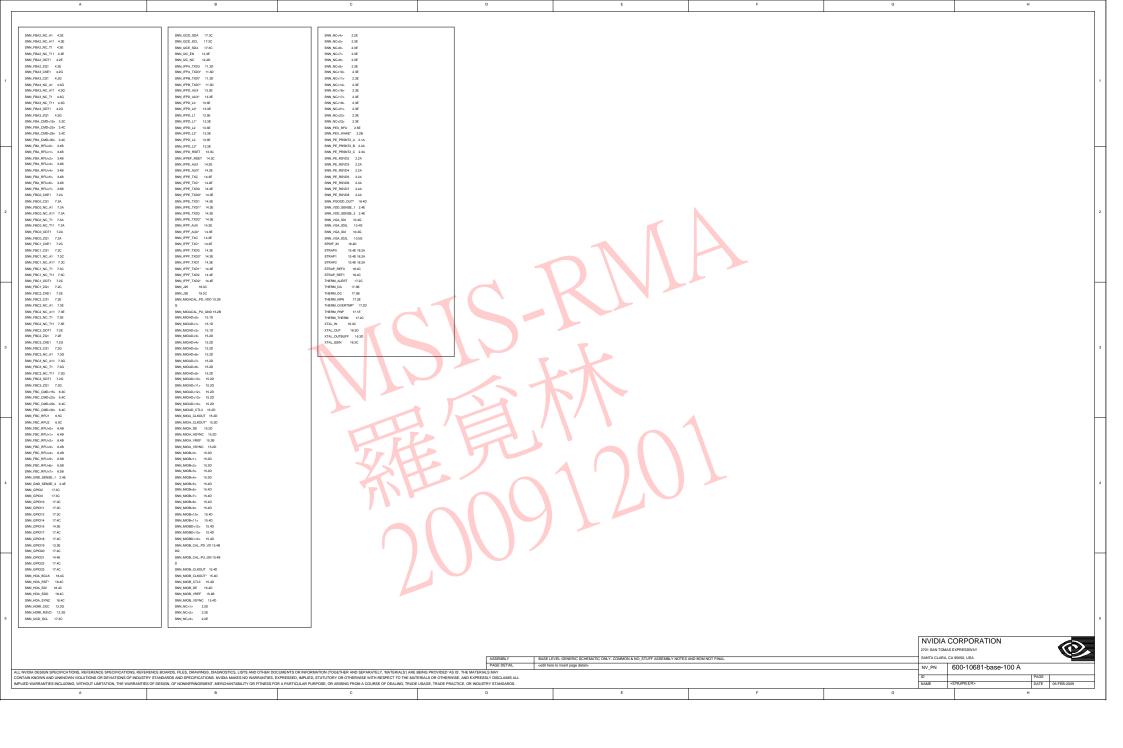


The column								
Company Comp								
A. C. C. C. C. C. C. C.								
Company		4.2A 4.2C	FBA_DQSN<2> 3.4B 4.4C 4.5E	FBC_D<28> 62B 7.4C	GPIO16_FAN_PWM 17.4C	NV/DD_MODE_Q 21.1B	PEX_TXX1* 228 2.9G	
The content								
Column	p681_lib.P681(@p681_lib.p681(ach_1)) Base Signal Location([Zone](dirl))	4.1E 4.1G FBA_CMD<25> 3.4C 3.4G 4.3A 4.3C				NV/DD_REFIN 21.9C NV/DD_RSET 21.9C	PEX_TXX2* 2.28.2.3G PEX_TXX3 2.38.2.3G	
The color of the		FBA_CMD<26> 3.2F 3.4C 4.1A 4.1C	FBA_DQSN-6> 3.4B 4.4E 4.5E	FBC_D<32> 6.2B 7.3D	12CA_SCL 9.2C 9.2D	NVVDD_SENSE 2.4F 21.4D	PEX_TXX3* 2:38 2:3G	
March Marc		4.1E 4.1G	FBA_DQSNx7> 3.48 4.4E 4.5E	FBC_D<33> 6.28 7.4D	I2CA_SCL_C 9.2H 11.3G	NV/DD_SENSE_R 21.4E	PEX_TXX4 23B23G	
Column C								
The color of the	1V8_ADJ 19.2F	4.9C	FBA_VREF1	FBC_D-36> 628 7.4D	I2CA_SDA_C 9.1H 11.3G	NV/DD_VREF 21.3C	PEX_TXX5* 2:38 2:3G	
The column	3V3 2.1A							
The column The	3V3_INFO 18.5F 5V 19.4C	HBA_DI-83.0> 3.18.4.38 FBA_D<1> 3.18.4.38	FBA_ZU1 4.3C FBA_ZU2 4.3E	FBC_DC85 62B7.4D FBC_Dc36 62B7.4D	1208_SCL 10.2C 1208_SCL R 10.1E	NVVDU_VSEL2_Q 21.38 NVVDD VSEL3 21.48	PEX_IXX8* 238 23G PEX_TXX7 238 23G	
The column	5V_ADJ 19.48	FBA_D<2> 3.18 4.48	FBA_ZQ3 4.3G	FBC D-40> 62B 7.4D	12CB SCL R L 10.1G	NVVDD_VSEL3_Q 21.3C	PEX_TXX7* 23823G	
Wilder W	12V 2.1A		FBC_CLK0	FBC_D<41> 6.2B 7.4D	12CB_SDA 10.2C			
March	12V_D 19.4A 12V F 21.1F							
State 1	DACA_BLUE 9.4E 9.5A	FBA_D+6> 3.18 4.48	FBC_CLK1* 6.4D 7.2D 7.2F 7.5G	FBC_D+44+ 6.38 7.4D	I2CC_SCL 17.2B 17.3F 18.5E	PEX_PLL_CLK_OUT* 22C	PEX_TXX9* 2:3G:2:4B	
March Marc	DACA_BLUE_C 9.4H 9.5A 11.3G	FBA_D<7> 3.18 4.48	FBC_CMD+0> 6:3C 6:4G 7:2A 7:2C	FBC_D-45> 6:38 7:4D	12CC_8CL_G 17.3C	PEX_PRSNT1* 2.1A	PEX_TXX10 2:3G 2:4B	
Manual	DACA_GREEN_C 9.4E 9.5A DACA_GREEN_C 9.4H 9.5A 11.3G			FBC_Do47> 6.38 7.4D	LEUC_SDA 17.28 17.3F 18.5E 12CC_SDA_G 17.3C	PEX_REFCLK* 2.10.2.28		
March 100	DACA_HSYNC 9.3C 9.5A	FBA_D<10> 3.18 4.48	FBC_CMD<1> 6.2F 6.3C 7.1A 7.1C	FBC_D<46> 6.38 7.3E	12CH_SCL 18.4D	PEX_RST* 2.2D 19.4E	PEX_TXX11* 2:3G 2:4B	
State Stat		FBA_D<11> 3.18 4.48	7.1E 7.1G	FBC_Do40> 6.3B 7.4E	12CH_SDA 18.4D		PEX_TXX12	
March Marc	DACA_HSYNC_C 9.3H 9.5A 11.3G DACA_HSYNC_R 9.3F 9.4A	HBA_D<12> 3.28 4.48 FBA_D<13> 3.28 4.49	FBC_CMD-3> 6.09.63C.7.1A.7.1C FBC_CMD-3> 6.29.63C.7.1A.7.1C	FBC D-51> 6.38 7.4E FBC D-51> 6.38 7.4F	IXUS_SCL 2.1C 17.3F I2CS SDA 2.2C 17.3F	PEX_RX0* 22B2.4G PEX_RX1 22B2.4G	PEX_TXX12* 2.3G 2.4B PEX_TXX13 2.3G 2.5B	
March Marc	DACA_RED 9.3E 9.5A	FBA_D<14> 328 4.48	7.1E 7.1G	FBC_D-62> 6:38 7:4E	12CW_SCL 12:3C	PEX_RX1* 22B2.4G	PEX_TXX13* 2.3G 2.5B	
March 1	DACA_RED_C 9.9H 9.5A 11.9G	FBA_D<15> 3.28 4.48	FBC_CMD+4+ 6.2G 6.3C 7.1A 7.1C	FBC_D-63> 6.3B 7.4E	12CW_SCL_R 12.2D	PEX_RX2	PEX_TXX14 2:9G 2:5B	
Note 100								
No. April	DACA_VREF 9.3B	FBA_D<18> 3.28 4.40	7.1E 7.1G	FBC_D-56> 6.3B 7.4E	12CW_SDA_R 12.1D	PEX_RX3* 2.3B 2.4G	PEX_TXX15* 2.4G 2.5B	
March Marc								
March Marc	DACA_VSYNC_BUF 9.2E 9.5A DACA_VSYNC_C 9.2H 9.5A 11.3G	FBA_D:20> 3:28.4.4C FBA_D:21> 3:28.4.4C	7.1E 7.1G FBC_CMD<7> 6.3C 6.3G 7.1A 7.1C		IFPAB_PUVDD 11.28 IFPAB_PUVDD 11.28	PEX_RX4* 2382.4G PEX_RX5 2382.4G	PS_1V1_CP 20.38 PS_1V1_DR 20.3C	
March Marc	DACA_VSYNC_R 9.2E 9.5A	FBA_D<22> 3.28 4.4C	7.1E 7.1G	FBC_0-60> 6.3B 7.4E	IFPAB_RSET 11.3B	PEX_RX5* 2.3B 2.4G	PS_1V1_FB 20.3C	
March Marc	DACB_BLUE 10.4D 10.5A	FBA_D-23> 32B 4.4C	FBC_CMD<8> 6.3C 6.4F 7.1A 7.1C	FBC_D<61> 6.38 7.4E	IFPA_TXC 11.3D	PEX_RX8 2382.4G	PS_FBVDDQ_BOOT 20:20	
March Marc						PEX_RX8* 2.3B 2.4G		
March Marc	DACB_GREEN_C 10.4F 10.5A	FBA_D<26> 32B 4.4C	7.2E 7.2G	FBC_DEBUG 6.4C	IFPA_TXD0° 11.2D	PEX_RX7* 2.4B.2.4G	PS_FBVDDQ_EN 20.48	
March Marc	DACB_HSYNC 10.9C 10.5A	FBA_D<27> 3.28 4.4C	FBC_CMD<10> 6.9C 6.9G 7.1A 7.1C	FBC_DQM+0s 6:38 7:48	IFPA_TXD1 11.2D	PEX_RX8 2.48 2.4G	PS_FBVDDQ_EN* 20.4C	
March	JACK_HSYNC_BUF 10.9E 10.5A DACB HSYNC C 10.9G 10.9A	FBA D-295 328 4.40 FBA D-295 328 4.40					PS FBVDDQ FB RC 20.40	
March Marc	DACB_HSYNC_R 10.3E 10.5A	FBA_D<30> 3.28 4.4C	FBC_CMD<12> 6.9C 6.4G 7.2A 7.2C	FBC_DQM<2> 8.38 7.4C	IFPA_TXD2* 11.2D	PEX_RX9* 2.4B 2.4G	PS_FBVDDQ_FS_DIS 20.3C	
March Marc	DACB_RED 10.3D 10.5A	FBA_D<31> 3.28 4.40	7.2E 7.2G	FBC_DQMx3> 6:38 7.4C	IFPB_TXD4 11.3D	PEX_RX10 2.4B 2.4G	PS_FBVDDQ_LG 20:3D	
Section Control Cont	DACB_RED_C 10.3F 10.5A DACB_RSET 10.3R	FBA_D-33> 3.28 4.30 FBA_D-33> 3.28 4.30	FBC_CMD<13> 6.3C 6.3F 7.2A 7.2C 7.2E 7.2G	FBC_DOMc4> 6.38 7.40 FBC_DOMc5> 6.38 7.40	IFPB_TXD4* 11.3D IFPB_TXD5 11.3D	PEX_RX10* 2.4B 2.4G PEX_RX11 2.4B 2.4G	PS_FBVDDQ_PH 20.30 PS_FBVDDQ_PVCC 20.20	
March 15 15 15 15 15 15 15 1	DACB_VDD 10.2B	FBA_D<34> 32B 4.4D	FBC_CMD<14> 6.1G 6.3C 7.1A 7.1C	FBC_DQM-6> 6.48 7.4E	IFPB_TXD5* 11.3D	PEX_RX11* 2.4B 2.4G	PS_FBVDDQ_PVCC_R 20.2C	
March Marc	DACB_VREF 10.2B	FBA_D<36> 3.28 4.4D	7.1E 7.1G	FBC_DQM<7> 6.48 7.4E	IFPB_TXD6 11.3D	PEX_RX12	PS_FBVDDQ_RC 202F	
March Marc			FBC_CMD<16> 6.3C 6.4G 7.2E 7.2G	FBC_DQS<0> 6.48 7.48 7.5E	IFPB_TXD6* 11.3D	PEX_RX12* 2.5B 2.5G		
March State March Marc		FBA_D<38> 3.28 4.4D	7.1E 7.1G	FBC_DQS<1> 6.48 7.48 7.5E	IFPC_IOVDD 12:3A	PEX_RX13* 2.58 2.5G	PS_FBVDDQ_VCC 20:2D	
Part	DACB_VSYNC_R 10.2E 10.5A	FBA_D<39> 3.28 4.4D	FBC_CMD<18> 6.1F 6.3C 7.1E 7.1G	FBC_DQ\$-2> 6.48 7.4C 7.5E	IFPC_PLLVDD 12:3A	PEX_RX14 2.5B 2.5G	PS_NVVDD_BOOT1 21:20	
March Marc	IDC_5V 19.4D FBA CLK0 3.4D 4.20.4.50			PBC_DQS:d> 6.48 7.40 7.5E FBC_DQS:d> 6.48 7.40 7.45		PEX.RX14* 2.58.2.5G PEX.RX15 2.58.2.5G		
Registration	FBA_CLK0* 3.4D 4.2A 4.2C 4.5G	FBA_D=42> 3.38 4.4D	7.1E 7.1G	FBC_DQS-5> 6.48 7.4D 7.5E	IFPC_TXC* 12:3D	PEX_RX15* 2.5B 2.5G	PS_NVVDD_EN* 21.2B	
Mile	FBA_CLK1 3.4D 4.2D 4.2F 4.5G	FBA_D-43> 3.38 4.4D	FBC_CMD<20> 6.3F 6.4C 7.1A 7.1C	FBC_DQS:6> 6.48 7.4E 7.5E	IFPC_TXC_C1 12:3F 12:4B	PEX_SMCLK 2.1B	PS_NVVDD_LG1 21:20	
Process State Process			7.1E 7.1G					
March Marc	FBA_CMD<30.0> 3.3D 4.1A 4.1C 4.1D	FBA_D<46> 3.38 4.4D	7.1E 7.1G	FBC_DQSN<7.0> 6.4A 7.3A 7.5E	IFPC_TXD0* 12:3D	PEX_TDI 2.1B	PS_NVVDD_PH2 21:3D	
March Marc	4.1F 4.5G	FBA_D<47> 3.38 4.4D	FBC_CMD<22> 6.1F 6.4C 7.1E 7.1G	FBC_DQSN<1> 6.48 7.48 7.5E	IFPC_TXID0_C1 12:3F 12:4B	PEX_TDO 2:18	PS_NVVDD_RC1 21:2F	
March Marc	FBA_CMD<1> 3.3C 3.4F 4.1A 4.1C 4.1E 4.1G	FBA_D<48> 3.38.4.3E FBA_D<40> 3.98.4.9F		FBC_DQSN<25	IFPC_TXXD_C1* 12.3F 12.4B IFPC_TXXD1	PEX_TERMP 2.5E PEX_TMS 2.1R	PS_NVVDD_RC2 21.3F PS_NVVDD_UG1 21.20	
Proc. Proc	FBA_CMD<2> 33C 34G 4.1A 4.1C	FBA_D-50> 3:38 4:4E	7.1E 7.1G	FBC_DQSN<45 6.48 7.4D 7.5E	IFPC_TXID1* 12:3D	PEX_TRST* 2.18	PS_NVVDD_UG1_R 212E	
## CF	FBA_CMD<3> 3.2G 3.3C 4.1A 4.1C	FBA_D-61> 3:38 4:4E	FBC_CMD<25> 6.40 6.4G 7:3A 7:3C	FBC_DQSN<5> 6.48.7.4D.7.5E	IFPC_TXD1_C1	PEX_TX0 2.1G.2.2D	PS_NVVDD_UG2 21.3D	
MAJOR MAJO	4.1E 4.1G	FBA_D<52> 3.38 4.4E	FBC_CMD<28> 6.2F 6.4C 7.1A 7.1C		IFPC_TXD1_C1* 123F 12.4B	PEX_TX0* 2:1G:2:2D	PS_NVVDD_UG2_R 21.3E	
March Marc	4.1E 4.1G	FBA_D-54> 3:38 4:4E	FBC_CMD<27> 6.4C 6.4G 7.2E 7.2G	FBC VREF0 7.3C 7.3E 7.4G	IFPC_TX02* 12.3D	PEX_TX1* 2:1G:2:20	PS_NVVDD_VCC12 21.2C	
Proc. 135 144	FBA_CMD<6> 3.3C 3.3G 4.1A 4.1C	FBA_D<55> 3.38 4.4E	FBC_CMD-28> 6.4C 7.2E 7.2G 7.3A	FBC_VREF1 7.3F.7.3H.7.4H	IFPC_TX02_C1 12:3F 12:4B	PEX_TX2 2.2D 2.2G	ROM_CS* 18.3D	
## 45 ## 50				FBC 200 7:3A				
Million STATE Million	PDM_CMIL/655 3.1G 3.3G 4.1A 4.1C 4.1E 4.1G			FBC_Z02 7.3E	IFPD_PLLVDD 13:3C	PEX_TX3	ROM_SO 182C 183D 183D ROM_SO 182C 183D 183D	
PACADES 250-24 ALE PACADES 250-25 PACADES 250-25	FBA_CMD<7> 33C 34F 4.1A 4.1C	FBA_D<59> 3.38 4.4E	FBC_D<1> 6.18 7.48	FBC_ZQ3 7.3G	IFPEF_JOVDO 14.3C	PEX_TX4 2.2G 2.3D	SNN_SV3AUX 2.1A	
## 14 10 PR_CODE 35 14 14 PR_CODE 15 15 PR_CODE 15 15	4.1E 4.1G			FBVDDQ 202H	IFP_JOVDD_EN* 17.2E 19.4G	PEX_TX4* 22G 23D	SNN_BIOB_HSYNC 15.4D	
Fig. Combination Fig. Combin	4.1E 4.1G	FBA_D-62> 3.38 4.4E	FBC_D<4> 6.18 7.48	FBVDDQ_VSEL 20.4E	IFP_PLLVDD 12.2A 19.2G	PEX_TXS* 2.2G.2.3D	SNN_BTXC* 11.3D	
## 44 0	FBA_CMD-d> 32F 33C 42A 42C	FBA_D<83> 3.38 4.4E	FBC_D<6> 6.18 7.48	FB_CAL_PD_VDDQ 6.5C	JTAG_TCLK 2.1C 17.4A	PEX_TX6 2.2G 2.3D	SNN_BUFRST* 184D	
## 45 C	4.2E 4.2G			FB_CAL_PU_GND 6.5C	JTAG_TDI 2.1C 17.4A	PEX_TX8* 2.2G 2.3D		
FRA_COMENT 373 SAC 45 45 50 FRA_COMENT 328 46 6 FRA_COMENT 328 46	. LAN, CARDON TO SEE 3.30 4.1A 4.1C 4.1E 4.1G	FBA_DQM<7.65 3.34.4.34.45G	- 30_0475 6.18 7.48 FBC_D485 6.18 7.48	FB_PLLAVDD 3.9C	JTAG_TMS 2:1C:17.4A	PEX_TX7* 22G 23D	SNN_FBA0_CS1 4.2A	
## AS FOR PROCESS 325 324 ALX C PROCESS 325 325 ALX A C PROCESS 325 325 ALX A C PROCESS 325 ALX A C PROCES	FBA_CMD<11> 3.1F 3.3C 4.1E 4.1G	FBA DQM<1> 3.38 4.48	FBC_D-db 6.18 7.48	GPI00_HP0_DVI 11.40	JTAG_TRST* 2.1C 17.5A	PEX_TX8	SNN FBA0 NC A1 4.3A	
FRA_CORNI	FBA_CMD<12> 3.10.3.3C 4.2A 4.2C	FBA_DOM-2> 3.38 4.40	FBC_D<10> 6.18 7.48	GP(00_HP0_DVI_Q 11.4D	MIOA_CLKIN 15.20	PEX_TX8* 22G 24D	SNN_FBAO_NC_A11 4.3A	
## ASK 40 FRA, DOM-6 38 44 45 FRA, DOM-6	FBA CMD<13> 3.3C 3.3G 4.2A 4.2C	FBA DQMo4> 3.38 4.4D	FBC D<12> 6.287.48			PEX TX9° 22G 24D	SNN FBA0 NC T11 4.3A	
FRA_CORN-1- 3 and 44E FRA_	4.2E.4.2G	FBA_DQM-5> 3.38 4.4D	FBC_D<13> 6.28 7.48	GPIO1_HPDC 12.4C	NVVDD 21.2H	PEX_TX10	SNN_FBA0_ODT1 42A	
FRA_DOMINION \$25.04.04.54.10	FBA_CMD<14> 3.3C 3.3F 4.1A 4.1C	FBA_DQM-6b 3.4B 4.4E	FBC_D<14> 6.28.7.48	GPI01_HPDC_Q 12.4D		PEX_TX10* 2.2G 2.4D	SNN_FBA0_ZQ1 4.2A	
FRA_CROIT \$23 23 344.34 10				GPI01_HPDC_R_L 12.4G				
FRA_DOSIGN SERVICE S	FBA_CMD<17> 3.3C 3.3G 4.1A 4.1C	FBA_DQS<7.0> 3.4A 4.3A 4.5E	FBC_D<17> 6:28 7:40	GPIO4_FAN_TACH 17:9C	NVVDD_CSN_R 21.3D	PEX_TX12	SNN_FBA1_NC_A1 4.9C	
## 43440 FBL,006-b 384-46-45E FBC,006-b 387-8C GP07/WIGU/RBIT 1793 124/14A PBL,006-b 384-46-45E FBC,006-b 387-8C GP07/WIGU/RBIT 1793 124/14A WOO, BP 179-78A PBL,TOT 1793 124/14A WOO, BP 179-78A WOO, BP 179								
FRA, D036-b 3 84 40 44 5E FRA, D036-b 3 84 40 40 40 40 40 40 40 40 40 40 40 40 40								
FBL, DOG-30- 349-44-44 E FBL DOG-50- 349-44-45 E FBL DOG-50- 4-93-7-0C FBL DOG-50- 349-44-45 E FBL DOG	FBA_CMD<19> 3.2G 3.3C 4.1A 4.1C	FBA_DQS-4> 3.48 4.4D 4.5E	FBC_D<21> 6.28 7.4C		NVVDD_EN* 17.1E	PEX_TX14 2.2G.2.5D	SNN_FBA1_0DT1 4.2C	
A 15 4 1 G PRA_DOBA* 3.48 4.45 E PRC_D-da* 6.28 7 AC OPPOR_FRAM_O 17 AF NVCO_CHO_SHORE 2.4F 2.48 PRA_C 230 230 BN. VPCO_CHO_SHORE 2.4F 2.48 PRA_C 230 BN. VPCO_CHO_SHO				P*		PEX_TX14* 2.2G 2.5D	SNN_FBA1_ZQ1 4.2C	
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