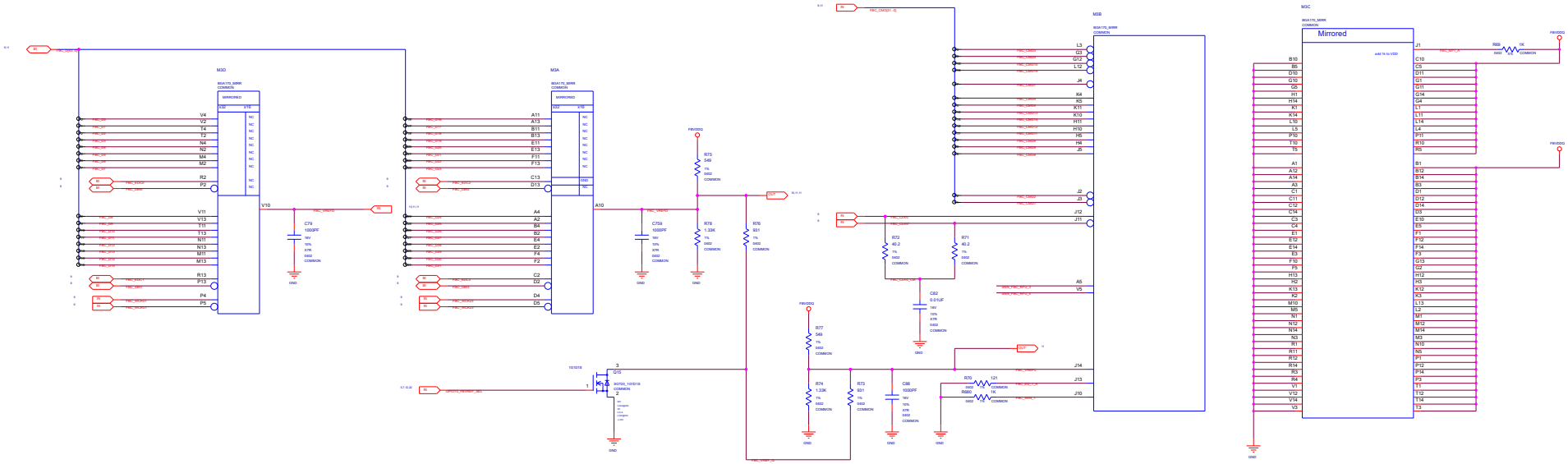

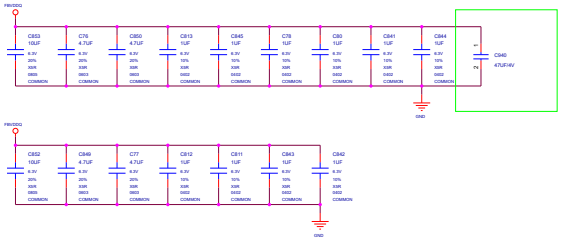

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBC[31:0]

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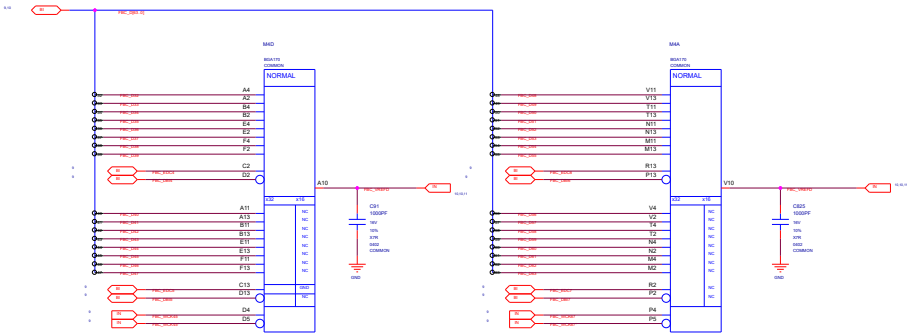

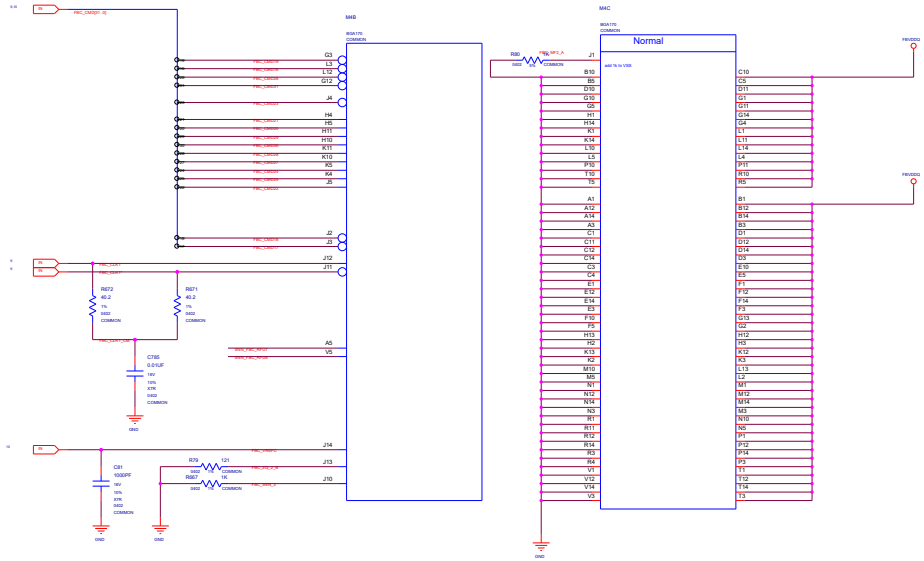

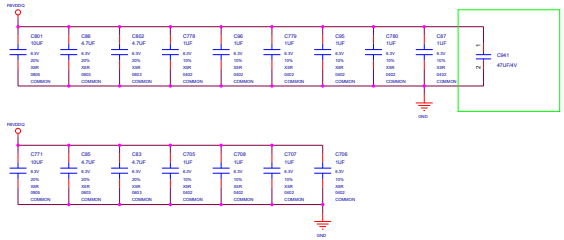

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBC[63:32]

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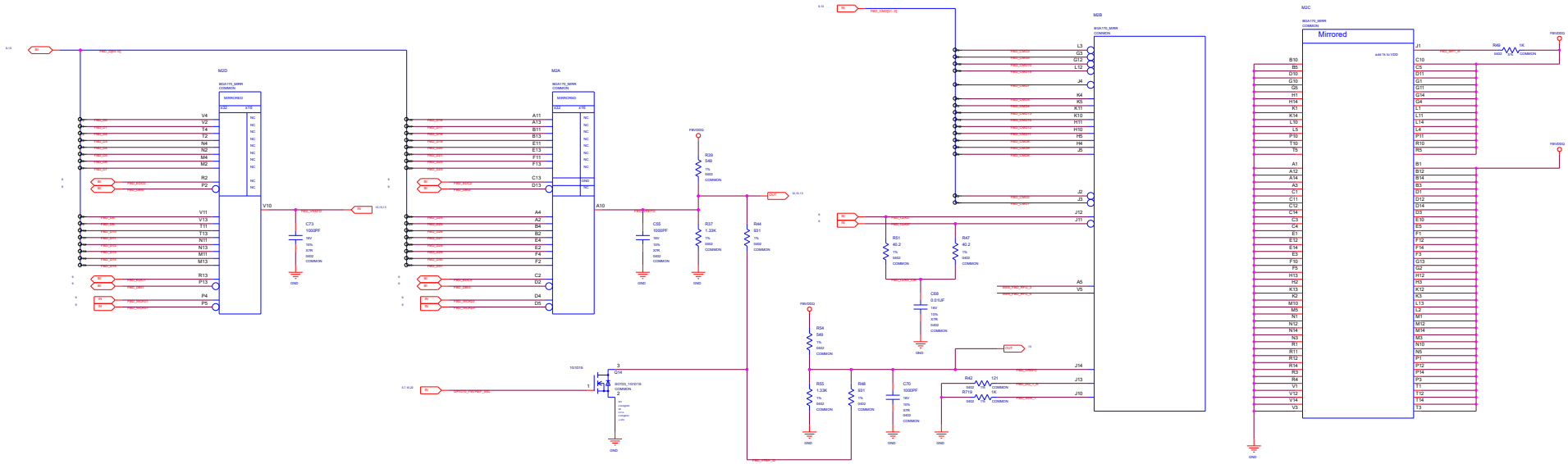
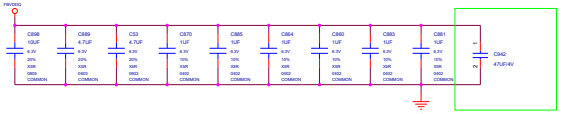
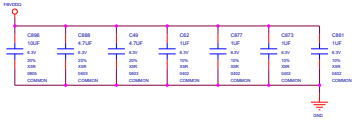
Page12: MEMORY: FBD Partition 31..0







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBD[31:0]

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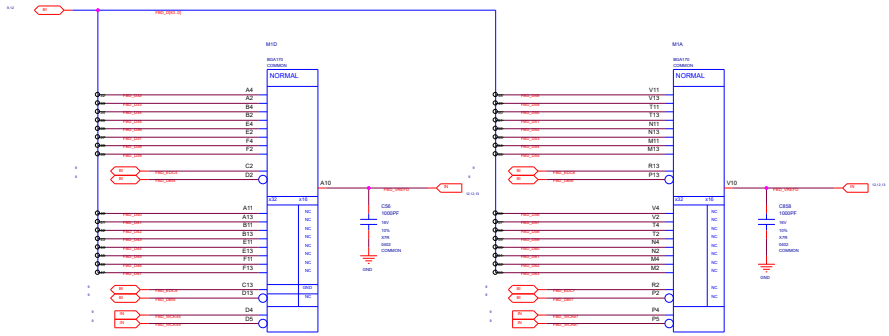
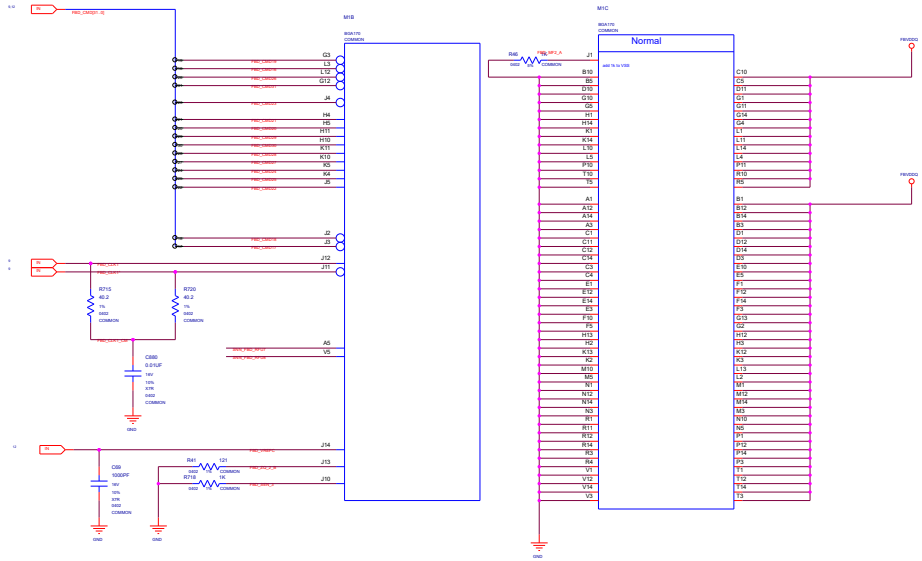
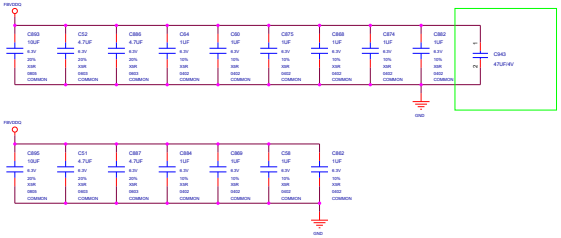
Page13: MEMORY: FBD Partition 63..32







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PAGE DETAIL	MEMORY: FBD[63:32]

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Page15: GPU Decoupling

Based on GB2-X GDDR5 FBVDDQ Decap Guideline

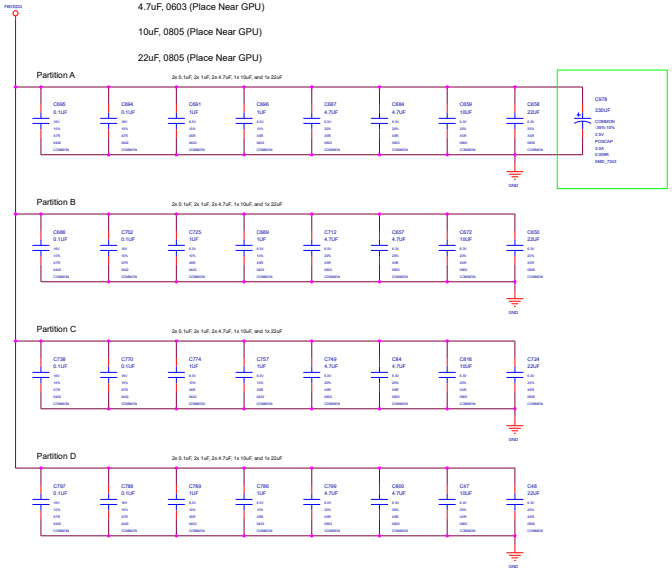
FBVDDQ

0.1uF, 0.47uF & 1uF, 0402 (Place Under GPU)

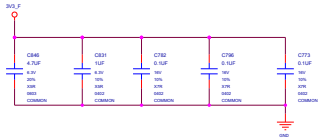
4.7uF, 0603 (Place Near GPU)

10uF, 0805 (Place Near GPU)

22uF, 0805 (Place Near GPU)

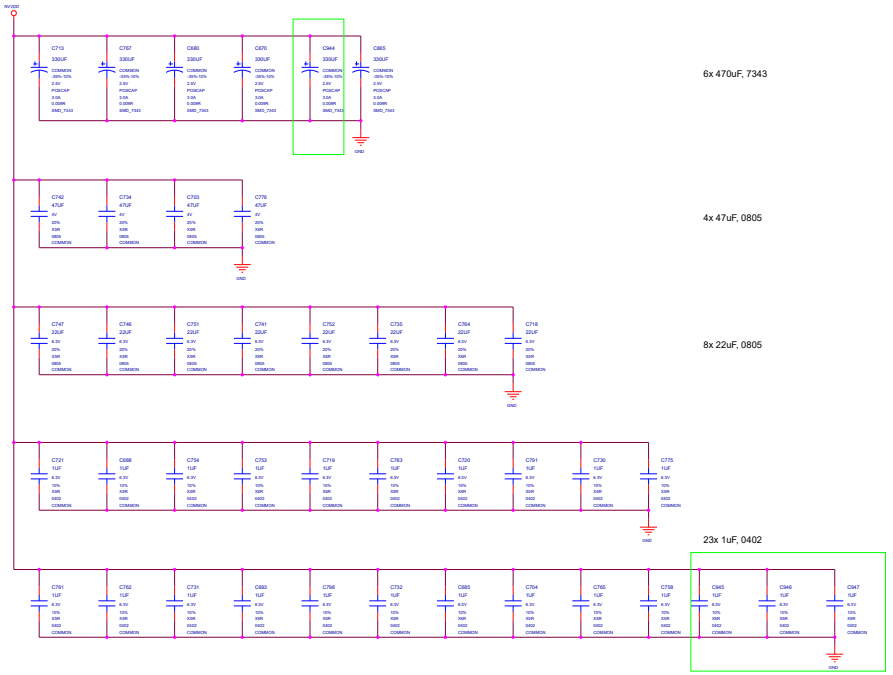


VDD33



NVVDD Decoupling caps. Place under GPU.

NVVDD



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU Decoupling

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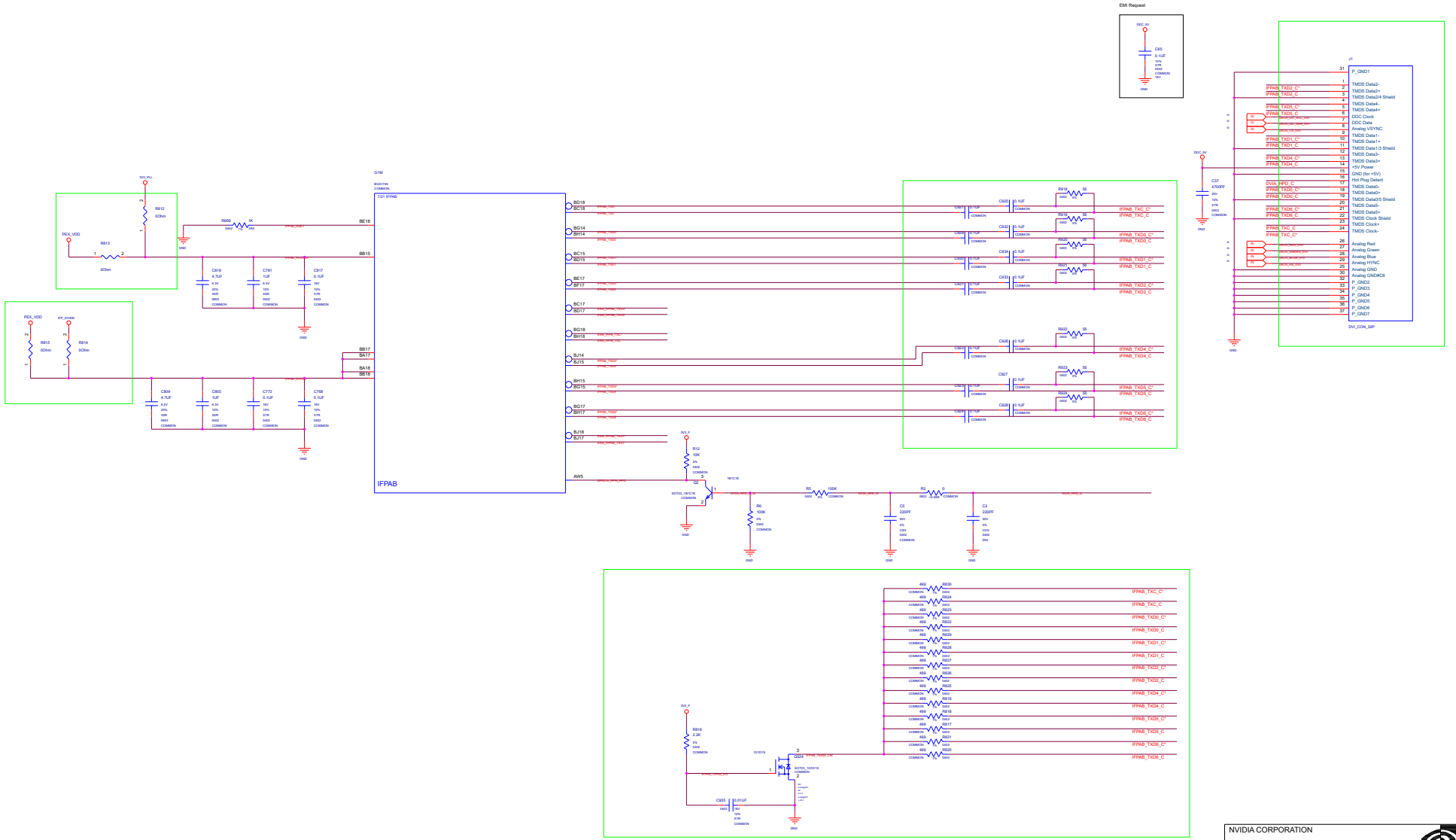
Page17: IFPAB DVI-I-DL



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPAB DVI-I-DL

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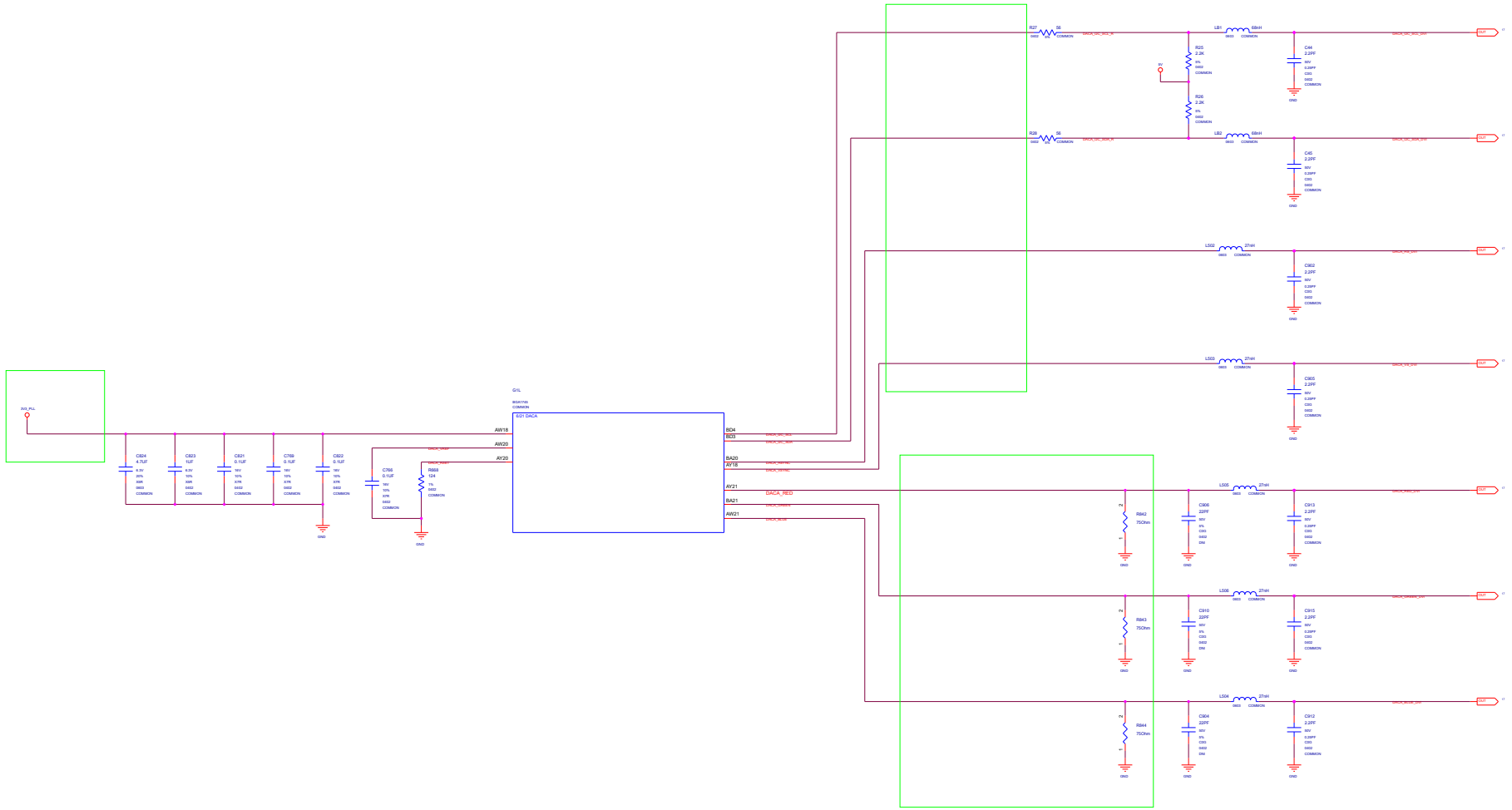
Page16: DACA Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DACA Interface

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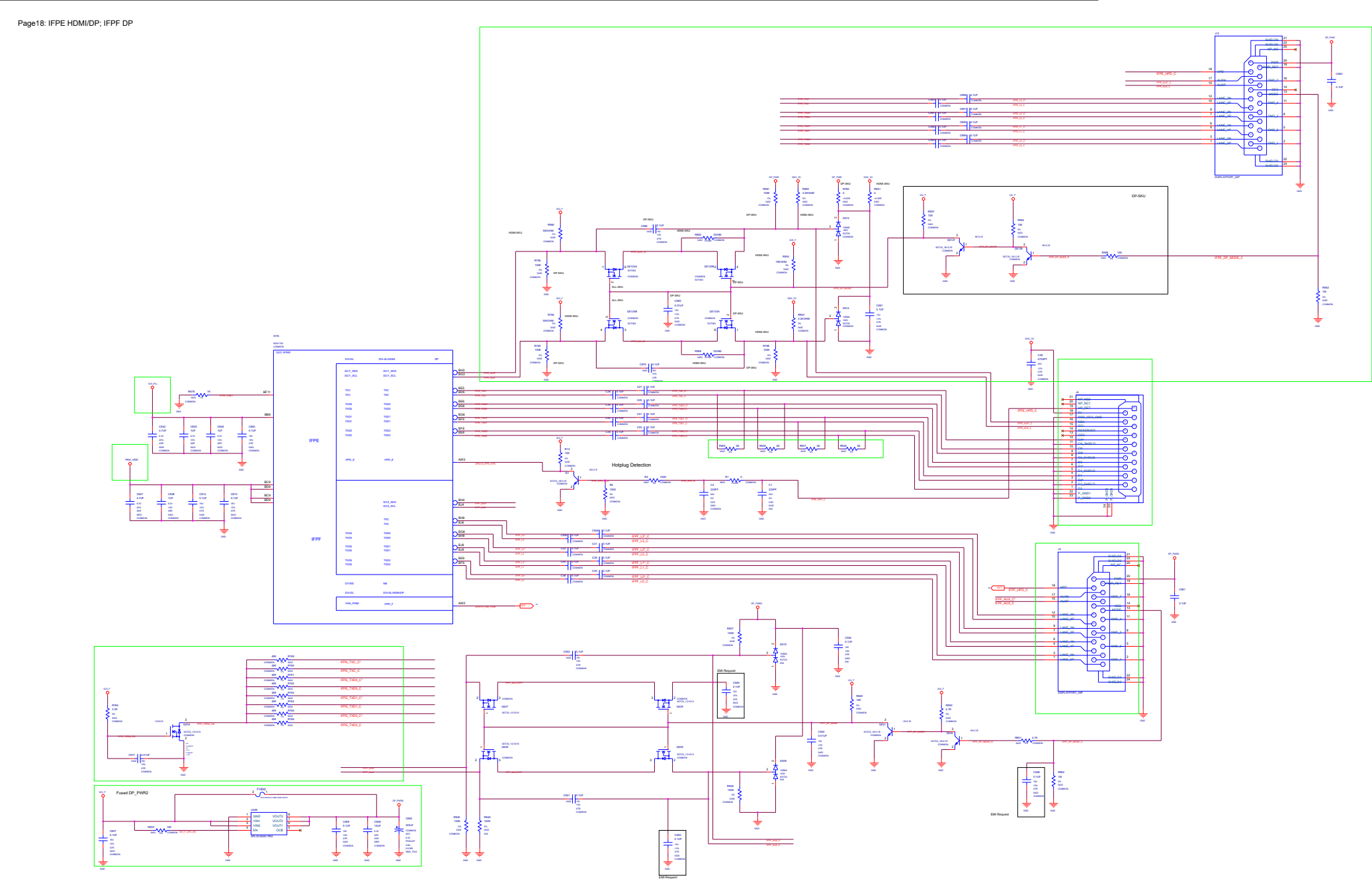
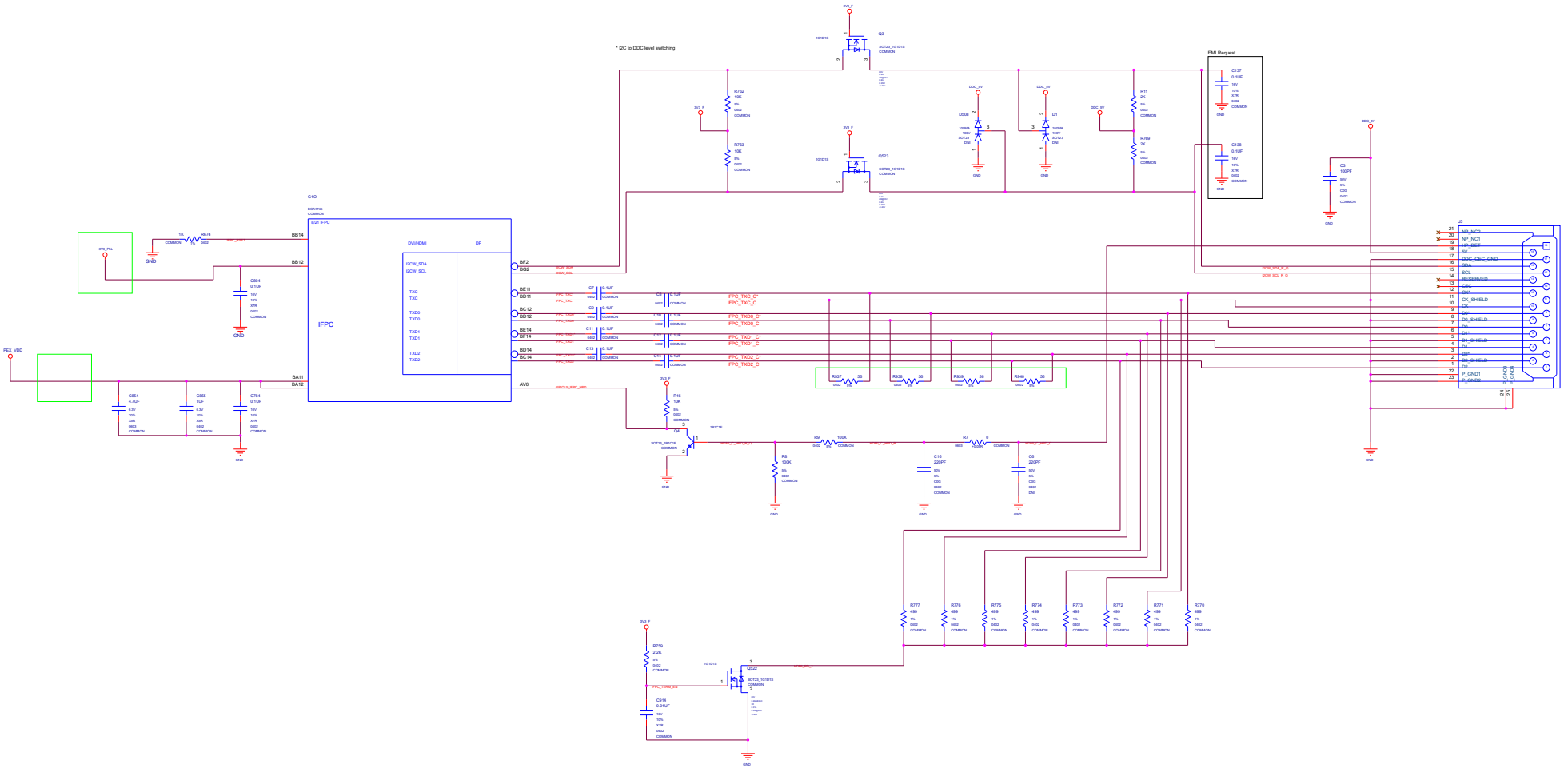

IFPE
IFPF
Hotplug Detection
Fused DP_PWR2
DISPLAYPORT_20P
EMI Request

Page19: IFPC HDMI



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPC HDMI

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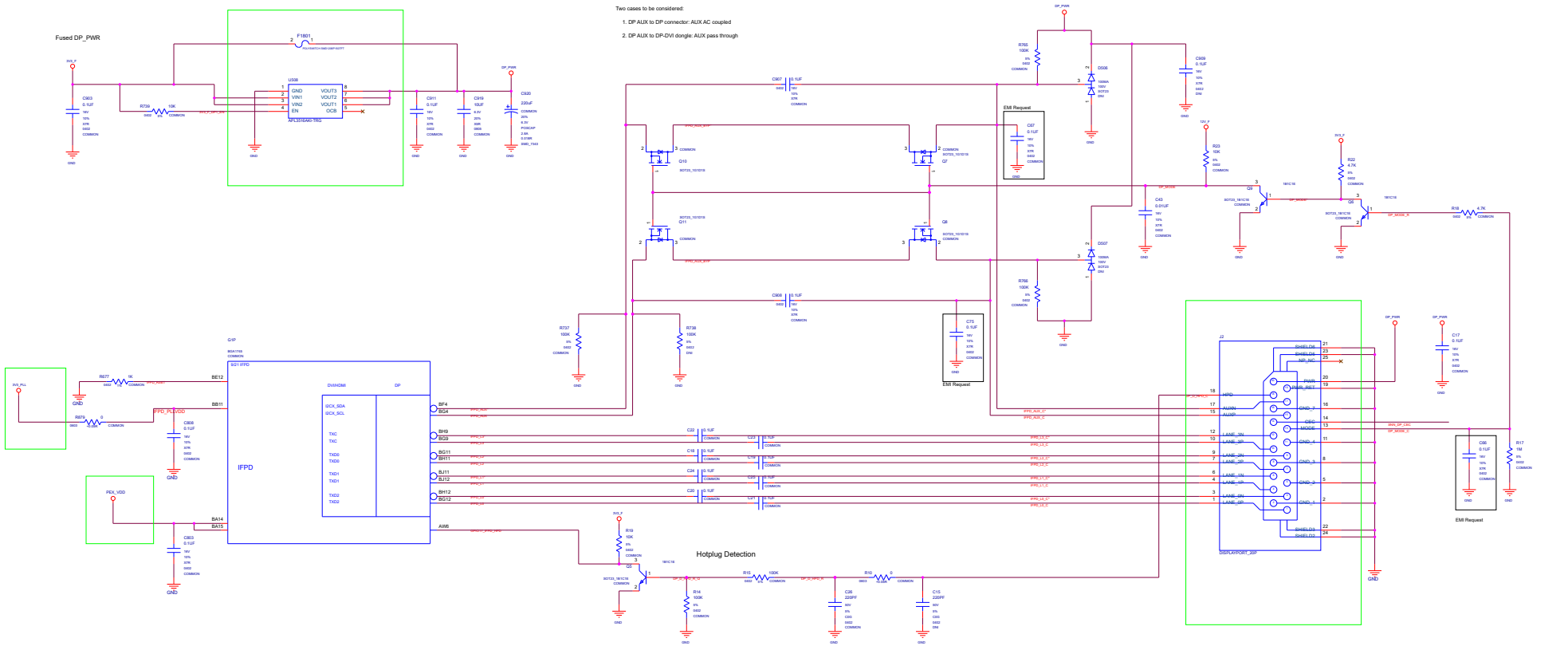
Page20: IFPD DP



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPD DP

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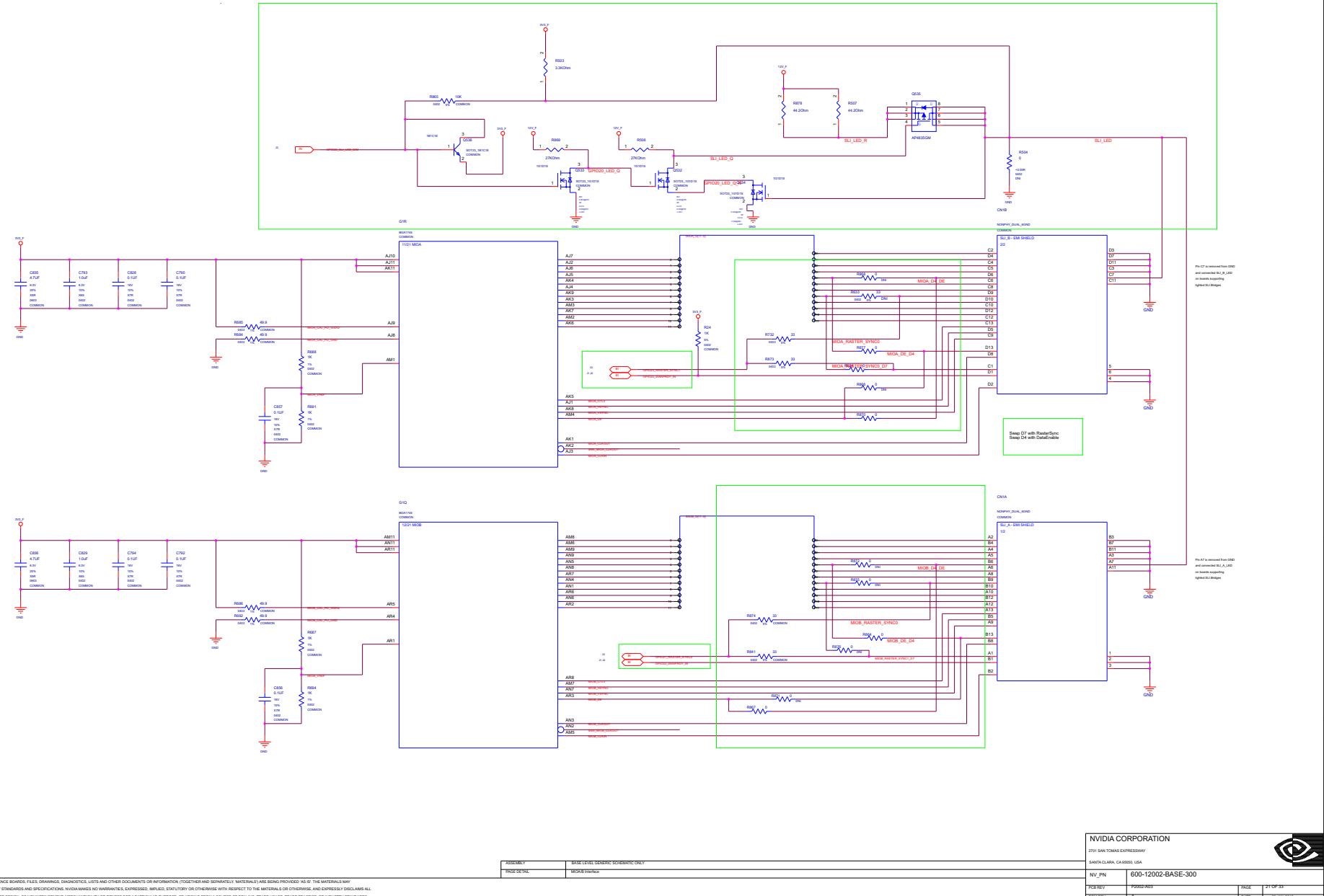
Page21: MIOA/B Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MIOA/B Interface

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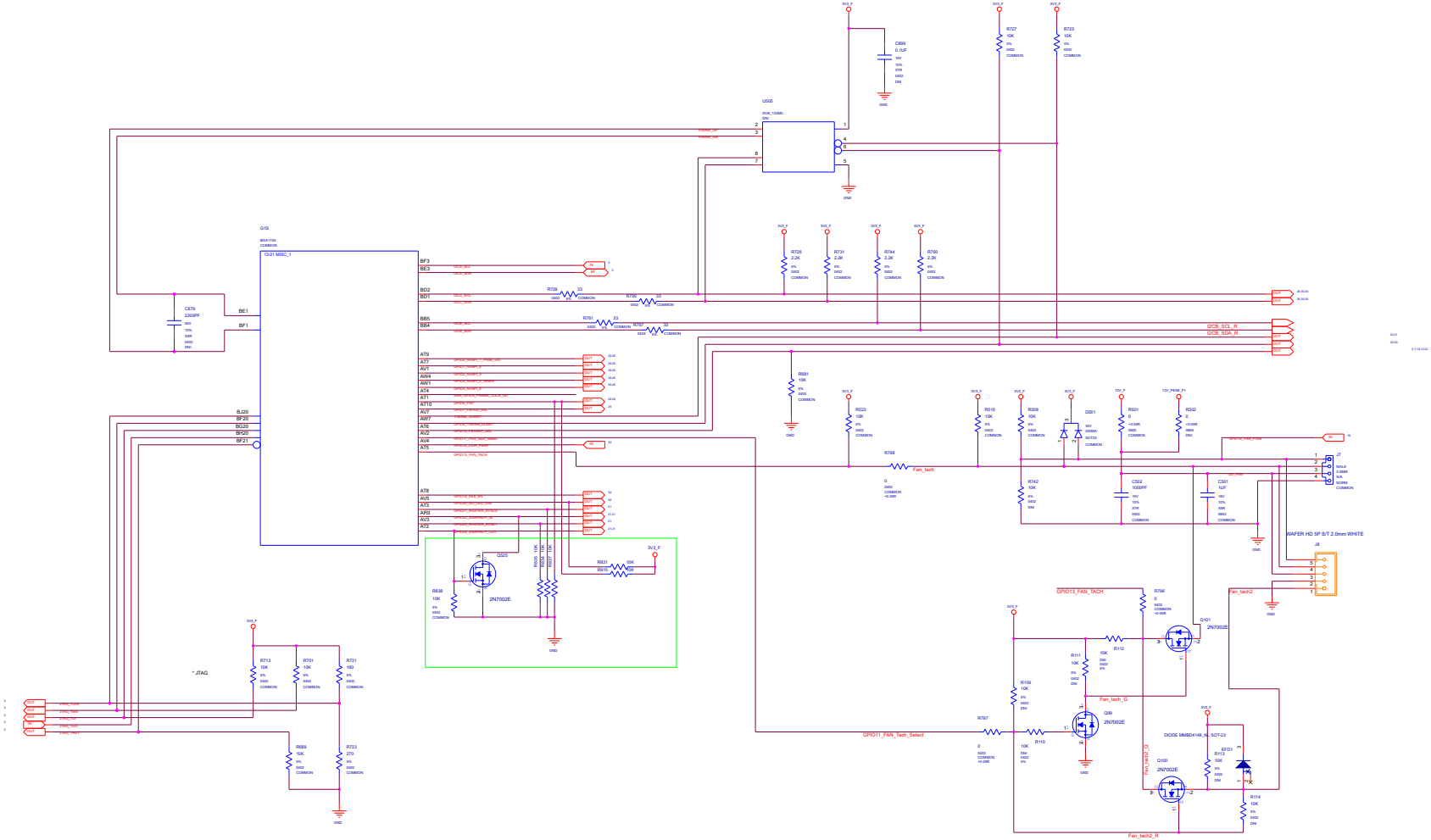
Page22: MISC1: Fan, Thermal, JTAG, GPIO



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO

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Page23: MISC2: ROM, XTAL, Straps

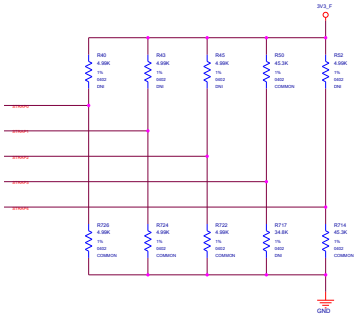
STRAP0	USER_BIT [3:0]*	0000*		5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*		5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0000 - (0x1180)*		5K PD -400 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*		45K PU*
STRAP4	DP_PLL_VDD_33V*	1*	FOR 3_3V*	
	PEX_MAX_SPEED*	1*	FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1*	ENABLED*	
	*			
ROM_SI	RAMCFG[0]*	0*		
	RAMCFG[1]*	1*		
	RAMCFG[2]*	1*		35K PD*
	RAMCFG[3]*	0*		
ROM_SO	VGA_DEVICE*	1*		
	SMB_ALT_ADDR*	0*		10k PU*
	FB[0]_APERTURE_SIZE*	0*	For 256MB*	
	FB[1]_APERTURE_SIZE*	1*	For 256MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0*	DISABLED*	
	PCI_DEVID_EXT[5]*	0*	For 0x1180*	25K PD*
	SUB_VENDOR*	1*	Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0*	For 0x1180*	

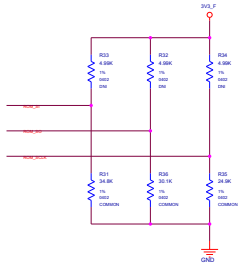
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

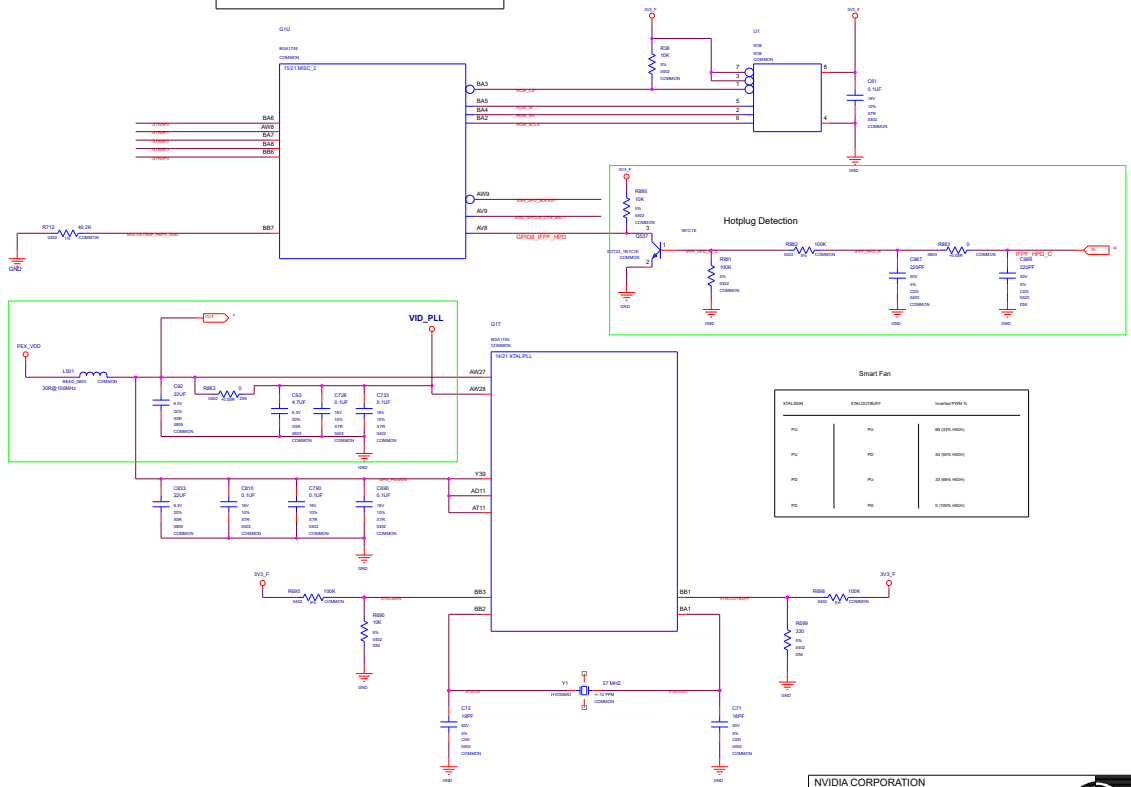
CFG[3:0] Config Width Vendor

0000 Reserved
0001 32Mx32 256-bit Elpida
0010 32Mx32 256-bit Hynix
0011 32Mx32 256-bit Samsung
0100 Reserved
0101 64Mx32 256-bit Elpida
0110 64Mx32 256-bit Hynix
0111 64Mx32 256-bit Samsung
1000 Reserved
1001 32Mx32 192-bit Elpida
1010 32Mx32 192-bit Hynix
1011 32Mx32 192-bit Samsung
1100 Reserved
1101 64Mx32 192-bit Elpida
1110 64Mx32 192-bit Hynix
1111 64Mx32 192-bit Samsung

MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2K 1% TO GND







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC2: ROM, XTAL, Straps

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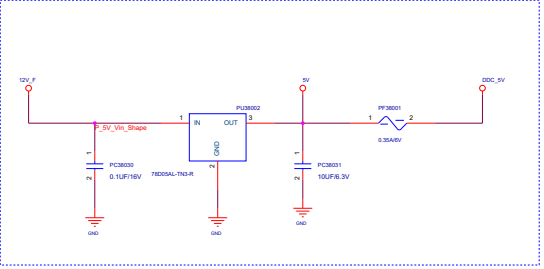
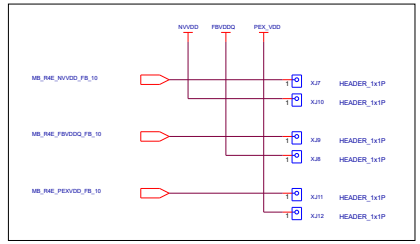
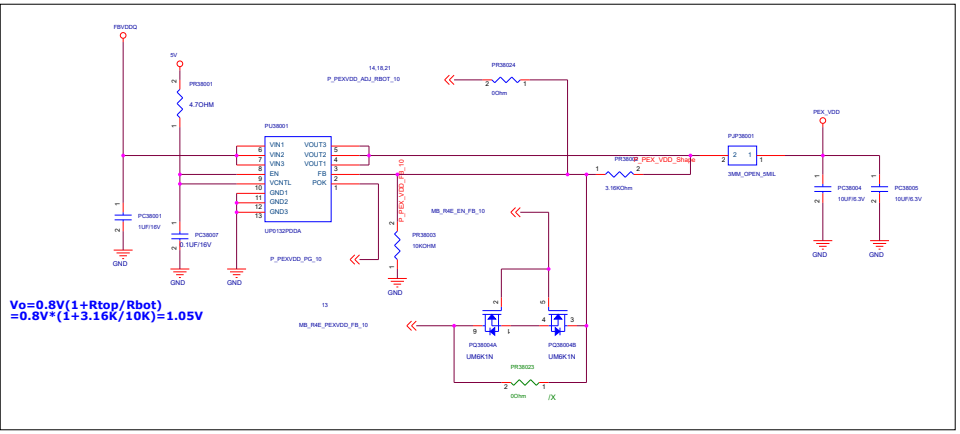
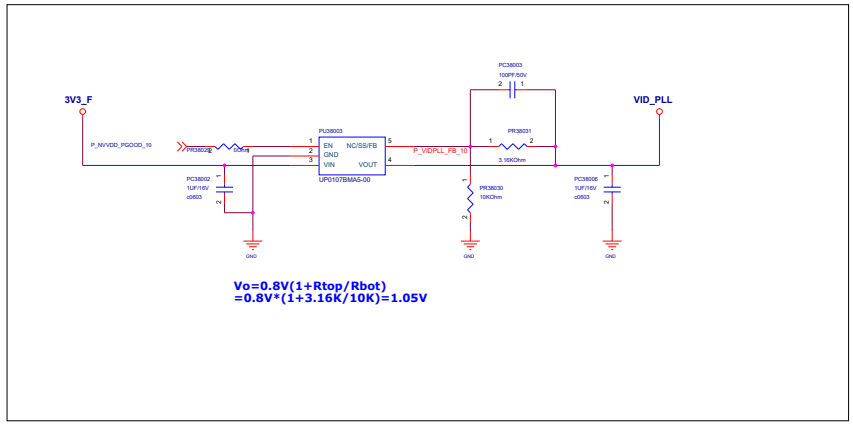
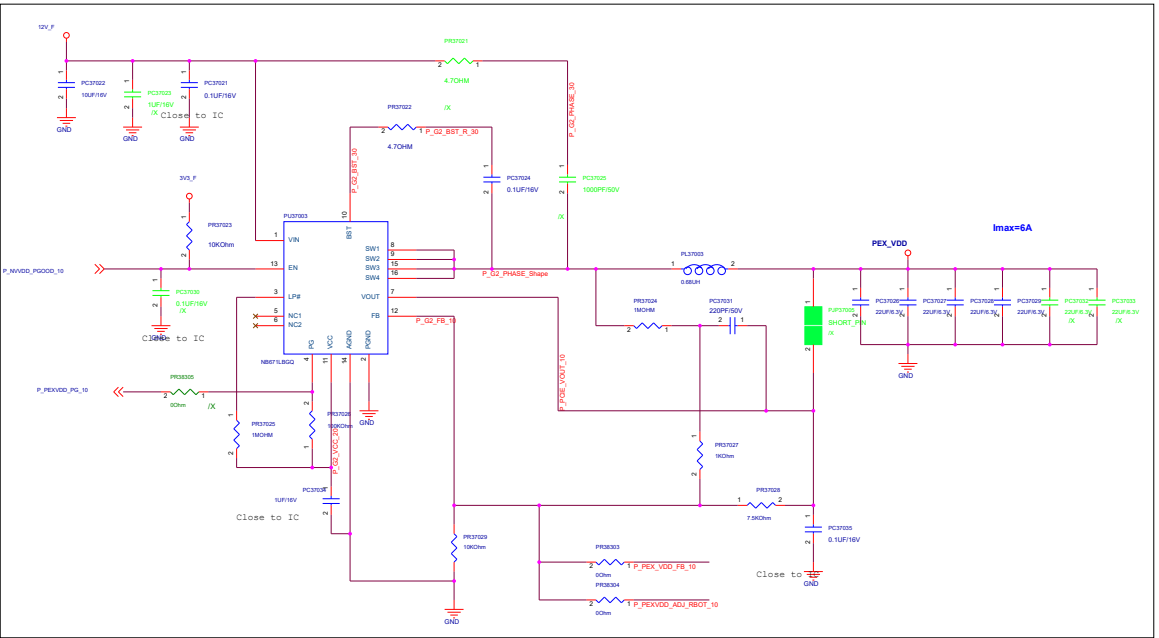


MB VGA Hotwire



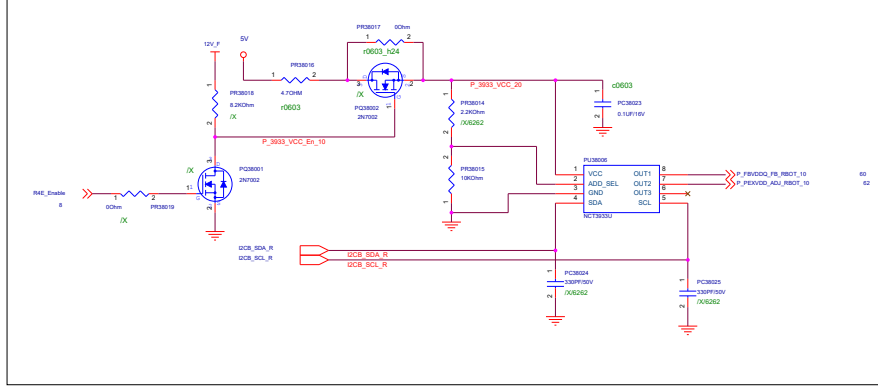


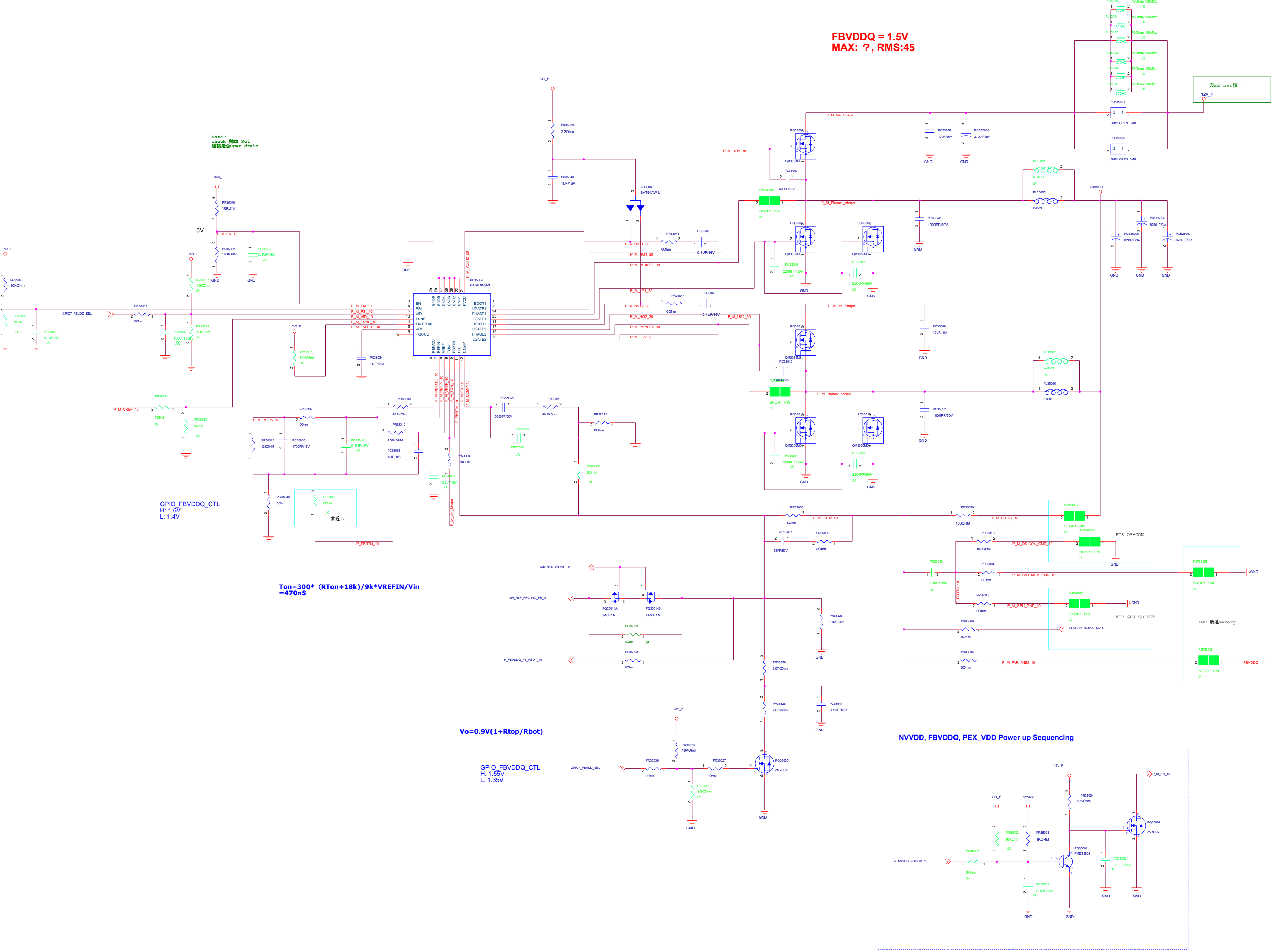




NCT3933U Over Voltage

Address : 0x2A





Power Info

1. I/P Current:

I in = Vo*Io/(0.75 * Vin) =6A

2. Ripple Current:

I rip =9A （Based on Iout=10A）
I spec=5230 mA ×2 pcs=10.46A

3. Dynamic:

I peak=45A
ESR/2 pcs =1.75 mohm
(One CAP for margin)
△V =78.75mV

4. Frequency:

PR12 = 31.6Kohm
F sw = 250 K HZ (Fixed)

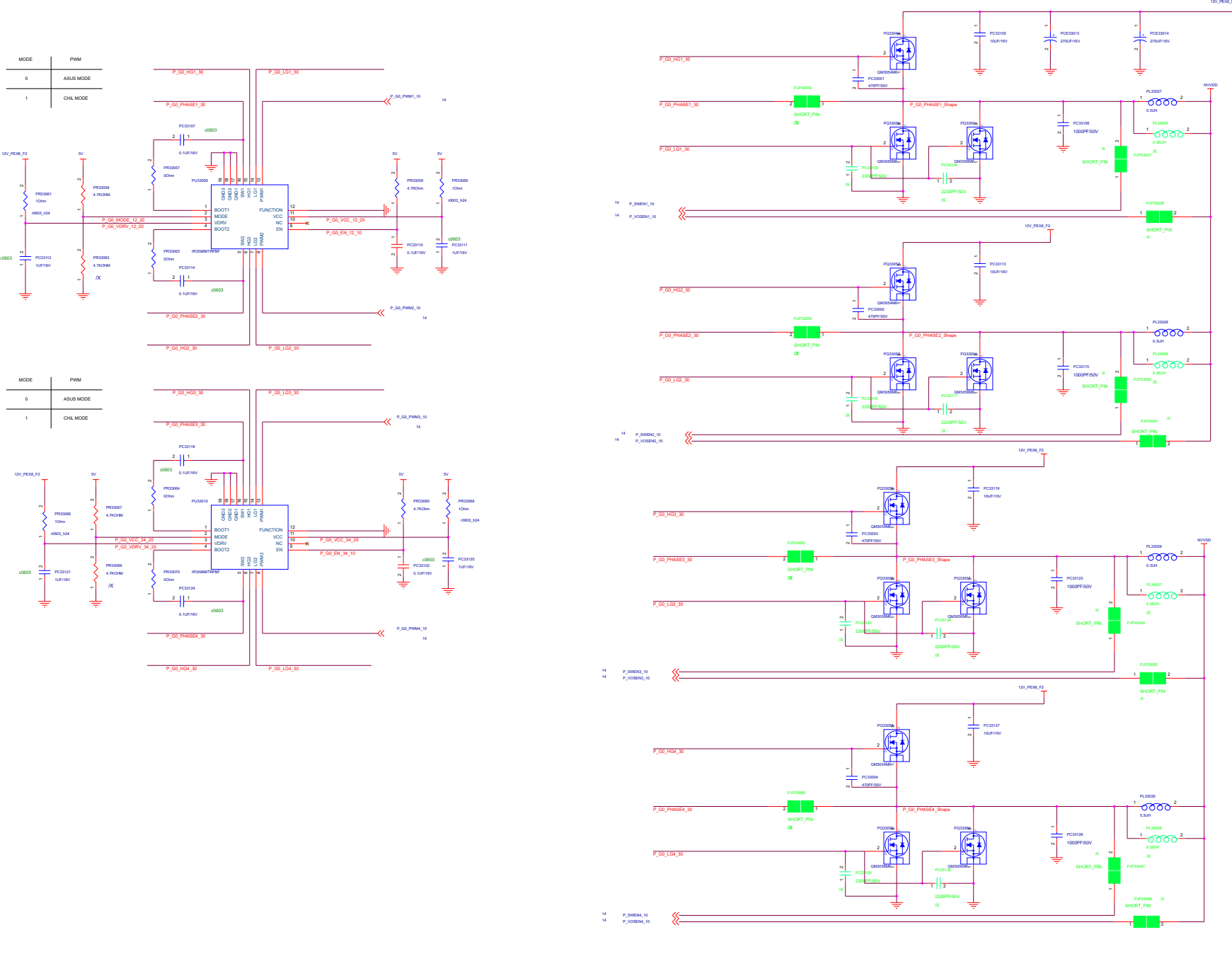
5. OCP:

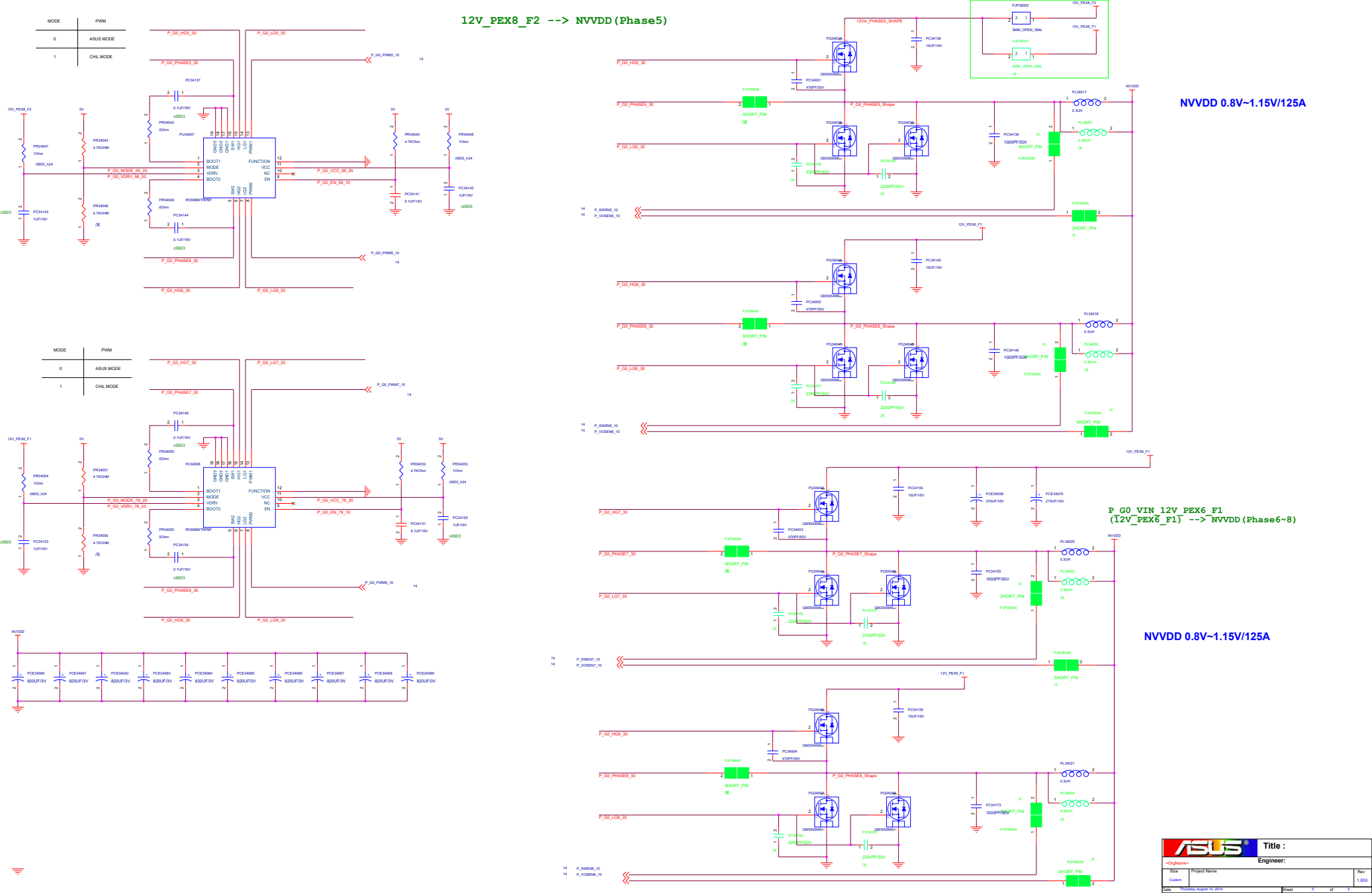
Set PR27= 15 K ohm
I ocp = 110 A

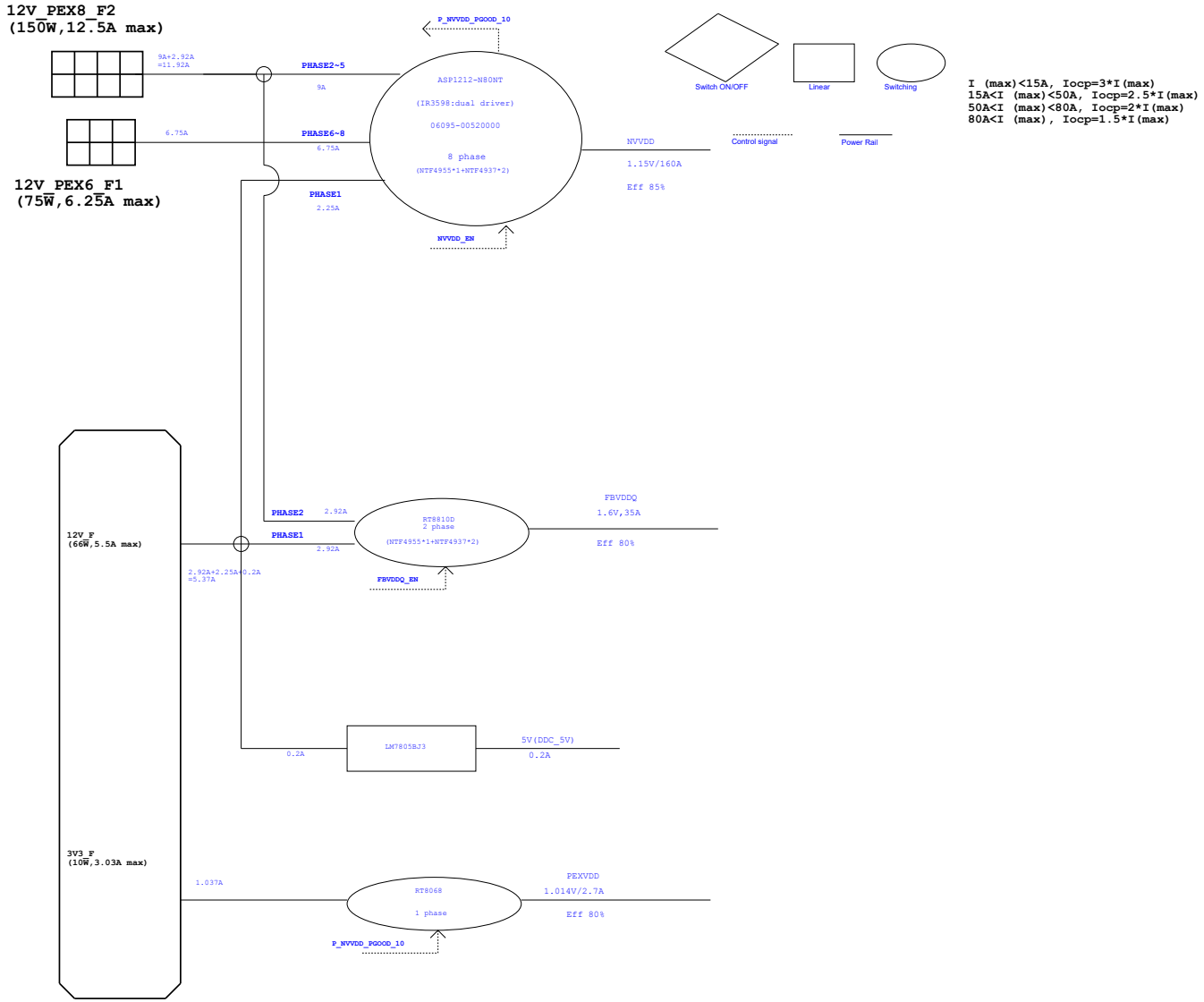
6. Phase selection:

14.9A 1p=>2p
9.96A 2p=>1p

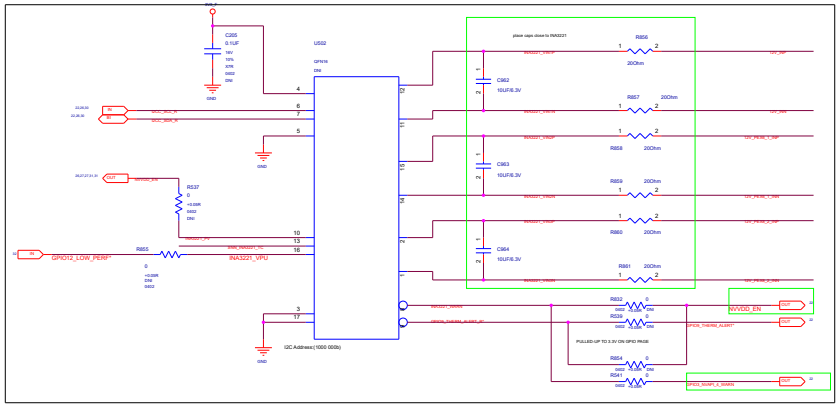
Title: VGA GPU 20A - 45A		
Size: A1	Document Number: Ripple_hu Power Team	Rev: <>
Date: Tuesday, September 23, 2014	Sheet 4 of 4	


MODE
PWM
0
ASUS MODE
1
CHIL MODE
P_G0_HG1_30
P_G0_LG1_30
P_G0_PHASE1_30
P_G0_PWM1_10
P_G0_MODE_12_20
P_G0_VDRV_12_20
P_G0_VCC_12_20
P_G0_EN_12_10
P_G0_PWM2_10
P_G0_PHASE2_30
P_G0_HG2_30
P_G0_LG2_30
12V_PEX8_F2
5V
PU33009
PU33010
BOOT1
MODE
VDRV
BOOT2
FUNCTION
VCC
NC
EN
PWM1
PWM2
IR3598MTRPBF
P_G0_HG3_30
P_G0_LG3_30
P_G0_PHASE3_30
P_G0_PWM3_10
P_G0_VCC_34_20
P_G0_VDRV_34_20
P_G0_EN_34_10
P_G0_PWM4_10
P_G0_PHASE4_30
P_G0_HG4_30
P_G0_LG4_30
P_G0_HG1_30
P_G0_PHASE1_30
P_G0_LG1_30
P_G0_PHASE1_Shape
P_SWEN1_10
P_VOSEN1_10
P_G0_HG2_30
P_G0_PHASE2_30
P_G0_LG2_30
P_G0_PHASE2_Shape
P_SWEN2_10
P_VOSEN2_10
P_G0_HG3_30
P_G0_PHASE3_30
P_G0_LG3_30
P_G0_PHASE3_Shape
P_SWEN3_10
P_VOSEN3_10
P_G0_HG4_30
P_G0_PHASE4_30
P_G0_LG4_30
P_G0_PHASE4_Shape
P_SWEN4_10
P_VOSEN4_10
NVVDD
SHORT_PIN
QM3054MD
QM3056MD
0.1UF/16V
1UF/16V
10UF/16V
470PF/50V
2200PF/50V
1000PF/50V
270UF/16V
0.3UH
0.36UH
NVVDD 0.8V~1.15V/125A
Title :
Engineer:
Size
Custom
Project Name
Rev
1.00X
Date:
Thursday, August 14, 2014
Sheet
5
of
6

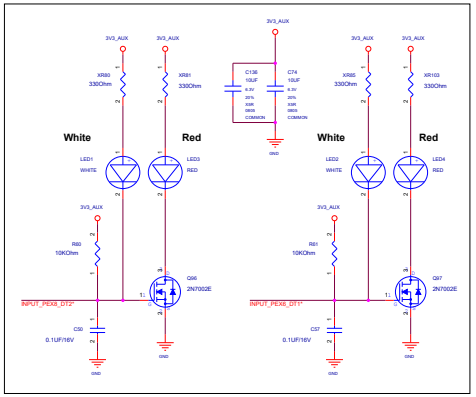

12V_PEX8_F2 --> NVVDD(Phase5)
NVVDD 0.8V~1.15V/125A
P_G0_VIN_12V_PEX6_F1
(12V_PEX6_F1) --> NVVDD(Phase6~8)
NVVDD 0.8V~1.15V/125A
MODE
PWM
0
ASUS MODE
1
CHIL MODE
Title :
Engineer:

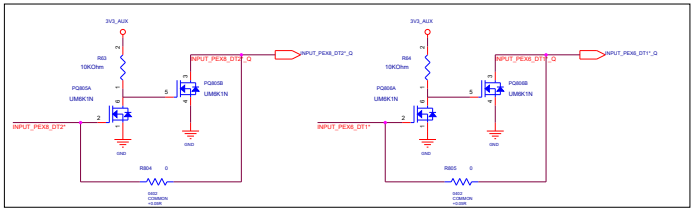

12V_PEX8_F2
(150W,12.5A max)
9A+2.92A
=11.92A
PHASE2~5
9A
6.75A
PHASE6~8
6.75A
12V_PEX6_F1
(75W,6.25A max)
P_NVVDD_PGOOD_10
ASP1212-N80NT
(IR3598:dual driver)
06095-00520000
8 phase
(NTF4955*1+NTF4937*2)
PHASE1
2.25A
NVVDD_EN
NVVDD
1.15V/160A
Eff 85%
Switch ON/OFF
Linear
Switching
Control signal
Power Rail
I (max)<15A, Iocp=3*I(max)
15A<I (max)<50A, Iocp=2.5*I(max)
50A<I (max)<80A, Iocp=2*I(max)
80A<I (max), Iocp=1.5*I(max)
12V_F
(66W,5.5A max)
PHASE2
2.92A
PHASE1
2.92A
2.92A+2.25A+0.2A
=5.37A
RT8810D
2 phase
(NTF4955*1+NTF4937*2)
FBVDDQ_EN
FBVDDQ
1.6V,35A
Eff 80%
0.2A
LM7805BJ3
5V(DDC_5V)
0.2A
3V3_F
(10W,3.03A max)
1.037A
RT8068
1 phase
P_NVVDD_PGOOD_10
PEXVDD
1.014V/2.7A
Eff 80%

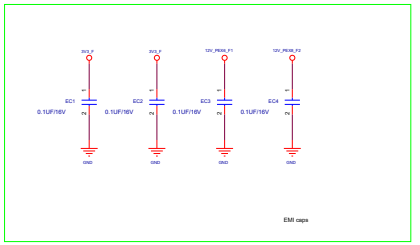
Page30: PS: Inputs, Filtering, and Monitoring

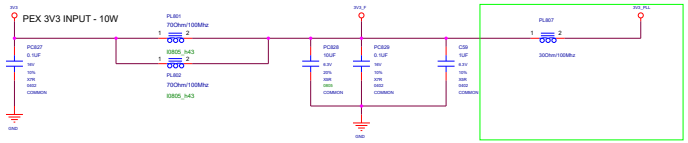


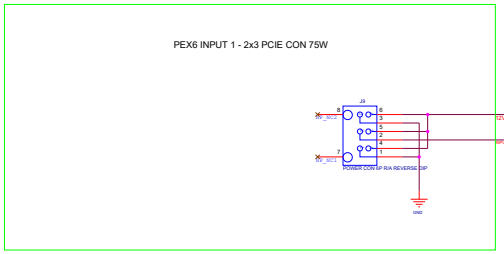
External Power LED

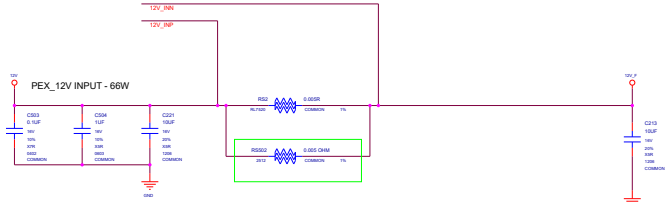


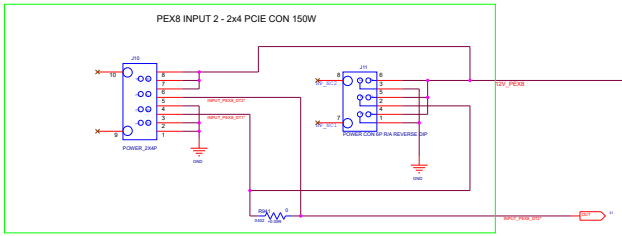












Current	ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
	PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

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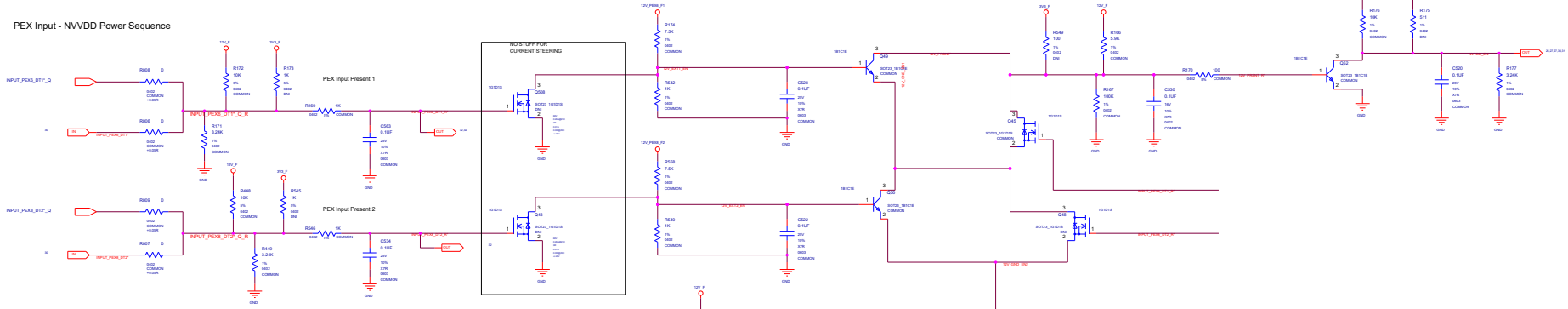
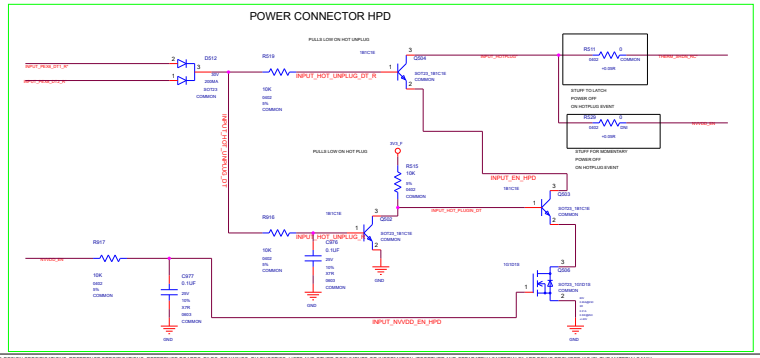
Page31: PS: Shutdown

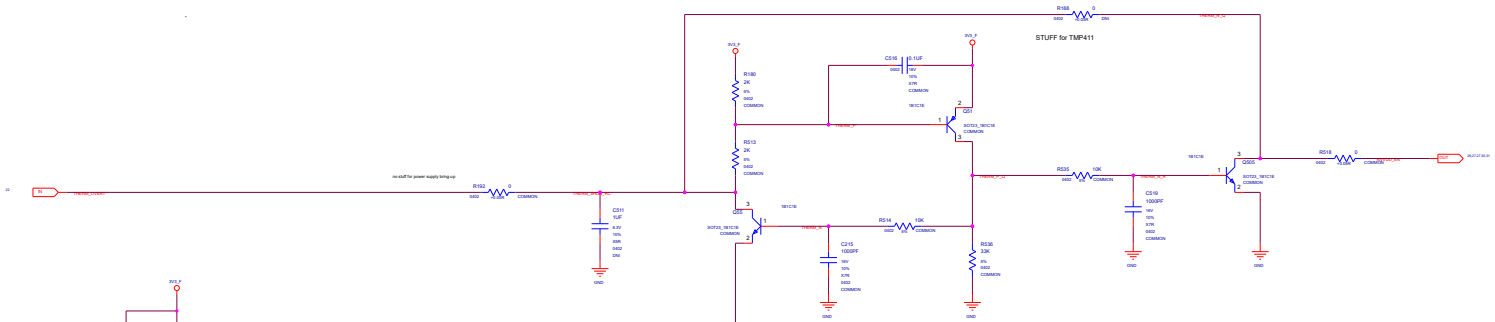
THERM OVERT SHUTDOWN LATCH

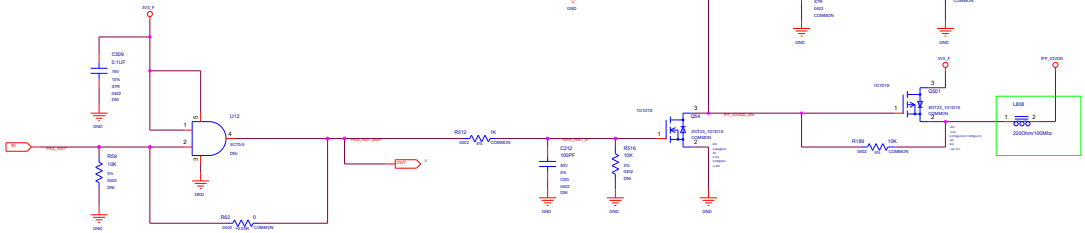
IFP_IOVDD (backdrive prevention)

PEX Input - NVVDD Power Sequence









ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Shutdown

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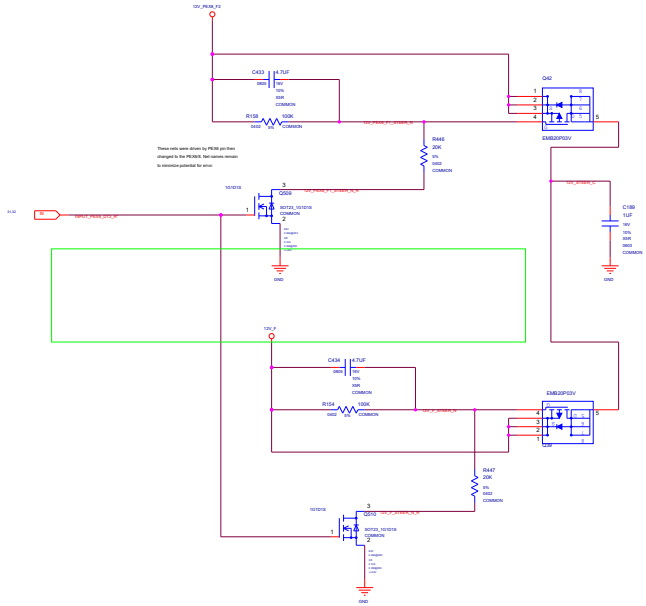
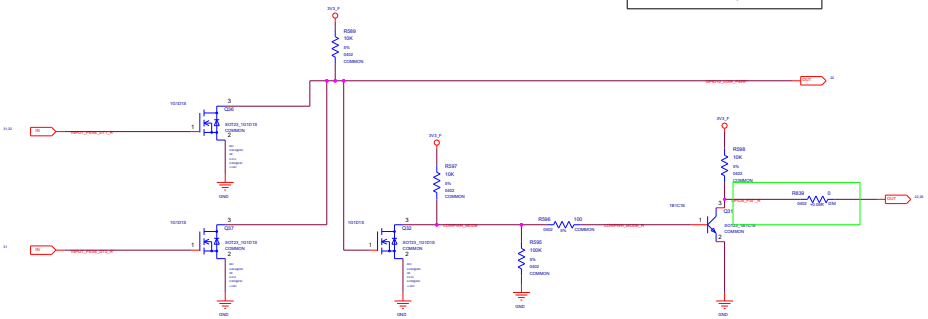
Page32: PS: 12V Current Steering, PSI Control, and LED

PEX Input - 12V Current Steering FETs



PEX Input - Power Level/PSI* Control

GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 12V Current Steering PSI Control and LED

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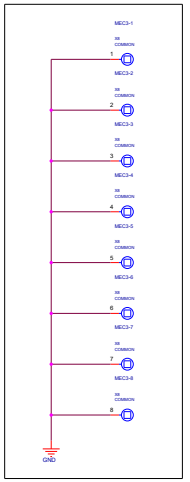
Page33: Mechanical: Bracket/Thermal Solution

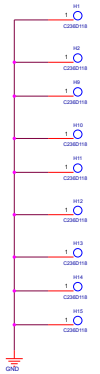
Brackets:

Bracket Screw

Hockey Stick

GPU Stiffner





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PAGE DETAIL	MECH: Bracket/Thermal

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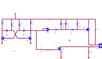
Page35: GPU Loading LED



C2002PGI

4GB GDDR5, 256b, 128Mx32

Tall DVI-I + DP x 2 + HDMI x 2

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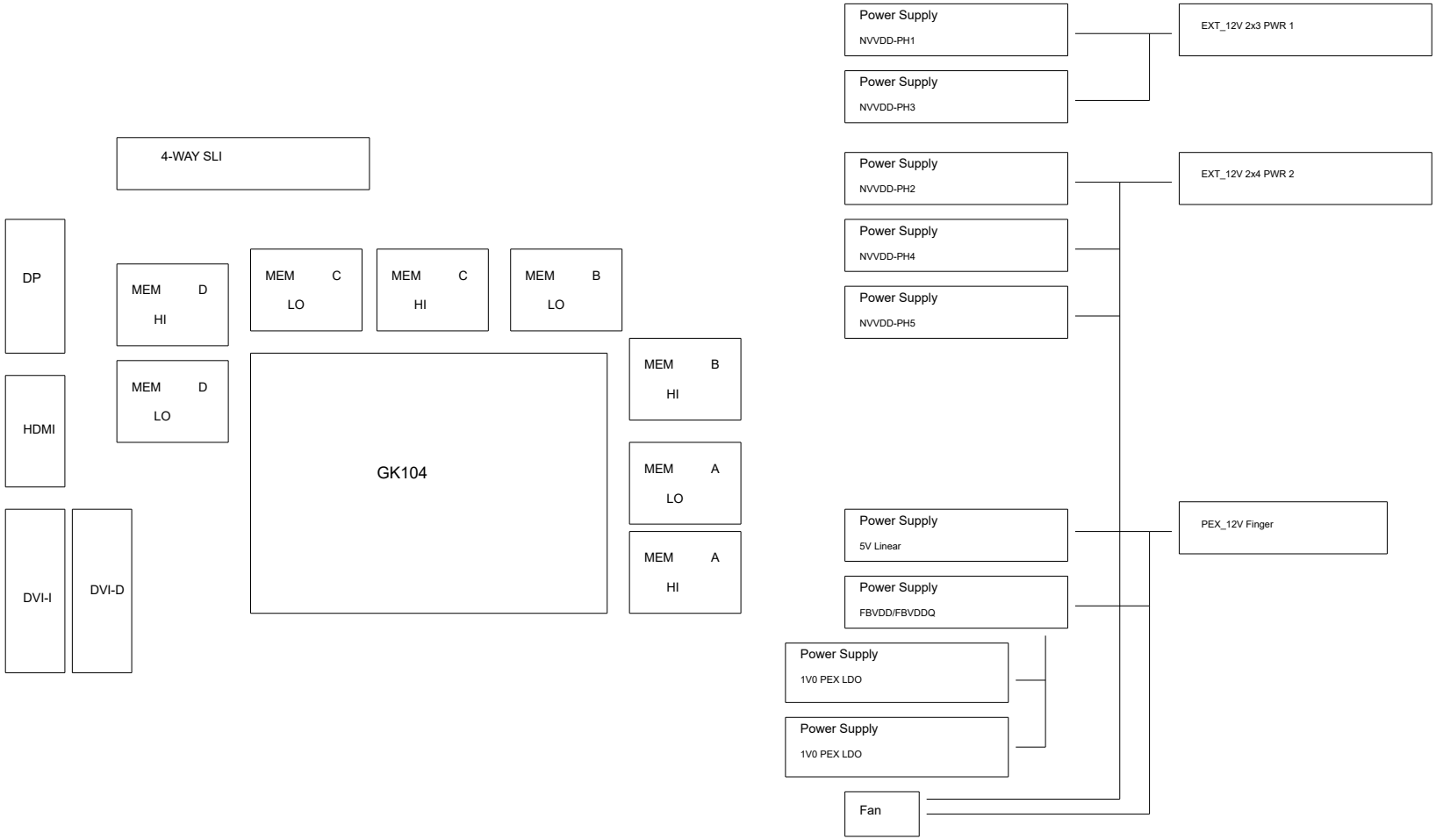
Page2: Block Diagram



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PAGE DETAIL	Block Diagram

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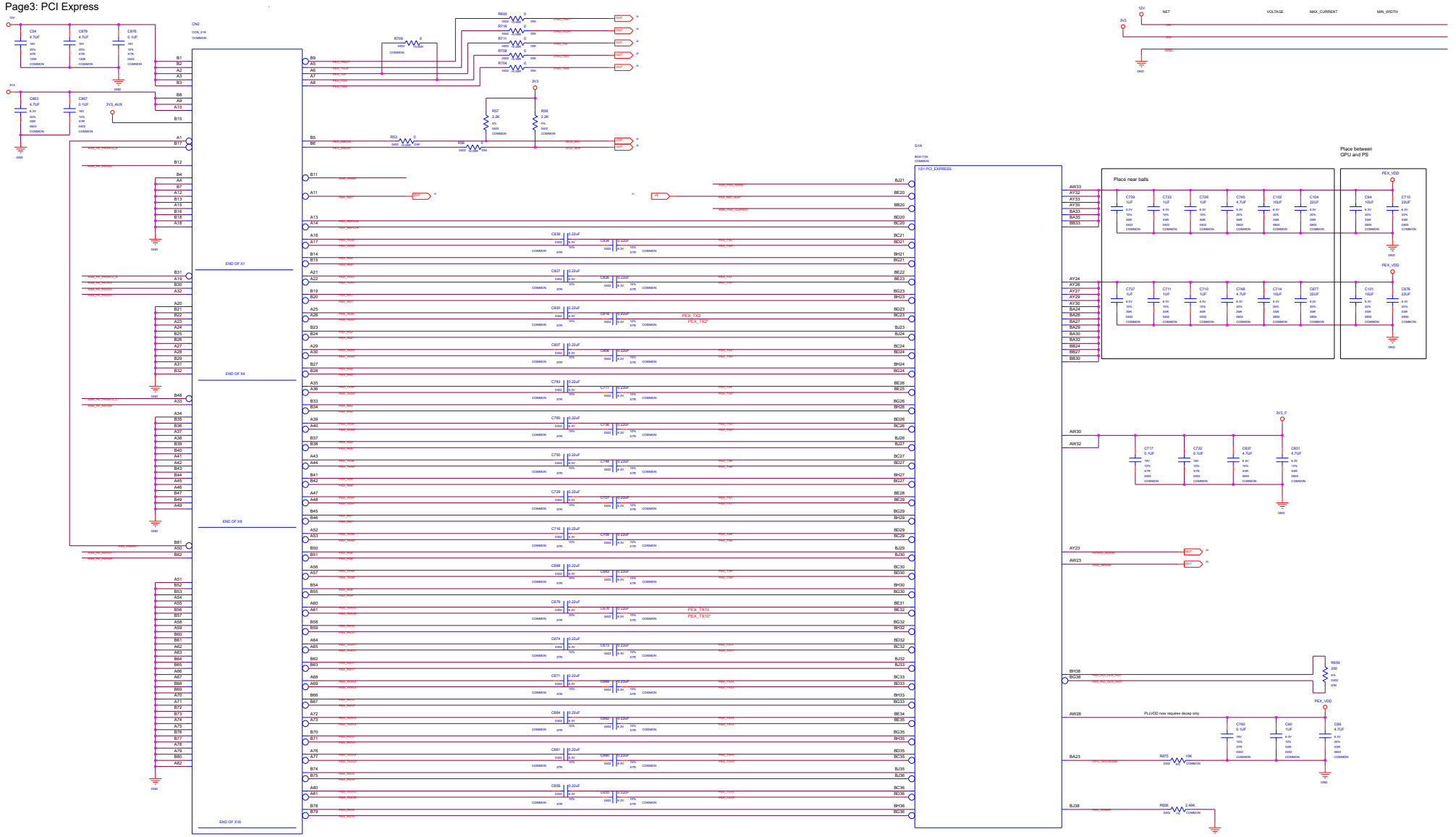
Page3: PCI Express



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PCI Express

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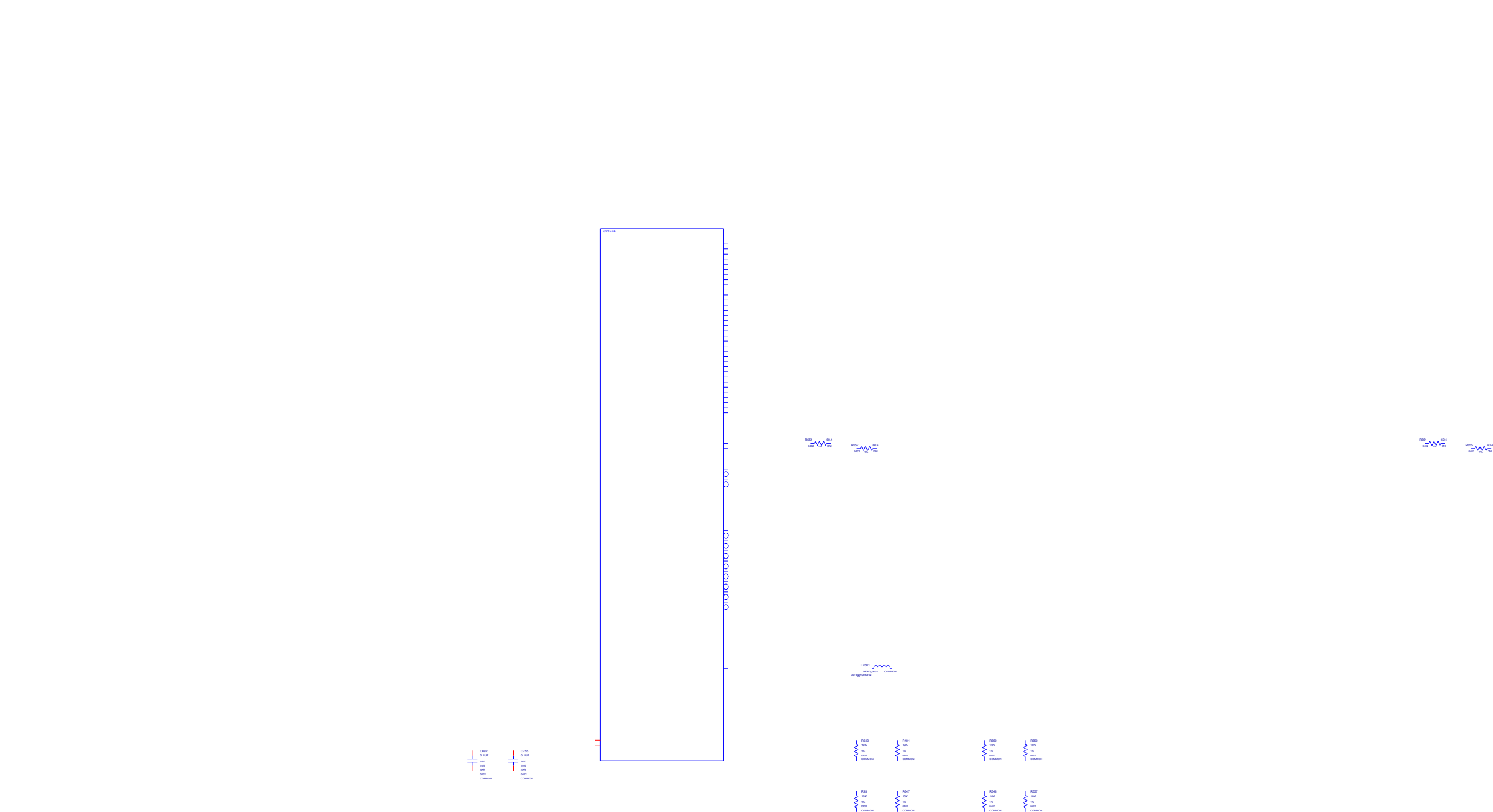
2/21 FBA
R651
60.4
0402
1%
R652
60.4
0402
1%
R661
60.4
0402
1%
R665
60.4
0402
1%
LBS01
WIND_0603
COMMON
30R@100MHz
C692
0.1UF
16V
10%
X7R
0402
COMMON
C755
0.1UF
16V
10%
X7R
0402
COMMON
R649
10K
1%
0402
COMMON
R101
10K
1%
0402
COMMON
R660
10K
1%
0402
COMMON
R650
10K
1%
0402
COMMON
R93
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1%
0402
COMMON
R647
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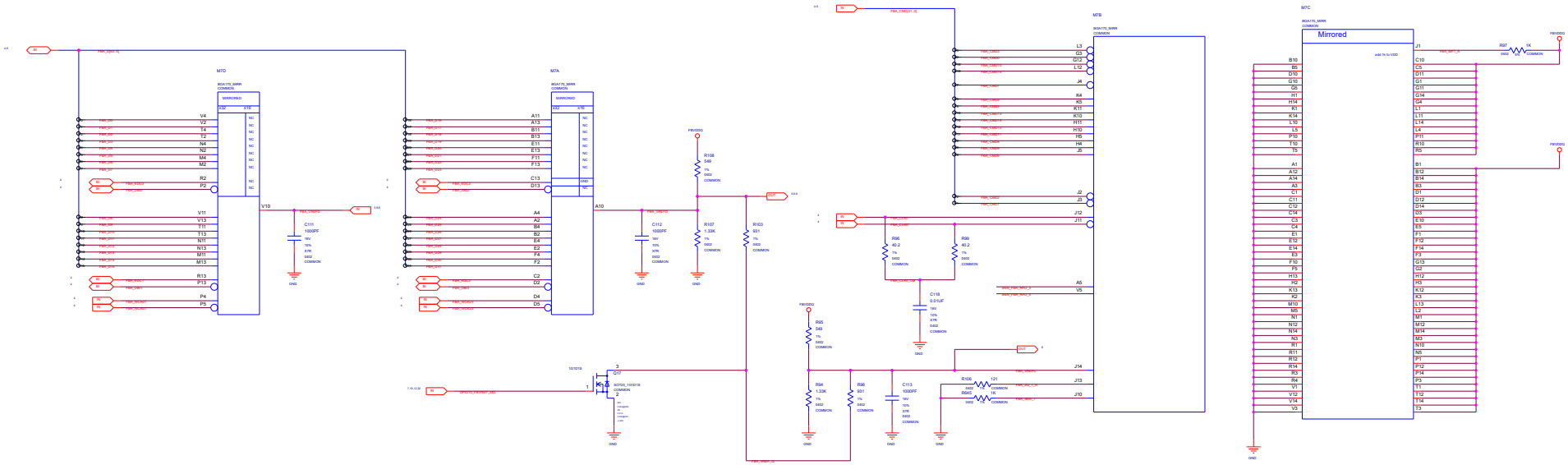
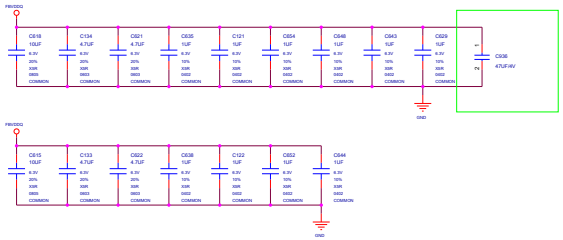
0402
COMMON

Page5: MEMORY: FBA Partition 31..0





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PAGE DETAIL	MEMORY: FBA[31:0]

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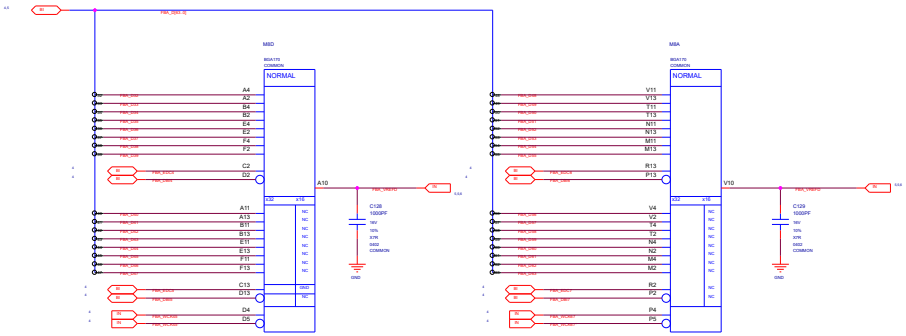
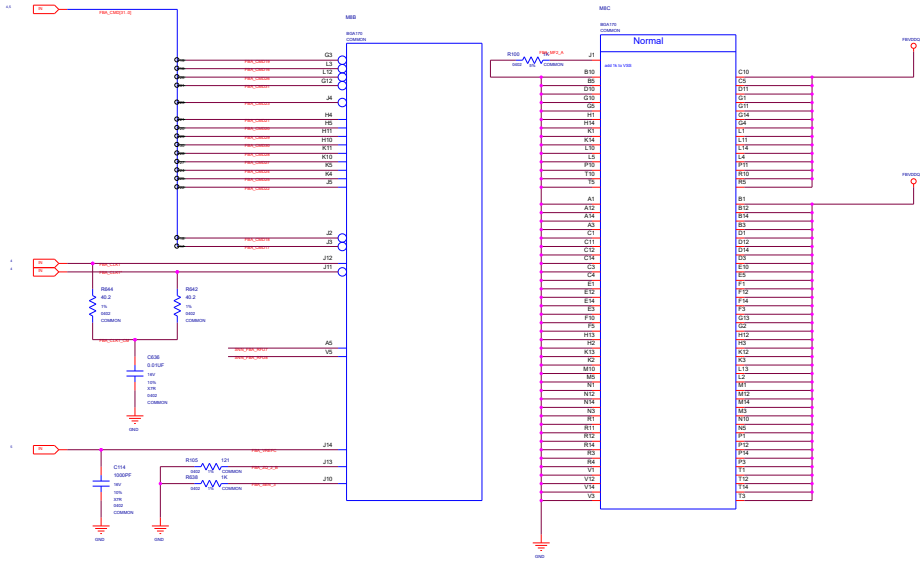
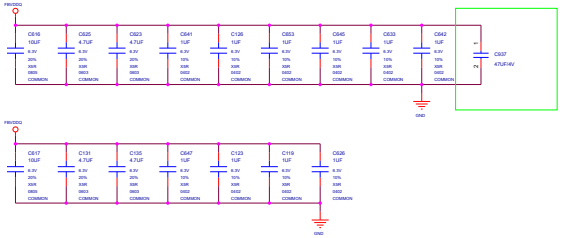
Page6: MEMORY: FBA Partition 63..32







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBA[63:32]

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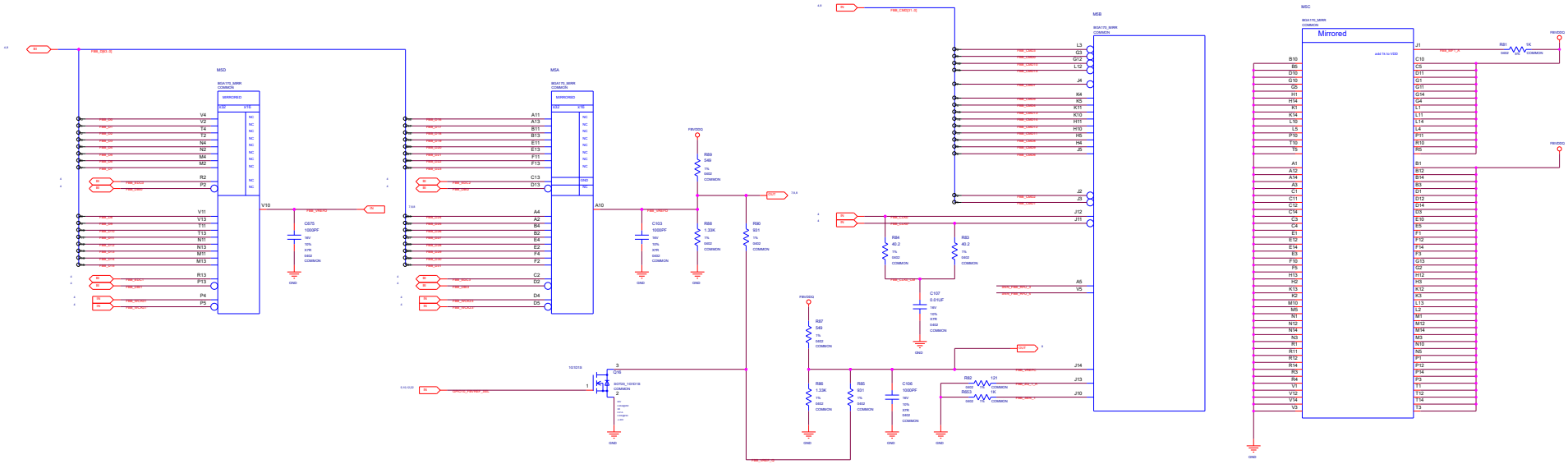
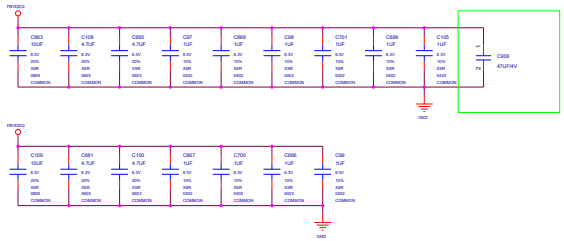
Page7: MEMORY: FBB Partition 31..0





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBB[31:0]

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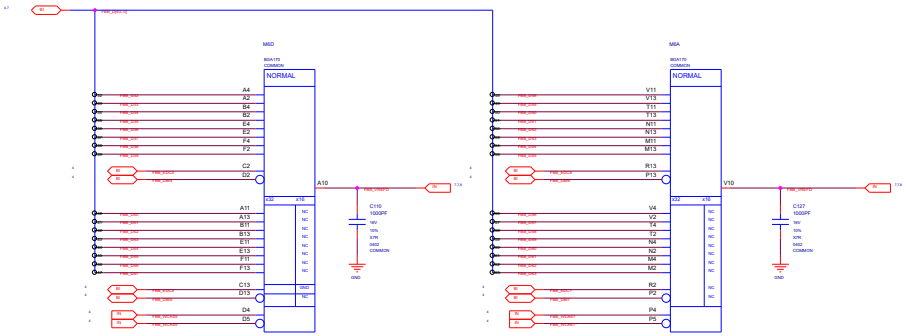
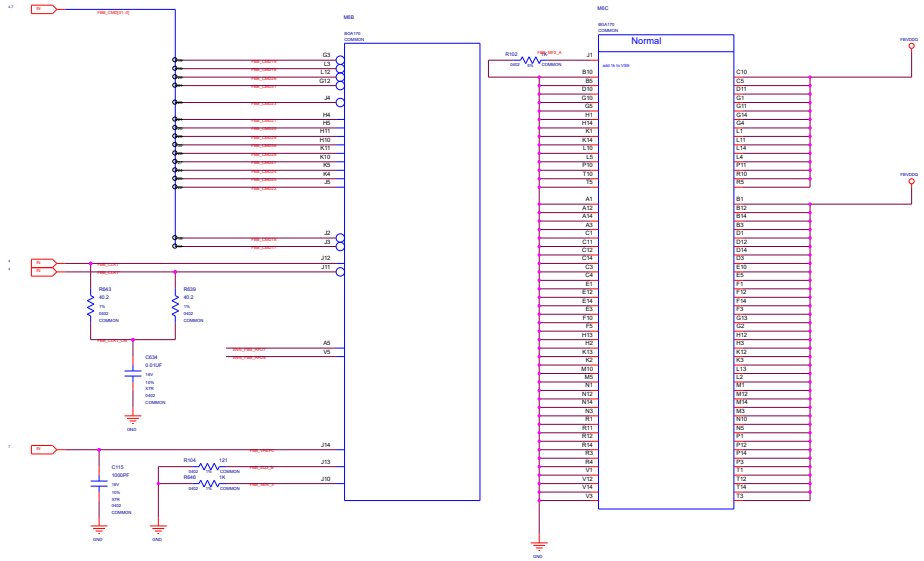
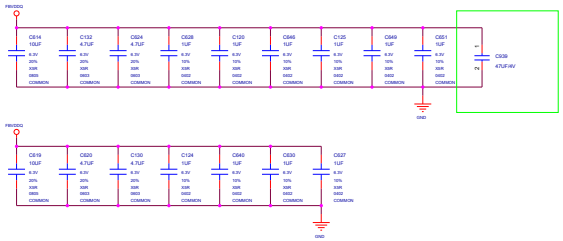
Page8: MEMORY: FBB Partition 63..32







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PAGE DETAIL	MEMORY: FBB[63:32]

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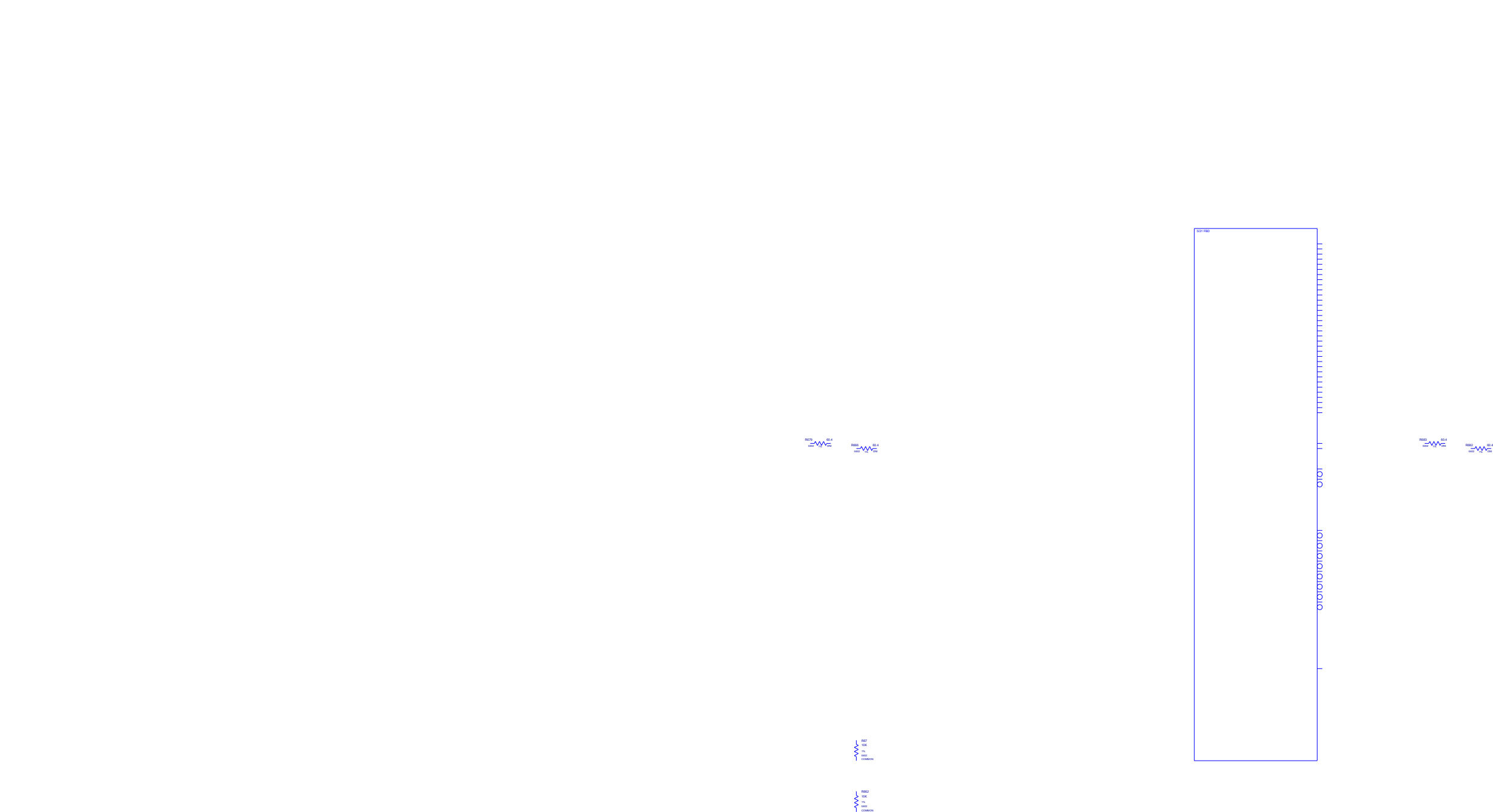
R679
60.4
0402
1%
R666
60.4
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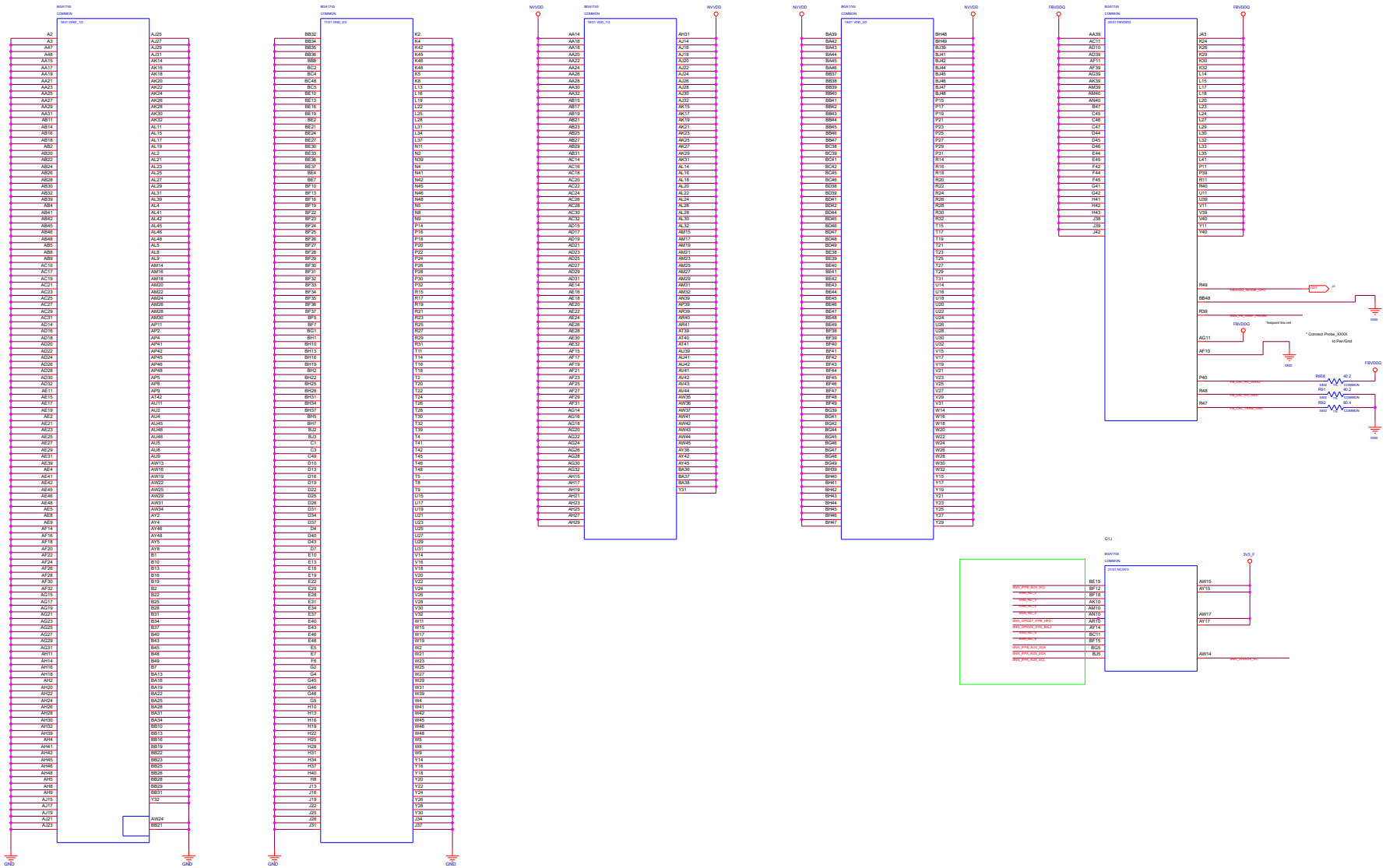
1%
R667
10K
1%
0402
COMMON
R662
10K
1%
0402
COMMON
SCH FBD
R683
60.4
0402
1%
R682
60.4
0402
1%

Page14: GPU PWR and GND



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU PWR and GND

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ASP1212-N80N-Controller-IR8318

LL set 0.6m Ohm

THERMISTOR NTC 0603 6.8K OHM

ASP1212-N80NT

+5V --> 3V3_VDDA

(150mA)

+3.328V

VRHOT TSEN1

Remote &Local sense

For MB R4E的OV電路

MB R4E Enable

P-STATE VOLTAGES

1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V

SOFT START (VR11)

1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPIO tri-state
   VID[5:1]=11000 to set 0.9125V

VID Table

GPIO7	GPIO6	GPIO5	GPIO2	GPIO17	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V