PCI-EXPRESS EDGE CONNECTOR

Koopa

Place these caps as close to the PCIE connector as possible

+12V_BUS
C157 10uF_16V
CAP CER 10UF 20% 16V X6S (0805)1.4MM H

+12V_BUS
C151 150nF_16V
C152 150nF_16V

+3.3V_BUS
C153 10uF
CAP CER 10UF 10% 6.3V X6S (0805)1.4MM MAX THICK

+3.3V_BUS
C154 100nF_6.3V
C155 1uF_6.3V
C156 10nF

p.7 GPIO_4_SMBCLK
p.7 GPIO_3_SMBDATA
+3.3V_BUS +3.3V_BUS
R105 45.3K DNI
R106 45.3K DNI
Q100 BSH111
Q101 BSH111
0R R107
0R R108
SMCLK
SMDAT
+3.3V_BUS

x16 PCIe

B1	+12V#B1	A1	PRESENCE
B2	+12V#B2	A2	+12V#A2
B3	+12V#B3	A3	+12V#A3
B4	GND#B4	A4	GND#A4
B5	SMCLK	A5	JTAG2
B6	SMDAT	A6	JTAG3
B7	GND#B7	A7	JTAG4
B8	+3.3V#B8	A8	JTAG5
B9	JTAG1	A9	+3.3V#A9
B10	3.3Vaux	A10	+3.3V#A10
B11	WAKE#	A11	PERST#
	Mechanical Key		
B12	RSVD#B12	A12	GND#A12
B13	GND#B13	A13	REFCLK+
B14	PETp0	A14	REFCLK-
B15	PETn0	A15	GND#A15
B16	GND#B16	A16	PERp0
B17	PRSNT2#B17	A17	PERn0
B18	GND#B18	A18	GND#A18
B19	PETp1	A19	RSVD#A19
B20	PETn1	A20	GND#A20
B21	GND#B21	A21	PERp1
B22	GND#B22	A22	PERn1
B23	PETp2	A23	GND#A23
B24	PETn2	A24	GND#A24
B25	GND#B25	A25	PERp2
B26	GND#B26	A26	PERn2
B27	PETp3	A27	GND#A27
B28	PETn3	A28	GND#A28
B29	GND#B29	A29	PERp3
B30	RSVD#B30	A30	PERn3
B31	PRSNT2#B31	A31	GND#A31
B32	GND#B32	A32	RSVD#A32
B33	PETp4	A33	RSVD#A33
B34	PETn4	A34	GND#A34
B35	GND#B35	A35	PERp4
B36	GND#B36	A36	PERn4
B37	PETp5	A37	GND#A37
B38	PETn5	A38	GND#A38
B39	GND#B39	A39	PERp5
B40	GND#B40	A40	PERn5
B41	PETp6	A41	GND#A41
B42	PETn6	A42	GND#A42
B43	GND#B43	A43	PERp6
B44	GND#B44	A44	PERn6
B45	PETp7	A45	GND#A45
B46	PETn7	A46	GND#A46
B47	GND#B47	A47	PERp7
B48	PRSNT2#B48	A48	PERn7
B49	GND#B49	A49	GND#A49
B50	PETp8	A50	RSVD#A50
B51	PETn8	A51	GND#A51
B52	GND#B52	A52	PERp8
B53	GND#B53	A53	PERn8
B54	PETp9	A54	GND#A54
B55	PETn9	A55	GND#A55
B56	GND#B56	A56	PERp9
B57	GND#B57	A57	PERn9
B58	PETp10	A58	GND#A58
B59	PETn10	A59	GND#A59
B60	GND#B60	A60	PERp10
B61	GND#B61	A61	PERn10
B62	PETp11	A62	GND#A62
B63	PETn11	A63	GND#A63
B64	GND#B64	A64	PERp11
B65	GND#B65	A65	PERn11
B66	PETp12	A66	GND#A66
B67	PETn12	A67	GND#A67
B68	GND#B68	A68	PERp12
B69	GND#B69	A69	PERn12
B70	PETp13	A70	GND#A70
B71	PETn13	A71	GND#A71
B72	GND#B72	A72	PERp13
B73	GND#B73	A73	PERn13
B74	PETp14	A74	GND#A74
B75	PETn14	A75	GND#A75
B76	GND#B76	A76	PERp14
B77	GND#B77	A77	PERn14
B78	PETp15	A78	GND#A78
B79	PETn15	A79	GND#A79
B80	GND#B80	A80	PERp15
B81	PRSNT2#B81	A81	PERn15
B82	RSVD#B82	A82	GND#A82

MPCIE1

p.2 PETp0_GFXRp0 / p.2 PETn0_GFXRn0
p.2 PETp1_GFXRp1 / p.2 PETn1_GFXRn1
p.2 PETp2_GFXRp2 / p.2 PETn2_GFXRn2
p.2 PETp3_GFXRp3 / p.2 PETn3_GFXRn3
p.2 PETp4_GFXRp4 / p.2 PETn4_GFXRn4
p.2 PETp5_GFXRp5 / p.2 PETn5_GFXRn5
p.2 PETp6_GFXRp6 / p.2 PETn6_GFXRn6
p.2 PETp7_GFXRp7 / p.2 PETn7_GFXRn7
p.2 PETp8_GFXRp8 / p.2 PETn8_GFXRn8
p.2 PETp9_GFXRp9 / p.2 PETn9_GFXRn9
p.2 PETp10_GFXRp10 / p.2 PETn10_GFXRn10
p.2 PETp11_GFXRp11 / p.2 PETn11_GFXRn11
p.2 PETp12_GFXRp12 / p.2 PETn12_GFXRn12
p.2 PETp13_GFXRp13 / p.2 PETn13_GFXRn13
p.2 PETp14_GFXRp14 / p.2 PETn14_GFXRn14
p.2 PETp15_GFXRp15 / p.2 PETn15_GFXRn15
PRESENCE

System JTAG TDI and TDO are hard wired. see p. 21 for GPU JTAG connection
JTDIO_LOOP

PERST#
p.19 1V_LDO_POK
R103 0R

PCIE_REFCLKP p.2
PCIE_REFCLKN p.2
PERp0 / PERn0 p.2
PERp1 / PERn1 p.2
PERp2 / PERn2 p.2
PERp3 / PERn3 p.2
PERp4 / PERn4 p.2
PERp5 / PERn5 p.2
PERp6 / PERn6 p.2
PERp7 / PERn7 p.2
PERp8 / PERn8 p.2
PERp9 / PERn9 p.2
PERp10 / PERn10 p.2
PERp11 / PERn11 p.2
PERp12 / PERn12 p.2
PERp13 / PERn13 p.2
PERp14 / PERn14 p.2
PERp15 / PERn15 p.2

PCIe RESET Buffered

+3.3V_BUS +3.3V_BUS
R102 10K
C158 100nF_6.3V
NC7SZ08P5X_NL
U100
PERST# gated
R_RST
R104 1K DNI
Place R104 in U100
D1714 DNI BAT54S
p.19 1V_LDO_POK

PERST# buf R109 0R PERST# gated
R109 to be installed for Barts
MU101 to be installed for Cypress
+3.3V_BUS
C159 100nF_6.3V
MU101
UX5901
p.2,20 PERST# buf
PERST# buf
IN2 NC OUT2 GND VCC IN1 OUT3 OUT1
PERST# gated
TESTEN
JTAG_TRSTB
TESTEN p.21
JTAG_TRSTB p.21

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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Title PCIE EDGE CONNECTOR
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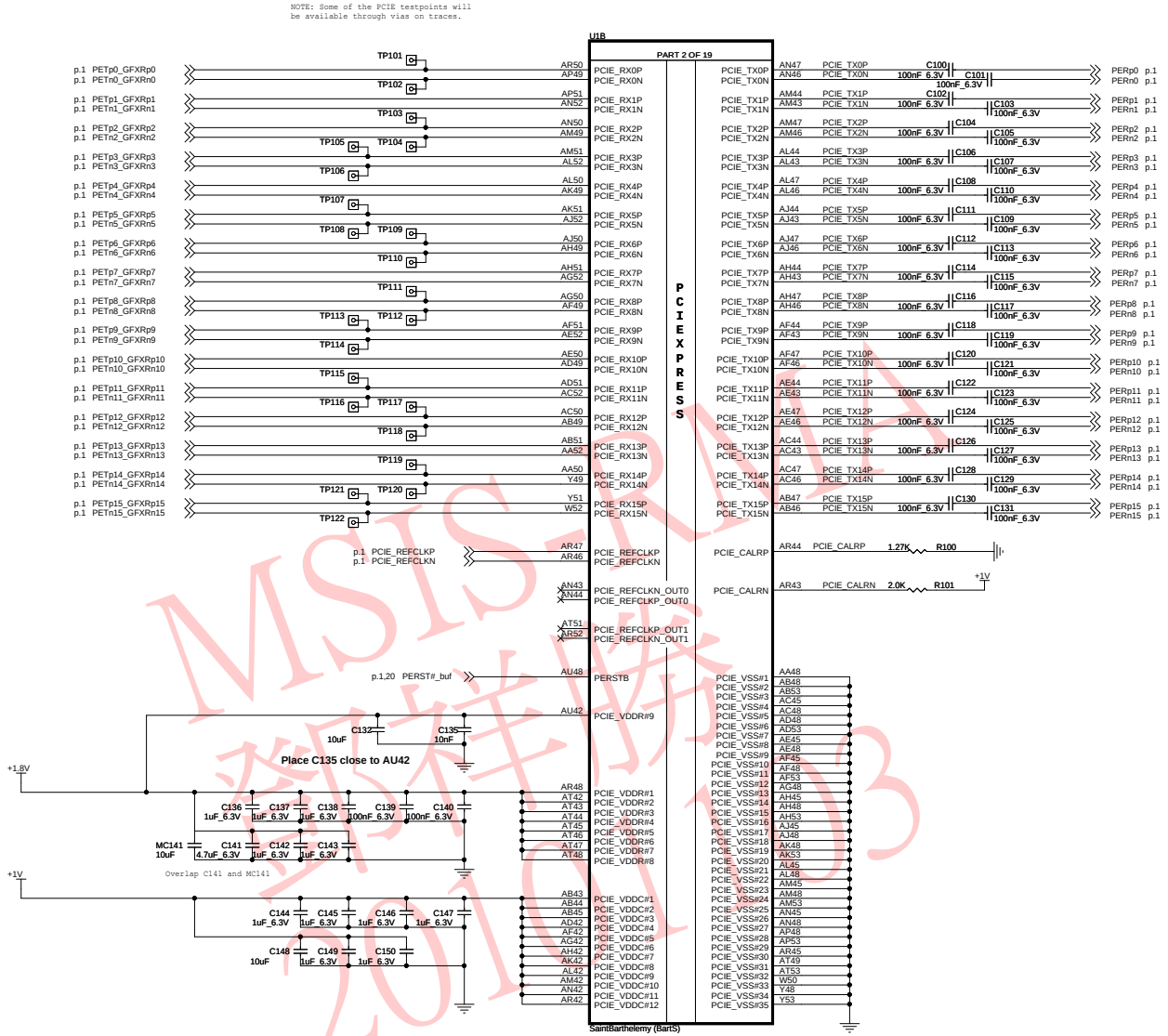
(2) BARTS PCIE Interface



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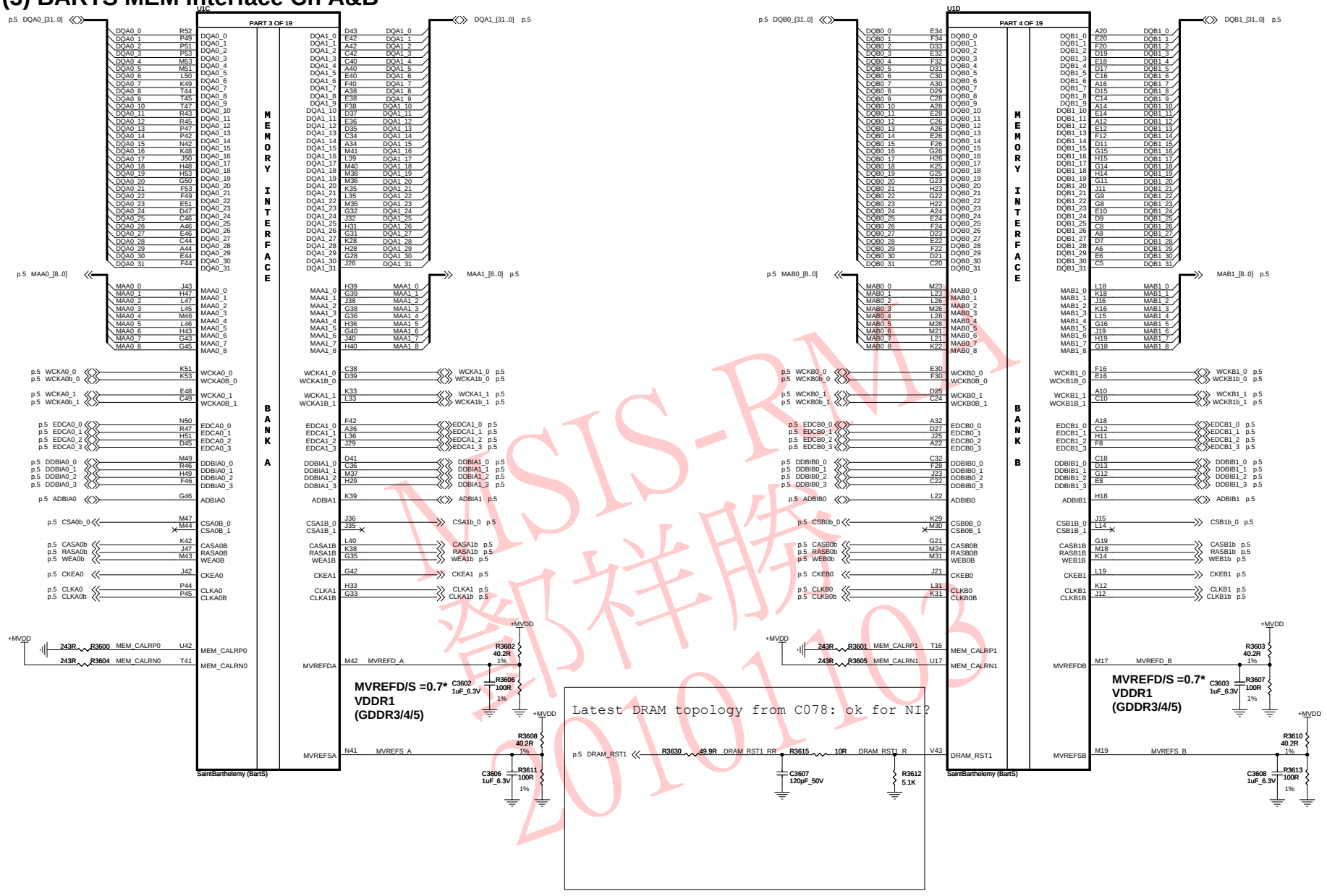
(3) BARTS MEM Interface Ch A&B



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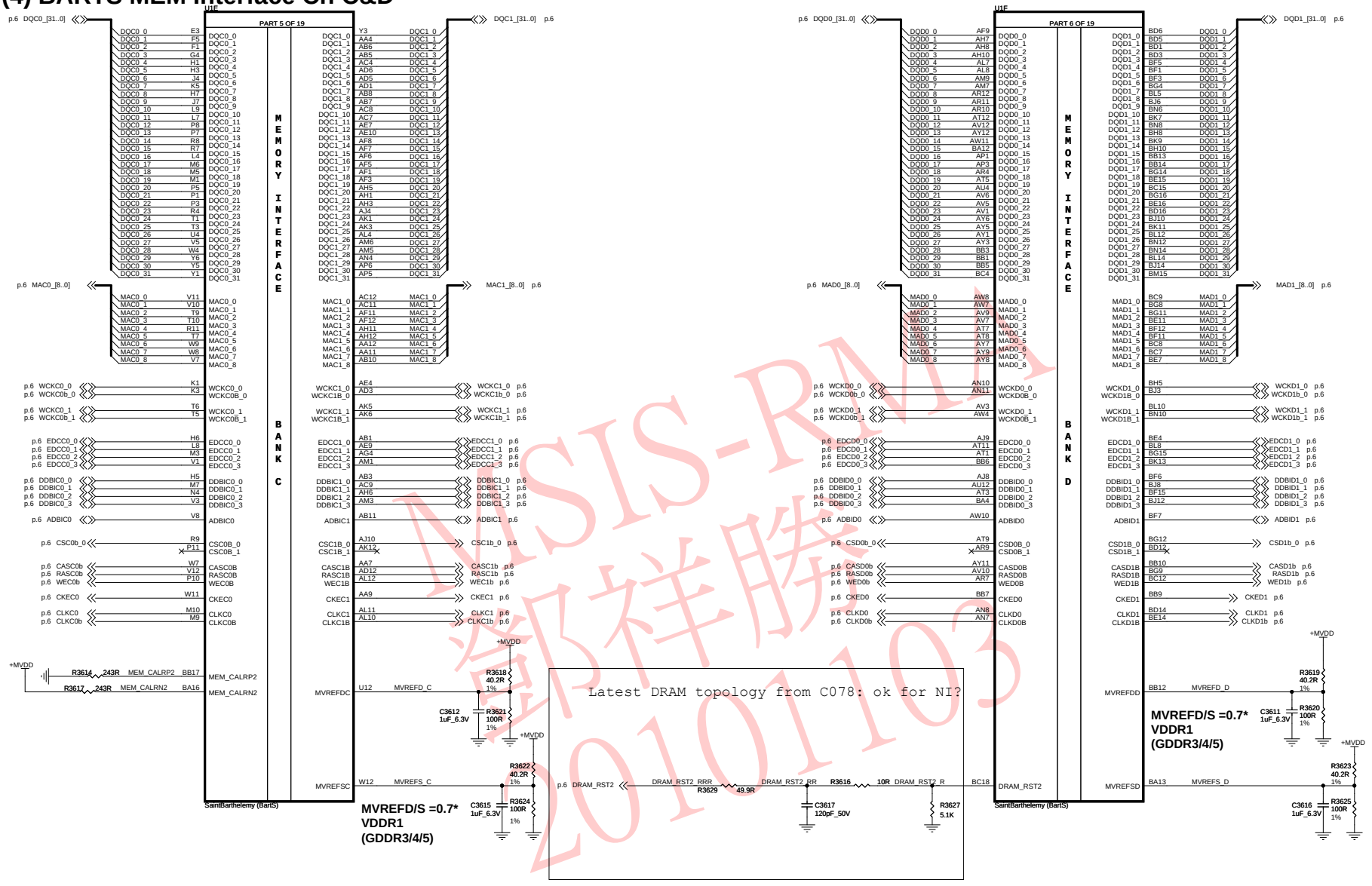
(4) BARTS MEM Interface Ch C&D



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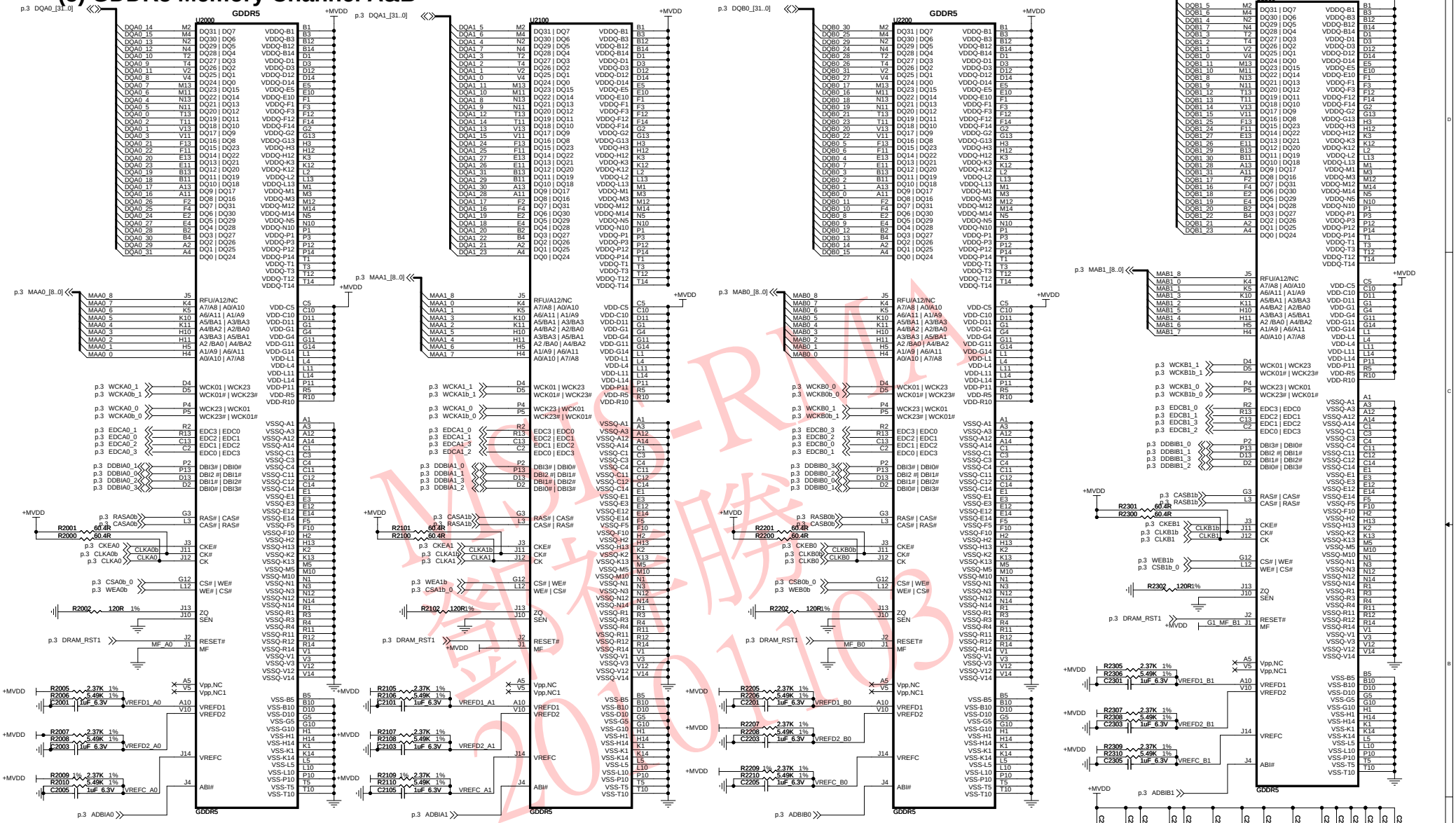
(5) GDDR5 Memory Channel A&B



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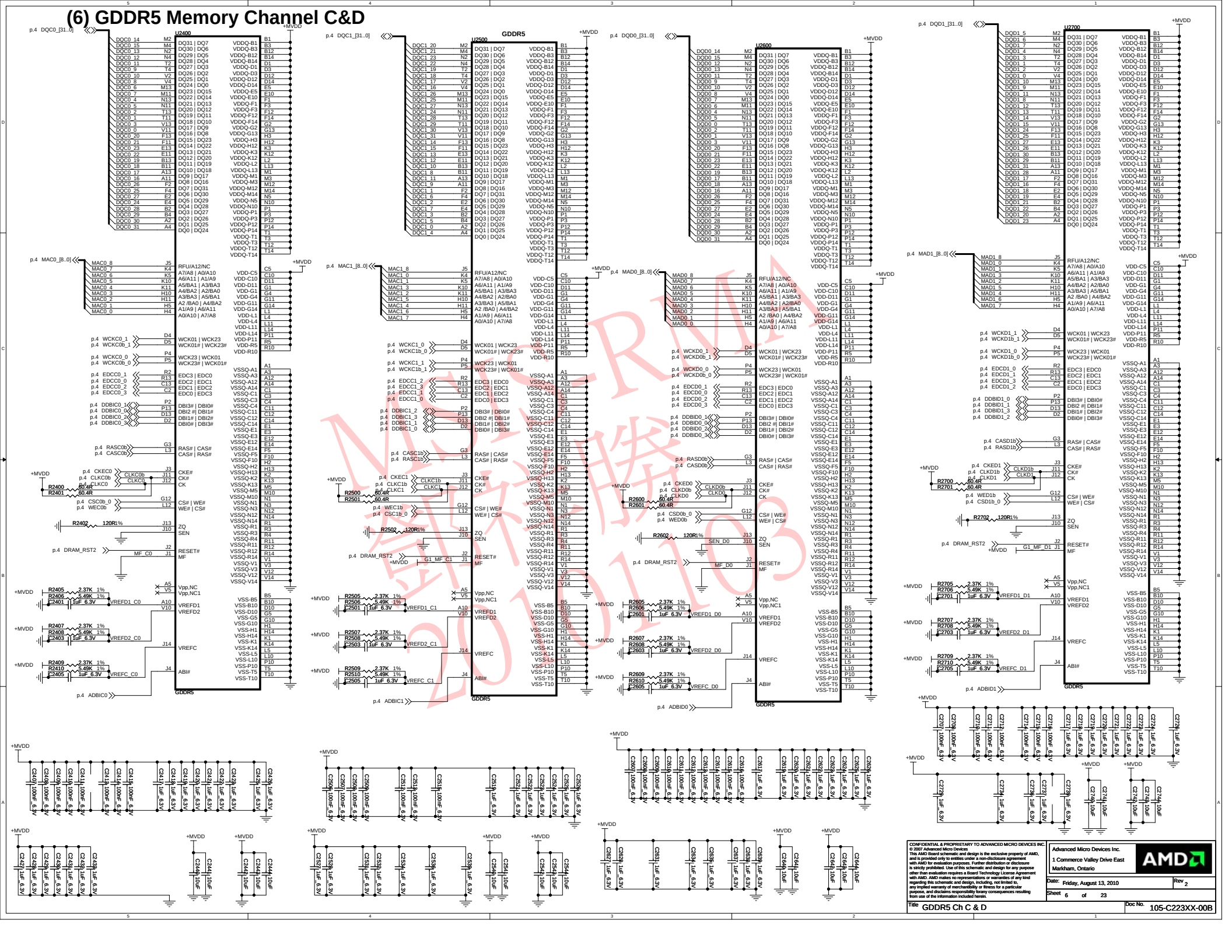
(6) GDDR5 Memory Channel C&D



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(07) BARTS GPIOs Strap CF XTAL OSC

PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

SCL / SDA BUS:

I2C Address	Function	Device
0x0A	VDDC REG	

DDC6 BUS:

I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

PWRGOOD must be connected to GND for normal operation

PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO(13,12,11) - CONFIG[2..0]

CONFIG[2]	100 - 512Kbit	M25P05A	(ST)
	101 - 1Mbit	M25P10A	(ST)
CONFIG[1]	101 - 2Mbit	M25P20	(ST)
	101 - 4Mbit	M25P40	(ST)
CONFIG[0]	101 - 8Mbit	M25P80	(ST)
	100 - 512Kbit	Pm25LV512	(Chingis)
	101 - 1Mbit	Pm25LV010	(Chingis)

VIP_DEVICE_STRAP_DIS
V2SYNC H2SYNC ?

RESERVED:
Internal use only. Other logic must not affect these signals during RESET.

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

RESERVED:
STRAP_BIOS_ROM_EN
CLKREQ# that requires open drain connection, and cannot be used as pinstrap
Don't set high at reset

Internal use only. Other logic must not affect these signals during RESET.

CrossFire Card-Edge

Lower Cable Card Edge

Place the crossfire testpoints near the ASIC and not the connector

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

Keep XIN_OSC and XOUT_OSC as short as possible to minimize stray capacitance

Overlap R26 and R19

Divider for 1.8V signaling.

Route 50ohms single-ended/100ohms diff and keep short

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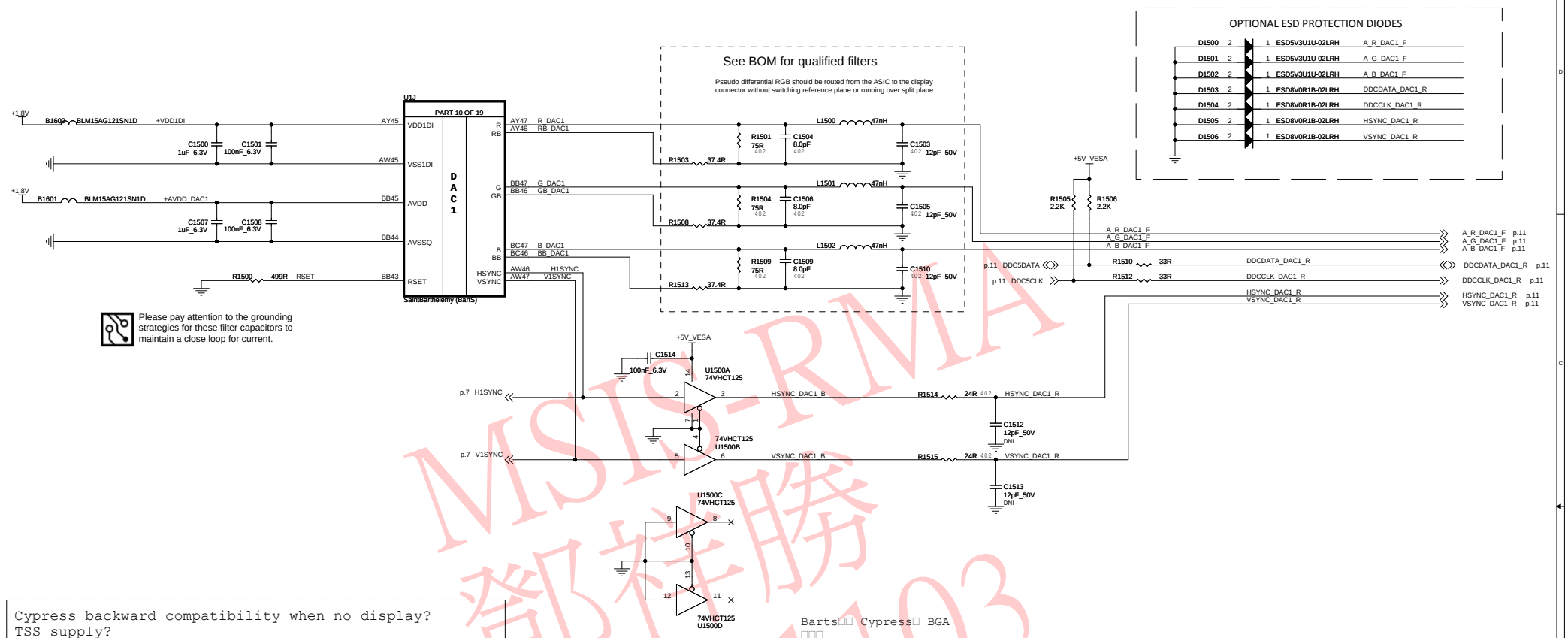
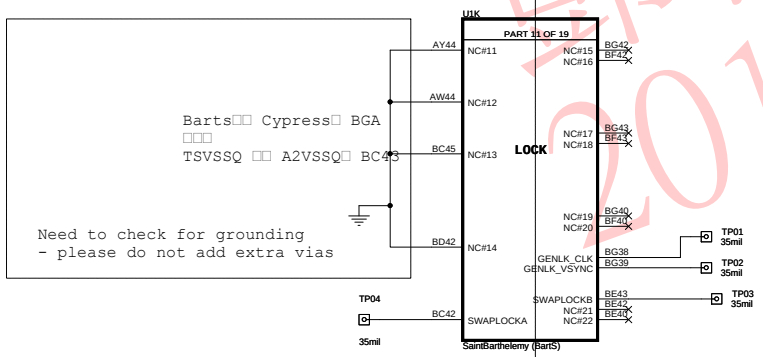
Title ASIC GPIO, STRAPS,CF, and XTAL

Doc No. 105-C223XX-00B

(08) BARTS DAC1



Cypress backward compatibility when no display?
TSS supply?



Barts□□ Cypress□ BGA
□□□
NC□□ B2□ BG40
NC□□ B2B□ BF40
NC□□ COMP□ BE40
NC□□ G2□ BG43
NC□□ G2B□ BF43
NC□□ R2□ BG42
NC□□ R2B□ BF42
SWAPLOCKA□ R2SET□ BC42
NC□□ A2VDD□ BD42
NC□□ A2VDDQ□ BC45
NC□□ VDD2DI□ AY44
NC□□ VSS2DI□ AW44
GENLK_CLK□ H2SYNC□ BG38
GENLK_VSYNC□ V2SYNC□ BG39
TSVSSQ □□ A2VSSQ□ BC43
SWAPLOCKB□ Y□ BE43
NC□□ C□ BE42
□
RSVD□□ NM_VDDC□ AM19
RSVD□□ NM_VDDCI□ AR19
RSVD□□ NM_VDDR1□ AN18
RSVD□□ NM_VSS□ AM18
RSVD□□ NM_VSS□ AN19
RSVD□□ NM_VSS□ AR18
□□□
VSS□□ VSS_MECH□ (12x)

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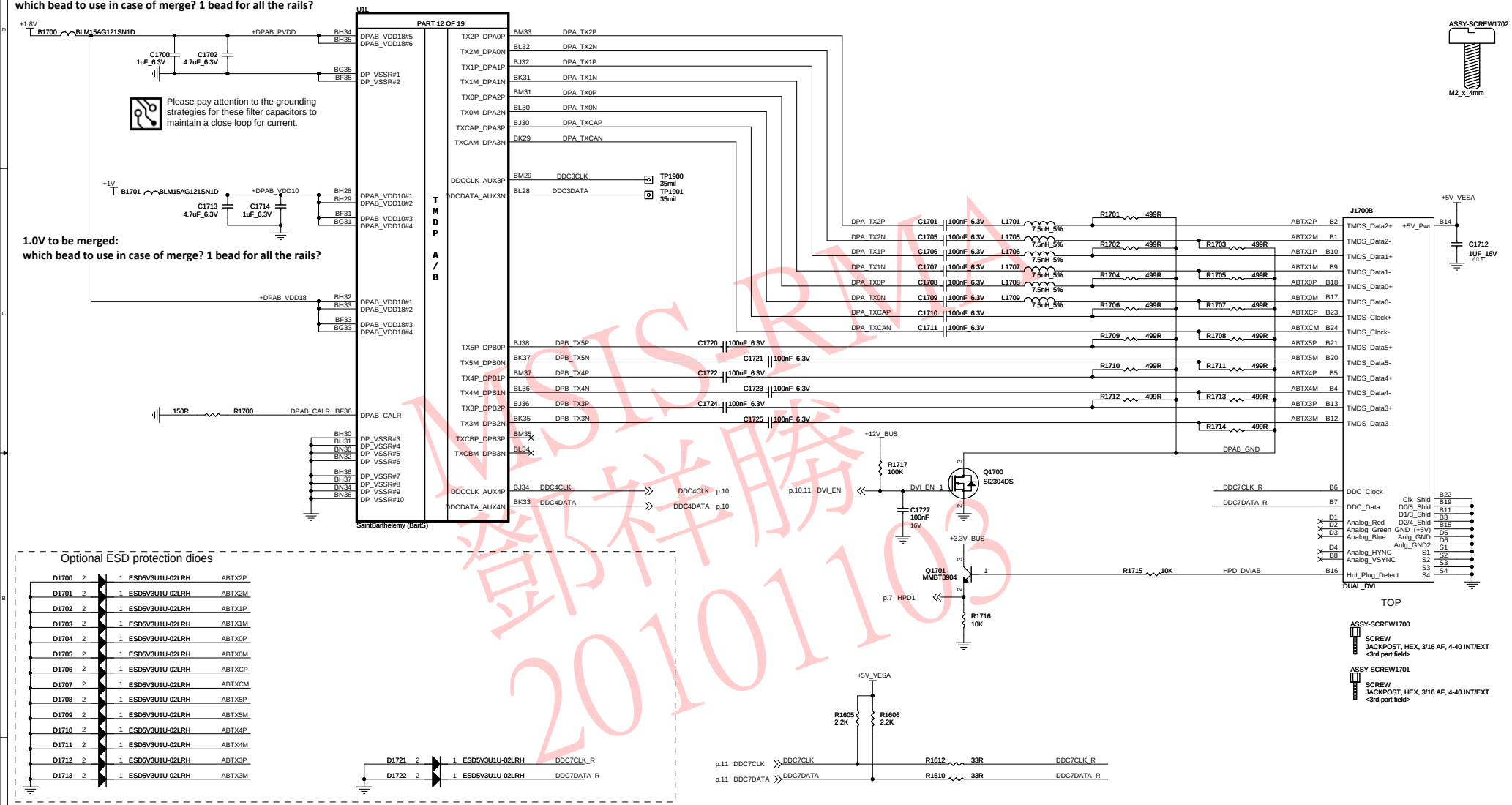
(09) BARTS TMDS A&B

1.8V to be merged:
which bead to use in case of merge? 1 bead for all the rails?

1.0V to be merged:
which bead to use in case of merge? 1 bead for all the rails?



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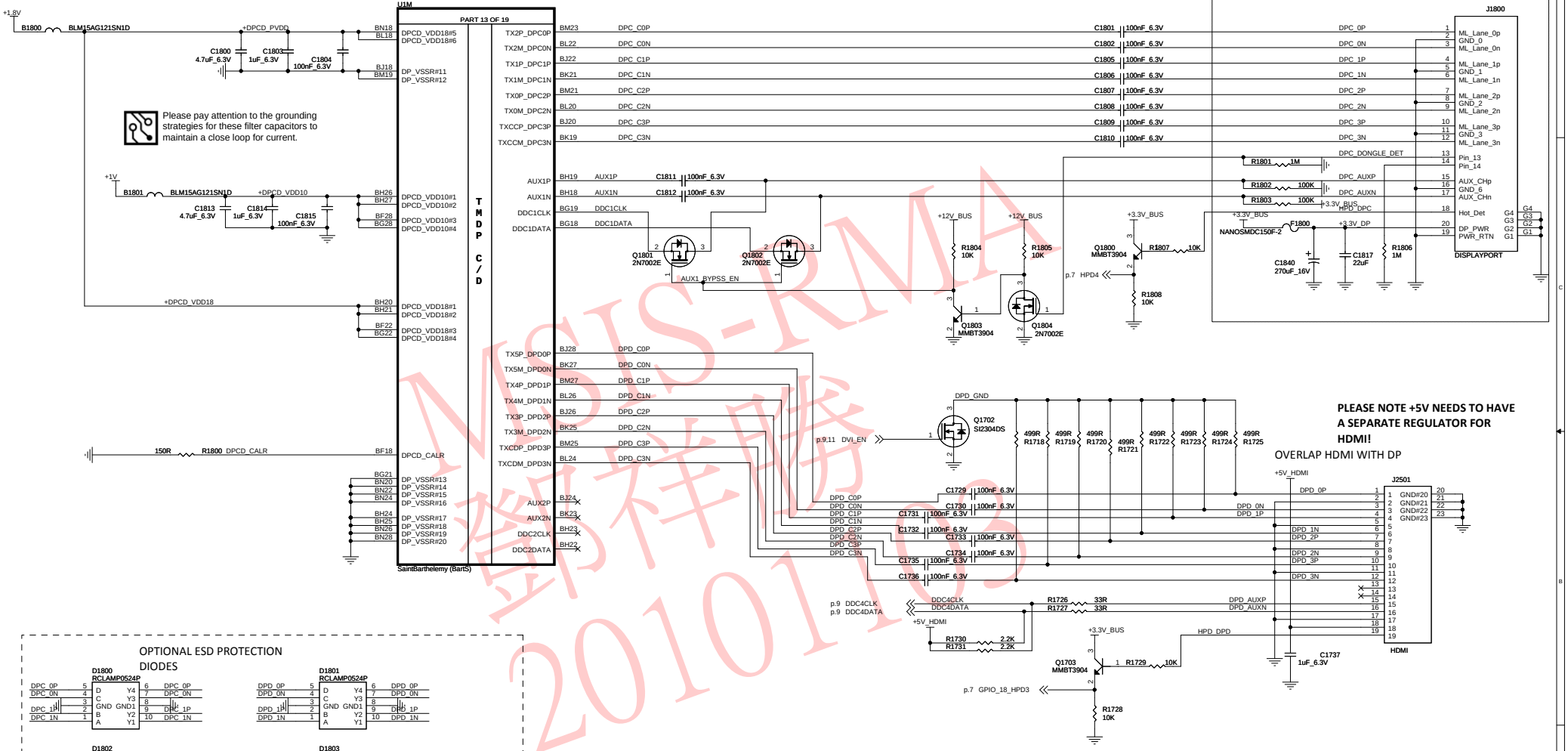
(10) BARTS Display Port/HDMI C&D



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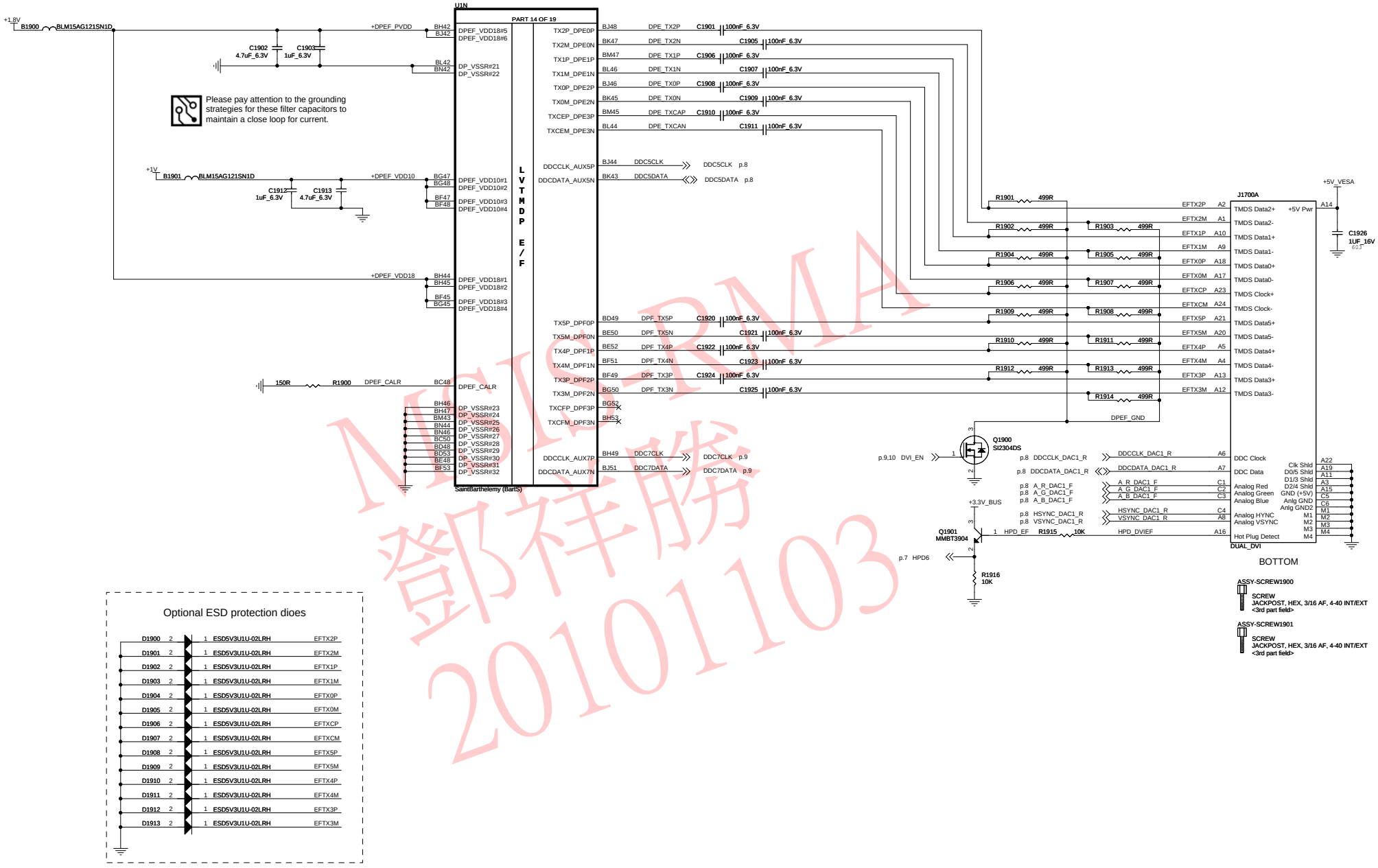
Title DP C,DP/HDMI D	Doc No. 105-C223XX-00B

(11) BARTS LVTMDP E&F



Optional ESD protection dioes

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Title TMDS EF

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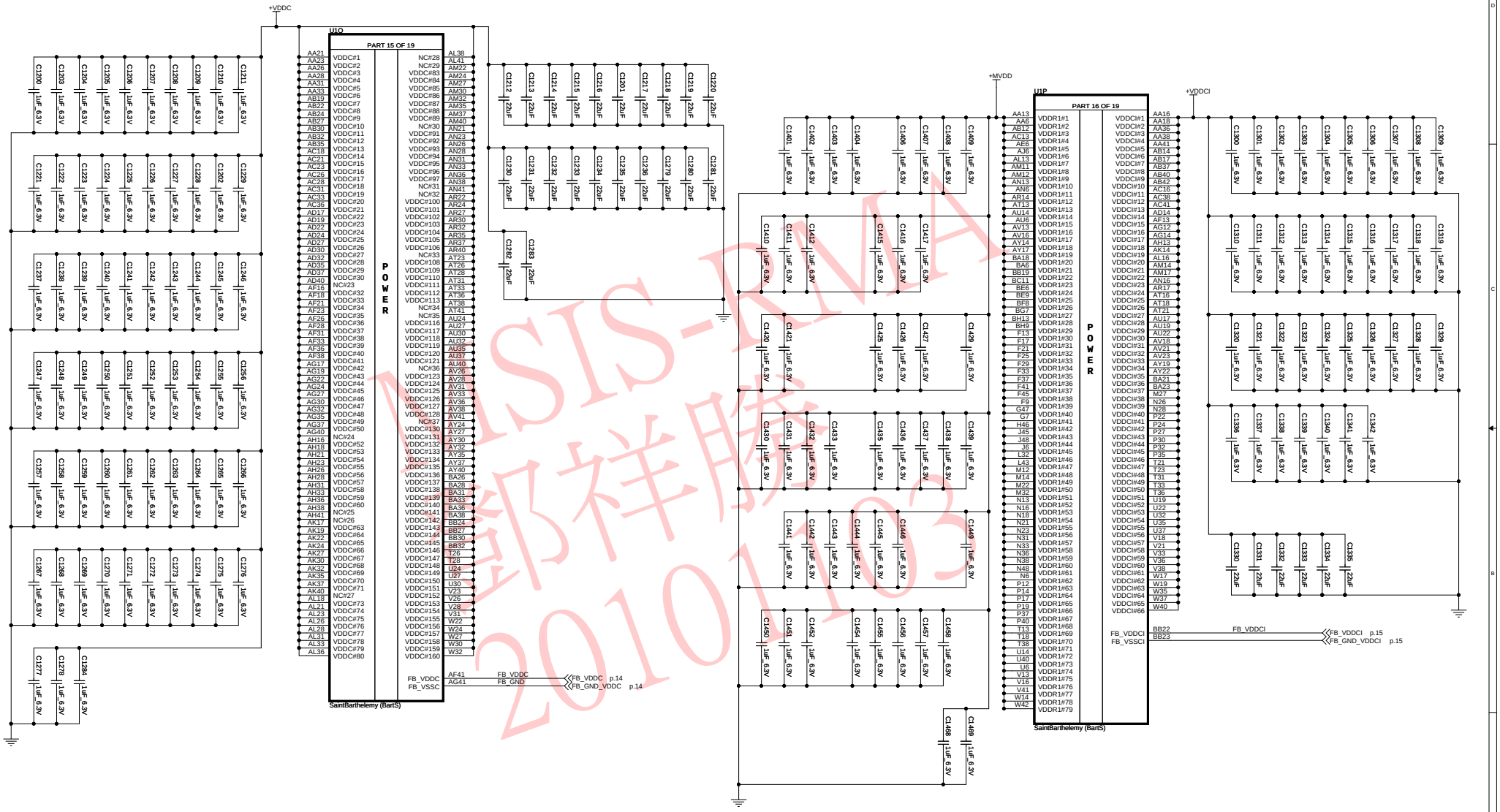
(12) BARTS Power



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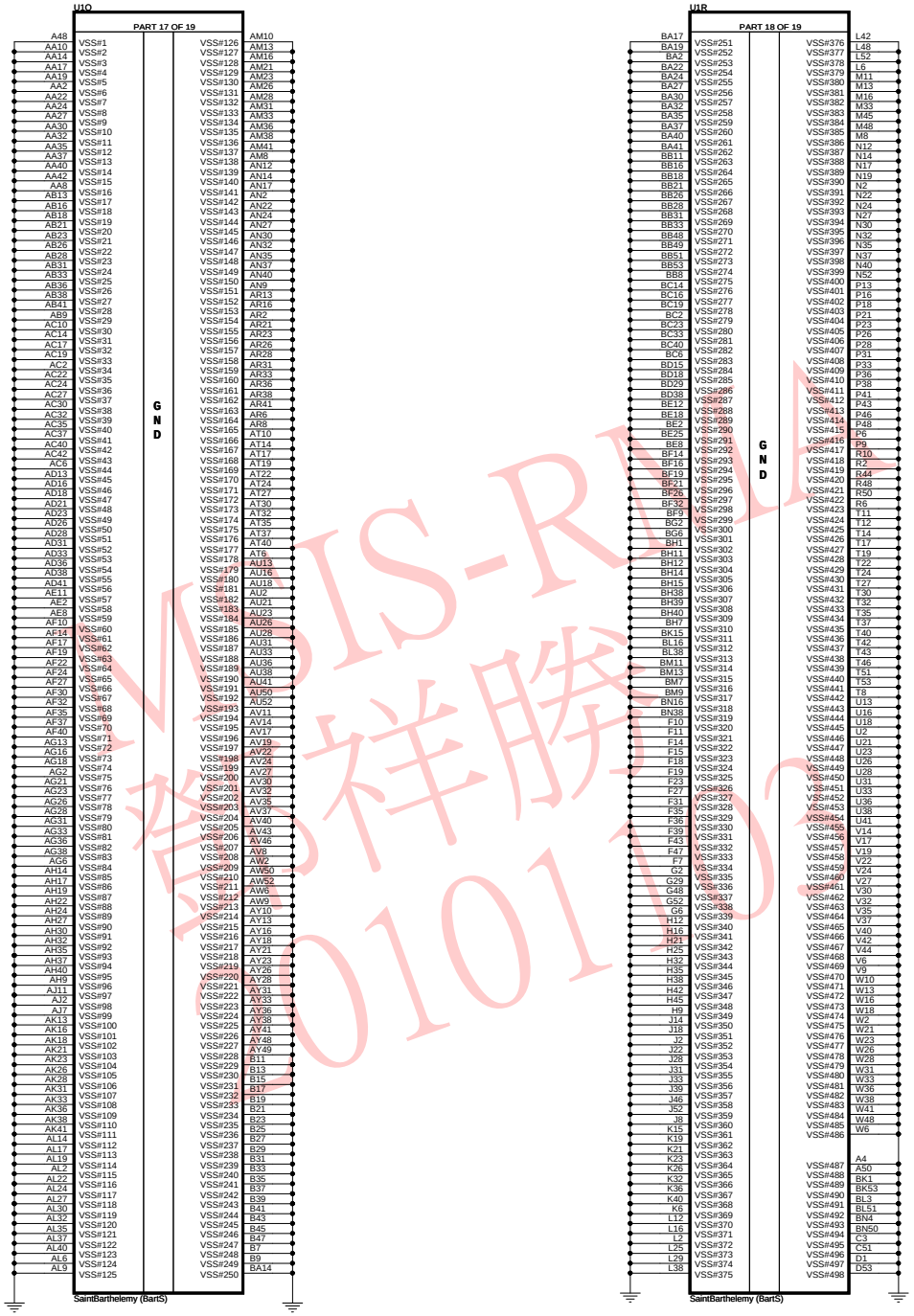
(13) BARTS GND



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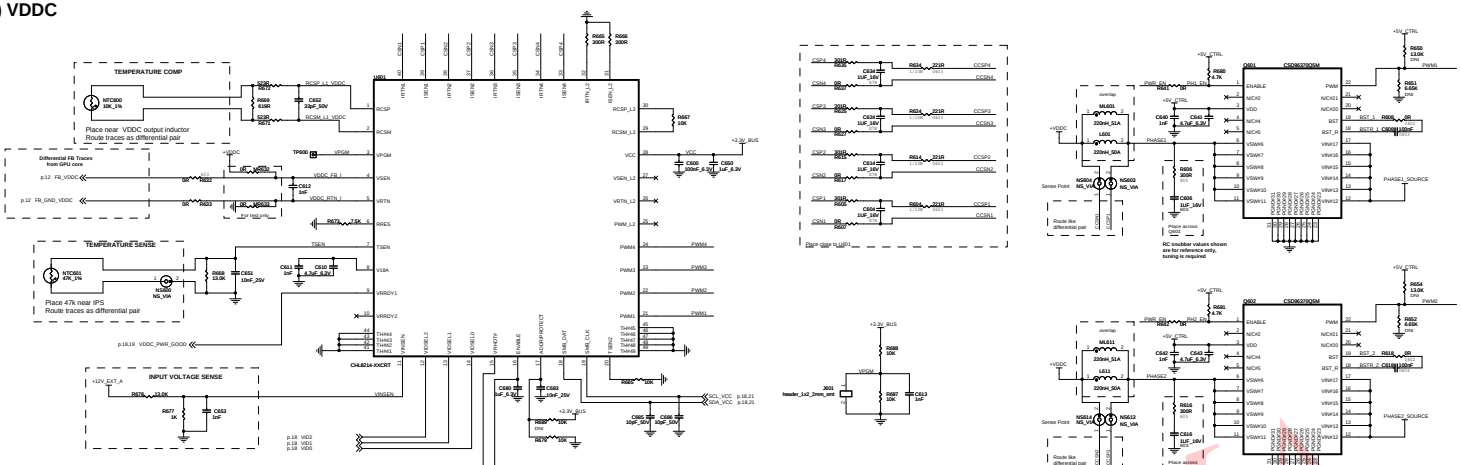
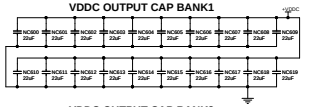
(14) VDDC

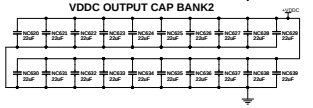


OUTPUT MLCC

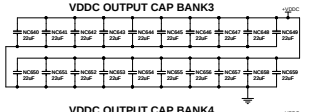
VDDC OUTPUT CAP BANK1



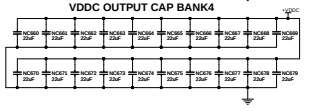
VDDC OUTPUT CAP BANK2



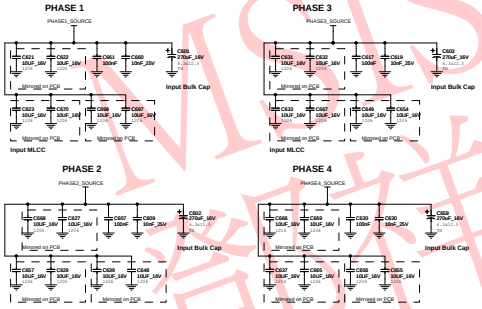
VDDC OUTPUT CAP BANK3



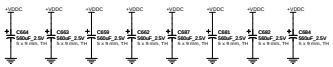
VDDC OUTPUT CAP BANK4



INPUT CAP



Output Bulk CAPs



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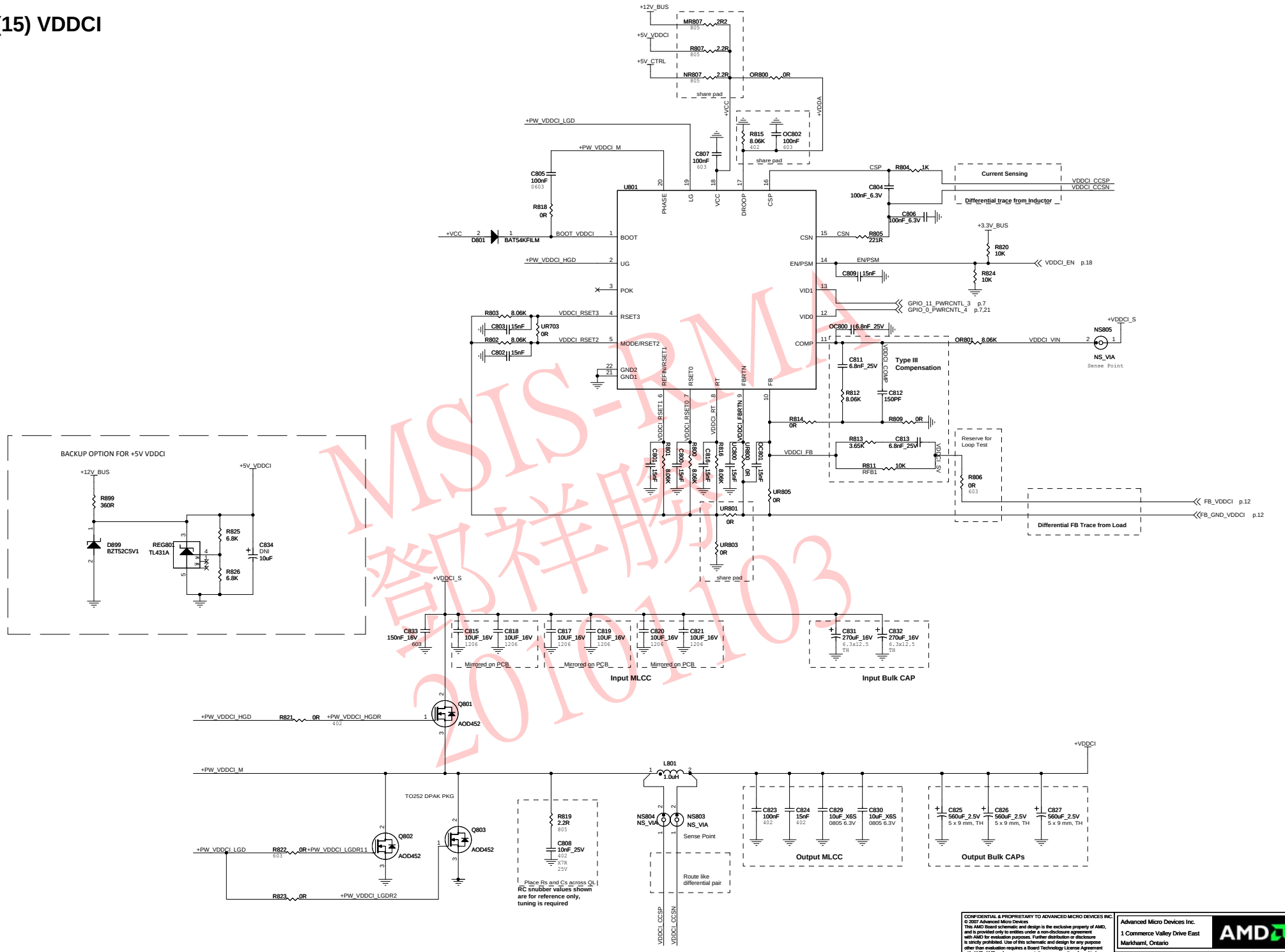
Doc No.: 105-C223XX-008

(15) VDDCI



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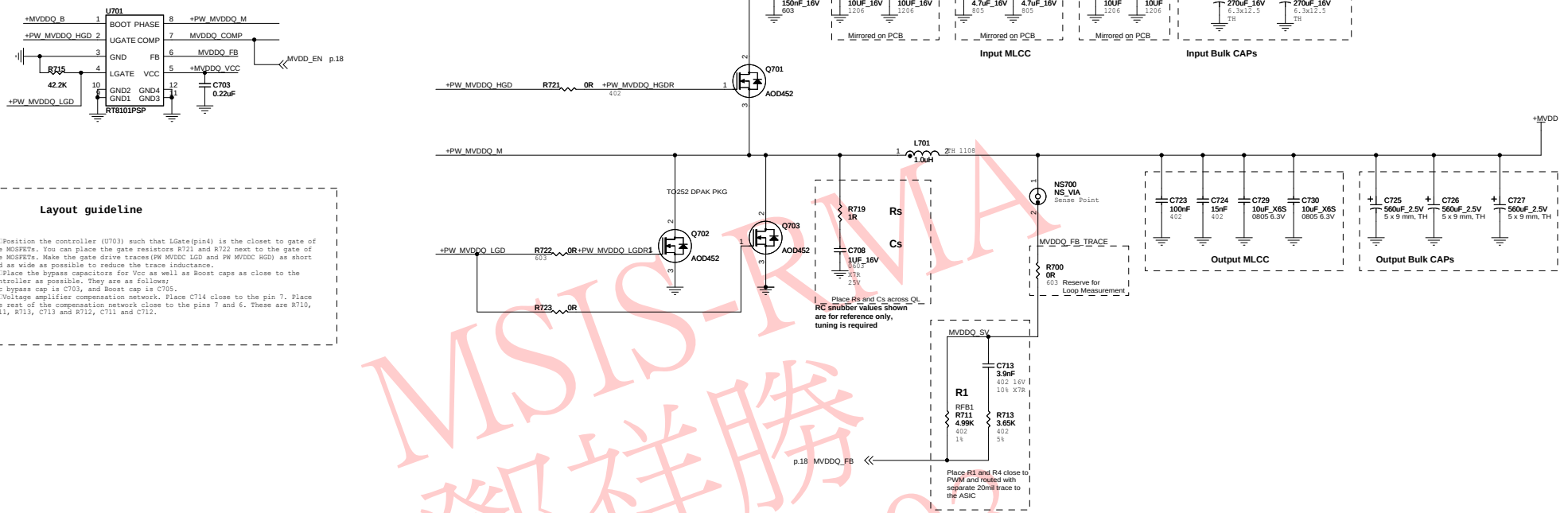
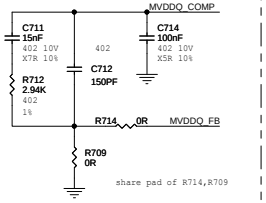
(16) MVDD



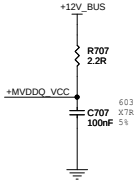
Layout guideline

1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW_MVDDC_LGD and PW_MVDDC_HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

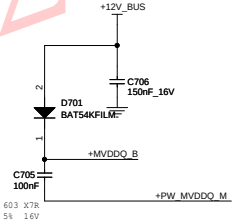
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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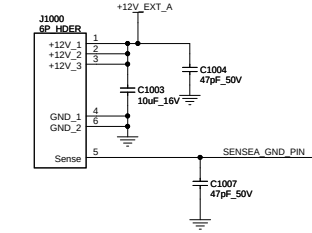
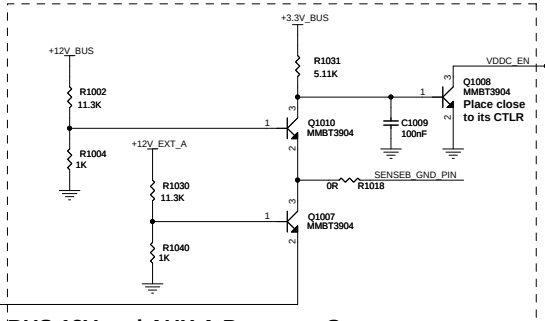
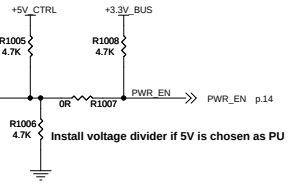
(17) BARTS POWER MGMNT

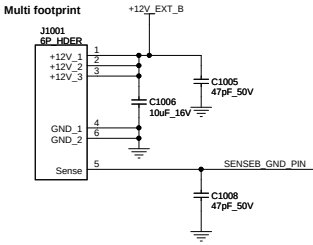


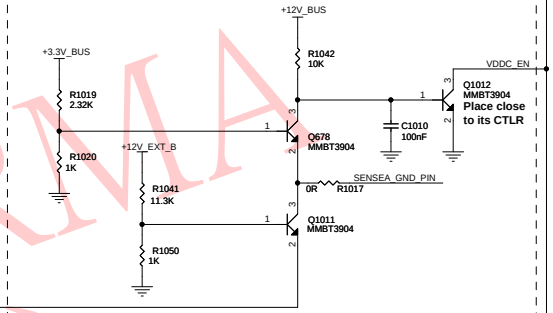


BUS 12V and AUX A Power up Seq

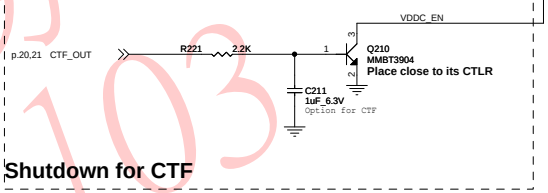


Multi footprint





BUS 3.3V and AUX B Power up Seq



Shutdown for CTF

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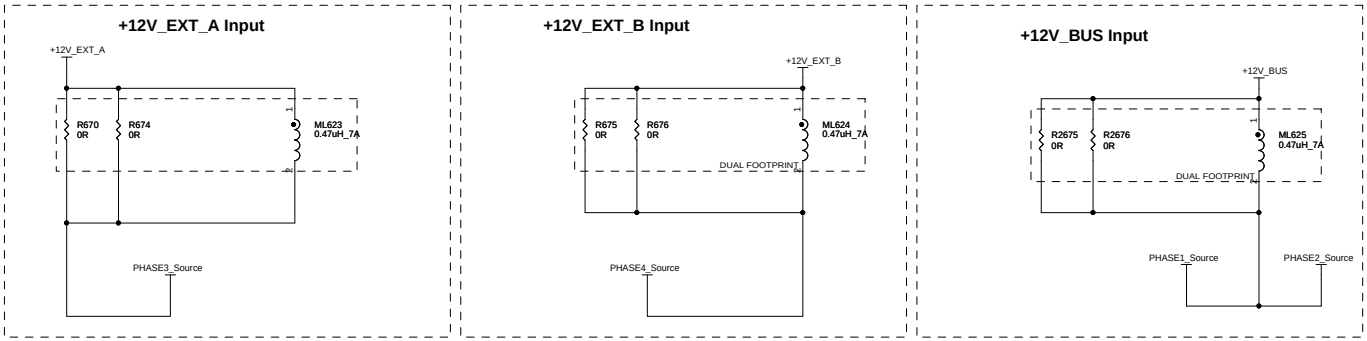
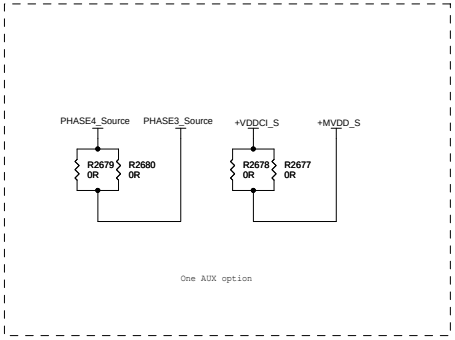
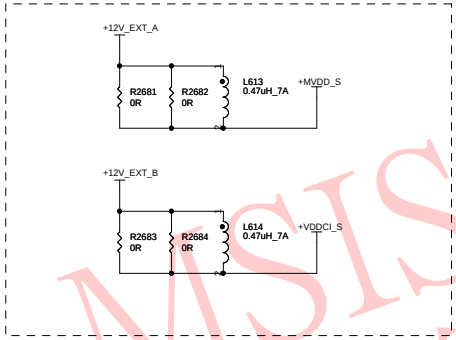
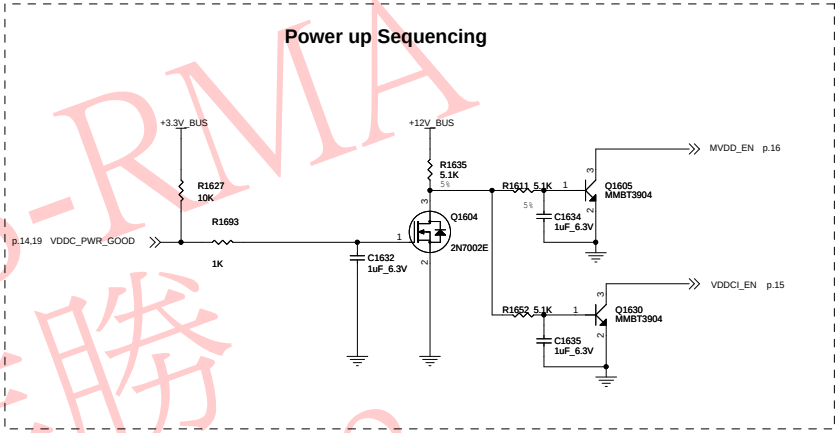
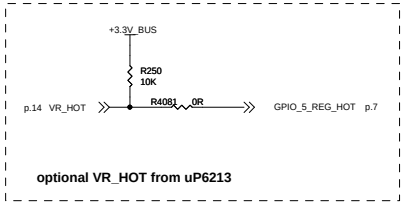
(18) BARTS VDDCI POWER PLAY

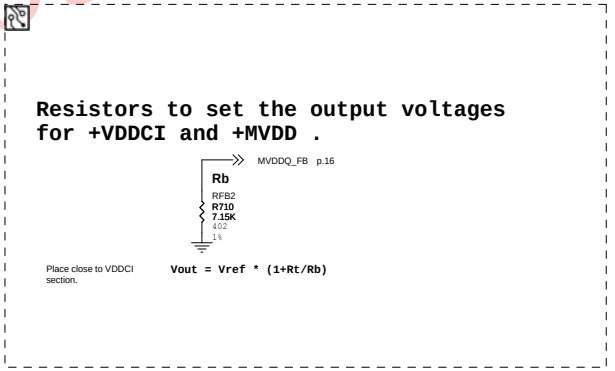


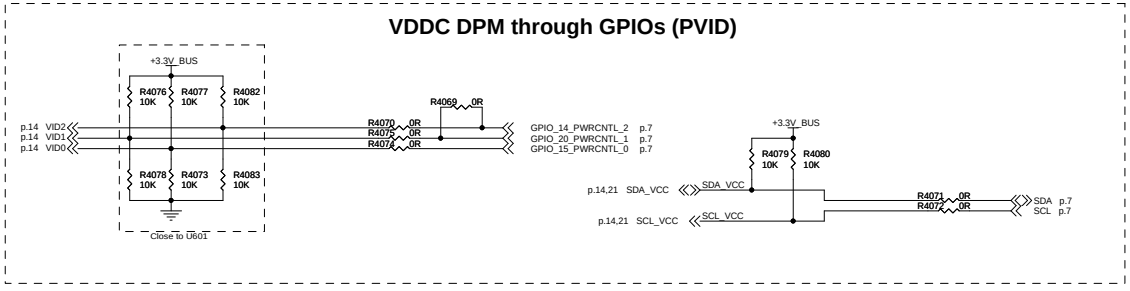












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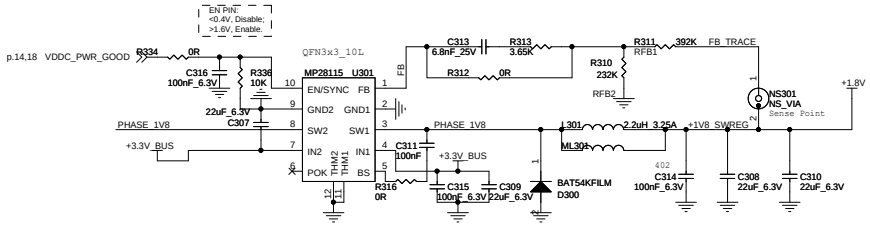
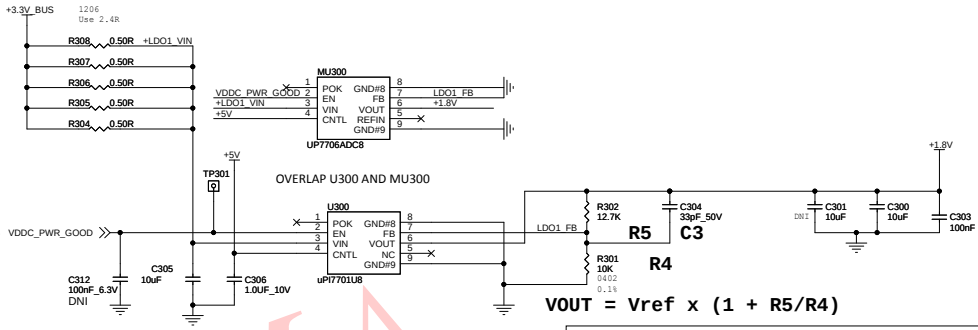
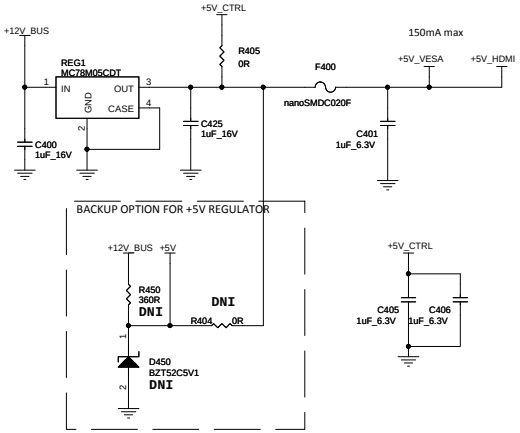
(18) BARTS Small Rail Regulators

LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

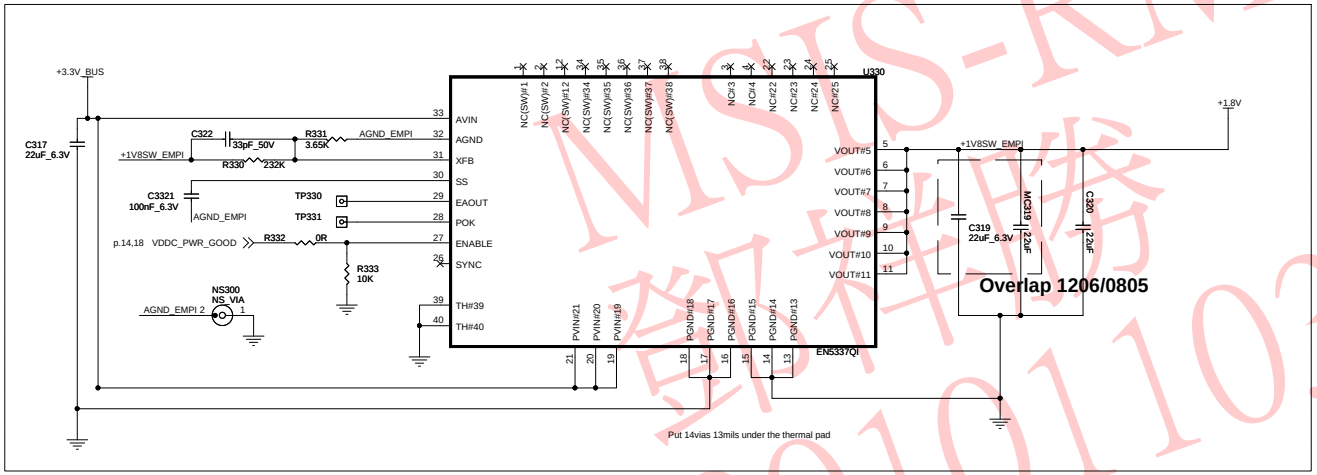




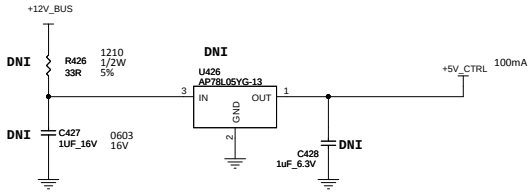
Regulators for +5V, +5V_VESA and +5V_HDMI
Iout max = 150mA (DVI+HDMI)



Other cheaper solution at 5MHz switching for 1.8V

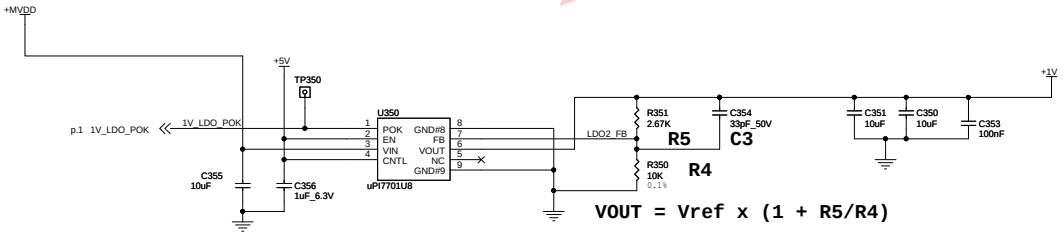


optional 5V power for VDDC regulator;



LDO #2: Vin = +1.35V to 1.8VMAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

OVERLAP ALTERNATE CAP FOOTPRINTS



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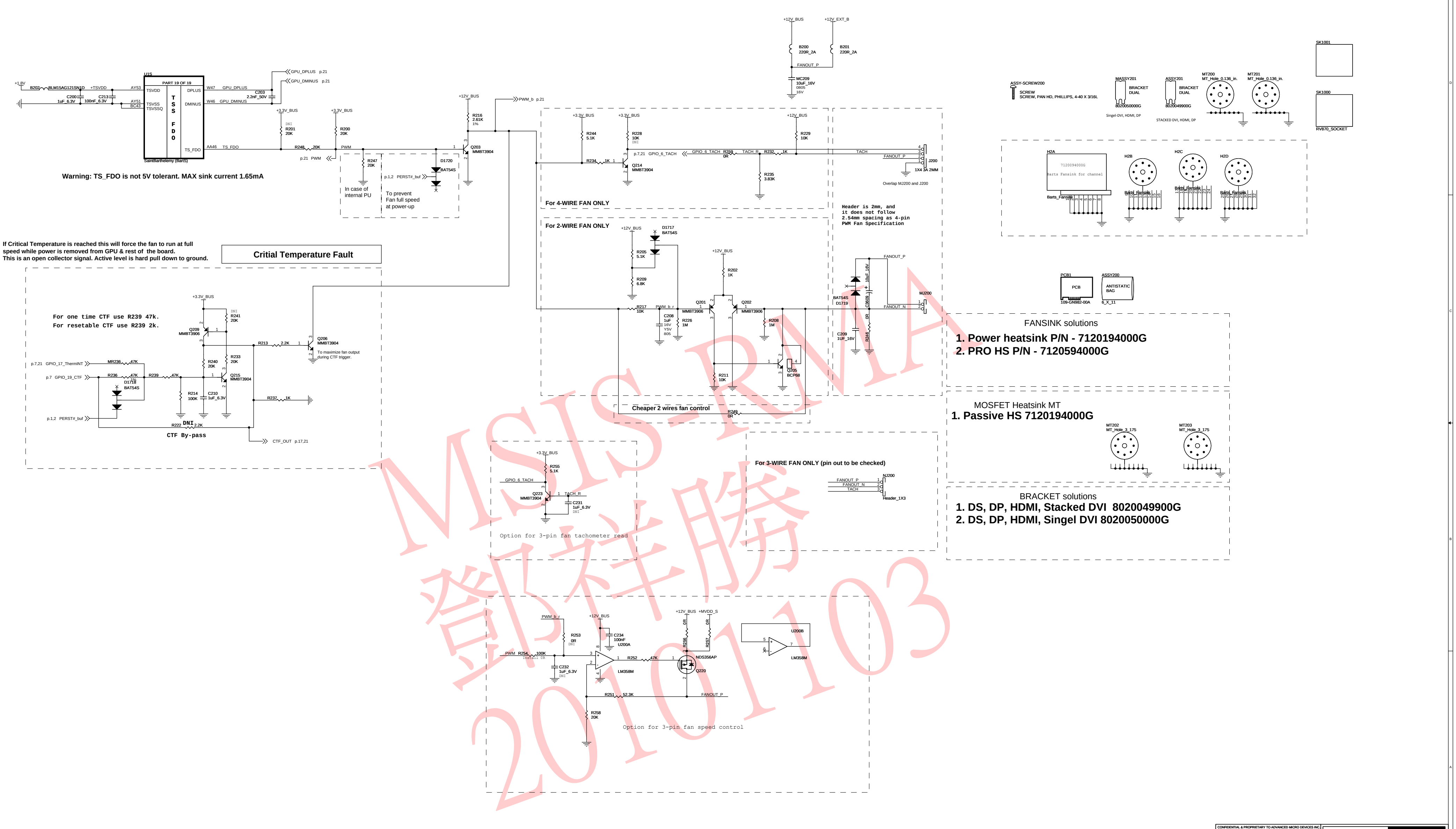
(20) BARTS Mechanical and Thermal Management



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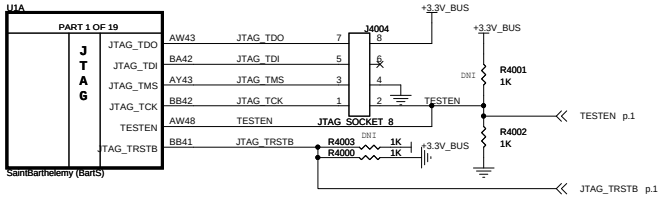
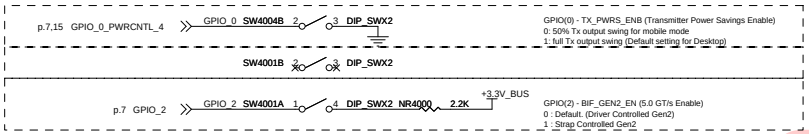
(21) BARTS Debug Circuits

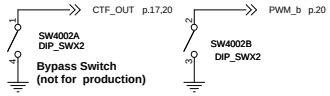
JTAG



For ALL bringup boards DNI R4000 and stuff R4003 otherwise the TAPC will be struck in Test-Logic-Reset and be useless since TRSTB is not on the connector.

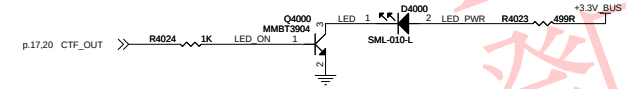
SWITCH CONNECTIONS TO PINSTRAPS



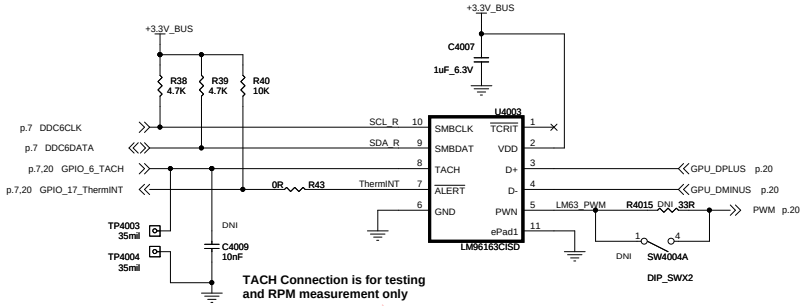


DNI For Production

LED RED "ON" shows Fault



LM96163 FOR BACKUP THERMAL CONTROL



TACH Connection is for testing and RPM measurement only

To ACCESS the VDDC CONTROLLER through I2C

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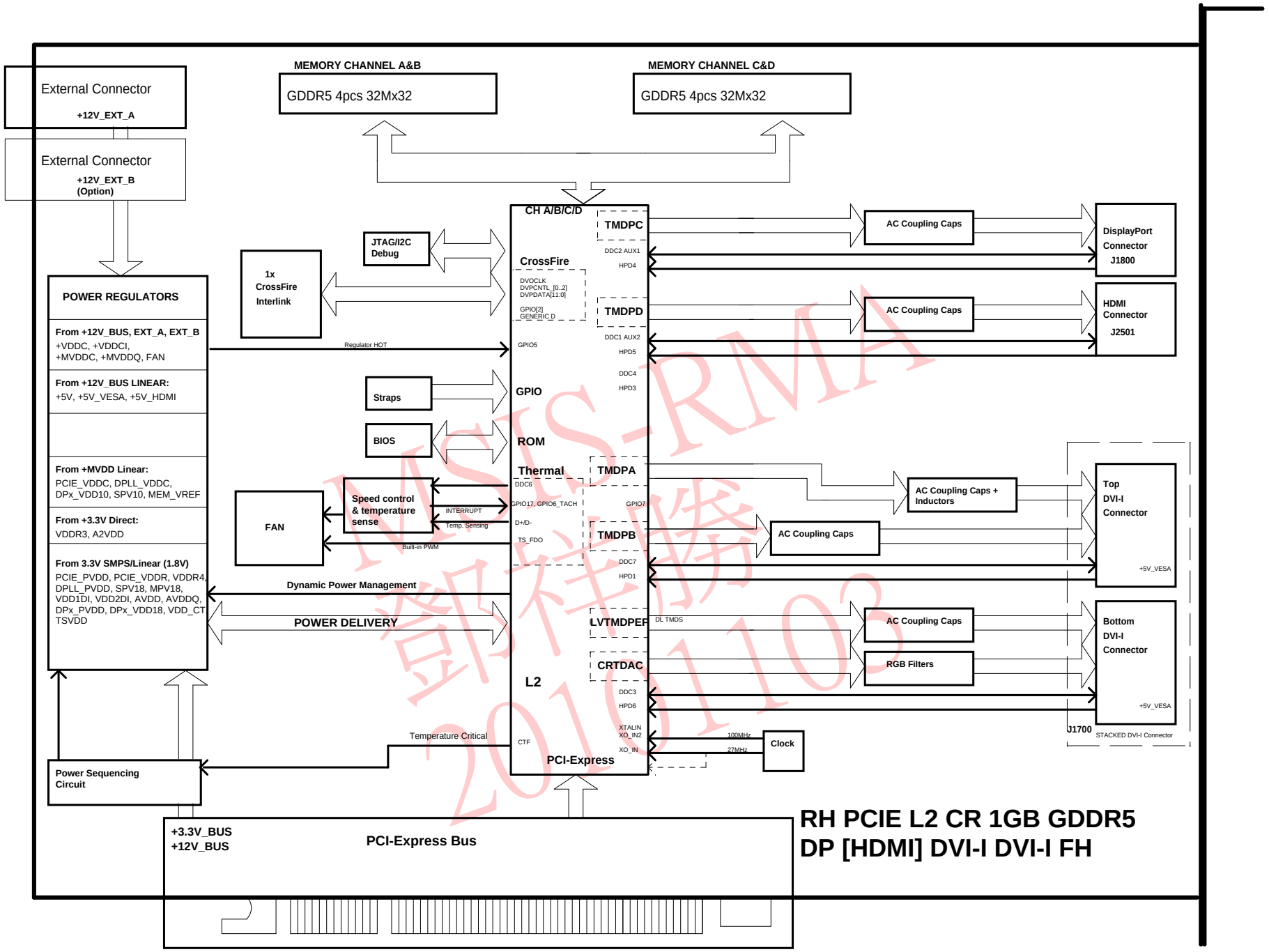

RH PCIE L2 CR 1GB GDDR5
DP [HDMI] DVI-I DVI-I FH

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RH BARTS GDDR5 DP-HDMI-DVII-DVII	105-C223XX-00B	Friday, August 13, 2010

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	21/06/2010	Initial release. Based on C221 layout
1	00B		Page17: add C221 Page14: update Q601,Q602,Q603,Q604 symbol Page18: add R241, R201. Page18: add optional 3-pin fan tach circuitry;add optional 3-pin fan speed control circuitry