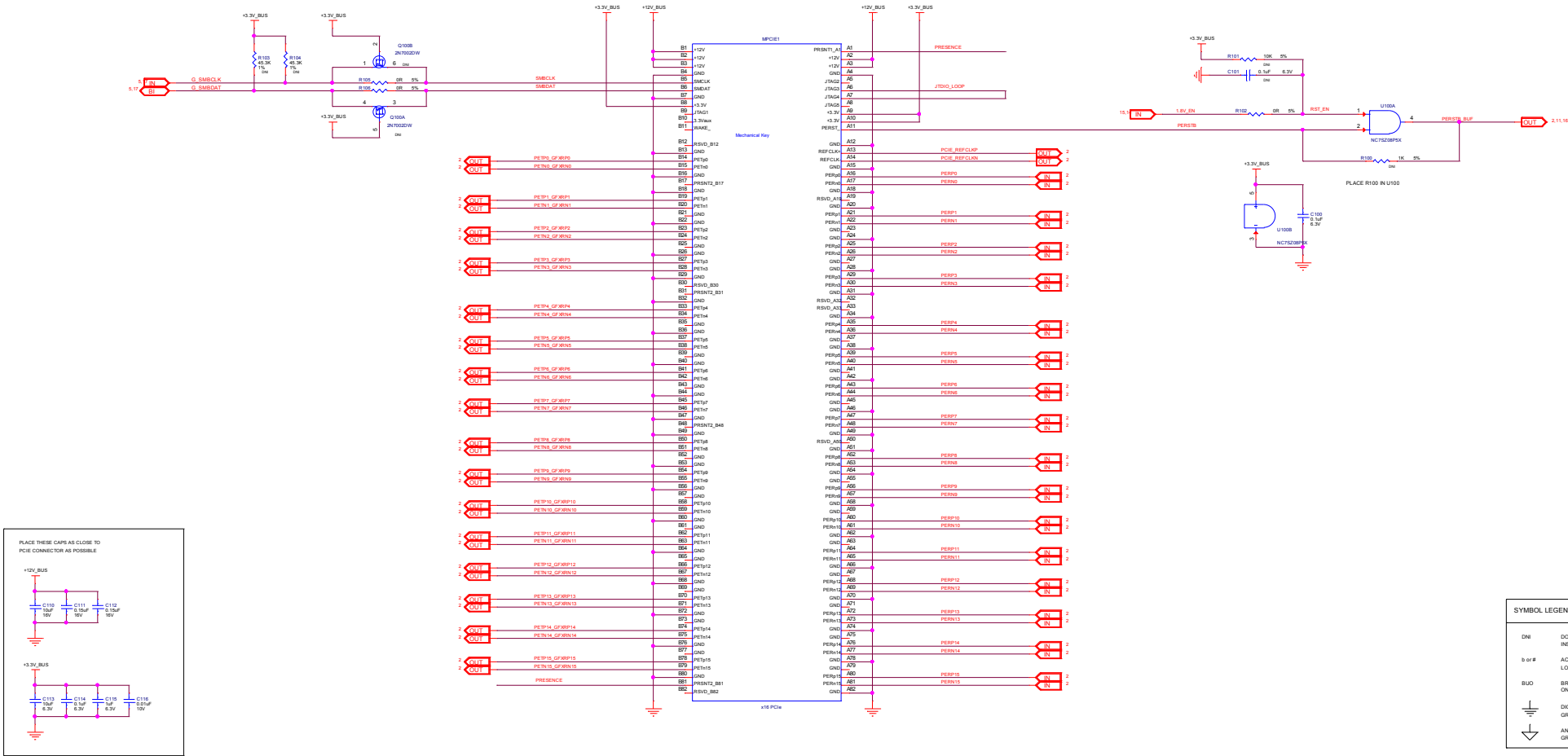


(1) PCI-EXPRESS EDGE CONNECTOR



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SHANGHAI, CHINA 201203

SHEET: PCI-EXPRESS EDGE CONNECTOR

DATE: Mon Nov 24 11:06:52 2014

SHEET NUMBER: 1 OF 19

DOCUMENT NUMBER: 105-C913xx-008

REV: 1.0

TITLE: TOBAGO GDDR5 x32

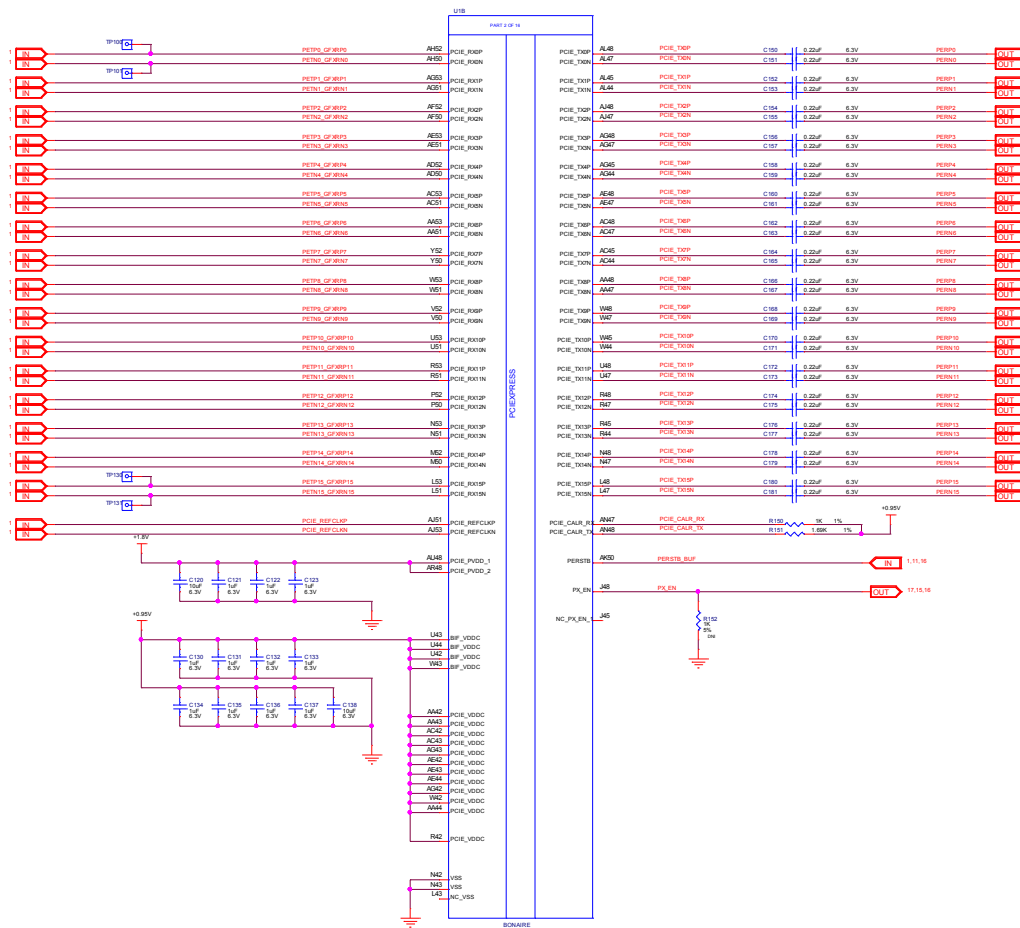
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## (2) TOBAGO PCIE INTERFACE



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SHEET: TOBAGO PCIE

DATE: Mon Nov 24 11:06:52 2014

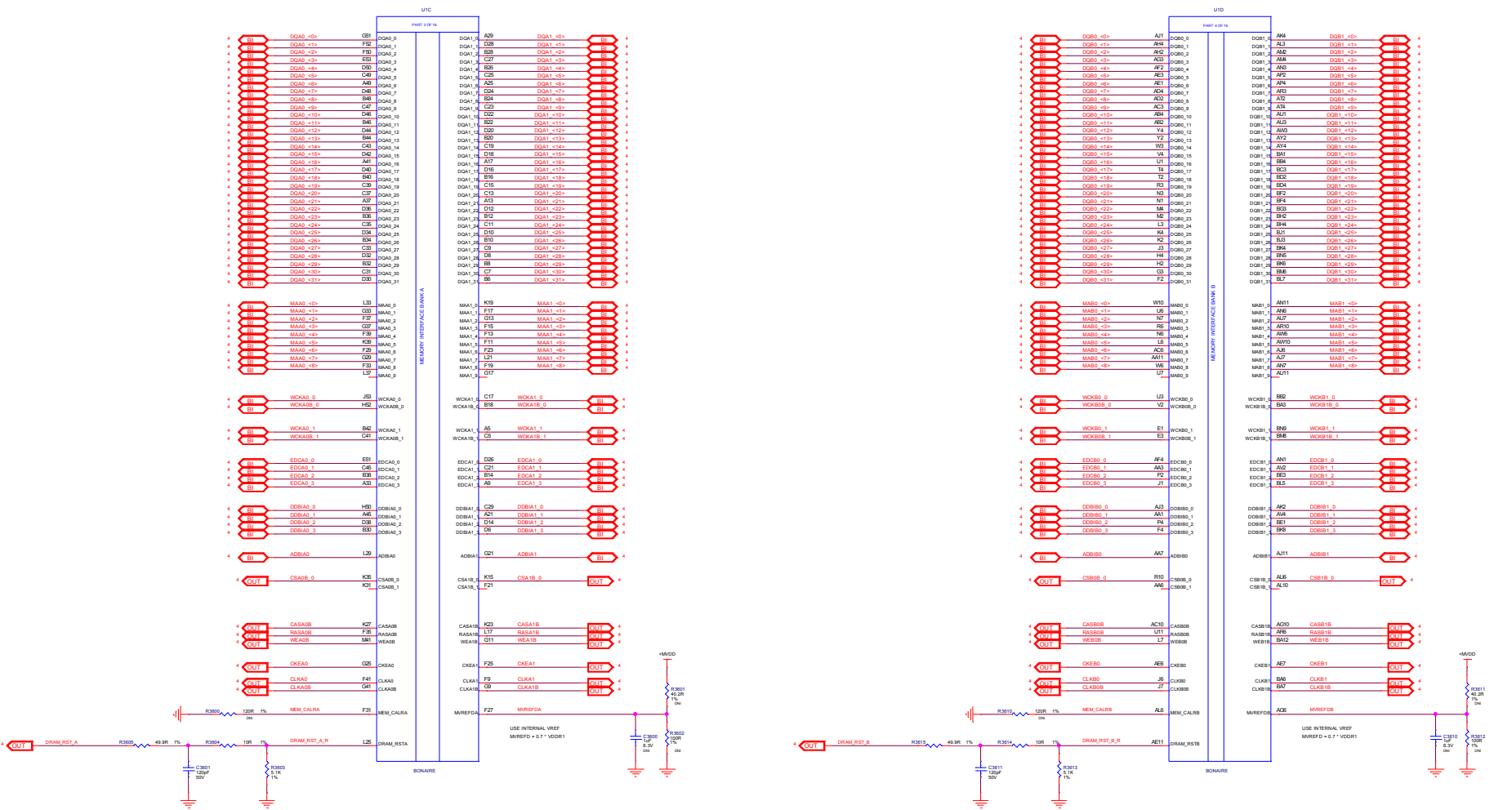
REV: 1.0

SHEET NUMBER: 2 OF 19

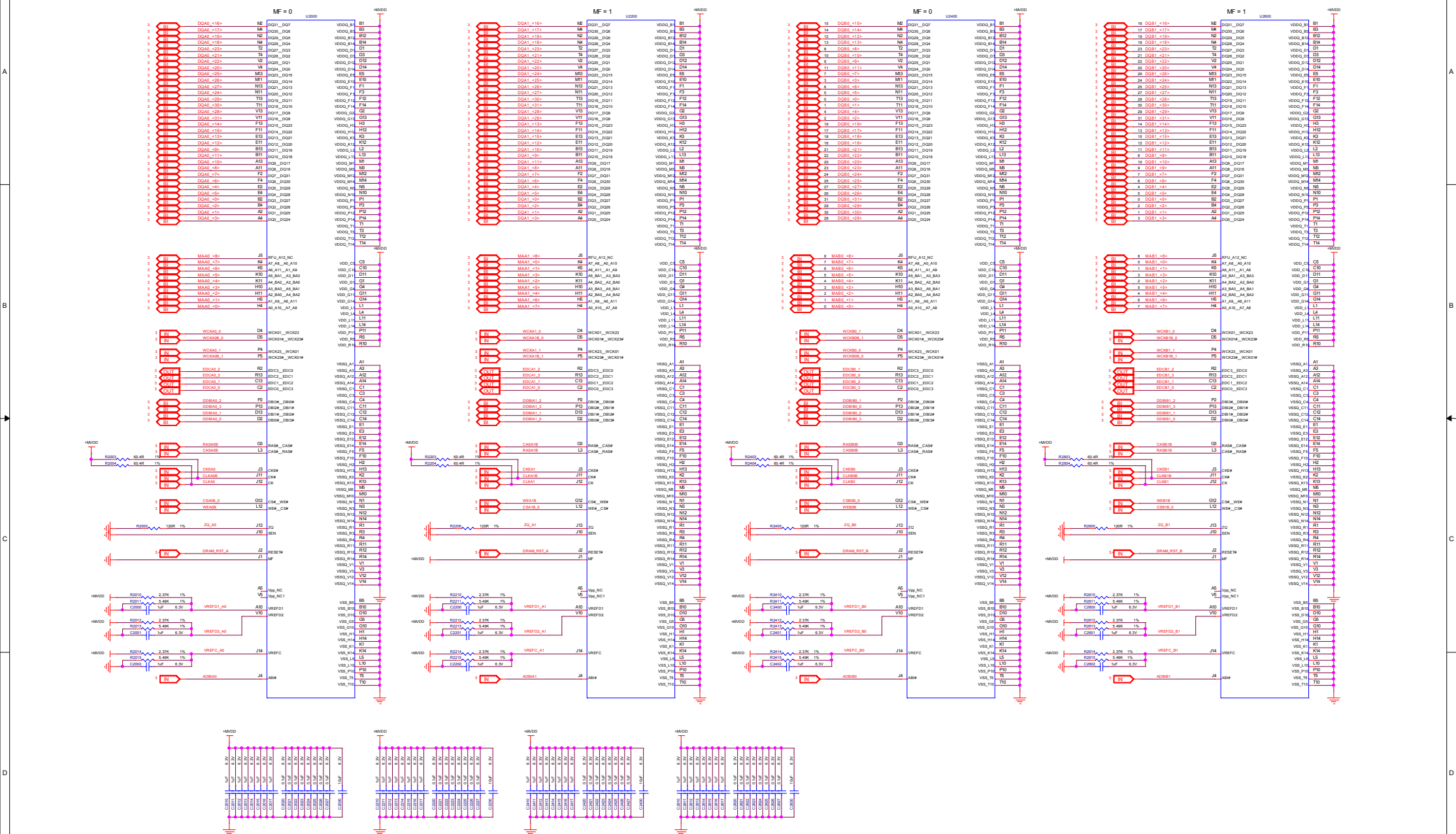
TITLE: TOBAGO GDDR5 x32

DOCUMENT NUMBER: 105-C913xx-00B

(3) TOBAGO MEMORY INTERFACE



(4) GDDR5 CHAB x32



1

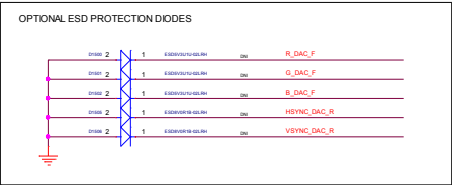
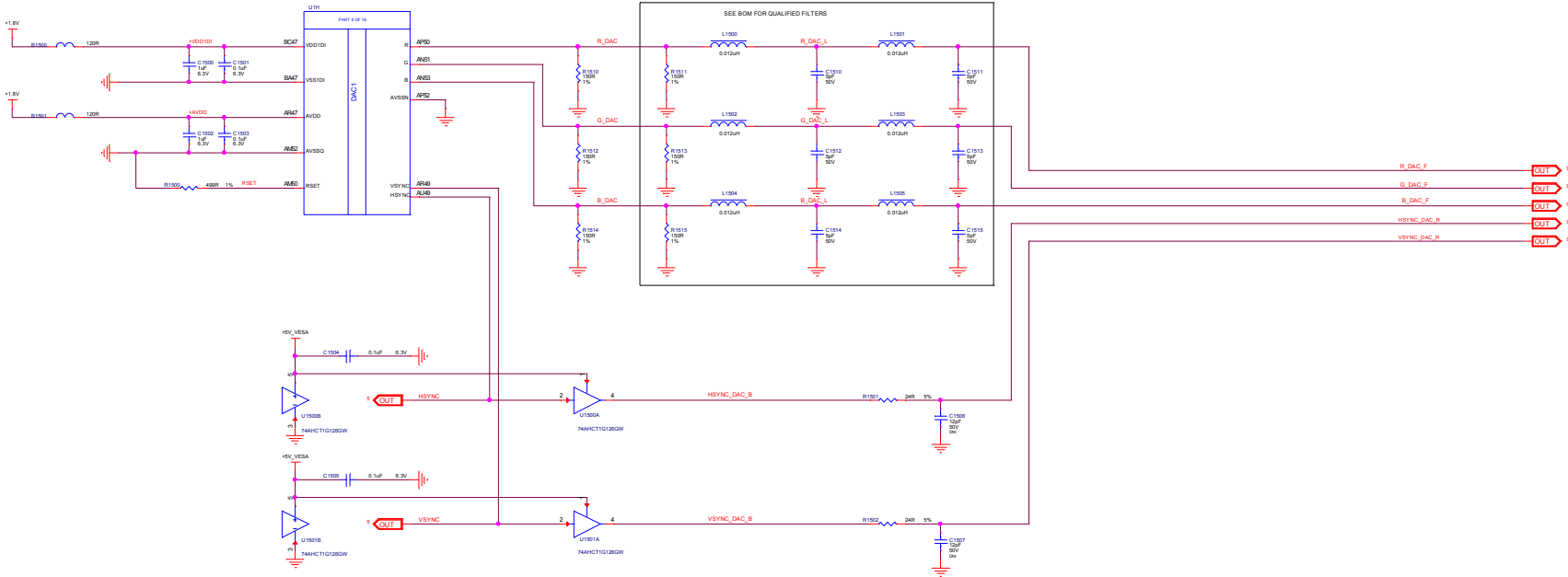


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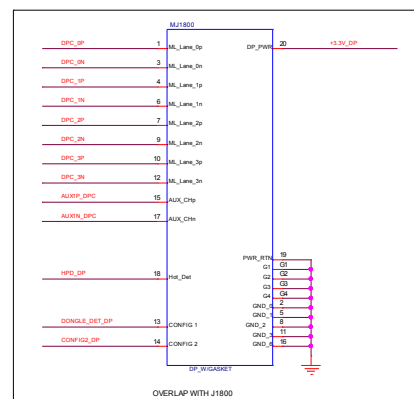
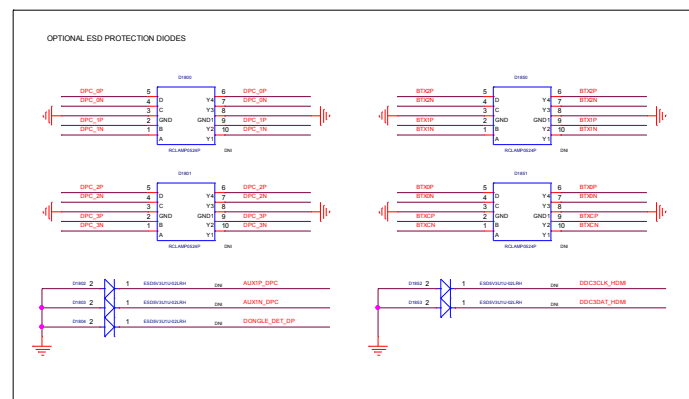
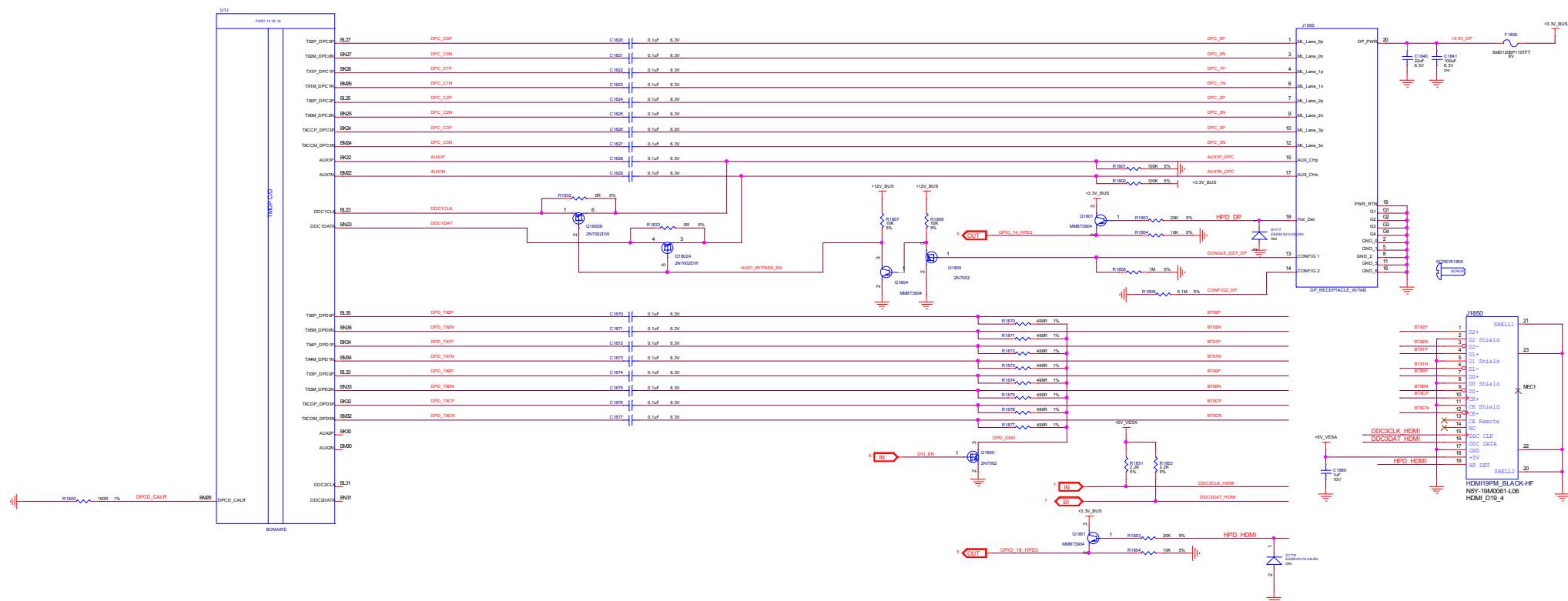
(6) TOBAGO DAC



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SHEET: TOBAGO DAC		REV: 1.0		TITLE: TOBAGO GDDR5 x32	
DATE: Mon Nov 24 11:06:54 2014					
SHEET NUMBER: 6 OF 19					
DOCUMENT NUMBER: 106-C913xx-008					

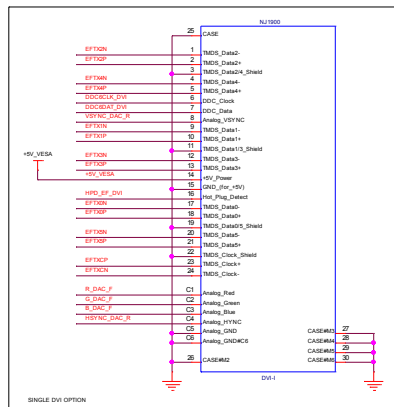
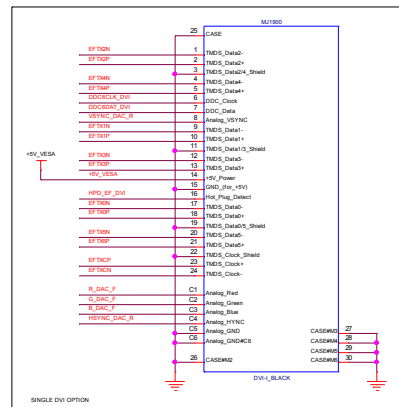
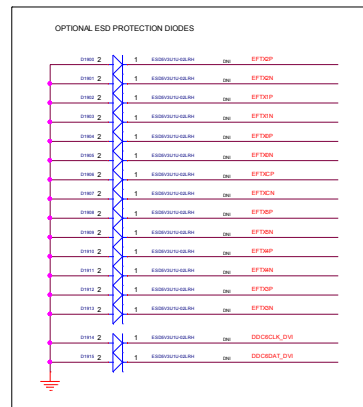
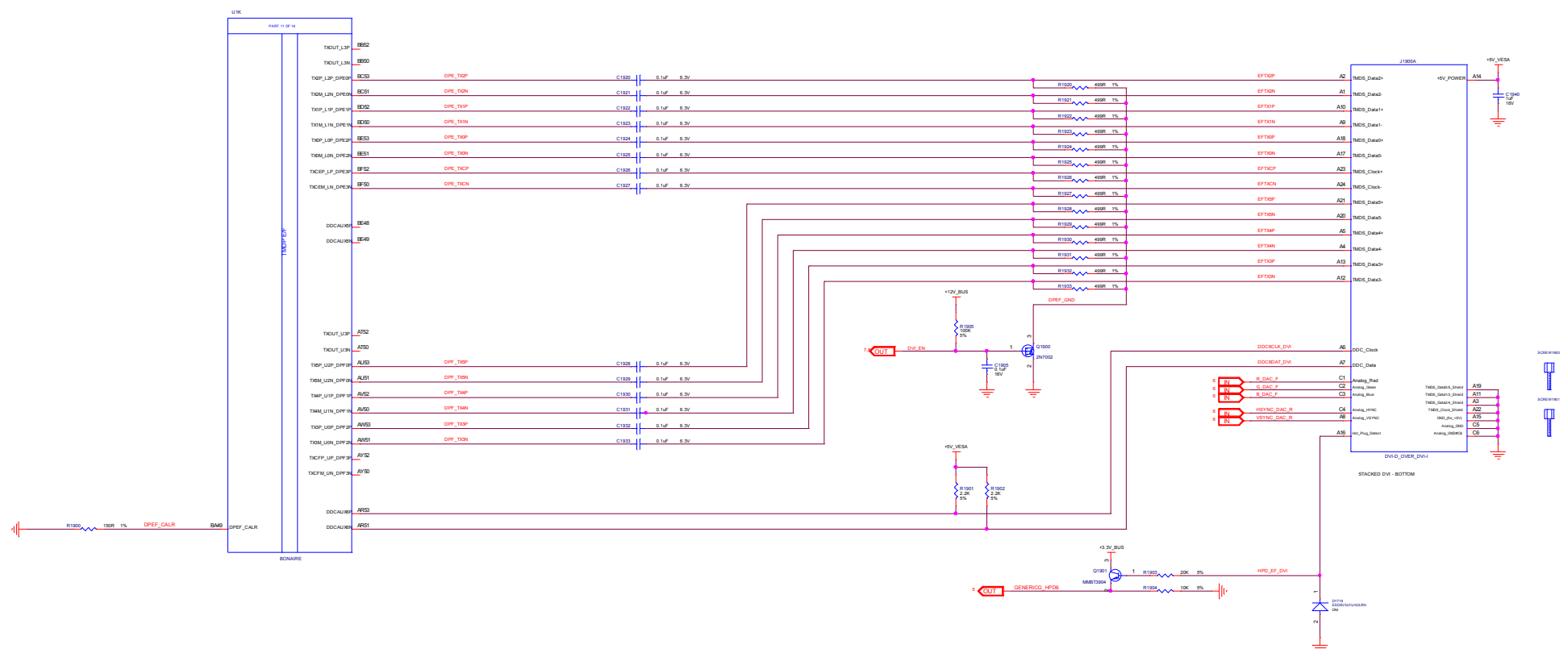
(7) TOBAGO TMDPAB dDVI


(8) TOBAGO TMDPCD DP HDMI



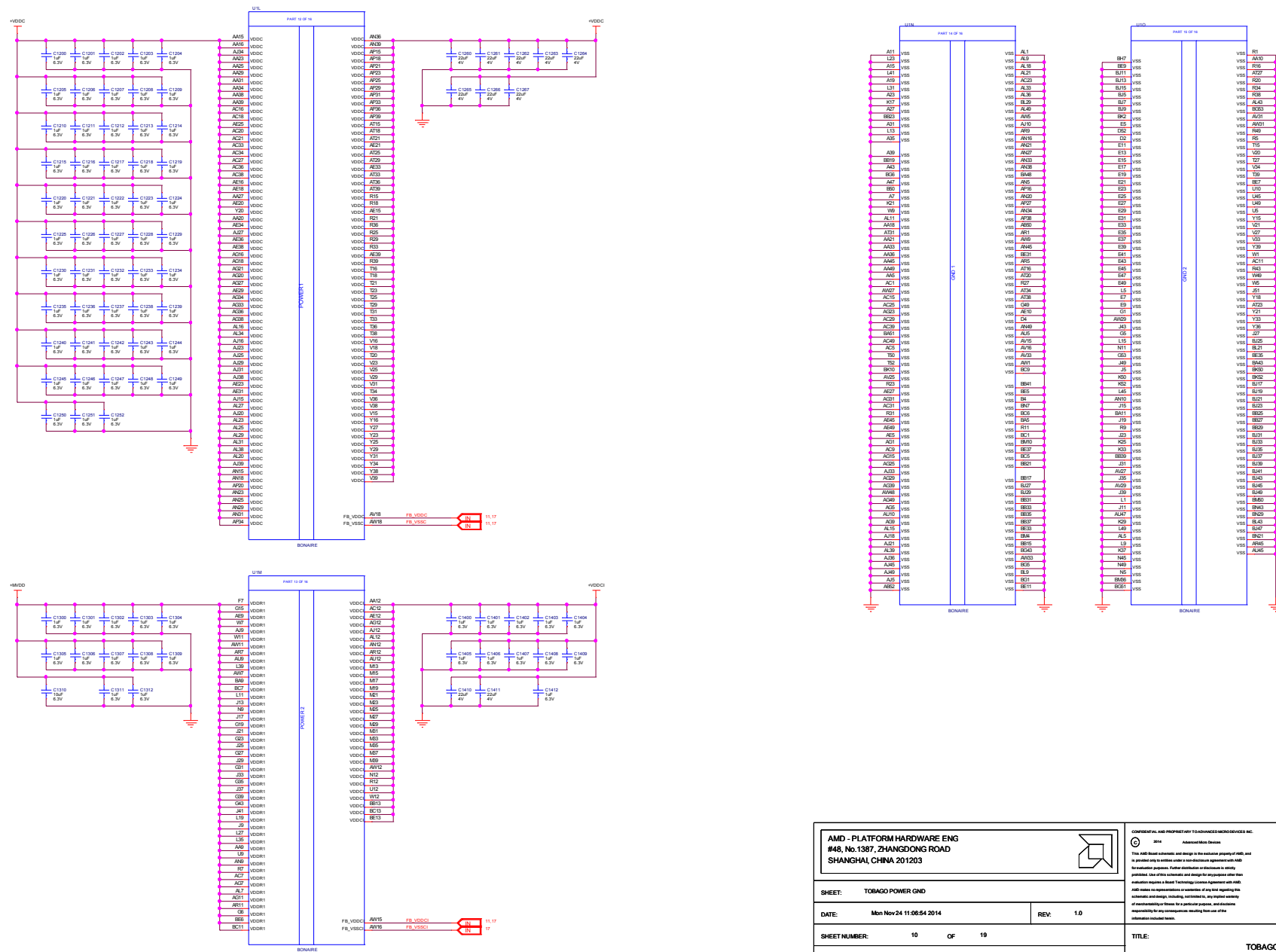


(9) TOBAGO TMDPEF dDVI



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<b>DATE:</b> Mon Nov 24 11:06:54 2014					
<b>SHEET NUMBER:</b> 9 OF 19					
<b>DOCUMENT NUMBER:</b> 105-C913w-008					

(10) TOBAGO POWER AND GROUND



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SHEET: TOBAGO POWER GNI

DATE: Mon Nov 24 11:06:54 2014

SHEET NUMBER: 10 OF 1

DOCUMENT NUMBER: 105-C913xx-00



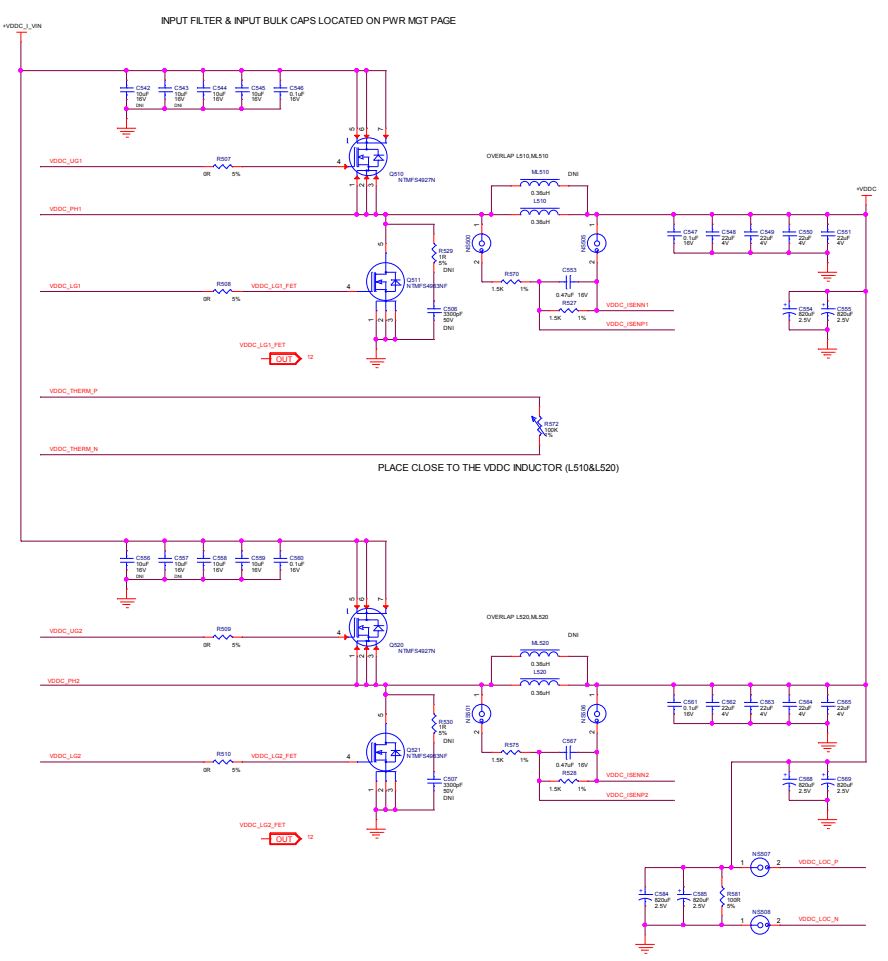
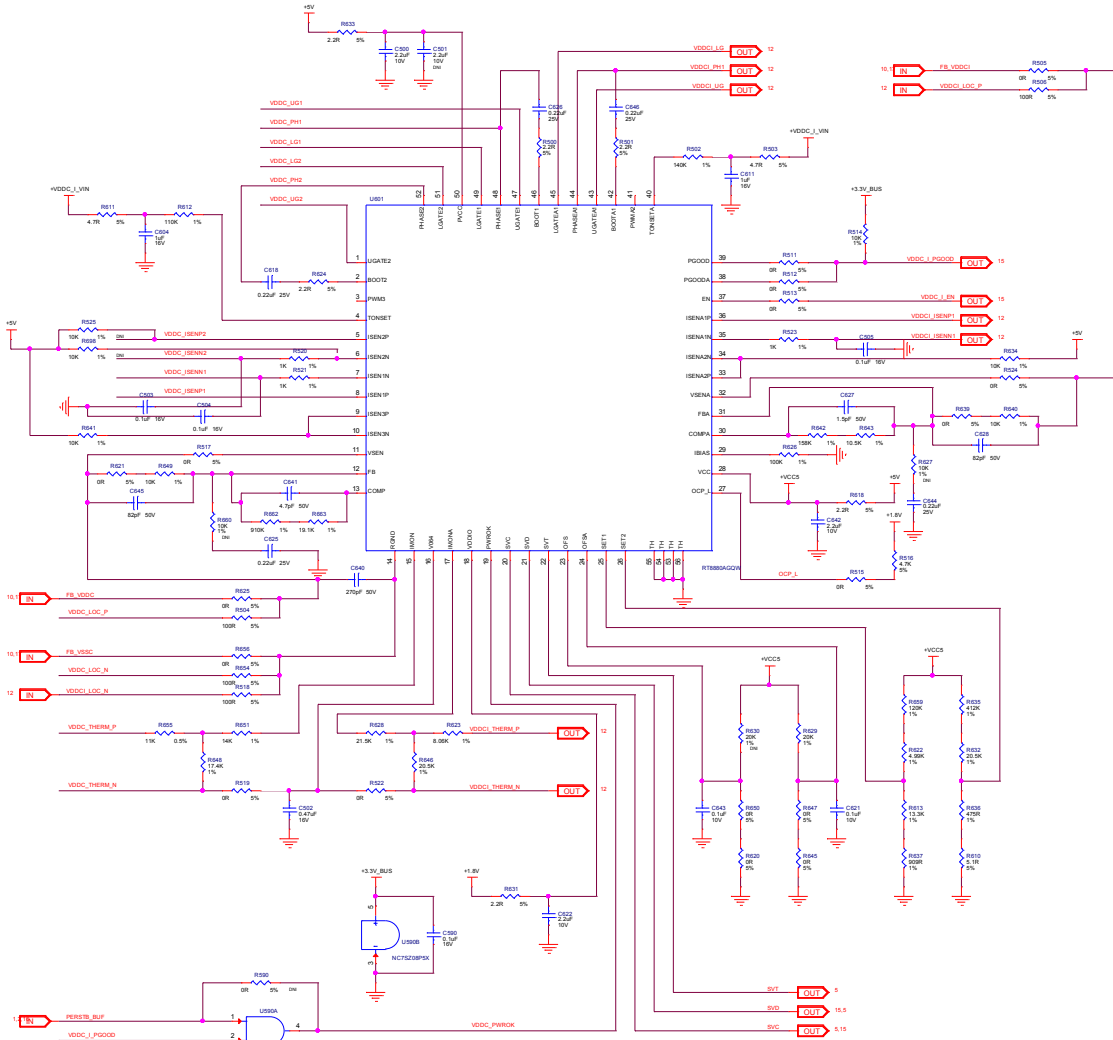
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(11) VDDC\_VDDCI\_I



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SHEET: VDDC\_VDDCI\_I

DATE: Mon Nov 24 11:06:56 2014

SHEET NUMBER: 11 OF 19

DOCUMENT NUMBER: 106-C913xx-008

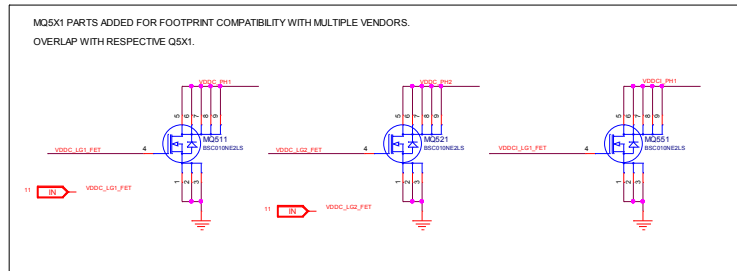
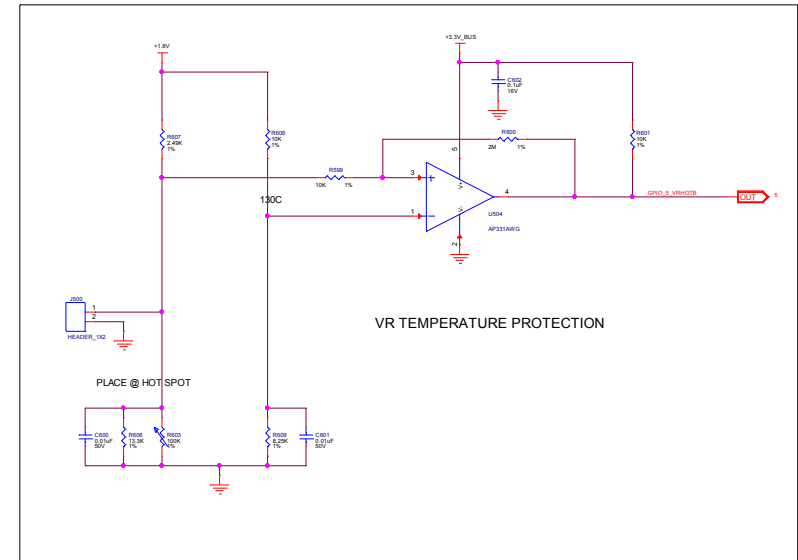
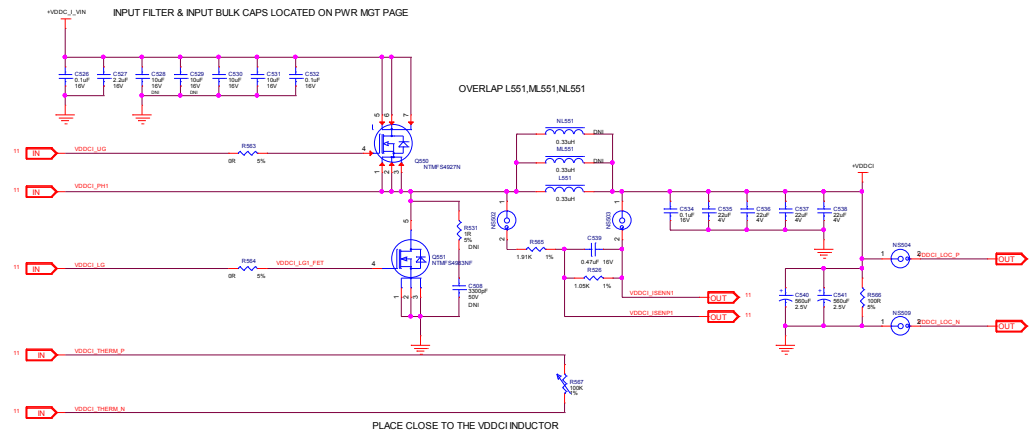
REV: 1.0

TITLE: TOBAGO GDDR5 x32

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(12) VDDC\_VDDCI\_II



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SHEET: VDDC\_VDDCI\_1

DATE: Mon Nov 24 11:06:56 2014

REV: 1.0

SHEET NUMBER: 12 OF 19

DOCUMENT NUMBER: 105-C913xx-00B


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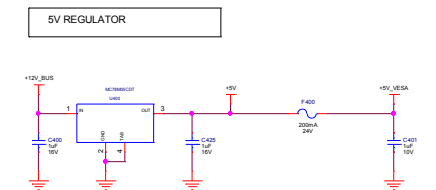
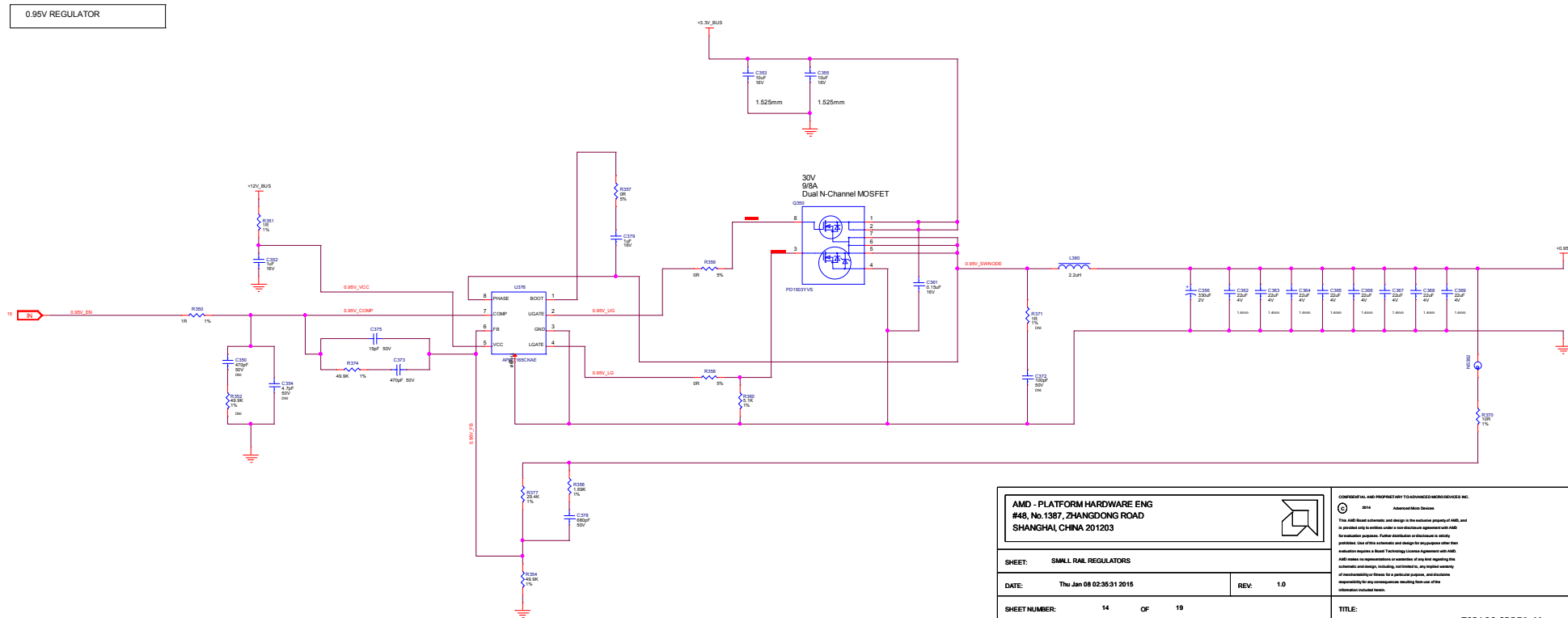
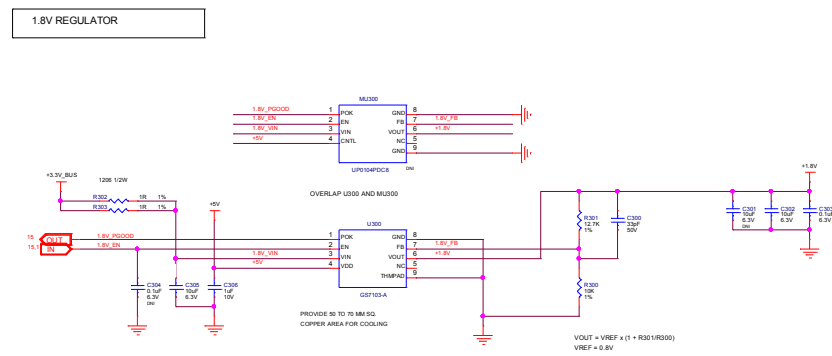
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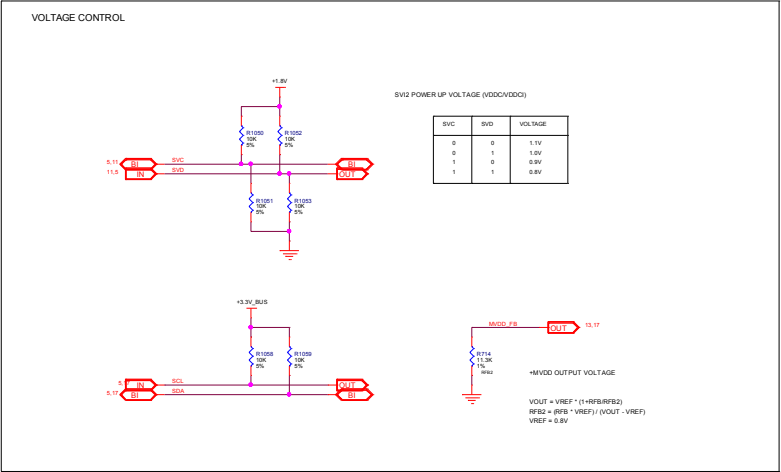
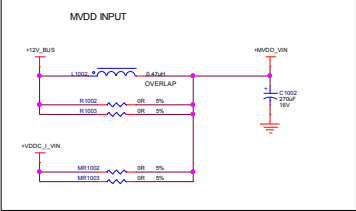
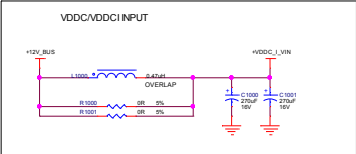
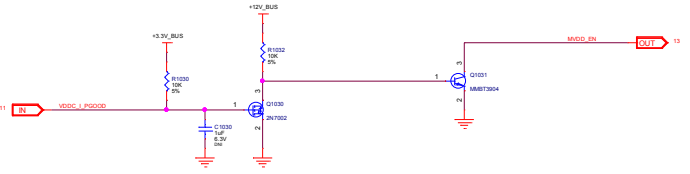
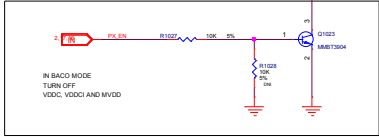
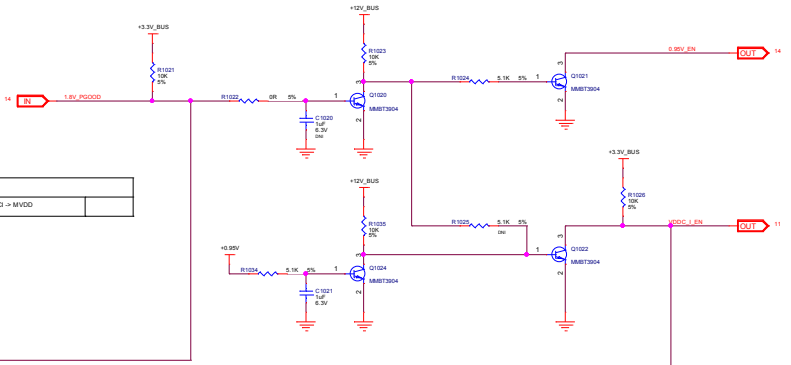
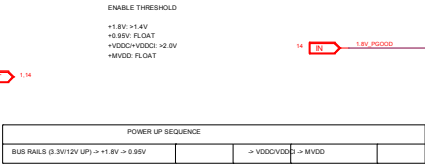
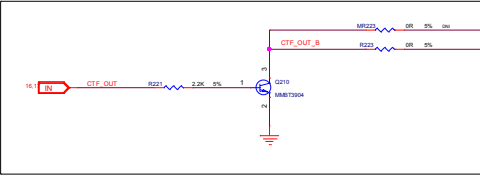
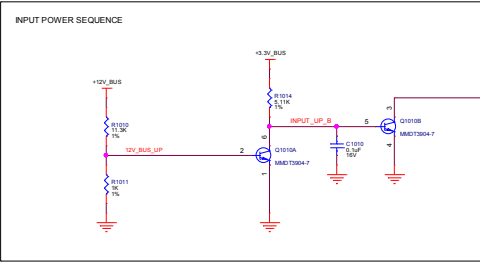
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SHEET: MDDO		REV: 1.0		TITLE:	
DATE: Mon Nov 24 11:06:56 2014				TORBAGO GDDR3 x32	
SHEET NUMBER: 13 OF 19					
DOCUMENT NUMBER: 105-C913xx-008					

#### (14) SMALL RAIL REGULATORS



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SHEET:	SMALL RAIL REGULATORS				
DATE:	Thu Jan 08 02:35:31 2015	REV:	1.0	TITLE:	TOBAGO GDPRS x32
SHEET NUMBER:	14 OF 19				
DOCUMENT NUMBER:	105-C913xx-008				

(15) POWER MANAGEMENT



SVC	SVD	VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

MVD OUTPUT VOLTAGE

$$VOUT = VREF * (1 + R1/R2/R3)$$
$$VREF = (VDDC - VREF) / (VOUT - VREF)$$
$$VREF = 0.8V$$

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SHEET: POWER MANAGEMENT

DATE: Mon Nov 24 11:06:56 2014

SHEET NUMBER: 15 OF 19

DOCUMENT NUMBER: 105-C913xx-008

REV: 1.0

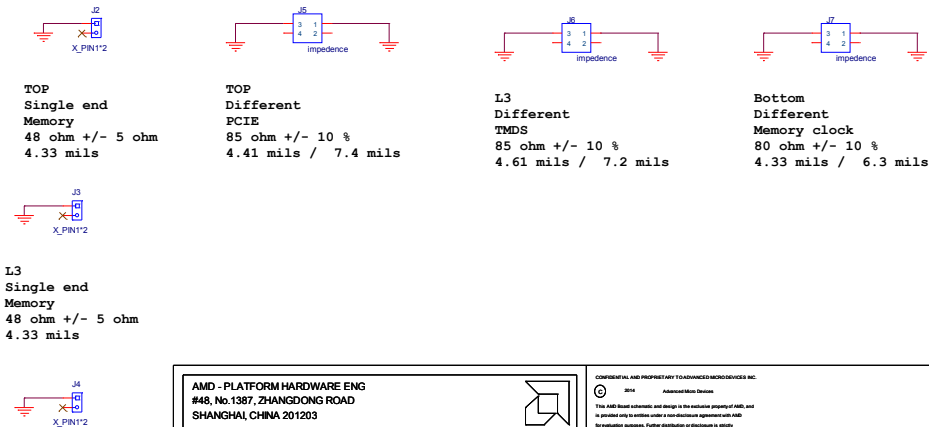
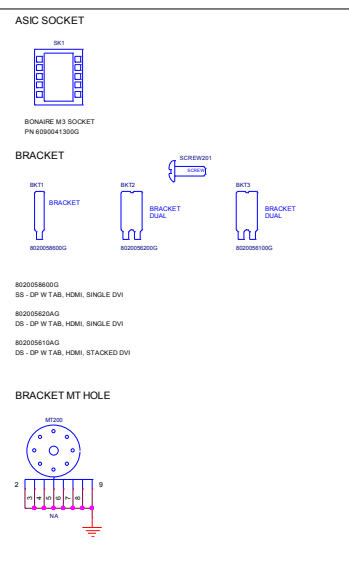
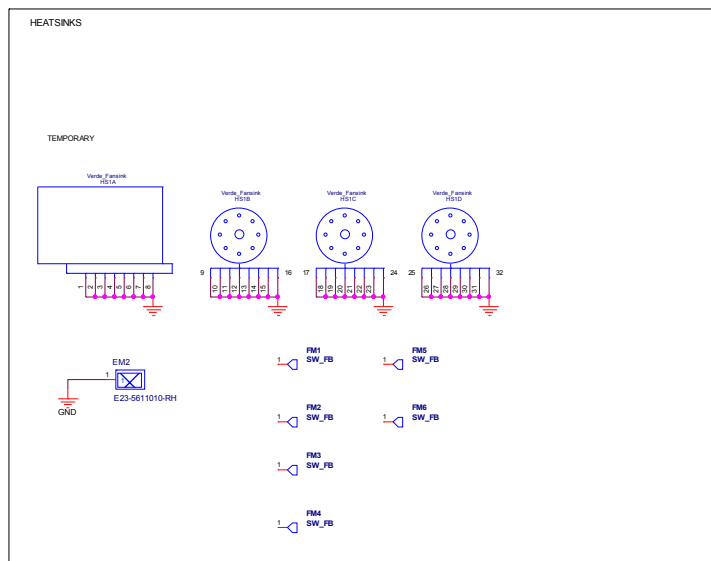
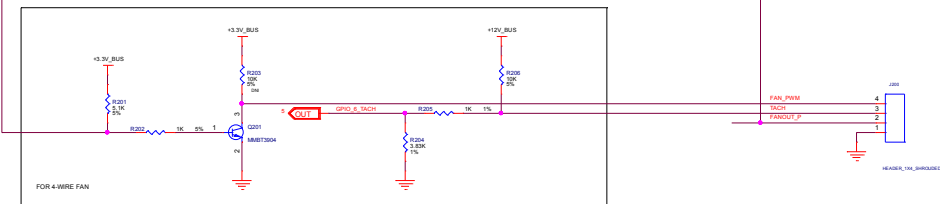
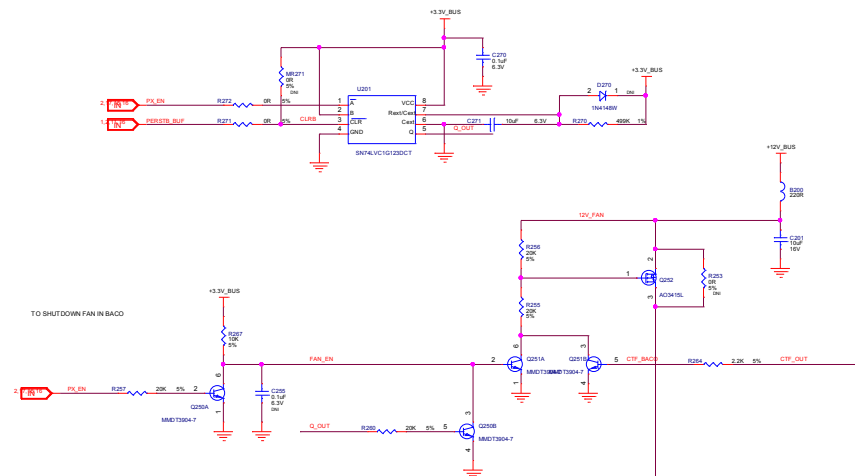
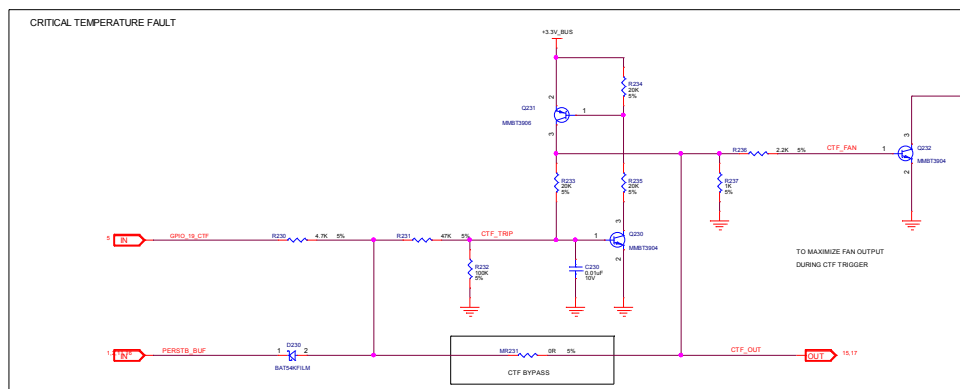
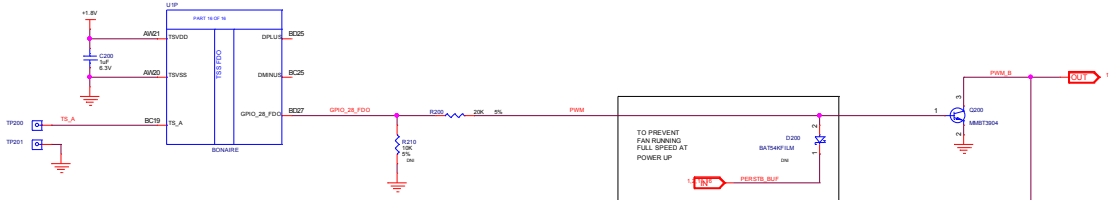
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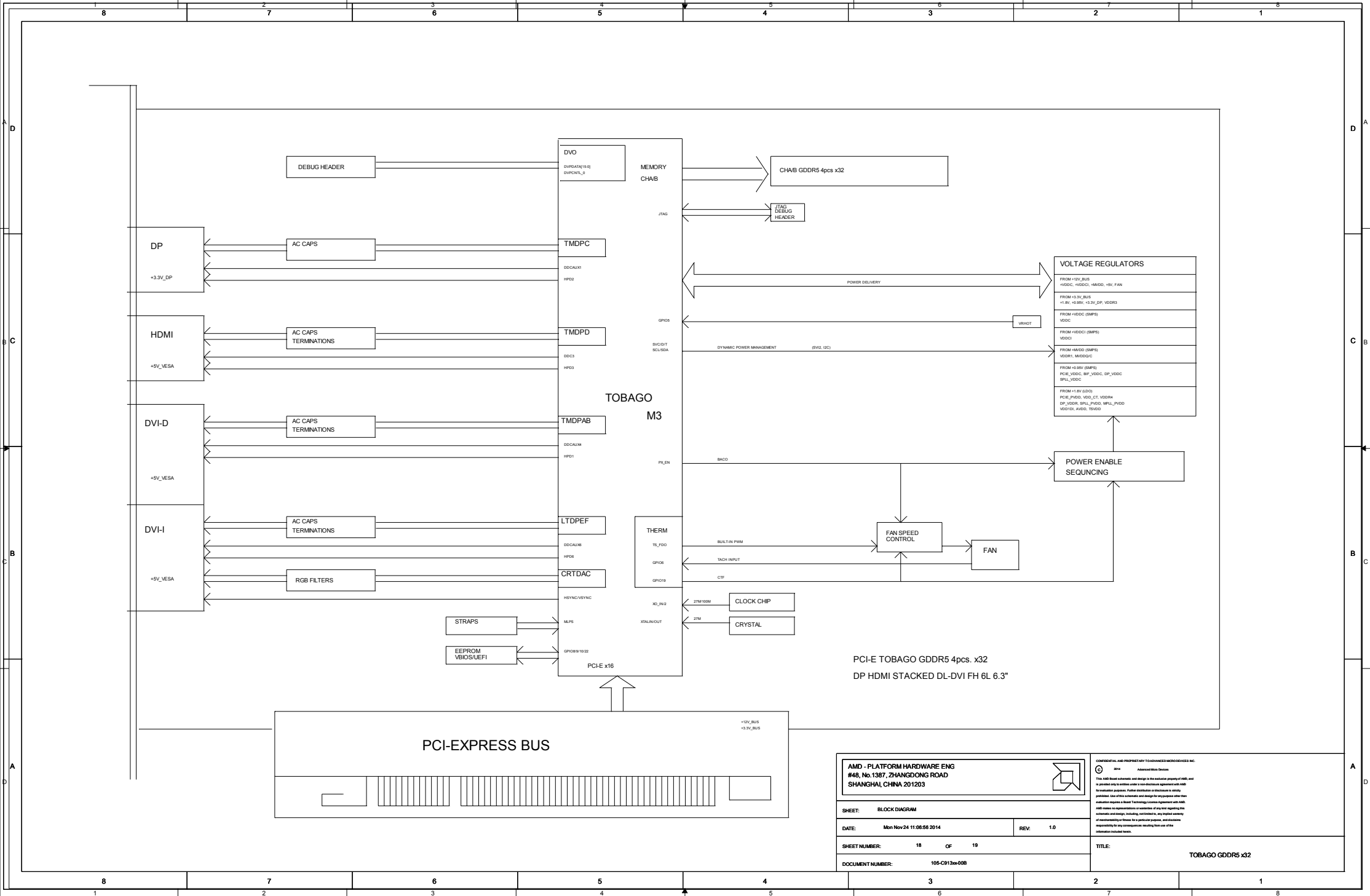
## (16) MECHANICAL AND THERMAL MANAGEMENT



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<b>SHEET NUMBER: 16 OF 19</b>					
<b>DOCUMENT NUMBER: 105-C913a-00B</b>					









TITLE:

TOBAGO GDDR5 x32

DOCUMENT NUMBER:

105-C913xx-008

DATE:

Mon Nov 24 11:27:56 2014

SHEET NUMBER:

19

OF

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## REVISION HISTORY

ENGINEER:

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NOTES:

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SCH  
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Rev

Date

REVISION DESCRIPTION

1

00A

08/18/2014

INITIAL DESIGN

1

00B

11/26/2014

CONNECTED TO VDD3