NAVI14 GDDR6 4PCS,8L 3xDPs +1xHDMI

105-D332xx-00B RevB Desktop board(110W TGP)

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MS-V382

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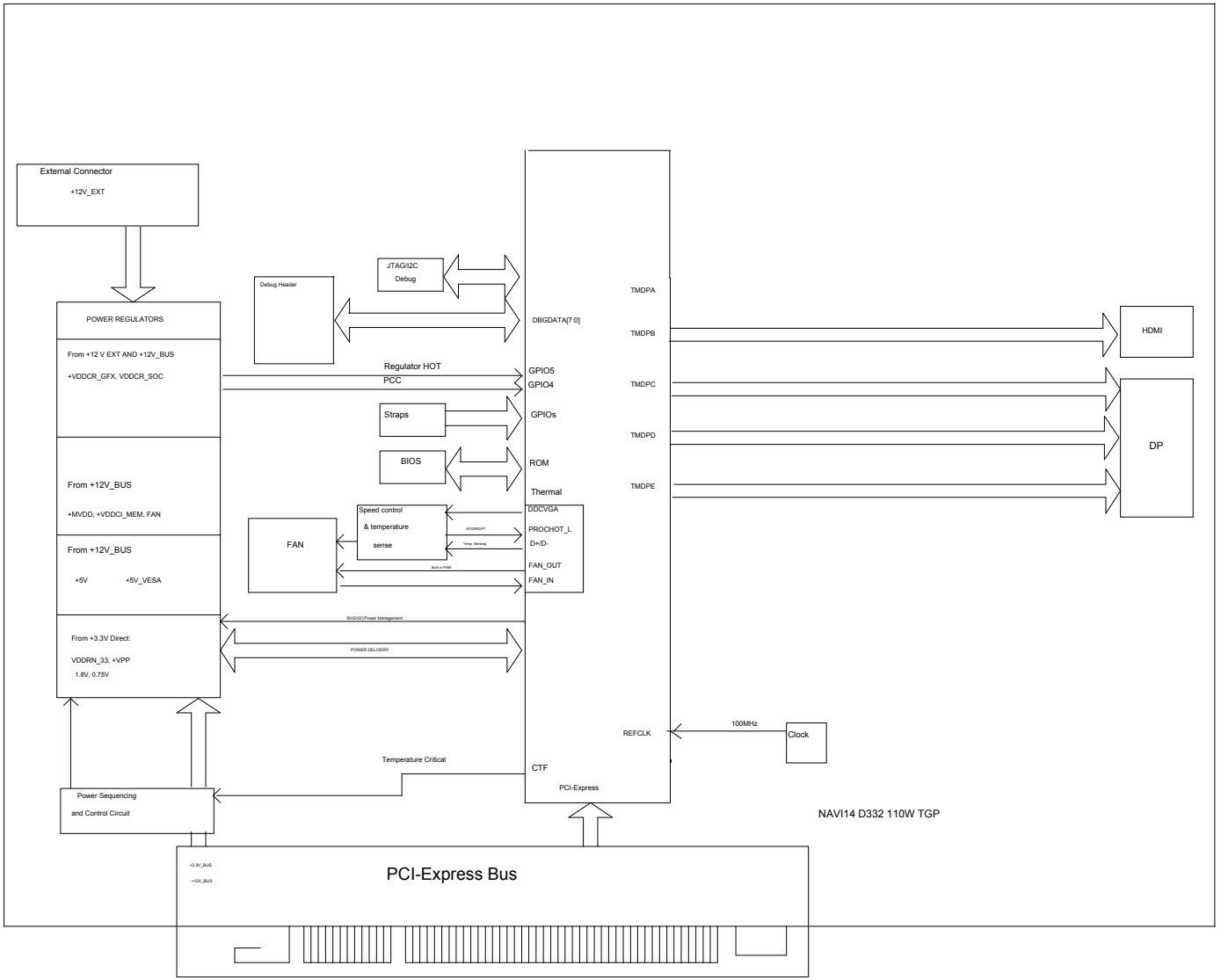

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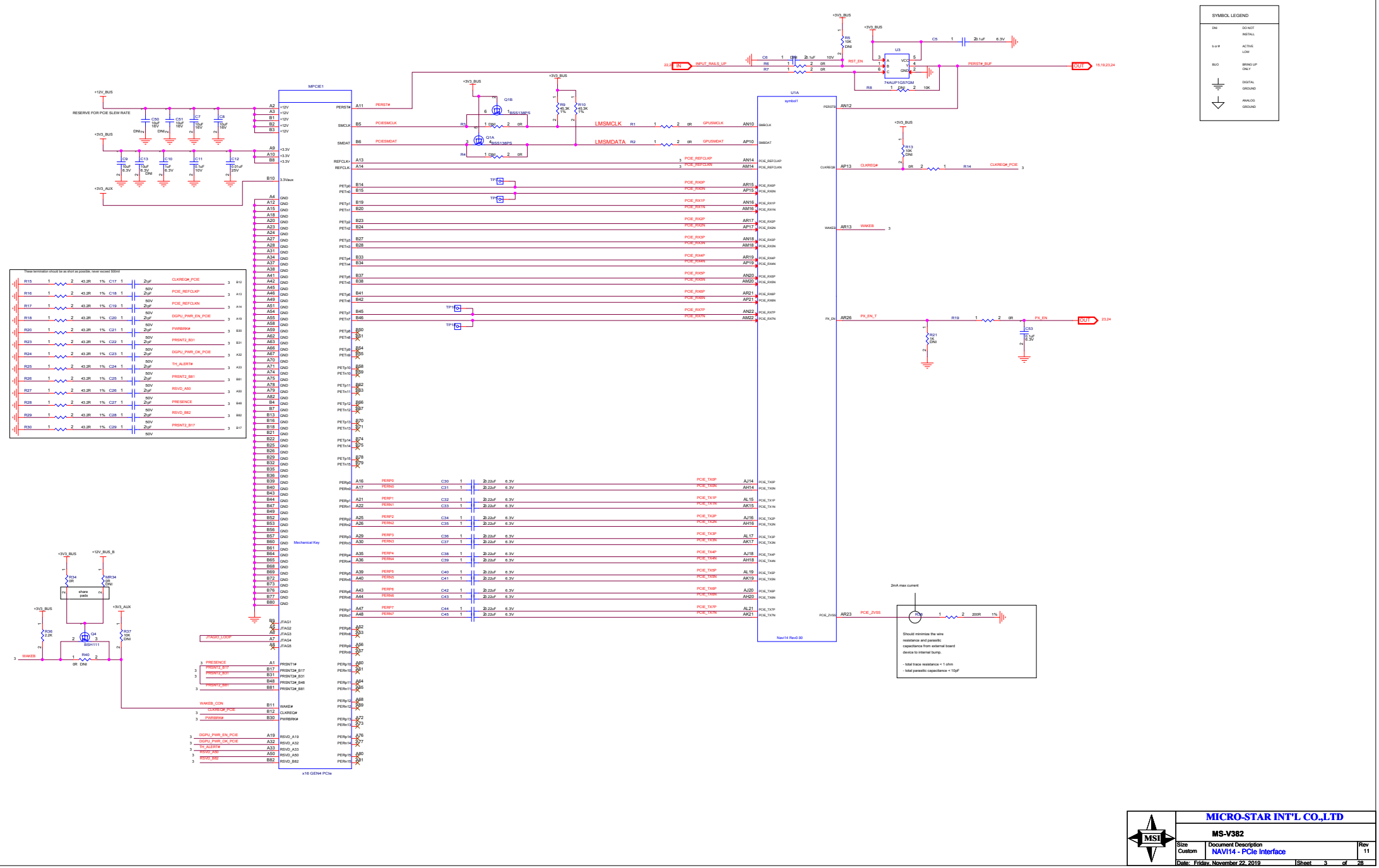

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MS-V382			
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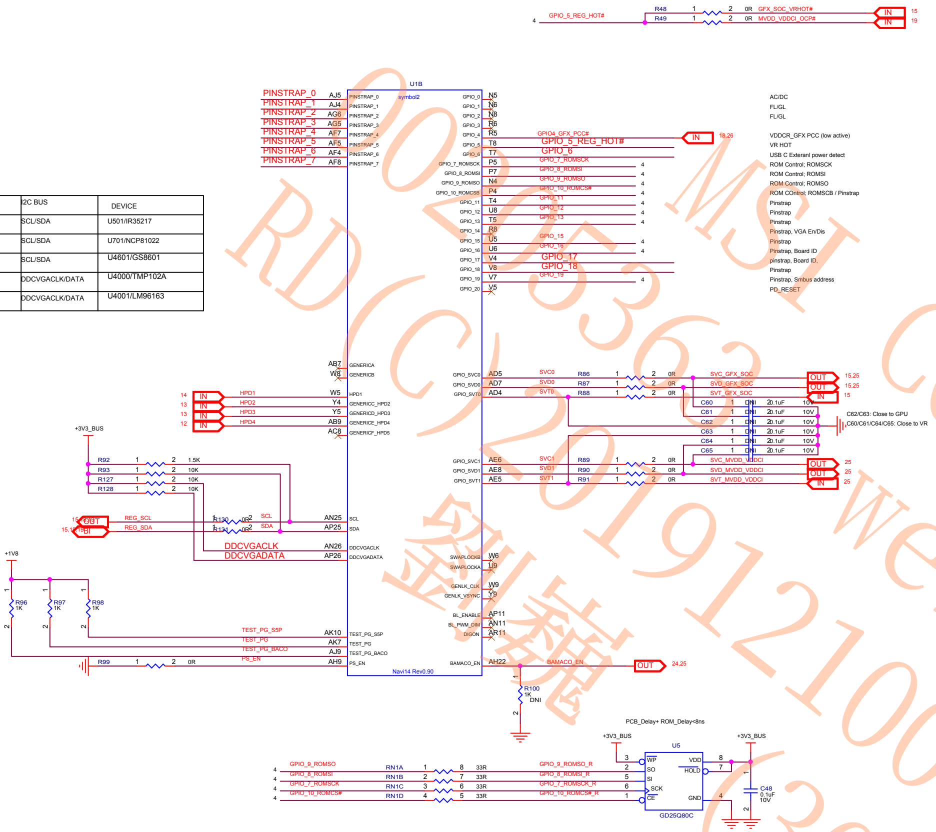
(4) NAVI14 GPIOs & ROM



7-BIT I2C ADDRESS	8-BIT I2C ADDRESS	FUNCTION	I2C BUS	DEVICE
0x30	0x60	VDDCR_GFX/SOC	SCL/SDA	U501/IR35217
0x22	0x44	MVDD/VDDCI	SCL/SDA	U701/NCP81022
0x53	0xA6	PCCψreserved	SCL/SDA	U4601/GS8601
0x48	0x90	G6 Temperture	DDCVGACLK/DATA	U4000/TMP102A
0x4C	0x98	EXT SENSOR	DDCVGACLK/DATA	U4001/LM96163

Note: Internal PU/PD at GPIO pad is ~40k strength in 14nm design spec

+3V3_BUS +1V8

User	Strap circuit	Internal Default Value	Definition
BIF	R51 1 DNI 2 10K; R52 1 DNI 2 10K; PINSTRAP_6 4	0	STRAP_BIF_GEN4_DIS_A 0: PCIe GEN 4 supported 1: PCIe GEN 4 not supported
BIF	R53 1 DNI 2 10K; R54 1 DNI 2 10K; PINSTRAP_7 4	0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled
BIF	R56 1 DNI 2 10K; R57 1 DNI 2 10K; GPIO_13 4	0	PINSTRAP_BIF_LC_TX_SWING 0: Full swing mode 1: Reduced swing mode(half swing)
BIF	R58 1 DNI 2 10K; R59 1 DNI 2 10K; GPIO_15 4	0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognised as the system's VGA controller
DCE	R60 1 DNI 2 10K; R61 1 DNI 2 10K; PINSTRAP_5 4 R62 1 DNI 2 10K; R63 1 DNI 2 10K; PINSTRAP_4 4 R64 1 DNI 2 10K; R65 1 DNI 2 10K; PINSTRAP_3 4	0 0 0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected Deafault(PINSTRAP5,PINSTRAR4,PINSTRAR3) = 000
DCE	R66 1 2 10K; R67 1 DNI 2 10K; GPIO_12 4 R68 1 2 10K; R69 1 DNI 2 10K; GPIO_11 4	0 0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for both DisplayPort and HDMI Deafault(GPIO12,GPIO11) = 11
Platform	R70 1 DNI 2 10K; R71 1 DNI 2 10K; GPIO_18 4 R72 1 DNI 2 10K; R73 1 DNI 2 10K; GPIO_17 4	0 0	PINSTRAP_FIG[1:0] - No definition on NV
Platform	R74 1 2 10K; R75 1 DNI 2 10K; RN700A 1 DNI 4 100R 0.1%; GPIO_16 4	0	PINSTRAP_MVDD_FB_DIVIDER_CONFIG 0: Divider does not exist 1: Divider exists
SMU	R76 1 DNI 2 10K; R77 1 DNI 2 10K; PINSTRAP_2 4 R78 1 DNI 2 10K; R79 1 DNI 2 10K; PINSTRAP_1 4 R80 1 DNI 2 10K; R81 1 DNI 2 10K; PINSTRAP_0 4	1 0 1	PINSTRAP_BFI_MEM_AP_SIZE[2:0] Or PINSTRAP_ROM_CONFIG[2:0] 100 - 512KBIT (ST) M25P05A 101 - 1MBIT (ST) (M25P10A) 101 - 2MBIT (ST) M25P20 101 - 4MBIT (ST) M25P40 101 - 8MBIT (ST) M25P80 100 - 512KBIT (CHINGIS) PM25LV512 101 - 1MBIT (CHINGIS) PM25LV010 Deafault(PINSTRAP2,PINSTRAR1,PINSTRAR0) = 101
SMU	R82 1 DNI 2 10K; R83 1 DNI 2 10K; GPIO_19 4	0	PINSTRAP_SMBUS_ADDR 0: 0x41h 1: 0x40h
SMU	R84 1 DNI 2 10K; R85 1 DNI 2 10K; GPIO_10_ROMCS# 4	1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device
	R124 1 DNI 2 1K; R125 1 DNI 2 10K; GPIO_6 4		

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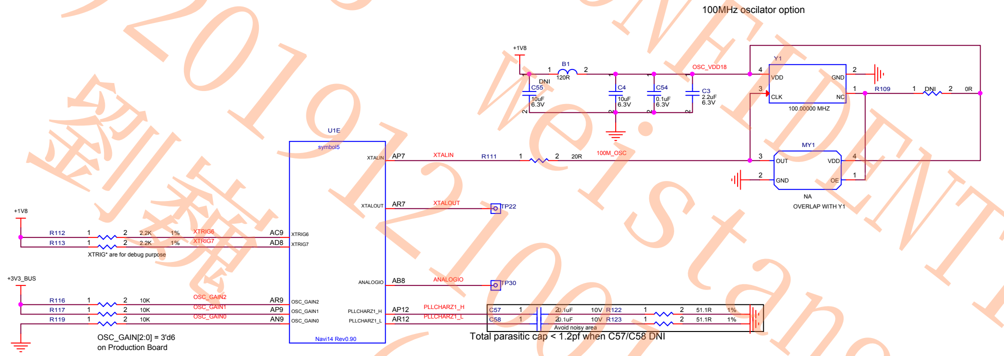
(5) NAVI14 XTAL



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00205363 weistang(唐浩倢)
RD(C)20191121001 RMA工程課
劉蘋(30001789)

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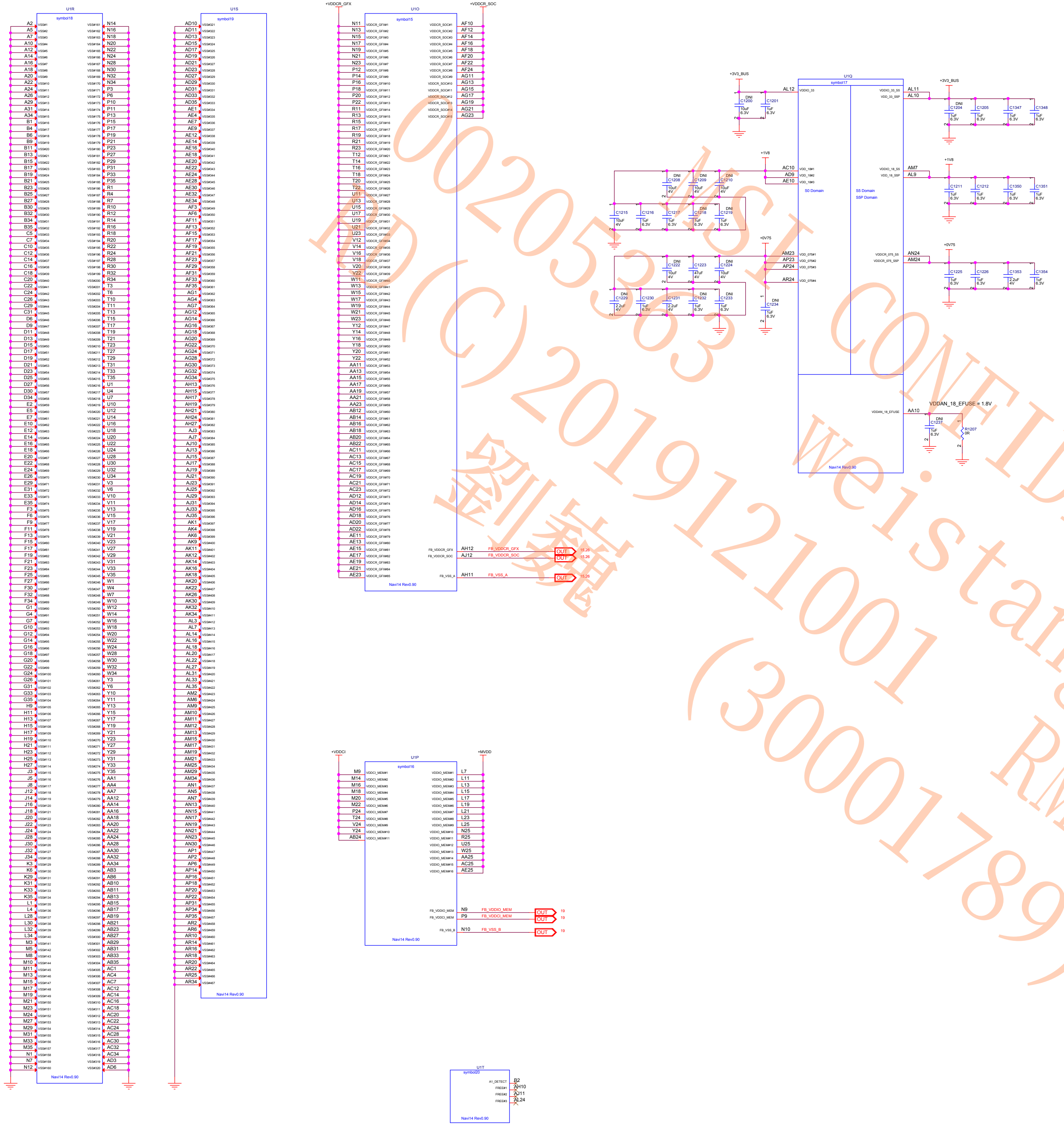
(6) NAVI14 POWER AND GND



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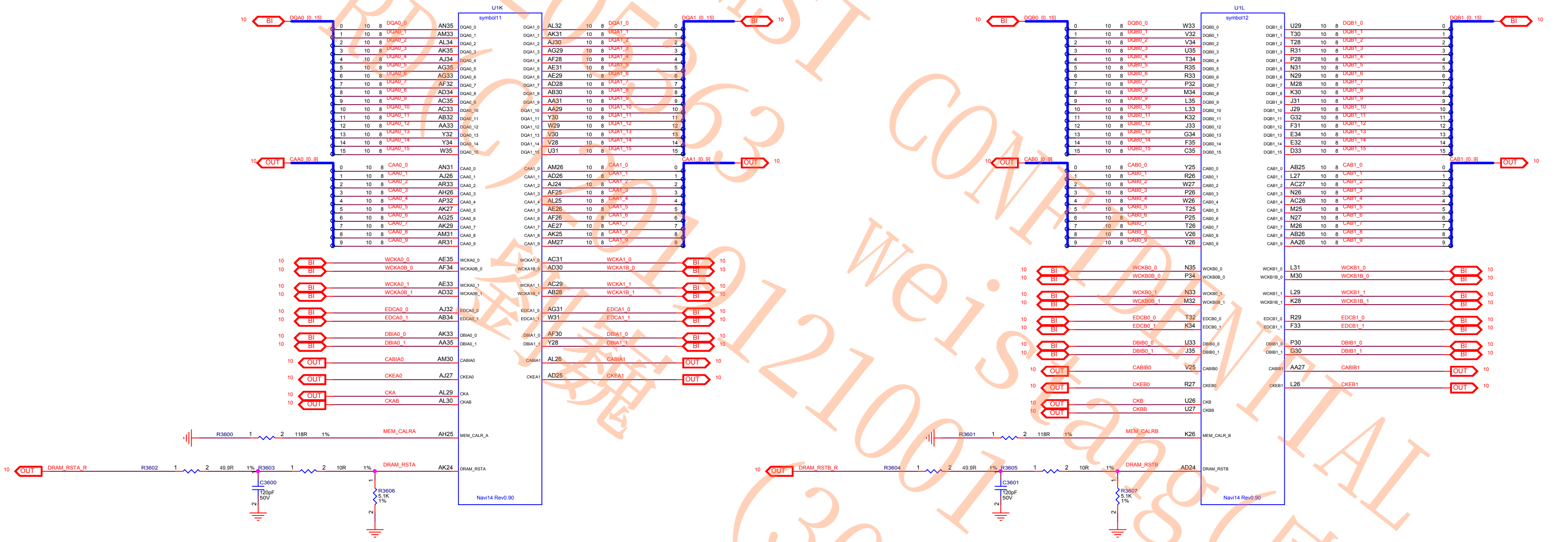
(8) NAVI14 MEM INTERFACE CH A/B



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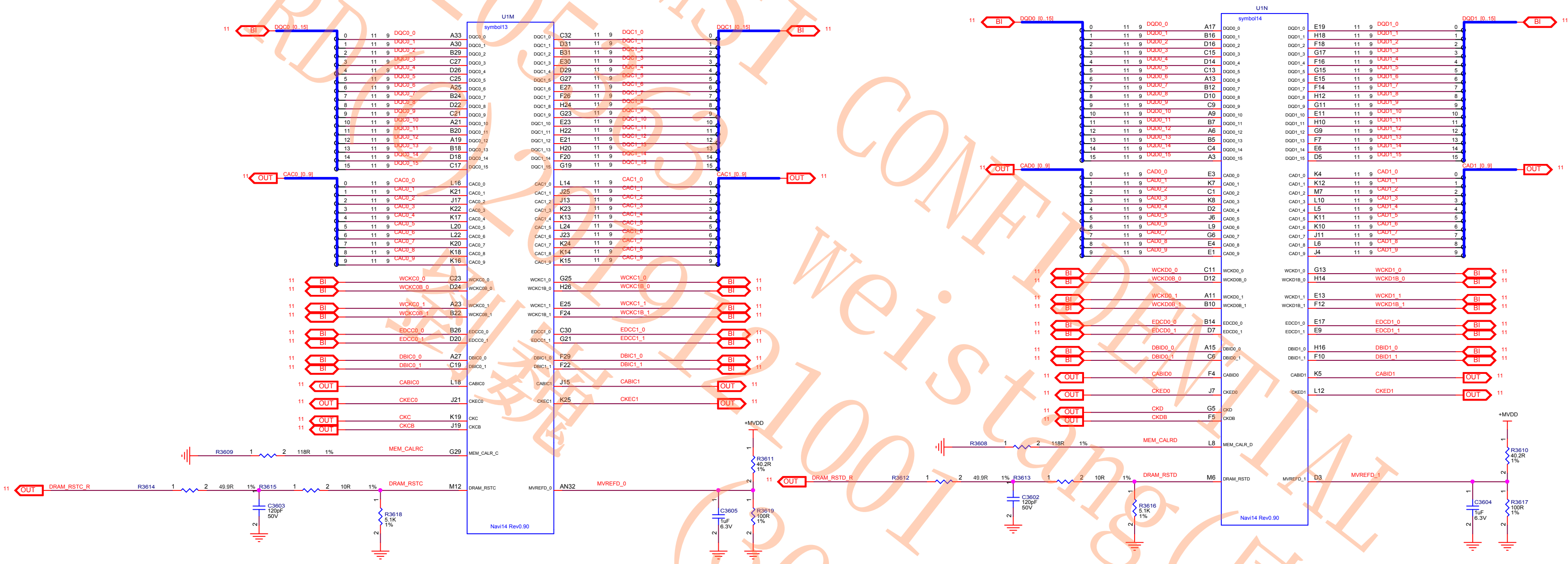
(9) NAVI14 MEM INTERFACE CH C/D



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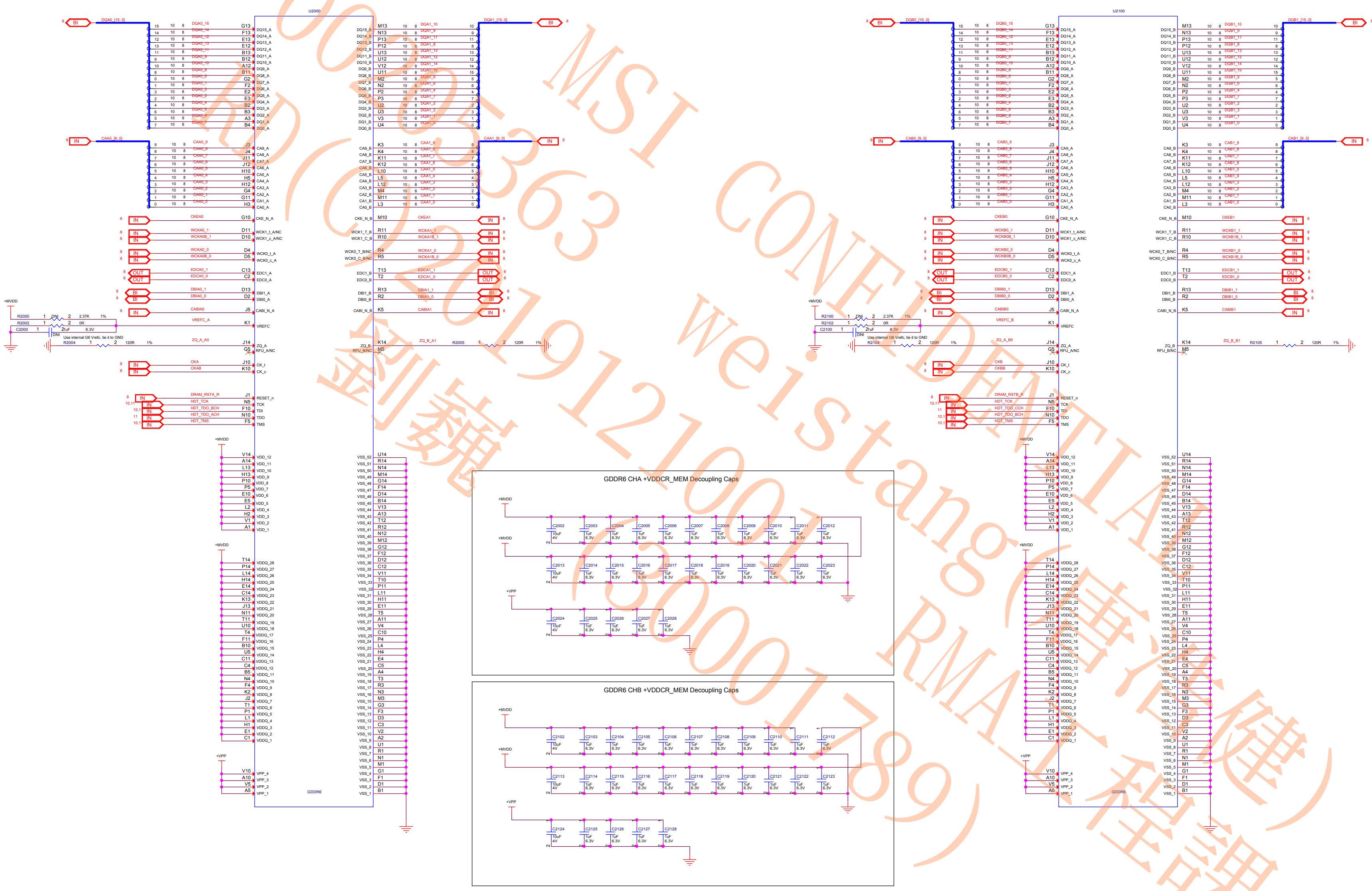
(10) GDDR6x16 CHAB Memory



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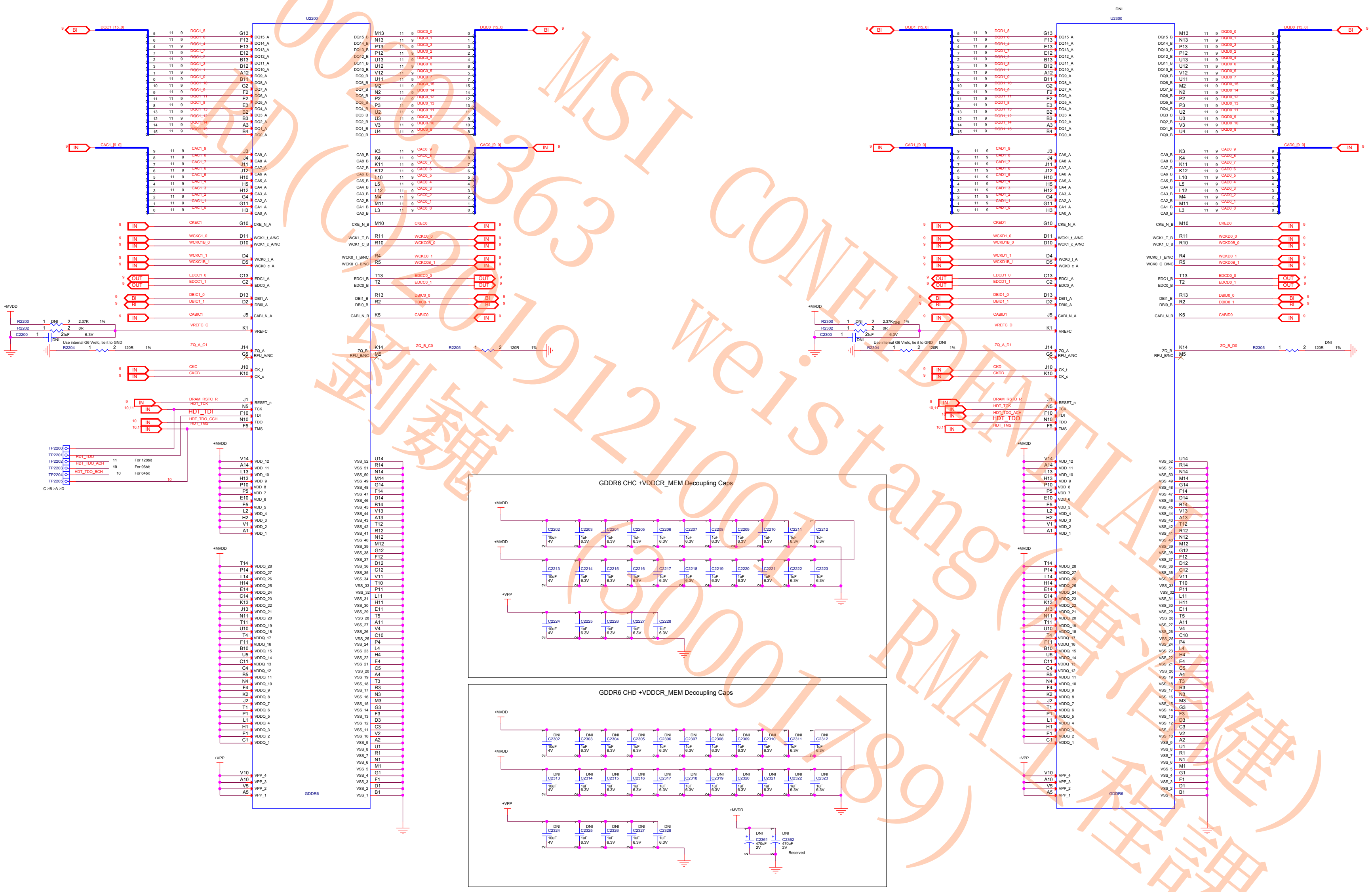
(11) GDDR6x16 CHCD Memory



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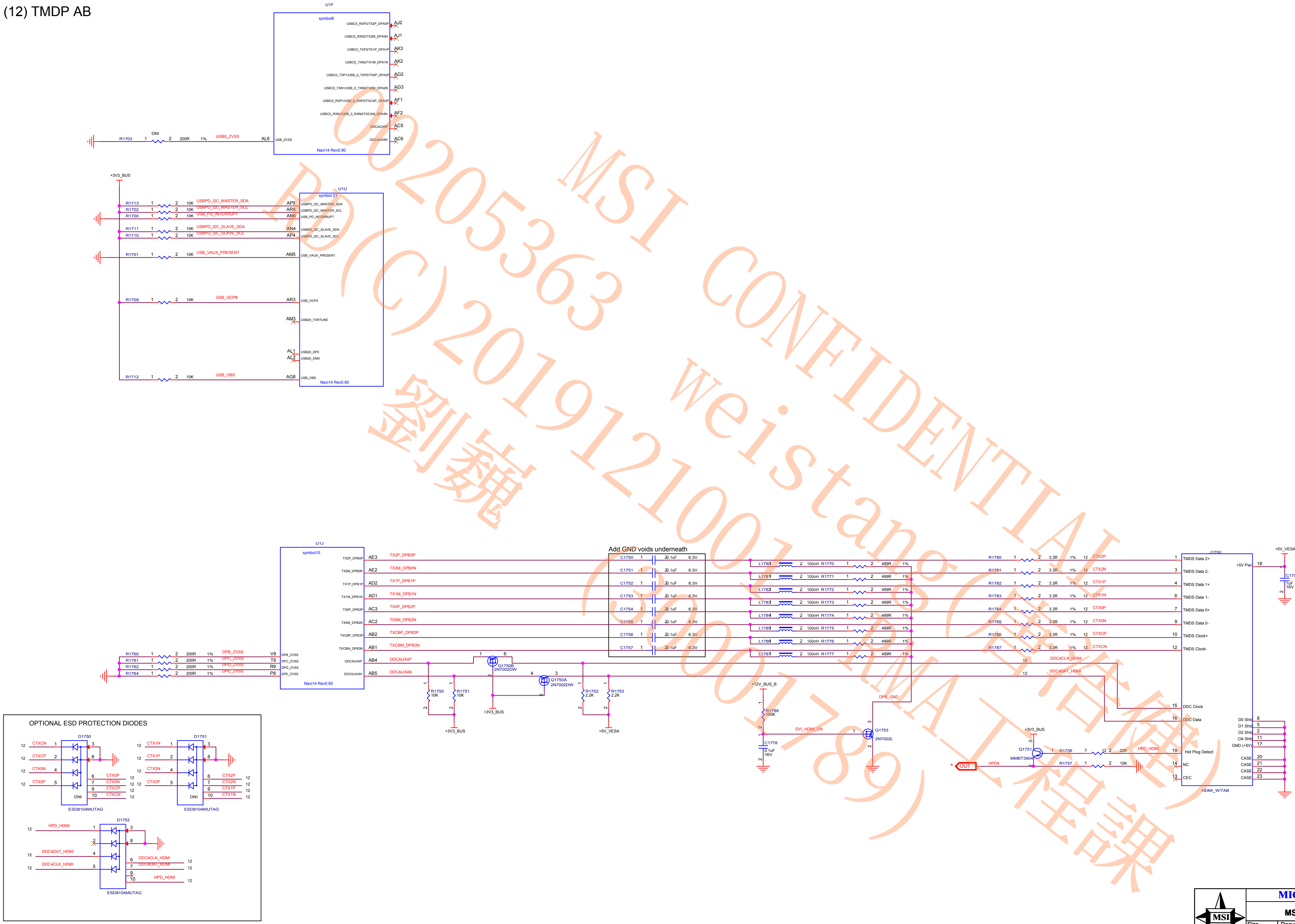
(12) TMDP AB



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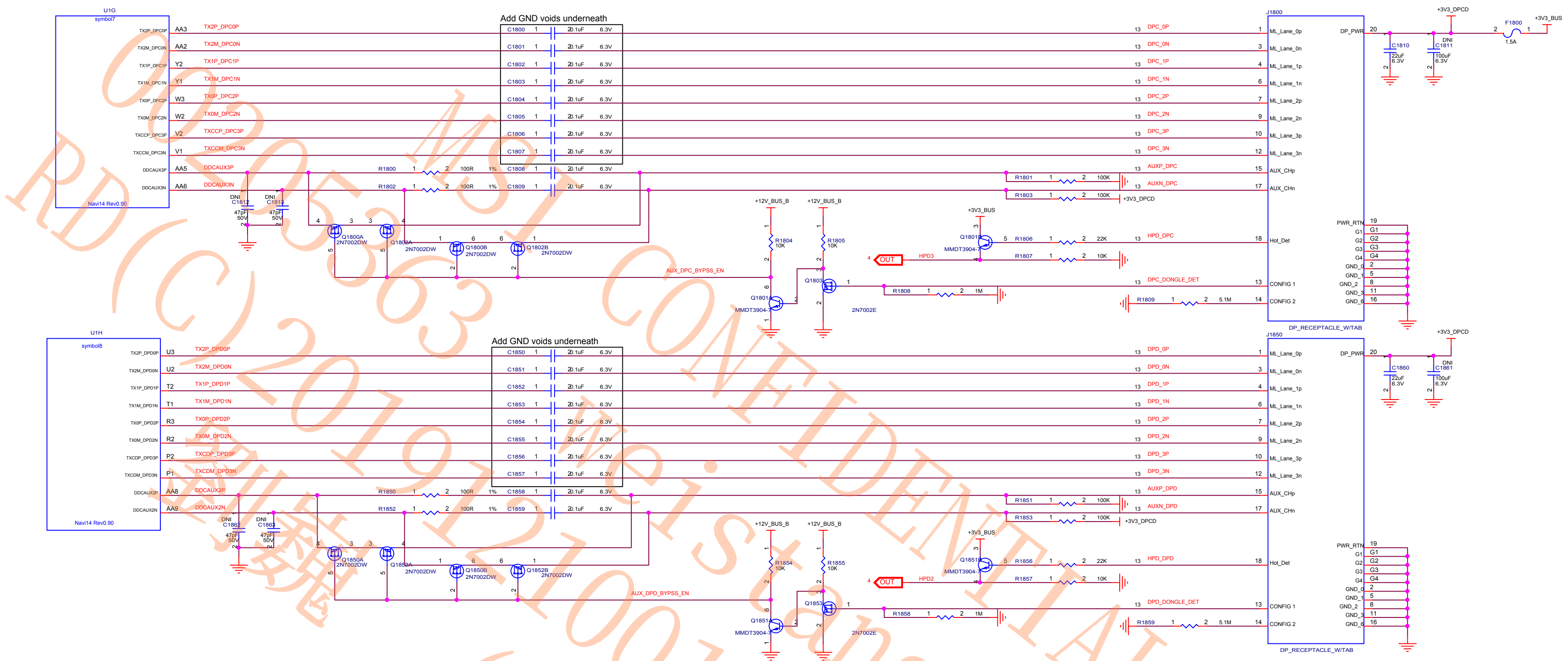
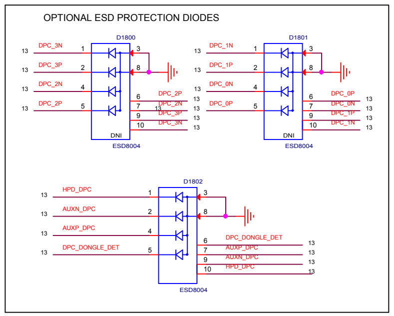
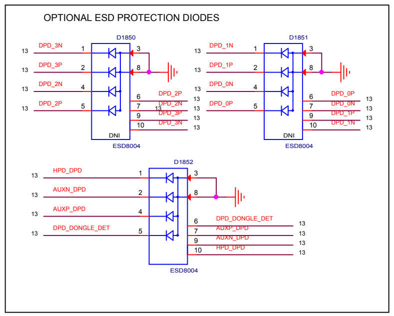
(13) TMDP D/E







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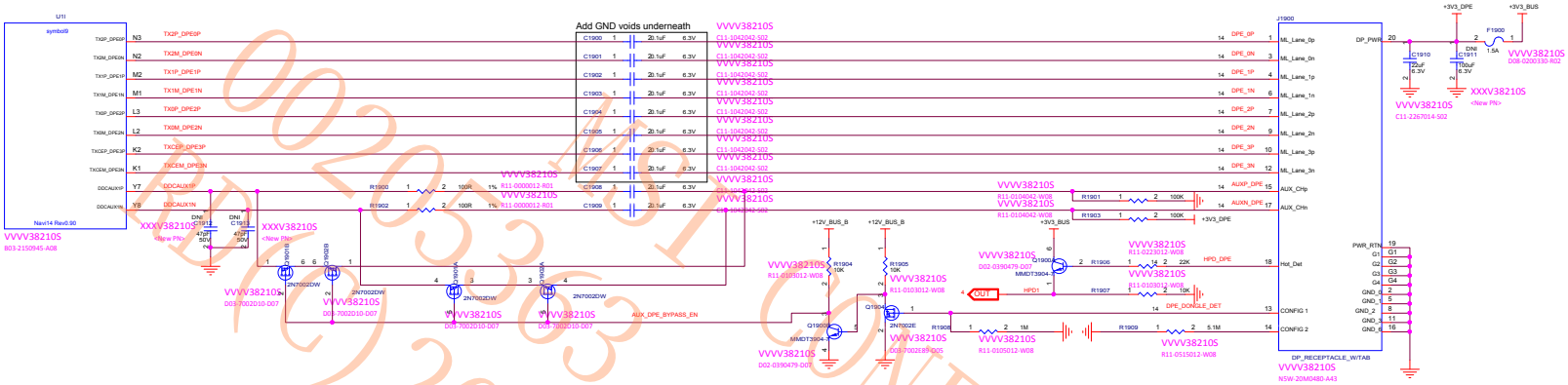

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(20)20191210001 weistang(唐浩健)
(30001789) RMA工程課
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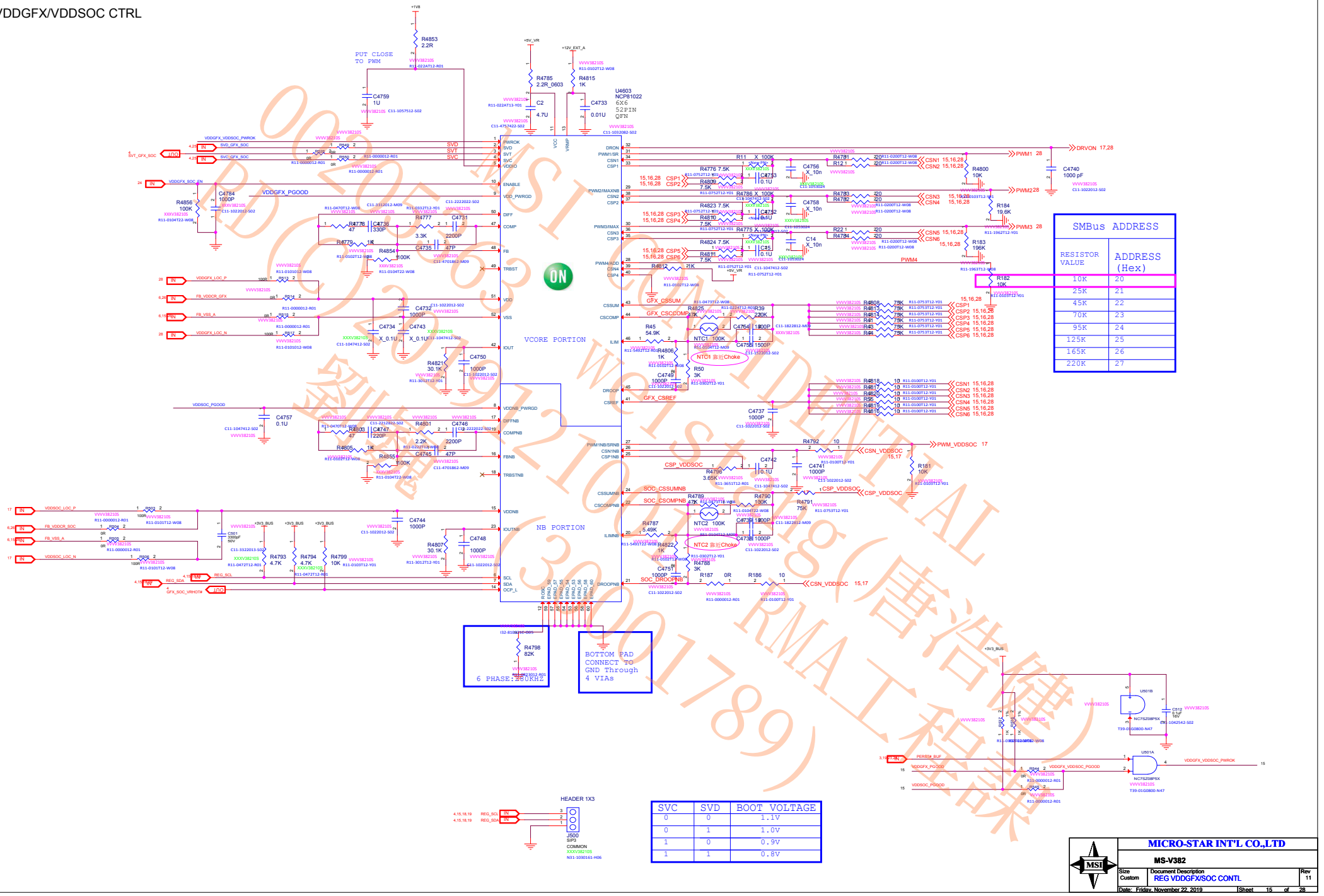
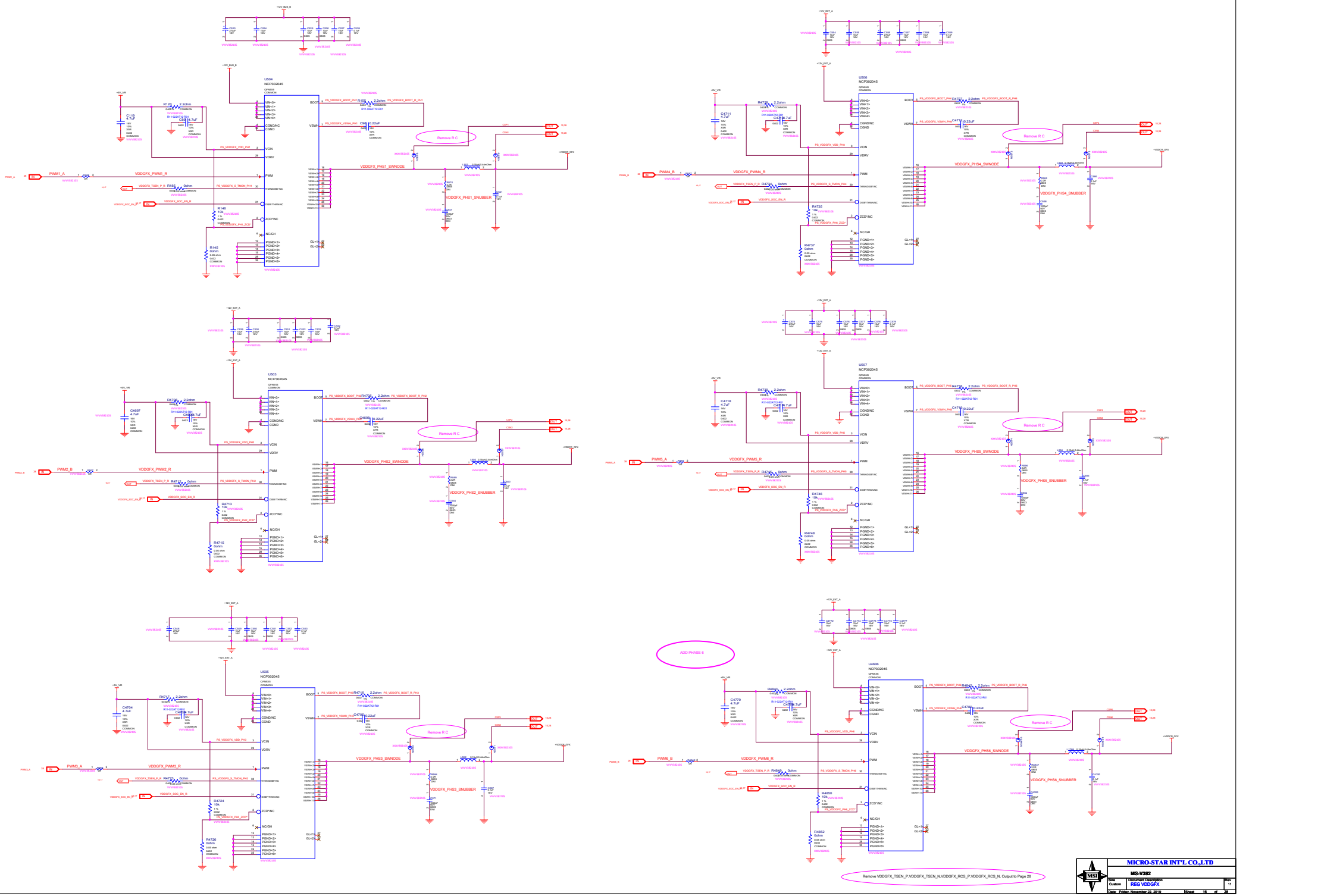
REG - VDDGFX/VDDSOC CTRL





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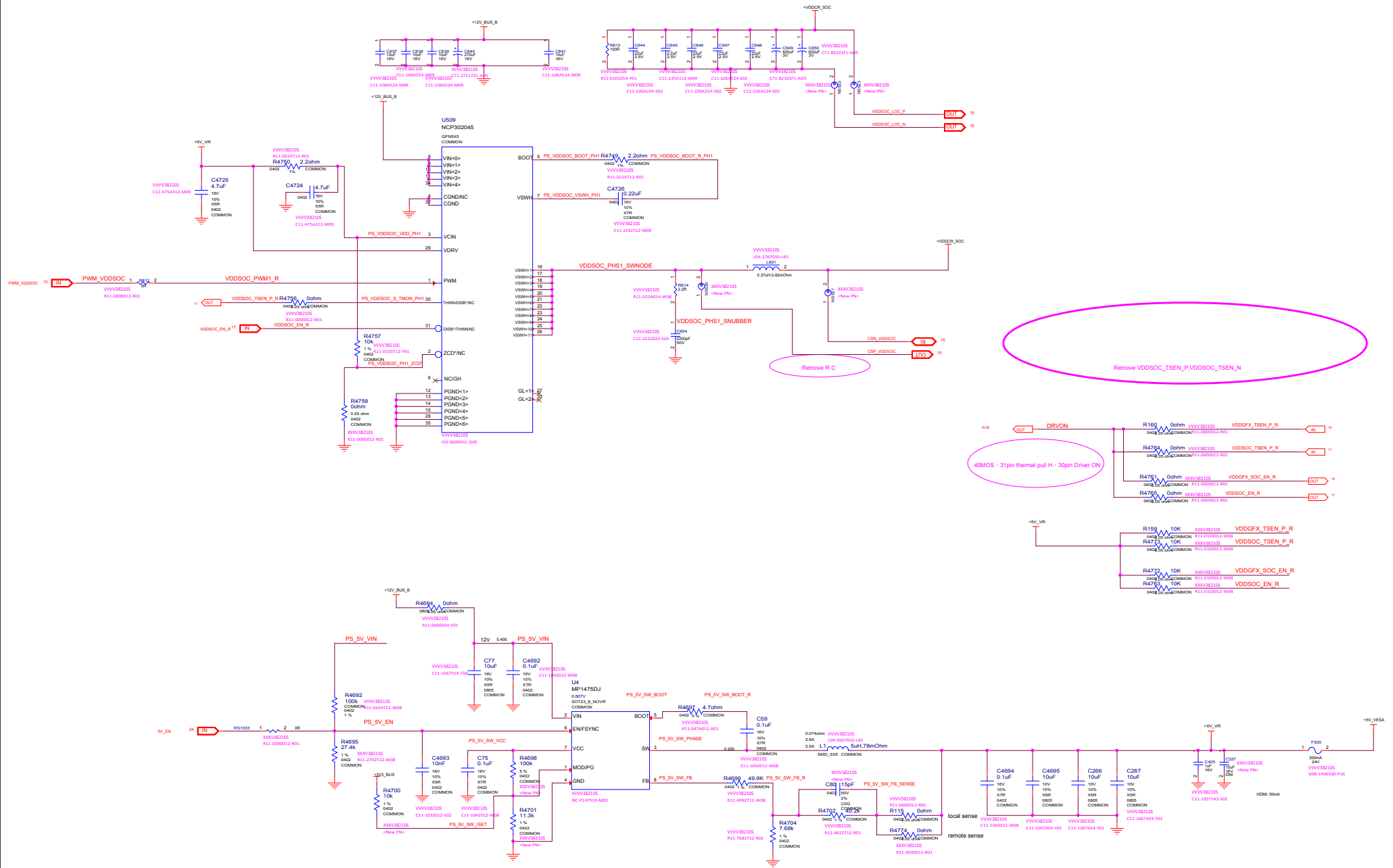
REG: VDDSOC



0.8V*(1+40.2K/7.68K)=4.9875V

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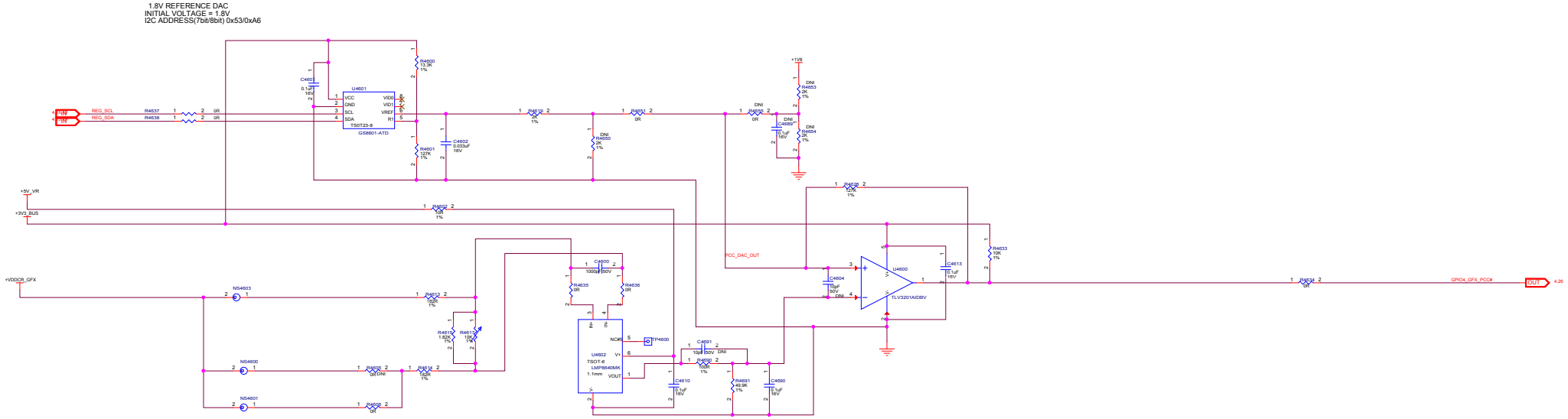
PCC



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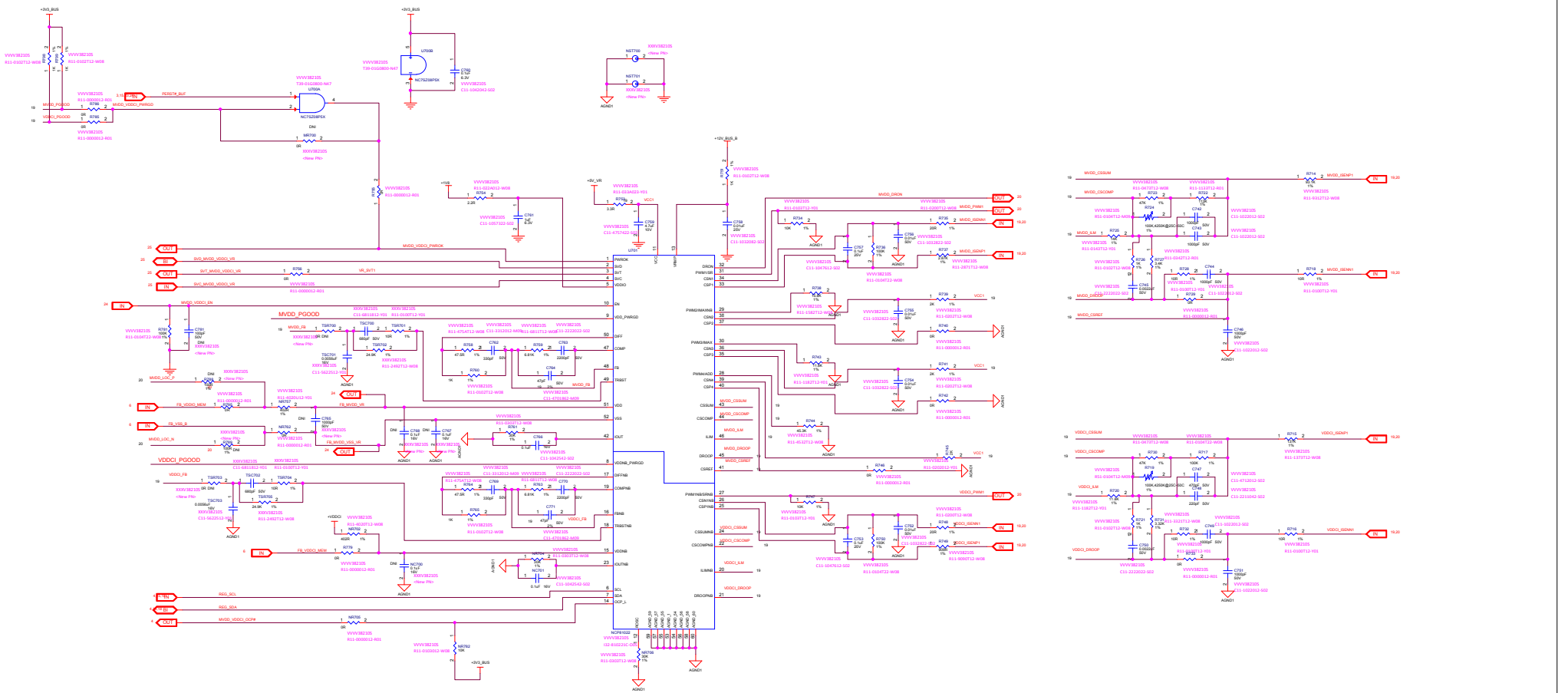
REG - MVDD/VDDCI CTRL



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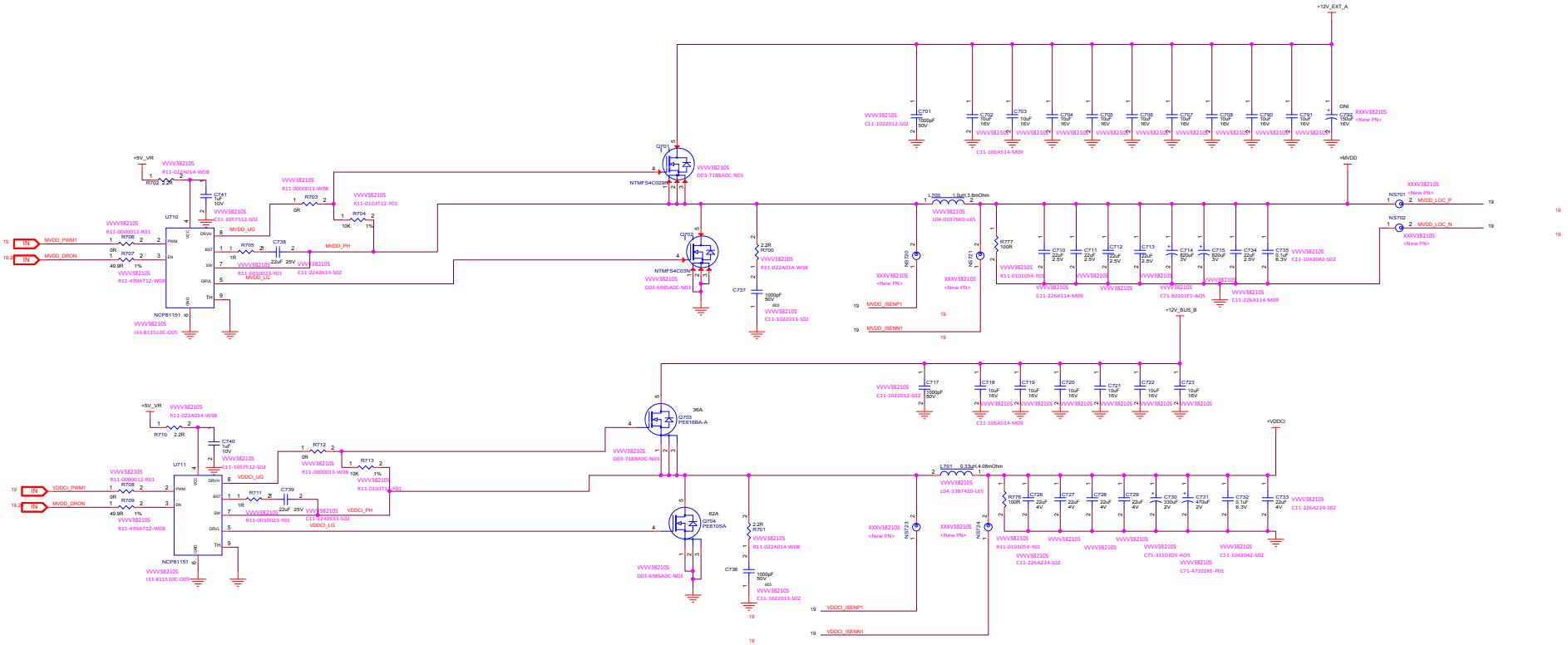
REG - MVDD/VDDCI



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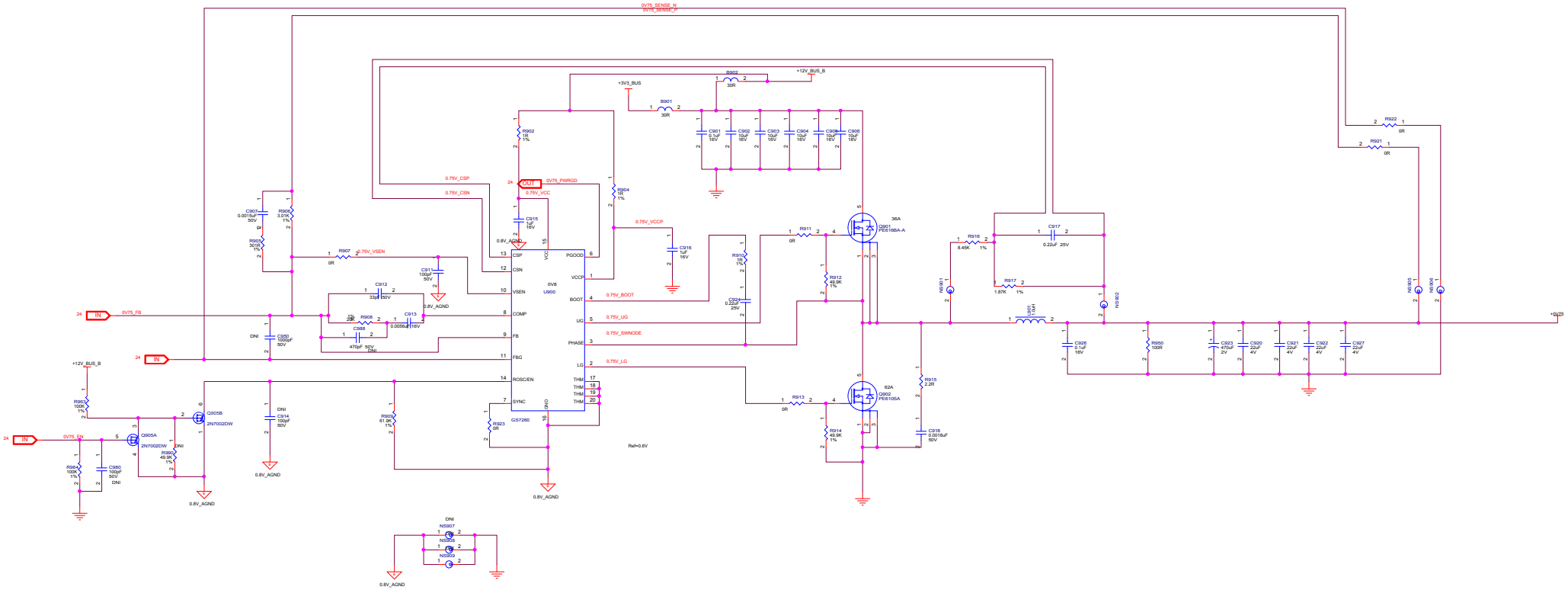
REG - 0.75V



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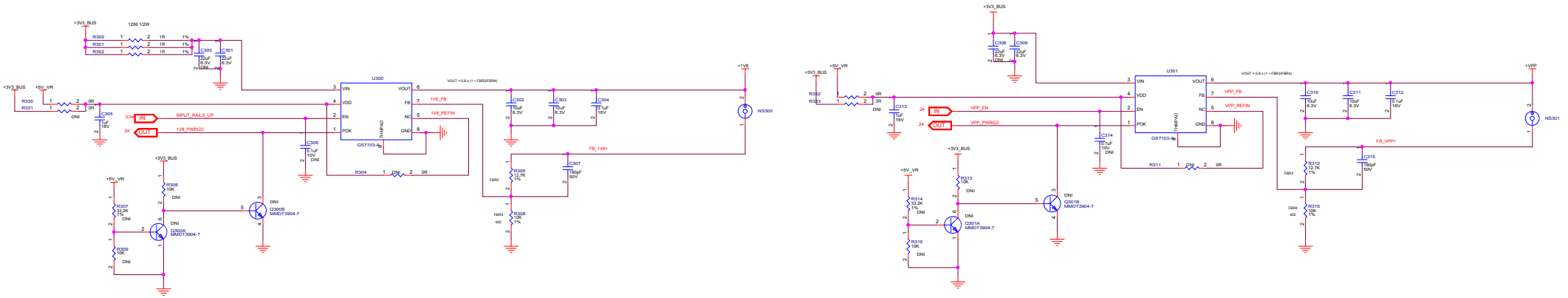
LDO - 1V8/VPP/5V



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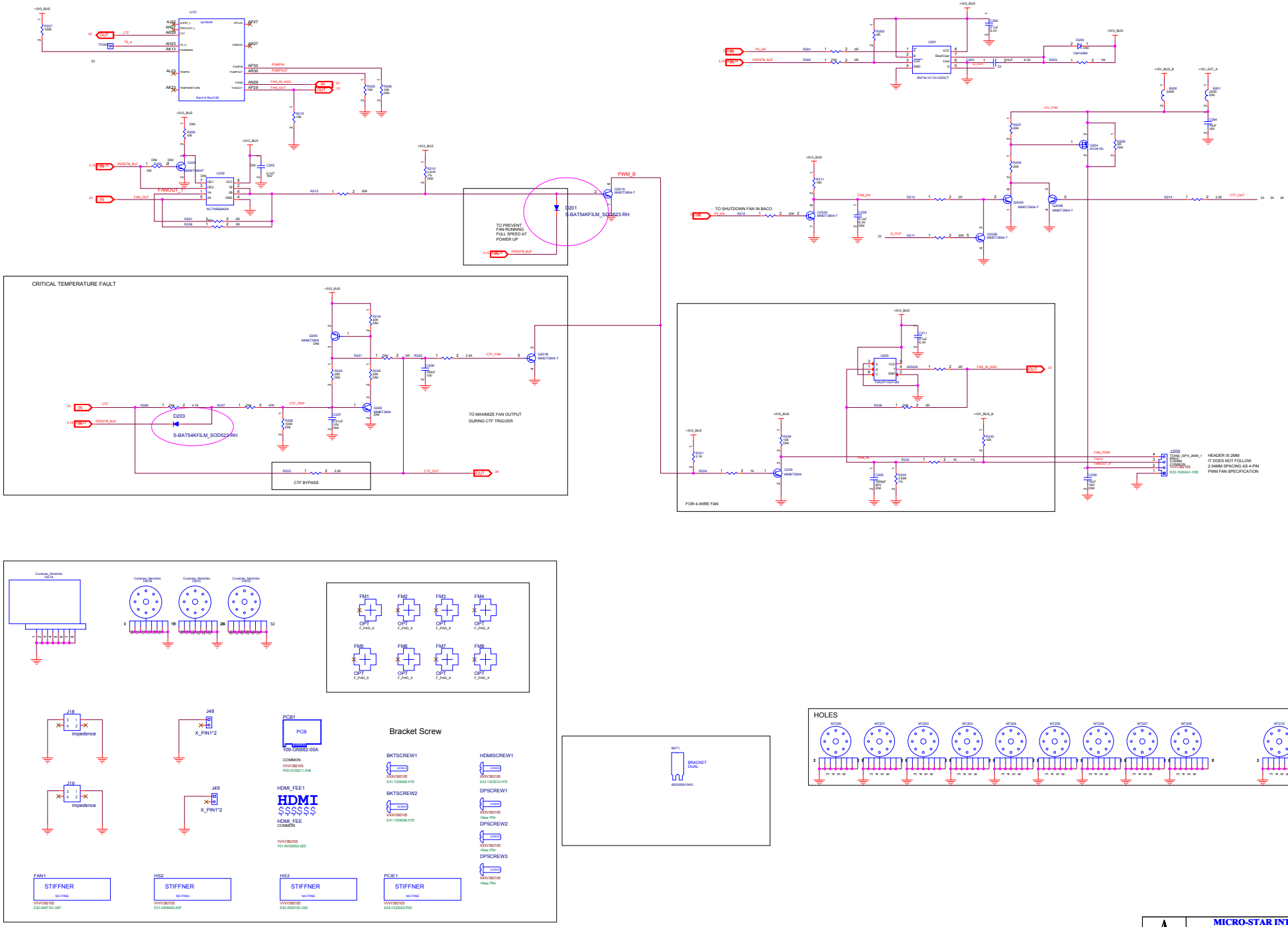

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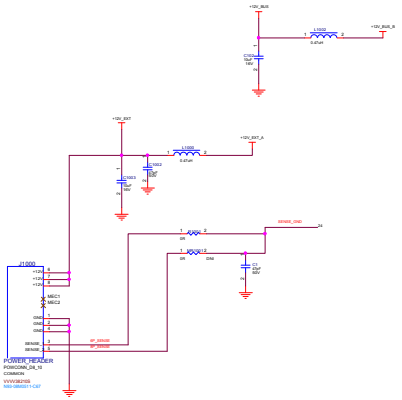
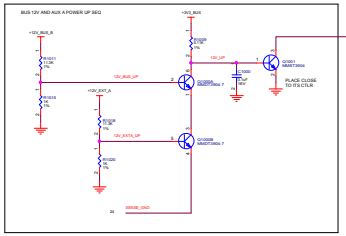
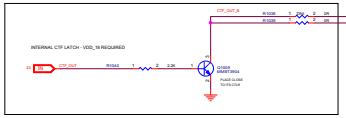
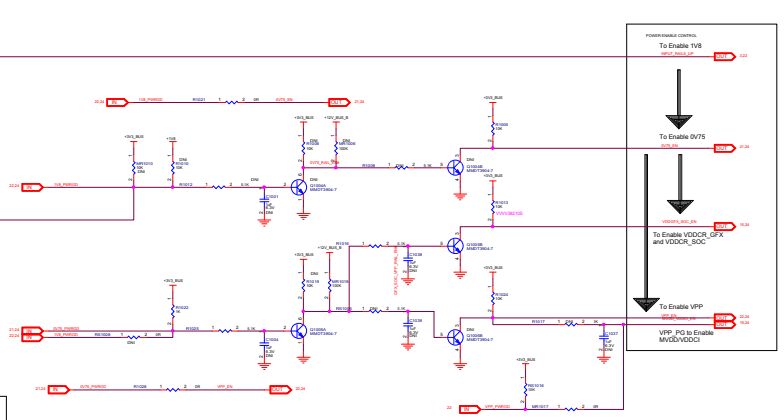
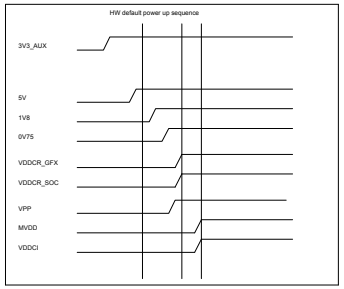
(27) POWER MANAGEMENT

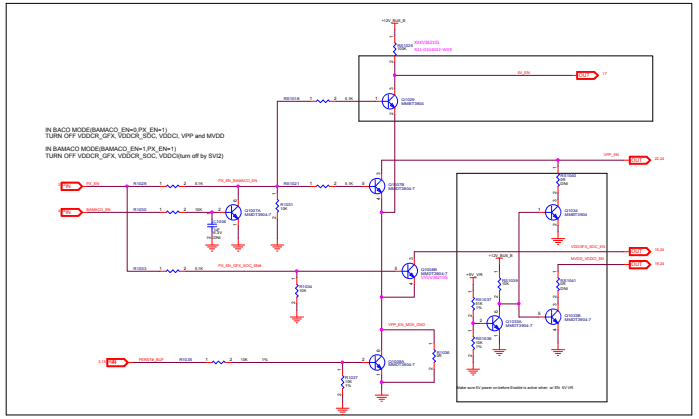


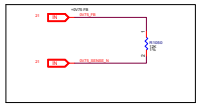


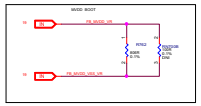












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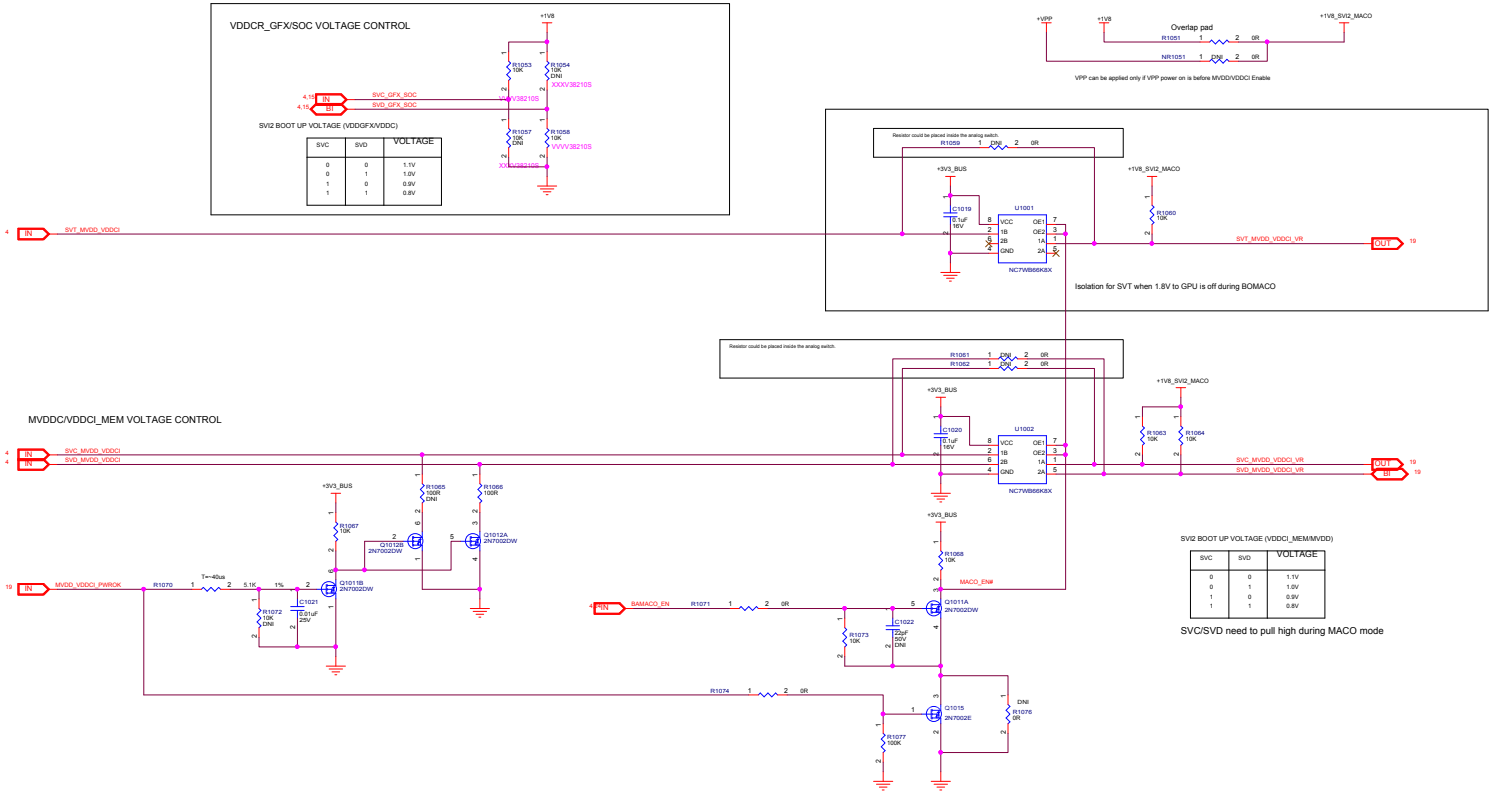
(28) SVI2



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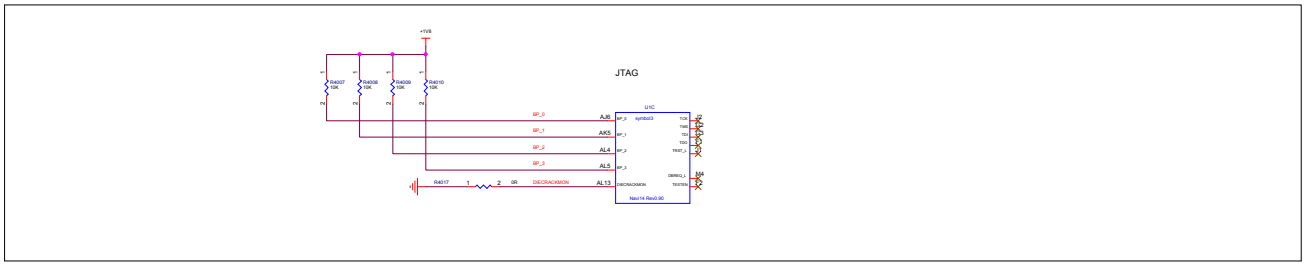
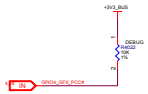
(29) DEBUG CIRCUIT





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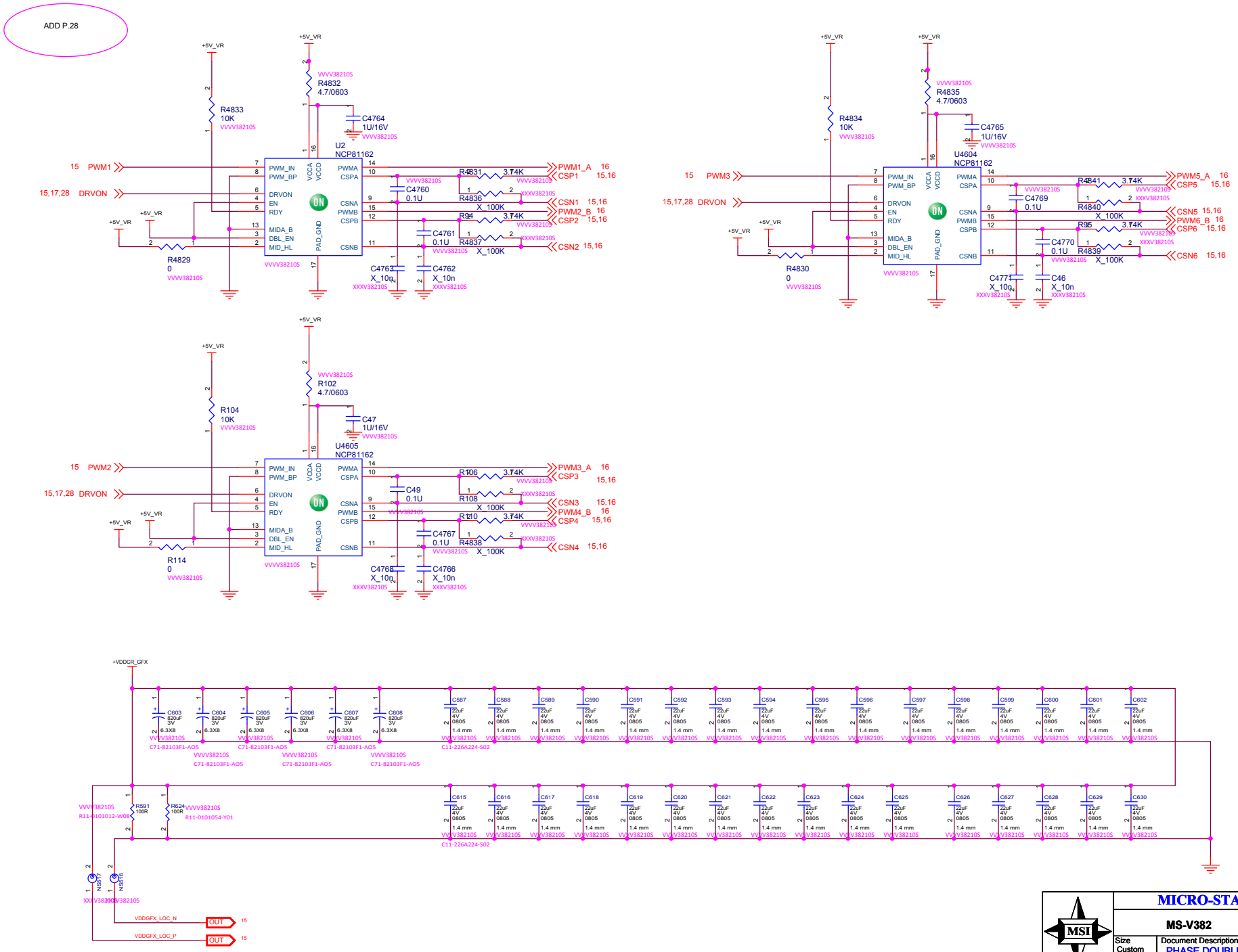
REVISION HISTORY

1.00	00A	08/09/2018	Initial schematic	
		12/28/2018	change all 4172010501G parts to 4172010500G	
1.00	00B	04/16/2019	ADD D1752 D1802 D1852 D1952	
			ADD R795 AND CHANGE MVDD LOCAL SENSE PONIT	
			ADD R1092 R1093 MR1092 MR1093 and reassign gfx phase1-3 input source	
			ADD R4653 R4654 R4655 C4689	
			Change 701: 0.33uH/5260116000G R749: 909R/3160909000G NR704:30K/3160300200G R743: 18K/3160180200G C747:470pF/4170047100G C748:220pF/4	170022100G

2019/11/8 .V382 1 0 -.V382 1 1 Change Vdd cGFX Vdd SOC PWM IR35217 -VON NCP81022N


ADD P.28
+5V_VR
R4833
10K
VVVV38210S
R4832
4.7/0603
C4764
1U/16V
U2
NCP81162
15 PWM1
15,17,28 DRVON
PWM_IN
PWM_BP
DRVON
EN
RDY
MIDA_B
DBL_EN
MID_HL
VCCA
VCCD
PWMA
CSPA
CSNA
PWMB
CSPB
CSNB
PAD_GND
R4829
0
C4760
0.1U
C4761
0.1U
C4763
X_10n
C4762
X_10n
R4831
3.74K
R4836
X_100K
R4834
R4837
X_100K
PWM1_A 16
CSP1 15,16
CSN1 15,16
PWM2_B 16
CSP2 15,16
CSN2 15,16
R4834
10K
R4835
4.7/0603
C4765
1U/16V
U4604
NCP81162
15 PWM3
15,17,28 DRVON
R4830
0
C4769
0.1U
C4770
0.1U
C4771
X_10n
C46
X_10n
R4841
3.74K
R4840
X_100K
R4839
X_100K
PWM5_A 16
CSP5 15,16
CSN5 15,16
PWM6_B 16
CSP6 15,16
CSN6 15,16
R104
10K
R102
4.7/0603
C47
1U/16V
U4605
NCP81162
15 PWM2
15,17,28 DRVON
R114
0
C49
0.1U
C4767
0.1U
C4768
X_10n
C4766
X_10n
R106
3.74K
R108
X_100K
R110
R4838
X_100K
PWM3_A 16
CSP3 15,16
CSN3 15,16
PWM4_B 16
CSP4 15,16
CSN4 15,16
+VDDCR_GFX
C603 C604 C605 C606 C607 C608
820uF 3V 6.3X8
C71-82103F1-AO5
C587 C588 C589 C590 C591 C592 C593 C594 C595 C596 C597 C598 C599 C600 C601 C602
22uF 4V 0805 1.4 mm
C11-226A224-S02
C615 C616 C617 C618 C619 C620 C621 C622 C623 C624 C625 C626 C627 C628 C629 C630
R691 100R
R624 100R
R11-0101012-W08
R11-0101054-Y01
NSN7
NSN8
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