P672: GT215-128bit, 32Mx32 GDDR5

DL-DVI, VGA, HDMI

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10672-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10672-0001-100	GT215-450, 550/1175MHz 512MB 32Mx16 BGA170 1800MHz GDDR5 DVI-I/VGA/HDMI
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TABLE OF CONTENTS

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PEX x16 INTERFACE

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS

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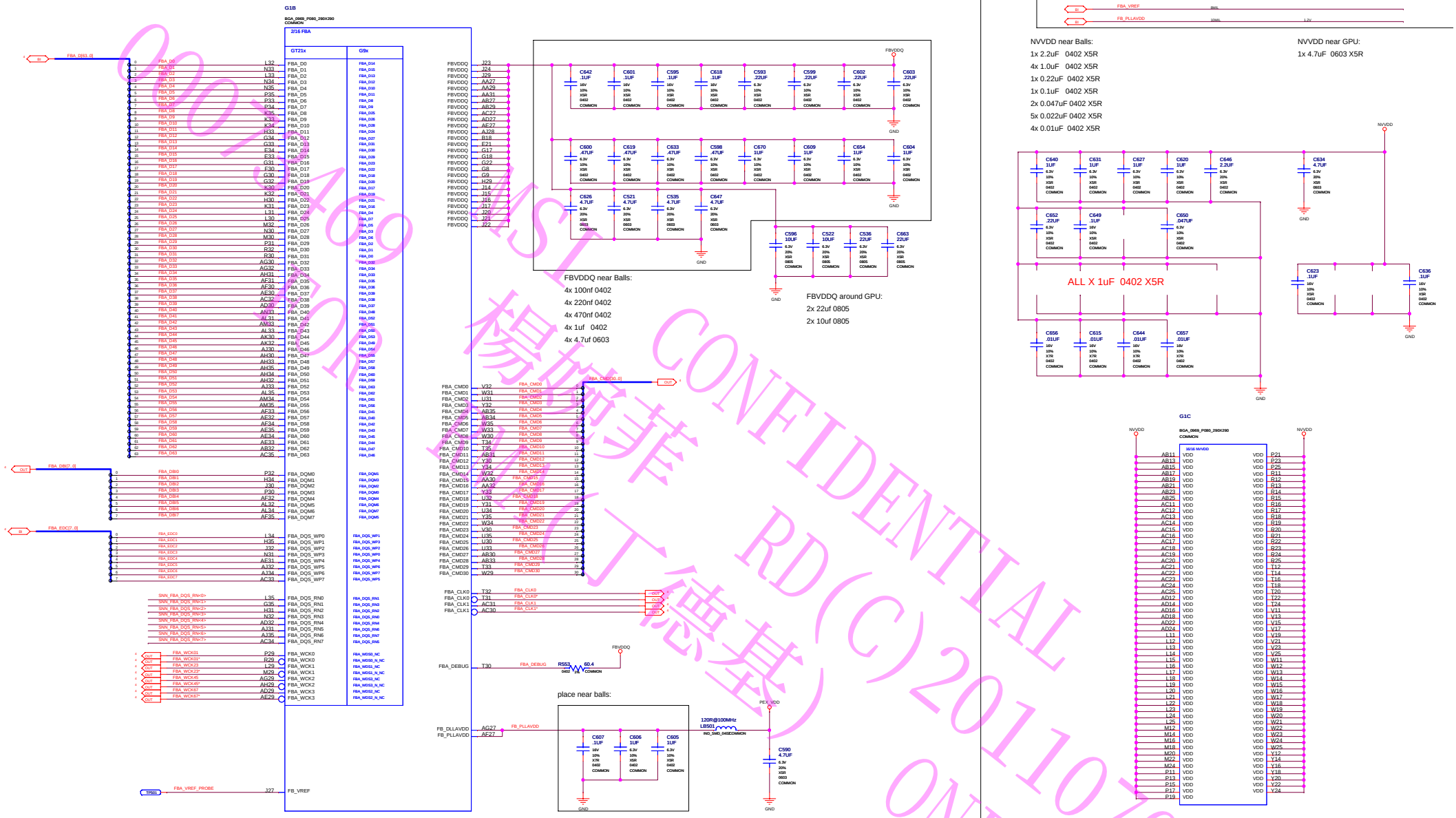
MEMORY Partition A - GPU, FBVDD/Q & NVVDD DECOUPLING



NET	MIN_LINE_WIDTH	VOLTAGE
FBA_VREF	8MIL	
FB_PLLAVDD	10MIL	1.2V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY INTERFACE, GPU NVVDD & FBVDDQ DECOUPLING CAPS

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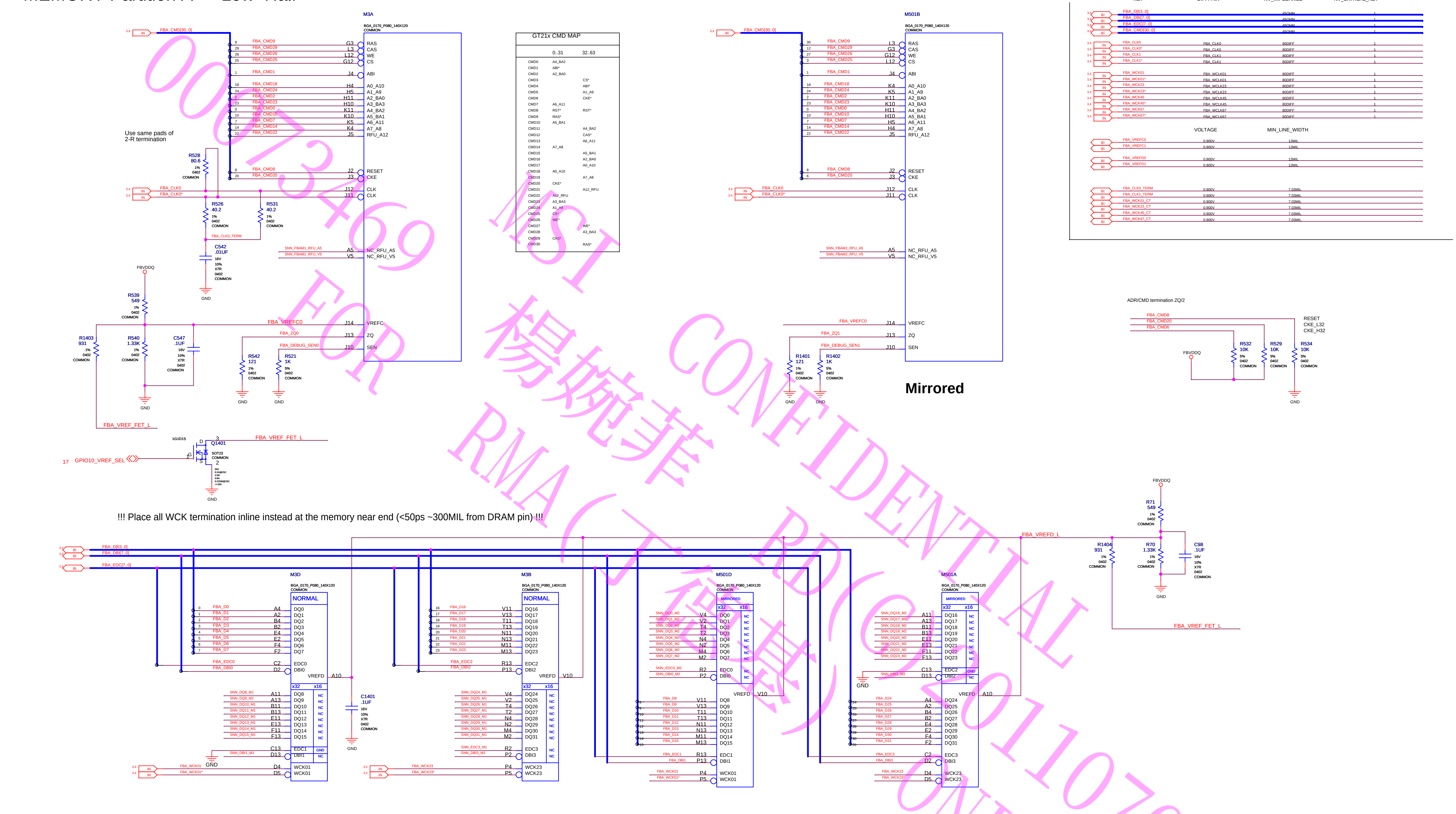
MEMORY Partition A --- Low Half



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 32Mx32 GDDR5 MEMORIES, FBA CLK TERMS

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MEMORY Partition A - Decoupling

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

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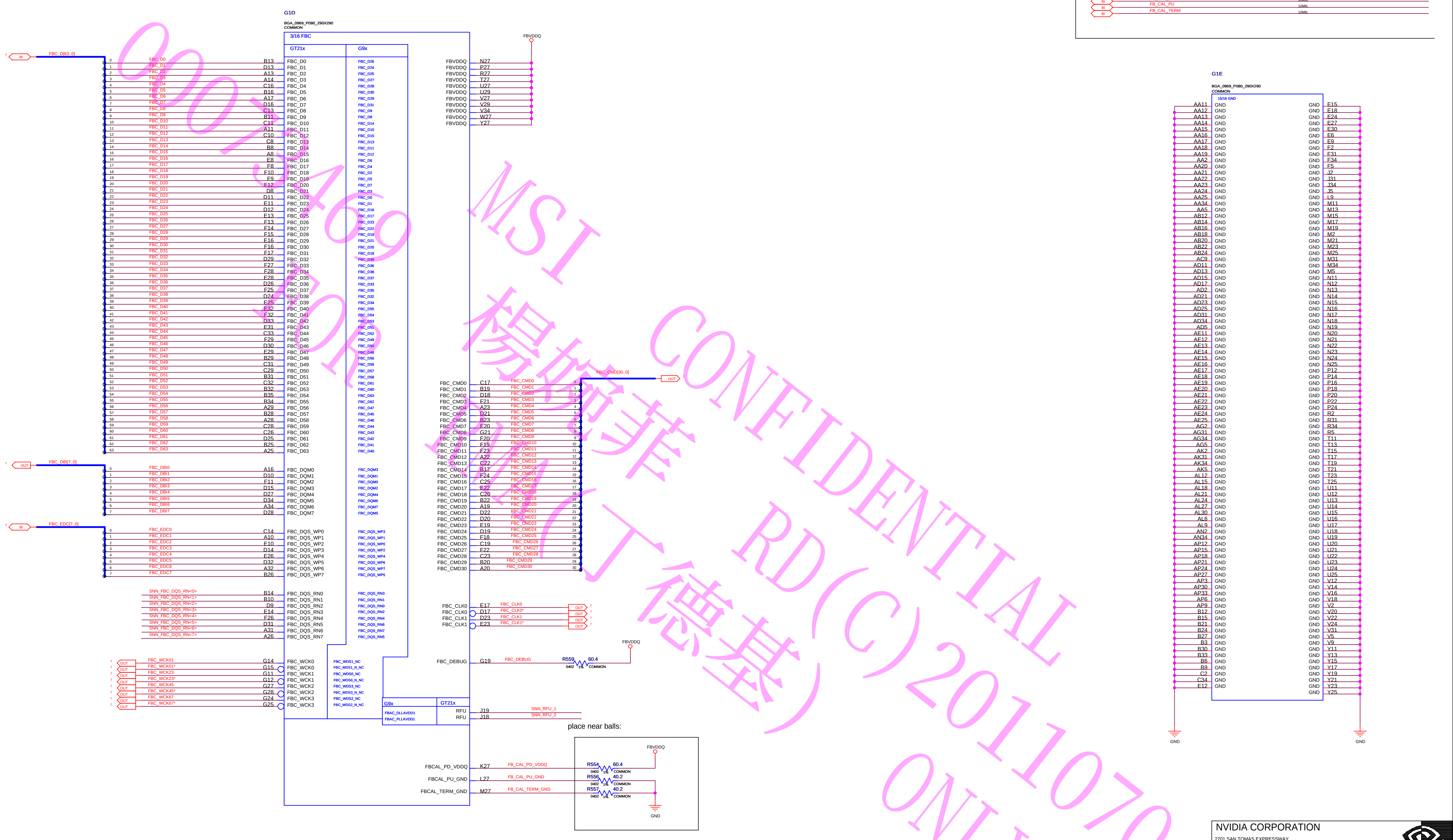
MEMORY Partition C - GPU



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY INTERFACE

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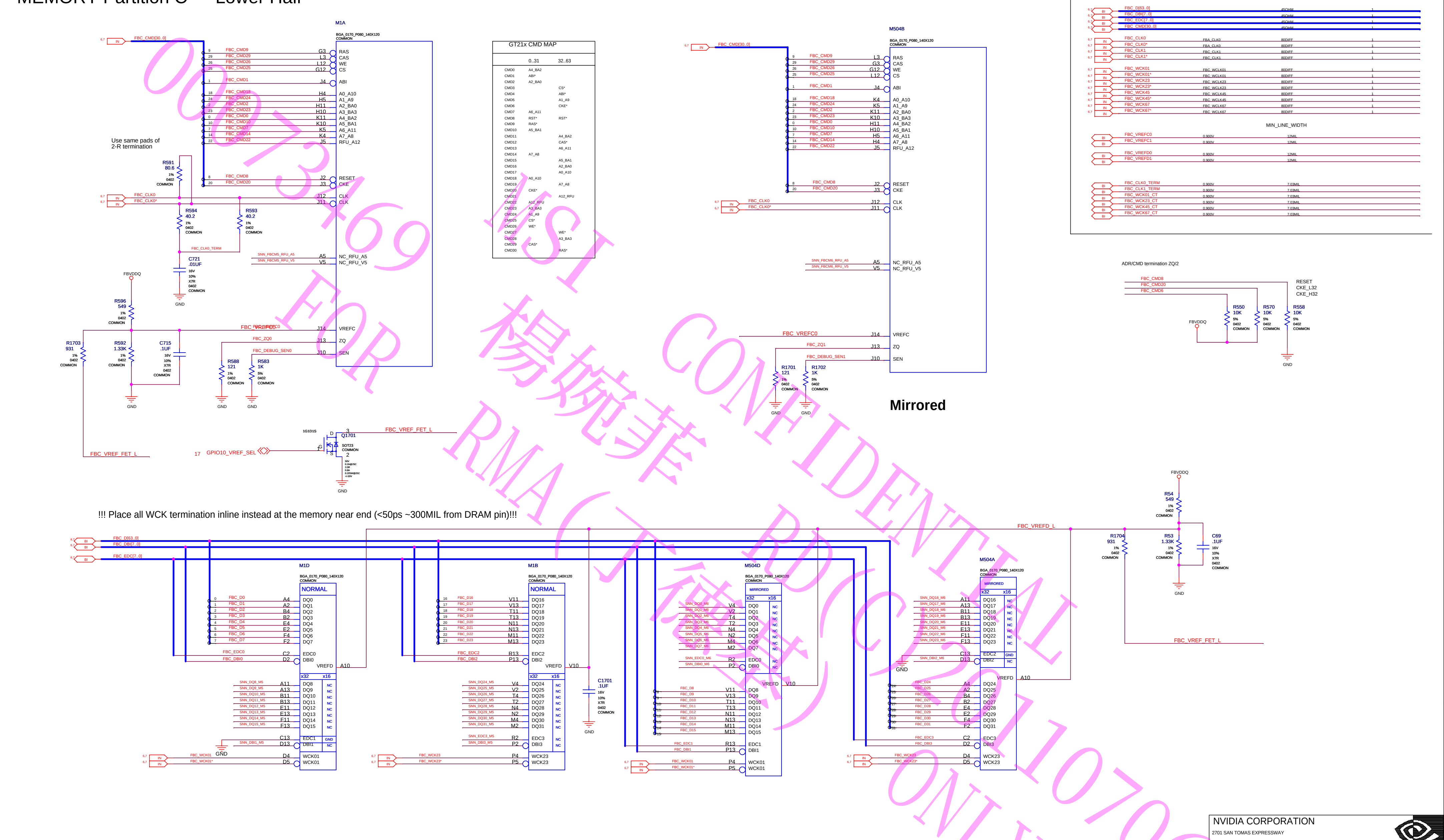
MEMORY Partition C --- Lower Half



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 32MX32 GDDR5 MEMORIES, FBC CLK TERMS

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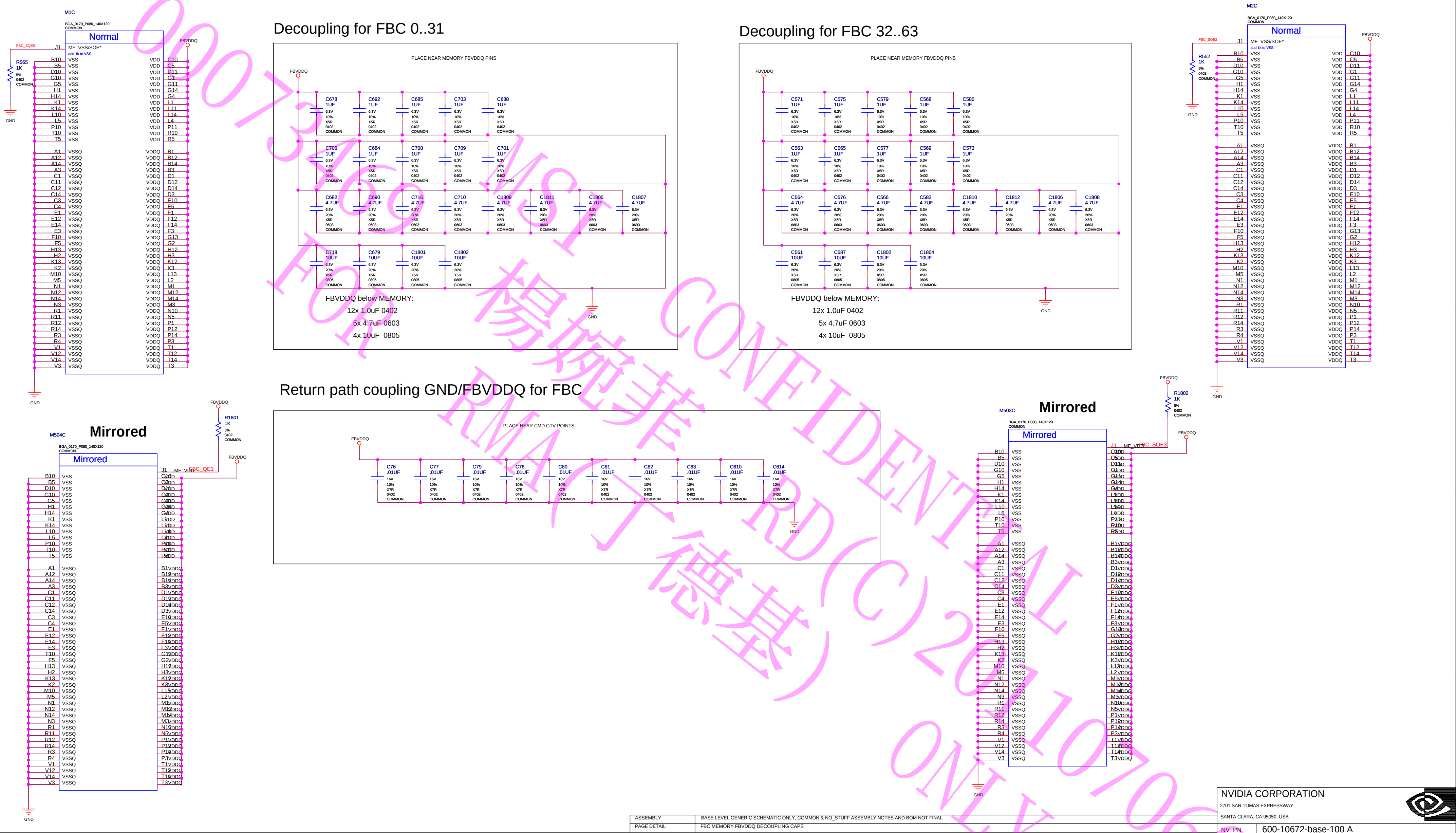
MEMORY PARTITION C DECOUPLING



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS

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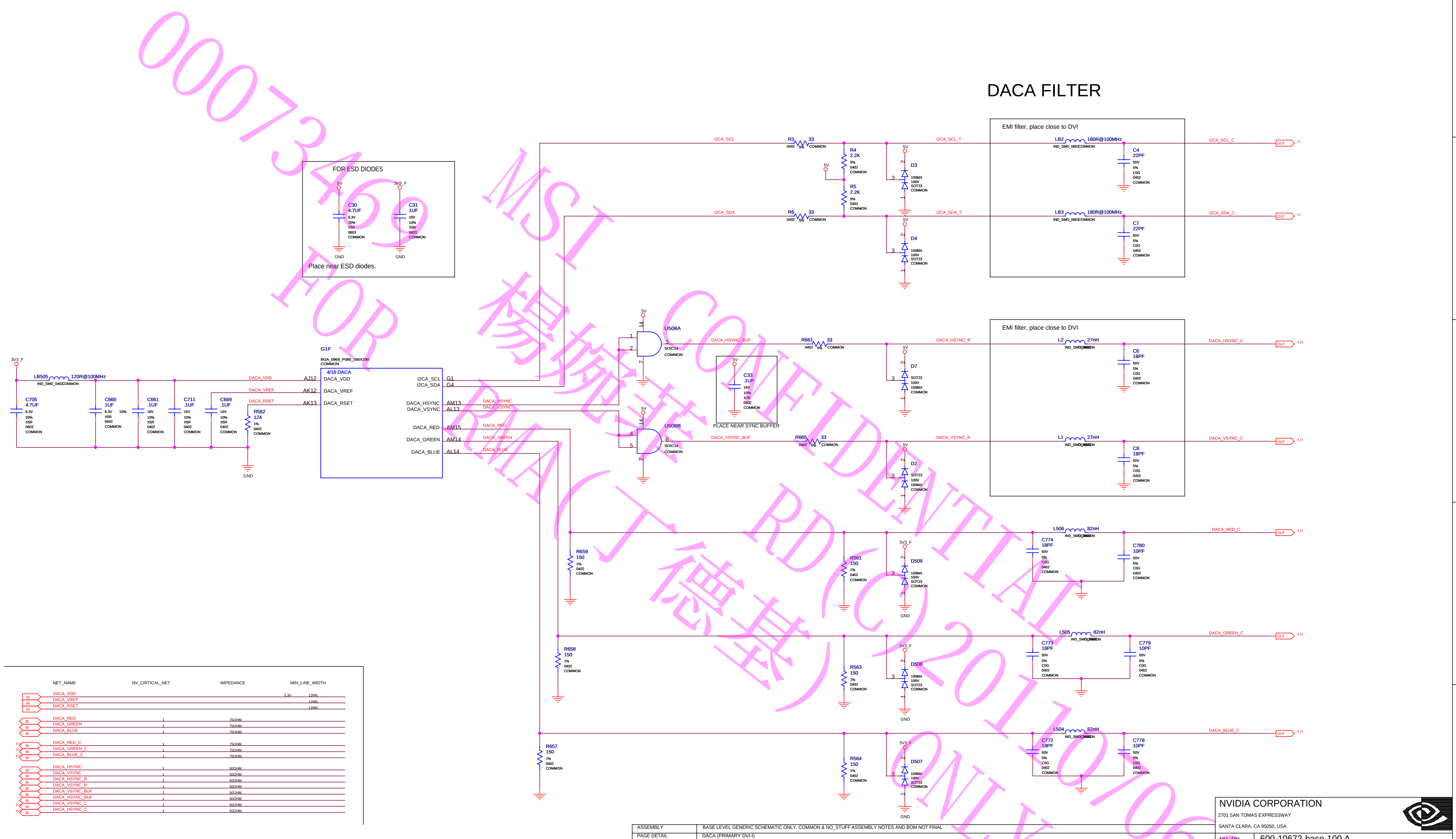
Primary Display (DACA), DVI-I (South)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA (PRIMARY DVI-I)

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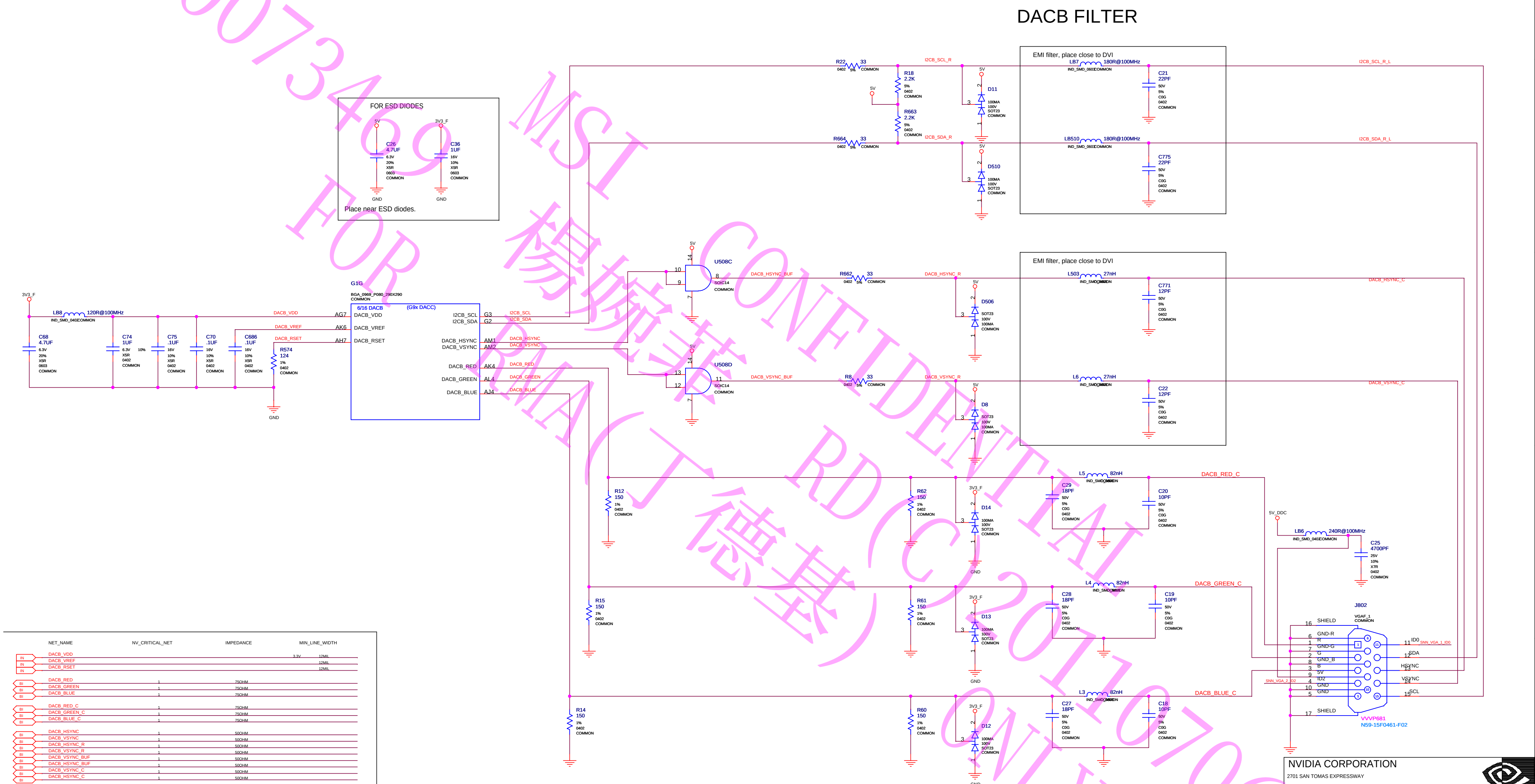
Secondary Display (DACB), VGA (Mid)



NET_NAME		NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
IN	DACB_VDD			3.3V 12MIL
IN	DACB_VREF			12MIL
IN	DACB_RSET			12MIL
BI	DACB_RED	1	75OHM	
BI	DACB_GREEN	1	75OHM	
BI	DACB_BLUE	1	75OHM	
BI	DACB_RED_C	1	75OHM	
BI	DACB_GREEN_C	1	75OHM	
BI	DACB_BLUE_C	1	75OHM	
BI	DACB_HSYNC	1	50OHM	
BI	DACB_VSYNC	1	50OHM	
BI	DACB_HSYNC_R	1	50OHM	
BI	DACB_VSYNC_R	1	50OHM	
BI	DACB_VSYNC_BUF	1	50OHM	
BI	DACB_HSYNC_BUF	1	50OHM	
BI	DACB_VSYNC_C	1	50OHM	
BI	DACB_HSYNC_C	1	50OHM	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB (SECONDARY VGA)

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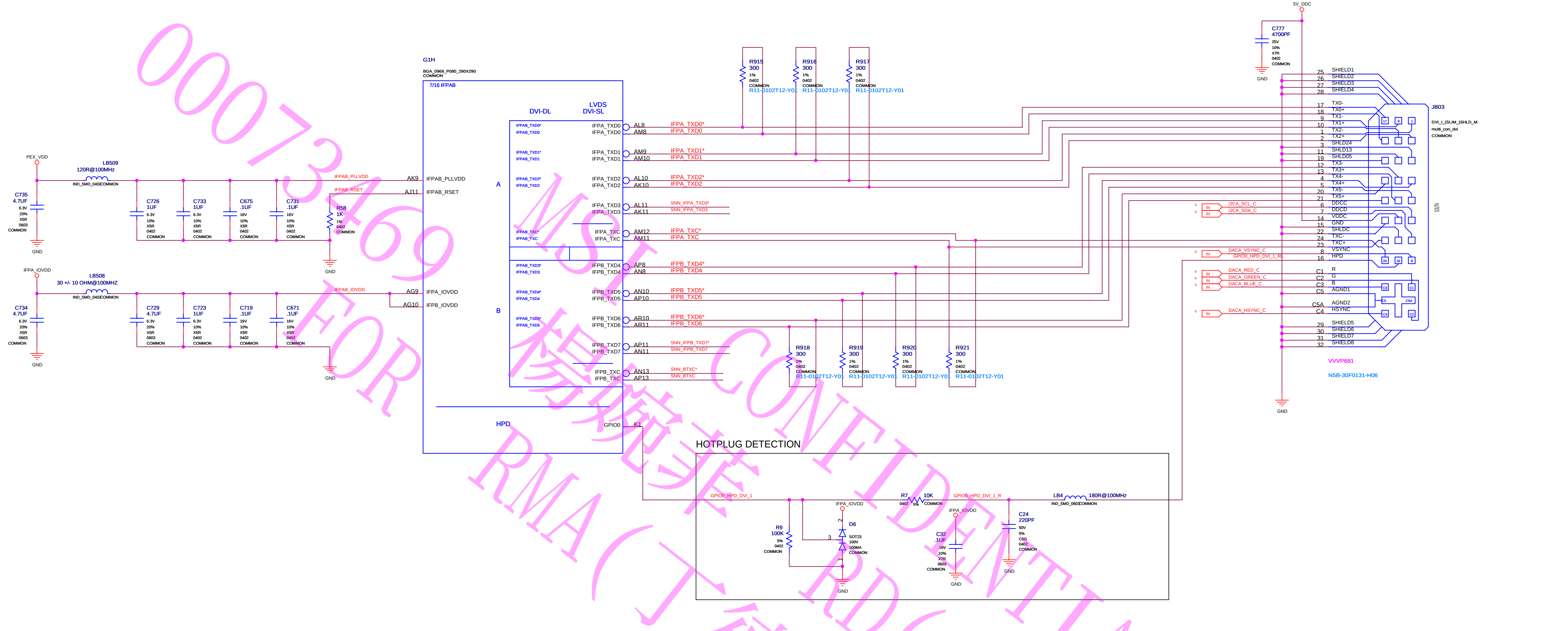
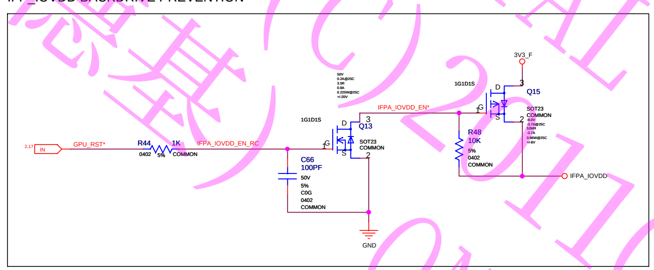
LINK A/B: TMDS, Primary DVI-I DL (South)



IFP_IOVDD BACKDRIVE PREVENTION



NETNAME	DIFF PAIR NAME	NV_CRITICAL_NET	NV_IMPEDANCE
IFPA_TXC*	IFPA_TXC	1	90DIFF
IFPA_TXC	IFPA_TXC	1	90DIFF
IFPA_TXD0*	IFPA_TXD0	1	90DIFF
IFPA_TXD0	IFPA_TXD0	1	90DIFF
IFPA_TXD1*	IFPA_TXD1	1	90DIFF
IFPA_TXD1	IFPA_TXD1	1	90DIFF
IFPA_TXD2*	IFPA_TXD2	1	90DIFF
IFPA_TXD2	IFPA_TXD2	1	90DIFF
IFPB_TXD4*	IFPB_TXD4	1	90DIFF
IFPB_TXD4	IFPB_TXD4	1	90DIFF
IFPB_TXD5*	IFPB_TXD5	1	90DIFF
IFPB_TXD5	IFPB_TXD5	1	90DIFF
IFPB_TXD6*	IFPB_TXD6	1	90DIFF
IFPB_TXD6	IFPB_TXD6	1	90DIFF
IFPAB_PLLVDD		12MIL	1.05V
IFPAB_IOVDD		12MIL	3.3V
IFPAB_RSET		12MIL	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK A/B: DVI-I (SOUTH)

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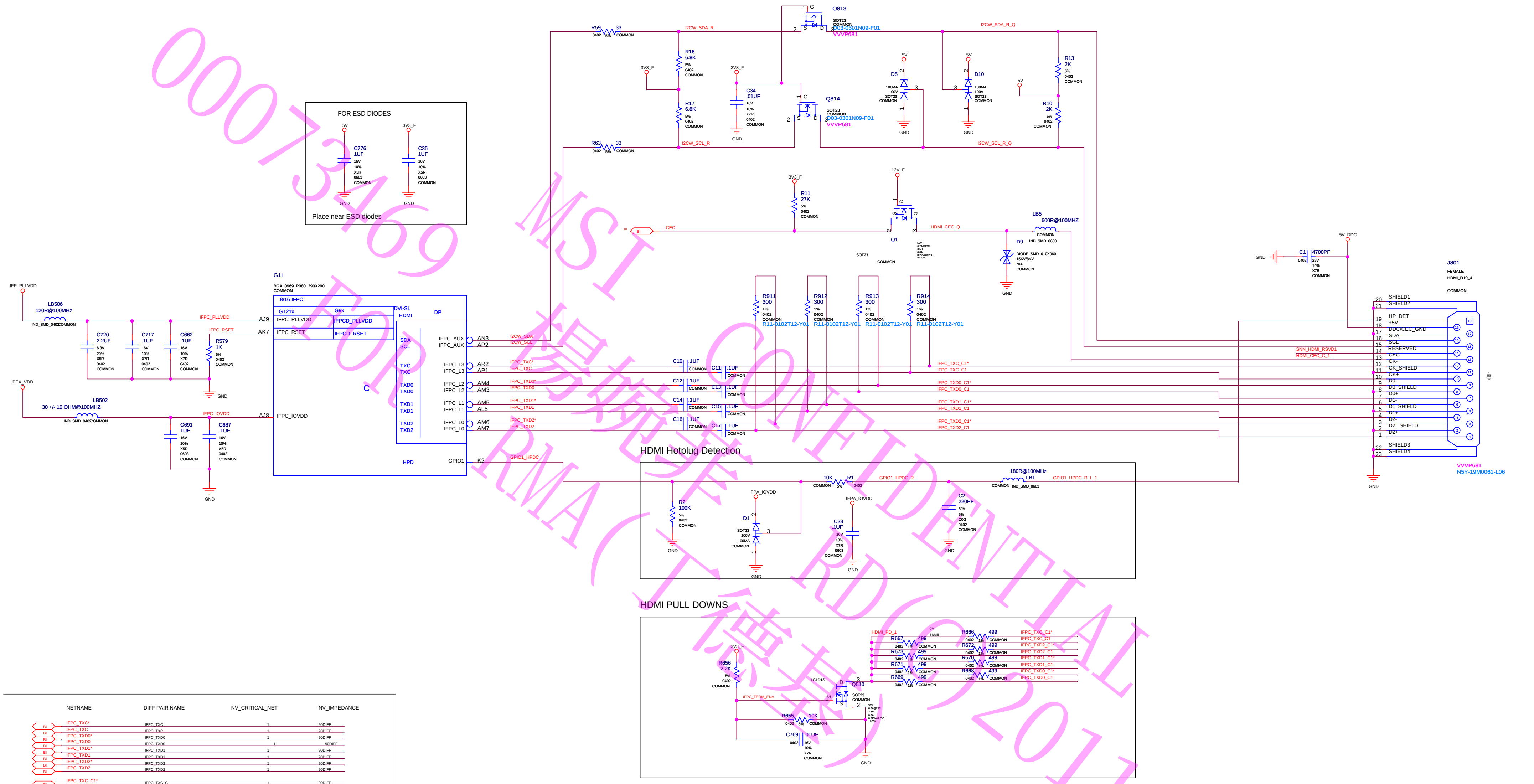
LINK C: HDMI (North)



NETNAME	DIFF PAIR NAME	NV_CRITICAL_NET	NV_IMPEDANCE
IFPC_TXC*	IFPC_TXC	1	90DIFF
IFPC_TXC	IFPC_TXC	1	90DIFF
IFPC_TXD0*	IFPC_TXD0	1	90DIFF
IFPC_TXD0	IFPC_TXD0	1	90DIFF
IFPC_TXD1*	IFPC_TXD1	1	90DIFF
IFPC_TXD1	IFPC_TXD1	1	90DIFF
IFPC_TXD2*	IFPC_TXD2	1	90DIFF
IFPC_TXD2	IFPC_TXD2	1	90DIFF
IFPC_TXC_C1*	IFPC_TXC_C1	1	90DIFF
IFPC_TXC_C1	IFPC_TXC_C1	1	90DIFF
IFPC_TXD0_C1*	IFPC_TXD0_C1	1	90DIFF
IFPC_TXD0_C1	IFPC_TXD0_C1	1	90DIFF
IFPC_TXD1_C1*	IFPC_TXD1_C1	1	90DIFF
IFPC_TXD1_C1	IFPC_TXD1_C1	1	90DIFF
IFPC_TXD2_C1*	IFPC_TXD2_C1	1	90DIFF
IFPC_TXD2_C1	IFPC_TXD2_C1	1	90DIFF

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
IFPC_IOVDD	12MIL	1.05V	0.15A
IFPC_RSET	12MIL		

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK C: HDMI (NORTH)

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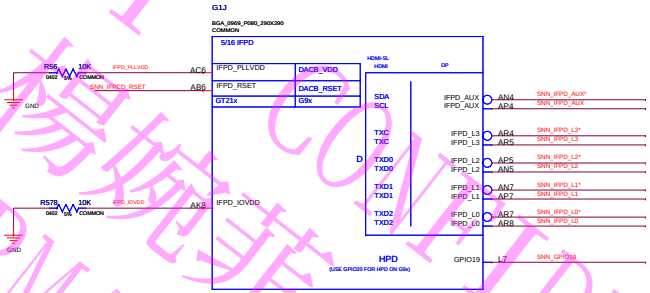
LINK D: UNUSED



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK D (UNUSED)

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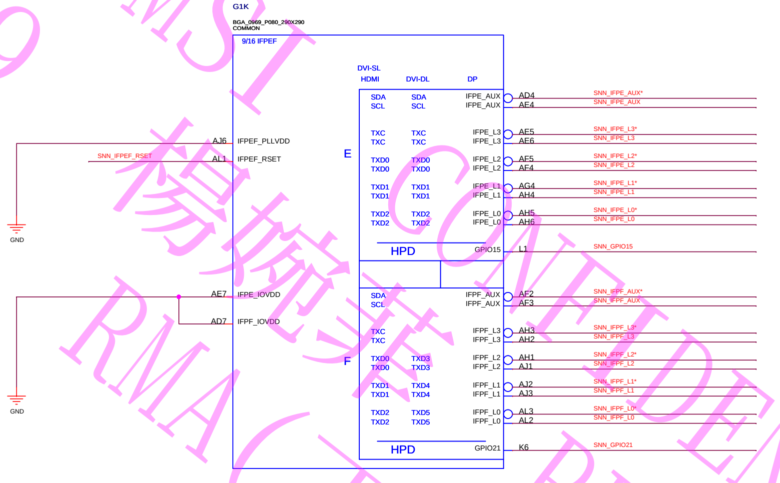
LINK E/F: (UNUSED)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK E/F: (UNUSED)

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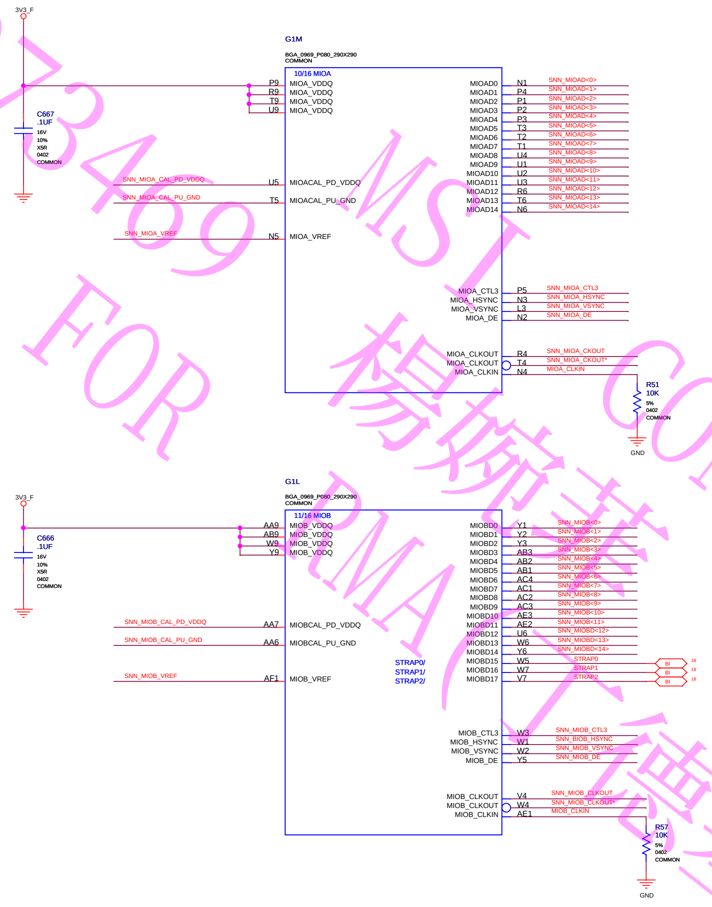
MIOA/B UNUSED



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB (UNUSED)

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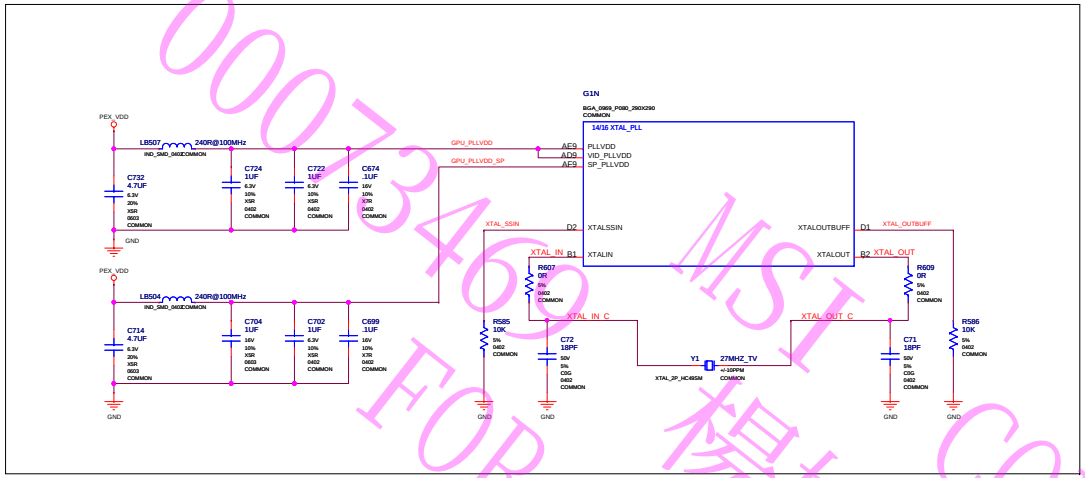
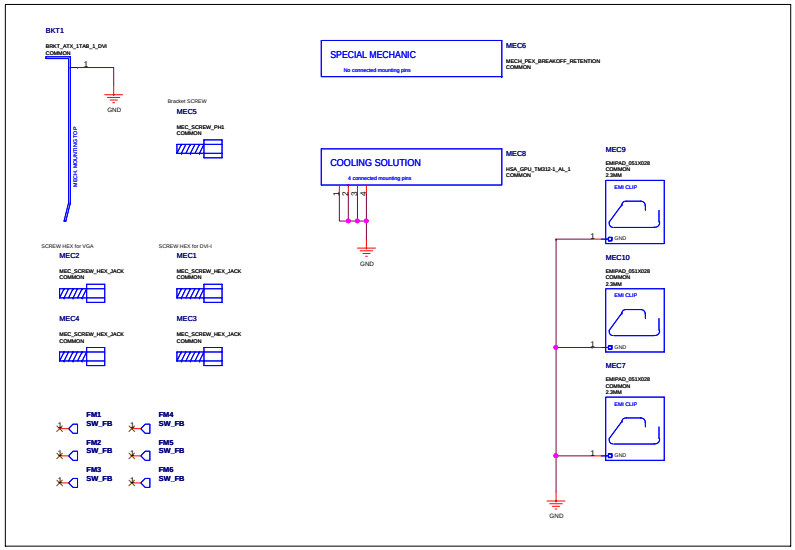
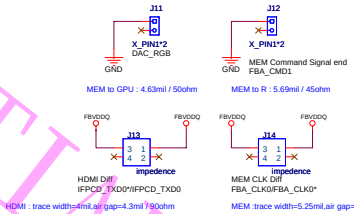
XTAL, MECHANICALS

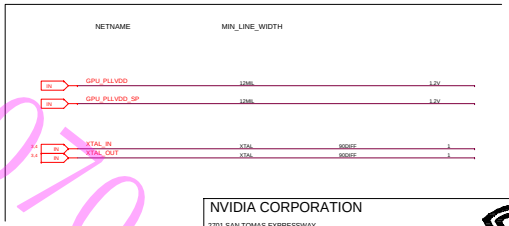
XTAL/GPU_PLLVDD



MECHANICALS & THERMALS







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, MECHANICALS, THERMALS

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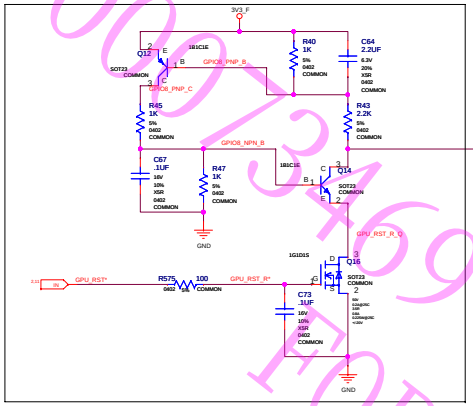
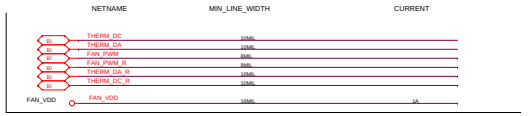
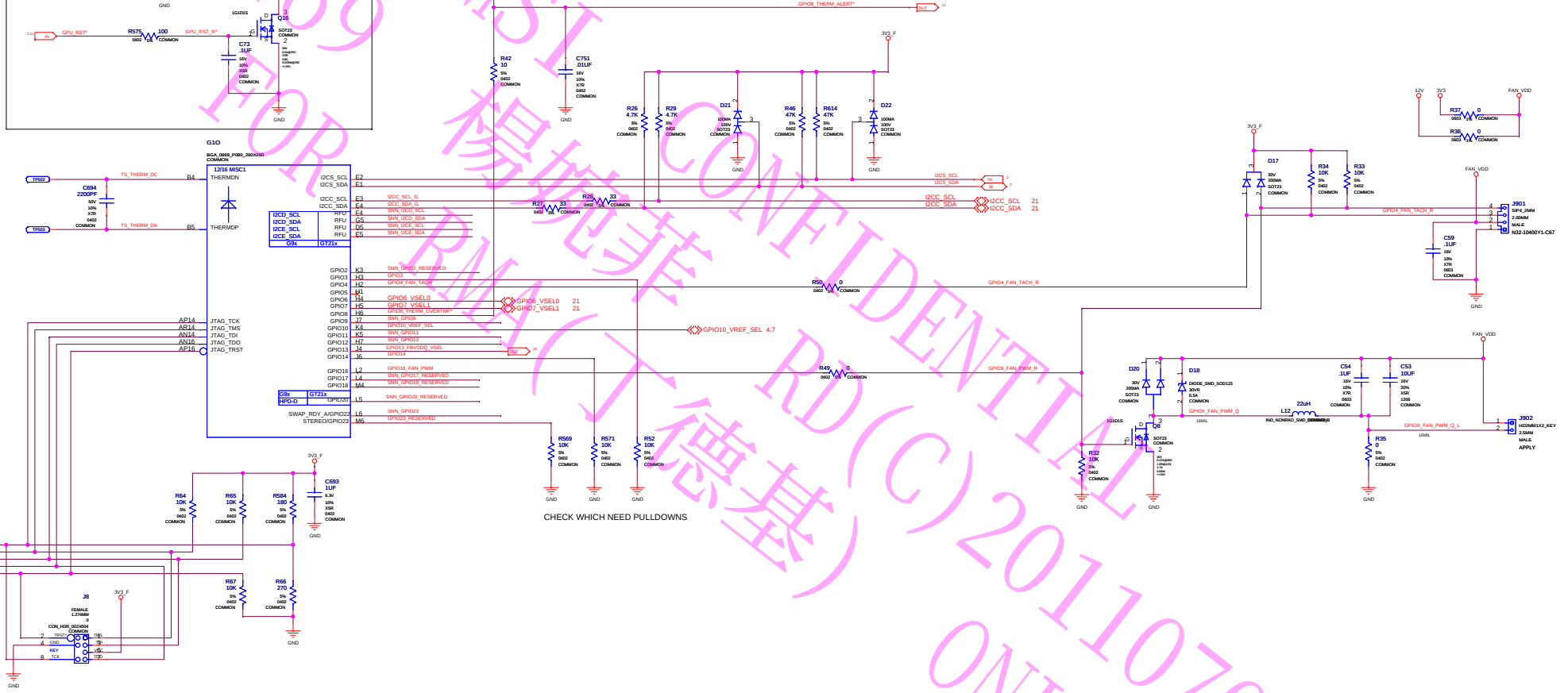
THERM ALERT, FAN CONTROL, GPIO & JTAG

THERM ALERT LATCH







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FAN CONTROL, THERMAL ALERT, GPIO, JTAG

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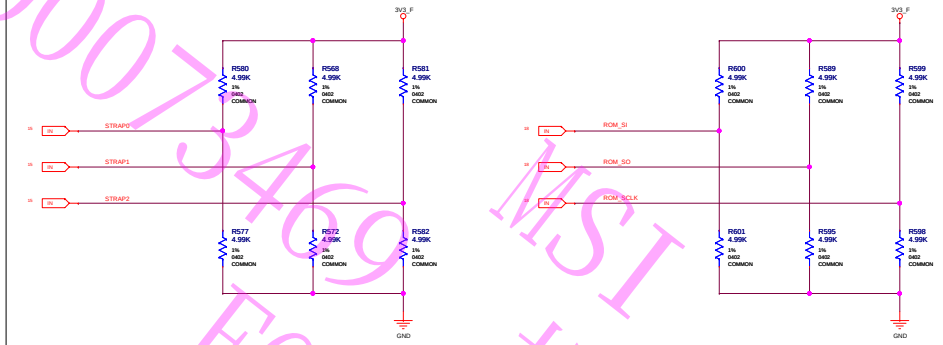
STRAPPING, VBIOS, INFOROM

STRAPPING OPTIONS



STRAP1[3..0] = 0x8 (3GIO_PADCFG DSKTOP default plus 0x8)

STRAP2[3..0] = 0xB (PCI_DEVID = 0xCAB)

ROM_SO[0] = 1 (VGA Device Enable)

ROM_SO[1] = 0 (SMB_ALT_ADDR, default (1GPU))

ROM_SO[2] = 0 (FB aper. size 256MB, default)

ROM_SO[3] = 0 (XCLK_417, default)

ROM_SCLK[0] = 0 (PEX_PLL_EN_TERM100 disabled, default)

ROM_SCLK[1] = 1 (SLT_CLK_CFG, default)

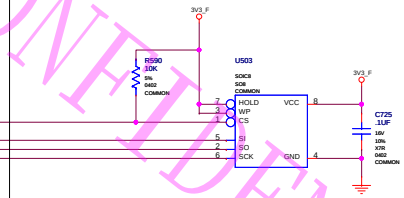
ROM_SCLK[2] = 1 (VBIOS RM present, default)

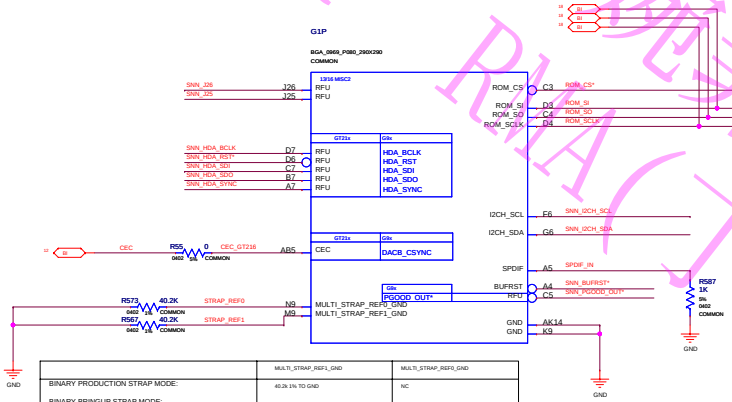
ROM_SCLK[3] = 0 (PCI_DEVID[4] = 0)

ROM_SI[3..0] = RAMCFG[3..0]

0x0001	Qimonda	128-bit, GDDR5
0x0010	Hynix	128-bit, GDDR5
0x0011	Samsung	128-bit, GDDR5

BIOS ROM(serial)





	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION STRAP MODE:	40.2k 1% TO GND	NC
BINARY BRINGUP STRAP MODE:	NC	NC
MULTI-LEVEL STRAP MODE:	40.2k 1% TO GND	40.2k 1% TO GND

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	VBIOS ROM, INFOROM, STRAPPING OPTIONS

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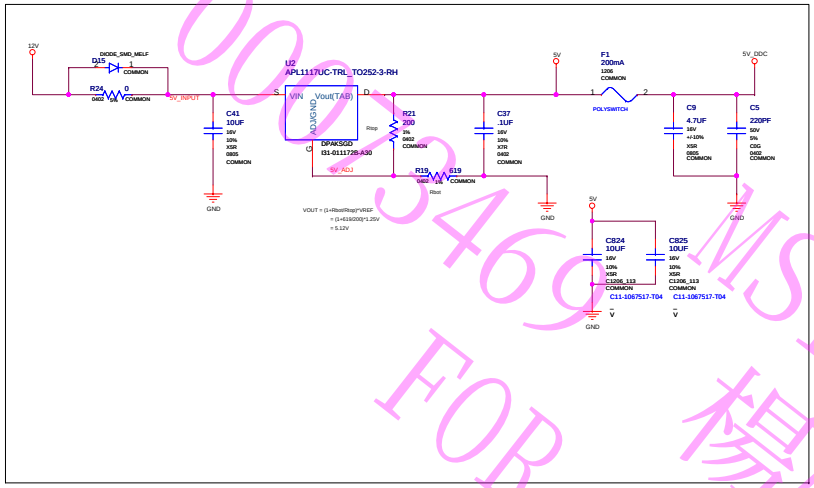
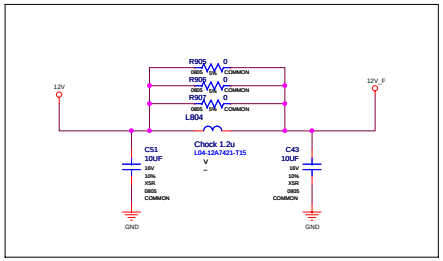
POWER SUPPLY: 5V, 5V_DDC, 1V8, INPUT FILTER

5V REGULATOR

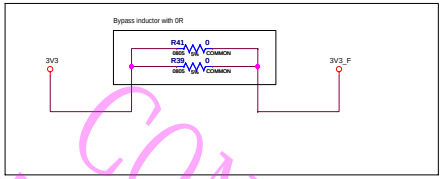


5V DDC

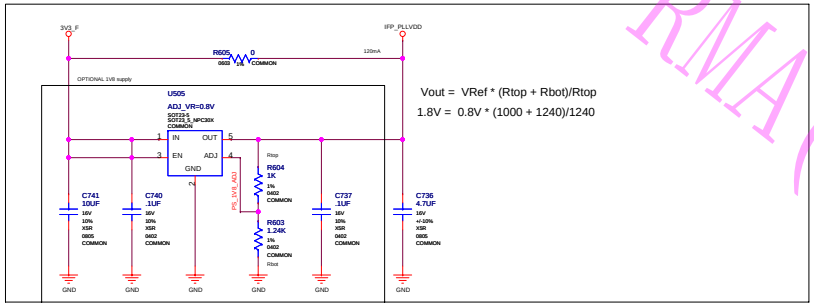
12V filter



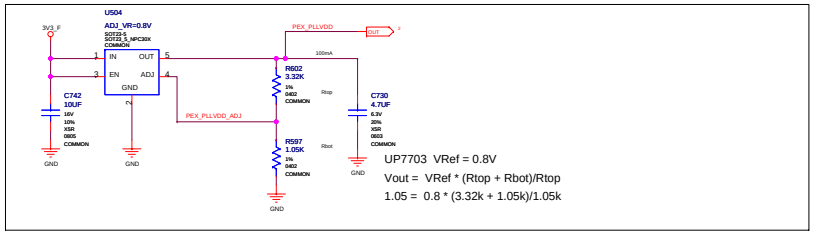
3.3V filter



IFPCEF PLLVDD supply



PEX_PLLVDD (optional)



NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	0.1A	12MIL	5V
5V_INPUT	0.2A	12MIL	5V
PS_1V8_ADJ		10MIL	1.8V
IFPA_IOVDD	0.3A	12MIL	3.2V
12V	6A	20MIL	12V
3V3	3A	12MIL	3.2V
3V3_F	4A	20MIL	3.3V
5V	0.3A	12MIL	5V
5V_DDC	0.1A	12MIL	5V
GND		10MIL	0V

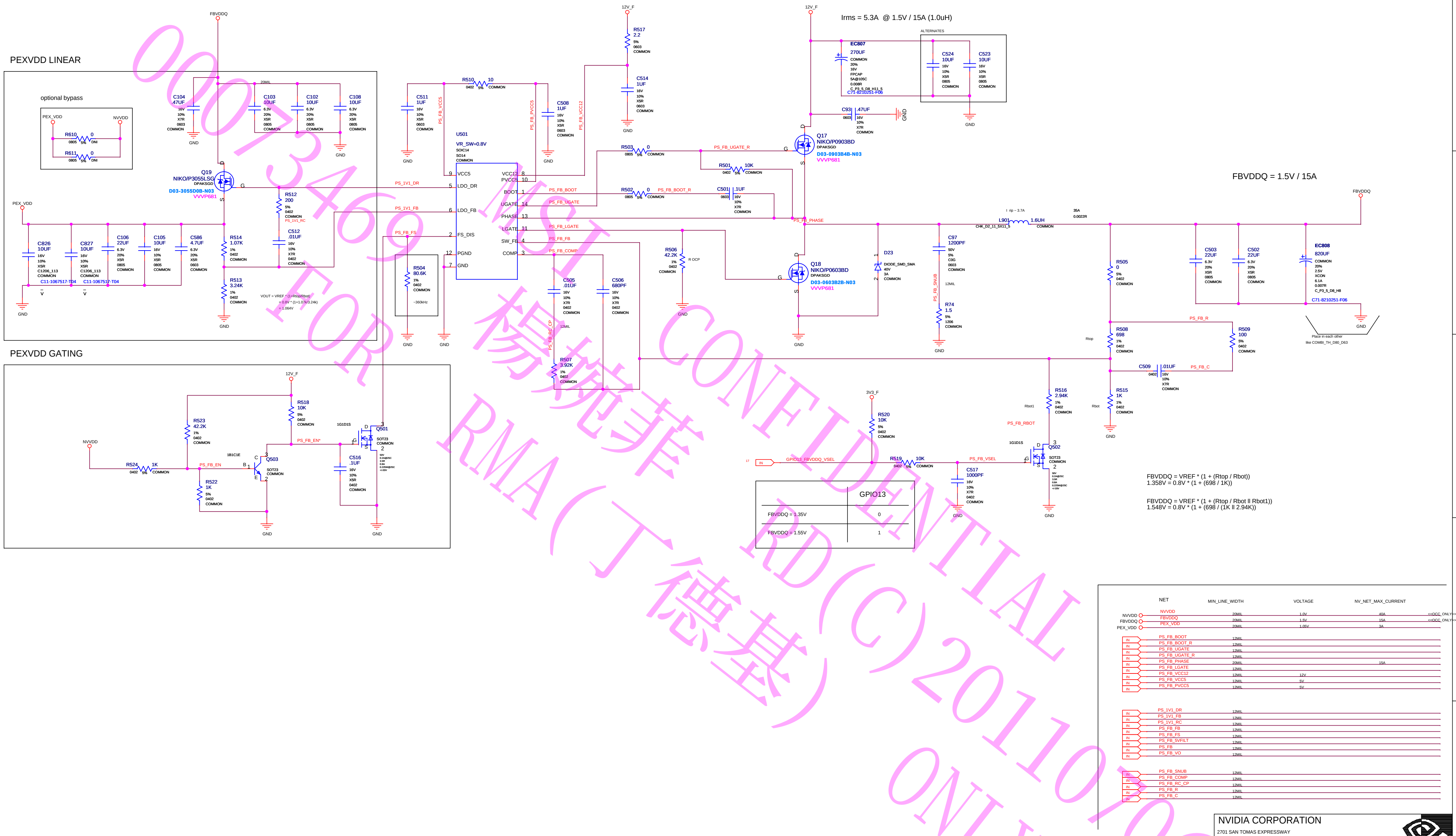
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	5V, DDC5V, IFP PLLVDD, IFP IOVDD, 3V3 FILTER, 12V FILTER

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A
ID	
PAGE	
NAME	
DATE	01-JUL-2009

POWER SUPPLY: FBVDDQ, PEX_VDD

FBVDDQ Power Supply 1.35-1.50V@15A



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBVDDQ SINGLE PHASE SWITCHER, PEX_VDD LINEAR

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN 600-10672-base-100 A
ID
PAGE
NAME
DATE 01-JUL-2009

Title: Basenet Report
Design: design
Date: Jun 9 10:09:58 2009

Base nets and synonyms for design_lib.DESIGN(@design_lib.design(sch_1))

Base Signal	Location([Zone][dir])
3V3	19.1G
3V3_F	19.1G
3V3_INFOROM	18.4F
3V3_PEX_SVDD	2.5G
3V3_PRSNT	21.2A
5V	19.1G
5V_ADJ	19.2B
5V_DDC	19.1G
5V_DDC_VGA	10.3G
5V_FUSED	19.1G
5V_INPUT	19.1A 19.1G
5V_PHASE	19.2B
12V	19.1G
12V_F	19.1G
12V_PRSNT	21.2A
CEC	12.2D 18.4B
CEC_GT216	18.4B
DACA_BLUE	9.3C 9.5A
DACA_BLUE_C	9.5A 9.5H 11.2G
DACA_GREEN	9.3C 9.5A
DACA_GREEN_C	9.4H 9.5A 11.2G
DACA_HSYNC	9.3C 9.5A
DACA_HSYNC_BUF	9.3D 9.5A
DACA_HSYNC_C	9.3H 9.5A 11.2G
DACA_HSYNC_R	9.3F 9.5A
DACA_RED	9.3C 9.5A
DACA_RED_C	9.4H 9.5A 11.2G
DACA_RSET	9.3B 9.5A
DACA_VDD	9.3B 9.5A
DACA_VREF	9.3B 9.5A
DACA_VSYNC	9.3C 9.5A
DACA_VSYNC_BUF	9.3D 9.5A
DACA_VSYNC_C	9.3H 9.5A 11.2G
DACA_VSYNC_R	9.3F 9.5A
DACB_BLUE	10.3C 10.5A
DACB_BLUE_C	10.5A 10.5G
DACB_GREEN	10.3C 10.5A
DACB_GREEN_C	10.4G 10.5A
DACB_HSYNC	10.3C 10.5A
DACB_HSYNC_BUF	10.3D 10.5A
DACB_HSYNC_C	10.3H 10.5A
DACB_HSYNC_R	10.3E 10.5A
DACB_RED	10.3C 10.5A
DACB_RED_C	10.4G 10.5A
DACB_RSET	10.3B 10.5A
DACB_VDD	10.3B 10.5A
DACB_VREF	10.3B 10.5A
DACB_VSYNC	10.3C 10.5A
DACB_VSYNC_BUF	10.3D 10.5A
DACB_VSYNC_C	10.3H 10.5A
DACB_VSYNC_R	10.3E 10.5A
FAN_PWM	17.1G
FAN_PWM_R	17.1G
FAN_VDD	17.1G
FBA_CLK0	3.4D 4.1F 4.2A
FBA_CLK0*	3.4D 4.1F 4.2A
FBA_CLK0_TERM	4.2B 4.2F
FBA_CLK1	3.4D 4.1F 4.2D
FBA_CLK1*	3.4D 4.1F 4.2D
FBA_CLK1_TERM	4.2E 4.2F
FBA_CMD<0>	3.3C 4.1B
FBA_CMD<30..0>	3.3D 4.1A 4.1D 4.1F
FBA_CMD<1>	3.3C 4.1B
FBA_CMD<2>	3.3C 4.1B
FBA_CMD<3>	3.3C 4.1E
FBA_CMD<4>	3.3C 4.1E
FBA_CMD<5>	3.3C 4.1E
FBA_CMD<6>	3.3C 4.2E 4.2G
FBA_CMD<7>	3.3C 4.1B
FBA_CMD<8>	3.3C 4.2B 4.2E 4.2G
FBA_CMD<9>	3.3C 4.1B
FBA_CMD<10>	3.3C 4.1B
FBA_CMD<11>	3.3C 4.1E
FBA_CMD<12>	3.3C 4.1E
FBA_CMD<13>	3.3C 4.1E
FBA_CMD<14>	3.3C 4.1B
FBA_CMD<15>	3.3C 4.1E
FBA_CMD<16>	3.3C 4.1E
FBA_CMD<17>	3.3C 4.1E
FBA_CMD<18>	3.3C 4.1B
FBA_CMD<19>	3.3C 4.1E
FBA_CMD<20>	3.3C 4.2B 4.2G
FBA_CMD<21>	3.3C 4.1E
FBA_CMD<22>	3.3C 4.1B
FBA_CMD<23>	3.4C 4.1B
FBA_CMD<24>	3.4C 4.1B
FBA_CMD<25>	3.4C 4.1B
FBA_CMD<26>	3.4C 4.1B
FBA_CMD<27>	3.4C 4.1E
FBA_CMD<28>	3.4C 4.1E
FBA_CMD<29>	3.4C 4.1B
FBA_CMD<30>	3.4C 4.1E
FBA_D<0>	3.1B 4.4B
FBA_D<63..0>	3.1A 4.1F 4.4A
FBA_D<1>	3.1B 4.4B
FBA_D<2>	3.1B 4.4B
FBA_D<3>	3.1B 4.4B
FBA_D<4>	3.1B 4.4B
FBA_D<5>	3.1B 4.4B
FBA_D<6>	3.1B 4.4B
FBA_D<7>	3.1B 4.4B
FBA_D<8>	3.1B 4.4B
FBA_D<9>	3.1B 4.4B
FBA_D<10>	3.1B 4.4B
FBA_D<11>	3.1B 4.5B
FBA_D<12>	3.1B 4.5B
FBA_D<13>	3.1B 4.5B
FBA_D<14>	3.1B 4.5B
FBA_D<15>	3.2B 4.5B
FBA_D<16>	3.2B 4.4C
FBA_D<17>	3.2B 4.4C
FBA_D<18>	3.2B 4.4C
FBA_D<19>	3.2B 4.4C
FBA_D<20>	3.2B 4.4C
FBA_D<21>	3.2B 4.4C
FBA_D<22>	3.2B 4.4C
FBA_D<23>	3.2B 4.4C
FBA_D<24>	3.2B 4.4C
FBA_D<25>	3.2B 4.4C
FBA_D<26>	3.2B 4.4C
FBA_D<27>	3.2B 4.5C
FBA_D<28>	3.2B 4.5C
FBA_D<29>	3.2B 4.5C
FBA_D<30>	3.2B 4.5C
FBA_D<31>	3.2B 4.5C
FBA_D<32>	3.2B 4.4D
FBA_D<33>	3.2B 4.4D
FBA_D<34>	3.2B 4.4D
FBA_D<35>	3.2B 4.4D
FBA_D<36>	3.2B 4.4D
FBA_D<37>	3.2B 4.4D
FBA_D<38>	3.2B 4.4D
FBA_D<39>	3.2B 4.4D
FBA_D<40>	3.2B 4.4D
FBA_D<41>	3.2B 4.4D
FBA_D<42>	3.2B 4.4D
FBA_D<43>	3.2B 4.5D
FBA_D<44>	3.2B 4.5D
FBA_D<45>	3.3B 4.5D
FBA_D<46>	3.3B 4.5D
FBA_D<47>	3.3B 4.5D
FBA_D<48>	3.3B
FBA_D<49>	3.3B
FBA_D<50>	3.3B
FBA_D<51>	3.3B
FBA_D<52>	3.3B
FBA_D<53>	3.3B
FBA_D<54>	3.3B
FBA_D<55>	3.3B
FBA_D<56>	3.3B
FBA_D<57>	3.3B
FBA_D<58>	3.3B
FBA_D<59>	3.3B
FBA_D<60>	3.3B
FBA_D<61>	3.3B
FBA_D<62>	3.3B
FBA_D<63>	3.3B
FBA_DBI<0>	3.3B 4.4B
FBA_DBI<7..0>	3.3A 4.1F 4.4A
FBA_DBI<1>	3.3B 4.5B
FBA_DBI<2>	3.3B 4.4C
FBA_DBI<3>	3.3B 4.5C
FBA_DBI<4>	3.3B 4.4D
FBA_DBI<5>	3.3B 4.5D
FBA_DBI<6>	3.3B 4.4E
FBA_DBI<7>	3.3B 4.5E
FBA_DEBUG	3.4D
FBA_DEBUG_SEN0	4.3B
FBA_DEBUG_SEN1	4.3E
FBA_EDC<0>	3.4B 4.4B
FBA_EDC<7..0>	3.4A 4.1F 4.4A
FBA_EDC<1>	3.4B 4.5B
FBA_EDC<2>	3.4B 4.4C
FBA_EDC<3>	3.4B 4.5C
FBA_EDC<4>	3.4B 4.4D
FBA_EDC<5>	3.4B 4.5D
FBA_EDC<6>	3.4B 4.4E
FBA_EDC<7>	3.4B 4.5E
FBA_VREF	3.1F
FBA_VREFC0	4.1F 4.2B
FBA_VREFC1	4.1F 4.2E
FBA_VREFD0	4.2F 4.4F
FBA_VREFD1	4.2F 4.4F
FBA_VREF_PROBE	3.5B
FBA_WCK01	3.4A 4.1F 4.5A
FBA_WCK01*	3.4A 4.1F 4.5A
FBA_WCK01_CT	4.2F 4.5B
FBA_WCK23	3.4A 4.1F 4.5C
FBA_WCK23*	3.4A 4.1F 4.5C
FBA_WCK23_CT	4.2F 4.5C
FBA_WCK45	3.4A 4.1F 4.5D
FBA_WCK45*	3.4A 4.1F 4.5D
FBA_WCK45_CT	4.2F 4.5D
FBA_WCK67	3.4A 4.1F 4.5E
FBA_WCK67*	3.4A 4.1F 4.5E
FBA_WCK67_CT	4.2F 4.5E
FBA_ZQ0	4.2B
FBA_ZQ1	4.2E
FBC_CLK0	6.4D 7.1G 7.2A
FBC_CLK0*	6.4D 7.1G 7.2A
FBC_CLK0_TERM	7.2B 7.2G
FBC_CLK1	6.4D 7.1G 7.2D
FBC_CLK1*	6.4D 7.1G 7.2D
FBC_CLK1_TERM	7.2E 7.2G
FBC_CMD<0>	6.3C 7.1B
FBC_CMD<30..0>	6.3D 7.1A 7.1D 7.1G
FBC_CMD<1>	6.3C 7.1B
FBC_CMD<2>	6.3C 7.1B
FBC_CMD<3>	6.3C 7.1E
FBC_CMD<4>	6.3C 7.1E
FBC_CMD<5>	6.3C 7.1E
FBC_CMD<6>	6.3C 7.2E 7.2G
FBC_CMD<7>	6.3C 7.1B
FBC_CMD<8>	6.3C 7.2B 7.2E 7.2G
FBC_CMD<9>	6.3C 7.1B
FBC_CMD<10>	6.3C 7.1B
FBC_CMD<11>	6.3C 7.1E
FBC_CMD<12>	6.3C 7.1E
FBC_CMD<13>	6.3C 7.1E
FBC_CMD<14>	6.3C 7.1B
FBC_CMD<15>	6.3C 7.1E
FBC_CMD<16>	6.3C 7.1E
FBC_CMD<17>	6.3C 7.1E
FBC_CMD<18>	6.3C 7.1B
FBC_CMD<19>	6.3C 7.1E
FBC_CMD<20>	6.3C 7.2B 7.2G
FBC_CMD<21>	6.3C 7.1E
FBC_CMD<22>	6.3C 7.1B
FBC_CMD<23>	6.4C 7.1B
FBC_CMD<24>	6.4C 7.1B
FBC_CMD<25>	6.4C 7.1B
FBC_CMD<26>	6.4C 7.1B
FBC_CMD<27>	6.4C 7.1E
FBC_CMD<28>	6.4C 7.1E
FBC_CMD<29>	6.4C 7.1B
FBC_CMD<30>	6.4C 7.1E
FBC_D<0>	6.1A 7.4B
FBC_D<63..0>	6.1A 7.1G 7.4A
FBC_D<1>	6.1A 7.4B
FBC_D<2>	6.1A 7.4B
FBC_D<3>	6.1A 7.4B
FBC_D<4>	6.1A 7.4B
FBC_D<5>	6.1A 7.4B
FBC_D<6>	6.1A 7.4B
FBC_D<7>	6.1A 7.4B
FBC_D<8>	6.1A 7.4B
FBC_D<9>	6.1A 7.4B
FBC_D<10>	6.1A 7.4B
FBC_D<11>	6.1A 7.4B
FBC_D<12>	6.1A 7.5B
FBC_D<13>	6.1A 7.5B
FBC_D<14>	6.1A 7.5B
FBC_D<15>	6.2A 7.5B
FBC_D<16>	6.2A 7.4C
FBC_D<17>	6.2A 7.4C
FBC_D<18>	6.2A 7.4C
FBC_D<19>	6.2A 7.4C
FBC_D<20>	6.2A 7.4C
FBC_D<21>	6.2A 7.4C
FBC_D<22>	6.2A 7.4C
FBC_D<23>	6.2A 7.4C
FBC_D<24>	6.2A 7.4C
FBC_D<25>	6.2A 7.4C
FBC_D<26>	6.2A 7.4C
FBC_D<27>	6.2A 7.4C
FBC_D<28>	6.2A 7.5C
FBC_D<29>	6.2A 7.5C
FBC_D<30>	6.2A 7.5C
FBC_D<31>	6.2A 7.5C
FBC_D<32>	6.2A 7.4D
FBC_D<33>	6.2A 7.4D
FBC_D<34>	6.2A 7.4D
FBC_D<35>	6.2A 7.4D
FBC_D<36>	6.2A 7.4D
FBC_D<37>	6.2A 7.4D
FBC_D<38>	6.2A 7.4D
FBC_D<39>	6.2A 7.4D
FBC_D<40>	6.2A 7.4D
FBC_D<41>	6.2A 7.4D
FBC_D<42>	6.2A 7.4D
FBC_D<43>	6.2A 7.4D
FBC_D<44>	6.2A 7.5D
FBC_D<45>	6.3A 7.5D
FBC_D<46>	6.3A 7.5D
FBC_D<47>	6.3A 7.5D
FBC_D<48>	6.3A
FBC_D<49>	6.3A
FBC_D<50>	6.3A
FBC_D<51>	6.3A
FBC_D<52>	6.3A
FBC_D<53>	6.3A
FBC_D<54>	6.3A
FBC_D<55>	6.3A
FBC_D<56>	6.3A
FBC_D<57>	6.3A
FBC_D<58>	6.3A
FBC_D<59>	6.3A
FBC_D<60>	6.3A
FBC_D<61>	6.3A
FBC_D<62>	6.3A
FBC_D<63>	6.3A
FBC_DBI<0>	6.3A 7.4B
FBC_DBI<7..0>	6.3A 7.1G 7.4A
FBC_DBI<1>	6.3A 7.5B
FBC_DBI<2>	6.3A 7.4C
FBC_DBI<3>	6.3A 7.5C
FBC_DBI<4>	6.3A 7.4D
FBC_DBI<5>	6.3A 7.5D
FBC_DBI<6>	6.3A 7.4E
FBC_DBI<7>	6.3A 7.5E
FBC_DEBUG	6.4C
FBC_DEBUG_SEN0	7.3B
FBC_DEBUG_SEN1	7.3E
FBC_EDC<0>	6.4A 7.4B
FBC_EDC<7..0>	6.4A 7.1G 7.4A
FBC_EDC<1>	6.4A 7.5B
FBC_EDC<2>	6.4A 7.4C
FBC_EDC<3>	6.4A 7.5C
FBC_EDC<4>	6.4A 7.4D
FBC_EDC<5>	6.4A 7.5D
FBC_EDC<6>	6.4A 7.4E
FBC_EDC<7>	6.4A 7.5E
FBC_VREFC0	7.1G 7.2B
FBC_VREFC1	7.1G 7.2E
FBC_VREFD0	7.1G 7.4F
FBC_VREFD1	7.2G 7.4F
FBC_WCK01	6.4A 7.1G 7.5A
FBC_WCK01*	6.4A 7.1G 7.5A
FBC_WCK01_CT	7.2G 7.5B
FBC_WCK23	6.4A 7.1G 7.5C
FBC_WCK23*	6.4A 7.1G 7.5C
FBC_WCK23_CT	7.2G 7.5C
FBC_WCK45	6.4A 7.1G 7.5D
FBC_WCK45*	6.4A 7.1G 7.5D
FBC_WCK45_CT	7.2G 7.5D
FBC_WCK67	6.4A 7.1G 7.5E
FBC_WCK67*	6.5A 7.1G 7.5E
FBC_WCK67_CT	7.2G 7.5F
FBC_ZQ0	7.2B
FBC_ZQ1	7.3E
FBVDDQ	20.4A
FB_CAL_PD	6.1G
FB_CAL_PD_VDDQ	6.5C
FB_CAL_PU	6.1G
FB_CAL_PU_GND	6.5C
FB_CAL_TERM	6.1G
FB_CAL_TERM_GND	6.5C
FB_PLLAVDD	3.1F 3.5C
GPIO0_HPD_DVI_1	11.3D
GPIO0_HPD_DVI_1_R	11.3E
GPIO0_HPD_DVI_1_RL	11.2G
GPIO1_HPDC	12.3C
GPIO1_HPDC_R	12.3E
GPIO1_HPDC_R_L_1	12.3F
GPIO3	17.3C
GPIO4_FAN_TACH	17.3C
GPIO4_FAN_TACH_R	17.3F 17.3H
GPIO5_VSEL0	17.3D 21.1A
GPIO5_VSEL_R	21.1A
GPIO6_VSEL1	17.3D 21.4A
GPIO6_VSEL1_R	21.4A
GPIO7_VSEL2	17.3D 21.3A
GPIO8_NPN_B	17.2B
GPIO8_PNP_B	17.1B
GPIO8_PNP_C	17.1B
GPIO8_THERM_ALERT*	17.2E 21.3A
GPIO8_THERM_OVERTM	17.3C
P*	
GPIO9_FAN_PWM_R	17.3H 17.4F
GPIO10_VREF_SEL	17.3C
GPIO13_FBVDDQ_VSEL	17.4D 20.4E
GPIO14	17.4C
GPIO16_FAN_PWM	17.4C
GPIO23_RESERVED	17.4C
GPIOX_FAN_PWM_Q	17.4G
GPIOX_FAN_PWM_Q_L	17.4H
GPU_PLLVDD	16.1B 16.5G
GPU_PLLVDD_SP	16.1B 16.5G
GPU_RST*	2.2D 11.5D 17.2A
GPU_RST_R*	17.2B
GPU_RST_R_Q	17.2B
GPU_TESTMODE	2.5E
HDMI_CEC_C_1	12.3G
HDMI_CEC_Q	12.2E
HDMI_PD_1	12.4E
I2CA_SCL	9.2D 9.3C
I2CA_SCL_C	9.2H 11.2G
I2CA_SCL_T	9.2F
I2CA_SDA	9.2D 9.3C
I2CA_SDA_C	9.2H 11.2G
I2CA_SDA_T	9.2F
I2CB_SCL	10.3C
I2CB_SCL_R	10.2E
I2CB_SCL_R_L	10.2H
I2CB_SDA	10.3C
I2CB_SDA_R	10.2E
I2CB_SDA_R_L	10.2H
I2CC_SCL	17.3F 18.4D
I2CC_SCL_G	17.3C
I2CC_SCL_ROM	18.4E
I2CC_SDA	17.3F 18.4D
I2CC_SDA_G	17.3C
I2CC_SDA_ROM	18.4E
I2CS_SCL	2.1C 17.3F
I2CS_SDA	2.2C 17.3F
I2CW_SCL	12.2C
I2CW_SCL_R	12.1D 12.1G
I2CW_SCL_R_Q	12.1F 12.1H
I2CW_SDA	12.2C
I2CW_SDA_R	12.1D 12.1G
I2CW_SDA_R_Q	12.1F 12.1H
IFPAB_IOVDD	11.2B 11.5A
IFPAB_PLLVDD	11.2B 11.5A
IFPAB_RSET	11.2B 11.5A
IFPA_IOVDD	19.1G
IFPA_IOVDD_EN*	11.4E
IFPA_IOVDD_EN_RC	11.4E
IFPA_TXC	11.2D 11.5A
IFPA_TXC*	11.2D 11.4A
IFPA_TXD0	11.1D 11.5A
IFPA_TXD0*	11.1D 11.5A
IFPA_TXD1	11.1D 11.5A
IFPA_TXD1*	11.1D 11.5A
IFPA_TXD2	11.2D 11.5A
IFPA_TXD2*	11.2D 11.5A
IFPB_TXD4	11.2D 11.5A
IFPB_TXD4*	11.2D 11.5A
IFPB_TXD5	11.2D 11.5A
IFPB_TXD5*	11.2D 11.5A
IFPB_TXD6	11.2D 11.5A
IFPB_TXD6*	11.2D 11.5A
IFPC_IOVDD	12.3B 12.5A
IFPC_PLLVDD	12.2B
IFPC_RSET	12.2B 12.5A
IFPC_TERM_ENA	12.4D
IFPC_TXC	12.3C 12.4A
IFPC_TXC*	12.3C 12.4A
IFPC_TXC_C1	12.3E 12.4F 12.5A
IFPC_TXC_C1*	12.3E 12.4F 12.5A
IFPC_TXD0	12.3C 12.5A
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IFPC_TXD2_C1*	12.3E 12.4F 12.5A
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MIOA_VDDQ	15.1B
MIOB_CLKIN	15.4D
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NVVDD_BOOT1_C	21.3D 21.5A
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NVVDD_CSN	21.4D
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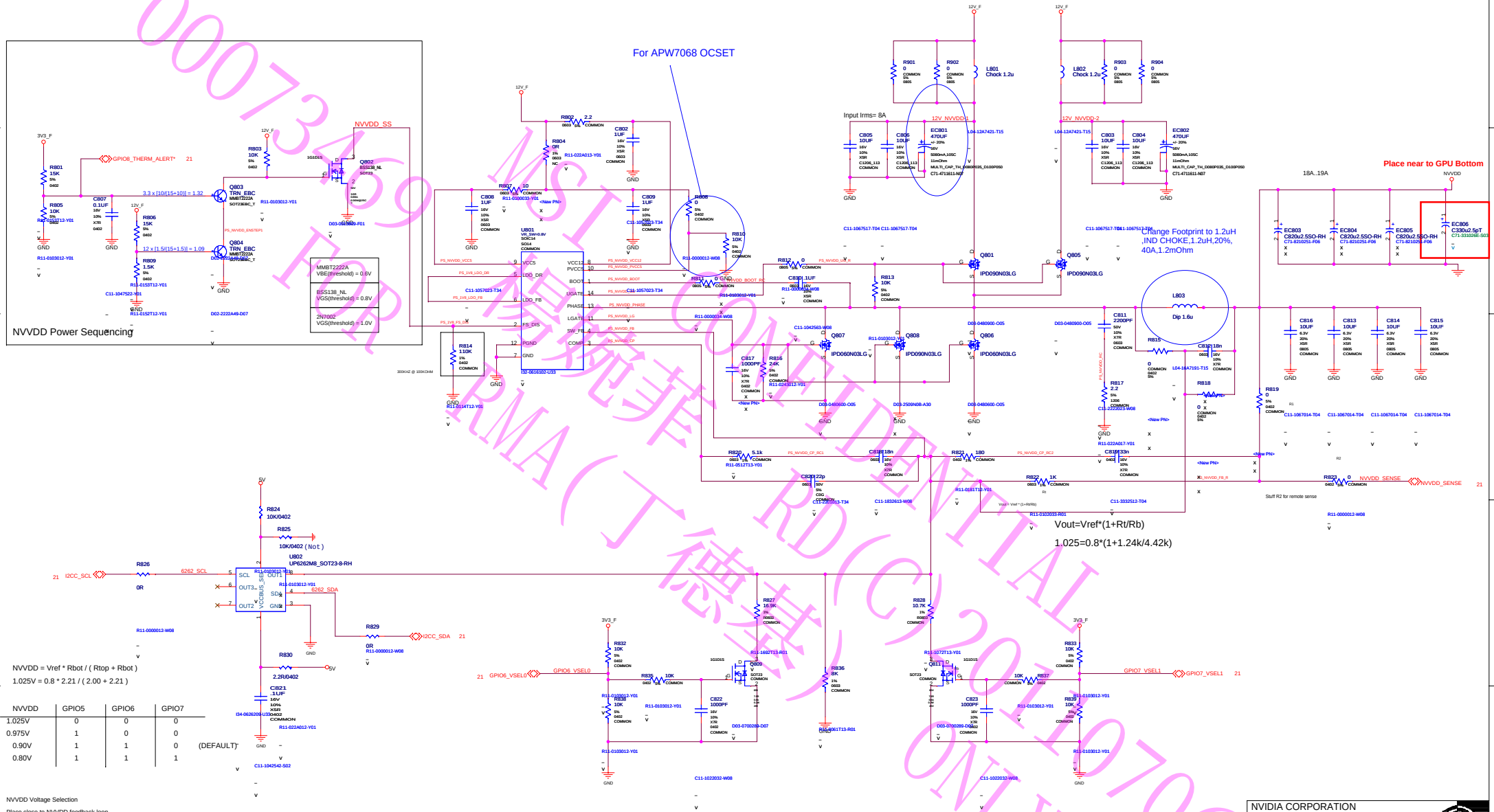
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME	<ENGINEER>	DATE	01-JUL-2009

Power Supply III: NVVDD



NVVDD	GPIO5	GPIO6	GPIO7
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0.975V	1	0	0
0.90V	1	1	0
0.80V	1	1	1

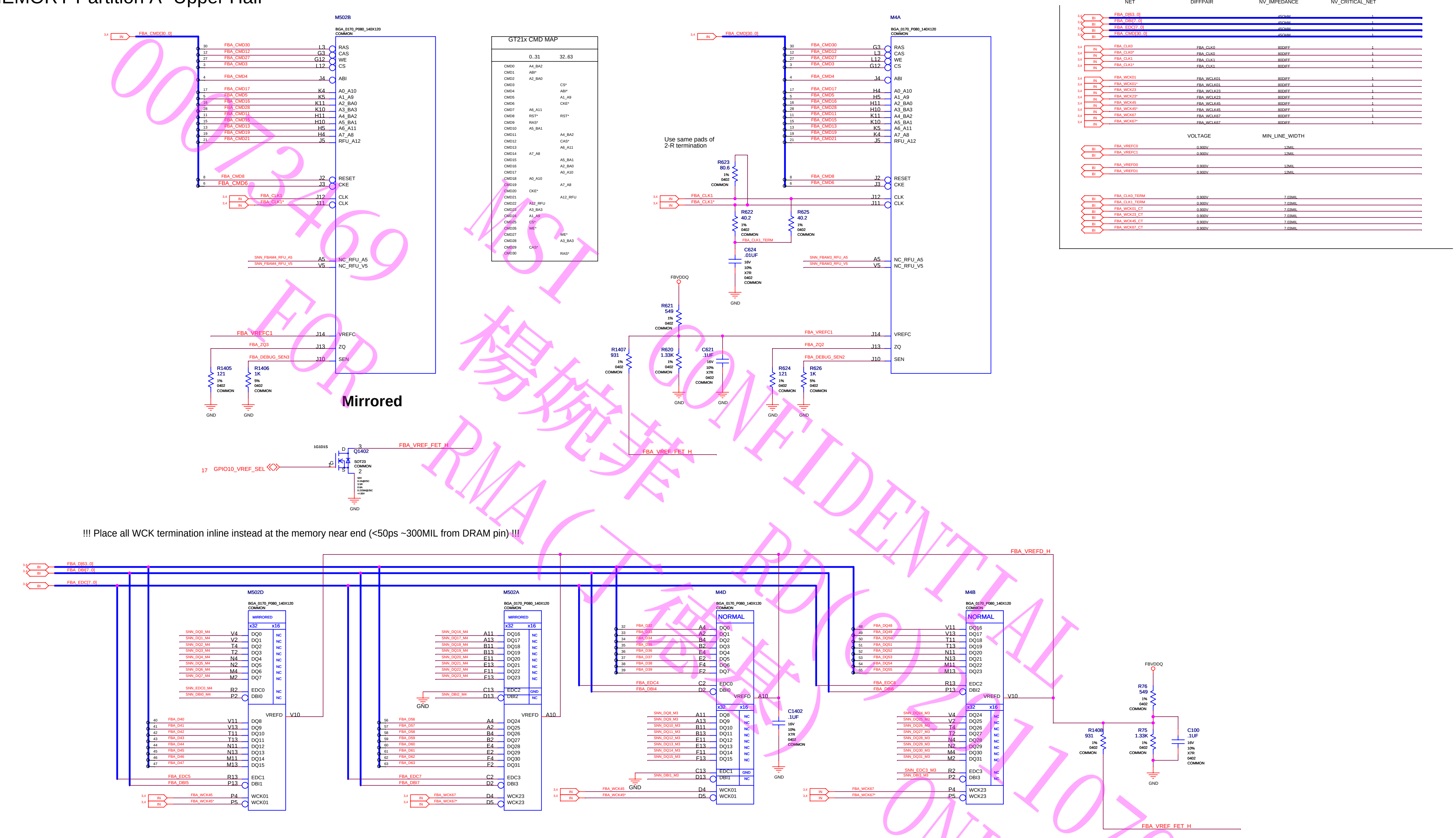
(DEFAULT)

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	NVVDD POWER SUPPLY

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10681-base-100 A
ID	
NAME	
PAGE	
DATE	05-FEB-2009

MEMORY Partition A -Upper Half



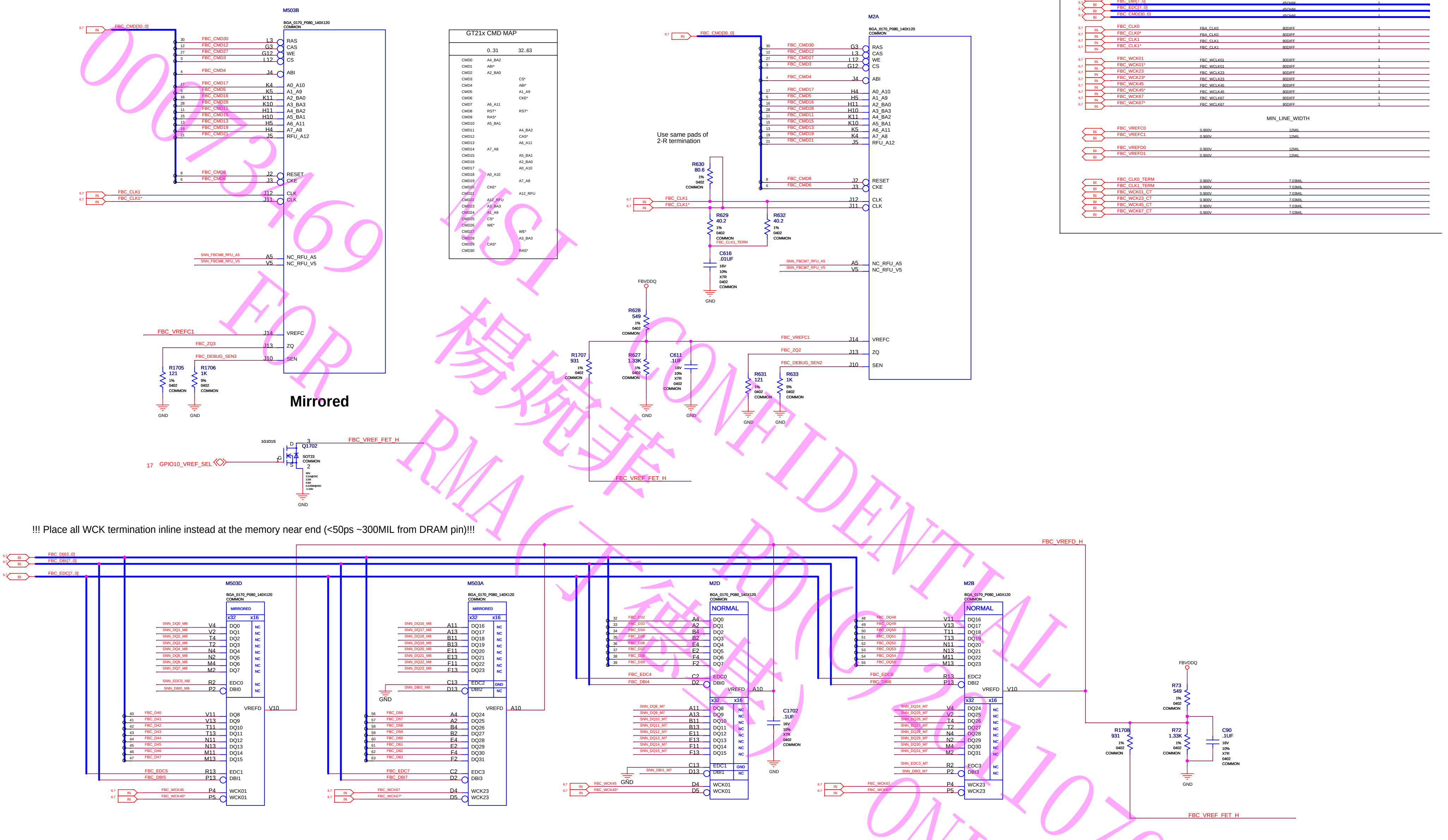
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 32Mx32 GDDR5 MEMORIES, FBA CLK TERMS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN 600-10672-base-100 A

ID | PAGE | NAME | DATE 01-JUL-2009

MEMORY Partition C-----Upper Half



!!! Place all WCK termination inline instead at the memory rear end (<50ps ~300MIL from DRAM pin)!!!

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 32MX32 GDDR5 MEMORIES, FBC CLK TERMS

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