P218 - NV43 Ultra AGP 128MB DDR3 Board

PAGE SUMMARY:

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10218-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	600102180000200	602-10218-0000-200	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA+DVI-I+HDTV-out
2	600102180001200	602-10218-0001-200	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
3	600102180002200	602-10218-0002-200	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, DVI-I + DVI-I + VIDEO-In
4	600102180003200	602-10218-0003-200	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

2. Update Memory bus per command bus

ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	P218 Top Page

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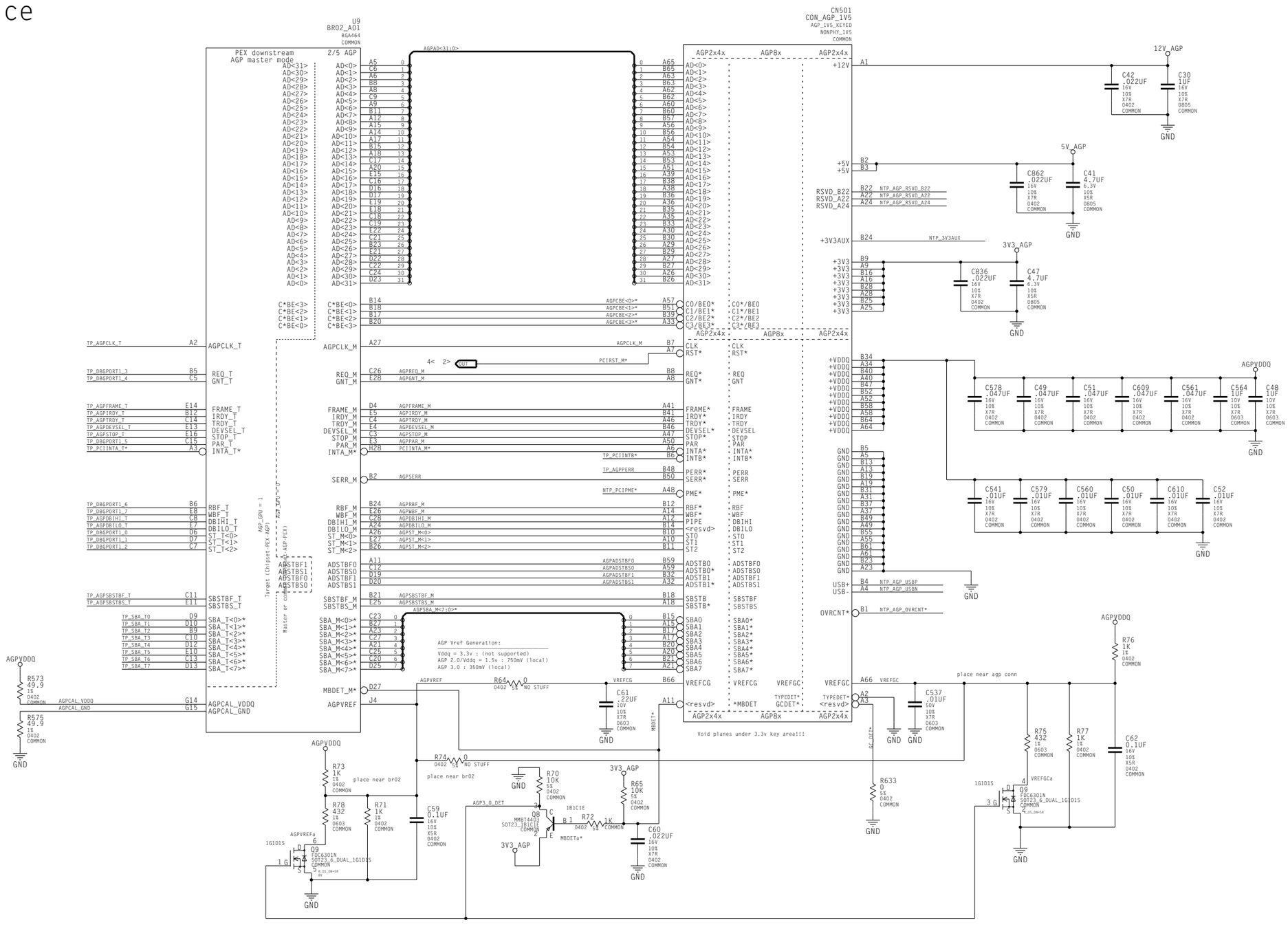
2. AGP to BR02 Interface



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ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal		
PAGE DETAIL	AGP to BR02 Interface		
NV_PN	602-10218-0001-200		
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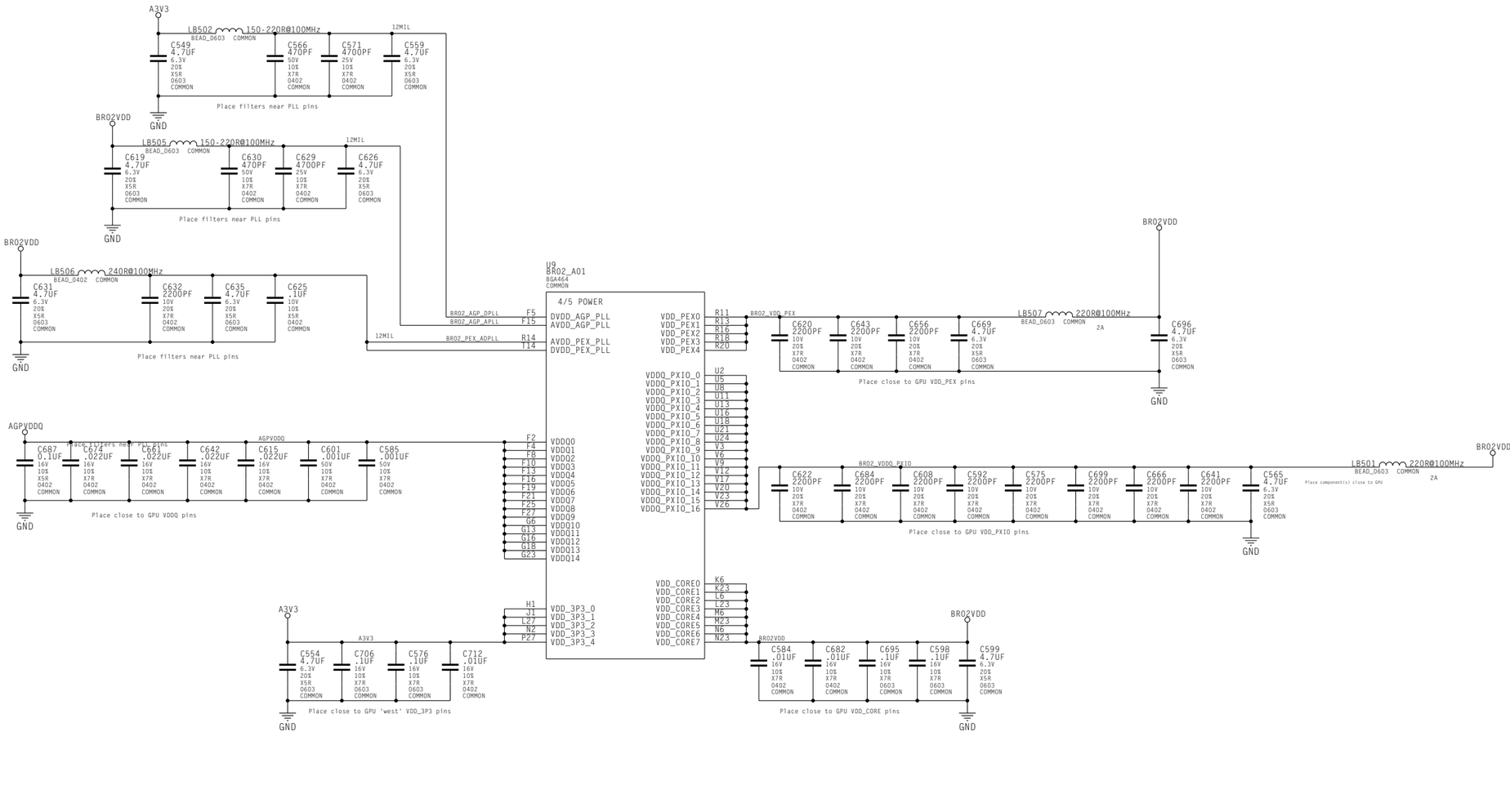
3. BR02 PWR/GND/De-Coupling



ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	BR02 PWR/GND/De-Coupling

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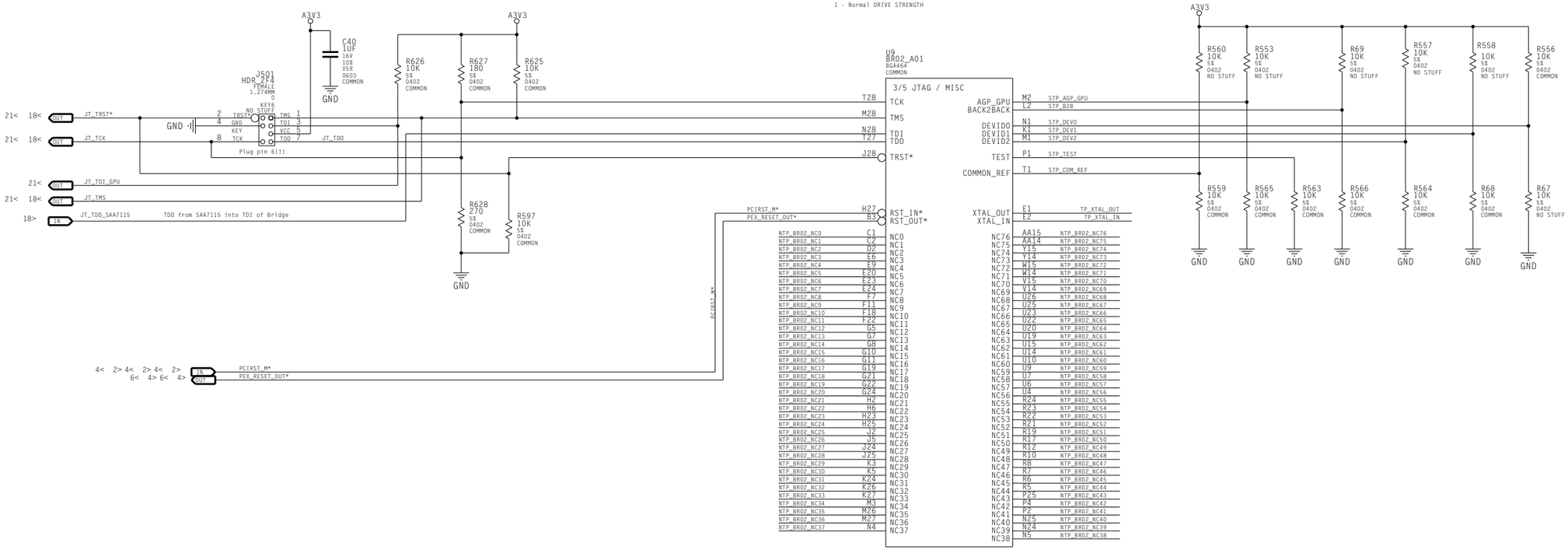
4. BR02 JTAG / Straps / Misc.

Straps:
AGP_GPU
0 - AGP Master, PCI Exp is Downstream Port (default)
1 - AGP Target, PCI Exp is Upstream Port
B2B
0 - No BR02 in PCIExp slot
1 - BR02 is plugged into PCIExp slot
DEVID[2:0]
000 - BR02 is plugged into PCIExp slot (PCI DevID = 00FD)
001 - High-Power GPU is plugged into PCIExp slot (PCI DevID = 00F1)
01X - High-Power GPU is plugged into PCIExp slot (PCI DevID = 00F3:00F2)
1XX - Mainstream GPU is plugged into PCIExp slot (PCI DevID = 00F7:F4)
DRIVE STRENGTH
0 - Reduced DRIVE STRENGTH
1 - Normal DRIVE STRENGTH



NTP_BR02_NC0	C1	NC0	NC76 AA15 NTP_BR02_NC76
NTP_BR02_NC1	C2	NC1	NC75 AA14 NTP_BR02_NC75
NTP_BR02_NC2	D2	NC2	NC74 Y15 NTP_BR02_NC74
NTP_BR02_NC3	E6	NC3	NC73 Y14 NTP_BR02_NC73
NTP_BR02_NC4	E9	NC4	NC72 W15 NTP_BR02_NC72
NTP_BR02_NC5	E20	NC5	NC71 W14 NTP_BR02_NC71
NTP_BR02_NC6	E23	NC6	NC70 V15 NTP_BR02_NC70
NTP_BR02_NC7	E24	NC7	NC69 V14 NTP_BR02_NC69
NTP_BR02_NC8	F7	NC8	NC68 U26 NTP_BR02_NC68
NTP_BR02_NC9	F11	NC9	NC67 U25 NTP_BR02_NC67
NTP_BR02_NC10	F18	NC10	NC66 U23 NTP_BR02_NC66
NTP_BR02_NC11	F22	NC11	NC65 U22 NTP_BR02_NC65
NTP_BR02_NC12	G5	NC12	NC64 U20 NTP_BR02_NC64
NTP_BR02_NC13	G7	NC13	NC63 U19 NTP_BR02_NC63
NTP_BR02_NC14	G8	NC14	NC62 U15 NTP_BR02_NC62
NTP_BR02_NC15	G10	NC15	NC61 U14 NTP_BR02_NC61
NTP_BR02_NC16	G11	NC16	NC60 U10 NTP_BR02_NC60
NTP_BR02_NC17	G19	NC17	NC59 U9 NTP_BR02_NC59
NTP_BR02_NC18	G21	NC18	NC58 U7 NTP_BR02_NC58
NTP_BR02_NC19	G22	NC19	NC57 U6 NTP_BR02_NC57
NTP_BR02_NC20	G24	NC20	NC56 U4 NTP_BR02_NC56
NTP_BR02_NC21	H2	NC21	NC55 R24 NTP_BR02_NC55
NTP_BR02_NC22	H6	NC22	NC54 R23 NTP_BR02_NC54
NTP_BR02_NC23	H23	NC23	NC53 R22 NTP_BR02_NC53
NTP_BR02_NC24	H25	NC24	NC52 R21 NTP_BR02_NC52
NTP_BR02_NC25	J2	NC25	NC51 R19 NTP_BR02_NC51
NTP_BR02_NC26	J5	NC26	NC50 R17 NTP_BR02_NC50
NTP_BR02_NC27	J24	NC27	NC49 R12 NTP_BR02_NC49
NTP_BR02_NC28	J25	NC28	NC48 R10 NTP_BR02_NC48
NTP_BR02_NC29	K3	NC29	NC47 R8 NTP_BR02_NC47
NTP_BR02_NC30	K5	NC30	NC46 R7 NTP_BR02_NC46
NTP_BR02_NC31	K24	NC31	NC45 R6 NTP_BR02_NC45
NTP_BR02_NC32	K26	NC32	NC44 R5 NTP_BR02_NC44
NTP_BR02_NC33	K27	NC33	NC43 P25 NTP_BR02_NC43
NTP_BR02_NC34	M3	NC34	NC42 P4 NTP_BR02_NC42
NTP_BR02_NC35	M26	NC35	NC41 P2 NTP_BR02_NC41
NTP_BR02_NC36	M27	NC36	NC40 N25 NTP_BR02_NC40
NTP_BR02_NC37	N4	NC37	NC39 N24 NTP_BR02_NC39
			NC38 N5 NTP_BR02_NC38

ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	BR02 JTAG / Straps / Misc.

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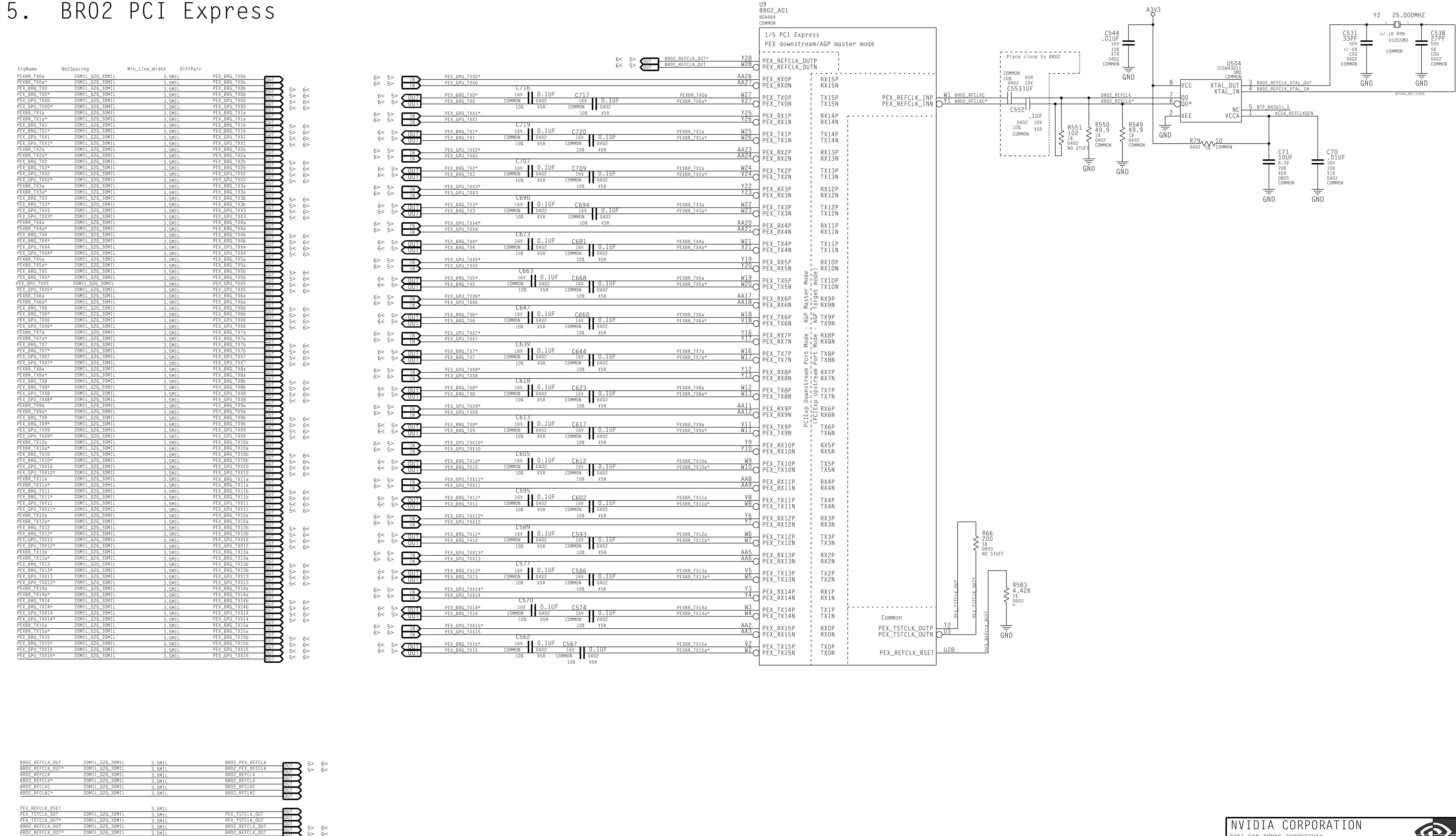
5. BR02 PCI Express



ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	BR02 PCI Express

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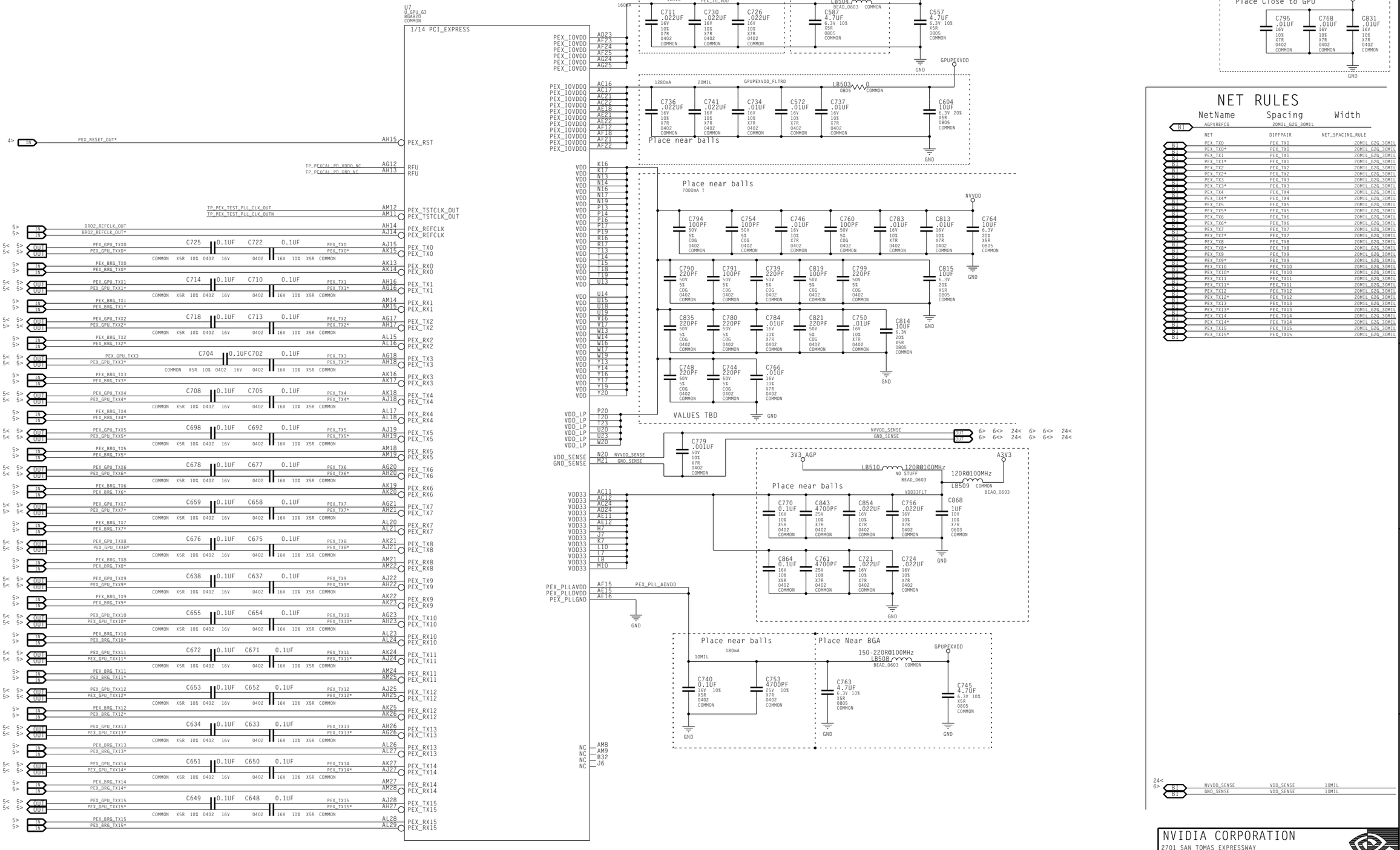
6. NV43 PCI Express Interface



NET RULES

NetName	Spacing	Width
AGPVREFCG	20MIL_G2G_30MIL	

NET	DIFFPAIR	NET_SPACING_RULE
PEX_TX0	PEX_TX0	20MIL_G2G_30MIL
PEX_TX0*	PEX_TX0	20MIL_G2G_30MIL
PEX_TX1	PEX_TX1	20MIL_G2G_30MIL
PEX_TX1*	PEX_TX1	20MIL_G2G_30MIL
PEX_TX2	PEX_TX2	20MIL_G2G_30MIL
PEX_TX2*	PEX_TX2	20MIL_G2G_30MIL
PEX_TX3	PEX_TX3	20MIL_G2G_30MIL
PEX_TX3*	PEX_TX3	20MIL_G2G_30MIL
PEX_TX4	PEX_TX4	20MIL_G2G_30MIL
PEX_TX4*	PEX_TX4	20MIL_G2G_30MIL
PEX_TX5	PEX_TX5	20MIL_G2G_30MIL
PEX_TX5*	PEX_TX5	20MIL_G2G_30MIL
PEX_TX6	PEX_TX6	20MIL_G2G_30MIL
PEX_TX6*	PEX_TX6	20MIL_G2G_30MIL
PEX_TX7	PEX_TX7	20MIL_G2G_30MIL
PEX_TX7*	PEX_TX7	20MIL_G2G_30MIL
PEX_TX8	PEX_TX8	20MIL_G2G_30MIL
PEX_TX8*	PEX_TX8	20MIL_G2G_30MIL
PEX_TX9	PEX_TX9	20MIL_G2G_30MIL
PEX_TX9*	PEX_TX9	20MIL_G2G_30MIL
PEX_TX10	PEX_TX10	20MIL_G2G_30MIL
PEX_TX10*	PEX_TX10	20MIL_G2G_30MIL
PEX_TX11	PEX_TX11	20MIL_G2G_30MIL
PEX_TX11*	PEX_TX11	20MIL_G2G_30MIL
PEX_TX12	PEX_TX12	20MIL_G2G_30MIL
PEX_TX12*	PEX_TX12	20MIL_G2G_30MIL
PEX_TX13	PEX_TX13	20MIL_G2G_30MIL
PEX_TX13*	PEX_TX13	20MIL_G2G_30MIL
PEX_TX14	PEX_TX14	20MIL_G2G_30MIL
PEX_TX14*	PEX_TX14	20MIL_G2G_30MIL
PEX_TX15	PEX_TX15	20MIL_G2G_30MIL
PEX_TX15*	PEX_TX15	20MIL_G2G_30MIL

NET	DIFFPAIR	NET_SPACING_RULE
NVVDD_SENSE	VDD_SENSE	10MIL
GND_SENSE	VDD_SENSE	10MIL

ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	NV43 PCI Express Interface

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7. GPU Frame Buffer A Interface

U7
U_GPU_G3
BGA820
COMMON

ALL FBVDD PINS ARE NC ON NV43 DESKTOP G3 PACKAGE

2/14 FBA

8<>	BI	FBAD<63..0>		
0	FBAD<0>	N27	FBAD0	
1	FBAD<1>	M27	FBAD1	
2	FBAD<2>	N28	FBAD2	
3	FBAD<3>	L29	FBAD3	
4	FBAD<4>	K27	FBAD4	
5	FBAD<5>	K28	FBAD5	
6	FBAD<6>	J29	FBAD6	
7	FBAD<7>	J28	FBAD7	
8	FBAD<8>	P30	FBAD8	
9	FBAD<9>	N31	FBAD9	
10	FBAD<10>	N30	FBAD10	
11	FBAD<11>	N32	FBAD11	
12	FBAD<12>	L31	FBAD12	
13	FBAD<13>	L30	FBAD13	
14	FBAD<14>	J30	FBAD14	
15	FBAD<15>	L32	FBAD15	
16	FBAD<16>	H30	FBAD16	
17	FBAD<17>	K30	FBAD17	
18	FBAD<18>	H31	FBAD18	
19	FBAD<19>	F30	FBAD19	
20	FBAD<20>	H32	FBAD20	
21	FBAD<21>	E31	FBAD21	
22	FBAD<22>	D30	FBAD22	
23	FBAD<23>	E30	FBAD23	
24	FBAD<24>	H28	FBAD24	
25	FBAD<25>	H29	FBAD25	
26	FBAD<26>	E29	FBAD26	
27	FBAD<27>	J27	FBAD27	
28	FBAD<28>	F27	FBAD28	
29	FBAD<29>	E27	FBAD29	
30	FBAD<30>	E28	FBAD30	
31	FBAD<31>	F28	FBAD31	
32	FBAD<32>	AD29	FBAD32	
33	FBAD<33>	AE29	FBAD33	
34	FBAD<34>	AD28	FBAD34	
35	FBAD<35>	AC28	FBAD35	
36	FBAD<36>	AB29	FBAD36	
37	FBAD<37>	AA30	FBAD37	
38	FBAD<38>	Y28	FBAD38	
39	FBAD<39>	AB30	FBAD39	
40	FBAD<40>	AM30	FBAD40	
41	FBAD<41>	AF30	FBAD41	
42	FBAD<42>	AJ31	FBAD42	
43	FBAD<43>	AJ30	FBAD43	
44	FBAD<44>	AJ32	FBAD44	
45	FBAD<45>	AK29	FBAD45	
46	FBAD<46>	AM31	FBAD46	
47	FBAD<47>	AL30	FBAD47	
48	FBAD<48>	AE32	FBAD48	
49	FBAD<49>	AE30	FBAD49	
50	FBAD<50>	AE31	FBAD50	
51	FBAD<51>	AD30	FBAD51	
52	FBAD<52>	AC31	FBAD52	
53	FBAD<53>	AC32	FBAD53	
54	FBAD<54>	AB32	FBAD54	
55	FBAD<55>	AB31	FBAD55	
56	FBAD<56>	AG27	FBAD56	
57	FBAD<57>	AF28	FBAD57	
58	FBAD<58>	AH28	FBAD58	
59	FBAD<59>	AG28	FBAD59	
60	FBAD<60>	AG29	FBAD60	
61	FBAD<61>	AD27	FBAD61	
62	FBAD<62>	AF27	FBAD62	
63	FBAD<63>	AE28	FBAD63	
8<>	OUT	FBADQM<7..0>		
0	FBADQM<0>	M29	FBADQM0	
1	FBADQM<1>	M30	FBADQM1	
2	FBADQM<2>	G30	FBADQM2	
3	FBADQM<3>	F29	FBADQM3	
4	FBADQM<4>	AA29	FBADQM4	
5	FBADQM<5>	AK30	FBADQM5	
6	FBADQM<6>	AC30	FBADQM6	
7	FBADQM<7>	AG30	FBADQM7	
8<>	BI	FBADQS_WP<7..0>		
0	FBADQS_WP<0>	L28	FBADQS_WP0	
1	FBADQS_WP<1>	K31	FBADQS_WP1	
2	FBADQS_WP<2>	G32	FBADQS_WP2	
3	FBADQS_WP<3>	G28	FBADQS_WP3	
4	FBADQS_WP<4>	AB28	FBADQS_WP4	
5	FBADQS_WP<5>	AL32	FBADQS_WP5	
6	FBADQS_WP<6>	AF32	FBADQS_WP6	
7	FBADQS_WP<7>	AH30	FBADQS_WP7	
8<>	BI	FBADQS_RN<7..0>		
0	FBADQS_RN<0>	M28	FBADQS_RN0	
1	FBADQS_RN<1>	K32	FBADQS_RN1	
2	FBADQS_RN<2>	G31	FBADQS_RN2	
3	FBADQS_RN<3>	G27	FBADQS_RN3	
4	FBADQS_RN<4>	AA28	FBADQS_RN4	
5	FBADQS_RN<5>	AL31	FBADQS_RN5	
6	FBADQS_RN<6>	AF31	FBADQS_RN6	
7	FBADQS_RN<7>	AH29	FBADQS_RN7	

FBVDD	A12	NTP_GPU_A12
FBVDD	A15	NTP_GPU_A15
FBVDD	A18	NTP_GPU_A18
FBVDD	A21	NTP_GPU_A21
FBVDD	A24	NTP_GPU_A24
FBVDD	A27	NTP_GPU_A27
FBVDD	A3	NTP_GPU_A3
FBVDD	A30	NTP_GPU_A30
FBVDD	A6	NTP_GPU_A6
FBVDD	A9	NTP_GPU_A9
FBVDD	AA32	NTP_GPU_AA32
FBVDD	AD32	NTP_GPU_AD32
FBVDD	AG32	NTP_GPU_AG32
FBVDD	AK32	NTP_GPU_AK32
FBVDD	C32	NTP_GPU_C32
FBVDD	F32	NTP_GPU_F32
FBVDD	J32	NTP_GPU_J32
FBVDD	M32	NTP_GPU_M32
FBVDD	R32	NTP_GPU_R32
FBVDD	V32	NTP_GPU_V32
FBVDDQ	AA25	
FBVDDQ	AA26	
FBVDDQ	AB25	
FBVDDQ	AB26	
FBVDDQ	G11	
FBVDDQ	G12	
FBVDDQ	G15	
FBVDDQ	G18	
FBVDDQ	G21	
FBVDDQ	G22	
FBVDDQ	H11	
FBVDDQ	H12	
FBVDDQ	H15	
FBVDDQ	H18	
FBVDDQ	H21	
FBVDDQ	H22	
FBVDDQ	L25	
FBVDDQ	L26	
FBVDDQ	M25	
FBVDDQ	M26	
FBVDDQ	R25	
FBVDDQ	R26	
FBVDDQ	V25	
FBVDDQ	V26	

FBA_CMD0	P32	FBA_CMD<0>	0	
FBA_CMD1	U27	FBA_CMD<1>	1	
FBA_CMD2	P31	FBA_CMD<2>	2	
FBA_CMD3	U30	FBA_CMD<3>	3	
FBA_CMD4	Y31	FBA_CMD<4>	4	
FBA_CMD5	W32	FBA_CMD<5>	5	
FBA_CMD6	W31	FBA_CMD<6>	6	
FBA_CMD7	T32	NTP_FBA_CMD<7>		
FBA_CMD8	V27	FBA_CMD<8>	8	
FBA_CMD9	T28	FBA_CMD<9>	9	
FBA_CMD10	T31	FBA_CMD<10>	10	
FBA_CMD11	U32	FBA_CMD<11>	11	
FBA_CMD12	W29	FBA_CMD<12>	12	
FBA_CMD13	W30	FBA_CMD<13>	13	
FBA_CMD14	T27	FBA_CMD<14>	14	
FBA_CMD15	V28	FBA_CMD<15>	15	
FBA_CMD16	V30	FBA_CMD<16>	16	
FBA_CMD17	U31	FBA_CMD<17>	17	
FBA_CMD18	R27	FBA_CMD<18>	18	
FBA_CMD19	V29	FBA_CMD<19>	19	
FBA_CMD20	T30	FBA_CMD<20>	20	
FBA_CMD21	W28	FBA_CMD<21>	21	
FBA_CMD22	R29	FBA_CMD<22>	22	
FBA_CMD23	R30	FBA_CMD<23>	23	
FBA_CMD24	P29	FBA_CMD<24>	24	
FBA_CMD25	U28	FBA_CMD<25>	25	
FBA_CMD26	Y32	NTP_FBA_CMD<26>		

6.5MIL
FBA_CMD<26..0> OUT 8<

FBA_CLK0	P28	FBA_CLK0	OUT 8<
FBA_CLK0	R28	FBA_CLK0*	OUT 8<
FBA_CLK1	Y27	FBA_CLK1	OUT 8<
FBA_CLK1	AA27	FBA_CLK1*	OUT 8<

RFU	Y30	TP_FBA_DBI0	
RFU	AC26	TP_FBA_DBI1	
FBA_DEBUG	AC27	TP_FBA_DEBUG	
FBA_REFCLK	D32	FBA_REFCLK	
FBA_REFCLK	D31	FBA_REFCLK*	
FBA_PLLVDD	G23	FBA_PLLVDD	
FBA_PLLAVDD	G25	FBA_PLLAVDD	
FBA_PLLGND	G24		

TP NOW

PLACE close to GPU

FBVDD
R612 2.2K 5% 0402 NO STUFF
R608 2.2K 5% 0402 NO STUFF
R615 2.2K 5% 0402 COMMON
R610 2.2K 5% 0402 COMMON
GND

PLACE BELOW GPU

FBVDD
C747 0.47UF 6.3V 10% X5R 0402 COMMON
C845 0.47UF 6.3V 10% X5R 0402 COMMON
C733 .1UF 10V 10% X5R 0402 COMMON
C828 .1UF 10V 10% X5R 0402 COMMON
C54 .1UF 10V 10% X5R 0402 COMMON
GND
C36 .1UF 10V 10% X5R 0402 COMMON
C29 .1UF 10V 10% X5R 0402 COMMON
C723 1UF 10V 10% X7R 0603 COMMON
C57 .1UF 10V 10% X5R 0402 COMMON
GND
C806 0.47UF 6.3V 10% X5R 0402 COMMON
C762 0.47UF 6.3V 10% X5R 0402 COMMON
C839 .1UF 10V 10% X5R 0402 COMMON
C759 .1UF 10V 10% X5R 0402 COMMON
C834 1UF 10V 10% X7R 0603 COMMON
GND
C742 .1UF 10V 10% X5R 0402 COMMON
C801 .1UF 10V 10% X5R 0402 COMMON
C817 .1UF 10V 10% X5R 0402 COMMON
C807 0.47UF 6.3V 10% X5R 0402 COMMON
C735 0.47UF 6.3V 10% X5R 0402 COMMON
GND

NET	DIFFPAIR	MIN_LINE_WIDTH	NET_SPACING_RULE
IN FBA_REFCLK		4MIL	10MIL
IN FBA_REFCLK*		4MIL	10MIL
IN FBA_PLLVDD		10MIL	
IN FBA_PLLAVDD		10MIL	

PLACE MIDWAY BETWEEN GPU AND MEMORY

FBVDD
C715 10UF 20% X5R 0805 COMMON
C628 10UF 20% X5R 0805 COMMON
C861 10UF 20% X5R 0805 COMMON
C906 10UF 20% X5R 0805 COMMON
GND

PLACE NEAR GPU

FBVDD
R582 10K 5% 0402 NO STUFF
FBA_CMD<11>
R581 10K 5% 0402 COMMON
GND

CKE Stuff options for DDR3 confiqation for on-die terminations at the memory
IMPORTANT FOR POWER ON INITIALIZATION OF DDR3 MEMS

DDR3: DETERMINES THE ODT VALUE FOR ADDR AND CONTROL PINS
CKE = 0 --> ODT = ZQ/2
CKE = 1 --> ODT = ZQ

FB_DLLVDD
ON NV3x version's of G3
FB_DLLVDD will be routed on FB_PLLVDD

PLACE close to balls

FBA_PLLVDD
150-220R@100MHz
LB514 BEAD_0603 COMMON
A3V3
C810 .01UF 16V 10% X7R 0402 COMMON
C816 .1UF 10V 10% X5R 0402 COMMON
C822 1UF 6.3V 10% X5R 0402 COMMON
C830 4.7UF 6.3V 10% X5R 0603 COMMON
GND

NVDD
150-220R@100MHz
LB512 BEAD_0603 COMMON
C778 .01UF 16V 10% X7R 0402 COMMON
C777 .1UF 10V 10% X5R 0402 COMMON
C805 1UF 6.3V 10% X5R 0402 COMMON
C788 4.7UF 6.3V 10% X5R 0603 COMMON
GND

FBA_AVDD is TBD. This may not be hooked up on the Package.

FBVDD
R607 1K 1% 0402 COMMON
Rtop
C769 .1UF 10V 10% X5R 0402 NS
R606 2.37K 1% 0402 COMMON
Rbot
C765 .1UF 10V 10% X5R 0402 COMMON
FBA_VREF E32 FB_VREF1
GND

VREF = FBVDDQ * Rbot/(Rtop + Rbot)

VREF = 0.70 * FBVDDQ
DDR3: 1.26V = 1.8V * 2.7K/(1.15K + 2.7K)

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ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	GPU Frame Buffer A Interface

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8. GPU Frame Buffer A Bank 0

A-CSO-LOW-32bit

U8
DDR3BGA144
BGA144
VERSION=BGA144
COMMON

8< 7> IN FBA_CMD<26..0>

15	FBA_CMD<15>	M5	RAS
25	FBA_CMD<25>	N6	CAS
9	FBA_CMD<9>	N9	WE
8 CS0	FBA_CMD<8>	M10	CS
1	FBA_CMD<1>	N2	A0
3	FBA_CMD<3>	N3	A1
0 FBA_CMD<0>		L3	A2
24 FBA_CMD<24>		L12	A3
22 FBA_CMD<22>		M12	A4
21	FBA_CMD<21>	N12	A5
23	FBA_CMD<23>	N13	A6
19	FBA_CMD<19>	N11	A7
20	FBA_CMD<20>	M11	A8
17	FBA_CMD<17>	M4	A9
16	FBA_CMD<16>	N4	A10
14	FBA_CMD<14>	L9	A11
			NC/A<12>
10	FBA_CMD<10>	N5	BA<0>
18	FBA_CMD<18>	N10	BA<1>
	TP_FBA0_BA<2>	L6	NC/BA<2>
11	FBA_CMD<11>	M7	CKE
8< 7> IN	FBA_CLK0	N7	CLK
8< 7> IN	FBA_CLK0*	N8	CLK
	TP_FBA0_NC1	E3	NC/RFU
	TP_FBA0_NC2	E12	NC/RFU
	TP_FBA0_NC3	M8	NC/RFU
12	FBA_CMD<12>	M6	RESET
	FBA_ZQ0	M9	ZQ

Low Sub-Partition

R554 10K 5% 0402 COMMON
R58 240 1% 0603 COMMON
GND GND

DDR3: ZQ = 6x desired output
impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

THERM: F6 F7 F8 F9 G6 G7 G8 G9 H6 H7 H8 H9 J6 J7 J8 J9

VDD: D7 D8 E4 E11 L4 L7 L8 L11
VDDQ: C4 C5 C7 C8 C10 C11 F4 F11 G4 G11 H4 H11 J4 J11 K4 K11
VSS: B4 B11 D4 D5 D6 D9 D10 D11 E6 E9 F5 F10 G5 G10 H5 H10 J5 J10 K5 K10 E5 E7 E8 E10 K6 K7 K8 K9 L5 L10
VREF: M2 FBA_VREF_DATA0, M13 FBA_VREF_ADDR0

FBVDD
GND

VREF:
M2 - DATA
M13 - ADDR

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 2.7K/(1.15K + 2.7K)

FBA Partition

Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!

FBA_CMD<26..0>

2	FBA_CMD<2>	120	R574
0	FBA_CMD<0>	120	R576
24	FBA_CMD<24>	120	R578
22	FBA_CMD<22>	120	R577
13	FBA_CMD<13>	120	R561
4	FBA_CMD<4>	120	R562
5	FBA_CMD<5>	120	R568
6	FBA_CMD<6>	120	R567
	FBA_CLK0	60.4	R60
	FBA_CLK0*	60.4	R59
	FBA_CLK1	60.4	R63
	FBA_CLK1*	60.4	R62

COMMON 1% 0402

HI Sub-Partition

FBVDD

R571 1K 1% 0402 COMMON
C621 .1UF 10V 10% X5R 0402 NO STUFF
R572 2.37K 1% 0402 COMMON
C624 .1UF 10V 10% X5R 0402 COMMON
R580 1K 1% 0402 COMMON
C691 .1UF 10V 10% X5R 0402 NO STUFF
R579 2.37K 1% 0402 COMMON
C686 .1UF 10V 10% X5R 0402 COMMON
GND

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 2.7K/(1.15K + 2.7K)

A-CSO-HI-32bit

U10
DDR3BGA144
PACK_TYPE=BGA144
VERSTION=BGA144
COMMON

FBA_CMD<26..0>

15	FBA_CMD<15>	M5	RAS
25	FBA_CMD<25>	N6	CAS
9	FBA_CMD<9>	N9	WE
8 CS0	FBA_CMD<8>	M10	CS
1	FBA_CMD<1>	N2	A0
3	FBA_CMD<3>	N3	A1
13	FBA_CMD<13>	M3	A2
4	FBA_CMD<4>	L3	A3
5	FBA_CMD<5>	L12	A4
6	FBA_CMD<6>	M12	A5
21	FBA_CMD<21>	N12	A6
23	FBA_CMD<23>	N13	A7
19	FBA_CMD<19>	N11	A8
20	FBA_CMD<20>	M11	A9
17	FBA_CMD<17>	M4	A10
16	FBA_CMD<16>	N4	A11
14	FBA_CMD<14>	L9	NC/A<12>
10	FBA_CMD<10>	N5	BA<0>
18	FBA_CMD<18>	N10	BA<1>
	TP_FBA1_BA<2>	L6	NC/BA<2>
11	FBA_CMD<11>	M7	CKE
8< 7> IN	FBA_CLK1	N7	CLK
8< 7> IN	FBA_CLK1*	N8	CLK
	TP_FBA1_NC1	E3	NC/RFU
	TP_FBA1_NC2	E12	NC/RFU
	TP_FBA1_NC3	M8	NC/RFU
	FBA_CMD<12>	M6	RESET
	FBA_ZQ1	M9	ZQ

R61 240 1% 0603 COMMON
GND

DDR3: ZQ = 6x desired output
impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

THERM: F6 F7 F8 F9 G6 G7 G8 G9 H6 H7 H8 H9 J6 J7 J8 J9

VDD: D7 D8 E4 E11 L4 L7 L8 L11
VDDQ: C4 C5 C7 C8 C10 C11 F4 F11 G4 G11 H4 H11 J4 J11 K4 K11
VSS: B4 B11 D4 D5 D6 D9 D10 D11 E6 E9 F5 F10 G5 G10 H5 H10 J5 J10 K5 K10 E5 E7 E8 E10 K6 K7 K8 K9 L5 L10
VREF: M2 FBA_VREF_DATA1, M13 FBA_VREF_ADDR1

FBVDD
GND

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 2.7K/(1.15K + 2.7K)

R552 1K 1% 0402 COMMON
C548 .1UF 10V 10% X5R 0402 NO STUFF
R555 2.37K 1% 0402 COMMON
C550 .1UF 10V 10% X5R 0402 COMMON
R570 1K 1% 0402 COMMON
C606 .1UF 10V 10% X5R 0402 NO STUFF
R569 2.37K 1% 0402 COMMON
C597 .1UF 10V 10% X5R 0402 COMMON
GND

NET	DIFFPAIR		
8< 7> IN FBA_CLK0	FBA_CLK0	5.5MIL	20MIL
8< 7> IN FBA_CLK0*	FBA_CLK0	5.5MIL	20MIL
8< 7> IN FBA_CLK1	FBA_CLK1	5.5MIL	20MIL
8< 7> IN FBA_CLK1*	FBA_CLK1	5.5MIL	20MIL
8< 7> IN FBA_CMD<26..0>		6.5MIL	15MIL
8<> 7<> B1 FBAD<63..0>		6.5MIL	15MIL
8<> 7<> B1 FBADQM<7..0>		6.5MIL	15MIL
8<> 7<> B1 FBADQS_RN<0>	FBADQS_RN0	6.5MIL	15MIL
8<> 7<> B1 FBADQS_WP<0>	FBADQS_RN0	6.5MIL	15MIL
8<> 7<> B1 FBADQS_RN<1>	FBADQS_RN1	6.5MIL	15MIL
8<> 7<> B1 FBADQS_WP<1>	FBADQS_RN1	6.5MIL	15MIL
8<> 7<> B1 FBADQS_RN<2>	FBADQS_RN2	6.5MIL	15MIL
8<> 7<> B1 FBADQS_WP<2>	FBADQS_RN2	6.5MIL	15MIL
8<> 7<> B1 FBADQS_RN<3>	FBADQS_RN3	6.5MIL	15MIL
8<> 7<> B1 FBADQS_WP<3>	FBADQS_RN3	6.5MIL	15MIL
8<> 7<> B1 FBADQS_RN<4>	FBADQS_RN4	6.5MIL	15MIL
8<> 7<> B1 FBADQS_WP<4>	FBADQS_RN4	6.5MIL	15MIL
8<> 7<> B1 FBADQS_RN<5>	FBADQS_RN5	6.5MIL	15MIL
8<> 7<> B1 FBADQS_WP<5>	FBADQS_RN5	6.5MIL	15MIL
8<> 7<> B1 FBADQS_RN<6>	FBADQS_RN6	6.5MIL	15MIL
8<> 7<> B1 FBADQS_WP<6>	FBADQS_RN6	6.5MIL	15MIL
8<> 7<> B1 FBADQS_RN<7>	FBADQS_RN7	6.5MIL	15MIL
8<> 7<> B1 FBADQS_WP<7>	FBADQS_RN7	6.5MIL	15MIL
B1 FBA_VREF_DATA0		12MIL	
B1 FBA_VREF_ADDR0		12MIL	
B1 FBA_VREF_DATA1		12MIL	
B1 FBA_VREF_ADDR1		12MIL	

144BGA CMD Mapping

CMD	ADDR
CMD15	BA5*
CMD25	CAS*
CMD9	WE*
CMD11	CKE
CMD12	RESET
CMD8	CS0*
CMD7	CS1**notused
CMD1	A<0>
CMD3	A<1>
CMD2	A<2>
CMD0	A<3> — Low Sub-Partition
CMD24	A<4>
CMD22	A<5>
CMD13	A<2>
CMD4	A<3> — HI Sub-Partition
CMD5	A<4>
CMD6	A<5>
CMD21	A<6>
CMD23	A<7>
CMD19	A<8>
CMD20	A<9>
CMD17	A<10
CMD16	A<11>
CMD14	A<12>
CMD10	BA0
CMD18	BA1

8<> 7<> B1 FBAD<63..0>

8<> 7<> B1 FBADQM<7..0>
8<> 7<> B1 FBADQS_RN<7..0>
8<> 7<> B1 FBADQS_WP<7..0>

U8 DDR3BGA144 BGA144 VERSION=BGA144 COMMON
U10 DDR3BGA144 BGA144 VERSION=BGA144 COMMON

	U8	U8	U8	U8	U10	U10	U10	U10
DQ0	FBAD<0> L2	FBAD<8> E2	FBAD<16> B10	FBAD<24> F12	FBAD<32> G12	FBAD<40> D2	FBAD<48> B9	FBAD<56> L2
DQ1	FBAD<1> K2	FBAD<9> D2	FBAD<17> B8	FBAD<25> G12	FBAD<33> L13	FBAD<41> B7	FBAD<49> B8	FBAD<57> F3
DQ2	FBAD<2> G2	FBAD<10> C2	FBAD<18> B9	FBAD<26> G13	FBAD<34> K12	FBAD<42> B6	FBAD<50> C9	FBAD<58> G2
DQ3	FBAD<3> J2	FBAD<11> D3	FBAD<19> C13	FBAD<27> F13	FBAD<35> J13	FBAD<43> B5	FBAD<51> B10	FBAD<59> K2
DQ4	FBAD<4> F2	FBAD<12> B5	FBAD<20> C9	FBAD<28> J13	FBAD<36> G13	FBAD<44> C6	FBAD<52> D12	FBAD<60> F2
DQ5	FBAD<5> J3	FBAD<13> B6	FBAD<21> D12	FBAD<29> K12	FBAD<37> K13	FBAD<45> E2	FBAD<53> C13	FBAD<61> K3
DQ6	FBAD<6> G3	FBAD<14> B7	FBAD<22> E13	FBAD<30> L13	FBAD<38> F12	FBAD<46> D3	FBAD<54> D13	FBAD<62> J2
DQ7	FBAD<7> K3	FBAD<15> C6	FBAD<23> D13	FBAD<31> K13	FBAD<39> F13	FBAD<47> C2	FBAD<55> E13	FBAD<63> G3
DQM	FBADQM<0> J3	FBADQM<1> C3	FBADQM<2> C12	FBADQM<3> J12	FBADQM<4> J12	FBADQM<5> C3	FBADQM<6> C12	FBADQM<7> J3
DQSR	FBADQS_RN<0> H3	FBADQS_RN<1> B12	FBADQS_RN<2> B13	FBADQS_RN<3> H12	FBADQS_RN<4> H12	FBADQS_RN<5> B3	FBADQS_RN<6> B12	FBADQS_RN<7> H3
DQSW	FBADQS_WP<0> H2	FBADQS_WP<1> B2	FBADQS_WP<2> B13	FBADQS_WP<3> H13	FBADQS_WP<4> H13	FBADQS_WP<5> B2	FBADQS_WP<6> B13	FBADQS_WP<7> H2

ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	GPU Frame Buffer A Bank 0

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2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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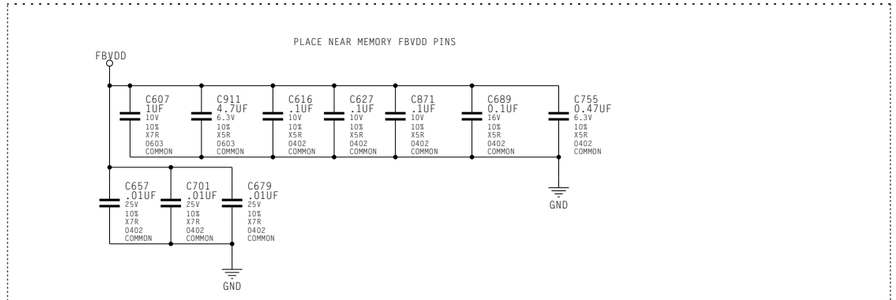
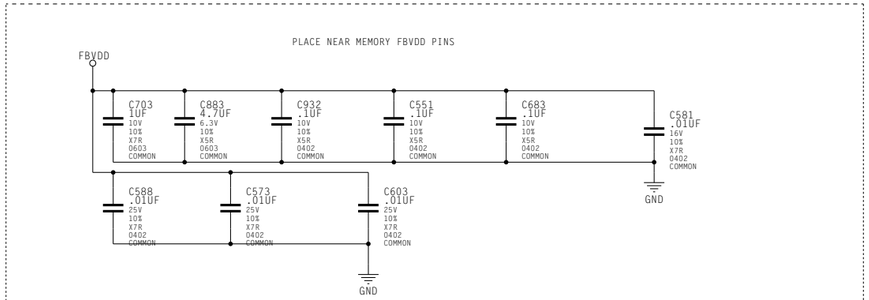
ID	p218_a02	PAGE	8 OF 31
NAME	fwynhamer	DATE	27-SEP-2004

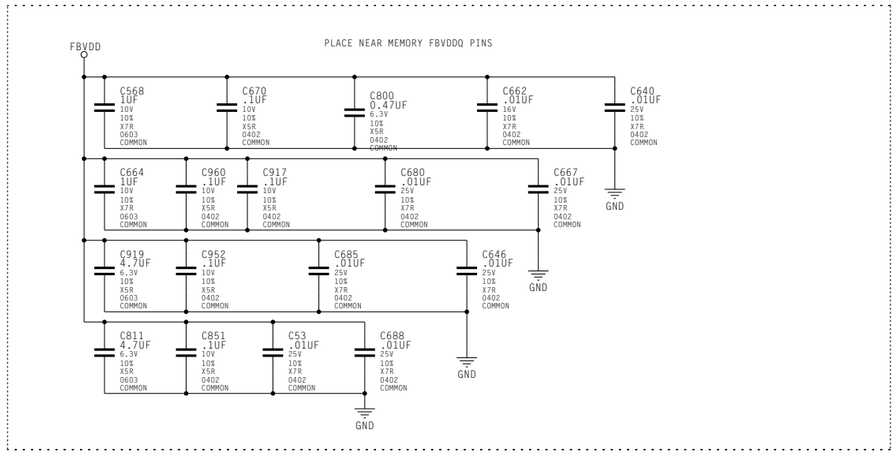
9. FRAME BUFFER: PARTITION A DECOUPLING

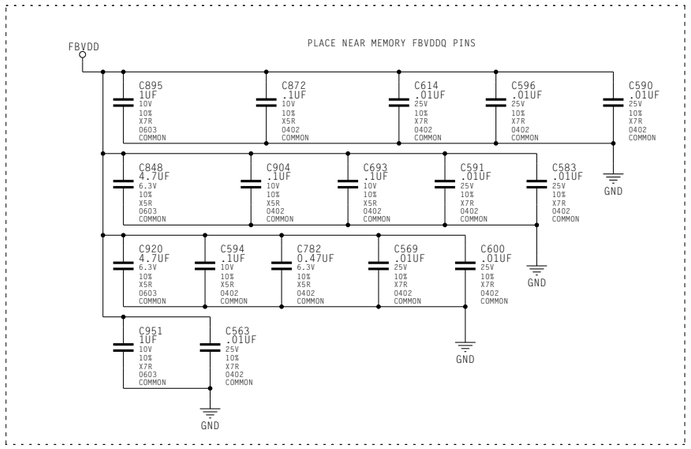
Decoupling for FBA 0..31



Decoupling for FBA 32..63







ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	Decoupling - Frame Buffer A

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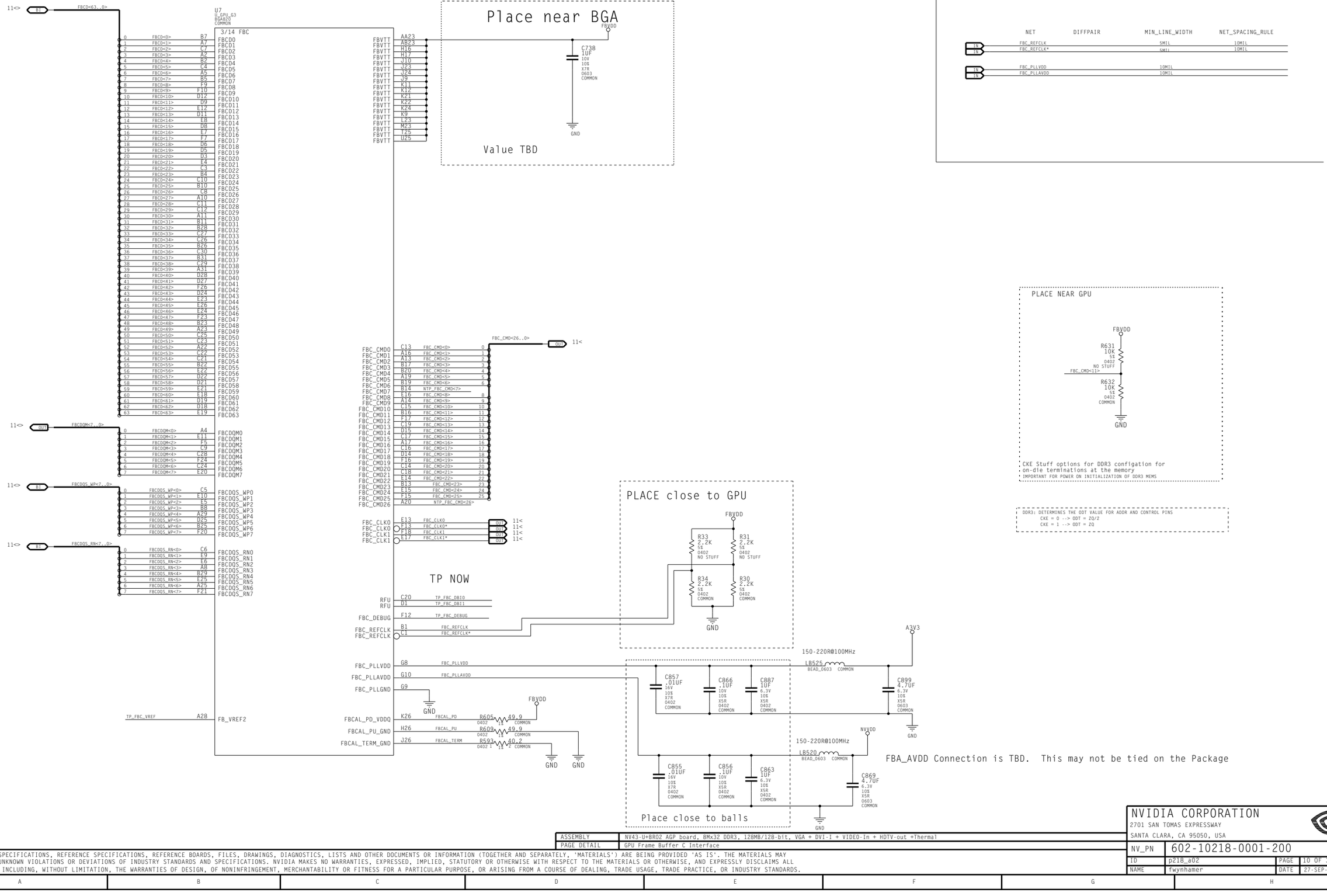
10. GPU Frame Buffer C Interface



ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	GPU Frame Buffer C Interface

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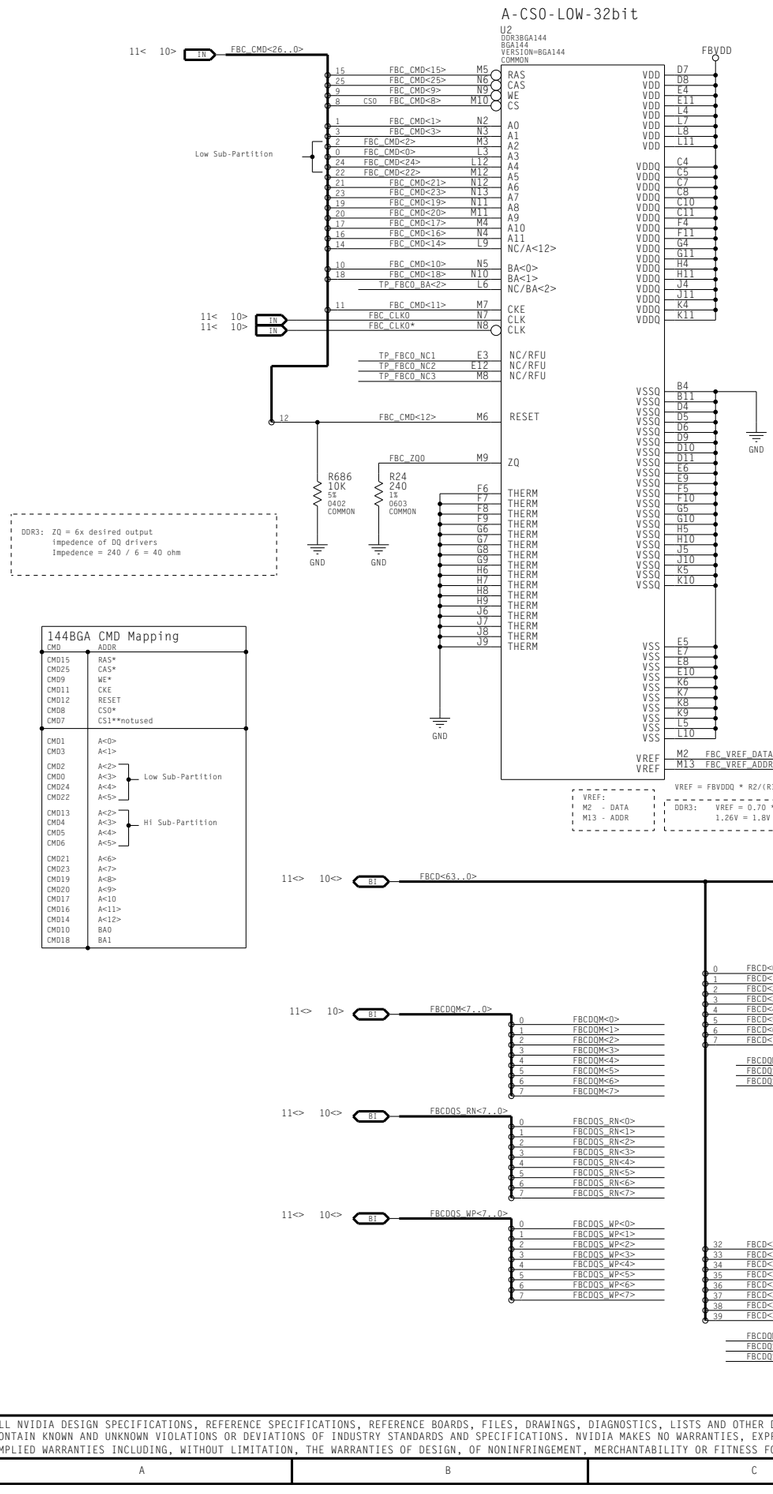
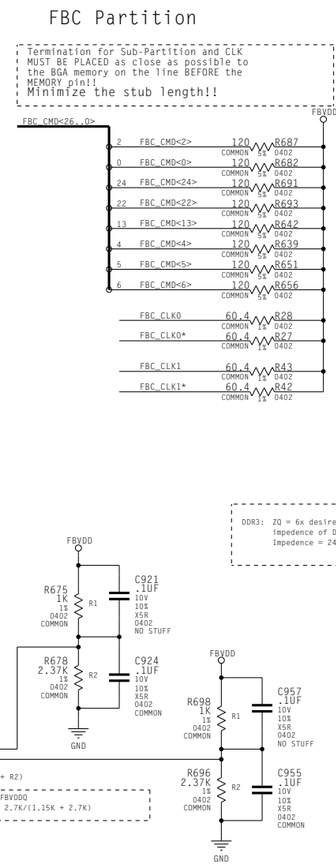
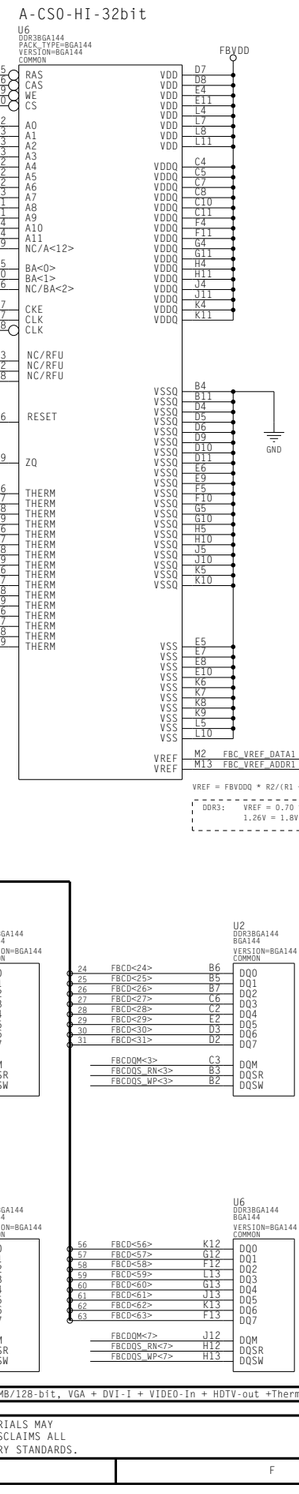
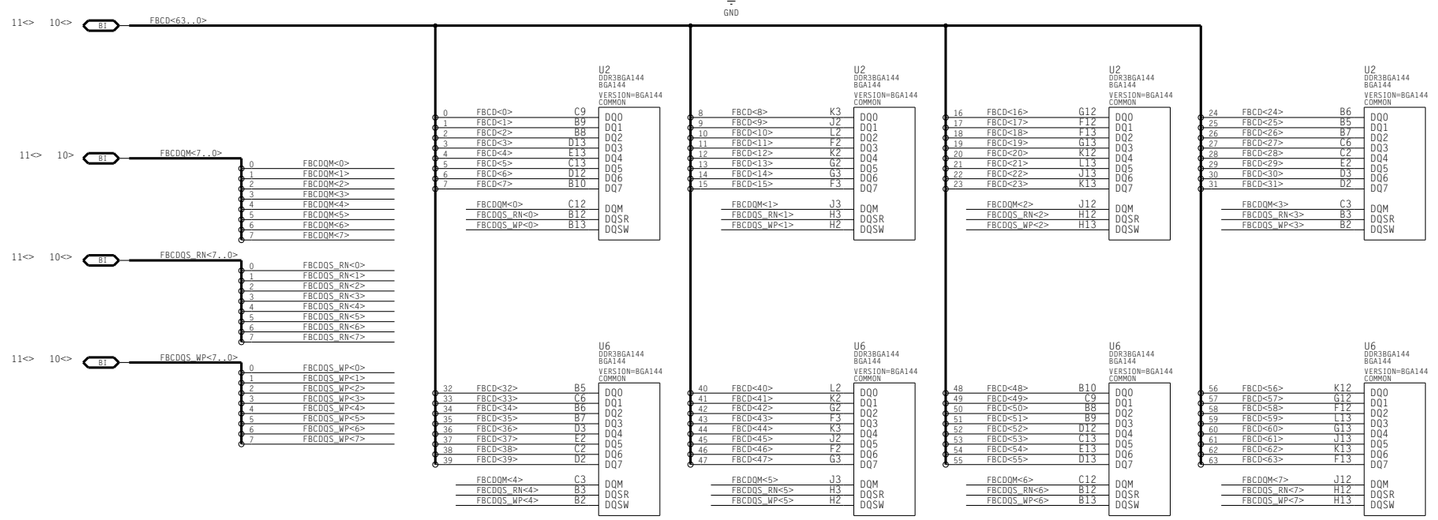
11. FRAMEBUFFER: PARTITION C 8Mx32 BGA144 DDR3







NET	DIFFPAIR	MIN_LINE_WIDTH	SPACING
FBC_CLK0	FBC_CLK0	5.5MIL	20MIL
FBC_CLK0*	FBC_CLK0	5.5MIL	20MIL
FBC_CLK1	FBC_CLK1	5.5MIL	20MIL
FBC_CLK1*	FBC_CLK1	5.5MIL	20MIL
FBC_CMD<26..0>			15MIL
FBCD<63..0>		6.5MIL	15MIL
FBCDQM<7..0>		6.5MIL	15MIL
FBCDQS_RN<0>	FBCDQS_RN0	6.5MIL	15MIL
FBCDQS_WP<0>	FBCDQS_RN0	6.5MIL	15MIL
FBCDQS_RN<1>	FBCDQS_RN1	6.5MIL	15MIL
FBCDQS_WP<1>	FBCDQS_RN1	6.5MIL	15MIL
FBCDQS_RN<2>	FBCDQS_RN2	6.5MIL	15MIL
FBCDQS_WP<2>	FBCDQS_RN2	6.5MIL	15MIL
FBCDQS_RN<3>	FBCDQS_RN3	6.5MIL	15MIL
FBCDQS_WP<3>	FBCDQS_RN3	6.5MIL	15MIL
FBCDQS_RN<4>	FBCDQS_RN4	6.5MIL	15MIL
FBCDQS_WP<4>	FBCDQS_RN4	6.5MIL	15MIL
FBCDQS_RN<5>	FBCDQS_RN5	6.5MIL	15MIL
FBCDQS_WP<5>	FBCDQS_RN5	6.5MIL	15MIL
FBCDQS_RN<6>	FBCDQS_RN6	6.5MIL	15MIL
FBCDQS_WP<6>	FBCDQS_RN6	6.5MIL	15MIL
FBCDQS_RN<7>	FBCDQS_RN7	6.5MIL	15MIL
FBCDQS_WP<7>	FBCDQS_RN7	6.5MIL	15MIL
FBC_VREF_DATA0		12MIL	
FBC_VREF_ADDR0		12MIL	
FBC_VREF_DATA1		12MIL	
FBC_VREF_ADDR1		12MIL	



ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	GPU Frame Buffer C Bank 0

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SANTA CLARA, CA 95050, USA

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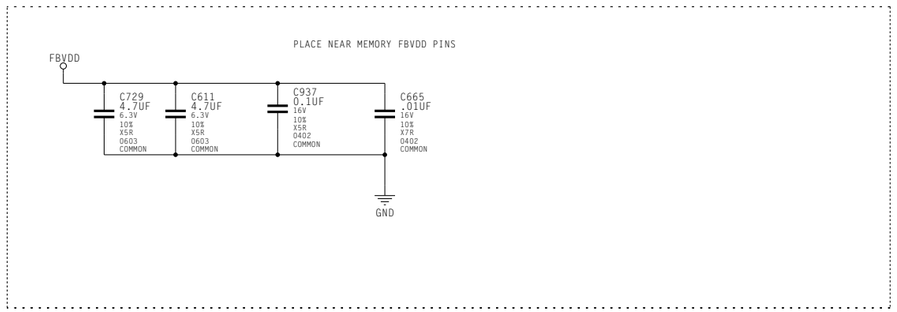
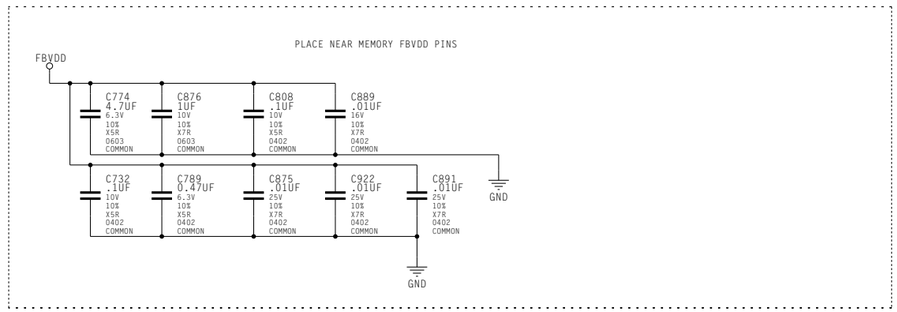
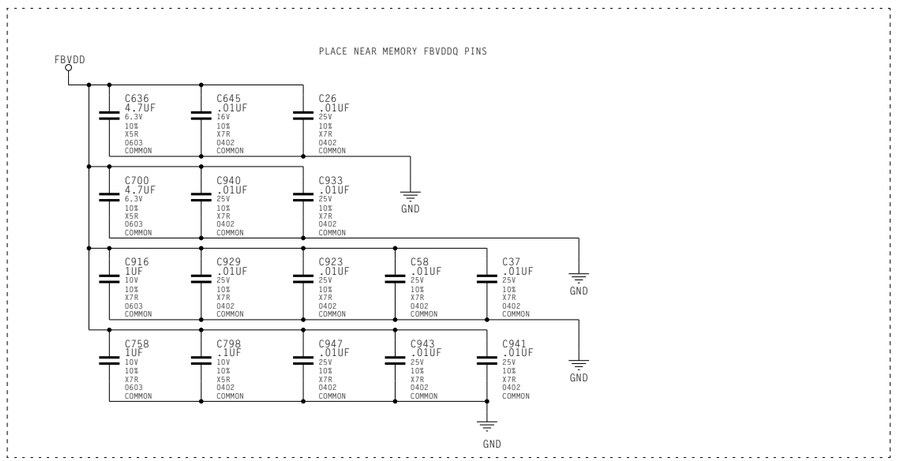
12. FRAMEBUFFER: PARTITION C DECOUPLING

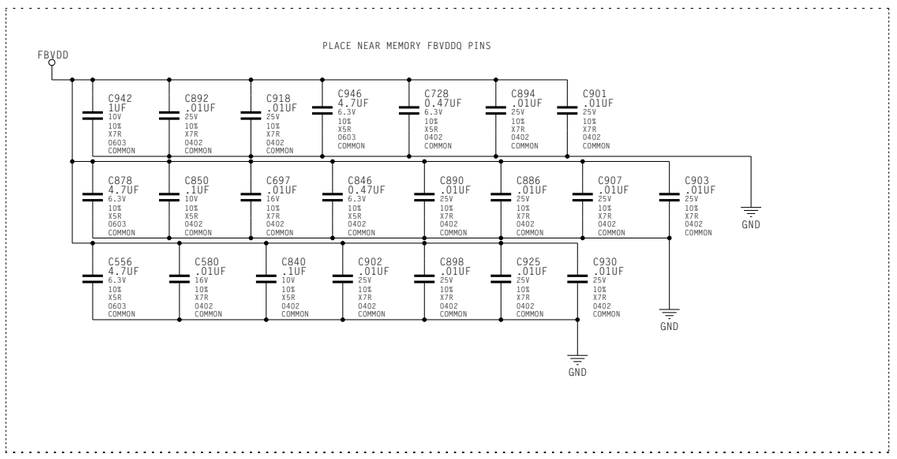
Decoupling for FBC 0..31



Decoupling for FBC 32..63







ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	Decoupling - Frame Buffer C

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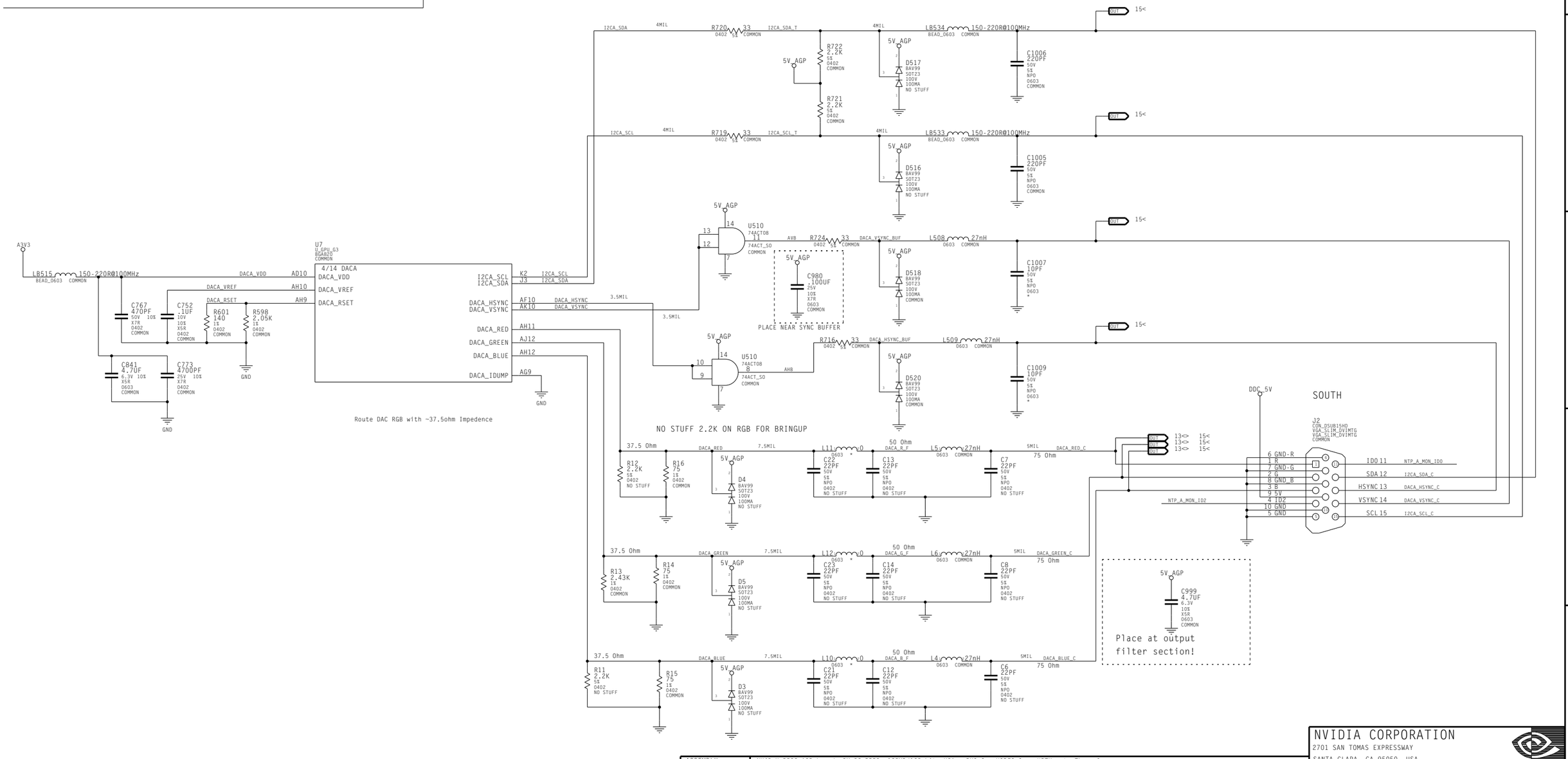
Primary Display (DACA), Slim DB15

DACA RGB-FILTER

NET_NAME	NET_SPACING_RULE	IMPEDANCE	MIN_LINE_WIDTH
DACA_VDD			12MIL
DACA_VREF			12MIL
DACA_RSET			12MIL
DACA_RED	20MIL		
DACA_GREEN	20MIL		
DACA_BLUE	20MIL		
DACA_R_F	20MIL		
DACA_G_F	20MIL		
DACA_B_F	20MIL		
DACA_RED_C	20MIL		
DACA_GREEN_C	20MIL		
DACA_BLUE_C	20MIL		



ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	DACA Primary Display with Connector

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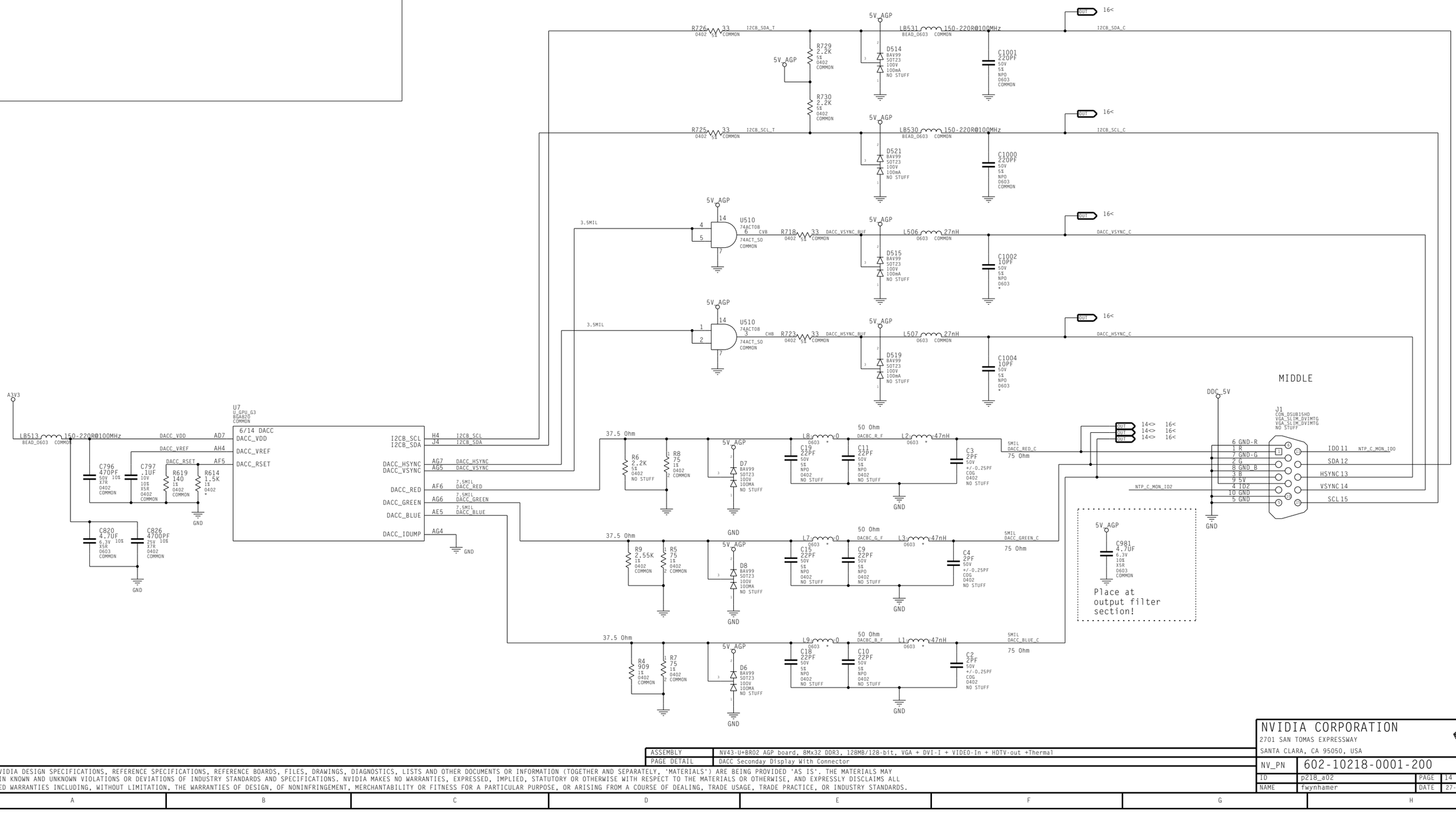
Secondary Display (DACC), Slim DB15

DACC RGB-FILTER

NET_NAME	NET_SPACING_RULE	IMPEDANCE	MIN_LINE_WIDTH
DACC_VDD			12MIL
DACC_VREF			12MIL
DACC_RSET			12MIL
DACC_RED	20MIL	U7.AF6:88.1:37.50 ohm:2 %	
DACC_GREEN	20MIL	U7.AG6:85.1:37.50 ohm:2 %	
DACC_BLUE	20MIL	U7.AE5:87.1:37.50 ohm:2 %	
DACBC_R_F	20MIL	L8.2:L2.1:50.00 ohm:2 %	
DACBC_G_F	20MIL	L7.2:L3.1:50.00 ohm:2 %	
DACBC_B_F	20MIL	L9.2:L1.1:50.00 ohm:2 %	
DACC_RED_C	20MIL	L2.2:J1.1:75.00 ohm:2 %	
DACC_GREEN_C	20MIL	L3.2:J1.2:75.00 ohm:2 %	
DACC_BLUE_C	20MIL	L1.2:J1.3:75.00 ohm:2 %	



ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	DACC Seconday Display With Connector

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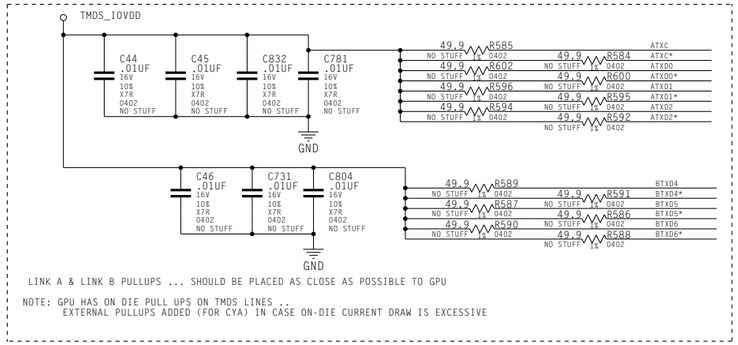
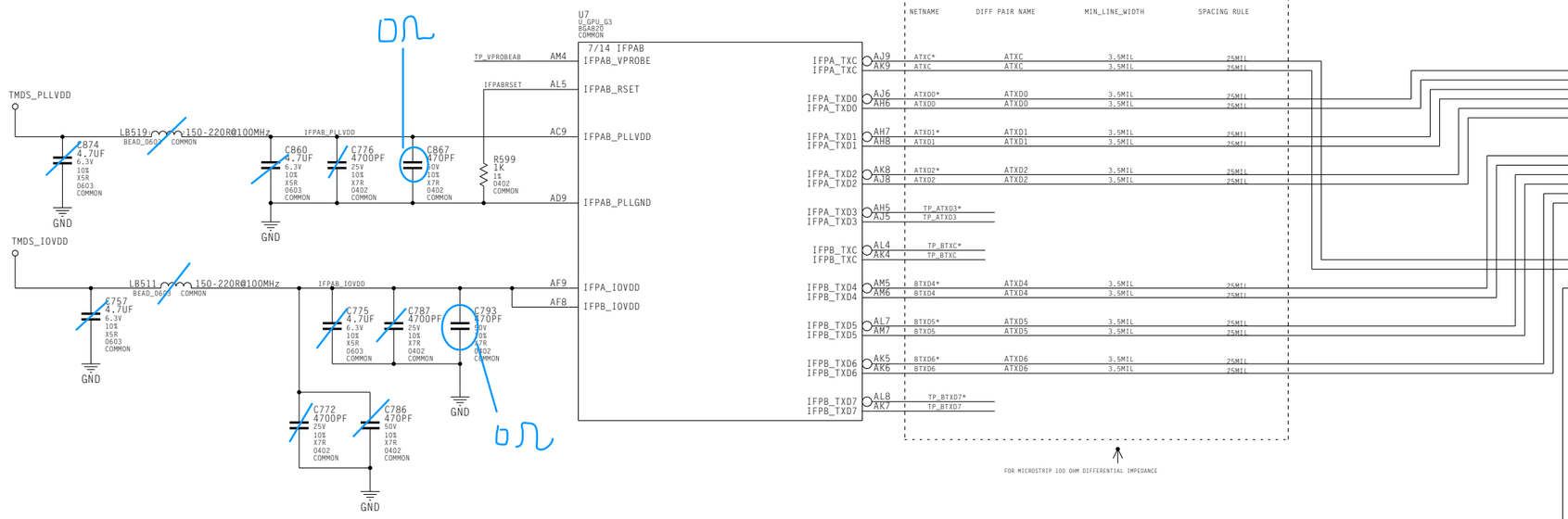
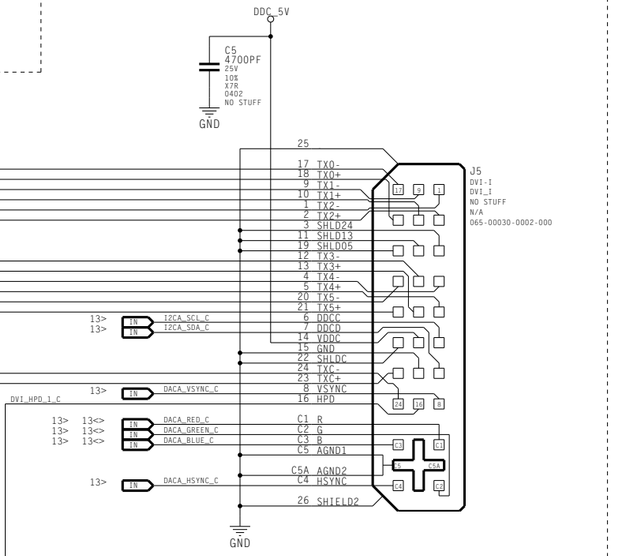
INTERNAL TMDS .. LINK A & B
SOUTH



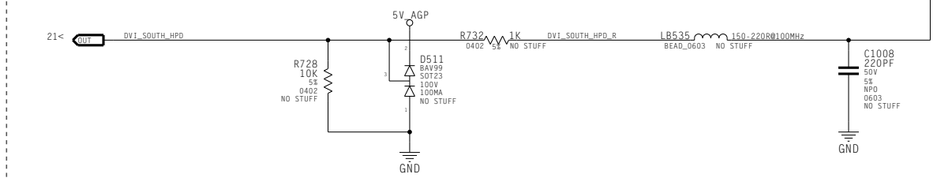
LINK A & LINK B PULLUPS ... SHOULD BE PLACED AS CLOSE AS POSSIBLE TO GPU

NOTE: GPU HAS ON DIE PULL UPS ON TMDS LINES ..
EXTERNAL PULLUPS ADDED (FOR CYA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE





Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
IFPAB_PLLVDD	12MIL	3.3V
IFPAB_IOVDD	12MIL	3.3V
IFPABRSET	12MIL	

ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	Internal TMDS - Link A-B with DVI-I Connector

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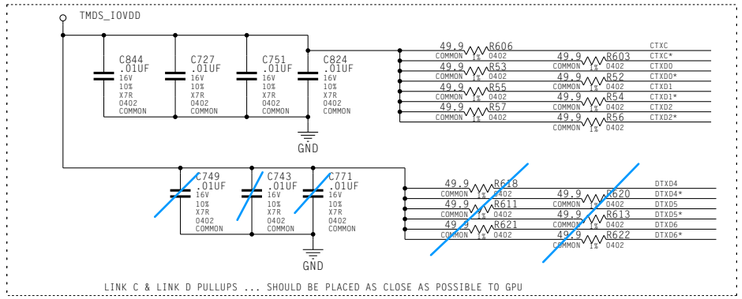
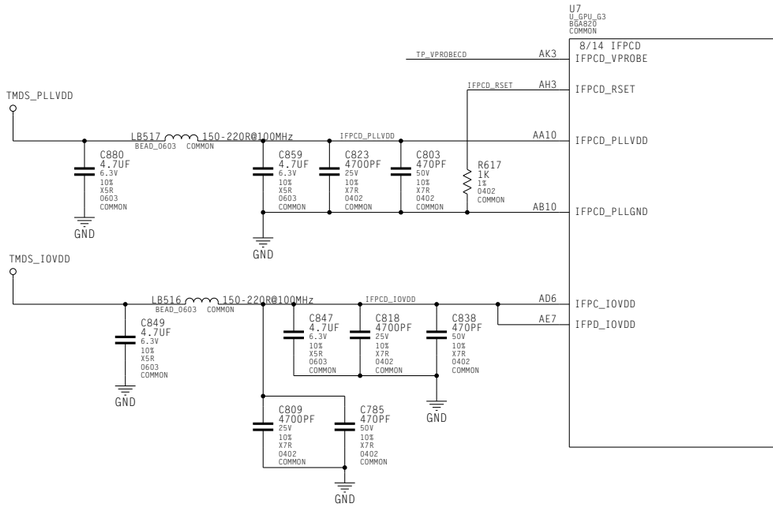
INTERNAL TMDS .. LINK C & D
MID

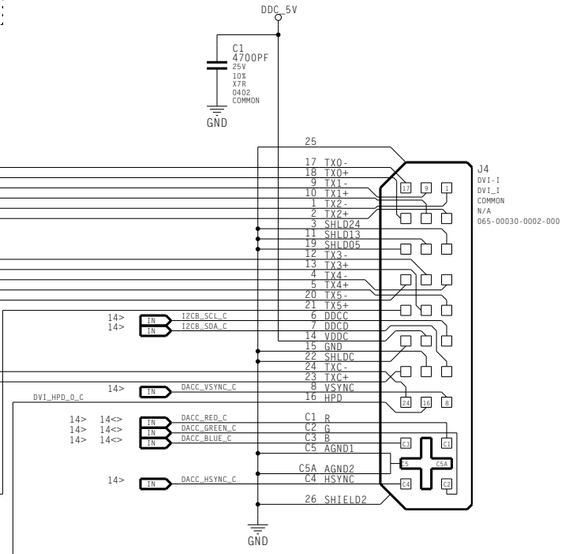


LINK C & LINK D PULLUPS ... SHOULD BE PLACED AS CLOSE AS POSSIBLE TO GPU

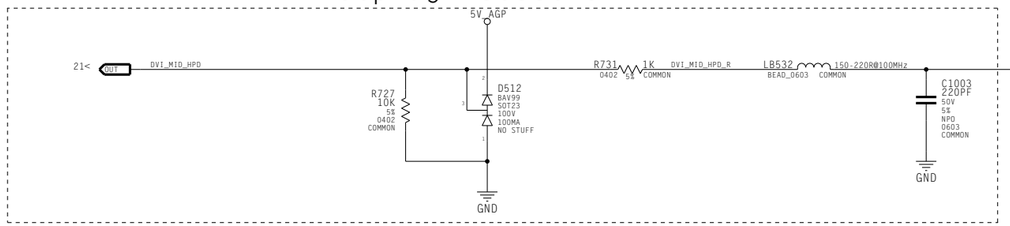


NETNAME	DIFF PAIR NAME	MIN_LINE_WIDTH	SPACING RULE
IFPC_TXC (AM3)	CTXC*	3.5MIL	25MIL
IFPC_TXC (AM2)	CTXC	3.5MIL	25MIL
IFPC_TXD0 (AE1)	CTXD0*	3.5MIL	25MIL
IFPC_TXD0 (AE2)	CTXD0	3.5MIL	25MIL
IFPC_TXD1 (AF2)	CTXD1*	3.5MIL	25MIL
IFPC_TXD1 (AF1)	CTXD1	3.5MIL	25MIL
IFPC_TXD2 (AH1)	CTXD2*	3.5MIL	25MIL
IFPC_TXD2 (AG1)	CTXD2	3.5MIL	25MIL
IFPD_TXC (AH2)	TP_DTXC*		
IFPD_TXC (AG3)	TP_DTXC		
IFPD_TXD4 (AJ1)	DTXD4*	3.5MIL	25MIL
IFPD_TXD4 (AK1)	DTXD4	3.5MIL	25MIL
IFPD_TXD5 (AL1)	DTXD5*	3.5MIL	25MIL
IFPD_TXD5 (AL2)	DTXD5	3.5MIL	25MIL
IFPD_TXD6 (AJ3)	DTXD6*	3.5MIL	25MIL
IFPD_TXD6 (AJ2)	DTXD6	3.5MIL	25MIL

FOR MICROSTRIP 100 OHM DIFFERENTIAL IMPEDANCE



Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
IFPCD_RSET	12MIL	
IFPCD_PLLVDD	12MIL	3.3V
IFPCD_IOVDD	12MIL	3.3V

ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	Internal TMDS - Link C-D with DVI-I Connector

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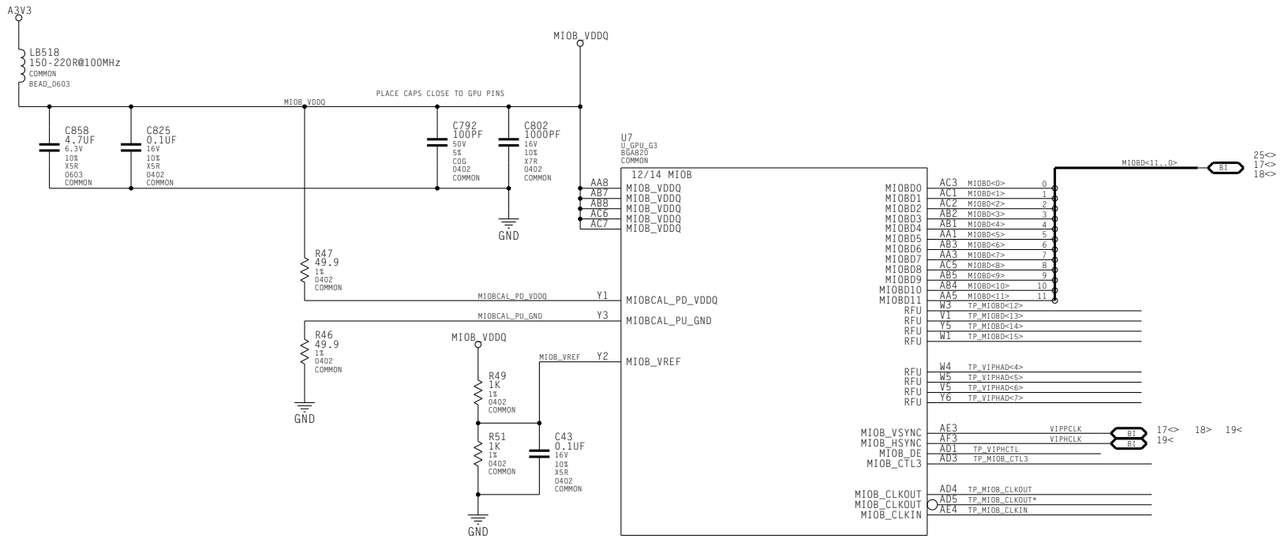
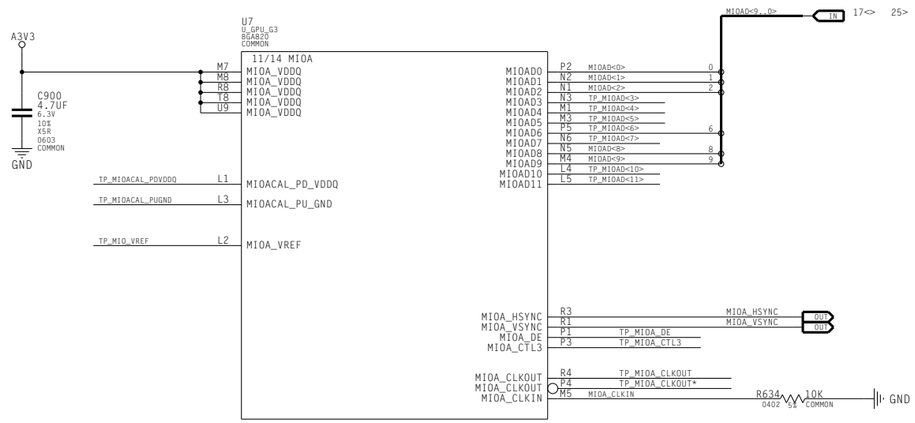
G3 VIP/MIOB



NETNAME	MIN_LINE_WIDTH	SPACING RULE
MIOBD<7..0>	4MIL	15MIL
MIOBD<11..10>	4MIL	10MIL
VIPPCLK	4MIL	15MIL
MIOAD<11..0>	4MIL	
MIOA_CLKOUT		15MIL
MIOA_CLKOUT*		15MIL

NETNAME	MIN_LINE_WIDTH
MIOB_VDDQ	12MIL
MIOB_VREF	12MIL
MIOA_VREF	12MIL

G3 MIOA



ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	GPU - MIOA - MIOB

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PHILIPS VIDEO CAPTURE

NETNAME	MIN_LINE_WIDTH
VDDA	12MIL
VDDX	12MIL
VDDE	12MIL

U507
SAA7115HL
I5_QFP100
COMMON
7114H,7115HL (QFP100)

Video In
NTP_7115_AOUT 22 AOUT
AI11 20 AI11
AI12 18 AI12
AI1D 19 AI1D
A21 16 AI21
A22 14 AI22
A23 12 AI23
A24 10 AI24
A2D 13 AI2D

19<> 19> IN MINIDIN_Y_CVBSin C948 .047UF 0402 16V 10% X7R COMMON
19<> 19> IN MINIDIN_Cin C954 .047UF 0402 16V 10% X7R COMMON

C949 .047UF 16V 10% X7R 0402 COMMON
C31 .047UF 16V 10% X7R 0402 COMMON
C956 .047UF 16V 10% X7R 0402 COMMON
C958 .047UF 16V 10% X7R 0402 COMMON
C961 .047UF 16V 10% X7R 0402 COMMON
C27 .047UF 16V 10% X7R 0402 COMMON

NTP_7115_AMCLK 37 AMCLK
NTP_7115_ALRCLK 40 ALRCLK
NTP_7115_ASCLK 39 ASCLK
41 AMXCLK

TP_7115_24576 4 XTOUT
7115Xout 6 XTALO
7115Xin 7 XTALI

Y501 XTAL CER_SMD 24.576MHZ +/-30PPM COMMON
C968 22PF 50V 5% NPO 0402 COMMON
C967 22PF 50V 5% NPO 0402 COMMON

A3V3
R683 10K 5% 0402 COMMON

32 SDA
31 SCL
R684 0 0402 5% COMMON
RESET_7114 27 RES (CE)
NTP_7115_RESOUT 30 RES_OUT

I-Port
0 MIOBD<0> 62 IPD0
1 MIOBD<1> 61 IPD1
2 MIOBD<2> 60 IPD2
3 MIOBD<3> 59 IPD3
4 MIOBD<4> 57 IPD4
5 MIOBD<5> 56 IPD5
6 MIOBD<6> 55 IPD6
7 MIOBD<7> 54 IPD7

21<> 19<> BI I2CC_SDA
21< 19< IN I2CC_SCL
21> IN RESET_BUF*
25<> 17<> BI MIOBD<7..0>

NTP_7115_HPD0 72 HPD0
NTP_7115_HPD1 71 HPD1
NTP_7115_HPD2 70 HPD2
NTP_7115_HPD3 69 HPD3
NTP_7115_HPD4 67 HPD4
NTP_7115_HPD5 66 HPD5
NTP_7115_HPD6 65 HPD6
NTP_7115_HPD7 64 HPD7

19< 17<> OUT VIPPCLK R679 0 0402 5% COMMON
7115_ICLK 45 ICLK
NTP_7115_IDQ 46 IDQ
NTP_7115_IGPH 53 IGPH
NTP_7115_IGPV 52 IGPV
NTP_7115_ITRDY 42 ITRDY
RESET_7115 47 ITRI
NTP_7115_IGPD 48 IGPD
NTP_7115_IGP1 49 IGP1

R680 4.7K 0402 5% COMMON
C928 .047UF 16V 10% X7R 0402 COMMON

VDDA0 23
VDDA1 17
VDDA2 11
AGND 21
VSSA0 24
VSSA1 15
VSSA2 9

C950 2200PF 50V 10% X7R 0402 COMMON
C945 2200PF 50V 10% X7R 0402 COMMON
C959 2200PF 50V 10% X7R 0402 COMMON
C944 0.1UF 16V 10% X5R 0402 COMMON
C935 4.7UF 6.3V 10% X5R 0603 COMMON
VDDA
LB527 600R@100MHz BEAD_0603 COMMON
A3V3
C934 4.7UF 6.3V 10% X5R 0603 COMMON

TDO 2
TMS 99
TDI 3
TRST 97
TCK 98

TDO from SAA7115 into TDI of Bridge
TDO from GPU into TDI of SAA7115
JT_TDO_SAA7115 OUT 4<
JT_TMS IN 4> 21<
JT_TDO_GPU IN 21>
JT_TRST* IN 4> 21<
JT_TCK IN 4> 21<

R703 0 0402 5% NO STUFF
JTAG bypass
Install component
if Video-In
is not installed

TEST0 44 NTP_7115_TEST0
TEST1 73 NTP_7115_TEST1
TEST2 74 NTP_7115_TEST2
TEST3 77 NTP_7115_TEST3
TEST4 78 NTP_7115_TEST4
TEST5 79 NTP_7115_TEST5

RTC0 36 7115_RTC0
RTS0 34 NTP_7115_RTS0
RTS1 35 NTP_7115_RTS1
LLC 28 NTP_7115_LLC
LLC2 29 NTP_7115_LLC2
R685 1K 5% 0402 COMMON

X-Port
XPD0 90 NTP_7115_XPD0
XPD1 89 NTP_7115_XPD1
XPD2 87 NTP_7115_XPD2
XPD3 86 NTP_7115_XPD3
XPD4 85 NTP_7115_XPD4
XPD5 84 NTP_7115_XPD5
XPD6 82 NTP_7115_XPD6
XPD7 81 NTP_7115_XPD7

XCLK 94 NTP_7115_XCLK
XDQ 95 NTP_7115_XDQ
XRH 92 NTP_7115_XRH
XRV 91 NTP_7115_XRV
XRDY 96 NTP_7115_XRDY
XTRI 80 NTP_7115_XTRI

VDD
VDD_XTAL 8
VDDDE1 1
VDDDE2 25
VDDDE3 51
VDDDE4 75
VDDDI1 33
VDDDI2 43
VDDDI3 58
VDDDI4 68
VDDDI5 83
VDDDI6 93

D-GND
VSS_XTAL 5
VSSDE1 26
VSSDE2 50
VSSDE3 76
VSSDE4 100
VSSDI1 38
VSSDI2 63
VSSDI3 88

C966 2200PF 50V 10% X7R 0402 COMMON
C964 2200PF 50V 10% X7R 0402 COMMON
VDDX
LB528 600R@100MHz BEAD_0603 COMMON
C962 4.7UF 6.3V 10% X5R 0603 COMMON
C969 4.7UF 6.3V 10% X5R 0603 COMMON
VDDE
LB529 600R@100MHz BEAD_0603 COMMON

C977 2200PF 50V 10% X7R 0402 COMMON
C926 2200PF 50V 10% X7R 0402 COMMON
C966 2200PF 50V 10% X7R 0402 COMMON
C976 2200PF 50V 10% X7R 0402 COMMON
C953 2200PF 50V 10% X7R 0402 COMMON
C978 0.1UF 16V 10% X5R 0402 COMMON
C939 0.1UF 16V 10% X5R 0402 COMMON
C979 4.7UF 6.3V 10% X5R 0603 COMMON
C983 4.7UF 6.3V 10% X5R 0603 COMMON

C938 2200PF 50V 10% X7R 0402 COMMON
C927 2200PF 50V 10% X7R 0402 COMMON
C936 2200PF 50V 10% X7R 0402 COMMON
C973 2200PF 50V 10% X7R 0402 COMMON
C972 2200PF 50V 10% X7R 0402 COMMON
C975 0.1UF 16V 10% X5R 0402 COMMON
C974 0.1UF 16V 10% X5R 0402 COMMON
C931 0.1UF 16V 10% X5R 0402 COMMON

SAA 7115
I2C ADDRESS 0X42

ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	Video In - SAA7115

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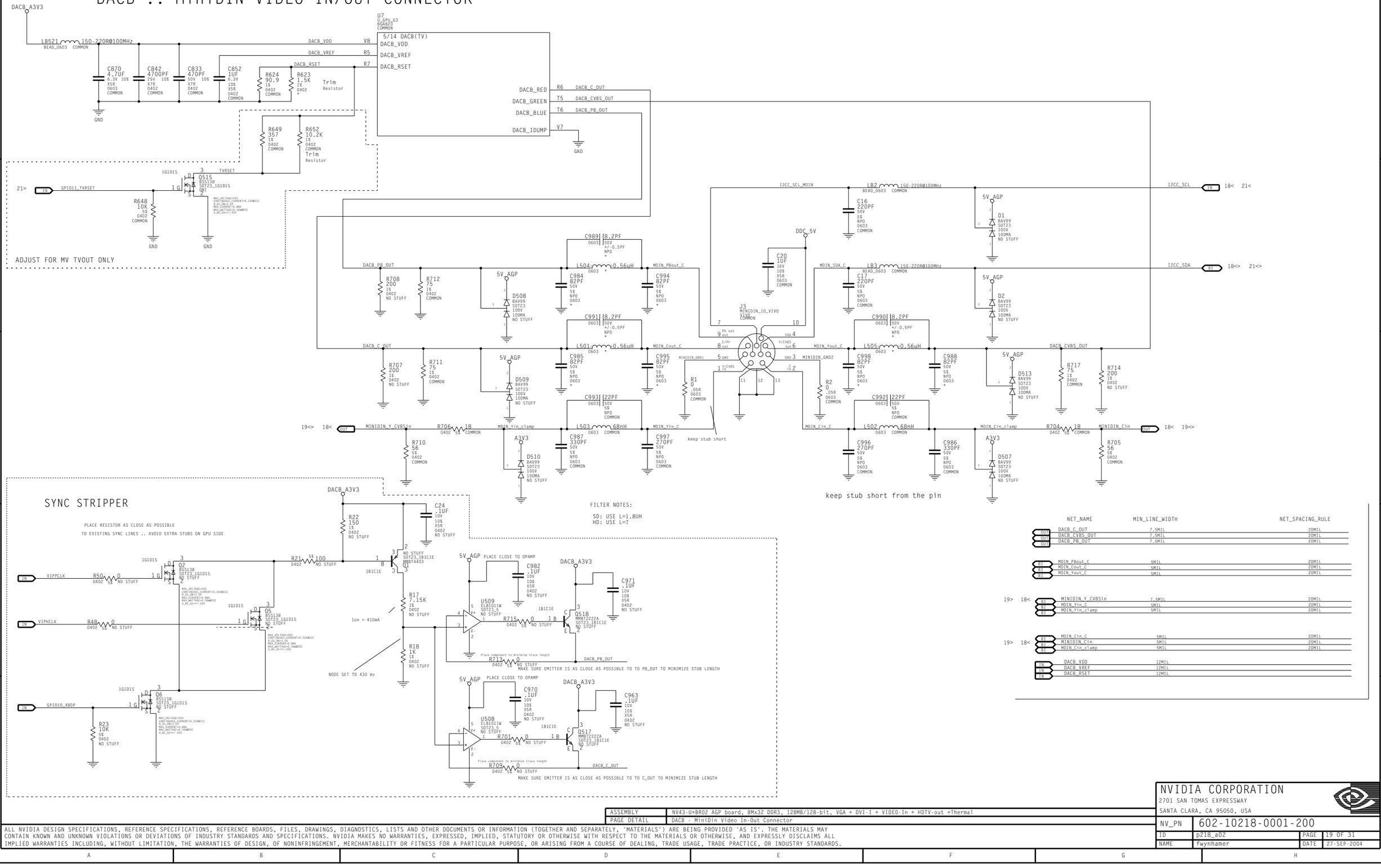
DACB .. MiniDIN VIDEO IN/OUT CONNECTOR



NET_NAME	MIN_LINE_WIDTH	NET_SPACING_RULE
OUT DACB_C_OUT	7.5MIL	20MIL
OUT DACB_CVBS_OUT	7.5MIL	20MIL
OUT DACB_PB_OUT	7.5MIL	20MIL
BI MDIN_PBout_C	5MIL	20MIL
BI MDIN_Cout_C	5MIL	20MIL
BI MDIN_Yout_C	5MIL	20MIL
19> 18< BI MINIDIN_Y_CVBSin	7.5MIL	20MIL
BI MDIN_Yin_C	5MIL	20MIL
BI MDIN_Yin_clamp	5MIL	20MIL
19> 18< BI MDIN_Cin_C	5MIL	20MIL
BI MINIDIN_Cin	5MIL	20MIL
BI MDIN_Cin_clamp	5MIL	20MIL
IN DACB_VDD	12MIL	
IN DACB_VREF	12MIL	
IN DACB_RSET	12MIL	

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ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	DACB - MiniDin Video In-Out Connector

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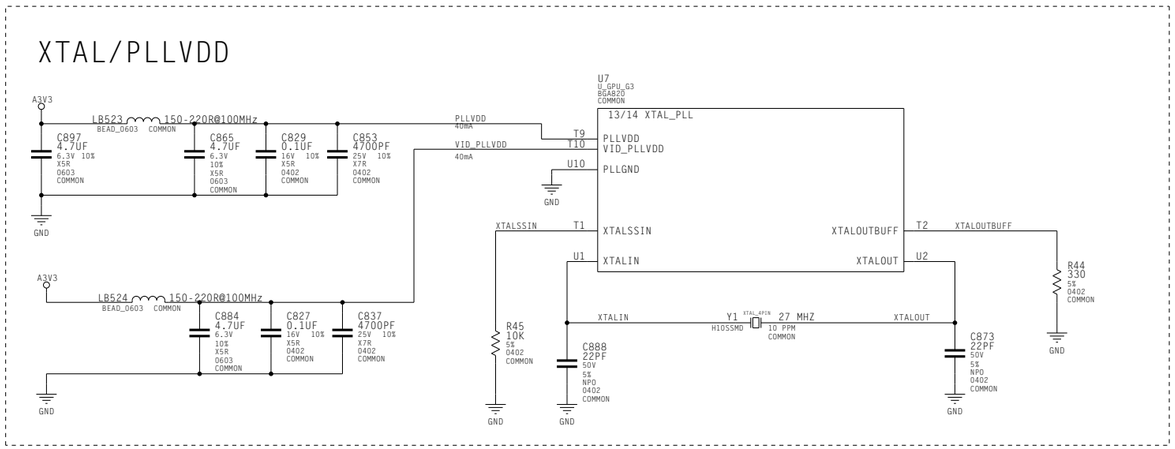
XTAL and GPU's GND

XTAL/PLLVDD



NETNAME	MIN_LINE_WIDTH	NET_SPACING_RULE
BI VidInt_Y_CVBSin		20MIL
BI VidInt_Cin		20MIL
BI VidInt_CVBSin		20MIL
BI VidInt_Y_F		20MIL
BI VidInt_C_F		20MIL
BI VidInt_CVBS_F		20MIL
BI SEC_CVBS1A		20MIL
BI SEC_LUMA		20MIL
BI SEC_CHROMA		20MIL
BI SEC_CVBS		20MIL
BI TUNER_CVBS		20MIL
IN XTALIN	4MIL	
IN XTALOUT	4MIL	
IN PLLVDD	12MIL	
IN VID_PLLVDD	12MIL	

U7
U_GPU_G3
BGA820
COMMON

14/14 _GND_

AA12	GND	K10	GND
AA2	GND	K23	GND
AA21	GND	K29	GND
AA31	GND	K4	GND
AB27	GND	L27	GND
AB6	GND	L6	GND
AC10	GND	M12	GND
AC23	GND	M2	GND
AC29	GND	M31	GND
AC4	GND	N15	GND
AD16	GND	N18	GND
AD17	GND	N29	GND
AD2	GND	N4	GND
AD31	GND	P13	GND
AE17	GND	P18	GND
AE27	GND	P27	GND
AE6	GND	P6	GND
AF11	GND	R13	GND
AF26	GND	R14	GND
AF29	GND	R15	GND
AF4	GND	R18	GND
AF7	GND	R19	GND
AG10	GND	R2	GND
AG11	GND	R20	GND
AG14	GND	R31	GND
AG15	GND	T16	GND
AG19	GND	T17	GND
AG2	GND	T24	GND
AG22	GND	T29	GND
AG31	GND	T4	GND
AG8	GND	U16	GND
AH24	GND	U17	GND
AJ10	GND	U24	GND
AJ13	GND	U29	GND
AJ16	GND	U8	GND
AJ17	GND	V13	GND
AJ20	GND	V14	GND
AJ23	GND	V15	GND
AJ26	GND	V18	GND
AJ29	GND	V19	GND
AJ4	GND	V2	GND
AJ7	GND	V20	GND
AK2	GND	V31	GND
AK28	GND	W15	GND
AK31	GND	W18	GND
AL11	GND	W27	GND
AL14	GND	W6	GND
AL19	GND	Y15	GND
AL22	GND	Y18	GND
AL25	GND	Y29	GND
AL3	GND	Y4	GND
AL6	GND	AL10	GND
AL9	GND	AM10	GND
AM13	GND	AG13	GND
AM16	GND		
AM17	GND		
AM20	GND		
AM23	GND		
AM26	GND		
AM29	GND		
B12	GND		
B15	GND		
B18	GND		
B21	GND		
B24	GND		
B27	GND		
B3	GND		
B30	GND		
B6	GND		
B9	GND		
C2	GND		
C31	GND		
D10	GND		
D13	GND		
D16	GND		
D17	GND		
D20	GND		
D23	GND		
D26	GND		
D29	GND		
D4	GND		
D7	GND		
F11	GND		
F14	GND		
F19	GND		
F2	GND		
F22	GND		
F25	GND		
F31	GND		
F8	GND		
G26	GND		
G29	GND		
G4	GND		
G7	GND		
H27	GND		
H6	GND		
J16	GND		
J17	GND		
J2	GND		
J31	GND		

GND

GND

ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	GPU - XTAL and GPU GND

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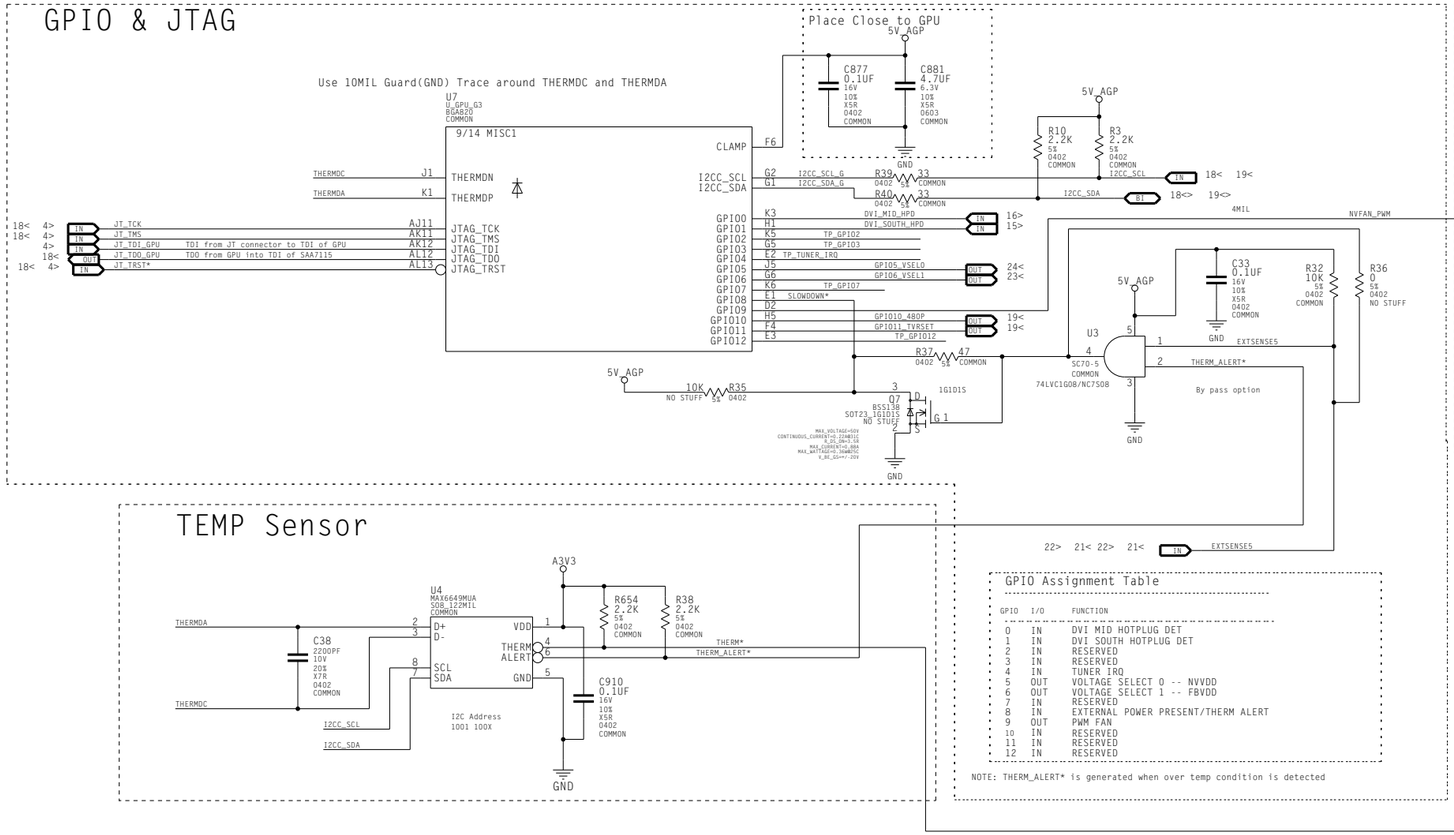
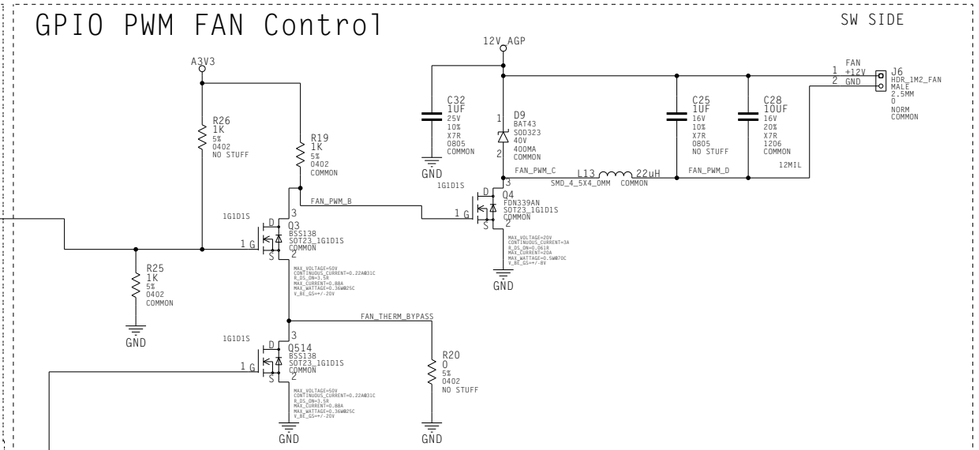
GPIO & JTAG



GPIO PWM FAN Control



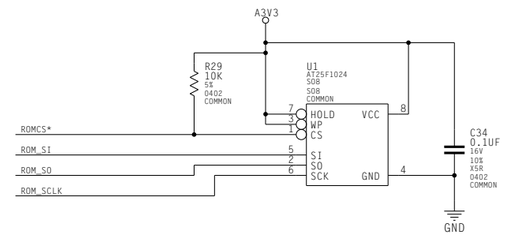
TEMP Sensor

GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	DVI SOUTH HOTPLUG DET
2	IN	RESERVED
3	IN	RESERVED
4	IN	TUNER IRQ
5	OUT	VOLTAGE SELECT 0 -- NVVDD
6	OUT	VOLTAGE SELECT 1 -- FBVDD
7	IN	RESERVED
8	IN	EXTERNAL POWER PRESENT/THERM ALERT
9	OUT	PWM FAN
10	IN	RESERVED
11	IN	RESERVED
12	IN	RESERVED

NOTE: THERM_ALERT* is generated when over temp condition is detected

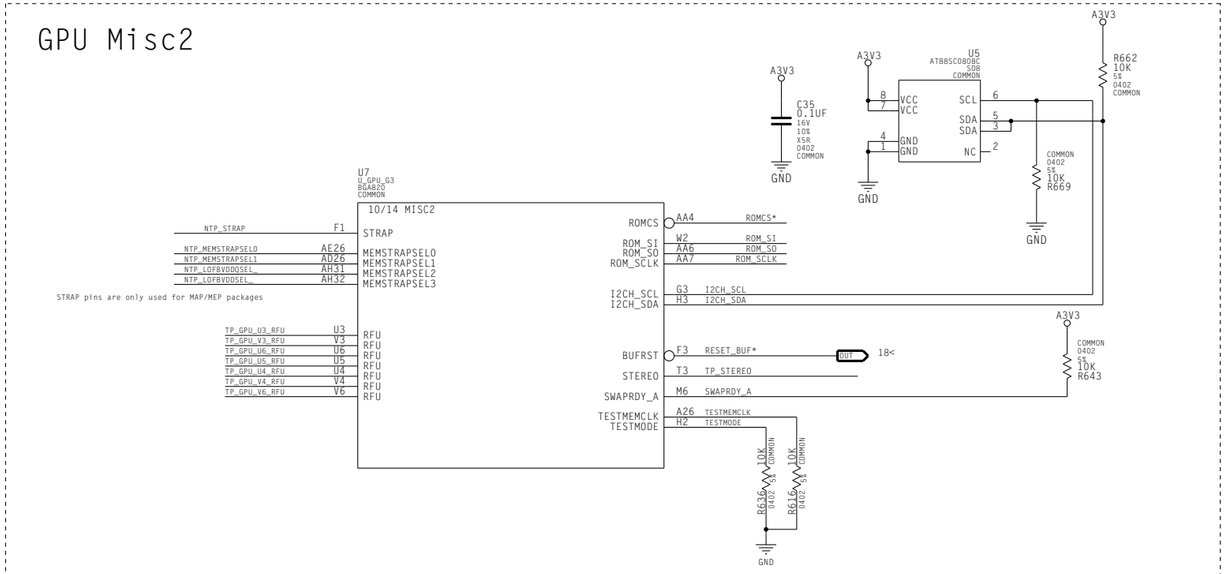
BIOS (serial)



SROM MAPPING

ROM	NV4x
SO	ROM_SO
SI	ROM_SI
SCK	ROM_SCK
CS*	ROM_CS*

GPU Misc2



AUDIO and VIDEO signals are reserved for future GPU's. NV4x will not have support for these signals

NETNAME	MIN_LINE_WIDTH	VOLTAGE
THERMDC	10MIL	
THERMDA	10MIL	

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GPIO - I2C - Expansion - FAN Control - BIOS ROM

DETAIL	DRAWING DETAIL CONTINUED...		
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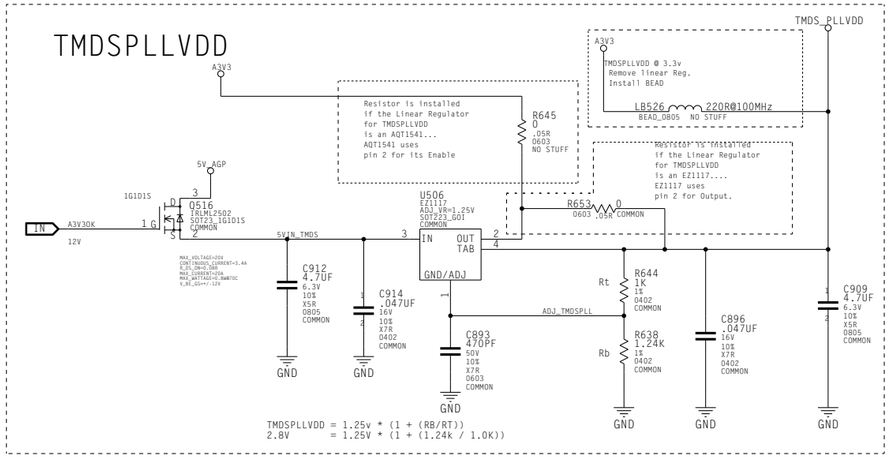
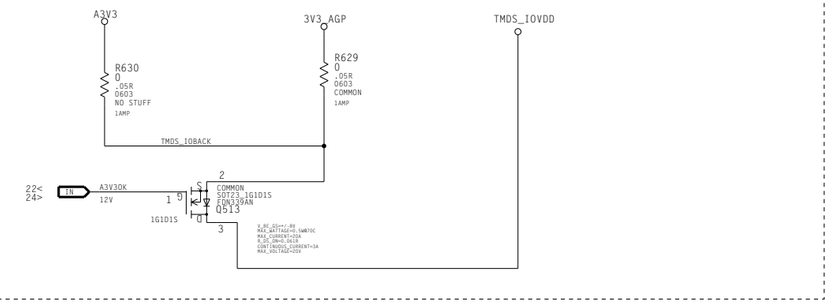
Power SupplY: TMDPSPLLVDD/TMDSIOVDD/EXT-POWER CONNECTOR

TMDSPLLVDD

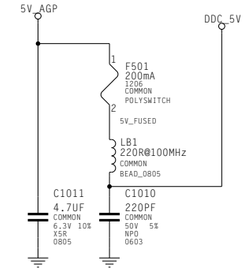


TMDS_IOVDD WITH BACKDRIVE PREVENTION



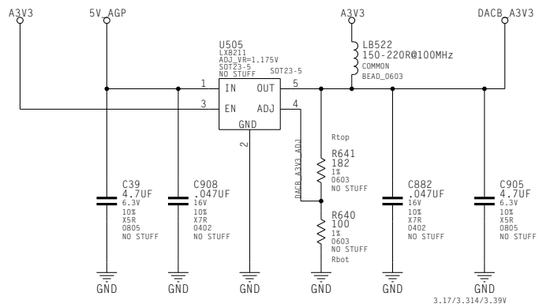
NETNAME	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	12MIL	5V
DDC_5V	12MIL	5V
TMDSABPLL_ADJ	10MIL	3.3V
TMDS_PLLVDD	12MIL	3.3V
MIOA2V5_VREF	10MIL	
TMDS_IOVDD	12MIL	3.3V
GND		0V
DACB_A3V3_ADJ	10MIL	3.3V
DACB_A3V3	12MIL	3.3V

DDC 5V



POWER_DDC5V

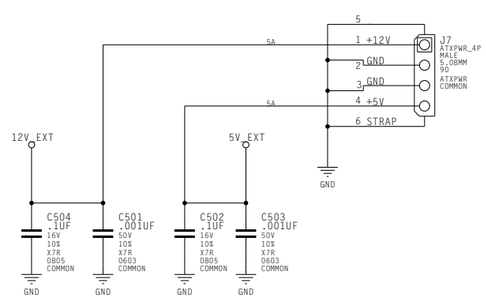
DACB Supply



POWER_TMDSPLL_REGO

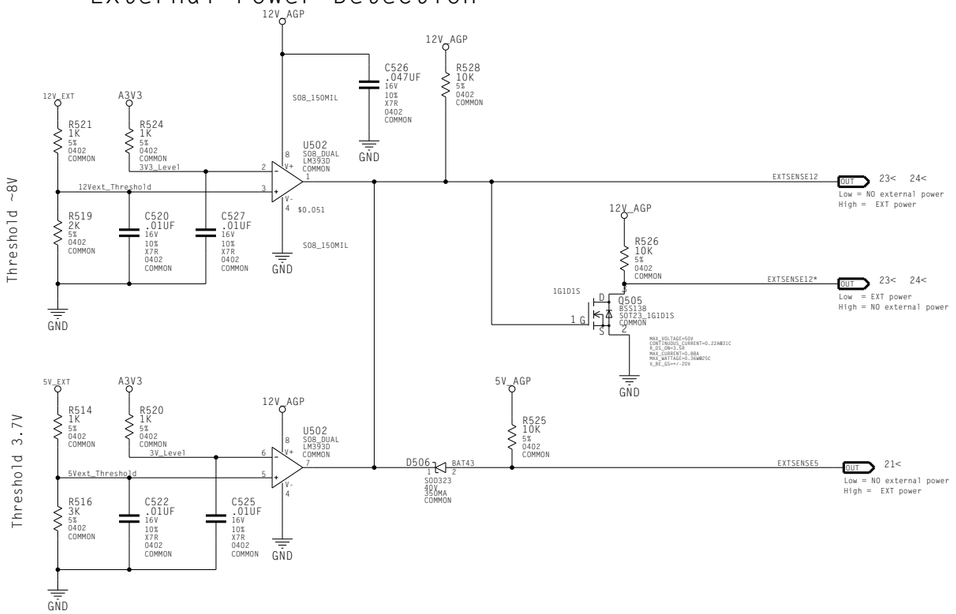
Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+(100/182))

External Power Connector



NOTE:
Shutdown the power before connecting or disconnecting Extenal Power

External Power Detection



ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	Power - TMDSPLLVDD - TMDSIOVDD - DACB - EXTERNAL PWR

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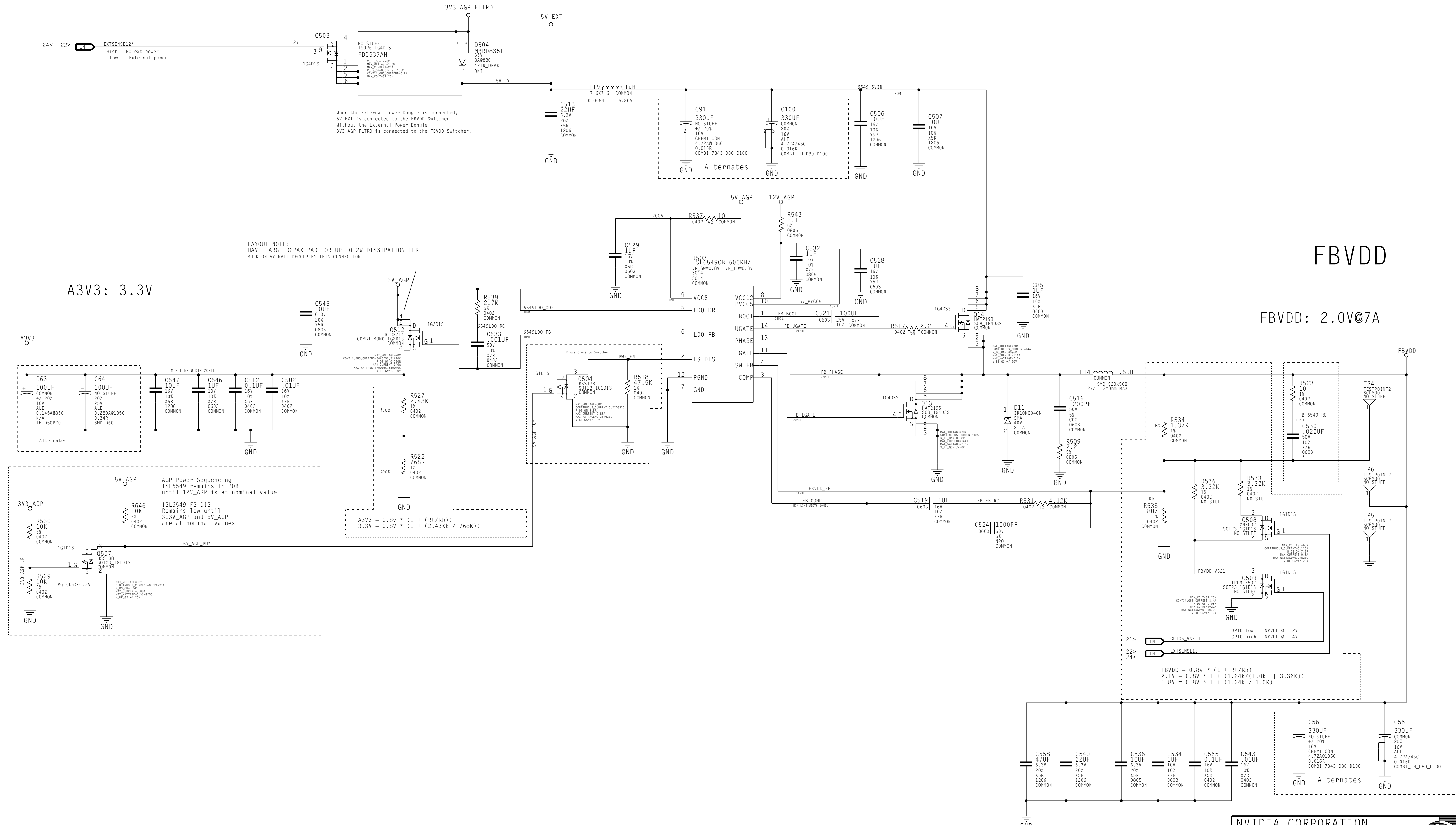
Power Supply .. ISL6549 FBVDD and A3V3



ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	Power - FBVDD - A3V3

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NVVDD and PEX Power

When the External Power Dongle is connected,
12V_EXT is connected to the GPU's NVVDD Switcher.
Without the External Power Dongle,
12V_AGP is connected to the GPU's NVVDD Switcher.

22> 23< EXTSENSE12* — High = NO ext power; Low = External power

12V_EXT, 12V_AGP, 12V_FLTRD, 12V_IN, 12V_AGP_D1, 12V_AGP_D2

F1 1A 1812 COMMON POLYSWITCH

D503 MBRD835L 35V BA0B8C 4PIN_DPAK NO STUFF

Q506 FDS4435 SO8_1G4D3S COMMON

D16, D15 SMA 40V 2.1A COMMON IR10MQ040N

R81 300 5% 0805 COMMON; R82 300 5% 0805 COMMON

L15 1uH CDR73 COMMON

C69 10UF NO STUFF +/-20% 16V ALE 0.05A@85C N/A TH_D50P20

C76 100UF COMMON 20% 25V ALE 0.28@A@105C 0.34R SMD_D6

THESE ARE ALTERNATES

C95 330UF COMMON 20% 16V OSCON 4.72A@105C 0.016R COMBI_7343D8OD1001812

C99 330UF NO STUFF 20% 16V ALE 4.72A/45C 0.016R COMBI_TH_D8O_D100

Alternates

C96 330UF NO STUFF 20% 16V ALE 4.72A/45C 0.016R COMBI_TH_D8O_D100

C97 330UF COMMON +/-20% 16V OSCON 4.72A@105C 0.016R COMBI_7343O8OD1001812

Alternates

NVVDD REMOTE SENSE

NVVDD_SENSE IN 6> 6<>; GND_SENSE IN 6> 6<>

R540 0 0402 5% COMMON

Place component close to NVVDD Power

3V3_AGP, 3V3_AGP_FLTRD

L18 1uH 6.84A CDR73 COMMON

C86 22UF 6.3V 20% X5R 1206 COMMON

C94 510U COMMON +50I/-10% 4 OSCON 4.08A@45C 0.014R COMBI_TH_D8O_D100

Alternates

C98 180UF NO STUFF +/-20% 16V OSCON 3.64A@105C 0.020R COMBI_7343_D8O_D100

C93 .047UF 16V 10% X7R 0402 COMMON; C101 1UF 16V 10% X7R 0805 COMMON

5V_AGP

C517 1UF 10V 10% X7R 0603 COMMON; C518 1UF 10V 10% X7R 0603 COMMON

U501 ISL6534CR-T VR_SW=0.6V MLFP32 MLFP32 COMMON

2 Phase PWM

ISL12V_VCC, COMP1_NVVDD, NVVDD_FB, Vref = 1.1V, VREFIN, COMP2_PEXVDD, FB2_PEXVDD, DRIVE3_PEX1V2, FB3_1V2, ISL_REFOUT, VREF_3V3, TP_6534_GOOD

VCC, COMP1, FB1, REFIN, COMP2, FB2, DRIVE3, FB3, REFOUT, VREF, PGOOD, GND, GND(PAD)

VCC12_1, VCC12_2, BOOT1, UGATE1, LGATE1, BOOT2, UGATE2, LGATE2, FS/SYNC, SS1/EN1, SS2/EN2, SS3/EN3, PGND_1, PGND_2

Please very close to Switcher

FREQ_SET; R513 0 5% 0402 COMMON 300KHz; 6534_SSEN

R510 2K 1% 0402 COMMON; R501 1K 1% 0402 COMMON; R506 1K 5% 0402 NS

C505 .1UF 10V 10% X5R 0402 COMMON; C515 1UF 6.3V 10% X5R 0402 COMMON; C509 .1UF 10V 10% X5R 0402 COMMON; C512 .47UF 10V 10% X5R 0603 COMMON

C508 1UF 16V 10% X5R 0603 COMMON

D505 BAT54ALT1 30V 200MA SOT23 COMMON

D502 CMSZDA3V3 3.5YR 275MW@25C SOT323 COMMON

NTP_ISL6534_ZENER

R502 2.2 0402 5% COMMON; UGATE_1_RG

C82 .100UF 0603 25V 10% X7R COMMON

Q17 HAT2168H LFPAK COMMON; Q16 HAT2168H LFPAK NO STUFF

C84 4.7UF 16V 10% X7R 1206 COMMON

PLACE CLOSE TO DRAIN OF UPPER FETS

NODE_1

L16 1UH SMD_590x530 COMMON 0.0017 MAX 32A

TP2 TESTPOINT2 SCHMOD NO STUFF; TP3 TESTPOINT2 SCHMOD NO STUFF

NVVDD = 1.4V@35A

NVVDD

R542 10 1% 0402 NO STUFF — Install if NO GPU..... Power Debug Only Purposes

R546 10 1% 0402 COMMON NVVDD_RC; C535 .022UF 16V 10% X7R 0402 COMMON — Type-3 Comp.

C542 10UF 6.3V 20% X5R 0805 COMMON; C539 1UF 10V 10% X7R 0603 COMMON

R541 1K 1% 0402 COMMON; TP1 TESTPOINT2 SCHMOD NO STUFF

R538 3.09K 1% 0402 NO STUFF; R544 3.09K 1% 0402 COMMON

Q510 2N7002 SOT23_1G1D1S COMMON; Q511 IRLML2502 SOT23_1G1D1S COMMON

R87 1K 1% 0402 COMMON

ALTERNATES

C68 1000UF COMMON +/-20% 4V OSCON 5.04A@45C 0.012R COMBI_TH_D8O_D100

C66 1200UF NO STUFF +/-20% 4V OSCON 5.44A@105C 0.012R COMBI_7343D8OD1001812

C67 1000UF COMMON +/-20% 4V OSCON 5.04A@45C 0.012R COMBI_TH_D8O_D100

C65 1200UF NO STUFF +/-20% 4V OSCON 5.44A@105C 0.012R COMBI_7343D8OD1001812

ALTERNATES

GPIO low = NVVDD @ 1.2V
GPIO high = NVVDD @ 1.4V

21> IN GPIO5_VSEL0; 24< 23< 22> IN EXTSENSE12

NVVDD = 0.6v * (1 + Rt/Rb)
1.4V = 0.6V * 1 + (1.0k/(1.0k || 3.09K))
1.2V = 0.6V * 1 + (1.0k / 1.0K)

Q18 IRF7313 SO8_DUAL_1G2D1S COMMON

R88 2.2 0402 5% COMMON UGATE_2_RG

3V3_AGP_FLTRD — PLACE CLOSE TO DRAIN OF UPPER FET

C92 4.7UF 16V 10% X7R 1206 COMMON

C87 .100UF 0603 25V 10% X7R COMMON

C105 1000PF 16V 10% X7R DNI

D12 1R10MQ040N 5MA 40V 2.1A COMMON

C88 2200PF 50V 10% X7R 0402 COMMON; R83 2.2 5% 0805 COMMON

L17 2.2uH SMD_6X6 COMMON .018R 8A

R84 10 5% 0402 COMMON; C81 10UF 6.3V 20% X5R 0805 COMMON; C83 1UF 10V 10% X7R 0603 COMMON

FB_6534_RC

C90 .047UF 16V 10% X7R 0402 COMMON

R85 1K 1% 0603 COMMON; R86 5.62K 1% 0603 COMMON

VOUT = REFIN * (Rt+Rb)/Rb
1.30 = 1.1 * (1k + 5.62K)/5.62K

BRO2VDD: 1.3V @ 5A
(INCLUDES GPUPEXVDD @ 2A)

GPUPEXVDD: 1.2V @ 2A

GPUPEXVDD

C73 100UF NO STUFF 20% 25V ALE 0.28@A@105C 0.34R SMD_D60; C72 100UF COMMON +/-20% 10V ALE 0.145A@85C N/A TH_D50P20

Alternates

C79 10UF 16V 10% X5R 1206 COMMON; C77 10UF 10V 10% X7R 0603 COMMON; C80 .1UF 10V 10% X5R 0402 COMMON; C78 .01UF 16V 10% X7R 0402 COMMON

Q11 IRF7313 SO8_1G4D3S COMMON

BRO2VDD

R547 0 0603 .05R NO STUFF; R548 0 0603 .05R NO STUFF; R545 0 0603 .05R NO STUFF

Stuff option
Unifying the BRO2VDD and GPUPEXVDD rails
Remove the LDO
Install resistors
Adjust BRO2VDD rail to 1.2V

1.2mP

R521 1K 1% 0402 COMMON; R512 2.7K 5% 0402 COMMON; R515 1K 1% 0402 COMMON

C514 .01UF 50V 10% X7R 0402 COMMON FB3_RC

12V_AGP

R507 10K 5% 0402 COMMON

22< OUT A3V30K — Enables the linear regulators

D501 BAT54ALT1 30V 200MA SOT23 COMMON

A3V3

R503 1.07K 1% 0402 COMMON; R505 1.15K 1% 0402 COMMON

Q502 BSS138 SOT23_1G1D1S COMMON; Q501 BSS138 SOT23_1G1D1S COMMON

A3V30K*

Vgs_th = 1.2V

GPU Core Power Enable

ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	Power - NVVDD - BRO2VDD - GPUPEXVDD

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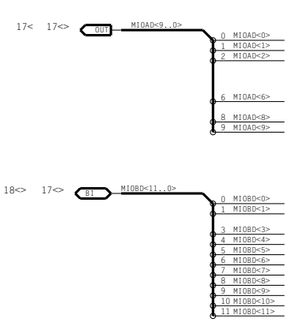
BIOS, Straps, Misc

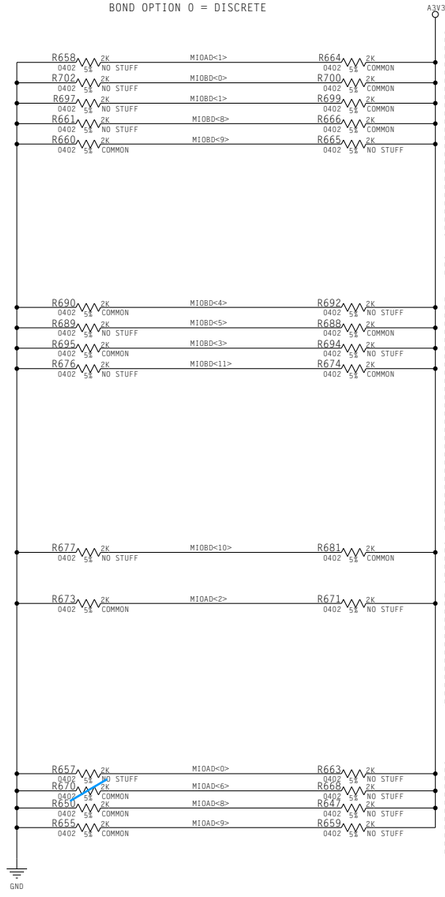
Assembly: BIOS

Straps



STUFF BETWEEN 1K & 2.7K

BOND OPTION 0 = DISCRETE



NV_STRAP_0

BIT	FUNCTION	MAP/MCP/SQUISH PIN (STL Name)	NORMAL PIN (STL Name)	REQUIED ON BOARD?
0	PCI_AD	`NV_PEXTDEV_BOOT_0_STRAP_PCI_AD_NORMAL`	`NV_PEXTDEV_BOOT_0_STRAP_PCI_AD_NORMAL`	PCI/AGP_ONLY
1	SUB_VENDOR	MIOBD02 (ctrl+a_data[1])	MIOBD02 (ctrl+a_data[1])	YES
2	RAMCFG[0]	MIOAD7 (ctrl+a_data[7])	MIOAD7 (ctrl+a_data[7])	NO
3	RAMCFG[1]	MIOAD6 (ctrl+a_data[6])	MIOAD6 (ctrl+a_data[6])	NO
4	RAMCFG[2]	MIOAD5 (ctrl+a_data[5])	MIOAD5 (ctrl+a_data[5])	NO
5	RAMCFG[3]	MIOAD4 (ctrl+a_data[4])	MIOAD4 (ctrl+a_data[4])	NO
6	CRYSTAL0	MIOAD3 (ctrl+a_data[3])	MIOAD3 (ctrl+a_data[3])	NO
7	TVMODE[0]	MIOAD7 (ctrl+a_data[7])	MIOAD7 (ctrl+a_data[7])	NO
8	TVMODE[1]	MIOAD2 (ctrl+a_data[2])	MIOAD2 (ctrl+a_data[2])	NO
9	AGP_4X	`NV_PEXTDEV_BOOT_0_STRAP_AGP_4X_DISABLED`	`NV_PEXTDEV_BOOT_0_STRAP_AGP_4X_DISABLED`	NO
10	AGP_SBA	`NV_PEXTDEV_BOOT_0_STRAP_AGP_SBA_DISABLED`	`NV_PEXTDEV_BOOT_0_STRAP_AGP_SBA_DISABLED`	NO
11	AGP_FASTWR	`NV_PEXTDEV_BOOT_0_STRAP_AGP_FASTWR_DISABLED`	`NV_PEXTDEV_BOOT_0_STRAP_AGP_FW_DISABLED`	NO
12	PCI_DEVID[0]	MIOBD04 (ctrl+b_data[4])	MIOBD04 (ctrl+b_data[4])	NO
13	PCI_DEVID[1]	MIOBD05 (ctrl+b_data[5])	MIOBD05 (ctrl+b_data[5])	NO
14	BUS_TYPE	`NV_PEXTDEV_BOOT_0_STRAP_BUS_TYPE_AGP`	`NV_PEXTDEV_BOOT_0_STRAP_BUS_TYPE_AGP`	PCI/AGP_ONLY
15	FP_IFACE	`NV_PEXTDEV_BOOT_0_STRAP_FP_IFACE_12BIT`	`NV_PEXTDEV_BOOT_0_STRAP_FP_IFACE_12BIT`	NO
16	USER[0]	MIOBD00 (ctrl+a_data[0])	MIOBD00 (ctrl+a_data[0])	NO
17	USER[1]	MIOBD01 (ctrl+a_data[1])	MIOBD01 (ctrl+a_data[1])	NO
18	USER[2]	MIOBD08 (ctrl+b_data[8])	MIOBD08 (ctrl+b_data[8])	NO
19	USER[3]	MIOBD09 (ctrl+b_data[9])	MIOBD09 (ctrl+b_data[9])	NO
20	PCI_DEVID2[0]	MIOBD2 (ctrl+b_data[2])	MIOBD2 (ctrl+b_data[2])	NO
21	PCI_DEVID2[1]	MIOA_HSYNC (ctrl+a_hsync)	MIOA_HSYNC (ctrl+a_hsync)	NO
22	FB[0]	MIOBD06 (ctrl+b_data[6])	MIOBD06 (ctrl+b_data[6])	NO
23	FB[1]	0	0	NO
24	FB[1]	0	0	NO
25	BR	`NV_SI_CReA_irl`	`NV_SI_CReA_irl`	MCP7F
26	BR_128M	`NV_PEXTDEV_BOOT_0_STRAP_BR_REG_128M_DISABLED`	`NV_PEXTDEV_BOOT_0_STRAP_BR_REG_128M_DISABLED`	NO
27	BR_AGP	`NV_PEXTDEV_BOOT_0_STRAP_BR_AGP_DEV_DISABLED`	`NV_PEXTDEV_BOOT_0_STRAP_BR_AGP_DEV_DISABLED`	NO
28	BR_IO	`NV_PEXTDEV_BOOT_0_STRAP_BR_IO_DEV_DISABLED`	`NV_PEXTDEV_BOOT_0_STRAP_BR_IO_DEV_DISABLED`	NO
29	ROMTYPE[0]	MIOBD10 (ctrl+b_data[10])	MIOBD10 (ctrl+b_data[10])	YES
30	ROMTYPE[1]	MIOBD11 (ctrl+b_data[11])	MIOBD11 (ctrl+b_data[11])	YES

NV_STRAP_1

BIT	FUNCTION	MAP/MCP/SQUISH PIN (STL Name)	NORMAL PIN (STL Name)	REQUIED ON BOARD?
0	1394	`NV_PEXTDEV_BOOT_1_STRAP_1_1394_DISABLED`	`NV_PEXTDEV_BOOT_1_STRAP_1_1394_DISABLED`	NO
1	1394_PHY	`NV_PEXTDEV_BOOT_1_STRAP_1_1394_PHY_DISABLED`	`NV_PEXTDEV_BOOT_1_STRAP_1_1394_PHY_DISABLED`	NO
2	1394_PHY_PWRCLASS[0]	0	0	NO
3	1394_PHY_PWRCLASS[1]	0	0	NO
4	VGA_DEVICE	`NV_PEXTDEV_BOOT_1_STRAP_1_VGA_DEVICE_ENABLED`	`NV_PEXTDEV_BOOT_1_STRAP_1_VGA_DEVICE_ENABLED`	NO
5	BR_LAST_DEV	`NV_PEXTDEV_BOOT_1_STRAP_1_BR_LAST_DEV_ENABLED`	`NV_PEXTDEV_BOOT_1_STRAP_1_BR_LAST_DEV_ENABLED`	NO
6	NV_LAST_DEV	`NV_PEXTDEV_BOOT_1_STRAP_1_NV_LAST_DEV_DISABLED`	`NV_PEXTDEV_BOOT_1_STRAP_1_NV_LAST_DEV_DISABLED`	NO
7	BR_BAR1_BCASTONLY	`NV_PEXTDEV_BOOT_1_STRAP_1_BR_BAR1_BCASTONLY_ENABLED`	`NV_PEXTDEV_BOOT_1_STRAP_1_BR_BAR1_BCASTONLY_ENABLED`	NO
8	BR_BAR1_STM_USER	`NV_PEXTDEV_BOOT_1_STRAP_1_BR_BAR1_STM_USER_DISABLED`	`NV_PEXTDEV_BOOT_1_STRAP_1_BR_BAR1_STM_USER_DISABLED`	NO
9	BOARD	`NV_PEXTDEV_BOOT_1_STRAP_1_BOARD_0`	`NV_PEXTDEV_BOOT_1_STRAP_1_BOARD_0`	NO
10	FPB_IFACE	`NV_PEXTDEV_BOOT_1_STRAP_1_FPB_IFACE_12BIT`	`NV_PEXTDEV_BOOT_1_STRAP_1_FPB_IFACE_12BIT`	NO
11	PEX_PLL_EN_TERM100	MIOBD05 (ctrl+a_data[5])	MIOBD05 (ctrl+a_data[5])	YES
12	3GIO_PADCFG_LUT_ADR[0]	MIOBD06 (ctrl+a_data[6])	MIOBD06 (ctrl+a_data[6])	YES
13	3GIO_PADCFG_LUT_ADR[1]	MIOBD07 (ctrl+a_data[7])	MIOBD07 (ctrl+a_data[7])	YES
14	3GIO_PADCFG_LUT_ADR[2]	MIOBD09 (ctrl+a_data[9])	MIOBD09 (ctrl+a_data[9])	YES

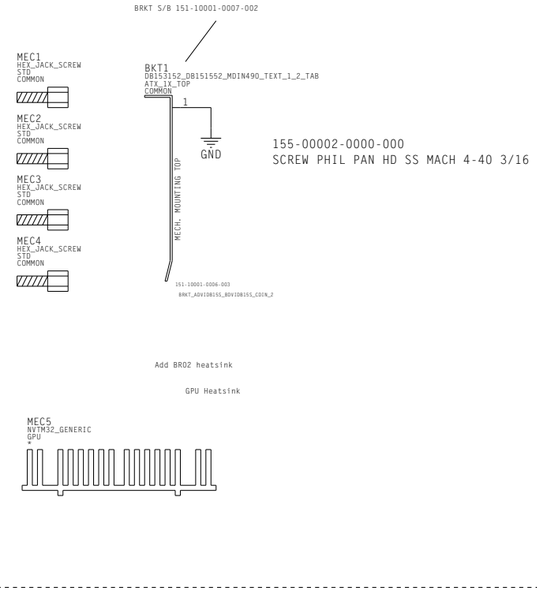
REG: NV_PEXTDEV_BOOT_0

Bit	Signal	VALUE_ID	VALUEs	
00:	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED	
			1 NORMAL	
01:	SUB_VENDOR	SUB_VENDOR	0 NO_BIOS	
			1 read from BIOS	
02:	RAM_CFG_0	RAM_CFG[3:0]	0000 RFU	1000 RFU
			0001 RFU	1001 RFU
03:	RAM_CFG_1		0010 RFU	1010 RFU
			0011 RFU	1011 RFU
04:	RAM_CFG_2		0100 RFU	1100 RFU
			0101 RFU	1101 RFU
05:	RAM_CFG_3		0110 RFU	1110 RFU
			0111 8Mx32 DDR3	1111 RFU
06:	CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz	
			01 14.31818 Mhz	
22:	CRYSTAL_1		10 27.000 Mhz	
			11 unknown	
07:	TV_MODE_0	TV_MODE[1:0]	00 SECAM	
			01 NTSC	
08:	TV_MODE_1		10 PAL	
			11 CRT	
09:	AGP8xEnable	AGP_3O_8x	0 AGP8x enabled	
			1 AGP8x disabled	
10:	AGP_SBA	AGP_SBA[0]	0 SBA enabled	
			1 SBA disabled	
11:	AGP_FASTWR	AGP_FASTWR[0]	0 enabled	
			1 disabled	
12:	PCI_DEVID_0	PCI_DEVID[3:0]	0000 0x140 ... 1111 0x014F	
			0000 (default 0x140)	
13:	PCI_DEVID_1			
20:	PCI_DEVID_2			
21:	PCI_DEVID_3			
14:	BUS_TYPE	BUS_TYPE[0]	0 PCI	
			1 AGP	
15:	FP_IFACE	FP_IFACE[0]	0 24Bit	
			1 12Bit (DEFAULT)	
23:	FB_0	FB[1:0]	00 64M	
			01 128M	
24:	FB_1		10 256M (DEFAULT)	
			11 512M	
25:	BR	BR[0]	0 BRIDGE disabled	
			1 BRIDGE enabled	
26:	BR_128M	BR bits are ignored if BRIDGE is disabled		
27:	BR_AGP			
28:	BR_IO			
29:	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel	
			01 Serial_AT25F	
30:	ROM_TYPE_1		10 Serial_SST45VF	
			11 RFU	
16:	USER_0	STRAP_USER[3:0]	0000 (default)	
17:	USER_1			
18:	USER_2			
19:	USER_3			

REG: NV_STRAP_1

Bit	Signal	VALUE_ID	VALUEs
11:	PEX_PLL_EN_TERM100		0 (default -- internal term on)
12:	3GIO_PADCFG_LUT_ADR[0]		
13:	3GIO_PADCFG_LUT_ADR[1]		
14:	3GIO_PADCFG_LUT_ADR[2]		

Mechanical parts



ASSEMBLY	NV43-U+BR02 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	STRAPS - Mechanical

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10218-0001-200		
ID	p218_a02	PAGE	25 OF 31
NAME	fwynhamer	DATE	27-SEP-2004

*** Signal Cross-Reference for the entire design ***

5V_FUSED	22.1G<> 22.3H
A3V3	3.4C 22.1A<
A3V3OK	22.1A< 22.2D< 24.4C>
AGPAD<31..0>	2.1D 2.4A>
AGPADSTBFO	2.3E 2.4A>
AGPADSTBF1	2.3E 2.4A>
AGPADSTBSO	2.3E 2.4A>
AGPADSTBS1	2.3E 2.4A>
AGPCAL_GND	2.4C 2.5A>
AGPCAL_VDDQ	2.4C 2.5A>
AGPCBE*<0>	2.2E
AGPCBE*<3..0>	2.4A>
AGPCBE*<1>	2.2E
AGPCBE*<2>	2.2E
AGPCBE*<3>	2.2E
AGPCLK_MA	2.4A>
AGPCLK_MB	2.4A>
AGPDBIHI_M	2.3D 2.4A>
AGPDBILO_M	2.3D 2.4A>
AGPDEVSEL_M	2.3D 2.4A>
AGPFRAME_M	2.2D 2.4A>
AGPGNT_M	2.2D 2.4A>
AGPIRDY_M	2.3D 2.4A>
AGPPAR_M	2.3D 2.4A>
AGPRBF_M	2.3D 2.4A>
AGPREQ_M	2.2D 2.4A>
AGPSBA_M*<7..0>	2.3D 2.5A>
AGPSBSTBF_M	2.3D 2.4A>
AGPSBSTBS_M	2.3D 2.5A>
AGPSERR	2.3D 2.4A>
AGPSTOP_M	2.3D 2.4A>
AGPST_M<0>	2.3D
AGPST_M<2..0>	2.4A>
AGPST_M<1>	2.3D
AGPST_M<2>	2.3D
AGPTRDY_M	2.3D 2.4A>
AGPVREF	2.4D 2.5A>
AGPVREFCG	6.1G<>
AGPWBF_M	2.3D 2.4A>
BRO2_REFCLK	5.1F 5.5B>
BRO2_REFCLK*	5.1F 5.5B>
BRO2_REFCLK_OUT	5.1D> 5.5B> 5.5B> 6.2A<
BRO2_REFCLK_OUT*	5.1D> 5.5B> 5.5B> 6.2A<
BRO2_RFCLKC	5.1F 5.5B>
BRO2_RFCLKC*	5.1F 5.5B>
DACA_BLUE	13.1A<> 13.5D
DACA_BLUE_C	13.1A<> 13.4G> 15.3G<
DACA_B_F	13.1A<> 13.5E
DACA_GREEN	13.1A<> 13.4D
DACA_GREEN_C	13.1A<> 13.4G> 15.3G<
DACA_G_F	13.1A<> 13.4E
DACA_HSYNC_C	13.3F> 15.3G<
DACA_RED	13.1A<> 13.4D
DACA_RED_C	13.1A<> 13.4G> 15.3G<
DACA_RSET	13.1A< 13.3B
DACA_R_F	13.1A<> 13.4E
DACA_VDD	13.1A< 13.3B
DACA_VREF	13.1A< 13.3B
DACA_VSYNC_C	13.3F> 15.3G<
DACBC_B_F	14.1A<> 14.5E
DACBC_G_F	14.1A<> 14.4E
DACBC_R_F	14.1A<> 14.4E
DACB_A3V3_ADJ	22.2G<> 22.3B
DACB_CVBS_OUT	19.1D 19.3G 19.4F>
DACB_C_OUT	19.1D 19.3C 19.4F> 19.5D
DACB_PB_OUT	19.1D 19.2C 19.4D 19.4F>
DACB_RSET	19.1B 19.5F<
DACB_VDD	19.1B 19.4F<
DACB_VREF	19.1B 19.4F<
DACC_BLUE	14.1A<> 14.4C
DACC_BLUE_C	14.1A<> 14.4G> 16.3G<
DACC_GREEN	14.1A<> 14.4C
DACC_GREEN_C	14.1A<> 14.4G> 16.3G<
DACC_HSYNC_C	14.3F> 16.3G<
DACC_RED	14.1A<> 14.4C
DACC_RED_C	14.1A<> 14.4G> 16.3G<
DACC_RSET	14.1A<> 14.4A
DACC_VDD	14.1A<> 14.4A
DACC_VREF	14.1A<> 14.4A
DACC_VSYNC_C	14.2F> 16.3G<
DVI_MID_HPD	16.5C> 21.1D<
DVI_SOUTH_HPD	15.5C> 21.1D<
EXTSENSE5	21.2D< 21.2D< 22.5F>
EXTSENSE12	22.4F> 23.4G< 24.1A< 24.4F<
EXTSENSE12*	22.4F> 23.1A< 24.1A<
FBAD<0>	7.1B 8.4C
FBAD<63..0>	7.1A<> 8.1G<> 8.4B<>
FBAD<1>	7.1B 8.4C
FBAD<2>	7.1B 8.4C
FBAD<3>	7.1B 8.4C
FBAD<4>	7.1B 8.4C
FBAD<5>	7.1B 8.4C
FBAD<6>	7.1B 8.4C
FBAD<7>	7.1B 8.4C
FBAD<8>	7.1B 8.4D
FBAD<9>	7.1B 8.4D
FBAD<10>	7.1B 8.4D
FBAD<11>	7.1B 8.4D
FBAD<12>	7.1B 8.4D
FBAD<13>	7.1B 8.4D
FBAD<14>	7.1B 8.4D
FBAD<15>	7.1B 8.4D
FBAD<16>	7.1B 8.4E
FBAD<17>	7.1B 8.4E
FBAD<18>	7.1B 8.4E
FBAD<19>	7.2B 8.4E
FBAD<20>	7.2B 8.4E
FBAD<21>	7.2B 8.4E
FBAD<22>	7.2B 8.4E
FBAD<23>	7.2B 8.4E
FBAD<24>	7.2B 8.4E
FBAD<25>	7.2B 8.4E
FBAD<26>	7.2B 8.4E
FBAD<27>	7.2B 8.4E
FBAD<28>	7.2B 8.4E
FBAD<29>	7.2B 8.4E
FBAD<30>	7.2B 8.4E
FBAD<31>	7.2B 8.4E
FBAD<32>	7.2B 8.5C
FBAD<33>	7.2B 8.5C
FBAD<34>	7.2B 8.5C
FBAD<35>	7.2B 8.5C
FBAD<36>	7.2B 8.5C
FBAD<37>	7.2B 8.5C
FBAD<38>	7.2B 8.5C
FBAD<39>	7.2B 8.5C
FBAD<40>	7.2B 8.5D
FBAD<41>	7.2B 8.5D
FBAD<42>	7.2B 8.5D
FBAD<43>	7.2B 8.5D
FBAD<44>	7.2B 8.5D
FBAD<45>	7.2B 8.5D
FBAD<46>	7.2B 8.5D
FBAD<47>	7.2B 8.5D
FBAD<48>	7.2B 8.5E
FBAD<49>	7.3B 8.5E
FBAD<50>	7.3B 8.5E
FBAD<51>	7.3B 8.5E
FBAD<52>	7.3B 8.5E
FBAD<53>	7.3B 8.5E
FBAD<54>	7.3B 8.5E
FBAD<55>	7.3B 8.5E
FBAD<56>	7.3B 8.5E
FBAD<57>	7.3B 8.5E
FBAD<58>	7.3B 8.5E
FBAD<59>	7.3B 8.5E
FBAD<60>	7.3B 8.5E
FBAD<61>	7.3B 8.5E
FBAD<62>	7.3B 8.5E
FBAD<63>	7.3B 8.5E
FBADQM<0>	7.3B 8.4B 8.4C
FBADQM<7..0>	7.3A> 8.1G<> 8.4B<>
FBADQM<1>	7.3B 8.4B 8.4D
FBADQM<2>	7.3B 8.4B 8.4E
FBADQM<3>	7.3B 8.4B 8.4E
FBADQM<4>	7.3B 8.4B 8.5C
FBADQM<5>	7.3B 8.4B 8.5D
FBADQM<6>	7.3B 8.4B 8.5E
FBADQM<7>	7.3B 8.4B 8.5E
FBADQS_RN<0>	7.4B 8.1G<> 8.4B 8.4C
FBADQS_RN<7..0>	7.4A<> 8.4B<>
FBADQS_RN<1>	7.4B 8.1G<> 8.4B 8.4D
FBADQS_RN<2>	7.4B 8.1G<> 8.4B 8.4E
FBADQS_RN<3>	7.4B 8.1G<> 8.4B 8.4E
FBADQS_RN<4>	7.4B 8.1G<> 8.5B 8.5C
FBADQS_RN<5>	7.4B 8.1G<> 8.5B 8.5D
FBADQS_RN<6>	7.4B 8.1G<> 8.5B 8.5E
FBADQS_RN<7>	7.4B 8.1G<> 8.5B 8.5E
FBADQS_WP<0>	7.3B 8.1G<> 8.4C 8.5B
FBADQS_WP<7..0>	7.3A<> 8.5B<>
FBADQS_WP<1>	7.3B 8.1G<> 8.4D 8.5B
FBADQS_WP<2>	7.3B 8.1G<> 8.4E 8.5B
FBADQS_WP<3>	7.4B 8.1G<> 8.4E 8.5B
FBADQS_WP<4>	7.4B 8.1G<> 8.5B 8.5C
FBADQS_WP<5>	7.4B 8.1G<> 8.5B 8.5D
FBADQS_WP<6>	7.4B 8.1G<> 8.5B 8.5E
FBADQS_WP<7>	7.4B 8.2G<> 8.5B 8.5E
FBA_CLKO	7.4D> 8.1G< 8.2A< 8.2C
FBA_CLKO*	7.4D> 8.1G< 8.2A< 8.2C
FBA_CLK1	7.4D> 8.1G< 8.2C 8.2D<
FBA_CLK1*	7.4D> 8.1G< 8.2C 8.2D<
FBA_CMD<0>	7.3C 8.1B 8.1C
FBA_CMD<26..0>	7.3D> 8.1A< 8.1C 8.1D 8.1G<
FBA_CMD<1>	7.3C 8.1B 8.1E
FBA_CMD<2>	7.3C 8.1B 8.1C
FBA_CMD<3>	7.3C 8.1B 8.1E
FBA_CMD<4>	7.3C 8.1E 8.2C
FBA_CMD<5>	7.3C 8.1E 8.2C
FBA_CMD<6>	7.3C 8.1E 8.2C
FBA_CMD<8>	7.3C 8.1B 8.1E
FBA_CMD<9>	7.3C 8.1B 8.1E
FBA_CMD<10>	7.3C 8.2B 8.2E
FBA_CMD<11>	7.3C 7.3G 8.2B 8.2E
FBA_CMD<12>	7.3C 8.2B 8.2E
FBA_CMD<13>	7.3C 8.1C 8.1E
FBA_CMD<14>	7.3C 8.2B 8.2E
FBA_CMD<15>	7.3C 8.1B 8.1E
FBA_CMD<16>	7.3C 8.1B 8.1E
FBA_CMD<17>	7.3C 8.1B 8.1E
FBA_CMD<18>	7.3C 8.2B 8.2E
FBA_CMD<19>	7.3C 8.1B 8.1E
FBA_CMD<20>	7.3C 8.1B 8.1E
FBA_CMD<21>	7.3C 8.1B 8.1E
FBA_CMD<22>	7.3C 8.1B 8.1C
FBA_CMD<23>	7.3C 8.1B 8.1E
FBA_CMD<24>	7.3C 8.1B 8.1C
FBA_CMD<25>	7.3C 8.1B 8.1E
FBA_PLLAVDD	7.1F< 7.4C
FBA_PLLVDD	7.1F< 7.4C 7.4E
FBA_REFCLK	7.1F< 7.4C
FBA_REFCLK*	7.1F< 7.4C
FBA_VREF_ADDR0	8.2G<> 8.3C
FBA_VREF_ADDR1	8.2G<> 8.3F
FBA_VREF_DATA0	8.2G<> 8.3C
FBA_VREF_DATA1	8.2G<> 8.3F
FBCD<0>	10.1B 11.4C
FBCD<63..0>	10.1A<> 11.1G<> 11.4B<>
FBCD<1>	10.1B 11.4C
FBCD<2>	10.1B 11.4C
FBCD<3>	10.1B 11.4C
FBCD<4>	10.1B 11.4C
FBCD<5>	10.1B 11.4C
FBCD<6>	10.1B 11.4C
FBCD<7>	10.1B 11.4C
FBCD<8>	10.1B 11.4D
FBCD<9>	10.1B 11.4D
FBCD<10>	10.1B 11.4D
FBCD<11>	10.1B 11.4D
FBCD<12>	10.1B 11.4D
FBCD<13>	10.1B 11.4D
FBCD<14>	10.1B 11.4D
FBCD<15>	10.1B 11.4D
FBCD<16>	10.1B 11.4E
FBCD<17>	10.1B 11.4E
FBCD<18>	10.1B 11.4E
FBCD<19>	10.1B 11.4E
FBCD<20>	10.1B 11.4E
FBCD<21>	10.2B 11.4E
FBCD<22>	10.2B 11.4E
FBCD<23>	10.2B 11.4E
FBCD<24>	10.2B 11.4E
FBCD<25>	10.2B 11.4E
FBCD<26>	10.2B 11.4E
FBCD<27>	10.2B 11.4E
FBCD<28>	10.2B 11.4E
FBCD<29>	10.2B 11.4E
FBCD<30>	10.2B 11.4E
FBCD<31>	10.2B 11.4E
FBCD<32>	10.2B 11.5C
FBCD<33>	10.2B 11.5C
FBCD<34>	10.2B 11.5C
FBCD<35>	10.2B 11.5C
FBCD<36>	10.2B 11.5C
FBCD<37>	10.2B 11.5C
FBCD<38>	10.2B 11.5C
FBCD<39>	10.2B 11.5C
FBCD<40>	10.2B 11.5D
FBCD<41>	10.2B 11.5D
FBCD<42>	10.2B 11.5D
FBCD<43>	10.2B 11.5D
FBCD<44>	10.2B 11.5D
FBCD<45>	10.2B 11.5D
FBCD<46>	10.2B 11.5D
FBCD<47>	10.2B 11.5D
FBCD<48>	10.2B 11.5E
FBCD<49>	10.2B 11.5E
FBCD<50>	10.2B 11.5E
FBCD<51>	10.3B 11.5E
FBCD<52>	10.3B 11.5E
FBCD<53>	10.3B 11.5E
FBCD<54>	10.3B 11.5E
FBCD<55>	10.3B 11.5E
FBCD<56>	10.3B 11.5E
FBCD<57>	10.3B 11.5E
FBCD<58>	10.3B 11.5E
FBCD<59>	10.3B 11.5E
FBCD<60>	10.3B 11.5E
FBCD<61>	10.3B 11.5E
FBCD<62>	10.3B 11.5E
FBCD<63>	10.3B 11.5E
FBCDQM<0>	10.3B 11.4B 11.4C
FBCDQM<7..0>	10.3A> 11.1G<> 11.4B<>
FBCDQM<1>	10.3B 11.4B 11.4D
FBCDQM<2>	10.3B 11.4B 11.4E
FBCDQM<3>	10.3B 11.4B 11.4E
FBCDQM<4>	10.3B 11.4B 11.5C
FBCDQM<5>	10.3B 11.4B 11.5D
FBCDQM<6>	10.3B 11.4B 11.5E
FBCDQM<7>	10.3B 11.4B 11.5E
FBCDQS_RN<0>	10.4B 11.1G<> 11.4B 11.4C
FBCDQS_RN<7..0>	10.4A<> 11.4B<>
FBCDQS_RN<1>	10.4B 11.1G<> 11.4B 11.4D
FBCDQS_RN<2>	10.4B 11.1G<> 11.4B 11.4E
FBCDQS_RN<3>	10.4B 11.1G<> 11.4E 11.5B
FBCDQS_RN<4>	10.4B 11.2G<> 11.5B 11.5C
FBCDQS_RN<5>	10.4B 11.2G<> 11.5B 11.5D
FBCDQS_RN<6>	10.4B 11.2G<> 11.5B 11.5E
FBCDQS_RN<7>	10.4B 11.2G<> 11.5B 11.5E
FBCDQS_WP<0>	10.3B 11.1G<> 11.4C 11.5B
FBCDQS_WP<7..0>	10.3A<> 11.5B<>
FBCDQS_WP<1>	10.3B 11.1G<> 11.4D 11.5B
FBCDQS_WP<2>	10.3B 11.1G<> 11.4E 11.5B
FBCDQS_WP<3>	10.3B 11.1G<> 11.4E 11.5B
FBCDQS_WP<4>	10.3B 11.2G<> 11.5B 11.5C
FBCDQS_WP<5>	10.4B 11.2G<> 11.5B 11.5D
FBCDQS_WP<6>	10.4B 11.2G<> 11.5B 11.5E
FBCDQS_WP<7>	10.4B 11.2G<> 11.5B 11.5E
FBC_CLKO	10.4D> 11.1G< 11.2A< 11.2D
FBC_CLKO*	10.4D> 11.1G< 11.2A< 11.2D
FBC_CLK1	10.4D> 11.1G< 11.2D< 11.2D
FBC_CLK1*	10.4D> 11.1G< 11.2D 11.2D<
FBC_CMD<0>	10.3C 11.1B 11.1D
FBC_CMD<26..0>	10.3D> 11.1A< 11.1C 11.1D 11.1G<
FBC_CMD<1>	10.3C 11.1B 11.1E
FBC_CMD<2>	10.3C 11.1B 11.1D
FBC_CMD<3>	10.3C 11.1B 11.1E
FBC_CMD<4>	10.3C 11.1E 11.2D
FBC_CMD<5>	10.3C 11.1E 11.2D
FBC_CMD<6>	10.3C 11.1E 11.2D
FBC_CMD<8>	10.3C 11.1B 11.1E
FBC_CMD<9>	10.3C 11.1B 11.1E
FBC_CMD<10>	10.3C 11.2B 11.2E
FBC_CMD<11>	10.3C 10.3G 11.2B 11.2E
FBC_CMD<12>	10.3C 11.2B 11.2E
FBC_CMD<13>	10.3C 11.1E 11.2D
FBC_CMD<14>	10.3C 11.2B 11.2E
FBC_CMD<15>	10.3C 11.1B 11.1E
FBC_CMD<16>	10.3C 11.2B 11.2E
FBC_CMD<17>	10.3C 11.1B 11.1E
FBC_CMD<18>	10.3C 11.2B 11.2E
FBC_CMD<19>	10.3C 11.1B 11.1E
FBC_CMD<20>	10.3C 11.1B 11.1E
FBC_CMD<21>	10.3C 11.1B 11.1E
FBC_CMD<22>	10.3C 11.1B 11.1D
FBC_CMD<23>	10.3C 11.1B 11.1E
FBC_CMD<24>	10.3C 11.1B 11.1D
FBC_CMD<25>	10.3C 11.1B 11.1E
FBC_PLLAVDD	10.1F< 10.4C
FBC_PLLVDD	10.1F< 10.4C
FBC_REFCLK	10.1F< 10.4C
FBC_REFCLK*	10.1F< 10.4C
FBC_VREF_ADDR0	11.2G<> 11.3C
FBC_VREF_ADDR1	11.2G<> 11.3F
FBC_VREF_DATA0	11.2G<> 11.3C
FBC_VREF_DATA1	11.2G<> 11.3F
GND_SENSE	6.3F> 6.3F> 6.5G<> 24.1G<
GPIO5_VSEL0	21.1D> 24.4F<
GPIO6_VSEL1	21.1D> 23.4G<
GPIO10_480P	19.5A< 21.2D>
GPIO11_TVRSET	19.1A< 21.2D>
I2CA_SCL_C	13.2F> 15.3G<
I2CA_SDA_C	13.1F> 15.3G<
I2CB_SCL_C	14.2F> 16.3G<
I2CB_SDA_C	14.1F> 16.3G<

ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
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I2CC_SCL	18.3A< 19.2H< 21.1D< 21.3B
I2CC_SDA	18.3A<> 19.2H<> 21.1D<> 21.3B
IFPABRSET	15.2B 15.4G<>
IFPAB_IOVDD	15.3B 15.4G<>
IFPAB_PLLVDD	15.2B 15.4G<>
IFPCD_IOVDD	16.3B 16.4G<>
IFPCD_PLLVDD	16.2B 16.4G<>
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JT_TDI_GPU	4.2B> 21.1A<
JT_TDO_GPU	18.2G< 21.1A>
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JT_TMS	4.2B> 18.2G< 21.1A<
JT_TRST*	4.2B> 18.2G< 21.1A<
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MDIN_CIN_CLAMP	19.3F 19.4F<>
MDIN_COUT_C	19.3D 19.4F<>
MDIN_PBOUT_C	19.2D 19.4F<>
MDIN_YIN_C	19.3D 19.4F<>
MDIN_YIN_CLAMP	19.3C 19.4F<>
MDIN_YOUT_C	19.3E 19.4F<>
MINIDIN_CIN	18.2A< 19.3G> 19.4F<>
MINIDIN_Y_CVBSIN	18.2A< 19.3B> 19.4F<>
MIOA2V5_VREF	22.1G<>
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MIOAD<9..0>	17.4E< 25.1A>
MIOAD<11..0>	17.1G<>
MIOAD<1>	17.4D 25.1A 25.2B
MIOAD<2>	17.4D 25.1A 25.4B
MIOAD<6>	25.1A 25.5B
MIOAD<8>	17.4D 25.1A 25.5B
MIOAD<9>	17.4D 25.1A 25.5B
MIOA_CLKOUT	17.1G<>
MIOA_CLKOUT*	17.1G<>
MIOA_HSYNC	17.4E>
MIOA_VREF	17.1G<>
MIOA_VSYNC	17.5E>
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MIOBD<11..0>	17.1E<> 25.2A<>
MIOBD<1>	17.2D 18.3D 25.2A 25.2B
MIOBD<2>	17.2D 18.3D
MIOBD<3>	17.2D 18.3D 25.2A 25.3B
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MIOBD<5>	17.2D 18.3D 25.2A 25.3B
MIOBD<6>	17.2D 18.3D 25.2A
MIOBD<7>	17.2D 18.3D 25.2A
MIOBD<8>	17.2D 25.2A 25.2B
MIOBD<9>	17.2D 25.2A 25.3B
MIOBD<10>	17.2D 25.2A 25.4B
MIOBD<11..10>	17.1G<>
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MIOB_VREF	17.1G<> 17.2C
NVVDD_SENSE	6.3F> 6.3F> 6.5G<> 24.1G<
PCIINTA_M*	2.3D 2.4A>
PCIINTB*	2.4A>
PCIPME*	2.4A>
PCIRST_M*	2.2D> 2.4A> 4.3B< 4.3B< 4.3B<
PCIRST_MB*	2.5A>
PEXBR_TX0A	5.1B> 5.1D
PEXBR_TX0A*	5.1B> 5.1D
PEXBR_TX1A	5.1B> 5.1D
PEXBR_TX1A*	5.1B> 5.1D
PEXBR_TX2A	5.1B> 5.2D
PEXBR_TX2A*	5.2B> 5.2D
PEXBR_TX3A	5.2B> 5.2D
PEXBR_TX3A*	5.2B> 5.2D
PEXBR_TX4A	5.2B> 5.2D
PEXBR_TX4A*	5.2B> 5.2D
PEXBR_TX5A	5.2B> 5.2D
PEXBR_TX5A*	5.2B> 5.2D
PEXBR_TX6A	5.2B> 5.2D
PEXBR_TX6A*	5.2B> 5.2D
PEXBR_TX7A	5.2B> 5.3D
PEXBR_TX7A*	5.3B> 5.3D
PEXBR_TX8A	5.3B> 5.3D
PEXBR_TX8A*	5.3B> 5.3D
PEXBR_TX9A	5.3B> 5.3D
PEXBR_TX9A*	5.3B> 5.3D
PEXBR_TX10A	5.3B> 5.3D
PEXBR_TX10A*	5.3B> 5.3D
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PEXBR_TX11A*	5.3B> 5.3D
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PEXBR_TX12A*	5.4B> 5.4D
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PEXBR_TX13A*	5.4B> 5.4D
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PEXBR_TX14A*	5.4B> 5.4D
PEXBR_TX15A	5.4B> 5.4D
PEXBR_TX15A*	5.4B> 5.4D

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PEX_BRG_TX7*	5.3B> 5.3C> 6.4A<
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PEX_GPU_TXX1*	5.1B> 5.1C< 6.2A>
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PEX_GPU_TXX3	5.2B> 5.2C< 6.3A>
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PEX_GPU_TXX4	5.2B> 5.2C< 6.3A>
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PEX_GPU_TXX5	5.2B> 5.2C< 6.3A>
PEX_GPU_TXX5*	5.2B> 5.2C< 6.3A>
PEX_GPU_TXX6	5.2B> 5.2C< 6.3A>
PEX_GPU_TXX6*	5.2B> 5.2C< 6.3A>
PEX_GPU_TXX7	5.3B> 5.3C< 6.3A>
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PEX_GPU_TXX8*	5.3B> 5.3C< 6.4A>
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PEX_GPU_TXX10	5.3B> 5.3C< 6.4A>
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PEX_GPU_TXX12*	5.3C< 5.4B> 6.4A>
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PEX_TSTCLK_OUT	5.4F 5.5B>
PEX_TSTCLK_OUT*	5.4F 5.5B>
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PEX_TX1	6.2C 6.2G<>
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PEX_TX2	6.2C 6.2G<>
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PEX_TX6	6.2G<> 6.3C
PEX_TX6*	6.2G<> 6.3C
PEX_TX7	6.2G<> 6.3C
PEX_TX7*	6.2G<> 6.3C
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PEX_TX9*	6.2G<> 6.4C
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PEX_TX11	6.2G<> 6.4C

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PEX_TX12*	6.2G<> 6.4C
PEX_TX13	6.2G<> 6.5C
PEX_TX13*	6.2G<> 6.5C
PEX_TX14	6.2G<> 6.5C
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SEC_CVBS1A	20.3A<>
SEC_LUMA	20.3A<>
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VREFGC	2.4F 2.5A>
XTALIN	20.2C 20.3A<
XTALOUT	20.2D 20.3A<

NVIDIA CORPORATION
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*** Part Cross-Reference for the entire design ***

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ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
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D10	D_SCHOTTKY	24
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D503	D_SCHOTTKY_3PIN_AA	24
D504	D_SCHOTTKY_3PIN_AA	23
D505	D_3PIN_AA	24
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D520	D_3PIN_AC	13
D521	D_3PIN_AC	14
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F501	F_POLYSW	22
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J2	CON_DSUB15HD	13
J3	CON_MINIDIN_10	19
J4	CON_DVI_I	16
J5	CON_DVI_I	15
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J7	HDR_1X4	22
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ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
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TP3	TESTPOINT	24
TP4	TESTPOINT	23
TP5	TESTPOINT	23
TP6	TESTPOINT	23
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U2	U_MEM_SD_DDR3_X32	11
U3	U_AND_2IN	21
U4	U_TEMP_AD1032	21
U5	U_MEM_EE_CRYPT_8X128	21
U6	U_MEM_SD_DDR3_X32	11
U7	U_GPU_G3	6 7 10 13 14 15 16 17 19 20 21
U8	U_MEM_SD_DDR3_X32	8
U9	U_BRDG_BRO2	2 3 4 5
U10	U_MEM_SD_DDR3_X32	8
U501	U_SWREG_ISL6534	24
U502	U_COMP	22
U503	U_SWREG_ISL6549	23
U504	U_CLK_ICS843011	5
U505	U_VREG_5PIN	22
U506	U_VREG_3PIN	22
U507	U_VDEC_SAA71XX	18
U508	U_OPAMP	19
U509	U_OPAMP	19
U510	U_AND_2IN	13 14
Y1	XTAL_4PIN	20
Y2	XTAL_4PIN	5
Y501	XTAL	18

ASSEMBLY	NV43-U+BRO2 AGP board, 8Mx32 DDR3, 128MB/128-bit, VGA + DVI-I + VIDEO-In + HDTV-out +Thermal
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