

P654 - GT200/NVIO2

P654, GT200-100, 896MB/1792MB - GDDR3 BGA136 16M/32Mx32

DVI-I + DVI-I/DP + HD/SD/TVout, SPDIF, Dual SLI

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2	SKU001	600-10654-0001-000	DT, GT200-100, 550/350/1000, 896MB - 16MX32 GDDR3, DVI-I + DP + HDTV
3	SKU001	600-10654-0051-300	DT, GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
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PAGE 21:VGS SLIM  
PAGE-22 remove DACB HDTV Circuit  
PAGE 24:DVI change HDMI  
PAGE 25:DP modify DSDA/DSCL circuit  
PAGE 28:ADD I2C0\_SCL/SDA and GPIO 3 circuit,remove GPIO 12  
PAGE 29:remove R112,R113 and GPIO8\_FAN\_TACH link to U21  
PAGE 33:remove R671,R572  
PAGE 35:remove RT8805CQVA change UPI6205 and UPI6262 circuit  
PAGE 36:remove NCP5388MNR2G change UPI6208 circuit  
PAGE 37/38 :remove NCP3418B change UPI6281 circuit  
PAGE 39 :Add WL83L786G circuit

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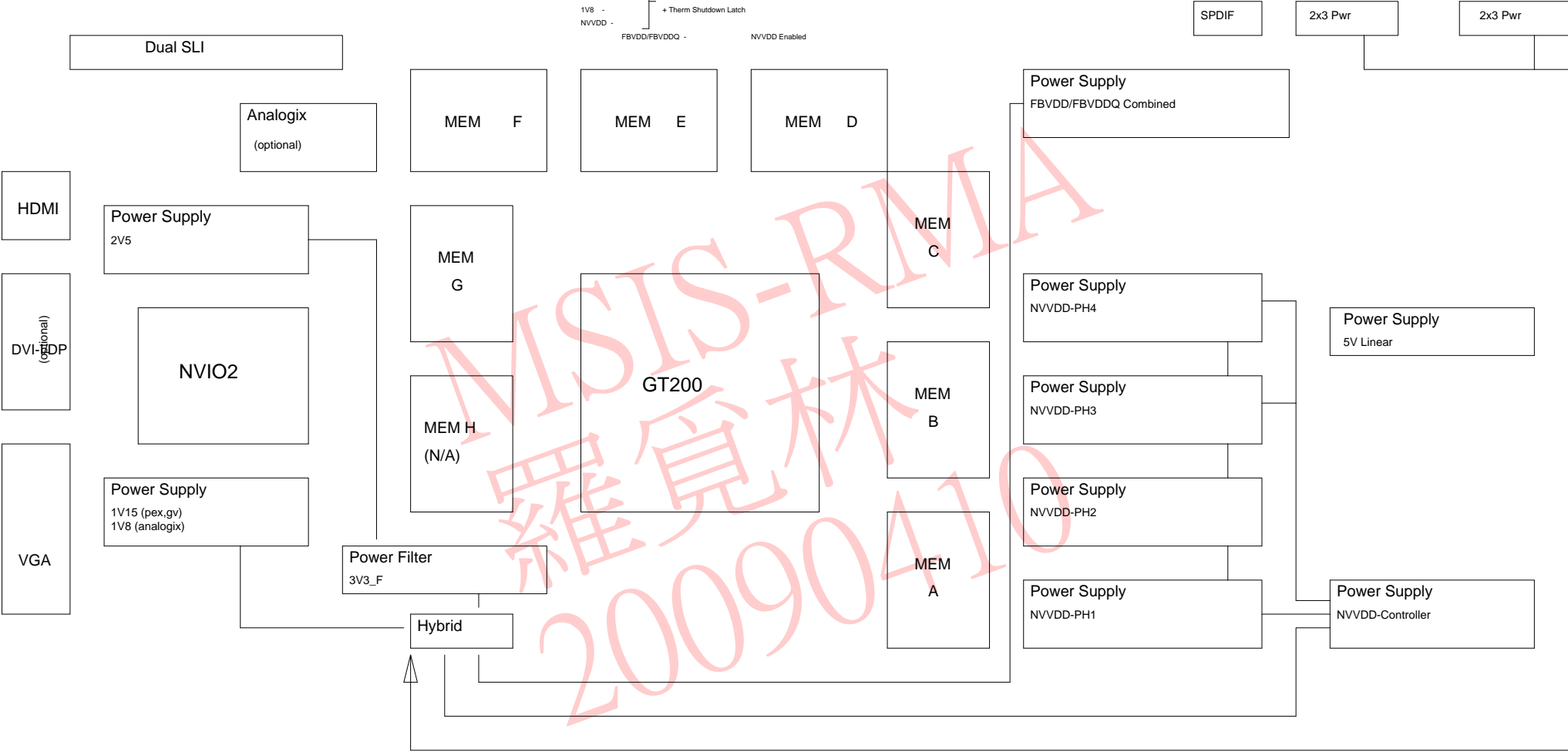
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Block Diagram

Power Sequence

- 5V - Always On
- 3V3 - Always On
- 12V\_F - Always On
- 12V\_PEX6\_F1 - Always On
- 12V\_PEX6\_F2 - Always On
- 3V3\_DP - Always On

- 3V3\_F - Hybrid Enable
- 2V5 - + Input\_PEX\_Enable
- 1V15 - + Therm Shutdown Latch
- 1V8 -
- NVVDQ - FBVDD/FBVDDQ - NVVDD Enabled



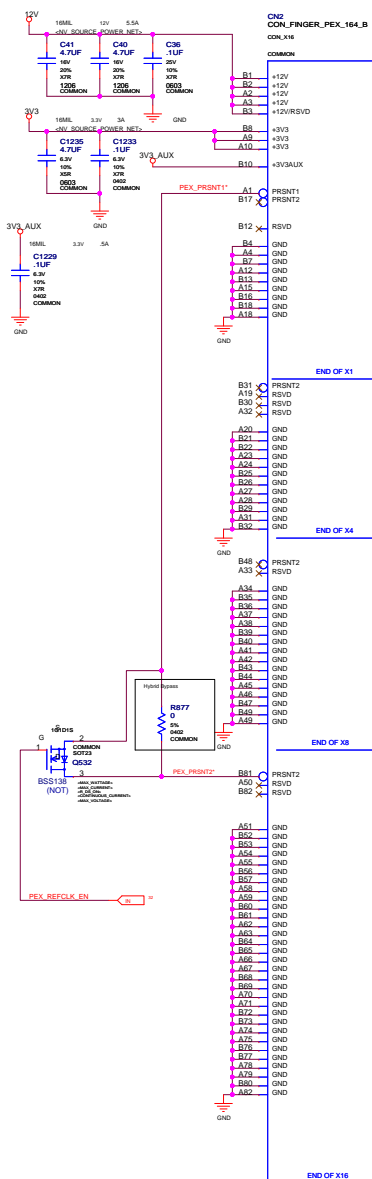
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Block Diagram

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## PCI Express / JTAG

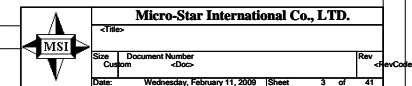


## JTAG



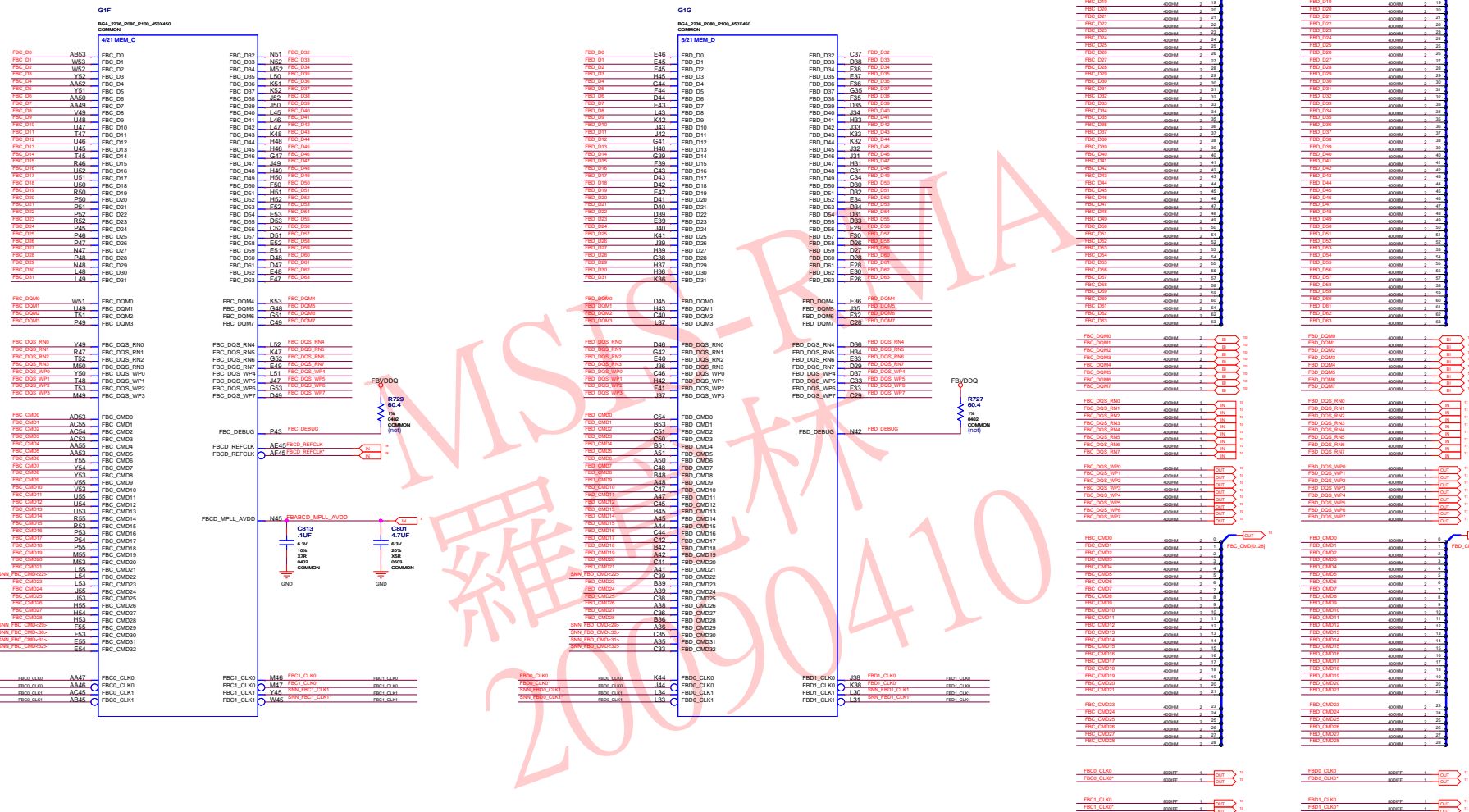
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PAGE DETAIL	PCI Express / JTAG





Framebuffer C,D: GPU Section



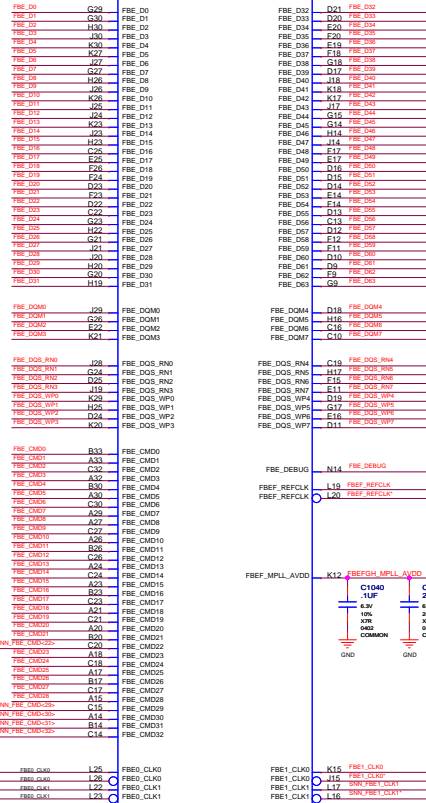
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# Framebuffer E,F: GPU Section

G1H

PGA\_238L\_P080\_P100\_400460

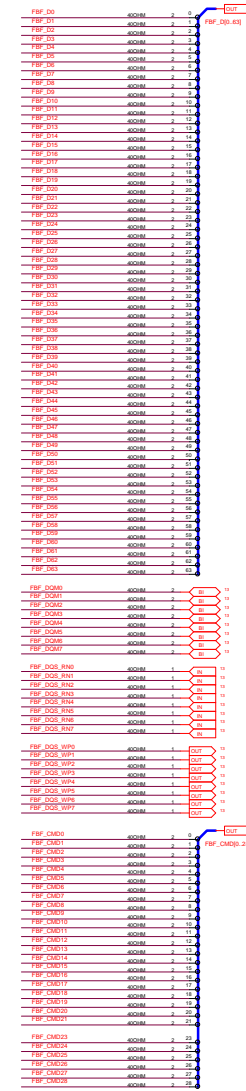
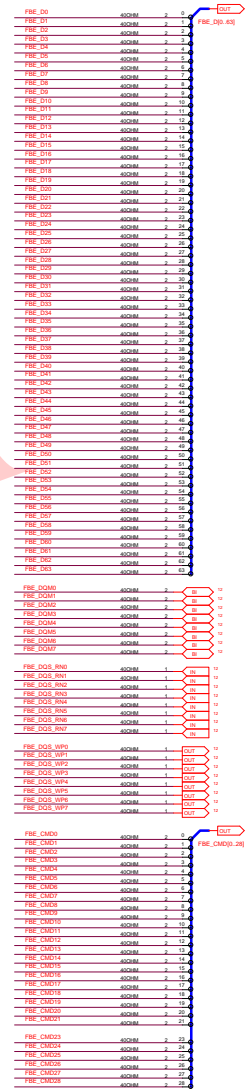
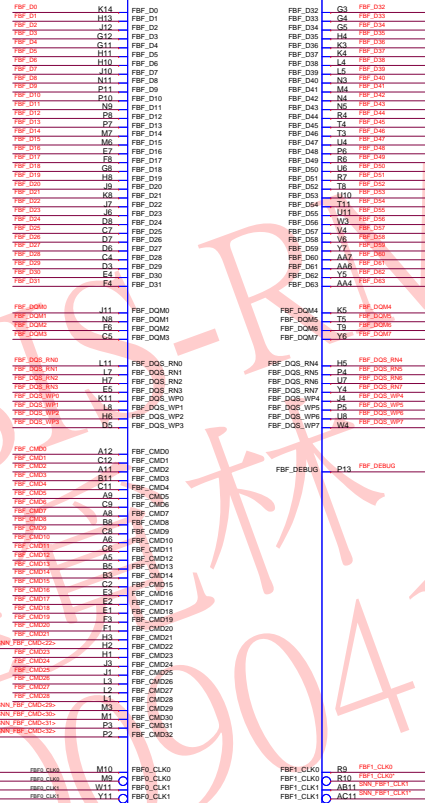
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G1H

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702 MEM\_F



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Framebuffer E,F: GPU Section

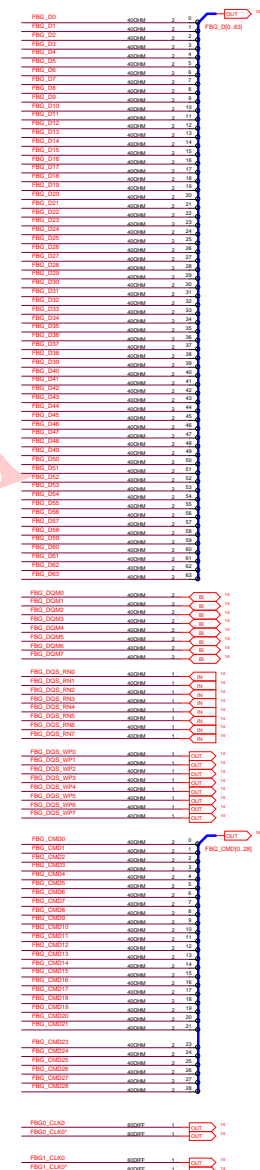
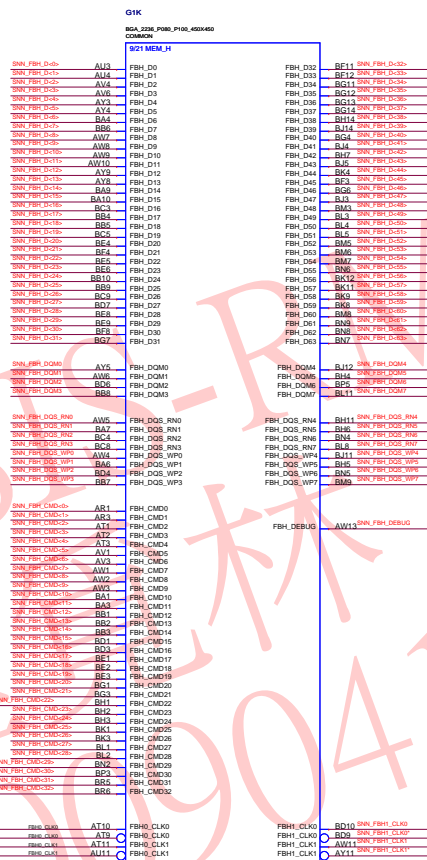
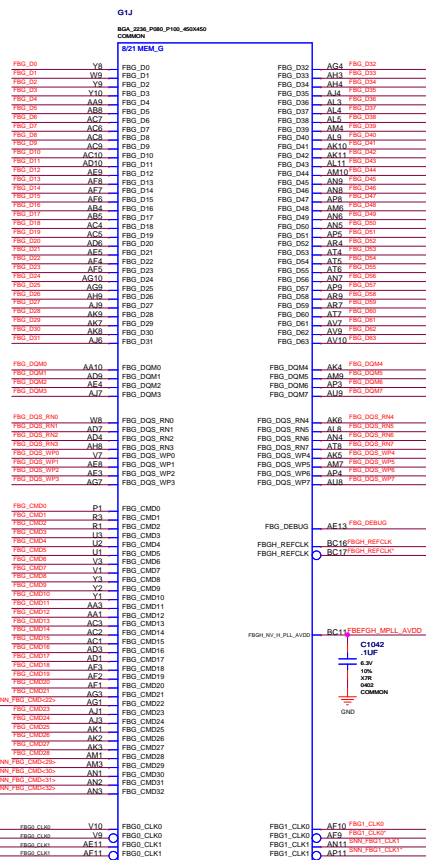
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Framebuffer G,H: GPU Section



The schematic diagram illustrates the BGA\_0136\_P0B0\_140X110 board layout, organized into four primary sections: M13B, M13D, M13C, and M13A. Each section provides a detailed pinout and connection list for the BGA package, including power, ground, and signal pins. The diagram is divided into 'NONMIRRORED' and 'MIRRORED' configurations, indicating the board's layout symmetry. A large red watermark 'Schematic' is overlaid on the diagram.

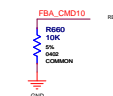
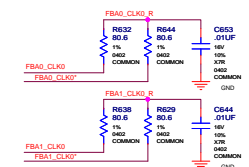
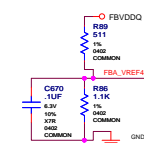
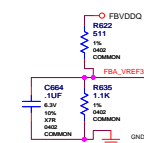
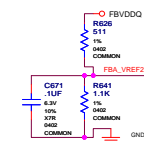
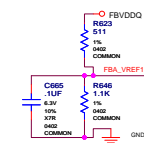
**Section M13B:** This section lists the pinout for the BGA package, including power pins (VDD, VSS, VDDA, VSSA), ground pins (GND), and signal pins (FBVDDQ, FBVDDQ, FBVDDQ, FBVDDQ). It also includes a 'NONMIRRORED' label.

**Section M13D:** This section lists the pinout for the BGA package, including power pins (VDD, VSS, VDDA, VSSA), ground pins (GND), and signal pins (FBVDDQ, FBVDDQ, FBVDDQ, FBVDDQ). It also includes a 'MIRRORED' label.

**Section M13C:** This section lists the pinout for the BGA package, including power pins (VDD, VSS, VDDA, VSSA), ground pins (GND), and signal pins (FBVDDQ, FBVDDQ, FBVDDQ, FBVDDQ). It also includes a 'MIRRORED' label.

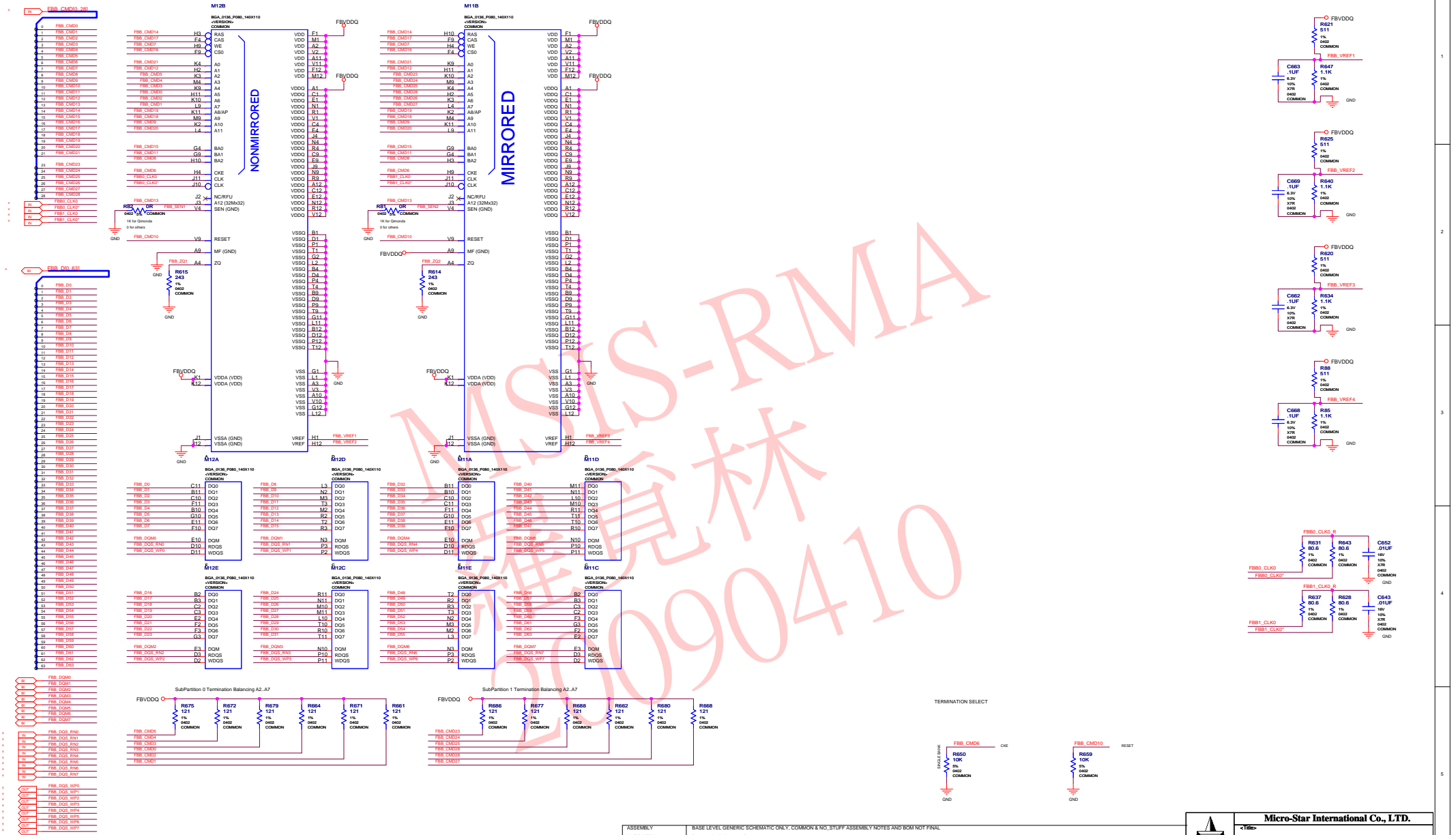
**Section M13A:** This section lists the pinout for the BGA package, including power pins (VDD, VSS, VDDA, VSSA), ground pins (GND), and signal pins (FBVDDQ, FBVDDQ, FBVDDQ, FBVDDQ). It also includes a 'MIRRORED' label.

The diagram also includes a 'SubPartition 0 Termination Balancing A2-A7' section, which shows the termination balancing for the A2-A7 pins. This section includes a list of components (R864, R865, R866, R867, R868, R869, R870, R871, R872, R873, R874, R875, R876, R877, R878, R879, R880, R881, R882, R883, R884, R885, R886, R887, R888, R889, R890, R891, R892, R893, R894, R895, R896, R897, R898, R899, R900, R901, R902, R903, R904, R905, R906, R907, R908, R909, R910, R911, R912, R913, R914, R915, R916, R917, R918, R919, R920, R921, R922, R923, R924, R925, R926, R927, R928, R929, R930, R931, R932, R933, R934, R935, R936, R937, R938, R939, R940, R941, R942, R943, R944, R945, R946, R947, R948, R949, R950, R951, R952, R953, R954, R955, R956, R957, R958, R959, R960, R961, R962, R963, R964, R965, R966, R967, R968, R969, R970, R971, R972, R973, R974, R975, R976, R977, R978, R979, R980, R981, R982, R983, R984, R985, R986, R987, R988, R989, R990, R991, R992, R993, R994, R995, R996, R997, R998, R999, R1000, R1001, R1002, R1003, R1004, R1005, R1006, R1007, R1008, R1009, R1010, R1011, R1012, R1013, R1014, R1015, R1016, R1017, R1018, R1019, R1020, R1021, R1022, R1023, R1024, R1025, R1026, R1027, R1028, R1029, R1030, R1031, R1032, R1033, R1034, R1035, R1036, R1037, R1038, R1039, R1040, R1041, R1042, R1043, R1044, R1045, R1046, R1047, R1048, R1049, R1050, R1051, R1052, R1053, R1054, R1055, R1056, R1057, R1058, R1059, R1060, R1061, R1062, R1063, R1064, R1065, R1066, R1067, R1068, R1069, R1070, R1071, R1072, R1073, R1074, R1075, R1076, R1077, R1078, R1079, R1080, R1081, R1082, R1083, R1084, R1085, R1086, R1087, R1088, R1089, R1090, R1091, R1092, R1093, R1094, R1095, R1096, R1097, R1098, R1099, R1100, R1101, R1102, R1103, R1104, R1105, R1106, R1107, R1108, R1109, R1110, R1111, R1112, R1113, R1114, R1115, R1116, R1117, R1118, R1119, R1120, R1121, R1122, R1123, R1124, R1125, R1126, R1127, R1128, R1129, R1130, R1131, R1132, R1133, R1134, R1135, R1136, R1137, R1138, R1139, R1140, R1141, R1142, R1143, R1144, R1145, R1146, R1147, R1148, R1149, R1150, R1151, R1152, R1153, R1154, R1155, R1156, R1157, R1158, R1159, R1160, R1161, R1162, R1163, R1164, R1165, R1166, R1167, R1168, R1169, R1170, R1171, R1172, R1173, R1174, R1175, R1176, R1177, R1178, R1179, R1180, R1181, R1182, R1183, R1184, R1185, R1186, R1187, R1188, R1189, R1190, R1191, R1192, R1193, R1194, R1195, R1196, R1197, R1198, R1199, R1200, R1201, R1202, R1203, R1204, R1205, R1206, R1207, R1208, R1209, R1210, R1211, R1212, R1213, R1214, R1215, R1216, R1217, R1218, R1219, R1220, R1221, R1222, R1223, R1224, R1225, R1226, R1227, R1228, R1229, R1230, R1231, R1232, R1233, R1234, R1235, R1236, R1237, R1238, R1239, R1240, R1241, R1242, R1243, R1244, R1245, R1246, R1247, R1248, R1249, R1250, R1251, R1252, R1253, R1254, R1255, R1256, R1257, R1258, R1259, R1260, R1261, R1262, R1263, R1264, R1265, R1266, R1267, R1268, R1269, R1270, R1271, R1272, R1273, R1274, R1275, R1276, R1277, R1278, R1279, R1280, R1281, R1282, R1283, R1284, R1285, R1286, R1287, R1288, R1289, R1290, R1291, R1292, R1293, R1294, R1295, R1296, R1297, R1298, R1299, R1300, R1301, R1302, R1303, R1304, R1305, R1306, R1307, R1308, R1309, R1310, R1311, R1312, R1313, R1314, R1315, R1316, R1317, R1318, R1319, R1320, R1321, R1322, R1323, R1324, R1325, R1326, R1327, R1328, R1329, R1330, R1331, R1332, R1333, R1334, R1335, R1336, R1337, R1338, R1339, R1340, R1341, R1342, R1343, R1344, R1345, R1346, R1347, R1348, R1349, R1350, R1351, R1352, R1353, R1354, R1355, R1356, R1357, R1358, R1359, R1360, R1361, R1362, R1363, R1364, R1365, R1366, R1367, R1368, R1369, R1370, R1371, R1372, R1373, R1374, R1375, R1376, R1377, R1378, R1379, R1380, R1381, R1382, R1383, R1384, R1385, R1386, R1387, R1388, R1389, R1390, R1391, R1392, R1393, R1394, R1395, R1396, R1397, R1398, R1399, R1400, R1401, R1402, R1403, R1404, R1405, R1406, R1407, R1408, R1409, R1410, R1411, R1412, R1413, R1414, R1415, R1416, R1417, R1418, R1419, R1420, R1421, R1422, R1423, R1424, R1425, R1426, R1427, R1428, R1429, R1430, R1431, R1432, R1433, R1434, R1435, R1436, R1437, R1438, R1439, R1440, R1441, R1442, R1443, R1444, R1445, R1446, R1447, R1448, R1449, R1450, R1451, R1452, R1453, R1454, R1455, R1456, R1457, R1458, R1459, R1460, R1461,





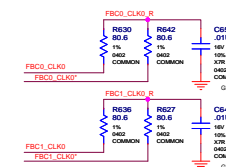
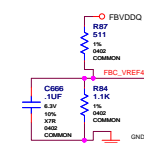
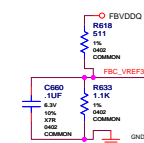
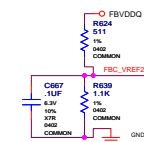
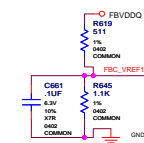
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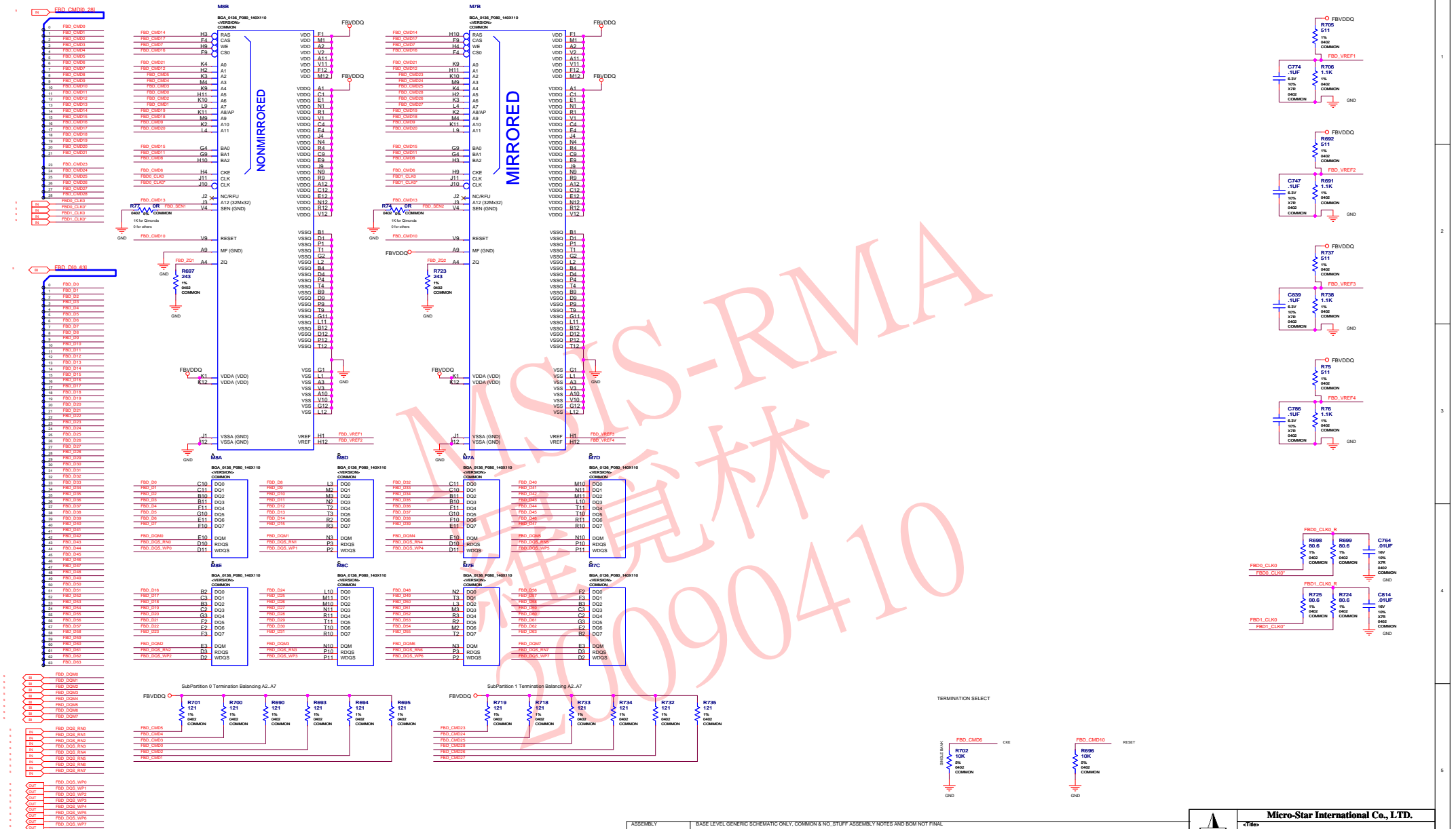
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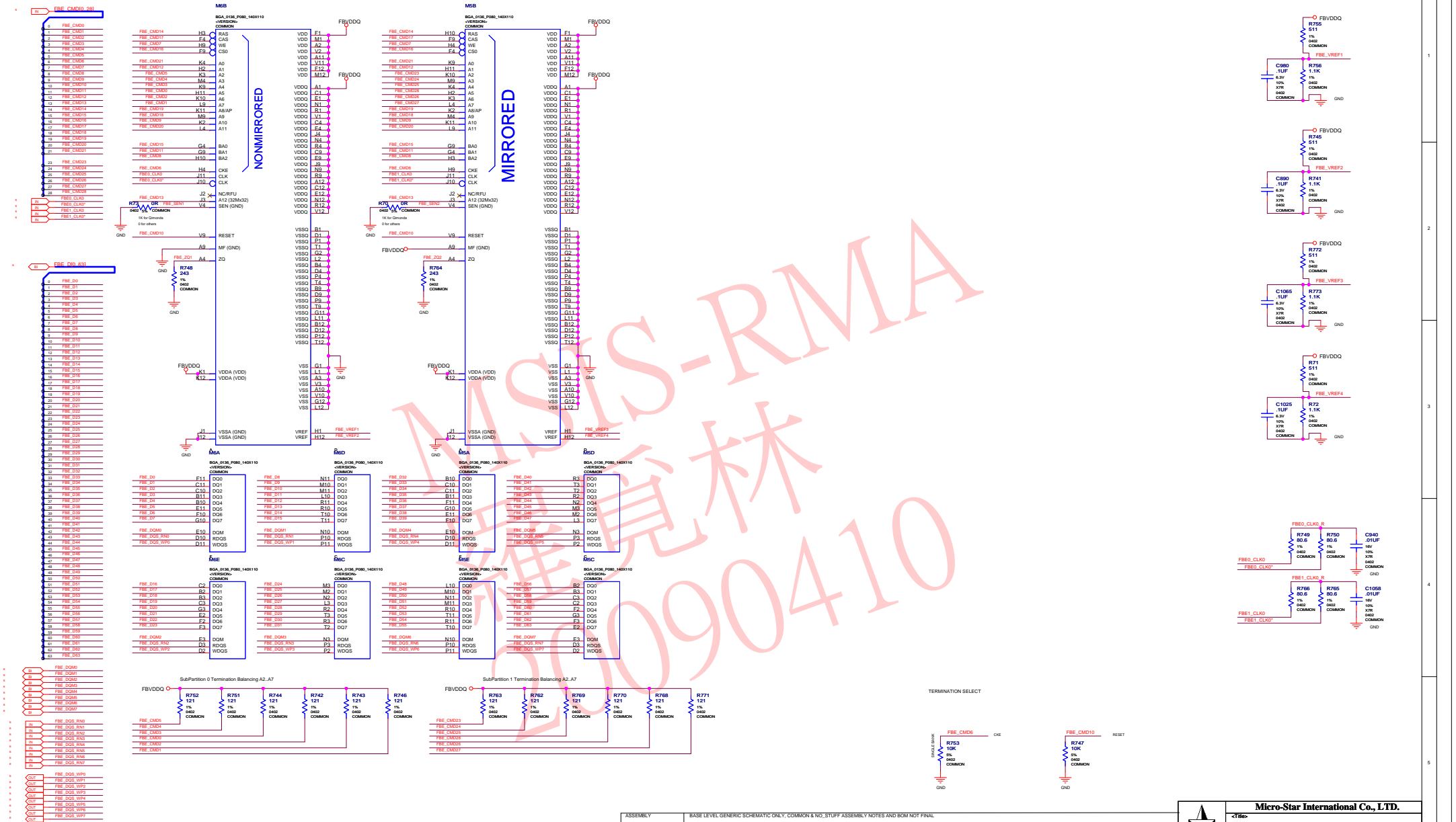
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Date: Wednesday, February 11, 2009 8 of 41			



# Framebuffer D: Memory Section



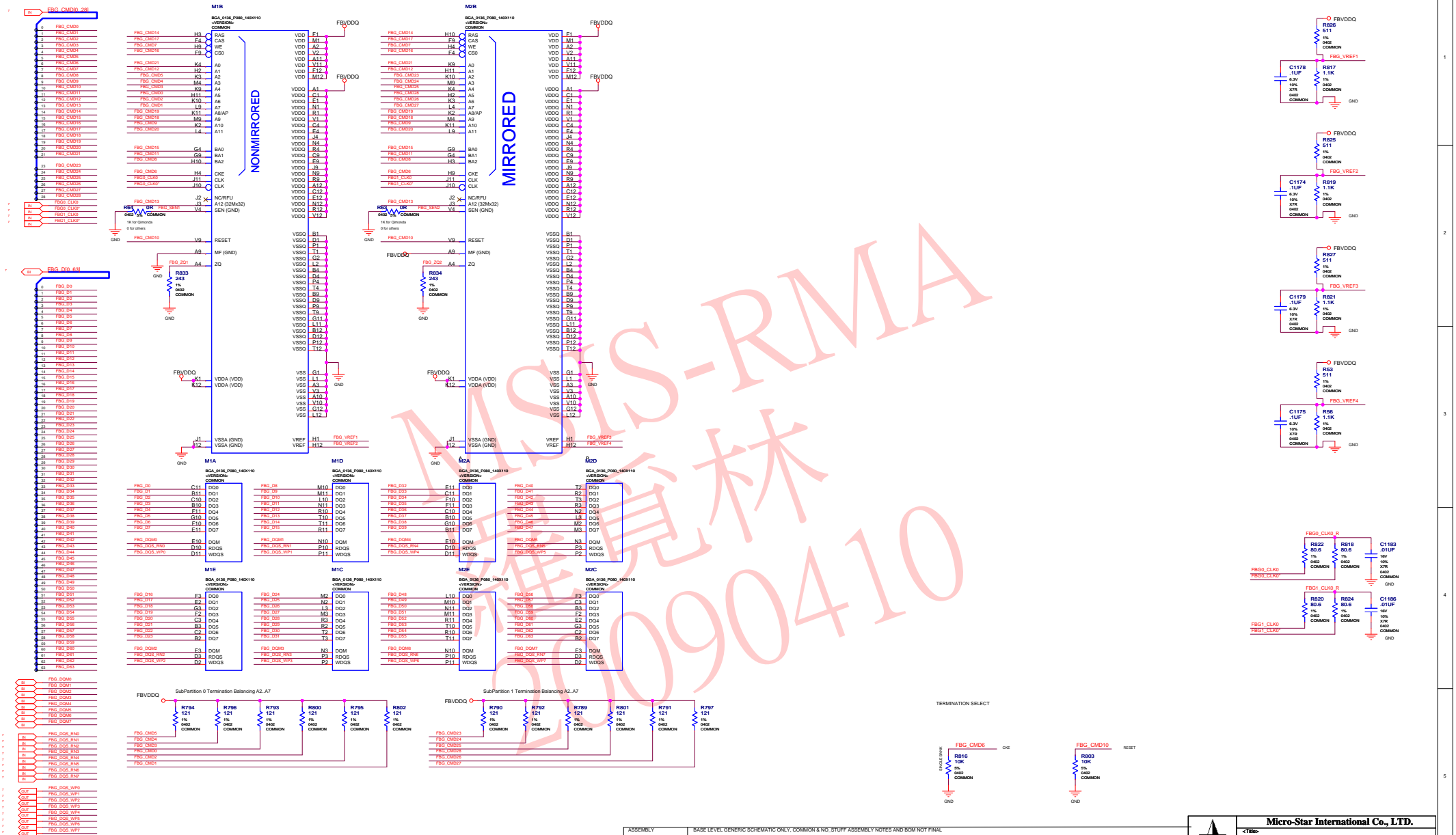
# Framebuffer E: Memory Section



```
IN FBF_CMD[0..28]
```



### Framebuffer G: Memory Section



☐ Cover ☐ Back Book Cover ☐ Endpapers  
☐ Title Page ☐ Table of Contents ☐ Index

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Framebuffer H: N/A

MSIS-RMA  
羅覓林  
20090410

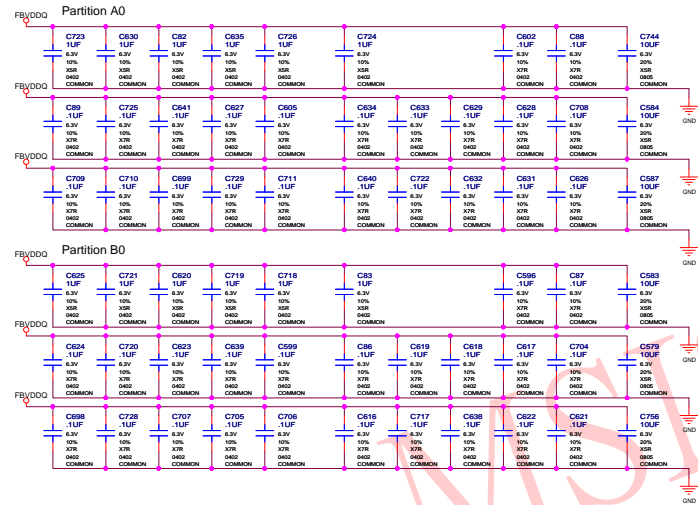
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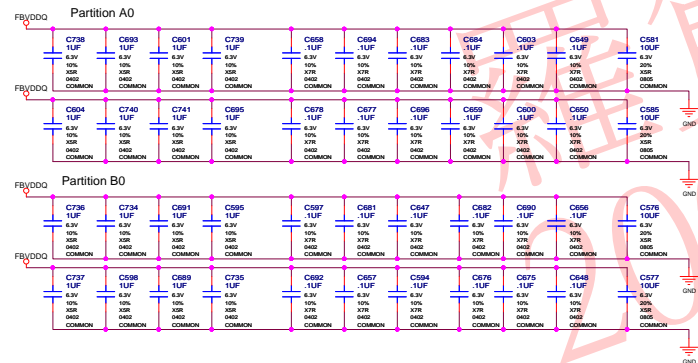
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	<Title>		
	Site	Document Number	Rev
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Date	Wednesday, February 11, 2009		Sheet 15 of 41

# Decoupling: Memory Section A-D

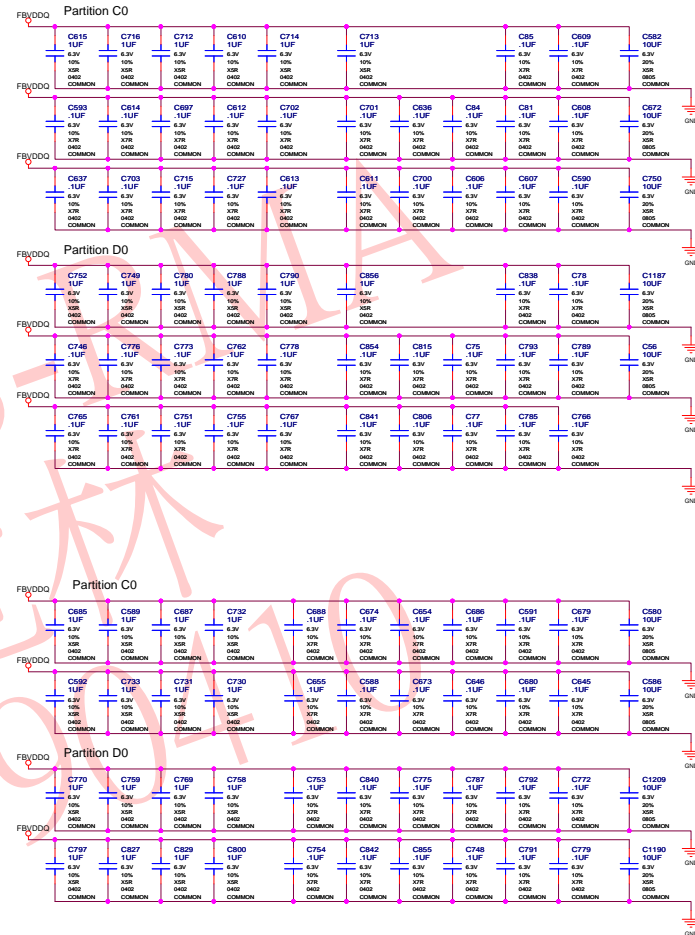
## Decoupling for FBVDDQ



## Decoupling for FBVDDQ



Banks A-D FBVDDQ  
Combined Distributed Capacitance  
280 uF



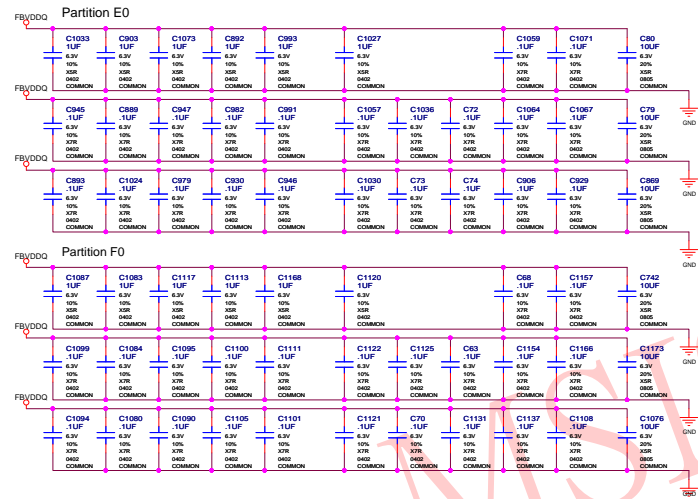
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PAGE DETAIL

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Decoupling Memory Section A-D

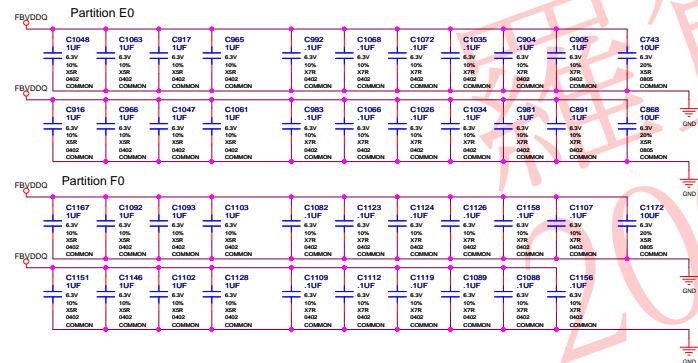
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Date	Wednesday, February 11, 2009
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# Decoupling: Memory Section E-G

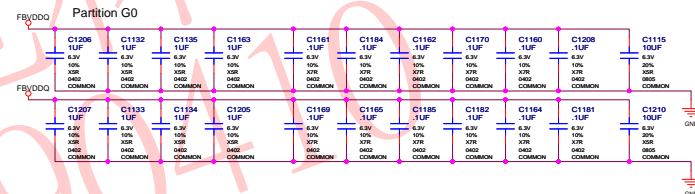
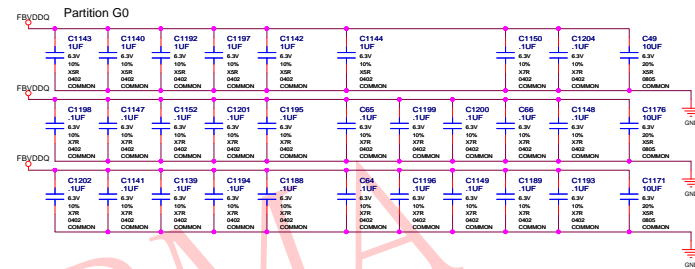
## Decoupling for FBVDDQ



## Decoupling for FBVDDQ



Banks E-G FBVDDQ  
Combined Distributed Capacitance  
210 uF



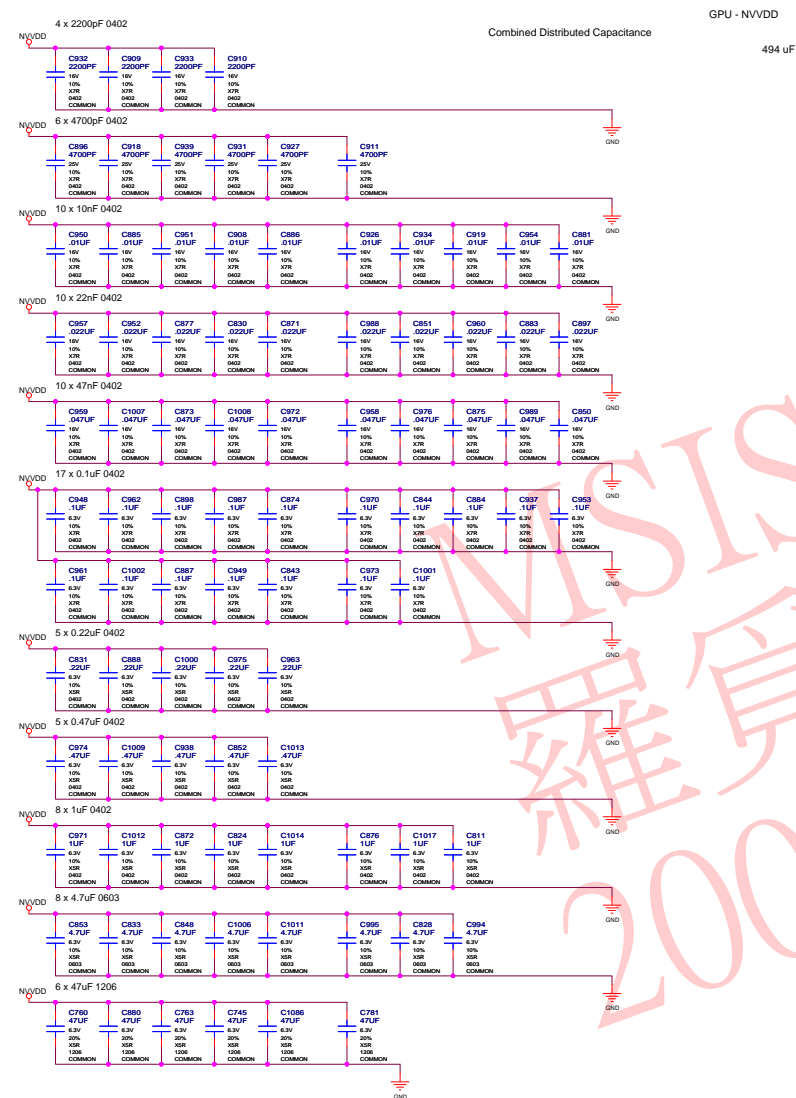
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Decoupling Memory Section E-G

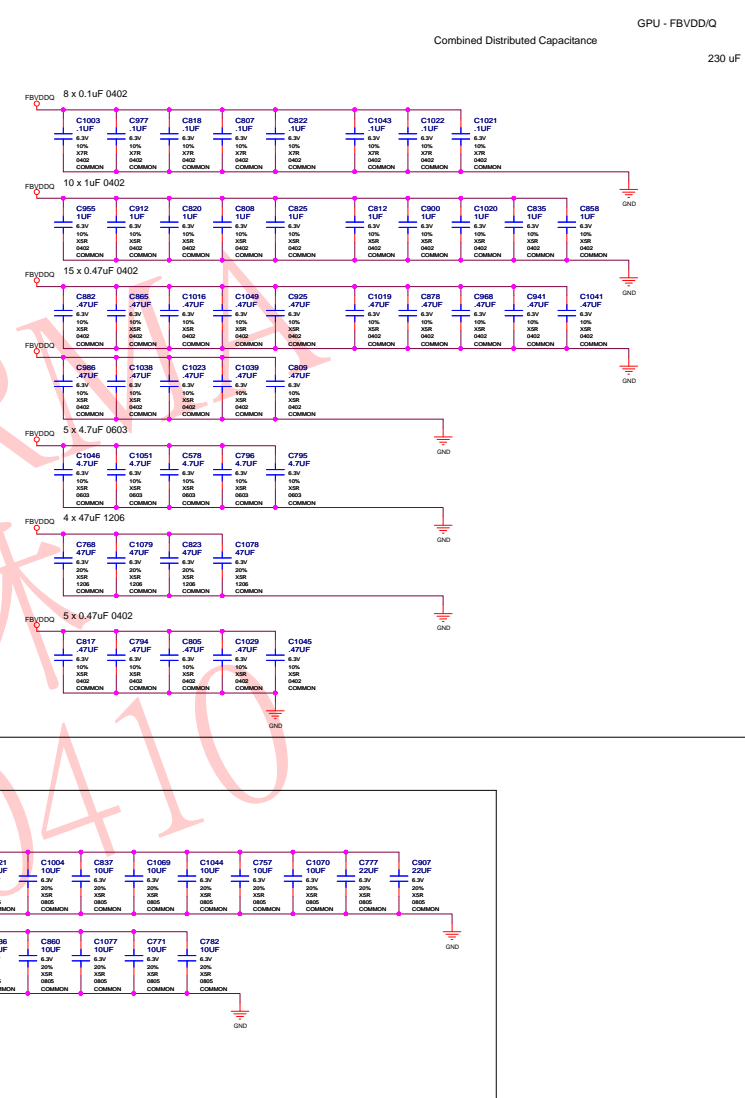
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# Decoupling: GPU (NVVDD, FBVDDQ)

## Decoupling for NVVDD (under GPU)



## Decoupling for FBVDDQ (under GPU)



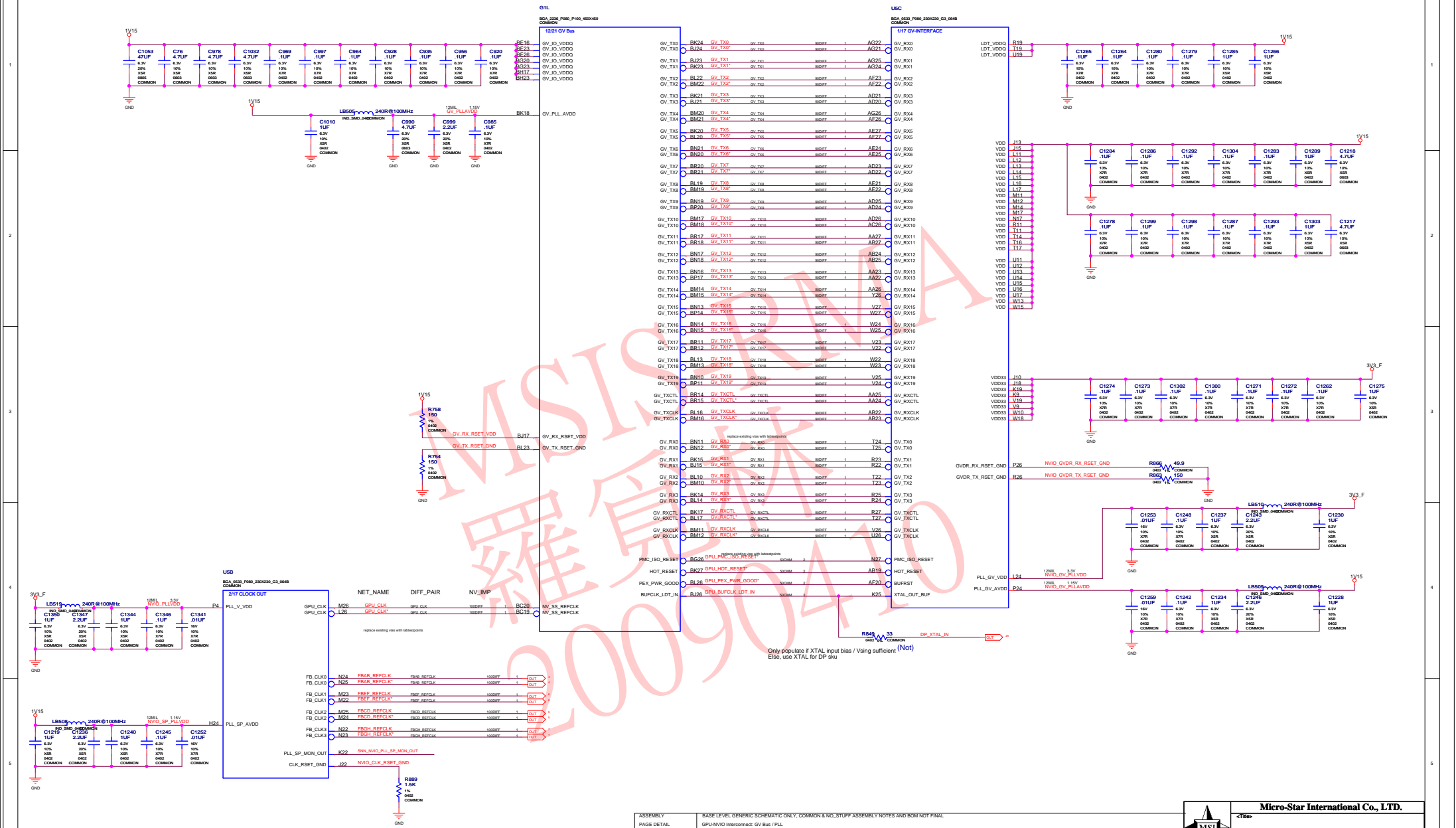
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PAGE DETAIL

DATE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL  
Decoupling GPU (NVVDD, FBVDDQ)

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Date: Wednesday, February 11, 2009	
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## GPU-NVIO Interconnect: GV Bus / PLL



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PAGE DETAIL	GPU-NVIO Interconnect: GV Bus / PLL



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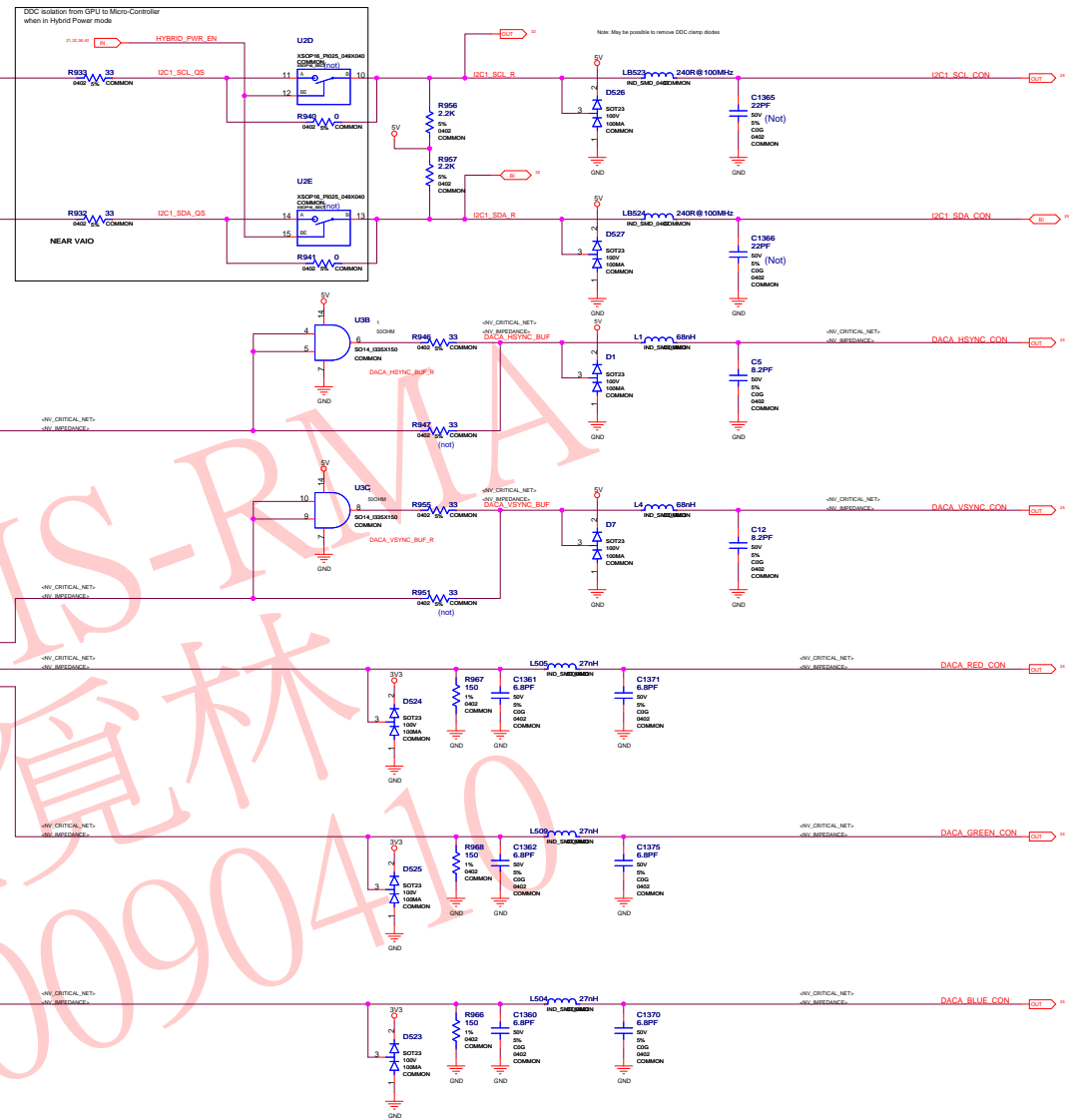
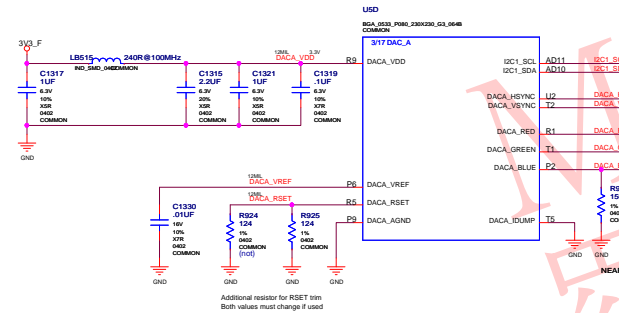
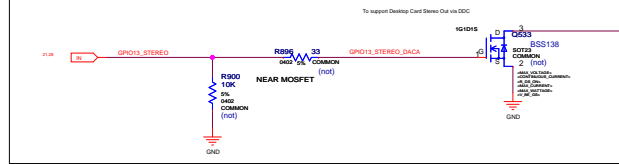
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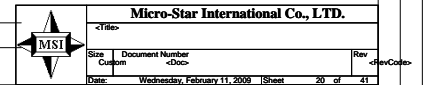
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[illegible]

Display: DACA (Middle DVI-I)



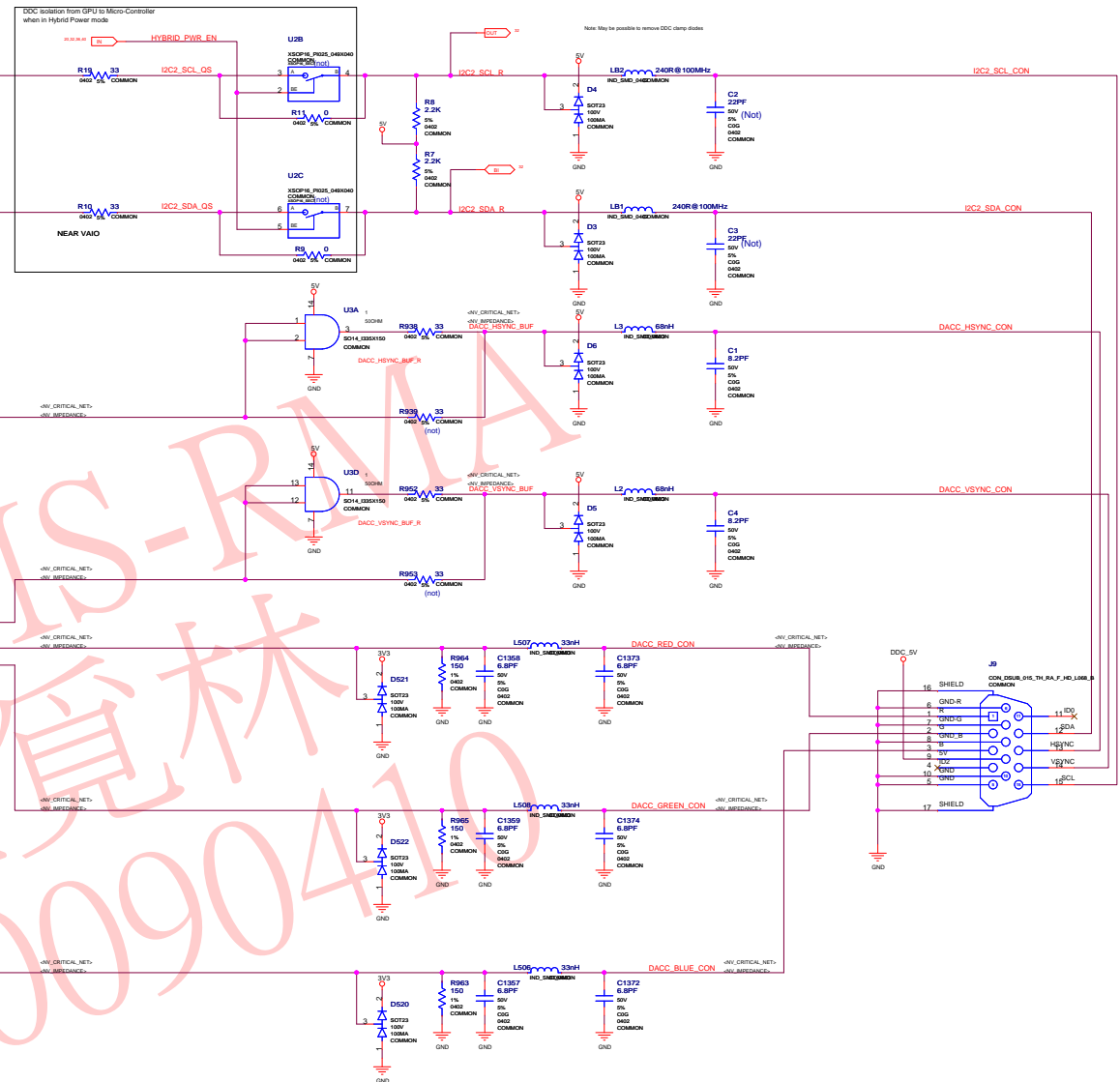
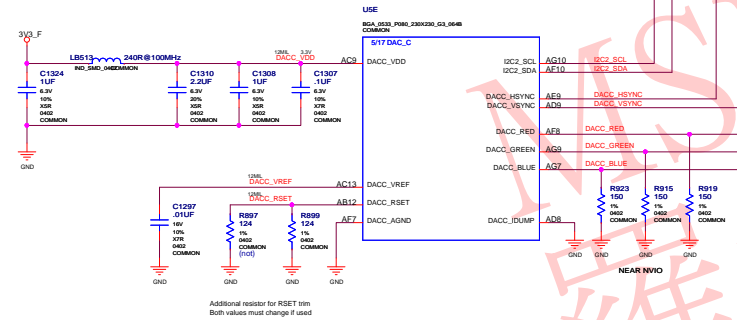
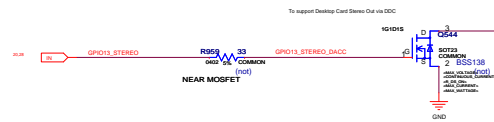
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PAGE DETAIL	Display: DACA (Middle DVI-I)



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Display: DACC (South DVI-I)



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PAGE DETAIL	Display: DACC (South DVI-I)



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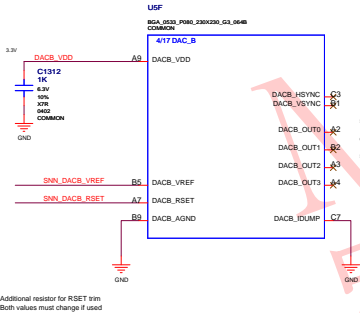
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Display: DACB (North MiniDIN) SD/HDTV out

11/21 remove TV

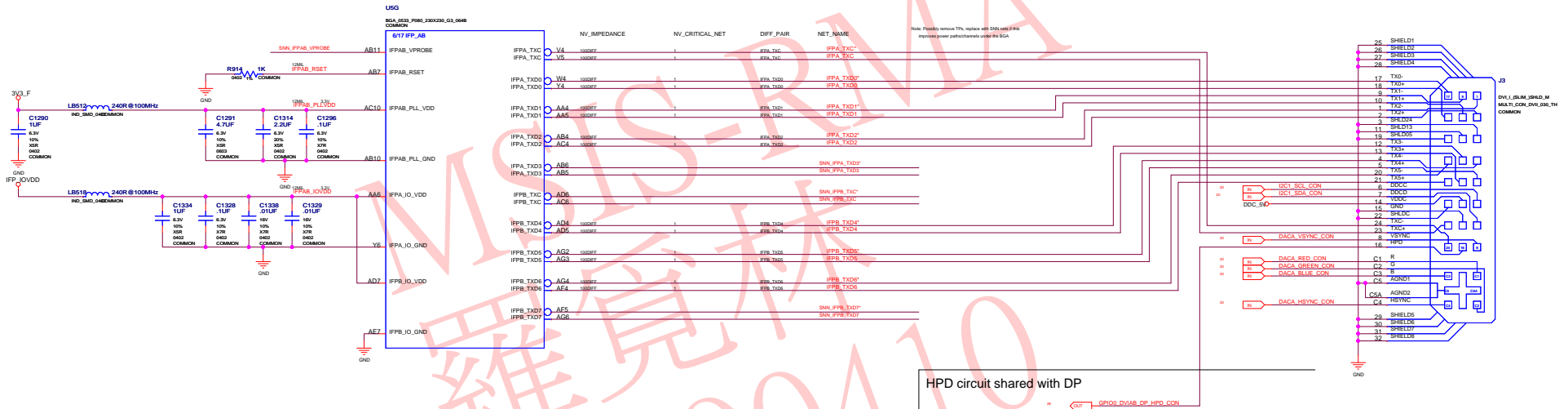


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Display: IFPAB for South DVI-I (with DACC)



HPD circuit shared with DP

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: IFPAB for south DVI-I (with DACC)

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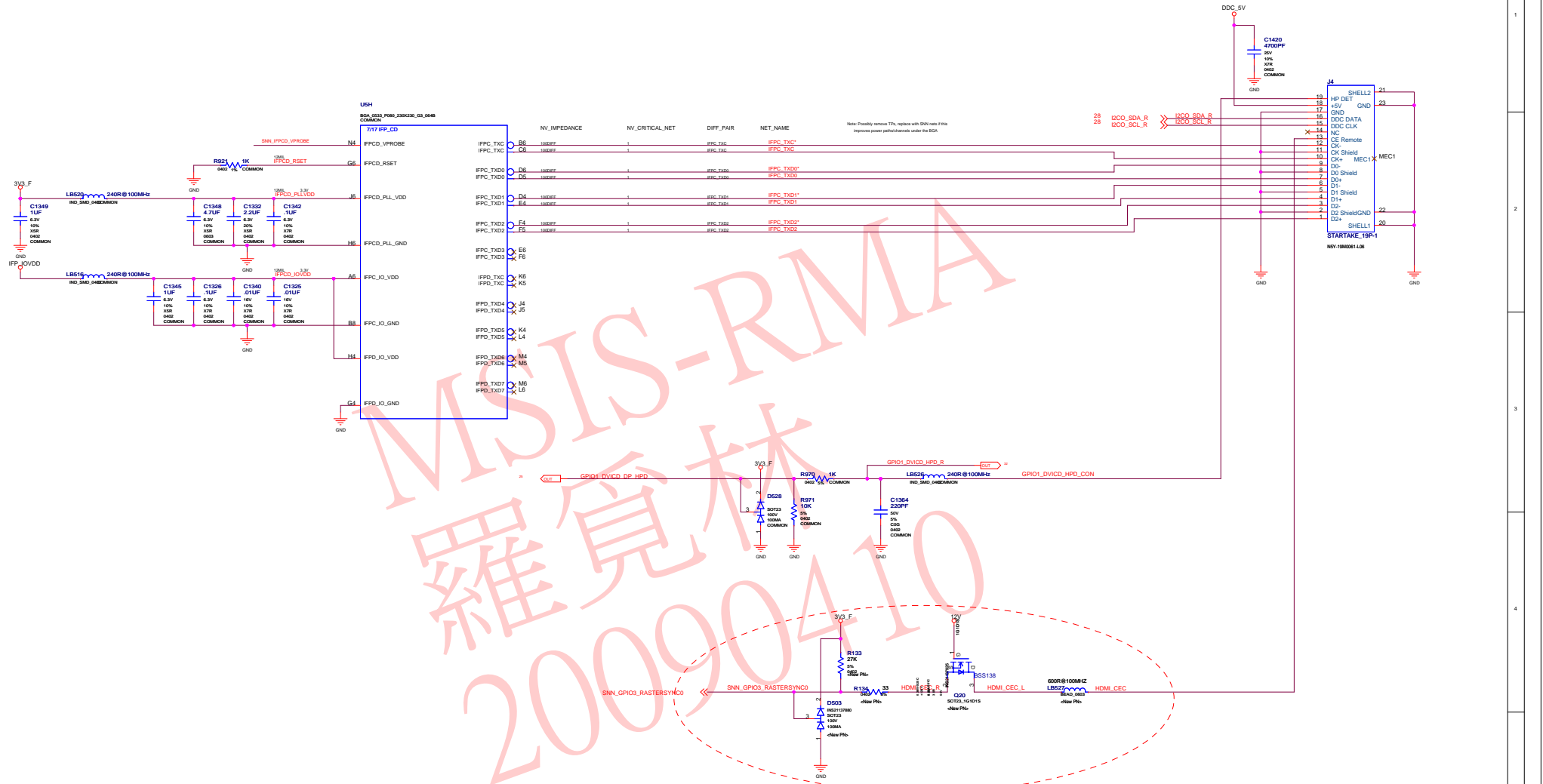
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Display: IFPCD for middle DVI-I (with DACA)



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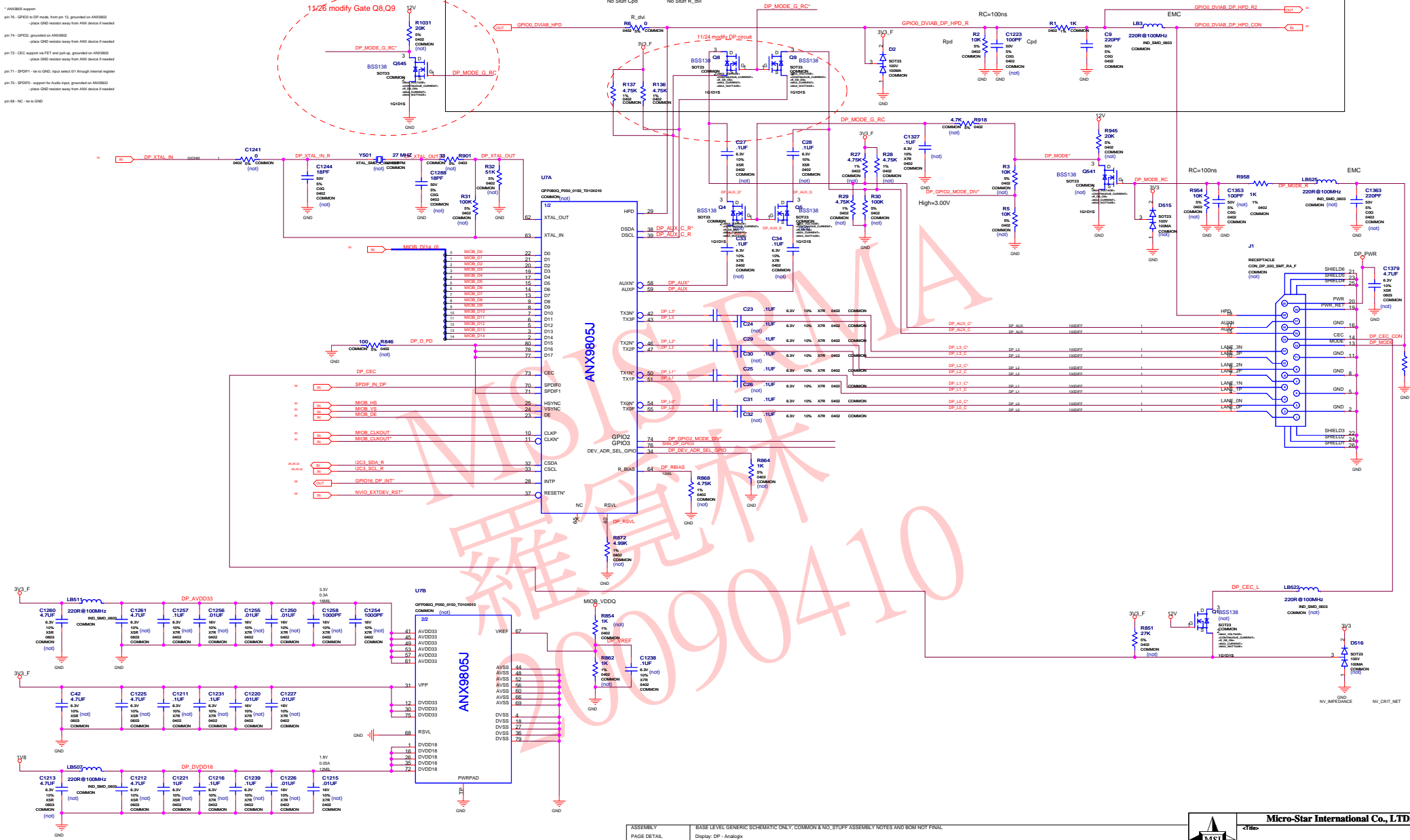
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Display: DP - Analogix

- \* AN0805 support
- pin 76 - GPIO3 to DP mode, from pin 13, grounded on AN0802
  - place GND resistor away from ANK device if needed
- pin 74 - GPIO2, grounded on AN0802
  - place GND resistor away from ANK device if needed
- pin 73 - CEC support via FET and pull-up, grounded on AN0802
  - place GND resistor away from ANK device if needed
- pin 71 - SPDIF1 - I<sub>2</sub>S to GND, input select 01 through internal registers
- pin 70 - SPDIF2 - support for Audio input, grounded on AN0802
  - place GND resistor away from ANK device if needed
- pin 68 - NC - tie to GND



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: DP - Analogix



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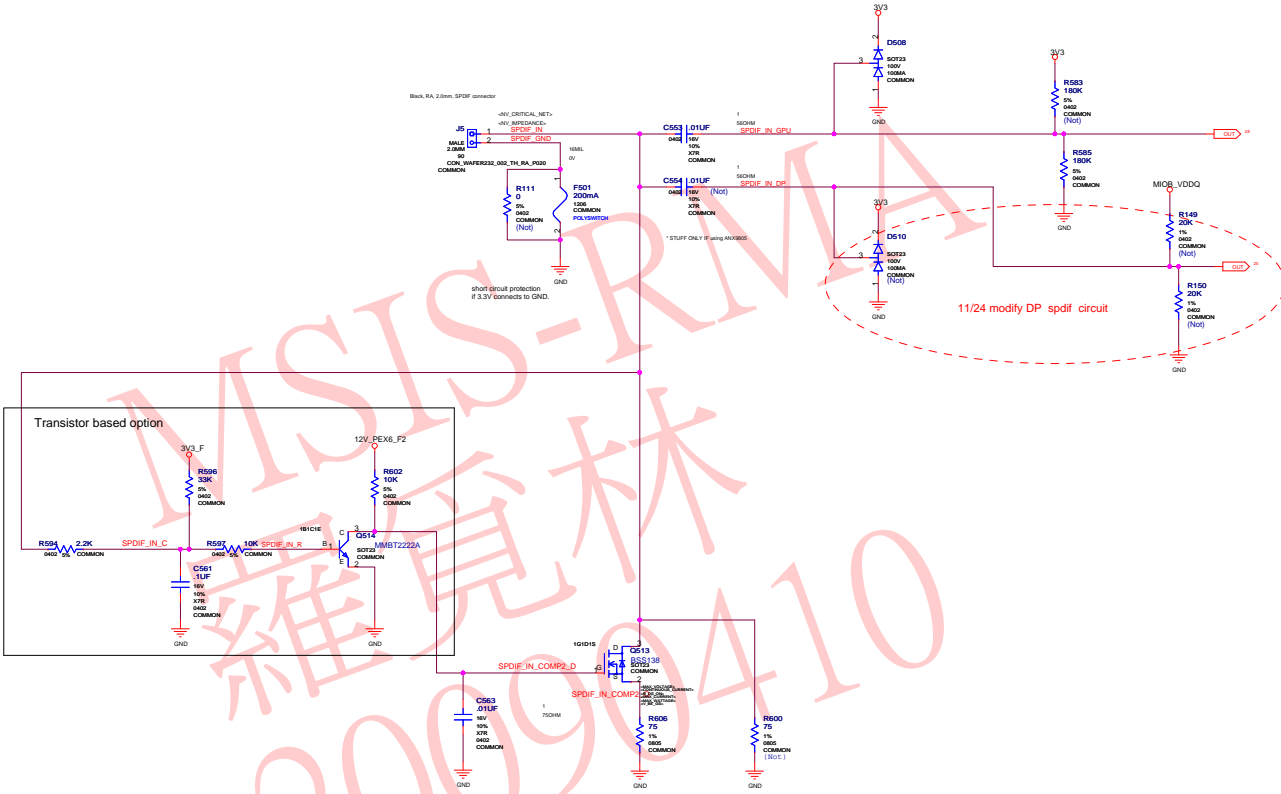
Date: Wednesday, Feb 22, 2012 11:51 AM

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Connectors: SPDIF

SPDIF INPUT / Level Detection



### Transistor based option

11/24 modify DP spdif circuit

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Connectors: SPDIF

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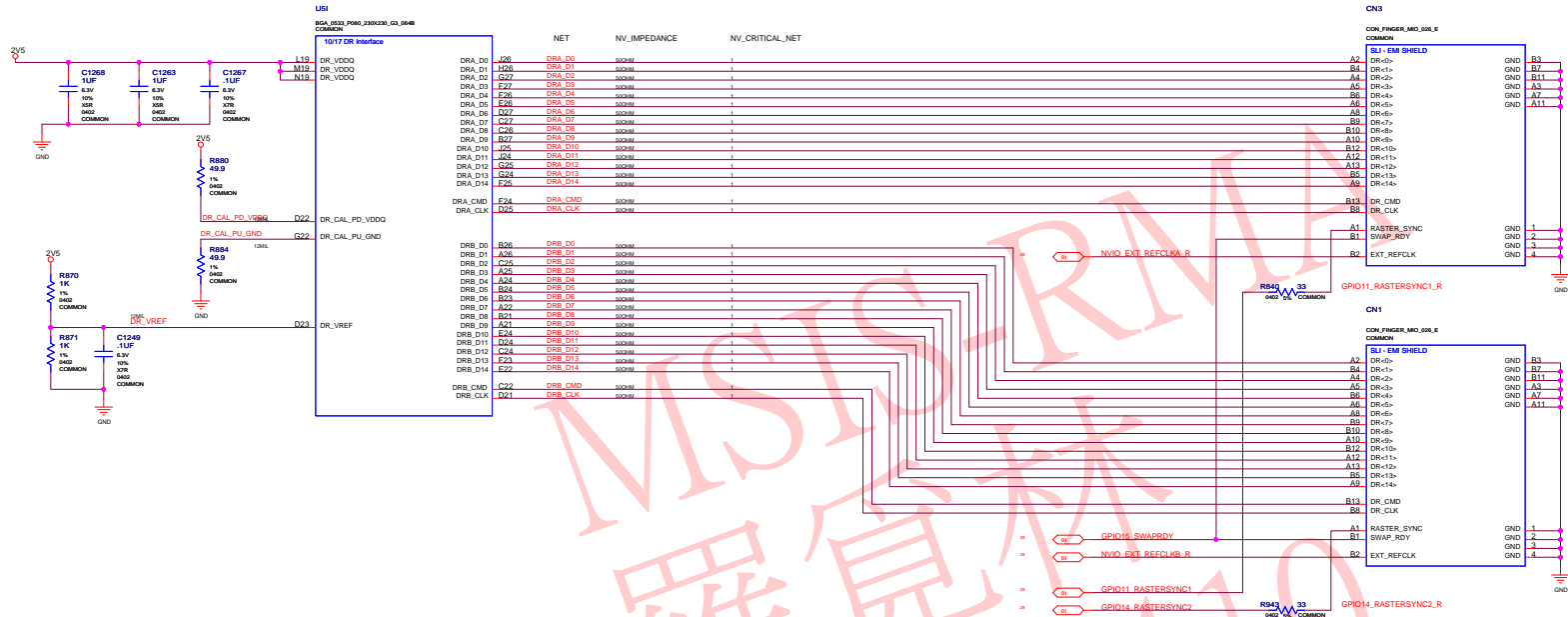
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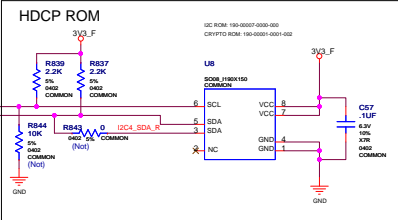
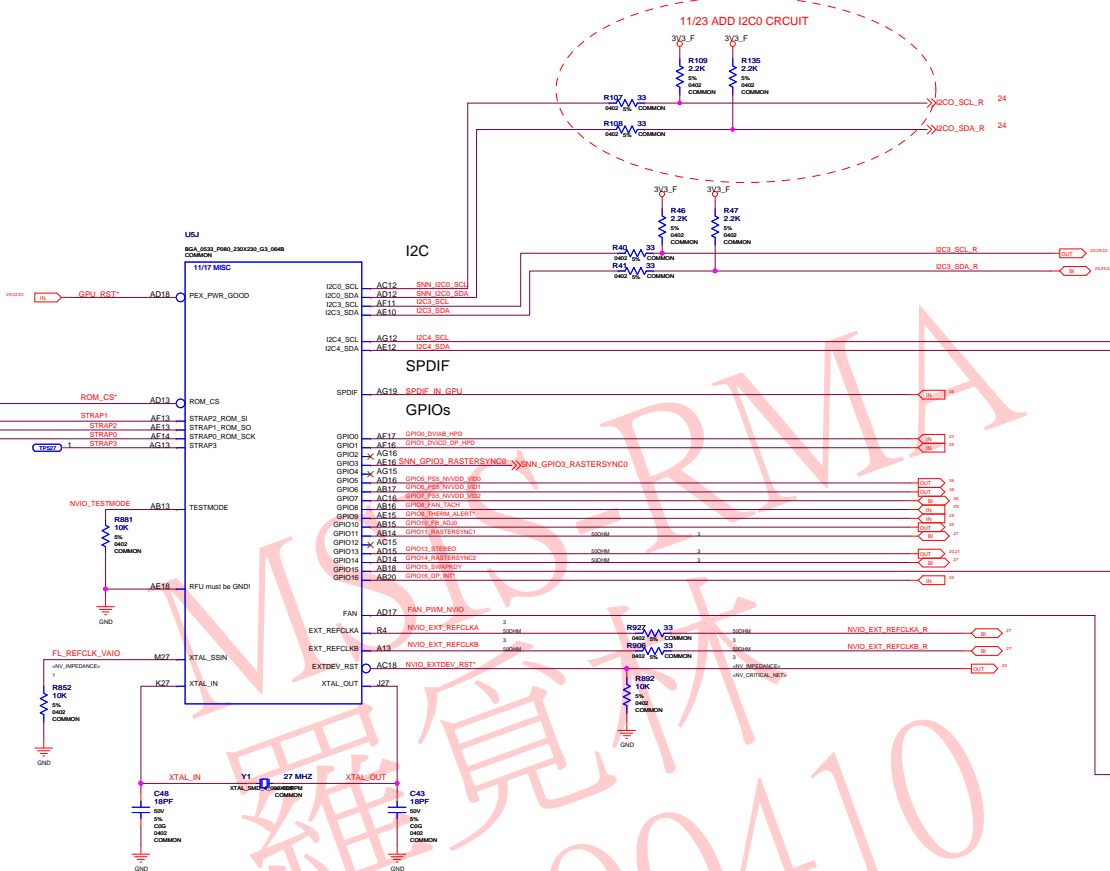
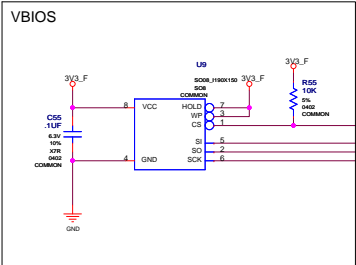
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Connectors: DR Interface (Dual SLI)



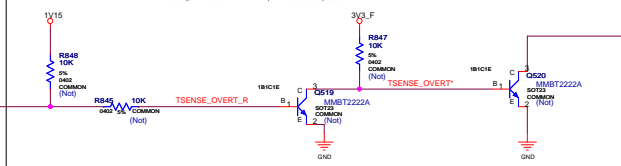
## MISC: GPIO / XTAL / VBIOS / HDCP / I2C



# MISC: FAN / THERM

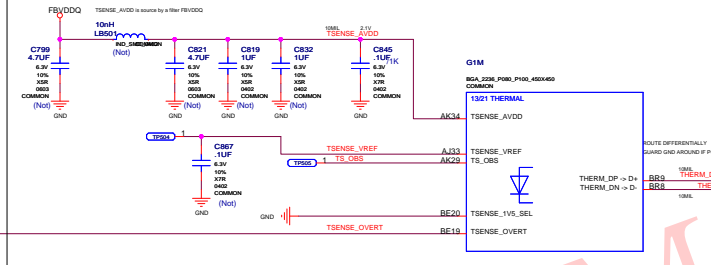
## TSENSE\_OVERT Level Shifter (1.15V to 3.3V)

TSENSE\_OVERT is the THERMAL\_ALERT pin for the Internal Temp Sensor



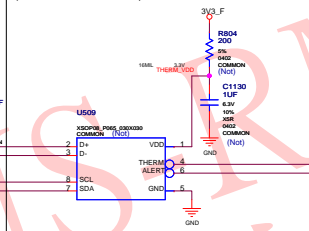
## Internal GPU Thermal Sensor

### Default Thermal Controller



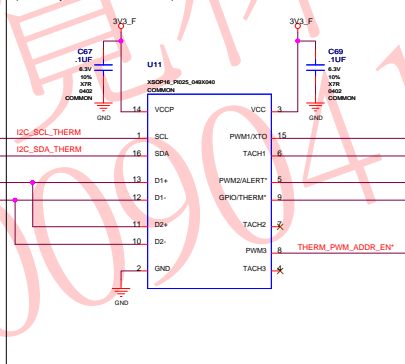
Notes: 1.45 and 1.75 V<sub>DD</sub> is 1.75 V<sub>DD</sub> (internal) to 1.75 V<sub>DD</sub> (internal)  
Notes: 1.45 and 1.75 V<sub>DD</sub> is 1.75 V<sub>DD</sub> (internal) to 1.75 V<sub>DD</sub> (internal)

## LM99/MAX6649 (Alternate Thermal Controller)

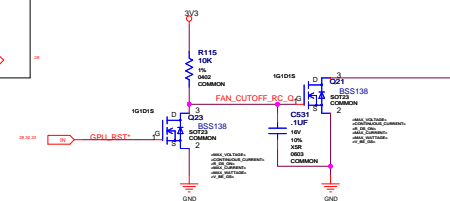


Note: POR internal thermal control external controls will be DNI

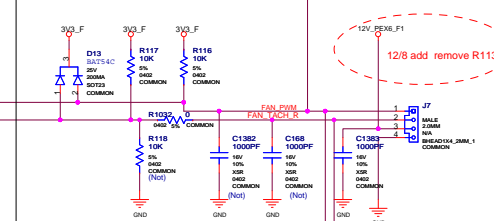
## ADT7473 (Secondary thermal controller choice)



## FAN Connector



## FAN Connector

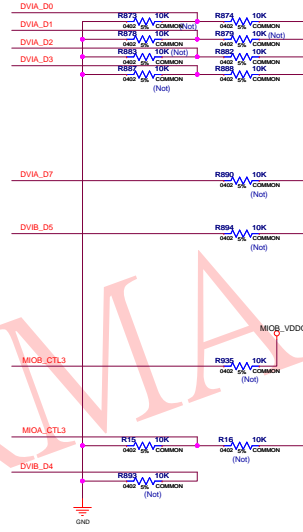
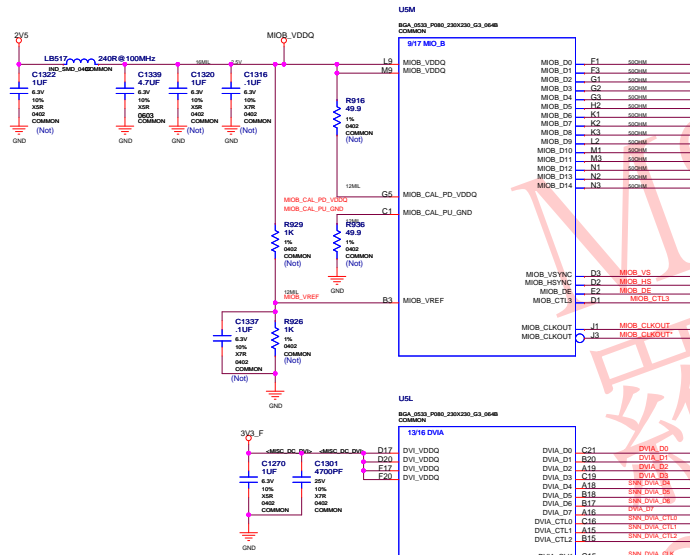
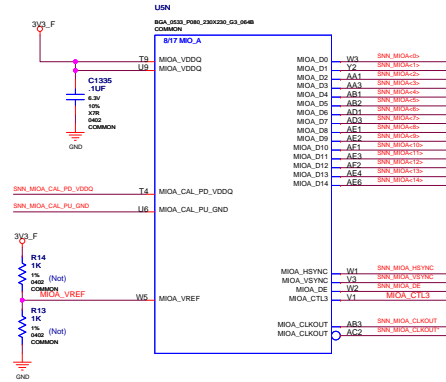


## GPU Driven Fan and Tach



ASSEMBLY  
PAGE DETAIL  
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MISC: FAN / THERM

MISC: MIO / DVI / STRAPS

STRAP BITS BOOT0 = 0x101000

NR.	USAGE	COMMENT
00	GV_WIDTH	DEFAULT=0x0 (WIDE)
01	SUB_VENDOR	DEFAULT=0x1 (FROM BIOS)
02	RAM_CFG[0]	
03	RAM_CFG[1]	
04	RAM_CFG[2]	
05	RAM_CFG[3]	
06	CRYSTAL	DEFAULT=0x0 (72MHz)
07	TV_MODE[0]	DEFAULT=0x1 (NTSC_J)
08	TV_MODE[1]	
09	TV_MODE[2]	
10	PCI_DEV[0]	SET BY BIOS
11	PCI_DEV[1]	
12	PCI_DEV[2]	
13	PCI_DEV[3]	DEFAULT=0x0
14	FB_SIZE[0]	DEFAULT=0x2 (256MB ??)
15	FB_SIZE[1]	
16	FB_SIZE[2]	
17	PEX_FLN_TERM100	DEFAULT=0x0 (ENABLED)
18	3GPO_CFG_PDO_LUT_ADR[0]	DEFAULT=0x3 (DESKTOP_DEFAULT)
19	3GPO_CFG_PDO_LUT_ADR[1]	
20	3GPO_CFG_PDO_LUT_ADR[2]	
21	3GPO_CFG_PDO_LUT_ADR[3]	
22	ROMTYP[0]	DEFAULT=0x1 (AT255)
23	ROMTYP[1]	
24	USER[0]	SET BY BIOS
25	USER[1]	
26	USER[2]	
27	USER[3]	
28	PCI_DEVID_EXT	DEFAULT=0x0

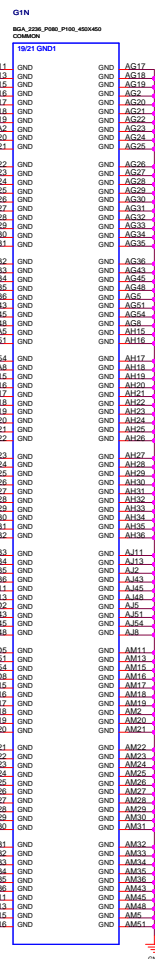
STRAP BITS BOOT3 = 0x10100C

```
NR_USAGE_____COMMENT_____
06 : XCLK_555          DEFAULT=0x0

16 : PCLJOBAR          DEFAULT=0x1
                        0=DISABLE 1=ENABLE
```

CFG	Config Width	Vendor
0000	Reserved	
0001	1600x32 512-bit Qimonda	
0010	1600x32 512-bit Hynix	
0011	1600x32 512-bit Samsung	
0100	Reserved	
0101	320x32 512-bit Qimonda	
0110	320x32 512-bit Hynix	
0111	320x32 512-bit Samsung	
1000	Reserved	
1001	1600x32 448-bit Qimonda	
1010	1600x32 448-bit Hynix	
1011	1600x32 448-bit Samsung	
1100	Reserved	
1101	320x32 448-bit Qimonda	
1110	320x32 448-bit Hynix	
1111	320x32 448-bit Samsung	

## GPU SECTION GND

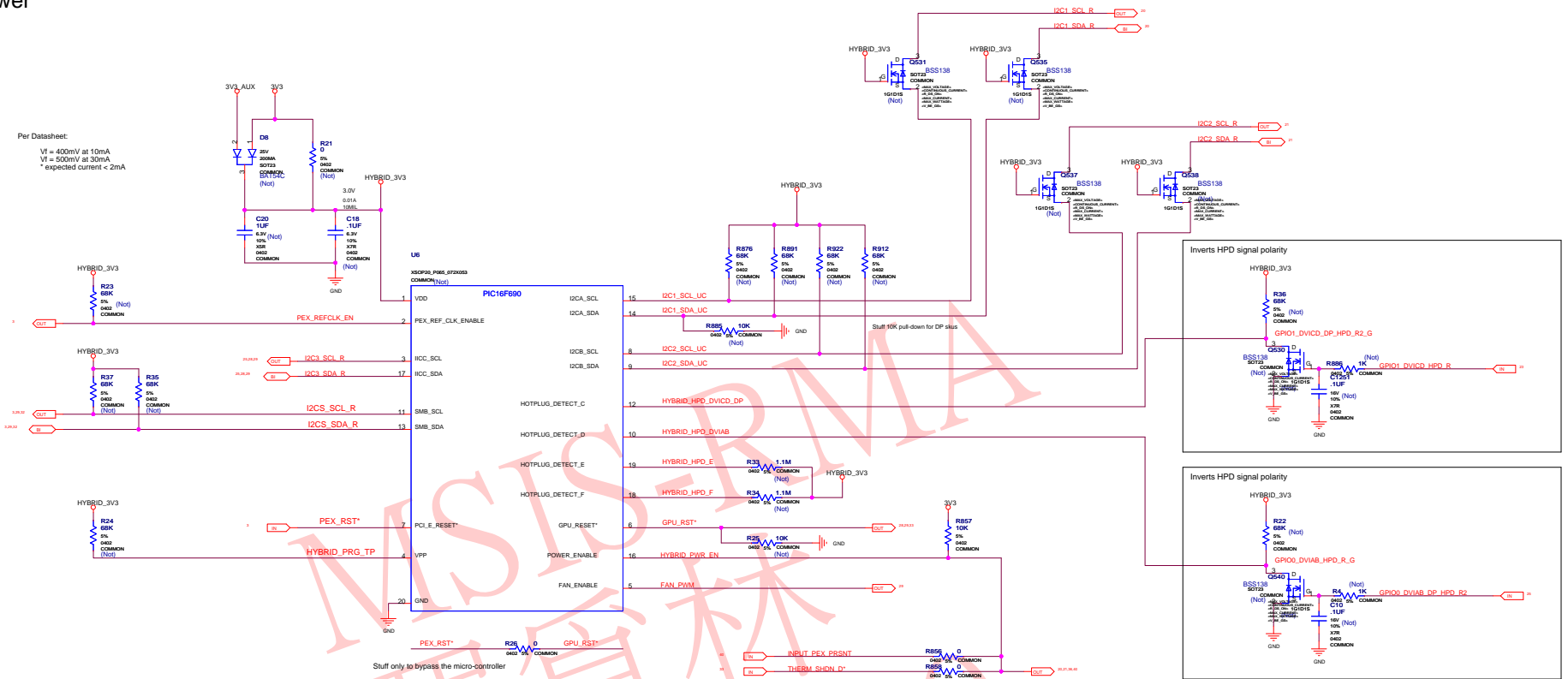
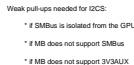
[illegible]

G1S		G2A_2226_P06B_P160_4501605 COMMON		G1T		G2A_2226_P06B_P160_4501605 COMMON	
1121 FBVDC0NFU				1621 SPARE0EMC			
013. FBVDC0	FBA, RFU0	B038	DNM FBA 0000	DNM SPARE 01	B050	SPARE	NO
042. FBVDC0	FBA, RFU0	B044	DNM FBA 0001	DNM SPARE 02	B056	SPARE	NO
013. FBVDC0	FBA, RFU0	B046	DNM FBA 0002	DNM SPARE 03	B063	SPARE	NO
042. FBVDC0	FBA, RFU0	B048	DNM FBA 0003	DNM SPARE 04	B069	SPARE	NO
043. FBVDC0	FBA, RFU0	B051	DNM FBA 0004	DNM SPARE 05	B074	SPARE	NO
013. FBVDC0	FBA, RFU0	B054	DNM FBA 0005	DNM SPARE 06	B081	SPARE	NO
043. FBVDC0	FBA, RFU0	B056	DNM FBA 0006	DNM SPARE 07	B087	SPARE	NO
013. FBVDC0	FBA, RFU0	B059	DNM FBA 0007	DNM SPARE 08	B094	SPARE	NO
043. FBVDC0	FBA, RFU0	B061	DNM FBA 0008	DNM SPARE 09	B101	SPARE	NO
013. FBVDC0	FBA, RFU0	B064	DNM FBA 0009	DNM SPARE 10	B107	SPARE	NO
043. FBVDC0	FBA, RFU0	B067	DNM FBA 0010	DNM SPARE 11	B114	SPARE	NO
013. FBVDC0	FBA, RFU0	B070	DNM FBA 0011	DNM SPARE 12	B121	SPARE	NO
043. FBVDC0	FBA, RFU0	B073	DNM FBA 0012	DNM SPARE 13	B128	SPARE	NO
013. FBVDC0	FBA, RFU0	B076	DNM FBA 0013	DNM SPARE 14	B135	SPARE	NO
043. FBVDC0	FBA, RFU0	B079	DNM FBA 0014	DNM SPARE 15	B142	SPARE	NO
013. FBVDC0	FBA, RFU0	B082	DNM FBA 0015	DNM SPARE 16	B149	SPARE	NO
043. FBVDC0	FBA, RFU0	B085	DNM FBA 0016	DNM SPARE 17	B156	SPARE	NO
013. FBVDC0	FBA, RFU0	B088	DNM FBA 0017	DNM SPARE 18	B163	SPARE	NO
043. FBVDC0	FBA, RFU0	B091	DNM FBA 0018	DNM SPARE 19	B170	SPARE	NO
013. FBVDC0	FBA, RFU0	B094	DNM FBA 0019	DNM SPARE 20	B177	SPARE	NO
043. FBVDC0	FBA, RFU0	B097	DNM FBA 0020	DNM SPARE 21	B184	SPARE	NO
013. FBVDC0	FBA, RFU0	B100	DNM FBA 0021	DNM SPARE 22	B191	SPARE	NO
043. FBVDC0	FBA, RFU0	B103	DNM FBA 0022	DNM SPARE 23	B198	SPARE	NO
013. FBVDC0	FBA, RFU0	B106	DNM FBA 0023	DNM SPARE 24	B205	SPARE	NO
043. FBVDC0	FBA, RFU0	B109	DNM FBA 0024	DNM SPARE 25	B212	SPARE	NO
013. FBVDC0	FBA, RFU0	B112	DNM FBA 0025	DNM SPARE 26	B219	SPARE	NO
043. FBVDC0	FBA, RFU0	B115	DNM FBA 0026	DNM SPARE 27	B226	SPARE	NO
013. FBVDC0	FBA, RFU0	B118	DNM FBA 0027	DNM SPARE 28	B233	SPARE	NO
043. FBVDC0	FBA, RFU0	B121	DNM FBA 0028	DNM SPARE 29	B240	SPARE	NO
013. FBVDC0	FBA, RFU0	B124	DNM FBA 0029	DNM SPARE 30	B247	SPARE	NO
043. FBVDC0	FBA, RFU0	B127	DNM FBA 0030	DNM SPARE 31	B254	SPARE	NO
013. FBVDC0	FBA, RFU0	B130	DNM FBA 0031	DNM SPARE 32	B261	SPARE	NO
043. FBVDC0	FBA, RFU0	B133	DNM FBA 0032	DNM SPARE 33	B268	SPARE	NO
013. FBVDC0	FBA, RFU0	B136	DNM FBA 0033	DNM SPARE 34	B275	SPARE	NO
043. FBVDC0	FBA, RFU0	B139	DNM FBA 0034	DNM SPARE 35	B282	SPARE	NO
013. FBVDC0	FBA, RFU0	B142	DNM FBA 0035	DNM SPARE 36	B289	SPARE	NO
043. FBVDC0	FBA, RFU0	B145	DNM FBA 0036	DNM SPARE 37	B296	SPARE	NO
013. FBVDC0	FBA, RFU0	B148	DNM FBA 0037	DNM SPARE 38	B303	SPARE	NO
043. FBVDC0	FBA, RFU0	B151	DNM FBA 0038	DNM SPARE 39	B310	SPARE	NO
013. FBVDC0	FBA, RFU0	B154	DNM FBA 0039	DNM SPARE 40	B317	SPARE	NO
043. FBVDC0	FBA, RFU0	B157	DNM FBA 0040	DNM SPARE 41	B324	SPARE	NO
013. FBVDC0	FBA, RFU0	B160	DNM FBA 0041	DNM SPARE 42	B331	SPARE	NO
043. FBVDC0	FBA, RFU0	B163	DNM FBA 0042	DNM SPARE 43	B338	SPARE	NO
013. FBVDC0	FBA, RFU0	B166	DNM FBA 0043	DNM SPARE 44	B345	SPARE	NO
043. FBVDC0	FBA, RFU0	B169	DNM FBA 0044	DNM SPARE 45	B352	SPARE	NO
013. FBVDC0	FBA, RFU0	B1					

**USP**

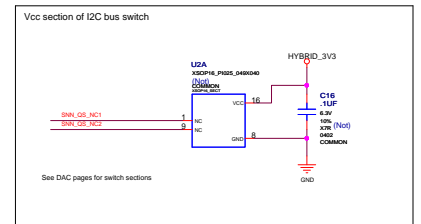
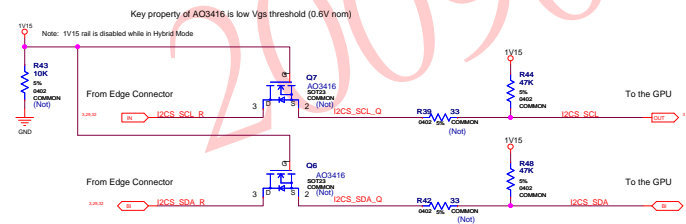
BCA\_0521\_P960\_2303262\_G1\_05-46  
COMMON

Power: Hybrid Power



## I2CS Isolation for Hybrid Power and Level Shifting(3.3V to 1.15V)

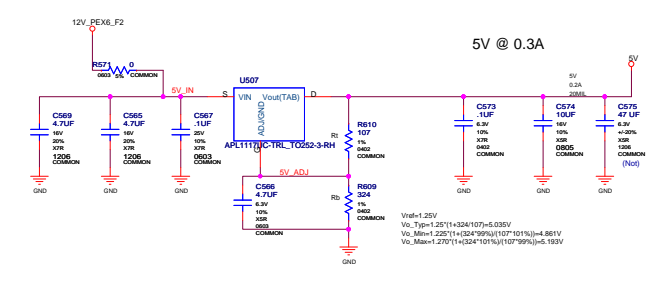
Isolates SMBus to the GPU when in Hybrid mode  
GT200 I2CS lanes are 1.2V tolerant signals



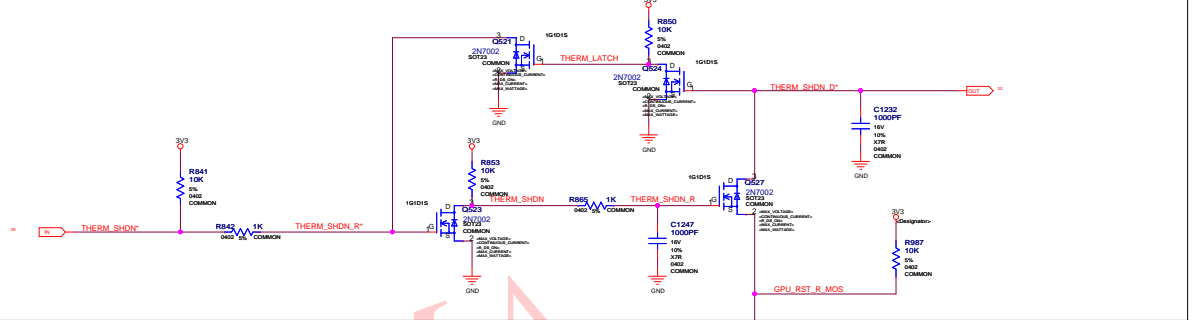


# Power Supply: 5V LDO / 3V3\_DP / THERM SHUTDOWN LATCH / IFP\_IOVDD / PEX\_PLVDD

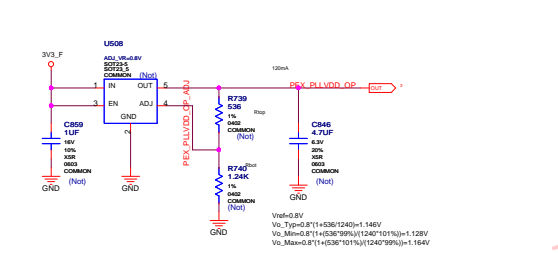
## 5V Linear



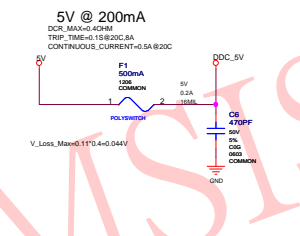
## THERM OVERT SHUTDOWN LATCH



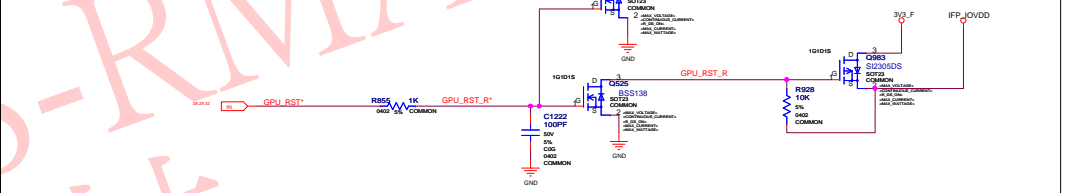
## PEX PLLVDD optional Supply



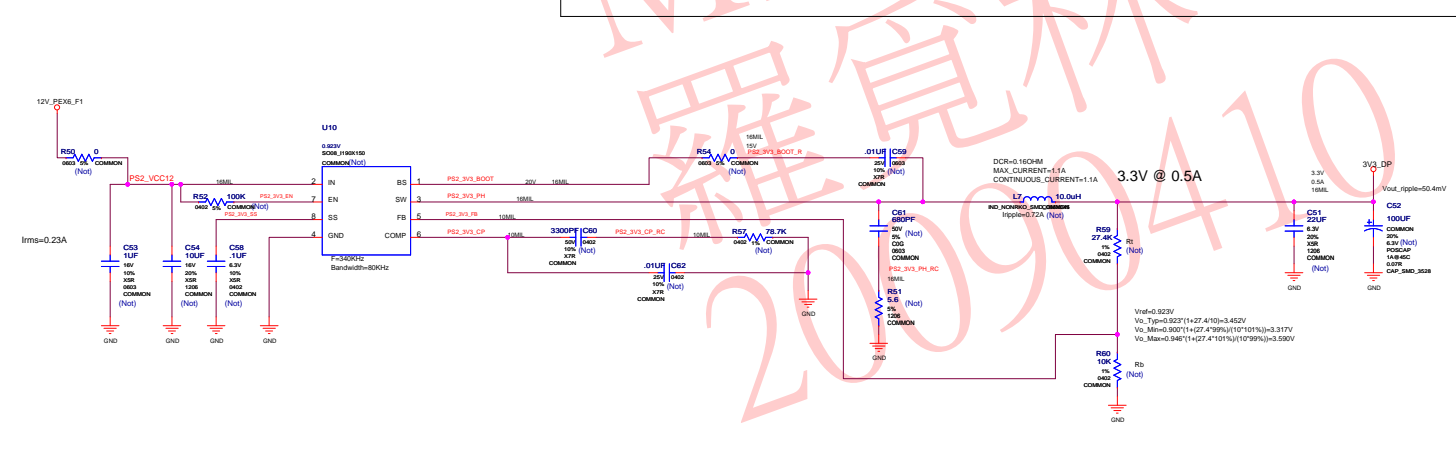
## DDC\_5V



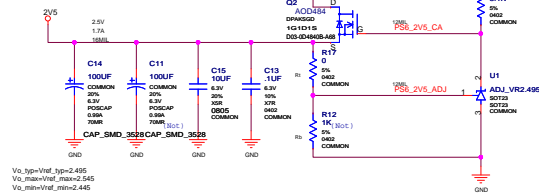
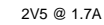
## IFP\_IOVDD (backdrive prevention)



## 3V3\_DP SWITCHER (Only required for DisplayPort SKU)

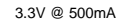


Power Supply: 2V5, DP\_PWR, 8V5 1V15 (PEX\_VDD, GV\_VDD)



Vo\_typ=Vref\_typ=2.495  
Vo\_max=Vref\_max=2.545  
Vo\_min=Vref\_min=2.445

## DP Dongle Supply



DCR\_MAX=10HM  
TRIP\_TIME=0.15S@20C,8A  
CONTINUOUS\_CURRENT=0.5A

8V5	11/21:remove 8V5 circuit
-----	--------------------------



$V_{ref}=0.8V$   
 $V_{o\_Typ}=0.8*(1+(1/0.806))=1.793V$   
 $V_{o\_Min}=0.784*(1+(1*99\%)/(0.806*101\%))=1.737V$   
 $V_{o\_Max}=0.816*(1+(1*101\%)/(0.806*99\%))=1.849V$

PEX\_VDD, GV  
1V15 @ 6A

PEX / GV 1V15

377 uF

112 uF

489 uF

# Power Supply: Combined FBVDD/Q

FVBDDQ ENABLE

NVDD\_PG000

NVDD\_PG000

NVDD\_PG000

NVDD\_PG000

NVDD\_PG000

NVDD\_PG000

NVDD\_PG000

NVDD\_PG000

NVDD\_PG000

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NVDD\_PG000

NVDD\_PG000

NVDD\_PG000

NVDD\_PG000

NVDD\_PG000

12V Driver -> R7301:0 ohm, R7300:NC ohm  
9V Driver -> R7301:NC, R7301:0 ohm

1/19 modify FBVDDQ Enable time

11/19 modify 12V to 12V\_Pex6\_F1

2/9 remove R7304 and R7315  
N-NTMFS4841NHT1G\_S08-RH

FBVDDQ = 1.9-2.0V @ 31A~35A

V<sub>ripple</sub> 28mV

Local Capacitance at Supply

Combined Distributed Capacitance

Total FBVDDQ Capacitance

FBVDDQ

630 uF

490 uF

1120 uF

## FBVDDQ Power Supply

FBVDDQ = 1.9~20V @ 31A~35A

FB VOLTAGE SENSE

0.6 V X (1+ R<sub>top</sub> / R<sub>bot</sub>)

2.057V = 0.6 V X (1+ 2.55K / 1.05K)

1.833V = 0.6 V X (1+ 2.55K / 1.24K)

1.93V = 0.6 V X (1+ 2.55K / 1.15K)



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Date

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Number

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Rev

<RevCode>

ASSEMBLY

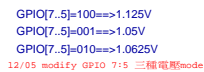
PAGE DETAIL

MAX LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO\_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

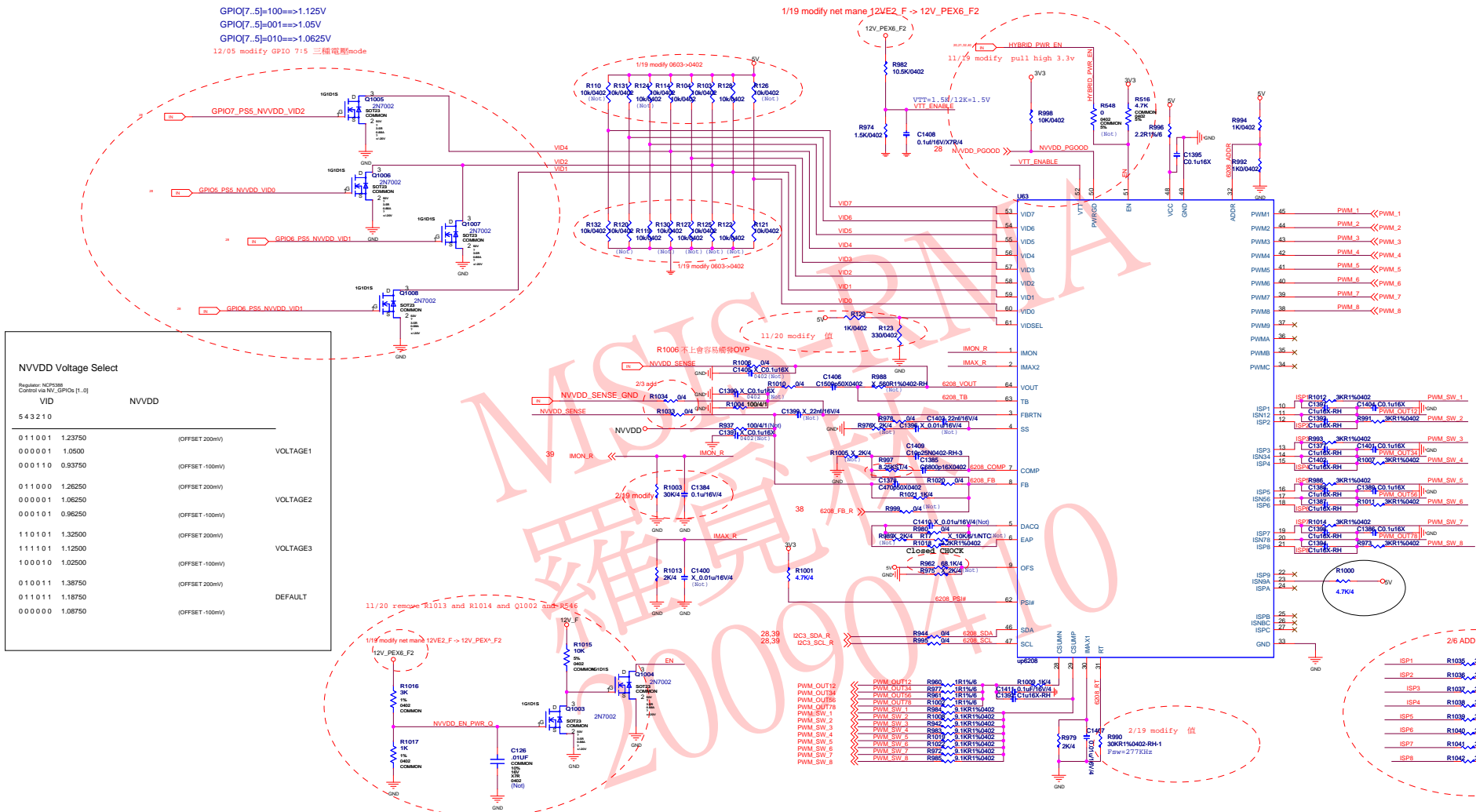
Power Supply: Combined FBVDDQ

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Power Supply: NVVDD Regulator



1/19 modify net mane ~~12VE2\_F~~ -> 12V\_PEX6\_F2

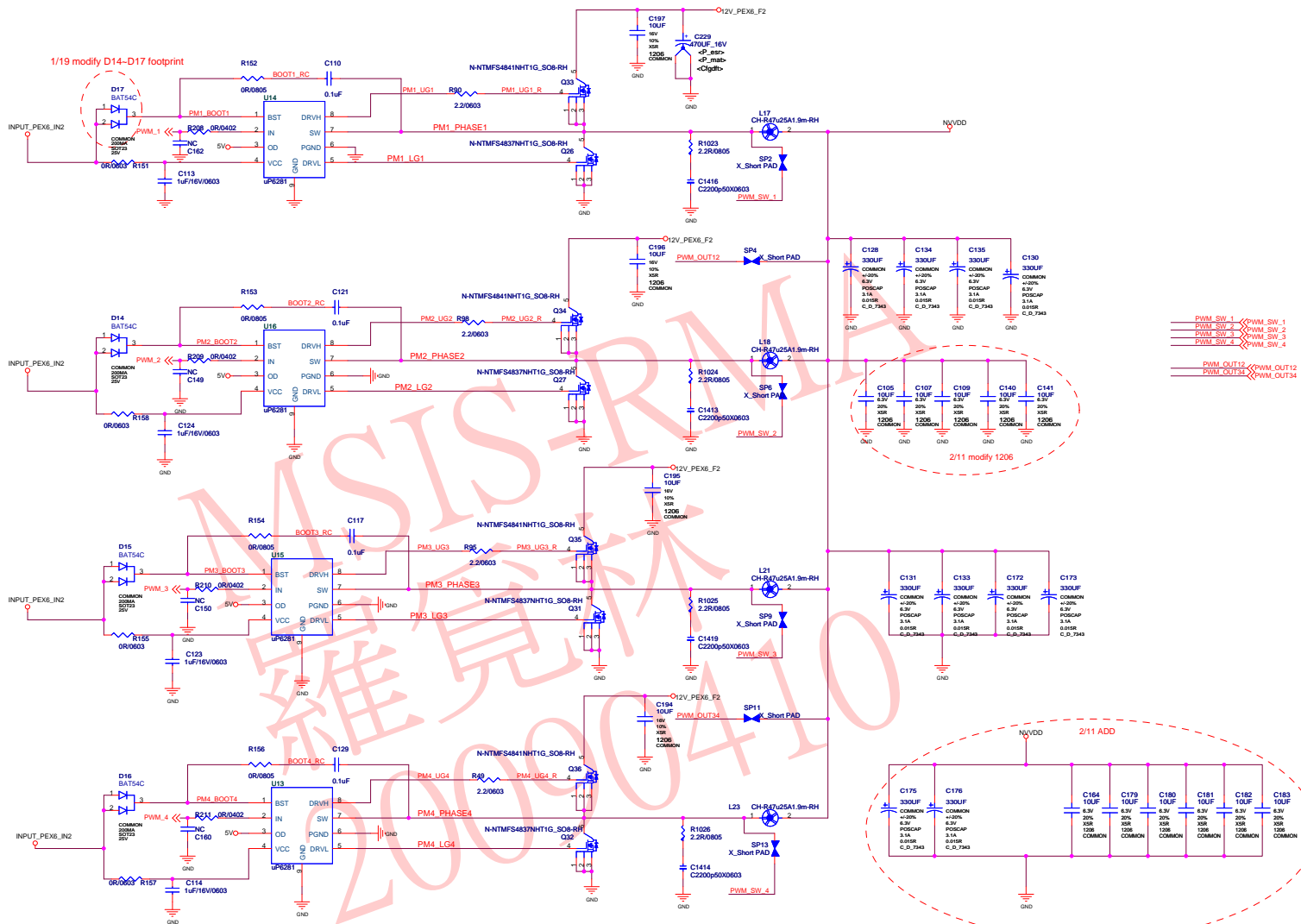



NVVDD Voltage Select			
Regulator: MCP5038 Control via NV_C0PFCs [1..2]			
V1D	NVVDD		
5 4 3 2 1 0			
0 1 1 0 0 1	1.23750	(OFFSET 200mV)	VOLTAGE1
0 0 0 0 0 1	1.0500		
0 0 0 1 1 0	0.93750	(OFFSET -100mV)	
0 1 1 0 0 0	1.26250	(OFFSET 200mV)	VOLTAGE2
0 0 0 0 0 1	1.06250		
0 0 0 1 0 1	0.96250	(OFFSET -100mV)	
1 1 0 1 0 1	1.32500	(OFFSET 200mV)	VOLTAGE3
1 1 1 1 0 1	1.12500		
1 0 0 0 1 0	1.02500	(OFFSET -100mV)	
0 1 0 0 1 1	1.38750	(OFFSET 200mV)	DEFAULT
0 1 1 0 1 1	1.18750		
0 0 0 0 0 0	1.08750	(OFFSET -100mV)	

2/6 ADD

	R1005	(Pci)	PVM
ISP1	R1005	30K11/0402	PVM_OUT12
ISP2	R1005	30K11/0402	PVM_OUT13
ISP3	R1005	30K11/0402	PVM_OUT14
ISP4	R1005	30K11/0402	PVM_OUT14
ISP5	R1005	30K11/0402	PVM_OUT156
ISP6	R1005	30K11/0402	PVM_OUT156
ISP7	R1005	30K11/0402	PVM_OUT178
ISP8	R1005	30K11/0402	PVM_OUT178

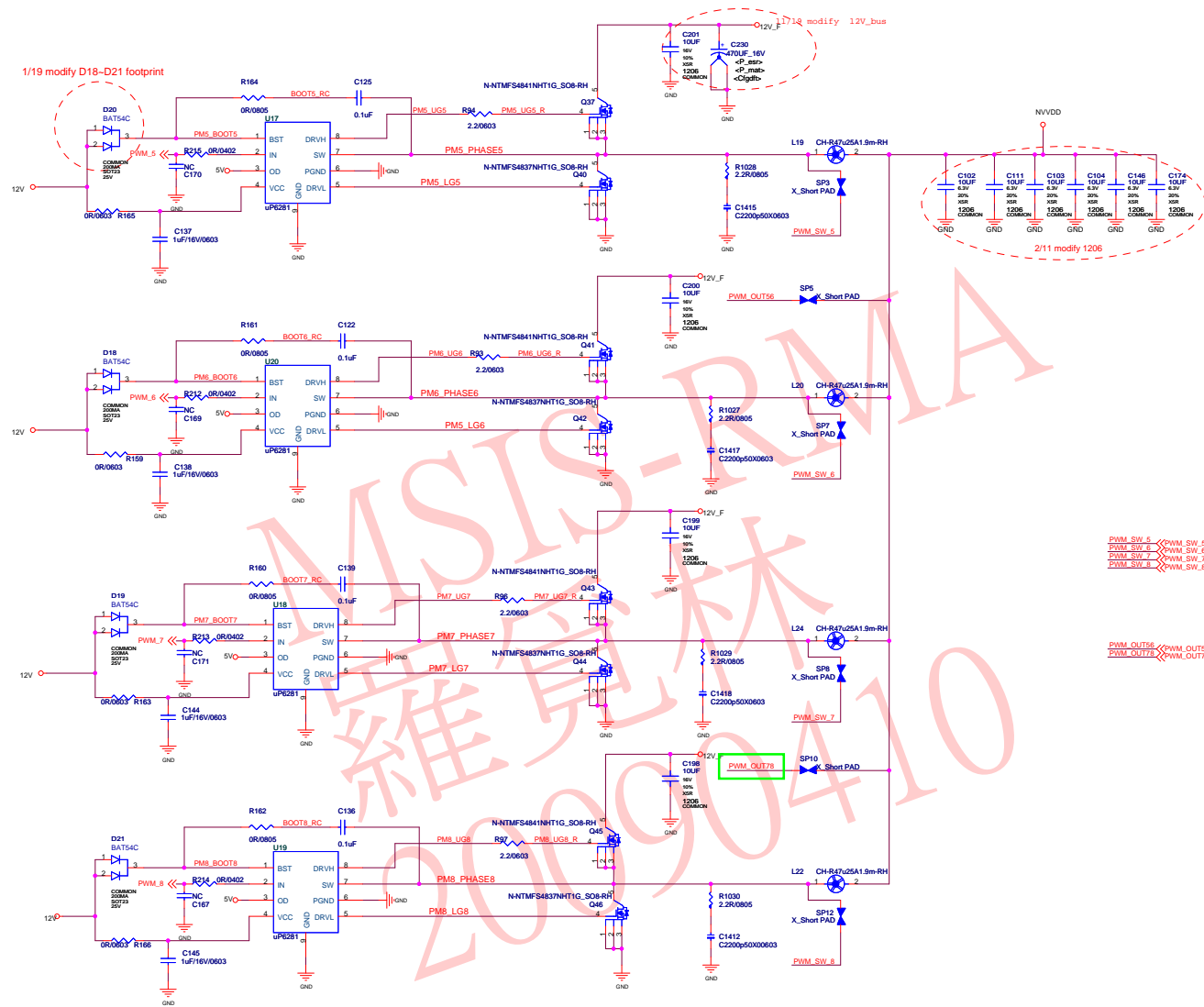
Power Supply: NVVDD Phase 1,2 powered from external PEX 6PIN



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	<file>		
	Size	Document Number	Rev
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# Power Supply: NVVDD Phase 5~8 powered from internal PEX edge connector

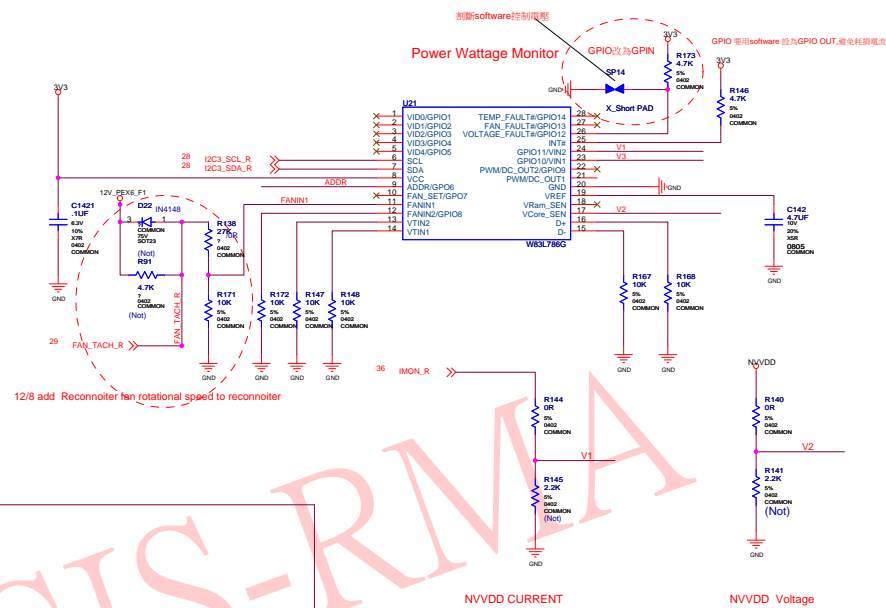
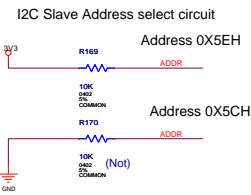


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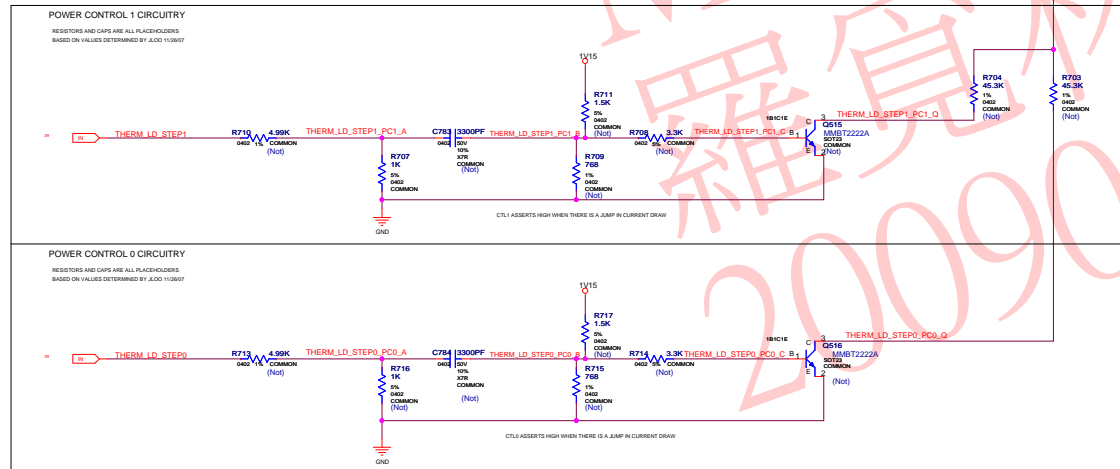
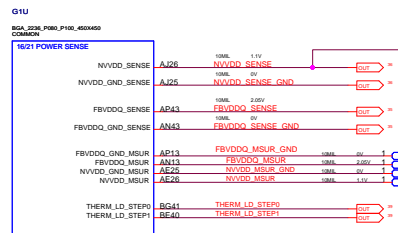
ASSEMBLY  
PAGE DETAIL  
BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 31000 ASSEMBLY NOTES AND BOM NOT FINAL  
Power Supply: NVVDD Phase 3-4 of 4

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Power Supply: NVVDD power control

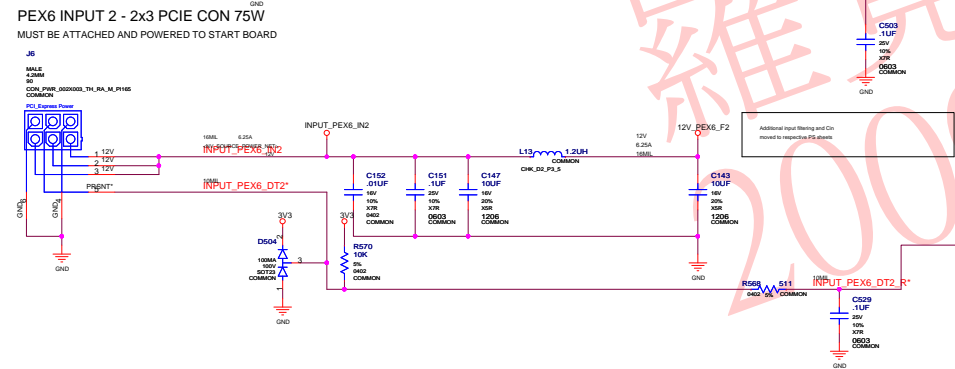
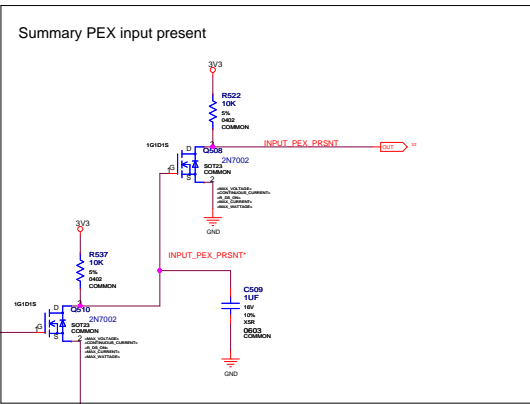
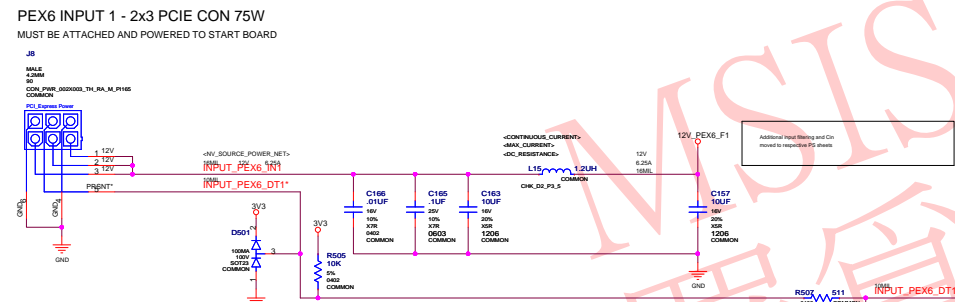
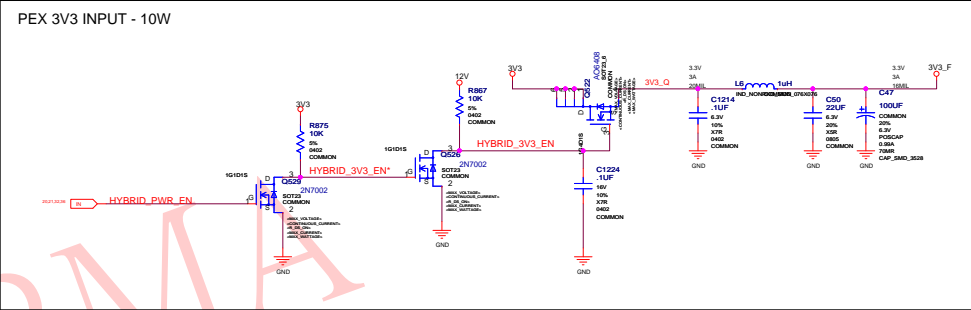
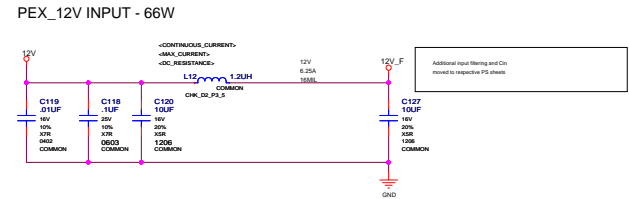


## NVVDD &amp; FBVDDQ SENSE/MSUR



Power: Input Rail Filter and Detection Logic

Connector Power State Table			
J33 Connector	J33 Connector	Power	STATE
Connected	Connected	225W	Full Post
Connected	Not Connected	105W	Board Off
Not Connected	Connected	105W	Board Off
Not Connected	Not Connected	75W	Board Off





# Thermal/Mechanical/ID

## Bracket and Assembly

MEC1  
MEC\_SCREW\_PN1  
COMMON  
MEC502  
MEC\_SCREW\_HEX\_JACK  
COMMON  
MEC503  
MEC\_SCREW\_HEX\_JACK  
COMMON  
MEC501  
MEC\_SCREW\_HEX\_JACK  
COMMON  
MEC504  
MEC\_SCREW\_HEX\_JACK  
COMMON

## GPU Socket

BGA SOCKET ASSY  
8 connected mounting pins  
MEC13  
BKT\_MGA\_POGO\_488X480\_PN10\_HIS  
COMMON

## GPU Stiffener

BOARD STIFFENER  
7 connected mounting pins  
MEC12  
BKT\_MGA\_OT200GPU\_T\_ST\_1  
COMMON

## NVIOx Socket

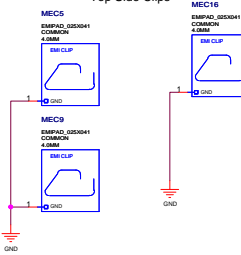
BGA SOCKET ASSY  
4 connected mounting pins  
MEC6  
BKT\_MGA\_POGO\_238X230  
COMMON

## Hockey Stick Retention Mechanism

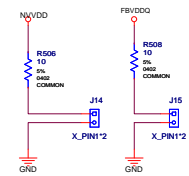
SPECIAL MECHANIC  
No connected mounting pins  
MEC2  
MECH\_PEN\_BREAKOFF\_RETENTION\_PN01  
COMMON

## EMI Gnd Clips

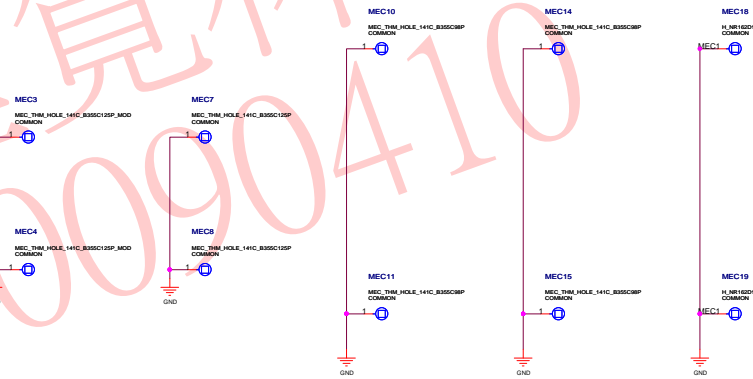
### Top Side Clips



### 電源量測點



## THERMAL/MECHANICAL HOLES



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