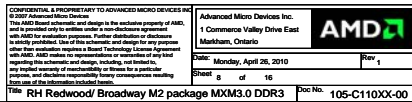
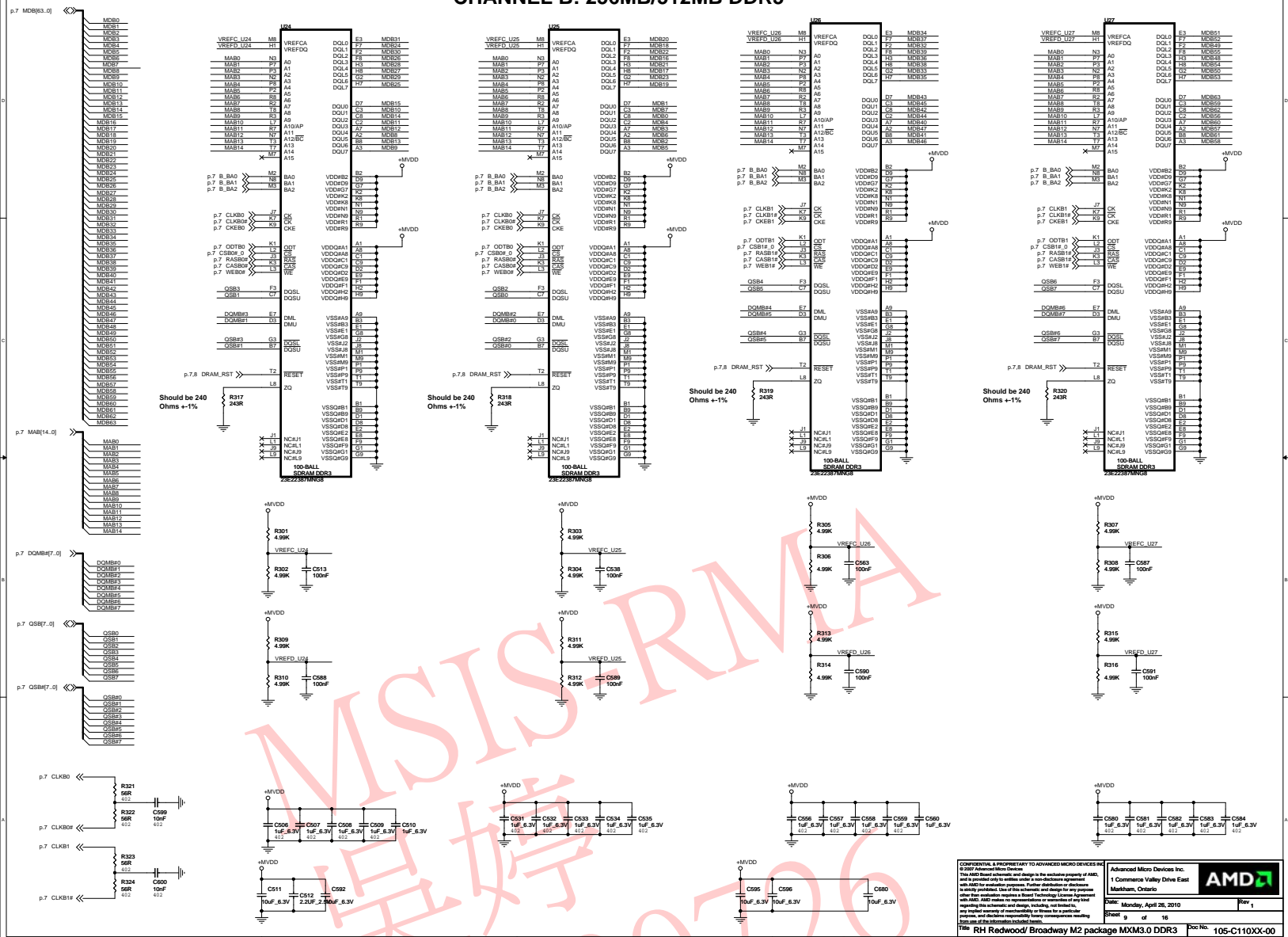


CHANNEL A: 256MB/512MB DDR3



CHANNEL B: 256MB/512MB DDR3



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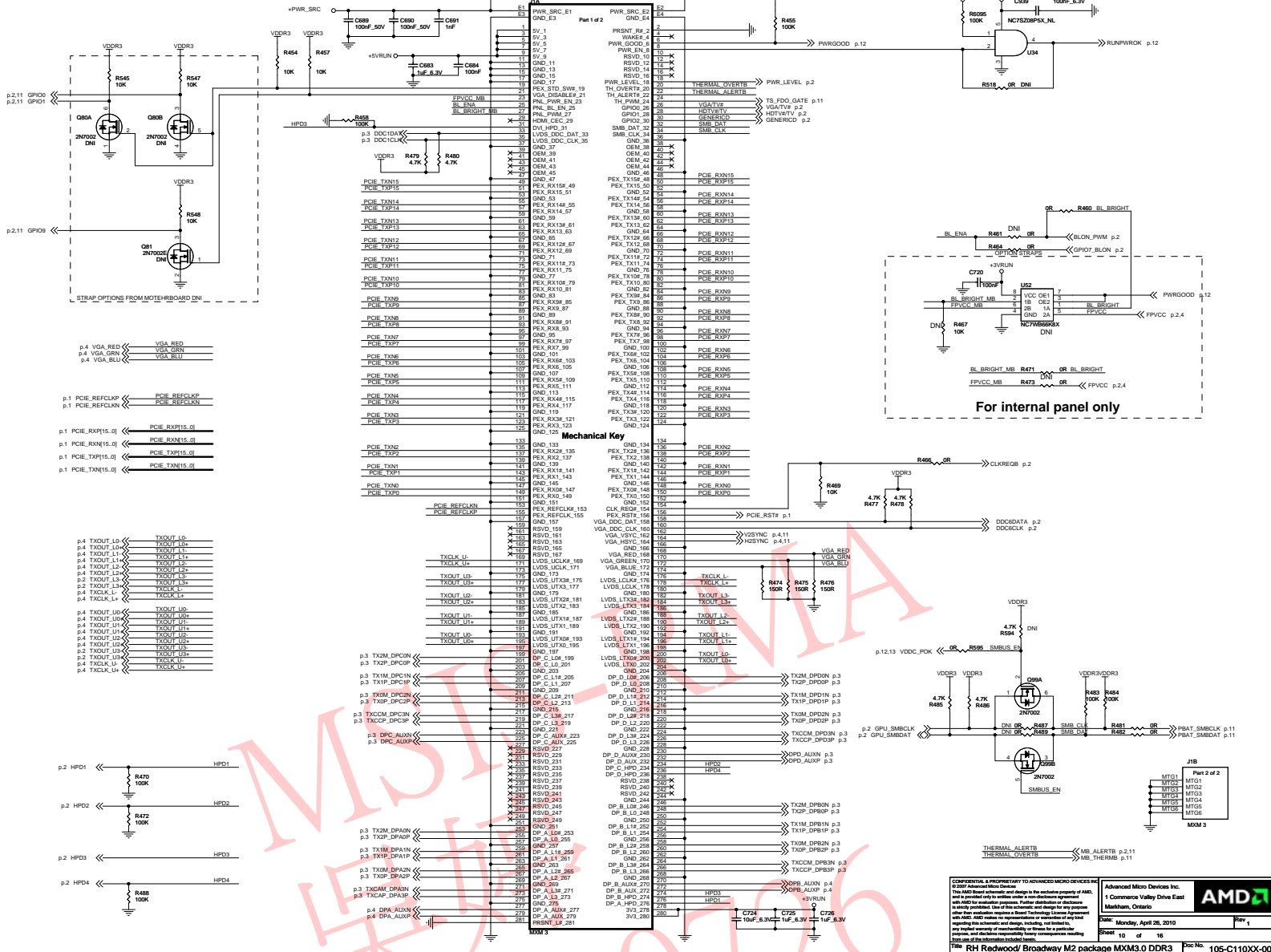
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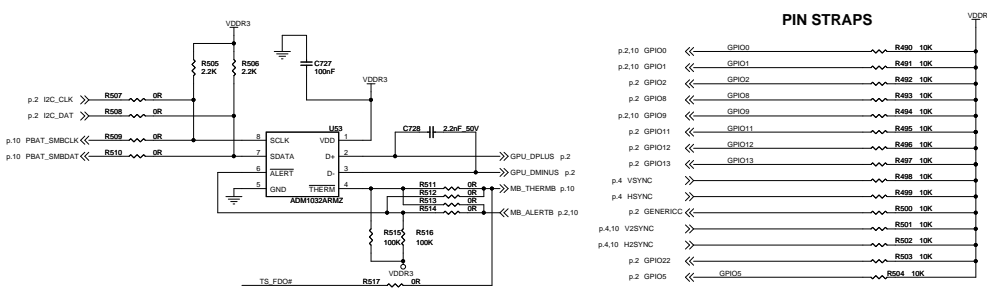
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Project RH Redwood/ Broadway Mx3 device MXM3.0 DDR3

Doc No. 105-1110X-00



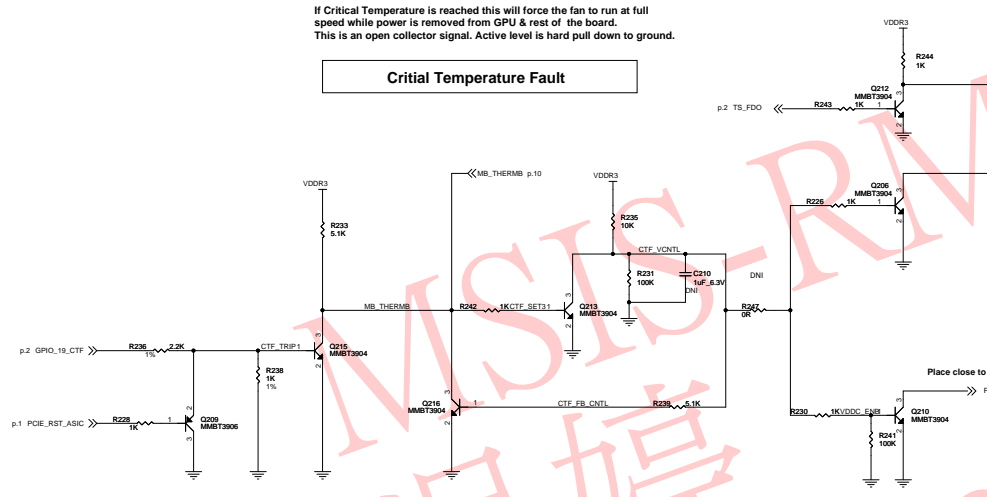
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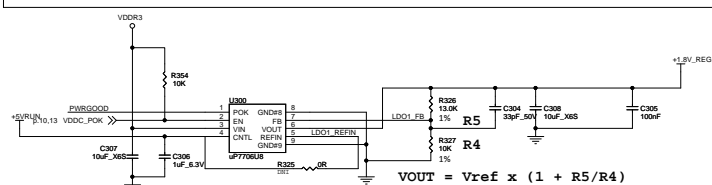
PIN STRAPS

p.2.10 GPIO0	<< GPIO0	R490 10K
p.2.10 GPIO1	<< GPIO1	R491 10K
p.2.10 GPIO2	<< GPIO2	R492 10K
p.2.10 GPIO8	<< GPIO8	R493 10K
p.2.10 GPIO9	<< GPIO9	R494 10K
p.2.10 GPIO11	<< GPIO11	R495 10K
p.2.10 GPIO12	<< GPIO12	R496 10K
p.2.10 GPIO13	<< GPIO13	R497 10K
p.4 VSYNC	<< VSYNC	R498 10K
p.4 HSYNC	<< HSYNC	R499 10K
p.2 GENERICC	<< GENERICC	R500 10K
p.4.10 V2SYN	<< V2SYN	R501 10K
p.4.10 H2SYN	<< H2SYN	R502 10K
p.2 GPIO22	<< GPIO22	R503 10K
p.2 GPIO5	<< GPIO5	R504 10K

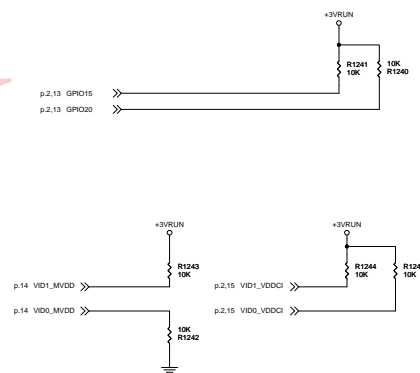
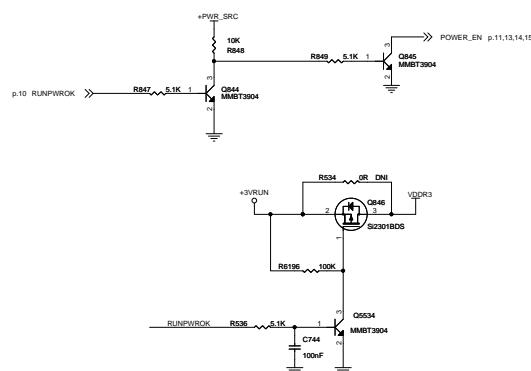
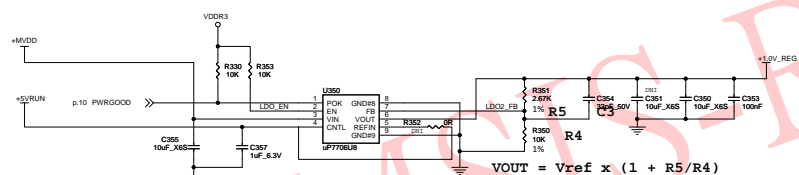
CONFIGURATION STRAPS			RECOMMENDED SETTINGS (= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDENT NA = NOT APPLICABLE)
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIe FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIe GEN2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF CLK PM EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLS_CALIB_BP	GPIO1	BIF_RX_PLS_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCS8	ENABLE EXTERNAL BIOS ROM	1
ROMDCFG22	GPIO13[11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYN	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYN	GENERICC	0
COBYPASS	HSYN	HSYN	0
AUD1	V2SYN	built-in HDMI connector	1
AUD0	V2SYN	Audio function present	1
MEMORY_CFG	[GPIO0:GPIO16]		1
HYNX	[1-1]		1
SAMSUNG	[1-1]		1
AMD RESERVED CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
H2SYN	GENERICC		
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
GPIO_28_TDO	GPIO21_BB_EN		



LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.0V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling




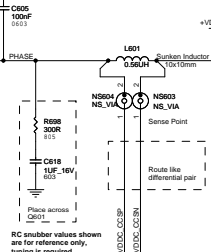
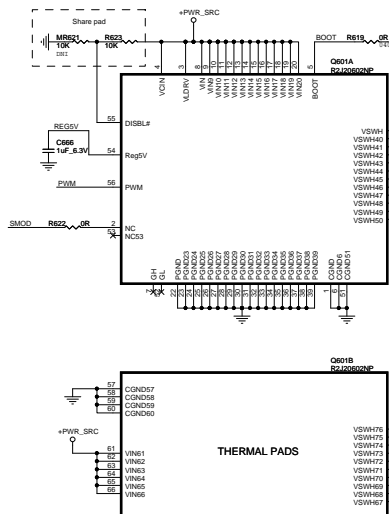
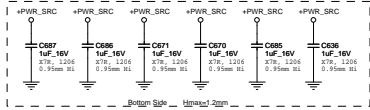
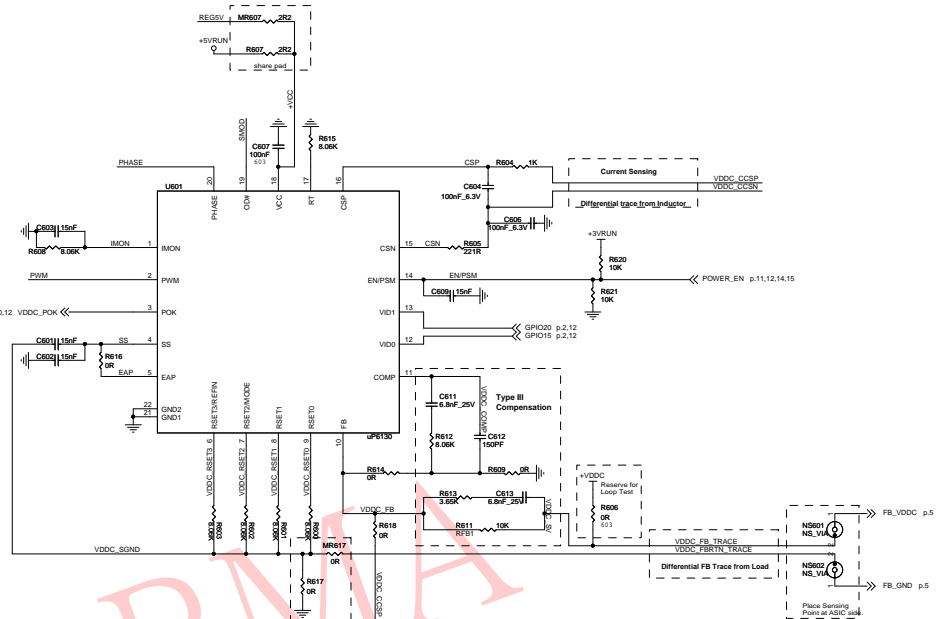
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Title: RH Redwood/ Broadway M2 package MXM3.0 DDR3		Doc No:	105-C110X-00		

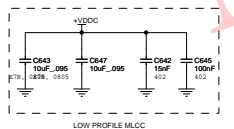
Figure 10 shows the power plane layout for the top side of the board. It features four power source symbols, each labeled +PWR_SRC, connected to a common ground plane. Each symbol includes a capacitor (C657, C669, C638, C665) with a value of 2.2uF_16V and a reference to X7R, 1206, 1.3mm HI. The layout is labeled 'Top Side' and 'Hmax=1.5mm'.

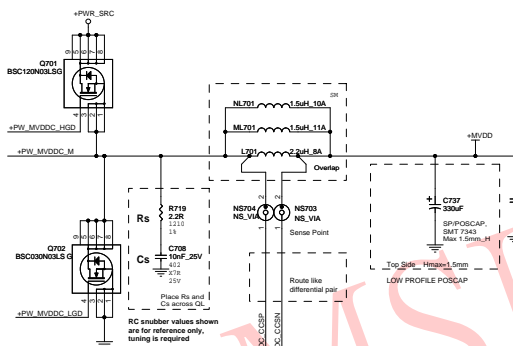
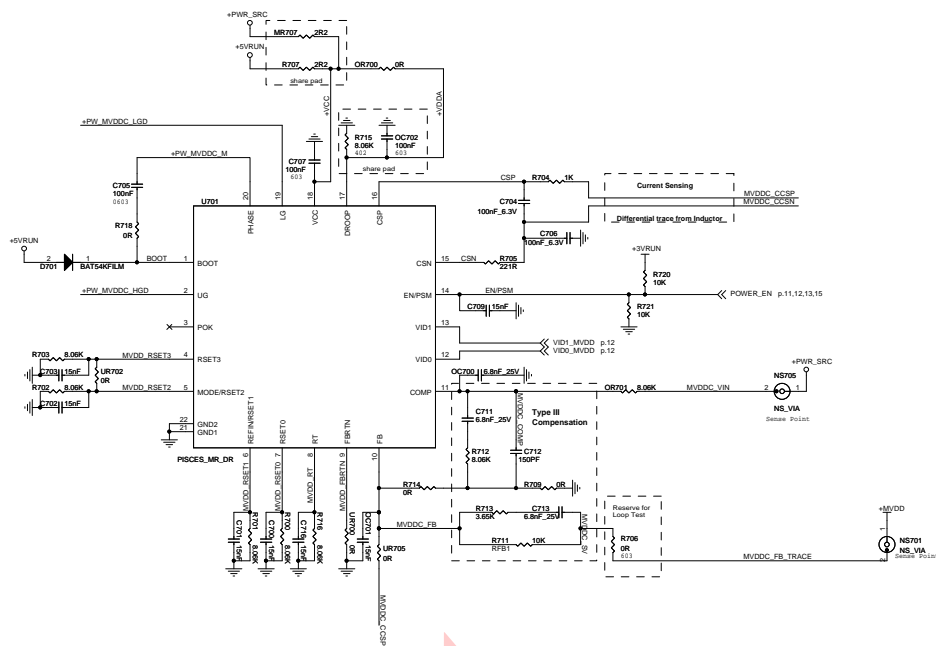
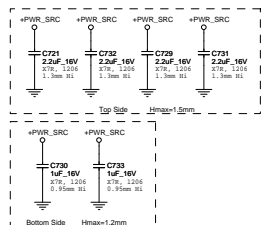


Pin Difference Between R2J2062NP and R2J2065NP		
	R2J2062NP	R2J2065NP
3	VLSRV	NC
8	VIN	NC
2	NC	LSDBL#
53	NC	THRN



Top Side Hmax<1.5mm





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