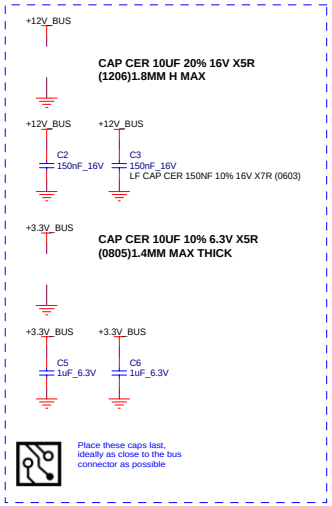
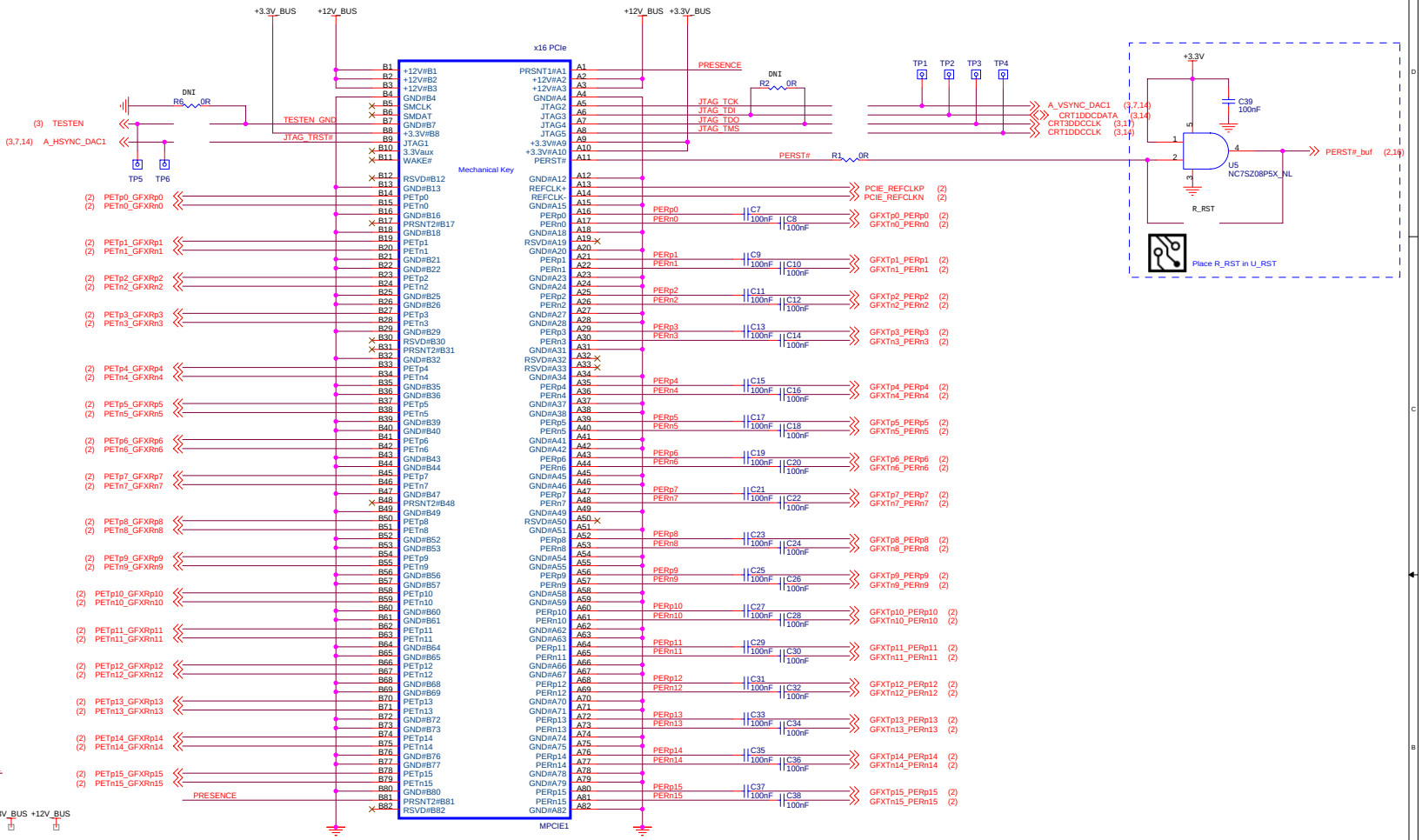
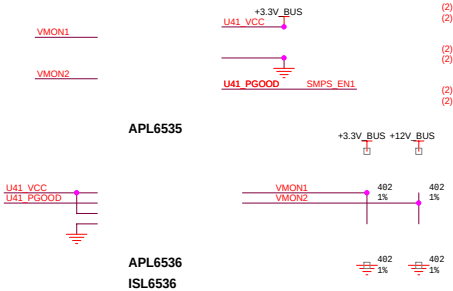
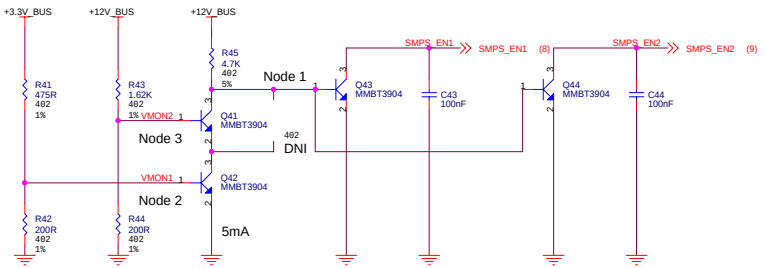
PCI-EXPRESS EDGE CONNECTOR





POWER SEQUENCING





Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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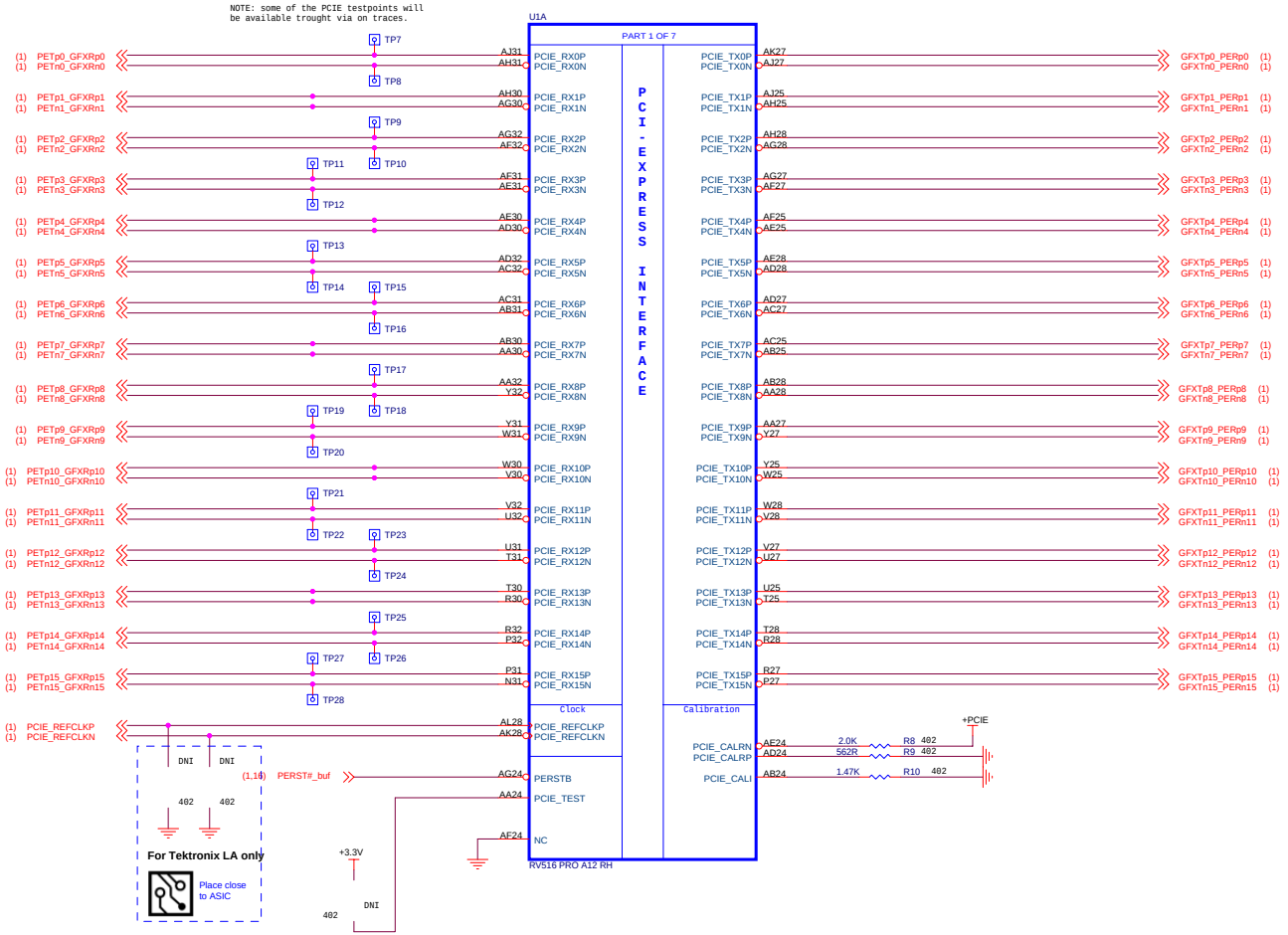

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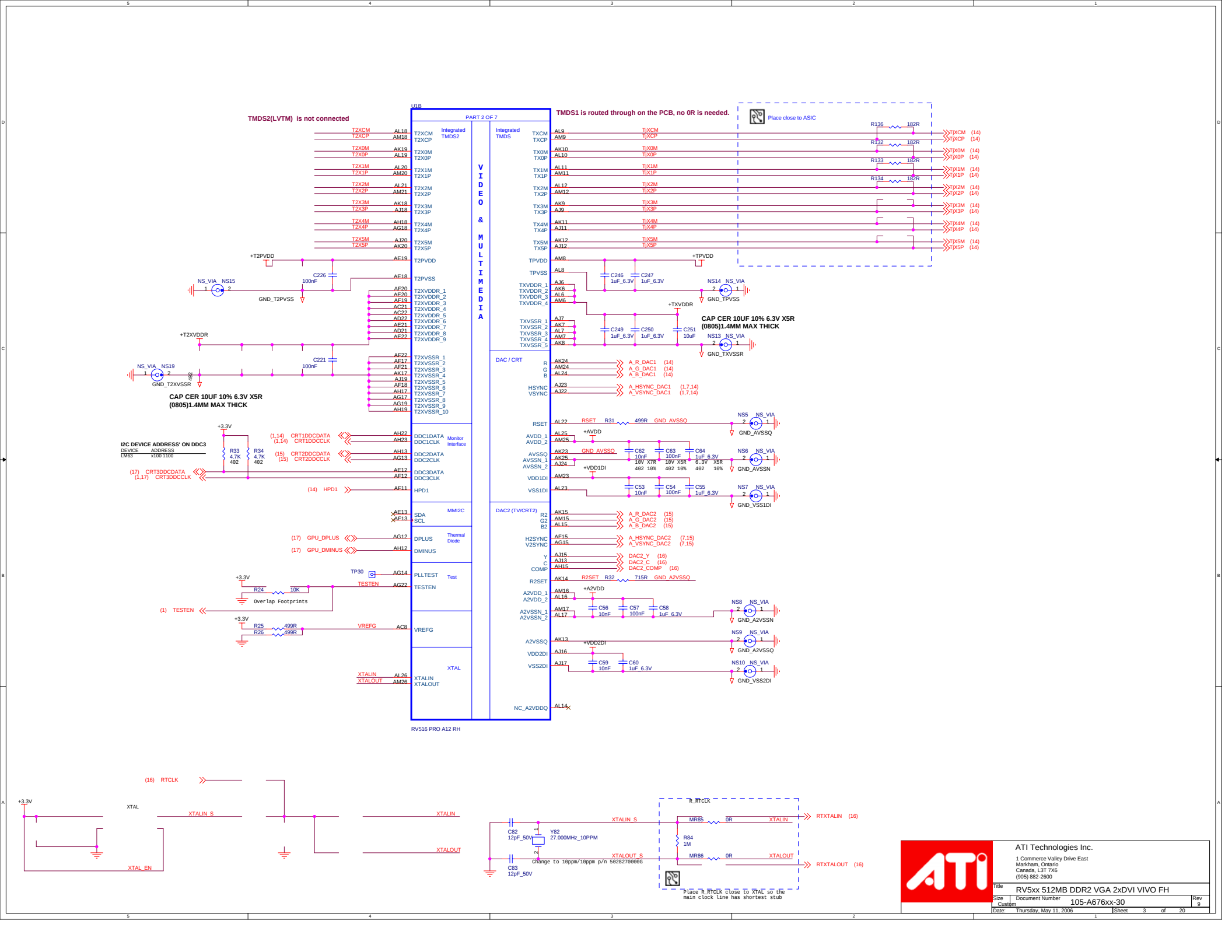
TMDS2(LVTM) is not connected
TMDS1 is routed through on the PCB, no 0R is needed.
Place close to ASIC
U1B
PART 2 OF 7
VIDEO & MULTIMEDIA
Integrated TMDS2
Integrated TMDS
DAC / CRT
DAC2 (TV/CRT2)
Monitor Interface
MMI2C
Thermal Diode
Test
XTAL
CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK
I2C DEVICE ADDRESS' ON DDC3
DEVICE ADDRESS
LM63 x100 1100
RV516 PRO A12 RH
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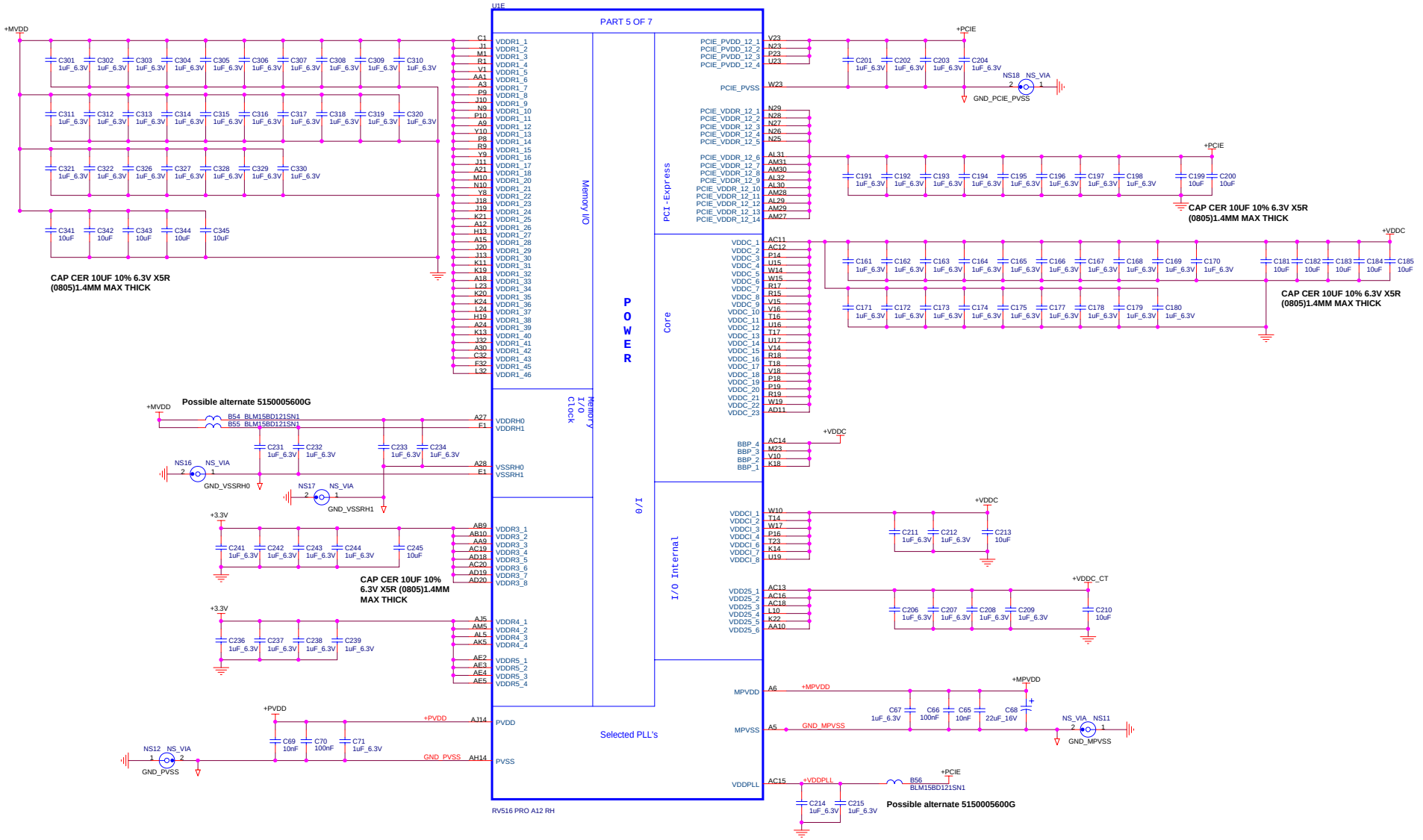
RV5xx 512MB DDR2 VGA 2xDVI VIVO FH
105-A676xx-30
Thursday, May 11, 2006
Sheet 3 of 20
Place R_RTCLK close to XTAL so the main clock line has shortest stub



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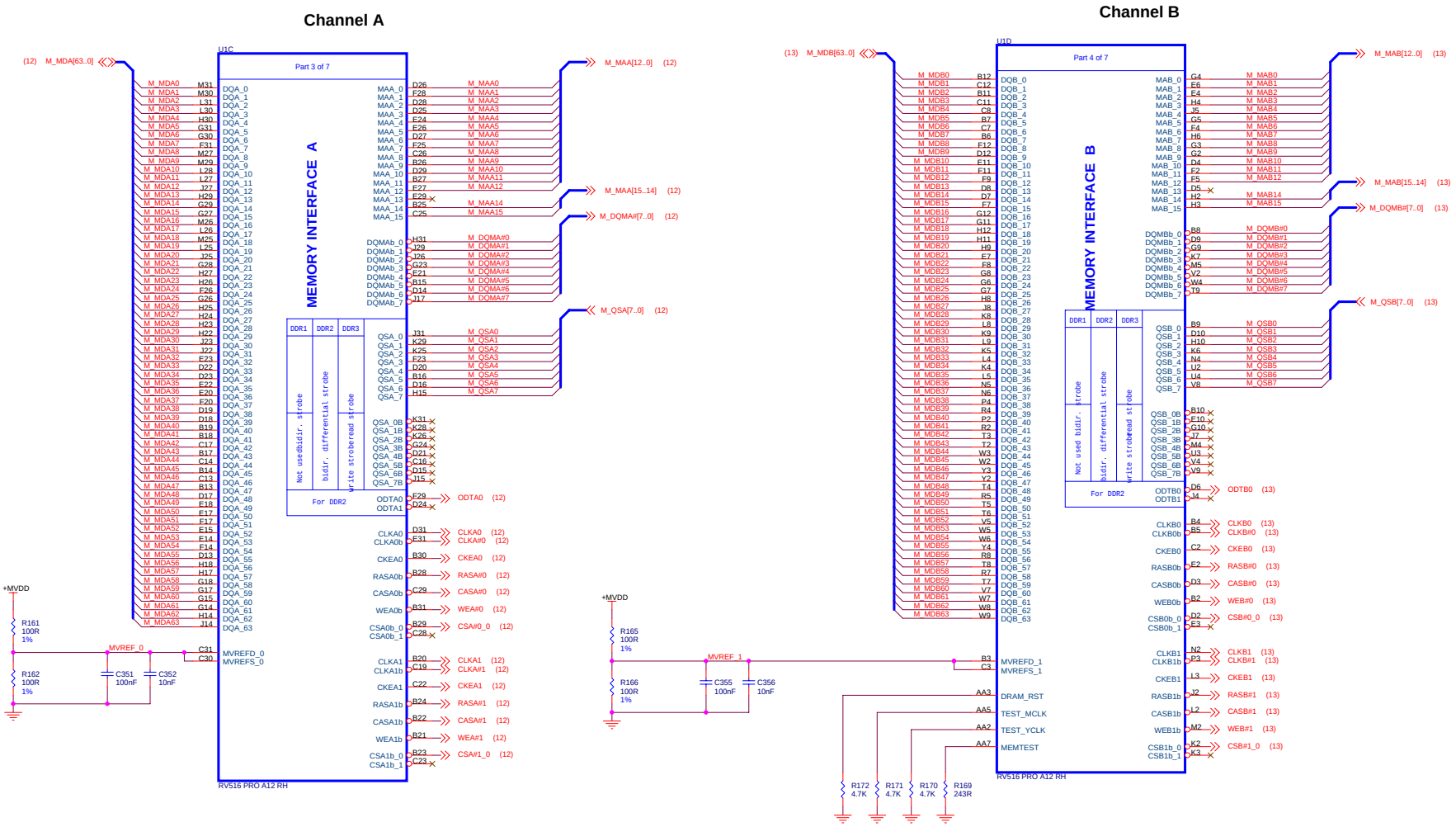
RV530 MEMORY CHANNELS A and B



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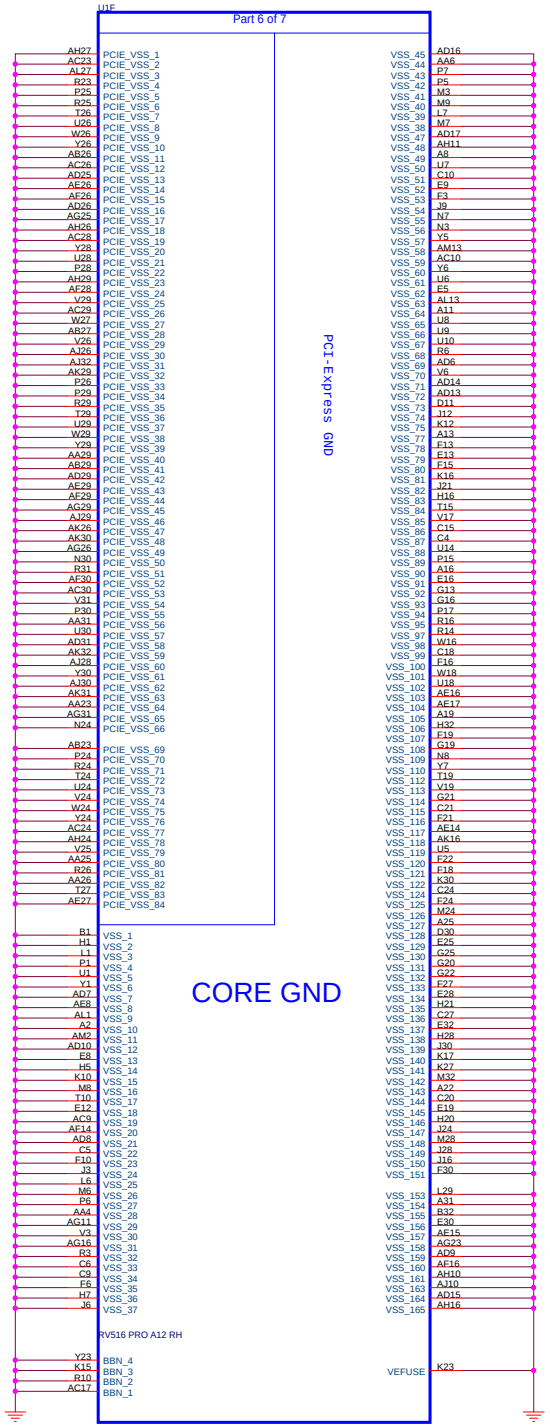

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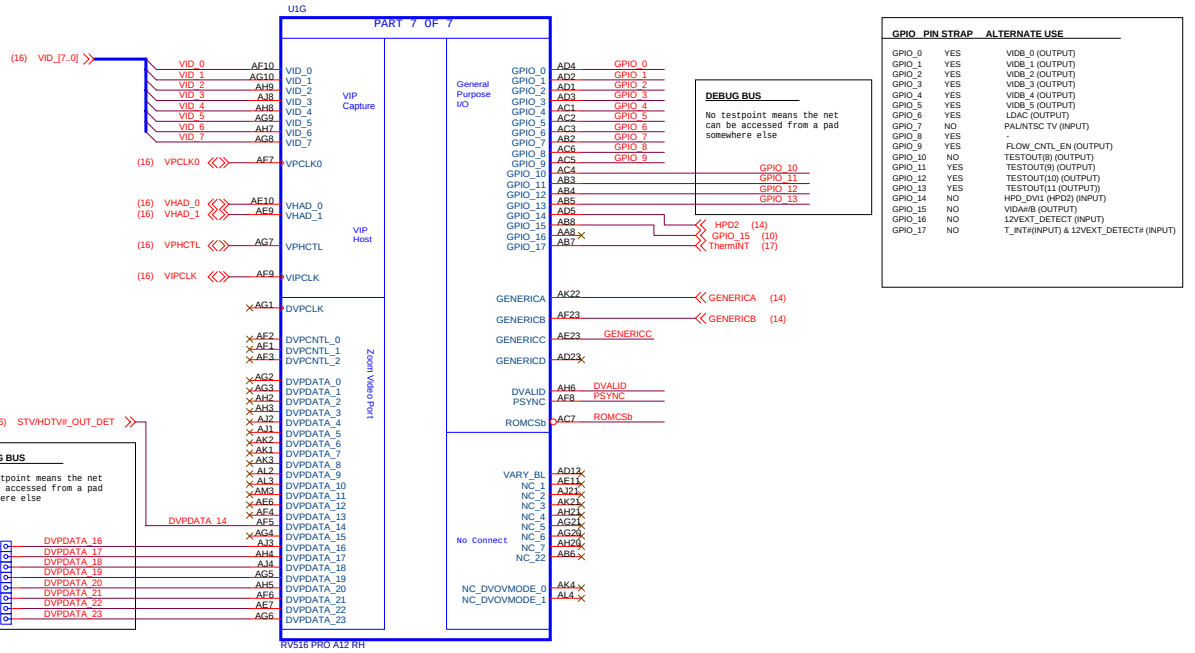
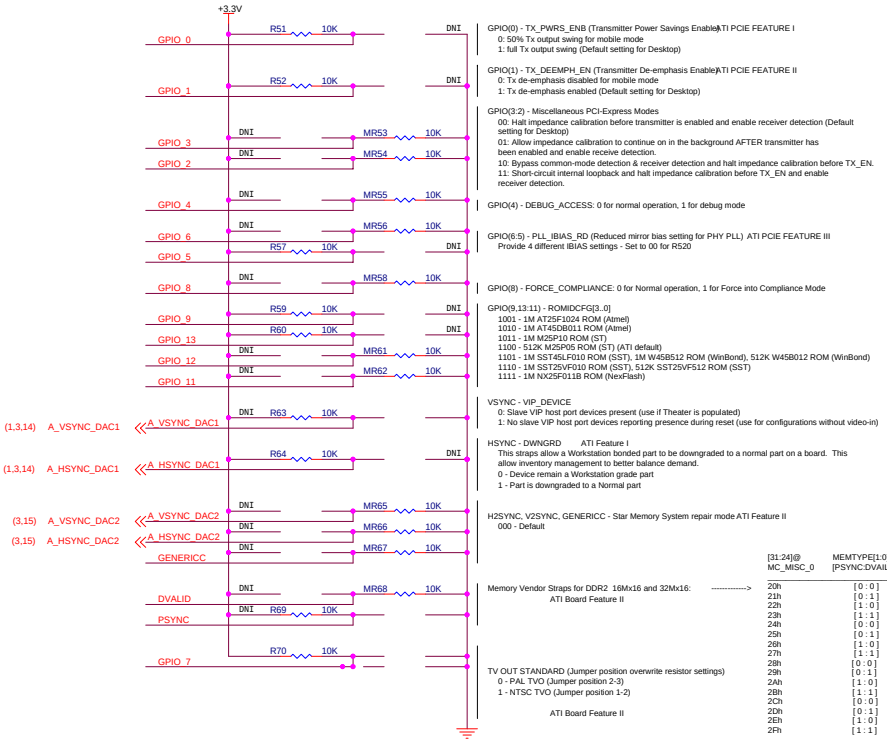


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDA#/B (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

DVPDATA	ALTERNATE USE
DVPDATA_0	-
DVPDATA_1	-
DVPDATA_2	-
DVPDATA_3	-
DVPDATA_4	-
DVPDATA_5	-
DVPDATA_6	-
DVPDATA_7	-
DVPDATA_8	-
DVPDATA_9	-
DVPDATA_10	-
DVPDATA_11	-
DVPDATA_12	-
DVPDATA_13	-
DVPDATA_14	STV/HDTV#_OUT_DET (INPUT)
DVPDATA_15	-
DVPDATA_16	TESTOUT(0) (OUTPUT)
DVPDATA_17	TESTOUT(1) (OUTPUT)
DVPDATA_18	TESTOUT(2) (OUTPUT) / NTSC/PAL#_TVO_DET (INPUT)
DVPDATA_19	TESTOUT(3) (OUTPUT)
DVPDATA_20	TESTOUT(4) (OUTPUT)
DVPDATA_21	TESTOUT(5) (OUTPUT)
DVPDATA_22	TESTOUT(6) (OUTPUT)
DVPDATA_23	TESTOUT(7) (OUTPUT)

PIN BASED STRAPS



GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - Miscellaneous PCI-Express Modes
00: Halt impedance calibration before transmitter is enabled and enable receiver detection (Default setting for Desktop)
01: Allow impedance calibration to continue on in the background AFTER transmitter has been enabled and enable receive detection.
10: Bypass common-mode detection & receiver detection and halt impedance calibration before TX_EN.
11: Short-circuit internal loopback and halt impedance calibration before TX_EN and enable receiver detection.

GPIO(4) - DEBUG_ACCESS: 0 for normal operation, 1 for debug mode

GPIO(6:5) - PLL_IBIAS_RD (Reduced mirror bias setting for PHY PLL) ATI PCIE FEATURE III
Provide 4 different IBIAS settings - Set to 00 for R520

GPIO(8) - FORCE_COMPLIANCE: 0 for Normal operation, 1 for Force into Compliance Mode

GPIO(9,13:11) - ROMIDCFG[3..0]
1001 - 1M AT25F1024 ROM (Atmel)
1010 - 1M AT45DB011 ROM (Atmel)
1011 - 1M M25P10 ROM (ST)
1100 - 512K M25P05 ROM (ST) (ATI default)
1101 - 1M SST45LF010 ROM (SST), 1M W45B512 ROM (WinBond), 512K W45B012 ROM (WinBond)
1110 - 1M SST25VF010 ROM (SST), 512K SST25VF512 ROM (SST)
1111 - 1M NX25F011B ROM (NexFlash)

VSYNC - VIP_DEVICE
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - DWNGRD ATI Feature I
This straps allow a Workstation bonded part to be downgraded to a normal part on a board. This allow inventory management to better balance demand.
0 - Device remain a Workstation grade part
1 - Part is downgraded to a Normal part

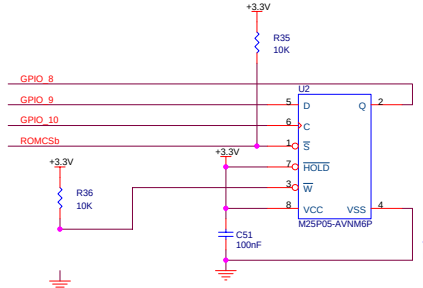
H2SYNC, V2SYNC, GENERICC - Star Memory System repair mode ATI Feature II
000 - Default

Memory Vendor Straps for DDR2 16Mx16 and 32Mx16: ----------> ATI Board Feature II

[31:24]@ MC_MISC_0	MEMTYPE[1:0] [PSYNC:DVALID]	Memory
20h	[0 : 0]	Common and Infineon 16Mx16 2.0V
21h	[0 : 1]	Samsung 16Mx16
22h	[1 : 0]	Infineon 16Mx16 1.8V
23h	[1 : 1]	Hynix 16Mx16
24h	[0 : 0]	Micron 16Mx16
25h	[0 : 1]	Elpida 16Mx16
26h	[1 : 0]	Reserved
27h	[1 : 1]	Reserved
28h	[0 : 0]	Common 32Mx16
29h	[0 : 1]	Samsung 32Mx16
2Ah	[1 : 0]	Infineon 32Mx16
2Bh	[1 : 1]	Hynix 32Mx16
2Ch	[0 : 0]	Micron 32Mx16
2Dh	[0 : 1]	Elpida 32Mx16
2Eh	[1 : 0]	Reserved
2Fh	[1 : 1]	Reserved

TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper position 2-3)
1 - NTSC TVO (Jumper position 1-2)

ATI Board Feature II



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VDDC-PWM1

SIPEX SP6132A p/n 2480054700G

VDDC-PWM2

INTERSIL ISL6522/ISL6535
RICHTEK RT9232/RT9232A
ANPEC APW7062A
ANPEC APW7062B

VDDC-PWM3

RICHTEK RT9214
INTERSIL ISL6545

VDDC-PWM4

ANPEC APW7061A

QH
QL
Q603
Q602
BSC119N03SG
BSC032N03S G
CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX
CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK
MULTI FOOTPRINT
DUAL FOOTPRINT
Rs
Cs
Place Rs and Cs across Q5
RC snubber values shown are for reference only, tuning is required
R1
R4
Place R1 and R4 close to PWM and routed with separate 20mil trace to the ASIC
0.8V Ref
R4 = (R1 x 0.8V) / (Vout1 - 0.8V)

This symbol is used for 103 SMPS p/n.

VDDC1

Regulator for VDDC (ASIC Core)
Vout = 1V ~ 1.3V

Part	Vout	R1	R2
0.8V Ref	1.2Vmin/1.22Vnorm/1.24Vmax	200R p/n 3160200000G (402 1%)	383R p/n 3160383000G (402 1%)

COMPENSATION CIRCUIT

FILTERED +12V_BUS

BOOT CIRCUIT

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Size: Custom | Document Number: 105-A676xx-21 | Rev: 8
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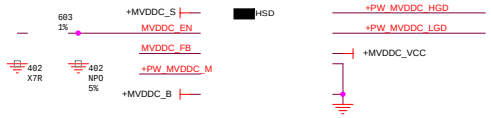
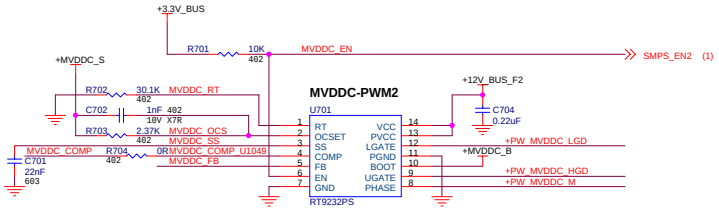
MVDDC-PWM1



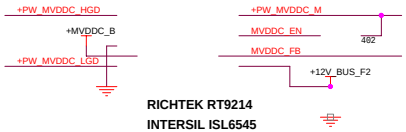
MAXIM MAX1954
MAXIM MAX1954A

MVDDC-PWM2



INTERSIL ISL6522
RICHTEK RT9232A
ANPEC APW7062A
ANPEC APW7062B

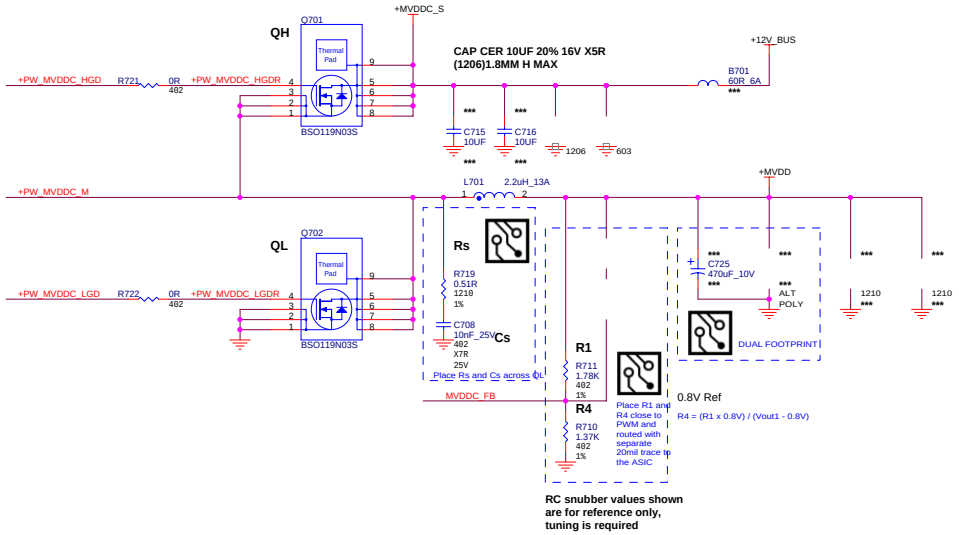
MVDDC-PWM3



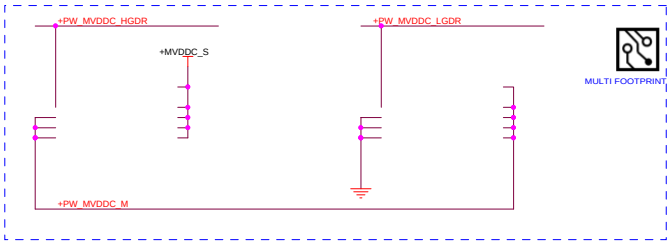
RICHTEK RT9214
INTERSIL ISL6545

MVDDC-PWM4

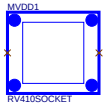
ANPEC APW7061A



RC snubber values shown are for reference only, tuning is required



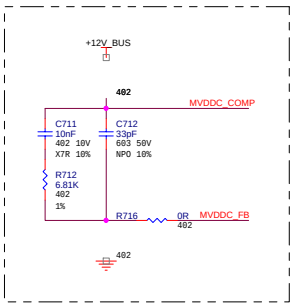
This symbol is used for 103 SMPS p/n.



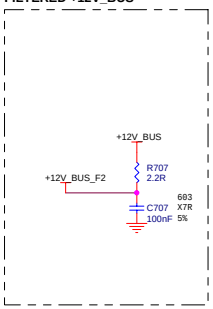
Regulator for MVDD
Vout = 1.8V ~ 2.85V

Part	Vout	R1	R2
0.8V Ref	1.9V	1.78K	1.3K
	2.0V	1.69K 1.78K	1.1K 1.21K

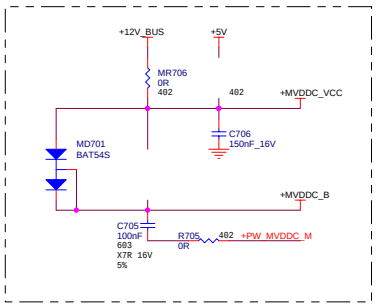
COMPENSATION CIRCUIT



FILTERED +12V_BUS



BOOT CIRCUIT



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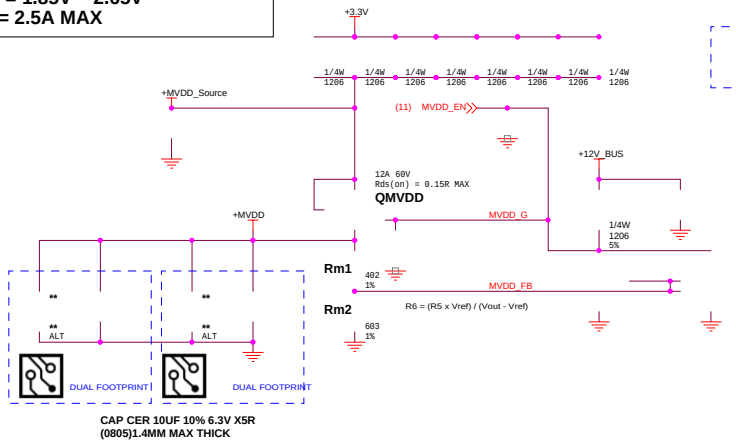
Regulator for +MVDDQ
Vout = 1.85V ~ 2.65V
Iout = 2.5A MAX

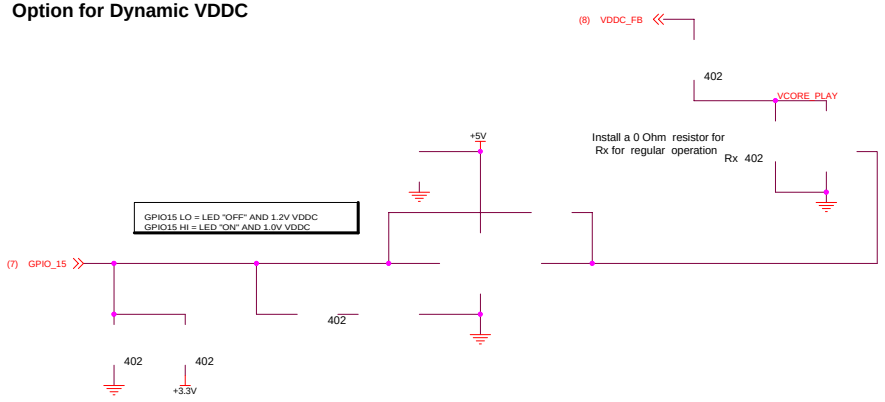


CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

Place Big Copper Area Under QMVDD
pin 2 and 4 for Heat Dissipation.

Voltage Req.	Rm1		Rm2		
2.85V					
2.55V	22.1R	316022R100G	1.1K	3240110100G	2.5V Ref.
2.5V	0R	3150000000	DNI		2.5V Ref.
2.1V min	681R	3160681000G	953R	3240953000	1.24V Ref.
2.0V min	681R	3160681000G	1.1K	3240110100G	1.24V Ref.
1.9V min, 1.94V nom.	562R	3160562000G	1K	3160100100G	1.24V Ref.

Option for Dynamic VDDC



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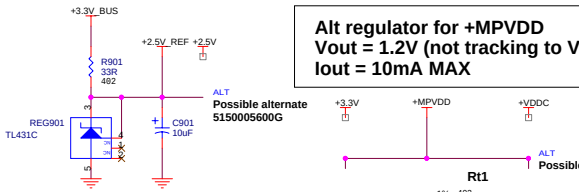
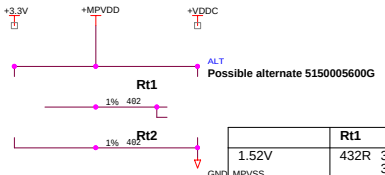
Alt regulator for +MPVDD
Vout = 1.2V (not tracking to VDDC)
Iout = 10mA MAX

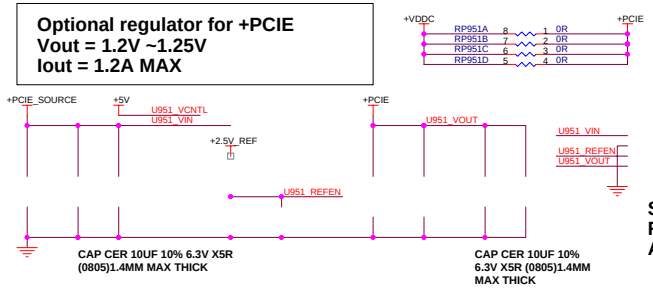
Optional regulator for +PCIE
Vout = 1.2V ~1.25V
Iout = 1.2A MAX

RT9199 p/n 2480054800G (480mR RdsON Max)
RT9199A (300mR RdsON Max)
RT9173C (250mR RdsON Max)
APL5331 p/n 2480054200G (350mR MAX for 2A)

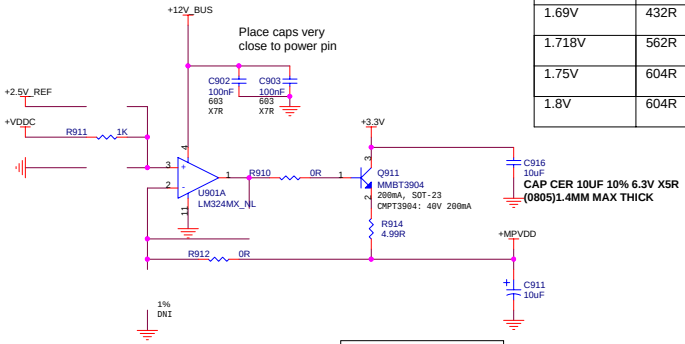




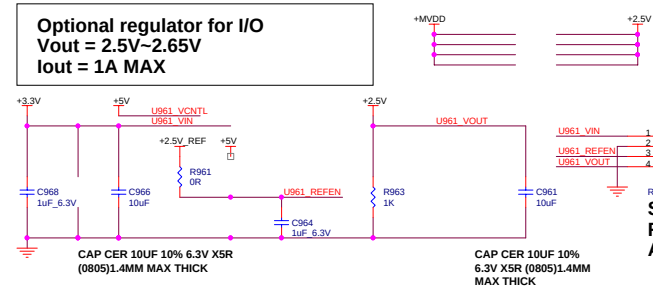
	Rt1		Rt2	
1.52V	432R	3240432000 3160432000	2.15K	 3160215100
1.61V	432R	3240432000	1.5K 1.5K	3230015200 3160150100
1.69V	432R	3240432000	1.21K	3240121100
1.718V	562R	3240562000	1.5K 1.5K	3230015200 3160150100
1.75V	604R	3160604000	1.5K 1.5K	3230015200 3160150100
1.8V	604R	3160604000	1.37K	3160137100



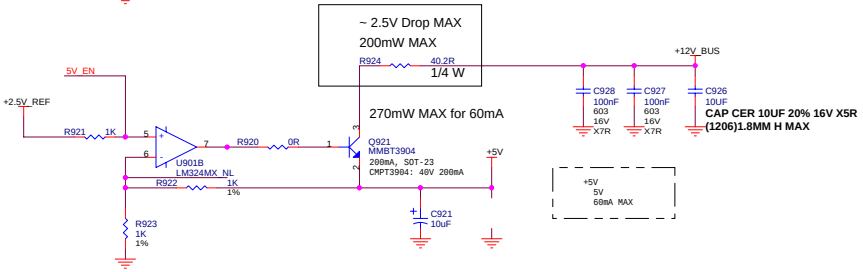
Supported footprint:
RT9173C/RT9199A/RT9199
APL5331



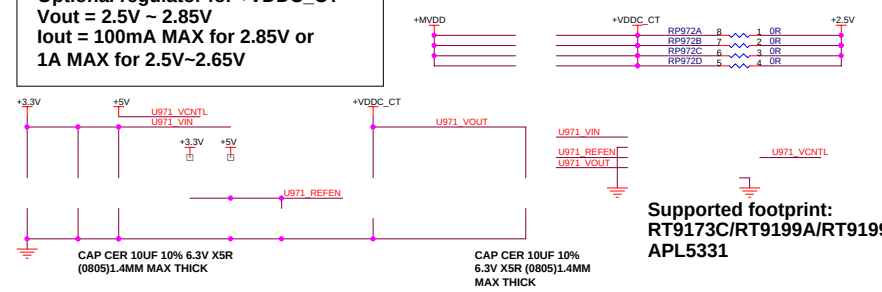
Optional regulator for I/O
Vout = 2.5V~2.65V
Iout = 1A MAX



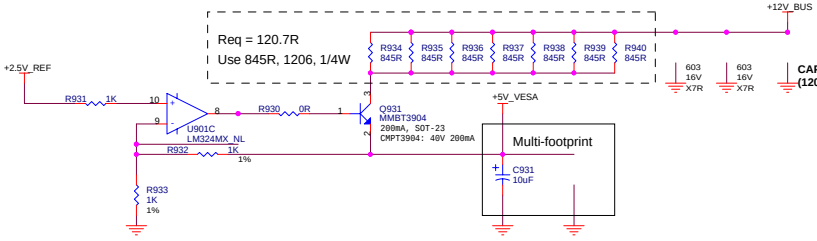
Supported footprint:
RT9173C/RT9199A/RT9199
APL5331

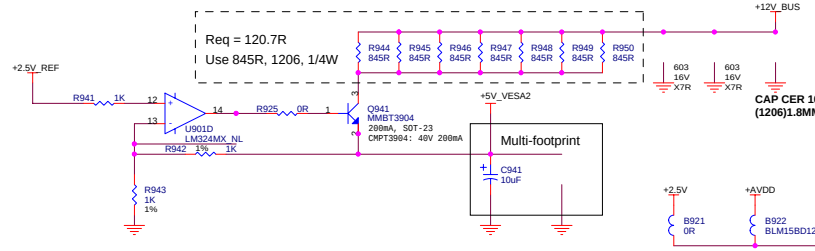


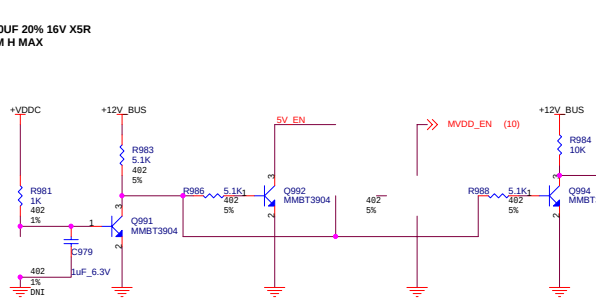
Optional regulator for +VDDC_CT
Vout = 2.5V ~ 2.85V
Iout = 100mA MAX for 2.85V or
1A MAX for 2.5V~2.65V

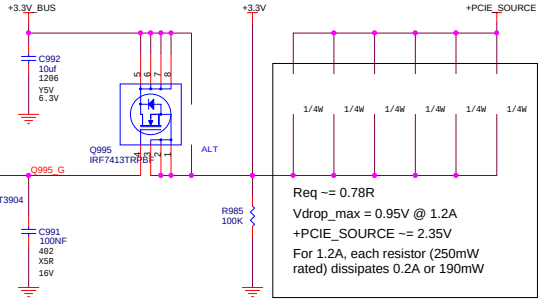


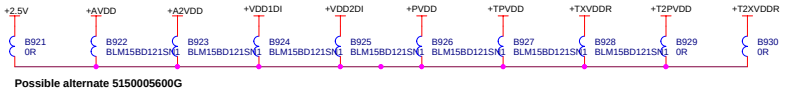
Supported footprint:
RT9173C/RT9199A/RT9199
APL5331











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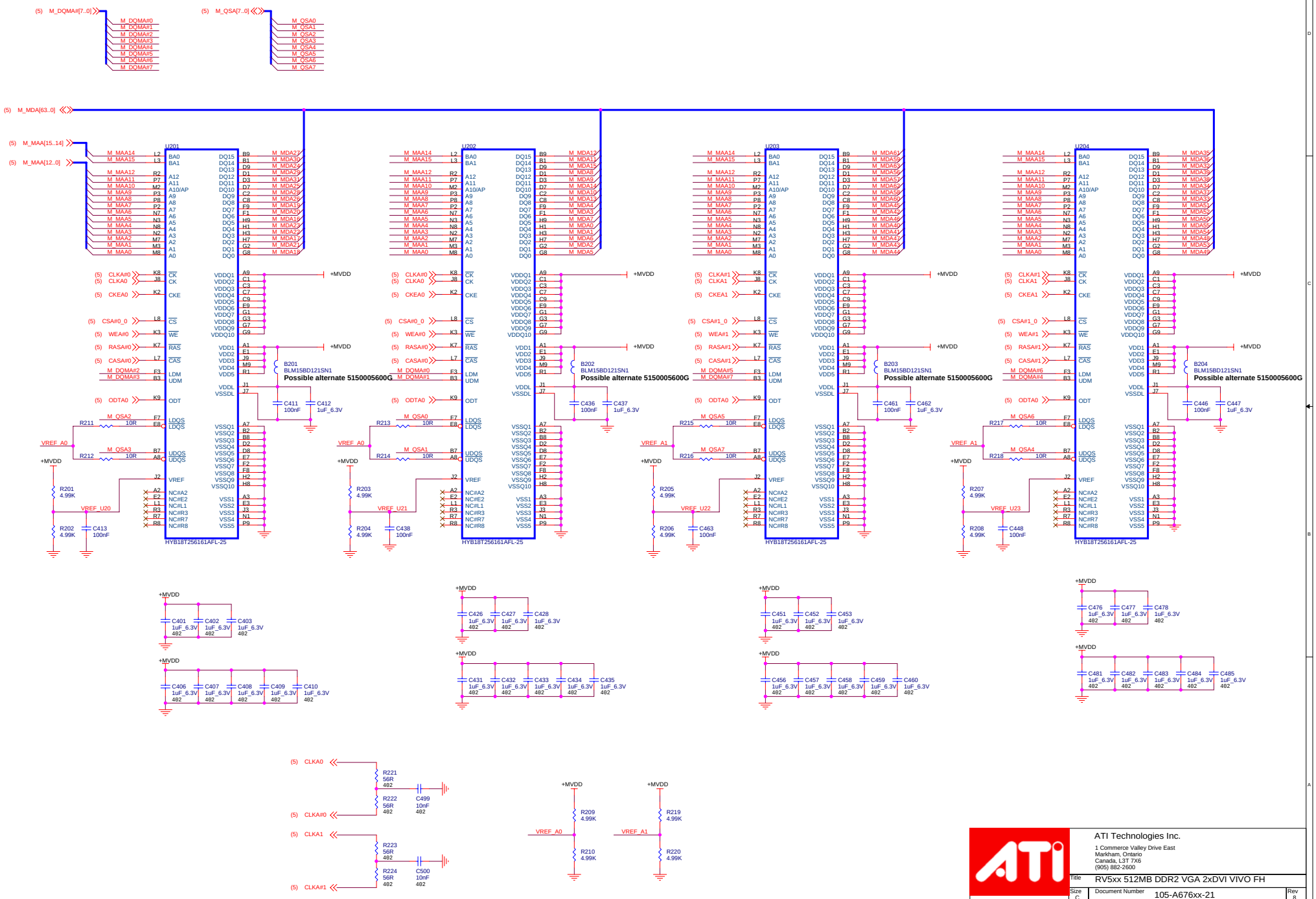
CHANNEL A: RANK 0 128MB DDR2



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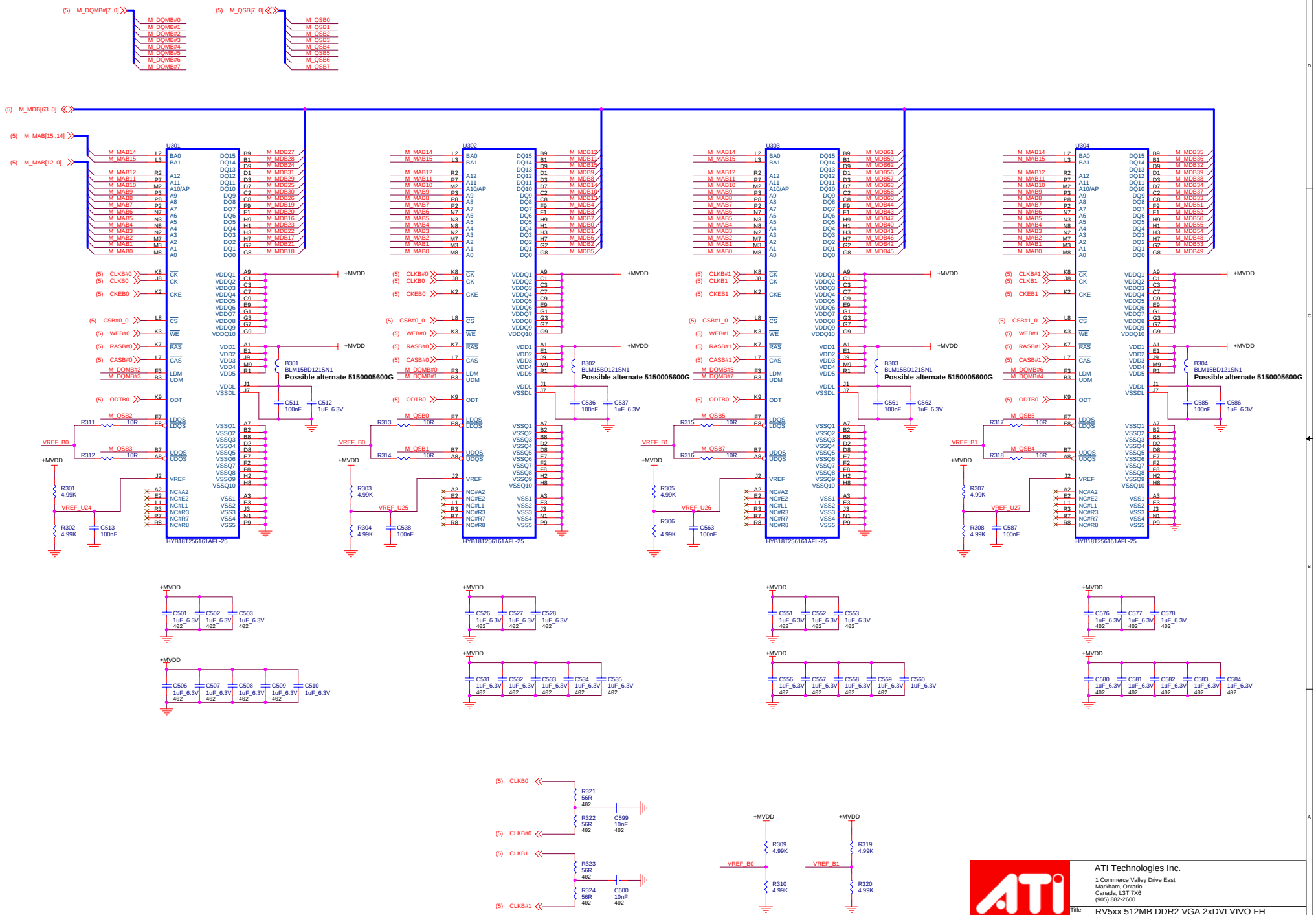
CHANNEL B: RANK 0 128MB DDR2



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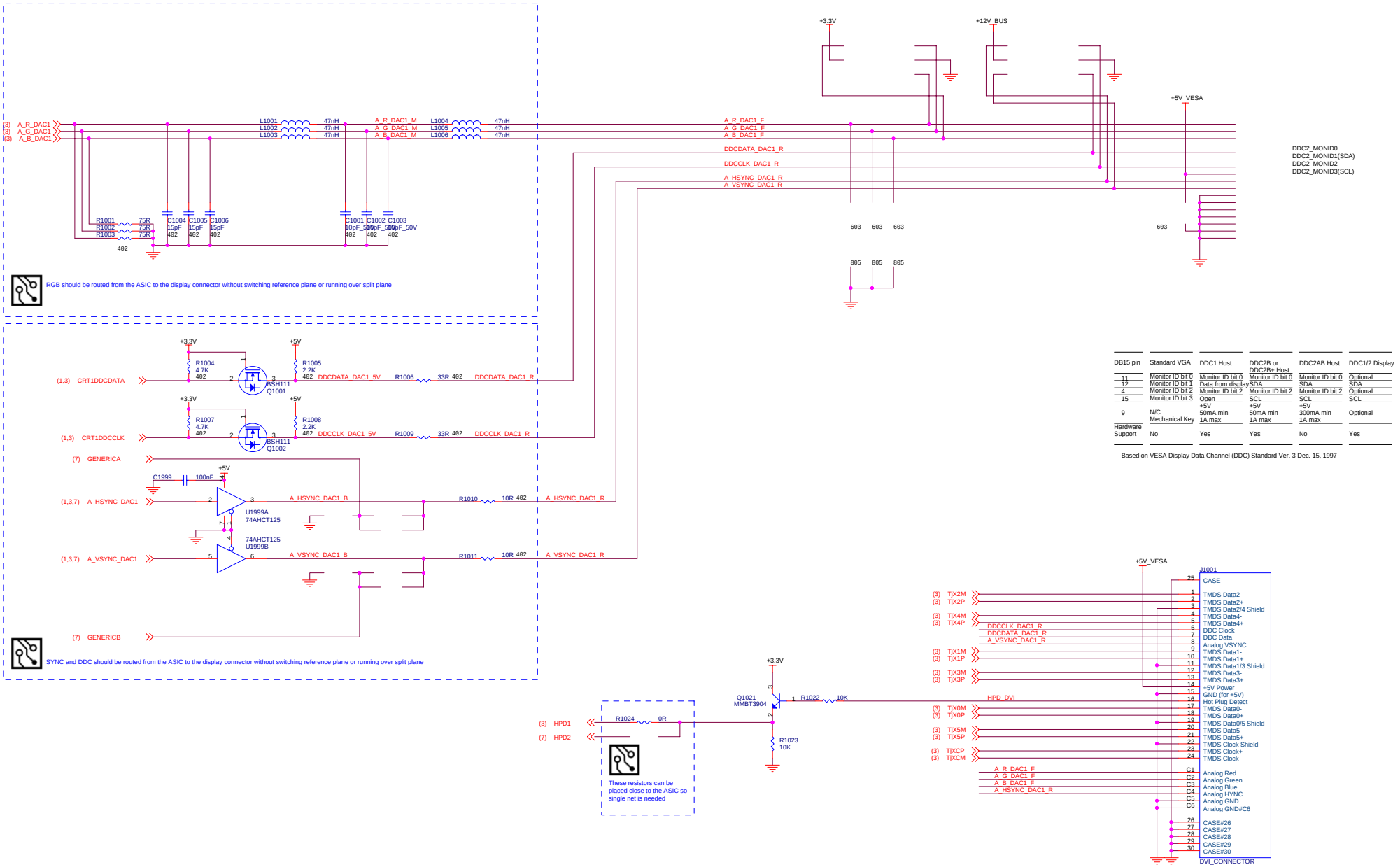

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Mechanical Key		1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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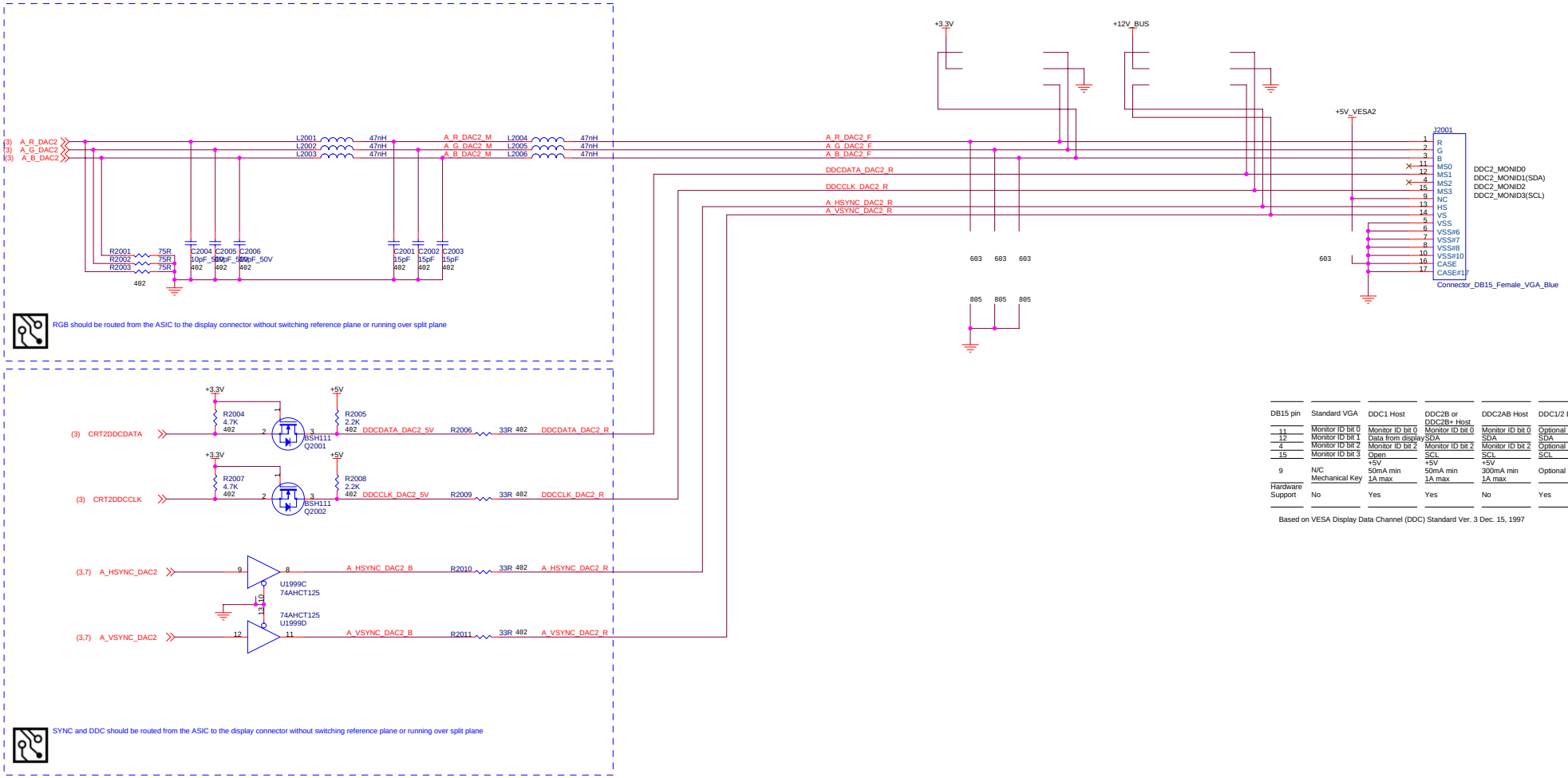

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	Mechanical Key	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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+RTAVDD
Vout = 3.3V
Iout = 125mA MAX, 80mA RMS

+12V_BUS
+RTAVDD
603
1%
402
+VDDC
These capacitors are for clossing references
+3.3V_BUS
Component (Y)
Component (Pr)
Component (Pb)
DAC2_Y_DIN
DAC2_C_DIN
DAC2_COMP_DIN
CompIn_R
CompIn
LumaIn_R
ChromaIn_R
LumaIn
ChromaIn
PIN6
Overlap with Rpin5
CompIn_R
1206
VADCFILTER
LumaIn_R
ChromaIn_R
As close as possible to pin 56 of Rage Theater
GND_VIN
NS3201
NS_VIA
(3) RTXTALIN
(3) RTXTALOUT
(1,2) PERST#_buf
5%
VIPCLK (7)
VPHCTL (7)
VHAD_0 (7)
VHAD_1 (7)
RTCLK (3)
VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
VID_7
Please close to RT
VID_[7..0] (7)
VPCLK0 (7)
Component (Y)
(3) DAC2_Y
L3001 470nH_250mA
DAC2_Y_F
R3001 75R
C3001 47pF_50V
C3004 47pF_50V
Component (Pr)
(3) DAC2_C
L3002 470nH_250mA
DAC2_C_F
R3002 75R
C3002 47pF_50V
C3005 47pF_50V
Component (Pb)
(3) DAC2_COMP
L3003 470nH_250mA
DAC2_COMP_F
R3003 75R
C3003 47pF_50V
C3006 47pF_50V
Install for Dell
R3011 0R
Install for Dell only when it's needed for EMI
Place near connector
0R leaves footprint for Ferrite Beads if req'd for EMI
Component (Y)
Component (Pr)
Component (Pb)
+3.3V
R3008 10K
Install for Dell
R3010 0R
DNI for Dell
(7) STV/HDTV#_OUT_DET
R3004 0R
R3005 0R
DNI for Dell
TV Out
J3001
HDTV_OUT_DET#
Y-OUT
C-OUT
Comp_out
SYNC
GND
GND#2
CASE
CASE#9
CASE#10
Rpin5
Conn_DIN_Mini_Circular_7_Pin_with_O_Ring

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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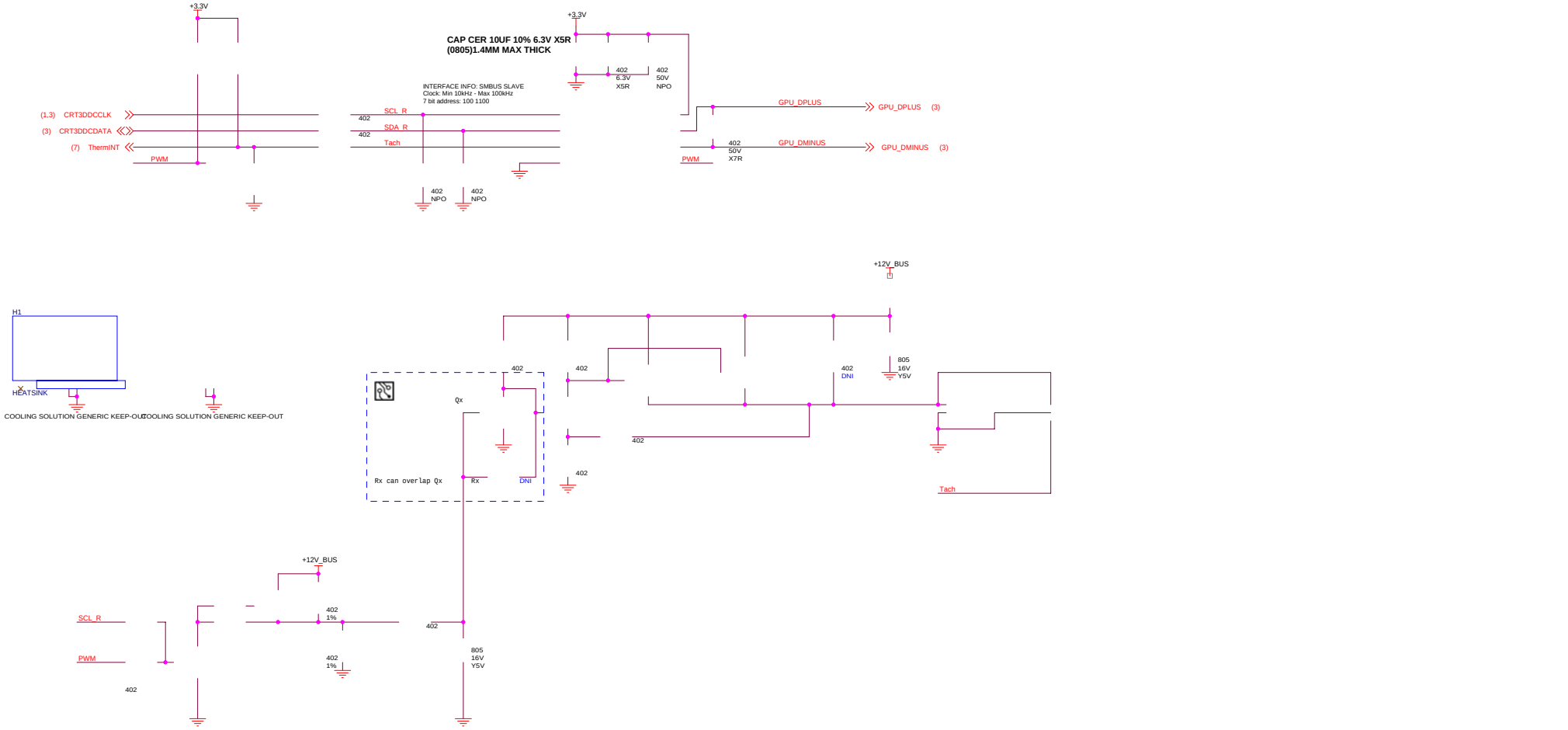

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DVI/VGA SCREWS

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

MT1
MT_Hole_0.136_in.
DNI

MT2
MT_Hole_0.136_in_6VIA
DNI

DNI

PCB1
109-A67631-30

<Variant Name>

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<variant Name>

Title

RV5xx 512MB DDR2 VGA 2xDVI VIVO FH

Schematic No.

105-A676xx-21

Date:

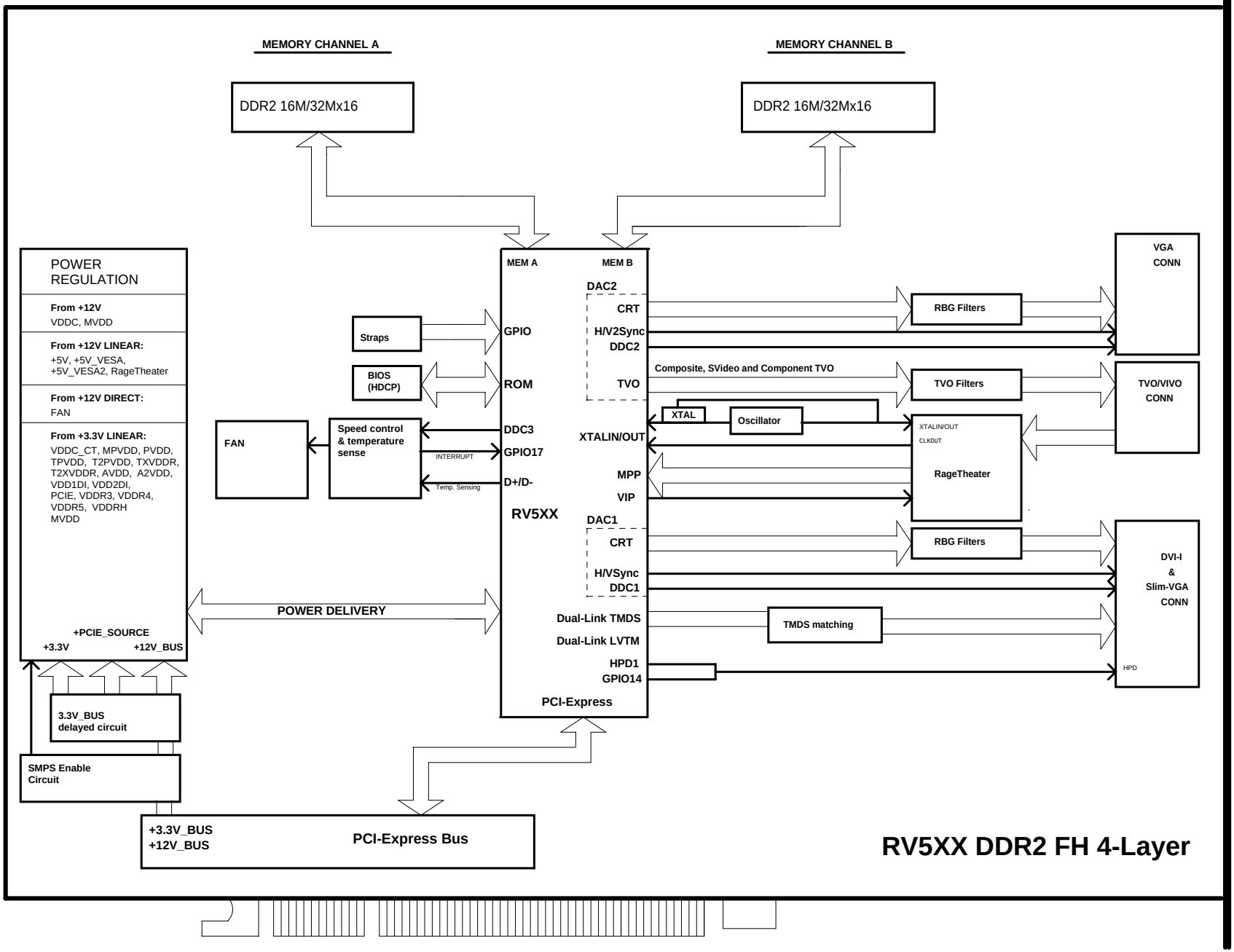
Thursday, May 11, 2006

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.

Rev 8

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	05/05/01	New design from scratch
1	00B	05/07/14	(Layout) Critical layout change (L1) Reduce +PW_MVDDC_M planes and replace it with GND (L1) Correct silkscreen "SMPS A601-00A TILE" (L3) Replace +PW_VDDC_M, +VDDC_S and +MVDDC_S planes with GND (pg 01) Correct clock circuitry to support RT (pg 08) Swap R603 and R604 to match layout for documentation purposes (pg 09) Swap R703 and R704 to match layout for documentation purposes (pg 10) Add MVDD linear regulator option (pg 11) Add R986, R987, R988; replace redundant power sequence circuit with +5V_EN and MVDD_EN (pg 11) Add MR911, R918 for +MPVDD for no-tracking option (pg 16) Change C3103 to 603 footprint, change RT to power from 3.3V_BUS to avoid leakage, remove redundant RT clock resistors
2	00C	05/07/29	(Layout) Critical layout change Add 2 to 3 more power vias for MOSFET source pin of VDDC (L3) Remove ground planes under the PWM IC Remove +MVDDC/+MVDDQ reference, use only +MVDD
3	00	05/08/24	(Layout) Move +PW_VDDC_HGDR trace on layer 3 slightly to avoid long overlap with VDDC_FB (pg 09) Add dynamic VDDC circuit for socket screening purposes (pg 11) Add MR961 for higher than 2.5V I/O voltage support (pg 14) Adding circuitry required for CrossFire ready
4	10	05/09/09	Moved VGA connector 1mm in to align with bracket
5	11	05/11/29	(Layout) Minor changes only. 1. A square pad fiducial has been added on the top side. 2. Mark for pin #1 for U3201 has been added 3. Lines have been added to define a minus polarity of the electrolytic caps
6	12	06/01/04	(Layout) Minor change only. Adding Microvision Certification Logo for TVO on the Silkscreen (pg 07) Updating the text description of PIN Straps DVALID & PSYNC to match MTAG definition for DDR2 memory.
7	20	06/02/20	(Layout) Increasing test point coverage (pg 07) Adding HDCP support (R36 and MR36) (pg 11) Adding C979 for power up sequencing (pg 14) Removing GPIO_9 connection to U1999 to eliminate conflict with HDCP, hardware CF support is no longer needed. (pg 16) Adding R3011, R3010, and C3010 to address new DIN connector pin assignment required by DELL (pg 17) Adding MQ4004 multi-footprint - Cost reduction (pg 17) Adding MR4027, MR4005, R4027, and Q4021 to provide option of running the fan at fixed voltage but lower than 12V
8	21	06/02/22	(pg 3) Removing MR139, MR140, MR141, MR142, MR143, MR144, MR145, MR146, MR147, MR148, MR149, MR150, MR151, MR152 , and disconnecting TMDS2 lines



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