

P262: NV44/G3-64, TSOP
MEMORY x16

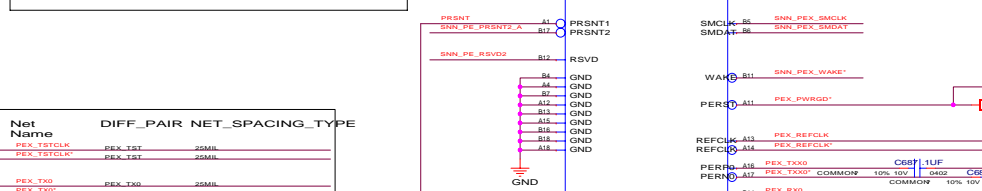
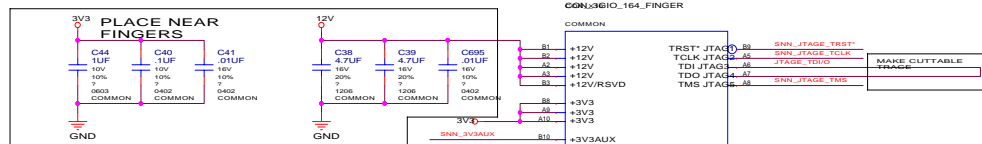
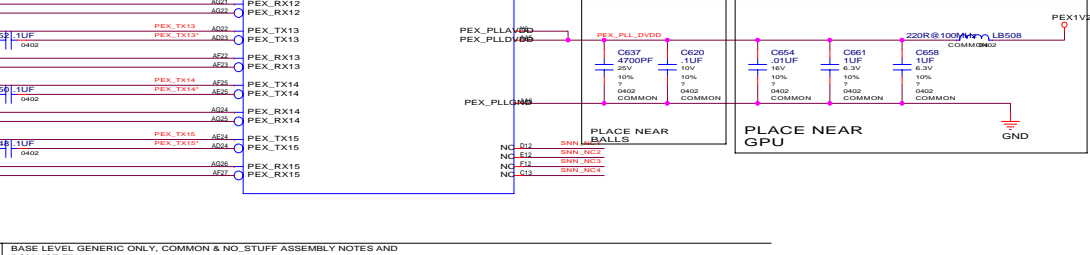
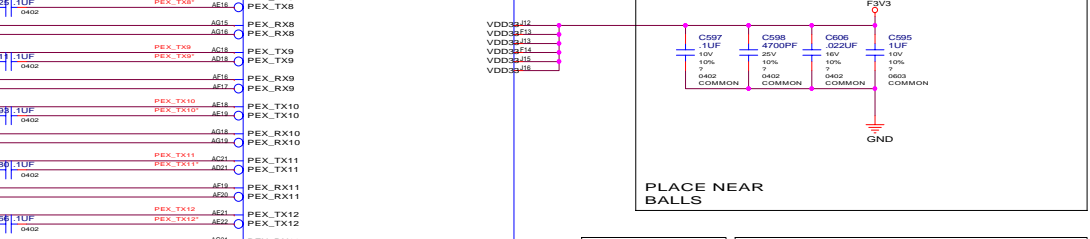
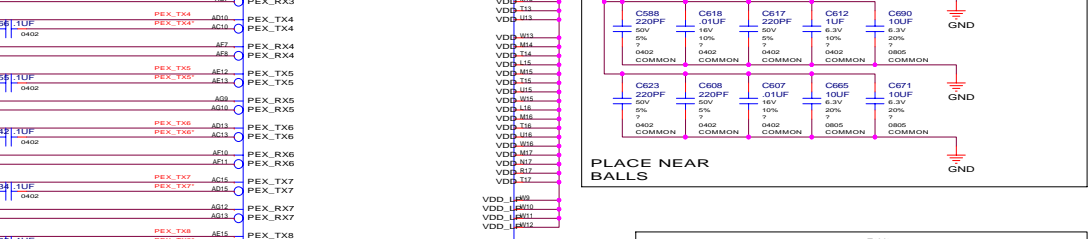
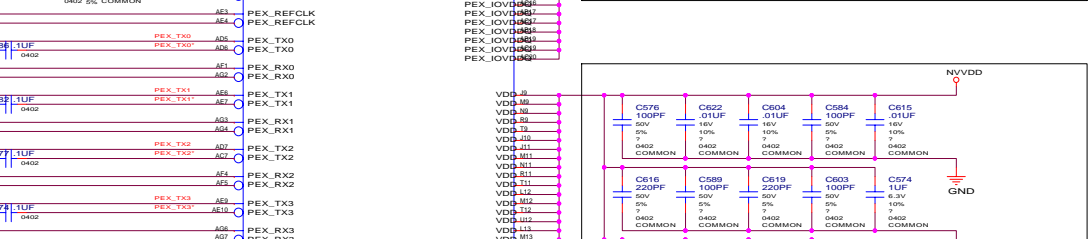
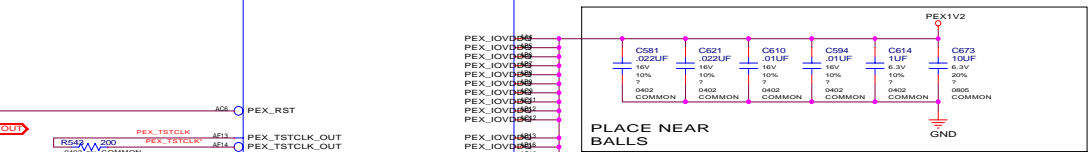
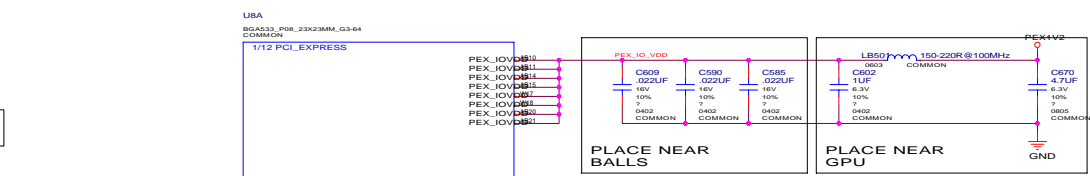
REV
HISTORY

A01

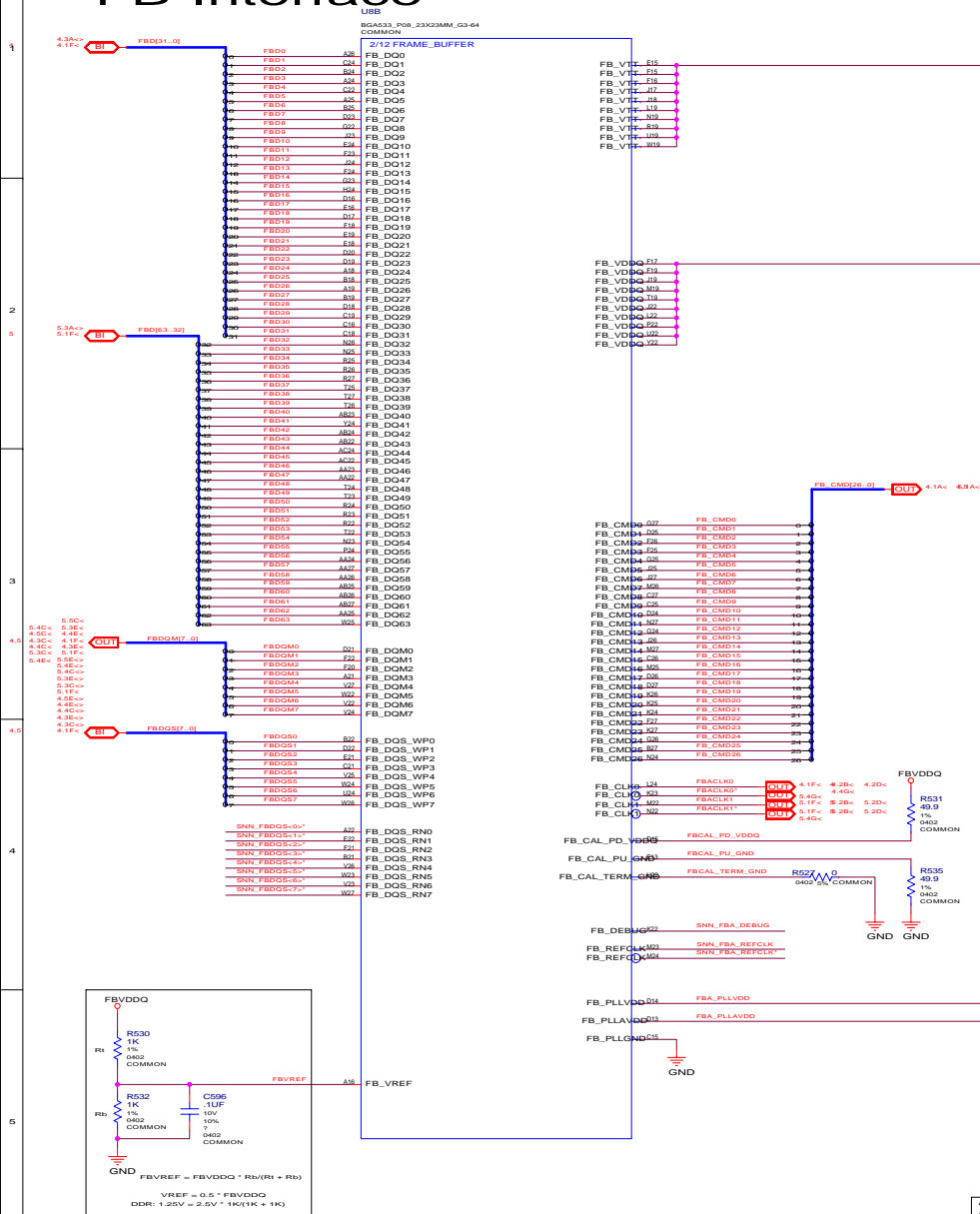
- 9/22/2004:
- Changed TMD5_PLLVDD to PLLVDD
 - Added bead option to PLLVDD rail of NV44
 - Changed RSET values for DACA and DACB
 - Changed DACA RSET FET to a dual package with GPIO11 control-Macrovision
 - Added F3V3 bypass to PLLVDD linear regulator
 - Changed location of R62

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10ppp-xxxx-ww	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
1	0000	600-10262-0000-000	UNREVIEWED FINAL
2	0001	600-10262-0001-000	<UNDEFINED>
3	0002	600-10262-0002-000	<UNDEFINED>
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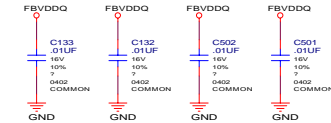
PEX-Interface

[illegible]

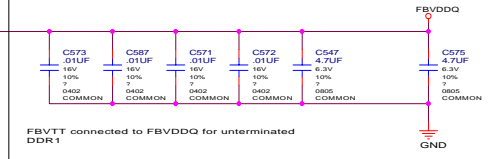
GPU: FB-Interface



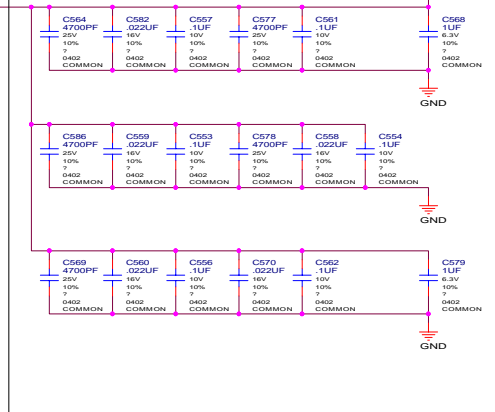
Net	NET_SPACING_RULE
IN FBAL_PU_GND	1.0MIL
IN FBAL_TERM_GND	1.0MIL
IN FB_DLVD	1.0MIL
IN FB_PFLVD	1.0MIL
IN FBVREF	1.0MIL

X-Caps for FB_CMD
BUS

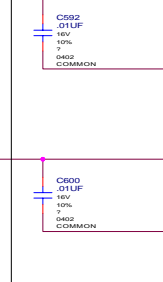
LABTESTPOINTS

PLACE NEAR
BGA

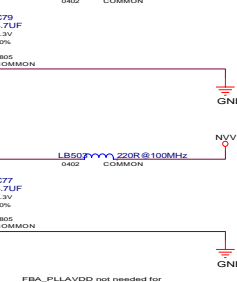
PLACE BELOW
GPU



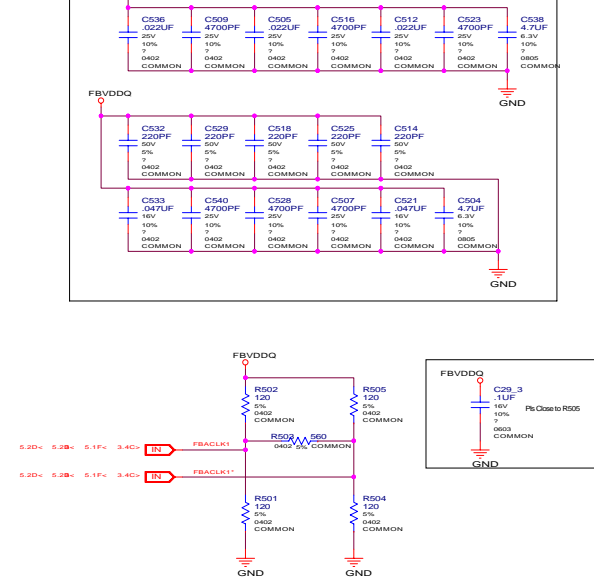
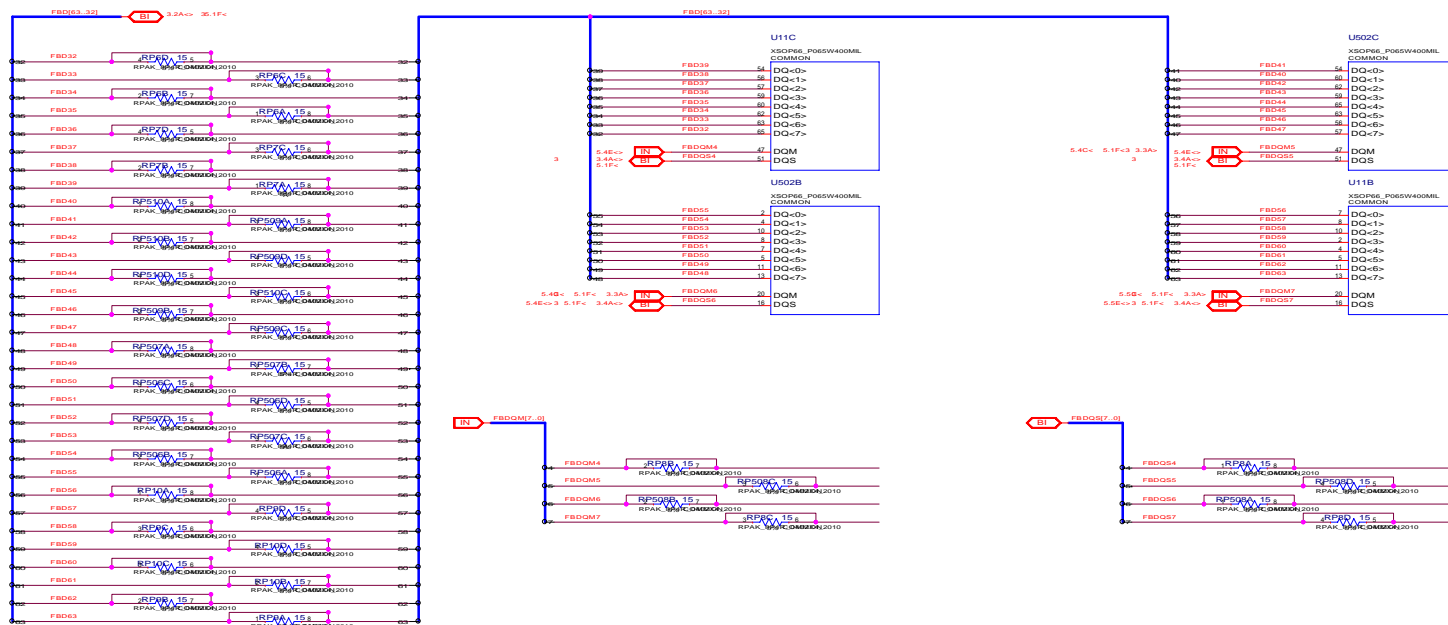
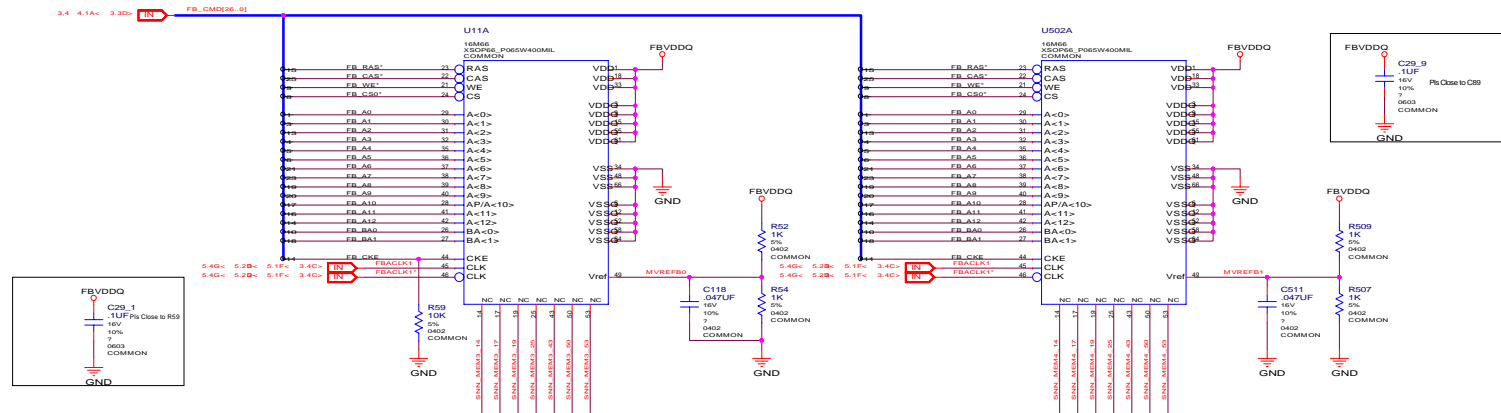
PLACE NEAR
BALLS



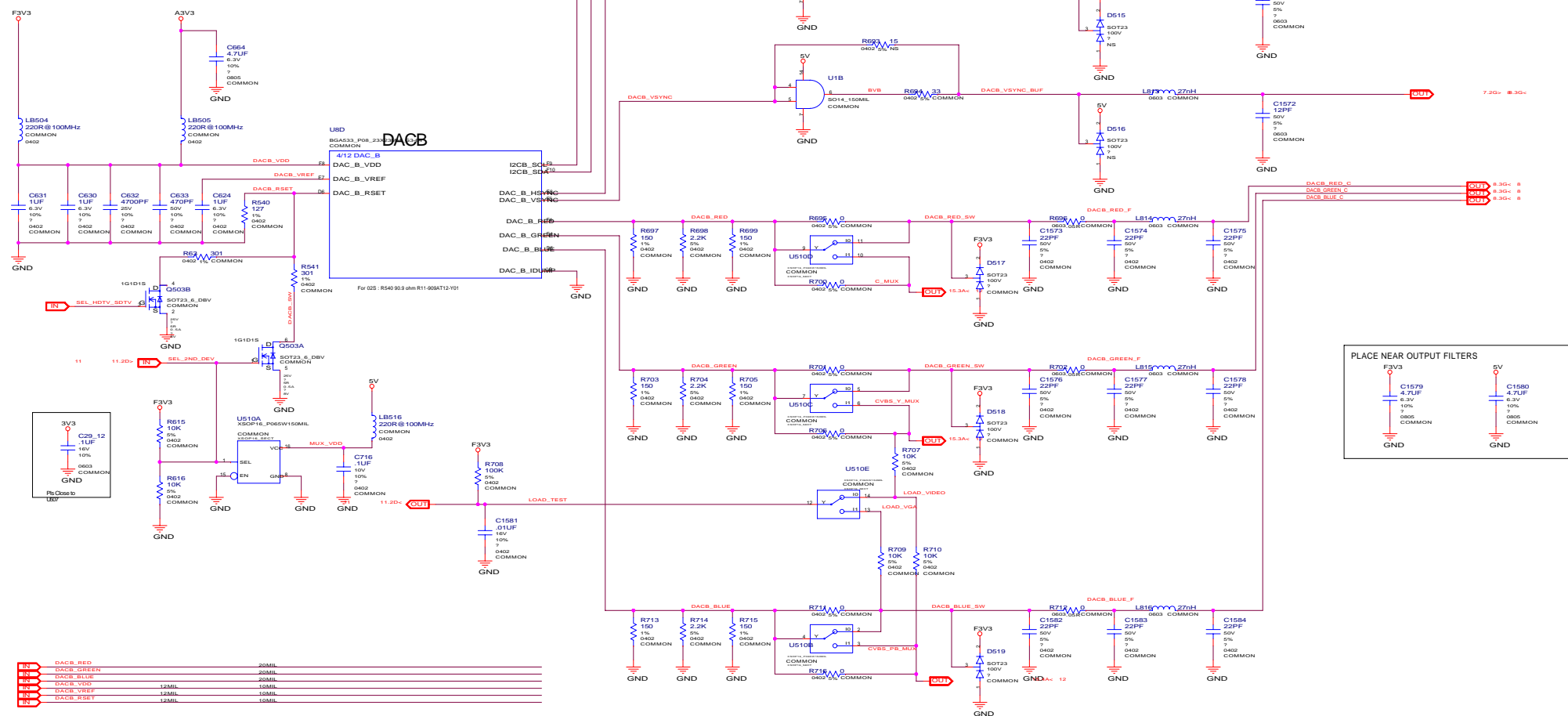
PLACE NEAR GPU



Memory Bit 32..63



	Net Name	Diffpair	NET_SPACING_RULE
IN	FBACKL1	FBACKL1	25MIL
IN	FBACKL1	FBACKL1	25MIL
IN	FBDSB7_321		10MIL
IN	FBDSB7_41		10MIL
IN	FBDSB7_41		10MIL

DAC-B, MUX,
DB15

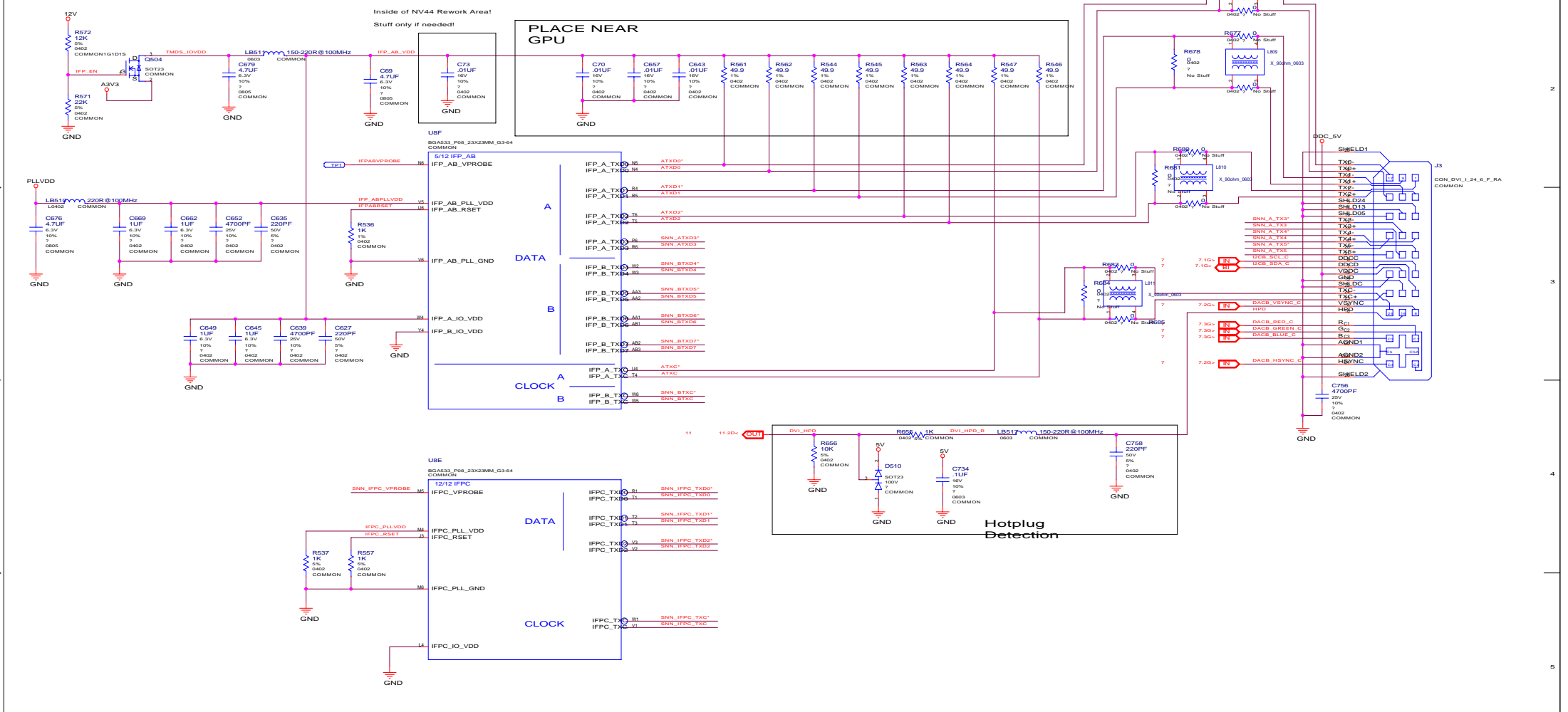
PLACE NEAR OUTPUT FILTERS

Two circuit diagrams illustrating the placement of output filters near the output:

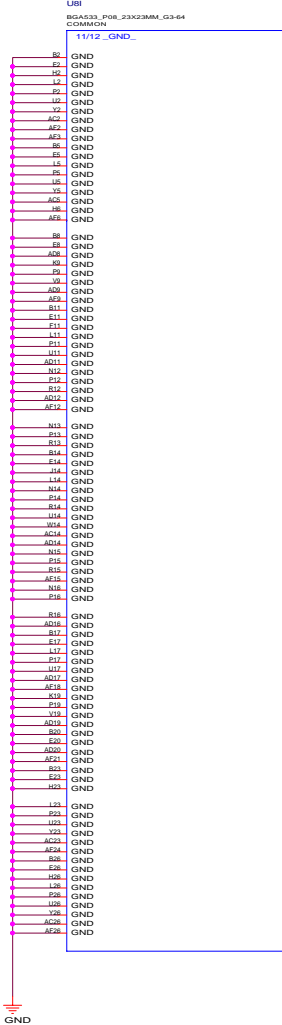
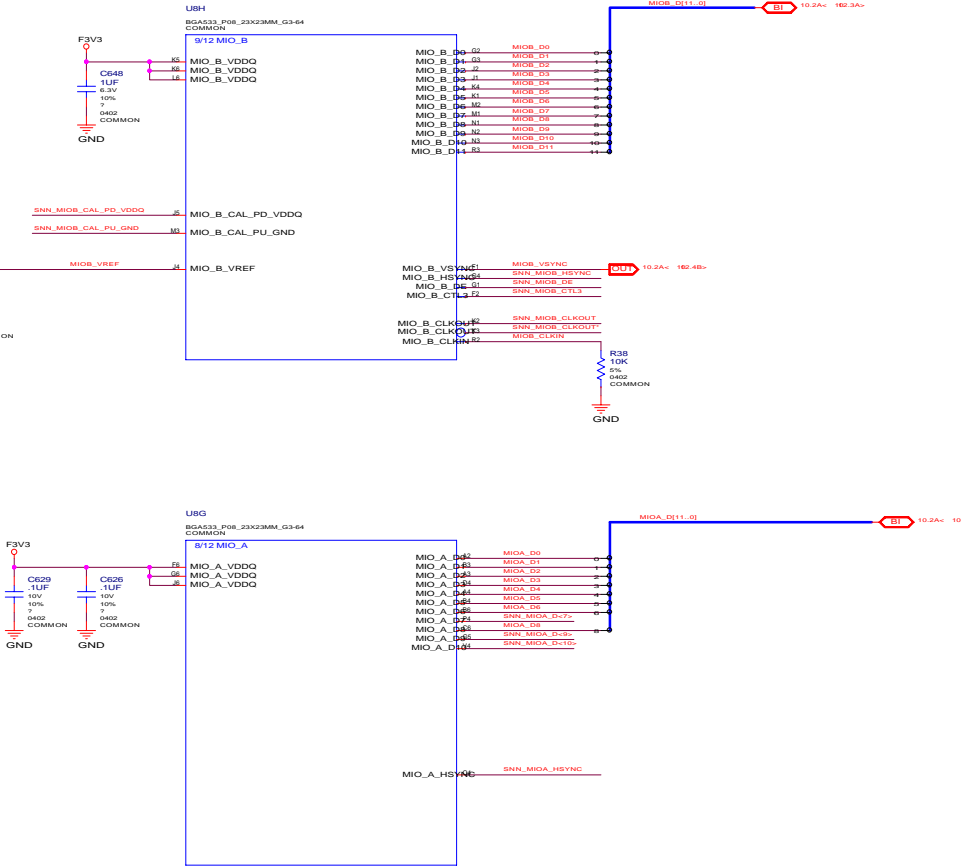
- Left Diagram:** A 3V3 input is connected to a capacitor C1579 (4.7uF). The capacitor is connected to a resistor (10% tolerance, marked 7) which is then connected to GND.
- Right Diagram:** A 5V input is connected to a capacitor C1580 (4.7uF). The capacitor is connected to a resistor (10% tolerance, marked 7) which is then connected to GND.

Internal TMD5, DVI-Connector

Net Name	Diffpair	NET_SPACING_RULE	voltage
IFP_AB_VDD			3.3V
ATX0	ATX0	25MIL	3.3V
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	



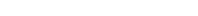
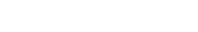
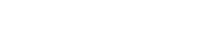
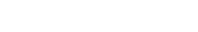
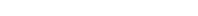
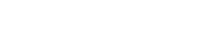
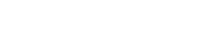
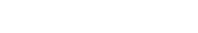
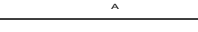
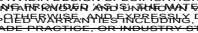
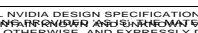
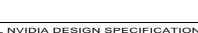
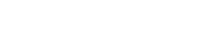
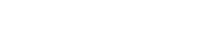
MIOA, MIOB
Interface,
LPC-ROM



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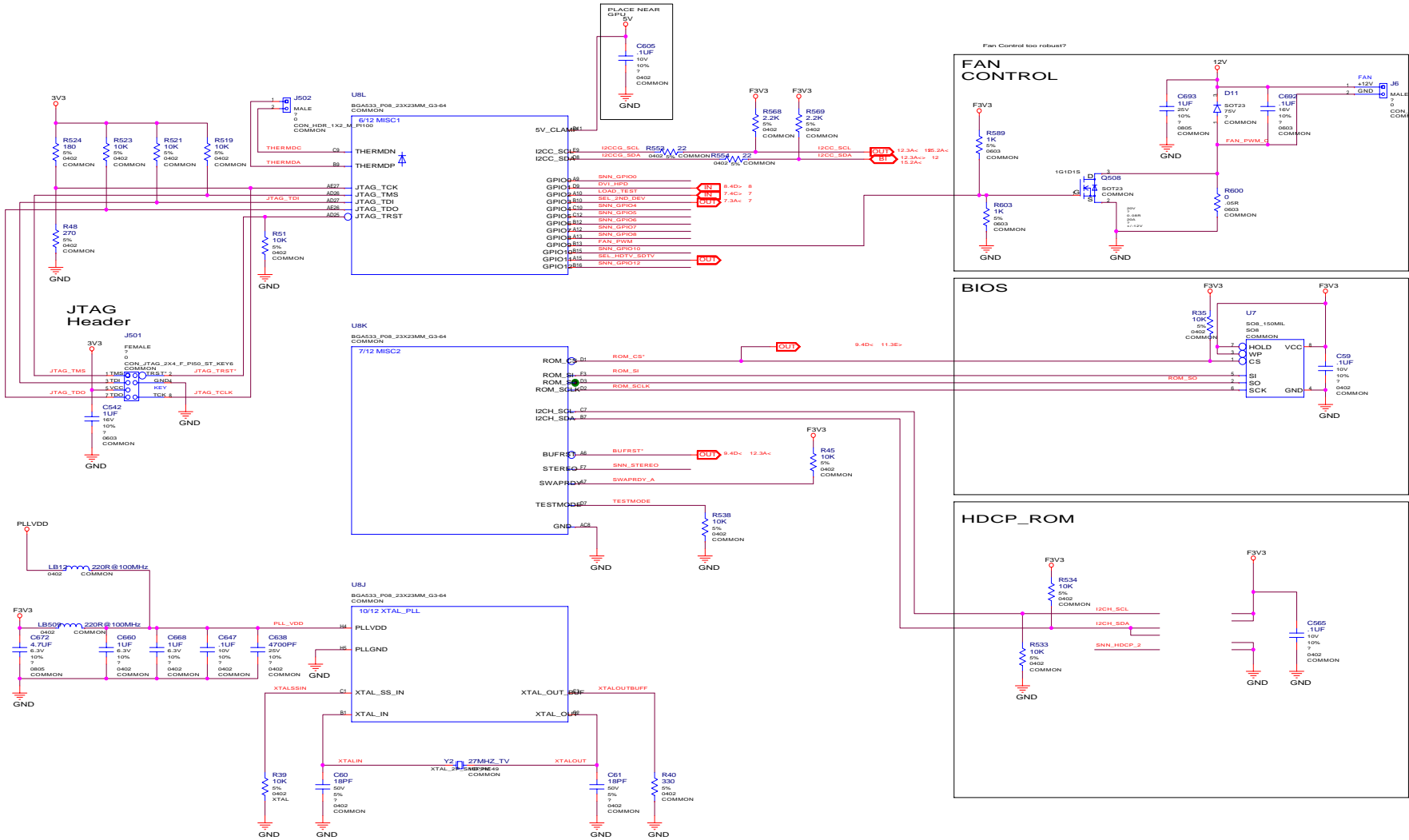
ASSEMBLY	LPC_ROM
PAGE	MIOA, MIOB Interface.

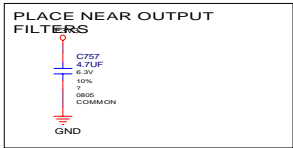
STRAPS, Mechanical Parts



XTAL, GPIO, BIOS, Fan Control, JTAG Headers

Net	Name	NET_PHYSICAL_TYPENET_SPACING_RULE
IN	XTALIN	5MIL TRACE
IN	XTALOUT	5MIL TRACE
IN	PLLVD	12MIL TRACE
IN	BIOS_FLVDD	12MIL TRACE





ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND
PAGE	FROM NOT FINAL
DETAIL	PRO CONNECTORS: MiniDIN, 2x6
	HCR

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A	B	C	D	E	F	G	H
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PowerSupplyII: 5V, DDC5V, A3V3, F3V3, TMDS_PLLVDD

