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AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: TOC

DATE: Tue Dec 09 14:00:57 2014 REV: 1.1

SHEET NUMBER: 1 OF 18

DOCUMENT NUMBER: 105-C93100-00A

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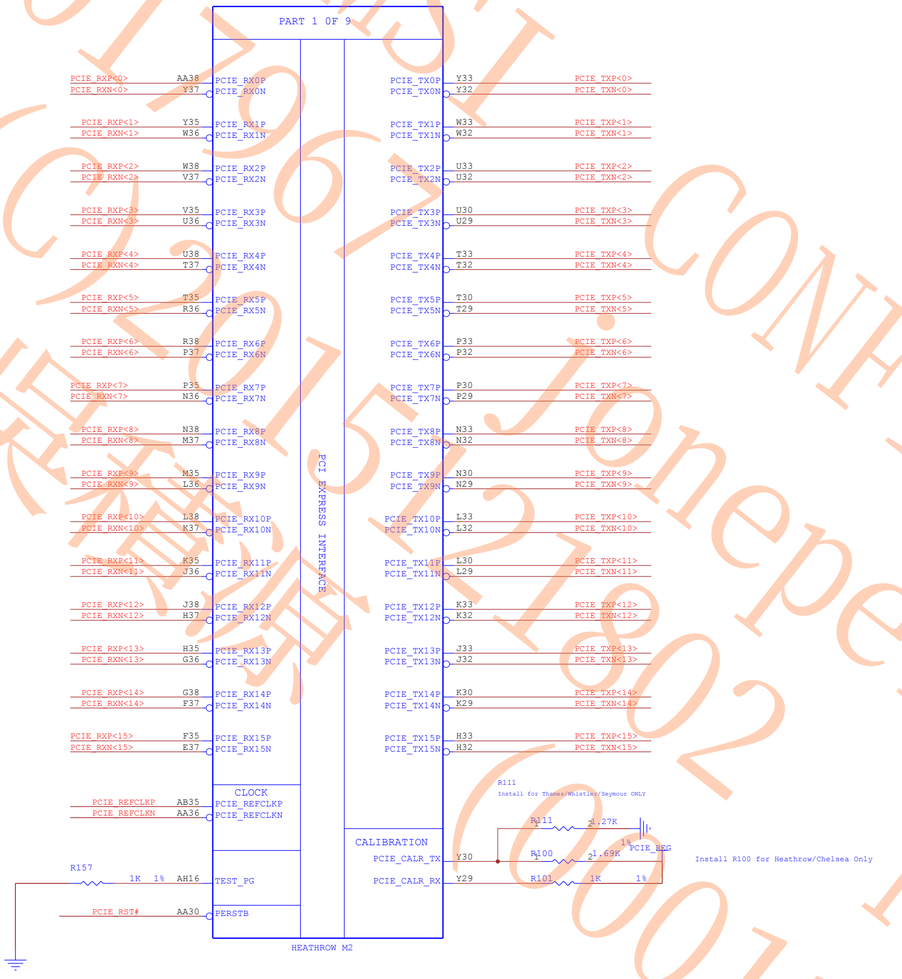
TITLE:

Tropo M2 GDDR5x32 MXM A



0001996 MSI CONFIDENTIAL
RD(C)2015121 Jonepei(裘完樂)
元智(0801802 RMA工程課(0001160

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: PCIE

DATE: Wed Dec 10 18:38:00 2014 REV: 1.1

SHEET NUMBER: 2 OF 18

DOCUMENT NUMBER: 105-C93100-00A

TITLE: Tropo M2 GDDR5x32 MXM A

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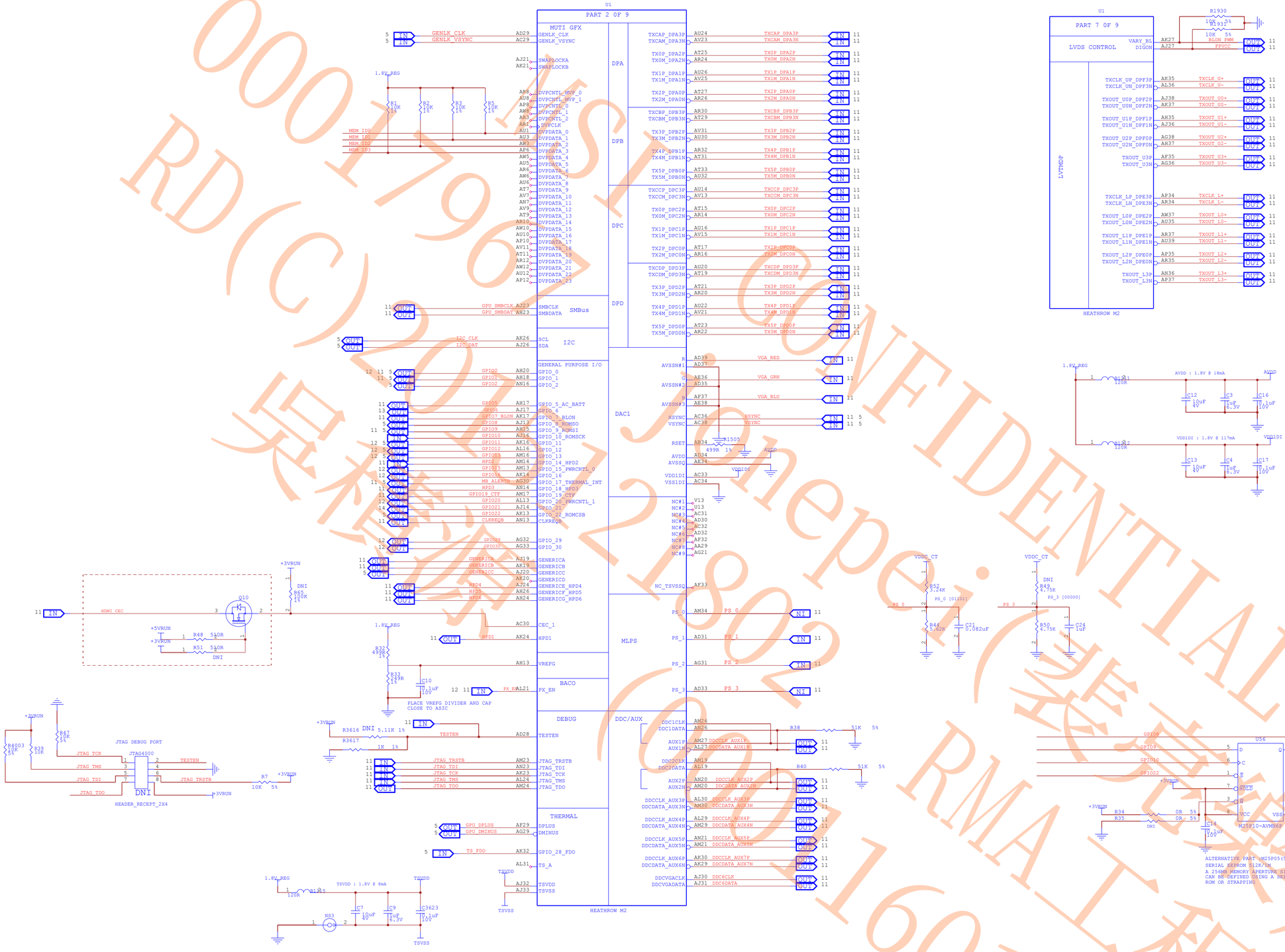

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Main

DATE: Wed Dec 10 18:38:00 2014 REV: 1.1

SHEET NUMBER: 3 OF 18

DOCUMENT NUMBER: 105-C93100-00A

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TITLE: Tropo M2 GDDR5x32 MXM A

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0001796 (2021-2-2 Jonepo 华硕(笔记本) RMA工程课)

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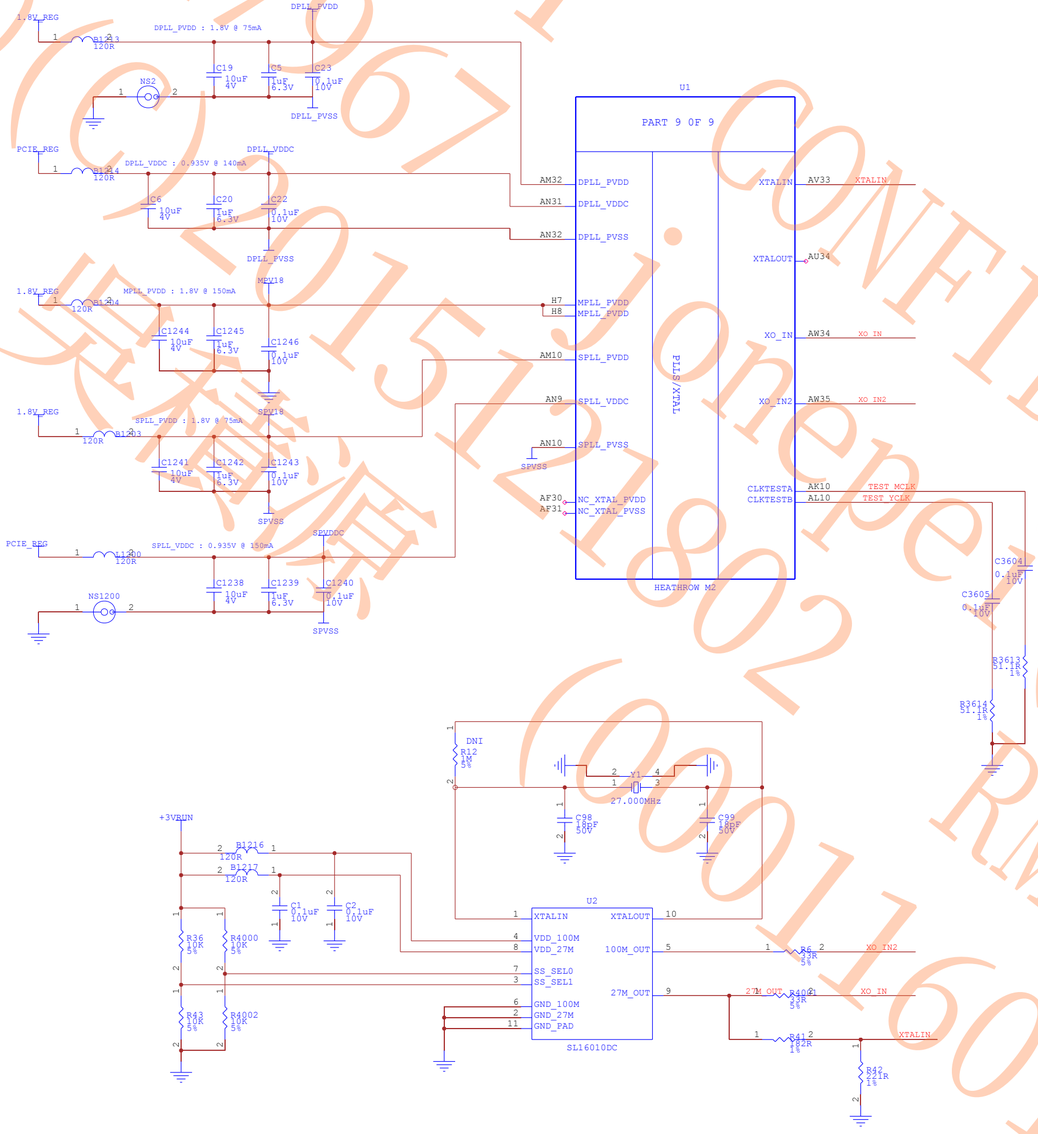
RD(C)2015121 Compal(裝完樂)
(0001601) RMA工程課



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: CLK	
DATE: Wed Dec 10 18:38:00 2014	REV: 1.1
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TITLE:
Tropo M2 GDDR5x32 MXM A

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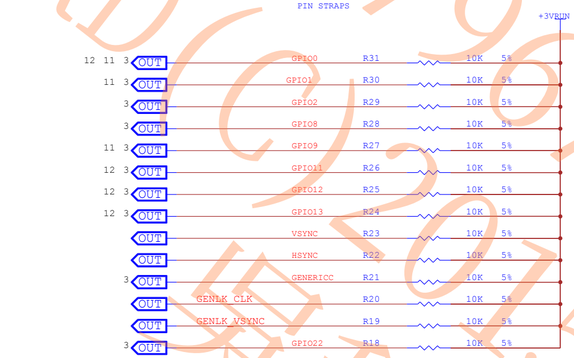
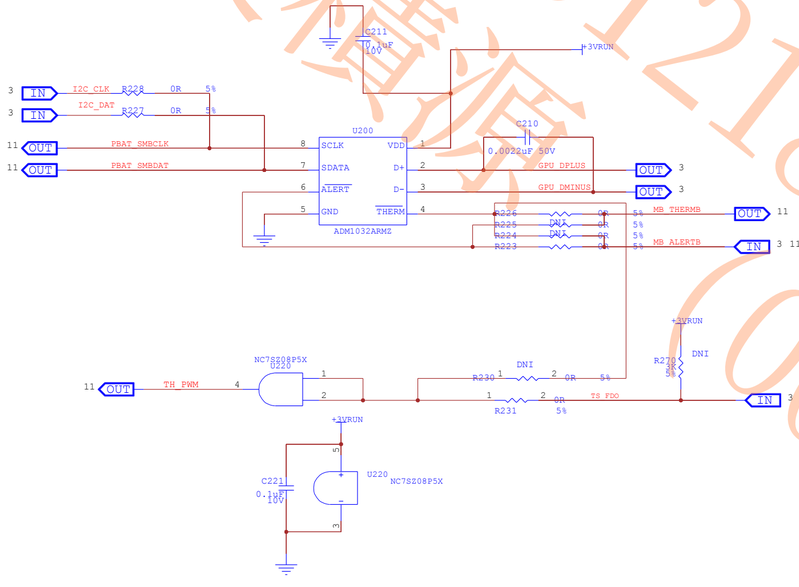
RD(C)2015121802 Jonepei(000116012 RMA工程樂)

PIN STRAPS





CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESET

STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED	PS_1[3]	GENLK_CLK	Reserved	0
RESERVED	PS_1[2]	GPIO6	Reserved	0
RESERVED	NA	GPIO21	Reserved	0
RESERVED	NA	GENERICC	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

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SHEET: Pin Straps

DATE: Wed Dec 10 18:38:00 2014 REV: 1.1

SHEET NUMBER: 5 OF 18

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TITLE:
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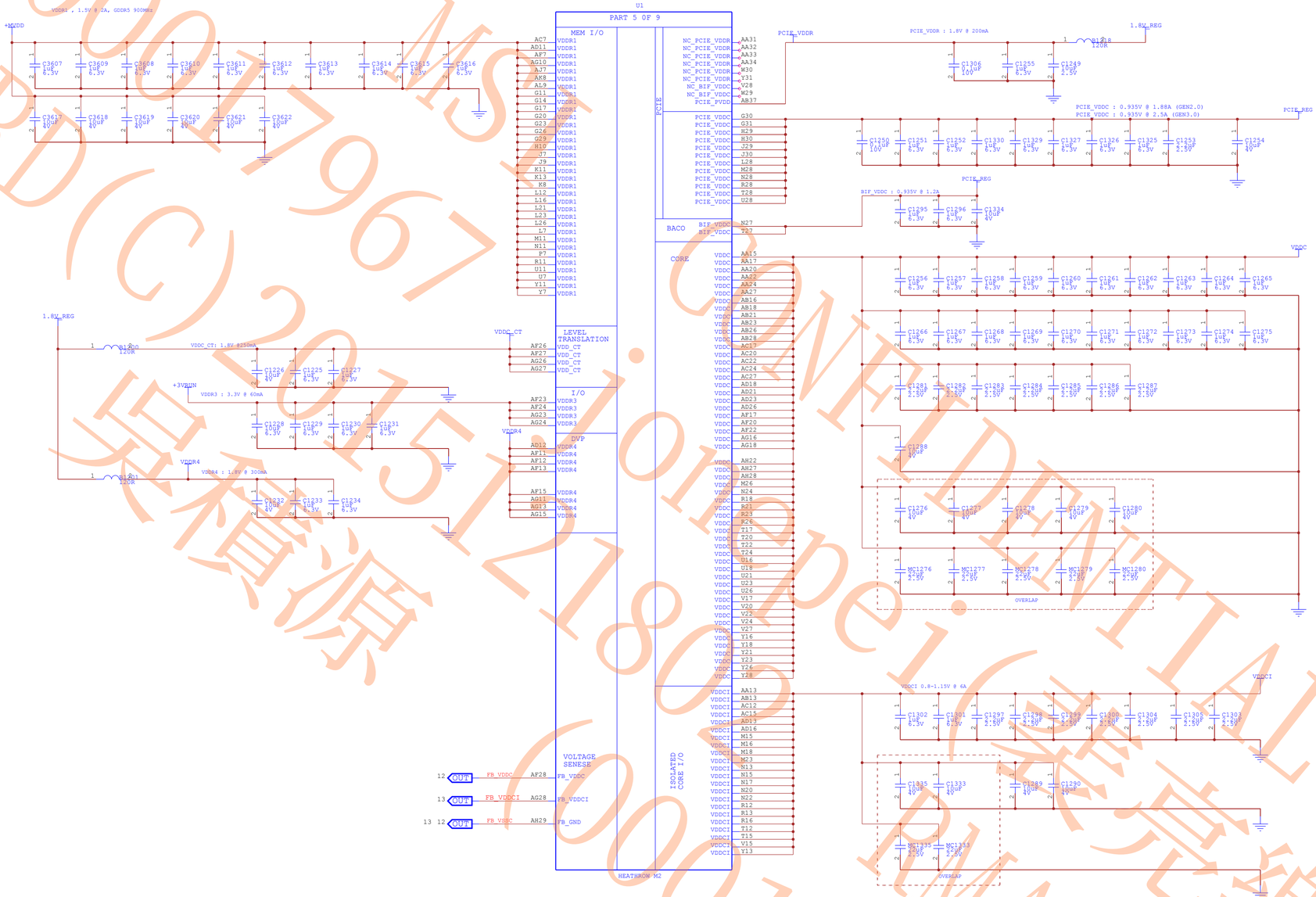

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SHEET: PWR	
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TITLE:
Tropo M2 GDDR5x32 MXM A

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RD(2015.10.1802 Taipei(緯創資通)
(00011601) RMA工程樣

DP/TMDS/LVDS Transmitter Power

DP mode: 1.8V@188mA per port
HDMI mode: 1.8V@237mA per port

1.8V_REG

C1319 10uF 4V
C1320 1uF 6.3V
C1321 0.1uF 10V
C1322 10uF 4V
C1323 1uF 6.3V
C1324 0.1uF 10V
C1312 10uF 4V
C1313 1uF 6.3V
C1314 0.1uF 10V

U1

PART 8 OF 9

DP_VDDR

AN24 AP24 AP25 AP26 AU28 AV29 AP20 AP21 AP22 AP23 AU18 AV19 AH34 AJ34 AE34 AG34 AM37 AL38 — DP_VDDR

DP_VDDC

DP_VDDC AP31 AP32 AN33 AP33
DP_VDDC AP12 AP13 AP14 AP15
DP_VDDC AL31 AM33 AK32 AK34

DP GND

DP_VSSR AN27 AP27 AP28 AM24 AM26 AM29 AP29 AP30 AM30 AM32 AN17 AP16 AP17 AM14 AM16 AN19 AP18 AP19 AM20 AM22 AN34 AP39 AR39 AU37 AF39 AH39 AN39 AL34 AV27 AR28 AV17 AR18 AN38 AM35 — DP_VSSR

CALIBRATION

R1700 1% 150R — AM28 DPAB_CALR
R1800 150R 1% — AM18 DPCD_CALR
R1900 150R 1% — AM39 DPEF_CALR

HEATHROW M2

DP/TMDS/LVDS Transmitter Power

0.935V@222mA per port

PCIE_REG

C1307 0.1uF 10V
C18 1uF 6.3V
C1311 10uF 4V
C1309 10uF 6.3V
C1310 1uF 6.3V
C1308 0.1uF 10V
C1317 0.1uF 10V
C1316 1uF 6.3V
C1315 10uF 4V

U1

PART 6 OF 9

PCIE_VSS

AB39 E39 F34 F39 G33 G34 H31 H34 H39 J31 J34 K31 K34 K39 L31 L34 M34 M39 N31 N34 P31 P34 P39 R34 T31 T34 T39 U31 U34 V34 V39 W31 W34 Y34 Y39

GND

P15 P17 P19 P21 P23 P25 P27 P29 P31 P33 F7 F9 G2 G6 H9 J2 J27 J6 J8 K14 K7 L11 L17 L2 L22 L24 L6 M17 M22 M24 N16 N18 N2 N21 N23 N26 N6 R15 R17 R2 R20 R22 R24 R27 R6 T11 T13 T16 T18 T21 T23 T26 U15 U17 U2 U20 U22 U24 U27 U6 V11 V16 V18 V21 V23 V26 W2 W6 Y15 Y17 Y20 Y22 Y24 Y27 — GND

A3 A37 AA16 AA18 AA2 AA21 AA23 AA26 AA28 AA6 AB12 AB15 AB17 AB20 AB22 AB24 AB27 AC11 AC13 AC16 AC18 AC2 AC21 AC23 AC26 AC28 AC6 AD15 AD17 AD20 AD22 AD24 AD27 AD9 AE2 AE6 AF10 AF16 AF18 AF21 AG17 AG2 AG20 AG22 AG6 AG9 AH21 AJ10 AJ11 AJ2 AJ28 AJ6 AK11 AK31 AK7 AL11 AL14 AL17 AL2 AL20 AL23 AL26 AL32 AL6 AL8 AM11 AM31 AM9 AN11 AN2 AN30 AN6 AN8 AP11 AP7 AP9 AR5 B11 B13 B15 B17 B19 B21 B23 B25 B27 B29 B31 B33 B7 B9 C1 C39 E35 E5 F11 F13 — GND

VSS_MECH A39 AM1 AW39

HEATHROW M2

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#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: DP-PWR

DATE: Wed Dec 10 18:38:01 2014 REV: 1.1

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TITLE:

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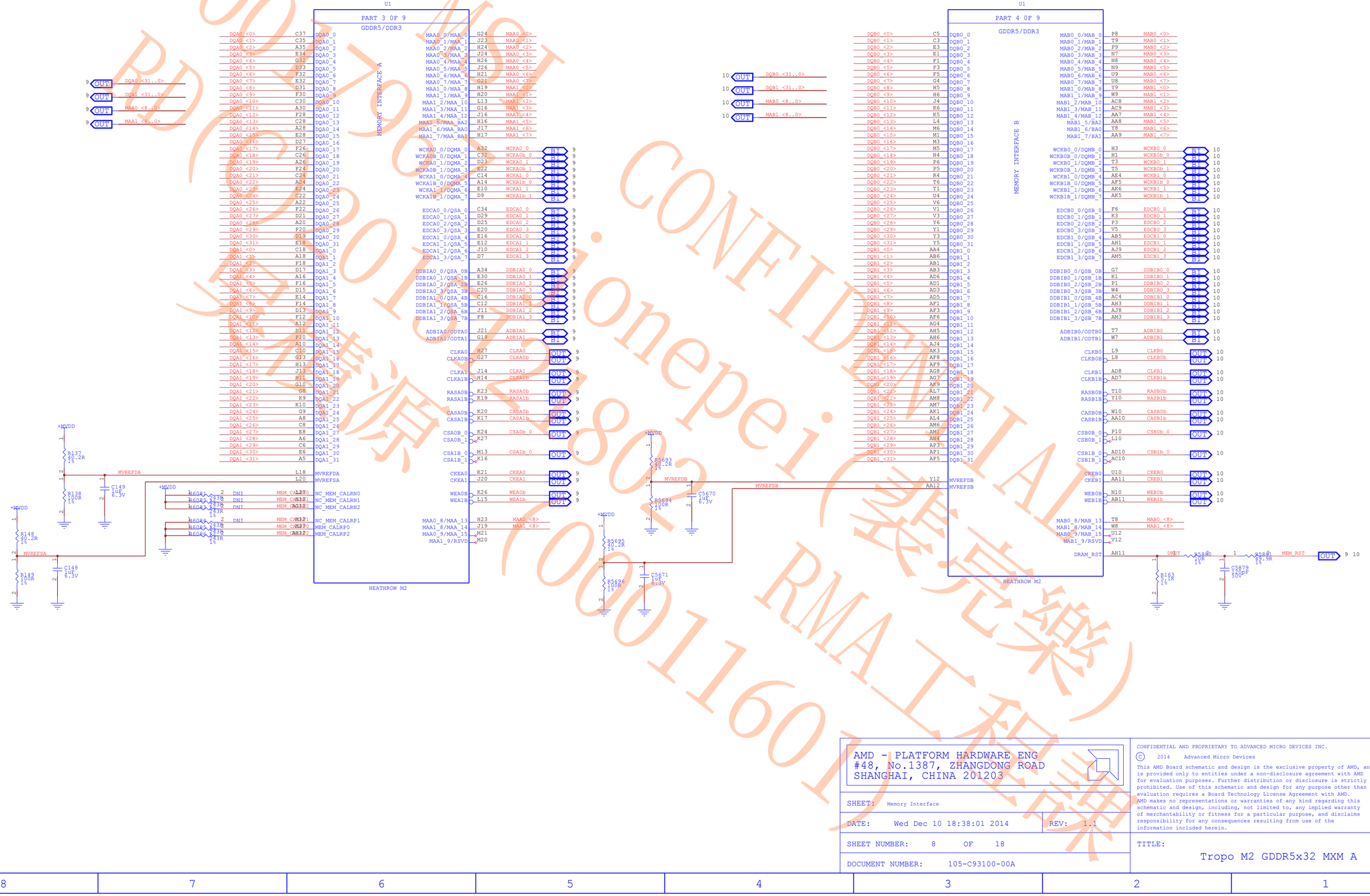

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#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Memory Interface

DATE: Wed Dec 10 18:38:01 2014 REV: 1.1

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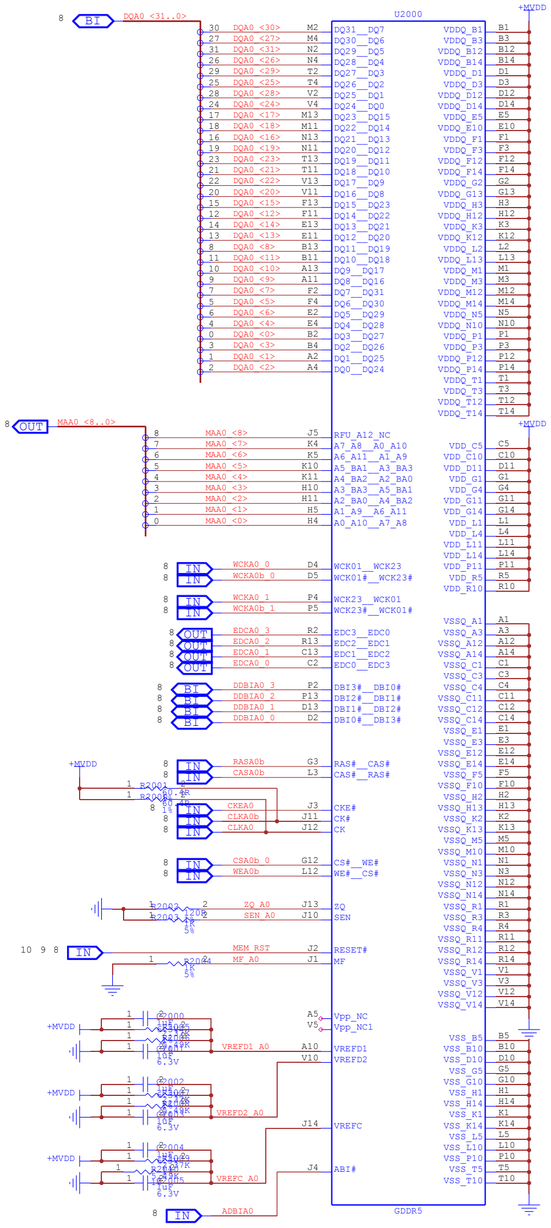
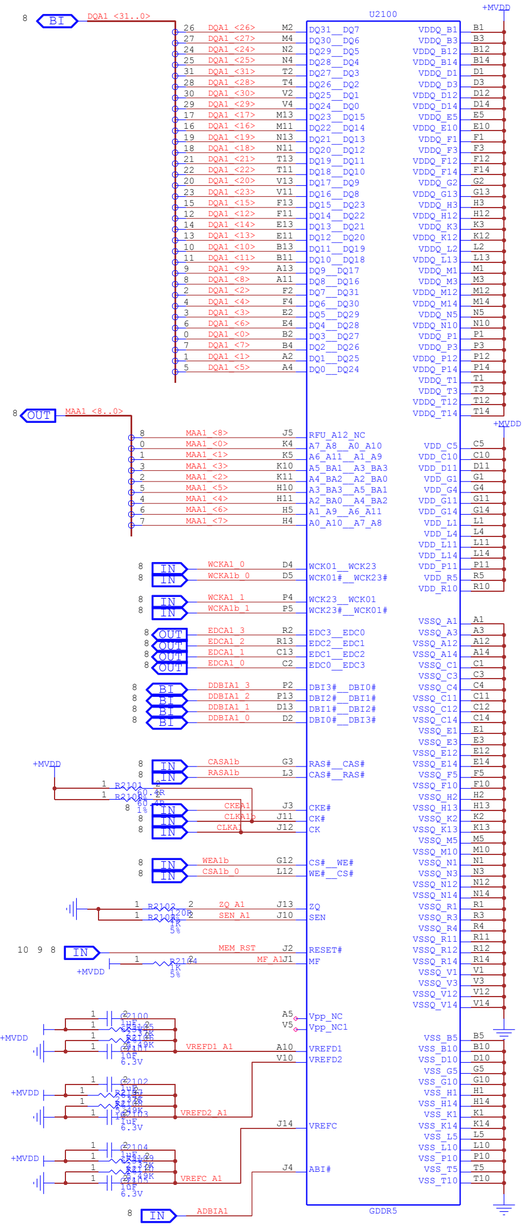
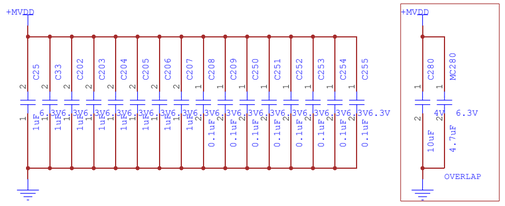
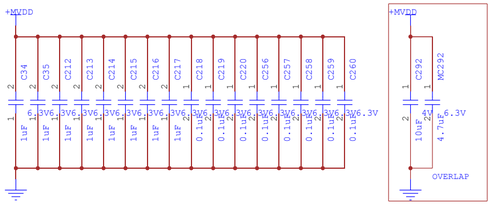
TITLE: Tropo M2 GDDR5x32 MXM A

000176961 MSI CONFIDENTIAL
RD2 0 0 1 0 2 0 2 0 onepei(裴完樂)
2006011601 RMA工程樂









DRAM SCAN PINS
SSH [J2] - SCAN SHIFT
SCK [G12] - SCAN CLOCK
SOUT [C2] - SCAN OUTPUT
SEN [J10] - SCAN ENABLE
SOE# [J1] - SCAN OUTPUT ENABLE

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SHEET: GDDR5_CHA

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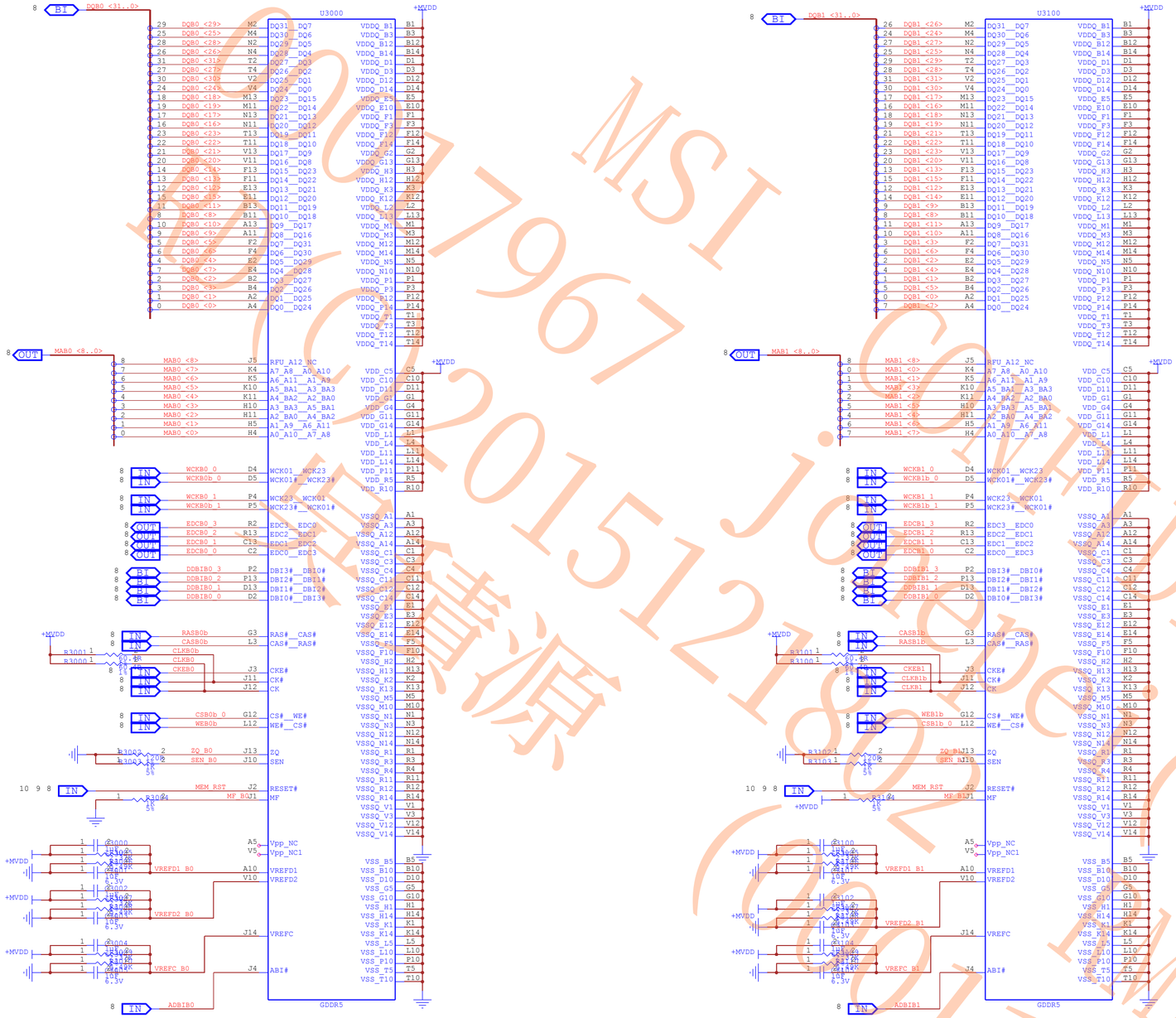

DRAM SCAN PINS
SSH [J2] - SCAN SHIFT
SCK [G12] - SCAN CLOCK
SOUT [C2] - SCAN OUTPUT
SEN [J10] - SCAN ENABLE
SOE# [J1] - SCAN OUTPUT ENABLE

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SHEET: GDDR5_CHB	
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PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE

STRAP OPTIONS FROM MOTHERBOARD DNI

PS_1 [11001]

PS_2 [00000]

J100 Part 1 of 2

J100 Part 2 of 2

Mechanical Key

NA

OPTION STRAPS

MXM3.0 specs asks for mandatory support of PWR_GOOD from module, but optional for motherboard to use it
For BACO designs where motherboards monitor PWR_GOOD: Do not install RB

For Non-BACO designs, or BACO designs where motherboards do not monitor PWR_GOOD: Do not install RB, Ra and Ca. Install RB.

Chose Ra and Ca values such that: the delay between PX_EN ramp-down to QB_B turn-on time is 25msec min

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TITLE: Tropo M2 GDDR5x32 MXM A

GPIO20	GPIO15	GPIO16	GPIO12	
VID4	VID3	VID2	VID1	VDDC
0	0	0	0	1.100V
0	0	0	1	1.075V
0	0	1	0	1.050V
0	0	1	1	1.025V
0	1	0	0	1.000V
0	1	0	1	0.975V
0	1	1	0	0.950V
1	1	1	1	0.925V
1	0	0	0	0.900V
1	0	0	1	0.875V
1	0	1	0	0.850V
1	0	1	1	0.825V
1	1	0	0	0.800V

GPU CORE REG

CORE PWM THREE PHASE REGULATOR 0.8V- 1.10V @ 40A

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0017967 jonepei
RD(C)20151218
(000116011)

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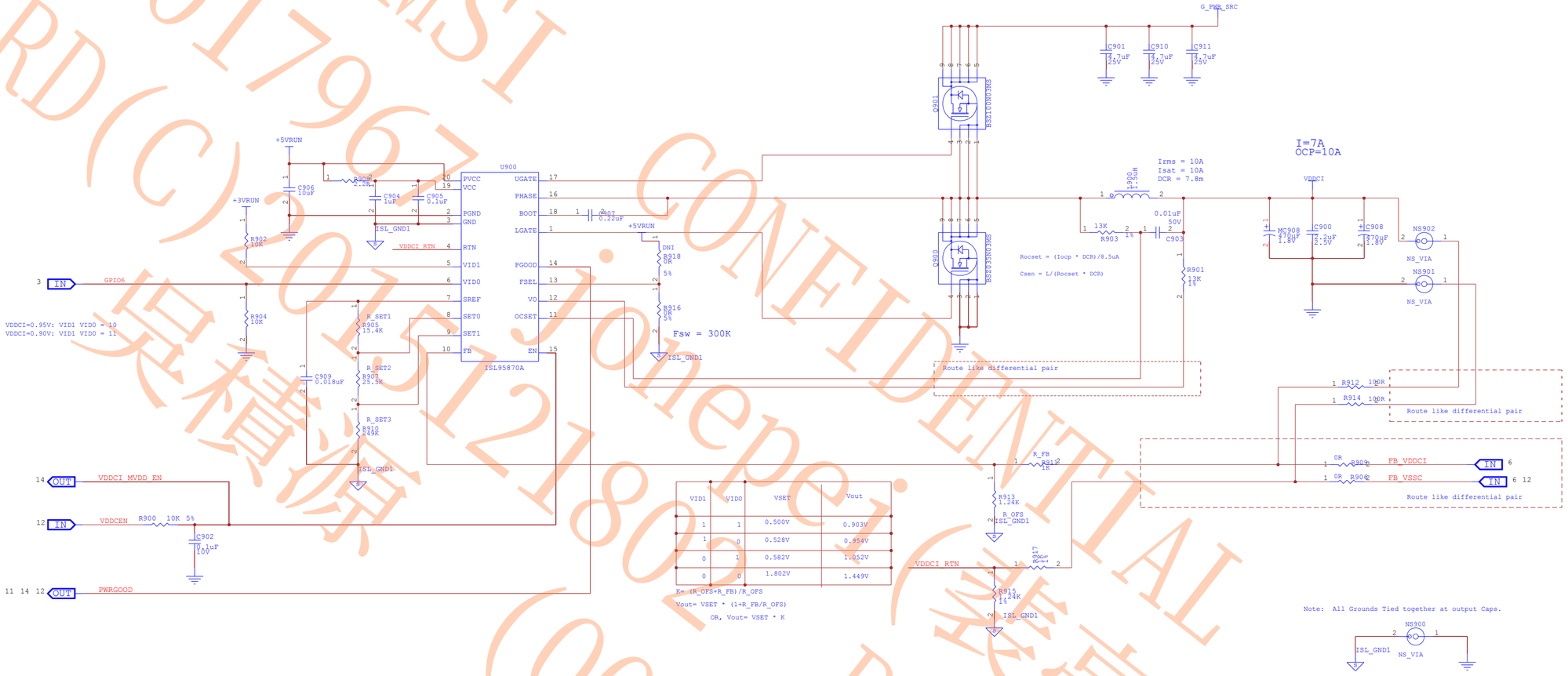
SHEET NUMBER: 12 OF 18	TITLE: Tropo M2 GDDR5x32 MXM A
DOCUMENT NUMBER: 105-C93100-00A	
NOTES: NOTE	



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SHEET: VDDCI	
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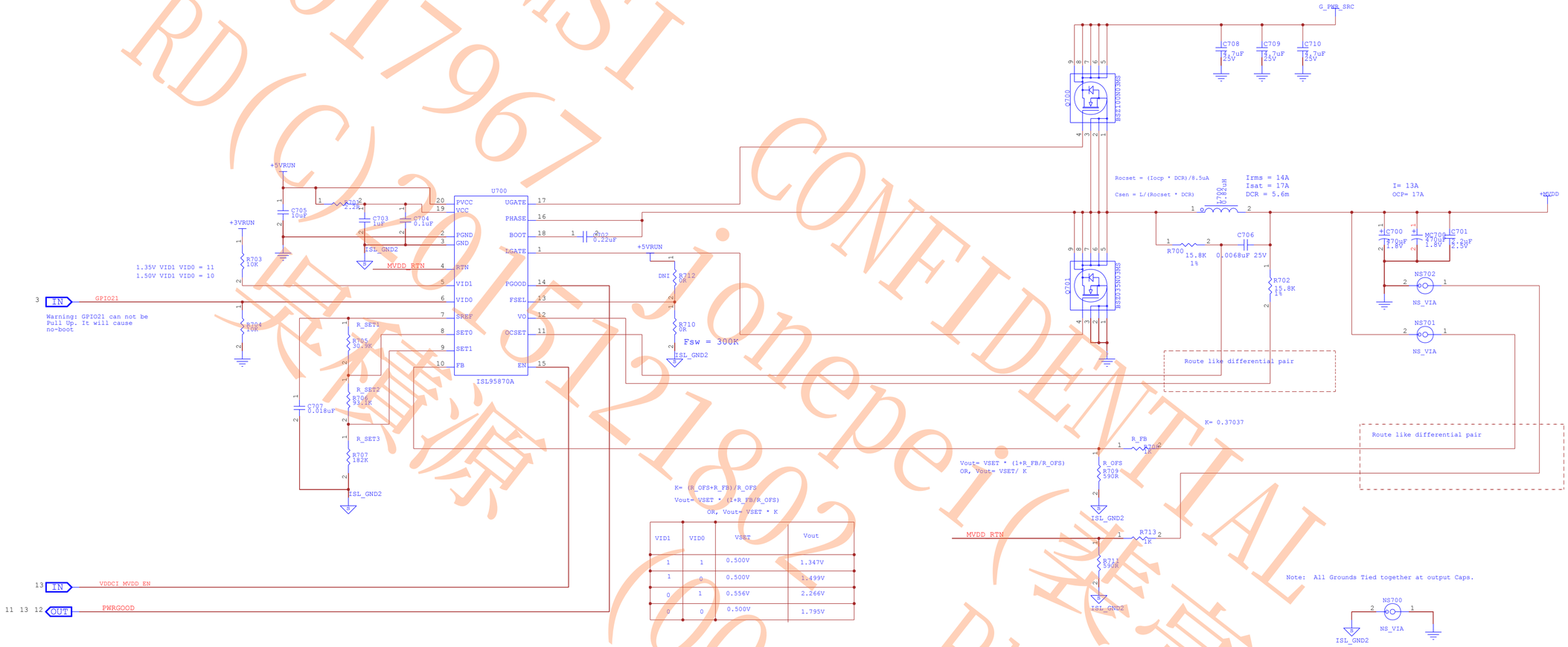
(樂完美)



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SHEET: MVDD

DATE: Wed Dec 10 18:38:02 2014 REV: 1.1

SHEET NUMBER: 14 OF 18

DOCUMENT NUMBER: 105-C93100-00A

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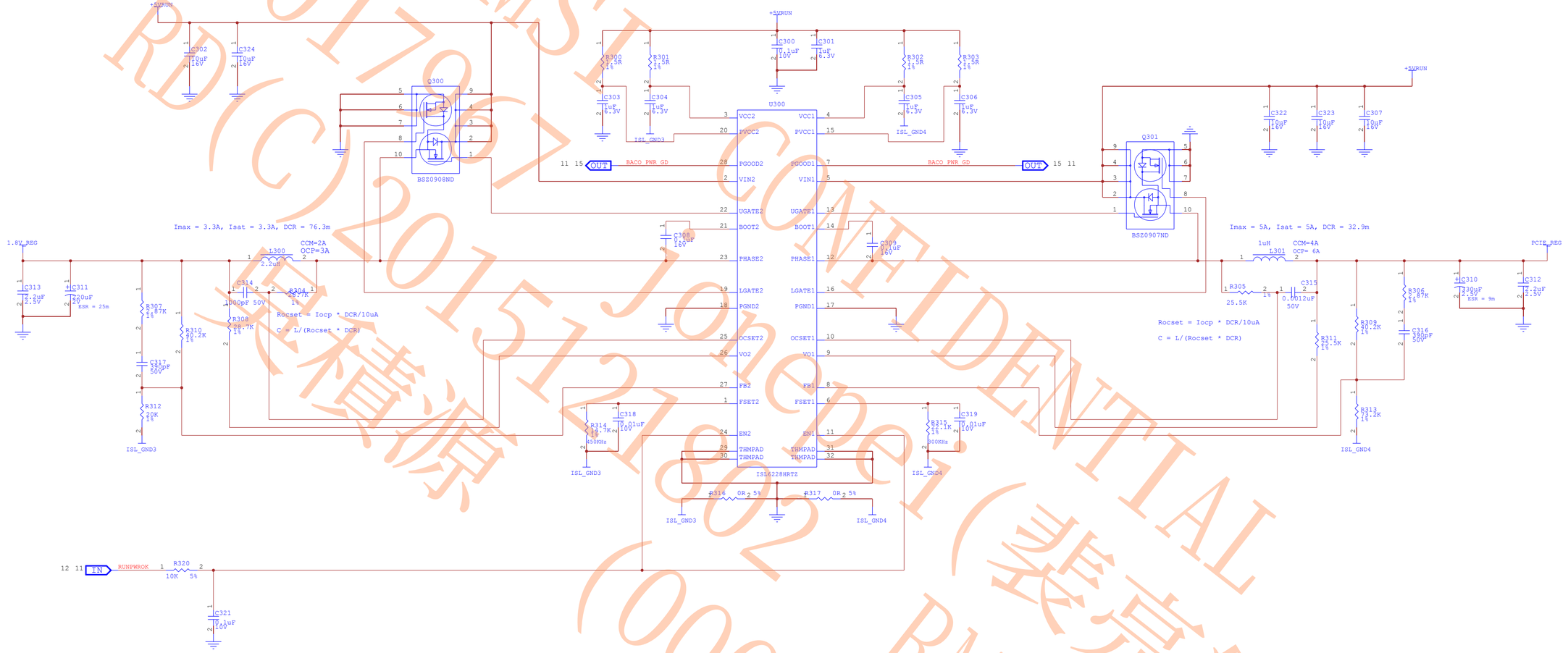

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SHEET: 1.8V&PCIE	
DATE: Wed Dec 10 18:38:02 2014	REV: 1.1
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NOTES: NOTE	

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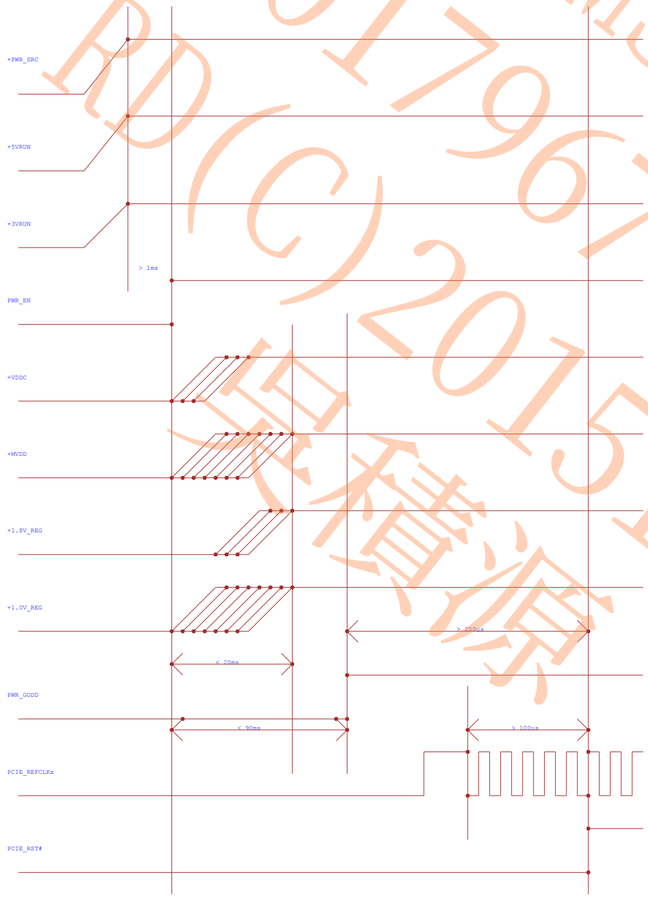
POWER UP SEQUENCE

(not to scale)



VDDR3

VDDC, VDDCI

VDDR1, MVDDQ/C

VDD_CT, VDDR4, TSVDD, PCIE_VDDR, PCIE_PVDD, DPLL_PVDD, DPx_PVDD, DPx_VDD18, MPV18, SPV18, AVDD, VDD1DI

+VDDC and +1.8V_REG ramp up can be swapped.

PCIE_VDDC, DPLL_VDDC, DPx_VDD10, SPV10

All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

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SHEET: Power Up Sequence

DATE: Tue Dec 09 14:01:23 2014

REV: 1.1

SHEET NUMBER: 16 OF 18

DOCUMENT NUMBER: 105-C93100-00A

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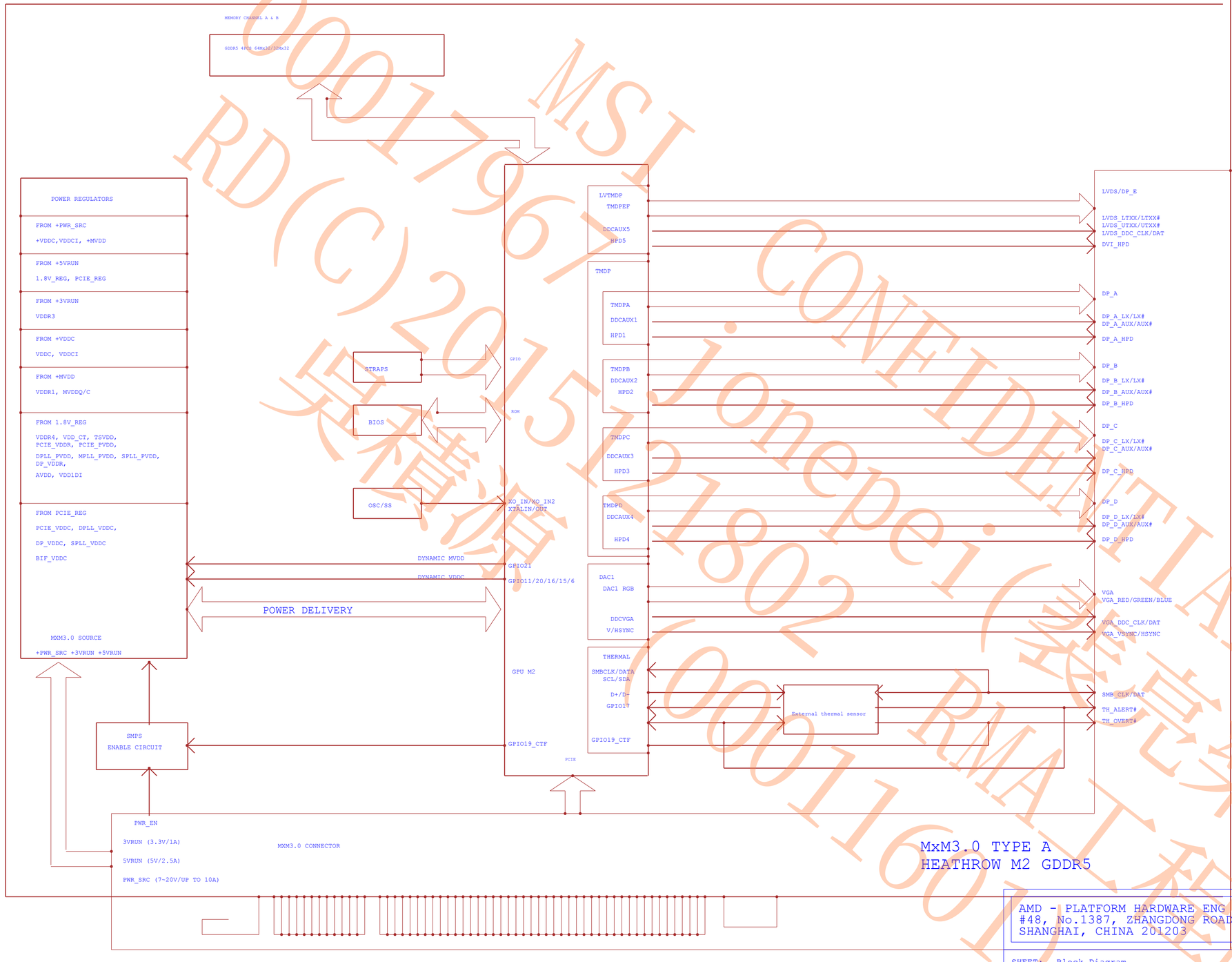

MxM3.0 TYPE A
HEATHROW M2 GDDR5

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SHEET: Block Diagram

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REVISION HISTORY

ENGINEER: XXX

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SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
1.0	00A	12/09/2014	Initial schematics based on C423
1.1	00A	12/10/2014	ADD MC505, MC511, MC524, MC700, MC908

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