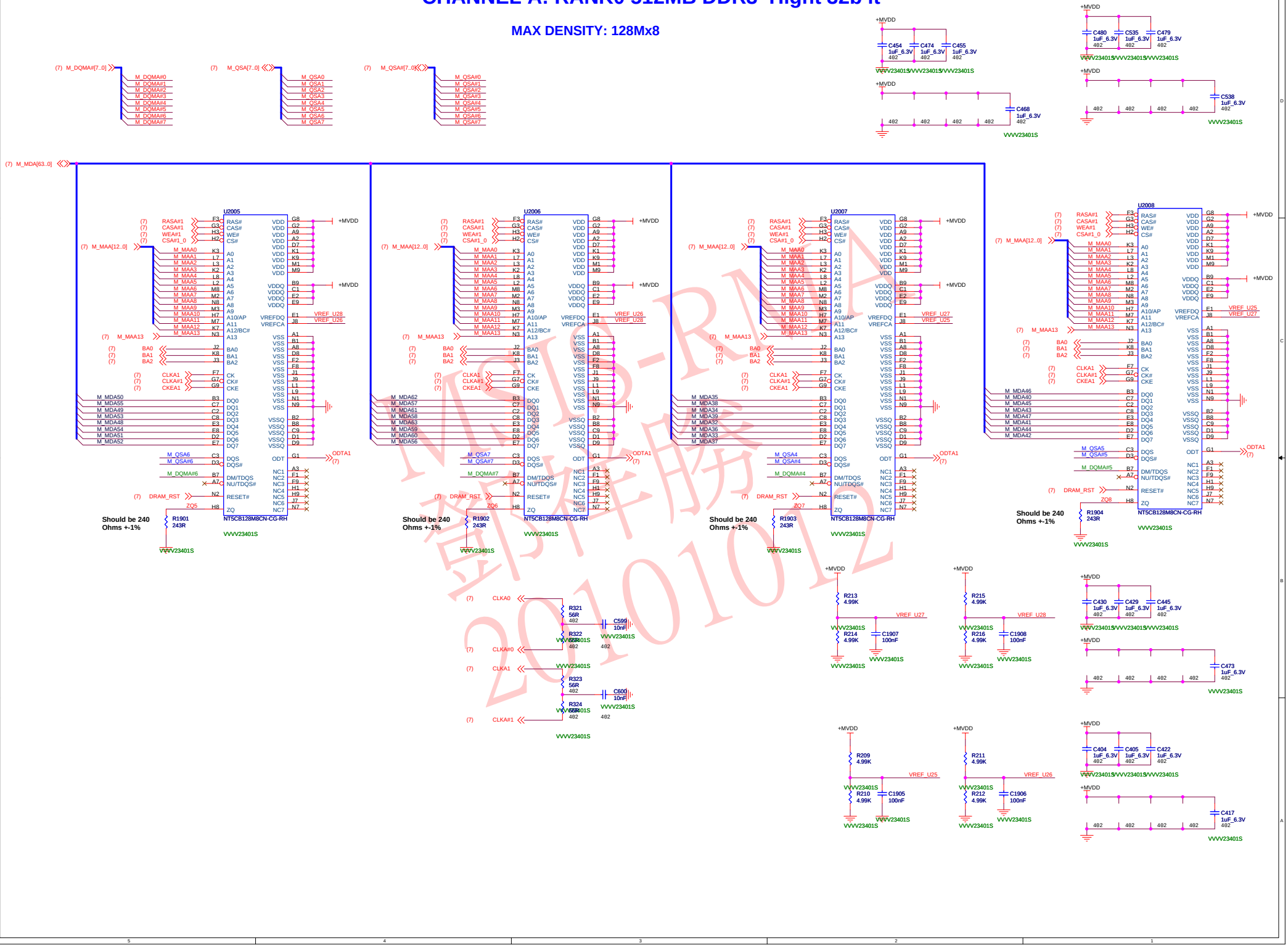
CHANNEL A: RANK0 512MB DDR3 Hight 32b it

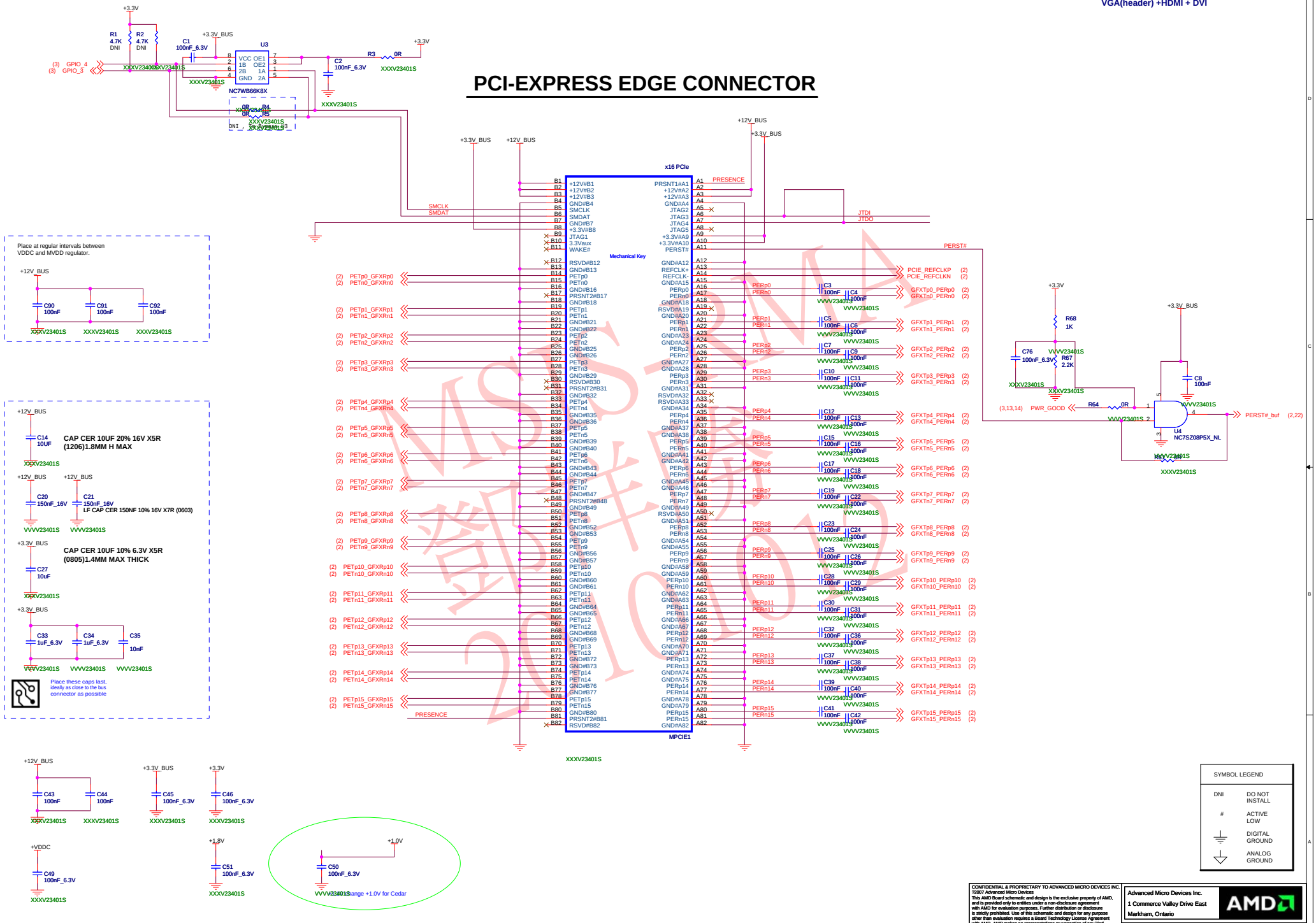
MAX DENSITY: 128Mx8



RV710 CLASH

VGA(header) +HDMI + DVI

PCI-EXPRESS EDGE CONNECTOR



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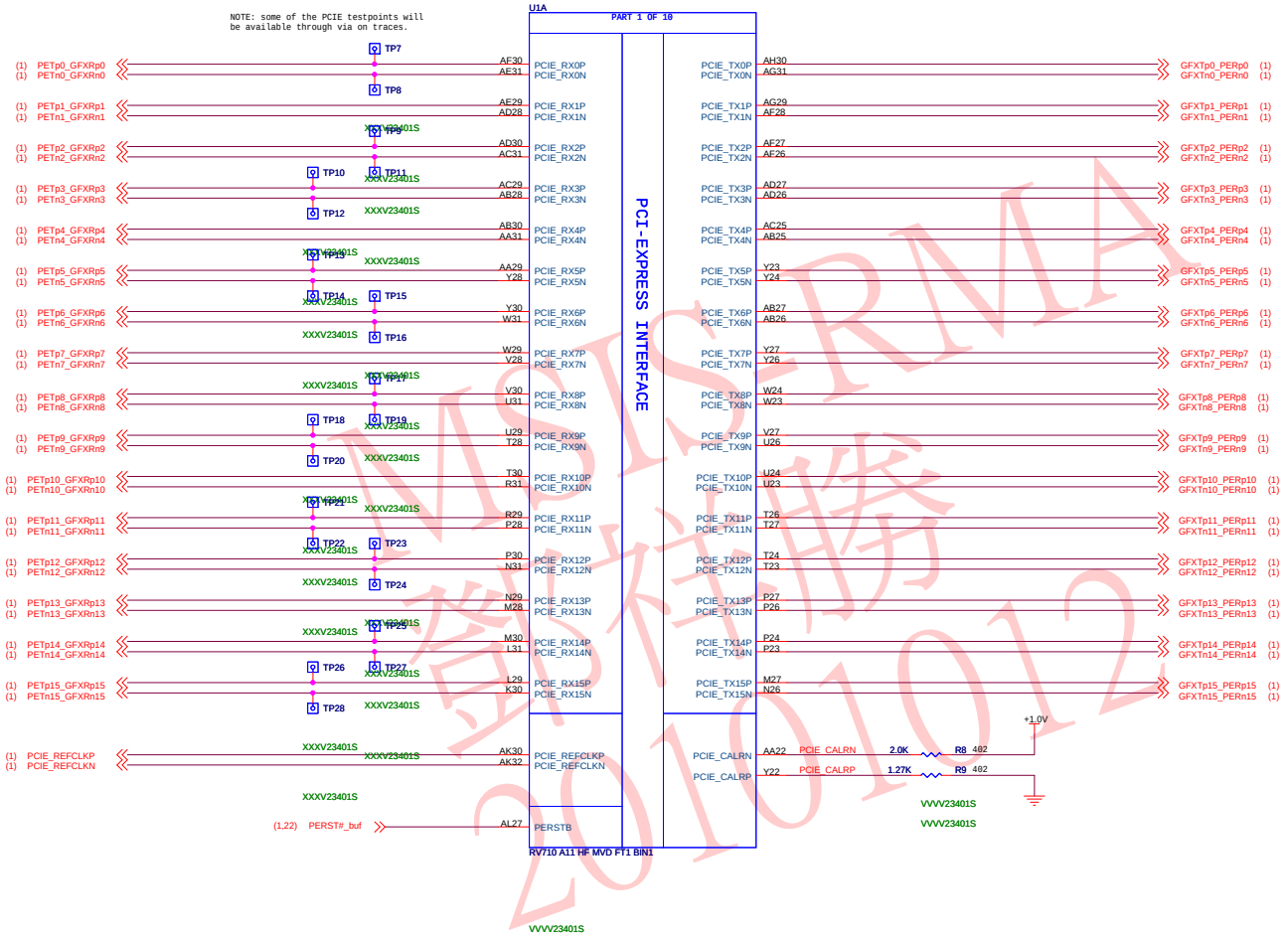
(2) RV710 PCIE Interface



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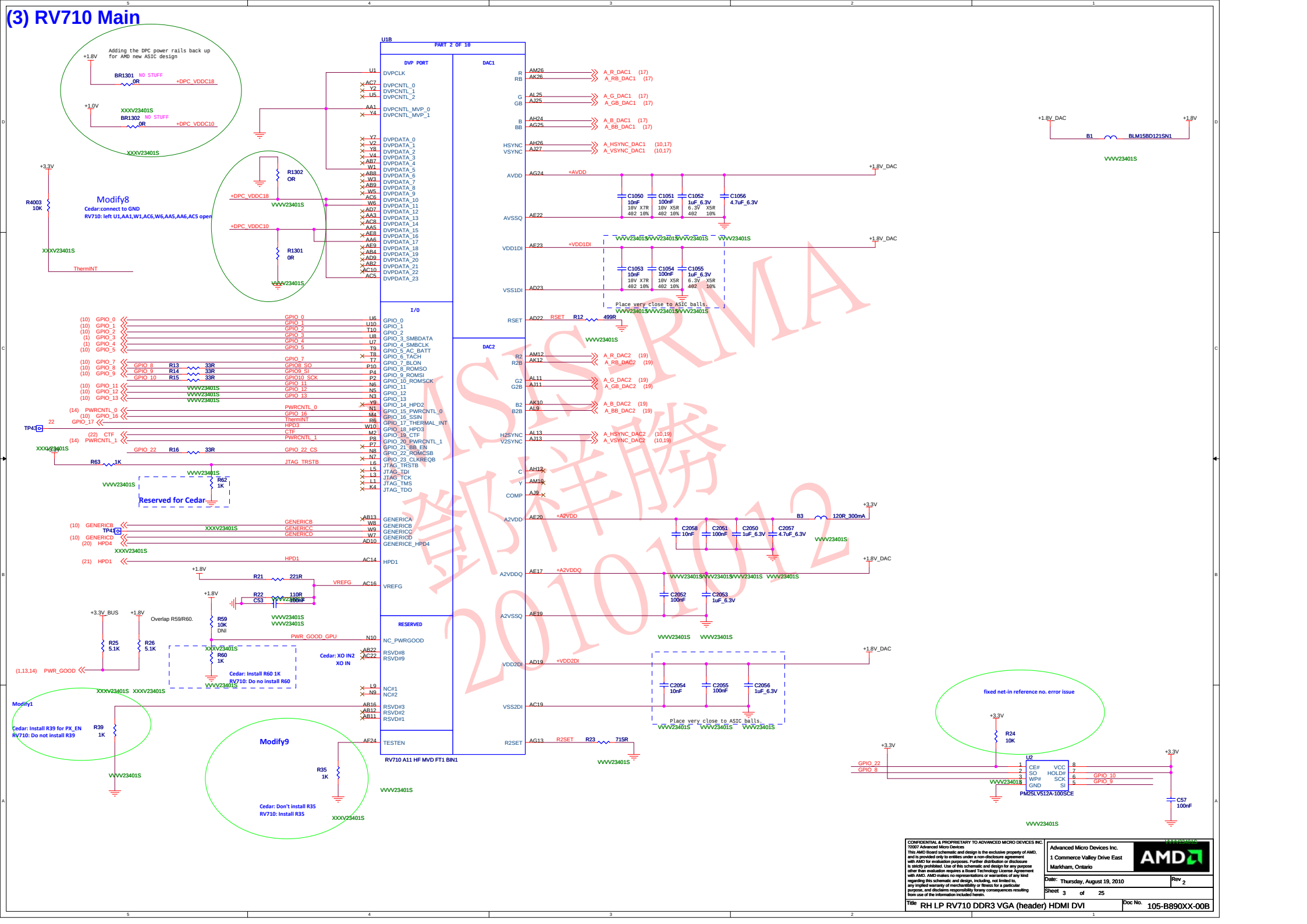
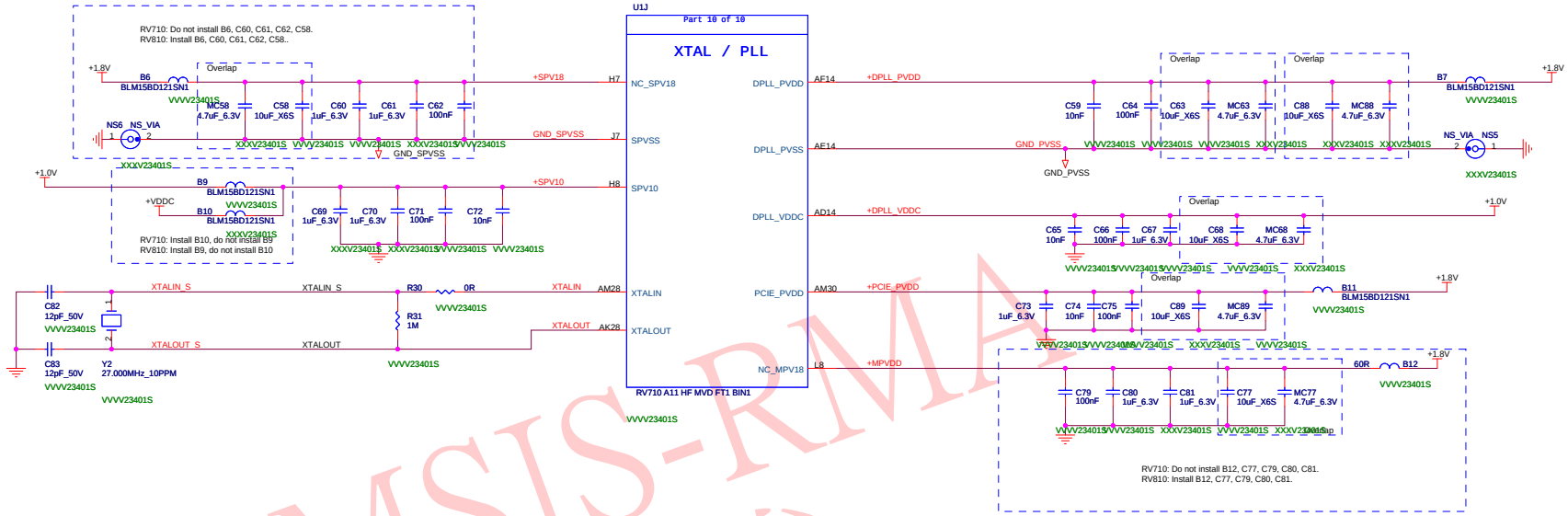
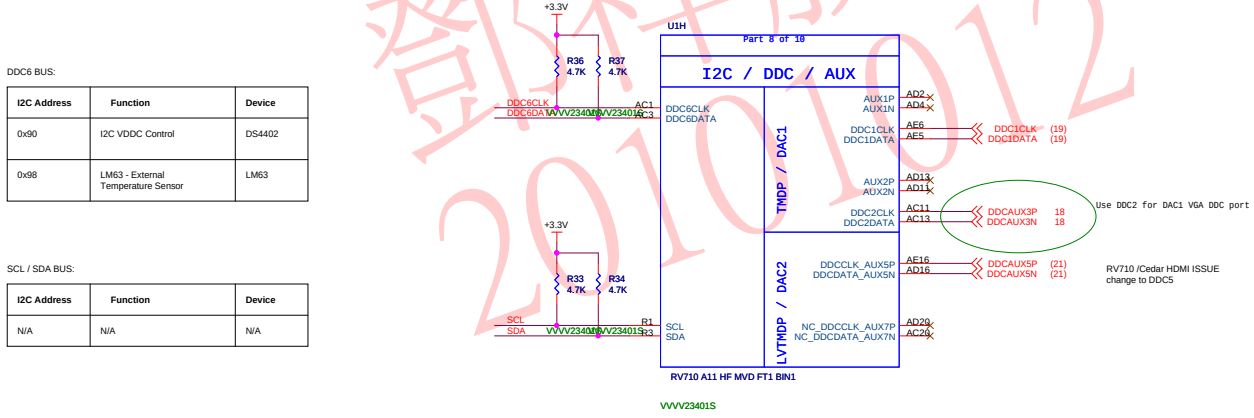
(3) RV710 Main



(04) RV710 GPIOs CF XTAL



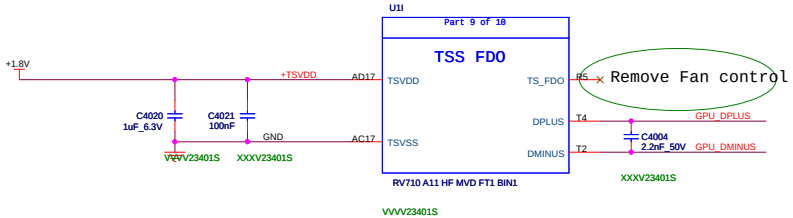


DDC6 BUS:

I2C Address	Function	Device
0x90	I2C VDDC Control	DS4402
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A



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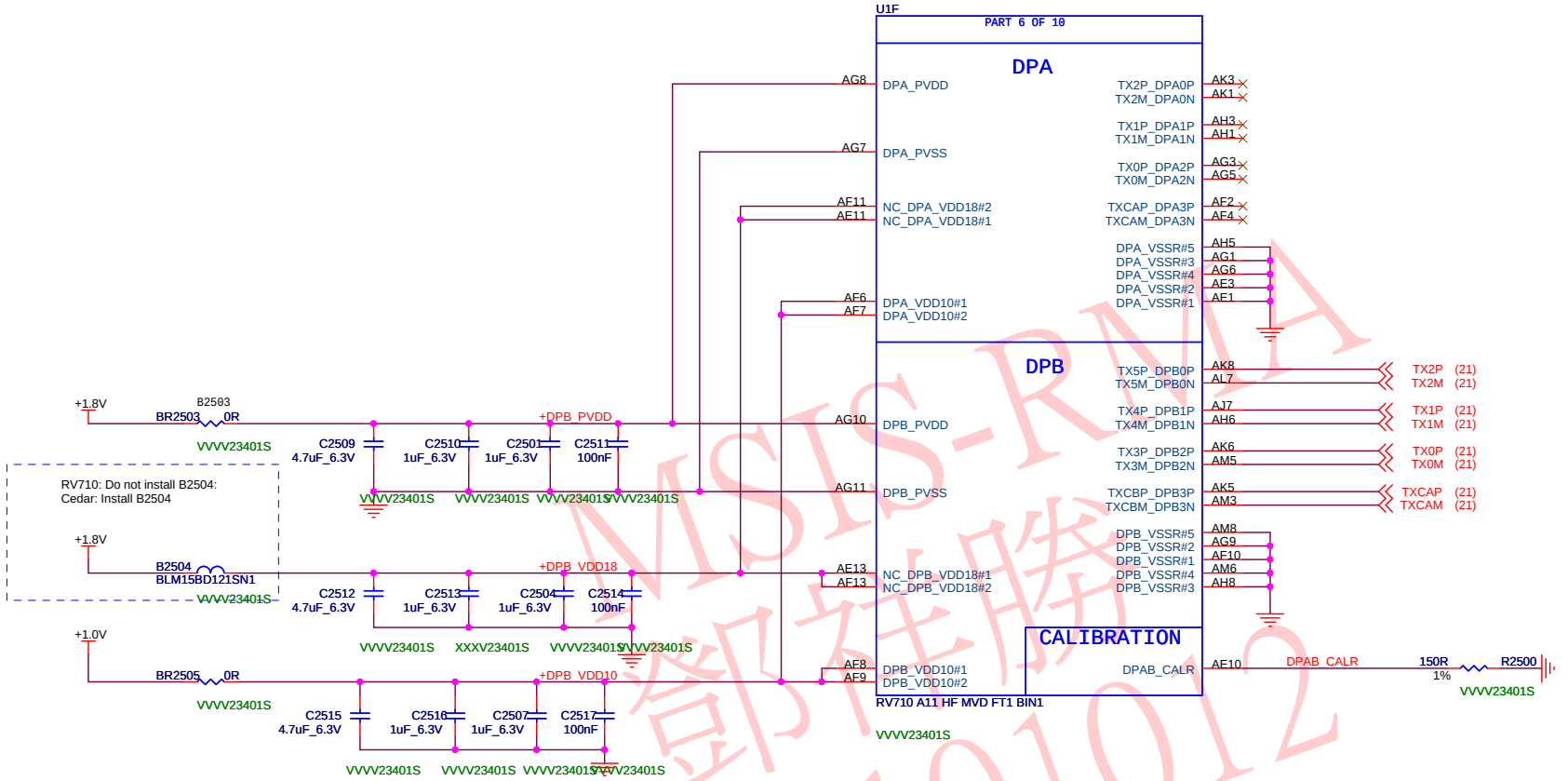
(05) RV710 TMDP A&B

TMDP INTERFACE



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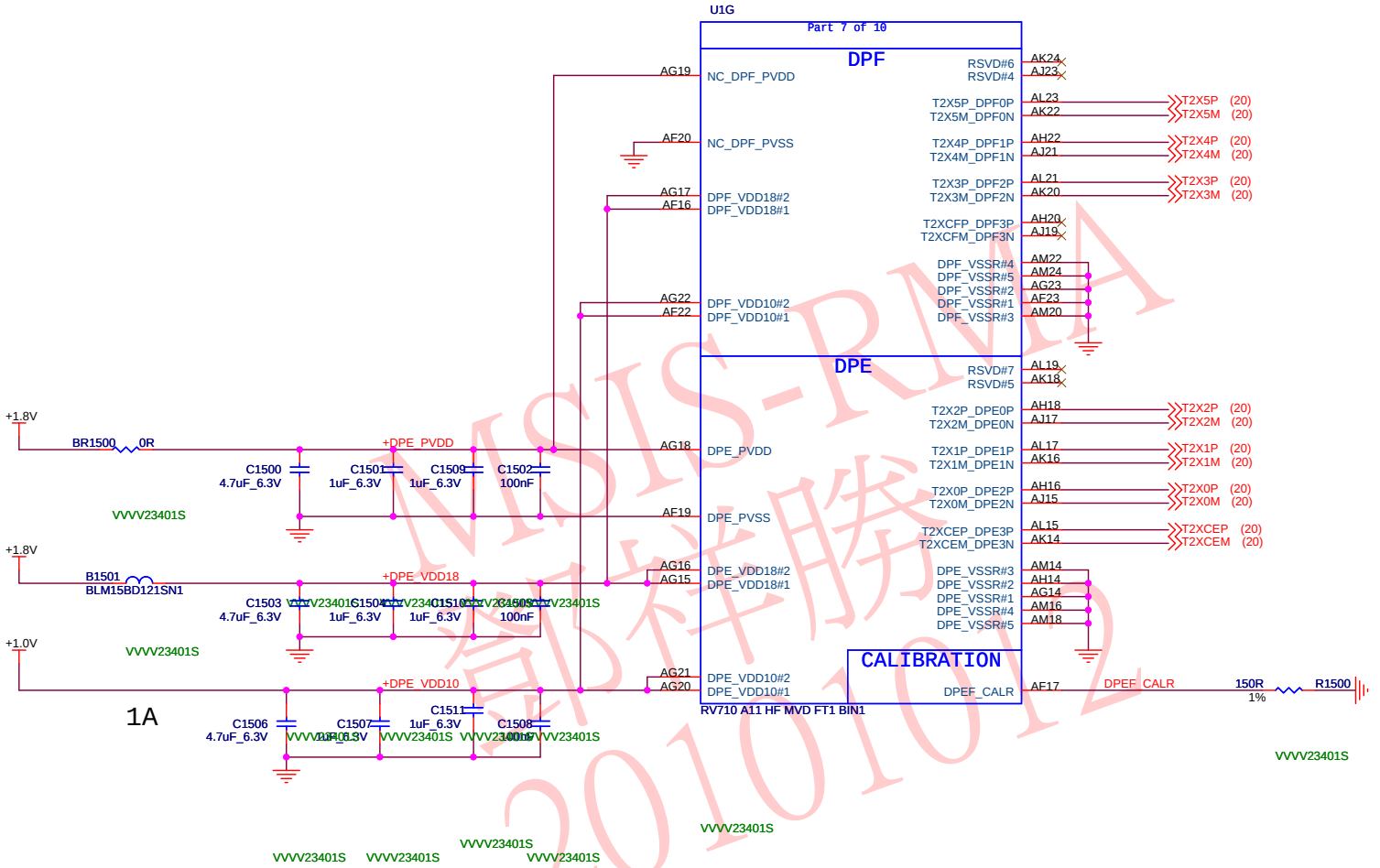
(06) RV710 TMDP E&F

LVTMDP INTERFACE



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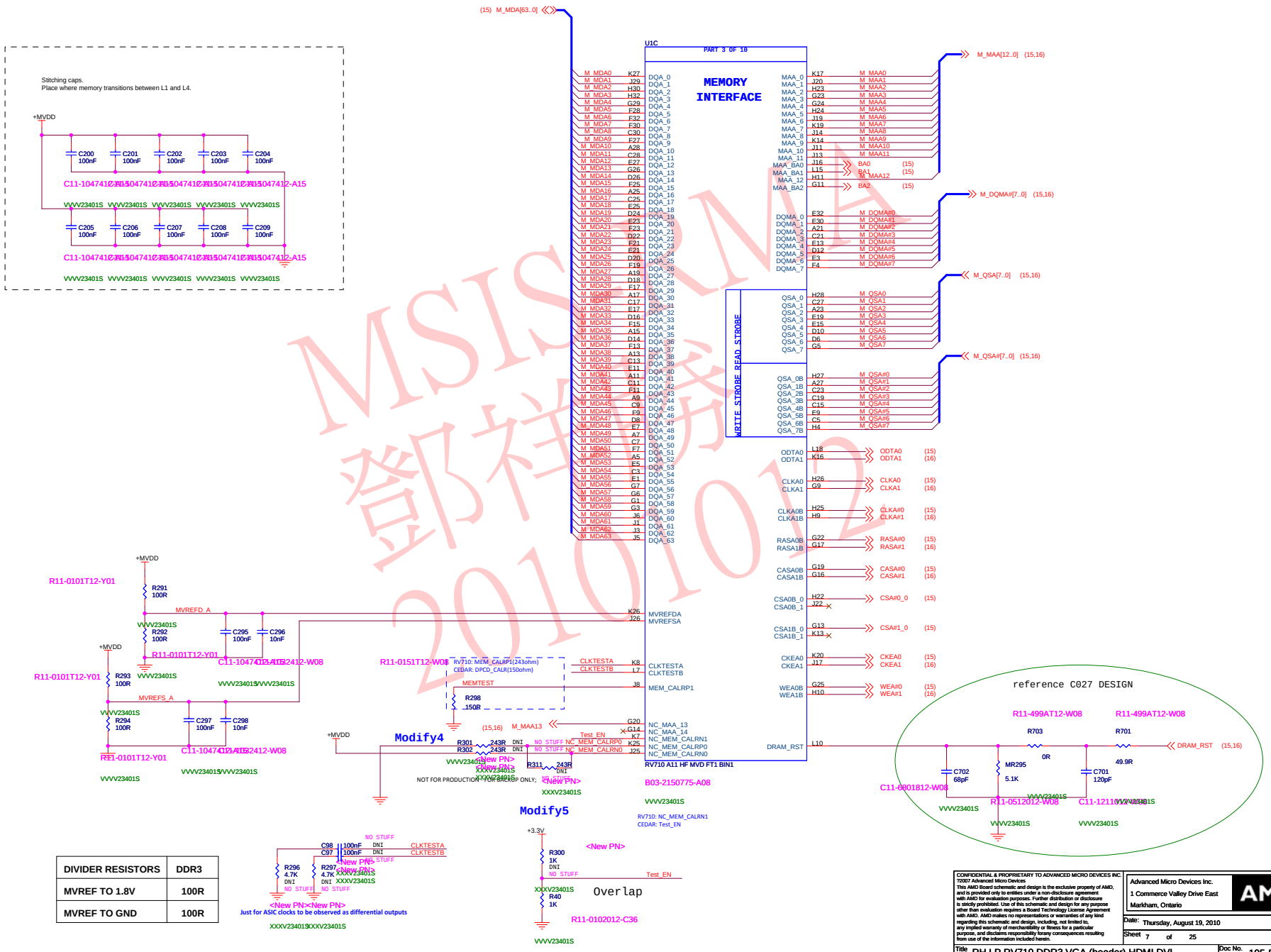
(07) RV710 MEM Interface Ch A

COPY FROM V161 2.1 DDR2 SCH.

MEMORY INTERFACE



DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R

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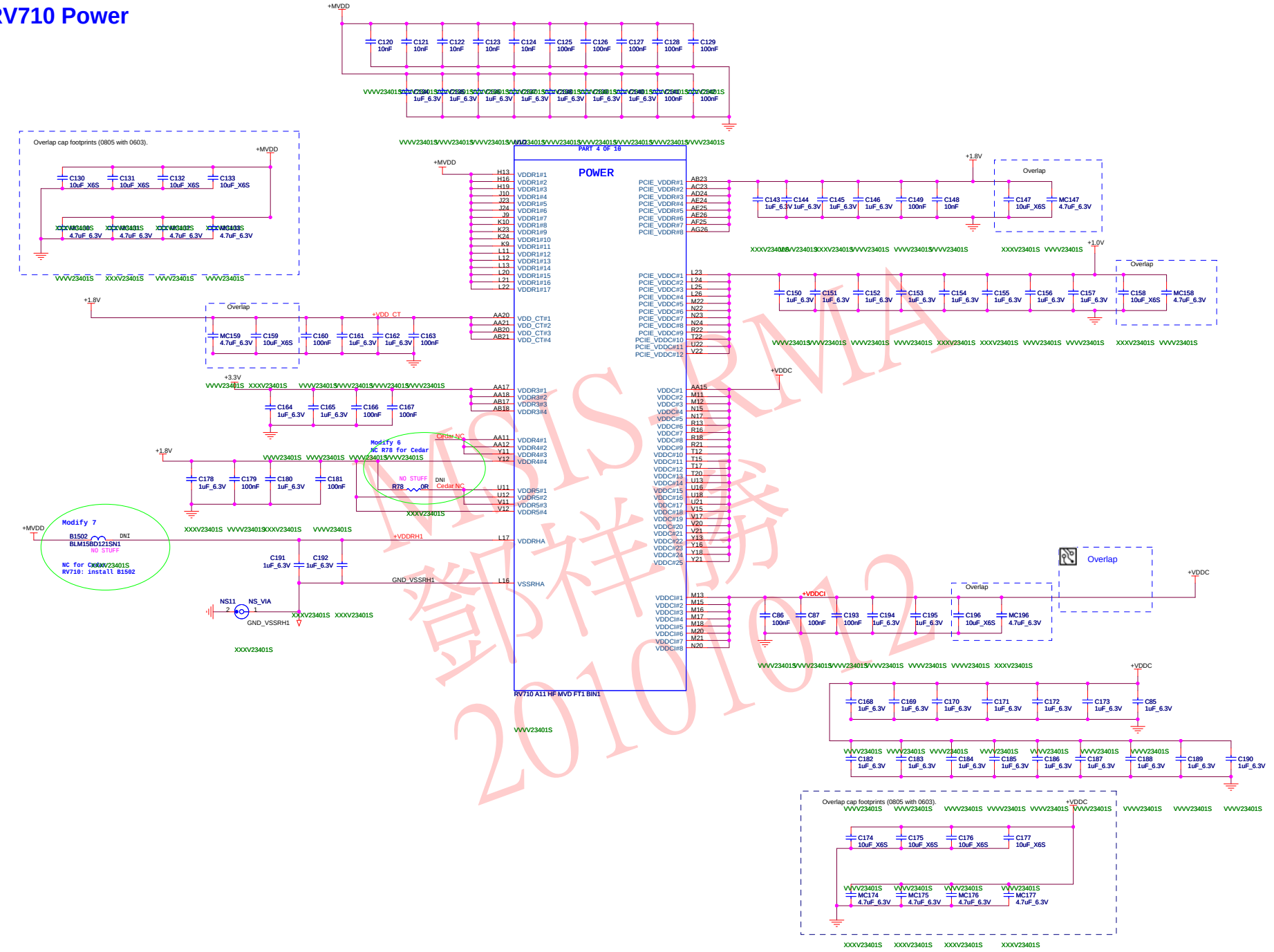
(08) RV710 Power



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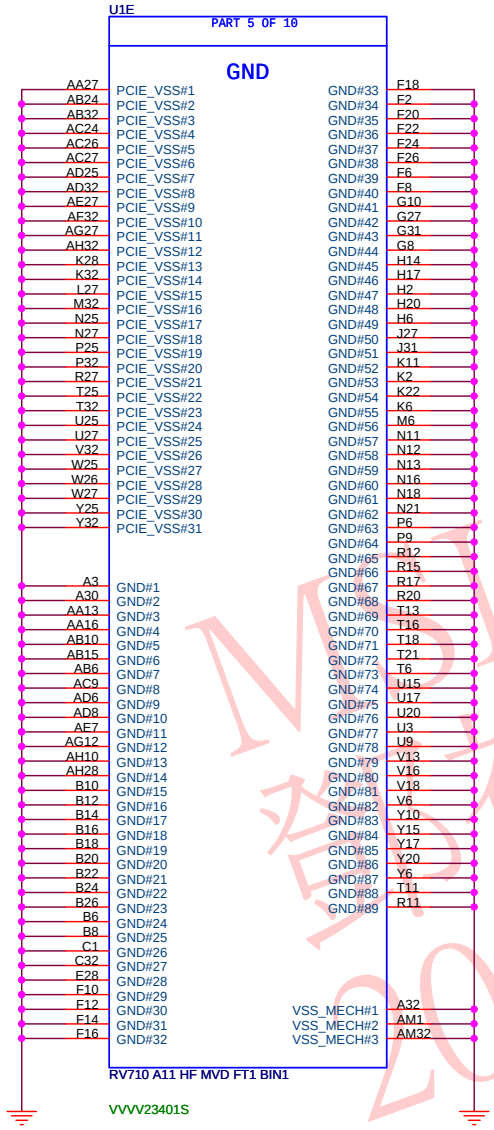
(09) RV710 GND



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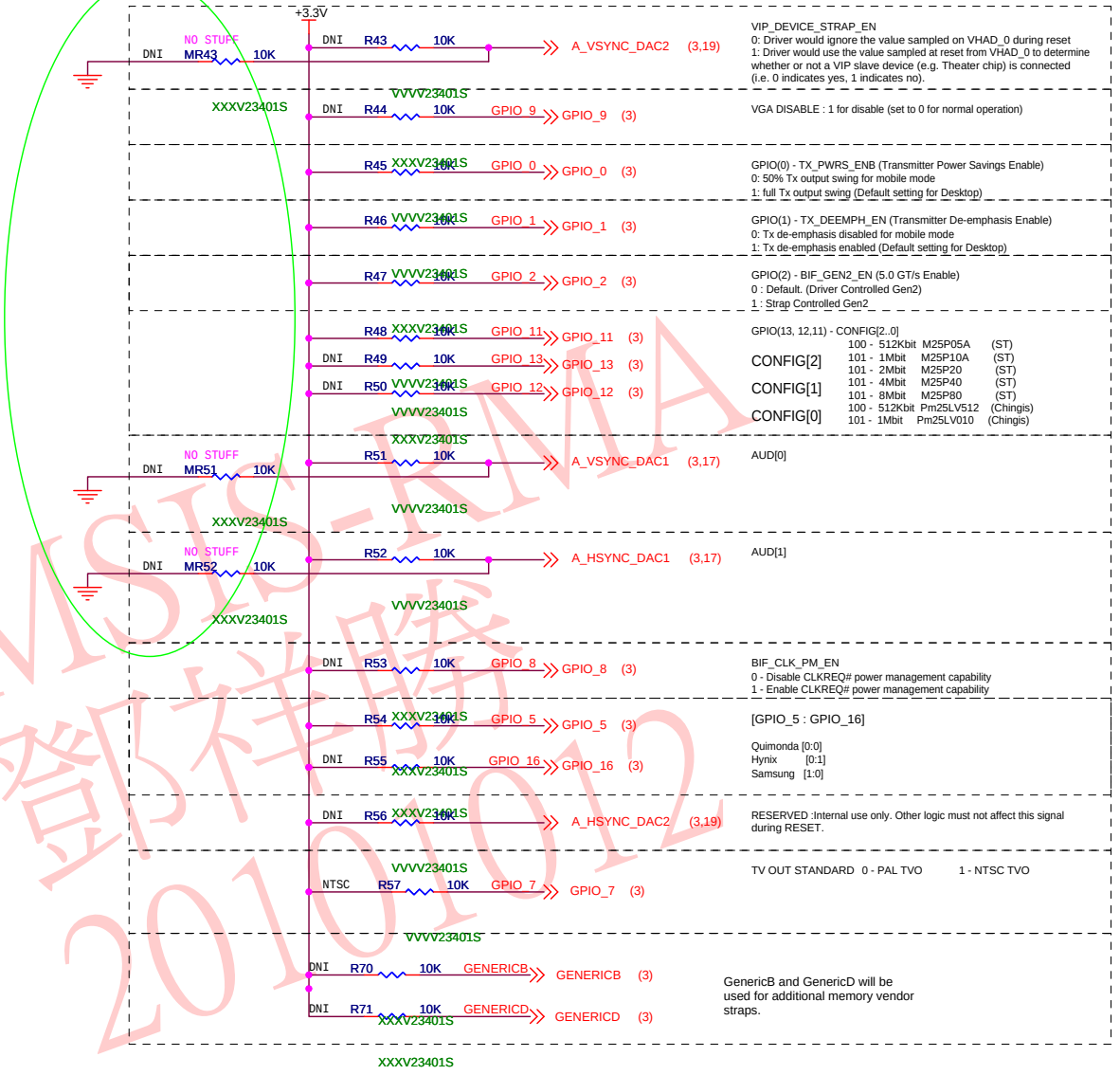
(10) RV710 STRAPS

same V217-0A

PIN BASED STRAPS



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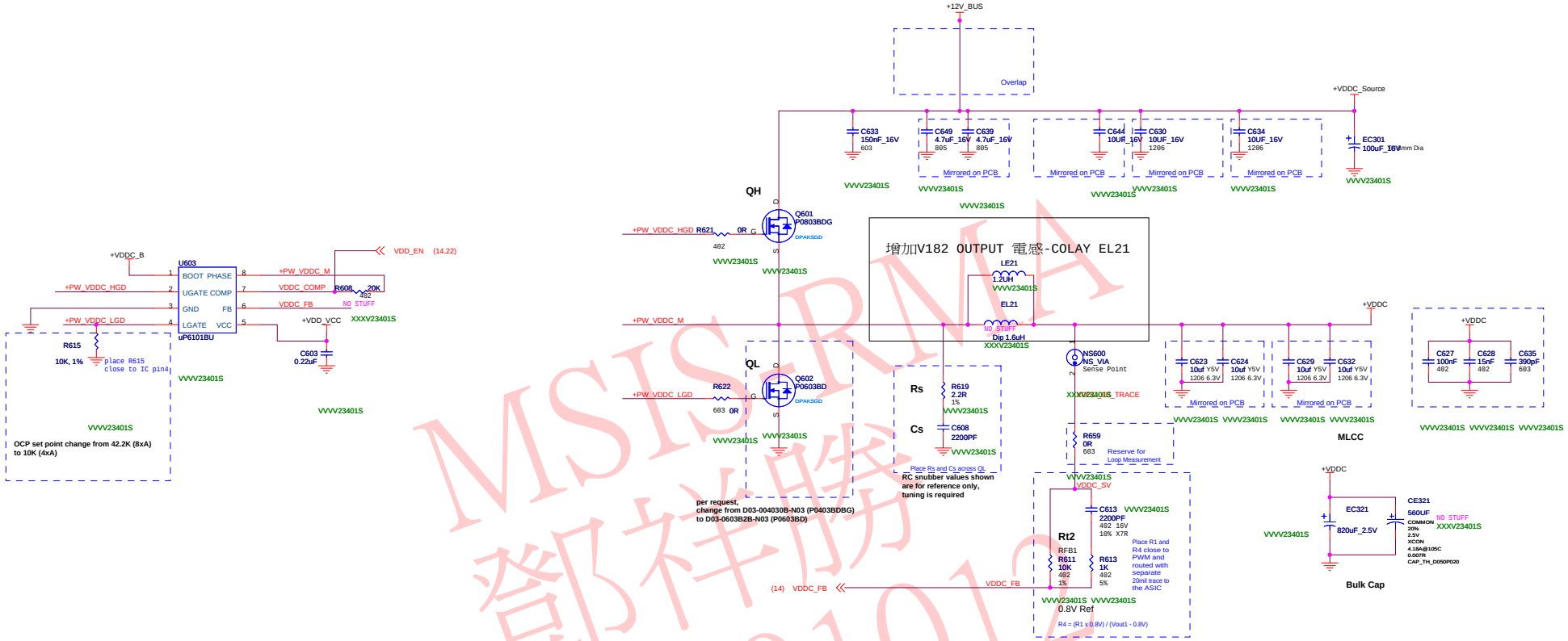
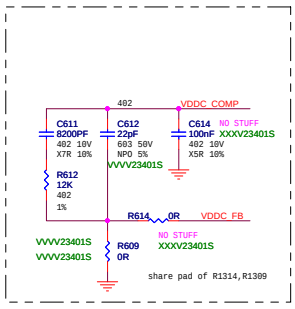
(11) VDDC

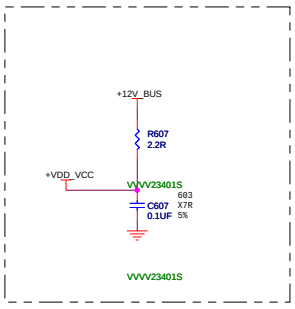


V217 2.0 use L04-12A7651-L65
R612 use 12K, 1%

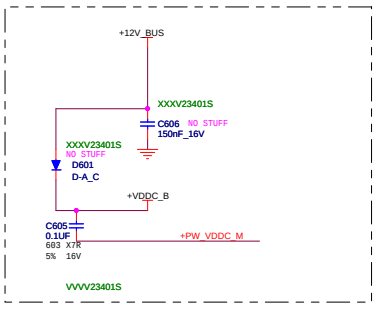
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



VVVV23401S

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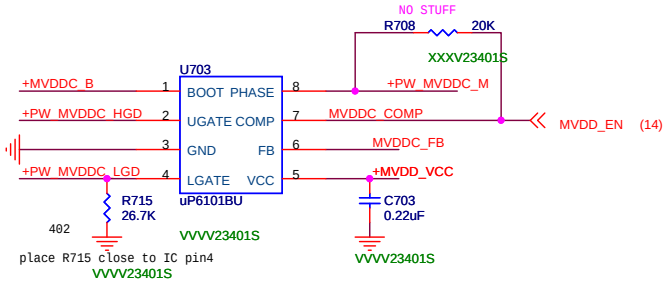
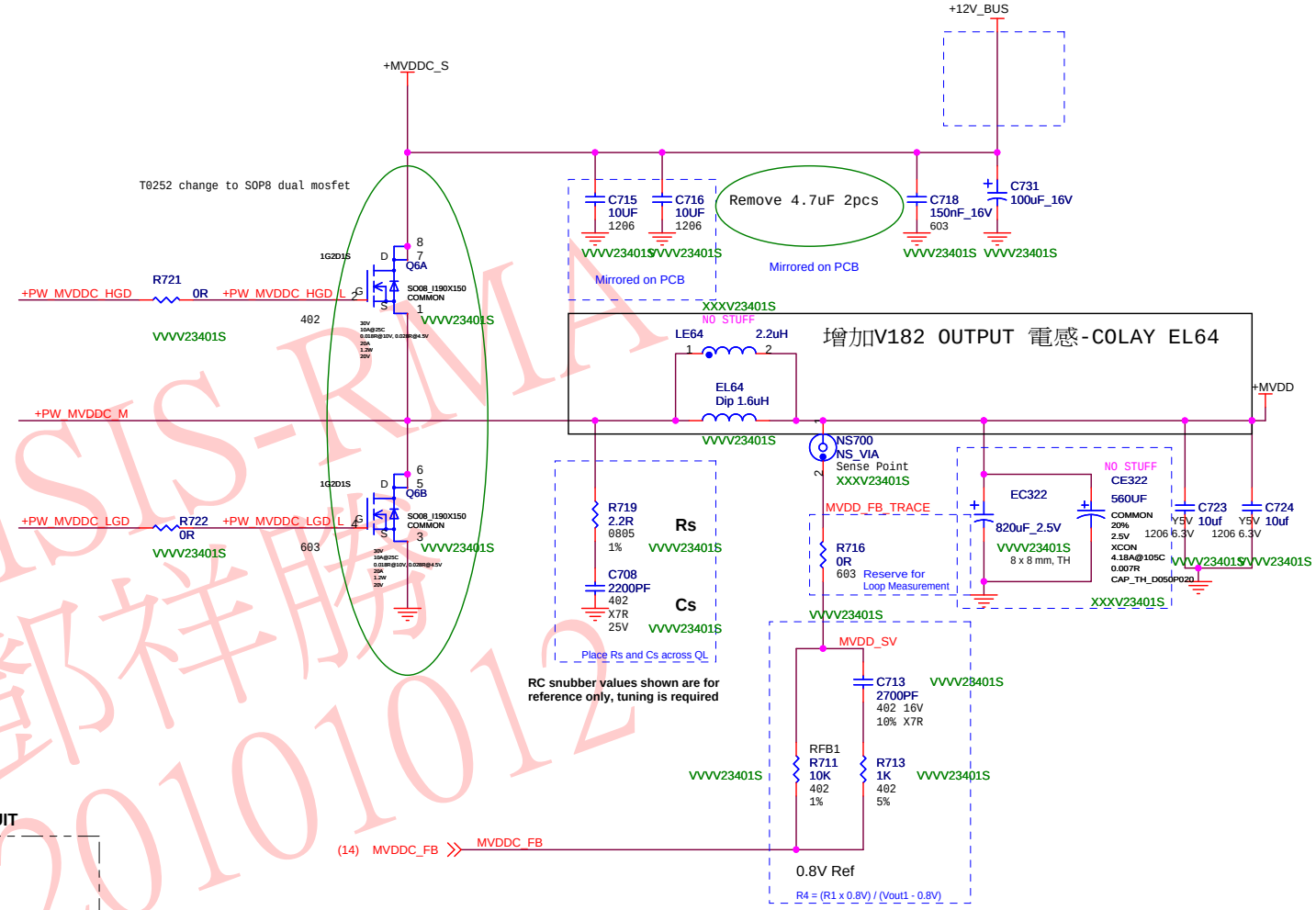
(12) MVDD

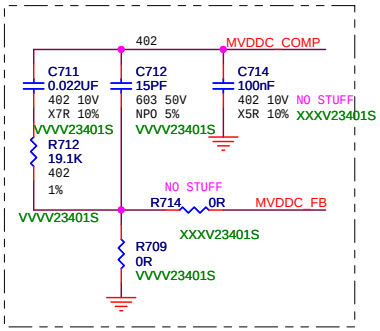


Layout guideline

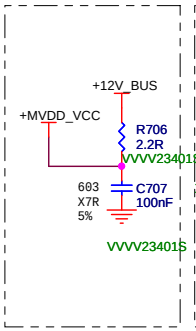
1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



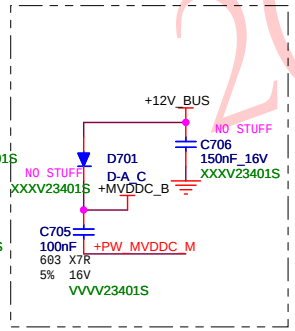
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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(13) Linear Regulators

Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX

LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

remove 5V SHUNT

1/2W@1210

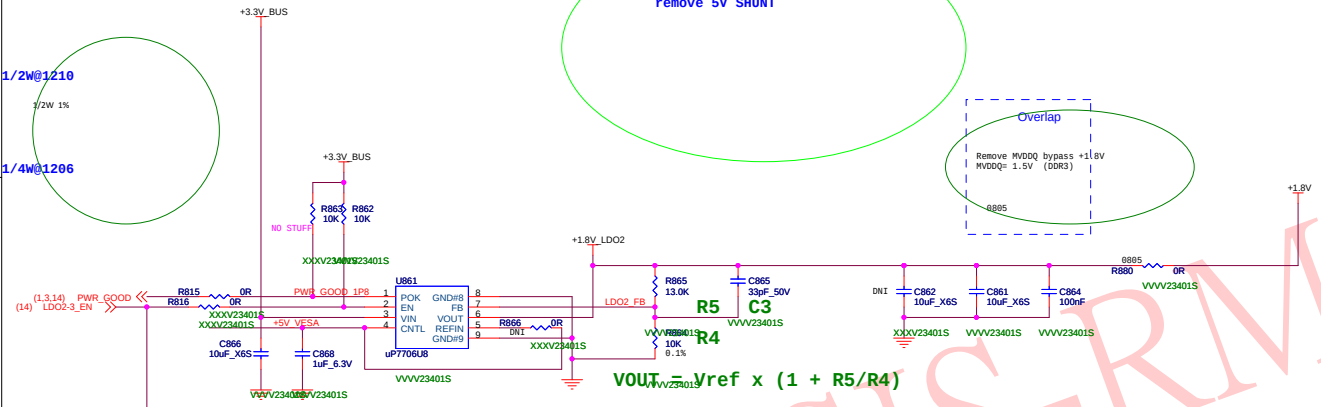
1/2W 1%

1/4W@1206

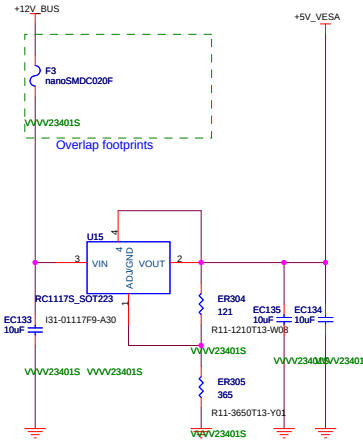
Overlap

Remove MVDDQ bypass +1.8V MVDDQ= 1.5V (DDR3)

0805



Regulators for +5V_VESA



Vout=1.25V* [1+(ER305/ER304)]

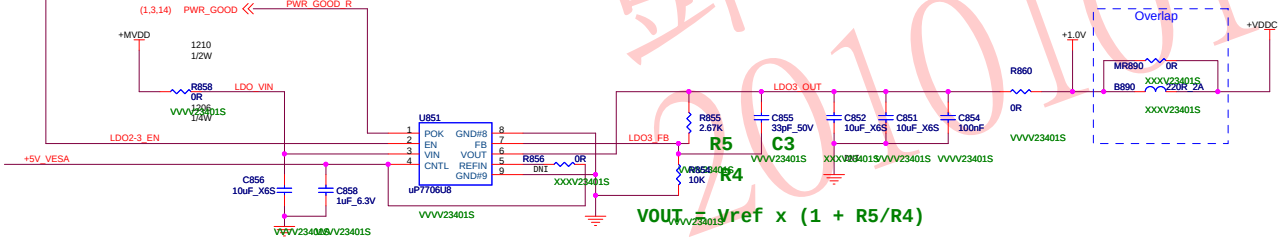
更改+5V_VESA線路,使用1117(COPY V182)

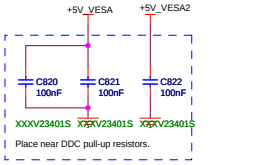
Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA

LDO #3: Vin = +1.4V to 2.087VMAX Vout = +1.1V +/- 2.5% Iout = 1.4A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling





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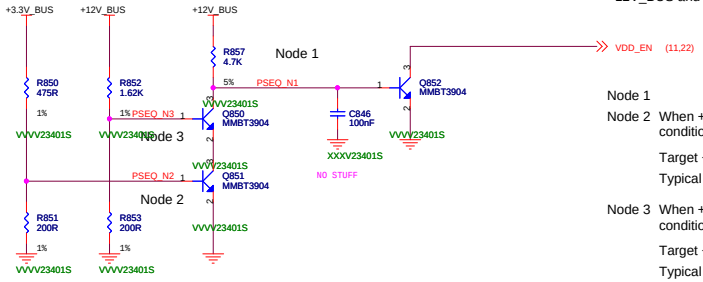
(14) Power Management

Power up/down Sequencing



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.

Node 1

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

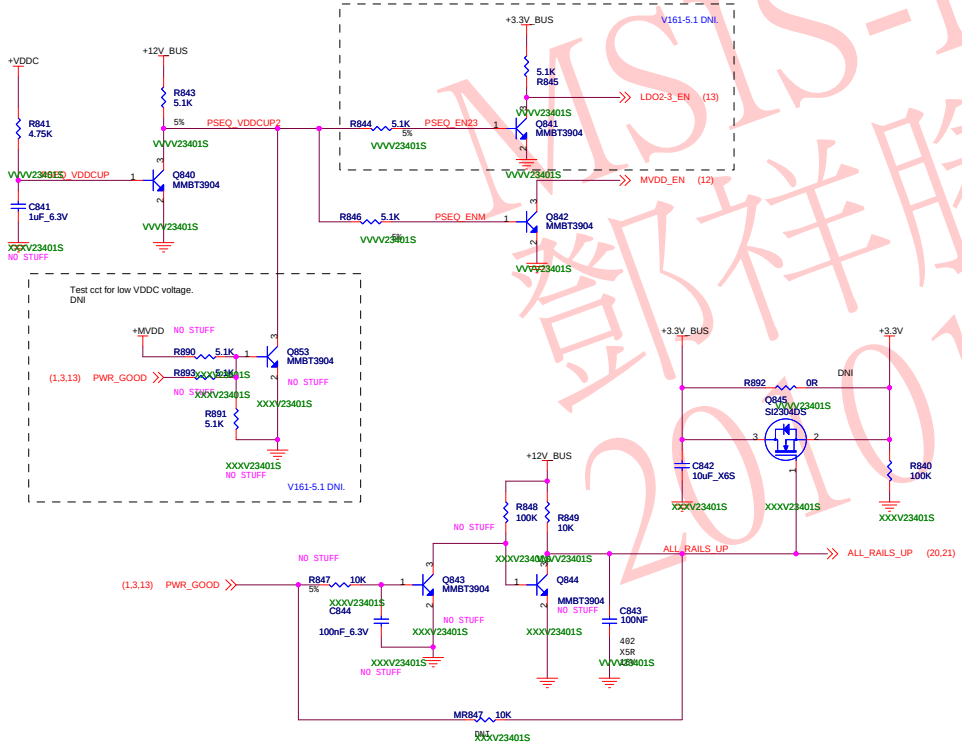
Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

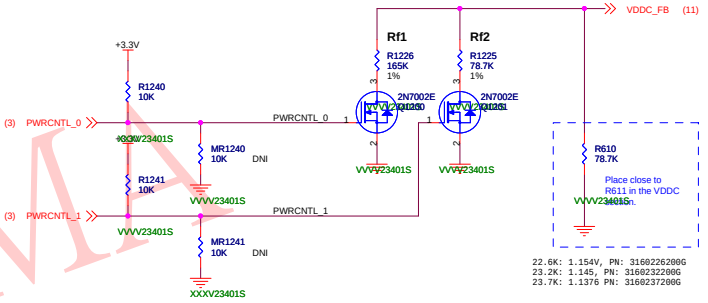
When +12V_BUS ramps above min Vbe, SMPS_EN will be held low



Power Play

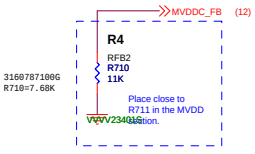
VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0	0				
0	1				
1	0				
1	1	1 0 1			Power-up Default



MVDD Voltage Settings Using GPIOs

PWRCNTL_2 GPIO_6	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0				
1	1 0 1			Power-up Default



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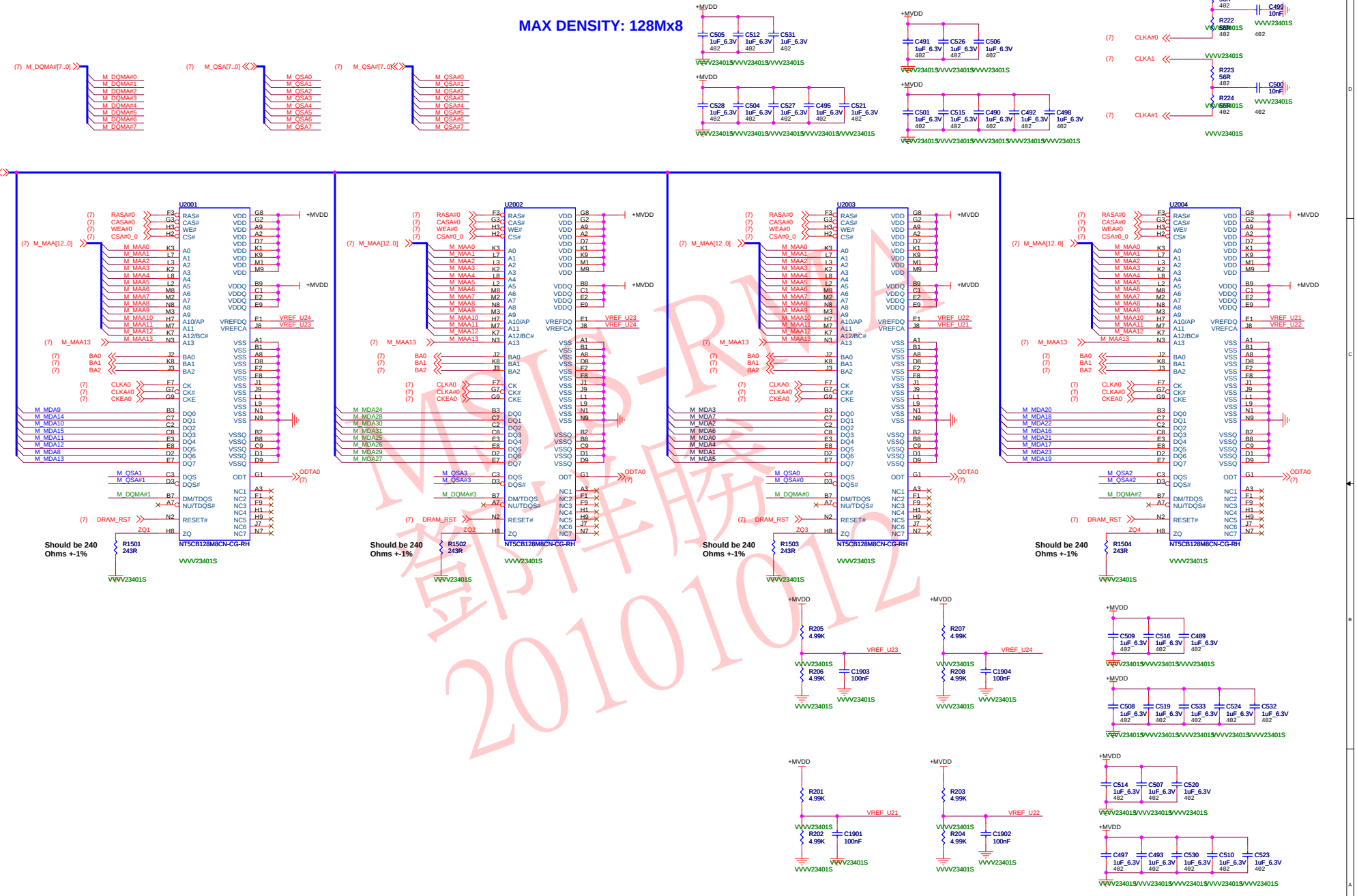
CHANNEL A: RANK 0 512MB DDR3 LOW 32 BIT

MAX DENSITY: 128Mx8



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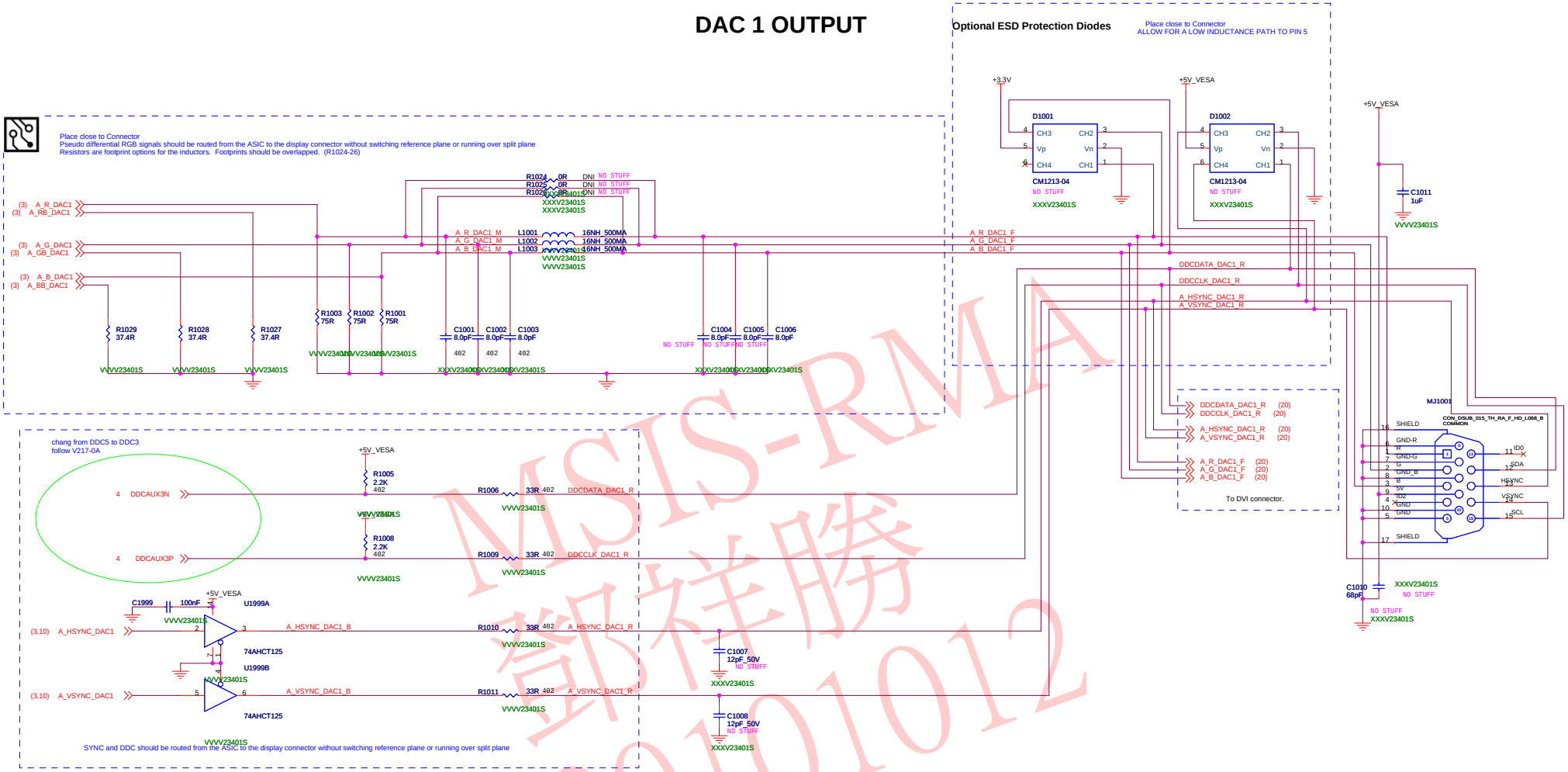
(18) DAC1 OUTPUT



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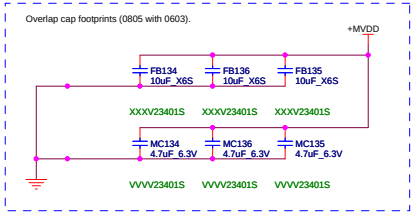
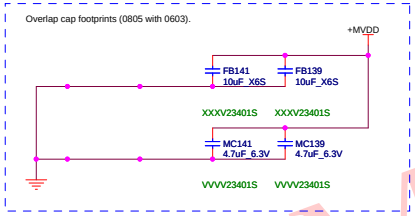
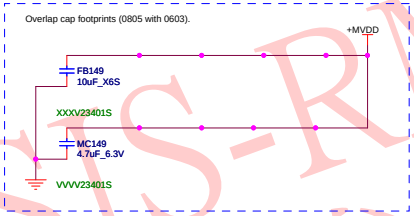
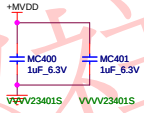
(17) DDR3 Termination







Overlap 0805 / 0603 footprints.



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(19) DAC2 OUTPUT

DAC 2 OUTPUT

Optional ESD Protection Diodes

Place near D2002, D2003, D2004, D2005

Place close to Connector

Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane

(3) A_R_DAC2
(3) A_RB_DAC2
(3) A_G_DAC2
(3) A_GB_DAC2
(3) A_B_DAC2
(3) A_BB_DAC2

R2024 0R DNI NO STUFF
R2025 0R DNI NO STUFF
R2026 0R DNI NO STUFF
XXXV23401S
XXXV23401S

A_R_DAC2_M
A_G_DAC2_M
A_B_DAC2_M

L2001 16NH_500MA
L2002 16NH_500MA
L2003 16NH_500MA
VVVV23401S
VVVV23401S
OVERLAP

R2029 37.4R
R2028 37.4R
R2027 37.4R
R2003 75R
R2002 75R
R2001 75R
C2001 8.0pF
C2002 8.0pF
C2003 8.0pF
C2004 8.0pF
C2005 8.0pF
C2006 8.0pF
NO STUFF

add 3pcs LC filter cap.

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R

+5V_VESA2
C2011 1uF
C2010 68pF NO STUFF

J2
Header_16_Pin_2X8

2X8 HEADER FOR VGA RIBBON CONNECTOR

remove level shift parts. same V217-0A

RV710: DDC2 is 5V tolerant. Do not install level shifter.
--> Do not install R2013, R2015, Q2001, Q2002. Install R2014, R2016.
RV810: DDC2 is NOT 5V tolerant. Install level shifter.
--> Do not install R2014, R2016. Install R2013, R2015, Q2001, Q2002.

(4) DDC1DATA
(4) DDC1CLK
R2005 2.2K 402
R2008 2.2K 402
R2006 33R 402 DDCDATA_DAC2_R
R2009 33R 402 DDCCLK_DAC2_R

U1999C 74AHCT125
U1999D 74AHCT125
(3,10) A_HSYNC_DAC2
(3,10) A_VSYNC_DAC2
A_HSYNC_DAC2_B
A_VSYNC_DAC2_B
R2010 33R 402 A_HSYNC_DAC2_R
R2011 33R 402 A_VSYNC_DAC2_R
C2007 12pF_50V NO STUFF
C2008 12pF_50V NO STUFF

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

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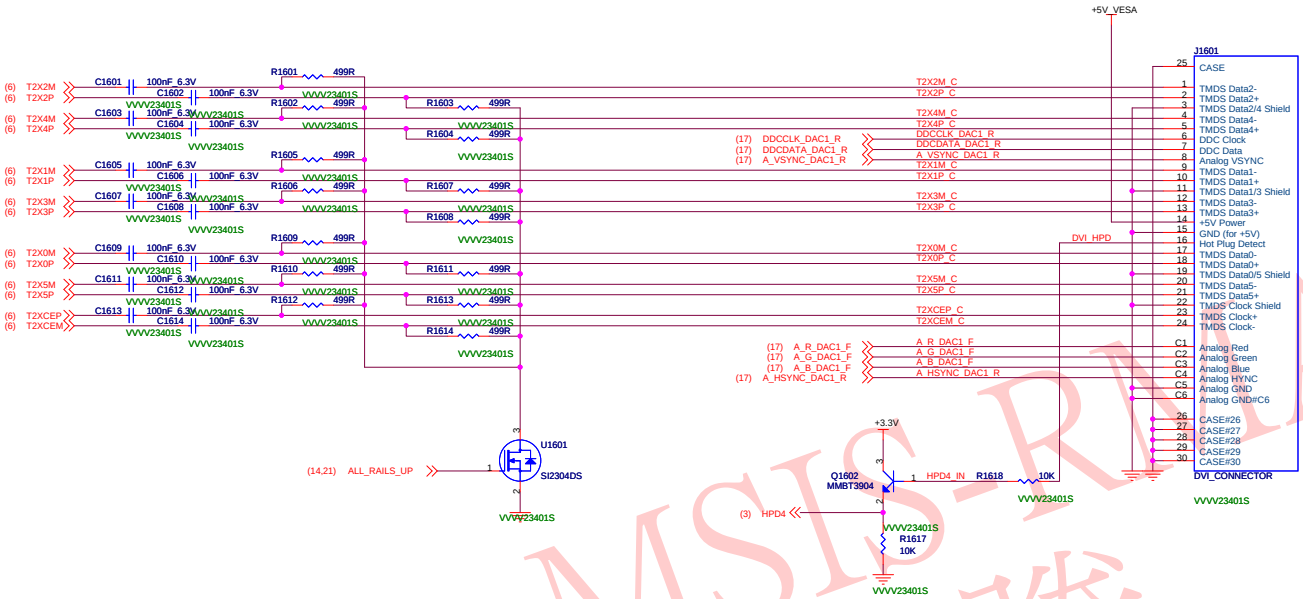
(20) DVI OUTPUT

DPE / DPF OUTPUT



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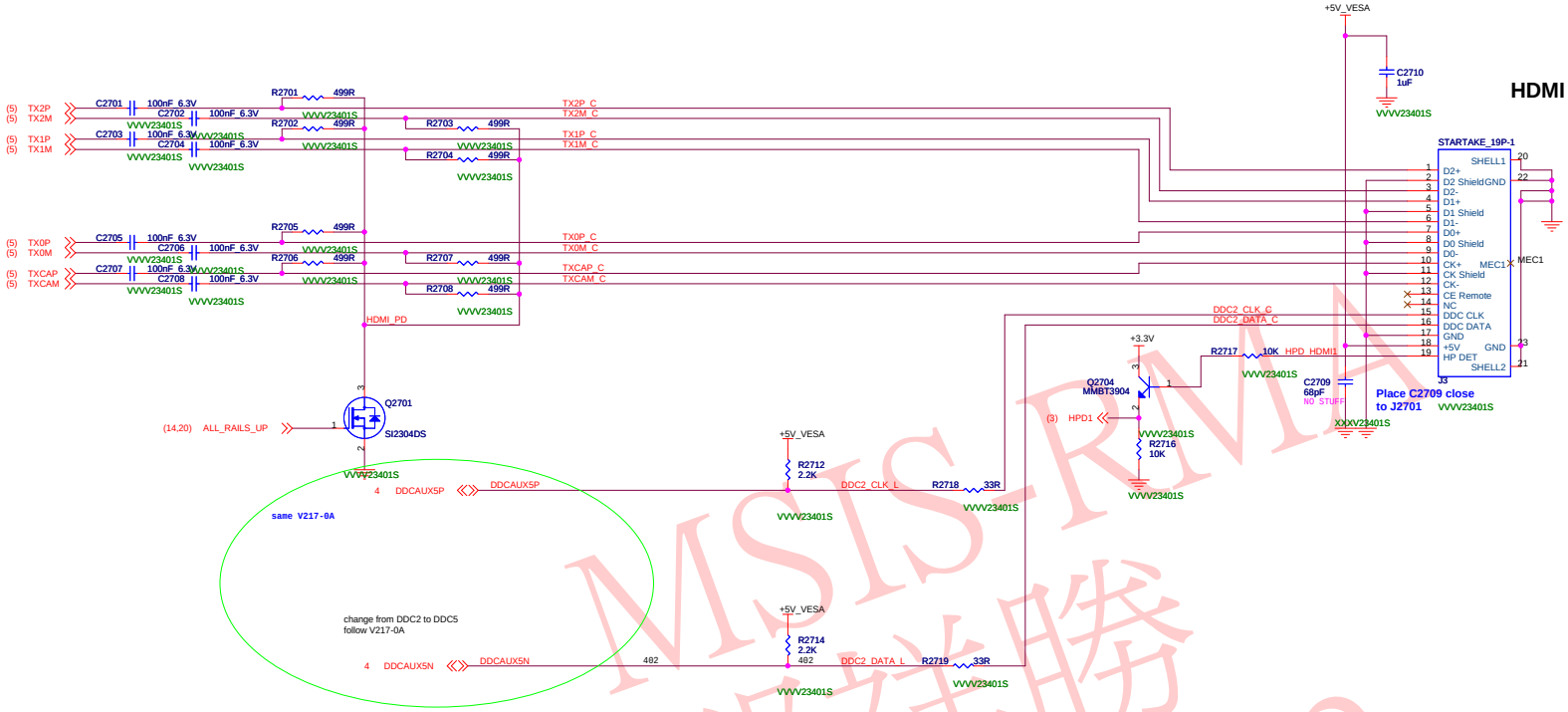
(21) HDMI OUTPUT

TMDP-B OUTPUT



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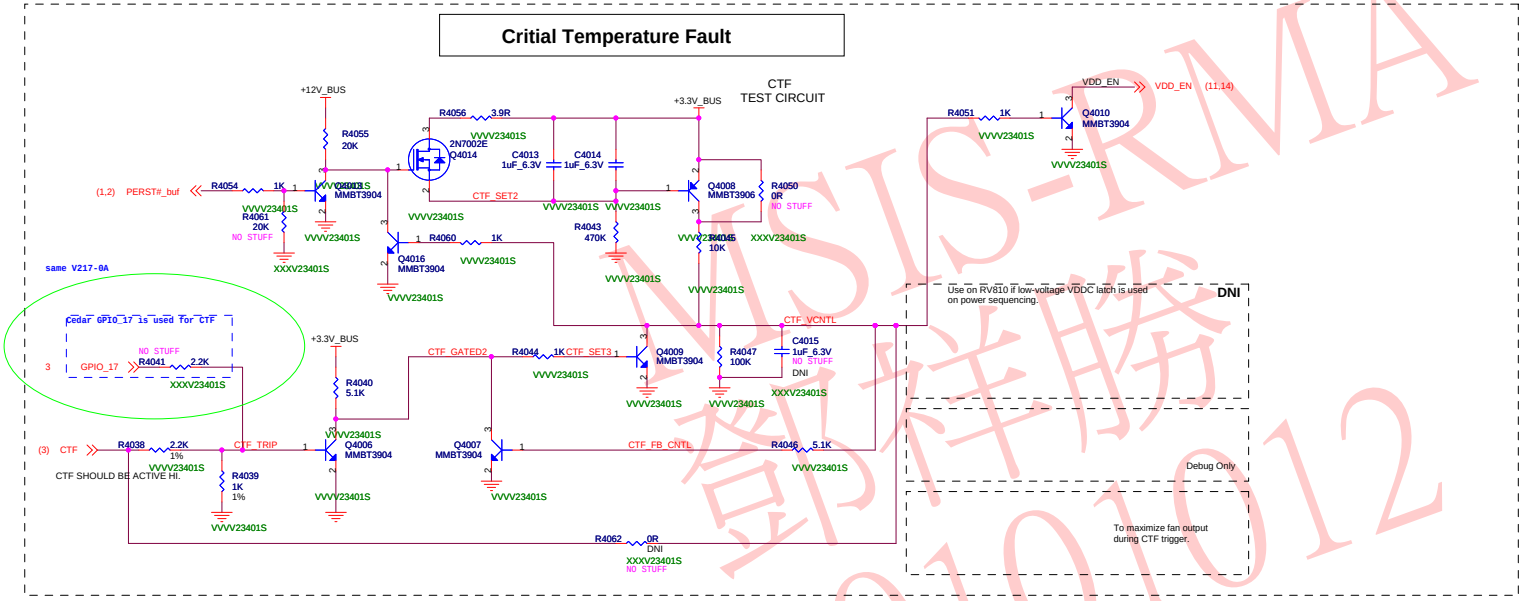
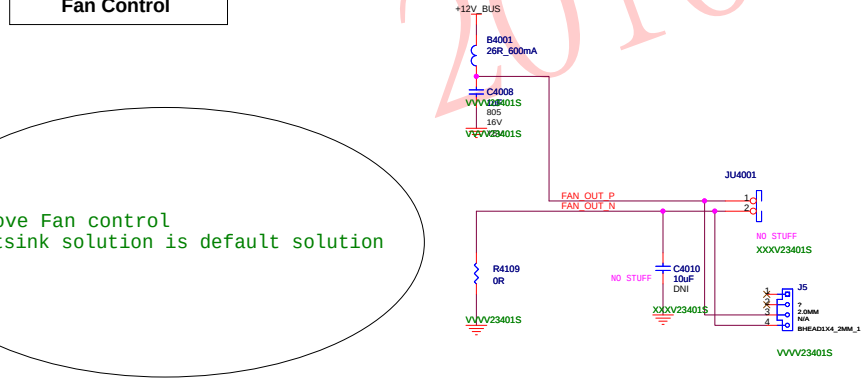
(22) Thermal Management



WARNING!
Be cautious when using a 3-wire fan with this fan control circuit. The negative pin will not always be ground. Some 3-wire fans with tachometers will only work if the negative pin of the fan is ground.



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H1A RV610_FANSINK

VVVV23401S

45 Ohm ，4.89 mil
Place BOTTOM Layer
J14

J14 X_PIN1*2

XXXV23401S

45 Ohm 5.83 mil
Place L3 Layer
J12

J12 X_PIN1*2

XXXV23401S

80 Ohm(DIFF)，Width 5.12 mil / Spacing 7.599 mil
Place BOTTOM Layer
J11

J11 impedence

XXXV23401S

85 ohm(DIFF)，Width 3.9 8 mil / Spacing 5.9 mil
Place TOP Layer
J13

J13 impedence

XXXV23401S

SK1

Socket_RV710-M92_50.8

XXXV23401S

H3 HEATSINK

XXXV23401S

H2 RV610_LP_HEATSINK

XXXV23401S

ASSY1 BRACKET

8020040100G

XXXV23401S

BKT BRACKET LP

8020040400G

VVVV23401S

FM1 FM2 FM3 FM4

OPT F_PAD_X

XXXV23401S

FM5 FM6

OPT F_PAD_X

XXXV23401S

FOR EMI

EM100 E23_1P XXXV23401S

EM101 E23_1P XXXV23401S

EM103 E23_1P XXXV23401S

EM104 E23_1P ATE_C006_106 XXXV23401S

EM105 E23_1P ATE_C006_106 XXXV23401S

Option for EMI

H1B H1C H1D

RV610_FANSINK

VVVV23401S

For DVI Connector

VGA SCREWS

MEC3 MEC4

MEC_SCREW_HEX_JACK

DVI SCREWS

MEC1 MEC2

MEC_SCREW_HEX_JACK

HDMI SCREWS

MEC5

<PCB Footprint>

PCB

PCB

109-GN982-00A

PK0-0V23410-E48

NullFootprint

VVVV23401S

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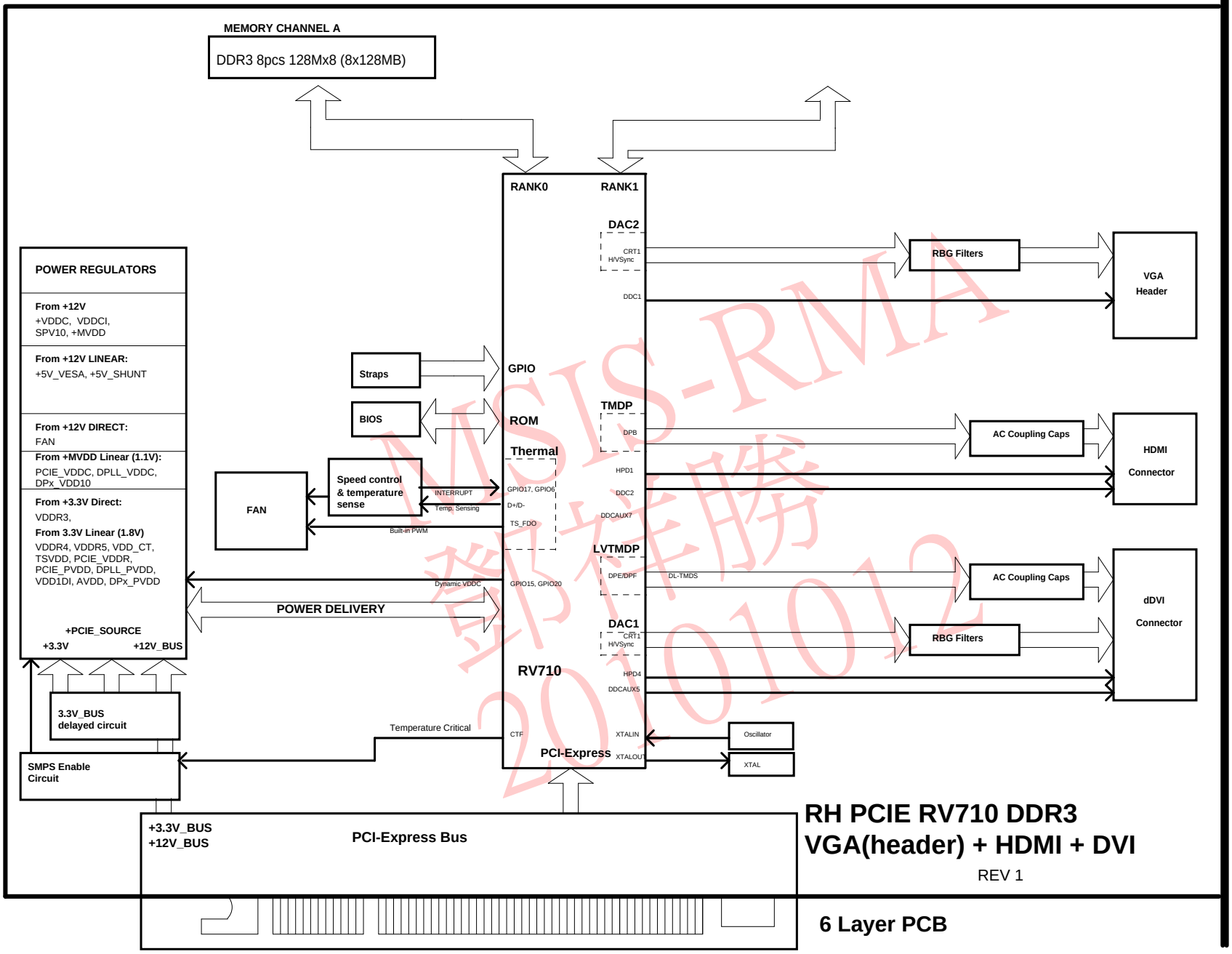

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Title	Schematic No.	Date:
RH LP RV710 DDR3 VGA (header) HDMI DVI	105-B890XX-00B	Thursday, August 19, 2010

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

RV710 ENGINEERING BOARD

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	2008.12.30	INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.
1	00B	2009.01.22	Sch no change. just modify HDMI connnecro location on PCB

V217 2.0 5450 1G LP (base on V161 5.1 modify)
reference
AMD 137-41731-10 reusing_rv710_boards_for cedar.pdf
and
V217-0A

+1.1V rail change to +1.0V

Page3 add connect GND pin U1,AA1,W1,AC6,AA5,AA6,AC5 for Cedar
Page4 remove DDC2 netname
add DDC3 netname
Page7 modify TESTEN for Cedar
follow V217-0A
Page8 add R78 for cedar NC pin AA11,AA12,Y11,U11,V11
add B1502 for Cedar NC use (VDDRHA/VSSRHA)
Page10 add
MR43 PD for A_VSYNC_DAC2
MR51 PD for A_VSYNC_DAC1
MR52 PD for A_HSYNC_DAC1
straps
Page13 follow V217-0A modify

Page18 DDC5 change to DDC3
Page19 remove DDC level shift parts
add LC 3 cap.
Page21 DDC2 CLK/DAT change to DDC5
remove level shift parts
Page22 add R4041 connect GPIO17

Page49 add EM104, EM105
EMI spring E23-5556060-CA7

Page3 R24 fixed reference no. issue
Page13 remove R821 5V SHUNT

Page11 change LE21 footprint
for L04-12A7651-L65 CHK_D2_11X11

PCB 2.1 update LE21 footpint
(pcb drew hole wrong size)
J2 and EC301 to close, update space
No change others layout things.

OCP set point change from 42.2K (8xA)
to 10K (4xA)

per request, VDDC low side
change from D03-004030B-N03 (P0403BDBG)
to D03-0603B2B-N03 (P0603BD)

V234 0.A 5450 1G LP (base on V217 2.1 modify)
reference

```
V234 0A
PAGE  3   Add DPC power rails back up for AMD new ASIC
PAGE  4   Use DDC2  for DAC1 VGA DDC port
PAGE  7   Add Addr 13 / QSA#0~7
PAGE 12  Change T0252 to SOP8 dual mosfet
PAGE 15  DDR3 128 x 8 Low 32bit
PAGE 16  DDR3 128 x 8 High 32bit
PAGE 22  Remove FAN control function
```

```
V234 10
PAGE 15  Change memory footprint BGA78_1
PAGE 16  Change memory footprint BGA78_1
```