

P229-B02 DESIGN

PAGE SUMMARY:

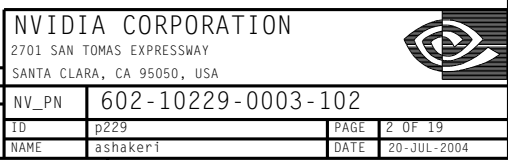
Page1: PAGE SUMMARY  
Page2: PCI EXPRESS, VDD, VDD33, VDD\_LP  
Page3: FB BANK A, FBVDDQ  
Page4: FB BANK C, FBVTT  
Page5: MEMORY 1ST BANK 0..31  
Page6: MEMORY 1ST BANK 23..6  
Page7: MEMORY 2ND BANK 0..31  
Page8: MEMORY 2ND BANK 32..63  
Page9: GND, DACA, DACB, DACC  
Page10: VGA DACA  
Page11: VGA/TV/HDTV DACB/C  
Page12: TMDS  
Page13: STRAPS, MIOA/MIOB  
Page14: XTAL, GPIO, ROM, FAN, Mechanical  
Page15: POWER SUPPLY I (Linear) FBVDDQ/A3V3/3V3/TMDSPLL/TMDSIO and POWER SEQUENCING  
Page16: POWER SUPPLY II (Switcher) NVVDD/5V/PEX1V2  
Page17: SIGNAL CROSS-REFERENCES  
Page18: PART CROSS-REFERENCES  
Page19: PART CROSS-REFERENCES

REVISION HISTORY:

- X1Initial Release
- X2Updated crystal loading capacitors.
- X3Changed the Rtrim for Green line on DACA and DACC

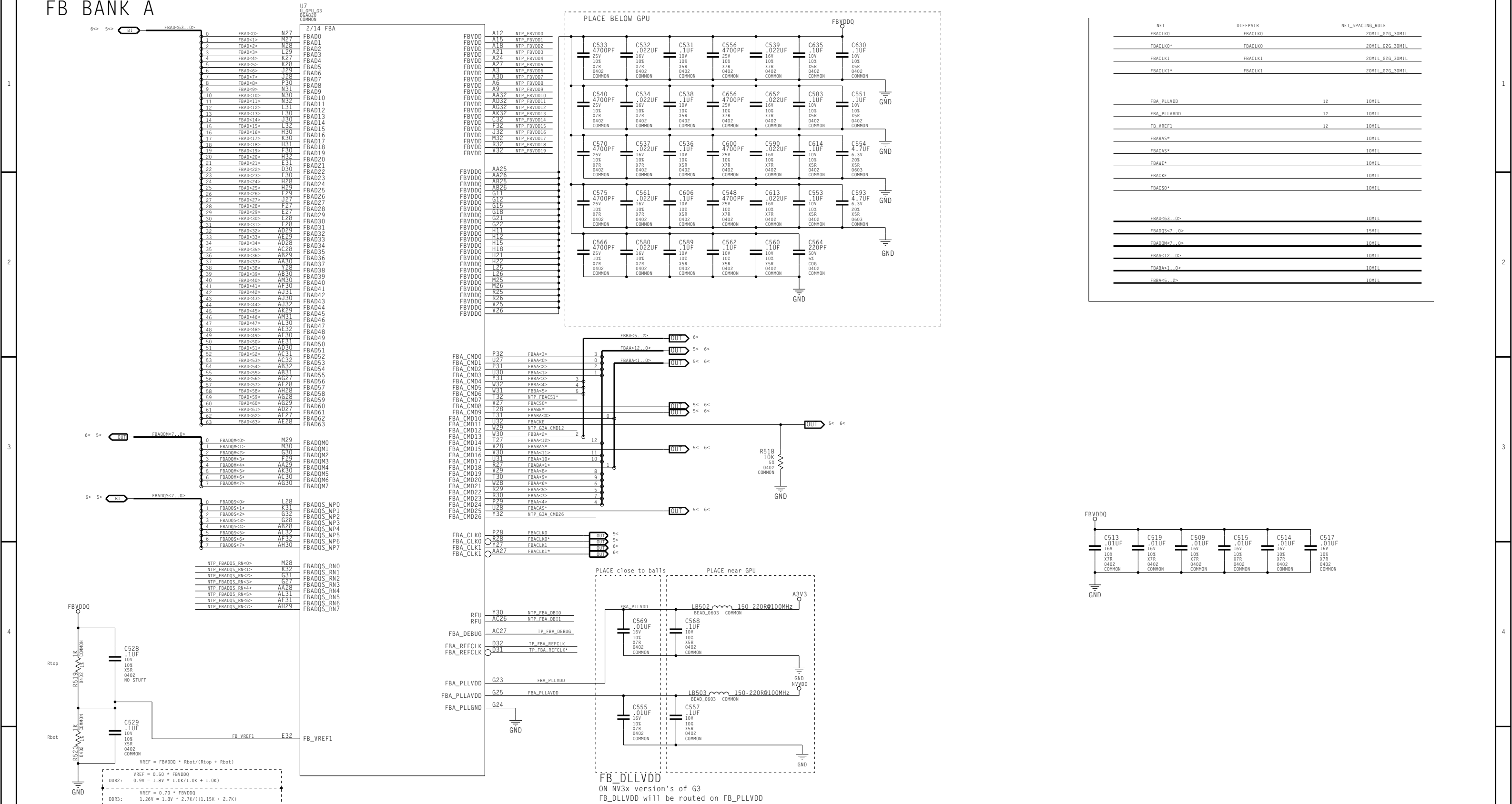
SKU	VARIANT	NVPN	ASSEMBLY
8	BASE	602-10229-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	nv43dvivgatv128m16x	602-10229-0002-102	P229-B02 NV43 GEN DVI-I/VGA/HDTV 128MB 16Mx16 TSOP
2	nv43dvivgatv128m8x	602-10229-0003-102	P229-B02 NV43 GEN DVI-I/VGA/HDTV 128MB 8Mx16 TSOP
3	43g1dvivgatv128m8x	602-50229-0001-102	P229-B02 NV43-GL GEN DVI-I/VGA/HDTV 128MB 8Mx16 TSOP
4	nv43dvivgatv256m16x	602-10229-0004-102	P229-B02 NV43 GEN DVI-I/VGA/HDTV 256MB 16Mx16 TSOP
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V3AUX CN1  
O NONPHY-X16

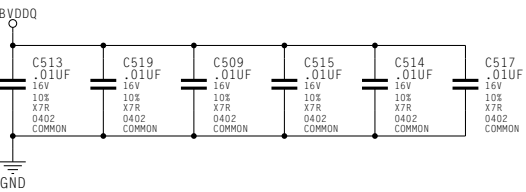


NV_PN	602-10229-0003-102		
ID	p229	PAGE	2 OF 19
NAME	ashakeri	DATE	20-JUL-2004

## FB BANK A



NET	DIFFPAIR	NET_SPACING_RULE
FBACLK0	FBACLK0	20MIL_G2G_30MIL
FBACLK0*	FBACLK0	20MIL_G2G_30MIL
FBACLK1	FBACLK1	20MIL_G2G_30MIL
FBACLK1*	FBACLK1	20MIL_G2G_30MIL
FBA_PLLVDD	12	10MIL
FBA_PLLAVDD	12	10MIL
FB_VREF1	12	10MIL
FBARAS*		10MIL
FBACAS*		10MIL
FBABWE*		10MIL
FBACKE		10MIL
FBACSD*		10MIL
FBAD<63, 0>		10MIL
FBADDS<7, 0>		15MIL
FBADDM<7, 0>		10MIL
FBAA<12, 0>		10MIL
FBABA<1, 0>		10MIL
FBBA<5, 2>		10MIL



```
FB_DLLVDD
ON NV3x version's of G3
FB_DLLVDD will be routed on FB_PLLVDD
```

FB BANK C

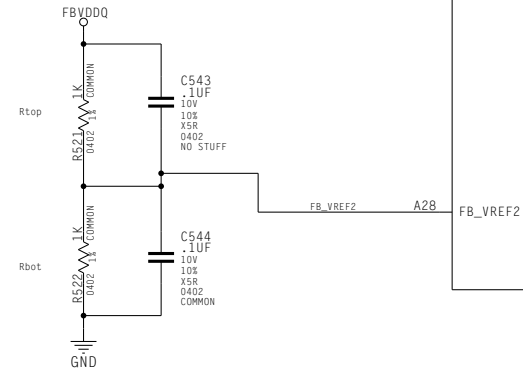
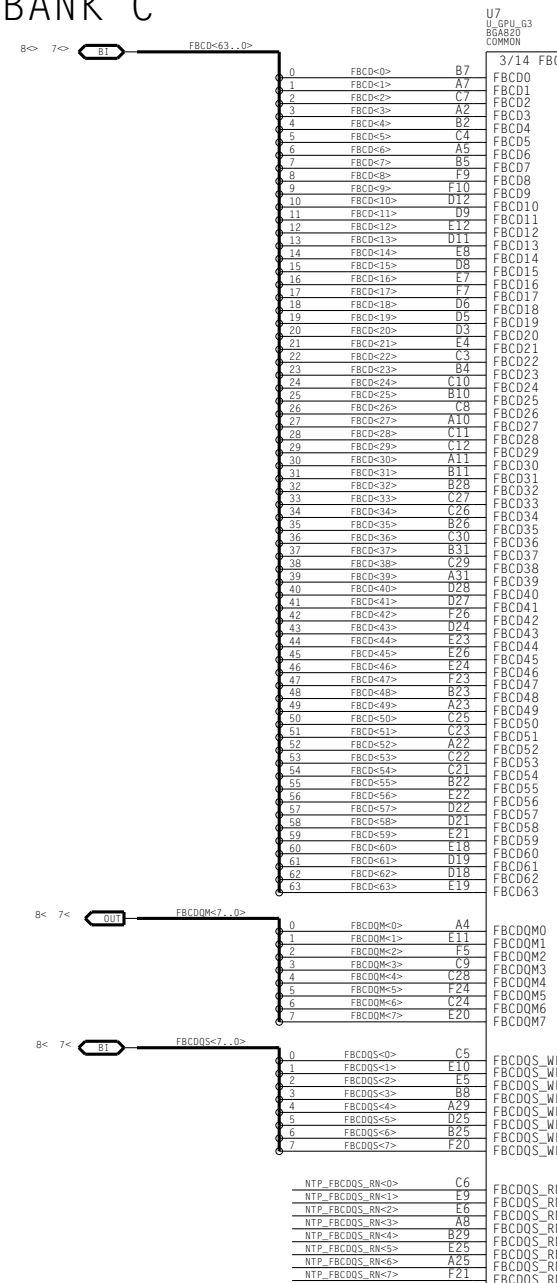
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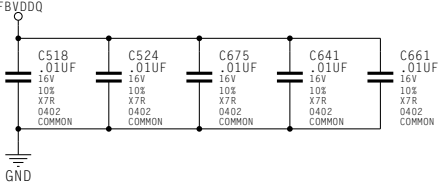
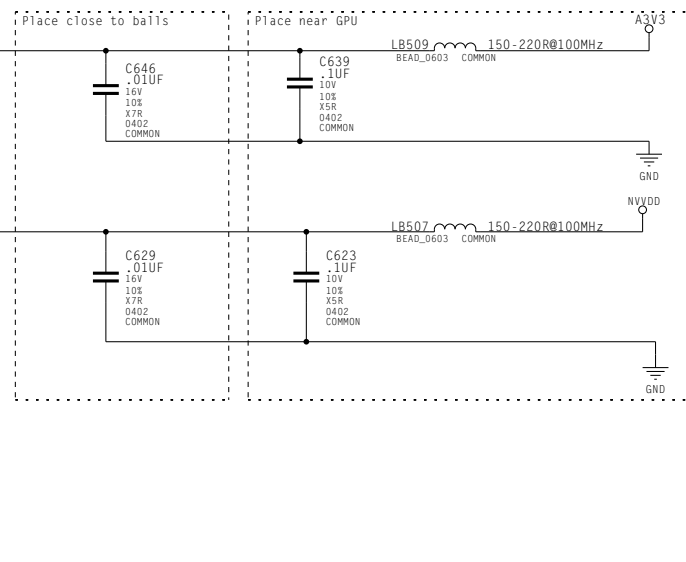
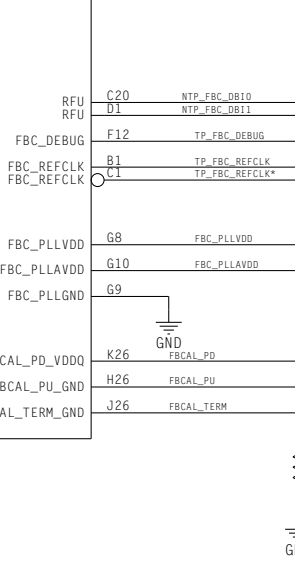
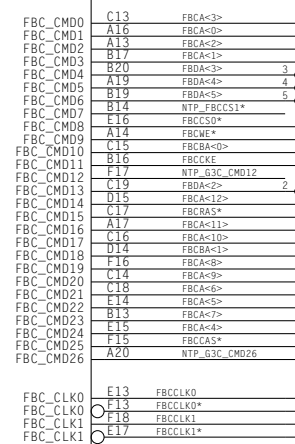
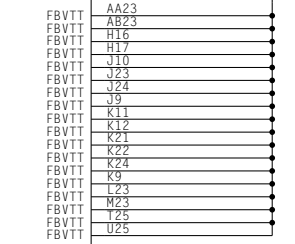
$VREF = FBVDDQ * Rbot / (Rtop + Rbot)$

$VREF = 0.50 * FBVDDQ$

DDR2:  $0.91V = 1.8V * 1.0K / (1.0K + 1.0K)$

$VREF = 0.70 * FBVDDQ$

DDR3:  $1.26V = 1.8V * 2.7K / (1.15K + 2.7K)$



NET	DIFFPAIR	NET_SPACING_RULE
FBCLK0	FBCLK0	20MIL_G2G_30MIL
FBCLK0*	FBCLK0	20MIL_G2G_30MIL
FBCLK1	FBCLK1	20MIL_G2G_30MIL
FBCLK1*	FBCLK1	20MIL_G2G_30MIL
FBC_PLLVDD		12 10MIL
FBC_PLLAVDD		12 10MIL
FBC_VREF2		12 10MIL
FBCRAS*		10MIL
FBCCAS*		10MIL
FBCWE*		10MIL
FBCCKE		10MIL
FBCCS0*		10MIL
FBCD<63..0>		10MIL
FBCDQS<7..0>		15MIL
FBCDQM<7..0>		10MIL
FBCA<12..0>		10MIL
FBCBA<1..0>		10MIL
FBDA<5..2>		10MIL
FBCAL_PD		10MIL
FBCAL_PU		10MIL
FBCAL_TERM		10MIL

1

2

3

4

5

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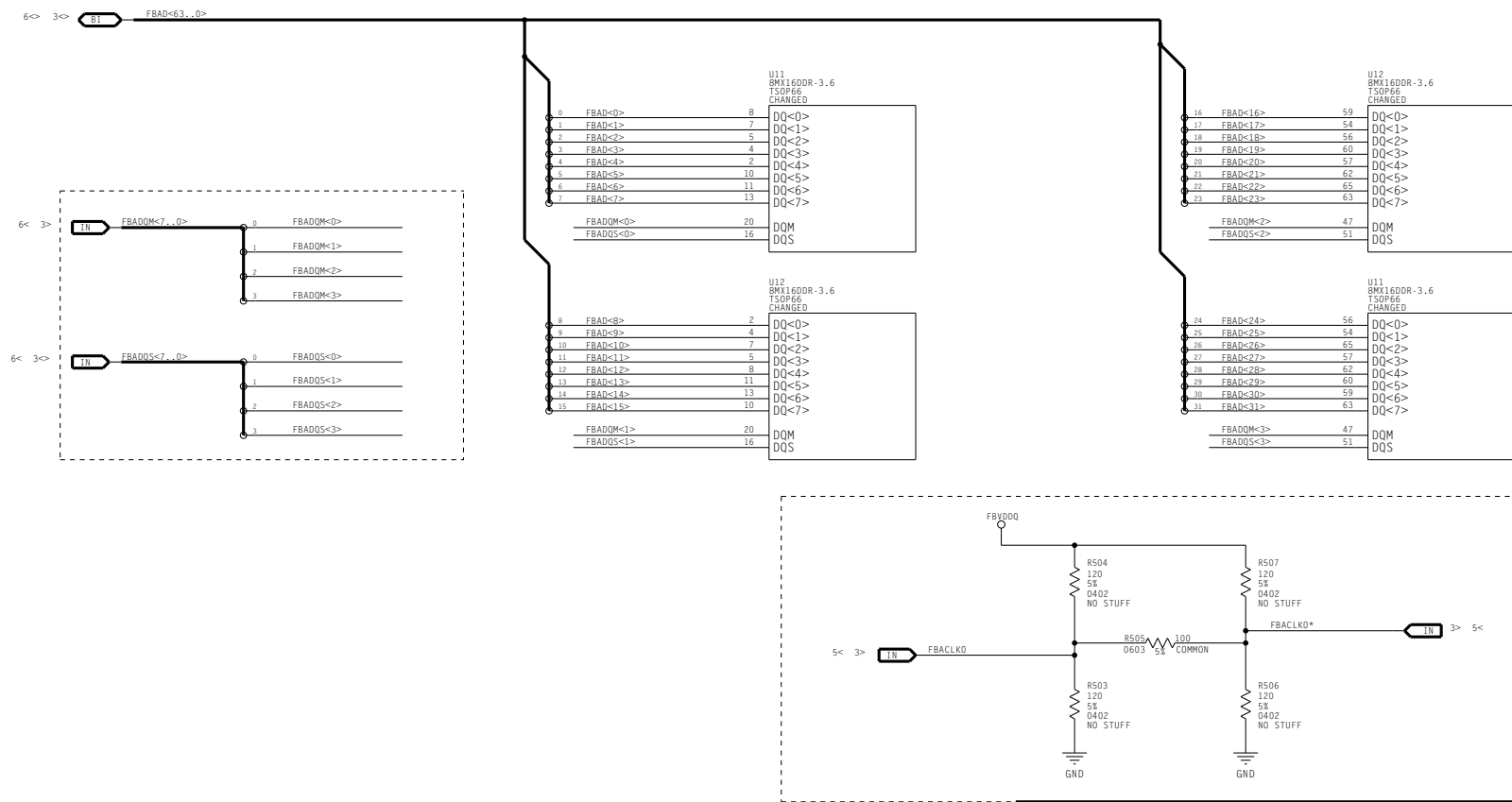
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ID p229 PAGE 4 OF 19

NAME asnakert DATE 20-JUL-2004

ASSEMBLY	P229-B02 NV43 GEN DVI-1/VGA/HDTV 128MB 8Mx16 TSOP
PAGE DETAIL	FB BANK C, FBVTT

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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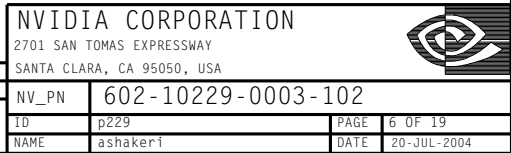
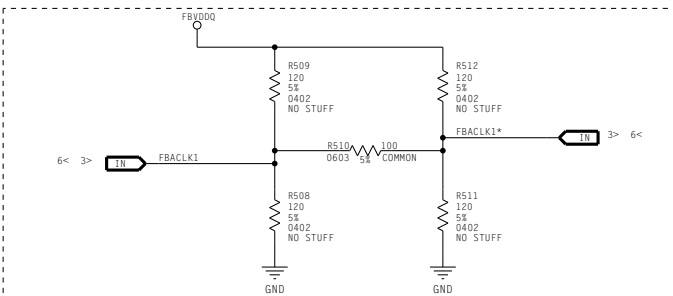
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ID	p229	PAGE	5 of 19
NAME	ashakeri	DATE	20-JUL-2004

2017-2018	2018-2019	2019-2020	2020-2021

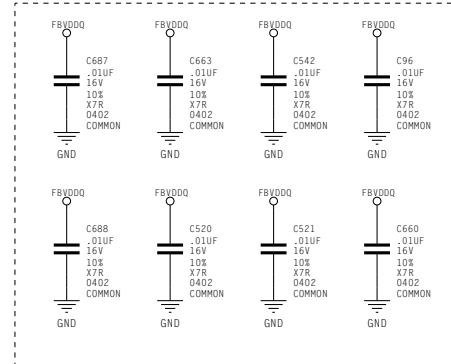
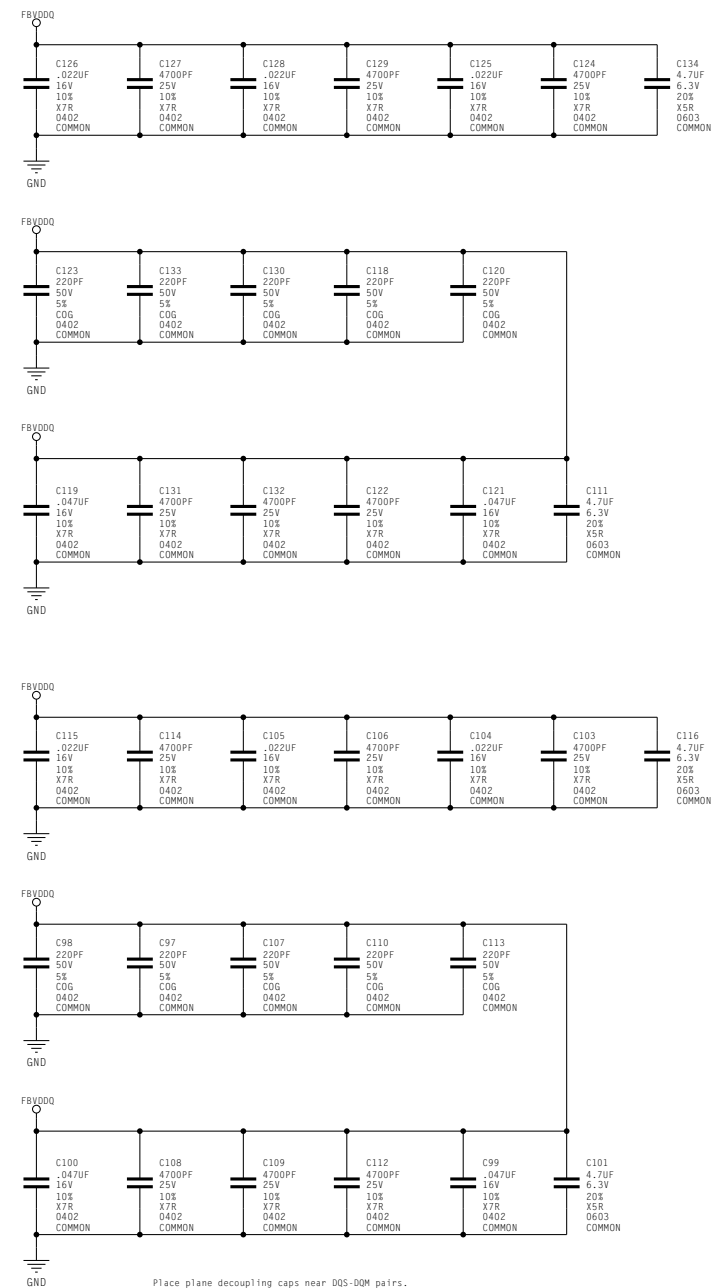
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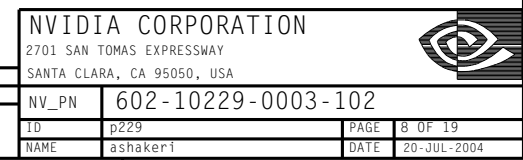
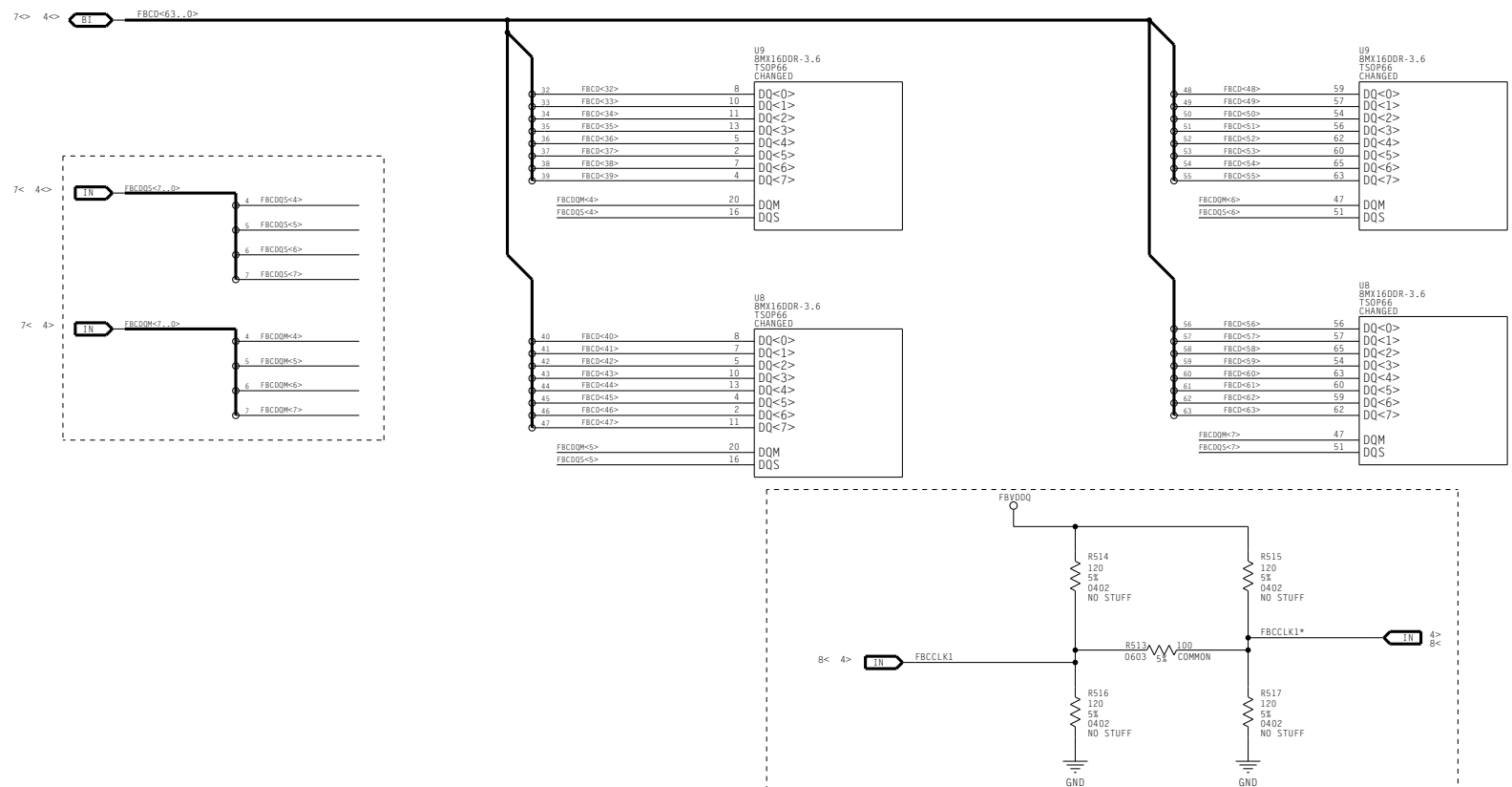
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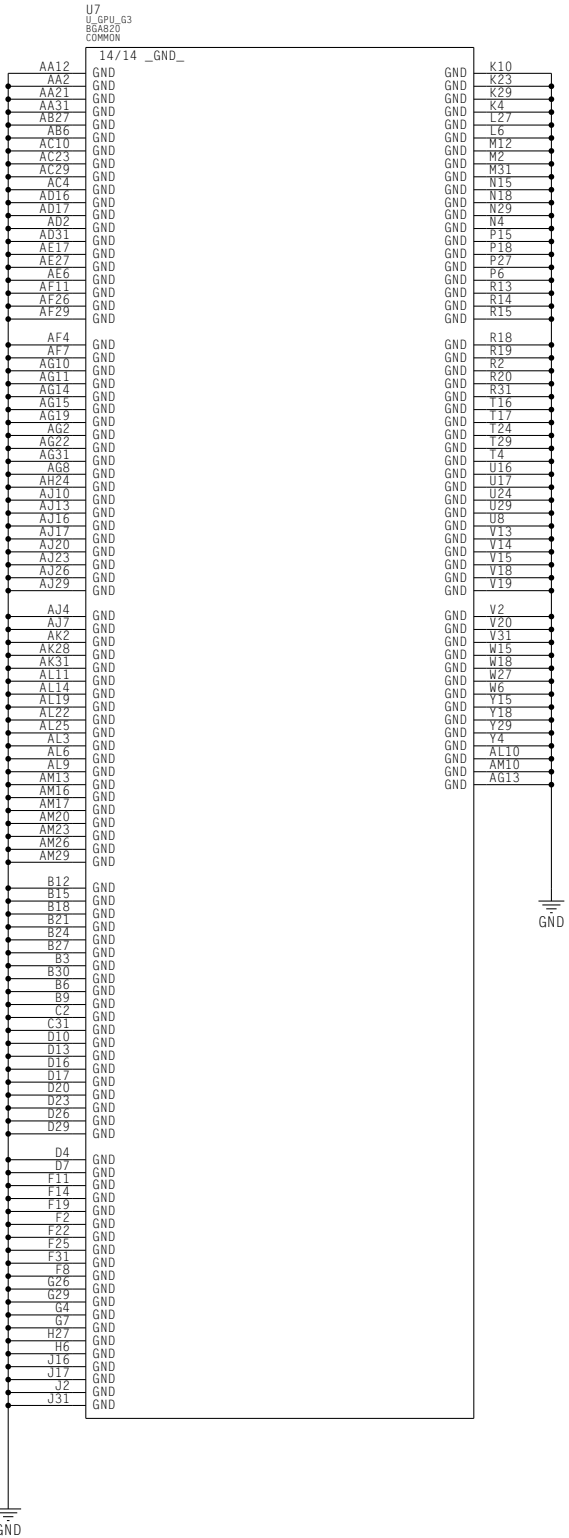
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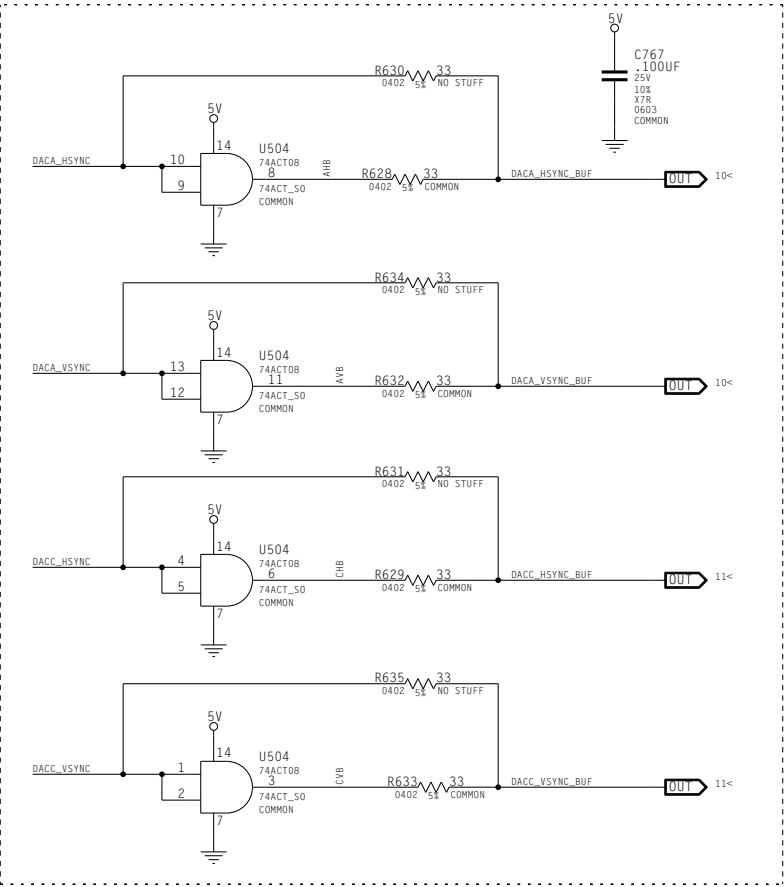
GND,DACA,DACB,DACC



NET RULES

NET_NAME	MIN_LINE_WIDTH	NET_SPACING_RULE	IMPEDANCE
I2CA_SCL		10MIL	
I2CA_SDA		10MIL	
DACA_HSYNC		10MIL	
DACA_VSYNC		10MIL	
DACA_RED		20MIL	U6_AH11:R617,1:37.50_OHM:2%
DACA_GREEN		20MIL	U6_A112:R616,1:37.50_OHM:2%
DACA_BLUE		20MIL	U6_AH12:R615,1:37.50_OHM:2%
DACA_VDD	12	10MIL	
DACA_VREF	12	10MIL	
DACA_RSET	12	10MIL	
DACB_C_OUT		20MIL	U6_R6:R641,1:37.50_OHM:2%
DACB_CVBS_OUT		20MIL	U6_TS:R608,1:37.50_OHM:2%
DACB_PB_OUT		20MIL	U6_T6:R633,1:37.50_OHM:2%
DACB_VDD	12	10MIL	
DACB_VREF	12	10MIL	
DACB_RSET	12	10MIL	
DACC_HSYNC		10MIL	
DACC_VSYNC		10MIL	
DACC_RED		20MIL	U6_AF6:R623,1:37.50_OHM:2%
DACC_GREEN		20MIL	U6_AG6:R627,1:37.50_OHM:2%
DACC_BLUE		20MIL	U6_AE5:R620,1:37.50_OHM:2%
DACC_VDD	12	10MIL	
DACC_VREF	12	10MIL	
DACC_RSET	12	10MIL	
TV_RSET_SEL	12	10MIL	
I2CB_SDA		10MIL	
I2CB_SCL		10MIL	
SEL_AND_DEV		10MIL	
AHB		10MIL	
AVB		10MIL	
DACA_HSYNC_BUF		10MIL	
DACA_VSYNC_BUF		10MIL	
CHB		10MIL	
CVB		10MIL	
DACC_HSYNC_BUF		10MIL	
DACC_VSYNC_BUF		10MIL	

DACA & DACC Sync Buffers



ASSEMBLY	P229-B02 NV43 GEN DVI-1/VGA/HDTV 128MB 8Mx16 TSOP
PAGE DETAIL	GND, DACA, DACB, DACC

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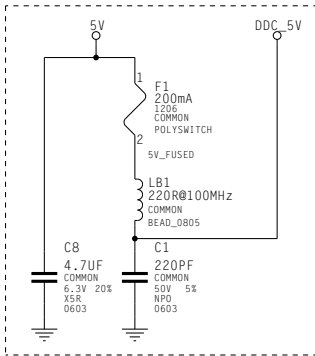
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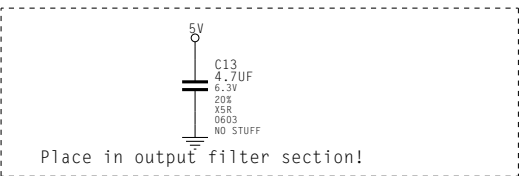
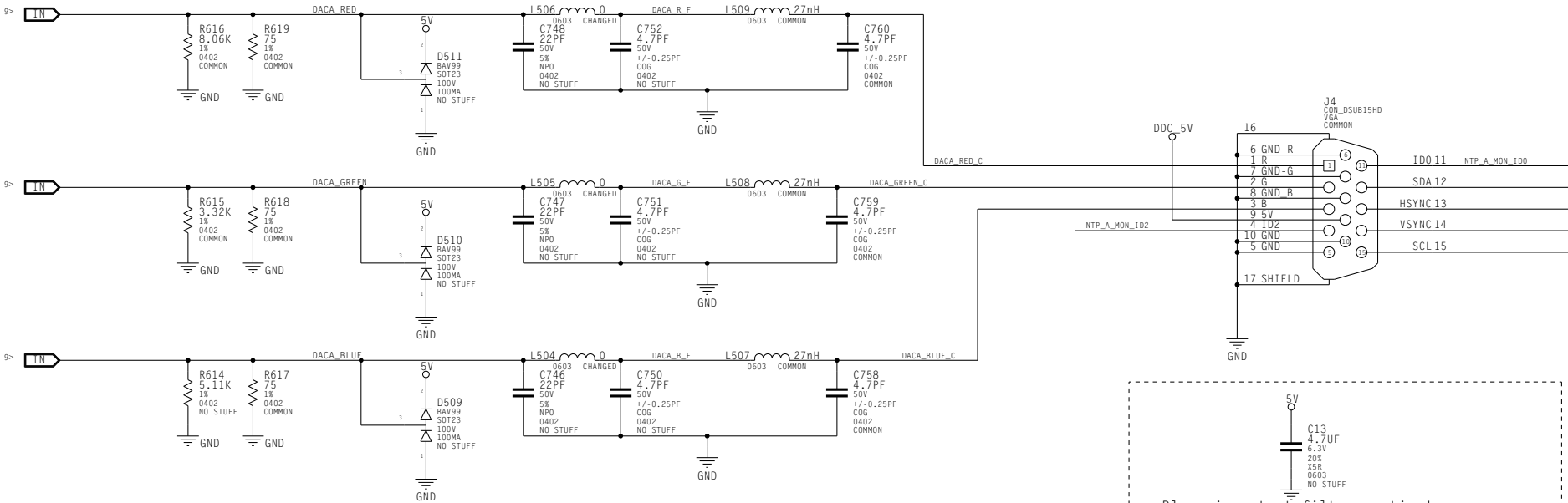
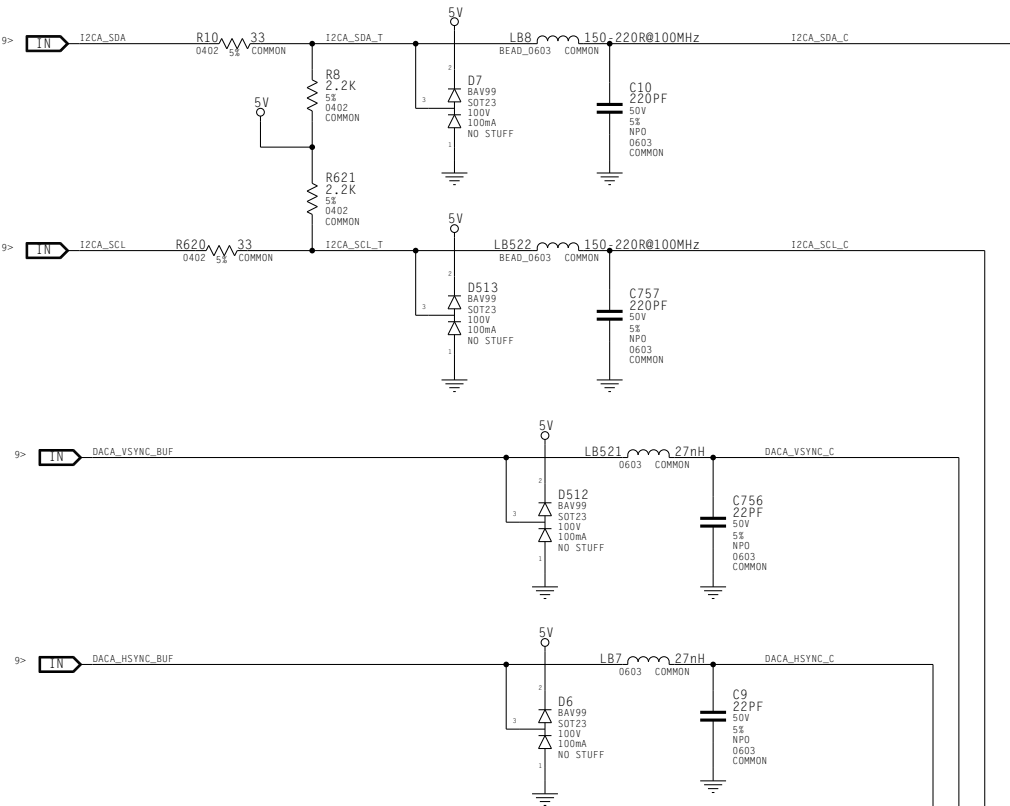
NV_PN	602-10229-0003-102		
ID	p229	PAGE	9 OF 19
NAME	ashakeri	DATE	20-JUL-2004

VGA DACA

DDC 5V



Changed the FUSE to 200mA



NET_NAME	NET_SPACING_RULE
DACA_R_F	20MIL
DACA_G_F	20MIL
DACA_B_F	20MIL
DACA_RED_C	20MIL
DACA_GREEN_C	20MIL
DACA_BLUE_C	20MIL
DACA_VSYNC_C	10MIL
DACA_HSYNC_C	10MIL

	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	16	5V
5V	16	5V
DDC_5V	16	5V
A3V3	16	3.3V
GND	16	0V

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PAGE DETAIL

VGA DACA

NV\_PN

602-10229-0003-102

ID

p229

PAGE

10 OF 19

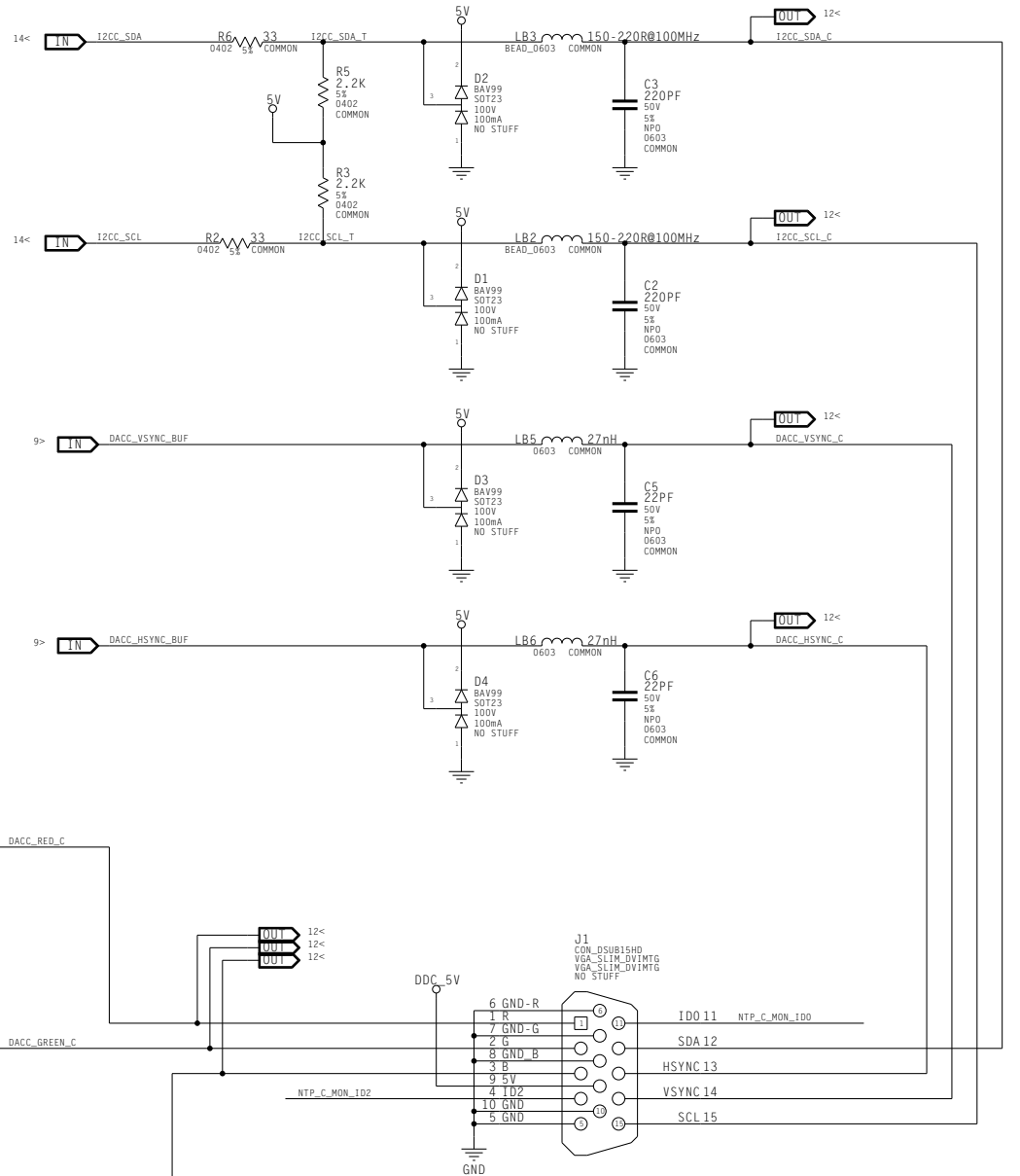
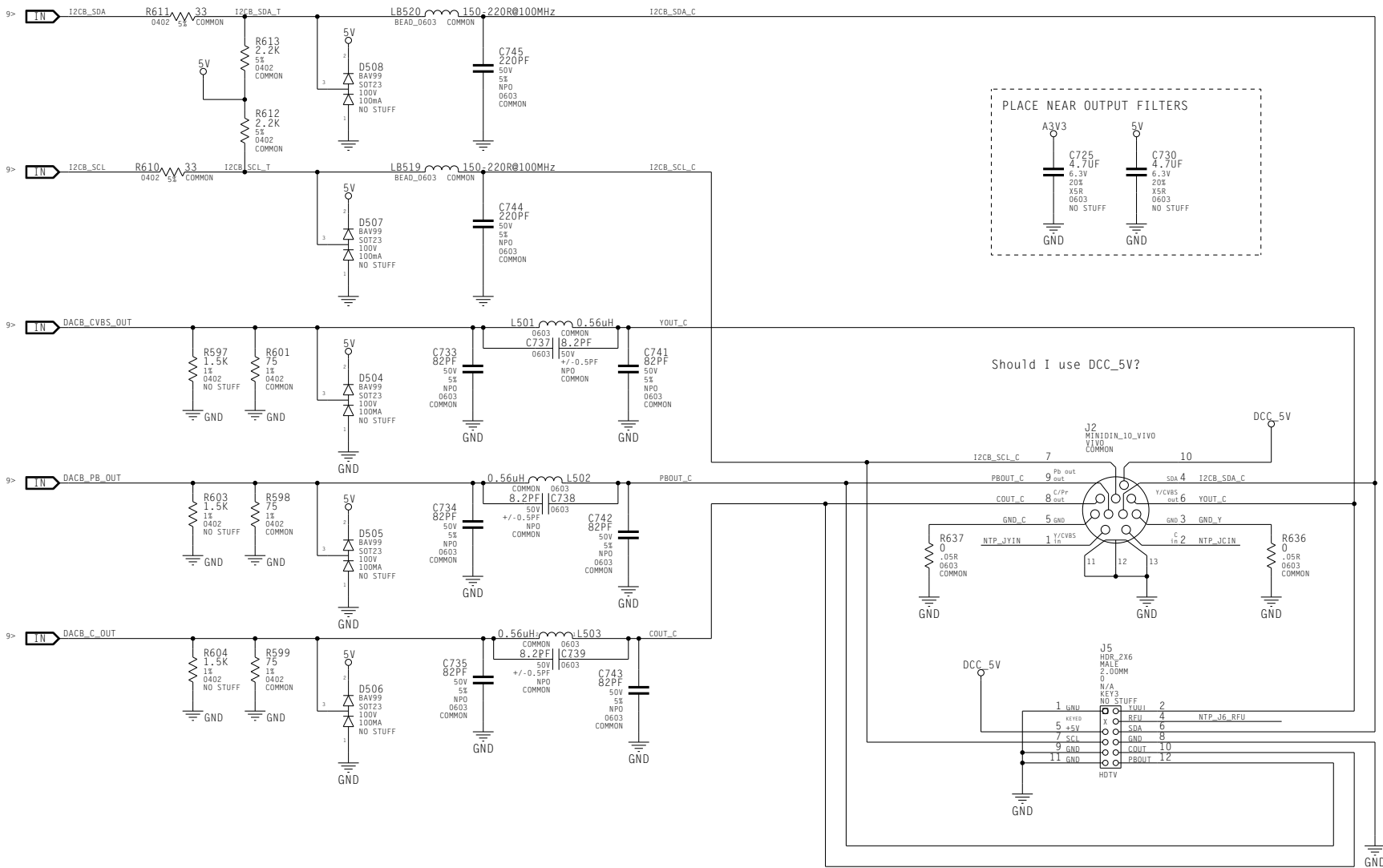
NAME

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DATE

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# VGA/TV Out/HDTV DACB/C



NET_NAME	NET_SPACING_TYPE
DACC_R_F	20MIL
DACC_G_F	20MIL
DACC_B_F	20MIL
DACC_RED_C	20MIL
DACC_GREEN_C	20MIL
DACC_BLUE_C	20MIL
DACC_RED_SW	20MIL
DACC_GREEN_SW	20MIL
DACC_BLUE_SW	20MIL
COU_T	20MIL
YOUT	20MIL
PBOUT	20MIL
DACC_VSYNC_C	10MIL
DACC_HSYNC_C	10MIL
COU_T_C	20MIL
YOUT_C	20MIL
PBOUT_C	20MIL

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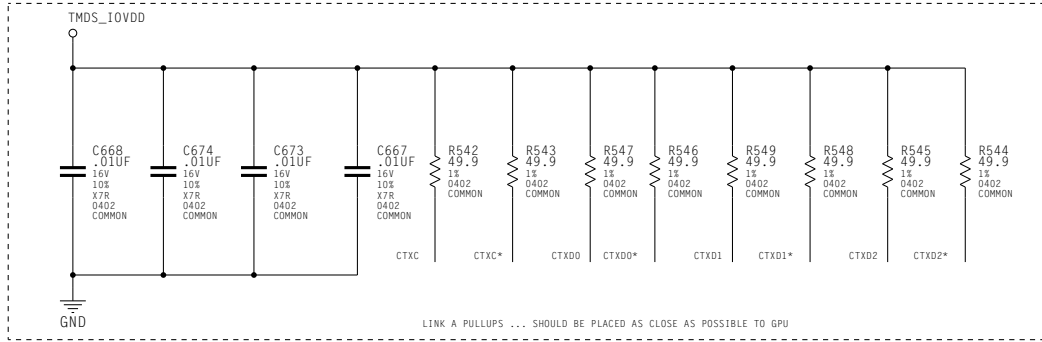
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ID	p229	PAGE	11 OF 19
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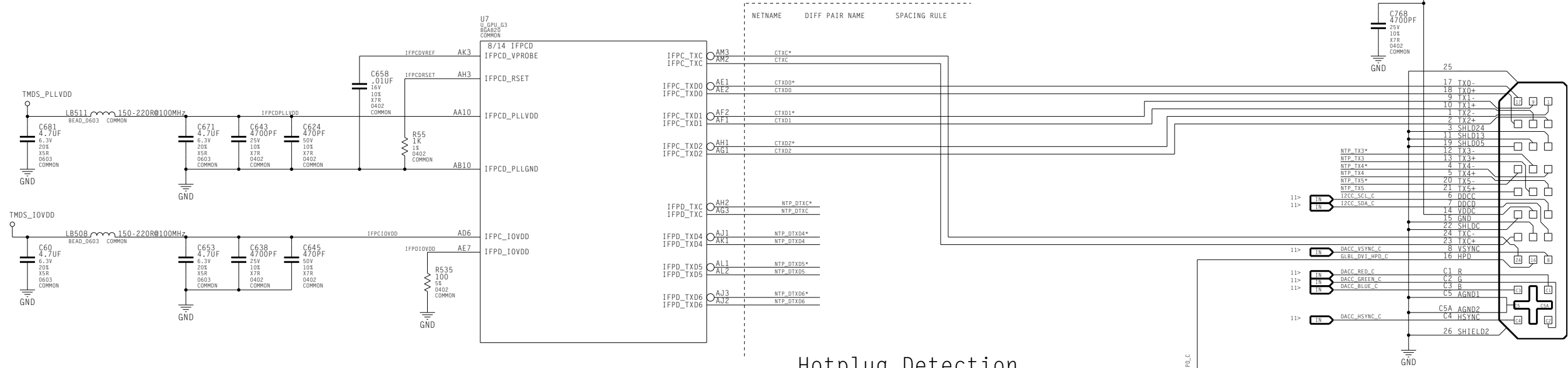
INTERNAL TMDS



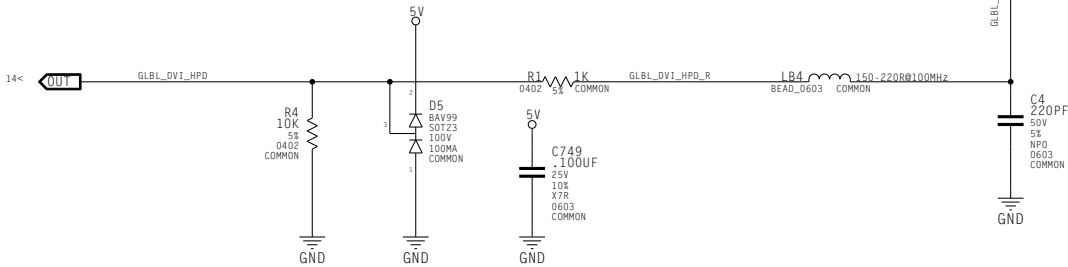
NET	MIN_LINE_WIDTH	VOLTAGE
IFPCDVREF	12	3.3V
IFPCPLLVD0	12	3.3V
IFPCIOVDD	12	3.3V

NETNAME	DIFF PAIR NAME	SPACING RULE
CTXC*	CTXC	20MIL_62G_30MIL
CTXC	CTXC	20MIL_62G_30MIL
CTXD0*	CTXD0	20MIL_62G_30MIL
CTXD0	CTXD0	20MIL_62G_30MIL
CTXD1*	CTXD1	20MIL_62G_30MIL
CTXD1	CTXD1	20MIL_62G_30MIL
CTXD2*	CTXD2	20MIL_62G_30MIL
CTXD2	CTXD2	20MIL_62G_30MIL

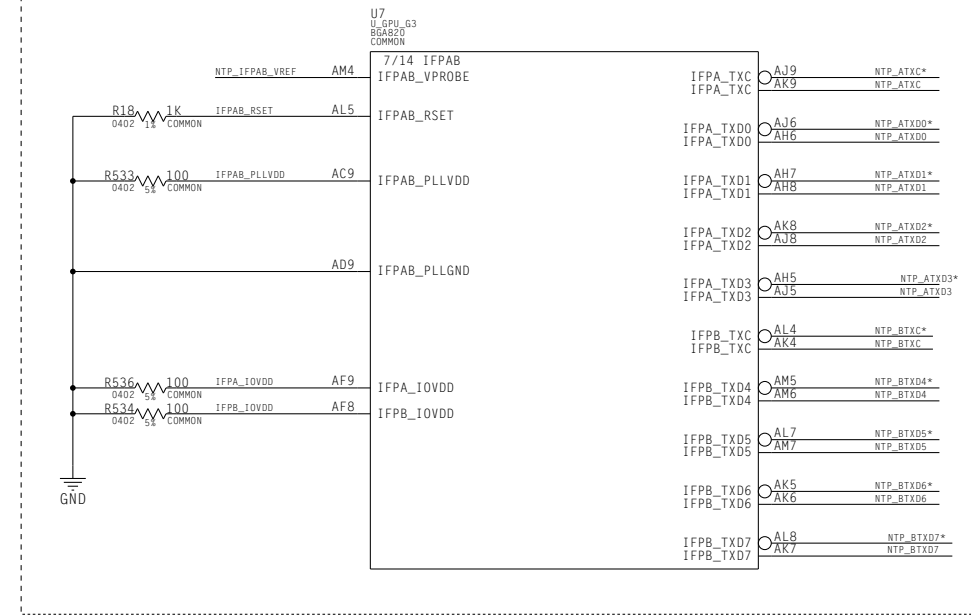
INTERNAL TMDS ..LINK C/D



Hotplug Detection



TMDS CHANNEL A & B



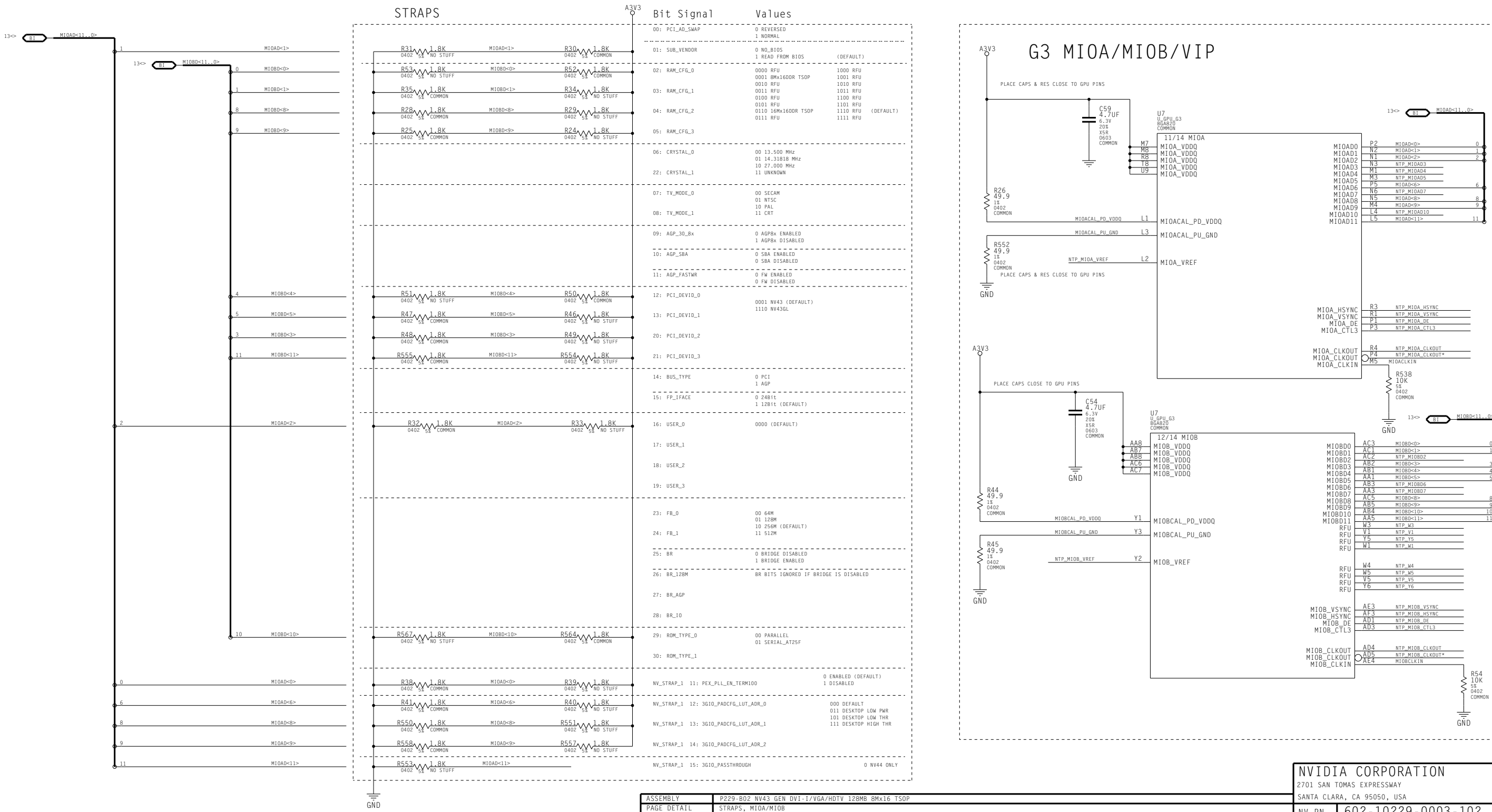
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ID	p229	PAGE	12 OF 19
NAME	ashaker1	DATE	20-JUL-2004

STRAPS, MIOA/MIOB

STRAPS

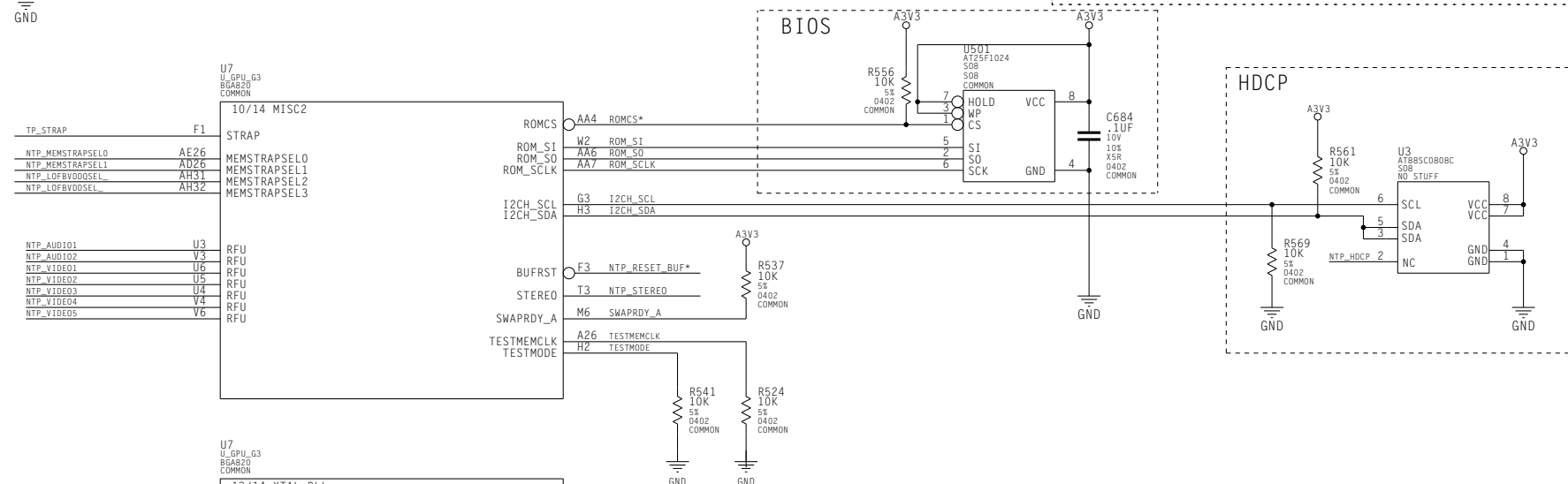
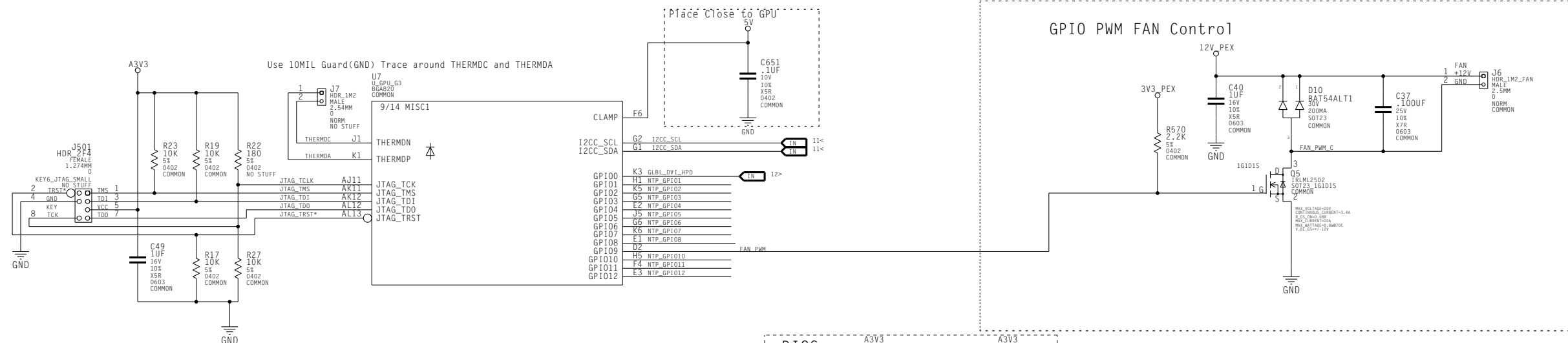
MIOs



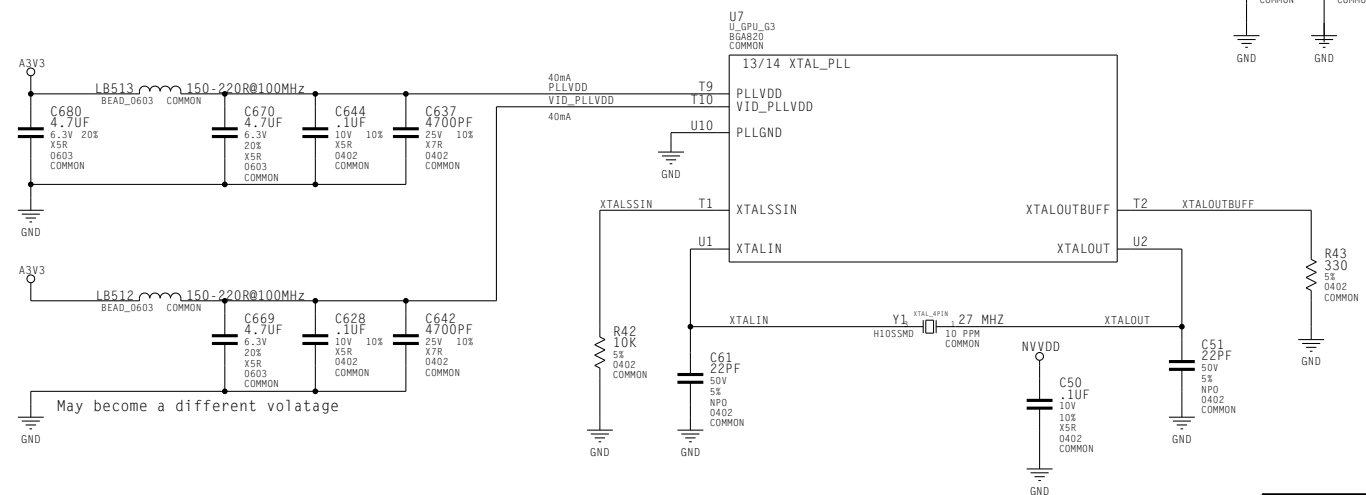
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XTAL, GPIO, ROM

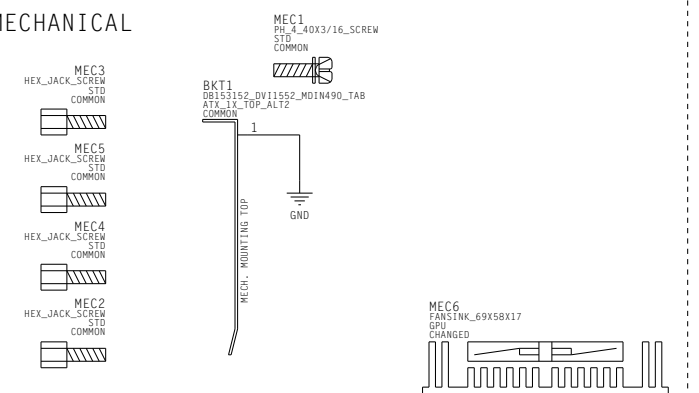
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XTALIN		20MIL
XTALOUT		20MIL
PLLVD	12	10MIL
VID_PLLVD	12	10MIL
FAN_PWM		20MIL
FAN_PWM_B		20MIL
FAN_PWM_c		20MIL
THERMDC	10	
THERMDA	10	



## XTAL/PLLVD




## MECHANICAL



Place the cap near the crystal

ASSEMBLY	P229-B02 NV43 GEN DVI-I/VGA/HDTV 128MB 8Mx16 TSOP
PAGE DETAIL	XTAL, GPIO, ROM, FAN, Mechanical

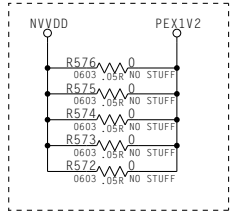
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<b>NAME</b>	ashakeri	<b>DATE</b>	20-JUL-2004



Power Supply II (ISL6534)

1V2 NVVDD bypass



PEX1V2 = 1.2V @ 3A

Net Name	MIN_LINE_WIDTH	VOLTAGE
5V	16	5V
NVVDD	16	1.35V
12V_PEX	20	12V
PEX1V2	20	1.2V
12V_PEX_FLTRD	20	12V
DRIVE3_1V2	20	
UGATE_1	20	
UGATE_2	20	
UGATE_1_RG	20	
UGATE_2_RG	20	
COMP1_RC	10	
COMP2_RC	10	
FB1_NVVDD	10	
FB2_5V	10	
FB3_1V2	10	
REFIN_5V	10	
ISL_REFOUT	10	
VREF_5V3	10	
FB3_RC	10	
BOOT_1	20	
BOOT_2	20	
FREQ_SET	10	
SS_NVVDD	10	
SS_5V	10	
SS_1V2	10	
UGATE_1_RG	20	
UGATE_2_RG	20	
COMP1_RC	10	
COMP2_RC	10	
NVVDD_RC	10	
5V_RC	10	
NODE_1_SNUB	20	
NODE_2_SNUB	20	
CLGATE_1	20	
BOOT1	20	
5VBOOST	20	

ALT Placement

NVVDD = 1.35V @ upto 18A

ALT Placement

5V = 5V @ upto 2A

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ID	p229	PAGE	16 OF 19
NAME	ashaker1	DATE	20-JUL-2004

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1

2

3

4

5

\*\*\* Signal Cross-Reference for the entire design \*\*\*

3V3ENABLE15.2A< 15.2F< 15.3F< 15.4C> 15.4F< 16.4C<

DACA\_BLUE9.1G 9.2F> 10.5A<

DACA\_GREEN9.1G 9.2F> 10.4A<

DACA\_HSYNC9.1G 9.2F> 9.3F

DACA\_HSYNC\_BUF9.2G 9.3H> 10.3C<

DACA\_RED9.1G 9.2F> 10.3A<

DACA\_VSYNC9.1G 9.2F> 9.3F

DACA\_VSYNC\_BUF9.2G 9.4H> 10.2C<

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DACC\_GREEN9.2G 9.4F> 11.4A<

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DACC\_HSYNC\_C11.1G 11.3H> 12.3F<

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DACC\_VSYNC9.2G 9.4F> 9.5F

DACC\_VSYNC\_BUF9.2G 9.5H> 11.3F<

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ASSEMBLYP229-B02 NV43 GEN DVI-I/VGA/HDTV 128MB 8Mx16 TSOP

PAGE DETAIL<edit here to insert page detail>

NV\_PN602-10229-0003-102

IDp229PAGE17 OF 19

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