

MS-V080 -- G72 7300GS, 128/256 MB 64bit DDR2-84pin, DVI-I,HDMI

P381: G72, DDR2 MEMORY 16Mx16

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Base on P381_ A04 (V056-V3.0)modify

- Page8, removed mini-din 4pin. add mini-din 7pin support HDTV
- Page 13: PowerSupplyI: NVVDD, A3V3 add mlcc 10U/16V 1206 5pcs
remove L5 L6 R7 R8 R9 ,D9
- Page 9: ADD 預留 R593,R594,R595,R596 FOR EMI
- Page 14: ADD 預留 R655,R656,R657,R658 FOR EMI
- Page 12: Remove C8 EL Cap and change Q1 MOSFET package to T0252

PLACE NEAR FINGERS

3V3

C24 0.1uF

C22 0.1uF

C23 0.1uF

0V

COMMON

COMMON

COMMON

5V

C51 4.7uF

C56B 4.7uF

C56F 4.7uF

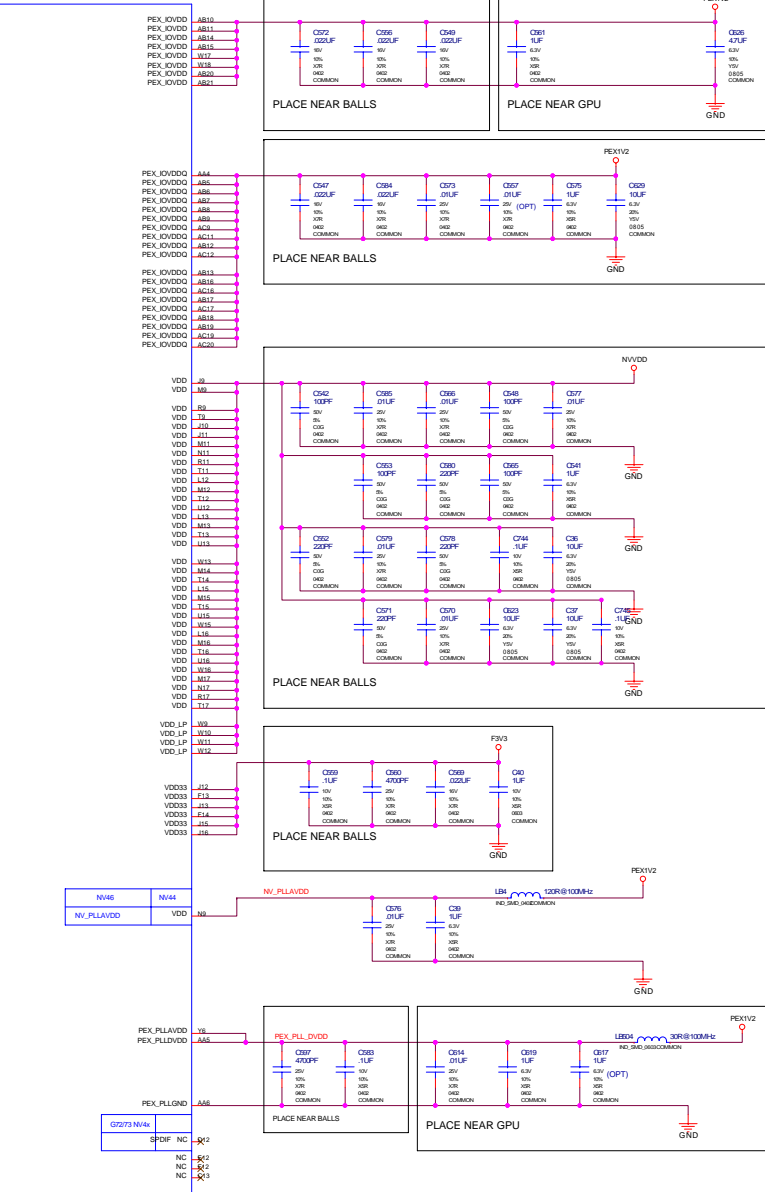
0V

COMMON

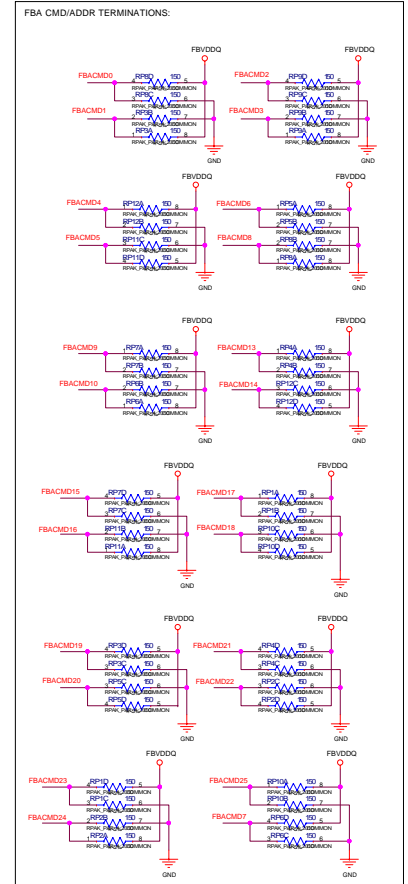
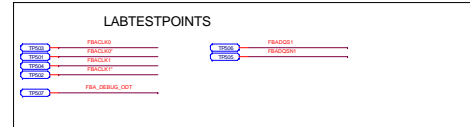
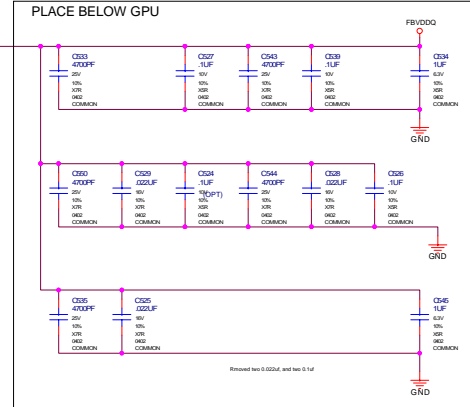
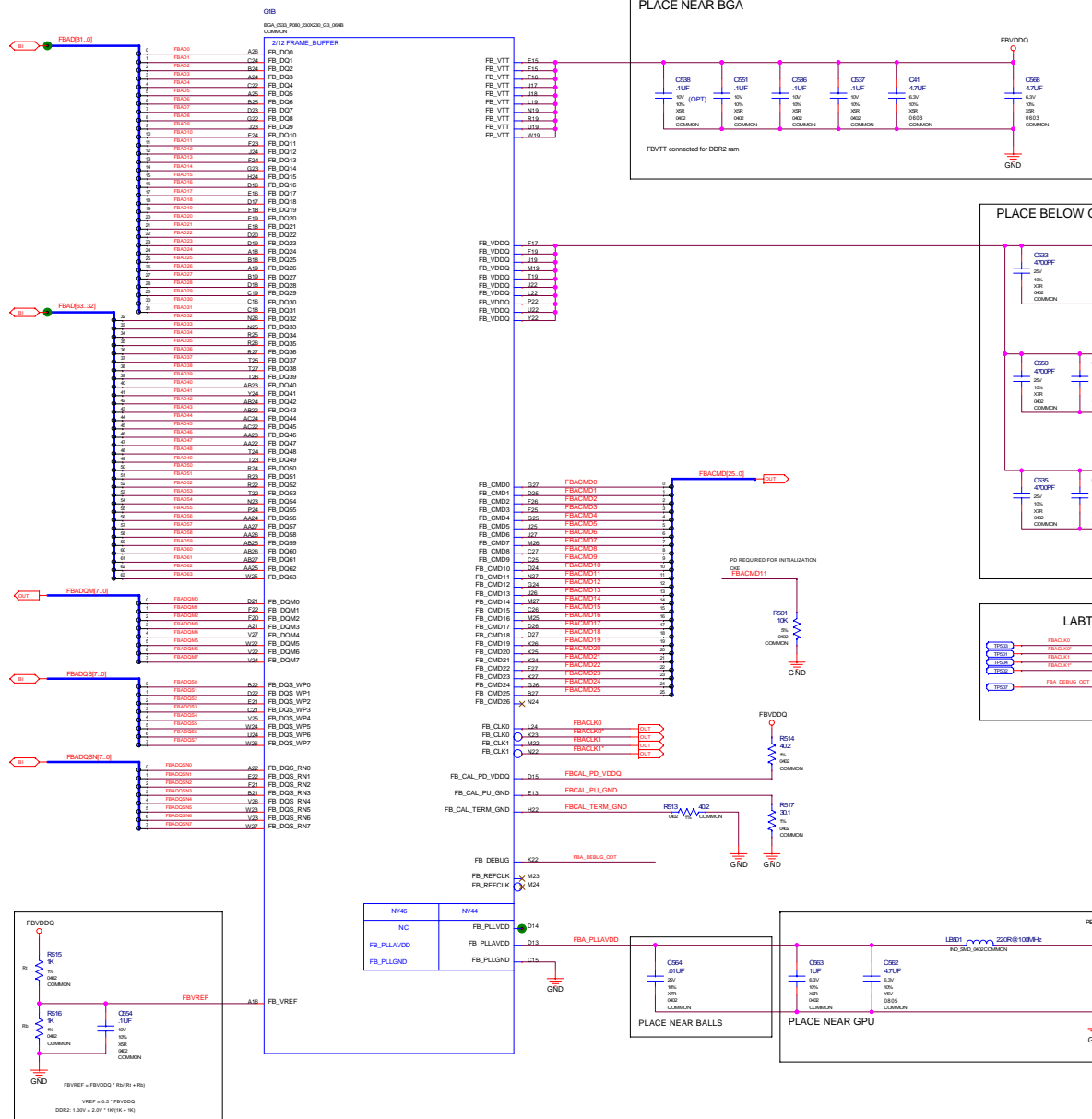
COMMON

COMMON

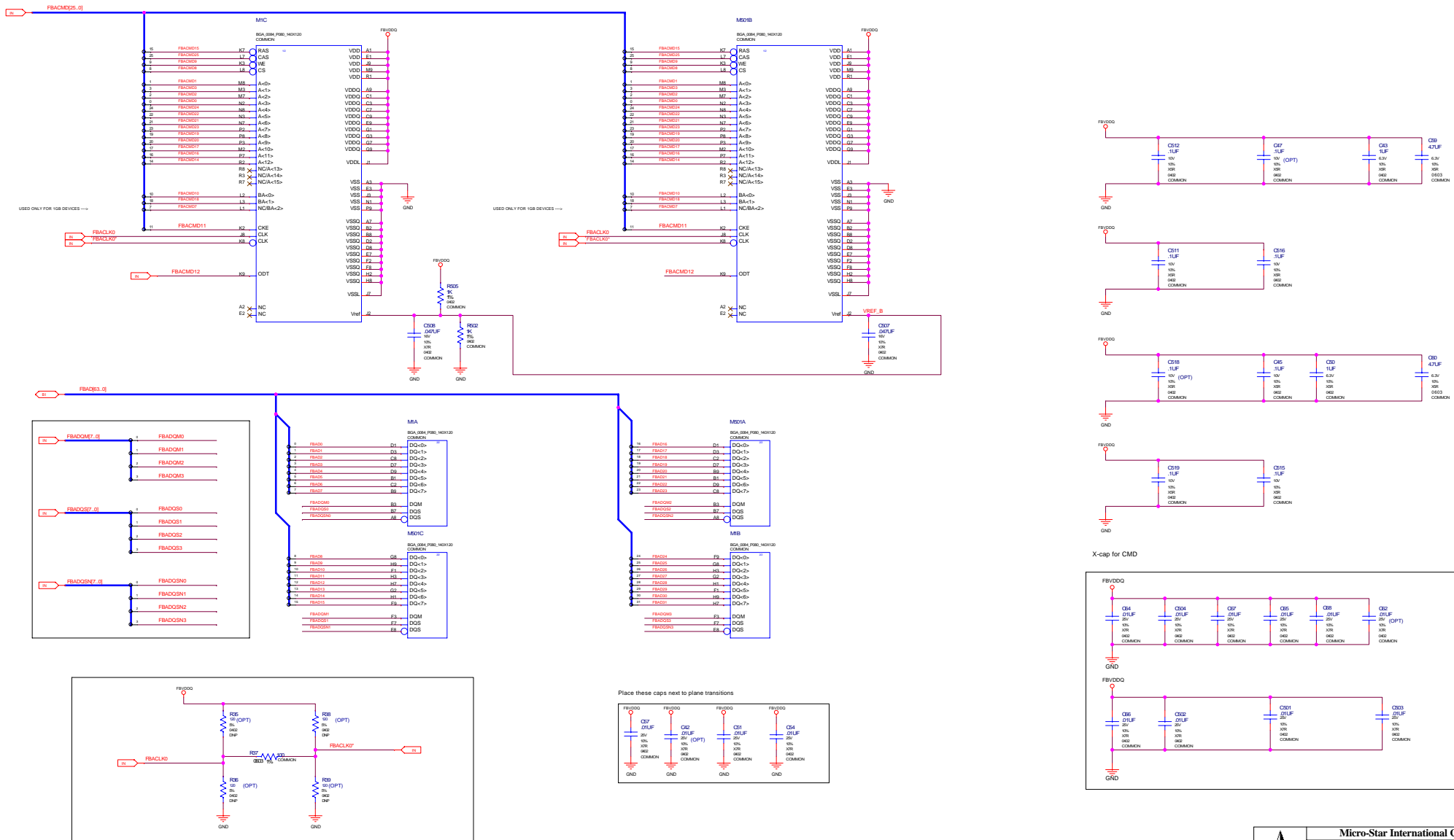
3V3



GPU: FB-Interface

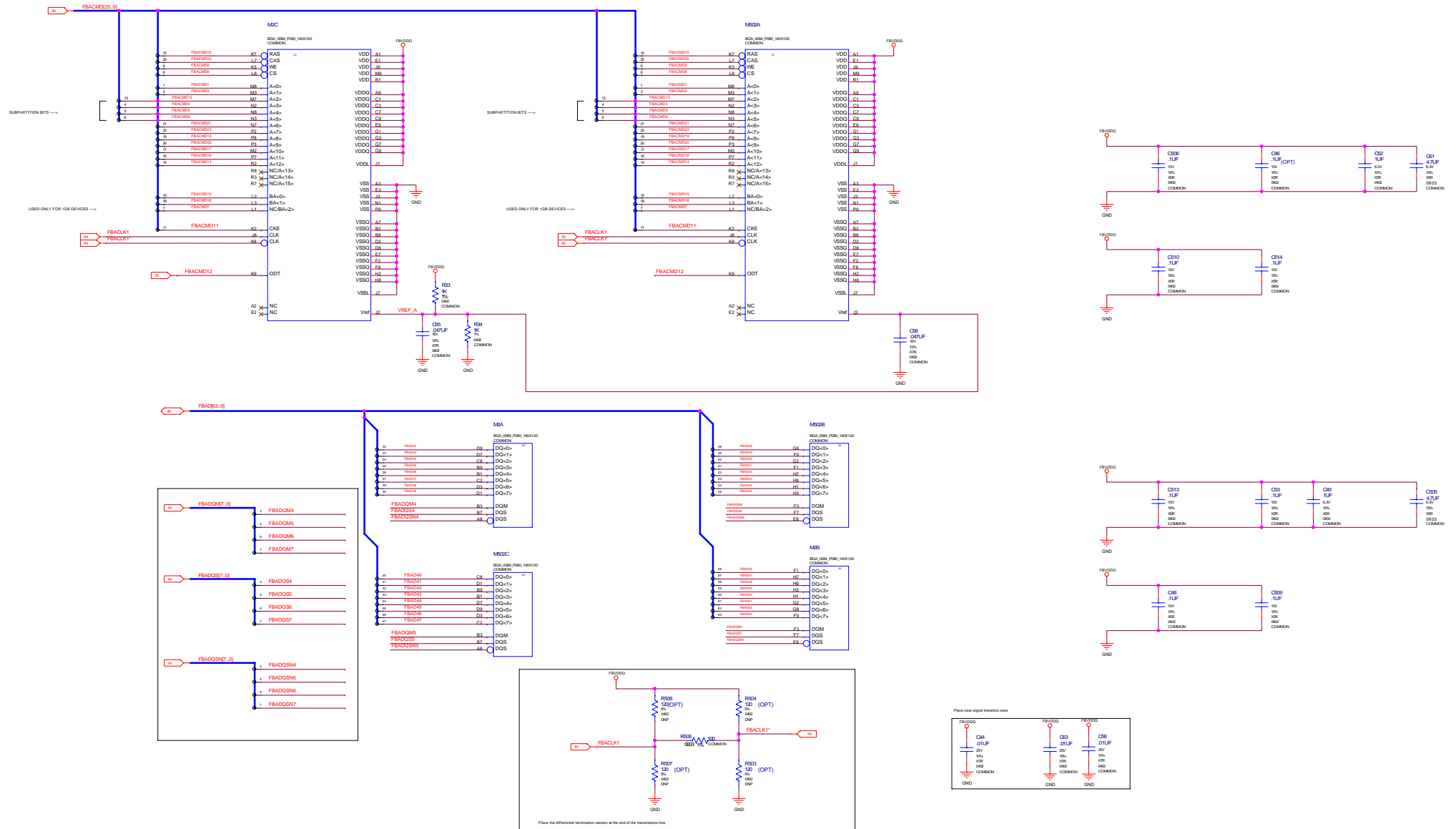


PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

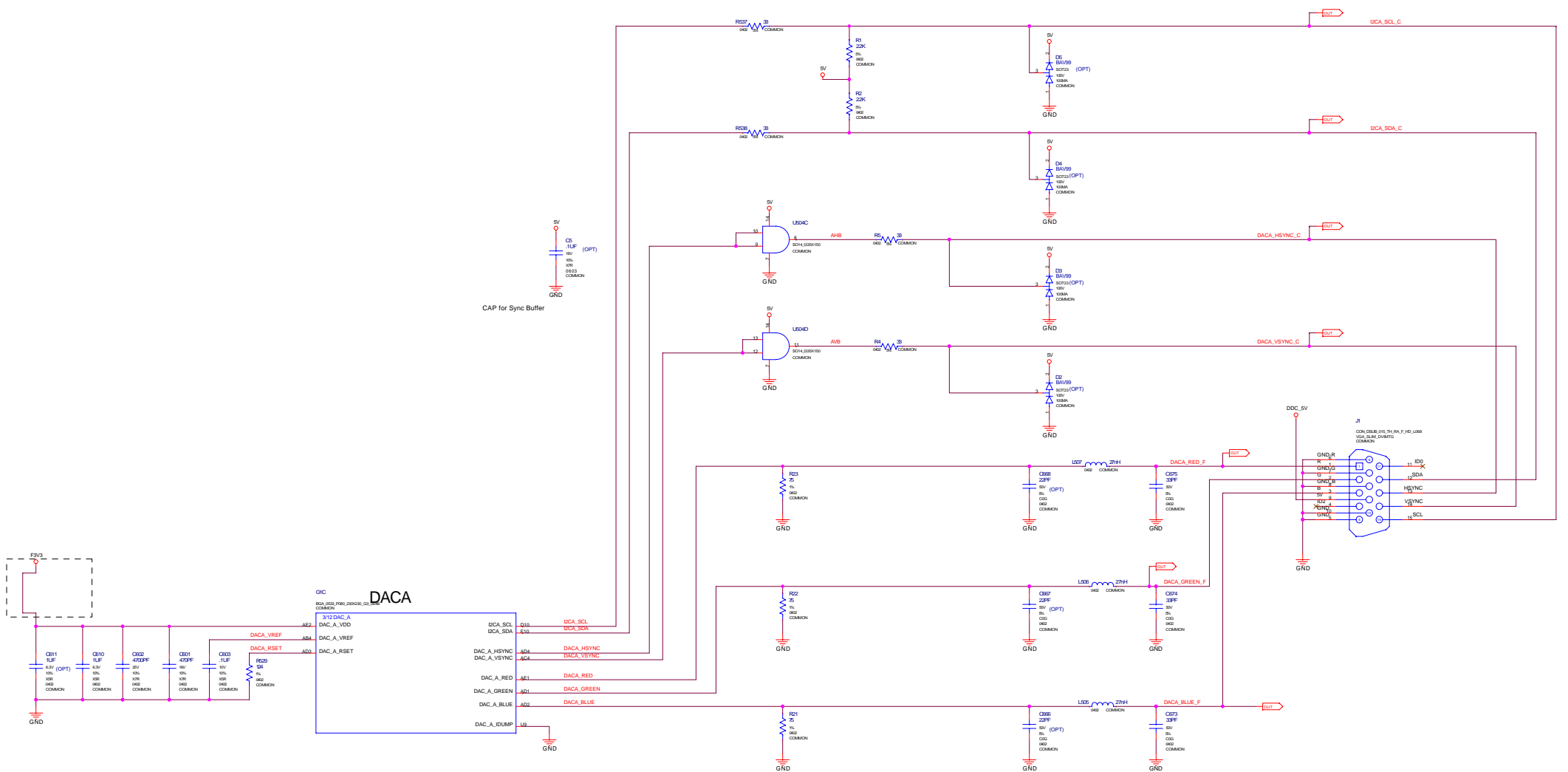


Memory Bit 32..63

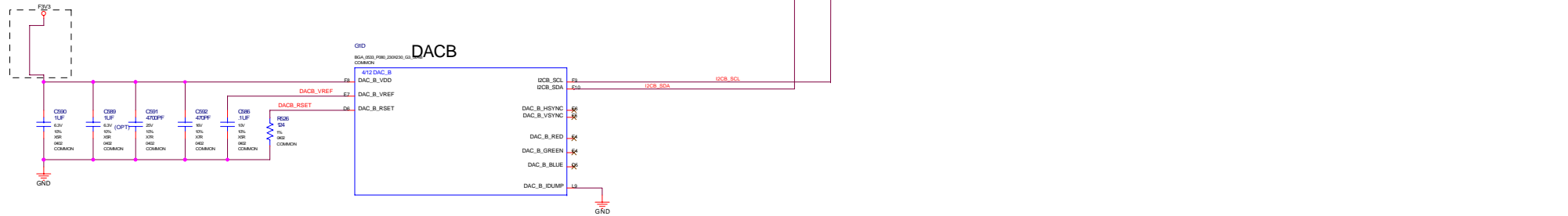
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



DAC-A, DB15 Connector



DAC-B

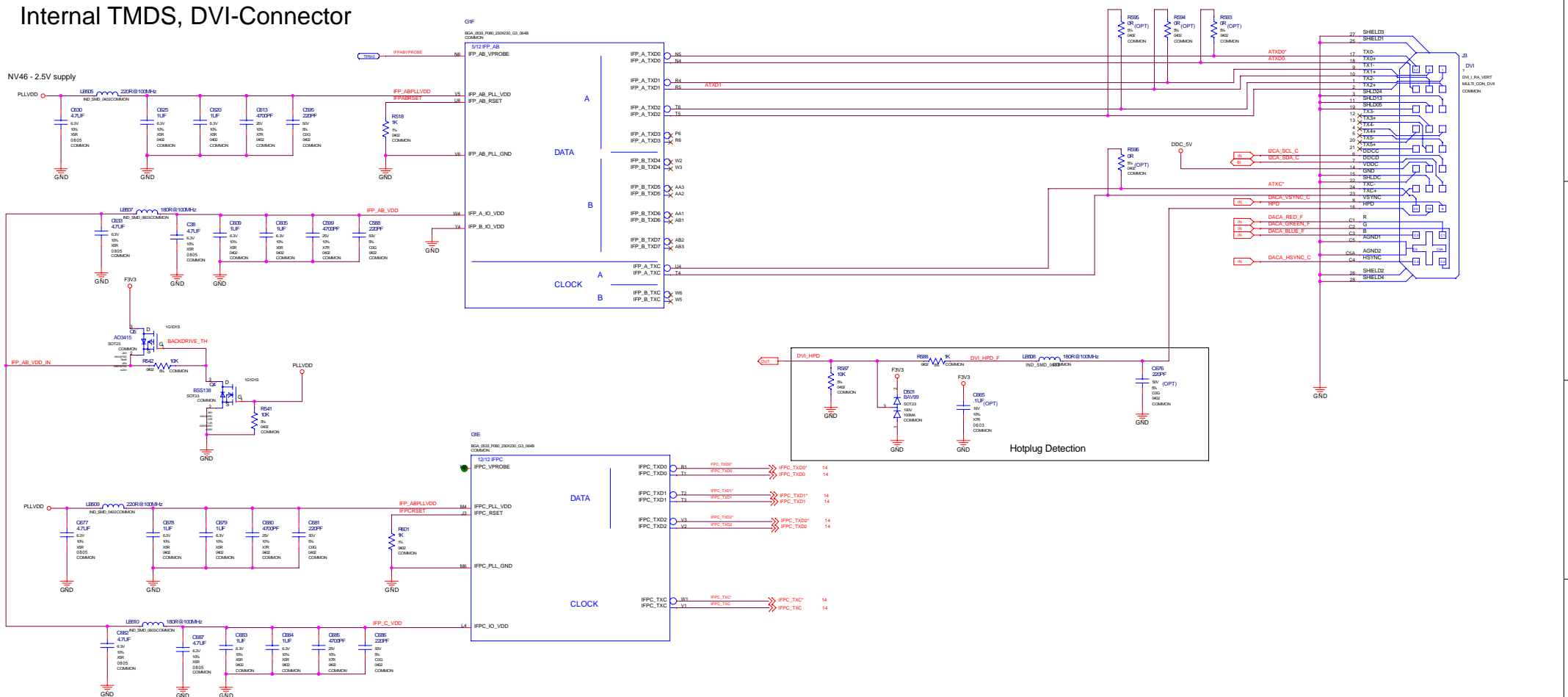


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DAC-B

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Internal TMDS, DVI-Connector



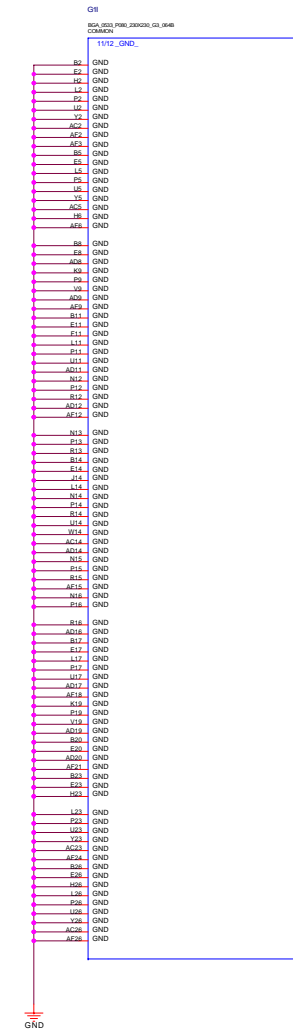
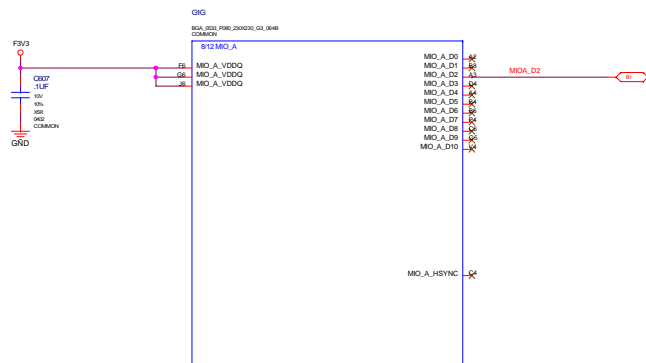
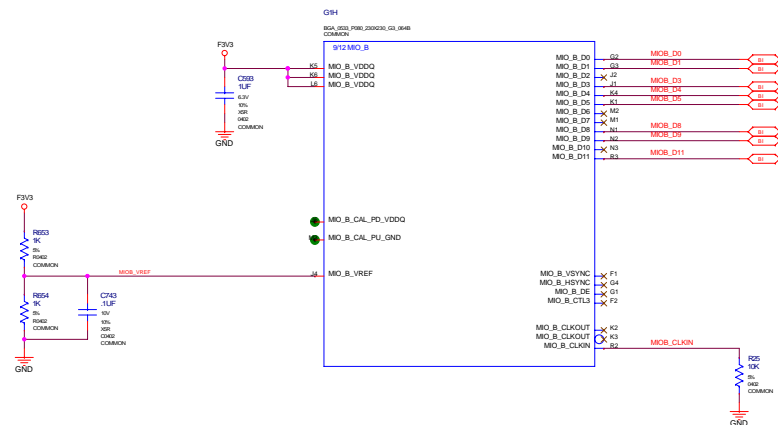
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Internal TMDS, DVI-Connecto

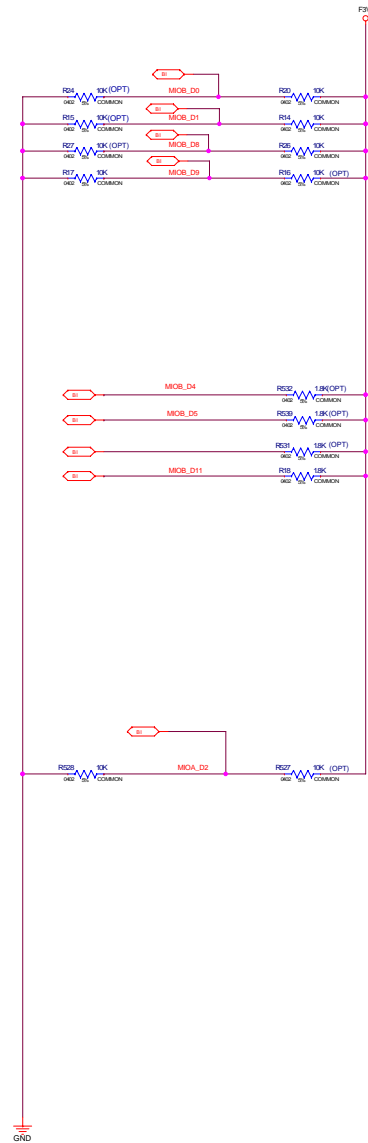
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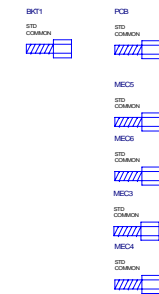
MIOA, MIOB Interface



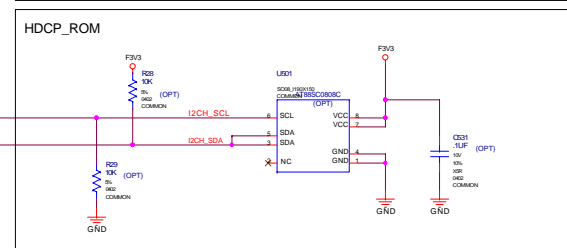
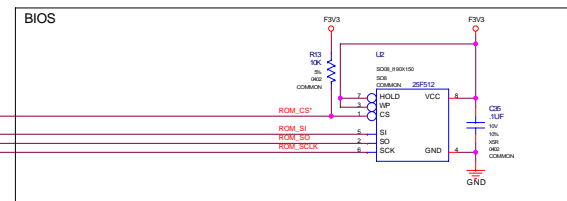
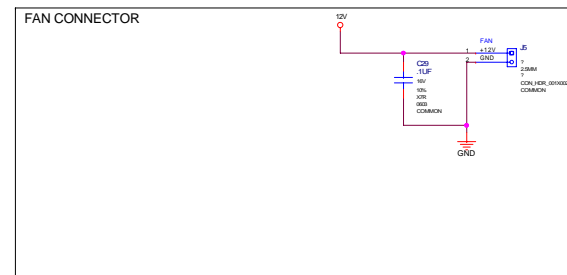
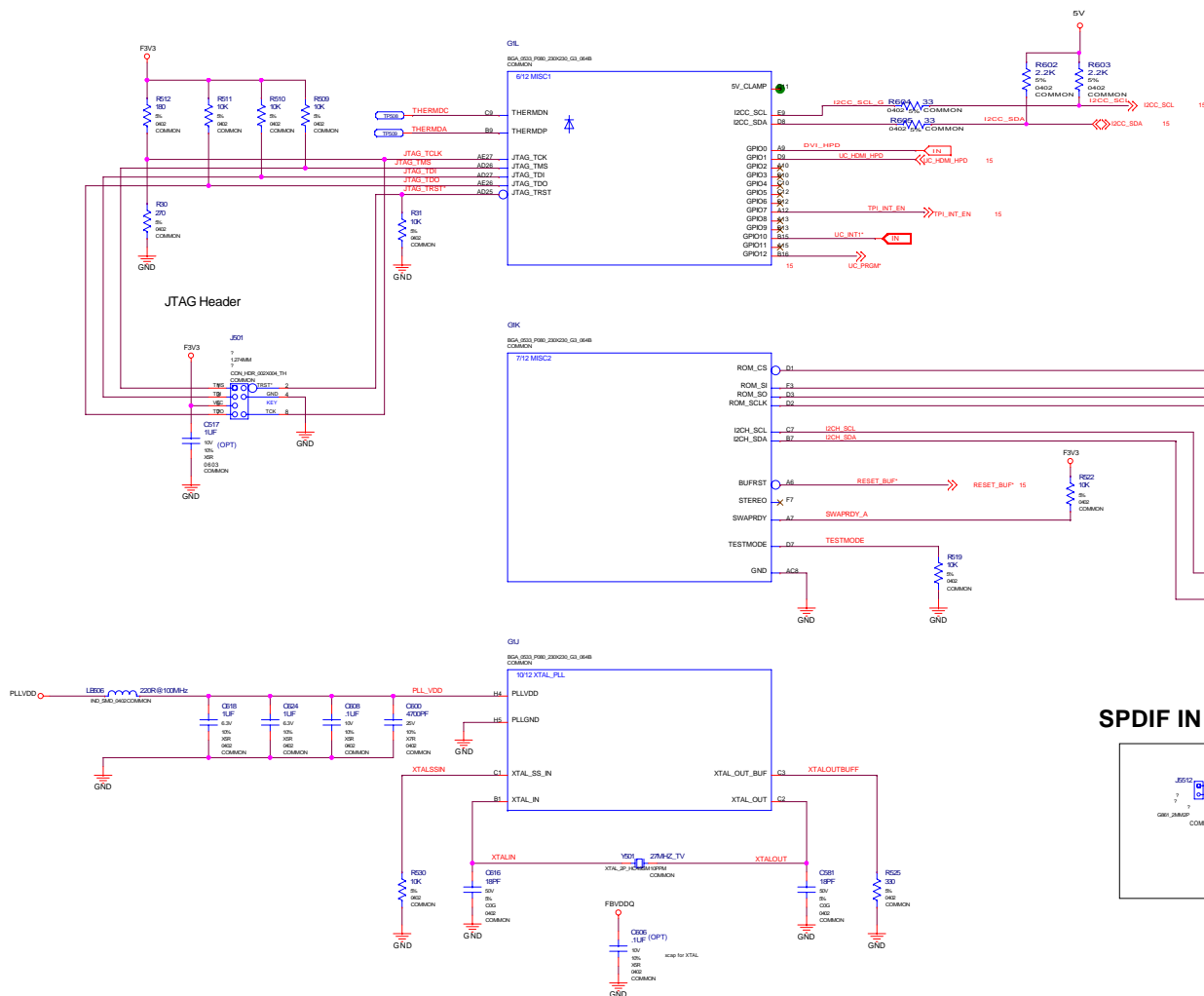
STRAPS, Mechanical Parts



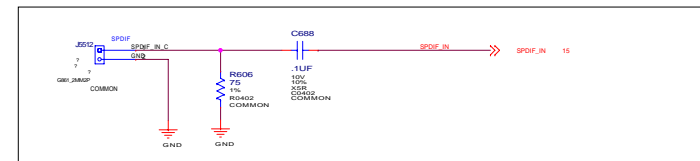
Bit Signal		Values
00	PCI_AC_STOP	0 RECEIVED 1 NORMAL
01	SUB_VENDOR	0 NO_ACE 1 READ FROM BIOS
02	RAM_CFG_0	000 0000 0000 0000 000 000 000 000 000 000 0000 0000 0000 0000 0000 0000 000 0000 0000 0000 0000 0000 0000 0000
03	RAM_CFG_1	000 0000 0000 0000 0000 0000 0000 0000 000 000 000 000 000 0000 0000 0000 0000 0000 0000 0000 000 0000 0000 0000 0000 0000 0000 0000
04	RAM_CFG_2	000 0000 0000 0000 0000 0000 0000 0000 000 000 000 000 000 0000 0000 0000 0000 0000 0000 0000 000 0000 0000 0000 0000 0000 0000 0000
05	RAM_CFG_3	000 0000 0000 0000 0000 0000 0000 0000 000 000 000 000 000 0000 0000 0000 0000 0000 0000 0000 000 0000 0000 0000 0000 0000 0000 0000
06	CRYSTAL_0	00 13.000 MHz 01 14.31818 MHz 10 17.000 MHz 11 UNKNOWN
22	CRYSTAL_1	00 13.000 MHz 01 14.31818 MHz 10 17.000 MHz 11 UNKNOWN
07	TV_MODE_0	00 SECAM 01 NTSC 10 PAL 11 DET
08	TV_MODE_1	00 SECAM 01 NTSC 10 PAL 11 DET
09	AGP_30_M	0 AGP4 ENABLED 1 AGP4 DISABLED
10	AGP_30A	0 SBA ENABLED 1 SBA DISABLED
11	AGP_FASTERR	0 FW ENABLED 1 FW DISABLED
12	PCI_DEVIE_0	1100 (default bus0FC)
13	PCI_DEVIE_1	
20	PCI_DEVIE_2	
21	PCI_DEVIE_3	
14	BUS_TYPE	0 PCI 1 AGP
15	FP_IFACE	0 24MB 1 USB (DEFAULT)
23	FB_0	00 64M 01 128M 10 256M (DEFAULT) 11 512M
24	FB_1	00 64M 01 128M 10 256M (DEFAULT) 11 512M
25	BR	0 BRIDGE DISABLED 1 BRIDGE ENABLED
26	BR_10M	BR BITS IGNORED IF BRIDGE IS DISABLED
27	BR_AGP	
28	BR_ID	
29	ROM_TYPE_0	00 PARALLEL 01 SERIAL_ATA20F 10 SERIAL_2ST40VF 11 LPC
30	ROM_TYPE_1	00 PARALLEL 01 SERIAL_ATA20F 10 SERIAL_2ST40VF 11 LPC
16	USER_0	0000 (DEFAULT)
17	USER_1	
18	USER_2	
19	USER_3	
FEX_PXL_ZN_1250P102		
SGIO_PADCFG_LUT_ADDR[0]		
SGIO_PADCFG_LUT_ADDR[1]		
hardware_init_check_configuration		



XTAL, GPIO, BIOS, FAN, JTAG, THERMAL,SPIDF



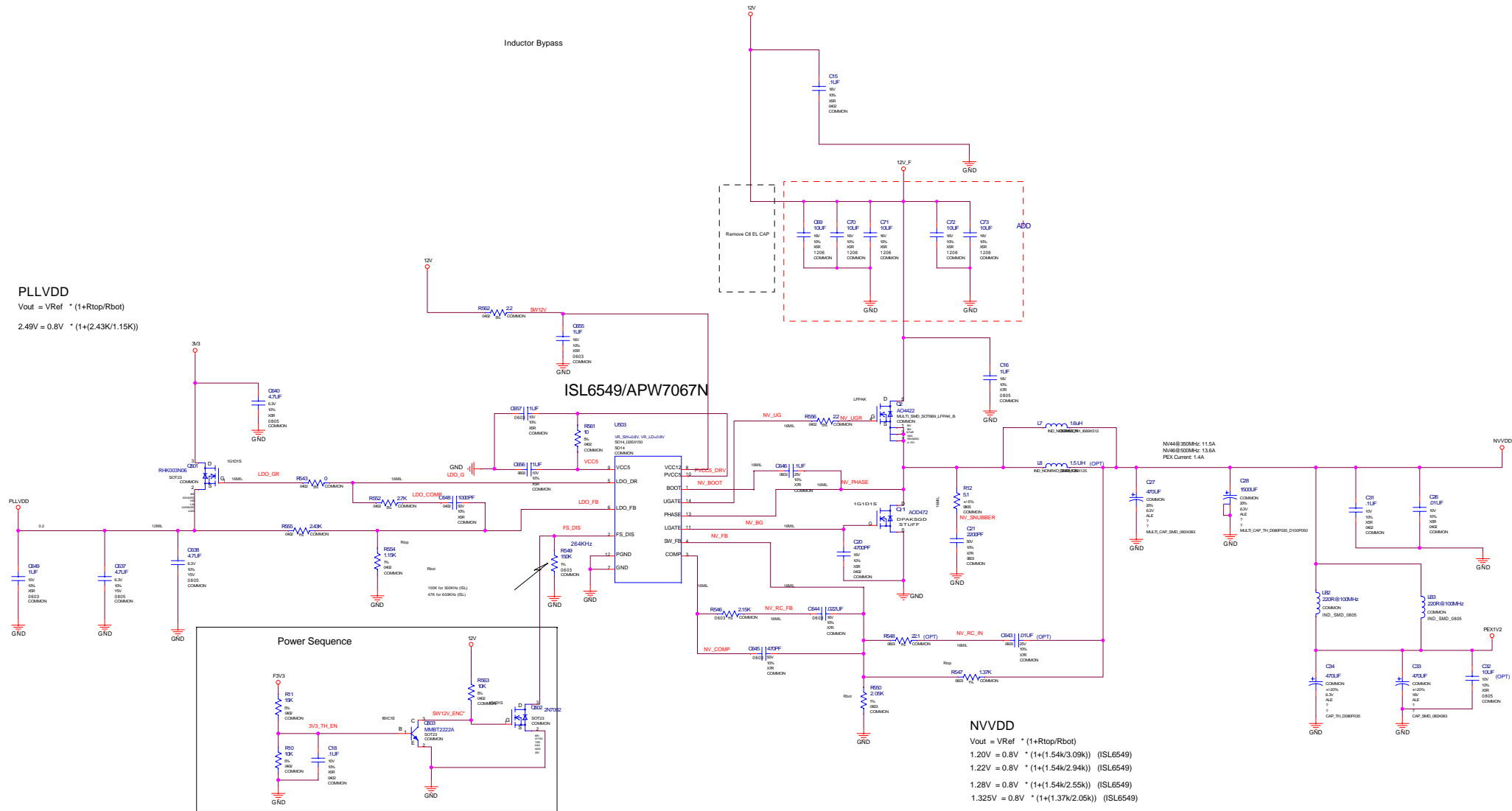
SPIDF IN



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XTAL, GPIO, BIOS, FAN			
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PowerSupplyI: NVVDD, PLLVDD

PLLVDD
 $V_{out} = V_{Ref} \cdot (1 + R_{top}/R_{bot})$
 $2.49V = 0.8V \cdot (1 + (2.43K/1.15K))$

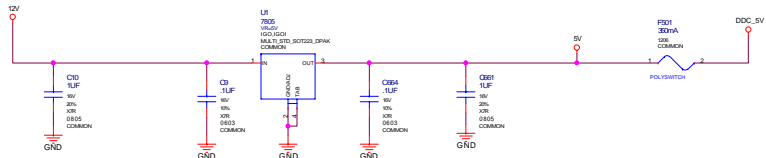


Replace SO-8 FETs with AO4422

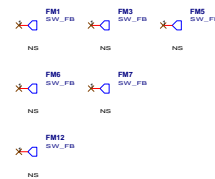
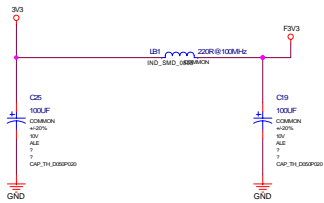
NVVDD
 $V_{out} = V_{Ref} \cdot (1 + R_{top}/R_{bot})$
 $1.20V = 0.8V \cdot (1 + (1.54K/3.09K))$ (ISL6549)
 $1.22V = 0.8V \cdot (1 + (1.54K/2.94K))$ (ISL6549)
 $1.28V = 0.8V \cdot (1 + (1.54K/2.55K))$ (ISL6549)
 $1.325V = 0.8V \cdot (1 + (1.37K/2.05K))$ (ISL6549)

PowerSupplyII: 5V, DDC5V, F3V3, FBVDDQ,1V8

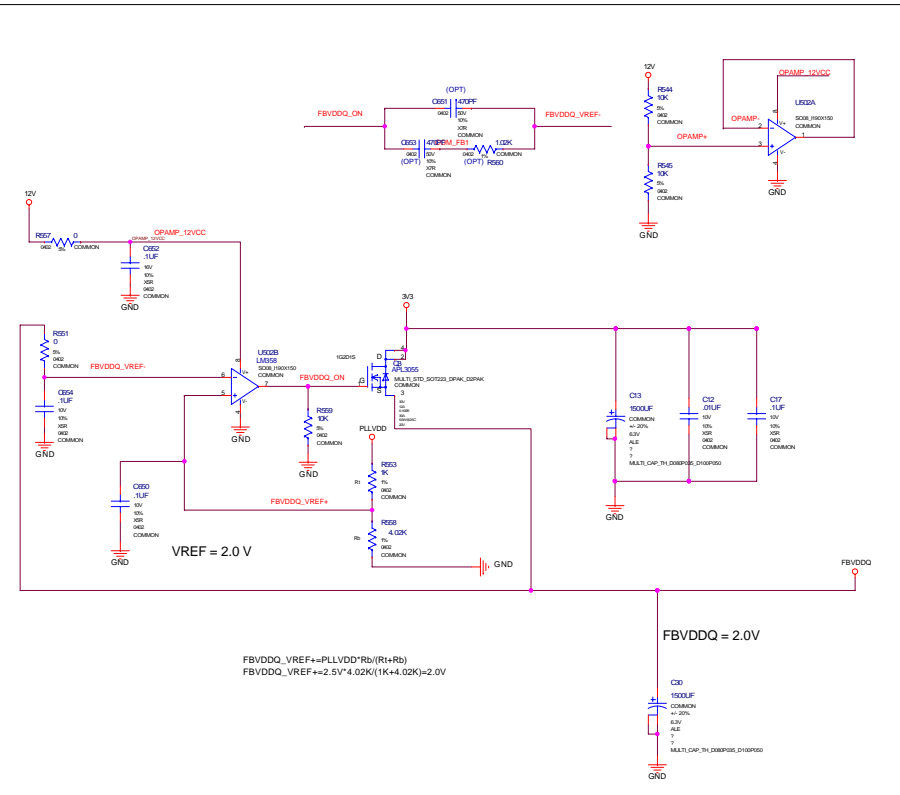
5V , DDC5V



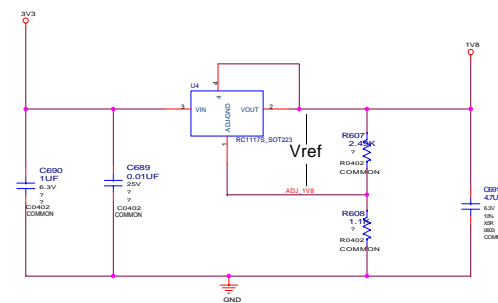
F3V3



FBVDDQ



1.8V 320mA



$$V_{out} = V_{ref} \left(1 + \frac{R_{bot}}{R_{top}} \right)$$

$$V_{out} = 1.25 \left(1 + \frac{1.1K}{2.49K} \right) = 1.8V$$

Hotplug Detection

Capacitance of HDMI_SDA_C & HDMI_SCL_C nets to Power/GND planes must be less than 50pF (try to make it lower)

TMDS AC termination PLACE CLOSE TO THE SI.

