PG165-A00

TU116 6GB GDDR5, 192b, X32
DVI-D + DP + HDMI

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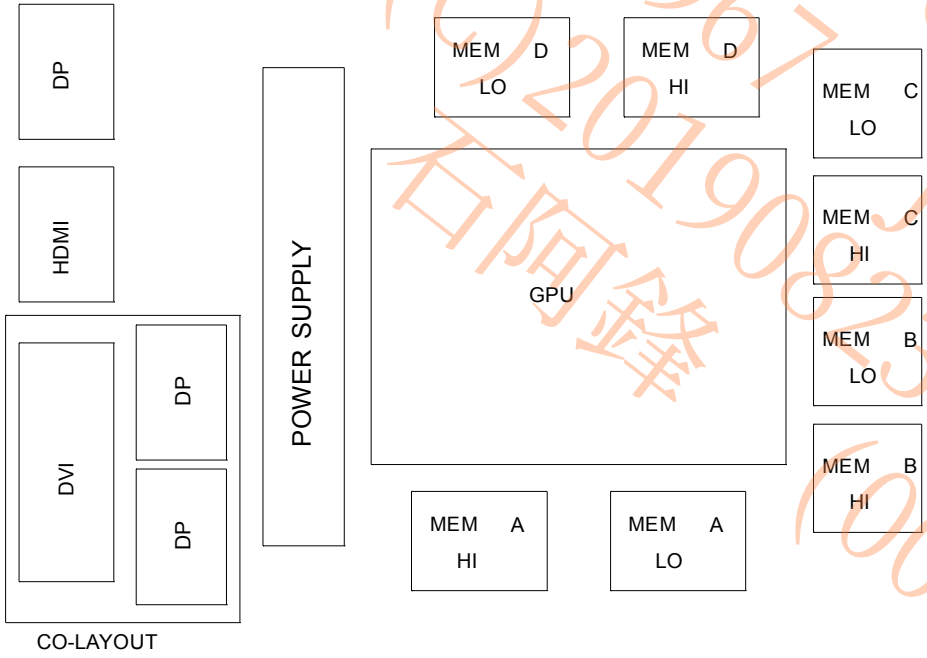
Page2: Block Diagram



Power Supply:

- Power Supply NVVDD-PH6
- Power Supply NVVDD-PH5
- Power Supply NVVDD-PH4
- Power Supply NVVDD-PH3
- Power Supply NVVDD-PH2
- Power Supply NVVDD-PH1
- Power Supply FBVDDQ-PH2
- Power Supply FBVDDQ-PH1
- Power Supply 5V
- PEX_VDD
- 1V8
- Fan
- DP_PWR

EXT_12V 8PIN PWR

PEX_12V Finger

PEX_3V3 FINGER

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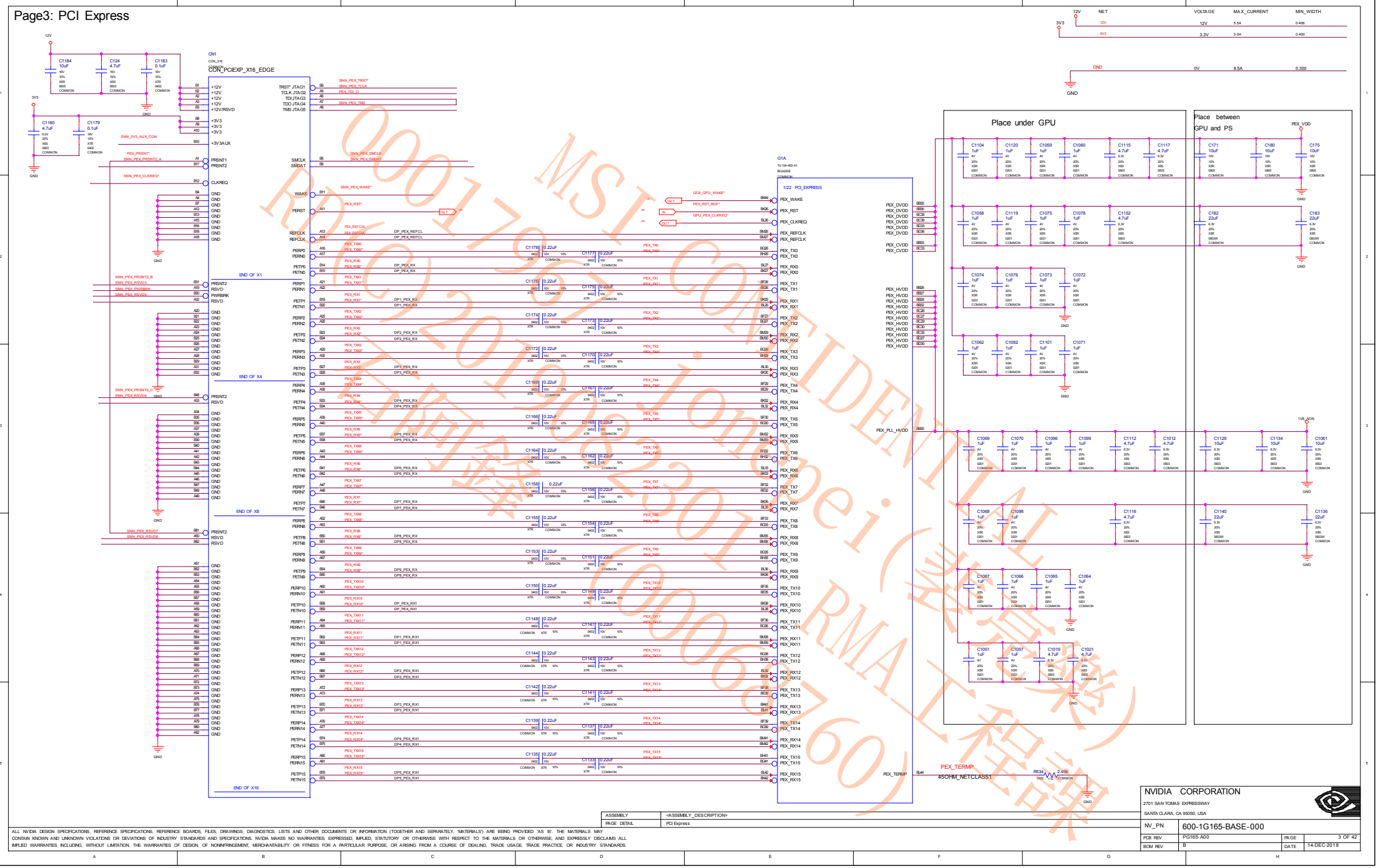
Page3: PCI Express



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.405
3V3	3.3V	3.0A	0.400
GND	0V	8.5A	0.300

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI Express

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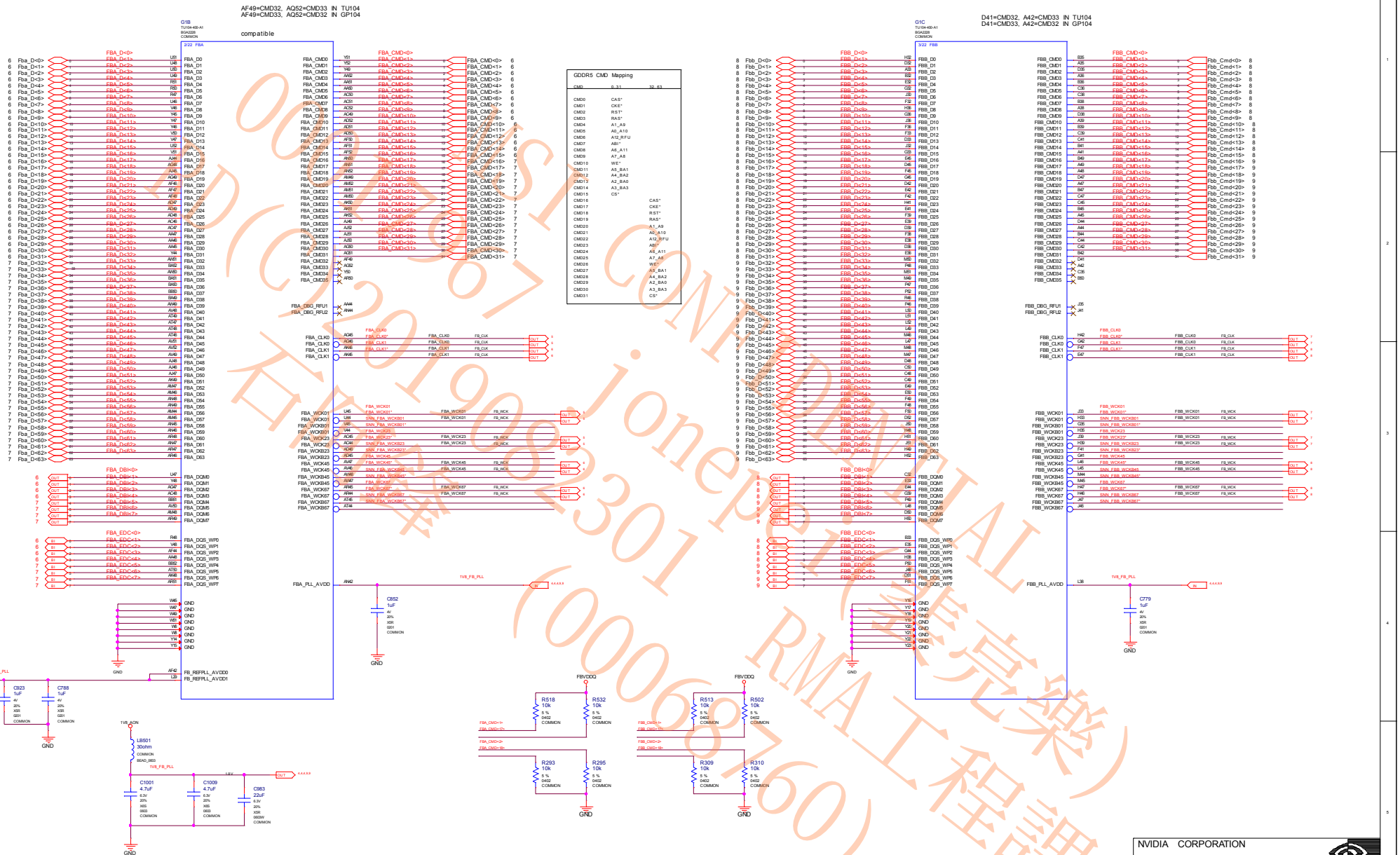
Page4: MEMORY: GPU Partition A/B



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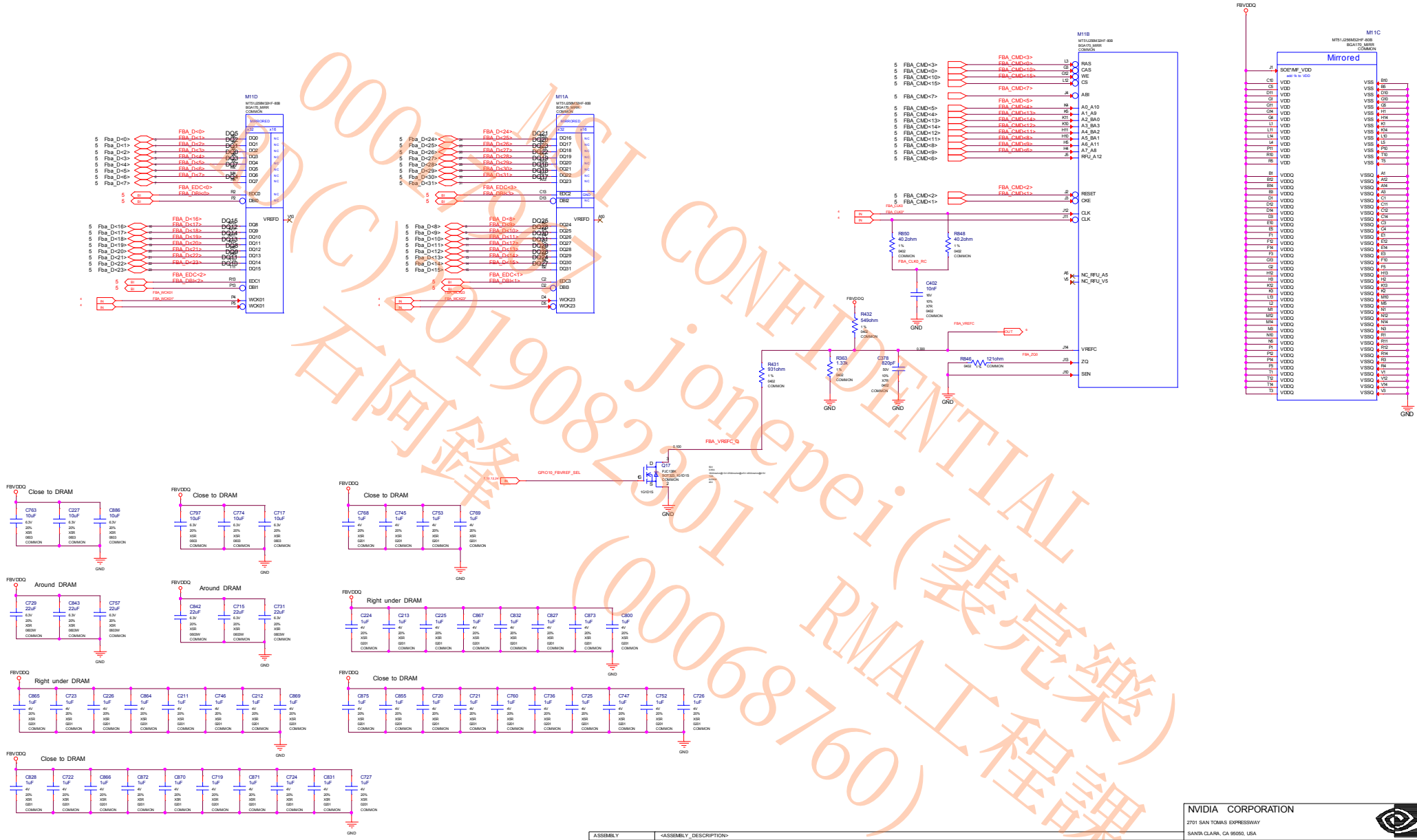

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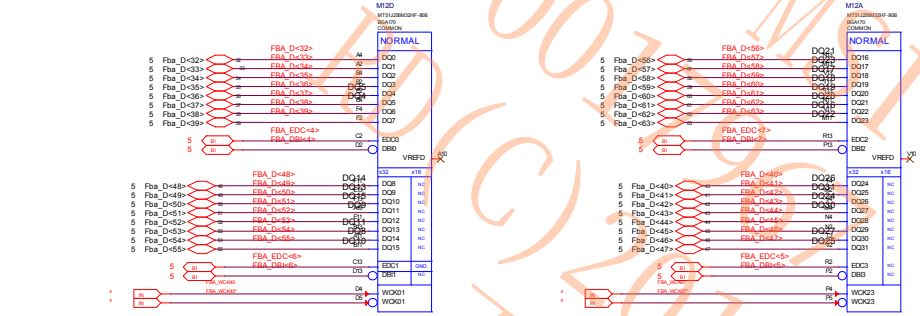

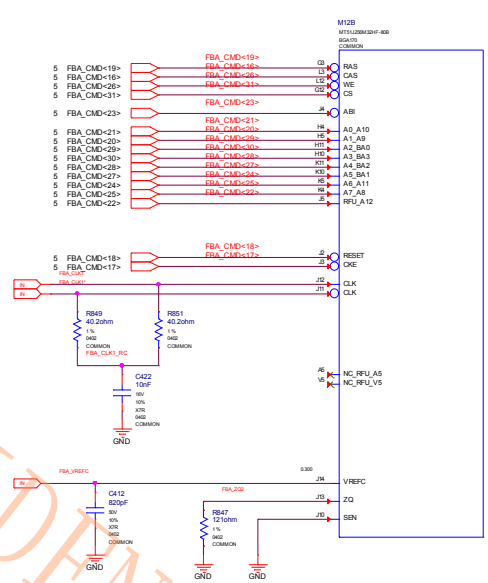

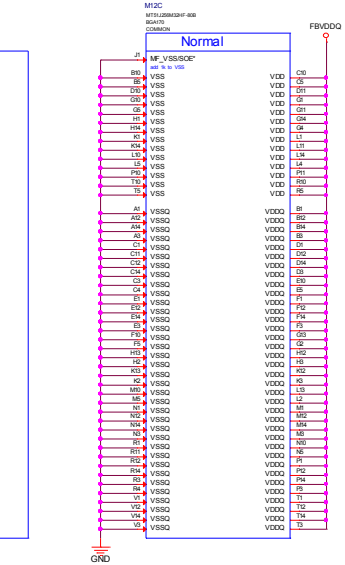

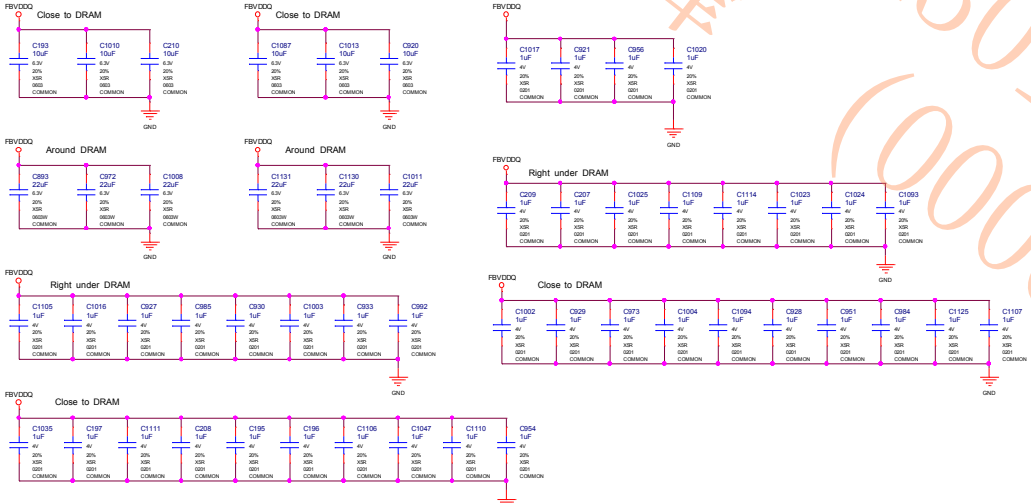

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0019(C)2619082301 (00068760)
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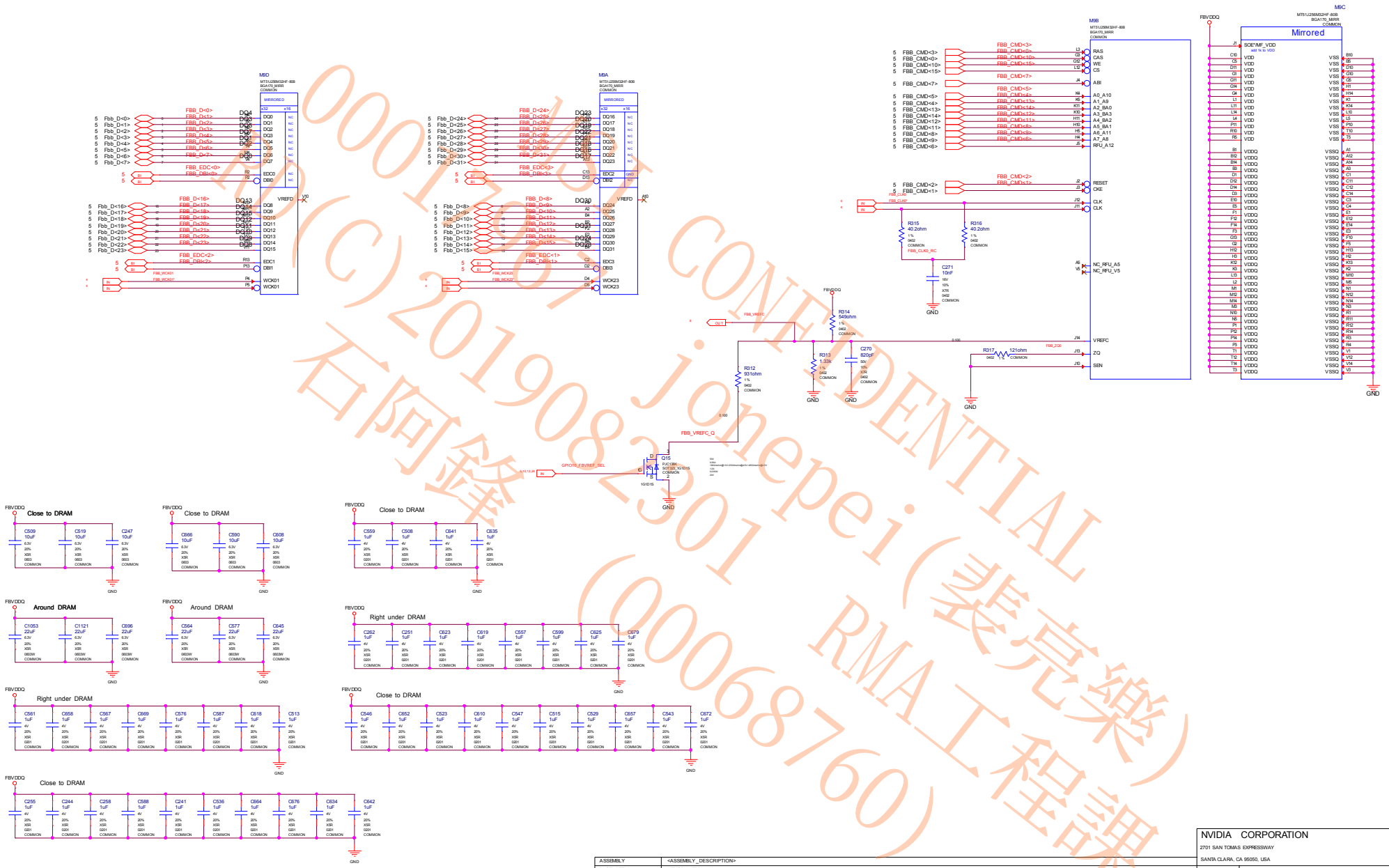

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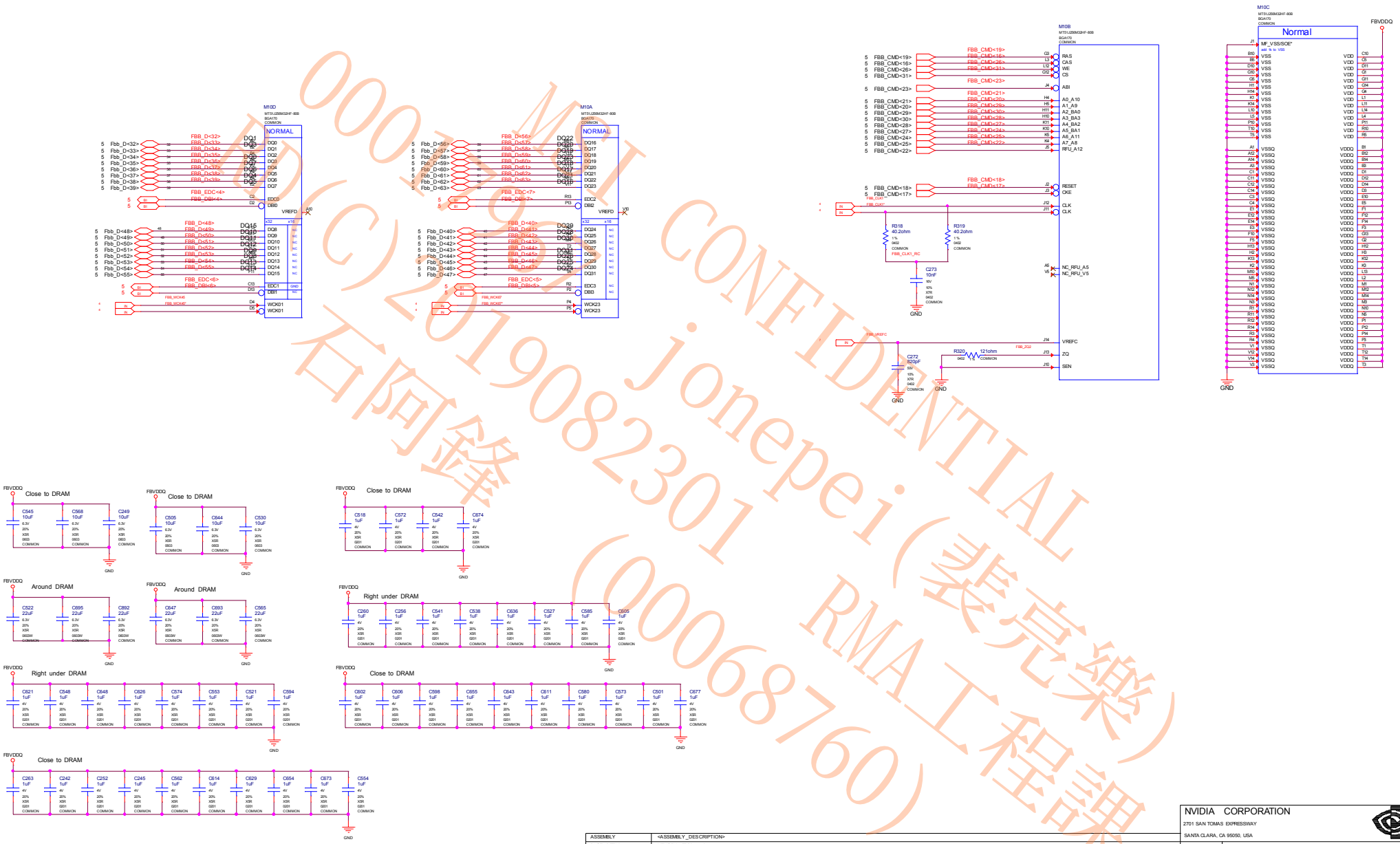

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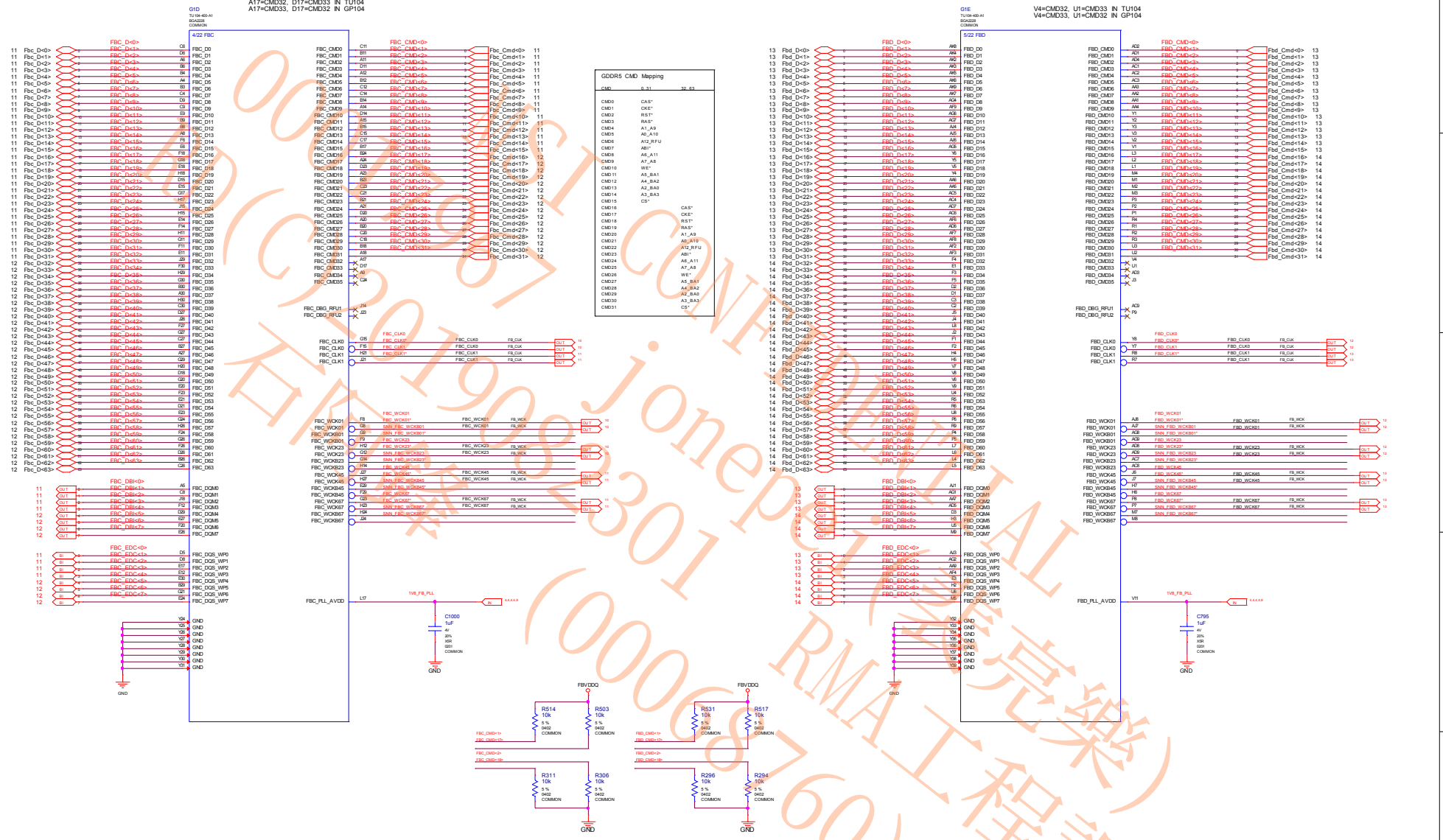
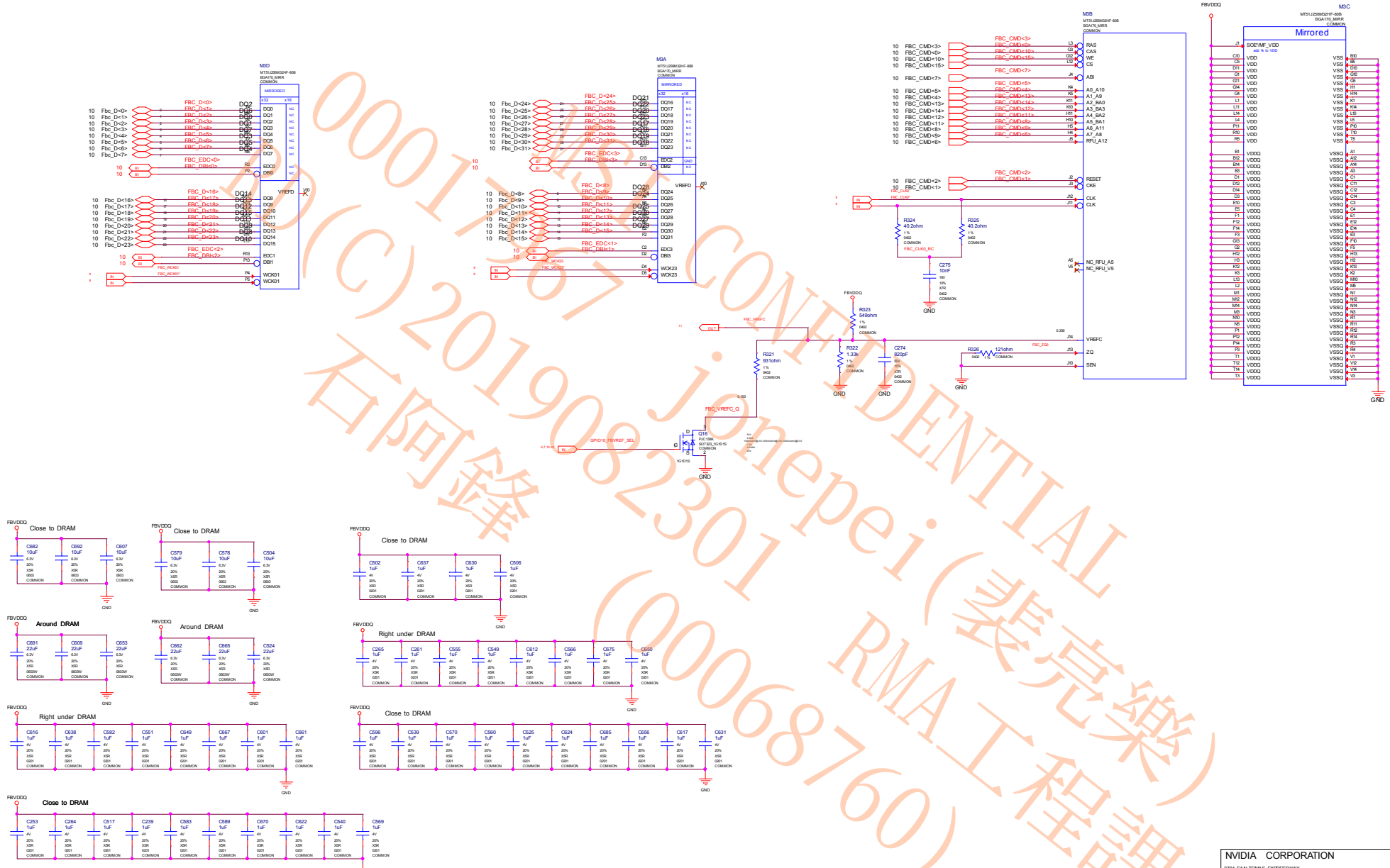
Page9: MEMORY: GPU Partition C/D



Page10: MEMORY: FBC Partition 31..0



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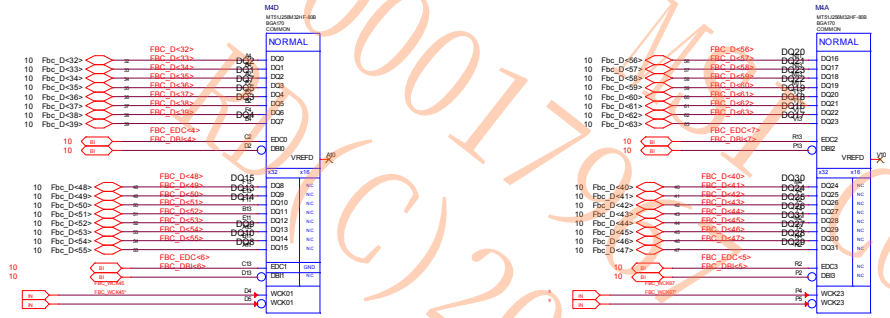
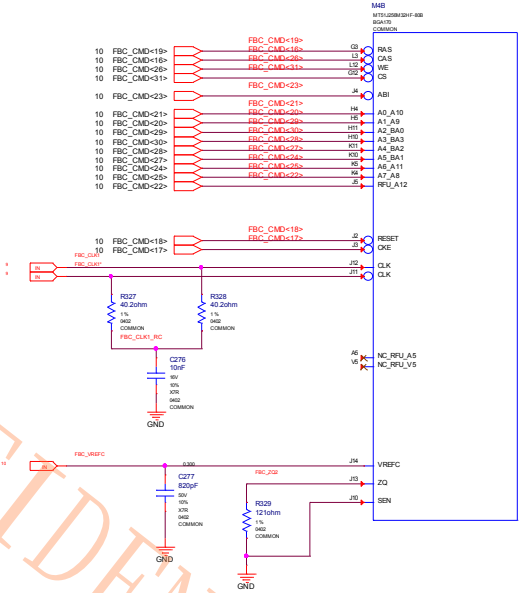
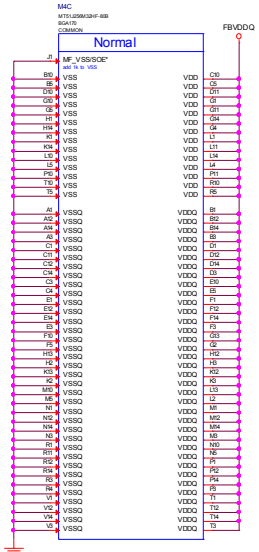
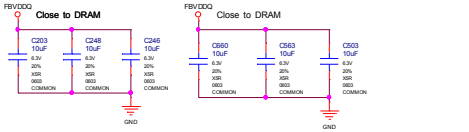
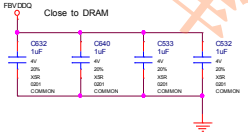
Page11: MEMORY: FBC Partition 63..32

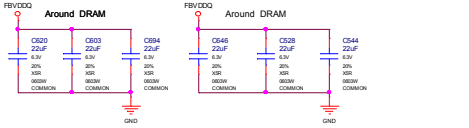


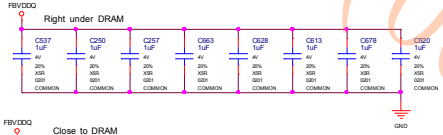


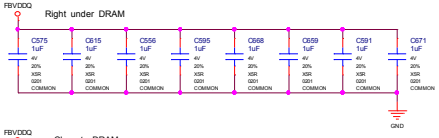


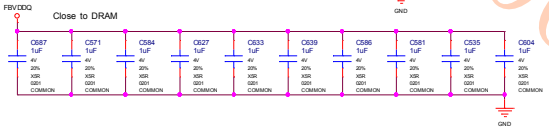


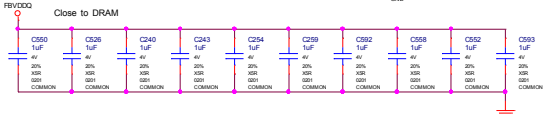












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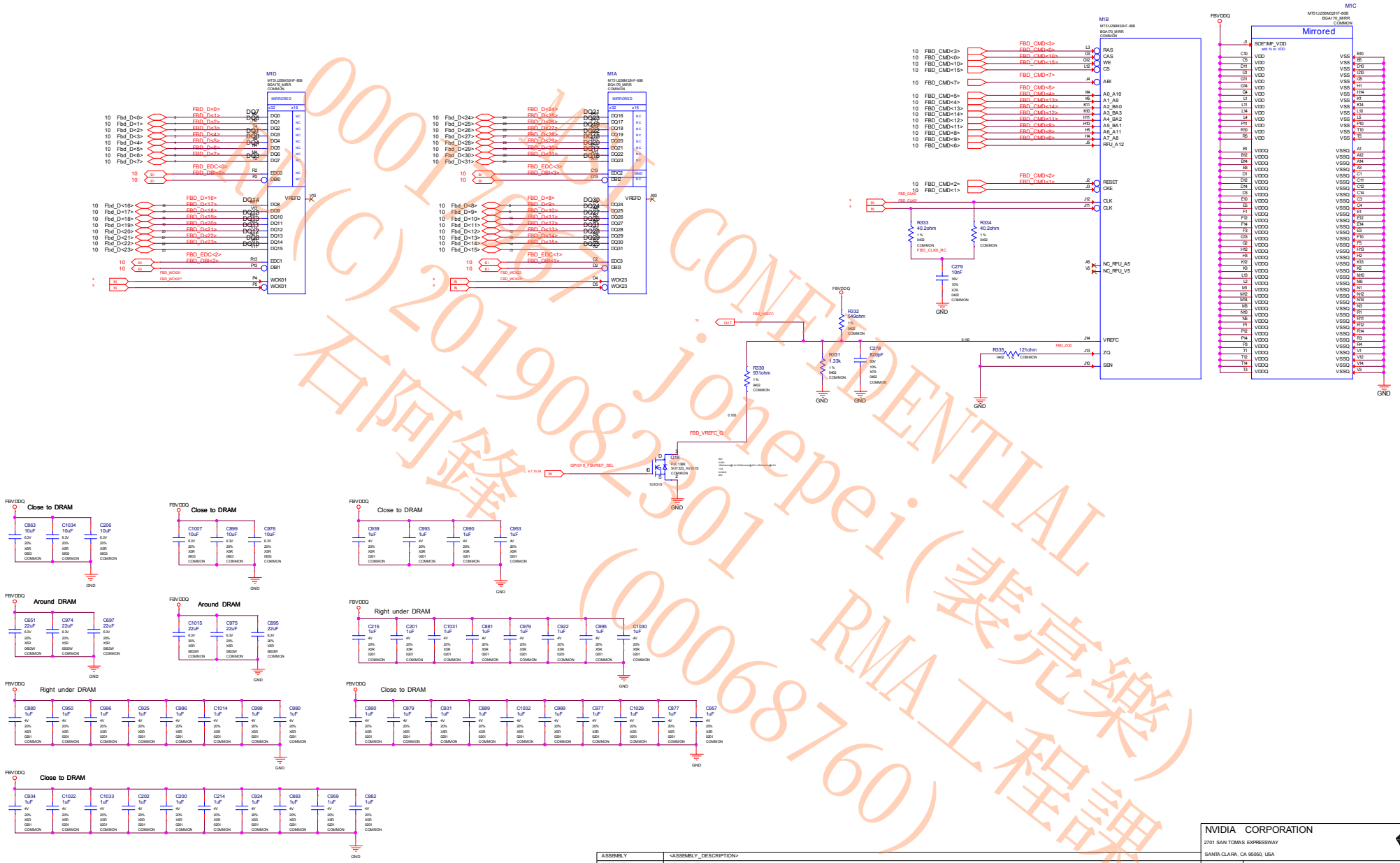

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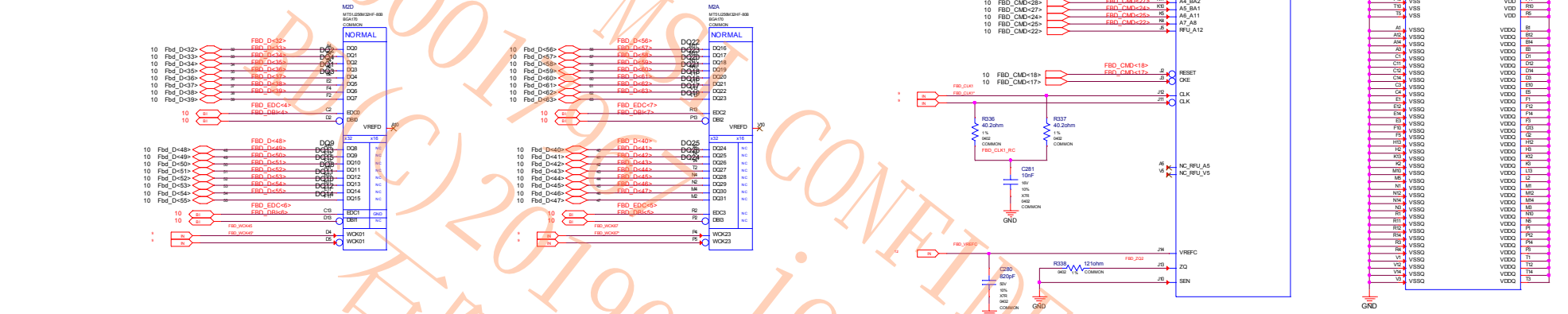
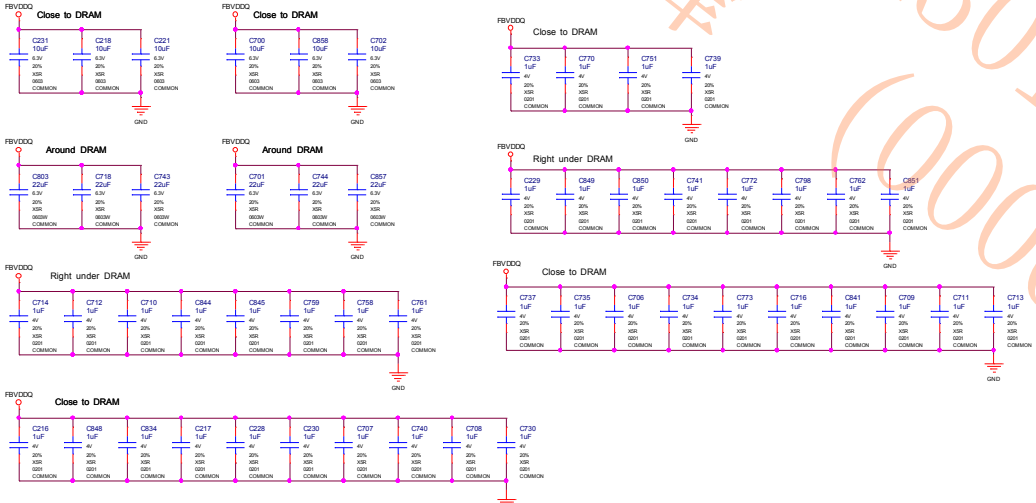
BOM REV	B	DATE	14-DEC-2018

(000168760) 石阿鋒 (001/2019082301) 裴亮樂 (RMA工程課)





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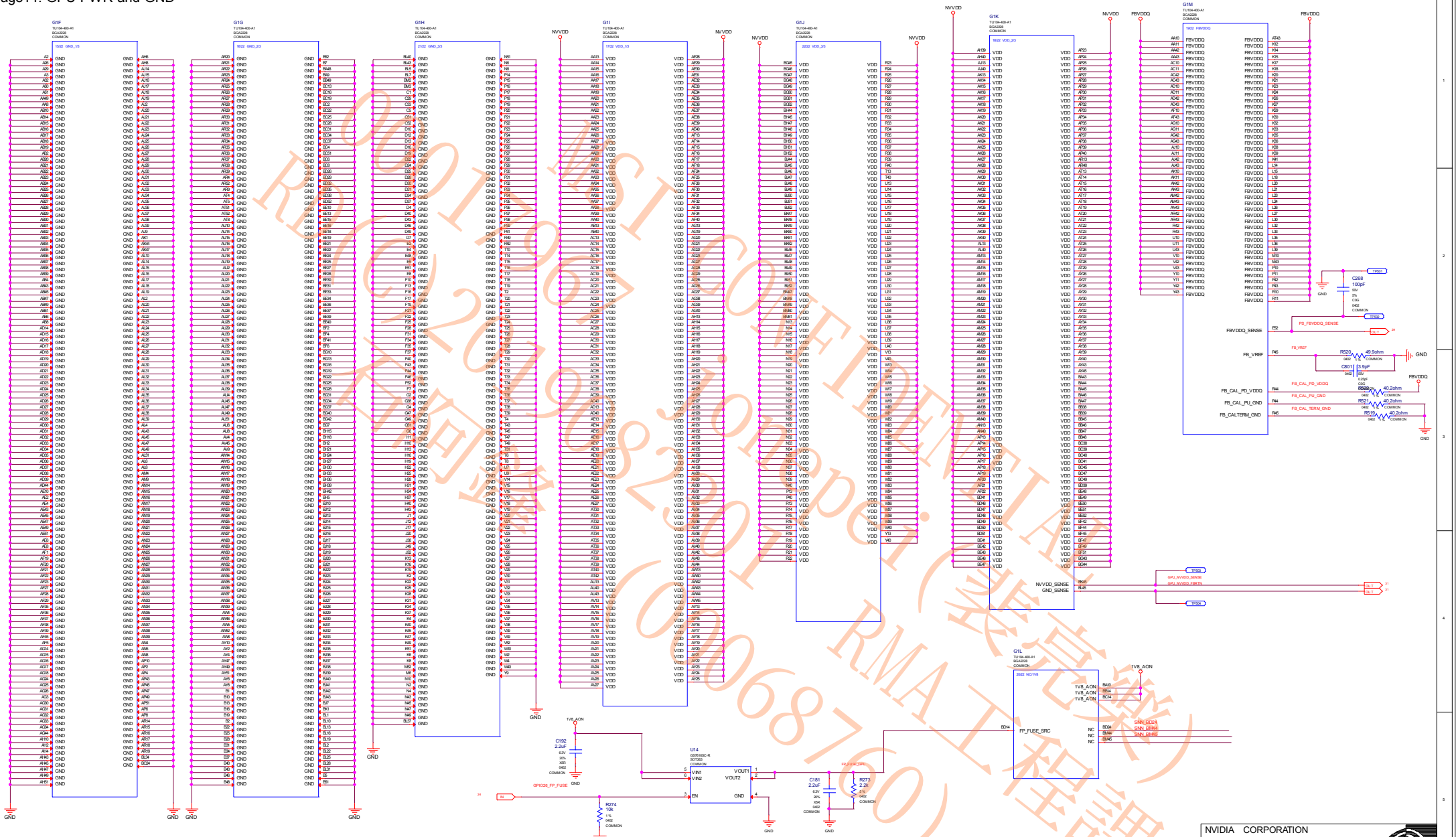
Page14: GPU PWR and GND



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PAGE DETAIL	GPU PWR & GND

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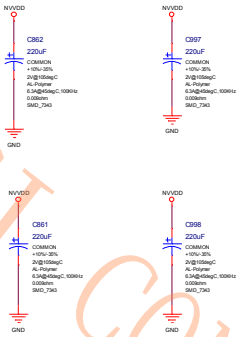
Page15: GPU DECOUPLING 1

FBVDDQ

NVVDD



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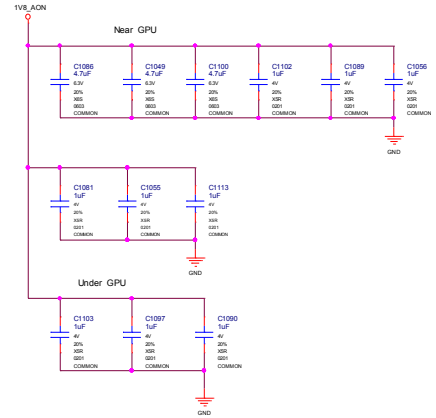

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PAGE DETAIL	GPU DECOUPLING 1

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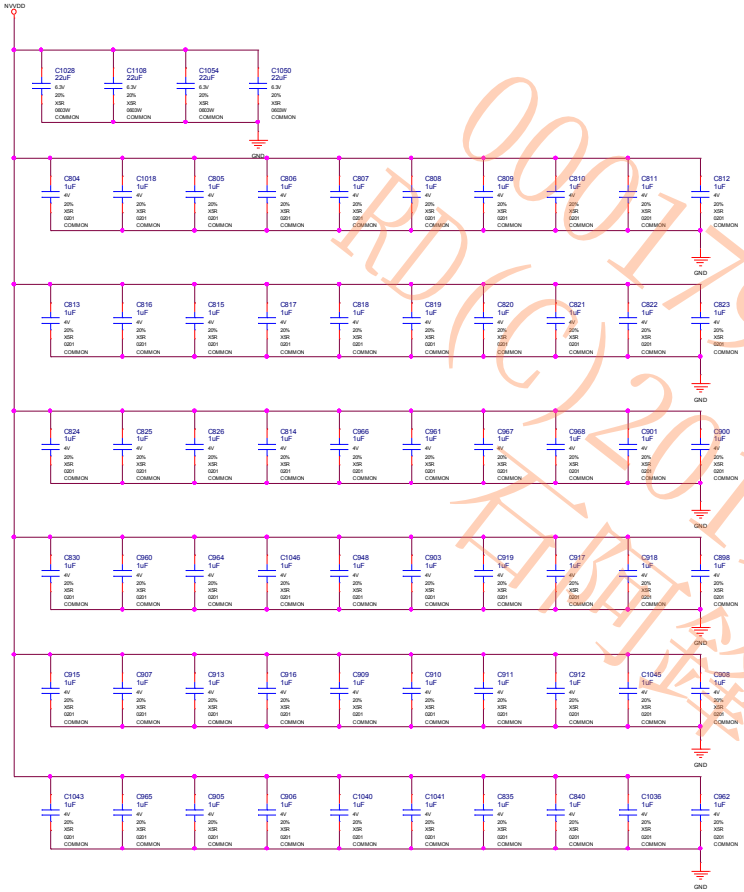
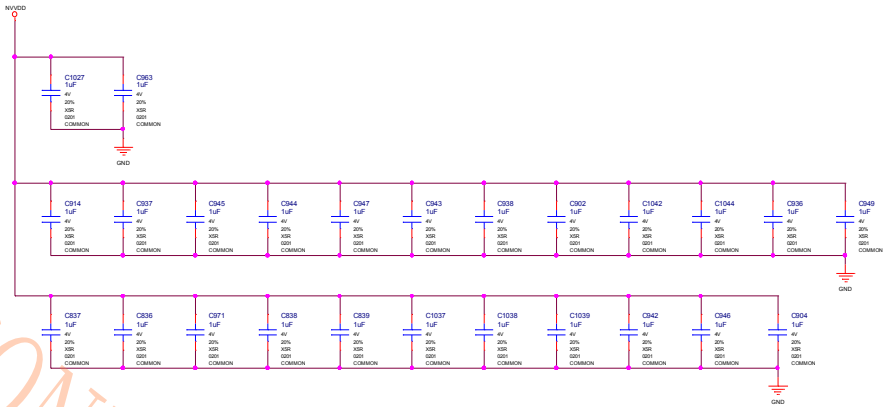
Page16: GPU DECOUPLING 2

NVVDD





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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING 2

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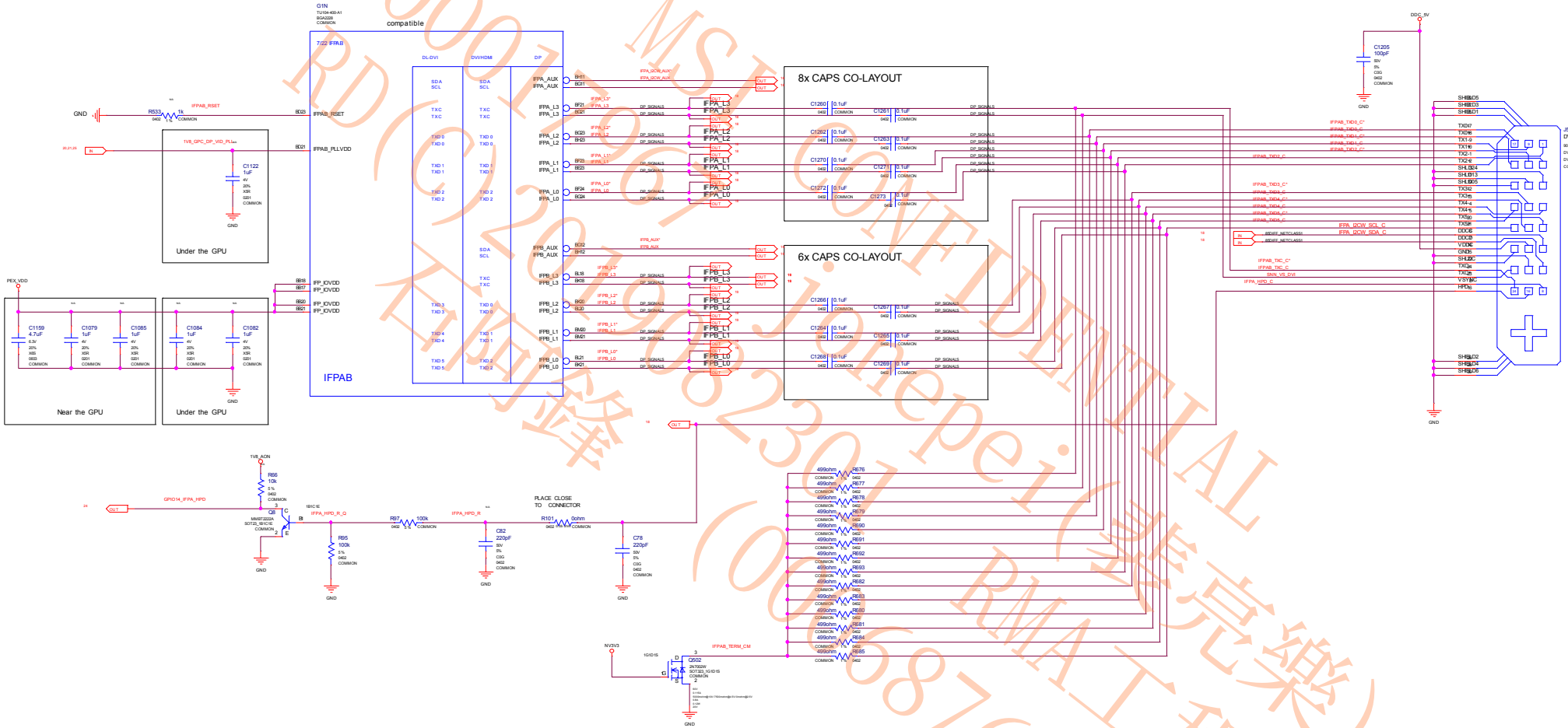
BOM REV	B	DATE	14-DEC-2018



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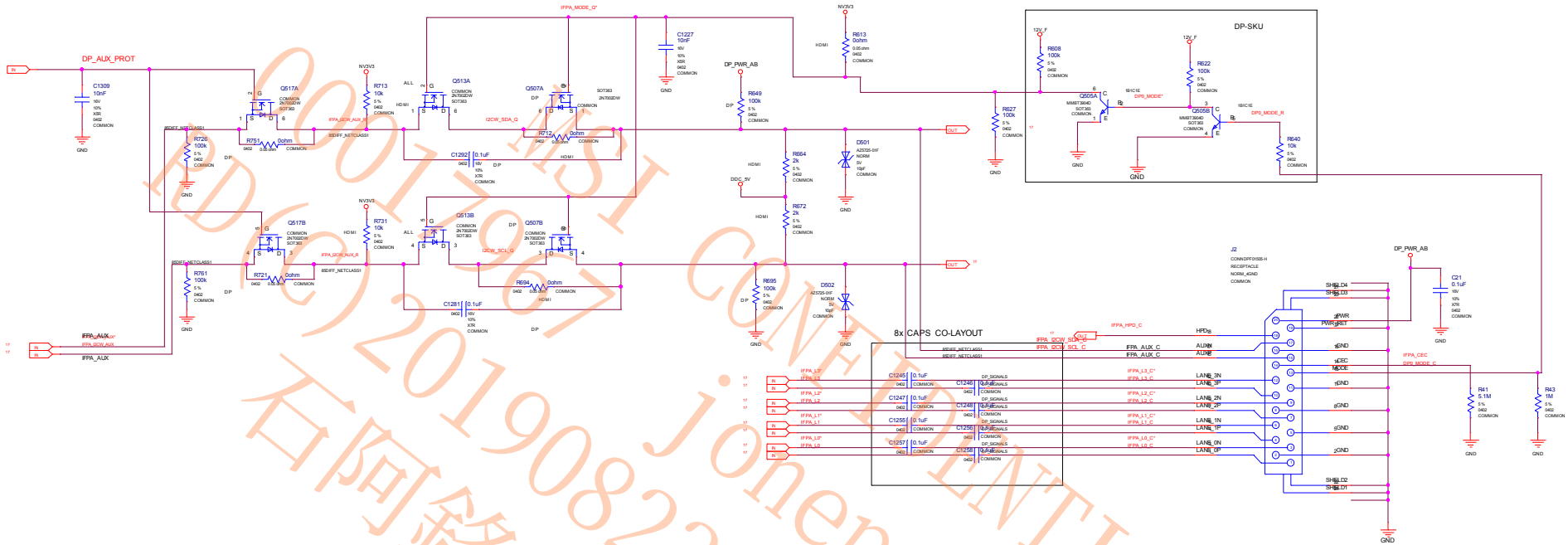

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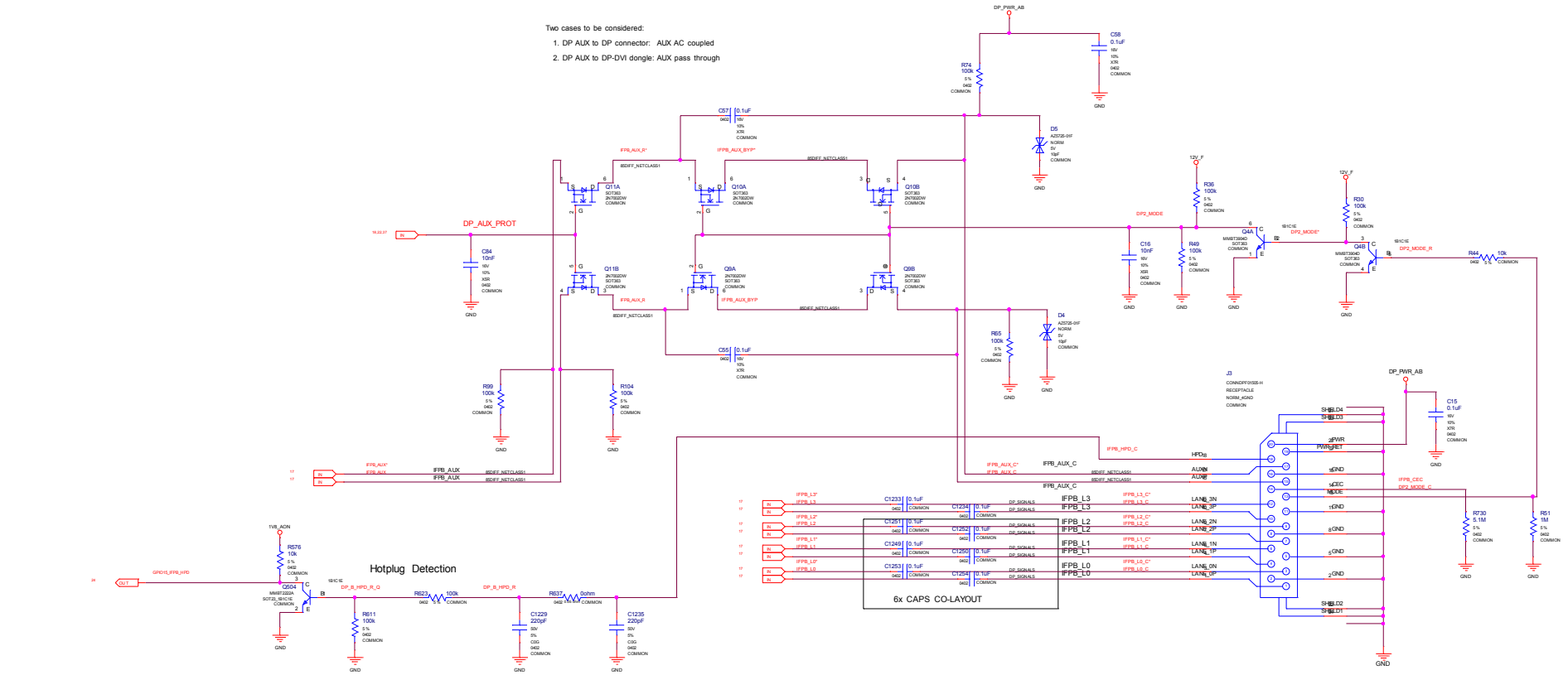
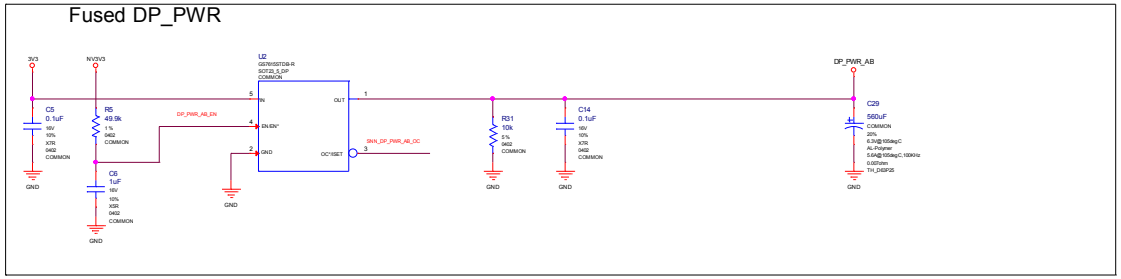
Page19: IFPB DP





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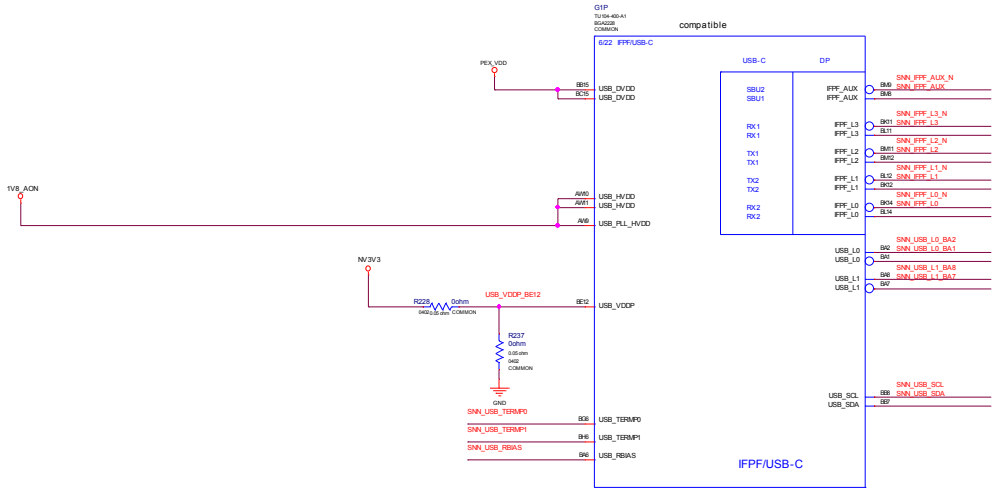
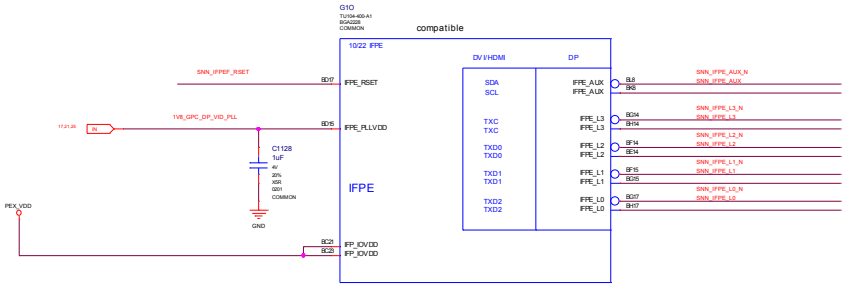
Page20: IFPE & IFPF NC





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IO: IFPE & IFPF NC

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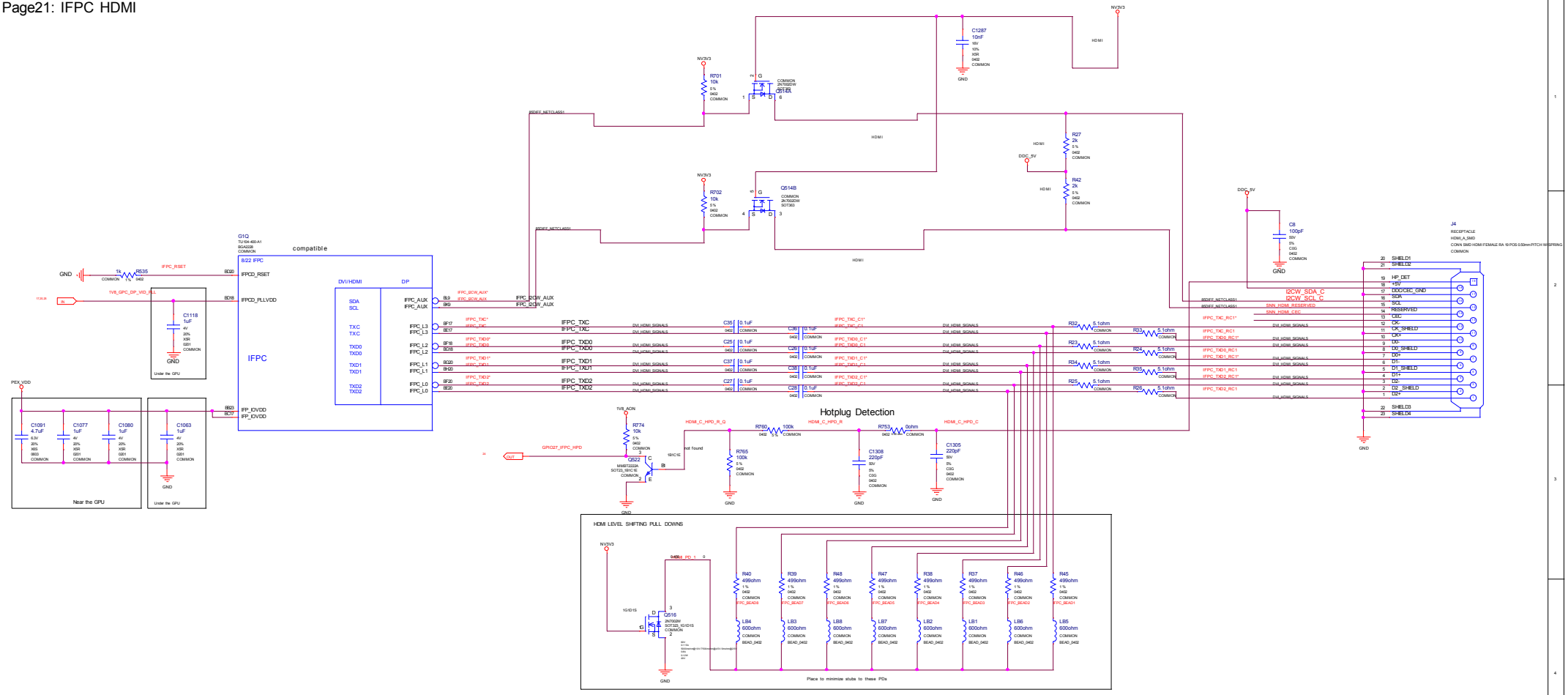
Page21: IFPC HDMI



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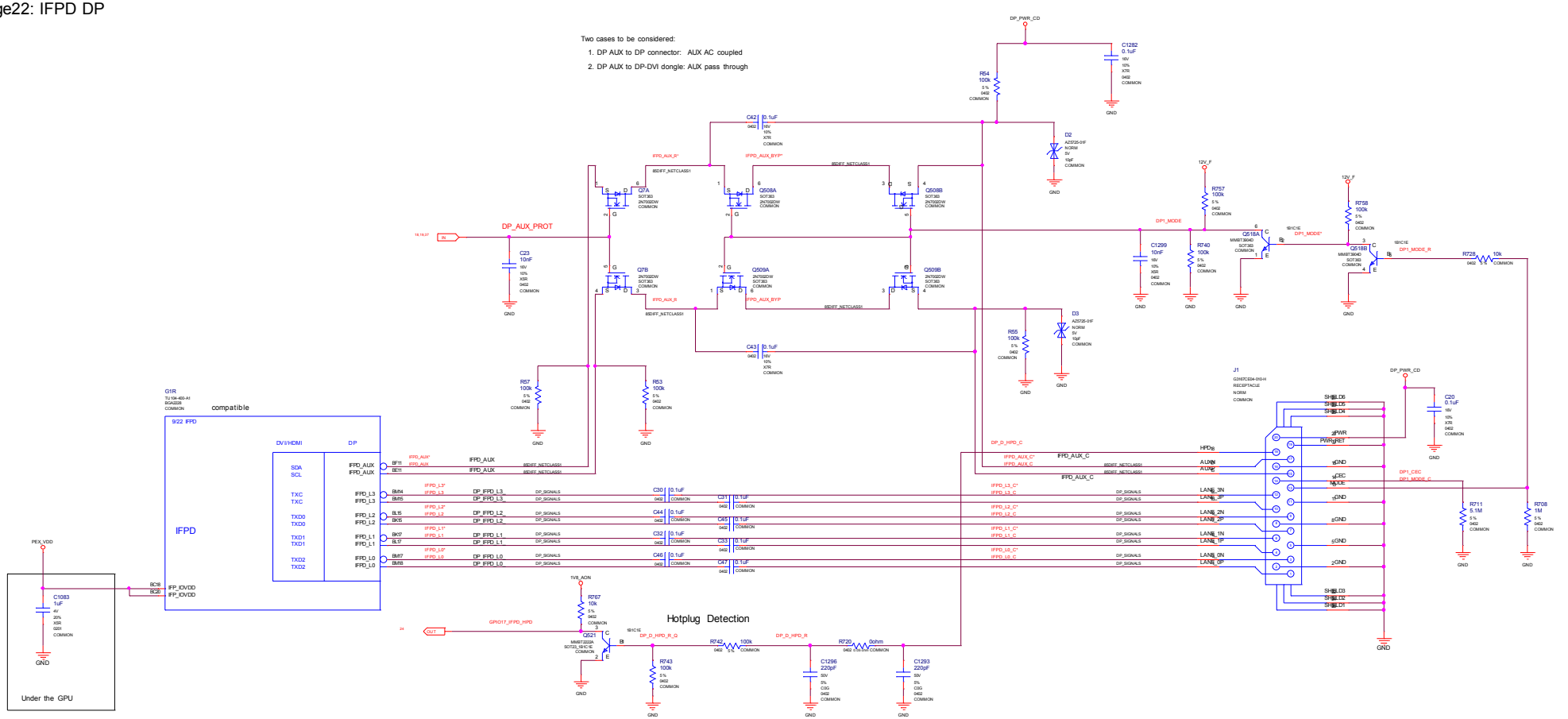
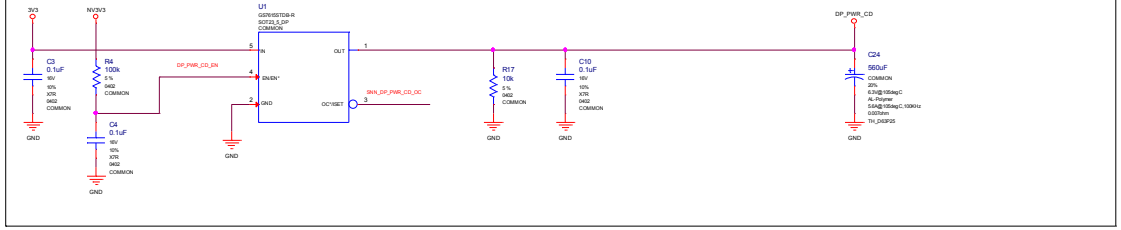
Page22: IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR



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PAGE DETAIL	IO: IFPD DP

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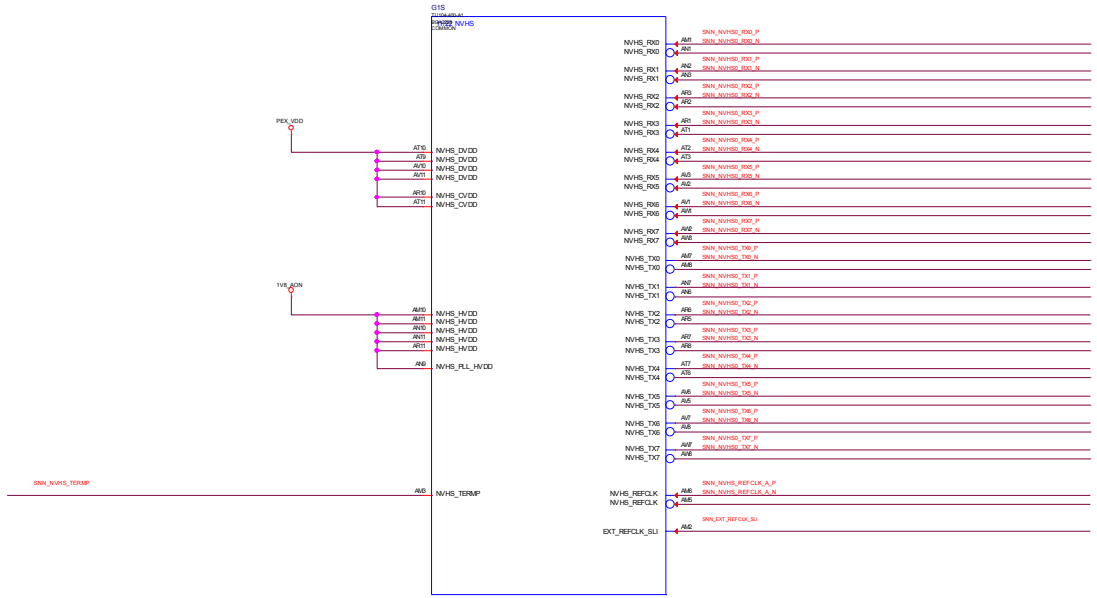
Page23: NVHS INTERFACE AND FRAME LOCK



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	IO: NVHS INTERFACE AND FRAME LOCK

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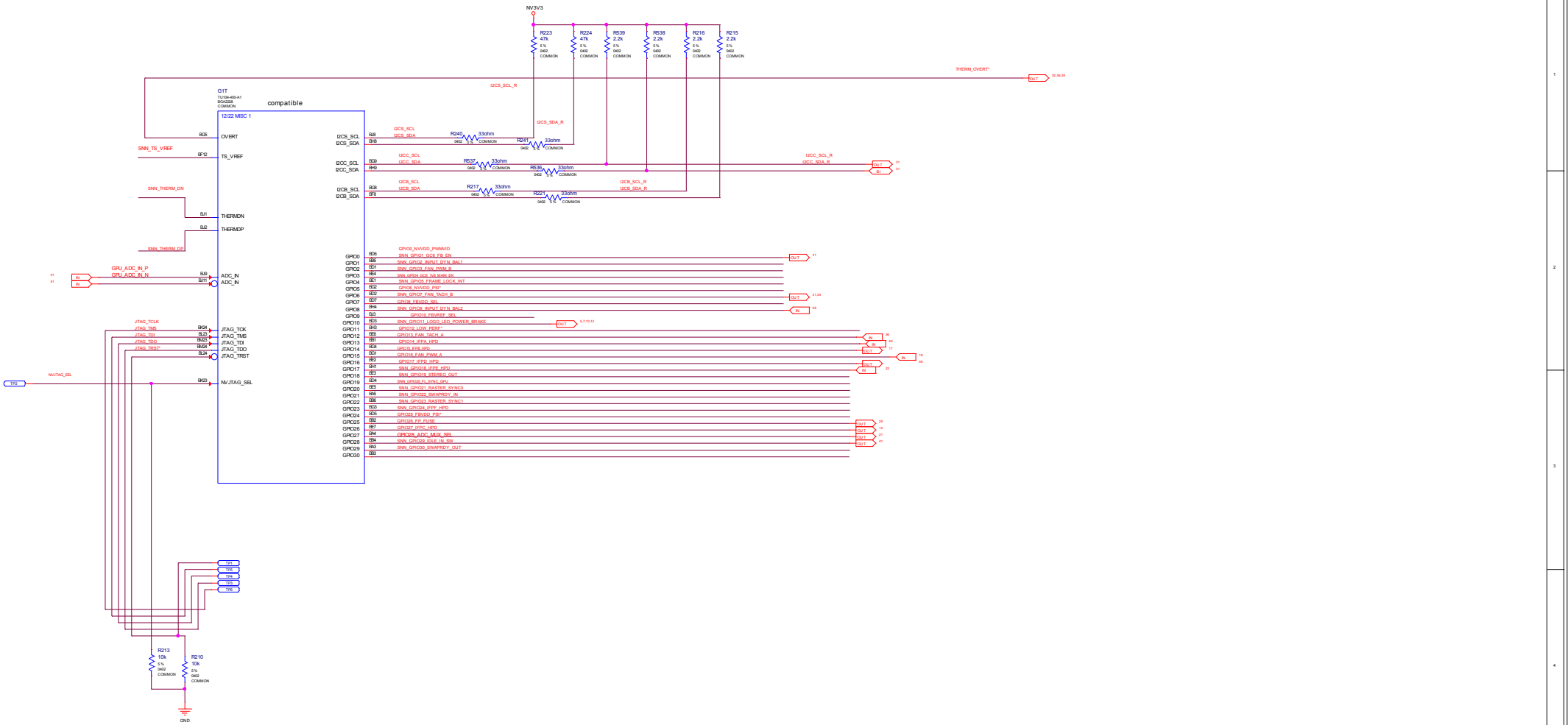
BOM REV	B	DATE	14-DEC-2018

Page24: MISC1: JTAG, GPIO, ADC, I2C, OVERT



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PAGE DETAIL	MISC1: JTAG,GPIO,ADC,I2C,OVERT

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BOM REV	B	DATE	14-DEC-2018

Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung 8Gb 256Mx32 K4G80325FC-HC25
L	L	H	0001	Micron 8Gb 256Mx32 MT51J256M32HF-80:B
L	H	L	0010	Hynix 8Gb 256Mx32 H5GC8H24AJR-R2C
L	H	H	0011	Hynix 8Gb 256Mx32 H5GQ8H24MJR-R4C
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

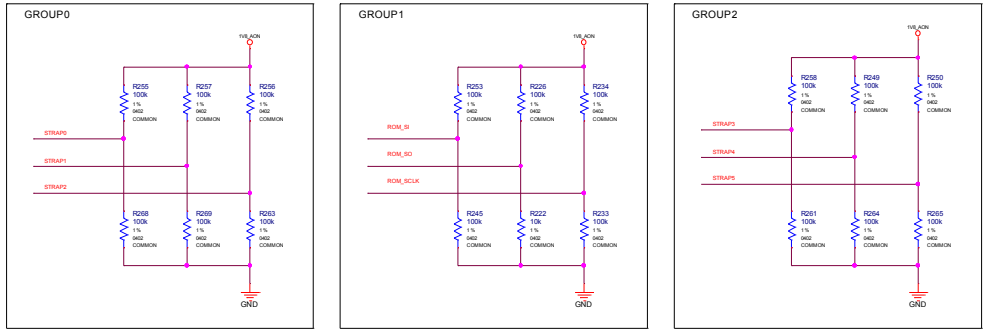
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

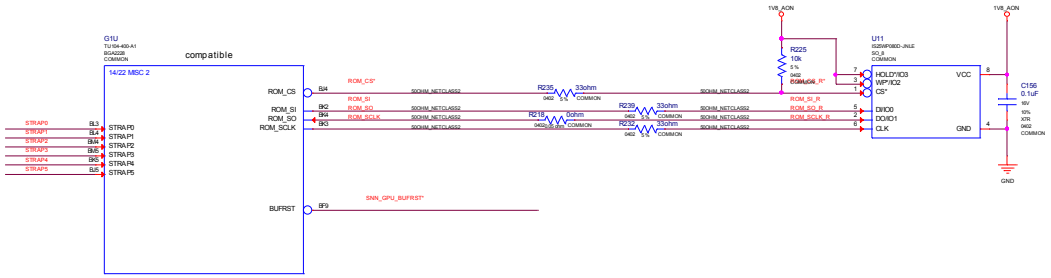
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

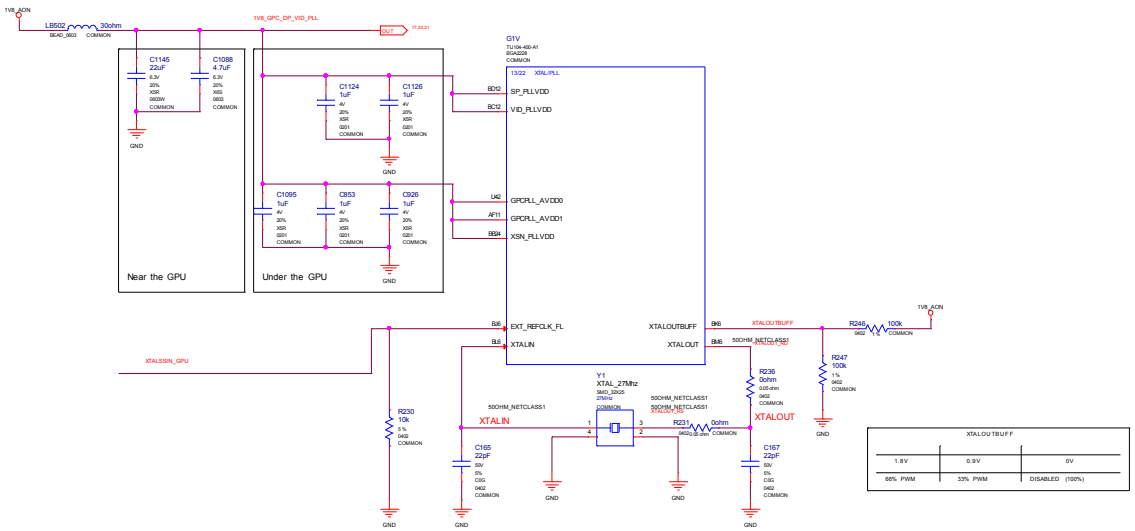
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL,STRAPS

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NV_PN	600-1G165-BASE-000		
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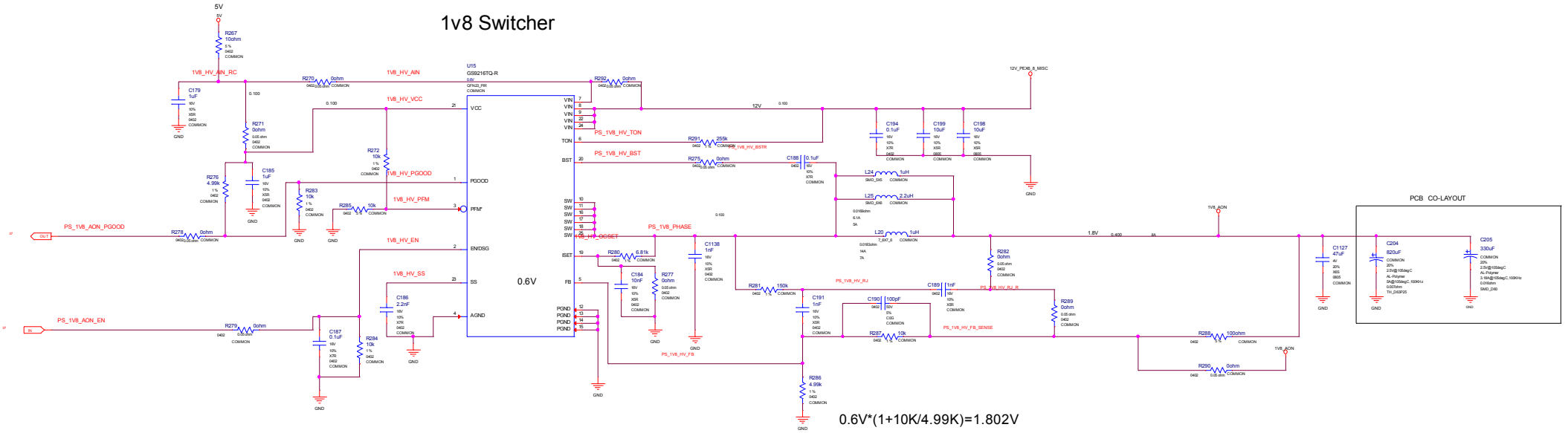
BOM REV	B	DATE	14-DEC-2018

1v8 Switcher



0.6V*(1+10K/4.99K)=1.802V

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 1V8_AON

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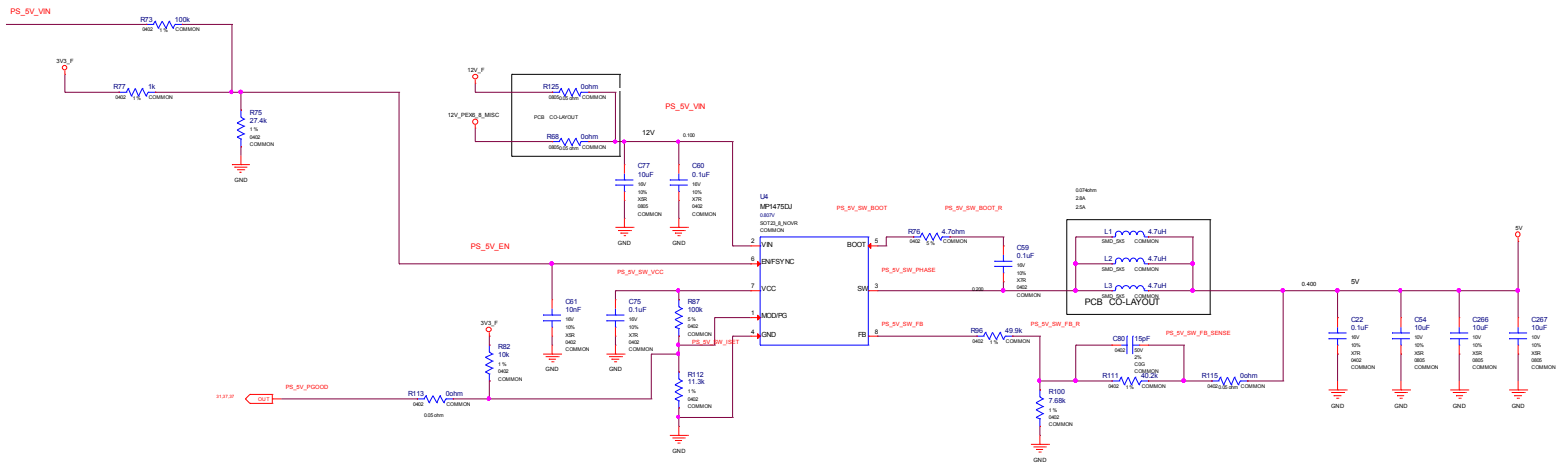

0.8V*(1+40.2K/7.68K)=4.9875V

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 5V

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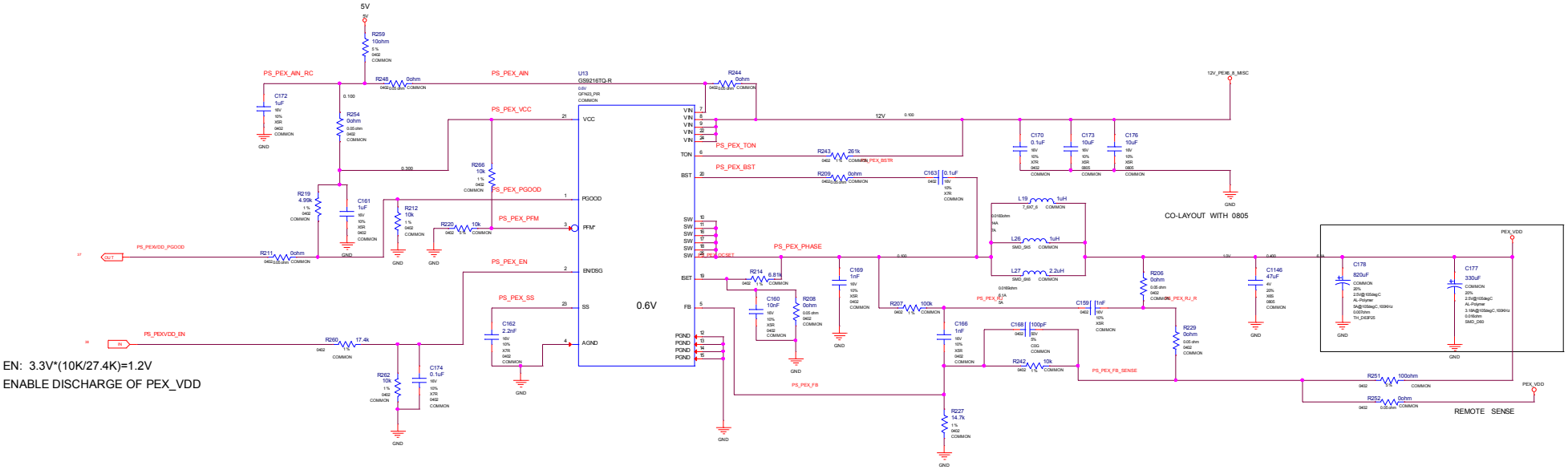
BOM REV	B	DATE	14-DEC-2018

PEX Switcher



EN: 3.3V*(10K/27.4K)=1.2V

ENABLE DISCHARGE OF PEX_VDD

0.6V*(1+10K/14.7K)=1.008V

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEXVDD

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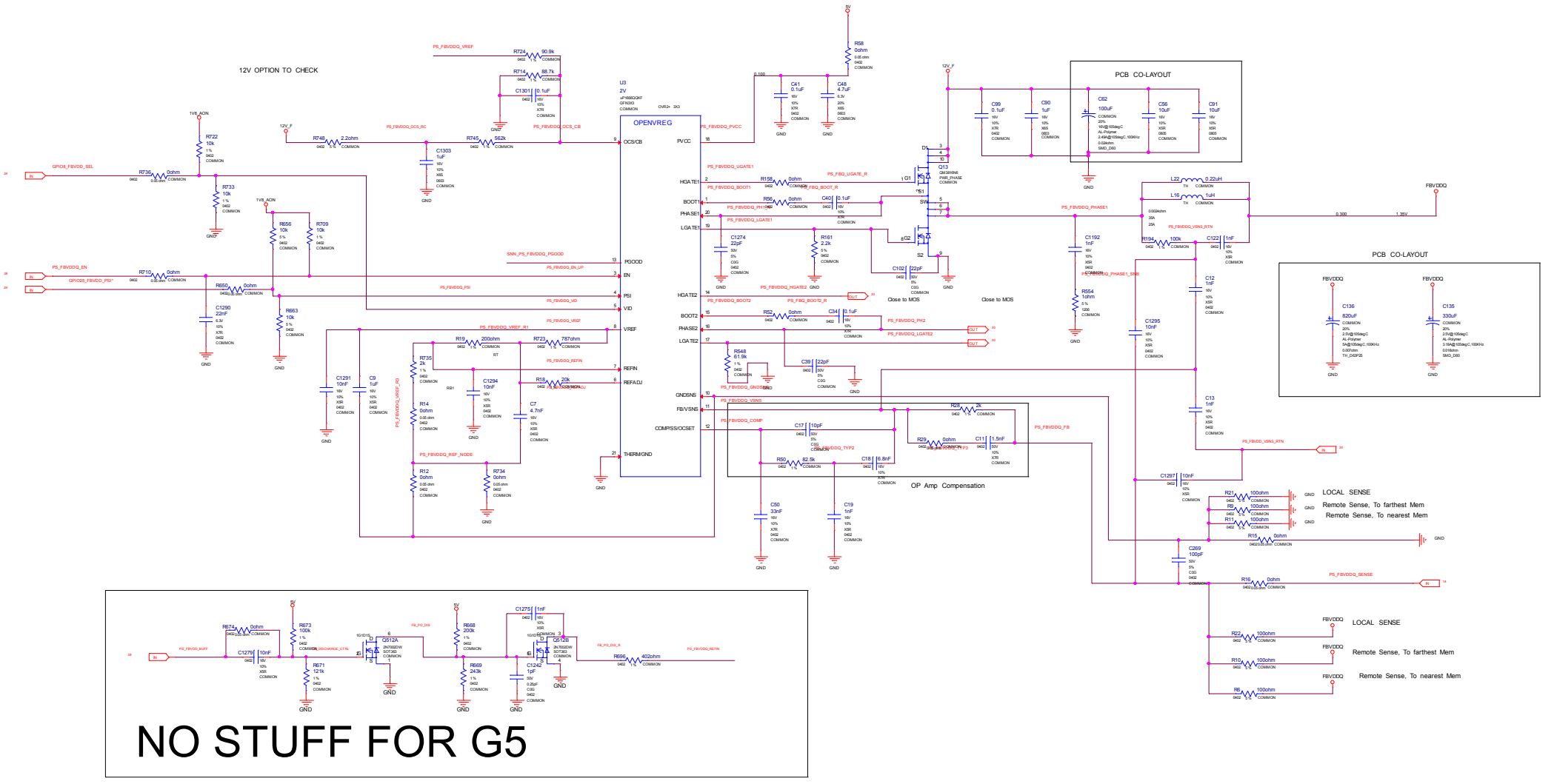

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDDQ

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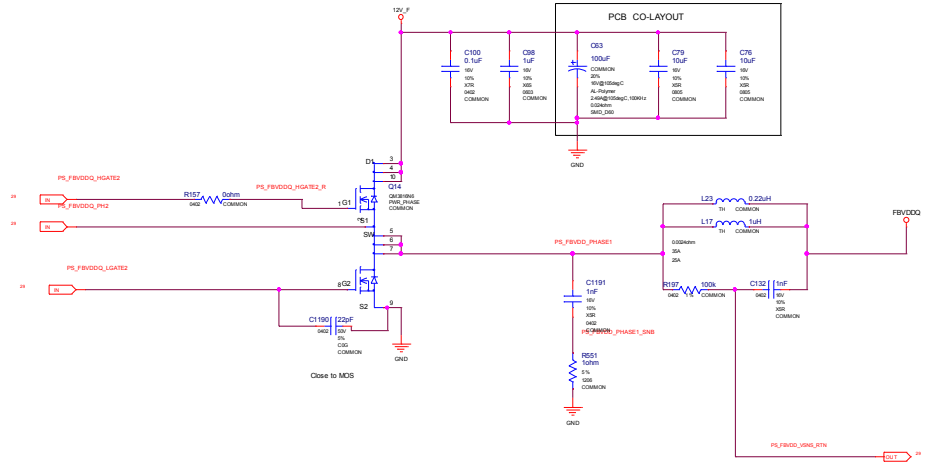
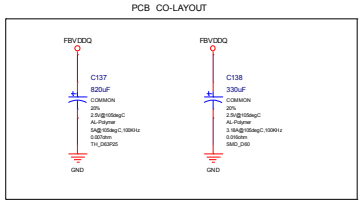
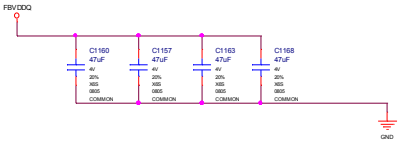
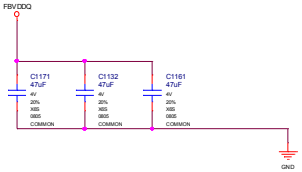
Page30: PS: FBVDDQ PH2









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PAGE DETAIL	PS: FBVDDQ PH2

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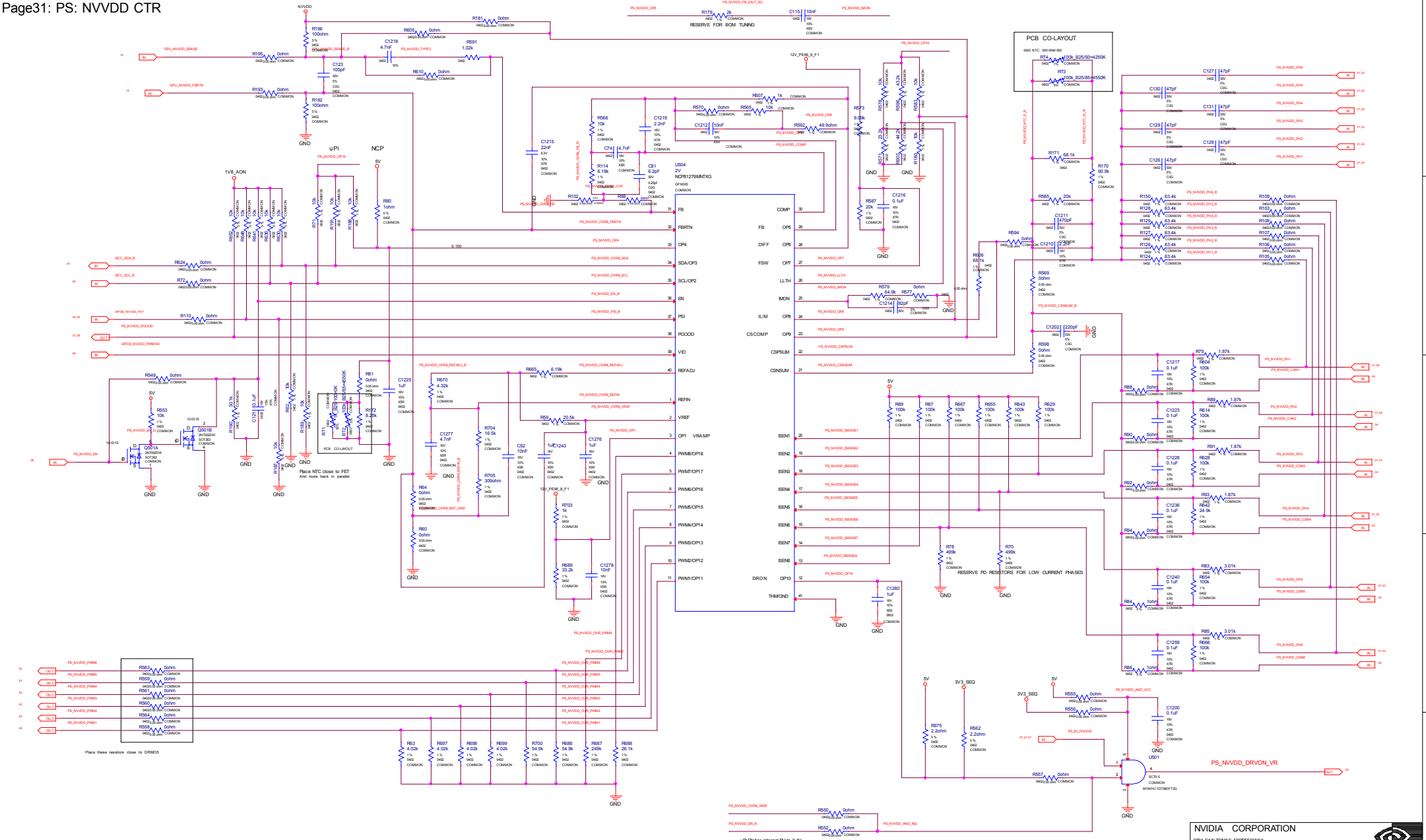
Page31: PS: NVVDD CTR



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Controller

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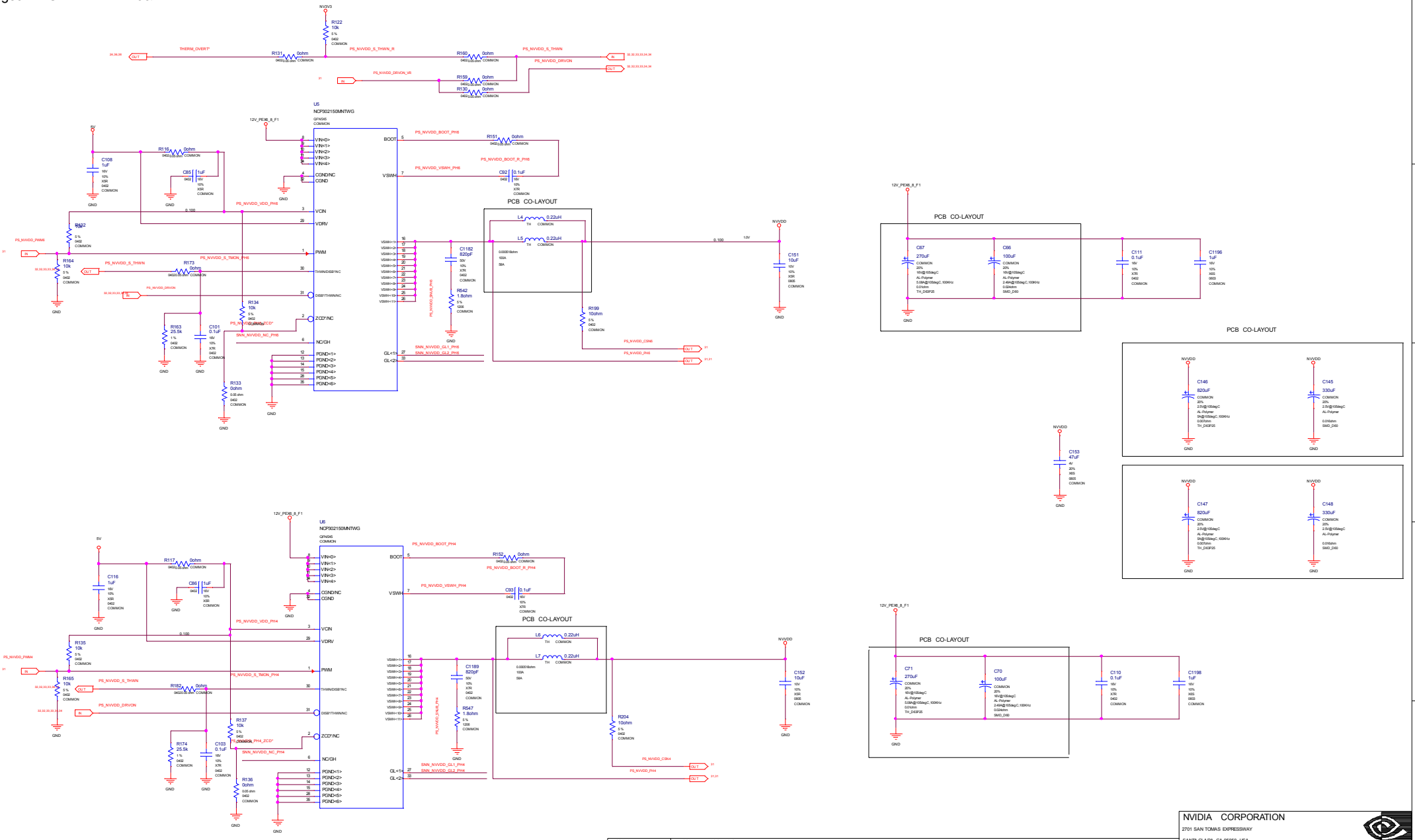
Page32: PS: NVVDD PH6&4



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 6,4

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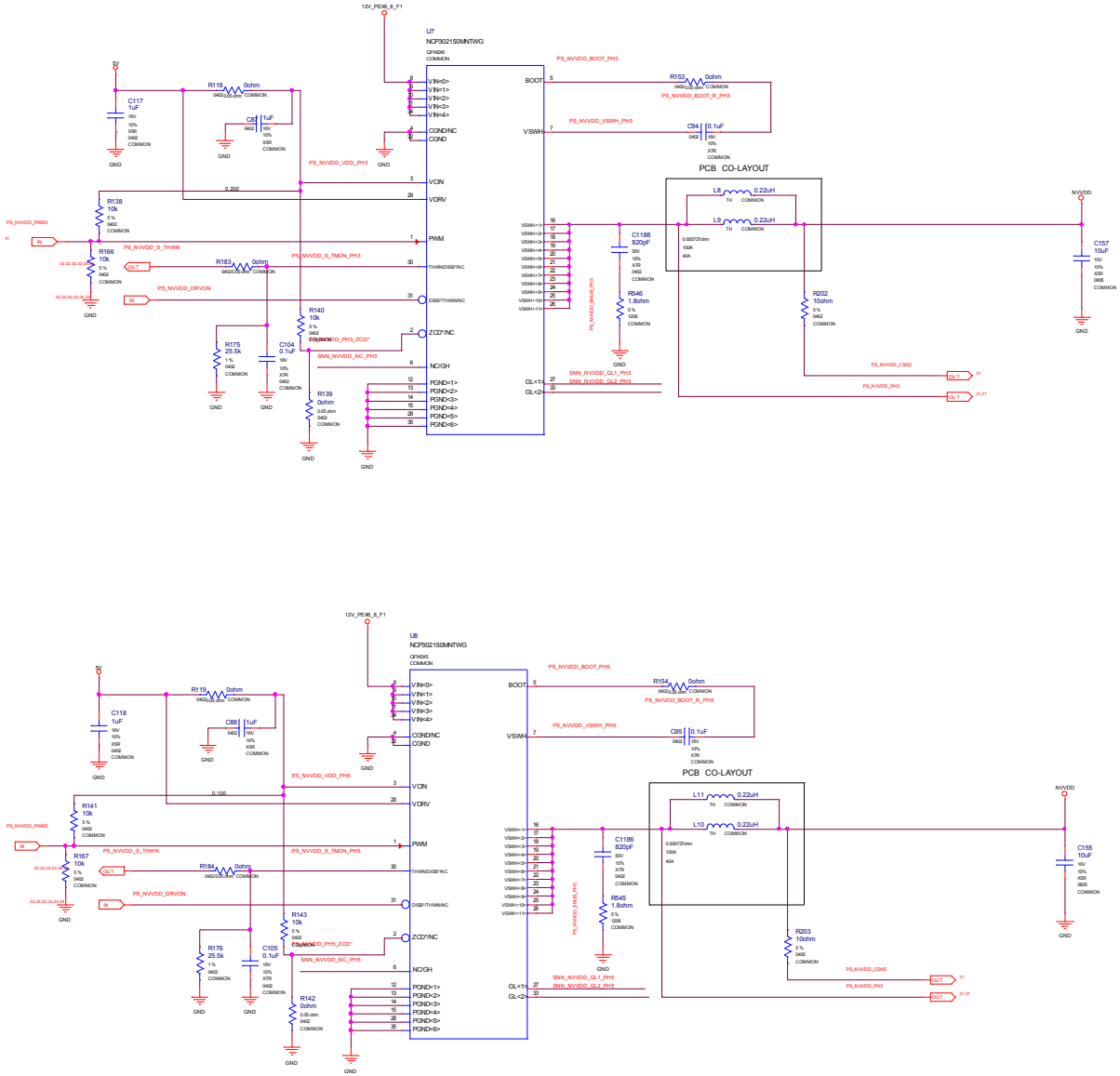
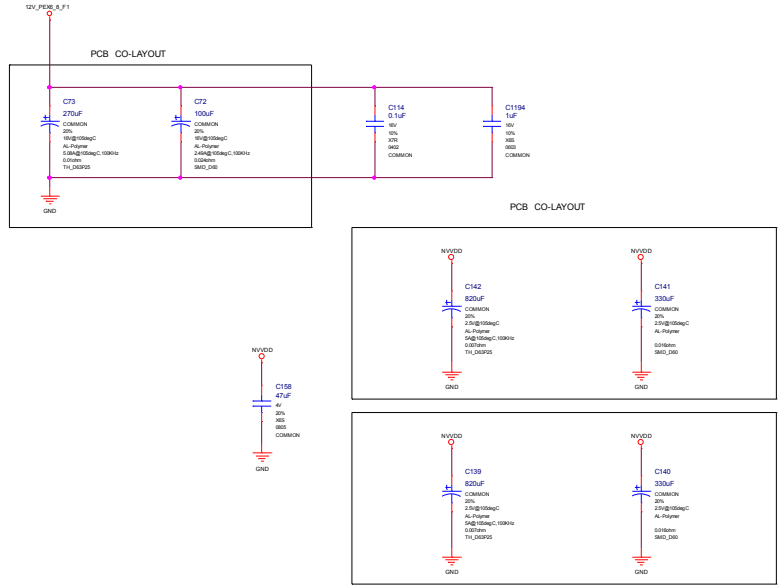
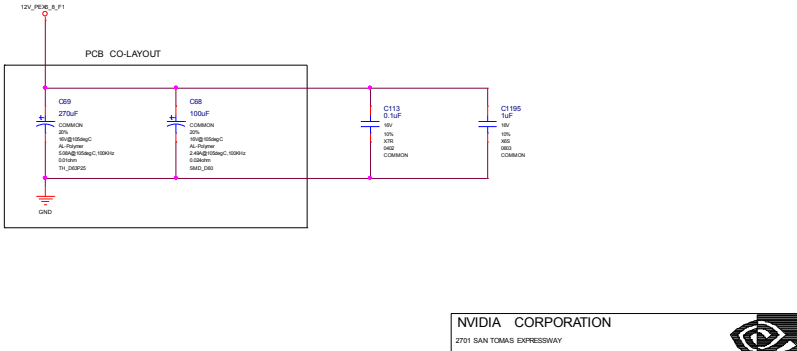
Page33: PS: NVVDD PH3&5







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 3,5

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PCB REV	PG165-A00	PAGE	33 OF 42
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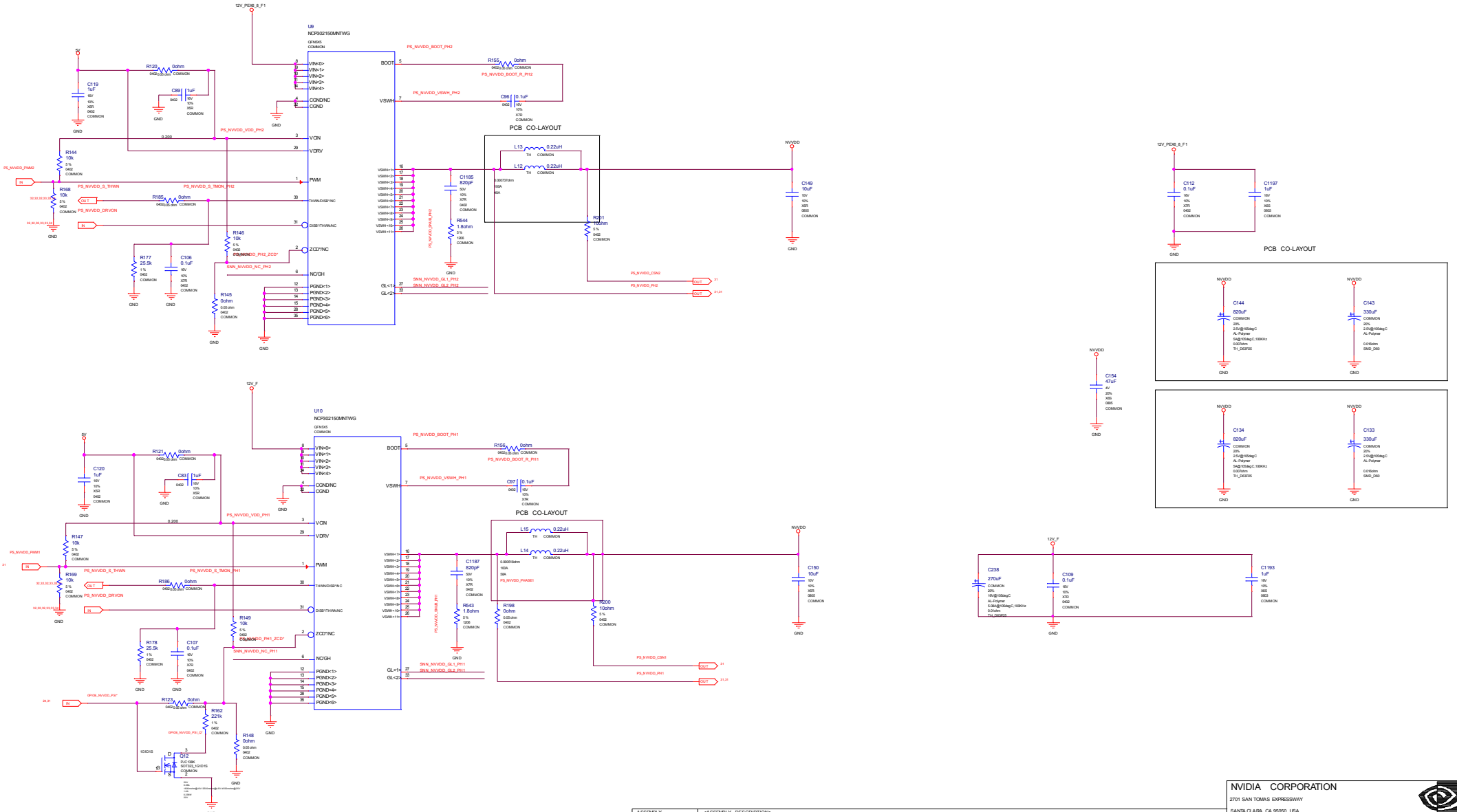
Page34: PS: NVVDD PH2&1



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PAGE DETAIL	PS: NVVDD Phase 2,1

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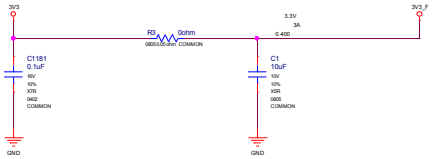
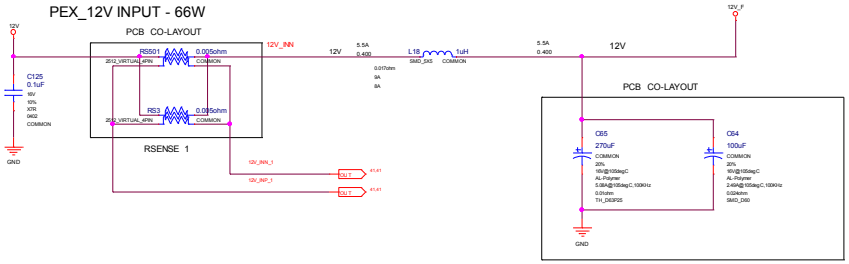
Page35: PS: PEX_INPUT, 12V_EXT_INPUT, FILTERING

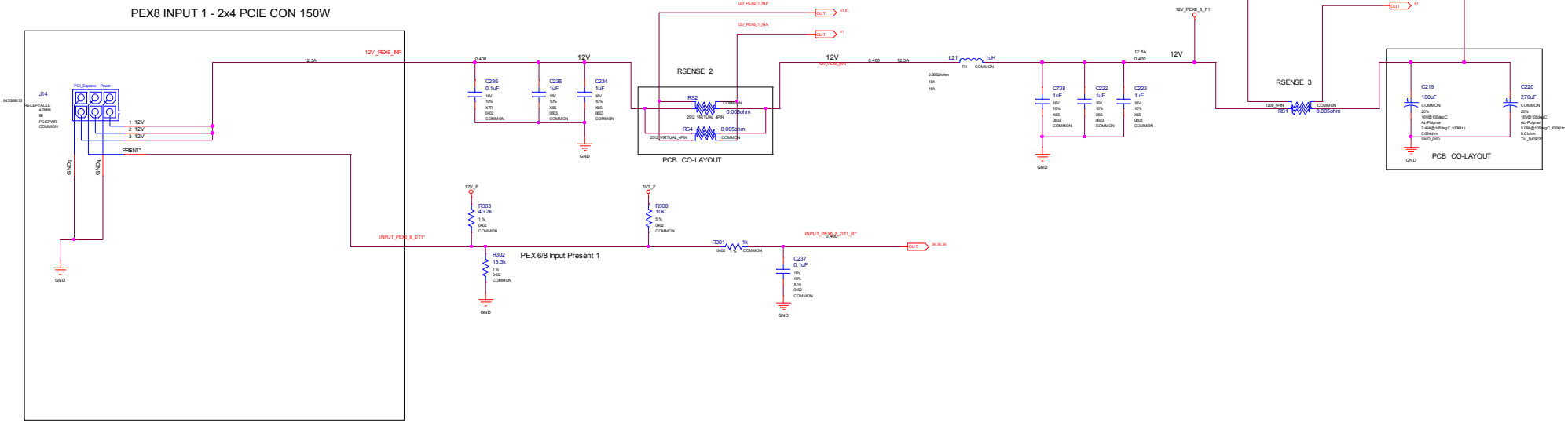
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEX_INPUT, 12V_EXT_INPUT, FILTERING

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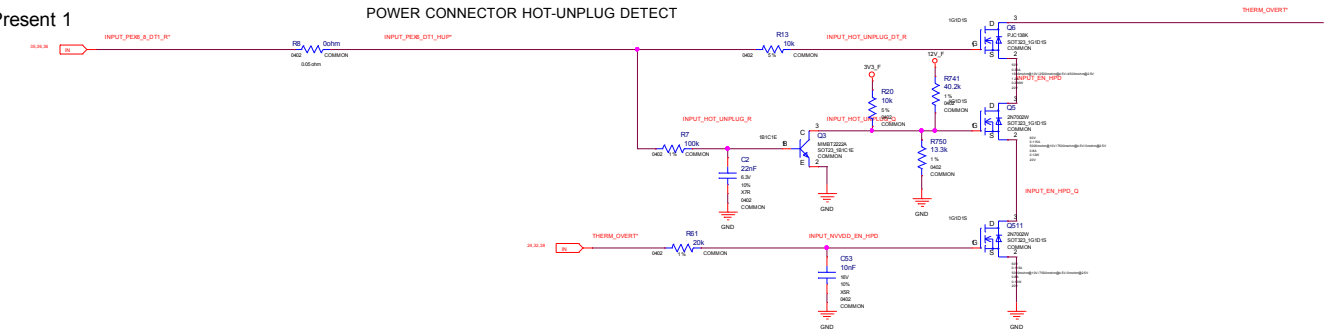
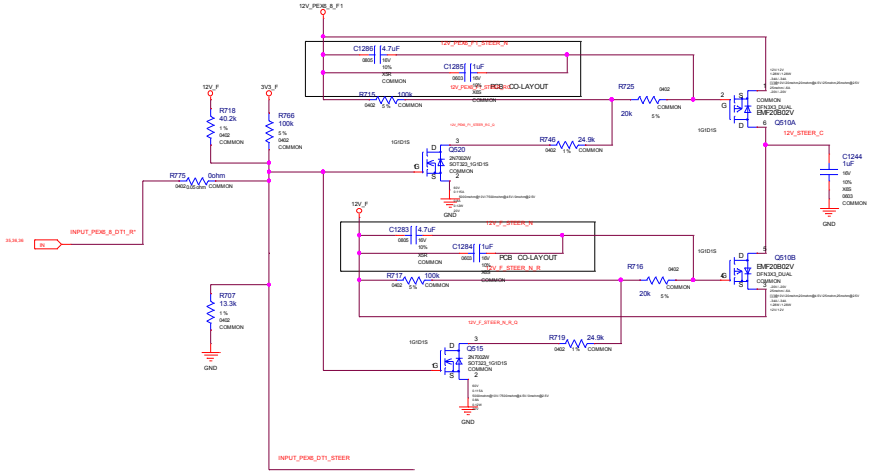
Page36: PS: CURRENT STEERING, UNDER POWER BOOT, HOT-UNPLUG

PEX Input Present 1

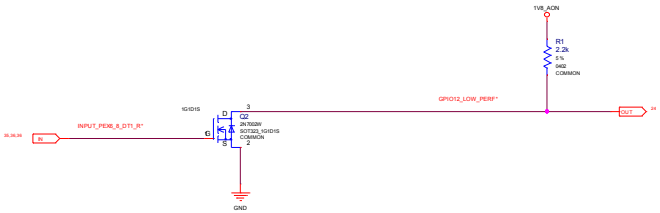


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: CURRENT STEERING,UPB,HOT-UNPLUG

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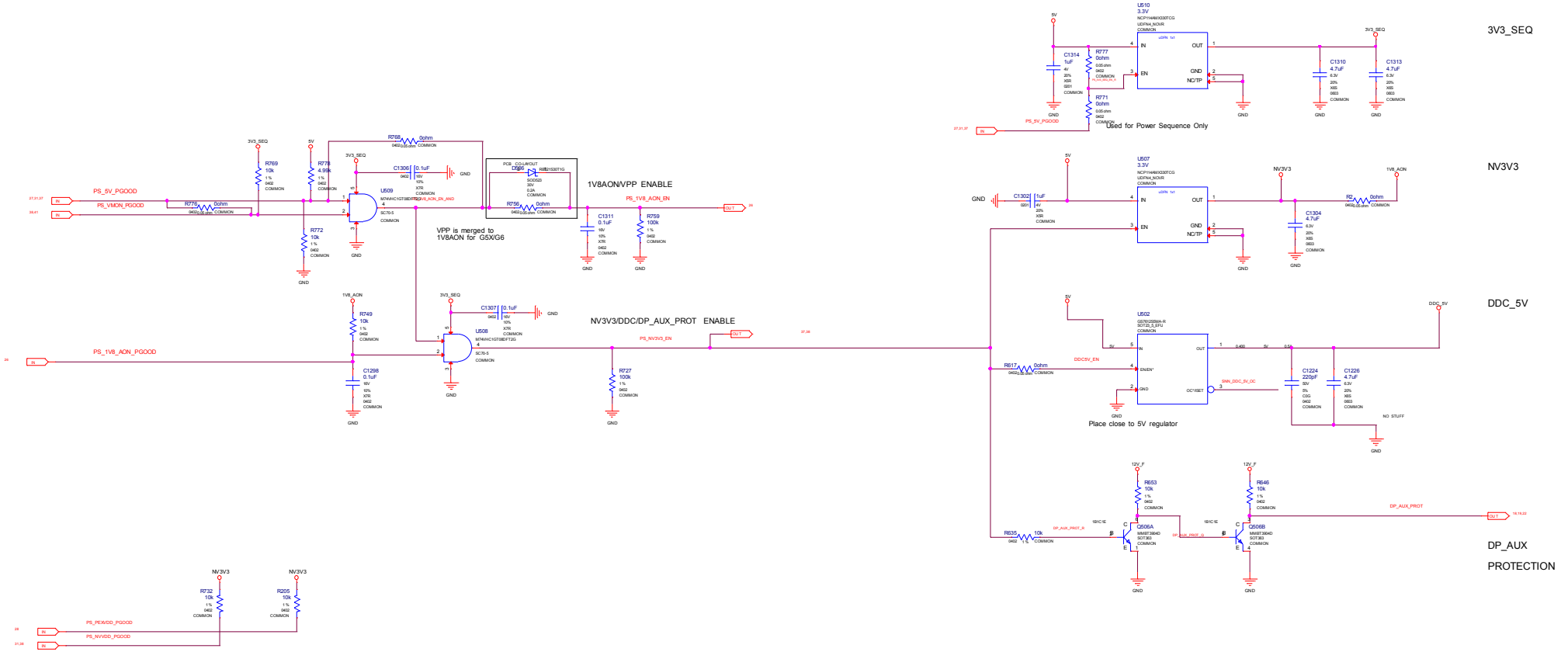
Page37: SEQ:1V8_AON, 3V3_SEQ, NV3V3, DDC_5V, DP_AUX_PROT



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PAGE DETAIL	SEQ: 1V8_AON, 3V3_SEQ, NV3V3, DDC_5V, DP_AUX_PROT

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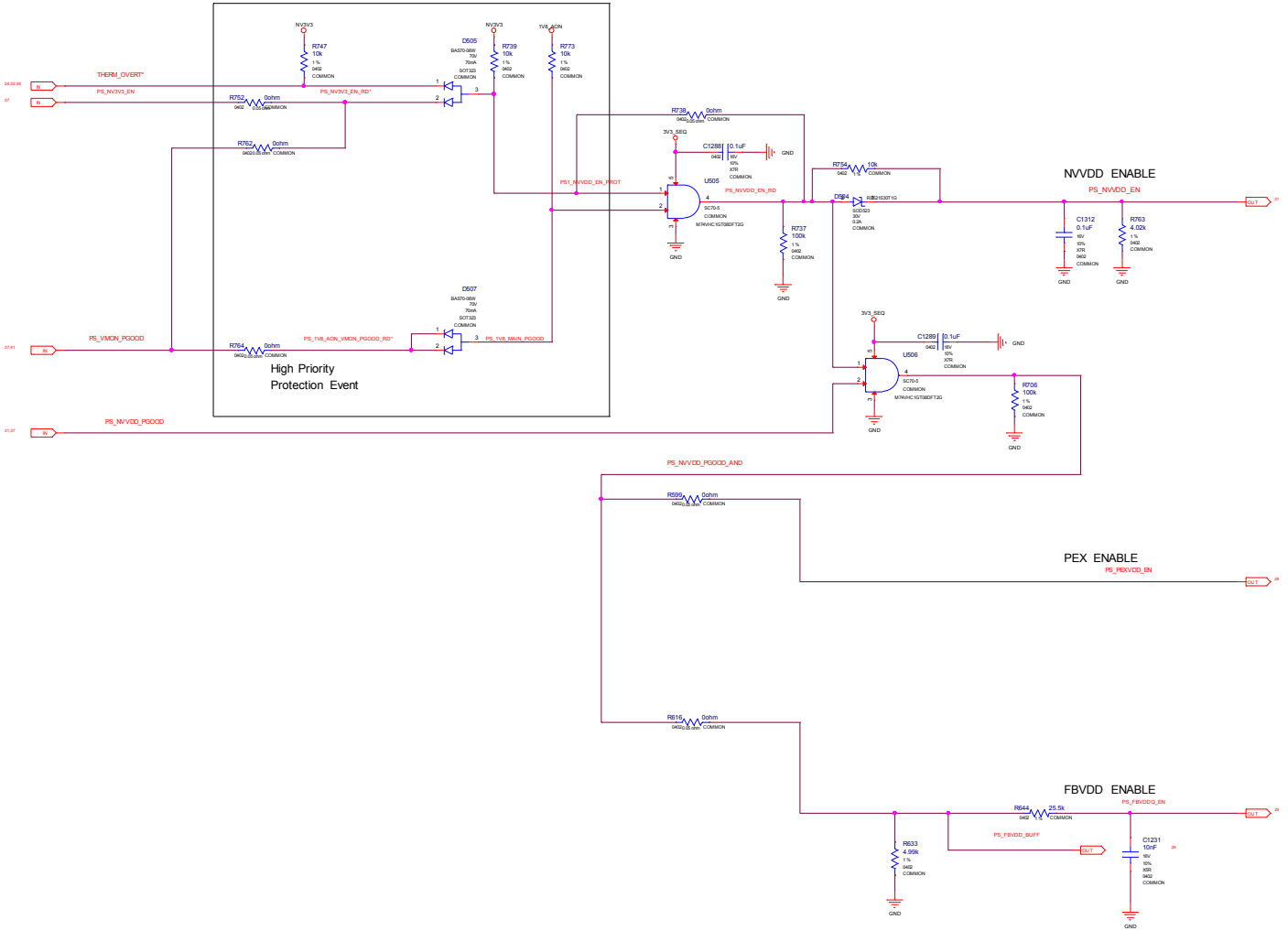
BOM REV	B	DATE	14-DEC-2018

Page38: SEQ:NVVDD, PEX, FBVDDQ ENABLE



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NVVDD, PEX, FBVDDQ ENABLE

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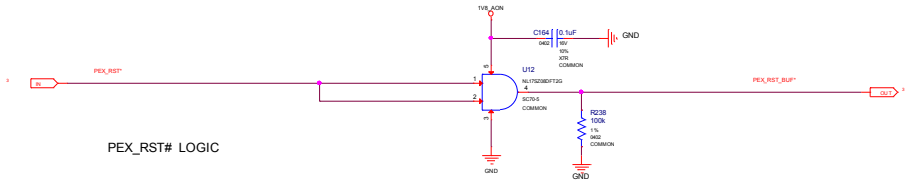
Page39: SEQ:MISC

PU ON GPU SIDE
NC ON GOLD FINGER SIDE

PU ON GPU SIDE
NC ON GOLD FINGER SIDE



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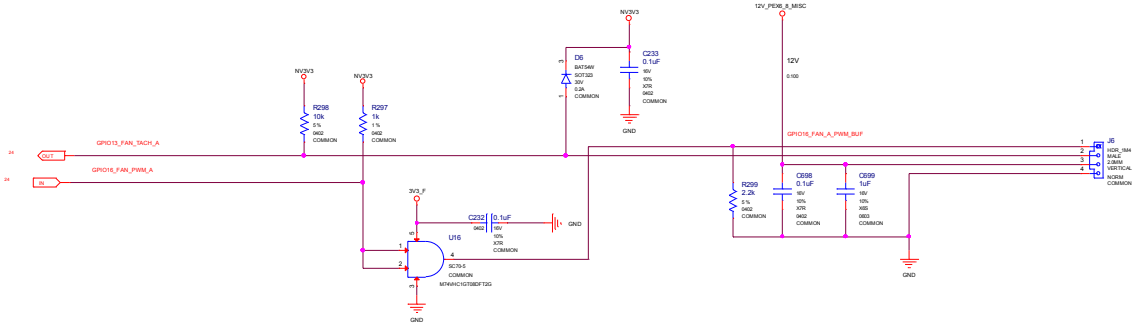
Page40: FAN



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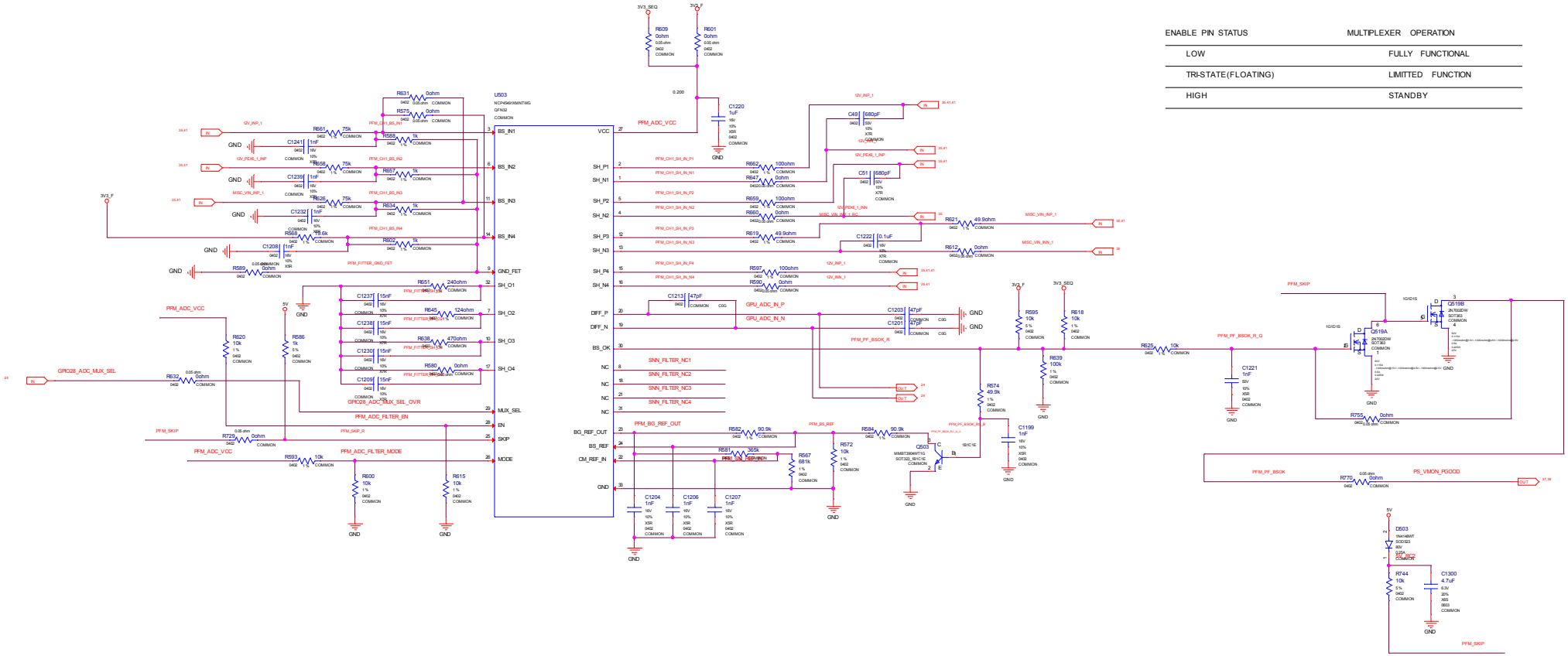
MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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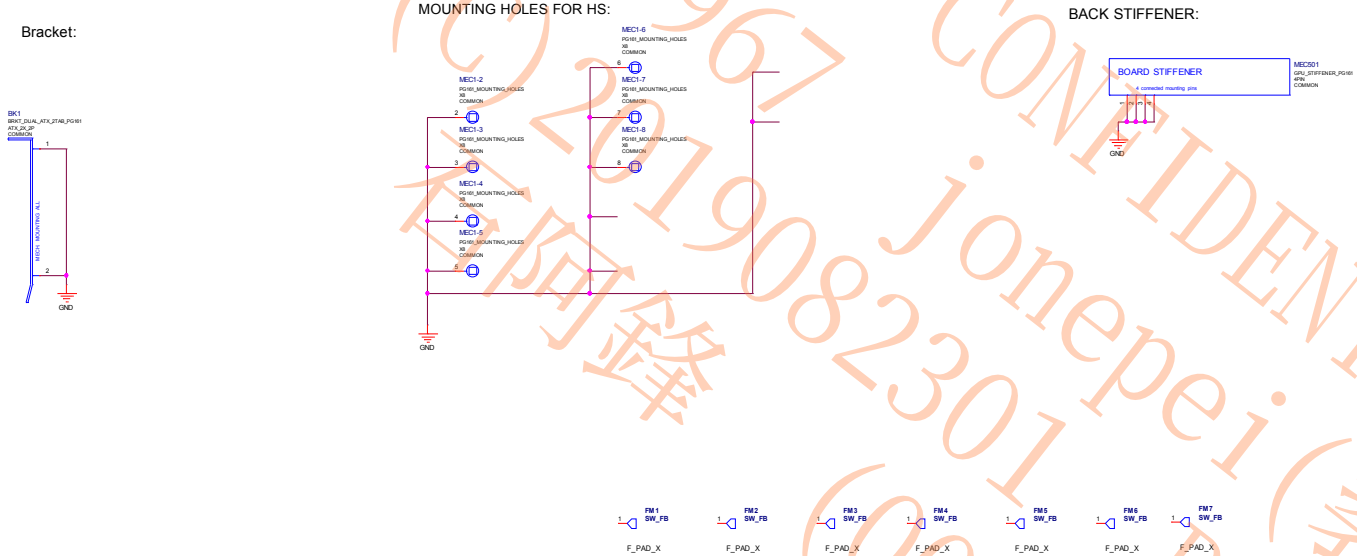

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