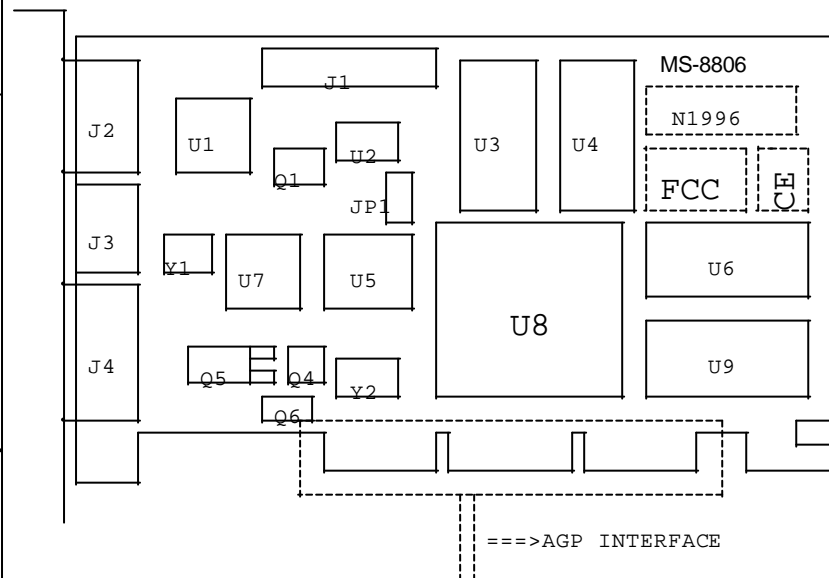


HISTORY :

1. MS-8806 VER:1.1 32MB SDRAM
- 2."0" MEANS "RESERVE"
- 3."1" MEANS "OPTIONAL"

VER1.0 VS VER1.1

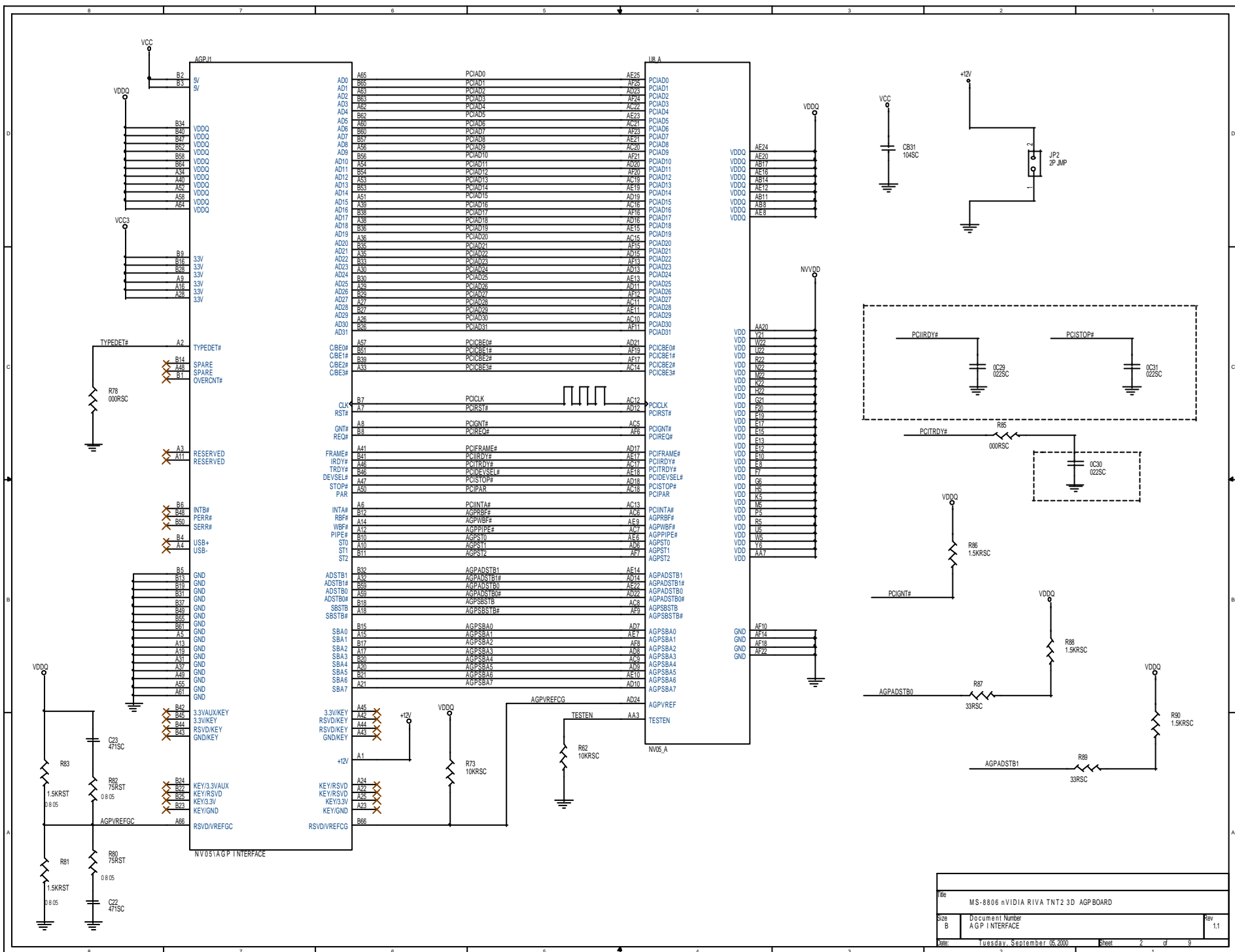
- 1.DDC ADD 100P CAP
- 2.ADD 0 OHM WITH DIGITAL GROUND AND ANALOG GROUND



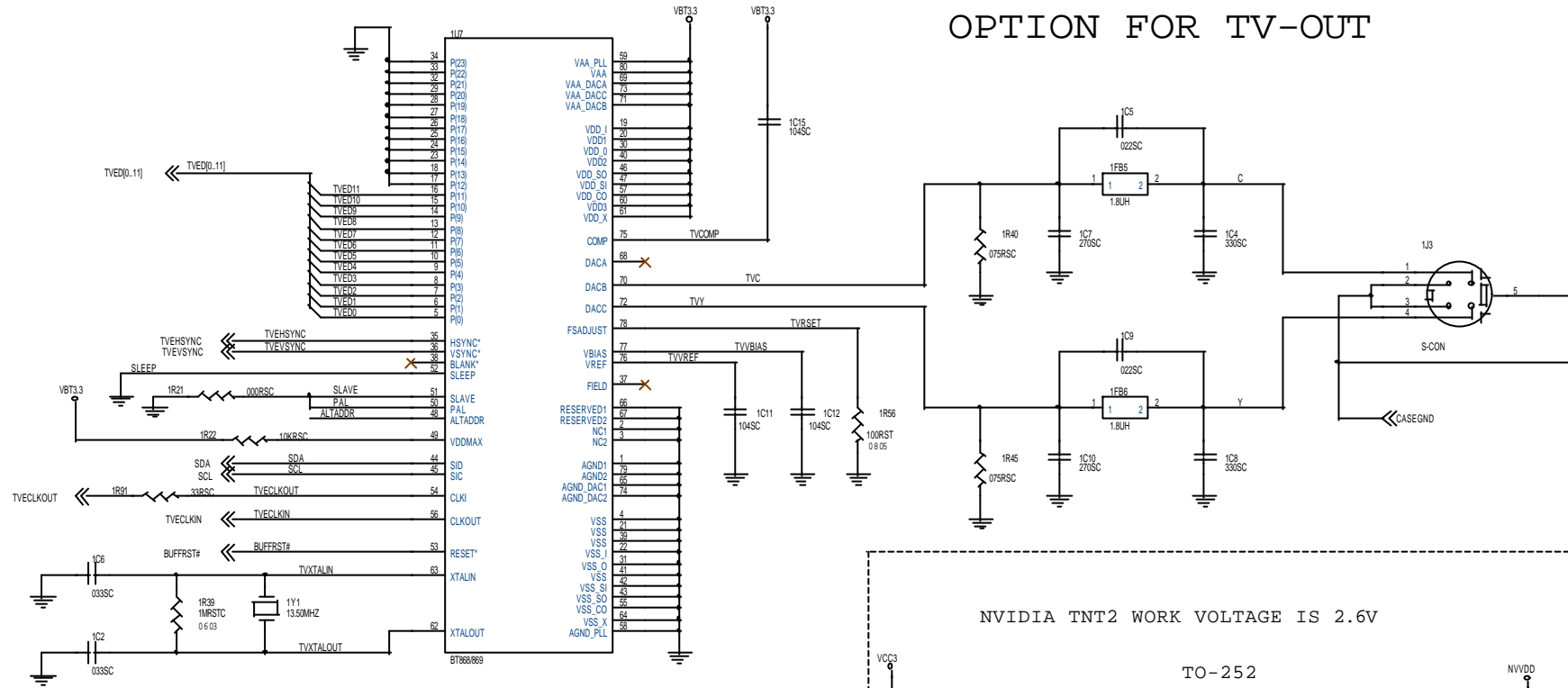
U8:nVIDIA RIVA TNT2 AGP GRAPHICS PROCESSOR
 U7:BROOKTREE BT868 TV-OUT (OPTIONAL)
 U5:VGA BIOS PLCC
 U2:QS3861 (RESERVE)
 U3,U4,U6,U9:SDRAM 2M*32
 U1:SiI 154 DFP CHIP (OPTIONAL)
 Y1:CRYSTAL 13.50MHZ TV-OUT USE (OPTIONAL)
 Y2:CRYSTAL 14.31818MHZ
 J3:S-VIDEO CONNECTOR TV-OUT (OPTIONAL)
 J1:FEATURE CONNECTOR (RESERVE)
 J4:VGA CONNECTOR
 J2:DIGITAL FLAT PANEL CONNECTOR (OPTIONAL)
 JP1:TV-OUT NTSC/PAL JUMPER (OPTIONAL)
 Q1:TL431 SMD
 Q5:MOSFET - N
 Q6:TL431 DIP (OPTIONAL)
 Q4:TL431 SMD

L1W
 P2.SCH
 P3.SCH
 P4.SCH
 P5.SCH
 P6.SCH
 P7.SCH
 P8.SCH
 P9.SCH

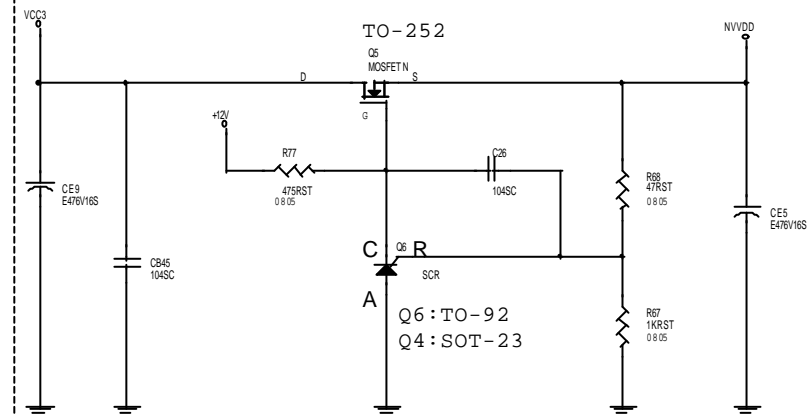
File		
MS-8806 nVIDIA RIVA TNT2 3D AGP BOARD		
Size	Document Number	Rev
B	HISTORY LIST 32MB 2M *32SDRAM	1.1
Date	Tuesday, September 05, 2000	
Sheet	1 of 9	



OPTION FOR TV-OUT



NVIDIA TNT2 WORK VOLTAGE IS 2.6V

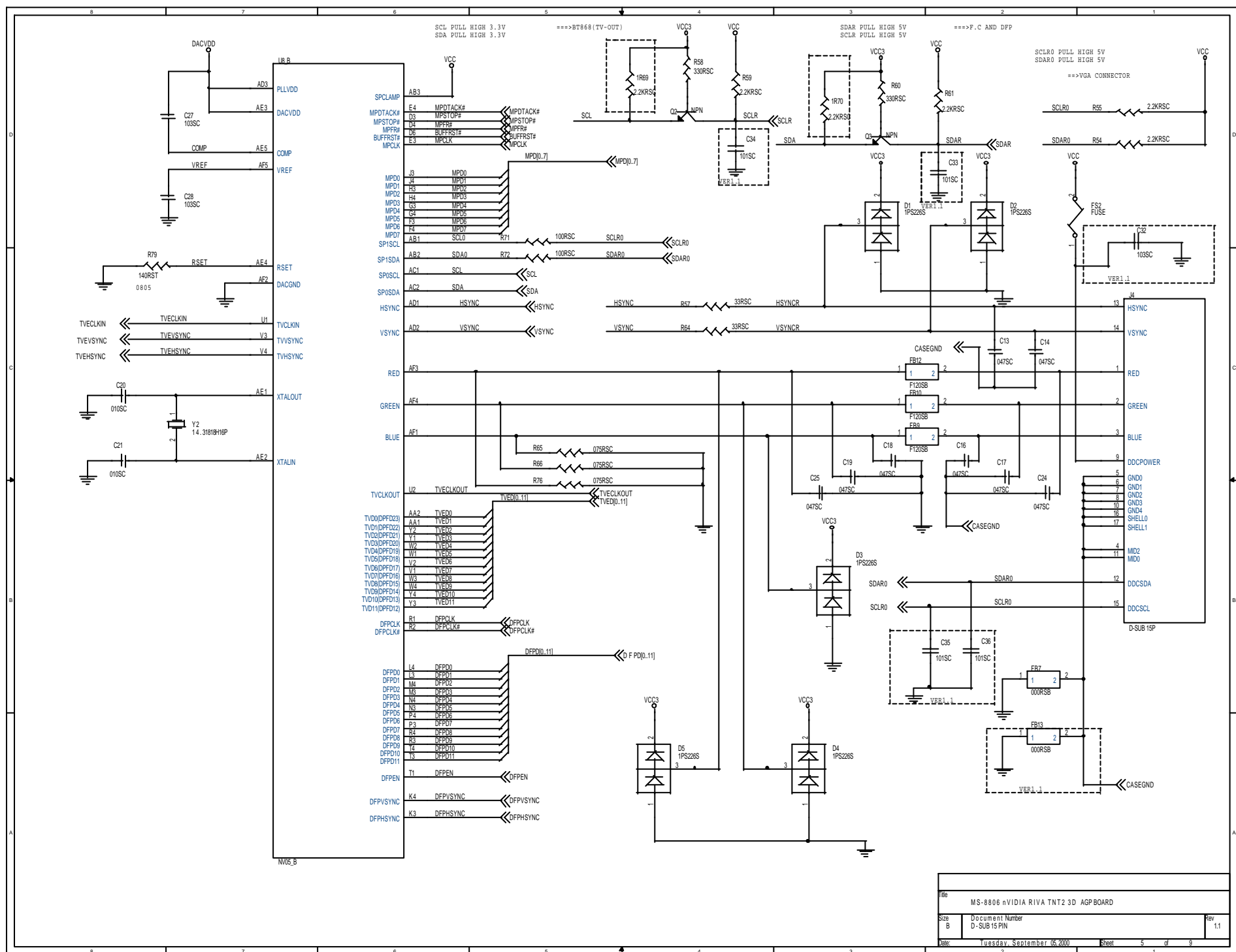


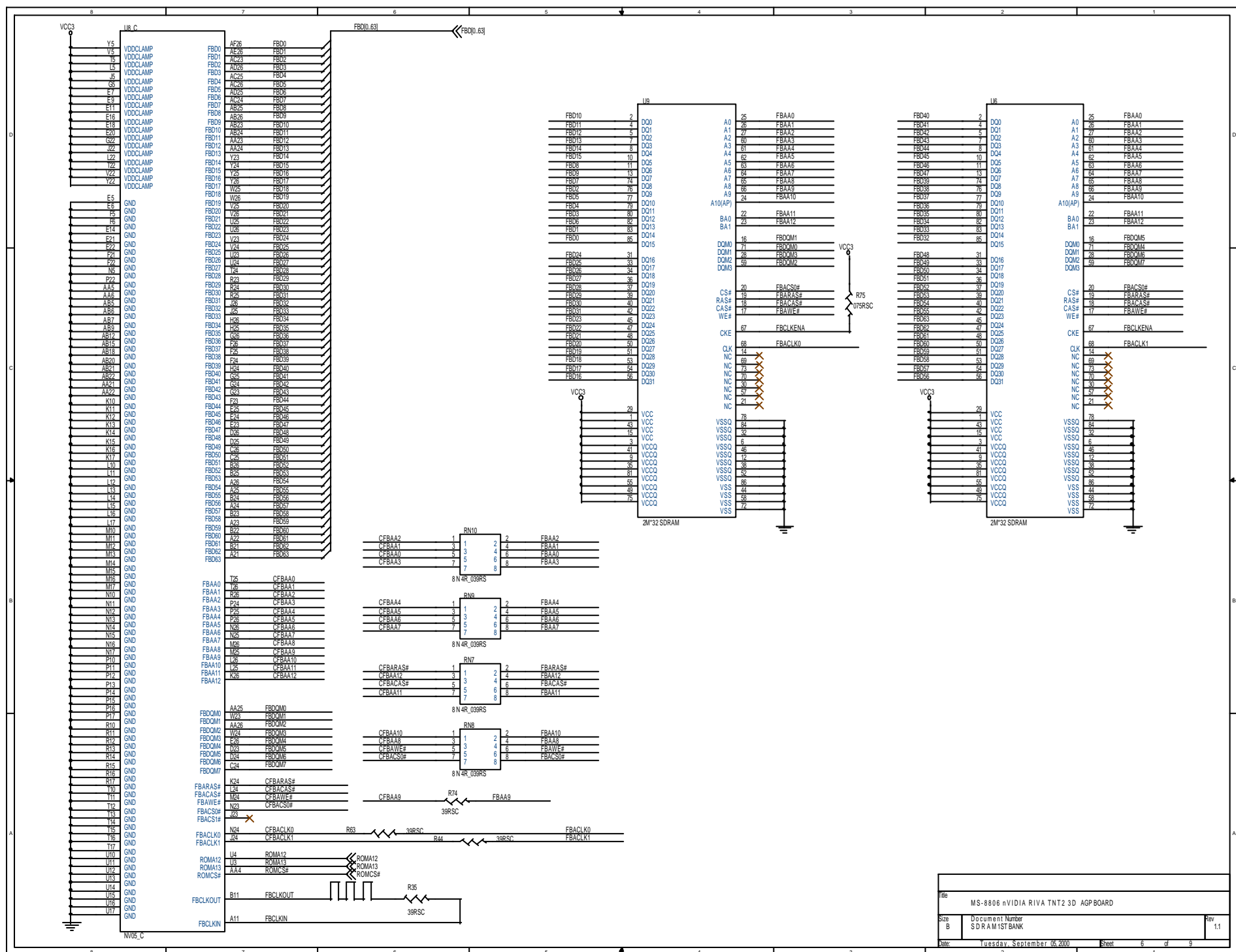
MS-8806 nVIDIA RIVA TNT2 3D AGP BOARD		
Size	Document Number	Rev
B	BROOKTREE 868/869 TV-OUT ENCODER	1.1
Date	Tuesday, September 05, 2000	
Sheet	3	of 9

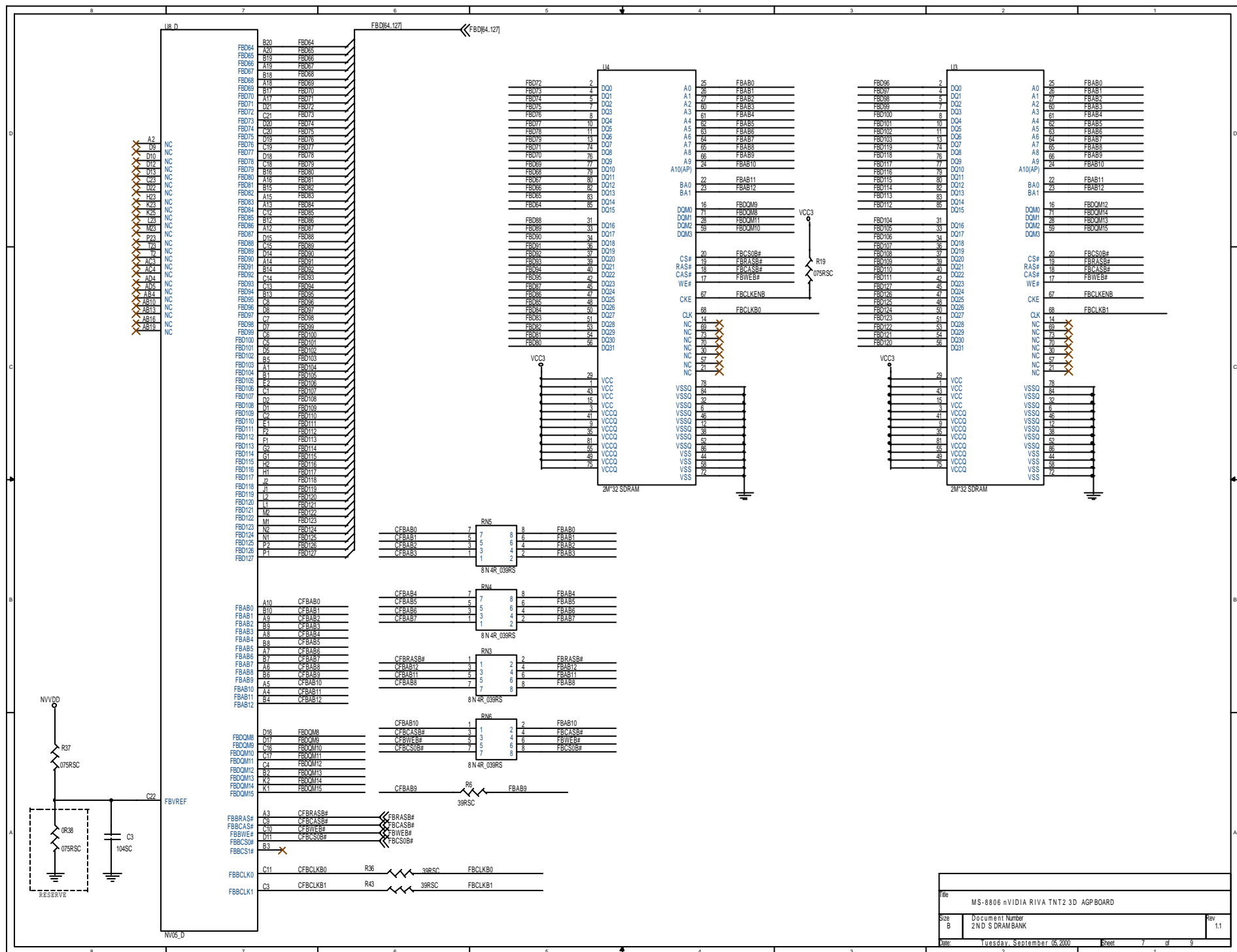
- POWER STRAPING
- BIOS

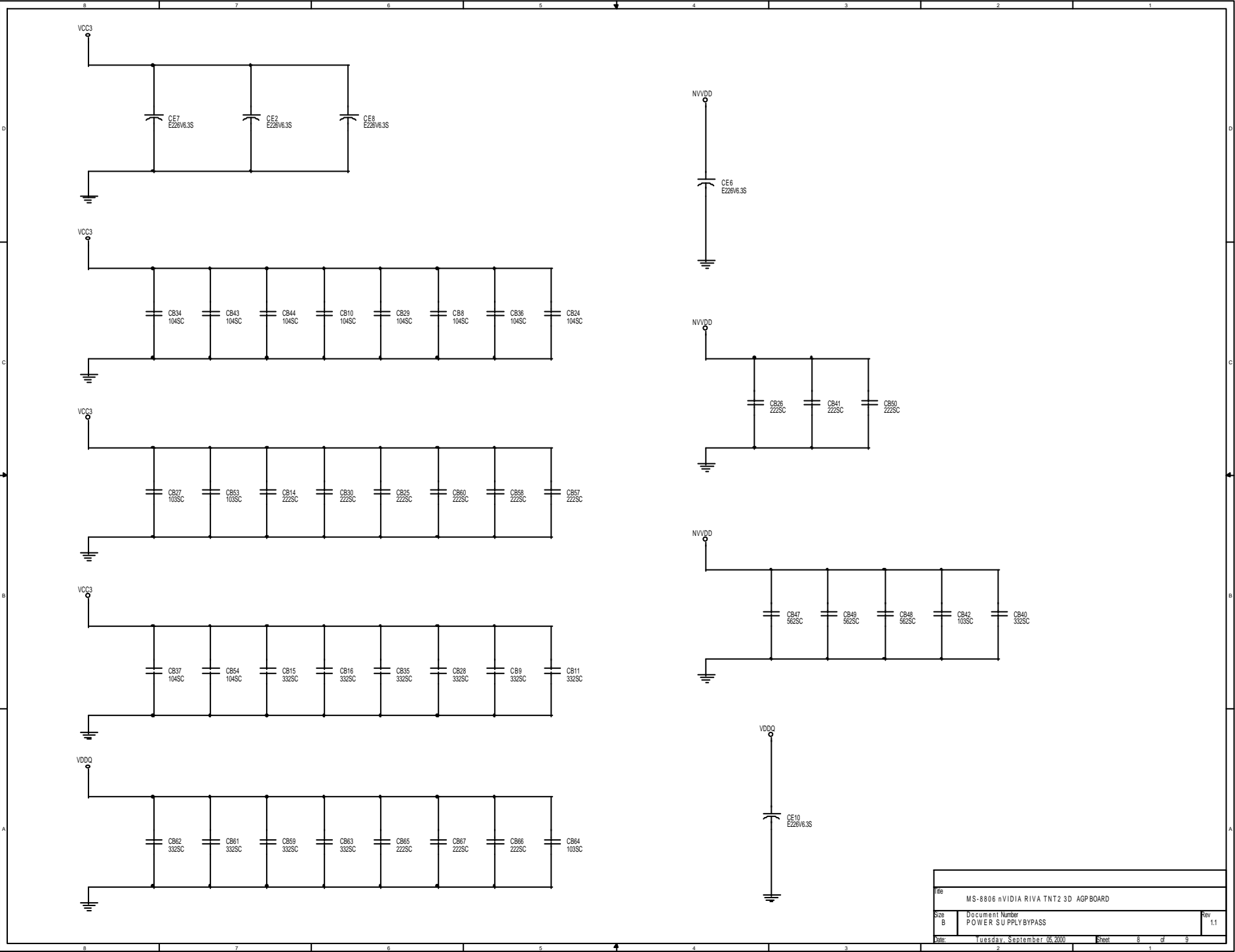
- POWER STRAPING
- BIOS

DERE 19

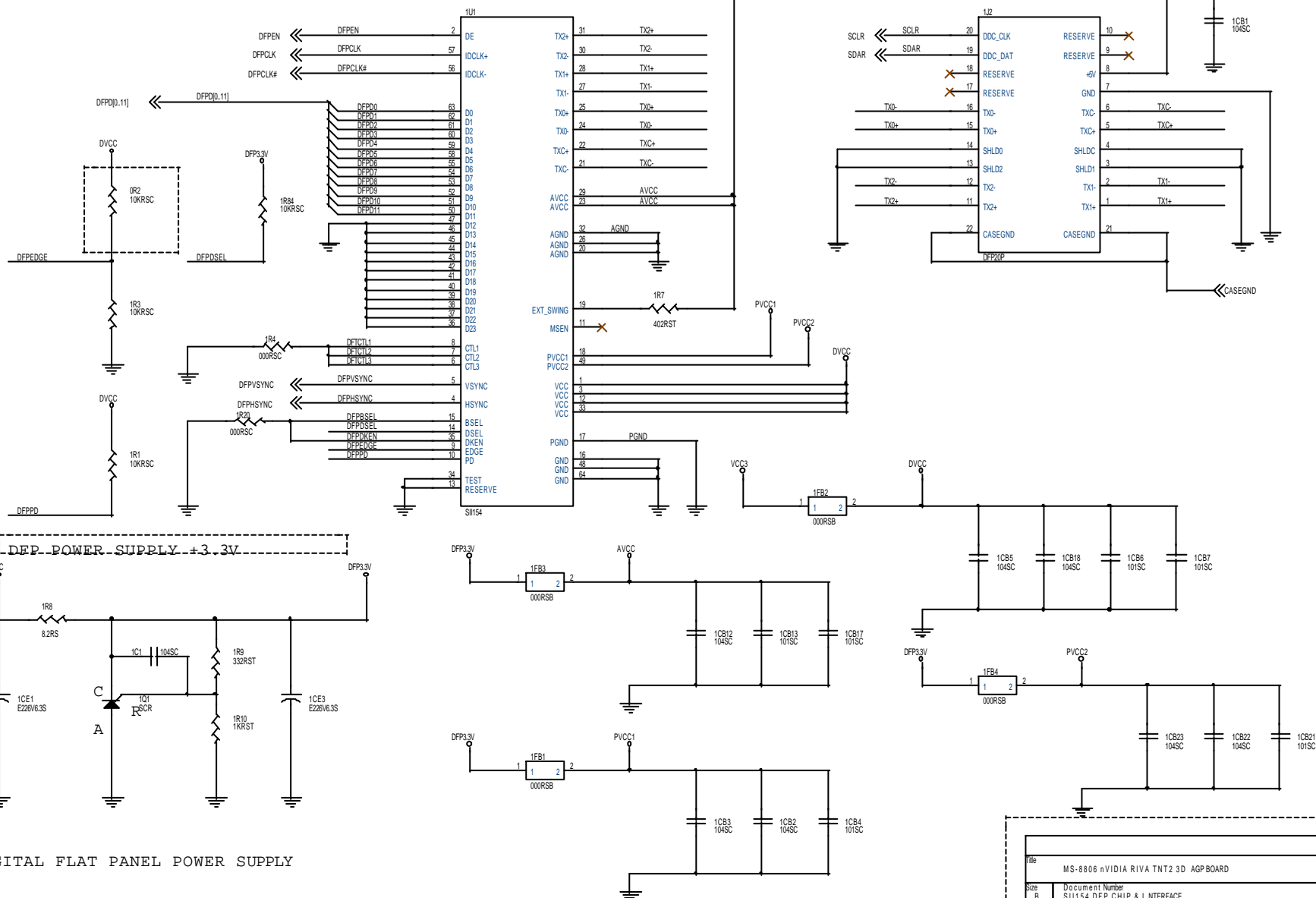








OPTION FOR Digital Flat Panel USE



DIGITAL FLAT PANEL POWER SUPPLY

Title			
MS-8806 nVIDIA RIVA TNT2 3D AGP BOARD			
Size	Document Number	Rev	
B	SI1154 DFP CHIP & I INTERFACE	1.1	
Date	Tuesday, September 05 2000	Sheet	9 of 9