45P214-NV45/48E Board

NV45/48E P214_B03 - NV45/48E BGA, 16 x 32MB DDR3 (16 x 8Mx32 = 512MB)
Dual TMDS (dual link), Internal TVout, TVin.
Framelock connector.

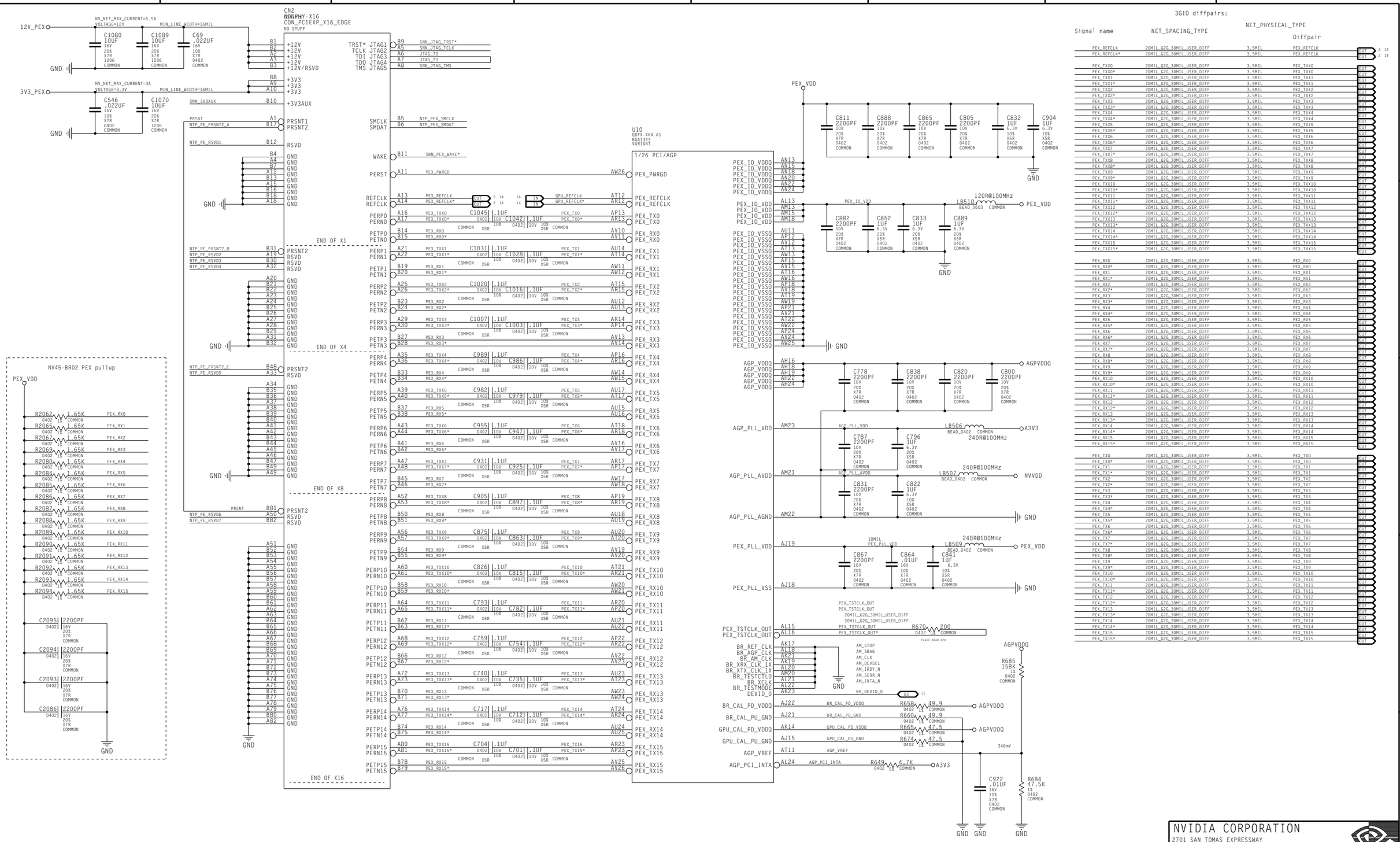
SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10214-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU9999COSTING	600-10214-9999-400	Costing SKU: NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo, BRINGUP SKU
2	SKU5000	600-50214-0000-400	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
3	SKU0000	600-10214-0000-400	DSKT SKU0000:NV45U-P214 B03, 512MB, GDDR3, dual SL-DVI-I, TVout
4	SKU0001	600-10214-0001-400	DSKT SKU0001:NV45U-P214 B03, 512MB, GDDR3, dual SL-DVI-I, VIVO
5	SKU5001	600-50214-0001-400	WKST SKU0001:QDFX4400-P214 B03,512MB, GDDR3, dual DL-DVI-I,Stereo
6	SKU0002	600-10214-0002-400	DSKT SKU0002:NV48E-U-P214 B03, 512MB, GDDR3, dual SL-DVI-I, TVout
7	SKU0003	600-10214-0003-400	DSKT SKU0003:NV48E-U-P214 B03, 512MB, GDDR3, dual SL-DVI-I, VIVO
8	SKU0004	600-10214-0004-400	DSKT SKU0004:NV48E-U-P214 B03, 256MB, GDDR3, dual SL-DVI-I, VIVO
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

Table of Contents:

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Table of Contents

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

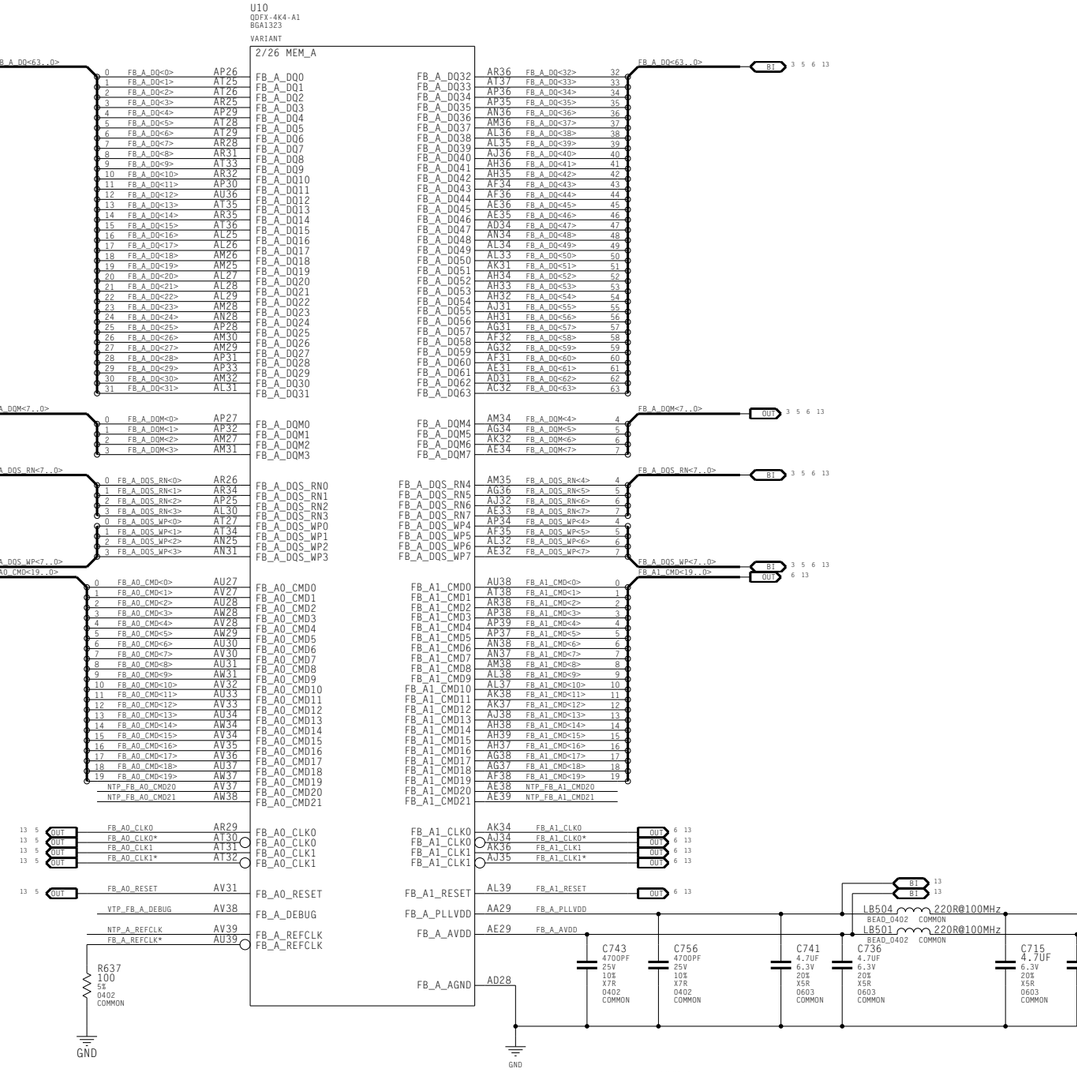
NV_PN	600-10214-base-sch		
ID	design	PAGE	1 OF 31
NAME	TSchirmer	DATE	3-NOV-2004

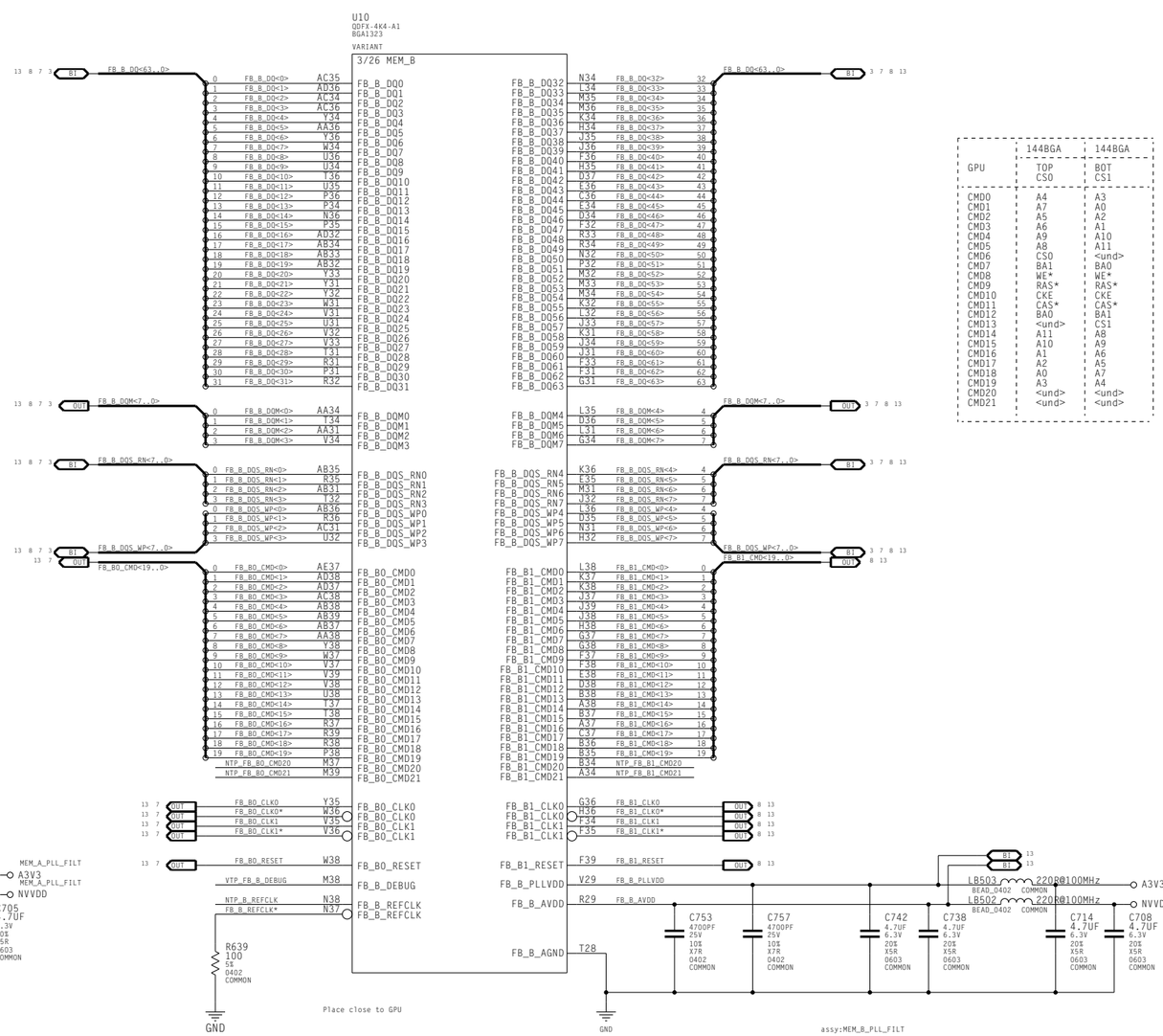


ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	PCI EXPRESS INTERFACE

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	2 OF 31
NAME	TSchirmer	DATE	4-NOV-2004





GPU	144BGA TOP CS0	144BGA BOT CS1
CMD0	A4	A3
CMD1	A7	A0
CMD2	A5	A2
CMD3	A6	A1
CMD4	A9	A10
CMD5	A8	A11
CMD6	CS0	<und>
CMD7	BA1	BA0
CMD8	WE*	WE*
CMD9	RAS*	RAS*
CMD10	CKE	CKE
CMD11	CAS*	CAS*
CMD12	BA0	BA1
CMD13	<und>	CS1
CMD14	A11	A8
CMD15	A10	A9
CMD16	A1	A6
CMD17	A2	A5
CMD18	A0	A7
CMD19	A3	A4
CMD20	<und>	<und>
CMD21	<und>	<und>

ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Memory: FB_A & FB_B Partitions

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	3 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

U10
QDFX-4K4-A1
BGA1323
VARIANT
4/26 MEM_C

U10
QDFX-4K4-A1
BGA1323
VARIANT
5/26 MEM_D

GPU	144BGA TOP CS0	144BGA BOT CS1
CMD0	A4	A3
CMD1	A7	A0
CMD2	A5	A2
CMD3	A6	A1
CMD4	A9	A10
CMD5	A8	A11
CMD6	CSO	<und>
CMD7	BA1	BA0
CMD8	WE*	WE*
CMD9	RAS*	RAS*
CMD10	CKE	CKE
CMD11	CAS*	CAS*
CMD12	BA0	BA1
CMD13	<und>	CS1
CMD14	A11	A8
CMD15	A10	A9
CMD16	A1	A6
CMD17	A2	A5
CMD18	A0	A7
CMD19	A3	A4
CMD20	<und>	<und>
CMD21	<und>	<und>

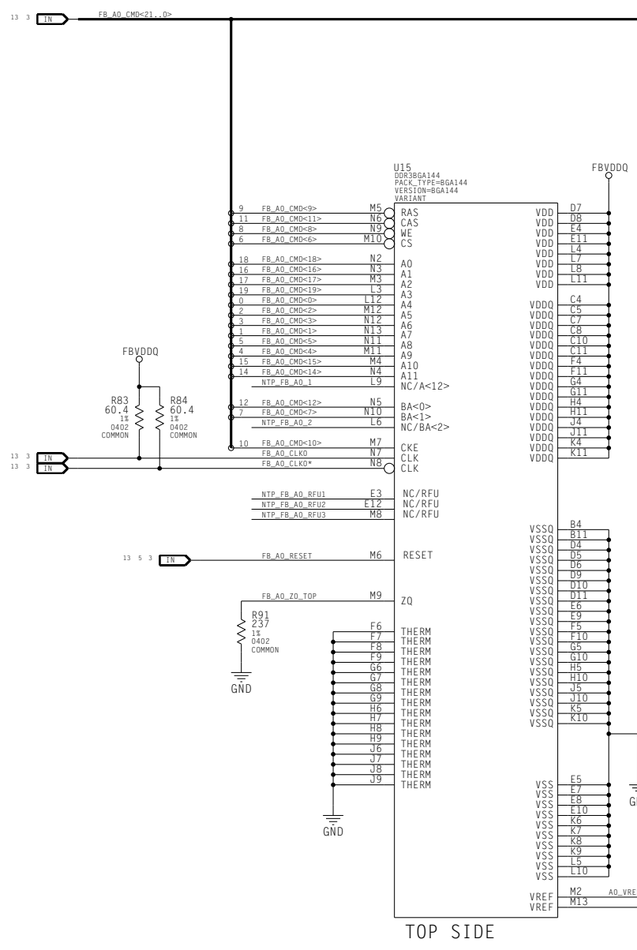
assy:MEM_C_PLL_FILT

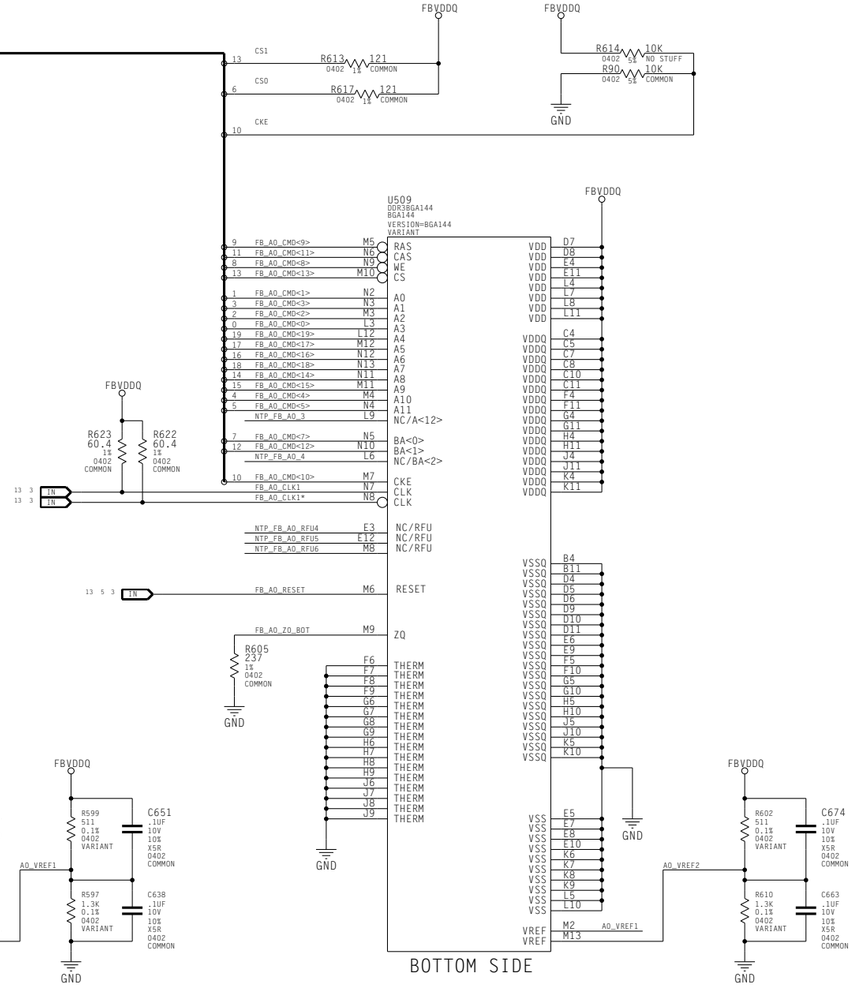
assy:MEM_C_PLL_FILT

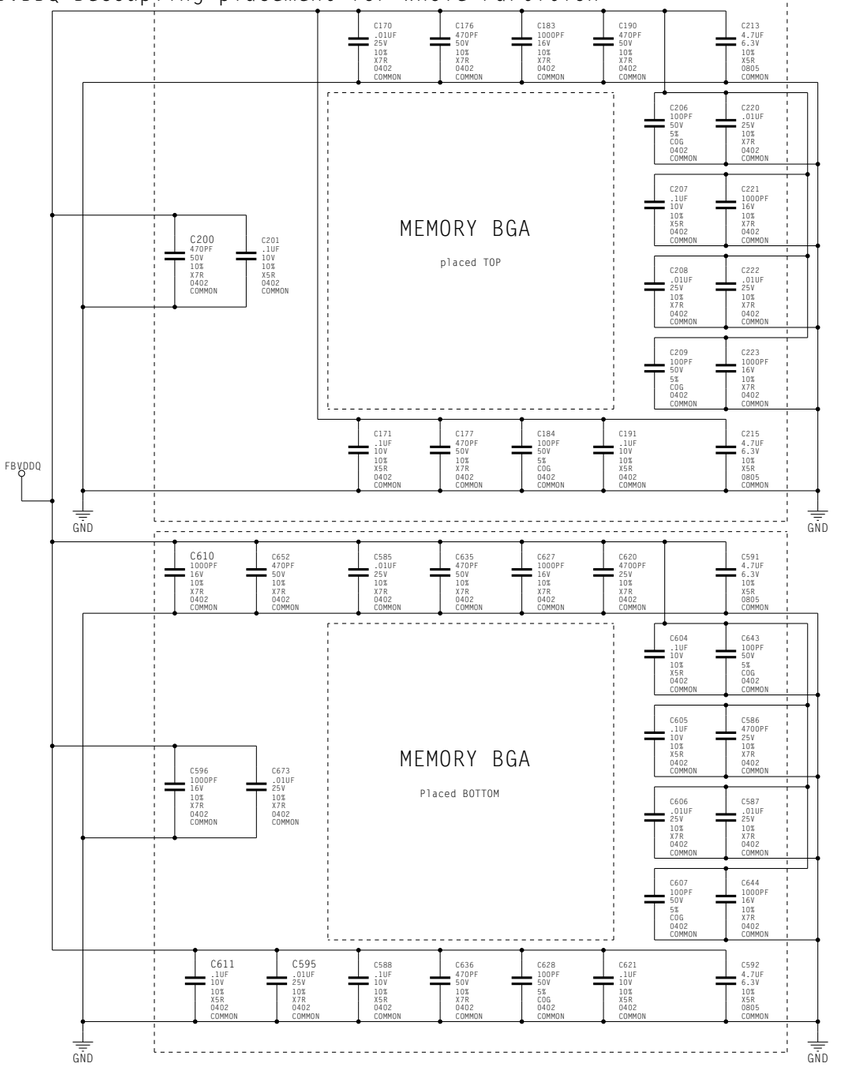
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Memory: FB_C & FB_D Partitions

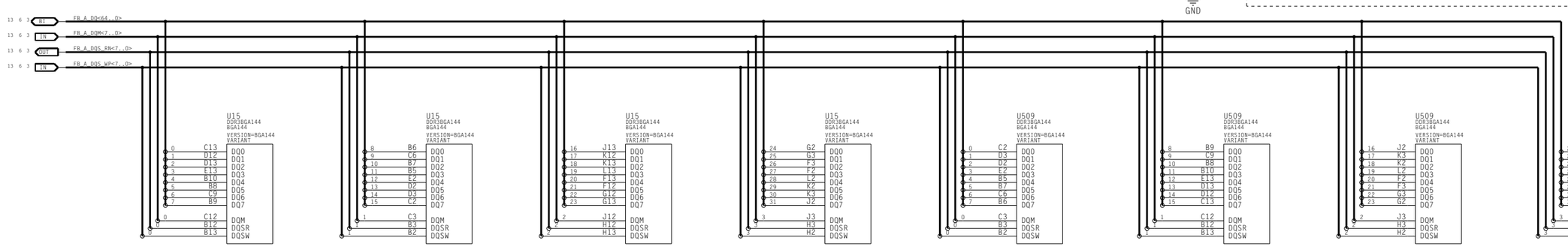
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	4 OF 31
NAME	TSchirmer	DATE	4-NOV-2004





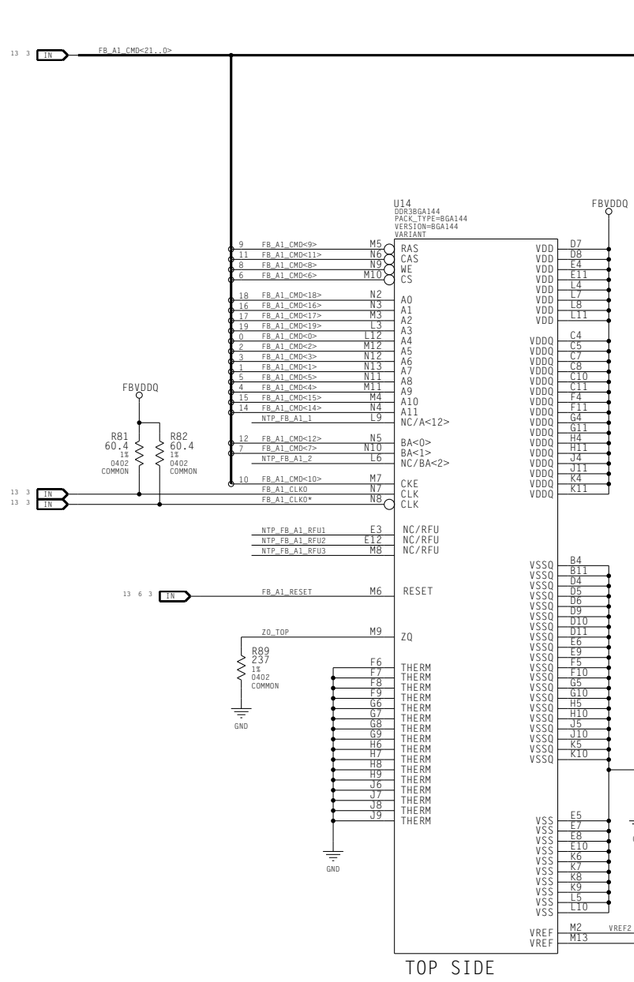


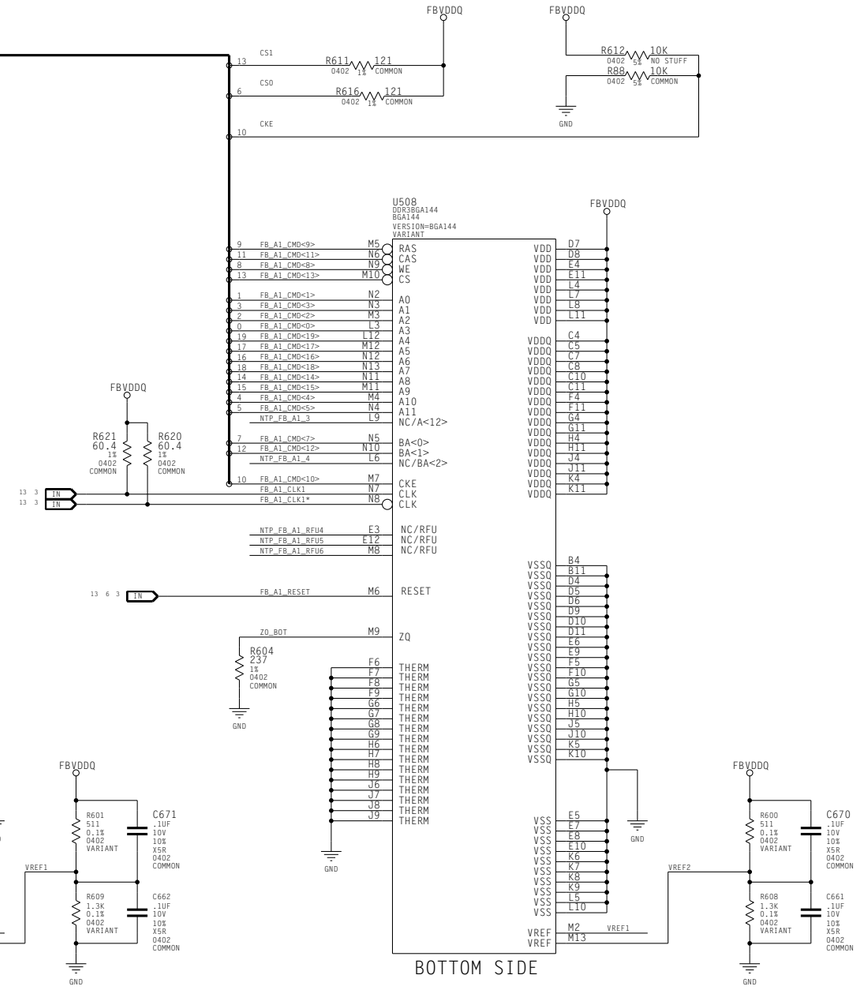


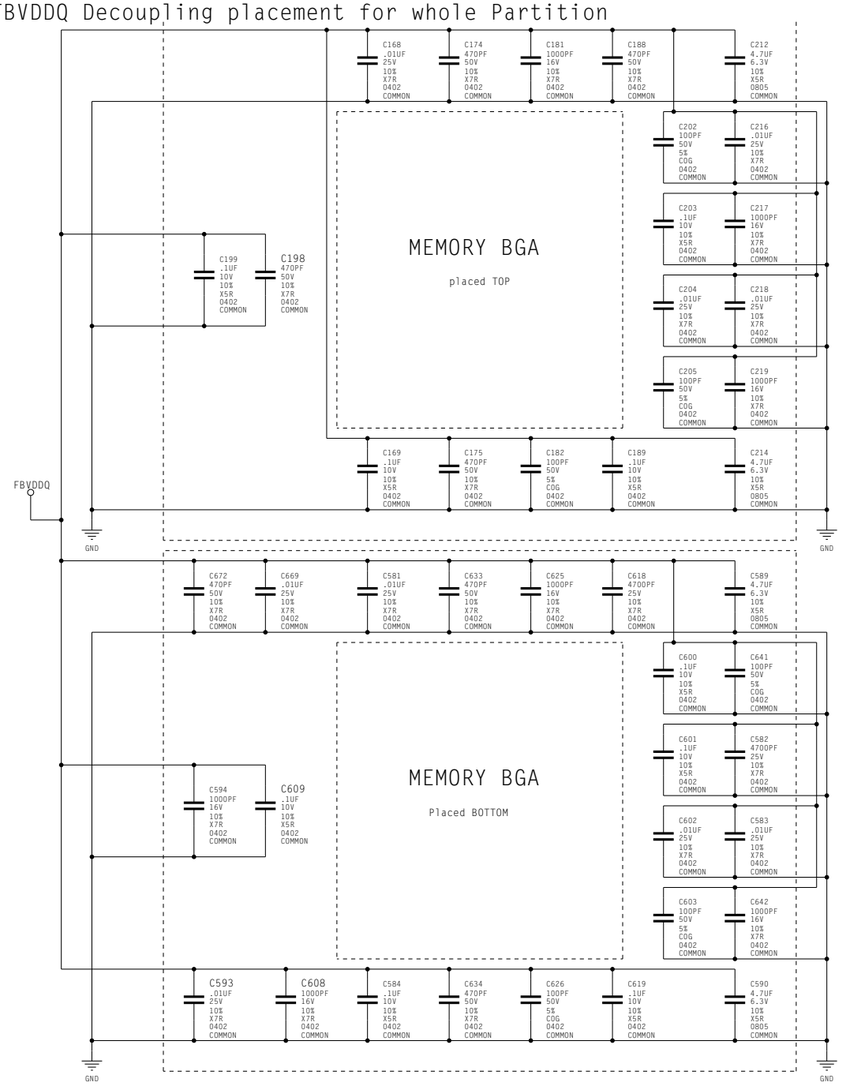
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Memory: FB_A0

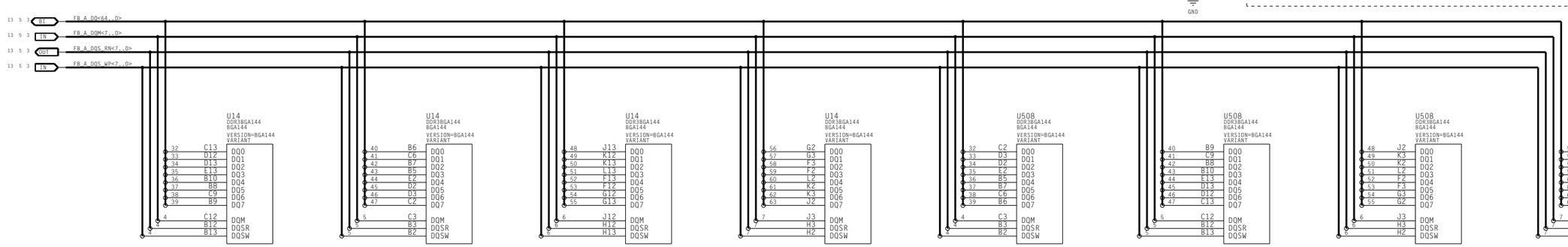
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	5 OF 31
NAME	TSchirmer	DATE	4-NOV-2004





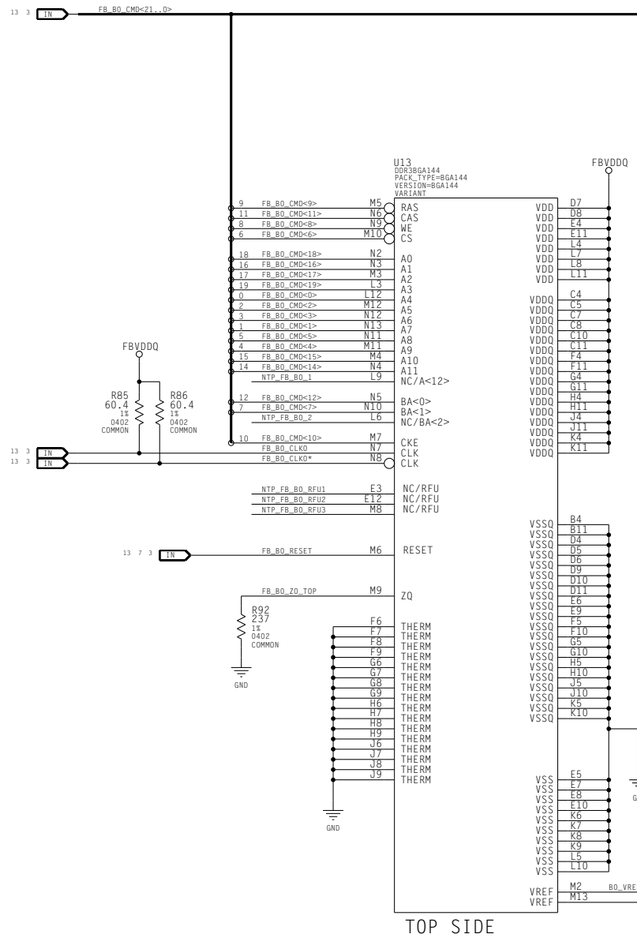


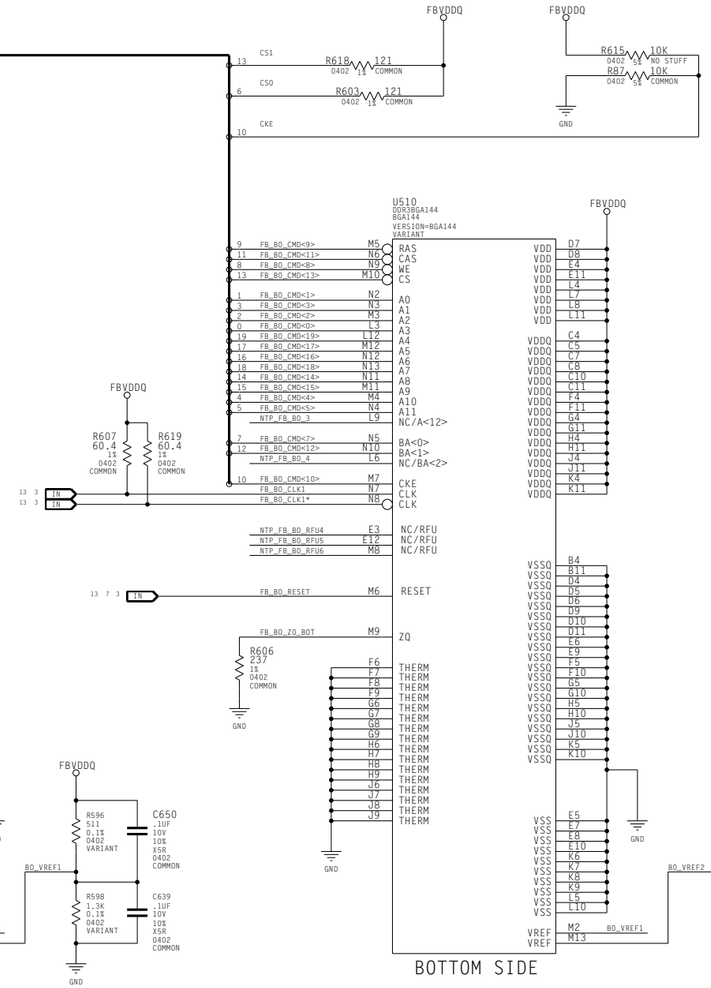


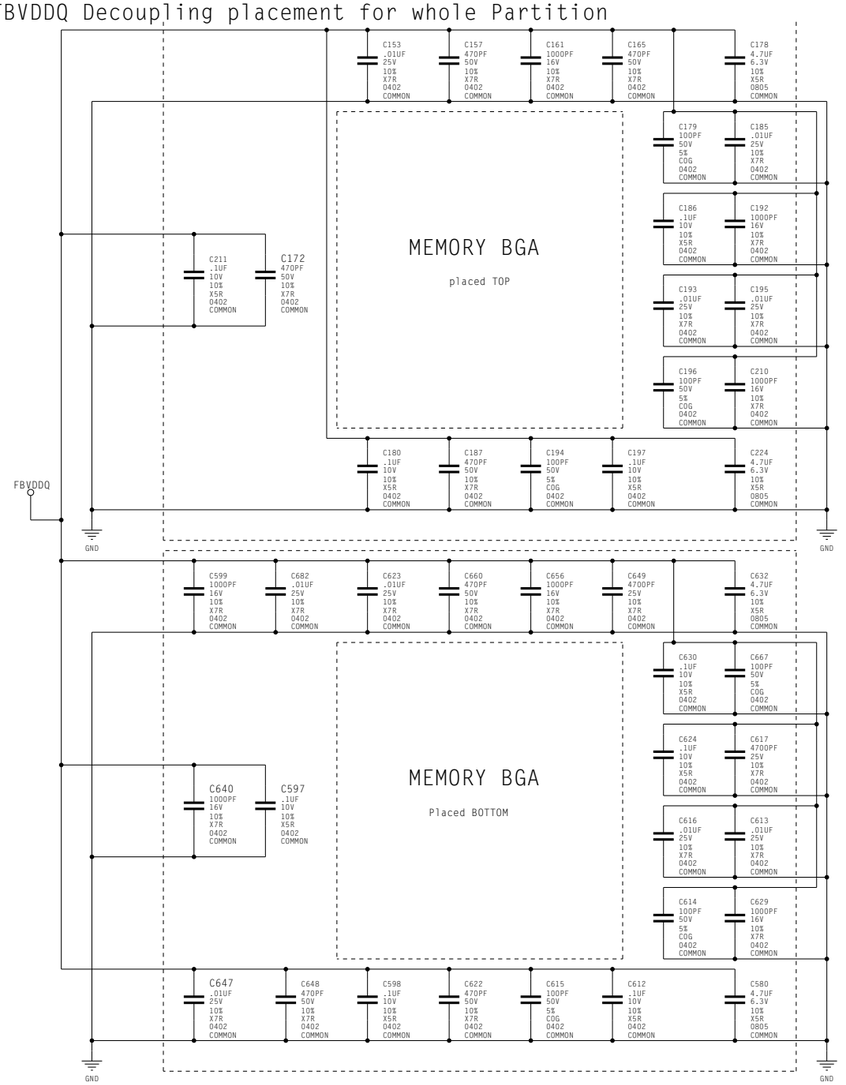
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Memory: FB_A1

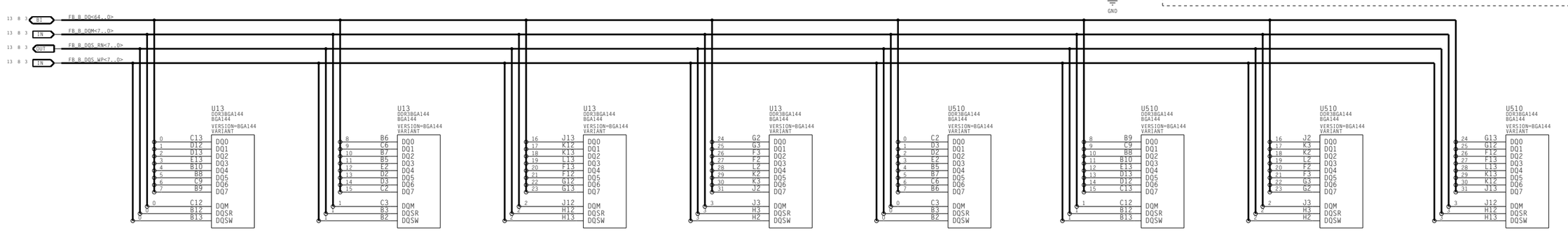
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	6 OF 31
NAME	TSchirmer	DATE	4-NOV-2004





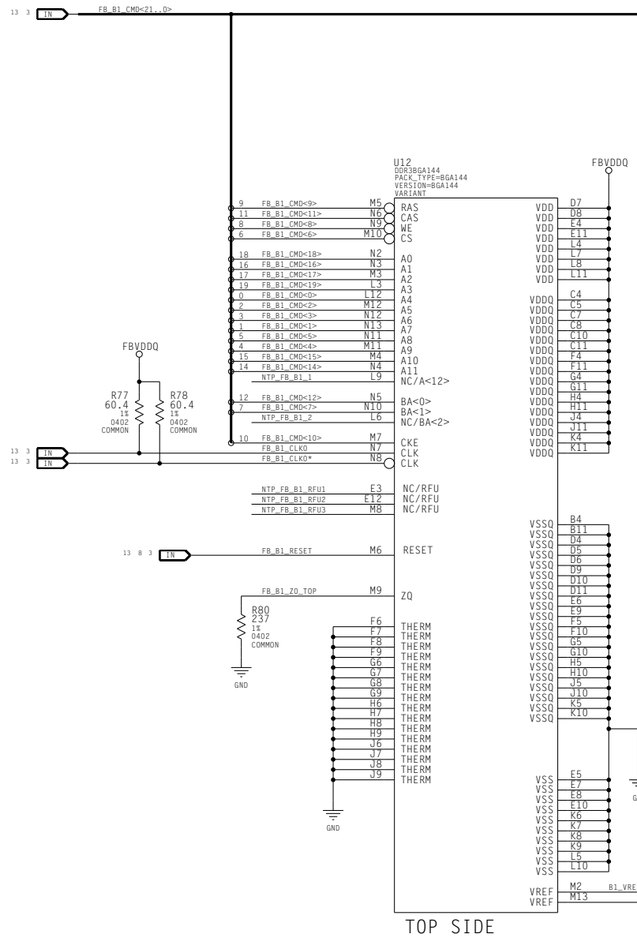


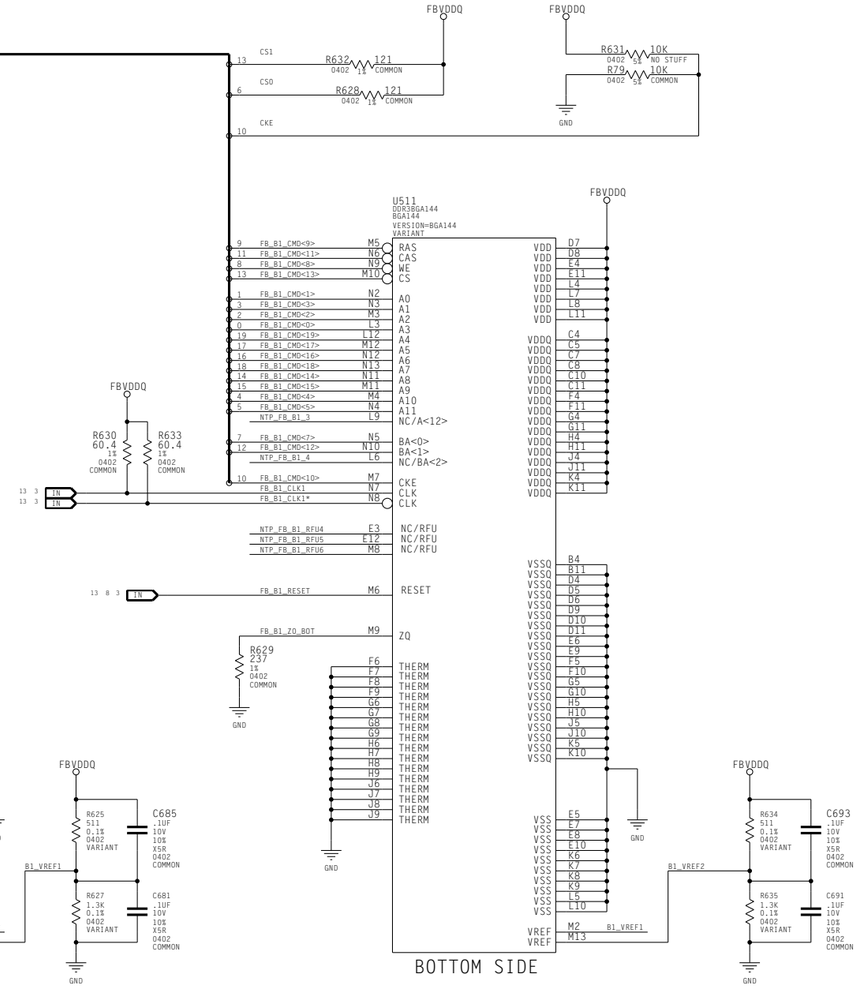


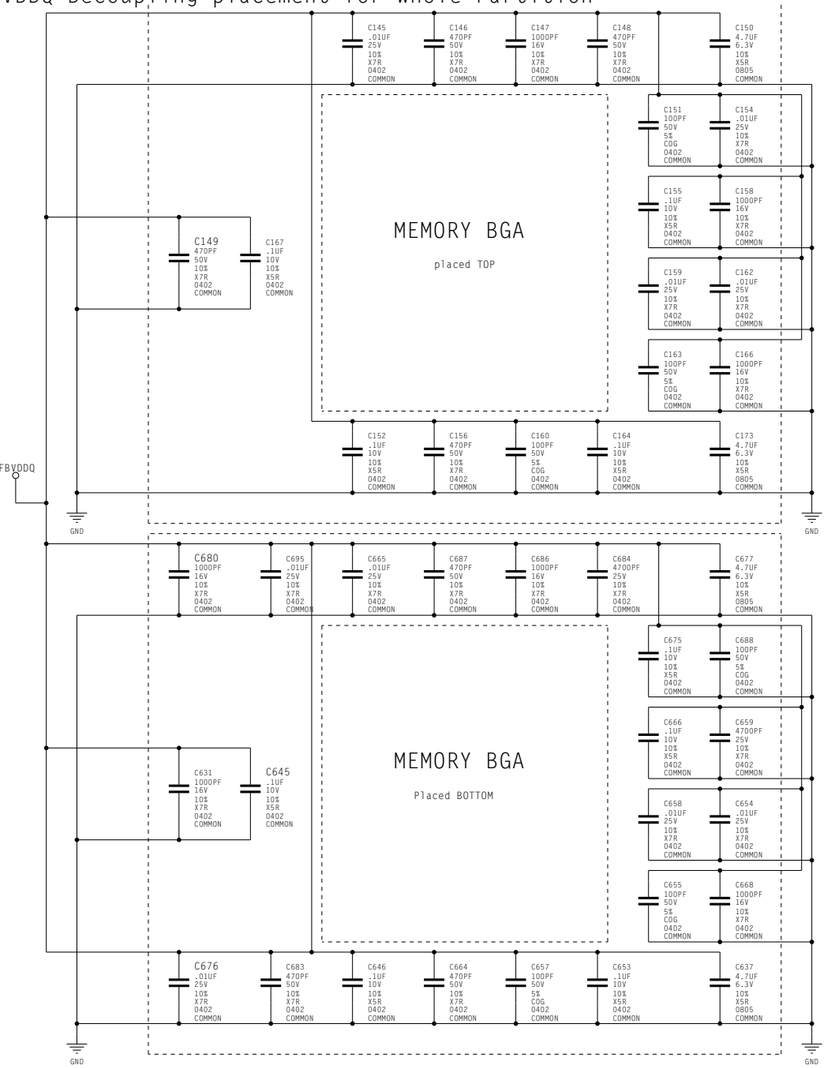
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Memory: FB_B0

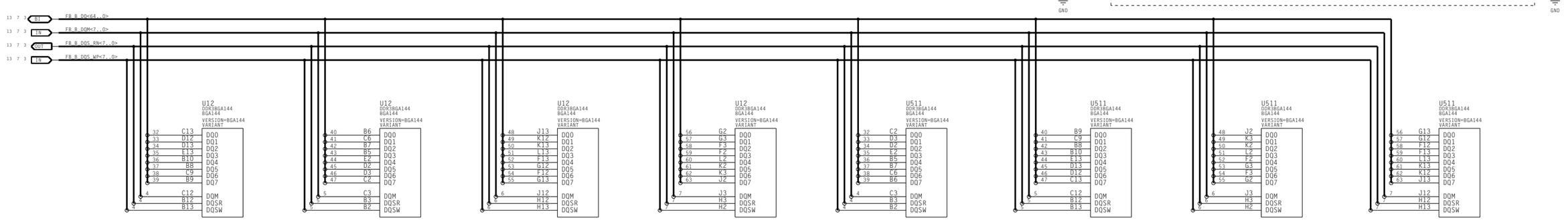
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	7 OF 31
NAME	TSchirmer	DATE	4-NOV-2004





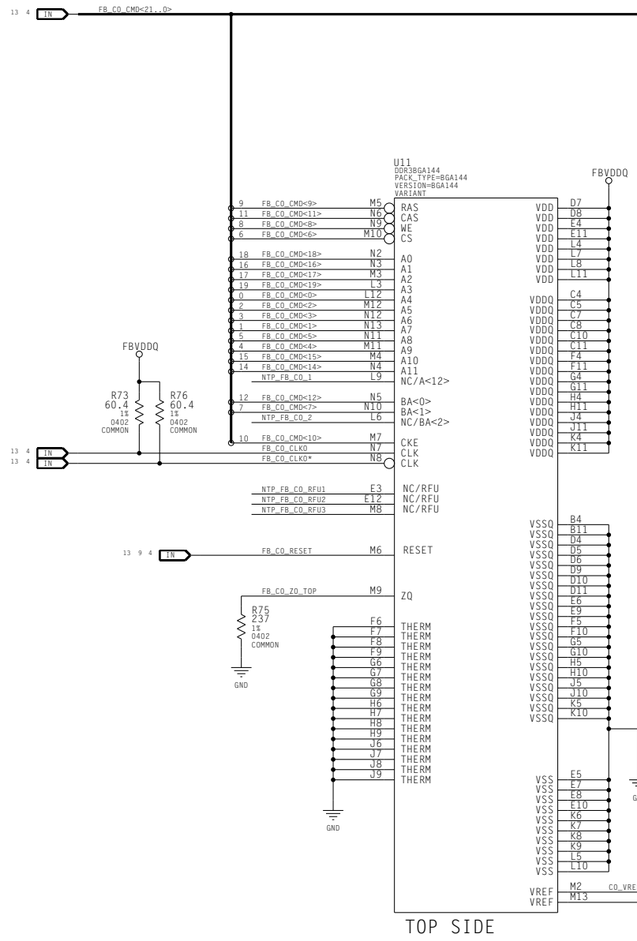


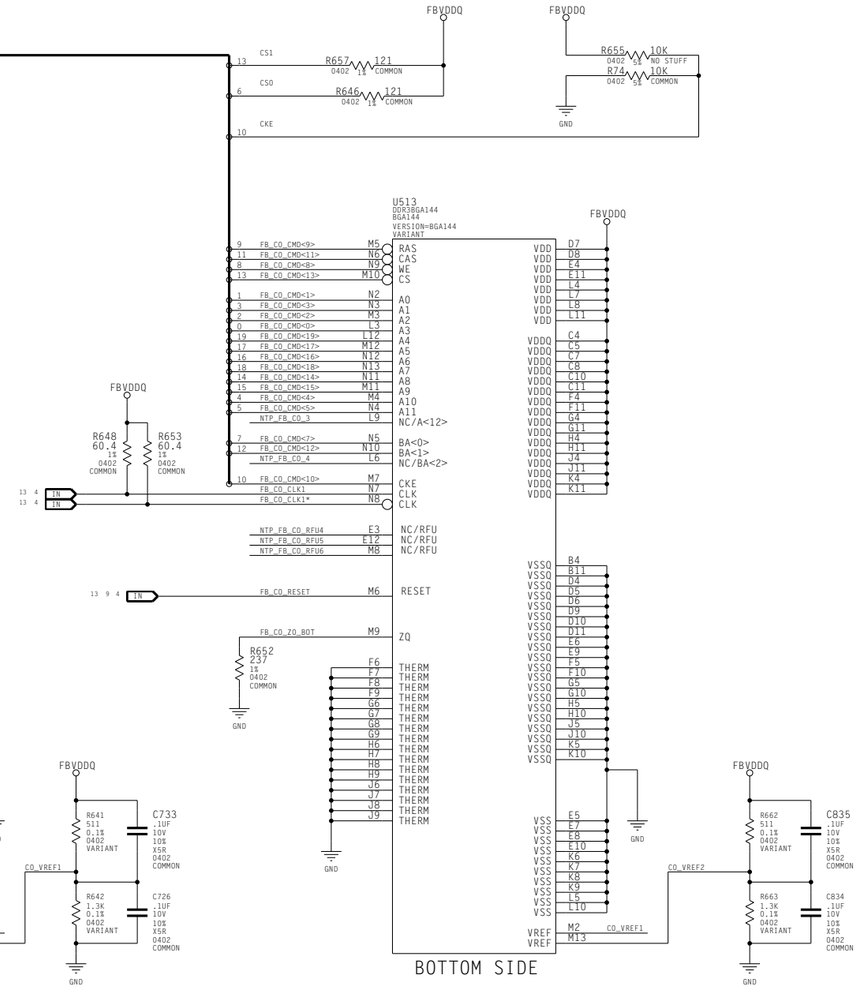


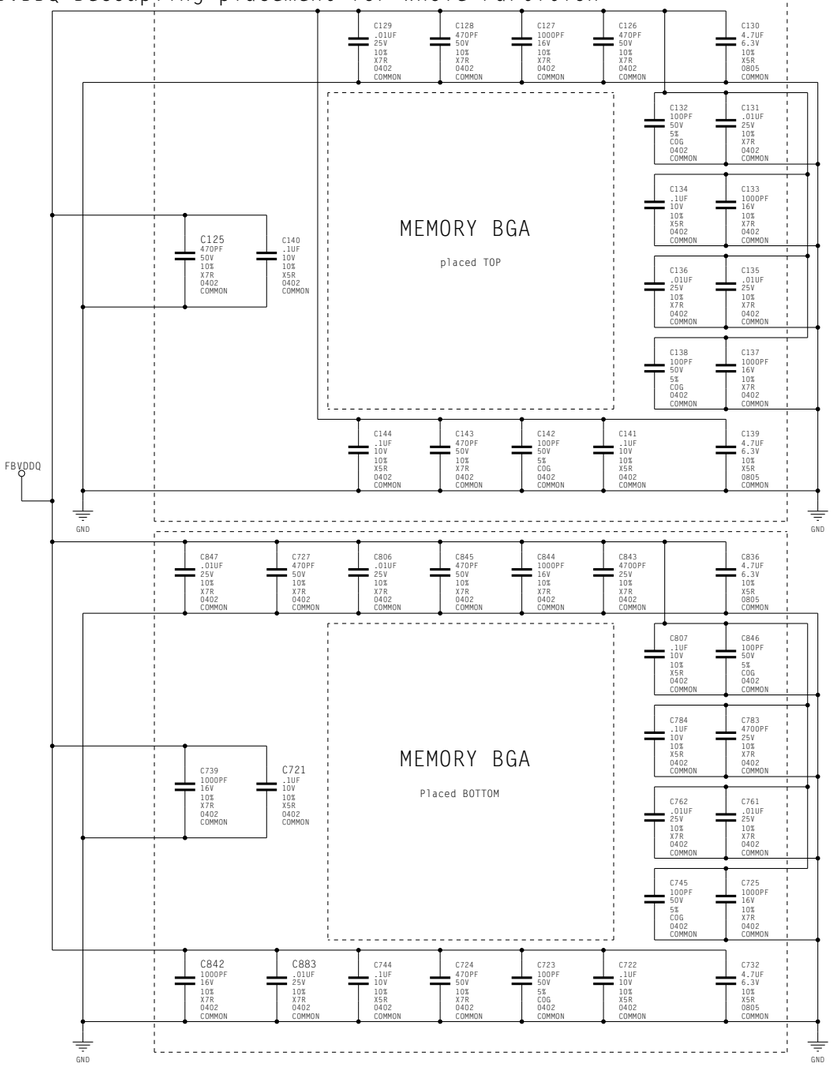
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Memory: FB_B1

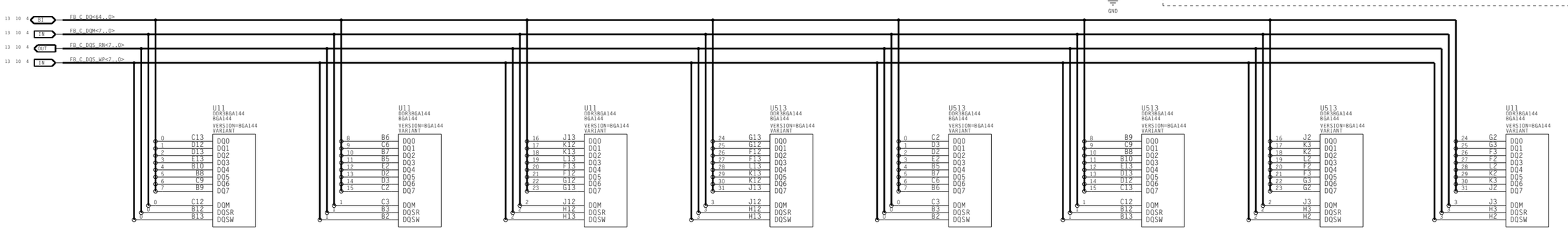
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	8 OF 31
NAME	TSchirmer	DATE	4-NOV-2004





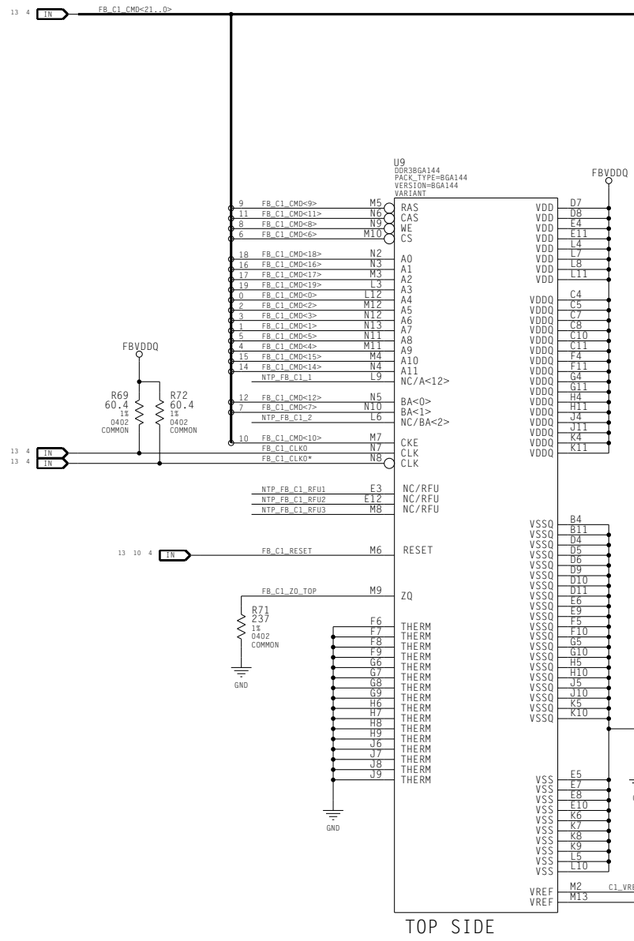


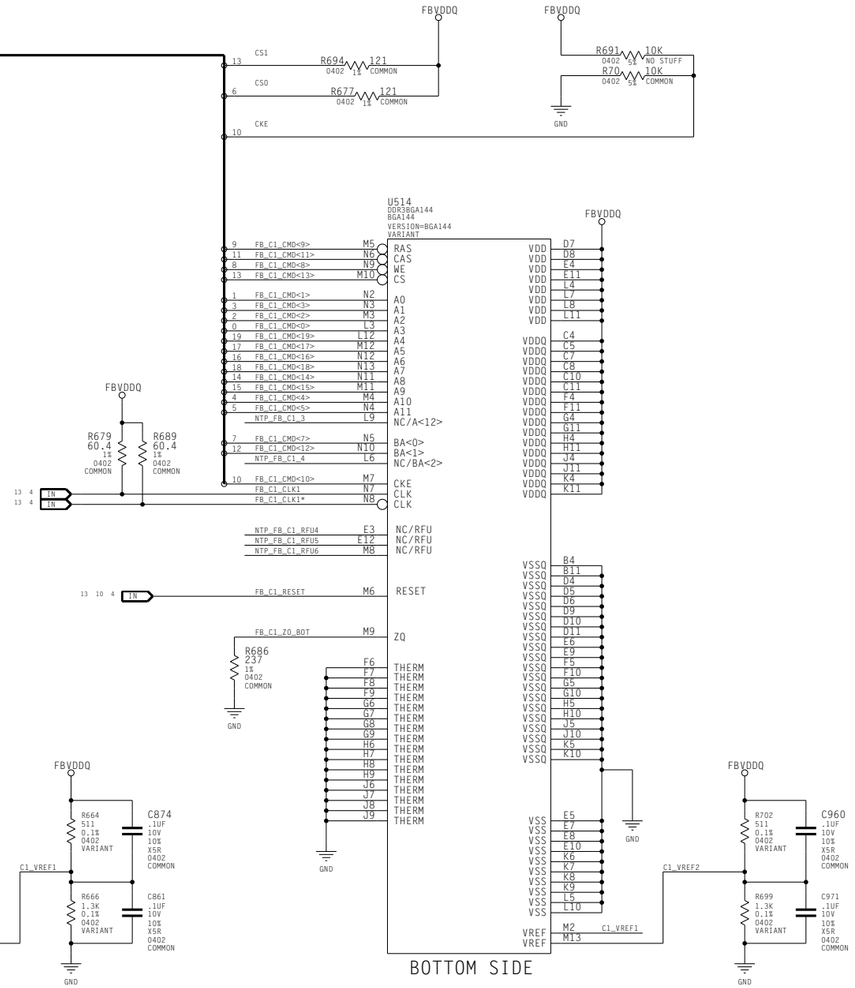


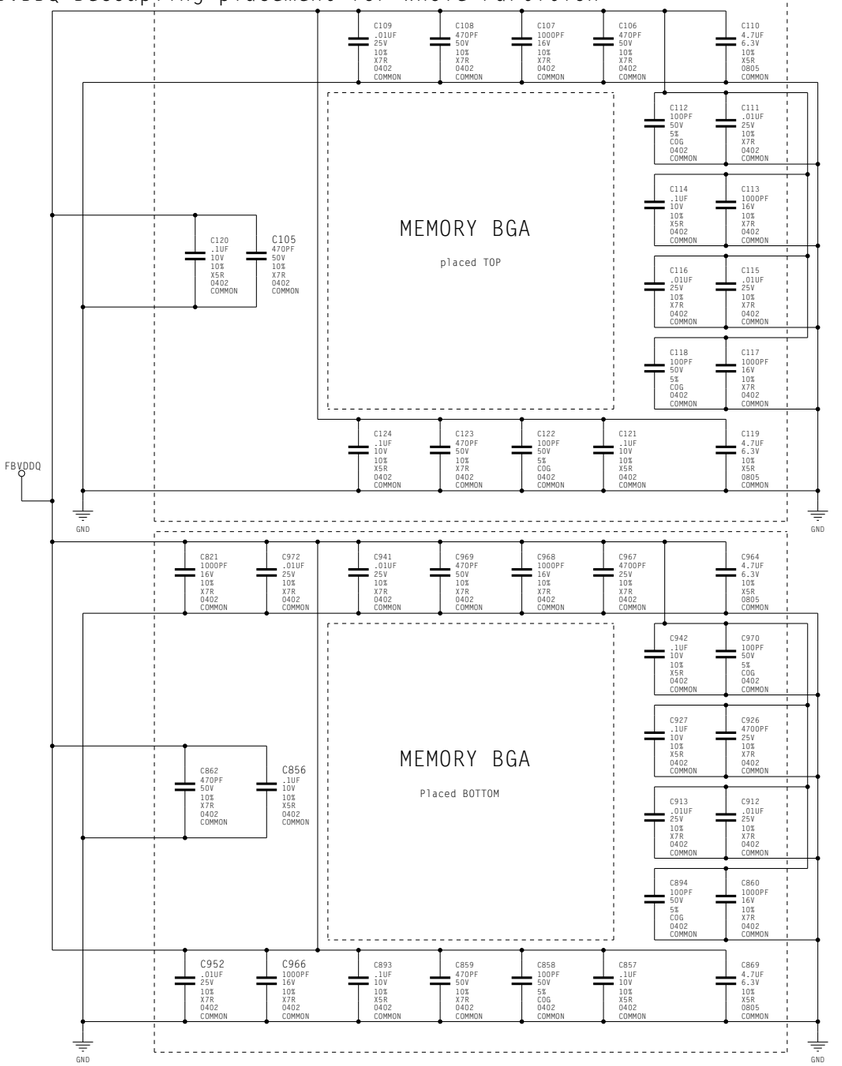
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Memory: FB_C0

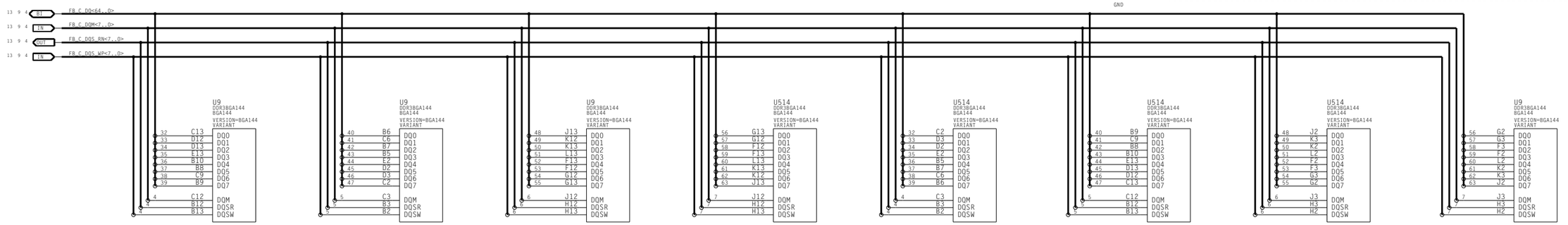
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	9 OF 31
NAME	TSchirmer	DATE	4-NOV-2004





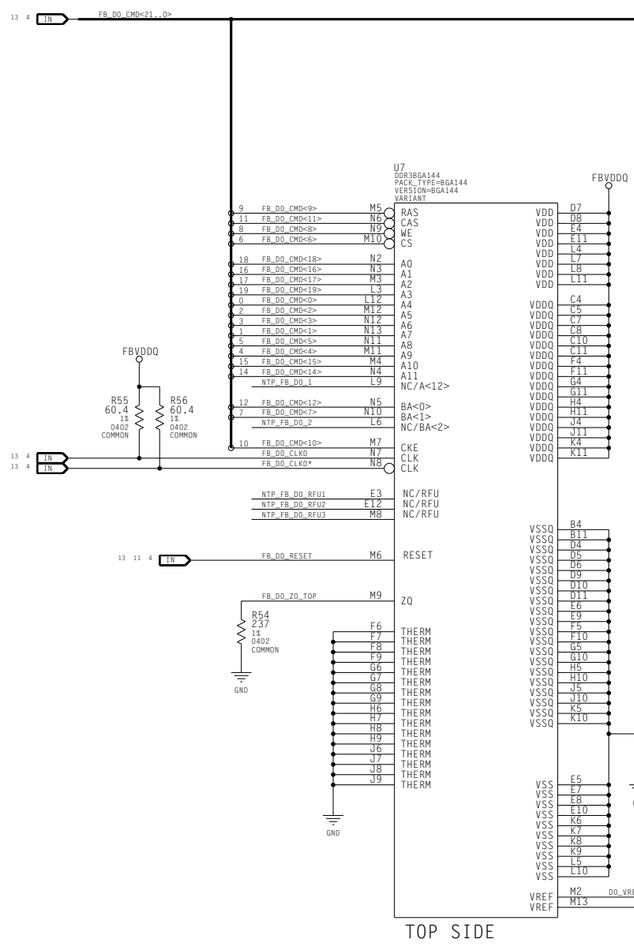


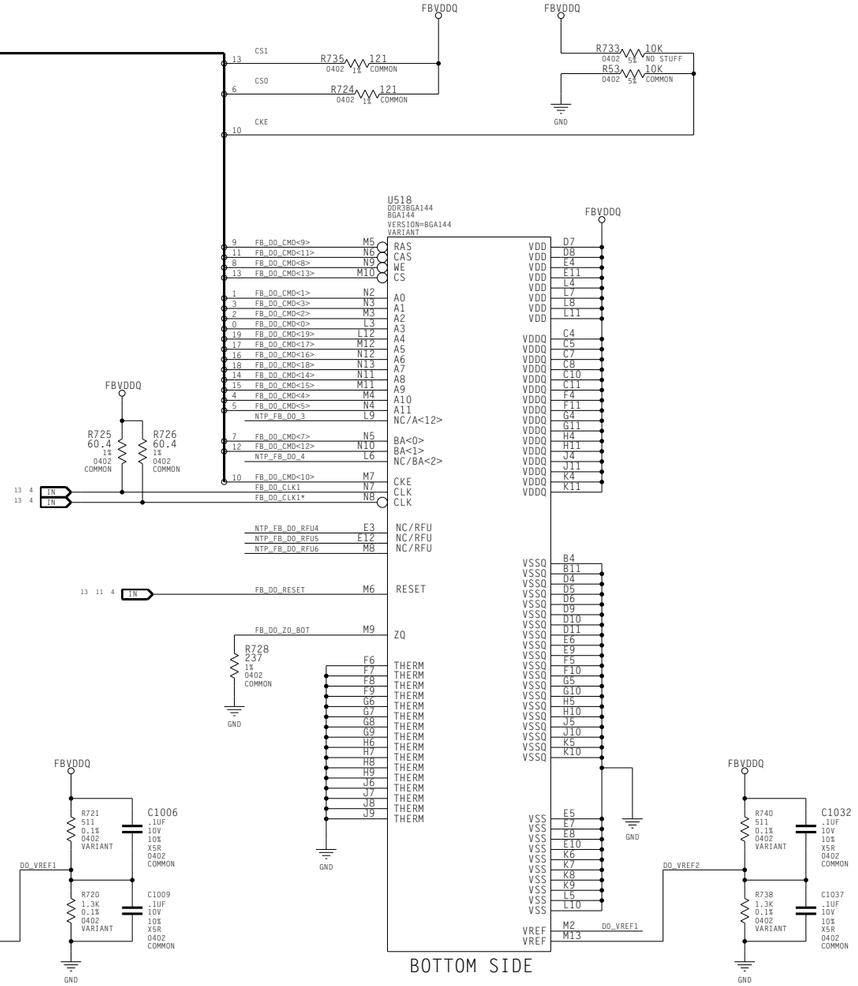


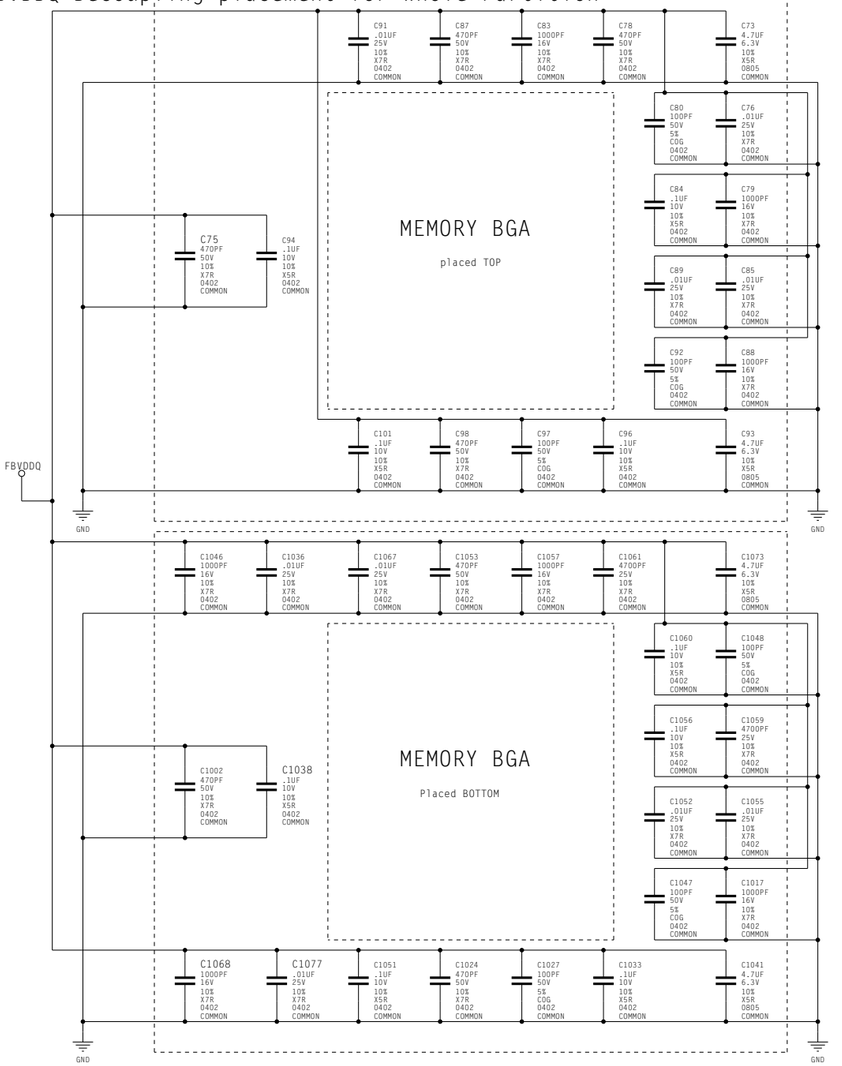
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Memory: FB_C1

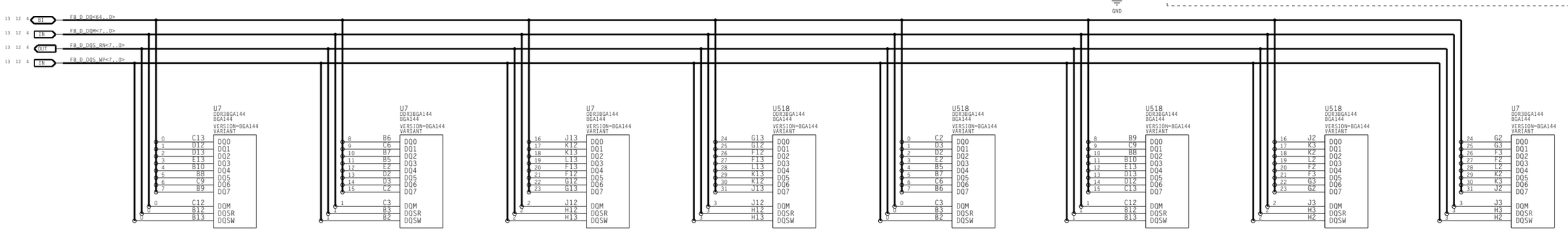
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	10 OF 31
NAME	TSchirmer	DATE	4-NOV-2004





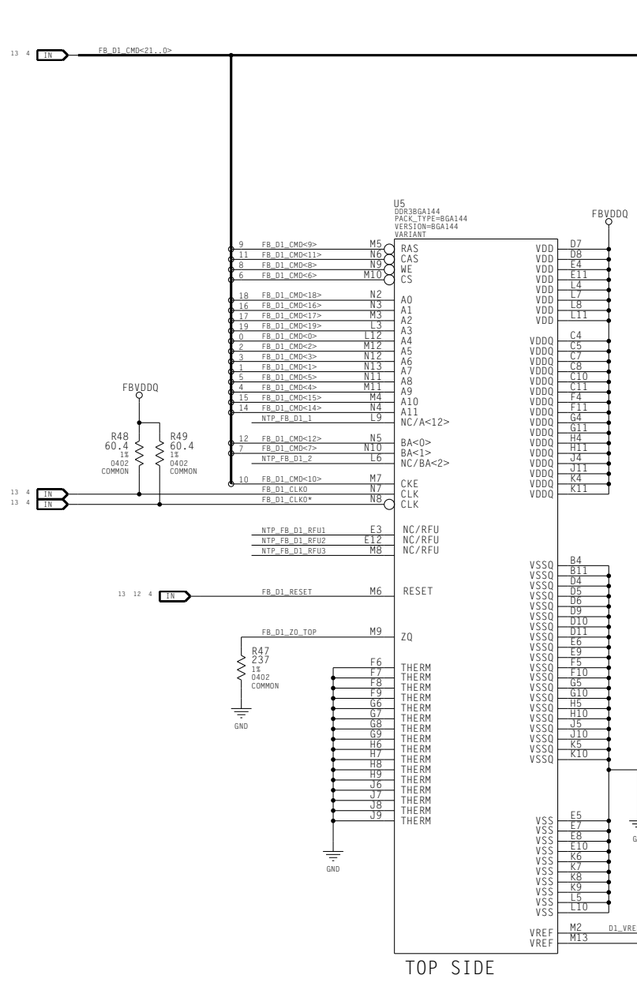


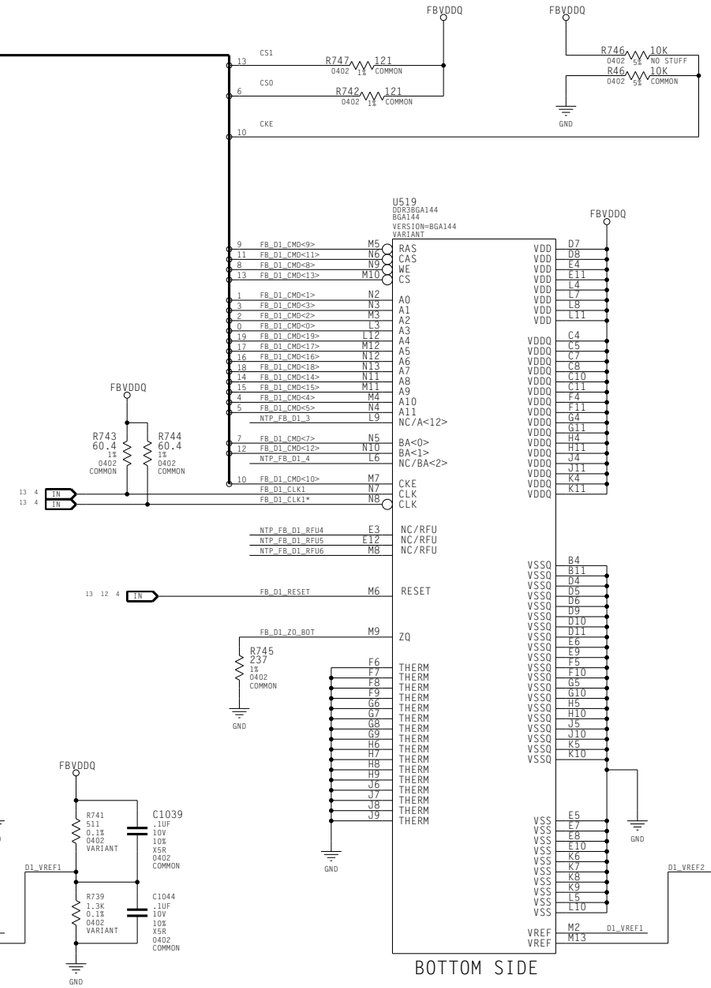


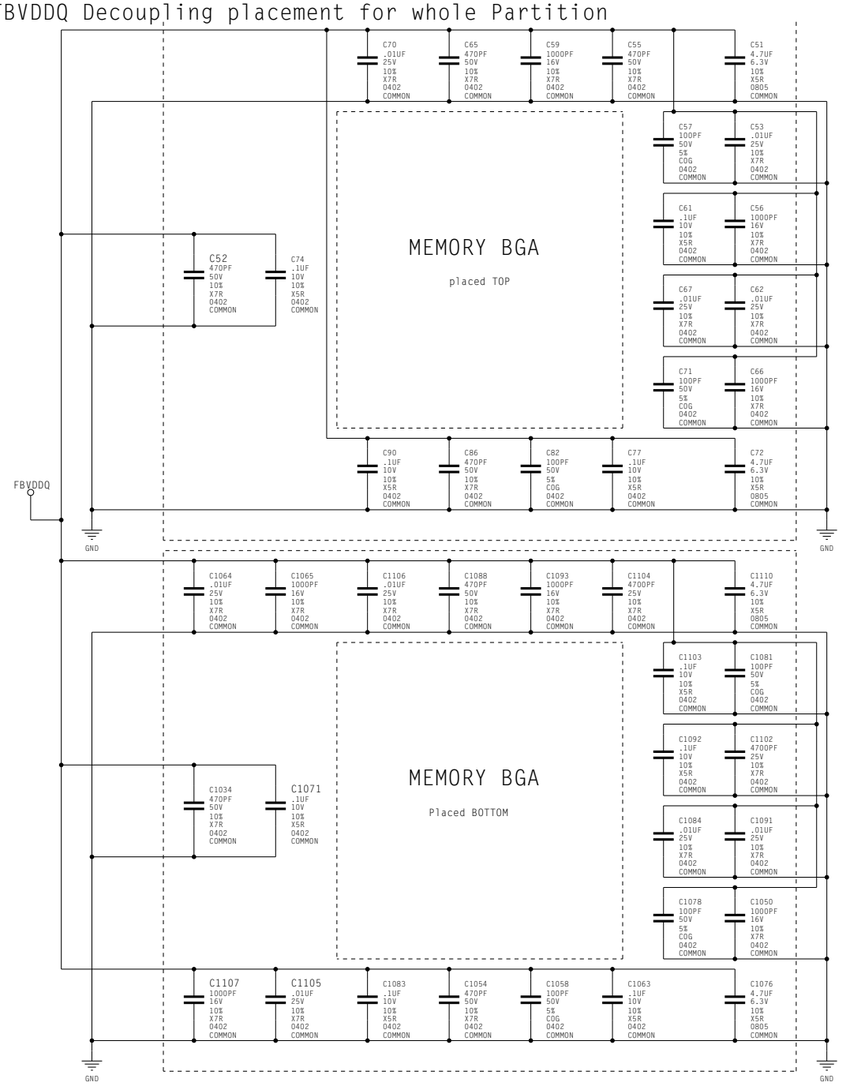
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Memory: FB_DO

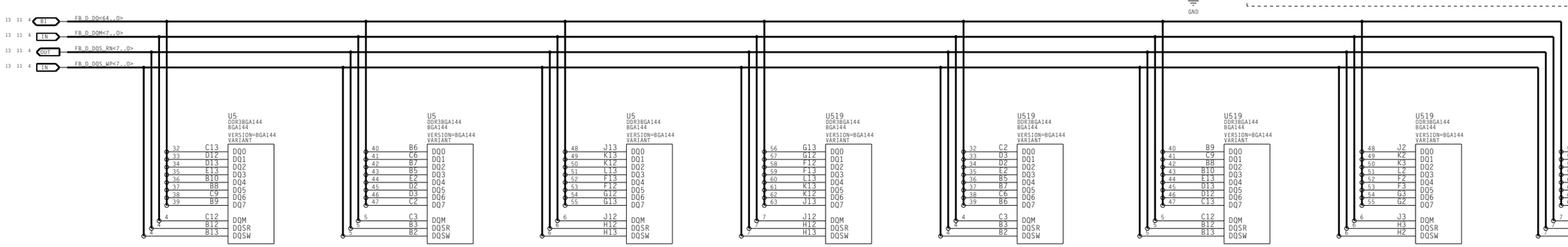
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	11 OF 31
NAME	TSchirmer	DATE	4-NOV-2004









ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Memory: FB_D1

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	12 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

Memory FBA FBB

NET Name	Diffpair	Spacing	MIN_LINE_WIDTH
FB_A0_CLK0	FBA0CLK0	80_OHM_DIFF	5MIL
FB_A0_CLK0*	FBA0CLK0	80_OHM_DIFF	5MIL
FB_A0_CLK1	FBA0CLK1	80_OHM_DIFF	5MIL
FB_A0_CLK1*	FBA0CLK1	80_OHM_DIFF	5MIL
FB_A1_CLK0	FBA1CLK0	80_OHM_DIFF	5MIL
FB_A1_CLK0*	FBA1CLK0	80_OHM_DIFF	5MIL
FB_A1_CLK1	FBA1CLK1	80_OHM_DIFF	5MIL
FB_A1_CLK1*	FBA1CLK1	80_OHM_DIFF	5MIL
FB_B0_CLK0	FBB0CLK0	80_OHM_DIFF	5MIL
FB_B0_CLK0*	FBB0CLK0	80_OHM_DIFF	5MIL
FB_B0_CLK1	FBB0CLK1	80_OHM_DIFF	5MIL
FB_B0_CLK1*	FBB0CLK1	80_OHM_DIFF	5MIL
FB_B1_CLK0	FBB1CLK0	80_OHM_DIFF	5MIL
FB_B1_CLK0*	FBB1CLK0	80_OHM_DIFF	5MIL
FB_B1_CLK1	FBB1CLK1	80_OHM_DIFF	5MIL
FB_B1_CLK1*	FBB1CLK1	80_OHM_DIFF	5MIL

NET Name	Spacing
FB_A_DQ<63..0>	10MIL
FB_B_DQ<63..0>	10MIL
FB_A_DQM<7..0>	10MIL
FB_A_DQS_RN<7..0>	10MIL
FB_A_DQS_WP<7..0>	10MIL
FB_B_DQM<7..0>	10MIL
FB_B_DQS_RN<7..0>	10MIL
FB_B_DQS_WP<7..0>	10MIL
FB_A0_CMD<19..0>	15MIL
FB_A1_CMD<19..0>	15MIL
FB_B0_CMD<19..0>	15MIL
FB_B1_CMD<19..0>	15MIL
FB_A0_RESET	10MIL
FB_A1_RESET	10MIL
FB_B0_RESET	10MIL
FB_B1_RESET	10MIL

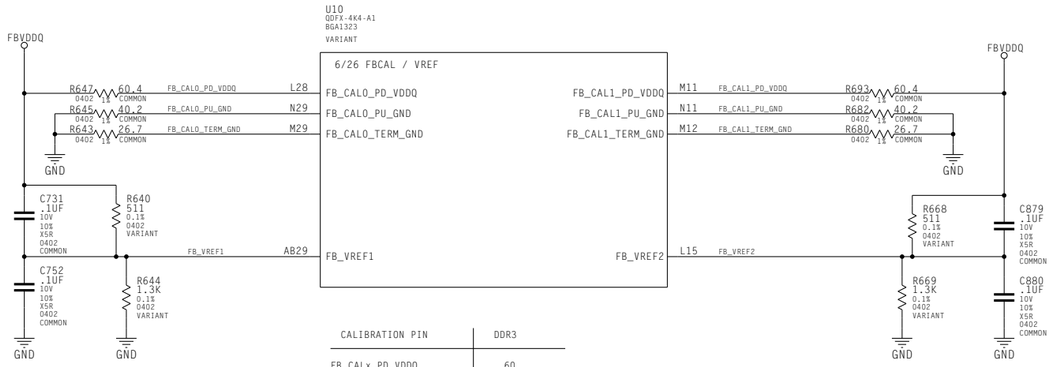
NET Name	MIN_LINE_WIDTH	VOLTAGE
FB_A_AVDD	12MIL	3.3V
FB_A_PLLVDD	12MIL	3.3V
FB_B_AVDD	12MIL	3.3V
FB_B_PLLVDD	12MIL	3.3V
FB_A0_ZO	12MIL	0.9V
FB_A1_ZO	12MIL	0.9V
FB_B0_ZO	12MIL	0.9V
FB_B1_ZO	12MIL	0.9V
FB_A0_VREF1	12MIL	0.9V
FB_A0_VREF2	12MIL	0.9V
FB_A1_VREF1	12MIL	0.9V
FB_A1_VREF2	12MIL	0.9V
FB_B0_VREF1	12MIL	0.9V
FB_B0_VREF2	12MIL	0.9V
FB_B1_VREF1	12MIL	0.9V
FB_B1_VREF2	12MIL	0.9V

Memory FBC FBD

NET Name	Diffpair	Spacing	MIN_LINE_WIDTH
FB_C0_CLK0	FBC0CLK0	80_OHM_DIFF	5MIL
FB_C0_CLK0*	FBC0CLK0	80_OHM_DIFF	5MIL
FB_C0_CLK1	FBC0CLK1	80_OHM_DIFF	5MIL
FB_C0_CLK1*	FBC0CLK1	80_OHM_DIFF	5MIL
FB_C1_CLK0	FBC1CLK0	80_OHM_DIFF	5MIL
FB_C1_CLK0*	FBC1CLK0	80_OHM_DIFF	5MIL
FB_C1_CLK1	FBC1CLK1	80_OHM_DIFF	5MIL
FB_C1_CLK1*	FBC1CLK1	80_OHM_DIFF	5MIL
FB_D0_CLK0	FBD0CLK0	80_OHM_DIFF	5MIL
FB_D0_CLK0*	FBD0CLK0	80_OHM_DIFF	5MIL
FB_D0_CLK1	FBD0CLK1	80_OHM_DIFF	5MIL
FB_D0_CLK1*	FBD0CLK1	80_OHM_DIFF	5MIL
FB_D1_CLK0	FBD1CLK0	80_OHM_DIFF	5MIL
FB_D1_CLK0*	FBD1CLK0	80_OHM_DIFF	5MIL
FB_D1_CLK1	FBD1CLK1	80_OHM_DIFF	5MIL
FB_D1_CLK1*	FBD1CLK1	80_OHM_DIFF	5MIL

NET Name	Spacing
FB_C_DQ<63..0>	10MIL
FB_D_DQ<63..0>	10MIL
FB_C_DQM<7..0>	10MIL
FB_C_DQS_RN<7..0>	10MIL
FB_C_DQS_WP<7..0>	10MIL
FB_D_DQM<7..0>	10MIL
FB_D_DQS_RN<7..0>	10MIL
FB_D_DQS_WP<7..0>	10MIL
FB_C0_CMD<19..0>	15MIL
FB_C1_CMD<19..0>	15MIL
FB_D0_CMD<19..0>	15MIL
FB_D1_CMD<19..0>	15MIL
FB_C0_RESET	10MIL
FB_C1_RESET	10MIL
FB_D0_RESET	10MIL
FB_D1_RESET	10MIL

NET Name	MIN_LINE_WIDTH	VOLTAGE
FB_C_AVDD	12MIL	3.3V
FB_C_PLLVDD	12MIL	3.3V
FB_D_AVDD	12MIL	3.3V
FB_D_PLLVDD	12MIL	3.3V
FB_C0_ZO	12MIL	0.9V
FB_C1_ZO	12MIL	0.9V
FB_D0_ZO	12MIL	0.9V
FB_D1_ZO	12MIL	0.9V
FB_C0_VREF1	12MIL	0.9V
FB_C0_VREF2	12MIL	0.9V
FB_C1_VREF1	12MIL	0.9V
FB_C1_VREF2	12MIL	0.9V
FB_D0_VREF1	12MIL	0.9V
FB_D0_VREF2	12MIL	0.9V
FB_D1_VREF1	12MIL	0.9V
FB_D1_VREF2	12MIL	0.9V

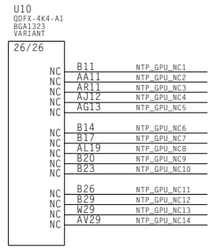


CALIBRATION PIN	DDR3
FB_CALx_PD_VDDQ	60
FB_CALx_PU_GND	40
FB_CALx_TERM_GND	26.7
VREF RATIO	0.7 FBVDDQ

GPU VREF RATIO DDR3 RECOMMEND 511/1.30k = 0.718 RATIO

MEM VREF RATIO DDR3 RECOMMEND 511/1.30k = 0.718 RATIO

DEFAULT BASE SCHEMATICS ARE SETUP FOR DDR3



NET Name	Spacing
FB_CAL0_PD_VDDQ	20MIL_G2G_25MIL
FB_CAL0_PU_GND	20MIL_G2G_25MIL
FB_CAL0_TERM_GND	20MIL_G2G_25MIL
FB_CAL1_PD_VDDQ	20MIL_G2G_25MIL
FB_CAL1_PU_GND	20MIL_G2G_25MIL
FB_CAL1_TERM_GND	20MIL_G2G_25MIL

NET Name	MIN_LINE_WIDTH	VOLTAGE
FB_VREF1	12MIL	3.3V
FB_VREF2	12MIL	3.3V

ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Memory Signal Constraints, FB-CAL

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	13 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

MEC501
PH_4_40X3/16_SCREW
STD
COMMON

MEC1
HEX_JACK_SCREW
STD
COMMON

MEC2
HEX_JACK_SCREW
STD
COMMON

MEC3
HEX_JACK_SCREW
STD
COMMON

MEC4
HEX_JACK_SCREW
STD
COMMON

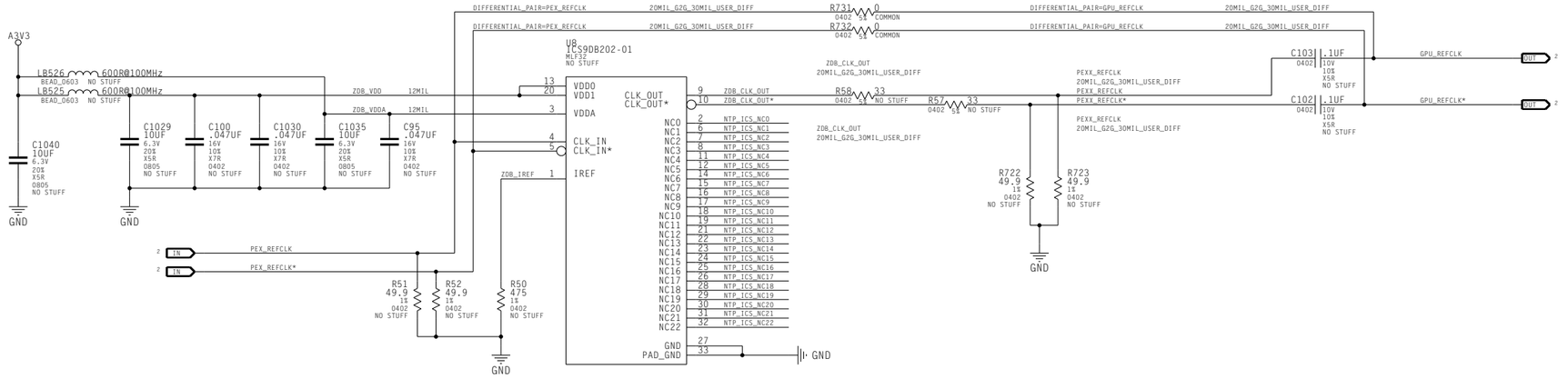
BKT1
DVI1152_DVI1552_MDIN49O_TEXT_1_2_DUAL_WIDE
ATX_2X_TOP
COMMON

1 GND

MECH. MOUNTING TOP

Symbols to be placed on PCB for Heatsink solution

HEATSINK_MEM_TOPSIDE_3670X1520
HEATSINK_MEM_BACKSIDE_3620X1340
HEATSINK_GPU_STAR2_BOT
HEATSINK_GPU_2_35X2_72_B
FAN_GPU_2_68X3_30
SKT_POGO_BGA_40MM_HS
PEX_EXTDR_CARD_BOT



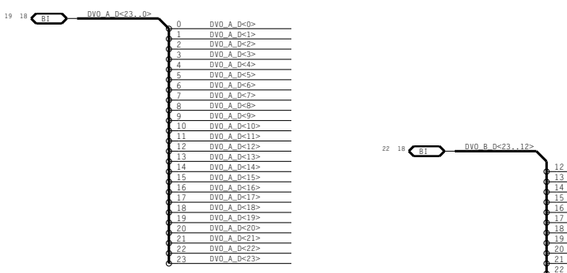
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	PEX Refclock Zero Delay Buffer, Mechanicals

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

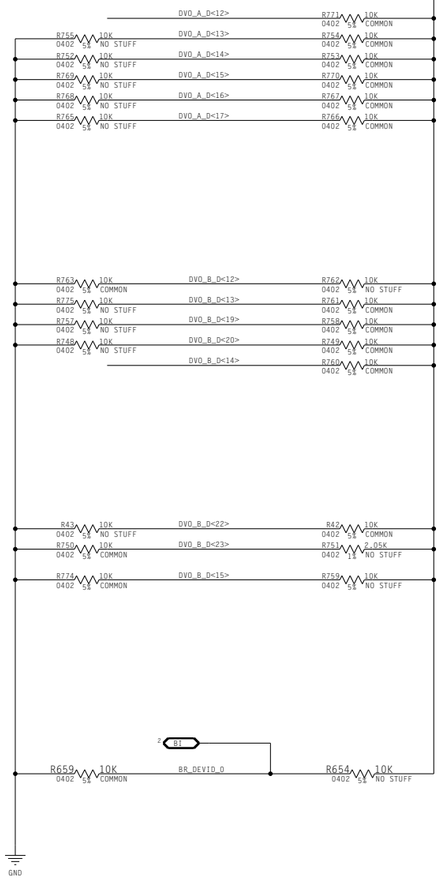
NV_PN	600-50214-0000-400		
ID	design	PAGE	14 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

Strapping Options

Assembly: BIOS



Unnecessary straps removed.. Is this ok?



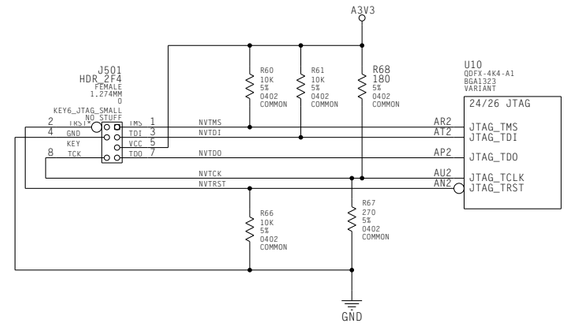
REG: NV_PEXTDEV_BOOT_0

Bit	Signal	VALUE_ID	VALUEs	
00:	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED	
			1 NORMAL	
01:	SUB_VENDOR	SUB_VENDOR	0 NO_BIOS	
			1 read from BIOS	
02:	RAM_CFG_0	RAM_CFG[3:0]	0000 RFU	1000 RFU
			0001 RFU	1001 RFU
03:	RAM_CFG_1		0010 RFU	1010 RFU
			0011 RFU	1011 RFU
04:	RAM_CFG_2		0100 RFU	1100 RFU
			0101 RFU	1101 RFU
05:	RAM_CFG_3		0110 RFU	1110 RFU
			0111 256MB GDDR3	1111 512MB GDDR3
06:	CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz	
			01 14.31818 Mhz	
22:	CRYSTAL_1		10 27.000 Mhz	
			11 unknown	
07:	TV_MODE_0	TV_MODE[1:0]	00 SECAM	
			01 NTSC	
08:	TV_MODE_1		10 PAL	
			11 CRT	
09:	AGPBxEnable	AGP_3D_8x	0 AGPBx enabled	
			1 AGPBx disabled	
10:	AGP_SBA	AGP_SBA[0]	0 SBA enabled	
			1 SBA disabled	
11:	AGP_FASTWR	AGP_FASTWR[0]	0 enabled	
			1 disabled	
12:	PCI_DEVID_0	PCI_DEVID[3:0]	0000 0x0 ... 1111 0xF	
13:	PCI_DEVID_1		0000 (0x0)	
20:	PCI_DEVID_2		1110 (0xE)	
21:	PCI_DEVID_3			
14:	BUS_TYPE	BUS_TYPE[0]	0 PCI	
			1 AGP	
15:	FP_IFACE	FP_IFACE[0]	0 24Bit	
			1 12Bit	
23:	FB_0	FB[1:0]	00 64M	
			01 128M	
24:	FB_1		10 256M	
			11 512M	
25:	BR	BR[0]	0 BRIDGE disabled	
			1 BRIDGE enabled	
26:	BR_128M	BR bits are ignored if BRIDGE is disabled		
27:	BR_AGP			
28:	BR_IO			
29:	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel	
			01 Serial_AT25F	
30:	ROM_TYPE_1		10 Serial_SST45VF	
			11 RFU	
16:	USER_0	STRAP_USER[3:0]	0000 (default)	
17:	USER_1			
18:	USER_2			
19:	USER_3			

BR02: DEVID_0

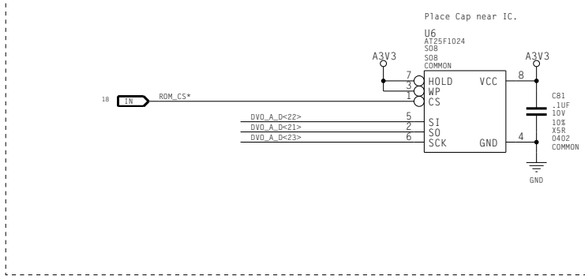
Signal	VALUEs
BR_DEVID_0	0 DEV_ID0 = 0
	1 DEV_ID0 = 1

JTAG

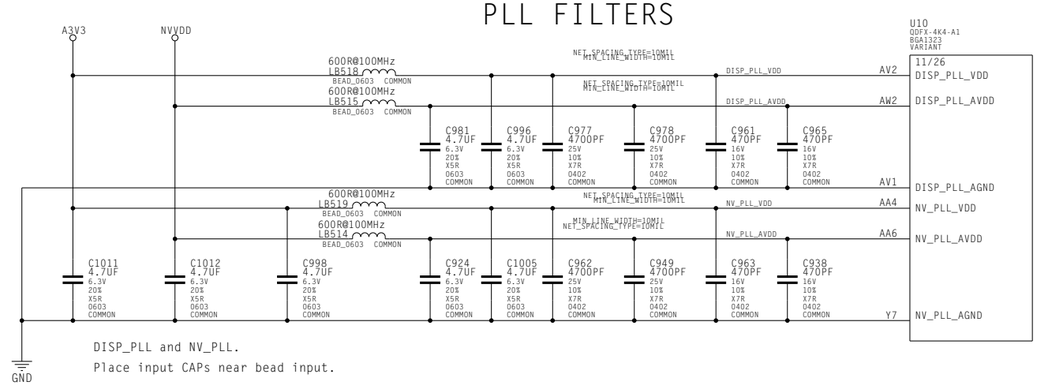


BIOS (serial)

Assembly: BIOS



PLL FILTERS



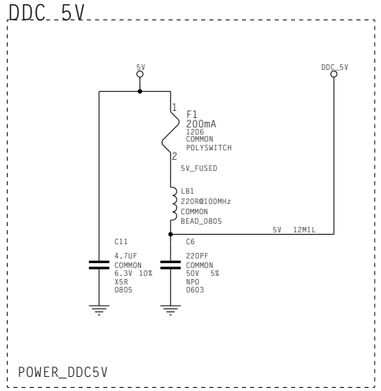
DISP_PLL and NV_PLL.
Place input CAPs near bead input.

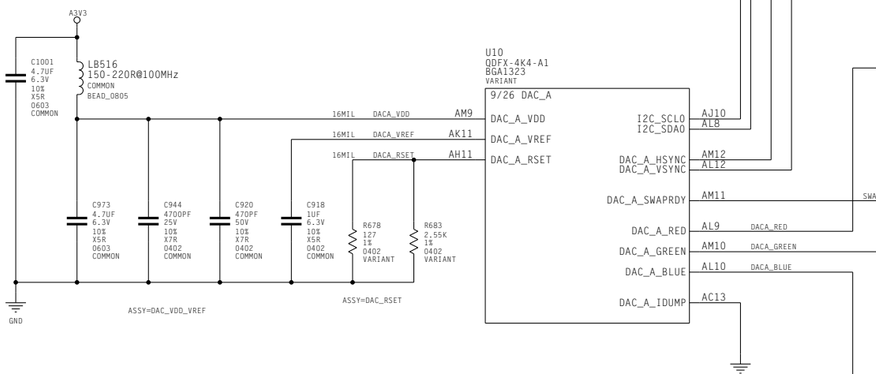
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	BIOS, Strapping options, JTAG and PLL supply

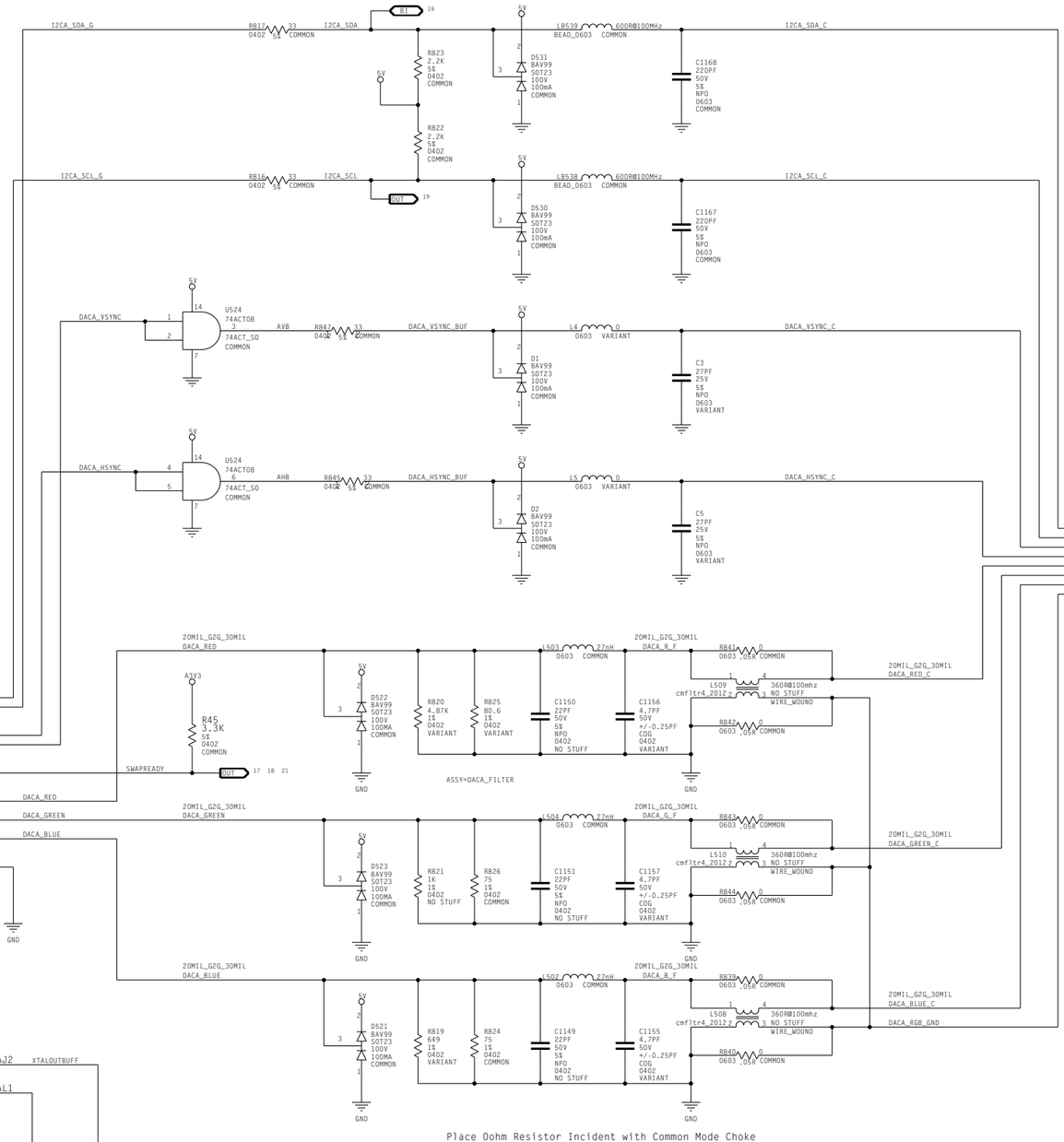
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	15 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

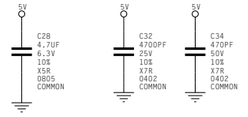
DDC_5V







Place 0ohm Resistor Incident with Common Mode Choke

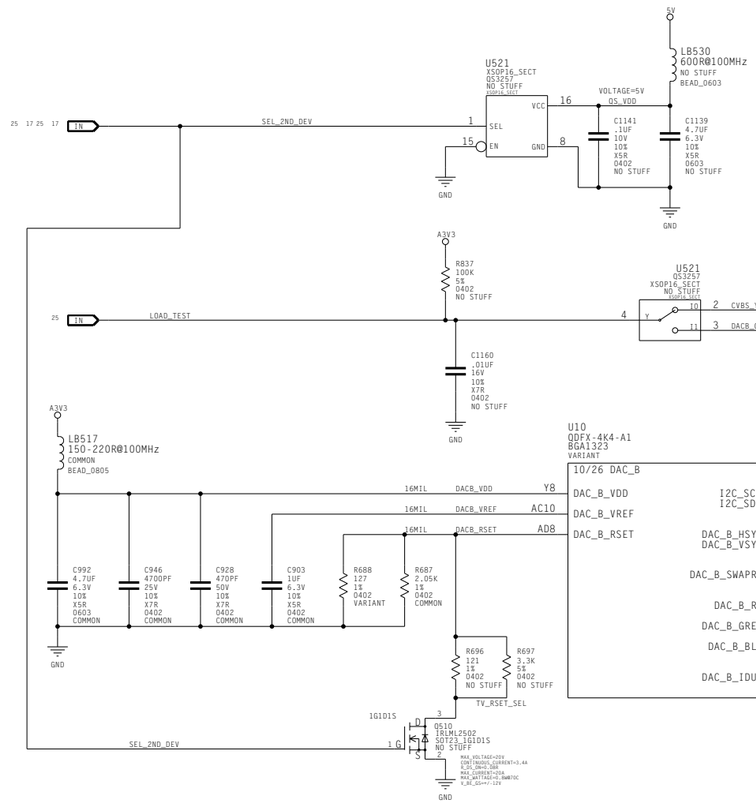


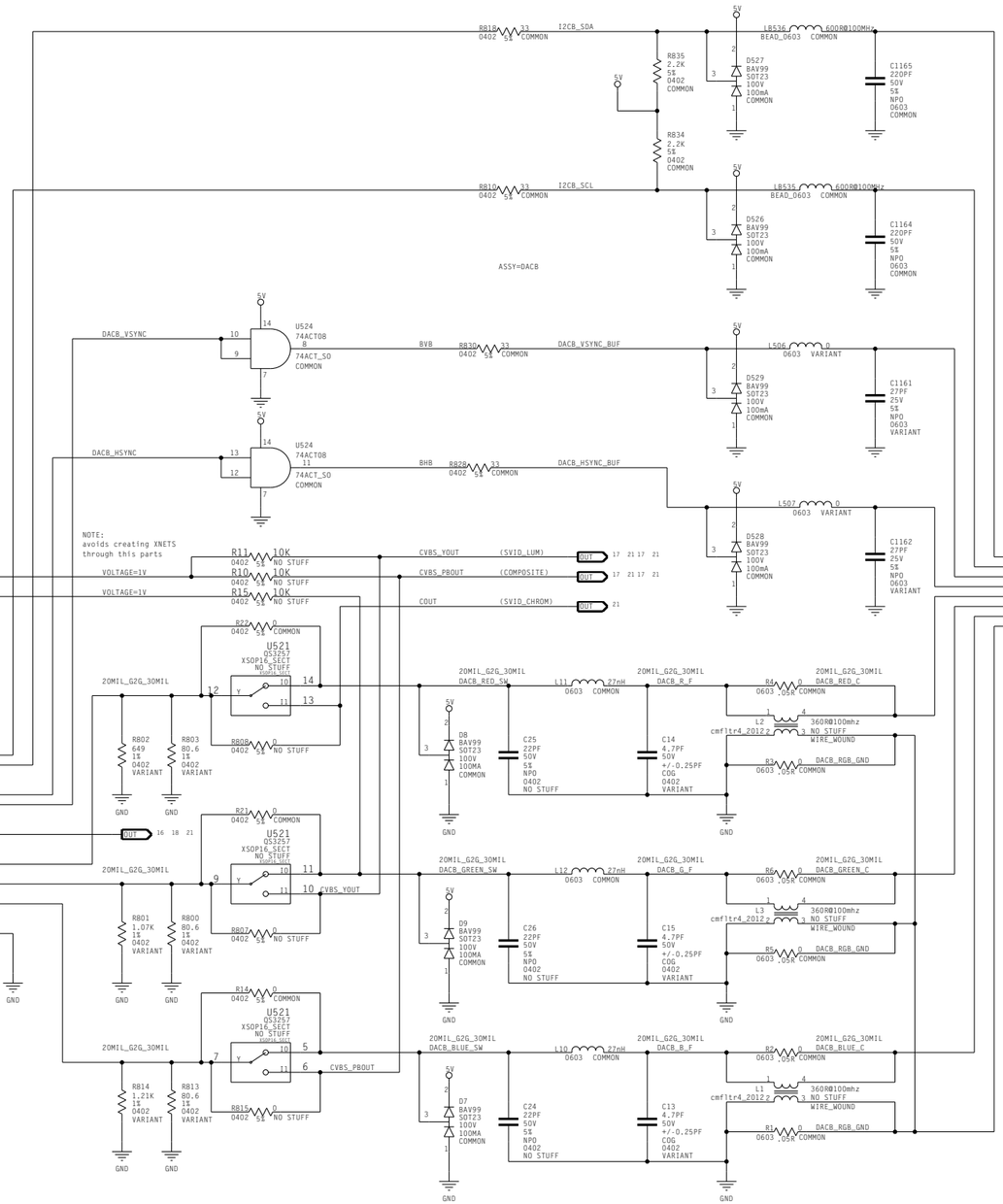
Place in output filter section!

ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	DACA filter and VGA connector, SOUTH

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	16 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

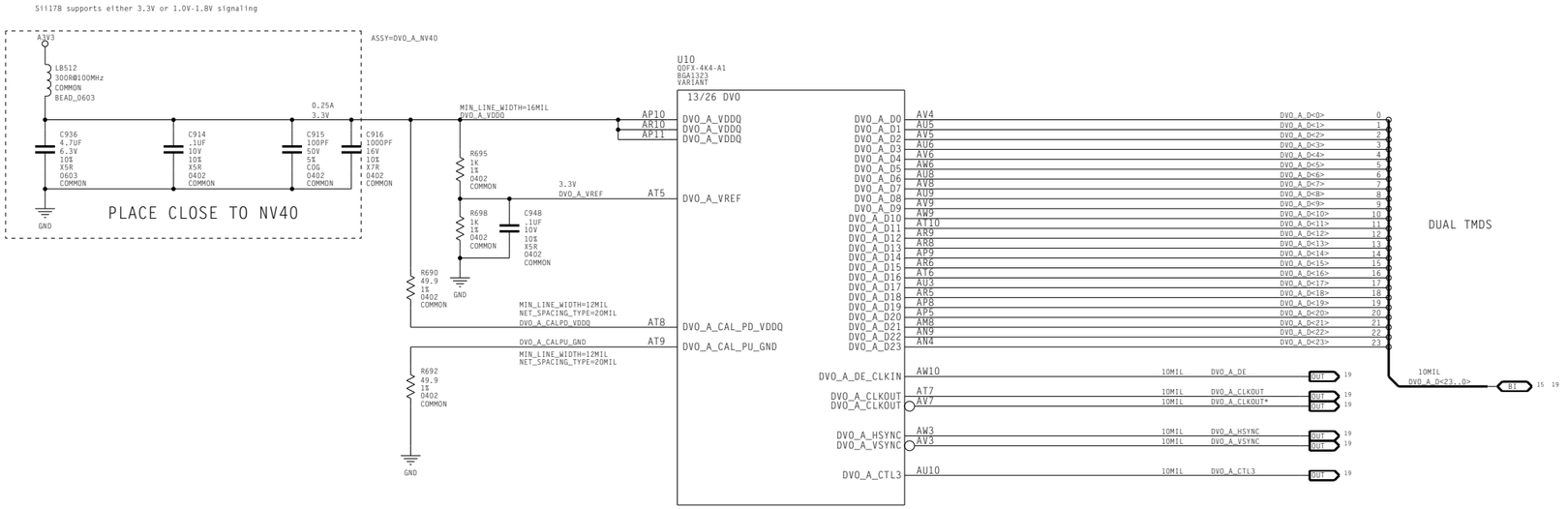


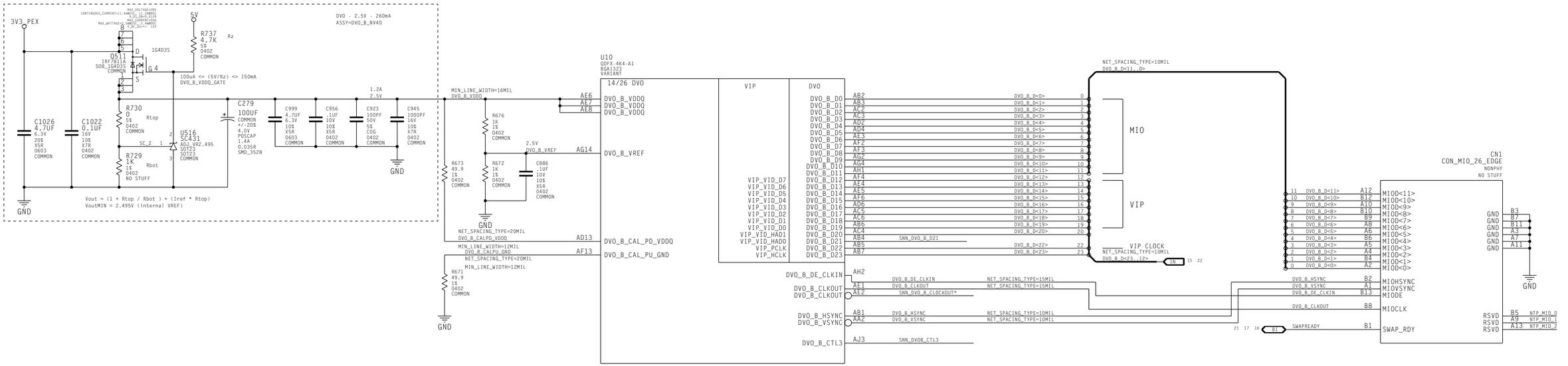


ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	DACB Filter, RGB SWITCH and VGA connector

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	17 OF 31
NAME	TSchirmer	DATE	4-NOV-2004





ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	MIO ports

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	18 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

SOUTH TMDS (primary)

Sil178 Dual-Link TMDS

ISEL/RST - I2C Interface Select,
HIGH - active (config programmed by I2C)

When ISEL/RST = HIGH
BSEL/SCL - I2C CLK
DSEL/SDA - I2C DATA

NV40 duallink:
Master: pixel D<11..0>
Slave: pixel D<23..12>

U520
SI1178
78_TQFP64B
COMMON
012-10178-0000-000
N/A

I2C=0x72 (Slave)
SLAVE
BOTTOM

SII1xx (combi_sym)

NET RULES

NET	DIFFPAIR	SPACING	MIN_LINE_WIDTH
SIIA_TXD3	SIIA_TXD3	25MIL	3.5MIL
SIIA_TXD3*	SIIA_TXD3	25MIL	3.5MIL
SIIA_TXD4	SIIA_TXD4	25MIL	3.5MIL
SIIA_TXD4*	SIIA_TXD4	25MIL	3.5MIL
SIIA_TXD5	SIIA_TXD5	25MIL	3.5MIL
SIIA_TXD5*	SIIA_TXD5	25MIL	3.5MIL
NTP_SIIA_NTC			
NTP_SIIA_NTC*			

MASTER
I2C Address is 70h and is based on MAST and DUAL pins.

SLAVE
I2C Address is 72h

Notes:

Make sure Software knows and programs this correctly.
1. Detect Dual-Link Capable
2. Detect Master and Slave
3. Both Master and Slave transmitters must
   set bit 2 (BSEL) at register addr 0x08 to 0 for 12-biot mode
4. For frequencies less than or equal to 165Mhz,
   bit 0 (PD) at register addr 0x08 of Slave must be set to 0.
   For frequencies greater than 165Mhz,
   bit 0 (PD) at register addr 0x08 of Slave must be set to 1.
5. Skew beween Master and Slave can be controlled by DCTL[2:0] register
6. Both Single-Link and Dual-Link mode will be configured via I2CC

U3
SII1162
162_TSSOP48
NO STUFF
012-11162-0000-000
SOLE SOURCE

MASTER
SINGLE
TOP

SII1162

NET RULES

NET	DIFFPAIR	SPACING	MIN_LINE_WIDTH
SIIA_TXD0	SIIA_TXD0	25MIL	3.5MIL
SIIA_TXD0*	SIIA_TXD0	25MIL	3.5MIL
SIIA_TXD1	SIIA_TXD1	25MIL	3.5MIL
SIIA_TXD1*	SIIA_TXD1	25MIL	3.5MIL
SIIA_TXD2	SIIA_TXD2	25MIL	3.5MIL
SIIA_TXD2*	SIIA_TXD2	25MIL	3.5MIL
SIIA_TXC	SIIA_TXC	25MIL	3.5MIL
SIIA_TXC*	SIIA_TXC	25MIL	3.5MIL

U2
SI1178
78_TQFP64B
COMMON
012-10178-0000-000
N/A

I2C=0x70 (Master)
MASTER
TOP

SII1xx (combi_sym)

NET RULES (OTHER)

NET	PHYSICAL	VOLTAGE	
SIIA_VCC	SIIA_VCC	12 MIL	3.3V	SIIA_VCC
SIIA_AVCC	SIIA_AVCC	12 MIL	3.3V	SIIA_AVCC
SIIA_PVCC1	SIIA_PVCC1	12 MIL	3.3V	SIIA_PVCC1
SIIA_PVCC2	SIIA_PVCC2	12 MIL	3.3V	SIIA_PVCC2

ASSY: DVO_A_COMMON stuff for single/dual link
ASSY: DVO_A_DS stuff for single/dual link
ASSY: DVO_A_D stuff for dual link
ASSY: DVO_A_S stuff for single link

MODIFIED AC TERMINATION

AC C33 22PF 50V 5% NPO 0402 COMMON
A5 C1126 22PF 50V 5% NPO 0402 COMMON
A4 C1143 22PF 50V 5% NPO 0402 COMMON
A3 C1144 22PF 50V 5% NPO 0402 COMMON
A2 C40 22PF 50V 5% NPO 0402 COMMON
A1 C39 22PF 50V 5% NPO 0402 COMMON
A0 C31 22PF 50V 5% NPO 0402 COMMON

ASSY=DVO_A_TERM_CAP

DDC 5V
Place near connector
C2 470PF 25V 10% X7R 0402 COMMON
ASSY=DACA_DVI

ASSY=DVO_A_TERM_R

J3
DVI_I
DVI_I
COMMON

SIIA_TXD0*	R27	150	A0	R26	150	TX0-	17
SIIA_TXD0	R32	150	A1	R31	150	TX0+	18
SIIA_TXD1*	R25	150	A2	R24	150	TX1-	9
SIIA_TXD1	R809	150	A3	R811	150	TX1+	10
SIIA_TXD2*	R804	150	A4	R806	150	TX2-	1
SIIA_TXD2	R798	150	A5	R799	150	TX2+	2
SIIA_TXD3*						SHLD24	3
SIIA_TXD3						SHLD13	11
SIIA_TXD4*						SHLD05	19
SIIA_TXD4						TX3-	12
SIIA_TXD5*						TX3+	13
SIIA_TXD5						TX4-	4
						TX4+	5
						TX5-	20
						TX5+	21
						DDCC	6
						DDCD	7
						VDDC	14
						GND	15
						SHLDC	22
						TXC-	24
						TXC+	23
						VSYNC	8
						HPD	16
						SHIELD2	26

DVIA_HPD_C
C1 R
C2 G
C3 B
C5 AGND1
C5A AGND2
C4 HSYNC

12CA_SCL_C
12CA_SDA_C
DACA_RED_C
DACA_GREEN_C
DACA_BLUE_C
DACA_RGB_GND
DACA_HSYNC_C
DACA_VSYNC_C

DVIA_HPD_F
R8 1K 0402 5% COMMON
LB2 600R@100MHz BEAD_0603 COMMON
R9 10K 5% 0402 COMMON
D10 BAY99 SOT23 100V 100MA COMMON
C4 220PF 50V 5% NPO 0603 COMMON
PullDown for default LOW

R785 4.7K 0402 5% COMMON
R786 4.7K 0402 5% COMMON
R787 4.7K 0402 5% COMMON
R786A 4.7K 0402 5% COMMON
R772 0 5% 0402 COMMON
R773 0 5% 0402 NO STUFF
R37 0 5% 0402 COMMON DUAL
R39 1.5K 5% 0402 COMMON
R38 0 5% 0402 NO STUFF SINGLE
R44 1.5K 5% 0402 NO STUFF
R785A 470 0603 1% COMMON
R783 4.7K 5% 0402 COMMON
R782 4.7K 5% 0402 COMMON
R781 4.7K 5% 0402 COMMON
C1098 .1UF 10V 10% X5R 0402 COMMON
C54 .1UF 10V 10% X5R 0402 COMMON

RP501 220 0402X4 5% NO STUFF
RP502 220 0402X4 5% NO STUFF
RP503 220 0402X4 5% NO STUFF

C1085 .1UF 10V 10% X5R 0402 COMMON
C1086 100PF 50V 5% C0G 0402 COMMON
C1087 100PF 50V 5% C0G 0402 COMMON
C63 .1UF 10V 10% X5R 0402 COMMON
C68 4.7UF 6.3V 10% X5R 0603 COMMON
LB528 600R@100MHz BEAD_0603 COMMON

C46 100PF 50V 5% C0G 0402 COMMON
C1124 100PF 50V 5% C0G 0402 COMMON
C43 .1UF 10V 10% X5R 0402 COMMON
C1123 .1UF 10V 10% X5R 0402 COMMON
C47 4.7UF 6.3V 10% X5R 0603 COMMON
LB6 600R@100MHz BEAD_0603 COMMON
C1116 4.7UF 6.3V 10% X5R 0603 COMMON

C1122 100PF 50V 5% C0G 0402 COMMON
C44 .1UF 10V 10% X5R 0402 COMMON
C1125 4.7UF 6.3V 10% X5R 0603 COMMON
C1121 100PF 50V 5% C0G 0402 COMMON
C45 .1UF 10V 10% X5R 0402 COMMON
C48 4.7UF 6.3V 10% X5R 0603 COMMON
LB5 600R@100MHz BEAD_0603 COMMON

C1114 .1UF 10V 10% X5R 0402 COMMON
C1090 100PF 50V 5% C0G 0402 COMMON
C60 100PF 50V 5% C0G 0402 COMMON
C58 100PF 50V 5% C0G 0402 COMMON
C1113 100PF 50V 5% C0G 0402 COMMON
C49 100PF 50V 5% C0G 0402 COMMON
C1101 .1UF 10V 10% X5R 0402 COMMON
C50 .1UF 10V 10% X5R 0402 COMMON
C1075 4.7UF 6.3V 10% X5R 0603 COMMON
LB527 600R@100MHz BEAD_0603 COMMON
C1082 4.7UF 6.3V 10% X5R 0603 COMMON

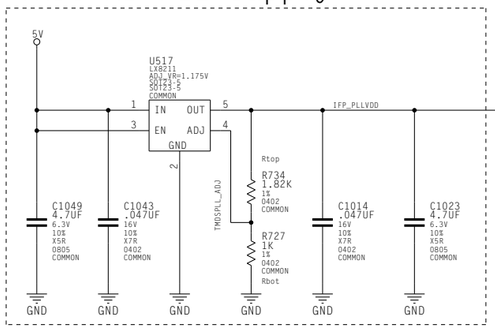
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	DUAL LINK TMDS External with Silicon Image (SOUTH)

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	19 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

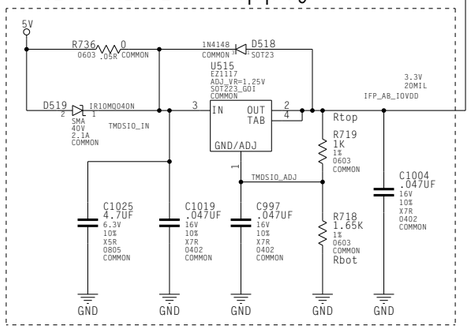
NORTH TMDS (secondary)

TMDS AB PLL Supply

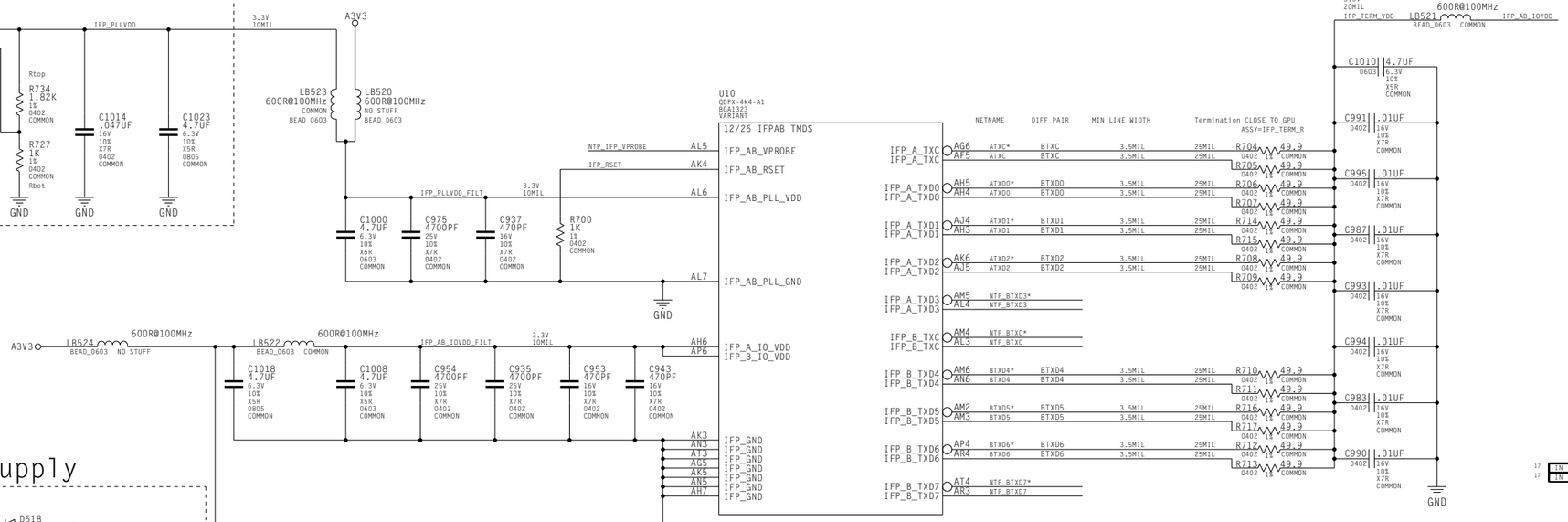


VOUT = 1.175 * (1 + (Rtop / Rbot))
3.31V = 1.175 * (1 + (1.82K / 1K))

TMDS AB IO Supply



VOUT = 1.25 * (1 + (Rbot / Rtop))
3.31 = 1.25 * (1 + (1.65K / 1K))



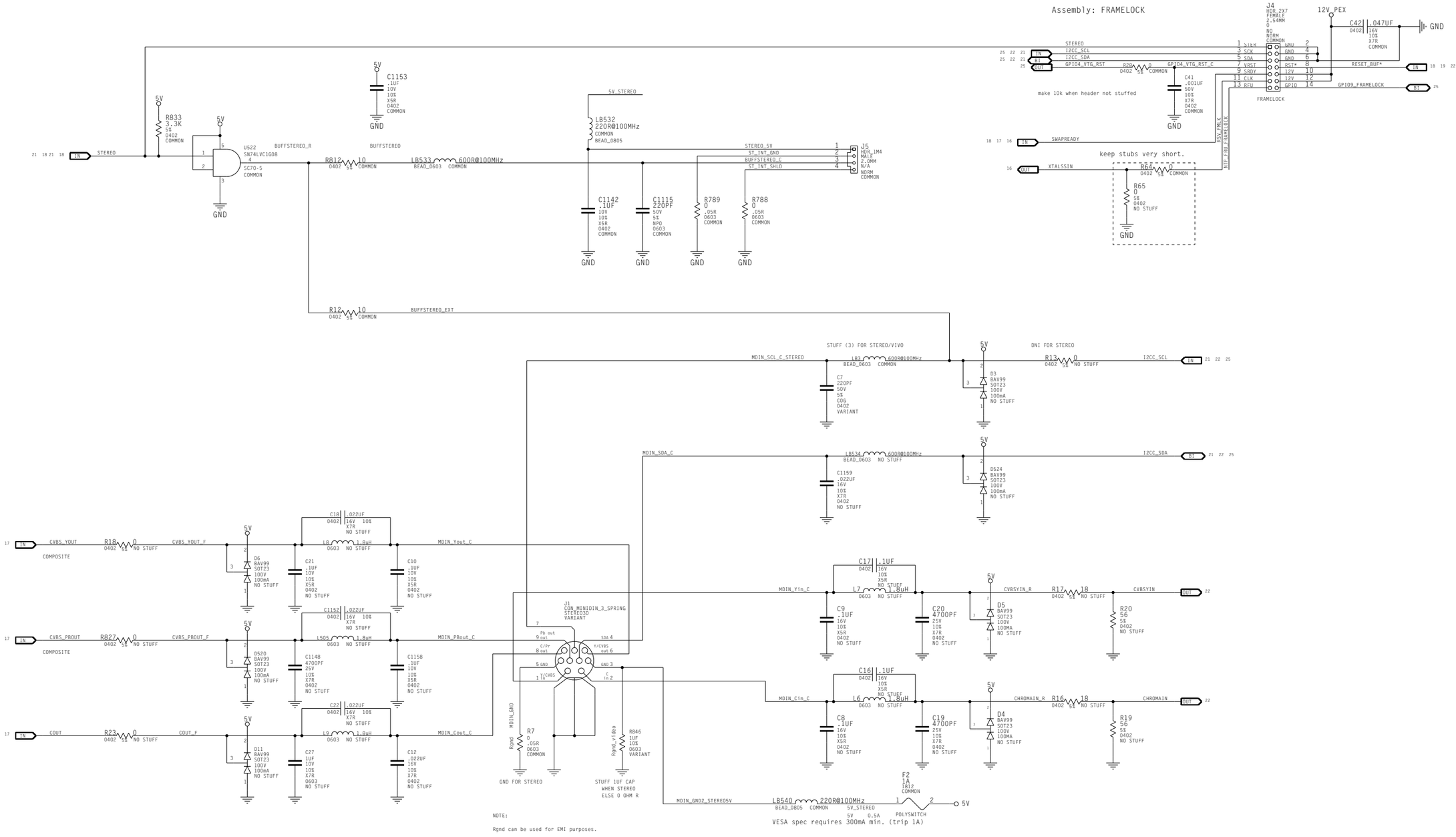
DVI B (north) DAC B for RA and straight DVI con.

ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	DUAL LINK TMDS Internal (NORTH)

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	20 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

Framelock



ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Video In/Out Connector, Stereo Connector, Framelock header

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

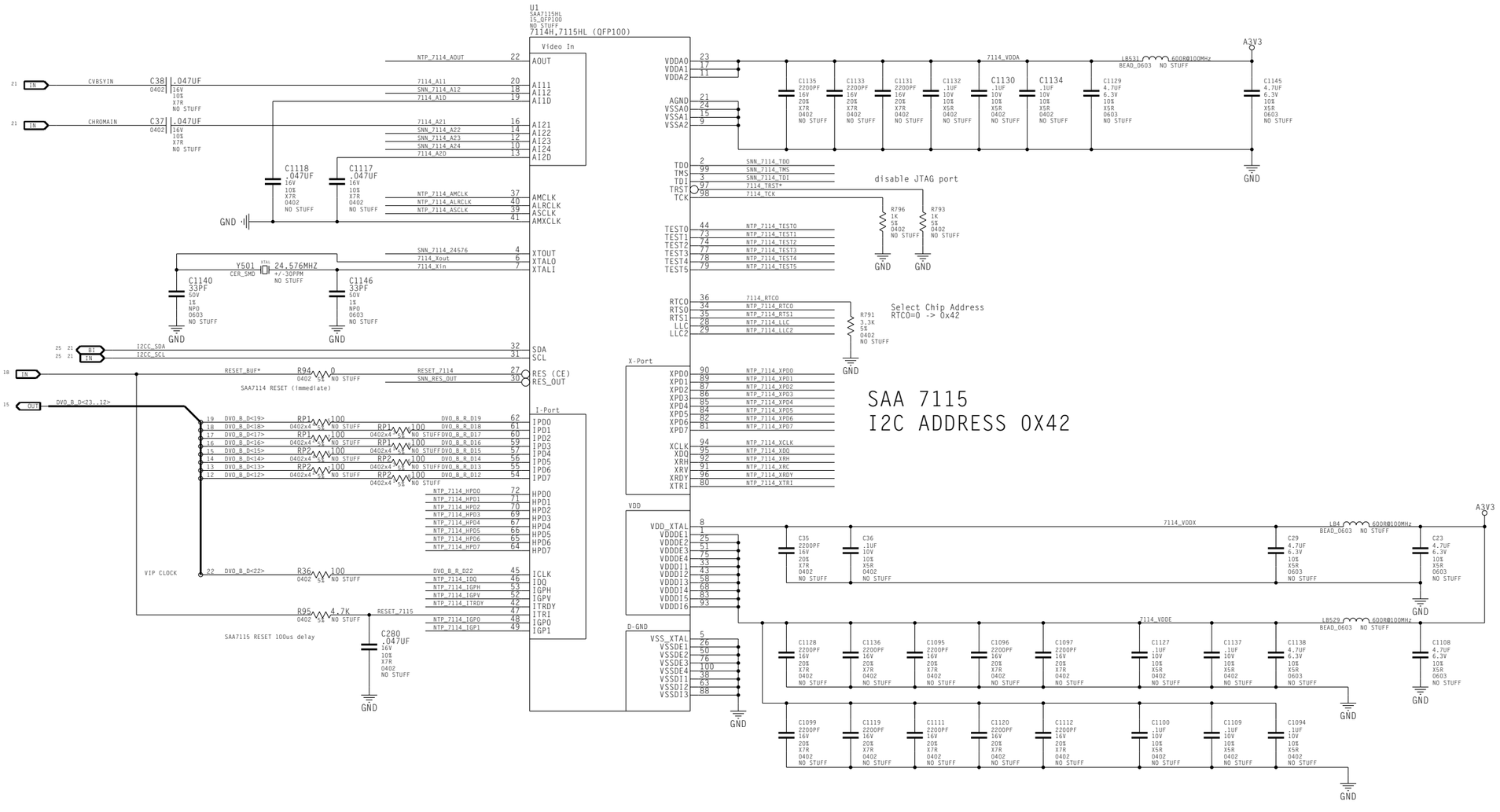
NV_PN	600-50214-0000-400		
ID	design	PAGE	21 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

NET RULES

NET	SPACING	PHYSICAL	VOLTAGE
7114_VDDA		12 MIL	3.3V
7114_VDDE		12 MIL	3.3V
7114_VDDX		12 MIL	3.3V
7114_Xout	20MIL		
7114_Xin	20MIL		

ASSY: 7114_COMMON

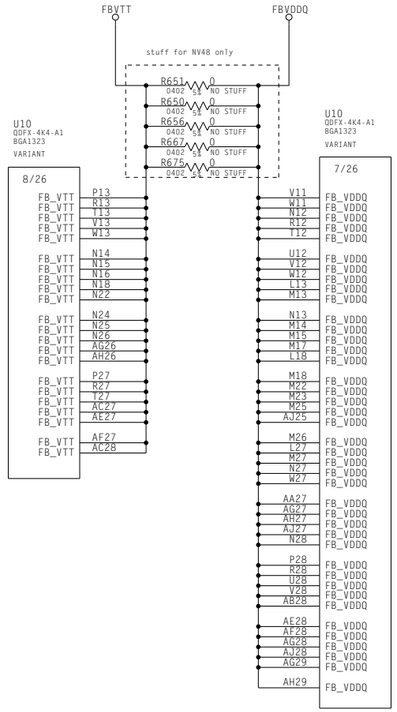
VIDEO CAPTURE

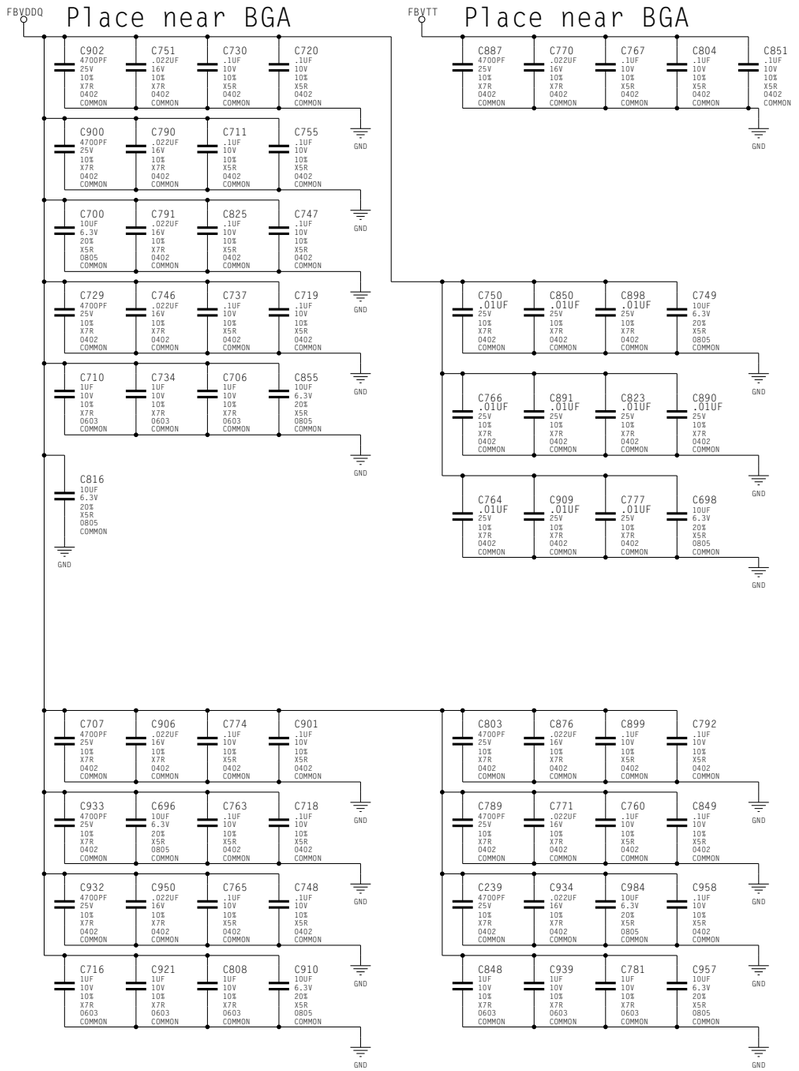


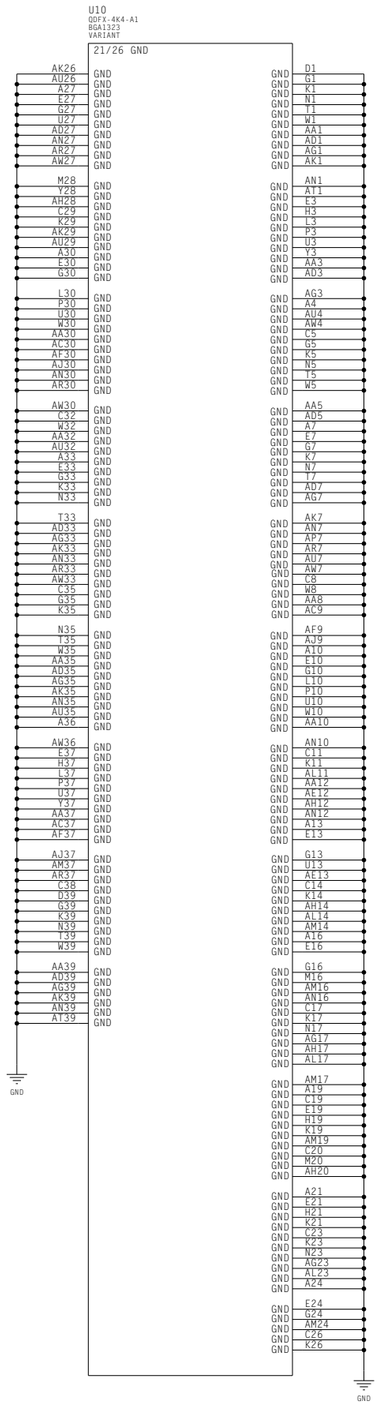
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	Video Capture (SAA7115)

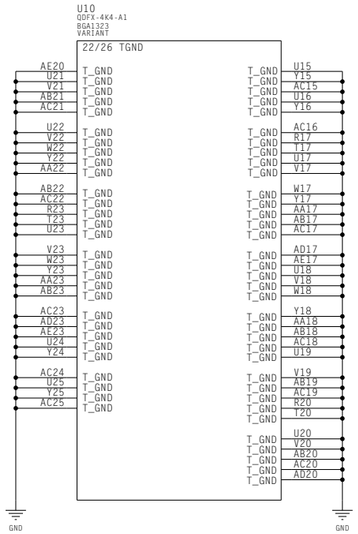
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	22 OF 31
NAME	TSchirmer	DATE	4-NOV-2004





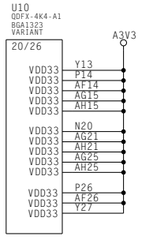


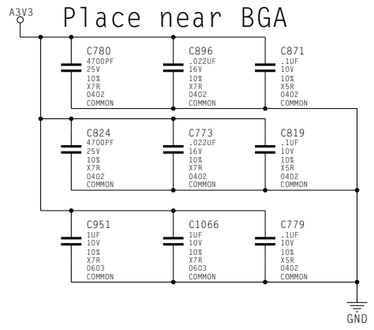


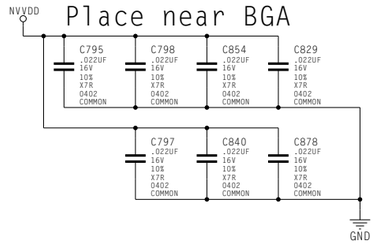
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	GPU decap: FBVDDQ and FBVTT, GND

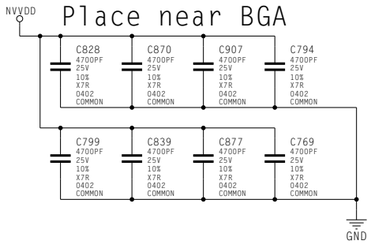
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

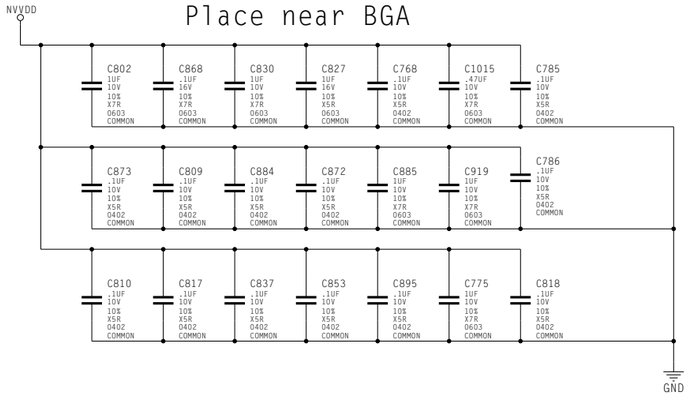
NV_PN	600-50214-0000-400		
ID	design	PAGE	23 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

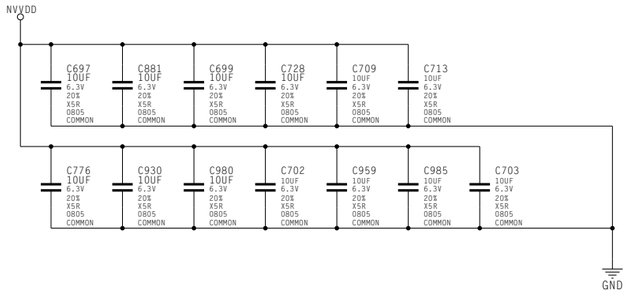


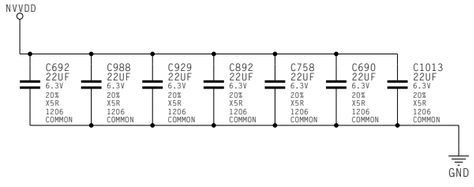


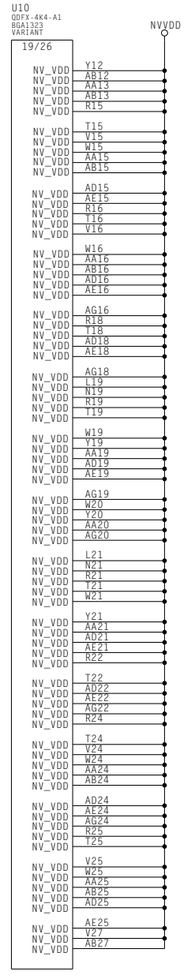












ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	GPU decap: 3V3 and NVVDD

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	24 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

GPIO CONTROL

C502 .1UF 10V 10% X5R 0402 COMMON

U523 U_XOR_2IN SC70 COMMON

DVIA_HPD, DVIB_HPD → DVIAB_HPD_R

R832 1K 5% 0402 COMMON

XOR bypass: R805 0 5% 0402 NO STUFF; R831 0 5% 0402 NO STUFF

R838 10K 5% 0402 COMMON — Sel_2nd_Dev: PU for 'NO MUX' detection

U10 QDFX-4K4-A1 BGA1323 VARIANT — 17/26 GPIO

GPIO<0>	AE9	LOAD_TEST
GPIO<1>	AF8	GPIO_DVI_A_HPD
GPIO<2>	AE11	FAN_PWM
GPIO<3>	AF10	GPIO3_HIGH_PWR
GPIO<4>	AJ8	GPIO4_VTG_RST
GPIO<5>	AG8	NV_Vsel0
GPIO<6>	AG9	NV_Vsel1
GPIO<7>	AG11	SEL_2ND_DEV
GPIO<8>	AH8	GPIO_SLOW*
GPIO<9>	AH9	GPIO9_FRAMELOCK

GPIO_DVI_B_HPD — R34 0 0603 .05W COMMON

R703 10K 5% 0402 NO STUFF

Default Sel_2nd_Dev: Pulldown for VGAout

VID CONTROL

Default selection for NVVDD_VID[4..1]

D503 BAT54C 25V 200MA SOT23 COMMON — 1.4V: R516 0 5% 0402 NO STUFF; R515 0 5% 0402 NO STUFF

D502 BAT54C 25V 200MA SOT23 COMMON — R514 0 5% 0402 COMMON; R513 0 5% 0402 COMMON

Q502 BSS138 SOT23_1G1D1S COMMON — R512 10K 5% 0402 COMMON

D508 BAT54C 25V 200MA SOT23 COMMON — 1.3V: R532 0 5% 0402 NO STUFF; R531 0 5% 0402 COMMON

D507 BAT54C 25V 200MA SOT23 COMMON — R530 0 5% 0402 NO STUFF; R529 0 5% 0402 COMMON

Q504 BSS138 SOT23_1G1D1S COMMON — R512 10K 5% 0402 COMMON

D513 BAT54C 25V 200MA SOT23 COMMON — 1.2V: R533 0 5% 0402 NO STUFF; R541 0 5% 0402 NO STUFF

D512 BAT54C 25V 200MA SOT23 COMMON — R540 0 5% 0402 NO STUFF; R543 0 5% 0402 COMMON

Q506 BSS138 SOT23_1G1D1S COMMON

D506 BAT54ALT1 30V 200MA SOT23 COMMON — R526 10K 5% 0402 COMMON

D511 BAT54ALT1 30V 200MA SOT23 COMMON — SNN_GATE_NC, GATE_DEF, GATE_DEF_R

R527 0 5% 0402 NO STUFF bridge diode; R528 10K 5% 0402 COMMON additional PD

NVVDD_VID<4..1> → OUT 27

NVVDD Voltage Select

NVVDD = 0.8V-1.55V

Regulator: ISL6559

Control via NV_GPIOs NV_VSEL[2..0] :

VID 4 3 2 1	NVVDD Vout
1 1 1 1	0.80V
1 1 1 0	0.85V
1 1 0 1	0.90V
1 1 0 0	0.95V
1 0 1 1	1.00V
1 0 1 0	1.05V
1 0 0 1	1.10V
1 0 0 0	1.15V
0 1 1 1	1.20V
0 1 1 0	1.25V
0 1 0 1	1.30V
0 1 0 0	1.35V
0 0 1 1	1.40V
0 0 1 0	1.45V
0 0 0 1	1.50V
0 0 0 0	1.55V

NET RULES

NET	SPACING	PHYSICAL
THERMDA		10MIL
THERMDC		10MIL
FAN_PWM	20MIL	10MIL
FAN_PWM_B	20MIL	12MIL
FAN_PWM_C	20MIL	12MIL

I2C C & D, Thermal Diode

U10 QDFX-4K4-A1 BGA1323 VARIANT — 18/26 THERMAL: THERM_DN (CATHODE) C39, THERM_DP (ANODE) B39

Place 10 Mil GND guard around THERMDA/C

Note: THERMDN PIN = THERMDC; THERMDP PIN = THERMDA

C694 2200PF 50V 10% X7R 0603 COMMON

R794 2.2K 5% 0402 COMMON; R792 2.2K 5% 0402 COMMON

U512 MAX6649MUA 50B_12MIL COMMON — D+, D-, VDD, THERM, ALERT, SCL, SDA, GND

C689 .1UF 10V 10% X5R 0402 COMMON

R636 2.2K 5% 0402 COMMON THERM*; R638 2.2K 5% 0402 COMMON

I2CC_SCL, I2CC_SDA — silicon image NOT 5V tolerant

U10 QDFX-4K4-A1 BGA1323 VARIANT — 16/26 I2C

I2C_SDA2	AG12	GPU_I2CC_SDA
I2C_SCL2	AF12	GPU_I2CC_SCL
I2C_SDA3	AJ13	I2CD_SDA
I2C_SCL3	AH13	I2CD_SCL

R790 33 0402 5% COMMON; R797 33 0402 5% COMMON

R41 2.2K 5% 0402 COMMON

U4 AT88SC0808C 50B NO STUFF — SCL, SDA, SDA, NC, VCC, VCC, GND, GND; NTP_HDCP_ROM

C64 4.7UF 6.3V 10% X5R 0805 NO STUFF

R40 2.2K 5% 0402 COMMON

FAN CONTROL 3.0

12V_PEX

3V3_PEX: R778 1K 5% 0402 NO STUFF; R779 1K 5% 0402 COMMON

C1079 1UF 25V 10% X7R 0805 COMMON

D12 BAT43 SOD323 40V 400MA COMMON

C1069 1UF 16V 10% X7R 0805 NO STUFF

C1074 10UF 16V 20% X7R 1206 COMMON

L13 22uH SMD_4_5X4_0MM COMMON

FAN +12V GND — J6 HDR_1MZ_FAN MALE 0.5MM 0 NORM COMMON

FAN_PWM_SW, FAN_PWM_B, FAN_PWM_C

Q512 TRLML2502 SOT23_1G1D1S COMMON

Q513 BSS138 SOT23_1G1D1S COMMON

Q514 BSS138 SOT23_1G1D1S COMMON

FAN_PWM, THERM*, FAN_THERM_BYPASS

R776 1K 5% 0402 COMMON; R780 0 5% 0402 NO STUFF

FAN_PWM = 1 turns fan OFF
FAN_PWM = 0 turns fan On

U10 QDFX-4K4-A1 BGA1323 VARIANT — 23/26 POWER SENSE

NV_VDD_SENSE	W28	NVVDD_SENSE → OUT 27
NV_VDD_GND_SENSE	AA28	NVVDD_SENSE* → OUT 27
FB_VDDQ_SENSE	M19	VTP_FBVDDQ_SENSE
FB_VDDQ_GND_SENSE	M21	VTP_FBVDDQ_SENSE*

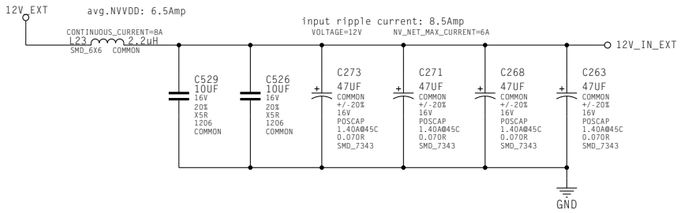
use accessable vias or TP's

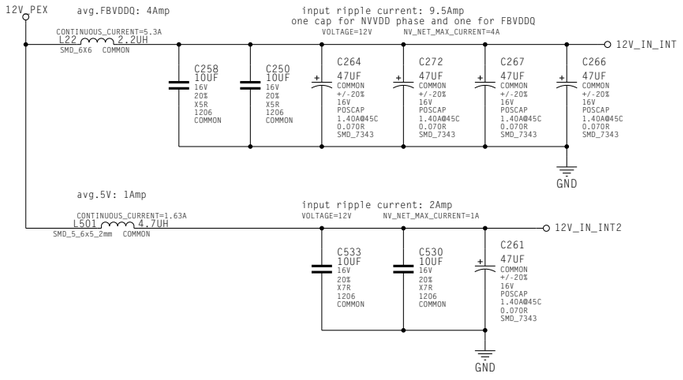
ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	GPIOs, NVVDD VID, TEMP and FAN Control

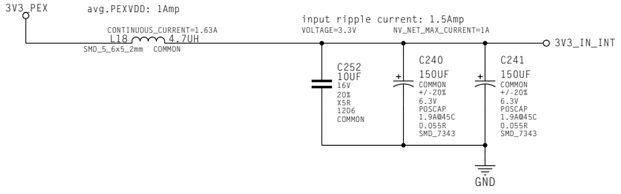
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

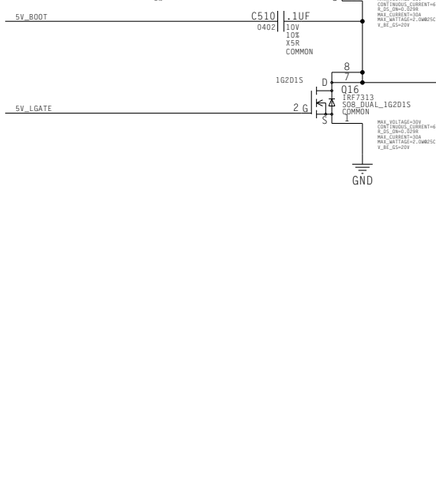
NV_PN	600-50214-0000-400		
ID	design	PAGE	25 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

Power rail input filter
place close to switcher input



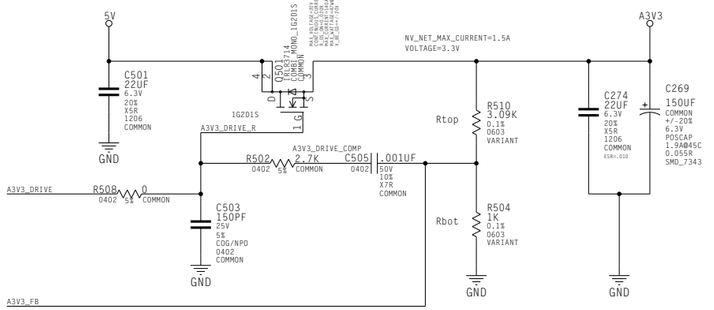






45.3k results in 600kHz

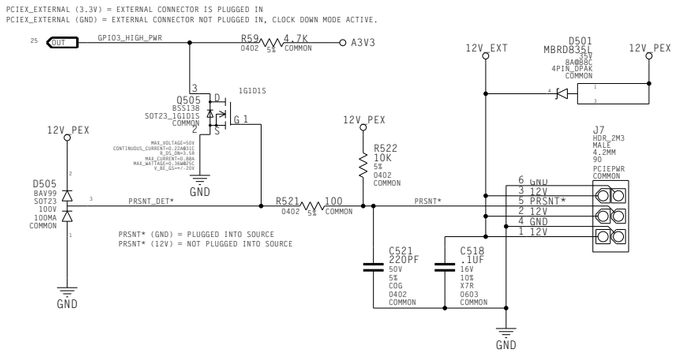
A3V3: 3.3V,1.5A



VOUT = 0.8V * (1 + (Rtop / Rbot))
3.27V = 0.8V * (1 + (3.09k / 1k))

5V: 5V,2A

VOUT = 0.8V * (1 + (Rtop / Rbot))
5.2V = 0.8V * (1 + (1k / 182R))



ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	POWER SUPPLY: Input filters, 5V and 3V3

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	26 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

12V: 6.5A = 1.4V/12V/90% * 50A

NVVDD = 1.0V..1.4V (50A)

POSCAP needed only for BULK

1.4V 50A

C579 47UF 6.3V 20% X5R 1206 COMMON
C576 47UF 6.3V 20% X5R 1206 COMMON
C575 47UF 6.3V 20% X5R 1206 COMMON
C574 47UF 6.3V 20% X5R 1206 COMMON
C573 47UF 6.3V 20% X5R 1206 COMMON
C571 47UF 6.3V 20% X5R 1206 COMMON
C572 47UF 6.3V 20% X5R 1206 COMMON
C568 47UF 6.3V 20% X5R 1206 COMMON
C236 330UF COMMON +/-20% 2.5V POSCAP 3.1A045C 0.015R SMD_7343
C235 330UF COMMON +/-20% 2.5V POSCAP 3.1A045C 0.015R SMD_7343
C225 330UF COMMON +/-20% 2.5V POSCAP 3.1A045C 0.015R SMD_7343
C237 330UF COMMON +/-20% 2.5V POSCAP 3.1A045C 0.015R SMD_7343

NVVDD

GND

ESR : 3mOhm max

Load Sense

Connect to NVVDD via SenseBack from NV45

25 IN NVVDD_SENSE
25 IN NVVDD_SENSE*

FOR BRINGUP OUTPUT CAP IS SENSE
Connect to NVVDD and GND at output cap

NVVDD
C565 .001UF 50V 10% X7R 0402 COMMON
R583 1K 0402 1% COMMON
R582 1K 0402 1% COMMON
GND

Comp Network

C3
C566 .01UF 50V 10% X7R 0603 COMMON NV_VDIFF_FB
R3 R591 2.2 5% 0402 COMMON
R1 R584 1.8K 5% 0402 COMMON
C2 C552 2200PF 50V 10% X7R 0402 COMMON
C1 C547 .1UF 16V 10% X7R 0603 COMMON NV_COMP_FB
R2 R565 3K 5% 0402 COMMON
DROOP R585 0 5% 0402 COMMON

12V_PEX
R593 150 5% 0805 COMMON ISL6559_VCC_RR
R592 150 5% 0805 COMMON
C559 1UF 10V 10% X7R 0805 COMMON
C564 .047UF 16V 10% X7R 0402 COMMON
GND GND

U503
ISL6559CR_FS
DYNAMIC VID(0.8V..1.55V)
MLFP32
MLFP32
COMMON
4 Phase PWM

5V ISL6559_VCC

15	VCC		
12	RGND	PWM1	21 PWM_1
11	VSEN	ISEN1	22 ISEN_1
10	VDIFF	PWM2	20 PWM_2
9	IOUT	ISEN2	18 ISEN_2
7	FB	PWM3	16 PWM_3
6	COMP	ISEN3	17 ISEN_3
25	PGOOD	PWM4	24 PWM_4
27	EN	ISEN4	23 ISEN_4
26	FS/DIS	OVP	29
13	GND		
14	GND		
19	GND		
28	GND		
33	GND(PAD)		
4	NC		
3	NC		
31	NC		

NV_VDIFF
NV_IOUT
NV_FB
NV_COMP

R581 0 0402 5% NO STUFF disable phase 3 and 4 when stuffed.
R580 0 0402 5% COMMON disabled phase 4 when stuffed.

25 IN NVVDD_VID<4..1>

1	NVVDD_VID<1>	VID1=50mV	
2	NVVDD_VID<2>	VID2=100mV	
3	NVVDD_VID<3>	VID3=200mV	
4	NVVDD_VID<4>	VID4=400mV	
	NVVDD_VID<0>	VID0=25mV	

NTP_ISL6559_PGOOD

NV_FS/DIS
R554 43.2K 1% 0402 COMMON
32.4kohms 750KHz

Set VID=LOW to prevent Shutdown state
R561 0 5% 0402 COMMON

A3V3
R555 1K 5% 0402 COMMON
R556 1K 5% 0402 COMMON
ISL6559_ENABLE
ENABLE >2.5V

NTP_ISL_1 NTP_ISL_2 NTP_ISL_3 NTP_NV_OVP

assembly of SO8 on LFPAK footprint is possible (i.e 2 SO8's instead of one LFPAK.

U504 ISL6605CR MOSFET_DRIVER MLFP8 MLFP8 COMMON

5V
C548 1UF 25V 10% X7R 0805 COMMON
C539 1UF 25V 10% X7R 0805 COMMON
GND
R572 470K 0402 5% COMMON PWM_1

5	VCC	UGATE	8
6	EN	PHASE	7
3	GND	BOOT	1
9	THERMAL_GND		
2	PWM	LGATE	4

THERMAL GND PACKAGE
R546 1.62K 0603 1% COMMON
ISEN_1

16MIL NV_UG1 R557 0 0402 5% COMMON 16MIL NV_UG1_R
NV_PHASE1
16MIL NV_BOOT1 R562 0 0603 .05R VARIANT C535 .100UF 25V 10% X7R COMMON
16MIL NV_LG1 R571 0 0402 5% COMMON 16MIL NV_LG1_R

LFPAK Q12 HAT2168H LFPAK COMMON
LFPAK Q1 HAT2165H LFPAK COMMON
LFPAK Q6 HAT2165H LFPAK NO STUFF
C554 .39PF 50V 5% COG 0402 COMMON

Place close to DRAIN
C243 1UF 16V 10% X5R 0603 COMMON
C259 10UF 16V 20% X5R 1206 COMMON
C257 10UF 16V 20% X5R 1206 COMMON
12V_IN_EXT
GND

17A 1.4V
C560 1500PF 50V 10% X7R 0603 COMMON
NV_RCG1 R587 15 5% 0603 COMMON
L14 0.33UH SMD_7X6 VARIANT
D514 IR10MQ040N SMA 40V COMMON 120A@5US
C578 47UF 6.3V 20% X5R 1206 COMMON
NVVDD

Risen: 750 Ohm = (5mOhms/2)/50uA*60A/4phases

U505 ISL6605CR MOSFET_DRIVER MLFP8 MLFP8 COMMON

5V
C540 1UF 25V 10% X7R 0805 COMMON
C549 1UF 25V 10% X7R 0805 COMMON
GND
R574 470K 0402 5% COMMON PWM_2

5	VCC	UGATE	8
6	EN	PHASE	7
3	GND	BOOT	1
9	THERMAL_GND		
2	PWM	LGATE	4

THERMAL GND PACKAGE
R546 1.62K 0603 1% COMMON
ISEN_2

16MIL NV_UG2 R558 0 0402 5% COMMON 16MIL NV_UG2_R
NV_PHASE2
16MIL NV_BOOT2 R563 0 0603 .05R VARIANT C536 .100UF 25V 10% X7R COMMON
16MIL NV_LG2 R573 0 0402 5% COMMON 16MIL NV_LG2_R

LFPAK Q13 HAT2168H LFPAK COMMON
LFPAK Q2 HAT2165H LFPAK COMMON
LFPAK Q7 HAT2165H LFPAK NO STUFF
C555 .39PF 50V 5% COG COMMON

Place close to DRAIN
C244 1UF 16V 10% X5R 0603 COMMON
C528 10UF 16V 20% X5R 1206 COMMON
C262 10UF 16V 20% X5R 1206 COMMON
12V_IN_EXT
GND

17A 1.4V
C561 1500PF 50V 10% X7R 0603 COMMON
NV_RCG2 R588 15 5% 0603 COMMON
L15 0.33UH SMD_7X6 VARIANT
D515 IR10MQ040N SMA 40V COMMON 120A@5US
C577 47UF 6.3V 20% X5R 1206 COMMON
NVVDD

U506 ISL6605CR MOSFET_DRIVER MLFP8 MLFP8 COMMON

5V
C550 1UF 25V 10% X7R 0805 COMMON
C541 1UF 25V 10% X7R 0805 COMMON
GND
R576 470K 0402 5% COMMON
R570 0 0402 5% COMMON PWM_3R
PWM_3
disabling this pahse: unstuff

5	VCC	UGATE	8
6	EN	PHASE	7
3	GND	BOOT	1
9	THERMAL_GND		
2	PWM	LGATE	4

THERMAL GND PACKAGE
R547 1.62K 0603 1% COMMON
ISEN_3

16MIL NV_UG3 R559 0 0402 5% COMMON 16MIL NV_UG3_R
NV_PHASE3
16MIL NV_BOOT3 R564 0 0603 .05R VARIANT C537 .100UF 25V 10% X7R COMMON
16MIL NV_LG3 R575 0 0402 5% COMMON 16MIL NV_LG3_R

LFPAK Q14 HAT2168H LFPAK COMMON
LFPAK Q3 HAT2165H LFPAK COMMON
LFPAK Q8 HAT2165H LFPAK NO STUFF
C556 .39PF 50V 5% COG COMMON

Place close to DRAIN
C245 1UF 16V 10% X5R 0603 COMMON
C256 10UF 16V 20% X5R 1206 COMMON
C260 10UF 16V 20% X5R 1206 COMMON
12V_IN_EXT
GND

17A 1.4V
C562 1500PF 50V 10% X7R 0603 COMMON
NV_RCG3 R589 15 5% 0603 COMMON
L16 0.33UH SMD_7X6 VARIANT
D516 IR10MQ040N SMA 40V COMMON 120A@5US
C570 47UF 6.3V 20% X5R 1206 COMMON
NVVDD

U507 ISL6605CR MOSFET_DRIVER MLFP8 MLFP8 NO STUFF

Voltage section independend of chip!
ISL6207 5V 5V(ENABLE)
ISL6605 5V ENABLE)
5V
C551 1UF 25V 10% X7R 0805 COMMON
C542 1UF 25V 10% X7R 0805 COMMON
GND
R578 470K 0402 5% NO STUFF
R586 0 0402 5% NO STUFF PWM_4R
PWM_4

5	VCC	UGATE	8
6	EN	PHASE	7
3	GND	BOOT	1
9	THERMAL_GND		
2	PWM	LGATE	4

THERMAL GND PACKAGE
R549 1.62K 0603 1% NO STUFF
ISEN_4

PWM_3 R579 0 0402 5% NO STUFF
ISEN_3 R548 1.62K 0603 1% NO STUFF
Alternate PHASE3 to 12V_PEX

16MIL NV_UG4 R560 0 0402 5% NO STUFF 16MIL NV_UG4_R
NV_PHASE4
16MIL NV_BOOT4 R552 5.1 0603 5% NO STUFF C538 .100UF 25V 10% X7R NO STUFF
16MIL NV_LG4 R577 0 0402 5% NO STUFF 16MIL NV_LG4_R

LFPAK Q15 HAT2168H LFPAK NO STUFF
LFPAK Q4 HAT2165H LFPAK NO STUFF
LFPAK Q9 HAT2165H LFPAK NO STUFF
C557 .39PF 50V 5% COG NO STUFF

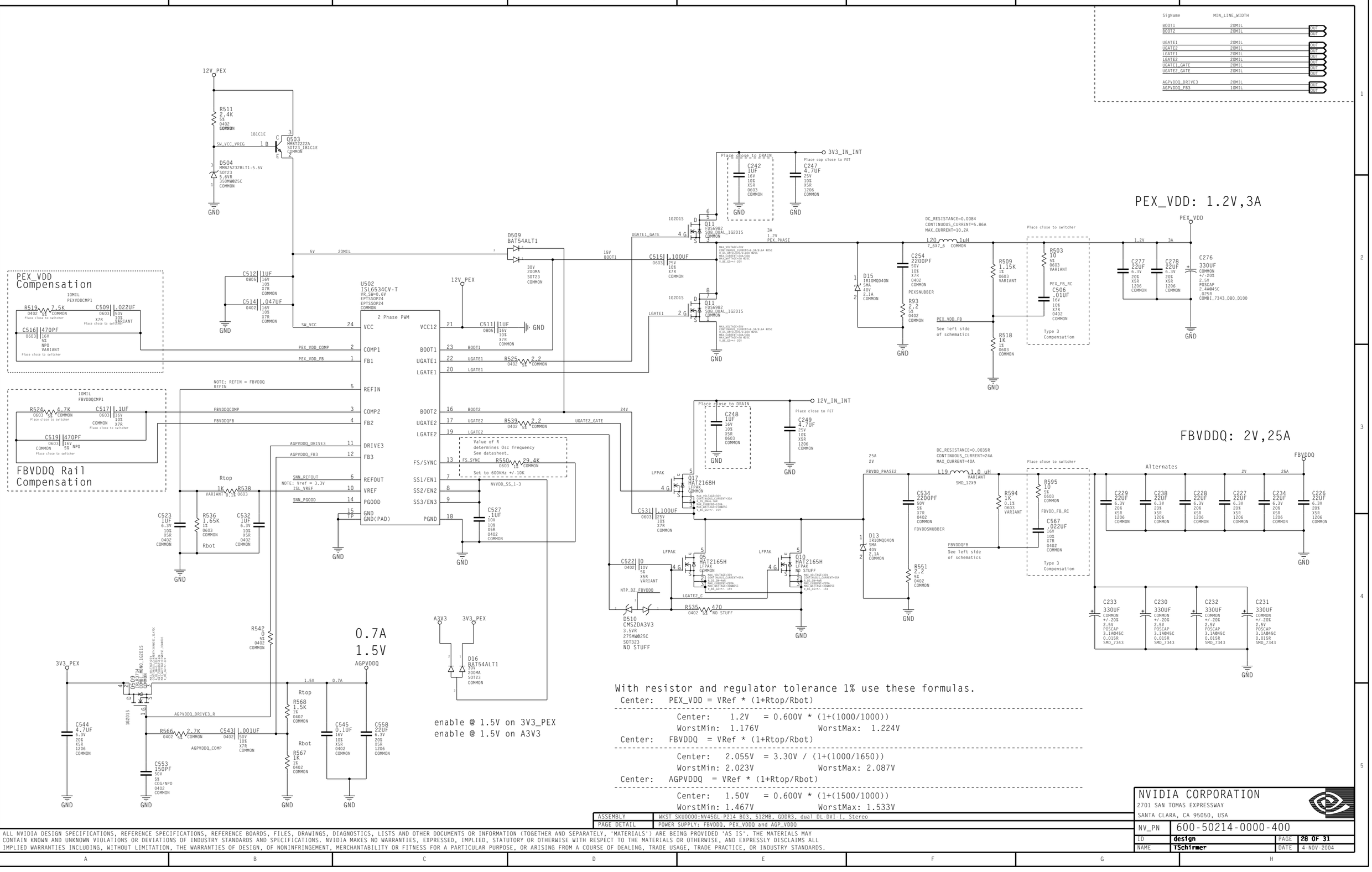
Place close to DRAIN
C246 1UF 16V 10% X5R 0603 COMMON
C251 10UF 16V 20% X5R 1206 COMMON
C265 10UF 16V 20% X5R 1206 COMMON
12V_IN_INT
GND

17A 1.4V
C563 1500PF 50V 10% X7R 0603 NO STUFF
NV_RCG4 R590 15 5% 0603 NO STUFF
L17 0.150uH SMD_7X6 NO STUFF
D517 IR10MQ040N SMA 40V NO STUFF 120A@5US
C569 47UF 6.3V 20% X5R 1206 COMMON
NVVDD

ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	POWER SUPPLY: Core power NVVDD

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	27 OF 31
NAME	TSchirmer	DATE	4-NOV-2004



*** Signal Cross-Reference for the entire design ***

7114_VDDA	22.1G< 22.2F
7114_VDDE	22.1G< 22.4G
7114_VDDX	22.1G< 22.4G
7114_XIN	22.1G< 22.3D
7114_XOUT	22.1G< 22.3D
AGPVDDQ_DRIVE3	28.1H> 28.3B
AGPVDDQ_FB3	28.1H> 28.3B
BOOT1	28.1H> 28.2D 28.3C
BOOT2	28.1H> 28.3C
BR_DEVID_0	2.4F<> 15.5B<>
CHROMAIN	21.4G> 22.2B<
COUT	17.3F> 21.5A<
CVBSYIN	21.4G> 22.2B<
CVBS_PBOUT	17.3F> 17.3F> 21.4A<
CVBS_YOUT	17.3F> 17.3F> 21.4A<
DACA_BLUE_C	16.3H> 16.3H> 19.4G<
DACA_GREEN_C	16.3H> 16.3H> 19.4G<
DACA_HSYNC_C	16.3H> 16.3H> 19.4G<
DACA_RED_C	16.3H> 16.3H> 19.4G<
DACA_RGB_GND	16.3H<> 16.3H<> 19.4G<
DACA_VSYNC_C	16.3H> 16.3H> 19.3G<
DACB_BLUE_C	17.3G> 17.3G> 20.4G<
DACB_GREEN_C	17.3G> 17.3G> 20.4G<
DACB_HSYNC_C	17.3G> 20.4G<
DACB_RED_C	17.3G> 17.3G> 20.4G<
DACB_RGB_GND	17.3G> 17.3G> 17.3G> 17.3G> 20.4G<
DACB_VSYNC_C	17.3G> 20.3G<
DVIA_HPD	19.4F<> 25.2A<
DVIB_HPD	20.4F<> 25.2A<
DVO_A_CLKOUT	18.2E> 19.2A< 19.2E
DVO_A_CLKOUT*	18.2E> 19.2A< 19.3E
DVO_A_CTL3	18.3E> 19.3A<
DVO_A_D<0>	15.1A 18.1E 19.4B
DVO_A_D<23..0>	15.1A<> 18.2F<> 19.2A< 19.2E
DVO_A_D<1>	15.1A 18.1E 19.4B
DVO_A_D<2>	15.1A 18.1E 19.4B
DVO_A_D<3>	15.1A 18.1E 19.4B
DVO_A_D<4>	15.1A 18.2E 19.4B
DVO_A_D<5>	15.1A 18.2E 19.4B
DVO_A_D<6>	15.1A 18.2E 19.4B
DVO_A_D<7>	15.1A 18.2E 19.4B
DVO_A_D<8>	15.1A 18.2E 19.4B
DVO_A_D<9>	15.1A 18.2E 19.4B
DVO_A_D<10>	15.1A 18.2E 19.4B
DVO_A_D<11>	15.1A 18.2E 19.4B
DVO_A_D<12>	15.1A 15.2B 18.2E 19.2B
DVO_A_D<13>	15.1A 15.2B 18.2E 19.2B
DVO_A_D<14>	15.2A 15.2B 18.2E 19.2B
DVO_A_D<15>	15.2A 15.2B 18.2E 19.2B
DVO_A_D<16>	15.2A 15.2B 18.2E 19.2B
DVO_A_D<17>	15.2A 15.2B 18.2E 19.2B
DVO_A_D<18>	15.2A 18.2E 19.2B
DVO_A_D<19>	15.2A 18.2E 19.2B
DVO_A_D<20>	15.2A 18.2E 19.2B
DVO_A_D<21>	15.2A 15.3F 18.2E 19.2B
DVO_A_D<22>	15.2A 15.3F 18.2E 19.2B
DVO_A_D<23>	15.2A 15.3F 18.2E 19.2B
DVO_A_DE	18.2E> 19.2A< 19.2E
DVO_A_HSYNC	18.2E> 19.2E 19.4A<
DVO_A_VSYNC	18.3E> 19.2A< 19.2E
DVO_B_D<12>	15.2C 15.3B 18.4F 22.3C
DVO_B_D<23..12>	15.1B<> 18.4F< 22.3B>
DVO_B_D<13>	15.2C 15.3B 18.4F 22.3C
DVO_B_D<14>	15.2C 15.3B 18.4F 22.3C
DVO_B_D<15>	15.2C 15.4B 18.4F 22.3C
DVO_B_D<16>	15.2C 18.4F 22.3C
DVO_B_D<17>	15.2C 18.4F 22.3C
DVO_B_D<18>	15.2C 18.4F 22.3C
DVO_B_D<19>	15.2C 15.3B 18.4F 22.3C
DVO_B_D<20>	15.2C 15.3B 18.4F
DVO_B_D<21>	15.2C
DVO_B_D<22>	15.2C 15.4B 18.4F 22.4C
DVO_B_D<23>	15.2C 15.4B 18.4F
FAN_PWM	25.1G<> 25.2B 25.4F
FAN_PWM_B	25.1G<> 25.4G
FAN_PWM_C	25.1G<> 25.4H
FB_A0_CLK0	3.4A> 5.2A< 13.1A<>
FB_A0_CLK0*	3.4A> 5.2A< 13.1A<>
FB_A0_CLK1	3.4A> 5.2C< 13.1A<>
FB_A0_CLK1*	3.4A> 5.2C< 13.1A<>
FB_A0_CMD<0>	3.3A 5.2A 5.2D
FB_A0_CMD<19..0>	3.3A> 13.2A<>
FB_A0_CMD<21..0>	5.1A<
FB_A0_CMD<1>	3.3A 5.2A 5.2D
FB_A0_CMD<2>	3.3A 5.2A 5.2D
FB_A0_CMD<3>	3.3A 5.2A 5.2D
FB_A0_CMD<4>	3.3A 5.2A 5.2D
FB_A0_CMD<5>	3.3A 5.2A 5.2D
FB_A0_CMD<6>	3.3A 5.2A
FB_A0_CMD<7>	3.3A 5.2A 5.2D
FB_A0_CMD<8>	3.3A 5.2A 5.2D
FB_A0_CMD<9>	3.3A 5.1A 5.1D
FB_A0_CMD<10>	3.3A 5.2A 5.2D
FB_A0_CMD<11>	3.3A 5.1A 5.1D
FB_A0_CMD<12>	3.3A 5.2A 5.2D
FB_A0_CMD<13>	3.3A 5.2D
FB_A0_CMD<14>	3.3A 5.2A 5.2D
FB_A0_CMD<15>	3.3A 5.2A 5.2D
FB_A0_CMD<16>	3.3A 5.2A 5.2D
FB_A0_CMD<17>	3.3A 5.2A 5.2D
FB_A0_CMD<18>	3.3A 5.2A 5.2D
FB_A0_CMD<19>	3.3A 5.2A 5.2D
FB_A0_RESET	3.4A> 5.3A< 5.3C< 13.3A<>
FB_A0_VREF1	13.4A<>
FB_A0_VREF2	13.4A<>
FB_A0_ZQ	13.4A<>
FB_A1_CLK0	3.4C> 6.2A< 13.1A<>
FB_A1_CLK0*	3.4C> 6.2A< 13.1A<>
FB_A1_CLK1	3.4C> 6.2C< 13.1A<>
FB_A1_CLK1*	3.4C> 6.2C< 13.1A<>
FB_A1_CMD<0>	3.3C 6.2A 6.2D
FB_A1_CMD<19..0>	3.3C> 13.3A<>
FB_A1_CMD<21..0>	6.1A<
FB_A1_CMD<1>	3.3C 6.2A 6.2D
FB_A1_CMD<2>	3.3C 6.2A 6.2D
FB_A1_CMD<3>	3.3C 6.2A 6.2D
FB_A1_CMD<4>	3.3C 6.2A 6.2D
FB_A1_CMD<5>	3.3C 6.2A 6.2D
FB_A1_CMD<6>	3.3C 6.2A
FB_A1_CMD<7>	3.3C 6.2A 6.2D
FB_A1_CMD<8>	3.3C 6.2A 6.2D
FB_A1_CMD<9>	3.3C 6.1A 6.1D
FB_A1_CMD<10>	3.3C 6.2A 6.2D
FB_A1_CMD<11>	3.3C 6.1A 6.1D
FB_A1_CMD<12>	3.3C 6.2A 6.2D
FB_A1_CMD<13>	3.3C 6.2D
FB_A1_CMD<14>	3.3C 6.2A 6.2D
FB_A1_CMD<15>	3.3C 6.2A 6.2D
FB_A1_CMD<16>	3.3C 6.2A 6.2D
FB_A1_CMD<17>	3.3C 6.2A 6.2D
FB_A1_CMD<18>	3.3C 6.2A 6.2D
FB_A1_CMD<19>	3.3C 6.2A 6.2D
FB_A1_RESET	3.4C> 6.3A< 6.3C< 13.3A<>
FB_A1_VREF1	13.4A<>
FB_A1_VREF2	13.4A<>
FB_A1_ZQ	13.4A<>
FB_A_AVDD	3.4D<> 13.4A<>
FB_A_DQ<0>	3.1A
FB_A_DQ<63..0>	3.1A<> 3.1C<> 13.2A<>
FB_A_DQ<64..0>	5.4A<> 6.4A<>
FB_A_DQ<1>	3.1A
FB_A_DQ<2>	3.1A
FB_A_DQ<3>	3.1A
FB_A_DQ<4>	3.1A
FB_A_DQ<5>	3.1A
FB_A_DQ<6>	3.1A
FB_A_DQ<7>	3.1A
FB_A_DQ<8>	3.1A
FB_A_DQ<9>	3.1A
FB_A_DQ<10>	3.1A
FB_A_DQ<11>	3.1A
FB_A_DQ<12>	3.1A
FB_A_DQ<13>	3.2A
FB_A_DQ<14>	3.2A
FB_A_DQ<15>	3.2A
FB_A_DQ<16>	3.2A
FB_A_DQ<17>	3.2A
FB_A_DQ<18>	3.2A
FB_A_DQ<19>	3.2A
FB_A_DQ<20>	3.2A
FB_A_DQ<21>	3.2A
FB_A_DQ<22>	3.2A
FB_A_DQ<23>	3.2A
FB_A_DQ<24>	3.2A
FB_A_DQ<25>	3.2A
FB_A_DQ<26>	3.2A
FB_A_DQ<27>	3.2A
FB_A_DQ<28>	3.2A
FB_A_DQ<29>	3.2A
FB_A_DQ<30>	3.2A
FB_A_DQ<31>	3.2A
FB_A_DQ<32>	3.1C
FB_A_DQ<33>	3.1C
FB_A_DQ<34>	3.1C
FB_A_DQ<35>	3.1C
FB_A_DQ<36>	3.1C
FB_A_DQ<37>	3.1C
FB_A_DQ<38>	3.1C
FB_A_DQ<39>	3.1C
FB_A_DQ<40>	3.1C
FB_A_DQ<41>	3.1C
FB_A_DQ<42>	3.1C
FB_A_DQ<43>	3.1C
FB_A_DQ<44>	3.1C
FB_A_DQ<45>	3.2C
FB_A_DQ<46>	3.2C
FB_A_DQ<47>	3.2C
FB_A_DQ<48>	3.2C
FB_A_DQ<49>	3.2C
FB_A_DQ<50>	3.2C
FB_A_DQ<51>	3.2C
FB_A_DQ<52>	3.2C
FB_A_DQ<53>	3.2C
FB_A_DQ<54>	3.2C
FB_A_DQ<55>	3.2C
FB_A_DQ<56>	3.2C
FB_A_DQ<57>	3.2C
FB_A_DQ<58>	3.2C
FB_A_DQ<59>	3.2C
FB_A_DQ<60>	3.2C
FB_A_DQ<61>	3.2C
FB_A_DQ<62>	3.2C
FB_A_DQ<63>	3.2C
FB_A_DQM<0>	3.2A
FB_A_DQM<7..0>	3.2A> 3.2C> 5.4A< 6.4A< 13.2A<>
FB_A_DQM<1>	3.2A
FB_A_DQM<2>	3.2A
FB_A_DQM<3>	3.2A
FB_A_DQM<4>	3.2C
FB_A_DQM<5>	3.2C
FB_A_DQM<6>	3.2C
FB_A_DQM<7>	3.2C
FB_A_DQS_RN<0>	3.2A
FB_A_DQS_RN<7..0>	3.2A<> 3.2C<> 5.4A> 6.4A> 13.2A<>
FB_A_DQS_RN<1>	3.2A
FB_A_DQS_RN<2>	3.2A
FB_A_DQS_RN<3>	3.3A
FB_A_DQS_RN<4>	3.2C
FB_A_DQS_RN<5>	3.2C
FB_A_DQS_RN<6>	3.2C
FB_A_DQS_RN<7>	3.3C
FB_A_DQS_WP<0>	3.3A
FB_A_DQS_WP<7..0>	3.3A<> 3.3C<> 5.4A< 6.4A< 13.2A<>
FB_A_DQS_WP<1>	3.3A
FB_A_DQS_WP<2>	3.3A
FB_A_DQS_WP<3>	3.3A
FB_A_DQS_WP<4>	3.3C
FB_A_DQS_WP<5>	3.3C
FB_A_DQS_WP<6>	3.3C
FB_A_DQS_WP<7>	3.3C
FB_A_PLLVDD	3.4D<> 13.4A<>
FB_B0_CLK0	3.4E> 7.2A< 13.1A<>
FB_B0_CLK0*	3.4E> 7.2A< 13.1A<>
FB_B0_CLK1	3.4E> 7.2C< 13.2A<>
FB_B0_CLK1*	3.4E> 7.2C< 13.2A<>
FB_B0_CMD<0>	3.3E 7.2A 7.2D
FB_B0_CMD<19..0>	3.3E> 13.3A<>
FB_B0_CMD<21..0>	7.1A<
FB_B0_CMD<1>	3.3E 7.2A 7.2D
FB_B0_CMD<2>	3.3E 7.2A 7.2D
FB_B0_CMD<3>	3.3E 7.2A 7.2D
FB_B0_CMD<4>	3.3E 7.2A 7.2D
FB_B0_CMD<5>	3.3E 7.2A 7.2D
FB_B0_CMD<6>	3.3E 7.2A
FB_B0_CMD<7>	3.3E 7.2A 7.2D
FB_B0_CMD<8>	3.3E 7.2A 7.2D
FB_B0_CMD<9>	3.3E 7.1A 7.1D
FB_B0_CMD<10>	3.3E 7.2A 7.2D
FB_B0_CMD<11>	3.3E 7.1A 7.1D
FB_B0_CMD<12>	3.3E 7.2A 7.2D
FB_B0_CMD<13>	3.3E 7.2D
FB_B0_CMD<14>	3.3E 7.2A 7.2D
FB_B0_CMD<15>	3.3E 7.2A 7.2D
FB_B0_CMD<16>	3.3E 7.2A 7.2D
FB_B0_CMD<17>	3.3E 7.2A 7.2D
FB_B0_CMD<18>	3.3E 7.2A 7.2D
FB_B0_CMD<19>	3.3E 7.2A 7.2D
FB_B0_RESET	3.4E> 7.3A< 7.3C< 13.3A<>
FB_B0_VREF1	13.4A<>
FB_B0_VREF2	13.4A<>
FB_B0_ZQ	13.4A<>
FB_B1_CLK0	3.4G> 8.2A< 13.2A<>
FB_B1_CLK0*	3.4G> 8.2A< 13.2A<>
FB_B1_CLK1	3.4G> 8.2C< 13.2A<>
FB_B1_CLK1*	3.4G> 8.2C< 13.2A<>
FB_B1_CMD<0>	3.3G 8.2A 8.2D
FB_B1_CMD<19..0>	3.3G> 13.3A<>
FB_B1_CMD<21..0>	8.1A<
FB_B1_CMD<1>	3.3G 8.2A 8.2D
FB_B1_CMD<2>	3.3G 8.2A 8.2D
FB_B1_CMD<3>	3.3G 8.2A 8.2D
FB_B1_CMD<4>	3.3G 8.2A 8.2D
FB_B1_CMD<5>	3.3G 8.2A 8.2D
FB_B1_CMD<6>	3.3G 8.2A
FB_B1_CMD<7>	3.3G 8.2A 8.2D
FB_B1_CMD<8>	3.3G 8.2A 8.2D
FB_B1_CMD<9>	3.3G 8.1A 8.1D
FB_B1_CMD<10>	3.3G 8.2A 8.2D
FB_B1_CMD<11>	3.3G 8.1A 8.1D
FB_B1_CMD<12>	3.3G 8.2A 8.2D
FB_B1_CMD<13>	3.3G 8.2D
FB_B1_CMD<14>	3.3G 8.2A 8.2D
FB_B1_CMD<15>	3.3G 8.2A 8.2D
FB_B1_CMD<16>	3.3G 8.2A 8.2D
FB_B1_CMD<17>	3.3G 8.2A 8.2D
FB_B1_CMD<18>	3.3G 8.2A 8.2D
FB_B1_CMD<19>	3.3G 8.2A 8.2D
FB_B1_RESET	3.4G> 8.3A< 8.3C< 13.3A<>
FB_B1_VREF1	13.4A<>
FB_B1_VREF2	13.4A<>
FB_B1_ZQ	13.4A<>
FB_B_AVDD	3.4H<> 13.4A<>
FB_B_DQ<0>	3.1E
FB_B_DQ<63..0>	3.1E<> 3.1G<> 13.2A<>
FB_B_DQ<64..0>	7.4A<> 8.4A<>
FB_B_DQ<1>	3.1E
FB_B_DQ<2>	3.1E
FB_B_DQ<3>	3.1E
FB_B_DQ<4>	3.1E
FB_B_DQ<5>	3.1E
FB_B_DQ<6>	3.1E
FB_B_DQ<7>	3.1E
FB_B_DQ<8>	3.1E
FB_B_DQ<9>	3.1E
FB_B_DQ<10>	3.1E
FB_B_DQ<11>	3.1E
FB_B_DQ<12>	3.2E
FB_B_DQ<13>	3.2E
FB_B_DQ<14>	3.2E
FB_B_DQ<15>	3.2E
FB_B_DQ<16>	3.2E
FB_B_DQ<17>	3.2E
FB_B_DQ<18>	3.2E
FB_B_DQ<19>	3.2E
FB_B_DQ<20>	3.2E
FB_B_DQ<21>	3.2E
FB_B_DQ<22>	3.2E
FB_B_DQ<23>	3.2E
FB_B_DQ<24>	3.2E
FB_B_DQ<25>	3.2E
FB_B_DQ<26>	3.2E
FB_B_DQ<27>	3.2E
FB_B_DQ<28>	3.2E
FB_B_DQ<29>	3.2E
FB_B_DQ<30>	3.2E
FB_B_DQ<31>	3.2E
FB_B_DQ<32>	3.1G
FB_B_DQ<33>	3.1G
FB_B_DQ<34>	3.1G
FB_B_DQ<35>	3.1G
FB_B_DQ<36>	3.1G
FB_B_DQ<37>	3.1G
FB_B_DQ<38>	3.1G
FB_B_DQ<39>	3.1G
FB_B_DQ<40>	3.1G
FB_B_DQ<41>	3.1G
FB_B_DQ<42>	3.1G
FB_B_DQ<43>	3.1G
FB_B_DQ<44>	3.2G
FB_B_DQ<45>	3.2G
FB_B_DQ<46>	3.2G
FB_B_DQ<47>	3.2G
FB_B_DQ<48>	3.2G
FB_B_DQ<49>	3.2G
FB_B_DQ<50>	3.2G
FB_B_DQ<51>	3.2G
FB_B_DQ<52>	3.2G
FB_B_DQ<53>	3.2G
FB_B_DQ<54>	3.2G
FB_B_DQ<55>	3.2G
FB_B_DQ<56>	3.2G
FB_B_DQ<57>	3.2G
FB_B_DQ<58>	3.2G
FB_B_DQ<59>	3.2G
FB_B_DQ<60>	3.2G
FB_B_DQ<61>	3.2G
FB_B_DQ<62>	3.2G
FB_B_DQ<63>	3.2G
FB_B_DQM<0>	3.2E
FB_B_DQM<7..0>	3.2E> 3.2G> 7.4A< 8.4A< 13.2A<>
FB_B_DQM<1>	3.2E
FB_B_DQM<2>	3.2E
FB_B_DQM<3>	3.2E
FB_B_DQM<4>	3.2G
FB_B_DQM<5>	3.2G
FB_B_DQM<6>	3.2G
FB_B_DQM<7>	3.2G
FB_B_DQS_RN<0>	3.2E
FB_B_DQS_RN<7..0>	3.2E<> 3.2G<> 7.4A> 8.4A> 13.2A<>
FB_B_DQS_RN<1>	3.2E
FB_B_DQS_RN<2>	3.3E
FB_B_DQS_RN<3>	3.3E
FB_B_DQS_RN<4>	3.2G
FB_B_DQS_RN<5>	3.2G
FB_B_DQS_RN<6>	3.3G
FB_B_DQS_RN<7>	3.3G
FB_B_DQS_WP<0>	3.3E
FB_B_DQS_WP<7..0>	3.3E<> 3.3G<> 7.4A< 8.4A< 13.2A<>
FB_B_DQS_WP<1>	3.3E
FB_B_DQS_WP<2>	3.3E
FB_B_DQS_WP<3>	3.3E
FB_B_DQS_WP<4>	3.3G
FB_B_DQS_WP<5>	3.3G
FB_B_DQS_WP<6>	3.3G
FB_B_DQS_WP<7>	3.3G
FB_B_PLLVDD	3.4H<> 13.4A<>
FB_C0_CLK0	4.4A> 9.2A< 13.1C<>
FB_C0_CLK0*	4.4A> 9.2A< 13.1C<>
FB_C0_CLK1	4.4A> 9.2C< 13.1C<>
FB_C0_CLK1*	4.4A> 9.2C< 13.1C<>
FB_C0_CMD<0>	4.3A 9.2A 9.2D
FB_C0_CMD<19..0>	4.3A> 13.2C<>
FB_C0_CMD<21..0>	9.1A<
FB_C0_CMD<1>	4.3A 9.2A 9.2D
FB_C0_CMD<2>	4.3A 9.2A 9.2D
FB_C0_CMD<3>	4.3A 9.2A 9.2D
FB_C0_CMD<4>	4.3A 9.2A 9.2D
FB_C0_CMD<5>	4.3A 9.2A 9.2D
FB_C0_CMD<6>	4.3A 9.2A
FB_C0_CMD<7>	4.3A 9.2A 9.2D
FB_C0_CMD<8>	4.3A 9.2A 9.2D
FB_C0_CMD<9>	4.3A 9.1A 9.1D
FB_C0_CMD<10>	4.3A 9.2A 9.2D
FB_C0_CMD<11>	4.3A 9.1A 9.1D
FB_C0_CMD<12>	4.3A 9.2A 9.2D
FB_C0_CMD<13>	4.3A 9.2D
FB_C0_CMD<14>	4.3A 9.2A 9.2D
FB_C0_CMD<15>	4.3A 9.2A 9.2D
FB_C0_CMD<16>	4.3A 9.2A 9.2D
FB_C0_CMD<17>	4.3A 9.2A 9.2D
FB_C0_CMD<18>	4.3A 9.2A 9.2D
FB_C0_CMD<19>	4.3A 9.2A 9.2D
FB_C0_RESET	4.4A> 9.3A< 9.3C< 13.3C<>
FB_C0_VREF1	13.4C<>
FB_C0_VREF2	13.4C<>
FB_C0_ZQ	13.4C<>
FB_C1_CLK0	4.4C> 10.2A< 13.1C<>
FB_C1_CLK0*	4.4C> 10.2A< 13.1C<>
FB_C1_CLK1	4.4C> 10.2C< 13.1C<>
FB_C1_CLK1*	4.4C> 10.2C< 13.1C<>
FB_C1_CMD<0>	4.3C 10.2A 10.2D
FB_C1_CMD<19..0>	4.3C> 13.3C<>
FB_C1_CMD<21..0>	10.1A<
FB_C1_CMD<1>	4.3C 10.2A 10.2D
FB_C1_CMD<2>	4.3C 10.2A 10.2D
FB_C1_CMD<3>	4.3C 10.2A 10.2D
FB_C1_CMD<4>	4.3C 10.2A 10.2D
FB_C1_CMD<5>	4.3C 10.2A 10.2D
FB_C1_CMD<6>	4.3C 10.2A
FB_C1_CMD<7>	4.3C 10.2A 10.2D
FB_C1_CMD<8>	4.3C 10.2A 10.2D
FB_C1_CMD<9>	4.3C 10.1A 10.1D
FB_C1_CMD<10>	4.3C 10.2A 10.2D
FB_C1_CMD<11>	4.3C 10.1A 10.1D
FB_C1_CMD<12>	4.3C 10.2A 10.2D
FB_C1_CMD<13>	4.3C 10.2D
FB_C1_CMD<14>	4.3C 10.2A 10.2D
FB_C1_CMD<15>	4.3C 10.2A 10.2D
FB_C1_CMD<16>	4.3C 10.2A 10.2D
FB_C1_CMD<17>	4.3C 10.2A 10.2D
FB_C1_CMD<18>	4.3C 10.2A 10.2D
FB_C1_CMD<19>	4.3C 10.2A 10.2D
FB_C1_RESET	4.4C> 10.3A< 10.3C< 13.3C<>
FB_C1_VREF1	13.4C<>
FB_C1_VREF2	13.4C<>
FB_C1_ZQ	13.4C<>
FB_CAL0_PD_VDDQ	13.1E 13.3F<>
FB_CAL0_PU_GND	13.1E 13.3F<>
FB_CAL0_TERM_GND	13.1E 13.3F<>
FB_CAL1_PD_VDDQ	13.1G 13.3F<>
FB_CAL1_PU_GND	13.1G 13.3F<>
FB_CAL1_TERM_GND	13.1G 13.3F<>
FB_C_AVDD	4.4D<> 13.4C<>
FB_C_DQ<0>	4.1A
FB_C_DQ<63..0>	4.1A<> 4.1D<> 13.2C<>
FB_C_DQ<64..0>	9.4A<> 10.4A<>
FB_C_DQ<1>	4.1A
FB_C_DQ<2>	4.1A
FB_C_DQ<3>	4.1A
FB_C_DQ<4>	4.1A
FB_C_DQ<5>	4.1A
FB_C_DQ<6>	4.1A
FB_C_DQ<7>	4.1A
FB_C_DQ<8>	4.1A
FB_C_DQ<9>	4.1A
FB_C_DQ<10>	4.1A
FB_C_DQ<11>	4.1A
FB_C_DQ<12>	4.1A
FB_C_DQ<13>	4.2A
FB_C_DQ<14>	4.2A
FB_C_DQ<15>	4.2A
FB_C_DQ<16>	4.2A
FB_C_DQ<17>	4.2A
FB_C_DQ<18>	4.2A
FB_C_DQ<19>	4.2A
FB_C_DQ<20>	4.2A
FB_C_DQ<21>	4.2A
FB_C_DQ<22>	4.2A
FB_C_DQ<23>	4.2A
FB_C_DQ<24>	4.2A
FB_C_DQ<25>	4.2A
FB_C_DQ<26>	4.2A
FB_C_DQ<27>	4.2A
FB_C_DQ<28>	4.2A
FB_C_DQ<29>	4.2A
FB_C_DQ<30>	4.2A
FB_C_DQ<31>	4.2A
FB_C_DQ<32>	4.1C
FB_C_DQ<33>	4.1C
FB_C_DQ<34>	4.1C
FB_C_DQ<35>	4.1C
FB_C_DQ<36>	4.1C
FB_C_DQ<37>	4.1C
FB_C_DQ<38>	4.1C
FB_C_DQ<39>	4.1C
FB_C_DQ<40>	4.1C
FB_C_DQ<41>	4.1C
FB_C_DQ<42>	4.1C
FB_C_DQ<43>	4.1C
FB_C_DQ<44>	4.1C
FB_C_DQ<45>	4.2C
FB_C_DQ<46>	4.2C
FB_C_DQ<47>	4.2C
FB_C_DQ<48>	4.2C
FB_C_DQ<49>	4.2C
FB_C_DQ<50>	4.2C
FB_C_DQ<51>	4.2C
FB_C_DQ<52>	4.2C
FB_C_DQ<53>	4.2C
FB_C_DQ<54>	4.2C
FB_C_DQ<55>	4.2C
FB_C_DQ<56>	4.2C
FB_C_DQ<57>	4.2C
FB_C_DQ<58>	4.2C
FB_C_DQ<59>	4.2C
FB_C_DQ<60>	4.2C
FB_C_DQ<61>	4.2C
FB_C_DQ<62>	4.2C
FB_C_DQ<63>	4.2C
FB_C_DQM<0>	4.2A
FB_C_DQM<7..0>	4.2A> 4.2C> 9.4A< 10.4A< 13.2C<>
FB_C_DQM<1>	4.2A
FB_C_DQM<2>	4.2A
FB_C_DQM<3>	4.2A
FB_C_DQM<4>	4.2C
FB_C_DQM<5>	4.2C
FB_C_DQM<6>	4.2C
FB_C_DQM<7>	4.2C
FB_C_DQS_RN<0>	4.2A
FB_C_DQS_RN<7..0>	4.2A<> 4.2D<> 9.4A> 10.4A> 13.2C<>
FB_C_DQS_RN<1>	4.2A
FB_C_DQS_RN<2>	4.2A
FB_C_DQS_RN<3>	4.3A
FB_C_DQS_RN<4>	4.2C
FB_C_DQS_RN<5>	4.2C
FB_C_DQS_RN<6>	4.2C
FB_C_DQS_RN<7>	4.3C
FB_C_DQS_WP<0>	4.3A
FB_C_DQS_WP<7..0>	4.3A<> 4.3D<> 9.4A< 10.4A< 13.2C<>
FB_C_DQS_WP<1>	4.3A
FB_C_DQS_WP<2>	4.3A
FB_C_DQS_WP<3>	4.3A
FB_C_DQS_WP<4>	4.3C
FB_C_DQS_WP<5>	4.3C
FB_C_DQS_WP<6>	4.3C
FB_C_DQS_WP<7>	4.3C
FB_C_PLLVDD	4.4D<> 13.4C<>
FB_D0_CLK0	4.4E> 11.2A< 13.1C<>
FB_D0_CLK0*	4.4E> 11.2A< 13.1C<>
FB_D0_CLK1	4.4E> 11.2C< 13.2C<>
FB_D0_CLK1*	4.4E> 11.2C< 13.2C<>
FB_D0_CMD<0>	4.3E 11.2A 11.2D
FB_D0_CMD<19..0>	4.3E> 13.3C<>
FB_D0_CMD<21..0>	11.1A<
FB_D0_CMD<1>	4.3E 11.2A 11.2D
FB_D0_CMD<2>	4.3E 11.2A 11.2D
FB_D0_CMD<3>	4.3E 11.2A 11.2D
FB_D0_CMD<4>	4.3E 11.2A 11.2D
FB_D0_CMD<5>	4.3E 11.2A 11.2D
FB_D0_CMD<6>	4.3E 11.2A
FB_D0_CMD<7>	4.3E 11.2A 11.2D
FB_D0_CMD<8>	4.3E 11.2A 11.2D
FB_D0_CMD<9>	4.3E 11.1A 11.1D
FB_D0_CMD<10>	4.3E 11.2A 11.2D
FB_D0_CMD<11>	4.3E 11.1A 11.1D
FB_D0_CMD<12>	4.3E 11.2A 11.2D
FB_D0_CMD<13>	4.3E 11.2D
FB_D0_CMD<14>	4.3E 11.2A 11.2D
FB_D0_CMD<15>	4.3E 11.2A 11.2D
FB_D0_CMD<16>	4.3E 11.2A 11.2D
FB_D0_CMD<17>	4.3E 11.2A 11.2D
FB_D0_CMD<18>	4.3E 11.2A 11.2D
FB_D0_CMD<19>	4.3E 11.2A 11.2D
FB_D0_RESET	4.4E> 11.3A< 11.3C< 13.3C<>
FB_D0_VREF1	13.4C<>
FB_D0_VREF2	13.4C<>
FB_D0_ZQ	13.4C<>
FB_D1_CLK0	4.4G> 12.2A< 13.2C<>
FB_D1_CLK0*	4.4G> 12.2A< 13.2C<>
FB_D1_CLK1	4.4G> 12.2C< 13.2C<>
FB_D1_CLK1*	4.4G> 12.2C< 13.2C<>
FB_D1_CMD<0>	4.3F 12.2A 12.2D
FB_D1_CMD<19..0>	4.3G> 13.3C<>
FB_D1_CMD<21..0>	12.1A<
FB_D1_CMD<1>	4.3F 12.2A 12.2D
FB_D1_CMD<2>	4.3F 12.2A 12.2D
FB_D1_CMD<3>	4.3F 12.2A 12.2D
FB_D1_CMD<4>	4.3F 12.2A 12.2D
FB_D1_CMD<5>	4.3F 12.2A 12.2D
FB_D1_CMD<6>	4.3F 12.2A
FB_D1_CMD<7>	4.3F 12.2A 12.2D
FB_D1_CMD<8>	4.3F 12.2A 12.2D
FB_D1_CMD<9>	4.3F 12.1A 12.1D
FB_D1_CMD<10>	4.3F 12.2A 12.2D
FB_D1_CMD<11>	4.3F 12.1A 12.1D
FB_D1_CMD<12>	4.3F 12.2A 12.2D
FB_D1_CMD<13>	4.3F 12.2D
FB_D1_CMD<14>	4.3F 12.2A 12.2D
FB_D1_CMD<15>	4.3F 12.2A 12.2D
FB_D1_CMD<16>	4.3F 12.2A 12.2D
FB_D1_CMD<17>	4.3F 12.2A 12.2D
FB_D1_CMD<18>	4.3F 12.2A 12.2D
FB_D1_CMD<19>	4.3F 12.2A 12.2D
FB_D1_RESET	4.4G> 12.3A< 12.3C< 13.3C<>
FB_D1_VREF1	13.4C<>
FB_D1_VREF2	13.4C<>
FB_D1_ZQ	13.4C<>
FB_D_AVDD	4.4H<> 13.4C<>
FB_D_DQ<0>	4.1E
FB_D_DQ<63..0>	4.1E<> 4.1G<> 13.2C<>
FB_D_DQ<64..0>	11.4A<> 12.4A<>
FB_D_DQ<1>	4.1E
FB_D_DQ<2>	4.1E
FB_D_DQ<3>	4.1E
FB_D_DQ<4>	4.1E
FB_D_DQ<5>	4.1E
FB_D_DQ<6>	4.1E
FB_D_DQ<7>	4.1E
FB_D_DQ<8>	4.1E
FB_D_DQ<9>	4.1E
FB_D_DQ<10>	4.1E
FB_D_DQ<11>	4.1E
FB_D_DQ<12>	4.1E
FB_D_DQ<13>	4.2E
FB_D_DQ<14>	4.2E
FB_D_DQ<15>	4.2E
FB_D_DQ<16>	4.2E
FB_D_DQ<17>	4.2E
FB_D_DQ<18>	4.2E
FB_D_DQ<19>	4.2E
FB_D_DQ<20>	4.2E
FB_D_DQ<21>	4.2E
FB_D_DQ<22>	4.2E
FB_D_DQ<23>	4.2E
FB_D_DQ<24>	4.2E
FB_D_DQ<25>	4.2E
FB_D_DQ<26>	4.2E
FB_D_DQ<27>	4.2E
FB_D_DQ<28>	4.2E
FB_D_DQ<29>	4.2E
FB_D_DQ<30>	4.2E
FB_D_DQ<31>	4.2E
FB_D_DQ<32>	4.1F
FB_D_DQ<33>	4.1F
FB_D_DQ<34>	4.1F
FB_D_DQ<35>	4.1F
FB_D_DQ<36>	4.1F
FB_D_DQ<37>	4.1F
FB_D_DQ<38>	4.1F
FB_D_DQ<39>	4.1F
FB_D_DQ<40>	4.1F
FB_D_DQ<41>	4.1F
FB_D_DQ<42>	4.1F
FB_D_DQ<43>	4.1F
FB_D_DQ<44>	4.1F
FB_D_DQ<45>	4.2F
FB_D_DQ<46>	4.2F
FB_D_DQ<47>	4.2F
FB_D_DQ<48>	4.2F
FB_D_DQ<49>	4.2F
FB_D_DQ<50>	4.2F
FB_D_DQ<51>	4.2F
FB_D_DQ<52>	4.2F
FB_D_DQ<53>	4.2F
FB_D_DQ<54>	4.2F
FB_D_DQ<55>	4.2F
FB_D_DQ<56>	4.2F
FB_D_DQ<57>	4.2F
FB_D_DQ<58>	4.2F
FB_D_DQ<59>	4.2F
FB_D_DQ<60>	4.2F
FB_D_DQ<61>	4.2F
FB_D_DQ<62>	4.2F
FB_D_DQ<63>	4.2F
FB_D_DQM<0>	4.2E
FB_D_DQM<7..0>	4.2E> 4.2G> 11.4A< 12.4A< 13.2C<>
FB_D_DQM<1>	4.2E
FB_D_DQM<2>	4.2E
FB_D_DQM<3>	4.2E
FB_D_DQM<4>	4.2F
FB_D_DQM<5>	4.2F
FB_D_DQM<6>	4.2F
FB_D_DQM<7>	4.2F
FB_D_DQS_RN<0>	4.2E
FB_D_DQS_RN<7..0>	4.2E<> 4.2G<> 11.4A> 12.4A> 13.2C<>
FB_D_DQS_RN<1>	4.2E
FB_D_DQS_RN<2>	4.2E
FB_D_DQS_RN<3>	4.3E
FB_D_DQS_RN<4>	4.2F
FB_D_DQS_RN<5>	4.2F
FB_D_DQS_RN<6>	4.2F
FB_D_DQS_RN<7>	4.3F
FB_D_DQS_WP<0>	4.3E
FB_D_DQS_WP<7..0>	4.3E<> 4.3G<> 11.4A< 12.4A< 13.2C<>
FB_D_DQS_WP<1>	4.3E
FB_D_DQS_WP<2>	4.3E
FB_D_DQS_WP<3>	4.3E
FB_D_DQS_WP<4>	4.3F
FB_D_DQS_WP<5>	4.3F
FB_D_DQS_WP<6>	4.3F
FB_D_DQS_WP<7>	4.3F
FB_D_PLLVDD	4.4H<> 13.4C<>
FB_VREF1	13.2E 13.4F<>
FB_VREF2	13.2G 13.4F<>
GPIO3_HIGH_PWR	25.2C< 26.4A>
GPIO4_VTG_RST	21.1F> 25.3C<
GPIO9_FRAMELOCK	21.1H<> 25.3C<>
GPIO_SLOW*	25.2H> 25.3C>
GPU_REFCLK	2.2D< 14.4H>
GPU_REFCLK*	2.2D< 14.4H>
I2CA_SCL	16.1D> 19.2A< 19.3E
I2CA_SCL_C	16.3H> 16.3H> 19.3G<
I2CA_SDA	16.1E<> 19.2A<> 19.3E
I2CA_SDA_C	16.3H> 16.3H> 19.3G<
I2CB_SCL_C	17.3G> 20.3G<
I2CB_SDA_C	17.3G> 20.3G<
I2CC_SCL	21.1F< 21.3G< 22.3B< 25.2F>
I2CC_SDA	21.1F<> 21.3G<> 22.3B<> 25.2F<>
LGATE1	28.1H> 28.2D 28.3C
LGATE2	28.1H> 28.3C
LOAD_TEST	17.3A< 25.2C<
NVVDD_SENSE	25.4B> 27.2A<
NVVDD_SENSE*	25.4B> 27.2A<
NVVDD_VID<1>	25.1E 27.4A
NVVDD_VID<4..1>	25.1F> 27.4A<
NVVDD_VID<2>	25.1E 27.4A
NVVDD_VID<3>	25.1E 27.4A
NVVDD_VID<4>	25.2E 27.4A
PEX_REFCLK	2.1H> 2.2C> 14.4C<
PEX_REFCLK*	2.1H> 2.2C> 14.4C<
PEX_RX0	2.2C 2.2H>
PEX_RX0*	2.2C 2.2H>
PEX_RX1	2.2C 2.2H>
PEX_RX1*	2.2C 2.2H>
PEX_RX2	2.2C 2.2H>
PEX_RX2*	2.2C 2.2H>
PEX_RX3	2.2C 2.2H>
PEX_RX3*	2.2C 2.2H>
PEX_RX4	2.2H> 2.3C
PEX_RX4*	2.2H> 2.3C
PEX_RX5	2.2H> 2.3C
PEX_RX5*	2.2H> 2.3C
PEX_RX6	2.2H> 2.3C
PEX_RX6*	2.2H> 2.3C
PEX_RX7	2.2H> 2.3C
PEX_RX7*	2.2H> 2.3C
PEX_RX8	2.3C 2.3H>
PEX_RX8*	2.3C 2.3H>
PEX_RX9	2.3H> 2.4C
PEX_RX9*	2.3H> 2.4C
PEX_RX10	2.3H> 2.4C
PEX_RX10*	2.3H> 2.4C
PEX_RX11	2.3H> 2.4C
PEX_RX11*	2.3H> 2.4C
PEX_RX12	2.3H> 2.4C
PEX_RX12*	2.3H> 2.4C
PEX_RX13	2.3H> 2.4C
PEX_RX13*	2.3H> 2.4C
PEX_RX14	2.3H> 2.5C
PEX_RX14*	2.3H> 2.5C
PEX_RX15	2.3H> 2.5C
PEX_RX15*	2.3H> 2.5C
PEX_TX0	2.2D 2.3H>
PEX_TX0*	2.2D 2.3H>
PEX_TX1	2.2D 2.3H>
PEX_TX1*	2.2D 2.3H>
PEX_TX2	2.2D 2.3H>
PEX_TX2*	2.2D 2.3H>
PEX_TX3	2.2D 2.3H>
PEX_TX3*	2.2D 2.3H>
PEX_TX4	2.2D 2.3H>
PEX_TX4*	2.3D 2.3H>
PEX_TX5	2.3D 2.3H>
PEX_TX5*	2.3D 2.3H>
PEX_TX6	2.3D 2.3H>
PEX_TX6*	2.3D 2.4H>
PEX_TX7	2.3D 2.4H>
PEX_TX7*	2.3D 2.4H>
PEX_TX8	2.3D 2.4H>
PEX_TX8*	2.3D 2.4H>
PEX_TX9	2.3D 2.4H>
PEX_TX9*	2.4D 2.4H>
PEX_TX10	2.4D 2.4H>
PEX_TX10*	2.4D 2.4H>
PEX_TX11	2.4D 2.4H>
PEX_TX11*	2.4D 2.4H>
PEX_TX12	2.4D 2.4H>
PEX_TX12*	2.4D 2.4H>
PEX_TX13	2.4D 2.4H>
PEX_TX13*	2.4D 2.4H>
PEX_TX14	2.4D 2.4H>
PEX_TX14*	2.4H> 2.5D
PEX_TX15	2.4H> 2.5D
PEX_TX15*	2.4H> 2.5D
PEX_TXX0	2.1H> 2.2C
PEX_TXX0*	2.1H> 2.2C
PEX_TXX1	2.1H> 2.2C
PEX_TXX1*	2.1H> 2.2C
PEX_TXX2	2.1H> 2.2C
PEX_TXX2*	2.1H> 2.2C
PEX_TXX3	2.1H> 2.2C
PEX_TXX3*	2.1H> 2.2C
PEX_TXX4	2.1H> 2.2C
PEX_TXX4*	2.1H> 2.3C
PEX_TXX5	2.1H> 2.3C
PEX_TXX5*	2.1H> 2.3C
PEX_TXX6	2.1H> 2.3C
PEX_TXX6*	2.1H> 2.3C
PEX_TXX7	2.1H> 2.3C
PEX_TXX7*	2.1H> 2.3C
PEX_TXX8	2.1H> 2.3C
PEX_TXX8*	2.1H> 2.3C
PEX_TXX9	2.1H> 2.3C
PEX_TXX9*	2.2H> 2.4C
PEX_TXX10	2.2H> 2.4C
PEX_TXX10*	2.2H> 2.4C
PEX_TXX11	2.2H> 2.4C
PEX_TXX11*	2.2H> 2.4C
PEX_TXX12	2.2H> 2.4C
PEX_TXX12*	2.2H> 2.4C
PEX_TXX13	2.2H> 2.4C
PEX_TXX13*	2.2H> 2.4C
PEX_TXX14	2.2H> 2.4C
PEX_TXX14*	2.2H> 2.5C
PEX_TXX15	2.2H> 2.5C
PEX_TXX15*	2.2H> 2.5C
RESET_BUF*	18.2H> 19.2A< 19.3E 21.1H< 22.3B<
ROM_CS*	15.3F< 18.2H>
SEL_2ND_DEV	17.2A< 17.2A< 25.3C>
STEREO	18.2H> 21.2A< 21.2A<
SWAPREADY	16.3D> 17.4D> 18.5G<> 21.2F<
THERMDA	25.1G<> 25.2G
THERMDC	25.1G<> 25.2G
UGATE1	28.1H> 28.3C
UGATE1_GATE	28.1H> 28.2D
UGATE2	28.1H> 28.3C
UGATE2_GATE	28.1H> 28.3D
XTALSSIN	16.5A< 21.2F>

ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	29 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

*** Part Cross-Reference for the entire design ***

BKT1	BRACKET	14
C1	C	20
C2	C	19
C3	C	16
C4	C	19
C5	C	16
C6	C	16
C7	C	21
C8	C	21
C9	C	21
C10	C	21
C11	C	16
C12	C	21
C13	C	17
C14	C	17
C15	C	17
C16	C	21
C17	C	21
C18	C	21
C19	C	21
C20	C	21
C21	C	21
C22	C	21
C23	C	22
C24	C	17
C25	C	17
C26	C	17
C27	C	21
C28	C	16
C29	C	22
C30	C	17
C31	C	19
C32	C	16
C33	C	19
C34	C	16
C35	C	22
C36	C	22
C37	C	22
C38	C	22
C39	C	19
C40	C	19
C41	C	21
C42	C	21
C43	C	19
C44	C	19
C45	C	19
C46	C	19
C47	C	19
C48	C	19
C49	C	19
C50	C	19
C51	C	12
C52	C	12
C53	C	12
C54	C	19
C55	C	12
C56	C	12
C57	C	12
C58	C	19
C59	C	12
C60	C	19
C61	C	12
C62	C	12
C63	C	19
C64	C	25
C65	C	12
C66	C	12
C67	C	12
C68	C	19
C69	C	2
C70	C	12
C71	C	12
C72	C	12
C73	C	11
C74	C	12
C75	C	11
C76	C	11
C77	C	12
C78	C	11
C79	C	11
C80	C	11
C81	C	15
C82	C	12
C83	C	11
C84	C	11
C85	C	11
C86	C	12
C87	C	11
C88	C	11
C89	C	11
C90	C	12
C91	C	11
C92	C	11
C93	C	11
C94	C	11
C95	C	14
C96	C	11
C97	C	11
C98	C	11
C99	C	16
C100	C	14
C101	C	11
C102	C	14
C103	C	14
C104	C	16
C105	C	10
C106	C	10
C107	C	10
C108	C	10
C109	C	10
C110	C	10
C111	C	10
C112	C	10
C113	C	10
C114	C	10
C115	C	10
C116	C	10
C117	C	10
C118	C	10
C119	C	10
C120	C	10
C121	C	10
C122	C	10
C123	C	10
C124	C	10
C125	C	9
C126	C	9
C127	C	9
C128	C	9
C129	C	9
C130	C	9
C131	C	9
C132	C	9
C133	C	9
C134	C	9
C135	C	9
C136	C	9
C137	C	9
C138	C	9
C139	C	9
C140	C	9
C141	C	9
C142	C	9
C143	C	9
C144	C	9
C145	C	8
C146	C	8
C147	C	8
C148	C	8
C149	C	8
C150	C	8
C151	C	8
C152	C	8
C153	C	7
C154	C	8
C155	C	8
C156	C	8
C157	C	7
C158	C	8
C159	C	8
C160	C	8
C161	C	7
C162	C	8
C163	C	8
C164	C	8
C165	C	7
C166	C	8
C167	C	8
C168	C	6
C169	C	6
C170	C	5
C171	C	5
C172	C	7
C173	C	8
C174	C	6
C175	C	6
C176	C	5
C177	C	5
C178	C	7
C179	C	7
C180	C	7
C181	C	6
C182	C	6
C183	C	5
C184	C	5
C185	C	7
C186	C	7
C187	C	7
C188	C	6
C189	C	6
C190	C	5
C191	C	5
C192	C	7
C193	C	7
C194	C	7
C195	C	7
C196	C	7
C197	C	7
C198	C	6
C199	C	6
C200	C	5
C201	C	5
C202	C	6
C203	C	6
C204	C	6
C205	C	6
C206	C	5
C207	C	5
C208	C	5
C209	C	5
C210	C	7
C211	C	7
C212	C	6
C213	C	5
C214	C	6
C215	C	5
C216	C	6
C217	C	6
C218	C	6
C219	C	6
C220	C	5
C221	C	5
C222	C	5
C223	C	5
C224	C	7
C225	C_POL	27
C226	C	28
C227	C	28
C228	C	28
C229	C	28
C230	C_POL	28
C231	C_POL	28
C232	C_POL	28
C233	C_POL	28
C234	C	28
C235	C_POL	27
C236	C_POL	27
C237	C_POL	27
C238	C	28
C239	C	23
C240	C_POL	26
C241	C_POL	26
C242	C	28
C243	C	27
C244	C	27
C245	C	27
C246	C	27
C247	C	28
C248	C	28
C249	C	28
C250	C	26
C251	C	27
C252	C	26
C253	C	26
C254	C	28
C255	C	26
C256	C	27
C257	C	27
C258	C	26
C259	C	27
C260	C	27
C261	C_POL	26
C262	C	27
C263	C_POL	26
C264	C_POL	26
C265	C	27
C266	C_POL	26
C267	C_POL	26
C268	C_POL	26
C269	C_POL	26
C270	C	26
C271	C_POL	26
C272	C_POL	26
C273	C_POL	26
C274	C	26
C275	C_POL	26
C276	C_POL	28
C277	C	28
C278	C	28
C279	C_POL	18
C280	C	22
C501	C	26
C502	C	25
C503	C	26
C504	C	26
C505	C	26
C506	C	28
C507	C	26
C508	C	26
C509	C	28
C510	C	26
C511	C	28
C512	C	28
C513	C	26
C514	C	28
C515	C	28
C516	C	28
C517	C	28
C518	C	26
C519	C	28
C520	C	26
C521	C	26
C522	C	28
C523	C	28
C524	C	26
C525	C	26
C526	C	26
C527	C	28
C528	C	27
C529	C	26
C530	C	26
C531	C	28
C532	C	28
C533	C	26
C534	C	28
C535	C	27
C536	C	27
C537	C	27
C538	C	27
C539	C	27
C540	C	27
C541	C	27
C542	C	27
C543	C	28
C544	C	28
C545	C	28
C546	C	2
C547	C	27
C548	C	27
C549	C	27
C550	C	27
C551	C	27
C552	C	27
C553	C	28
C554	C	27
C555	C	27
C556	C	27
C557	C	27
C558	C	28
C559	C	27
C560	C	27
C561	C	27
C562	C	27
C563	C	27
C564	C	27
C565	C	27
C566	C	27
C567	C	28
C568	C	27
C569	C	27
C570	C	27
C571	C	27
C572	C	27
C573	C	27
C574	C	27
C575	C	27
C576	C	27
C577	C	27
C578	C	27
C579	C	27
C580	C	7
C581	C	6
C582	C	6
C583	C	6
C584	C	6
C585	C	5
C586	C	5
C587	C	5
C588	C	5
C589	C	6
C590	C	6
C591	C	5
C592	C	5
C593	C	6
C594	C	6
C595	C	5
C596	C	5
C597	C	7
C598	C	7
C599	C	7
C600	C	6
C601	C	6
C602	C	6
C603	C	6
C604	C	5
C605	C	5
C606	C	5
C607	C	5
C608	C	6
C609	C	6
C610	C	5
C611	C	5
C612	C	7
C613	C	7
C614	C	7
C615	C	7
C616	C	7
C617	C	7
C618	C	6
C619	C	6
C620	C	5
C621	C	5
C622	C	7
C623	C	7
C624	C	7
C625	C	6
C626	C	6
C627	C	5
C628	C	5
C629	C	7
C630	C	7
C631	C	8
C632	C	7
C633	C	6
C634	C	6
C635	C	5
C636	C	5
C637	C	8
C638	C	5
C639	C	7
C640	C	7
C641	C	6
C642	C	6
C643	C	5
C644	C	5
C645	C	8
C646	C	8
C647	C	7
C648	C	7
C649	C	7
C650	C	7
C651	C	5
C652	C	5
C653	C	8
C654	C	8
C655	C	8
C656	C	7
C657	C	8
C658	C	8
C659	C	8
C660	C	7
C661	C	6
C662	C	6
C663	C	5
C664	C	8
C665	C	8
C666	C	8
C667	C	7
C668	C	8
C669	C	6
C670	C	6
C671	C	6
C672	C	6
C673	C	5
C674	C	5
C675	C	8
C676	C	8
C677	C	8
C678	C	7
C679	C	7
C680	C	8
C681	C	8
C682	C	7
C683	C	8
C684	C	8
C685	C	8
C686	C	8
C687	C	8
C688	C	8
C689	C	25
C690	C	24
C691	C	8
C692	C	24
C693	C	8
C694	C	25
C695	C	8
C696	C	23
C697	C	24
C698	C	23
C699	C	24
C700	C	23
C701	C	2
C702	C	24
C703	C	24
C704	C	2
C705	C	3
C706	C	23
C707	C	23
C708	C	3
C709	C	24
C710	C	23
C711	C	23
C712	C	2
C713	C	24
C714	C	3
C715	C	3
C716	C	23
C717	C	2
C718	C	23
C719	C	23
C720	C	23
C721	C	9
C722	C	9
C723	C	9
C724	C	9
C725	C	9
C726	C	9
C727	C	9
C728	C	24
C729	C	23
C730	C	23
C731	C	13
C732	C	9
C733	C	9
C734	C	23
C735	C	2
C736	C	3
C737	C	23
C738	C	3
C739	C	9
C740	C	2
C741	C	3
C742	C	3
C743	C	3
C744	C	9
C745	C	9
C746	C	23
C747	C	23
C748	C	23
C749	C	23
C750	C	23
C751	C	23
C752	C	13
C753	C	3
C754	C	2
C755	C	23
C756	C	3
C757	C	3
C758	C	24
C759	C	2
C760	C	23
C761	C	9
C762	C	9
C763	C	23
C764	C	23
C765	C	23
C766	C	23
C767	C	23
C768	C	24
C769	C	24
C770	C	23
C771	C	23
C772	C	4
C773	C	24
C774	C	23
C775	C	24
C776	C	24
C777	C	23
C778	C	2
C779	C	24
C780	C	24
C781	C	23
C782	C	2
C783	C	9
C784	C	9
C785	C	24
C786	C	24
C787	C	2
C788	C	4
C789	C	23
C790	C	23
C791	C	23
C792	C	23
C793	C	2
C794	C	24
C795	C	24
C796	C	2
C797	C	24
C798	C	24
C799	C	24
C800	C	2
C801	C	4
C802	C	24
C803	C	23
C804	C	23
C805	C	2
C806	C	9
C807	C	9
C808	C	23
C809	C	24
C810	C	24
C811	C	2
C812	C	4
C813	C	4
C814	C	4
C815	C	2
C816	C	23
C817	C	24
C818	C	24
C819	C	24
C820	C	2
C821	C	10
C822	C	2
C823	C	23
C824	C	24
C825	C	23
C826	C	2
C827	C	24
C828	C	24
C829	C	24
C830	C	24
C831	C	2
C832	C	2
C833	C	2
C834	C	9
C835	C	9
C836	C	9
C837	C	24
C838	C	2
C839	C	24
C840	C	24
C841	C	2
C842	C	9
C843	C	9
C844	C	9
C845	C	9
C846	C	9
C847	C	9
C848	C	23
C849	C	23
C850	C	23
C851	C	23
C852	C	2
C853	C	24
C854	C	24
C855	C	23
C856	C	10
C857	C	10
C858	C	10
C859	C	10
C860	C	10
C861	C	10
C862	C	10
C863	C	2
C864	C	2
C865	C	2
C866	C	4
C867	C	2
C868	C	24
C869	C	10
C870	C	24
C871	C	24
C872	C	24
C873	C	24
C874	C	10
C875	C	2
C876	C	23
C877	C	24
C878	C	24
C879	C	13
C880	C	13
C881	C	24
C882	C	2
C883	C	9
C884	C	24
C885	C	24
C886	C	18
C887	C	23
C888	C	2
C889	C	2
C890	C	23
C891	C	23
C892	C	24
C893	C	10
C894	C	10
C895	C	24
C896	C	24
C897	C	2
C898	C	23
C899	C	23
C900	C	23
C901	C	23
C902	C	23
C903	C	17
C904	C	2
C905	C	2
C906	C	23
C907	C	24
C908	C	4
C909	C	23
C910	C	23
C911	C	4
C912	C	10
C913	C	10
C914	C	18
C915	C	18
C916	C	18
C917	C	4
C918	C	16
C919	C	24
C920	C	16
C921	C	23
C922	C	2
C923	C	18
C924	C	15
C925	C	2
C926	C	10
C927	C	10
C928	C	17
C929	C	24
C930	C	24
C931	C	2
C932	C	23
C933	C	23
C934	C	23
C935	C	20
C936	C	18
C937	C	20
C938	C	15
C939	C	23
C940	C	4
C941	C	10
C942	C	10
C943	C	20
C944	C	16
C945	C	18
C946	C	17
C947	C	2
C948	C	18
C949	C	15
C950	C	23
C951	C	24
C952	C	10
C953	C	20
C954	C	20
C955	C	2
C956	C	18
C957	C	23
C958	C	23
C959	C	24
C960	C	10
C961	C	15
C962	C	15
C963	C	15
C964	C	10
C965	C	15
C966	C	10
C967	C	10
C968	C	10
C969	C	10
C970	C	10
C971	C	10
C972	C	10
C973	C	16
C974	C	18
C975	C	20
C976	C	4
C977	C	15
C978	C	15
C979	C	2
C980	C	24
C981	C	15
C982	C	2
C983	C	20
C984	C	23
C985	C	24
C986	C	2
C987	C	20
C988	C	24
C989	C	2
C990	C	20
C991	C	20
C992	C	17
C993	C	20
C994	C	20
C995	C	20
C996	C	15
C997	C	20
C998	C	15
C999	C	18
C1000	C	20
C1001	C	16
C1002	C	11
C1003	C	2
C1004	C	20
C1005	C	15
C1006	C	11
C1007	C	2
C1008	C	20
C1009	C	11
C1010	C	20
C1011	C	15
C1012	C	15
C1013	C	24
C1014	C	20
C1015	C	24
C1016	C	2
C1017	C	11
C1018	C	20
C1019	C	20
C1020	C	2
C1022	C	18
C1023	C	20
C1024	C	11
C1025	C	20
C1026	C	18
C1027	C	11
C1028	C	2
C1029	C	14
C1030	C	14
C1031	C	2
C1032	C	11
C1033	C	11
C1034	C	12
C1035	C	14
C1036	C	11
C1037	C	11
C1038	C	11
C1039	C	12
C1040	C	14
C1041	C	11
C1042	C	2
C1043	C	20
C1044	C	12
C1045	C	2
C1046	C	11
C1047	C	11
C1048	C	11
C1049	C	20
C1050	C	12
C1051	C	11
C1052	C	11
C1053	C	11
C1054	C	12
C1055	C	11
C1056	C	11
C1057	C	11
C1058	C	12
C1059	C	11
C1060	C	11
C1061	C	11
C1062	C	12
C1063	C	12
C1064	C	12
C1065	C	12
C1066	C	24
C1067	C	11
C1068	C	11
C1069	C	25
C1070	C	2
C1071	C	12
C1072	C	12
C1073	C	11
C1074	C	25
C1075	C	19
C1076	C	12
C1077	C	11
C1078	C	12
C1079	C	25
C1080	C	2
C1081	C	12
C1082	C	19
C1083	C	12
C1084	C	12
C1085	C	19
C1086	C	19
C1087	C	19
C1088	C	12
C1089	C	2
C1090	C	19
C1091	C	12
C1092	C	12
C1093	C	12
C1094	C	22
C1095	C	22
C1096	C	22
C1097	C	22
C1098	C	19
C1099	C	22
C1100	C	22
C1101	C	19
C1102	C	12
C1103	C	12
C1104	C	12
C1105	C	12
C1106	C	12
C1107	C	12
C1108	C	22
C1109	C	22
C1110	C	12
C1111	C	22
C1112	C	22
C1113	C	19
C1114	C	19
C1115	C	21
C1116	C	19
C1117	C	22
C1118	C	22
C1119	C	22
C1120	C	22
C1121	C	19
C1122	C	19
C1123	C	19
C1124	C	19
C1125	C	19
C1126	C	19
C1127	C	22
C1128	C	22
C1129	C	22
C1130	C	22
C1131	C	22
C1132	C	22
C1133	C	22
C1134	C	22
C1135	C	22
C1136	C	22
C1137	C	22
C1138	C	22
C1139	C	17
C1140	C	22
C1141	C	17
C1142	C	21
C1143	C	19
C1144	C	19
C1145	C	22
C1146	C	22
C1147	C	17
C1148	C	21
C1149	C	16
C1150	C	16
C1151	C	16
C1152	C	21
C1153	C	21
C1154	C	16
C1155	C	16
C1156	C	16

ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	30 OF 31
NAME	TSchirmer	DATE	4-NOV-2004

```
C1157 C        16
C1158 C        21
C1159 C        21
C1160 C        17
C1161 C        17
C1162 C        17
C1163 C        17
C1164 C        17
C1165 C        17
C1166 C        20
C1167 C        16
C1168 C        16
CN1   CON_MIO_26 18
CN2   CON_PCI_EXPRESS 2
D1    D_3PIN_AC 16
D2    D_3PIN_AC 16
D3    D_3PIN_AC 21
D4    D_3PIN_AC 21
D5    D_3PIN_AC 21
D6    D_3PIN_AC 21
D7    D_3PIN_AC 17
D8    D_3PIN_AC 17
D9    D_3PIN_AC 17
D10   D_3PIN_AC 19
D11   D_3PIN_AC 21
D12   D_SCHOTTKY 25
D13   D_SCHOTTKY 28
D14   D_SCHOTTKY 26
D15   D_SCHOTTKY 28
D501  D_SCHOTTKY_3PIN_AA 26
D502  D_3PIN_CC 25
D503  D_3PIN_CC 25
D504  D_ZENER   28
D505  D_3PIN_AC 26
D506  D_3PIN_AA 25
D507  D_3PIN_CC 25
D508  D_3PIN_CC 25
D509  D_3PIN_AA 28
D510  D_ZENER_3PIN_AA 28
D511  D_3PIN_AA 25
D512  D_3PIN_CC 25
D513  D_3PIN_CC 25
D514  D_SCHOTTKY 27
D515  D_SCHOTTKY 27
D516  D_SCHOTTKY 27
D517  D_SCHOTTKY 27
D518  D         20
D519  D_SCHOTTKY 20
D520  D_3PIN_AC 21
D521  D_3PIN_AC 16
D522  D_3PIN_AC 16
D523  D_3PIN_AC 16
D524  D_3PIN_AC 21
D525  D_3PIN_AC 20
D526  D_3PIN_AC 17
D527  D_3PIN_AC 17
D528  D_3PIN_AC 17
D529  D_3PIN_AC 17
D530  D_3PIN_AC 16
D531  D_3PIN_AC 16
F1    F_POLYSW  16
F2    F_POLYSW  21
J1    CON_MINIDIN_9 21
J2    CON_DVI_I 20
J3    CON_DVI_I 19
J4    HDR_2X7   21
J5    HDR_1X4   21
J6    HDR_1X2   25
J7    HDR_2X3   26
J501  HDR_2X4   15
L1    L_CMF_4P  17
L2    L_CMF_4P  17
L3    L_CMF_4P  17
L4    L         16
L5    L         16
L6    L         21
L7    L         21
L8    L         21
L9    L         21
L10   L         17
L11   L         17
L12   L         17
L13   L         25
L14   L         27
L15   L         27
L16   L         27
L17   L         27
L18   L         26
L19   L         28
L20   L         28
L21   L         26
L22   L         26
L23   L         26
L501  L         26
L502  L         16
L503  L         16
L504  L         16
L505  L         21
L506  L         17
L507  L         17
L508  L_CMF_4P  16
L509  L_CMF_4P  16
L510  L_CMF_4P  16
LB1   L         16
LB2   L         19
LB3   L         21
LB4   L         22
LB5   L         19
LB6   L         19
LB501 L         3
LB502 L         3
LB503 L         3
LB504 L         3
LB505 L         4
LB506 L         2
LB507 L         2
LB508 L         4
LB509 L         2
LB510 L         2
LB511 L         4
LB512 L         18
LB513 L         4
LB514 L         15
LB515 L         15
LB516 L         16
LB517 L         17
LB518 L         15
LB519 L         15
LB520 L         20
LB521 L         20
LB522 L         20
LB523 L         20
LB524 L         20
LB525 L         14
```

```
LB526 L         14
LB527 L         19
LB528 L         19
LB529 L         22
LB530 L         17
LB531 L         22
LB532 L         21
LB533 L         21
LB534 L         21
LB535 L         17
LB536 L         17
LB537 L         20
LB538 L         16
LB539 L         16
LB540 L         21
MEC1  MEC_SCREW 14
MEC2  MEC_SCREW 14
MEC3  MEC_SCREW 14
MEC4  MEC_SCREW 14
MEC501 MEC_SCREW 14
Q1    Q_FET_N_ENH 27
Q2    Q_FET_N_ENH 27
Q3    Q_FET_N_ENH 27
Q4    Q_FET_N_ENH 27
Q5    Q_FET_N_ENH 28
Q6    Q_FET_N_ENH 27
Q7    Q_FET_N_ENH 27
Q8    Q_FET_N_ENH 27
Q9    Q_FET_N_ENH 27
Q10   Q_FET_N_ENH 28
Q11   Q_FET_N_ENH 28
Q12   Q_FET_N_ENH 27
Q13   Q_FET_N_ENH 27
Q14   Q_FET_N_ENH 27
Q15   Q_FET_N_ENH 27
Q16   Q_FET_N_ENH 26
Q17   Q_FET_N_ENH 28
Q501  Q_FET_N_ENH 26
Q502  Q_FET_N_ENH 25
Q503  Q_NPN     28
Q504  Q_FET_N_ENH 25
Q505  Q_FET_N_ENH 26
Q506  Q_FET_N_ENH 25
Q507  Q_FET_N_ENH 28
Q508  Q_NPN     28
Q509  Q_FET_N_ENH 28
Q510  Q_FET_N_ENH 17
Q511  Q_FET_N_ENH 18
Q512  Q_FET_N_ENH 25
Q513  Q_FET_N_ENH 25
Q514  Q_FET_N_ENH 25
R1    R         17
R2    R         17
R3    R         17
R4    R         17
R5    R         17
R6    R         17
R7    R         21
R8    R         19
R9    R         19
R10   R         17
R11   R         17
R12   R         21
R13   R         21
R14   R         17
R15   R         17
R16   R         21
R17   R         21
R18   R         21
R19   R         21
R20   R         21
R21   R         17
R22   R         17
R23   R         21
R24   R         19
R25   R         19
R26   R         19
R27   R         19
R28   R         21
R29   R         19
R30   R         19
R31   R         19
R32   R         19
R33   R         19
R34   R         25
R35   R         18
R36   R         22
R37   R         19
R38   R         19
R39   R         19
R40   R         25
R41   R         25
R42   R         15
R43   R         15
R44   R         19
R45   R         16
R46   R         12
R47   R         12
R48   R         12
R49   R         12
R50   R         14
R51   R         14
R52   R         14
R53   R         11
R54   R         11
R55   R         11
R56   R         11
R57   R         14
R58   R         14
R59   R         26
R60   R         15
R61   R         15
R62   R         18
R63   R         16
R64   R         21
R65   R         21
R66   R         15
R67   R         15
R68   R         15
R69   R         10
R70   R         10
R71   R         10
R72   R         10
R73   R         9
R74   R         9
R75   R         9
R76   R         9
R77   R         8
R78   R         8
R79   R         8
R80   R         8
R81   R         6
R82   R         6
R83   R         5
```

```
R84   R         5
R85   R         7
R86   R         7
R87   R         7
R88   R         6
R89   R         6
R90   R         5
R91   R         5
R92   R         7
R93   R         28
R94   R         22
R95   R         22
R501  R         26
R502  R         26
R503  R         28
R504  R         26
R505  R         26
R506  R         26
R507  R         26
R508  R         26
R509  R         28
R510  R         26
R511  R         28
R512  R         25
R513  R         25
R514  R         25
R515  R         25
R516  R         25
R517  R         25
R518  R         28
R519  R         28
R520  R         26
R521  R         26
R522  R         26
R523  R         26
R524  R         28
R525  R         28
R526  R         25
R527  R         25
R528  R         25
R529  R         25
R530  R         25
R531  R         25
R532  R         25
R533  R         25
R534  R         26
R535  R         28
R536  R         28
R537  R         26
R538  R         28
R539  R         28
R540  R         25
R541  R         25
R542  R         28
R543  R         25
R544  R         28
R545  R         27
R546  R         27
R547  R         27
R548  R         27
R549  R         27
R550  R         28
R551  R         28
R552  R         27
R553  R         28
R554  R         27
R555  R         27
R556  R         27
R557  R         27
R558  R         27
R559  R         27
R560  R         27
R561  R         27
R562  R         27
R563  R         27
R564  R         27
R565  R         27
R566  R         28
R567  R         28
R568  R         28
R569  R         28
R570  R         27
R571  R         27
R572  R         27
R573  R         27
R574  R         27
R575  R         27
R576  R         27
R577  R         27
R578  R         27
R579  R         27
R580  R         27
R581  R         27
R582  R         27
R583  R         27
R584  R         27
R585  R         27
R586  R         27
R587  R         27
R588  R         27
R589  R         27
R590  R         27
R591  R         27
R592  R         27
R593  R         27
R594  R         28
R595  R         28
R596  R         7
R597  R         5
R598  R         7
R599  R         5
R600  R         6
R601  R         6
R602  R         5
R603  R         7
R604  R         6
R605  R         5
R606  R         7
R607  R         7
R608  R         6
R609  R         6
R610  R         5
R611  R         6
R612  R         6
R613  R         5
R614  R         5
R615  R         7
R616  R         6
R617  R         5
R618  R         7
R619  R         7
R620  R         6
R621  R         6
R622  R         5
```

```
R623  R         5
R624  R         7
R625  R         8
R626  R         7
R627  R         8
R628  R         8
R629  R         8
R630  R         8
R631  R         8
R632  R         8
R633  R         8
R634  R         8
R635  R         8
R636  R         25
R637  R         3
R638  R         25
R639  R         3
R640  R         13
R641  R         9
R642  R         9
R643  R         13
R644  R         13
R645  R         13
R646  R         9
R647  R         13
R648  R         9
R649  R         2
R650  R         23
R651  R         23
R652  R         9
R653  R         9
R654  R         15
R655  R         9
R656  R         23
R657  R         9
R658  R         2
R659  R         15
R660  R         2
R661  R         4
R662  R         9
R663  R         9
R664  R         10
R665  R         2
R666  R         10
R667  R         23
R668  R         13
R669  R         13
R670  R         2
R671  R         18
R672  R         18
R673  R         18
R674  R         2
R675  R         23
R676  R         18
R677  R         10
R678  R         16
R679  R         10
R680  R         13
R681  R         18
R682  R         13
R683  R         16
R684  R         2
R685  R         2
R686  R         10
R687  R         17
R688  R         17
R689  R         10
R690  R         18
R691  R         10
R692  R         18
R693  R         13
R694  R         10
R695  R         18
R696  R         17
R697  R         17
R698  R         18
R699  R         10
R700  R         20
R701  R         4
R702  R         10
R703  R         25
R704  R         20
R705  R         20
R706  R         20
R707  R         20
R708  R         20
R709  R         20
R710  R         20
R711  R         20
R712  R         20
R713  R         20
R714  R         20
R715  R         20
R716  R         20
R717  R         20
R718  R         20
R719  R         20
R720  R         11
R721  R         11
R722  R         14
R723  R         14
R724  R         11
R725  R         11
R726  R         11
R727  R         20
R728  R         11
R729  R         18
R730  R         18
R731  R         14
R732  R         14
R733  R         11
R734  R         20
R735  R         11
R736  R         20
R737  R         18
R738  R         11
R739  R         12
R740  R         11
R741  R         12
R742  R         12
R743  R         12
R744  R         12
R745  R         12
R746  R         12
R747  R         12
R748  R         15
R749  R         15
R750  R         15
R751  R         15
R752  R         15
R753  R         15
R754  R         15
R755  R         15
R756  R         12
```

```
R757  R         15
R758  R         15
R759  R         15
R760  R         15
R761  R         15
R762  R         15
R763  R         15
R764  R         12
R765  R         15
R766  R         15
R767  R         15
R768  R         15
R769  R         15
R770  R         15
R771  R         15
R772  R         19
R773  R         19
R774  R         15
R775  R         15
R776  R         25
R777  R         19
R778  R         25
R779  R         25
R780  R         25
R781  R         19
R782  R         19
R783  R         19
R784  R         19
R785  R         19
R786  R         19
R787  R         19
R788  R         21
R789  R         21
R790  R         25
R791  R         22
R792  R         25
R793  R         22
R794  R         25
R795  R         19
R796  R         22
R797  R         25
R798  R         19
R799  R         19
RB00  R         17
RB01  R         17
RB02  R         17
RB03  R         17
RB04  R         19
RB05  R         25
RB06  R         19
RB07  R         17
RB08  R         17
RB09  R         19
RB10  R         17
RB11  R         19
RB12  R         21
RB13  R         17
RB14  R         17
RB15  R         17
RB16  R         16
RB17  R         16
RB18  R         17
RB19  R         16
RB20  R         16
RB21  R         16
RB22  R         16
RB23  R         16
RB24  R         16
RB25  R         16
RB26  R         16
RB27  R         21
RB28  R         17
RB29  R         20
RB30  R         17
RB31  R         25
RB32  R         25
RB33  R         21
RB34  R         17
RB35  R         17
RB36  R         20
RB37  R         17
RB38  R         25
RB39  R         16
RB40  R         16
RB41  R         16
RB42  R         16
RB43  R         16
RB44  R         16
RB45  R         16
RB46  R         21
RB47  R         16
RP1   R_PAK     22
RP2   R_PAK     22
RP501 R_PAK     19
RP502 R_PAK     19
RP503 R_PAK     19
U1    U_VDC_SAA71XX 22
U2    U_PNLNK_S111XX 19
U3    U_PNLNK_S111XX 19
U4    U_MEM_EE_CRYPT_B12B 25
U5    U_MEM_SD_DDR3_X32 12
U6    U_MEM_FL_SER_128KX8 15
U7    U_MEM_SD_DDR3_X32 11
U8    U_CLK_FL_908Z07 14
U9    U_MEM_SD_DDR3_X32 10
U10   U_GPU_G4_PCIEX 2 3 4 13 15 16 17 18 20 23 24
                      25
U11   U_MEM_SD_DDR3_X32 9
U12   U_MEM_SD_DDR3_X32 8
U13   U_MEM_SD_DDR3_X32 7
U14   U_MEM_SD_DDR3_X32 6
U15   U_MEM_SD_DDR3_X32 5
U501  U_SWREG_ISL6549 26
U502  U_SWREG_ISL6534 28
U503  U_SWREG_ISL6559 27
U504  U_SWREG_HIP660X 27
U505  U_SWREG_HIP660X 27
U506  U_SWREG_HIP660X 27
U507  U_SWREG_HIP660X 27
U508  U_MEM_SD_DDR3_X32 6
U509  U_MEM_SD_DDR3_X32 5
U510  U_MEM_SD_DDR3_X32 7
U511  U_MEM_SD_DDR3_X32 8
U512  U_TEMP_AD1032 25
U513  U_MEM_SD_DDR3_X32 9
U514  U_MEM_SD_DDR3_X32 10
U515  U_VREG_3PIN 20
U516  U_SHNTREG_TL431 18
U517  U_VREG_5PIN 20
U518  U_MEM_SD_DDR3_X32 11
U519  U_MEM_SD_DDR3_X32 12
U520  U_PNLNK_S111XX 19
U521  U_SW_ANA_3257 17
U522  U_AND_2IN 21
```

```
U523  U_XOR_2IN 25
U524  U_AND_2IN 16 17
Y1    XTAL_4PIN 16
Y501  XTAL      22
```

ASSEMBLY	WKST SKU0000:NV45GL-P214 B03, 512MB, GDDR3, dual DL-DVI-I, Stereo
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-50214-0000-400		
ID	design	PAGE	31 OF 31
NAME	TSchirmer	DATE	4-NOV-2004