PRELIMINARY AND SUBJECT TO CHANGE

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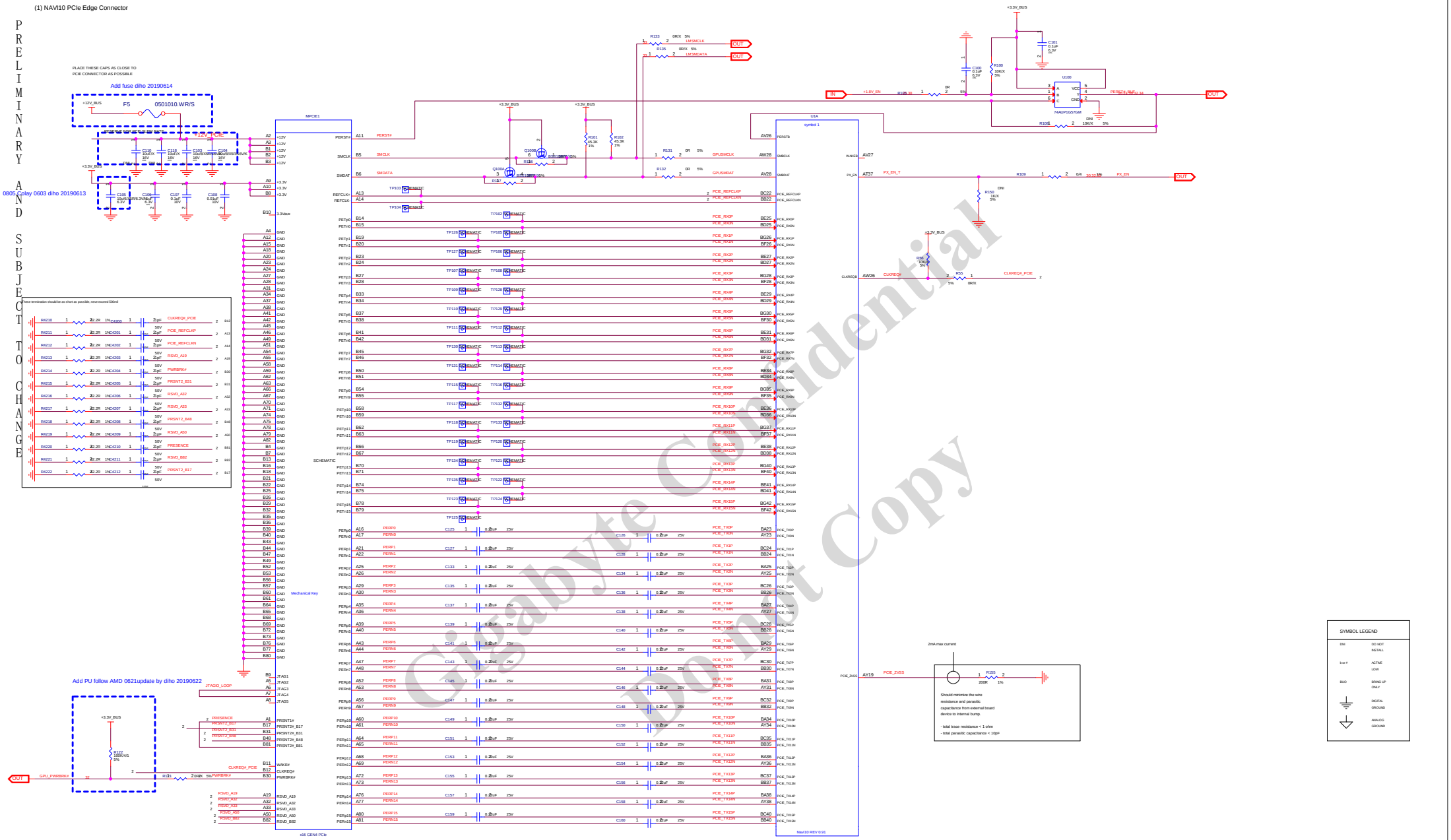
(1) NAVI10 PCIe Edge Connector
PRELIMINARY AND SUBJECT TO CHANGE
PLACE THESE CAPS AS CLOSE TO PCIE CONNECTOR AS POSSIBLE
Add fuse dih0 20190614
F5
0501010.WR/S
0805_delay 0603 dih0 20190613
MPCIE1
x16 GEN4 PCIe
Mechanical Key
U1A
symbol 1
Nav10 REV 0.91
Add PU follow AMD 0621update by dih0 20190622
JTAGIO_LOOP
PRESENCE
CLKREQ#_PCIE
PWRBRK#
GPU_PWRBRK#
RSVD_A19
RSVD_A32
RSVD_A33
RSVD_A50
RSVD_B82
PERST#
SMCLK
SMDATA
GPUSMCLK
GPUSMDAT
PCIE_REFCLKP
PCIE_REFCLKN
PX_EN
PX_EN_T
CLKREQ#
CLKREQ#_PCIE
PCIE_2V5S
2mA max current
Should minimize the wire resistance and parasitic capacitance from external board device to internal bump.
- total trace resistance < 1 ohm
- total parasitic capacitance < 10pF
SYMBOL LEGEND
DO NOT INSTALL
ACTIVE LOW
BRING UP ONLY
DIGITAL GROUND
ANALOG GROUND
Confidential
Do not Copy
GIGABYTE
PCIE INTERFACE
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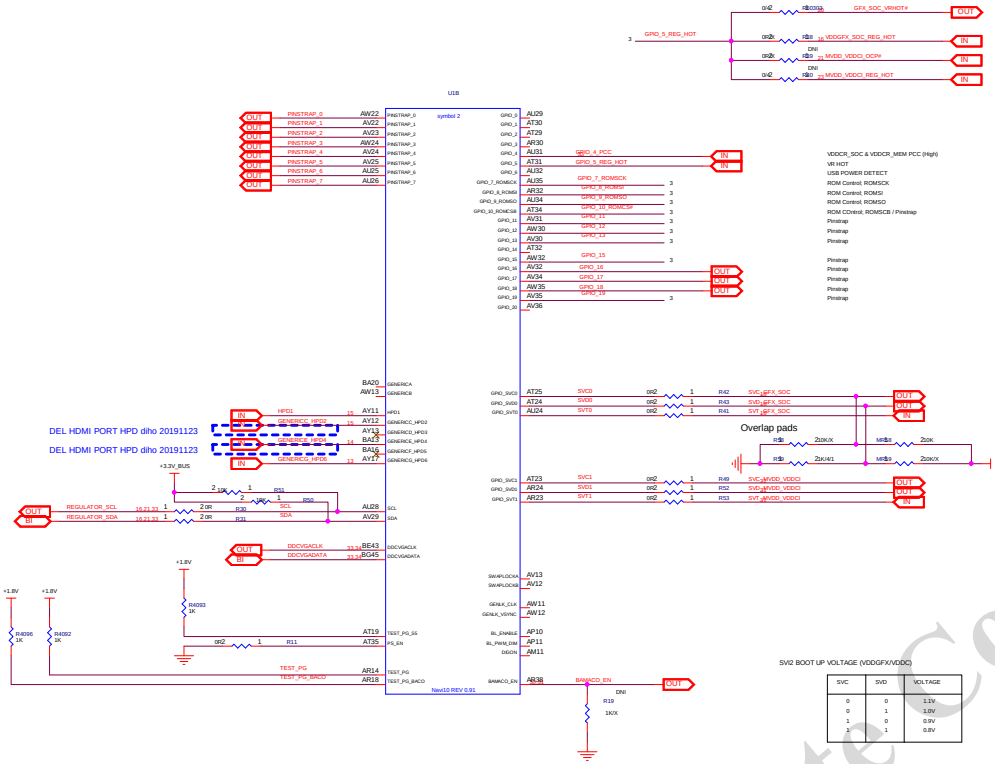

Note: Internal PU/PD at GPIO pad is ~40k strength in 14nm design spec

User		Internal Default Value	Definition
BIF		0	STRAP_BIF_GEN4_DIS_A 0: PCIe GEN 4 supported 1: PCIe GEN 4 not supported
		0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled
		0	PINSTRAP_BIF_LC_TX_SWING
		0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognised as the system's VGA controller
DCE		0 0 0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected
		0 0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for DisplayPort and native HDMI
Platform		0 0 0	
SMU		1 0 1	
			PINSTRAP_SMBUS_ADDR 0: 0x41h 1: 0x40h
		1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device

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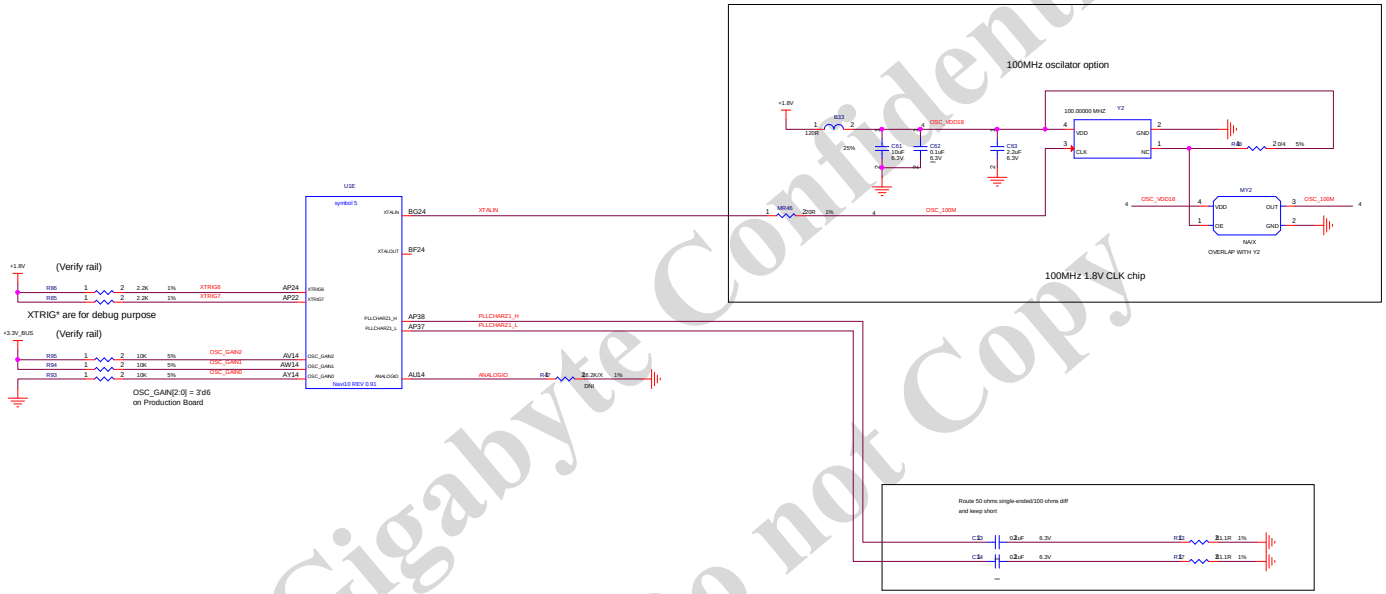

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NAVI 10 MEM INTERFACE CH A/B

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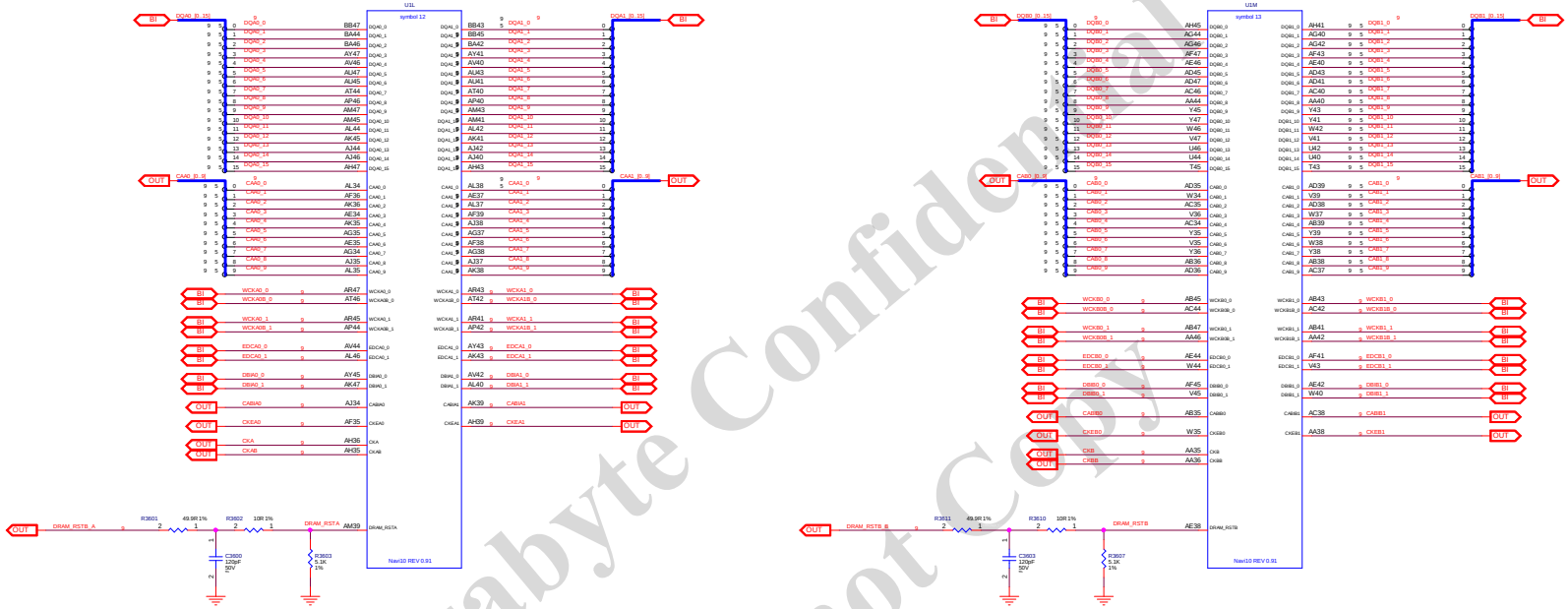

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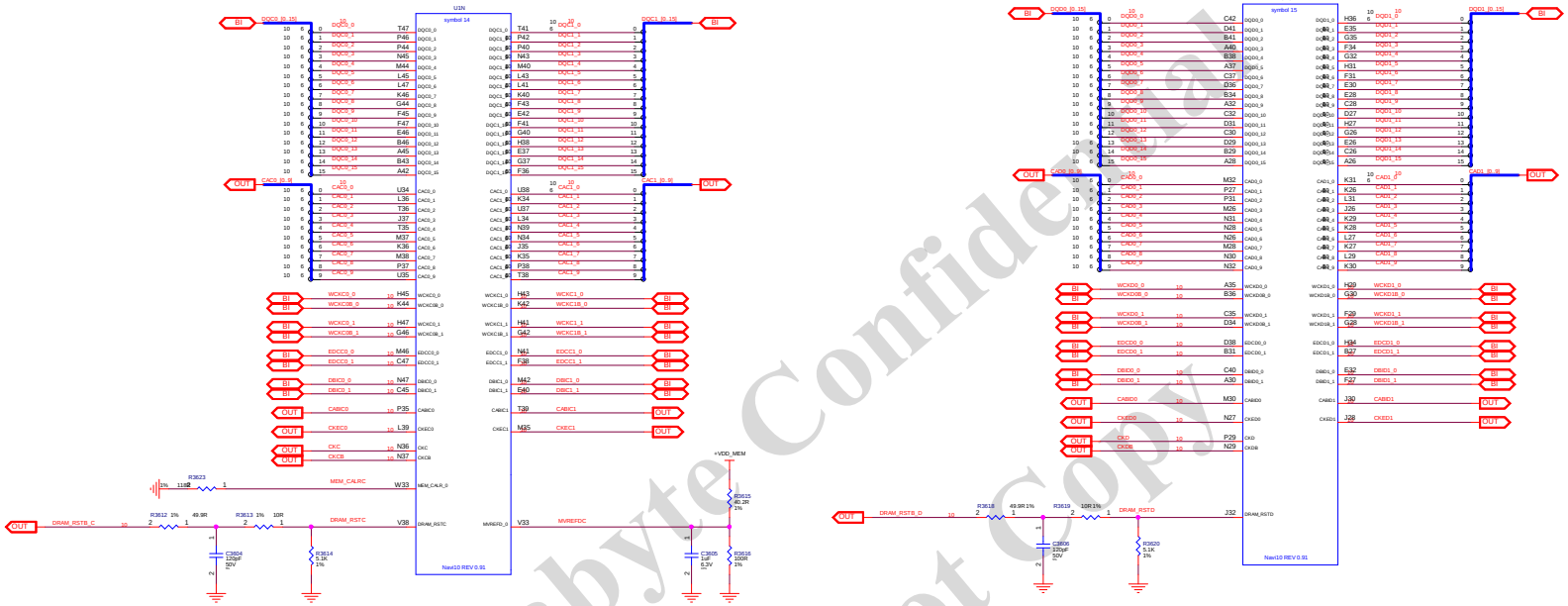

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NAVI 10 MEM INTERFACE CH E/F

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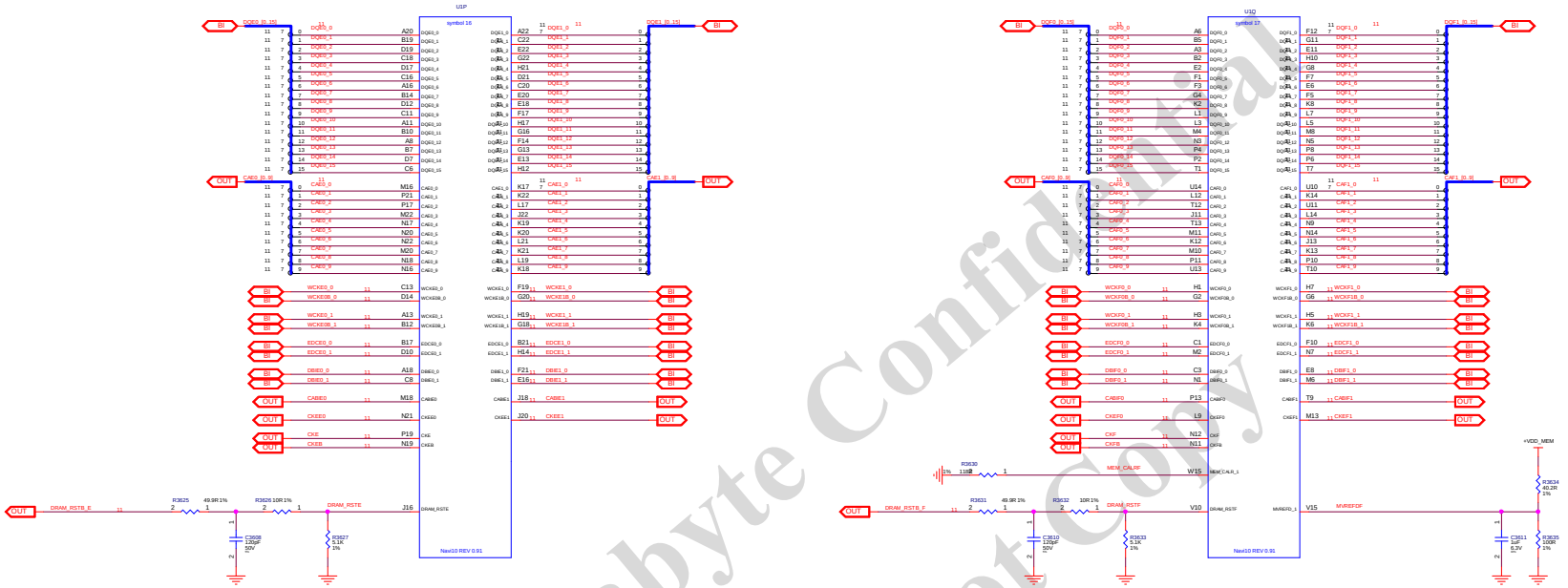

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NAVI 10 MEM INTERFACE CH G/H

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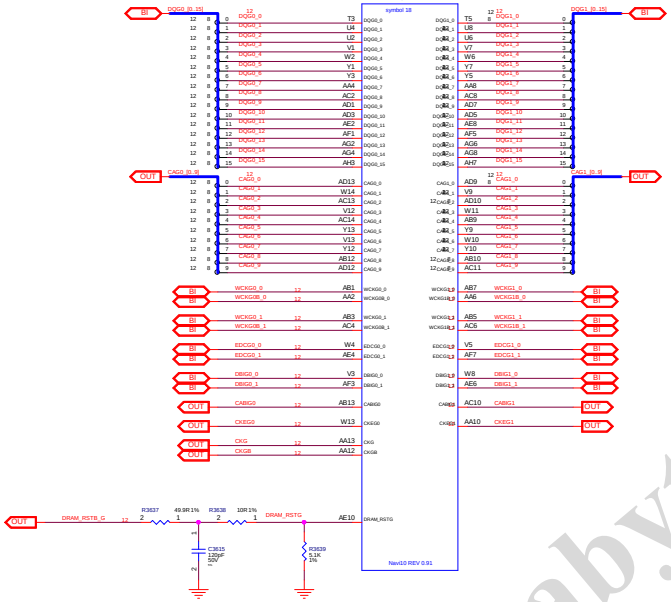

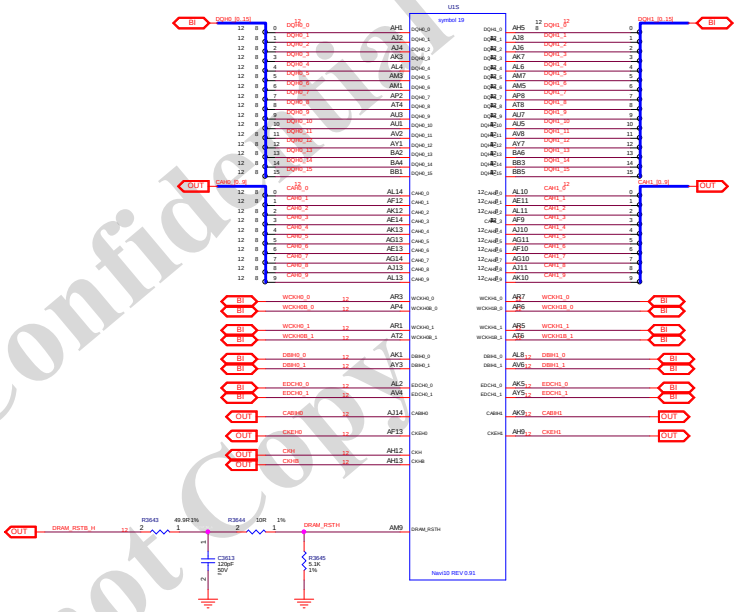

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Title: NAVI 10 CHGH			
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GDDR6x16 CHAB Memory

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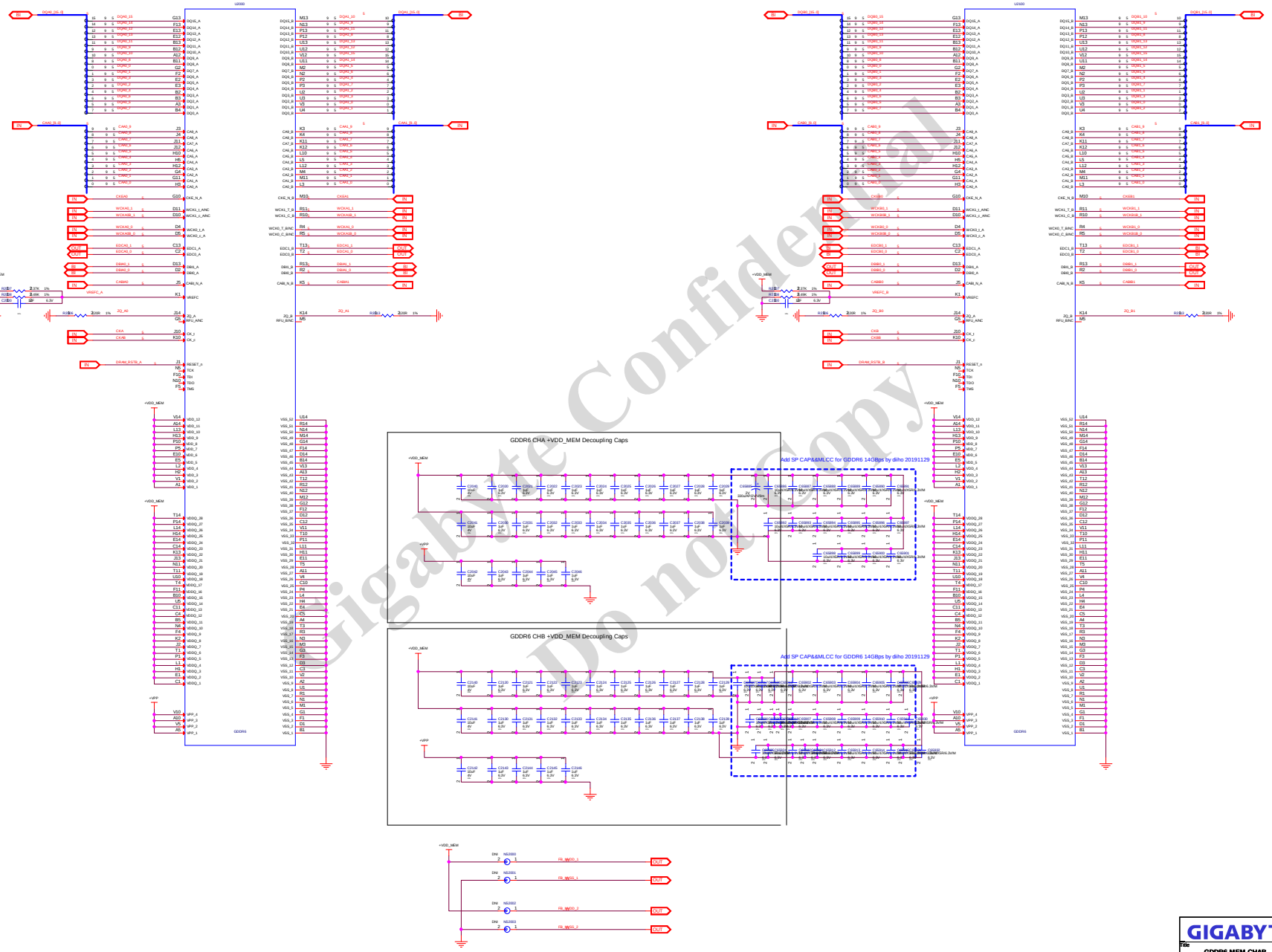

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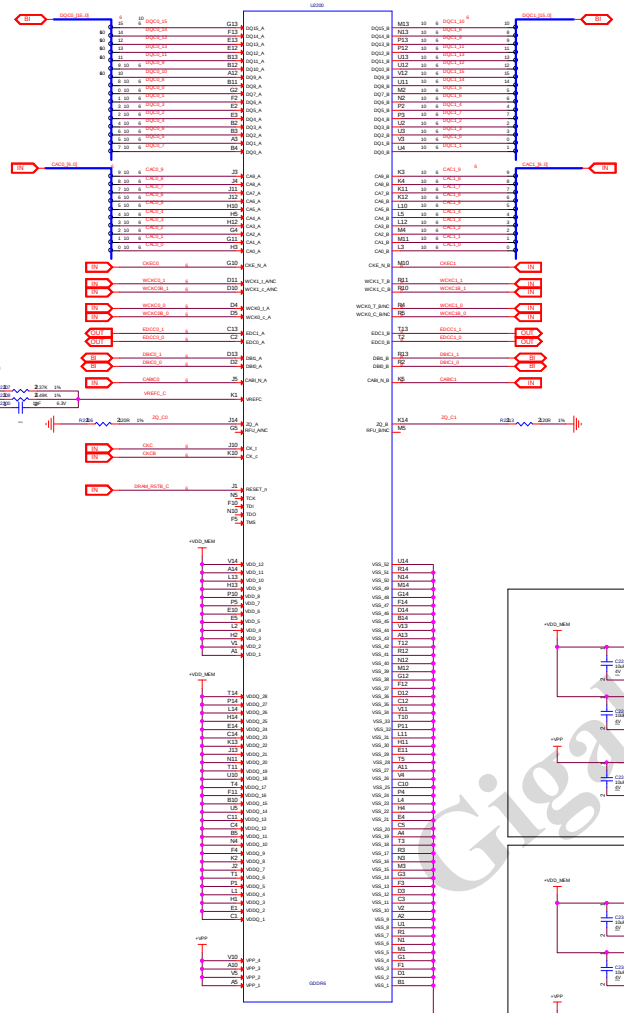

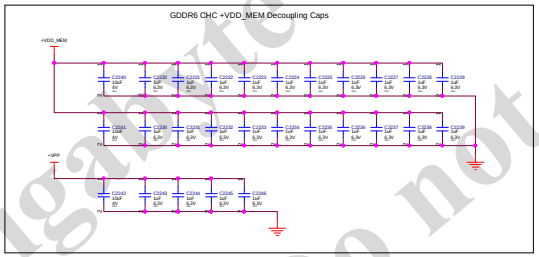

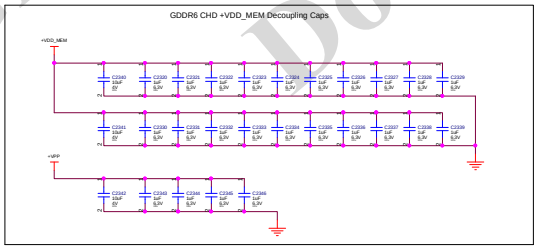

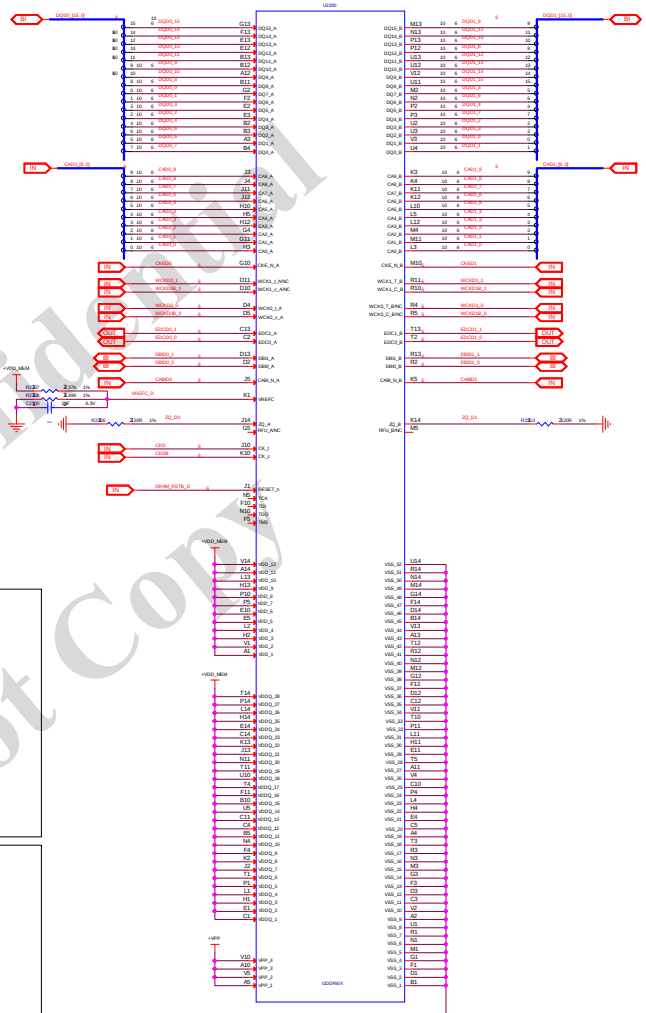

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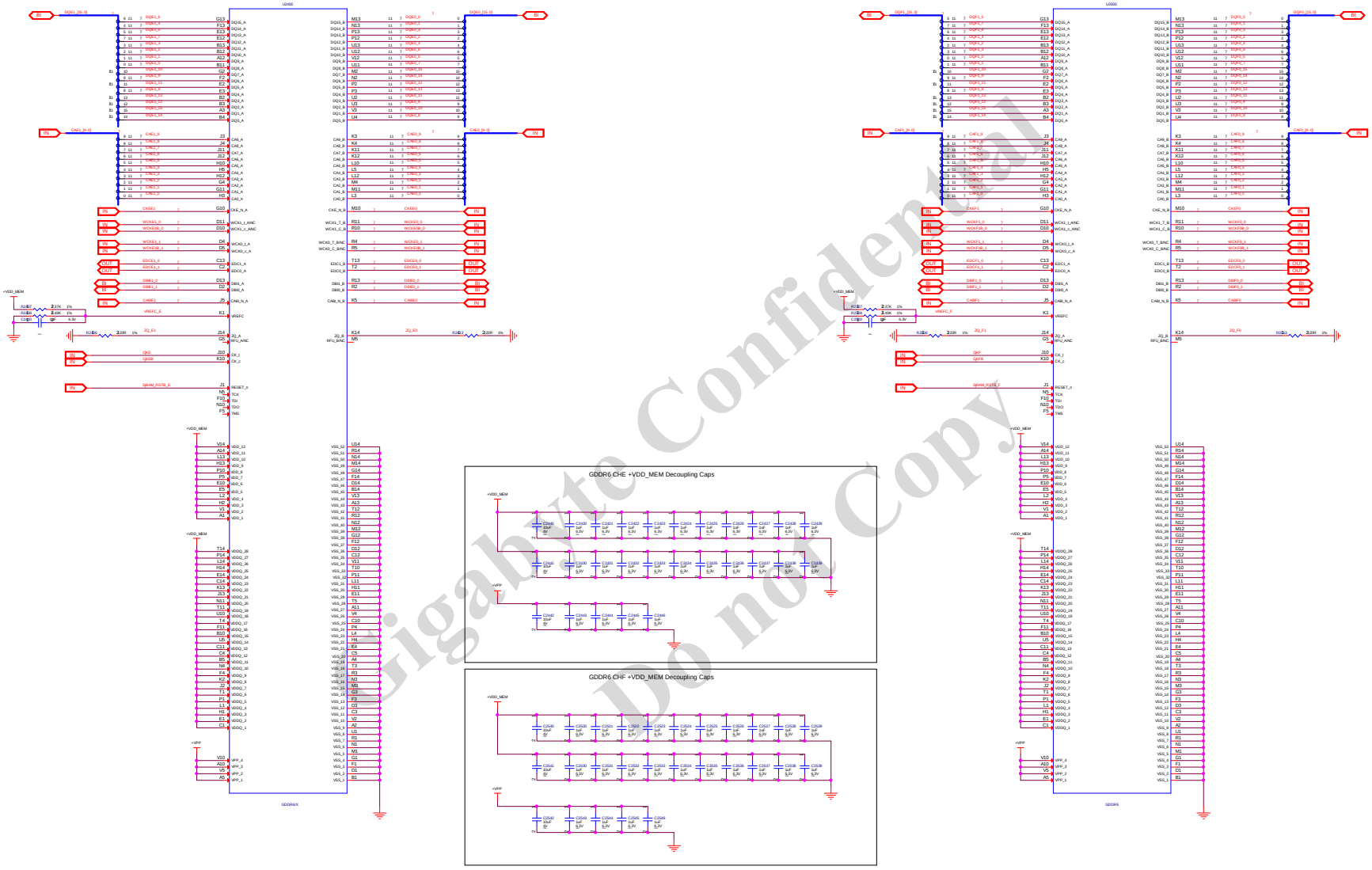

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GDDR6x16 CHGH Memory

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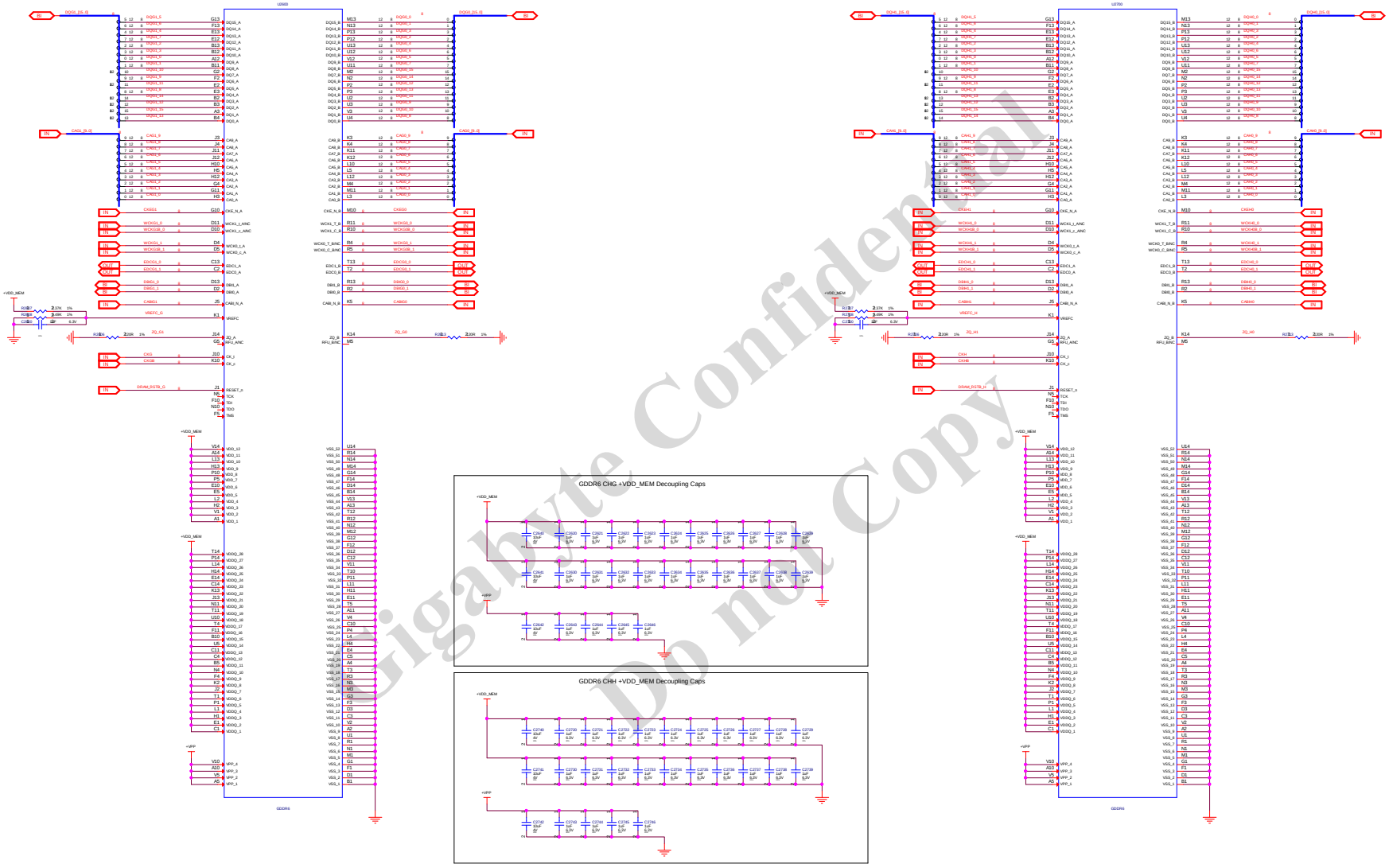

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NAVI10 TMDP A/B

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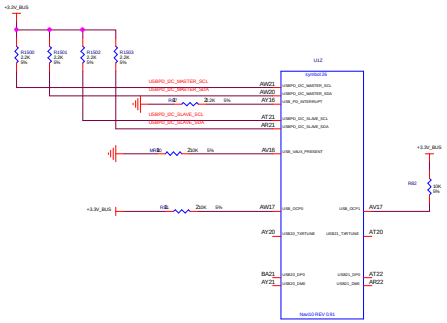

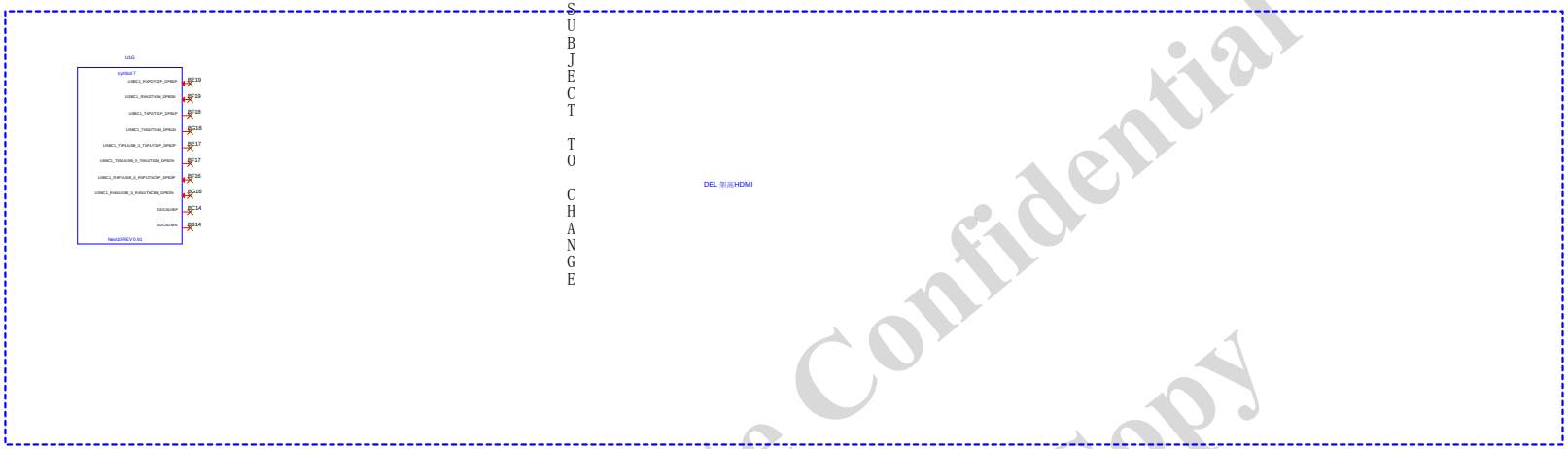

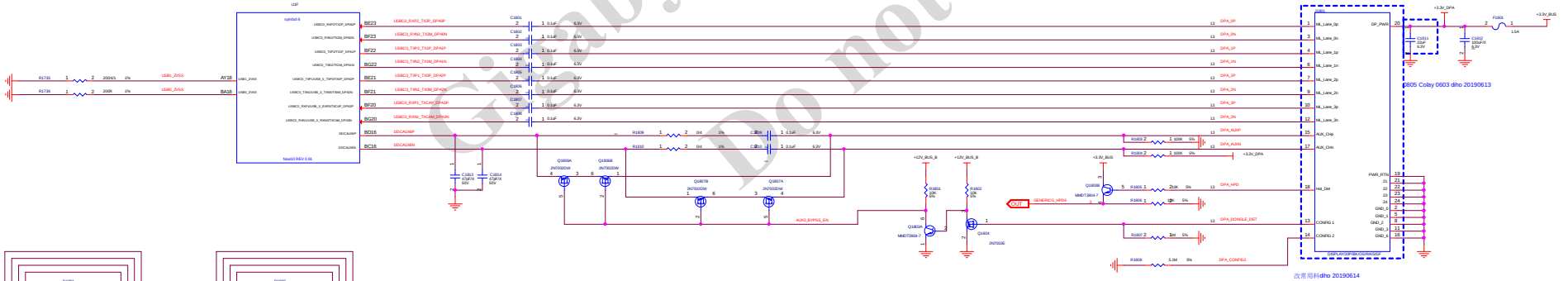

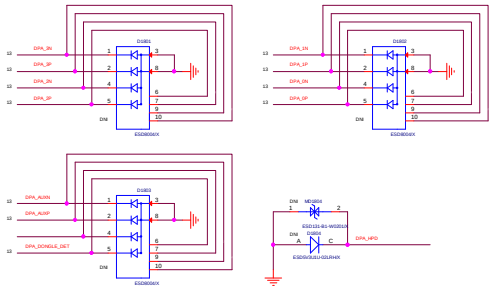

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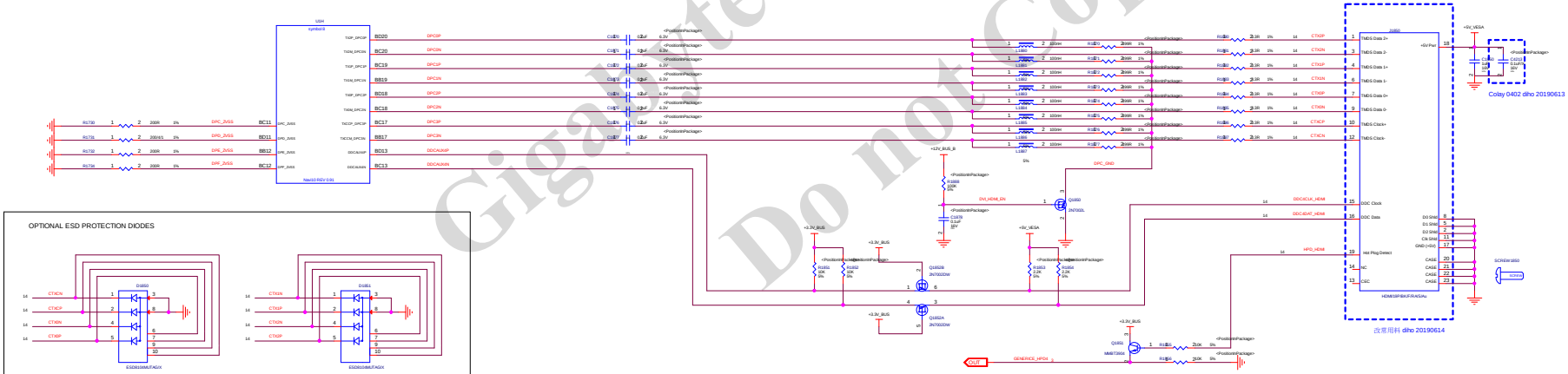
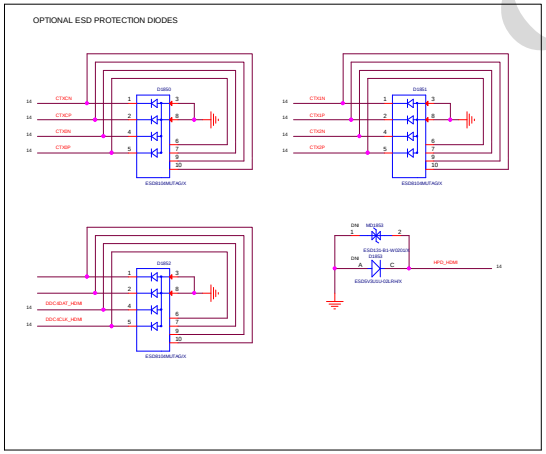
NAVI10 TMDP C/D





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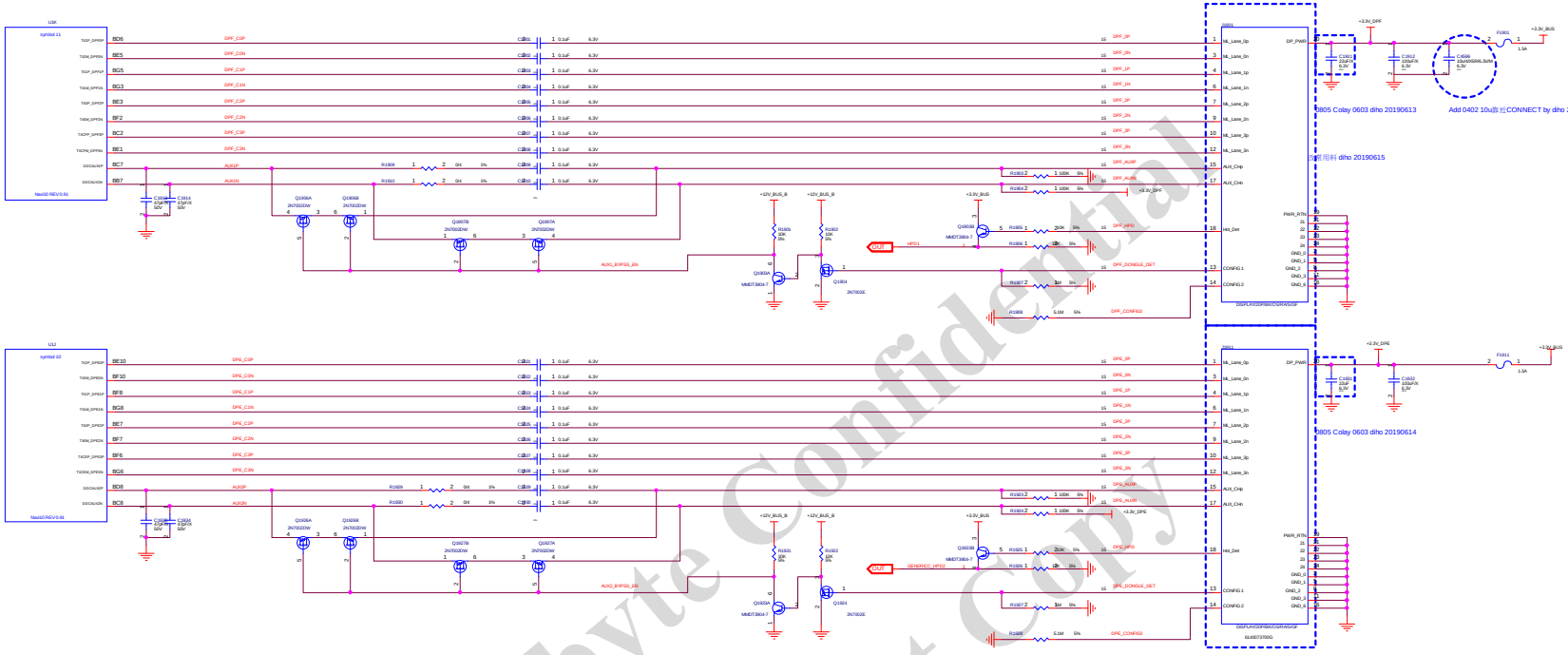
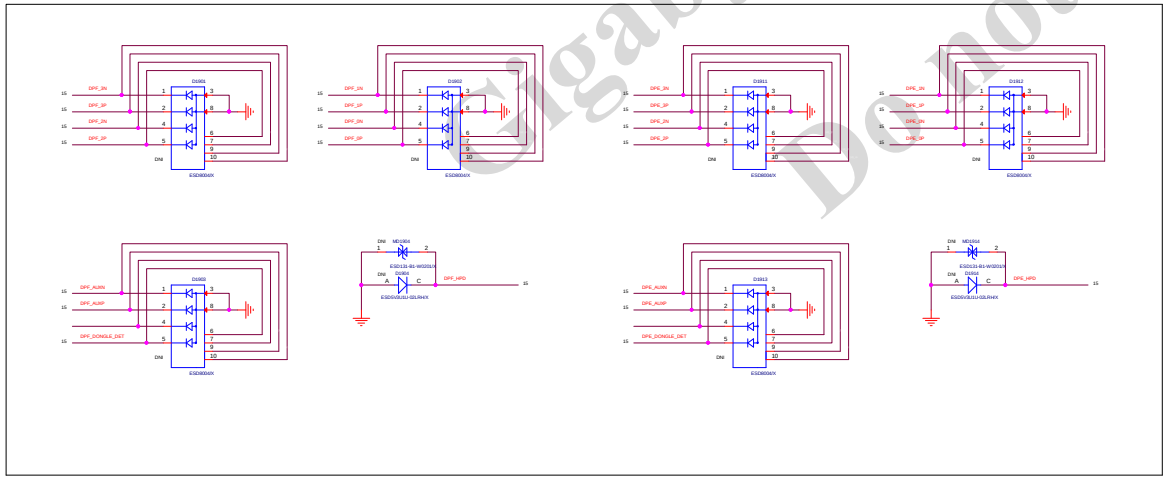
(9) NAVI10 TMDP E/F





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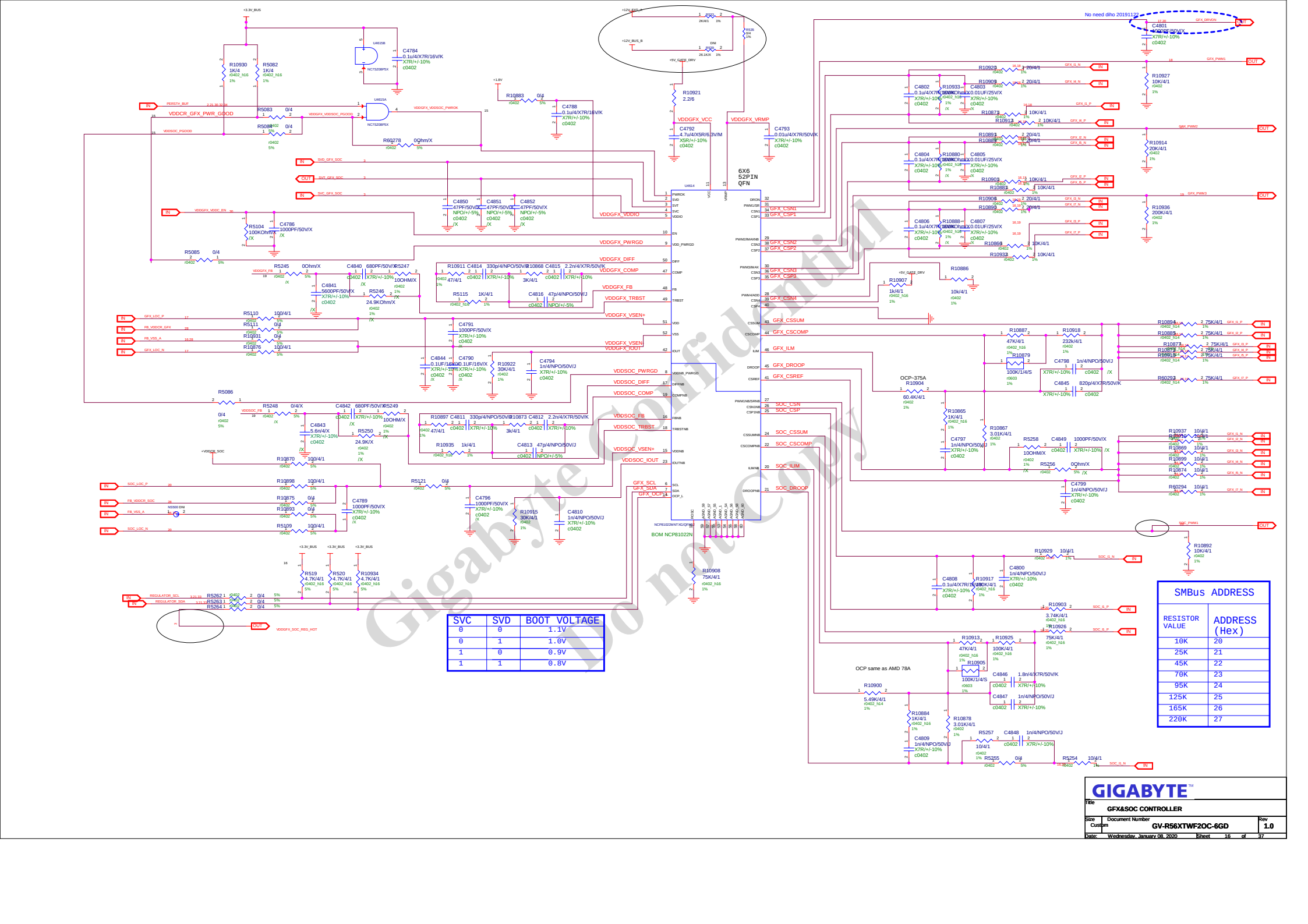
No need dlho 20191122
6X6
52PIN
QFN
U4614
NCP81022MNTXG/QFN52
BOM NCP81022N
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VDDGFX_VCC
VDDGFX_VRMP
VDDGFX_VDDIO
VDDGFX_PWRGD
VDDGFX_DIFF
VDDGFX_COMP
VDDGFX_FB
VDDGFX_TRBST
VDDGFX_VSEN+
VDDGFX_VSEN-
VDDGFX_IOUT
VDDSOC_PWRGD
VDDSOC_DIFF
VDDSOC_COMP
VDDSOC_FB
VDDSOC_TRBST
VDDSOC_VSEN+
VDDSOC_IOUT
GFX_SCL
GFX_SDA
GFX_OCP_L
SOC_CSN
SOC_CSP
SOC_CSSUM
SOC_CSCOMP
SOC_ILIM
SOC_DROOP
GFX_CSSUM
GFX_CSCOMP
GFX_ILM
GFX_DROOP
GFX_CSREF
GFX_CSN1
GFX_CSP1
GFX_CSN2
GFX_CSP2
GFX_CSN3
GFX_CSP3
GFX_CSN4
OCP same as AMD 78A
OCP~375A
SMBus ADDRESS
RESISTOR VALUE
ADDRESS (Hex)
10K 20
25K 21
45K 22
70K 23
95K 24
125K 25
165K 26
220K 27
SVC SVD BOOT VOLTAGE
0 0 1.1V
0 1 1.0V
1 0 0.9V
1 1 0.8V
GIGABYTE
GFX&SOC CONTROLLER
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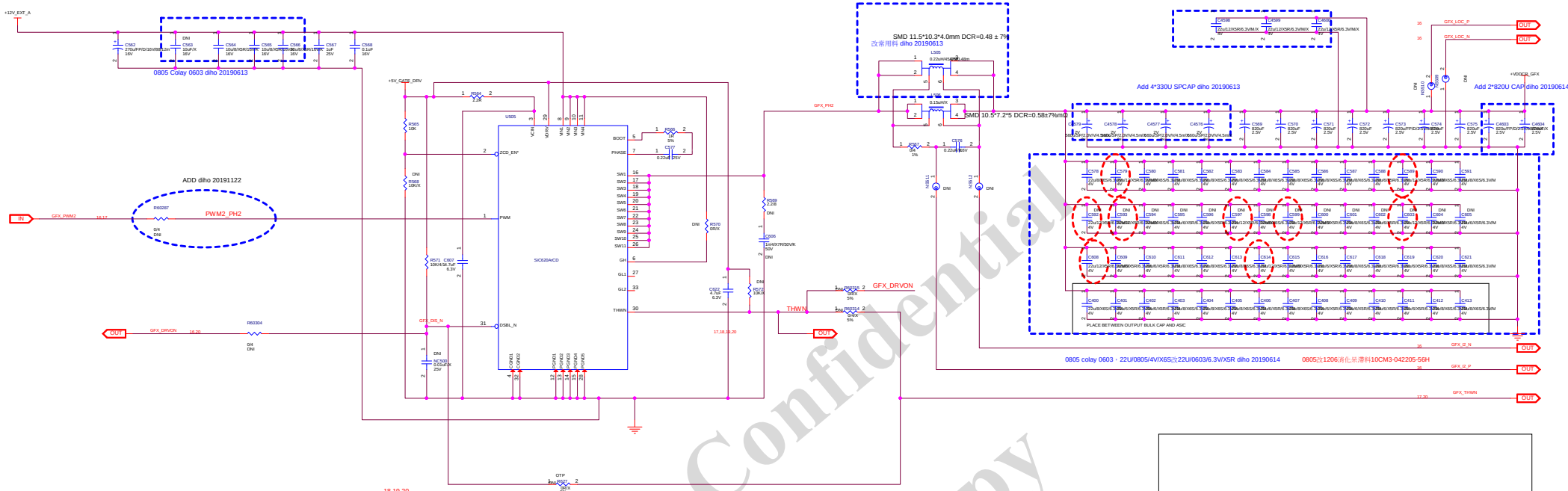

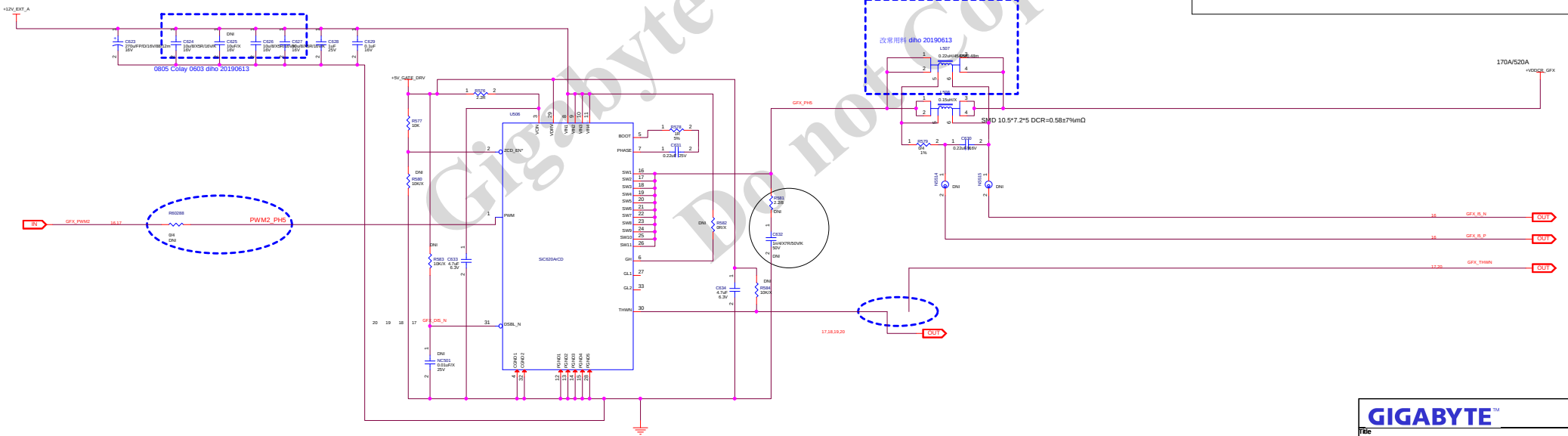

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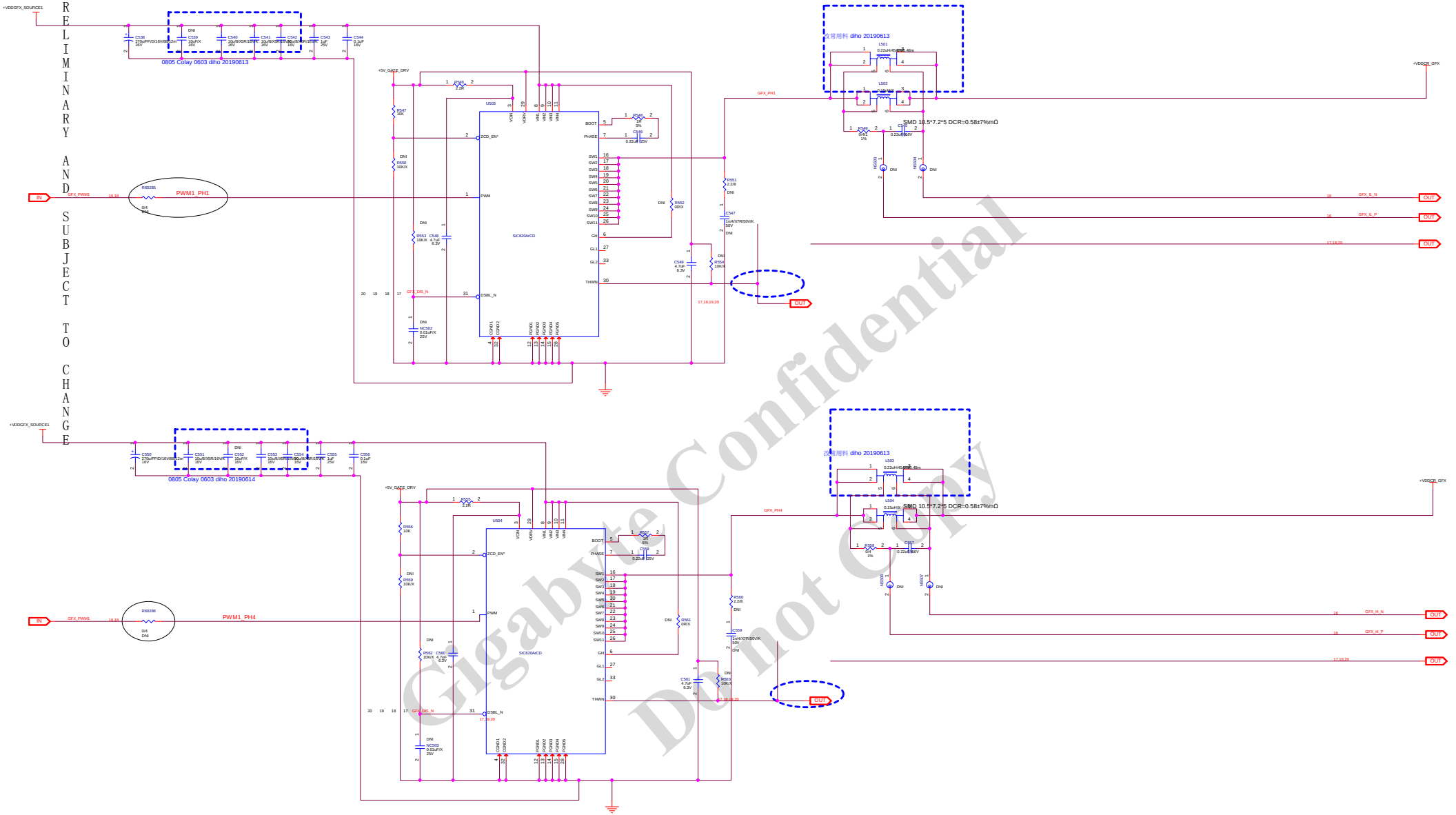

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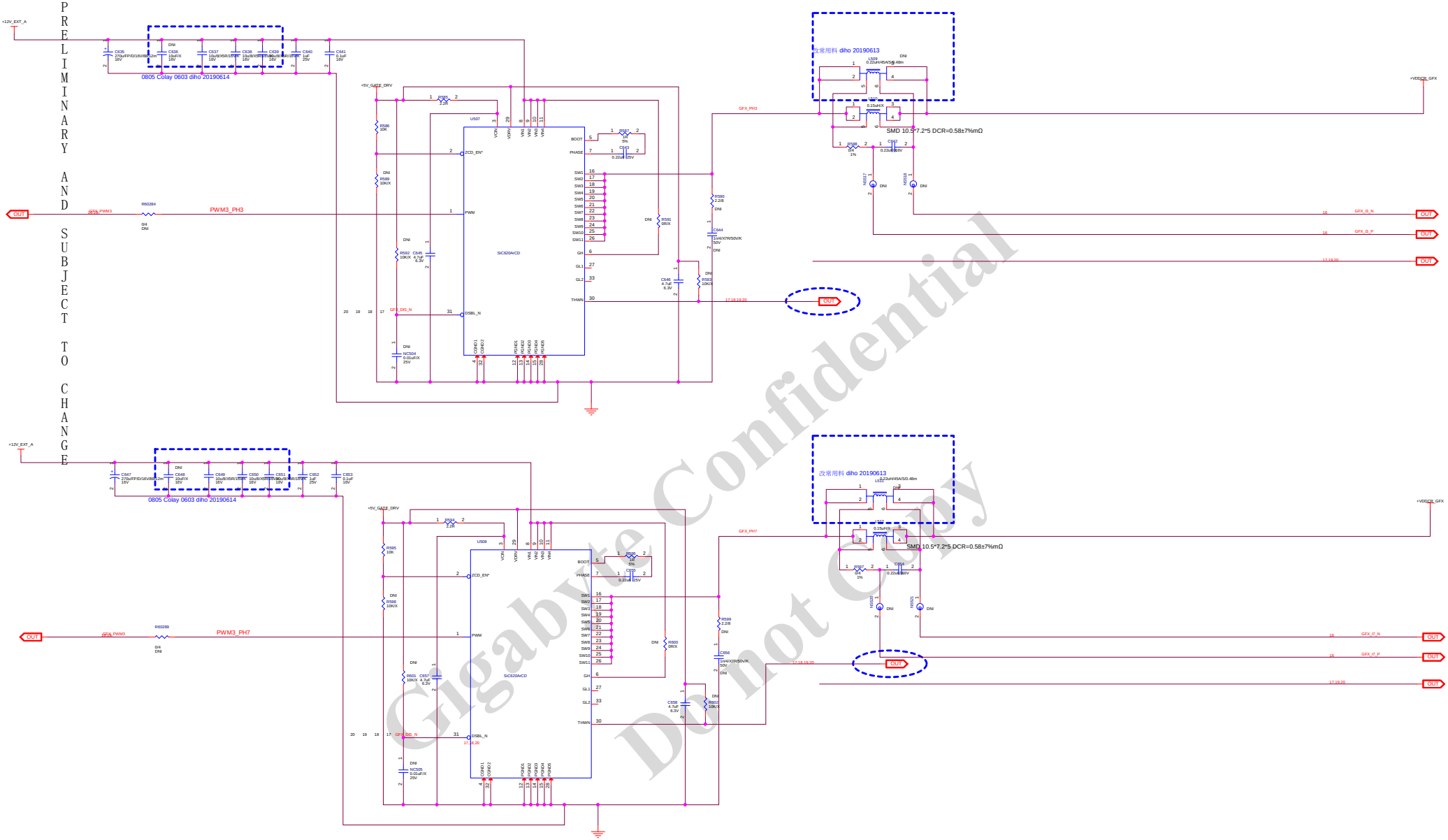

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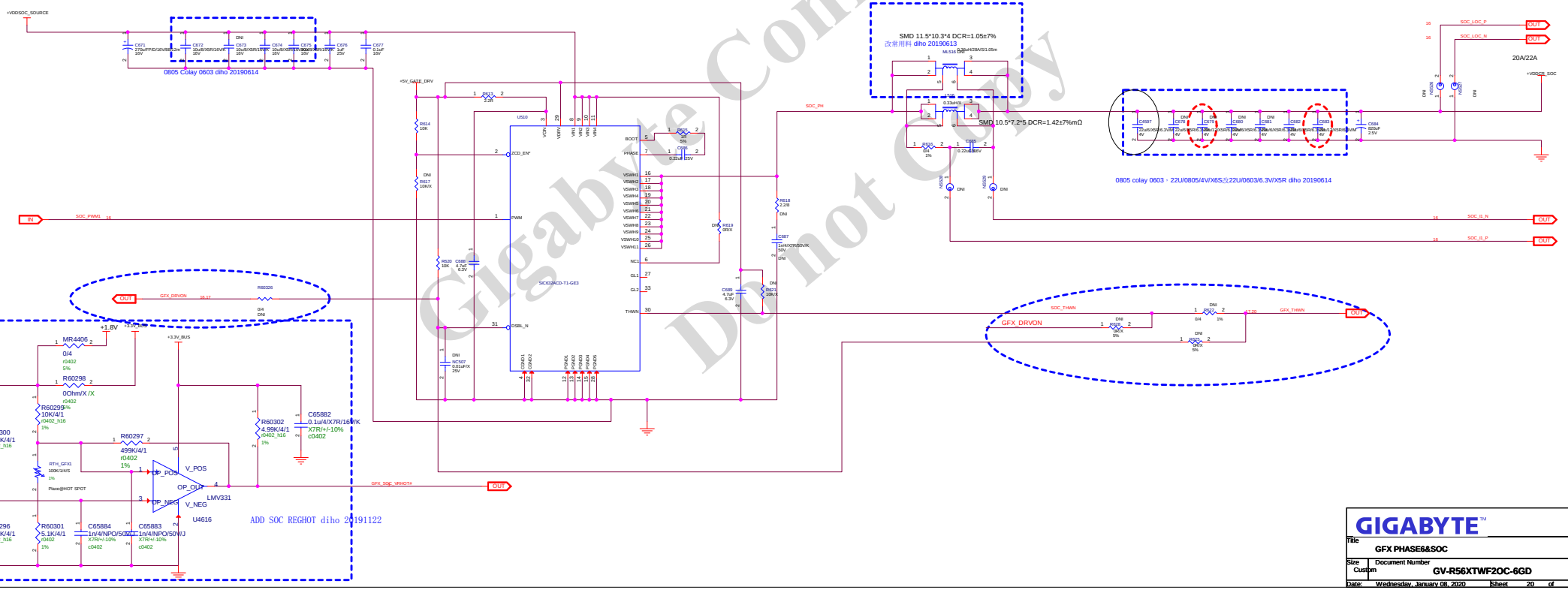

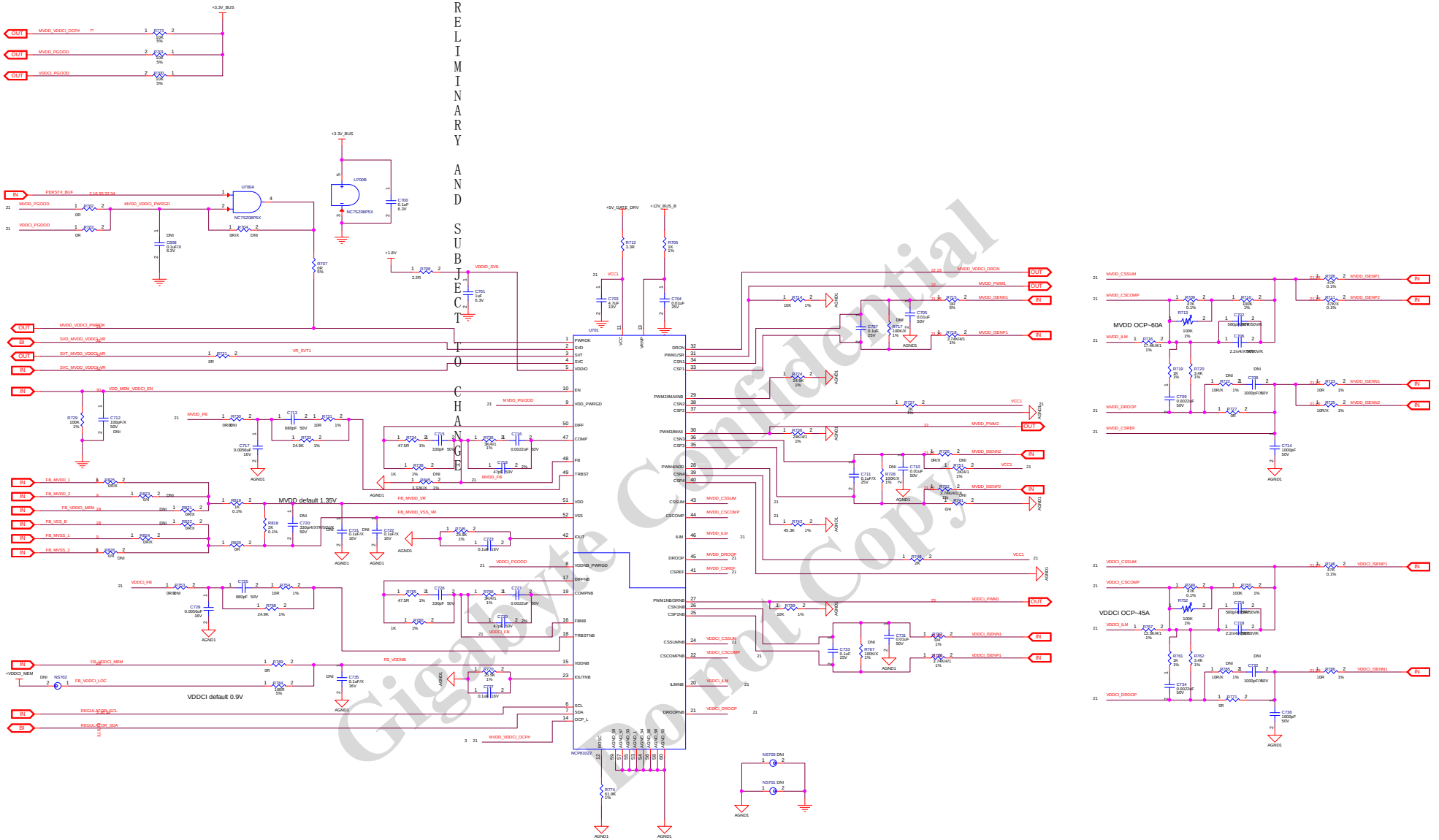

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Title	MVDD&VDDCI CONTROLLER	
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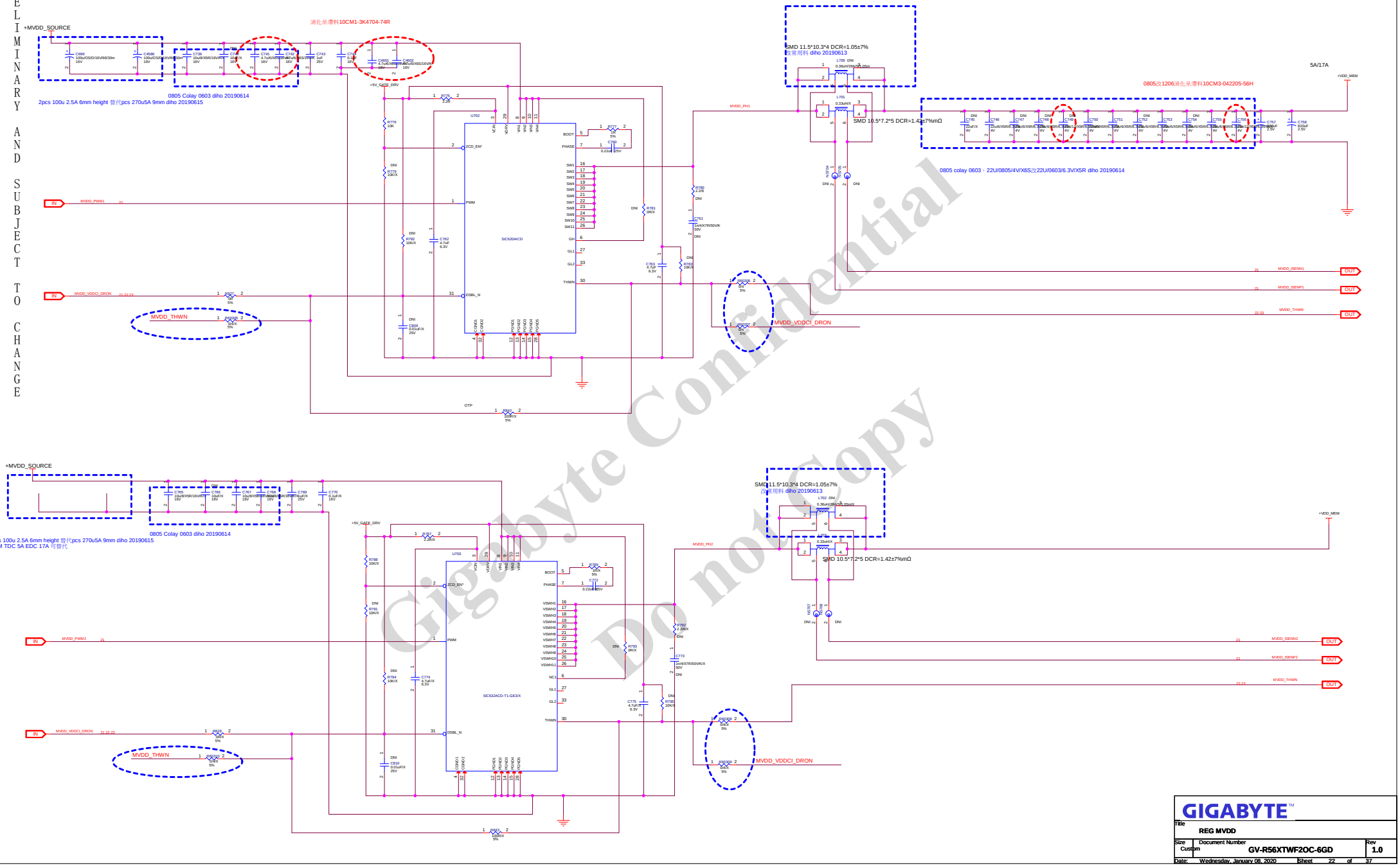

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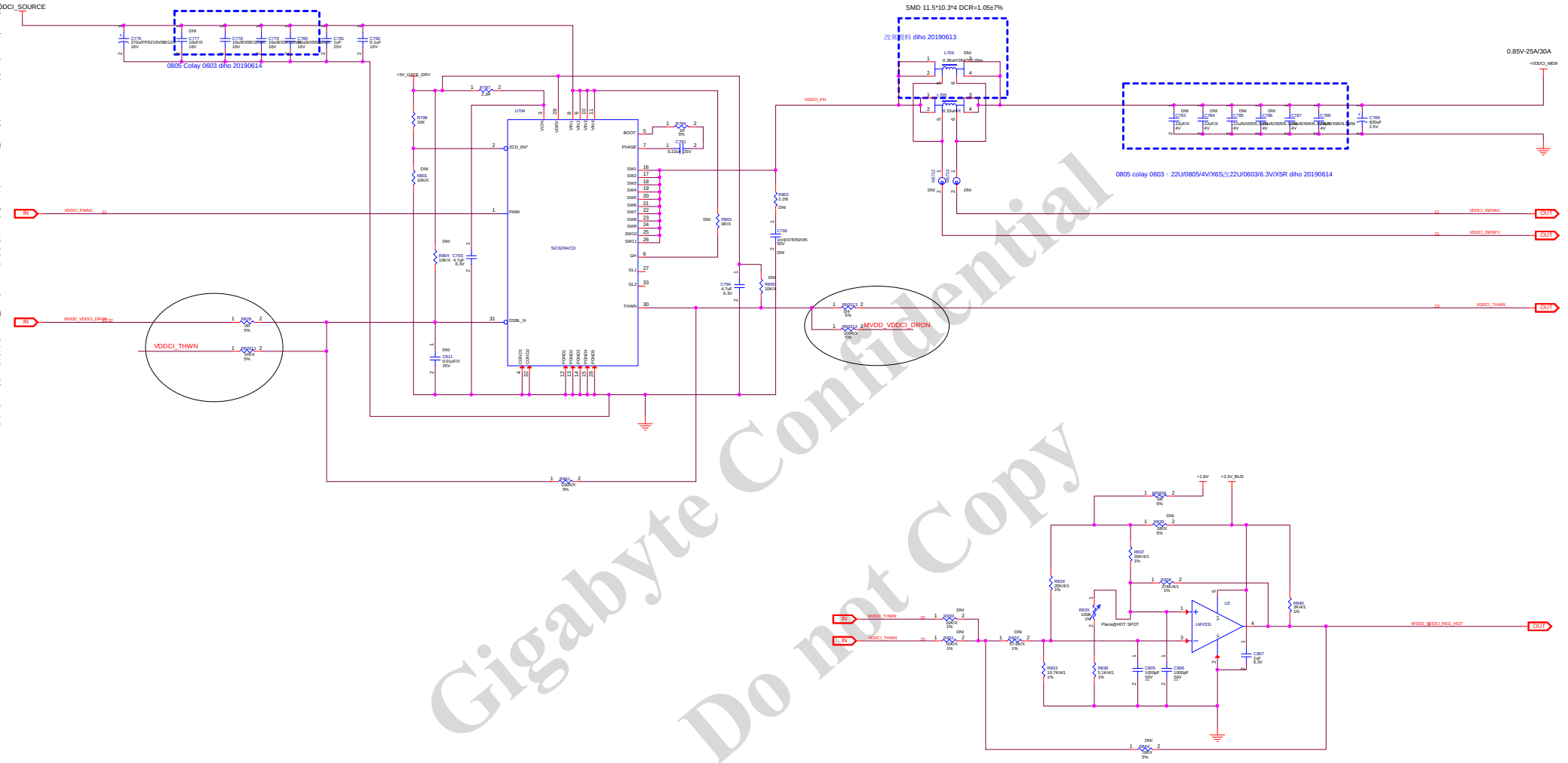

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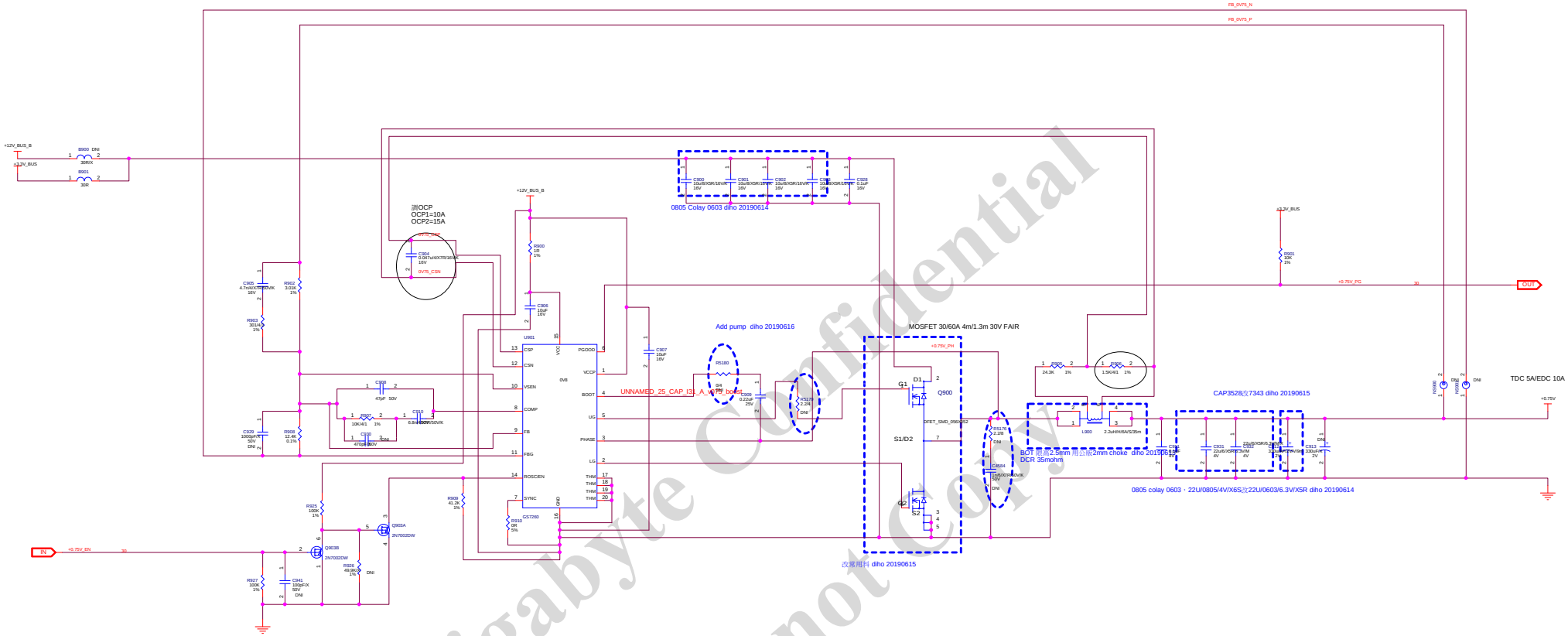

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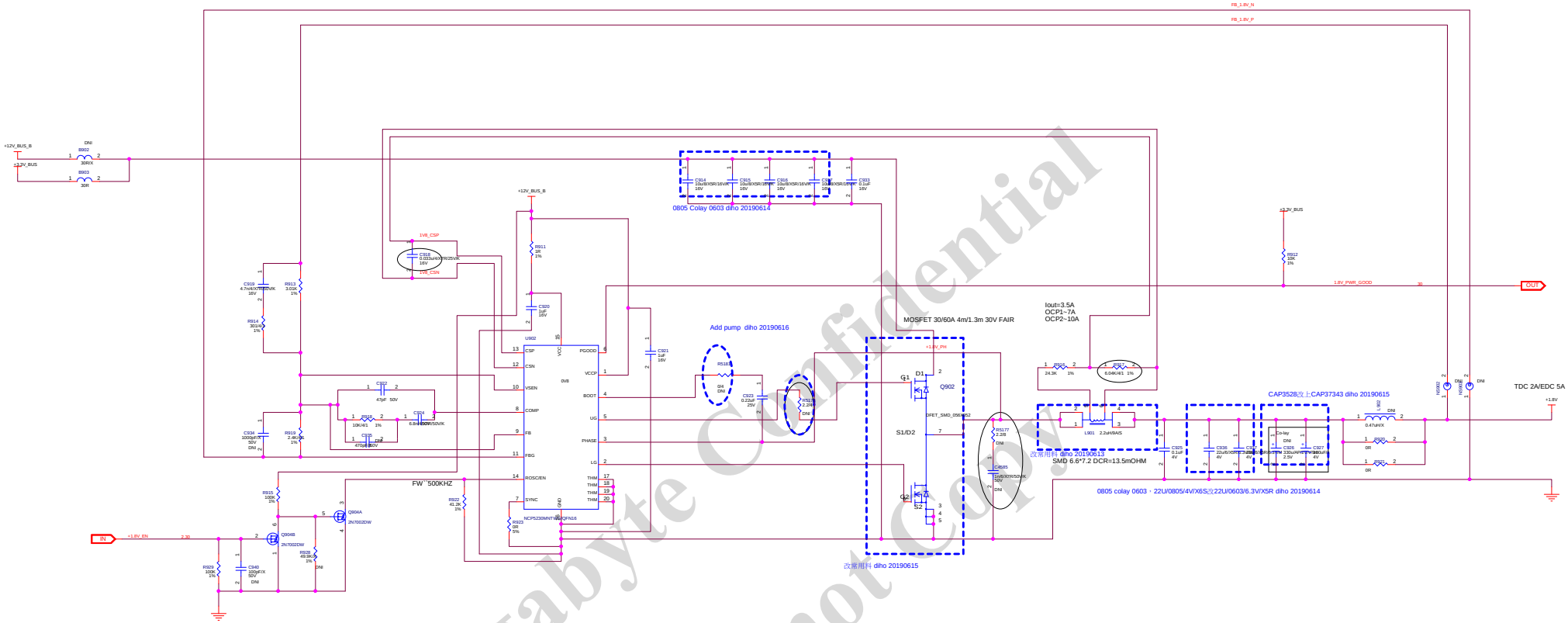

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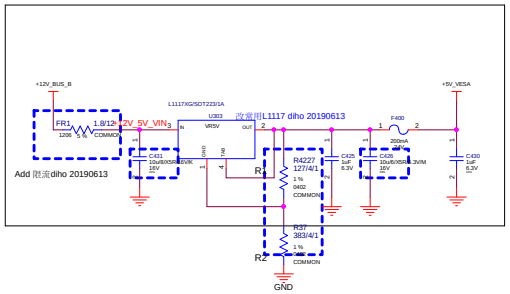
REGULATOR FOR +5V RAILS

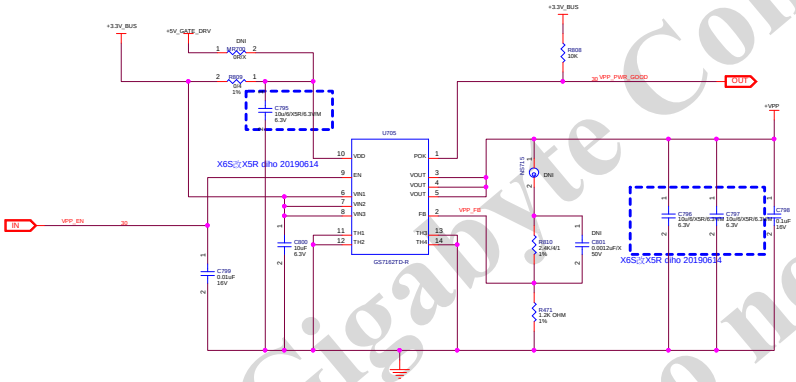
IOUT = 50mA



VOUT = 1.25X(1+R2/R1)

= 1.25 X (1 + 383/127)

= 5.02V



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Title: SMALL RAIL REGULATOR		
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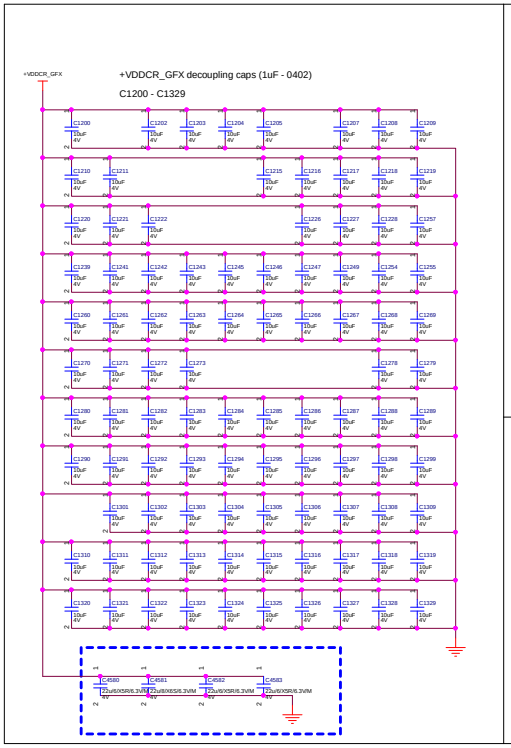
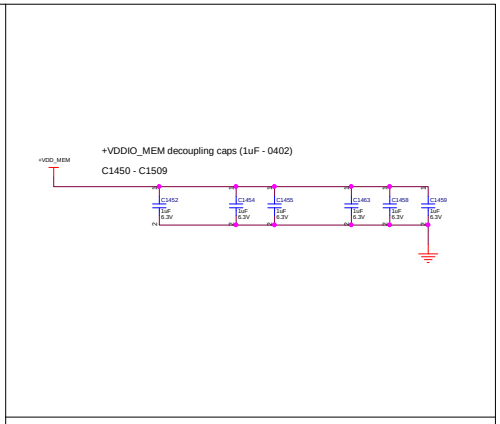
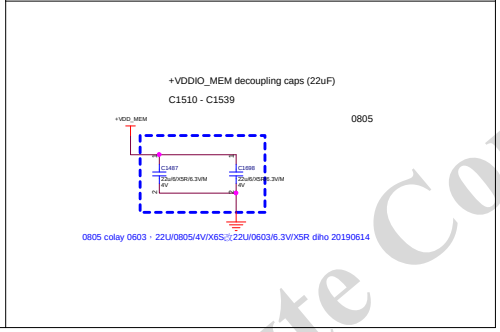
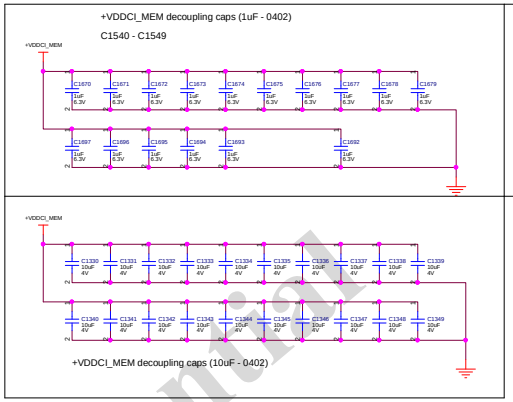
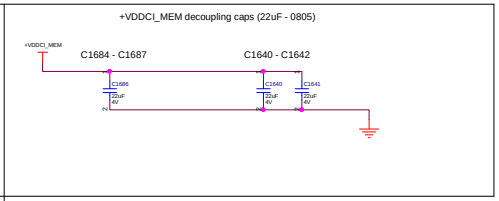
PRELIMINARY AND SUBJECT TO CHANGE

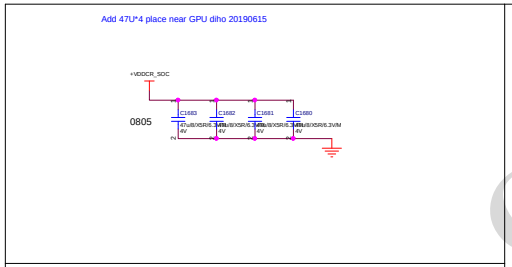


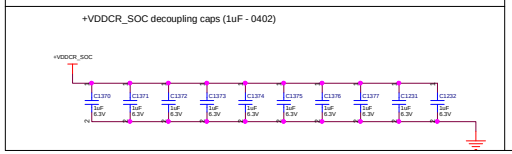


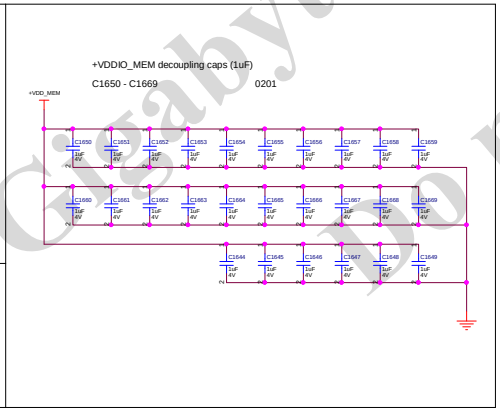












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Title: NAVI 10 DECAPS		
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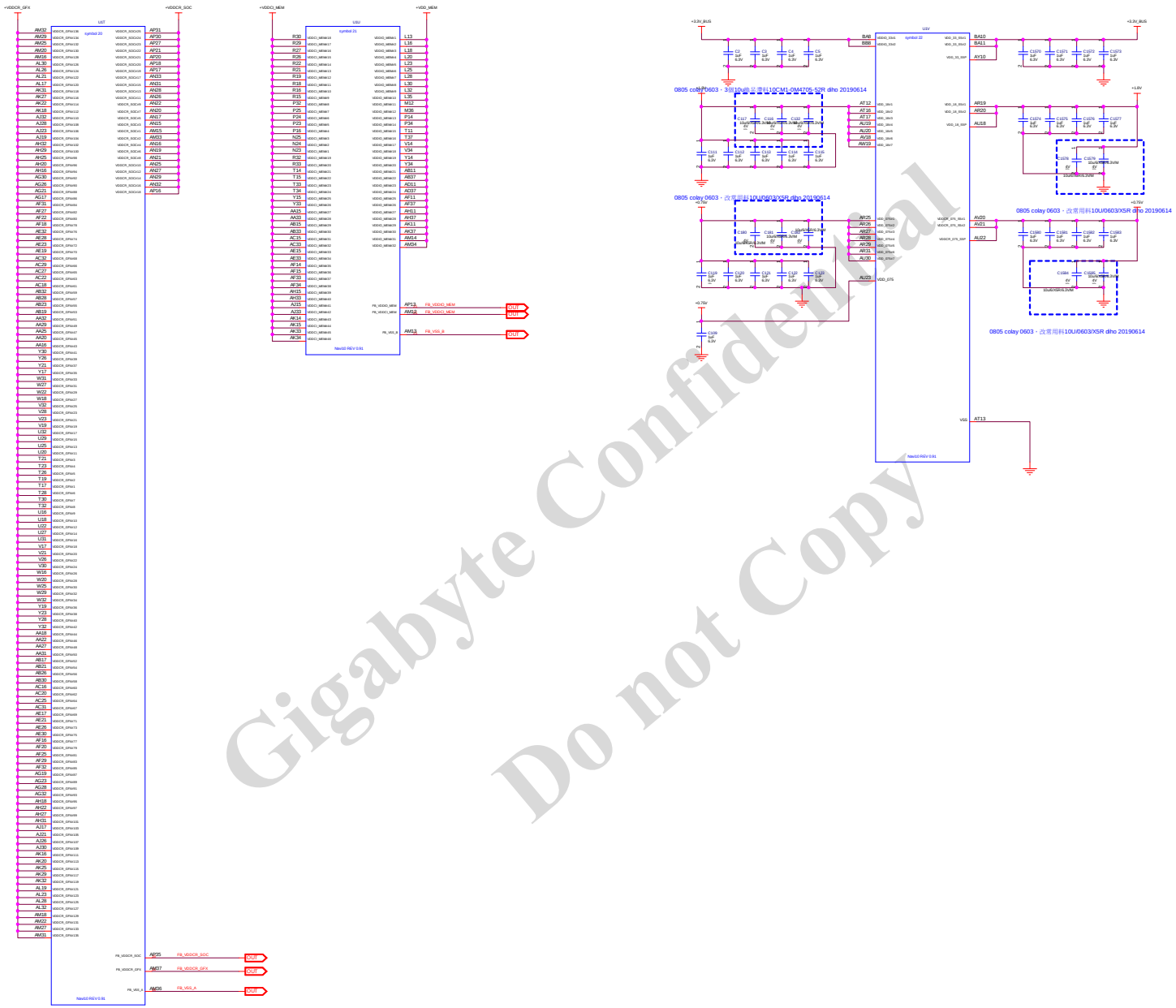

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Title	NAVI 10 POWER	
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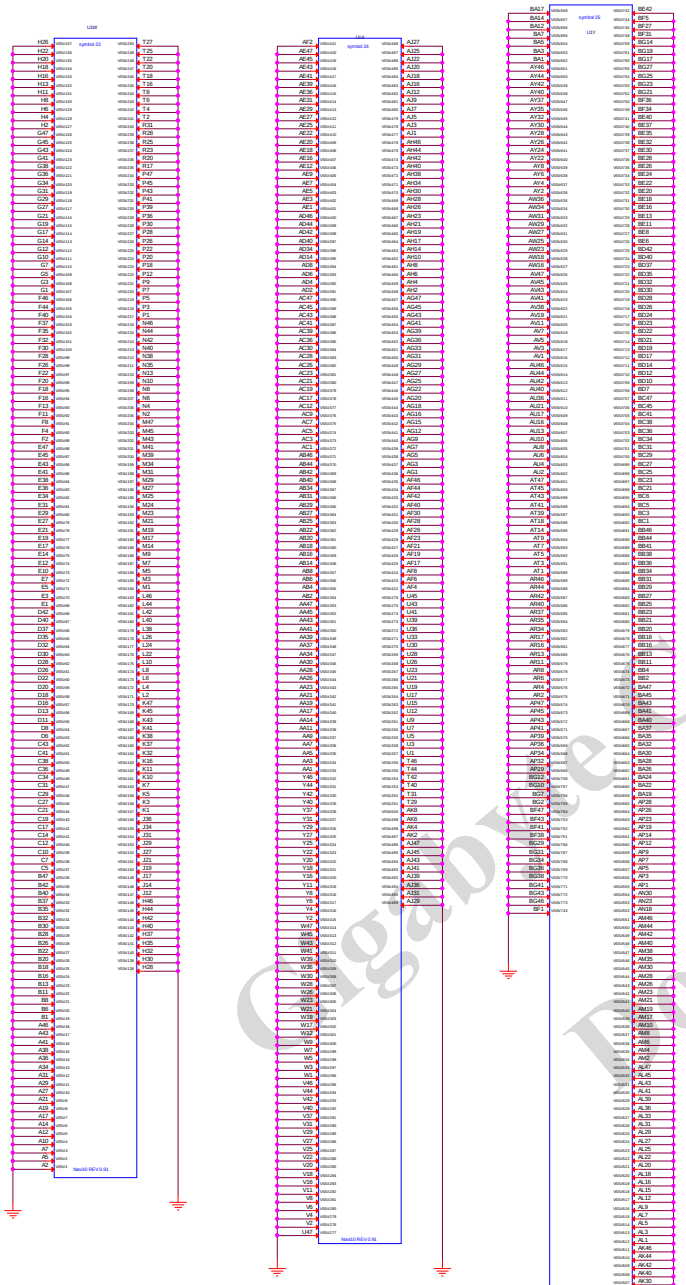

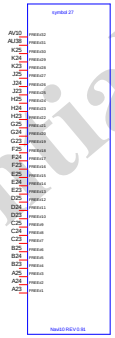

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Title	NAVI 10 GND	
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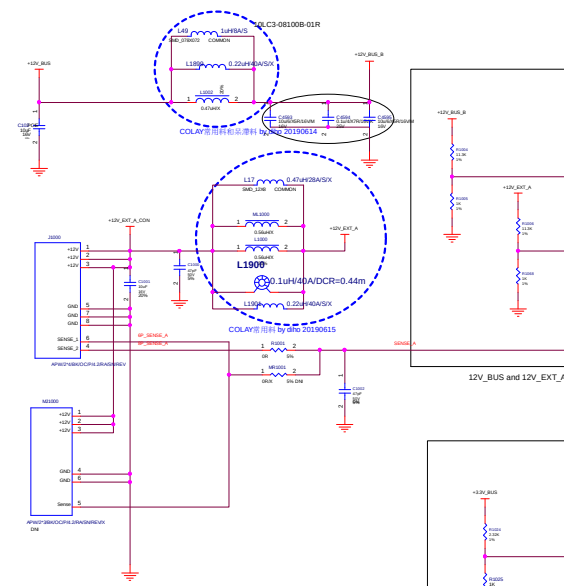

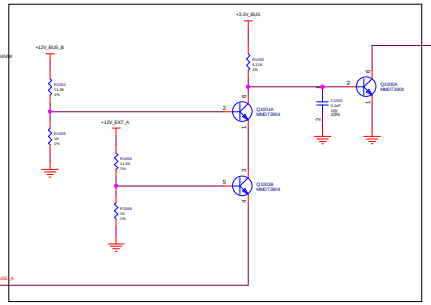

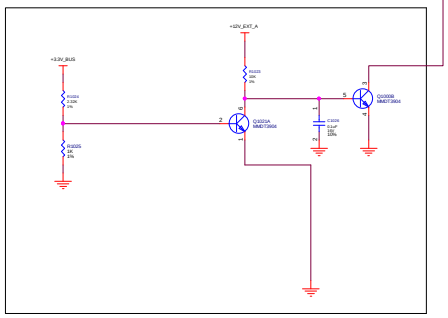

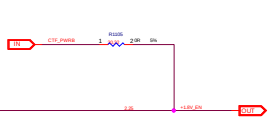

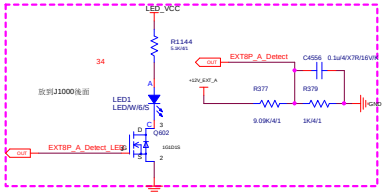

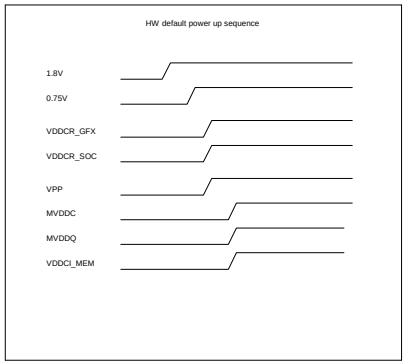

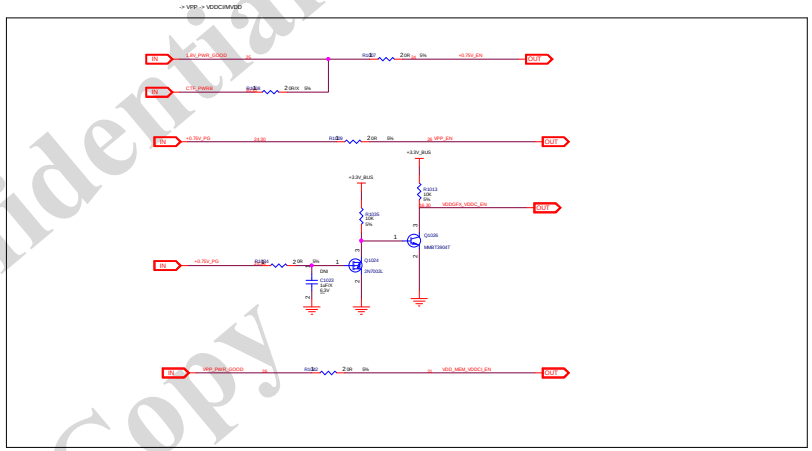

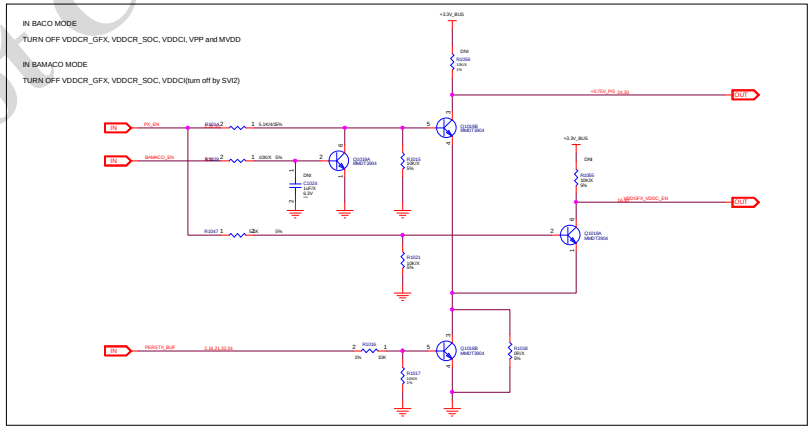

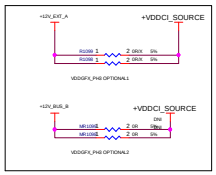

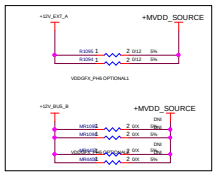

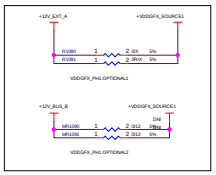

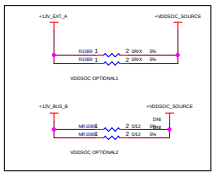

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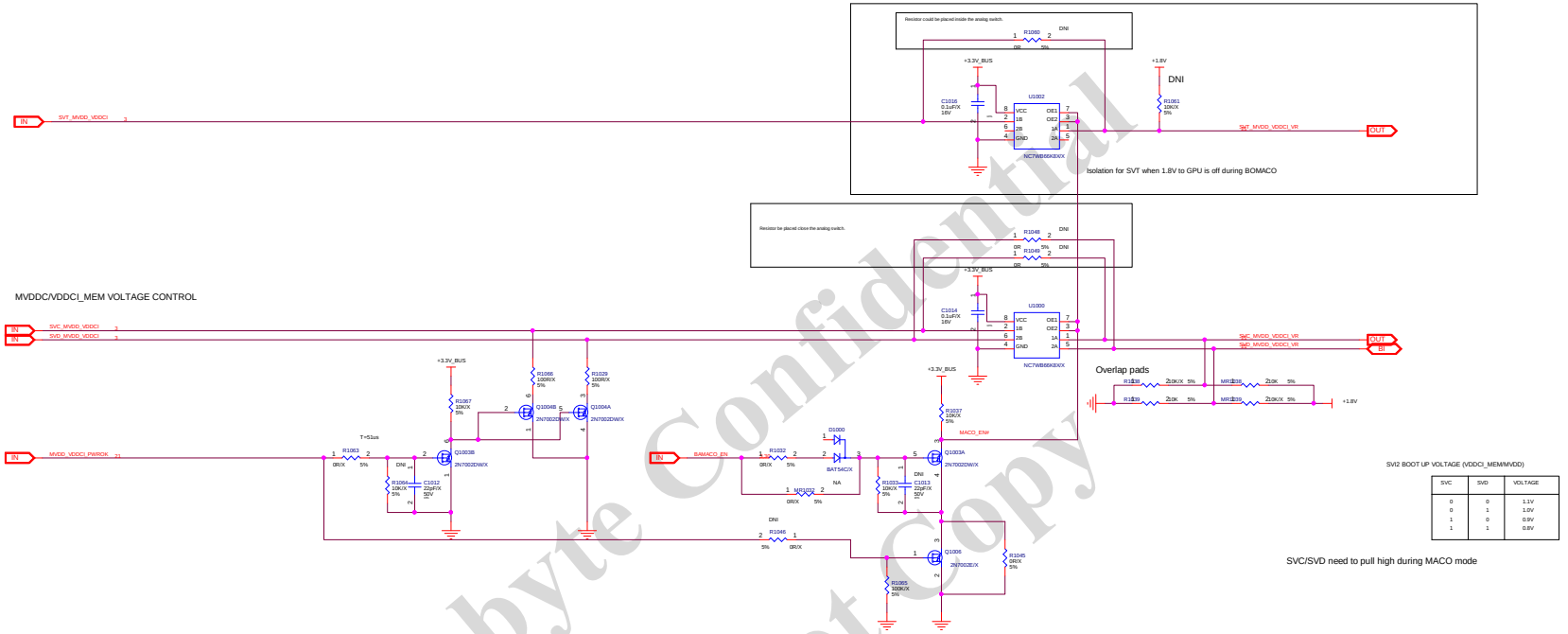

SVI2 BOOT UP VOLTAGE (VDDCI_MEM/MVDD)

SVC	SVD	VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

SVC/SVD need to pull high during MACO mode

GIGABYTE™

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PRELIMINARY AND SUBJECT TO CHANGE

BKT SINK

改常用螺絲孔 by diho 20190619

GPU SINK

BOARD STIFFENER

MEC33 MEC20 MEC21 MEC26 MEC16 MEC23 MEC27 MEC24 MEC28 MEC25 MEC29 MEC12 MEC17 MEC18 MEC31 MEC19 MEC22 MEC30

MH-C2SED125-10 COMMON

MH-C2SED119-10 COMMON

9 connected mounting pins

GND

DEL EXT_B By diho 20191126

update value follow amd 0714

change back follow amd 0719

For 4-WIRE FAN ONLY

LM96 external GPU temperature sensor

Fan Connector

colay 0805&0603 diho 20190613

Add Offpage by diho 20190616

MOS SINK

BK

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GIGABYTE

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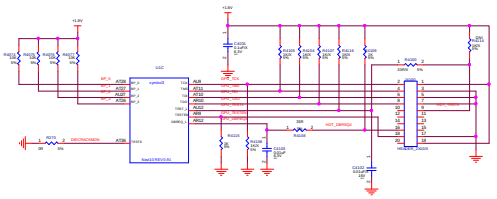
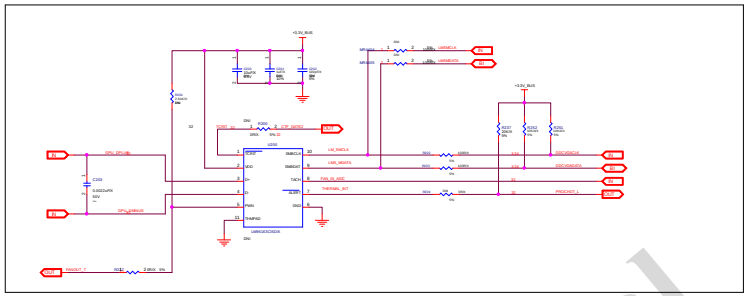
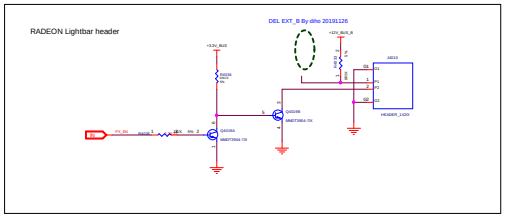
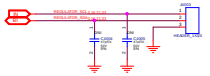
PRELIMINARY AND SUBJECT TO CHANGE



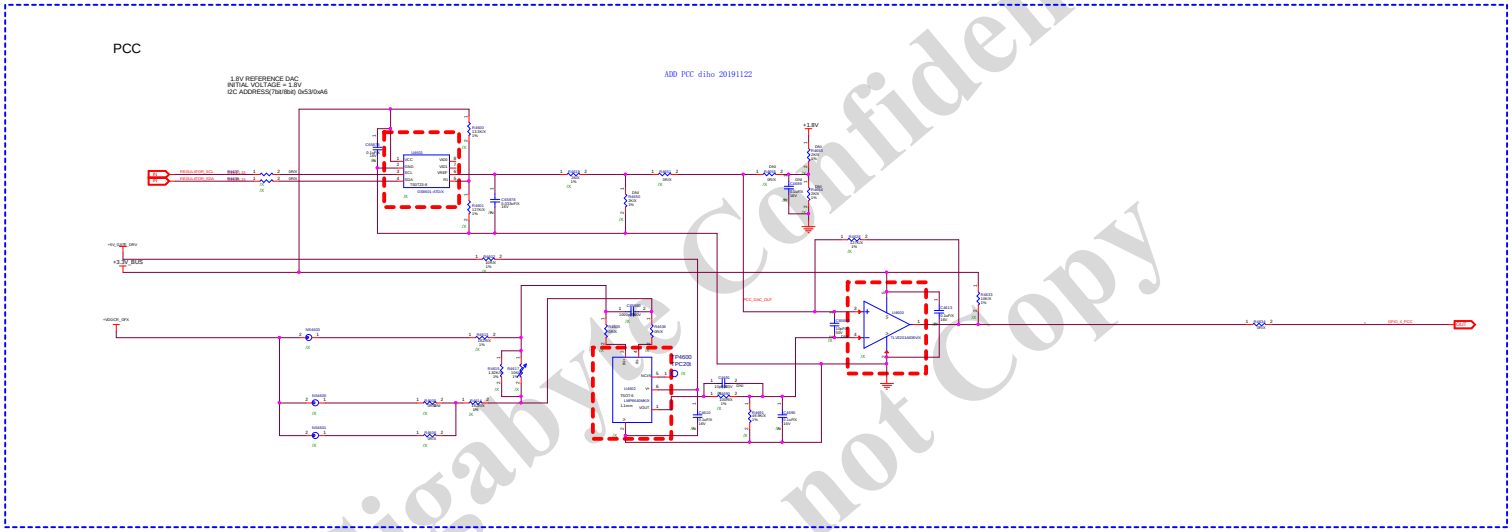






PCC

ADD PCC diho 20191122



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File: DEBUG

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Custom

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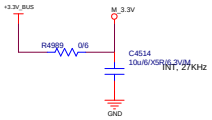
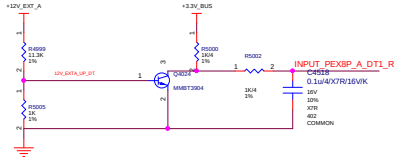
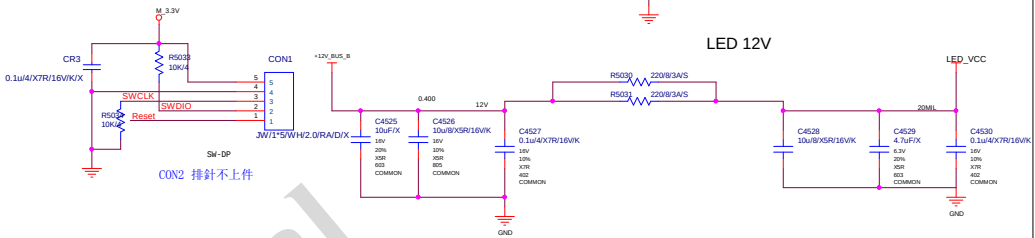
ADD Page35: LED Control MCU circuit by diho 20190619

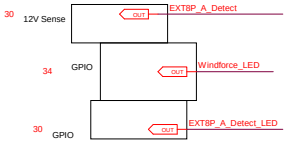




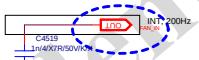
LED 12V



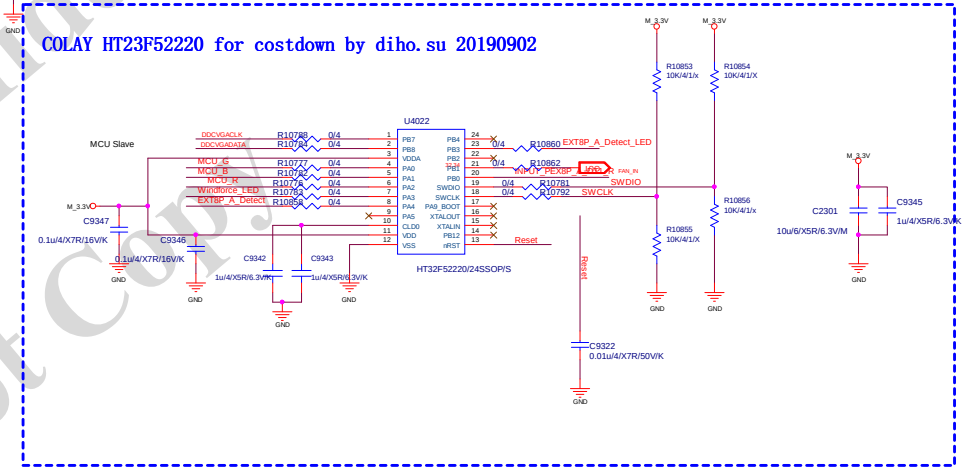
DEL MCU HT50241 By diho 20191126

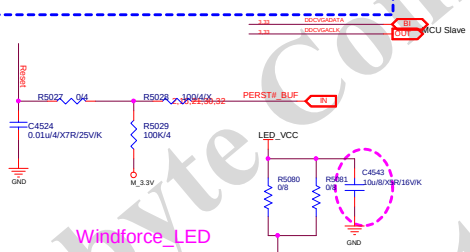


FAN Stop LED

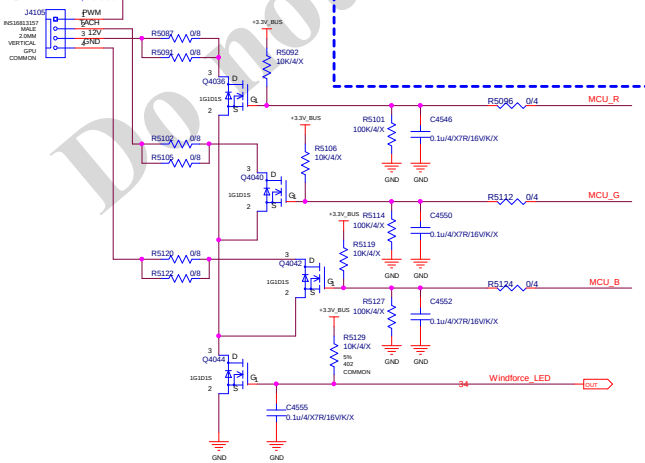


COLAY HT23F52220 for costdown by diho.su 20190902





Windforce_LED



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Title: MCU		
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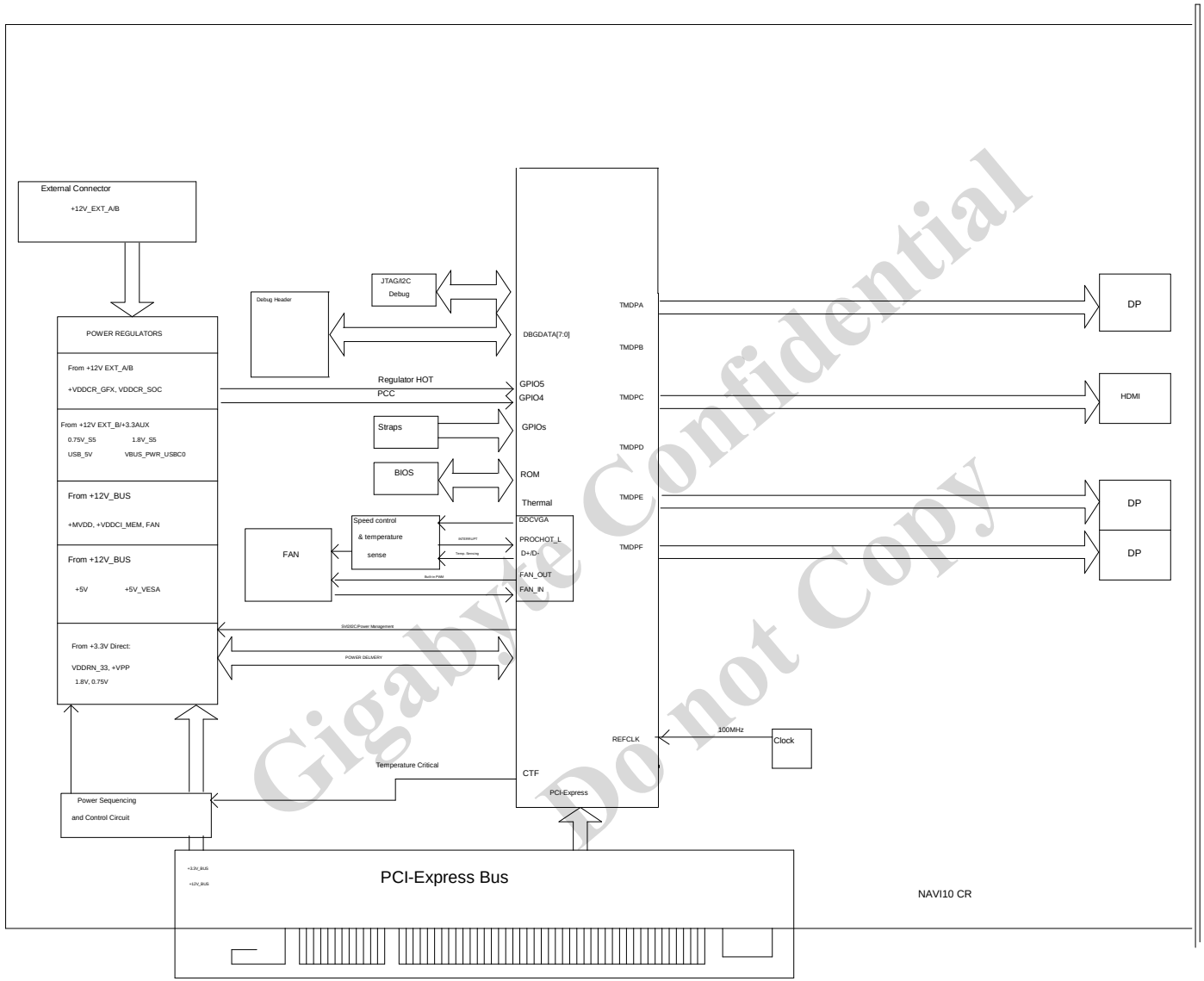

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1	-00A	FEB 11 2019	-00A schematics

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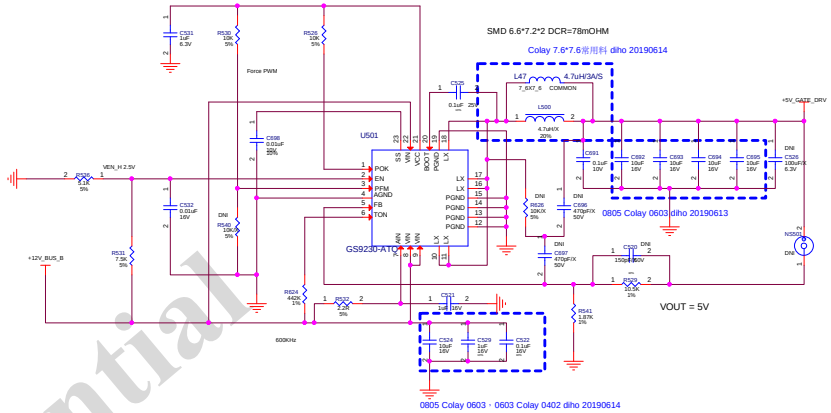

DEL PHASE8 By diho 20191126

GIGABYTE™

Title	GFX PHASE3&7	
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