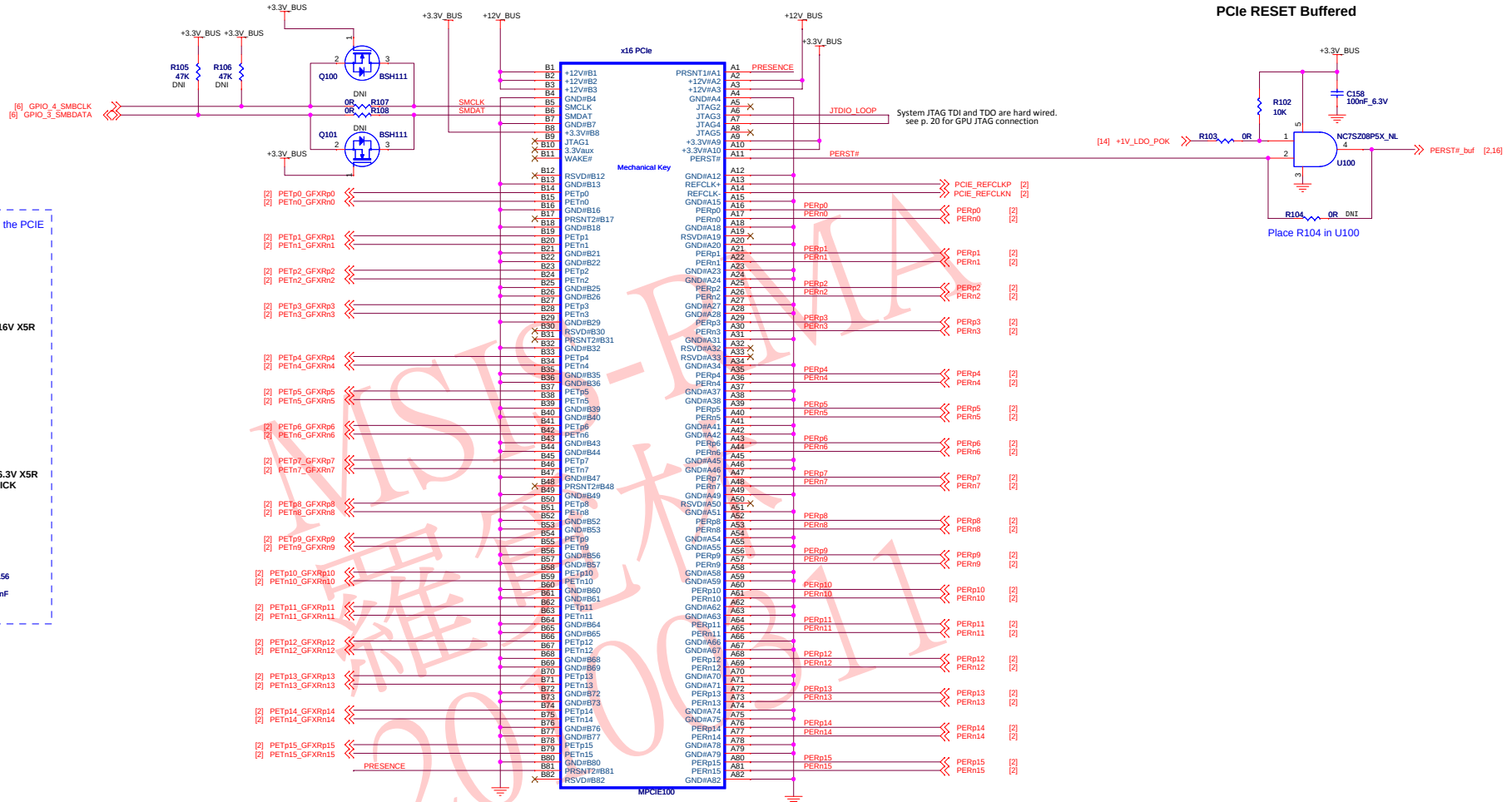
PCI-EXPRESS EDGE CONNECTOR

REDWOOD WOLVERINE



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

Advanced Micro Devices Inc.
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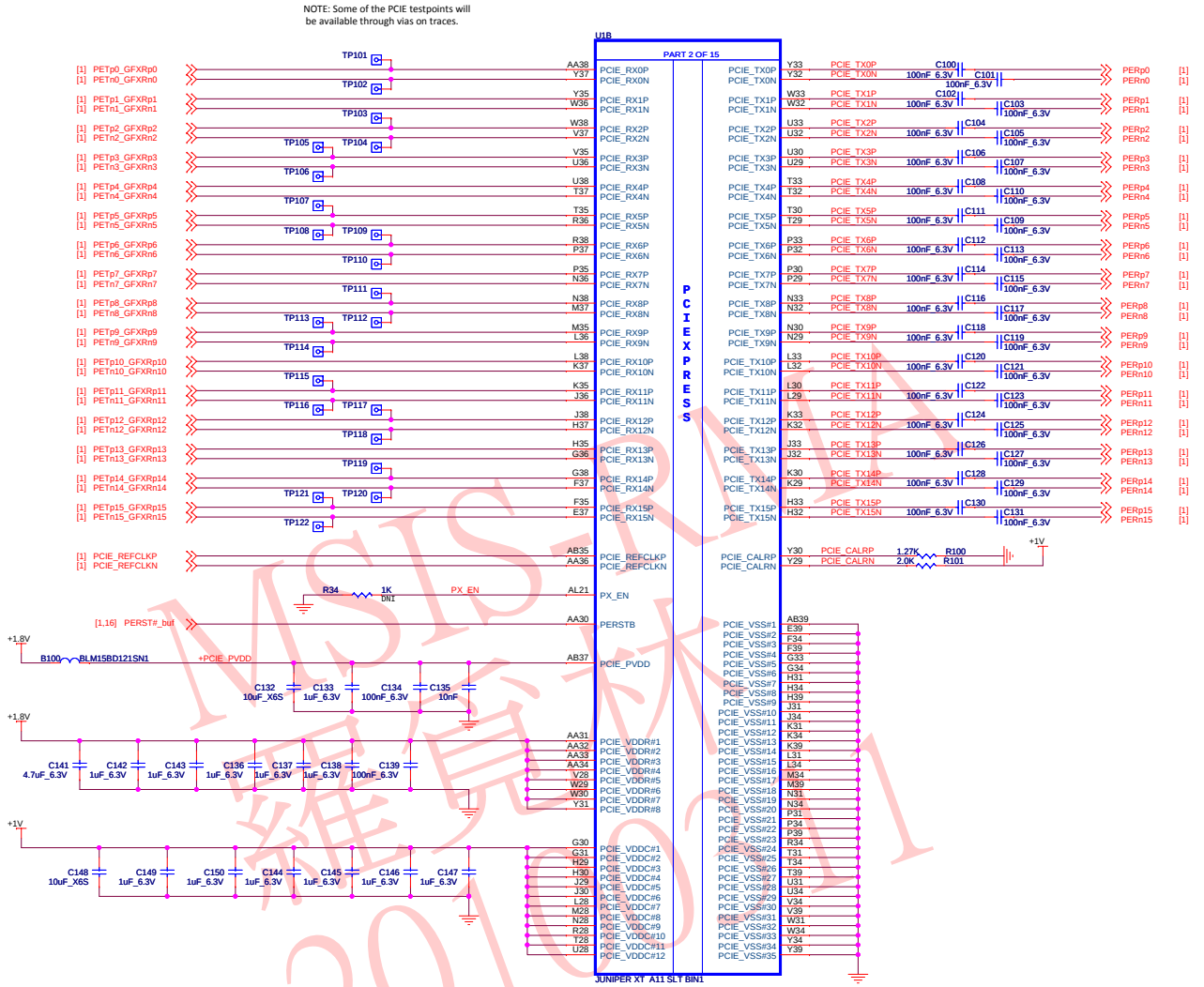
Markham, Ontario

Date: Tuesday, December 29, 2009 Rev P11

Sheet 1 of 19

Title RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI Doc No. 105-C029xx-00C

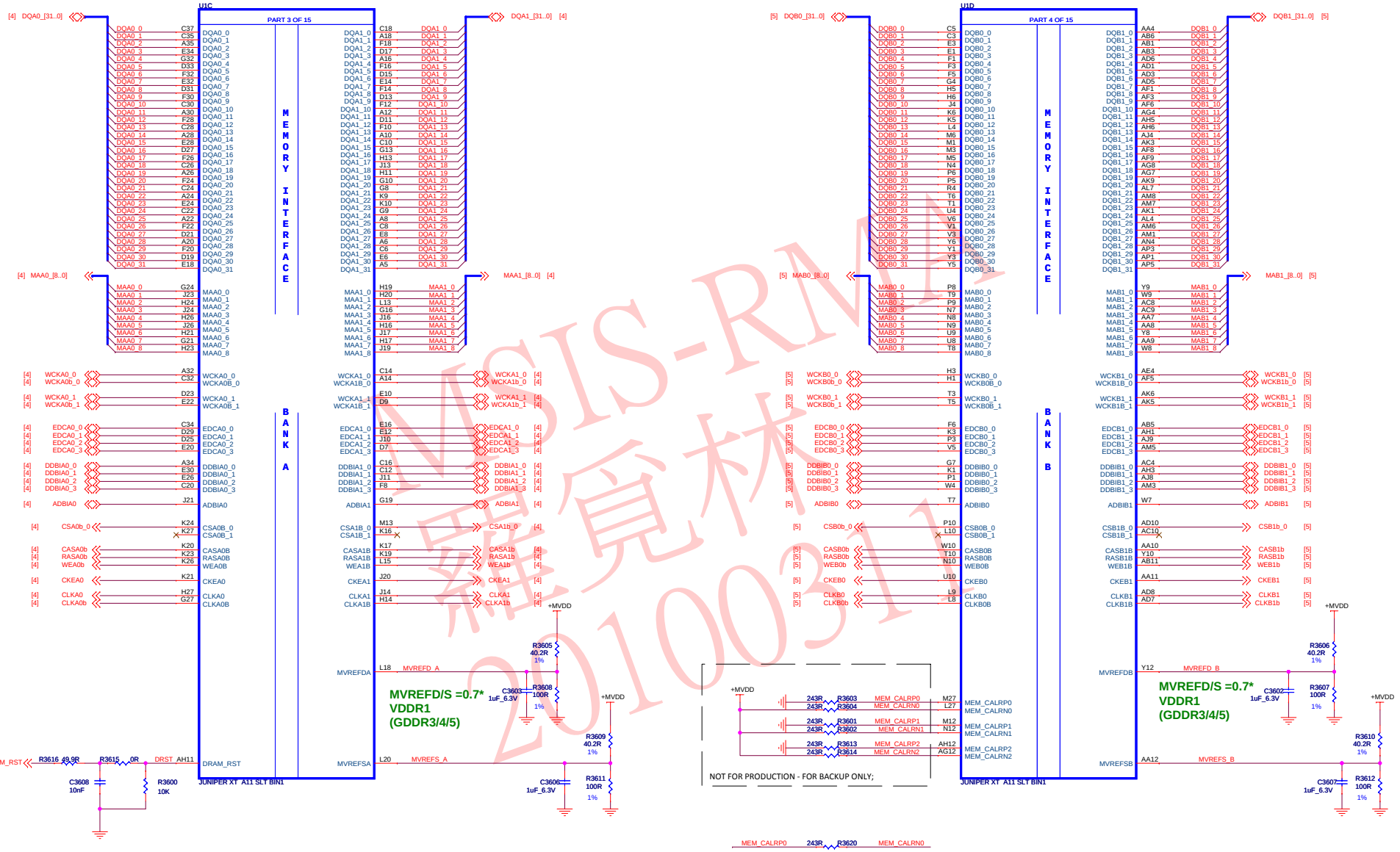
(2) REDWOOD PCIe Interface



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Tuesday, December 29, 2009
Rev	P11
Sheet	2 of 19
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI
Doc No.	105-C029xx-00C

(3) REDWOOD MEM Interface Ch A&B



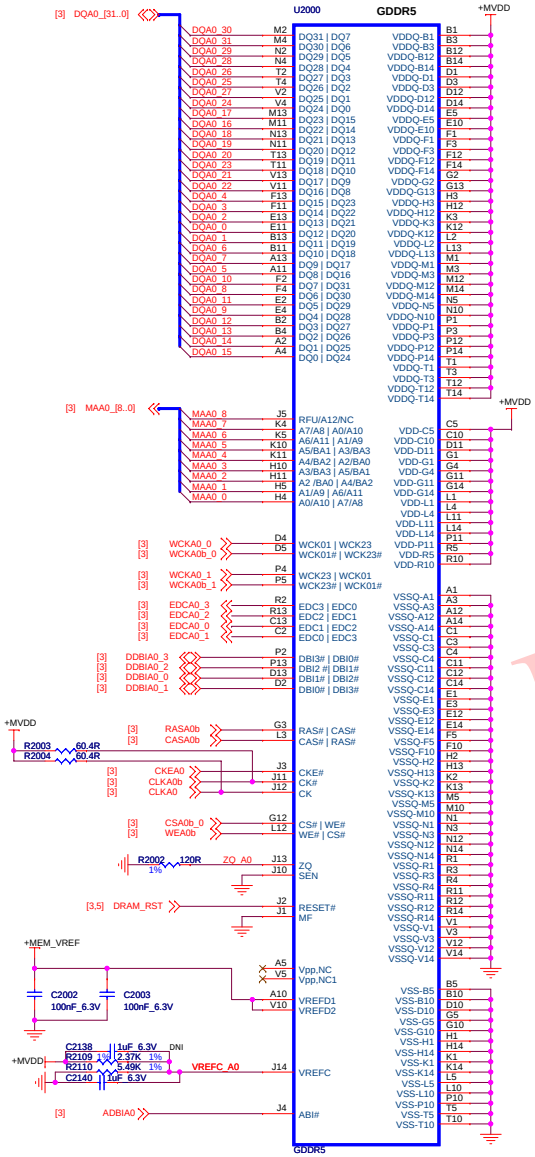
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

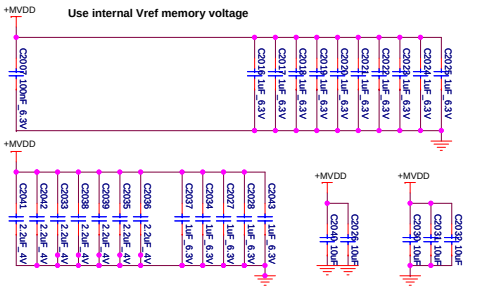
Date:	Tuesday, December 29, 2009
Rev	P11
Sheet	3 of 19
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI
Doc No.	105-C029xx-00C

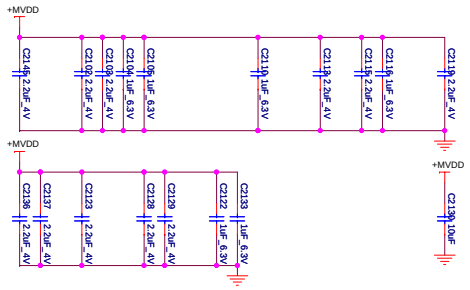
(4) GDDR5 x16 MEM Channel A

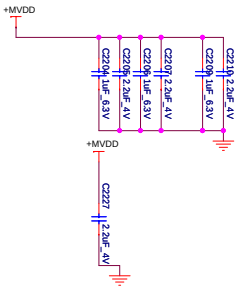
CH_A0 =U2000

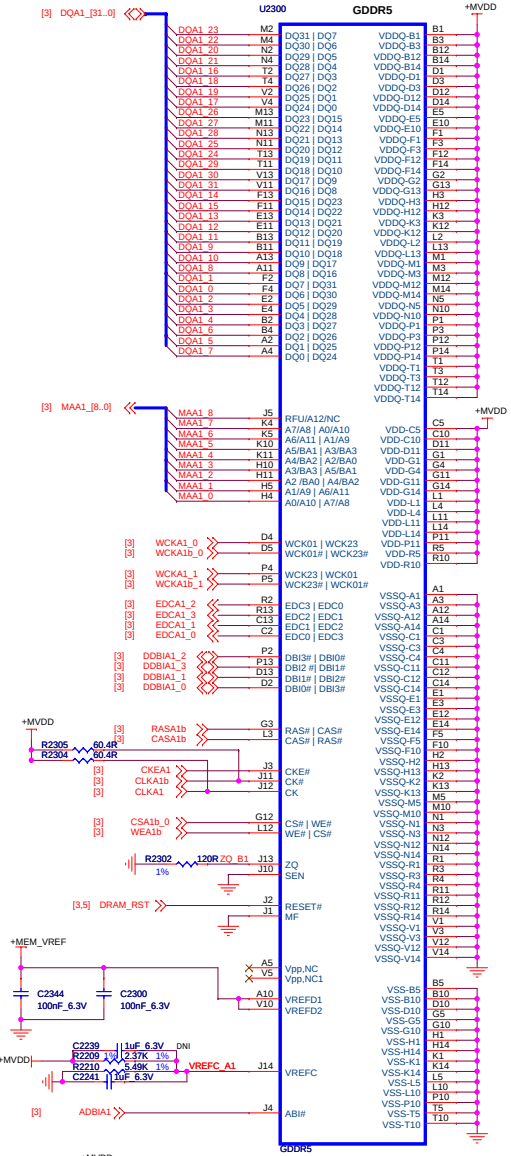
CH_A1 = U2300

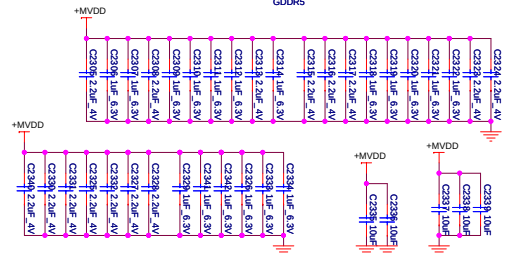












Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

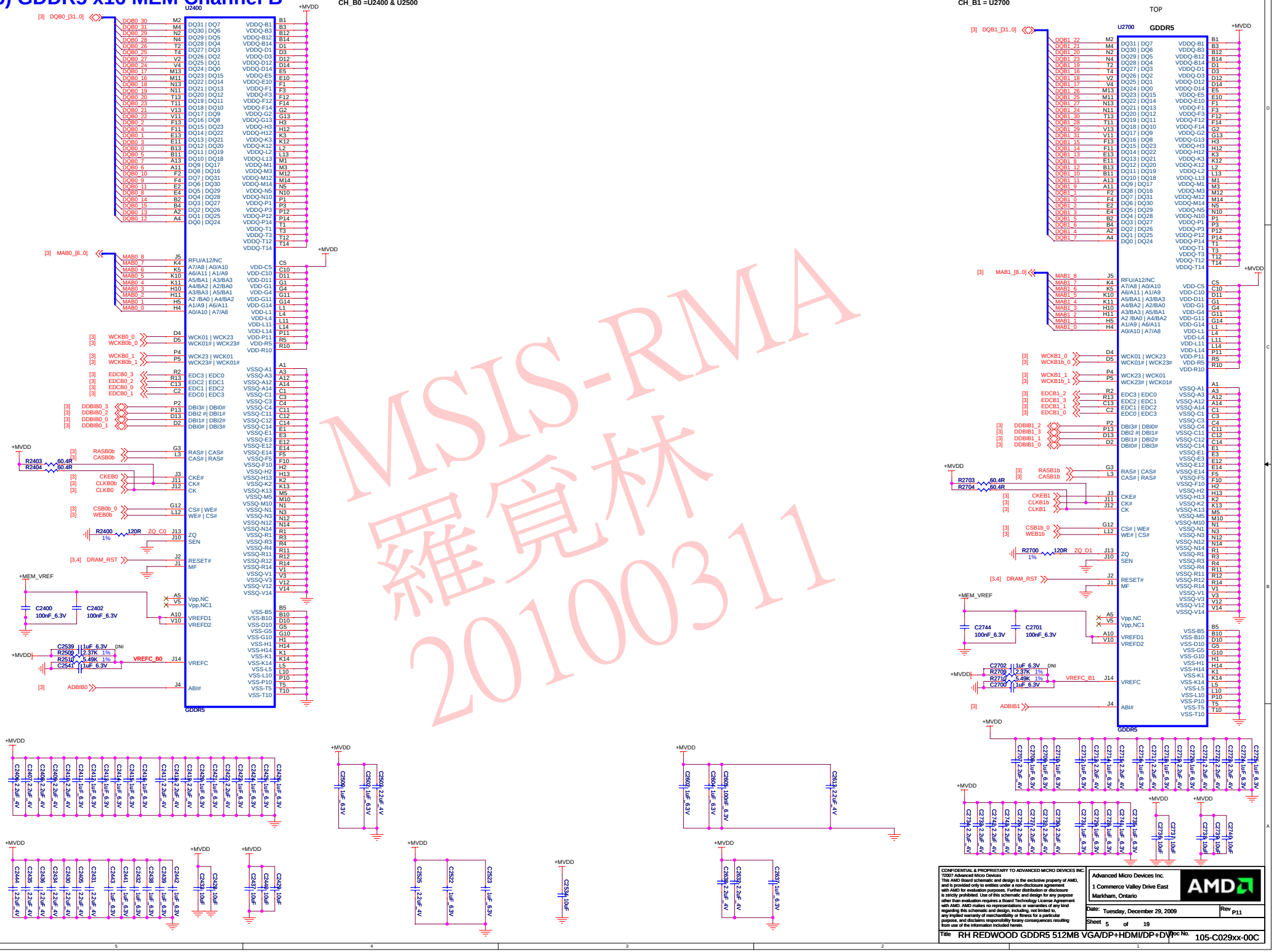
Date:	Tuesday, December 29, 2009
Rev	P11
Sheet	4 of 19
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI
Doc No.	105-C029xx-00C

(5) GDDR5 x16 MEM Channel B

CH_B0 =U2400 & U2500

CH_B1 = U2700

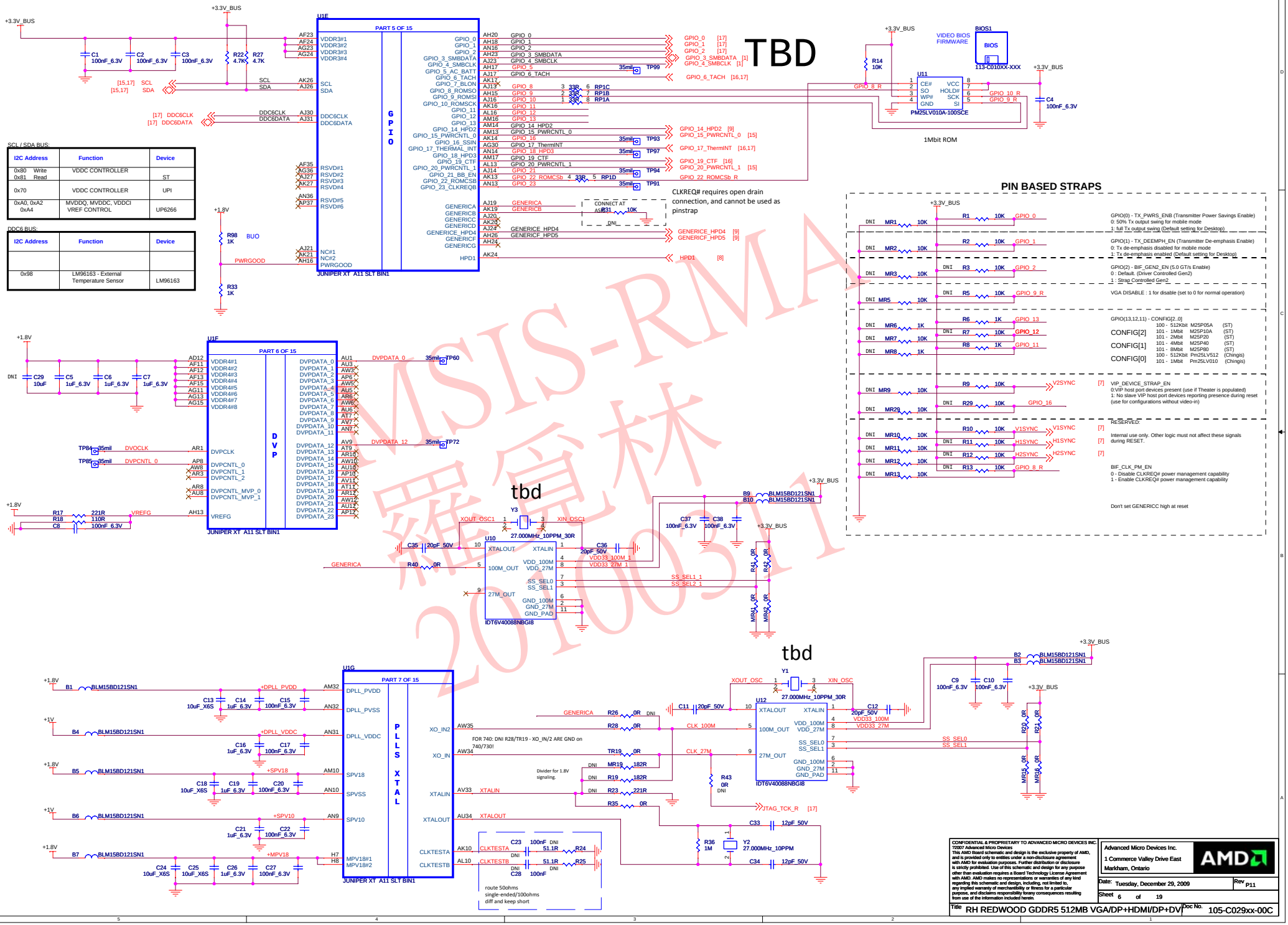
TOP



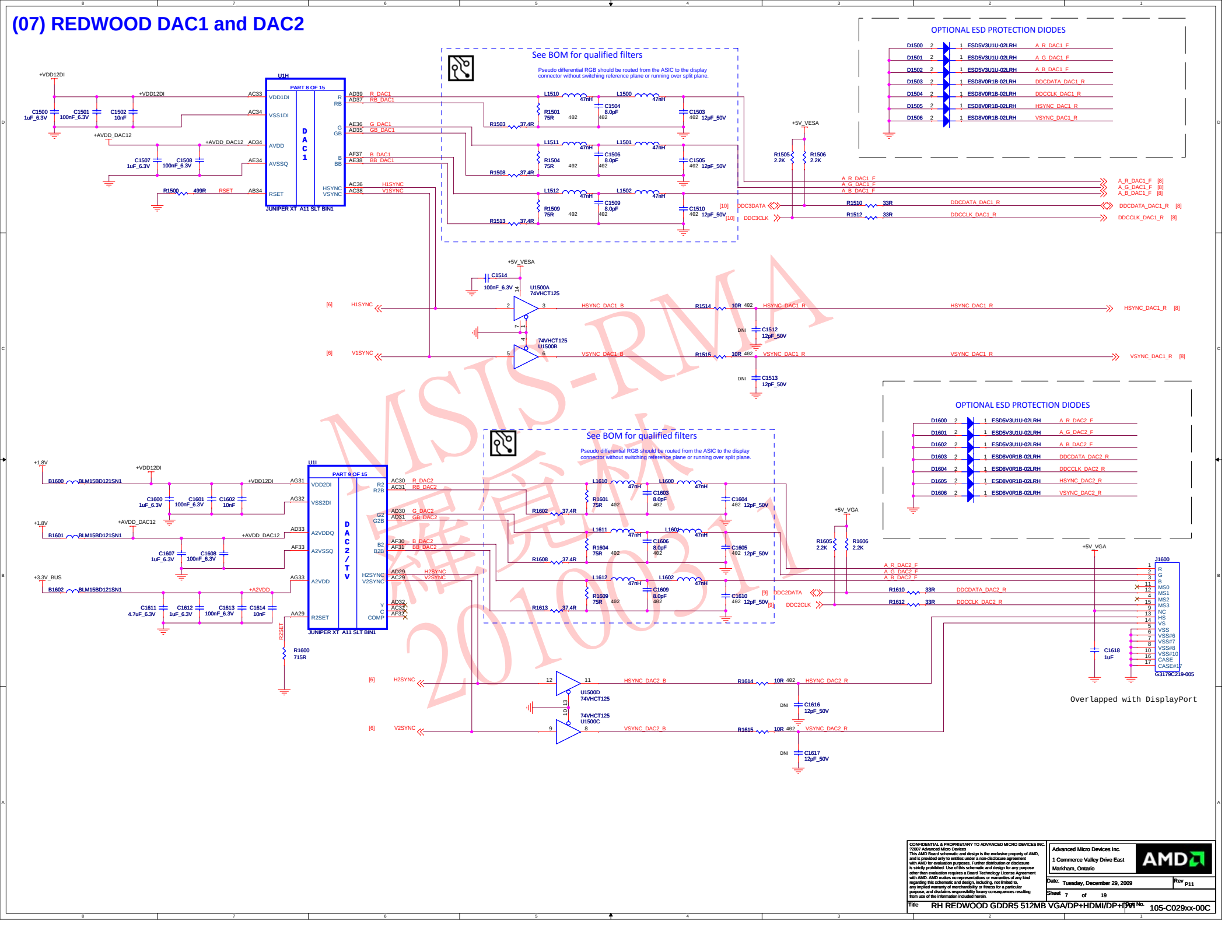
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Tuesday, December 29, 2009
Rev	P11
Sheet	5 of 19
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI
Doc No.	105-C029xx-00C

(06) REDWOOD GPIOs Strap CF XTAL OSC



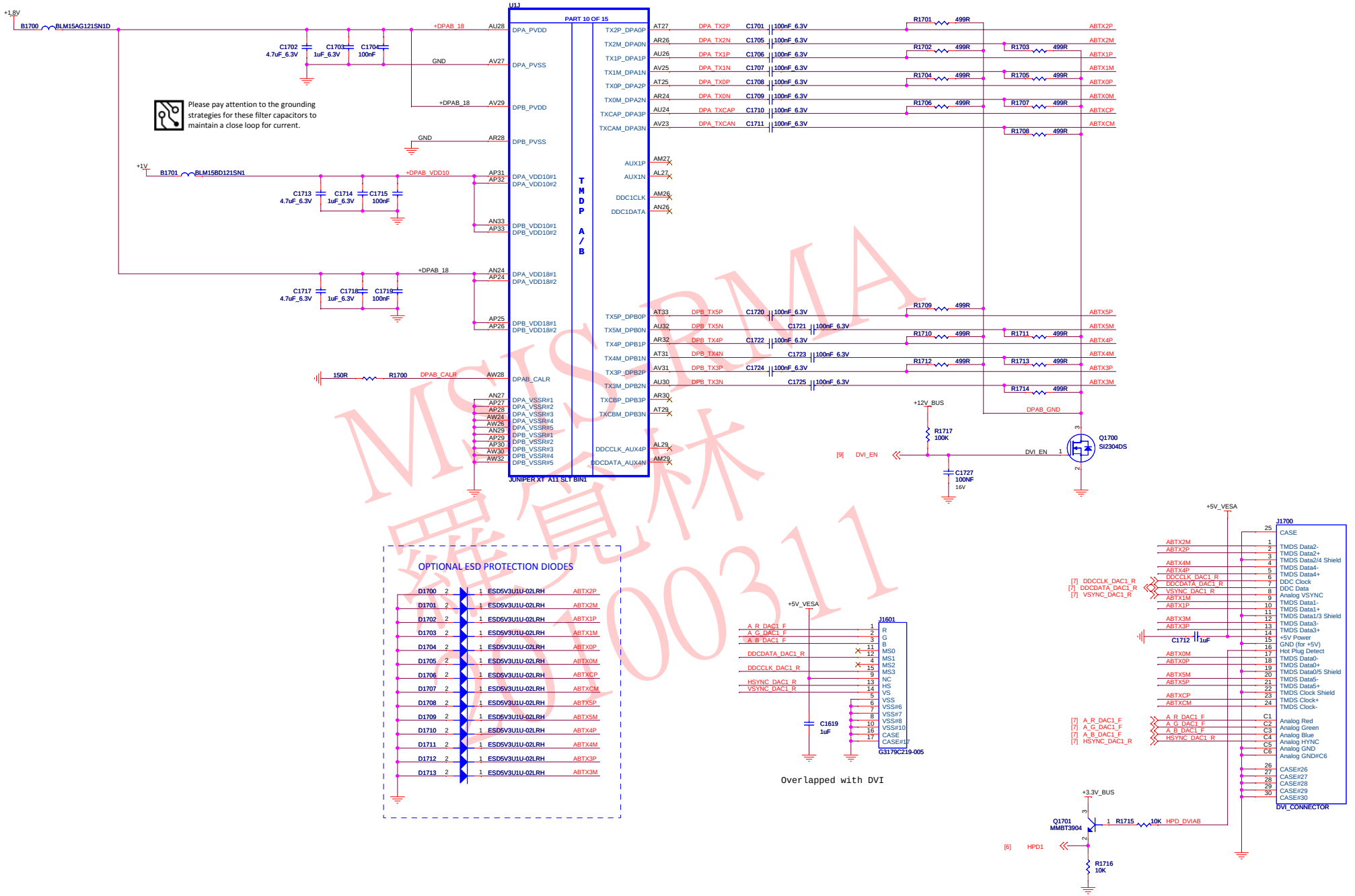
(07) REDWOOD DAC1 and DAC2



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Tuesday, December 29, 2009
Rev	P11
Sheet	7 of 19
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI
Doc No.	105-C029xx-00C

(08) REDWOOD TMDP A&B dDVI-I TOP



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Tuesday, December 29, 2009 Rev P11

Sheet 8 of 19

Title RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI Doc No. 105-C029xx-00C

(09) REDWOOD Display Port C & Display Port/HDMI D

To DP/HDMI connector.

To VGA connector.

DDC2CLK — DDC2CLK [7]

DDC2DATA — DDC2DATA [7]

AUX/DDC:
FOR 740/730, INSTALL 0R ON ASIC-SIDE OF AC COUPLING CAPS ONLY;
FOR JUNIPER, INSTALL 0R ON CONNECTOR SIDE OF AC COUPLING CAPS ONLY;

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

U1K — PART 11 OF 15 — TMDP C/D — JUNIPER XT A11 SLT BIN1

J1800 — DISPLAYPORT

J1801 — DISPLAYPORT

OPTIONAL ESD protection diodes

D1800 RCLAMP0524P

D1801 RCLAMP0524P

D1802 RCLAMP0524P

D1803 RCLAMP0524P

D1809 ESD5V3U1U-02LRH DPC_AUXN

D1808 ESD5V3U1U-02LRH DPC_AUXP

D1807 ESD5V3U1U-02LRH DPD_AUXN

D1806 ESD5V3U1U-02LRH DPD_AUXP

D1805 ESD5V3U1U-02LRH DPC_DONGLE_DET

D1804 ESD5V3U1U-02LRH DPD_DONGLE_DET

U1801A 74VHCT125

U1801B 74VHCT125

U1801C 74VHCT125

U1801D 74VHCT125

U1800 NC7WB66K8X

U1802 NC7WB66K8X

Q1800 MMBT3904

Q1801 MMBT3904

Q1802 SI2304DS

F1800 NANOSMDC150F-2

F1801 NANOSMDC150F-2

Share PADs

MJ1801 LONG_TYPE-2_HDMI

TP1800

OVERLAP HDMI WITH DP D

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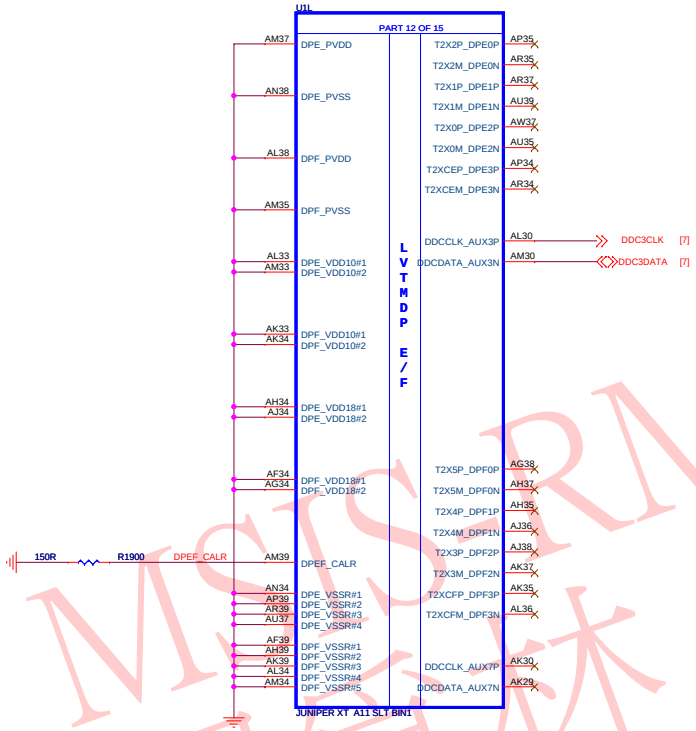
Date: Tuesday, December 29, 2009 Rev P11

Sheet 9 of 19

Title RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI Doc No. 105-C029xx-00C

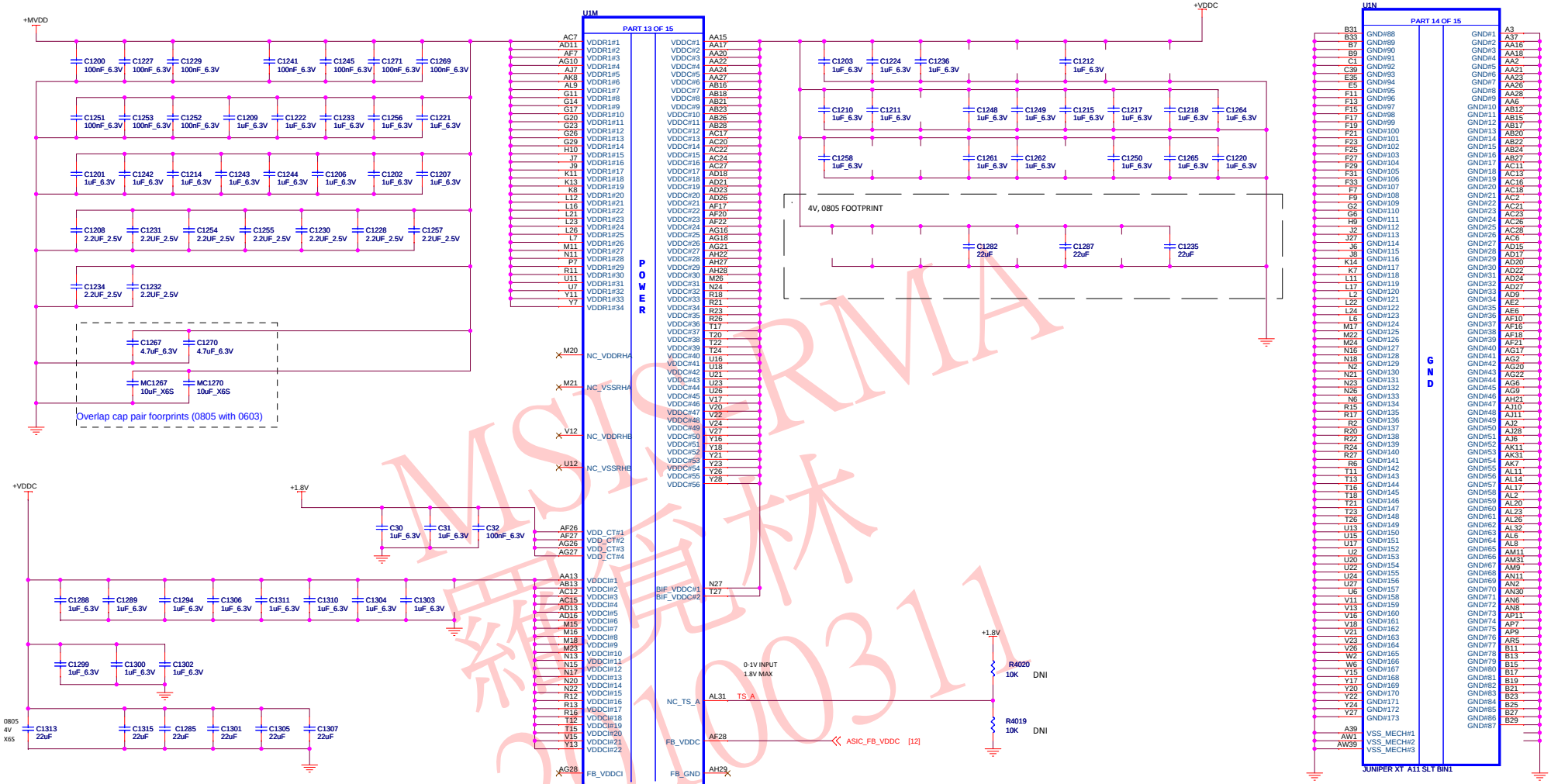
(10) REDWOOD LVTMDP E&F



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

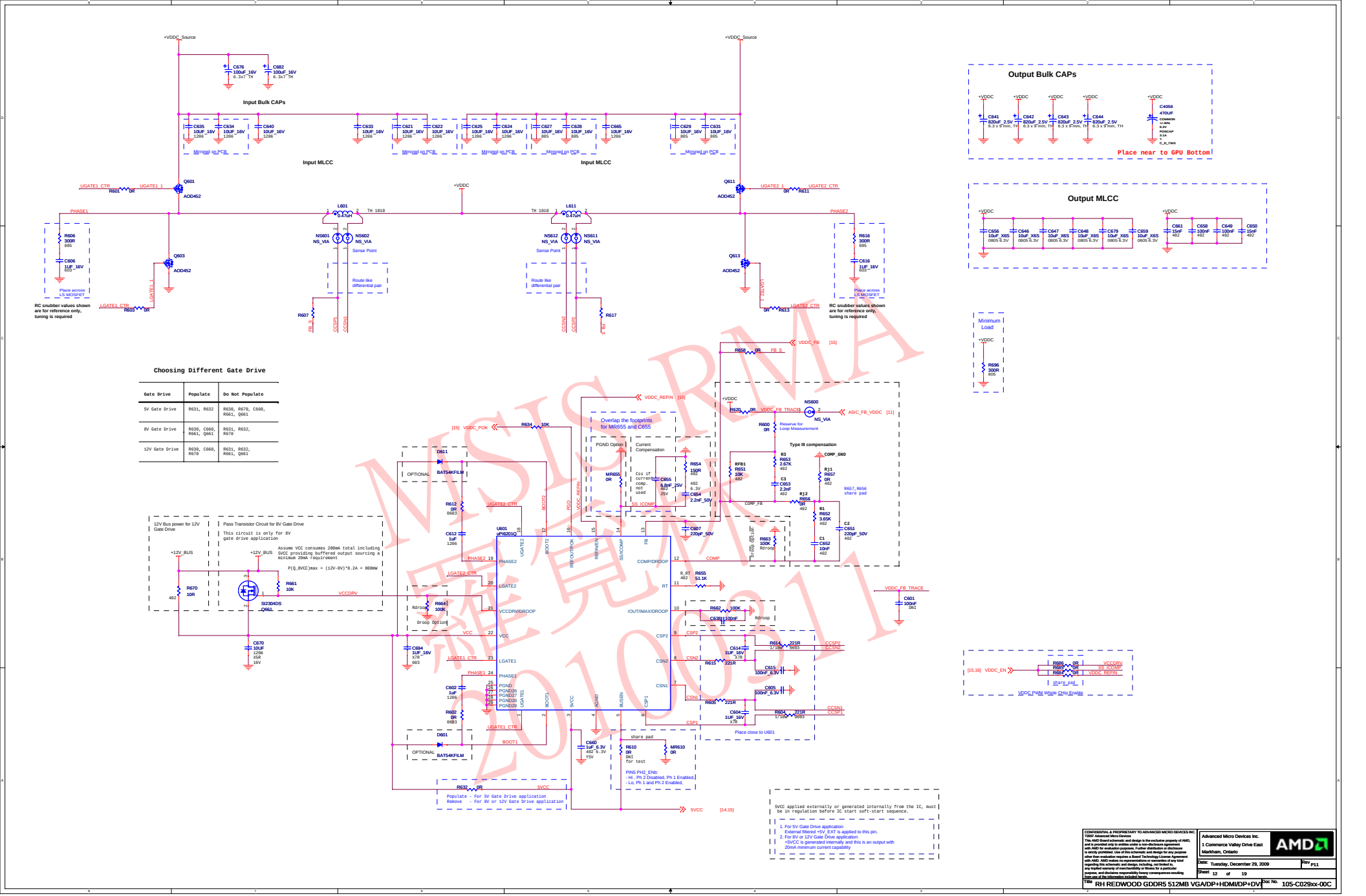
Date:	Tuesday, December 29, 2009
Rev	P11
Sheet	10 of 19
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI
Doc No.	105-C029xx-00C

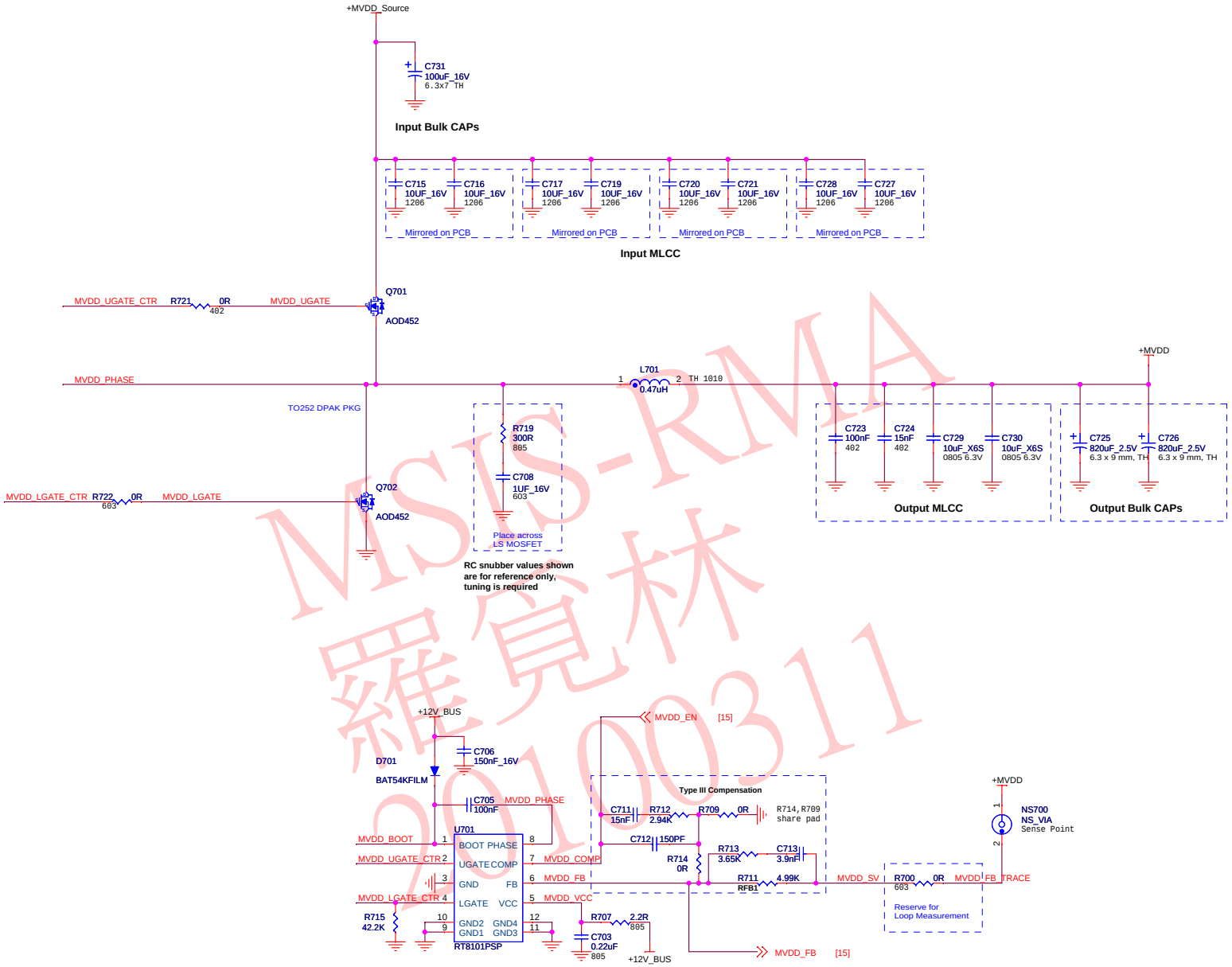
(11) REDWOOD Power & GND



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Tuesday, December 29, 2009
Rev	P11
Sheet	11 of 19
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI
Doc No.	105-C029xx-00C


Output Bulk CAPs
Place near to GPU Bottom
Output MLCC
Minimum Load
Input Bulk CAPs
Input MLCC
Choosing Different Gate Drive
Gate Drive | Populate | Do Not Populate
5V Gate Drive | R631, R632 | R630, R670, C660, R661, Q661
8V Gate Drive | R630, C660, R661, Q661 | R631, R632, R670
12V Gate Drive | R630, C660, R670 | R631, R632, R661, Q661
RC snubber values shown are for reference only, tuning is required
Overlap the footprints for MR655 and C655
Type III compensation
Pass Transistor Circuit for 8V Gate Drive
This circuit is only for 8V gate drive application
Assume VCC consumes 200mA total including 5VCC providing buffered output sourcing a minimum 20mA requirement
P(Q_8VCC)max = (12V-8V)*0.2A = 800mW
Droop Option
SVCC applied externally or generated internally from the IC, must be in regulation before IC start soft-start sequence.
1. For 5V Gate Drive application: External filtered +5V_EXT is applied to this pin.
2. For 8V or 12V Gate Drive application: +5VCC is generated internally and this is an output with 20mA minimum current capability
PINS PH2_Enb: - Hi : Ph 2 Disabled. Ph 1 Enabled. - Lo. Ph 1 and Ph 2 Enabled.
VDDC_PWM Whole Chip Enable
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario
Date: Tuesday, December 29, 2009
Rev P11
Sheet 12 of 19
Title RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI
Doc No. 105-C029xx-00C



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Tuesday, December 29, 2009 Rev P11

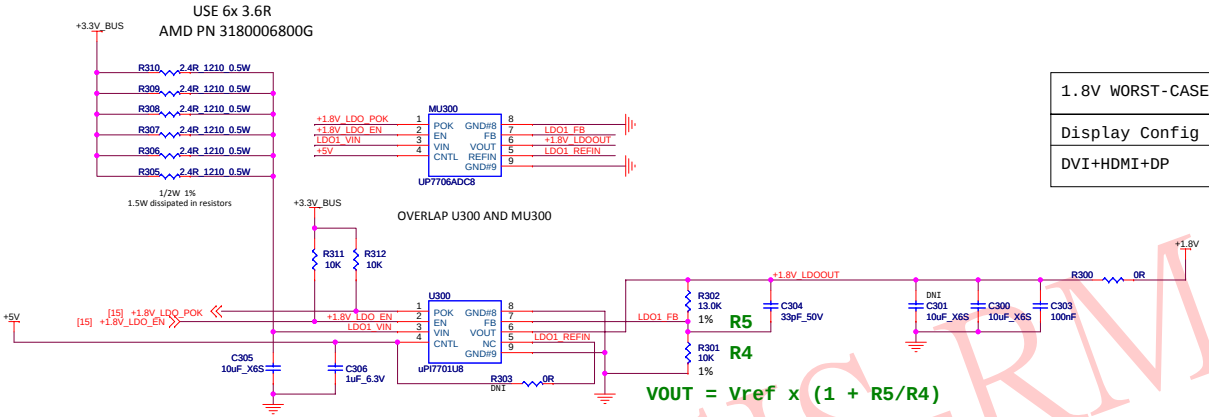
Sheet 13 of 19

Title RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI Doc No. 105-C029xx-00B

(15) Linear Regulators

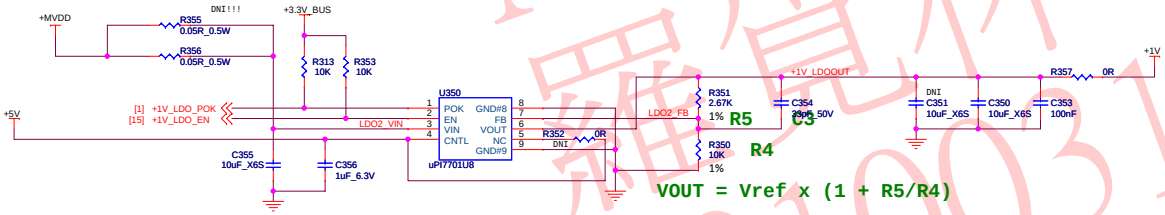
Regulators for +5V, +5V_VESA and +5V_HDMI

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



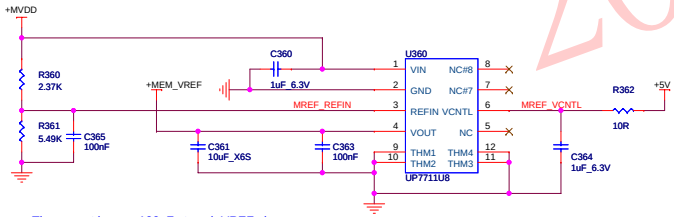
1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

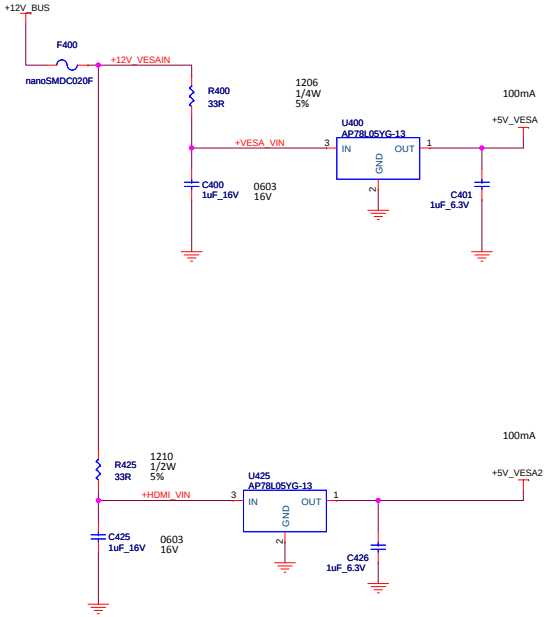


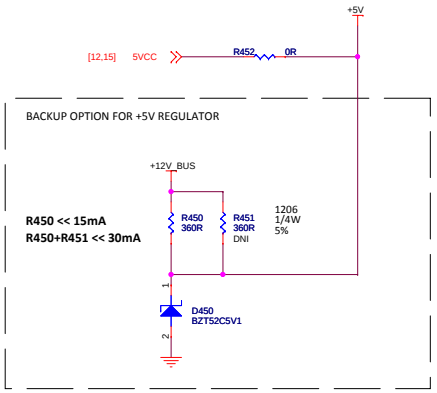
1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA

Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ



There must be one 100nF at each VREF pin
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices



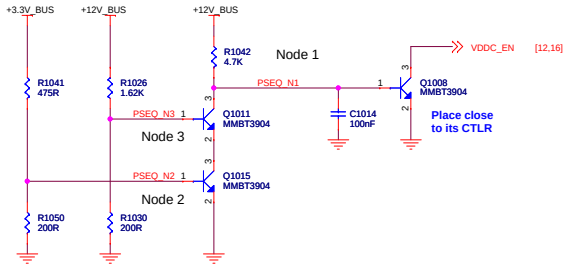


Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Tuesday, December 29, 2009 Rev P11
Sheet 14 of 19
Title RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI Doc No. 105-C029xx-00C

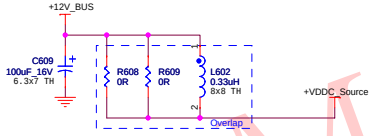
(16) Power Management - Power Gating and Dynamic Voltage Control

12V_BUS & 3V3_BUS POWER SEQUENCING

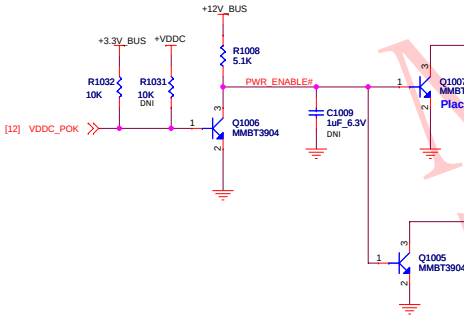


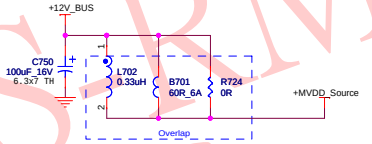
Install R1010 to gate 1V LDO with 1.8V LDO.

[14] +1.8V_LDO_POK — R1010 0R — +1V_LDO_EN [14]

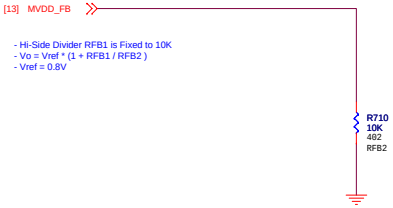


POWER SEQUENCING CIRCUIT



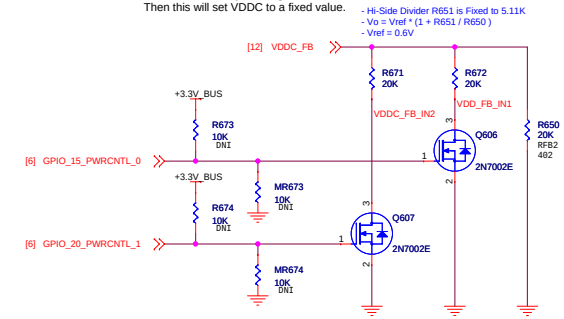


MVDD Low Side Divider

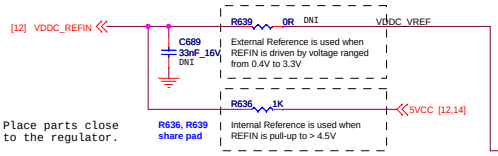


VDDC Low Side Divider

R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.



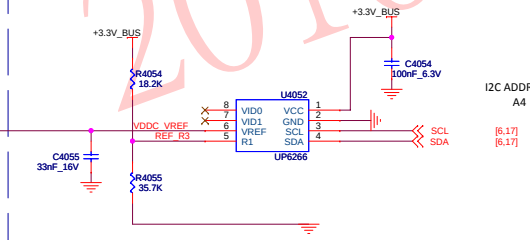
VDDC Reference Voltage Selection



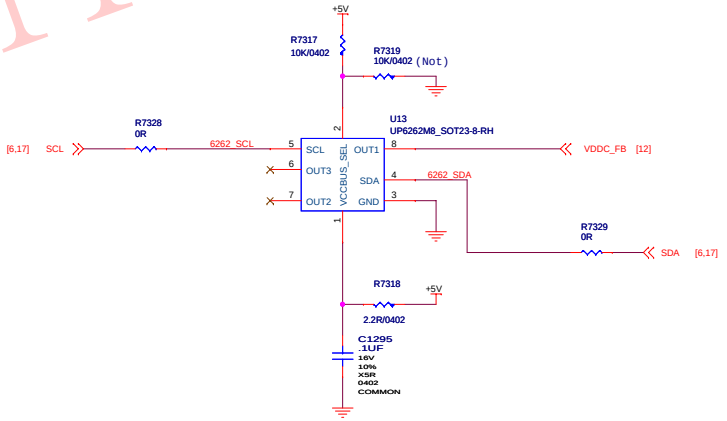
VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

I2C VOLTAGE REFERENCE FOR VDDC (not for production)



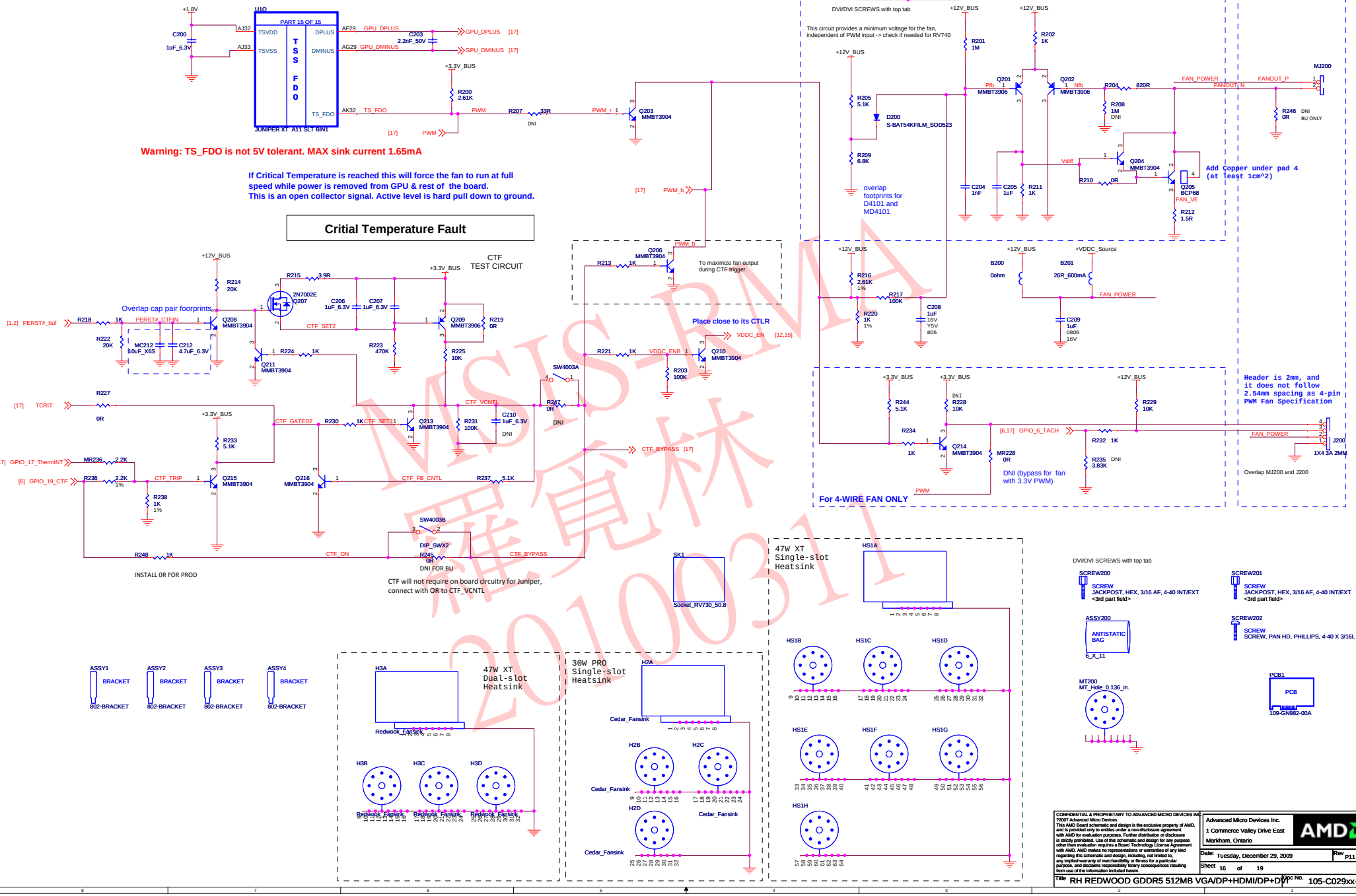
I2C ADDRESS: A4



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Tuesday, December 29, 2009
Rev	P11
Sheet	15 of 19
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI
Doc No.	105-C029xx-00C

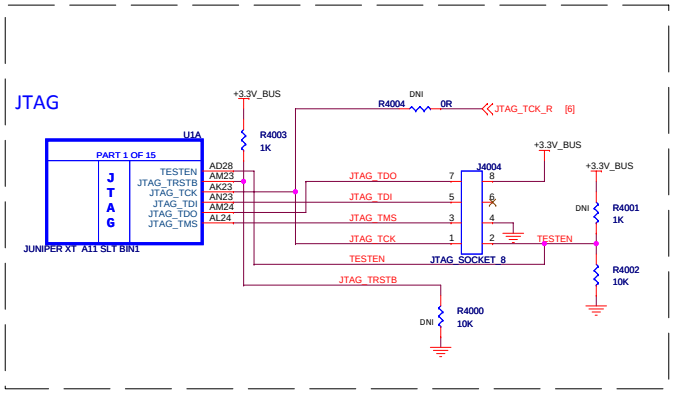
(19) Mechanical and Thermal Management

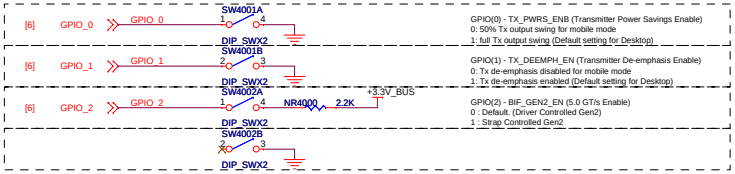


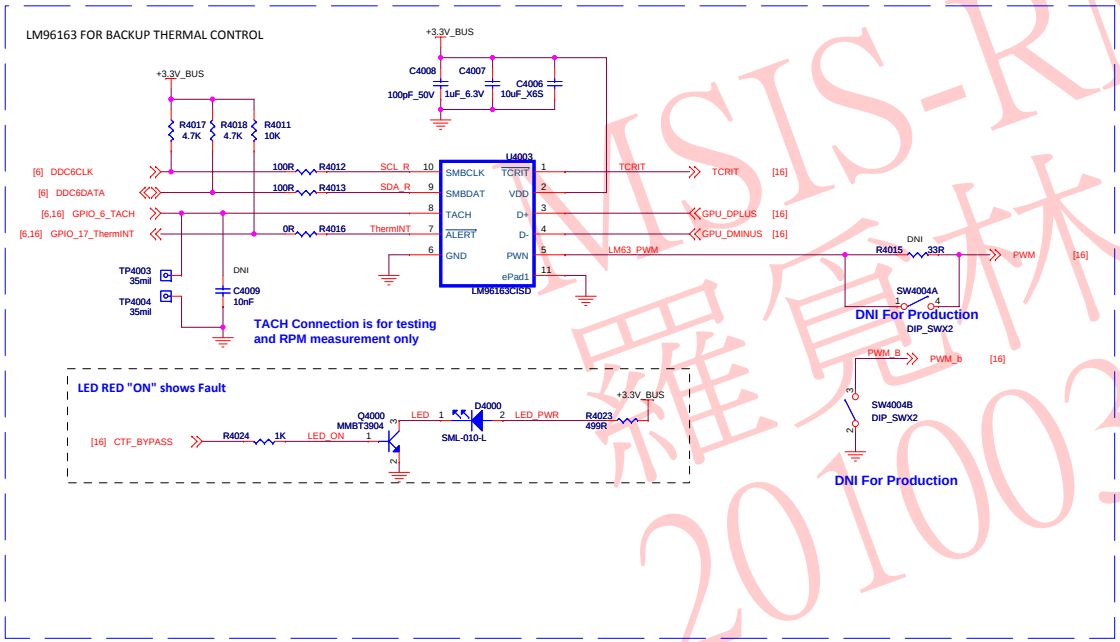
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

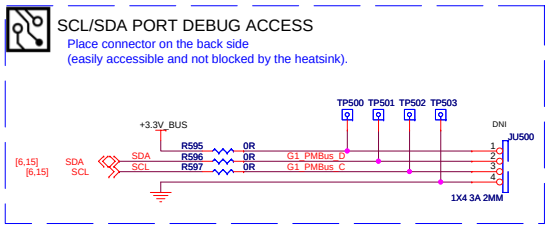
Date:	Tuesday, December 29, 2009
Rev	P11
Sheet	16 of 19
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI
Doc No.	105-C029xx-00C

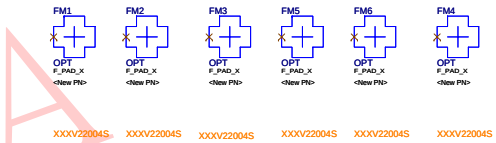
(19) Debug Circuits

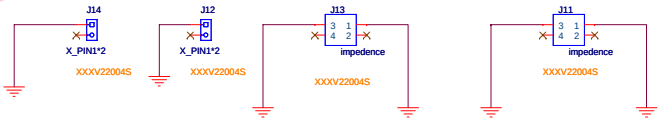












J11 6 層 80OHM (0.14mm/0.17mm =>5.5 mils/6.7 mils) MEM_CLK
J13 3 層 80OHM (0.175mm/0.28mm=>6.889 mils/11.0236 mils) MEM_CLK
J12 1.6層 45OHM (0.13mm => 5.1181 mils) MEM
J14 3 層 45OHM (0.175mm =>6.9mils) MEM

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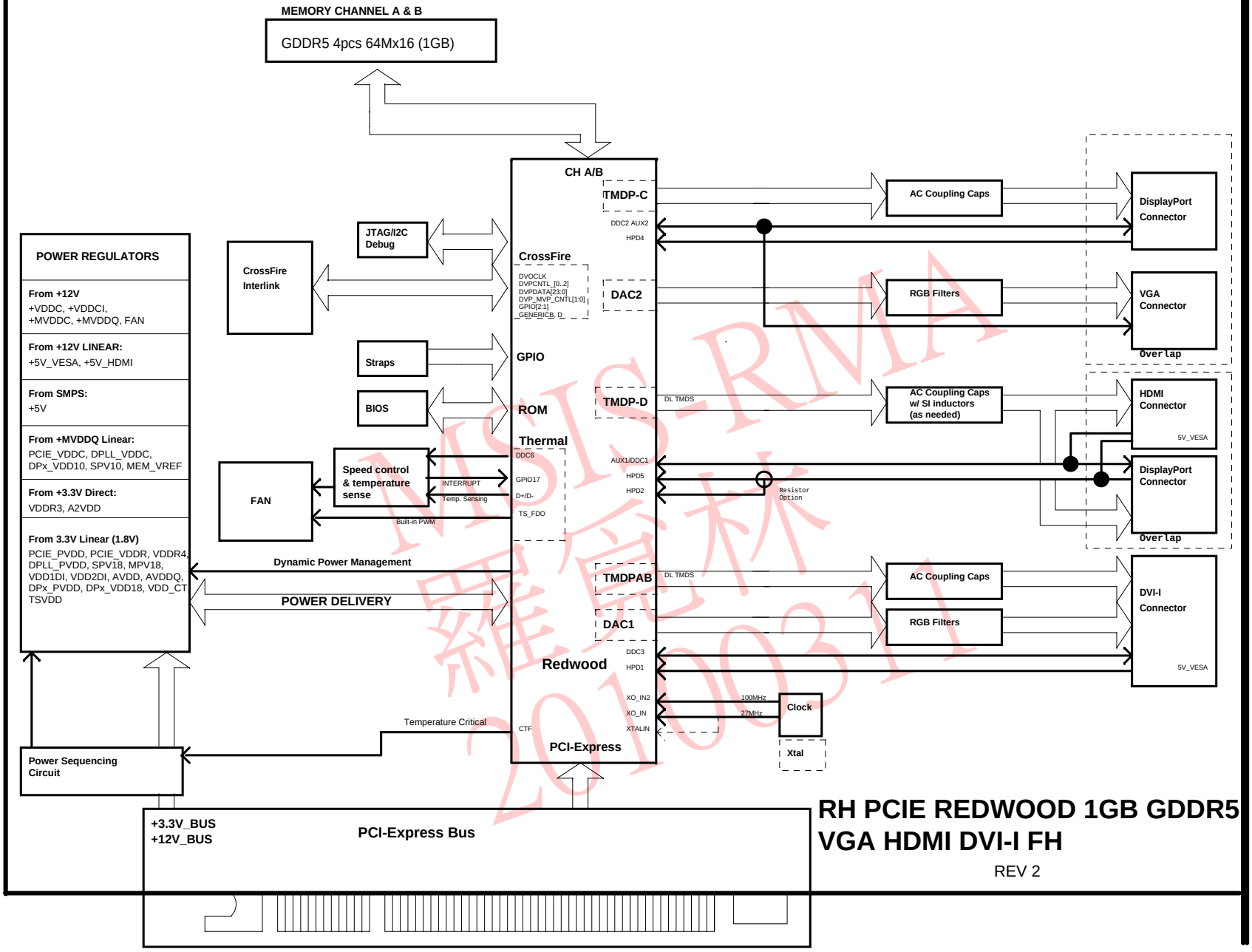
Date:	Tuesday, December 29, 2009
Rev	P11
Sheet	17 of 19
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI
Doc No.	105-C029xx-00C



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Date:	Tuesday, December 29, 2009	Rev	P11
Sheet	of	105-C029xx-00C	
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI	Doc No.	18 19

Title	Schematic No.	Date:
RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI	105-C029xx-00C	Tuesday, December 29, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev P11

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/05/08	REDWOOD XT GDDR5 512MB - BASED ON C020 ;
	00B	2009/10/12	1) SWAP DDC LINE TO FIX HDMI CERTIFICATE ISSUE 2) ADD ONE MORE SERIES RESISTOR ON DRAM_RST NET BASED ON SI TEAM SIMULATION RESULT 3) ADD 27MHz CLOCK TO JTAG CLK
	00C	2009/12/02	1) ADD 1.8V I/O SHUT DOWN CIRCUIT
	V220-4.0	2009/12/25	1)Modify Choke to SSC 2)Add POSCAP 1)Add uPI / uP6262