

PG111-A01

GP108 64Bit sDDR4 X16

HDMI/DP + DL DVI-D /DP

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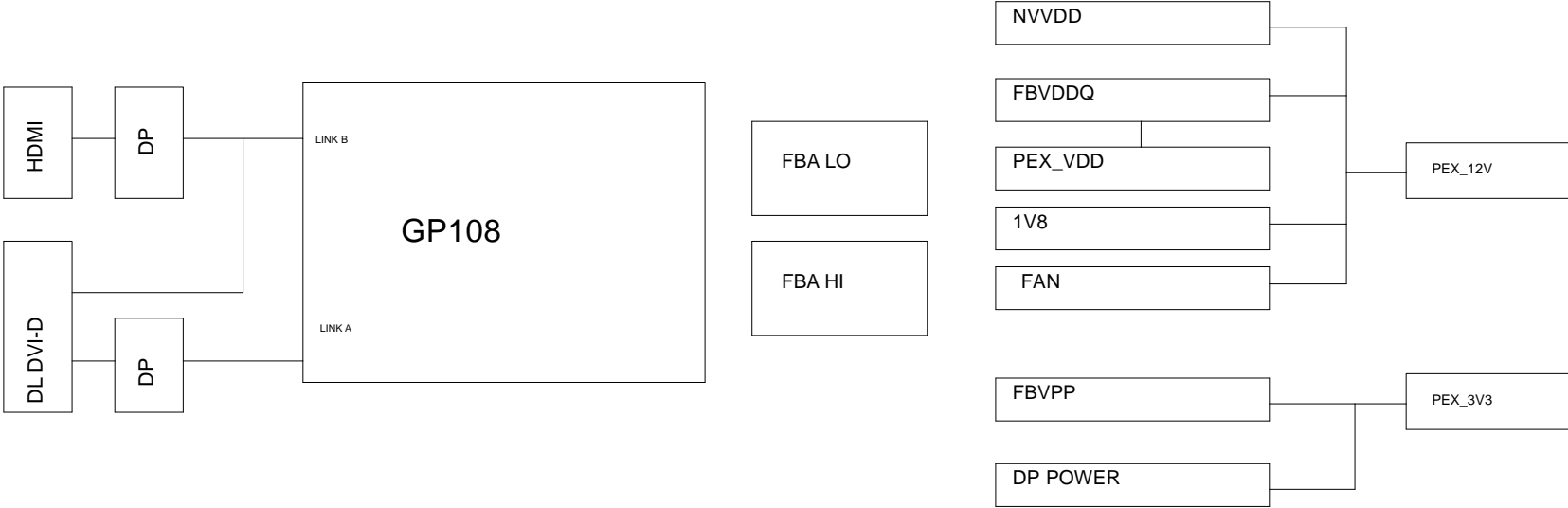
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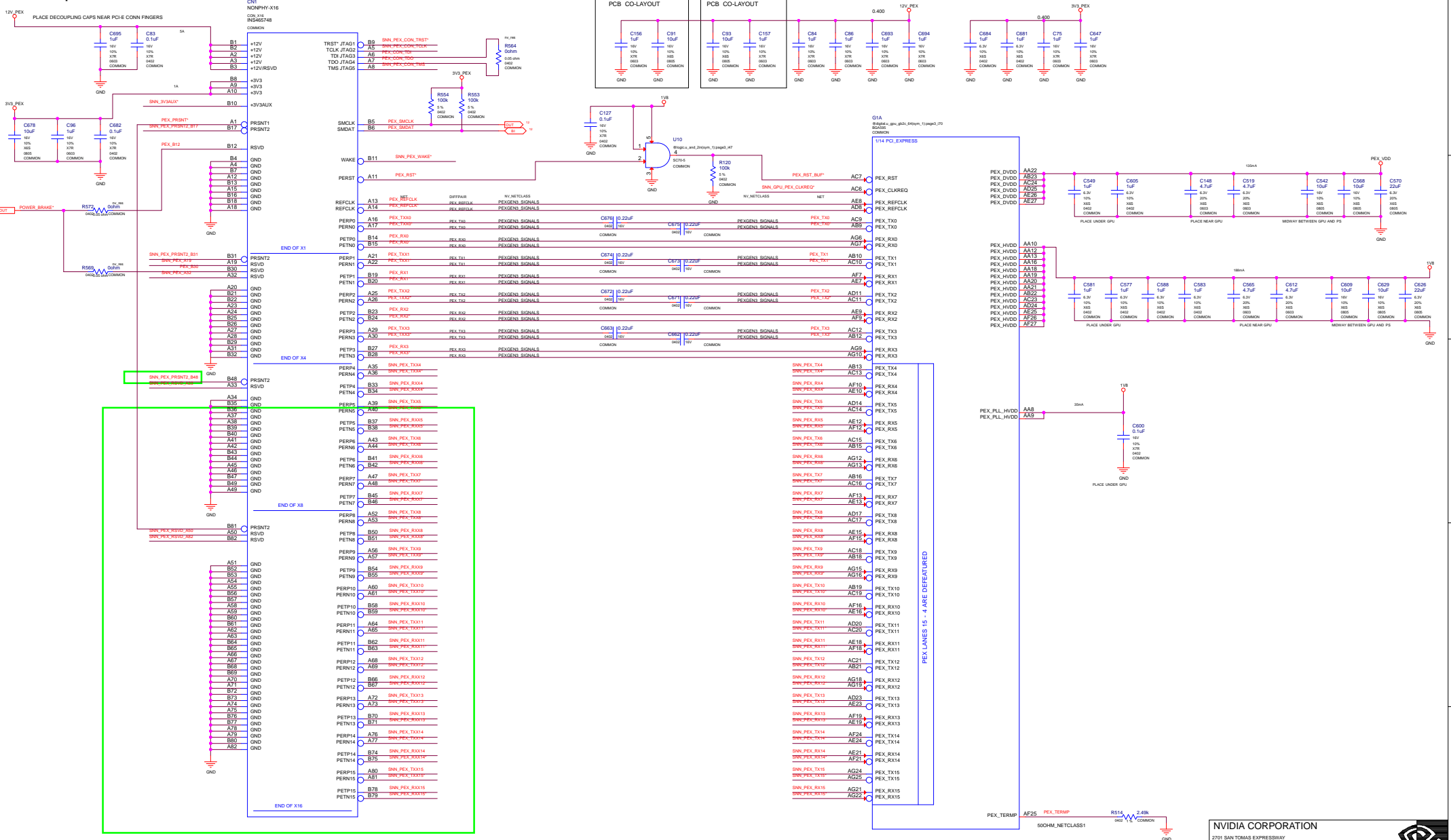
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Block Diagram



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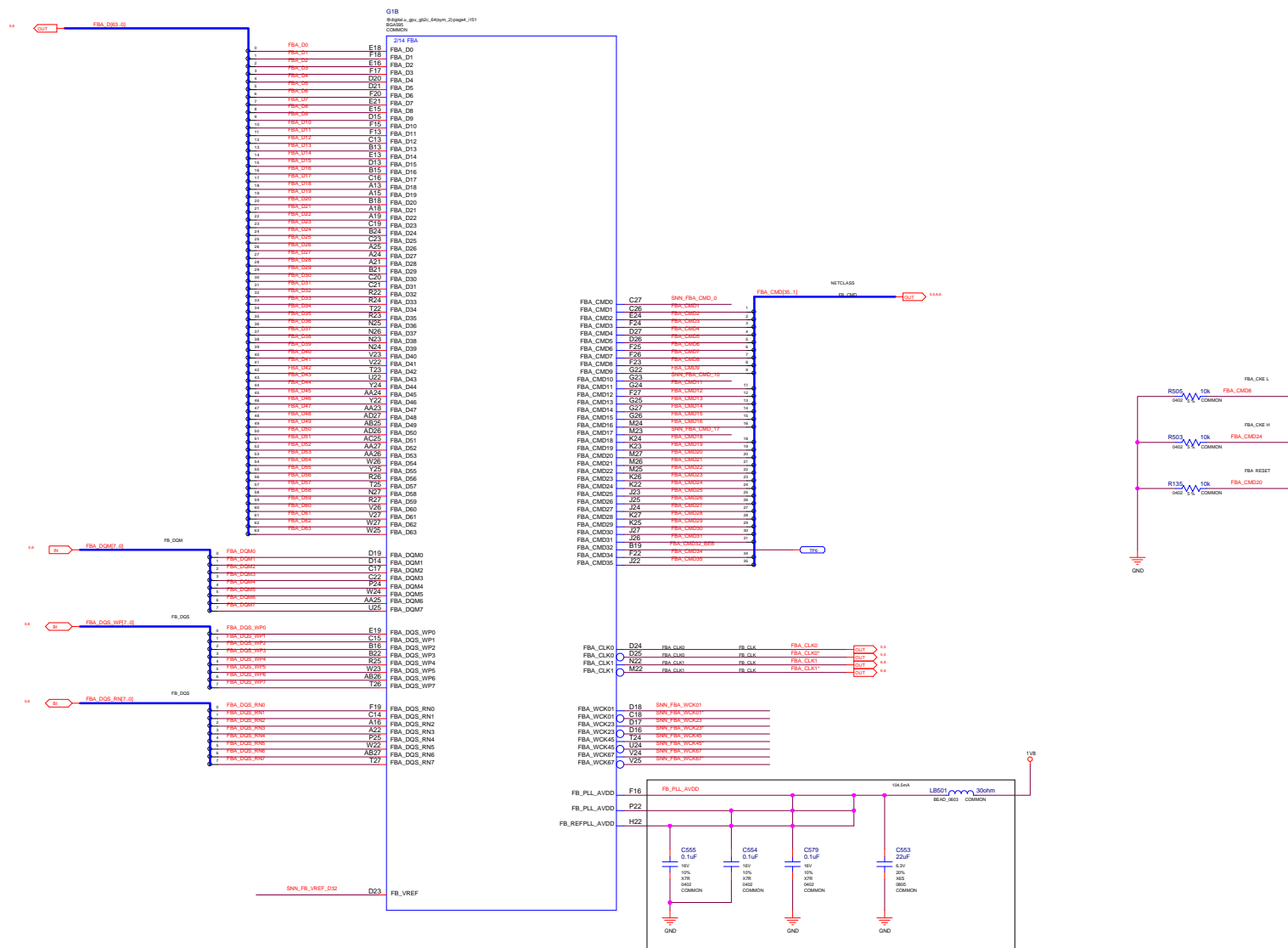
PCI Express



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MAY NO CLAIMS ALL STANDARDS.		NV_PN 600-1G111-BASE-A01	
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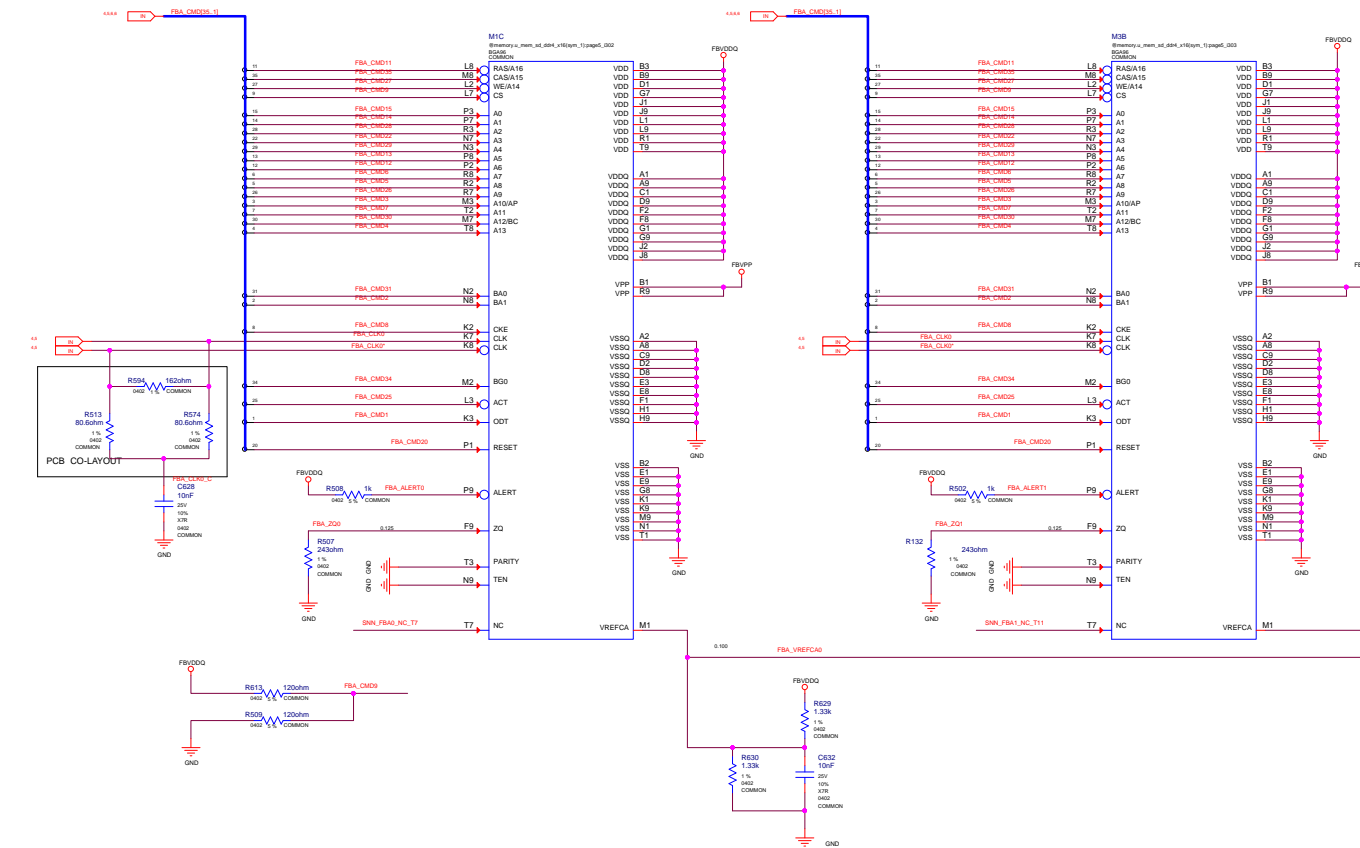
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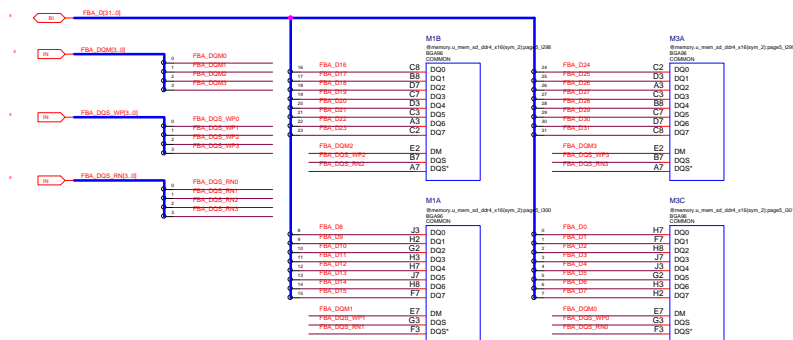
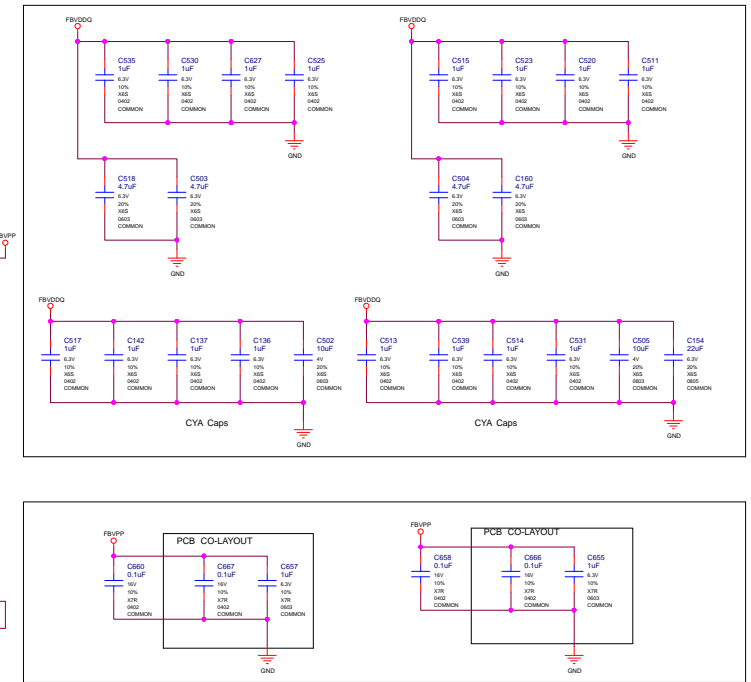
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	0.31	30.40
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FBA bits 31..00



Each memory
4x1uF 0402
2x4.7uF 0603



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PAGE DETAIL	FBA bits 31..00

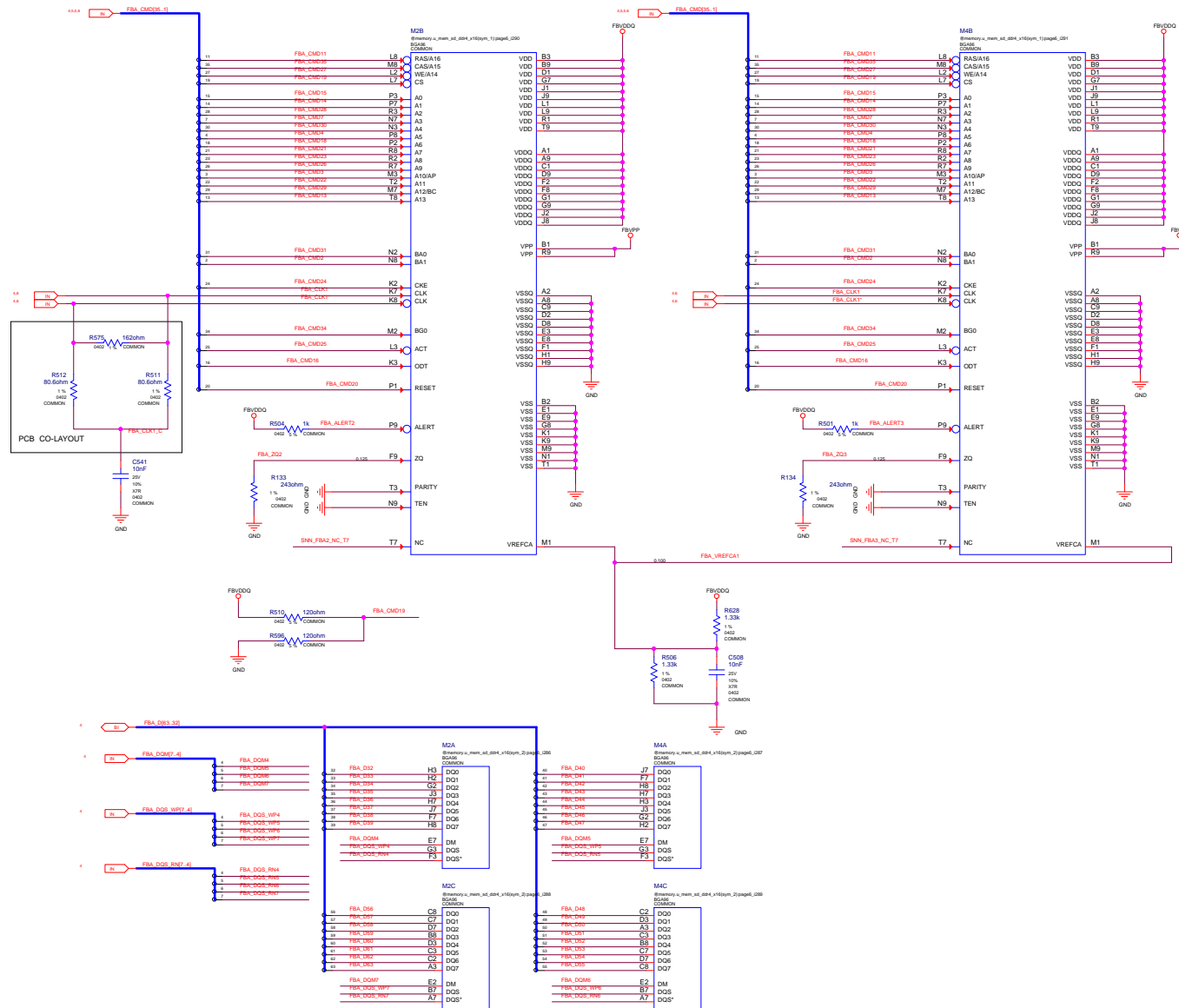
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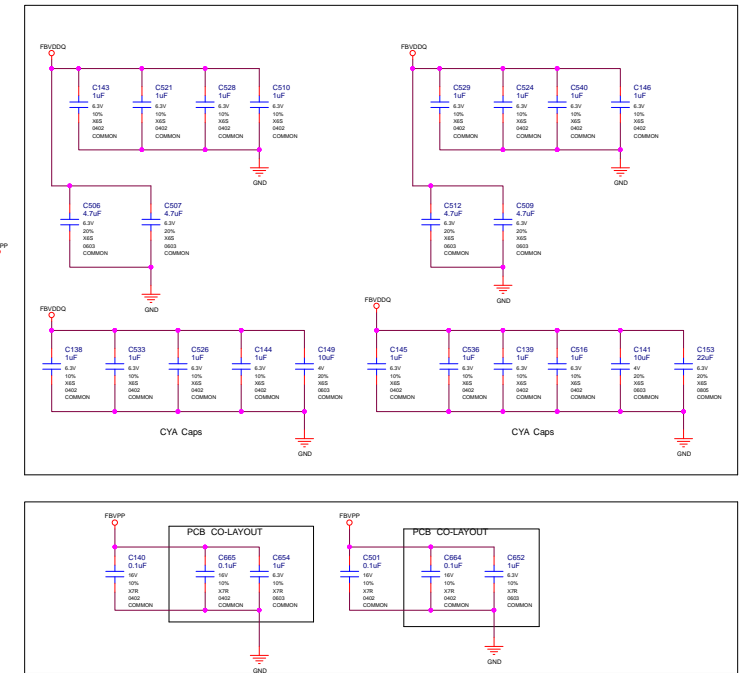


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FBA bits 63..32



Each memory
4x1uF 0402
2x4.7uF 0603



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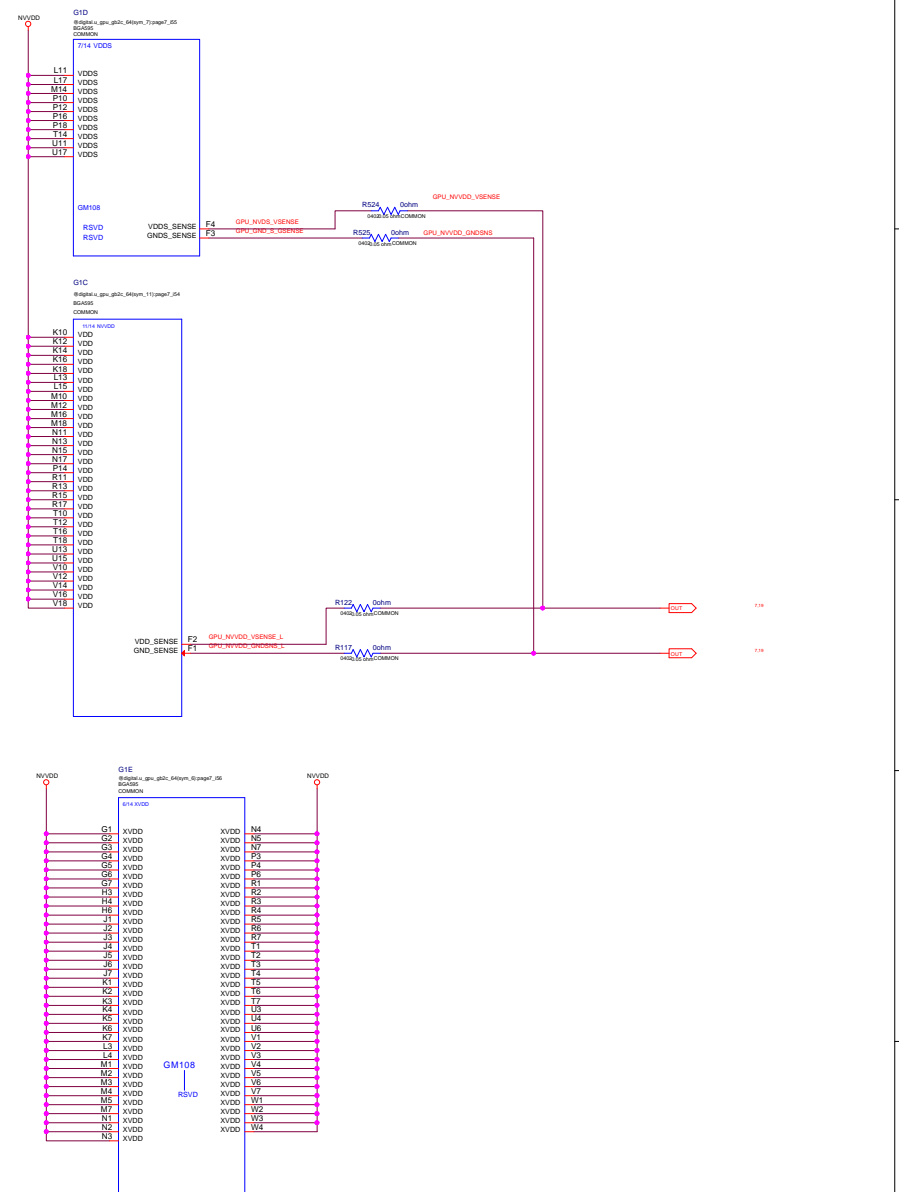
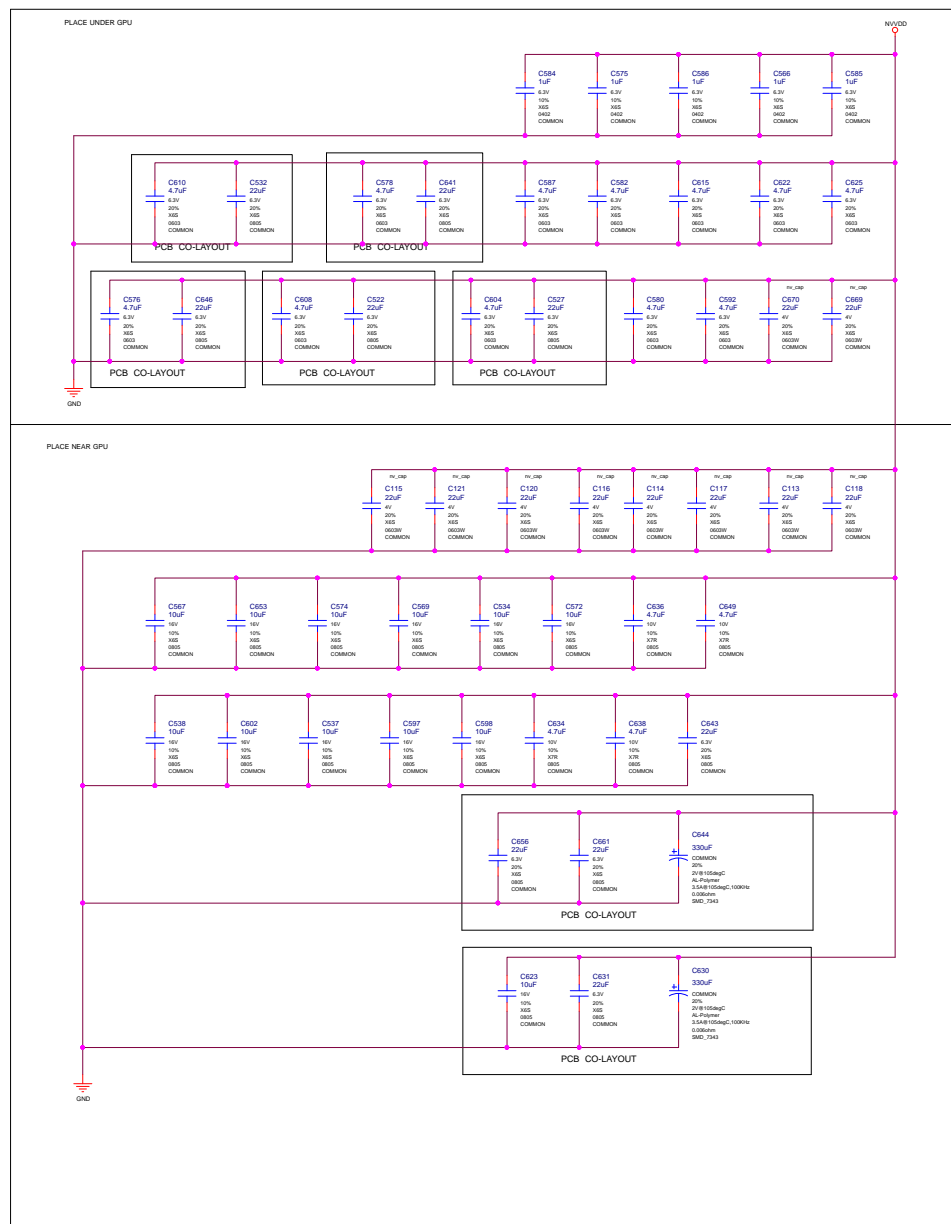
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NVDD Decoupling

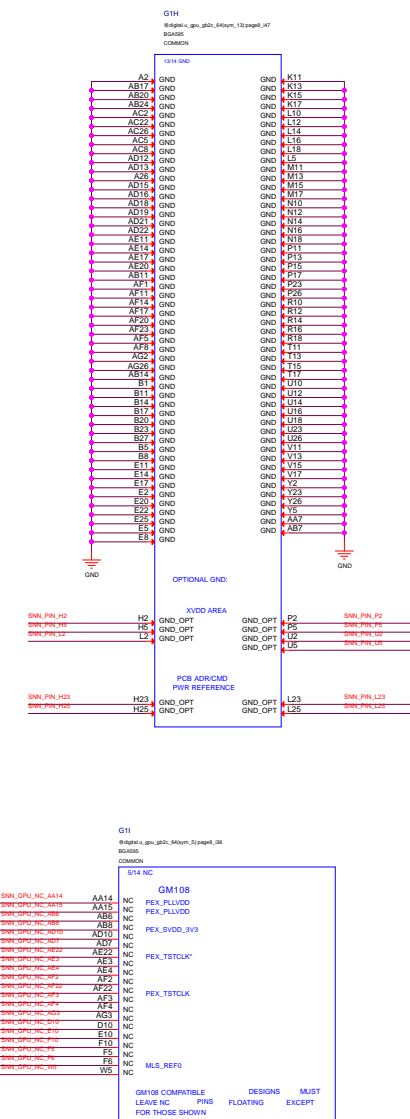
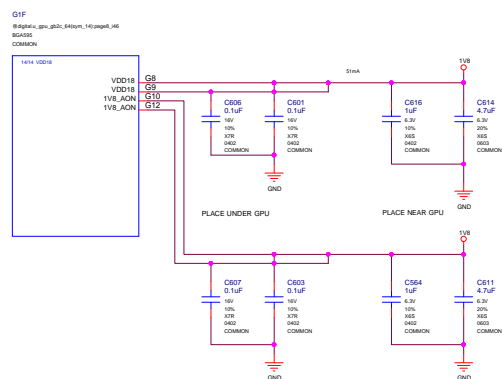
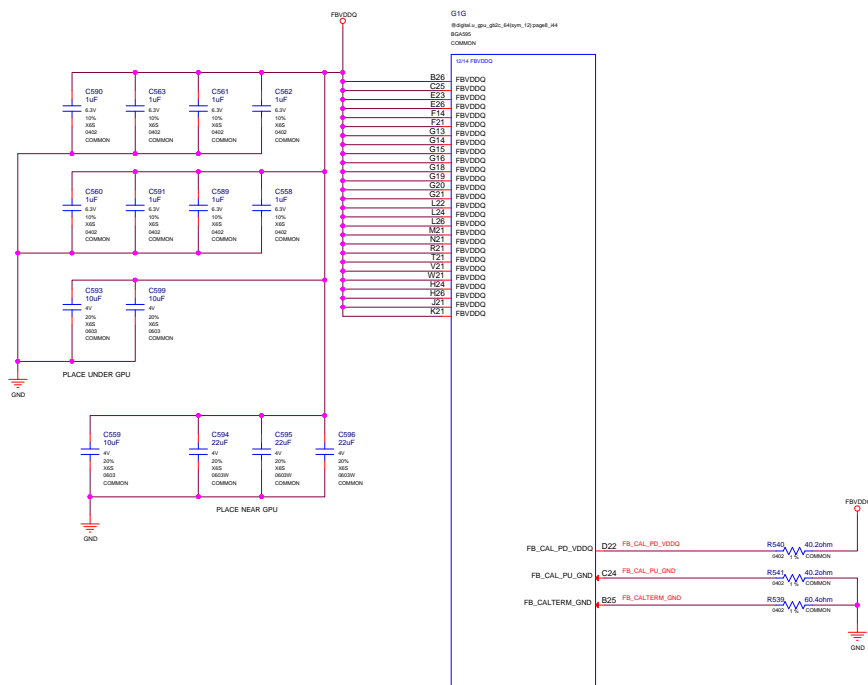


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FBVDDQ and 1V8 Decoupling



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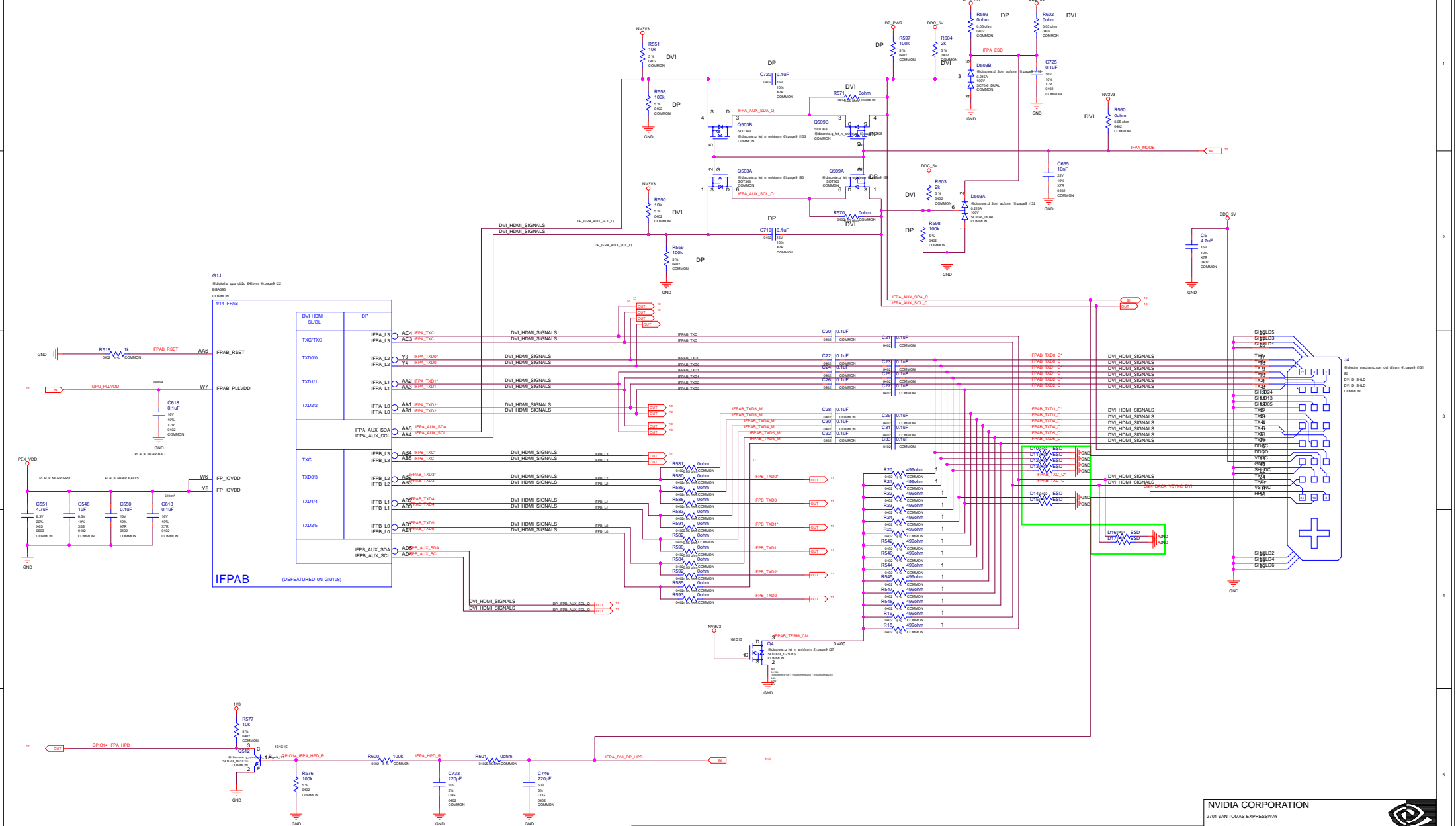
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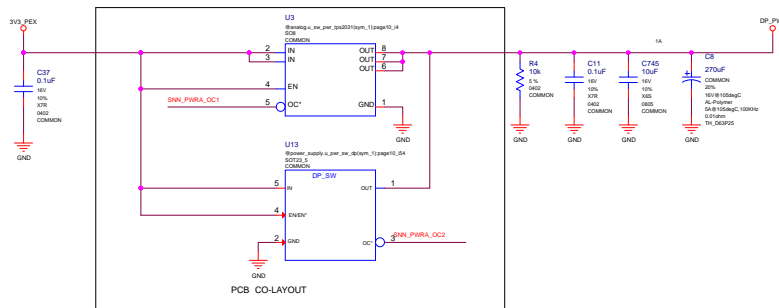
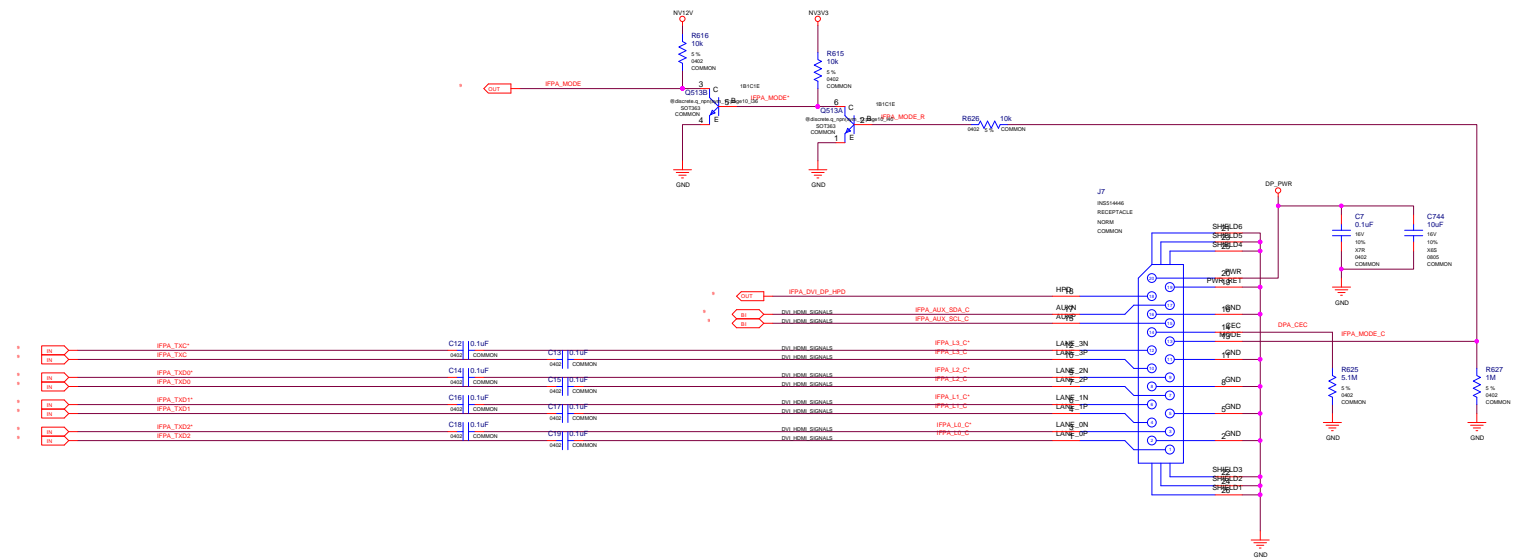
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PAGE DETAIL	FBVDDQ and 1V8 Decoupling

IFPAB DL DVI-D



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IFPA DP



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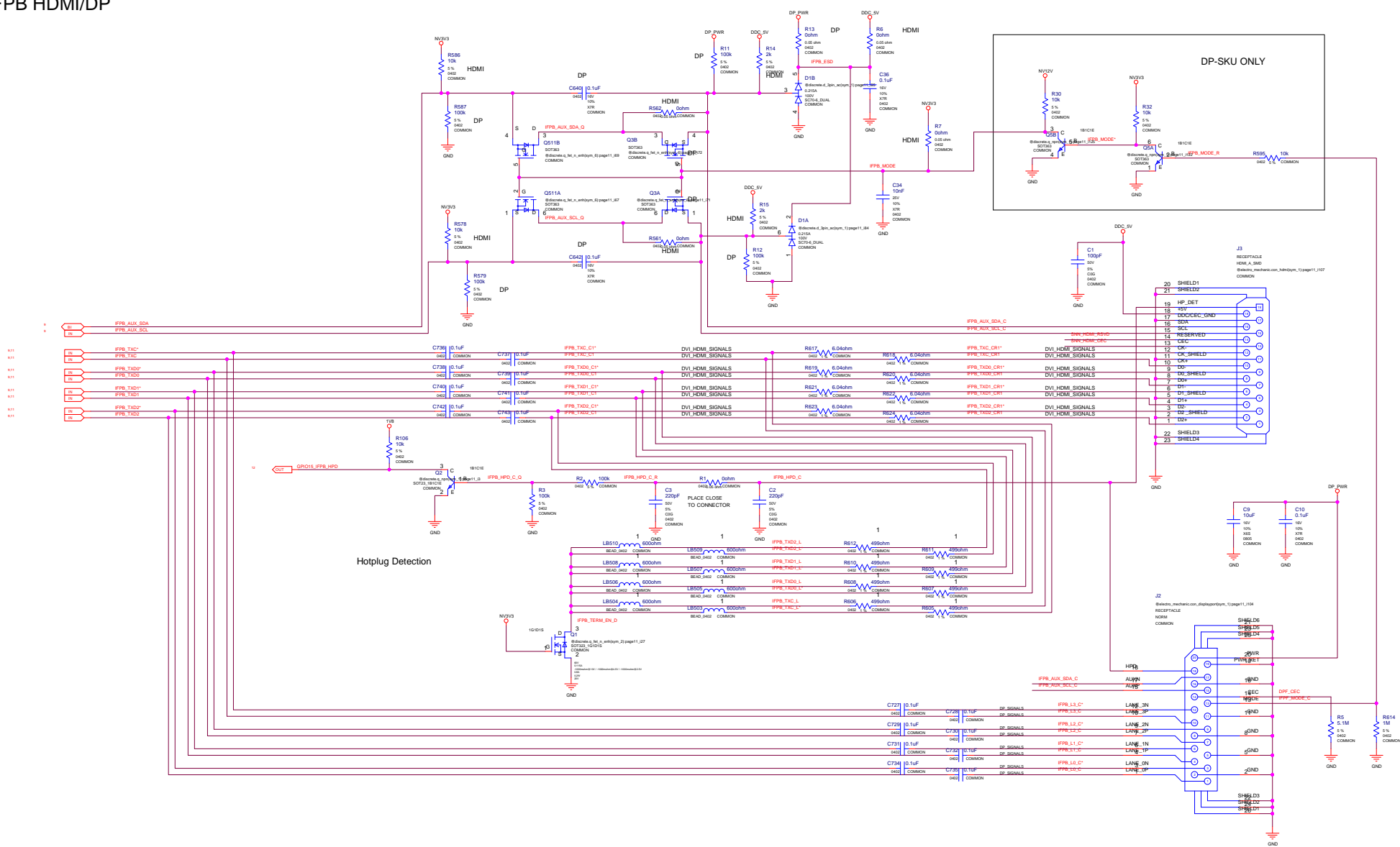
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IFPB HDMI/DP



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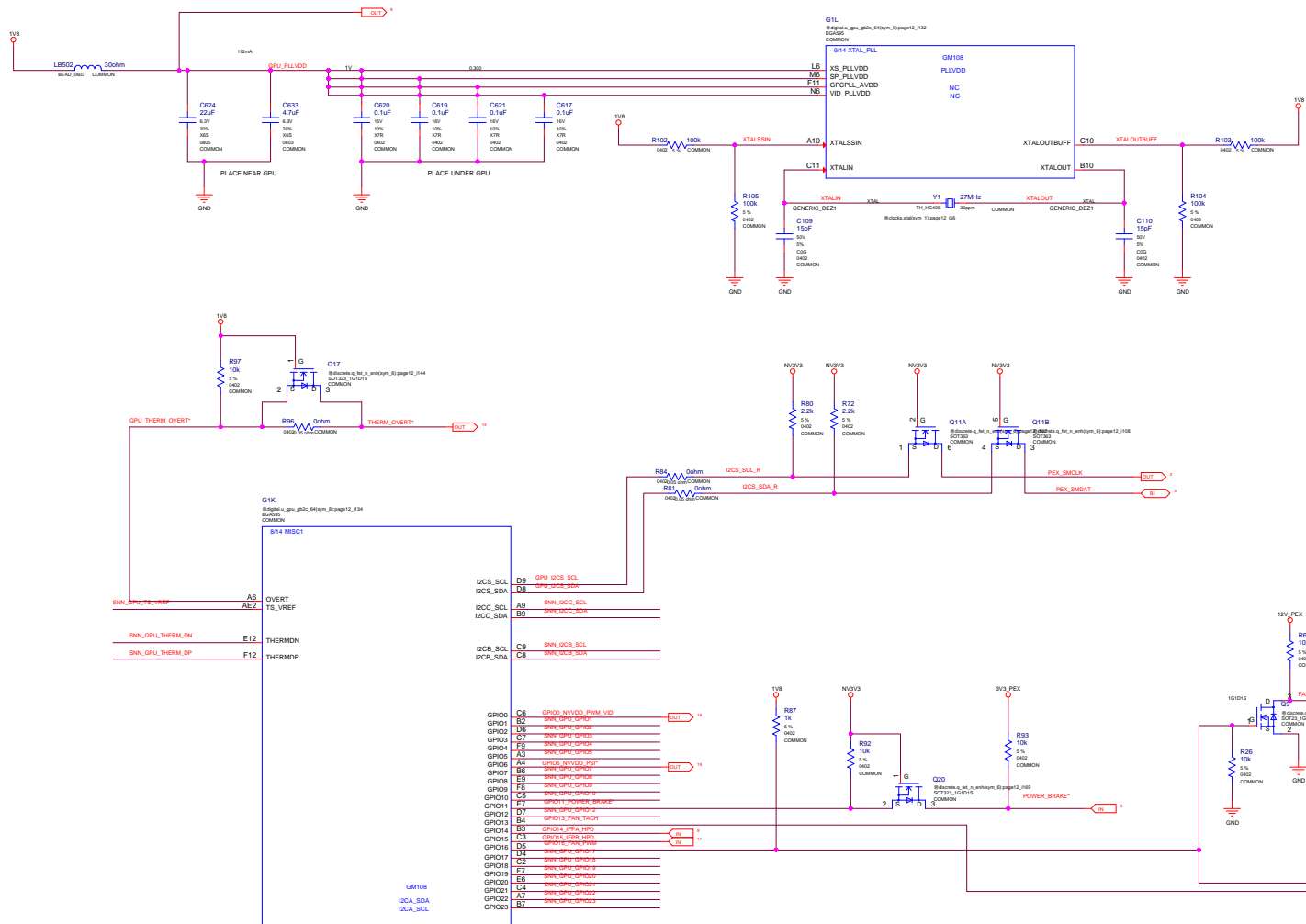
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JTAG,GPIO&XTAL



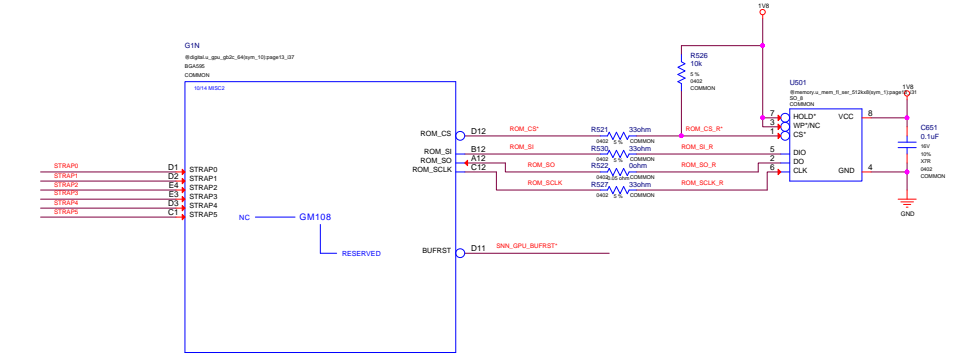
ROM & STRAPS

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L	L	L	1111	DEFAULT	SOR0/1 ENABLE
L	L	H	1110		
L	H	L	1101		
L	H	H	1100		
H	L	L	1011		
H	L	H	1010		
H	H	L	1001		
H	H	H	1000		
L	L	M	0111		
L	M	L	0110		
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H	L	M	0011		
H	M	L	0010		
H	M	H	0001		
H	H	M	0000		

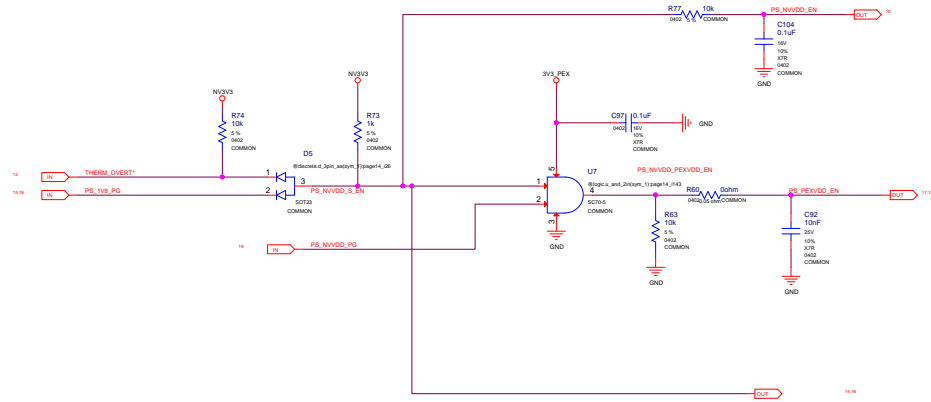
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L	L	H	0001
L	H	L	0010
L	H	H	0011
H	H	L	0110
H	H	H	0111
L	L	M	1000
L	M	L	1001

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V



Power Sequence



ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	Power Sequence

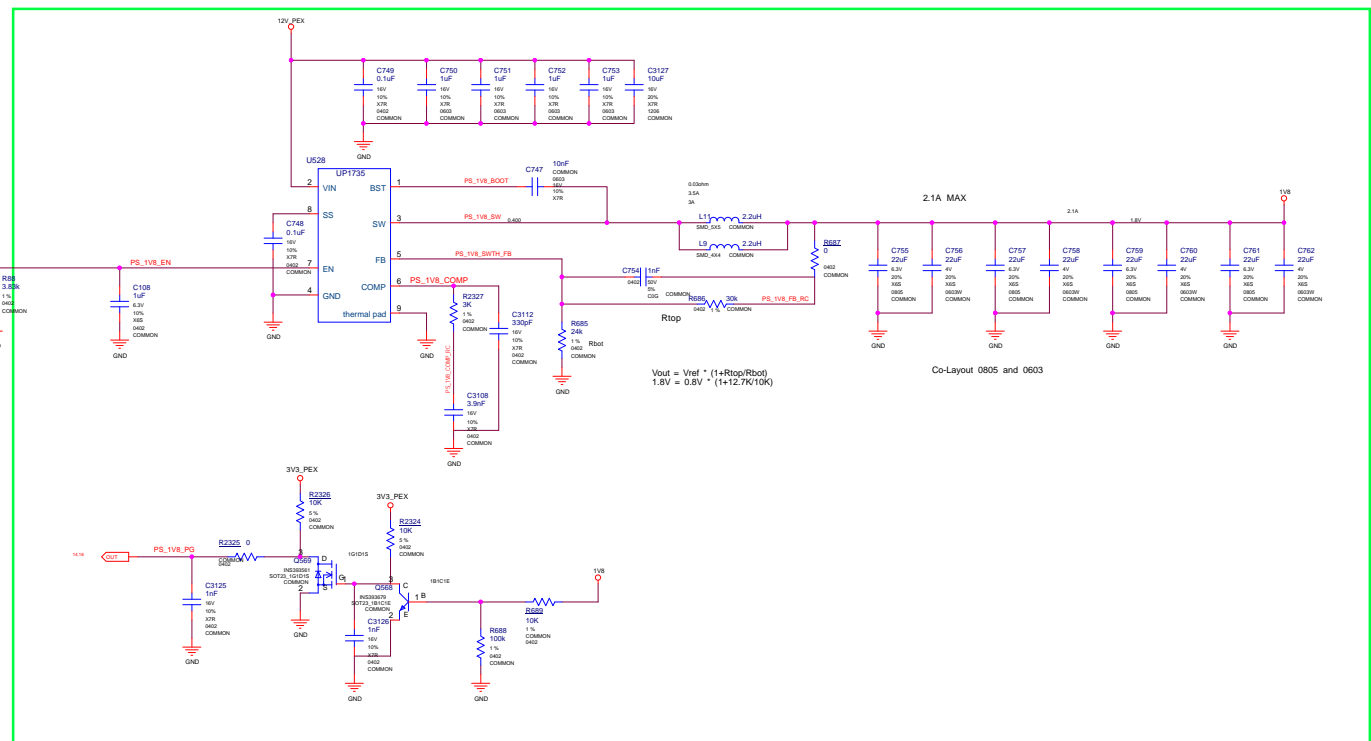
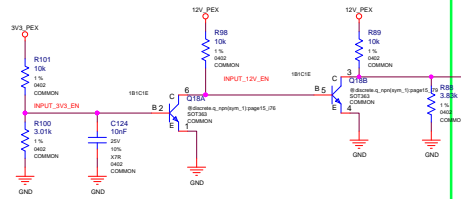
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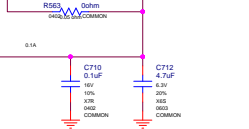
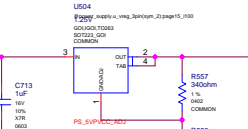
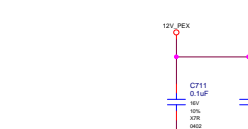
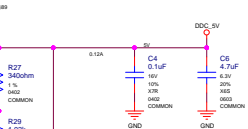
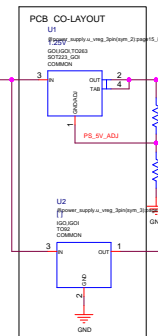
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POWER:1V8 & 5V



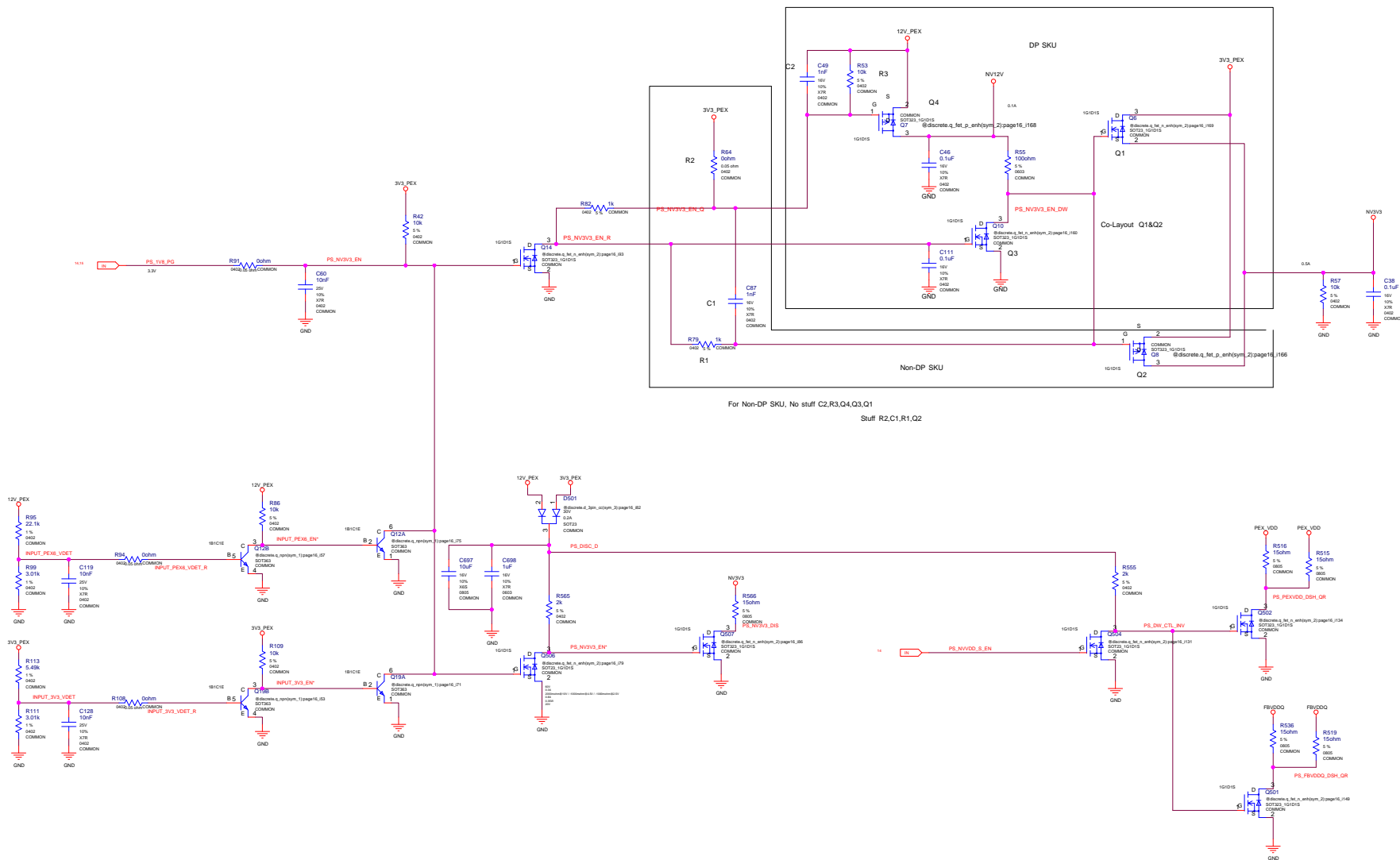
5V = 5V @ 120mA



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POWER: NV3V3, NV12V



For Non-DP SKU, No stuff C2,R3,Q4,Q3,Q1
Stuff R2,C1,R1,Q2

ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	POWER: NV3V3,NV12V

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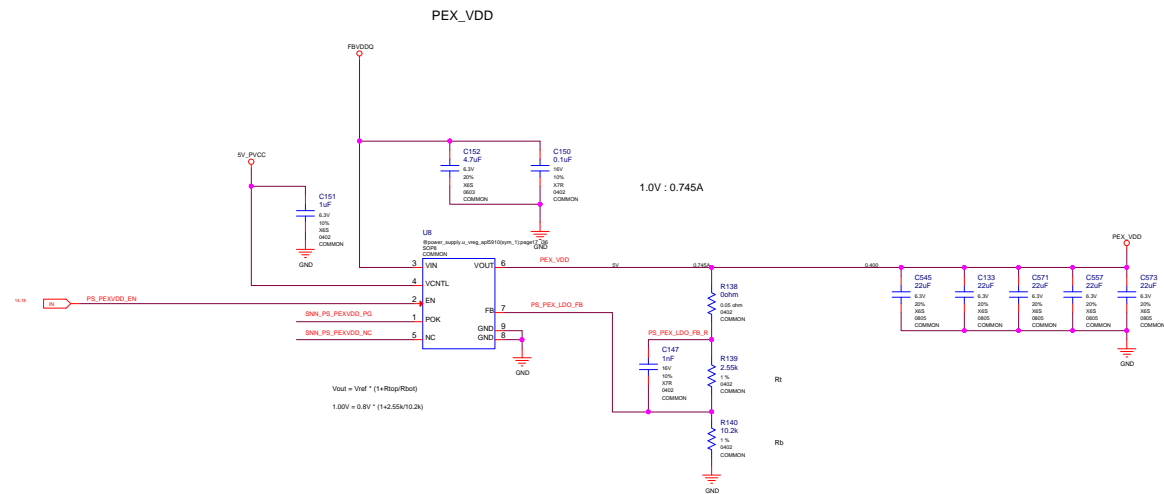
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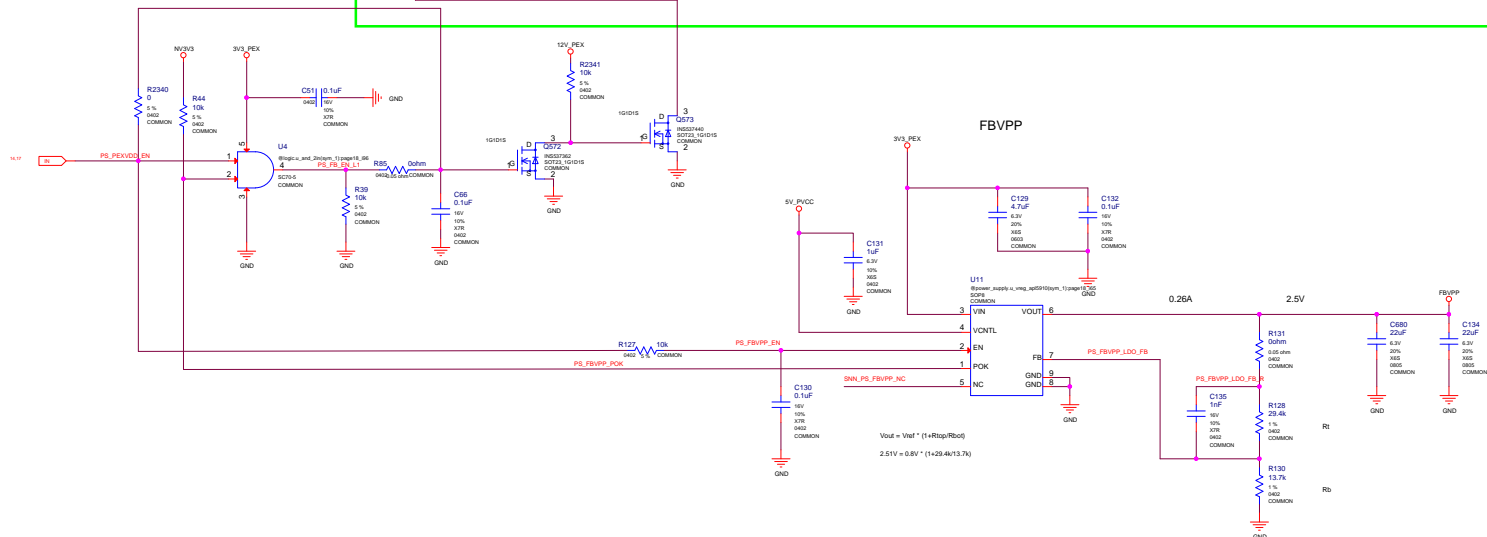
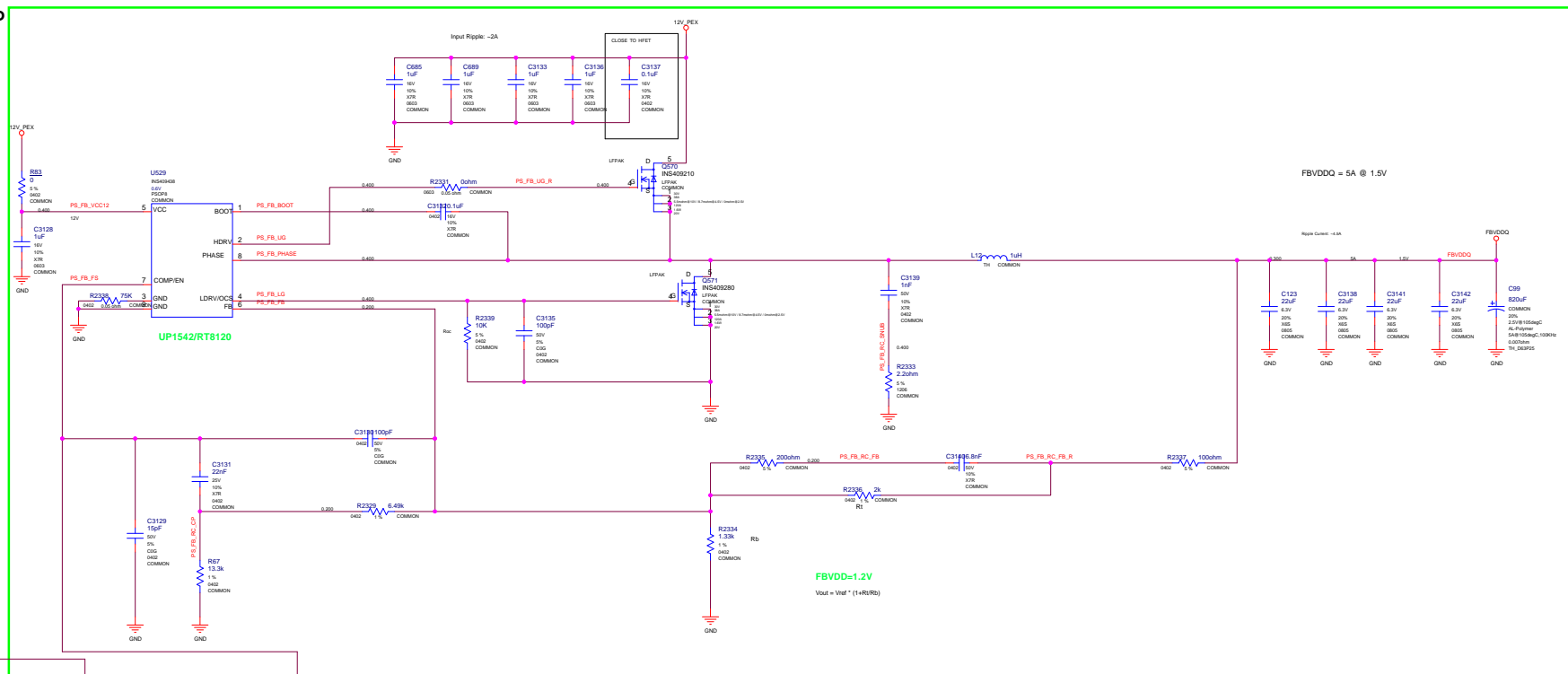
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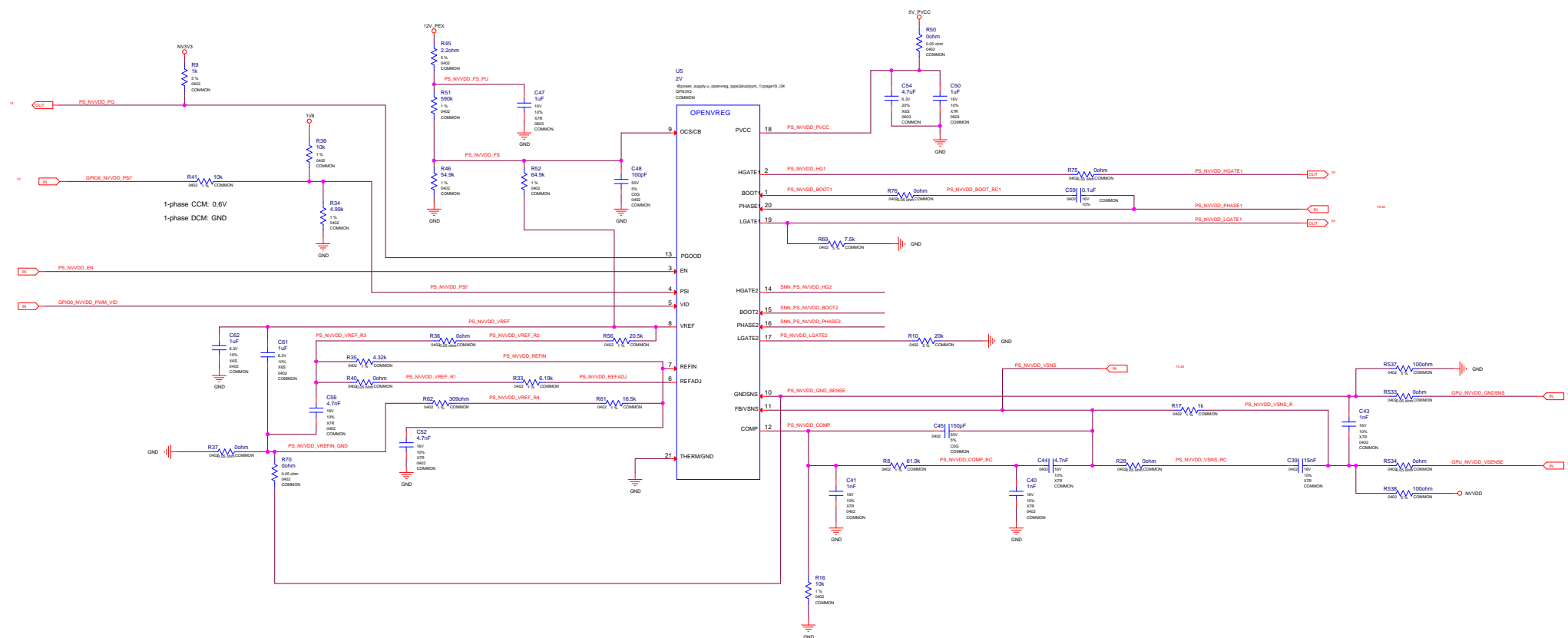
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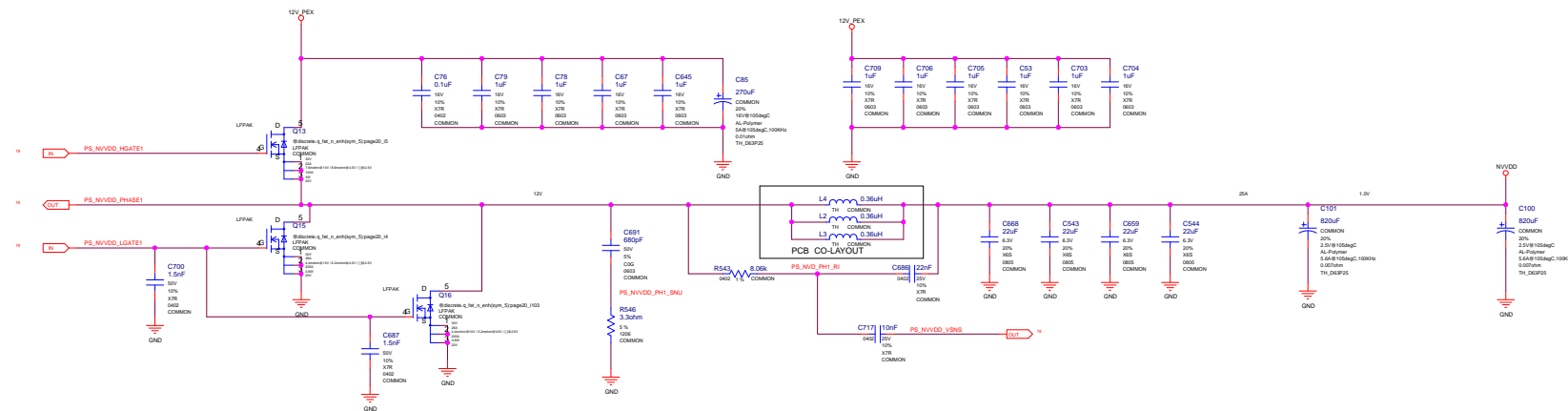
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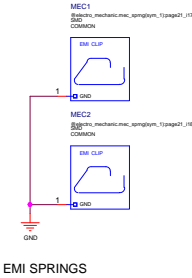
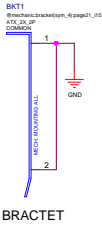
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