

P815-D00: G96 MXM V3.0  
128/256MB 128-BIT GDDR3  
LVDS, QUAD DP

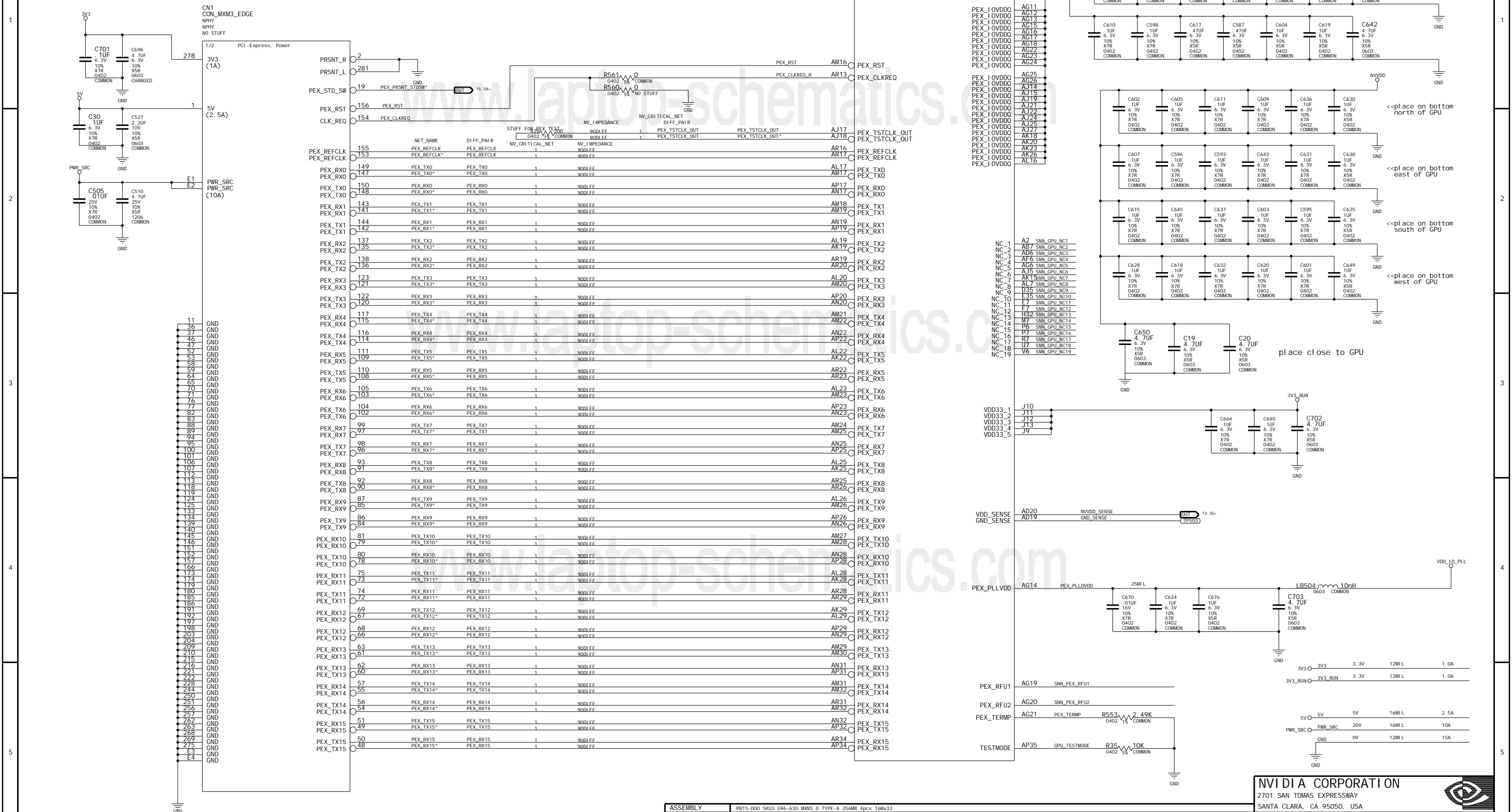
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SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10815-base-300	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
1	SKU0000	600-10815-0000-300	GRAM 128bit GDDR3 MXM V3.0
2	SKU0001	600-10815-0001-300	P815-D00 SKU1 G96-600 MXM3.0 TYPE-B 512MB 4pcs 32Mx32
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

PAGE 2) MXM-11 GOLDEN EDGE, PCI EXPRESS INTERFACE

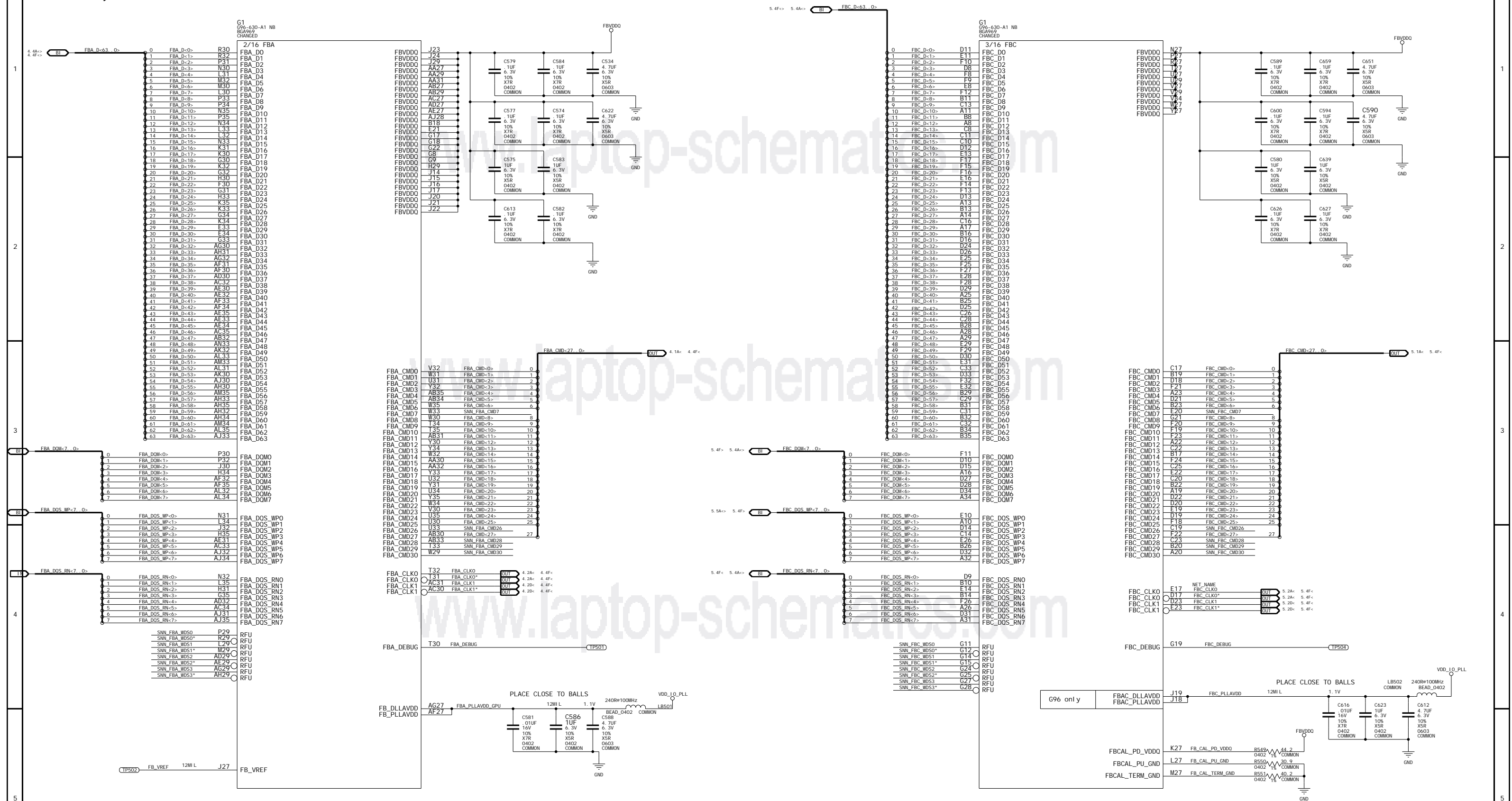


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ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	PCI EXPRESS Interface

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NV_PN	600-10815-0003-300 A		
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NAME	hl u	DATE	15-MAY-2008

PAGE 3) GPU MEMORY INTERFACE



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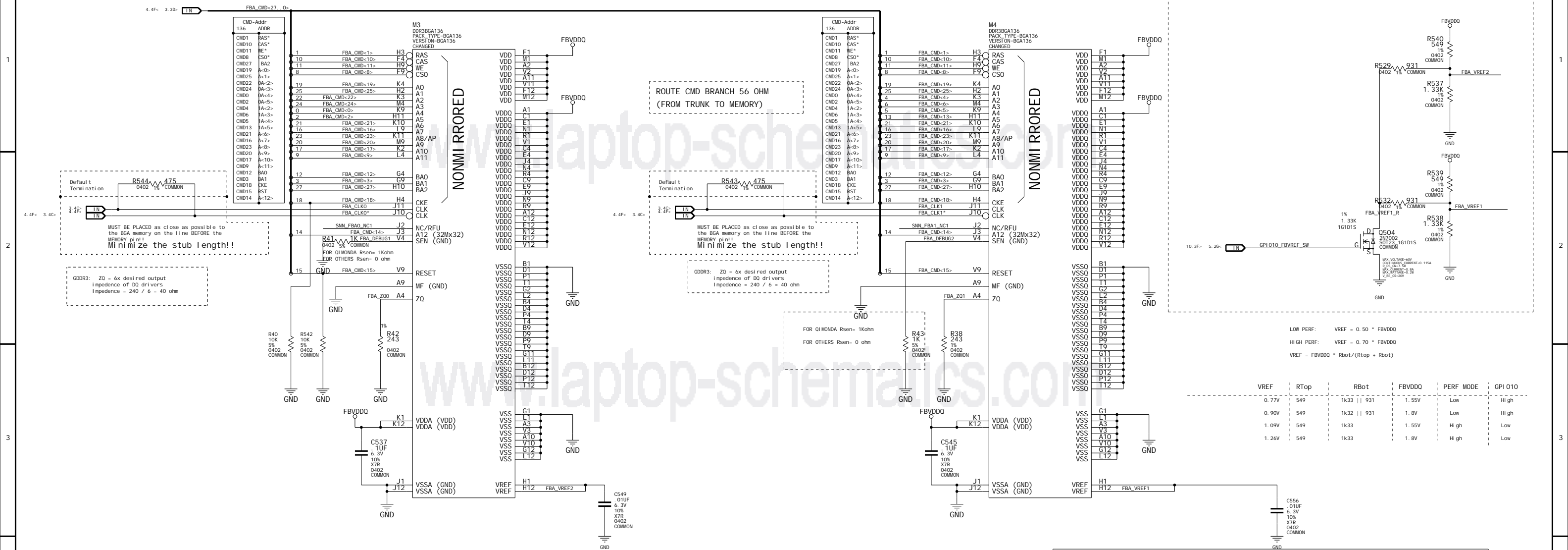
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FRAME BUFFER PARTITION A



NET RULES for FrameBuffer A

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBA_CLK0	1	80DI FF	FBA_CLK0
FBA_CLK0*	1	80DI FF	FBA_CLK0
FBA_CLK1	1	80DI FF	FBA_CLK1
FBA_CLK1*	1	80DI FF	FBA_CLK1

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBA_VREF0	1.26V	0.02A	12MI L
FBA_VREF1	1.26V	0.02A	12MI L
FBA_VREF2	1.26V	0.02A	12MI L
FBA_VREF3	1.26V	0.02A	12MI L
FBA_Z00	1.26V	0.02A	12MI L
FBA_Z01	1.26V	0.02A	12MI L

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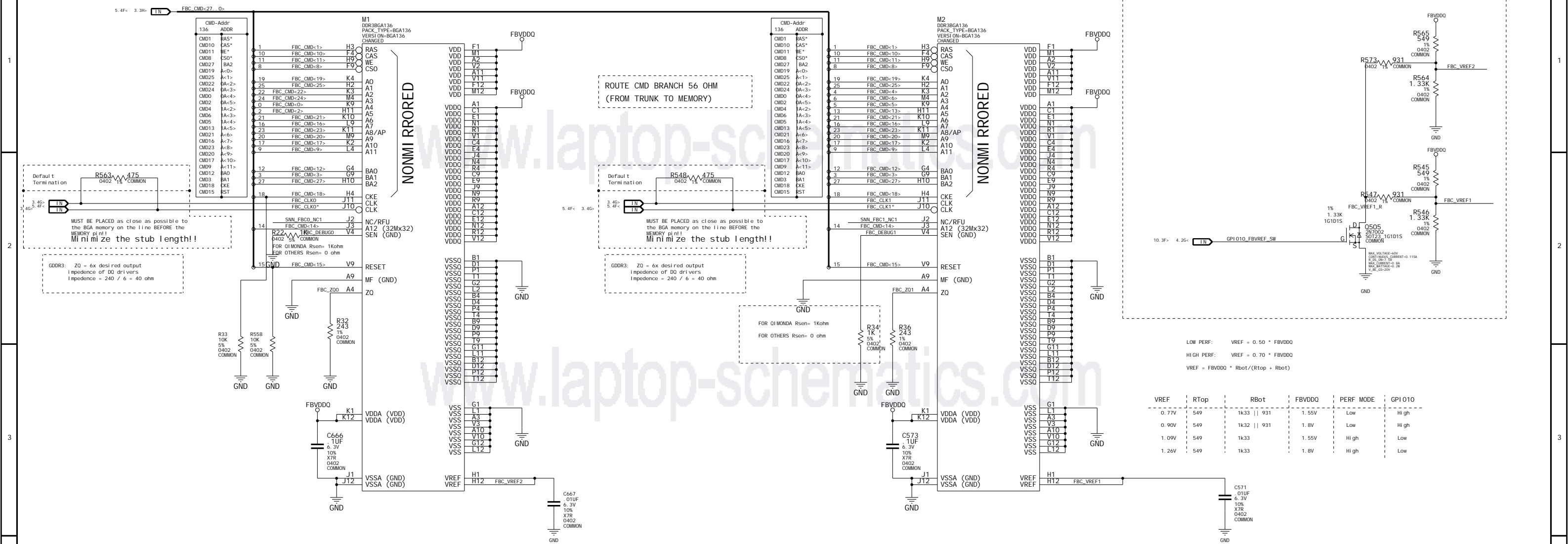
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ASSEMBLY	P815-D00 SKU3 G96-630 MM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	Frame Buffer Partition A Memories

NV_PN	600-10815-0003-300 A		
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## PAGE 5) MEMORY PARTITION C

NET RULES for FrameBuffer C

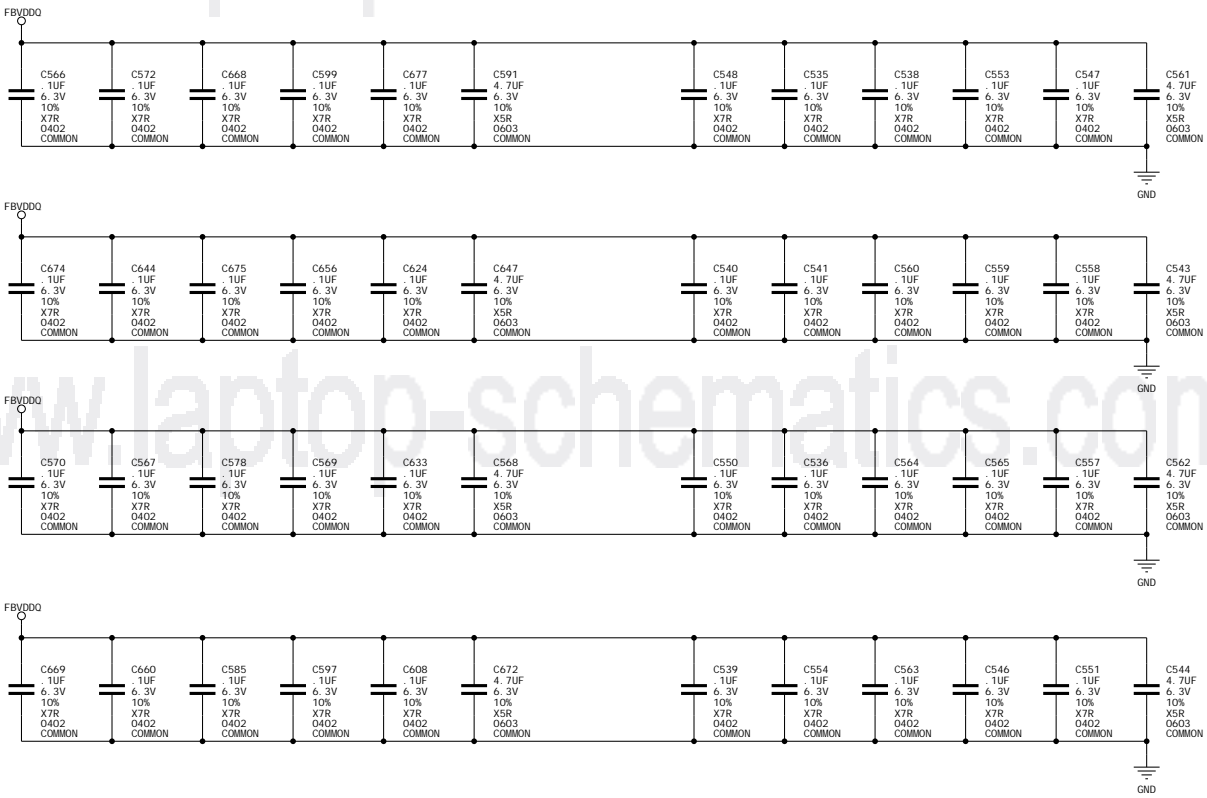
	NET	NV_CR1 TI CAL	NV_I MPEDANCE	DI FFPAI R
5.2K~ 3.4G	 FBC_CLK0	1	80DI FF	FBC_CLK0
5.2K~ 3.4G	 FBC_CLK0*	1	80DI FF	FBC_CLK0
5.2K~ 3.4G	 FBC_CLK1	1	80DI FF	FBC_CLK1
5.2K~ 3.4G	FBC_CLK1*	1	80DI FF	FBC_CLK1

5.1Ae	5.5Ae < 3.3D <	OUT	FBC DGS WP<7, 0>	1	400HM
	5.4Ae < 3.4D <	IN	FBC DGS RM<7, 0>	1	400HM
	5.4Ae < 3.3D <	OUT	FBC DM<7, 0>	1	400HM
	3.1E < 5.4Ae <	BI	FBC D<63, 0>	1	400HM
	3.3H <	IN	FBC DM<27, 0>	1	600HM

NET		VOLTAGE	MAX_CURRENT	MIN_WI_DTH
	FBC_VREF0	1.26V	0.02A	12MM L
	FBC_VREF1	1.26V	0.02A	12MM L
	FBC_VREF2	1.26V	0.02A	12MM L
	FBC_VREF3	1.26V	0.02A	12MM L
	FBC_Z00	1.26V	0.02A	12MM L
	FBC_Z01	1.26V	0.02A	12MM L

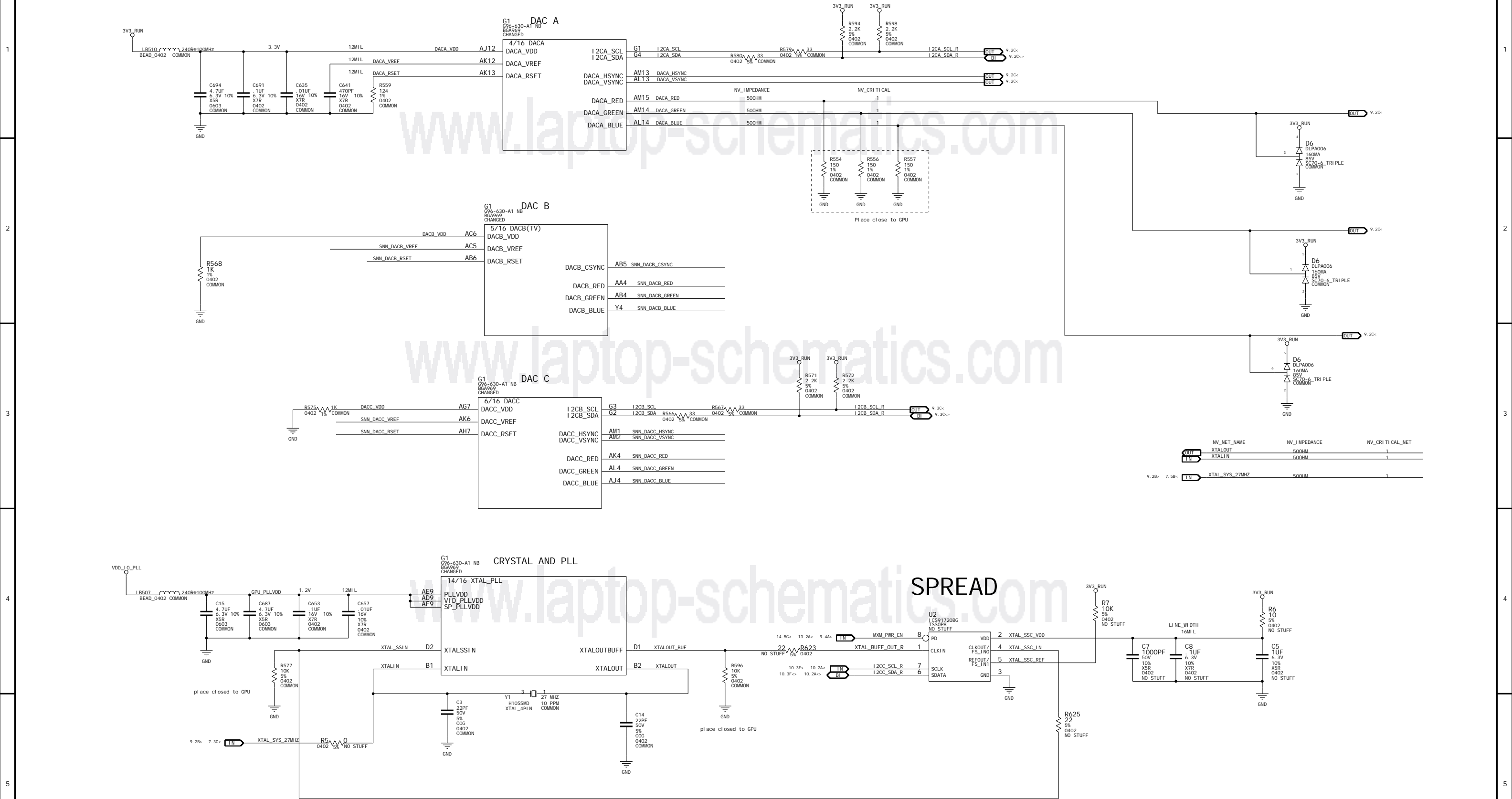


DECOUPLING CAPS FOR MEMORYS (PARTION A AND PARTION C)



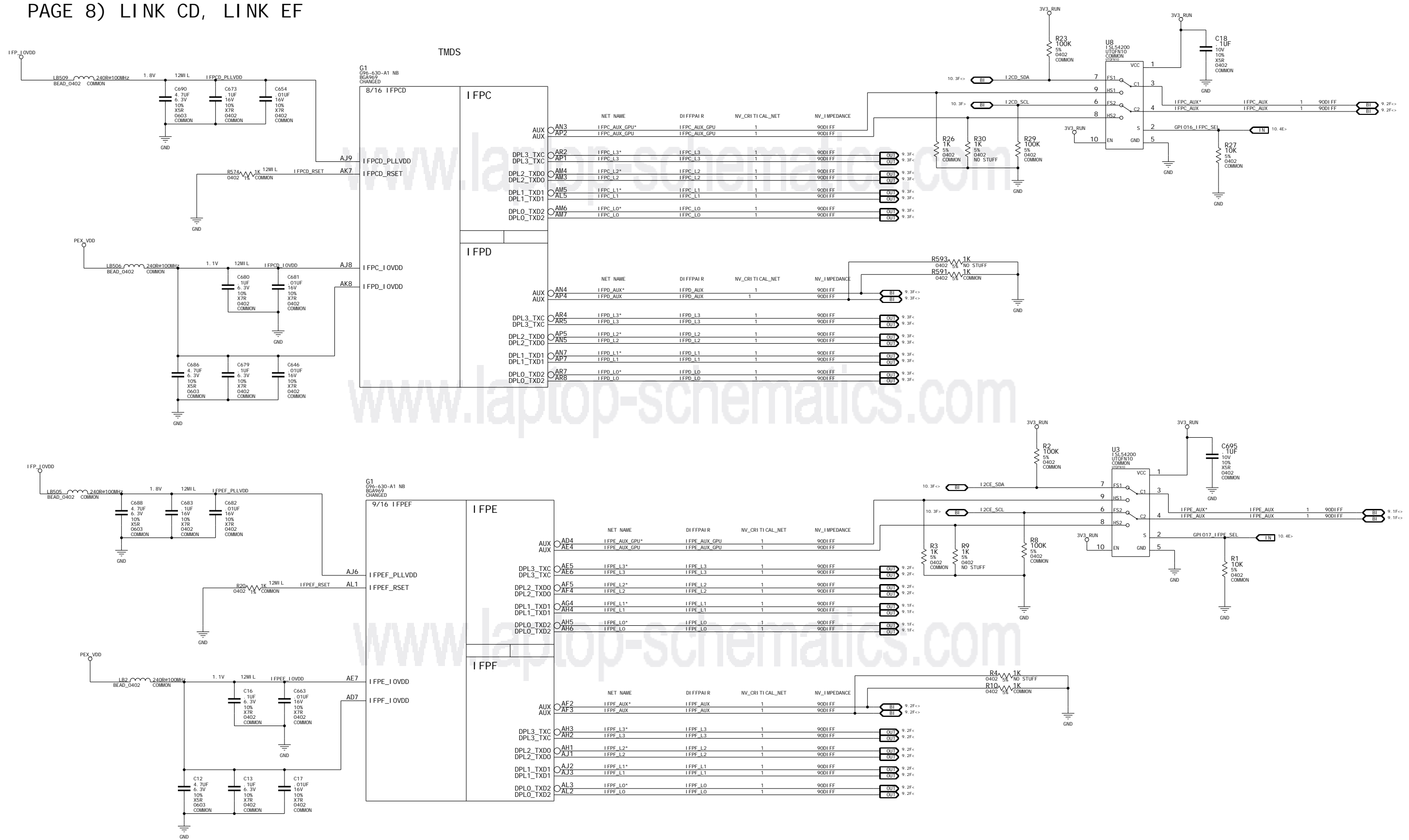
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PAGE 7) DAC\_A, DAC\_B, DAC\_C, PLL, CRYSTAL



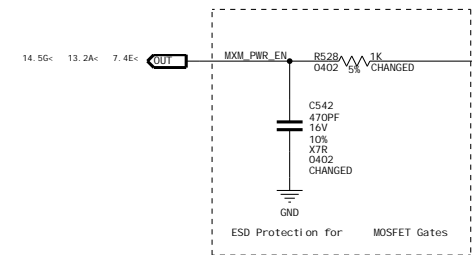
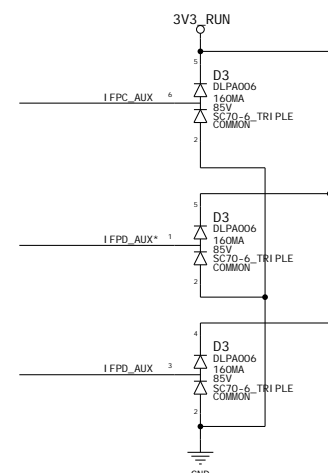
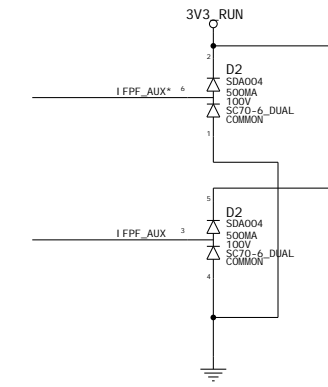
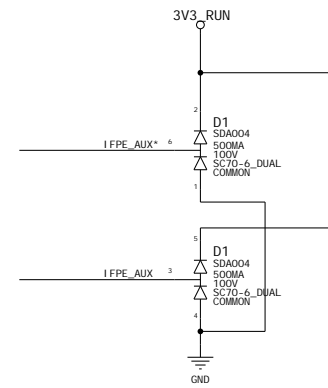
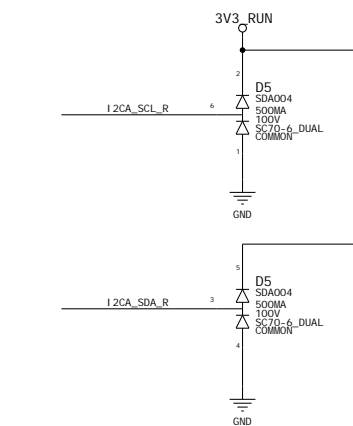
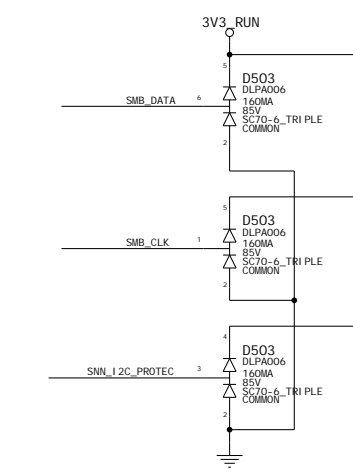
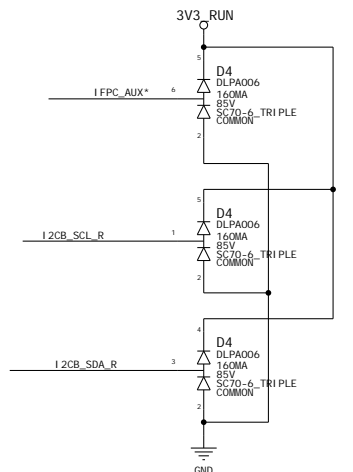
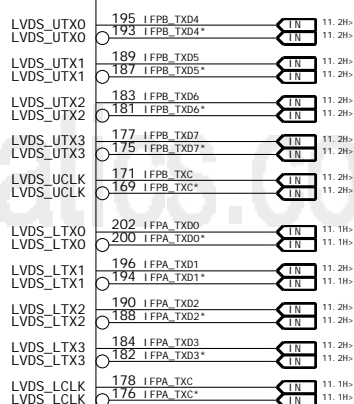
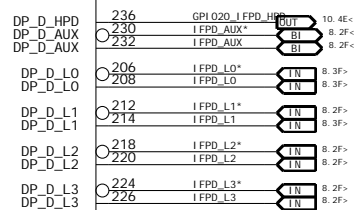
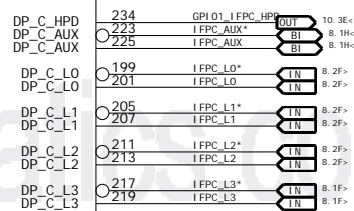
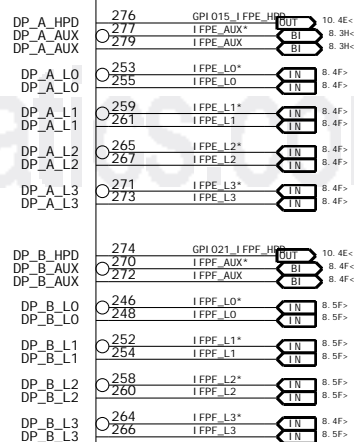
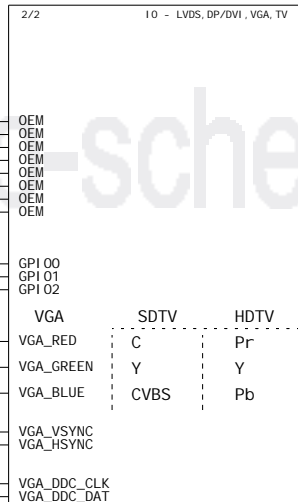
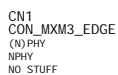
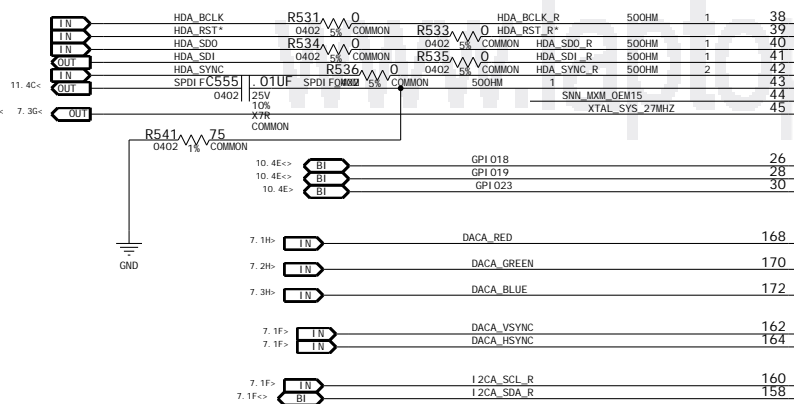
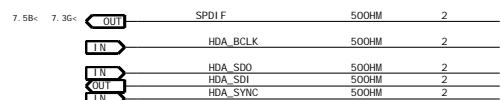
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PAGE 8) LINK CD, LINK EF



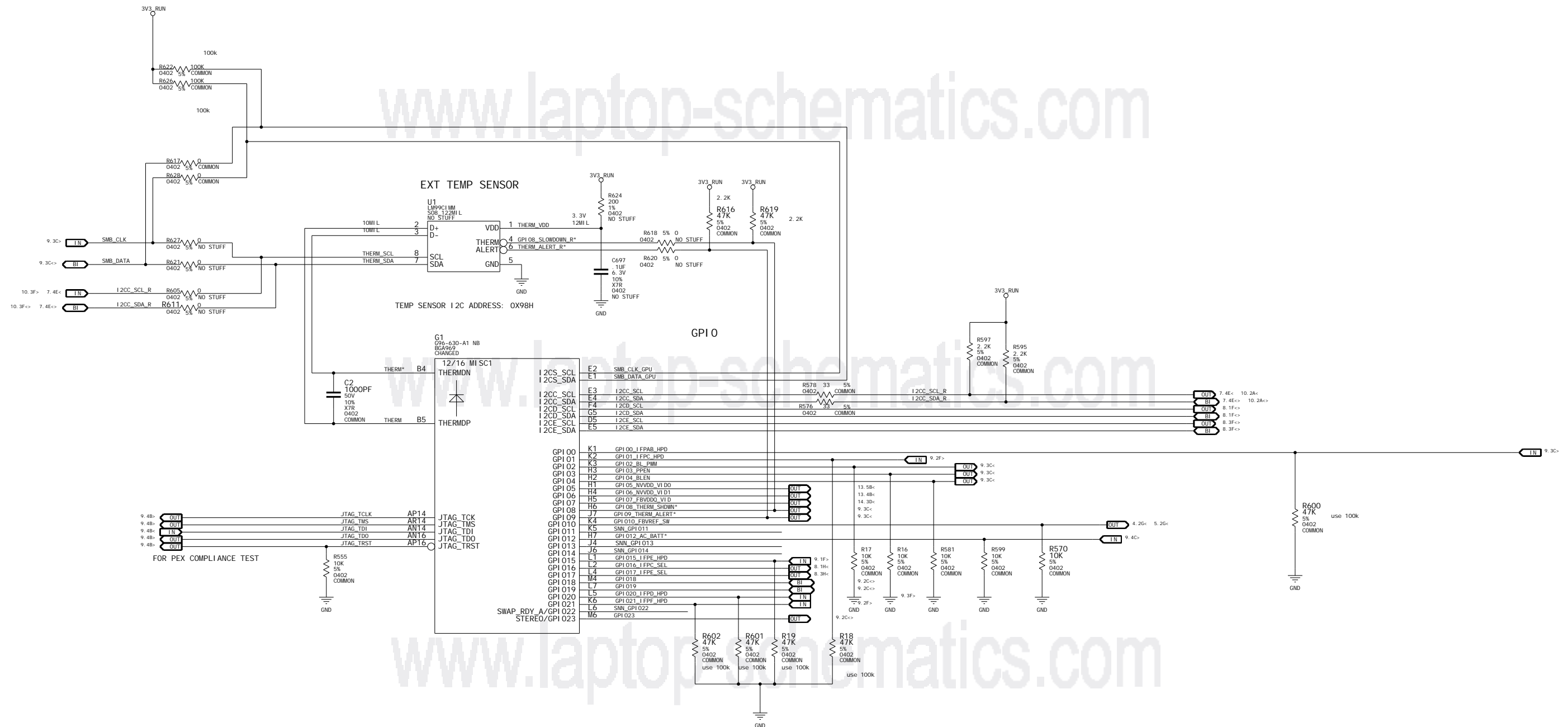


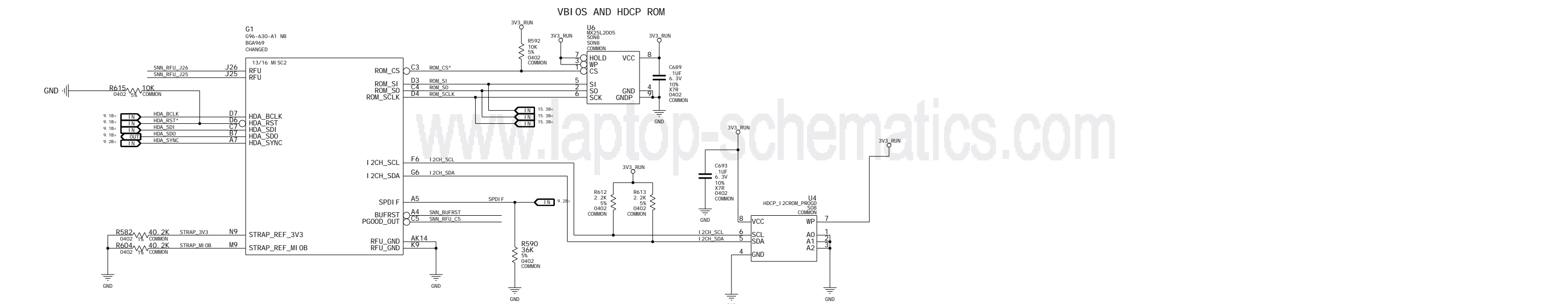
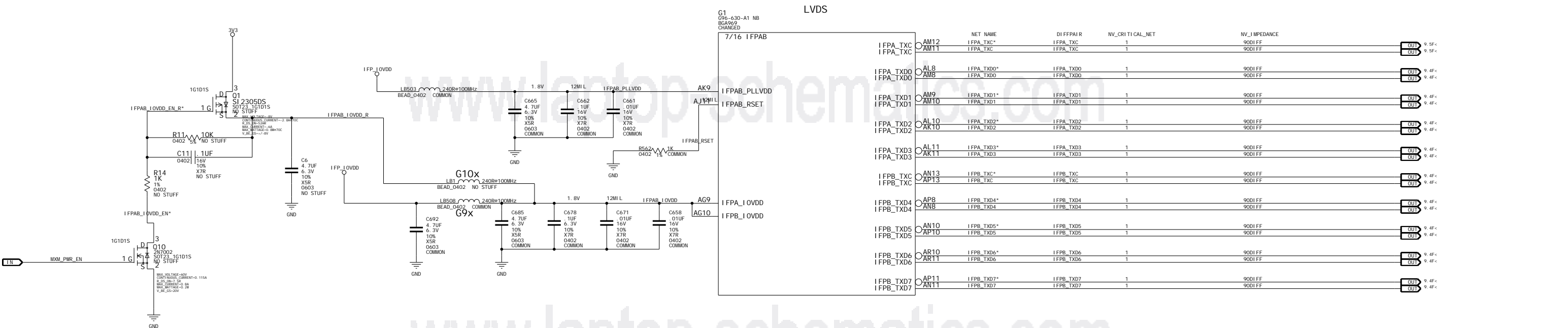
## MXM CONNECTOR

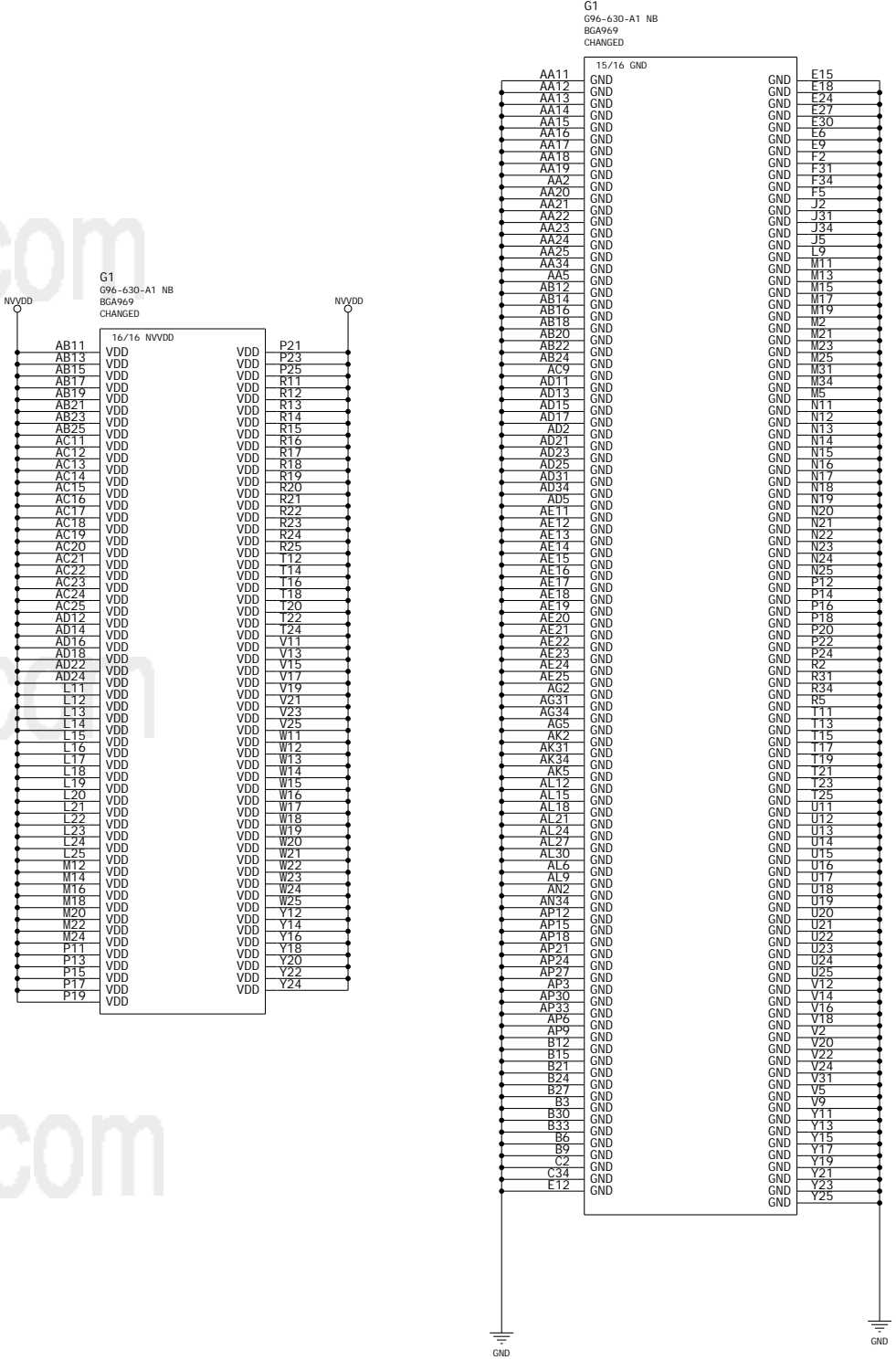
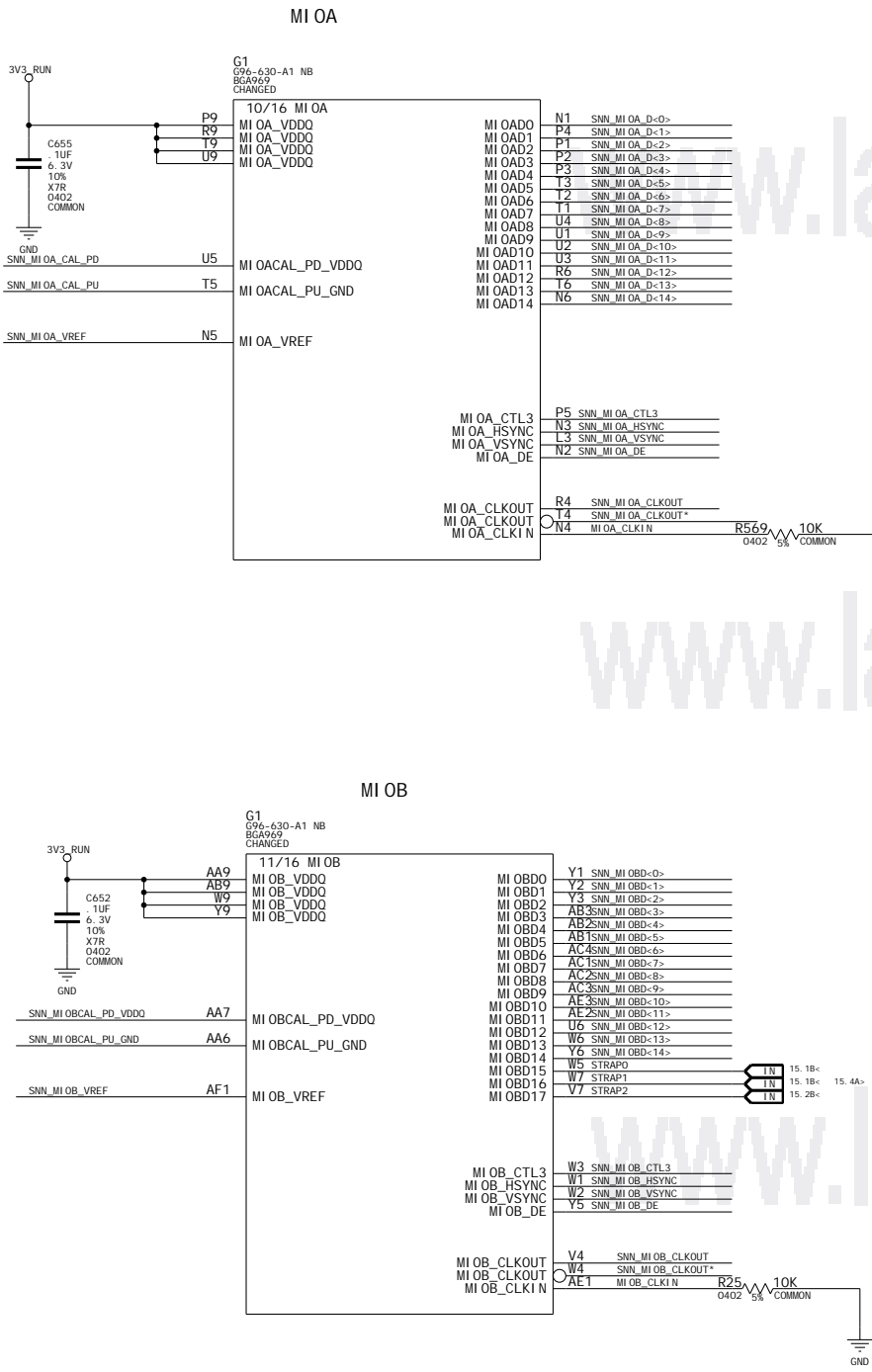


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PAGE DETAIL	MXM Connector, 10-Section

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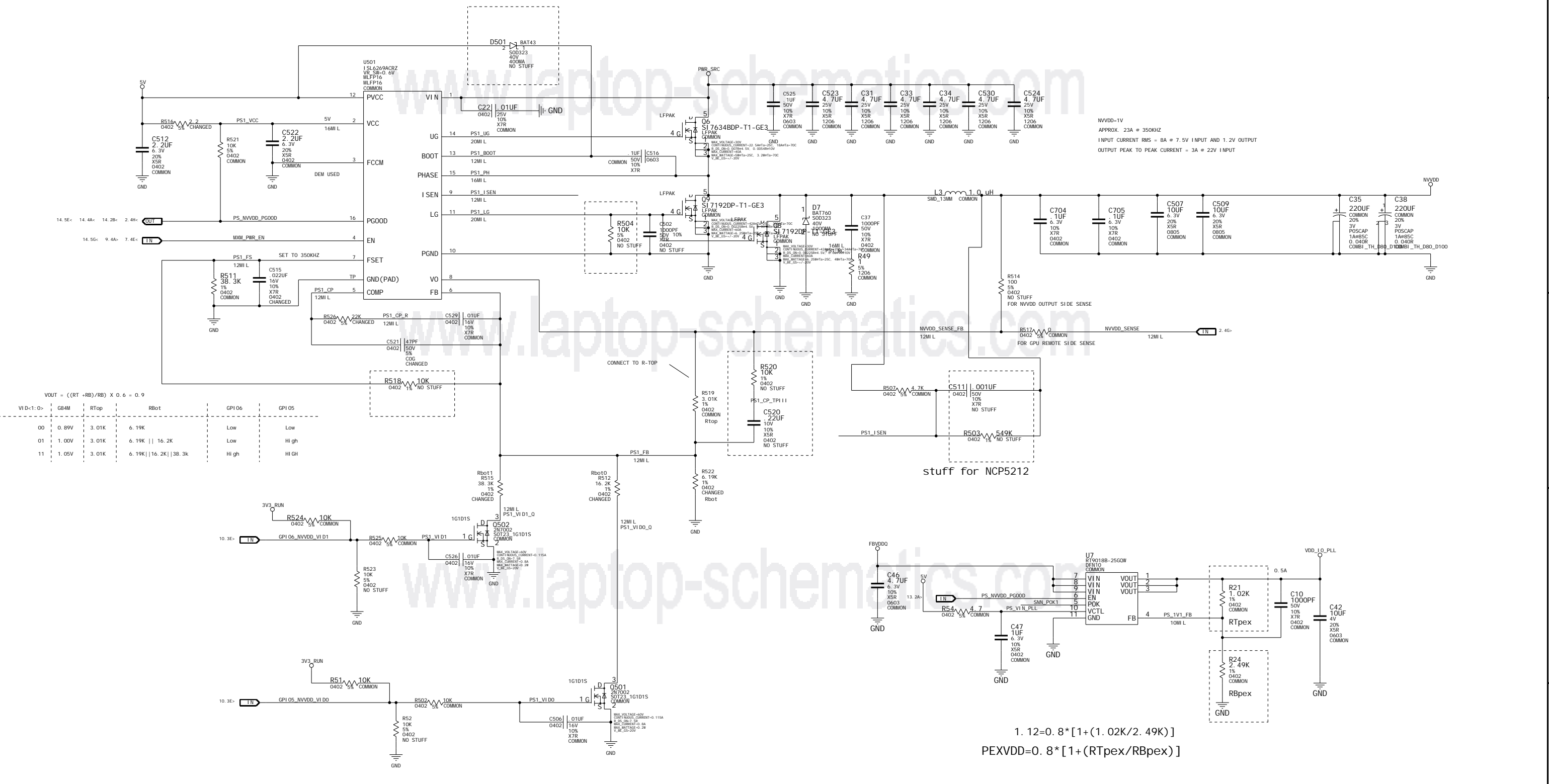


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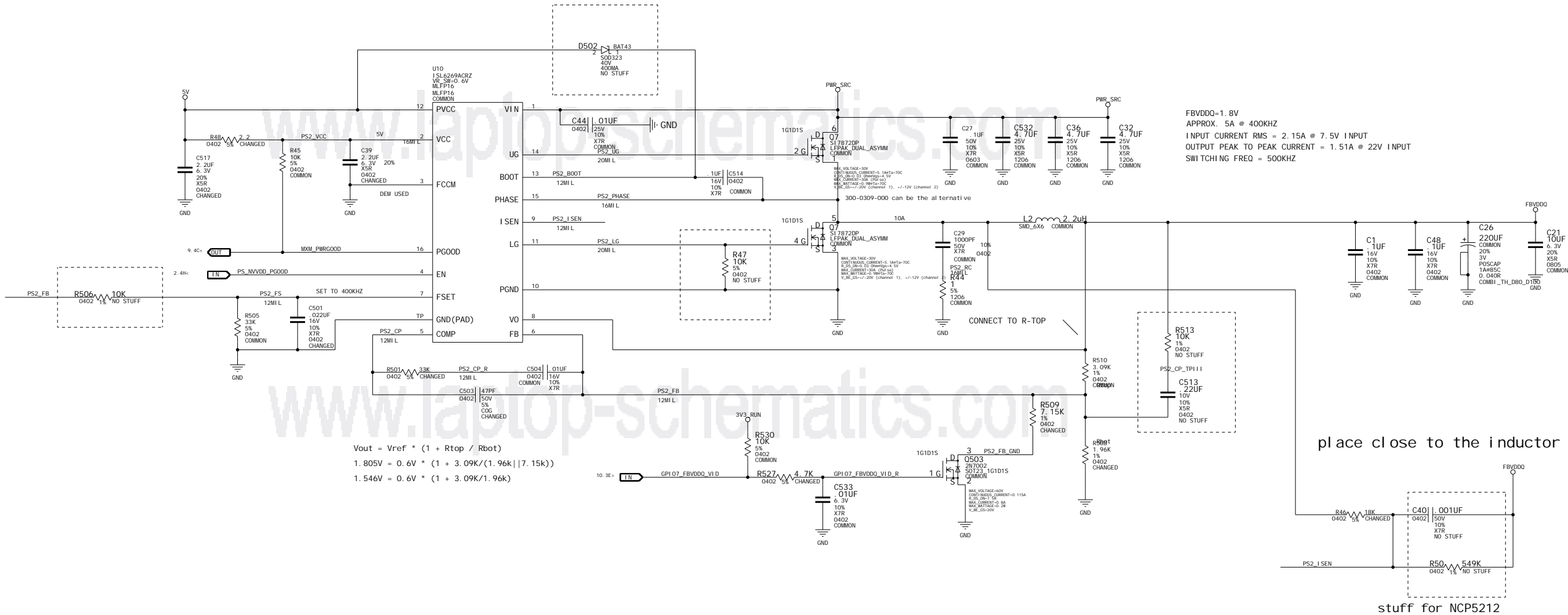
ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	MI OA, MI OB, GPU GND

NET	VOLTAGE	MIN_WI DTH_LI NE	NV_NET_MAX_CURRENT
NVVDD	1V	12MI L	30A

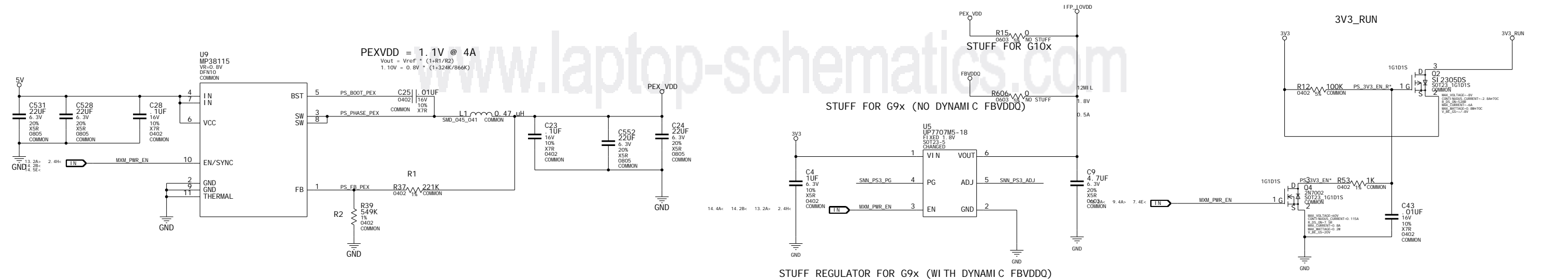




NET	VOLTAGE	MI_N_WI_OTH_LI_NE	NV_NET_MAX_CURRENT
PEX_VDD	PEX_VDD	1.2V	12MI L
FBVDDQ	FBVDDQ	1.8V	12MI L
PS_VI_N_PEX	PS_VI_N_PEX	12MI L	10A



$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$   
 $1.805V = 0.6V * (1 + 3.09K / (1.96K || 7.15K))$   
 $1.546V = 0.6V * (1 + 3.09K / 1.96K)$

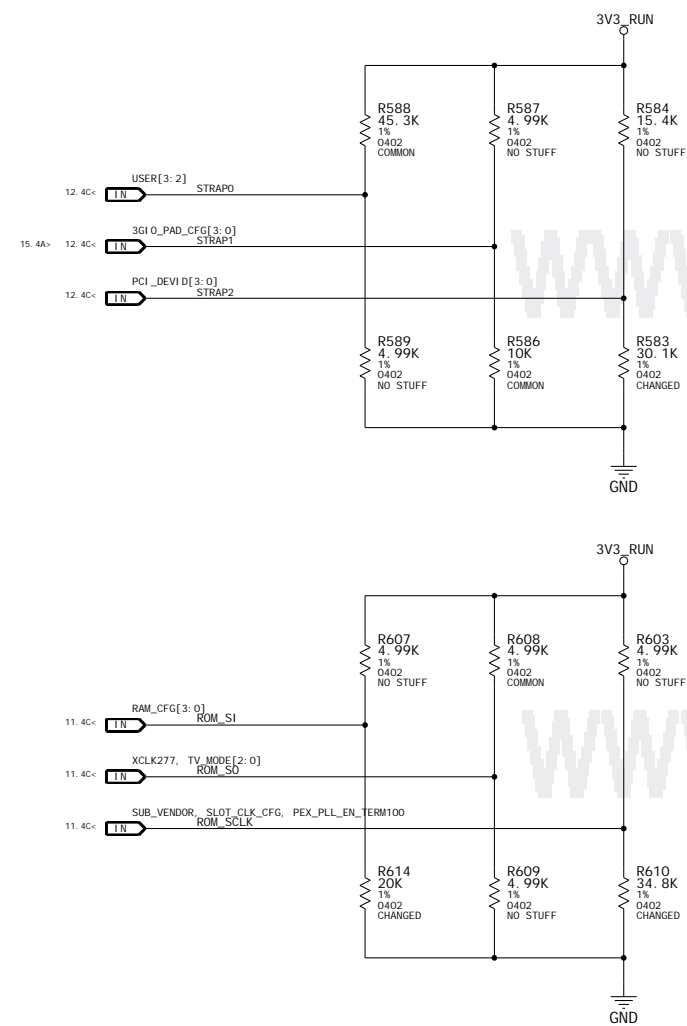


$PEXVDD = 1.1V @ 4A$   
 $V_{out} = V_{ref} * (1 + R1 / R2)$   
 $1.10V = 0.6V * (1 + 324K / 866K)$

STUFF REGULATOR FOR G9x (WITH DYNAMIC FBVDDQ)

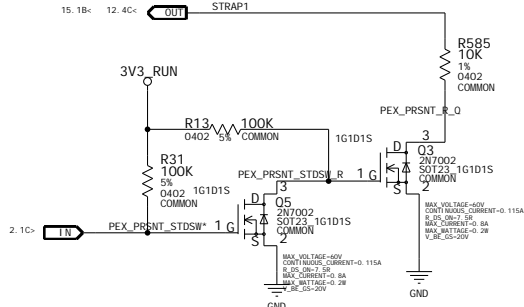
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ID	p815_d00	PAGE	14 OF 15
NAME	ntu	DATE	15-MAY-2008

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	3V3	GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

PEX\_PADCFG



PEX_PRSTNT_R*	R_STRAP1	3_GIO_PADCFG_LUT<3..0>
FLOAT	10k	0x1 MOBILE_DEFAULT
GND	5k (10k    10k)	0x0 DESKTOP_DEFAULT

STRAP0

STRAP1

STRAP2

ROM\_SI

ROM\_SI

ROM\_SCLK

USER_BIT0	0xF: 45K PU (unused)
USER_BIT1	
USER_BIT2	
USER_BIT3	
3GIO_PADCFG_LUT_ADR0	
3GIO_PADCFG_LUT_ADR1	0x0: Desktop default (normal swing) - 5k PD
3GIO_PADCFG_LUT_ADR2	0x1: Mobile default (low swing) - 10k PD
3GIO_PADCFG_LUT_ADR3	acc. to //hw/tesla_g98b/manuals/dev_ext_devices.ref
PCI_DEVICE0	all 4 bits set by HW strapping
PCI_DEVICE1	0x064A: 15K PU (NB9E-GE)
PCI_DEVICE2	
PCI_DEVICE3	
TV_MODE_BIT0	0x0: NTSC-M
TV_MODE_BIT1	5K PU
TV_MODE_BIT2	
XCLK_277	1: PCI-E GEN2
RAM_CFG_0	256 MB (4pcs. 16Mx32)
RAM_CFG_1	RAM_CFG[3:0] Definitions
RAM_CFG_2	0000 Reserved 0001 Qimonda 0010 Hynix 0011 Samsung
RAM_CFG_3	512 MB (4pcs. 32Mx32)
	RAM_CFG[3:0] Definitions
	0100 25k PD Reserved 0101 30k PD Qimonda 0110 35k PD Hynix 0111 45k PD Samsung
PCI_DEVICE_EXT	0:
SUB_VENDOR	1: SUB_VENDOR BIOS
SLOT_CLK_CONFIG	1:
PEX_PLL_EN_TERM100	1: TERM100 ENABLED

