MS-V069 -- G73GT, 128/256 Mb DDR3-136pin, VGA, DVI-I, SD/HDTV, VIVO,HDMI

SUMMARY:

1. Base on V060-120 to Modify
2. BGA-136 DDRIII
3. Dual MS-11 for NVVDD and FBVDD

Table of Contents:

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Page 23: FBVDD with MS-11
Page 24: EXTERNAL HDMI LINK SII1930
Page 25: Micro Controller & Audio DAC

Rev History

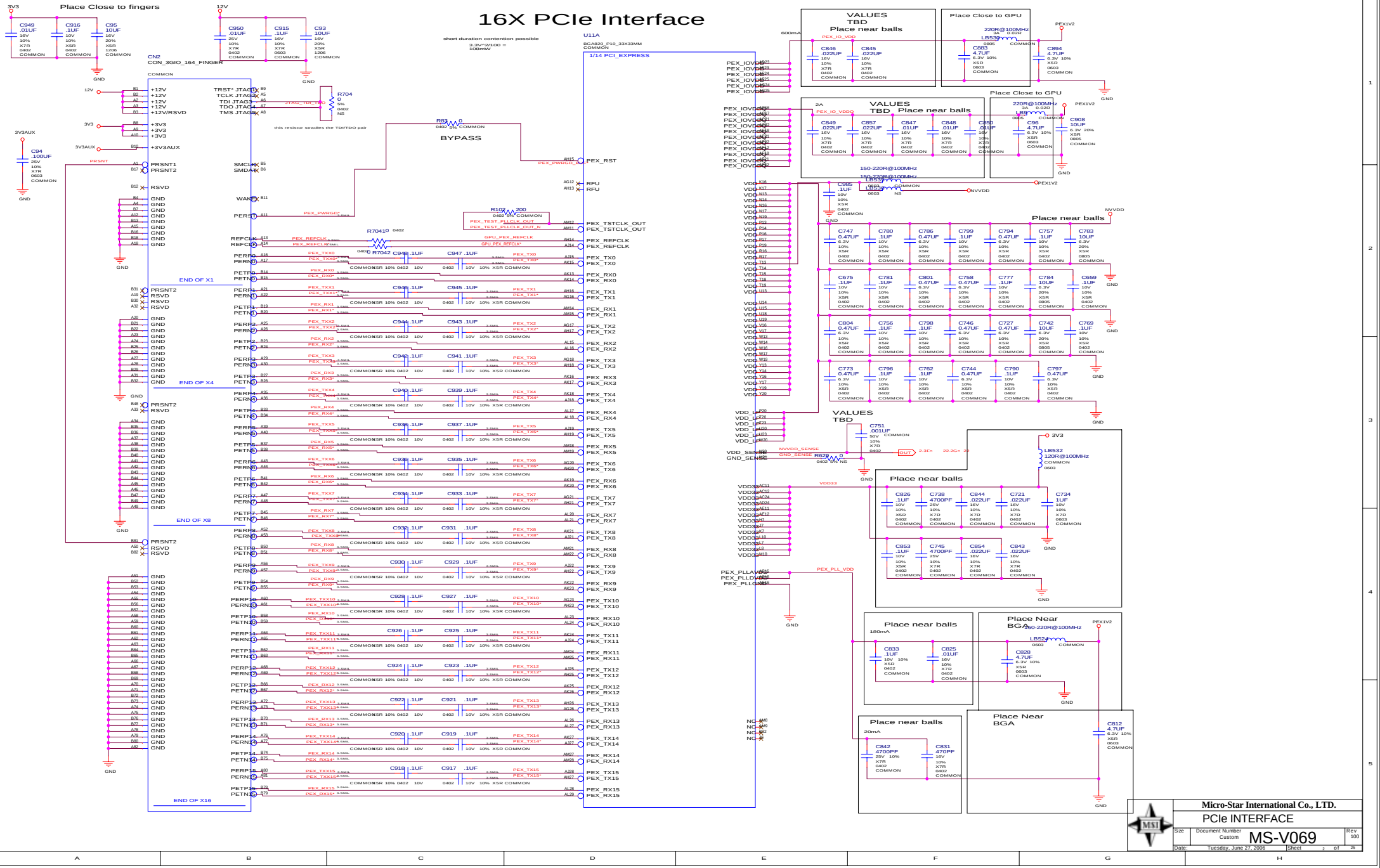
OA

Page24 Add EXTERNAL HDMI LINK SII1930
Page25 Add Micro Controller & Audio DAC
Page 12 Remove DACC RGB and Sync signal
Page 17 Remove J5 DVI connector Link to HDMI
Page 18 Modify SPDIF IN circuit base on P364
Page19 Enable GPIO 1,7,10,12
Add Page21 Liner power 1.8V

100

1.Modify A3V3 circuit all 3V3 use PEX3V3 except 7115H A3V3
2.Change Y502 and J5511HDMI TYPE A Conn to SMD Type
3.Remove Extend 12V,MOS Heatsink and 4 pin Video Conn

16X PCIe Interface



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PCIe INTERFACE
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U11B

ALL FBVDD PINS ARE NC ON NV43 DESKTOP G3 PACKAGE

BGA820_P10_33X33MM COMMON

2/14 FBA

PLACE BELOW GPU

PLACE MIDWAY BETWEEN GPU AND MEMORY

PLACE NEAR GPU

PLACE close to GPU

PLACE close to balls

TP NOW

FBx_PLLVDD NOT REQUIRED FOR G73 -- UNSTUFF

CKE Stuff options for DDR3 configation for on-die terminations at the memory
IMPORTANT FOR POWER ON INITIALIZATION OF DDR3 MEMS

DDR3: DETERMINES THE ODT VALUE FOR ADDR AND CONTROL PINS
CKE = 0 --> ODT = ZQ/2
CKE = 1 --> ODT = ZQ

VREF = FBVDDQ * Rbot/(Rtop + Rbot)

VREF = 0.70 * FBVDDQ (DDR3: 1.26V = 1.8V * 2.7K/(1.15K + 2.7K))

FBA_AVDD is TBD. This may not be hooked up on the Package.

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FBA INTERFACE	
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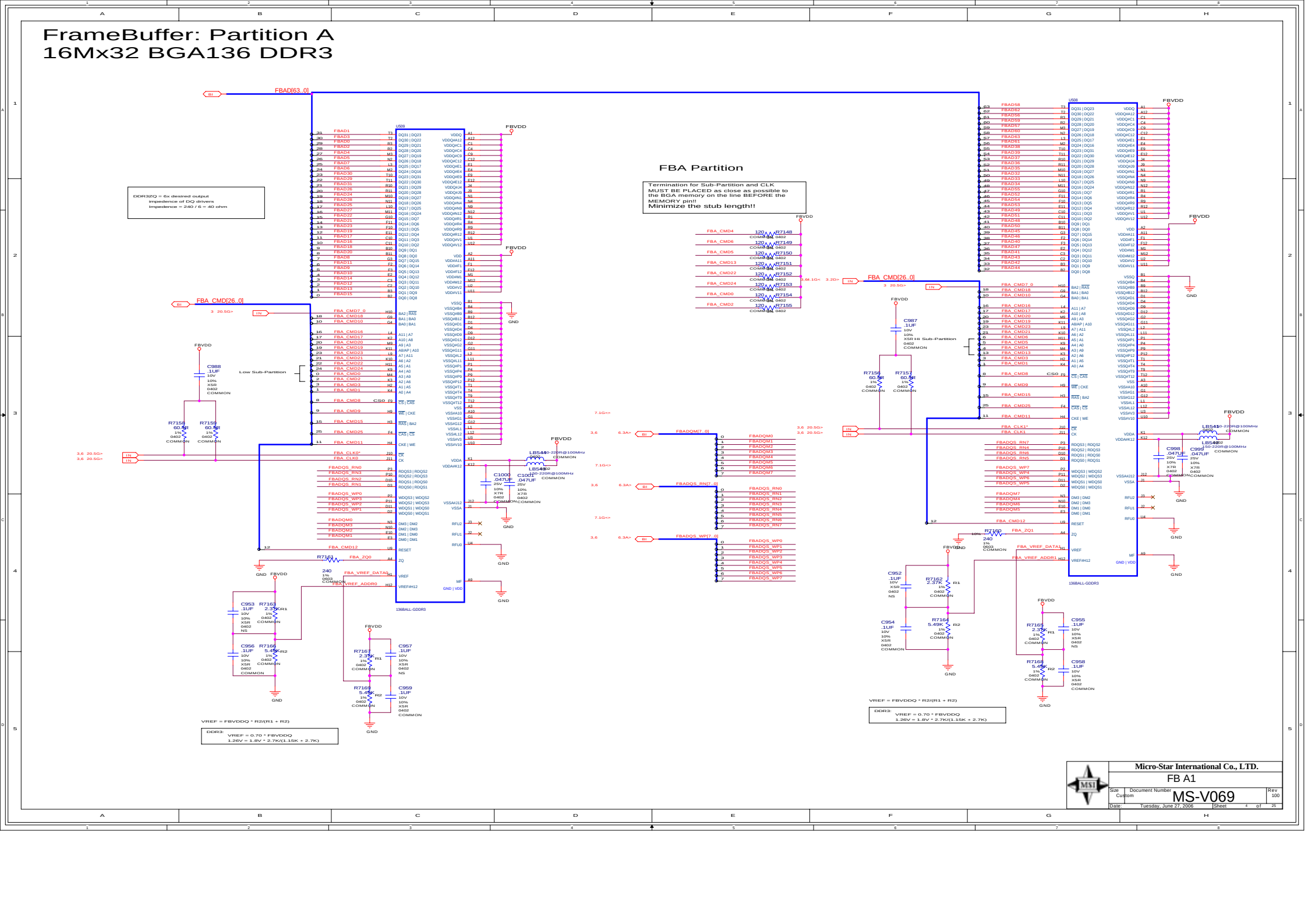
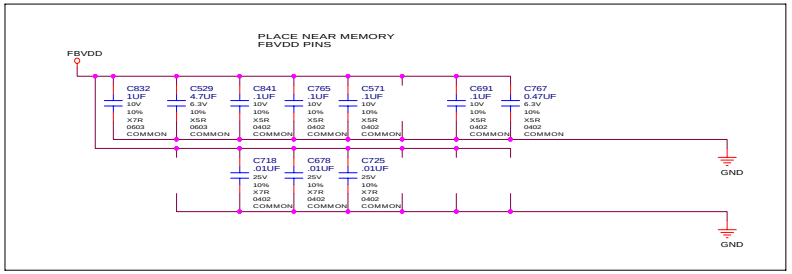
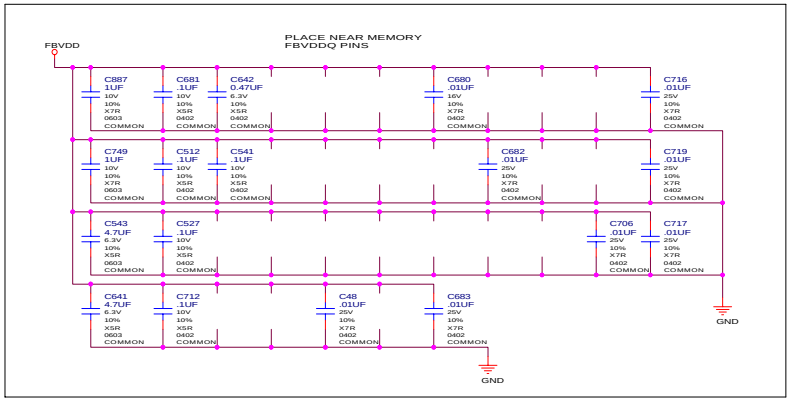
FrameBuffer: Partition A
16Mx32 BGA136 DDR3



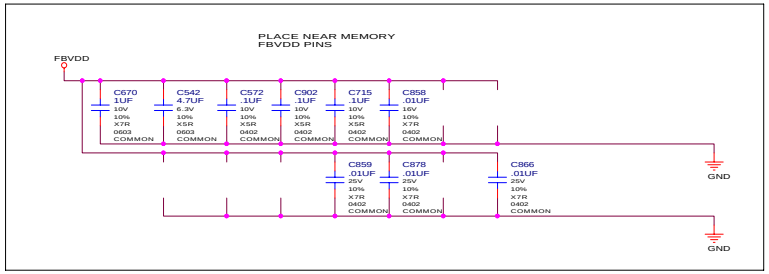
FRAME BUFFER: PARTITION A DECOUPLING

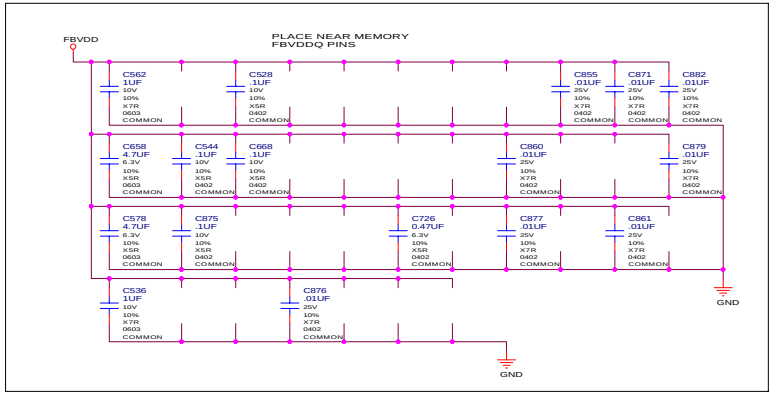
Decoupling for FBA 0..31





Decoupling for FBA 32..63





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FBA DECOUPLING	
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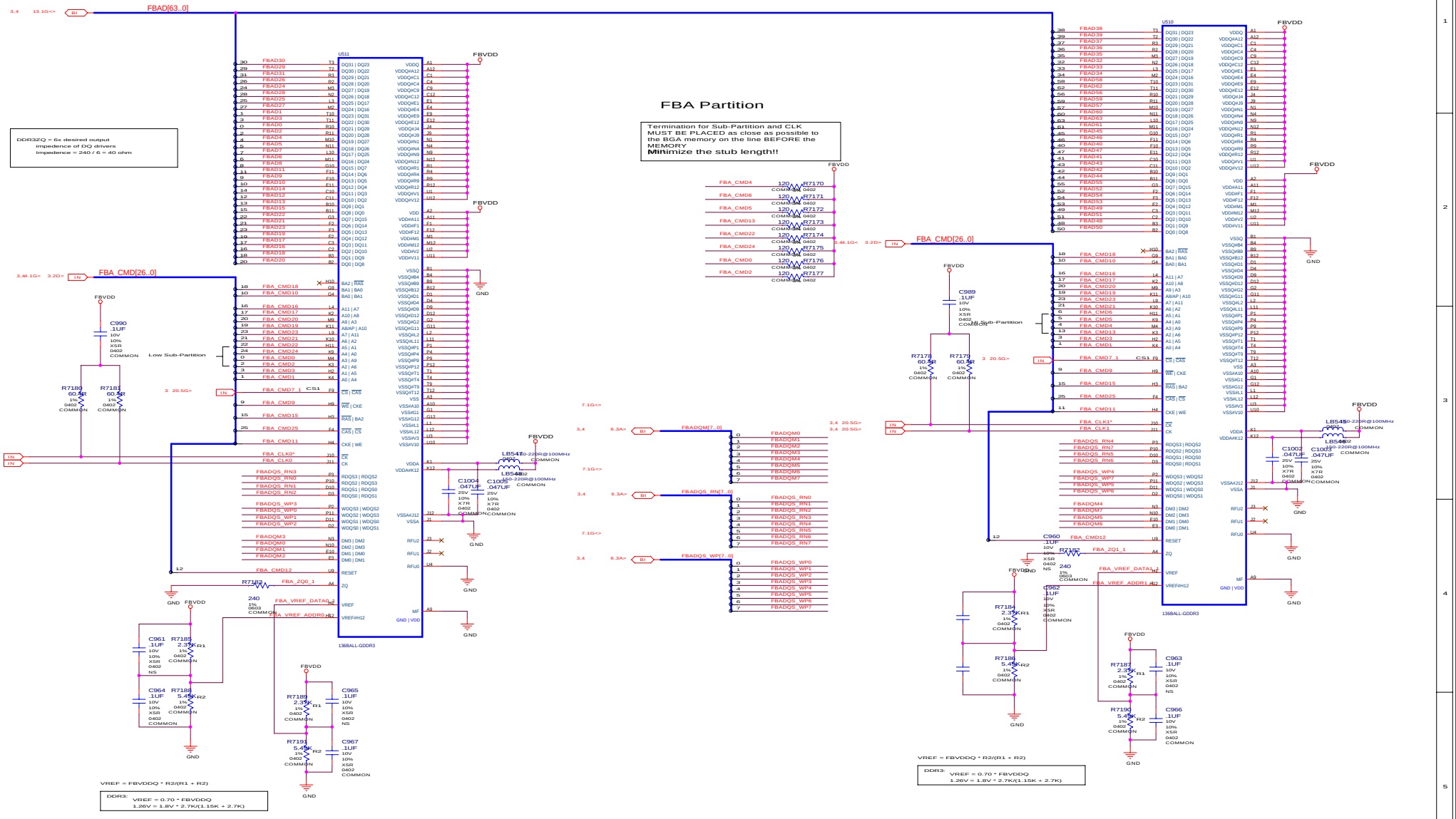
FrameBuffer: Partition A
16Mx32 BGA136 DDR3



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FB A2	
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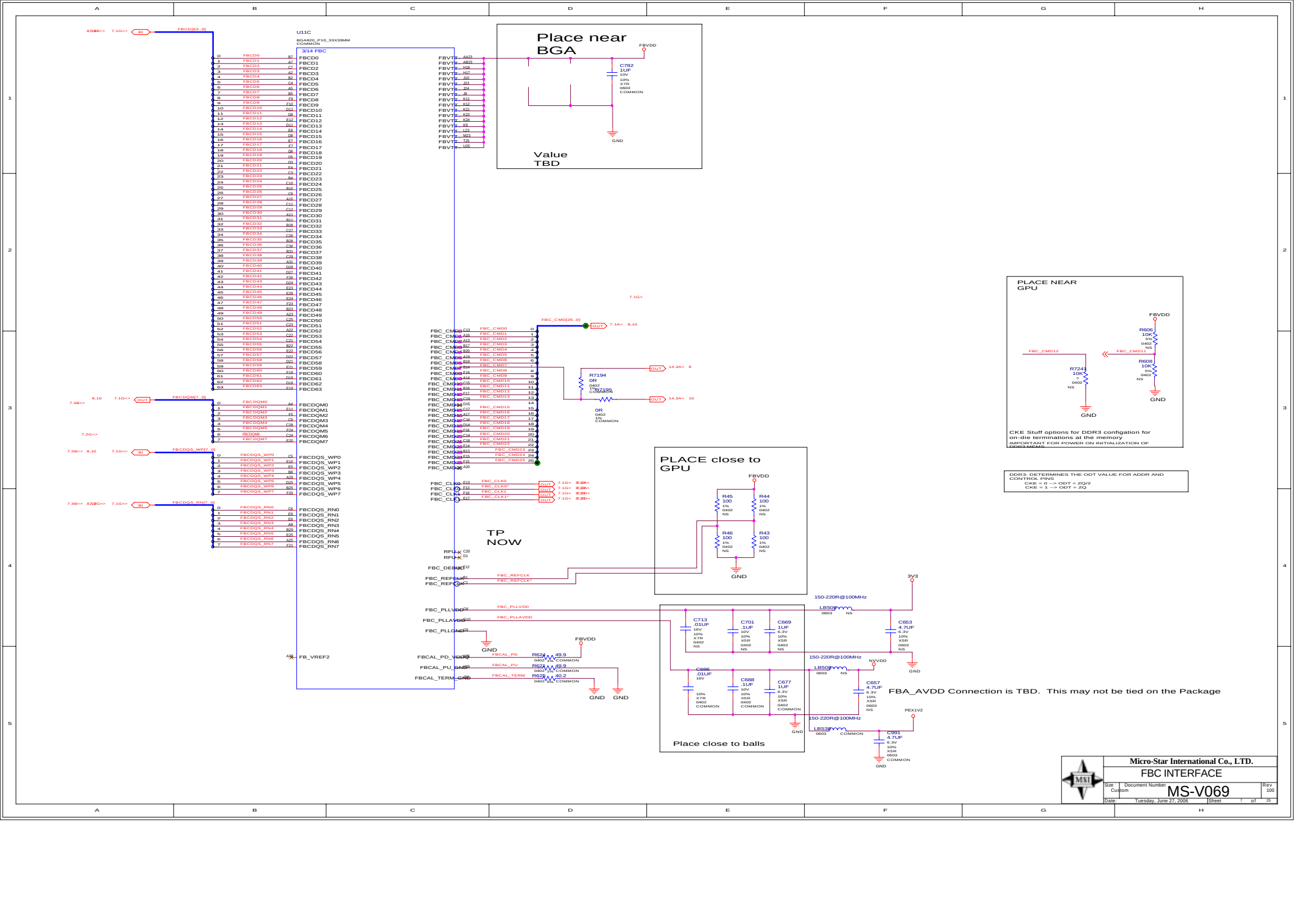
U11C
BGA820_P10_33X33MM
COMMON
3/14 FBC
Place near BGA
FBVDD
C782
1UF
10V
10%
X7R
0603
COMMON
GND
Value
TBD
FBCD[63..0]
FBCDQM[7..0]
FBCDQS_WP[7..0]
FBCDQS_RN[7..0]
FBCD_CMD[26..0]
FB_VREF2
R7194
0R
0402
1%
COMMON
R7195
0R
0402
1%
COMMON
PLACE NEAR GPU
R606
10K
5%
0402
NS
R608
10K
5%
0402
NS
R7243
10K
5%
0402
NS
CKE Stuff options for DDR3 configation for on-die terminations at the memory
IMPORTANT FOR POWER ON INITIALIZATION OF DDR3 MEMS
DDR3: DETERMINES THE ODT VALUE FOR ADDR AND CONTROL PINS
CKE = 0 --> ODT = ZQ/2
CKE = 1 --> ODT = ZQ
PLACE close to GPU
R45
100
1%
0402
NS
R44
100
1%
0402
NS
R46
100
1%
0402
NS
R43
100
1%
0402
NS
TP NOW
RFU
DEBUG
REFCLK
PLLVDD
PLLAVDD
PLLGND
FBCAL_PD_VDD
FBCAL_PU_GND
FBCAL_TERM_GND
R624
49.9
1%
COMMON
R625
40.2
1%
COMMON
3V3
150-220R@100MHz
LB508
LB509
LB538
C713
.01UF
16V
10%
X7R
0402
NS
C701
1UF
10V
10%
X5R
0402
NS
C669
1UF
6.3V
10%
X5R
0402
NS
C653
4.7UF
6.3V
10%
X5R
0603
NS
C686
.01UF
16V
10%
X7R
0402
COMMON
C688
.1UF
10V
10%
X5R
0402
COMMON
C677
1UF
6.3V
10%
X5R
0402
COMMON
C657
4.7UF
6.3V
10%
X5R
0603
NS
C991
4.7UF
6.3V
10%
X5R
0603
COMMON
NVVDD
PEX1V2
FBA_AVDD Connection is TBD. This may not be tied on the Package
Place close to balls
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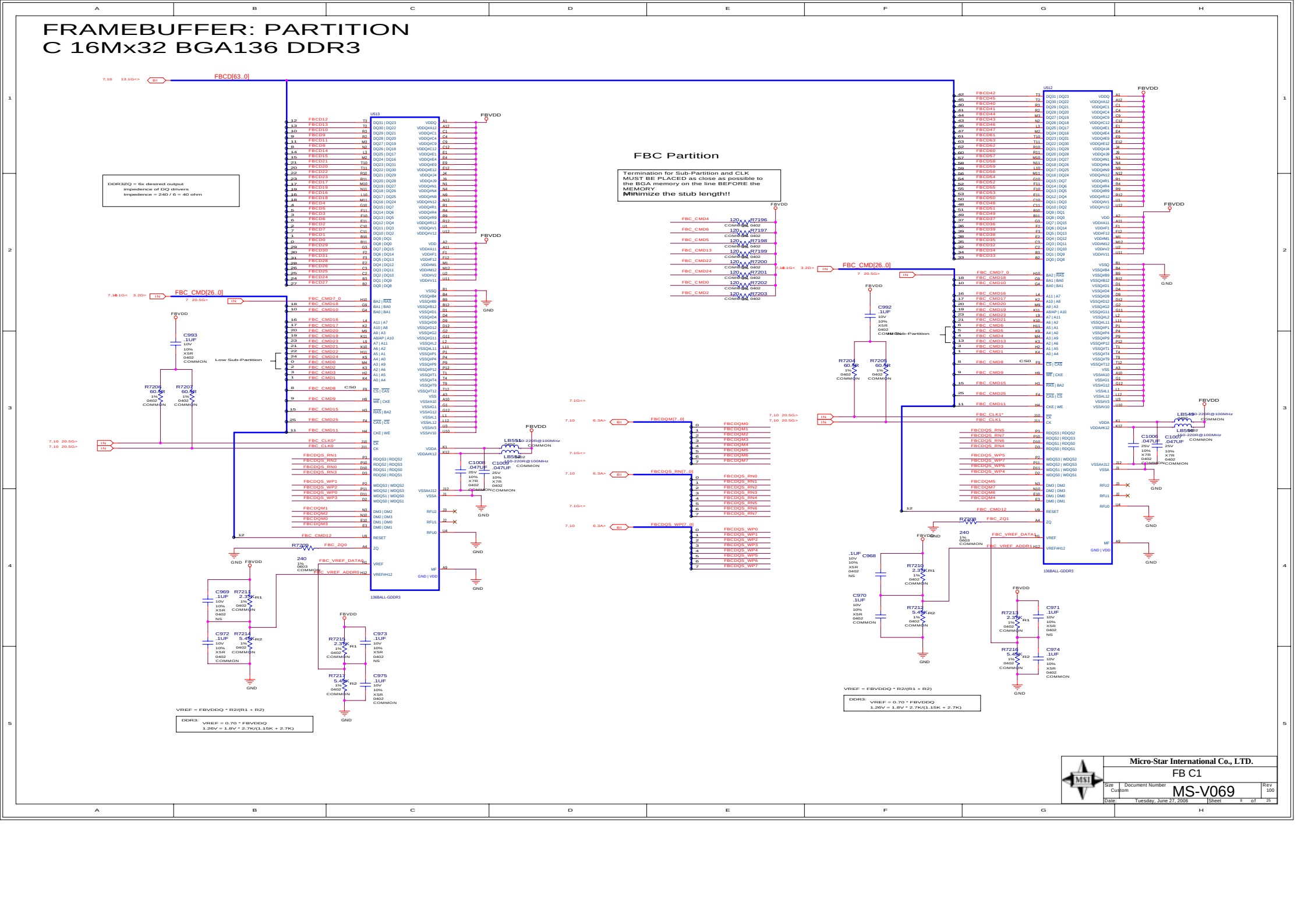
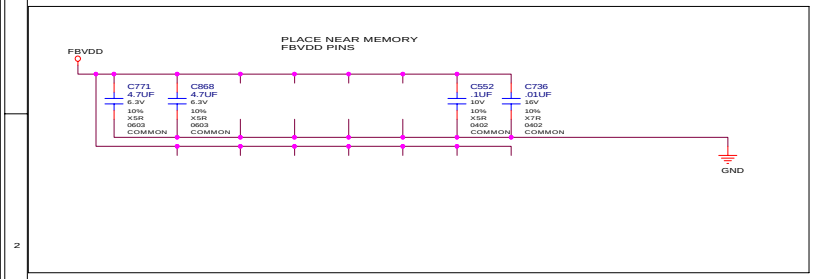
FRAMEBUFFER: PARTITION
C 16Mx32 BGA136 DDR3

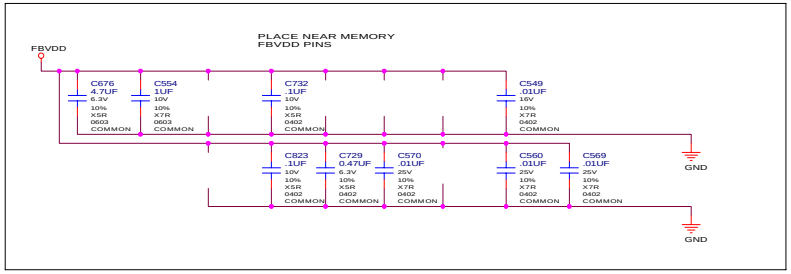


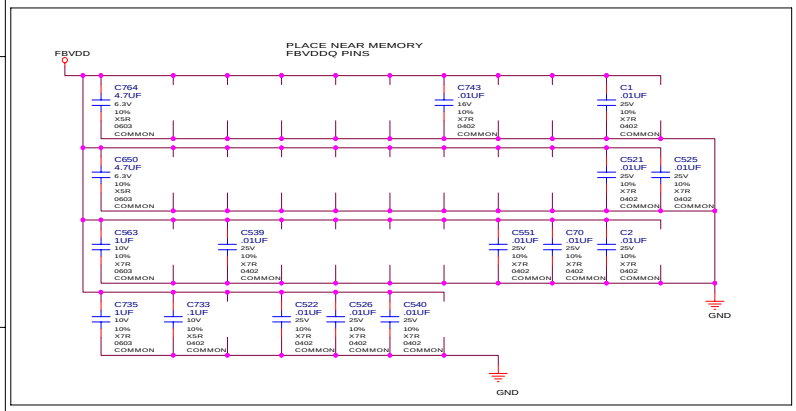
FRAMEBUFFER: PARTITION C DECOUPLING

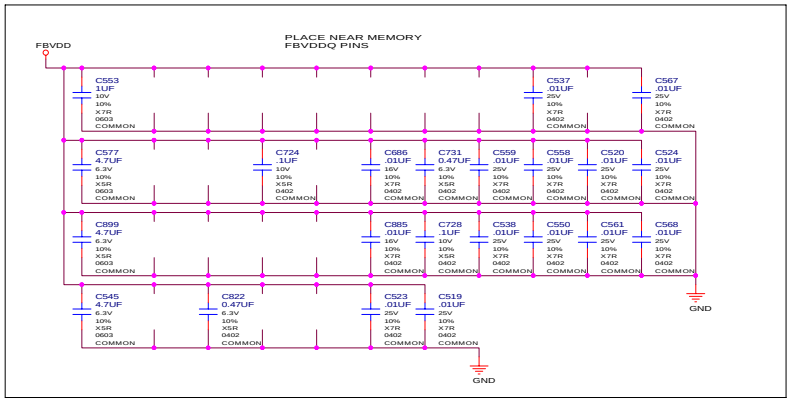
Decoupling for FBC 0..31

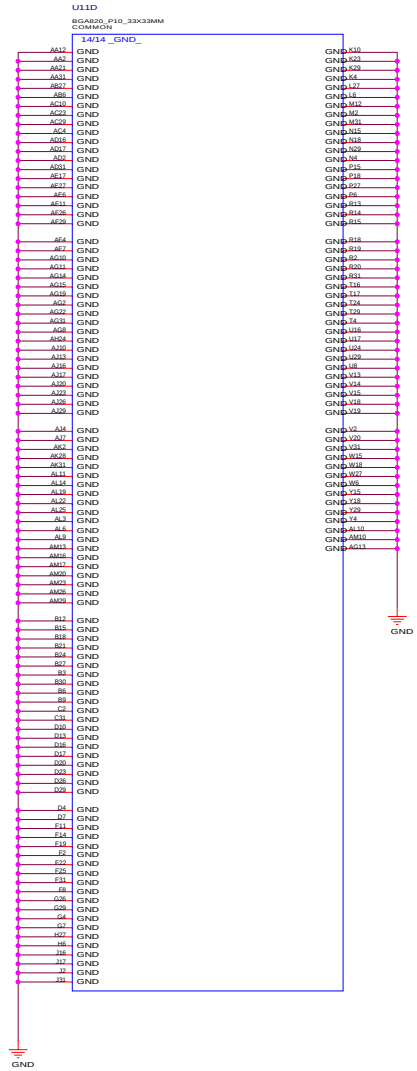


Decoupling for FBC 32..63









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FBC DECOUPLING	
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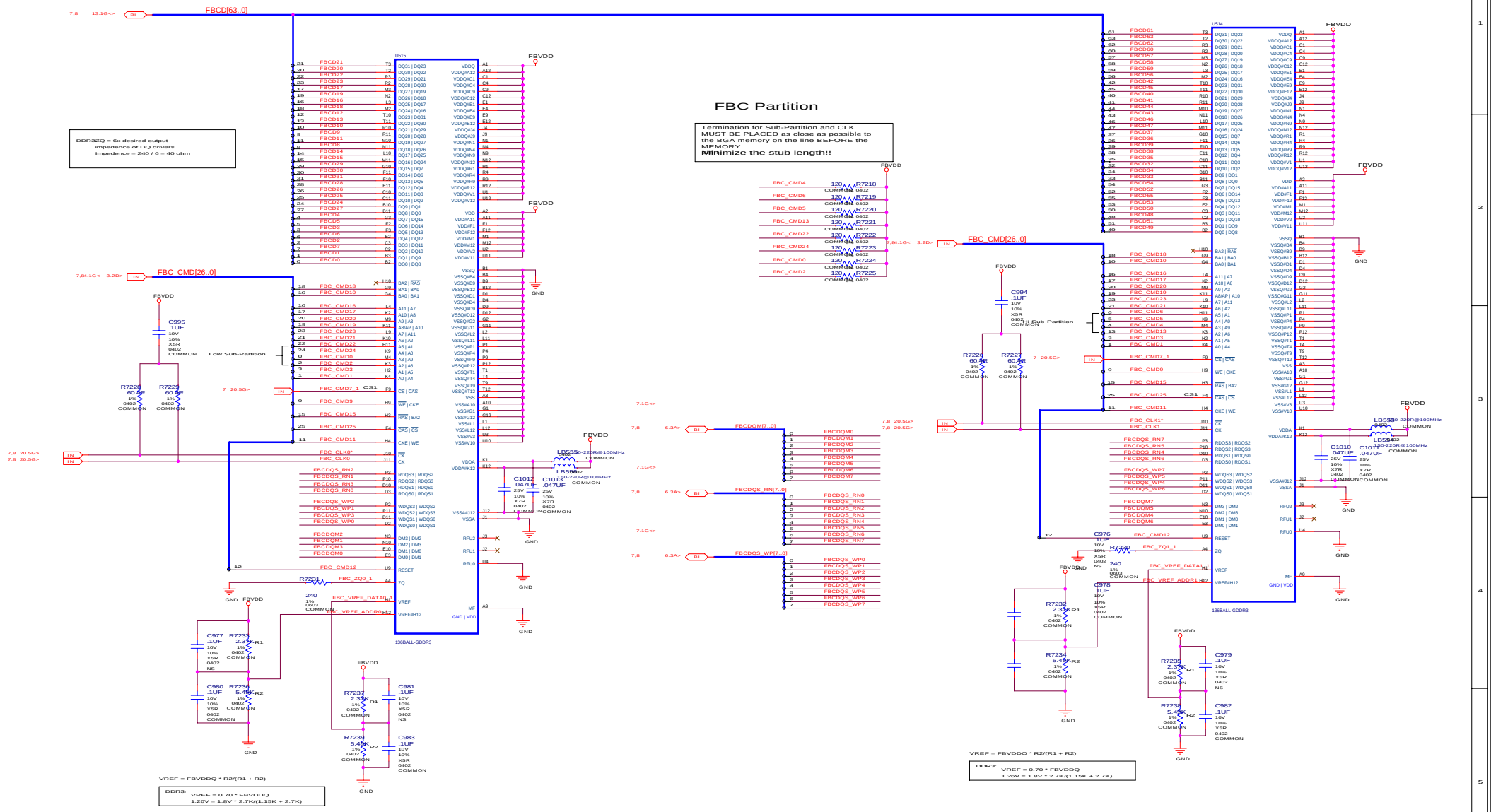
FRAMEBUFFER: PARTITION C 8Mx32 BGA136 DDR3



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FB C2	
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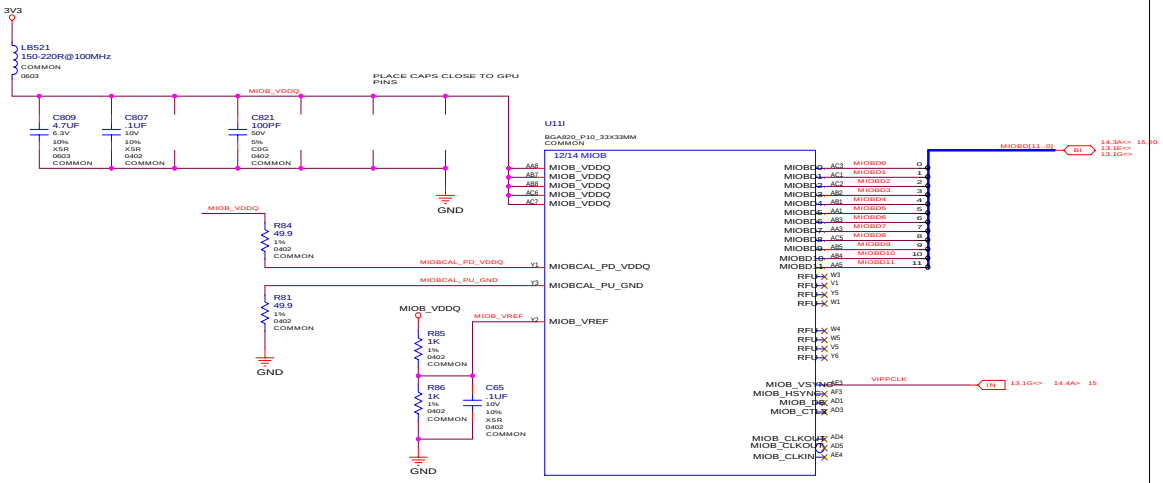
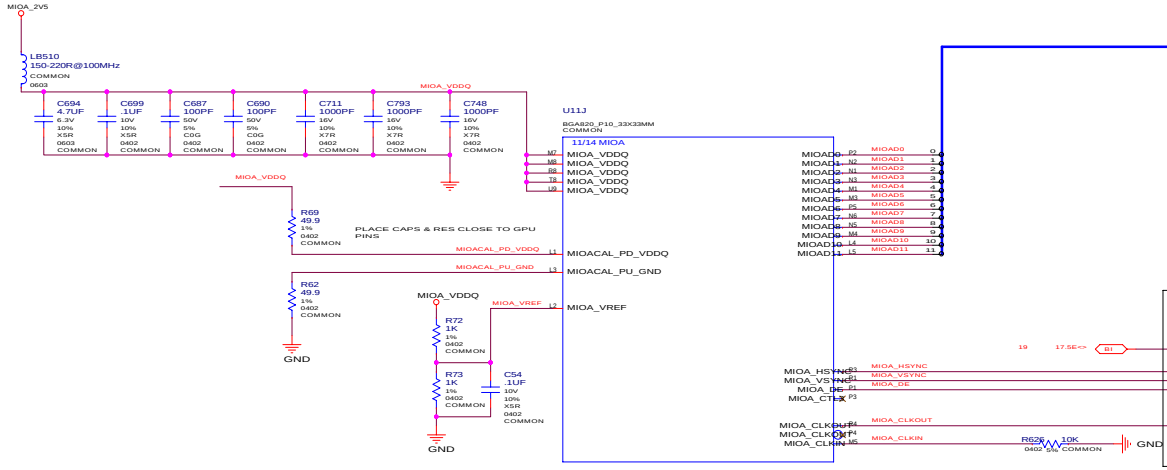
G3 VIP/MIOB



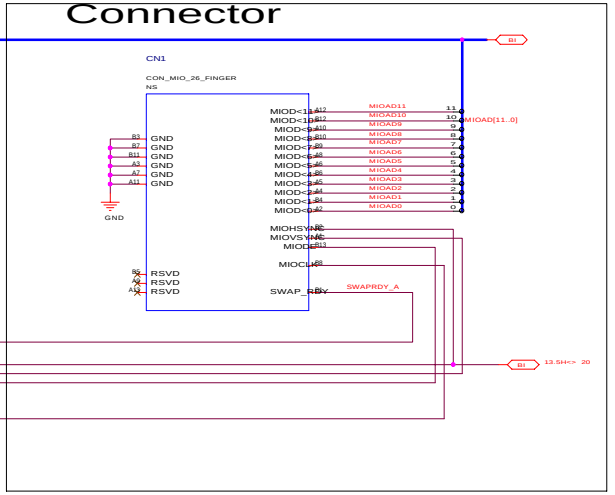
NETNAME | MIN_LINE_WIDTH | SPACING RULE

MIOBD[7..0] | 3.5MIL | 15MIL

G3 MIOA



Feature Connector



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MIOA/MIOB			
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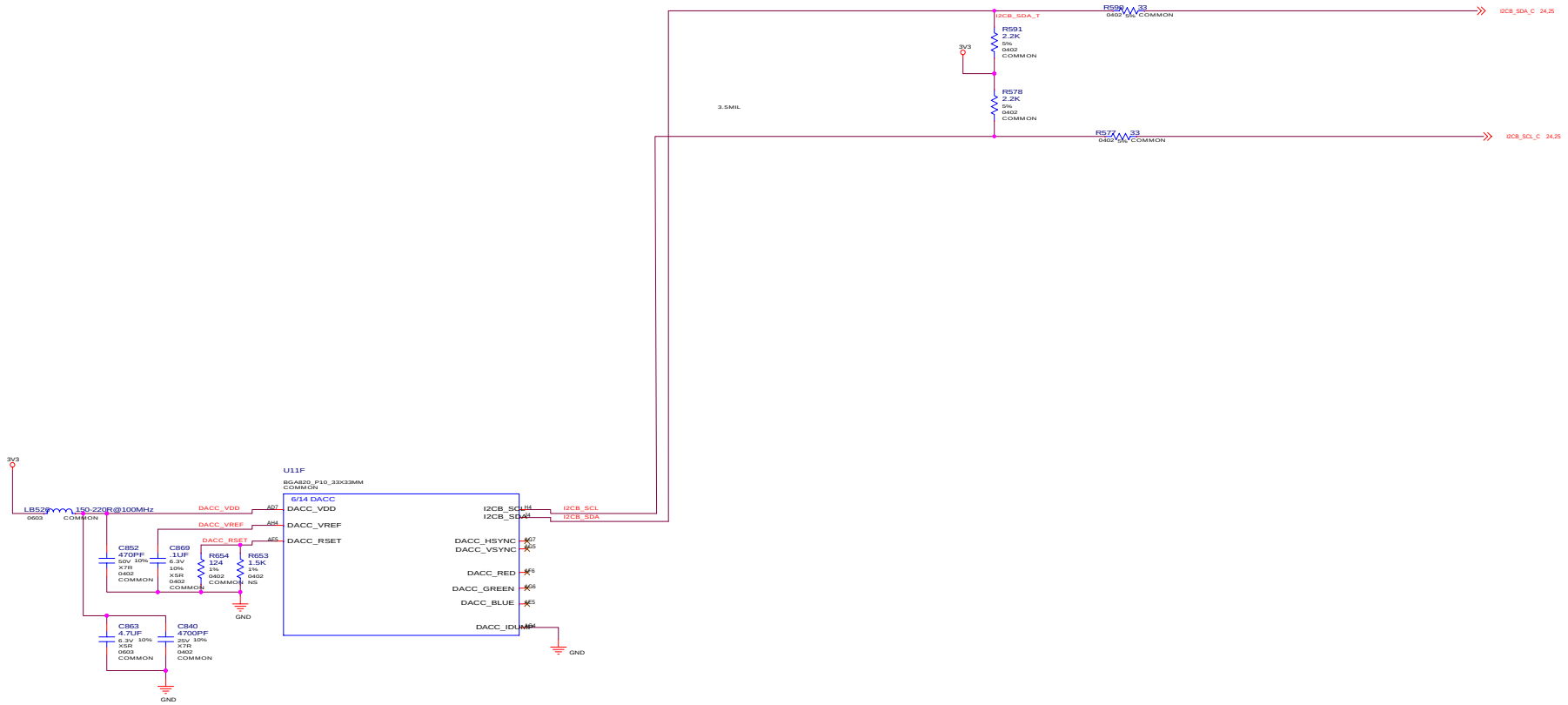
Secondary Display (DACC), Slim DB15

DACC RGB-FILTER



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DACC		
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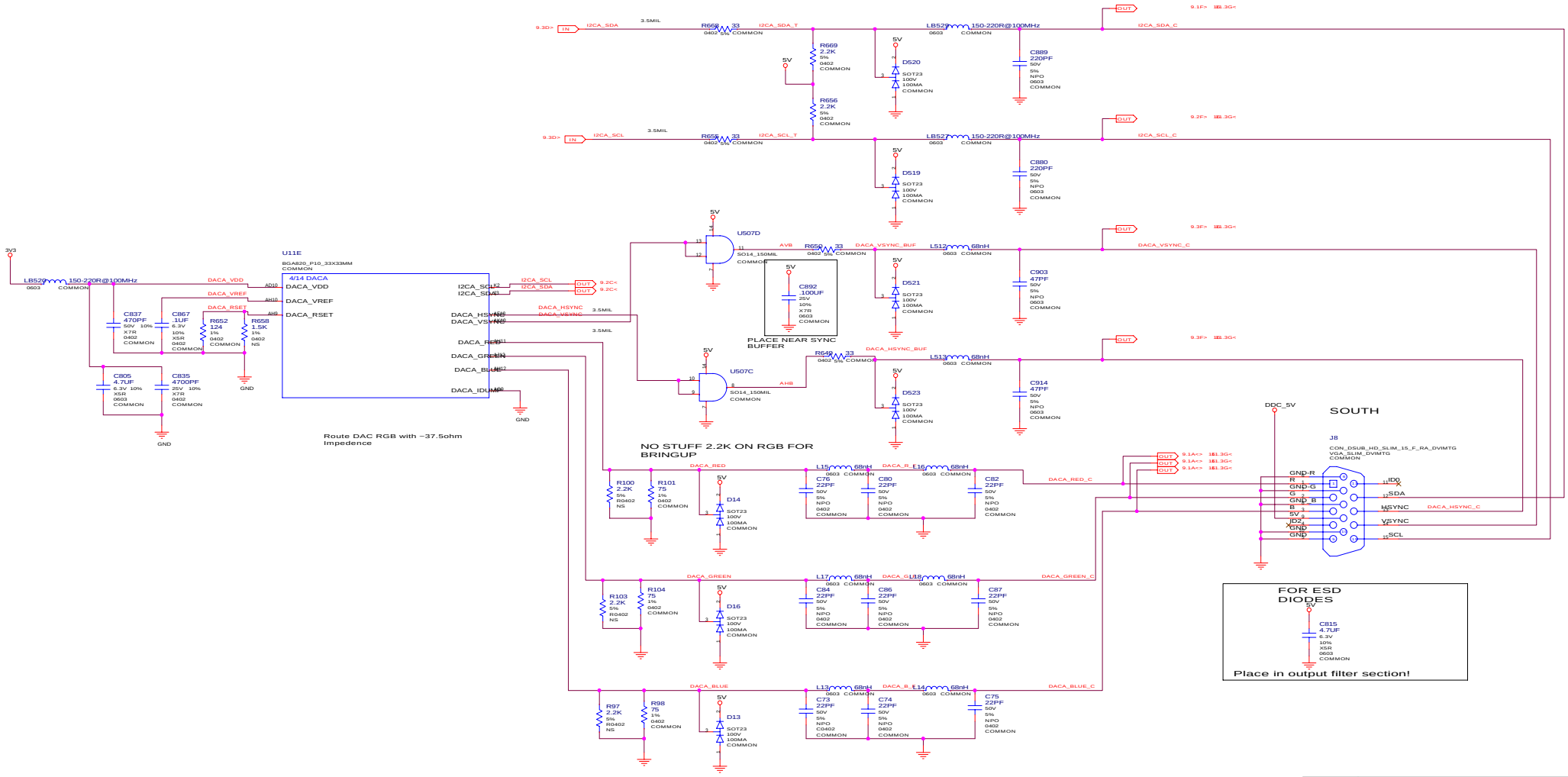
Primary Display (DACA), Slim DB15

DACA
RGB-FILTER



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DACA	
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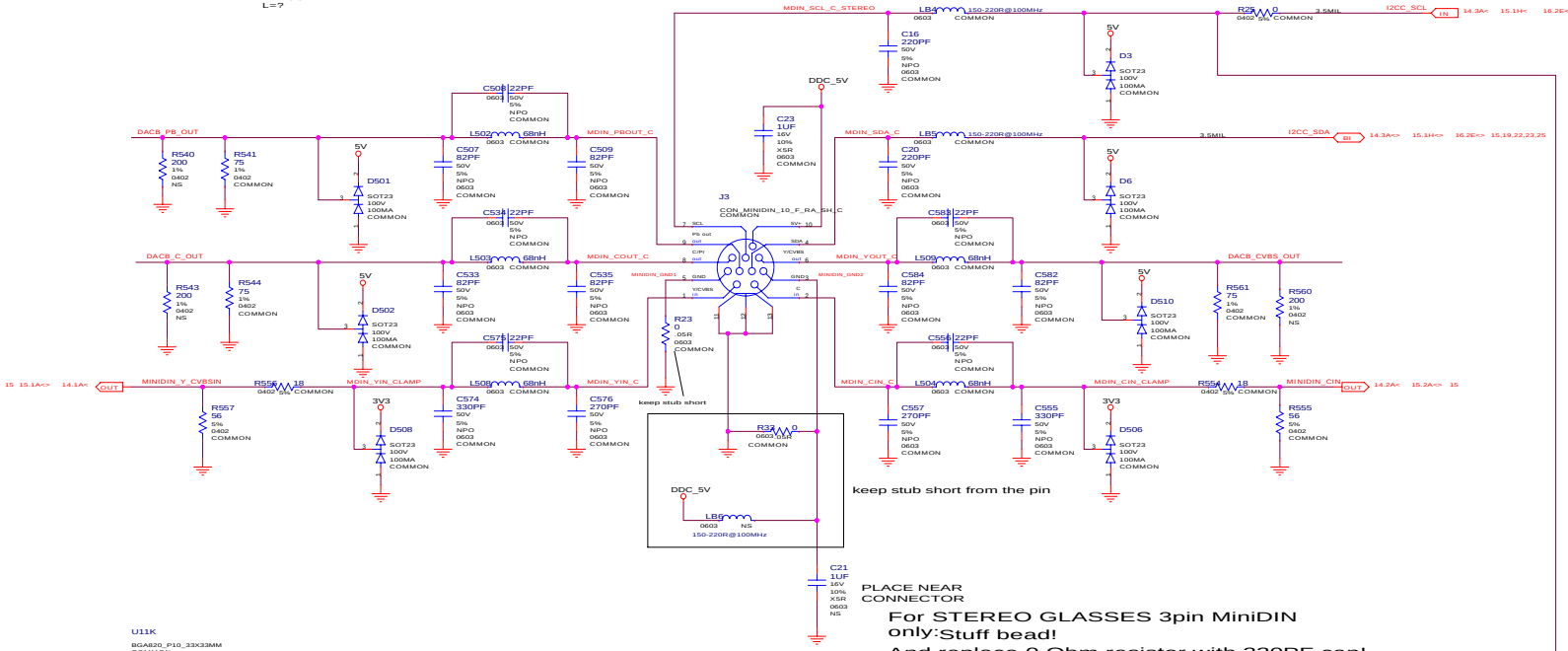
DACB .. MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES

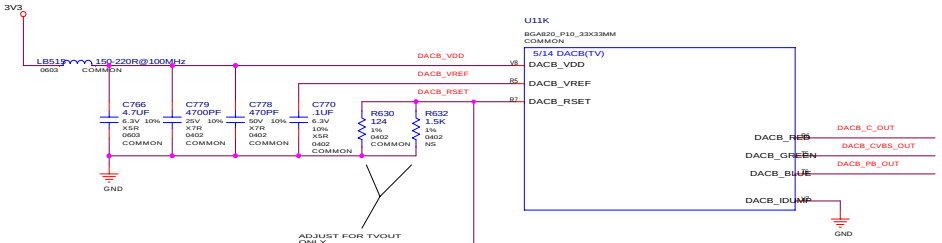
FILTER NOTES:

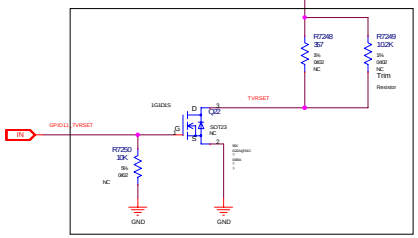
SD: USE L=1.8UH

HD: USE L=?



For STEREO GLASSES 3pin MiniDIN only:Stuff bead!
And replace 0 Ohm resistor with 220PF cap!

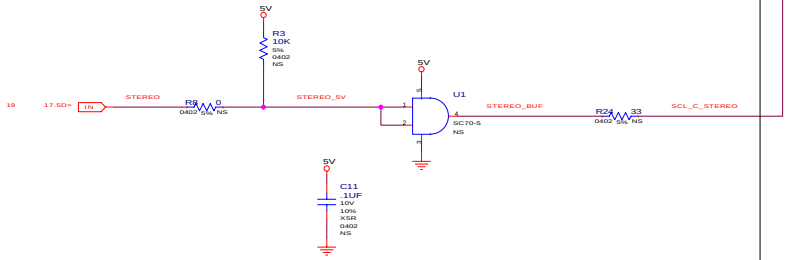




NC for G73

STEREO GLASSES BUFFER

Place close to MiniDIN connector!



FOR DEBUG PURPOSES ONLY .. DEFAULT IS NO STUFF

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DACB		
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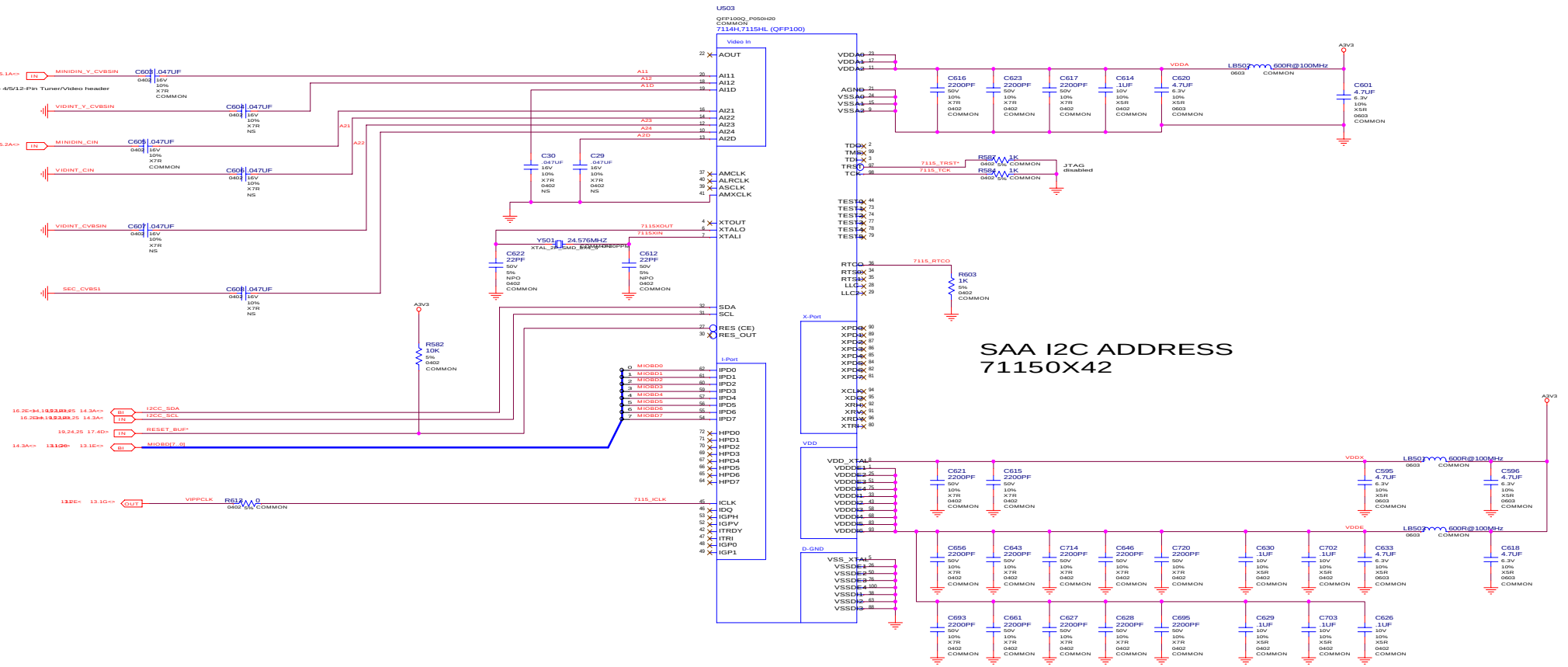
PHILIPS
VIDEO
CAPTURE



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VIDEO CAPTURE			
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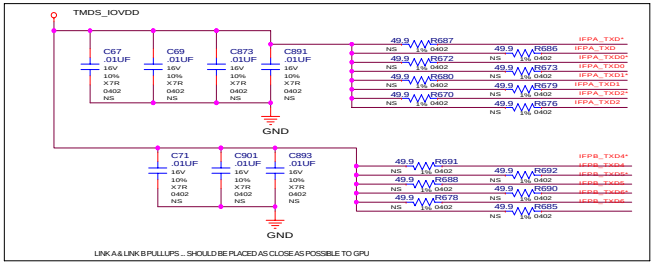
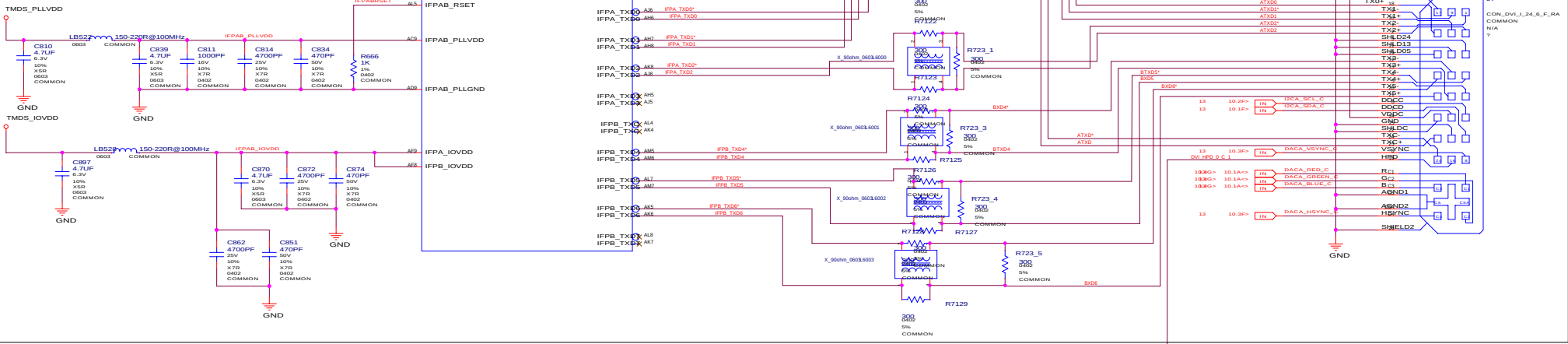
INTERNAL TMDS .. LINK A & B

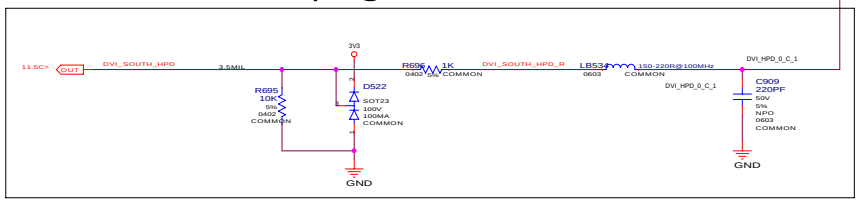
G73 - UNSTUFF PU's



NOTE: GPU HAS ON DIE PULL UPS ON TMDS LINES .. EXTERNAL PULLUPS ADDED (FOR CYA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE



Hotplug Detection



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TMDS LINK A & B		
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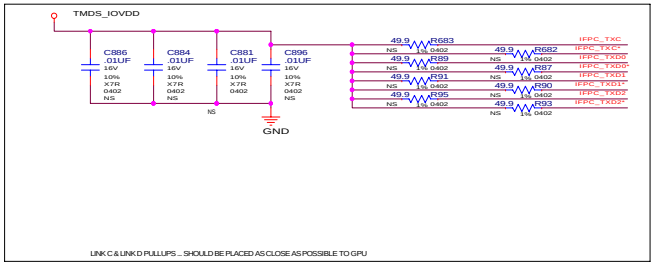
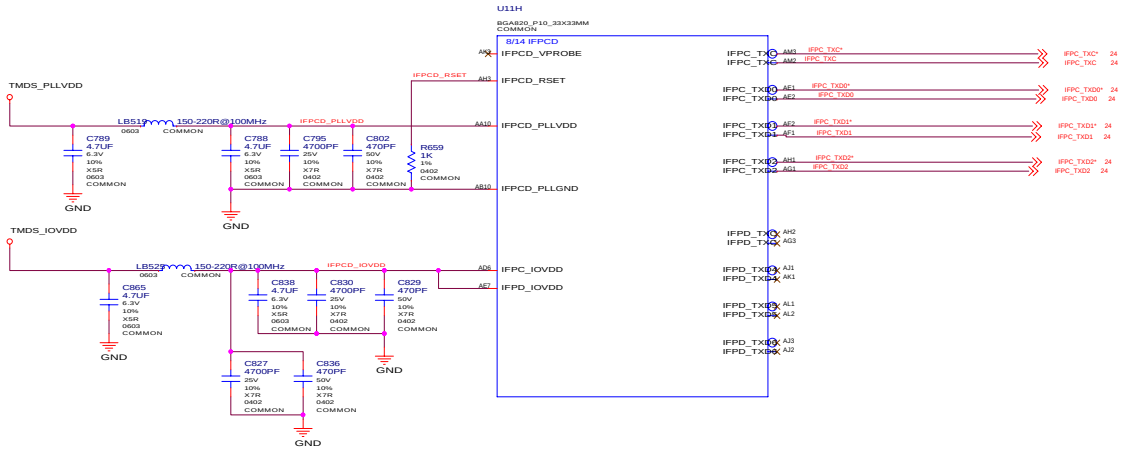
INTERNAL TMDS
.. LINK C & D





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TMDS LINK C & D	
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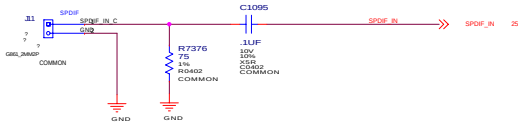
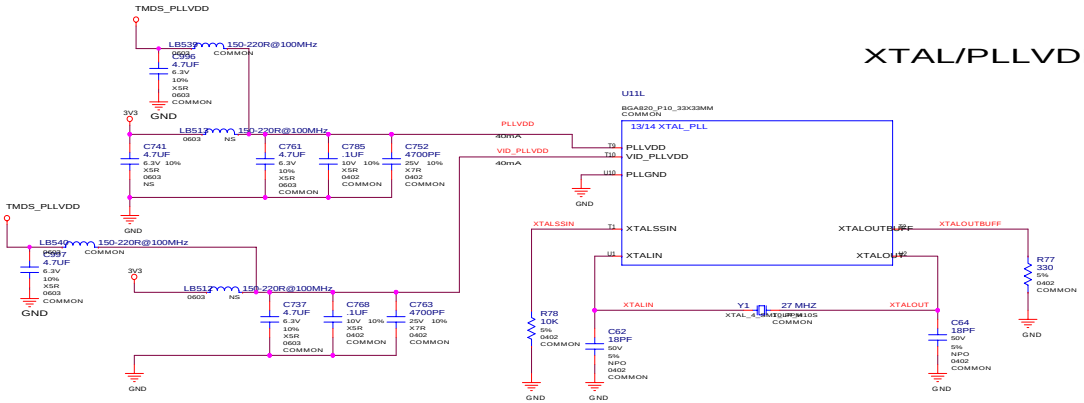
SPDIF IN



XTAL/PLLVDD



	Micro-Star International Co., LTD.	
	4-Pin Video-In/SPDIF IN	
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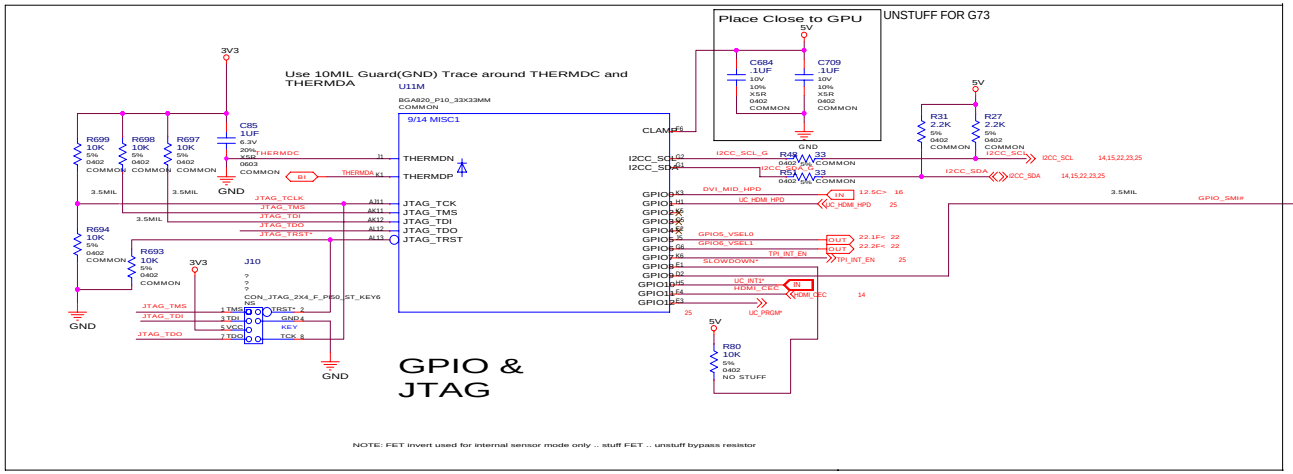
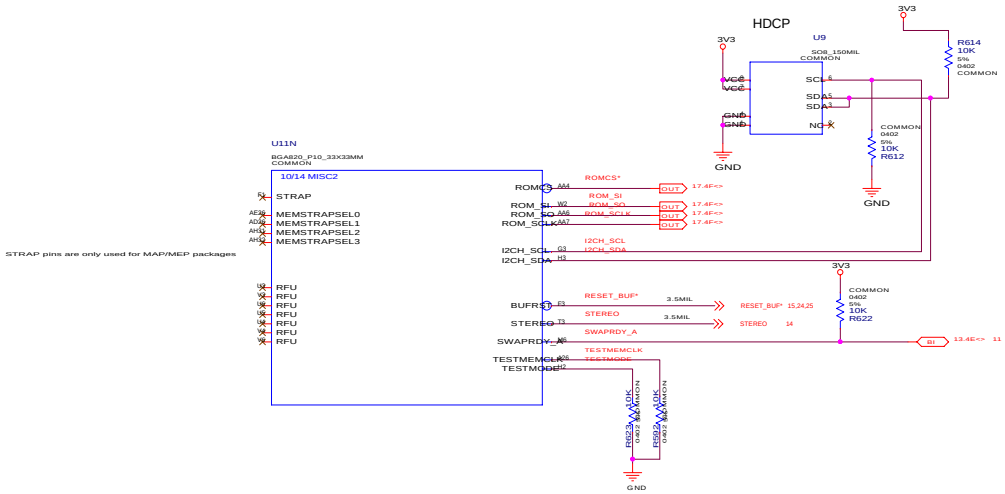
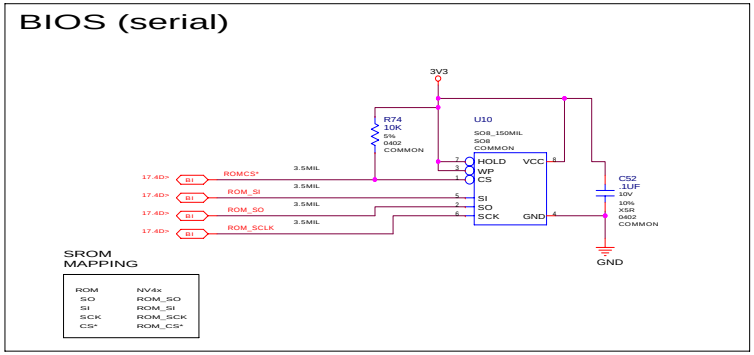


GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	HDMI hotplug
2	IN	RESERVED
3	IN	RESERVED
4	IN	TUNER IRQ
5	OUT	NVVDD VOLTAGE SELECT 0
6	OUT	NVVDD VOLTAGE SELECT 1
7	Out	TPI INTERRUPT ENABLE
8	IN	RESERVED
9	OUT	PWM FAN
10	IN	INT from Sil1930 TVRSET
11	IN	TVRSET
12	IN	uC PROGRAMMING CONTROL





Micro-Star International Co., LTD.	
GPIO/ROM/HDCP ROM	
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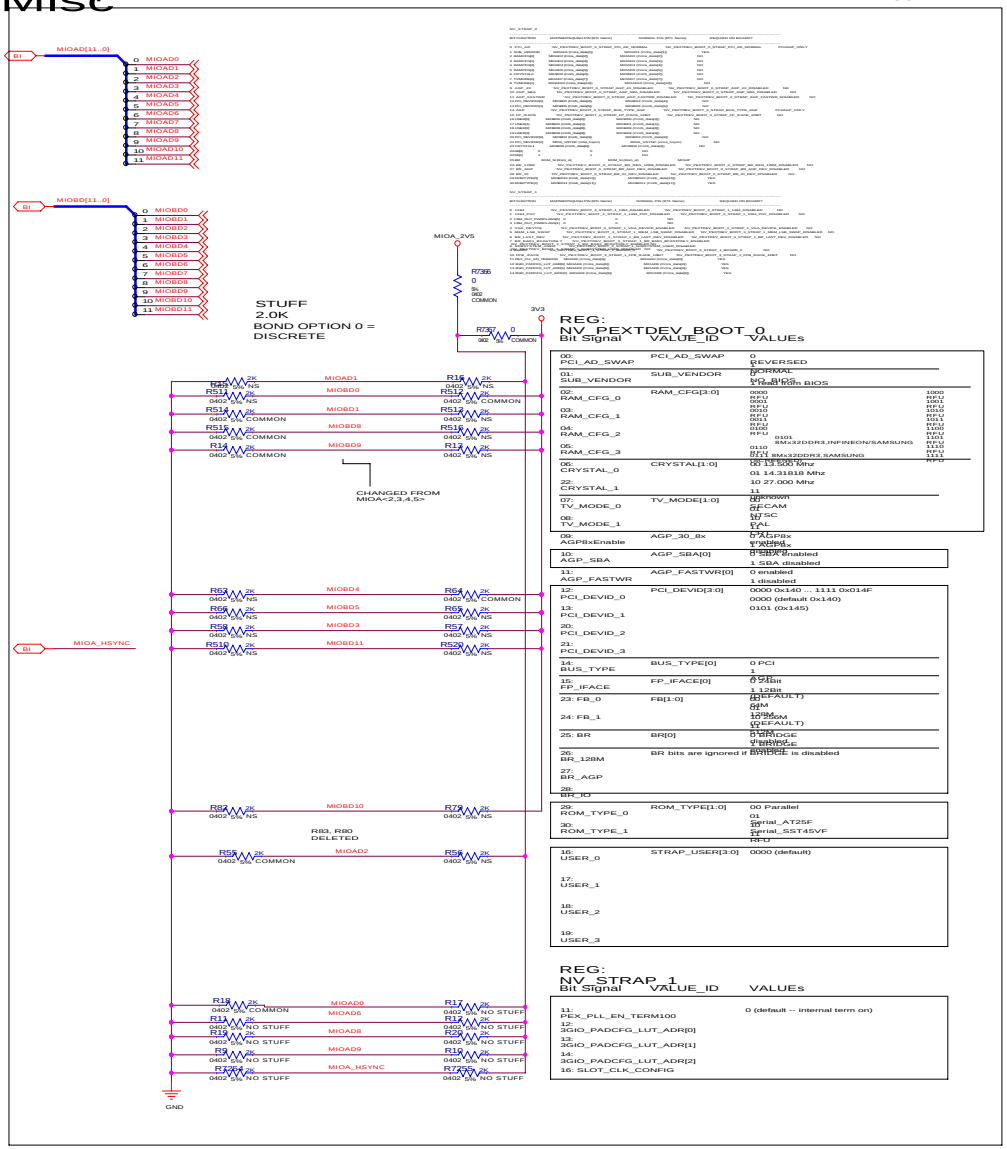
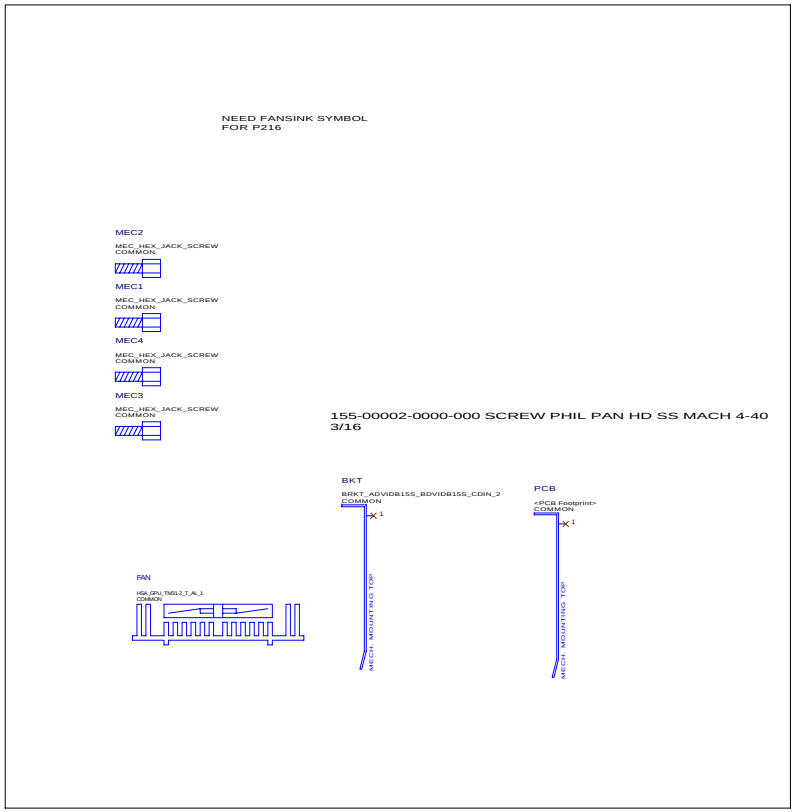
BIOS, Straps, Misc

Straps

Assembly: BIOS



Mechanical parts



Micro-Star International Co., LTD.			
Straps/Mechanical			
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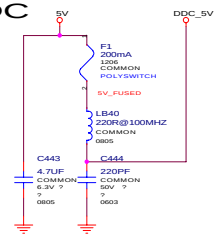
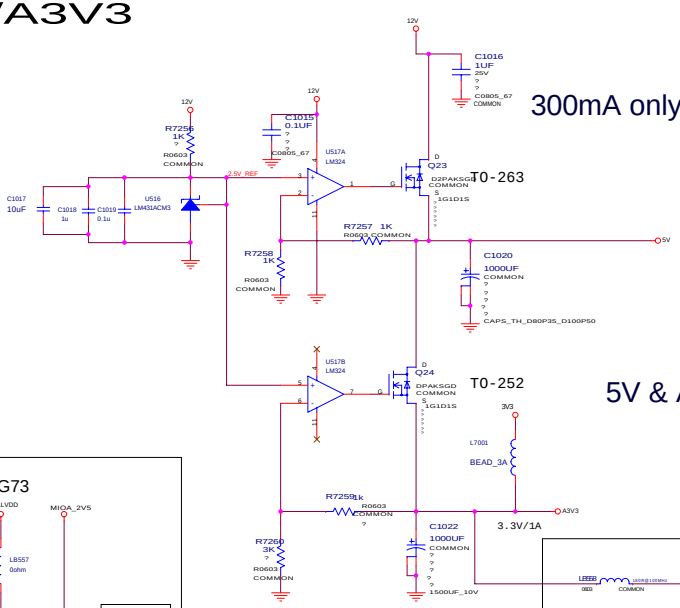
Power Supply TMDS/A3V3

DDC 5V



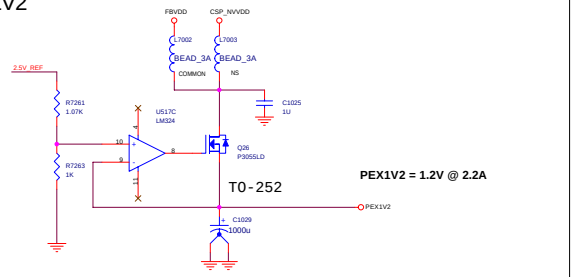
POWER_DDC5V

300mA only



5V & A3V3

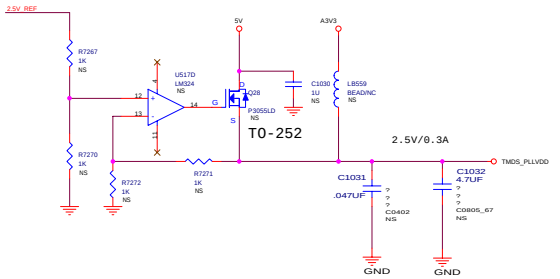
PEX1V2



PEX1V2 = 1.2V @ 2.2A

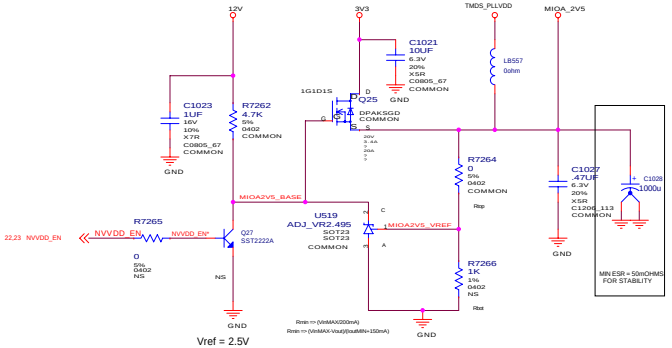
TMDS AB/CD PLL Supply

Non-use for G73



MIOA_VDDQ

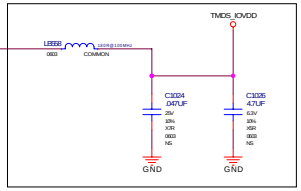
Use for G73



Vref = 2.5V

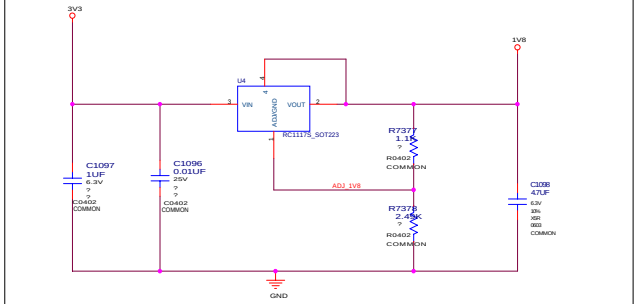
Vout = 2.495(1+Rtop/Rbot) + (Iref + Rtop)

For Vout = Vref (Rtop = 0ohm, Rbot = NO STUFF)

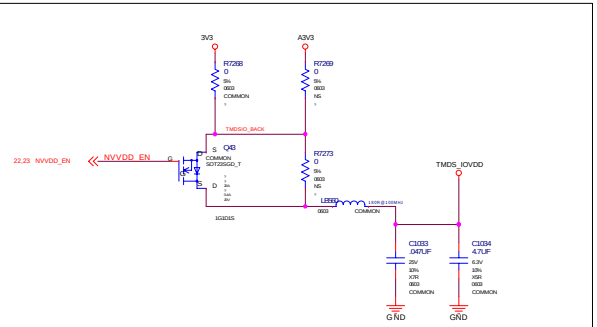


No Stuff

1.8V 320mA



TMDS IO SUPPLY WITH BACKDRIVE PROTECTION



Micro-Star International Co., LTD.			
Linear Power			
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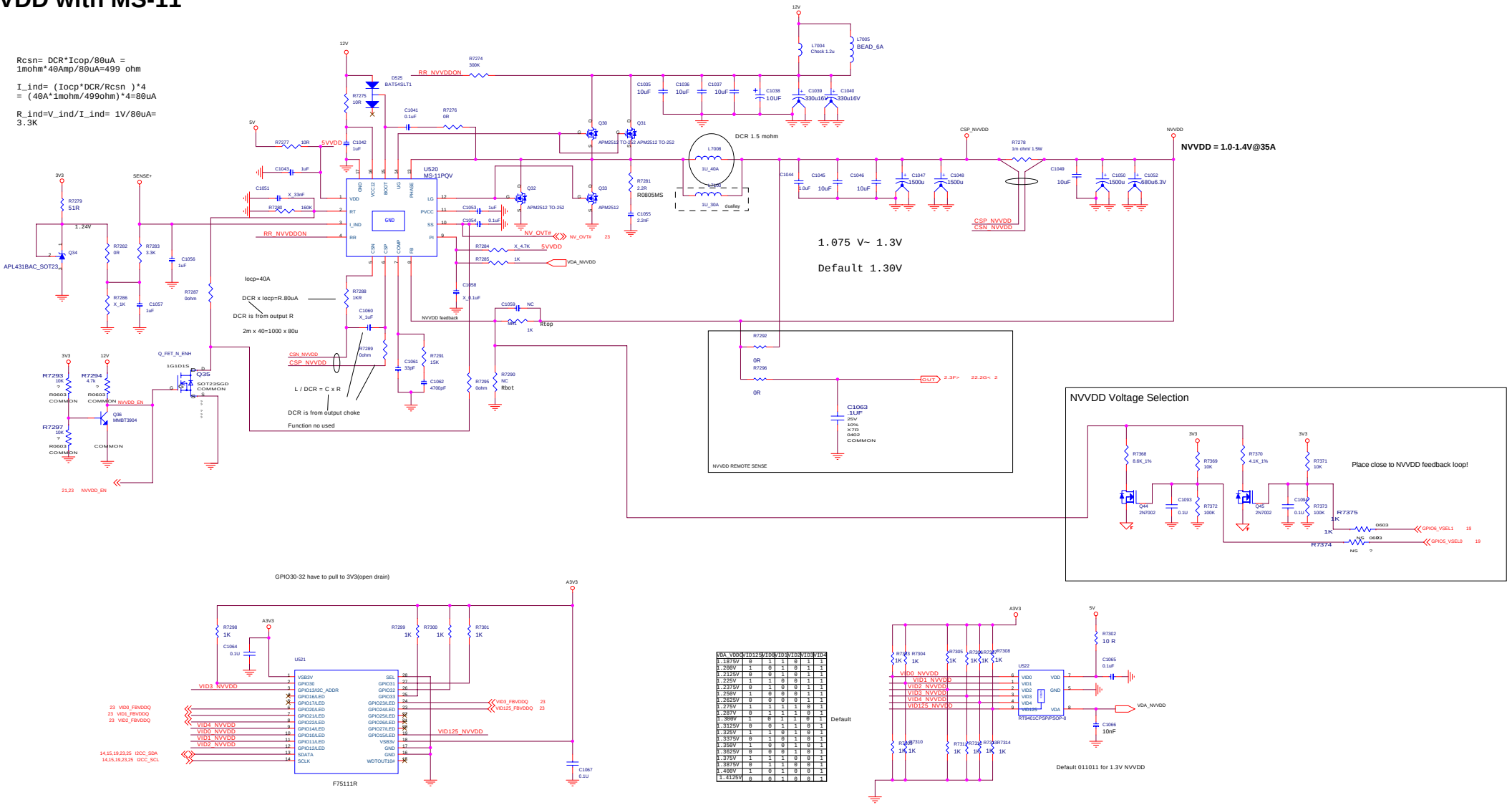
NVVDD with MS-11



VDA_VDDQ	VID125	VID4	VID3	VID2	VID1	VID0
1.1875V	0	1	1	0	1	1
1.200V	1	0	1	0	1	1
1.2125V	0	0	1	0	1	1
1.225V	1	1	0	0	1	1
1.2375V	0	1	0	0	1	1
1.250V	1	0	0	0	1	1
1.2625V	0	0	0	0	1	1
1.275V	1	1	1	1	0	1
1.287V	0	1	1	1	0	1
1.300V	1	0	1	1	0	1
1.3125V	0	0	1	1	0	1
1.325V	1	1	0	1	0	1
1.3375V	0	1	0	1	0	1
1.350V	1	0	0	1	0	1
1.3625V	0	0	0	1	0	1
1.375V	1	1	1	0	0	1
1.3875V	0	1	1	0	0	1
1.400V	1	0	1	0	0	1
1.4125V	0	0	1	0	0	1

Default

NVVDD_ GPIO:10~15

FBVDDQ_ GPIO:20~24

DACA_ RESET---GPIO:25~28

DACC_ RESET---GPIO:30~32

NVVDD 1.33V default 010101

Micro-Star International Co., LTD.			
NVVDD with MS-11			
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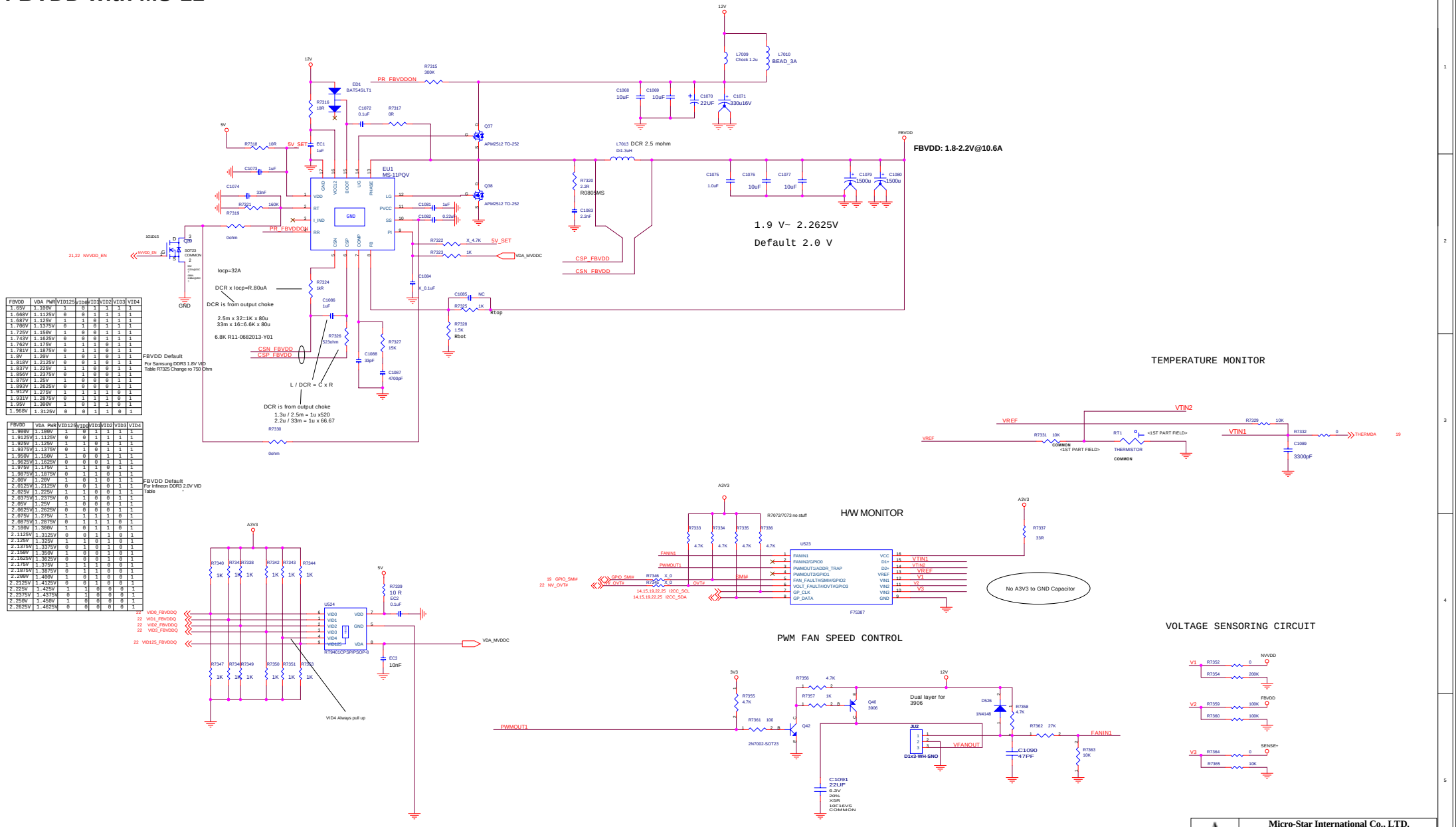
FBVDD with MS-11



FBVDD	VDA_PWR	VID125	VID0	VID1	VID2	VID3	VID4
1.65V	1.100V	1	0	1	1	1	1
1.668V	1.1125V	0	0	1	1	1	1
1.687V	1.125V	1	1	0	1	1	1
1.706V	1.1375V	0	1	0	1	1	1
1.725V	1.150V	1	0	0	1	1	1
1.743V	1.1625V	0	0	0	1	1	1
1.762V	1.175V	1	1	1	0	1	1
1.781V	1.1875V	0	1	1	0	1	1
1.8V	1.20V	1	0	1	0	1	1
1.818V	1.2125V	0	0	1	0	1	1
1.837V	1.225V	1	1	0	0	1	1
1.856V	1.2375V	0	1	0	0	1	1
1.875V	1.25V	1	0	0	0	1	1
1.893V	1.2625V	0	0	0	0	1	1
1.912V	1.275V	1	1	1	1	0	1
1.931V	1.2875V	0	1	1	1	0	1
1.95V	1.300V	1	0	1	1	0	1
1.968V	1.3125V	0	0	1	1	0	1

FBVDD	VDA_PWR	VID125	VID0	VID1	VID2	VID3	VID4
1.900V	1.100V	1	0	1	1	1	1
1.9125V	1.1125V	0	0	1	1	1	1
1.925V	1.125V	1	1	0	1	1	1
1.9375V	1.1375V	0	1	0	1	1	1
1.950V	1.150V	1	0	0	1	1	1
1.9625V	1.1625V	0	0	0	1	1	1
1.975V	1.175V	1	1	1	0	1	1
1.9875V	1.1875V	0	1	1	0	1	1
2.00V	1.20V	1	0	1	0	1	1
2.0125V	1.2125V	0	0	1	0	1	1
2.025V	1.225V	1	1	0	0	1	1
2.0375V	1.2375V	0	1	0	0	1	1
2.05V	1.25V	1	0	0	0	1	1
2.0625V	1.2625V	0	0	0	0	1	1
2.075V	1.275V	1	1	1	1	0	1
2.0875V	1.2875V	0	1	1	1	0	1
2.100V	1.300V	1	0	1	1	0	1
2.1125V	1.3125V	0	0	1	1	0	1
2.125V	1.325V	1	1	0	1	0	1
2.1375V	1.3375V	0	1	0	1	0	1
2.150V	1.350V	1	0	0	1	0	1
2.1625V	1.3625V	0	0	0	1	0	1
2.175V	1.375V	1	1	1	0	0	1
2.1875V	1.3875V	0	1	1	0	0	1
2.200V	1.400V	1	0	1	0	0	1
2.2125V	1.4125V	0	0	1	0	0	1
2.225V	1.425V	1	1	0	0	0	1
2.2375V	1.4375V	0	1	0	0	0	1
2.250V	1.450V	1	0	0	0	0	1
2.2625V	1.4625V	0	0	0	0	0	1

Micro-Star International Co., LTD.	
FBVDD with MS-11	
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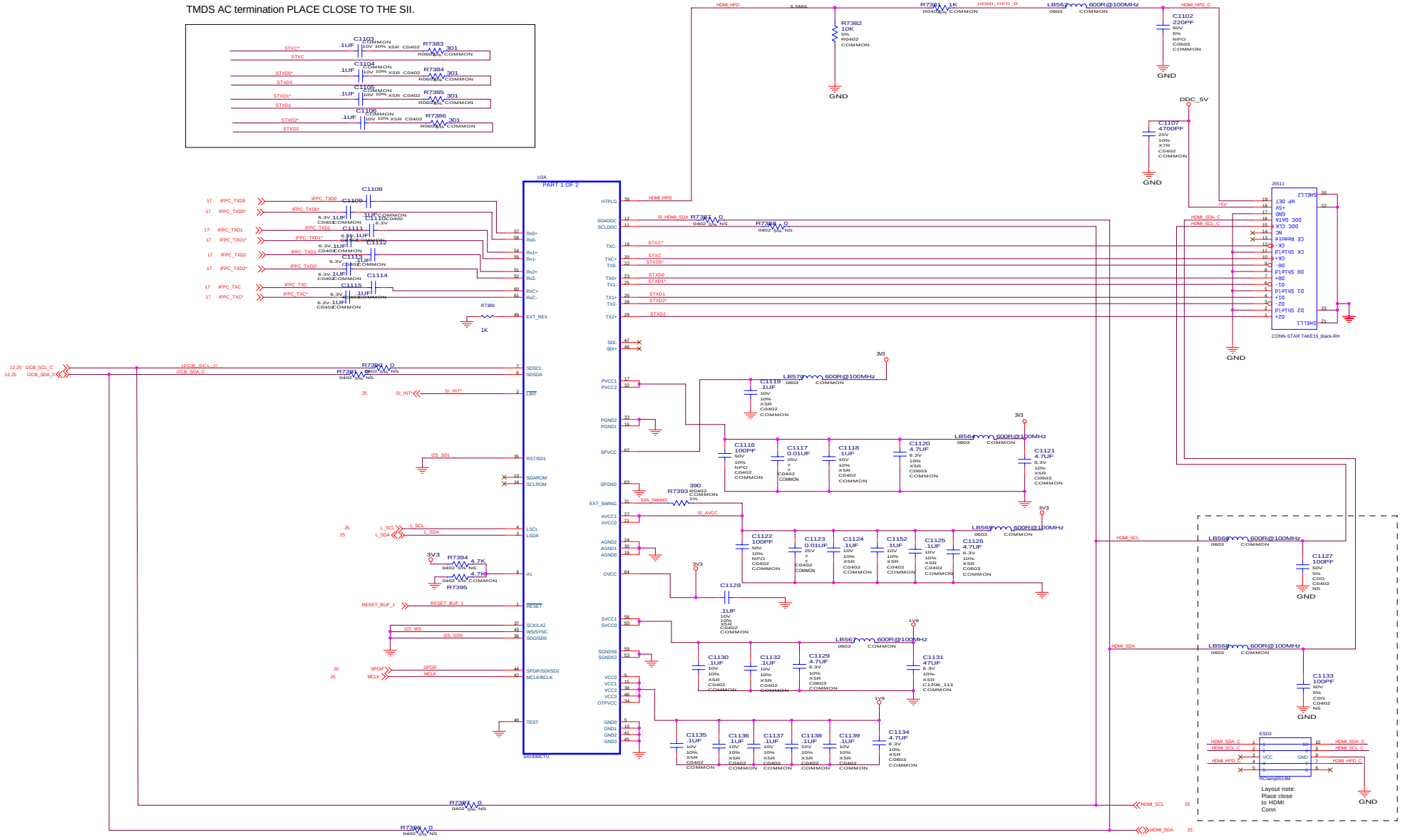
Hotplug Detection

Capacitance of HDMI_SDA_C & HDMI_SCL_C nets to Power/GND planes must be less than 50pF (try to make it lower)

TMDS AC termination PLACE CLOSE TO THE SII.



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HDMI LINK Sil 1930	
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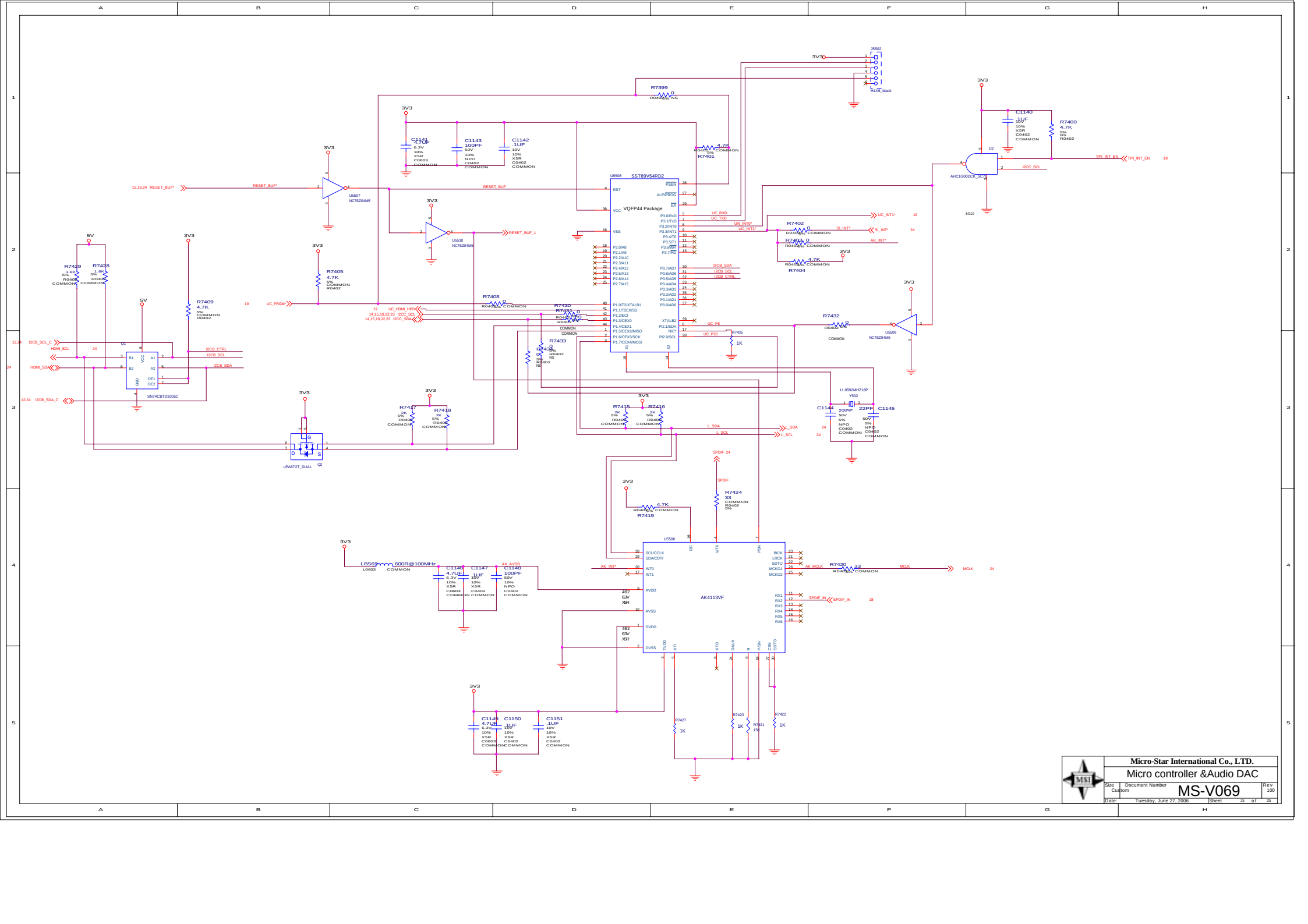
Micro-Star International Co., LTD.
Micro controller &Audio DAC
Size: Custom
Document Number: MS-V069
Rev: 100
Date: Tuesday, June 27, 2006
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SST89V54RD2
VQFP44 Package
AK4113VF
SN74CBTD3305C
uPA672T_DUAL
NC7SZ04M5
AHC1G00DCK_SC70
LB603 600R@100MHz COMMON
11.0592MHZ18P
JS502
TPI_INT_EN
SPDIF
SPDIF_IN
MCLK
AK_MCLK
I2CB_SCL
I2CB_SDA
I2CB_CTRL
L_SDA
L_SCL
UC_INT1*
SI_INT*
AK_INT*
UC_RXD
UC_TXD
UC_P6
UC_P28
RESET_BUF
RESET_BUF*
UC_PRGM*
UC_HDMI_HPD
I2CC_SCL
I2CC_SDA
HDMI_SCL
HDMI_SDA
AK_AVDD