P409:MXM-III,G3-128,256/512MB,128-bit,8/16Mx32 DDR-3 LVDS,DVI_A, DVI_B,TV_OUT,VGA

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HISTORY:

A03: INITIAL VERSION

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10409-xxxx-300	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	0501	600-50409-0501-300	N88E-SE/G84-750 with HDCP Kit,512MB, 8pcs 16Mx32 GDDR3
2	0002	600-10409-0002-300	N88P-NVS2/G84-710 with HDCP Kit, 256MB,4pcs 16Mx32 GDDR3 (1MbVBIOSROM)
3	0003	600-10409-0003-300	N88E-SE/G84-750 with HDCP Kit, 512MB, 8pcs 16Mx32 GDDR3 (1MbVBIOSROM)
4	0004	600-10409-0004-300	N88E-SE/G84-750 with HDCP Kit, 512MB, 8pcs 16Mx32 GDDR3
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview

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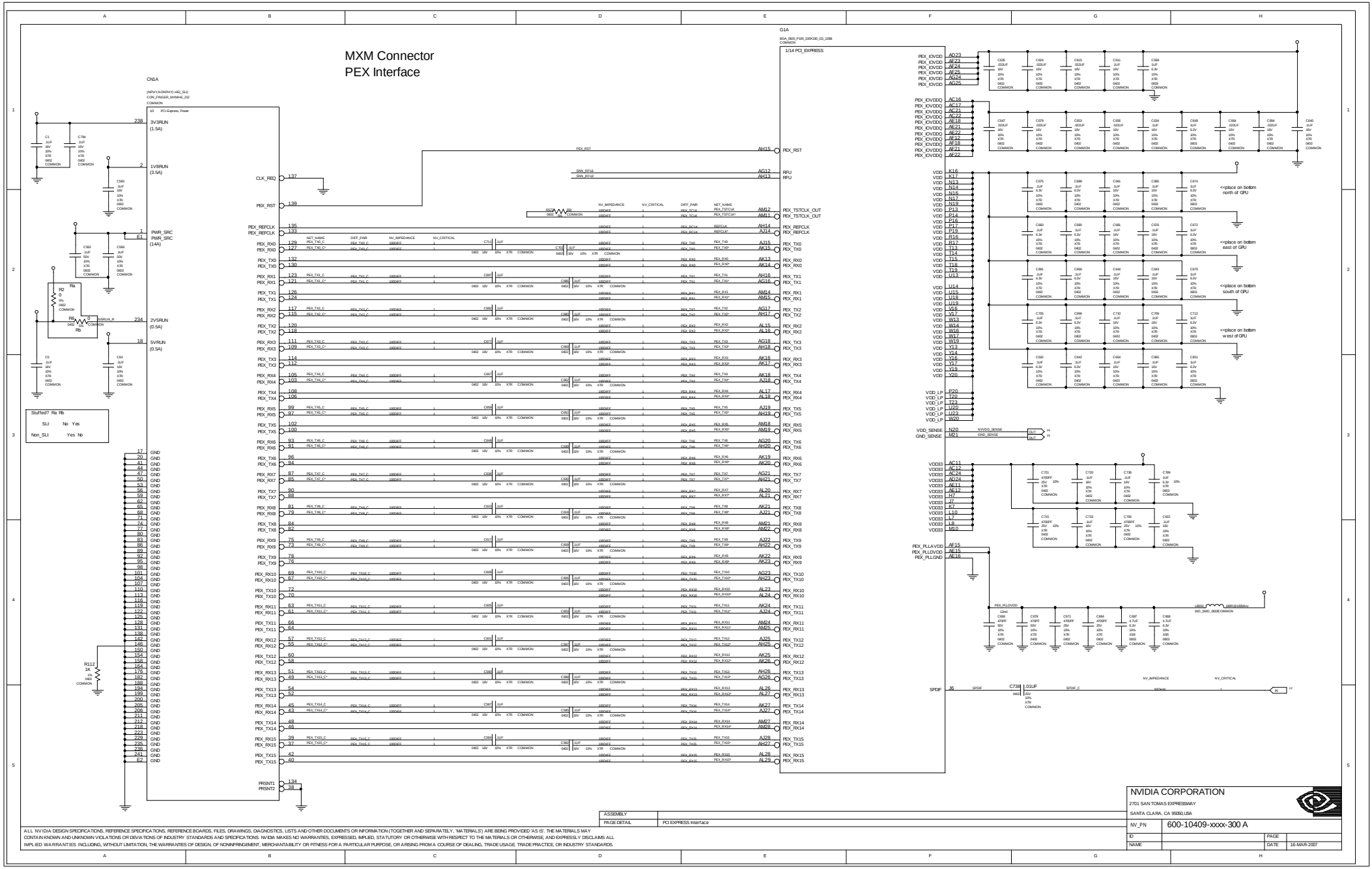

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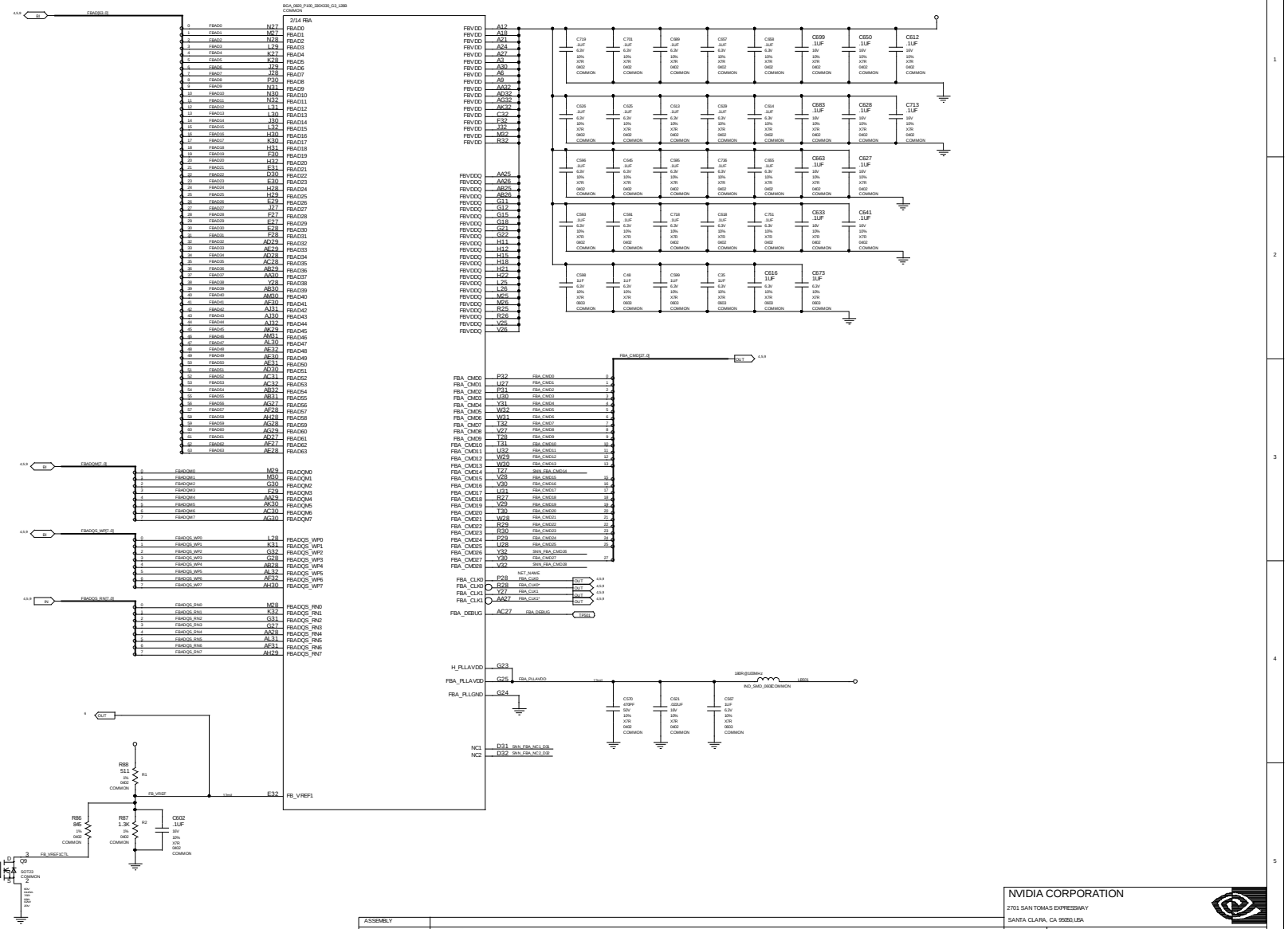
Frame Buffer A GPU



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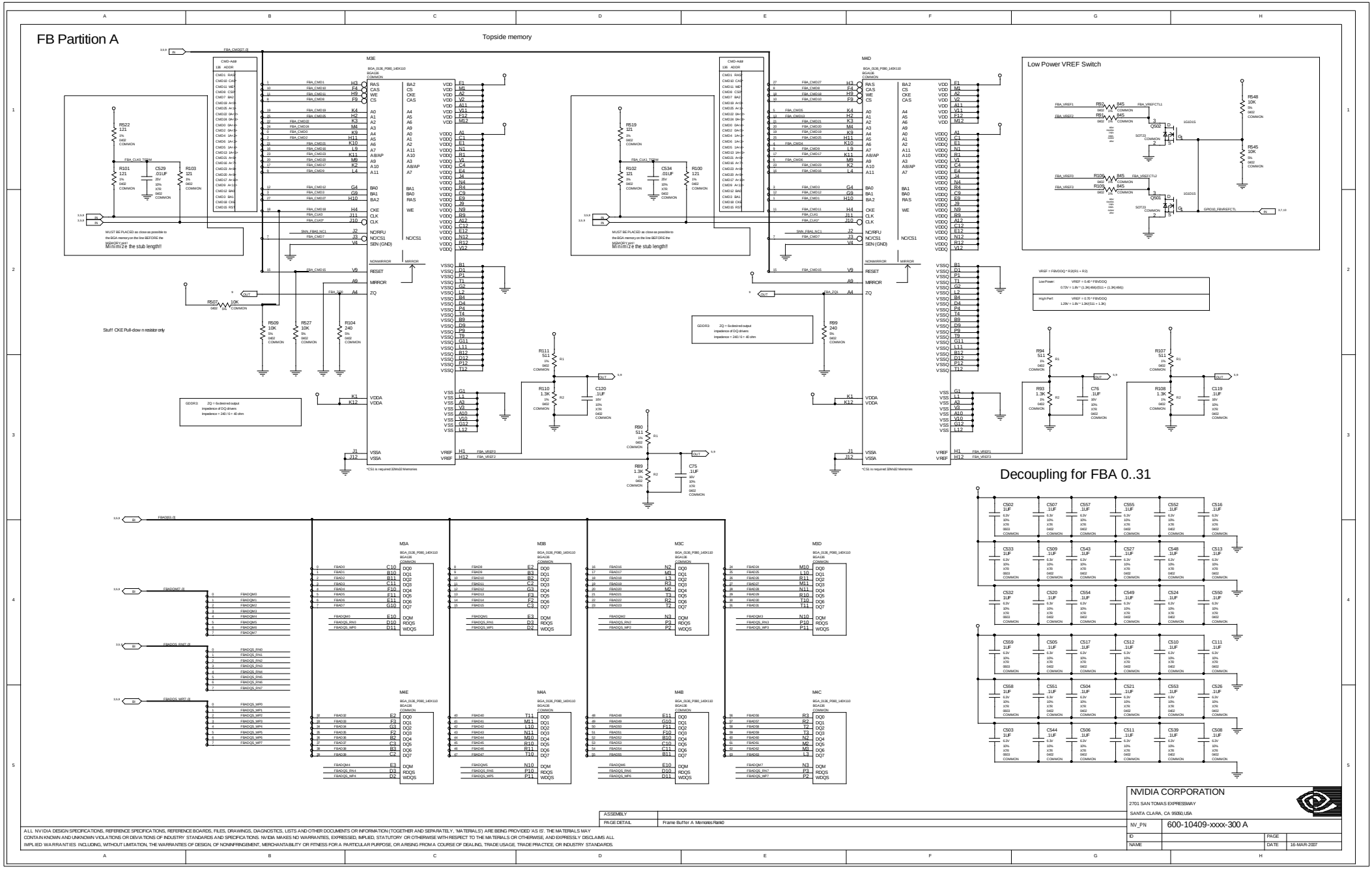

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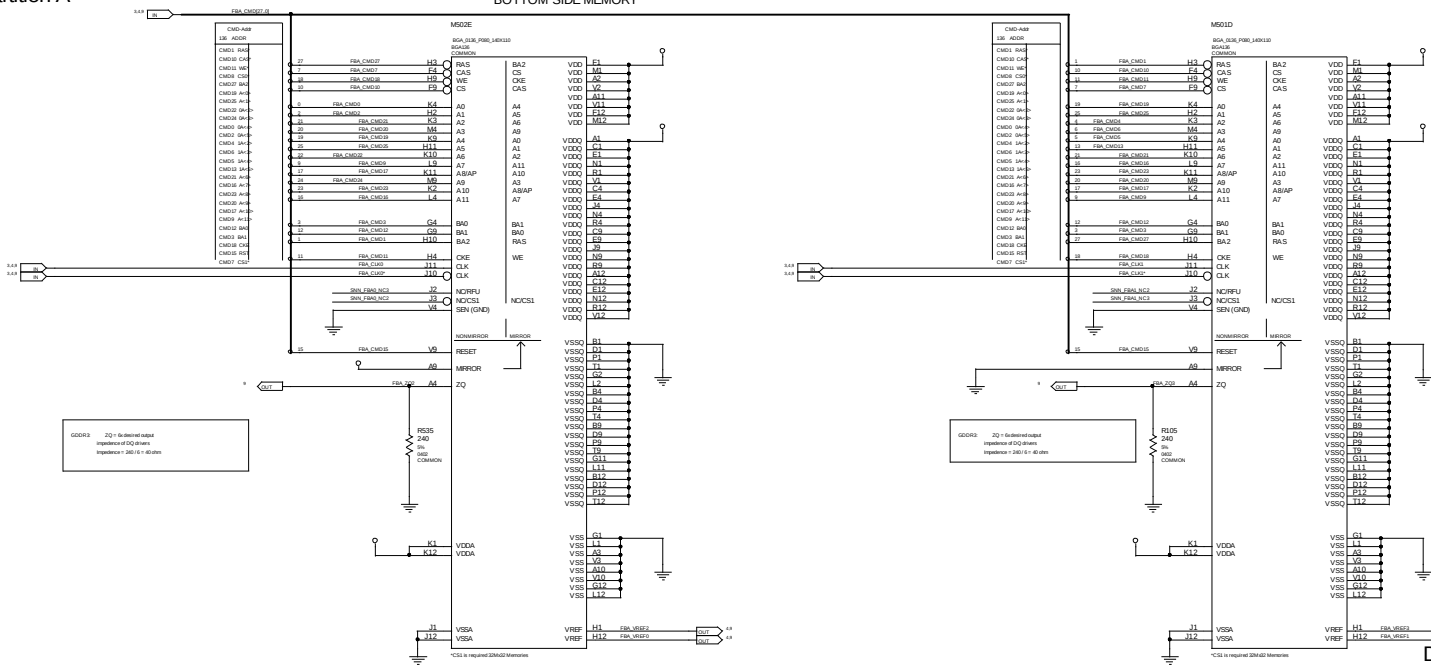
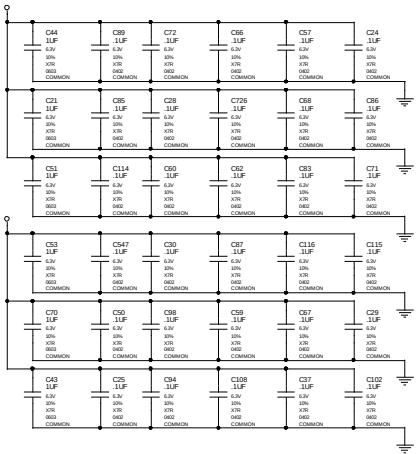
FB Partition A

BOTTOM SIDE MEMORY



Decoupling for FBA 0..31



ASSEMBLY	
PAGE DETAIL	Frame Buffer A Memories Rank1

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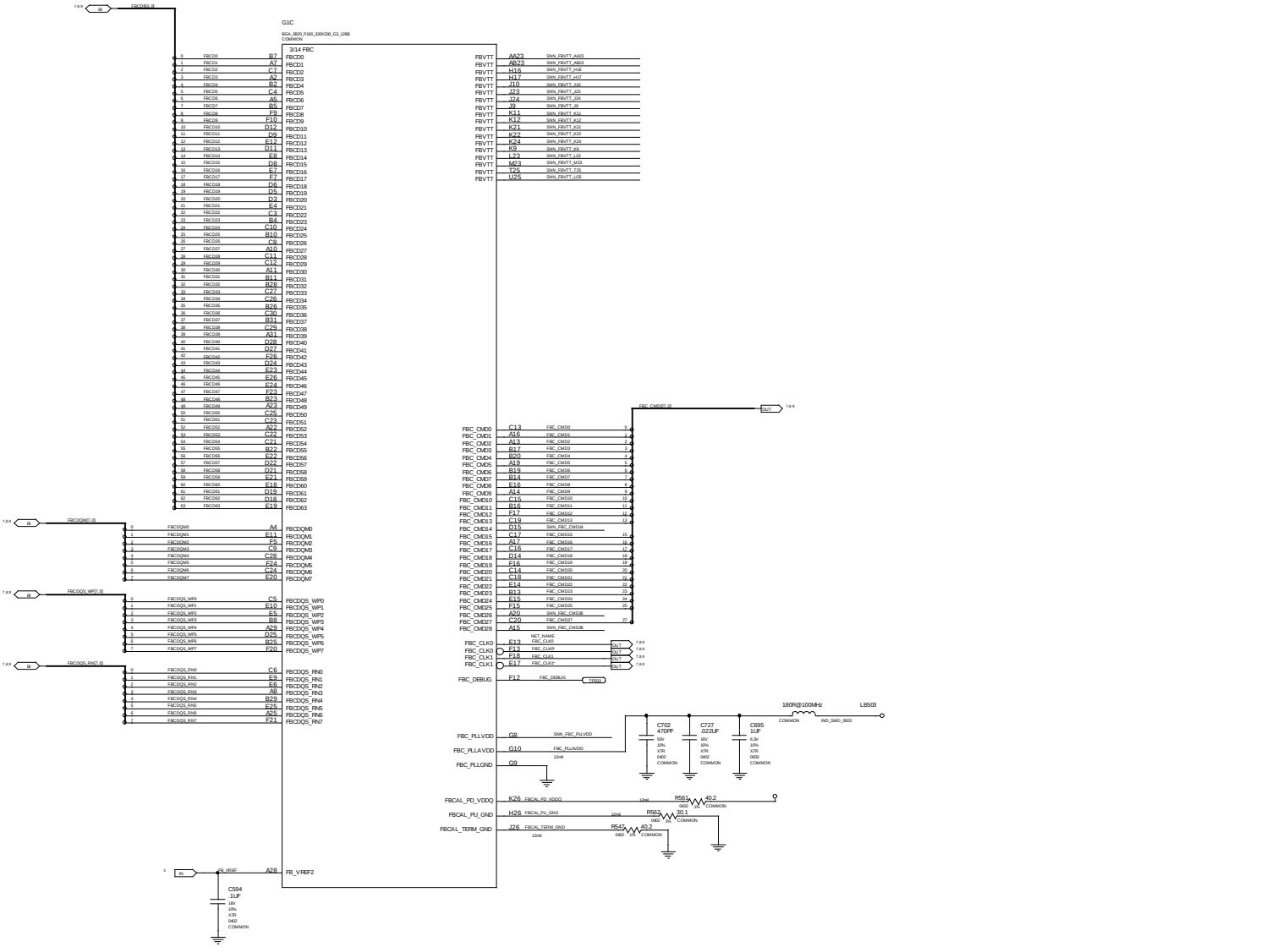
Frame Buffer C GPU



ASSEMBLY	
PAGE DETAIL	Frame Buffer C GPU

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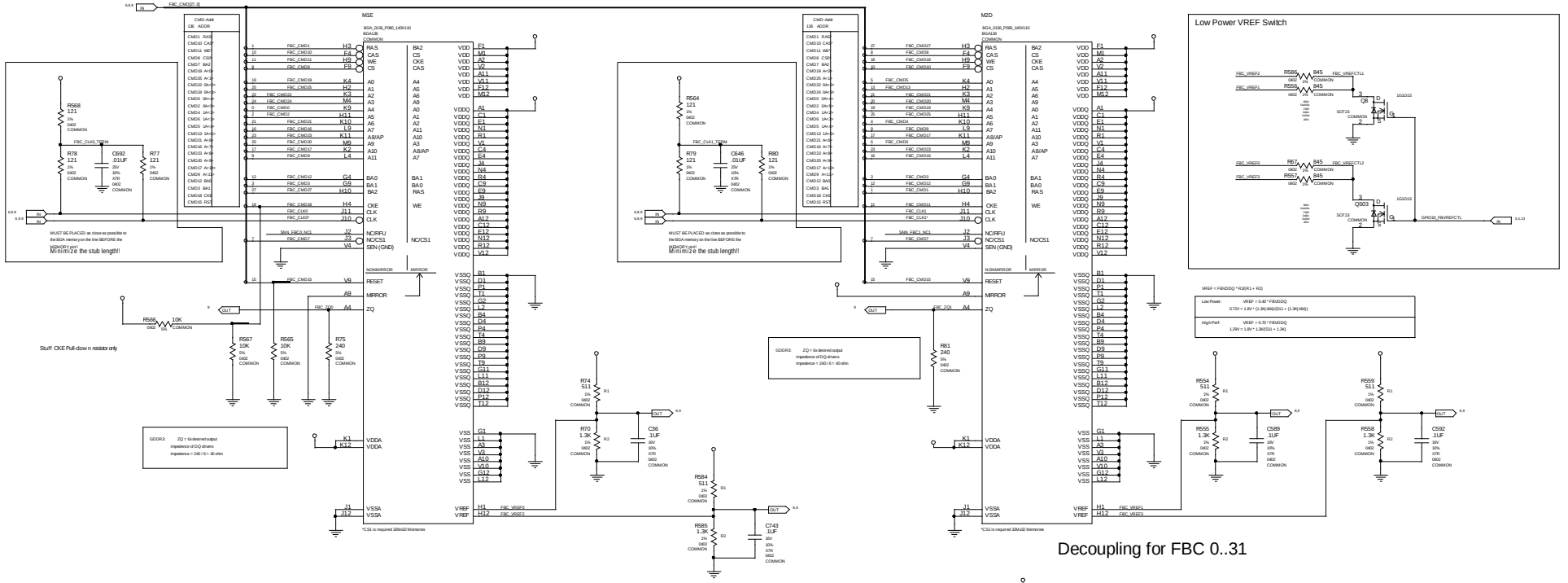
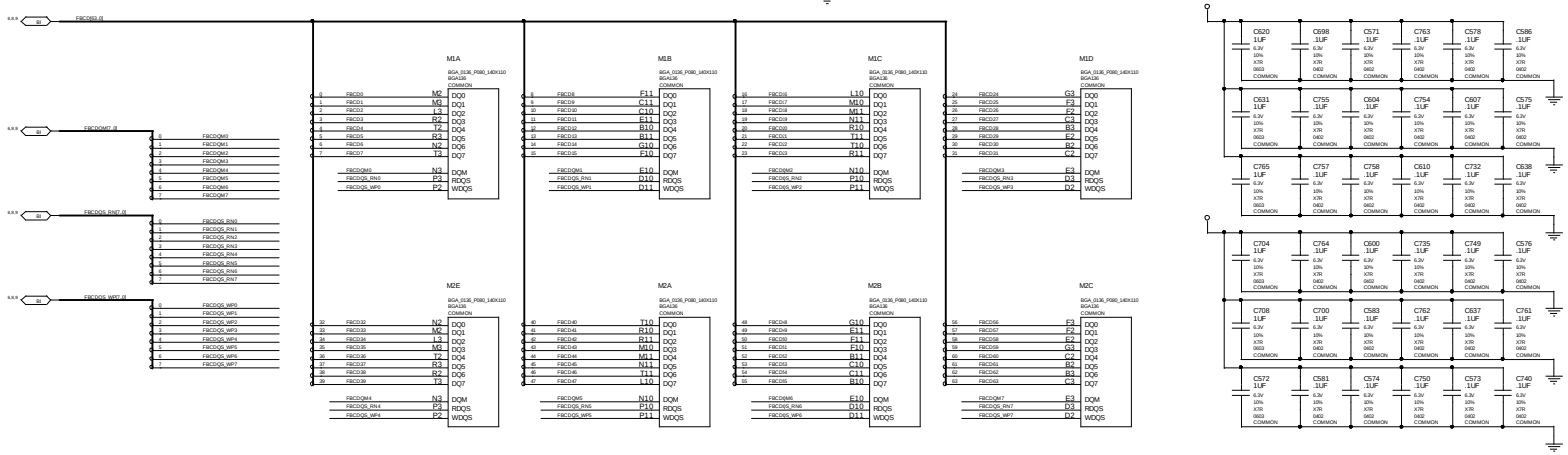
FB Partition C

Topside memory





ASSEMBLY	
PAGE DETAIL	Frame Buffer C Memories Rank0

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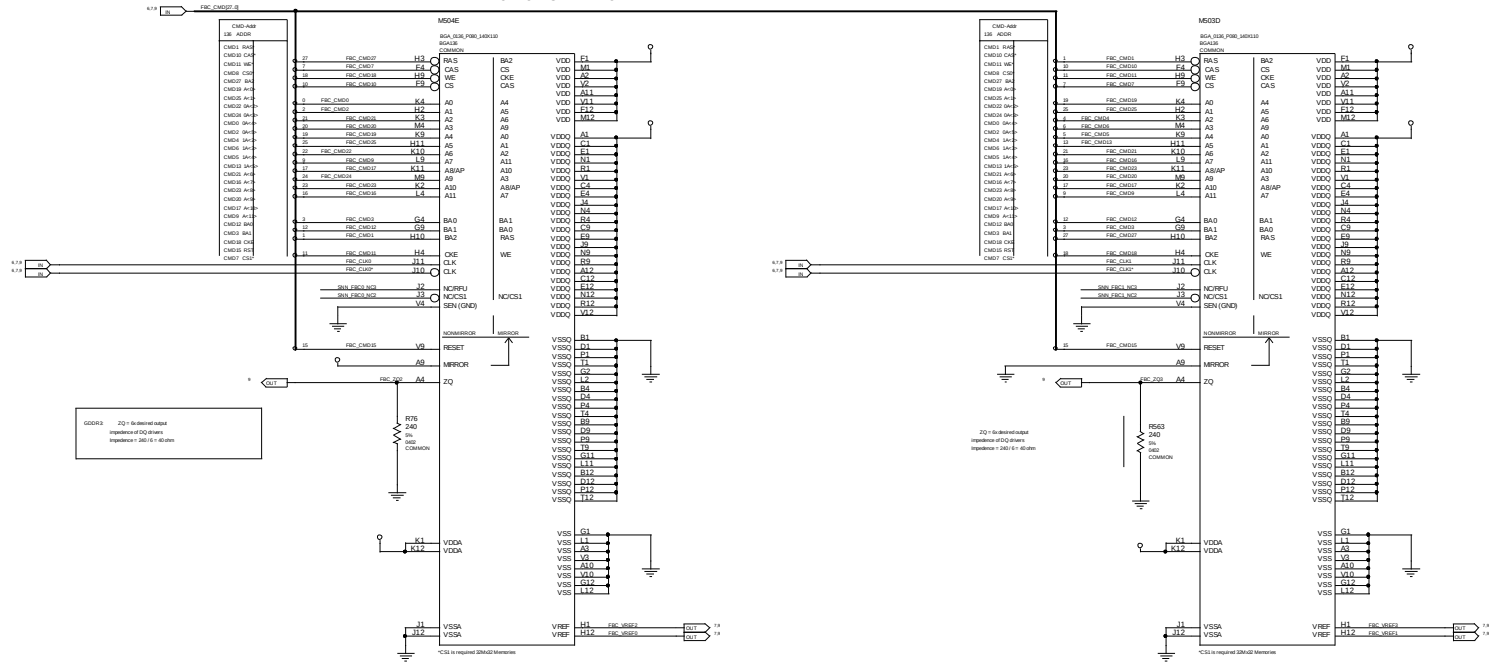
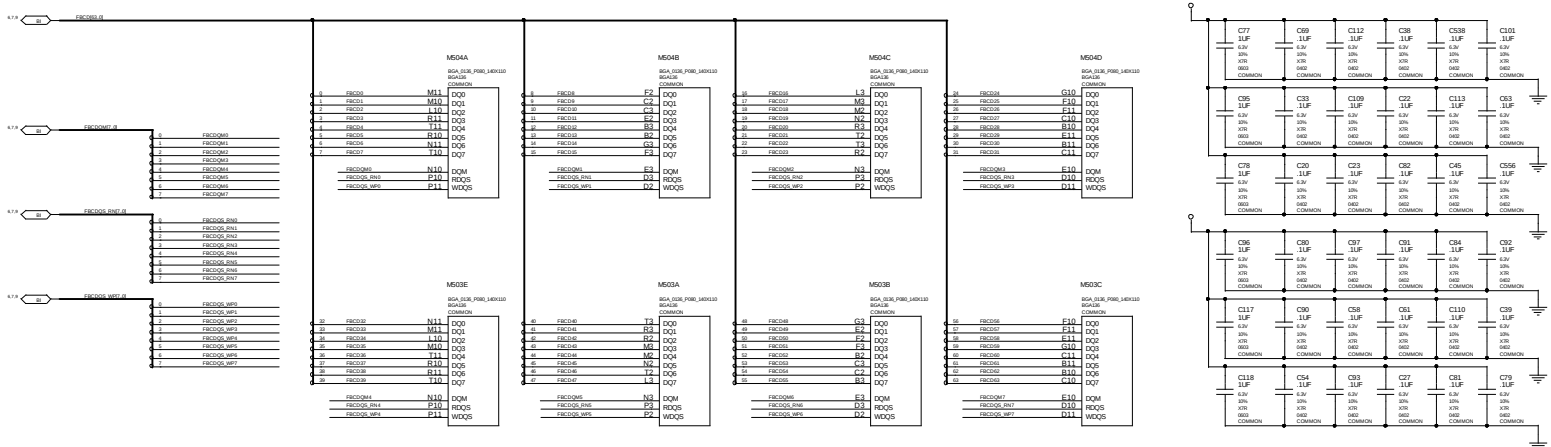
FB Partition C

BOTTOM SIDE MEMORY



Decoupling for FBC 0..31



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PAGE DETAIL	Frame Buffer C Memories Rank1

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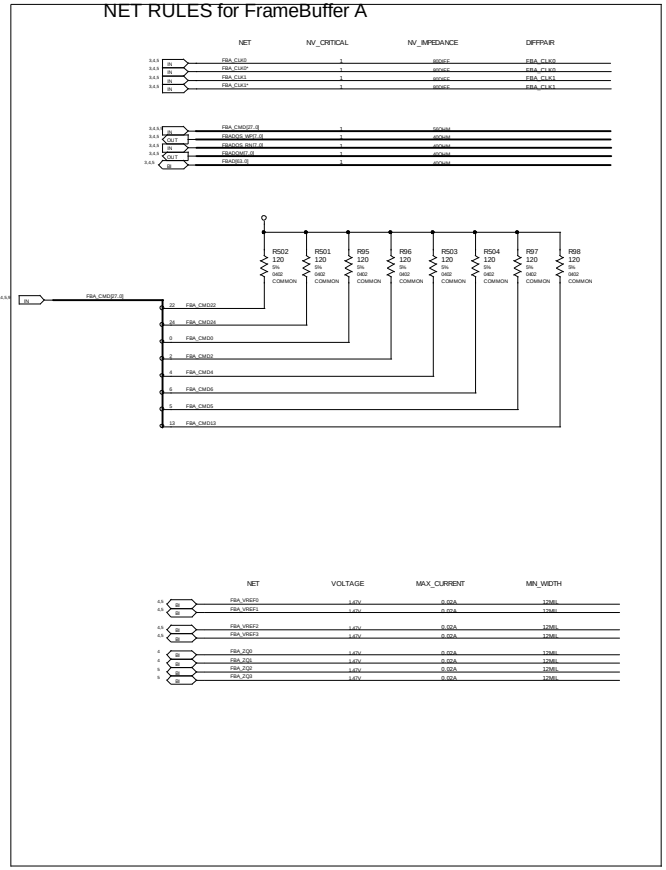
FrameBuffer Net Rules

NET RULES for FrameBuffer A



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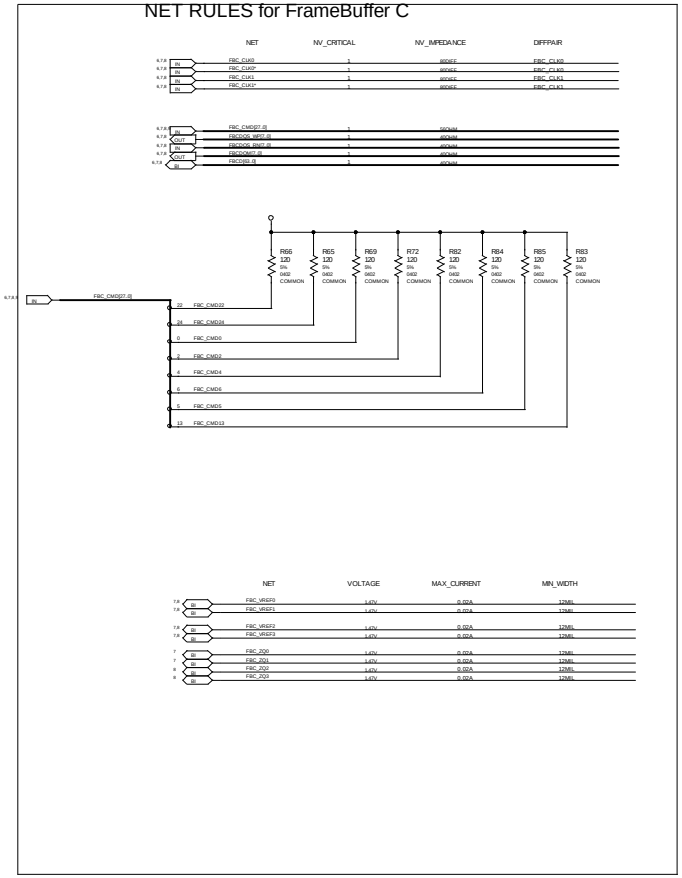

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ASSEMBLY	
PAGE DETAIL	Frame Buffer Physical Constrains

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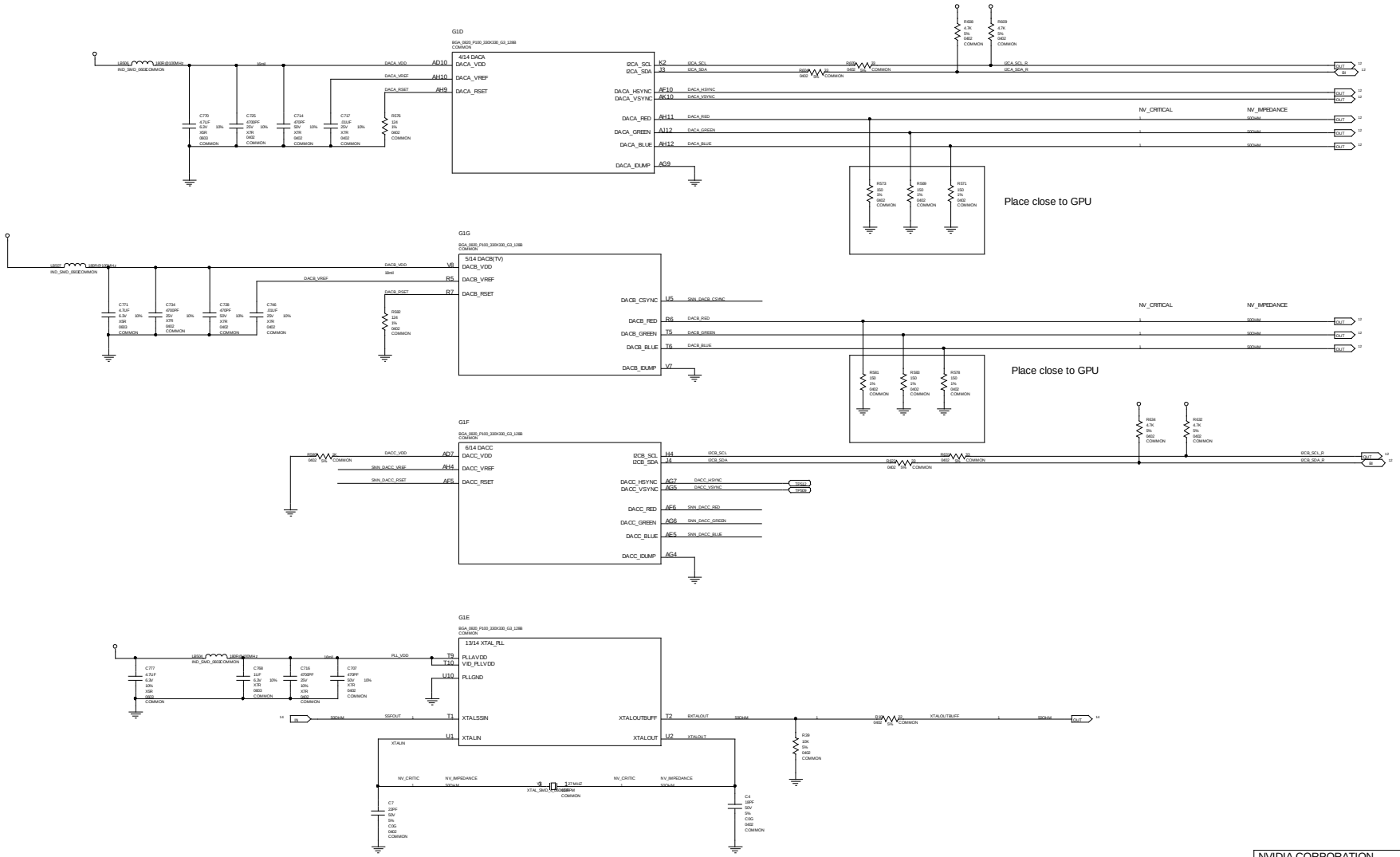
DACs, Clockgeneration



ASSEMBLY	
PAGE DETAIL	DACs, Clock-Generation

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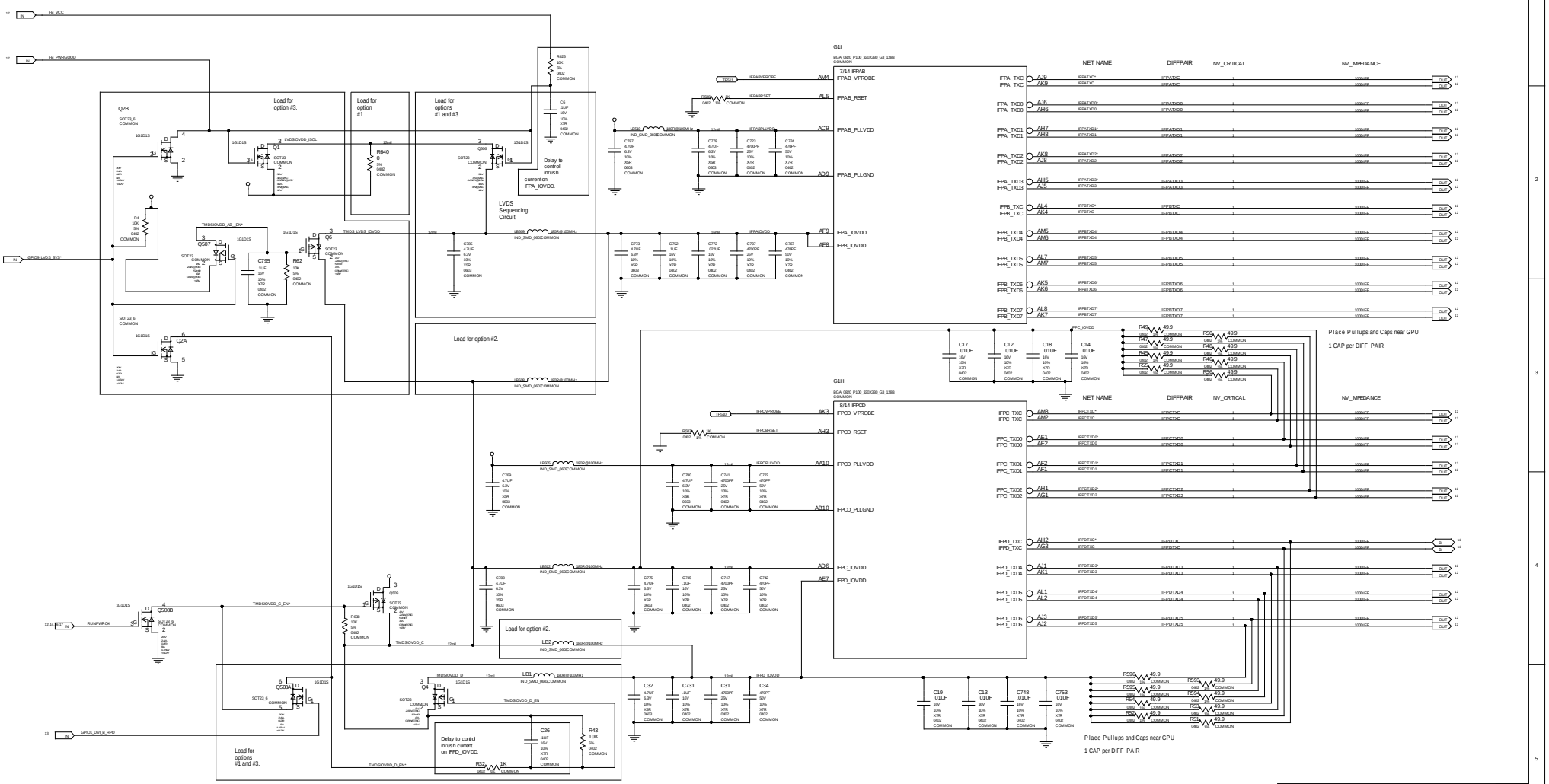
LVDS / TMDS Interface

Loading options for IFPAB outputs

Option #1) IFPAB outputs to LVDS only.
Option #2) IFPAB outputs to DVI-C only.
Option #3) Controlled with GPIO9, IFPAB dynamically outputs to LVDS or DVI-C.



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LVDS / TMDS Interface GPU

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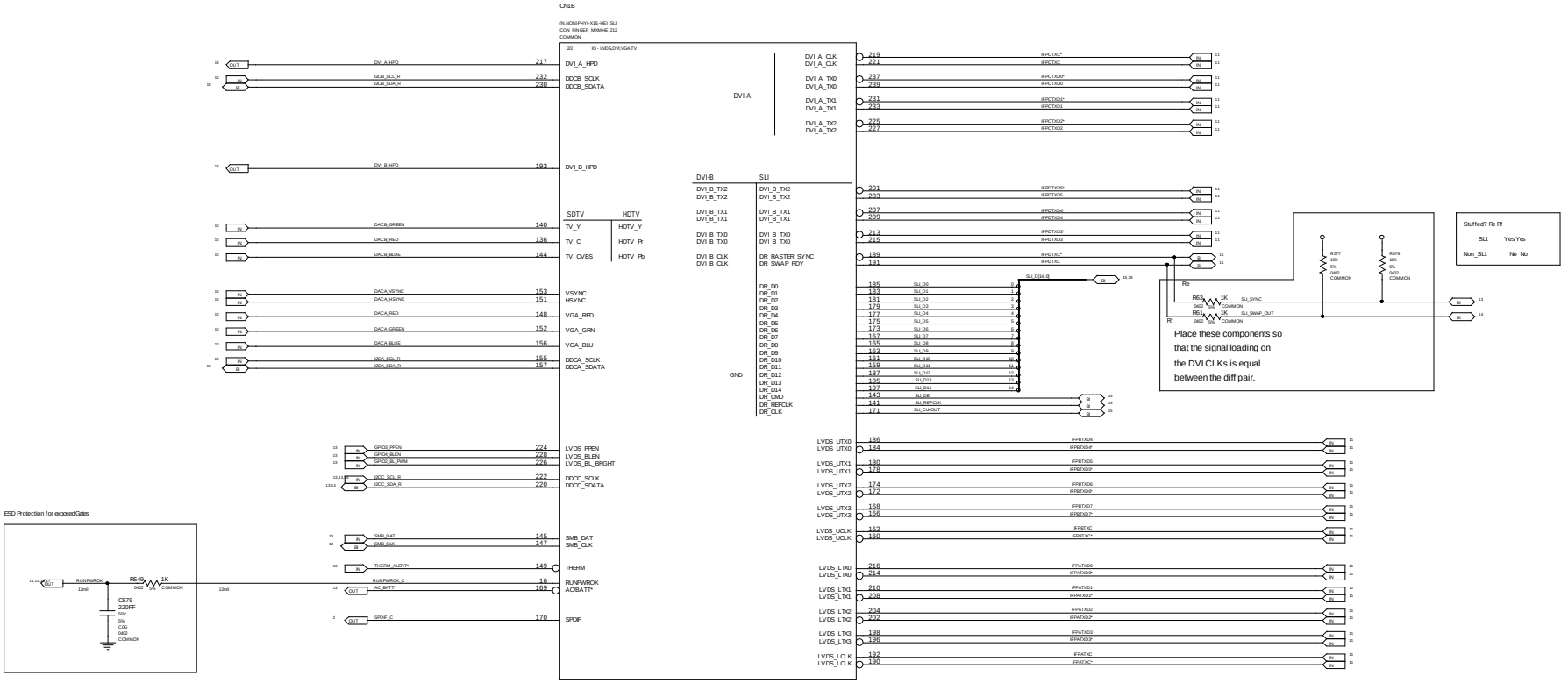
MXM Connector IO-Section



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ASSEMBLY	
PAGE DETAIL	MXM Connector IO-Section

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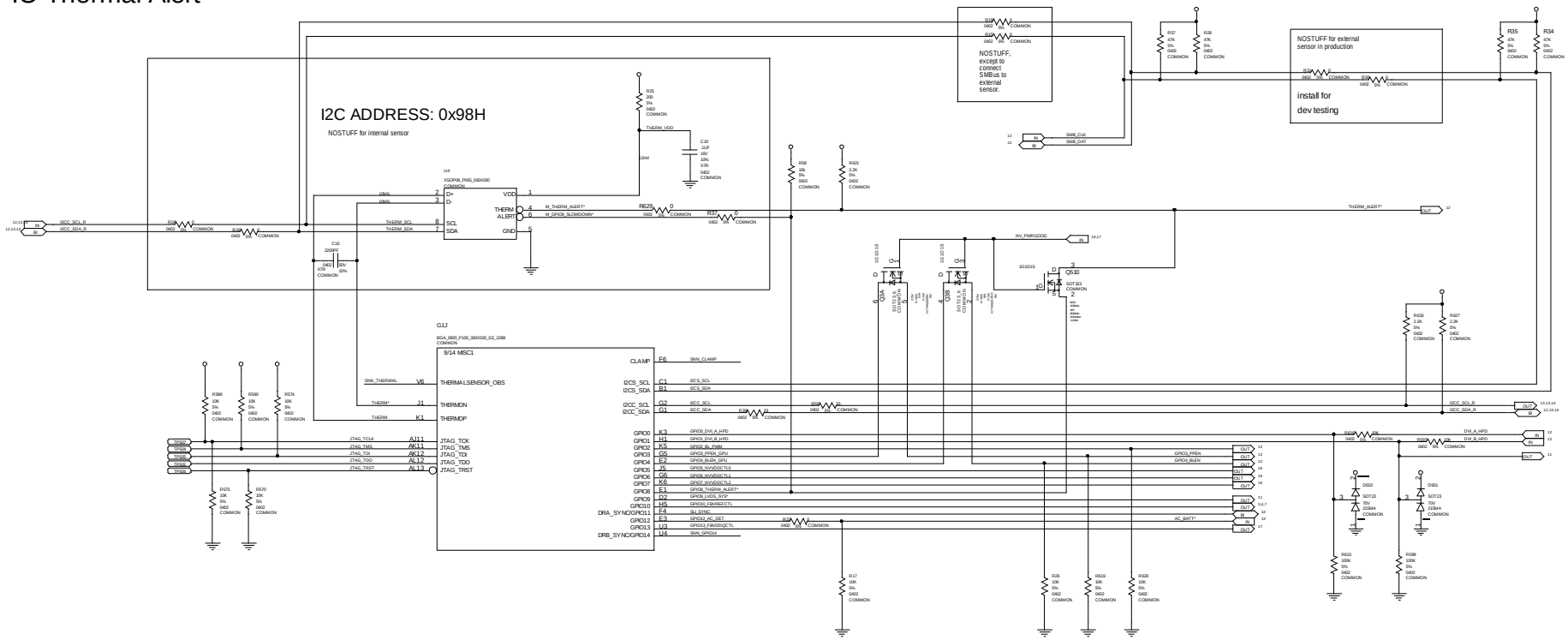
GPIO Thermal Alert



ASSEMBLY	
PAGE DETAIL	GPIO Thermal Sensor Chip

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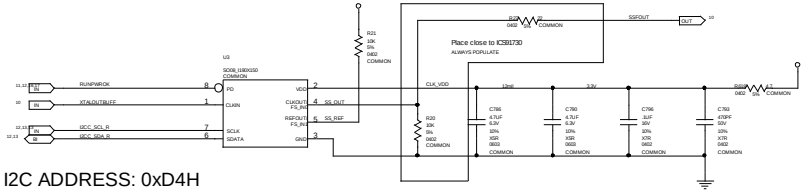
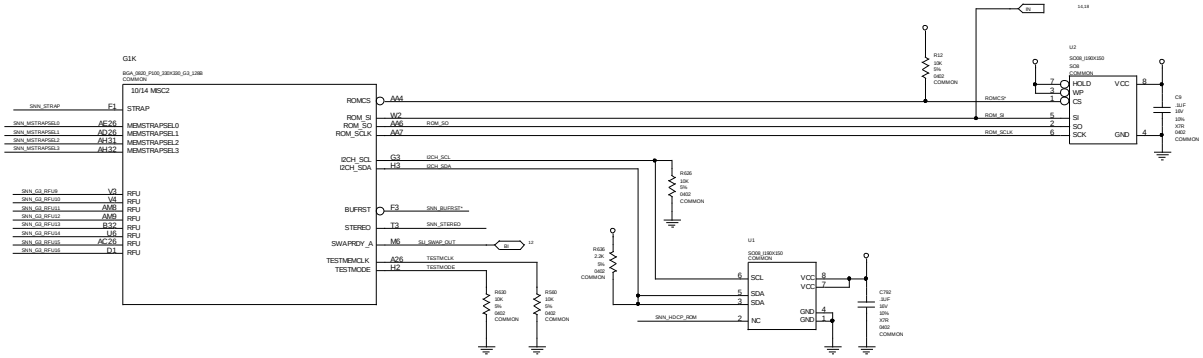
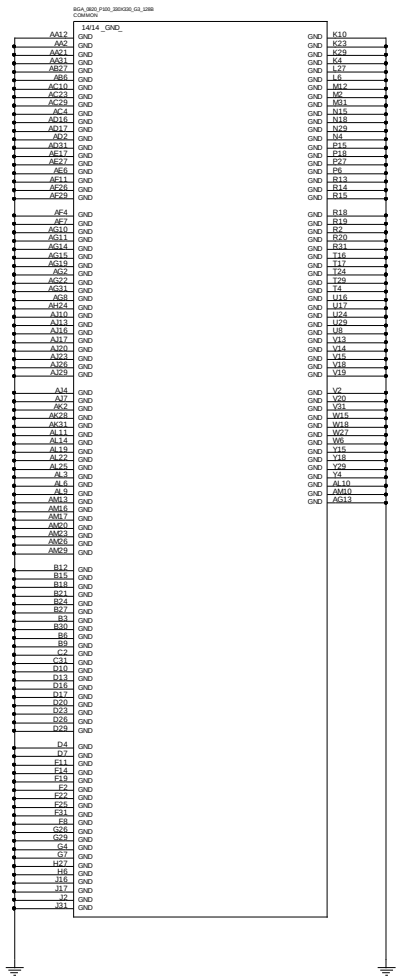
SPREAD SPECTRUM CLOCK



I2C ADDRESS: 0xD4H

ROM Interface





ASSEMBLY	
PAGE DETAIL	Spread Spectrum, BIOS/ HDCP ROM

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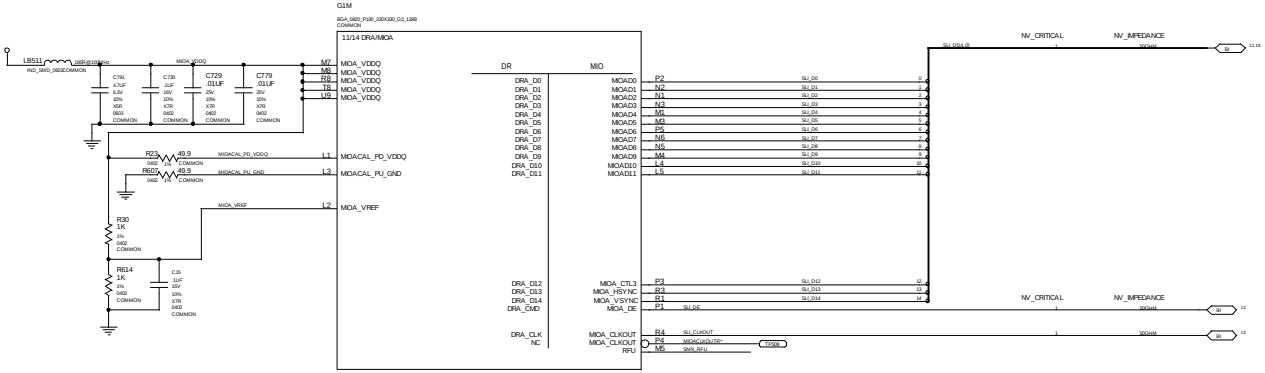
MIOA



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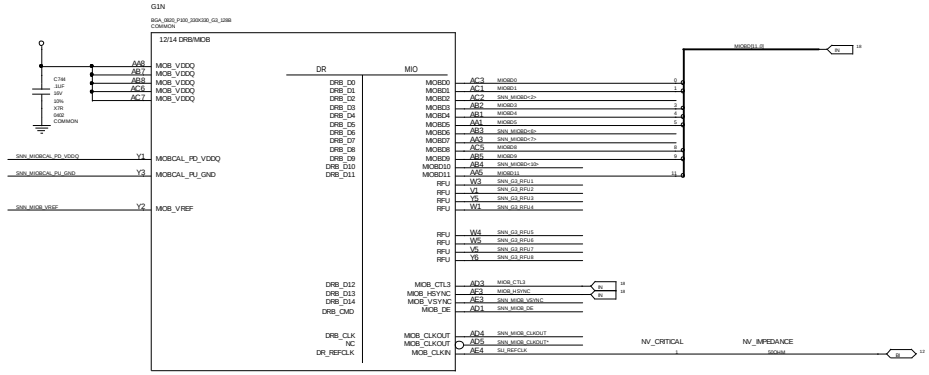

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ASSEMBLY	
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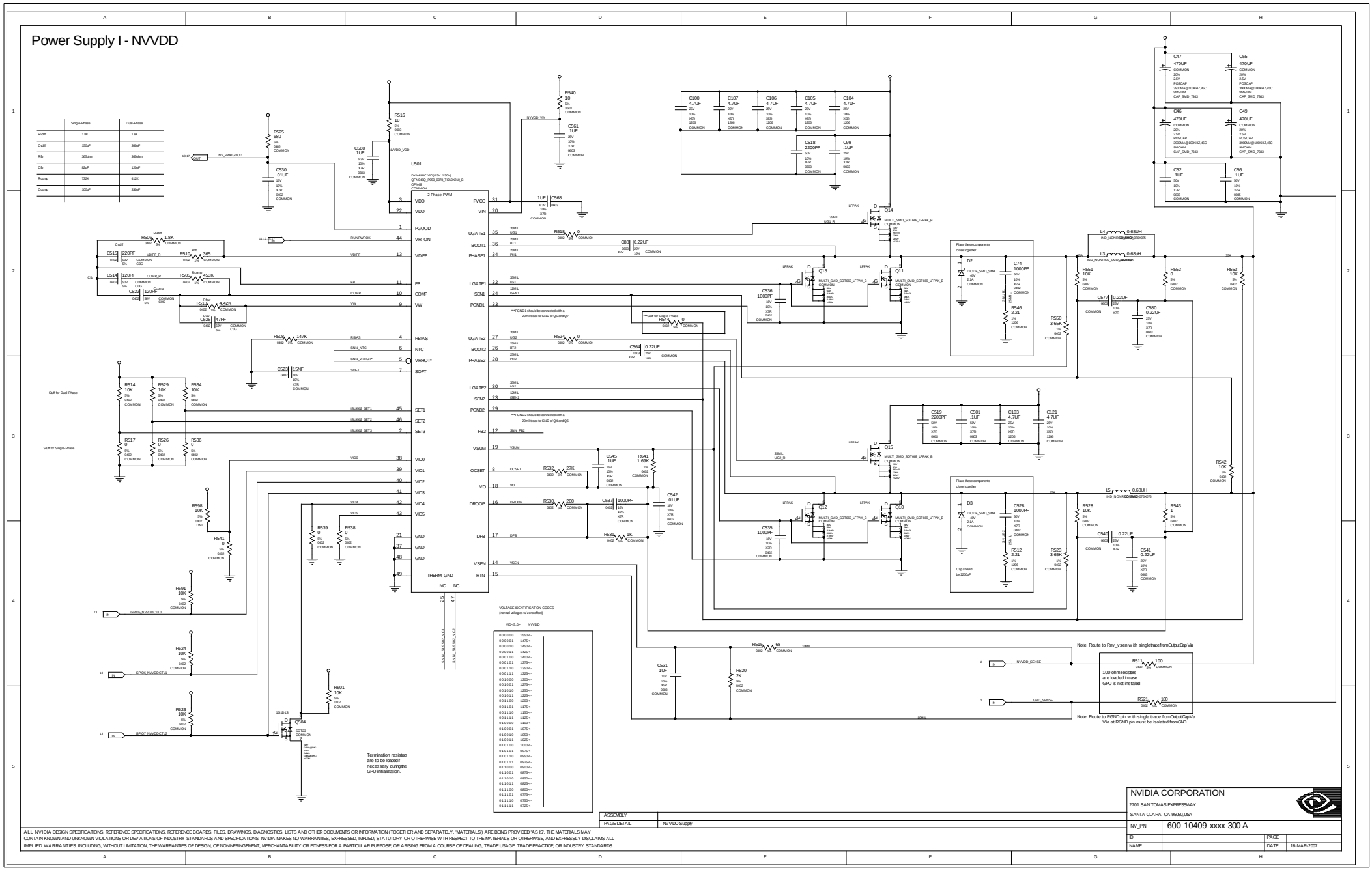

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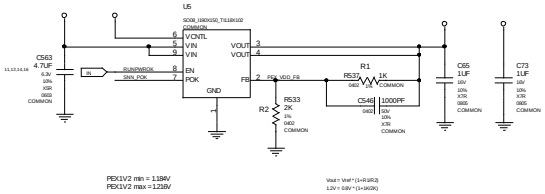
Power Supply II - FBVDDQ, PEX_VDD, and LVDS_IOVDD

NETatt	MIN_LINE_WIDTH		VOLTAGE
5VRUN	16MIL	0.5A	5V
3V3RUN	16MIL	1.5A	3.3V
1V8RUN	16MIL	3.5A	1.8V
PEX1V2	16MIL	1A	1.2V
FBVDDQ	16MIL	10A	2.0V
NVVDD	25MIL		1.25V
PWR_SRC	16MIL	4A	22V
2V5RUN	16MIL	0.5A	2.5V
GND	16MIL	25A	0V

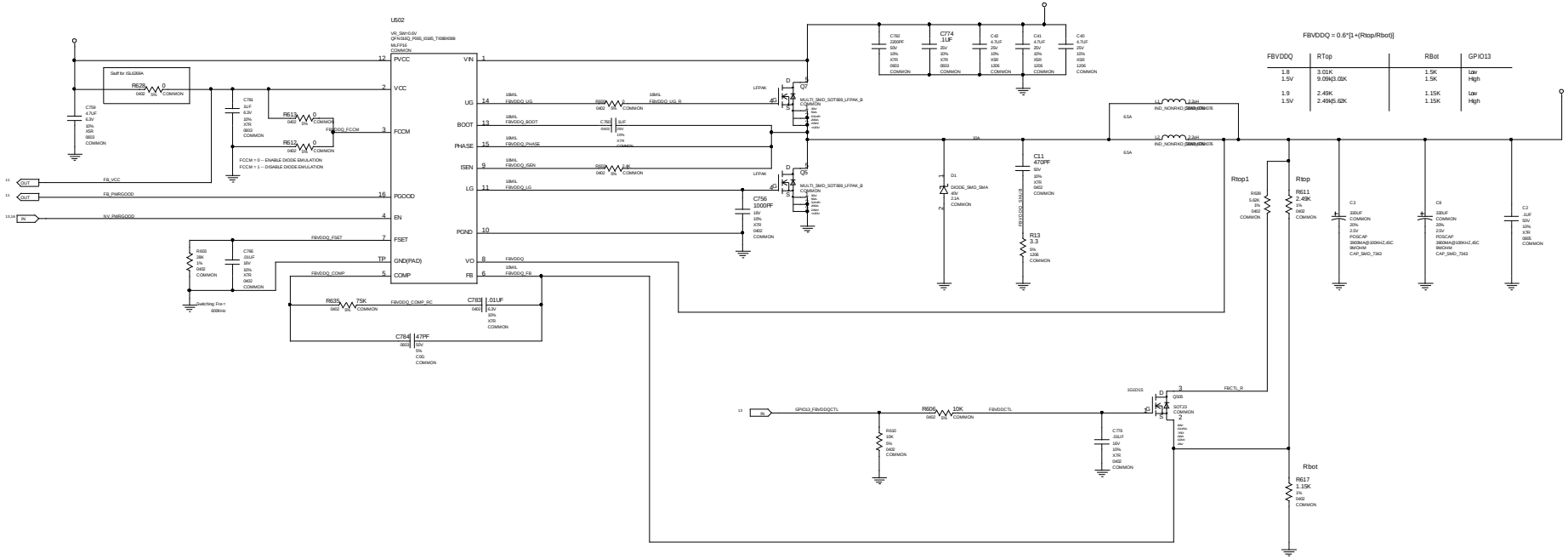
PEX_VDD

PEXVDD = 1.2V @ 1.8A



PEX1V2 min = 1.188V
PEX1V2 max = 1.212V

FBVDDQ



FBVDDQ = 0.6*[1+(Rtop/Rbot)]

FBVDDQ	RTop	RBot	GPIO13
1.8	3.01K	1.5K	Low
1.5V	9.09K|3.01K	1.5K	High
1.9	2.49K	1.15K	Low
1.5V	2.49K|5.62K	1.15K	High

ASSEMBLY	
PAGE DETAIL	FBVDDQ, PEX1V2, PLLVDD Supply

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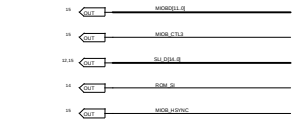
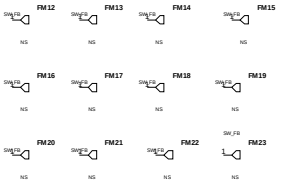
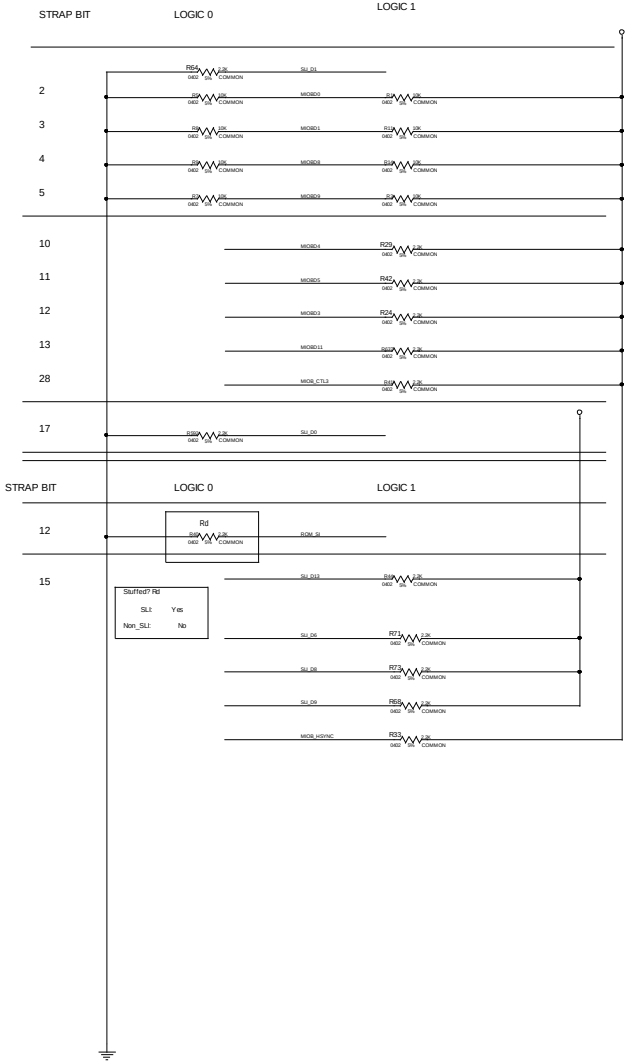




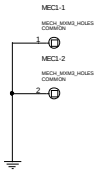


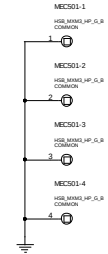
REG: NV_STRAP_0

SUB_VENDOR	1 = Read from BIOS
RAM_CFG_0	RAM_CFG[3:0]
RAM_CFG_1	MS_1001: 16Mx32 GDDR3 SDRAM 128 Bit, Qimoda Dual Rank MS_1010: 16Mx32 GDDR3 SDRAM 128 Bit, Hynix Dual Rank
RAM_CFG_2	MS_1011: 16Mx32 GDDR3 SDRAM 128 Bit, Samsung Dual Rank MS_0011: 16Mx32 GDDR3 SDRAM 128 Bit, Samsung Single Rank
RAM_CFG_3	MS_0010: 16Mx32 GDDR3 SDRAM 128 Bit, Hynix Single Rank
PCI_DEVID_0	MS_00111: (G84M-600)
PCI_DEVID_1	MS_01000: (G84M-700) MS_01001: (G84M-750)
PCI_DEVID_2	MS_01010: (G84M-610) MS_01100: (G84GLM-950)
PCI_DEVID_3	MS_01101: (G84GLM-975)
PCI_DEVID_EXT (4)	
PEX_PLL_EN_TERM100	

REG: NV_STRAP_1

MIOA_EN_3.3V	
Slot Clock Configuration	
3GIO_PADCFG_LUT_ADR[0]	
3GIO_PADCFG_LUT_ADR[1]	
3GIO_PADCFG_LUT_ADR[2]	
3GIO_PADCFG_LUT_ADR[3]	





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Title: Basenet Report
Design: p409
Date: Feb 9 16:02:25 2007

Base nets and synonyms for
p409_lib:P409{@p409_lib.p409(sch_1)}
Base Signal Location([Zone]([dir])

1VBRUN 17.1A
2VSRUN 17.1A
2VSRUN_R 2.2A
3VSRUN 17.1A
5VRUN 17.1A
AC_BATT* 12.4C> 13.3G<
BT1 16.2C
BT2 16.2C
BXTALOUT 10.4D
CLK_VDD 14.2C
COMP 16.2B
COMP_R 16.2A
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DACA_GREEN 10.2H> 12.3B<
DACA_HSYNC 10.1H> 12.3B<
DACA_RED 10.2H> 12.3B<
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DACC_VSYNC 10.3D
DFB 16.4C
DROOP 16.3C
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FBCDQS_WPB<5> 6.3C 7.5B 7.5C 8.5B 8.5C
FBCDQS_WPB<6> 6.4C 7.5B 7.5D 8.5B 8.5D
FBCDQS_WPB<7> 6.4C 7.5B 7.5E 8.5B 8.5E
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FBC_CLK0* 6.4E> 7.2A< 8.2A< 9.1E<
FBC_CLK0_TERM 7.1A
FBC_CLK1 6.4E> 7.2D< 8.2D< 9.1E<
FBC_CLK1* 6.4E> 7.2D< 8.2D< 9.2E<
FBC_CLK1_TERM 7.1D
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FBC_VREFCTL2 7.1G
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FBVDDCTL 17.4E
FBVDDQ 17.1A 17.3C
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FBVDDQ_COMP 17.3B
FBVDDQ_COMP_RC 17.3C
FBVDDQ_FB 17.3C
FBVDDQ_FCCM 17.3B
FBVDDQ_FSET 17.3B
FBVDDQ_ISEN 17.3C
FBVDDQ_LG 17.3C
FBVDDQ_PHASE 17.3C
FBVDDQ_SNUB 17.3F
FBVDDQ_UG 17.2C
FBVDDQ_UG_R 17.2D
FB_PWRGOOD 11.1A< 17.3A>
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GPIO1_DVI_B_HPD 11.5A< 13.3H>
GPIO2_BL_PWM 12.4C< 13.3G>
GPIO3_PPEN 12.3C< 13.3G>
GPIO3_PPEN_GPU 13.3D
GPIO4_BLEN 12.4C< 13.3G>
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GPIO8_THERM_ALERT* 13.3D
GPIO9_LVDS_SYS* 11.2A< 13.3G>
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GPIO12_AC_DET 13.3D
GPIO13_FBVDDQCTL 13.3G> 17.4D<
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I2CC_SCL 13.3D
I2CC_SCL_R 12.4C< 13.2A< 13.3H> 14.2A<
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I2CC_SDA_R 12.4C<> 13.2A<> 13.3H<> 14.2A<>
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I2CH_SDA 14.4C
I2CS_SCL 13.3D
I2CS_SDA 13.3D
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IFPABRSET 11.2D
IFPABVPROBE 11.1D
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ISL9502_SET2 16.3B
ISL9502_SET3 16.3B
JTAG_TCLK 13.3C
JTAG_TDI 13.3C
JTAG_TDO 13.3C
JTAG_TMS 13.3C
JTAG_TRST 13.3C
LG1 16.2C
LG2 16.3C
LVDSIOVDD_ISOL 11.2B
MIOACAL_PD_VDDQ 15.2B
MIOACAL_PU_GND 15.2B
MIOACLKOUTR* 15.2D
MIOA_VDDQ 15.1B
MIOA_VREF 15.2A
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MIOB_CTL3 15.4F< 18.1A> 18.2C
MIOB_HSYNC 15.4F< 18.2A> 18.4C
M_GPIO8_SLOWDOWN* 13.2C
M_THERM_ALERT* 13.2C
NVVDD 17.1A
NVVDD_SENSE 2.3G> 16.4F<
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NVVDD_VIN 16.1D
NV_PWRGOOD 13.2F< 16.1B> 17.3A<
OCSET 16.3C
PEX1V2 17.1A
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PEX_RST 2.1D
PEX_RX0 2.2E
PEX_RX0* 2.2E
PEX_RX1 2.2E
PEX_RX1* 2.2E
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PEX_TX15_C 2.5B
PEX_TX15_C* 2.5B
PEX_VDD_FB 17.1G
PH1 16.2C
PH2 16.3C
PLL_VDD 10.4C
PWR_SRC 17.1A
RBIAS 16.2B
REFCLK 2.2E
REFCLK* 2.2E

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ROMCS* 14.3C 14.3E
ROM_SCLK 14.3C 14.3E
ROM_SI 14.3E< 14.3E< 18.2A> 18.3C
ROM_SO 14.3C 14.3E
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SLI_D<10> 12.3E 15.2D
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SMB_DAT 12.4C< 13.2F<>
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SNN_CLAMP 13.3D
SNN_DACB_CSYNC 10.2D
SNN_DACC_BLUE 10.4D
SNN_DACC_GREEN 10.3D
SNN_DACC_RED 10.3D
SNN_DACC_RSET 10.3C
SNN_DACC_VREF 10.3C
SNN_FB2 16.3C
SNN_FBA0_NC1 4.2B
SNN_FBA0_NC2 5.2B
SNN_FBA0_NC3 5.2B
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SNN_FBA1_NC2 5.2E
SNN_FBA1_NC3 5.2E
SNN_FBA_CMD14 3.3E
SNN_FBA_CMD26 3.3E
SNN_FBA_CMD28 3.4E
SNN_FBA_NC1_D31 3.4E
SNN_FBA_NC2_D32 3.4E
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SNN_FBC0_NC2 8.2B
SNN_FBC0_NC3 8.2B
SNN_FBC1_NC1 7.2E
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SNN_FBC1_NC3 8.2E
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SNN_FBVTT_AB23 6.1E
SNN_FBVTT_H16 6.1E
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SNN_FBVTT_M23 6.1E
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SNN_FBVTT_U25 6.1E
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SNN_G3_RFU2 15.4F
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SNN_G3_RFU10 14.4A
SNN_G3_RFU11 14.4A
SNN_G3_RFU12 14.4A
SNN_G3_RFU13 14.4A
SNN_G3_RFU14 14.4A
SNN_G3_RFU15 14.4A
SNN_G3_RFU16 14.4A

SNN_GPIO14 13.3D
SNN_HDCP_ROM 14.4D
SNN_ISL9502_NC1 16.4C
SNN_ISL9502_NC2 16.4C
SNN_MIOBCAL_PD_VDD 15.4D
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SNN_MIOBCAL_PU_GND 15.4D
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SNN_MIOB_CLKOUT* 15.4F
SNN_MIOB_DE 15.4F
SNN_MIOB_VREF 15.4D
SNN_MIOB_VSYNC 15.4F
SNN_MSTRAPSEL0 14.3A
SNN_MSTRAPSEL1 14.3A
SNN_MSTRAPSEL2 14.3A
SNN_MSTRAPSEL3 14.4A
SNN_NTC 16.2B
SNN_POK 17.1F
SNN_RFU 15.2D
SNN_RFU1 2.1D
SNN_RFU2 2.1D
SNN_STEREO 14.4C
SNN_STRAP 14.3A
SNN_THERMAL 13.3C
SNN_VRHOT* 16.3B
SNUB1 16.2F
SNUB2 16.4F
SOFT 16.3B
SPDIF 2.5F
SPDIF_C 2.5H< 12.4C>
SSFOUT 10.4B< 14.1D>
SS_OUT 14.3C
SS_REF 14.2C
TESTMCLK 14.4C
TESTMODE 14.4C
THERM 13.3C
THERM* 13.3C
THERM_ALERT* 12.4C< 13.2H>
THERM_SCL 13.2C
THERM_SDA 13.2C
THERM_VDD 13.1D
TMDSIOVDD_AB_EN* 11.2B
TMDSIOVDD_C 11.4C
TMDSIOVDD_C_EN* 11.4B
TMDSIOVDD_D 11.5C
TMDSIOVDD_D_EN 11.5C
TMDSIOVDD_D_EN* 11.5B
TMDS_LVDS_IOVDD 11.2B
UG1 16.2C
UG1_R 16.2E
UG2 16.2C
UG2_R 16.3E
VDIFF 16.2B
VDIFF_R 16.2A
VID0 16.3B
VID4 16.3B
VID5 16.3B
VO 16.3C
VSEN 16.4C
VSUM 16.3C 16.3F 16.4G
VW 16.2B
XTALIN 10.5C
XTALOUT 10.5D
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C2 [17.3H]
C3 [17.3G]
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