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	2. Add AC Coupling capacitors
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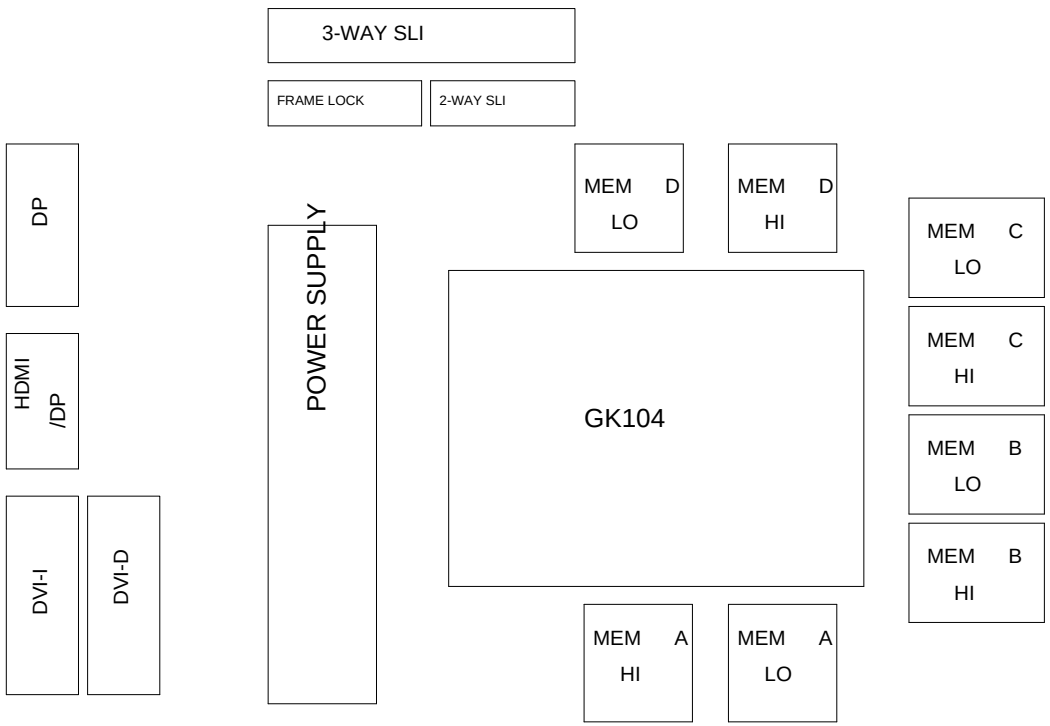
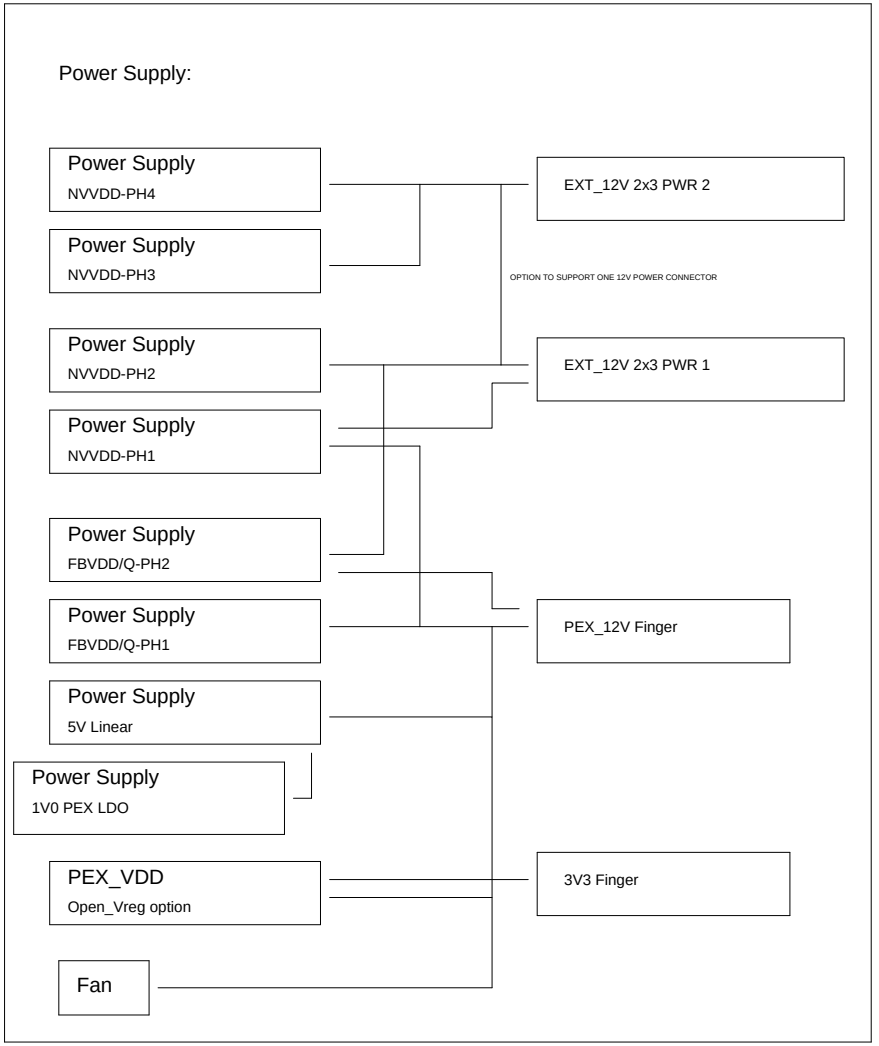
Page2: Block Diagram



Power Supply:



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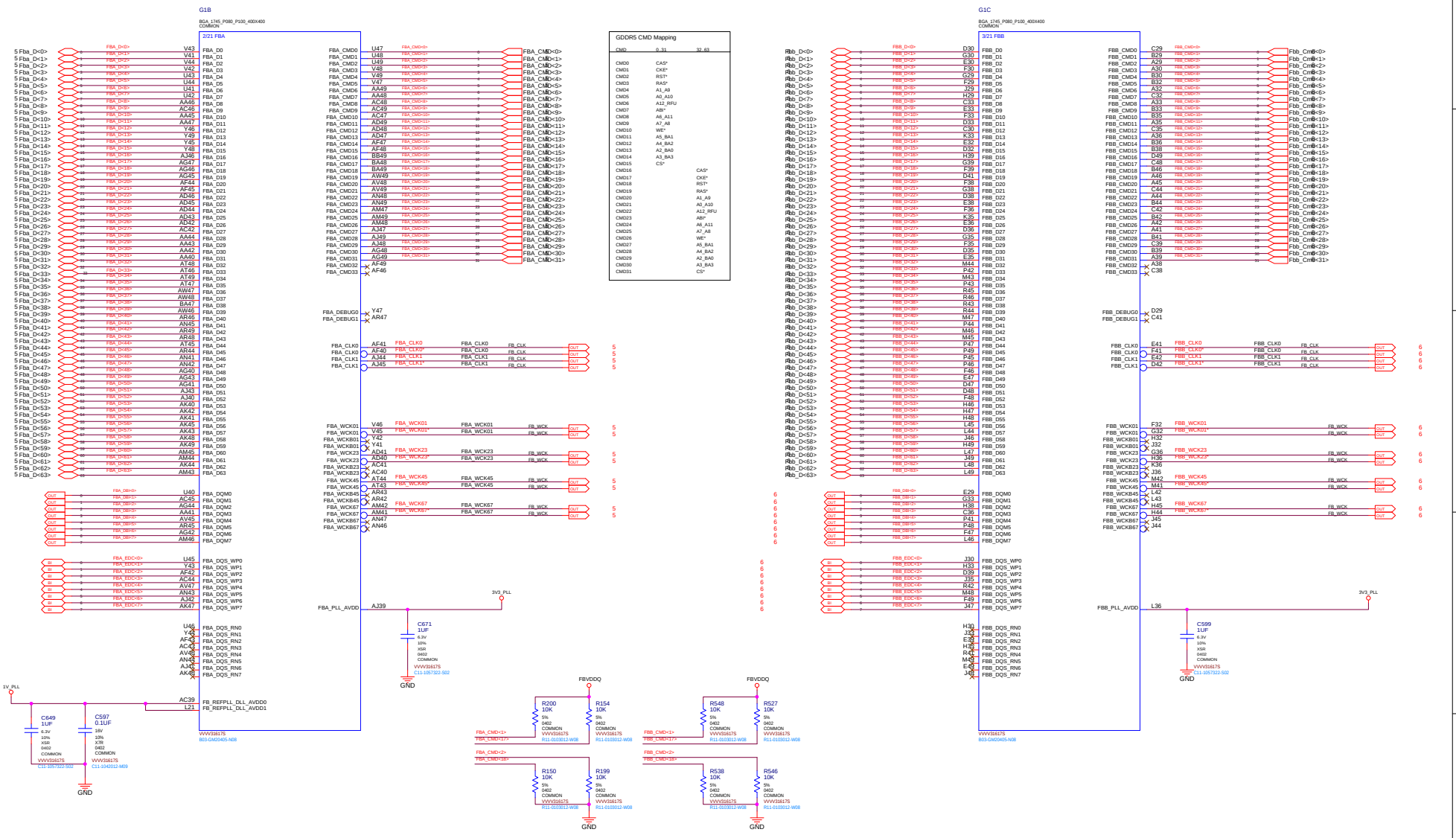
Page3: PCI Express

Page4: MEMORY: GPU Partition A/B



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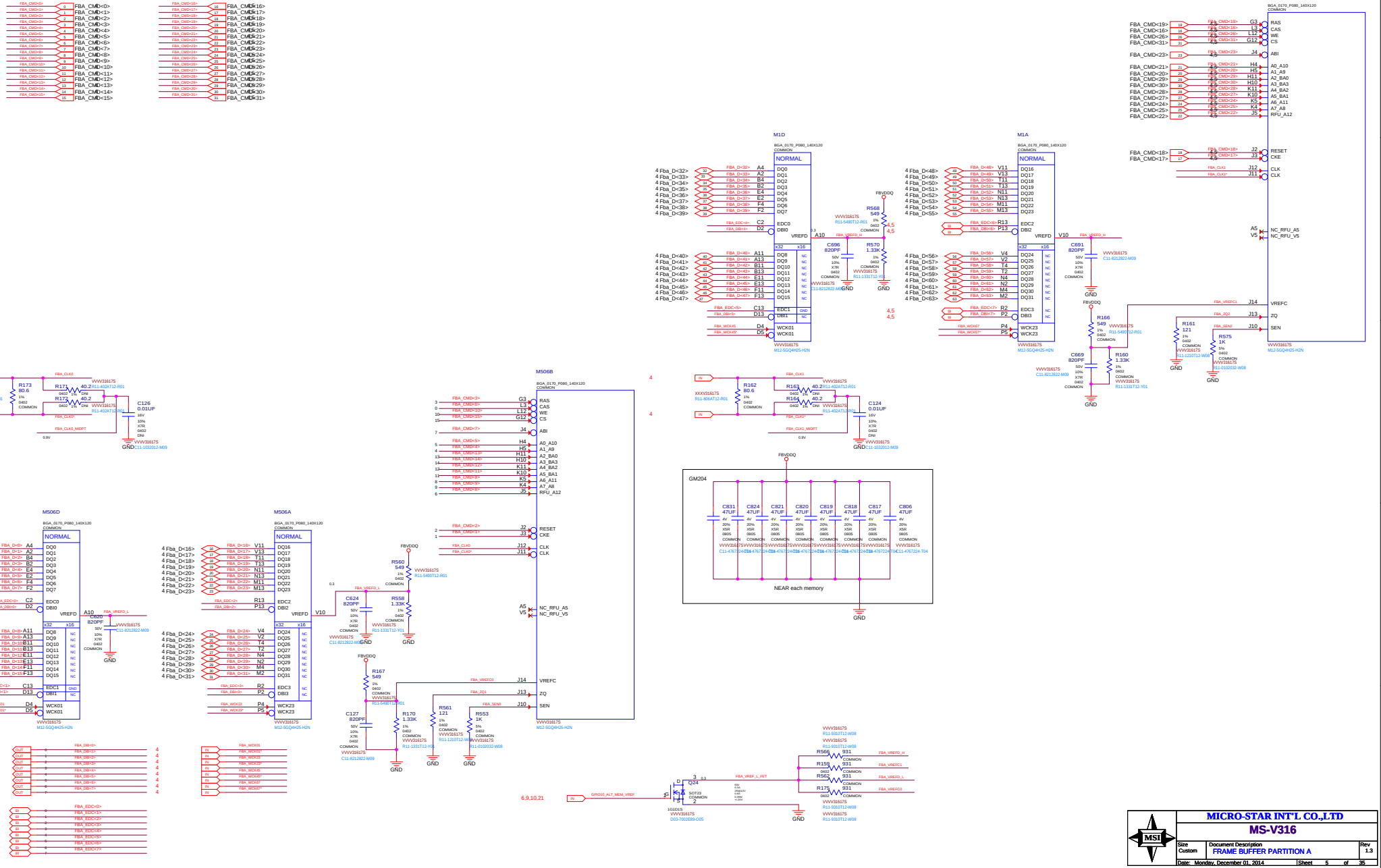
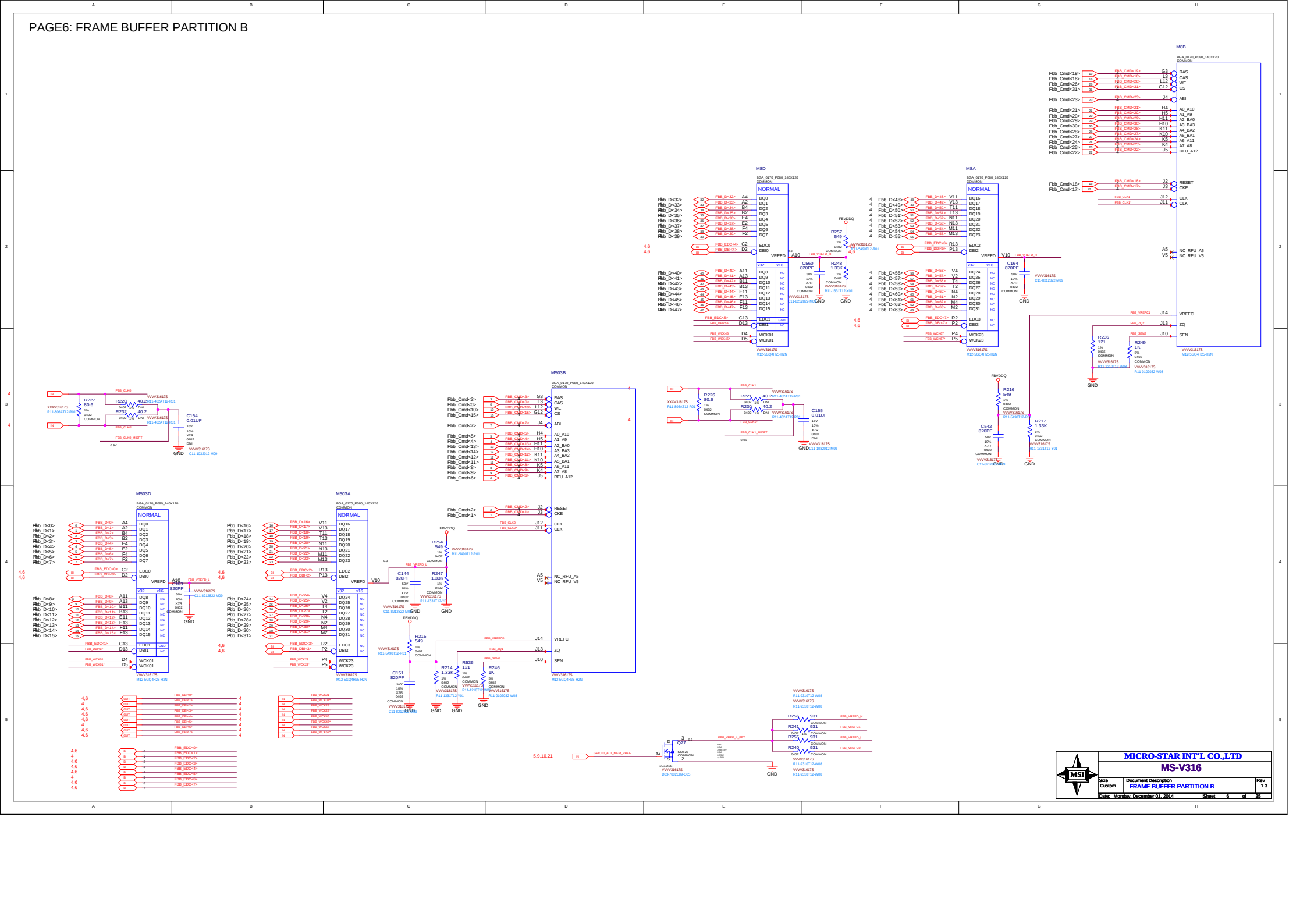
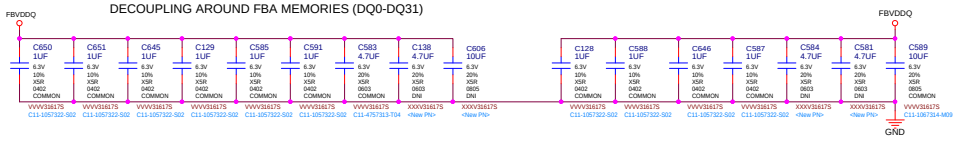
PAGE5: FRAME BUFFER PARTITION A

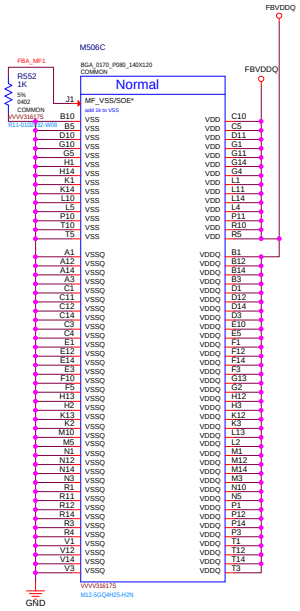


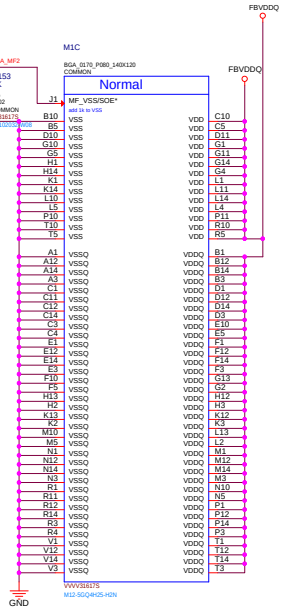
PAGE6: FRAME BUFFER PARTITION B

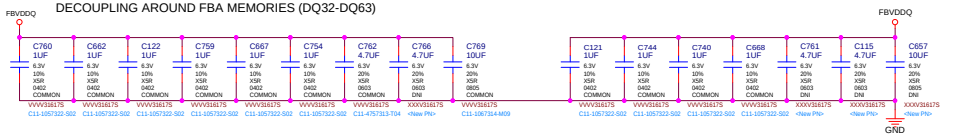


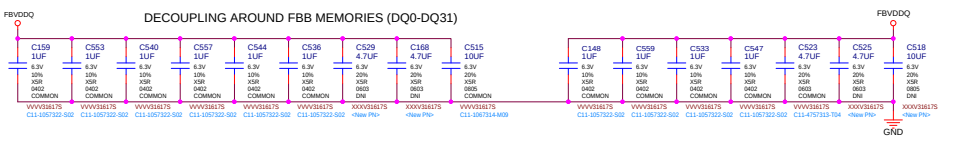
PAGE7: FRAME BUFFER PARTITION A/B DECOUPLING

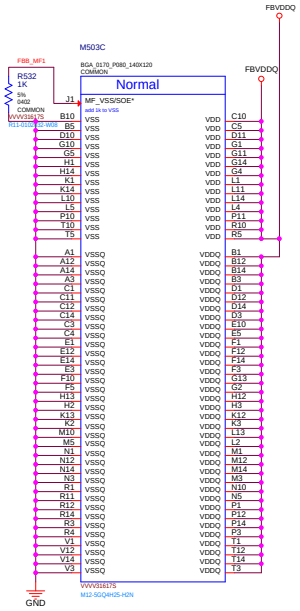


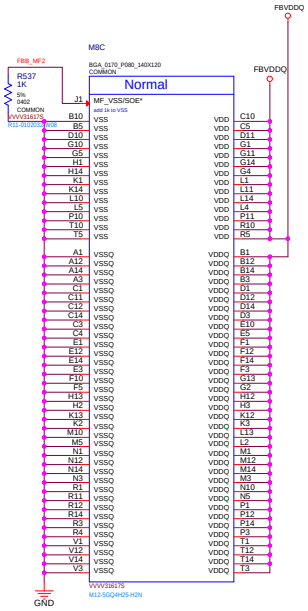


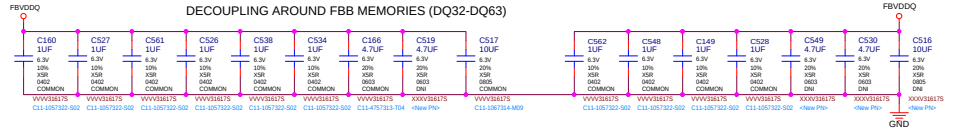












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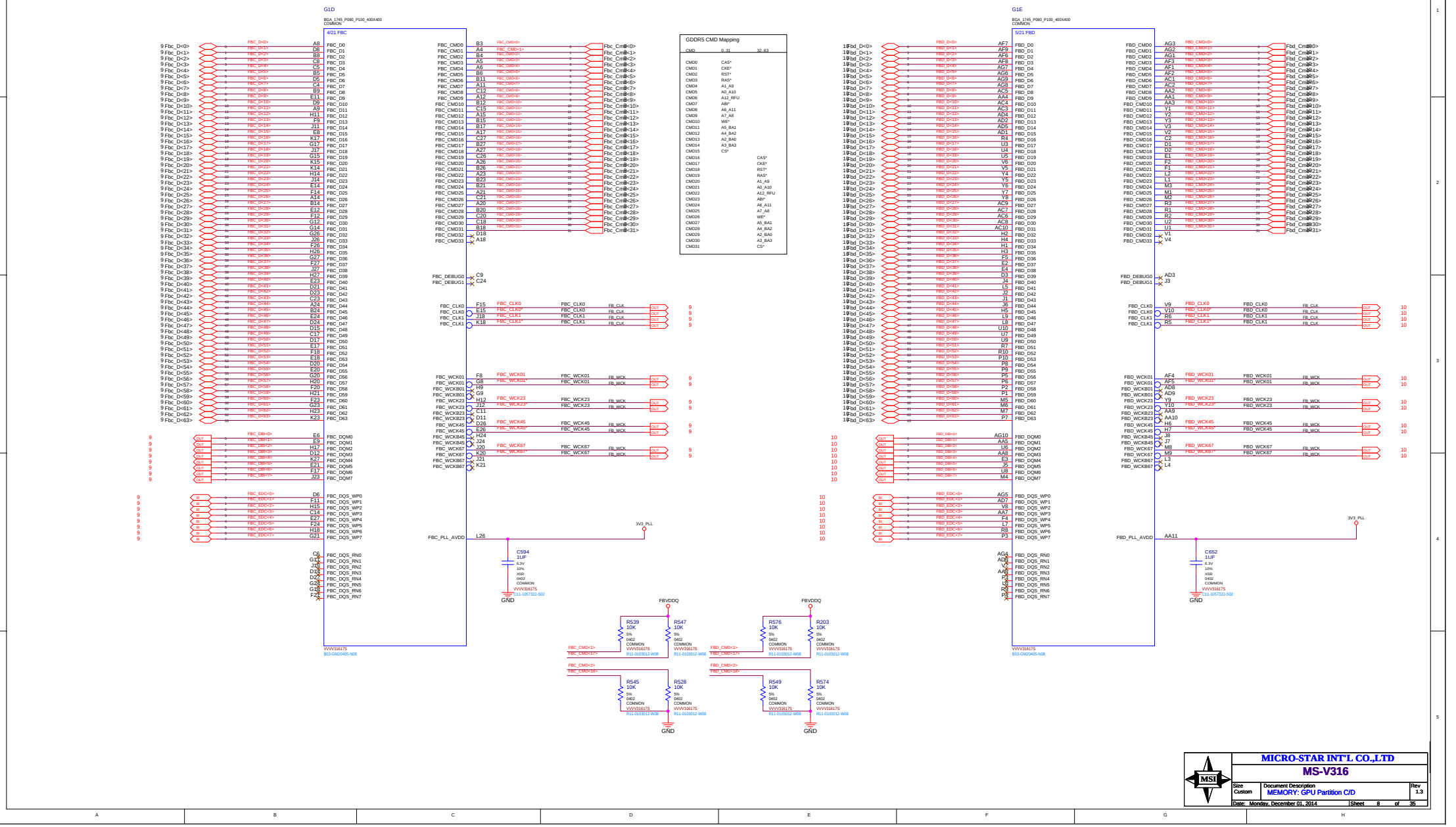
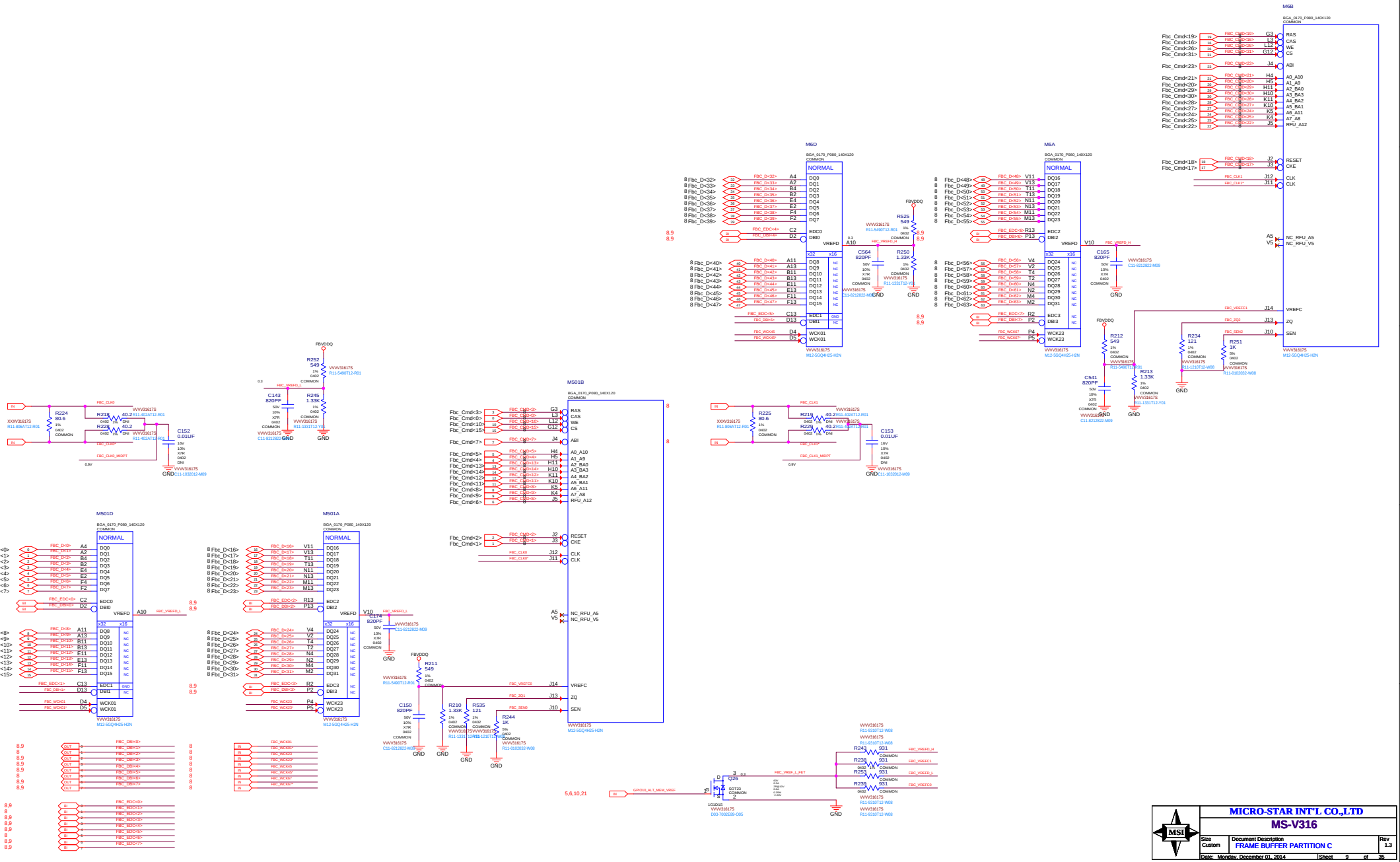
Page8: MEMORY: GPU Partition C/D



PAGE9: FRAME BUFFER PARTITION C



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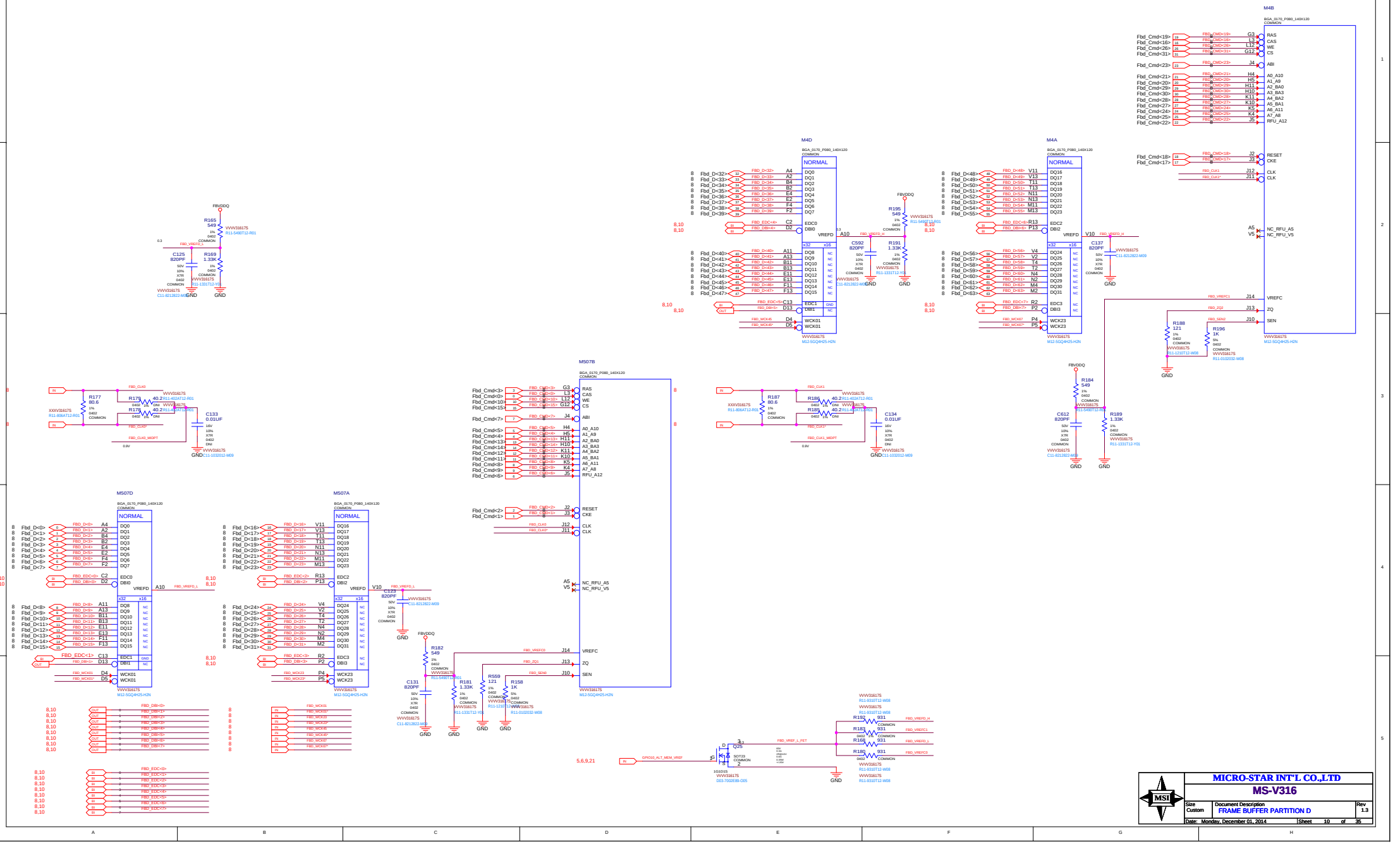
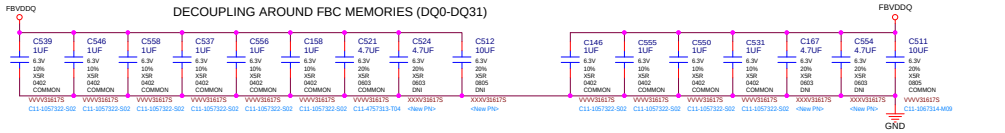
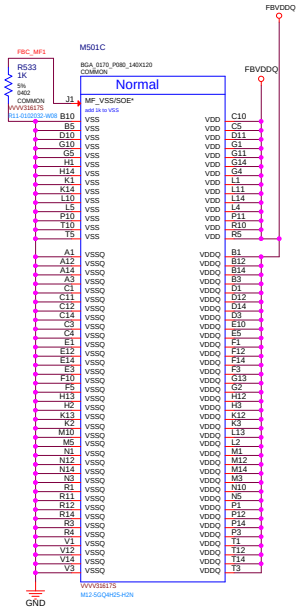
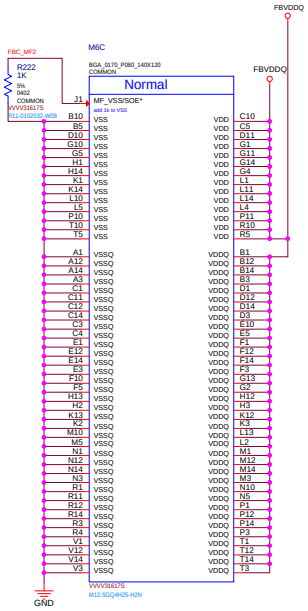
PAGE10: FRAME BUFFER PARTITION D

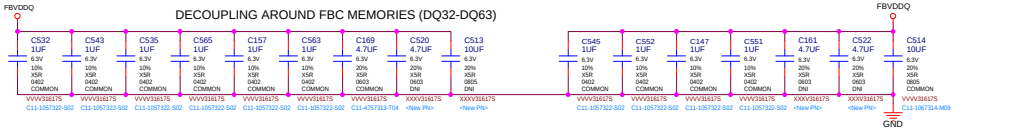


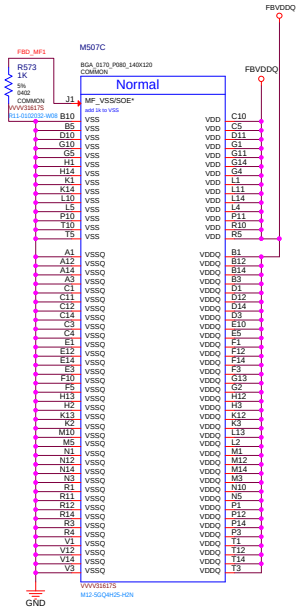
PAGE11: FRAME BUFFER PARTITION C/D DECOUPLING

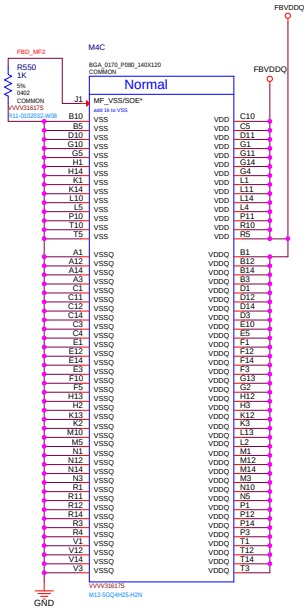


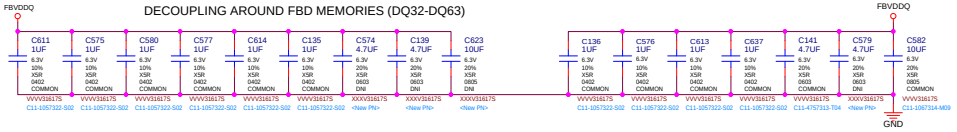












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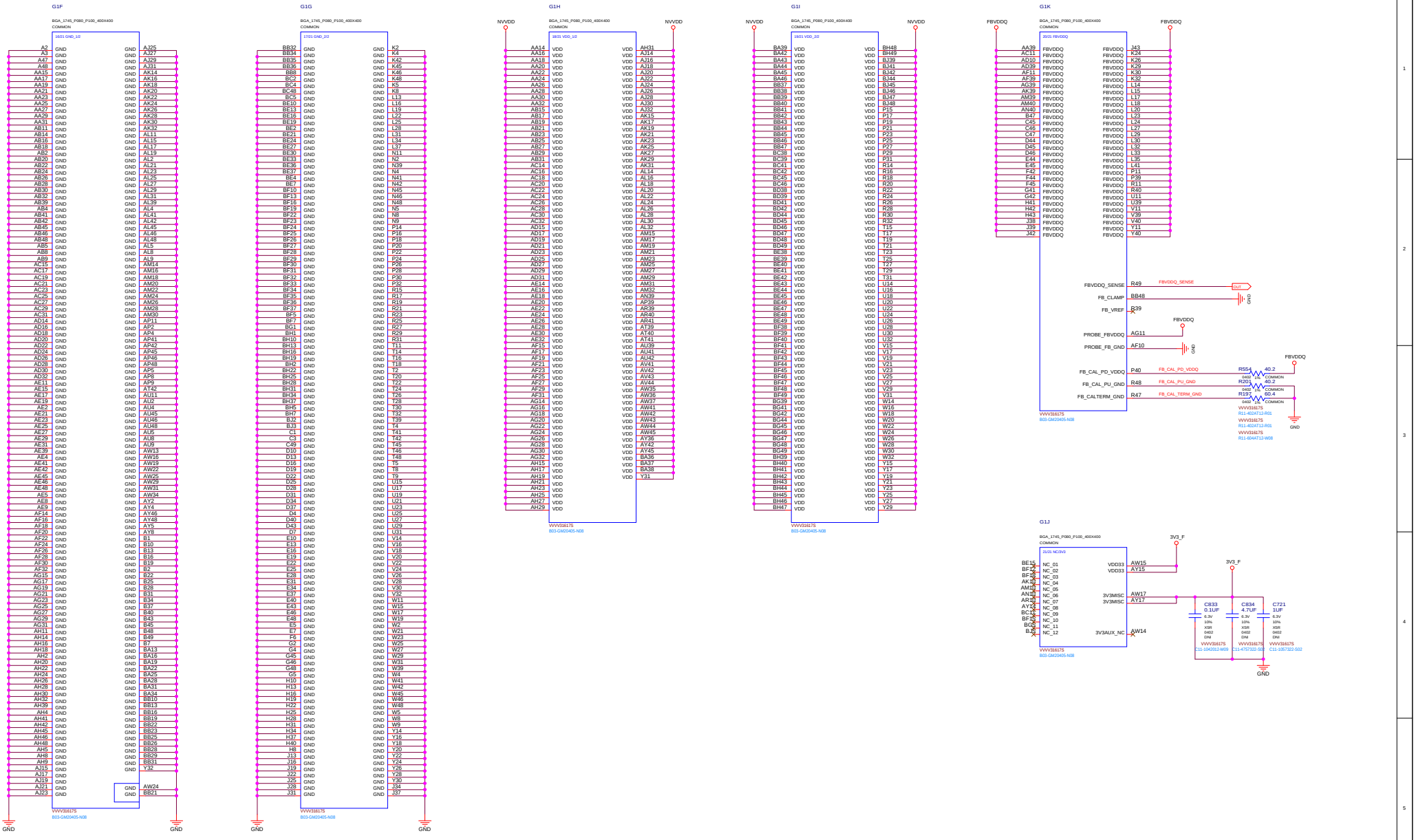
Page12: GPU PWR and GND



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Page13: GPU Decoupling

Based on GB2-X GDDR5 FBVDDQ Decap Guideline

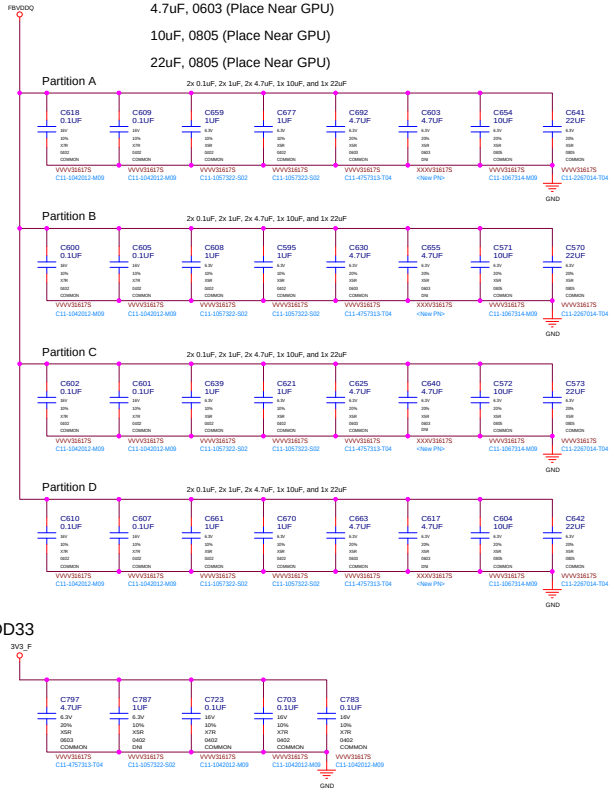
FBVDDQ

0.1uF, 0.47uF & 1uF, 0402 (Place Under GPU)

4.7uF, 0603 (Place Near GPU)

10uF, 0805 (Place Near GPU)

22uF, 0805 (Place Near GPU)



VDD33

NVVDD Decoupling caps. Place under GPU.

NVVDD

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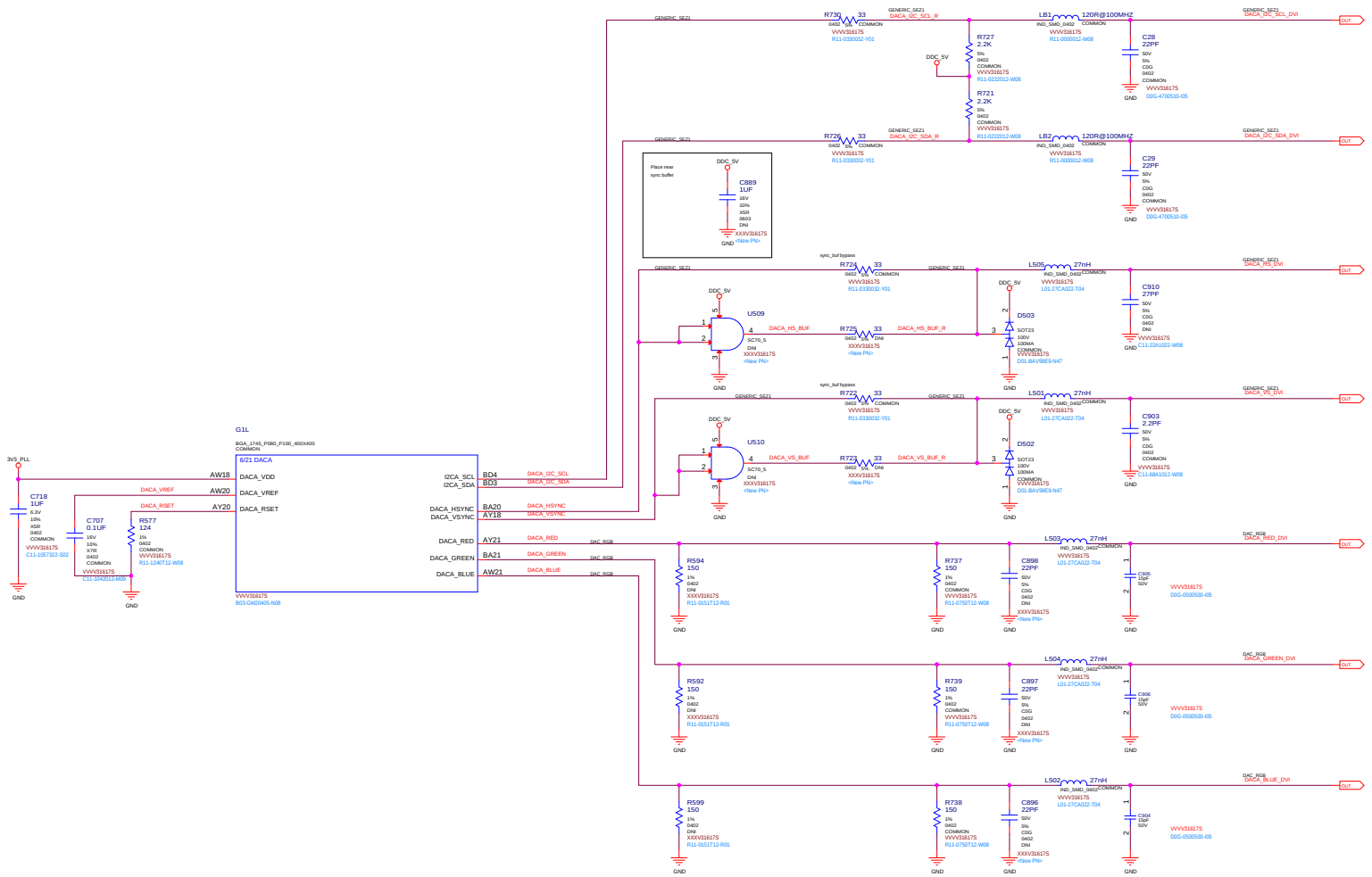
Page14: DACA Interface



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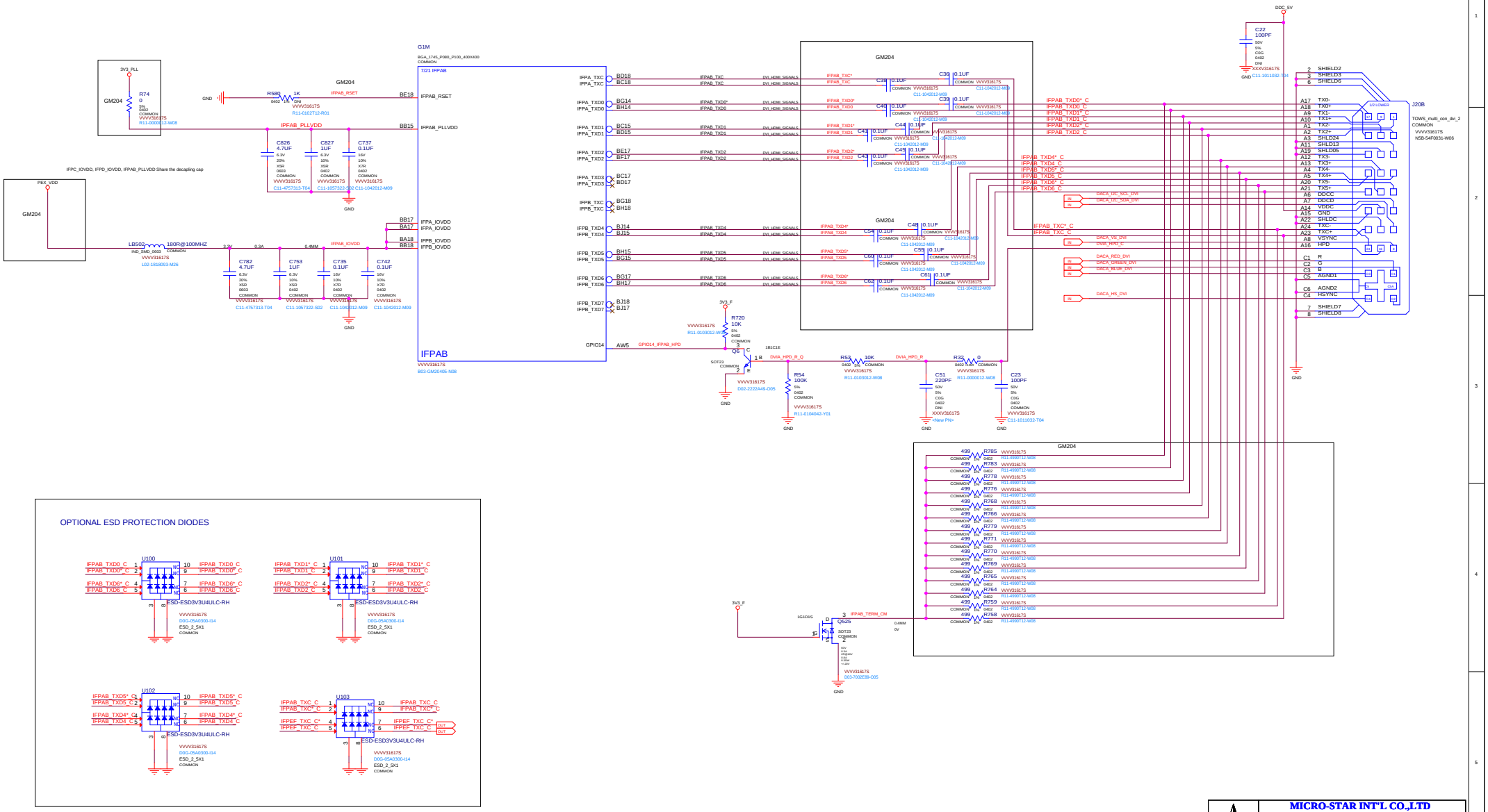
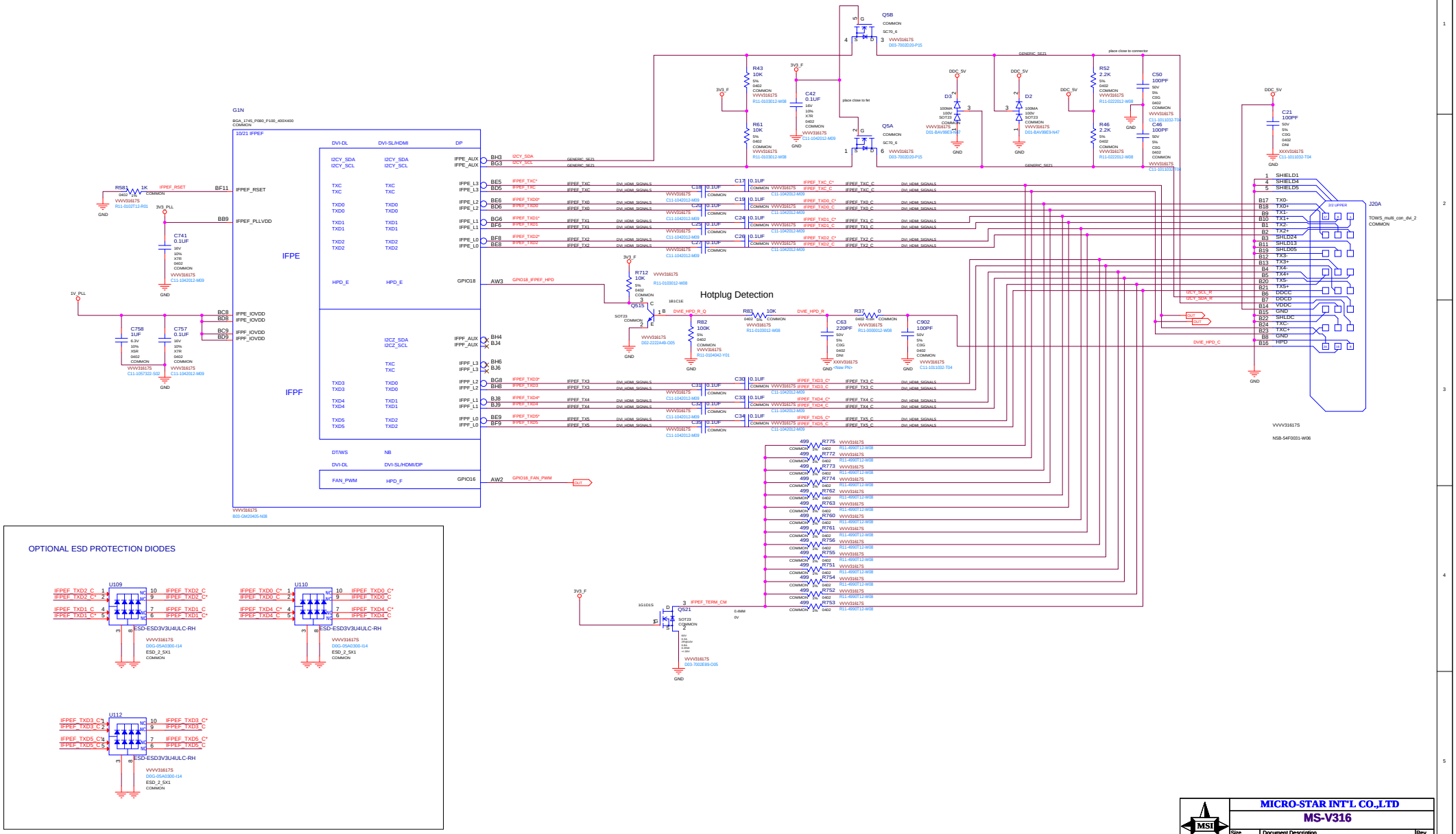
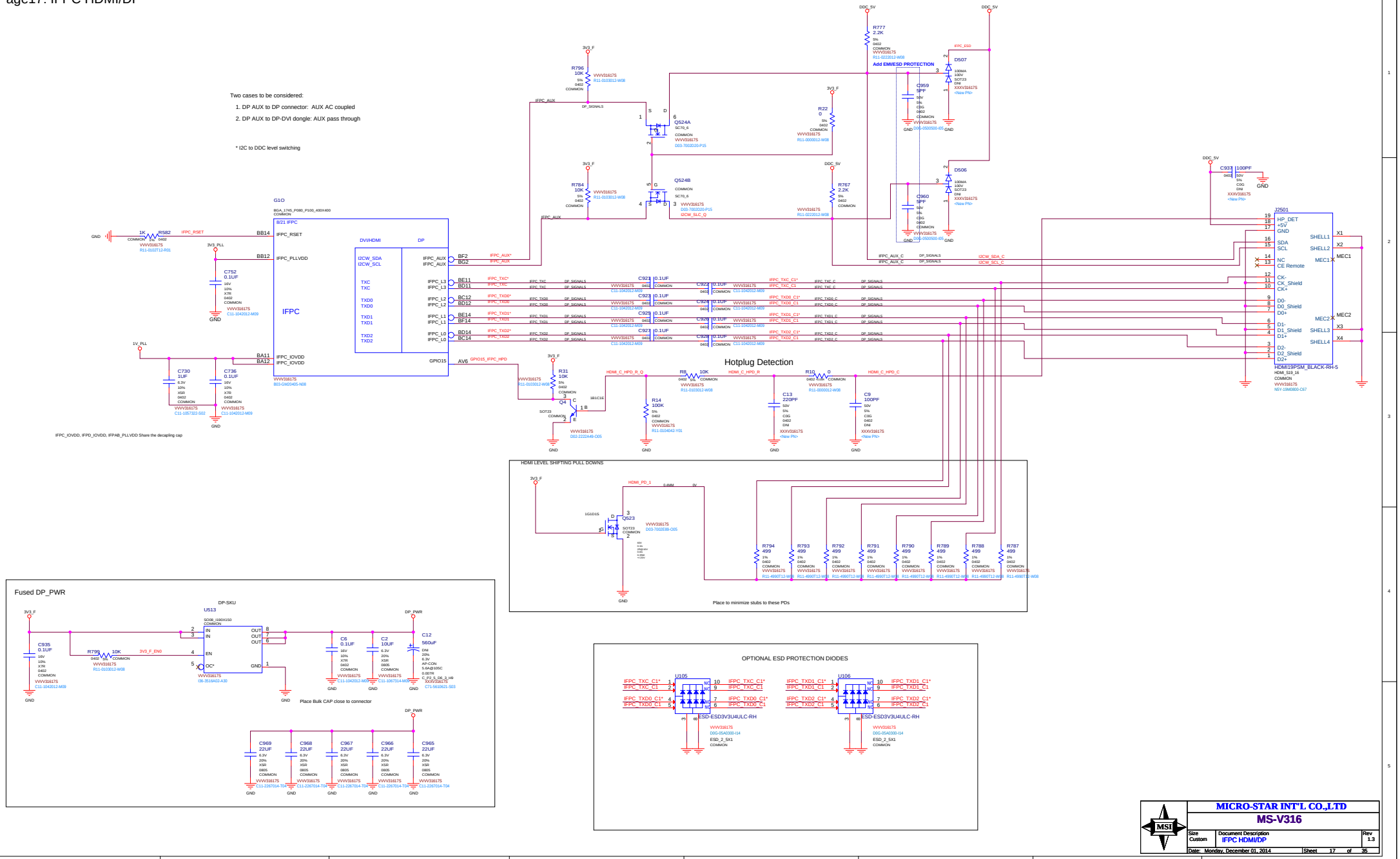
Page15: IFPAB DVI-I-DL



Page16: IFPEF DVI-D-DL



Page17: IFPC HDMI/DP



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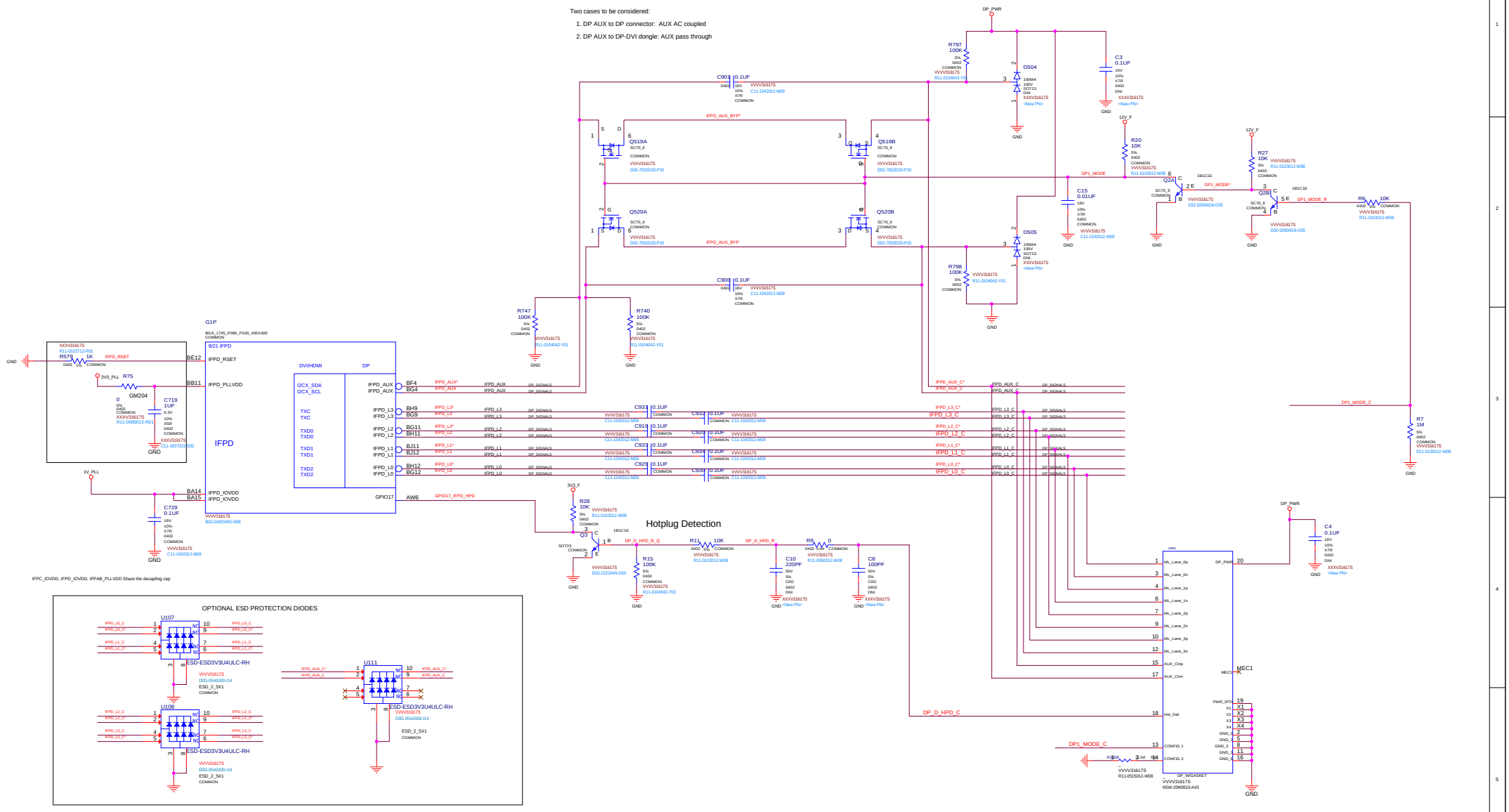
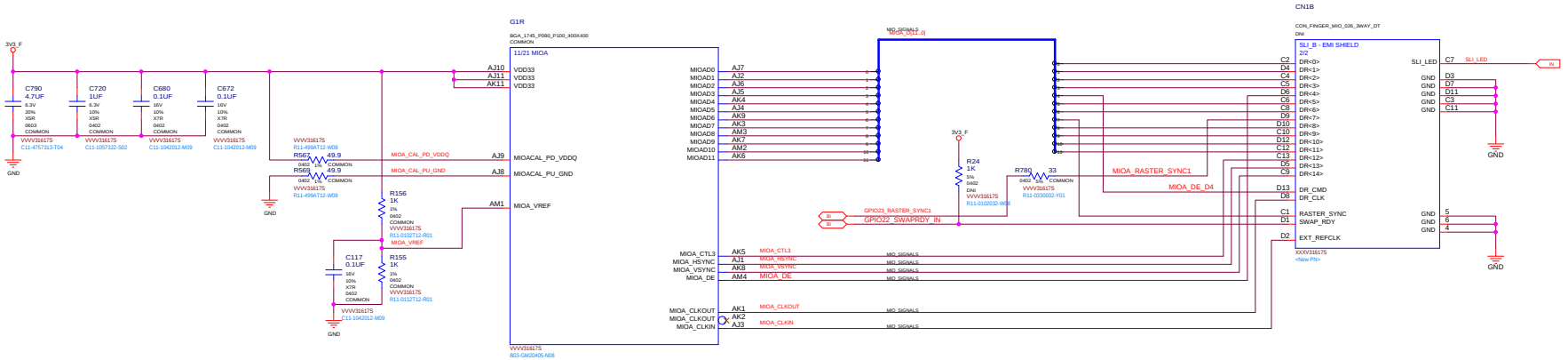
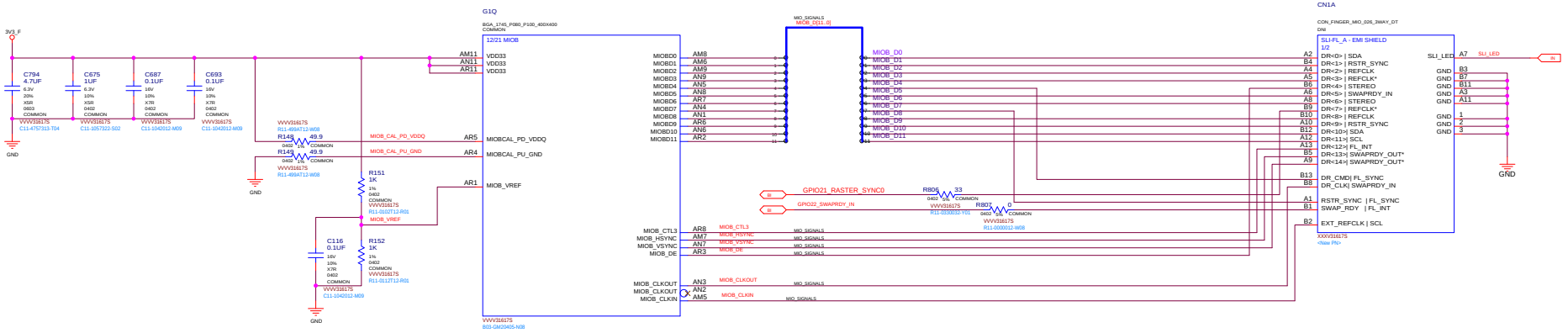
Page18: IFPD DP



Page19: MIOA/B Interface and Frame Lock





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Page20: Stereo Connector

remove

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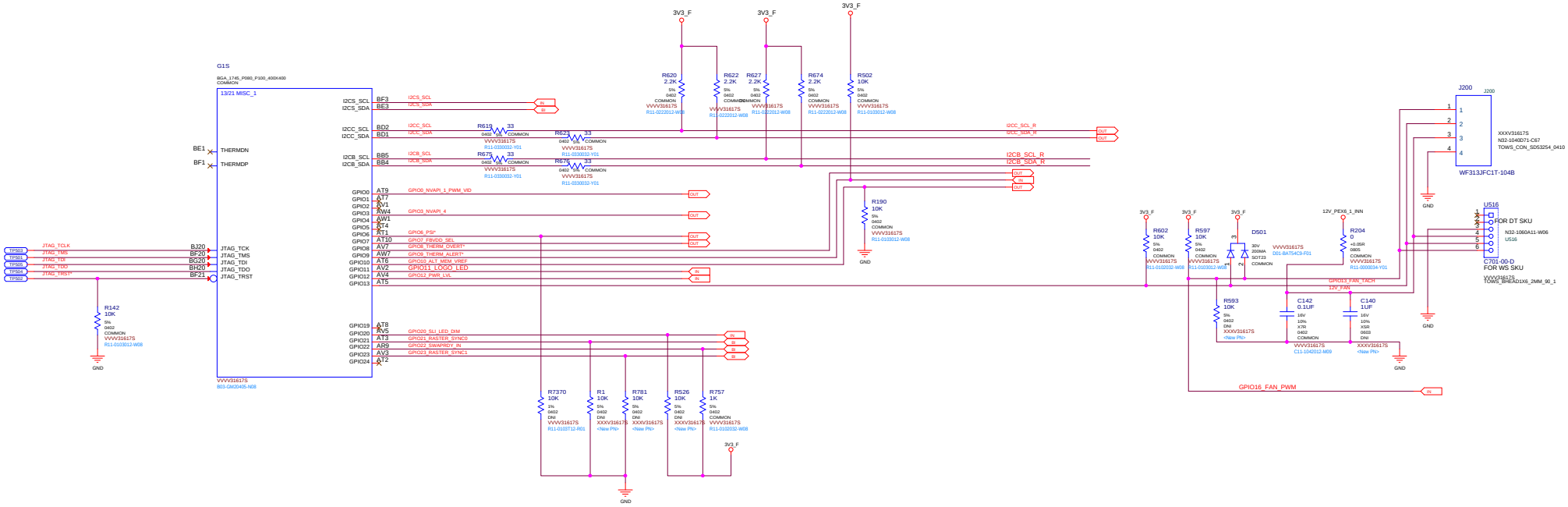
Page21: MISC1: Fan, Thermal, JTAG, GPIO



Page22: MISC2: ROM, XTAL, Straps

STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	1001 - (0x1189)*	10K PU -325 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		
ROM_SI	RAMCFG[0]*	0*	
	RAMCFG[1]*	1*	35K PD*
	RAMCFG[2]*	1*	
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	30k PD*
	FB[0]_APERTURE_SIZE*	1* For 128MB*	
	FB[1]_APERTURE_SIZE*	0* For 128MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0* DISABLE*	
	PCI_DEVID_EXT[5]*	0* For 0x1189*	25K PD*
	SUB_VENDOR*	1* Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0* For 0x1189*	

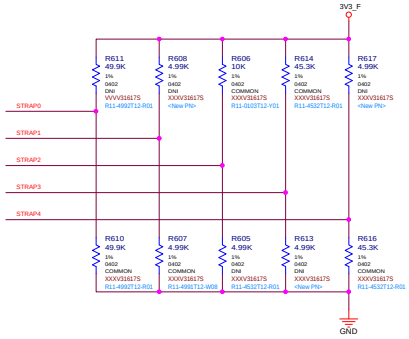
64Mx32 256 bit hynix for SKUS primary memory

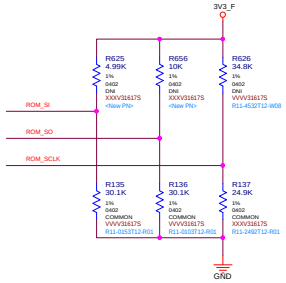
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

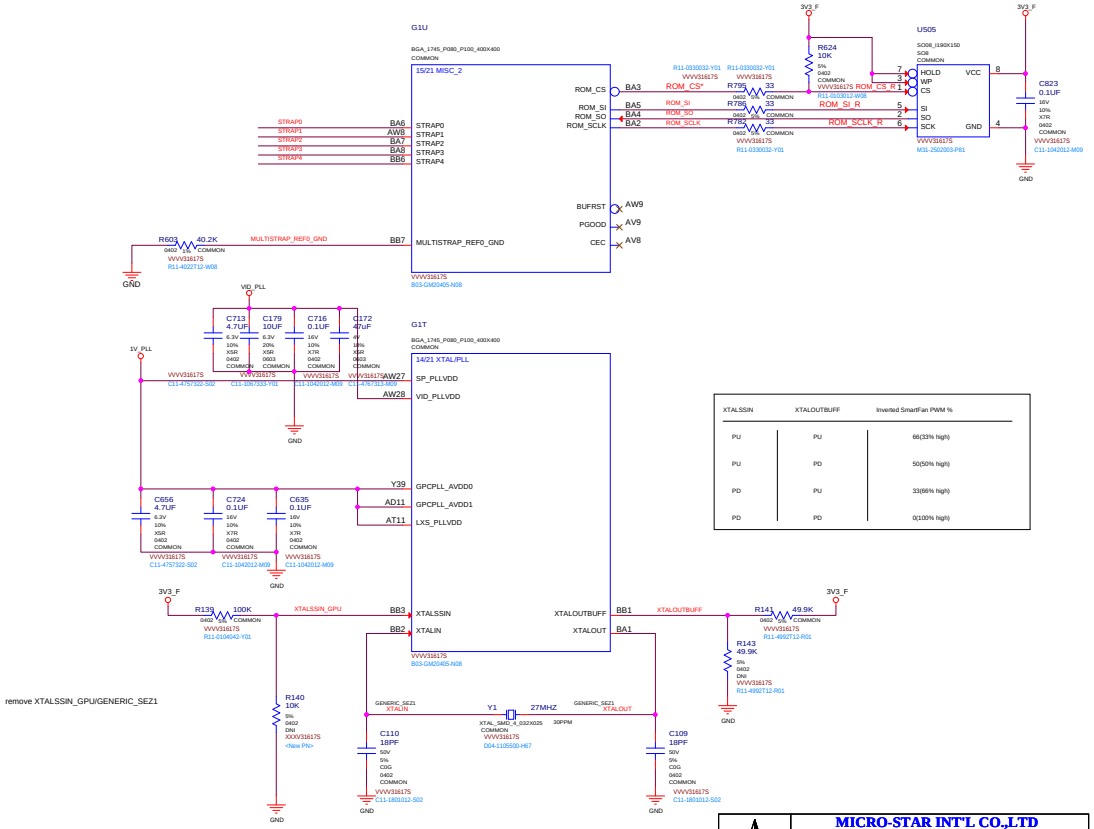
X32 MODE 256bit

CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	32Mx32	256-bit	Elpida
0010	32Mx32	256-bit	Hynix
0011	32Mx32	256-bit	Samsung
0100	Reserved		
0101	64Mx32	256-bit	Elpida
0110	64Mx32	256-bit	Hynix
0111	64Mx32	256-bit	Samsung

MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND







XTALSSIN	XTALOUTBUFF	Inverted SmartFan PWM %
PU	PU	66(33% high)
PU	PD	50(50% high)
PD	PU	33(66% high)
PD	PD	0(100% high)

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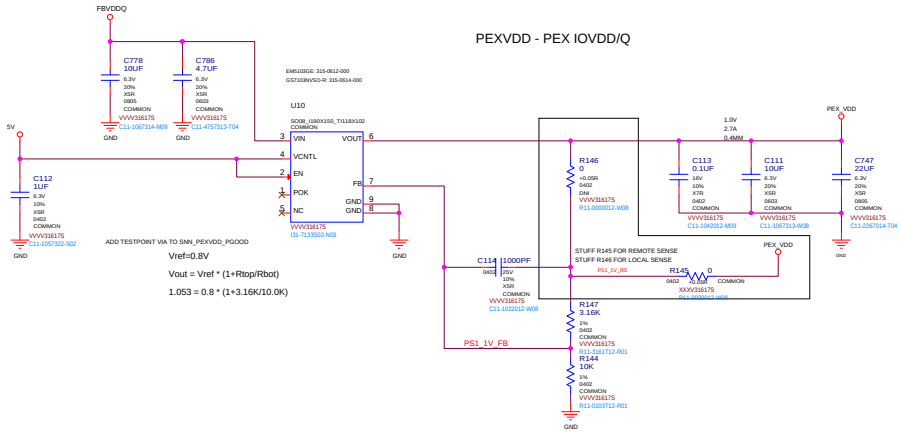
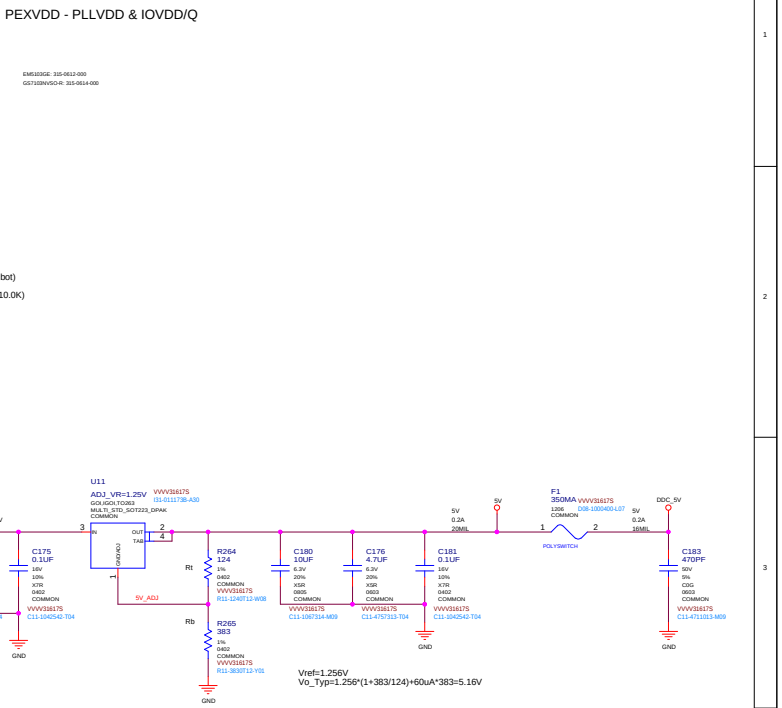
Page23: PS: 5V, PEX_VDD

PEXVDD - PEX IOVDD/Q



PEXVDD - PLLVDD & IOVDD/Q



PEXVDD - PLLVDD & IOVDD/Q

REMOVE PEXVDD PWM

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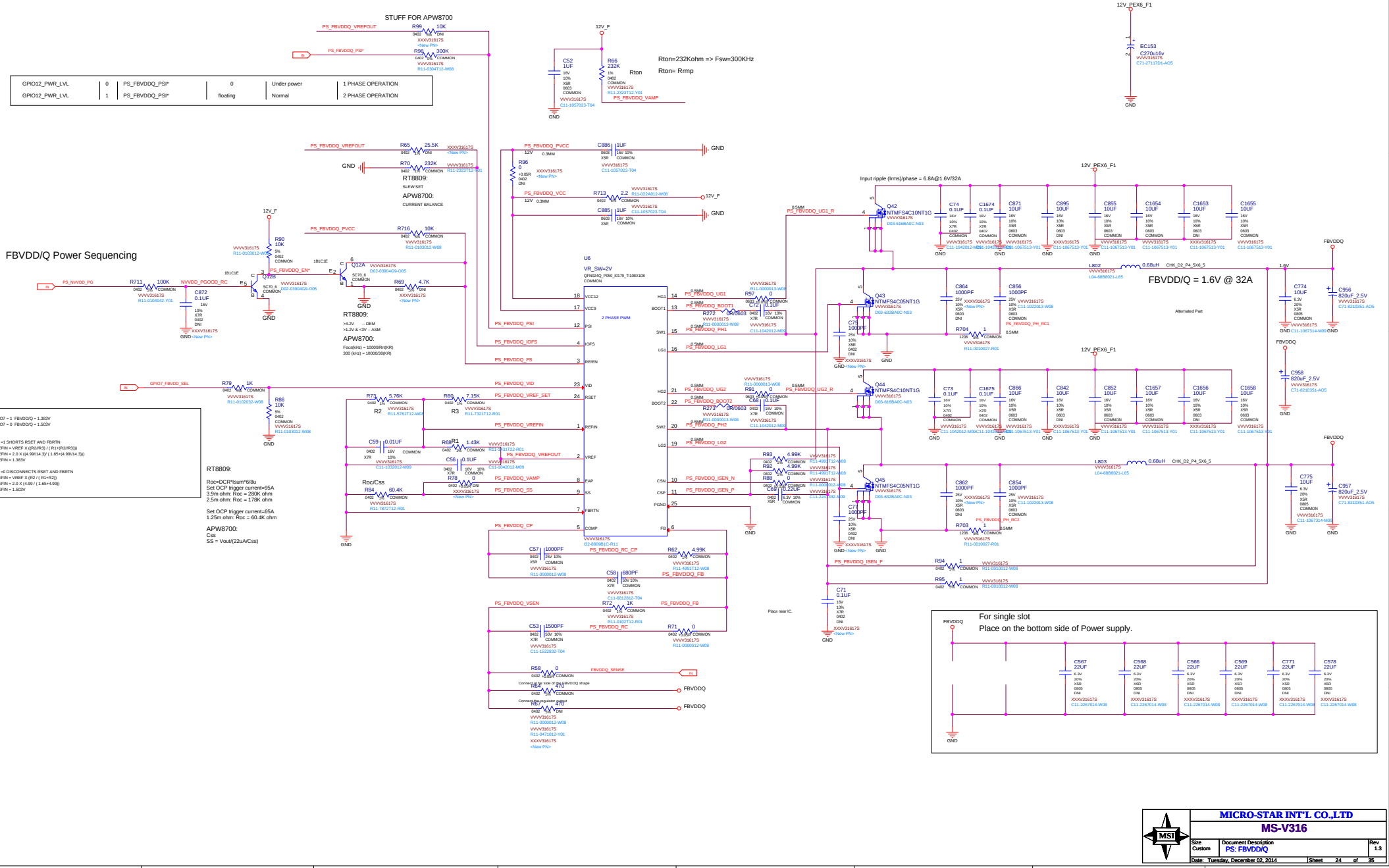
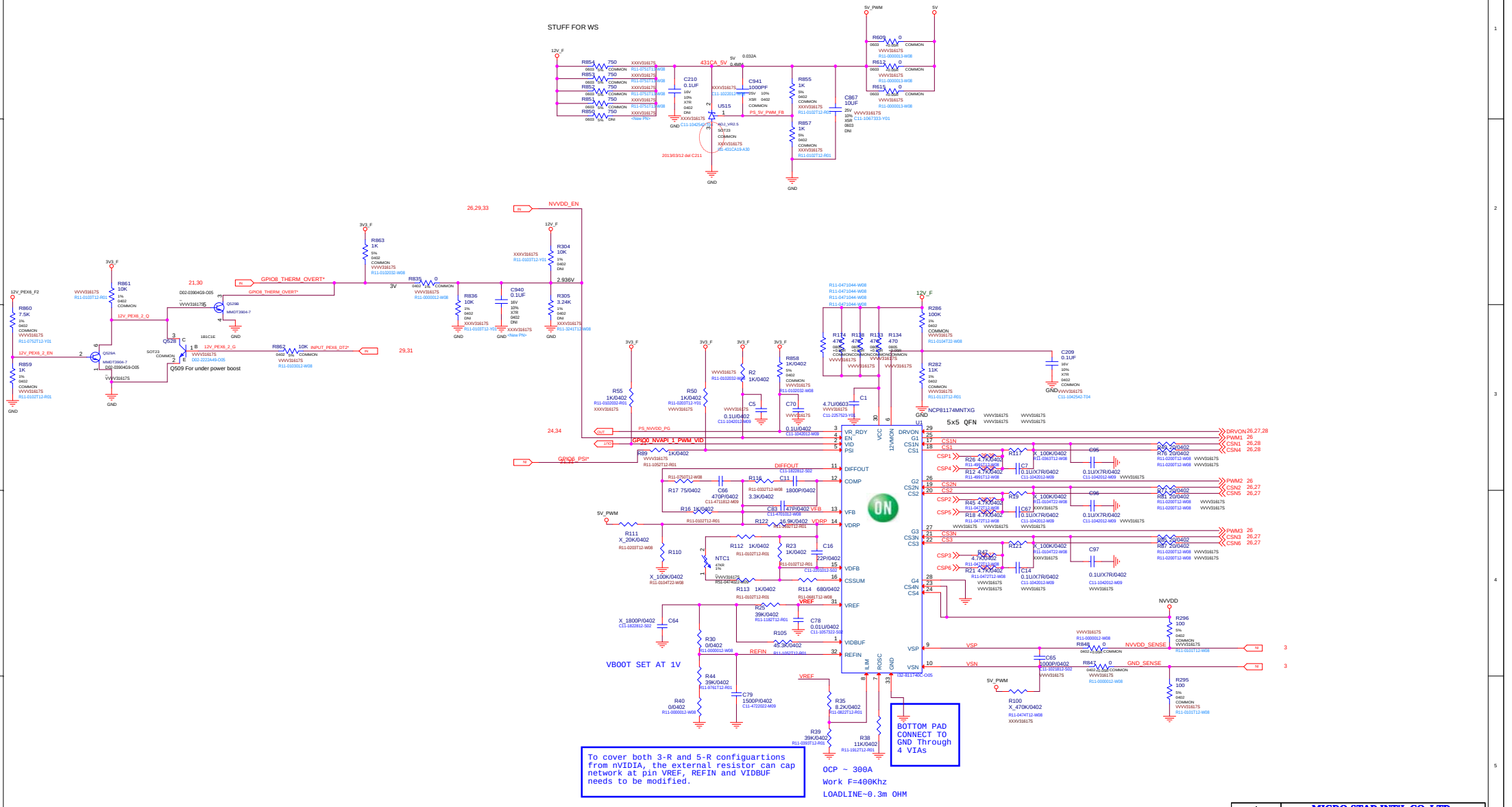
Page24: PS: FBVDD/Q



Page25: NVVDD Controller NCP81174



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Custom	NVVDD Controller	1.3

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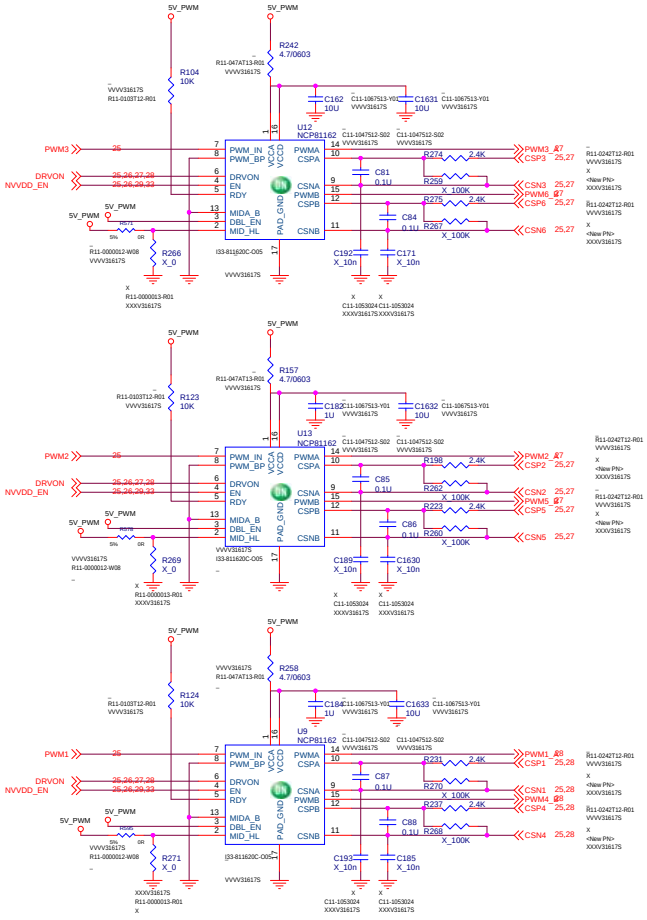
Page26: NVVDD PHASE DOUBLERS



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Size: Custom	Document Description: NVVDD PHASE DOUBLERS		Rev: 1.3
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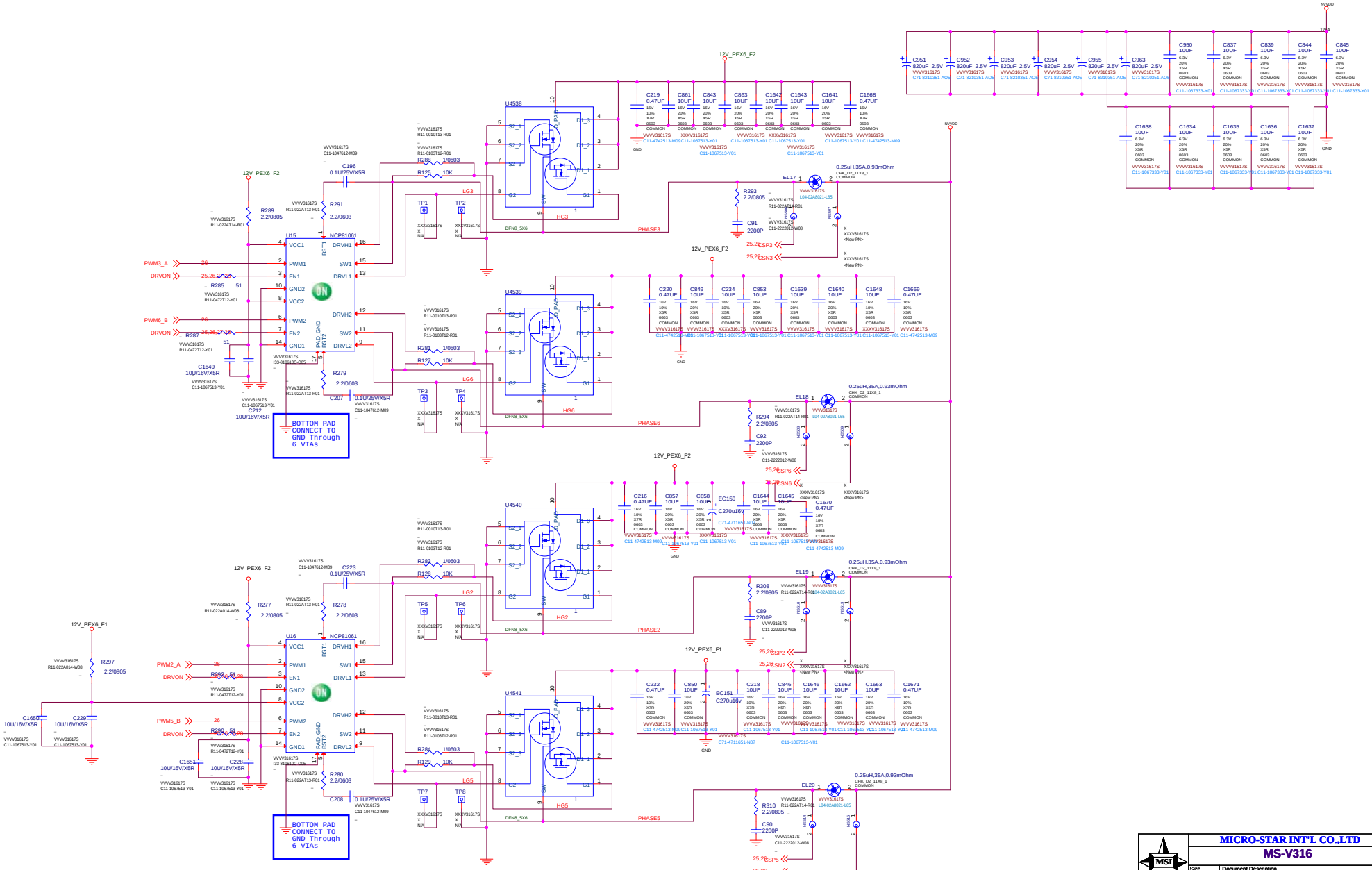
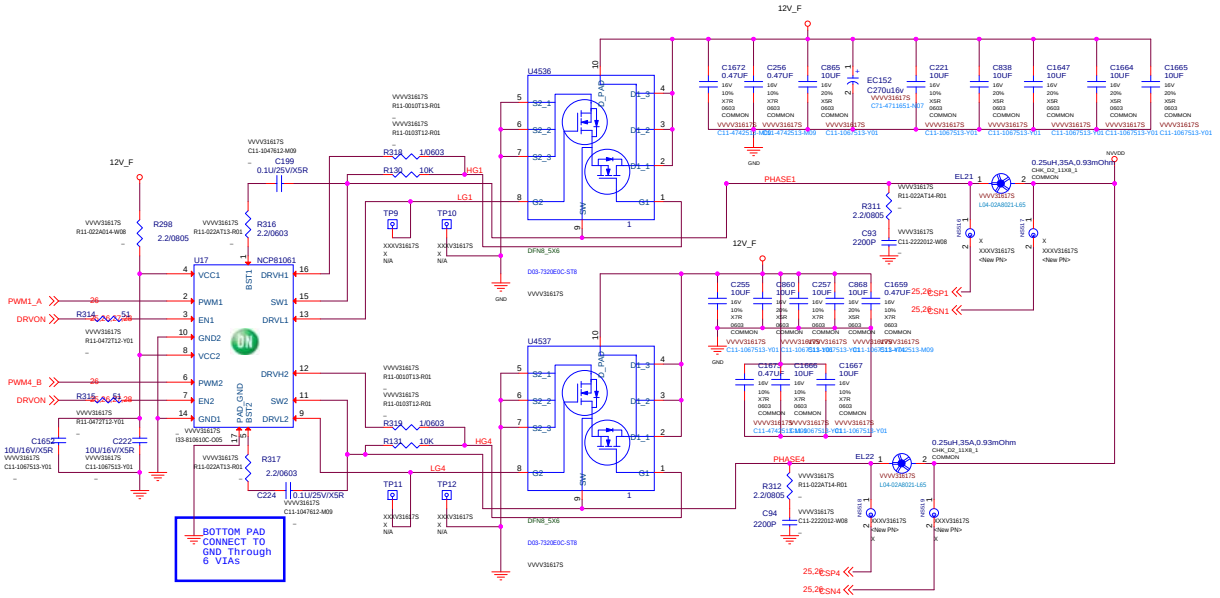
Page27: NVVDD Phase 2 & 3 & 5 & 6



Page28: NVVDD Phase 1 & 4



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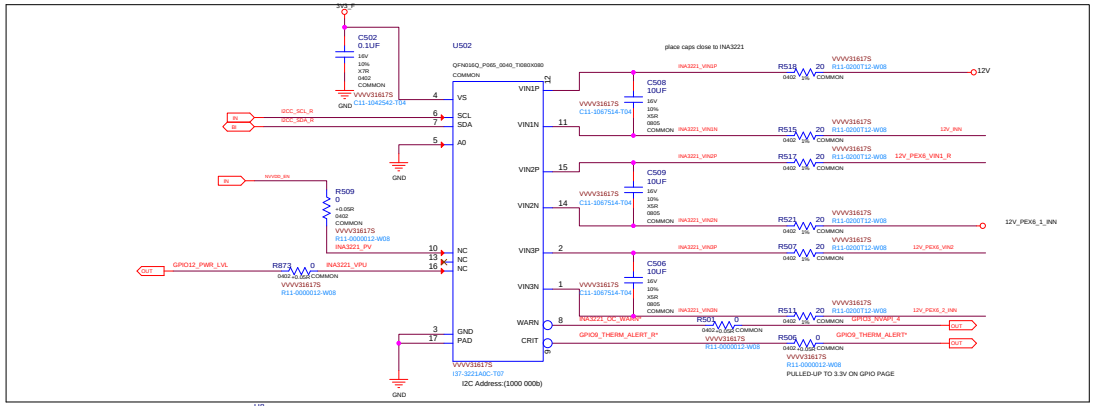
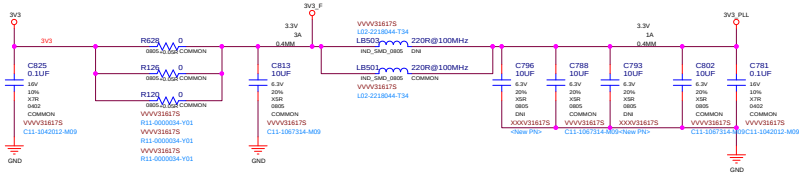
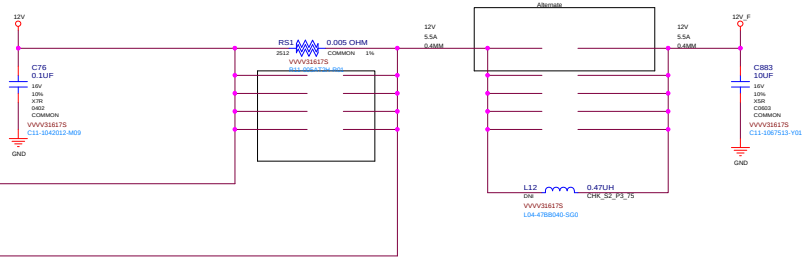
Page29: PS: Inputs, Filtering, and Monitoring

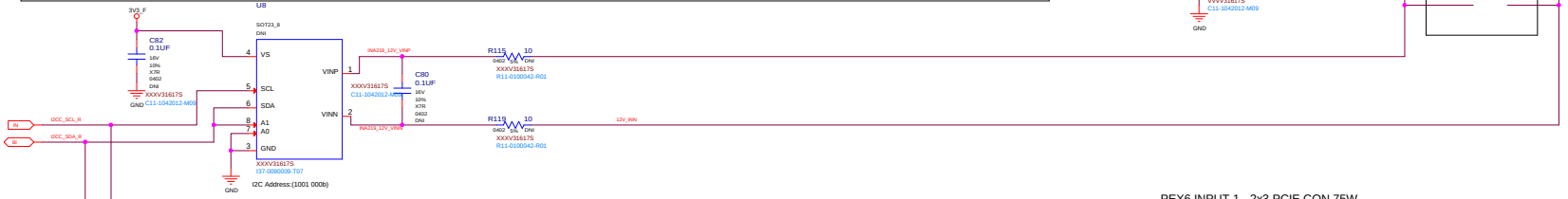


PEX 3V3 INPUT - 10W

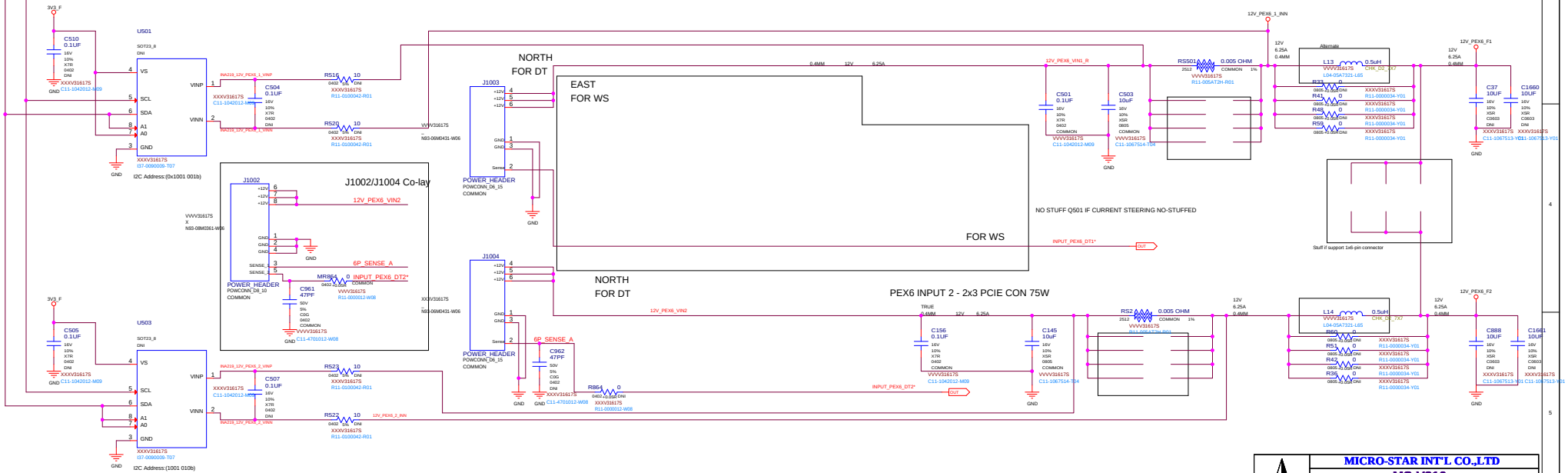


PEX_12V INPUT - 66W





PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX6 INPUT 2 - 2x3 PCIE CON 75W

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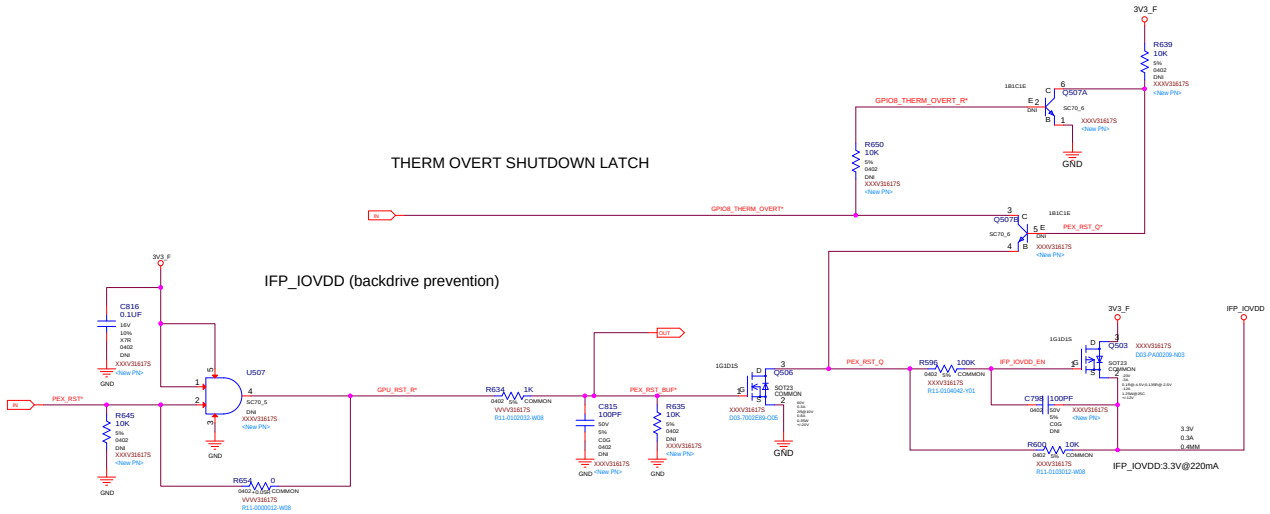

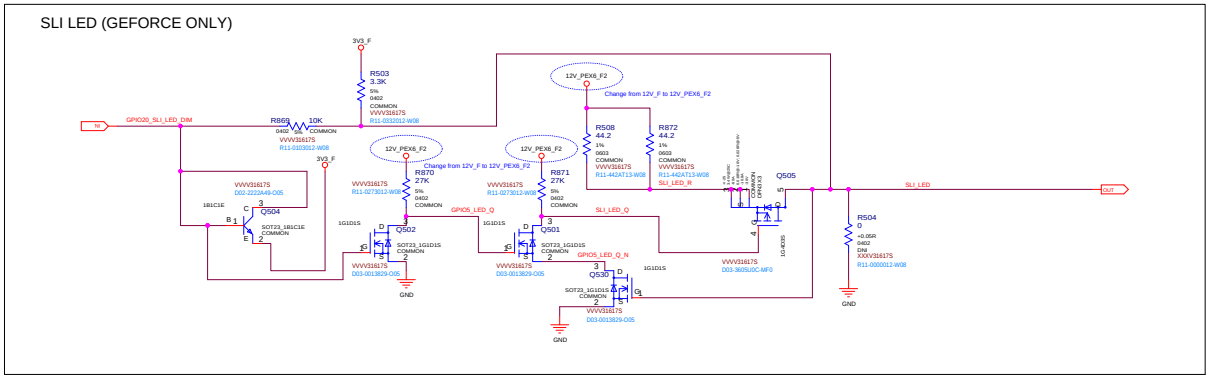

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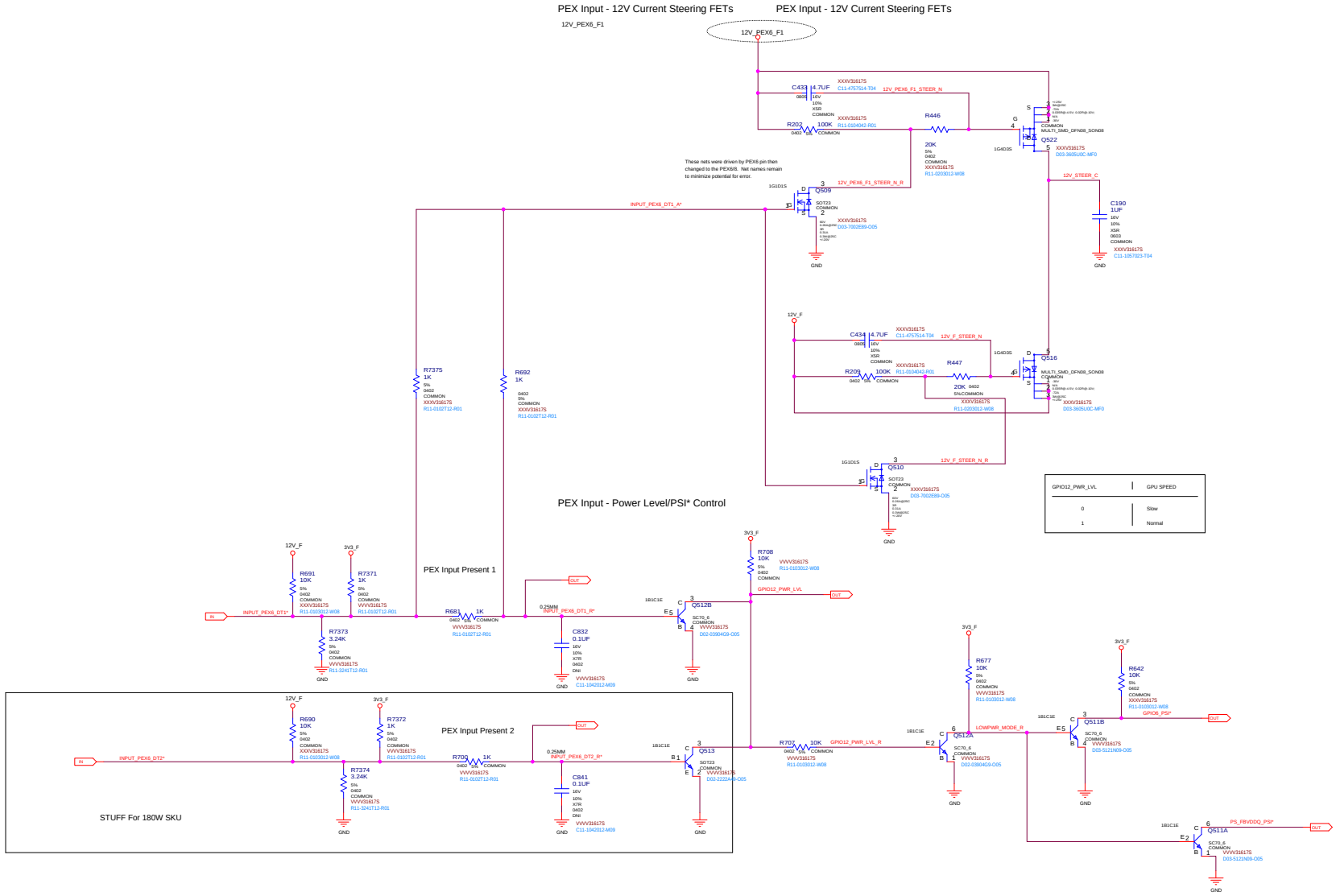
PEX Input - 12V Current Steering FETs
PEX Input - 12V Current Steering FETs
12V_PEX6_F1
12V_PEX6_F1
C433 4.7UF
R203 100K
R446 20K
Q522
12V_PEX6_F1_STEER_N
12V_PEX6_F1_STEER_N_R
Q509
INPUT_PEX6_DT1_A*
C190 1UF
12V_STEER_C
GND
12V_F
C434 4.7UF
R209 100K
R447 20K
Q516
12V_F_STEER_N
12V_F_STEER_N_R
Q510
R7375 1K
R692 1K
PEX Input - Power Level/PSI* Control
PEX Input Present 1
R691 10K
R7371 1K
R7373 3.24K
R681 1K
C832 0.1UF
Q512B
INPUT_PEX6_DT1*
INPUT_PEX6_DT1_R*
R708 10K
GPIO12_PWR_LVL
GPIO12_PWR_LVL
GPIO12_PWR_LVL_R
R690 10K
R7372 1K
R7374 3.24K
R700 1K
C841 0.1UF
Q513
PEX Input Present 2
INPUT_PEX6_DT2*
INPUT_PEX6_DT2_R*
STUFF For 180W SKU
R677 10K
Q512A
LOWPWR_MODE_R
R642 10K
Q511B
GPIO_PSI*
Q511A
PS_FBVDDQ_PSI*
GPIO12_PWR_LVL | GPU SPEED
0 | Slow
1 | Normal
These nets were driven by PEX6 pin then changed to the PEX6/8. Net names remain to minimize potential for error.
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PS: 12V Current Steering
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Page32: NCT7511 FAN2

Thermal IC : NCT7511Y

Layout notice :
*Add ground shielding for D+ and Dtraces.
*D+/D- route has to be away from the high noise area.
*The recommended traces width and ground shielding spacing are 10mils.

Please refer datasheet
TCRIT_SET Table
If floating,shutdown temp. set to 65℃

Thermal Diode

EEPROM

Fan connector option

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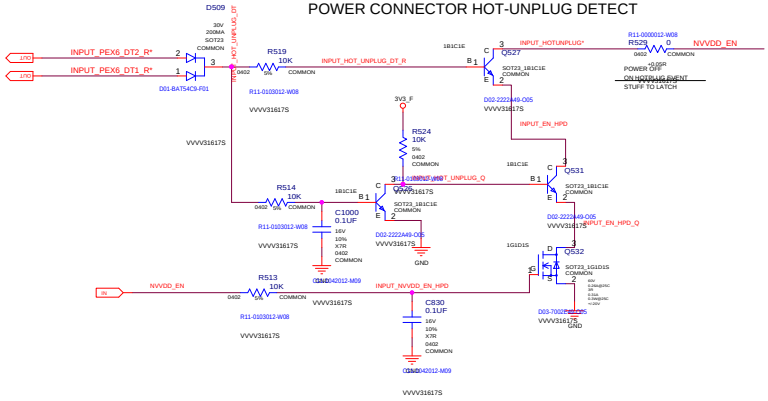
Page33: Power Connector Hot unplug

PEX Input - NVVDD Power Sequence

CURRENT STEERING

POWER CONNECTOR HPD

POWER CONNECTOR HOT-UNPLUG DETECT



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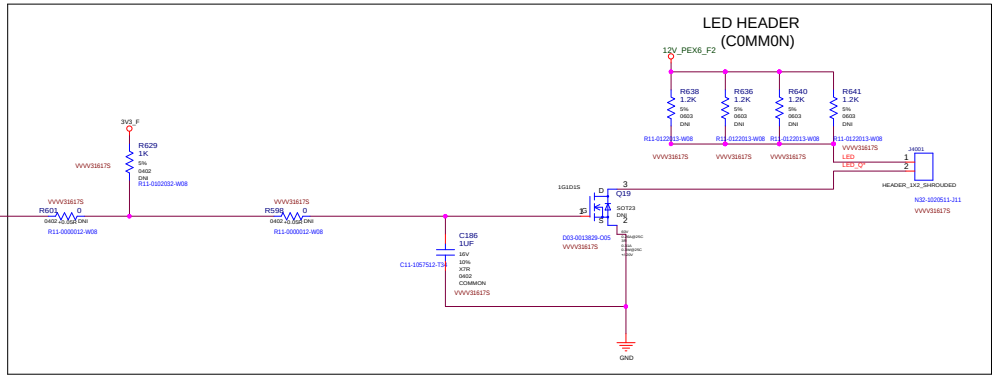
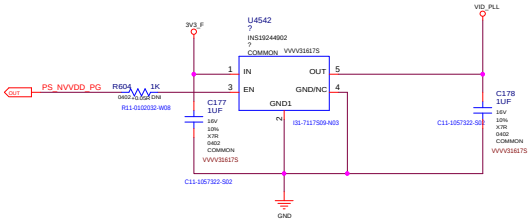
GeForce Logo LED





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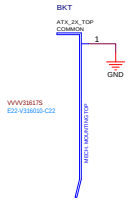
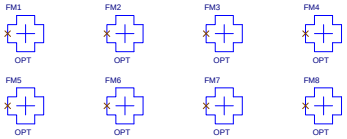
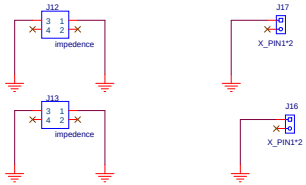
Brackets:



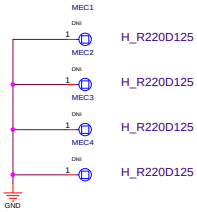
optical cross point



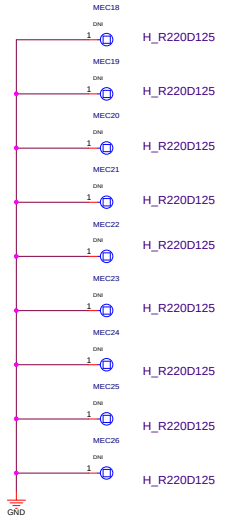
Top & bottom each layer set 4 points



GPU Stiffener:



MOUNTING HOLES FOR HS:



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