

P2004

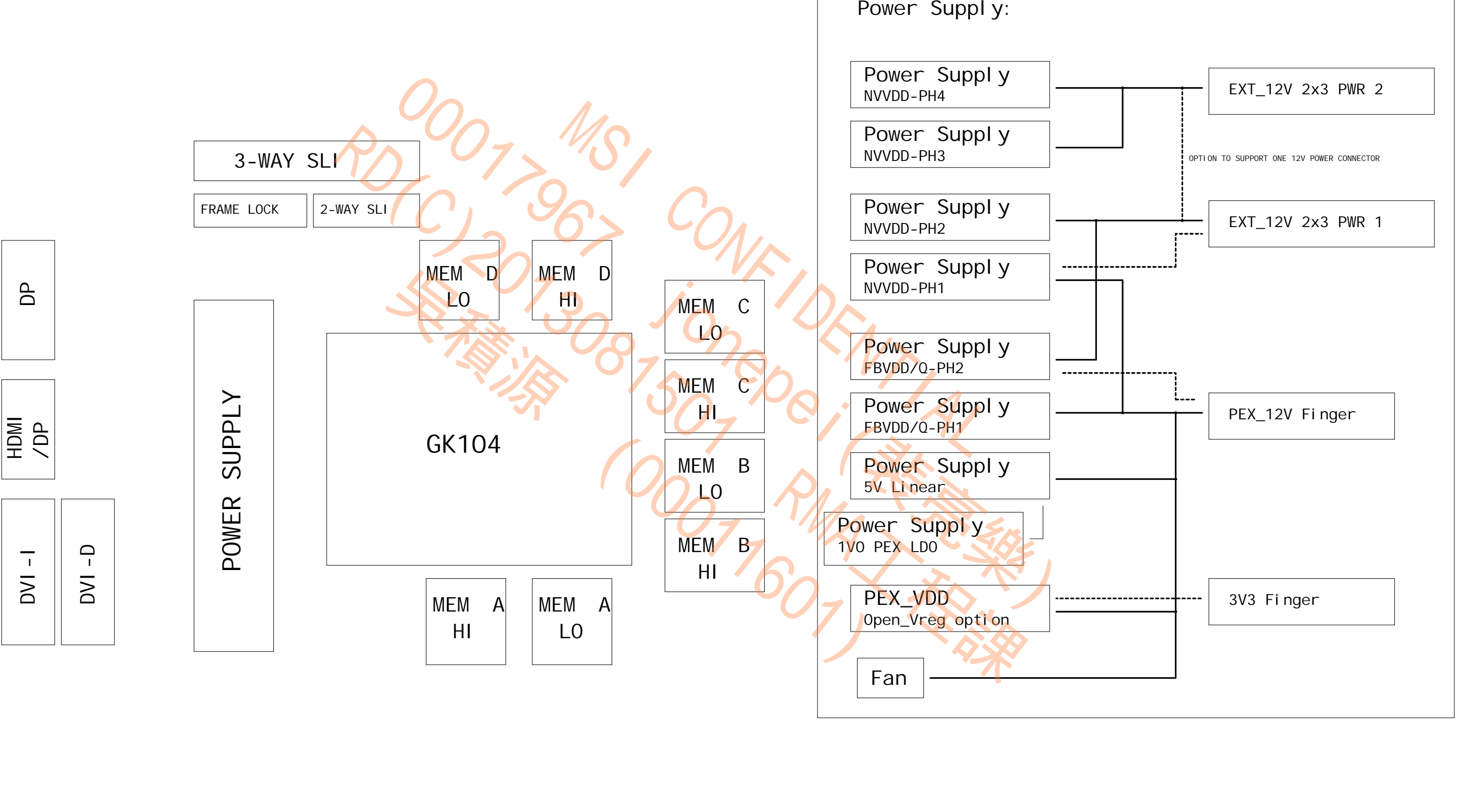
4/2GB GDDR5, 256/192b, 128Mx16/64Mx32  
DVI -I +DVI -D (stacked) + HDMI /DP + DP

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00017967 MSI CONFIDENTIAL  
RD(C)2013081501 jonepei (裴亮樂)  
吳積源 (00011601) RMA工程師

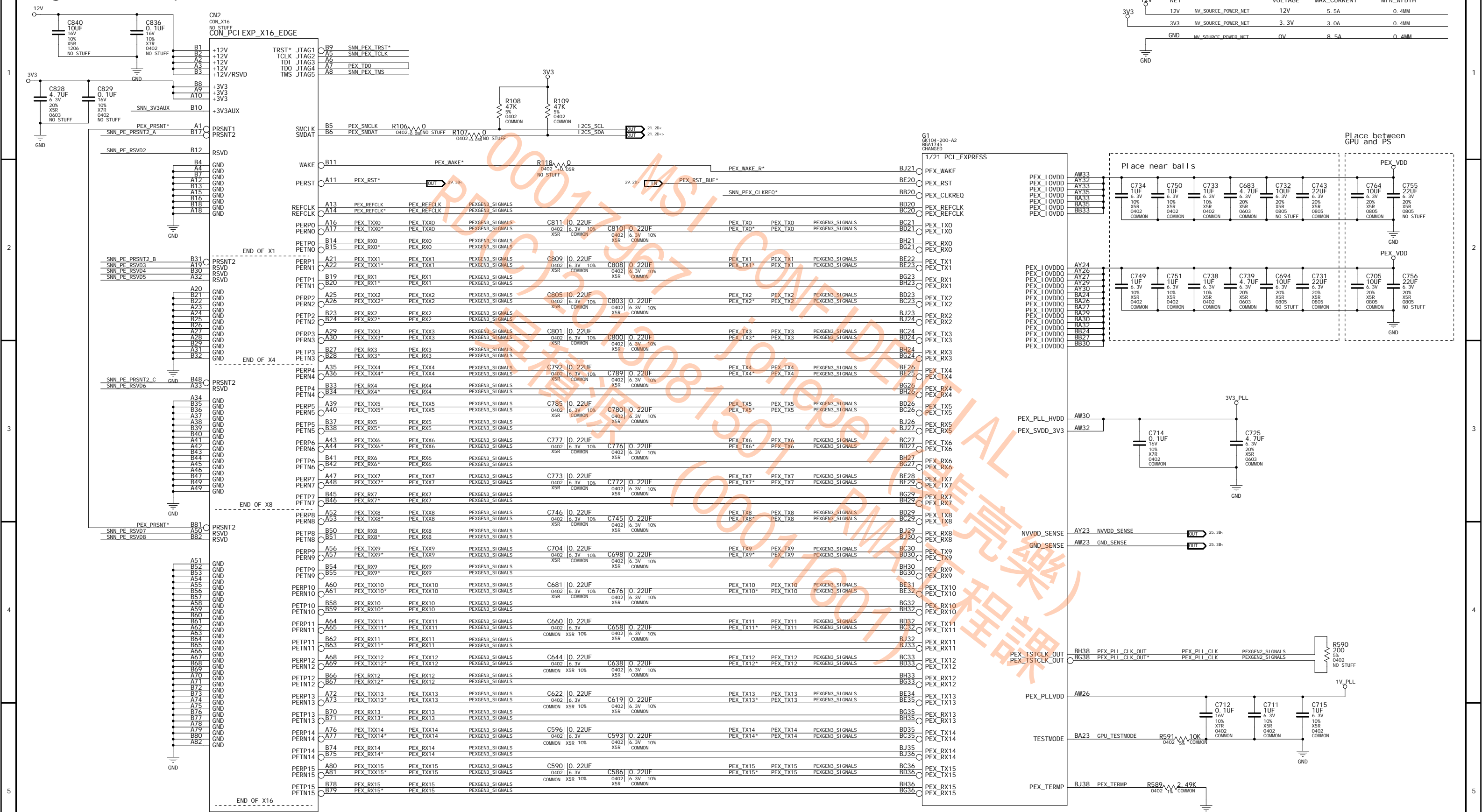


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ASSEMBLY	SKU0: GK104-200 / 192-BIT 1536MB GDDR5 / STACTED DVI + HDMI + DP
PAGE DETAIL	Block Diagram

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## Page3: PCI Express



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PAGE DETAIL	PCI Express

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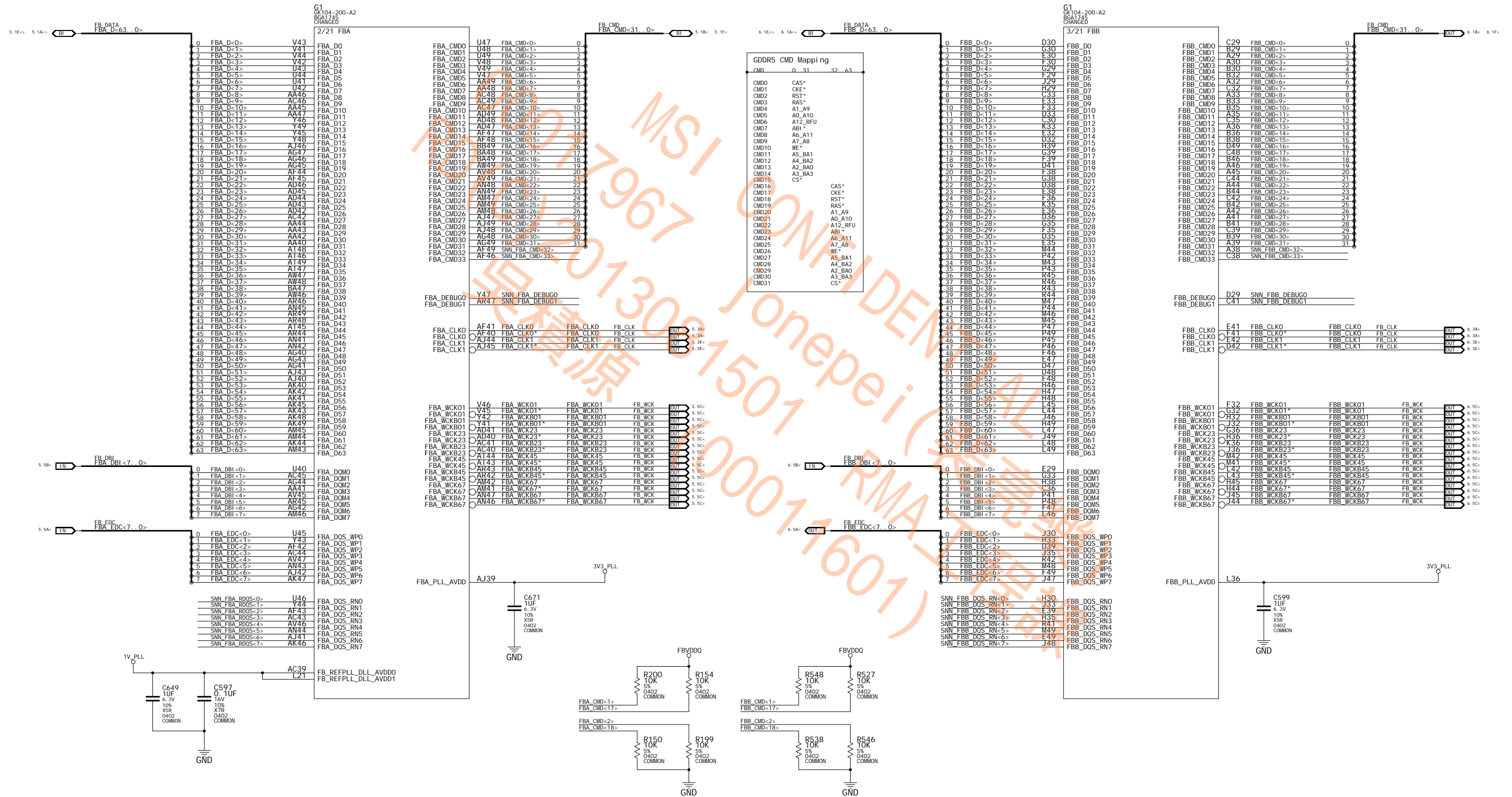


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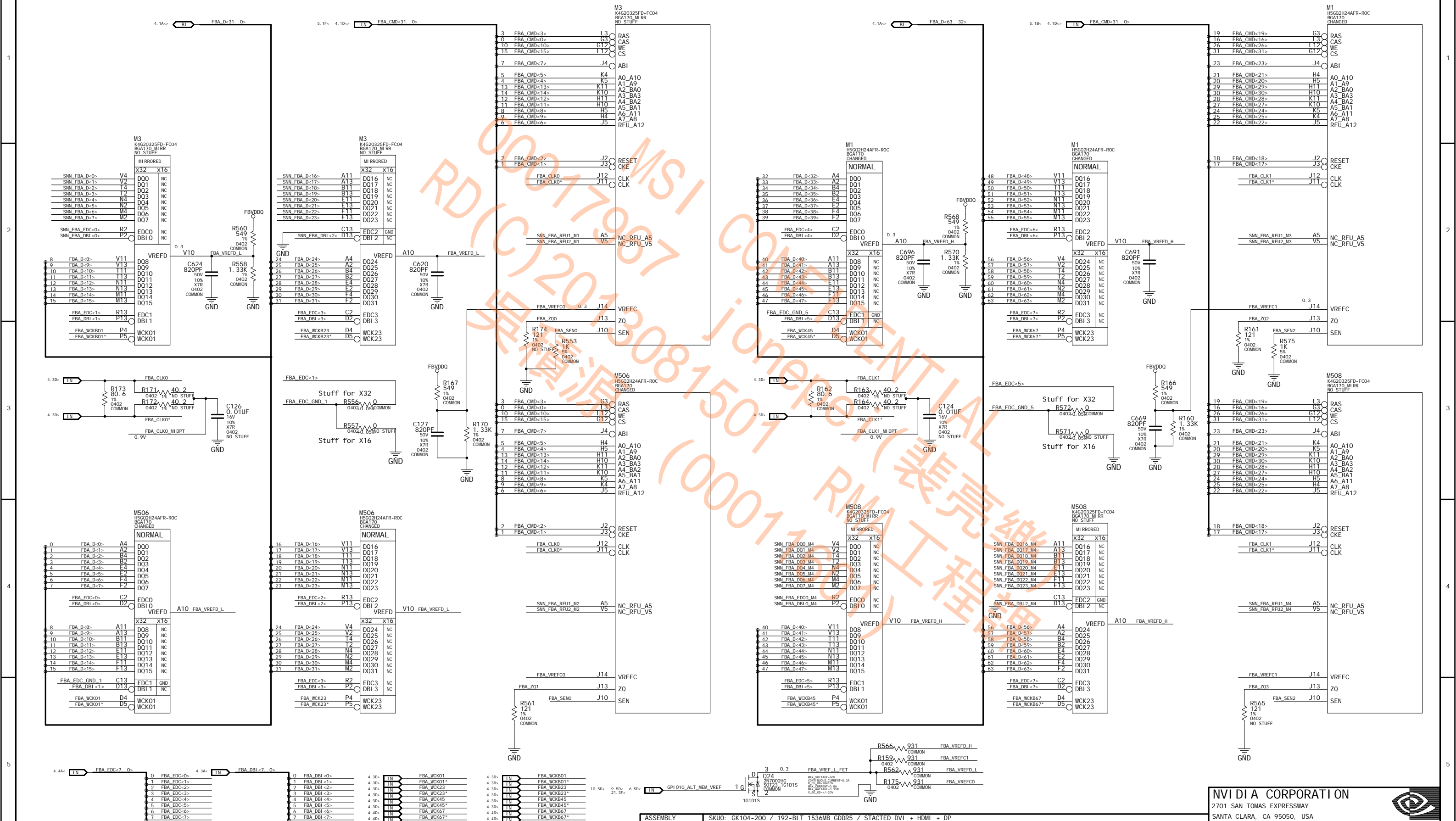
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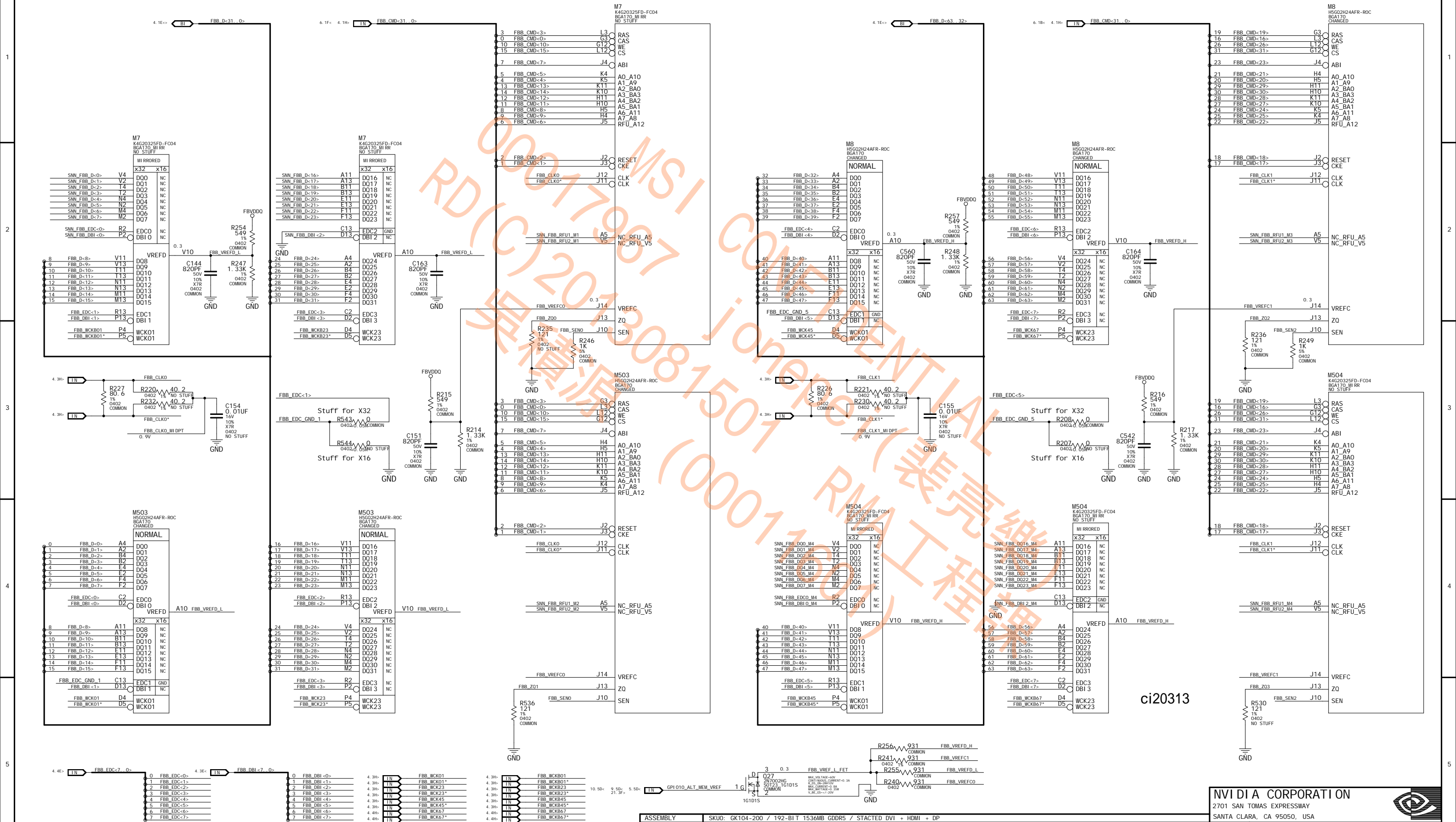


## PAGE5: FRAME BUFFER PARTITION A

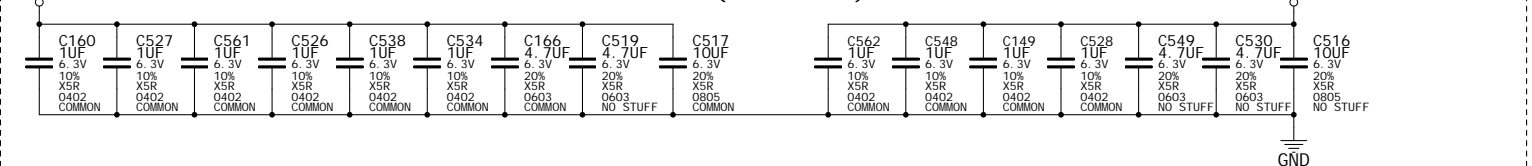
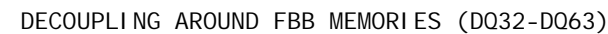
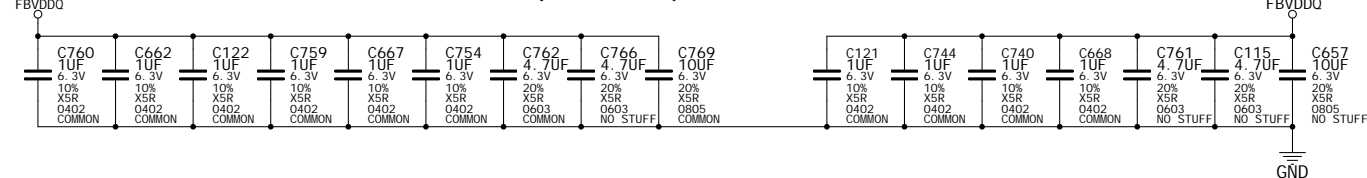
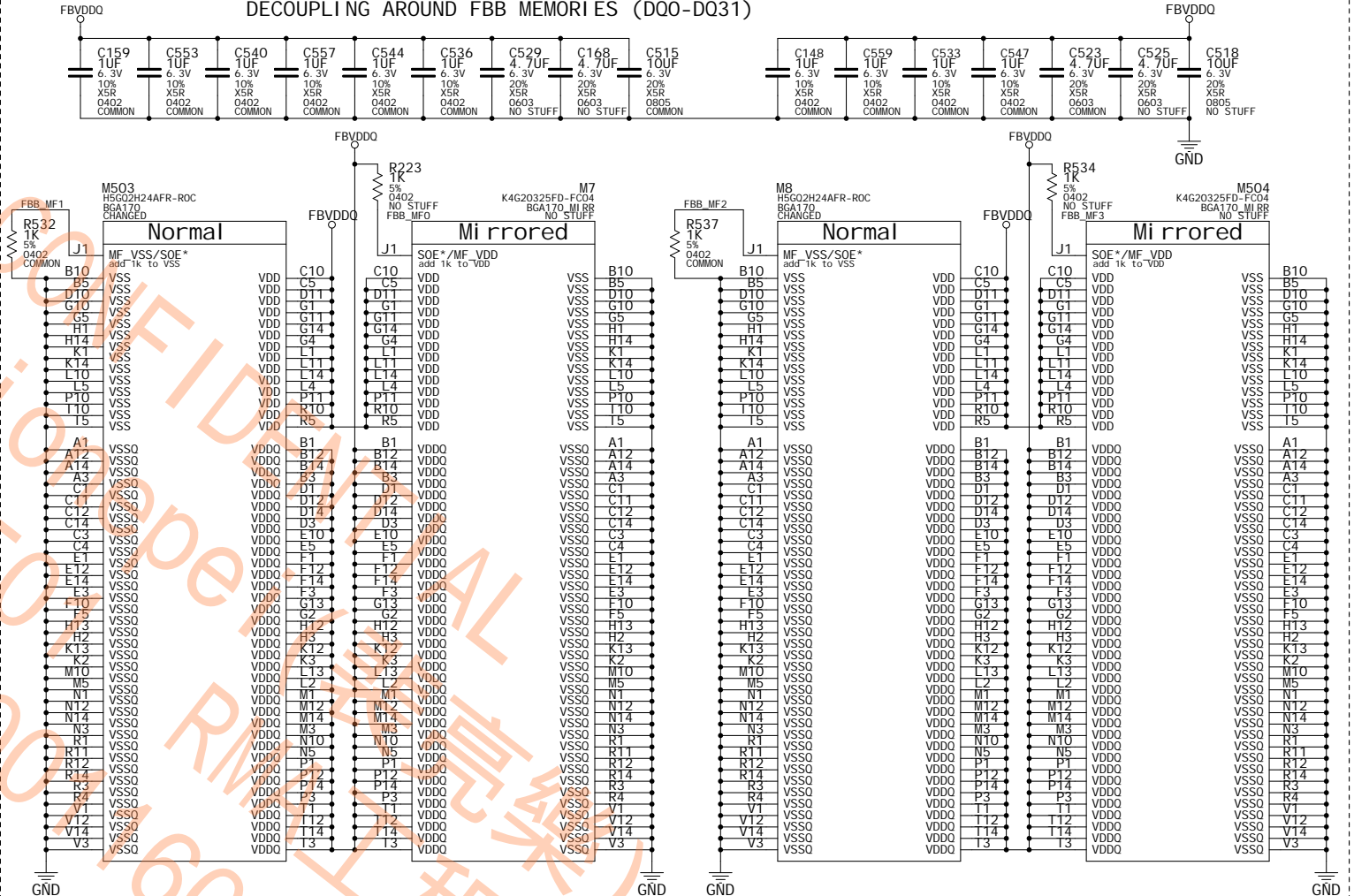
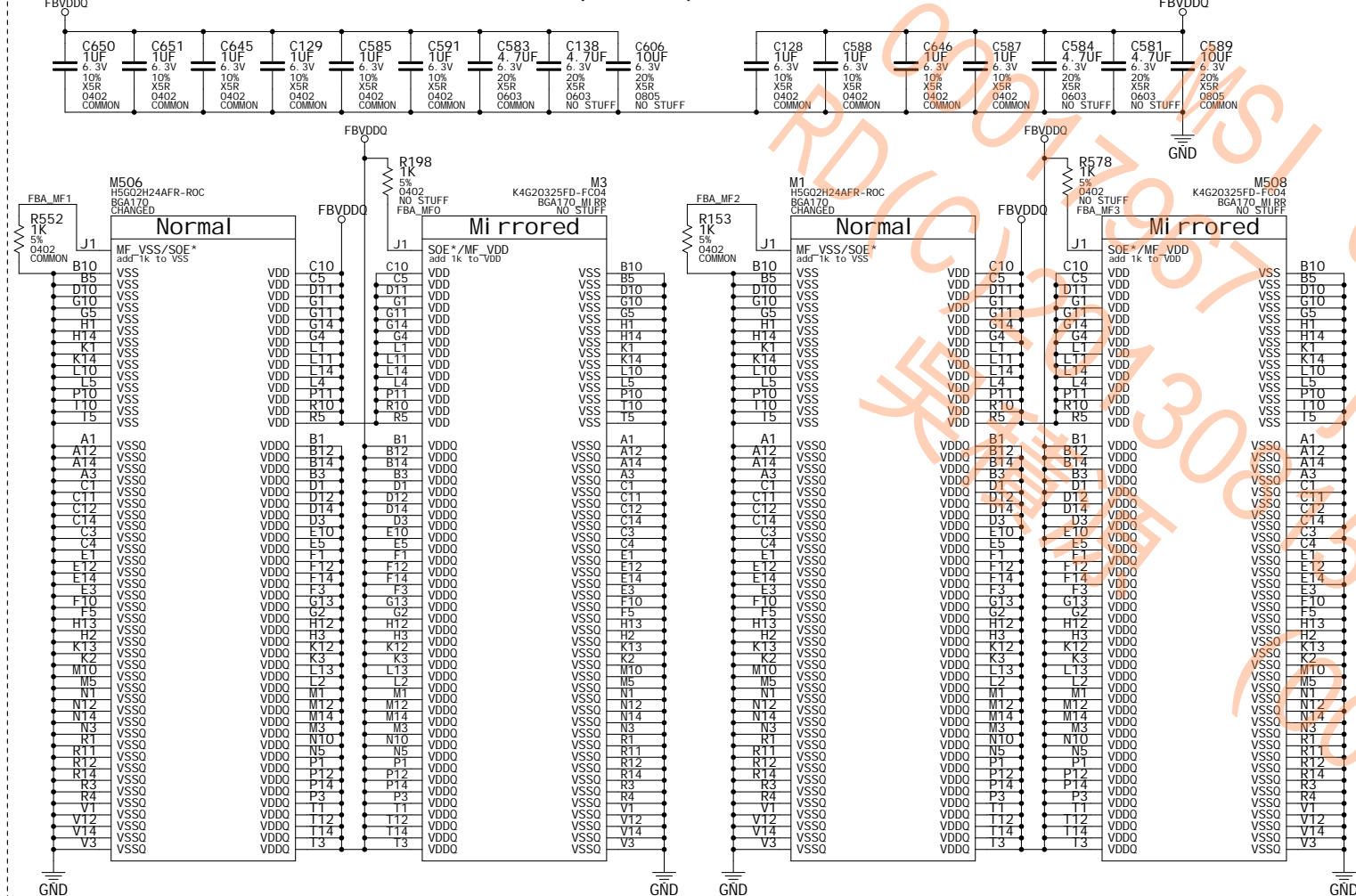


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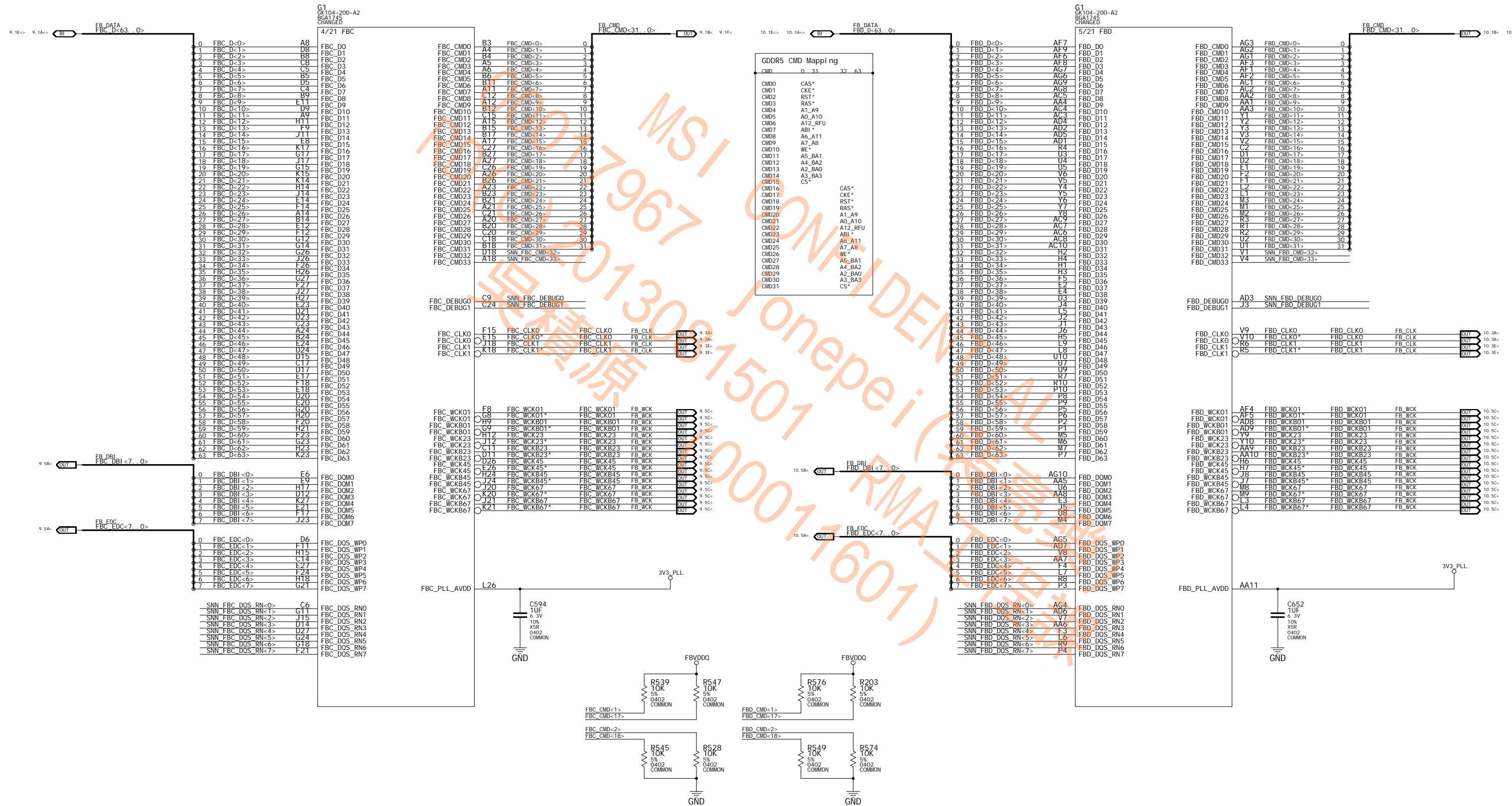
PAGE6: FRAME BUFFER PARTITION B



## PAGE7: FRAME BUFFER PARTITION A/B DECOUPLING

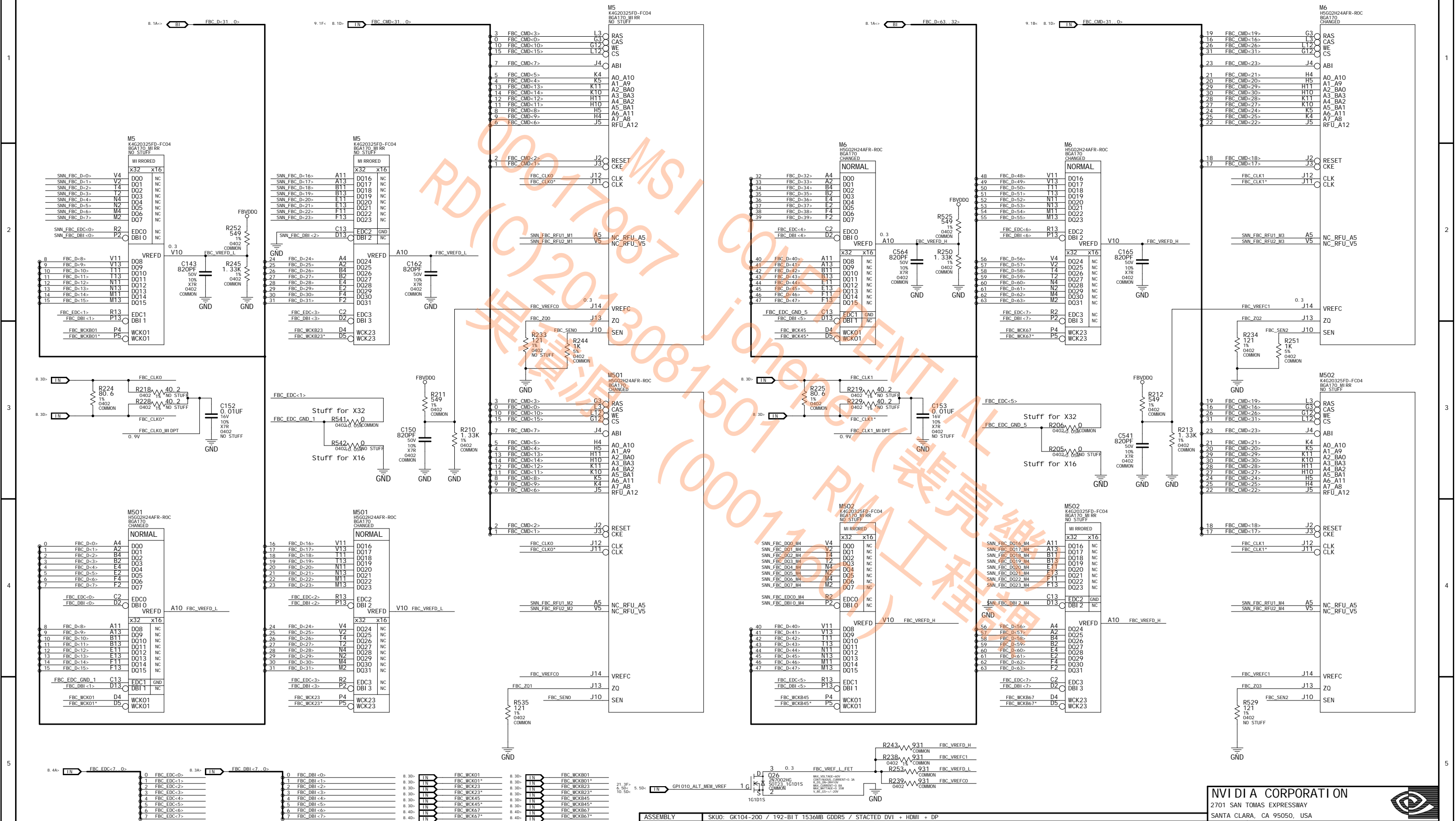









## PAGE9: FRAME BUFFER PARTITION C

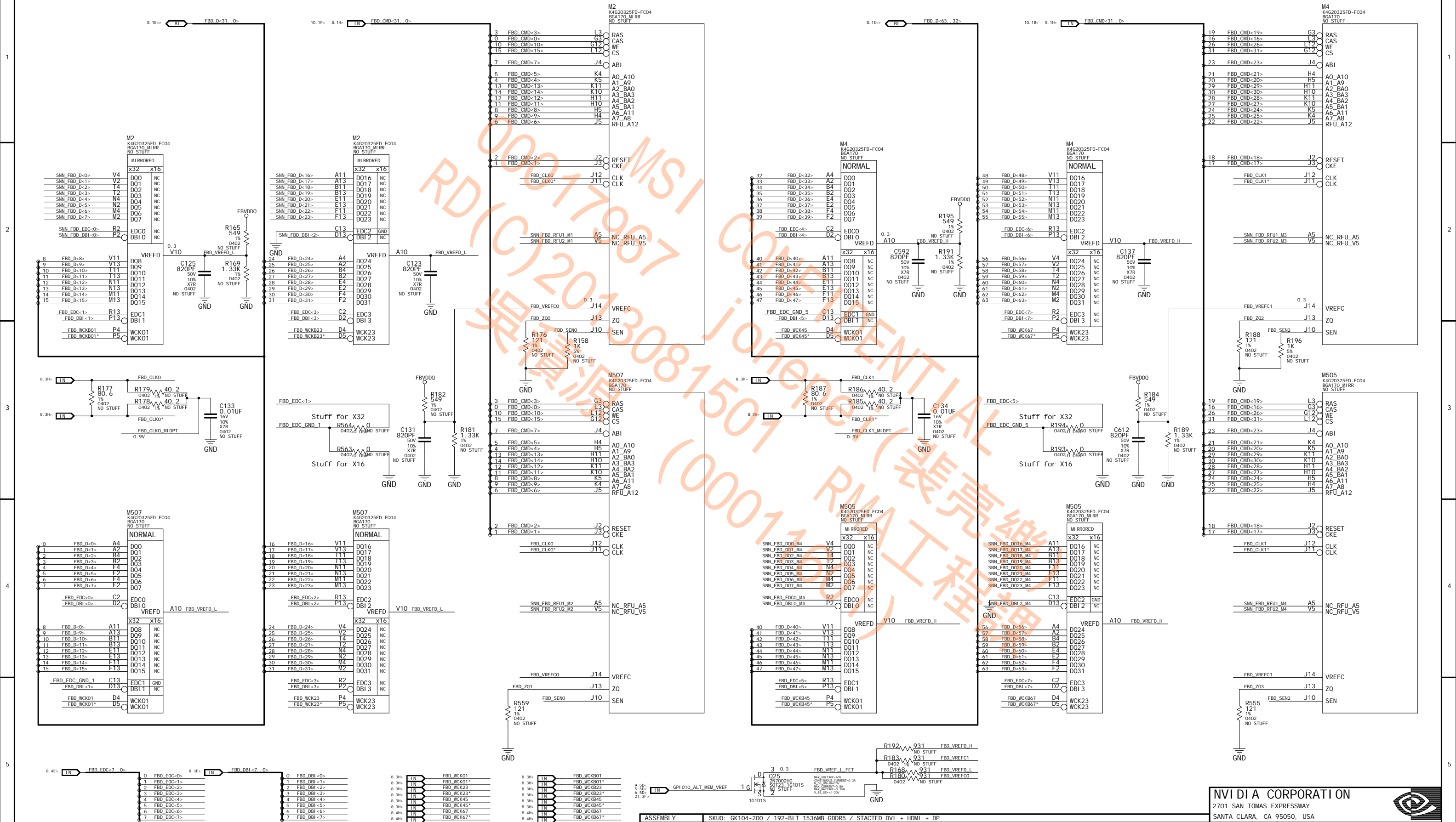


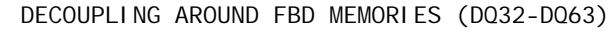
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PAGE DETAIL L	MEM FB_C

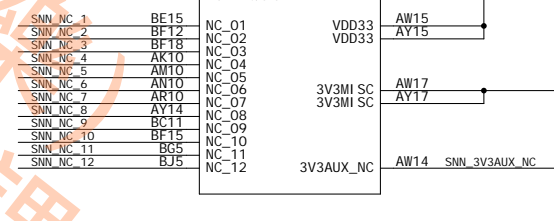
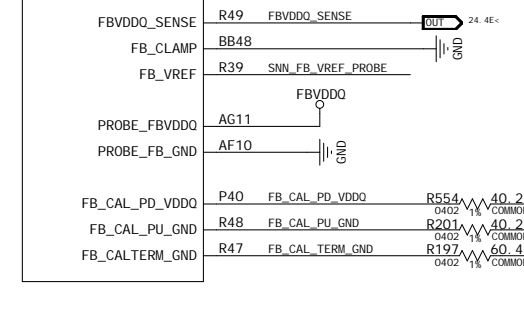
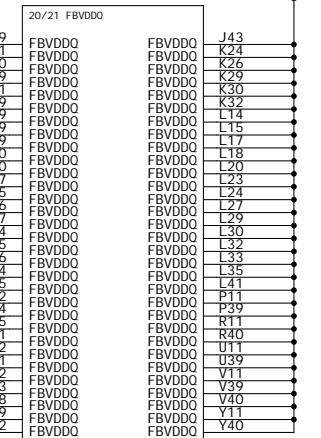
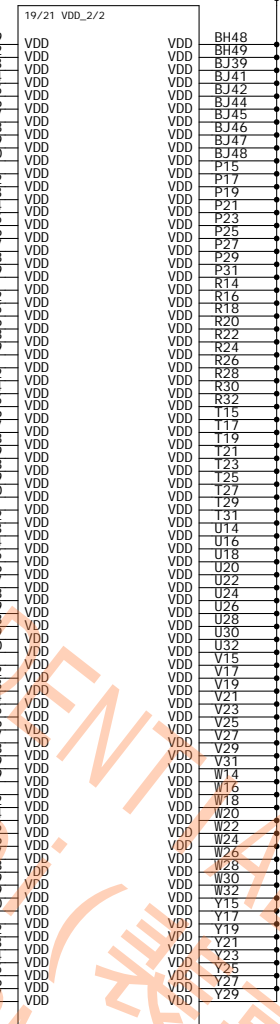
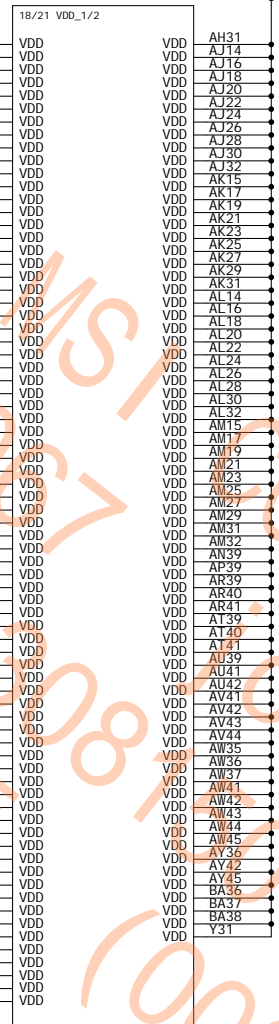
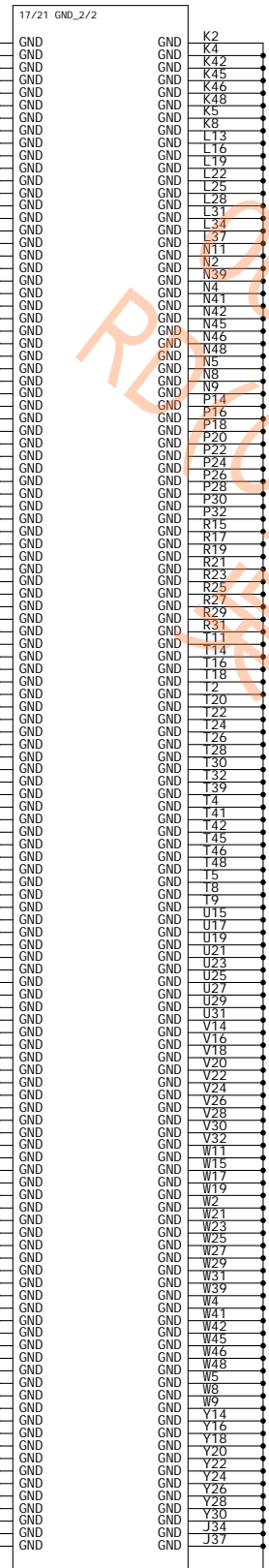
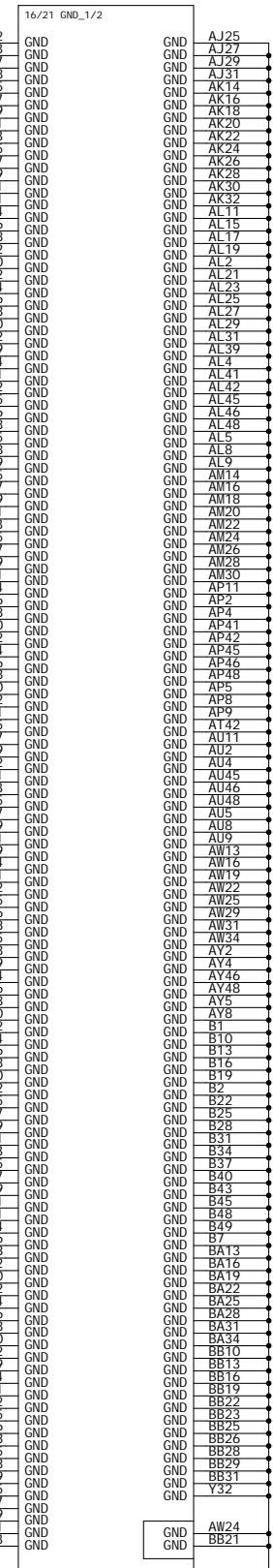
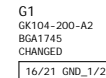
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PAGE10: FRAME BUFFER PARTITION D



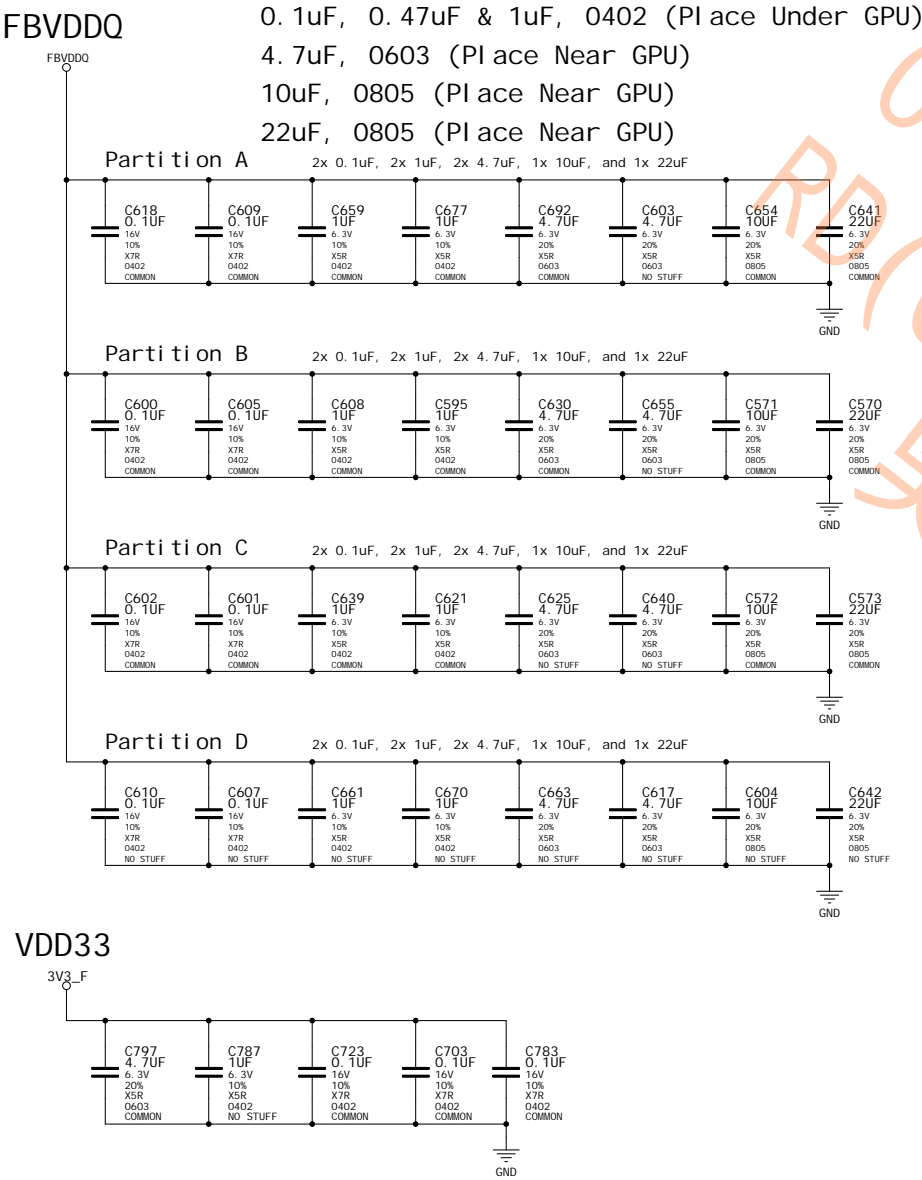




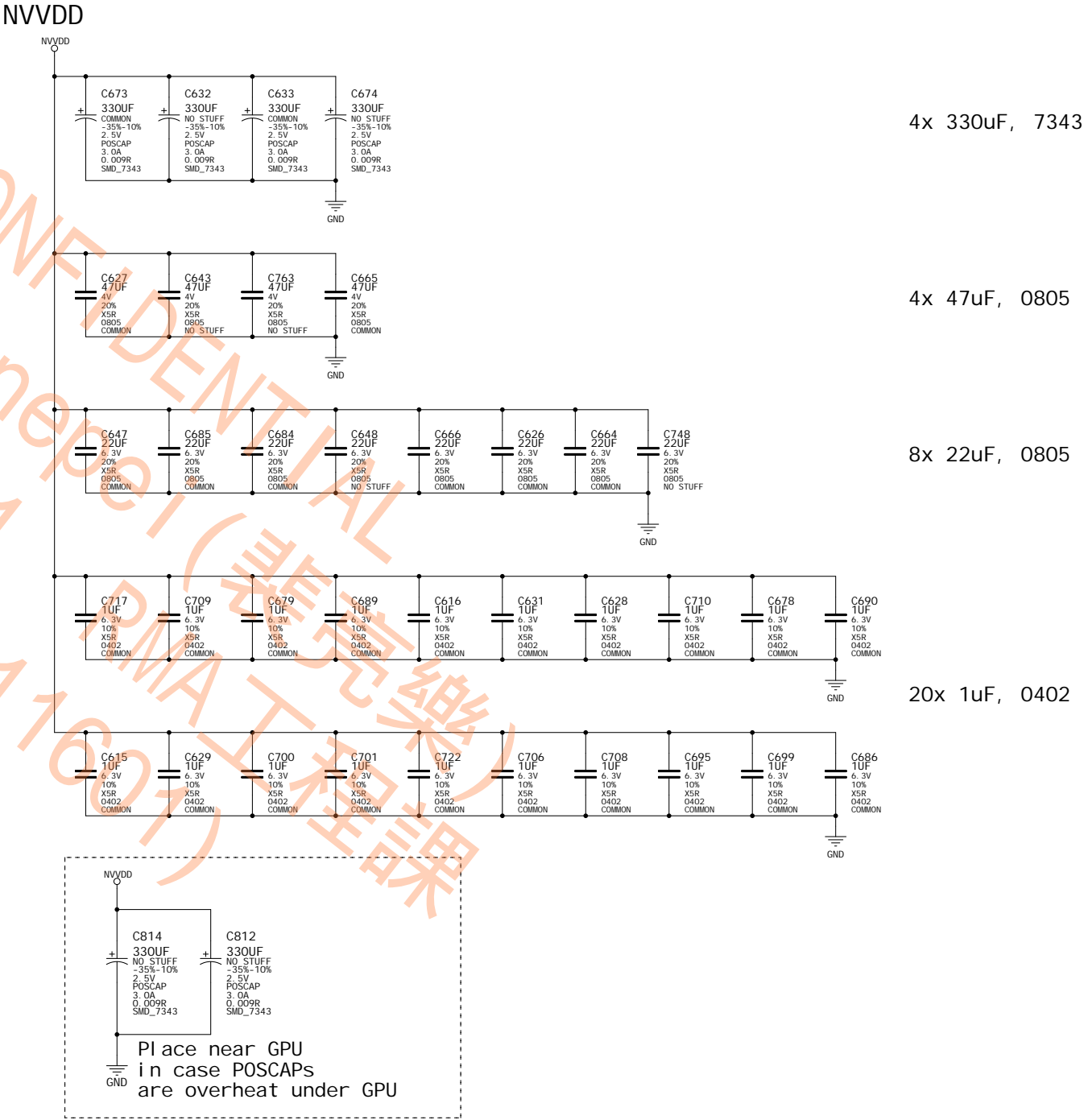


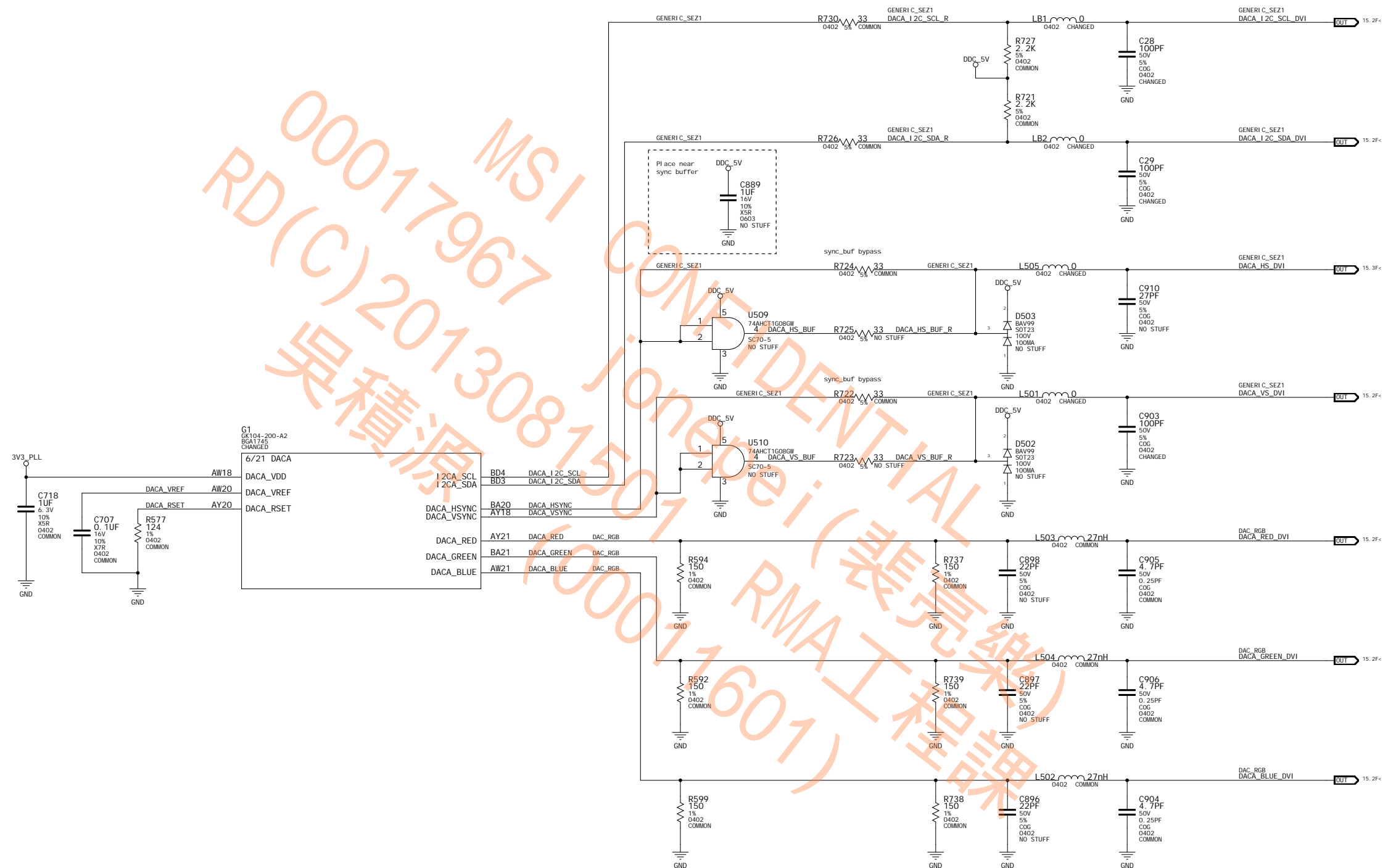
ci20313

Based on GB2-X GDDR5 FBVDDQ Decap Guideline




NVVDD Decoupling caps. Place under GPU.



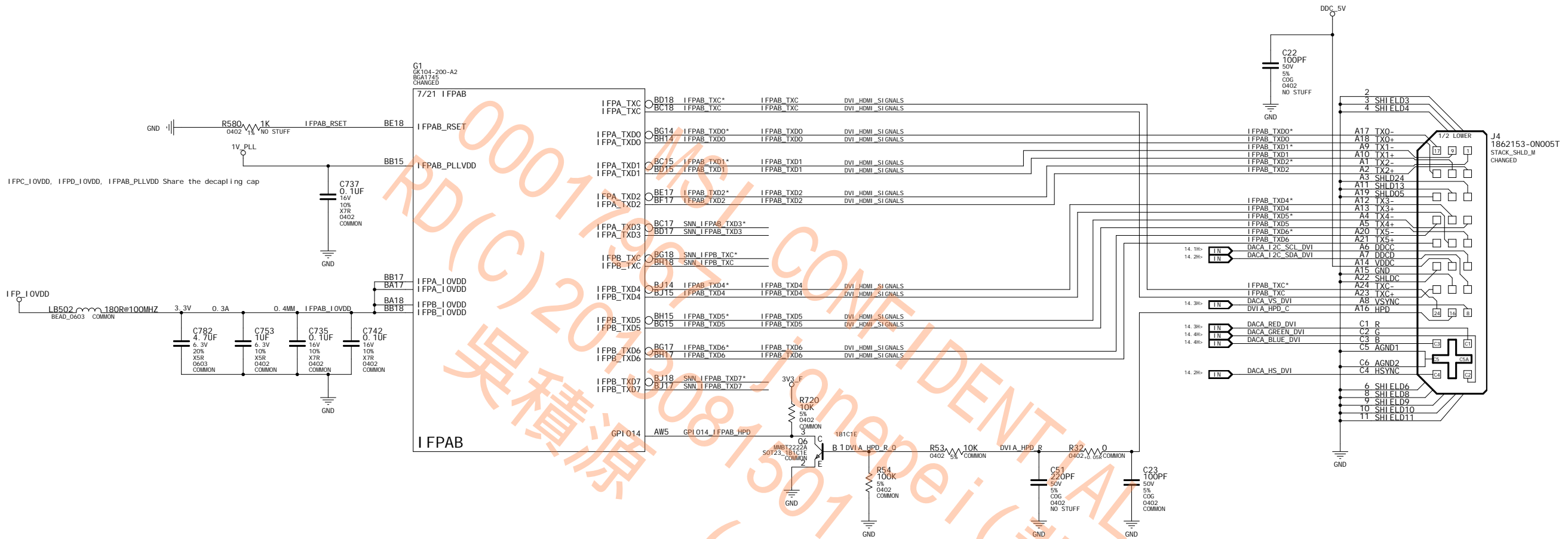


ASSEMBLY	SKU: GK104-200 / 192-BIT 1536MB GDDR5 / STACTED DVI + HDMI + DP
PAGE DETAIL	DACA Interface

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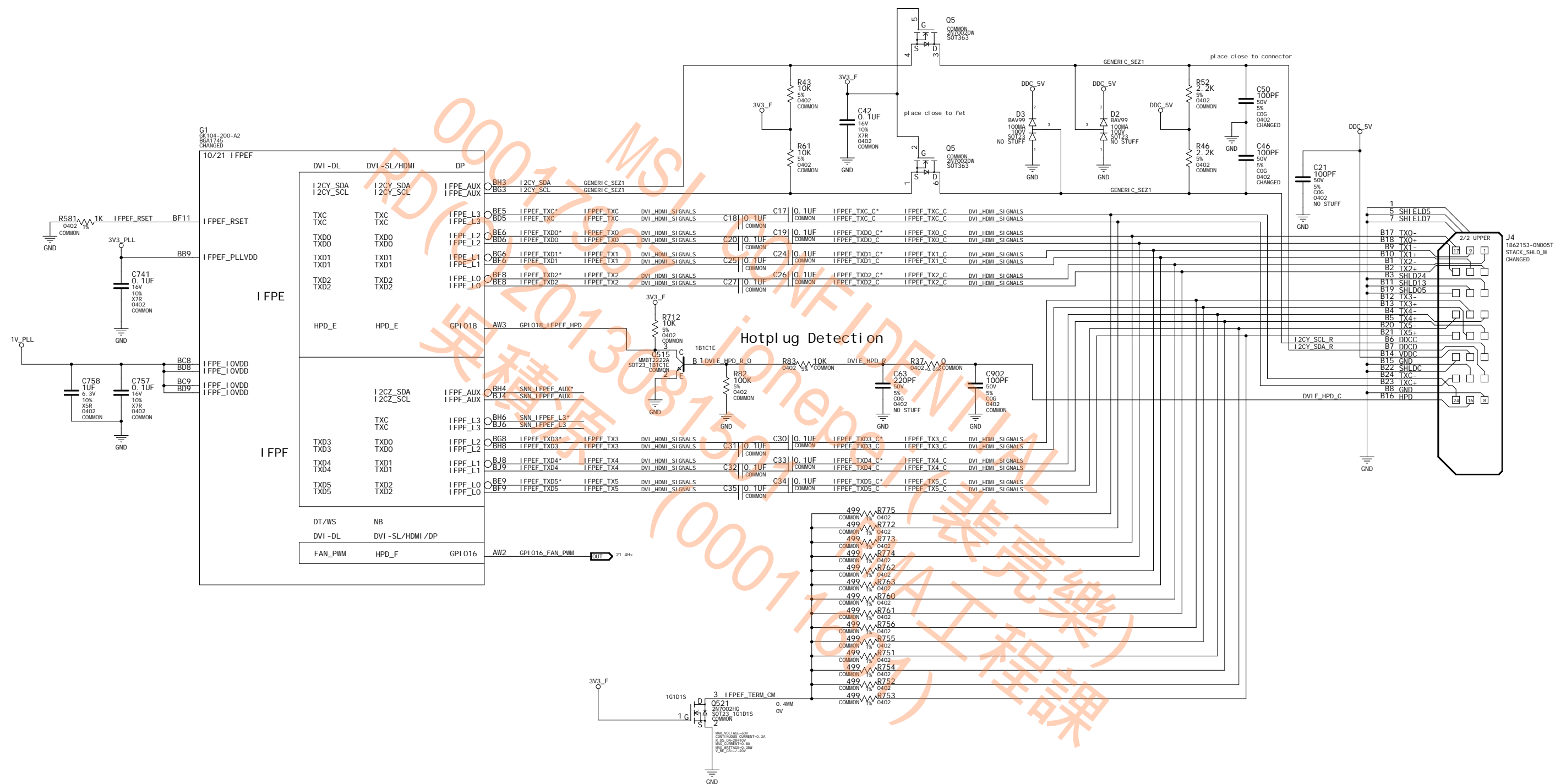
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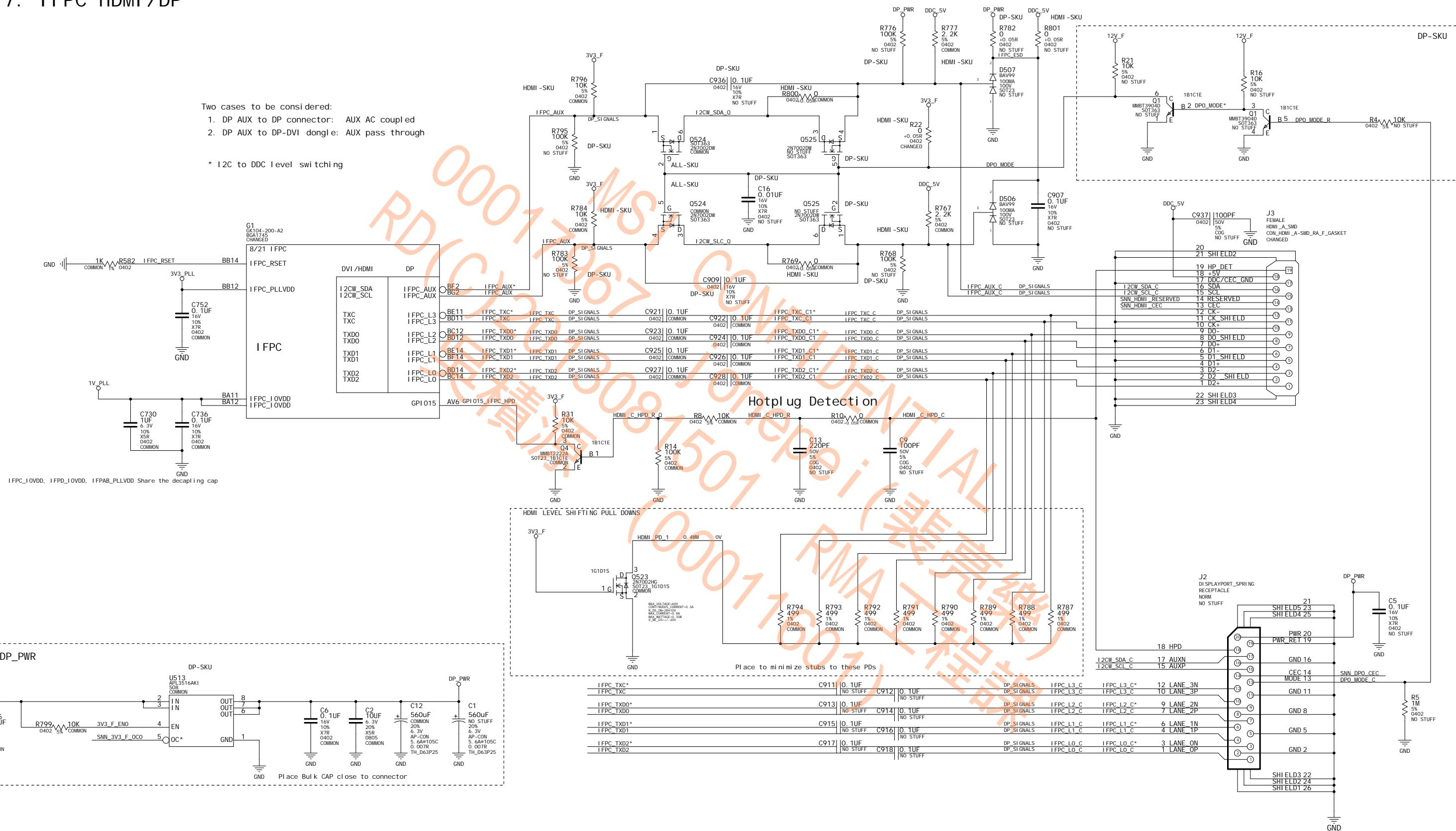
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Two cases to be considered:

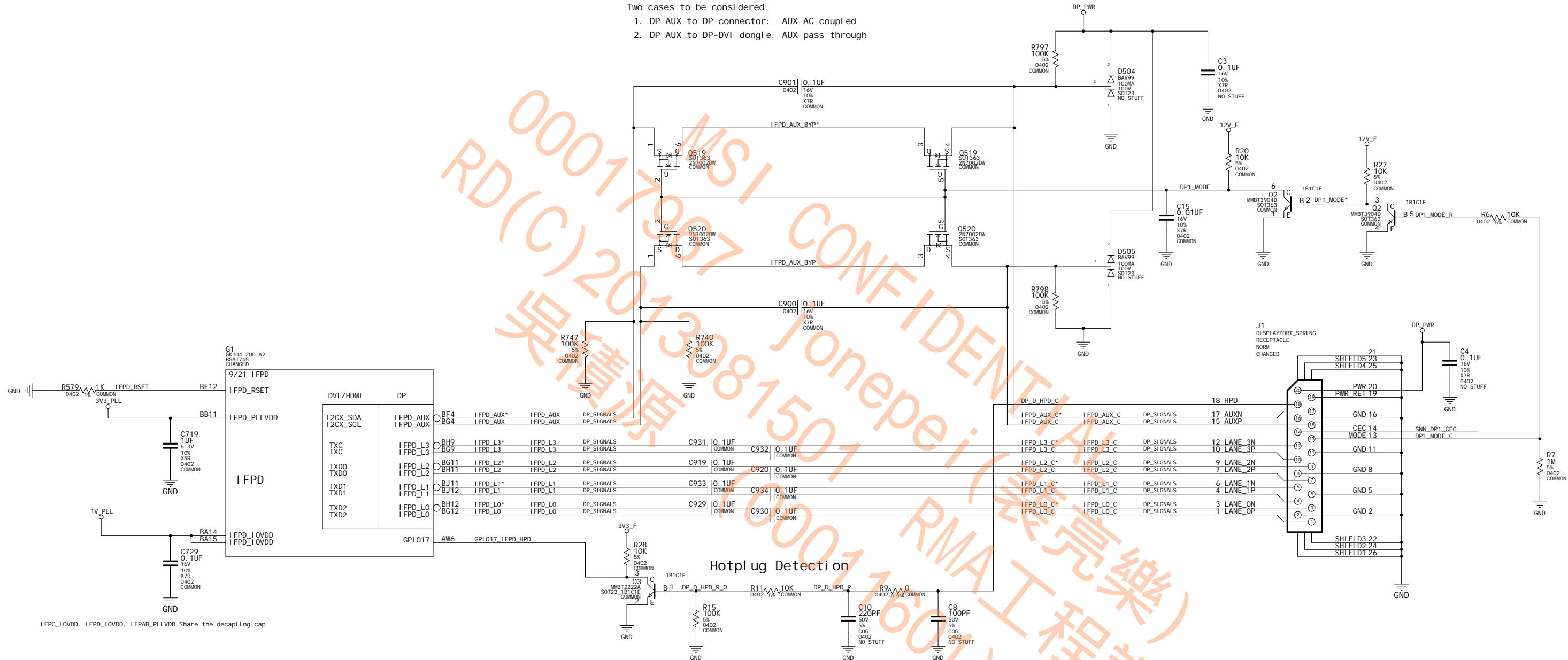
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

\* I2C to DDC level switching





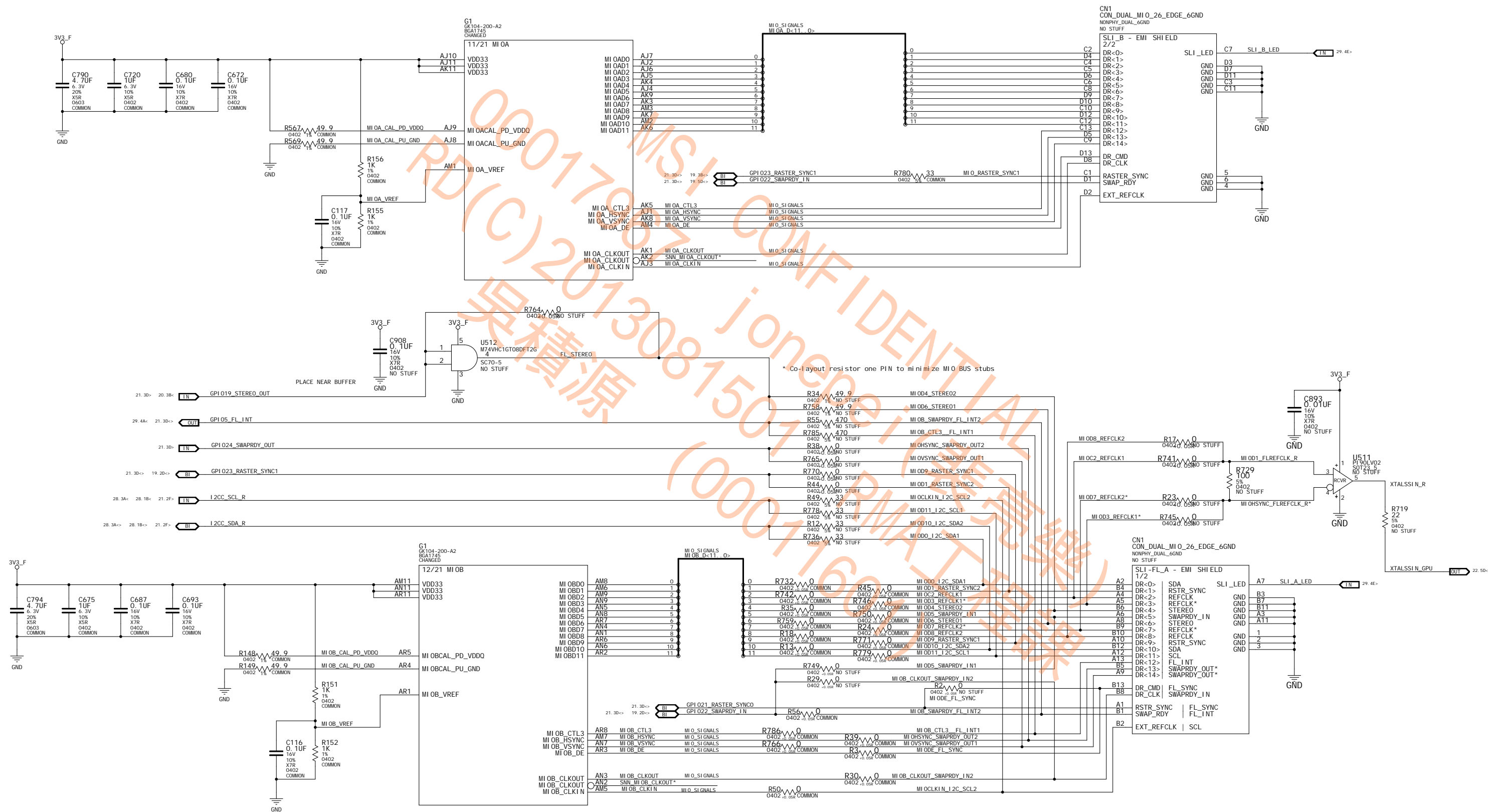
- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
  2. DP AUX to DP-DVI dongle: AUX pass through

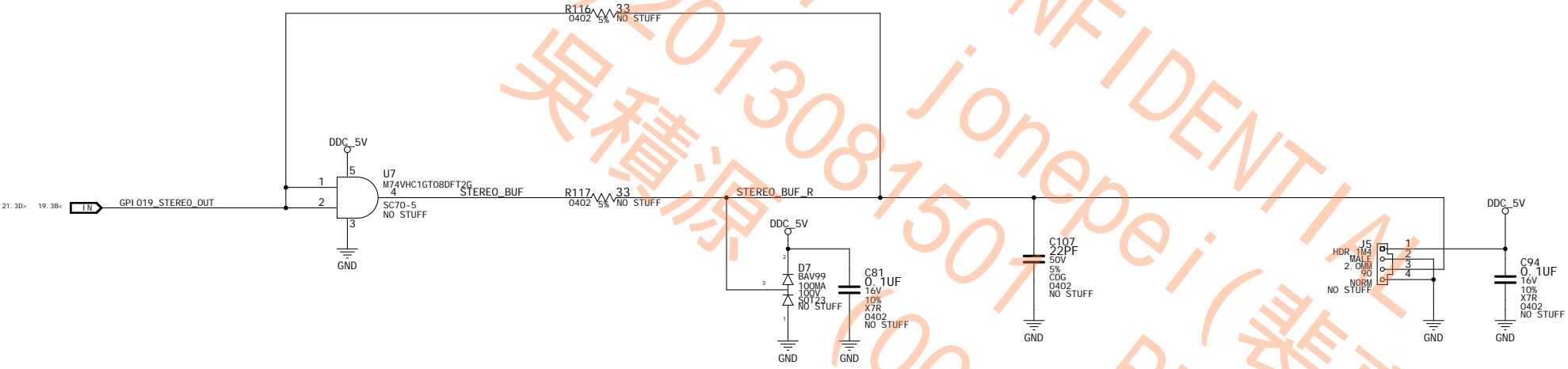


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## Page19: MI 0A/B Interface and Frame Lock

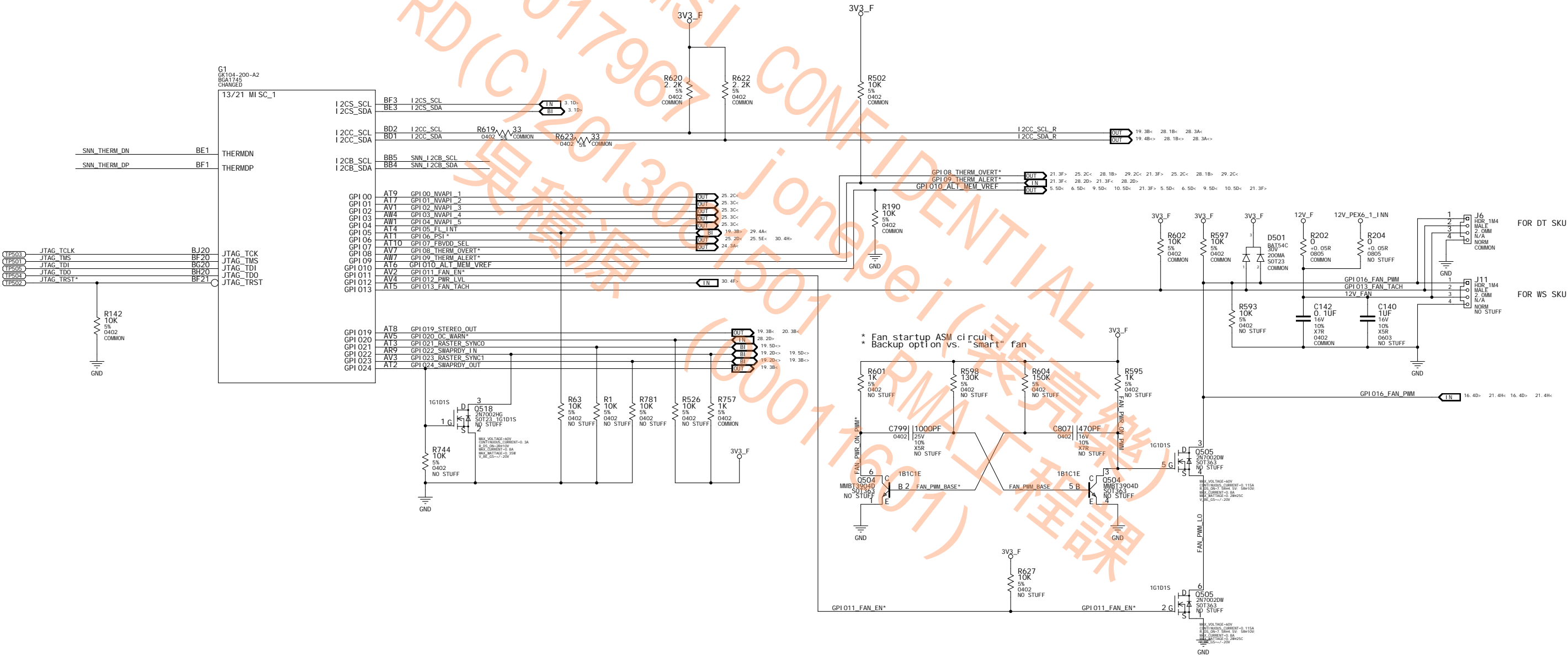




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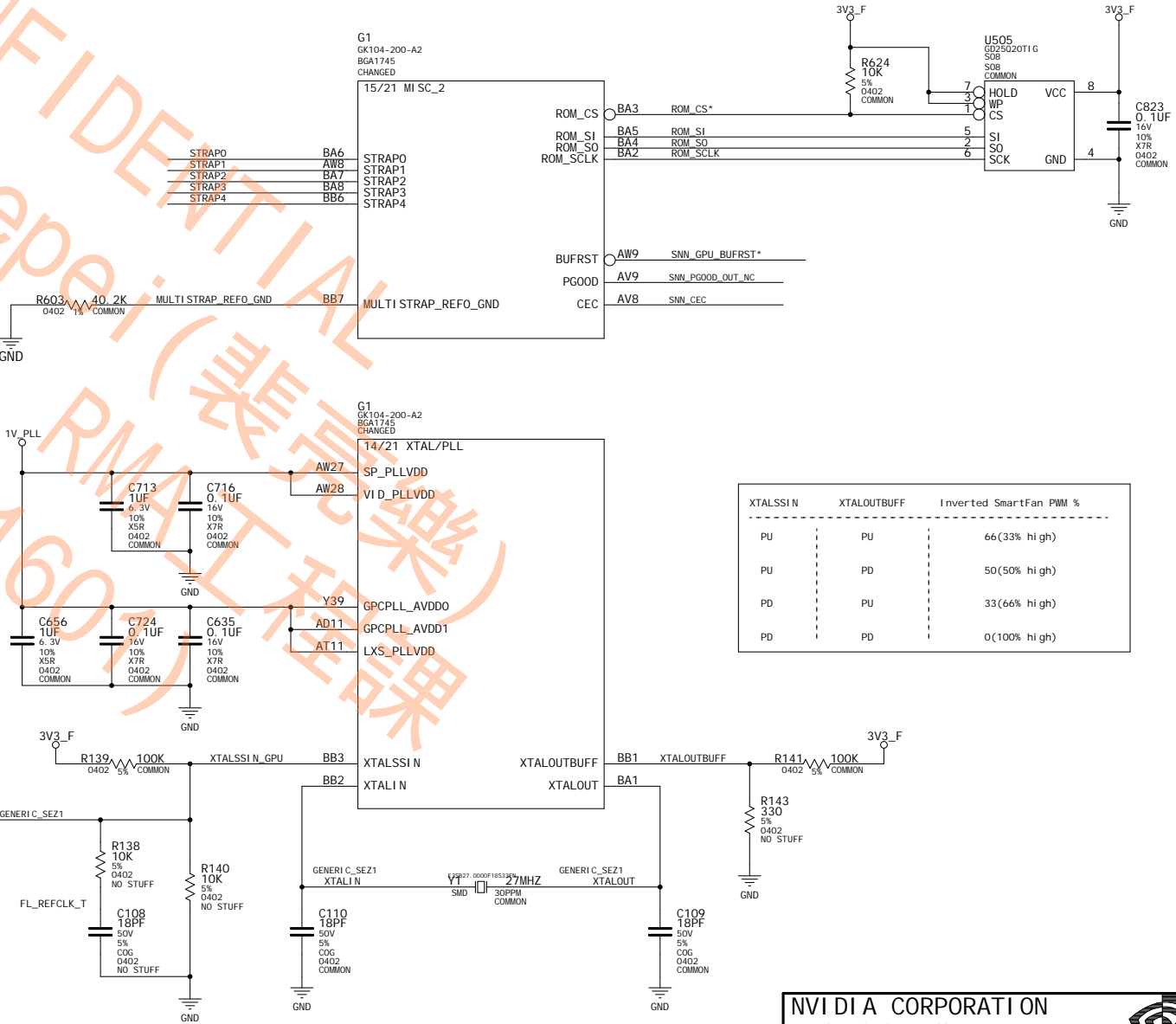
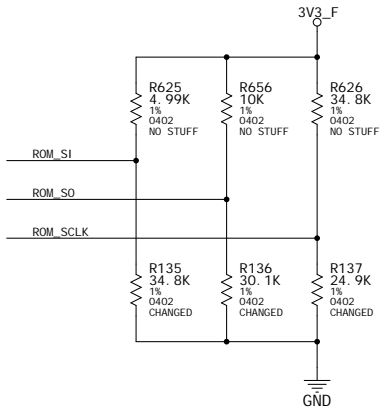
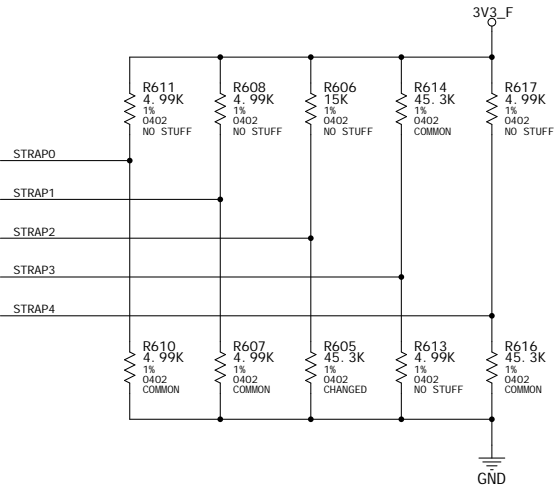
Page22: MI SC2: ROM, XTAL, Straps

STRAPO	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVICEID [3:0]*	0111 - (0x1187)*	45K PD -200 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		
ROM_SI	RAMCFG[0]*	0*	
	RAMCFG[1]*	1*	64Mx32 192 bit hynix for SKU0 primary memory
	RAMCFG[2]*	1*	35K PD*
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	30k PD*
	FB[0]_APERTURE_SIZE*	1* For 128MB*	
	FB[1]_APERTURE_SIZE*	0* For 128MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0* DISABLE*	
	PCI_DEVICEID_EXT[5]*	0* For 0x1187*	25K PD*
	SUB_VENDOR*	1* Dedicated BIOS*	
	PCI_DEVICEID_EXT[4]*	0* For 0x1187*	

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32	192-bit Elpida
0010	32Mx32	192-bit Hynix
0011	32Mx32	192-bit Samsung
0100	Reserved	
0101	64Mx32	192-bit Elpida
0110	64Mx32	192-bit Hynix
0111	64Mx32	192-bit Samsung

	MULTI_STRAP_REFO_GND
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND



XTALSSIN	XTALOUTBUFF	Inverted SmartFan PWM %
PU	PU	66(33% high)
PU	PD	50(50% high)
PD	PU	33(66% high)
PD	PD	0(100% high)

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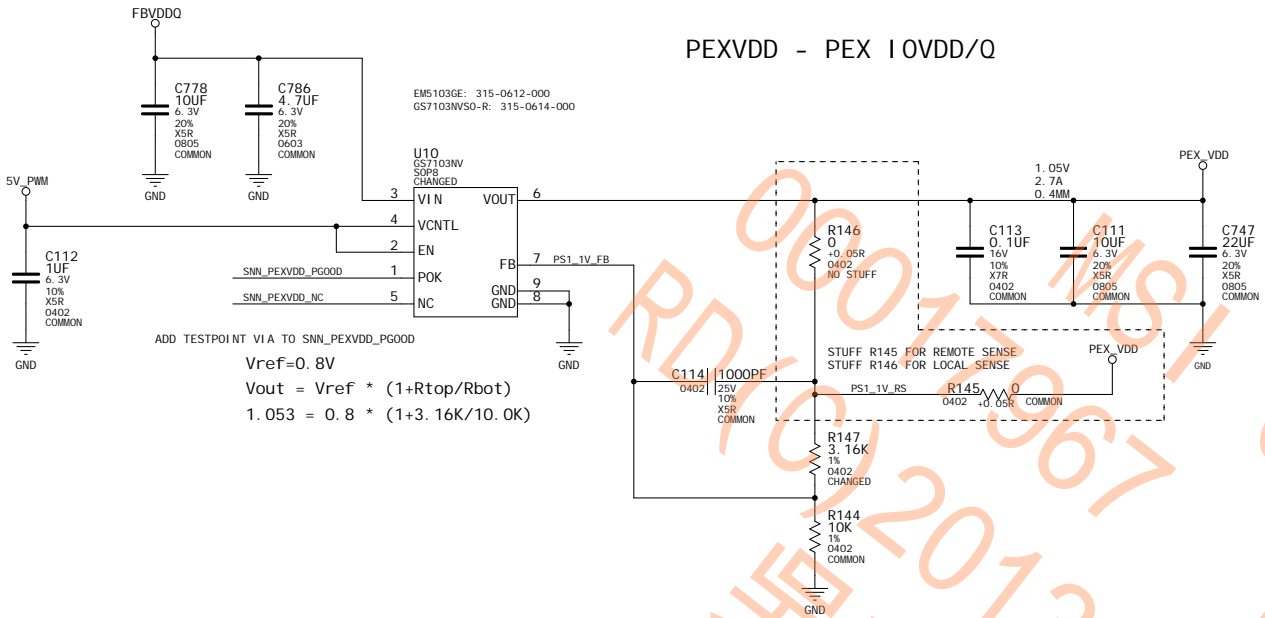
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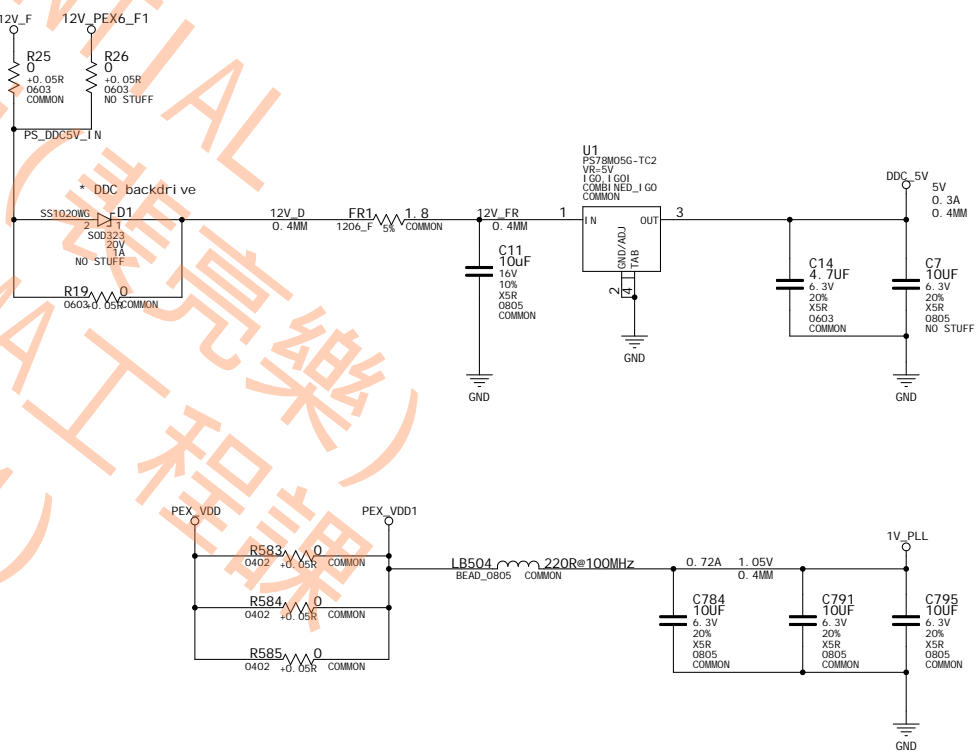
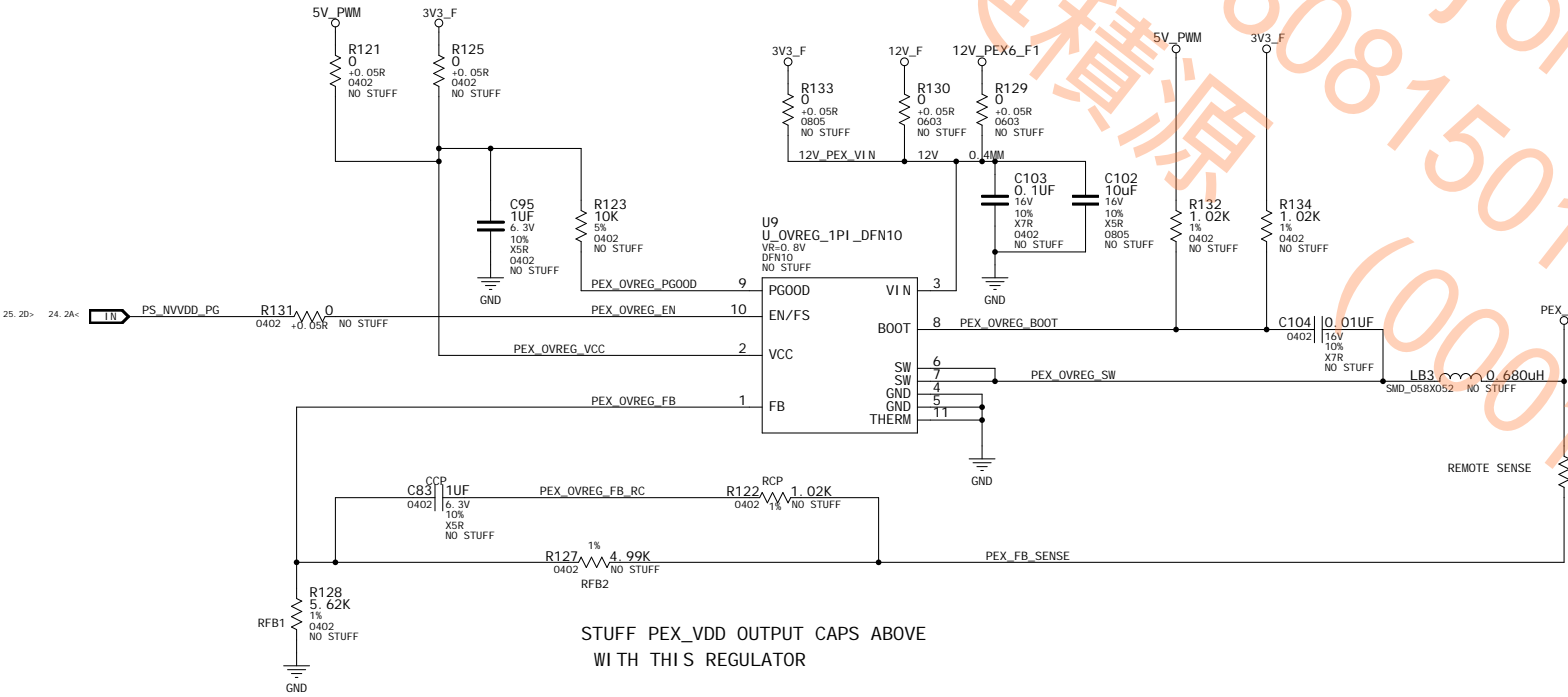
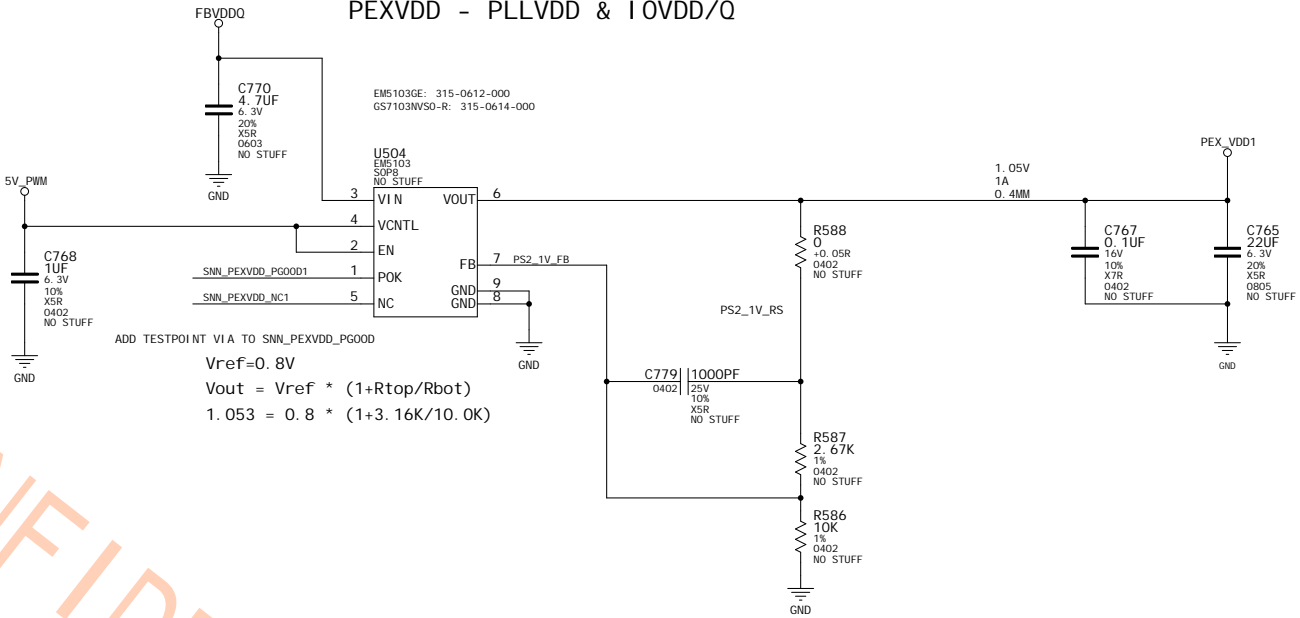
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1  
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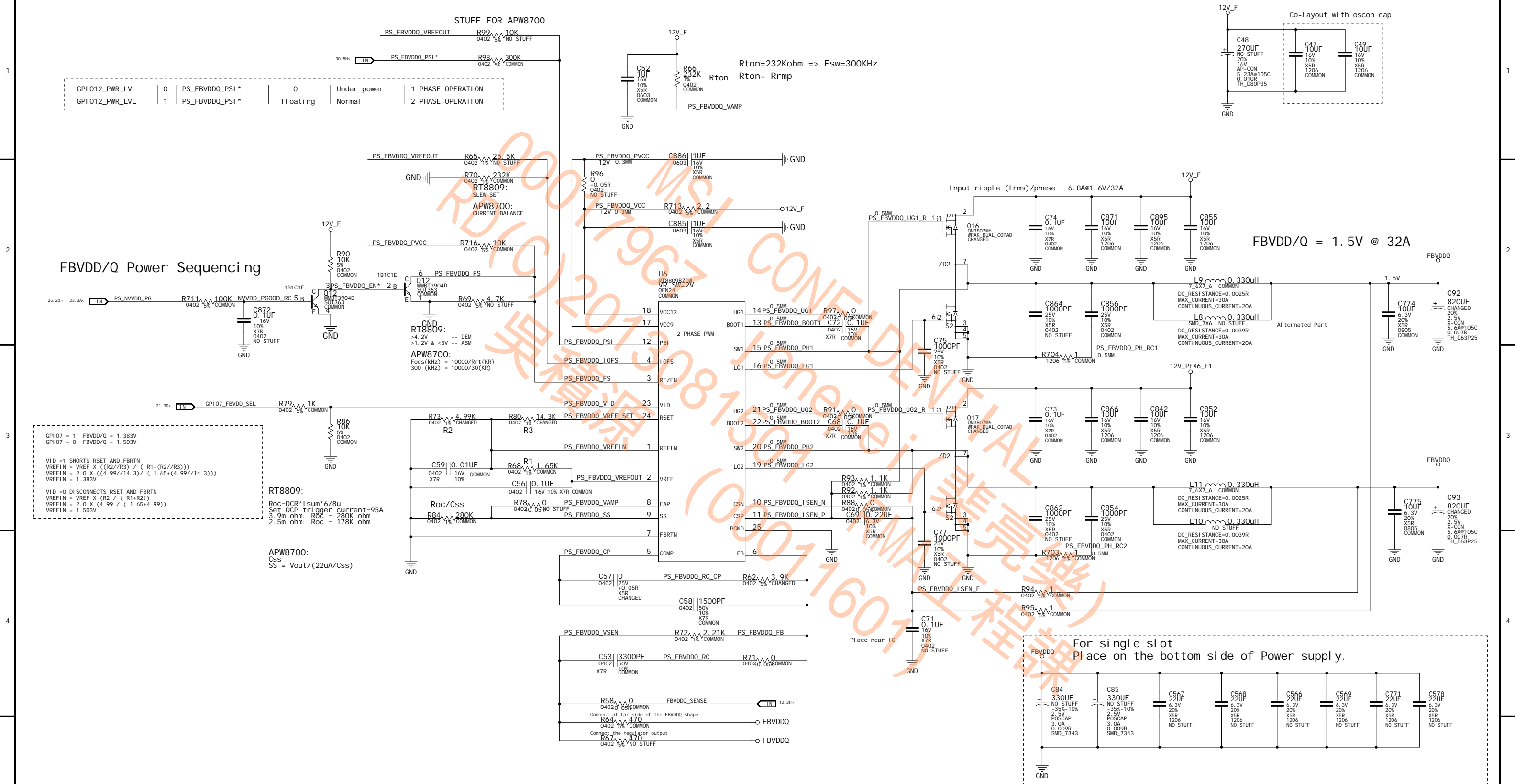
PEXVDD - PEX IOVDD/Q



PEXVDD - PLLVDD & IOVDD/Q



STUFF PEX\_VDD OUTPUT CAPS ABOVE WITH THIS REGULATOR





## Page25: POWER SUPPLY: NVVDD Controller

NVVDD POWER SEQUENCE:

### OPTION1: ONE 12V 6PIN Power Connector

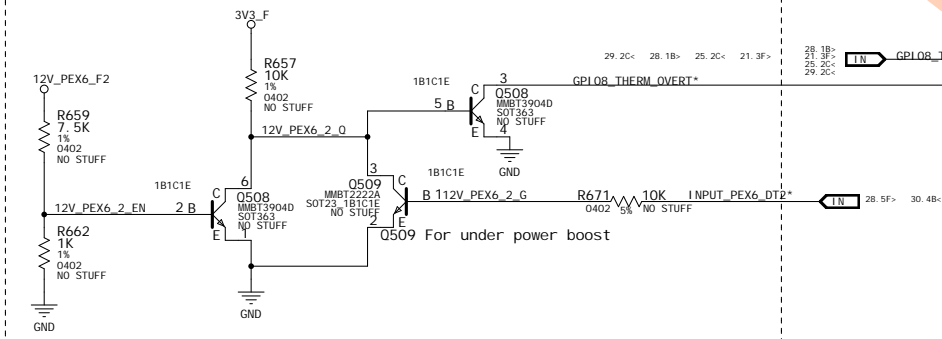
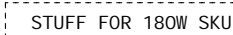
GPI08\_THERM\_OVERT\*(EN): Come from 3V3\_F  
Voltage Monitor: USE NCP5392P to Monitor 12V\_F and 12V\_PEX\_F1

### OPTION2: TWO 12V 6PIN Power ConnectorS

GPI08\_THERM\_OVERT\*(EN): Combine 3V3\_F and 12V\_PEX\_F2  
Voltage Monitor: USE NCP5392P to Monitor 12V\_F and 12V\_PEX\_F1

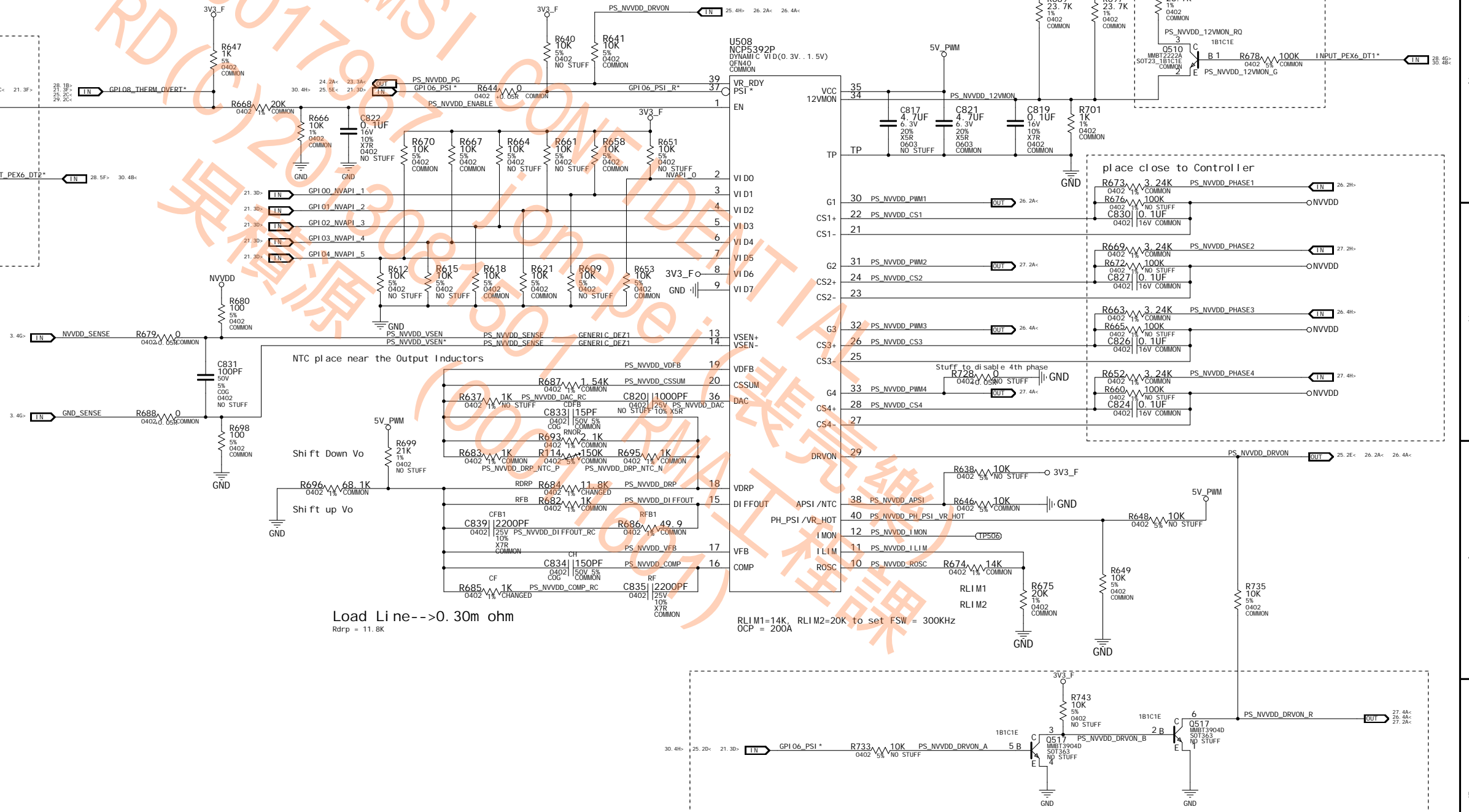
12V\_MON PIN SPEC:  
VH(threshold) = 0.820V (MAX)  
VL(threshold) = 0.640V (MIN)

Stuff these parts if steering no-stuffed  
For under power boost



## VI D Table

GPI 04 VID_5	GPI 03 VID_4	GPI 02 VID_3	GPI 01 VID_2	GPI 00 VID_1	VOUT
0	0	0	0	0	1. 2125V
0	0	0	0	1	1. 2000V
0	0	0	1	0	1. 1875V
0	0	0	1	1	1. 1750V
0	0	1	0	0	1. 1625V
0	0	1	0	1	1. 1500V
0	0	1	1	0	1. 1375V
0	0	1	1	1	1. 1250V
0	1	0	0	0	1. 1125V
0	1	0	0	1	1. 1000V
0	1	0	1	0	1. 0875V
0	1	0	1	1	1. 0750V
0	1	1	0	0	1. 0625V
0	1	1	0	1	1. 0500V
0	1	1	1	0	1. 0375V
0	1	1	1	1	1. 0250V
1	0	0	0	0	1. 0125V
1	0	0	0	1	1. 0000V
1	0	0	1	0	0. 9875V
1	0	0	1	1	0. 9750V
1	0	1	0	0	0. 9625V
1	0	1	0	1	0. 9500V
1	0	1	1	0	0. 9375V
1	0	1	1	1	0. 9250V
1	1	0	0	0	0. 9125V
1	1	0	0	1	0. 9000V
1	1	0	1	0	0. 8875V
1	1	0	1	1	0. 8750V
1	1	1	0	0	0. 8625V
1	1	1	0	1	0. 8500V
1	1	1	1	0	0. 8375V
1	1	1	1	1	0. 8250V



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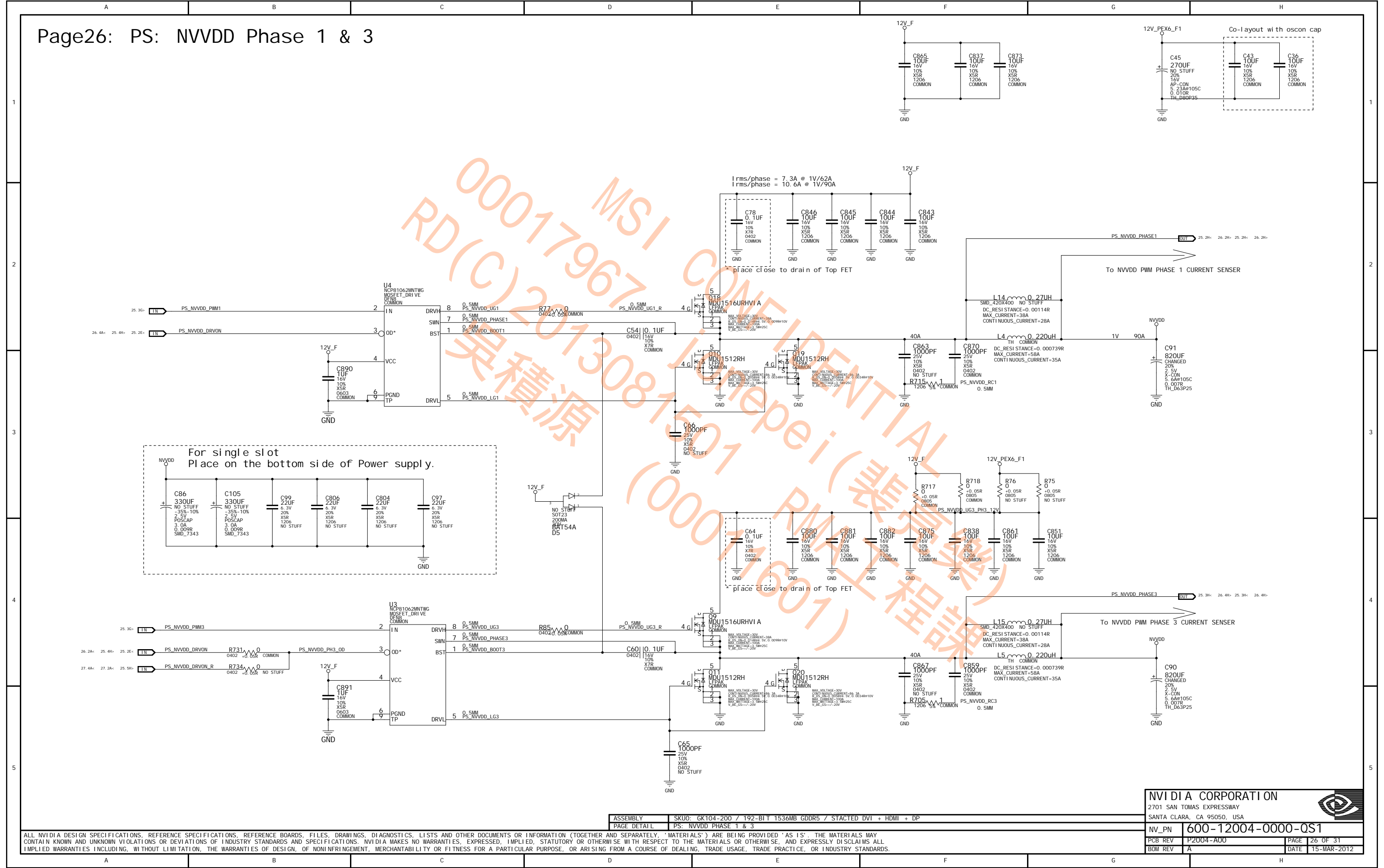
SANTA CLARA, CA 95050, USA

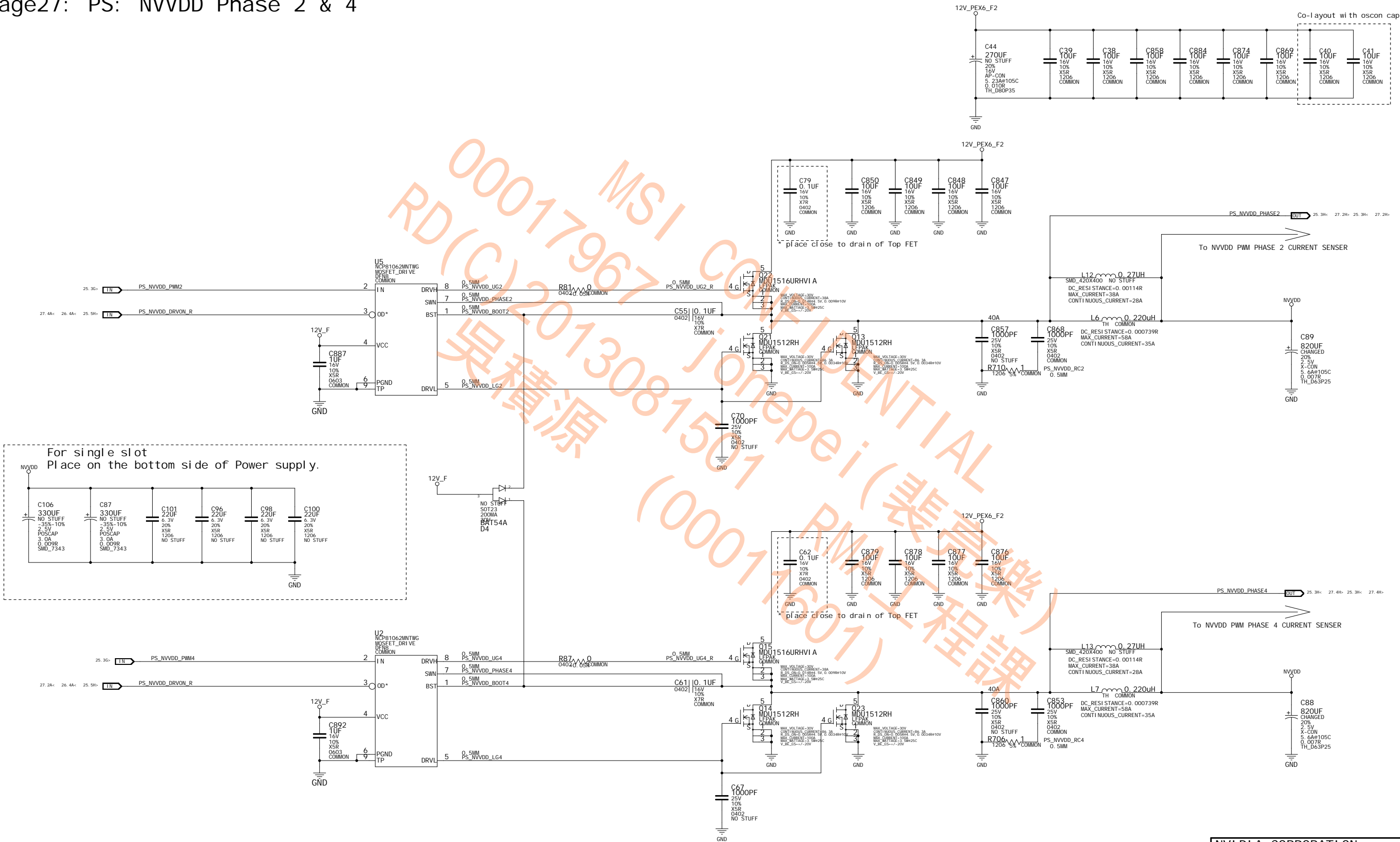
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BOM REV	A	DATE	15-MAR-2012
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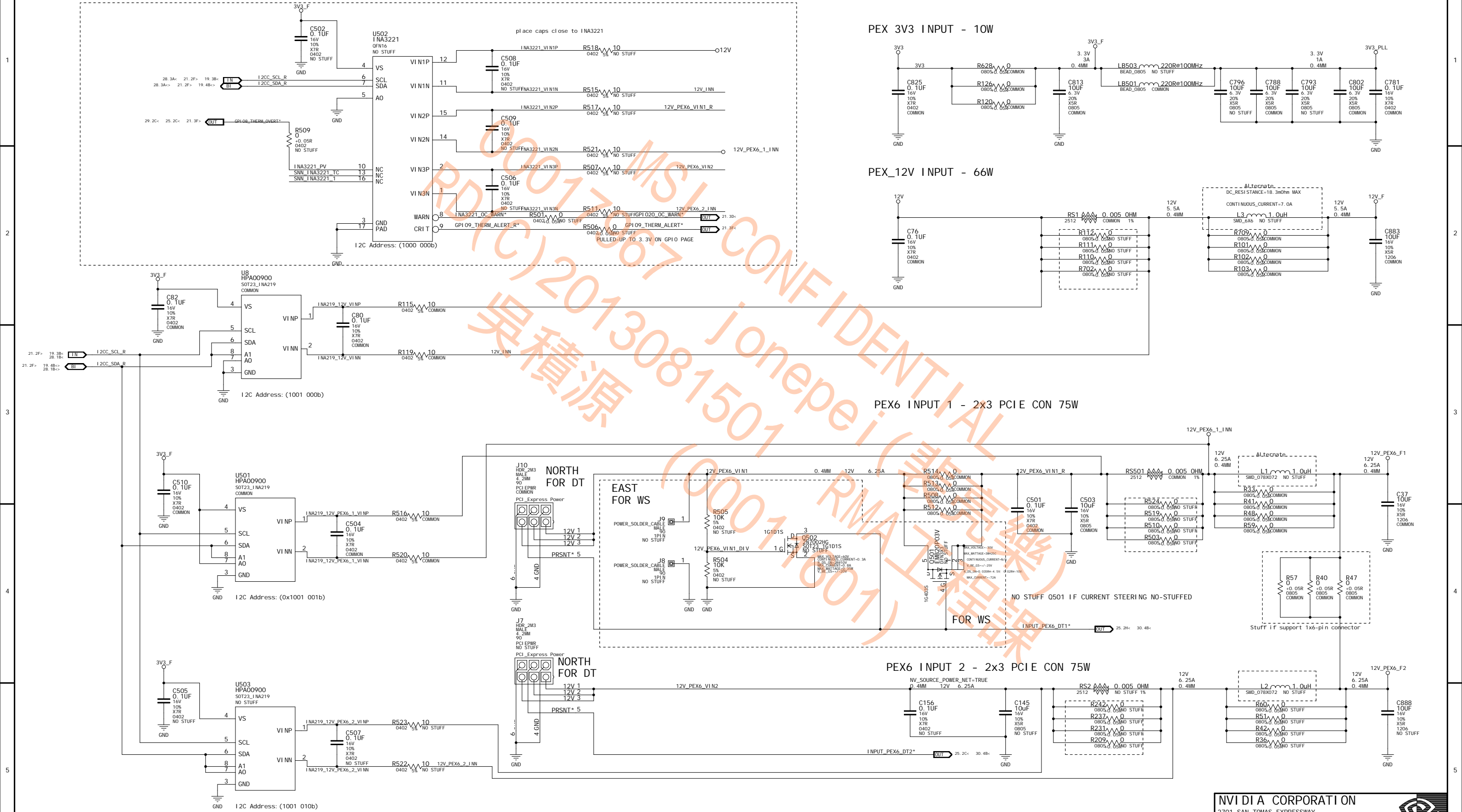
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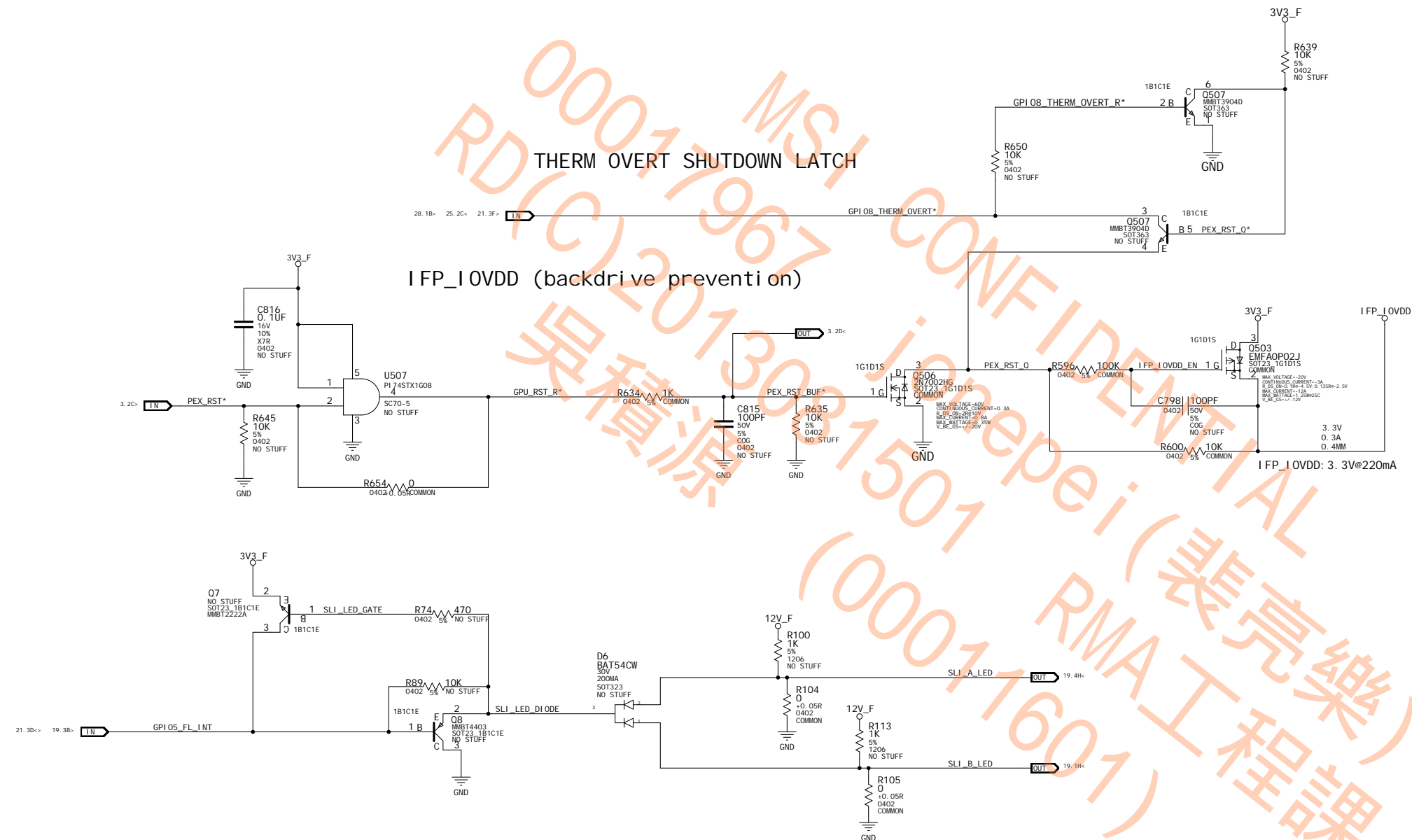


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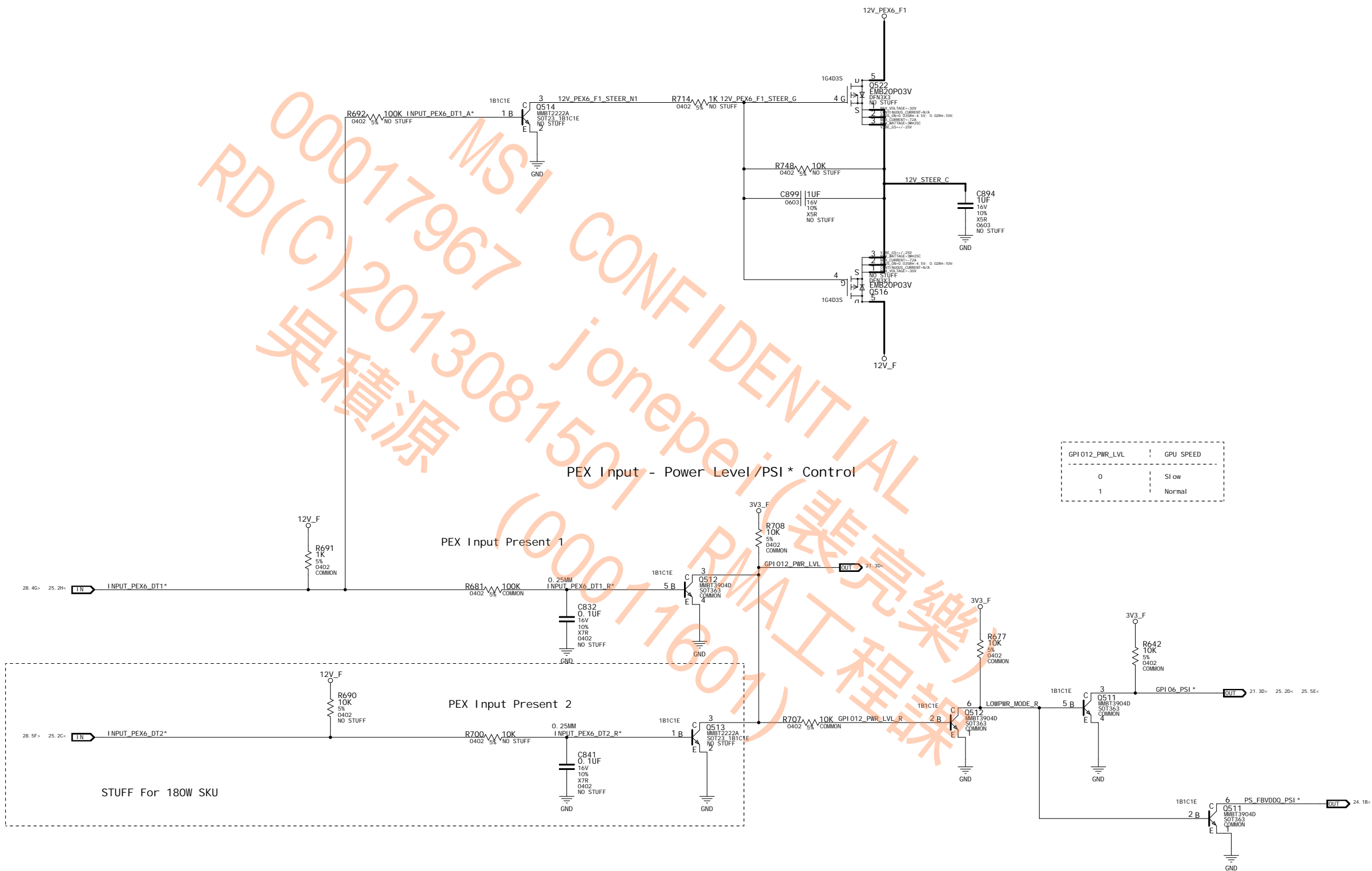
Page28: PS: Inputs, Filtering, and Monitoring



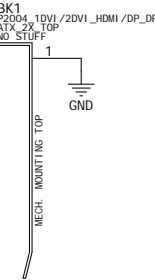




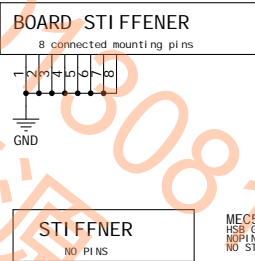
PEX Input - 12V Current Steering FETs



Brackets:



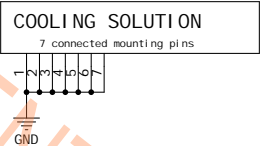
GPU Stiffener:



MEC1  
GPU STIFF\_GK104  
8PIN  
NO STUFF

MEC501  
HSB GK104  
NO PIN  
NO STUFF

MOUNTING HOLES FOR HS:



MEC2  
P2004\_GPU\_HS  
7PIN  
NO STUFF

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