

P690: GT218, DDR3 MEMORY 64MX16/32MX16

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REV	VARIANT	NVPIN	ASSEMBLY
B	BASE	600-10690-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10690-0000-000	GT218-300, 5501375/800, 512MB/64bit, 64MB/16 DDR3, DVI-DL+DP+VGA, DT
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

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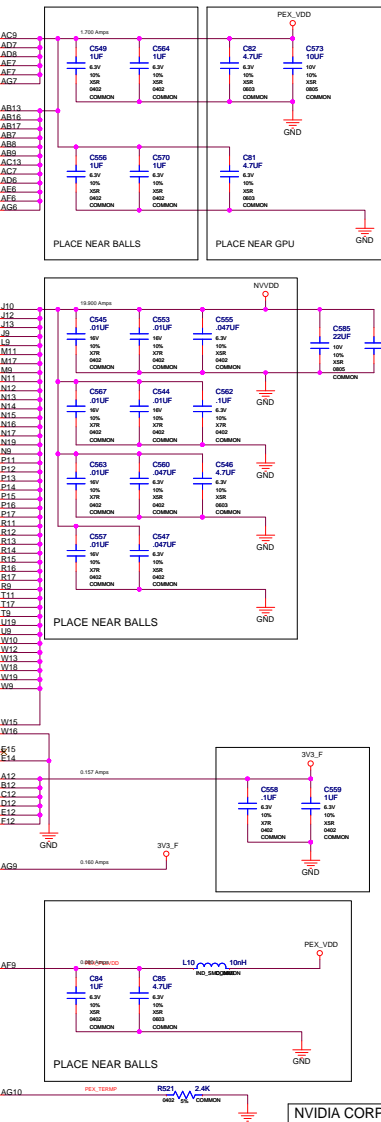
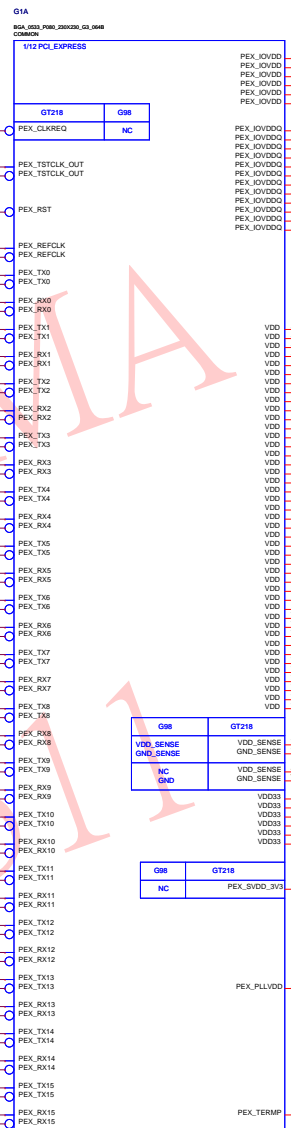
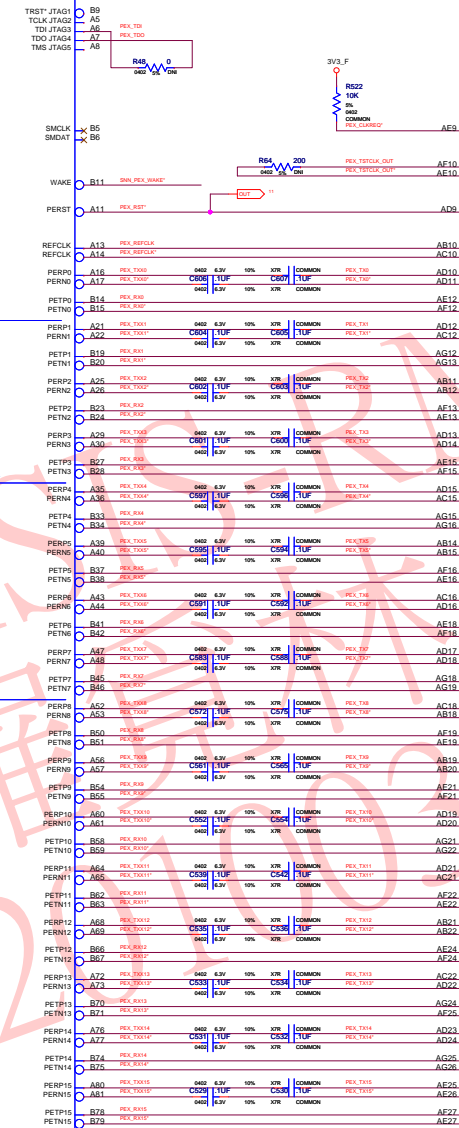
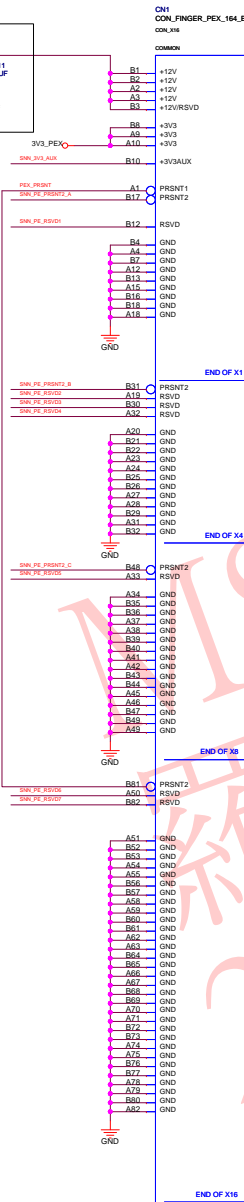
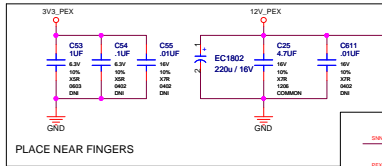
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01-DEC-2008



PCI Express Interface



Net Name

MIN_WIDTH

MAX_WIDTH

IN

PEX_P0P0T

PEX_P0P0B

PEX_P0P0V

PEX_P0P0W

120ML

Net Name

VOLTAGE

MAX_CURRENT

IN

PEX_P0P0T

PEX_P0P0B

PEX_P0P0V

PEX_P0P0W

1.0V


0.000A

120ML

	Net Name	DIFF PAIR	CRITICAL	IMPEDANCE
Differential Pairs	PEX 126	PEX 126	+	0.0017
	PEX 127	PEX 127	+	0.0017
	PEX 128	PEX 128	+	0.0017
	PEX 129	PEX 129	+	0.0017
	PEX 130	PEX 130	+	0.0017
	PEX 131	PEX 131	+	0.0017
	PEX 132	PEX 132	+	0.0017
	PEX 133	PEX 133	+	0.0017
	PEX 134	PEX 134	+	0.0017
	PEX 135	PEX 135	+	0.0017
	PEX 136	PEX 136	+	0.0017
	PEX 137	PEX 137	+	0.0017
	PEX 138	PEX 138	+	0.0017
	PEX 139	PEX 139	+	0.0017
	PEX 140	PEX 140	+	0.0017
	PEX 141	PEX 141	+	0.0017
	PEX 142	PEX 142	+	0.0017
	PEX 143	PEX 143	+	0.0017
	PEX 144	PEX 144	+	0.0017
	PEX 145	PEX 145	+	0.0017
	PEX 146	PEX 146	+	0.0017
	PEX 147	PEX 147	+	0.0017
	PEX 148	PEX 148	+	0.0017
	PEX 149	PEX 149	+	0.0017
	PEX 150	PEX 150	+	0.0017
	PEX 151	PEX 151	+	0.0017
	PEX 152	PEX 152	+	0.0017
	PEX 153	PEX 153	+	0.0017
	PEX 154	PEX 154	+	0.0017
	PEX 155	PEX 155	+	0.0017
	PEX 156	PEX 156	+	0.0017
	Differential Pairs	PEX 156	PEX 156	+
PEX 157		PEX 157	+	0.0017
PEX 158		PEX 158	+	0.0017
PEX 159		PEX 159	+	0.0017
PEX 160		PEX 160	+	0.0017
PEX 161		PEX 161	+	0.0017
PEX 162		PEX 162	+	0.0017
PEX 163		PEX 163	+	0.0017
PEX 164		PEX 164	+	0.0017
PEX 165		PEX 165	+	0.0017
PEX 166		PEX 166	+	0.0017
PEX 167		PEX 167	+	0.0017
PEX 168		PEX 168	+	0.0017
PEX 169		PEX 169	+	0.0017
PEX 170		PEX 170	+	0.0017
PEX 171		PEX 171	+	0.0017
PEX 172		PEX 172	+	0.0017
PEX 173		PEX 173	+	0.0017
PEX 174		PEX 174	+	0.0017
PEX 175		PEX 175	+	0.0017
PEX 176		PEX 176	+	0.0017
PEX 177		PEX 177	+	0.0017
PEX 178		PEX 178	+	0.0017
PEX 179		PEX 179	+	0.0017
PEX 180		PEX 180	+	0.0017
PEX 181		PEX 181	+	0.0017
PEX 182		PEX 182	+	0.0017
PEX 183		PEX 183	+	0.0017
PEX 184		PEX 184	+	0.0017
PEX 185		PEX 185	+	0.0017
PEX 186		PEX 186	+	0.0017
PEX 187		PEX 187	+	0.0017
PEX 188	PEX 188	+	0.0017	
PEX 189	PEX 189	+	0.0017	
PEX 190	PEX 190	+	0.0017	
PEX 191	PEX 191	+	0.0017	
PEX 192	PEX 192	+	0.0017	
PEX 193	PEX 193	+	0.0017	
PEX 194	PEX 194	+	0.0017	
PEX 195	PEX 195	+	0.0017	
PEX 196	PEX 196	+	0.0017	
PEX 197	PEX 197	+	0.0017	
PEX 198	PEX 198	+	0.0017	
PEX 199	PEX 199	+	0.0017	
PEX 200	PEX 200	+	0.0017	
PEX 201	PEX 201	+	0.0017	
PEX 202	PEX 202	+	0.0017	
PEX 203	PEX 203	+	0.0017	
PEX 204	PEX 204	+	0.0017	
PEX 205	PEX 205	+	0.0017	
PEX 206	PEX 206	+	0.0017	
PEX 207	PEX 207	+	0.0017	
PEX 208	PEX 208	+	0.0017	
PEX 209	PEX 209	+	0.0017	
PEX 210	PEX 210	+	0.0017	
PEX 211	PEX 211	+	0.0017	
PEX 212	PEX 212	+	0.0017	
PEX 213	PEX 213	+	0.0017	
PEX 214	PEX 214	+	0.0017	
PEX 215	PEX 215	+	0.0017	
PEX 216	PEX 216	+	0.0017	
PEX 217	PEX 217	+	0.0017	
PEX 218	PEX 218	+	0.0017	
PEX 219	PEX 219	+	0.0017	
PEX 220	PEX 220	+	0.0017	
Differential Pairs	PEX 220A	PEX 220A	+	0.0017
	PEX 220B	PEX 220B	+	0.0017
	PEX 220C	PEX 220C	+	0.0017
	PEX 220D	PEX 220D	+	0.0017
	PEX 220E	PEX 220E	+	0.0017

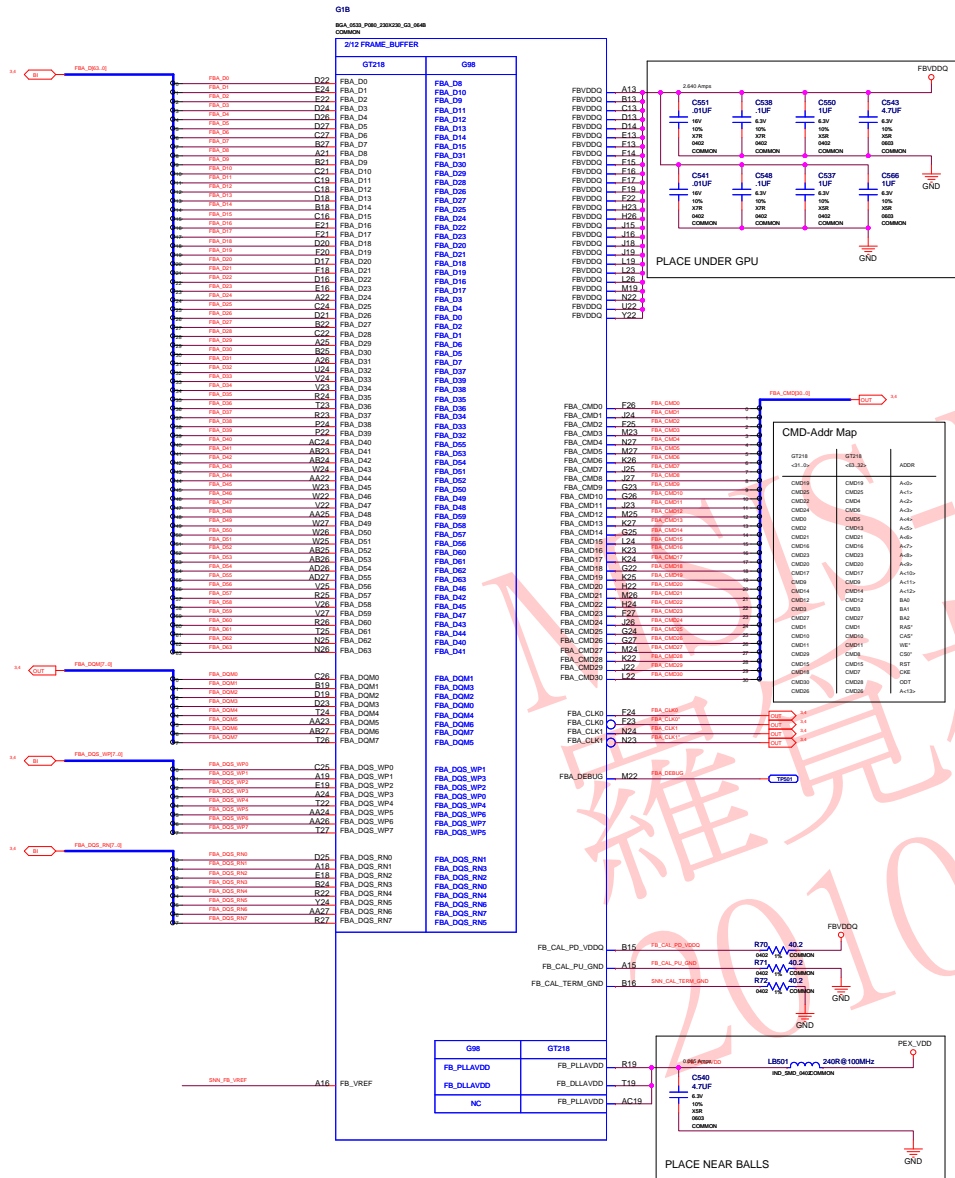
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express Interface

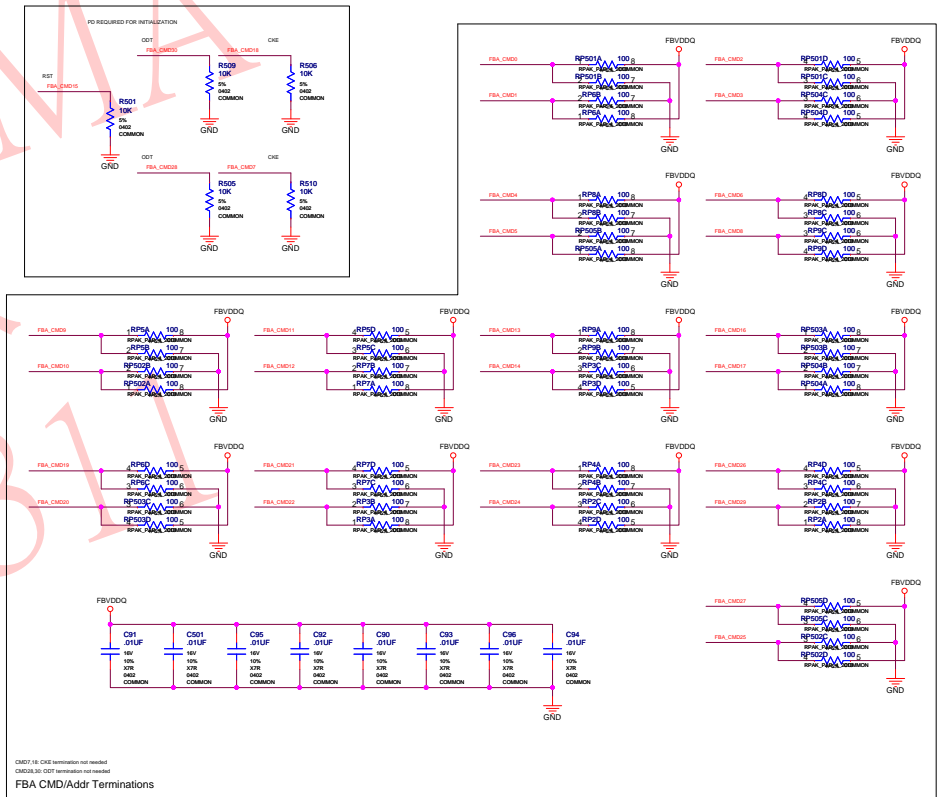
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NV_PN	600-10690-BASE-000 A		
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NAME		DATE	01-DEC-2008



Frame Buffer Interface



Net Name		DIFF_PAIR	CRITICAL	IMPEDANCE
0.4	FRA_DDR05_05	+	2	40.00Ω
0.4	FRA_DDR05_06	+	2	40.00Ω
0.4	FRA_DDR05_07	+	2	40.00Ω
0.4	FRA_DDR05_08	+	2	40.00Ω
0.4	FRA_DDR05_09	+	2	40.00Ω
0.4	FRA_DDR05_10	+	2	40.00Ω
0.4	FRA_DDR05_11	+	2	40.00Ω
0.4	FRA_DDR05_12	+	2	40.00Ω
0.4	FRA_DDR05_13	+	2	40.00Ω
0.4	FRA_DDR05_14	+	2	40.00Ω
0.4	FRA_DDR05_15	+	2	40.00Ω
0.4	FRA_DDR05_16	+	2	40.00Ω
0.4	FRA_DDR05_17	+	2	40.00Ω
0.4	FRA_DDR05_18	+	2	40.00Ω
0.4	FRA_DDR05_19	+	2	40.00Ω
0.4	FRA_DDR05_20	+	2	40.00Ω
0.4	FRA_DDR05_21	+	2	40.00Ω
0.4	FRA_DDR05_22	+	2	40.00Ω
0.4	FRA_DDR05_23	+	2	40.00Ω
0.4	FRA_DDR05_24	+	2	40.00Ω
0.4	FRA_DDR05_25	+	2	40.00Ω
0.4	FRA_DDR05_26	+	2	40.00Ω
0.4	FRA_DDR05_27	+	2	40.00Ω
0.4	FRA_DDR05_28	+	2	40.00Ω
0.4	FRA_DDR05_29	+	2	40.00Ω
0.4	FRA_DDR05_30	+	2	40.00Ω
0.4	FRA_DDR05_31	+	2	40.00Ω
0.4	FRA_DDR05_32	+	2	40.00Ω
0.4	FRA_DDR05_33	+	2	40.00Ω
0.4	FRA_DDR05_34	+	2	40.00Ω
0.4	FRA_DDR05_35	+	2	40.00Ω
0.4	FRA_DDR05_36	+	2	40.00Ω
0.4	FRA_DDR05_37	+	2	40.00Ω
0.4	FRA_DDR05_38	+	2	40.00Ω
0.4	FRA_DDR05_39	+	2	40.00Ω
0.4	FRA_DDR05_40	+	2	40.00Ω
0.4	FRA_DDR05_41	+	2	40.00Ω
0.4	FRA_DDR05_42	+	2	40.00Ω
0.4	FRA_DDR05_43	+	2	40.00Ω
0.4	FRA_DDR05_44	+	2	40.00Ω
0.4	FRA_DDR05_45	+	2	40.00Ω
0.4	FRA_DDR05_46	+	2	40.00Ω
0.4	FRA_DDR05_47	+	2	40.00Ω
0.4	FRA_DDR05_48	+	2	40.00Ω
0.4	FRA_DDR05_49	+	2	40.00Ω
0.4	FRA_DDR05_50	+	2	40.00Ω
0.4	FRA_DDR05_51	+	2	40.00Ω
0.4	FRA_DDR05_52	+	2	40.00Ω
0.4	FRA_DDR05_53	+	2	40.00Ω
0.4	FRA_DDR05_54	+	2	40.00Ω
0.4	FRA_DDR05_55	+	2	40.00Ω
0.4	FRA_DDR05_56	+	2	40.00Ω
0.4	FRA_DDR05_57	+	2	40.00Ω
0.4	FRA_DDR05_58	+	2	40.00Ω
0.4	FRA_DDR05_59	+	2	40.00Ω
0.4	FRA_DDR05_60	+	2	40.00Ω
0.4	FRA_DDR05_61	+	2	40.00Ω
0.4	FRA_DDR05_62	+	2	40.00Ω
0.4	FRA_DDR05_63	+	2	40.00Ω
0.4	FRA_DDR05_64	+	2	40.00Ω
0.4	FRA_DDR05_65	+	2	40.00Ω
0.4	FRA_DDR05_66	+	2	40.00Ω
0.4	FRA_DDR05_67	+	2	40.00Ω
0.4	FRA_DDR05_68	+	2	40.00Ω
0.4	FRA_DDR05_69	+	2	40.00Ω
0.4	FRA_DDR05_70	+	2	40.00Ω
0.4	FRA_DDR05_71	+	2	40.00Ω
0.4	FRA_DDR05_72	+	2	40.00Ω
0.4	FRA_DDR05_73	+	2	40.00Ω
0.4	FRA_DDR05_74	+	2	40.00Ω
0.4	FRA_DDR05_75	+	2	40.00Ω
0.4	FRA_DDR05_76	+	2	40.00Ω
0.4	FRA_DDR05_77	+	2	40.00Ω
0.4	FRA_DDR05_78	+	2	40.00Ω
0.4	FRA_DDR05_79	+	2	4



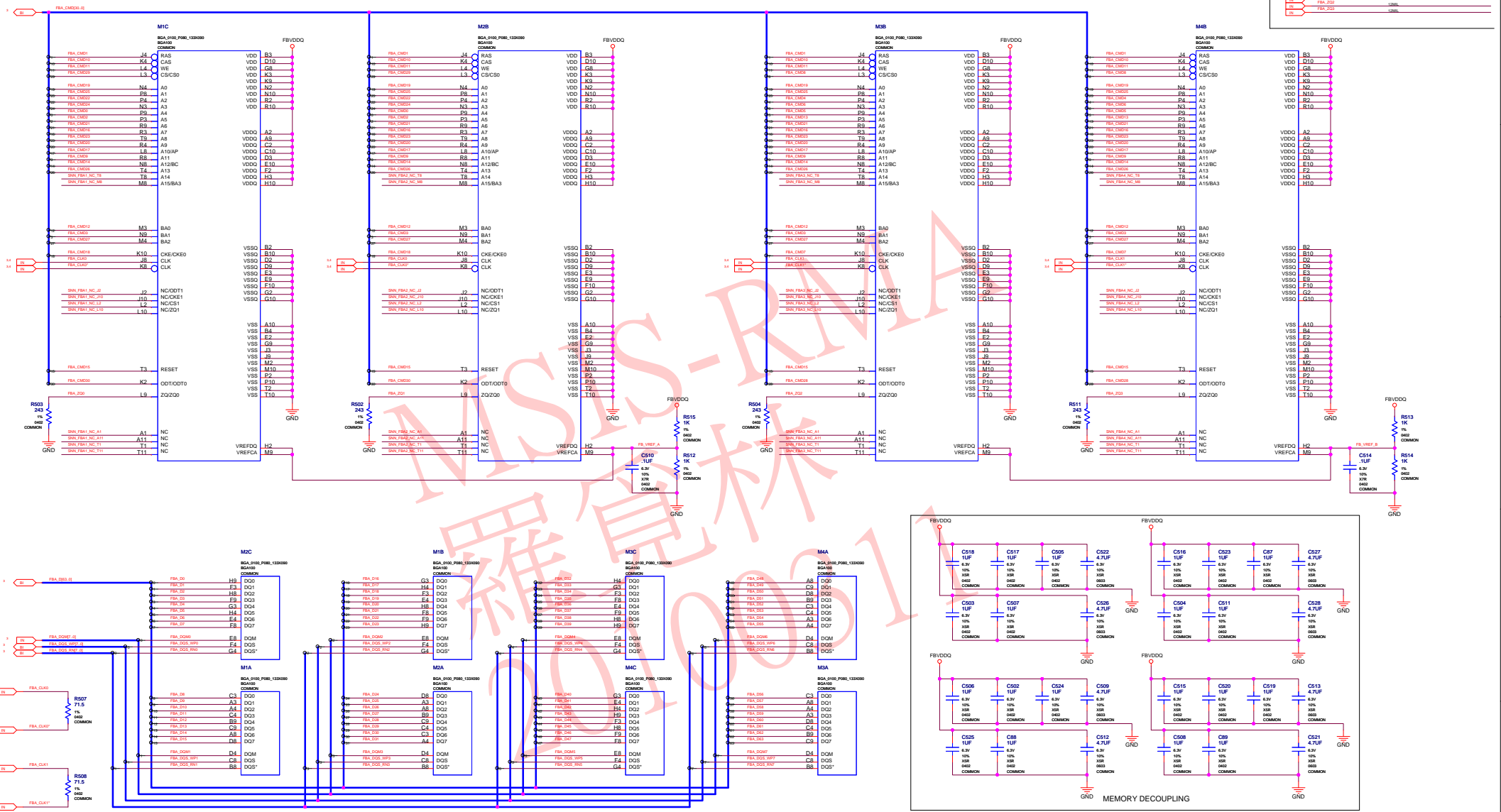
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PAGE DETAIL	Frame Buffer Interface

FBA CMD/Addr Termination

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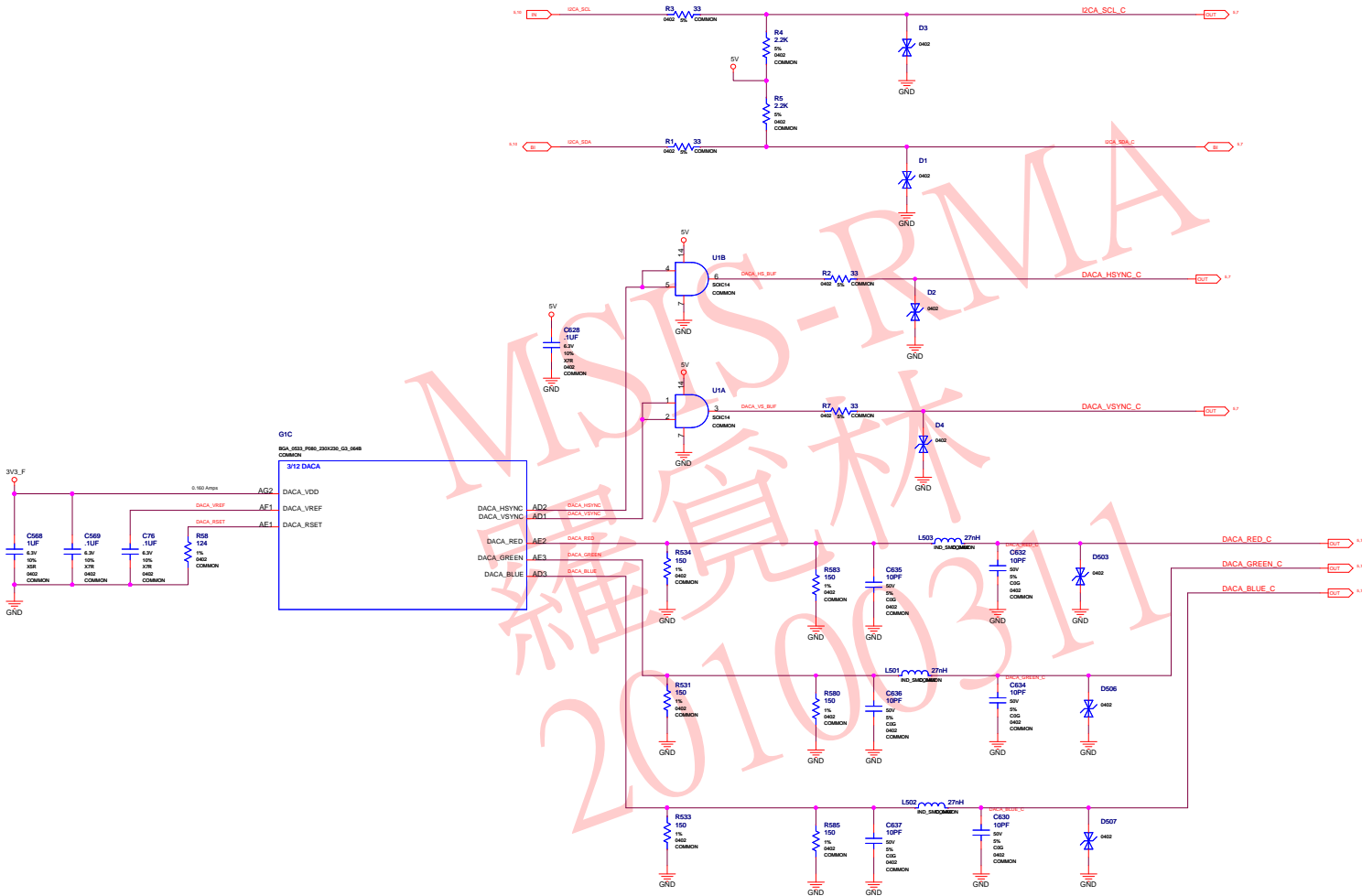
A	B	C	D	E	F	G	H
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DDR3 Memories



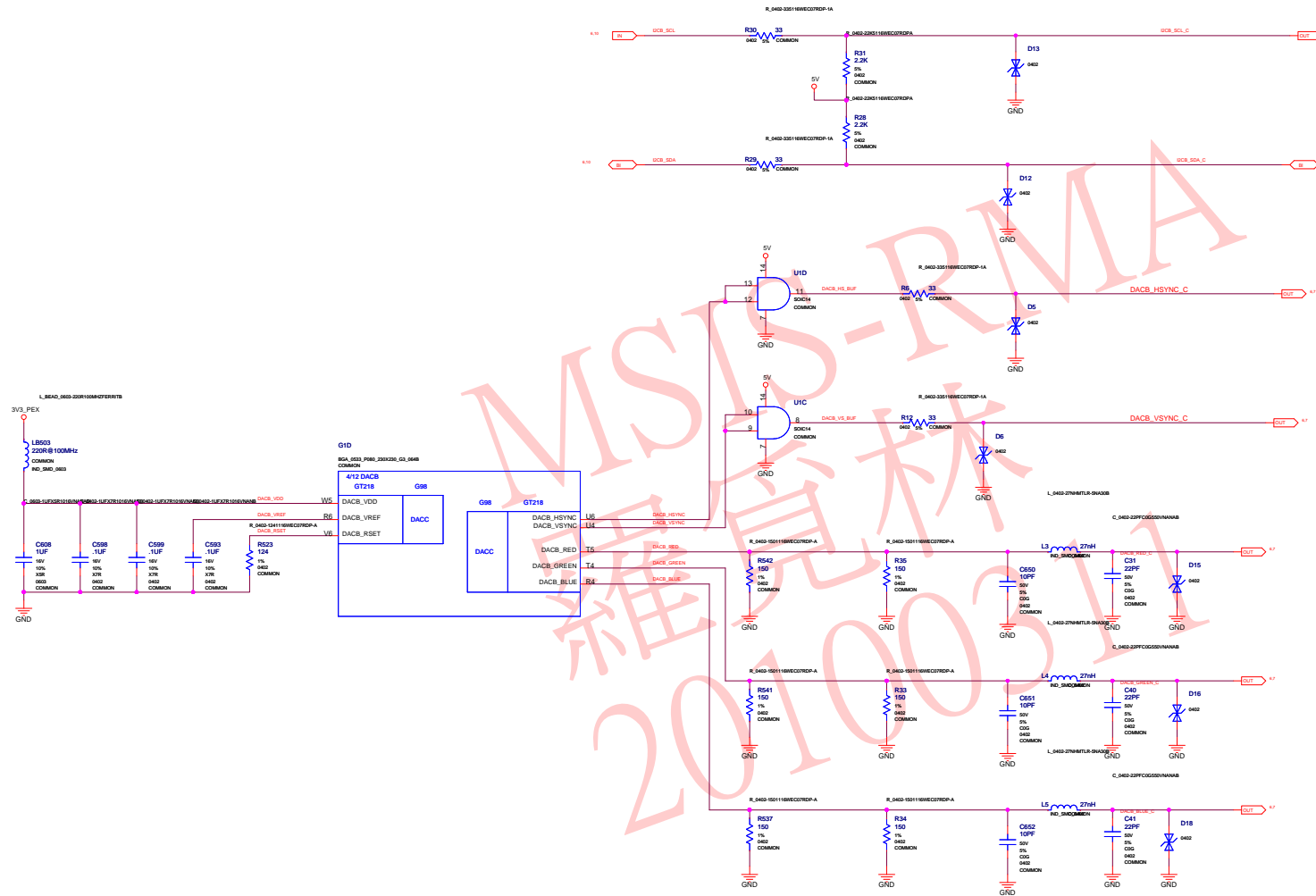
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DAC A Slim VGA



Net Name		CRITICAL	IMPEDANCE
13	DACA_RED	1	50Ω
14	DACA_GREEN	1	50Ω
15	DACA_BLUE	1	50Ω
16	DACA_RED_0'	1	50Ω
17	DACA_GREEN_0'	1	50Ω
18	DACA_BLUE_0'	1	50Ω
19	DACA_HSYNC	2	50Ω
20	DACA_VSYNC	2	50Ω
21	DACA_VDD_BUF	2	50Ω
22	DACA_VDD_BUF	2	50Ω
23	DACA_VSYNC_0'	2	50Ω
24	DACA_VSYNC_0'	2	50Ω
Net Name		MIN_WIDTH	MAX_WIDTH
130	DACA_SCL		
131	DACA_SDA		
132	DACA_SCL_0'		
133	DACA_SDA_0'		
Net Name		VOLTAGE	MAX_CURRENT
134	DACA_VREF	1.2V	1300mA
135	DACA_VDD0V1		1300mA

DAC B VGA Header

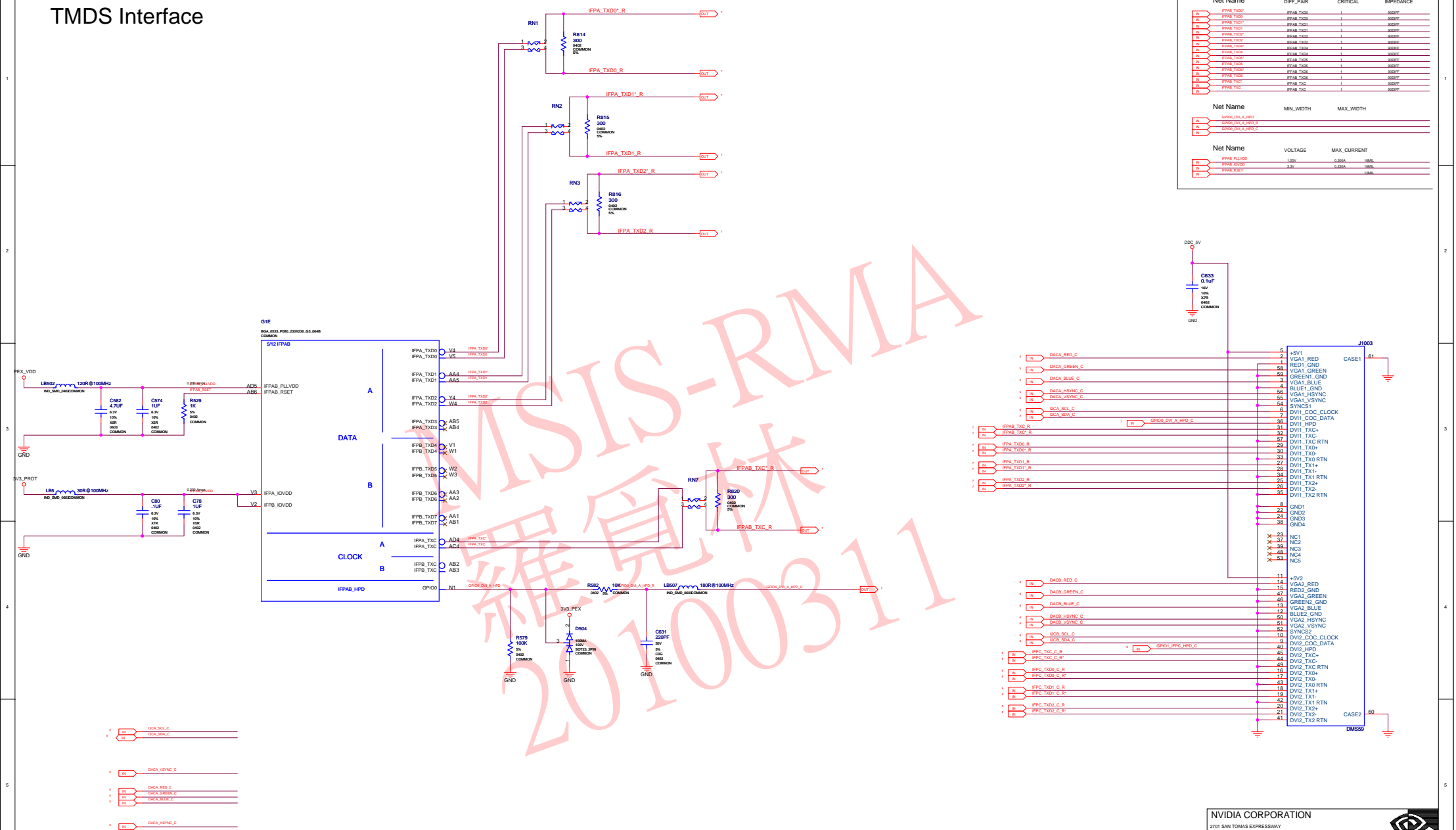



Net Name		CRITICAL	IMPEDANCE
(H)	DACR_RED	1	50Ω±1%
(H)	DACR_GREEN	1	50Ω±1%
(H)	DACR_BLUE	1	50Ω±1%
(H)	DACR_RED_C	1	50Ω±1%
(H)	DACR_GREEN_C	1	50Ω±1%
(H)	DACR_BLUE_C	1	50Ω±1%
(H)	DACR_HVING	2	50Ω±1%
(H)	DACR_VSING	2	50Ω±1%
(H)	DACR_HVING_C	2	50Ω±1%
(H)	DACR_VSING_C	2	50Ω±1%
(H)	DACR_HS_BUF	2	50Ω±1%
(H)	DACR_VS_BUF	2	50Ω±1%

Net Name		MIN_WIDTH	MAX_WIDTH
6.10	IN	12CB_SCL	
	IN	12CB_SDA	
6.10	SI	12CB_SCL_C	
	IN	12CB_SDA_C	
	IN		

Net Name	VOLTAGE	MAX_CURRENT
IN	DACB_VREF	1.2V
IN	DACB_ISET	125mA

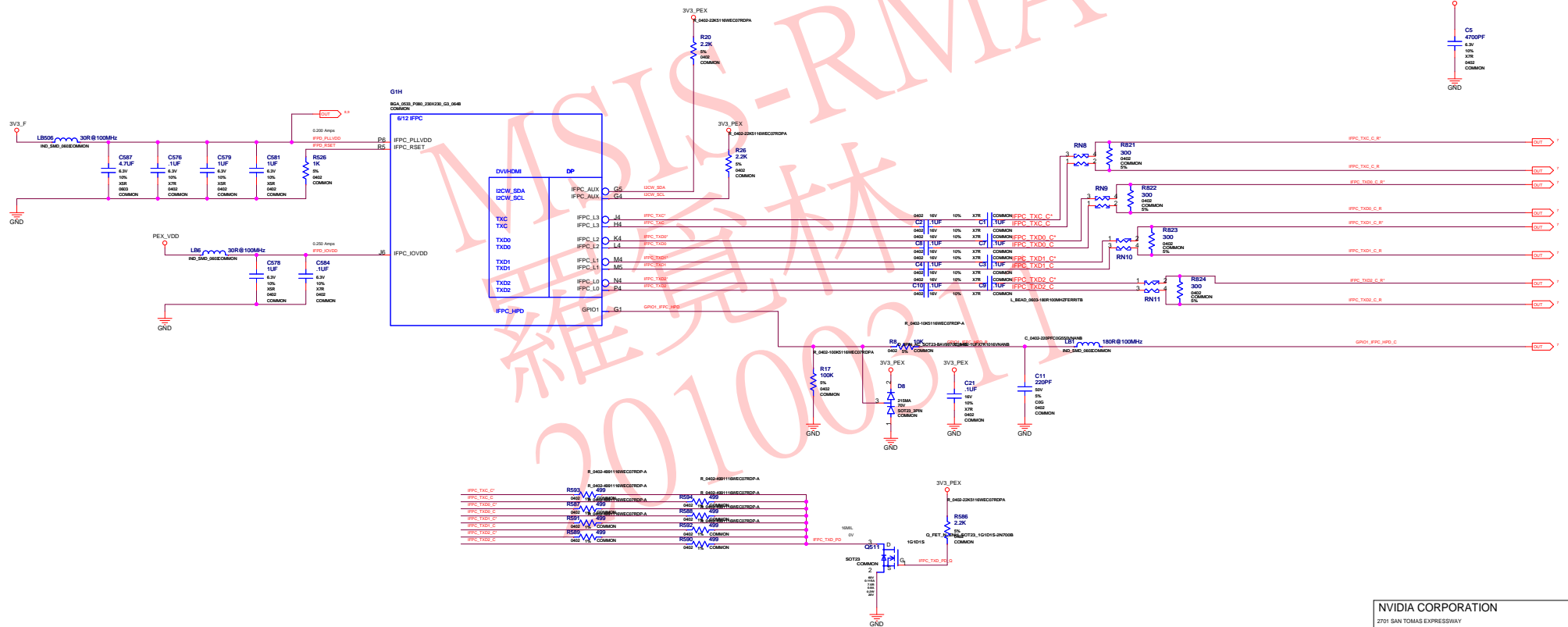
TMDS Interface




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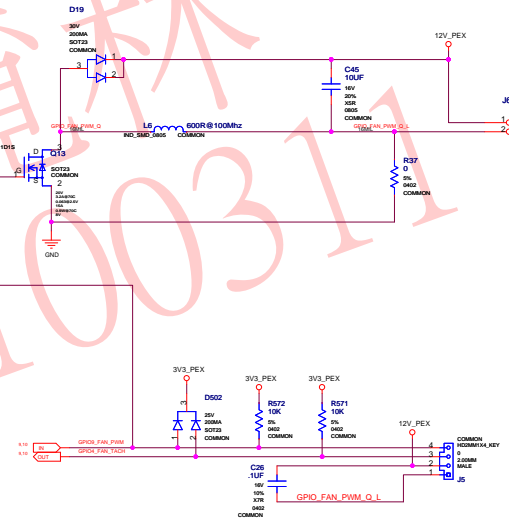
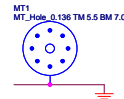
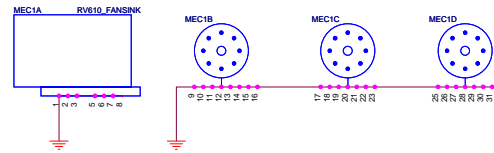
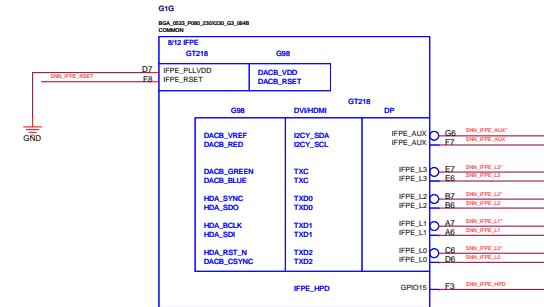
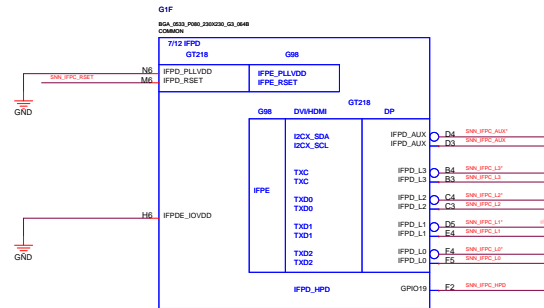
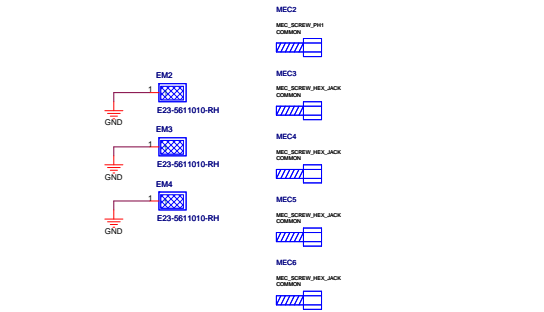
Link C

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IFPC, IFPE Interface, Fan, Mechanical



Net Name

	VOLTAGE	MAX_CURRENT
IN IPFC_FLU_ID	3.3V	0.200A
IN IPFC_CHRD	1.20V	0.00A

Net Name

	MIN_WIDTH	MAX_WIDTH
IN GRPC_FAN_TACH	4.10	4.10
OUT GRPC_FAN_PWM	4.10	4.10

G11		BGA_0025_F001_20X220_01_0040	
CONNECTION			
12/12 GND_NC			
AC11 GND		NC	C15 0000 GP15_015
AC14 GND		NC	D15 0000 GP15_015
AC12 GND		NC	J5 0000 GP15_015
AC2 GND			
AC20 GND			
AC21 GND			
AC26 GND			
AC5 GND			
AC8 GND			
AF11 GND			
AF14 GND			
AF17 GND			
AF5 GND			
AF20 GND			
AF21 GND			
AF26 GND			
AF5 GND			
AF8 GND			
B11 GND			
B14 GND			
B17 GND			
B2 GND			
B20 GND			
B21 GND			
B23 GND			
B26 GND			
B5 GND			
B6 GND			
E11 GND			
E17 GND			
E2 GND			
E26 GND			
E22 GND			
E28 GND			
E4 GND			
E8 GND			
H2 GND			
H5 GND			
J11 GND			
J14 GND			
J17 GND			
K18 GND			
K8 GND			
L11 GND			
L12 GND			
L13 GND			
L14 GND			
L15 GND			
L16 GND			
L17 GND			
L2 GND			
L6 GND			
M2 GND			
M13 GND			
M14 GND			
M15 GND			
M16 GND			
P18 GND			
P2 GND			
P21 GND			
P26 GND			
P5 GND			
P9 GND			
T12 GND			
T13 GND			
T14 GND			
T15 GND			
T16 GND			
U11 GND			
U12 GND			
U13 GND			
U14 GND			
U15 GND			
U16 GND			
U17 GND			
U2 GND			
U21 GND			
U26 GND			
U5 GND			
U6 GND			
U18 GND			
U19 GND			
W11 GND			
W14 GND			
W17 GND			
Y2 GND			
Y26 GND			
Y5 GND			
Y6 GND			
Y8 GND			
GND			

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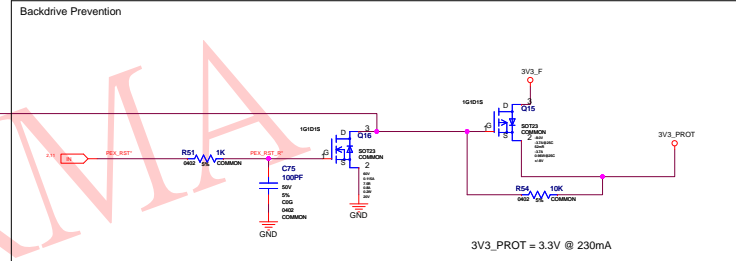
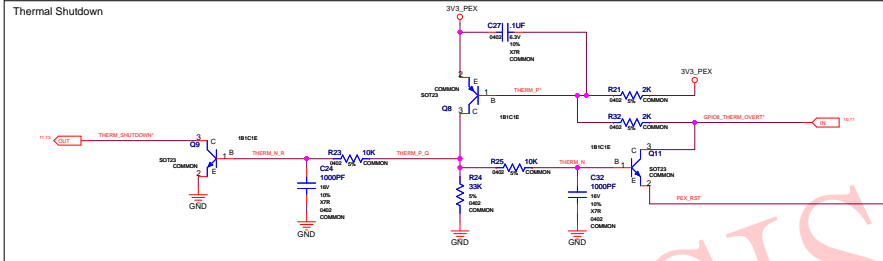
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PAGE DETAIL	IFPC, IFPE Interface, Fan, Mechanical

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Thermal Protection, IFP_IOVDD, Straps

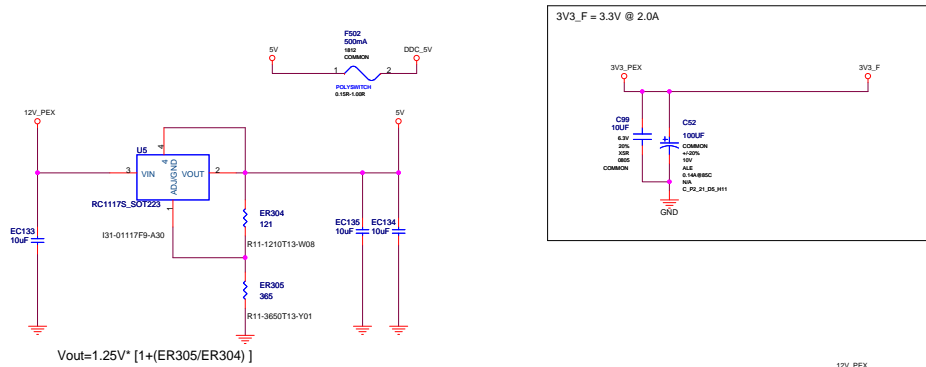


GT218 Straps MLS Mode		Values		Multilevel Straps	
03	RAMCQ1Q2	0000	Empty		
02	RAMCQ1	0001	Sampling Memory		
03	RAMCQ2	0010	Geometry		
01	RAMCQ1Q2	0011	Flags		
03	RAMCQ2	0020	History		
02	ICGA_HF7	0	777 (Default)	56 16 QAO	0000
				106 16 QAO	0001
				126 16 QAO	0010
				136 16 QAO	0011
				236 16 QAO	0100
				256 16 QAO	0101
02	FREEI	0	256M (Default)	4096 16 QAO	0110
				8K 16 VCC	1000
01	DAB_LA_T_ADDR	0	DABT	10K 16 VCC	1001
		1	DABT	16K 16 VCC	1010
02	VISA_DEVICE	0	Class mode 385	32K 16 VCC	1100
		1	Class mode 300	256K 16 VCC	1101
				32K 16 VCC	1110
				256K 16 VCC	1111
03	PCI_LBHD_EXT	0	GT218-300-A1		
02	SVL_VENDOR	0	No BIOS		
		1	BIOS		
01	SLUT_CSK_CPS	0	Disable		
		1	Enable		
02	PEX_PLL_2N_TERM100	0	Disable		
		1	Enable		
03	PCI_DEV1Q3	0000	GT218-300-A1		
02	PCI_DEV1Q2				
01	PCI_DEV1Q1				
03	PCI_DEV1Q3				
02	SDIO_PIOCFG_LUT_ADDR0	0000	DISKTOP_PIOCFG	1000	DISKTOP_PIOCFG
01	SDIO_PIOCFG_LUT_ADDR1	0001	MOBILE_PIOCFG_DEFAULT	1001	MOBILE_PIOCFG_NANP
02	SDIO_PIOCFG_LUT_ADDR2	0010	MOBILE_PIOCFG_LAMP	1010	MOBILE_PIOCFG_LAMP
01	SDIO_PIOCFG_LUT_ADDR3	0011	MOBILE_PIOCFG_LAMP	1011	MOBILE_PIOCFG_LAMP
02	SDIO_PIOCFG_LUT_ADDR4	0100	MOBILE_PIOCFG_LAMP	1100	MOBILE_PIOCFG_LAMP
01	SDIO_PIOCFG_LUT_ADDR5	0101	MOBILE_PIOCFG_LAMP	1101	MOBILE_PIOCFG_LAMP
02	SDIO_PIOCFG_LUT_ADDR6	0110	MOBILE_PIOCFG_LAMP	1110	MOBILE_PIOCFG_LAMP
01	SDIO_PIOCFG_LUT_ADDR7	0111	MOBILE_PIOCFG_LAMP	1111	MOBILE_PIOCFG_LAMP
03	USERCFG	0000	Default		
02	USERCFG2				
01	USERCFG1				
03	USERCFG				

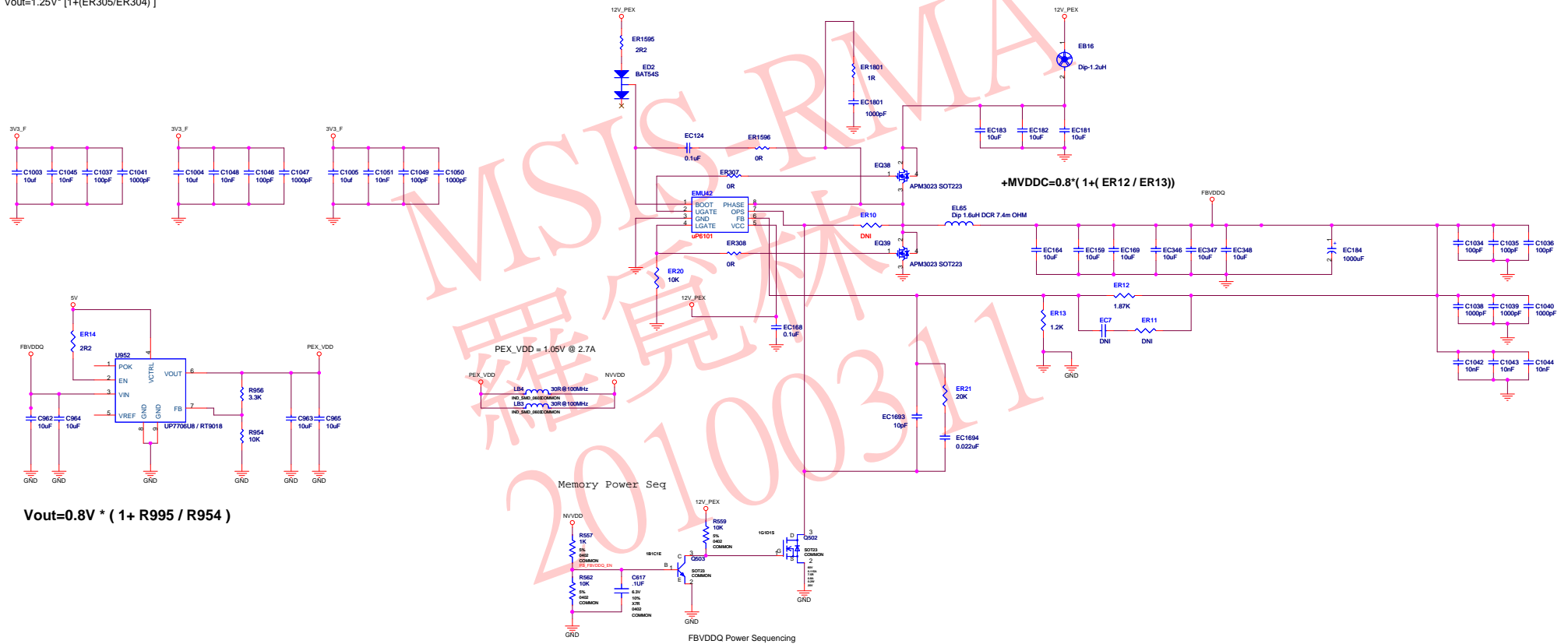
GT218 Straps		
BU Mode		
Bit Signal	Values	
PCLE_DEV0_EXT	0	GT218-30A-01
SCC_A_H7	0	277 (Default)
SGIO_PADCFG_LUT_ADDR0	0000	DS2TOP_DEFAULT
	0001	MOBILE_DEFAULT
	0009	MOBILE_HTTFS_LAMP
	0011	MOBILE_HTTFS_LAMP
	0100	MOBILE_HTTFS_LAMP
	0104	MOBILE_HTTFS_LAMP
	0110	MOBILE_HTTFS_LAMP
	0111	MOBILE_HTTFS_LAMP
	1000	DS2TOP_HTTFS
	1001	MOBILE_HTTFS_LAMP
	1010	MOBILE_HTTFS_LAMP
	1011	MOBILE_HTTFS_LAMP
SGIO_PADCFG_LUT_ADDR0	1100	MOBILE_HTTFS_LAMP
	1101	MOBILE_HTTFS_LAMP
	1110	MOBILE_HTTFS_LAMP
	1111	MOBILE_HTTFS_LAMP
SGIO_PADCFG_LUT_ADDR1		
SGIO_PADCFG_LUT_ADDR2		

GT218 Straps	
PM Mode	
Bit Signal	Values
PCI_DEVIDE_EXT	0 GT218-300-A1
WGLA_417	0 2770277 OR 417417
PCI_DEVIDE	0 GT218-300-A1
R4MCFG[2]	0000 Ejside 0001 Setpoint, Motion 0010 Commands 0011 Flywhe 0100 Numpk
R4MCFG[2]	0000 Ejside 0001 Setp 0010 No start 0011 Start one
R4MCFG[2]	Mode REFDEF1

Power Supply I: FBVDD/Q, PEX_VDD, 5V, 3V3_F

[illegible]

Net Name	VOLTAGE	MAX_CURRENT
5V	5V	0.310A
DDC_5V	DDC_5V	0.110A
3V3_F	3V3_F	2.0A
3V3_FUSE	3V3_FUSE	0.000A
PEX_VDD	PEX_VDD	2.7A
FBVDDQ	FBVDDQ	10.0A



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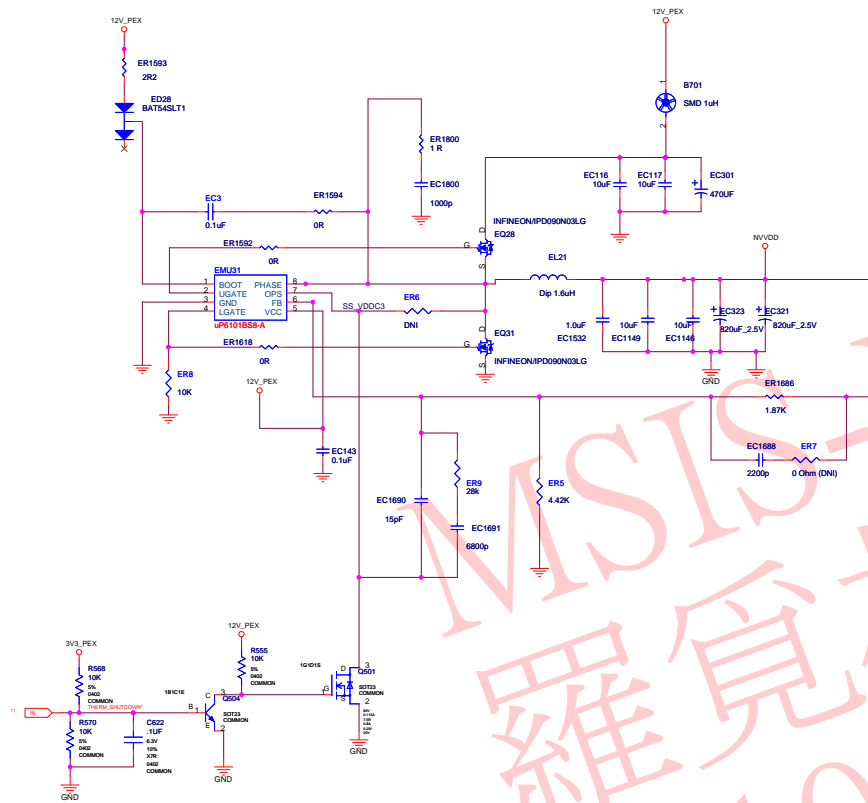
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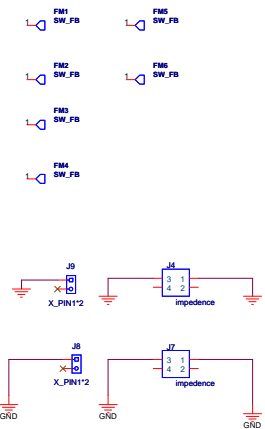
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply I: FBVDDIQ, PEX_VDD, 5V, 3V3_F


Power Supply II: PLLVDD, NVVDD

[illegible]

Net Name	VOLTAGE	MAX_CURRENT	POWER_NET
12V_PEX	12V	5.5A	30MM
3V3_PEX	3.3V	3.0A	10MM
NVDD	1.1V	17.5A	30MM



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