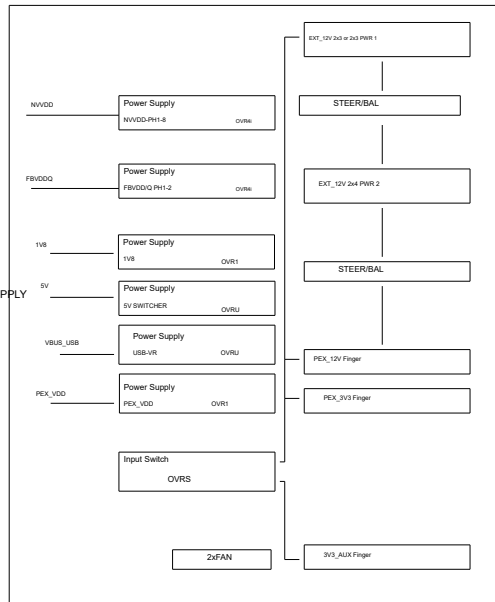
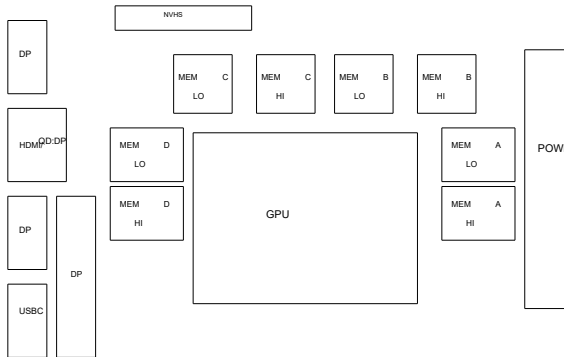


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GP104_MVVD0_P0I*

P0_MVVD0_P0000

GP100_MVVD0_P0M0I0

P0_MVVD0_EN

I200_S0A_R

I200_S0C_R

I200_S0C_R

I200_S0A_R

GPU_MVVD0_P0M0N

GPU_MVVD0_REM0R

V000_P00_EN

P0_US00C_A0T

V000_P00T_EN

US00_S00C_C0T

US00_I200_S0C

US00_I200_S0A

P0_I0001_V0C

PF_P0000_R0U

P0_I0001_P0P

DP_A000_P00T

GP1000_P0_P000R

P0_P0_P0000

P0_M0V0V3_EN

P0_M0V000_P0000

I2V_P000_P0

P0_V0000_P0000

GP100_G0C_P0_EN

P0M_R0I0

P0_R0D0_I2V_EN

P0M_P0_R000C

GP1001_P0V0D_P0I*

P0_P0V0D_P0000

GP100_P0V0D_R0L

P0_P0V0D_M0FF_R

P0_P0V0D_EN

P0V0D0_R0M0R_P0N

P0V0D0_R0M0R_R0U

I200_S0C_R

I200_S0A_R

GP1000_A0C_M0N_R0L

P0M_P0_R000C

I0000001_L0W_P00P*

P0M_A0C_I0_R

P0M_R0I0P

P0M_A0C_I0_R

P0_R0D0_I2V_EN

P0M_A0C_I0_R

GP100_G0C_P0_EN

P0M_A0C_I0_R

I2V_P0P

I2V_P0P

I2V_P0P

I2V_P0P

I2V_P000_R_1_I0D

I2V_P000_R_1_I0D

I2V_P000_R_1_I0D

I2V_P000_R_1_I0D

I2V_P000_R_1_I0D

I2V_P000_R_1_I0D

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I2V_P000_R_1_I0D

I2V_P000_R_1_I0D

I2V_P000_R_1_I0D

I2V_P000_R_1_I0D

P0_I0V_A0M_EN

P0_I0V_A0M_P0000

GP100_G0C_P0_EN

P0_P0V0D_P0000

P0_P0V0D_EN

GP100_G0C_P0_EN

P0_I0V_M0000_EN

P00_R0P_R0P*

US00_I200_S0C

GP100_G0C_P0_EN

IP00_I200_S0A

GP1004_I0V_P0P

US00_I200_S0A

IP00_I200_S0C

GP1004_I0V_P0P

IP00_I200_S0A

V000_P00_EN

US00_C0C

P0_US00C_A0T

US00_C0C

US00_A0X_R

US00_A0X_R

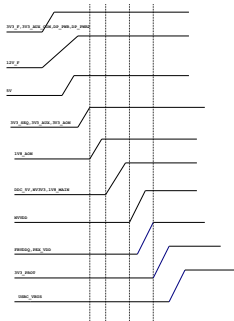
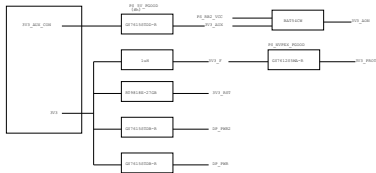
US00_C0C

US00_C0C

US00_S00C_C0T

US00_P00T_EN

V000_P00T_EN

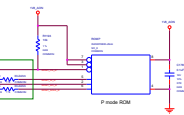
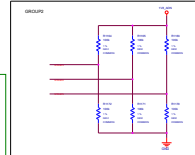
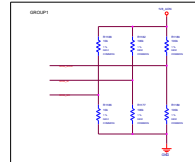
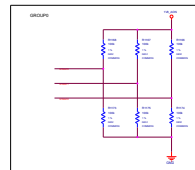
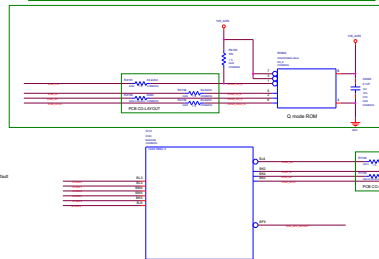
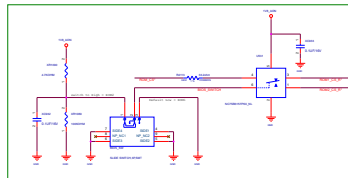


1980. *Journal of the Royal Society of Medicine*, 73, 105-110.

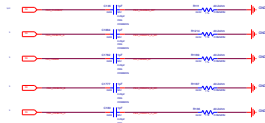
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	0SDIO_SEL ORGNAL	0VGA_DEVICE DISABLE
1SMR_ALT_ADDR ENABLE		
0SMR_ALT_ADDR DISABLE	1PCI_CFG LOW POWER	
	0PCI_CFG HIGH POWER	

	STRAP1	STRAP2	DATE_ALT_ADDR	DEVID_SGL	PCID_CPD	VISA_SERVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

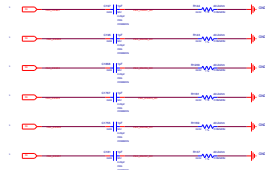
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05000	8Gb	230-62	Samsung
05001	8Gb	230-62	Mitsumi
05015	8Gb	230-62	Hynix
05110	16Gb	230-62	Samsung
05111	16Gb	230-62	Samsung







PLACE CLOSE TO BR1



PROPERTY	PROPERTY DESCRIPTION
NAME	PCI_TERMINATION

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4500 Riva Road, Santa Clara, CA 95051

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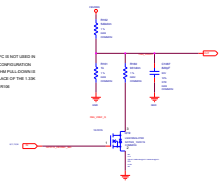
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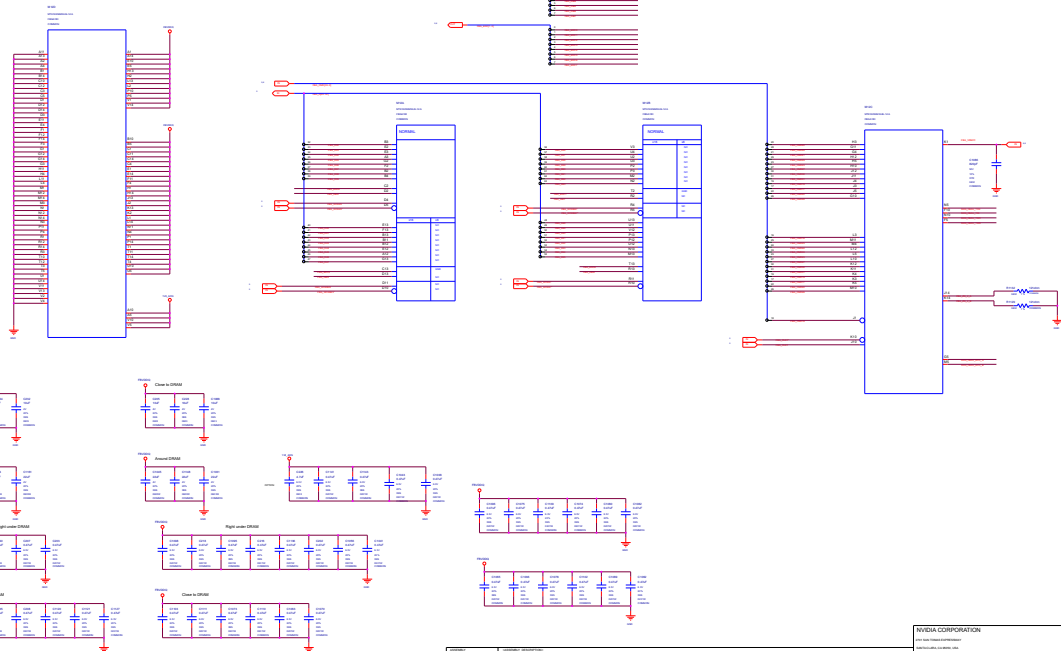
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variable	variable _id number
value label	define this part of a





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WLPN 885-1G180-BASE-200

WLPN

WLPN

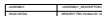
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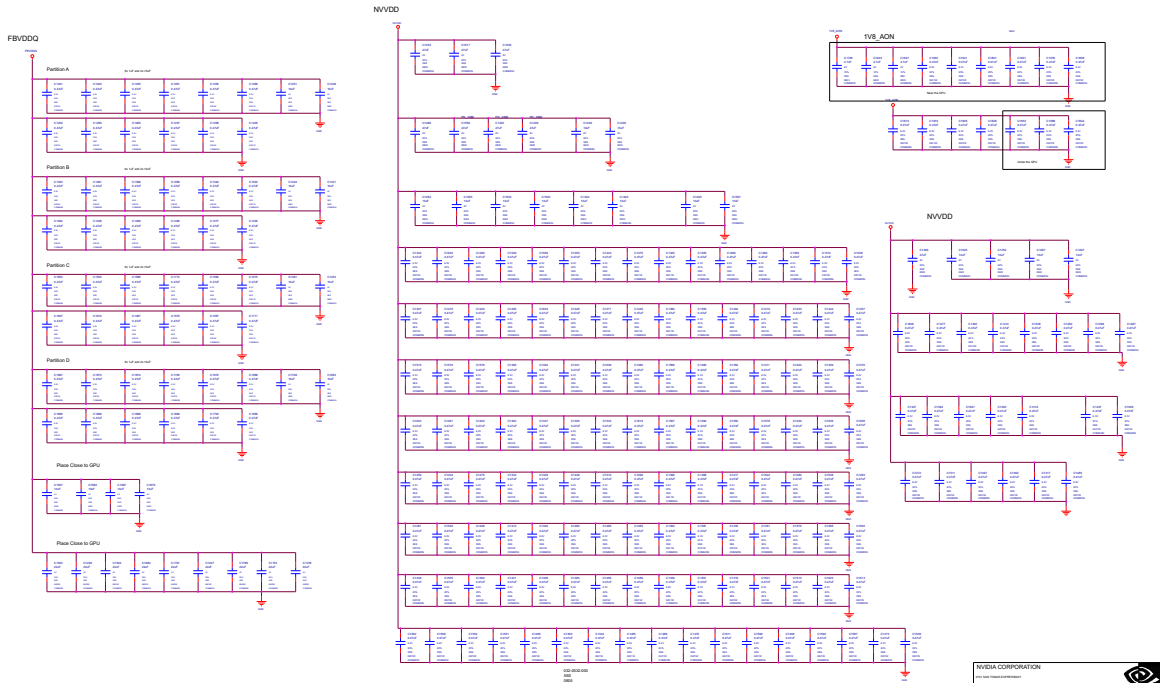












DESIGN	GPU-100-000
DATE	2023-10-10
REVISION	1.0

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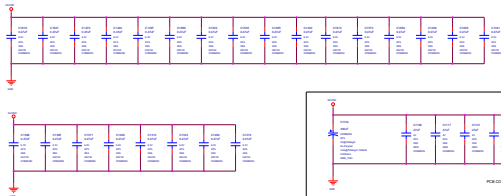
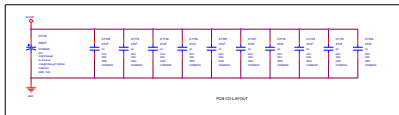


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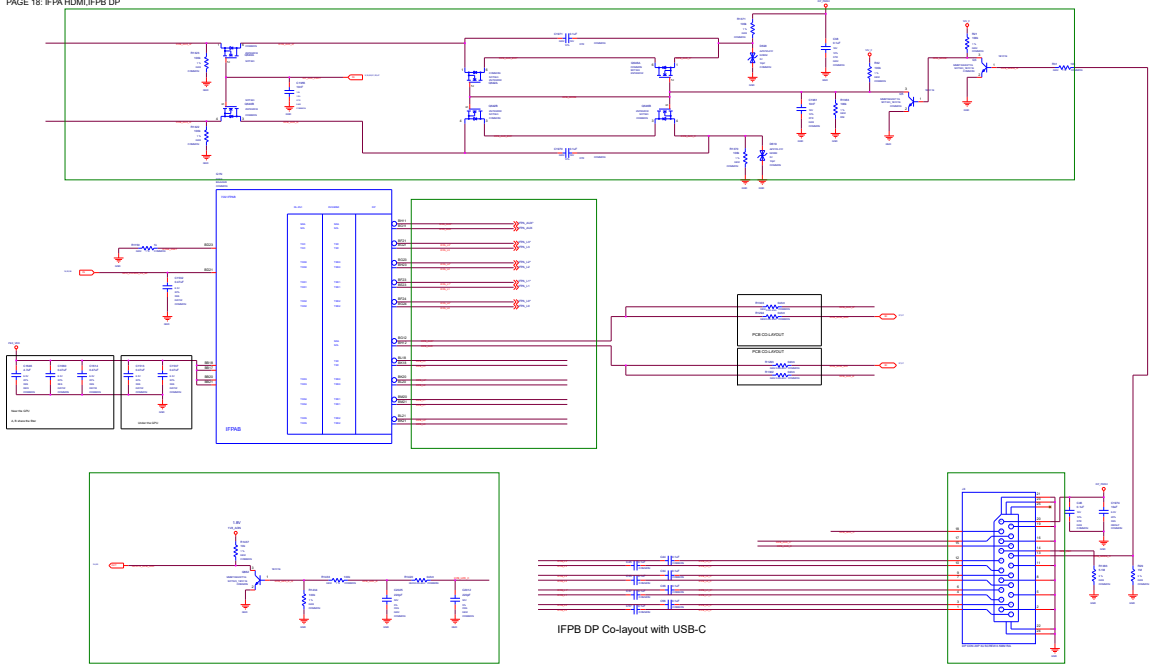
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type name	type_declaration





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NVIDIA DRIVE AGX Xavier

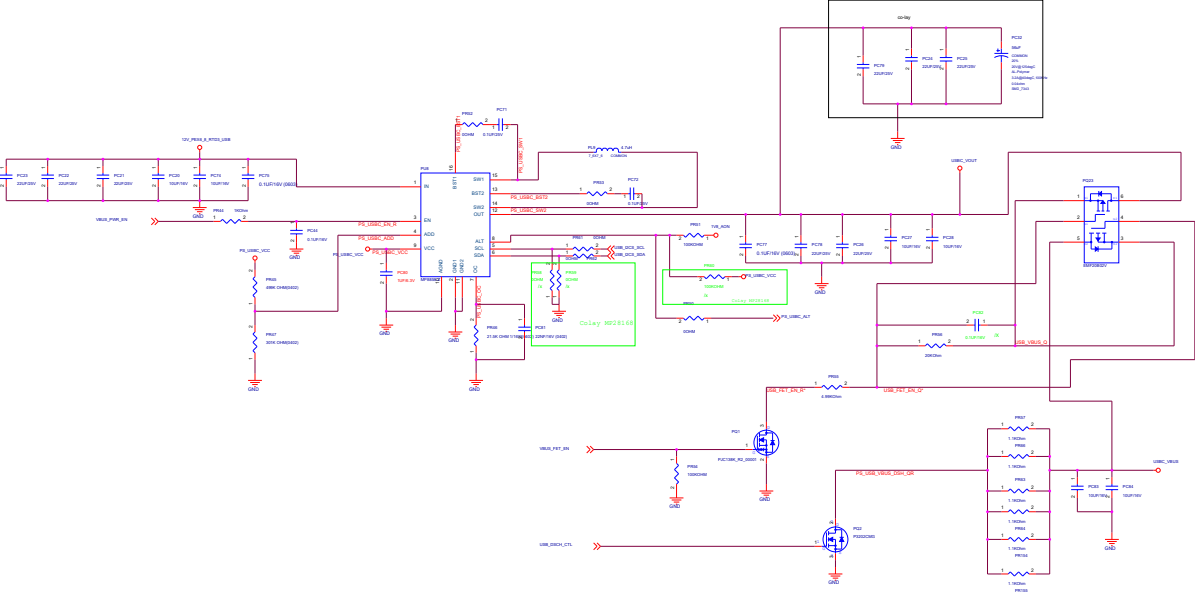
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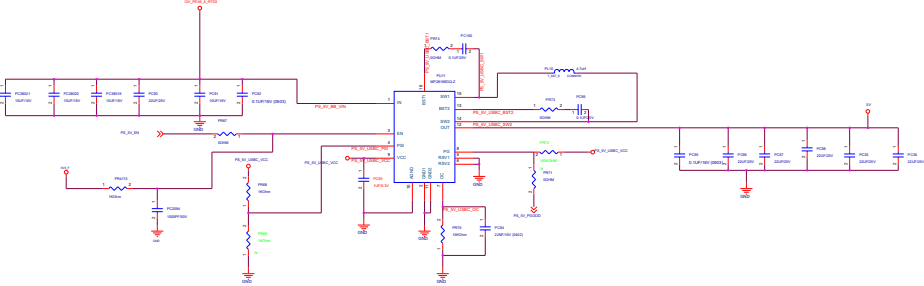
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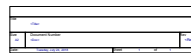
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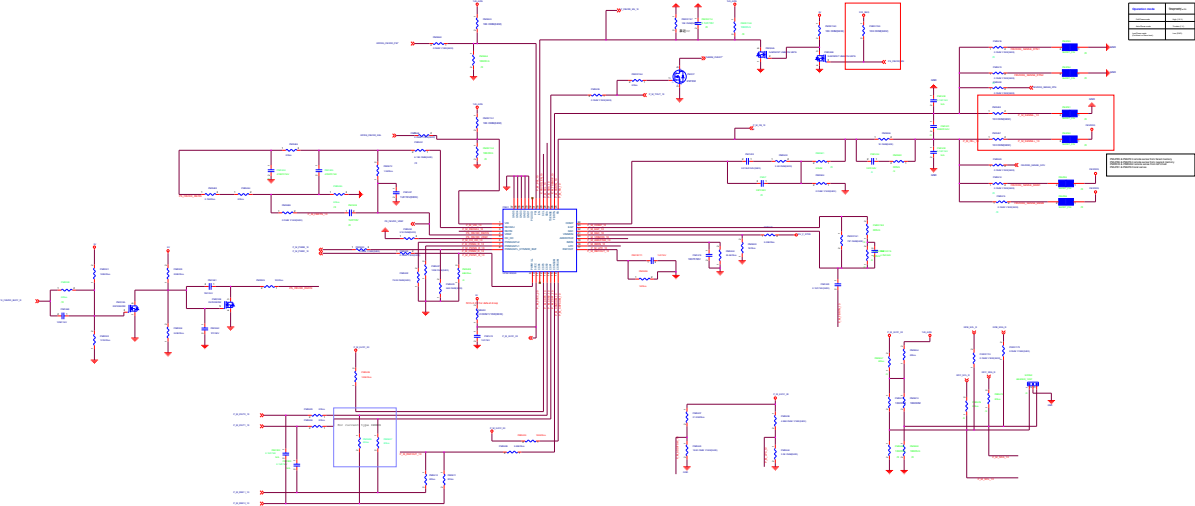
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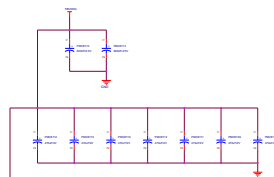
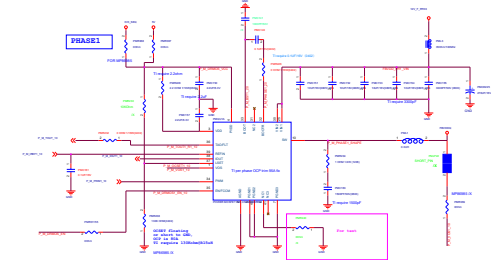




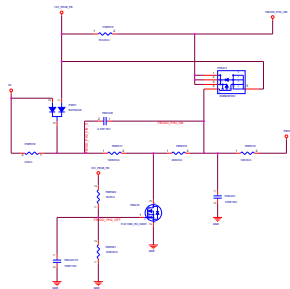
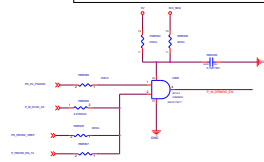
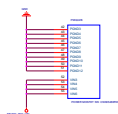
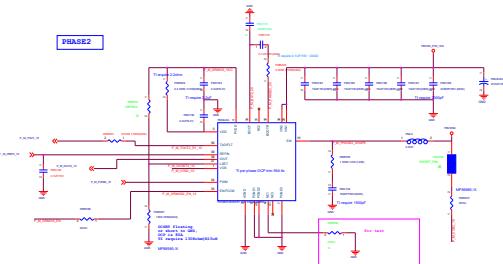




		RIS (2007-16 40000000)	
		L1-V1 (2007-16 40000000)	L1-V1 (2007-16 40000000)
AC switch	Chin	0.1uF	0.1uF
	Ring	14.70 uA	0.00 uA
Total OCP (1216)	Power	0.00 uA	0.00 uA
	Input	0.00 uA	0.00 uA
	Output	0.00 uA (0.00 uA)	0.00 uA (0.00 uA)
Indirect (1216)	RL	1.470 uA	1.470 uA
Indirect No Threshold (1216, 16, 16, 16)	Ring	1.470 uA	1.470 uA
	Max	1.470 uA	1.470 uA

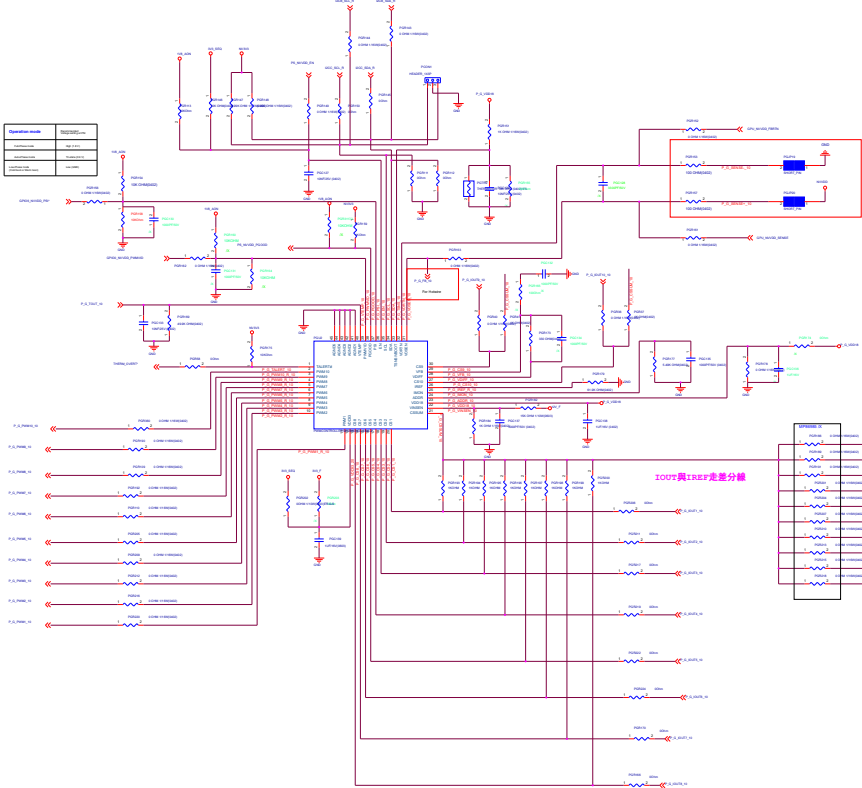


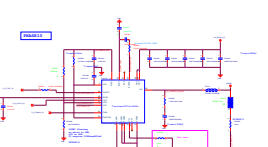
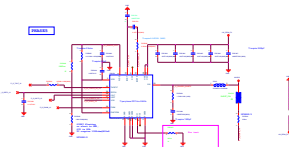
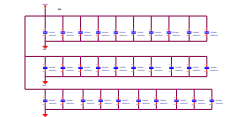
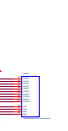
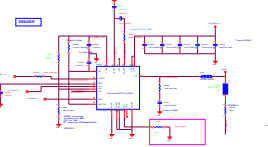
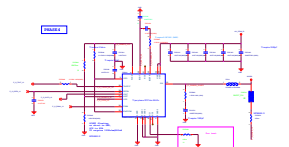
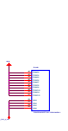
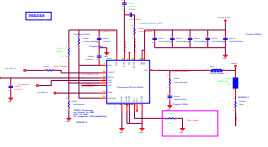
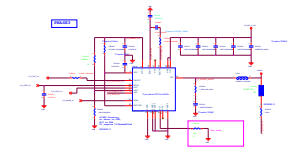
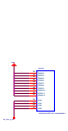
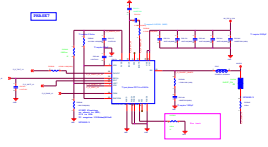
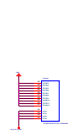
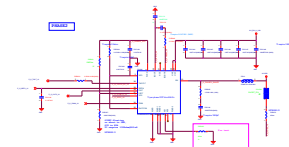
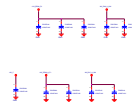
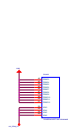
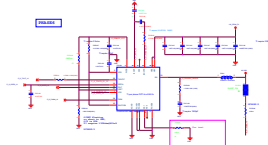
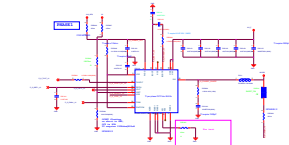
99



Operation mode	Test condition
continuous	50% duty
continuous	100% duty
continuous	100% duty

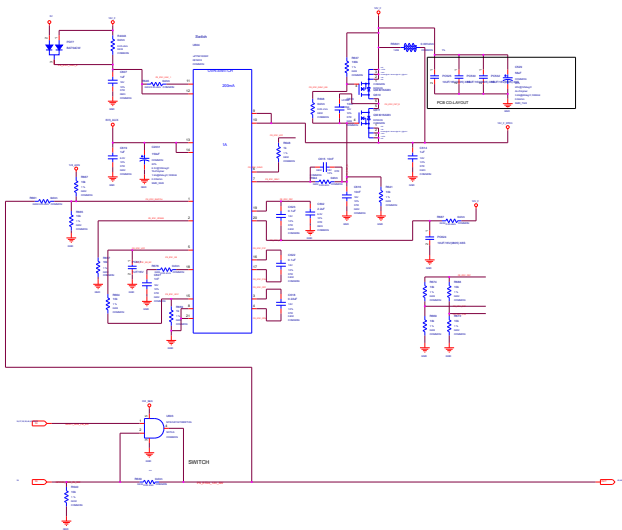
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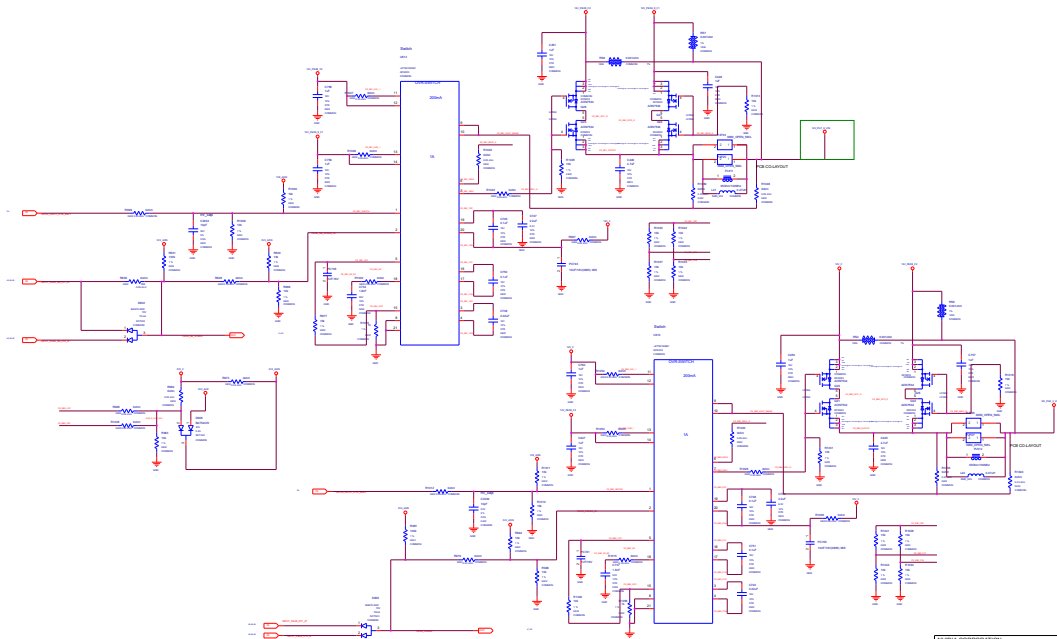




AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO28	SWITCH	VOUT
0	0	0	2V2
0	1	0	2V2
1	0	0	2V2
1	1	1	2V3A





REVISION: 1.0
 DATE: 10/10/2010
 AUTHOR: [REDACTED]
 CHECKED: [REDACTED]
 APPROVED: [REDACTED]

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 Santa Monica, CA 90409-1471

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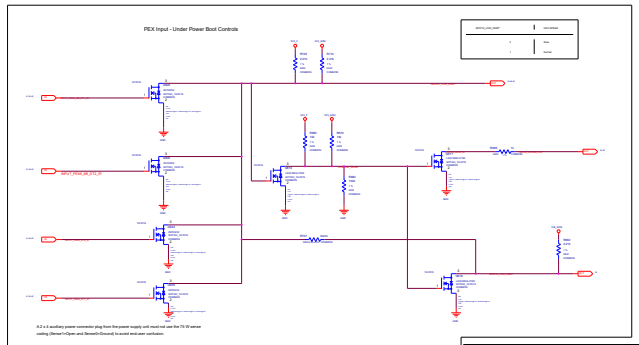


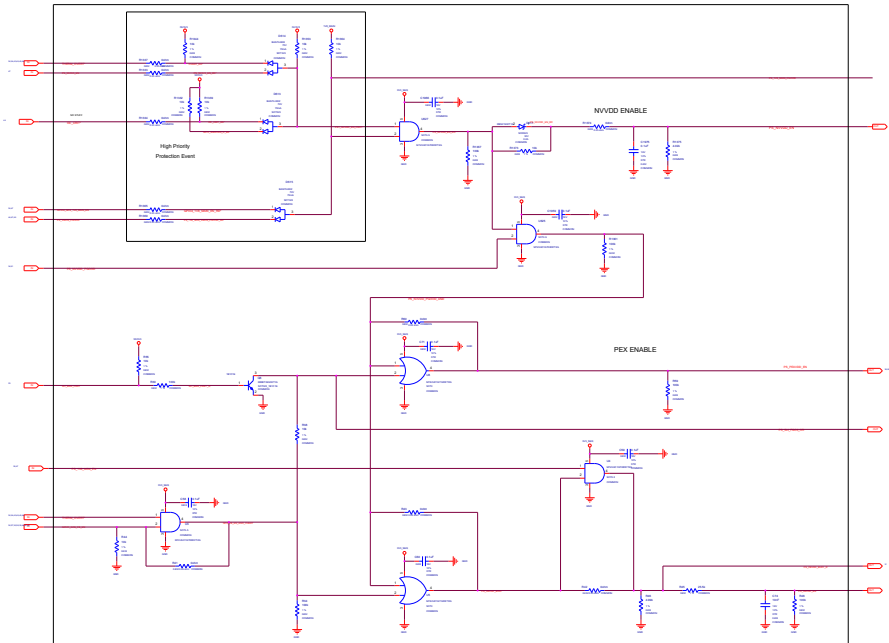
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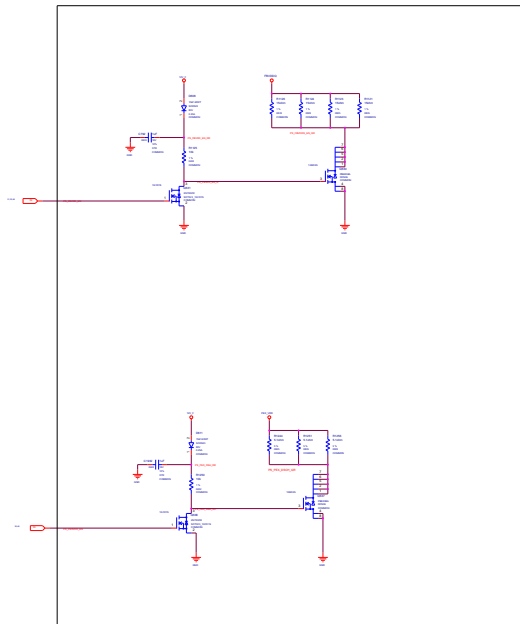
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4500 Riva Road, Santa Clara, CA 95051

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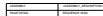
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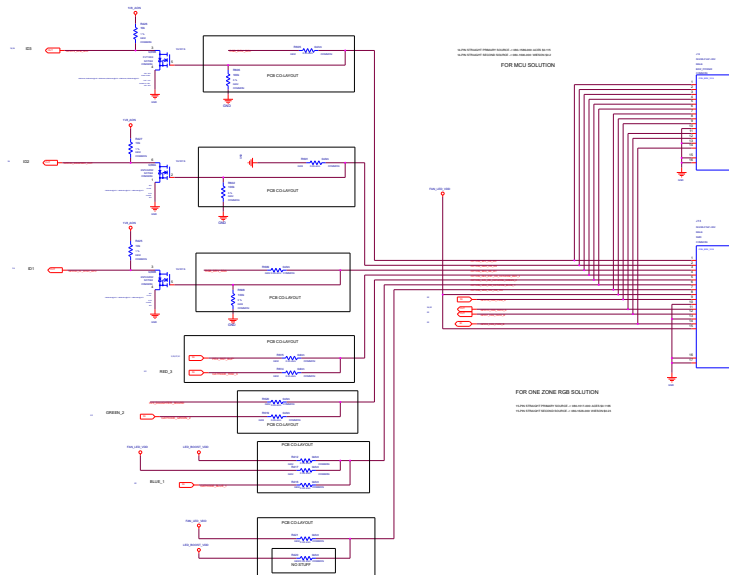
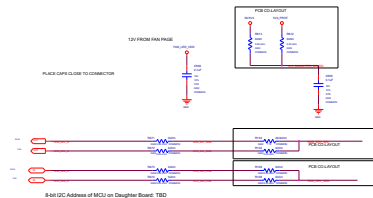
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NVIDIA-10180-BASE-200

REV: 1.0

DATE: 10/10/2013

PAGE: 1

TOTAL: 1

NVIDIA-10180-BASE-200

REV: 1.0

DATE: 10/10/2013

PAGE: 1

TOTAL: 1

Bracket Screw

[illegible]

- **salivary gland**
- **basal gland**
- **serous**
- **compound**



CPU Model Symbol

	relative
	percentage



Age Group	No opinion	Dislike	Like	Love	Hate
18-24	45%	25%	15%	10%	5%
25-34	40%	30%	15%	10%	5%
35-44	35%	35%	15%	10%	5%
45-54	30%	40%	15%	10%	5%
55-64	25%	45%	15%	10%	5%
65-74	20%	50%	15%	10%	5%
75-84	15%	55%	15%	10%	5%
85+	10%	60%	15%	10%	5%



ASUS VGA PCB Logo

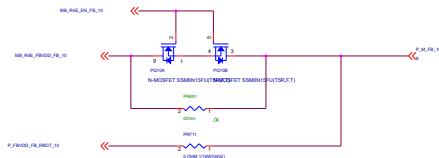
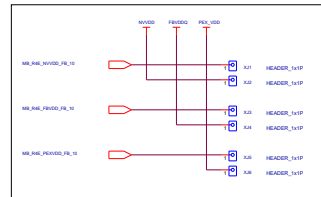
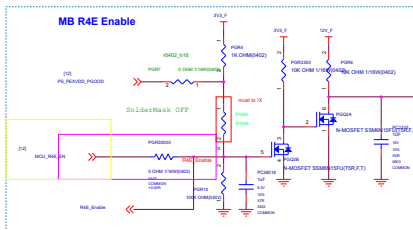


PCB MADE IN CHINA

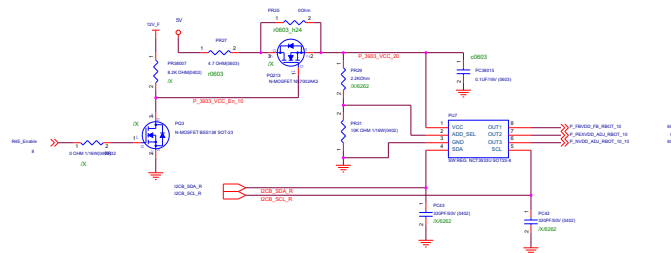


CAN ICES-3 (B) /NMB-3(B)



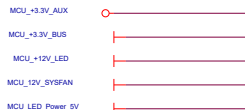


12V MOSFET driver circuit diagram. The MOSFET is an N-channel MOSFET with a 10A/150V rating. The gate is driven by a 12V source through a 10kΩ resistor. The drain is connected to a 12V source through a 10kΩ resistor. The source is connected to ground through a 10kΩ resistor. The MOSFET is labeled 'MOSFET 10A/150V (N-CHANNEL MOSFET)'. The gate is labeled 'GATE' and the drain is labeled 'DRAIN'. The source is labeled 'SOURCE'. The MOSFET is also labeled 'MOSFET 10A/150V (N-CHANNEL MOSFET)'.



2018/06/14

Power



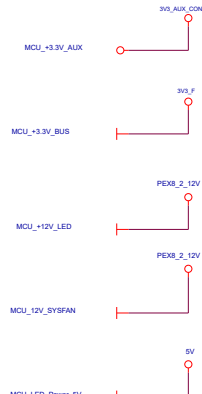
From PCIE 3V3_AUX (for ITE)

From BUS 3V3 (for ITE logic判斷)

From BUS 12V (for Cover LED/RGB Header使用, Max 2.3A)

From 12V (for 外接式風扇使用, 任一組12V皆可)

From 5V (for 背板LED)



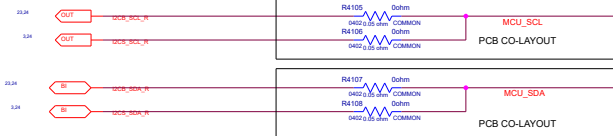
I2C



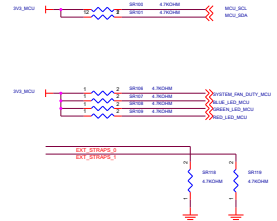
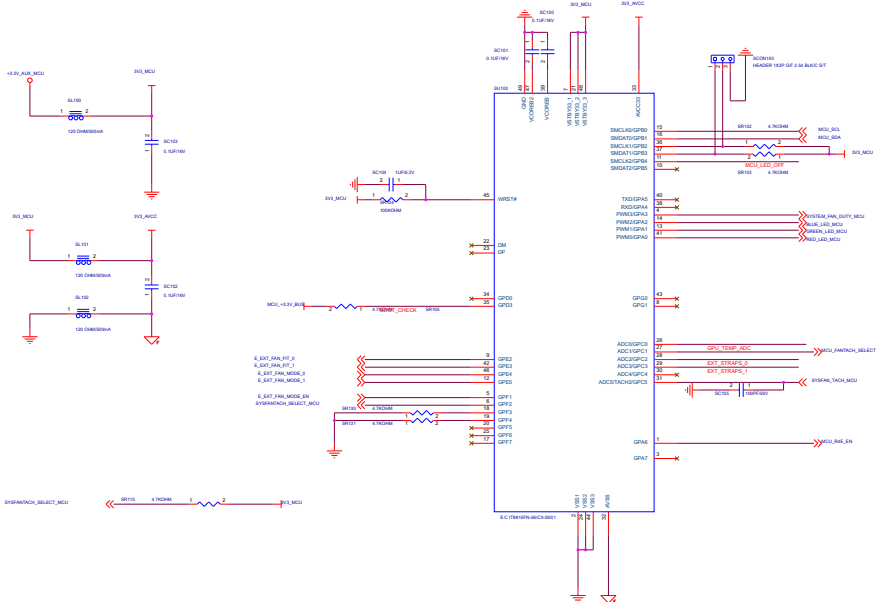
From GPU (for ITE / ENE)

NV I2C 建議使用 I2CB_SDA & I2CB_SCL

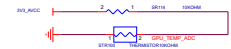
Layout前請再與AMD/NV EE Leader or AMD/NV AE 確認



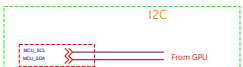




00: 無EXT Powe

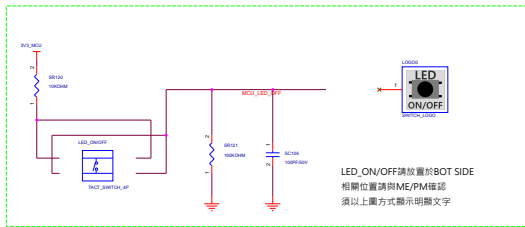
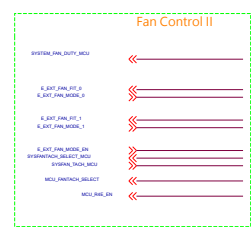


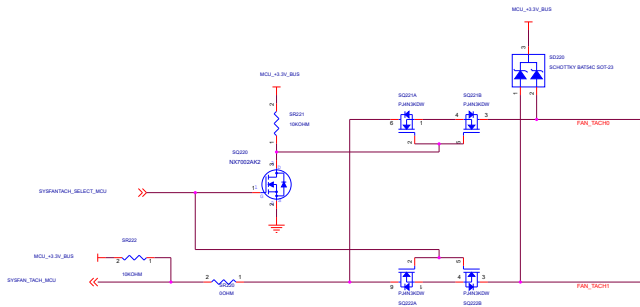
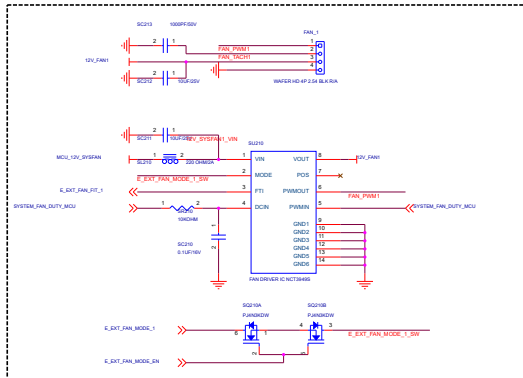
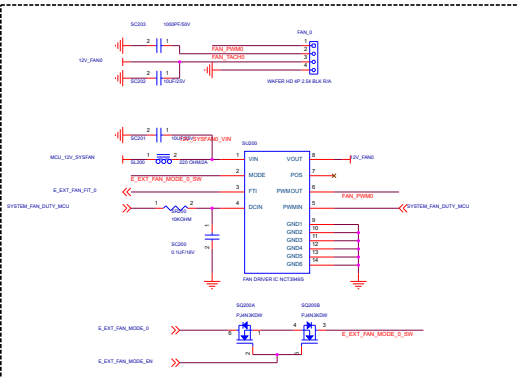
STR100 請盡可能放置於GPU附近位置



12C

Power





Power

MCU_3.3V_BUS From BUS 3V3

MCU_12V_SYSFAN From 12V

Fan Control II

E_EXT_FAN_FIT_0
 E_EXT_FAN_MODE_0

 E_EXT_FAN_FIT_1
 E_EXT_FAN_MODE_1

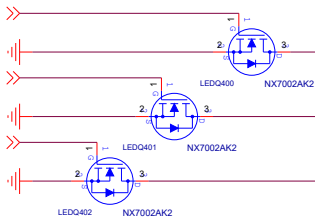
 SYSTEM_FAN_DUTY_MCU
 E_EXT_FAN_MODE_SN
 SYSFAN_TACH_SELECT_MCU
 SYSFAN_TACH_MCU

S0003 RGB LED

BLUE_LED_MCU

RED_LED_MCU

GREEN_LED_MCU



LED BOARD

VF 3.2V BLUE 1206 1/4W 1% 169ohm x3pcs

VF 1.95V RED 1206 1/4W 1% 324ohm x4pcs

VF 3.2V GREEN 1206 1/4W 1% 169ohm x3pcs

MCU_+12V_LED

MCU_+12V_LED

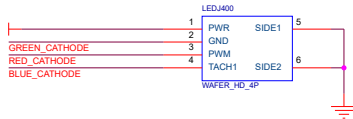
MCU_+12V_LED

Power

MCU_+12V_LED

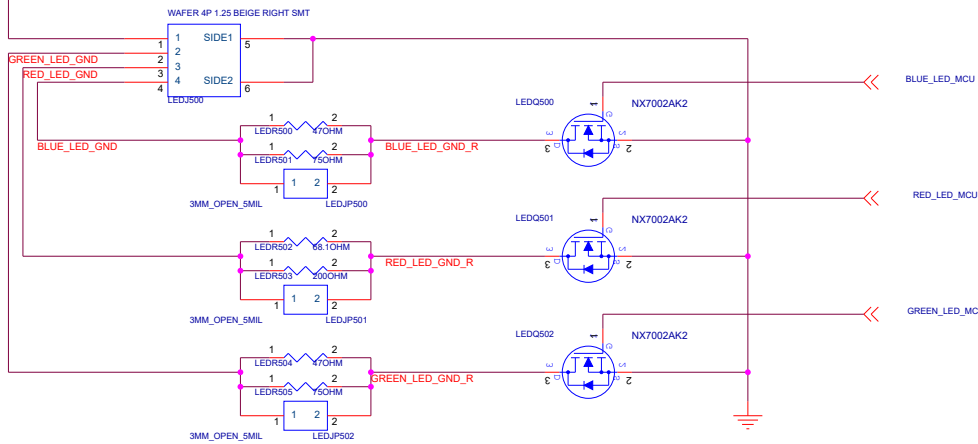
From BUS 12V

MCU_+12V_LED



S0014 LIGHT BACK PLATE

MCU_LED_Power_5V



Power

From S000

MCU_LED_Power_5V

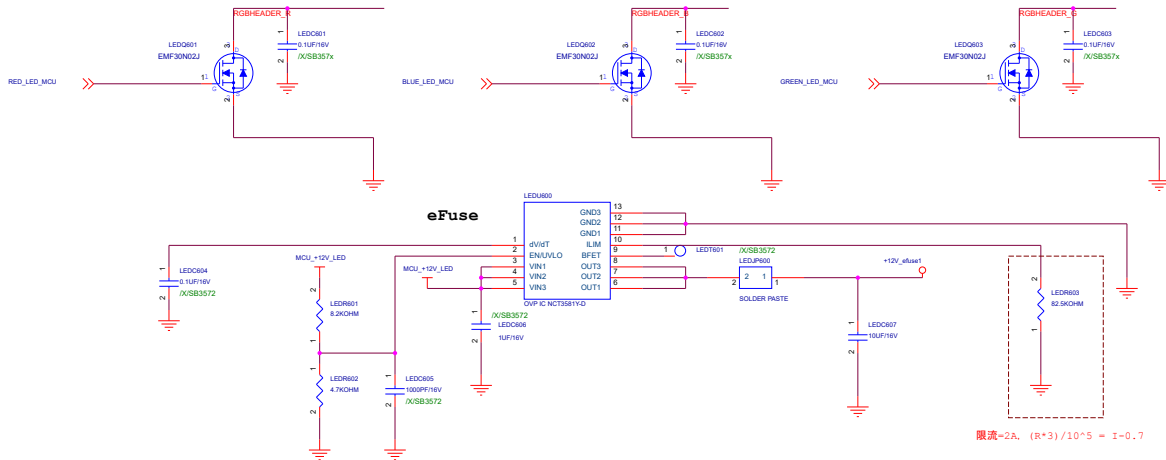
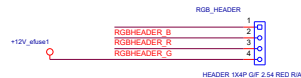


示意圖

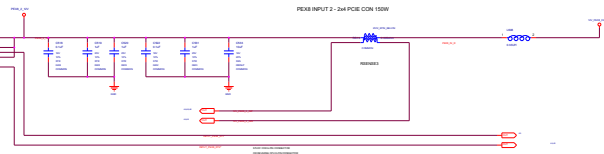
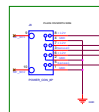
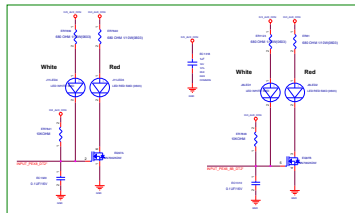


連接座旁請註明 12V G R B

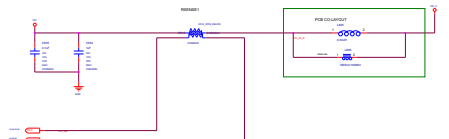
RGB Header



限流=2A, $(R \times 3) / 10^5 = I = 0.7$



PEK_12V INPUT - 60W



PEX8 INPUT 2 - 2x4 PCIE CON 150W

ACCOUNT	ACCOUNT_DESCRIPTION
PLANT COSTS	PLANT COSTS, PLANT COSTS, AND PLANT COSTS