

PG600-B02 NI GHTHAWK

GB3B-384, 6GB GDDR5 128Mx32

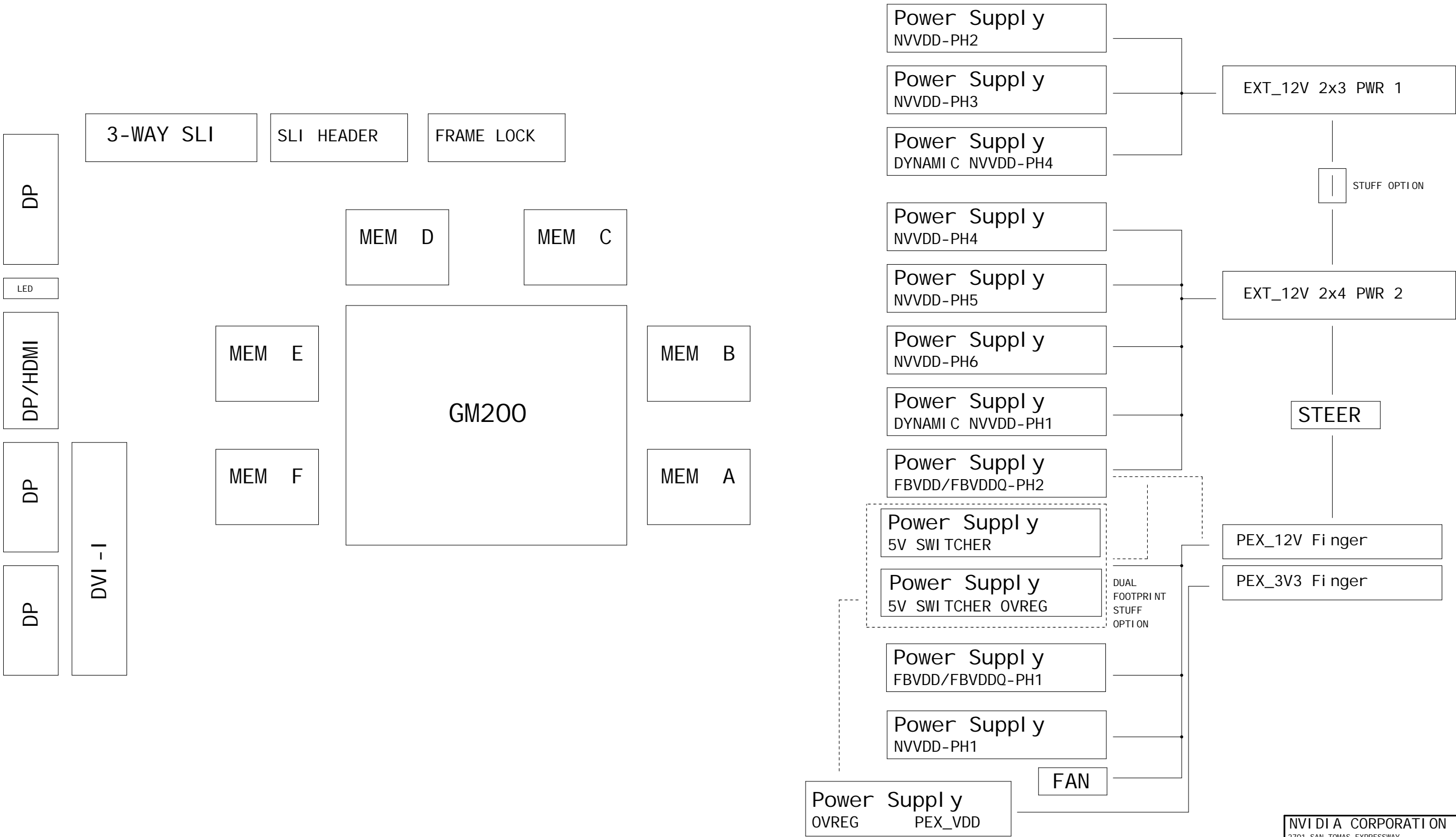
DP + HDMI /DP + DP + DP + DVI -I

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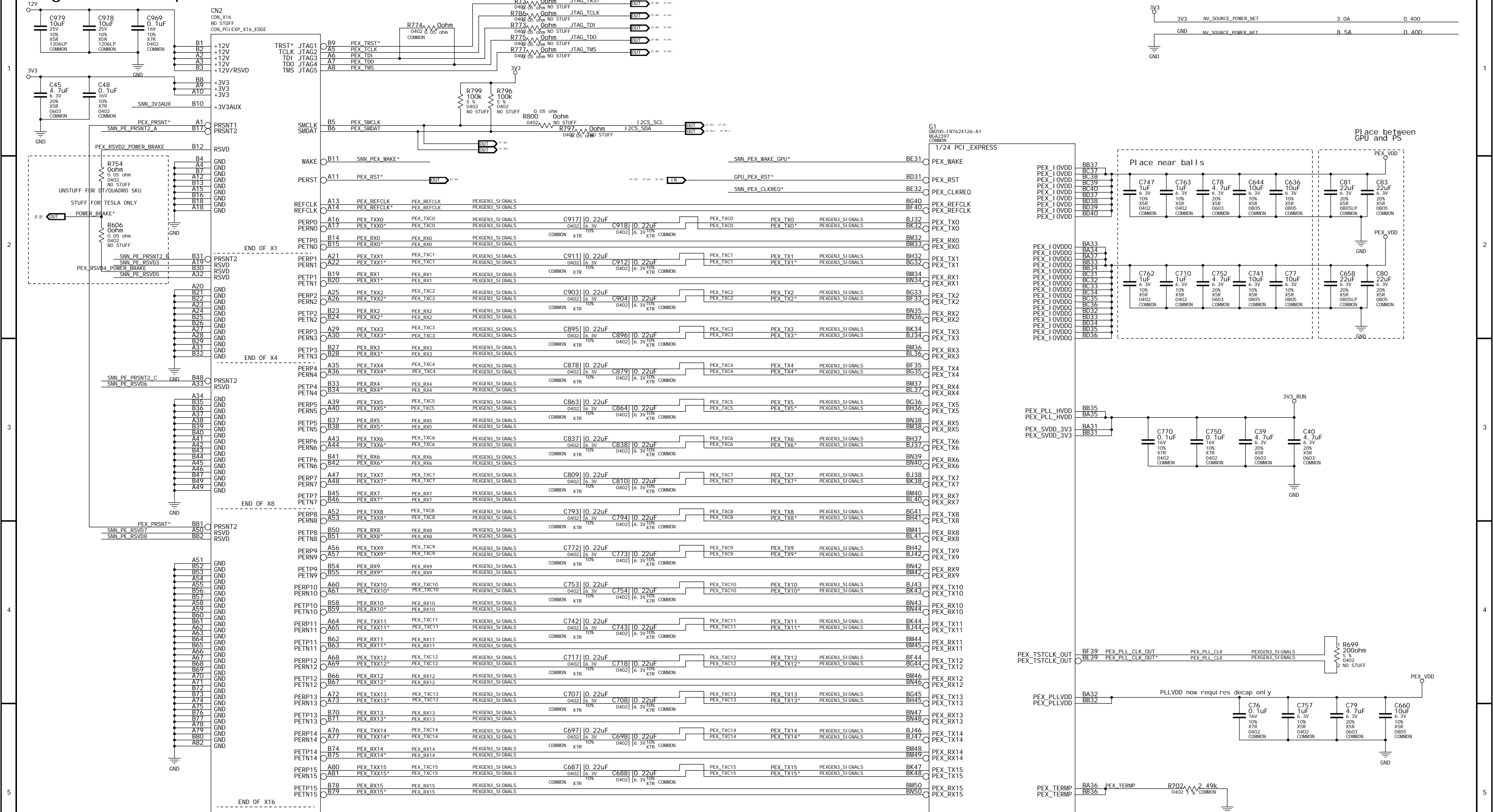
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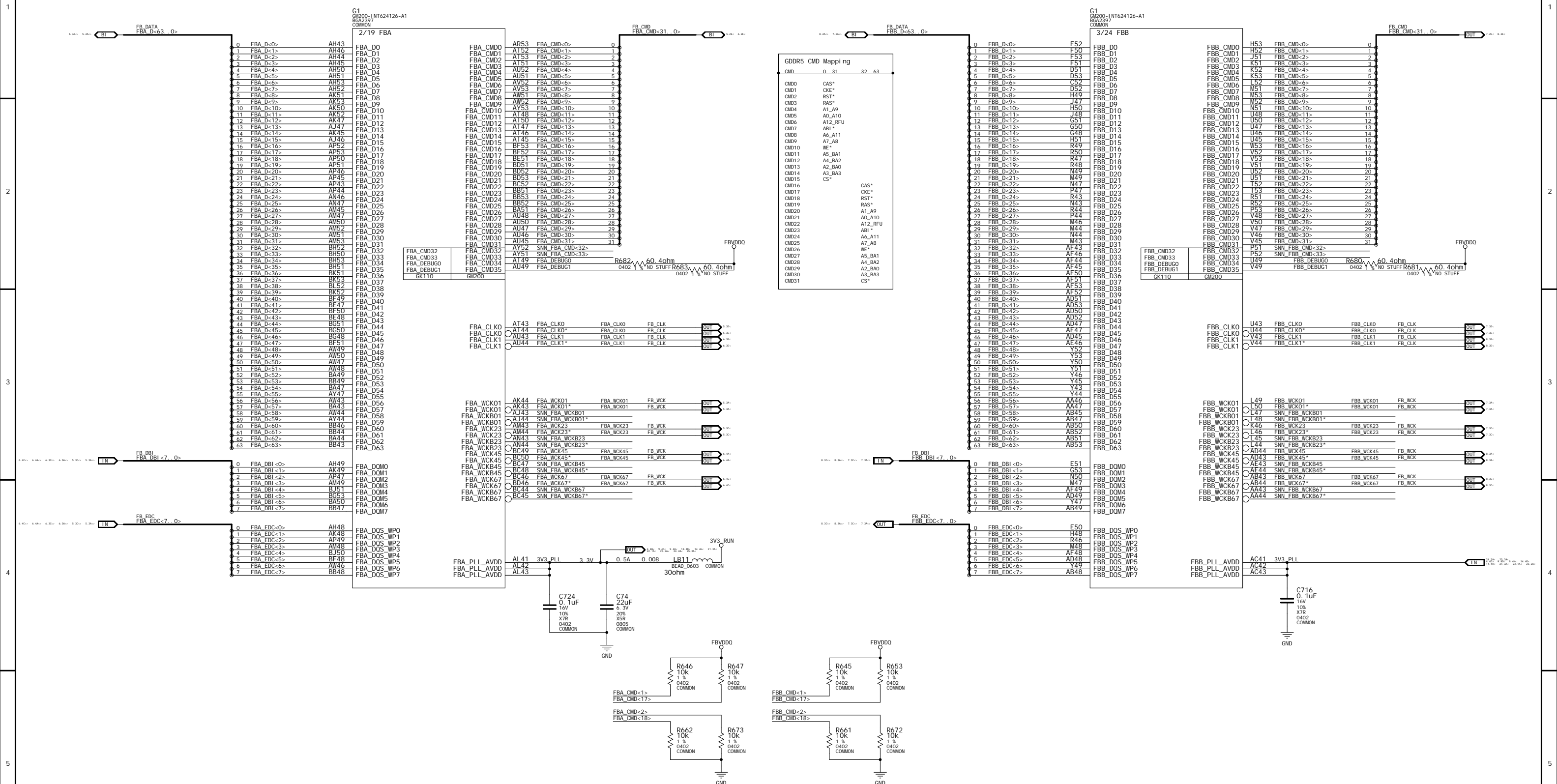
Page3: PCI Express

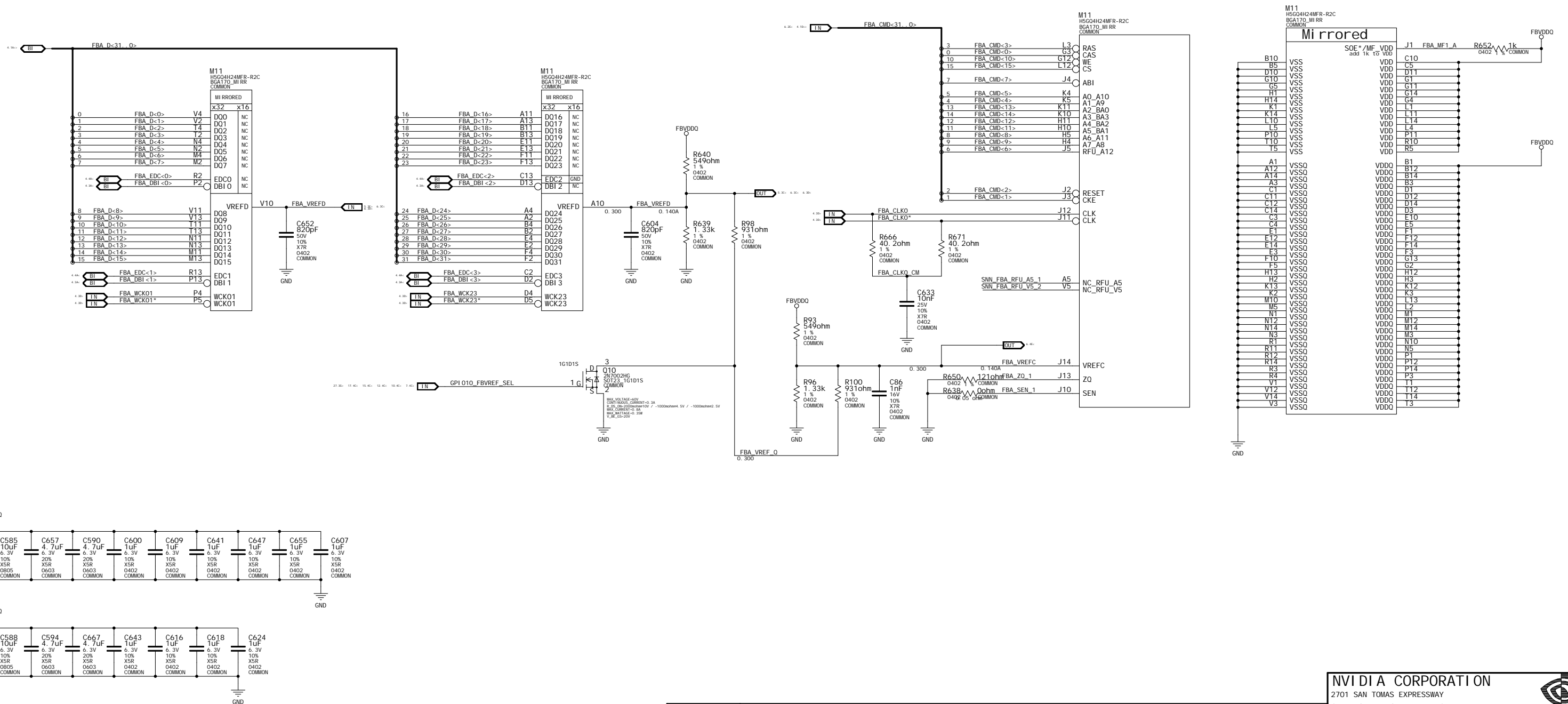


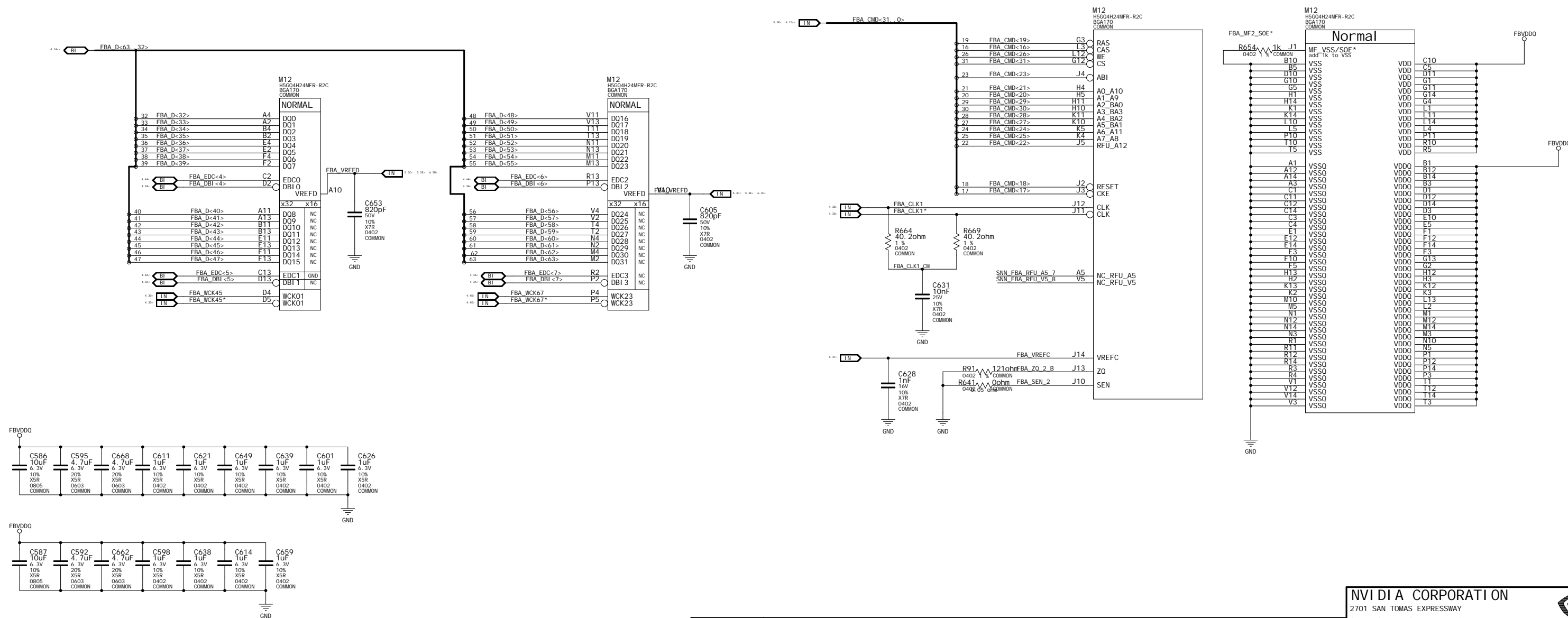
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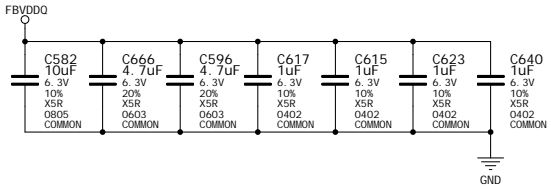
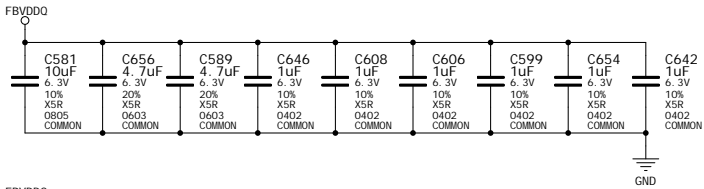
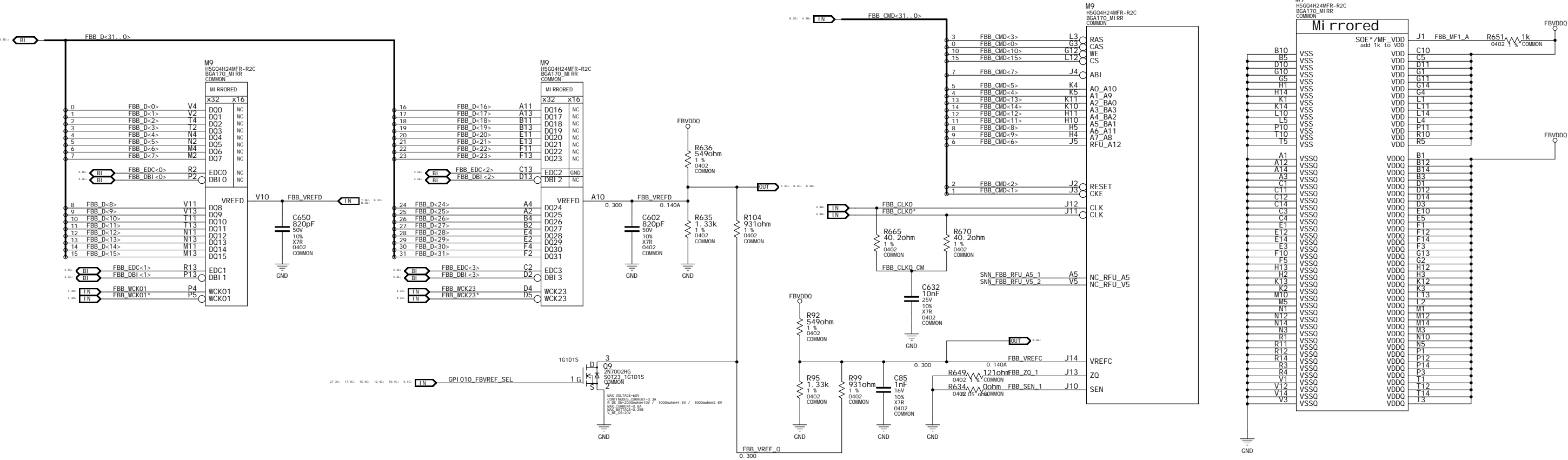
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PAGE DETAIL	PCI Express

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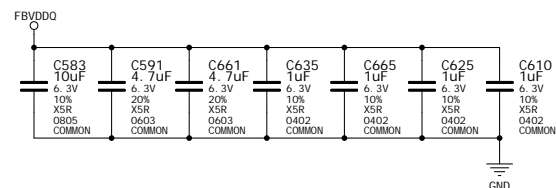
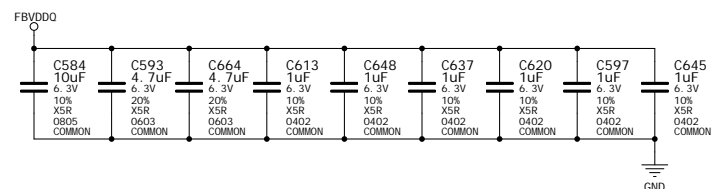
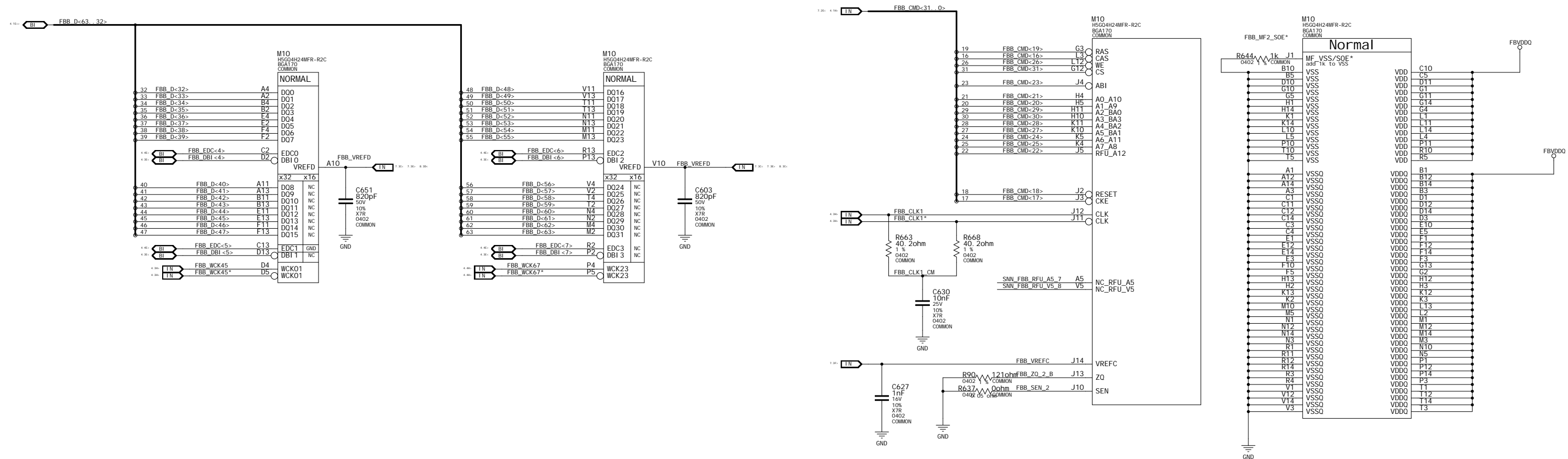







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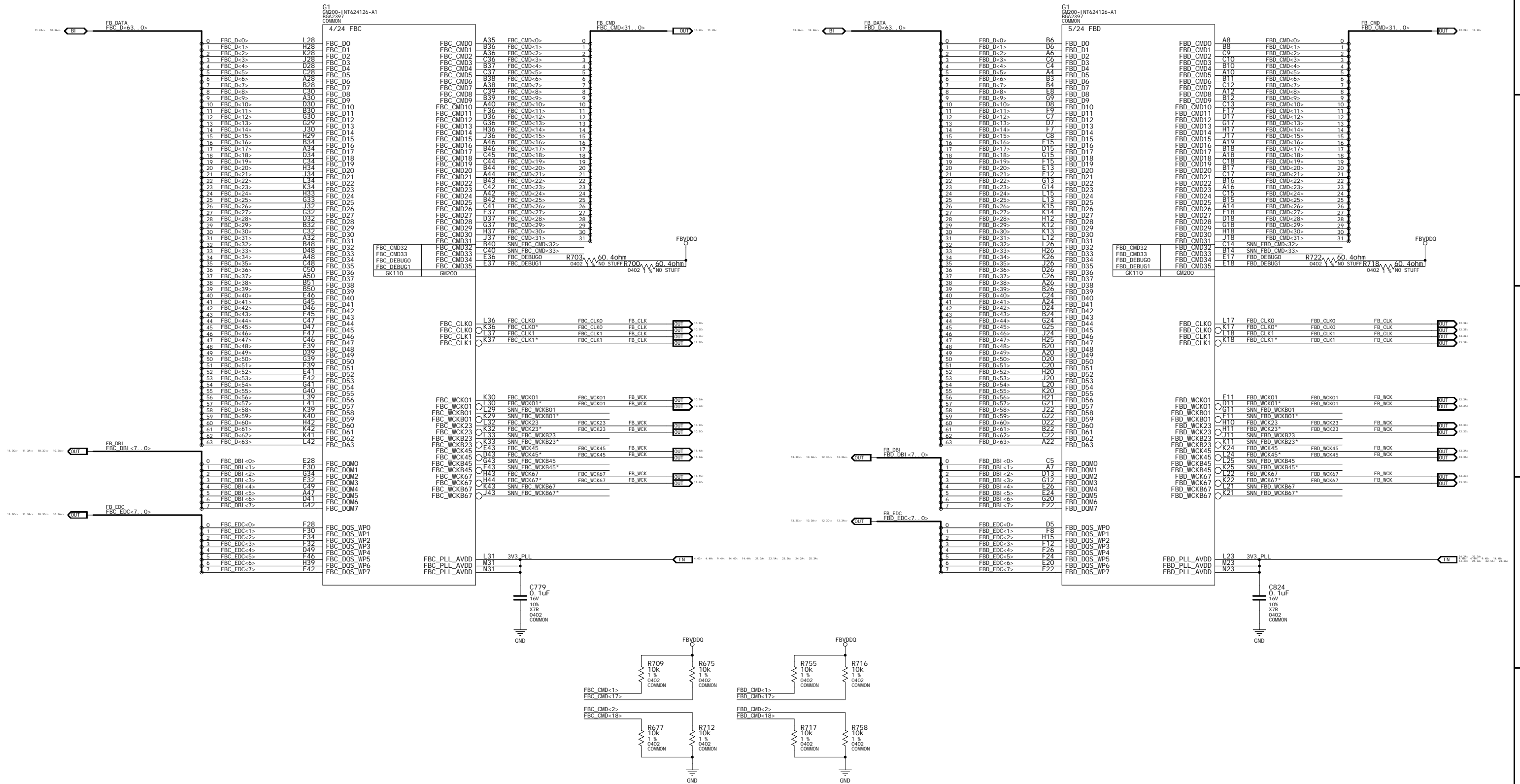
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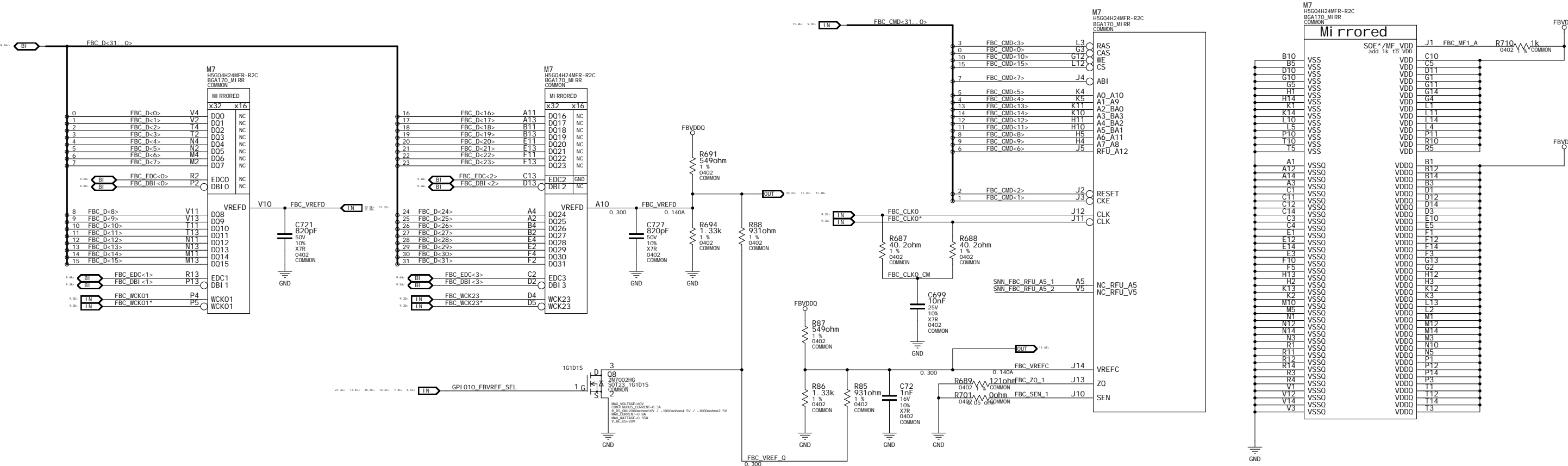


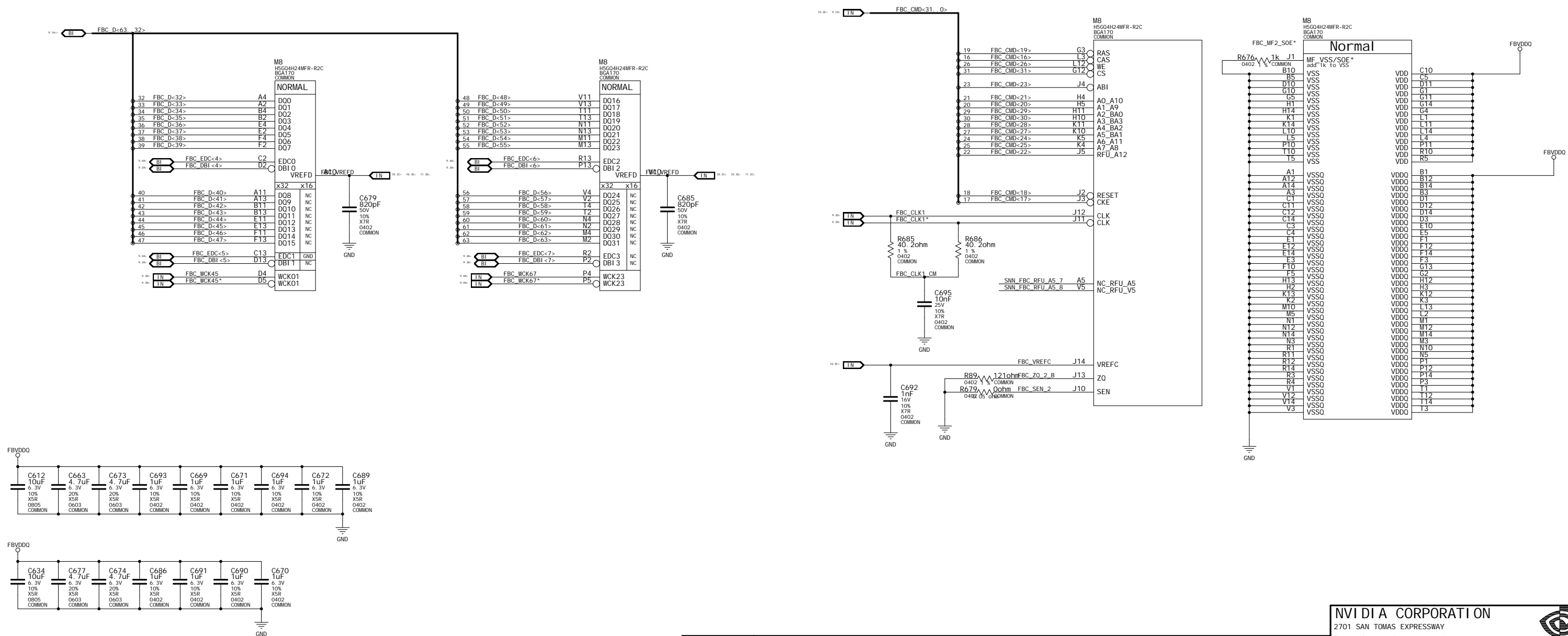
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PAGE DETAIL	MEMORY: FBB[63:32]

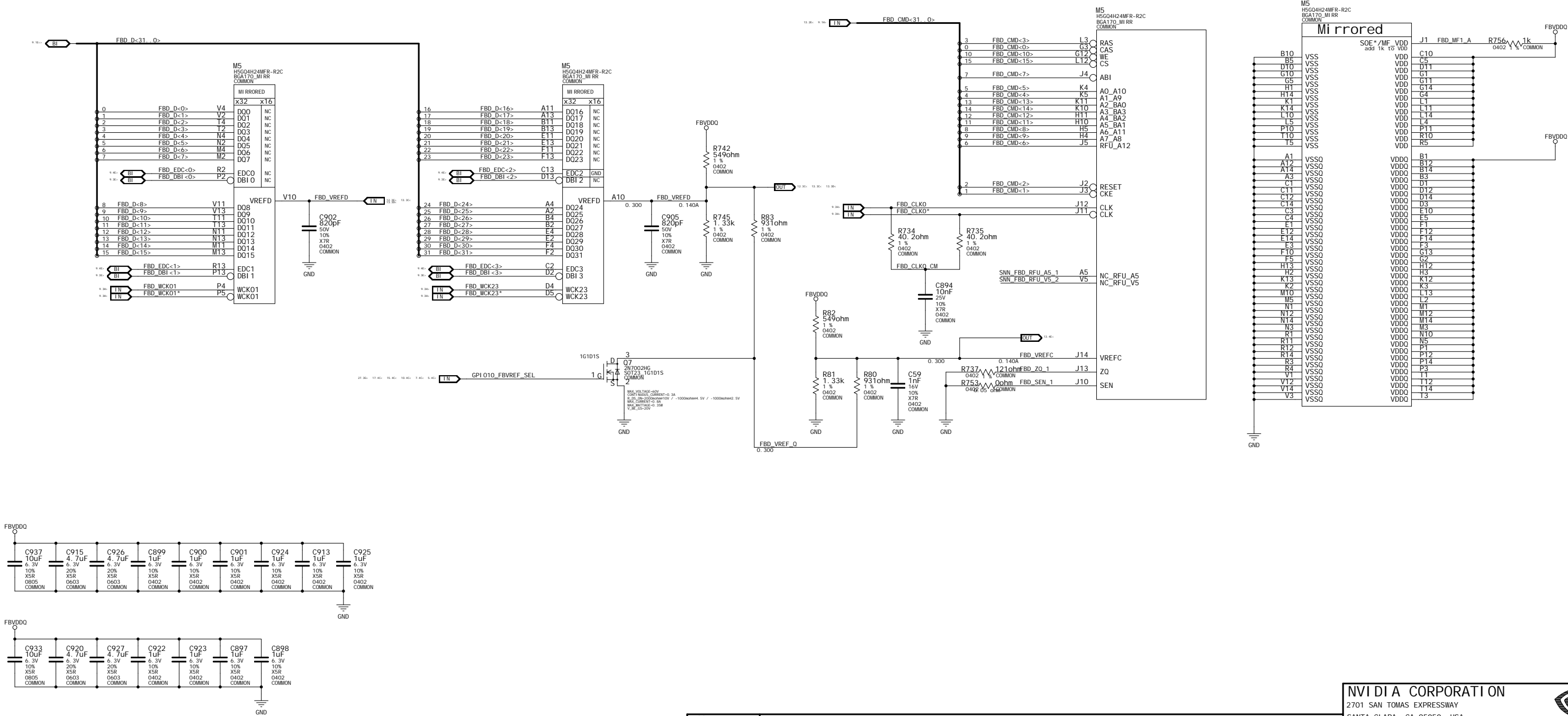
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ASSEMBLY

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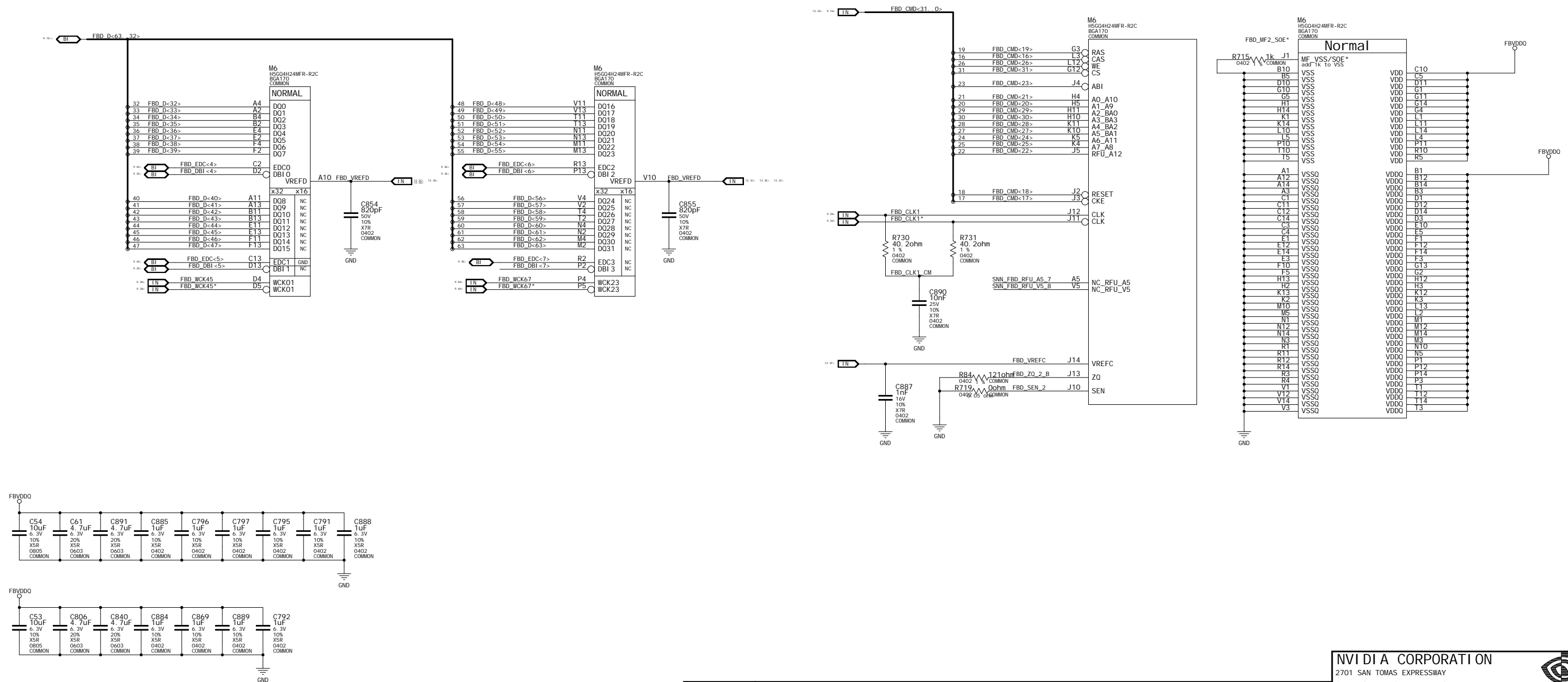
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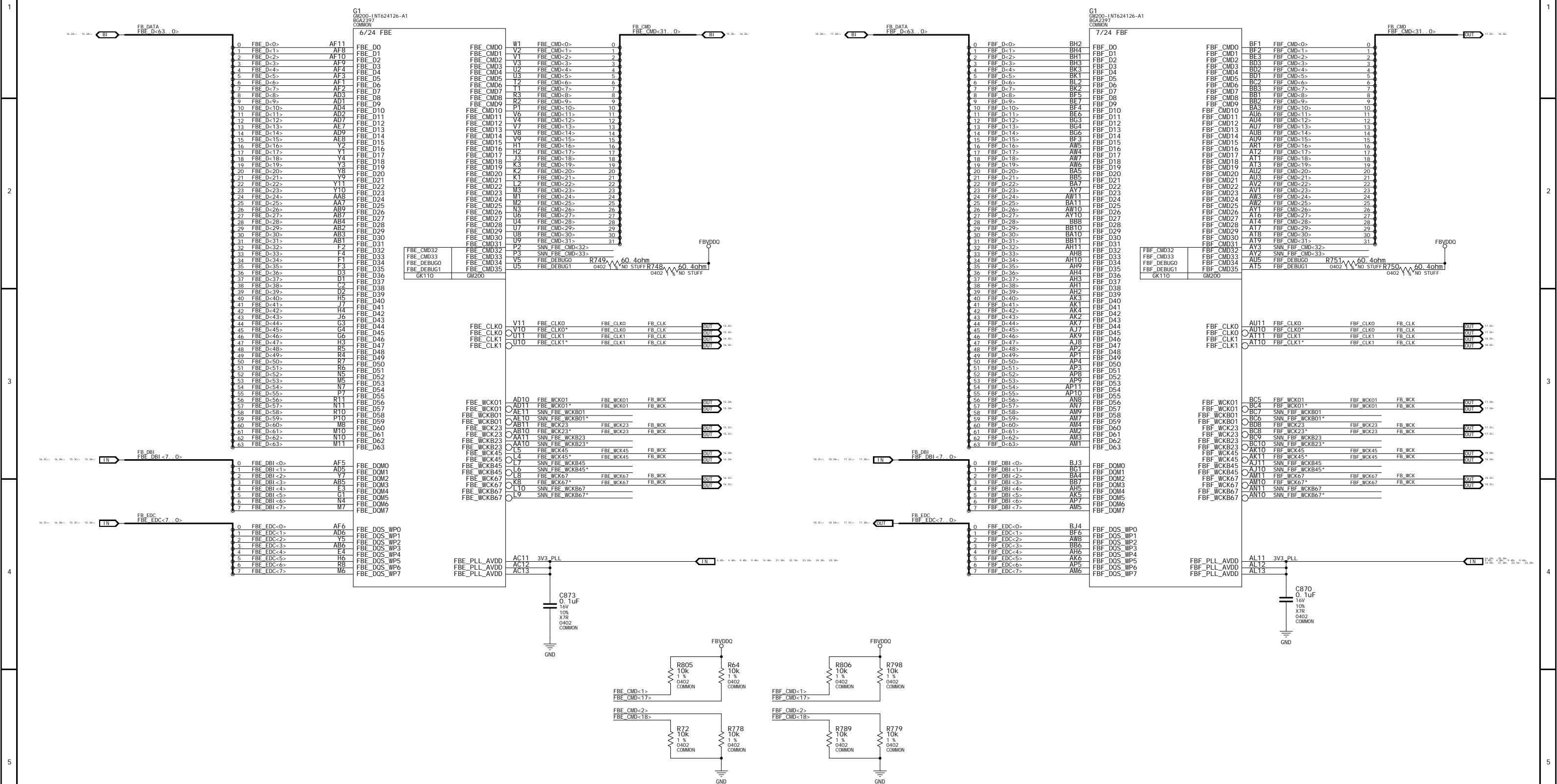
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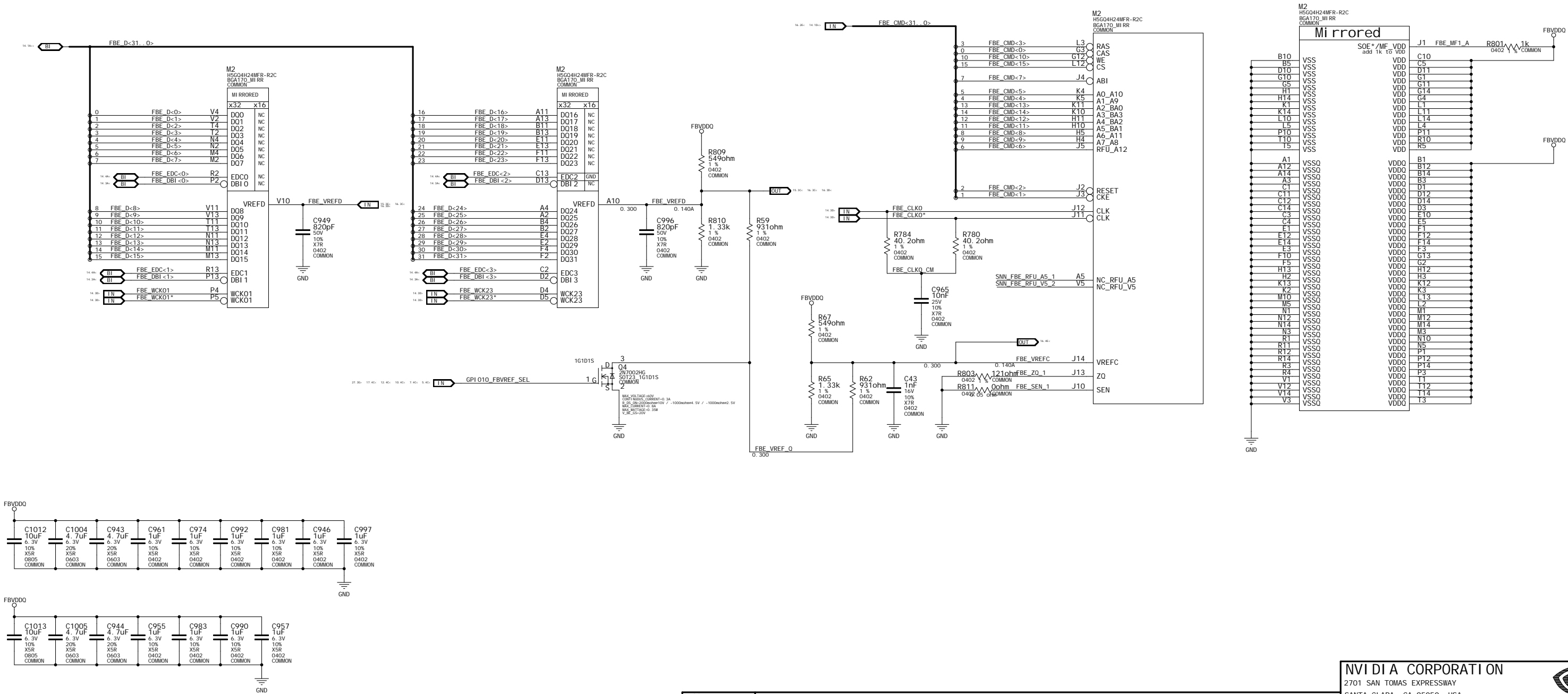
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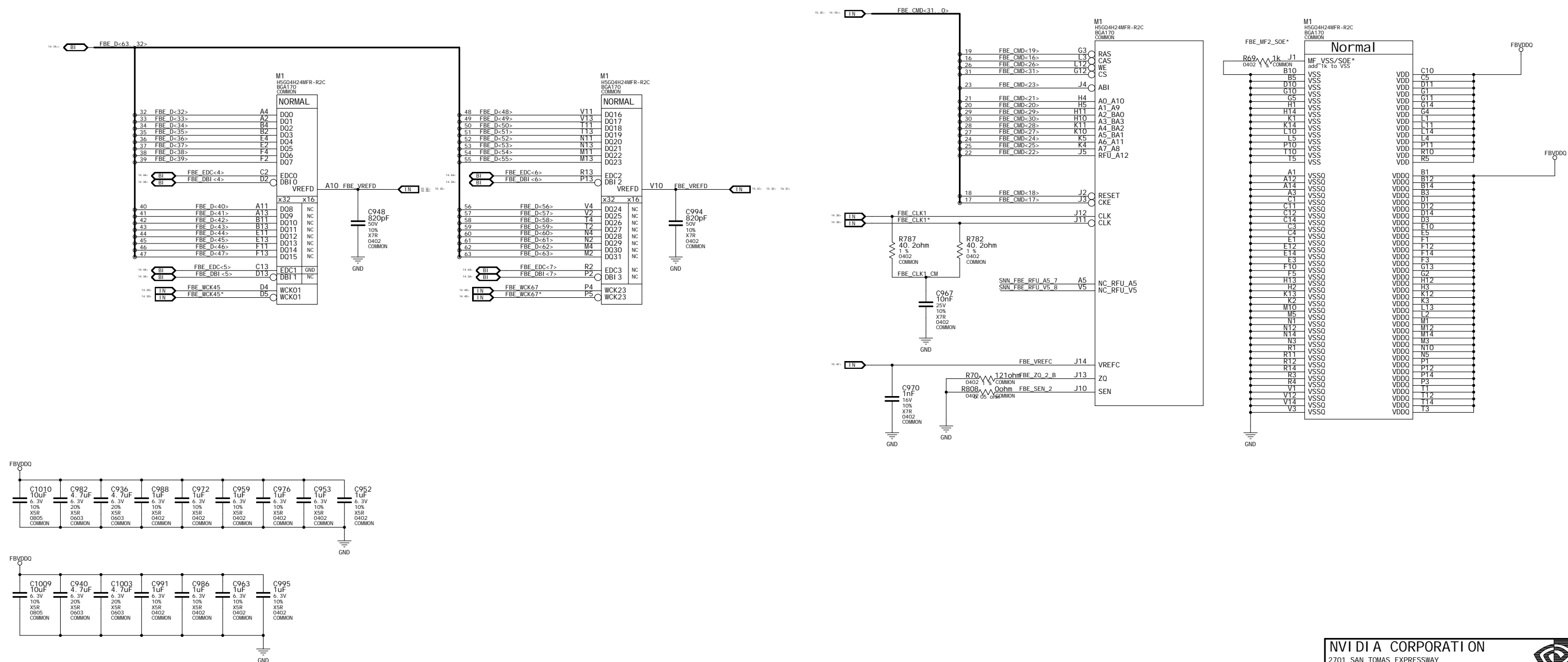
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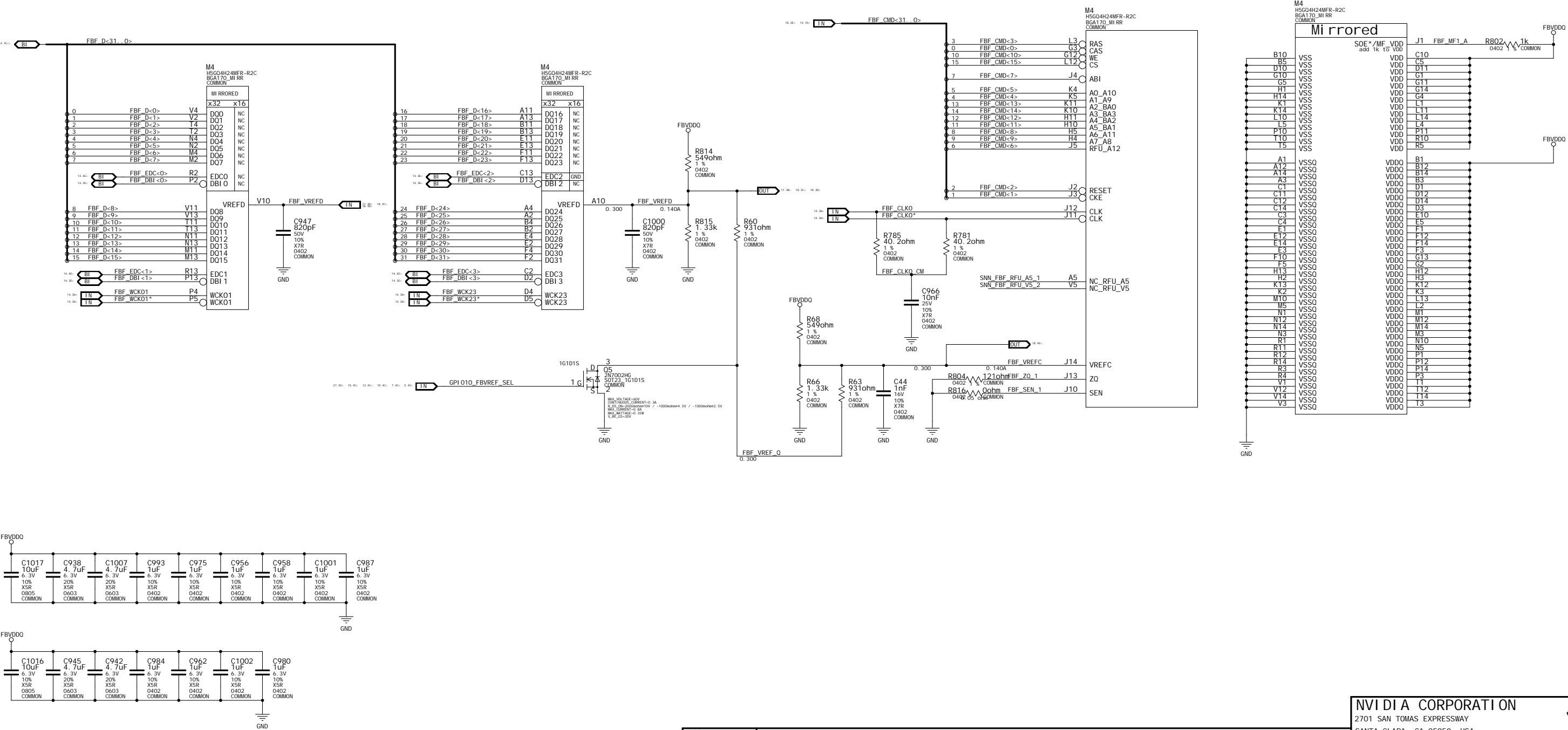




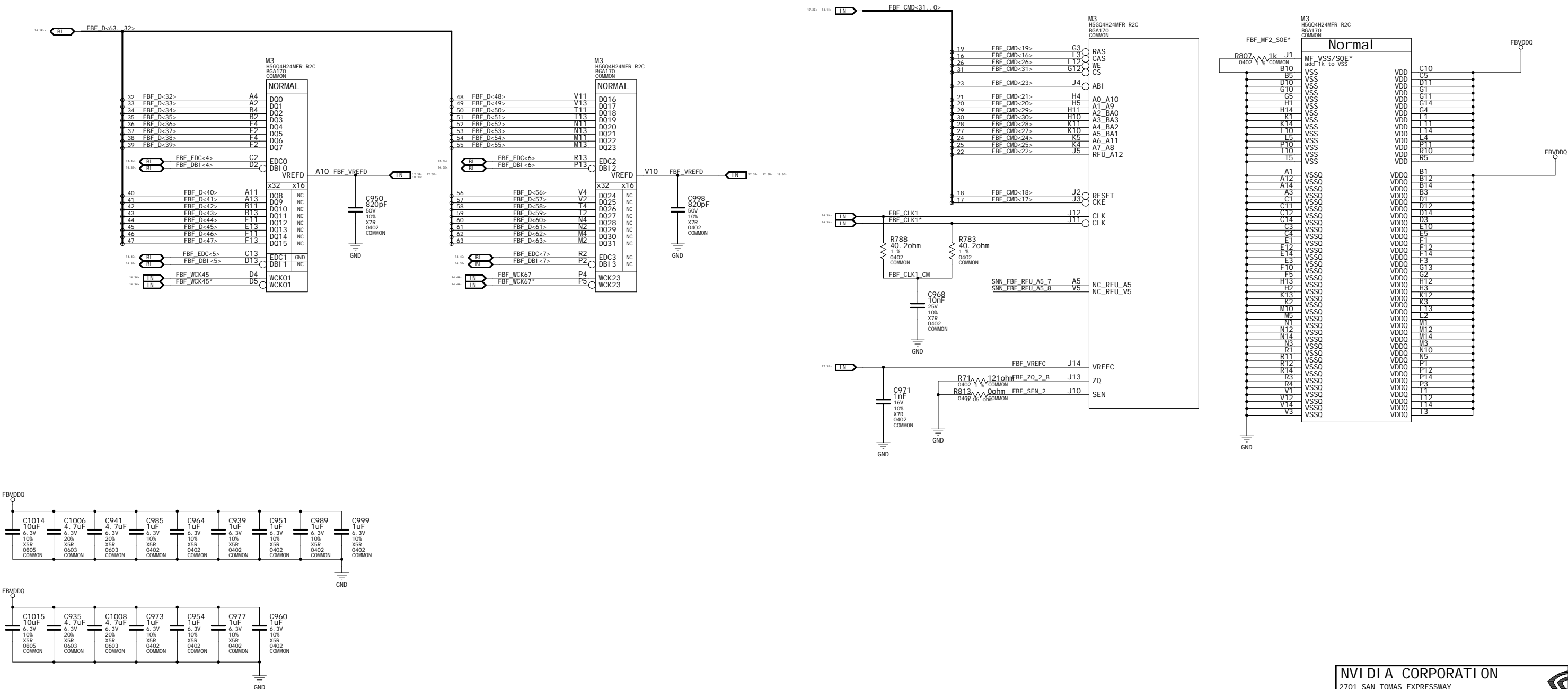
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Page17: MEMORY: FBF Partition 31..0

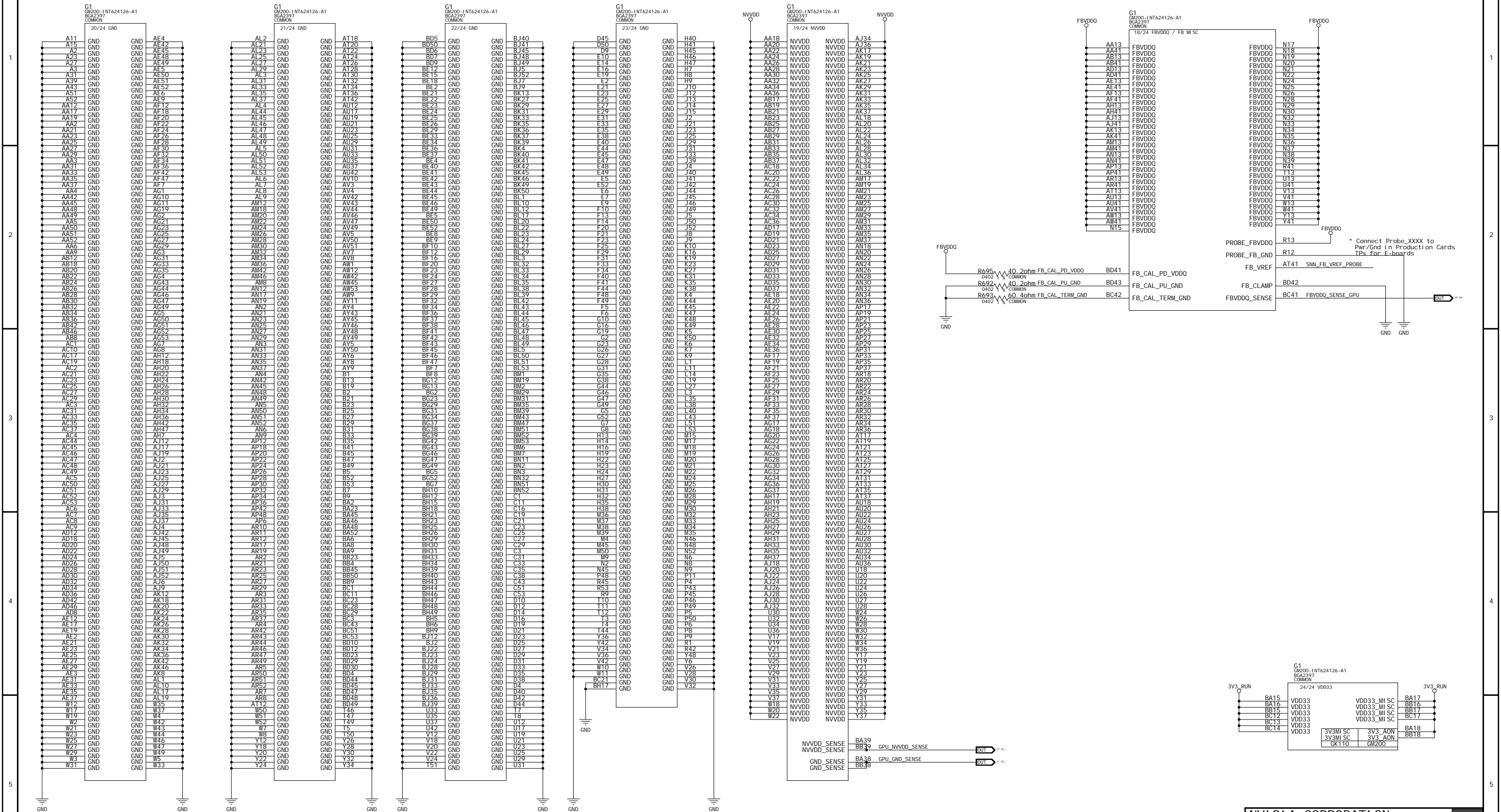


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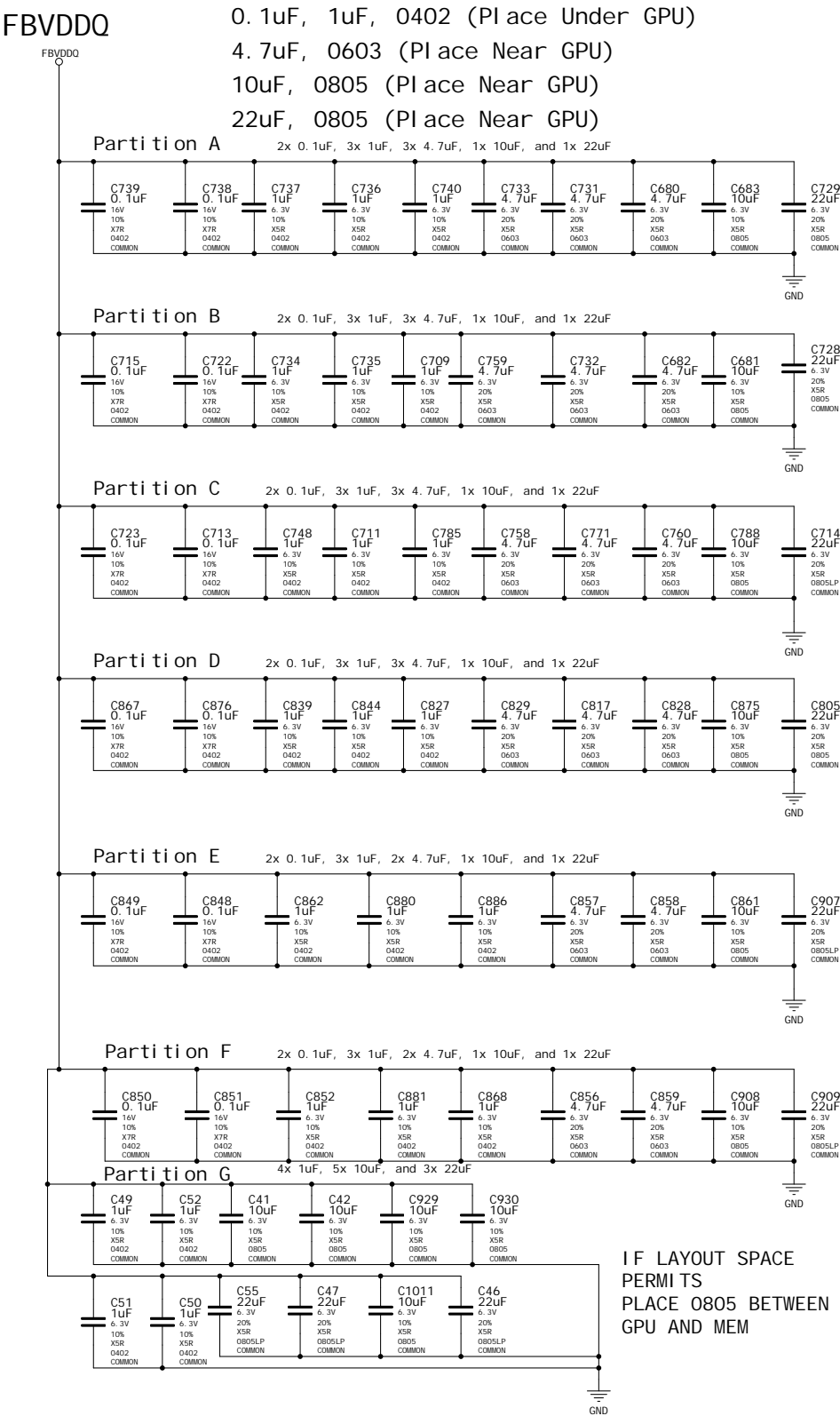


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Page19: GPU PWR and GND

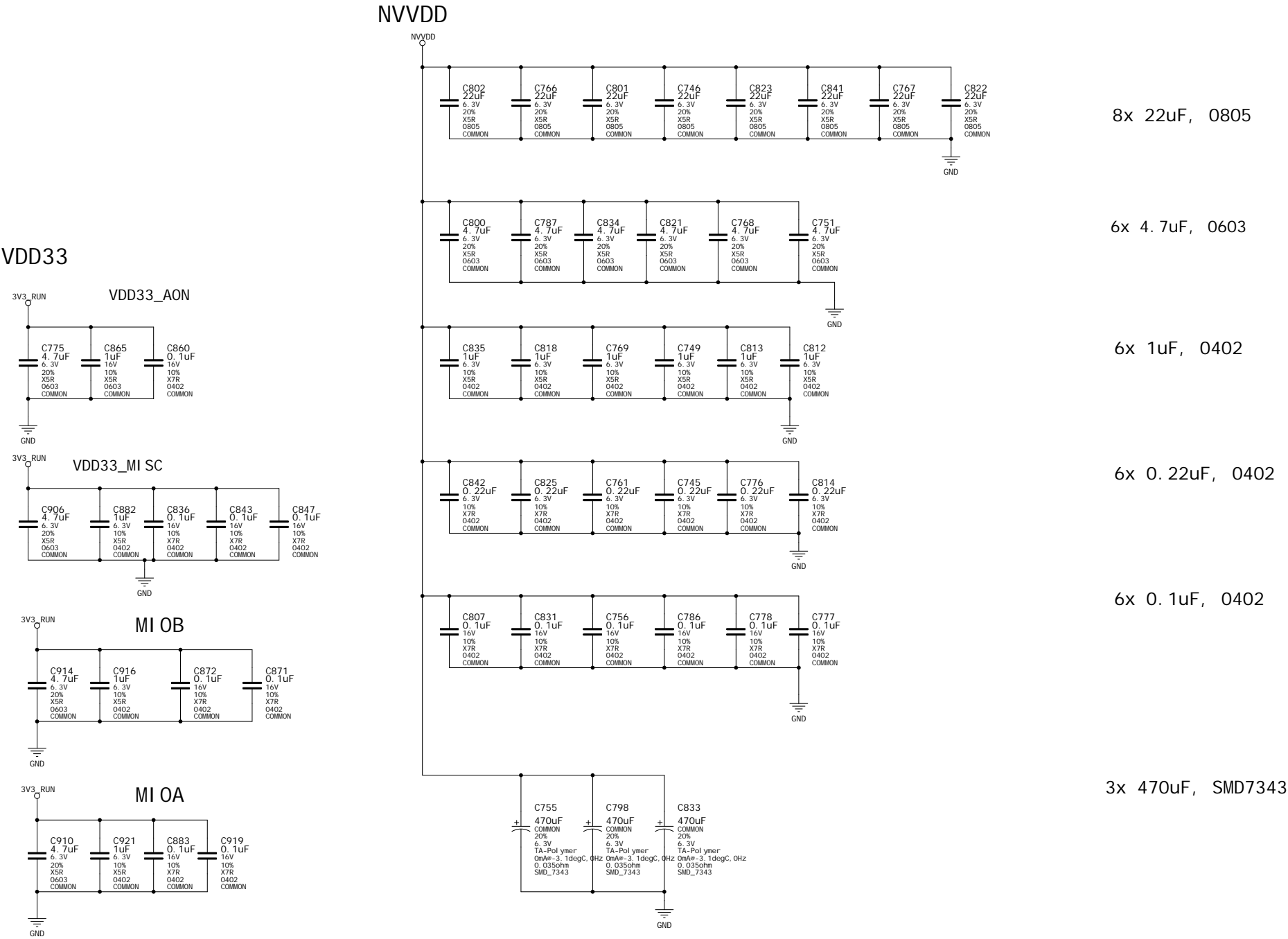


Based on GB3-X GDDR5 FBVDDQ Decap Guideline



NVVDD Decoupling caps. Place under GPU.

NVVDD



Page21: DACA Interface

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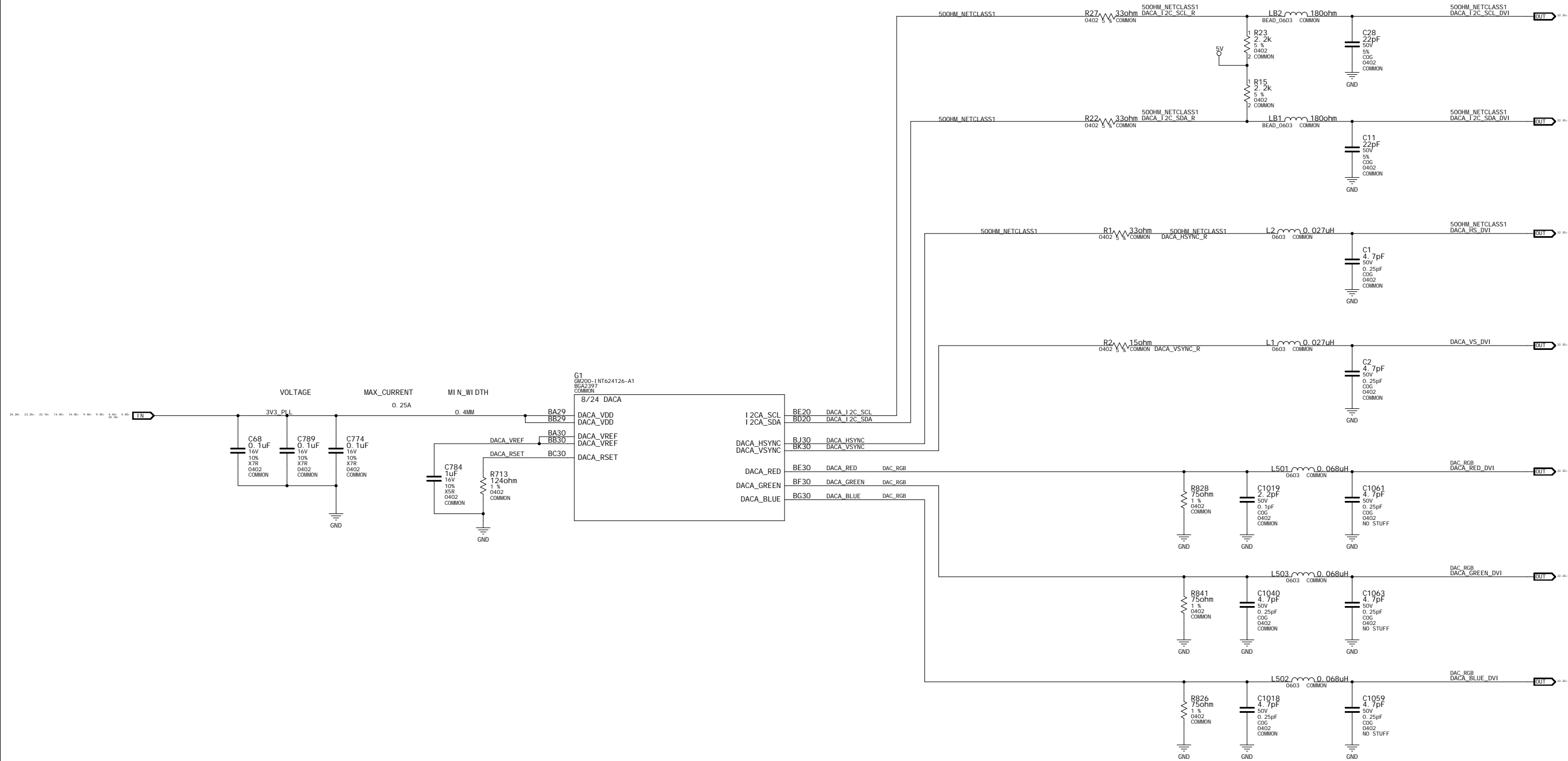
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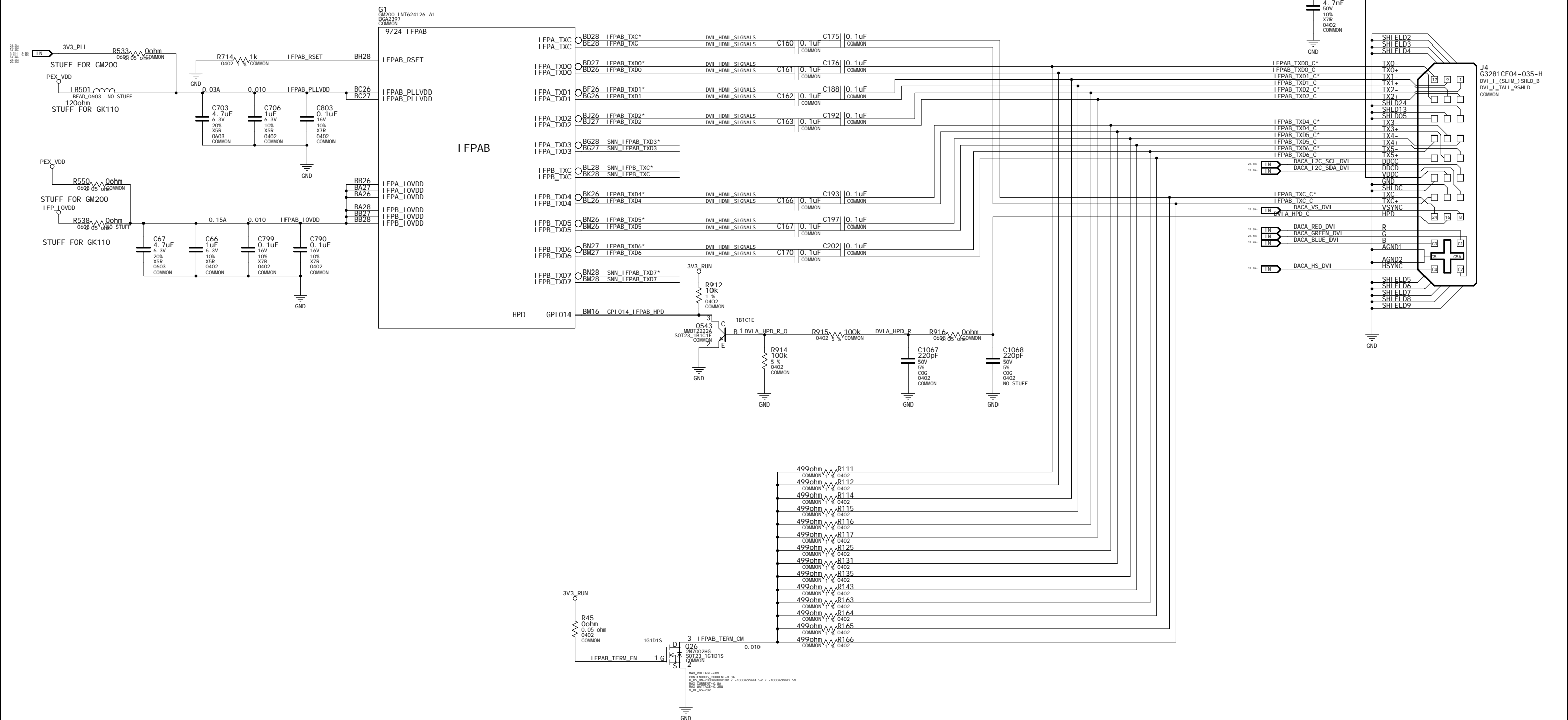
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Page22: I FPAB DVI -I -DL


AC COUPLING NOT NEEDED for KEPLER

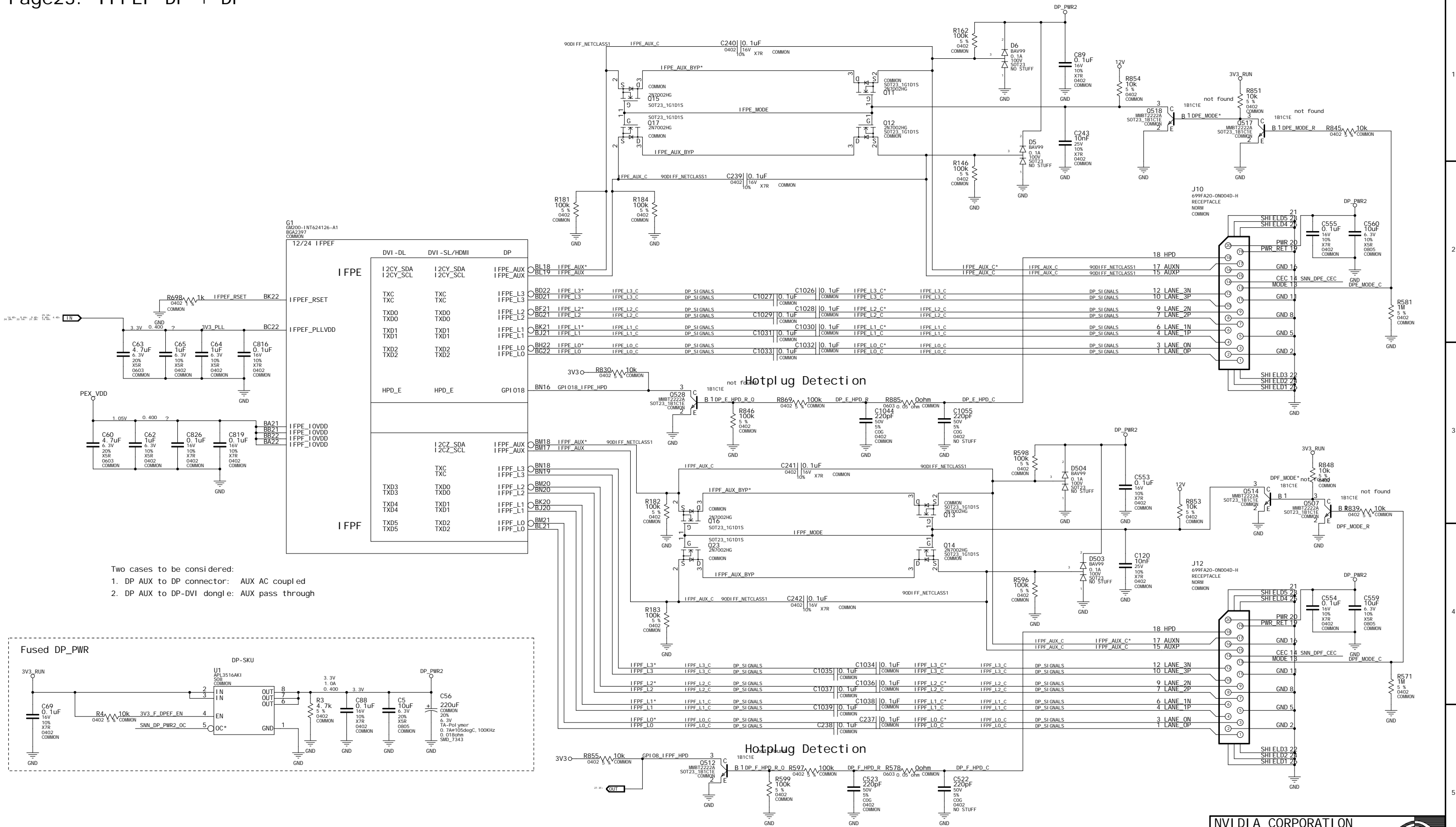
REPLACE WITH ZERO OHM RESISTORS FOR KEPLER SKUs



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PAGE DETAIL L	I FPAB DVI -I -DL

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PAGE DETAIL	IFPEF DP + DP

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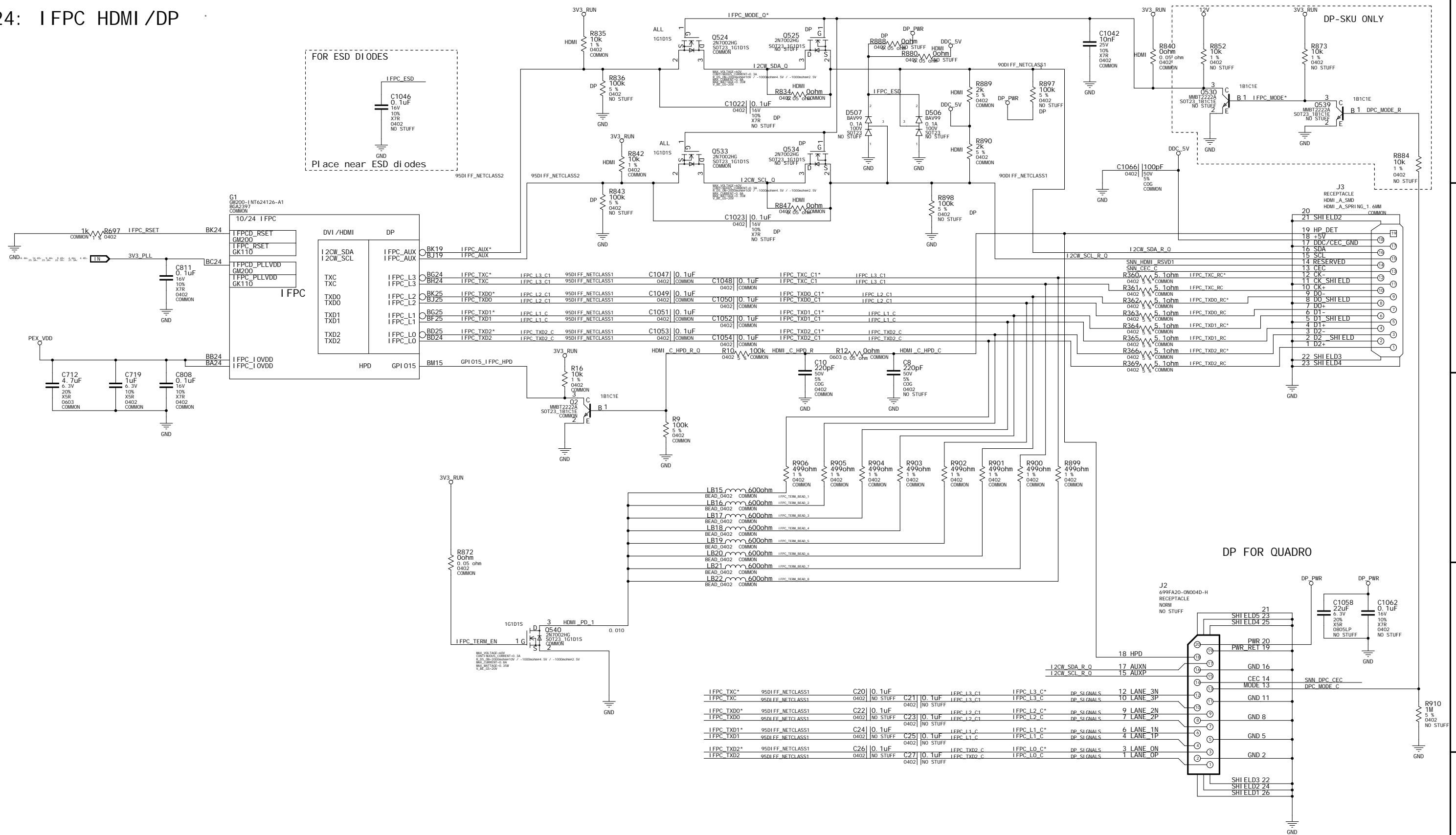
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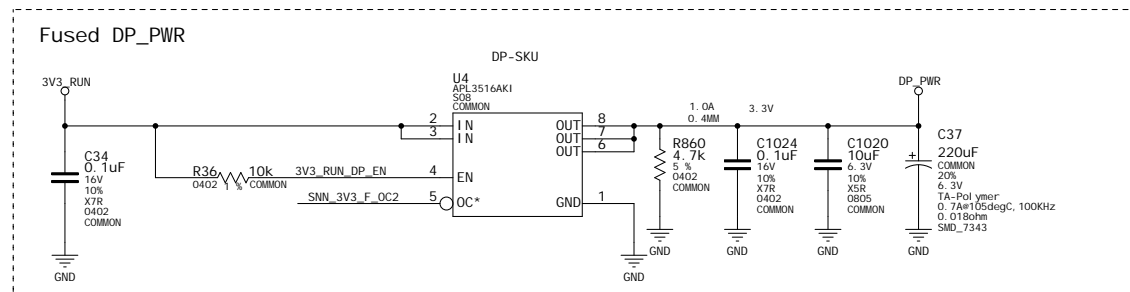
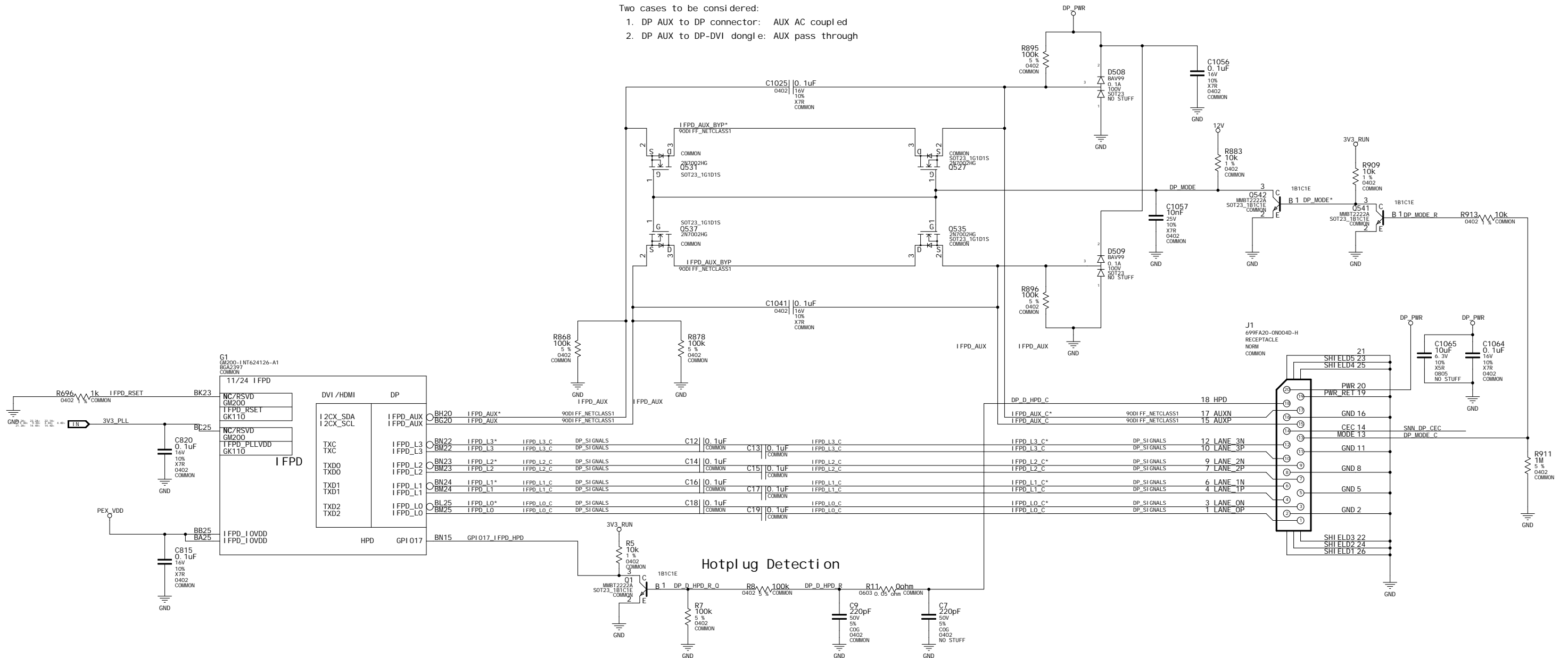
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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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PAGE DETAIL	1FPD DP

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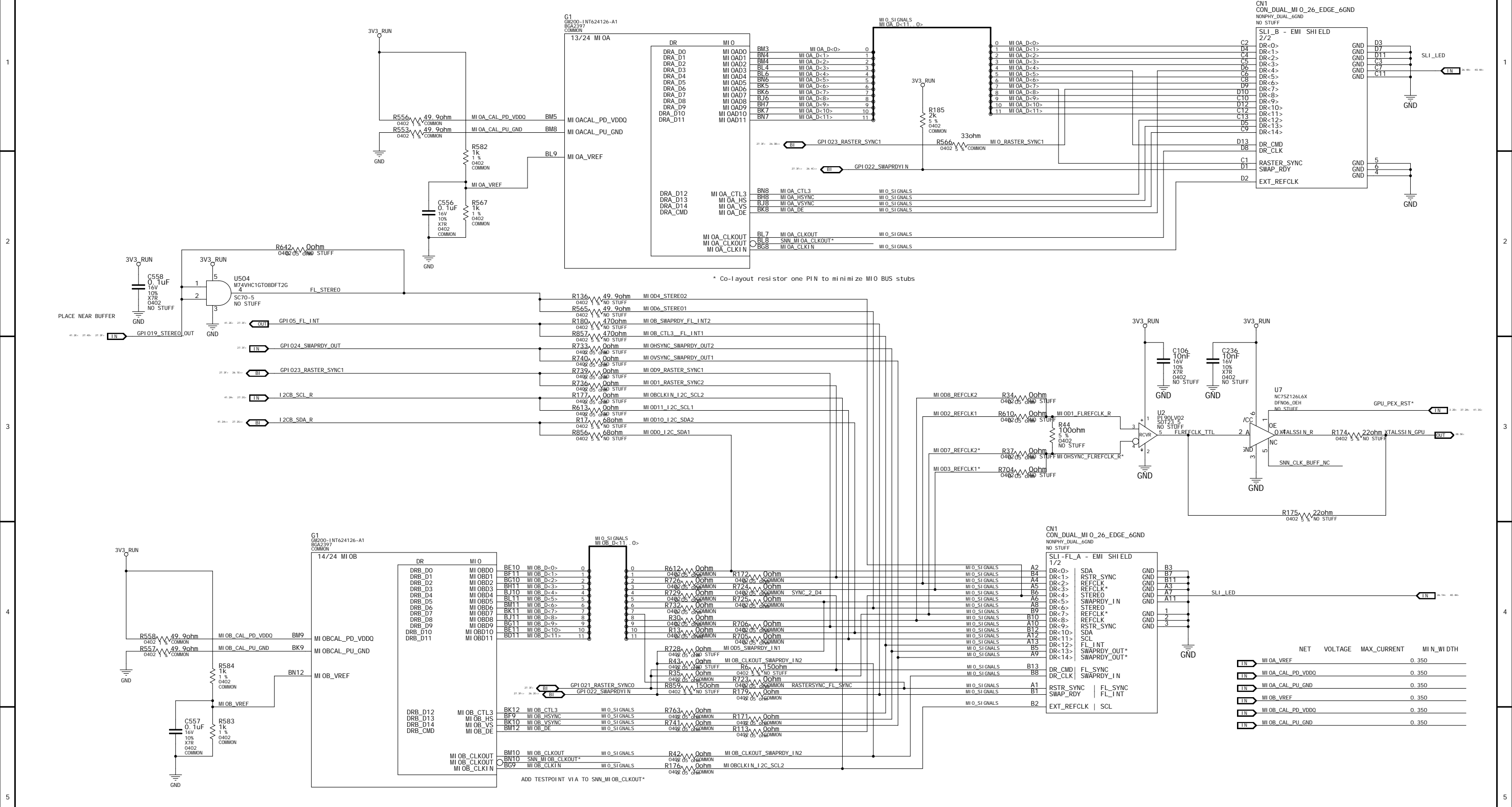
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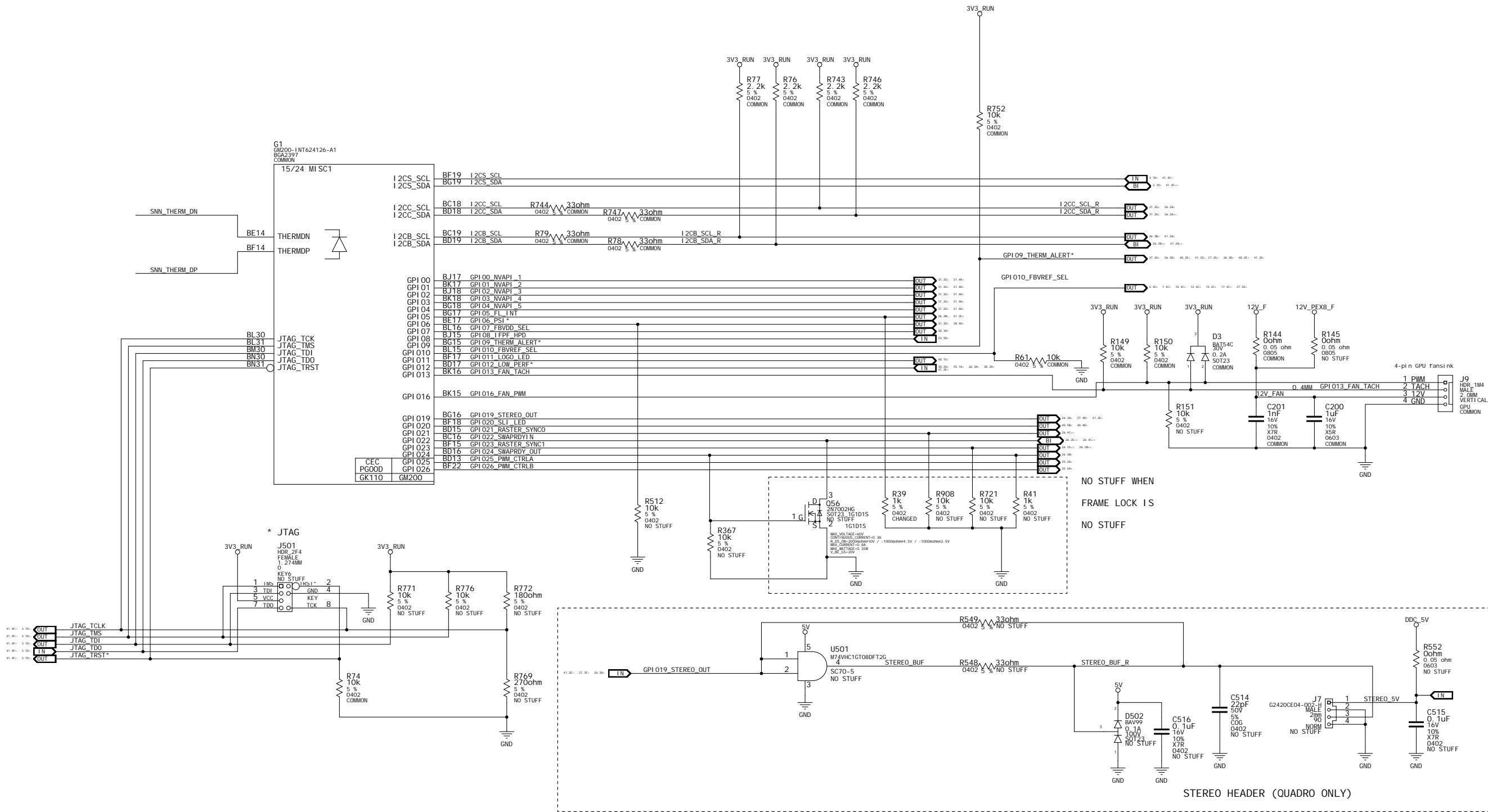


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Page26: MI 0A/B and FRAMELOCK Interface



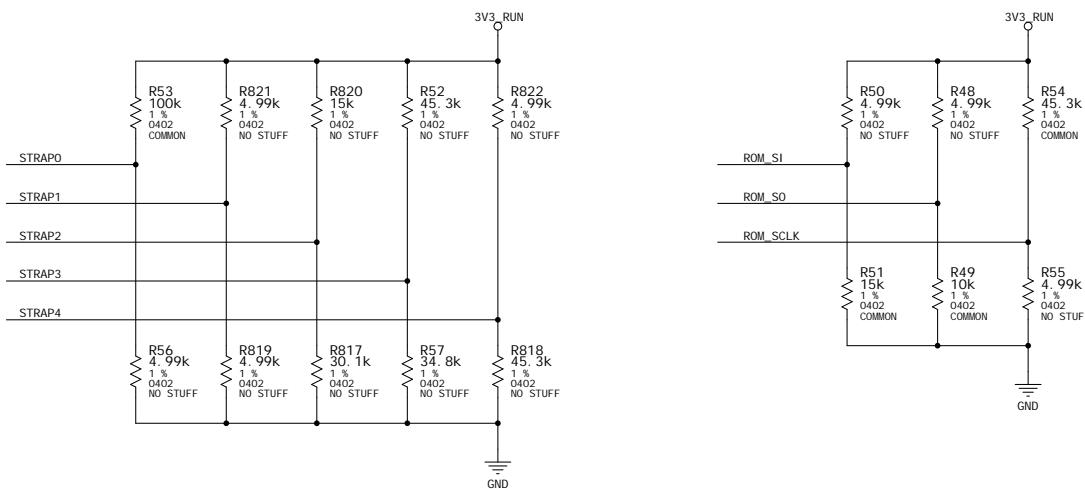


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		GK110	GM200
STRAP0	USER_BIT [3:0]*	0000*	GC6_ENABLE(3.3V) PU
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	N/A
STRAP2	PCI_DEVICEID [3:0]*	100A*	N/A
STRAP3	SOR_EXPOSED [3:0]*	1111*	N/A
STRAP4	[LSB] DP_PLL_VDD_33V*	1* FOR 3_3V*	N/A
	PEX_MAX_SPEED*	1* FOR GEN2/3*	N/A
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	N/A
	[MSB] RESERVED	0*	N/A
ROM_SI	[LSB] RAMCFG[0]*	1*	RAMCFG[0]*
	RAMCFG[1]*	0*	RAMCFG[1]*
	RAMCFG[2]*	1*	RAMCFG[2]*
	[MSB] RAMCFG[3]*	0*	RAMCFG[3]*
ROM_SO	[LSB] VGA_DEVICE*	1*	VGA_DEVICE* 1* For Enable
	SMB_ALT_ADDR*	0*	SMB_ALT_ADDR 0* For Disable
	FB[0]_APERTURE_SIZE*	1* For 128MB*	PCI_E_CFG 0* For Desktop
	[MSB] FB[1]_APERTURE_SIZE*	0* For 128MB*	DEVICE_SEL 0* For Device A
ROM_SCLK	[LSB] PEX_PLL_EN_TERM100*	0* DISABLED*	SOR0_EXPOSED
	PCI_DEVICEID_EXT[5]*	0*	SOR1_EXPOSED
	SUB_VENDOR*	1* Dedicated BIOS*	SOR2_EXPOSED
	[MSB] PCI_DEVICEID_EXT[4]*	0*	SOR3_EXPOSED

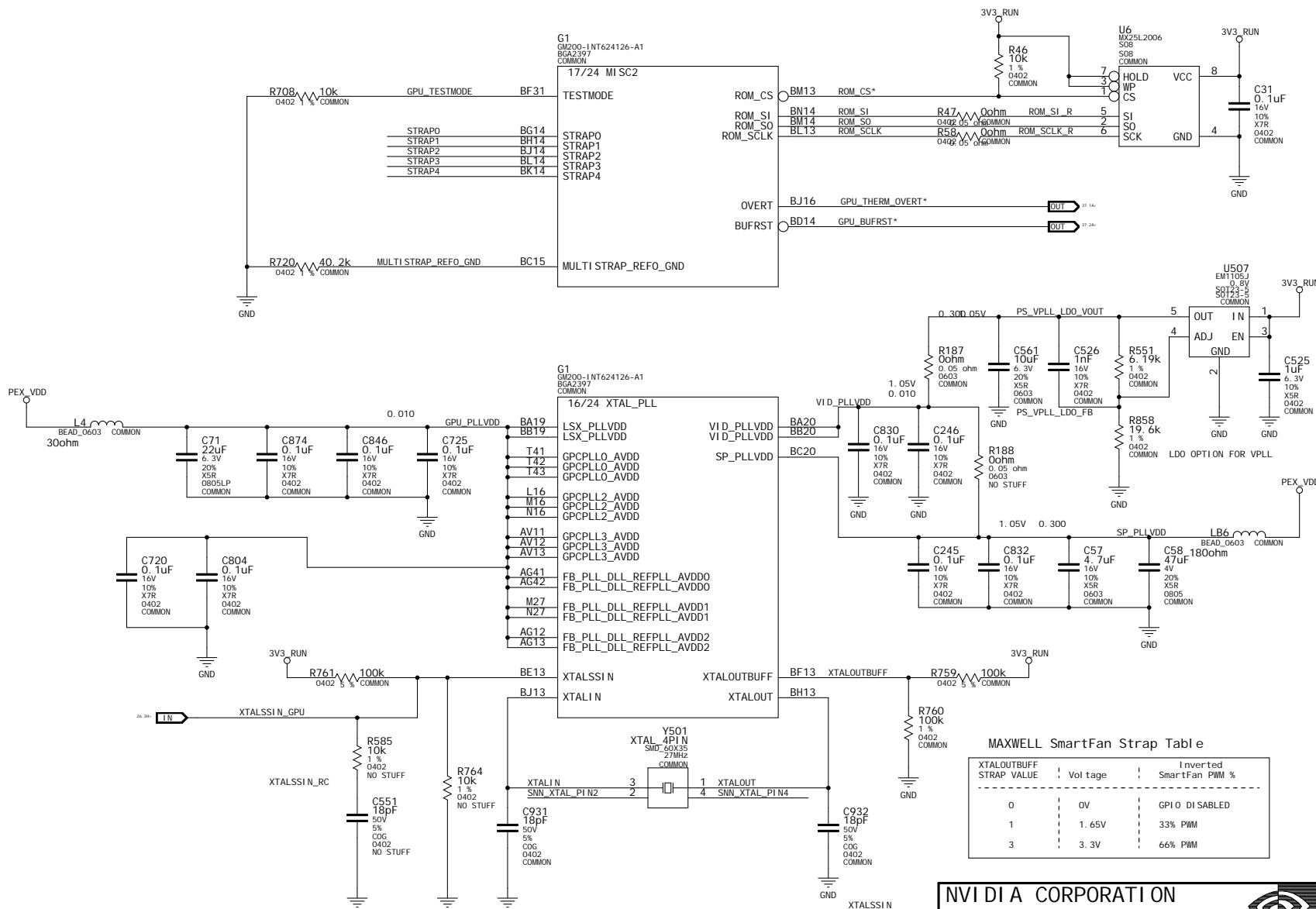
	MULTI_STRAP_REFO_GND
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40. 2k 1% TO GND



	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

x32	DENSITY	MODE	STRAPS
CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	128Mx32	384-bit	Elpi da
0010	128Mx32	384-bit	Hyni x
0011	128Mx32	384-bit	Samsung
0100	64Mx32	384-bit	Hyni x B
0101	64Mx32	384-bit	Elpi da
0110	64Mx32	384-bit	Hyni x
0111	64Mx32	384-bit	Samsung
1000	Reserved		
1001	128Mx32	320-bit	Elpi da
1010	128Mx32	320-bit	Hyni x
1011	128Mx32	320-bit	Samsung
1100	64Mx32	320-bit	Hyni x B
1101	64Mx32	320-bit	Elpi da
1110	64Mx32	320-bit	Hyni x
1111	64Mx32	320-bit	Samsung

x16 DENSITY MODE STRAPS	
CFG[3:0]	Config Width Vendor
0000	Reserved
0001	256Mx16 384-bi t El pi da
0010	256Mx16 384-bi t Hyni x
0011	256Mx16 384-bi t Samsung
0100	128Mx16 384-bi t Hyni x B
0101	128Mx16 384-bi t El pi da
0110	128Mx16 384-bi t Hyni x
0111	128Mx16 384-bi t Samsung
1000	Reserved
1001	256Mx16 320-bi t El pi da
1010	256Mx16 320-bi t Hyni x
1011	256Mx16 320-bi t Samsung
1100	128Mx16 320-bi t Hyni x B
1101	128Mx16 320-bi t El pi da
1110	128Mx16 320-bi t Hyni x
1111	128Mx16 320-bi t Samsung



MAXWELL SmartFan Strap Table		
XTALOUTBUFF STRAP VALUE	Vol tage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	1.65V	33% PWM
3	3.3V	66% PWM

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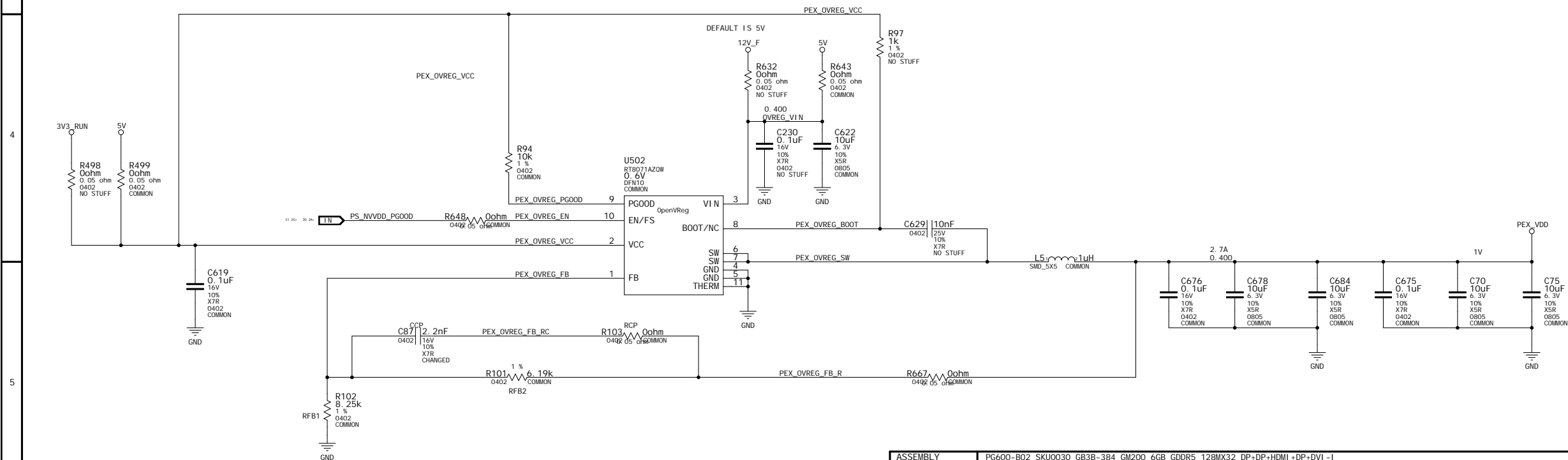
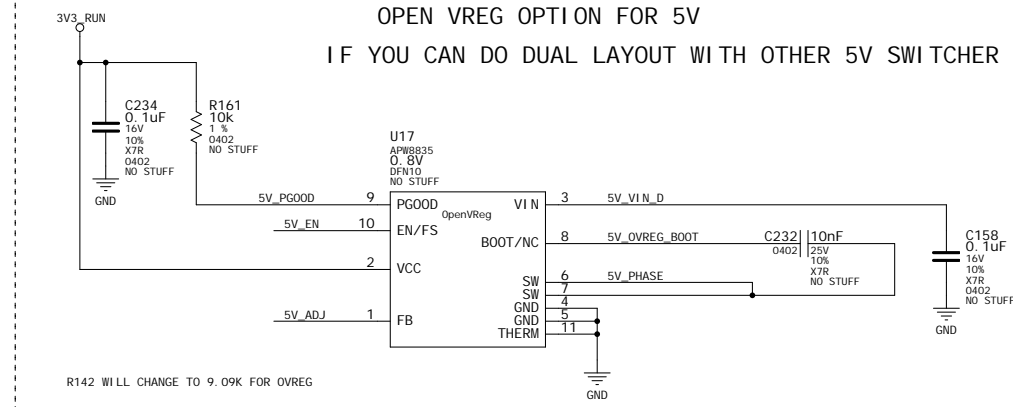
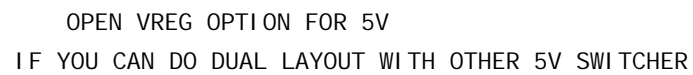
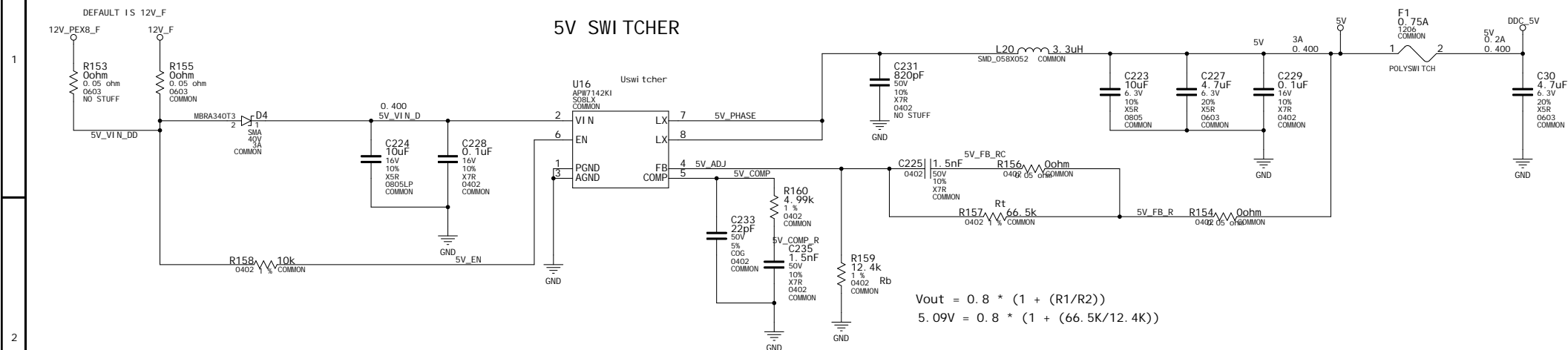
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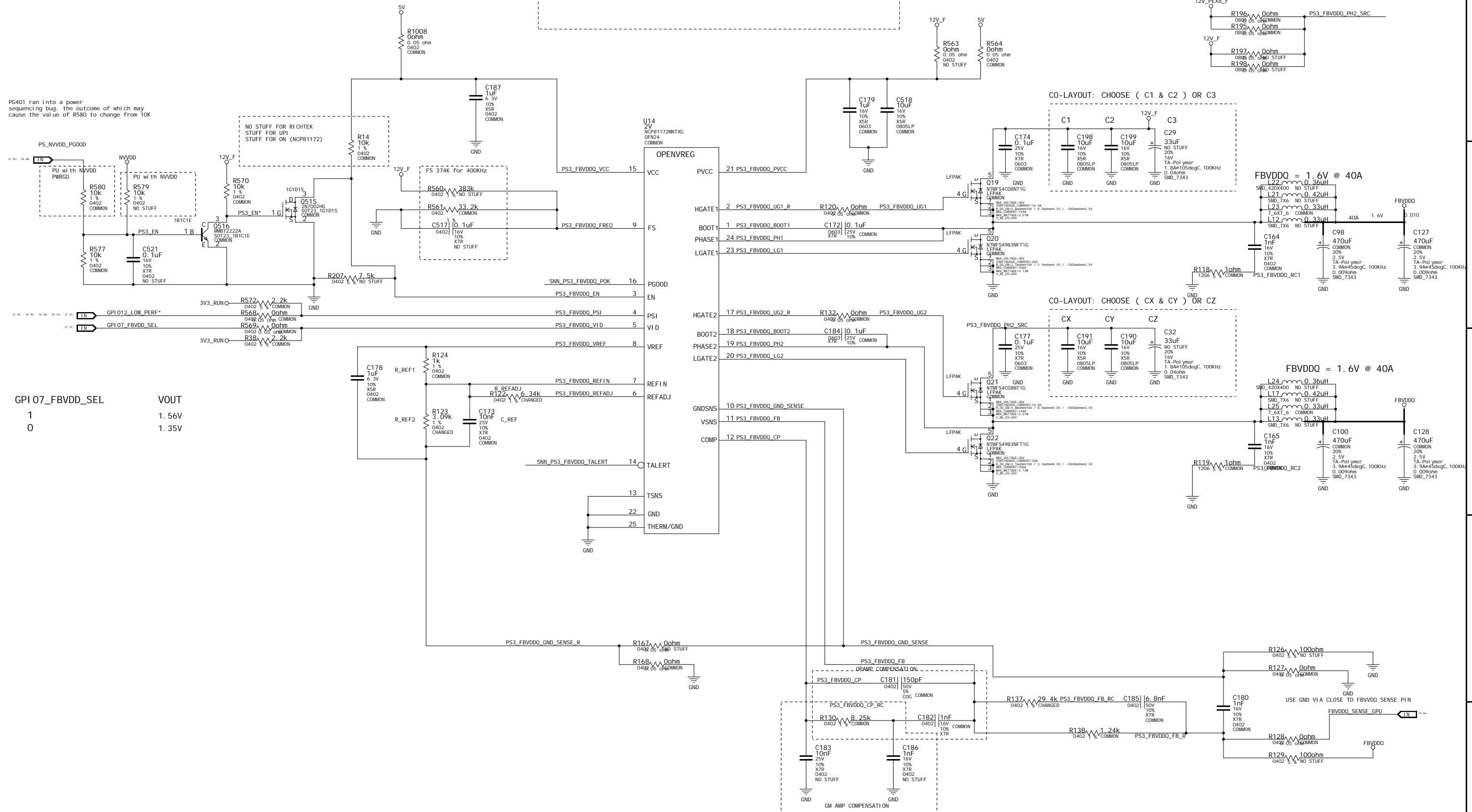
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Page30: PS: FBVDDQ



ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI +DP+DVI -
PAGE DETAIL	PS: FBVDD/Q

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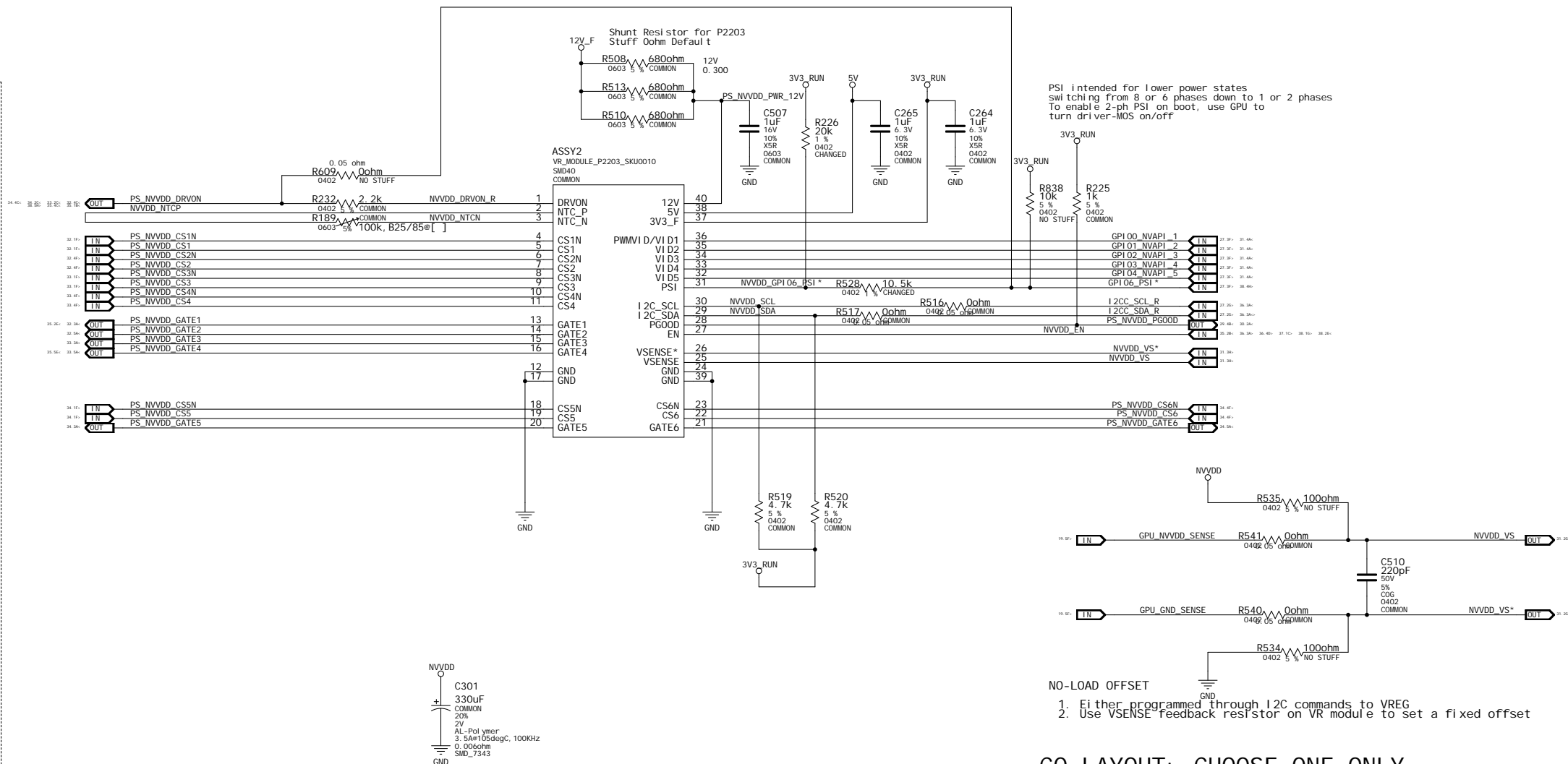
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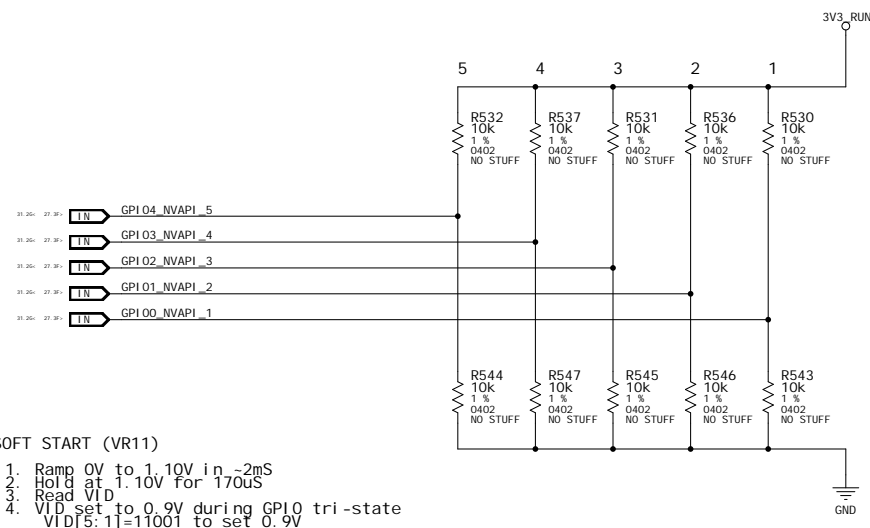
V I D T a b l e					
GPI 04	GPI 03	GPI 02	GPI 01	GPI 00	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1. 2125V
0	0	0	0	1	1. 2000V
0	0	0	1	0	1. 1875V
0	0	0	1	1	1. 1750V
0	0	1	0	0	1. 1625V
0	0	1	0	1	1. 1500V
0	0	1	1	0	1. 1375V
0	0	1	1	1	1. 1250V
0	1	0	0	0	1. 1125V
0	1	0	0	1	1. 1000V
0	1	0	1	0	1. 0875V
0	1	0	1	1	1. 0750V
0	1	1	0	0	1. 0625V
0	1	1	0	1	1. 0500V
0	1	1	1	0	1. 0375V
0	1	1	1	1	1. 0250V
1	0	0	0	0	1. 0125V
1	0	0	0	1	1. 0000V
1	0	0	1	0	0. 9875V
1	0	0	1	1	0. 9750V
1	0	1	0	0	0. 9625V
1	0	1	0	1	0. 9500V
1	0	1	1	0	0. 9375V
1	0	1	1	1	0. 9250V
1	1	0	0	0	0. 9125V
1	1	0	0	1	0. 9000V
1	1	0	1	0	0. 8875V
1	1	0	1	1	0. 8750V
1	1	1	0	0	0. 8625V
1	1	1	0	1	0. 8500V
1	1	1	1	0	0. 8375V
1	1	1	1	1	0. 8250V



CO-LAYOUT: CHOOSE ONE ONLY

Library Part

Library Part



SOFT START (VR11)


1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPIO tri-state
VID[5:1]=11001 to set 0.9V

P-STATE VOLTAGES

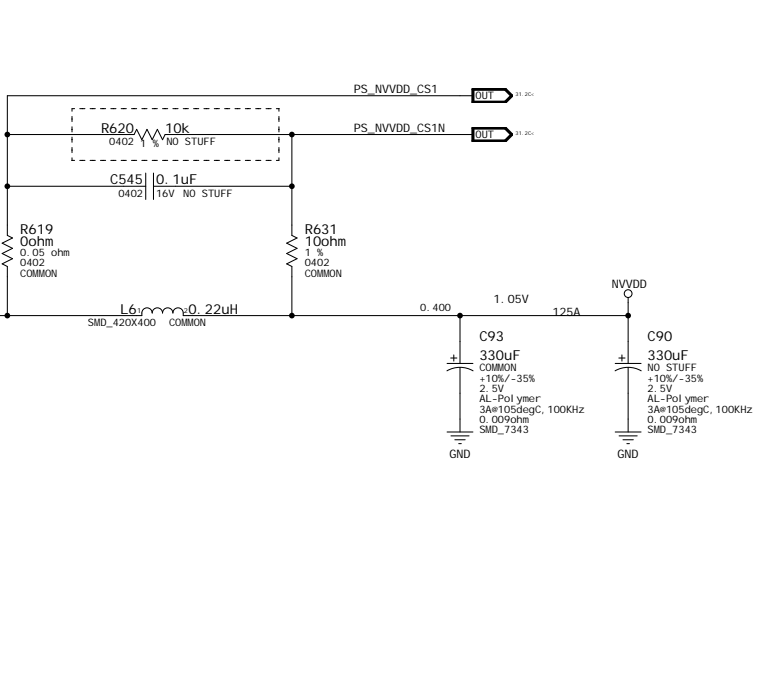
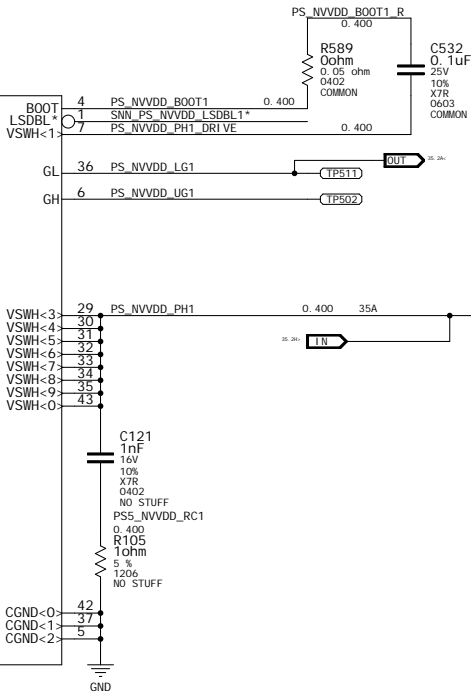
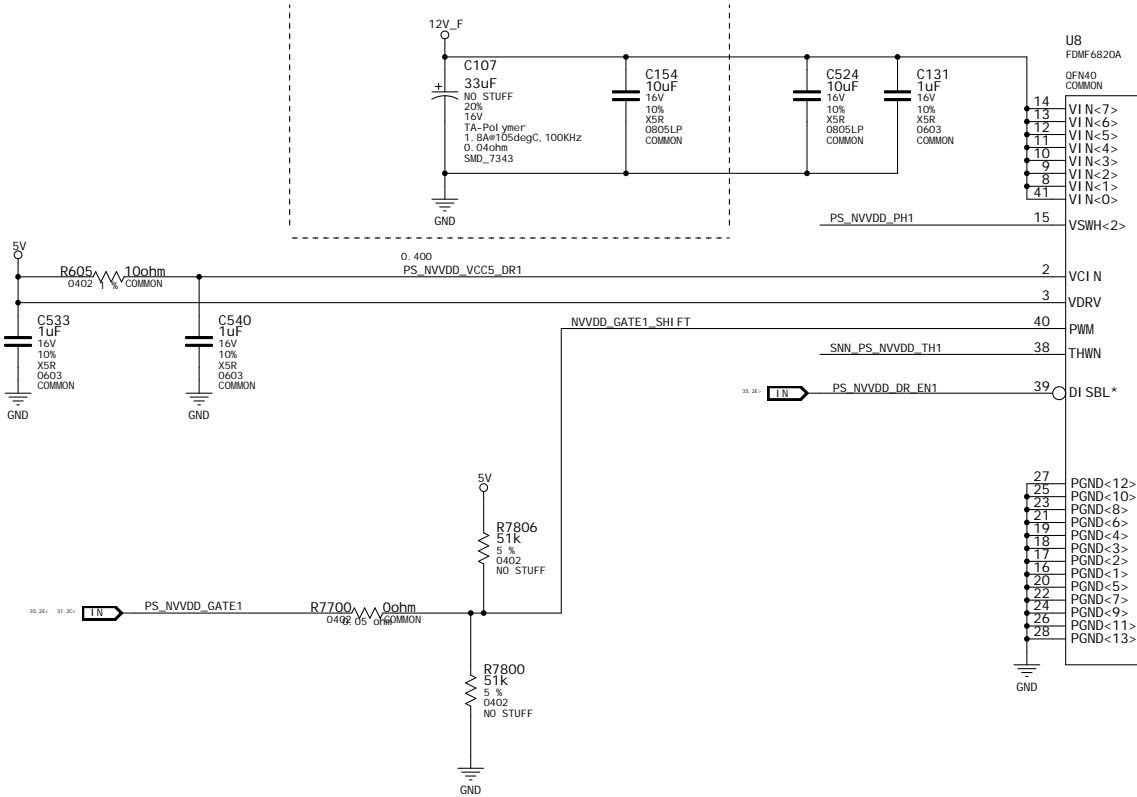
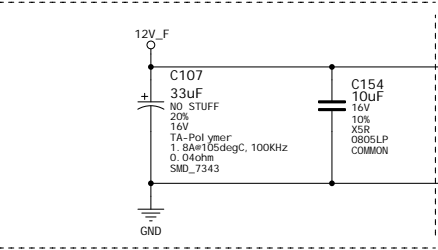
1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V

ASSEMBLY	PG600-B02 SKU0030 G83B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI+DP+DVI -I
PAGE DETAIL	PS: NVVDD Controller

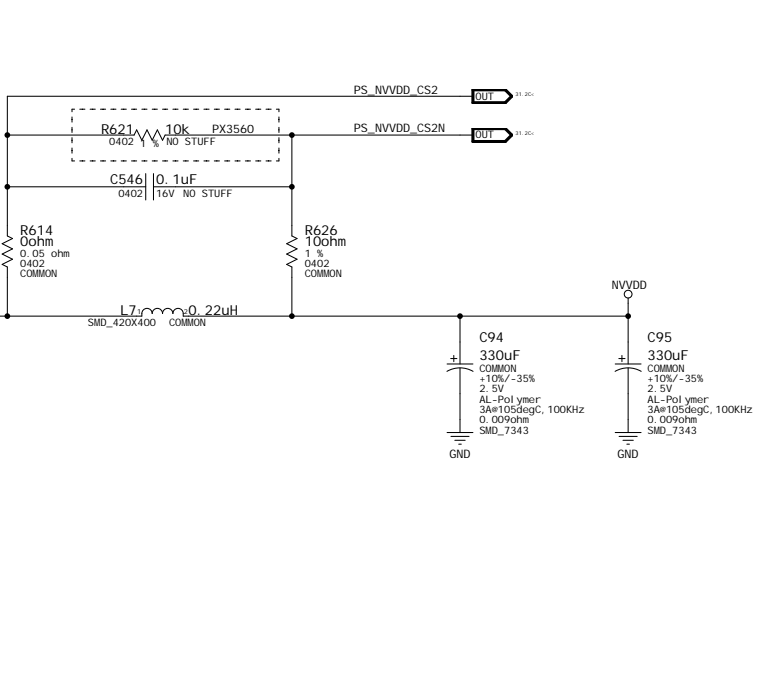
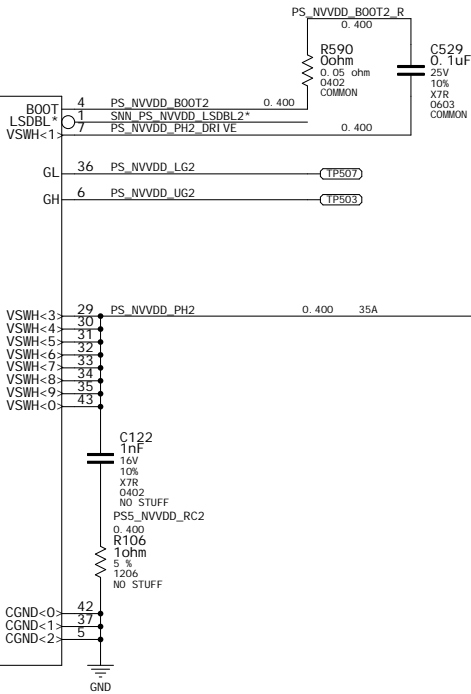
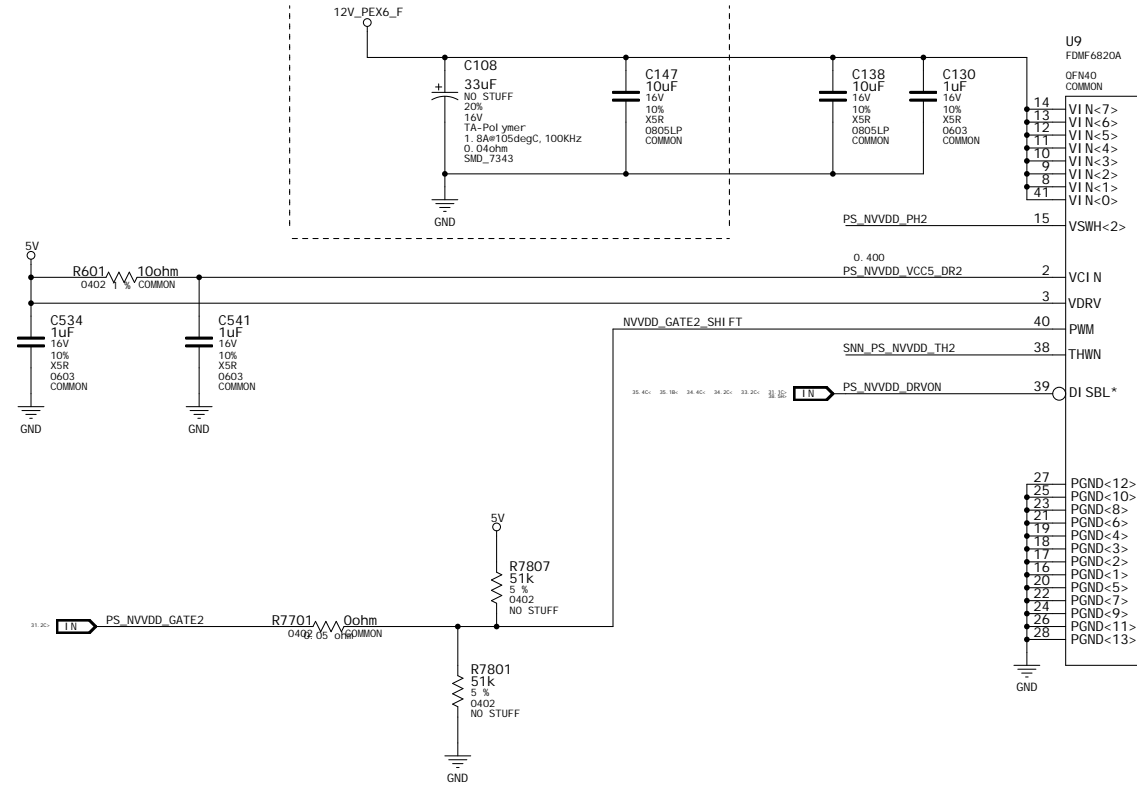
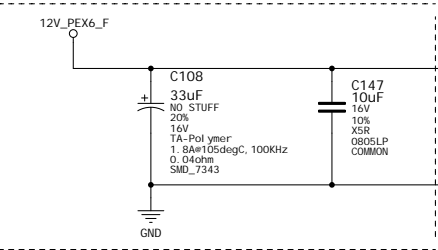
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CO-LAYOUT: STUFF ONLY ONE



CO-LAYOUT: STUFF ONLY ONE



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ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI +DP+DVI-I
PAGE DETAIL	PS: NVVDD Phase 1, 2

NV_PN 600-1G600-0030-QS1

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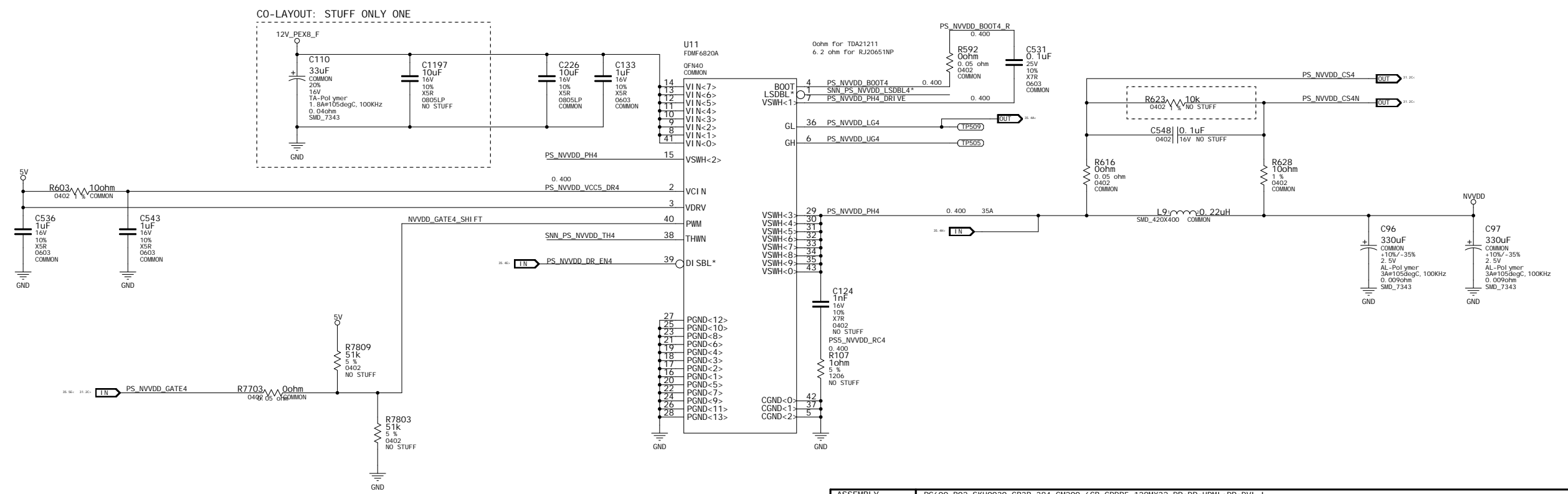
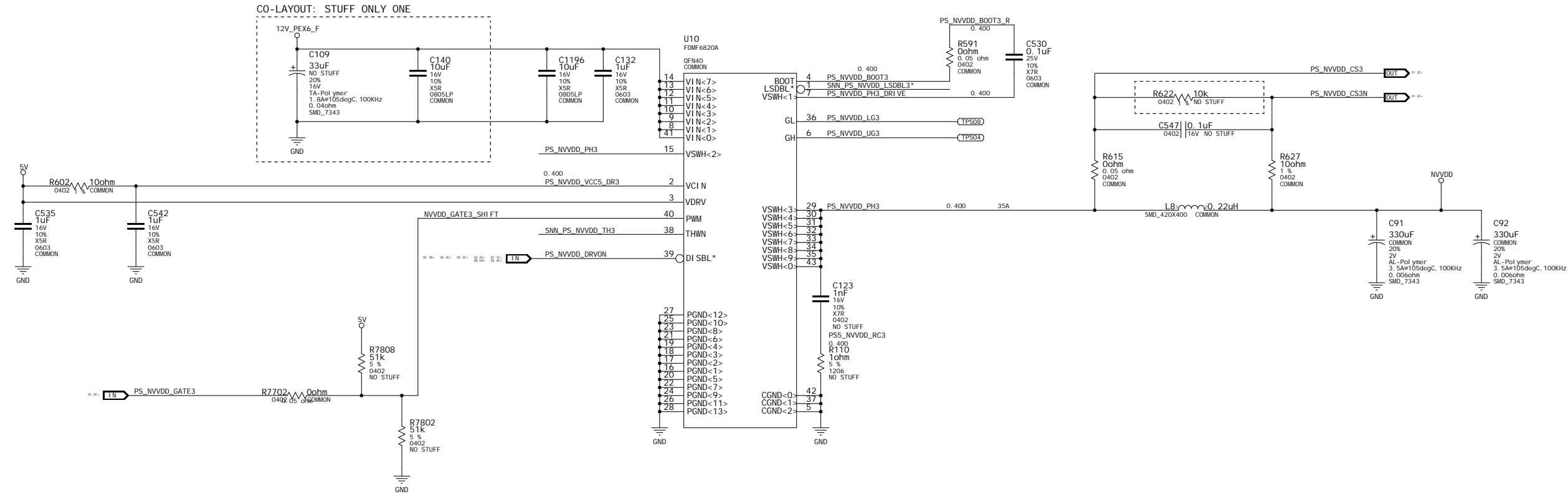
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PCB REV	PG600-B02	PAGE	33 OF 41
BOM REV	A	DATE	21-APR-2015

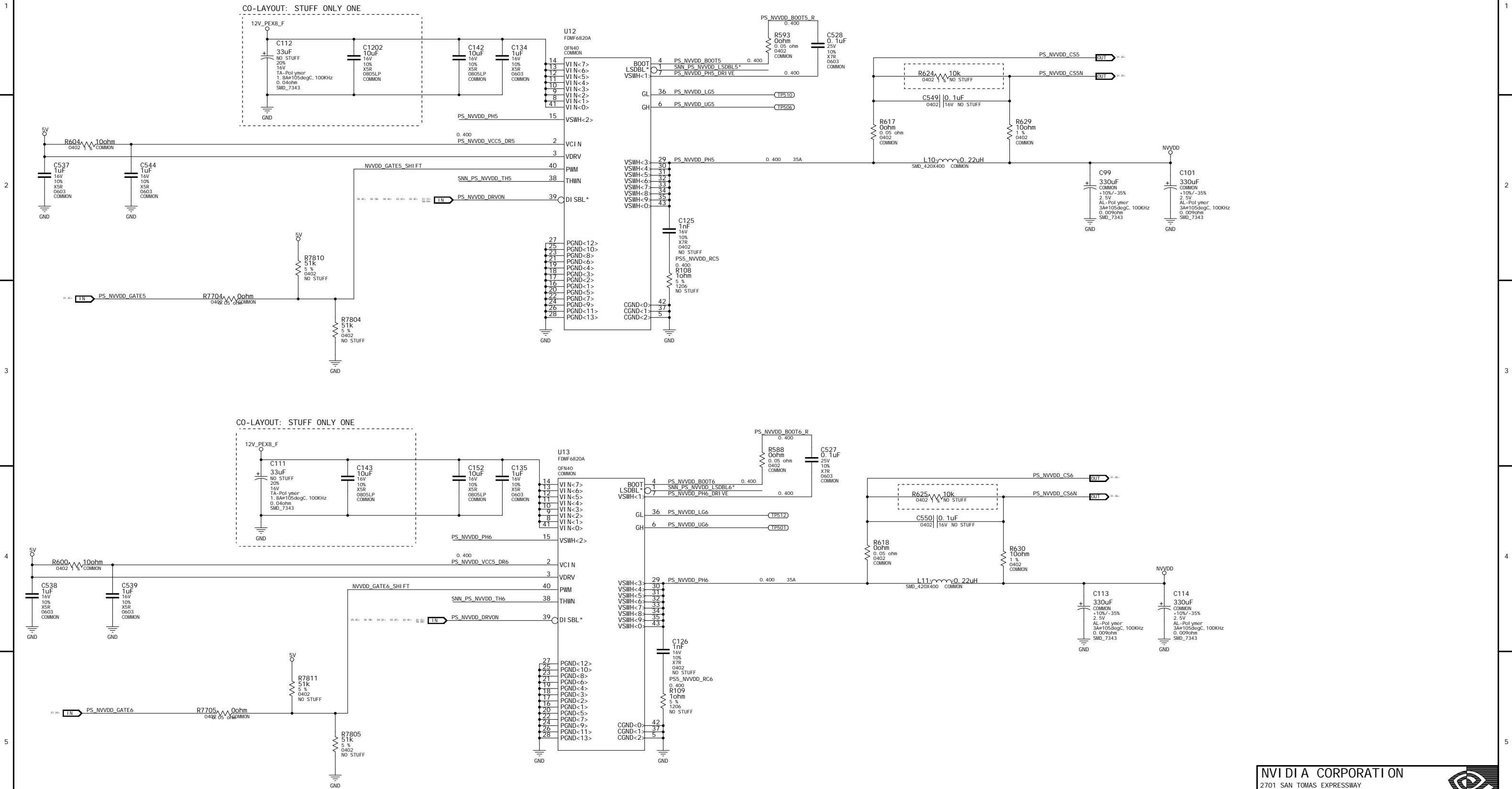
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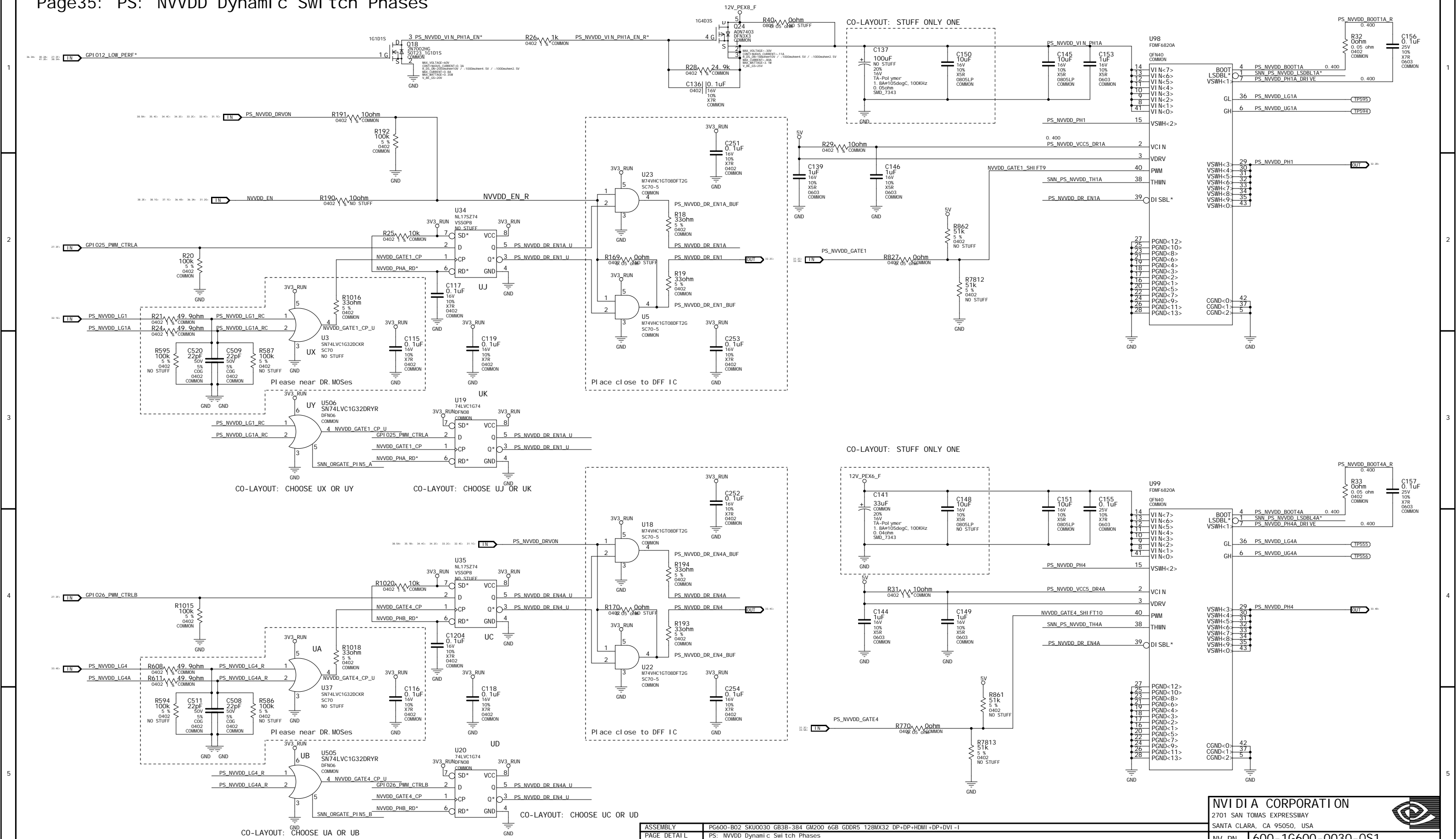
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NV_PN	600-1G600-0030-QS1		
PCB REV	PG600-B02	PAGE	34 OF 41
BOM REV	A	DATE	21-APR-2015

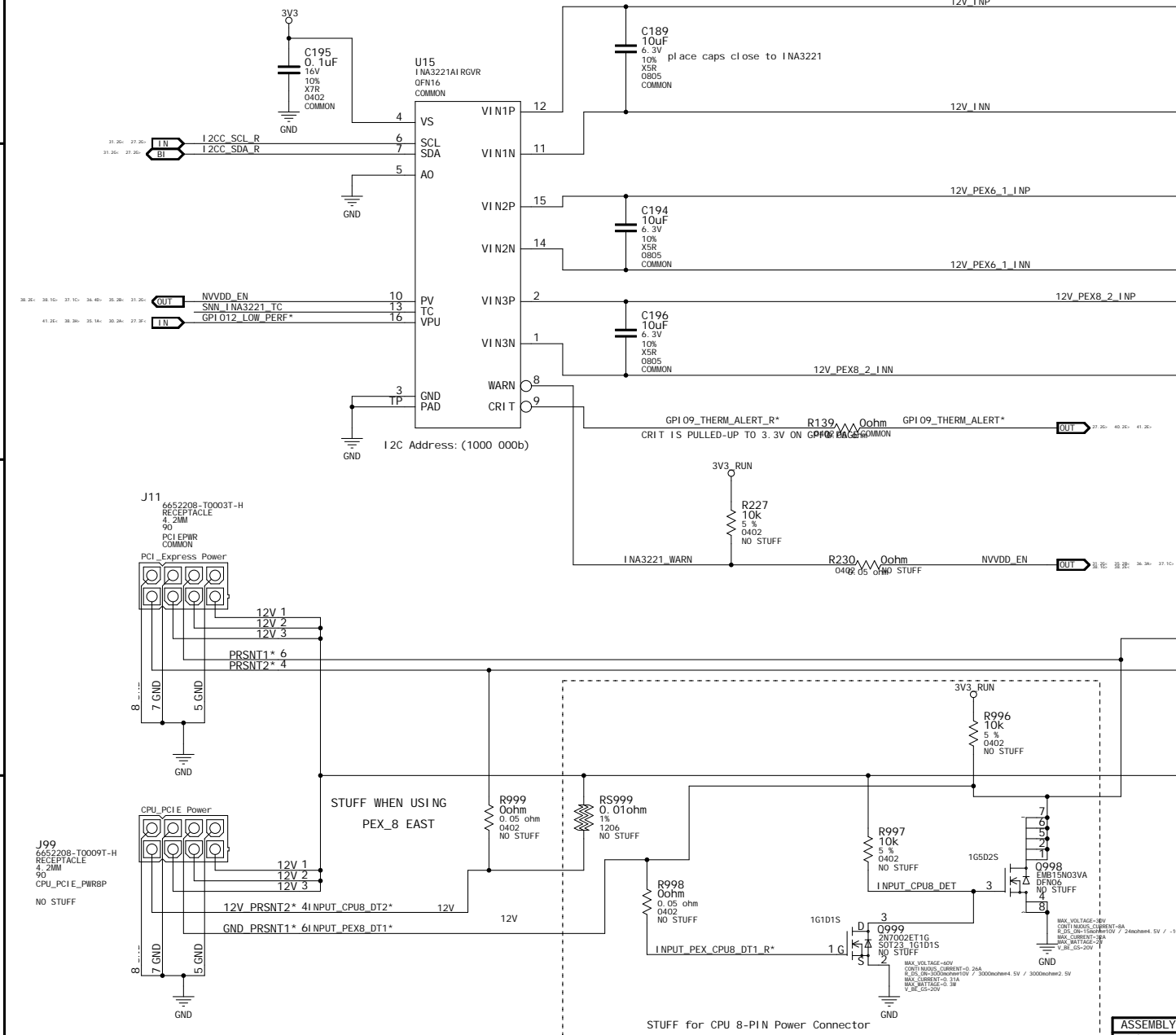
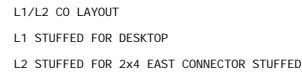
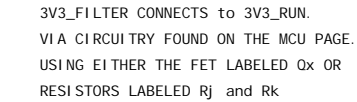
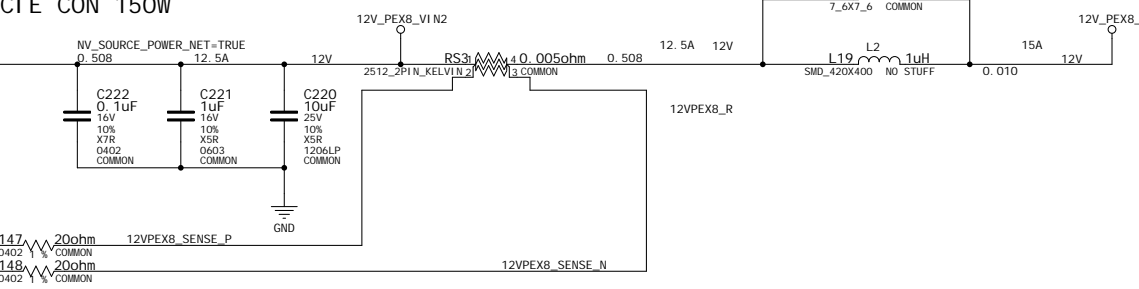
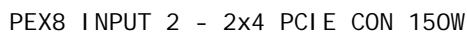
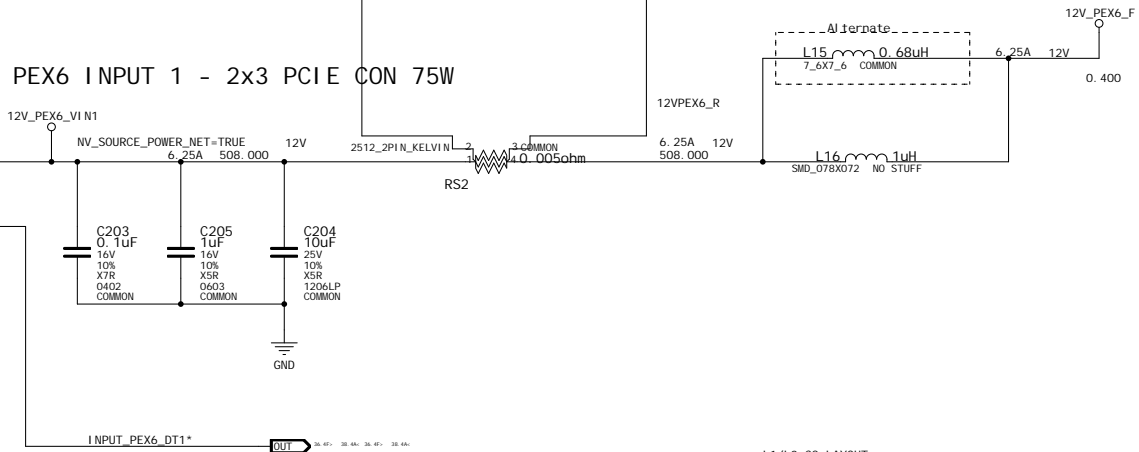
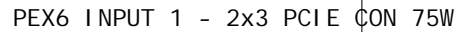
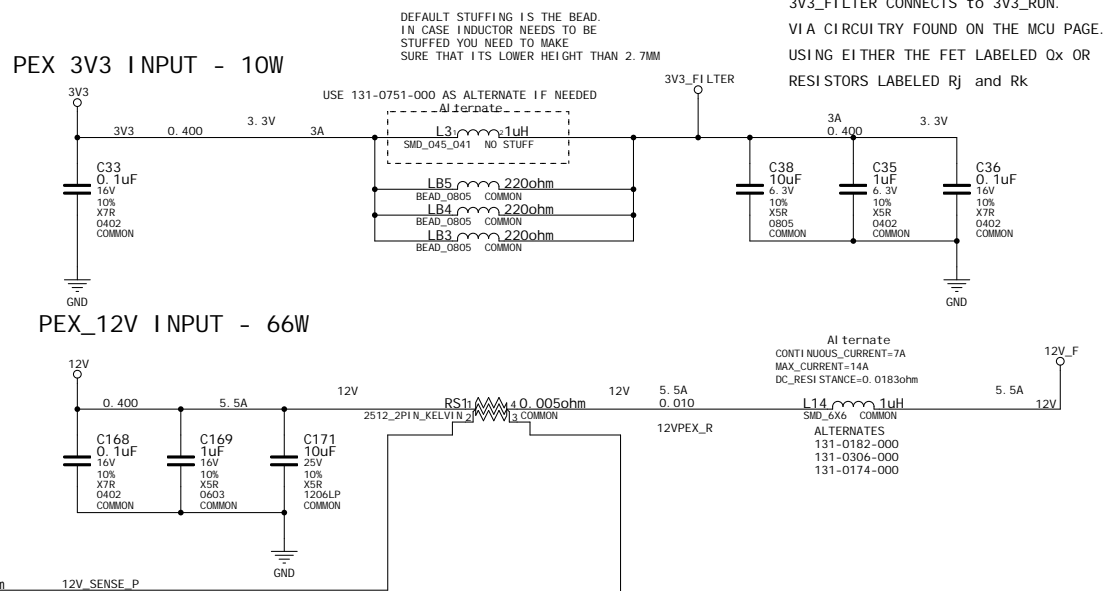
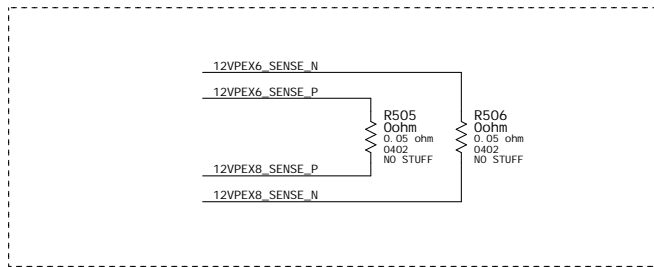
Page35: PS: NVVDD Dynami c Swi tch Phases



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ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI +DP+DVI -
PAGE DETAIL	PS: NVDD Dynamic Switch Phases

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ASSEMBLY	
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

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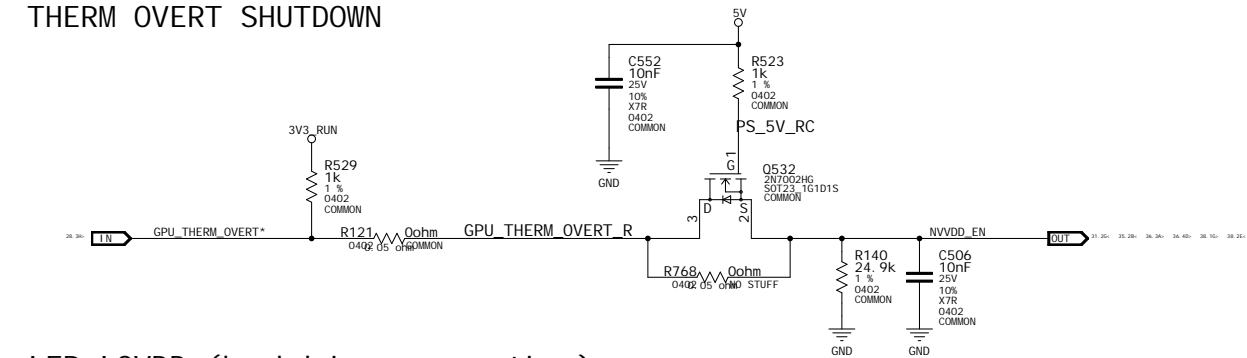
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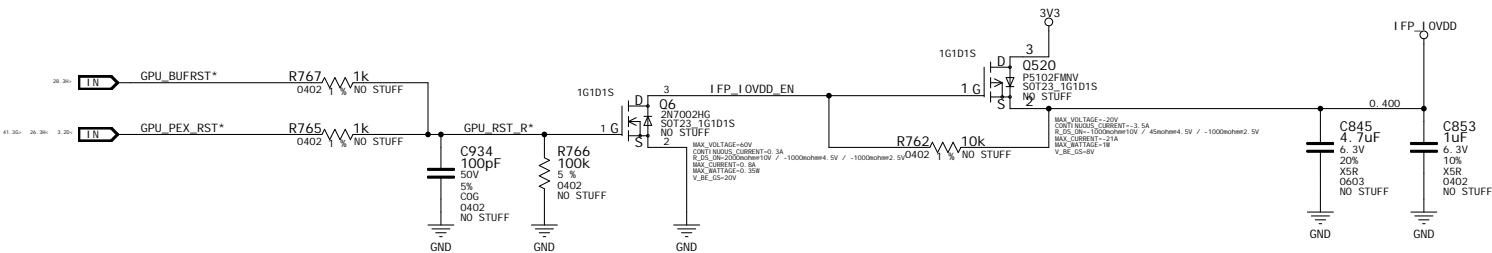
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THERM OVERT SHUTDOWN



I FP_I OVDD (backdri ve preventi on)



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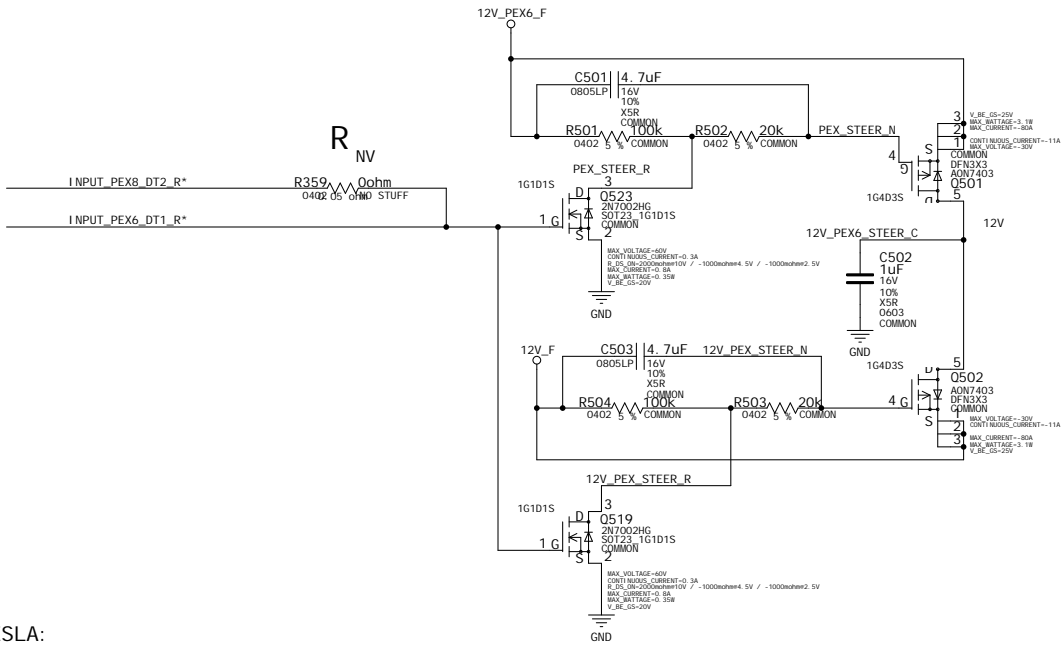
PCB REV PG600-B02 PAGE 37 OF 41

BOM REV A DATE 21-APR-2015

Page38: PS: 12V Current Steering & Hot Unplug Detect

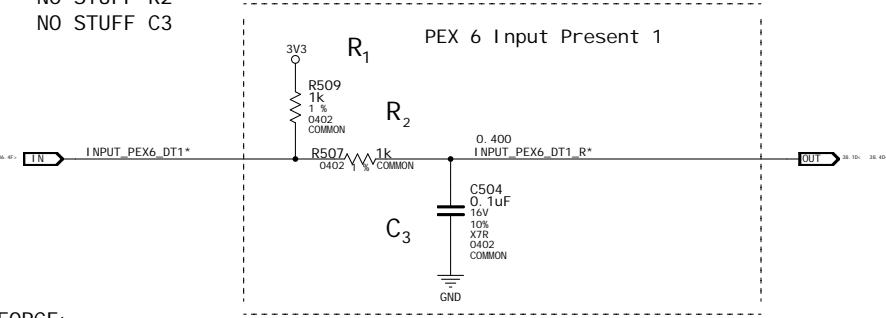
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PS1 mode



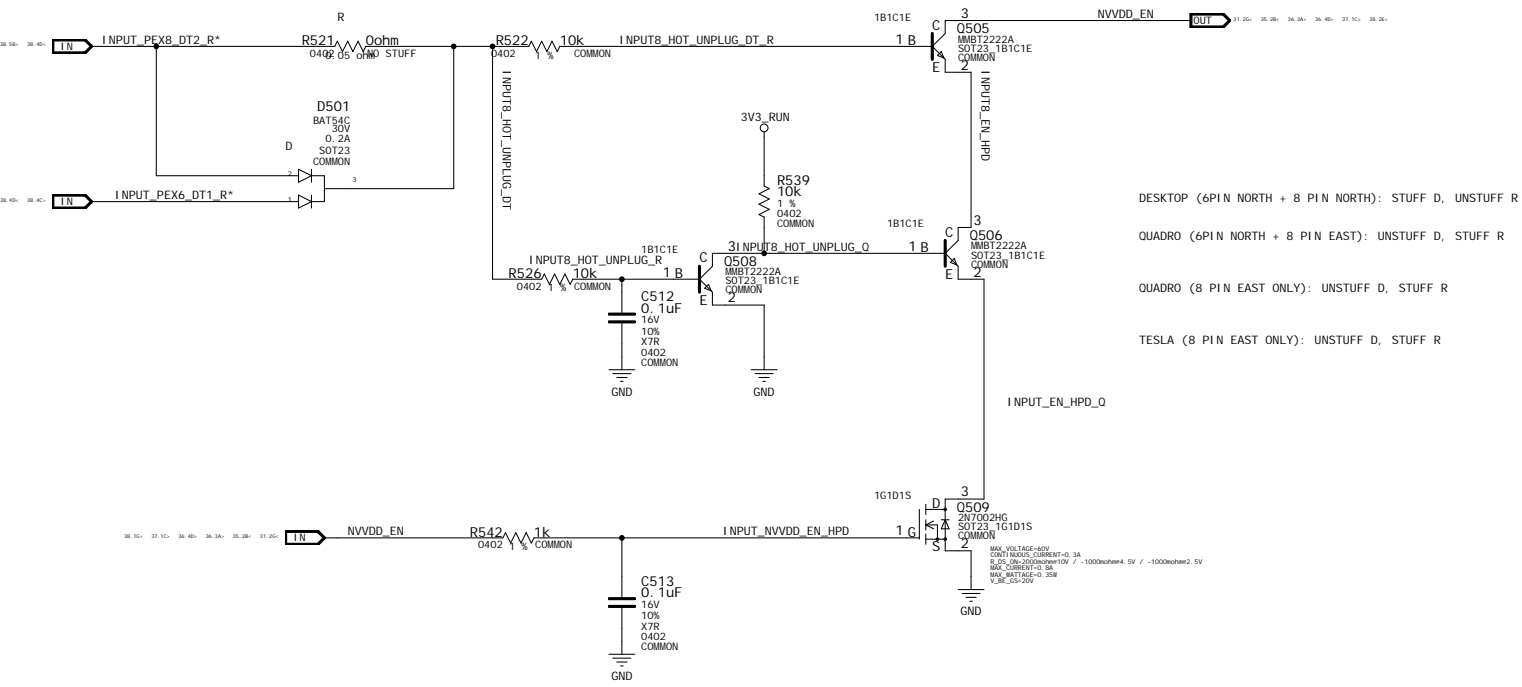
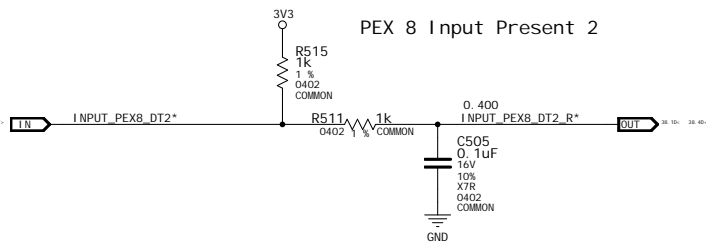
QUADRO/TESLA:

- PEX 6 INPUT CONNECTOR IS NOT LOADED
- PEX 6 INPUT DETECT MUST BE DISABLED
- PEX 8 INPUT DETECT MUST BE USED TO CONTROL STEERING
- STUFF Rnv IN STEERING CIRCUIT
- NO STUFF R1
- NO STUFF R2
- NO STUFF C3



GeFORCE:

- PEX 6 INPUT CONNECTOR IS LOADED
- PEX 6 INPUT DETECT MUST BE USED TO CONTROL STEERING
- NO STUFF Rnv IN STEERING CIRCUIT
- STUFF R1
- STUFF R2
- STUFF C3



DT SKU + WS SKU:

- FULL POWER WHEN BOTH 6PIN+8PIN ARE PRESENT
- STUFF Q508 AND Q509

TESLA SKU:

- FULL POWER WHEN 6PIN+8PIN OR 8PIN ONLY ARE PRESENT
- STUFF Q508 ONLY

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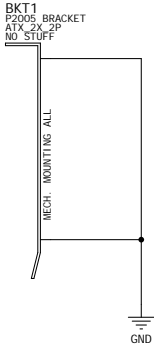


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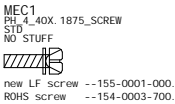
ASSEMBLY	PG600-B02 SKU0030 GB3B-384 CM200 6GB GDDR5 128MX32 DP+DP+HDMI +DP+DV1-I		
PAGE DETAIL	PS: 12V Current Steering & Hot Unplug Detect		
NV_PN	600-1G600-0030-QS1	PAGE	38 OF 41
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BOM REV	A		

Brackets:

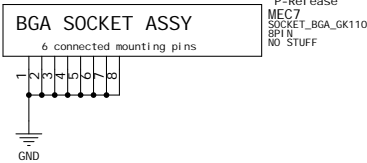
DVI DVI _HDMI _DP : 151-10001-0441-092



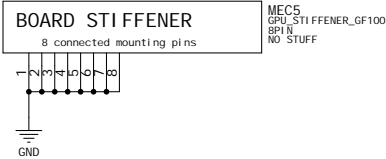
Bracket Screw



GPU SOCKET



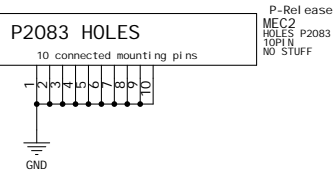
GPU Sti ffener (BRI NG-UP COOLER)



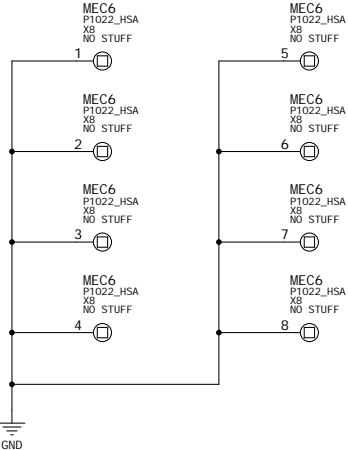
Sti ffener

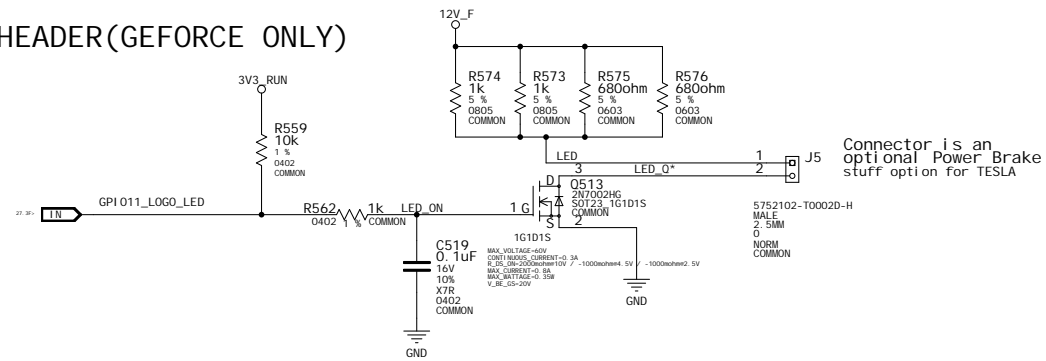


Mechani cal Hol es Symbol



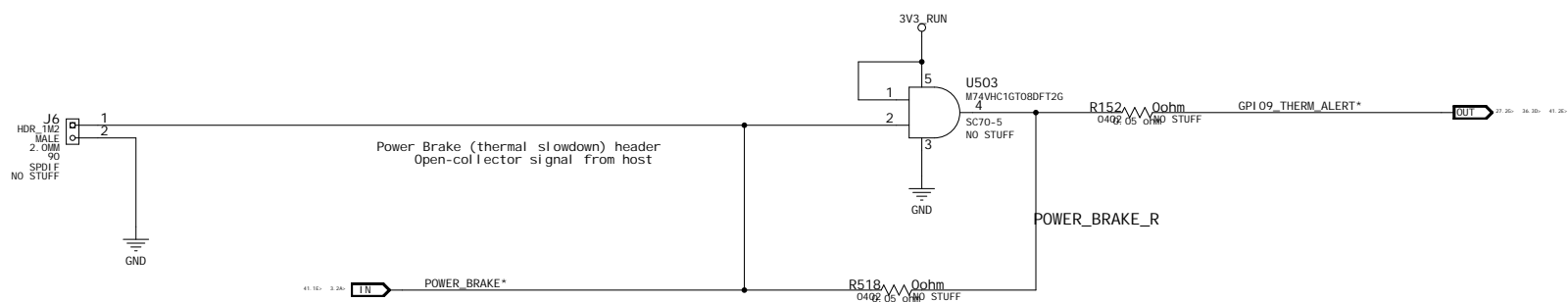
Bri ng Up Cooler



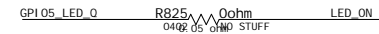


Connector is an optional Power Brake stuff option for TESLA

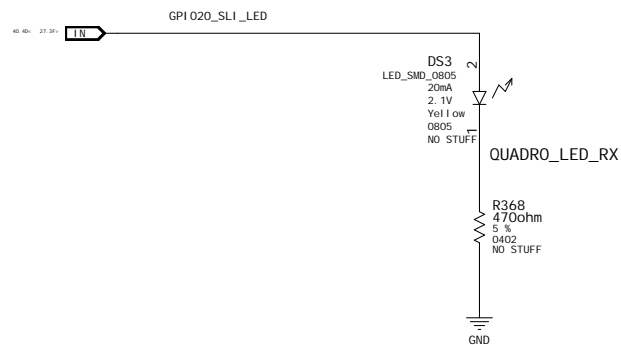
Bypass filter option



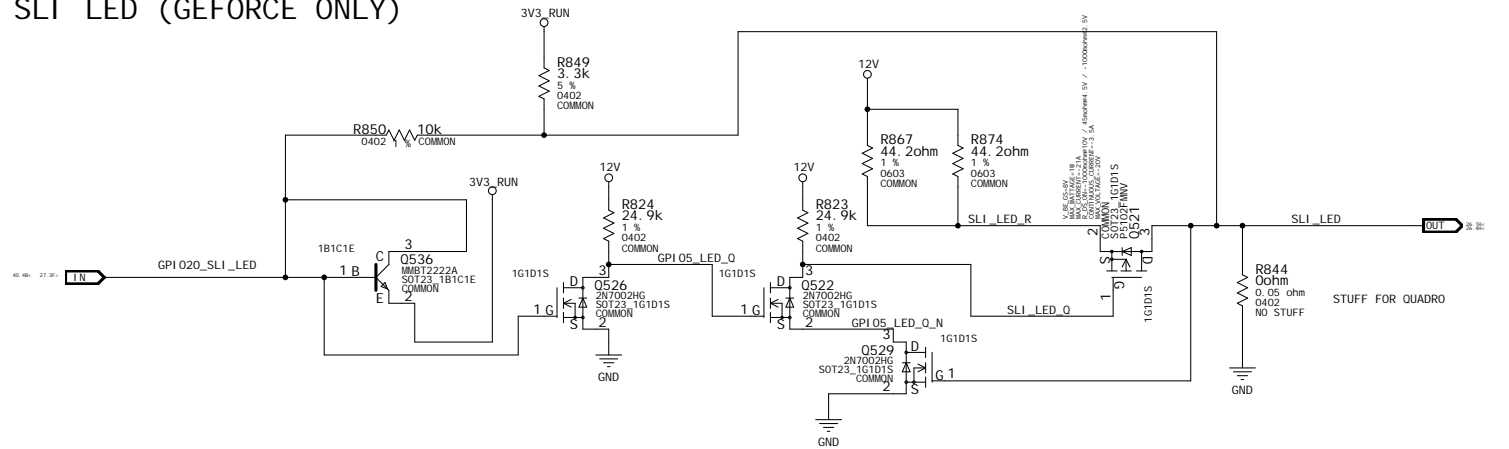
USING GPIO5 TO DIM GEFORCE AND SLI LED



LED FOR QUADRO
PLACE BETWEEN DP Connectors
CONNECTORS



SLI LED (GEFORCE ONLY)



NVI DI A CORPORATI ON

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV_PN	600-1G600-0030-QS1
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