MS8853_CPQ

GF3-Ti 500, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X

PCI DEVICE ID 0X0=0X200 FOR NV20.

Title	Section	Page
Cover Sheet	0	1
Bus I/O	1.1	2
NV20 Host	2.1	3
NV20 DAC/TV/TMDS	2.2	4
NV20 Decoupling	2.3	5
NV20 Host Strapping	2.4	6
DAC Connector	3.1	7
NV20 FBA/B/C/D	4.1	8
4MX16 DDR Decoupling	4.2	9
FB 4MX16 DDR	4.3 & 4.4	10, 11
ROM & VIDEO IF	5.1	12
DVI Controllor	6.1	13
DVI Connector	6.2	14
TV-Out	7.1	15
NV20 Power	8.1	16

NVVDD SET TO: 1.67V
FBVDD SET TO: 3.63V
FBVDDQ SET TO: 2.59V

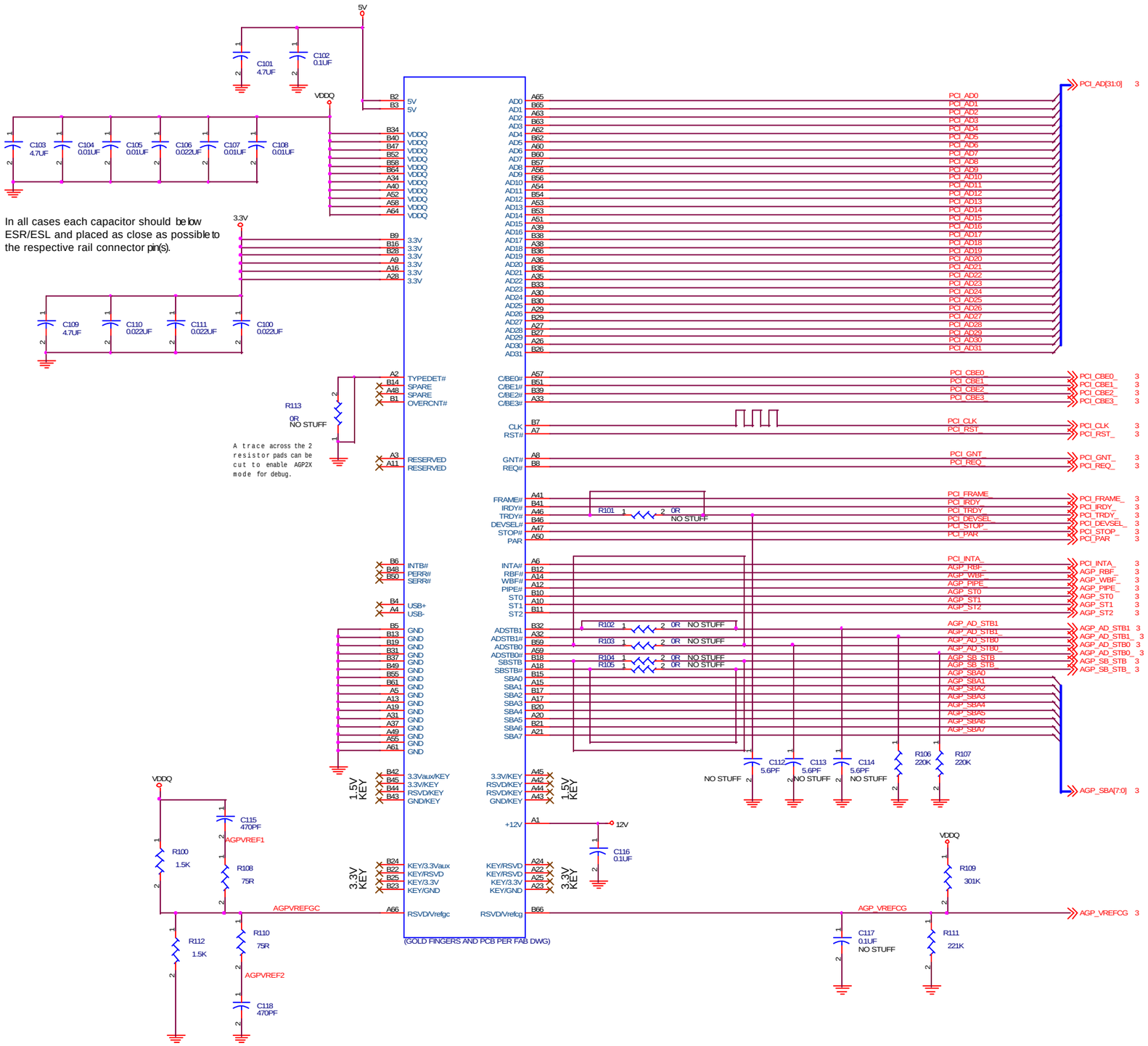
0 Cover Sheet

Micro-Star International Co., LTD.

MS-8853

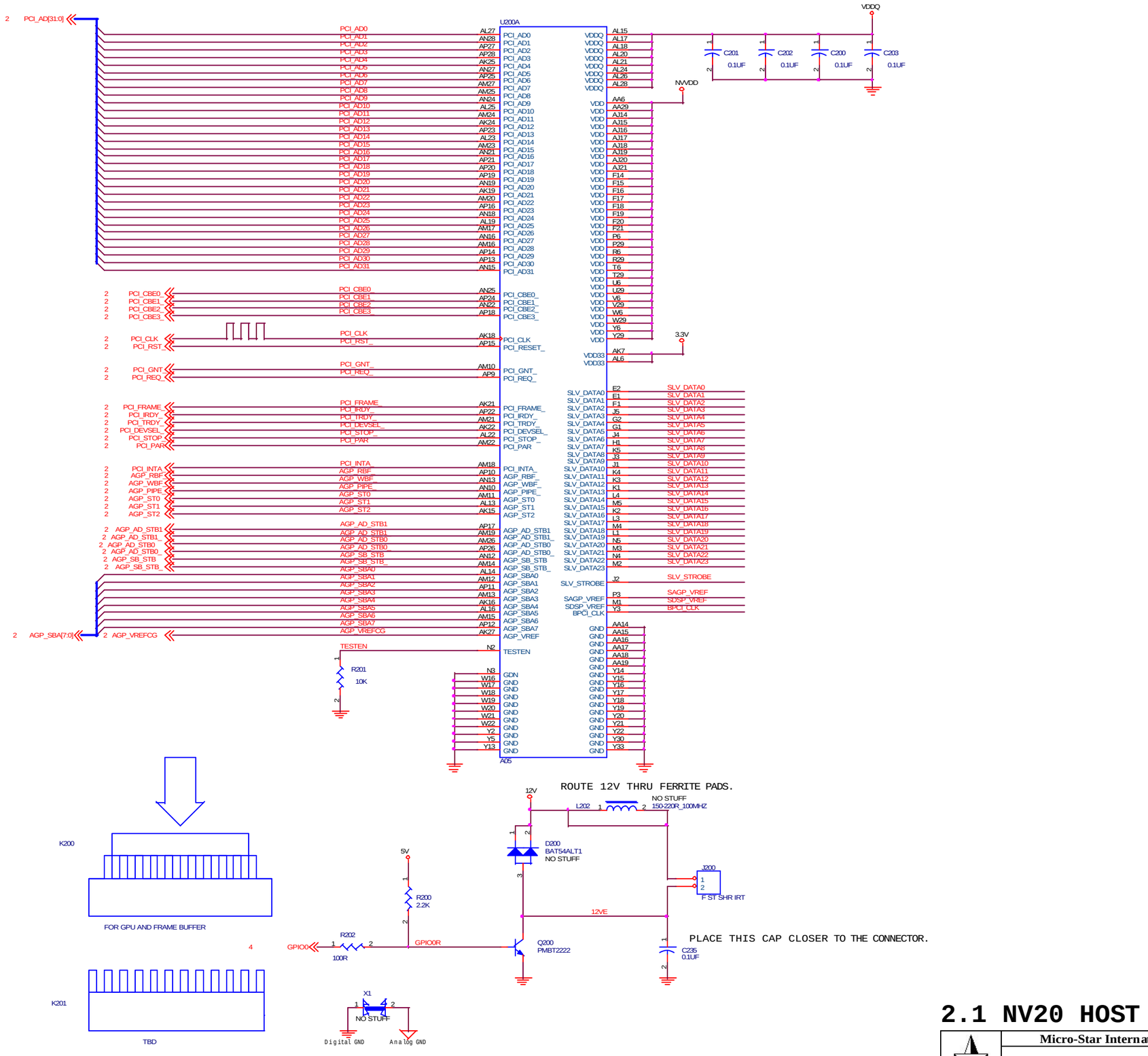
Size: C | Document Number: Cover Sheet | Rev: 0A

Date: Thursday, October 11, 2001 | Sheet 1 of 16



1.1 Bus I/O

Micro-Star International Co., LTD.	
MS-8853	
Size: C	Document Number: Bus I/O
Rev: 0A	
Date: Thursday, October 11, 2001	Sheet 2 of 16



2.1 NV20 HOST

Micro-Star International Co., LTD.		
MS-8853		
Size: C	Document Number: NV20 Host	Rev: 0A
Date: Thursday, October 11, 2001	Sheet 3 of 16	

6,12,13,15 CCIR_DATA[11:0]
6,12 VIP_VID[7:0]

PLL_VDD_SW
An option to bypass power sequencing circuit.
R259 0R
R261 0R NO STUFF
DAC_VDD_DLY
Q201 BSS138
C301 4.7UF NO STUFF
16 PWRGD_FBVDD
C300 4.7UF NO STUFF
PLL_DAC_SRC
L201 150-220R_100MHZ
L200 150-220R_100MHZ
C206 0.022UF
C207 150PF
C240 4.7UF
C208 0.022UF
C209 150PF
C241 4.7UF
C205 0.01UF
C210 0.33UF
R207 118R
5V
R203 2.2K
R204 2.2K
R205 33R
R206 33R
C204 0.1UF

SDA → SDA 12,14,15
SCL → SCL 12,14,15

U200B

7 I2C_SCL1	I2C_SCL0	AH4	I2C_SCL0
7 I2C_SDA1	I2C_SDA0	AH3	I2C_SDA0
	I2C_SCL1	AG5	I2C_SCL1
	I2C_SDA1	AH2	I2C_SDA1
12 VIP_HCLK	VIP_HCLK	Y1	VIP_HCLK
12 VIP_HCTL	VIP_HCTL	W2	VIP_HCTL
12 VIP_HAD0	VIP_HAD0	V3	VIP_HAD0
12 VIP_HAD1	VIP_HAD1	V2	VIP_HAD1
VIP_HAD2	VIP_HAD2	V1	VIP_HAD2
6 VIP_HAD3	VIP_HAD3	W1	VIP_HAD3
VIP_HAD4	VIP_HAD4	W5	VIP_HAD4
VIP_HAD5	VIP_HAD5	W4	VIP_HAD5
12 VIP_HAD6	VIP_HAD6	AB5	VIP_HAD6
12 VIP_HAD7	VIP_HAD7	W3	VIP_HAD7
		AH1	FT_CLAMP
	PLL_VDD	AN9	PLL_VDD
	DAC_VDD	AN7	DAC_VDD
	DAC_COMP	AL11	DAC_COMP
	DAC_VREF	AL12	DAC_VREF
	DAC_RSET	AL10	DAC_RSET
		AK13	DAC_GND
15 BUFFRST_	BUFFRST_	R5	BUFFRST_
12 ROM_CS_	ROM_CS_	P4	ROM_CS_
13 FP_PEN		AG4	FP_DE
13 FP_DATA_LO[11:0]	FP_DATA_LO0	AD4	FP_DATA_LO0
	FP_DATA_LO1	AE1	FP_DATA_LO1
	FP_DATA_LO2	AE2	FP_DATA_LO2
	FP_DATA_LO3	AE3	FP_DATA_LO3
	FP_DATA_LO4	AE4	FP_DATA_LO4
	FP_DATA_LO5	AF1	FP_DATA_LO5
	FP_DATA_LO6	AE5	FP_DATA_LO6
	FP_DATA_LO7	AF3	FP_DATA_LO7
	FP_DATA_LO8	AF4	FP_DATA_LO8
	FP_DATA_LO9	AG1	FP_DATA_LO9
	FP_DATA_LO10	AG2	FP_DATA_LO10
	FP_DATA_LO11	AG3	FP_DATA_LO11
		AN5	IFP0_VDD
		AK6	IFP0_VREF
		AL4	IFP0_RSET
		AM5	IFP0_GND
		AM6	IFP1_VDD
		AP7	IFP1_VREF
		AP6	IFP1_RSET
		AN6	IFP1_GND
		AM1	XTAL_IN
		AL2	XTAL_OUT

A05

	VIP_PCLK	N1	VIP_PCLK → VIP_PCLK 12
	VIP_VID0	P1	VIP_VID0
	VIP_VID1	R4	VIP_VID1
	VIP_VID2	V5	VIP_VID2 → VIP_VID[15:0] 6,12
	VIP_VID3	T5	VIP_VID3
	VIP_VID4	R1	VIP_VID4
	VIP_VID5	R2	VIP_VID5
	VIP_VID6	R3	VIP_VID6
	VIP_VID7	T4	VIP_VID7
	VIP_VID8	T1	VIP_VID8
	VIP_VID9	T2	VIP_VID9
	VIP_VID10	T3	VIP_VID10
	VIP_VID11	U4	VIP_VID11
	VIP_VID12	AD5	VIP_VID12
	VIP_VID13	U1	VIP_VID13
	VIP_VID14	U3	VIP_VID14
	VIP_VID15	V4	VIP_VID15
GPIO0	GPIO0	AJ1	GPIO0 → GPIO0 3
GPIO1	GPIO1	AJ3	GPIO1 → GPIO1 14
HSYNC	DAC_HSYNC	AL1	DAC_HSYNC → DAC_HSYNC 7
VSYNC	DAC_VSYNC	AK2	DAC_VSYNC → DAC_VSYNC 7
DAC_RED	DAC_RED	AP8	DAC_RED → DAC_RED 7
DAC_GREEN	DAC_GREEN	AK12	DAC_GREEN → DAC_GREEN 7
DAC_BLUE	DAC_BLUE	AM9	DAC_BLUE → DAC_BLUE 7
CCIR_HSYNC	CCIR_HSYNC	AA2	CCIR_HSYNC → CCIR_HSYNC 13,15
CCIR_VSYNC	CCIR_VSYNC	AA5	CCIR_VSYNC → CCIR_VSYNC 13,15
CCIR_CLK_IN	CCIR_CLK_IN	AA1	CCIR_CLK_IN → CCIR_CLK_IN 13,15
CCIR_CLK_OUT	CCIR_CLK_OUT	Y4	CCIR_CLK_OUT → R211 0R → R_CCIR_CLK_OUT 13,15
CCIR_DATA0	CCIR_DATA0	AA3	
CCIR_DATA1	CCIR_DATA1	AA4	
CCIR_DATA2	CCIR_DATA2	AB1	
CCIR_DATA3	CCIR_DATA3	AB2	
CCIR_DATA4	CCIR_DATA4	AB3	
CCIR_DATA5	CCIR_DATA5	AB4	
CCIR_DATA6	CCIR_DATA6	AC1	
CCIR_DATA7	CCIR_DATA7	AC3	
CCIR_DATA8	CCIR_DATA8	AC4	
CCIR_DATA9	CCIR_DATA9	AD1	
CCIR_DATA10	CCIR_DATA10	AD2	
CCIR_DATA11	CCIR_DATA11	AD3	

CCIR_DATA[11:0] 6,12,13,15 → R246 470R

	IFP_TXD0	AM4	
	IFP_TXD0_	AN4	
	IFP_TXD1	AP3	
	IFP_TXD1_	AN3	
	IFP_TXD2	AL3	
	IFP_TXD2_	AM3	
	IFP_TXD3	AP2	
	IFP_TXD3_	AN2	
	IFP_TXD4	AL9	
	IFP_TXD4_	AM8	
	IFP_TXD5	AK9	
	IFP_TXD5_	AK10	
	IFP_TXD6	AM7	
	IFP_TXD6_	AL8	
	IFP_TXD7	AL7	
	IFP_TXD7_	AK8	
	IFP_TXC0	AN1	
	IFP_TXC0_	AP1	
	IFP_TXC1	AP4	
	IFP_TXC1_	AP5	

R208 75R
R209 75R
R210 75R

This part also serves as curent return path for PLL_VDD and DAC_VDD.

X10
Digital GND
Analog GND

USE THIS AREA FOR "SINGLE POINT" CONNECTION.

3.3V

100_100_20 14.31818MHZ Y200
DAC_XTAL_IN — DAC_XTAL_OUT
C211 10PF
C212 10PF

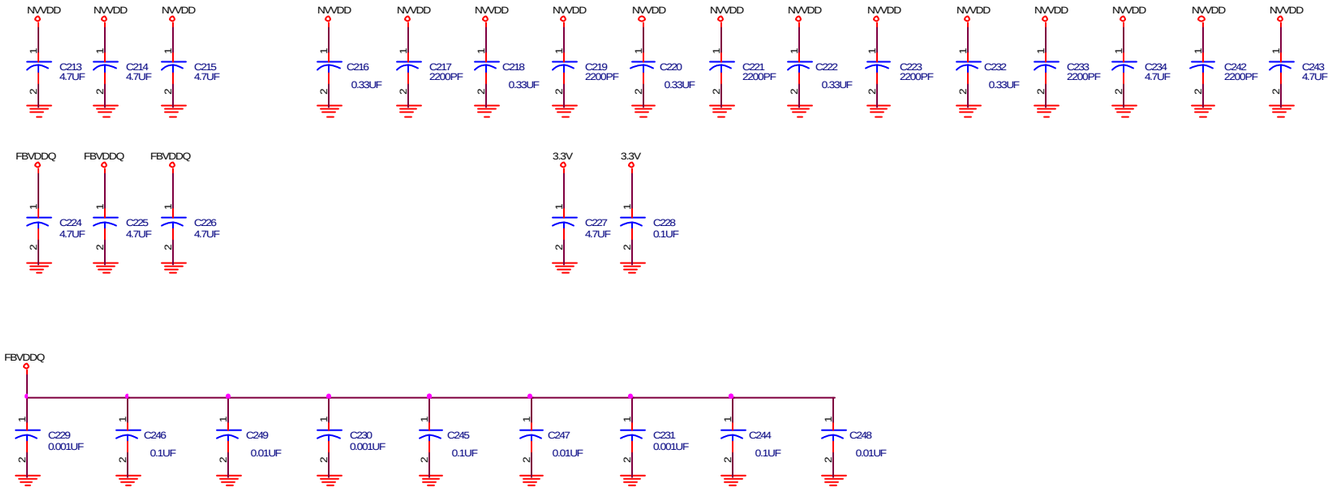
Use thick (non-impedance controlled) traces on XTALIN/OUT

2.2 NV20 DAC/TV/TMDS

Micro-Star International Co., LTD.

MS-8853

Size	Document Number	Rev
C	NV20 DAC/TV/TMDS	0A
Date: Thursday, October 11, 2001	Sheet 4 of 16	



2.3 NV20 DECOUPLING

Micro-Star International Co., LTD.		
MS-8853		
Size: C	Document Number: NV20 Decoupling	Rev: 0A
Date: Thursday, October 11, 2001	Sheet 5 of 16	

4,12,13,15 CCIR_DATA[11:0]
4,12 VIP_VID[15:0]
4,13 FP_DATA_LO[11:0]

4,12 VIP_HAD0
4,12 VIP_HAD1
4 VIP_HAD2
4 VIP_HAD3
4 VIP_HAD4
4 VIP_HAD5
4,12 VIP_HAD6
4,12 VIP_HAD7

3.3V

CCIR_DATA0 R212 1 2 10K
[0] STRAP_AD_SWAP
STRAP_AD_SWAP=0 : PCIAD bus [31:0] swapped
STRAP_AD_SWAP=1 : PCIAD bus [31:0] normal

CCIR_DATA5 R213 1 2 10K
[1] STRAP_SUB_VENDOR
STRAP_SUB_VENDOR=0 : System BIOS
STRAP_SUB_VENDOR=1 : Adaptor BIOS

R214 1 2 10K VIP_VID9 R215 1 2 10K
NO STUFF
[11] STRAP_FAST_WRITES
STRAP_FAST_WRITES=0 : FAST WRITE ENABLED
STRAP_FAST_WRITES=1 : FAST WRITE DISABLED

R216 1 2 10K VIP_VID11 R217 1 2 10K
NO STUFF
VID[11:10] PCI_DEV_ID
PCI_DEV_ID = 0x202 (Default)

R218 1 2 10K VIP_VID10 R219 1 2 10K
NO STUFF

R220 1 2 10K VIP_VID6 R221 1 2 10K
NO STUFF
[VID6:CCIR11] STRAP_TVMODE
STRAP_TVMODE=0 : PAL
STRAP_TVMODE=1 : NTSC
STRAP_TVMODE=2 : Reserved
STRAP_TVMODE=3 : Disabled

R222 1 2 10K CCIR_DATA11 R223 1 2 10K
NO STUFF

R224 1 2 10K CCIR_DATA10 R225 1 2 10K
NO STUFF
[CCIR10] STRAP_CRYSTAL
STRAP_CRYSTAL=0 : 13.50000MHz
STRAP_CRYSTAL=1 : 14.31818MHz

R226 1 2 10K CCIR_DATA9 R227 1 2 10K
NO STUFF
[9:6] STRAP_RAM_TYPE

1000 2Mx32, DLL on, low drive (Micron and Hyundai 2Mx32, when eventually qualified)
1001 2Mx32, DLL on, high/no drive (Samsung 2Mx32, where bit 1 in EMRS needs to be low, when DLL is on)
1110 1Mx32 Infineon DD2, DLL on (reserved for future use if needed)
1011 1Mx32 Infineon DD1, dll-off with CAS=1 (these are the original Infineon parts we used)
1100 1Mx32 Infineon DD2, DLL-off, but with 0x100080 set to CAS+0,rather than the standard CAS+1 that we have used with DLL-off (this is for the latest Infineon parts)
1010 4Mx16 DDR

R228 1 2 10K CCIR_DATA8 R229 1 2 10K
NO STUFF

R230 1 2 10K CCIR_DATA7 R231 1 2 10K
NO STUFF

R232 1 2 10K CCIR_DATA6 R233 1 2 10K
NO STUFF

R234 1 2 10K VIP_VID7 R235 1 2 10K
NO STUFF
[VID7] STRAP_AGP4X
STRAP_AGP4X=0 : AGP4X transfers enabled
STRAP_AGP4X=1 : AGP2X only

R236 1 2 10K VIP_VID8 R237 1 2 10K
NO STUFF
[VID8] STRAP_AGPSBA
STRAP_AGPSBA=0 : sideband enabled
STRAP_AGPSBA=1 : pipelined only transfers
Set SideBand OFF in the first prototype built.12/21/2K

R238 1 2 10K VIP_VID13 R239 1 2 10K
NO STUFF
[VID13] FP_INTERFACE
0=24 bit FP
1=12 bit FP

VIP_VID12 R240 1 2 10K
[VID12] AGP MODE
STRAP_HOST=1 : AGP Mode

R241 1 2 10K VIP_HAD3 R242 1 2 10K
NO STUFF
Strap_user[0]
Video Module Sense bit = TBD.

R243 1 2 10K VIP_VID4
BRIDGE_EN

VIP_VID3 R244 1 2 10K
MULTI_AGP

VIP_VID5 R245 1 2 10K
MULTI_IO

R249 1 2 10K VIP_VID15 R247 1 2 10K
NO STUFF
VID[15:14] Strap_FB[1:0]:
00 = 64MB.

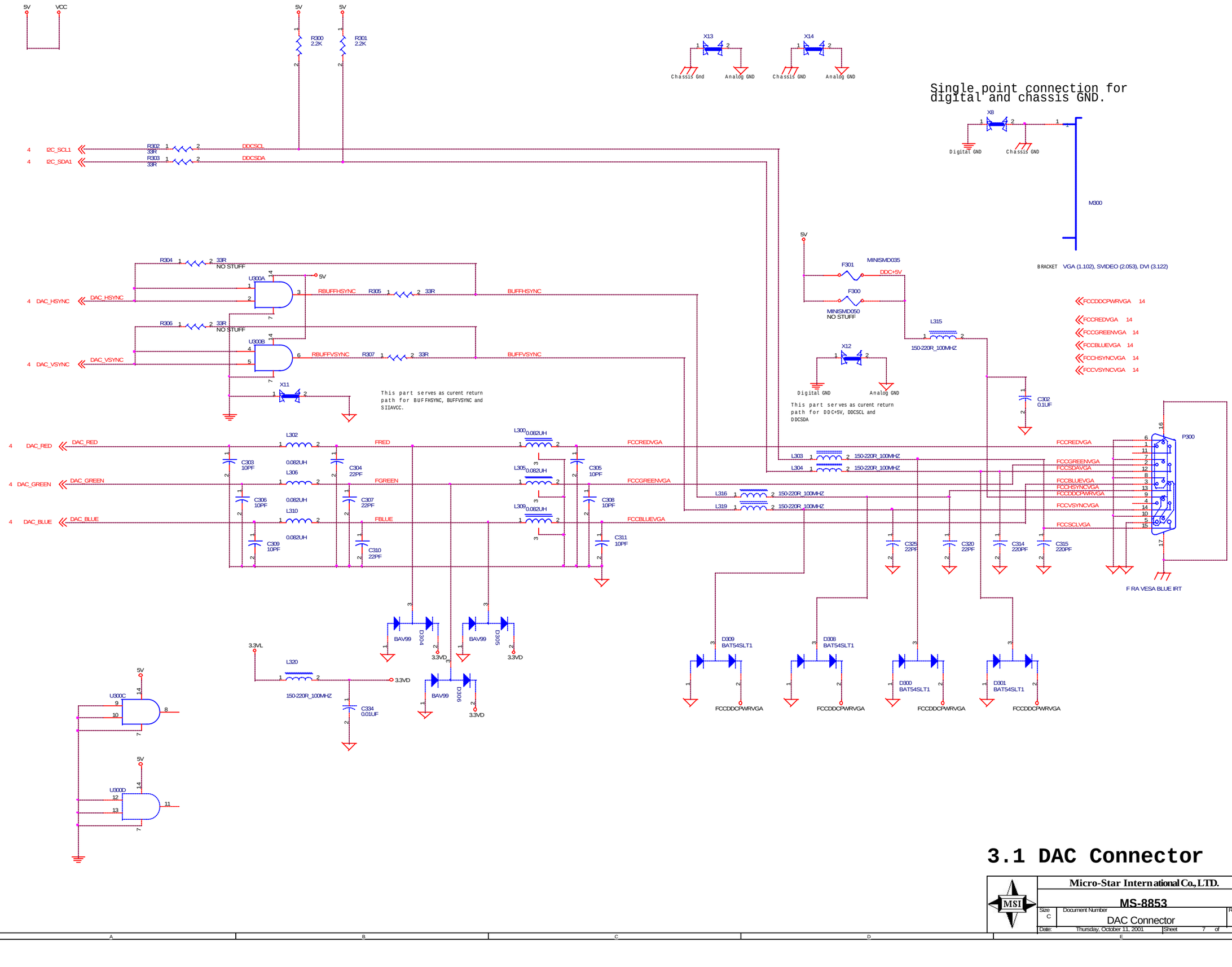
R250 1 2 10K VIP_VID14 R248 1 2 10K
NO STUFF

2.4 NV20 HOST STRAPS

Micro-Star International Co., LTD.

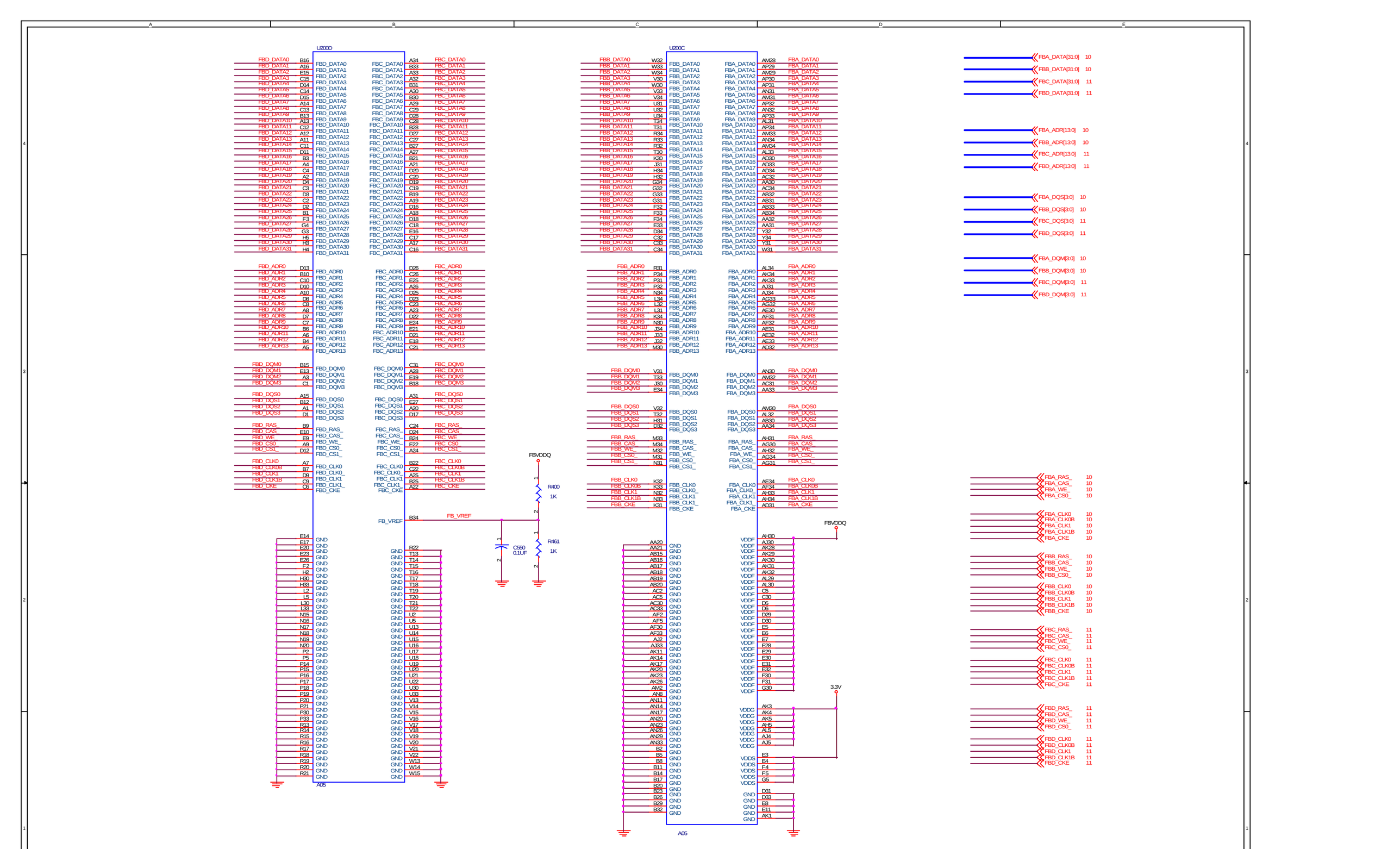
MS-8853

Size	Document Number	Rev
C	NV20 Host Strapping	0A
Date: Thursday, October 11, 2001	Sheet 6 of 16	



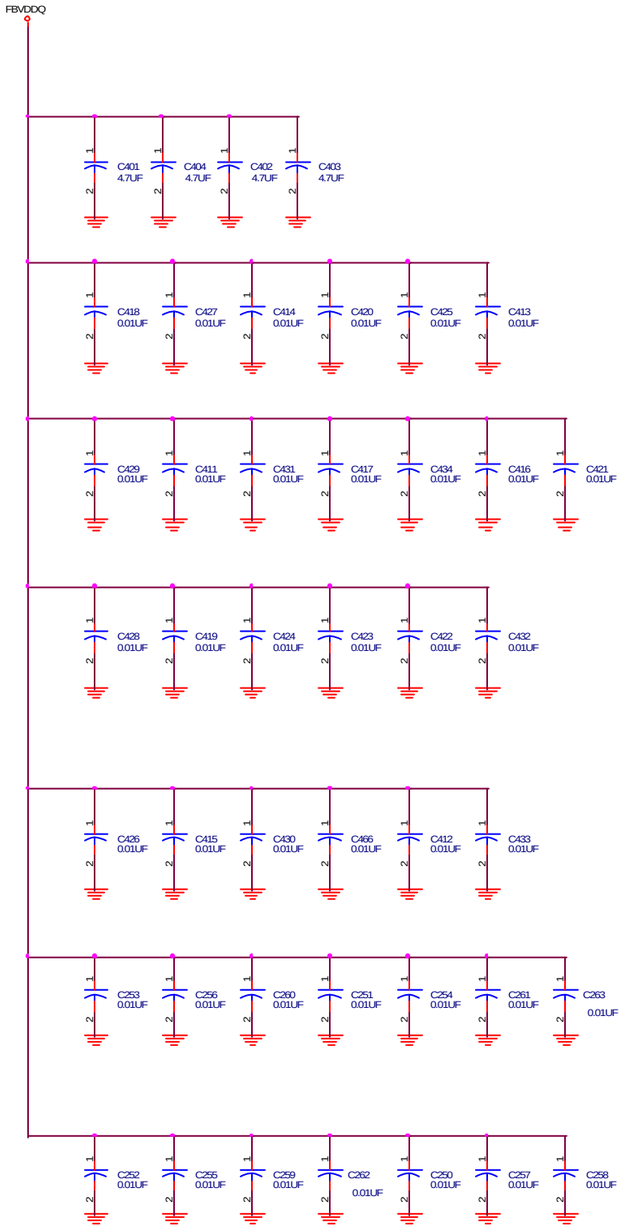
3.1 DAC Connector

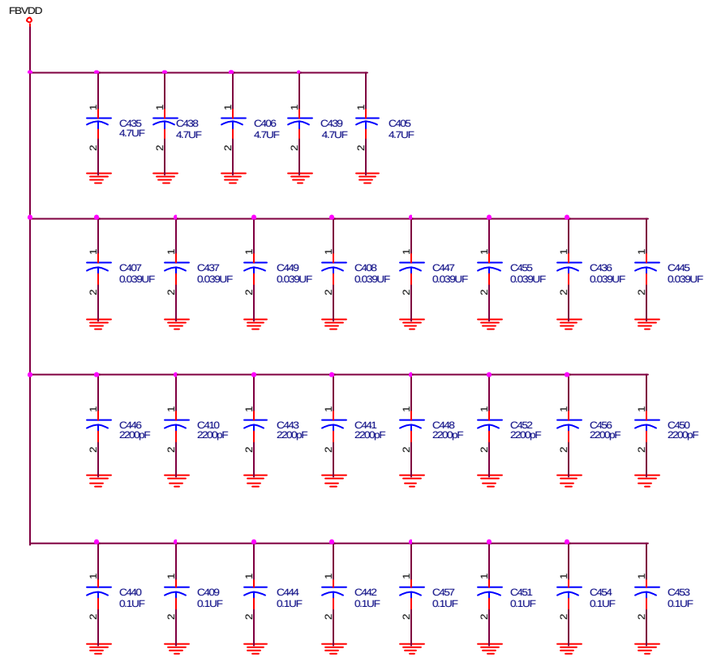
Micro-Star International Co., LTD.		
MS-8853		
Size: C	Document Number: DAC Connector	Rev: 0A
Date: Thursday, October 11, 2001	Sheet 7 of 16	



4.1 NV20 FBA/B/C/D

Micro-Star International Co., LTD.			
MS-8853			
Size: C	Document Number: NV20 FBA/B/C/D		Rev: 0A
Date: Thursday, October 11, 2001	Sheet 8 of 16		



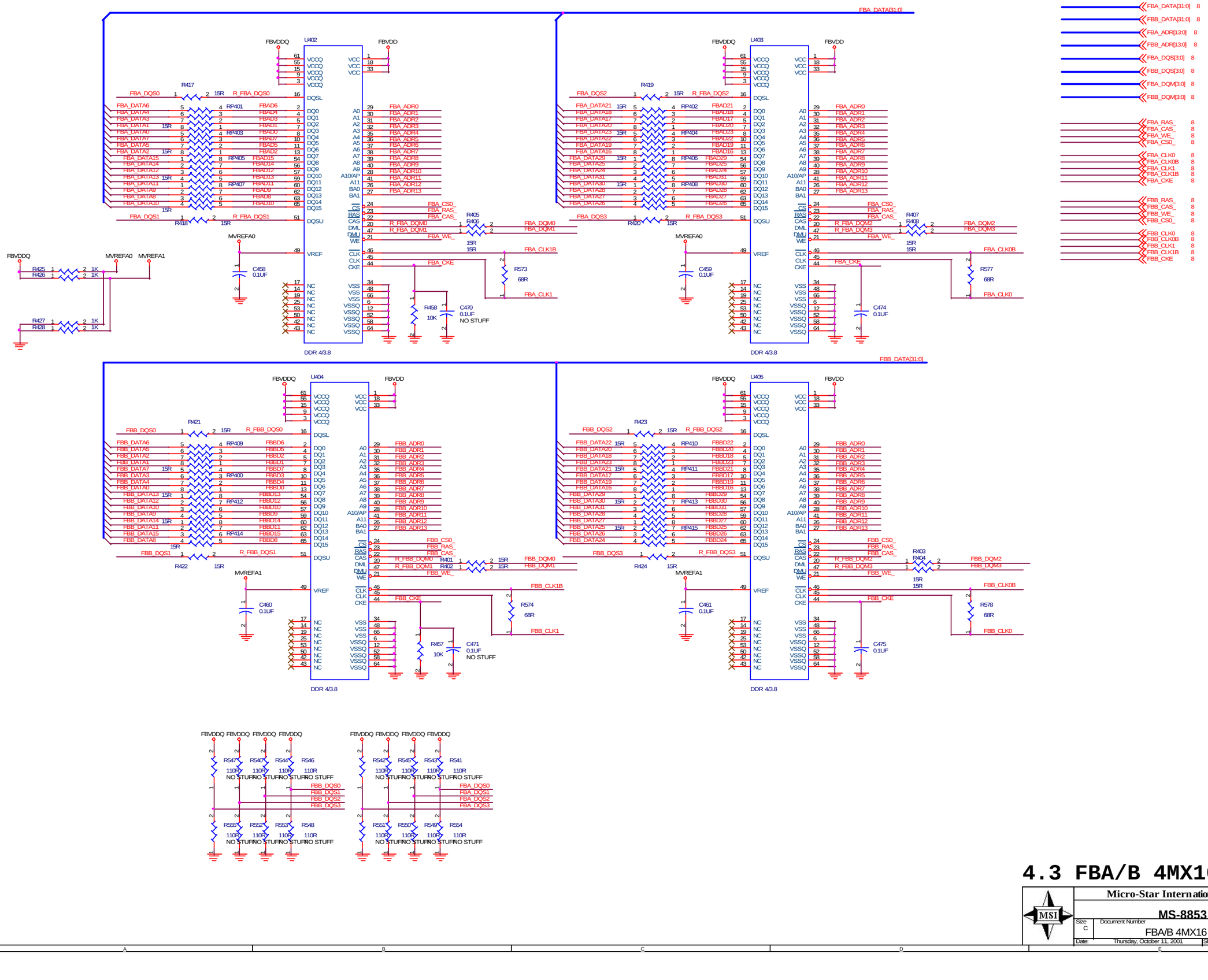


4.2 4MX16 DDR DECOUPLING

Micro-Star International Co., LTD.

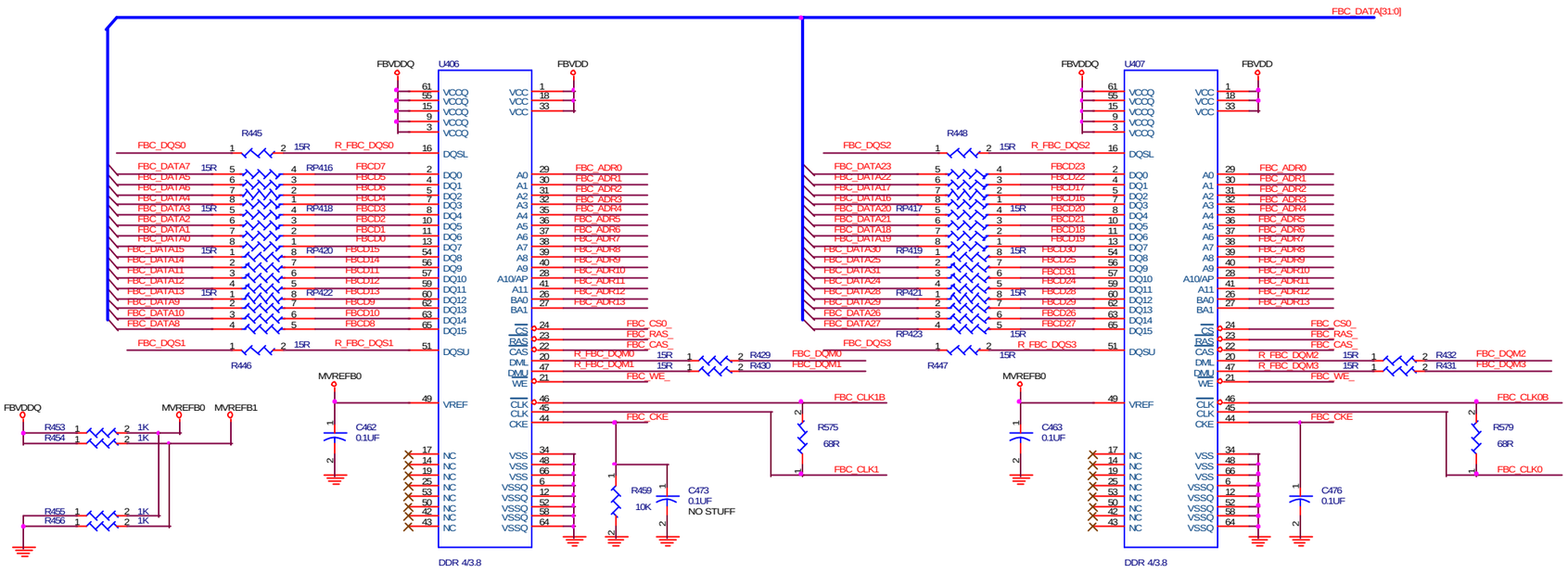
MS-8853

Size	Document Number	Rev
C	4MX16 DDR Decoupling	0A
Date: Thursday, October 11, 2001	Sheet 9 of 16	



4.3 FBA/B 4MX16 DDR

Micro-Star International Co., LTD.		
MS-8853		
Size: C	Document Number: FBA/B 4MX16 DDR	Rev: 0A
Date: Thursday, October 11, 2001	Sheet 10 of 16	



4.4 FBC/D 4MX16 DDR

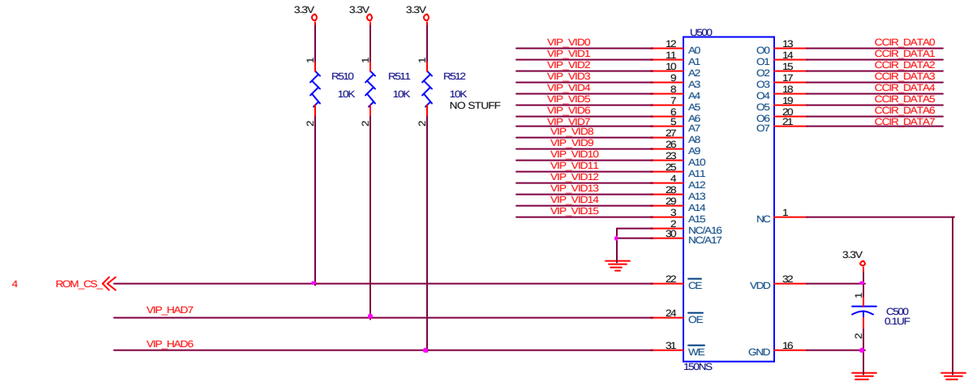
Micro-Star International Co., LTD.

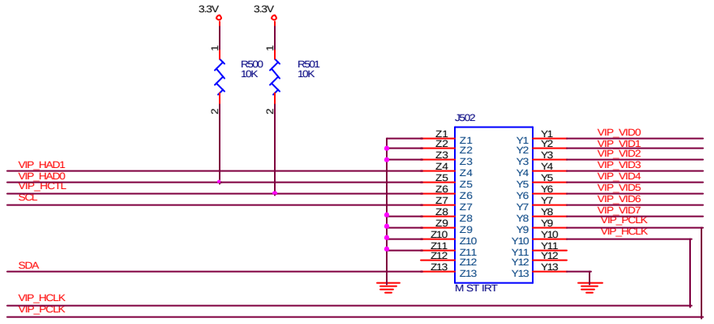
MS-8853

Size	Document Number	Rev
C	FBC/D 4MX16 DDR	0A

Date: Thursday, October 11, 2001 Sheet 11 of 16

4,6 VIP_VID[15:0]
4 VIP_PCLK
4 VIP_HCLK
4 VIP_HCTL
4 VIP_HAD0
4 VIP_HAD1
4 VIP_HAD2
4,6 VIP_HAD3
4 VIP_HAD4
4 VIP_HAD5
4 VIP_HAD6
4 VIP_HAD7
4,6,13,15 CCIR_DATA[11:0]
4,13,15 CCIR_HSYNC
4,13,15 CCIR_VSYNC
4,13,15 CCIR_CLK_IN
4,13,15 R_CCIR_CLK_OUT
4,15 BUFFRST_
4,14,15 SCL
4,14,15 SDA





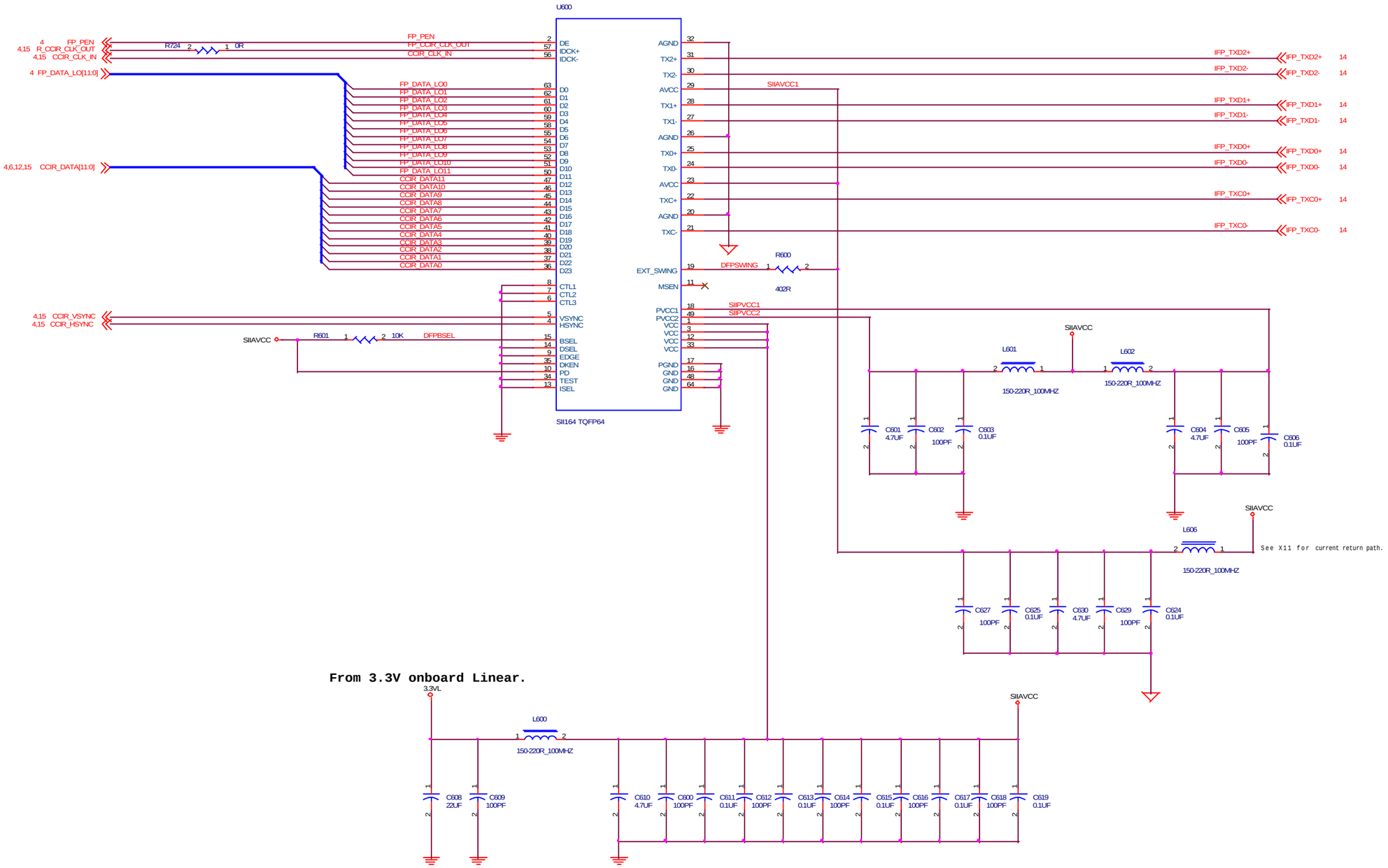
5.1 ROM & VIDEO IF

Micro-Star International Co., LTD.

MS-8853

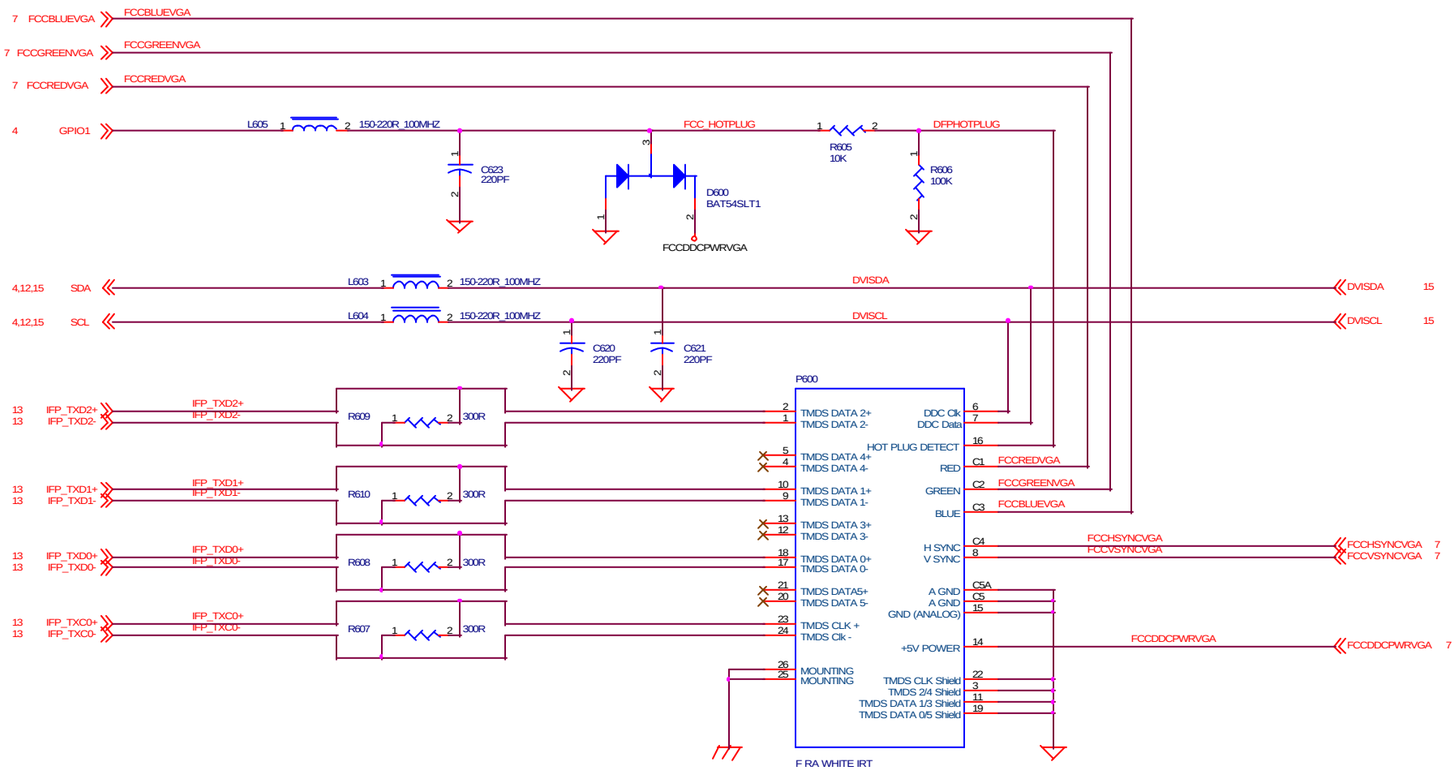
Size: C | Document Number: ROM & Video IF | Rev: 0A

Date: Thursday, October 11, 2001 | Sheet 12 of 16



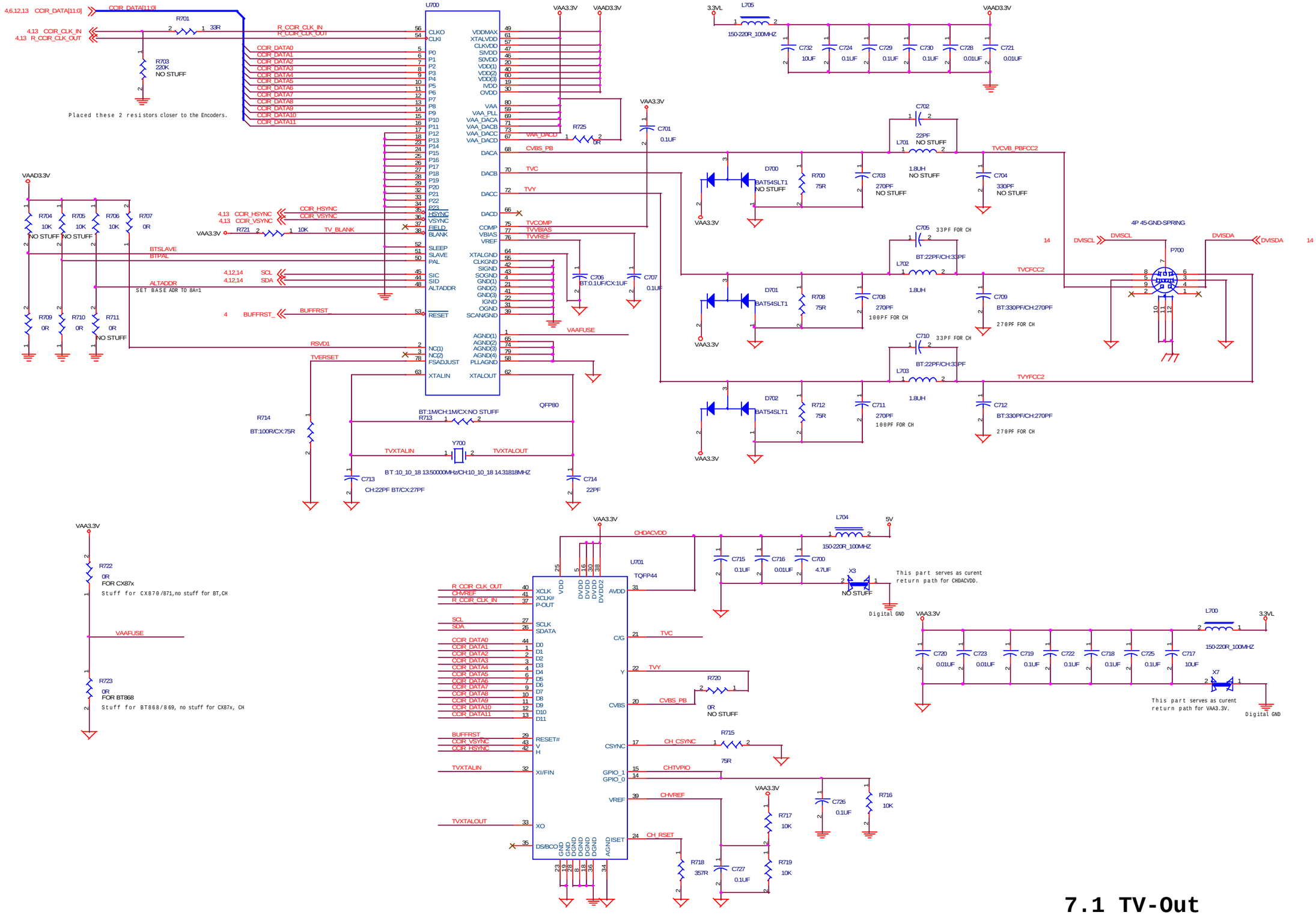
6.1 DVI Controllor

Micro-Star International Co., LTD.		
MS-8853		
Size: C	Document Number: DVI Controllor	Rev: 0A
Date: Thursday, October 11, 2001	Sheet 13 of 16	



6.1 DVI Connector

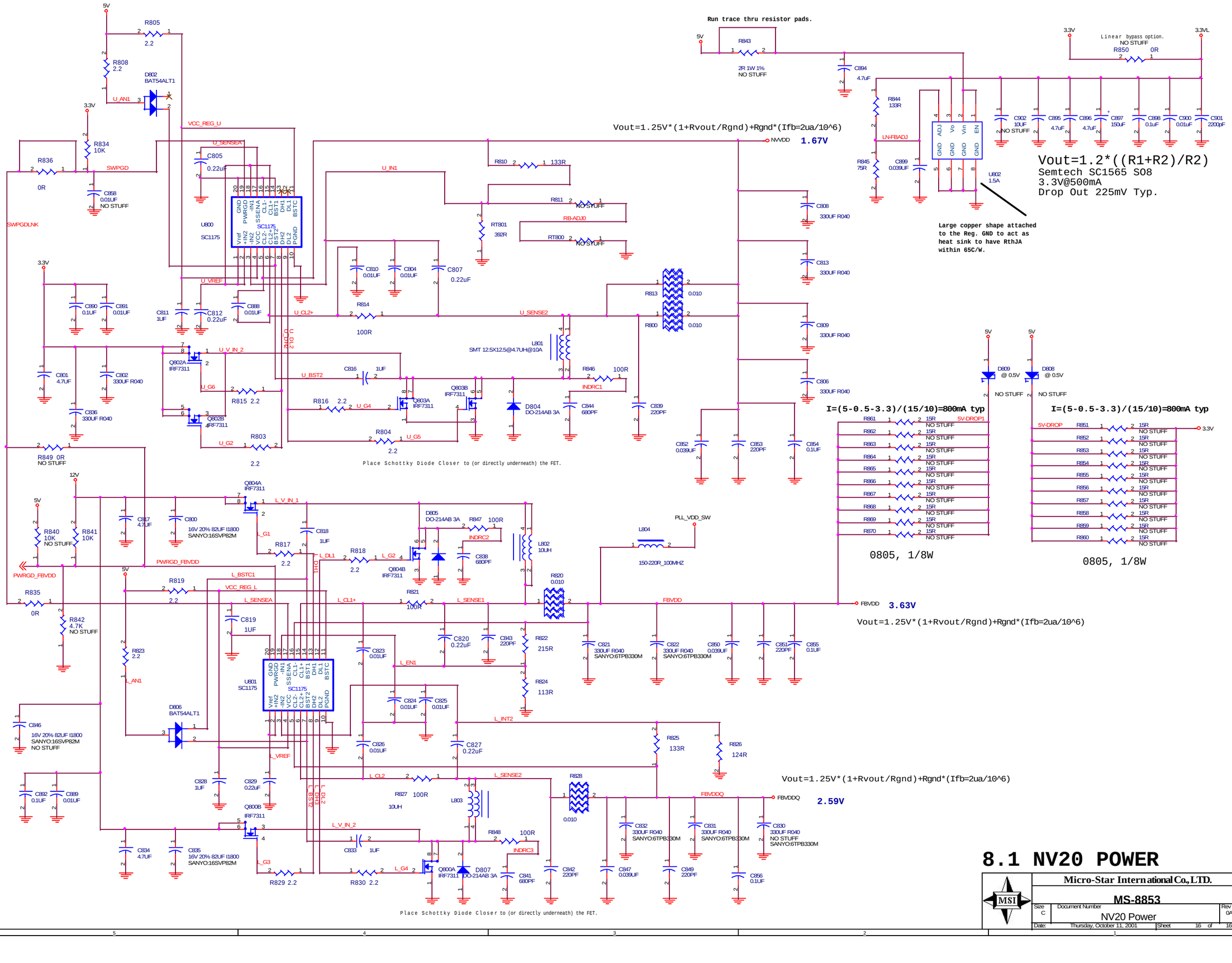
Micro-Star International Co., LTD.			
MS-8853			
Size: C	Document Number: DVI Connector		Rev: 0A
Date: Thursday, October 11, 2001		Sheet 14 of 16	



Parts for Chrontel CH7007/8

7.1 TV-Out

Micro-Star International Co., LTD.		
MS-8853		
Size: C	Document Number: TV-Out	Rev: 0A
Date: Thursday, October 11, 2001	Sheet 15 of 16	


Run trace thru resistor pads.
Vout=1.25V*(1+Rvout/Rgnd)+Rgnd*(Ifb=2ua/10^6)
NVDD 1.67V
Linear bypass option.
NO STUFF
Vout=1.2*((R1+R2)/R2)
Semtech SC1565 SO8
3.3V@500mA
Drop Out 225mV Typ.
Large copper shape attached to the Reg. GND to act as heat sink to have RthJA within 65C/W.
Place Schottky Diode Closer to (or directly underneath) the FET.
I=(5-0.5-3.3)/(15/10)=800mA typ
0805, 1/8W
FBVDD 3.63V
Vout=1.25V*(1+Rvout/Rgnd)+Rgnd*(Ifb=2ua/10^6)
FBVDDQ 2.59V
8.1 NV20 POWER
Micro-Star International Co., LTD.
MS-8853
NV20 Power
Rev 0A
Thursday, October 11, 2001
Sheet 16 of 16