P601 REV:1.2 : G96-GS/GE2-128, MXM-II, 512/256MB DDR2 (32/16Mx16)
LVDS, DP-A/B, DVI-A/B/C, TV_OUT, VGA, HD AUDIO, SPDIF
MXM 2.1a SPECIFICATION COMPLIANT

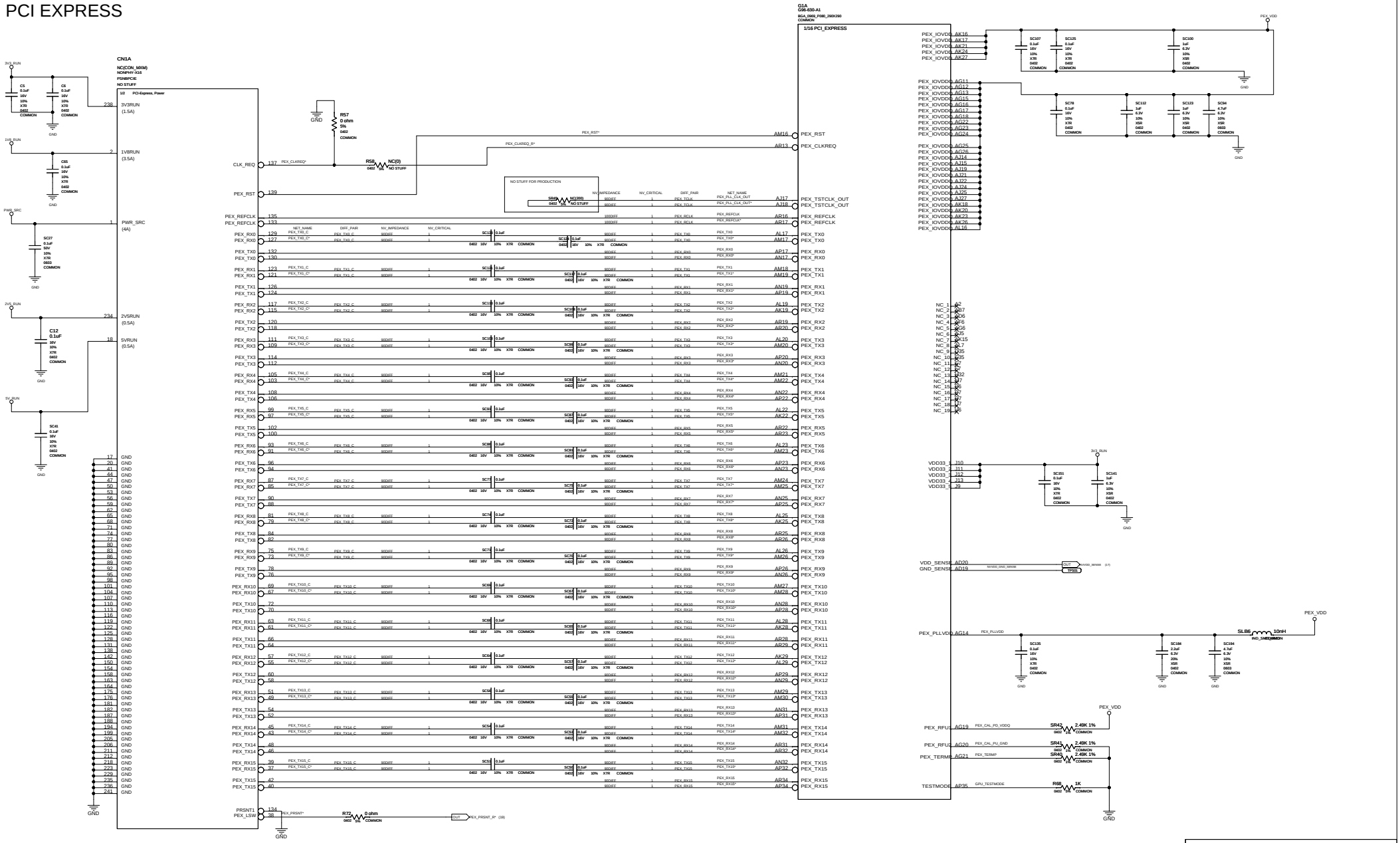
Table of Contents

REVISION HISTORY

Sch Rev	PCB Rev	DATE	REVISION DESCRIPTION
1.0	1.0	2008-04-16	Base NV P616-A03 design. Change GDDR3 to DDR2
1.0	1.0	2008-05-07	Model name change to P601 V1.0
1.1	1.1	2008-05-26	Add D3, D4, D7, SD2, SD4 ESD diodes for I2C bus.
1.2	1.2	2008-06-02	Modify PCB layout. Down impedance of NVVDD plane

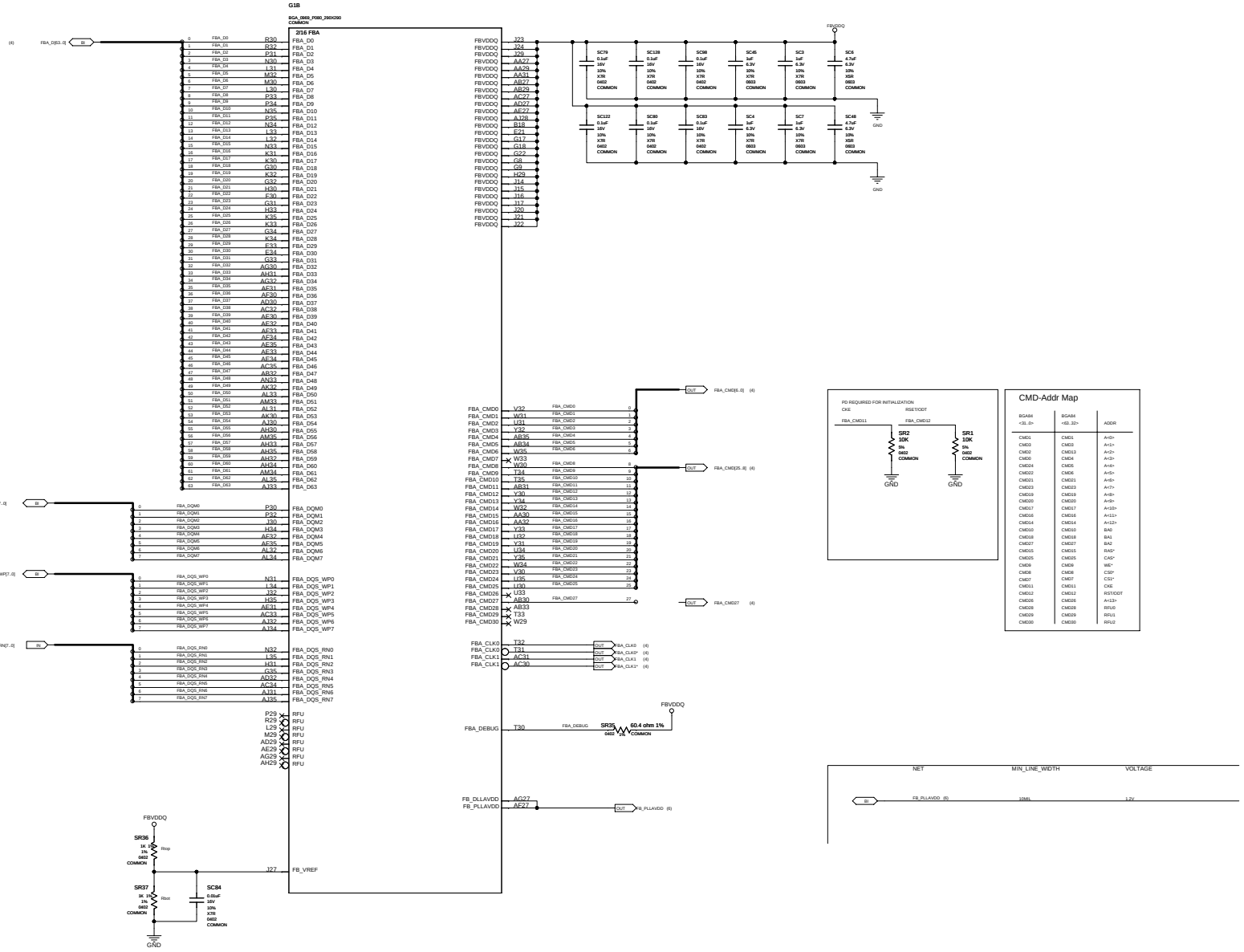
Title	<Title>	
Size B	Document Number <Doc>	Rev A
Date: Tuesday, June 03, 2008	Sheet 1 of 19	

PCI EXPRESS



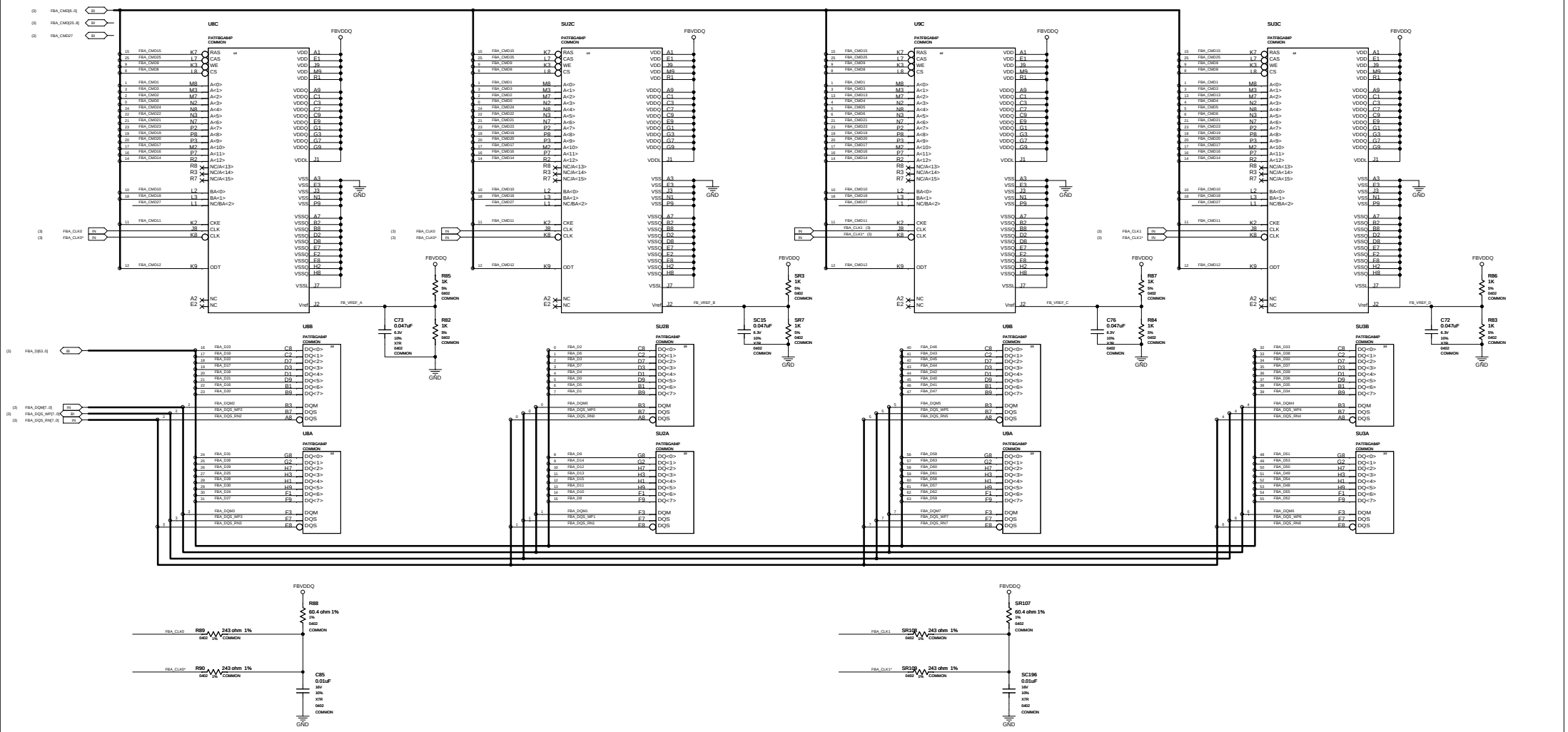
Title	<Title>
Size	Document Number: Custom<Doc>
Rev	A
Date:	Tuesday, June 03, 2008
Sheet	2 of 19

GPU MEMORY INTERFACE: PARTITION A



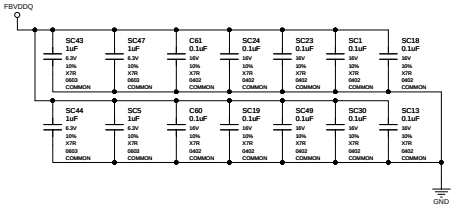
Title	<Title>
Size	Document Number: Custom<Doc>
Rev	A
Date:	Tuesday, June 03, 2008
Sheet	3 of 19

Partition A Memories

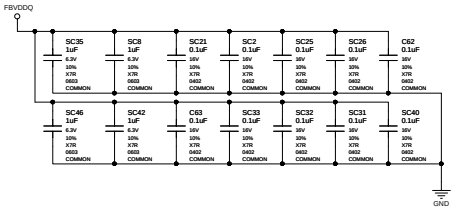


Title	<Title>	
Size: Custom	Document Number <Doc>	Rev: A
Date: Tuesday, June 03, 2008	Sheet 4 of 19	

FRAME BUFFER: PARTITION A DECOUPLING

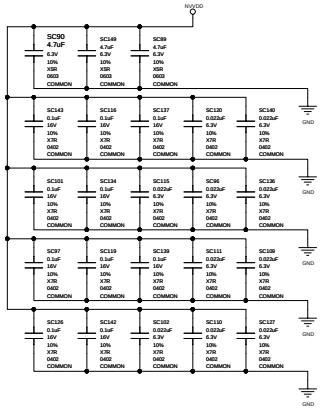


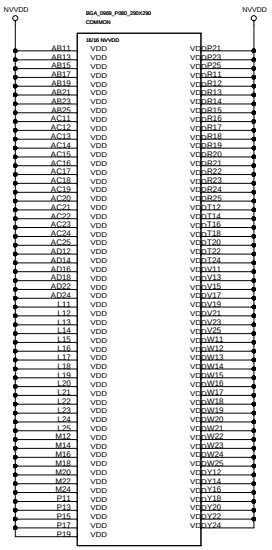
Decoupling for FBA North Side Memory Device.



Decoupling for FBA South Side Memory Device.

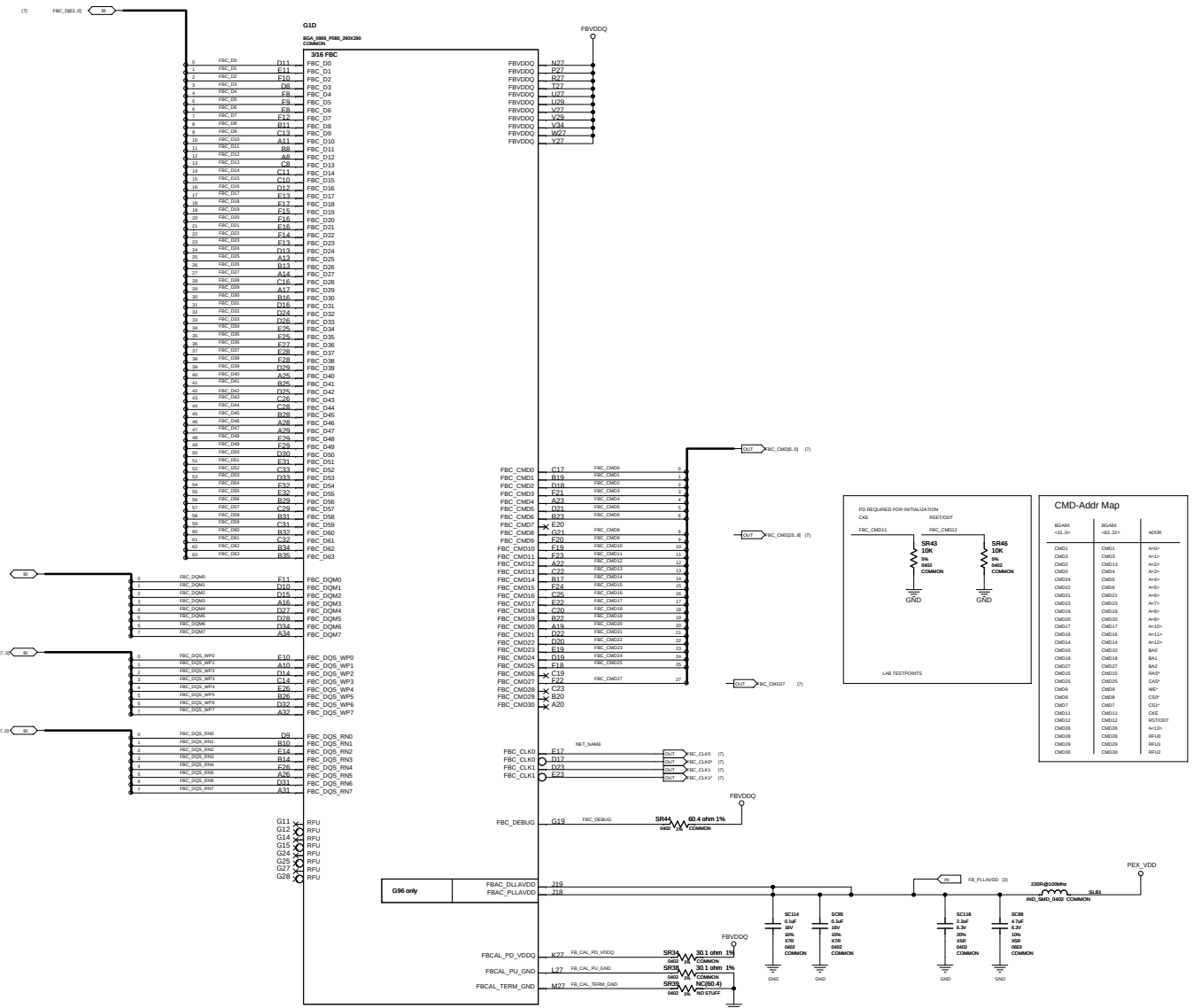
NVVDD POWER AND DECOUPLING



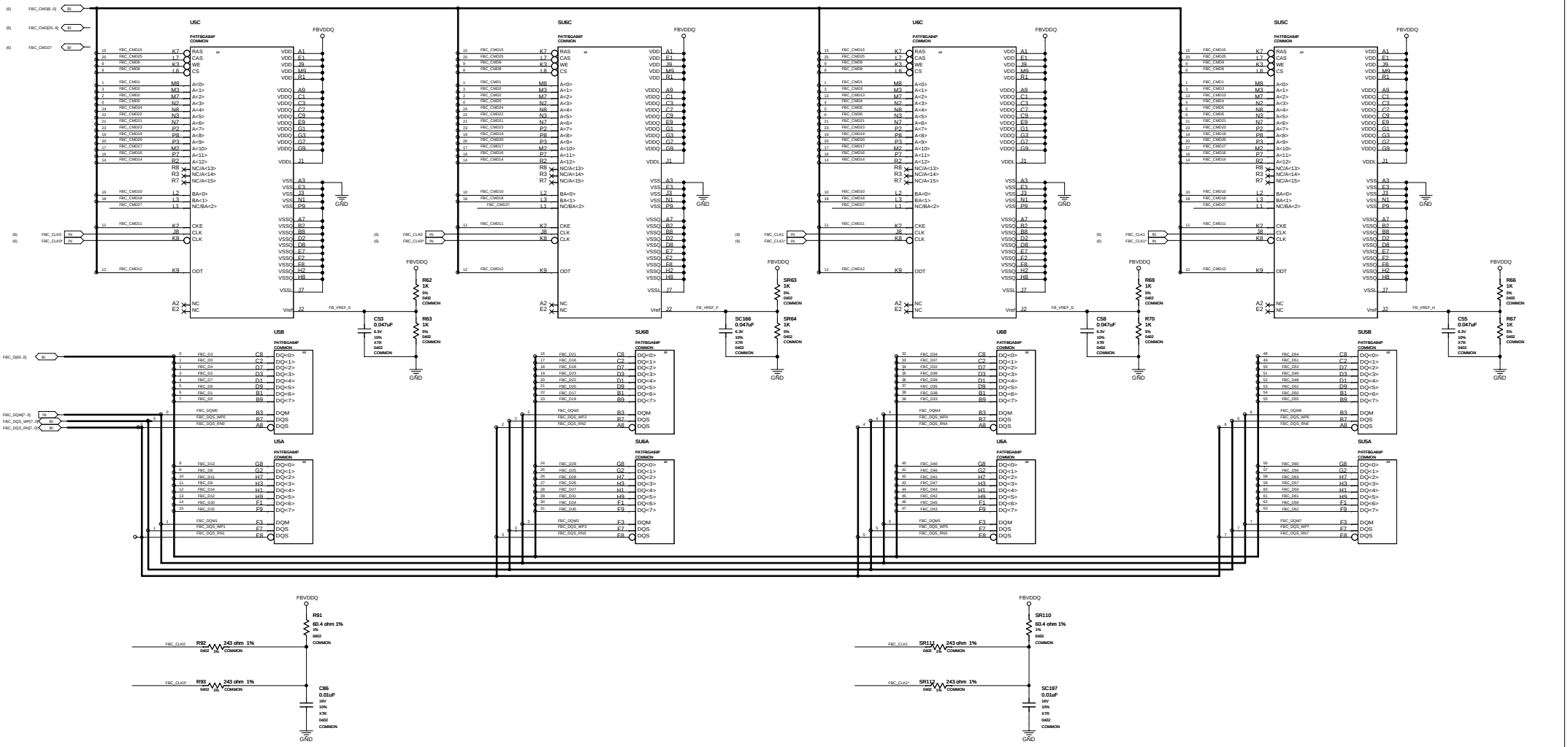


Title	<Title>	
Size	Document Number	Rev
Custom	<Doc>	A
Date:	Tuesday, June 03, 2008	Sheet 5 of 19

GPU MEMORY INTERFACE: PARTITION C

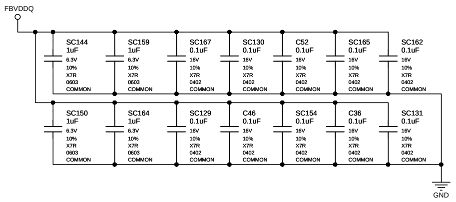


Title	<Title>		
Size	Document Number		Rev
Custom	<Doc>		A
Date:	Tuesday, June 03, 2008	Sheet 6 of 19	

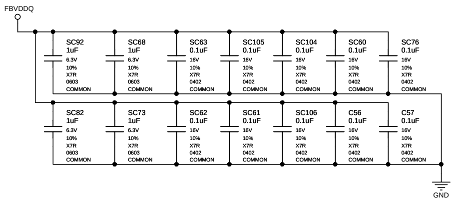


Title	<Title>	
Size	Document Number	Rev
Custom	<Doc>	A
Date:	Tuesday, June 03, 2008	Sheet 7 of 19

FRAMEBUFFER: PARTITION C DECOUPLING

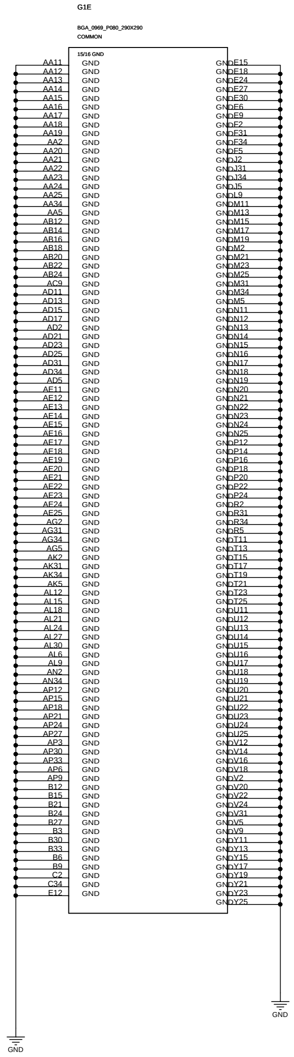


Decoupling for
FBC West Side
Memory Device.



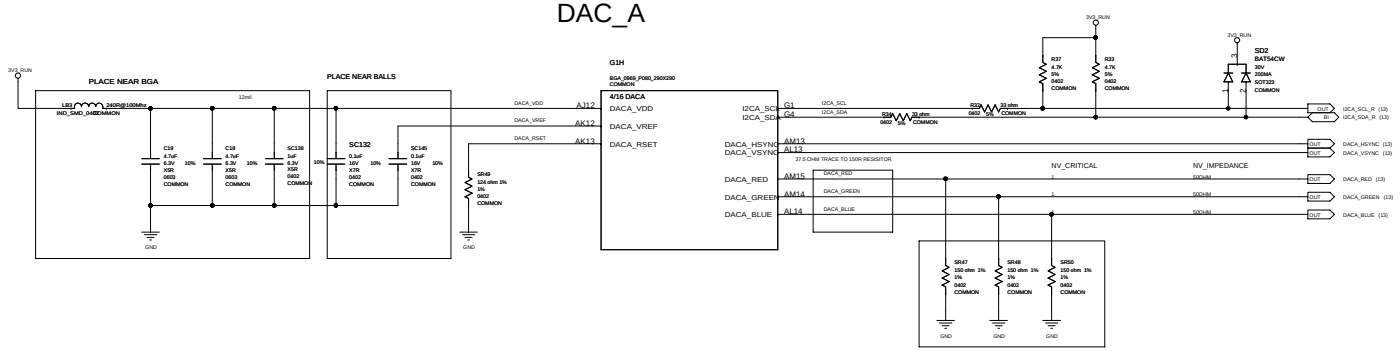
Decoupling for
FBC East Side
Memory Device.

NVVDD GROUND



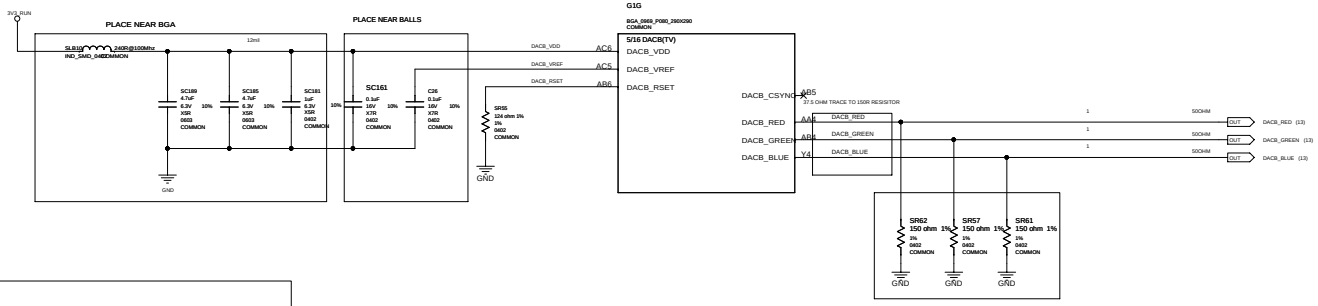
Title <Title>		
Size Custom	Document Number <Doc>	Rev A
Date: Tuesday, June 03, 2008	Sheet 8 of 19	

DAC_A

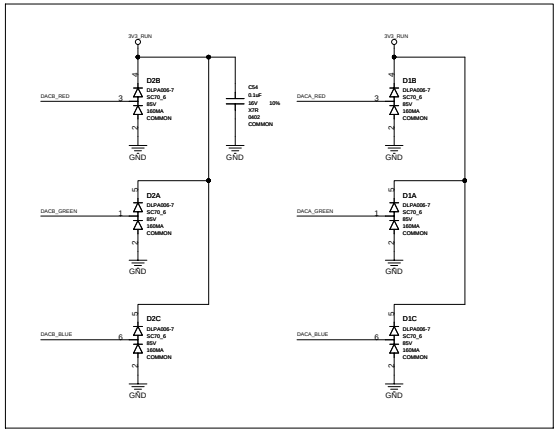


Place close to GPU

DAC_B

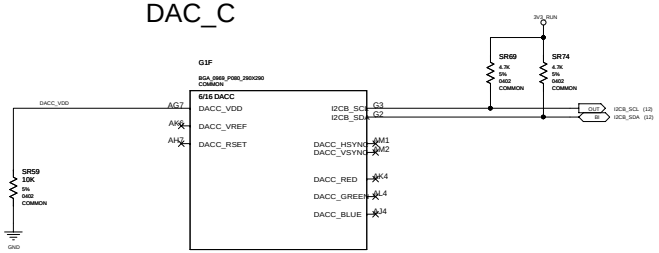


Place close to GPU



TV DAC ESD PROTECTION

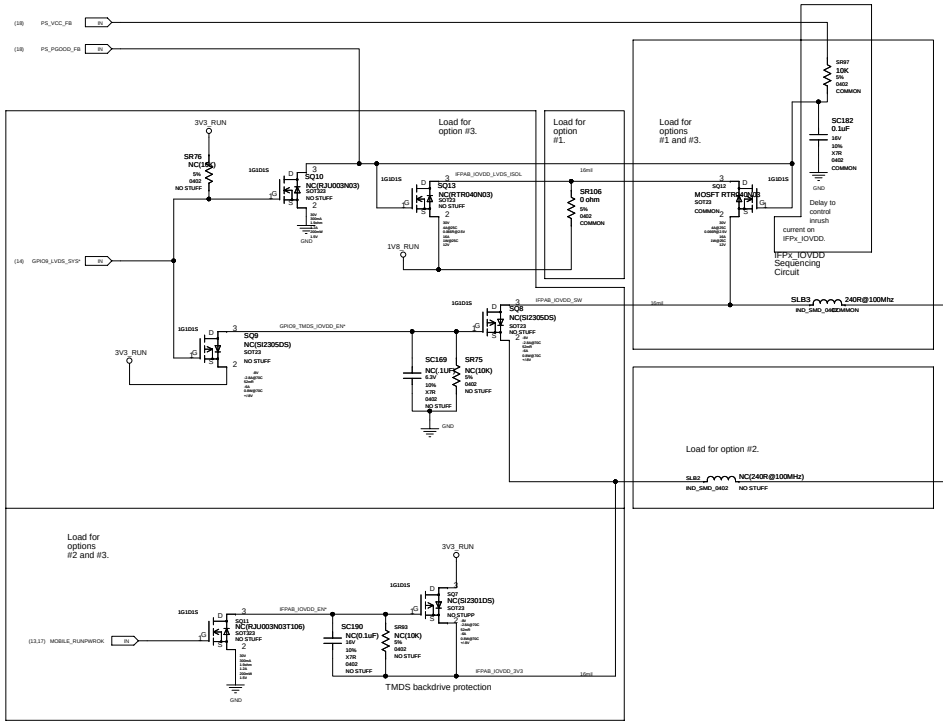
DAC_C



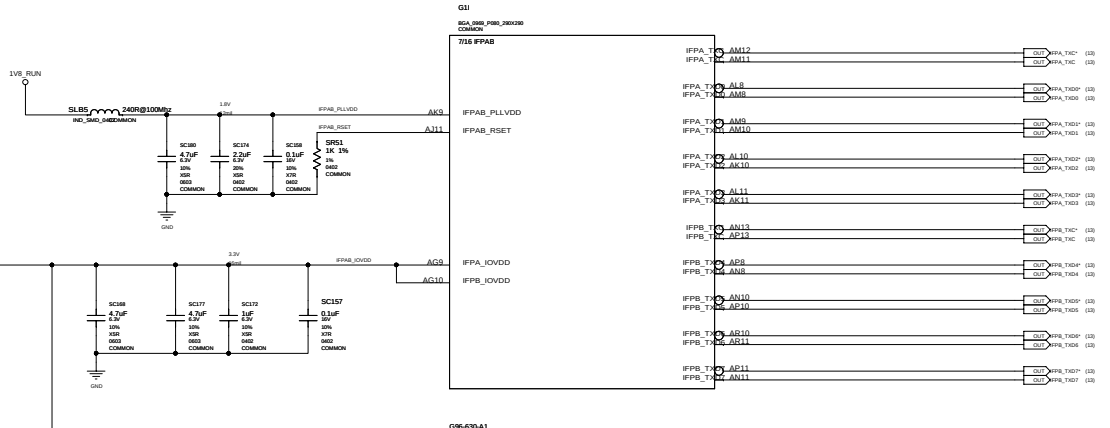
Title: <Title>		
Size: Custom	Document Number: <Doc>	Rev: A
Date: Tuesday, June 03, 2008	Sheet 9 of 19	

Loading options for IFPAB outputs

Option #1) IFPAB outputs to LVDS only.
Option #2) IFPAB outputs to DVI-C only.
Option #3) Controlled with GPIO9, IFPAB dynamically outputs to LVDS or DVI-C.



LVDS/TMDS(link A&B)

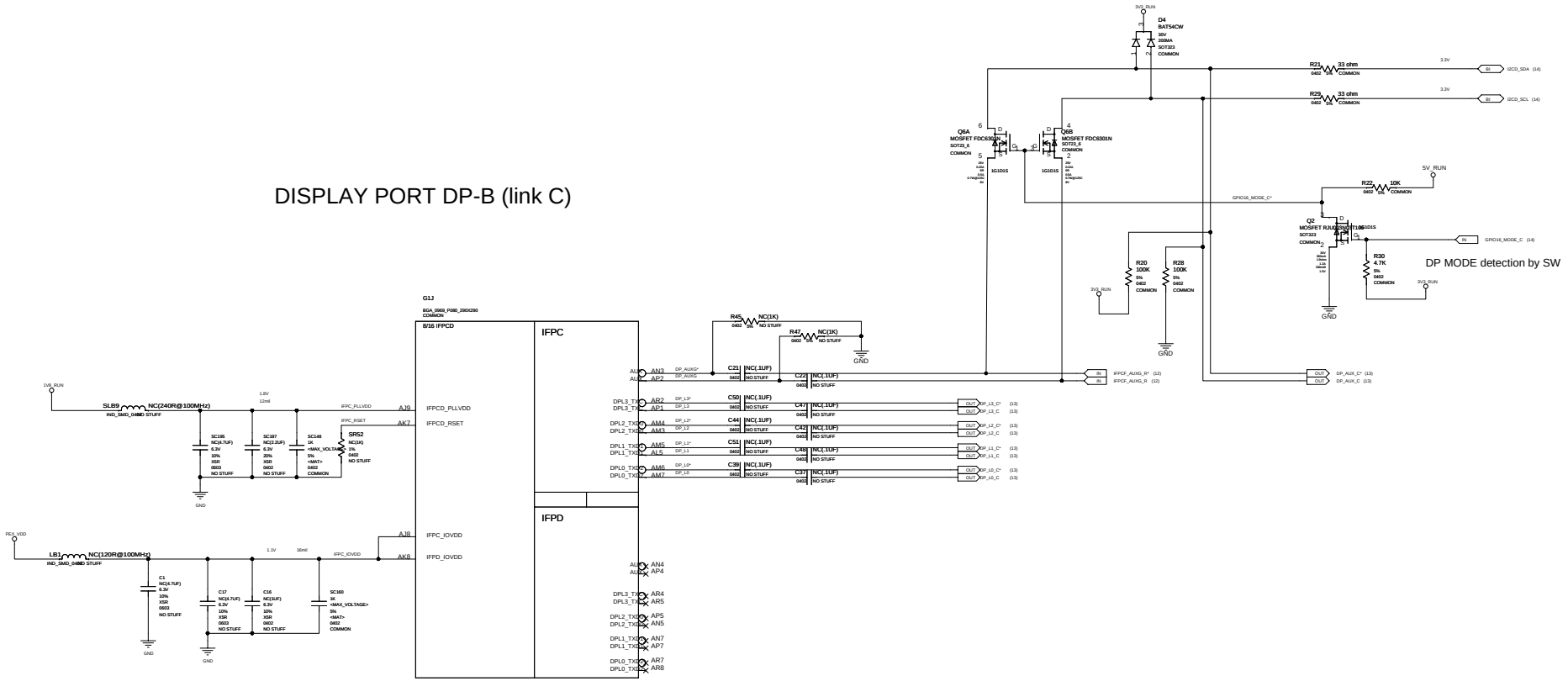


(LVDS CONSTRAINTS)

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
(12) IFPA_TXD0+	IFPATXD0	1	100DIFF
(12) IFPA_TXD0-	IFPATXD0	1	100DIFF
(12) IFPA_TXD1+	IFPATXD1	1	100DIFF
(12) IFPA_TXD1-	IFPATXD1	1	100DIFF
(12) IFPA_TXD2+	IFPATXD2	1	100DIFF
(12) IFPA_TXD2-	IFPATXD2	1	100DIFF
(12) IFPA_TXD3+	IFPATXD3	1	100DIFF
(12) IFPA_TXD3-	IFPATXD3	1	100DIFF
(12) IFPB_TXD4+	IFPBTXD4	1	100DIFF
(12) IFPB_TXD4-	IFPBTXD4	1	100DIFF
(12) IFPB_TXD5+	IFPBTXD5	1	100DIFF
(12) IFPB_TXD5-	IFPBTXD5	1	100DIFF
(12) IFPB_TXD6+	IFPBTXD6	1	100DIFF
(12) IFPB_TXD6-	IFPBTXD6	1	100DIFF
(12) IFPB_TXD7+	IFPBTXD7	1	100DIFF
(12) IFPB_TXD7-	IFPBTXD7	1	100DIFF
(12) IFPA_TXC+	IFPATXC	1	100DIFF
(12) IFPA_TXC-	IFPATXC	1	100DIFF
(12) IFPB_TXC+	IFPBTXC	1	100DIFF
(12) IFPB_TXC-	IFPBTXC	1	100DIFF

Title: <Title>			
Size: Custom	Document Number: <Doc>		Rev: A
Date: Tuesday, June 03, 2008	Sheet 10 of 19		

DISPLAY PORT DP-B (link C)



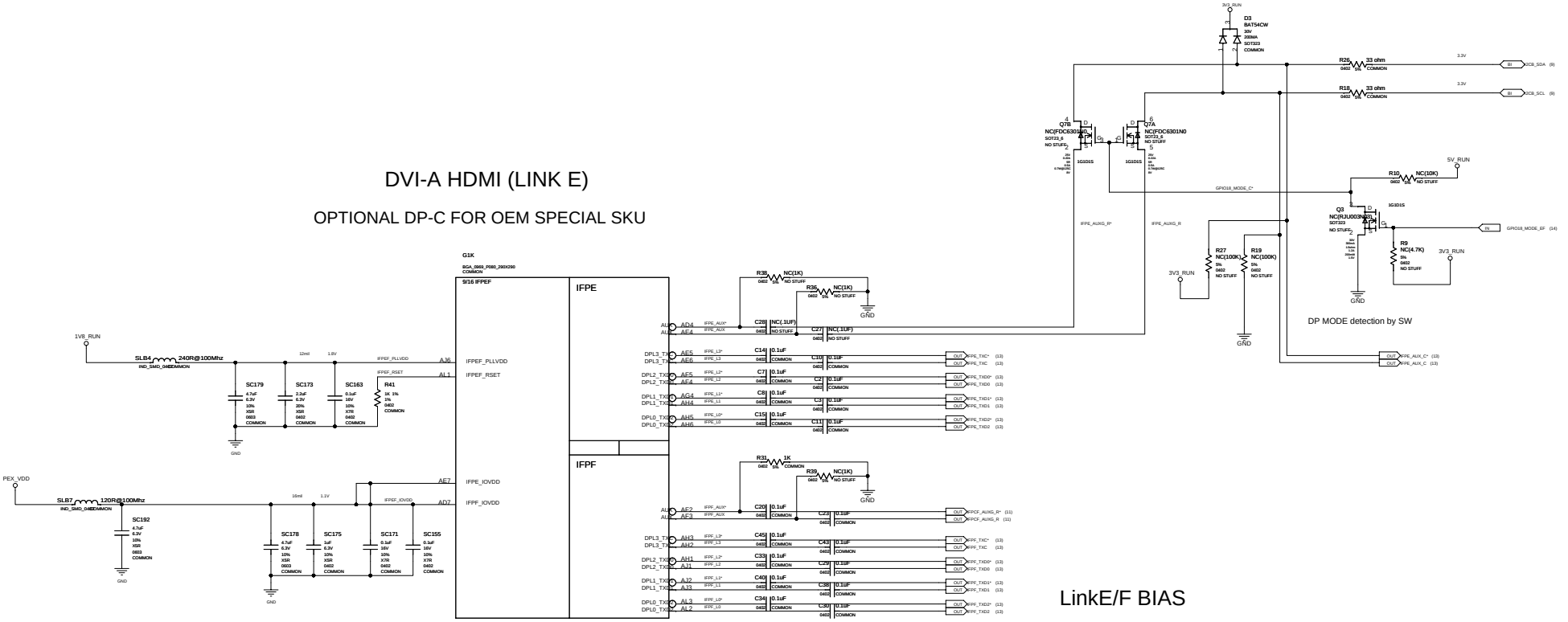
(DP CONSTRAINTS)

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
(12) DP_AUX_C*	DP_AUX3	1	100DIFF
(12) DP_AUX_C	DP_AUX3	1	100DIFF
(13) DP_L3_C*	DPL3C	1	100DIFF
(13) DP_L3_C	DPL3C	1	100DIFF
(13) DP_L2_C*	DPL2C	1	100DIFF
(13) DP_L2_C	DPL2C	1	100DIFF
(12) DP_L1_C*	DPL1C	1	100DIFF
(12) DP_L1_C	DPL1C	1	100DIFF
(13) DP_L0_C*	DPL0C	1	100DIFF
(13) DP_L0_C	DPL0C	1	100DIFF

Title	<Title>	
Size: Custom	Document Number: <Doc>	Rev: A
Date: Tuesday, June 03, 2008	Sheet 11 of 19	

DVI-A HDMI (LINK E)

OPTIONAL DP-C FOR OEM SPECIAL SKU



DISPLAY PORT DP-A (LINK F)

OPTIONAL DVI-B TMDS SL OR DL W/ DVI-A

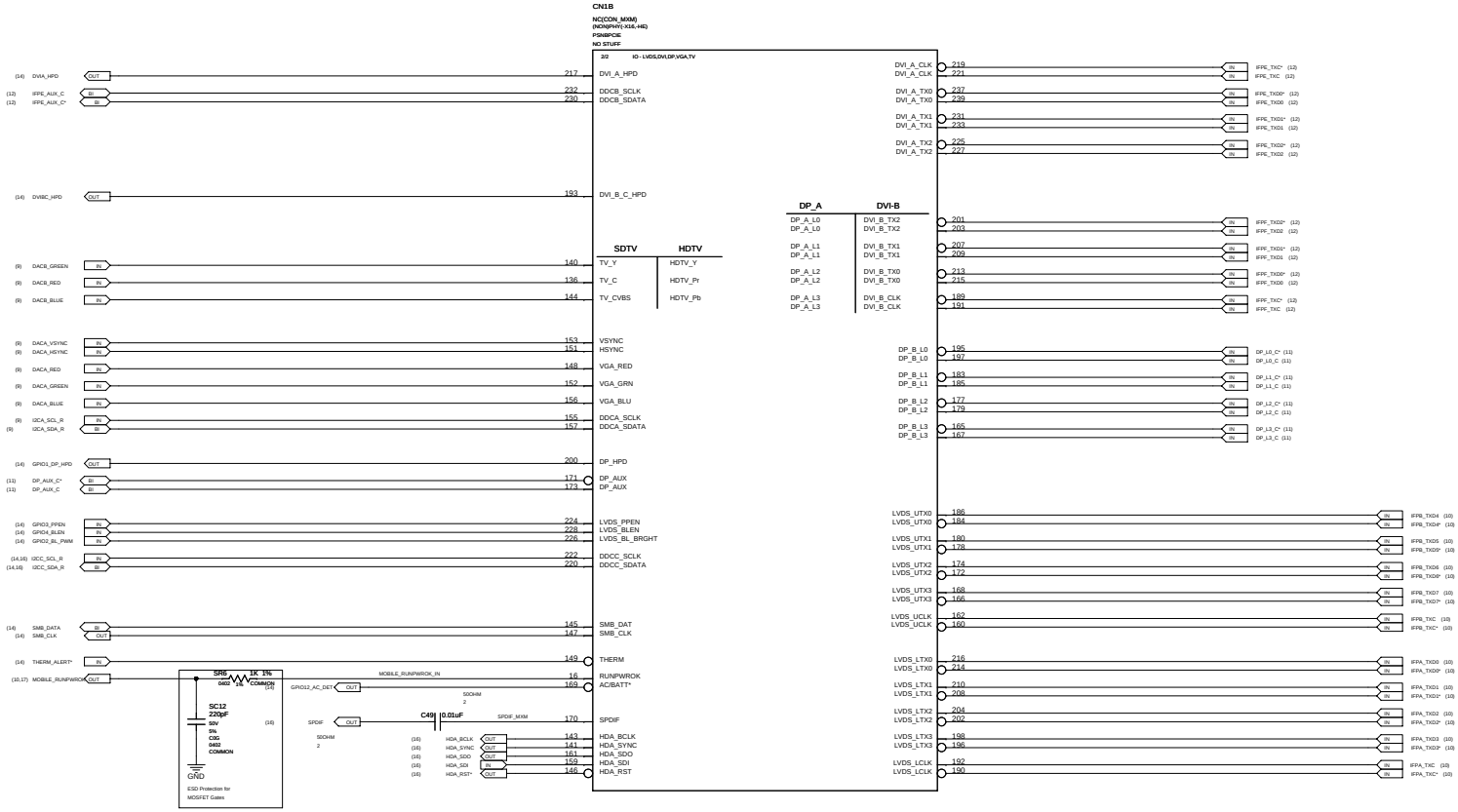
(TMDS/HDMI/DP OPTION CONSTRAINTS)

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
IFPE_TXC*	IFPETXC	1	100DIFF
IFPE_TXC	IFPETXC	1	100DIFF
IFPE_TXD0*	IFPETXD0	1	100DIFF
IFPE_TXD0	IFPETXD0	1	100DIFF
IFPE_TXD1*	IFPETXD1	1	100DIFF
IFPE_TXD1	IFPETXD1	1	100DIFF
IFPE_TXD2*	IFPETXD2	1	100DIFF
IFPE_TXD2	IFPETXD2	1	100DIFF

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
IFPE_TXC*	IFPETXC	1	100DIFF
IFPE_TXC	IFPETXC	1	100DIFF
IFPE_TXD0*	IFPETXD0	1	100DIFF
IFPE_TXD0	IFPETXD0	1	100DIFF
IFPE_TXD1*	IFPETXD1	1	100DIFF
IFPE_TXD1	IFPETXD1	1	100DIFF
IFPE_TXD2*	IFPETXD2	1	100DIFF
IFPE_TXD2	IFPETXD2	1	100DIFF

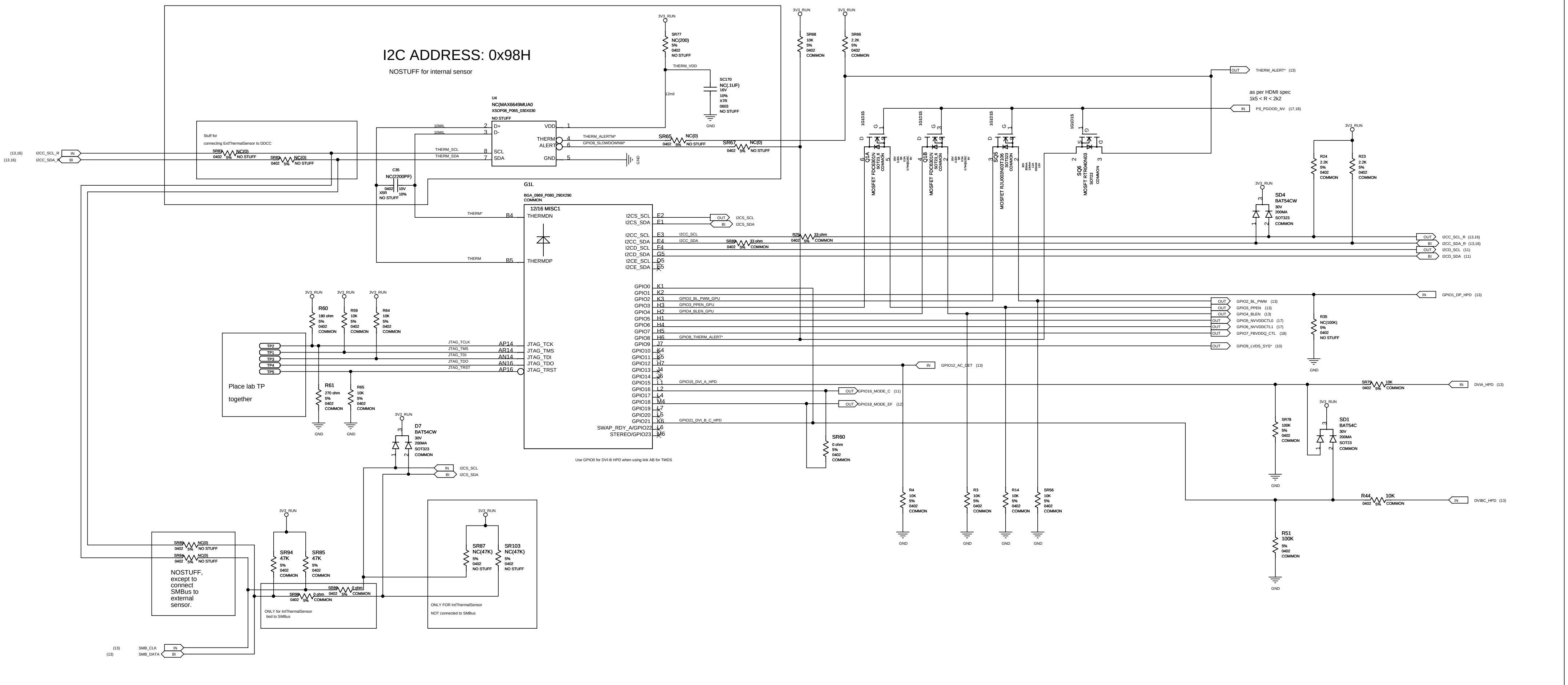
Title	<Title>		
Size: Custom	Document Number <Doc>		Rev A
Date: Tuesday, June 03, 2008	Sheet 12 of 19		

MXM CONNECTOR



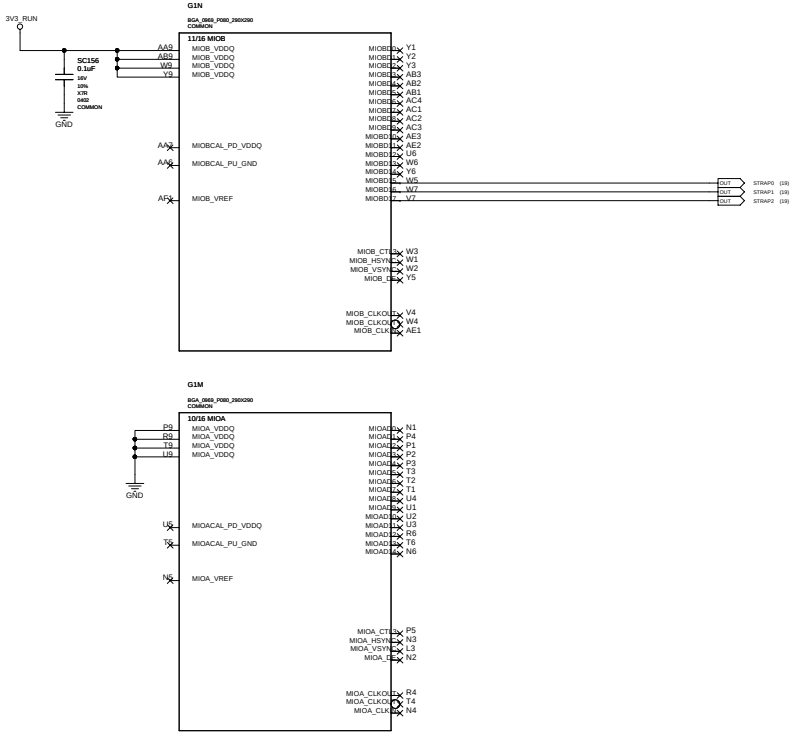
Title	<Title>		
Size	Document Number		Rev
Custom	<Doc>		A
Date:	Tuesday, June 03, 2008	Sheet 13 of 19	

GPIO, TEMP SENSOR, JTAG



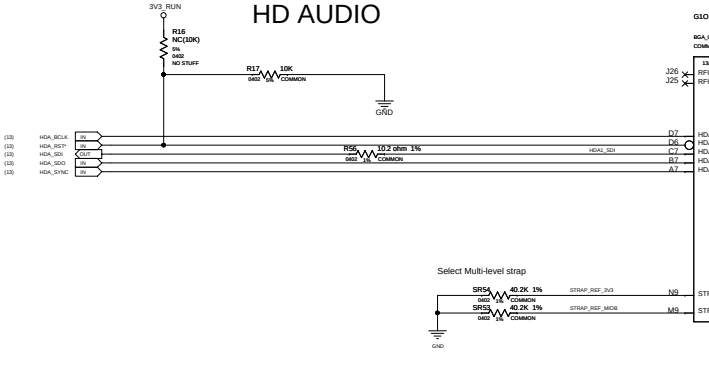
Title	<Title>		
Size Custom	Document Number <Doc>		Rev A
Date:	Tuesday, June 03, 2008	Sheet 14 of 19	

MIOA/B

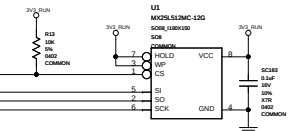


Title: <Title>		
Size: Custom	Document Number: <Doc>	Rev: A
Date: Tuesday, June 03, 2008	Sheet 15 of 19	

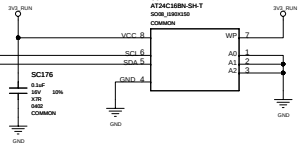
HD AUDIO



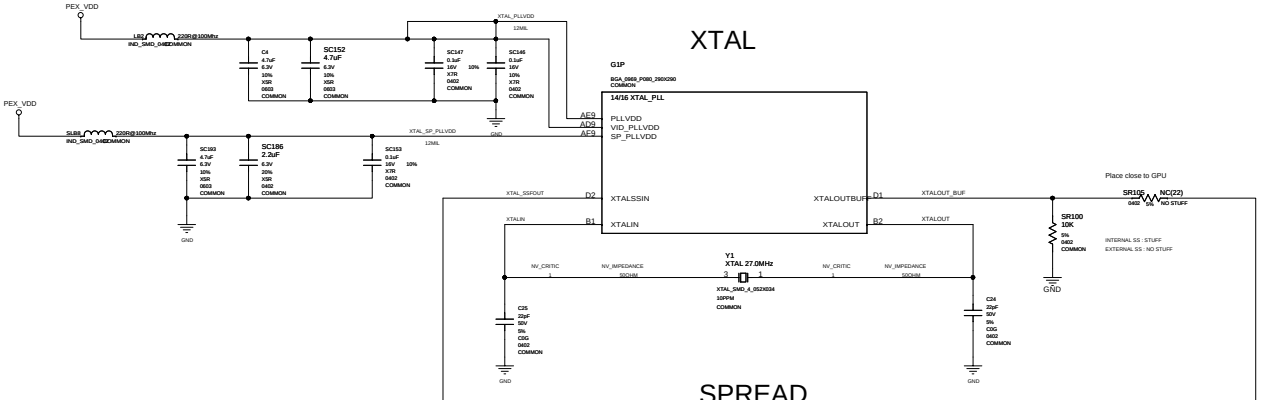
VBIOS ROM



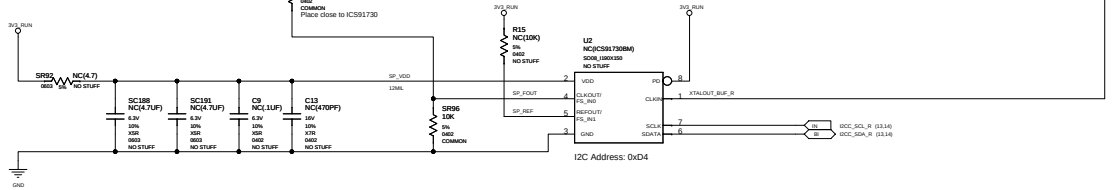
HDCP I2C ROM



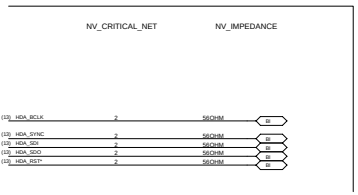
XTAL



SPREAD



(HD AUDIO CONSTRAINTS)

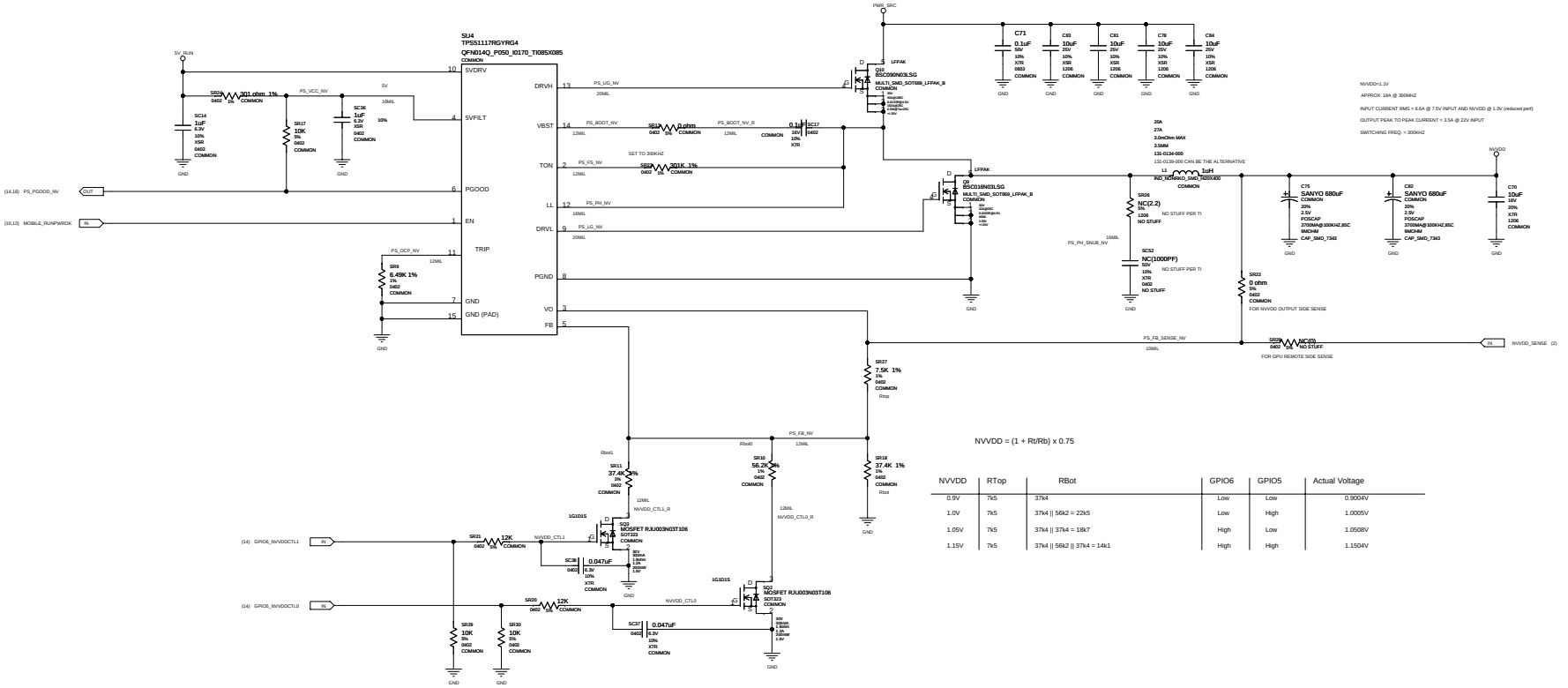


Title	<Title>		
Size	Document Number		Rev
Custom	<Doc>		A
Date:	Tuesday, June 03, 2008	Sheet 16 of 19	

NVVDD POWER SUPPLY

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
NVVDD	1V	12MIL	18A

NVVDD SWITCHER POWER SUPPLY



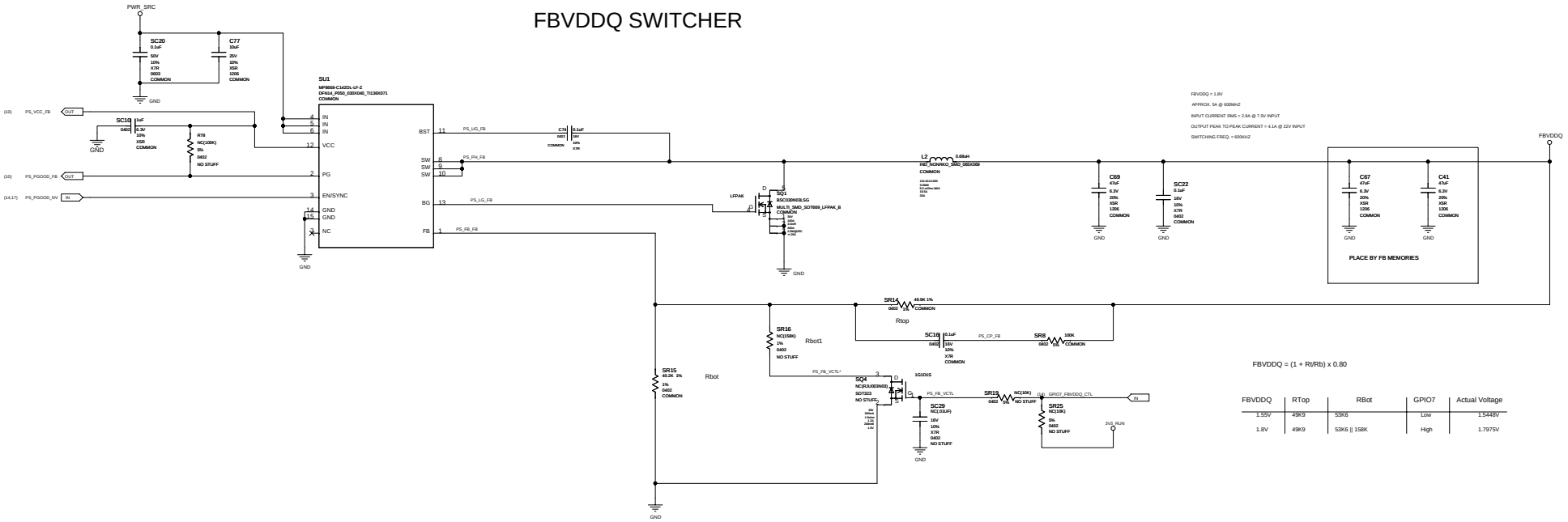
NVVDD	RTop	RBot	GPIO6	GPIO5	Actual Voltage
0.9V	7k5	37k4	Low	Low	0.9004V
1.0V	7k5	37k4 || 56k2 = 22k5	Low	High	1.0005V
1.05V	7k5	37k4 || 37k4 = 18k7	High	Low	1.0508V
1.15V	7k5	37k4 || 56k2 || 37k4 = 14k1	High	High	1.1504V

Title	<Title>		
Size	Document Number Custom<Doc>		Rev A
Date:	Tuesday, June 03, 2008	Sheet 17 of 19	

FBVDDQ AND PEX_VDD POWER SUPPLY

NET	VOLTAGE	NV_NET_MAX_CURRENT
PEX_VDD	1.1V	6A
FBVDDQ	1.8V	5A

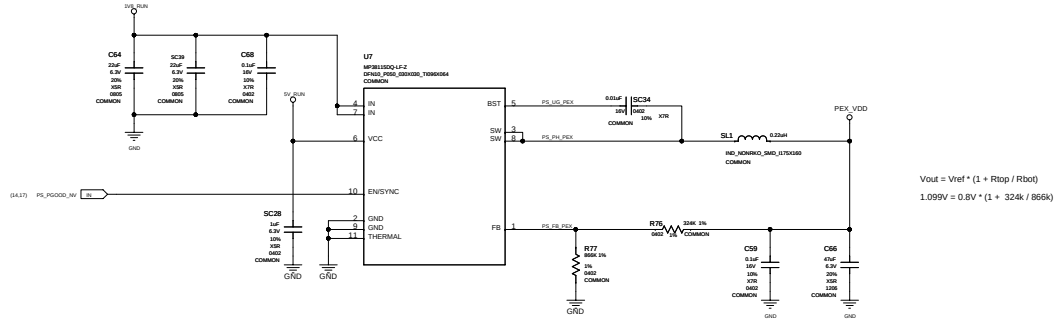
FBVDDQ SWITCHER



FBVDDQ = (1 + Rt/Rb) x 0.80

FBVDDQ	RTop	RBot	GPIO7	Actual Voltage
1.55V	49K9	53K6	Low	1.5448V
1.8V	49K9	53K6 || 158K	High	1.7975V

PEX_VDD SWITCHER

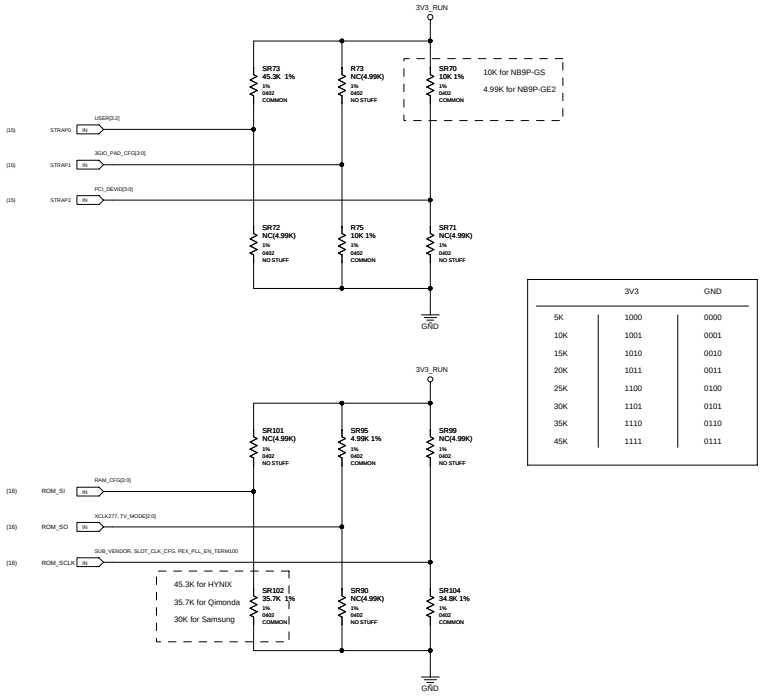


Vout = Vref * (1 + Rtop / Rbot)

1.099V = 0.8V * (1 + 324k / 866k)

Title	<Title>			
Size	Document Number			Rev
	Custom<Doc>			A
Date:	Tuesday, June 03, 2008	Sheet	18 of	19

STRAPPING OPTIONS



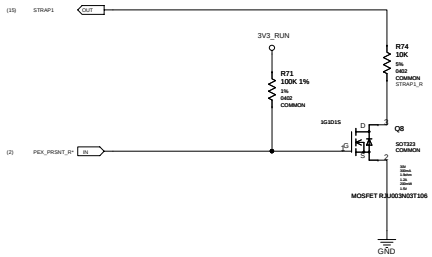
	3V3	GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

STRAP0	USER_BIT0	0xF: 45K PU (unused)	
	USER_BIT1		
	USER_BIT2		
	USER_BIT3		
STRAP1	3GIO_PADCFG_LUT_ADR0		
	3GIO_PADCFG_LUT_ADR1	0x0: Desktop default (normal swing) - 5k PD	
	3GIO_PADCFG_LUT_ADR2	0x1: Mobile default (low swing) - 10k PD	
	3GIO_PADCFG_LUT_ADR3	acc. to //hw/tesla_g98b/manuals/dev_ext_devices.ref	
STRAP2	PCI_DEVID_0	all 4 bits set by HW strapping	
	PCI_DEVID_1	0x0649: 10K PU (NB9P-GS)	
	PCI_DEVID_2	0x0648: 5K PU (NB9P-GE2)	
	PCI_DEVID_3	0x065C: 25K PU (NB9P-GLM2)	
ROM_SO	TV_MODE_BIT0	0x0: NTSC-M	
	TV_MODE_BIT1		5K PU
	TV_MODE_BIT2		
	XCLK_277	1: PCI-E GEN2	

ROM_SI	256 MB (4pcs. 16Mx32)		512 MB (4pcs. 32Mx32)	
	RAM_CFG[3:0]	Definitions	RAM_CFG[3:0]	Definitions
RAM_CFG_0	0000	Reserved	0100 25k PD	Reserved
RAM_CFG_1	0001	Qimonda	0101 30k PD	Qimonda
RAM_CFG_2	0010	Hynix	0110 35k PD	Hynix
RAM_CFG_3	0011	Samsung	0111 45k PD	Samsung

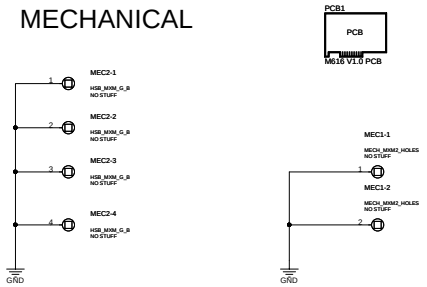
ROM_SCLK			
	PEX_PLL_EN_TERM100	0:	
	SLOT_CLK_CONFIG	1: GPU/MCH SHARE COM REF CLK	35K PD
	SUB_VENDOR	1: SUB_VENDOR BIOS	
	PCI_DEVID_EXT	0: TERM100 DISABLED	

PEX SWING LEVEL



PEX_PRSNT2_R	R_STRAP1	3_GIO_PADCFG_LUT<3..0>
GND	10k	0x1 MOBILE_DEFAULT
FLOAT	5k (10k ll 10k)	0x0 DESKTOP_DEFAULT

MECHANICAL



Title	<Title>		
Size	Document Number <Doc>		Rev A
Date:	Tuesday, June 03, 2008	Sheet 19 of 19	