

PG600-B02 NIGHTHAWK


GB3B-384, 6GB GDDR5 128Mx32
DP + HDMI/DP + DP + DP + DVI-I

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03 Remove Jtag
04-18 更改<> 5 CMD0/DAT
21 ADD DQG-0500500-005
22 更改DVI-I footprint
23 更改DP1-I footprint
24 更改HDMI-I footprint & 更改COLAY/DP
25 更改DP footprint
26 更改SLIC 更改COLAY
30 更改MEM PWRM
27 更改JTAG & Stereo Heard
31-35 更改V3217 1.1 NVVDD POWER
36 REMOVE NO STUFF FOR GEFORCE SKUS ONLY / 更改input choke
39 更改滤波片
40 Remove Bypass filter option
41 Remove MCU

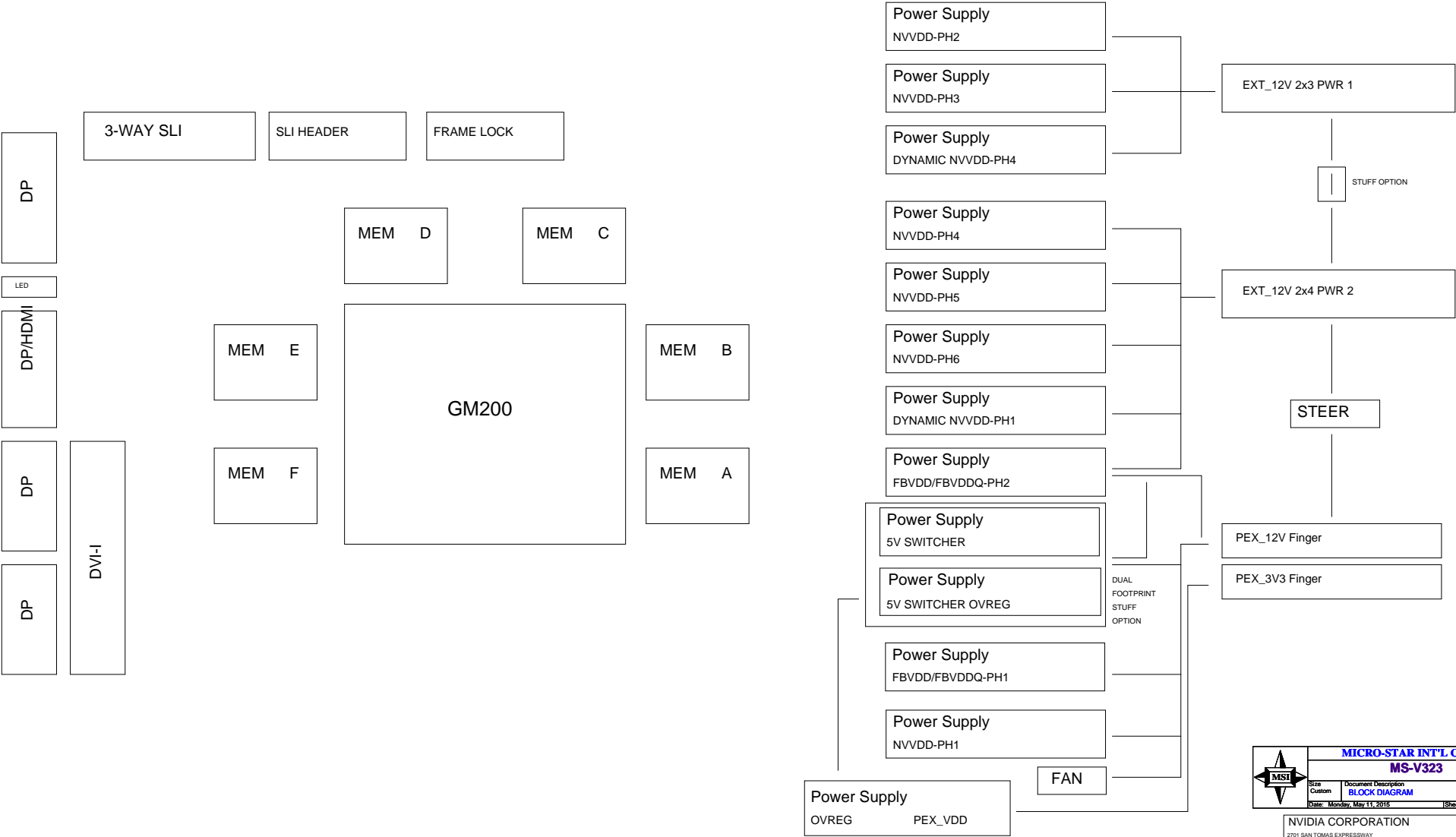
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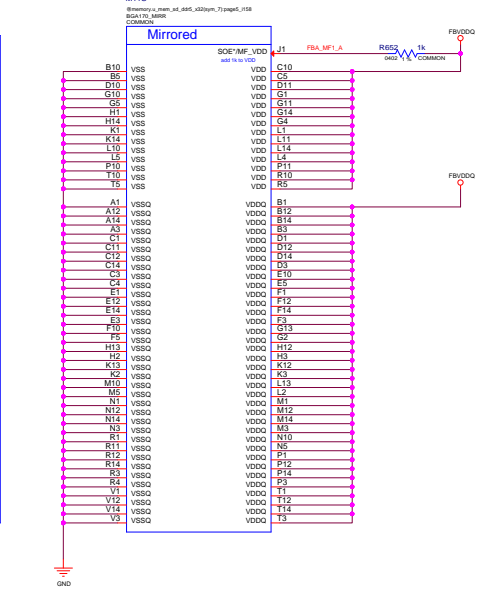
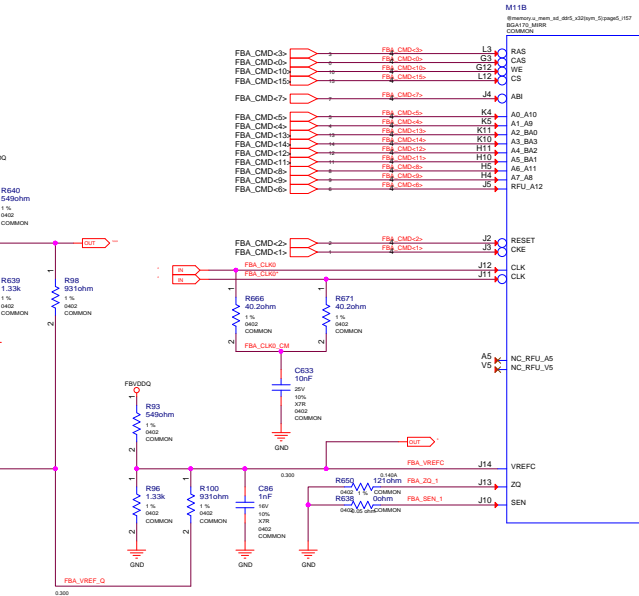
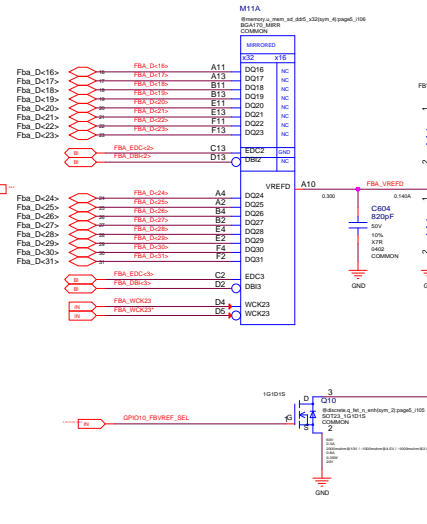
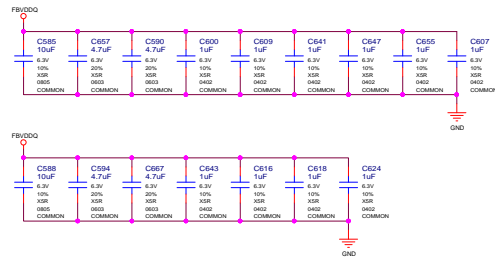
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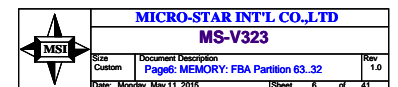


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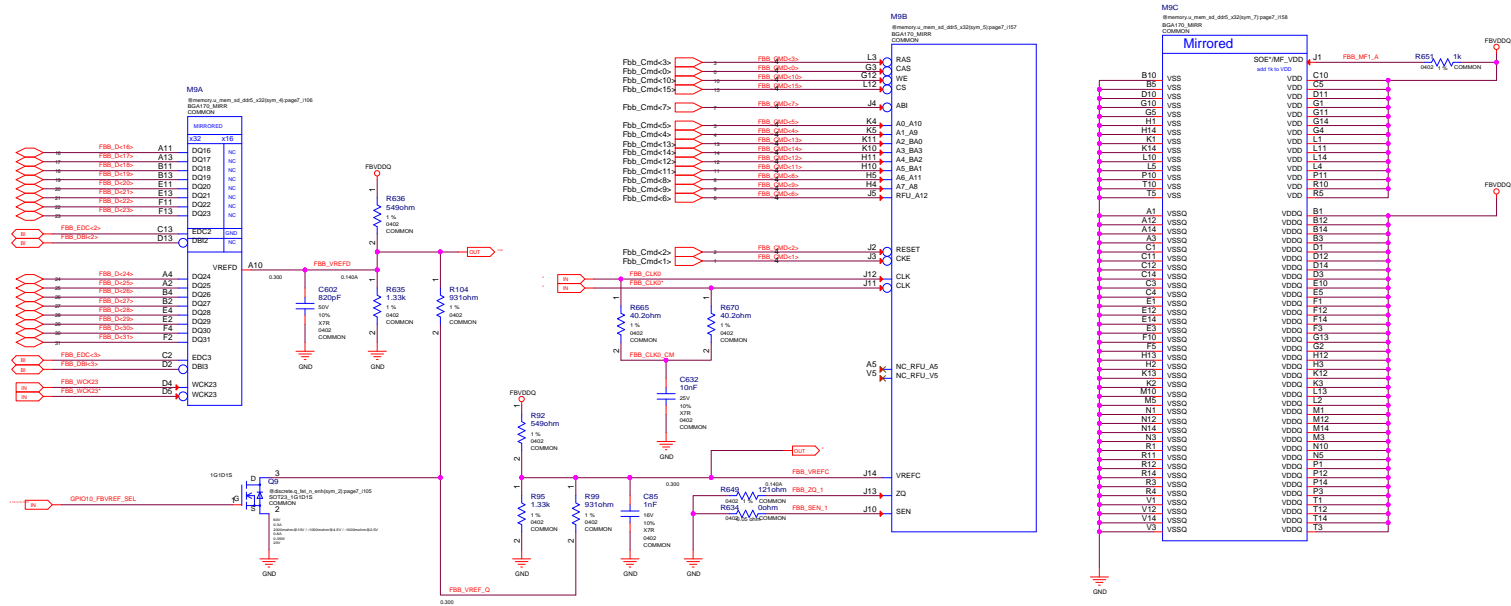
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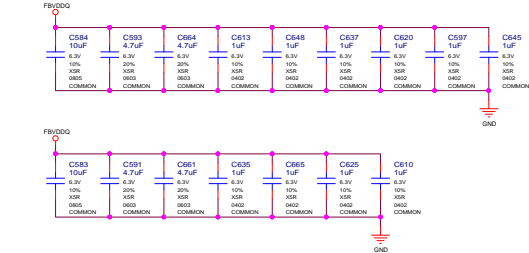


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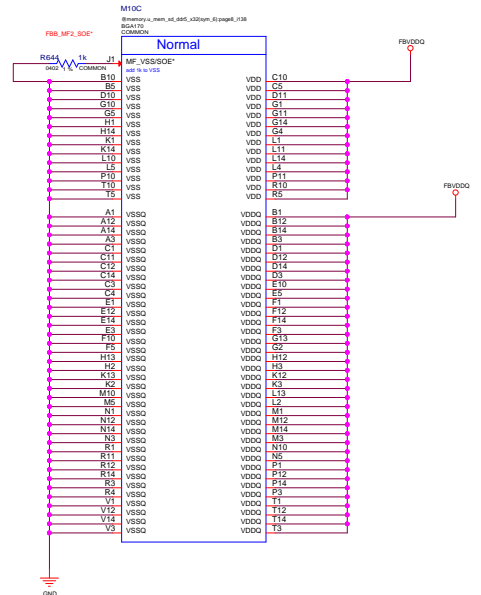
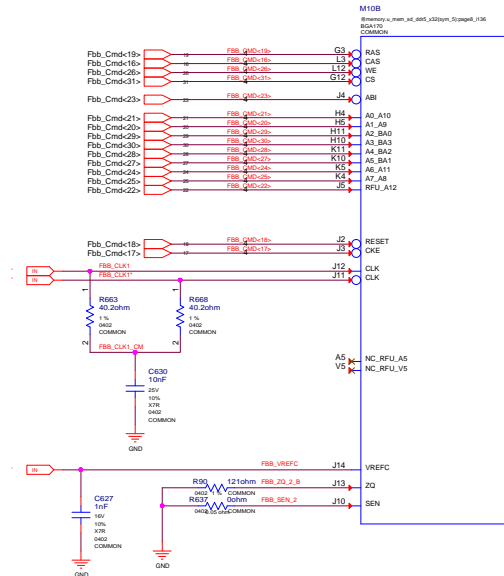
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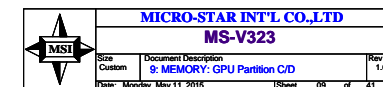
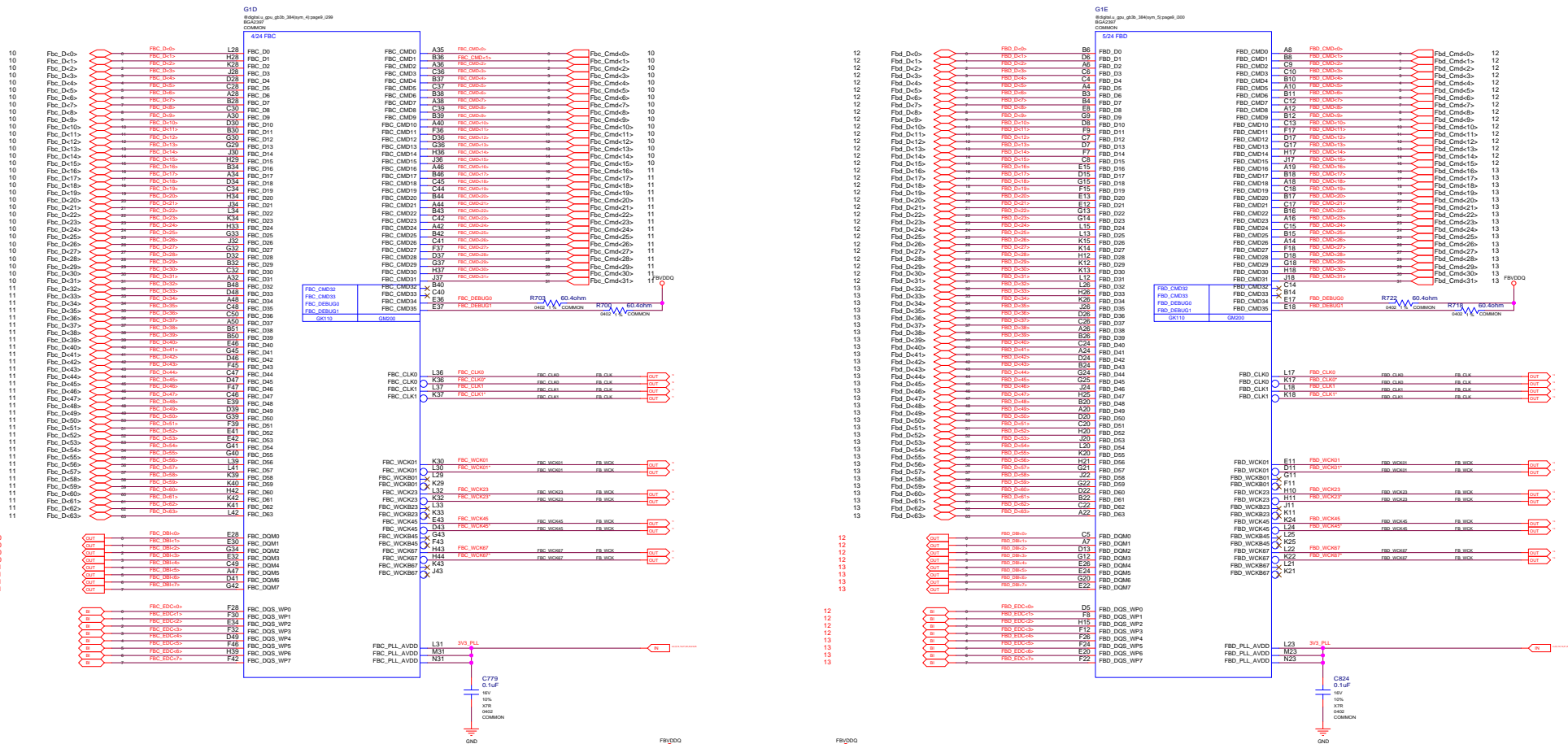
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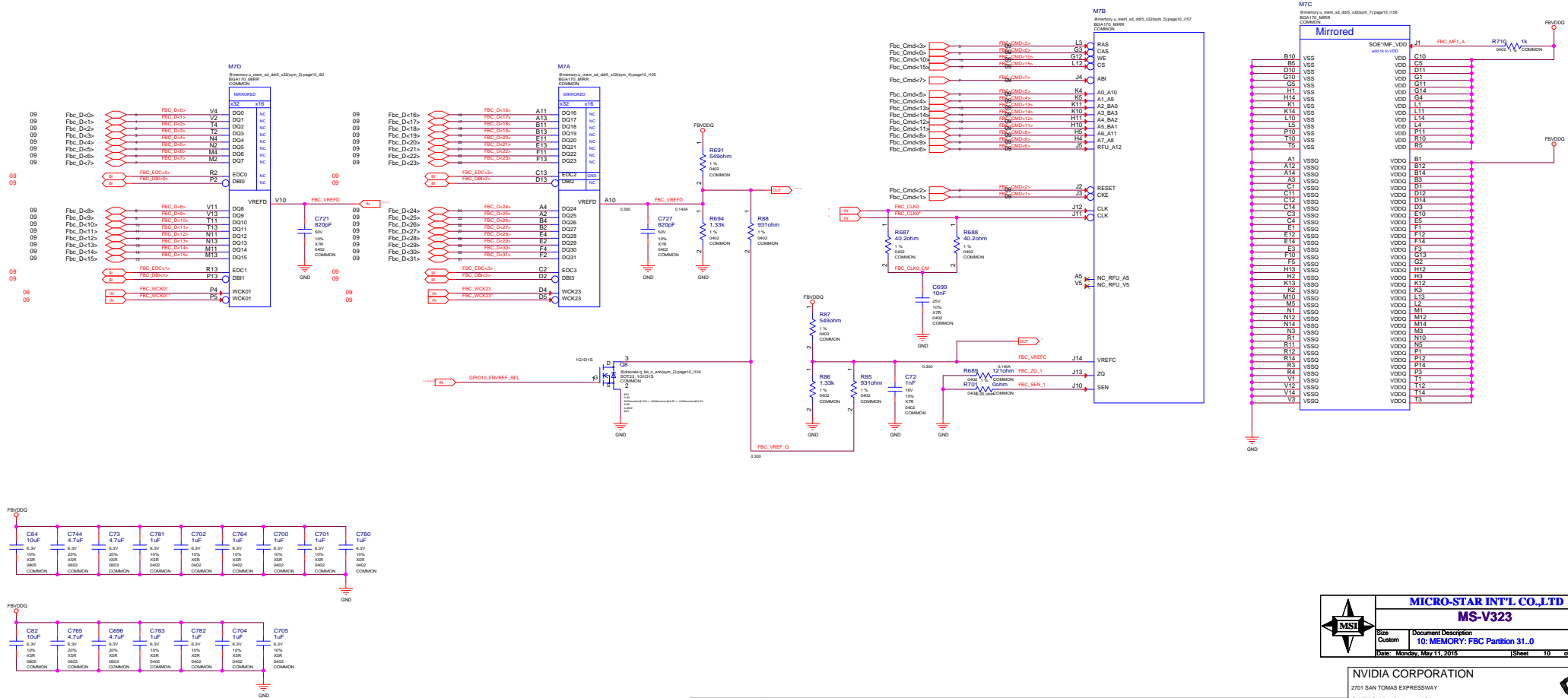
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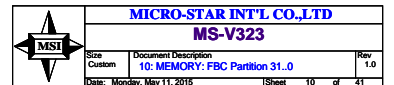


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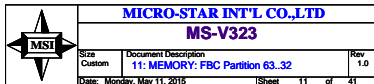
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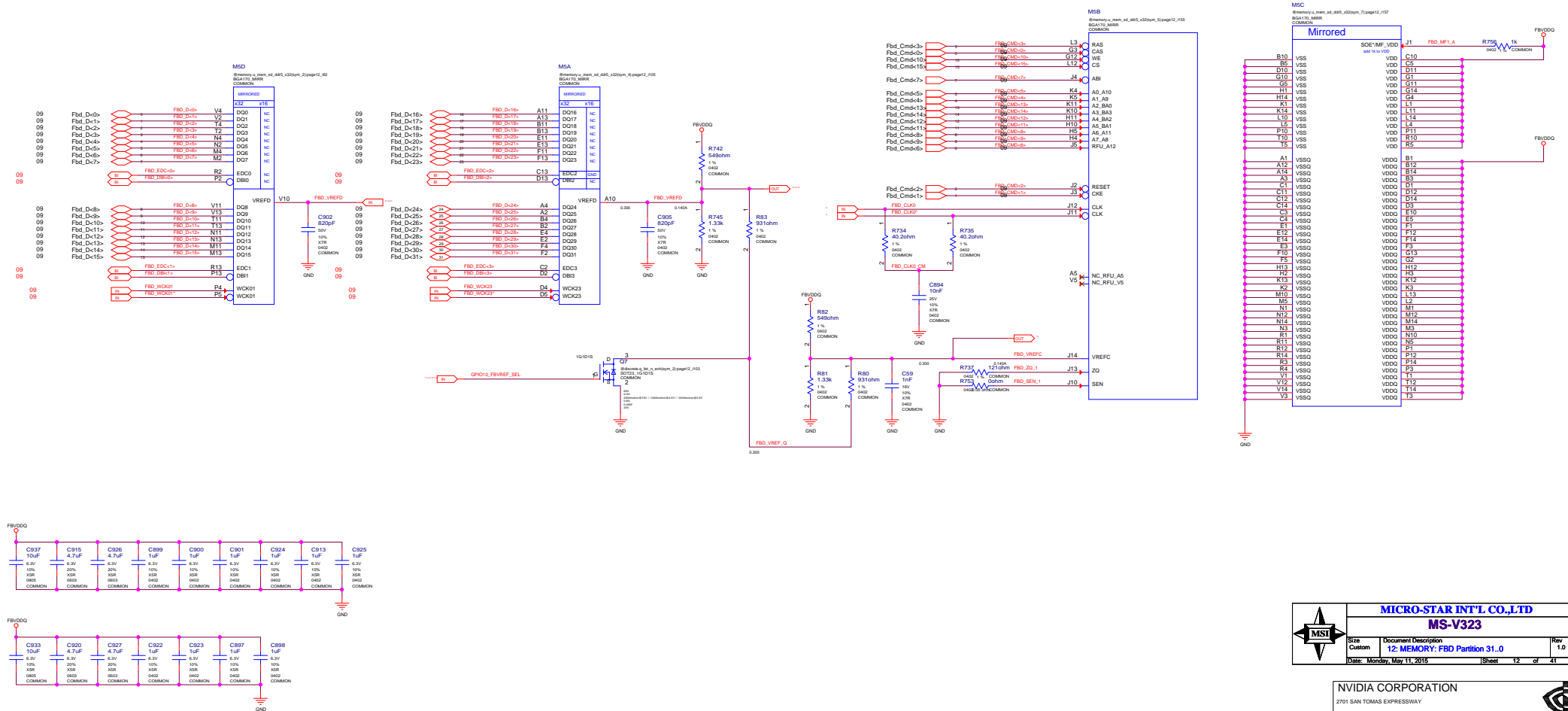
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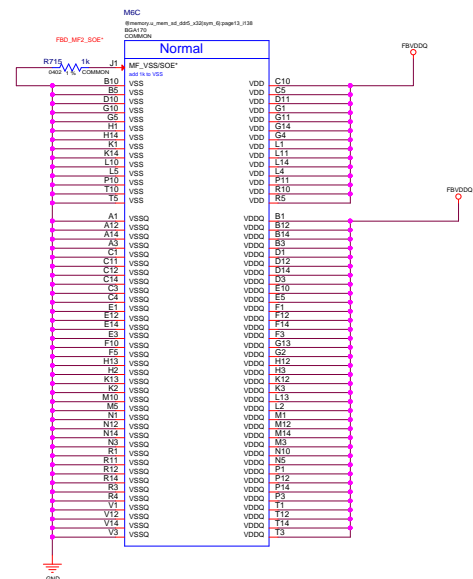
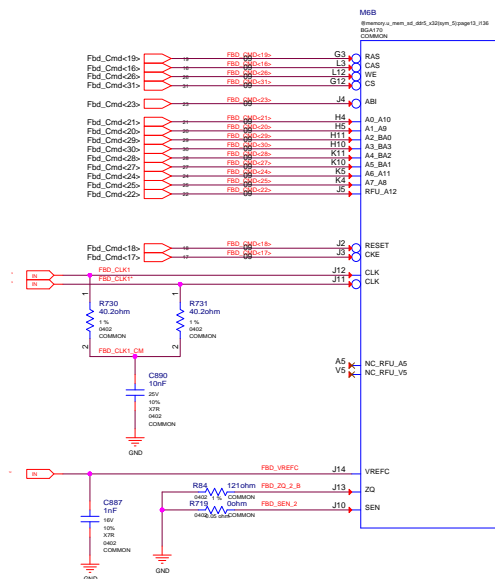
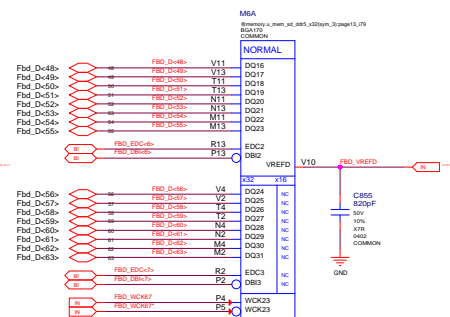
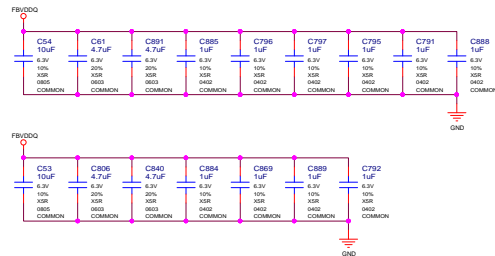



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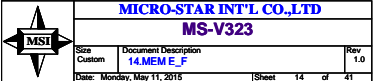
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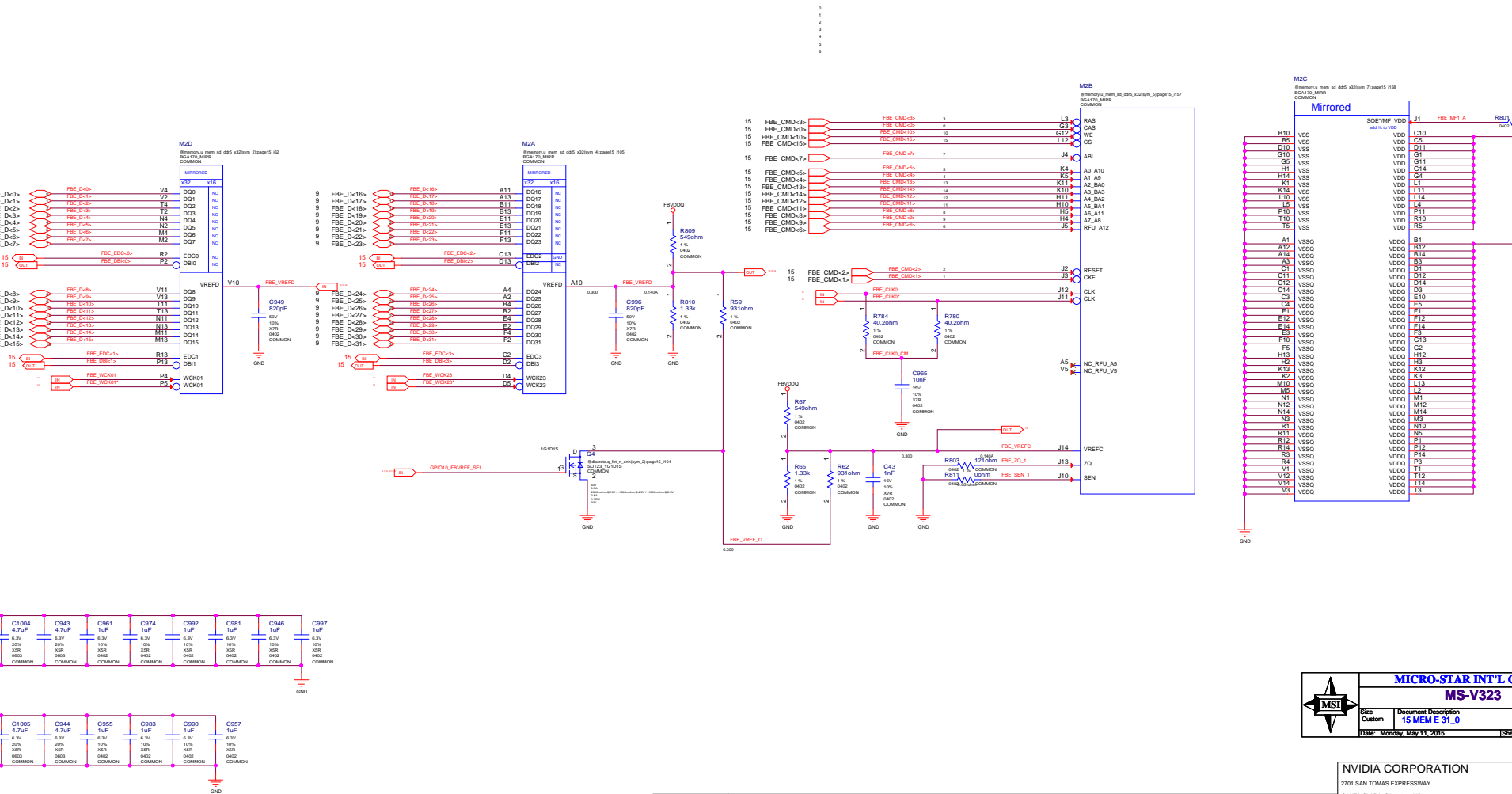
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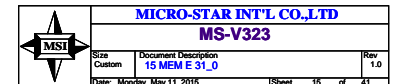


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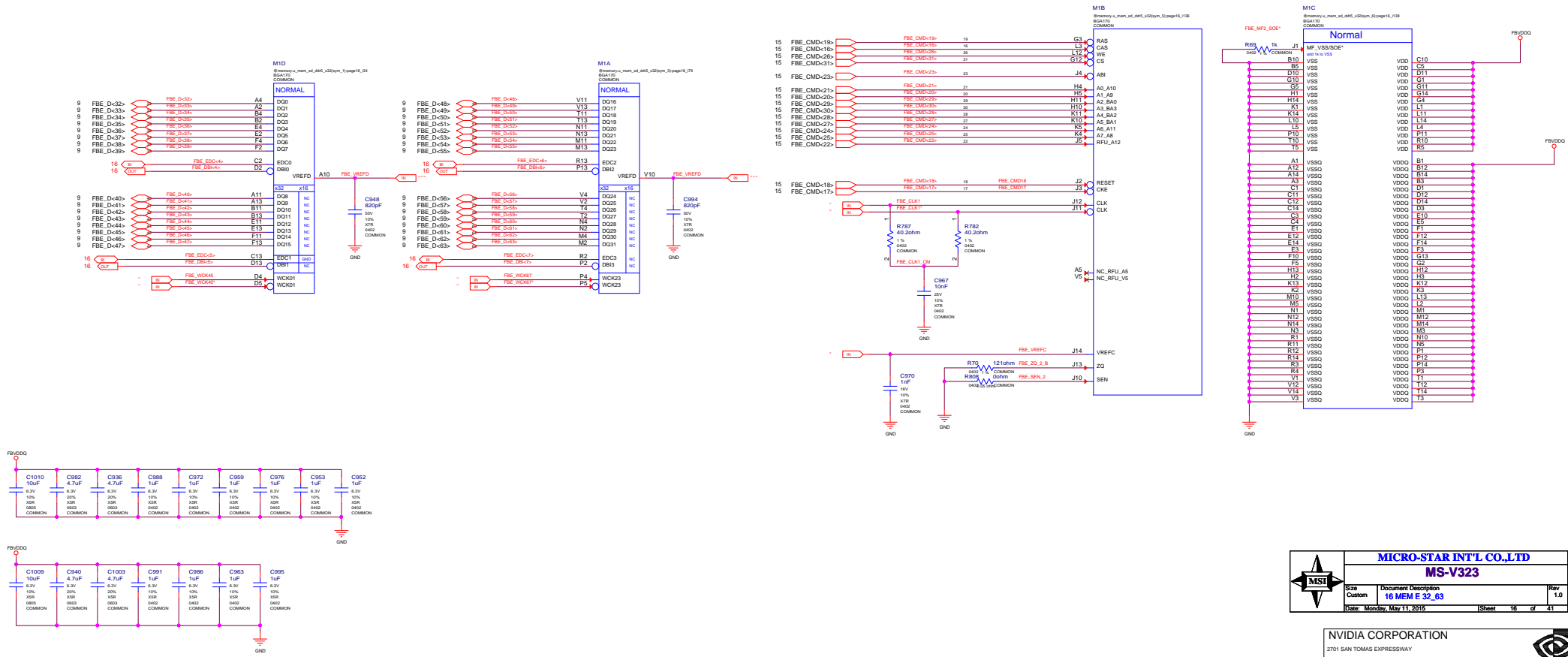
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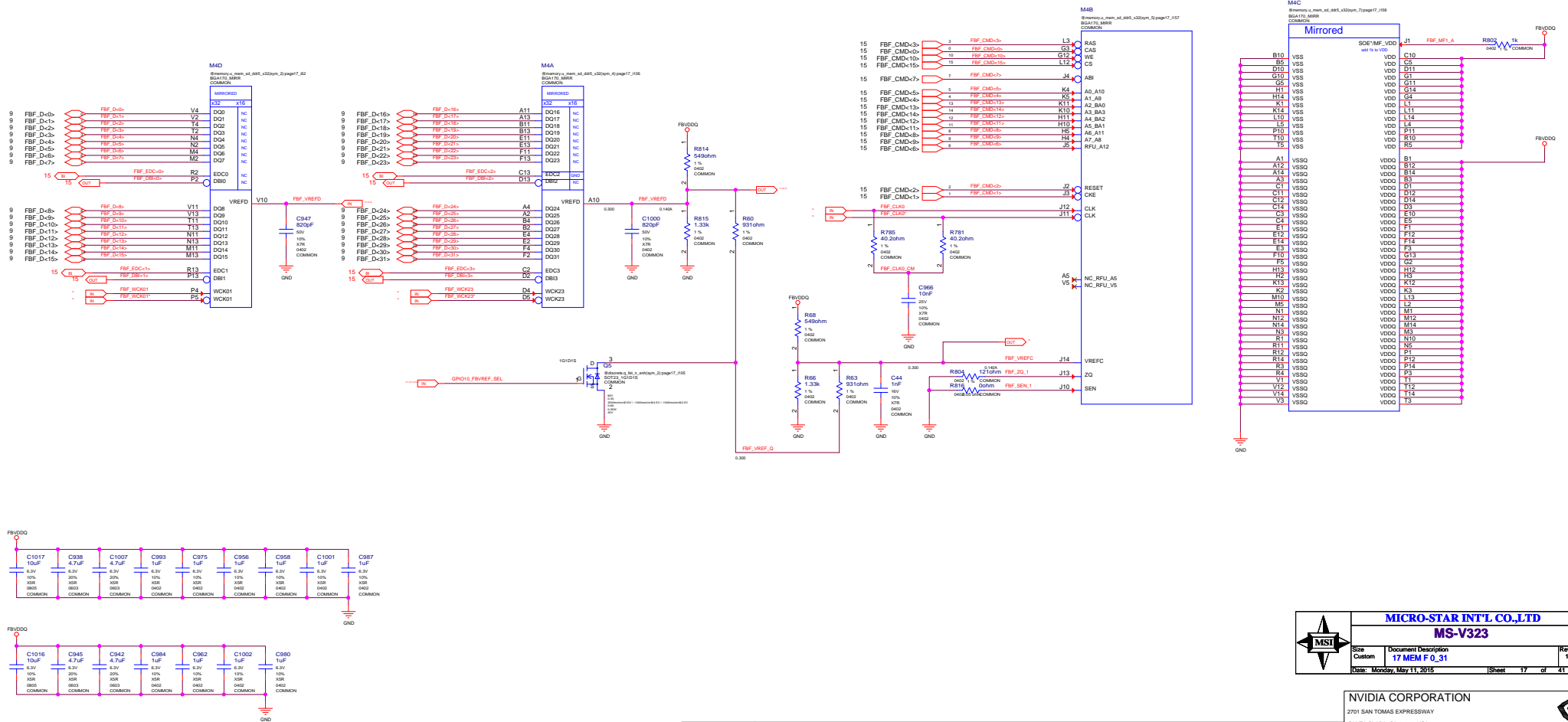


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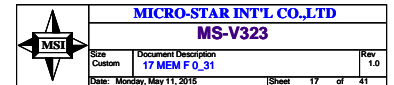
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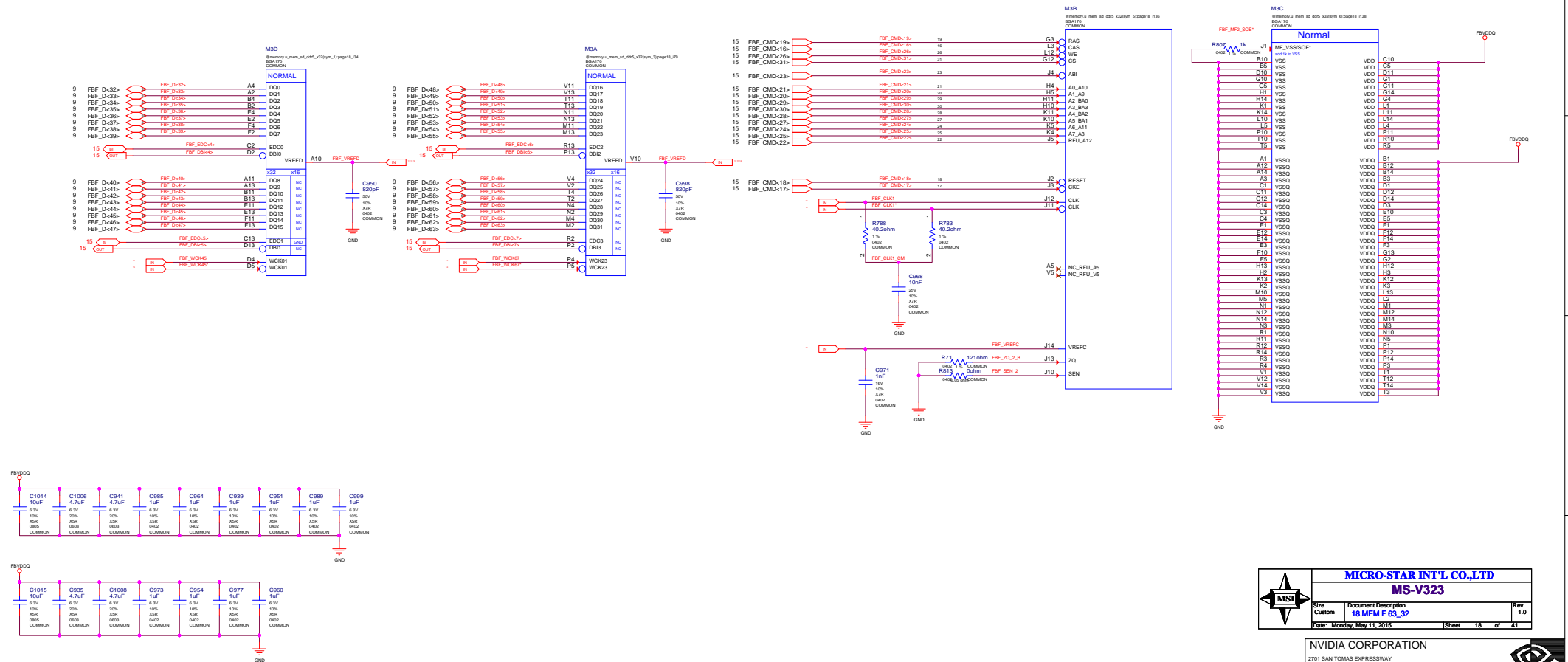
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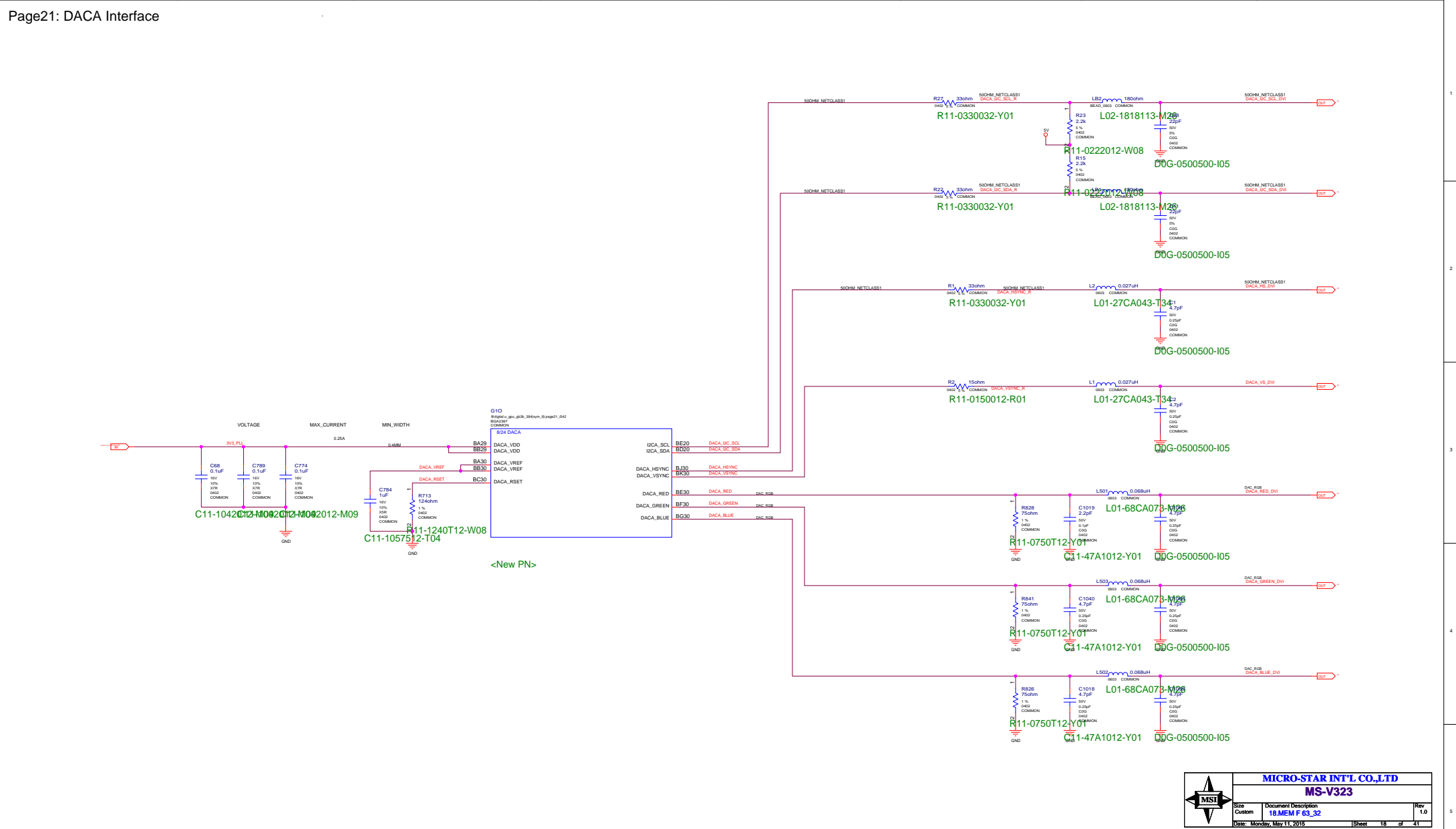
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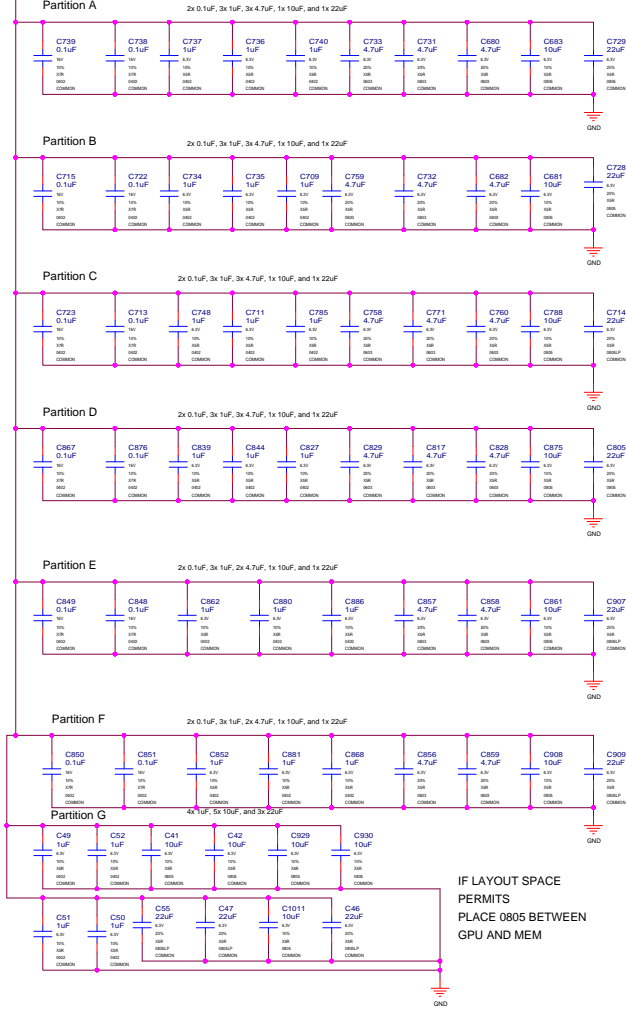
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PCB REV	PG600-B02	PAGE	18 OF 45
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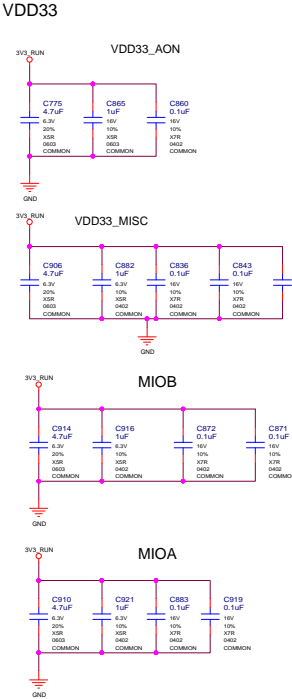
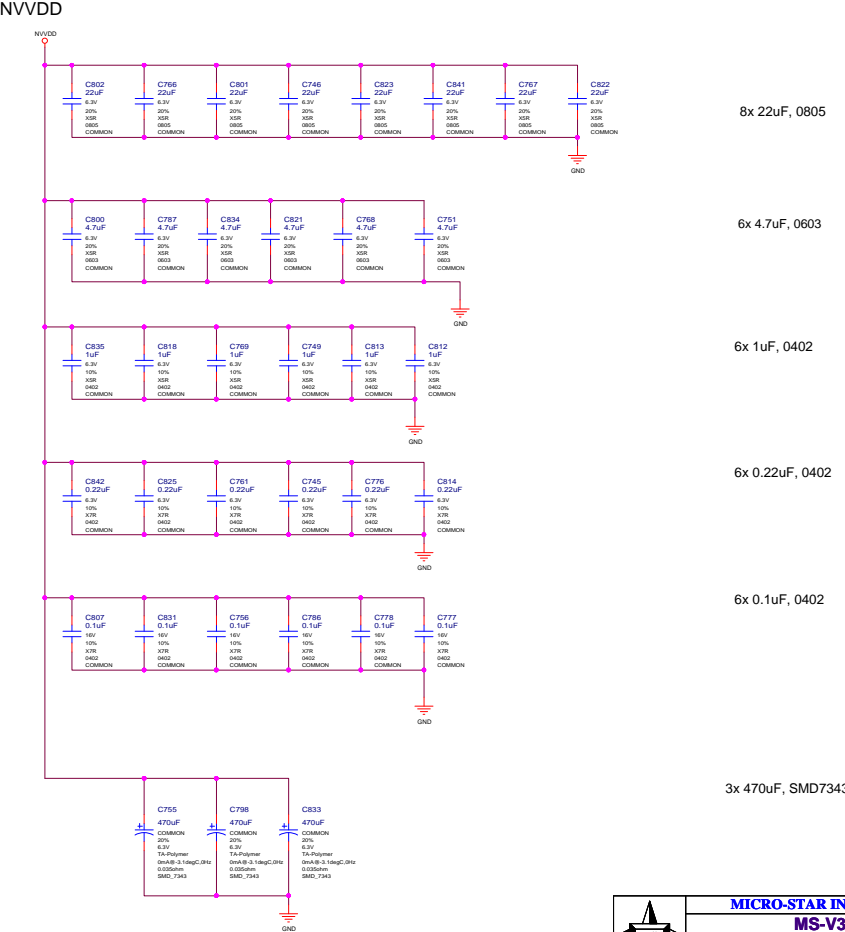
Based on GB3-X GDDR5 FBVDDQ Decap Guideline

FBVDDQ
0.1uF, 1uF, 0402 (Place Under GPU)
4.7uF, 0603 (Place Near GPU)
10uF, 0805 (Place Near GPU)
22uF, 0805 (Place Near GPU)



IF LAYOUT SPACE
PERMITS
PLACE 0805 BETWEEN
GPU AND MEM

NVVDD Decoupling caps. Place under GPU.



8x 22uF, 0805


6x 4.7uF, 0603

6x 1uF, 0402

6x 0.22uF, 0402


6x 0.1uF, 0402

3x 470uF, SMD7343



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Date	Monday, May 11, 2015	Sheet	30	of	41

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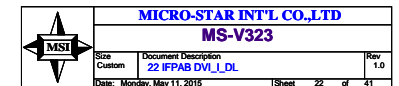
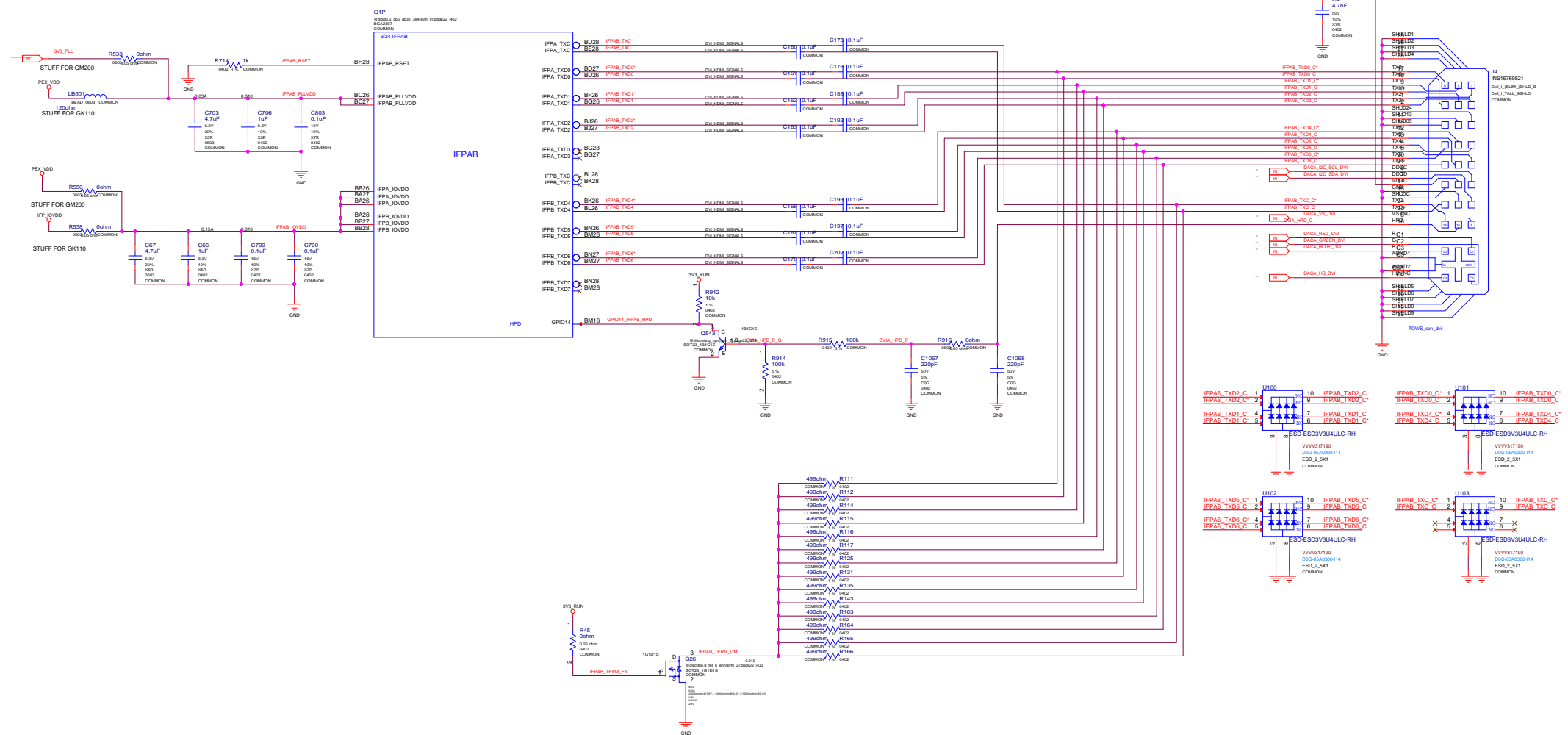
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PAGE DETAIL GPU Decoupling

REPLACE WITH ZERO OHM RESISTORS FOR KEPLER SKUs



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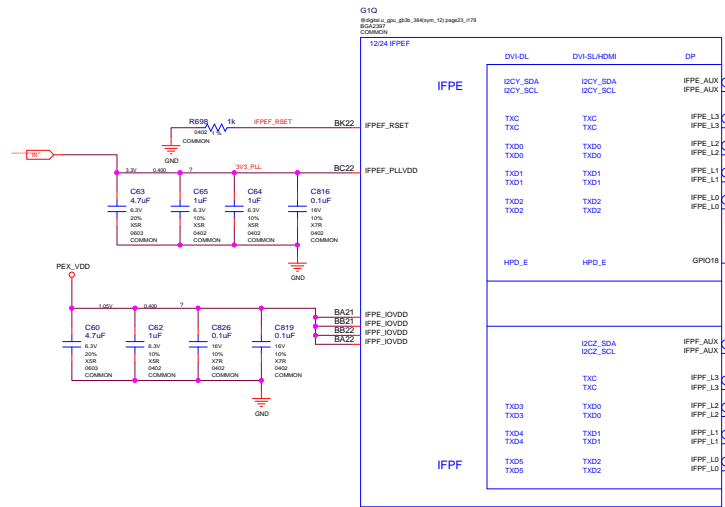
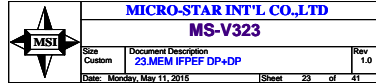
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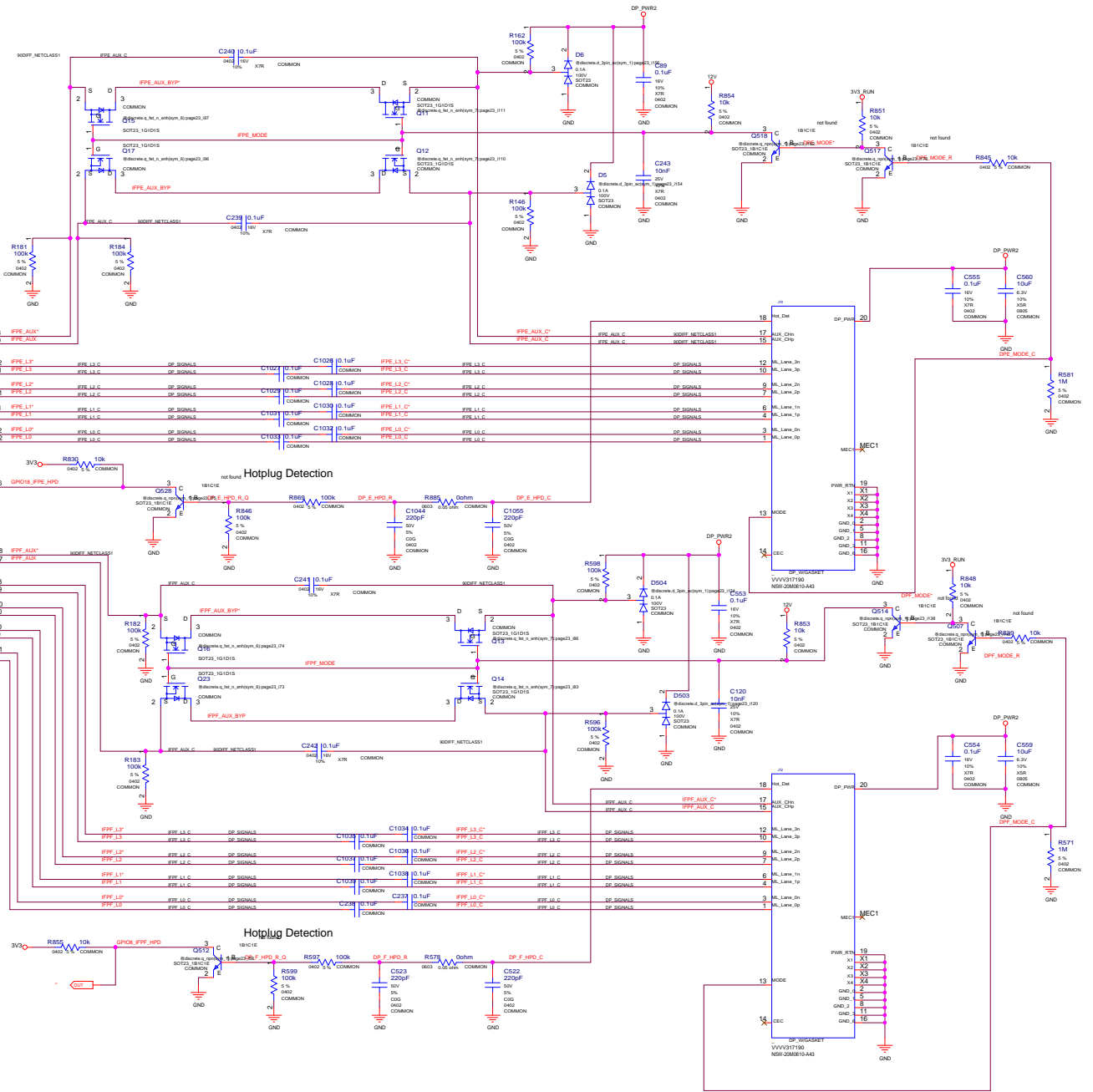
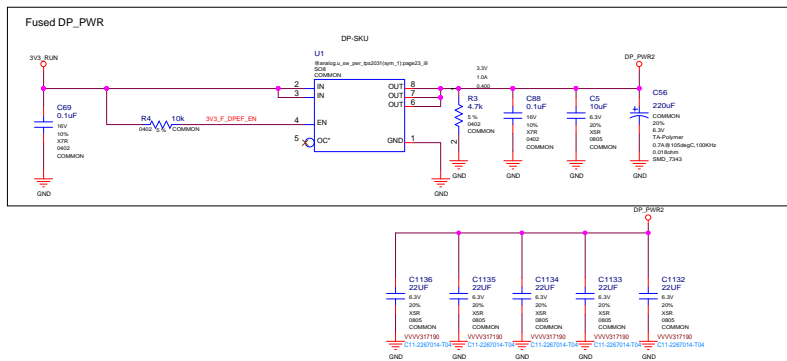
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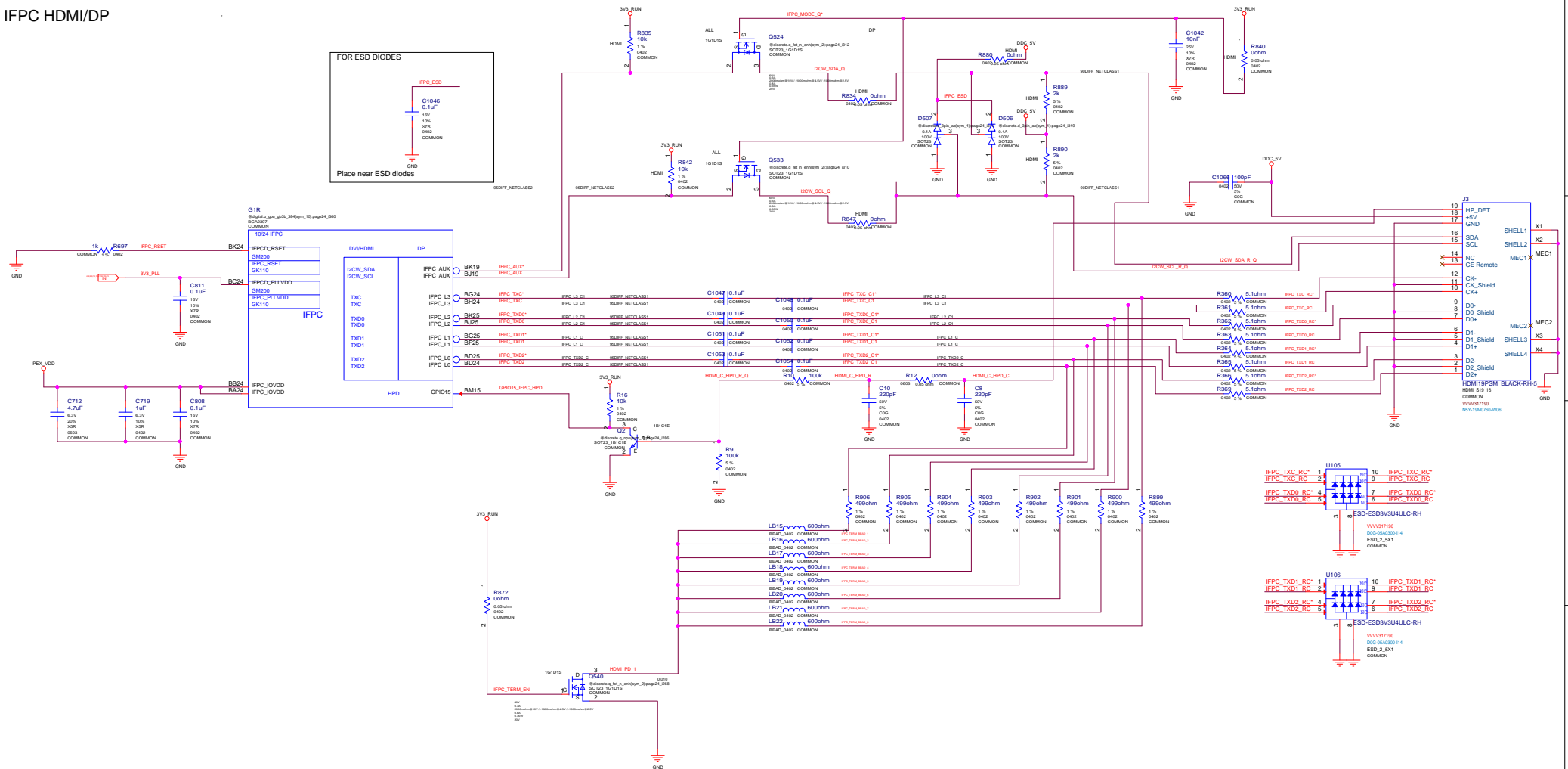
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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through





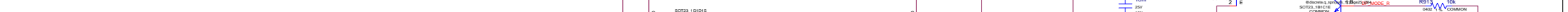
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BOM REV	A	DATE	21-APR-2015

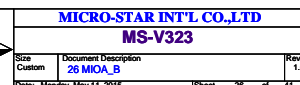
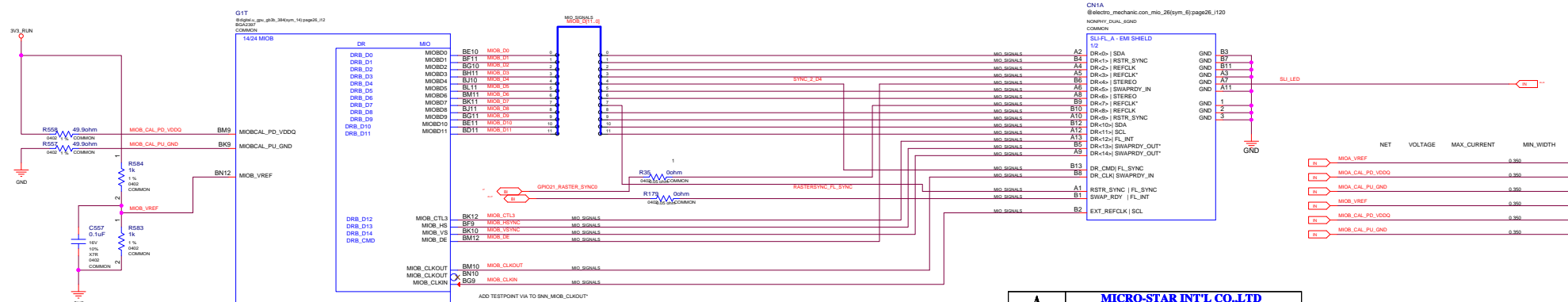
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PAGE DETAIL	IFPC HDMI / DP

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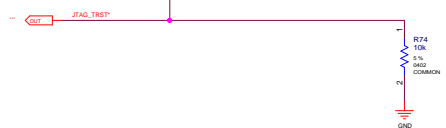


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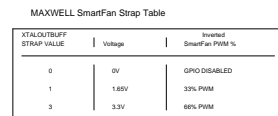


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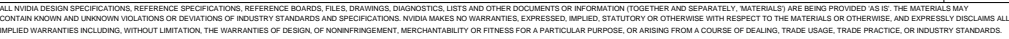
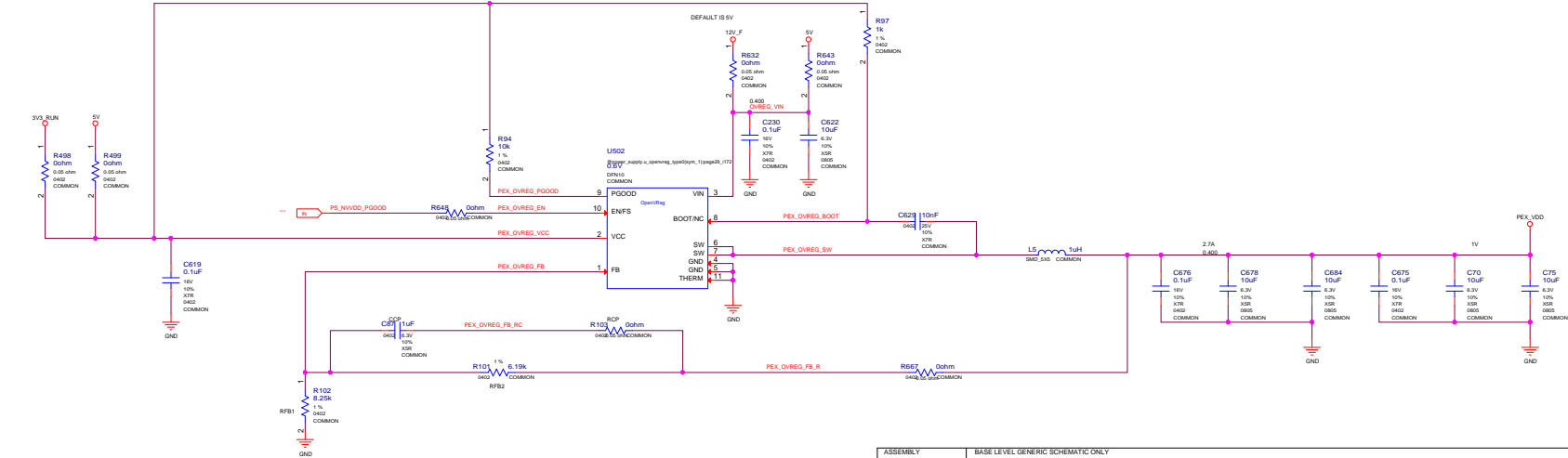
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	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

x16 DENSITY MODE STRAPS	
CFG[3:0] Config	Width Vendor
0000	Reserved
0001	256Mx16 384-bit Elpida
0010	256Mx16 384-bit Hynix
0011	256Mx16 384-bit Hynix
0100	128Mx16 384-bit Hynix B
0101	128Mx16 384-bit Elpida
0110	128Mx16 384-bit Hynix
0111	128Mx16 384-bit Samsung
1000	Reserved
1001	256Mx16 320-bit Elpida
1010	256Mx16 320-bit Hynix
1011	256Mx16 320-bit Samsung
1100	128Mx16 320-bit Hynix B
1101	128Mx16 320-bit Elpida
1110	128Mx16 320-bit Hynix
1111	128Mx16 320-bit Samsung

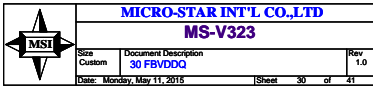
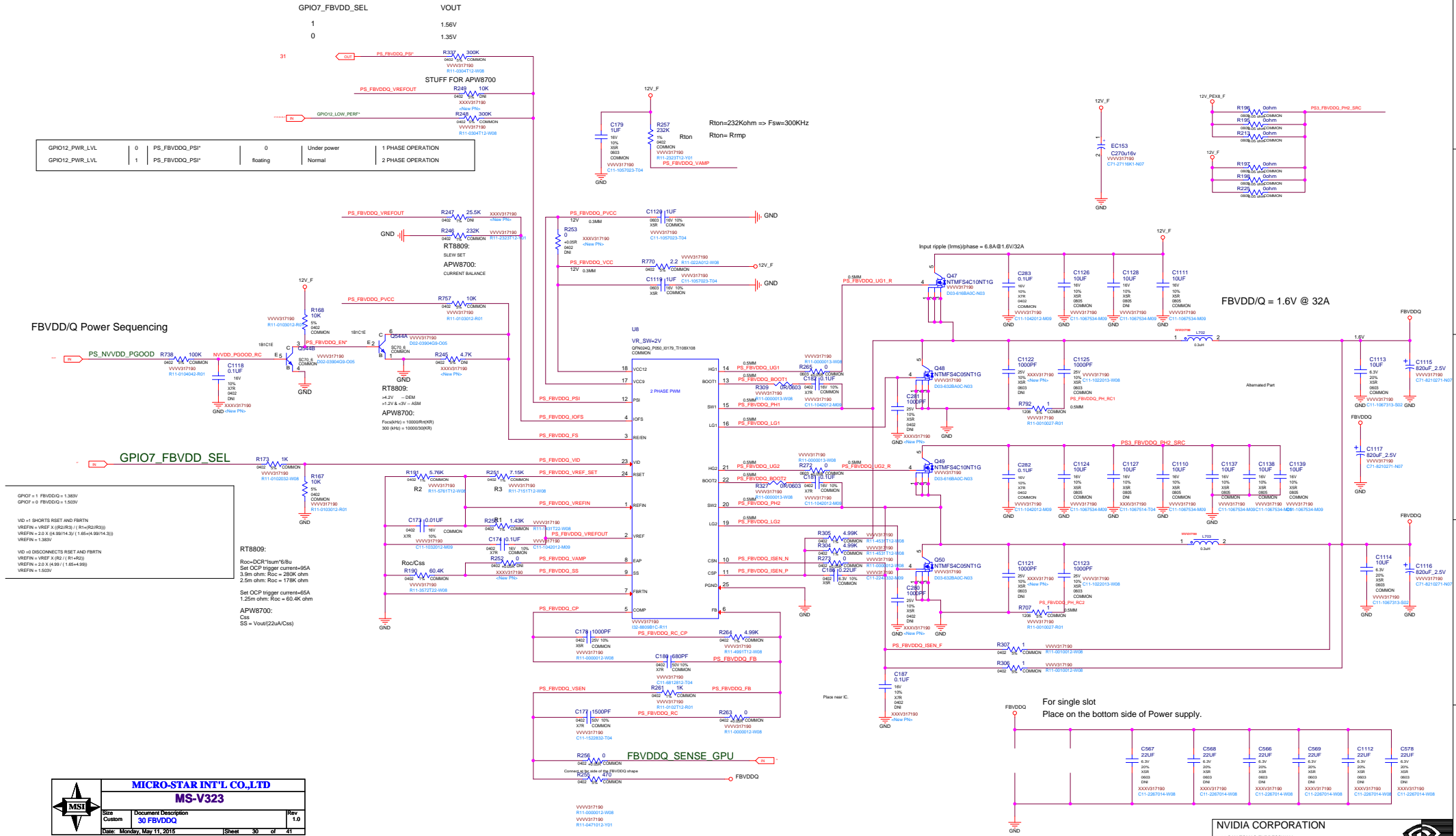


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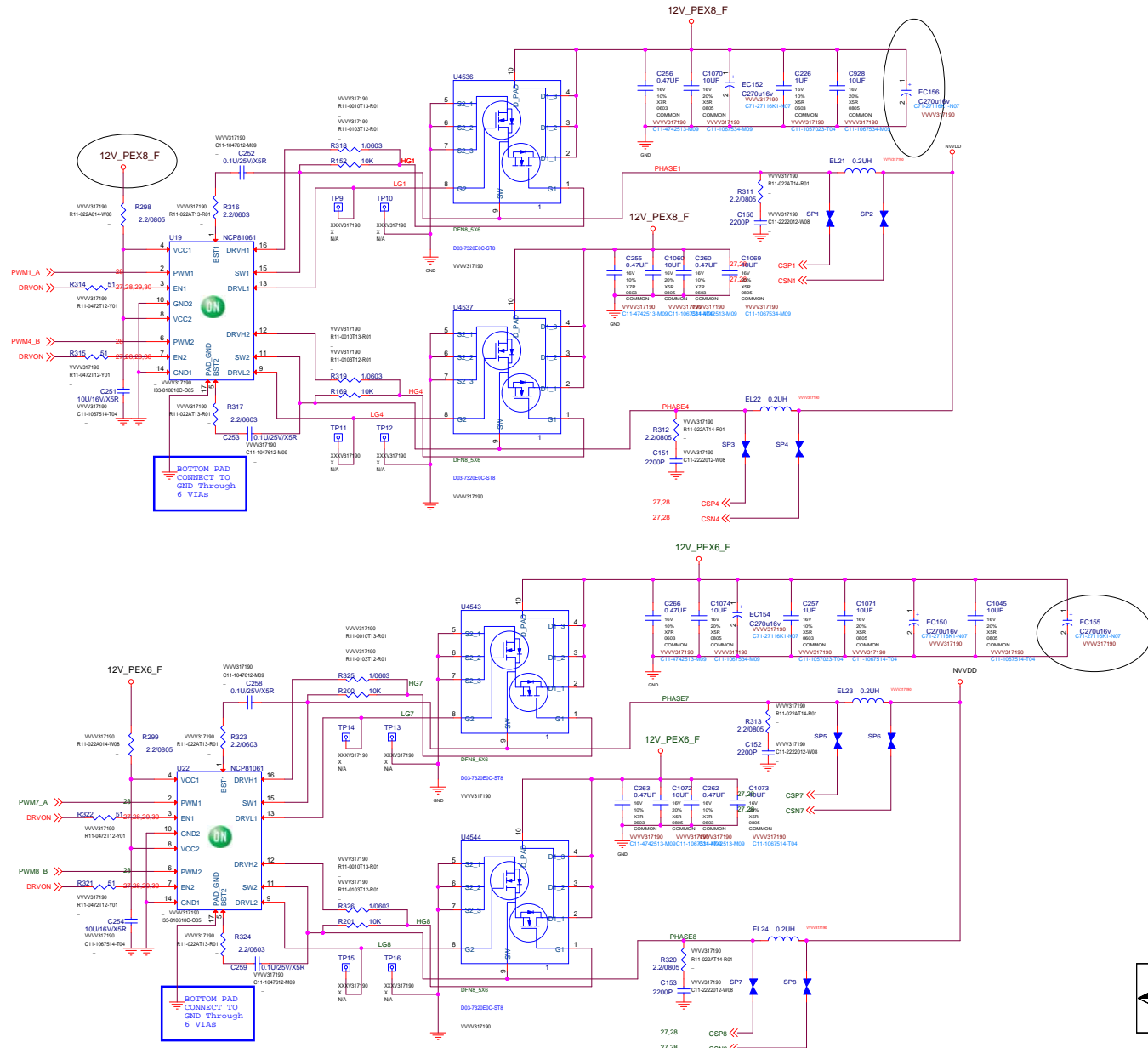


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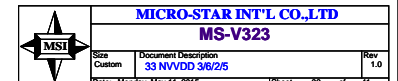
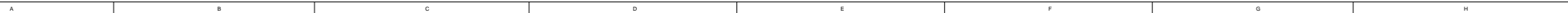
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Company: QIP
US
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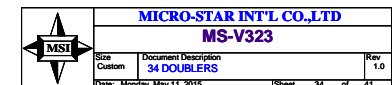
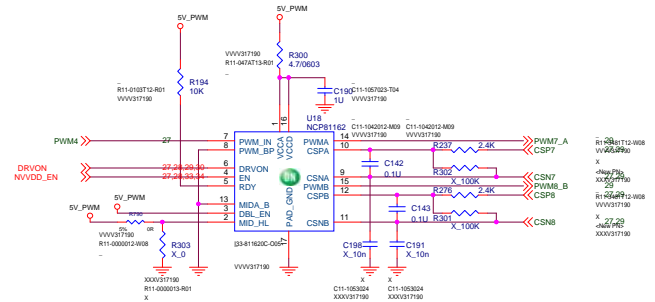
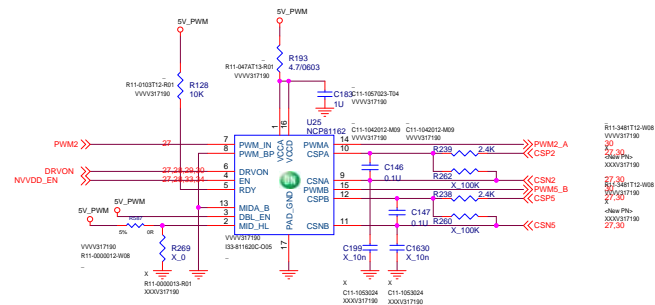


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PAGE DETAIL	PS: NVVDD Phase 5,6

VID Table

GPI04 VID_5	GPI03 VID_4	GPI02 VID_3	GPI01 VID_2	GPI00 VID_1	VOUT
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	1	0	1	0.8875V
1	1	0	1	1	0.8750V
1	1	1	1	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V



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Page36: PS: Inputs, Filtering, and Monitoring

REMOVE NO STUFF FOR GEFORCE SKUS ONLY

PEX 3V3 INPUT - 10W

DEFAULT STUFFING IS THE BEAD.
IN CASE INDUCTOR NEEDS TO BE
STUFFED YOU NEED TO MAKE
SURE THAT ITS LOWER HEIGHT THAN 2.7MM

3V3_FILTER CONNECTS TO 3V3_RUN.
VIA CIRCUITRY FOUND ON THE MCU PAGE.
USING EITHER THE FET LABELED Qx OR
RESISTORS LABELED Rj and Rk

PEX_12V INPUT - 66W

Alternate

CHK_D2_TX7
L04-65A732T-LB5

CHK_D2_TX7
L04-65A732T-LB5

L162 CO LAYOUT
L1 STUFFED FOR DESKTOP
L2 STUFFED FOR 24x EAST CONNECTOR STUFFED

PEX8 INPUT 2 - 2x4 PCIE CON 150W

CHK_D2_TX7
L04-65A732T-LB5

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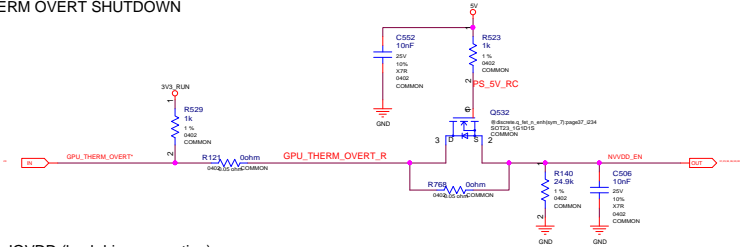
NV_PN 600-1G600-BASE-QS1

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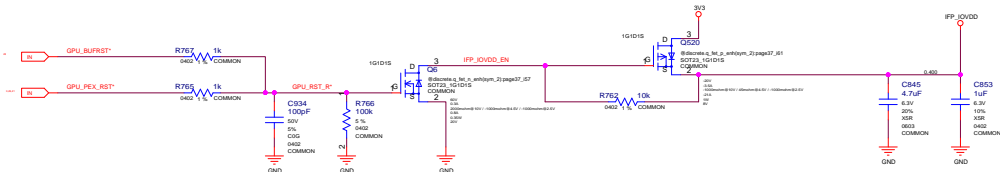
ASSEMBLY	PS: Inputs, Filtering, and Monitoring
PAGE DETAIL	

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THERM OVERT SHUTDOWN



IFP_IOVDD (backdrive prevention)





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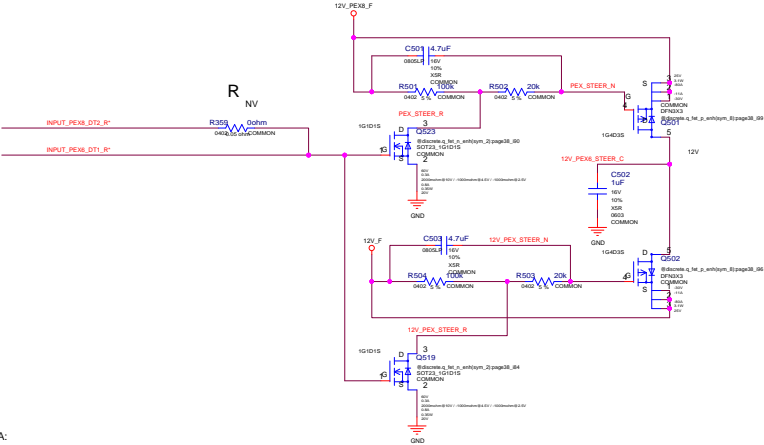
DATE 21-APR-2015

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ASSEMBLY BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL PS: Shutdown

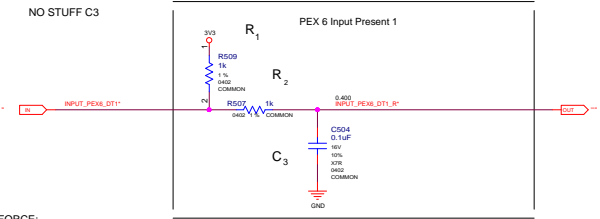
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

For Open/Reg Type4 + Phase Doubler, 2 phase PSI mode



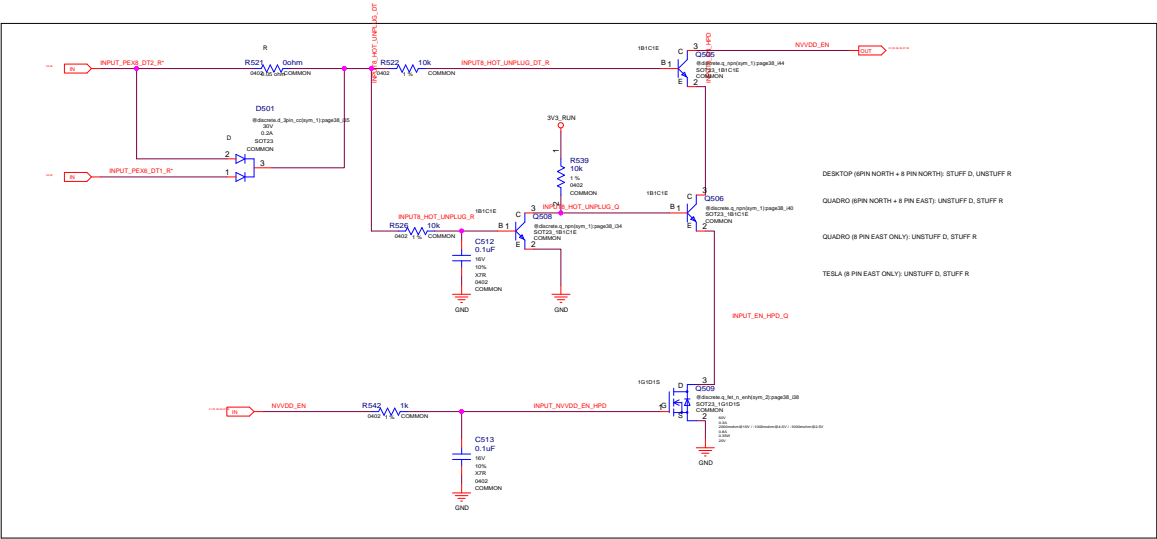
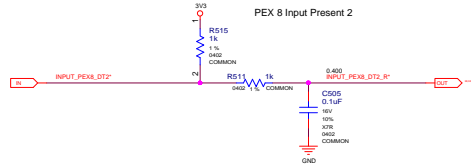
QUADRO/TESLA:

- PEX 6 INPUT CONNECTOR IS NOT LOADED
- PEX 6 INPUT DETECT MUST BE DISABLED
- PEX 8 INPUT DETECT MUST BE USED TO CONTROL STEERING
- STUFF Rnv IN STEERING CIRCUIT
- NO STUFF R1
- NO STUFF R2
- NO STUFF C3

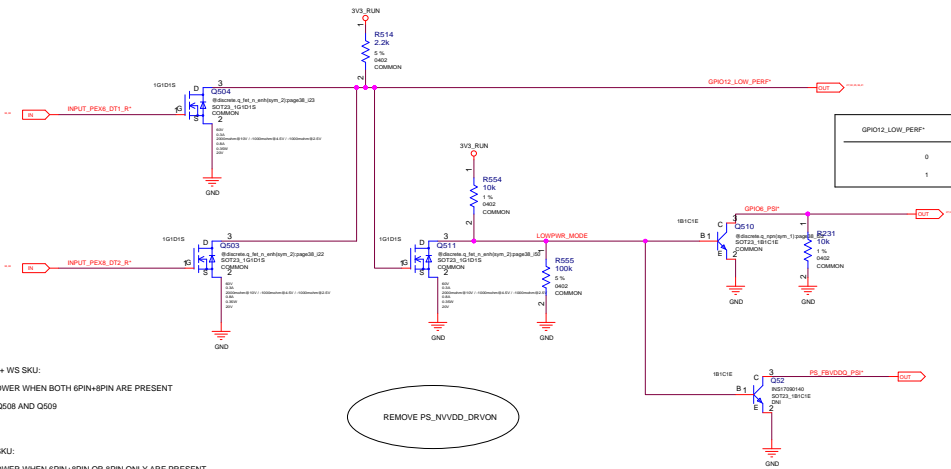


GeFORCE:

- PEX 6 INPUT CONNECTOR IS LOADED
- PEX 6 INPUT DETECT MUST BE USED TO CONTROL STEERING
- NO STUFF Rnv IN STEERING CIRCUIT
- STUFF R1
- STUFF R2
- STUFF C3



PEX Input - Under Power Boot Controls



- DT SKU + WS SKU:
FULL POWER WHEN BOTH 6PIN+6PIN ARE PRESENT
STUFF Q508 AND Q509
- TESLA SKU:
FULL POWER WHEN 6PIN+6PIN OR 6PIN ONLY ARE PRESENT
STUFF Q508 ONLY



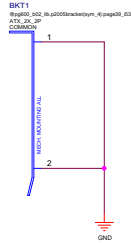
MICRO-STAR INT'L CO.,LTD		
MS-V323		
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Brackets:

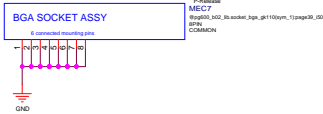
DVIDVI_HDMI_DP_151-10001-0441-092



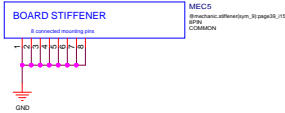
Bracket Screw

MEC1
@mechanical_mounting_1,1 page39_13
DTS
COMMON
New LP screw - 155-0001-000
RDS screw - 155-0000-000

GPU SOCKET



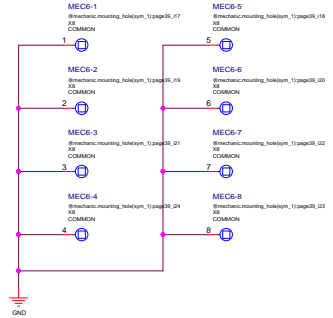
GPU Stiffener (BRING-UP COOLER)



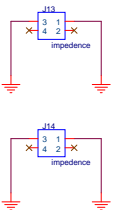
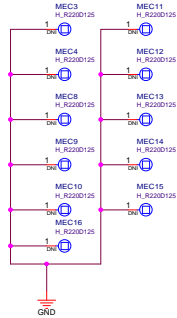
Stiffener



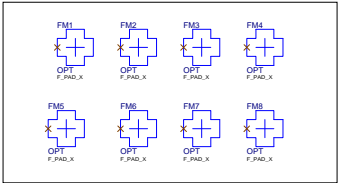
Bring Up Cooler



Mechanical Holes Symbol



HDMI_FEE
HDMI_FEE
COMMON
V1017055
V01-RDM03-000



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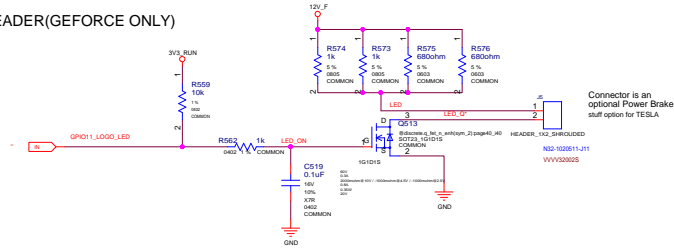
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LED HEADER(GEFORCE ONLY)

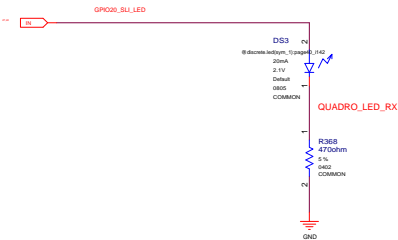


Remove Bypass filter option

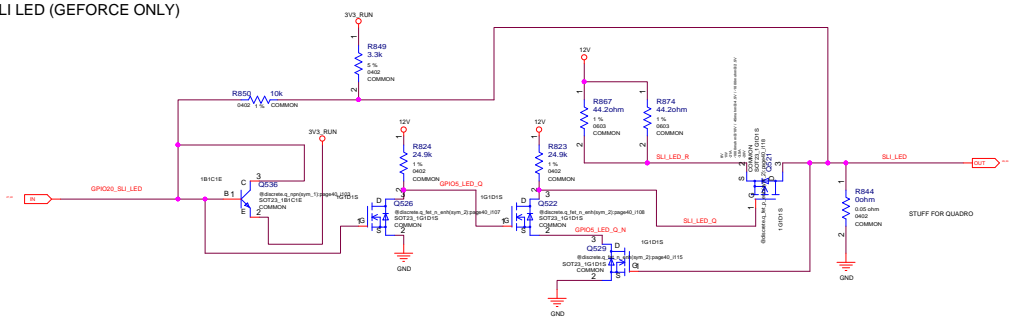
USING GPIO5 TO DIM
GEFORCE AND SLI LED



LED FOR QUADRO
PLACE BETWEEN DP Connectors
CONNECTORS



SLI LED (GEFORCE ONLY)



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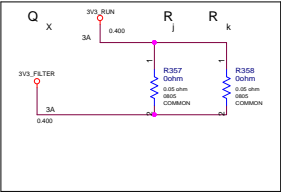
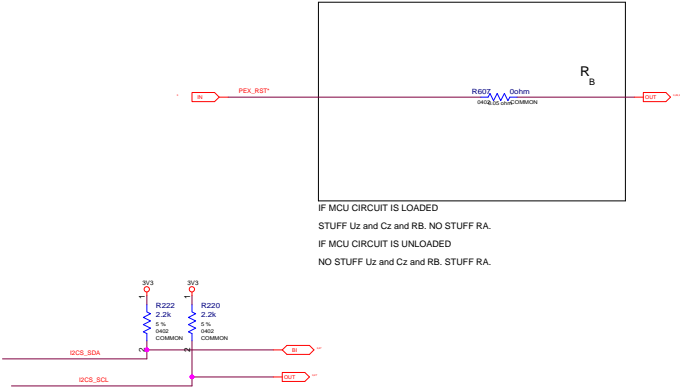
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