



# TU102-300 GPU

NPN-09107-001\_v01 | July 2018

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New Product Notice

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Gigabyte Desktop 2018-08-12 23:52:28

# New Product Notice

NPN-09107-001\_v01

New Product Introduction			
This NPN specifies the following new NVIDIA® TU102-300 GPU. This GPU is offered in the GB4-384 (2824-ball BGA, 47.5 mm × 47.5 mm) package only.			
<b>Notification</b>	July 2018	<b>Planned Implementation</b>	Now

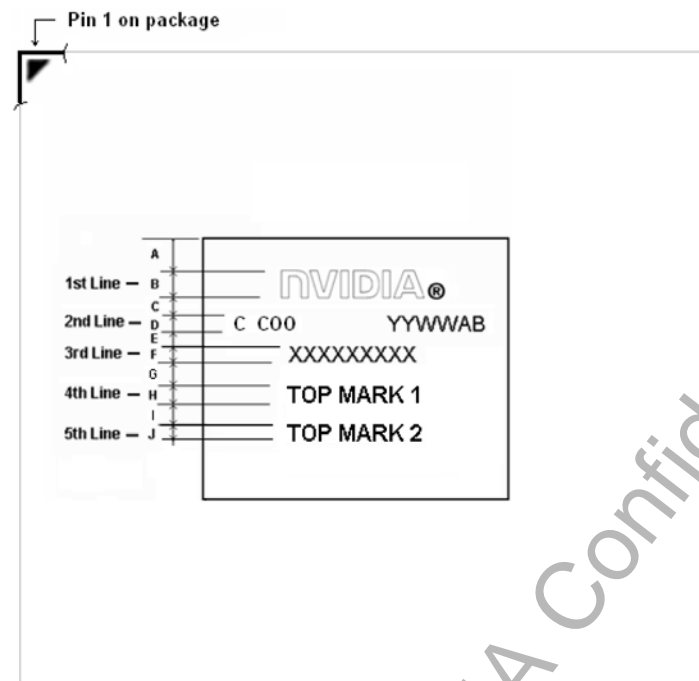
Product Information	
These new products represent the ultimate Enthusiast consumer desktop GPU. They are based on the new NVIDIA Turing graphics architecture and will be manufactured using qualified suppliers per our approved suppliers' list and are RoHS and Halogen-free compliant.	
Key Specifications:	
	<b>TU102-300</b>
<b>Chip</b>	TU102-300-Kx-A1
<b>Device ID</b>	0x1E04
<b>Memory interface</b>	352-bit GDDR6
<b>Package</b>	GB4-384

Impact of Change and Recommended Action
NVIDIA is committed to providing our customers with quality products that push the edge of technology and at the same time enable product segmentation. To help guarantee a rapid time-to-market launch and smooth and uninterrupted product supply, NVIDIA strongly recommends that customers qualify these GPUs as soon as possible.

Forecasted Key Milestones
TU102-300-Kx-A1: OS..... August 4, 2018
TU102-300-Kx-A1: Production..... September 4, 2018

## Product Marking and Traceability

### TU102-300 Markings



Pin 1: Location of Pin 1 in upper left when reading the marking.

Line 1: Company Name

Line 2: Assembly information: plant identifier (C) and country of origin (COO):

- C = Plant identifier: A (ASE), B (Amkor K5), K (Amkor K4), R (ATT - Amkor Tech), S (SPIL), T (TSMC).

- COO = Country of origin: Taiwan for ASE, ATT, SPIL and TSMC, and Korea for Amkor K4 and Amkor K5.

- YYWW = Assembly date code
- AB = Mask revision

Line 3: Assembly lot number (XXXXXXXX).

The first character identifies the wafer Fab location:

- P = TSMC Fab 14

Line 4: Product Part Number, for example: XXXXX-XX-XX

Line 5: <BLANK>

### Products Affected/Ordering Codes

Product	NVIDIA Part Number <sup>1</sup>	Marketing Part Number for P.O.	Comments
TU102-300	TU102-300-K1-A1	TU102-300-K1-A1	47.5 mm × 47.5 mm 2824-ball BGA (GB4-384)
TU102-300	TU102-300-K2-A1	TU102-300-K2-A1	47.5 mm × 47.5 mm 2824-ball BGA (GB4-384)
TU102-300	TU102-300-K3-A1	TU102-300-K3-A1	47.5 mm × 47.5 mm 2824-ball BGA (GB4-384)
TU102-300	TU102-300-K4-A1	TU102-300-K4-A1	47.5 mm × 47.5 mm 2824-ball BGA (GB4-384)
TU102-300	TU102-300-K5-A1	TU102-300-K5-A1	47.5 mm × 47.5 mm 2824-ball BGA (GB4-384)
TU102-300	TU102-300-K6-A1	TU102-300-K6-A1	47.5 mm × 47.5 mm 2824 ball BGA (GB4-384)

#### Note:

<sup>1</sup> The NVIDIA part number is provided in this document as a reference for product shipping and handling at factory. This part number is NVIDIA confidential.

### Revision History

Version	Date	Authors	Description of Change
01	July 24, 2018	QL, DR	Initial release

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# TU102 Graphics Processing Unit

DS-08839-001\_v01 | August 2018  
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## Data Sheet

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## DOCUMENT CHANGE HISTORY

DS-08839-001\_v01

Version	Date	Authors	Description of Change
01	August 10, 2018	RT, DR	Initial Release

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# 1 INTRODUCTION

## Overview

The Graphics Processing Unit (GPU) covered in this data sheet is designed using a new architecture to bring a new level of performance to visual graphics and computing software applications. This GPU fully integrates hardware acceleration for both graphics and computing code enabling hardware acceleration of a wider class of software applications than ever before.

The NVIDIA® TU102 GPU is fabricated using TSMC 12FFB process technology to provide maximum performance. The TU102 GPU supports GDDR6 memories.

## Features and Technologies

The TU102 family of GPUs supports the following features and technologies:

- ▶ Direct3D 12 and Shader Model 7.0
- ▶ OpenGL 4.5
- ▶ Vulkan 1.0
- ▶ NVIDIA® Ageia PhysXTM technology
- ▶ NVIDIA® CUDA technology

## Memory Support

The TU102 GPU supports a 384-bit frame buffer memory interface using GDDR6 memories.

## Display

Key display features include:

- ▶ Four display pipelines for quad independent display
- ▶ Pipeline pixel depth 12 bits per each color
- ▶ HDMI version: 2.0b
  - Full backwards compatibility with HDMI 1.x
- ▶ DisplayPort (DP) version: 1.4a
- ▶ DVI I and DVI D: Dual-link resolution of  $2560 \times 1600 \times 24$  bpp at 60 Hz refresh rate
- ▶ USB-C

## Digital Audio

Digital audio features include:

- ▶ Support for HD Audio over PCI Express
- ▶ Data rates of 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz, 176 KHz, and 192 KHz with HDMI. Only 48 KHz supported over DP.
- ▶ Word sizes of 16-bit, 20-bit, and 24-bit

## Video

The TU102 GPU introduces a new video engine, which is backward compatible with the video engine in earlier GPUs.

The following video formats are supported:

► Decode

- H264 (MPEG4 AVC)
- H265 (HEVC)
- VP9
- MVC
- MV-HEVC
- MPEG2
- MPEG4 ASP
- VP8
- VC1

► Encode

- H264 (MPEG4 AVC)
- H265 (HEVC)
- MVC
- MV-HEVC

A full range of resolutions are supported including 2160p, 1080p, 1080i, 720p, 480p, and 480i. The TU102 GPUs provide hardware acceleration for the computationally intensive parts of video processing. The TU102 video processor provides improved video playback speeds via faster decode and transcode.

## PCI Express

The TU102 GPU supports PCI Express 3.0 with 16 lanes of PCIe traffic for a peak bandwidth (counting both directions) of up to 16 gigabytes (GBps) per second.

## NVLink

The TU102 GPU supports one x16 wide NVLink™2 interface, which can support up to 51.56 GB/s/direction raw bandwidth.



## GPIOs

The GPIO interface allows for basic control of devices on the graphics card.

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## Power Management Technologies

The TU102 GPU uses enhanced power management to achieve very low GPU power consumption. The following features are supported:

- ▶ ASLM and ASPM power management
- ▶ PLLs on lower voltage rails
- ▶ Dynamic memory termination
- ▶ Adaptive clocking
- ▶ Adaptive Power States

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## 2 SIGNAL DESCRIPTIONS

The signal description section contains definitions grouped under the following functions:

- ▶ Conventions
- ▶ PCI Express Interface
- ▶ NVLink Interface
- ▶ Frame Buffer Memory Interface
- ▶ ROM Access Signals
- ▶ Digital Display Interface
- ▶ USB-C Display Interface
- ▶ I2C Interface
- ▶ Clock Reference Signals
- ▶ Power Rail Signals
- ▶ Test Signals
- ▶ Miscellaneous



**Note:** For detailed functionality and usage please refer to the D18 Hardware Design Guide.

## Conventions

The following conventions are used to describe the signals for the TU102 GPU:

- ▶ Signal names listed in the ballout are written in bold *sans serif* font to distinguish them from other text. Single-ended active low signals are identified by an underscore and the letter “n” (**\_N**) after the signal. For example, **PEX\_TX1\_N** indicates an active low signal. Signal names that do not appear in the ballout, but that are used for alternate interfaces are written in *sans serif* font without bold.
- ▶ Vendor signals appear as are standard for the vendor data sheets. For instance,  $\overline{\text{CAS}}$  represents the active low Column Address Strobe signal in the frame buffer memory interface.
- ▶ I/O Type  
The signal I/O state is represented as a code to indicate the operational characteristics of the signal. Table 2.1 lists the I/O codes used in the signal description tables.

**Table 2.1 I/O Codes for Signal Descriptions**

I/O Code	Meaning
I	Input signal
I/O	Input/output signal
O	Output signal
P	Power/ground
AI	Analog input
AO	Analog output

## PCI Express Interface

The PCI Express Interface signals are given in Table 2.2.

**Table 2.2 PCI Express Interface**

Signal	I/O	Description
PEX_RX[15:0] PEX_RX[15:0]_N	I	<p>PCI Express Receive Data Bus</p> <p>This is the high-speed unidirectional differential input data bus. The raw data rate is 2.5 Gbps per differential pair for PCI Express 1.1, 5.0 Gbps for PCI Express 2.0, 8.0 Gbps for PCI Express 3.0, including the symbol overhead for an embedded clock.</p>

Table 2.2 PCI Express Interface

Signal	I/O	Description
PEX_TX[15:0] PEX_TX[15:0]_N	O	<p>PCI Express Transmit Data Bus</p> <p>This is the high-speed unidirectional differential output data bus. The raw data rate is 2.5 Gbps per differential pair for PCI Express 1.1, 5.0 Gbps for PCI Express 2.0, 8.0 Gbps for PCI Express 3.0, including the symbol overhead for an embedded clock.</p>
PEX_REFCLK PEX_REFCLK_N	I	<p>PCI Express Reference Clock</p> <p>The reference clock is a differential low-jitter input the GPU uses for its internal timing purposes. This input clock may be spread spectrum. Refer to the latest PCI Express specification for details on the reference clock spread spectrum.</p>
PEX_RST_N	I	<p>PCI Express Reset</p> <p>The PEX_RST_N signal indicates when the power supply is within its specified voltage tolerance and is stable. It goes inactive after a delay time from the power rails, achieving specified tolerance and power up. Refer to the latest PCI Express specification for details on the PCI Express reset.</p>
PEX_TERM_P	AB	<p>PCI Express Input/Output Termination Calibration</p> <p>The PEX_TERM_P signal provides the reference for the internal calibration of the PCI Express input/output termination. Use a pull-down to GND that is the same value as the desired termination.</p>
PEX_CLKREQ_N	O	<p>PCI Express Clock Request</p> <p>This active low signal is driven to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data.</p>
PEX_WAKE_N	I/O	<p>PCI Express Wake Request</p> <p>This active low signal is driven to request that the PCI Express interfaces wakes up from a lower power state.</p>

## NVLink Interface

The NVLink Interface signals are given in Table 2.3.

Table 2.3 NVLink Interfaces

Signal	I/O	Description
NVHSx_RX[7:0] NVHSx_RX[7:0]_N (x=0,1)	I	NVLink Receive Data Bus This is the high-speed unidirectional differential input data bus. The raw data rate is 2.5 Gbps per differential pair.
NVHSx_TX[7:0] NVHSx_TX[7:0]_N (x=0,1)	O	NVLink Receive Data Bus This is the high-speed unidirectional differential input data bus. The raw data rate is 2.5 Gbps per differential pair.
NVHS_REFCLK NVHS_REFCLK_N	I	NVLink Reference Clock The reference clock is a differential low-jitter input the GPU uses for its internal timing purposes. Refer to the latest NVIDIA NVLink specification for details.
NVHSx_TERM (x=0)	AO	NVLink Input/Output Termination Calibration The <b>NVHSx_TERM</b> signal provides the reference for the internal calibration of the NVLink input/output termination. Refer to the NVIDIA Hardware Design Guide for the recommended resistor value.



## Frame Buffer Memory Interface

The TU102 frame buffer memory interface supports GDDR6 memories. Each memory partition has its own set of command signals. To see how the frame buffer control signals map to the memory command signals, refer to the Hardware Design Guide.

Table 2.4 and Table 2.5 describes the data and clock signals for each memory partition.

**Table 2.4 Frame Buffer Command Interface for GDDR6**

Signal	I/O	Description
FBx_CMD[35:0] (x = A,B,C,D,E,F)	O	Command Address Bus Inversion (CABI_n) Used to reduce power consumption on the command Address bus.
	O	Reset (RESET_n) Asynchronous DRAM reset signal
	O	Memory Clock Enable (CKE_n) Enables the clock receivers for the target RAM.
	O	Command Address Inputs ( CA[9:0] ): The CA inputs receive DDR Command and Address inputs

Table 2.5 Frame Buffer Interface

Signal	I/O	Description
<b>FBx_CLK[1:0]</b> <b>FBx_CLK[1:0]_N</b> (x=A,B,C,D,E,F)	0	<b>Memory Clock Signals</b> These are separate sets of clock signals for each memory partition. For a further reduction in loading, there are two sets of clocks per partition. Each partition has two clock pairs that control either the most significant 32 bits or the least significant 32 bits per partition. The active low CA signals switch on the falling clock edge. The active high CA signals switch on the rising clock edge. The memory clock signals are as follows: <b>FBx_CLK0 and FBx_CLK0_N → FBx_D[31:0]</b> <b>FBx_CLK1 and FBx_CLK1_N → FBx_D[63:32]</b> <b>x= A,B,C,D,E,F</b>
<b>FBx_D[63:0]</b> (x=A,B,C,D,E,F)	I/O	<b>Memory Data Bus</b> These signals connect to data signals of the memory device for each 64-bit partition.
<b>FBx_DQM[7:0]</b> (x=A,B,C,D,E,F)	I/O	<b>Data Bus Inversion ( DBI )</b> <b>FBx_DQM[7:0]</b> signals are connected to DBI[7:0] signals of the memory. Used to reduce power consumption and VDD noise of the DRAM.
<b>FBx_DQS_WP[7:0]</b> (x=A,B,C,D,E,F)	1	<b>Error Detection Code ( EDC )</b> <b>FBx_DQS_WP[7:0]</b> signals are connected to the EDC[7:0] signals of the memory. The CRC data is communicated on these signals

Table 2.5 Frame Buffer Interface

Signal	I/O	Description
FBx_WCK01 FBx_WCK01_N FBx_WCK23 FBx_WCK23_N FBx_WCK45 FBx_WCK45_N FBx_WCK67 FBx_WCK67_N (x=A,B,C,D,E,F) FBx_WCKB01 FBx_WCKB01_N FBx_WCKB23 FBx_WCKB23_N FBx_WCKB45 FBx_WCKB45_N FBx_WCKB67 FBx_WCKB67_N (x=A,B,C,D,E,F)	O	Differential clocks used as the reference for read and write data latching.
FB_CAL_PD_VDDQ FB_CAL_PU_GND	AO	Calibration Pull-Down/Pull-Up When the frame buffer bus operates in high-speed source-synchronous mode, several signals require dynamic calibration. Other slower signals are calibrated once on power-up. <b>FB_CAL_PD_VDDQ</b> and <b>FB_CAL_PU_GND</b> are used to compute the drive strength of the frame buffer pads. <b>FB_CAL_PD_VDDQ</b> connects to <b>FBVDDQ</b> and is pulled up through a precision resistor. <b>FB_CAL_PU_GND</b> is pulled down to <b>GND</b> through a precision resistor.

Table 2.5 Frame Buffer Interface

Signal	I/O	Description
FB_CAL_TERM_GND	AO	Termination Calibration Signal When the frame buffer bus operates in high-speed source-synchronous mode, it may use internal termination provided by the GPU. This signal provides the calibration for the internal termination. It should be tied to <b>GND</b> through a precision resistor that is the same value as the desired termination.
FB_VREF	I	Frame Buffer Voltage Reference Sets switching threshold for inputs on the frame buffer when the frame buffer input pads are set to input mode. Leave as a No Connect.
FBVDDQ_SENSE	AO	Frame Buffer Power Rail Sense Signal
FBVDDQ_GND_SENSE	AO	Frame Buffer Ground Sense Signal

## ROM Access Signals

Table 2.6 Serial ROM Access Signals

Signal	I/O	Description
ROM_SCLK	O	Serial ROM Clock ROM_SCLK supplies the clock signal for accessing serial ROM data.
ROM_CS_N	O	Chip Select.
ROM_SI	O	Serial Output ROM_SI supplies the data signal to the SROM_SI serial ROM signal.
ROM_SO	I	Serial Input ROM_SO accepts the data signal input from SROM_SO of the serial ROM as input.

## Digital Display Interface

The TU102 GPUs enables Links A, B, C, D, E, and F to support DisplayPort. Links can also be configured to support DVI and HDMI.

**Table 2.7 Digital Display Interface Signals, Links A & B**

Signal	I/O	Description
IFPA_AUX_SCL/ IFPA_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link A)
IFPA_L0/IFPA_L0_N	O	DisplayPort Main Link Lane 0 (Link A)
IFPA_L1/IFPA_L1_N	O	DisplayPort Main Link Lane 1 (Link A)
IFPA_L2/IFPA_L2_N	O	DisplayPort Main Link lane 2 (Link A)
IFPA_L3/IFPA_L3_N	O	DisplayPort Main Link Lane 3 (Link A)
IFPB_AUX_SCL IFPB_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link B)
IFPB_L0/IFPB_L0_N	O	DisplayPort Main Link Lane 0 (Link B)
IFPB_L1/IFPB_L1_N	O	DisplayPort Main Link Lane 1 (Link B)
IFPB_L2/IFPB_L2_N	O	DisplayPort Main Link Lane 2 (Link B)
IFPB_L3/IFPB_L3_N	O	DisplayPort Main Link Lane 3 (Link B)
IFPAB_RESET	I/O	Set Reference Current Generate a reference current through connecting an external resistor to this signal.

Table 2.8 Digital Display Interface Signals, Links C, D, E &amp; F

Signal	I/O	Description
IFPC_AUX_SCL / IFPC_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link C)
IFPC_L0/IFPC_L0_N	O	DisplayPort Main Link Lane 0 (Link C)
IFPC_L1/IFPC_L1_N	O	DisplayPort Main Link Lane 1 (Link C)
IFPC_L2/IFPC_L2_N	O	DisplayPort Main Link Lane 2 (Link C)
IFPC_L3/IFPC_L3_N	O	DisplayPort Main Link Lane 3 (Link C)
IFPCD_RSET	I/O	Set Reference Current Generates a reference current through connecting an external resistor to this signal
IFPD_AUX_SCL/ IFPD_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link D)
IFPD_L0/IFPD_L0_N	O	DisplayPort Main Link Lane 0 (Link D)
IFPD_L1/IFPD_L1_N	O	DisplayPort Main Link Lane 1 (Link D)
IFPD_L2/IFPD_L2_N	O	DisplayPort Main Link Lane 2 (Link D)
IFPD_L3/IFPD_L3_N	O	DisplayPort Main Link Lane 3 (Link D)
IFPE_AUX_SCL/ IFPE_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link E)
IFPE_L0/IFPE_L0_N	O	DisplayPort Main Link Lane 0 (Link E)
IFPE_L1/IFPE_L1_N	O	DisplayPort Main Link Lane 1 (Link E)
IFPE_L2/IFPE_L2_N	O	DisplayPort Main Link Lane 2 (Link E)
IFPE_L3/IFPE_L3_N	O	DisplayPort Main Link Lane 3 (Link E)
IFPE_RSET	I/O	Set Reference Current Generates a reference current through connecting an external resistor to this signal
IFPF_AUX_SCL/ IFPF_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link F)
IFPF_L0/IFPF_L0_N	O	DisplayPort Main Link Lane 0 (Link F);



Table 2.8 Digital Display Interface Signals, Links C, D, E &amp; F

Signal	I/O	Description
IFPF_L1/IFPF_L1_N	O	DisplayPort Main Link Lane 1 (Link F)
IFPF_L2/IFPF_L2_N	O	DisplayPort Main Link Lane 2 (Link F)
IFPF_L3/IFPF_L3_N	O	DisplayPort Main Link Lane 3 (Link F)

The TU102 GPUs enables Links A, B, C, D, E, and F to support DisplayPort. Links can also be configured to support DVI and HDMI.

## USB-C Display Interface

Link F and IFPB\_AUX support USB-C, as described in Table 2.9.

Table 2.9 USB Interface Signals

Signal	I/O	Description
IFPF_AUX_SCL/ IFPF_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane/USB-C Sideband signals SBU1/SBU2
IFPB_AUX_SCL/ IFPB_AUX_SDA_N	I/O	Master I2C to USB-C PPC
IFPF_L0/IFPF_L0_N	O	USB3 RX+ / USB3 RX- <b>Note:</b> This signal pad is used as USB3 RX+ / USB3 RX- for USB-C interface
IFPF_L1/IFPF_L1_N	O	USB3 TX+ / USB3 TX- <b>Note:</b> This signal pad is used as USB3 TX+ / USB3 TX- for USB-C interface
IFPF_L2/IFPF_L2_N	O	USB3 TX+ / USB3 TX- <b>Note:</b> This signal pad is used as USB3 TX+ / USB3 TX- for USB-C interface
IFPF_L3/IFPF_L3_N	O	USB3 RX+ / USB3 RX- <b>Note:</b> This signal pad is used as USB3 RX+ / USB3 RX- for USB-C interface
USB_L0/USB_L0_N	O	USB3 TX+ or USB2+/USB3 TX- or USB2- <b>Note:</b> This signal pad is used as USB3 TX+/USB3 TX- for USB-C interface
USB_L1/USB_L1_N	O	USB3 RX+ or USB2+/USB3 RX- or USB2 <b>Note:</b> This signal pad is used as USB3 RX+ / USB3 RX- for USB-C interface
USB_RBIAS	AI	USB Reference Resistor
USB_SCL	I/O	Slave I2C Clock interface for controlling integrated DP/USB cross-connect
USB_SDA	I/O	Slave I2C Data interface for controlling integrated DP/USB cross-connect

Table 2.9 USB Interface Signals

Signal	I/O	Description
USB_TERMP0	AI	USB PLL Reference Resistor 0
USB_TERMP1	AI	USB PLL Reference Resistor 1

## I2C Interface

Table 2.10 I2C Interface Signals

Signal	I/O	Description
I2CB_SCL I2CB_SDA	I/O	If not used for any external Bus, this bus may be used for embedded devices.
I2CC_SCL I2CC_SDA	I/O	Restricted to embedded devices such as voltage regulators and power monitors.
I2CS_SCL I2CS_SDA	I/O	Slave I2C-Compatible Bus Signal.

## Clock Reference Signals

Table 2.11 Clock Reference Signals

Signal	I/O	Description
XTAL_IN XTAL_OUT	I O	A series resonant crystal is connected between these two points to provide the reference clock for the internal clock synthesizers. Alternately, an external LVTTTL clock oscillator output may be driven in XTAL_IN, leaving XTAL_OUT unconnected.
XTAL_OUTBUFF	O	XTAL_OUTBUFF is a buffered version of the XTAL_IN/XTAL_OUT. Used as a strap to set the fan PWM.
EXT_REFCLK_FL	I	EXT_REFCLK_FL connects to the Quadro framelock source.

## Power Rail Signals

### IFP Power Rail Signals

Table 2.12 IFP Power Rail Signals

Signal	I/O	Description
IFP_IOVDD	P	1.0V supply for integrated Digital Display I/O Power Rails for all IFP links.
IFPAB_PLLVDD	P	1.8V supply for integrated Digital Display PLL Power Rails for the IFP-A and IFP-B links.
IFPCD_PLLVDD	P	1.8V supply for Integrated Digital Display PLL Power Rails for the IFP-C and IFP-D links.
IFPE_PLLVDD	P	1.8V supply for Integrated Digital Display PLL Power Rails for the IFP-E link.

### PEX Power Rail Signals

Table 2.13 PEX Power Rail Signals

Signal	I/O	Description
PEX_CVDD / PEX_DVDD	P	1.0V supply for PCIe interface/PLL digital power rail
PEX_HVDD	P	1.8V supply for PCIe interface/PLL analog power rail
PEX_PLL_HVDD	P	1.8V supply for the PEX PLL

### Frame Buffer Power Rail Signals

Table 2.14 FrameBuffer Power Rail Signals

Signal	I/O	Description
FB_REFPLL_AVDDx (x=0,1,2)	P	1.8V supply for Frame Buffer Digital Power Rails
FBVDDQ	P	Frame Buffer Power Rail

Table 2.14 FrameBuffer Power Rail Signals

Signal	I/O	Description
FBVDDQ_SENSE	O	Frame Buffer Power Rail Sense Signal
FBx_PLL_AVDD (x=A,B,C,D,E,F)	P	1.8V supply for Frame Buffer PLL Analog Power Rails

## NVLink Rail Signals

Table 2.15 General Power Rail Signals

Signal	I/O	Description
NVHS_CVDD / NVHS_DVDD	P	1.0V supply for NVLink Internal Core Power Rail
NVHS_HVDD	P	1.8V supply for NVLink High Voltage Power Rail
NVHSx_PLL_HVDD	P	1.8V supply for NVLink PLL Power Rail

## General Power Rail Signals

Table 2.16 General Power Rail Signals

Signal	I/O	Description
GPCPLL_AVDDx (x=0,1,2)	P	1.8V supply for Analog Power Rails for GPCs
SP_PLLVDD	P	1.8V supply for Core Clock PLL Analog Power Rail
VDD	P	Core Power Rail. Connect to NVVDD power supply.
1V8_AON	P	1.8V Always On Power Rail
VID_PLLVDD	P	1.8V supply for Video Pixel Clock PLL Analog power rail
XS_PLLVDD	P	1.8V supply for Core PLL Analog rail

## USB Power Rail Signals

Table 2.17 USB Power Rail Signals

Signal	I/O	Description
USB_DVDD	P	USB 1.0V Core Power Rail
USB_HVDD	P	USB 1.8V Voltage Power Rail
USB_PLL_HVDD	P	USB 1.8V PLL Power Rail
USB_VDDP	P	USB 3.3V Analog Supply

## Test Signals

Table 2.18 Test Signals

Signals	I/O	Description
JTAG_TCK	I	JTAG Test Signals
JTAG_TDI	I	
JTAG_TDO	Z	
JTAG_TMS	I	
NVJTAG_SEL	I	JTAG Select

## Miscellaneous

Table 2.19 Miscellaneous Signals

Signal	I/O	Description
STRAP[5:0]	I	Strap Signals
THERMDP	I	Thermal Monitor Signals Leave floating and unconnected.
THERMDN	O	
ADC_IN / ADC_IN_N	I	External current sense for power monitoring
GPIO [30:0]	I	General Purpose I/O
BUFRST_N	O	Behaves as a buffered copy of the system PEX_RST* signal in all operating modes <b>when 1V8 is present</b> . Tri-state when <b>1V8 is not present</b> .
FP_FUSE_SRC	I	TBD

### 3 ELECTRICAL SPECIFICATIONS

This section provides absolute maximum ratings and operating conditions for the TU102 GPU.

For more information about the core graphics voltage (NVVDD), frame buffer clock frequency (MCLK), and core clock frequency (GPCCLK/NVCLK) values and electrical and thermal design guidelines for these products, refer to the SKU specific Electrical and Thermal Design Guidelines.

The frame buffer memory clock, MCLK, is defined as an actual clock output (not as a data rate). The NVIDIA® GPU Boost™ technology manages the clocks dynamically.

Table 3.1 lists the absolute maximum ratings of the power rails.

**Table 3.1 Absolute Maximum Ratings**

Symbol	Parameter	Min.	Max. <sup>1</sup>	Units	Notes
FBVDDQ	Frame buffer power rail	-0.3	1.98	V	
FBx_PLL_AVDD (x=A,B,C,D)	Frame buffer PLL analog power rail	-0.3	1.854	V	
GPCPLL_AVDD0 GPCPLL_AVDD1	Core PLL Analog Rails	-0.3	1.854	V	
IFP_IOVDD	Integrated Digital Display I/O power rails	-0.3	1.1	V	
IFPAB_PLLVDD	Integrated Digital Display PLL power rails	-0.3	1.854	V	



Table 3.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max. <sup>1</sup>	Units	Notes
IFPCD_PLLVDD	Integrated Digital Display PLL power rails	-0.3	1.854	V	
IFPE_PLLVDD	Integrated Digital Display PLL power rails	-0.3	1.854	V	
PEX_DVDD	PCIe interface/PLL digital power rail	-0.3	1.1	V	
PEX_HVDD	PCIe interface/PLL analog power rail	-0.3	1.854	V	
PEX_PLL_HVDD	PCIe interface PLL supply power rail	-0.3	1.854	V	
SP_PLLVDD	Core clock PLL analog power rail	-0.3	1.854	V	
VDD	Core (NVVDD) power rail	-0.3	TBD	V	
VDD_SENSE	VDD Power Plane Sense signal				
1V8_AON	1.8 V power rail	-0.3	1.854	V	
VID_PLLVDD	Thermal controller and Video pixel clock PLL analog power rail	-0.3	1.854	V	
XS_PLLVDD	Core PLL Analog Rails	-0.3	1.854	V	
T <sub>j</sub>	Die junction temperature	Refer to the Product Specification		°C	

**Notes:**

1. Stress greater than those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 3.2 lists the operating conditions of the clock and power rail signals.

**Table 3.2 Operating Conditions**

Symbol	Parameter	Min.	Typ.	Max. <sup>1</sup>	Units	Notes
FBVDDQ	Frame buffer power rail		1.25	1.35	V	Note 2
FBx_PLL_AVDD (x=A,B,C,D,E,F)	Frame buffer PLL analog power rail	1.746	1.800	1.854	V	
GPCPLL_AVDD0 GPCPLL_AVDD1	Core PLL Analog Rails	1.746	1.800	1.854	V	
IFP_IOVDD	Integrated Digital Display I/O power rails	0.97	1.00	1.03	V	
IFPAB_PLLVDD	Integrated Digital Display PLL power rails	1.746	1.800	1.854	V	
IFPCD_PLLVDD	Integrated Digital Display PLL power rails	1.746	1.800	1.854	V	
IFPE_PLLVDD	Integrated Digital Display PLL power rails	1.746	1.800	1.854	V	
PEX_DVDD/ PEX_CVDD	PCIe interface/PLL digital power rail	0.97	1.00	1.03	V	
PEX_HVDD	PCIe interface/PLL analog power rail	1.746	1.800	1.854	V	
PEX_PLL_HVDD	PCIe interface PLL supply power rail	1.746	1.800	1.854	V	
SP_PLLVDD	Core clock PLL analog power rail	1.746	1.800	1.854	V	
VDD or NVVDD	Core power rail	NVVDD -2.5%	NVVDD	NVVDD + 2.5%	V	
1V8_AON	1.8 V power rail	-0.3		1.854	V	
VID_PLLVDD	Thermal controller and Video pixel clock PLL analog power rail	1.746	1.800	1.854	V	
XS_PLLVDD	Core PLL Analog Rails	1.746	1.800	1.854	V	
T <sub>j</sub>	Die junction temperature	0	Refer to the product specific Thermal Design Guide	Refer to the product specific Thermal Design Guide	°C	See Note 3.

**Notes:**

1 This specification defines the goals for the DC supply at **VDD**. Short pulses due to switching noise on **VDD** may exceed this limit.

2 Min/Typ/Max/ should meet memory vendor spec which can vary from 1.35V to 1.55V.

3 T<sub>j</sub> is the maximum die temperature at which the GPU can operate at its maximum clock frequencies, as defined in the NVIDIA Product Specification.

Table 3.3 GPIO Electrical Specifications

Voh,Vih/min	Voh,Vih/max	Vol,Vil/min	Vol,Vil/max	Vi_mid max	Vi_mid min
1.50V	1.854V	0V	0.3V	1.3V	0.5V

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## 4 MASTER SIGNAL LIST

This chapter contains the master signal list for the TU102 GPU.

**Table 4.1 Master Signal List**

Master Signal List for TU102 GPU					
<b>IOB Key:</b> B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z= Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		<b>Reset &amp; Initial Value Key:</b> Z= Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
<b>I2C</b>					
I2CB_SCL	O			+1.8V_AON	
I2CB_SDA	B			+1.8V_AON	
I2CC_SCL	O			+1.8V_AON	
I2CC_SDA	B			+1.8V_AON	
I2CS_SCL	O			+1.8V_AON	
I2CS_SDA	B			+1.8V_AON	
<b>IFP</b>					
IFPA_L0_N	O				
IFPA_L0	O				
IFPA_L1_N	O				
IFPA_L1	O				
IFPA_L2_N	O				
IFPA_L2	O				
IFPA_L3_N	O				
IFPA_L3	O				
IFPB_L0_N	O				

Table 4.1 Master Signal List

Master Signal List for TU102 GPU					
<b>IOB Key:</b> B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z = Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		<b>Reset &amp; Initial Value Key:</b> Z= Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
IFPB_L0	O				
IFPB_L1_N	O				
IFPB_L1	O				
IFPB_L2_N	O				
IFPB_L2	O				
IFPB_L3_N	O				
IFPB_L3	O				
IFPAB_RSET	AI				
IFPC_L0_N	O				
IFPC_L0	O				
IFPC_L1_N	O				
IFPC_L1	O				
IFPC_L2_N	O				
IFPC_L2	O				
IFPC_L3_N	O				
IFPC_L3	O				
IFPD_L0_N	O				
IFPD_L0	O				
IFPD_L1_N	O				
IFPD_L1	O				
IFPD_L2_N	O				
IFPD_L2	O				
IFPD_L3_N	O				
IFPD_L3	O				
IFPCD_RSET	AI				
IFPE_L0_N	O				
IFPE_L0	O				
IFPE_L1_N	O				
IFPE_L1	O				
IFPE_L2_N	O				
IFPE_L2	O				
IFPE_L3_N	O				
IFPE_L3	O				
IFPF_L0_N	O				
IFPF_L0	O				
IFPF_L1_N	O				
IFPF_L1	O				
IFPF_L2_N	O				
IFPF_L2	O				

Table 4.1 Master Signal List

Master Signal List for TU102 GPU					
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Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
IFPF_L3_N	O				
IFPF_L3	O				
IFPE_RSET	AI				
IFPA_AUX_SCL	O				
IFPA_AUX_SDA_N	B				
IFPB_AUX_SCL	O				
IFPB_AUX_SDA_N	B				
IFPC_AUX_SCL	O				
IFPC_AUX_SDA_N	B				
IFPD_AUX_SCL	O				
IFPD_AUX_SDA_N	B				
IFPE_AUX_SCL	O				
IFPE_AUX_SDA_N	B				
IFPF_AUX_SCL	O				
IFPF_AUX_SDA_N	B				
IFPAB_PLLVDD	P				
IFP_IOVDD	P				
IFPCD_PLLVDD	P				
IFPE_PLLVDD	P				
IFPE_PLLVDD	P				
Frame Buffer A					
FBA_D[63:0]	B			FBVDDQ	
FBA_DQM[7:0]	B			FBVDDQ	
FBA_DQS_WP[7:0]	I			FBVDDQ	
FBA_WCK01	O			FBVDDQ	
FBA_WCK01_N	O			FBVDDQ	
FBA_WCKB01	O			FBVDDQ	
FBA_WCKB01_N	O			FBVDDQ	
FBA_WCK23	O			FBVDDQ	
FBA_WCK23_N	O			FBVDDQ	
FBA_WCKB23	O			FBVDDQ	
FBA_WCKB23_N	O			FBVDDQ	
FBA_WCK45	O			FBVDDQ	
FBA_WCK45_N	O			FBVDDQ	
FBA_WCKB45	O			FBVDDQ	
FBA_WCKB45_N	O			FBVDDQ	
FBA_WCK67	O			FBVDDQ	
FBA_WCK67_N	O			FBVDDQ	
FBA_WCKB67	O			FBVDDQ	

Table 4.1 Master Signal List

Master Signal List for TU102 GPU					
<b>IOB Key:</b> B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z = Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		<b>Reset &amp; Initial Value Key:</b> Z = Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
FBA_WCKB67_N	O			FBVDDQ	
FBA_CMD[35:0]	O			FBVDDQ	
FBA_CLK0	O			FBVDDQ	
FBA_CLK0_N	O			FBVDDQ	
FBA_CLK1	O			FBVDDQ	
FBA_CLK1_N	O			FBVDDQ	
Frame Buffer B					
FBB_D[63:0]	B			FBVDDQ	
FBB_DQM[7:0]	B			FBVDDQ	
FBB_DQS_WP[7:0]	I			FBVDDQ	
FBB_WCK01	O			FBVDDQ	
FBB_WCK01_N	O			FBVDDQ	
FBB_WCKB01	O			FBVDDQ	
FBB_WCKB01_N	O			FBVDDQ	
FBB_WCK23	O			FBVDDQ	
FBB_WCK23_N	O			FBVDDQ	
FBB_WCKB23	O			FBVDDQ	
FBB_WCKB23_N	O			FBVDDQ	
FBB_WCK45	O			FBVDDQ	
FBB_WCK45_N	O			FBVDDQ	
FBB_WCKB45	O			FBVDDQ	
FBB_WCKB45_N	O			FBVDDQ	
FBB_WCK67	O			FBVDDQ	
FBB_WCK67_N	O			FBVDDQ	
FBB_WCKB67	O			FBVDDQ	
FBB_WCKB67_N	O			FBVDDQ	
FBB_CMD[35:0]	O			FBVDDQ	
FBB_CLK0	O			FBVDDQ	
FBB_CLK0_N	O			FBVDDQ	
FBB_CLK1	O			FBVDDQ	
FBB_CLK1_N	O			FBVDDQ	
Frame Buffer C					
FBC_D[63:0]	B			FBVDDQ	
FBC_DQM[7:0]	B			FBVDDQ	
FBC_DQS_WP[7:0]	I			FBVDDQ	
FBC_WCK01	O			FBVDDQ	
FBC_WCK01_N	O			FBVDDQ	
FBC_WCKB01	O			FBVDDQ	
FBC_WCKB01_N	O			FBVDDQ	

Table 4.1 Master Signal List

Master Signal List for TU102 GPU					
<b>IOB Key:</b> B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z = Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		<b>Reset &amp; Initial Value Key:</b> Z = Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
FBC_WCK23	O			FBVDDQ	
FBC_WCK23_N	O			FBVDDQ	
FBC_WCKB23	O			FBVDDQ	
FBC_WCKB23_N	O			FBVDDQ	
FBC_WCK45	O			FBVDDQ	
FBC_WCK45_N	O			FBVDDQ	
FBC_WCKB45	O			FBVDDQ	
FBC_WCKB45_N	O			FBVDDQ	
FBC_WCK67	O			FBVDDQ	
FBC_WCK67_N	O			FBVDDQ	
FBC_WCKB67	O			FBVDDQ	
FBC_WCKB67_N	O			FBVDDQ	
FBC_CMD[35:0]	O			FBVDDQ	
FBC_CLK0	O			FBVDDQ	
FBC_CLK0_N	O			FBVDDQ	
FBC_CLK1	O			FBVDDQ	
FBC_CLK1_N	O			FBVDDQ	
Frame Buffer D					
FBD_D[63:0]	B			FBVDDQ	
FBD_DQM[7:0]	B			FBVDDQ	
FBD_DQS_WP[7:0]	I			FBVDDQ	
FBD_WCK01	O			FBVDDQ	
FBD_WCK01_N	O			FBVDDQ	
FBD_WCKB01	O			FBVDDQ	
FBD_WCKB01_N	O			FBVDDQ	
FBD_WCK23	O			FBVDDQ	
FBD_WCK23_N	O			FBVDDQ	
FBD_WCKB23	O			FBVDDQ	
FBD_WCKB23_N	O			FBVDDQ	
FBD_WCK45	O			FBVDDQ	
FBD_WCK45_N	O			FBVDDQ	
FBD_WCKB45	O			FBVDDQ	
FBD_WCKB45_N	O			FBVDDQ	
FBD_WCK67	O			FBVDDQ	
FBD_WCK67_N	O			FBVDDQ	
FBD_WCKB67	O			FBVDDQ	
FBD_WCKB67_N	O			FBVDDQ	
FBD_CMD[35:0]	O			FBVDDQ	
FBD_CLK0	O			FBVDDQ	



Table 4.1 Master Signal List

Master Signal List for TU102 GPU					
<b>IOB Key:</b> B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z = Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		<b>Reset &amp; Initial Value Key:</b> Z = Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
FBD_CLK0_N	O			FBVDDQ	
FBD_CLK1	O			FBVDDQ	
FBD_CLK1_N	O			FBVDDQ	
Frame Buffer E					
FBE_D[63:0]	B			FBVDDQ	
FBE_DQM[7:0]	B			FBVDDQ	
FBE_DQS_WP[7:0]	I			FBVDDQ	
FBE_WCK01	O			FBVDDQ	
FBE_WCK01_N	O			FBVDDQ	
FBE_WCKB01	O			FBVDDQ	
FBE_WCKB01_N	O			FBVDDQ	
FBE_WCK23	O			FBVDDQ	
FBE_WCK23_N	O			FBVDDQ	
FBE_WCKB23	O			FBVDDQ	
FBE_WCKB23_N	O			FBVDDQ	
FBE_WCK45	O			FBVDDQ	
FBE_WCK45_N	O			FBVDDQ	
FBE_WCKB45	O			FBVDDQ	
FBE_WCKB45_N	O			FBVDDQ	
FBE_WCK67	O			FBVDDQ	
FBE_WCK67_N	O			FBVDDQ	
FBE_WCKB67	O			FBVDDQ	
FBE_WCKB67_N	O			FBVDDQ	
FBE_CMD[35:0]	O			FBVDDQ	
FBE_CLK0	O			FBVDDQ	
FBE_CLK0_N	O			FBVDDQ	
FBE_CLK1	O			FBVDDQ	
FBE_CLK1_N	O			FBVDDQ	
Frame Buffer F					
FBF_D[63:0]	B			FBVDDQ	
FBF_DQM[7:0]	B			FBVDDQ	
FBF_DQS_WP[7:0]	I			FBVDDQ	
FBF_WCK01	O			FBVDDQ	
FBF_WCK01_N	O			FBVDDQ	
FBF_WCKB01	O			FBVDDQ	
FBF_WCKB01_N	O			FBVDDQ	
FBF_WCK23	O			FBVDDQ	
FBF_WCK23_N	O			FBVDDQ	
FBF_WCKB23	O			FBVDDQ	

Table 4.1 Master Signal List

Master Signal List for TU102 GPU					
<b>IOB Key:</b> B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z = Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		<b>Reset &amp; Initial Value Key:</b> Z = Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
FBF_WCKB23_N	O			FBVDDQ	
FBF_WCK45	O			FBVDDQ	
FBF_WCK45_N	O			FBVDDQ	
FBF_WCKB45	O			FBVDDQ	
FBF_WCKB45_N	O			FBVDDQ	
FBF_WCK67	O			FBVDDQ	
FBF_WCK67_N	O			FBVDDQ	
FBF_WCKB67	O			FBVDDQ	
FBF_WCKB67_N	O			FBVDDQ	
FBF_CMD[35:0]	O			FBVDDQ	
FBF_CLK0	O			FBVDDQ	
FBF_CLK0_N	O			FBVDDQ	
FBF_CLK1	O			FBVDDQ	
FBF_CLK1_N	O			FBVDDQ	
Mem Miscellaneous Signals					
FB_CAL_VDDQ	AI			FBVDDQ	
FB_CAL_GND	AI			FBVDDQ	
FB_CAL_TERM	AI			FBVDDQ	
FBVDDQ	P				
FB_VREF	AI			FBVDDQ	
FBVDDQ_SENSE	P				
PCI Express					
PEX_RX[15:0]	I				
PEX_RX[15:0]_N	I				
PEX_TX[15:0]	O				
PEX_TX[15:0]_N	O				
PEX_TERM	AI				
PEX_REFCLK	I				
PEX_REFCLK_N	I				
PEX_CLKREQ_N	O			+1.8V_AON	
PEX_RST_N	I			+1.8V_AON	
PEX_HVDD	P				
PEX_DVDD	P				
PEX_PLL_HVDD	P				
PEX_DVDD	P				
PEX_WAKE	O				
JTAG Interface					
JTAG_TMS	I			+1.8V_AON	
JTAG_TCK	I			+1.8V_AON	

Table 4.1 Master Signal List

Master Signal List for TU102 GPU					
<b>IOB Key:</b> B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z = Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		<b>Reset &amp; Initial Value Key:</b> Z = Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
JTAG_TRST_N	I			+1.8V_AON	
JTAG_TDI	I			+1.8V_AON	
JTAG_TDO	O			+1.8V_AON	
NVJTAG_SEL	I			+1.8V_AON	
Other Clocks					
ROM_CS_N	O			+1.8V_AON	
ROM_SCLK	B			+1.8V_AON	
ROM_SI	B			+1.8V_AON	
ROM_SO	B			+1.8V_AON	
XTAL_OUTBUFF	O			+1.8V_AON	
EXT_REFCLK_FL	I			+1.8V_AON	
XTAL_IN	AI			+1.8V_AON	
XTAL_OUT	AO			+1.8V_AON	
GPIO					
GPIO0	B			+1.8V_AON	
GPIO1	B			+1.8V_AON	
GPIO2	B			+1.8V_AON	
GPIO3	B			+1.8V_AON	
GPIO4	B			+1.8V_AON	
GPIO5	B			+1.8V_AON	
GPIO6	B			+1.8V_AON	
GPIO7	B			+1.8V_AON	
GPIO8	B			+1.8V_AON	
GPIO9	B			+1.8V_AON	
GPIO10	B			+1.8V_AON	
GPIO11	B			+1.8V_AON	
GPIO12	B			+1.8V_AON	
GPIO13	B			+1.8V_AON	
GPIO14	B			+1.8V_AON	
GPIO15	B			+1.8V_AON	
GPIO16	B			+1.8V_AON	
GPIO17	B			+1.8V_AON	
GPIO18	B			+1.8V_AON	
GPIO19	B			+1.8V_AON	
GPIO20	B			+1.8V_AON	
GPIO21	B			+1.8V_AON	
GPIO22	B			+1.8V_AON	
GPIO23	B			+1.8V_AON	
GPIO24	B			+1.8V_AON	

Table 4.1 Master Signal List

Master Signal List for TU102 GPU					
<b>IOB Key:</b> B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z = Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		<b>Reset &amp; Initial Value Key:</b> Z = Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
GPIO25	B			+1.8V_AON	
GPIO26	B			+1.8V_AON	
GPIO27	B			+1.8V_AON	
GPIO28	B			+1.8V_AON	
GPIO29	B			+1.8V_AON	
GPIO30	B			+1.8V_AON	
System Interfaces					
BUFRST_N	O			+1.8V_AON	
STRAPO	I			+1.8V_AON	
STRAP1	I			+1.8V_AON	
STRAP2	I			+1.8V_AON	
STRAP3	I			+1.8V_AON	
STRAP4	I			+1.8V_AON	
STRAP5	I			+1.8V_AON	
OVERT	B			+1.8V_AON	
THERMDP	AO				
THERMDN	AO				
TS_VREF	AI				
GND_SENSE	P				
VDD_SENSE	P				
ADC_IN	AI				
ADC_IN_N	AI				
Power Direct Drills - IO voltage Rails & Core Voltages					
VDD	P				
GND	P				
1V8_AON	P			+1.8V_AON	
PLLs					
XS_PLLVDD	P				
FB_REFPLL_AVDD0	P				
FB_REFPLL_AVDD1	P				
VID_PLLVDD	P				
SP_PLLVDD	P				
XS_PLLVDD	P				
GPCPLL_AVDD0	P				
GPCPLL_AVDD1	P				
FBA_PLL_AVDD	P				
FBB_PLL_AVDD	P				
FBC_PLL_AVDD	P				
FBD_PLL_AVDD	P				

Table 4.1 Master Signal List

Master Signal List for TU102 GPU					
<b>IOB Key:</b> B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z = Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		<b>Reset &amp; Initial Value Key:</b> Z= Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
<b>NVHS</b>					
NVHS_CVDD	P				
NVHS_DVDD	P				
NVHS_HVDD	P				
NVHS_PLL_HVDD	P				
NVHS_REFCLK	I				
NVHS_REFCLK_N	I				
EXT_REFCLK_SLI	B				
NVHS_TERM	AI				
NVHS0_RX0	I				
NVHS0_RX0_N	I				
NVHS0_RX1	I				
NVHS0_RX1_N	I				
NVHS0_RX2	I				
NVHS0_RX2_N	I				
NVHS0_RX3	I				
NVHS0_RX3_N	I				
NVHS0_RX4	I				
NVHS0_RX4_N	I				
NVHS0_RX5	I				
NVHS0_RX5_N	I				
NVHS0_RX6	I				
NVHS0_RX6_N	I				
NVHS0_RX7	I				
NVHS0_RX7_N	I				
NVHS0_TX0	O				
NVHS0_TX0_N	O				
NVHS0_TX1	O				
NVHS0_TX1_N	O				
NVHS0_TX2	O				
NVHS0_TX2_N	O				
NVHS0_TX3	O				
NVHS0_TX3_N	O				
NVHS0_TX4	O				
NVHS0_TX4_N	O				
NVHS0_TX5	O				
NVHS0_TX5_N	O				
NVHS0_TX6	O				
NVHS0_TX6_N	O				

Table 4.1 Master Signal List

Master Signal List for TU102 GPU					
<b>IOB Key:</b> B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z = Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		<b>Reset &amp; Initial Value Key:</b> Z= Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
NVHS0_TX7	O				
NVHS0_TX7_N	O				
NVHS1_RX0	I				
NVHS1_RX0_N	I				
NVHS1_RX1	I				
NVHS1_RX1_N	I				
NVHS1_RX2	I				
NVHS1_RX2_N	I				
NVHS1_RX3	I				
NVHS1_RX3_N	I				
NVHS1_RX4	I				
NVHS1_RX4_N	I				
NVHS1_RX5	I				
NVHS1_RX5_N	I				
NVHS1_RX6	I				
NVHS1_RX6_N	I				
NVHS1_RX7	I				
NVHS1_RX7_N	I				
NVHS1_TX0	O				
NVHS1_TX0_N	O				
NVHS1_TX1	O				
NVHS1_TX1_N	O				
NVHS1_TX2	O				
NVHS1_TX2_N	O				
NVHS1_TX3	O				
NVHS1_TX3_N	O				
NVHS1_TX4	O				
NVHS1_TX4_N	O				
NVHS1_TX5	O				
NVHS1_TX5_N	O				
NVHS1_TX6	O				
NVHS1_TX6_N	O				
NVHS1_TX7	O				
NVHS1_TX7_N	O				
USB					
USB_DVDD	P				
USB_HVDD	P				
USB_LO	O				
USB_LO_N	O				

Table 4.1 Master Signal List

Master Signal List for TU102 GPU					
<b>IOB Key:</b> B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z = Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		<b>Reset &amp; Initial Value Key:</b> Z = Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) <b>Note:</b> Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
USB_L1	O				
USB_L1_N	O				
USB_PLL_HVDD	P				
USB_RBIA5	AI				
USB_SCL	O				
USB_SDA	B				
USB_TERMPO	AI				
USB_TERMPI	AI				
USB_VDDP	P				

## 5 PACKAGE DESCRIPTIONS

### Mechanical Specifications

This section provides the following mechanical specifications and characteristics for the TU102 GPU.

[Table 5.1](#) shows the package specifications for the TU102 GPU in a 47.5 mm x 47.5 mm S-FCBGA package with 2824 balls. [Table 5.1](#) provides the package measurements.



# TU102 47.5 mm x 47.5 mm Package Specification

**Note:** Drawings are not to scale.

Figure 5.1 shows the TU102 package.

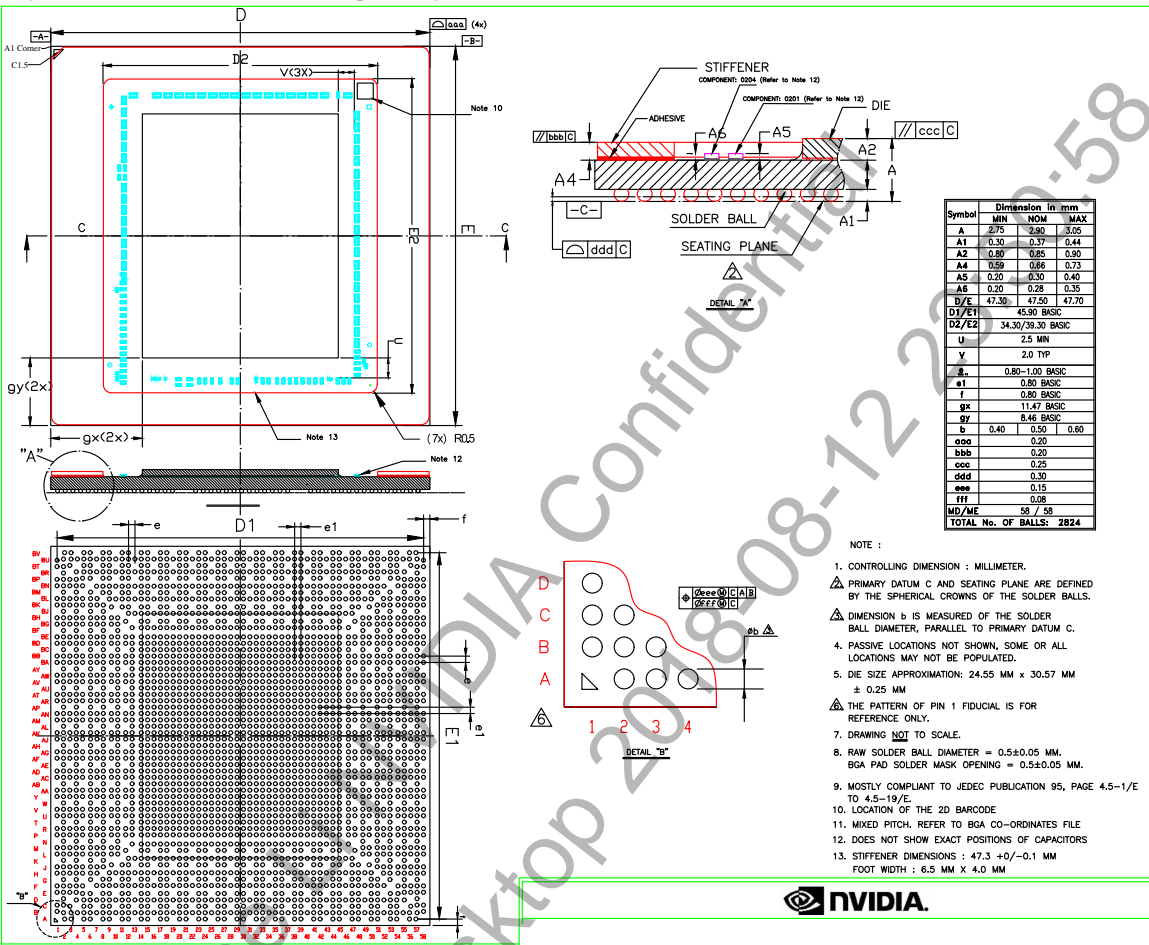


Figure 5.1 TU102 47.5 mm x 47.5 mm Package Specification

# Mechanical and Environmental Specifications

Table 5.1 describes the mechanical characteristics for the packages.

**Table 5.1 Mechanical Characteristics**

Symbol	Parameter	Min.	Nominal	Max.	Units	Notes
P <sub>cont</sub>	Maximum allowable pressure during PCA, system assembly and operation.	-	≤60	≤80	psi	1
T <sub>pkg</sub>	Maximum allowable package temperature during device operation	-	-	≤ TBD	°C	2
T <sub>reflow</sub>	Maximum package temperature during surface mount to printed circuit board	Refer to NVIDIA specifications 630-0011-001				
e <sub>max</sub>	Maximum allowable strain during PCA, system assembly or operation			≤500	μstrains	3

**Notes:**

- 1) This specification is based on the following conditions:
  - a. This specification is based on solder ball deformation and die chips and cracks. Additional requirements may be needed to meet the thermal performance and/or long term reliability as to specific application,
  - b. When a compliant thermal interface is used between die and heat sink, the bond line thickness must have less than 20% in variation.
  - c. The pressure should be measured on the top of the die surface by an instrument equipped pressure sensors. See details in "GPU Load Distribution Measurement Application Note".
  - d. Nominal pressure is the total force divided by the die surface area. Since the pressure may have variations across the whole surfaces. The following additional requirement is applied:
    - i. The pressure has to be measured from the top of the die surface with a grid resolution of 1x1mm<sup>2</sup> for the pressure sensor.
  - e. Both nominal and maximum pressure requirement must be met.
- 2) Maximum package temperature allowed. It includes device case and/or junction temperature.
- 3) Strain measurement shall follow IPC-9704, particularly on following items:
  - a. The strain shall be measured on the top side of PCB close to the four corners of the package. A rigid PCB is assumed.
  - b. For generic application, the max. allowable strain must be no more than 500 μstrains for a board thickness from 1.0 to 3.2mm. A separate requirement may be specified and the qualification test should be performed if
    - i. A sensitive PCB laminate and build up structure is used where the pad cratering occurs at a PCB strain of 500 μstrains or below.
    - ii. A weak surface finish of PCB is used where cracked solder joint has been observed at a PCB strain of 500 μstrains or below.
    - iii. The strain rate is too high (.5000 μstrains/second) during the PCA operations.
  - c. For PCB thickness less than 1,0mm, the max. allowable strain shall follow IPC 9704.

Table 5.2 contains information regarding environmental specifications and conditions.

**Table 5.2 Environmental Specifications and Conditions**

Specifications	Conditions
Storage temperature	-40 °C to 125 °C
Operating humidity	5% to 90% RH
Storage humidity	5% to 95% RH

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## 6 BALL INFORMATION

The TU102 GPU use the GB4-384 package. The TU102 ball list, and ball map are included in this chapter.

## GB4-384 Ball List (Sorted by Ball Name)

Table 6.1 GB4-384 Ball List

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
1V8_AON	BG14	FBA_CMD24	BG57	FBA_D26	AT55
1V8_AON	BG15	FBA_CMD25	BG56	FBA_D27	AV55
1V8_AON	BG17	FBA_CMD26	BE56	FBA_D28	AV52
1V8_AON	BG18	FBA_CMD27	BE57	FBA_D29	AV50
ADC_IN	BP17	FBA_CMD28	BE58	FBA_D3	AN53
ADC_IN*	BP18	FBA_CMD29	BD58	FBA_D30	AV49
BUFRST*	BN12	FBA_CMD3	BA52	FBA_D31	AV48
EXT_REFCLK_FL	BT12	FBA_CMD30	BD57	FBA_D32	BP53
EXT_REFCLK_SLI	BN2	FBA_CMD31	BB58	FBA_D33	BP55
FB_CAL_PD_VDDQ	J50	FBA_CMD32	BA58	FBA_D34	BR54
FB_CAL_PU_GND	J51	FBA_CMD33	BB57	FBA_D35	BP56
FB_CAL_TERM_GND	H50	FBA_CMD34	BA50	FBA_D36	BT57
FB_REFPLL_AVDD0	AN47	FBA_CMD35	BA51	FBA_D37	BT56
FB_REFPLL_AVDD1	M36	FBA_CMD4	BA53	FBA_D38	BU56
FB_REFPLL_AVDD2	V12	FBA_CMD5	BA54	FBA_D39	BT54
FB_VREF	E56	FBA_CMD6	BA56	FBA_D4	AN54
FBA_CLK0	BA49	FBA_CMD7	BA55	FBA_D40	BL55
FBA_CLK0*	BA48	FBA_CMD8	BB50	FBA_D41	BL53
FBA_CLK1	BB48	FBA_CMD9	BB51	FBA_D42	BK52
FBA_CLK1*	BB49	FBA_D0	AM57	FBA_D43	BK54
FBA_CMD0	AV58	FBA_D1	AM58	FBA_D44	BN58
FBA_CMD1	AW58	FBA_D10	AR57	FBA_D45	BN57
FBA_CMD10	BB52	FBA_D11	AT51	FBA_D46	BN55
FBA_CMD11	BB53	FBA_D12	AR54	FBA_D47	BN54
FBA_CMD12	BB56	FBA_D13	AT52	FBA_D48	BD53
FBA_CMD13	BB54	FBA_D14	AT53	FBA_D49	BD55
FBA_CMD14	BB55	FBA_D15	AT54	FBA_D5	AN52
FBA_CMD15	BA57	FBA_D16	AW49	FBA_D50	BD52
FBA_CMD16	BL58	FBA_D17	AV57	FBA_D51	BD56
FBA_CMD17	BK55	FBA_D18	AW48	FBA_D52	BE54
FBA_CMD18	BK58	FBA_D19	AV56	FBA_D53	BD51
FBA_CMD19	BK57	FBA_D2	AN55	FBA_D54	BE50
FBA_CMD2	AW57	FBA_D20	AW56	FBA_D55	BD50
FBA_CMD20	BK56	FBA_D21	AW55	FBA_D56	BE55
FBA_CMD21	BH57	FBA_D22	AW54	FBA_D57	BG54
FBA_CMD22	BH58	FBA_D23	AW53	FBA_D58	BG55
FBA_CMD23	BG58	FBA_D24	AT58	FBA_D59	BG52
		FBA_D25	AT57	FBA_D6	AR51

Ball Name	Ball #
FBA_D60	BG51
FBA_D61	BH52
FBA_D62	BH53
FBA_D63	BH54
FBA_D7	AR50
FBA_D8	AR56
FBA_D9	AR53
FBA_DQM0	AN57
FBA_DQM1	AR55
FBA_DQM2	AW50
FBA_DQM3	AV53
FBA_DQM4	BP57
FBA_DQM5	BL56
FBA_DQM6	BE51
FBA_DQM7	BH56
FBA_DQS_WP0	AN58
FBA_DQS_WP1	AR58
FBA_DQS_WP2	AW52
FBA_DQS_WP3	AV54
FBA_DQS_WP4	BP58
FBA_DQS_WP5	BL57
FBA_DQS_WP6	BE53
FBA_DQS_WP7	BH55
FBA_PLL_AVDD	BB47
FBA_WCK01	AM49
FBA_WCK01*	AM48
FBA_WCK23	AR49
FBA_WCK23*	AR48
FBA_WCK45	BG49
FBA_WCK45*	BG50
FBA_WCK67	BE49
FBA_WCK67*	BE48
FBA_WCKB01	AN49
FBA_WCKB01*	AN48
FBA_WCKB23	AT50
FBA_WCKB23*	AT49
FBA_WCKB45	BH51
FBA_WCKB45*	BH50
FBA_WCKB67	BD49
FBA_WCKB67*	BD48
FBB_CLK0	AC48

Ball Name	Ball #
FBB_CLK0*	AC49
FBB_CLK1	AD48
FBB_CLK1*	AD49
FBB_CMD0	L57
FBB_CMD1	L58
FBB_CMD10	U58
FBB_CMD11	V58
FBB_CMD12	V57
FBB_CMD13	Y57
FBB_CMD14	Y58
FBB_CMD15	AA58
FBB_CMD16	AD56
FBB_CMD17	AD57
FBB_CMD18	AD58
FBB_CMD19	AD55
FBB_CMD2	M58
FBB_CMD20	AD54
FBB_CMD21	AC58
FBB_CMD22	AD53
FBB_CMD23	AD52
FBB_CMD24	AD51
FBB_CMD25	AC54
FBB_CMD26	AC55
FBB_CMD27	AC53
FBB_CMD28	AC52
FBB_CMD29	AC57
FBB_CMD3	P56
FBB_CMD30	AC51
FBB_CMD31	AC56
FBB_CMD32	AA57
FBB_CMD33	AA56
FBB_CMD34	AC50
FBB_CMD35	AD50
FBB_CMD4	P57
FBB_CMD5	P58
FBB_CMD6	R58
FBB_CMD7	R57
FBB_CMD8	U56
FBB_CMD9	U57
FBB_D0	P53
FBB_D1	P51

Ball Name	Ball #
FBB_D10	V50
FBB_D11	R52
FBB_D12	U53
FBB_D13	R54
FBB_D14	U55
FBB_D15	U54
FBB_D16	Y54
FBB_D17	AA49
FBB_D18	AA50
FBB_D19	AA48
FBB_D2	M55
FBB_D20	AA52
FBB_D21	AA54
FBB_D22	AA53
FBB_D23	AA55
FBB_D24	V51
FBB_D25	Y53
FBB_D26	V53
FBB_D27	V54
FBB_D28	Y52
FBB_D29	Y50
FBB_D3	M54
FBB_D30	Y49
FBB_D31	Y48
FBB_D32	AM50
FBB_D33	AM53
FBB_D34	AM51
FBB_D35	AM54
FBB_D36	AK58
FBB_D37	AM56
FBB_D38	AN50
FBB_D39	AN51
FBB_D4	P55
FBB_D40	AJ55
FBB_D41	AJ58
FBB_D42	AJ56
FBB_D43	AJ57
FBB_D44	AK53
FBB_D45	AK52
FBB_D46	AK51
FBB_D47	AK50

Ball Name	Ball #
FBB_D48	AF56
FBB_D49	AF54
FBB_D5	P54
FBB_D50	AF51
FBB_D51	AF53
FBB_D52	AF55
FBB_D53	AF50
FBB_D54	AG51
FBB_D55	AG50
FBB_D56	AJ50
FBB_D57	AJ51
FBB_D58	AJ53
FBB_D59	AG52
FBB_D6	R50
FBB_D60	AG54
FBB_D61	AG57
FBB_D62	AG55
FBB_D63	AG58
FBB_D7	R51
FBB_D8	U51
FBB_D9	U50
FBB_DQM0	M56
FBB_DQM1	R56
FBB_DQM2	Y55
FBB_DQM3	V55
FBB_DQM4	AM55
FBB_DQM5	AK55
FBB_DQM6	AF58
FBB_DQM7	AJ54
FBB_DQS_WP0	M57
FBB_DQS_WP1	R55
FBB_DQS_WP2	Y56
FBB_DQS_WP3	V56
FBB_DQS_WP4	AK57
FBB_DQS_WP5	AK54
FBB_DQS_WP6	AF57
FBB_DQS_WP7	AG53
FBB_PLL_AVDD	AD47
FBB_WCK01	P48
FBB_WCK01*	P49
FBB_WCK23	U49

Ball Name	Ball #
FBB_WCK23*	U48
FBB_WCK45	AK48
FBB_WCK45*	AK49
FBB_WCK67	AG49
FBB_WCK67*	AG48
FBB_WCKB01	R48
FBB_WCKB01*	R49
FBB_WCKB23	V49
FBB_WCKB23*	V48
FBB_WCKB45	AJ49
FBB_WCKB45*	AJ48
FBB_WCKB67	AF49
FBB_WCKB67*	AF48
FBC_CLK0	K44
FBC_CLK0*	L44
FBC_CLK1	L45
FBC_CLK1*	K45
FBC_CMD0	C44
FBC_CMD1	B44
FBC_CMD10	D45
FBC_CMD11	A47
FBC_CMD12	B47
FBC_CMD13	H45
FBC_CMD14	G45
FBC_CMD15	A45
FBC_CMD16	C57
FBC_CMD17	C56
FBC_CMD18	B56
FBC_CMD19	C54
FBC_CMD2	A44
FBC_CMD20	B54
FBC_CMD21	A54
FBC_CMD22	A53
FBC_CMD23	B53
FBC_CMD24	C51
FBC_CMD25	B51
FBC_CMD26	A51
FBC_CMD27	A50
FBC_CMD28	B50
FBC_CMD29	C48
FBC_CMD3	H44

Ball Name	Ball #
FBC_CMD30	B48
FBC_CMD31	A48
FBC_CMD32	B45
FBC_CMD33	C45
FBC_CMD34	J44
FBC_CMD35	J45
FBC_CMD4	G44
FBC_CMD5	D44
FBC_CMD6	E44
FBC_CMD7	F44
FBC_CMD8	F45
FBC_CMD9	E45
FBC_D0	F36
FBC_D1	G36
FBC_D10	A38
FBC_D11	J38
FBC_D12	G39
FBC_D13	F39
FBC_D14	E39
FBC_D15	A39
FBC_D16	A41
FBC_D17	F42
FBC_D18	E42
FBC_D19	K42
FBC_D2	D36
FBC_D20	D42
FBC_D21	G42
FBC_D22	J42
FBC_D23	H42
FBC_D24	B39
FBC_D25	D39
FBC_D26	B41
FBC_D27	C41
FBC_D28	F41
FBC_D29	H41
FBC_D3	E36
FBC_D30	J41
FBC_D31	K41
FBC_D32	L53
FBC_D33	L54
FBC_D34	J54

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
FBC_D35	J55	FBC_DQM6	D48	FBD_CMD18	A27
FBC_D36	L55	FBC_DQM7	D53	FBD_CMD19	E27
FBC_D37	P50	FBC_DQS_WP0	A36	FBD_CMD2	B15
FBC_D38	M53	FBC_DQS_WP1	H38	FBD_CMD20	F27
FBC_D39	L56	FBC_DQS_WP2	A42	FBD_CMD21	G27
FBC_D4	C38	FBC_DQS_WP3	D41	FBD_CMD22	H27
FBC_D40	F58	FBC_DQS_WP4	J57	FBD_CMD23	G26
FBC_D41	F57	FBC_DQS_WP5	H56	FBD_CMD24	F26
FBC_D42	H53	FBC_DQS_WP6	E48	FBD_CMD25	D26
FBC_D43	H52	FBC_DQS_WP7	C53	FBD_CMD26	B24
FBC_D44	H58	FBC_PLL_AVDD	M41	FBD_CMD27	E26
FBC_D45	H57	FBC_WCK01	K35	FBD_CMD28	D27
FBC_D46	J52	FBC_WCK01*	L35	FBD_CMD29	A26
FBC_D47	J53	FBC_WCK23	K38	FBD_CMD3	A15
FBC_D48	F47	FBC_WCK23*	L38	FBD_CMD30	H26
FBC_D49	E47	FBC_WCK45	M51	FBD_CMD31	B26
FBC_D5	D38	FBC_WCK45*	M50	FBD_CMD32	A24
FBC_D50	G47	FBC_WCK67	J48	FBD_CMD33	C26
FBC_D51	C47	FBC_WCK67*	H48	FBD_CMD34	J26
FBC_D52	D50	FBC_WCKB01	K36	FBD_CMD35	J27
FBC_D53	F50	FBC_WCKB01*	J36	FBD_CMD4	B17
FBC_D54	G50	FBC_WCKB23	J39	FBD_CMD5	A17
FBC_D55	G48	FBC_WCKB23*	K39	FBD_CMD6	A18
FBC_D56	C50	FBC_WCKB45	L51	FBD_CMD7	B18
FBC_D57	G51	FBC_WCKB45*	L50	FBD_CMD8	C20
FBC_D58	E51	FBC_WCKB67	H47	FBD_CMD9	B20
FBC_D59	D51	FBC_WCKB67*	J47	FBD_D0	F15
FBC_D6	E38	FBD_CLK0	K26	FBD_D1	H17
FBC_D60	E53	FBD_CLK0*	L26	FBD_D10	C17
FBC_D61	F54	FBD_CLK1	L27	FBD_D11	J21
FBC_D62	D54	FBD_CLK1*	K27	FBD_D12	G18
FBC_D63	E55	FBD_CMD0	B14	FBD_D13	F18
FBC_D7	H36	FBD_CMD1	A14	FBD_D14	C18
FBC_D8	B38	FBD_CMD10	A20	FBD_D15	D18
FBC_D9	F38	FBD_CMD11	B21	FBD_D16	E23
FBC_DQM0	B36	FBD_CMD12	A21	FBD_D17	K24
FBC_DQM1	H39	FBD_CMD13	C23	FBD_D18	J24
FBC_DQM2	B42	FBD_CMD14	B23	FBD_D19	L24
FBC_DQM3	E41	FBD_CMD15	A23	FBD_D2	E17
FBC_DQM4	J58	FBD_CMD16	C27	FBD_D20	F24
FBC_DQM5	H55	FBD_CMD17	B27	FBD_D21	E24



Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
FBD_D22	D24	FBD_D6	J18	FBE_CLK0	M9
FBD_D23	C24	FBD_D60	D32	FBE_CLK0*	M10
FBD_D24	D20	FBD_D61	C32	FBE_CLK1	L9
FBD_D25	E20	FBD_D62	B32	FBE_CLK1*	L8
FBD_D26	F20	FBD_D63	A32	FBE_CMD0	V1
FBD_D27	E21	FBD_D7	H18	FBE_CMD1	V2
FBD_D28	F21	FBD_D8	H20	FBE_CMD10	H4
FBD_D29	F23	FBD_D9	J20	FBE_CMD11	H2
FBD_D3	E15	FBD_DQM0	D15	FBE_CMD12	H3
FBD_D30	H23	FBD_DQM1	H21	FBE_CMD13	H5
FBD_D31	J23	FBD_DQM2	D23	FBE_CMD14	H6
FBD_D32	J35	FBD_DQM3	D21	FBE_CMD15	R2
FBD_D33	H35	FBD_DQM4	B35	FBE_CMD16	B3
FBD_D34	J33	FBD_DQM5	B33	FBE_CMD17	C3
FBD_D35	C35	FBD_DQM6	B29	FBE_CMD18	C2
FBD_D36	D35	FBD_DQM7	E30	FBE_CMD19	E3
FBD_D37	D33	FBD_DQS_WP0	C15	FBE_CMD2	U1
FBD_D38	E35	FBD_DQS_WP1	D17	FBE_CMD20	E2
FBD_D39	F35	FBD_DQS_WP2	H24	FBE_CMD21	E1
FBD_D4	F17	FBD_DQS_WP3	C21	FBE_CMD22	F2
FBD_D40	J32	FBD_DQS_WP4	A35	FBE_CMD23	F1
FBD_D41	H32	FBD_DQS_WP5	A33	FBE_CMD24	F3
FBD_D42	F32	FBD_DQS_WP6	A29	FBE_CMD25	H1
FBD_D43	E32	FBD_DQS_WP7	D30	FBE_CMD26	J2
FBD_D44	E33	FBD_PLL_AVDD	M23	FBE_CMD27	J1
FBD_D45	F33	FBD_WCK01	K18	FBE_CMD28	L1
FBD_D46	G33	FBD_WCK01*	L18	FBE_CMD29	M2
FBD_D47	H33	FBD_WCK23	L21	FBE_CMD3	J7
FBD_D48	F29	FBD_WCK23*	K21	FBE_CMD30	M1
FBD_D49	H29	FBD_WCK45	L33	FBE_CMD31	P2
FBD_D5	J17	FBD_WCK45*	K33	FBE_CMD32	R1
FBD_D50	C29	FBD_WCK67	K30	FBE_CMD33	P1
FBD_D51	J29	FBD_WCK67*	L30	FBE_CMD34	J8
FBD_D52	D29	FBD_WCKB01	K20	FBE_CMD35	H7
FBD_D53	E29	FBD_WCKB01*	L20	FBE_CMD4	L3
FBD_D54	A30	FBD_WCKB23	L23	FBE_CMD5	L2
FBD_D55	B30	FBD_WCKB23*	K23	FBE_CMD6	J3
FBD_D56	J30	FBD_WCKB45	L32	FBE_CMD7	J4
FBD_D57	H30	FBD_WCKB45*	K32	FBE_CMD8	J5
FBD_D58	G30	FBD_WCKB67	K29	FBE_CMD9	J6
FBD_D59	F30	FBD_WCKB67*	L29	FBE_D0	Y6

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
FBE_D1	Y7	FBE_D47	J11	FBE_WCK23	R10
FBE_D10	U9	FBE_D48	E5	FBE_WCK23*	R11
FBE_D11	V8	FBE_D49	E6	FBE_WCK45	L17
FBE_D12	U5	FBE_D5	V4	FBE_WCK45*	K17
FBE_D13	U3	FBE_D50	E4	FBE_WCK67	K14
FBE_D14	U4	FBE_D51	F4	FBE_WCK67*	J14
FBE_D15	U2	FBE_D52	B6	FBE_WCKB01	U10
FBE_D16	M6	FBE_D53	C5	FBE_WCKB01*	U11
FBE_D17	P6	FBE_D54	A6	FBE_WCKB23	P10
FBE_D18	M5	FBE_D55	A5	FBE_WCKB23*	P11
FBE_D19	P7	FBE_D56	G9	FBE_WCKB45	K15
FBE_D2	Y1	FBE_D57	E9	FBE_WCKB45*	J15
FBE_D20	M8	FBE_D58	D9	FBE_WCKB67	J12
FBE_D21	L4	FBE_D59	E8	FBE_WCKB67*	H12
FBE_D22	L6	FBE_D6	V5	FBF_CLK0	AK11
FBE_D23	L7	FBE_D60	D8	FBF_CLK0*	AK10
FBE_D24	R4	FBE_D61	B8	FBF_CLK1	AJ11
FBE_D25	R5	FBE_D62	C9	FBF_CLK1*	AJ10
FBE_D26	R3	FBE_D63	A8	FBF_CMD0	BA1
FBE_D27	R6	FBE_D7	Y8	FBF_CMD1	BA2
FBE_D28	P3	FBE_D8	V6	FBF_CMD10	AN3
FBE_D29	P4	FBE_D9	V9	FBF_CMD11	AN2
FBE_D3	Y5	FBE_DQM0	Y4	FBF_CMD12	AN1
FBE_D30	P9	FBE_DQM1	U6	FBF_CMD13	AM1
FBE_D31	P8	FBE_DQM2	M4	FBF_CMD14	AM2
FBE_D32	H15	FBE_DQM3	R9	FBF_CMD15	AK3
FBE_D33	F14	FBE_DQM4	D14	FBF_CMD16	AF1
FBE_D34	H14	FBE_DQM5	B12	FBF_CMD17	AG1
FBE_D35	F12	FBE_DQM6	D5	FBF_CMD18	AG2
FBE_D36	E12	FBE_DQM7	A9	FBF_CMD19	AJ3
FBE_D37	D12	FBE_DQS_WP0	Y2	FBF_CMD2	BA3
FBE_D38	C12	FBE_DQS_WP1	U8	FBF_CMD20	AJ2
FBE_D39	E14	FBE_DQS_WP2	M3	FBF_CMD21	AJ1
FBE_D4	V3	FBE_DQS_WP3	R8	FBF_CMD22	AJ8
FBE_D40	C11	FBE_DQS_WP4	C14	FBF_CMD23	AJ6
FBE_D41	E11	FBE_DQS_WP5	A12	FBF_CMD24	AJ5
FBE_D42	A11	FBE_DQS_WP6	D6	FBF_CMD25	AJ4
FBE_D43	B11	FBE_DQS_WP7	B9	FBF_CMD26	AJ7
FBE_D44	D11	FBE_PLL_AVDD	P12	FBF_CMD27	AK8
FBE_D45	G11	FBE_WCK01	V10	FBF_CMD28	AK7
FBE_D46	H11	FBE_WCK01*	V11	FBF_CMD29	AK2

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
FBF_CMD3	AW2	FBF_D34	AA9	FBF_DQM5	AD3
FBF_CMD30	AK6	FBF_D35	AA6	FBF_DQM6	AF3
FBF_CMD31	AK5	FBF_D36	AA1	FBF_DQM7	AF6
FBF_CMD32	AK1	FBF_D37	AA2	FBF_DQS_WP0	AW5
FBF_CMD33	AK4	FBF_D38	AA3	FBF_DQS_WP1	AV9
FBF_CMD34	AK9	FBF_D39	AA5	FBF_DQS_WP2	AN5
FBF_CMD35	AJ9	FBF_D4	AV2	FBF_DQS_WP3	AR4
FBF_CMD4	AW1	FBF_D40	AC2	FBF_DQS_WP4	AC1
FBF_CMD5	AW3	FBF_D41	AC5	FBF_DQS_WP5	AD1
FBF_CMD6	AV1	FBF_D42	AD2	FBF_DQS_WP6	AF2
FBF_CMD7	AT1	FBF_D43	AC6	FBF_DQS_WP7	AD6
FBF_CMD8	AR1	FBF_D44	AC3	FBF_PLL_AVDD	AM12
FBF_CMD9	AR2	FBF_D45	AD9	FBF_WCK01	AT11
FBF_D0	BB3	FBF_D46	AC7	FBF_WCK01*	AT10
FBF_D1	BB2	FBF_D47	AC8	FBF_WCK23	AN10
FBF_D10	AW9	FBF_D48	AG6	FBF_WCK23*	AN11
FBF_D11	AV10	FBF_D49	AG7	FBF_WCK45	Y11
FBF_D12	AT8	FBF_D5	AW7	FBF_WCK45*	Y10
FBF_D13	AT7	FBF_D50	AG3	FBF_WCK67	AC9
FBF_D14	AV5	FBF_D51	AG8	FBF_WCK67*	AC10
FBF_D15	AV6	FBF_D52	AG4	FBF_WCKB01	AR11
FBF_D16	AN6	FBF_D53	AG9	FBF_WCKB01*	AR10
FBF_D17	AN9	FBF_D54	AF4	FBF_WCKB23	AM9
FBF_D18	AM8	FBF_D55	AG10	FBF_WCKB23*	AM10
FBF_D19	AN8	FBF_D56	AF11	FBF_WCKB45	AA10
FBF_D2	AV3	FBF_D57	AF10	FBF_WCKB45*	AA11
FBF_D20	AM4	FBF_D58	AF9	FBF_WCKB67	AD10
FBF_D21	AM7	FBF_D59	AF7	FBF_WCKB67*	AD11
FBF_D22	AM6	FBF_D6	AW8	FBVDDQ	AA12
FBF_D23	AM3	FBF_D60	AF5	FBVDDQ	AA47
FBF_D24	AT2	FBF_D61	AD4	FBVDDQ	AC11
FBF_D25	AT3	FBF_D62	AD5	FBVDDQ	AC12
FBF_D26	AT5	FBF_D63	AD8	FBVDDQ	AC47
FBF_D27	AT6	FBF_D7	AV4	FBVDDQ	AD12
FBF_D28	AR6	FBF_D8	AW10	FBVDDQ	AF12
FBF_D29	AR7	FBF_D9	AT9	FBVDDQ	AF47
FBF_D3	BB1	FBF_DQM0	AW6	FBVDDQ	AG11
FBF_D30	AR8	FBF_DQM1	AV8	FBVDDQ	AG12
FBF_D31	AR9	FBF_DQM2	AN4	FBVDDQ	AG47
FBF_D32	Y9	FBF_DQM3	AR3	FBVDDQ	AJ12
FBF_D33	AA8	FBF_DQM4	AA4	FBVDDQ	AJ47

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
FBVDDQ	AK12	FBVDDQ	M24	GND	AA39
FBVDDQ	AK47	FBVDDQ	M26	GND	AA41
FBVDDQ	AM11	FBVDDQ	M27	GND	AA43
FBVDDQ	AM47	FBVDDQ	M29	GND	AA45
FBVDDQ	AN12	FBVDDQ	M30	GND	AA51
FBVDDQ	AR12	FBVDDQ	M32	GND	AA7
FBVDDQ	AR47	FBVDDQ	M33	GND	AB10
FBVDDQ	AT48	FBVDDQ	M35	GND	AB12
FBVDDQ	AV47	FBVDDQ	M38	GND	AB14
FBVDDQ	AW47	FBVDDQ	M39	GND	AB16
FBVDDQ	BA47	FBVDDQ	M42	GND	AB18
FBVDDQ	BD47	FBVDDQ	M44	GND	AB2
FBVDDQ	BE47	FBVDDQ	M45	GND	AB20
FBVDDQ	BG44	FBVDDQ	M49	GND	AB22
FBVDDQ	BG45	FBVDDQ	P47	GND	AB24
FBVDDQ	BH44	FBVDDQ	R12	GND	AB26
FBVDDQ	BH45	FBVDDQ	R47	GND	AB28
FBVDDQ	BJ44	FBVDDQ	U12	GND	AB30
FBVDDQ	BJ45	FBVDDQ	U47	GND	AB32
FBVDDQ	BJ47	FBVDDQ	V47	GND	AB34
FBVDDQ	F8	FBVDDQ	Y12	GND	AB36
FBVDDQ	G8	FBVDDQ	Y47	GND	AB38
FBVDDQ	H9	FBVDDQ_GND_SENSE	E57	GND	AB4
FBVDDQ	J9	FBVDDQ_SENSE	E58	GND	AB40
FBVDDQ	K12	GND	BJ33	GND	AB42
FBVDDQ	K47	GND	A2	GND	AB44
FBVDDQ	L10	GND	A3	GND	AB47
FBVDDQ	L11	GND	A56	GND	AB49
FBVDDQ	L14	GND	A57	GND	AB51
FBVDDQ	L15	GND	AA15	GND	AB53
FBVDDQ	L36	GND	AA17	GND	AB55
FBVDDQ	L39	GND	AA19	GND	AB57
FBVDDQ	L41	GND	AA21	GND	AB6
FBVDDQ	L42	GND	AA23	GND	AB8
FBVDDQ	L48	GND	AA25	GND	AC15
FBVDDQ	L49	GND	AA27	GND	AC17
FBVDDQ	M14	GND	AA29	GND	AC19
FBVDDQ	M17	GND	AA31	GND	AC21
FBVDDQ	M18	GND	AA33	GND	AC23
FBVDDQ	M20	GND	AA35	GND	AC25
FBVDDQ	M21	GND	AA37	GND	AC27

Ball Name	Ball #
GND	AC29
GND	AC31
GND	AC33
GND	AC35
GND	AC37
GND	AC39
GND	AC4
GND	AC41
GND	AC43
GND	AC45
GND	AD14
GND	AD16
GND	AD18
GND	AD20
GND	AD22
GND	AD24
GND	AD26
GND	AD28
GND	AD30
GND	AD32
GND	AD34
GND	AD36
GND	AD38
GND	AD40
GND	AD42
GND	AD44
GND	AD7
GND	AE10
GND	AE12
GND	AE15
GND	AE17
GND	AE19
GND	AE2
GND	AE21
GND	AE23
GND	AE25
GND	AE27
GND	AE29
GND	AE31
GND	AE33
GND	AE35

Ball Name	Ball #
GND	AE37
GND	AE39
GND	AE4
GND	AE41
GND	AE43
GND	AE45
GND	AE47
GND	AE49
GND	AE51
GND	AE53
GND	AE55
GND	AE57
GND	AE6
GND	AE8
GND	AF14
GND	AF16
GND	AF18
GND	AF20
GND	AF22
GND	AF24
GND	AF26
GND	AF28
GND	AF30
GND	AF32
GND	AF34
GND	AF36
GND	AF38
GND	AF40
GND	AF42
GND	AF44
GND	AF52
GND	AF8
GND	AG15
GND	AG17
GND	AG19
GND	AG21
GND	AG23
GND	AG25
GND	AG27
GND	AG29
GND	AG31

Ball Name	Ball #
GND	AG33
GND	AG35
GND	AG37
GND	AG39
GND	AG41
GND	AG43
GND	AG45
GND	AG5
GND	AG56
GND	AH10
GND	AH12
GND	AH14
GND	AH16
GND	AH18
GND	AH2
GND	AH20
GND	AH22
GND	AH24
GND	AH26
GND	AH28
GND	AH30
GND	AH32
GND	AH34
GND	AH36
GND	AH38
GND	AH4
GND	AH40
GND	AH42
GND	AH44
GND	AH47
GND	AH49
GND	AH51
GND	AH53
GND	AH55
GND	AH57
GND	AH6
GND	AH8
GND	AJ15
GND	AJ17
GND	AJ19
GND	AJ21

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
GND	AJ23	GND	AL31	GND	AN27
GND	AJ25	GND	AL33	GND	AN29
GND	AJ27	GND	AL35	GND	AN31
GND	AJ29	GND	AL37	GND	AN33
GND	AJ31	GND	AL39	GND	AN35
GND	AJ33	GND	AL4	GND	AN37
GND	AJ35	GND	AL41	GND	AN39
GND	AJ37	GND	AL43	GND	AN41
GND	AJ39	GND	AL45	GND	AN43
GND	AJ41	GND	AL47	GND	AN45
GND	AJ43	GND	AL49	GND	AN56
GND	AJ45	GND	AL51	GND	AN7
GND	AJ52	GND	AL53	GND	AP10
GND	AK14	GND	AL55	GND	AP12
GND	AK16	GND	AL57	GND	AP14
GND	AK18	GND	AL6	GND	AP16
GND	AK20	GND	AL8	GND	AP18
GND	AK22	GND	AM14	GND	AP2
GND	AK24	GND	AM16	GND	AP20
GND	AK26	GND	AM18	GND	AP22
GND	AK28	GND	AM20	GND	AP24
GND	AK30	GND	AM22	GND	AP26
GND	AK32	GND	AM24	GND	AP28
GND	AK34	GND	AM26	GND	AP30
GND	AK36	GND	AM28	GND	AP32
GND	AK38	GND	AM30	GND	AP34
GND	AK40	GND	AM32	GND	AP36
GND	AK42	GND	AM34	GND	AP38
GND	AK44	GND	AM36	GND	AP4
GND	AK56	GND	AM38	GND	AP40
GND	AL10	GND	AM40	GND	AP42
GND	AL12	GND	AM42	GND	AP44
GND	AL15	GND	AM44	GND	AP47
GND	AL17	GND	AM5	GND	AP49
GND	AL19	GND	AM52	GND	AP51
GND	AL2	GND	AN15	GND	AP53
GND	AL21	GND	AN17	GND	AP55
GND	AL23	GND	AN19	GND	AP57
GND	AL25	GND	AN21	GND	AP6
GND	AL27	GND	AN23	GND	AP8
GND	AL29	GND	AN25	GND	AR15

Ball Name	Ball #
GND	AR17
GND	AR19
GND	AR21
GND	AR23
GND	AR25
GND	AR27
GND	AR29
GND	AR31
GND	AR33
GND	AR35
GND	AR37
GND	AR39
GND	AR41
GND	AR43
GND	AR45
GND	AR5
GND	AR52
GND	AT14
GND	AT16
GND	AT18
GND	AT20
GND	AT22
GND	AT24
GND	AT26
GND	AT28
GND	AT30
GND	AT32
GND	AT34
GND	AT36
GND	AT38
GND	AT4
GND	AT40
GND	AT42
GND	AT44
GND	AT56
GND	AU10
GND	AU12
GND	AU15
GND	AU17
GND	AU19
GND	AU2

Ball Name	Ball #
GND	AU21
GND	AU23
GND	AU25
GND	AU27
GND	AU29
GND	AU31
GND	AU33
GND	AU35
GND	AU37
GND	AU39
GND	AU4
GND	AU41
GND	AU43
GND	AU45
GND	AU47
GND	AU49
GND	AU51
GND	AU53
GND	AU55
GND	AU57
GND	AU6
GND	AU8
GND	AV14
GND	AV16
GND	AV18
GND	AV20
GND	AV22
GND	AV24
GND	AV26
GND	AV28
GND	AV30
GND	AV32
GND	AV34
GND	AV36
GND	AV38
GND	AV40
GND	AV42
GND	AV44
GND	AV51
GND	AV7
GND	AW15

Ball Name	Ball #
GND	AW17
GND	AW19
GND	AW21
GND	AW23
GND	AW25
GND	AW27
GND	AW29
GND	AW31
GND	AW33
GND	AW35
GND	AW37
GND	AW39
GND	AW4
GND	AW41
GND	AW43
GND	AW45
GND	AW51
GND	AY10
GND	AY12
GND	AY14
GND	AY16
GND	AY18
GND	AY2
GND	AY20
GND	AY22
GND	AY24
GND	AY26
GND	AY28
GND	AY30
GND	AY32
GND	AY34
GND	AY36
GND	AY38
GND	AY4
GND	AY40
GND	AY42
GND	AY44
GND	AY47
GND	AY49
GND	AY51
GND	AY53

Ball Name	Ball #
GND	AY55
GND	AY57
GND	AY6
GND	AY8
GND	B1
GND	B10
GND	B13
GND	B16
GND	B19
GND	B2
GND	B22
GND	B25
GND	B28
GND	B31
GND	B34
GND	B37
GND	B4
GND	B40
GND	B43
GND	B46
GND	B49
GND	B5
GND	B52
GND	B55
GND	B57
GND	B58
GND	B7
GND	BA15
GND	BA17
GND	BA19
GND	BA21
GND	BA23
GND	BA25
GND	BA27
GND	BA29
GND	BA31
GND	BA33
GND	BA35
GND	BA37
GND	BA39
GND	BA4

Ball Name	Ball #
GND	BA41
GND	BA43
GND	BA45
GND	BA9
GND	BB14
GND	BB16
GND	BB18
GND	BB20
GND	BB22
GND	BB24
GND	BB26
GND	BB28
GND	BB30
GND	BB32
GND	BB34
GND	BB36
GND	BB38
GND	BB4
GND	BB40
GND	BB42
GND	BB44
GND	BB5
GND	BB8
GND	BC10
GND	BC12
GND	BC15
GND	BC17
GND	BC19
GND	BC2
GND	BC21
GND	BC23
GND	BC25
GND	BC27
GND	BC29
GND	BC31
GND	BC33
GND	BC35
GND	BC37
GND	BC39
GND	BC4
GND	BC41

Ball Name	Ball #
GND	BC43
GND	BC45
GND	BC47
GND	BC49
GND	BC51
GND	BC53
GND	BC55
GND	BC57
GND	BC6
GND	BC8
GND	BD14
GND	BD16
GND	BD18
GND	BD20
GND	BD22
GND	BD24
GND	BD26
GND	BD28
GND	BD30
GND	BD32
GND	BD34
GND	BD36
GND	BD38
GND	BD4
GND	BD40
GND	BD42
GND	BD44
GND	BD54
GND	BD9
GND	BE15
GND	BE17
GND	BE19
GND	BE21
GND	BE23
GND	BE25
GND	BE27
GND	BE29
GND	BE31
GND	BE33
GND	BE35
GND	BE37



Ball Name	Ball #
GND	BE39
GND	BE4
GND	BE41
GND	BE43
GND	BE45
GND	BE5
GND	BE52
GND	BE8
GND	BF10
GND	BF2
GND	BF4
GND	BF49
GND	BF51
GND	BF53
GND	BF55
GND	BF57
GND	BF6
GND	BF8
GND	BG13
GND	BG16
GND	BG19
GND	BG22
GND	BG25
GND	BG28
GND	BG31
GND	BG34
GND	BG37
GND	BG4
GND	BG40
GND	BG43
GND	BG46
GND	BG53
GND	BG9
GND	BH4
GND	BH5
GND	BH8
GND	BJ13
GND	BJ16
GND	BJ19
GND	BJ2
GND	BJ22

Ball Name	Ball #
GND	BJ25
GND	BJ28
GND	BJ31
GND	BJ34
GND	BJ37
GND	BJ4
GND	BJ40
GND	BJ43
GND	BJ46
GND	BJ51
GND	BJ53
GND	BJ55
GND	BJ57
GND	BJ6
GND	BJ8
GND	BK23
GND	BK26
GND	BK29
GND	BK3
GND	BK32
GND	BK35
GND	BK38
GND	BK41
GND	BK44
GND	BK47
GND	BK48
GND	BK50
GND	BK51
GND	BK53
GND	BK8
GND	BK9
GND	BL10
GND	BL13
GND	BL16
GND	BL19
GND	BL22
GND	BL24
GND	BL25
GND	BL27
GND	BL28
GND	BL3

Ball Name	Ball #
GND	BL30
GND	BL31
GND	BL33
GND	BL34
GND	BL37
GND	BL39
GND	BL4
GND	BL40
GND	BL42
GND	BL43
GND	BL45
GND	BL46
GND	BL48
GND	BL49
GND	BL52
GND	BL54
GND	BL7
GND	BM2
GND	BM4
GND	BM53
GND	BM55
GND	BM57
GND	BM6
GND	BN10
GND	BN13
GND	BN16
GND	BN19
GND	BN22
GND	BN25
GND	BN28
GND	BN31
GND	BN34
GND	BN37
GND	BN4
GND	BN40
GND	BN43
GND	BN46
GND	BN49
GND	BN52
GND	BN56
GND	BN7

Ball Name	Ball #
GND	BP24
GND	BP27
GND	BP30
GND	BP33
GND	BP36
GND	BP39
GND	BP4
GND	BP42
GND	BP45
GND	BP48
GND	BP51
GND	BP54
GND	BP8
GND	BR10
GND	BR13
GND	BR16
GND	BR19
GND	BR2
GND	BR22
GND	BR23
GND	BR25
GND	BR26
GND	BR27
GND	BR28
GND	BR29
GND	BR30
GND	BR31
GND	BR32
GND	BR33
GND	BR34
GND	BR35
GND	BR36
GND	BR37
GND	BR38
GND	BR39
GND	BR4
GND	BR40
GND	BR41
GND	BR42
GND	BR43
GND	BR44

Ball Name	Ball #
GND	BR45
GND	BR46
GND	BR47
GND	BR48
GND	BR49
GND	BR5
GND	BR50
GND	BR51
GND	BR52
GND	BR55
GND	BR57
GND	BR7
GND	BR8
GND	BR9
GND	BT1
GND	BT5
GND	BT58
GND	BT6
GND	BU1
GND	BU10
GND	BU13
GND	BU16
GND	BU19
GND	BU2
GND	BU22
GND	BU24
GND	BU25
GND	BU28
GND	BU31
GND	BU34
GND	BU37
GND	BU4
GND	BU40
GND	BU43
GND	BU46
GND	BU49
GND	BU52
GND	BU53
GND	BU54
GND	BU55
GND	BU57

Ball Name	Ball #
GND	BU58
GND	BU7
GND	BV2
GND	BV3
GND	BV56
GND	BV57
GND	C1
GND	C30
GND	C33
GND	C36
GND	C39
GND	C42
GND	C58
GND	C6
GND	C8
GND	D10
GND	D13
GND	D16
GND	D19
GND	D2
GND	D22
GND	D25
GND	D28
GND	D31
GND	D34
GND	D37
GND	D4
GND	D40
GND	D43
GND	D46
GND	D47
GND	D49
GND	D52
GND	D55
GND	D57
GND	D7
GND	E18
GND	E50
GND	E54
GND	F10
GND	F11

Ball Name	Ball #
GND	F13
GND	F16
GND	F19
GND	F22
GND	F25
GND	F28
GND	F31
GND	F34
GND	F37
GND	F40
GND	F43
GND	F46
GND	F48
GND	F49
GND	F5
GND	F51
GND	F52
GND	F55
GND	F7
GND	F9
GND	G12
GND	G14
GND	G15
GND	G17
GND	G2
GND	G20
GND	G21
GND	G23
GND	G24
GND	G29
GND	G32
GND	G35
GND	G38
GND	G4
GND	G41
GND	G53
GND	G55
GND	G57
GND	G6
GND	H10
GND	H13

Ball Name	Ball #
GND	H16
GND	H19
GND	H22
GND	H25
GND	H28
GND	H31
GND	H34
GND	H37
GND	H40
GND	H43
GND	H46
GND	H49
GND	H54
GND	J56
GND	K13
GND	K16
GND	K19
GND	K2
GND	K22
GND	K25
GND	K28
GND	K31
GND	K34
GND	K37
GND	K4
GND	K40
GND	K43
GND	K46
GND	K51
GND	K53
GND	K55
GND	K57
GND	K6
GND	K8
GND	L5
GND	L52
GND	M13
GND	M16
GND	M19
GND	M22
GND	M25

Ball Name	Ball #
GND	M28
GND	M31
GND	M34
GND	M37
GND	M40
GND	M43
GND	M46
GND	M52
GND	M7
GND	N10
GND	N2
GND	N4
GND	N49
GND	N51
GND	N53
GND	N55
GND	N57
GND	N6
GND	N8
GND	P14
GND	P16
GND	P18
GND	P20
GND	P22
GND	P24
GND	P26
GND	P28
GND	P30
GND	P32
GND	P34
GND	P36
GND	P38
GND	P40
GND	P42
GND	P44
GND	P5
GND	P52
GND	R15
GND	R17
GND	R19
GND	R21

Ball Name	Ball #
GND	R23
GND	R25
GND	R27
GND	R29
GND	R31
GND	R33
GND	R35
GND	R37
GND	R39
GND	R41
GND	R43
GND	R45
GND	R53
GND	R7
GND	T10
GND	T12
GND	T14
GND	T16
GND	T18
GND	T2
GND	T20
GND	T22
GND	T24
GND	T26
GND	T28
GND	T30
GND	T32
GND	T34
GND	T36
GND	T38
GND	T4
GND	T40
GND	T42
GND	T44
GND	T47
GND	T49
GND	T51
GND	T53
GND	T55
GND	T57
GND	T6

Ball Name	Ball #
GND	T8
GND	U15
GND	U17
GND	U19
GND	U21
GND	U23
GND	U25
GND	U27
GND	U29
GND	U31
GND	U33
GND	U35
GND	U37
GND	U39
GND	U41
GND	U43
GND	U45
GND	U52
GND	U7
GND	V14
GND	V16
GND	V18
GND	V20
GND	V22
GND	V24
GND	V26
GND	V28
GND	V30
GND	V32
GND	V34
GND	V36
GND	V38
GND	V40
GND	V42
GND	V44
GND	V52
GND	V7
GND	W10
GND	W12
GND	W15
GND	W17

Ball Name	Ball #
GND	W19
GND	W2
GND	W21
GND	W23
GND	W25
GND	W27
GND	W29
GND	W31
GND	W33
GND	W35
GND	W37
GND	W39
GND	W4
GND	W41
GND	W43
GND	W45
GND	W47
GND	W49
GND	W51
GND	W53
GND	W55
GND	W57
GND	W6
GND	W8
GND	Y14
GND	Y16
GND	Y18
GND	Y20
GND	Y22
GND	Y24
GND	Y26
GND	Y28
GND	Y3
GND	Y30
GND	Y32
GND	Y34
GND	Y36
GND	Y38
GND	Y40
GND	Y42
GND	Y44

Ball Name	Ball #
GND	Y51
GND	BH33
GND_SENSE	BT53
GPCPLL_AVDD0	AT47
GPCPLL_AVDD1	M15
GPCPLL_AVDD2	AT12
GPIO0	BL17
GPIO1	BM17
GPIO10	BN17
GPIO11	BL15
GPIO12	BH14
GPIO13	BK18
GPIO14	BR15
GPIO15	BR14
GPIO16	BK17
GPIO17	BL14
GPIO18	BM14
GPIO19	BP14
GPIO2	BL18
GPIO20	BM18
GPIO21	BT15
GPIO22	BU15
GPIO23	BN15
GPIO24	BV15
GPIO25	BU14
GPIO26	BV14
GPIO27	BM15
GPIO28	BN14
GPIO29	BH15
GPIO3	BK14
GPIO30	BJ15
GPIO4	BK15
GPIO5	BJ12
GPIO6	BJ14
GPIO7	BN18
GPIO8	BT14
GPIO9	BP15
I2CB_SCL	BR17
I2CB_SDA	BT17
I2CC_SCL	BU18
I2CC_SDA	BU17

Ball Name	Ball #
I2CS_SCL	BR18
I2CS_SDA	BT18
IFP_IOVDD	BG29
IFP_IOVDD	BJ30
IFP_IOVDD	BG30
IFP_IOVDD	BG32
IFP_IOVDD	BG33
IFP_IOVDD	BH29
IFP_IOVDD	BH30
IFP_IOVDD	BJ26
IFP_IOVDD	BJ27
IFP_IOVDD	BJ29
IFPA_AUX_SCL	BV18
IFPA_AUX_SDA*	BV17
IFPA_L0	BM33
IFPA_L0*	BN33
IFPA_L1	BP32
IFPA_L1*	BN32
IFPA_L2	BL32
IFPA_L2*	BM32
IFPA_L3	BN30
IFPA_L3*	BM30
IFPAB_PLLVDD	BH27
IFPAB_RSET	BK30
IFPB_AUX_SCL	BV20
IFPB_AUX_SDA*	BV21
IFPB_L0	BT33
IFPB_L0*	BU33
IFPB_L1	BV33
IFPB_L1*	BV32
IFPB_L2	BU32
IFPB_L2*	BT32
IFPB_L3	BT30
IFPB_L3*	BU30
IFPC_AUX_SCL	BU21
IFPC_AUX_SDA*	BT21
IFPC_L0	BP29
IFPC_L0*	BN29
IFPC_L1	BM29
IFPC_L1*	BL29
IFPC_L2	BN27

Ball Name	Ball #
IFPC_L2*	BM27
IFPC_L3	BL26
IFPC_L3*	BM26
IFPCD_PLLVDD	BH26
IFPCD_RSET	BK27
IFPD_AUX_SCL	BT20
IFPD_AUX_SDA*	BU20
IFPD_L0	BV30
IFPD_L0*	BV29
IFPD_L1	BU29
IFPD_L1*	BT29
IFPD_L2	BT27
IFPD_L2*	BU27
IFPD_L3	BV27
IFPD_L3*	BV26
IFPE_AUX_SCL	BR21
IFPE_AUX_SDA*	BP21
IFPE_L0	BN26
IFPE_L0*	BP26
IFPE_L1	BU26
IFPE_L1*	BT26
IFPE_L2	BR24
IFPE_L2*	BT24
IFPE_L3	BU23
IFPE_L3*	BT23
IFPE_PLLVDD	BG24
IFPE_RSET	BK24
IFPF_AUX_SCL	BP20
IFPF_AUX_SDA*	BR20
IFPF_L0	BV23
IFPF_L0*	BV24
IFPF_L1	BM23
IFPF_L1*	BL23
IFPF_L2	BN24
IFPF_L2*	BM24
IFPF_L3	BN23
IFPF_L3*	BP23
JTAG_TCK	BU35
JTAG_TDI	BV35
JTAG_TDO	BU36
JTAG_TMS	BV36

Ball Name	Ball #
JTAG_TRST*	BT36
NC	BH17
NC	BH18
NC	BJ17
NC	BJ18
NC	BJ32
NC	BK33
NC	BN3
NC	F56
NVHS_CVDD	AV12
NVHS_CVDD	AW12
NVHS_DVDD	AV11
NVHS_DVDD	BE12
NVHS_DVDD	AW11
NVHS_DVDD	BA11
NVHS_DVDD	BA12
NVHS_DVDD	BB11
NVHS_DVDD	BB12
NVHS_DVDD	BD11
NVHS_DVDD	BD12
NVHS_DVDD	BE11
NVHS_HVDD	BA10
NVHS_HVDD	BB10
NVHS_HVDD	BB9
NVHS_HVDD	BD10
NVHS_HVDD	BE9
NVHS_HVDD	BG10
NVHS_HVDD	BH10
NVHS_HVDD	BH11
NVHS_PLL_HVDD	BE10
NVHS_REFCLK	BA6
NVHS_REFCLK*	BA5
NVHS_TERMPP	BT2
NVHS0_RX0	BD3
NVHS0_RX0*	BD2
NVHS0_RX1	BD1
NVHS0_RX1*	BE1
NVHS0_RX2	BE2
NVHS0_RX2*	BE3
NVHS0_RX3	BG3
NVHS0_RX3*	BG2

Ball Name	Ball #
NVHS0_RX4	BH2
NVHS0_RX4*	BH3
NVHS0_RX5	BG1
NVHS0_RX5*	BH1
NVHS0_RX6	BK1
NVHS0_RX6*	BK2
NVHS0_RX7	BL1
NVHS0_RX7*	BL2
NVHS0_TX0	BA7
NVHS0_TX0*	BA8
NVHS0_TX1	BB6
NVHS0_TX1*	BB7
NVHS0_TX2	BD6
NVHS0_TX2*	BD5
NVHS0_TX3	BD7
NVHS0_TX3*	BD8
NVHS0_TX4	BE7
NVHS0_TX4*	BE6
NVHS0_TX5	BG6
NVHS0_TX5*	BG5
NVHS0_TX6	BG7
NVHS0_TX6*	BG8
NVHS0_TX7	BH7
NVHS0_TX7*	BH6
NVHS1_RX0	BP2
NVHS1_RX0*	BP3
NVHS1_RX1	BN1
NVHS1_RX1*	BP1
NVHS1_RX2	BT3
NVHS1_RX2*	BU3
NVHS1_RX3	BU5
NVHS1_RX3*	BV5
NVHS1_RX4	BV6
NVHS1_RX4*	BU6
NVHS1_RX5	BU8
NVHS1_RX5*	BT8
NVHS1_RX6	BT9
NVHS1_RX6*	BU9
NVHS1_RX7	BV9
NVHS1_RX7*	BV8
NVHS1_TX0	BK4

Ball Name	Ball #
NVHS1_TX0*	BK5
NVHS1_TX1	BK6
NVHS1_TX1*	BK7
NVHS1_TX2	BN5
NVHS1_TX2*	BP5
NVHS1_TX3	BL5
NVHS1_TX3*	BL6
NVHS1_TX4	BP6
NVHS1_TX4*	BR6
NVHS1_TX5	BM8
NVHS1_TX5*	BN8
NVHS1_TX6	BL9
NVHS1_TX6*	BM9
NVHS1_TX7	BN9
NVHS1_TX7*	BP9
NVJTAG_SEL	BT35
OVERT	BN11
PEX_CLKREQ*	BN35
PEX_CVDD	BG35
PEX_CVDD	BG36
PEX_DVDD	BG38
PEX_DVDD	BH42
PEX_DVDD	BG39
PEX_DVDD	BG41
PEX_DVDD	BG42
PEX_DVDD	BH35
PEX_DVDD	BH36
PEX_DVDD	BH38
PEX_DVDD	BH39
PEX_DVDD	BH41
PEX_HVDD	BJ35
PEX_HVDD	BJ36
PEX_HVDD	BJ38
PEX_HVDD	BJ39
PEX_HVDD	BJ41
PEX_HVDD	BJ42
PEX_HVDD	BK39
PEX_HVDD	BK42
PEX_PLL_HVDD	BK36
PEX_REFCLK	BM35
PEX_REFCLK*	BL35

Ball Name	Ball #
PEX_RST*	BP35
PEX_RX0	BT38
PEX_RX0*	BU38
PEX_RX1	BV38
PEX_RX1*	BV39
PEX_RX10	BV47
PEX_RX10*	BV48
PEX_RX11	BU48
PEX_RX11*	BT48
PEX_RX12	BT50
PEX_RX12*	BU50
PEX_RX13	BV50
PEX_RX13*	BV51
PEX_RX14	BU51
PEX_RX14*	BT51
PEX_RX15	BV53
PEX_RX15*	BV54
PEX_RX2	BU39
PEX_RX2*	BT39
PEX_RX3	BT41
PEX_RX3*	BU41
PEX_RX4	BV41
PEX_RX4*	BV42
PEX_RX5	BU42
PEX_RX5*	BT42
PEX_RX6	BT44
PEX_RX6*	BU44
PEX_RX7	BV44
PEX_RX7*	BV45
PEX_RX8	BU45
PEX_RX8*	BT45
PEX_RX9	BT47
PEX_RX9*	BU47
PEX_TERM	BK45
PEX_TX0	BM36
PEX_TX0*	BN36
PEX_TX1	BN38
PEX_TX1*	BP38
PEX_TX10	BN47
PEX_TX10*	BP47
PEX_TX11	BM47

Ball Name	Ball #
PEX_TX11*	BL47
PEX_TX12	BM48
PEX_TX12*	BN48
PEX_TX13	BN50
PEX_TX13*	BP50
PEX_TX14	BM50
PEX_TX14*	BL50
PEX_TX15	BM51
PEX_TX15*	BN51
PEX_TX2	BM38
PEX_TX2*	BL38
PEX_TX3	BM39
PEX_TX3*	BN39
PEX_TX4	BN41
PEX_TX4*	BP41
PEX_TX5	BM41
PEX_TX5*	BL41
PEX_TX6	BM42
PEX_TX6*	BN42
PEX_TX7	BN44
PEX_TX7*	BP44
PEX_TX8	BM44
PEX_TX8*	BL44
PEX_TX9	BM45
PEX_TX9*	BN45
PEX_WAKE*	BL36
ROM_CS*	BR12
ROM_SCLK	BP12
ROM_SI	BP11
ROM_SO	BR11
NC	BH48
NC	BH21
NC	BJ21
NC	BN20
NC	BN21
NC	BH49
SP_PLLVDD	BG26
STRAP0	BK11
STRAP1	BL11
STRAP2	BM11
STRAP3	BM12

Ball Name	Ball #
STRAP4	BK12
STRAP5	BL12
THERMDN	BT11
THERMDP	BU11
TS_VREF	BH9
USB_DVDD	BH23
USB_DVDD	BH24
USB_HVDD	BG20
USB_HVDD	BG21
USB_L0	BM21
USB_L0*	BL21
USB_L1	BJ20
USB_L1*	BH20
USB_PLL_HVDD	BG23
USB_RBIAS	BK20
USB_SCL	BJ24
USB_SDA	BJ23
USB_TERMPO	BK21
USB_TERMPP1	BL20
USB_VDDP	BM20
VDD	AA14
VDD	AA16
VDD	AA18
VDD	AA20
VDD	AA22
VDD	AA24
VDD	AA26
VDD	AA28
VDD	AA30
VDD	AA32
VDD	AA34
VDD	AA36
VDD	AA38
VDD	AA40
VDD	AA42
VDD	AA44
VDD	AB15
VDD	AB17
VDD	AB19
VDD	AB21
VDD	AB23

Ball Name	Ball #
VDD	AB25
VDD	AB27
VDD	AB29
VDD	AB31
VDD	AB33
VDD	AB35
VDD	AB37
VDD	AB39
VDD	AB41
VDD	AB43
VDD	AB45
VDD	AC14
VDD	AC16
VDD	AC18
VDD	AC20
VDD	AC22
VDD	AC24
VDD	AC26
VDD	AC28
VDD	AC30
VDD	AC32
VDD	AC34
VDD	AC36
VDD	AC38
VDD	AC40
VDD	AC42
VDD	AC44
VDD	AD15
VDD	AD17
VDD	AD19
VDD	AD21
VDD	AD23
VDD	AD25
VDD	AD27
VDD	AD29
VDD	AD31
VDD	AD33
VDD	AD35
VDD	AD37
VDD	AD39
VDD	AD41

Ball Name	Ball #
VDD	AD43
VDD	AD45
VDD	AE14
VDD	AE16
VDD	AE18
VDD	AE20
VDD	AE22
VDD	AE24
VDD	AE26
VDD	AE28
VDD	AE30
VDD	AE32
VDD	AE34
VDD	AE36
VDD	AE38
VDD	AE40
VDD	AE42
VDD	AE44
VDD	AF15
VDD	AF17
VDD	AF19
VDD	AF21
VDD	AF23
VDD	AF25
VDD	AF27
VDD	AF29
VDD	AF31
VDD	AF33
VDD	AF35
VDD	AF37
VDD	AF39
VDD	AF41
VDD	AF43
VDD	AF45
VDD	AG14
VDD	AG16
VDD	AG18
VDD	AG20
VDD	AG22
VDD	AG24
VDD	AG26

Ball Name	Ball #
VDD	AG28
VDD	AG30
VDD	AG32
VDD	AG34
VDD	AG36
VDD	AG38
VDD	AG40
VDD	AG42
VDD	AG44
VDD	AH15
VDD	AH17
VDD	AH19
VDD	AH21
VDD	AH23
VDD	AH25
VDD	AH27
VDD	AH29
VDD	AH31
VDD	AH33
VDD	AH35
VDD	AH37
VDD	AH39
VDD	AH41
VDD	AH43
VDD	AH45
VDD	AJ14
VDD	AJ16
VDD	AJ18
VDD	AJ20
VDD	AJ22
VDD	AJ24
VDD	AJ26
VDD	AJ28
VDD	AJ30
VDD	AJ32
VDD	AJ34
VDD	AJ36
VDD	AJ38
VDD	AJ40
VDD	AJ42
VDD	AJ44



Ball Name	Ball #
VDD	AK15
VDD	AK17
VDD	AK19
VDD	AK21
VDD	AK23
VDD	AK25
VDD	AK27
VDD	AK29
VDD	AK31
VDD	AK33
VDD	AK35
VDD	AK37
VDD	AK39
VDD	AK41
VDD	AK43
VDD	AK45
VDD	AL14
VDD	AL16
VDD	AL18
VDD	AL20
VDD	AL22
VDD	AL24
VDD	AL26
VDD	AL28
VDD	AL30
VDD	AL32
VDD	AL34
VDD	AL36
VDD	AL38
VDD	AL40
VDD	AL42
VDD	AL44
VDD	AM15
VDD	AM17
VDD	AM19
VDD	AM21
VDD	AM23
VDD	AM25
VDD	AM27
VDD	AM29
VDD	AM31

Ball Name	Ball #
VDD	AM33
VDD	AM35
VDD	AM37
VDD	AM39
VDD	AM41
VDD	AM43
VDD	AM45
VDD	AN14
VDD	AN16
VDD	AN18
VDD	AN20
VDD	AN22
VDD	AN24
VDD	AN26
VDD	AN28
VDD	AN30
VDD	AN32
VDD	AN34
VDD	AN36
VDD	AN38
VDD	AN40
VDD	AN42
VDD	AN44
VDD	AP15
VDD	AP17
VDD	AP19
VDD	AP21
VDD	AP23
VDD	AP25
VDD	AP27
VDD	AP29
VDD	AP31
VDD	AP33
VDD	AP35
VDD	AP37
VDD	AP39
VDD	AP41
VDD	AP43
VDD	AP45
VDD	AR14
VDD	AR16

Ball Name	Ball #
VDD	AR18
VDD	AR20
VDD	AR22
VDD	AR24
VDD	AR26
VDD	AR28
VDD	AR30
VDD	AR32
VDD	AR34
VDD	AR36
VDD	AR38
VDD	AR40
VDD	AR42
VDD	AR44
VDD	AT15
VDD	AT17
VDD	AT19
VDD	AT21
VDD	AT23
VDD	AT25
VDD	AT27
VDD	AT29
VDD	AT31
VDD	AT33
VDD	AT35
VDD	AT37
VDD	AT39
VDD	AT41
VDD	AT43
VDD	AT45
VDD	AU14
VDD	AU16
VDD	AU18
VDD	AU20
VDD	AU22
VDD	AU24
VDD	AU26
VDD	AU28
VDD	AU30
VDD	AU32
VDD	AU34

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
VDD	AU36	VDD	AY23	VDD	BB41
VDD	AU38	VDD	AY25	VDD	BB43
VDD	AU40	VDD	AY27	VDD	BB45
VDD	AU42	VDD	AY29	VDD	BC14
VDD	AU44	VDD	AY31	VDD	BC16
VDD	AV15	VDD	AY33	VDD	BC18
VDD	AV17	VDD	AY35	VDD	BC20
VDD	AV19	VDD	AY37	VDD	BC22
VDD	AV21	VDD	AY39	VDD	BC24
VDD	AV23	VDD	AY41	VDD	BC26
VDD	AV25	VDD	AY43	VDD	BC28
VDD	AV27	VDD	AY45	VDD	BC30
VDD	AV29	VDD	BA14	VDD	BC32
VDD	AV31	VDD	BA16	VDD	BC34
VDD	AV33	VDD	BA18	VDD	BC36
VDD	AV35	VDD	BA20	VDD	BC38
VDD	AV37	VDD	BA22	VDD	BC40
VDD	AV39	VDD	BA24	VDD	BC42
VDD	AV41	VDD	BA26	VDD	BC44
VDD	AV43	VDD	BA28	VDD	BD15
VDD	AV45	VDD	BA30	VDD	BD17
VDD	AW14	VDD	BA32	VDD	BD19
VDD	AW16	VDD	BA34	VDD	BD21
VDD	AW18	VDD	BA36	VDD	BD23
VDD	AW20	VDD	BA38	VDD	BD25
VDD	AW22	VDD	BA40	VDD	BD27
VDD	AW24	VDD	BA42	VDD	BD29
VDD	AW26	VDD	BA44	VDD	BD31
VDD	AW28	VDD	BB15	VDD	BD33
VDD	AW30	VDD	BB17	VDD	BD35
VDD	AW32	VDD	BB19	VDD	BD37
VDD	AW34	VDD	BB21	VDD	BD39
VDD	AW36	VDD	BB23	VDD	BD41
VDD	AW38	VDD	BB25	VDD	BD43
VDD	AW40	VDD	BB27	VDD	BD45
VDD	AW42	VDD	BB29	VDD	BE14
VDD	AW44	VDD	BB31	VDD	BE16
VDD	AY15	VDD	BB33	VDD	BE18
VDD	AY17	VDD	BB35	VDD	BE20
VDD	AY19	VDD	BB37	VDD	BE22
VDD	AY21	VDD	BB39	VDD	BE24

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
VDD	BE26	VDD	R44	VDD	V31
VDD	BE28	VDD	T15	VDD	V33
VDD	BE30	VDD	T17	VDD	V35
VDD	BE32	VDD	T19	VDD	V37
VDD	BE34	VDD	T21	VDD	V39
VDD	BE36	VDD	T23	VDD	V41
VDD	BE38	VDD	T25	VDD	V43
VDD	BE40	VDD	T27	VDD	V45
VDD	BE42	VDD	T29	VDD	W14
VDD	BE44	VDD	T31	VDD	W16
VDD	P15	VDD	T33	VDD	W18
VDD	P17	VDD	T35	VDD	W20
VDD	P19	VDD	T37	VDD	W22
VDD	P21	VDD	T39	VDD	W24
VDD	P23	VDD	T41	VDD	W26
VDD	P25	VDD	T43	VDD	W28
VDD	P27	VDD	T45	VDD	W30
VDD	P29	VDD	U14	VDD	W32
VDD	P31	VDD	U16	VDD	W34
VDD	P33	VDD	U18	VDD	W36
VDD	P35	VDD	U20	VDD	W38
VDD	P37	VDD	U22	VDD	W40
VDD	P39	VDD	U24	VDD	W42
VDD	P41	VDD	U26	VDD	W44
VDD	P43	VDD	U28	VDD	Y15
VDD	P45	VDD	U30	VDD	Y17
VDD	R14	VDD	U32	VDD	Y19
VDD	R16	VDD	U34	VDD	Y21
VDD	R18	VDD	U36	VDD	Y23
VDD	R20	VDD	U38	VDD	Y25
VDD	R22	VDD	U40	VDD	Y27
VDD	R24	VDD	U42	VDD	Y29
VDD	R26	VDD	U44	VDD	Y31
VDD	R28	VDD	V15	VDD	Y33
VDD	R30	VDD	V17	VDD	Y35
VDD	R32	VDD	V19	VDD	Y37
VDD	R34	VDD	V21	VDD	Y39
VDD	R36	VDD	V23	VDD	Y41
VDD	R38	VDD	V25	VDD	Y43
VDD	R40	VDD	V27	VDD	Y45
VDD	R42	VDD	V29	VDD Sense	BR53

Ball Name	Ball #
VID_PLLVDD	BG27
XSN_PLLVDD	BH32
XTAL_IN	BV12
XTAL_OUT	BV11
XTAL_OUTBUFF	BU12

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Gigabyte Desktop 2018-08-12 23:50:58



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58																																																																																																																																																																																																																																																																										
1	A	GND	GND	F8C_D05	F8C_D55	F8C_D54	F8C_D63	F8C_D00V1	F8C_D12	F8C_D05_W0V	F8C_D42	F8C_D05_W0V	F8C_D00	F8C_D002	GND	F8C_D004	F8C_D007	GND	F8C_D003	F8C_D001	GND	F8C_D004	F8C_D006	GND	F8C_D003	F8C_D007	GND	F8C_D004	F8C_D005	F8C_D55	GND	F8C_D42	F8C_D006	GND	F8C_D004	F8C_D009	GND	F8C_D18	F8C_D15	F8C_D16	F8C_D05_W0V	F8C_D002	F8C_D003	F8C_D001	F8C_D002	GND	F8C_D003	F8C_D005	GND	F8C_D002	GND	F8C_D006	GND	F8C_D001	GND	A	1																																																																																																																																																																																																																																																																											
2	B	GND	GND	F8C_D00V1	GND	GND	F8C_D61	F8C_D04_W0V	GND	F8C_D43	F8C_D006	GND	F8C_D004	F8C_D002	GND	F8C_D004	F8C_D007	GND	F8C_D003	F8C_D001	GND	F8C_D004	F8C_D006	GND	F8C_D003	F8C_D007	GND	F8C_D004	F8C_D005	GND	F8C_D55	GND	F8C_D42	F8C_D006	GND	F8C_D004	F8C_D009	GND	F8C_D18	F8C_D15	F8C_D16	F8C_D05_W0V	F8C_D002	F8C_D003	F8C_D001	F8C_D002	GND	F8C_D003	F8C_D005	GND	F8C_D002	GND	F8C_D006	GND	F8C_D001	GND	B	2																																																																																																																																																																																																																																																																										
3	C	GND	F8C_D00V1	F8C_D007	F8C_D53	GND	F8C_D62	F8C_D40	F8C_D58	F8C_D44	F8C_D57	GND	F8C_D004	F8C_D009	GND	F8C_D004	F8C_D007	GND	F8C_D003	F8C_D001	GND	F8C_D004	F8C_D006	GND	F8C_D003	F8C_D007	GND	F8C_D004	F8C_D005	GND	F8C_D55	GND	F8C_D42	F8C_D006	GND	F8C_D004	F8C_D009	GND	F8C_D18	F8C_D15	F8C_D16	F8C_D05_W0V	F8C_D002	F8C_D003	F8C_D001	F8C_D002	GND	F8C_D003	F8C_D005	GND	F8C_D002	GND	F8C_D006	GND	F8C_D001	GND	C	3																																																																																																																																																																																																																																																																										
4	D	GND	GND	GND	F8C_D05_W0V	GND	F8C_D60	F8C_D56	GND	F8C_D44	F8C_D57	GND	F8C_D004	F8C_D009	GND	F8C_D004	F8C_D007	GND	F8C_D003	F8C_D001	GND	F8C_D004	F8C_D006	GND	F8C_D003	F8C_D007	GND	F8C_D004	F8C_D005	GND	F8C_D55	GND	F8C_D42	F8C_D006	GND	F8C_D004	F8C_D009	GND	F8C_D18	F8C_D15	F8C_D16	F8C_D05_W0V	F8C_D002	F8C_D003	F8C_D001	F8C_D002	GND	F8C_D003	F8C_D005	GND	F8C_D002	GND	F8C_D006	GND	F8C_D001	GND	D	4																																																																																																																																																																																																																																																																										
5	E	F8C_D002	F8C_D009	F8C_D00V1	F8C_D59	F8C_D48	F8C_D49	GND	F8C_D57	F8C_D41	F8C_D56	F8C_D09	F8C_D01	F8C_D02	GND	F8C_D02	F8C_D02	GND	F8C_D02	F8C_D02	GND	F8C_D02	F8C_D02	GND	F8C_D02	F8C_D02	GND	F8C_D02	F8C_D02	GND	F8C_D55	GND	F8C_D42	F8C_D006	GND	F8C_D004	F8C_D009	GND	F8C_D18	F8C_D15	F8C_D16	F8C_D05_W0V	F8C_D002	F8C_D003	F8C_D001	F8C_D002	GND	F8C_D003	F8C_D005	GND	F8C_D002	GND	F8C_D006	GND	F8C_D001	GND	E	5																																																																																																																																																																																																																																																																										
6	F	F8C_D002	F8C_D002	F8C_D002	F8C_D59	F8C_D48	GND	F8C_D57	F8C_D41	F8C_D56	F8C_D09	F8C_D01	F8C_D02	GND	F8C_D02	F8C_D02	GND	F8C_D02	F8C_D02	GND	F8C_D02	F8C_D02	GND	F8C_D02	F8C_D02	GND	F8C_D02	F8C_D02	GND	F8C_D55	GND	F8C_D42	F8C_D006	GND	F8C_D004	F8C_D009	GND	F8C_D18	F8C_D15	F8C_D16	F8C_D05_W0V	F8C_D002	F8C_D003	F8C_D001	F8C_D002	GND	F8C_D003	F8C_D005	GND	F8C_D002	GND	F8C_D006	GND	F8C_D001	GND	F	6																																																																																																																																																																																																																																																																											
7	G	GND	GND	GND	GND	F8C_D59	F8C_D56	F8C_D56	F8C_D45	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	F8C_D55	GND	F8C_D42	F8C_D006	GND	F8C_D004	F8C_D009	GND	F8C_D18	F8C_D15	F8C_D16	F8C_D05_W0V	F8C_D002	F8C_D003	F8C_D001	F8C_D002	GND	F8C_D003	F8C_D005	GND	F8C_D002	GND	F8C_D006	GND	F8C_D001	GND	G	7																																																																																																																																																																																																																																																																										
8	H	F8C_D002	F8C_D001	F8C_D003	F8C_D001	F8C_D001	F8C_D001	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005	F8C_D005



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