

PG150-C03

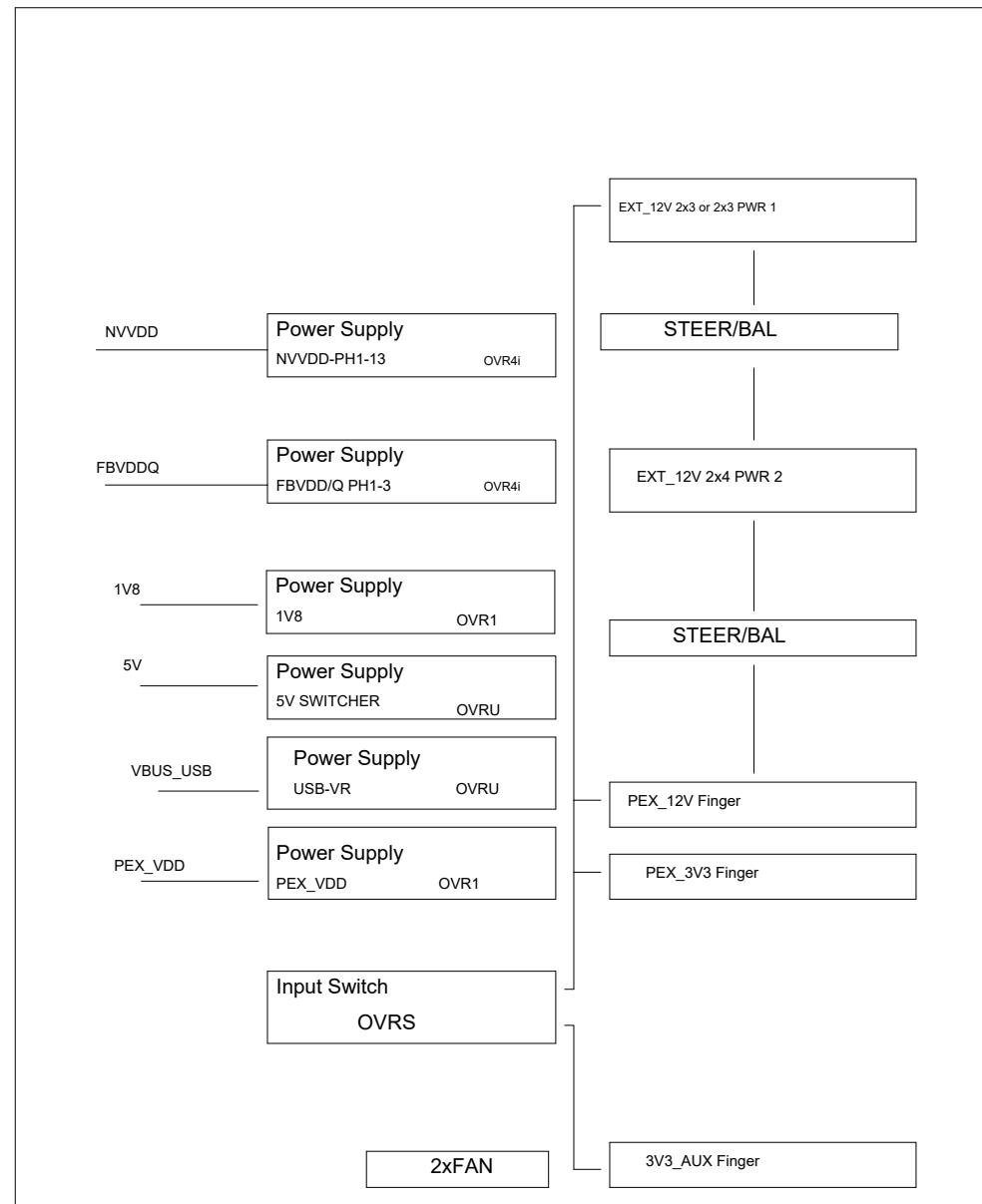
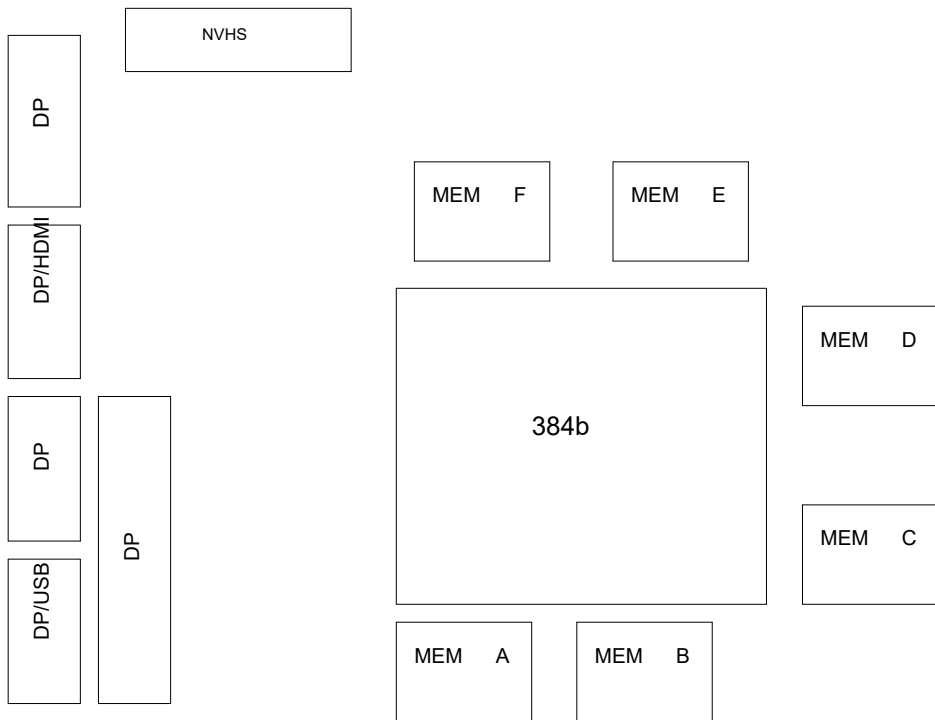
384b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

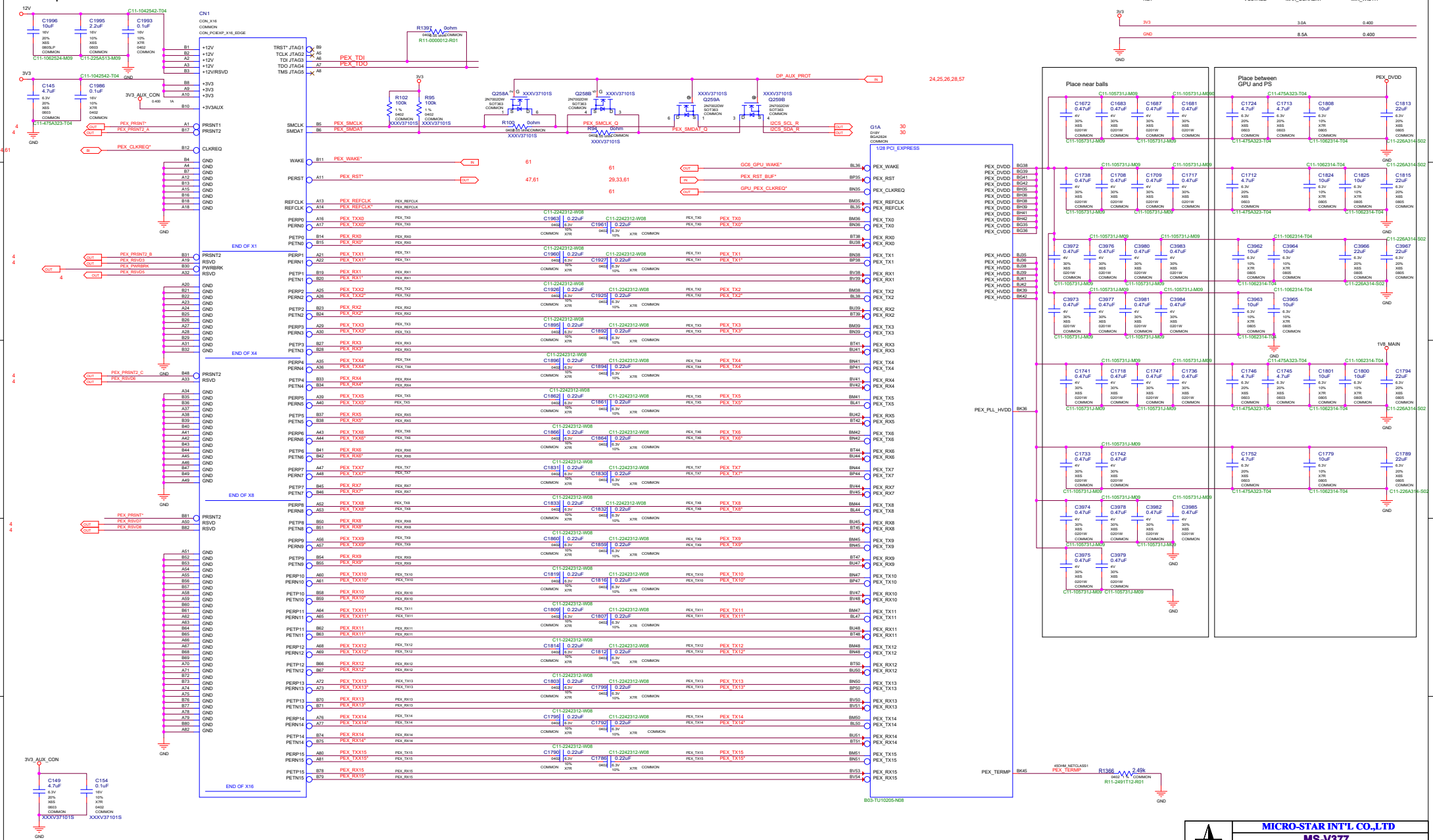
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Block Diagram



## PCI Express



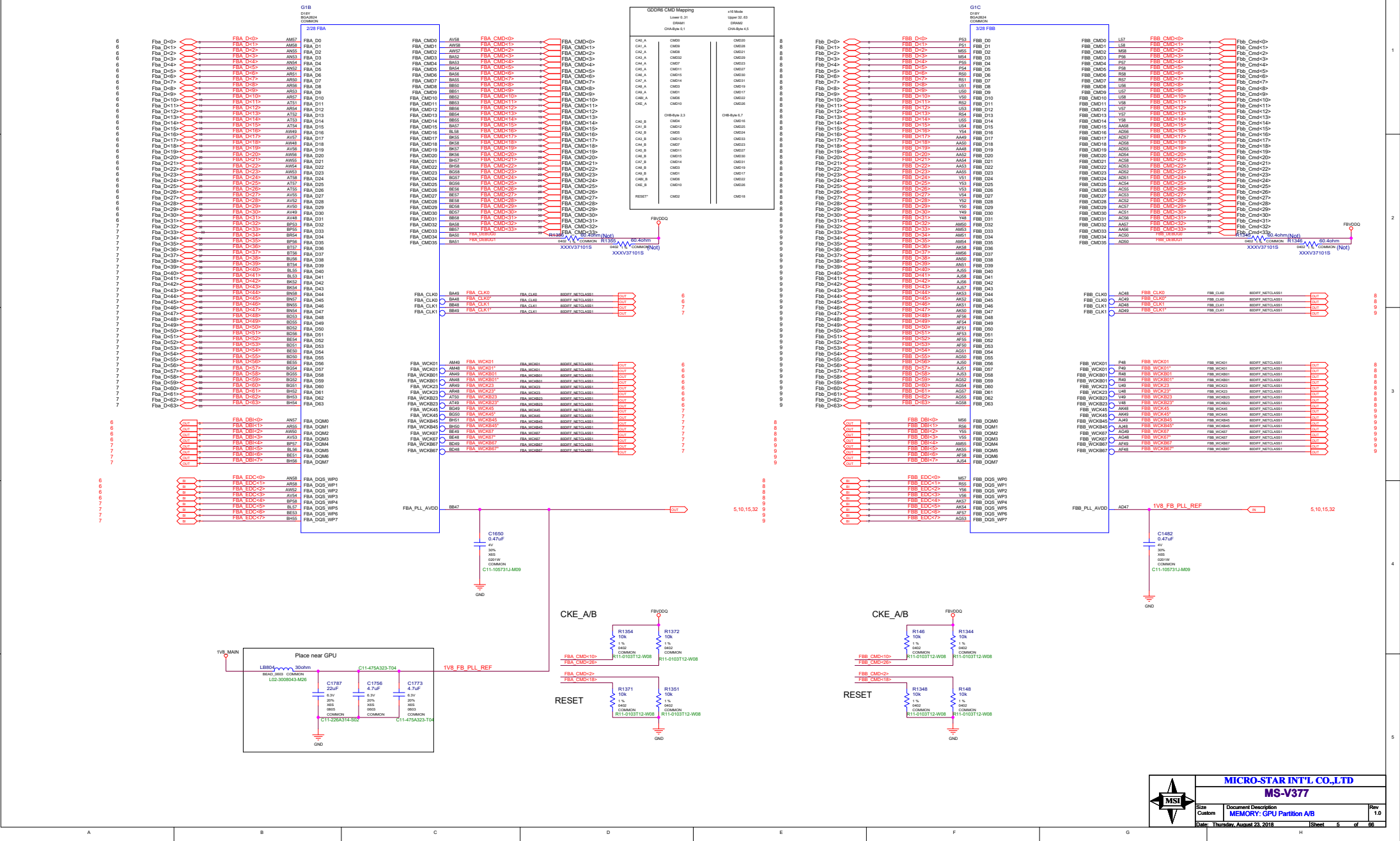
**MICRO-STAR INT'L CO.,LTD**  
**MS-V377**

Size Custom	Document Description <b>MEMORY: GPU Partition A/B</b>	Rev 1.0
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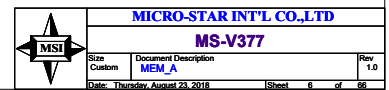
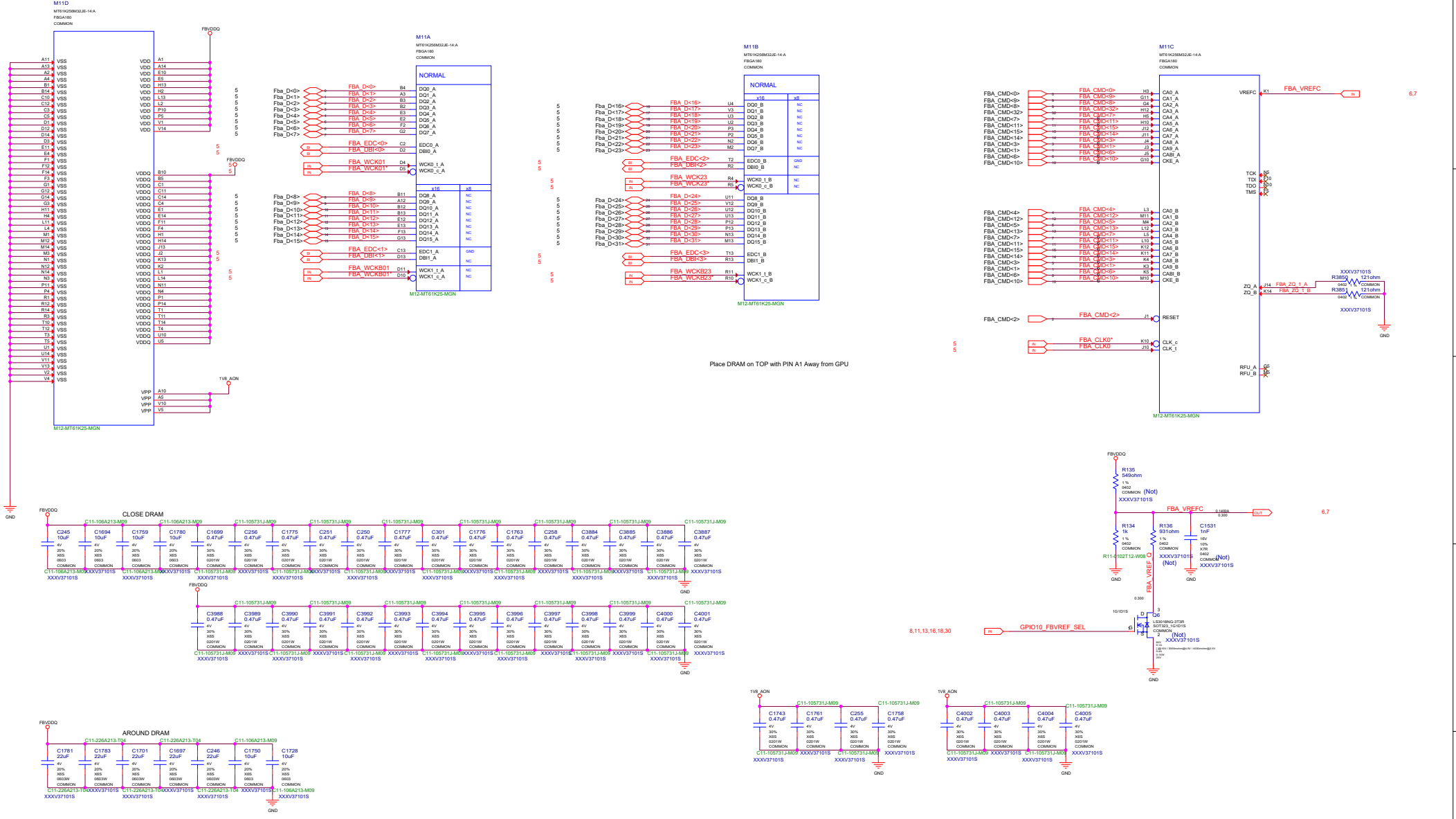
## PCI TERM

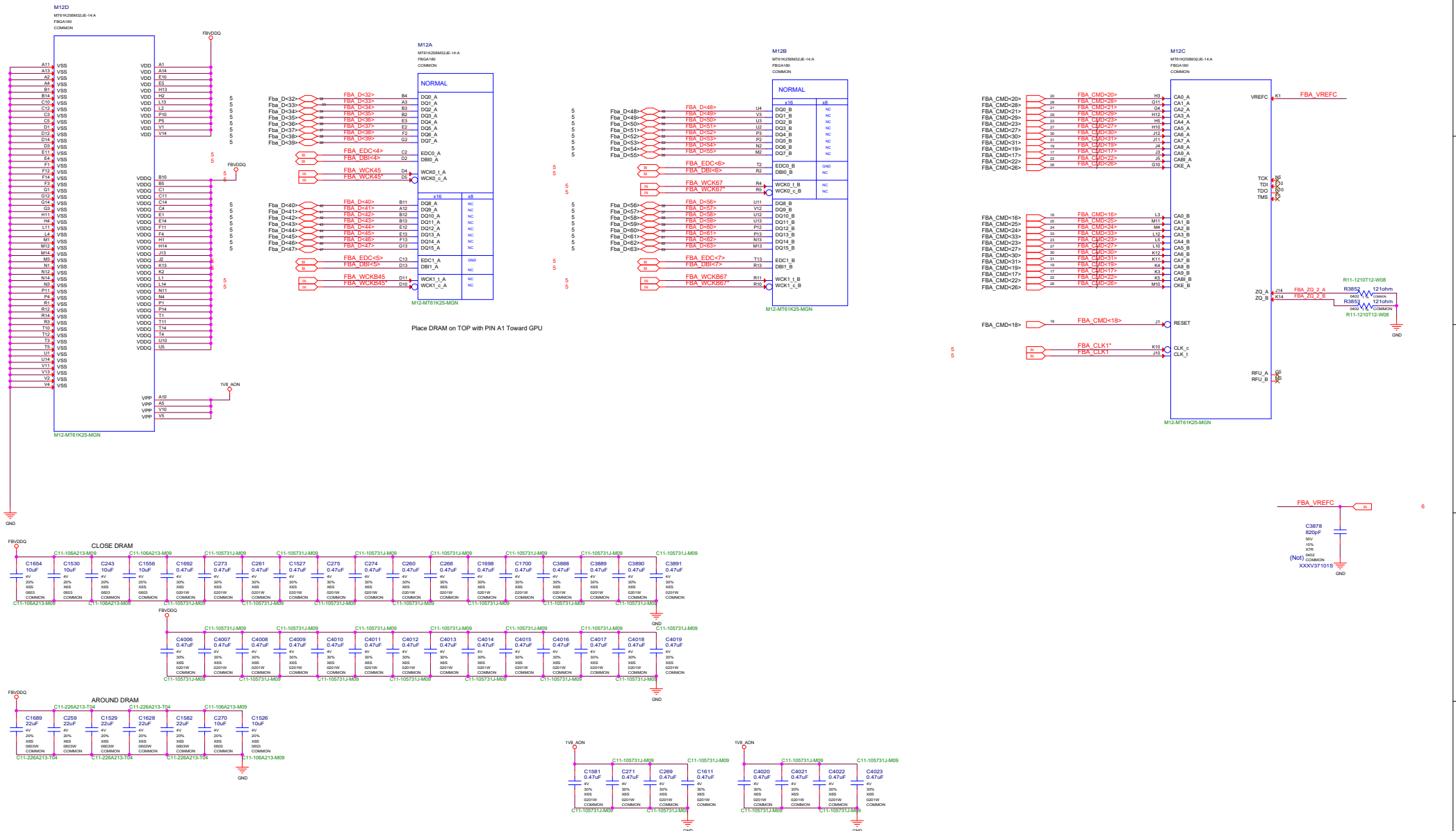


# MEMORY: GPU Partition A/B

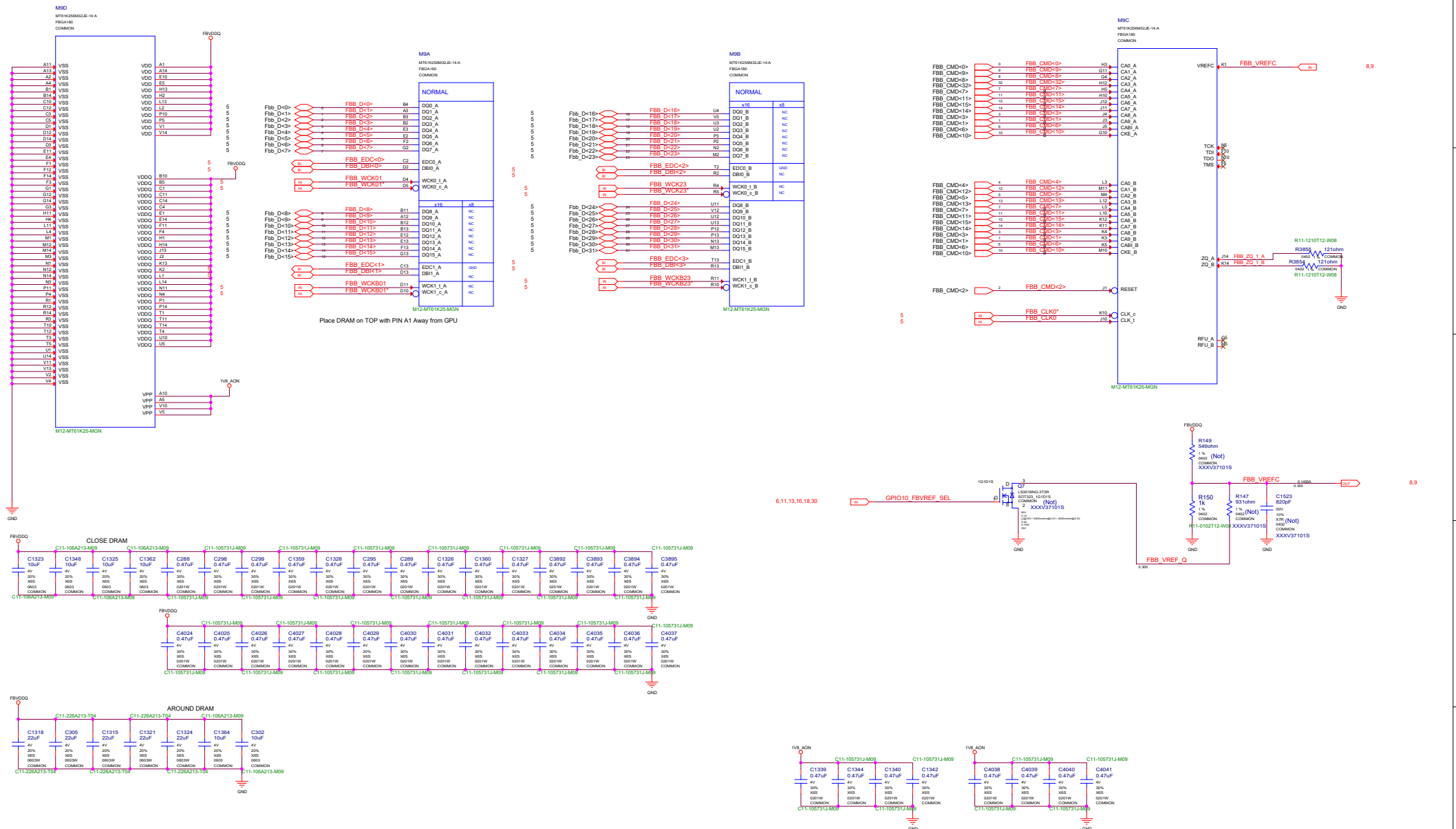


MEMORY: FBA Partition 31..0

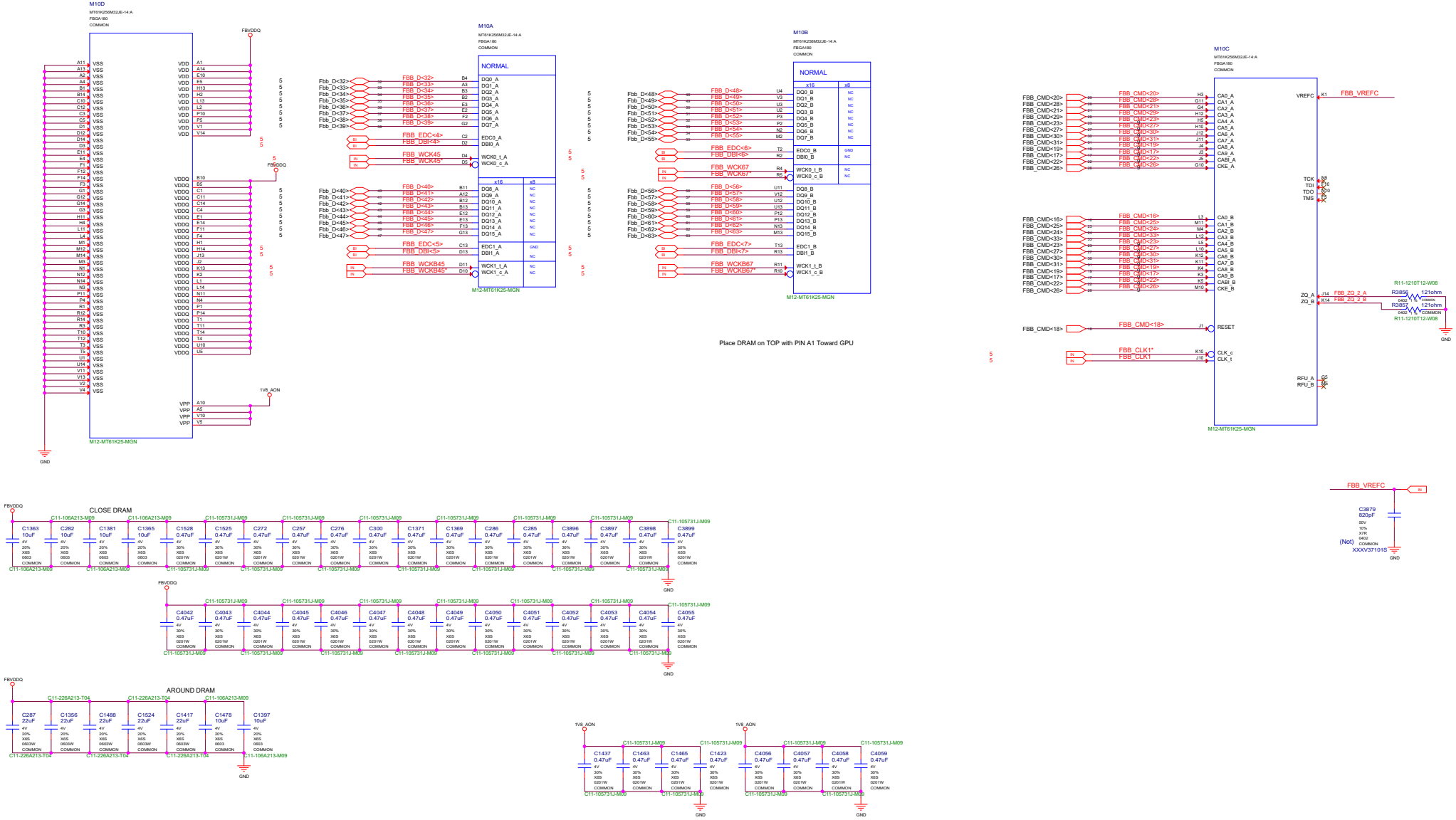




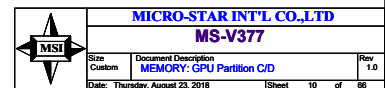
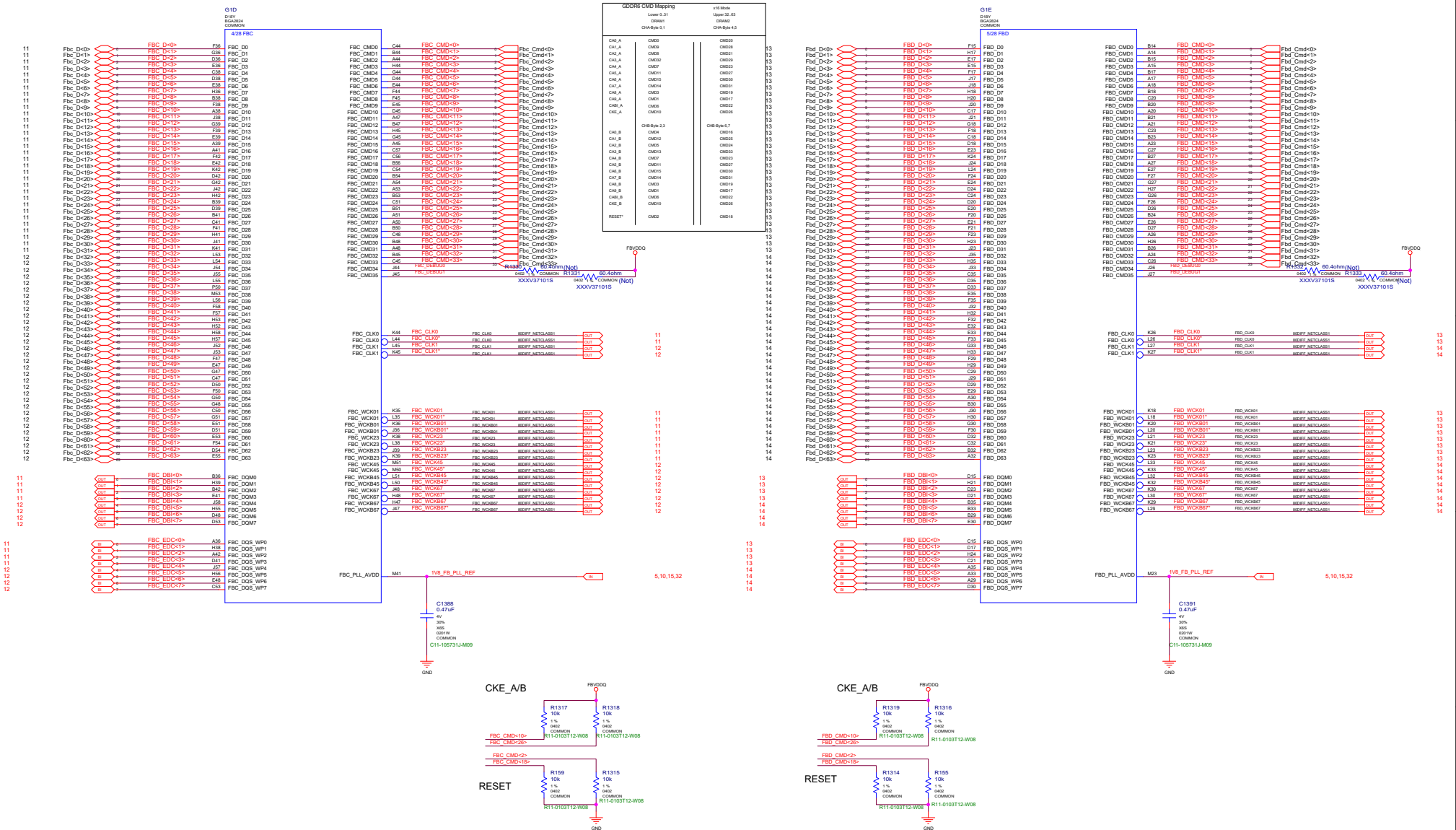
# MEMORY: FBB Partition 31.0



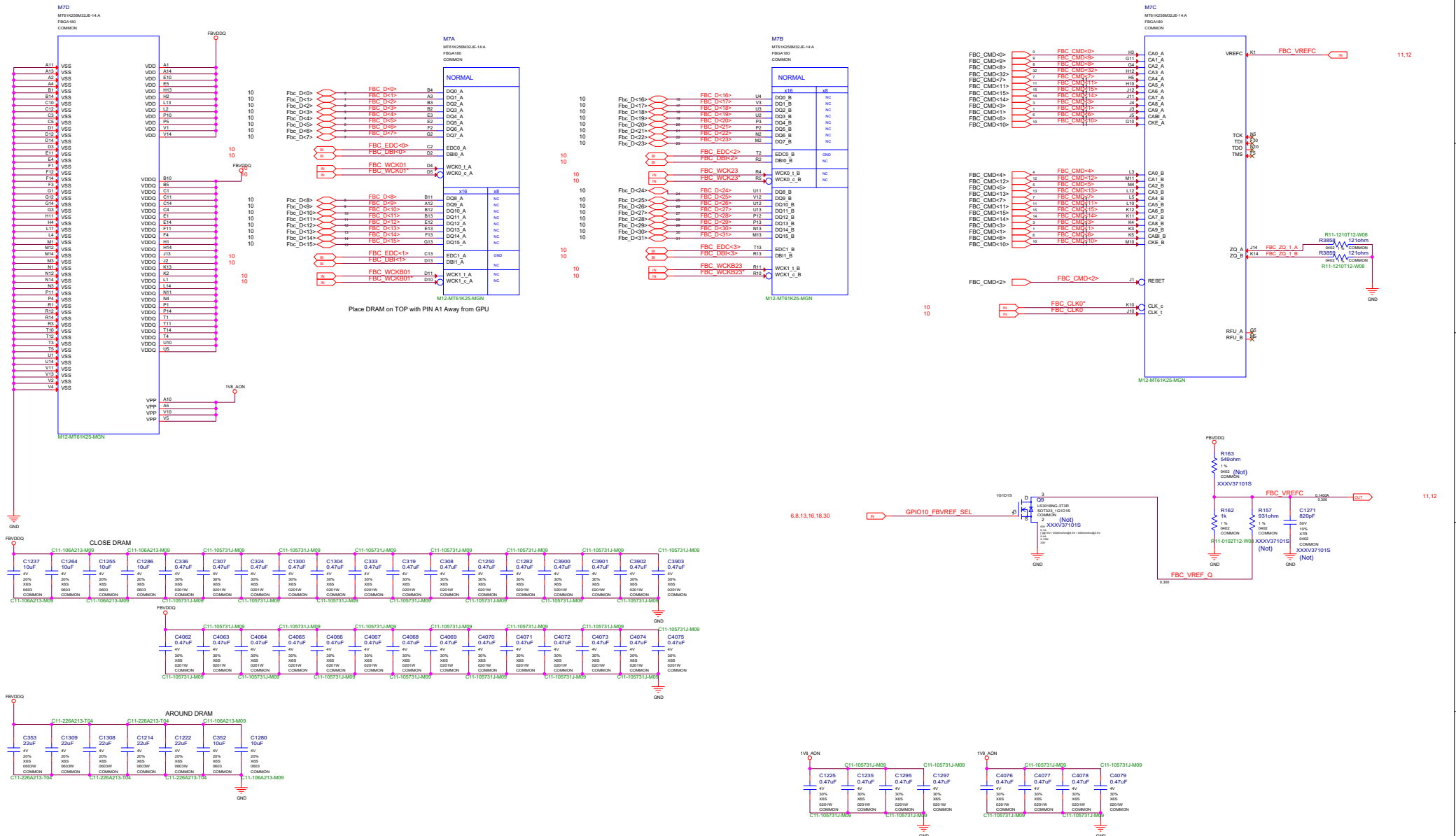




MEMORY: GPU Partition C/D

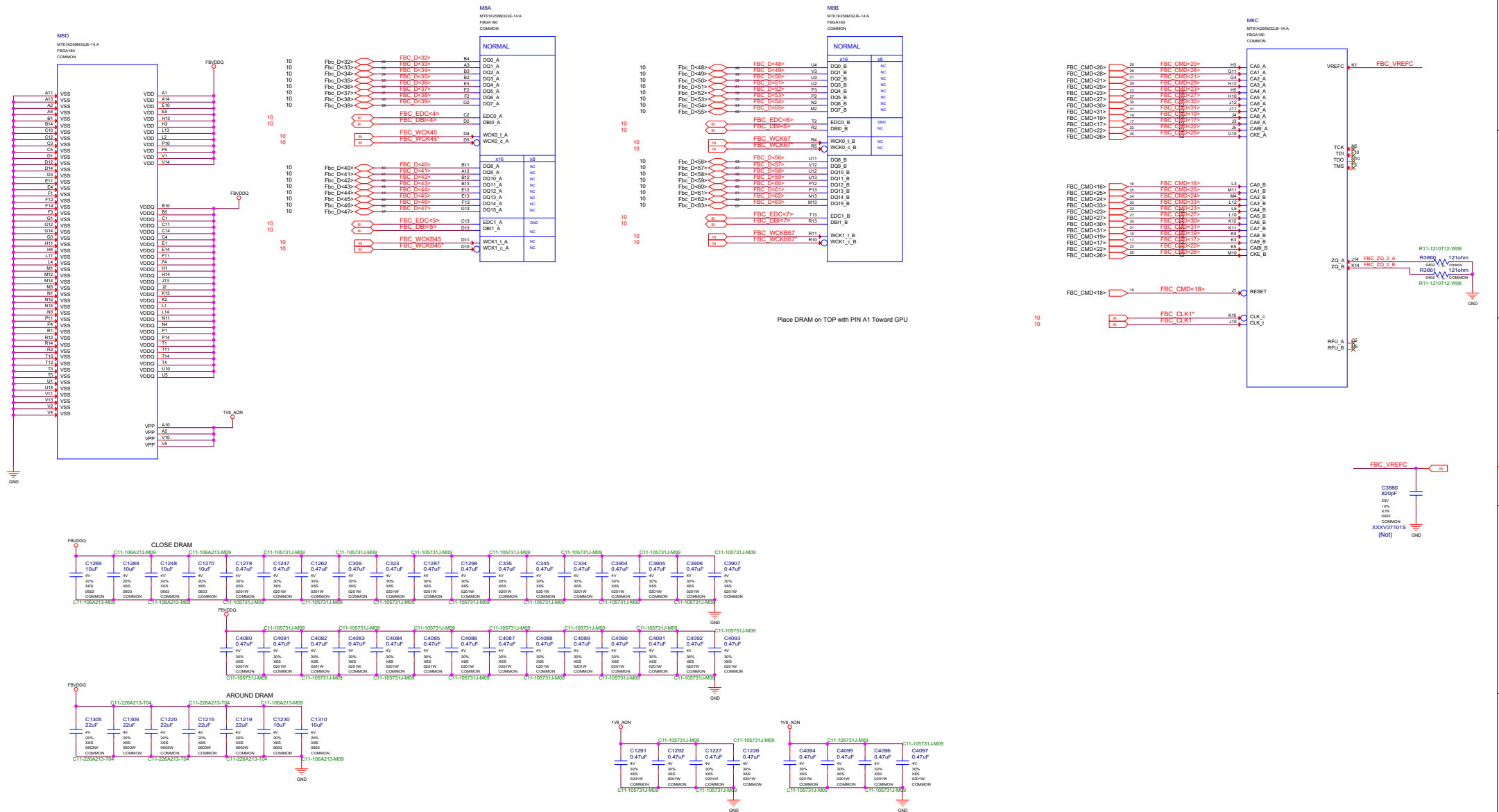


MEMORY: FBC Partition 31..0

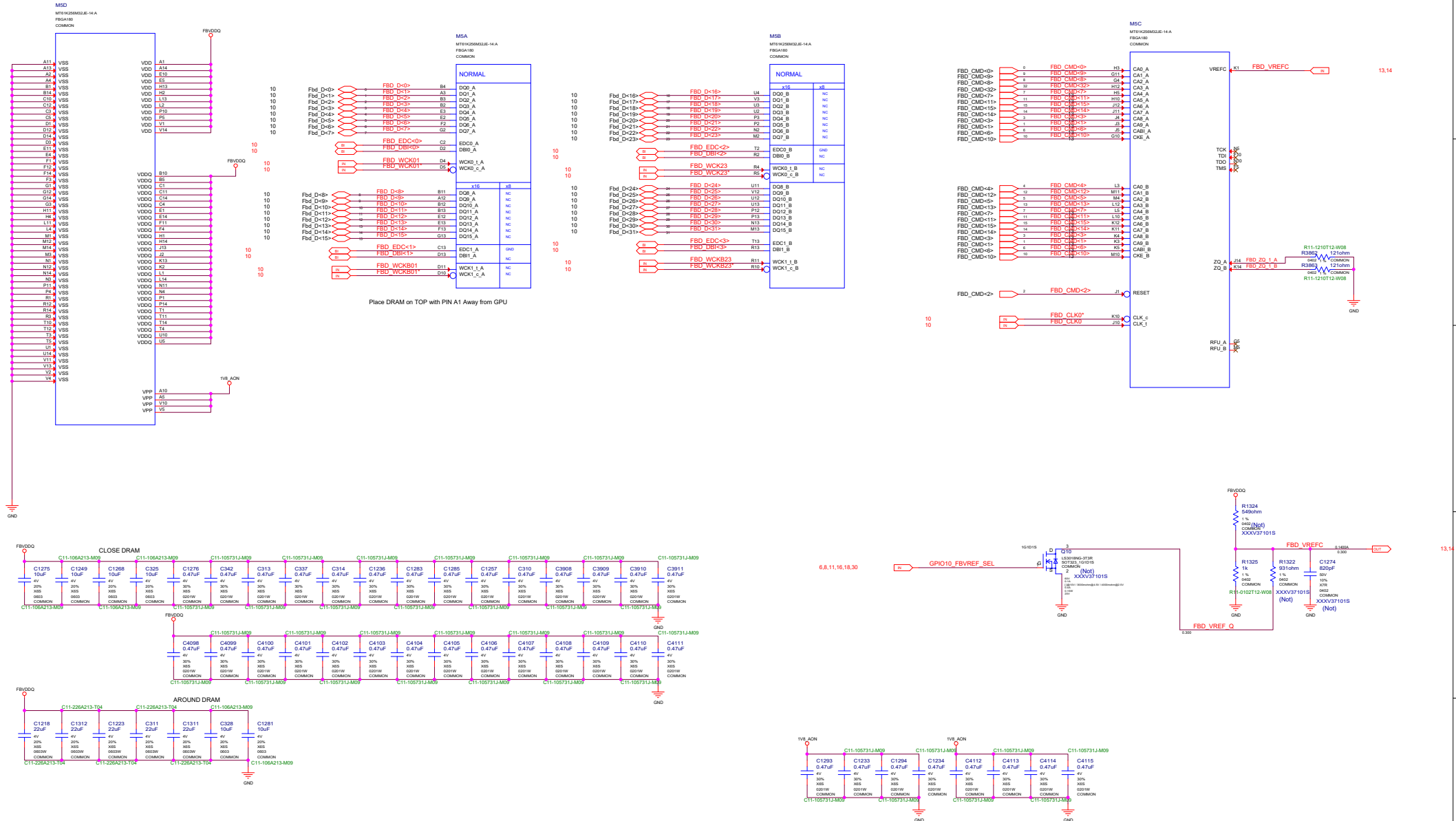


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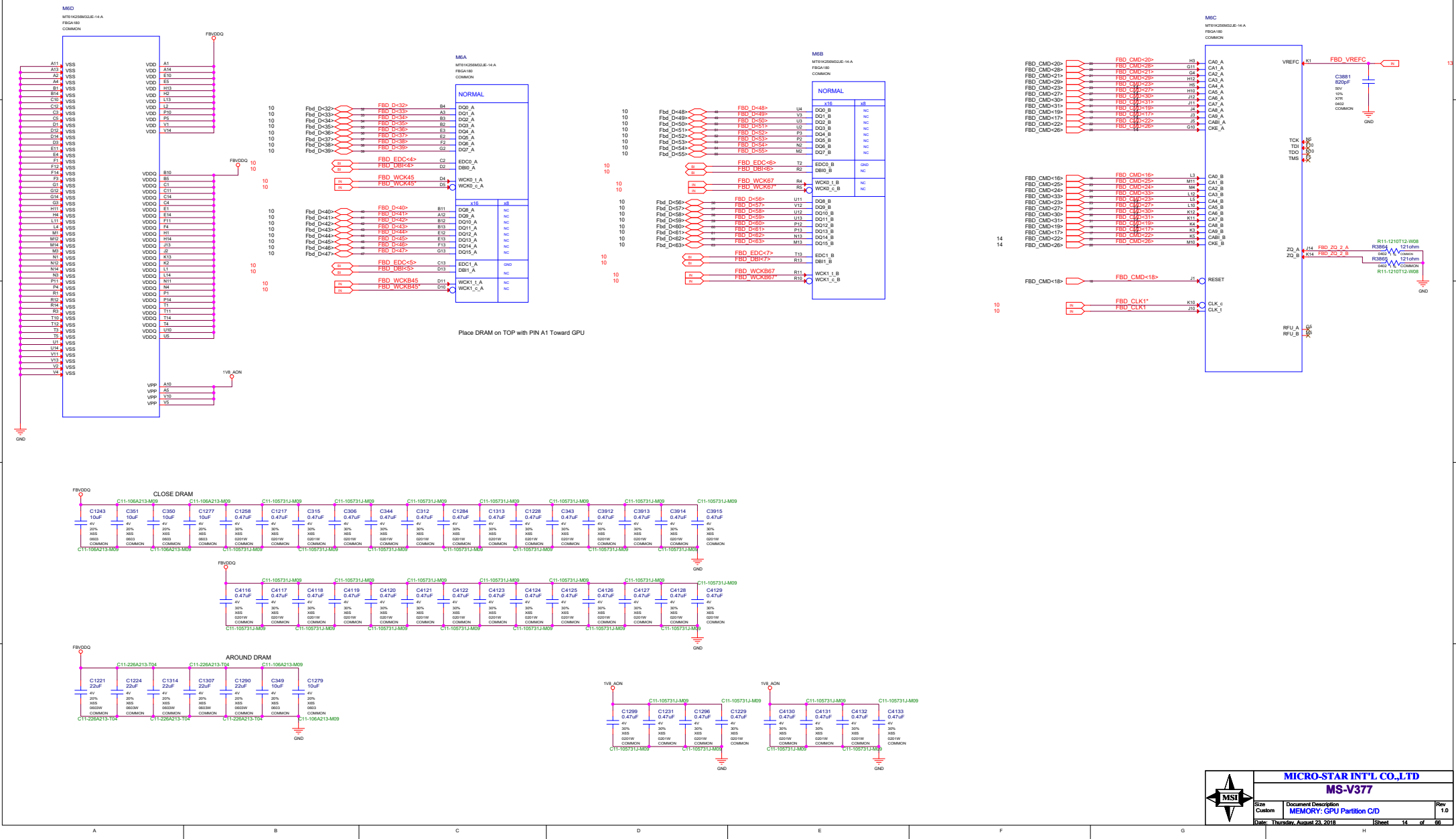
Size Custom	Document Description <b>MEMORY: GPU Partition C</b>	Rev 1.0
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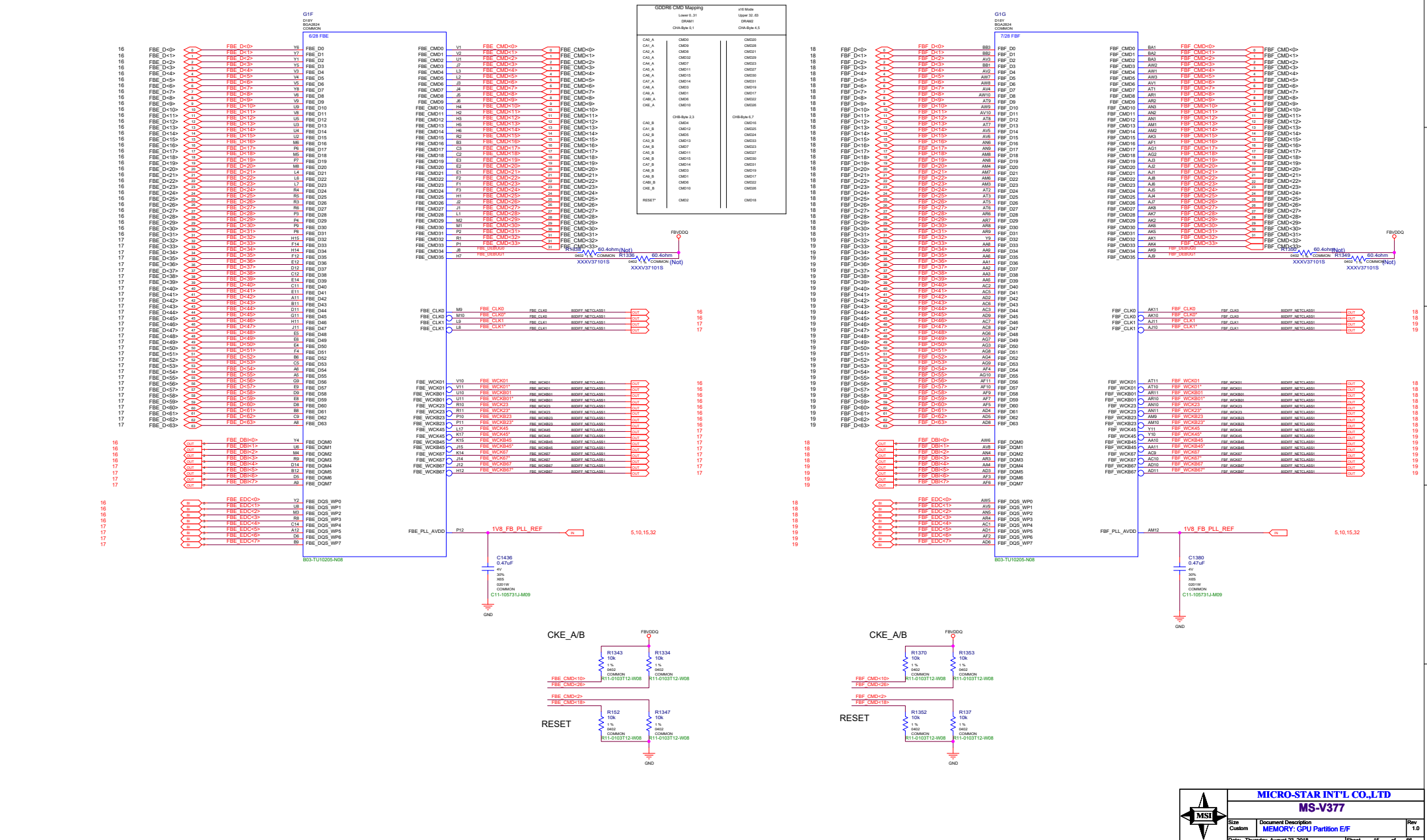


# MEMORY: FBD Partition 31.0

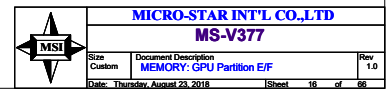
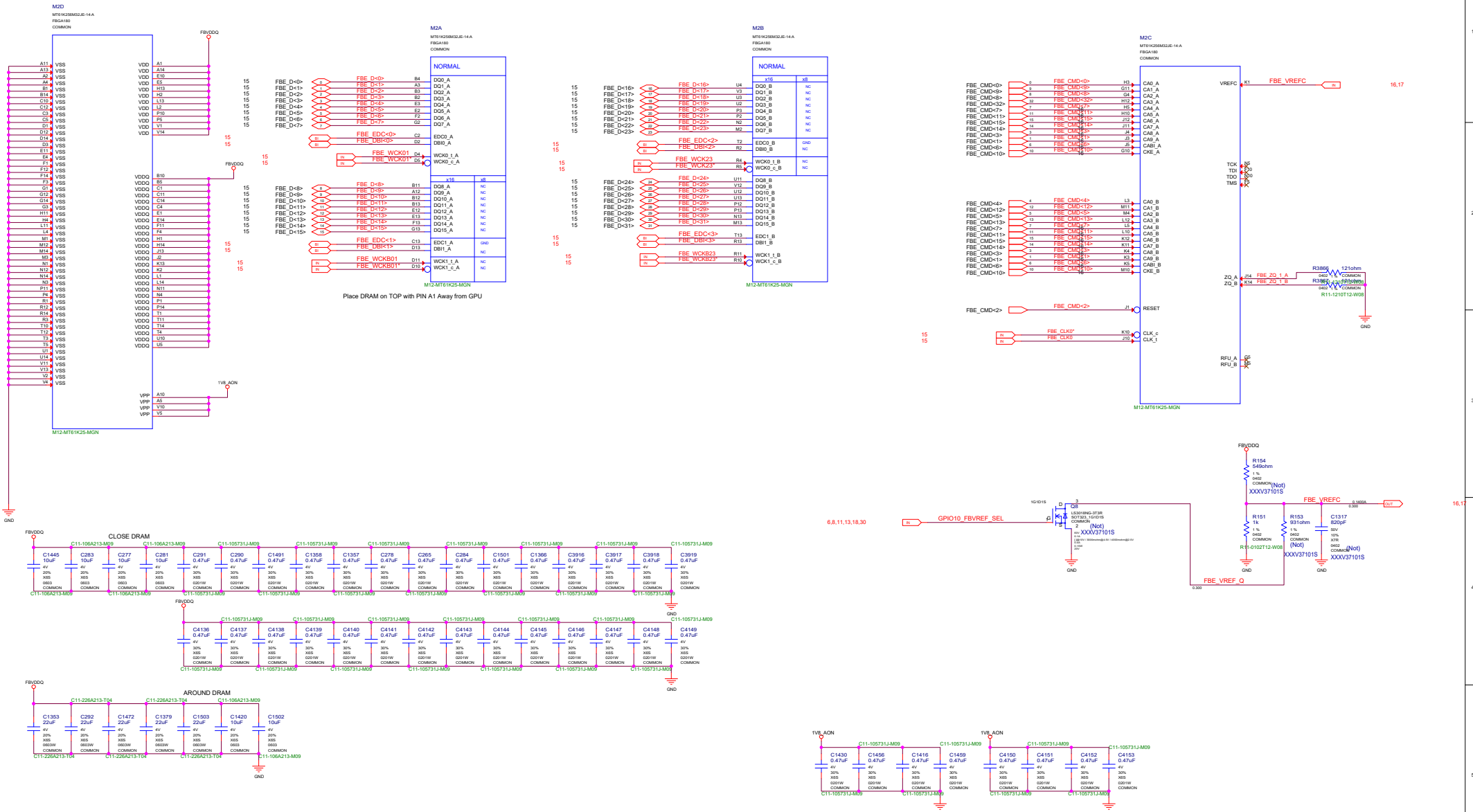


MEMORY: FBD Partition 63..32





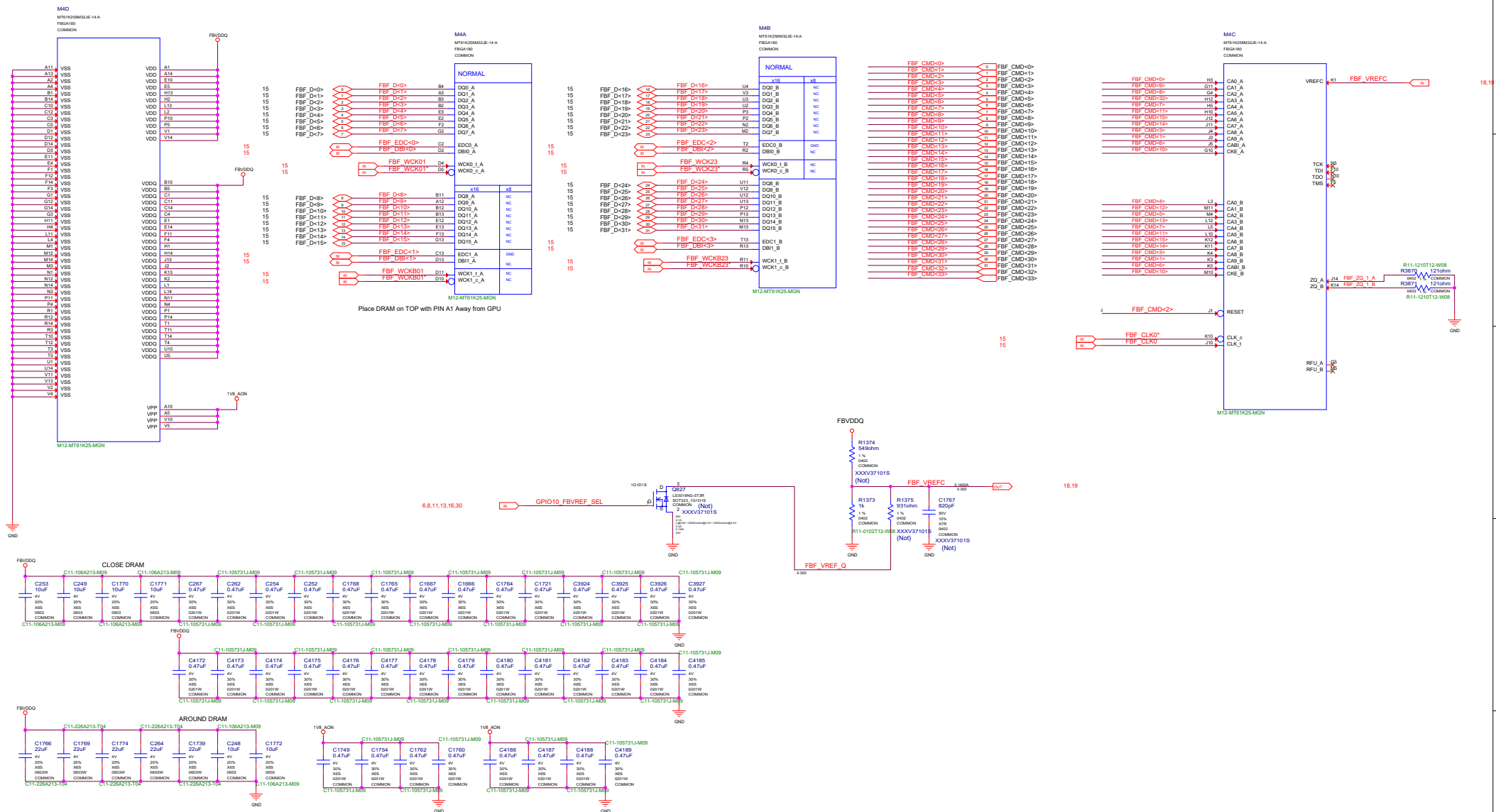
MEMORY: FBE Partition 31..0



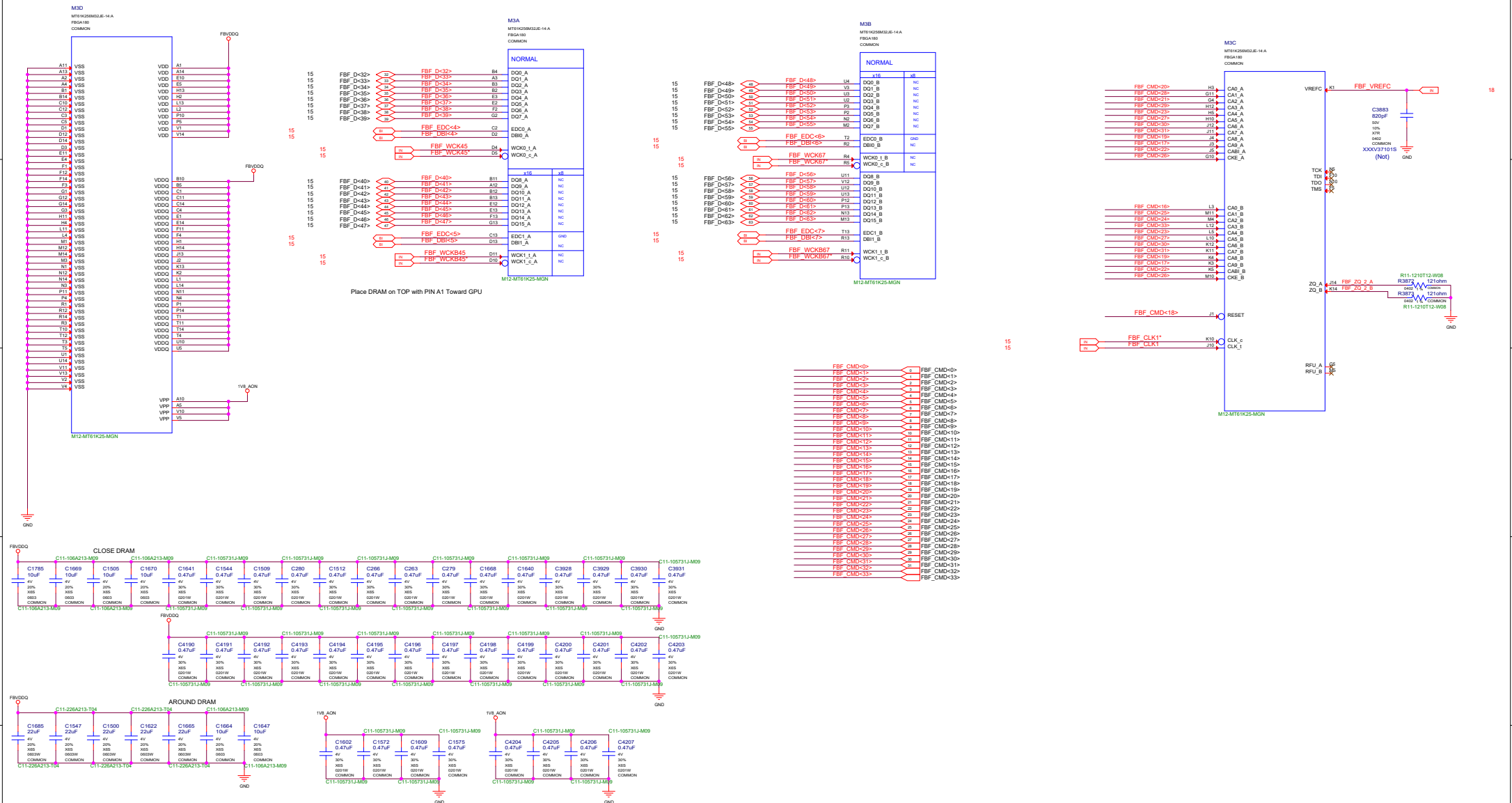




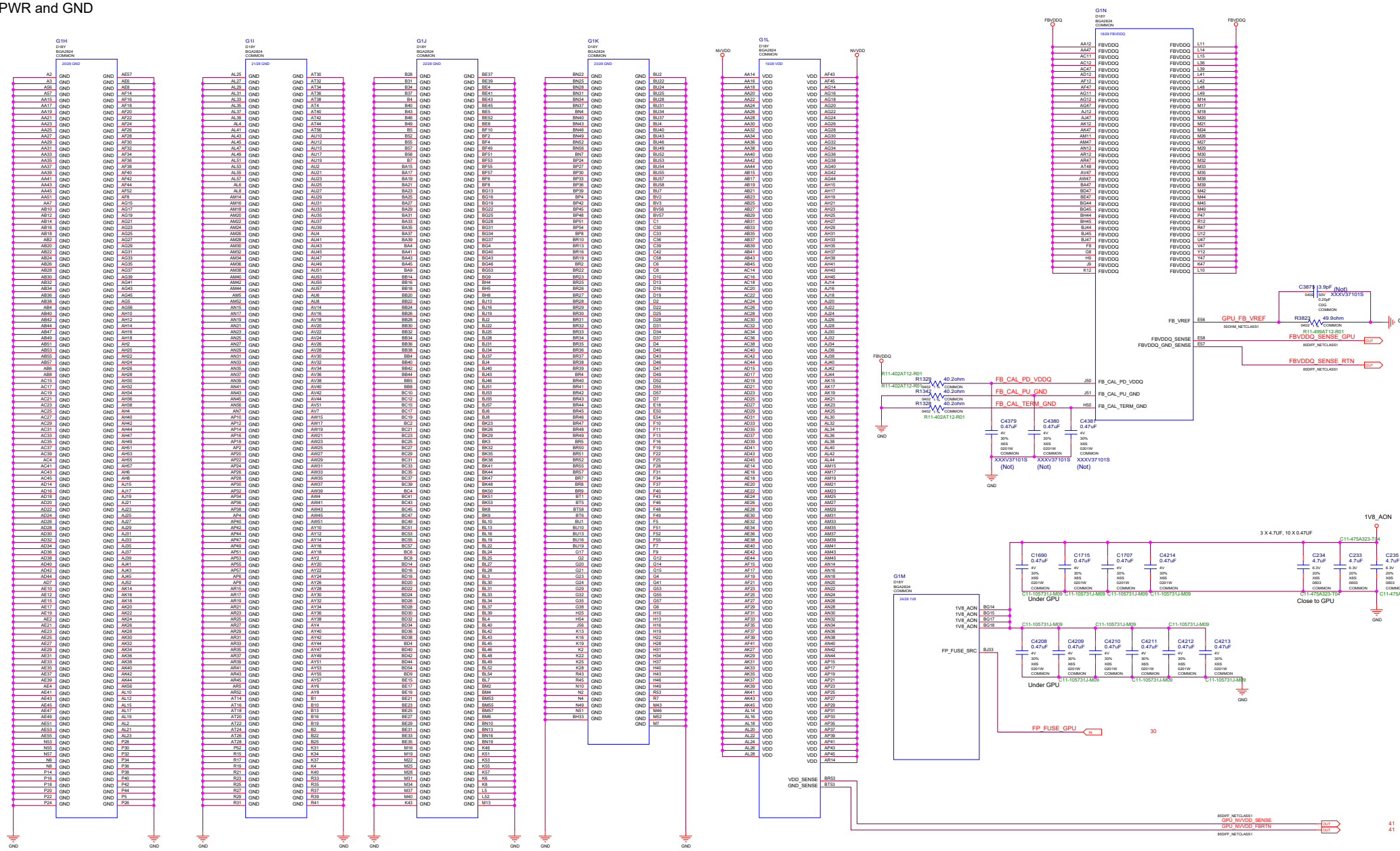
MEMORY: FBF Partition 31..0



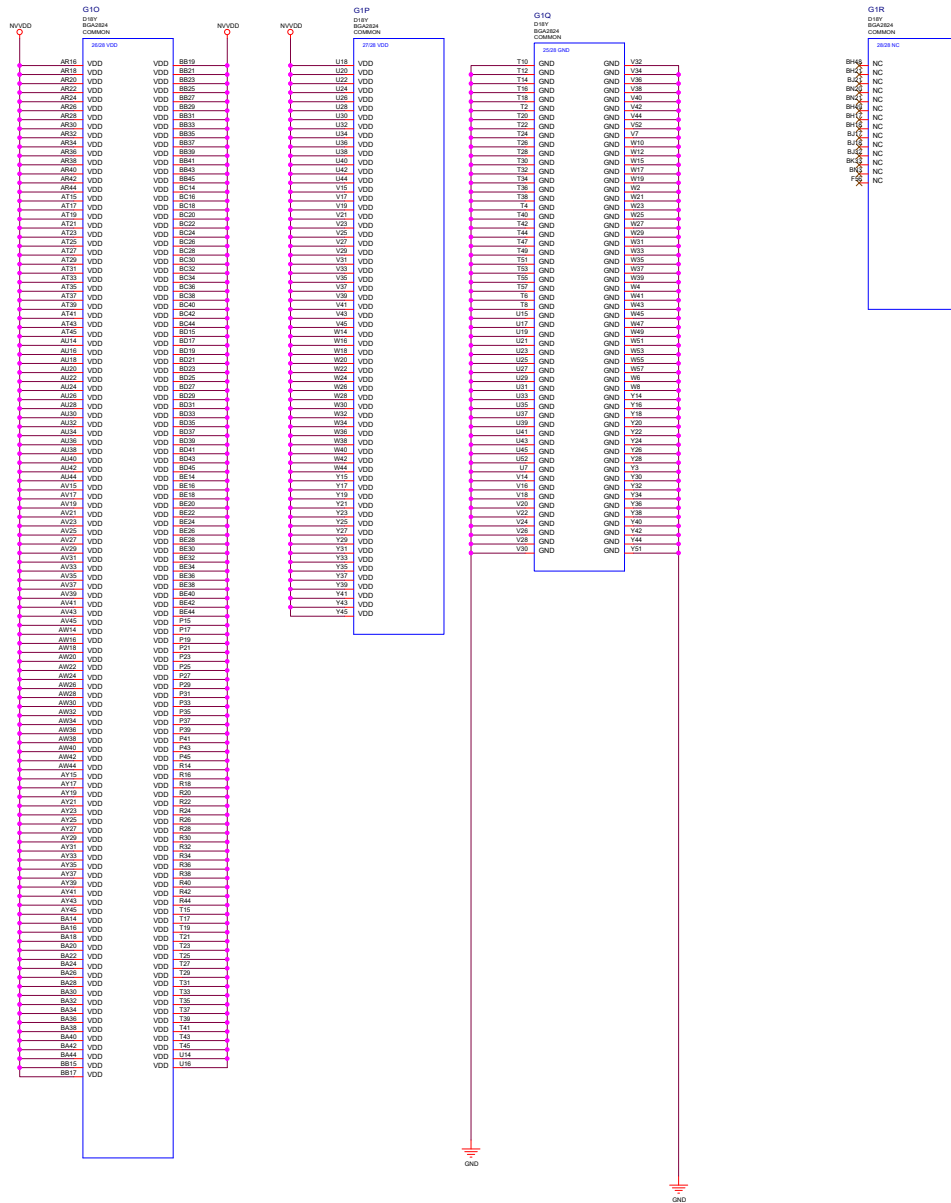
MEMORY: FBF Partition 63..32



## GPU PWR and GND

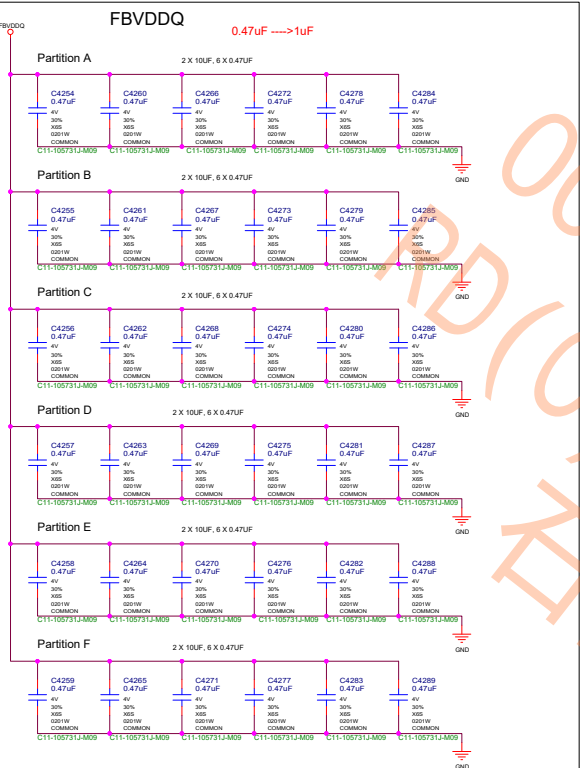


## GPU PWR GND NCs



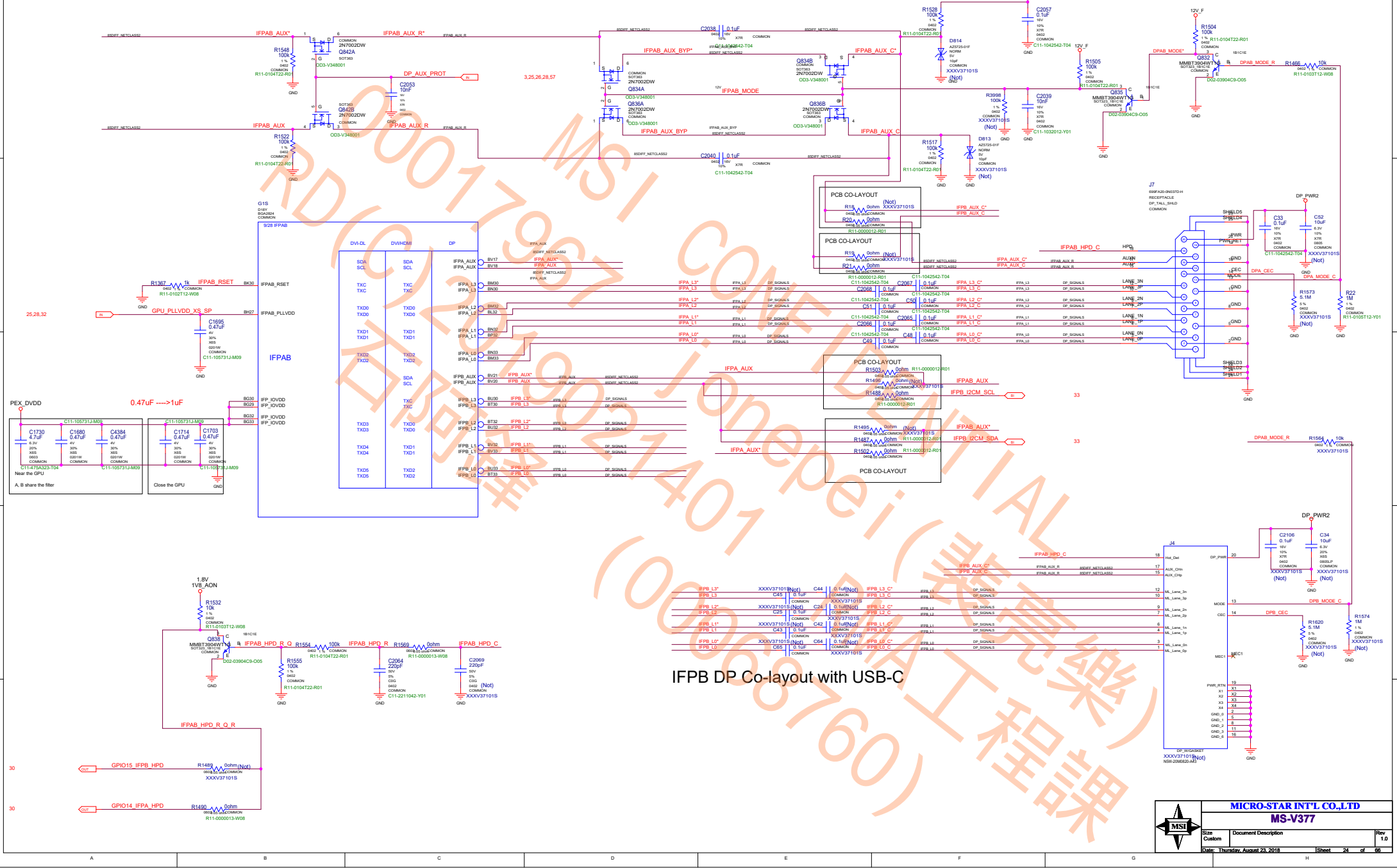


GPU Decoupling

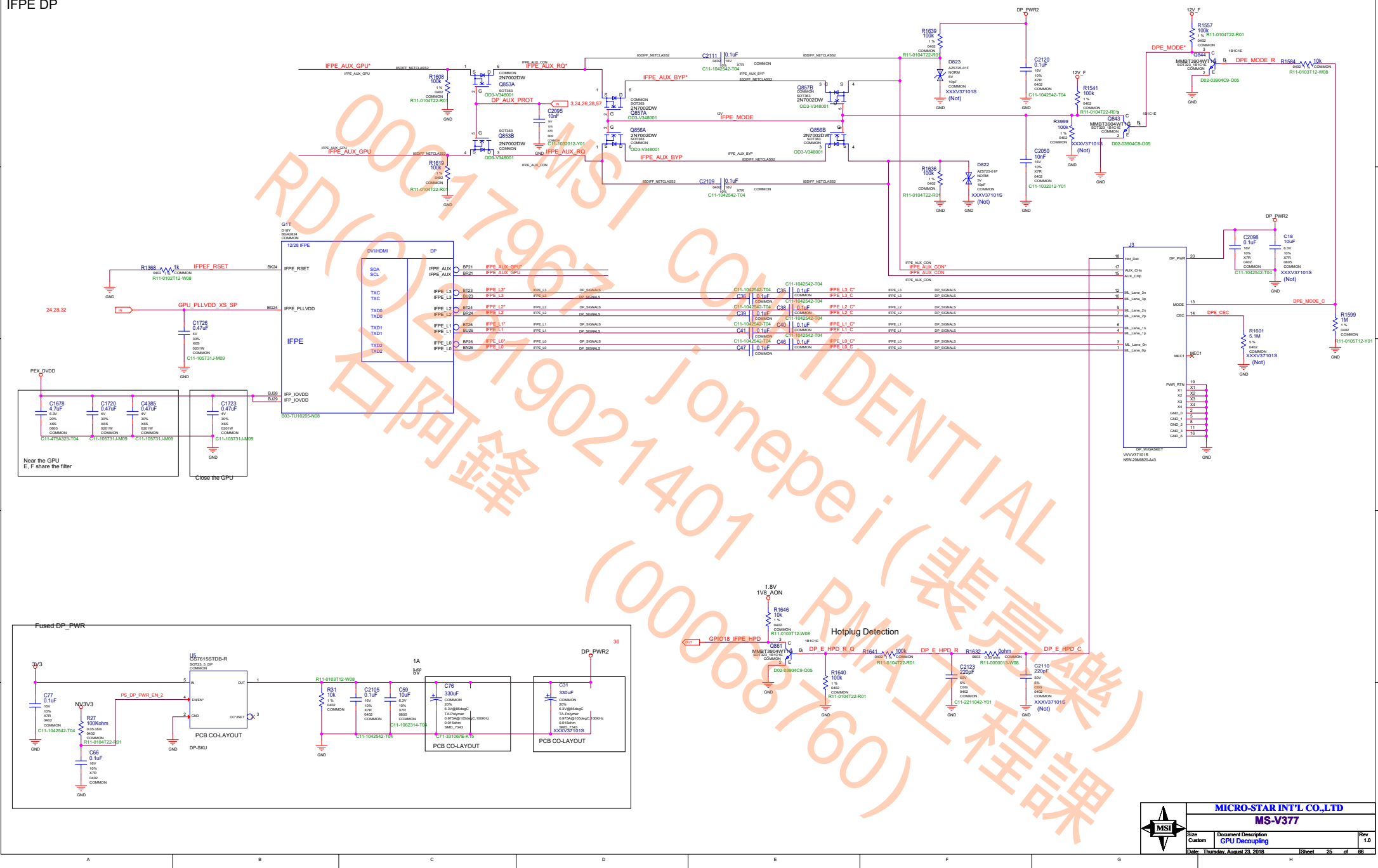




## IFPAB TALL-DP

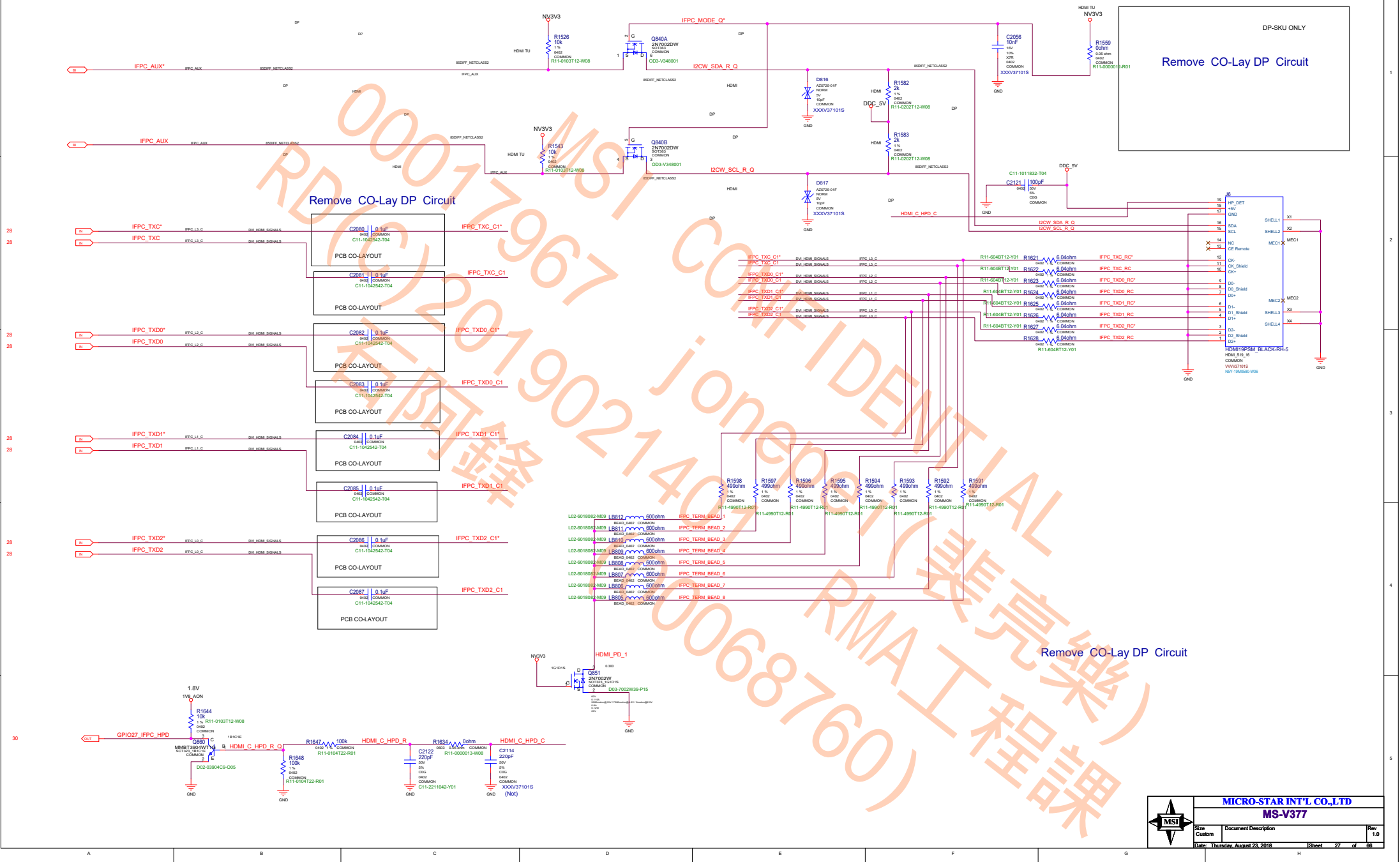








IFPC HDMI 2.0/DP





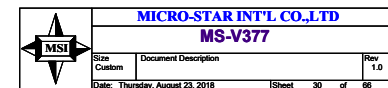
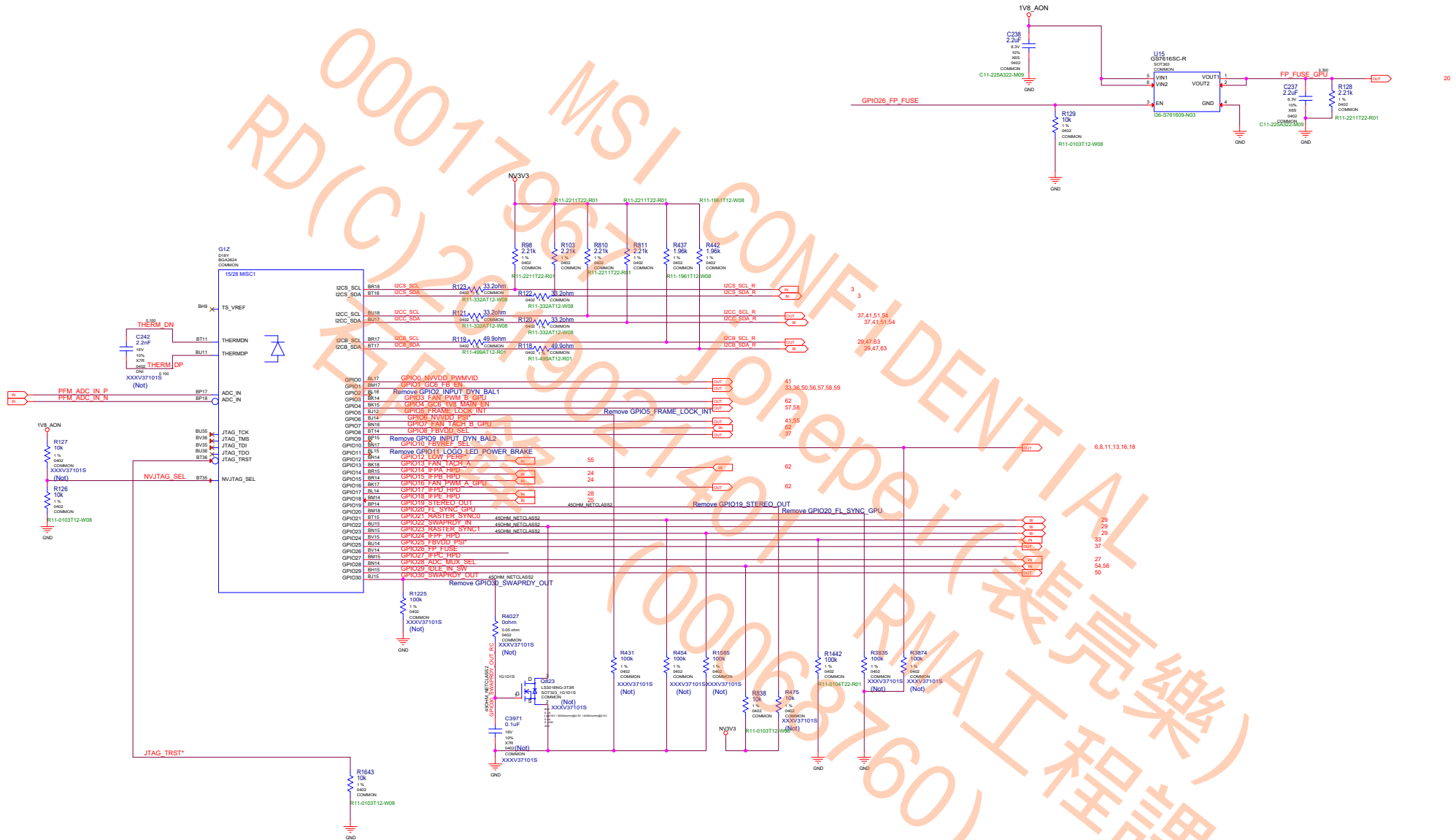
## NVHS Interface and FRAME LOCK



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## MISC1: Fan, Thermal, JTAG, GPIO, STEREO



MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
H	L	H	00101
H	H	L	00110
H	H	H	00111
L	L	M	01000
L	M	L	01001

DEFAULT

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	H	XXX0	FS_OVERT DISABLE

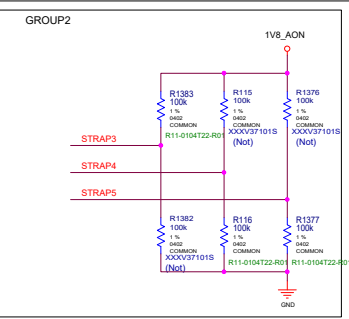
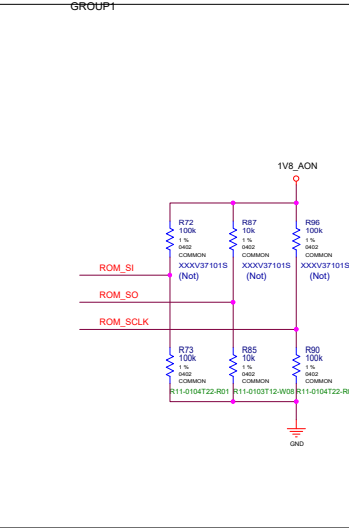
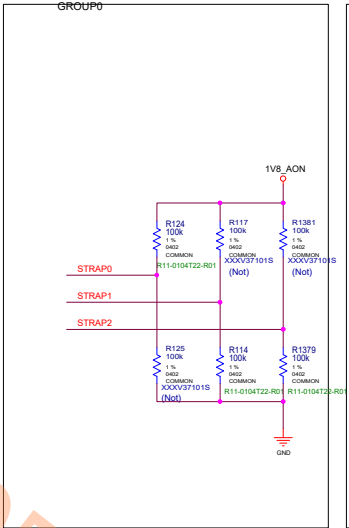
DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

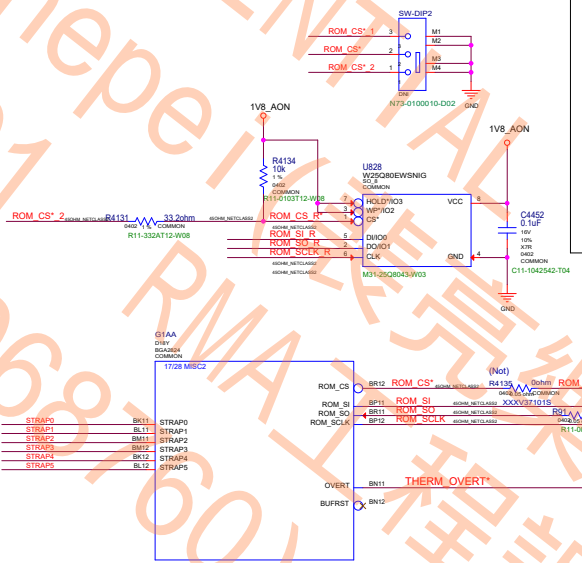
Default

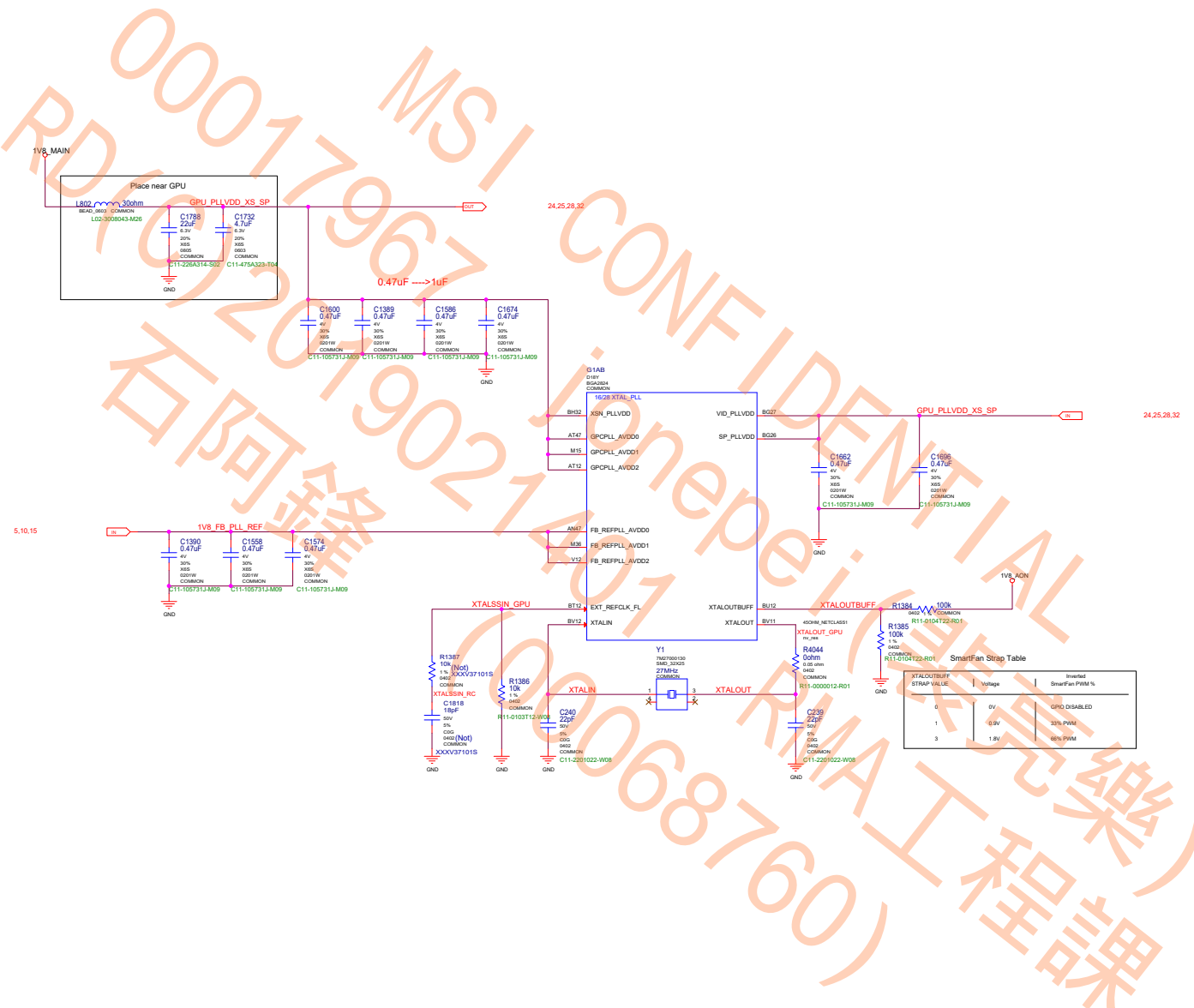
SKU 200

- 1:SMB\_ALT\_ADDR ENABLE
- 0:SMB\_ALT\_ADDR DISABLE
- 1:DEVID\_SEL REBRAND
- 0:DEVID\_SEL ORIGINAL
- 1:PCIE\_CFG LOW POWER
- 0:PCIE\_CFG HIGH POWER
- 1:VGA\_DEVICE ENABLE
- 0:VGA\_DEVICE DISABLE



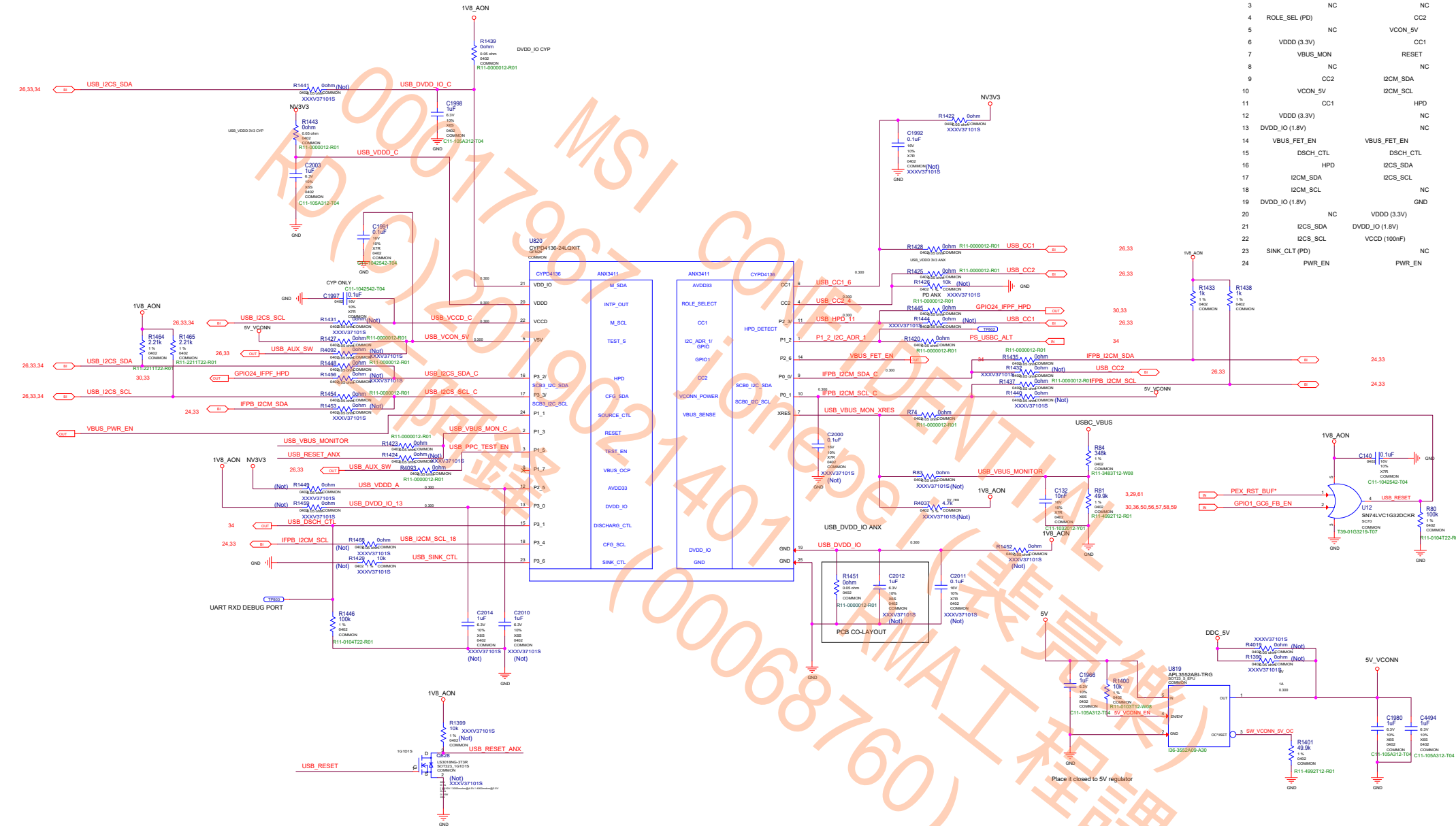
Add Dual BIOS







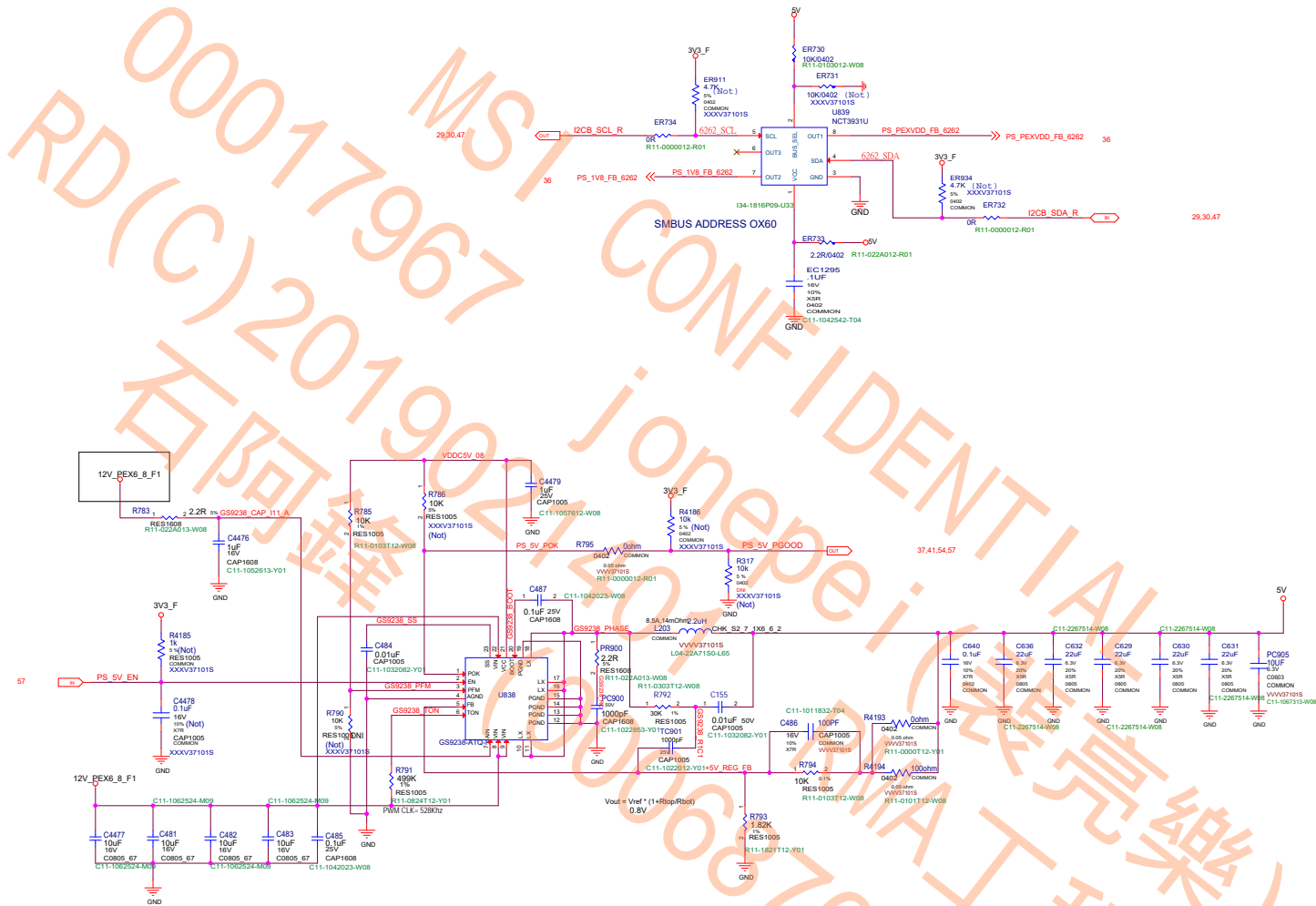
MISC: USB PPC



PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_SV
6	VDDO (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_SV	I2CM_SCL
11	CC1	HPD
12	VDDO (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDO (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCO (100F)
23	SINK_CTL (PD)	NC
24	PWR_EN	PWR_EN



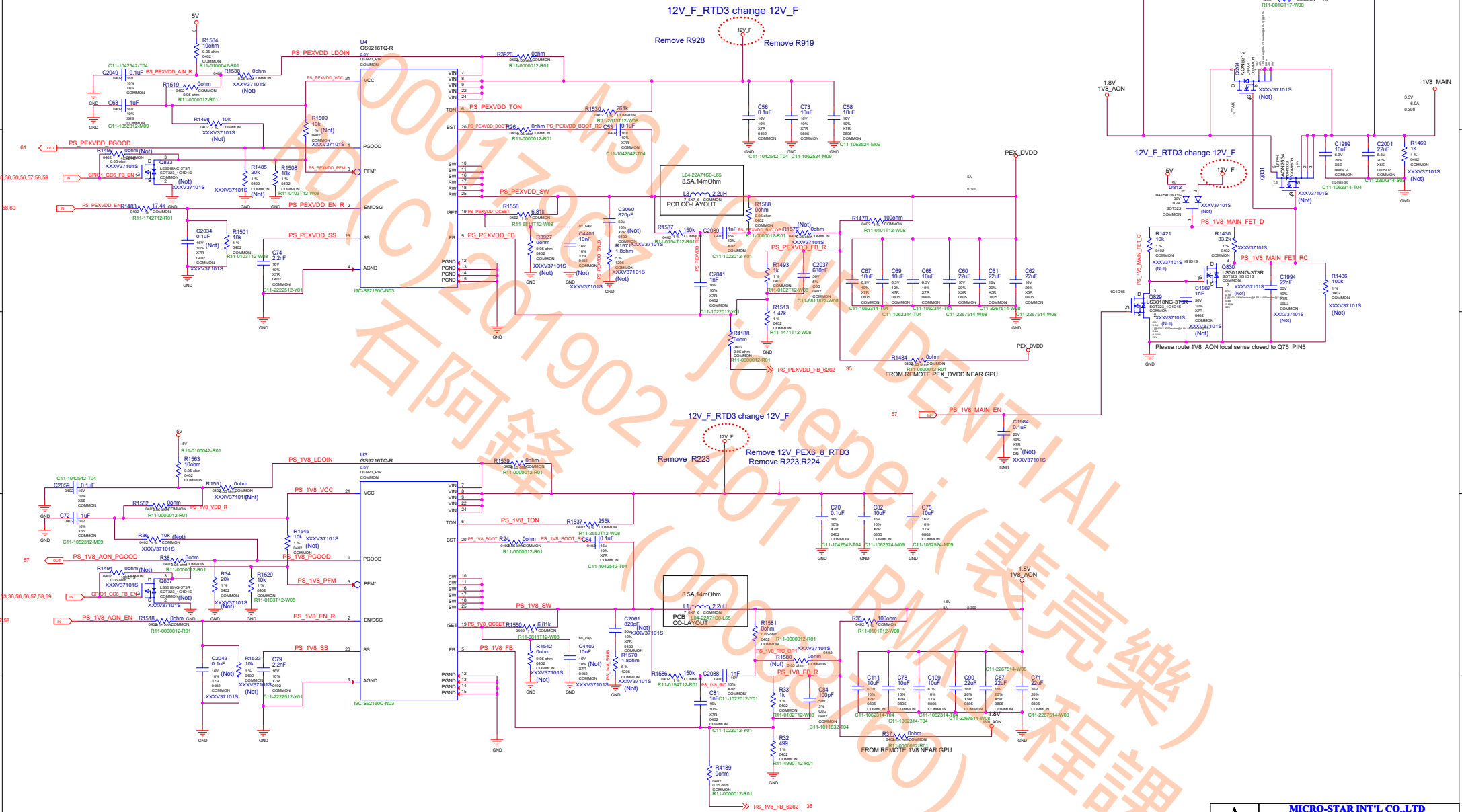
PS: 5V, 5V\_BACKUP



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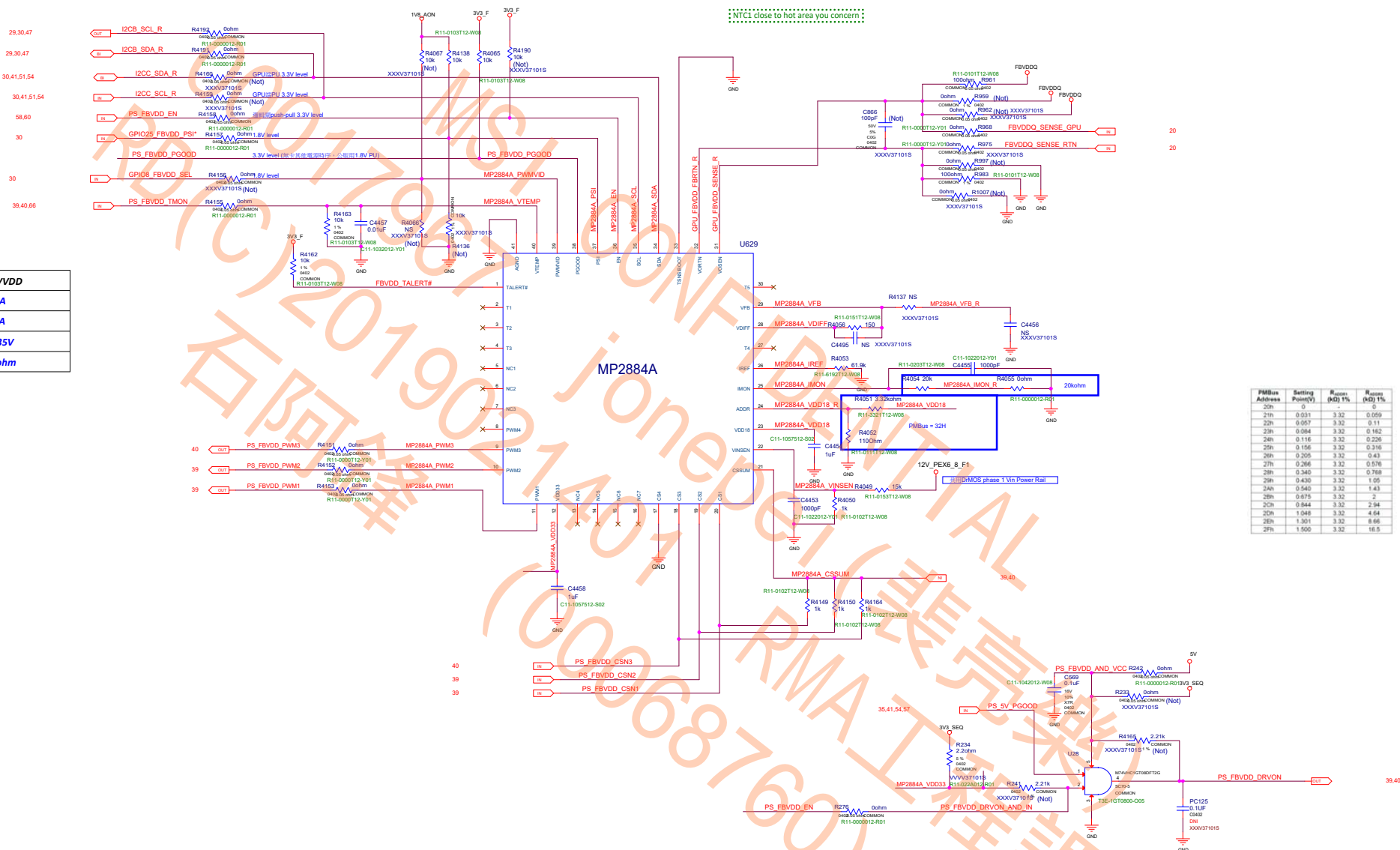
## PS: FBVDD Controller

EN Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

<i>PWMVID</i>	<i>V<sub>out</sub></i>
<i>High</i>	<i>VID in 24h</i>
<i>Hi-Z</i>	<i>VID in 21h</i>
<i>Low</i>	<i>VID in 1Fh</i>

	+NVVDD
TDC	??A
IccMax	??A
Vboot	1.35V
Load Line	0mohm



PMI#s Address	Setting Priority	Reason (pQI %)	Reason (pQI %)
20n	0	-	0
22n	0.031	3.2	0.059
22n	0.057	3.32	0.11
23n	0.084	3.32	0.162
24n	0.116	3.32	0.226
25n	0.156	3.32	0.316
26n	0.205	3.32	0.43
27n	0.266	3.32	0.576
28n	0.342	3.32	0.768
29n	0.430	3.32	1.05
2An	0.540	3.32	1.43
2Bn	0.675	3.32	2
2Cn	0.844	3.32	2.94
2Dn	1.048	3.32	4.4
2En	1.301	3.32	6.66
2Fn	1.605	3.32	8.64



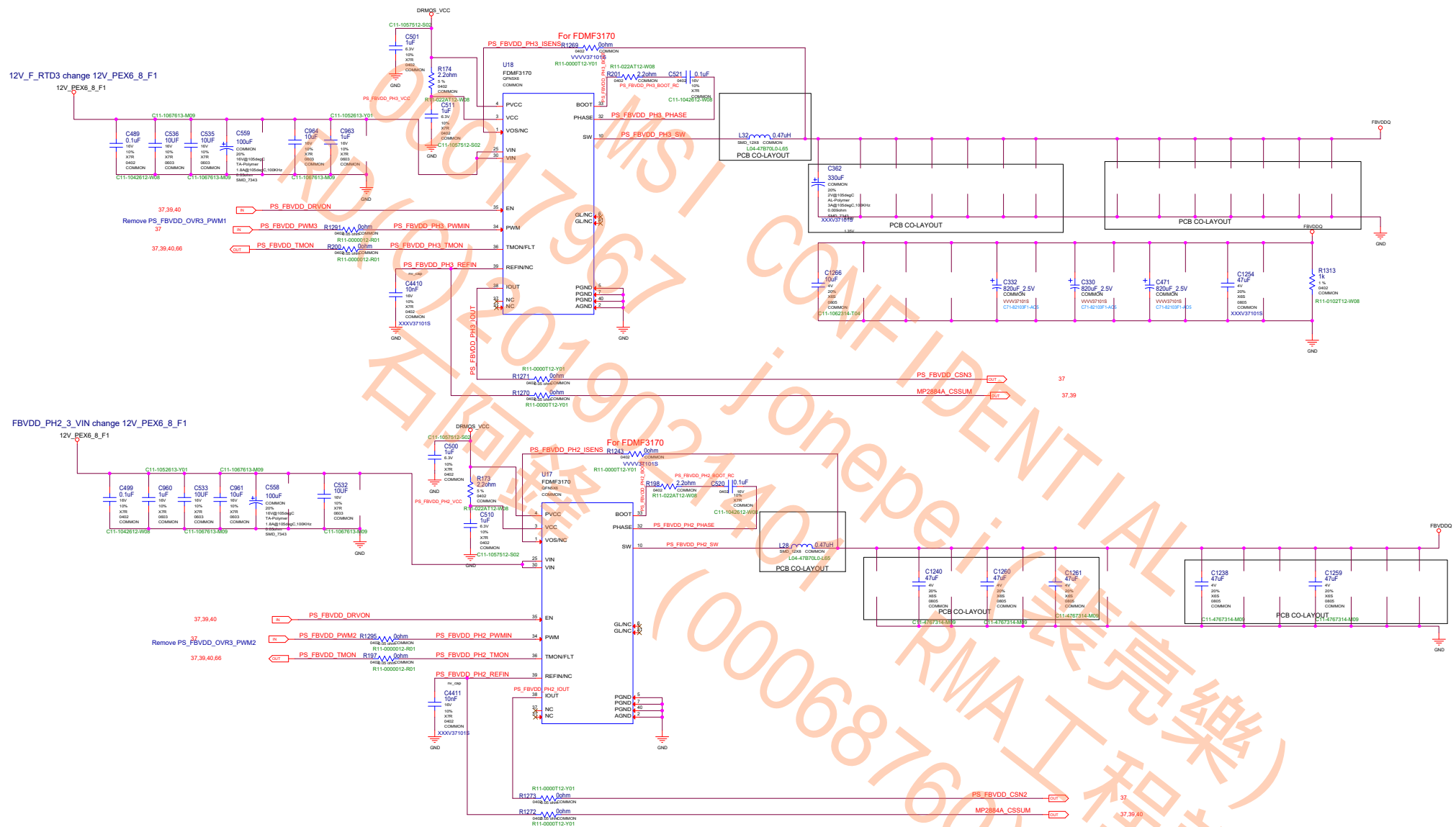
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MSI CONFIDENTIAL  
00017967 jonepei (裴亮樂)  
RD(C)2019021401 RMA工程課  
石阿鋒 (00068760)

PS: FBVDD PH2,3

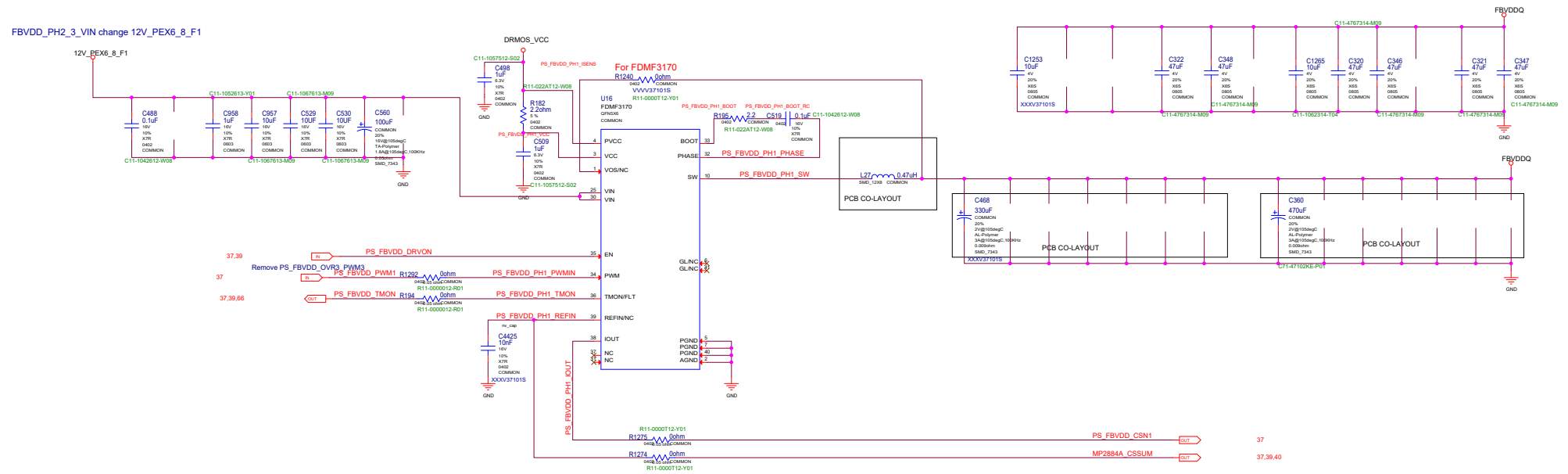


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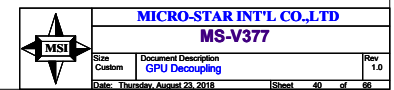
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PS: FBVDD PH1



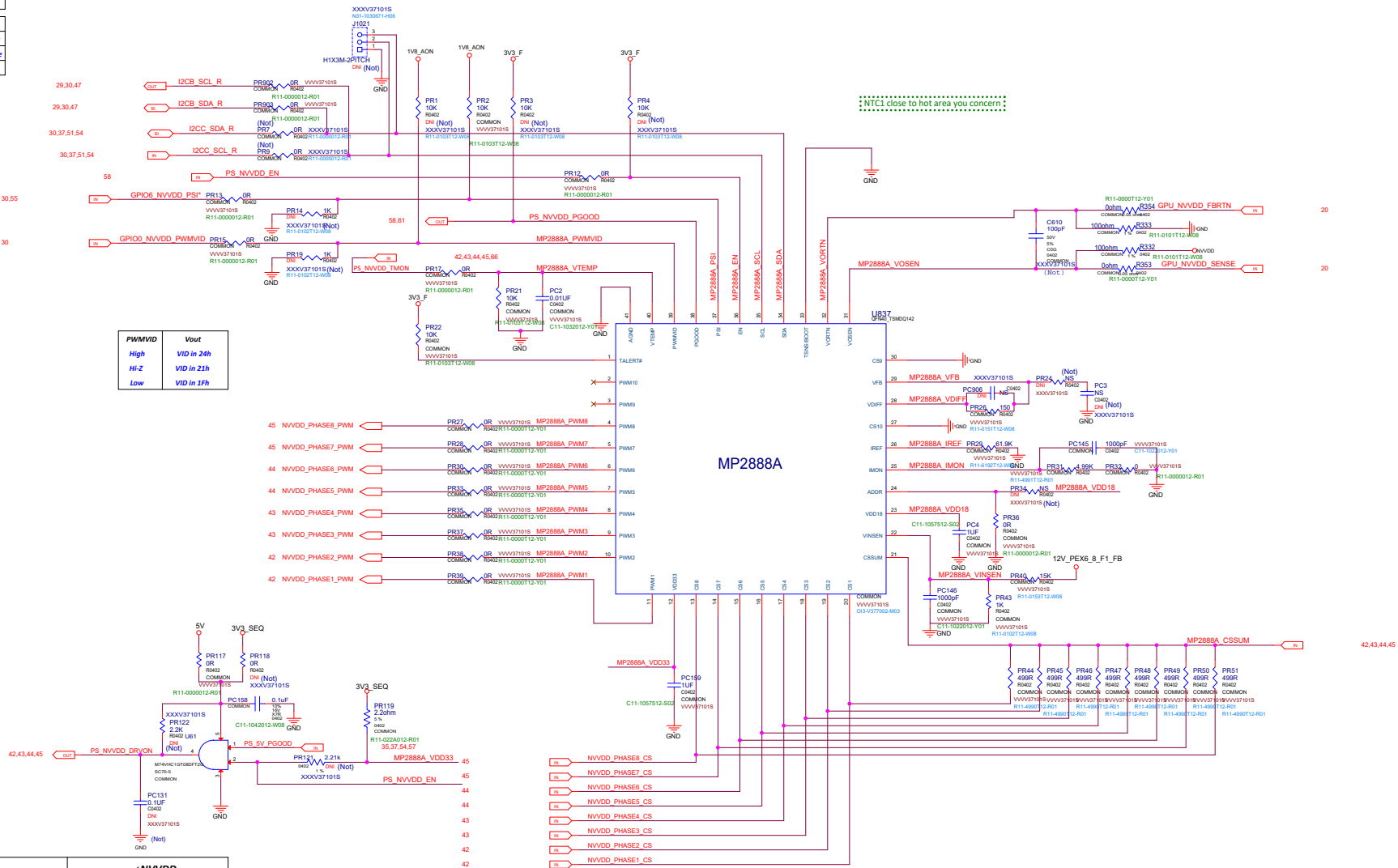
Remove 12V\_PEX\_FB ---->FBVDD\_PH2\_3\_VIN circuit





<i>EN Type</i>	<i>R3</i>
<i>Open Drain</i>	<i>10k</i>
<i>Push Pull</i>	<i>NS</i>

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count



	<b>+NVVDD</b>
<b>TDC</b>	<b>200A</b>
<b>IccMax</b>	<b>330A</b>
<b>Vboot</b>	<b>0.8V</b>
<b>Load Line</b>	<b>0mohm</b>

PMU Address	Setting Point(V)	R <sub>max</sub> (%)	R <sub>min</sub> (%)
20n	0	-	0.059
21n	0.031	3.32	0.11
22n	0.057	3.32	0.11
23n	0.084	3.32	0.163
24n	0.116	3.32	0.226
25n	0.156	3.32	0.316
26n	0.205	3.32	0.43
27n	0.266	3.32	0.576
28n	0.340	3.32	0.768
29n	0.430	3.32	1.05
2Aa	0.540	3.32	1.43
2Bn	0.675	3.32	2
2Cn	0.844	3.32	2.94
2Dn	1.048	3.32	4.64
2En	1.301	3.32	8.66
2Fn	1.500	3.32	16.8

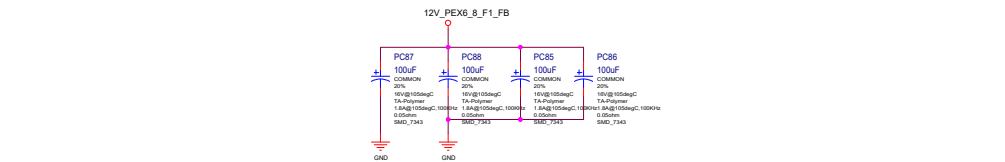
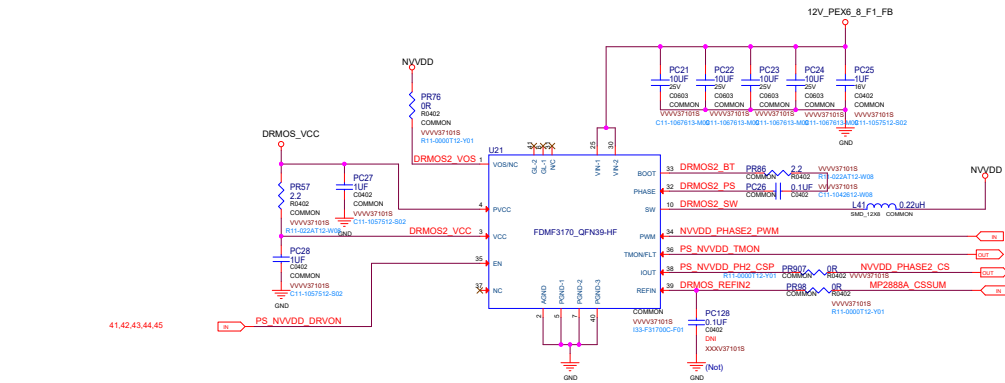
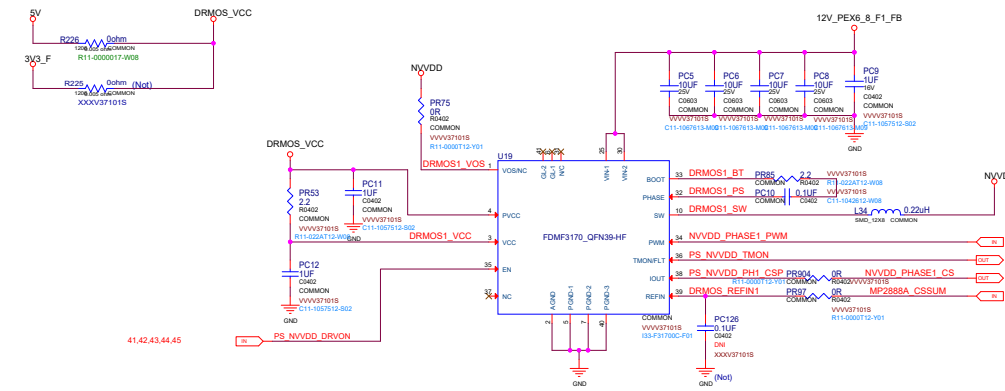


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# PS: NVVDD Phase 1~4



41,42

41,42,43,44,45,46

41,42

41,42,43,44,45

41,42,43,44,45

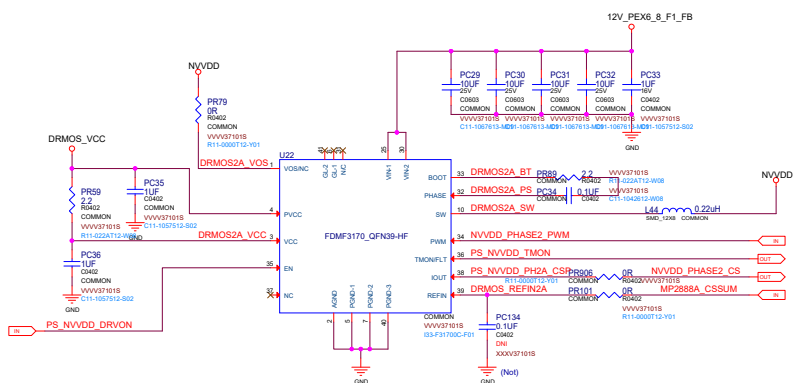
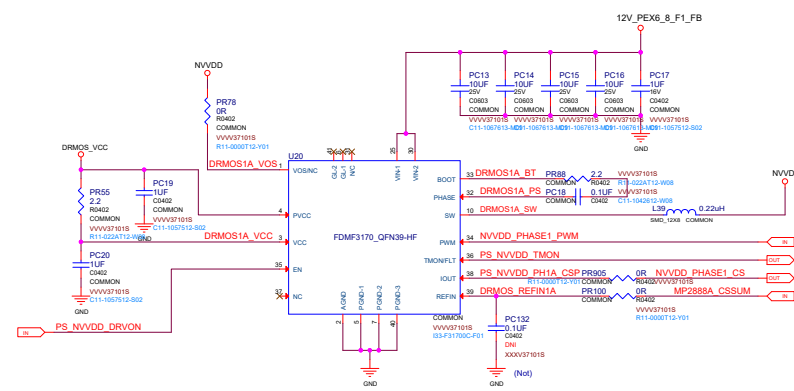
41,42

41,42,43,44,45,46

41,42

41,42,43,44,45

41,42,43,44,45



41,42,43,44,45

41,42

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41,42

41,42,43,44,45

41,42,43,44,45



41,42,43,44,45

41,42

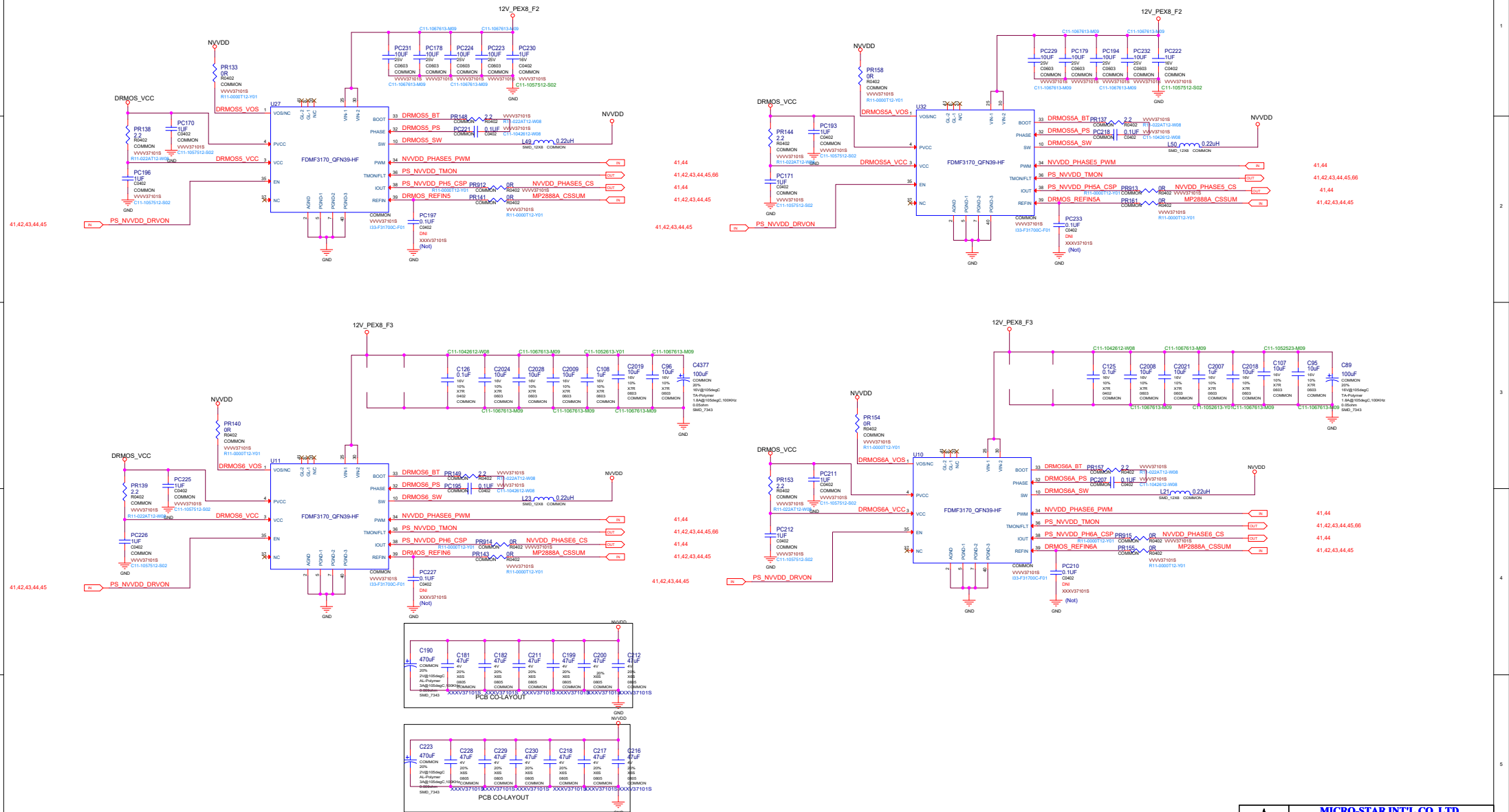
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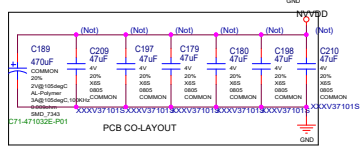
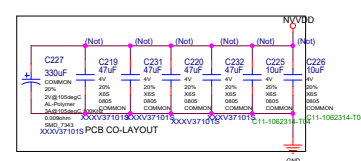
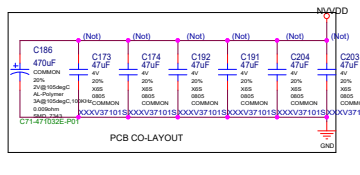
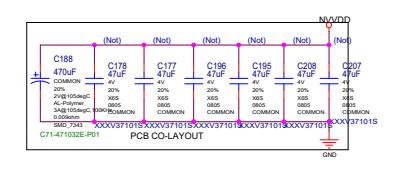
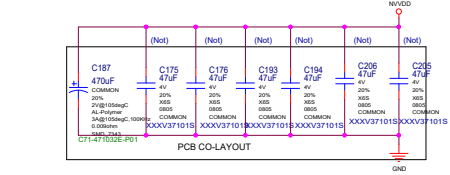
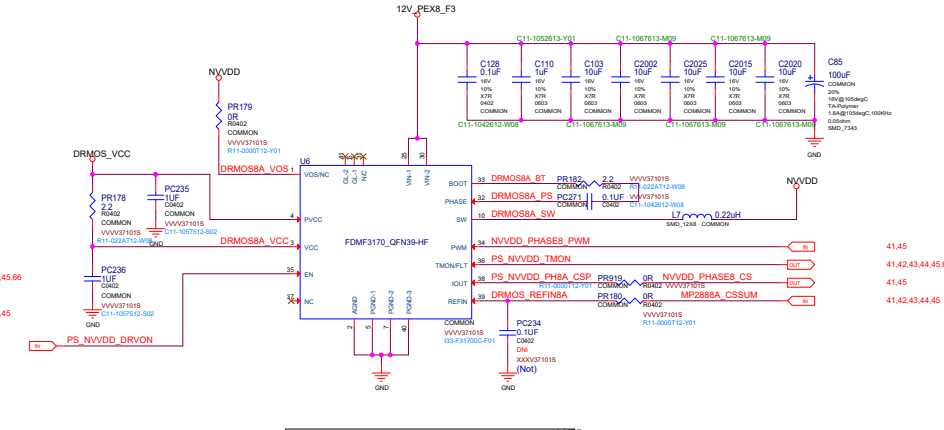
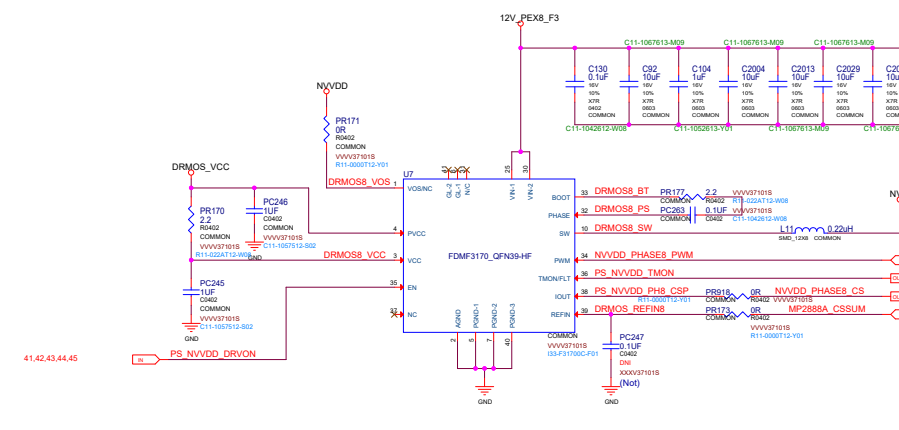
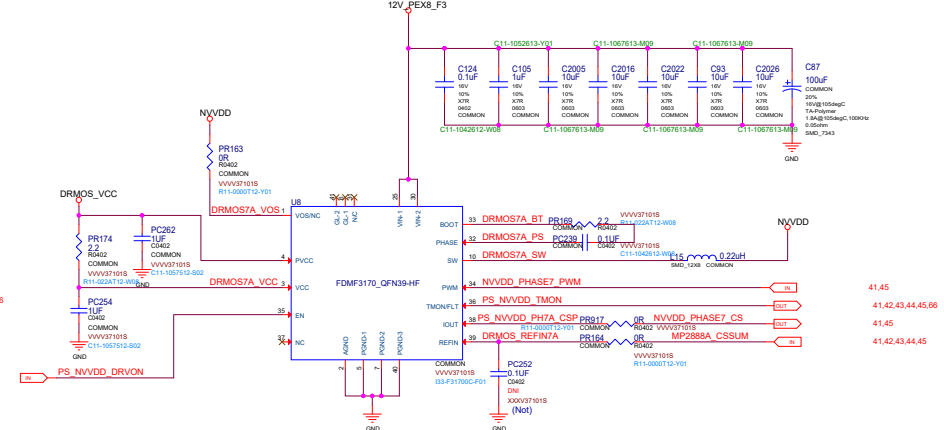
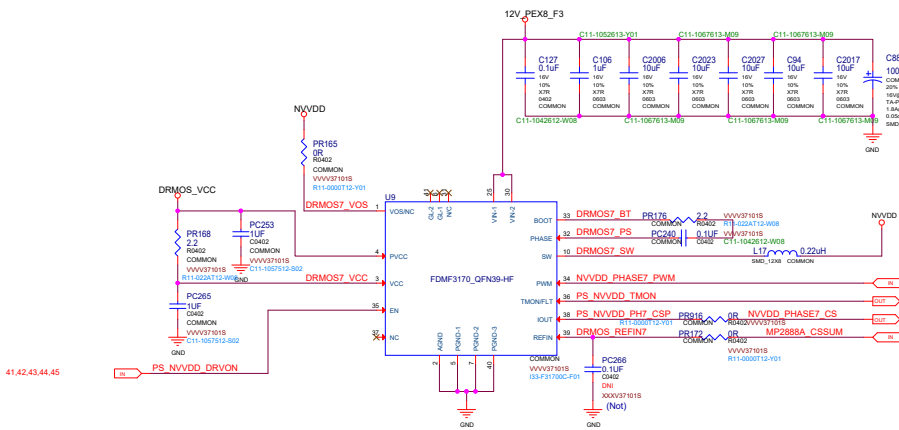
41,42,43,44,45

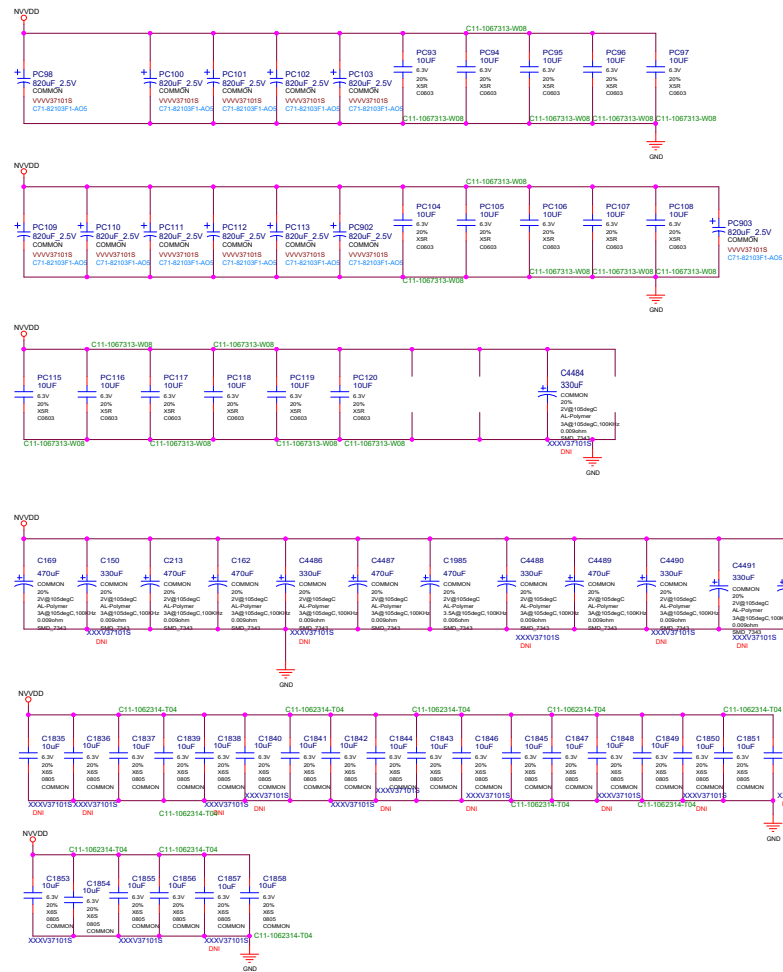
41,42,43,44,45



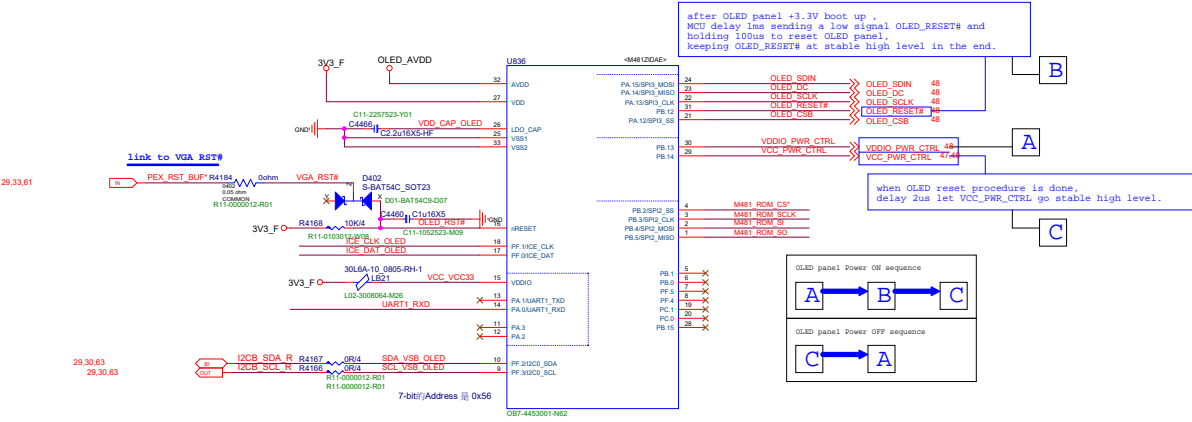


PS: NVDD Phase 13~16



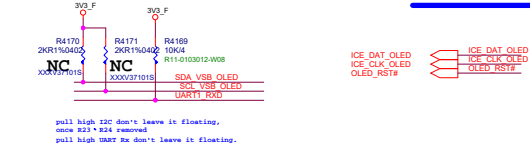


PS: NVDD PH 9,10  
32 PIN OLED MCU

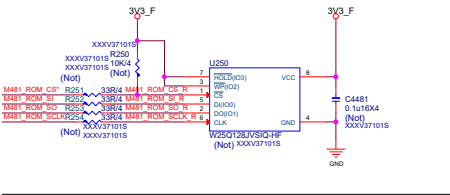


I2C and UART Reserve

FW update

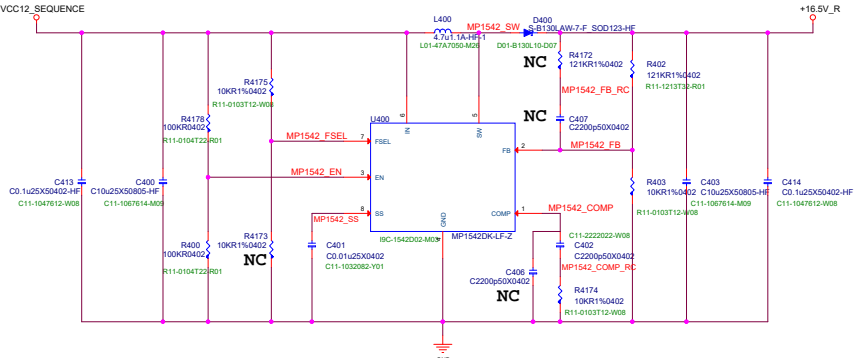
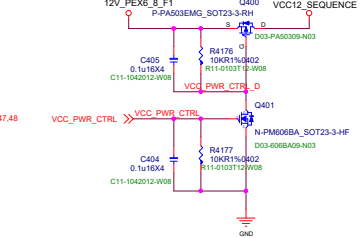


External 3.3V SPI ROM,128M(16Mx8bit)



MPS1542 BUCK BOOST FOR OLED POWER 12Vin 16.5Vout

+16.5V power up sequence

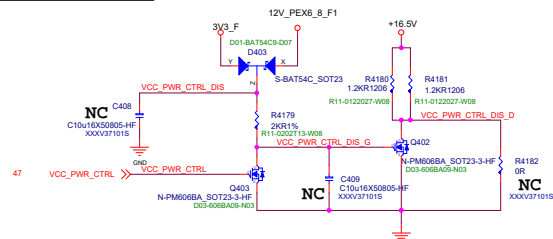


PIN FUNCTIONS

Pin #	Name	Description
1	COMP	Compensation Pin. Connect a capacitor and resistor in series to ground for loop stability.
2	FB	Feedback Input. Reference voltage is 1.25V. Connect a resistor divider to this pin.
3	EN	Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input source (through a 100kΩ pull-up resistor if $V_{IN} > 6V$ ) for automatic startup. EN cannot be left floating.



## +16.5V Discharge



100ms time interval is counting from 2 voltages rating 10% to 0% or lower level.

### Power OFF / Display OFF Sequence

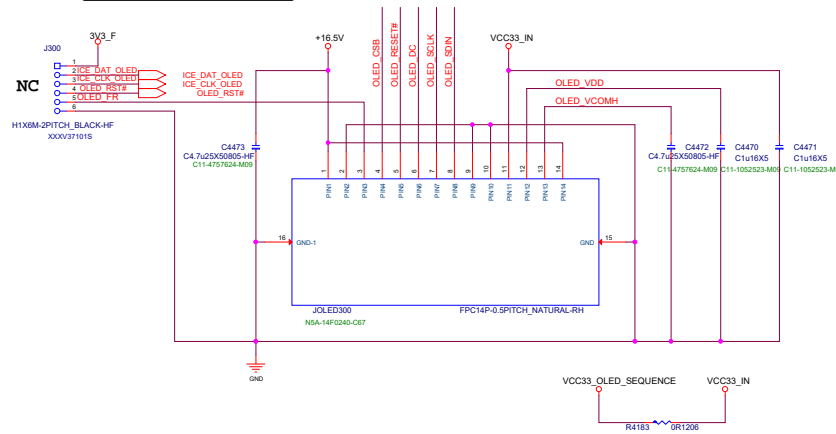


### 12-2) 入力端子名称 Pin Assignment

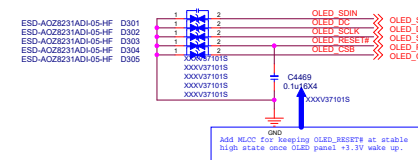
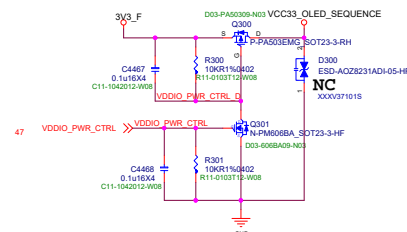
I: Input, O: Output, P: Power

PIN No.	名称 Pin Name	機能 Function Description	I/O
1	VCC	OLED駆動電源 OLED Driving Voltage	P
2	AGND	グラウンド Analog Ground	P
3	FR	同期信号 Synchronization Signal	O
4	CSB	チップセレクト Chip Select	I
5	RSTB	リセット Reset	I
6	DC	データ/コマンド選択 Data/Command Selection	I
7	SCLK	シリアルクロック Serial Clock	I
8	SDIN	データ Data Input	I
9	GND	グラウンド Ground Pin	P
10	AGND	グラウンド Analog Ground	P
11	VCI	ロジック電源 Logic Power Voltage	P
12	VDD	コア電源 Core Voltage	P
13	VCOMH	COMH 電源 COMH Voltage	P
14	VCC	OLED駆動電源 OLED Driving Voltage	P

## OLED housing



### +3.3V power up sequence



### LDO A1117 fixed

+5V to +3.3V

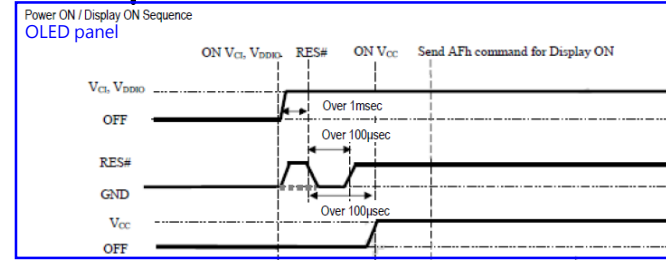
### BOOST Circuit

+12V to +16.5V

MCU NUC481  
OLED controller  
VDDIO for UART

OLED panel  
VCC 52mA (max.)  
VDD/VCI uA

1. after OLED panel +3.3V boot up ,  
delay 1ms sending a low signal OLED\_RESET# and  
holding 100us to reset OLED panel,  
keeping OLED\_RESET# at stable high level in the end.
2. when OLED reset procedure is done,  
delay 2us let VCC\_PWR\_CTRL go stable high level.







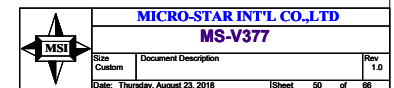
## A

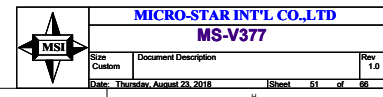
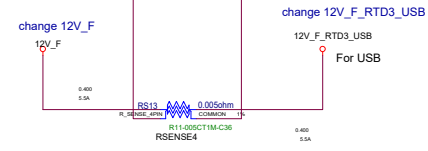
#### AND GATE LOGIC FOR P-BOARD

Remove 12V\_F\_RTD3 circuit

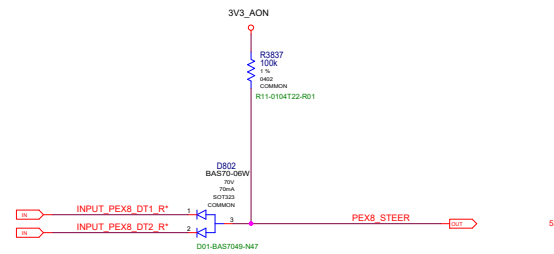
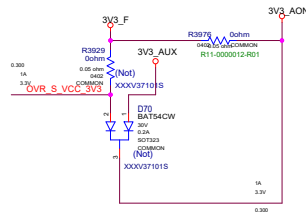
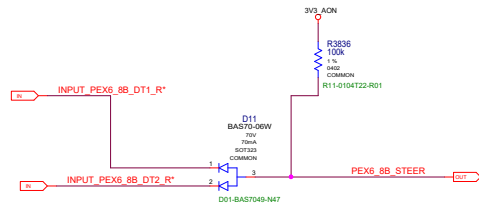
### AND GATE LOGIC FOR P-BOARD

Remove 3V3\_RTD3 circuit

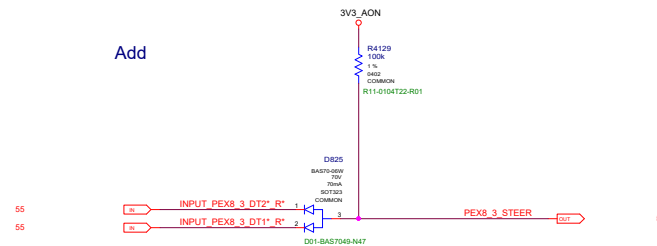




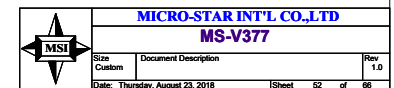
## PS: Input Switch Rail Balance



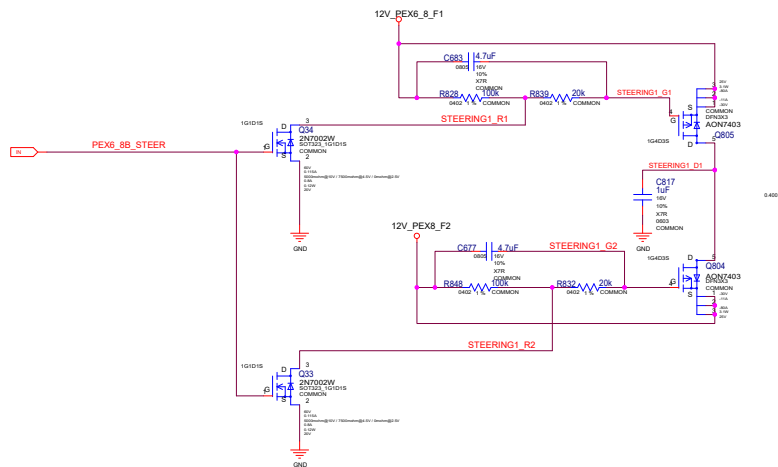
Add



### Remove NVVDD VIN change circuit

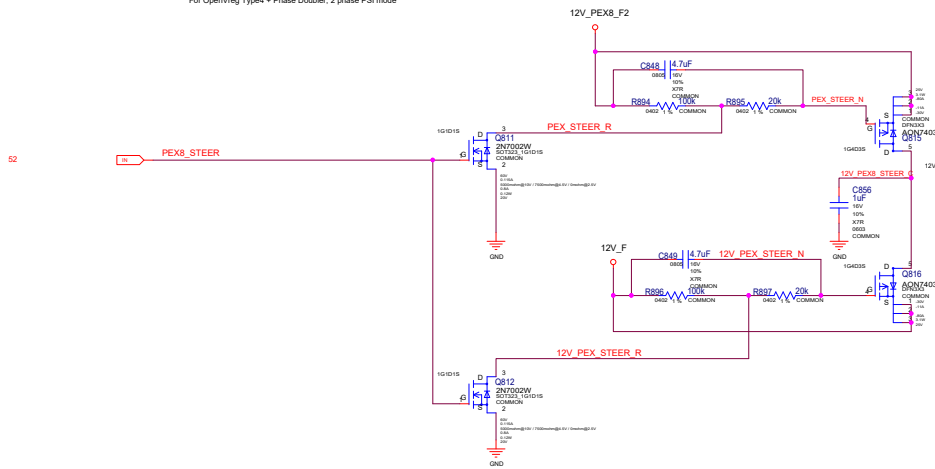


12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

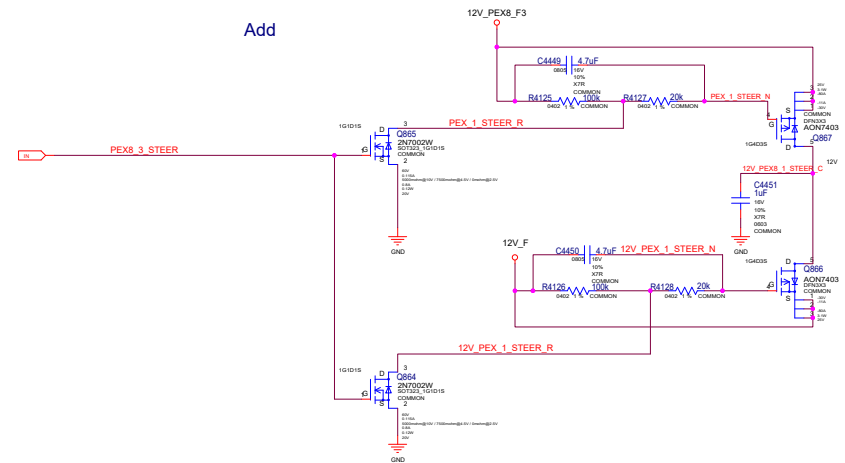


12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

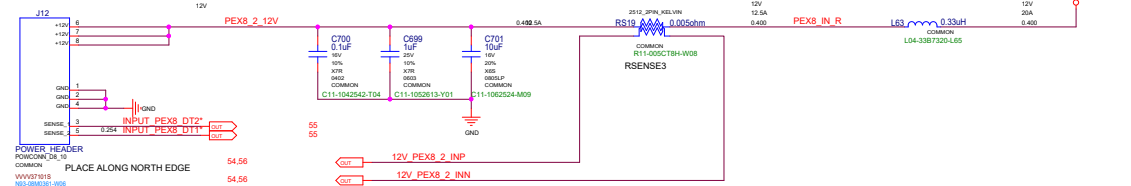
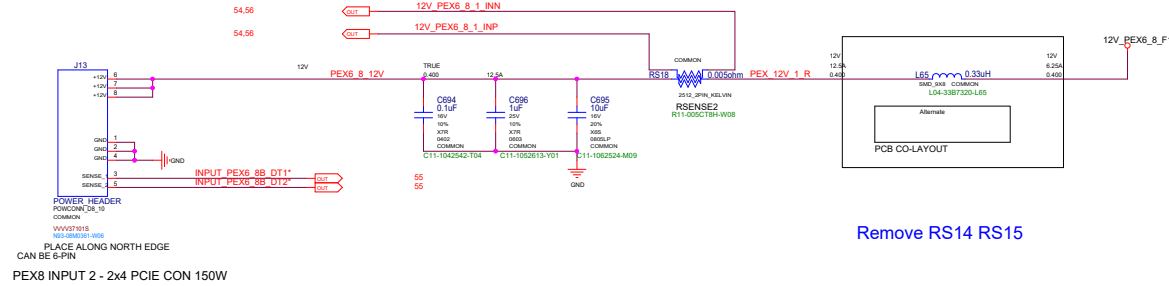
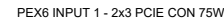
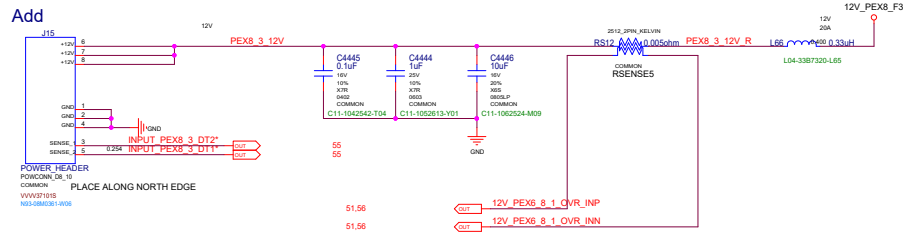
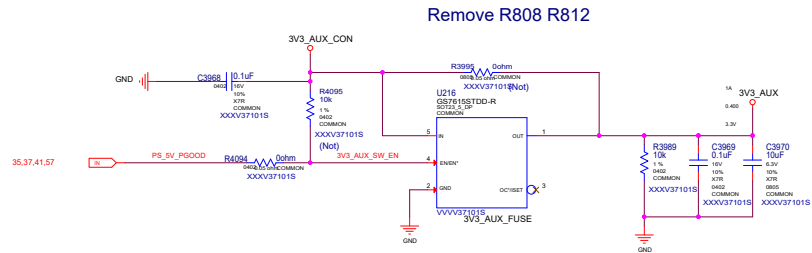
For OpenVing Type4 + Phase Doubler, 2 phase PSI mode



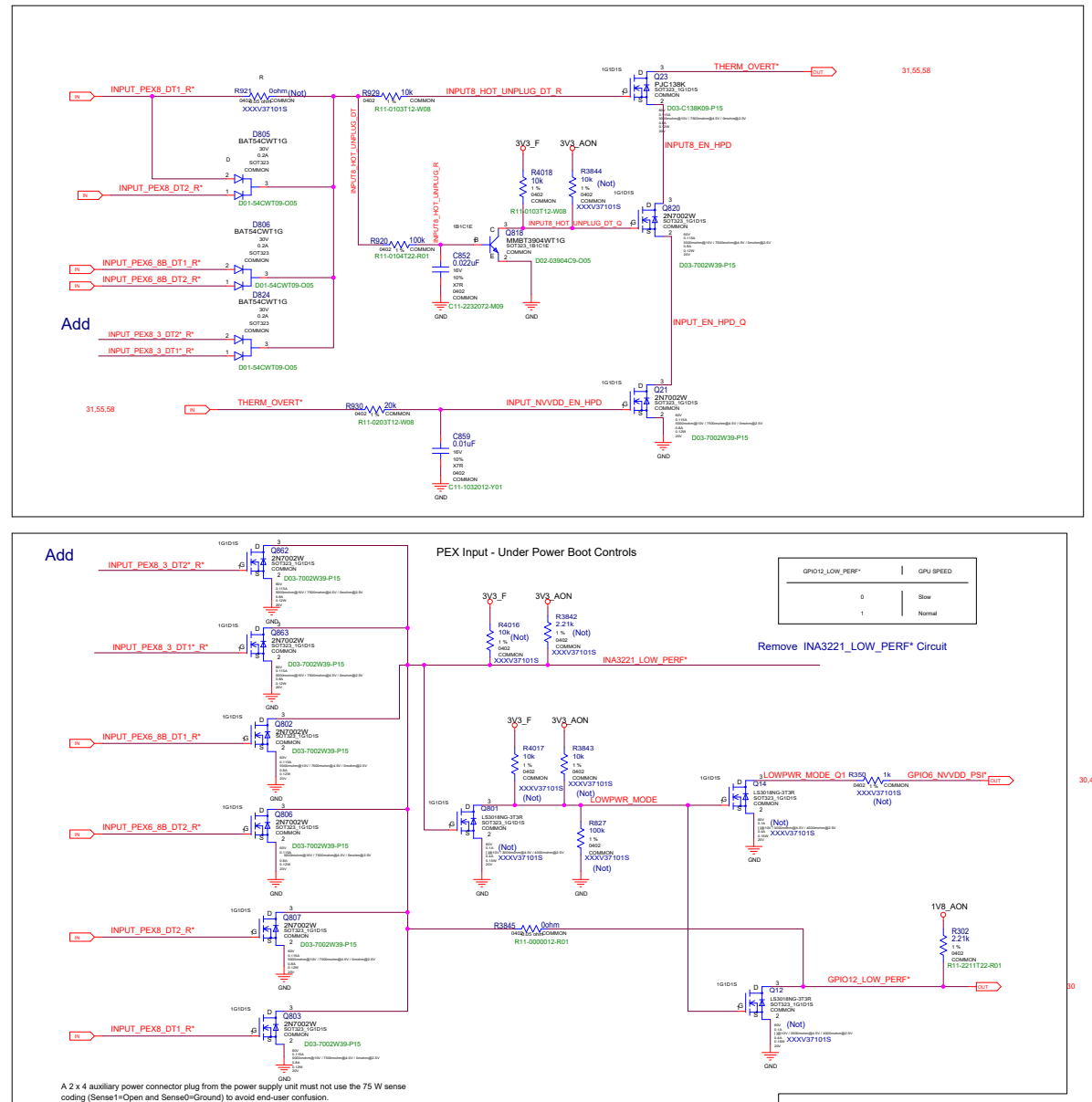
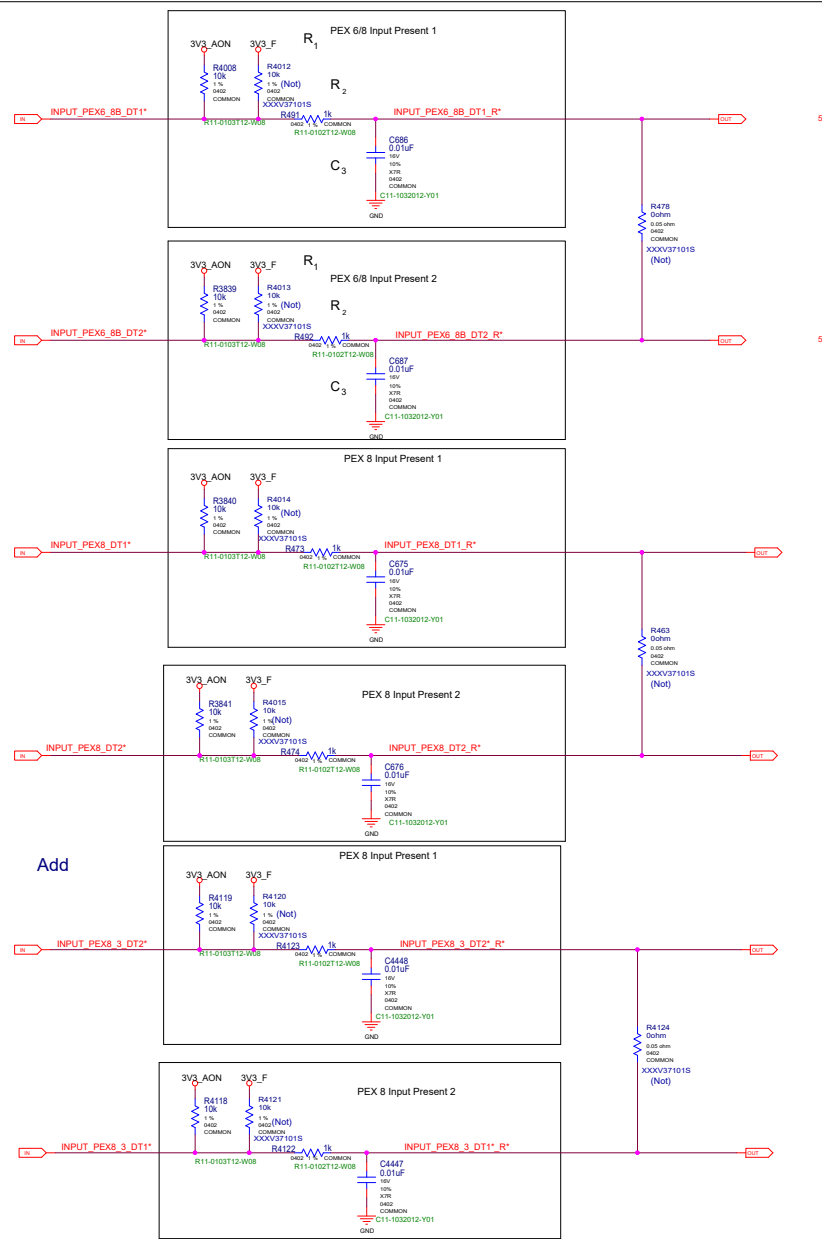
Add



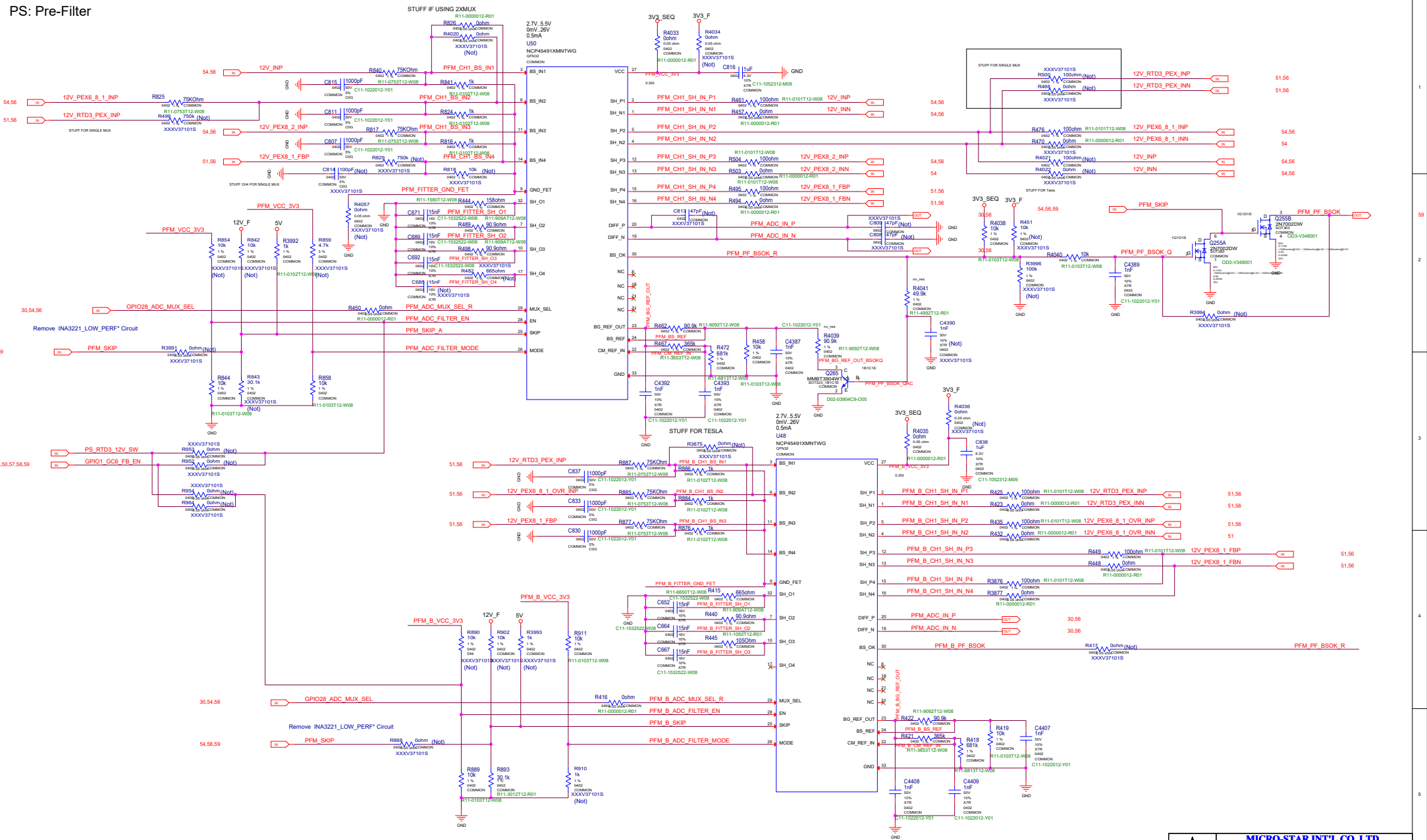
## PS: Inputs, Filtering, and Monitoring



## PS: 12V Current Steering &amp; Hot Unplug Detect



PS: Pre-Filter

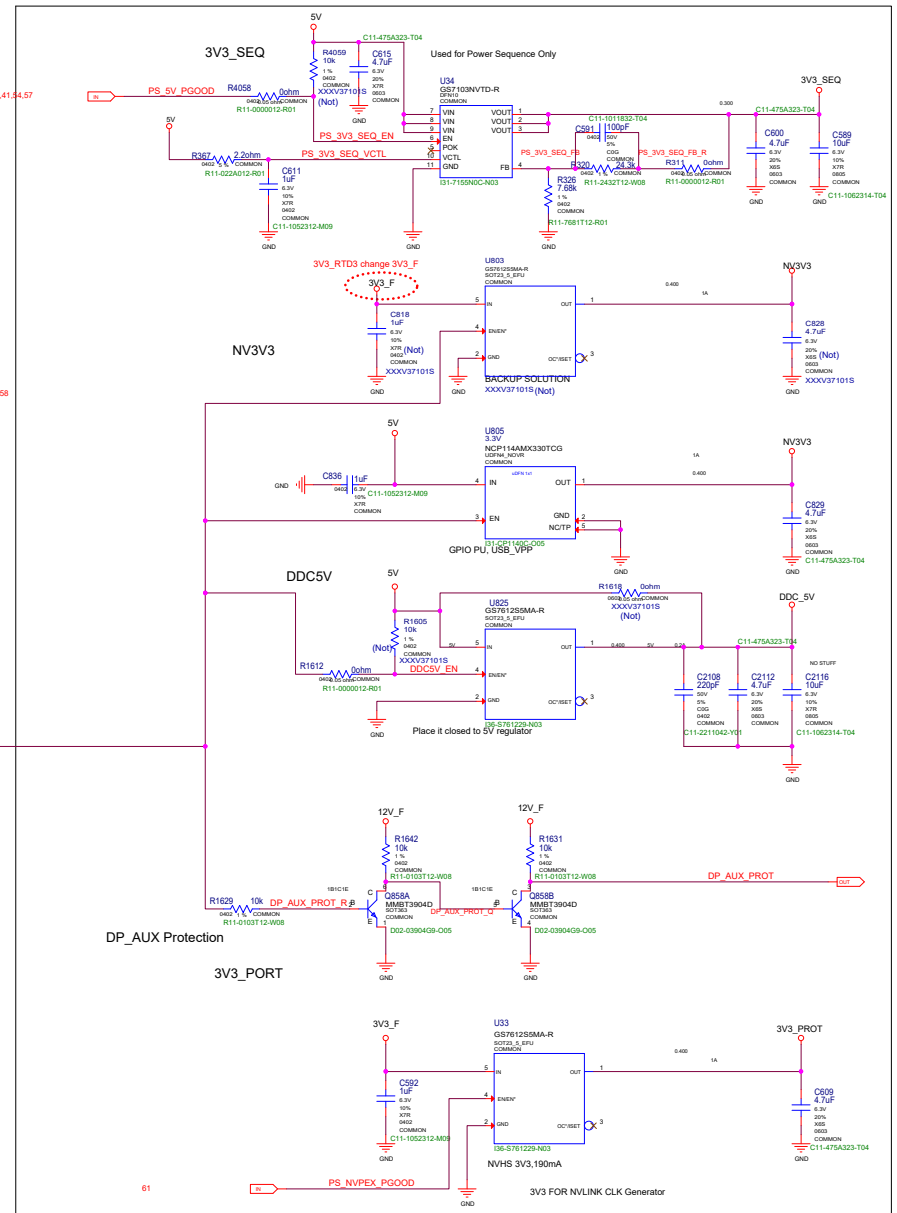
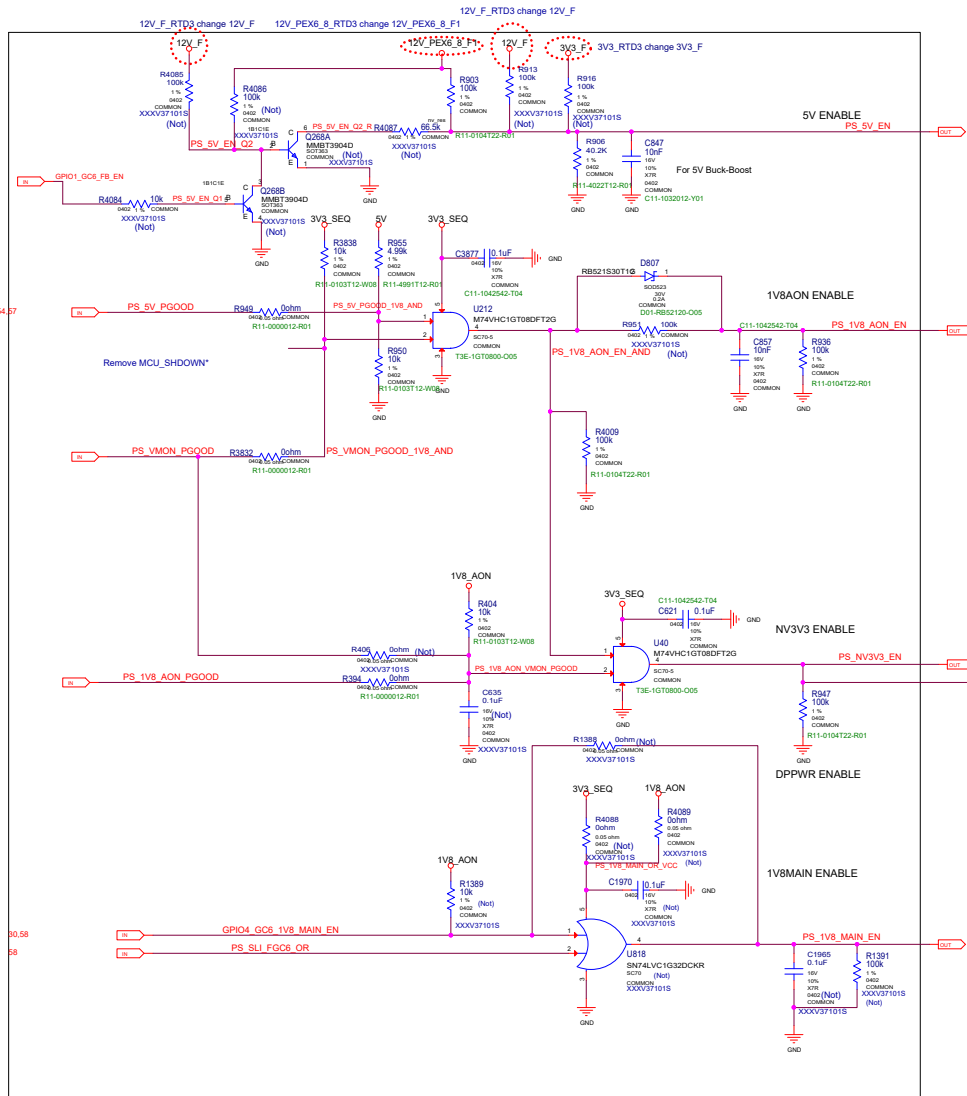


**MICRO-STAR INT'L CO.,LTD**  
**MS-V377**

Size Custom	Document Description	Rev 1.0
Date: Thursday, August 23, 2018		Sheet 56 of 66



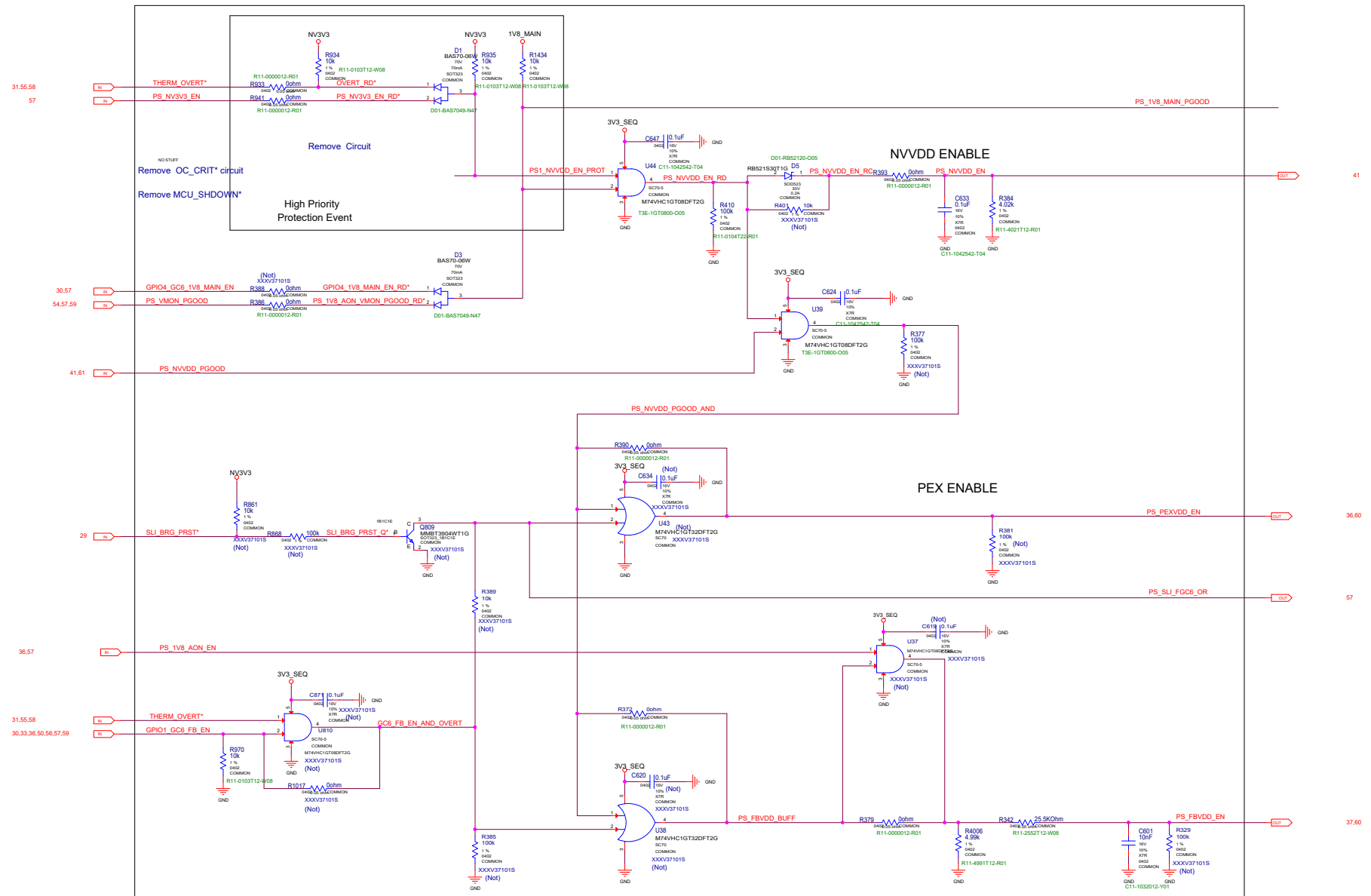
SEQUENCE:5V,1V8,NV3V3 ENABLE



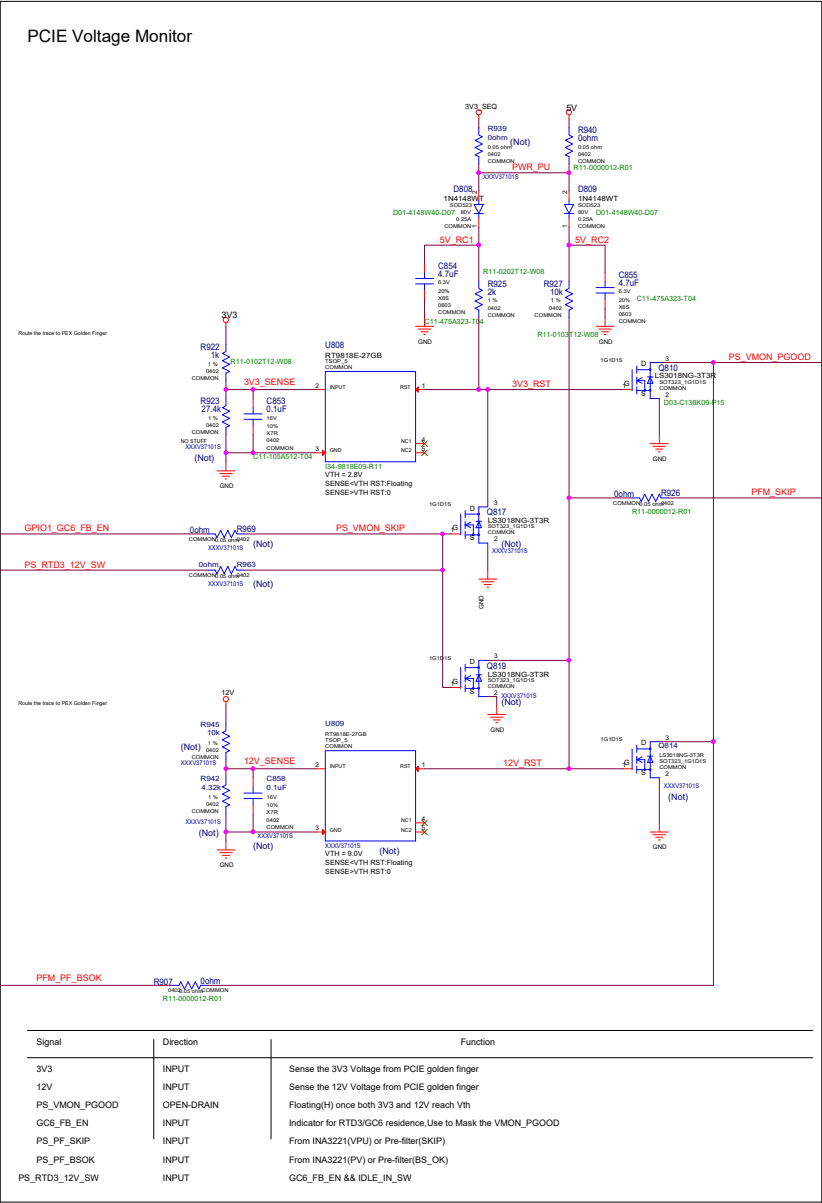
**MICRO-STAR INT'L CO.,LTD**  
**MS-V377**

Size Custom	Document Description <b>5V,1V8,NV3V3 ENABLE</b>	Rev 1.0
Date: Thursday, August 23, 2018		Sheet 57 of 66

SEQUENCE:NV,PEX,FB ENABLE



<p><b>MICRO-STAR INT'L CO.,LTD</b></p> <p><b>MS-V377</b></p>		
m	<p>Document Description</p> <p><b>NV,PEX,FB ENABLE</b></p>	<p>Rev</p> <p><b>1.0</b></p>



BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

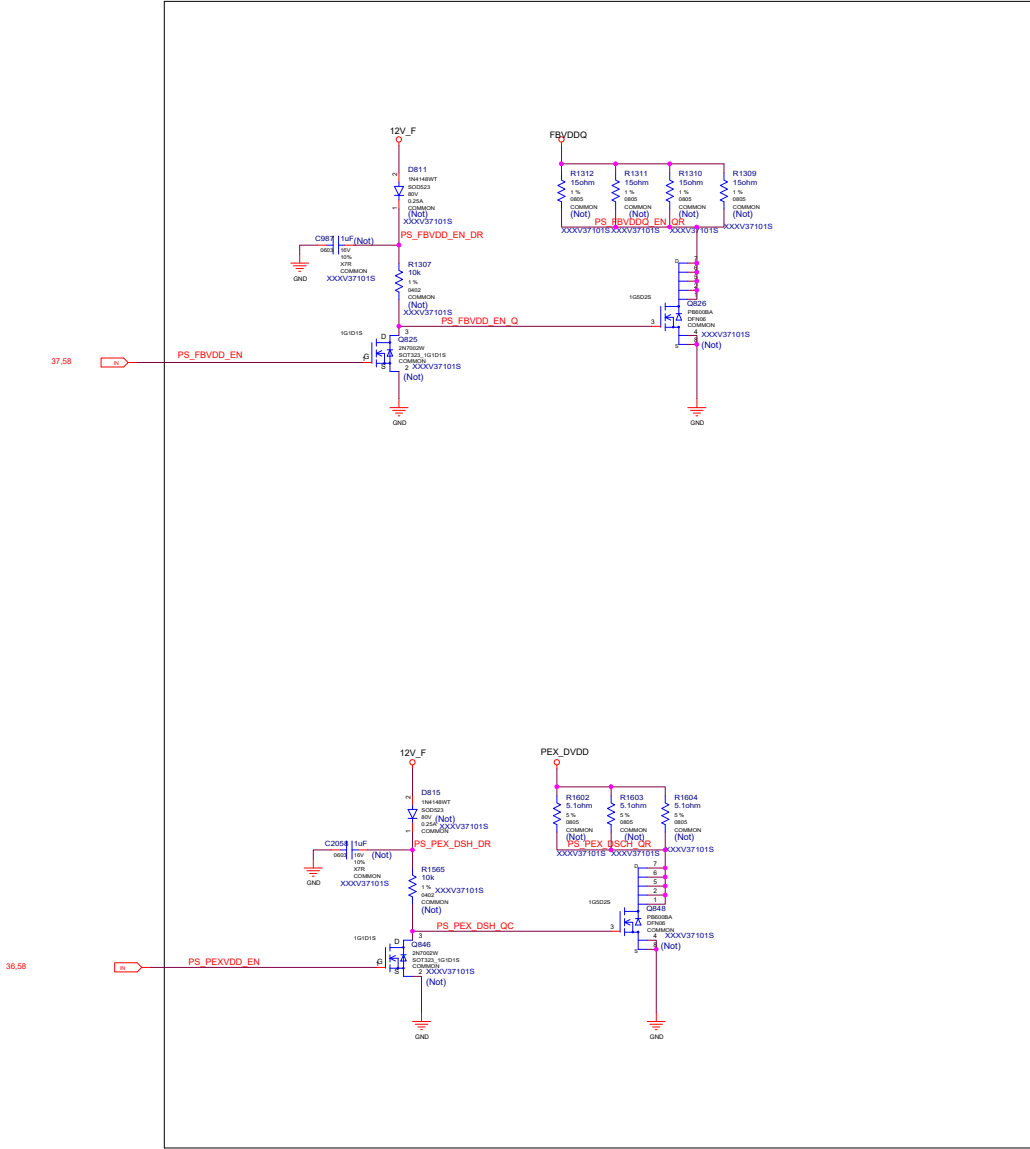
Power Supply

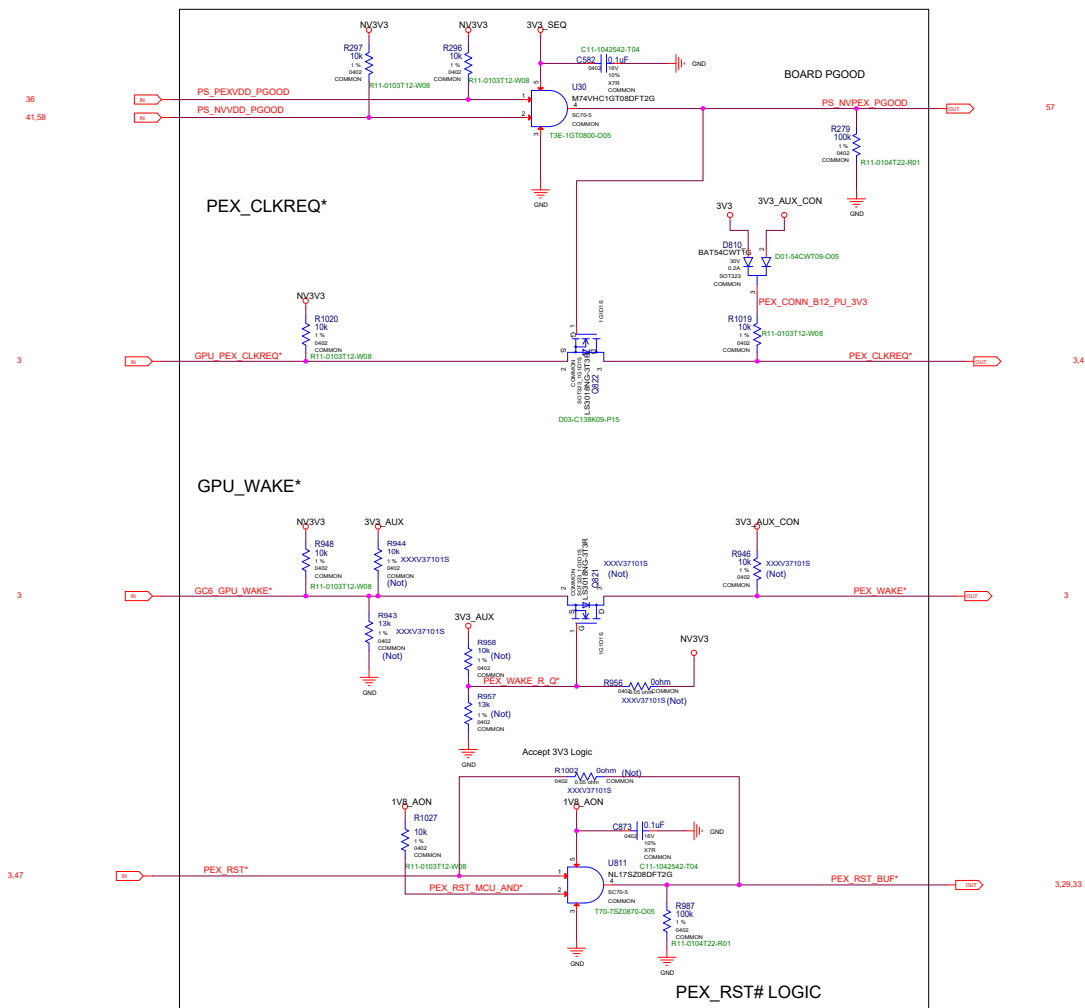
INA3221:3V3\_SEQ

Pre\_Filter(ADC\_MUX):3V3(PEX)

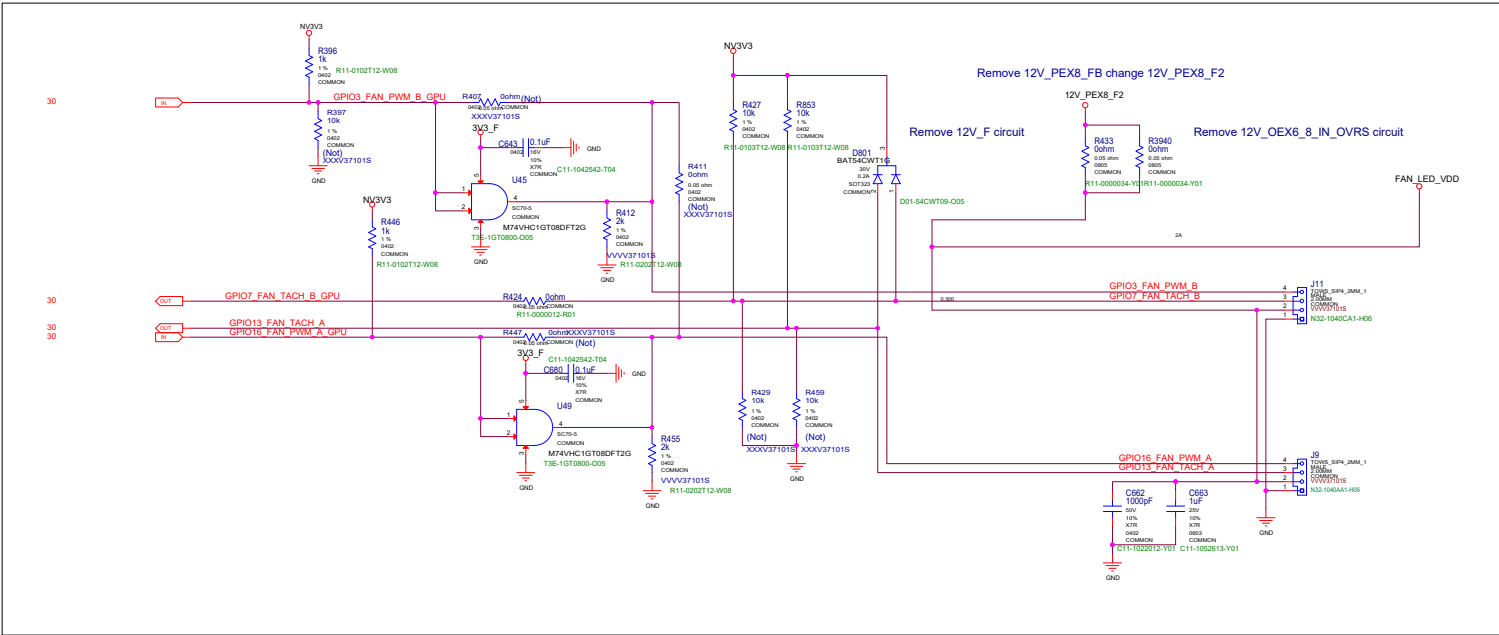
Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX  
and All Input 12Vs





MISC: FAN



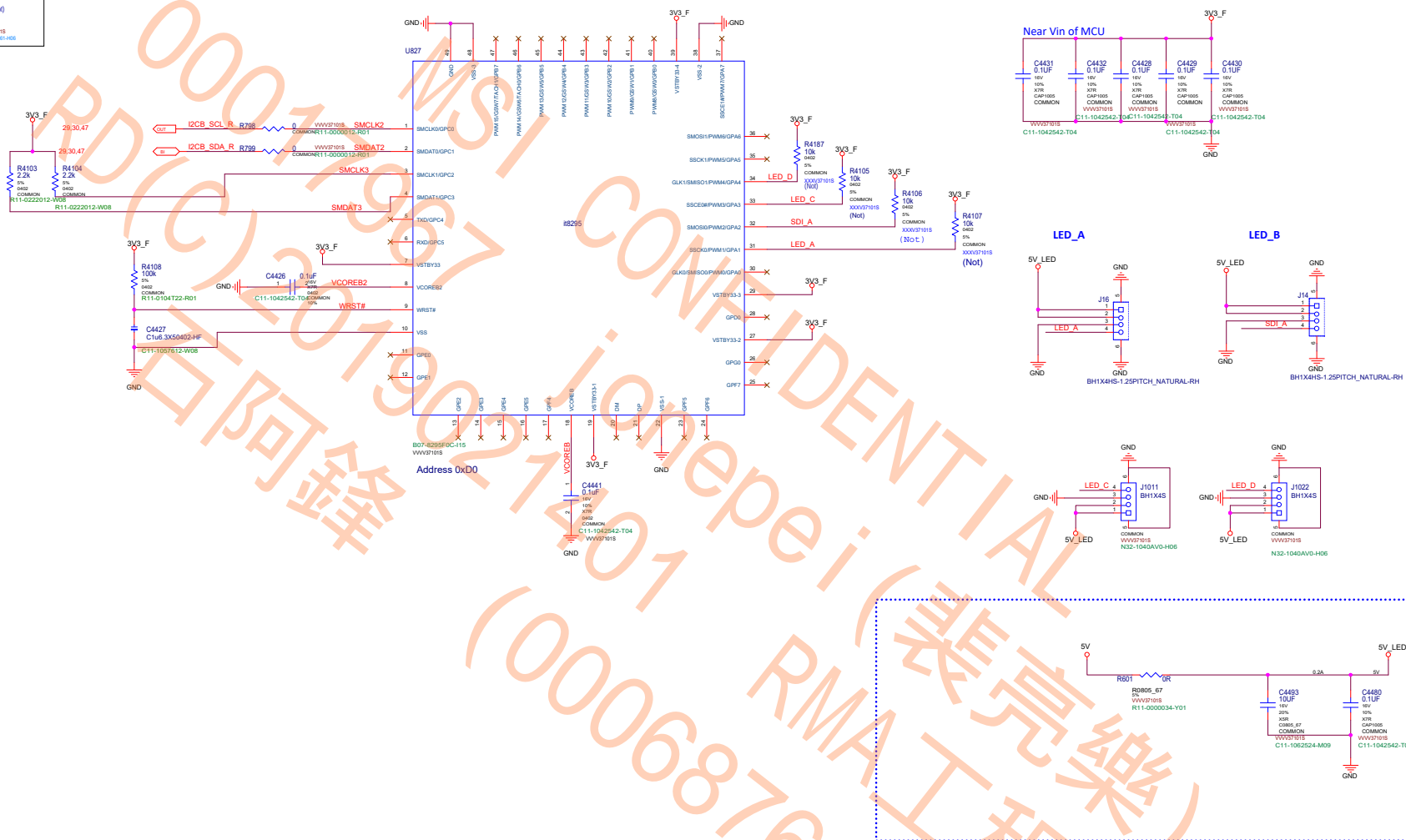
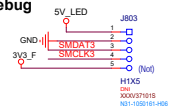
LED BOOST

Remove LED BOOST



## Firmware Programming

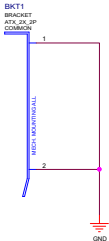
## Debug



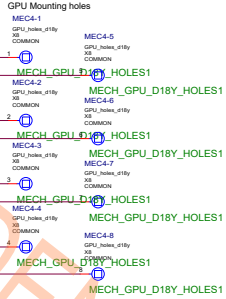
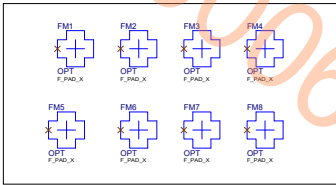
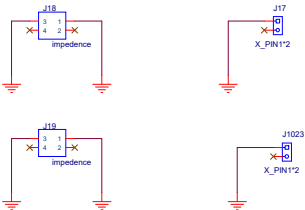
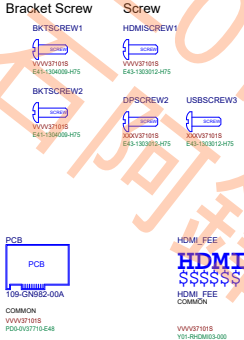
MSI CONFIDENTIAL  
00017967 jonepei (裴亮樂)  
RD(C)2019021401 RMA工程課  
石阿鋒 (00068760)



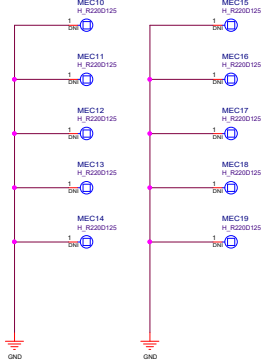
Brackets:



Bracket Screw



Mechanical Holes Symbol



VR THERMAL PROTECTION

41,42,43,44,45  
37,39,40

