P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4X

PCI DEVICE ID 0X0=0X171 FOR NV17-128D.

HISTORY:

X00:
Adapted from E63

X39: 1) Show unused inverter U14F.
2) Connect GPIO2 to Backlight On

X49: 1) Show Stuff Option and explanation for GATEBS and GATE12V. Add R263 to GATEBS stuff option.

X55: 1) Disabled current limit circuits on SC1176. Removed C241, C244, R261, R267, and grounded U13.6 and U13.15
2) Corrected strap options to select 27MHz crystal
3) Corrected values for R248 and R250 to produce expected output voltage for U801
4) Corrected power supply name on J10.170 to +3.3VRUN
5) Corrected R262 value to 221 ohms 1%
6) Changed LP600 to RP600 10K resistor pack and changed connections for BP001 to PTDn signals
7) Removed USER STRAP option resistors R234-R41
8) Added SS3V:SS5V stuff option to power spread spectrum chip from 5VSUS
9) DAC2 Rset R315 changed to 63.4 ohms 1%
10) Corrected spread spectrum settings for 27 MHz operation

X56: 1) Corrected connection on C152 to +3.3VRUN

X59: 1) Changed footprint for spread spectrum part (U8) to be compatible with Cypress W245 part
2) Rewired spread spectrum part to use GPIOs 0 and 5
3) Added protection FETs to DDC lines

X61: 1) Unswapped I2CSCL and I2CSDAT
2) Changed to I2C2 for LCD EDID detection

X62: 1) Deleted R500-R503
2) Connected GPIO6 to SUS_STAT_L

X64: 1) Changed crystal load caps to 18 pF
2) Added R101 to optionally ground TYPEDET
3) Added D12 protection diode pair for CVBS.

X65: 1) Changed R400 to pullup to +3.3VSUS

X68: 1) Changed R300 and R302 to NO STUFF so I2C1 lines not pulled up

A02:

X71: 1) Swapped input rails for switcher U13.
2) Added R/C across L39 and L40 for improved stability.
3) NO-STUFF C242 and C243.
4) Changed clock terminators to 100 ohms.
5) Changed R891 to 820 ohms 1%

X73: 1) Added L406 to power IFP0PLLVDD from +3.3VRUN

X74: 1) Added inverter for SUS_STAT in NVVDD voltage switch

X76: 1) Connected crystal to GPU instead of SS chip

X78: 1)Grounded power supplies for IFP1

X79: 1) Replaced U16 with 2 discrete FETs, Q9 & Q10
2) Connected J1 pin 22 to 3.3VSUS.
3) Connected gate drive for Q4, Q7, and Q8 to 5VRUN

X80: 1) Add power switches for 5VSUS and 3.3VSUS
2) Relabeled J1 P22 as DDCPOWER

X82: 1) Changed decoupling caps at the AGP connector to the corresponding input rails 3.3VSUSIN and 5VSUSIN.
2) added EMI clip (M7)

X83: 1) Added decoupling caps around the MOSFETs to switch 3.3VSUSIN and 5VSUSIN (C905-C908).
2) Added decoupling cap for 3.3VSUS add J1 (C909).

X84: 1) Changed power switches Q101 and Q102 to P-channel. Remove R149, change R148 pullup to 5VSUSIN.
2) Changed drain connection for Q6 to 3.3VSUSIN.

X87: 1) Added Q103 to isolate NV17 AGPVDDQ rail from system AGPVDDQ rail
2) Added C20 and C556 EMI caps near clock terminators.
3) Added R153 and R154

X89: 1) Changed R400 to 3.3K, and R285 to 100 ohms and marked as NO_STUFF

A03:

X92: 1) Corrected connection of Q9 to FB2
2) Change value of R262 to 243 ohms 1% to set FBVDD to 2.58V

X01: 1) Added linear LDO regulators for suspend operation

X02: 1) Added R278 bypass option for Q11

X03: 1) Added R279-282 gate pull-down resistors for switcher FETs

X05: 1) Added C301 plane stitching cap for XTALIN/XTALOUT layer transition.

X06: 1) Changed voltage setting resistors (R262 R264) for FBVDD

X10: 1) Changed voltage setting resistors (R262 R264) for FBVDD. Set FBVDD to 2.50 V for 32 Meg (Samsung) SKUs. R262 = 2.67K, R264 = 1.5K
2) Changed voltage setting resistors for NVVDD, R265 => 1K 1%, R266 => 2K 1%

A04:

X11: 1) Replaced R258 with BAT54A to prevent power back-feed to 5VRUN

X12: 1) Added R273 to allow U13 BSTC source from 5VSUS

X13: 1) Added C304 and C305 as plane stitching caps for XTALOUTBUF reference plane transitions.

X15: 1) Changed LDO enables to FBVDD, added C264 and C265 decoupling caps.
2) Changed BST1 to 12V drive, changed C236 to decouple BST1.
3) NO STUFF R279 and R282

X16: 1) Changed BST1 back to bootstrap powered from +5VRUN, with C236 as bootstrap cap.
2) Added Shottky diode from BST2 to BST1 to aid startup.

X17: 1) Added R287 and C227 as stuff option to allow 12V source for BST1.

X18: 1) Add R272 as stuff option if 12V is used to power BST1

X19: 1) Changed topology of RBST1 and BST1 for ease of layout.

X20: 1) Added R109 and R111 terminators to GND for DVOCLKOUT lines.

X21: 1) Connect SC1176 CL- pins to Vref (as recommended by Semtech)

X22: 1) Changed C236 to .1 uF to reduce loading on BST2 when diode D23 is placed.

X23: 1) Changed stuff option values for R264 to 1.4K for both 32 Meg and 64 Meg SKUs.
2) Added R247 in series with output of LDO U601

X24: 1) Connected drain of Q103 to AGPVDDQ and source to AGPVDDQIN

X25: 1) Changed Q1 and Q2 part numbers to 300-17311-0000-0100 for IRF7311 only

X26: 1) Corrected C20 NVPN for 0402 cap.
2) Removed note on power supply page about 12V gate drive.

X27: 1) Corrected R110, R107,C159, and C556 NVPN to match PCB footprint.

PAGE OVERVIEW

STUFF OPTION	MEANING
These 2 are mutually exclusive. **C3STAT**	C3_STAT_L is the source of AGPSTOP_.
SUSC3STAT	(SUS_STAT_L or C3_STAT_L) is the source of AGPSTOP_.
TRIMVREFCG	On-board trim components for AGPVREFCG
CLKTERM	Differential FB clock terminators.
ALIN	Linear regulator U801 and associated components for analog 3.3V or GPU 2.8V.
These 2 are mutually exclusive. **A33LIN**	U801 output to analog 3.3V
A33SUS	Analog 3.3V derived directly from 3.3VSUS
GPU33	GPU 3.3V derived directly from 3.3VSUS
PID	Parallel Panel ID bits
32MEG	32 Meg frame buffer
64MEG	64 Meg frame buffer
These 2 are mutually exclusive. **GATE12V**	Gate drive for high-side FETs set directly to 12V
GATEBS	Gate drive for high-side FETs derived from bootstrap circuit
ABIOS	Adapter BIOS
SBIOS	System BIOS
These 2 are mutually exclusive. **DESK**	Desktop GPU
WKSTN	GL GPU

140-10072-0000-xxx
602-10072-0000-xxx

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Size	CAGE Code	DWG NO	Rev
Custom			

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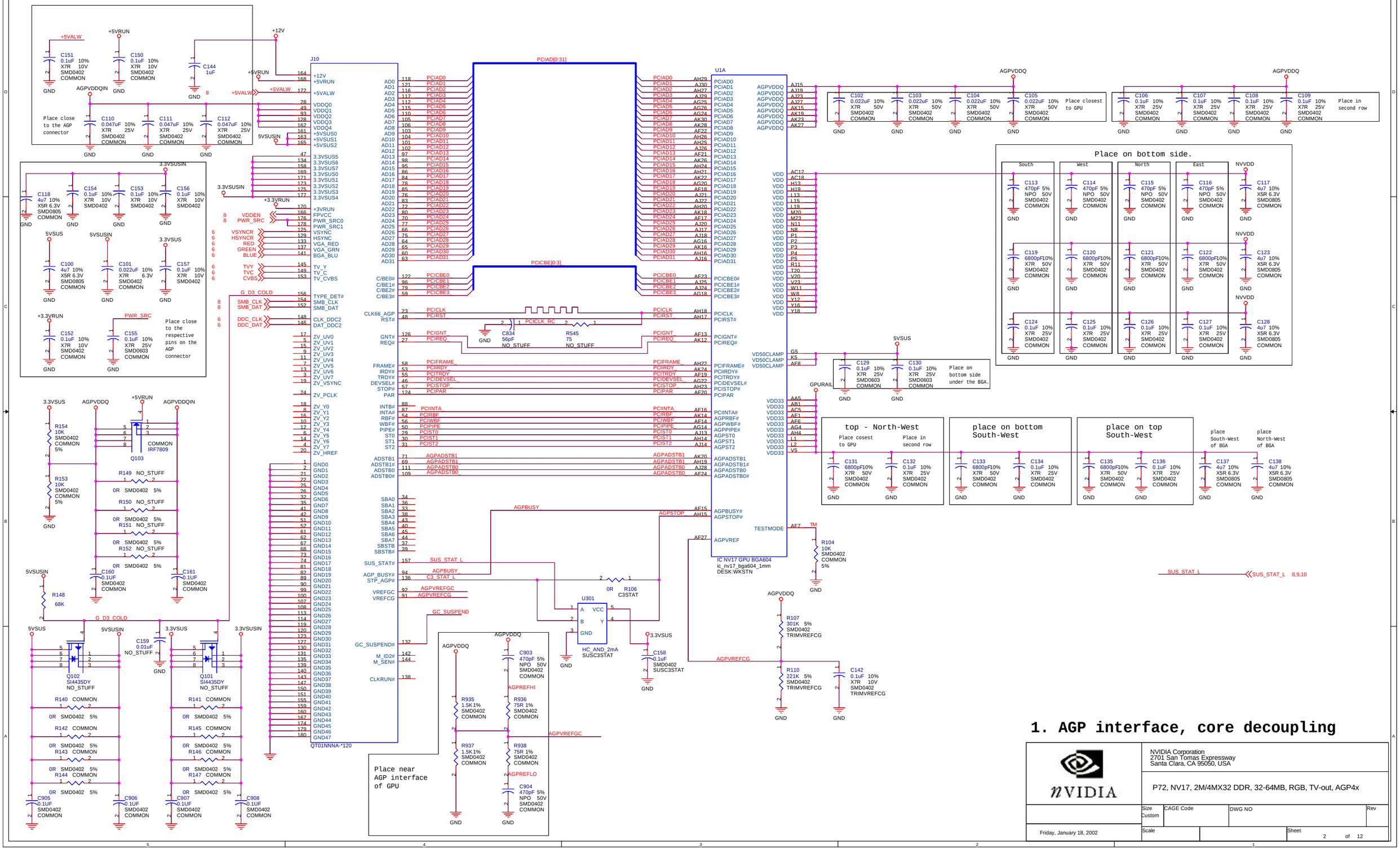
Scale

Sheet 1 of 12


Place close to the AGP connector
Place close to the respective pins on the AGP connector
Place near AGP interface of GPU
Place on bottom side.
South
West
North
East
Place on bottom side under the BGA.
Place closest to GPU
Place in second row
top - North-West
Place cosest to GPU
Place in second row
place on bottom South-West
place on top South-West
place South-West of BGA
place North-West of BGA
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WKSTN
HC_AND_2mA
SUSC3STAT
QT01NNNA-*120
Q102 SI4435DY NO_STUFF
Q101 SI4435DY NO_STUFF
Q103 IRF7809
1. AGP interface, core decoupling
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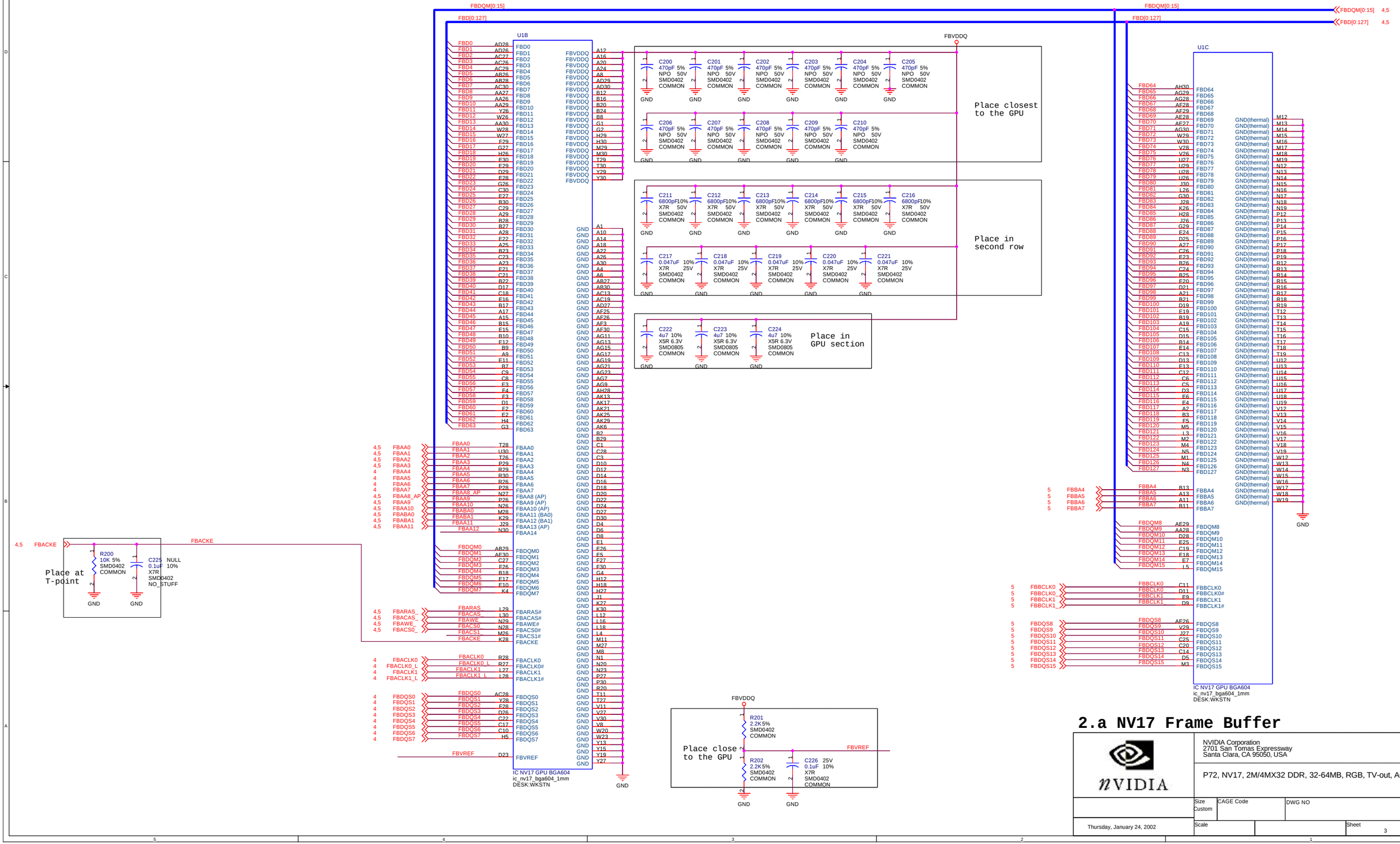
Friday, January 18, 2002
Sheet 2 of 12



2.a NV17 Frame Buffer

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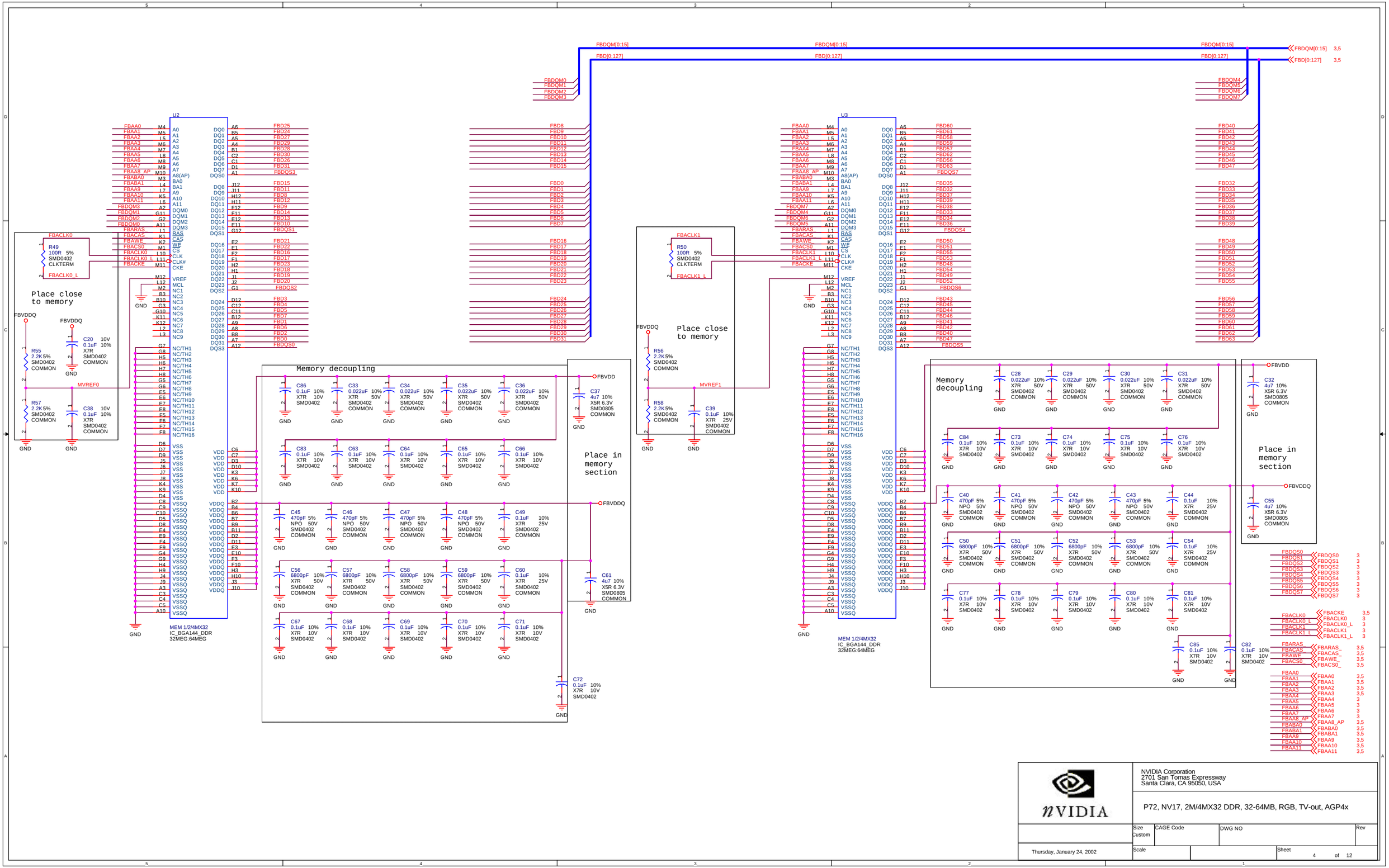
	Size Custom	CAGE Code	DWG NO	Rev
Thursday, January 24, 2002	Scale		Sheet 3 of 12	



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Size	CAGE Code	DWG NO	Rev
Custom			

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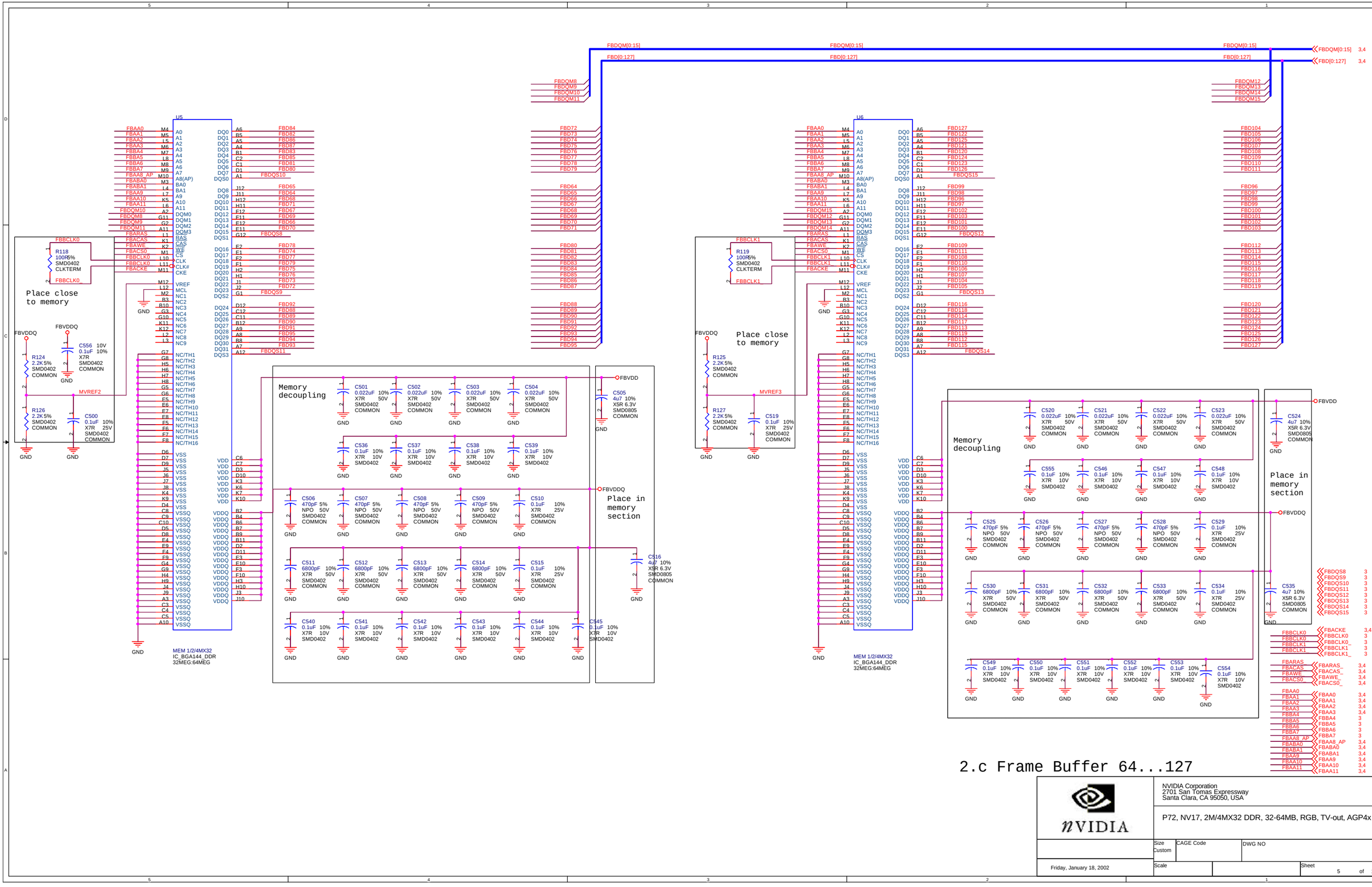
Scale

Sheet 4 of 12


FBDQM[0:15]
FBD[0:127]
U5
MEM 1/2/4MX32
IC_BGA144_DDR
32MEG:64MEG
Place close
to memory
Memory
decoupling
Place in
memory
section
2.c Frame Buffer 64...127
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Friday, January 18, 2002
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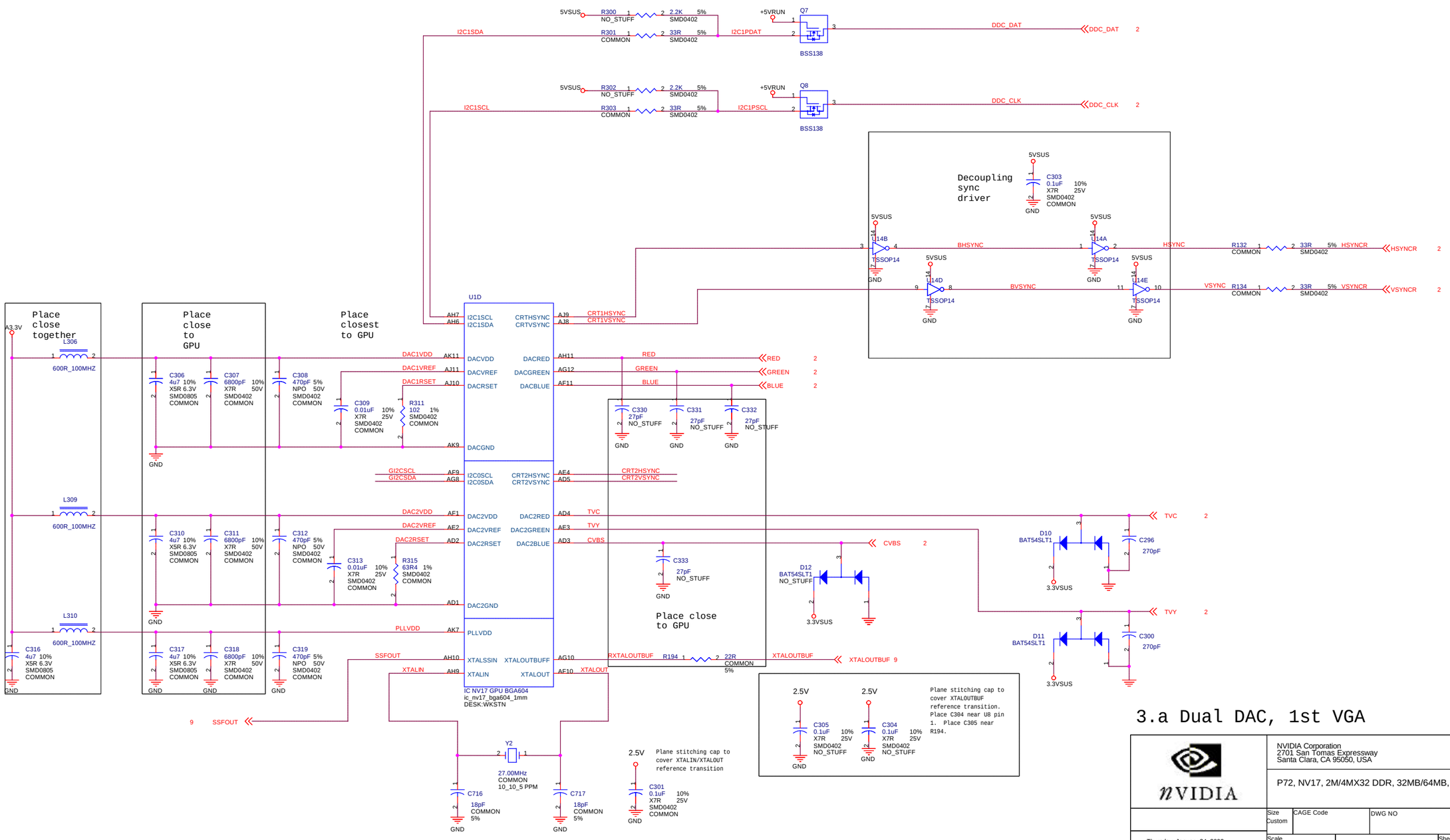

3.a Dual DAC, 1st VGA

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Size	CAGE Code	DWG NO	Rev
Custom			

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3.b Dual DAC, 2nd VGA

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Size	CAGE Code	DWG NO	Rev
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Scale

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Place close together

Place close to GPU

Place closest to GPU

A3.3V
L400 600R_100MHZ
L403 600R_100MHZ
+3.3VRUN
L406 600R_100MHZ COMMON
L405 600R_100MHZ NO_STUFF
C419 4u7 10% X5R 6.3V SMD0805 COMMON
GND

IFP0AVDD
C400 4u7 10% X5R 6.3V SMD0805 COMMON
C402 6800pF 10% X7R 50V SMD0402 COMMON
C403 470pF 5% NPO 50V SMD0402 COMMON

IFP0BVDD
C405 4u7 10% X5R 6.3V SMD0805 COMMON
C406 6800pF 10% X7R 50V SMD0402 COMMON
C407 470pF 5% NPO 50V SMD0402 COMMON
C408 0.1uF 10% X7R 25V SMD0402 COMMON
R404 1K SMD0402 COMMON 1%

IFP0PLLVDD
C410 4u7 10% X5R 6.3V SMD0805 COMMON
C411 6800pF 10% X7R 50V SMD0402 COMMON
C412 470pF 5% NPO 50V SMD0402 COMMON

U1E
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WKSTN

IFP0AVDD	Y1	IFP0IOAVDD	
IFP0BVDD	AC1	IFP0IOBVDD	
IFP0VREF	W2	IFP0VREF	
IFP0RSET	V1	IFP0RSET	
	W5	IFP0IOGND	
IFP0PLLVDD	W1	IFP0PLLVDD	
	AB5	IFP0PLLGND	
	U1	IFP1IOVDD	
	T2	IFP1VREF	
	R1	IFP1RSET	
	T5	IFP1IOGND	
	T1	IFP1PLLVDD	
	V4	IFP1PLLGND	

TXD0#	V2	TXD0	DFPTX0-
TXD0	V3		DFPTX0+
TXD1#	W3	TXD1	DFPTX1-
TXD1	W4		DFPTX1+
TXD2#	Y2	TXD2	DFPTX2-
TXD2	Y3		DFPTX2+
TXD3#	AA1	TXD3	TXD3-
TXD3	AA2		TXD3+
TXD4#	AA3	TXD4	DFPTX4-
TXD4	AA4		DFPTX4+
TXD5#	AB2	TXD5	DFPTX5-
TXD5	AB3		DFPTX5+
TXD6#	AC2	TXD6	DFPTX6-
TXD6	AC3		DFPTX6+
TXD7#	AB4	TXD7	TXD7-
TXD7	AC4		TXD7+
TXC0#	U4	TXC0	DFPTXC0-
TXC0	U5		DFPTXC0+
TXC1#	Y4	TXC1	DFPTXC1-
TXC1	Y5		DFPTXC1+
TXD8#	R5	TXD8	TXD8-
TXD8	R4		TXD8+
TXD9#	T3	TXD9	TXD9-
TXD9	T4		TXD9+
TXD10#	U2	TXD10	TXD10-
TXD10	U3		TXD10+
TXC2#	R2	TXC2	TXCLK2-
TXC2	R3		TXCLK2+
I2C2SDA	AH8	I2C2SDA	I2C2SDA 9
I2C2SCL	AJ7	I2C2SCL	I2C2SCL 9
GPIO7	J5	GPIO7	GPIO7 10
GPIO6	A3	SUS_STAT_L	SUS_STAT_L 2,9,10
GPIO5	A5	GPIO5	GPIO5 9
GPIO4	B6	GPIO4	GPIO4
GPIO3	C7	VDDEN	VDDEN 2
GPIO2	D7	GPIO2	GPIO2
GPIO1	E8	GPIO1	GPIO1
GPIO0	B5	GPIO0	GPIO0 9

R415 0R SMD0402 COMMON 5%
R421 0R SMD0402 COMMON 5%

GPIO4
R550 10K NO_STUFF

+5VALW
PWR_SRC
Q4 2N7002
+5VRUN
PSRC_G
R165 68K
C323 0.1uF
R164 100K
Q3 SI4435DY
IINV_PWR_SRC
PSRC_GR
GPIO2
R561 10K SMD0402
5VSUS

J1
FI-D50SB-E1500

1	PWR_SRC0		
2	PWR_SRC1		
3	GND_0		
4	5V_SUS		
5	+5VALW		
6	GND_1		
7	SMB_DAT		
8	SMB_CLK		
9	GND_2		
10	BKLT_ON		
11	PWR_SRC2		
12	GND_3		
13	PID3_I2CDAT		
14	PID2_I2CCLK		
15	GND_4		
16	PID1	MGND1	51
17	PID0		
18	GND_5	MGND2	52
19	LCD_VCC0		
20	LCD_VCC1	MGND3	53
21	GND_6		
22	DDCPOWER	MGND4	54
23	NC_CLCD_P23		
24	GND_7	MGND5	55
25	PID2_I2C_CLK		
26	PID3_I2C_DAT	MGND6	56
27	GND_8		
28	TXOUT_U0-	MGND7	57
29	TXOUT_U0+		
30	GND_9	MGND8	58
31	TXOUT_U1-		
32	TXOUT_U1+	MGND9	59
33	GND_10		
34	TXOUT_U2-	MGND10	60
35	TXOUT_U2+		
36	GND_11	MGND11	61
37	TXCLK_U-		
38	TXCLK_U+	MGND12	62
39	GND_12		
40	TXOUT_L0-		
41	TXOUT_L0+		
42	GND_13		
43	TXOUT_L1-		
44	TXOUT_L1+		
45	GND_14		
46	TXOUT_L2-		
47	TXOUT_L2+		
48	GND_15		
49	TXCLKL_L-		
50	TXCLK_L+		

2 SMB_DAT
2 SMB_CLK
PID3
PID2
PID1
PID0
I2C2SCL
I2C2SDA
DFPTX0-
DFPTX0+
DFPTX1-
DFPTX1+
DFPTX2-
DFPTX2+
DFPTXC0-
DFPTXC0+
DFPTX4-
DFPTX4+
DFPTX5-
DFPTX5+
DFPTX6-
DFPTX6+
DFPTXC1-
DFPTXC1+

3.3VSUS
C909 0.1UF SMD0402 COMMON

LCD_VCC
LCDVCC_GR
R163 100K
+12V
3.3VSUSIN
Q6 SI4410DY
C322 0.01uF
Q5 2N7002
C329 0.1uF
C328 4u7 10% X5R 6.3V SMD0805 COMMON
VDDEN
VDDENJ
U14C TSSOP14
R548 10K SMD0402
U14F TSSOP14

RP600
12	VIPHAD1	VIPHAD1	PID3
12	VIPHAD0	VIPHAD0	PID2
12	VIPD1	VIPD1	PID1
11,12	VIPD0	VIPD0	PID0

10K PID

RP601 10K PID

C620 0.01uF SMD0402 PID
C621 0.01uF SMD0402 PID
C622 0.01uF SMD0402 PID
C623 0.01uF SMD0402 PID

4. Panel

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Size	CAGE Code	DWG NO	Rev
Custom			

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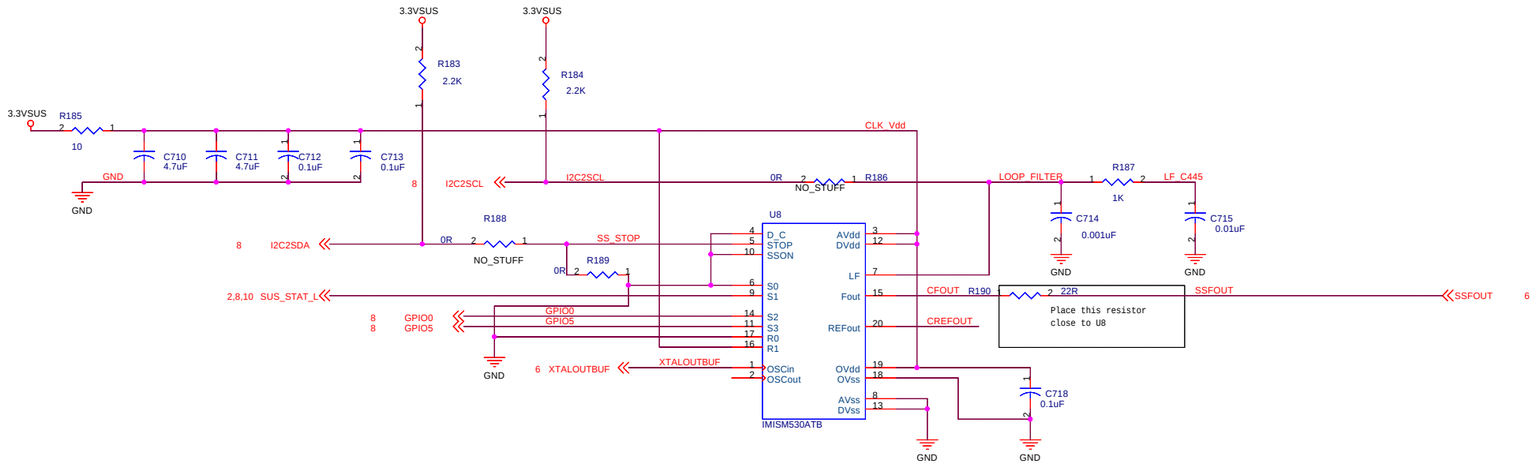

5.b Spread Spectrum Control

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Size	CAGE Code	DWG NO	Rev
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Analog 3.3V

U600 Vout = 1.175 - ((U601 Vout) - 1.175)*(R274/R276)

U601 Vout = 1.175 * (1 + R275/R277)

R275	R277	Vout
3.57K	3.32K	2.438V

Vo=(1.20 * (R248 + R250)) / R250

R248	R250	Nominal Output Voltage
215R	115R	3.44V
200R	115R	3.29V
154R	115R	2.81V
21K	12.1K	3.28V

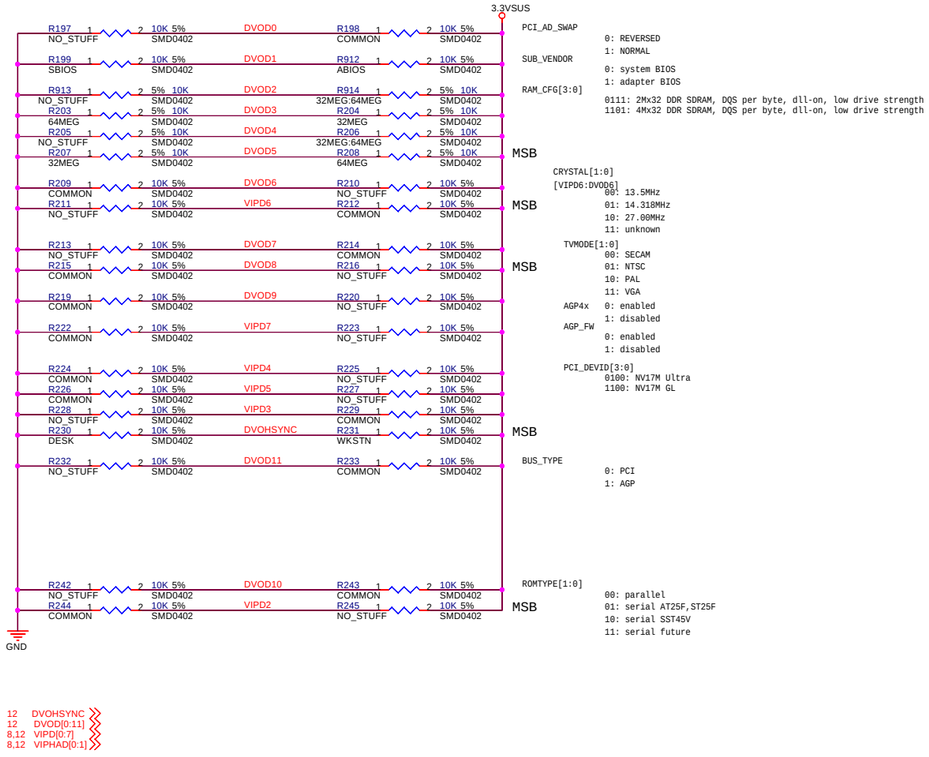
3.3V@1.5A max
Drop Out
350mV @ 1.5A

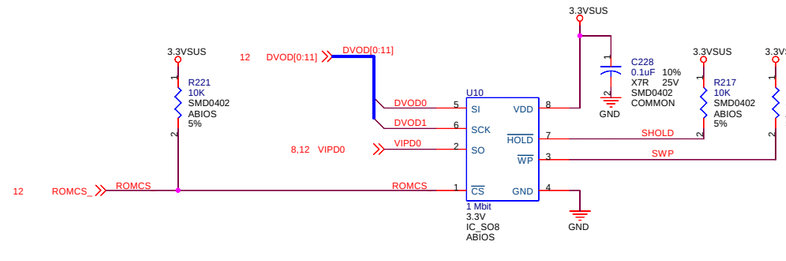
1.2V/1.5V@3A

(FBVDD)
2.5V@3A

NVVDD Switching	SUS_STAT =0	SUS_STAT = 1
GPIO7 = 0	NVVDD = 1.2V	NVVDD = 0.94V
GPIO7 = 1 or not driven	NVVDD = 1.35V	NVVDD = 0.96V

Title	P72, NV17, 2M/4MX32 DDR, 32-64MB, RGB, TV-out, AGP4x	
Size: Custom	Document Number: <Doc>	Rev: A
Date: Thursday, January 24, 2002	Sheet 10 of 12	





7. BIOS, Strapping

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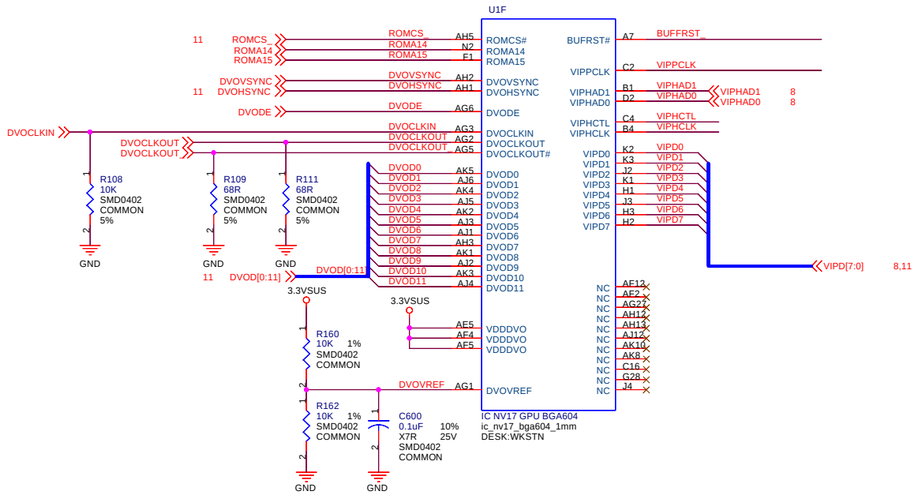
Size	CAGE Code	DWG NO	Rev
Custom			

Thursday, January 24, 2002

Scale

Sheet 11 of 12



5.a TV out,video capture,stereo

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	Size: Custom; CAGE Code; DWG NO; Rev
Thursday, January 24, 2002	Scale; Sheet 12 of 12