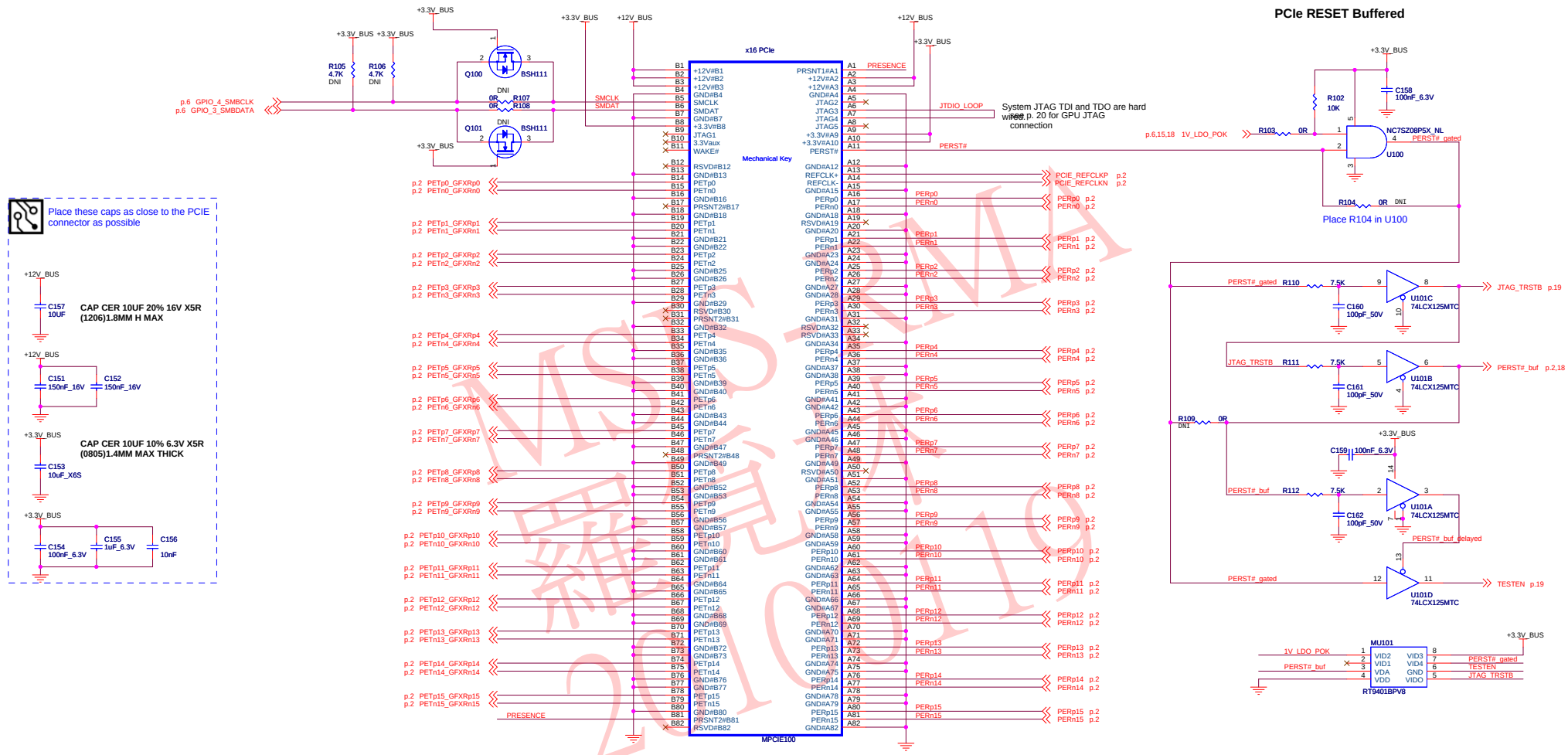
PCI-EXPRESS EDGE CONNECTOR

C013



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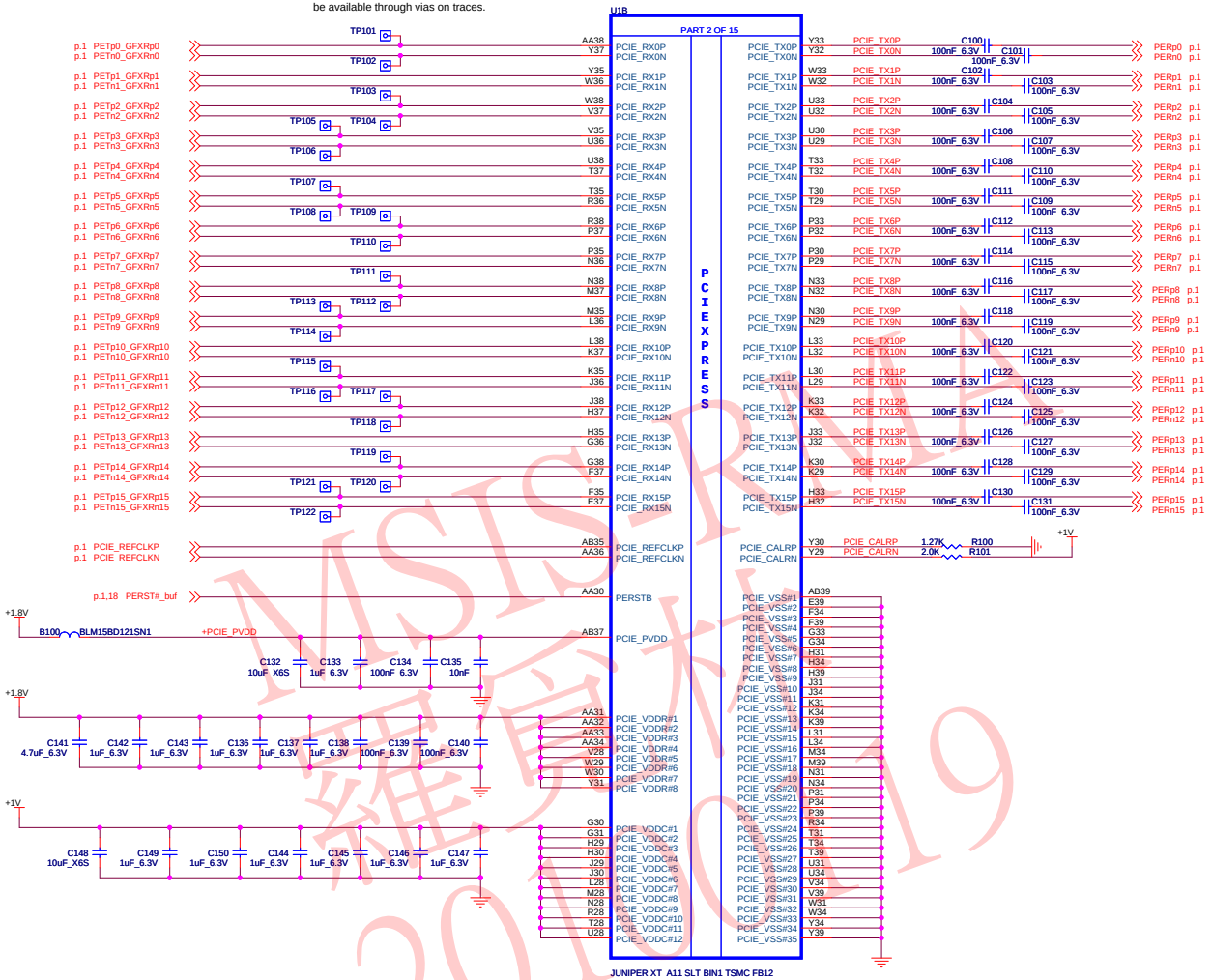
(2) JUNIPER PCIe Interface

NOTE: Some of the PCIE testpoints will be available through vias on traces.



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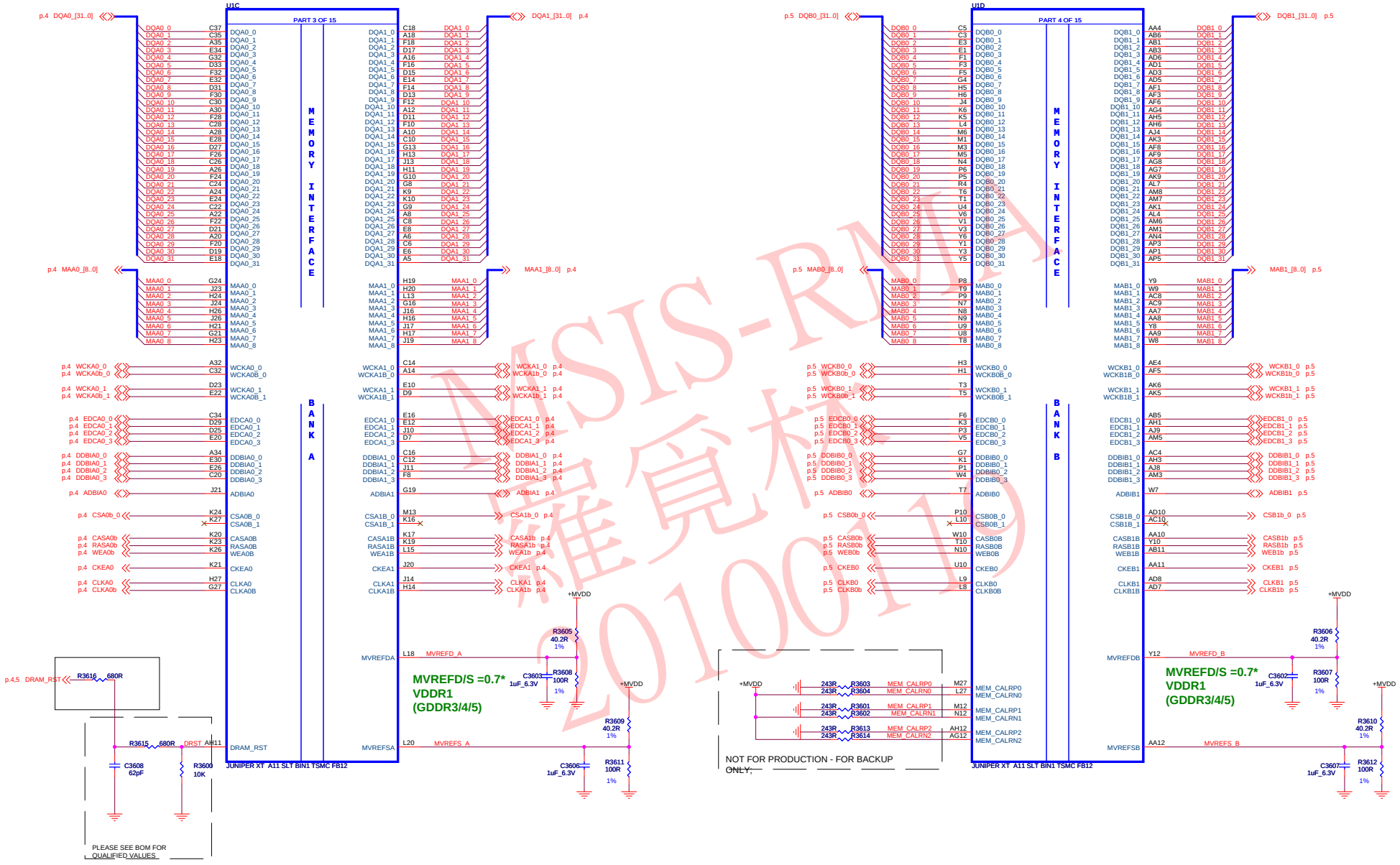
(3) JUNIPER MEM Interface Ch A&B



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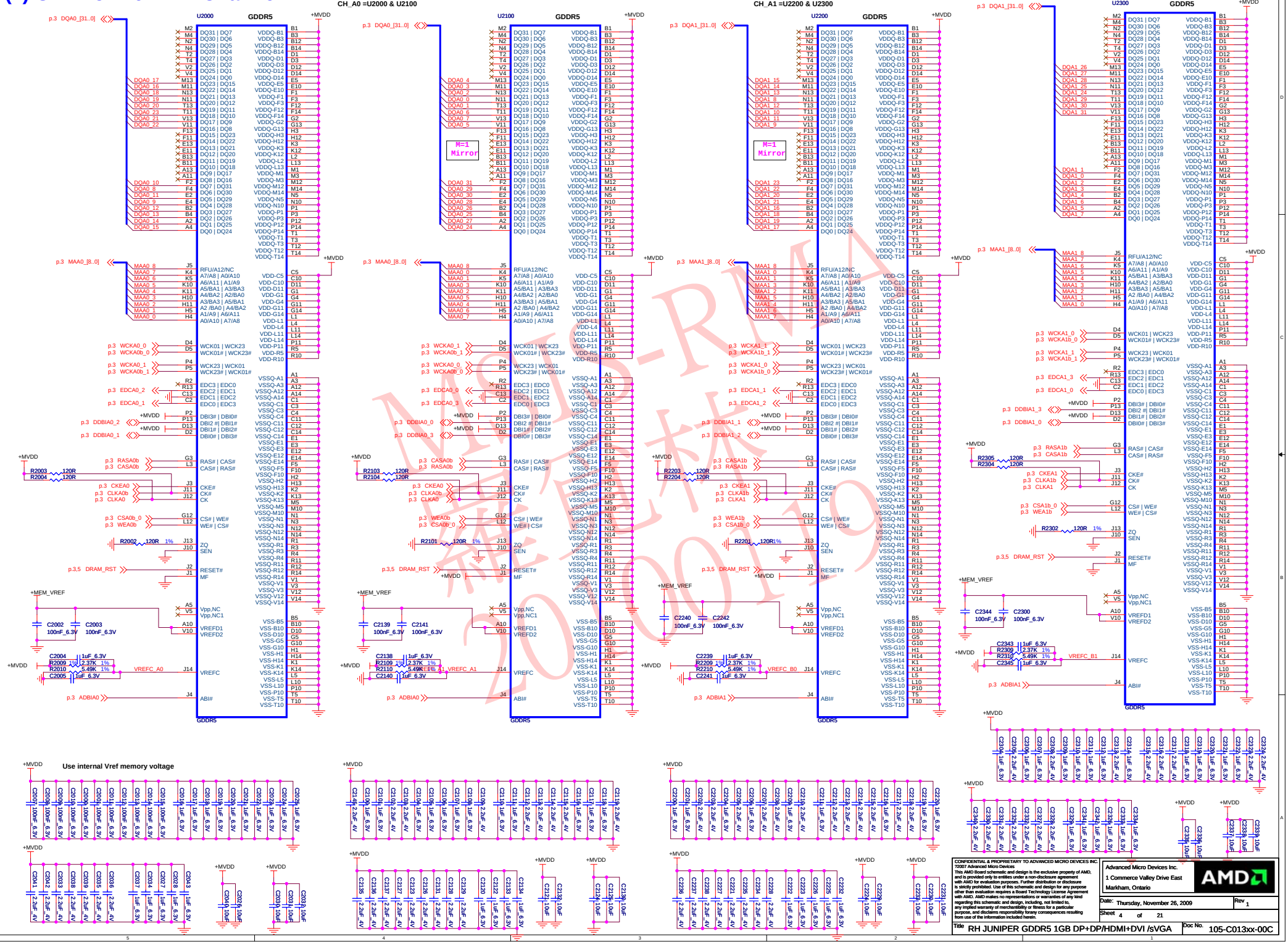
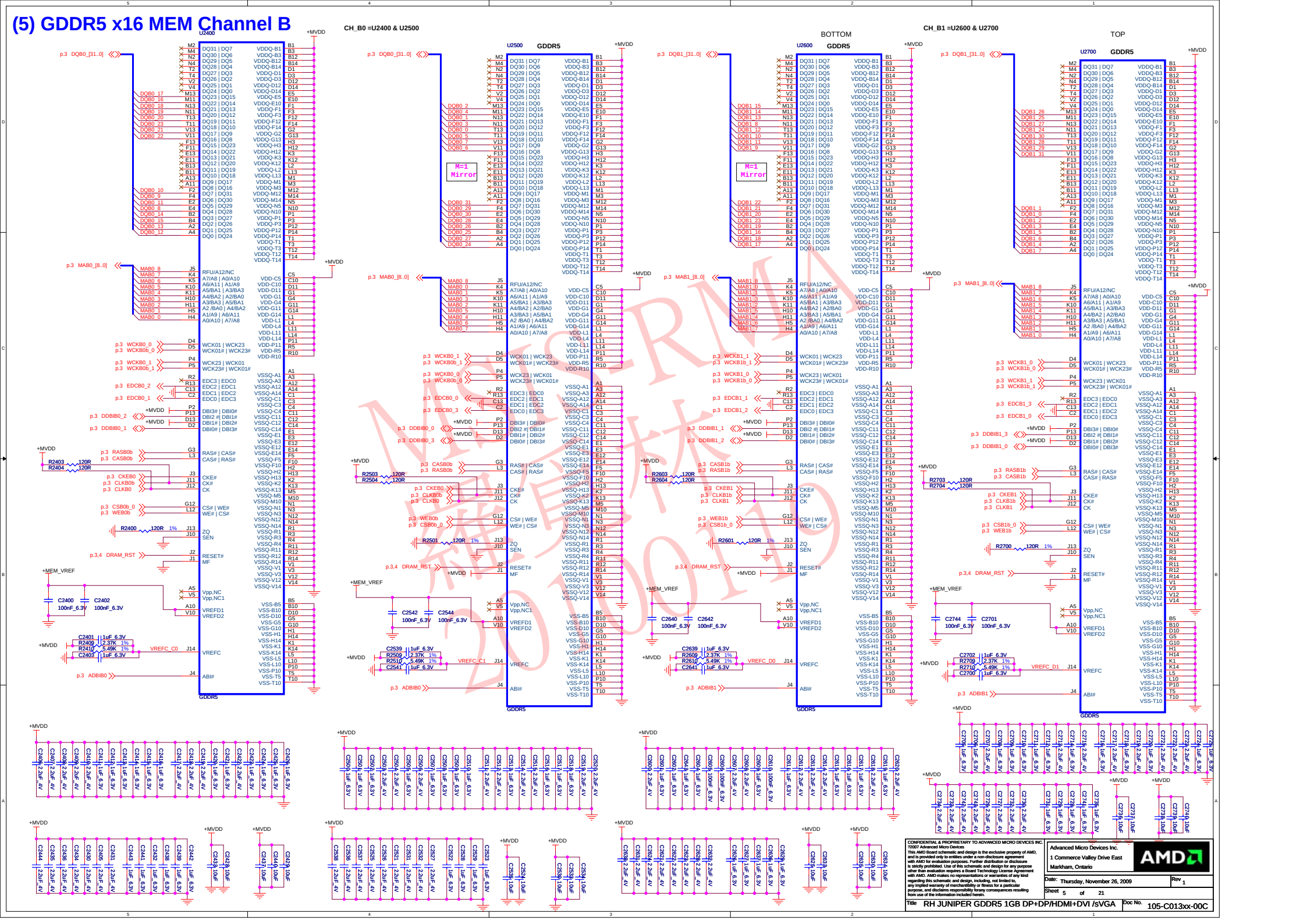
(4) GDDR5 x16 MEM Channel A



(5) GDDR5 x16 MEM Channel B



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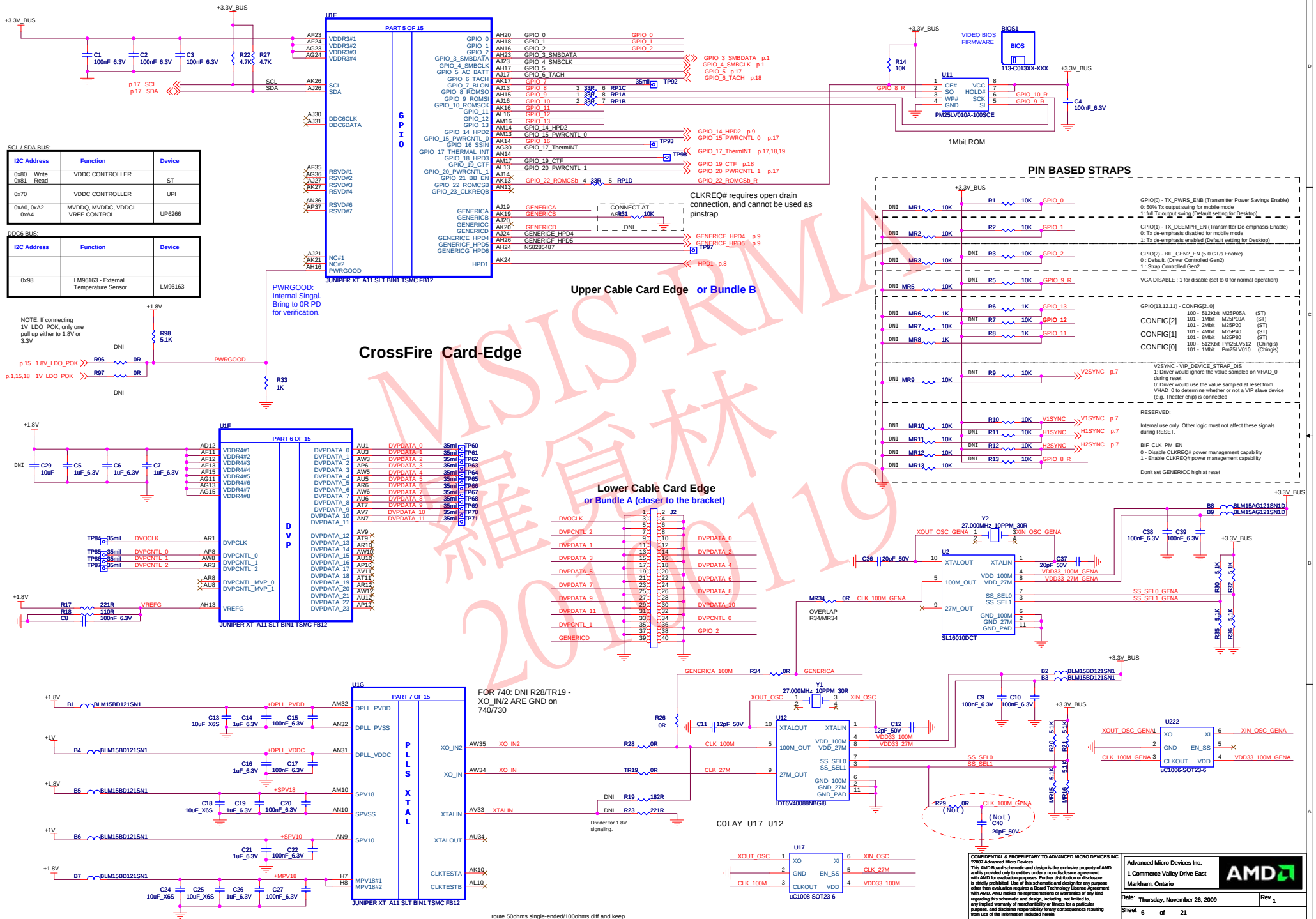
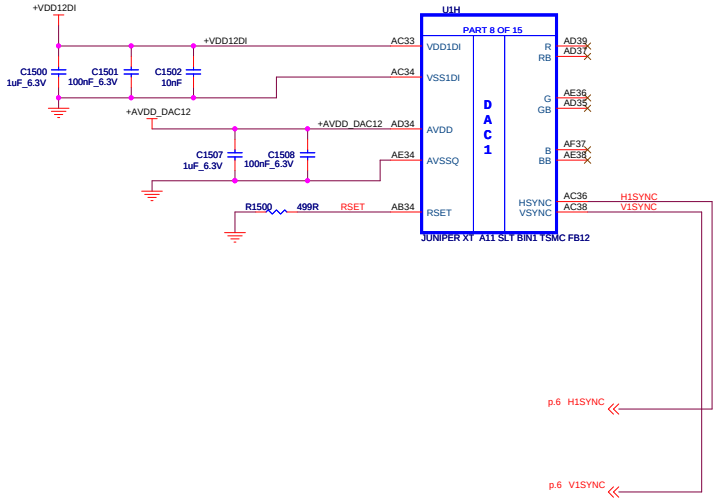
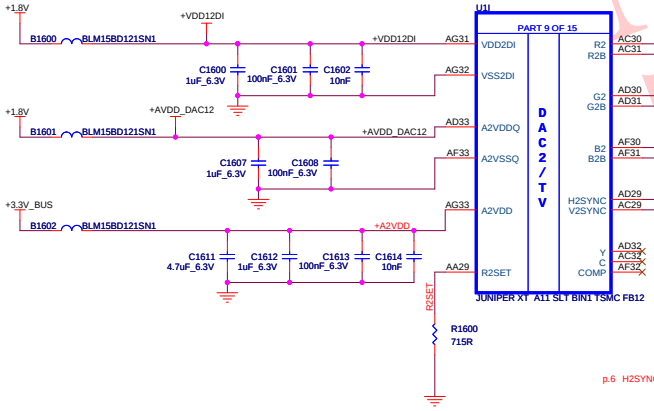
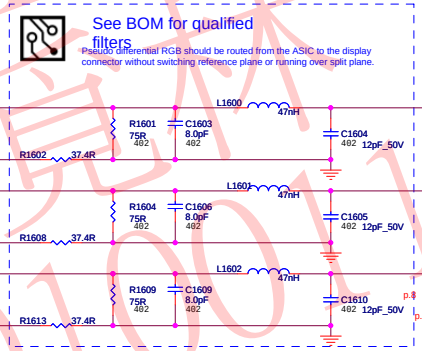
(06) JUNIPER GPIOs Strap CF XTAL OSC

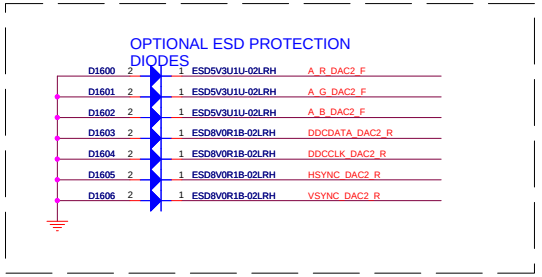


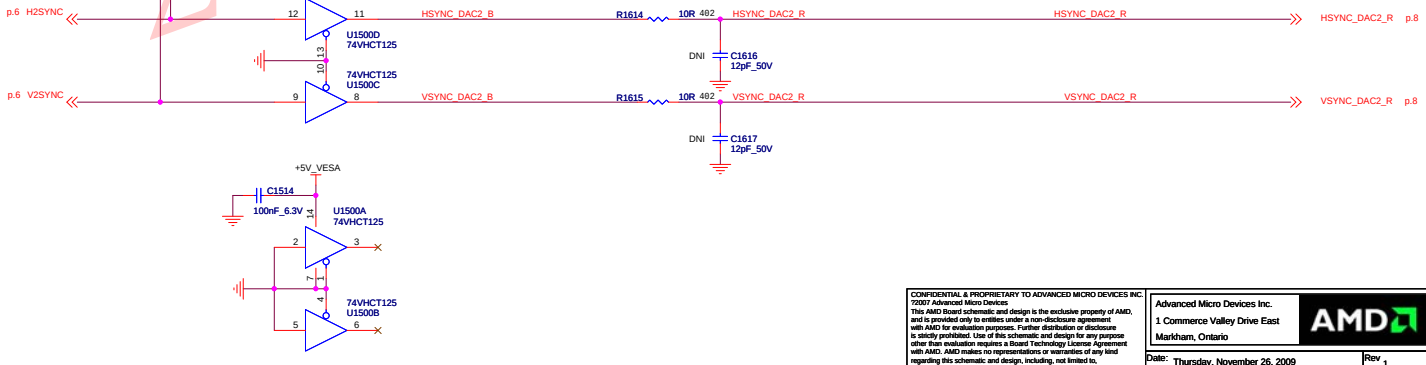
(07) JUNIPER DAC1 and DAC2











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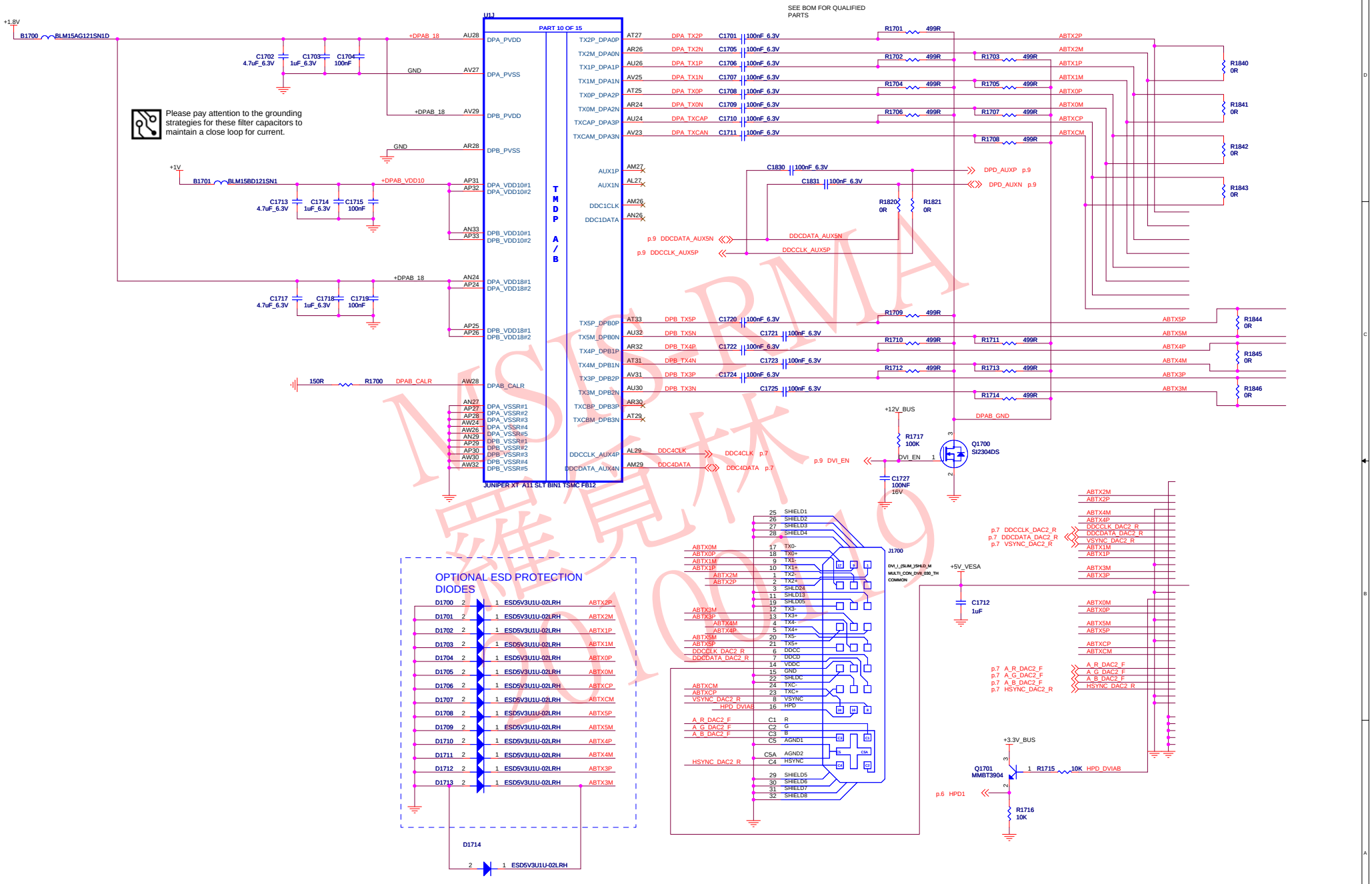
(08) JUNIPER TMDP A&B dDVI-I TOP



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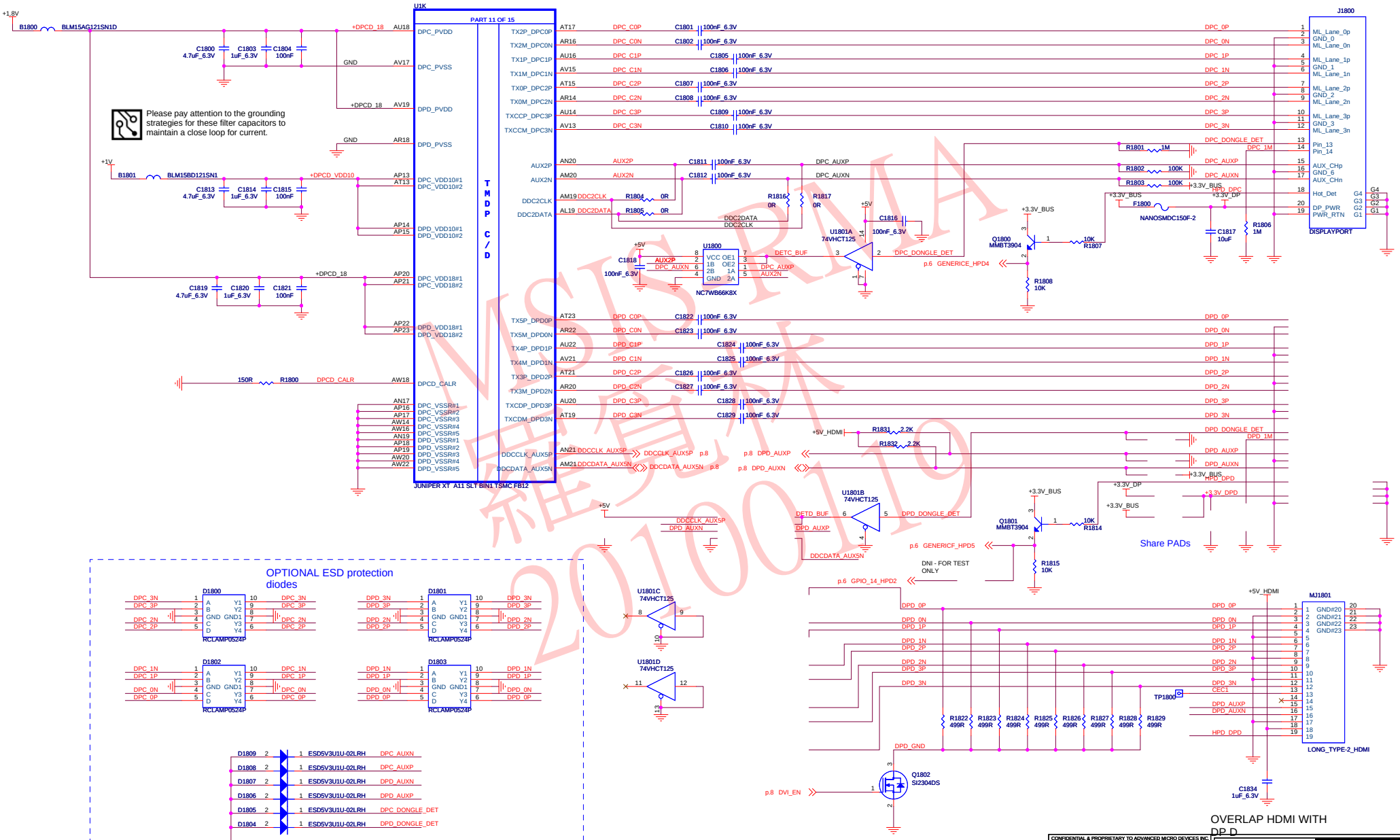
(09) JUNIPER Display Port C & Display Port/HDMI D

AUX/DDC:
FOR 740/730, INSTALL 0R ON ASIC-SIDE OF AC COUPLING CAPS ONLY;
FOR JUNIPER, INSTALL 0R ON CONNECTOR SIDE OF AC COUPLING CAPS ONLY;



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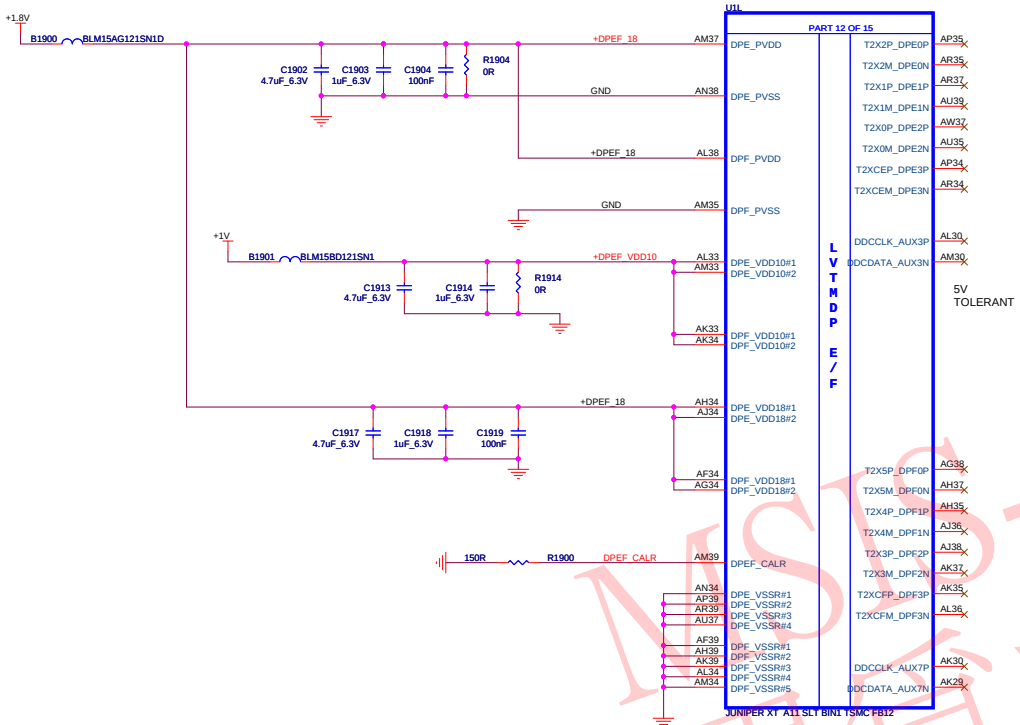
(10) JUNIPER LVTMDP E&F



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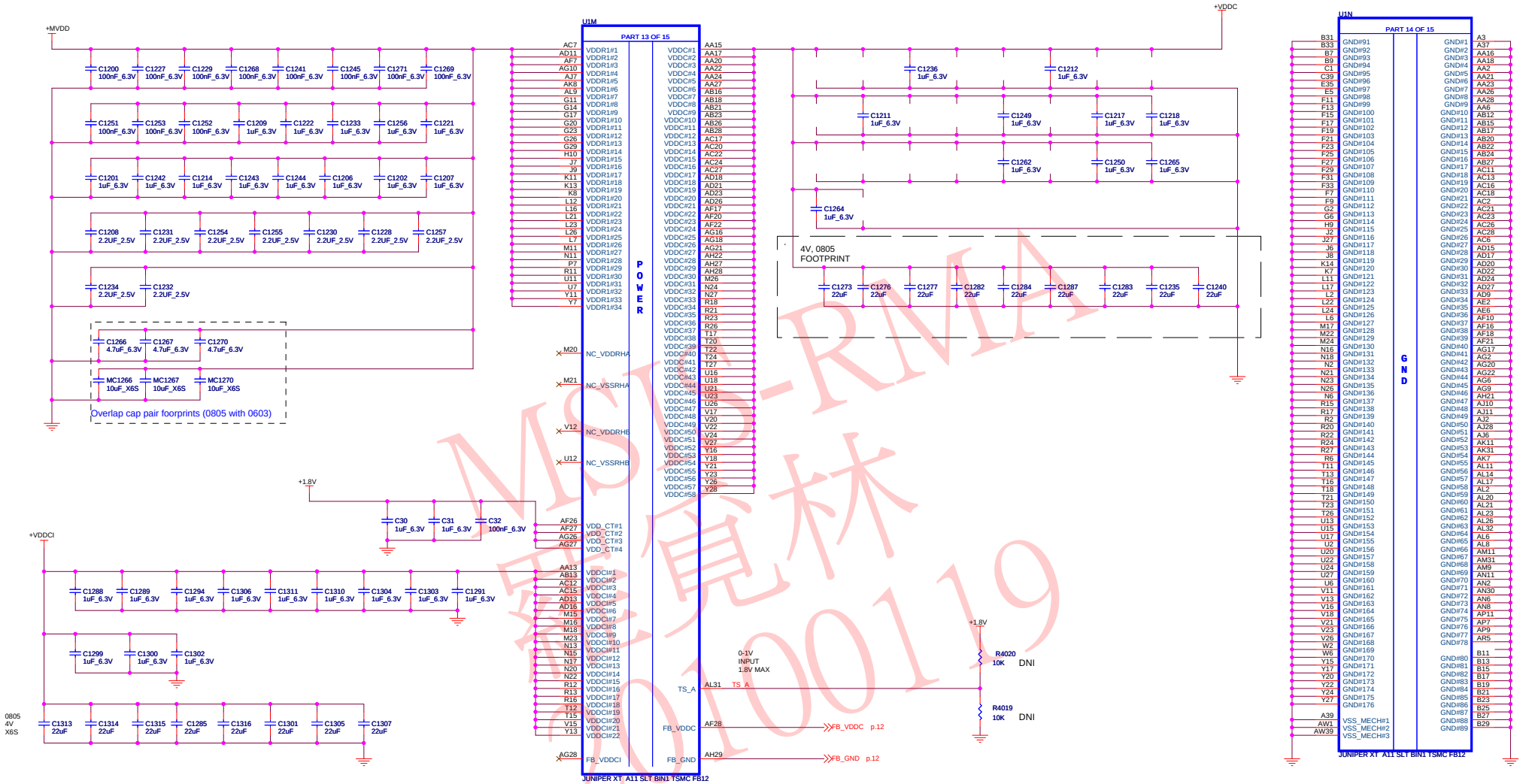
(11) JUNIPER Power & GND



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(12) VDDC

PHASE 1

PHASE 2

PHASE 3

Output Bulk CAPs

Output MLCC

Input MLCC

Input Bulk CAPs

Table 1 MODE Pin Definition Table

VPM Mode	Mode Pin Status	Mode Pin Voltage (V)	Phase Operation		
			Phase 1	Phase 2	Phase 3
3-Phase Mode	0	0	Enabled	Enabled	Enabled
2-Phase Mode	1	3.3	Enabled	Enabled	Disabled
1-Phase Mode	Floating	~1.7	Enabled	Disabled	Disabled

Circuitry that have to be placed close to the device:
- current sense,
- compensation network,
- thermal compensation network (Droop, OCP, etc)

VR_HOT/EN Circuit

UP

SM

Table 1 VRHOT/EN Table

EN	Q1	Q2	VR_HOT/EN	IC	VR_HOT	GPIO
1	on	off	0	Disabled	/	1
0	off	on	5V	Enabled	No Warning	0
0	off	off	0.45V	Enabled	Warming	1

Table 1 VRHOT/EN Table

EN	Q1	Q3	Q2	VR_HOT/EN	IC	VR_HOT	GPIO
1	on	on	on	0	Disabled	/	0
0	off	on	on	1.5V	Enabled	No Warning	0
0	off	off	off	3.3V	Enabled	Warming	1

CASE1, CASE3 Special Case Power Up Detection

NOTE: This is for the IC that uses VCC2 for EXT_12V Detection.

Table 5 MODE Pin & Phase3 Strip Detection Table

App	Condition	Mode Pin	VPM Mode	Phase 3	IC Behavior
CASE 1	PwrUp without EXT_12V Cable	1	2-Ph Mode	Open	IC enabled without detecting EXT_12V (VCC2) voltage.
CASE 3	PwrUp with EXT_12V Cable	1	2-Ph Mode	Pull Down	Detect EXT_12V (VCC2) voltage before IC enable.

RT (For HW ver IC)

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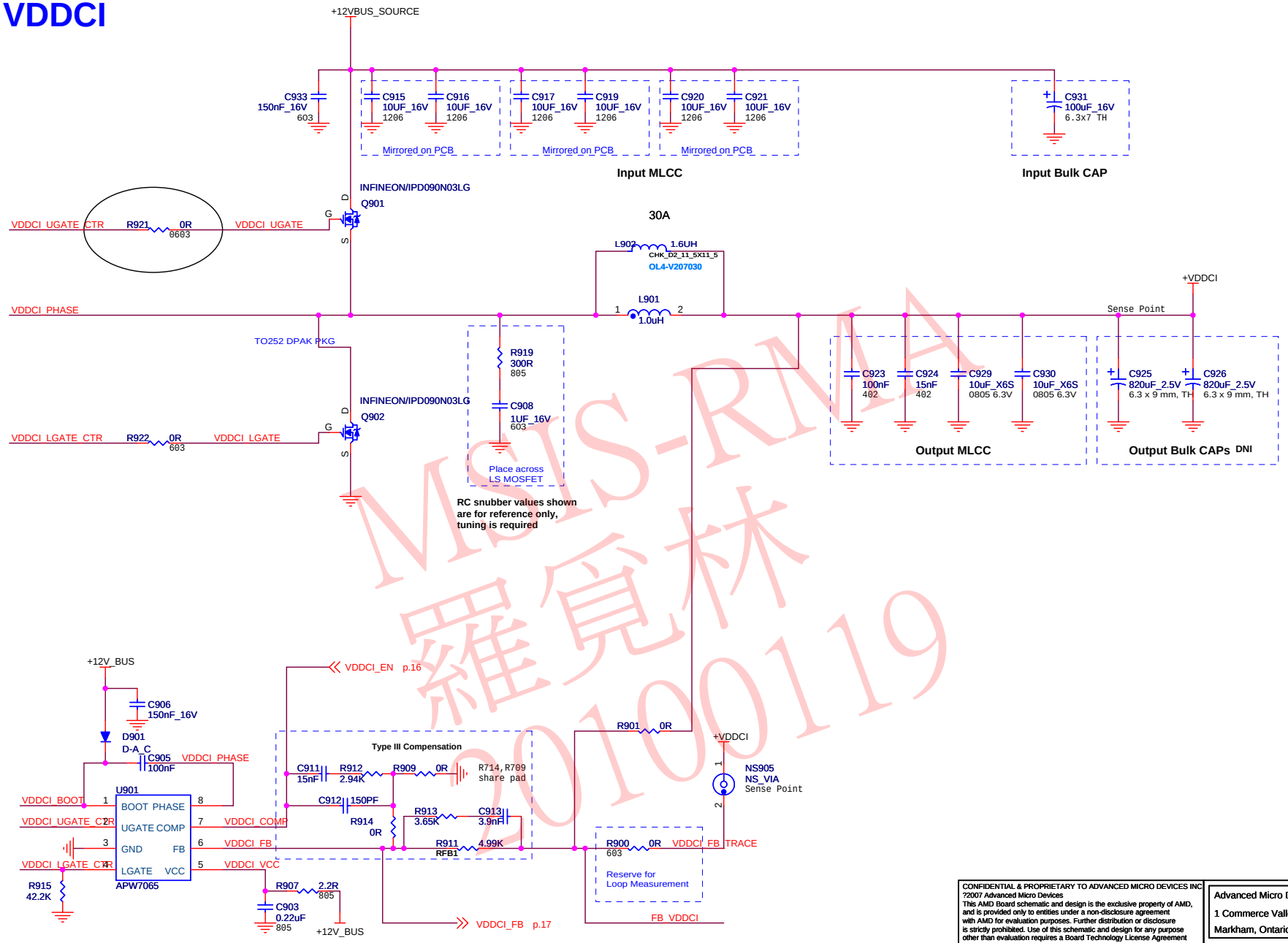
(13) VDDCI



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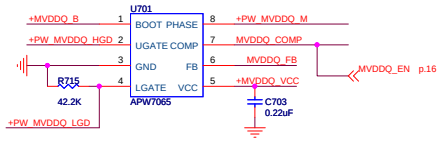
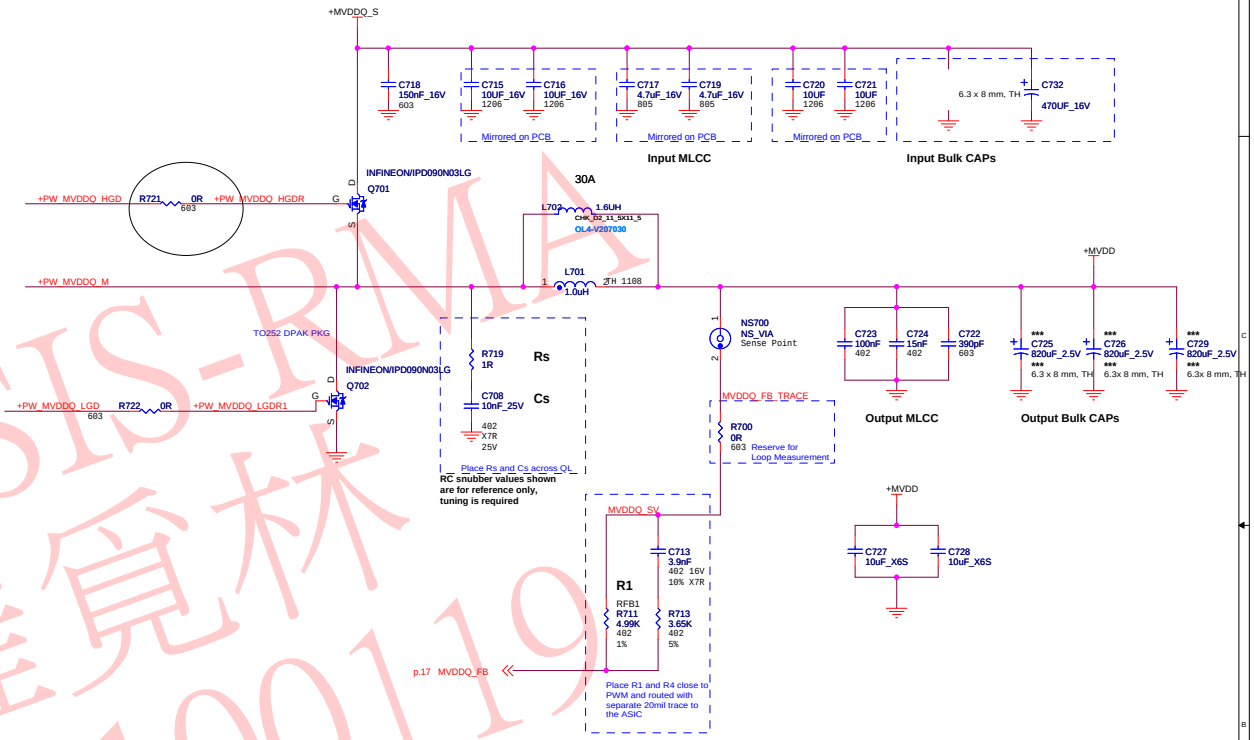
(14) MVDDQ

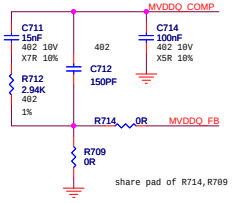


Layout guideline

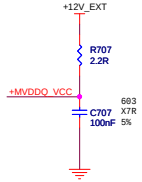
1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



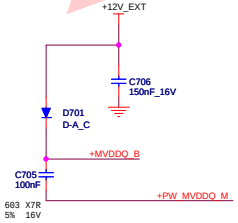
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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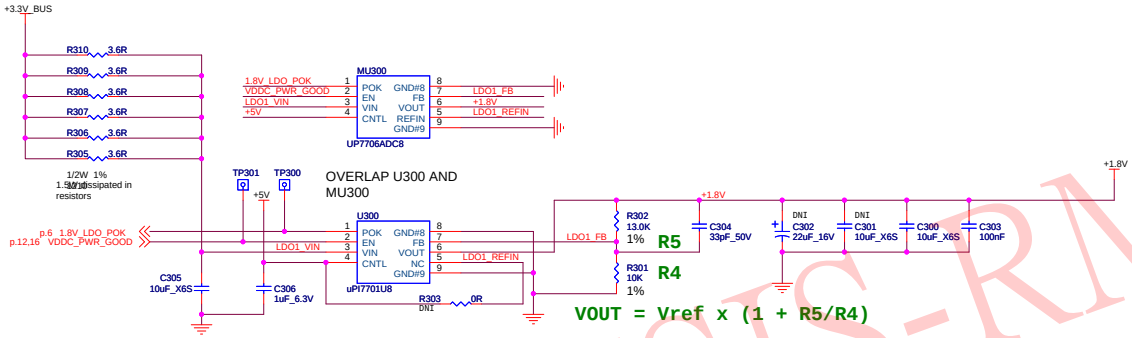
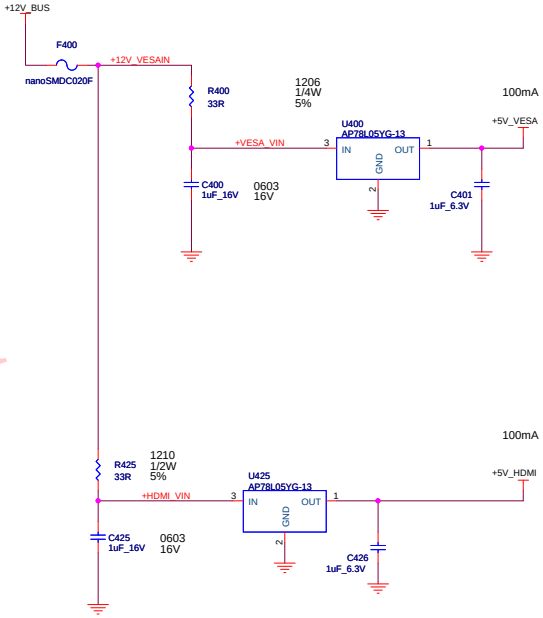
(15) Linear Regulators

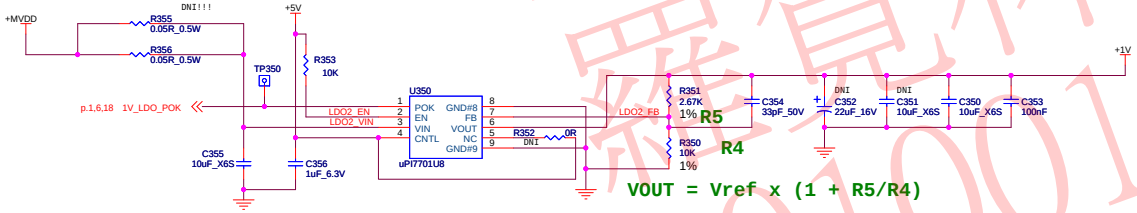
Regulators for +5V, +5V_VESA and +5V_HDMI

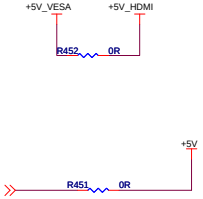
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



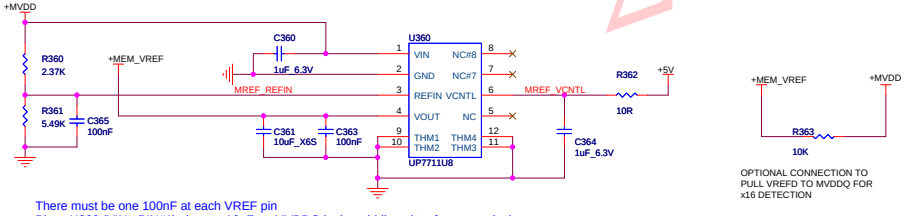


LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling





Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ



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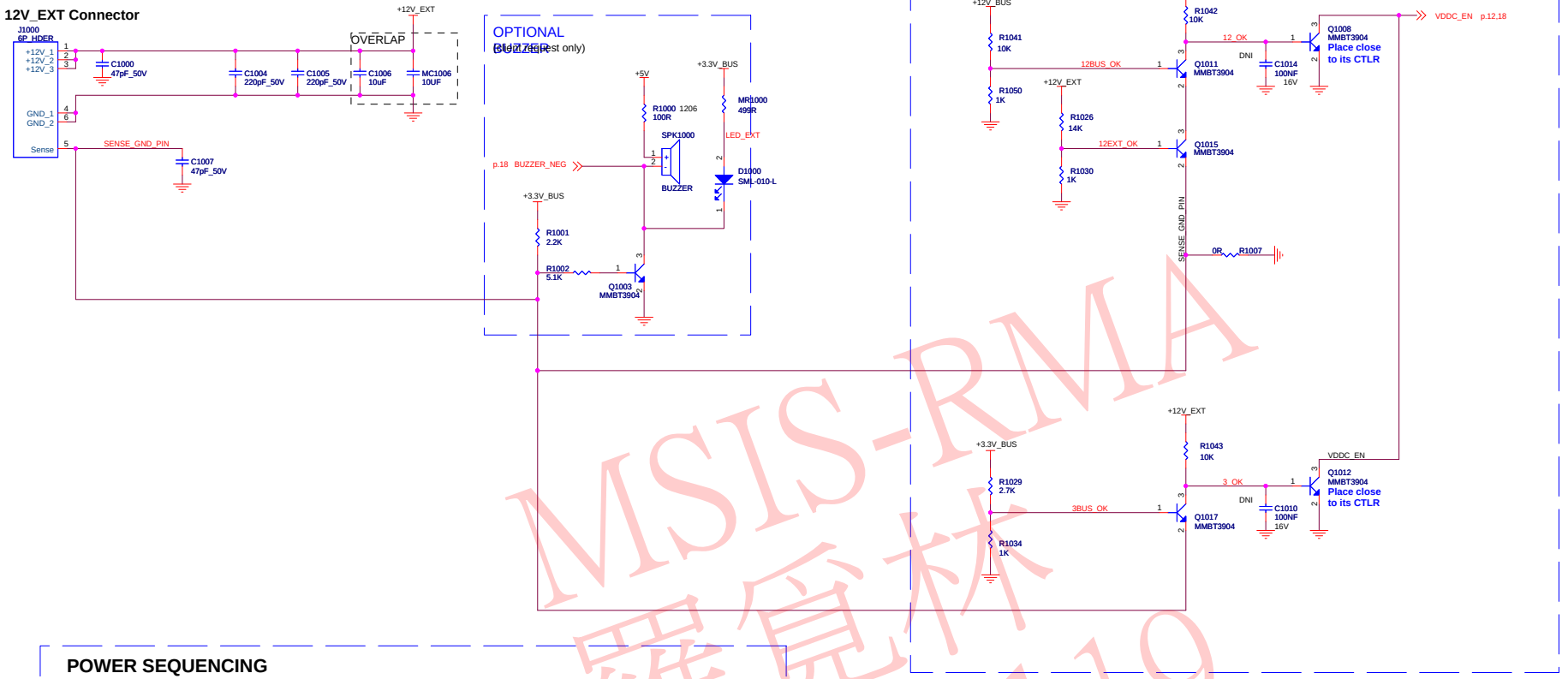
(16) Power Management - Power Gating



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(17) Power Management 2

NOTE: Use ML623 with Fansink P/N 7120084000G

+12V_BUS

L804 Chock 1.2u L04-33B7060-T15

C690 100uF_16V TH 6x7mm

R674 0R 1206

R670 0R 1206

DAUL FOOTPRINT OVERLAP

TH Toroid

+12VBUS_SOURCE

(VDDCI SOURCE)
(VDDC PHASE 1 SOURCE)

+12V_EXT

L805 Chock 1.2u L04-33B7060-T15

C695 100uF_16V TH 6x7mm

R675 0R 1206

R676 0R 1206

DAUL FOOTPRINT OVERLAP

TH Toroid

+MVDDQ_S

(MVDD SOURCE)

L625 0.47uH_7A

R680 0R

R687 0R

DAUL FOOTPRINT OVERLAP

+12VEXT_SOURCE

(VDDC PHASE 2 SOURCE)
(VDDC PHASE 3 SOURCE)

C691 100uF_16V

IF MVDD IS 5A, MAX 1.4% DROP THROUGH R-PAKS.
MAX CURRENT LIMIT FOR EACH RESISTOR IN THE PAK IS 1A;

MODE Pin Detection Circuit

MVDDQ_FB p.14

Rb RFB2 R710 7.15K 402 1%

+3.3V_BUS

R686 10K

R685 10K

p.12 MODE

MODE

+VDDC

C1216 1uF_6.3V

C1219 1uF_6.3V

C1225 1uF_6.3V

VDDC Setting

Analog Reference (Refer R to AGND)
Close to U601
Be careful when changing R655 value (VDDC IREF)

SET DEFAULT VOLTAGE POWER-ON TABLE

p.12 R1
p.12 R2
p.12 R3

10K R610 R1
10K R620 R2
10K R630 R3

p.12 VREF_R1R2R3

R608 10K C608 1uF_6.3V
R618 10K C618 1uF_6.3V
R628 10K C628 1uF_6.3V

R1R2R3_GND p.12

For IC Source # 2: Assume VREF_R1R2R3 = 2.1V.

For IC Source # 1: Assume 100uA injection current.

VDDCI Low Side Divider

p.13 VDDCI_FB

Rb1 RFB2 R910 10.2K 402

+3.3V_BUS

p.6,18,19 GPIO_17_ThermINT R243 0R

p.6 GPIO_5 R242 0R

R241 10K

HOT_INT p.12

DNI

For Testing Only

p.12 FB

RFB2 R650 10K 402 For testing only: Need to be installed for VDDC>1.35V

p.12 FBRTN

VDDC DPM through GPIOs (PVID)

+3.3V_BUS

R677 10K R678 10K

p.12 VID1
p.12 VID0

R644 0R R645 0R

GPIO_20_PWRCNTL_1 p.6
GPIO_15_PWRCNTL_0 p.6

R679 10K R661 10K

AGND

Close to U601

VDDC I2C INTERFACE

p.12 SDA_VCC
p.12 SCL_VCC

R643 0R R639 0R

SDA p.6
SCL p.6

ALL 0R RESISTORS TO BE REMOVED FOR PRODUCTION;

+5V

R624 10K/0402

R825 10K/0402 (Not)

U802 UP6262M8_SOT23-8-RH

21 SCL

R826 0R

6262_SCL

6262_SDA

SCL OUT1 SDA OUT2 OUT3 VCCBUS_SEL GND

R11-0103012-Y01

R11-0000012-Y01

R829 0R R11-0000012-W08

SDA 21

R830 2.2R/0402

+5V

CB21 .1UF 16V 10% X5R 0402 COMMON

I34-6262A05-U330

R11-022A012-Y01

C11-1042542-S02

+VDDC

B77 220R_2A
B4009 220R_2A
B4010 220R_2A
B4006 220R_2A
B4007 220R_2A
B4008 220R_2A
B4109 220R_2A
B4110 220R_2A

+VDDCI

+12V_BUS

B4012 220R_2A
B4013 220R_2A
B4014 220R_2A
B4111 220R_2A

+12V_EXT

+12VBUS_SOURCE

B4115 220R_2A
B4116 220R_2A
B4117 220R_2A

+12VEXT_SOURCE

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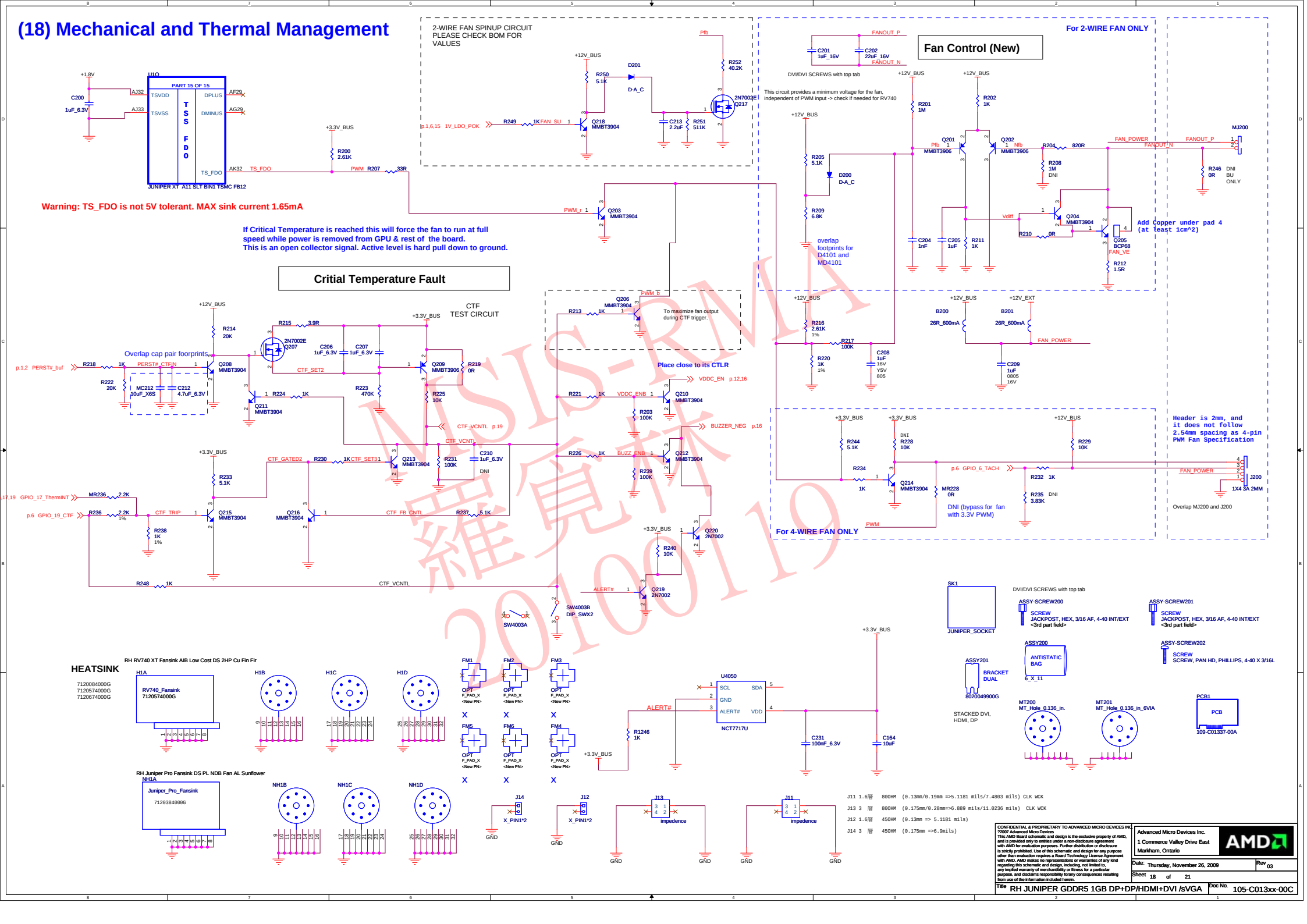
(18) Mechanical and Thermal Management



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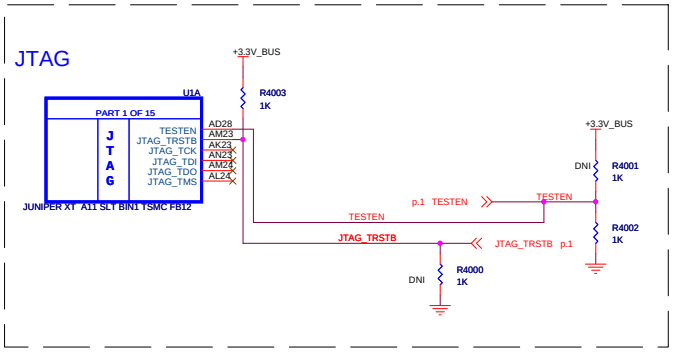
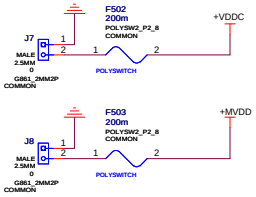
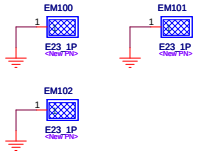
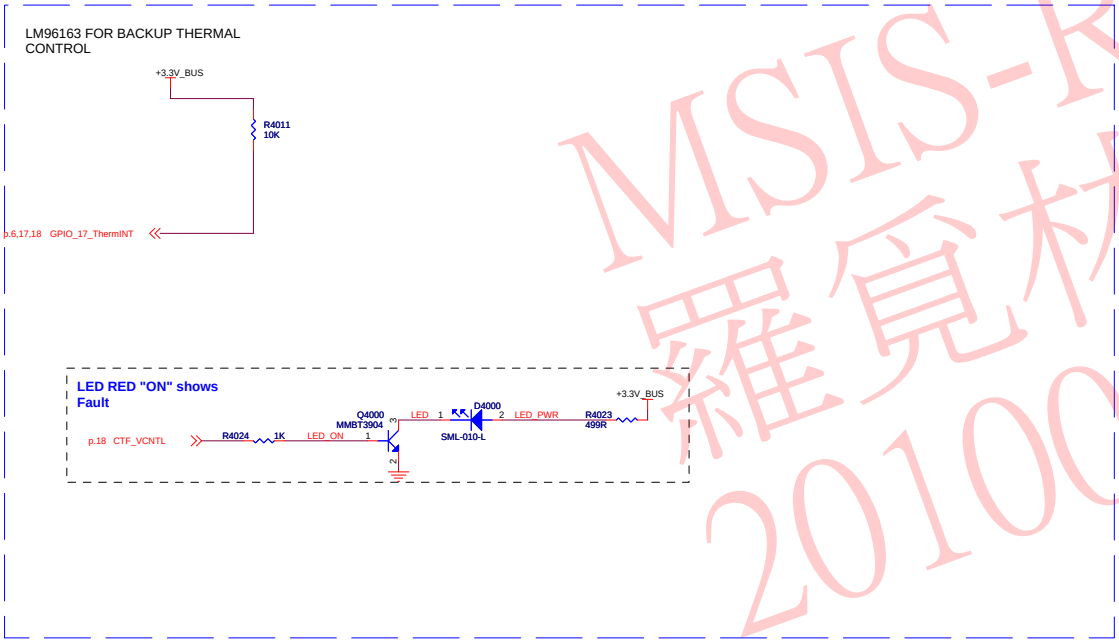
(19) Debug Circuits









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Date:	Thursday, November 26, 2009
Rev	1
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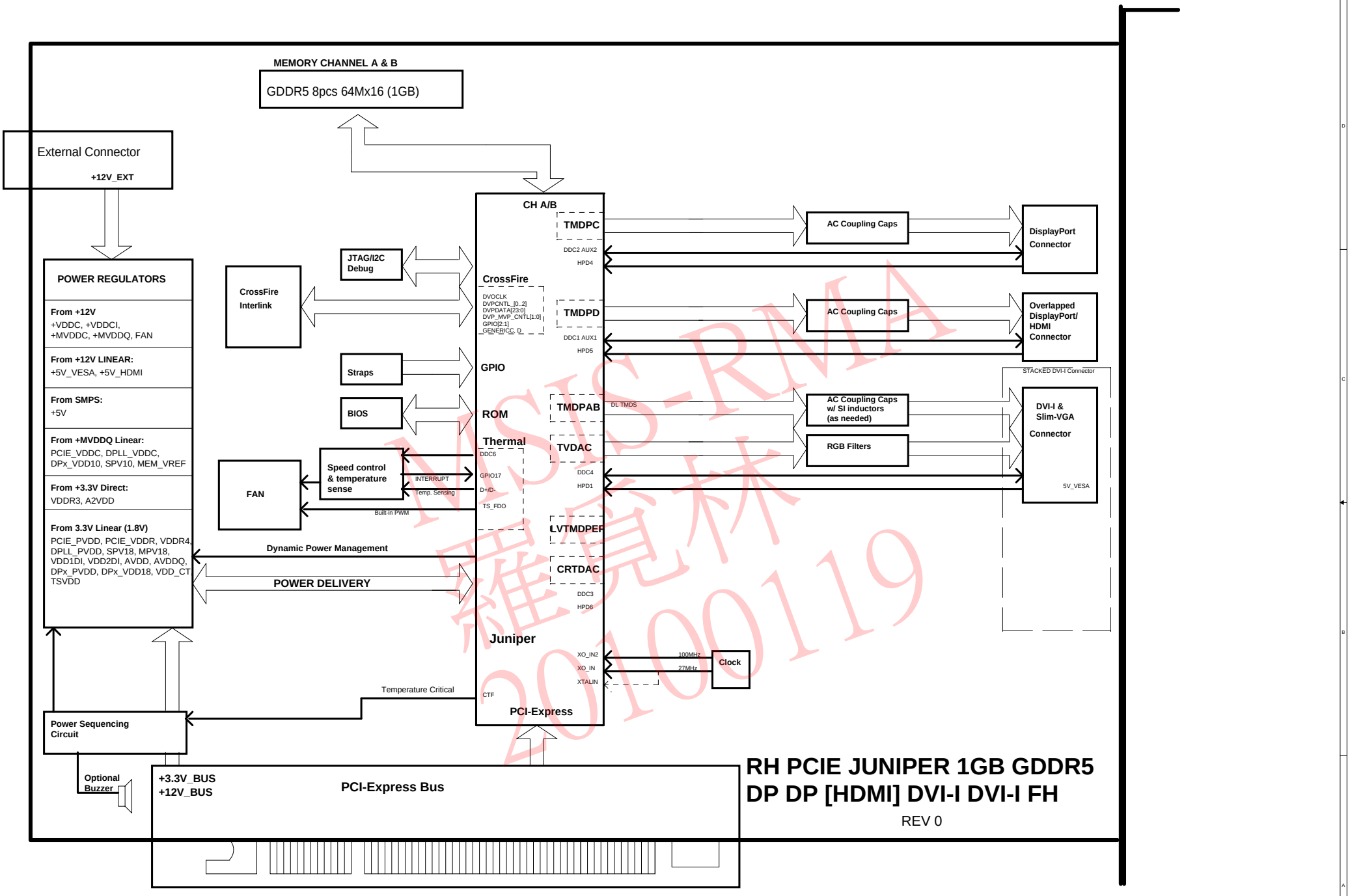
Title	RH JUNIPER GDDR5 1GB DP+DP/HDMI+DVI /sVGA
Doc No.	105-C013xx-00C



RH PCIE JUNIPER 1GB GDDR5
DP DP [HDMI] DVI-I DVI-I FH

REV 0

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Title	Schematic No.	Date:
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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/07/14	JUNIPER GDDR5 1GB - BASED ON C010; VDDC/VDDCI/MVDD SMPS CHANGES; OTHER CIRCUITS UPDATED;
01	00B	2009/09/10	Initial Release
02	00C	2009/09/25	Initial Release