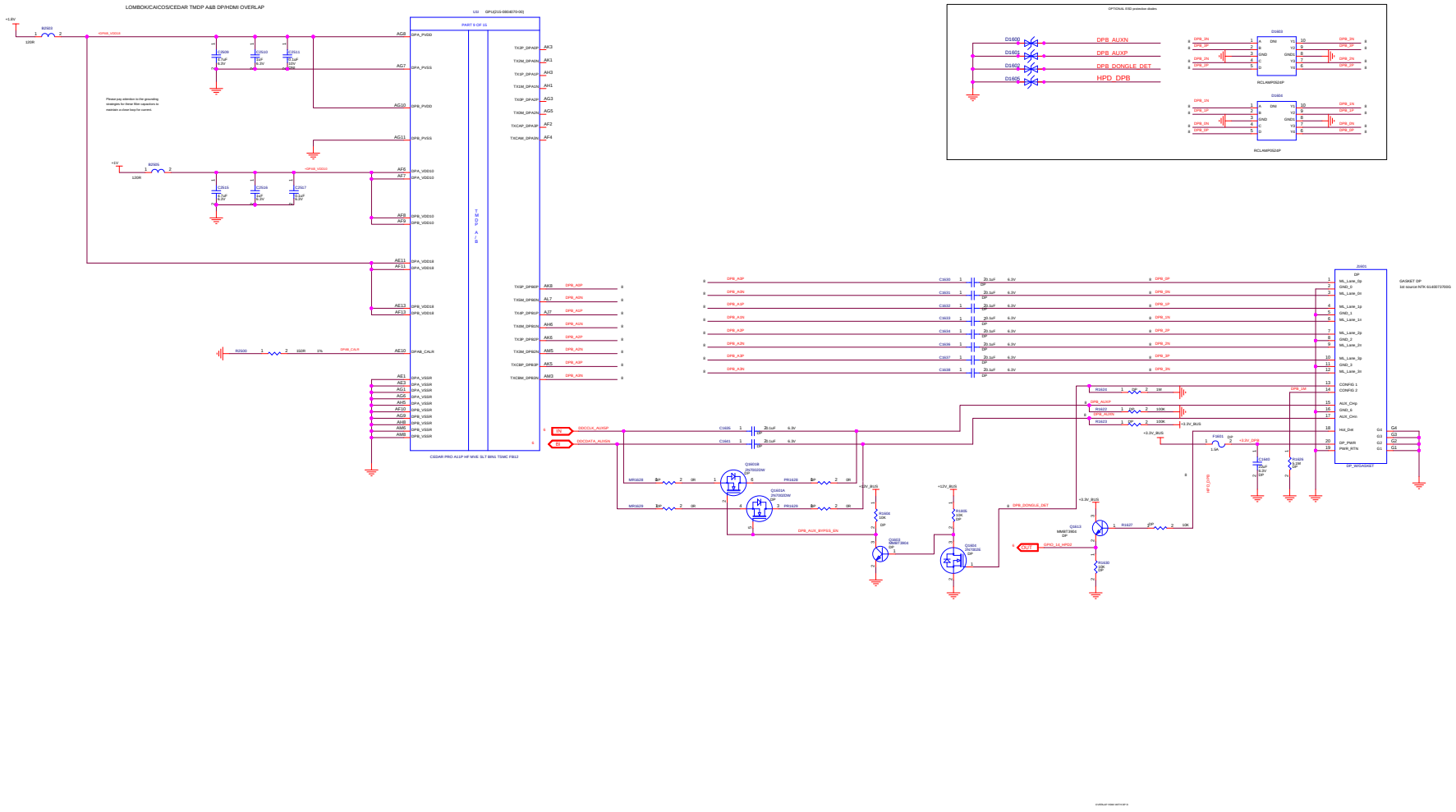
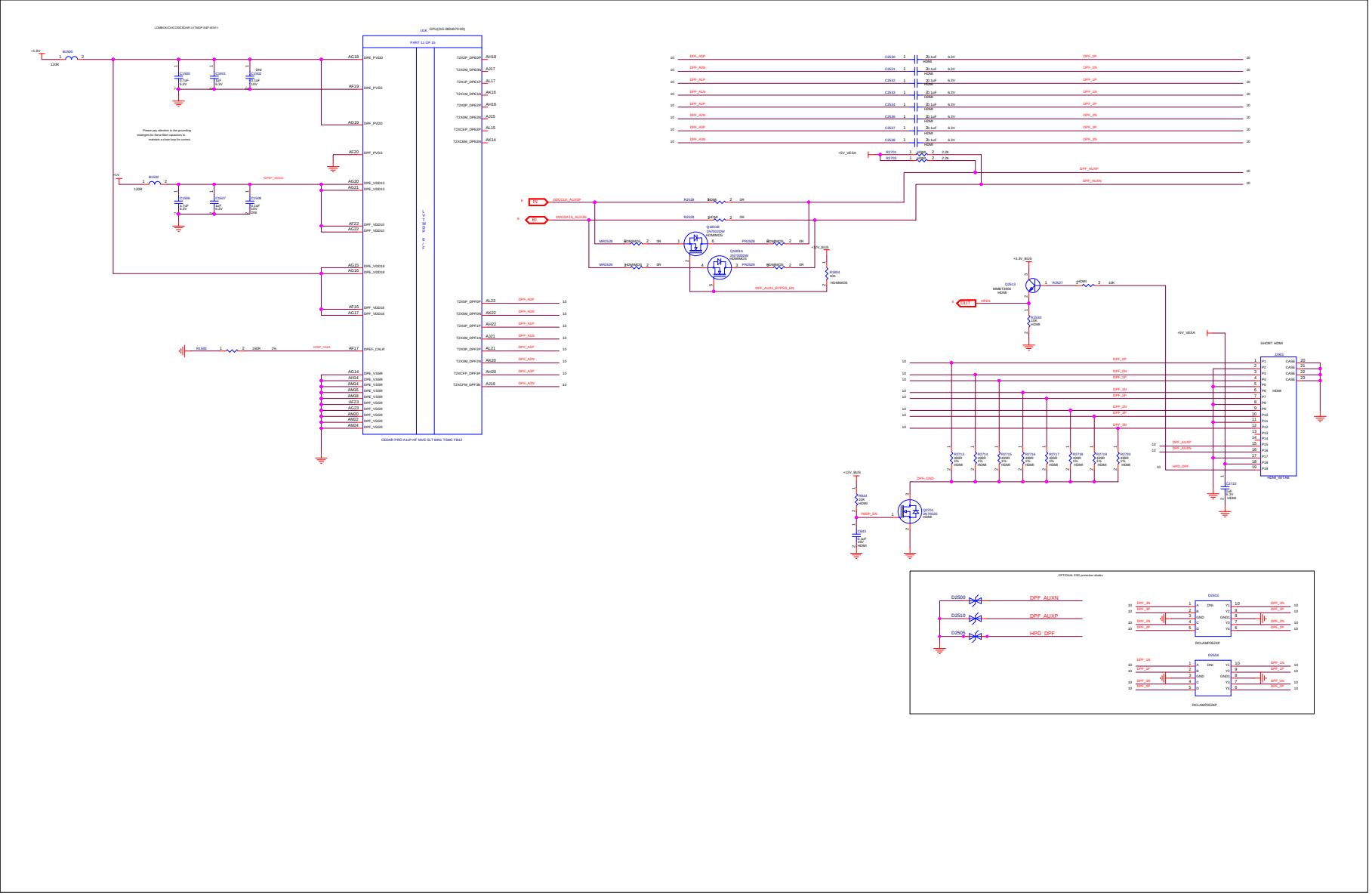

LOMBOK/CAICOS/CEDAR TMDP A&B DP/HDMI OVERLAP
U2I GPU(215-0804070-00)
PART 9 OF 15
CEDAR PRO A11P HF MVE SLT BNS TSMC FB12
DP OPTIONAL ESD protection diodes.
D1600
D1601
D1602
D1605
DPB_AUXN
DPB_AUXP
DPB_DONGLE_DET
HPD_DPB
D1603
D1604
RCLAMP0524P
J5401
DP
DP_WRGASKET
GASKET DP
1st source:NTK 614030737000S
Please pay attention to the grounding
strategies for these filter capacitors to
maintain a closed loop for current.


U2K GPU(215-0B04070-00)
PART 11 OF 16
DPE_PVDD
DPE_PVSS
DPF_PVDD
DPF_PVSS
DPE_VDD10
DPF_VDD10
DPE_VDD18
DPF_VDD18
DPF_CALR
DPE_VSSR
DPF_VSSR
T2X1P_DPE1P
T2X1N_DPE1N
T2X0P_DPE0P
T2X0N_DPE0N
T2X3P_DPF3P
T2X3M_DPF3N
T2X2P_DPF2P
T2X2M_DPF2N
T2X1P_DPF1P
T2X1M_DPF1N
T2X0P_DPF0P
T2X0M_DPF0N
T2XCFP_DPFCP
T2XCFM_DPFCN
DDC1X_AUX3P
DDC1X_AUX3N
DPF_AUX3_BYPASS_EN
+5V_VESA
+3V_BUS
+12V_BUS
SHORT HDMI
HDMI_WITHAE
OPTIONAL ESD protection diodes
D2500
D2510
D2505
DPF_AUXN
DPF_AUXP
HPD_DPF
RCLAMP0524P
RCLAMP0524P

Mechanical and Thermal Management

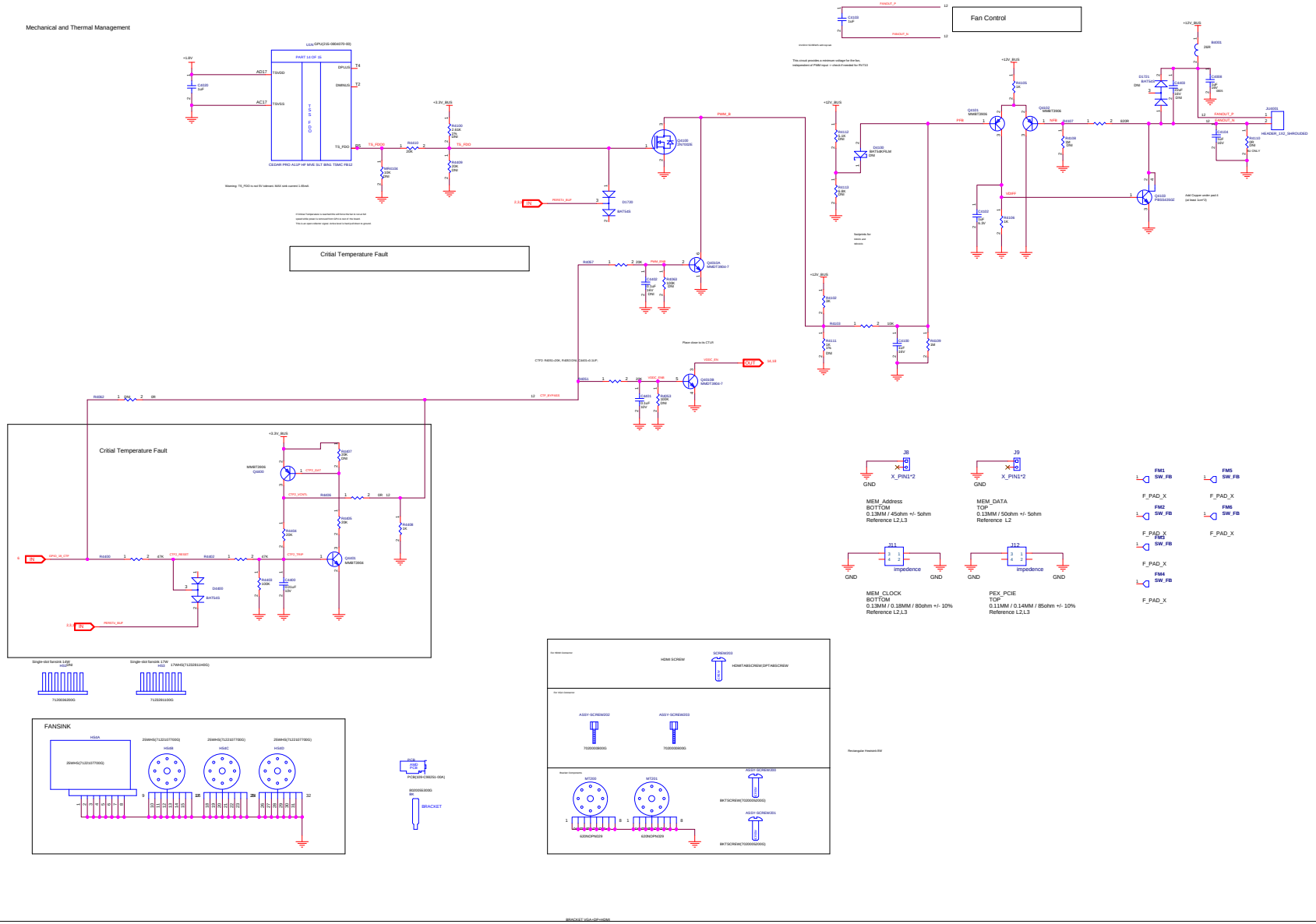


TABLE OF CONTENTS

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3	CAICOS PCIE
4	CAICOS MEM
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6	CAICOS GPIO STRAP PLL
7	CAICOS DAC
8	CAICOS TMDP AB DP
9	CAICOS TMDP C (UNUSED)
10	CAICOS LVTMDP E&F HDMI
11	CAICOS Power&GND
12	Mech/Thermal Management
13	Debug Circuit
14	PWR SEQ
15	1V
16	1.8V
17	5V
18	VDDC
19	MVDD
20	Diagram
21	REVISION HISTORY

GROUP NAME DESCRIPTION	
COMMON	INSTALLED IN MAIN BOM
NOPN	NO PN WON'T BE IN BOM
DNI	DONT INSTALL
INT	INTERNAL BOM, WON'T BE IN PRODUCTION BOM
GPU	GPU PN
BK	BRACKET
HS	HEATSINK OR FANSINK
BACO	BACO circuit
SUBBOM	SUBBOM PN
SUB BOM	
MEM	MEMORY SUB BOM
DEBUG	DEBUG SUB BOM
POWER SUB BOM	
VDDC	VDDC SUB BOM
VDDCI	VDDCI SUB BOM
MVDD	MVDD SUB BOM

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET:	TOC
DATE:	Thu Jun 04 06:11:34 2015
REV:	1.0
SHEET NUMBER:	1 OF 21
DOCUMENT NUMBER:	105-C982xx-00A
NOTES:	NOTE

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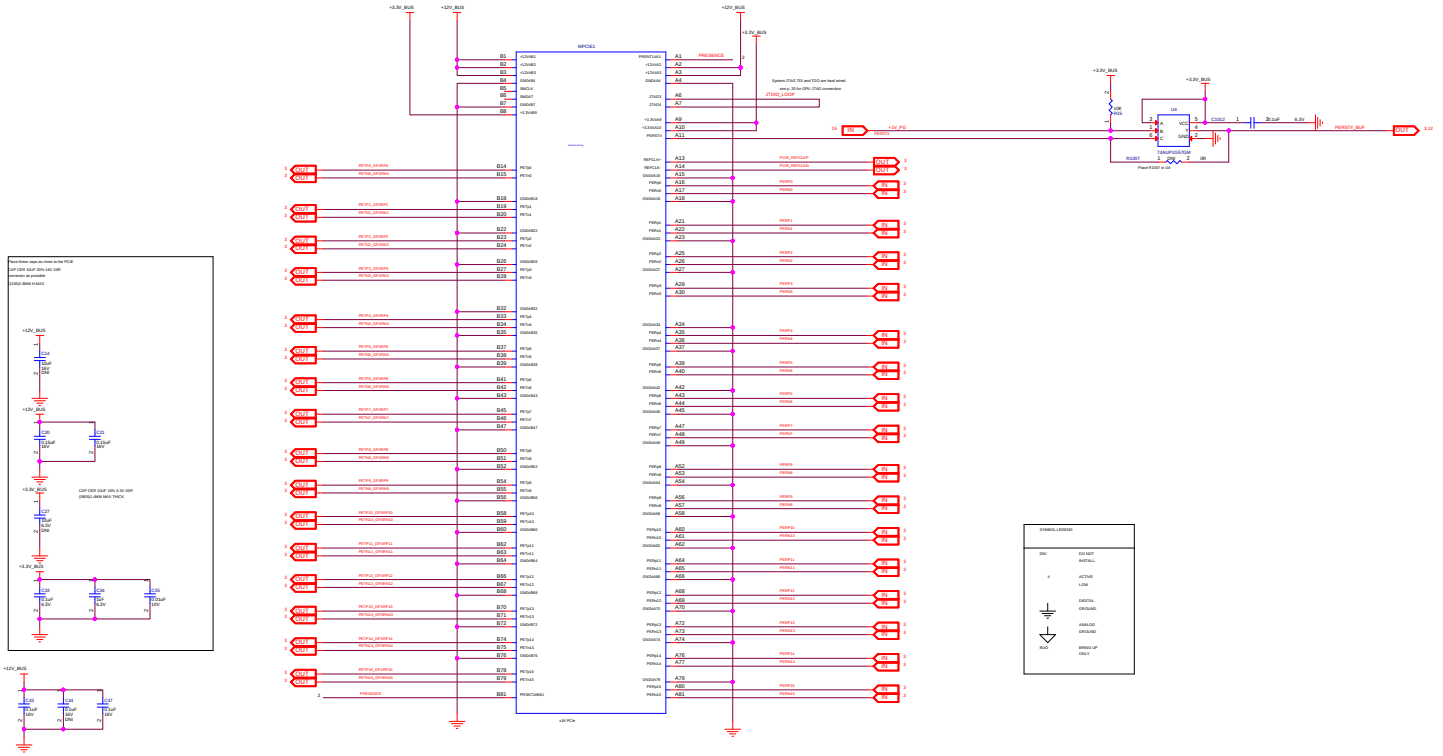
TITLE:

Calcos G5 VGA+DP+HDMI 25W ASIC, 5.7"

PCI-EXPRESS EDGE CONNECTOR



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET:	PCI-E Edge Connector
DATE:	Thu Jun 04 06:11:34 2015
REV:	1.0
SHEET NUMBER:	2 OF 21
DOCUMENT NUMBER:	105-C982xx-00A
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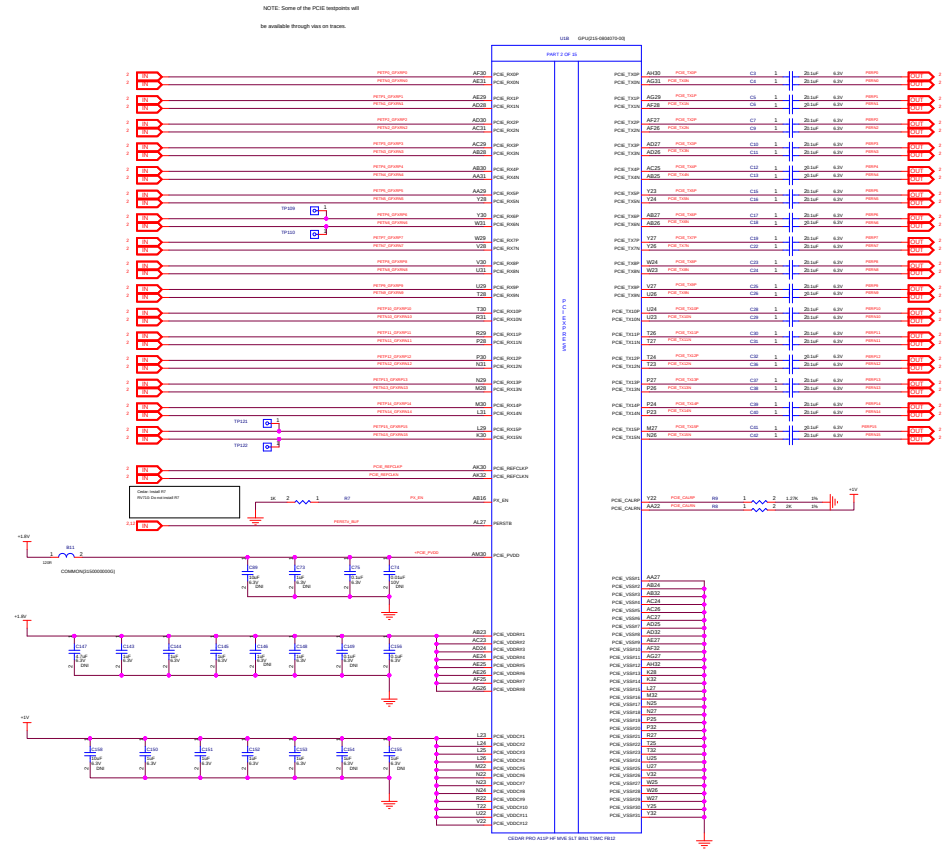
TITLE: Calcos G5 VGA+DP+HDMI 25W ASIC, 5.7"

LOMBOK/CAICOS/CEDAR PCIe Interface



AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET:	CAICOS PCIE
DATE:	Thu Jun 04 08:11:35 2015
REV:	1.0
SHEET NUMBER:	3 OF 21
DOCUMENT NUMBER:	105-C982xx-00A
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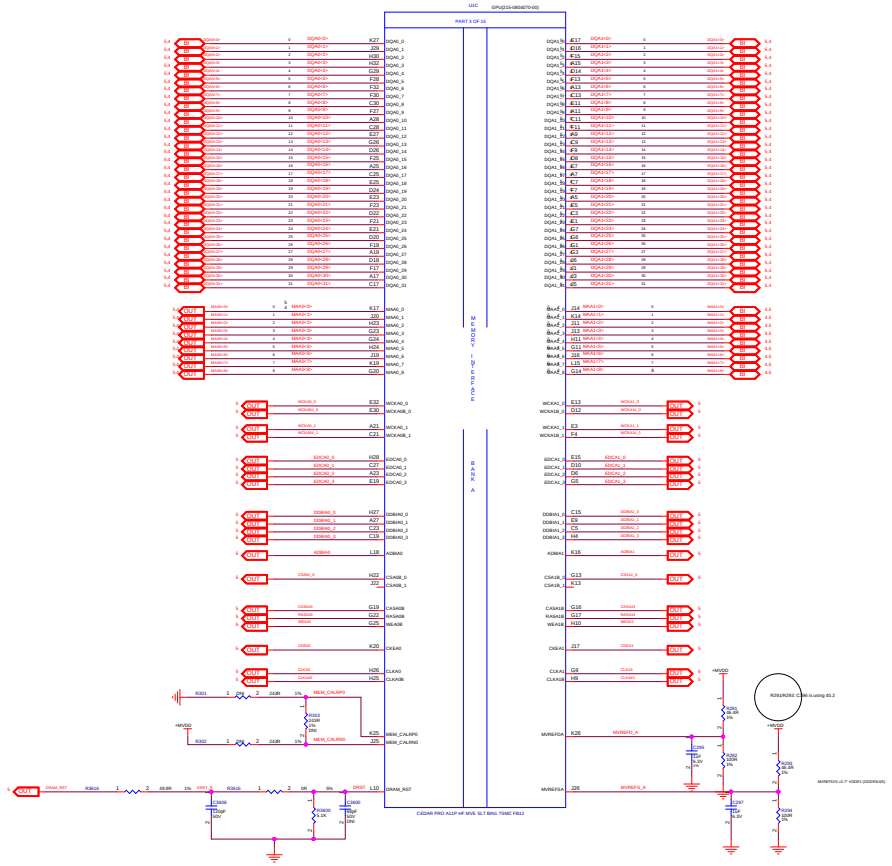
TITLE: Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: CAICOS MEM	
DATE: Thu Jun 04 08:11:35 2015	REV: 1.0
SHEET NUMBER: 4 OF 21	
DOCUMENT NUMBER: 105-C982xx-00A	
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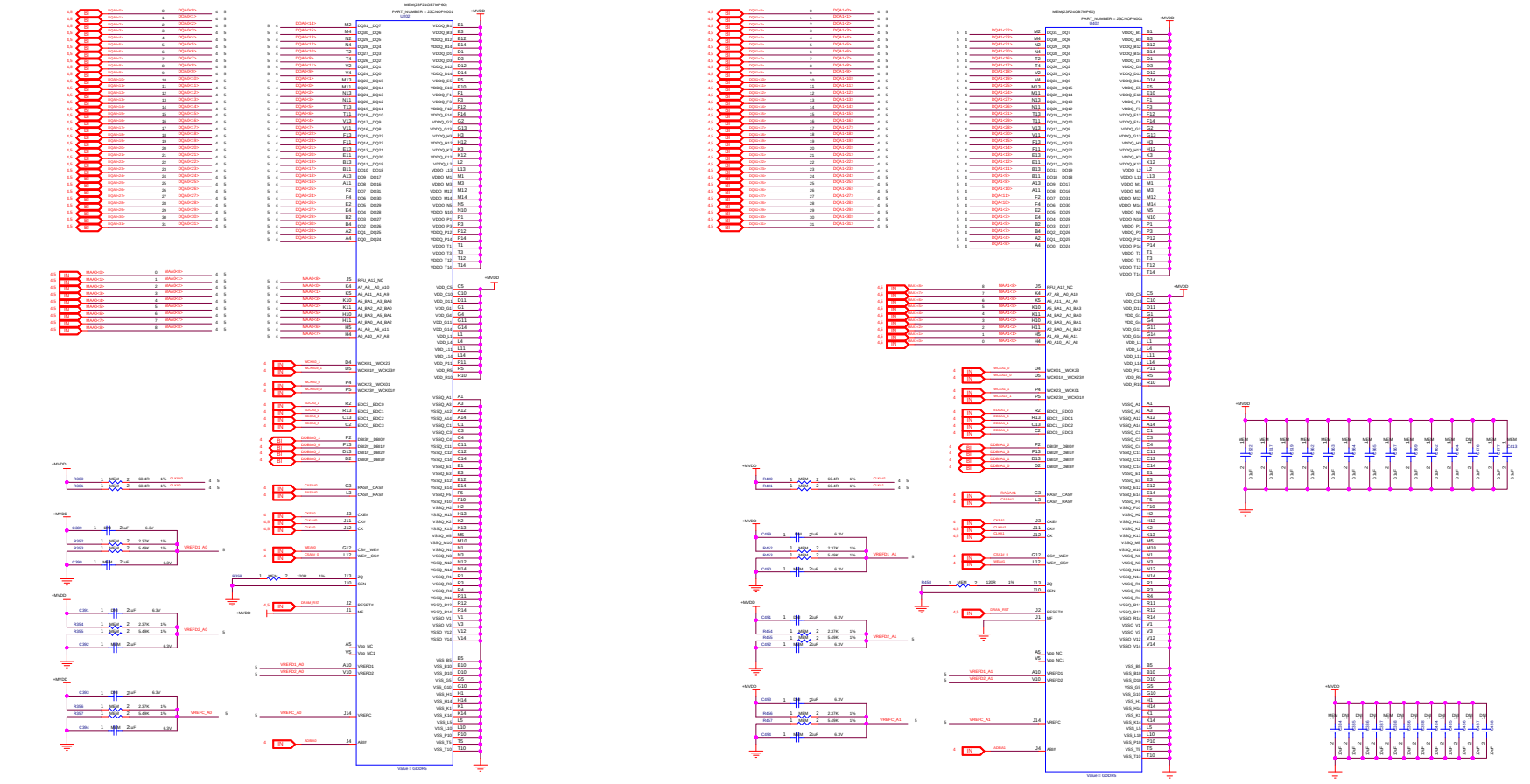
TITLE: Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"

2pcs GDDR5 x32



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: GDDR5	
DATE: Thu Jun 04 06:11:36 2015	REV: 1.0
SHEET NUMBER: 5 OF 21	
DOCUMENT NUMBER: 105-C982xx-00A	
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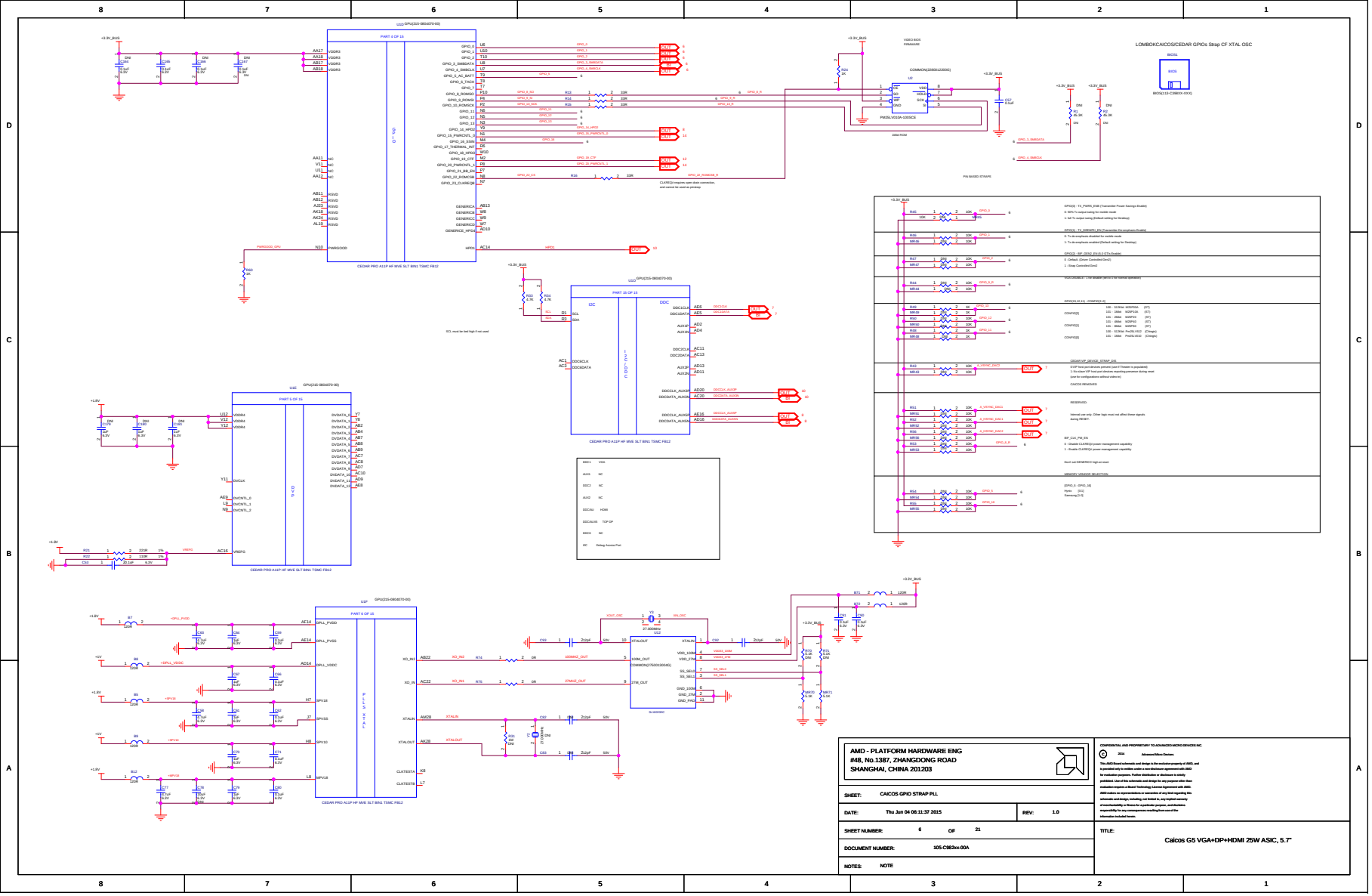
TITLE: Calcos G5 VGA+DP+HDMI 25W ASIC, 5.7"


LOMBOKCAICOS/CEDAR GPIOs Strap CF XTAL OSC
BIOS1
BIOS
MICRO-LCB-CSB8DX-XXXQ
COMMON(2350012200G)
PM25LV010A-100SCE
1Mbit ROM
VIDEO BIOS FIRMWARE
PIN BASED STRAPS
CEDAR PRO A11P HF MV6 SLT BIN1 TSMC FB12
GPU(215-0804070-00)
CLKREQ# requires open drain connection, and cannot be used as pinstrap
SCL must be tied high if not used
GPIO[2] - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 92% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)
GPIO[1] - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)
GPIO[2] - BIF_GEN2_EN,(0-1) CTI's Enable)
0 : Default, (Gen1 Controlled Gen2)
1 : Strap Controlled Gen2
GPIO[3:0],11) : CONFIG[3:0]
CONFIG[2]
CONFIG[1]
CONFIG[0]
CEDAR VIP_DEVICE_STRAP_EN
0:VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices requesting presence during reset
(use for configurations without video in)
CAICOS REMOVED
RESERVED
Internal use only. Other logic must not affect these signals during RESET.
BIF_CLK_PM_EN
0 : Disable CLKREQ# power management capability
1 : Enable CLKREQ# power management capability
Don't set GENERIC2 high at reset
MEMORY VENDOR SELECTION
[GPIO_3 : GPIO_10]
Hynix [D1]
Samsung [1-0]
AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203
SHEET: CAICOS GPIO STRAP PLL
DATE: Thu Jun 04 06:11:37 2015
REV: 1.0
SHEET NUMBER: 6 OF 21
DOCUMENT NUMBER: 105-C982xx-00A
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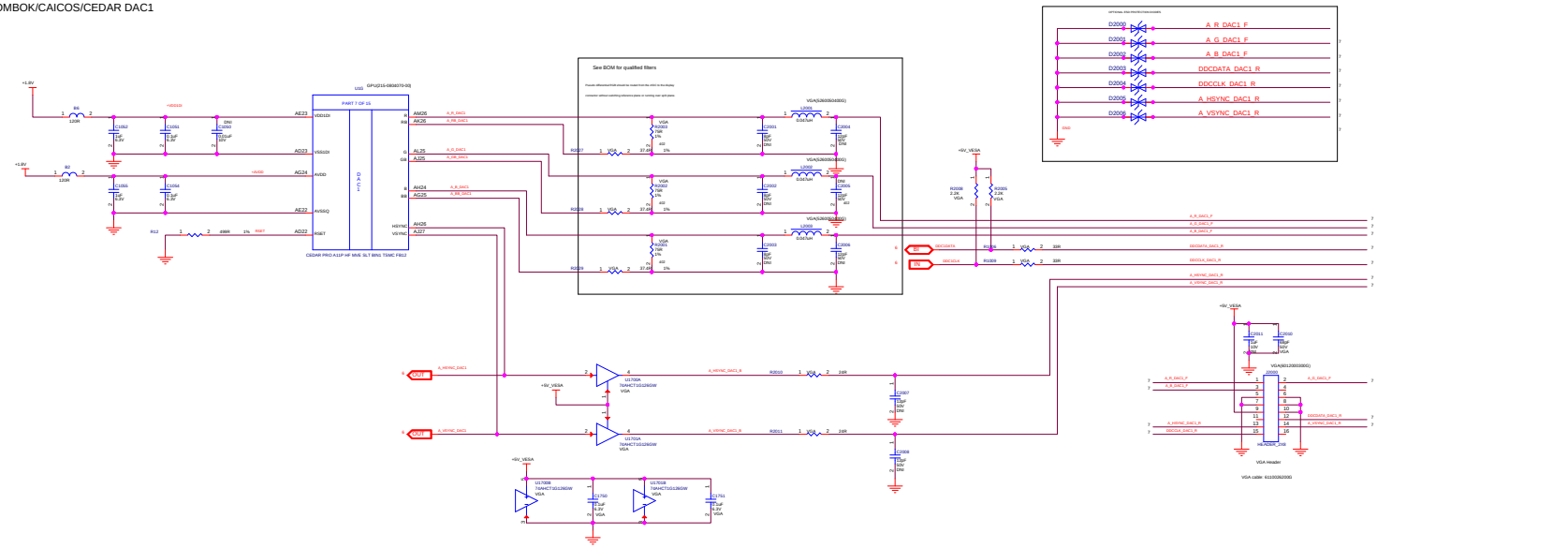
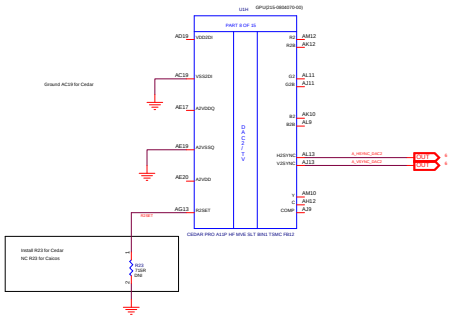
TITLE: Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"

LOMBOK/CAICOS/CEDAR DAC1





AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: CAICOS DAC	
DATE: Thu Jun 04 06:11:37 2015	REV: 1.0
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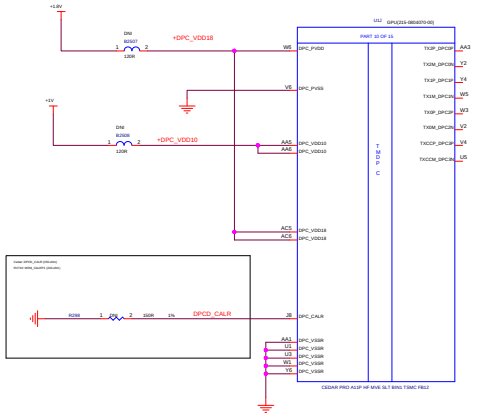
TITLE: Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"

LOMBOK/CAICOS/CEDAR Display Port C (Unused)



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: CAICOS TMDP C (UNUSED)	
DATE: Thu May 28 03:09:00 2015	REV: 1.0
SHEET NUMBER: 9 OF 21	
DOCUMENT NUMBER: 105-C982xx-00A	

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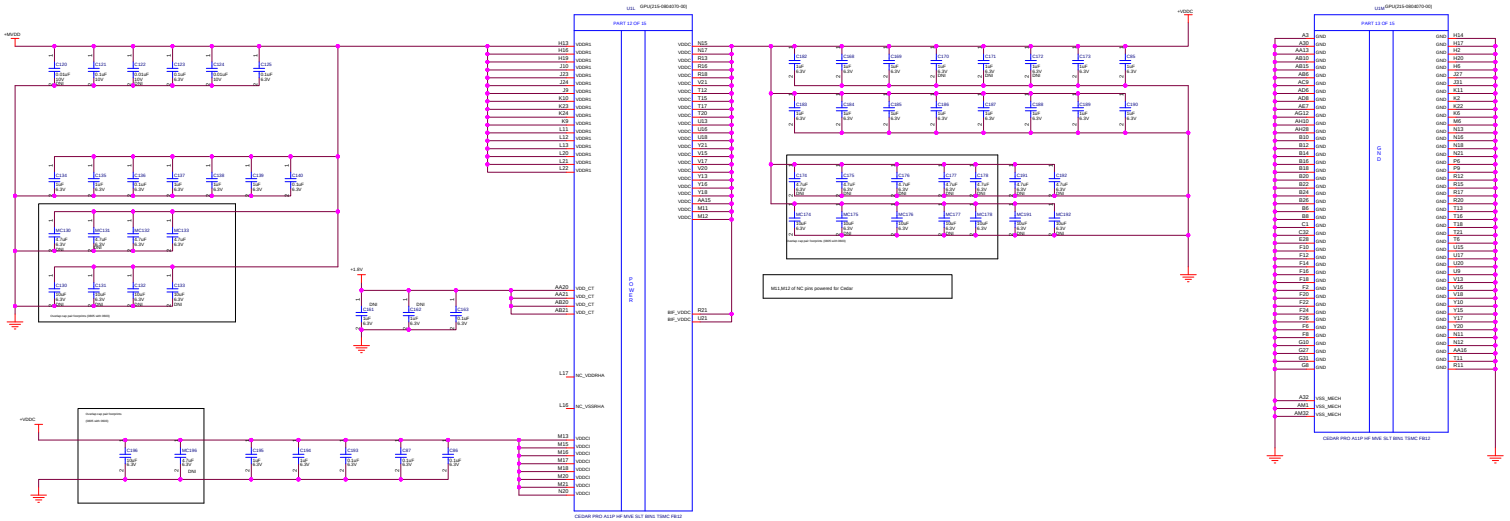
TITLE: Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"

LOMBOK/CAICOS/CEDAR Power & GND



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: CAICOS Power&GND	
DATE: Thu May 28 03:09:00 2015	REV: 1.0
SHEET NUMBER: 11 OF 21	
DOCUMENT NUMBER: 105-C982xx-00A	

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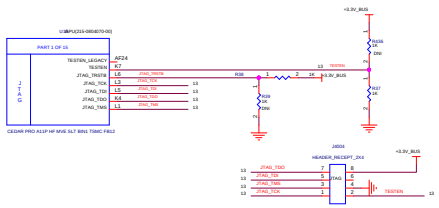
TITLE: Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"

(19) Debug Circuits



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: Debug Circuit	
DATE: Thu May 28 03:09:00 2015	REV: 1.0
SHEET NUMBER: 13 OF 21	
DOCUMENT NUMBER: 105-C982xx-00A	

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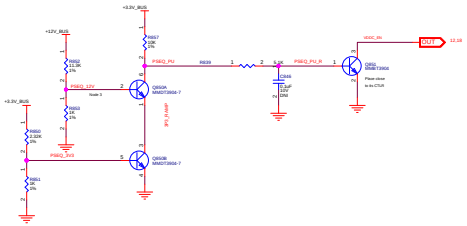
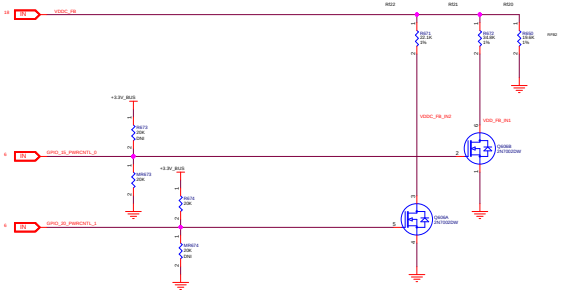
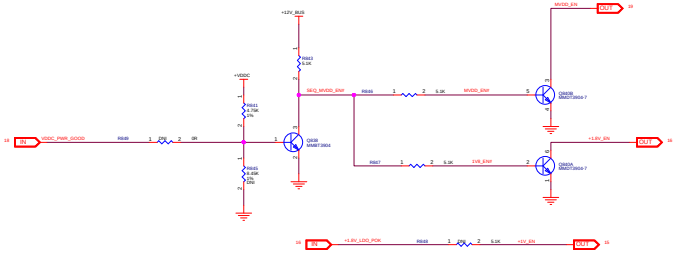
TITLE:

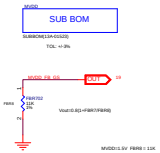
Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"

Power Management - Power Gating and Dynamic Voltage Control









MEM

SUB BOM

SUBBOM(13B-00920)

256Mx16 1.5V 1GHz
HYNIX(13B-00827) SAMSUNG(13B-00828)

VDDC

SUB BOM

SUBBOM(13A-01522)

TOL: +/-3%

MVDD

SUB BOM

SUBBOM(13A-01523)

TOL: +/-3%

AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: PWR SEQ	
DATE: Thu May 28 03:08:58 2015	REV: 1.0
SHEET NUMBER: 14 OF 21	
DOCUMENT NUMBER: 105-C982xx-00A	

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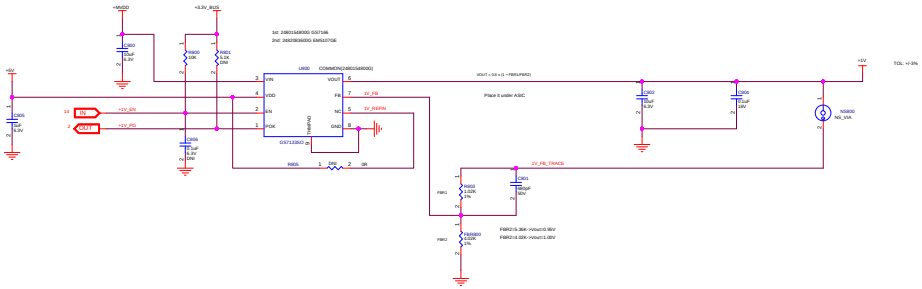
TITLE:

Calcos G5 VGA+DP+HDMI 25W ASIC, 5.7"

Linear Regulators

LDO #1: Vin = +1.5V +/-2% Vout = 1V +/- 2%; Iout = 3A MAX

PCB: 50 to 70mm sq. copper area for cooling



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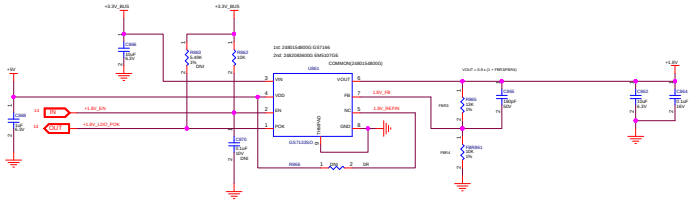
SHEET: 1V	
DATE: Thu Jun 04 08:11:37 2015 REV: 1.0	
SHEET NUMBER: 15 OF 21	TITLE: Calcos G5 VGA+DP+HDMI 25W ASIC, 5.7"
DOCUMENT NUMBER: 105-C982xx-00A	
NOTES: NOTE	

Linear Regulators

LDO #2: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1A MAX

PCB: 50 to 70mm sq. copper area for cooling



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: 1.8V	
DATE: Thu May 28 03:08:59 2015	REV: 1.0
SHEET NUMBER: 16 OF 21	
DOCUMENT NUMBER: 105-C982xx-00A	

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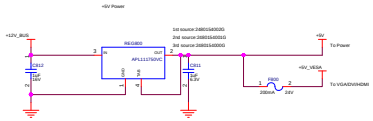
TITLE: Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: 5V	
DATE: Thu Jun 04 06:11:37 2015	REV: 1.0
SHEET NUMBER: 17 OF 21	
DOCUMENT NUMBER: 105-C982xx-00A	
NOTES: NOTE	

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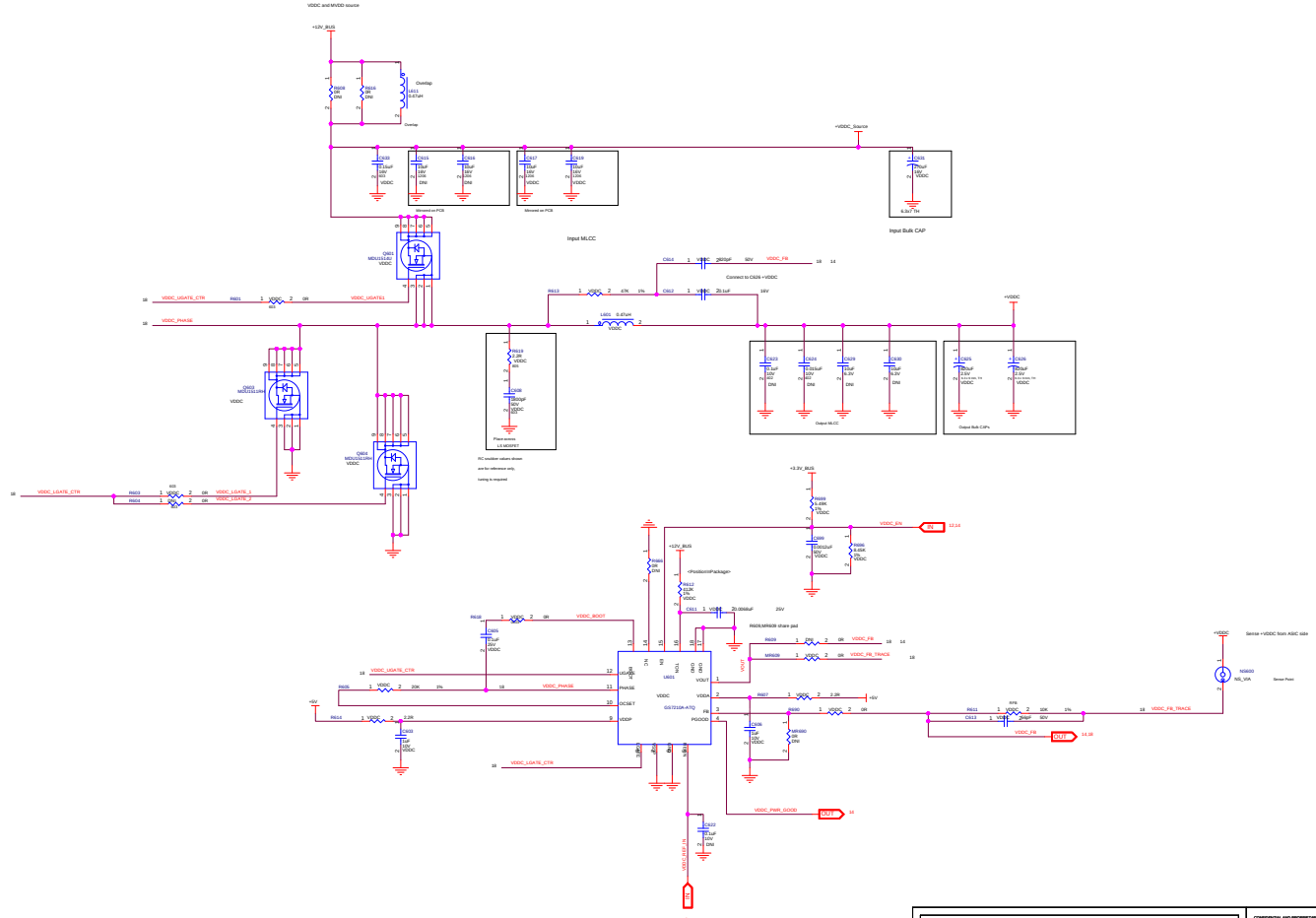
TITLE: Calcos G5 VGA+DP+HDMI 25W ASIC, 5.7"



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: VDDC	
DATE: Thu May 28 03:08:57 2015	REV: 1.0
SHEET NUMBER: 18 OF 21	
DOCUMENT NUMBER: 105-C982xx-00A	

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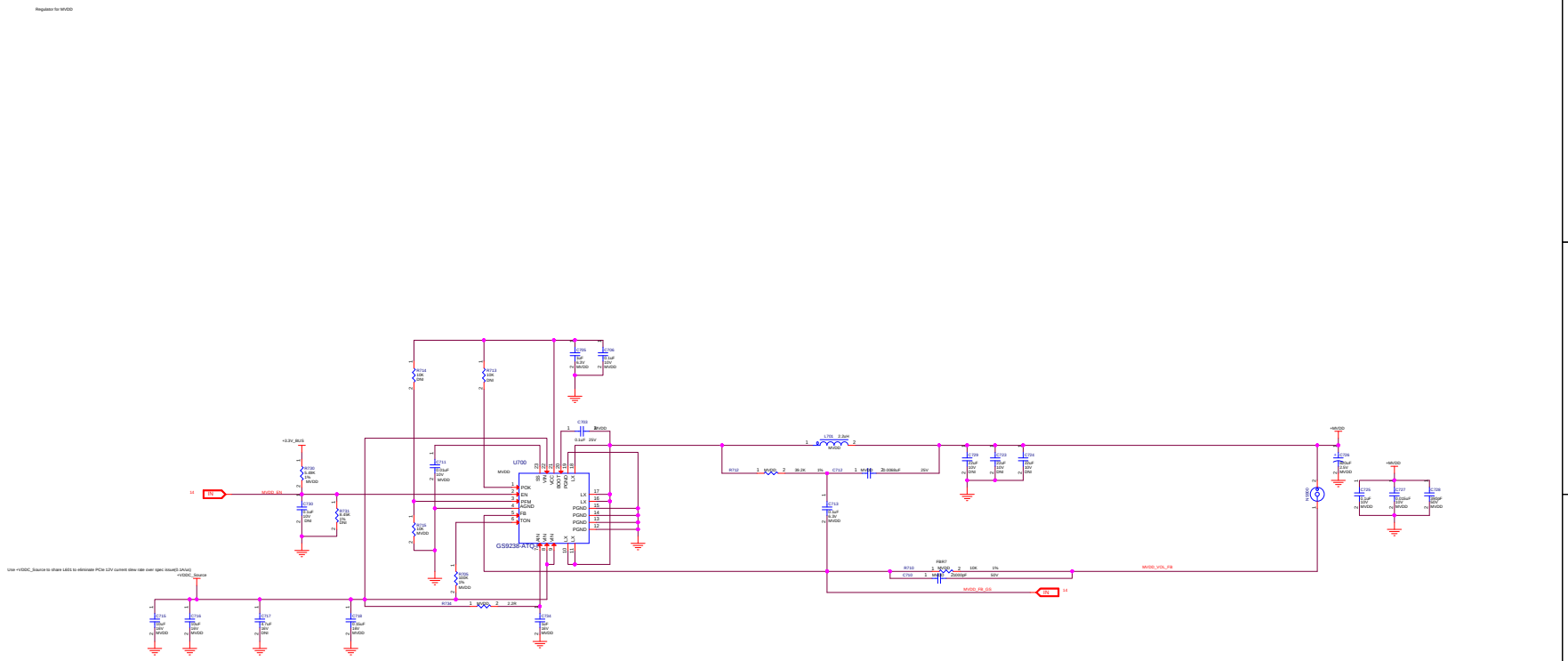
TITLE: Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: MVDD	
DATE: Thu May 28 03:08:58 2015	REV: 1.0
SHEET NUMBER: 19 19 OF 21 21	
DOCUMENT NUMBER: 105-C982xx-00A	

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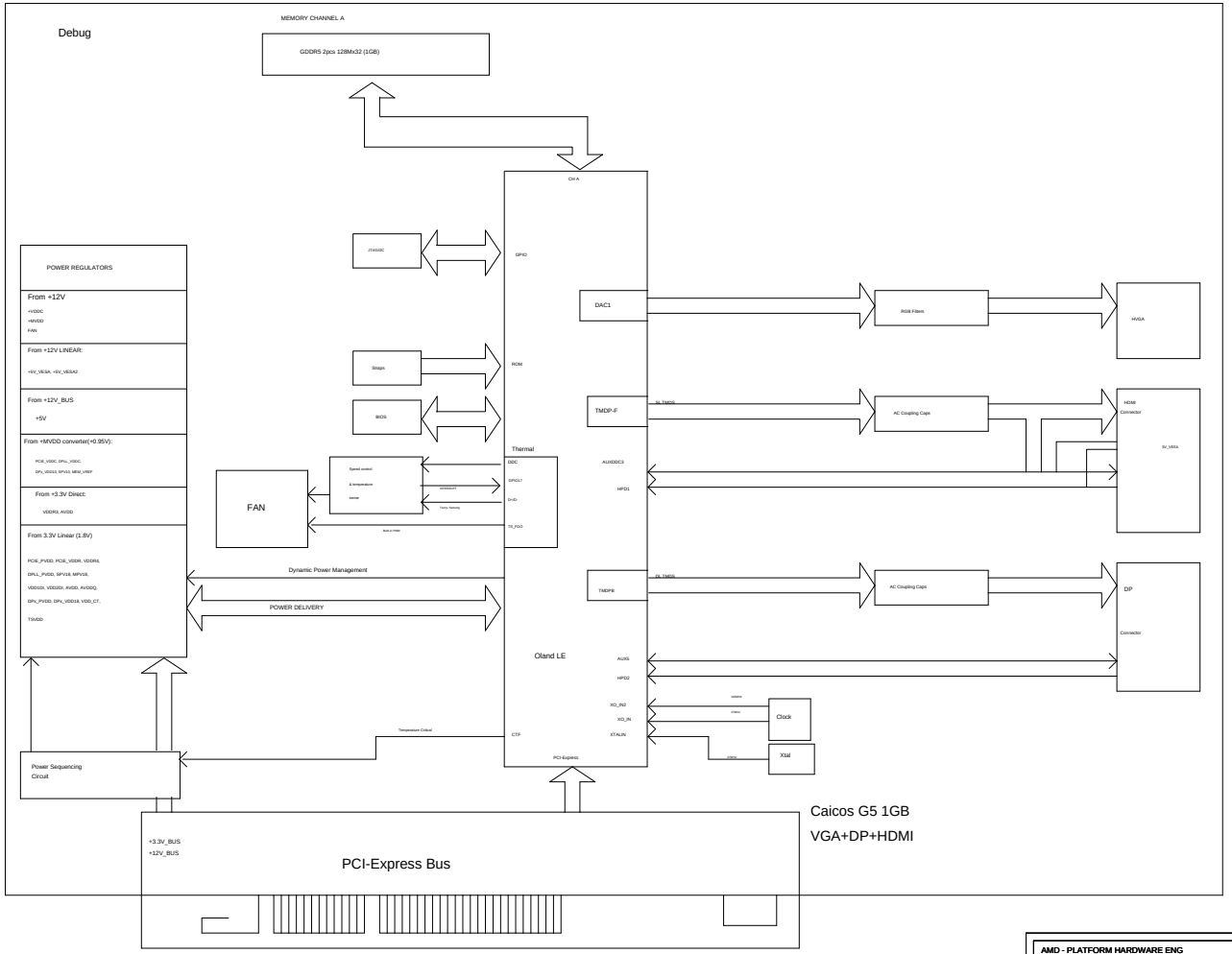
TITLE: Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: Diagram	
DATE: Thu May 21 06:47:46 2015	REV: 1.0
SHEET NUMBER: 20 OF 21	
DOCUMENT NUMBER: 105-C982xx-00A	

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TITLE: Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"

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TITLE: Caicos G5 VGA+DP+HDMI 25W ASIC, 5.7"

DOCUMENT NUMBER: 105-C982xx-00A

DATE: Thu May 28 02:44:26 2015

SHEET NUMBER: 21 OF 21

REV: 1.0

REVISION HISTORY

ENGINEER: Tony Yang

NOTES: NOTE

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SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
1.00	00A	05/26/15	1. Initial release