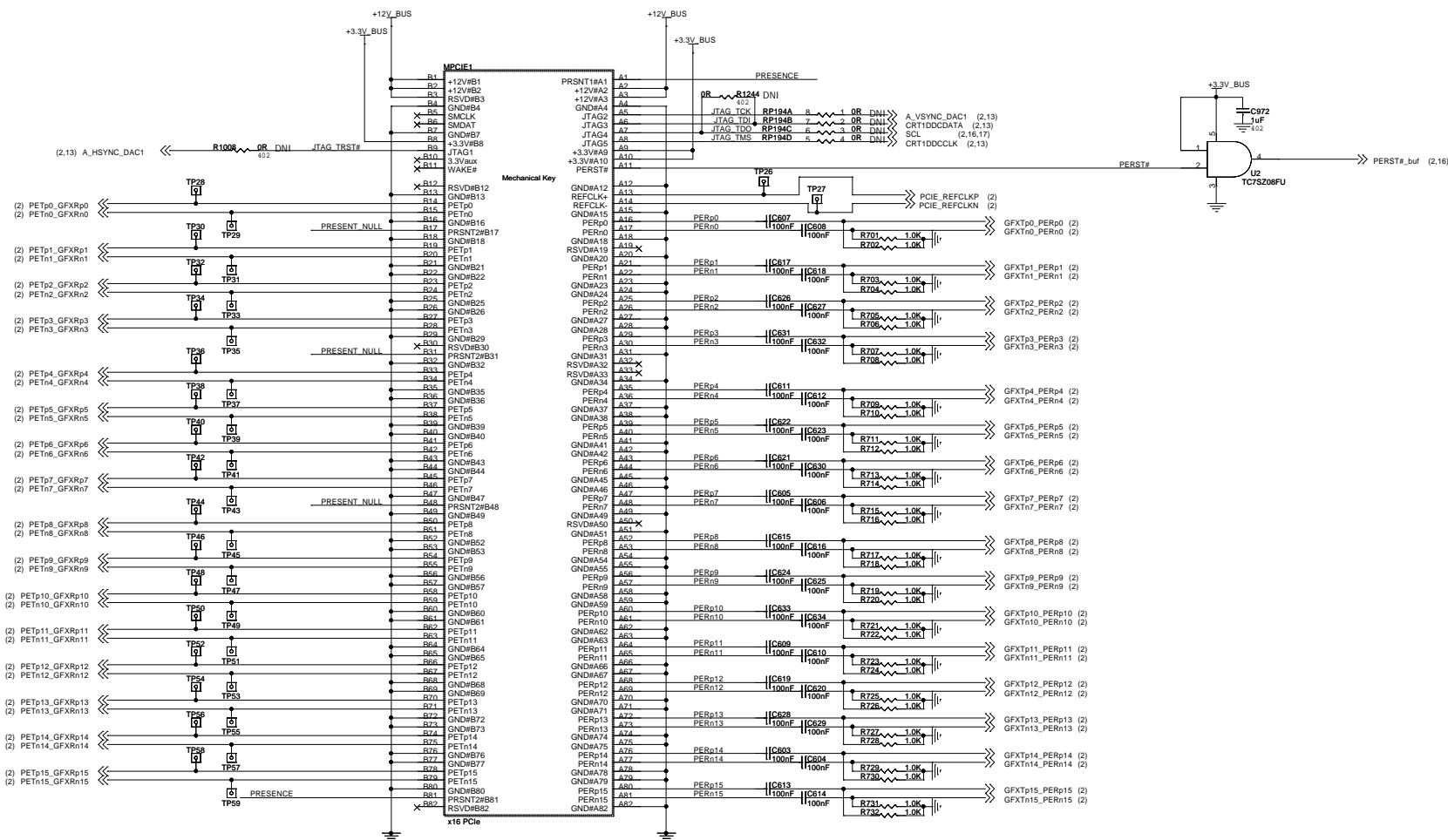
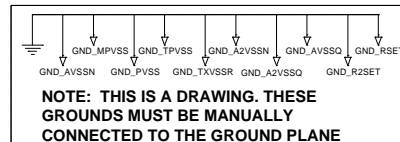


Place these capacitors close to the PCIe connector

PCI-EXPRESS EDGE CONNECTOR

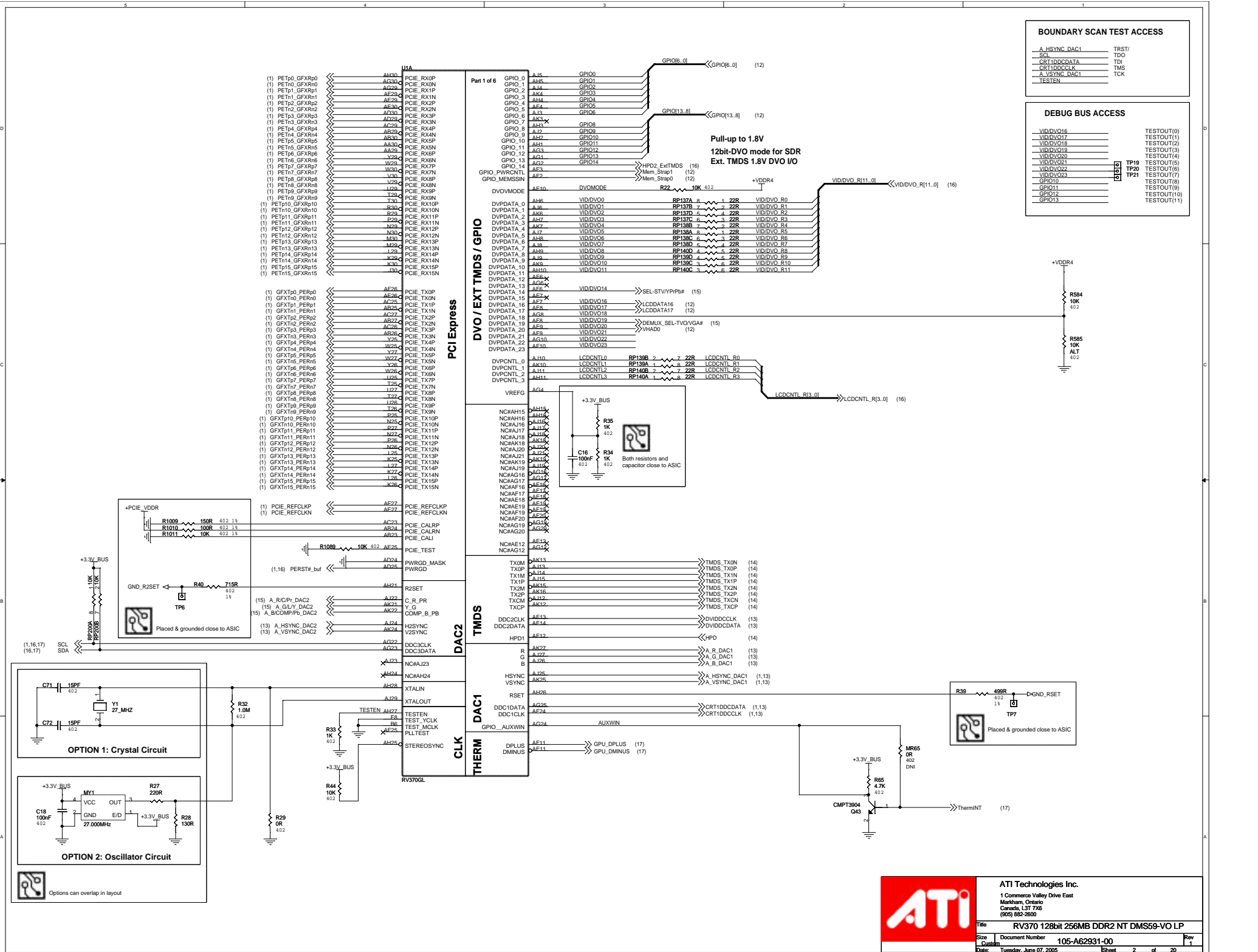


SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND



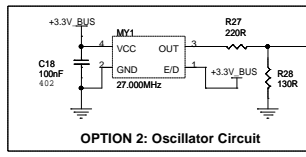
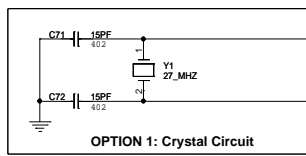
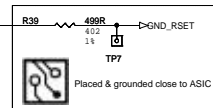
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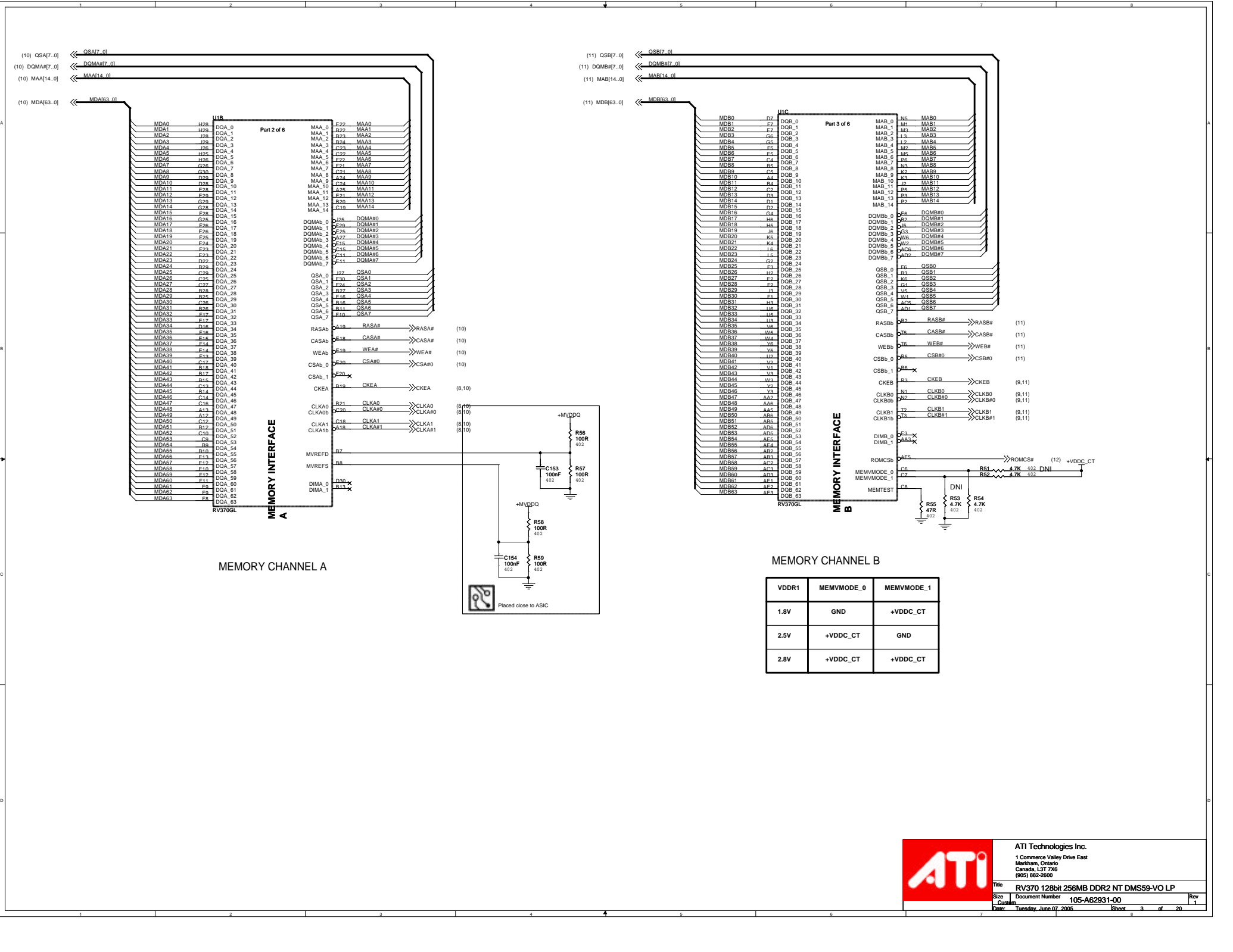
Title	RV370 128bit 256MB DDR2 NT MS59-VO LP		
Size	Document Number	105-A62931-00	Rev 1
Date	Tuesday, June 07, 2005	Sheet 1	of 20



BOUNDARY SCAN TEST ACCESS			
A_HSYNC_DAC1	TRST/		
SCL	TDO		
CRT1DDCLK	TDI		
A_VSYNC_DAC1	TMS		
TESTEN	TCK		

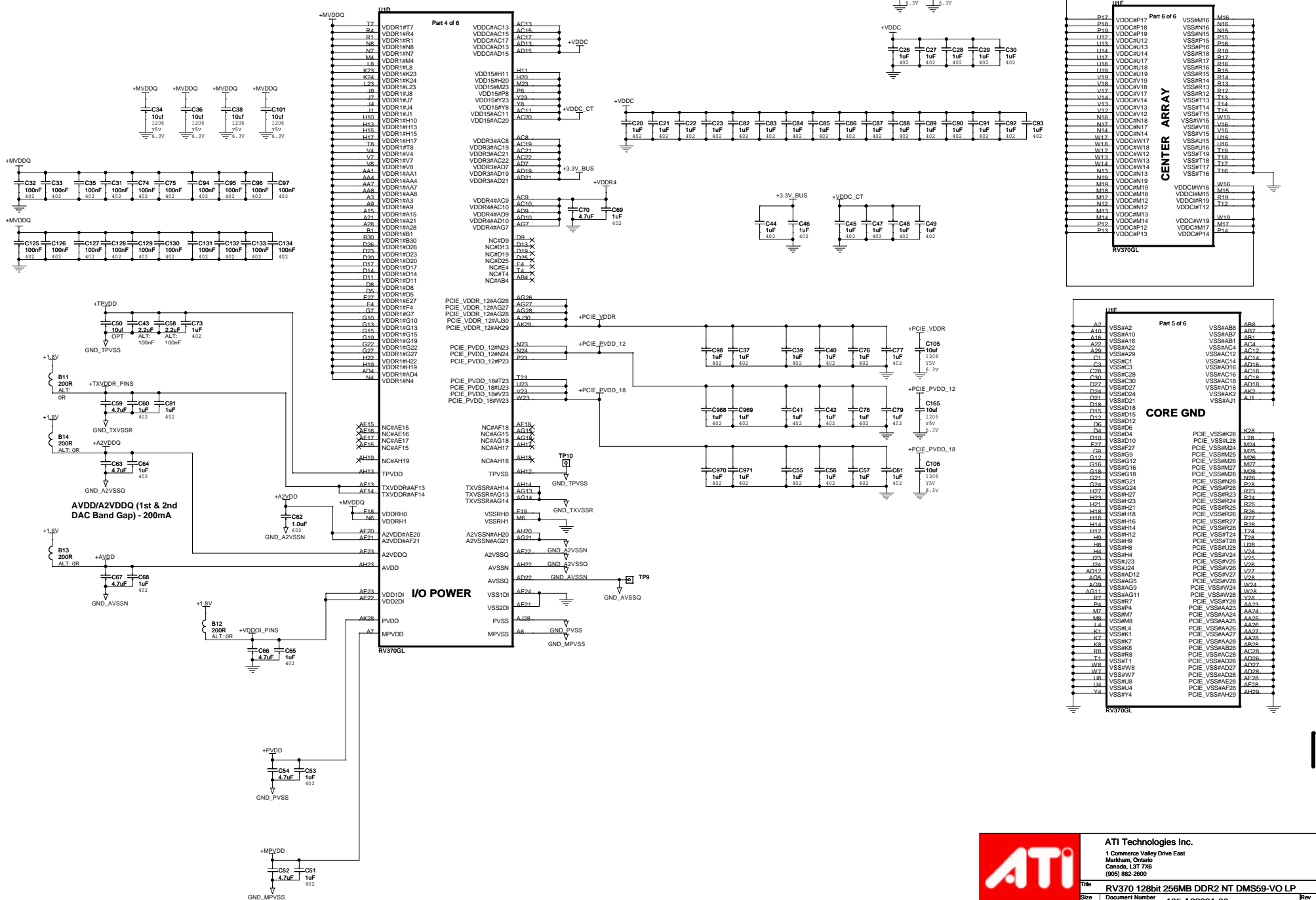
DEBUG BUS ACCESS			
VIDDV016	TESTOUT(0)		
VIDDV017	TESTOUT(1)		
VIDDV018	TESTOUT(2)		
VIDDV019	TESTOUT(3)		
VIDDV020	TESTOUT(4)		
VIDDV021	TESTOUT(5)		
VIDDV022	TESTOUT(6)		
VIDDV023	TESTOUT(7)		
GPIO10	TESTOUT(8)		
GPIO11	TESTOUT(9)		
GPIO12	TESTOUT(10)		
GPIO13	TESTOUT(11)		





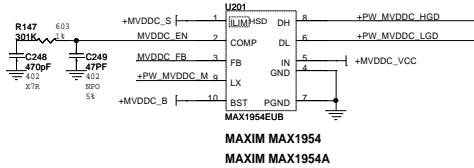
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Title: RV370 128bit 256MB DDR2 NT DMS59-VO LP
Size: 105-A62931-00
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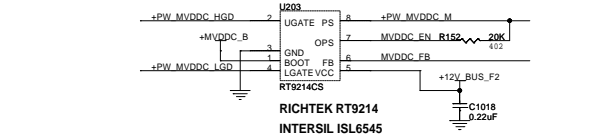
Size	Document Number	105-A62931-00	Rev	1
Custom				
Date:	Tuesday, June 07, 2005	Sheet	5	of 20

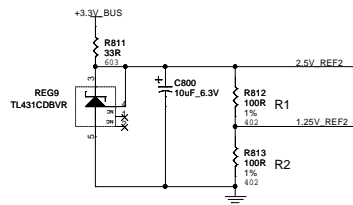
MVDDC-PWM1



MAXIM MAX1954
MAXIM MAX1954A

MVDDC-PWM2



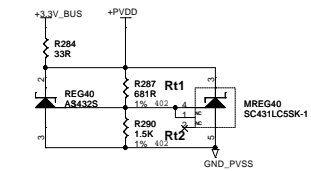


Voltage Req.	R1	R2
0.8V	150R P/N 3160150000	402 P/N 324075R500
1.25V	100R P/N 3160100000	402 P/N 3160100000
1.5V	100R P/N 3160100000	402 P/N 3160150000
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

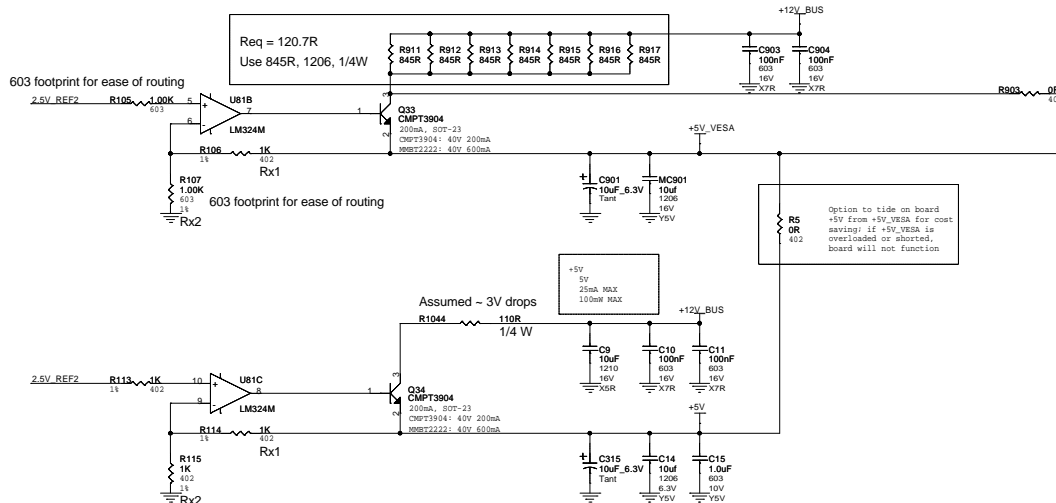
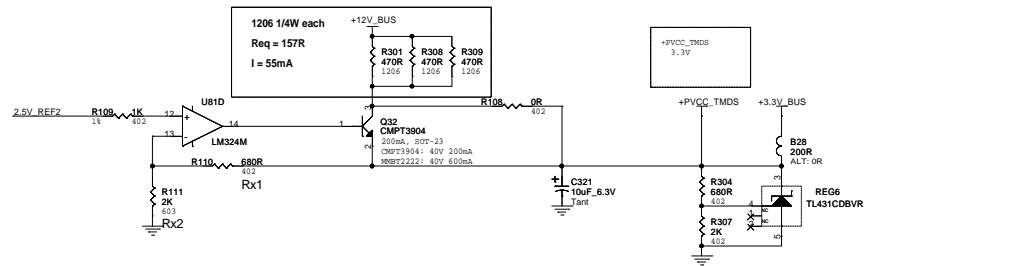
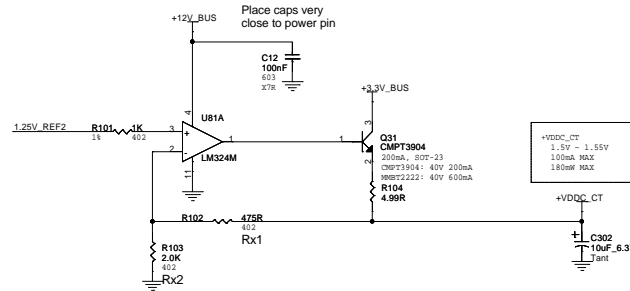
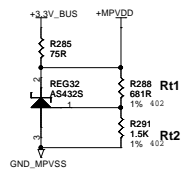
Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.55	475R (402, 1%) P/N 3160200100G (402) P/N 3160475000	2K (1%) P/N 3160200100G (402) P/N 3240200100 (603)
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 P/N 3160681000	1.5K P/N 3240150100

Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100 P/N 3160107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.61V	221R (402, 1%) P/N 3160221000	4.99K (402, 1%) P/N 3160499100
2.5V	OR P/N 3230000000 P/N 3150000000	DNI

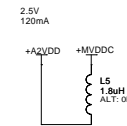
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



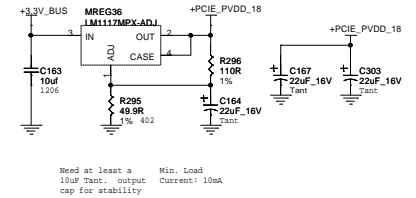
Alt. regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX



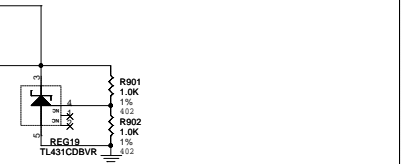
Alt. regulator for +A2VDD
Vout = 2.5V
Iout = 120mA MAX



Alt. Regulator for PCIE_PVDD_18
Vout = 1.82V
Iout = 500mA MAX



Alt regulator for +5V_VESA

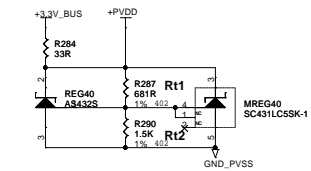


Normal +5V regulated operation
This circuit provide upto 55mA

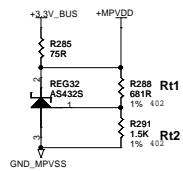
If Iload > 55mA, +5V will drop

If Vout is shorted
Current across each Rx is 12V/845R = 14.2mA
Power dissipated by each Rx is 14.2mA x 12V = 171mW
Each Rx are rated 250mW (1/4W)
Derating 250mW by 70% is 175mW (1/4W)

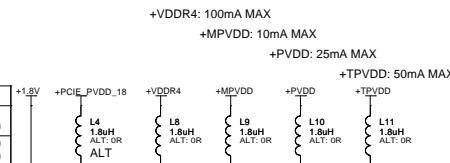
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



Alt. regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX

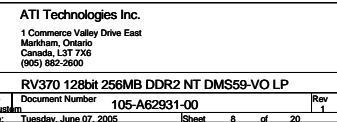
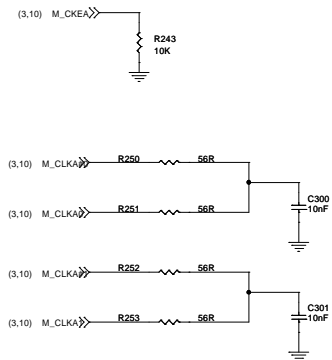


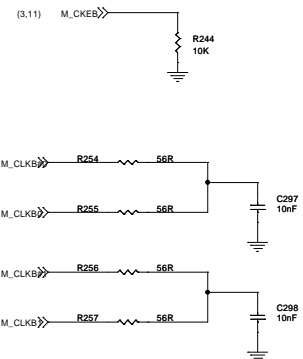
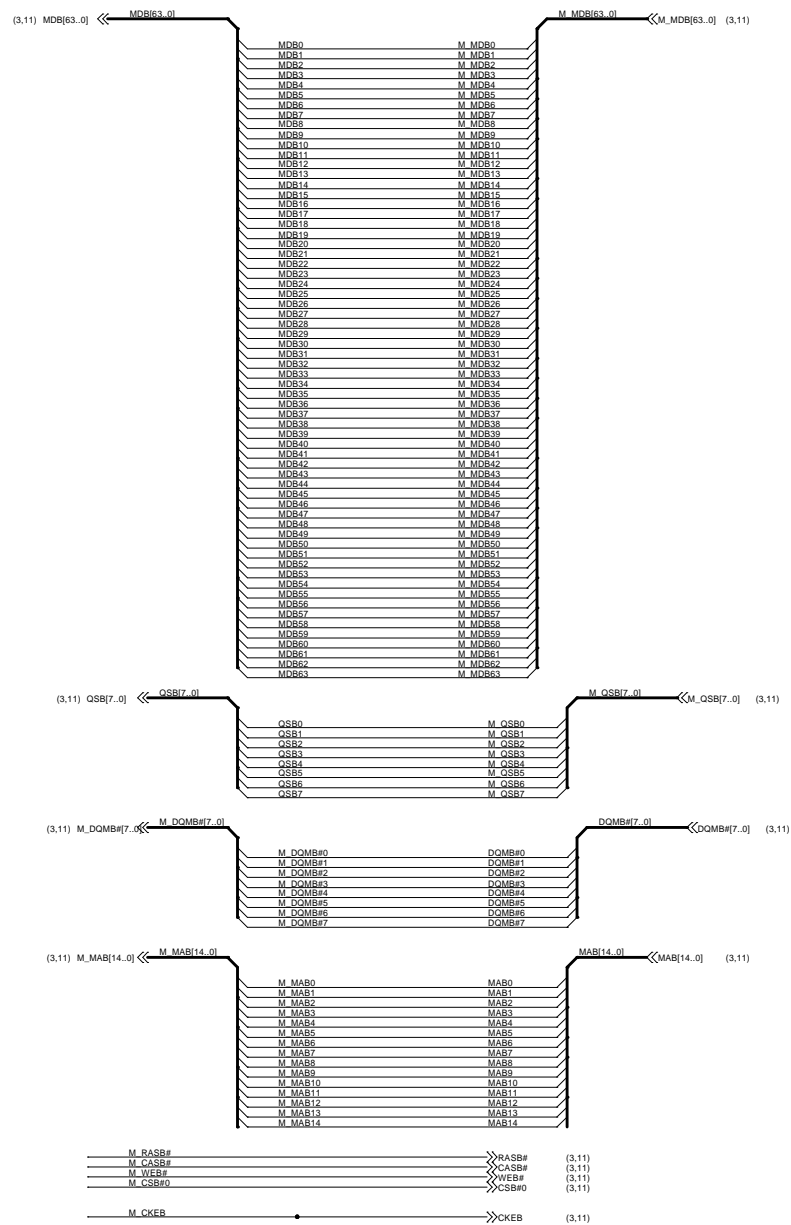
	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100



Rails derived from +1.8V
+AVDD: 10mA MAX
+A2VDD: 20mA MAX
+VDDOL_PINS: 20mA MAX
+TXVDD: 20mA MAX







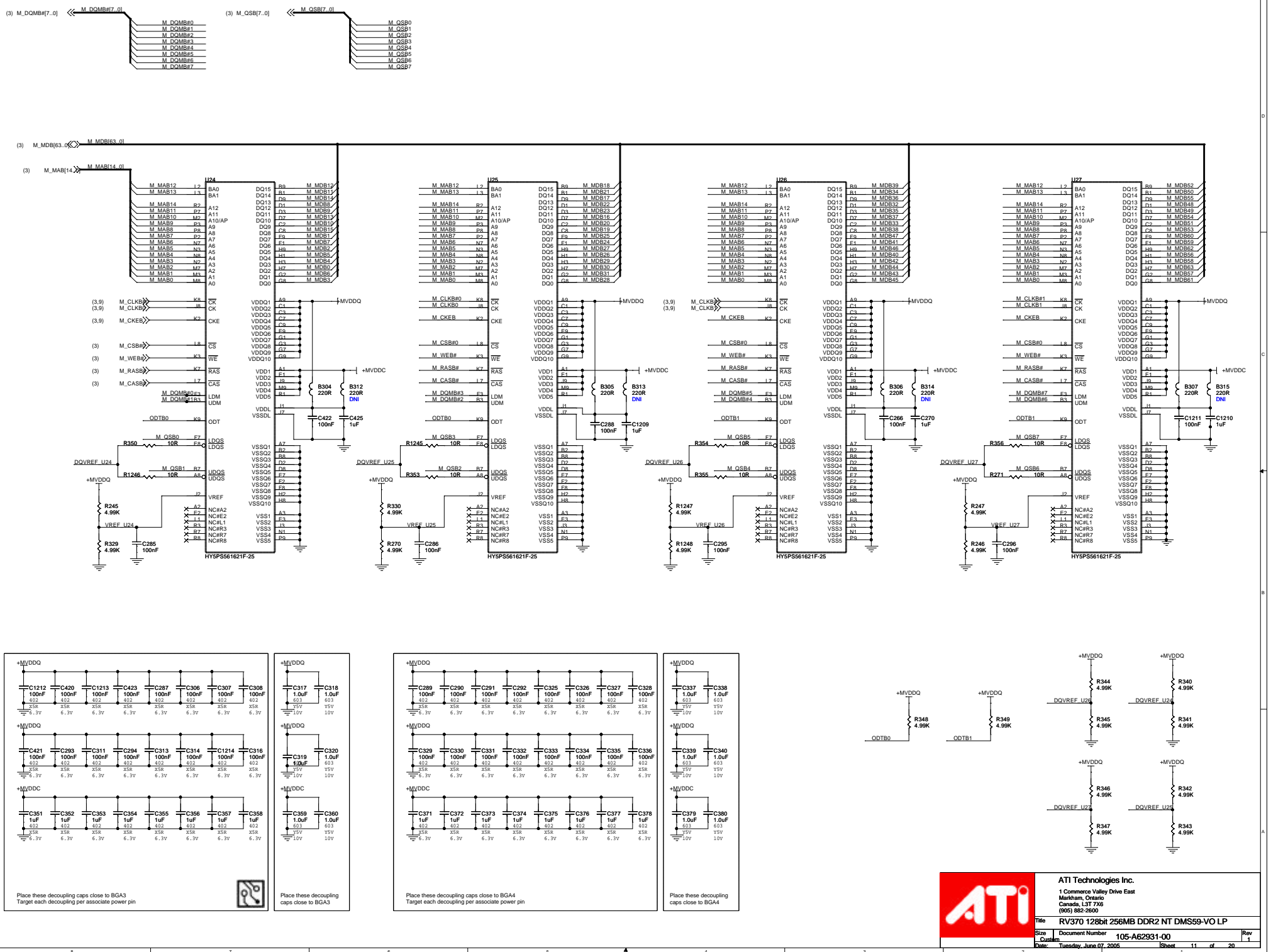
(3,11) M_RASB# >> M_RASB#
 (3,11) M_CKEB >> M_CKEB
 (3,11) M_CASB# >> M_CASB#
 (3,11) M_WEB# >> M_WEB#
 (3,11) M_CSB#0 >> M_CSB#0

(3,11) M_CLKB0 >> M_CLKB0 >> CLKB0 (3,11)
 (3,11) M_CLKB1 >> M_CLKB1 >> CLKB1 (3,11)
 (3,11) M_CLKB2 >> M_CLKB2 >> CLKB2 (3,11)
 (3,11) M_CLKB3 >> M_CLKB3 >> CLKB3 (3,11)

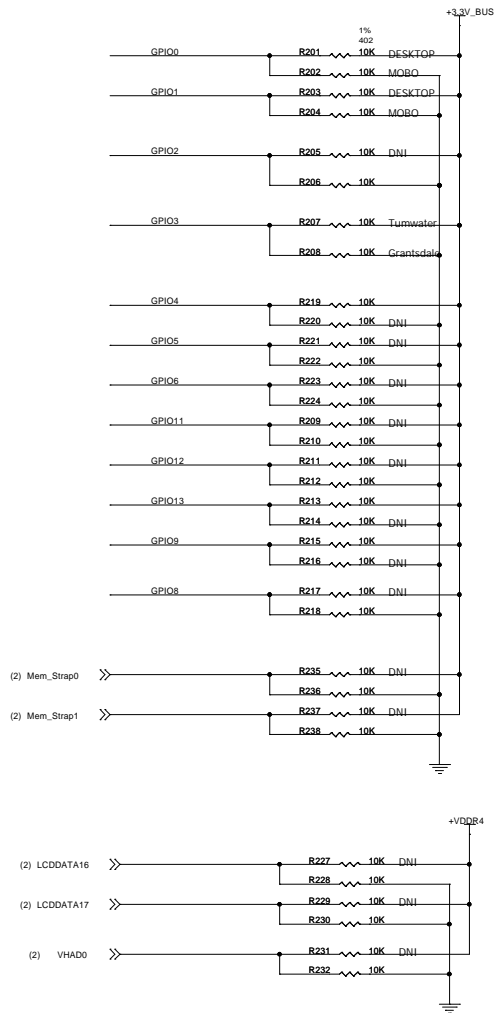


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Title: RV370 128bit 256MB DDR2 NT DMS59-VO LP
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 Date: Tuesday, June 07, 2005 Sheet 9 of 20



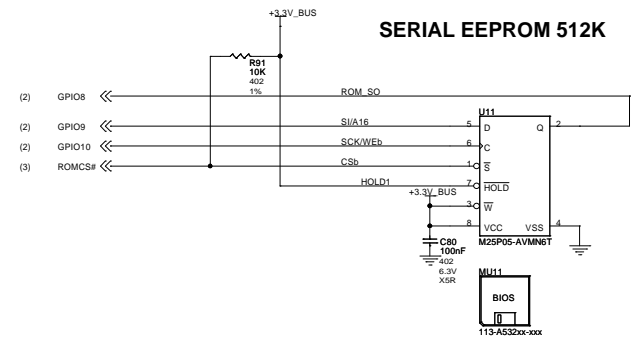
OPTION STRAPS



STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCI_E_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrone-compatible mode 10: PCI Express 1.0 mode (Turmwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PLRL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDs. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDs from ROM 1011 - Serial M25P10 ROM (ST), chip IDs from ROM 1100 - Serial M25P05 ROM (ST), chip IDs from ROM 1109 - Serial NX25F0118 ROM (ISSI), chip IDs from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present 1 - No slave VIP host port devices reporting presence during reset	

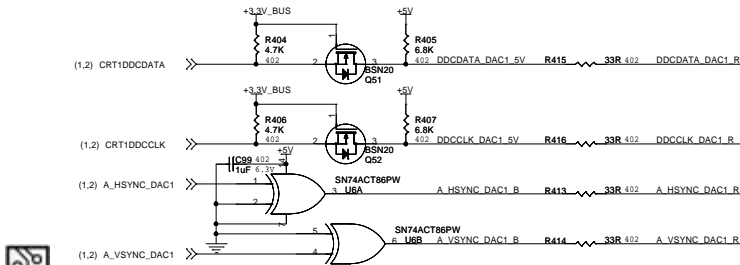
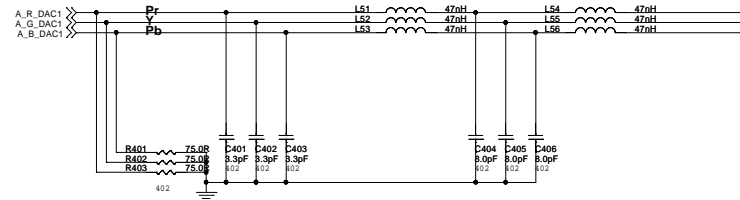
STRAP_P	INTERRUPT
LOW	ENABLED (DEFAULT)
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	0	0
INF	1	0
HYN	0	1
ELPIDA	1	1





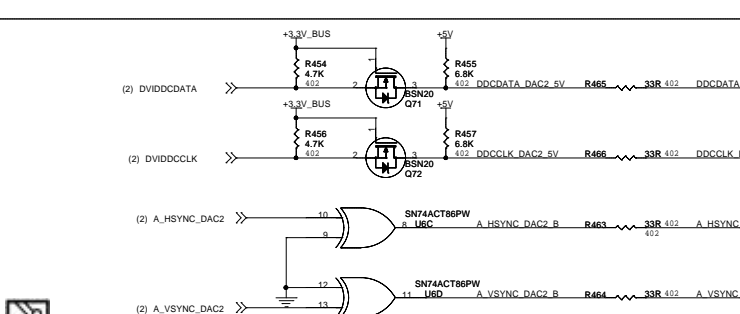
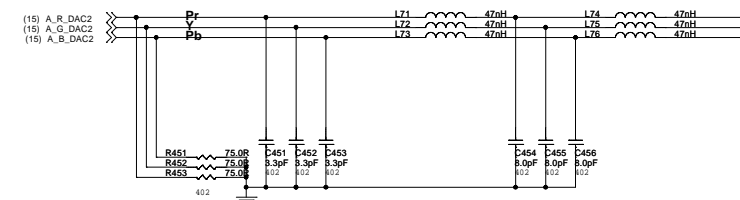
Place close to the ASIC
RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane



SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane



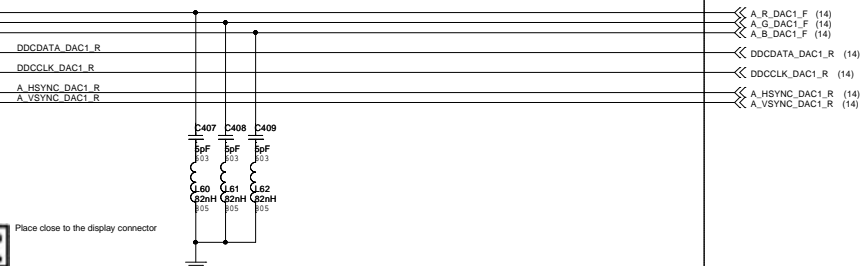
Place close to the ASIC
RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane



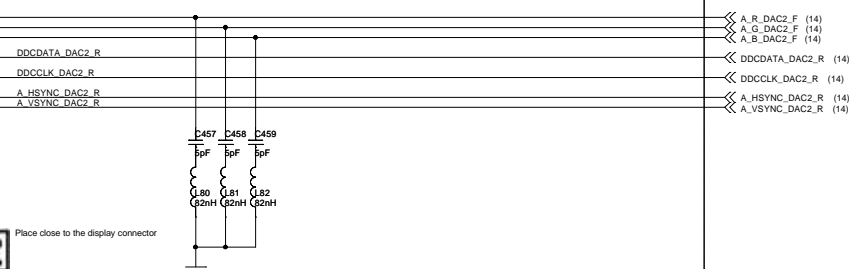
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane



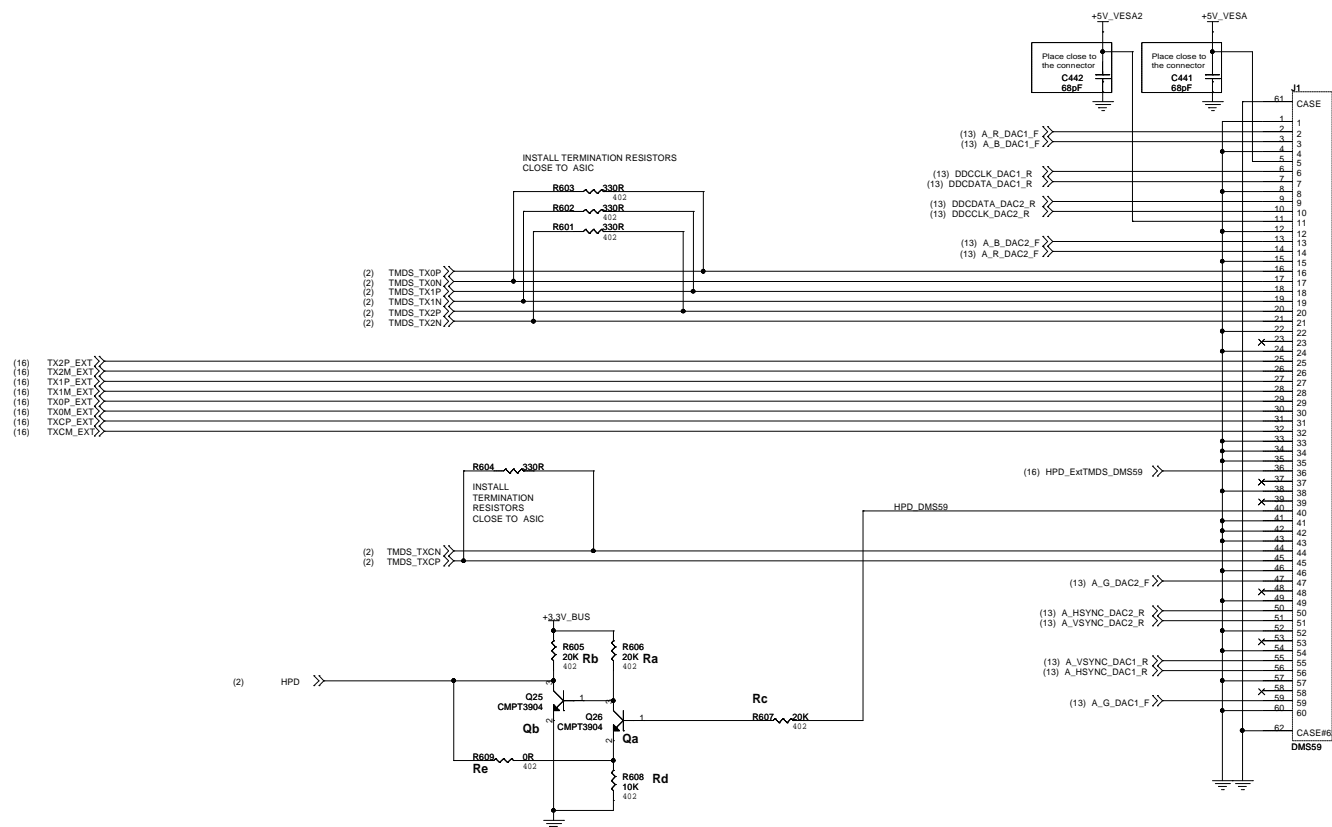
Place close to the display connector



Place close to the display connector



VESA Multi-Display Interface DMS-59 Connector



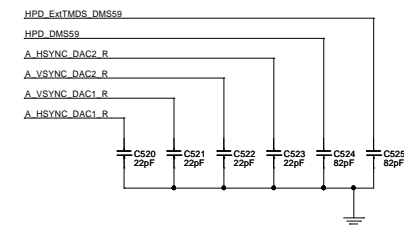
Connector 1	
Signals	Mapping
VGA:	DAC1
DVI:	External TMD5
HPD:	External TMD5 HPD
DDC:	CRT1 DDC
5V:	+5V_VESA

Connector 2	
Signals	Mapping
VGA:	DAC2 (TV/DAC)
DVI:	Internal/Integrated TMD5
HPD:	Internal/Integrated TMD5 HPD
DDC:	DVI DDC
5V:	+5V_VESA2

STUFFING OPTIONS

Hot-Plug Detect Circuit	MUST INSTALL	MUST NOT INSTALL
Type A	Ra, Rb, Rc, Rd=0R, Qa, Qb	Re
Type B	Ra=0R, Rc, Rd=10K, Re, Qa	Rb, Qb

	HPD_ExtTMD5_DVI	HPD_ExtTMD5 Type A	HPD_ExtTMD5 Type B
NC	High Z	0 (0V)	0 (0V)
Connected	5V	1 (3.3V)	1 (3.3V)



EMI Capacitors, place close to connector



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Title	RV370 128bit 256MB DDR2 NT DMS59-VO LP		
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From DAC2

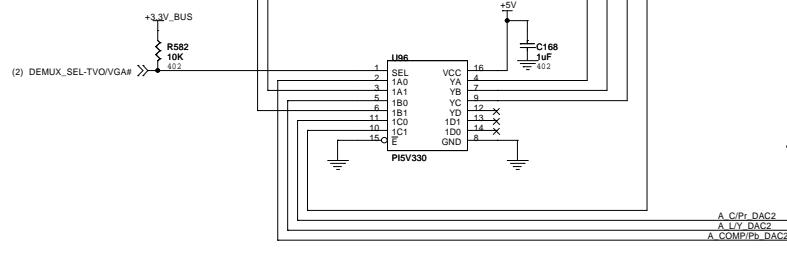
R/C/Pr
G/L/Y
B/COMP/Pb

(2) A_R/C/Pr_DAC2
(2) A_G/L/Y_DAC2
(2) A_B/COMP/Pb_DAC2

DAC2 DeMux

To VGA Filters

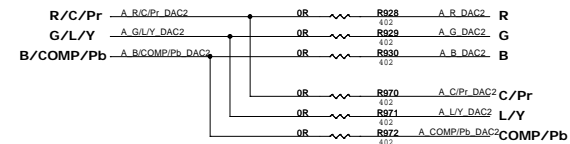
R
G
B



To TVO filters

C/Pr
L/Y
COMP/Pb

DAC2 DeMux BYPASS



From VGA DeMux

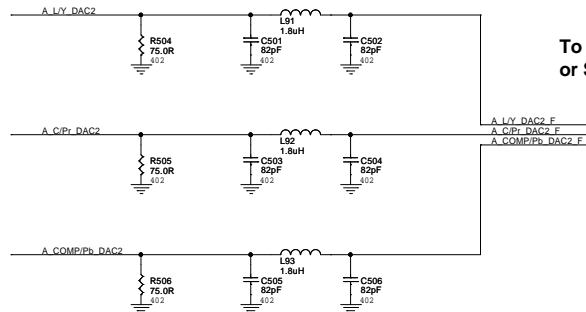
L/Y

C/Pr

COMP/Pb

To TVO Connector or STV/HDTV DeMux

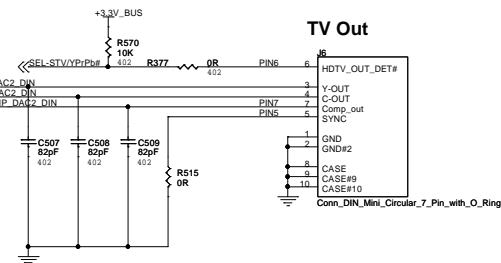
L/Y
C/Pr
COMP/Pb



From TVO Filters

L/Y
C/Pr
COMP/Pb

(2) SEL-STV/YPr/Pb#
(2) SEL-STV/YPr/Pb#
(2) SEL-STV/YPr/Pb#



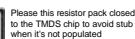
TV Out

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500
- 4-pin Svideo MiniDIN P/N 6070001000



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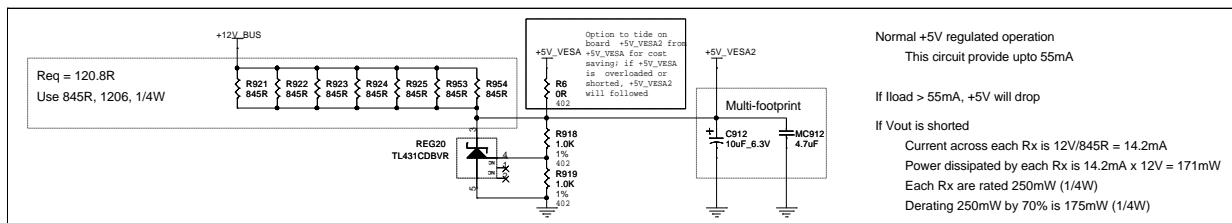
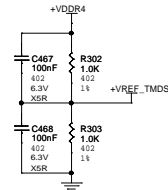
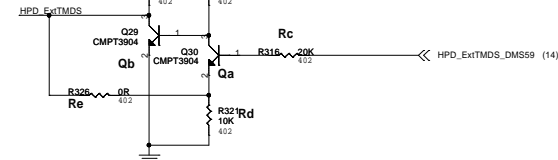
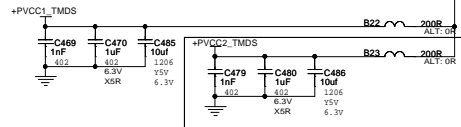
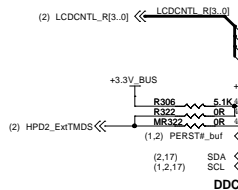
Title		RV370 128bit 256MB DDR2 NT DMS59-VO LP	
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LCDCNTL R[3:0]

Signal	Resistor	Value
LCDCNTL R0	RP600A	10K
LCDCNTL R1	RP600B	10K
LCDCNTL R2	RP600C	10K
LCDCNTL R3	RP600D	10K

+3.3V_BUS



STUFFING OPTIONS

EXT TMD5 TX TO BE USED MUST INSTALL MUST NOT INSTALL CAN BE REMOVED

Sil1162 R Ext-Swing = 523R

NOTE:

- 1 - Other components are to be installed.
- 2 - Components marked as DNI should not be installed. They should only be installed if default board settings are to be changed in which case other components may have to be adjusted accordingly.

STUFFING OPTIONS		
Hot-Plug Detect Circuit	MUST INSTALL	MUST NOT INSTALL
Type A	Ra, Rb, Rc, Rd=0R, Qa, Qb	Re
Type B	Ra=0R, Rc, Rd=10K, Re, Qa	Rb, Qb

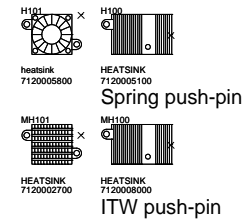
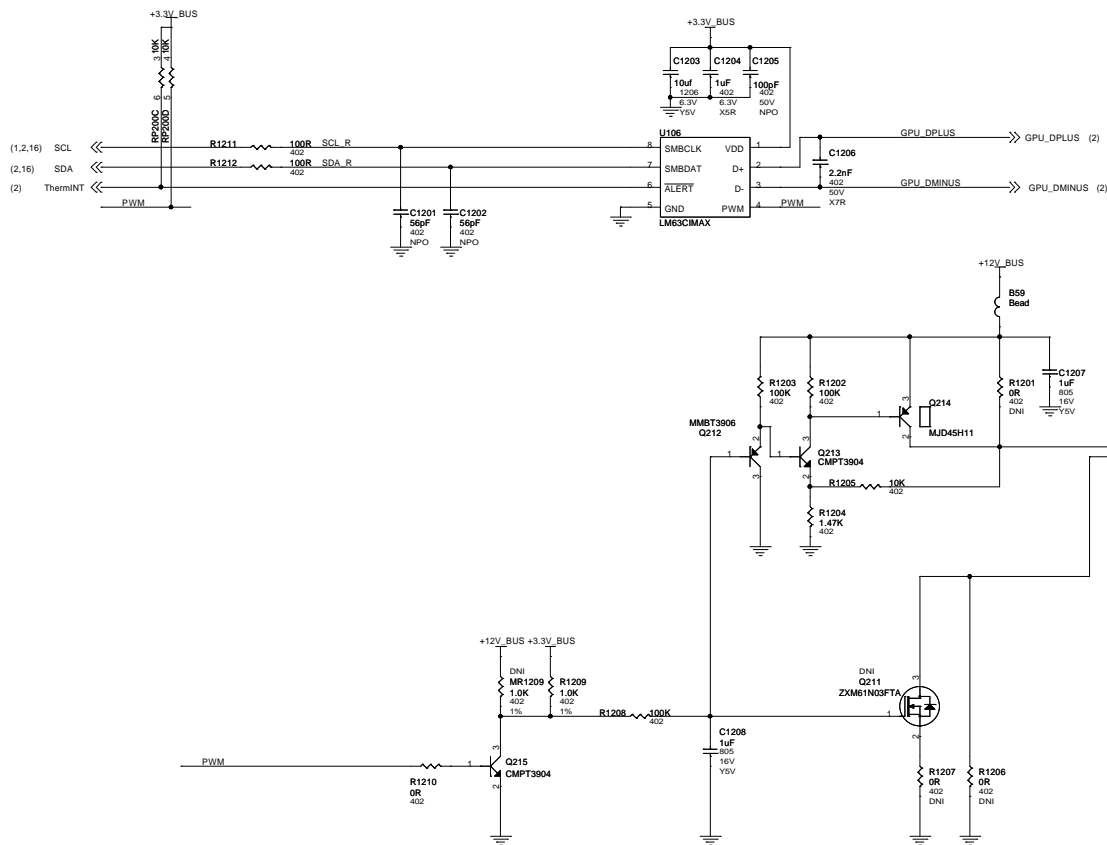
	HPD_ExtTMDS_DVI	HPD_ExtTMDS Type A	HPD_ExtTMDS Type B
NC	High Z	0 (0V)	0 (0V)
Connected	5V	1 (3.3V)	1 (3.3V)



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Canada, L3T 7X6
(416) 491-0000

Title	RV370 128bit 256MB DDR2 NT DMS59 V/O L E
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Size	Document Number	Rev
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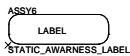
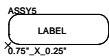
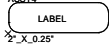
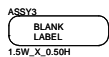
DVI/VGA SCREWS



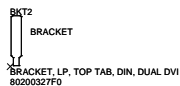
Bracket Screws



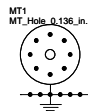
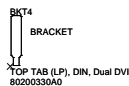
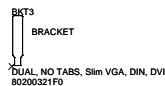
MISC. BOARD PARTS

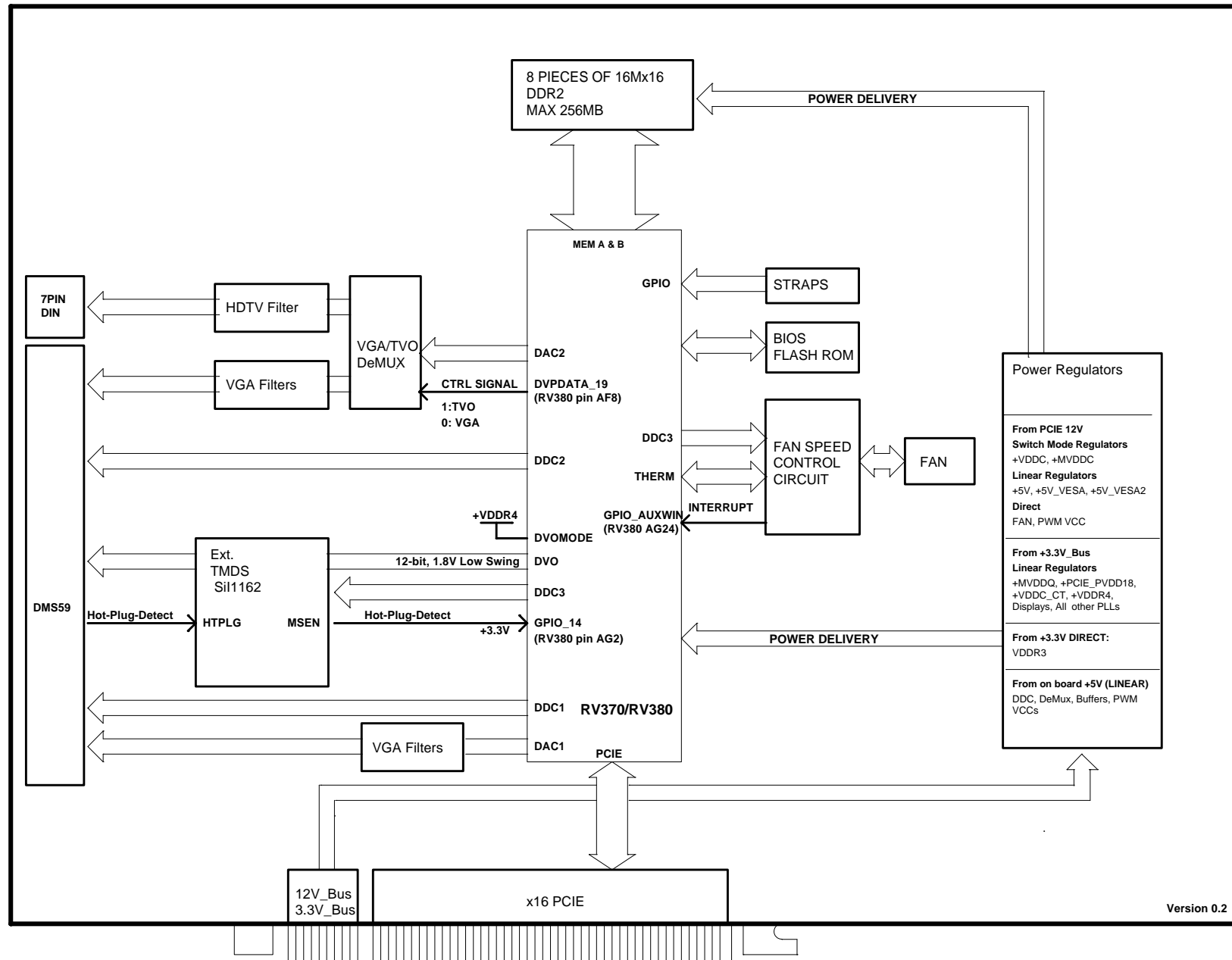


LP brackets



ATX brackets





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