
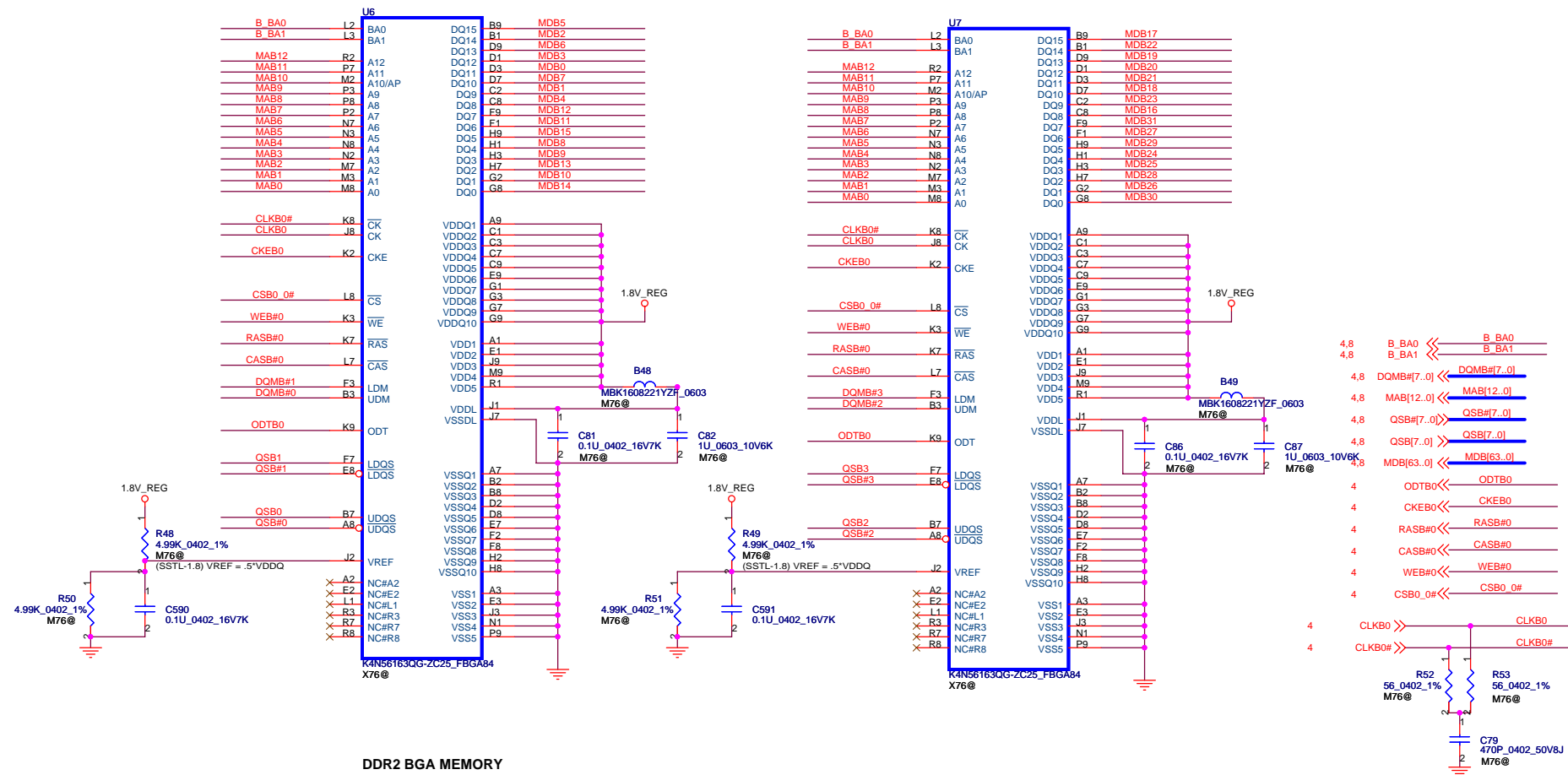


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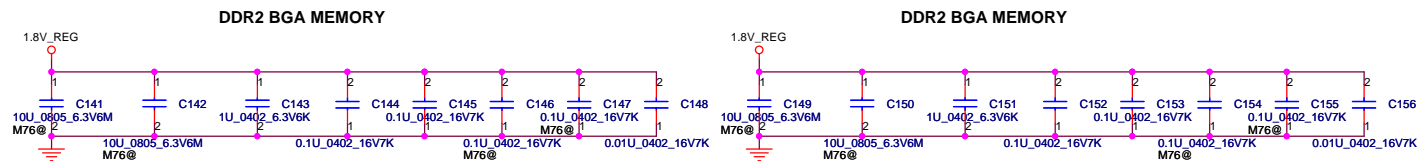
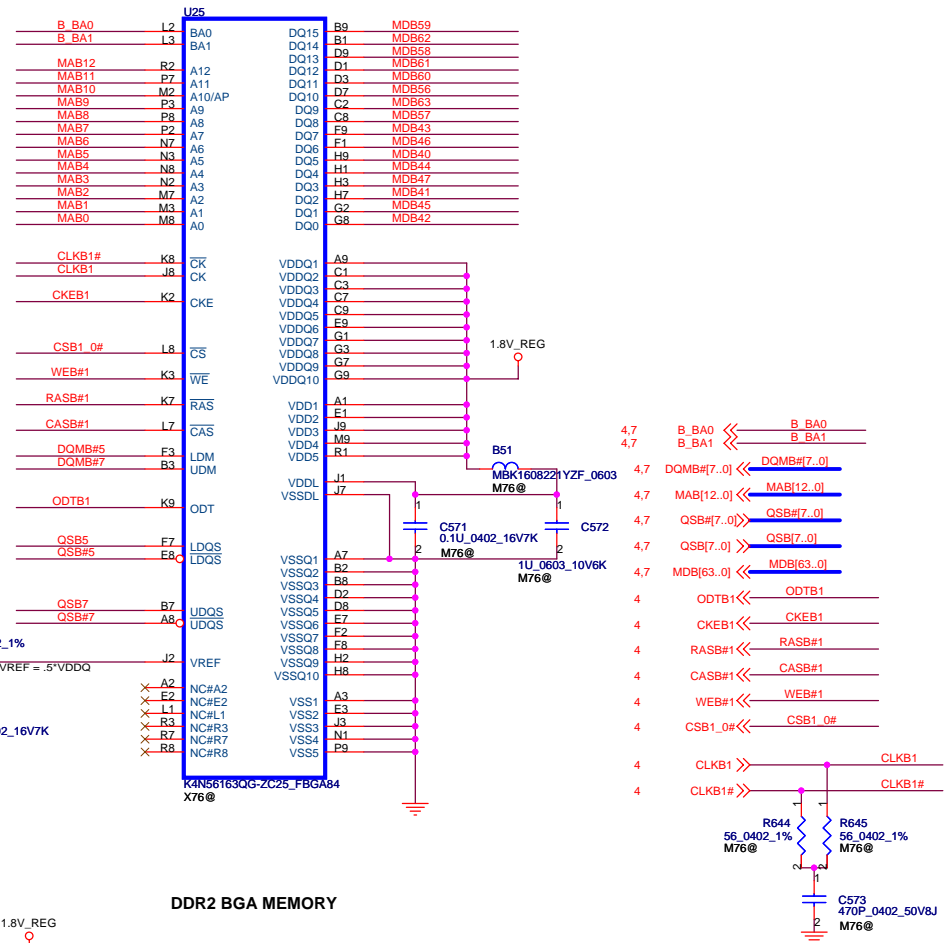
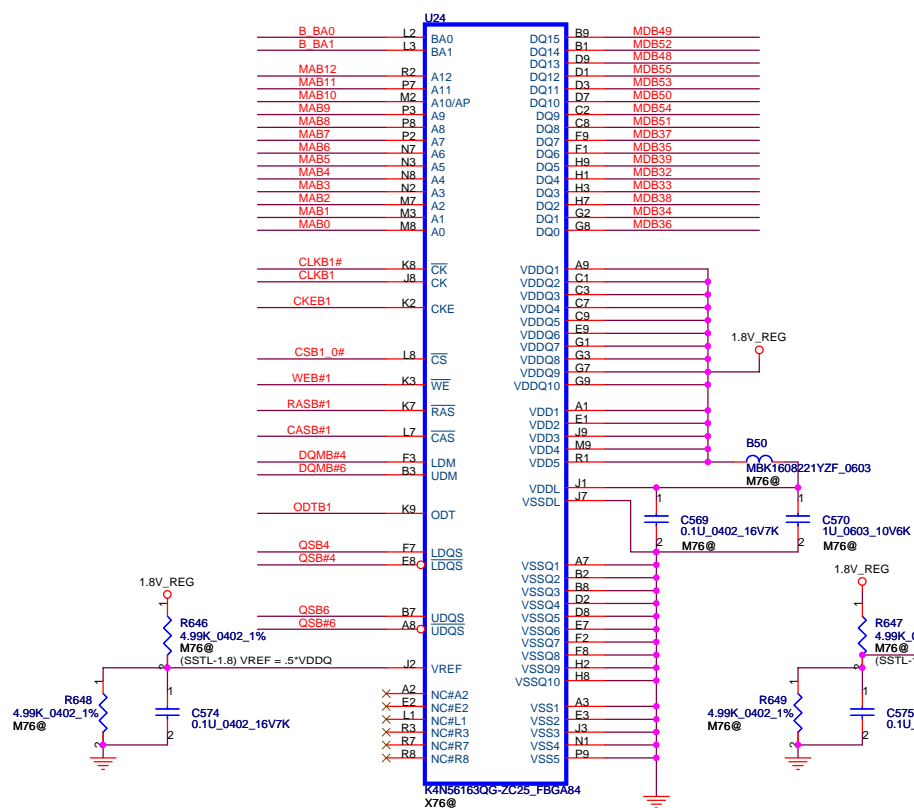
		ATI Technologies Inc. 1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600	
		Title: M76MXT 256MB DDR2 Size: Custom Date: Monday, April 09, 2007	
Document Number: 105-B24731-00A		Rev: 0	
Sheet: 5 of 13			



CHAN C RANK0 DDR2 BGA MEMORY

<Variant Name>

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		1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600	
Title	Custom	M76MXT 256MB DDR2	
Size	Document Number	105-B24731-00A	Rev 0
Date	Wednesday, May 23, 2007	Sheet 7 of 13	



CHAN D RANK0 DDR2 BGA MEMORY



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(905) 882-2600

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Size	Document Number	105-B24731-00A
Custom		

Date: Wednesday, May 23, 2007 Sheet 8 of 13

Rev	0
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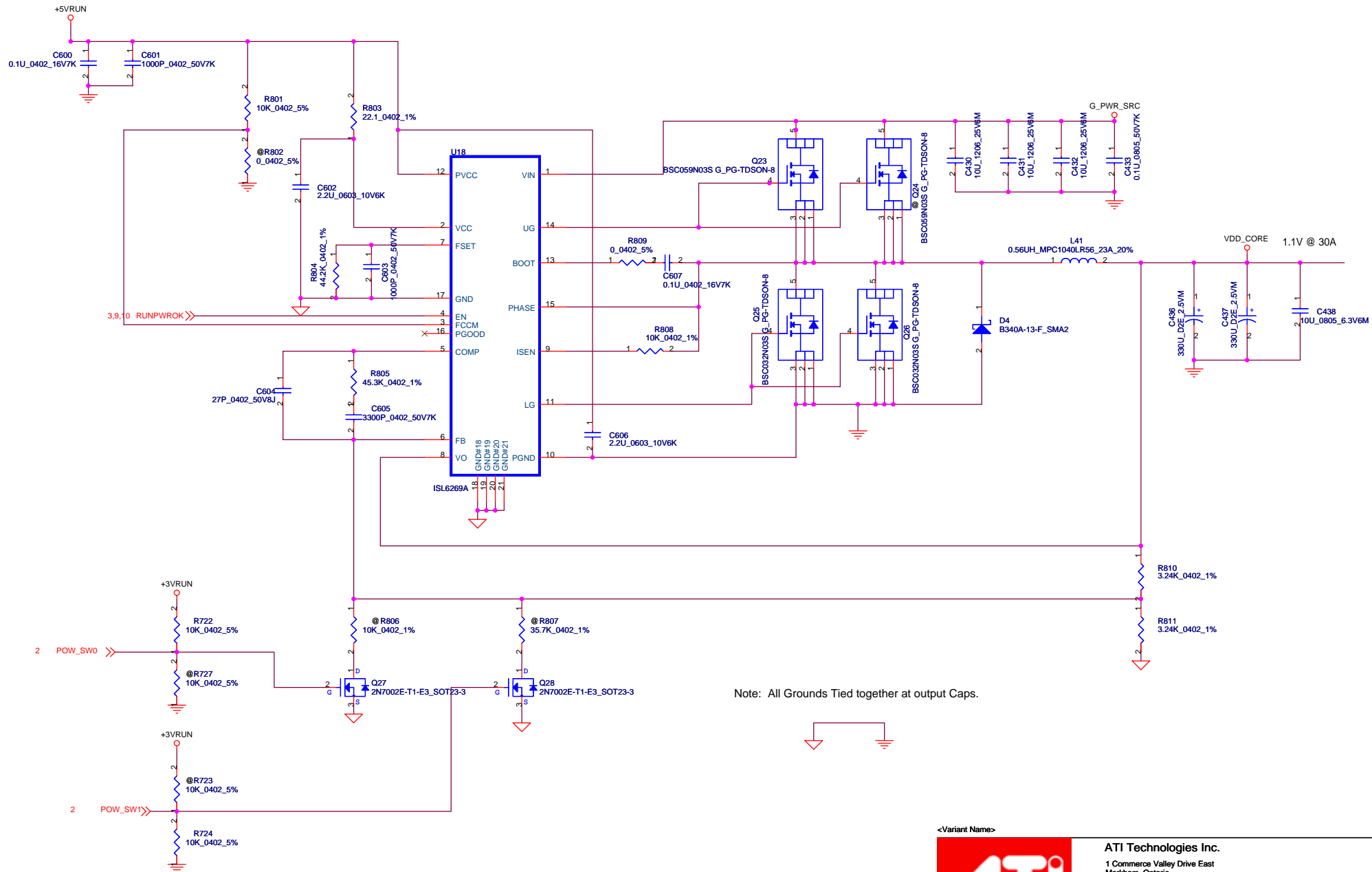
G_PWR_SRC



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Canada, L3T 7X6
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CORE PWM REGULATOR .95V - 1.1V @ 30A



Note: All Grounds Tied together at output Caps.

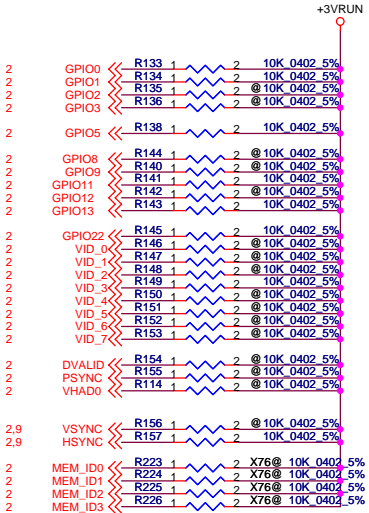
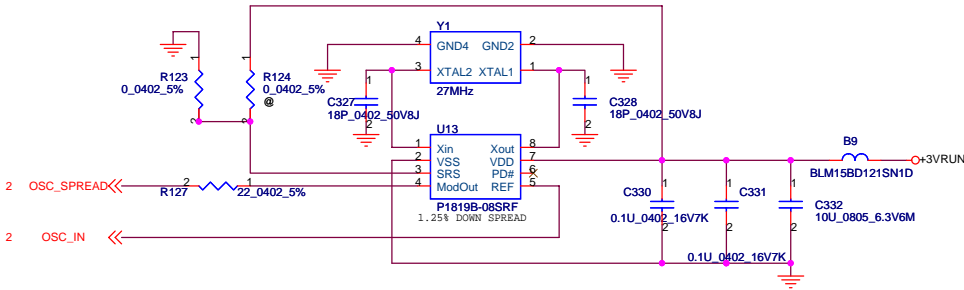
<Variant Name>



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MEMORY CLOCK SPREAD SPECTRUM

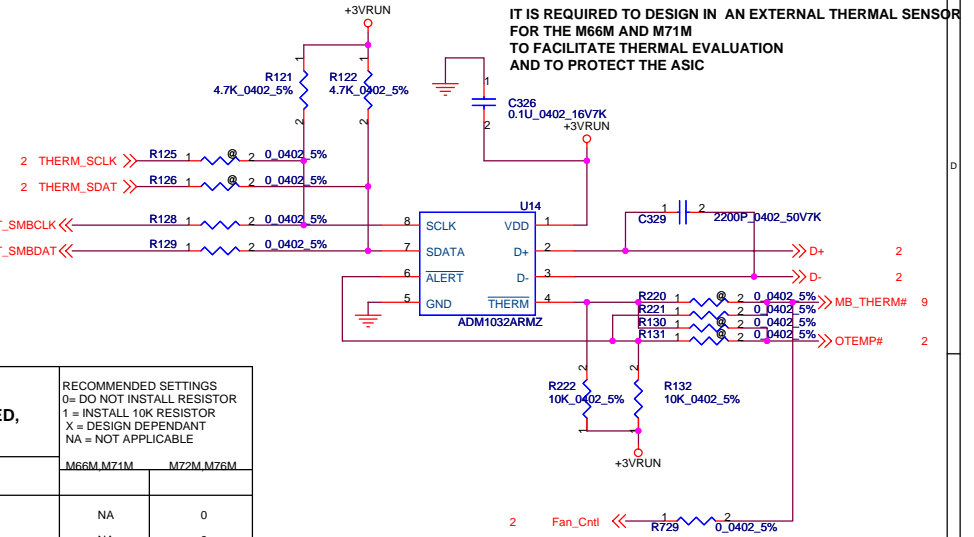


CONFIGURATION STRAPS			RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M66M,M71M	M72M,M76M
BIF_MSI_DIS	VID1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_64BAR_EN_A	VID5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	1
PLL_IBIAS_RD_0	GPIO5	M66(71)BIAS CURRENT FOR PCIE PHY PLL LSBIT (M72(76)RSVD)	1	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1	1
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYN	IGNORE VIP DEVICE STRAPS	X	X
BIF_VGA_DIS	PSYN	VGA ENABLED	NA	0
MEM_TYPE	UNUSED GPIO	MEMORY TYPE,MAKE AND SIZE INFO	X X X	X X X

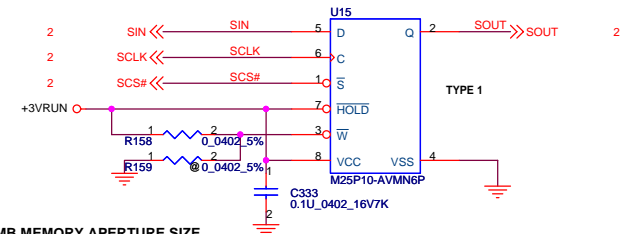
ATI RESERVED CONFIGURATION STRAPS												
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET												
VID0	VID2	VID3	VID4	VID6	VID7	HSYN	DVALID	GPIO2	GPIO3	GPIO5	GPIO6	GPIO8
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET												
GPIO_28_TDO	GENERICC	GPIO21_BB_EN	GPIO_23_CLKREQB (DRIVES LOW DURING RESET)	H2SYN	V2SYN							

Vedio Memory Config. (GPU Internal PD)							
	R224	R223	R225	R226	MEM	Size	Vendor Chips
M74	0	0	0	0	128MB	16Mx16	Samsung x4
	0	0	0	1	256MB	32Mx16	Samsung x4
	0	0	1	0	128MB	16Mx16	Hynix x4
	0	0	1	1	256MB	32Mx16	Hynix x4
	0	1	0	0	128MB	16Mx16	Infineon x4
	0	1	0	1	256MB	32Mx16	Infineon x4
M76	0	0	0	0	256MB	16Mx16	Samsung x8
	0	0	0	1	512MB	32Mx16	Samsung x8
	0	0	1	0	256MB	16Mx16	Hynix x8
	0	0	1	1	512MB	32Mx16	Hynix x8
	0	1	0	0	256MB	16Mx16	Infineon x8
	0	1	0	1	512MB	32Mx16	Infineon x8

DVPDATA22 DVPDATA6
DVPDATA23 DVPDATA7




FLASH ROM



A 256MB MEMORY APERTURE SIZE CAN BE DEFINED USING A SEPARATE ROM OR STRAPPING

<Variant Name>

	ATI Technologies Inc.			
	1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600			
	Title M76MXT 256MB DDR2			
	Size B	Document Number	105-B24731-00A	Rev 0
	Date:	Friday, May 25, 2007	Sheet 12 of 13	



Title
M76MXT 256MB DDR2

Schematic No.
105-B24731-00A

Date:
Wednesday, January 10, 2007

REVISION HISTORY

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	04/10/06	PROTOTYPE BASED ON 105-B17831-00A