

P616-A03: G96-GB1-128, MXM-II, 512/256MB GDDR3 (32/16Mx32), LVDS, DP-A/B, DVI -A/B/C, TV_OUT, VGA, HD AUDIO, SPDIF
MXM 2.1a SPECIFICATION COMPLIANT

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SKU	VARIANT	NVPN	ASSEMBLY
B	Base	600-10616-0000-300	BASE LEVEL GENERIC SCHEMATIC ONLY
1	SKU0001	600-10616-0001-300	NB9P-GS G96M, 800MHz 512MB(128bit) GDDR3 32Mx32 136FBGA, LVDS + DP-A + DVI-A + SD/HD(TV_OUT) + VGA
2	SKU0002	600-10616-0002-300	NB9P-GS G96M, 800MHz 256MB(128bit) GDDR3 16Mx32 136FBGA, LVDS + DP-A + DVI-A + SD/HD(TV_OUT) + VGA
3	SKU0003	600-10616-0003-300	NB9P-GE2 G96M, 800MHz 512MB(128bit) GDDR3 32Mx32 136FBGA, LVDS + DP-A + DVI-A + SD/HD(TV_OUT) + VGA
4	SKU0004	600-10616-0004-300	NB9P-GE2 G96M, 800MHz 256MB(128bit) GDDR3 16Mx32 136FBGA, LVDS + DP-A + DVI-A + SD/HD(TV_OUT) + VGA
5	SKU0005	600-10616-0005-300	NB9P-GS G96M, 800MHz 512MB(128bit) GDDR3 32Mx32 136FBGA, LVDS + DP-B + DVI-A + DVI-B + SD/HD(TV_OUT) + VGA
6	SKU0006	600-10616-0006-300	NB9P-GS G96M, 800MHz 512MB(128bit) GDDR3 32Mx32 136FBGA, LVDS + DP-B + DP-C + DVI-B + SD/HD(TV_OUT) + VGA
7	SKU0011	600-10616-0011-300	NB9P-GS G96M 55nm, 800MHz 512MB(128bit) GDDR3 32Mx32 136FBGA, LVDS + DP-A + DVI-A + SD/HD(TV_OUT) + VGA
8	SKU0500	600-50616-0500-300	NB9P-GLM2 G96M, 800MHz 256MB(128bit) GDDR3 16Mx32 136FBGA, DVI-C + DVI-A + DVI-B + SD/HD(TV_OUT) + VGA
9	SKU9998	600-10616-9998-300	All components
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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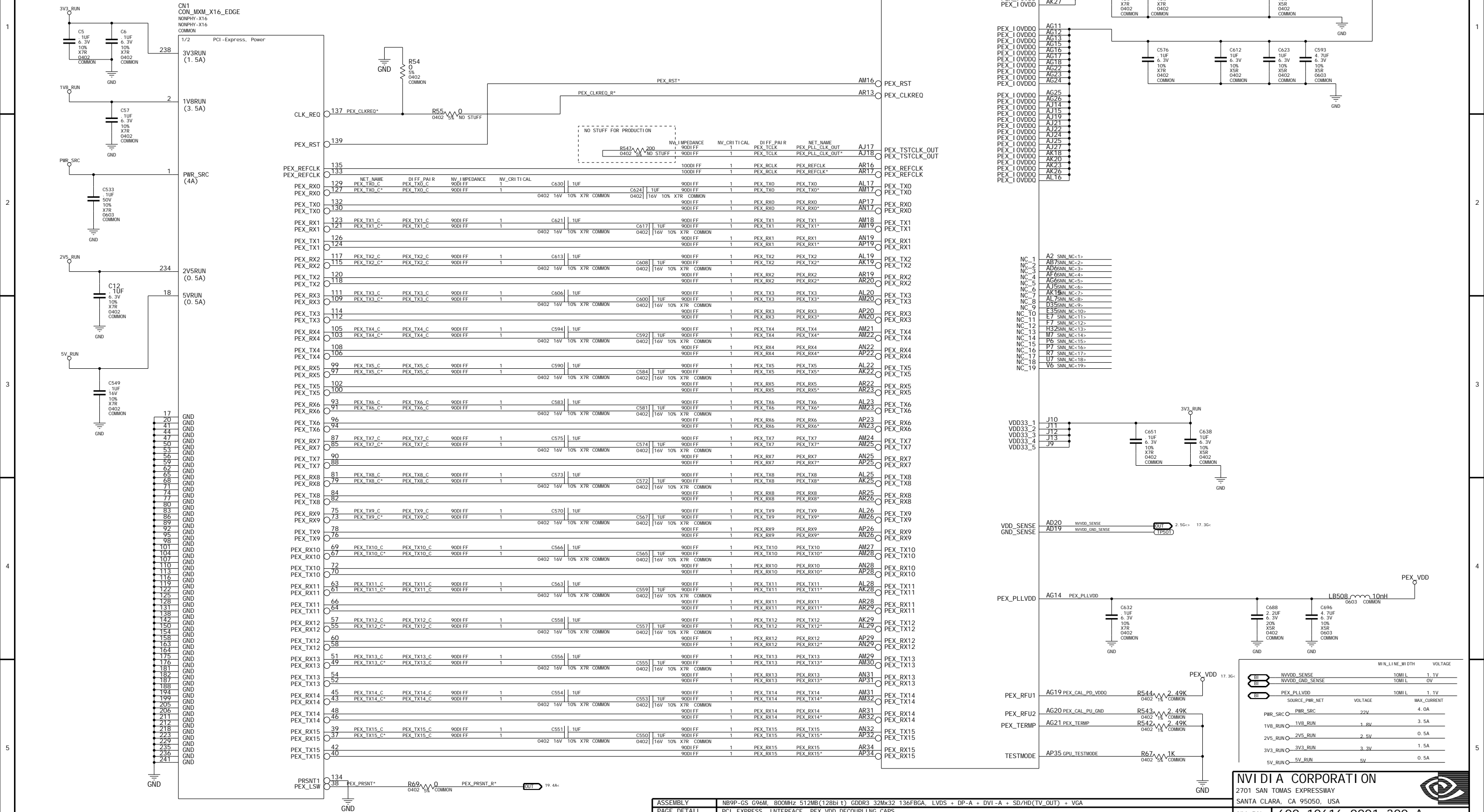
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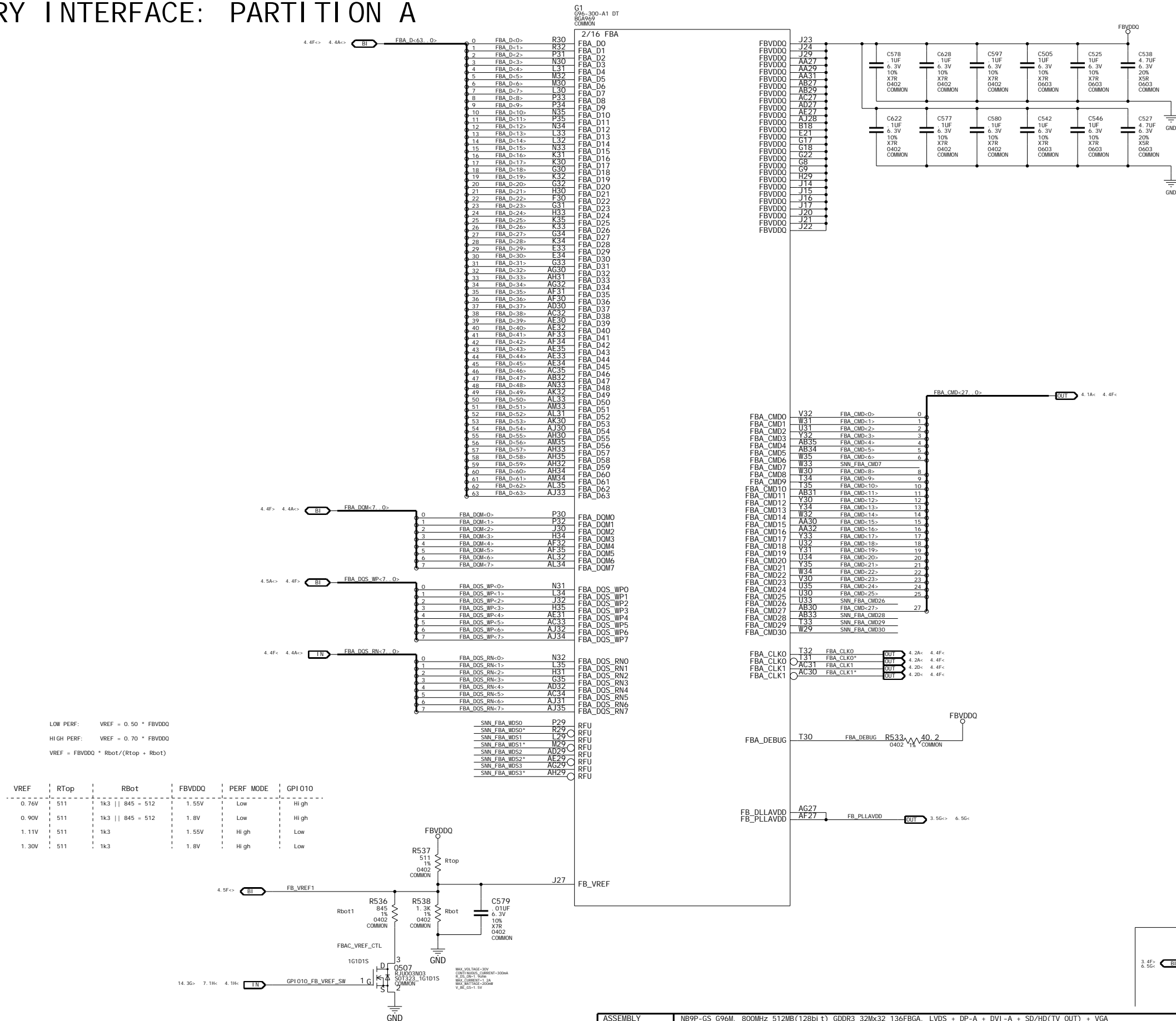


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PCI EXPRESS



GPU MEMORY INTERFACE: PARTITION A

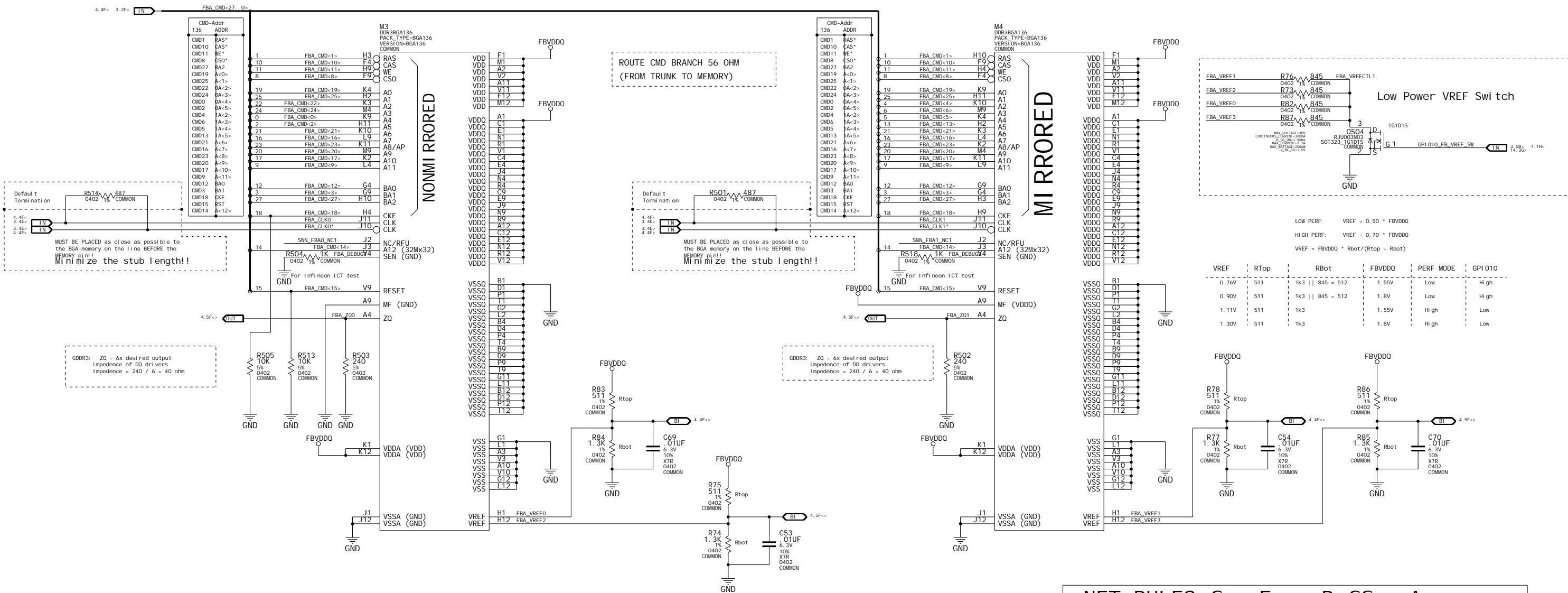


ASSEMBLY	NB9P-GS G96M, 800MHz 512MB(128bi t) GDDR3 32Mx32 136FBGA, LVDS + DP-A + DVI -A + SD/HD(TV_OUT) + VGA
PAGE DETAIL	FBA MEMORY INTERFACE & FBVDDO DECOUPLING CAPS

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FRAME BUFFER PARTITION A



NET RULES for FrameBuffer A

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBA_CLK0	1	80DIFF	FBA_CLK0
FBA_CLK0*	1	80DIFF	FBA_CLK0
FBA_CLK1	1	80DIFF	FBA_CLK1
FBA_CLK1*	1	80DIFF	FBA_CLK1

FBA_DQS_WP<7>_O	1	50OHM	
FBA_DQS_WP<7>_I	1	50OHM	
FBA_D<63>_O	1	50OHM	
FBA_D<63>_I	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBA_VREF0	1.47V	0.02A	12MIL
FBA_VREF1	1.47V	0.02A	12MIL
FBA_VREF2	1.47V	0.02A	12MIL
FBA_VREF3	1.47V	0.02A	12MIL
FBA_Z00	1.47V	0.02A	12MIL
FBA_Z01	1.47V	0.02A	12MIL
FB_VREF1	1.47V	0.02A	12MIL

ASSEMBLY	NB9P-GS G94M, 800MHz 512MB(128bit) GDDR3 32Mx32 136FBGA, LVDS + DP-A + DVI-A + SD/HD(TV_OUT) + VGA
PAGE	DETAIL
	FRAME BUFFER A MEMORIES

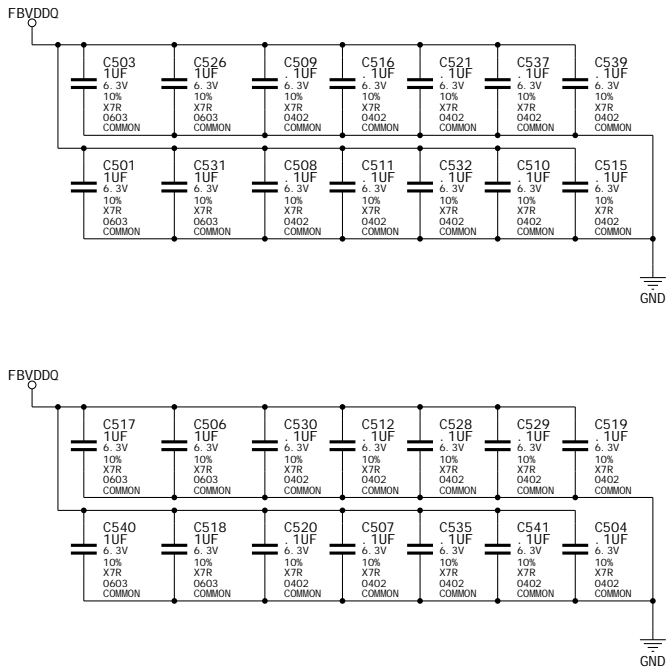
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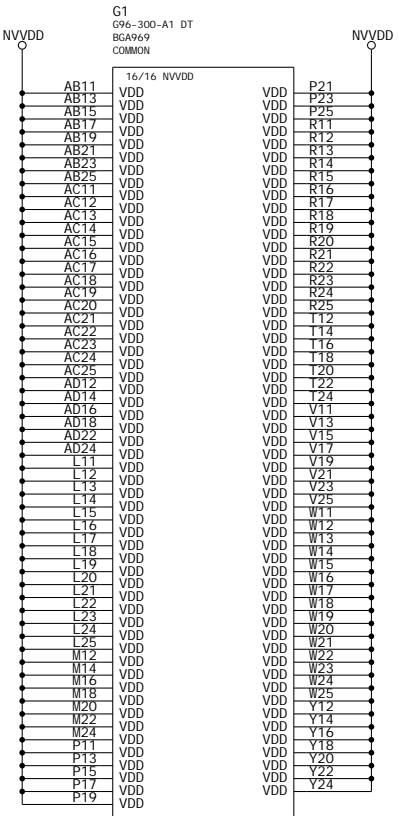
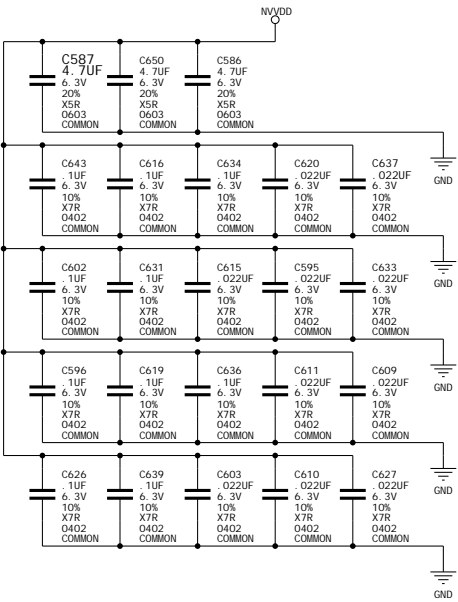
FRAME BUFFER: PARTITION A DECOUPLING



Decoupling for
FBA North Side
Memory Device.

Decoupling for
FBA South Side
Memory Device.

NVVDD POWER AND DECOUPLING



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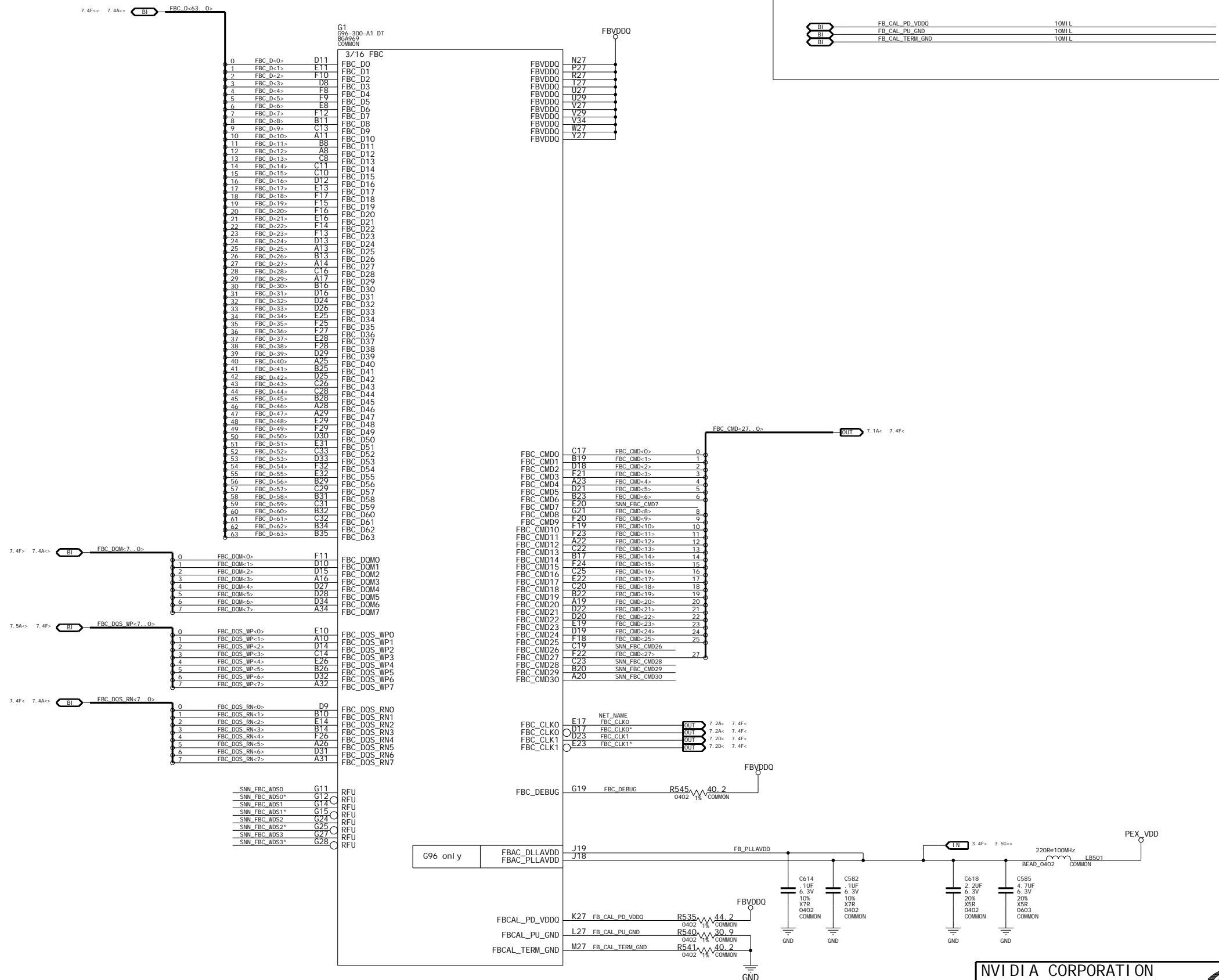


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GPU MEMORY INTERFACE: PARTITION C



ASSEMBLY	NB9P-GS G96M, 800MHz 512MB(128bit) GDDR3 32Mx32 136FBGA, LVDS + DP-A + DVI-A + SD/HD(TV_OUT) + VGA
PAGE DETAIL	FBC MEMORY INTERFACE

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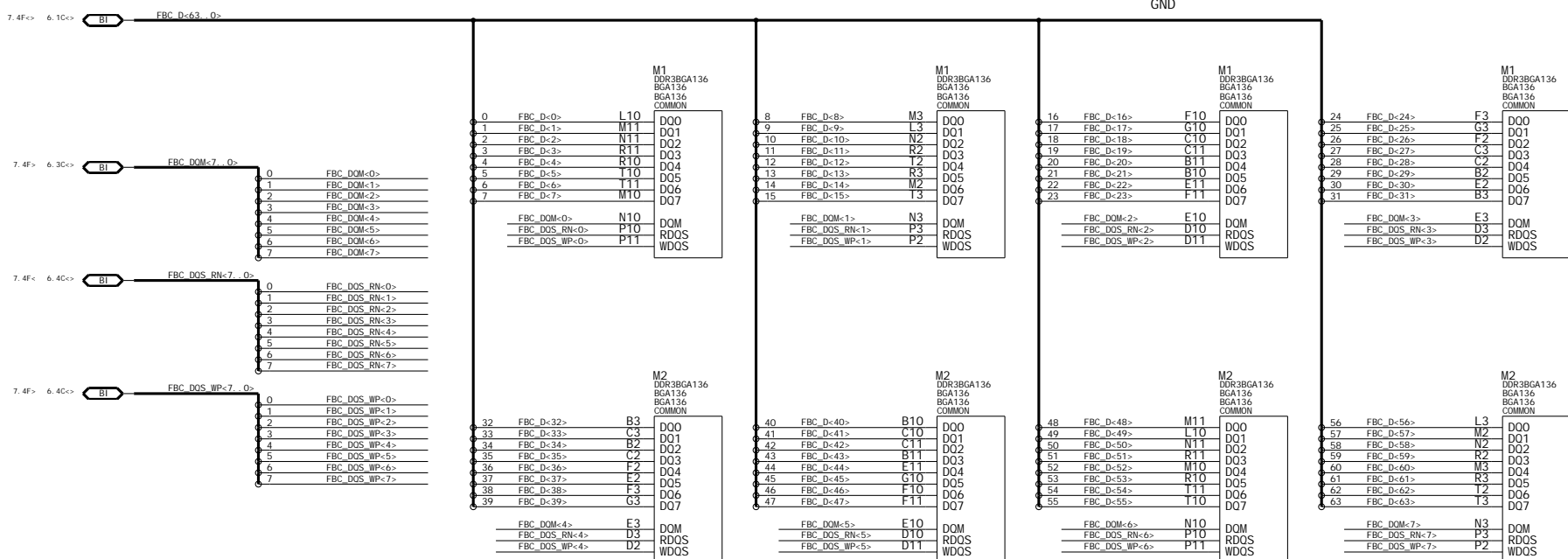
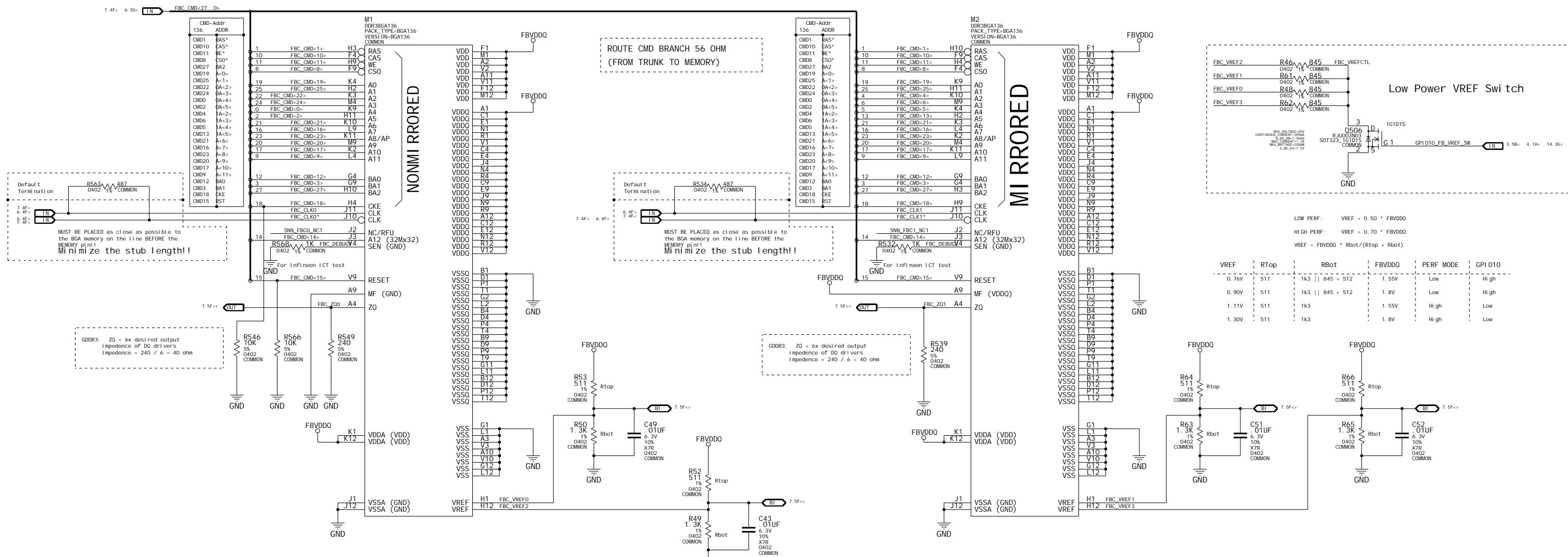
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FRAME BUFFER PARTITION C

NET RULES for StringBuffer C

	NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
7.2K~ 6.4F*	 FBC_CLK0	1	800I FF	FBC_CLK0
7.2K~ 6.4F*	 FBC_CLK0*	1	800I FF	FBC_CLK0
7.2K~ 6.4F*	 FBC_CLK1	1	800I FF	FBC_CLK1
7.2K~ 6.4F*	 FBC_CLK1*	1	800I FF	FBC_CLK1

7.5A<>	6.4C<>	OUT	FBC DOS WP<7.0>	1	500HM
7.4A<>	6.4C<>	IN	FBC DOS RN<7.0>	1	500HM
7.4A<>	6.3C<>	OUT	FBC DOM<7.0>	1	500HM
	6.1C<>	BI	FBC D<63.0>	1	500HM
6.3G<>	7.4A<>	IN	FBC CMD<25.0>	1	500HM

	NET	VOLTAGE	MAX_CURRENT	MI_N_WI_DTH
7_3D<>	 FBC_VREF0	1.47V	0.02A	12MI L
7_3G<>	 FBC_VREF1	1.47V	0.02A	12MI L
7_3E<>	 FBC_VREF2	1.47V	0.02A	12MI L
7_3H<>	 FBC_VREF3	1.47V	0.02A	12MI L
7_2B<	 FBC_Z00	1.47V	0.02A	12MI L
7_2E<	 FBC_Z01	1.47V	0.02A	12MI L

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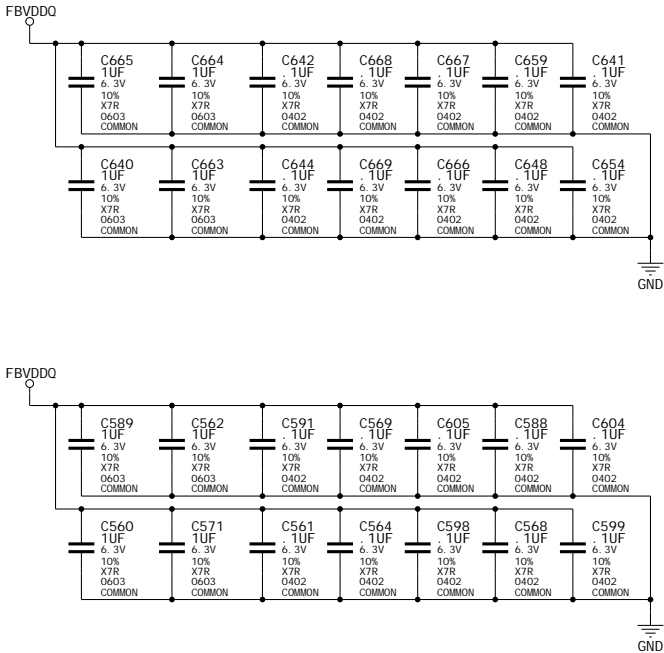
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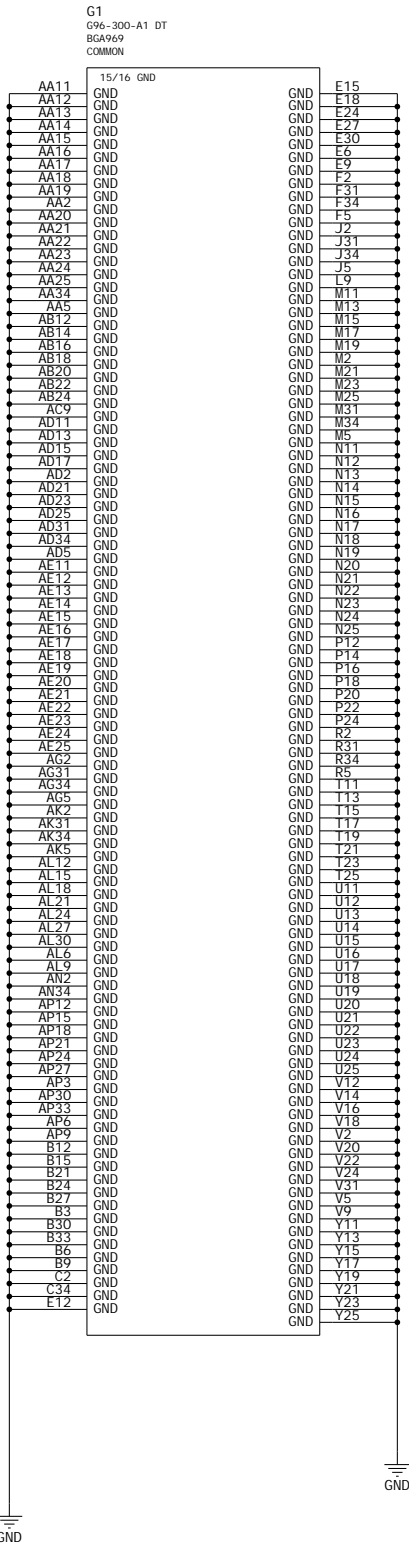
FRAMEBUFFER: PARTITION C DECOUPLING



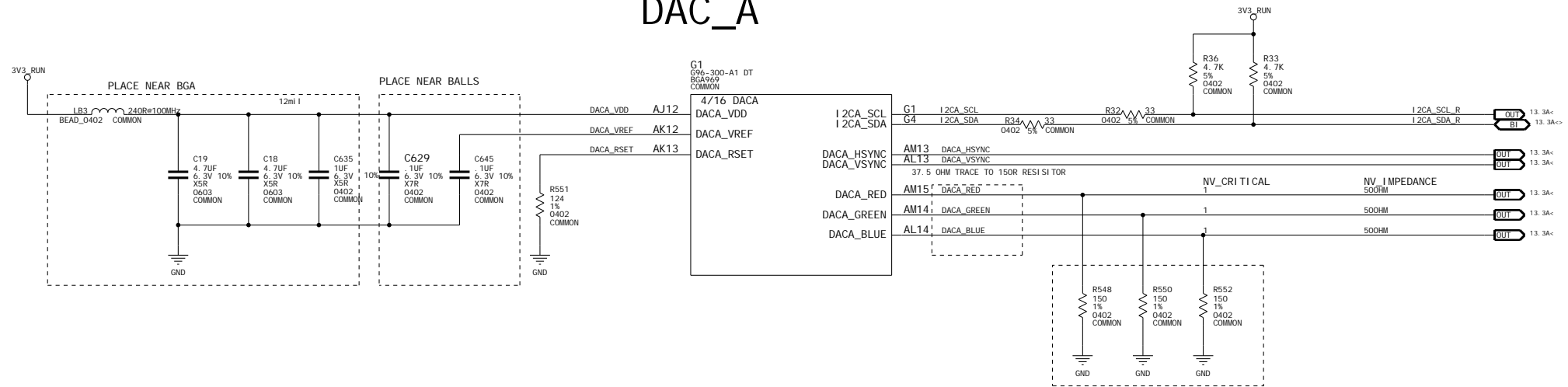
Decoupling for FBC West Side Memory Device.

Decoupling for FBC East Side Memory Device.

NVVDD GROUND

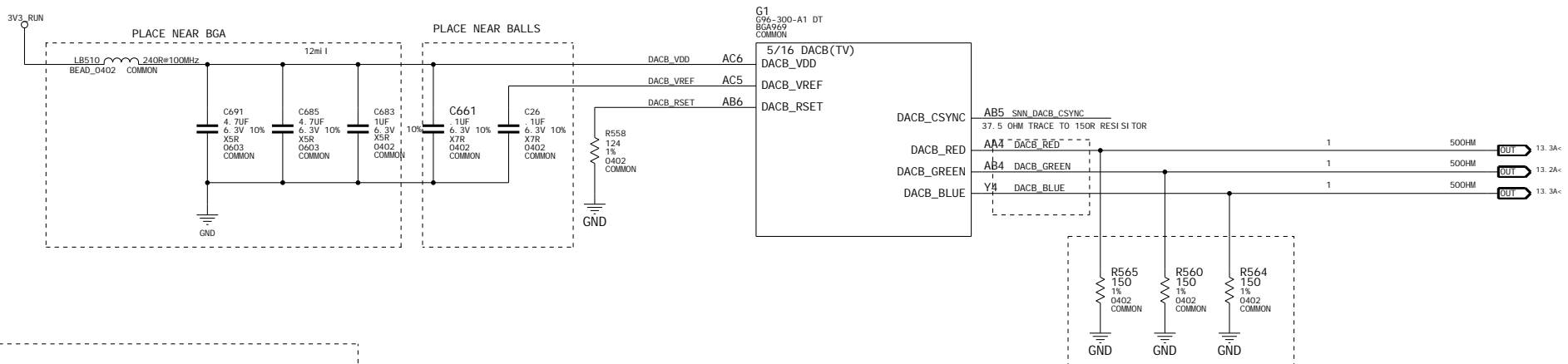


DAC_A



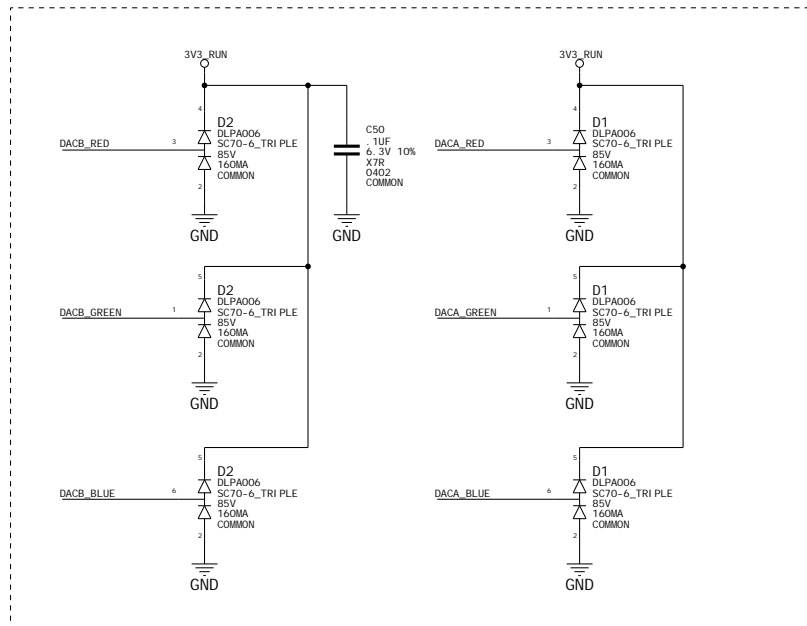
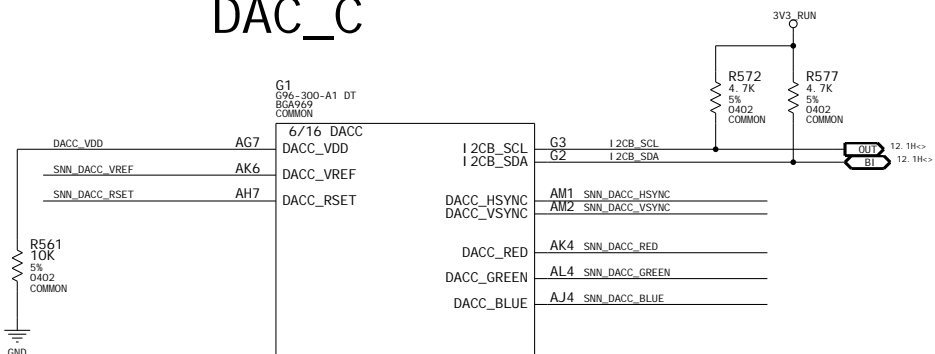
Place close to GPU

DAC_B



Place close to GPU

DAC_C



TV DAC ESD PROTECTION

ASSEMBLY	
PAGE DETAIL	DAC A/B

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Option #1) IFPAB outputs to LVDS only.
 Option #2) IFPAB outputs to DVI-C only.
 Option #3) Controlled with GPIO9, IFPAB dynamically outputs to LVDS or DVI-C.



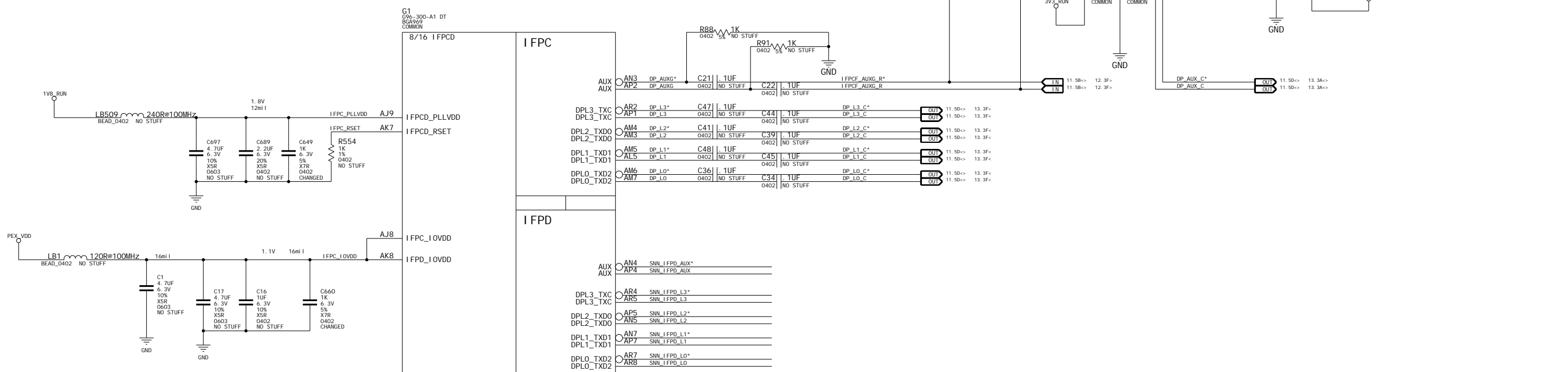
NET NAME	DI_FFPAI R	NV_CRI TI CAL_NET	NV_I MPEDANCE	
I_FPA_TXD0*	I_FPATXD0	1	100DI FF	13.4F%
I_FPA_TXD0	I_FPATXD0	1	100DI FF	10.1H%
I_FPA_TXD1*	I_FPATXD1	1	100DI FF	10.1H%
I_FPA_TXD1	I_FPATXD1	1	100DI FF	13.4F%
I_FPA_TXD2*	I_FPATXD2	1	100DI FF	10.2H%
I_FPA_TXD2	I_FPATXD2	1	100DI FF	13.4F%
I_FPA_TXD3*	I_FPATXD3	1	100DI FF	10.2H%
I_FPA_TXD3	I_FPATXD3	1	100DI FF	13.4F%
I_FPB_TXD4*	I_FPBTXD4	1	100DI FF	10.2H%
I_FPB_TXD4	I_FPBTXD4	1	100DI FF	13.3F%
I_FPB_TXD5*	I_FPBTXD5	1	100DI FF	13.4F%
I_FPB_TXD5	I_FPBTXD5	1	100DI FF	10.2H%
I_FPB_TXD6*	I_FPBTXD6	1	100DI FF	13.4F%
I_FPB_TXD6	I_FPBTXD6	1	100DI FF	10.2H%
I_FPB_TXD7*	I_FPBTXD7	1	100DI FF	10.2H%
I_FPB_TXD7	I_FPBTXD7	1	100DI FF	13.4F%
I_FPA_TXC*	I_FPATXC	1	100DI FF	10.1H%
I_FPA_TXC	I_FPATXC	1	100DI FF	13.4F%
I_FPB_TXC*	I_FPBTXC	1	100DI FF	10.2H%
I_FPB_TXC	I_FPBTXC	1	100DI FF	13.4F%

10. 2H>	13. 3F>
10. 2H>	13. 4F>
10. 3H>	13. 4F>
10. 1H>	13. 4F>
10. 2H>	13. 4F>

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DISPLAY PORT DP-B (Link C)



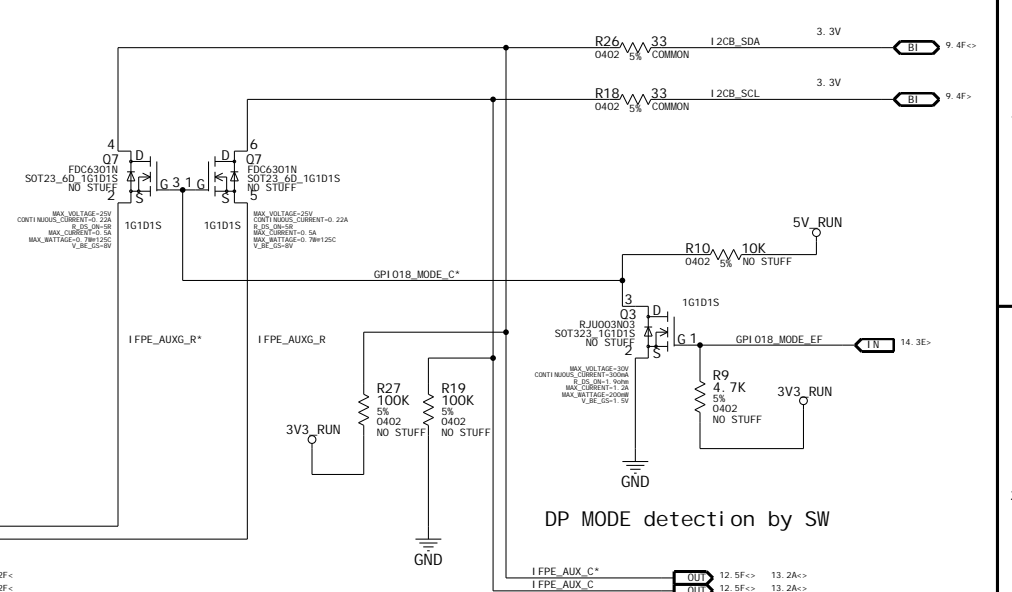
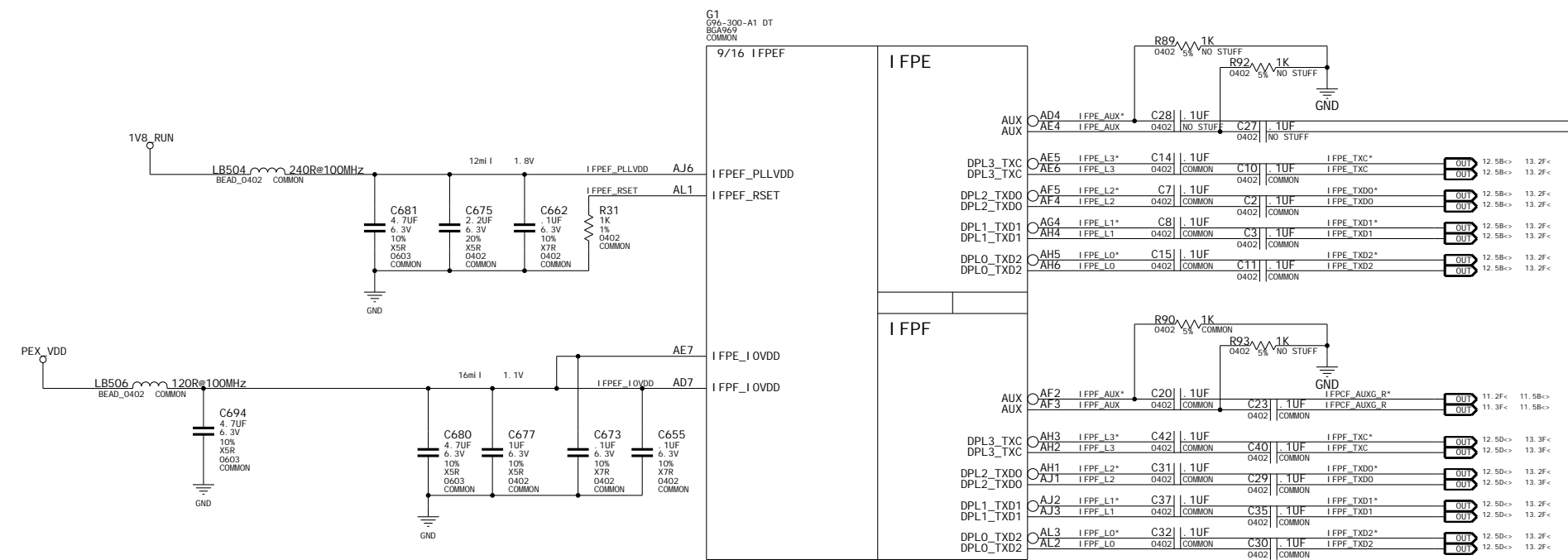
(DP CONSTRAINTS)

[illegible]

ASSEMBLY	NB9P-GS G96M, 800MHz 512MB(128bit) GDDR3 32Mx32 136FBGA, LVDS + DP-A + DVI -A + SD/HD(TV_OUT) + VGA
PAGE DETAIL	DISPLAY PORT DP-B (LINK C)

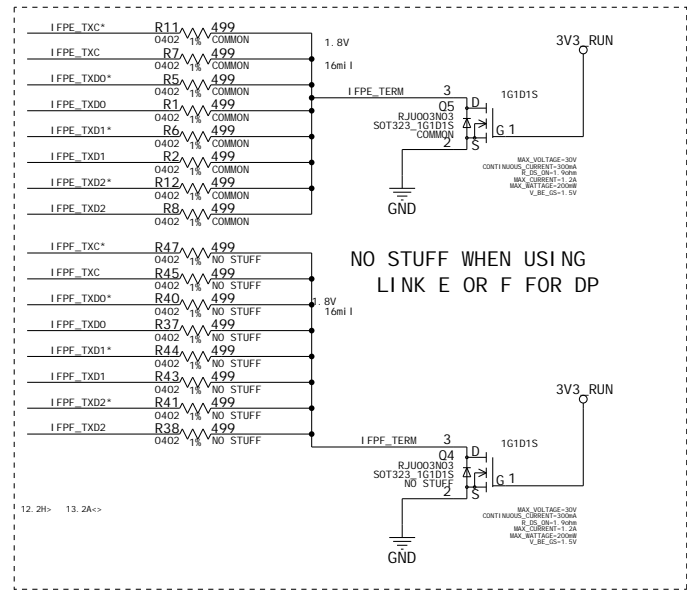
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DVI -A HDMI (LINK E)
OPTIONAL DP-C FOR OEM SPECIAL SKU



Li nkE/F B I A S

DISPLAY PORT DP-A (LINK F)
OPTIONAL DVI -B TMDS SL OR DL W/ DVI -A



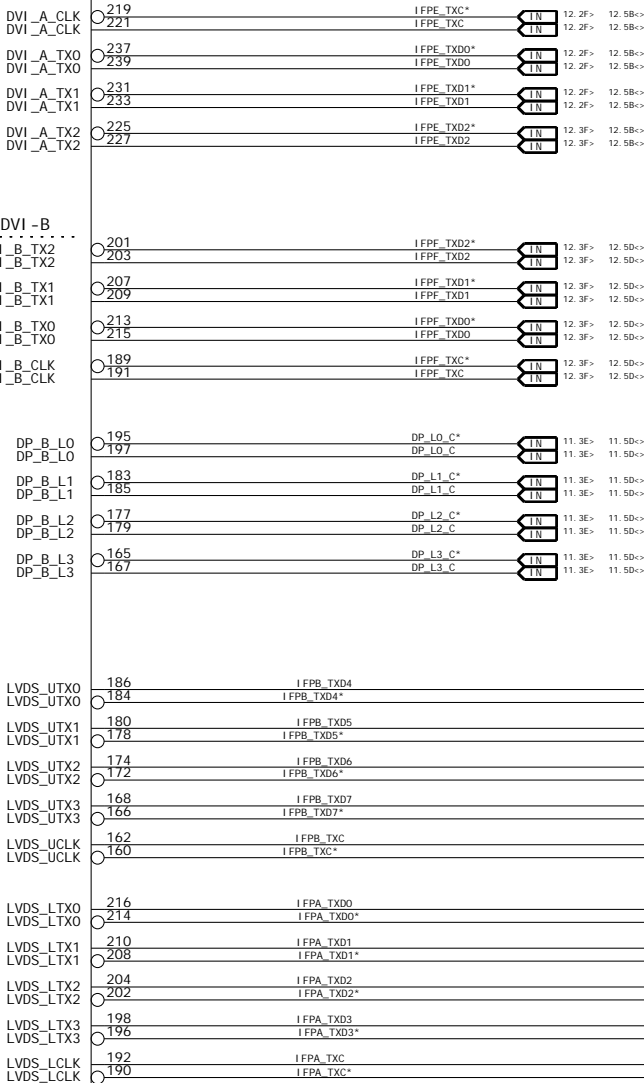
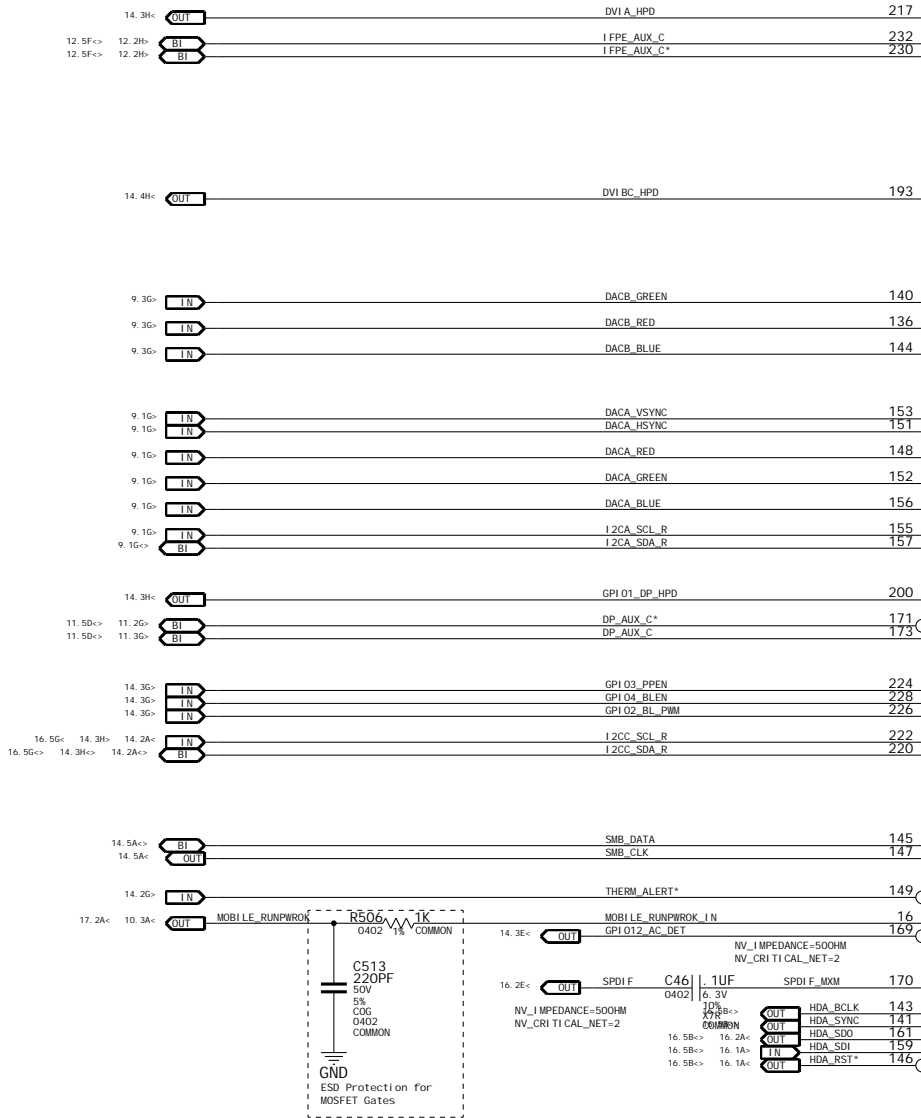
(TMDS/HDMI /DP OPTI ON CONSTRAI NTS)

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I FPE_L3*	I FPE_L3	1	100DI FF	I FPF_L3*	I FPF_L3	1	100DI FF	I FPF_AUX*	I FPF_AUX	1	100DI FF
I FPE_L3	I FPE_L3	1	100DI FF	I FPF_L3	I FPF_L3	1	100DI FF	I FPF_AUX	I FPF_AUX	1	100DI FF
I FPE_L2*	I FPE_L2	1	100DI FF	I FPF_L2*	I FPF_L2	1	100DI FF	I FPF_AUX*_R	I FPF_AUX*_R	1	100DI FF
I FPE_L2	I FPE_L2	1	100DI FF	I FPF_L2	I FPF_L2	1	100DI FF	I FPF_AUX*_R	I FPF_AUX*_R	1	100DI FF
I FPE_L1*	I FPE_L1	1	100DI FF	I FPF_L1*	I FPF_L1	1	100DI FF	I FPF_AUX_C*	I FPF_AUX_C	1	100DI FF
I FPE_L1	I FPE_L1	1	100DI FF	I FPF_L1	I FPF_L1	1	100DI FF	I FPF_AUX_C	I FPF_AUX_C	1	100DI FF
I FPE_LO*	I FPE_LO	1	100DI FF	I FPF_LO*	I FPF_LO	1	100DI FF	I FPF_AUX	I FPF_AUX	1	100DI FF
I FPE_LO	I FPE_LO	1	100DI FF	I FPF_LO	I FPF_LO	1	100DI FF	I FPF_AUX	I FPF_AUX	1	100DI FF
I FPE_TXC*	I FPE_TXC	1	100DI FF	I FPF_TXC*	I FPF_TXC	1	100DI FF	I FPF_AUX*	I FPF_AUX	1	100DI FF
I FPE_TXC	I FPE_TXC	1	100DI FF	I FPF_TXC	I FPF_TXC	1	100DI FF	I FPF_AUX	I FPF_AUX	1	100DI FF
I FPE_TXD0*	I FPE_TXD0	1	100DI FF	I FPF_TXD0*	I FPF_TXD0	1	100DI FF	I FPF_AUX*	I FPF_AUX	1	100DI FF
I FPE_TXD0	I FPE_TXD0	1	100DI FF	I FPF_TXD0	I FPF_TXD0	1	100DI FF	I FPF_AUX	I FPF_AUX	1	100DI FF
I FPE_TXD1*	I FPE_TXD1	1	100DI FF	I FPF_TXD1*	I FPF_TXD1	1	100DI FF	I FPF_AUX*	I FPF_AUX	1	100DI FF
I FPE_TXD1	I FPE_TXD1	1	100DI FF	I FPF_TXD1	I FPF_TXD1	1	100DI FF	I FPF_AUX	I FPF_AUX	1	100DI FF
I FPE_TXD2*	I FPE_TXD2	1	100DI FF	I FPF_TXD2*	I FPF_TXD2	1	100DI FF	I FPF_AUX*	I FPF_AUX	1	100DI FF
I FPE_TXD2	I FPE_TXD2	1	100DI FF	I FPF_TXD2	I FPF_TXD2	1	100DI FF	I FPF_AUX	I FPF_AUX	1	100DI FF

MXM CONNECTOR

CN1
CON_MXM_X16_EDGE
(NON)PHY (-X16, -HE)
NONPHY-X16
COMMON

2/2 I/O - LVDS, DVI, DP, VGA, TV



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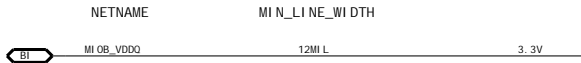


ASSEMBLY	NB9P-GS G96M, 800MHz 512MB(128bit) GDDR3 32Mx32 136FBGA, LVDS + DP-A + DVI-A + SD/HD(TV_OUT) + VGA
PAGE DETAIL	MXM CONNECTOR

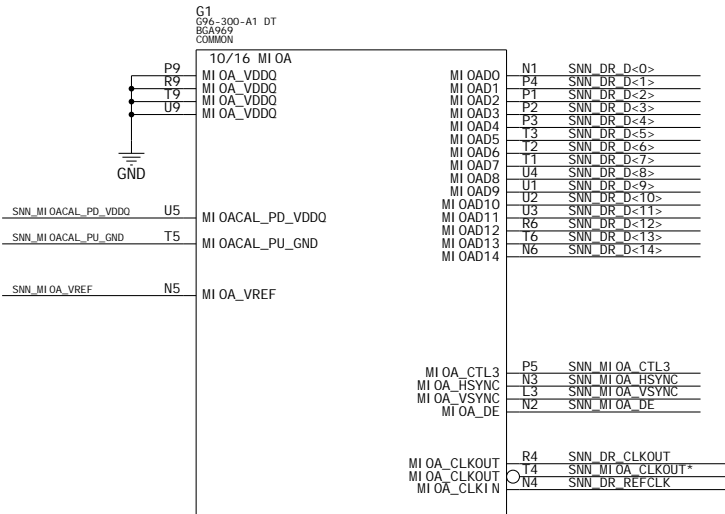
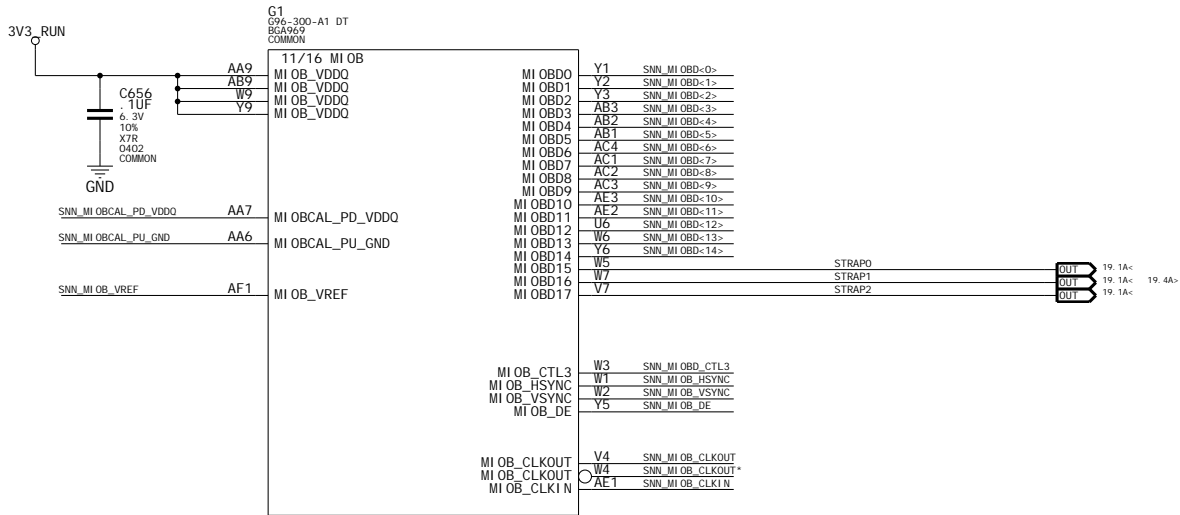
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





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[illegible]

NV_CRI TI CAL_NET		NV_I MPEDANCE	
HDA1_SDI	2	560HM	
HDA_BCLK	2	560HM	 13.4C> 16.1A<
HDA_SYNC	2	560HM	 13.4C> 16.2A<
HDA_SDI	2	560HM	 13.4C> 16.1A>
HDA_SDO	2	560HM	 13.4C> 16.2A<
HDA_RST*	2	560HM	 13.4C> 16.1A<

ASSEMBLY	NB9P-GS G96M, 800MHz 512MB(128bi t) GDDR3 32Mx32 136FBGA, LVDS + DP-A + DVI -A + SD/HD(TV_OUT) + VGA
PAGE DETAIL	VB10S, HDCP/12C ROM, XTAL, SPREAD SPECTRUM, HD AUDIO

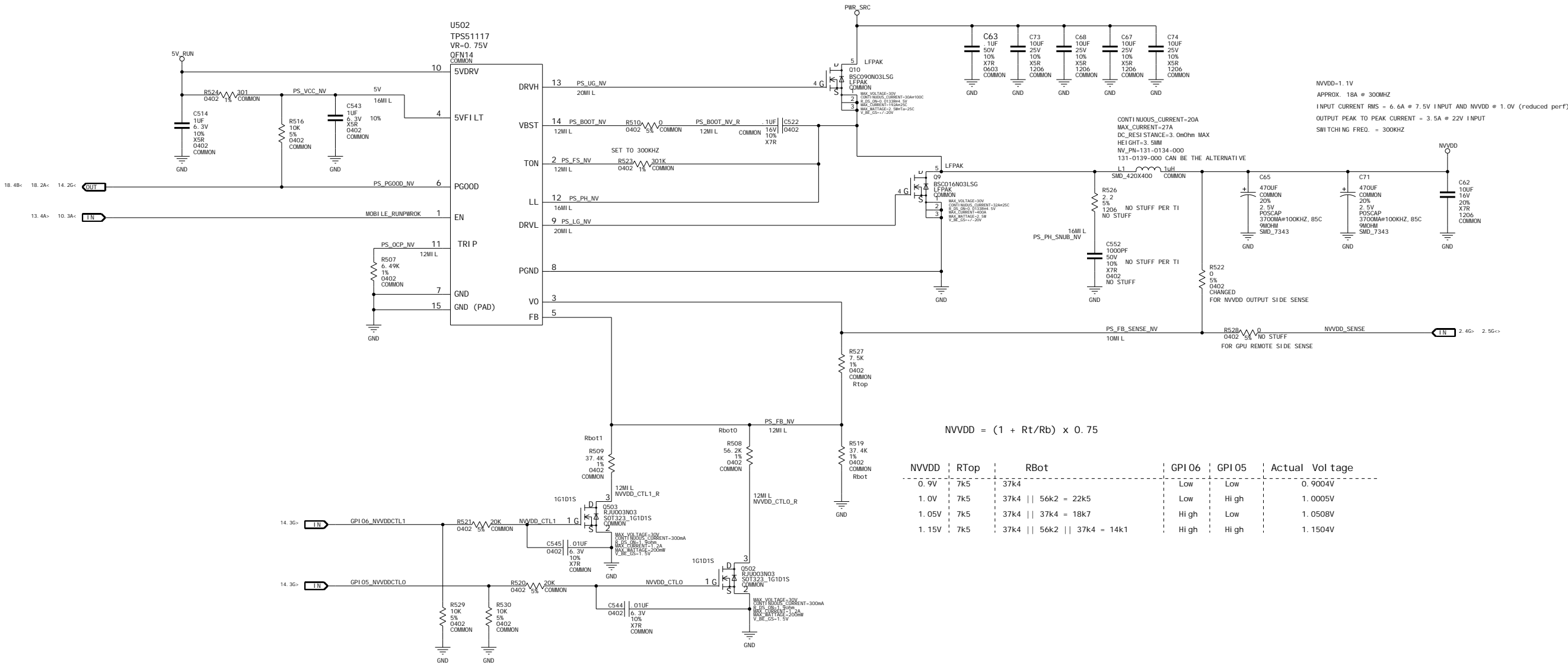
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NVVDD POWER SUPPLY

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
NVVDD	1V	12MIL	18A

NVVDD SWITCHER POWER SUPPLY



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ASSEMBLY	NB9P-GS G96M, 800MHz 512MB(128bit) GDDR3 32Mx32 136FBGA, LVDS + DP-A + DVI-A + SD/HD(TV_OUT) + VGA
PAGE DETAIL	NVVDD POWER SUPPLY

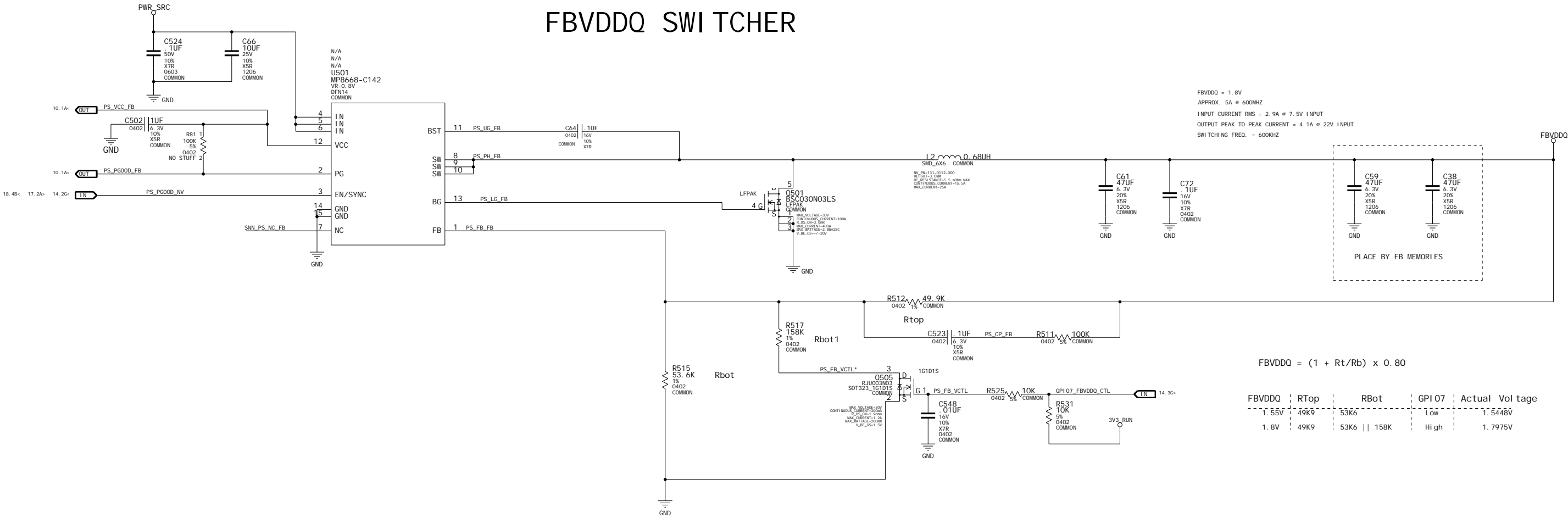
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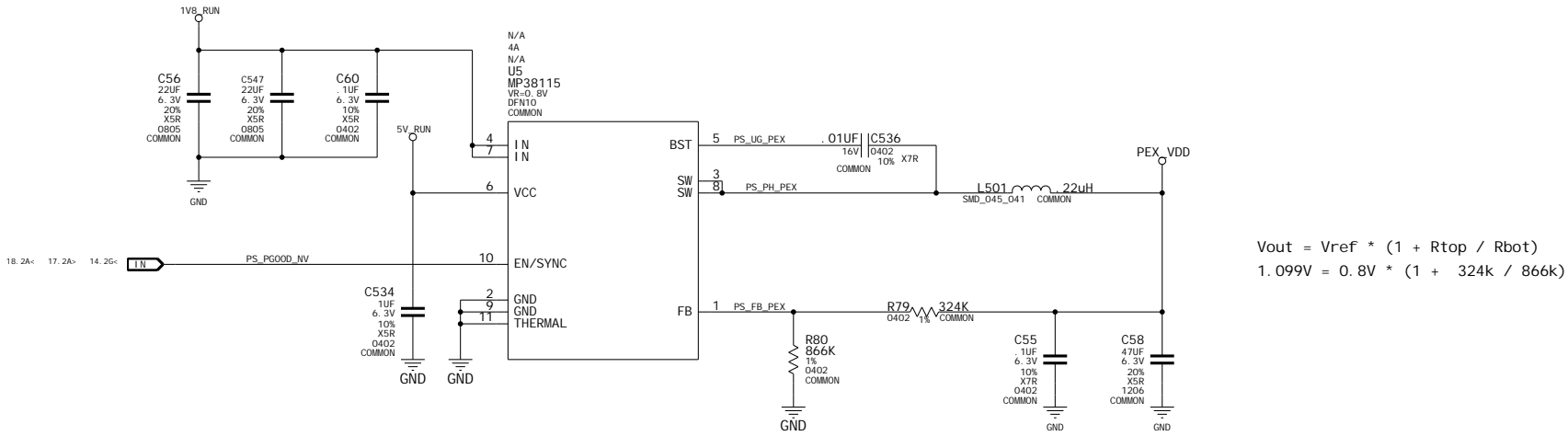
FBVDDQ AND PEX_VDD POWER SUPPLY

NET	VOLTAGE	NV_NET_MAX_CURRENT
PEX_VDD	1.1V	4A
FBVDDQ	1.8V	5A

FBVDDQ SWITCHER



PEX_VDD SWITCHER



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ASSEMBLY

NB9P-GS G96M, 800MHz 512MB(128bit) GDDR3 32Mx32 136FBGA, LVDS + DP-A + DVI-A + SD/HD(TV_OUT) + VGA

PAGE DETAIL

FBVDDQ AND PEX_VDD POWER SUPPLY

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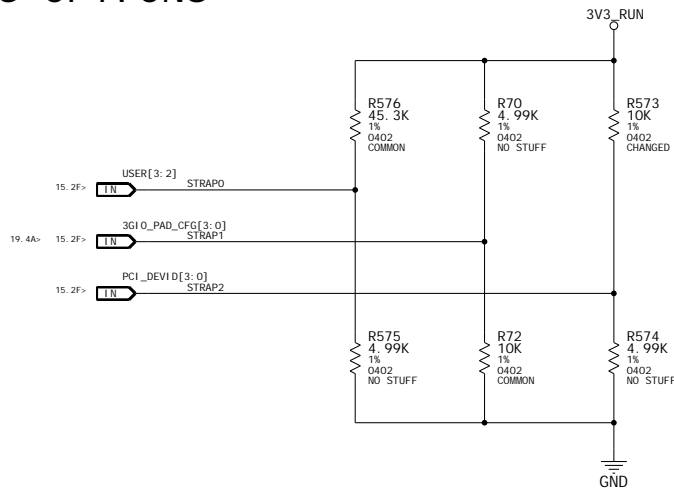
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DATE

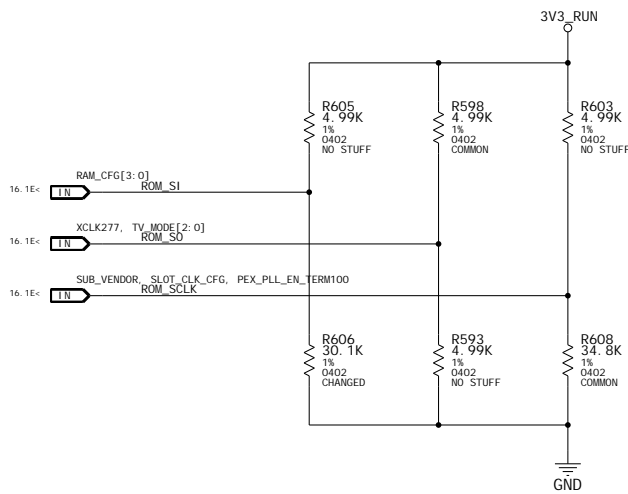
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STRAPPING OPTIONS



	3V3	GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



STRAP0

USER_BI T0 0xF: 45K PU (unused)

USER_BI T1

USER_BI T2

USER_BI T3

STRAP1

3GIO_PADCFG_LUT_ADR0

3GIO_PADCFG_LUT_ADR1

0x0: Desktop default t (normal swing) - 5k PD

3GIO_PADCFG_LUT_ADR2

0x1: Mobile default t (low swing) - 10k PD

3GIO_PADCFG_LUT_ADR3

acc. to //hw/tesla_g98b/manual s/dev_ext_devices.ref

STRAP2

PCI_DEVID_0

all 4 bits set by HW strapping

PCI_DEVID_1

0x0649: 10K PU (NB9P-GS)

PCI_DEVID_2

0x0648: 5K PU (NB9P-GE2)

PCI_DEVID_3

0x065C: 25K PU (NB9P-GLM2)

ROM_S0

TV_MODE_BI T0

0x0: NTSC-M

TV_MODE_BI T1

5K PU

TV_MODE_BI T2

XCLK_277

1: PCI-E GEN2

ROM_S1

RAM_CFG_0 256 MB (4pcs. 16Mx32)

512 MB (4pcs. 32Mx32)

RAM_CFG_1 RAM_CFG[3:0] Defini ti ons

RAM_CFG[3:0] Defini ti ons

RAM_CFG_2 0000 Reserved

0100 25k PD Reserved

RAM_CFG_3 0001 Dimonda

0101 30k PD Dimonda

PEX_PLL_EN_TERM100

0:

SLOT_CLK_CONFIG

1: GPU/MCH SHARE COM REF CLK

35K PD

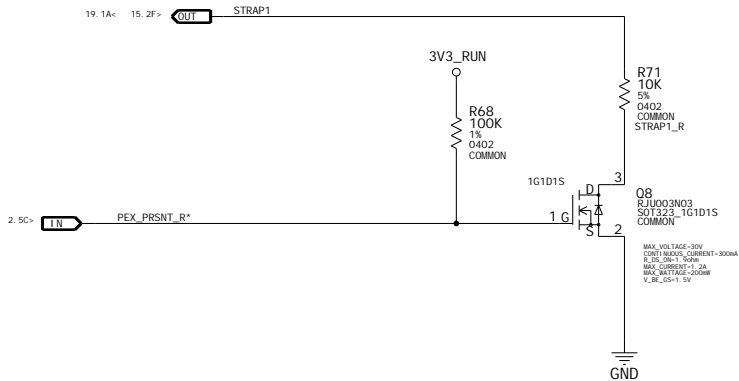
SUB_VENDOR

1: SUB_VENDOR BIOS

PCI_DEVID_EXT

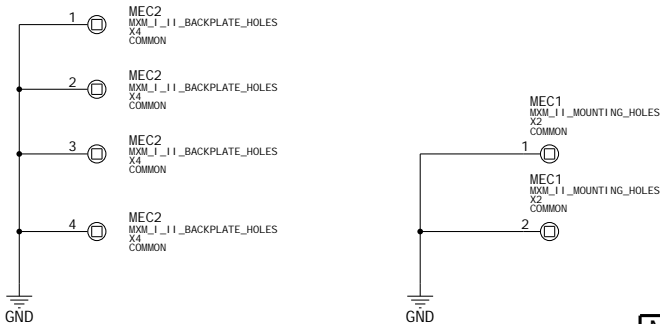
0: TERM100 DISABLED

PEX SWING LEVEL



PEX_PRSENT2_R	R_STRAP1	3_GI O_PADCFG_LUT<3. . 0>
GND	10k	0x1 MOBI LE_DEFAULT
FLOAT	5k (10k 10k)	0x0 DESKTOP_DEFAULT

MECHANI CAL



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