
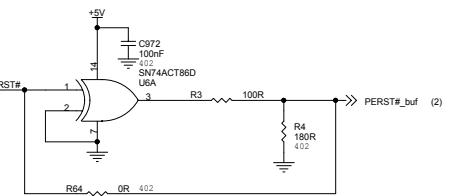
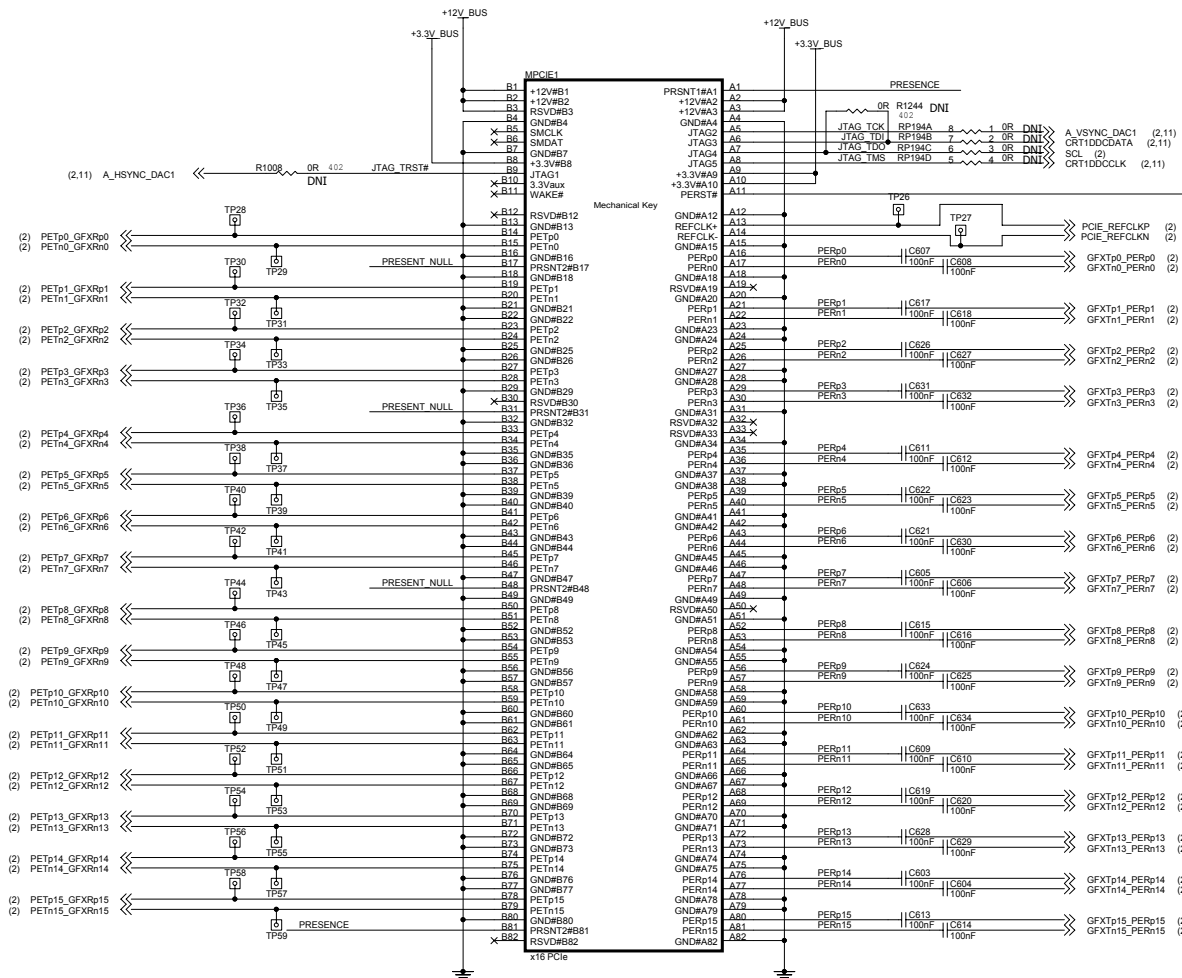




Variant Name>		5	4	3	2	1
		Title PCI-E RV370 128M TSOP VO-SV/DI			Schematic No. 105-A260xx-00	Date: Friday, April 30, 2004
REVISION HISTORY						Rev 5
Sch Rev	Date	REVISION DESCRIPTION				
0 00A	2003-09-10	<p>PRELIMINARY BASED ON 105-A181xx-00A and 105-A200xx-00</p> <ul style="list-style-type: none">- Use 402 R and C footprints as preferred- (pg1) Add 0R bypass for PERST#, and use XOR spared gate for buffer- (pg1) Keep only 1 100uF decoupling for +12V_BUS- (pg1) Connect B3 of edge connector directly to +12V_BUS- (pg2) Remove oscillator and change crystal to surface mount- (pg2) Hard pull-down on TEST_Y/MCLK- (pg2) Remove thermal interrupt, no provision for speed controlled fan- (pg2) Remove redundant TPs- (pg2) Pull-up on DVPCNTL_[3:0], remove RageTheater capture ports (VID/DVO[7:0])- (pg2) DVOMode pull-up to 1.8V, set to 12-bit DVO (1.8V DVO I/O signalling)- (pg3) Memory interface based on A198, remove Channel B- (pg4) Remove power-up diodes- (pg5, 6, 7) Redesigned power regulators- (pg8, 9) Channel A only Series-Terminated TSOP interface (based on A200)- (pg11, 12, 13) Front-end based on Low-Profile VGA/DVI + VO design (based on A200)				
	2003-09-22	<ul style="list-style-type: none">- (pg5) Add RC snubber circuit on switching regulator- (pg7) Add R124 for power dissipation				
	2003-10-16	<ul style="list-style-type: none">- (pg14) Add MT2, second mounting hole- (pg6 and 7) Remove R817, option for sharing REG8 and REG9, due to layout concerns- (pg4) Add C979..C985 On request of EMI team. These are for decoupling adjacent planes.- (pg6) Make RP2 dual footprint with 0402 Caps C986..C989. Created a similar circuit using RP195 and C990..C993. The RP can be used to short +MVDDQ and +MVDDC, and the caps can be used to decouple the planes.- (pg6) Add C973..C978 Decoupling caps. These are placed accross +MVDDQ/+MVDDC plane splits- (pg11) Remove R994..R996 stitching GND to Chassis GND.				
1 00B	2003/11/14	<ul style="list-style-type: none">- (Layout) Change to 6-layer PCB- (Layout) Change PCIE test points- (pg1) Change PCIE test points, add 3.3V_BUS polymer cap, add R1244- (pg2) Add R23 for DVO pull-down- (pg4) Add B15 for +3.3V_BUS VDDR4 alternate, change PCIE regulators filter from 100nF to 1uF- (pg5) Add stand-alone +PCIE_VDDR, +PCIE_PVDD12 and +PCIE_PVDD18 regulators, improve power sequence circuit- (pg5) Add R315 and R316 to Select +12V_BUS or +5V for boot circuit, change R368 footprint to 603- (pg6) Add C314 and C315 for MVDDC and MVDDQ, 1.8V from PCIE_PVDD18- (pg7) Remove R124, add polymer cap for PCIE_PVDD18, add +PCIE_VDDR and +PCIE_PVDD12 tied option and single package FET for +PCIE_VDDR- (pg14) Add fan connector				
2 00C	2004/03/05	<ul style="list-style-type: none">- (pg02, 10) Fix pull-up +VDD_DVO to +VDDR4- (Layout) TVO filters move close to connector- (pg04) Remove CP2, 3, 4, 5, 6 and 8 for dual footprint manufacturing issues (Capacitor packs sharing with 402 footprints)- (Layout) Components using the same foot print. (remove MC2)- (pg06) Remove C986, C987, C988, C989, C990, C991, C992 and C993- (pg06) Add C800 for options- (pg11) +5V supply with current limiting for VESA DDC spec, remove F1, B21- (pg05) Remove dual-packaged MOSFET- (Layout/EMI) C507, C508, C509, R513, R514, R515 (added), L60, L61 and L62 connect to digital Gnd instead of chassis Gnd.				
3 00E	2004/04/16	<ul style="list-style-type: none">- (pg04) Remove redudant dual-footprint capacitor array- (pg11) Add R994, extra resistor to tide chassis/digital ground- (pg12) Add R916 and R917 for +5V_VESA resistor dissipation to meet 70% derating spec- (pg13) Remove R513 and R514 and tide TVO MiniDIN shield directly to chassis ground				
4 00D	2004/04/16	<ul style="list-style-type: none">- (pg11, 12, 13 and 14) Change chassis ground to digital ground- (pg11) Remove R991, R992, R993, R994, R997, R998 and R999 for chassis/digital ground tide- (pg12) Change DVI-I connector to fully-shielded connector- (pg14) Remove Mounting Hole MT2- (Layout) Remove TMDS ground guards				
5 00	2004/04/27	<p>Released based on -00D PCB (not -00E)</p> <ul style="list-style-type: none">- (pg05) Tide R357 to +3.3V instead of +12V for proper power sequence				
		5	4	3	2	1

Three circuit diagrams illustrating decoupling capacitor connections for different power supplies:

- +12V BUS:** A capacitor labeled C5 (100uF, 16V) is connected between the +12V BUS and DNI.
- +3.3V BUS:** A capacitor labeled C8 (100uF, 16V) is connected between the +3.3V BUS and DNI. A note below the capacitor indicates $\geq 6.3V$.
- +3.3V BUS:** A capacitor labeled C2 (47uF, 16V) is connected between the +3.3V BUS and DNI. A note below the capacitor indicates $\geq 6.5V$.

USE 47uF TANTALUM CAPACITOR OR HIGHER

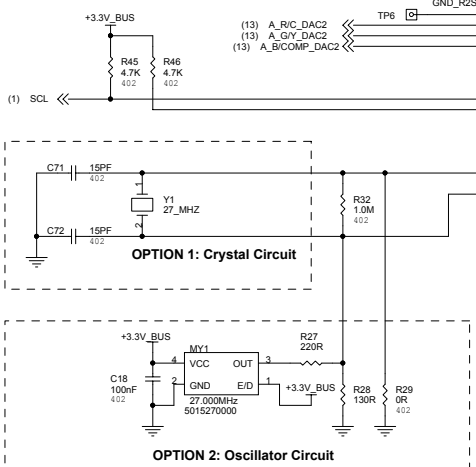
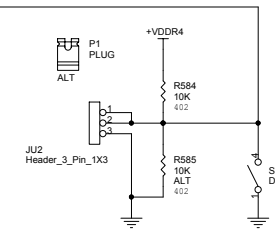
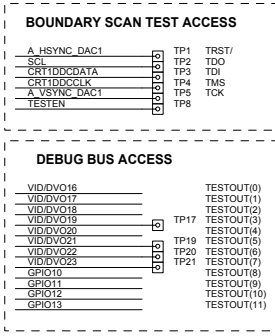
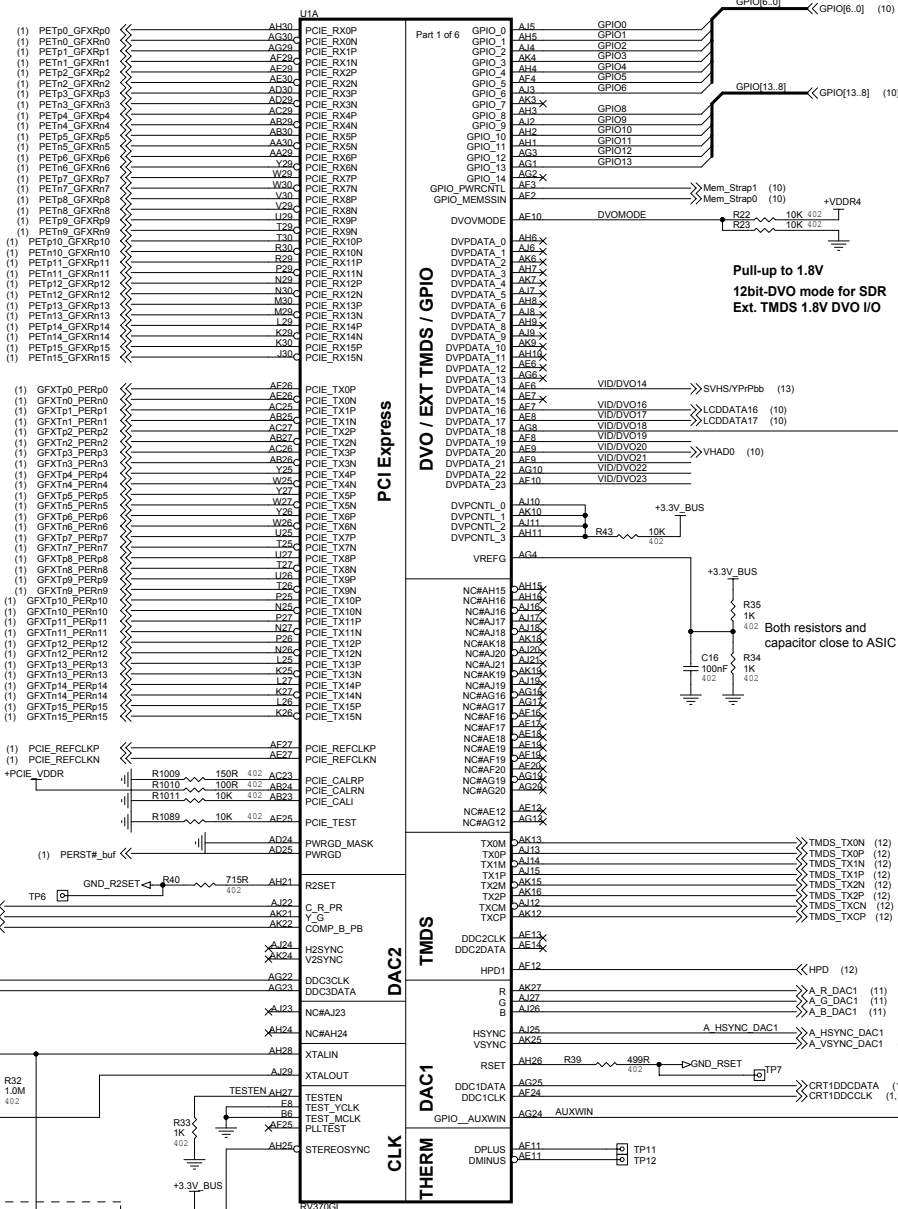


SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

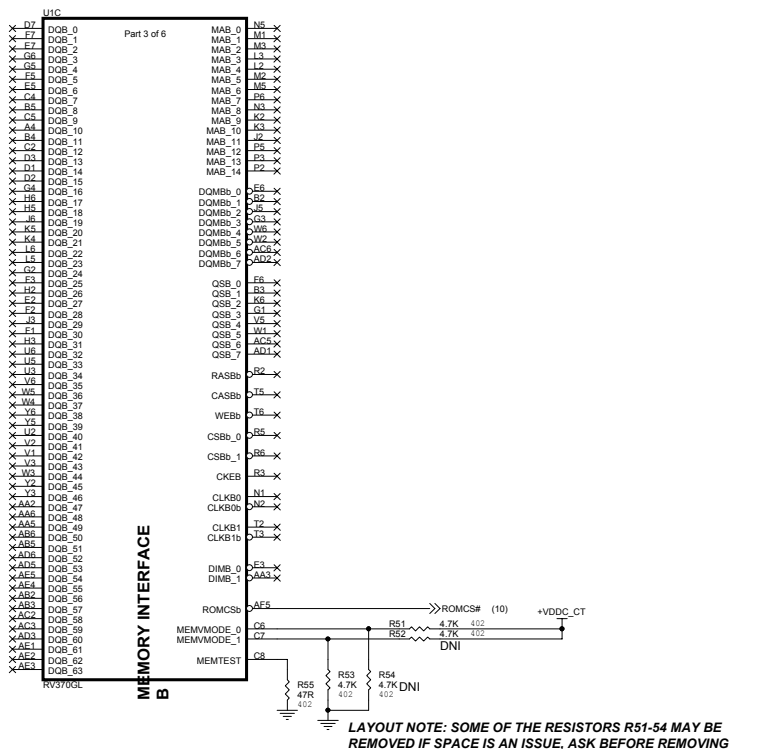
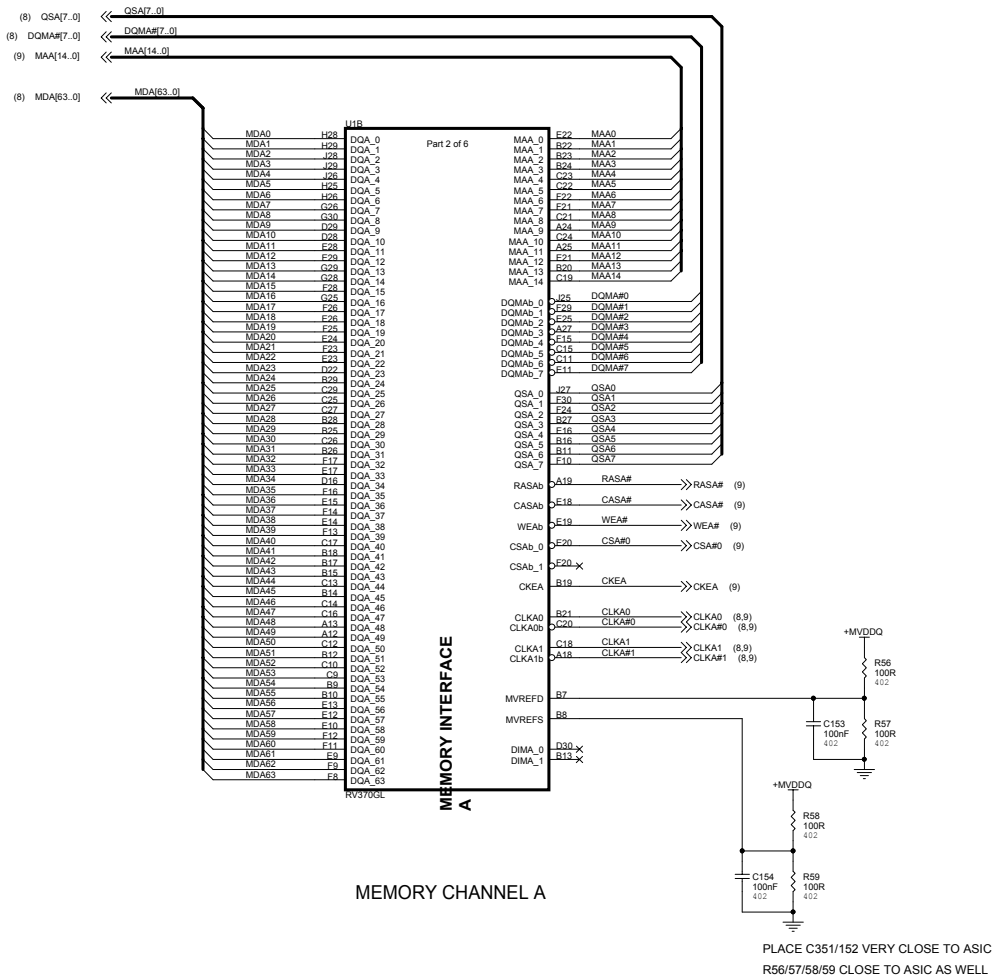


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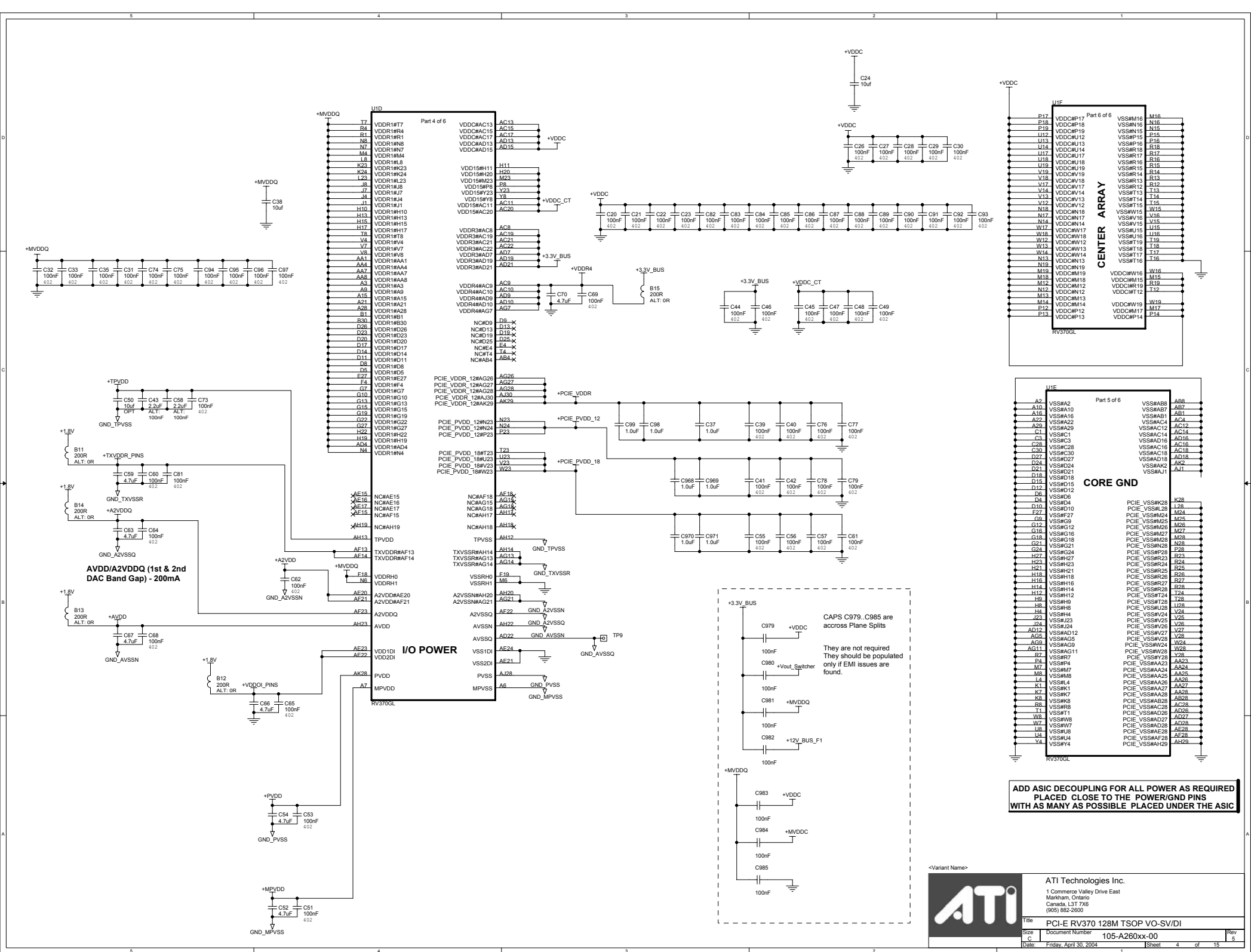
Title		PCI-E RV370 128M TSOP VO-SV/DI	
Size C	Document Number		105-A260xx-00
Date:	Friday, April 30, 2004	Sheet	1 of 15



IT IS RECOMMENDED TO ALLOW SERIES RESISTOR FOOT PRINTS ON THE INDICATED AGIP CONTROL SIGNALS TO ADDRESS ANY LAYOUT NOISE RELATED SIGNAL DAMPING REQUIREMENTS



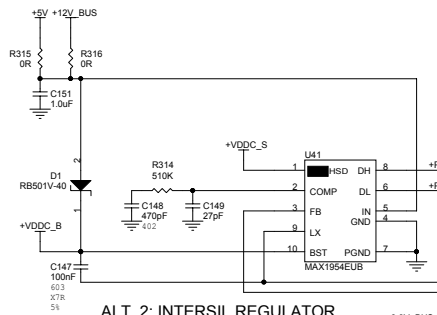
VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT



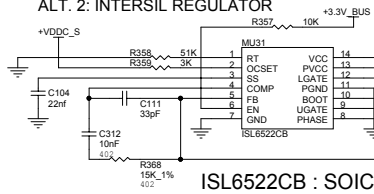
Regulator for VDDC (ASIC Core)

Vout = 1.2V ~ 1.3V

ALT. 1: MAXIM REGULATOR

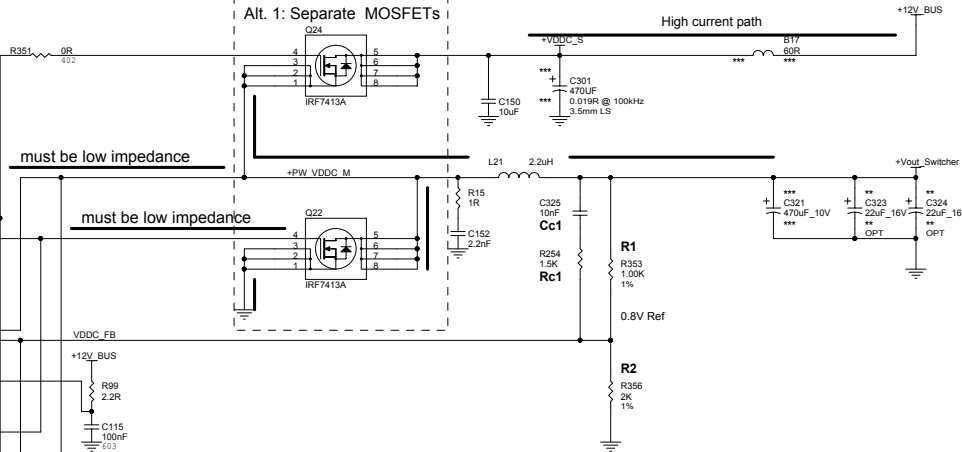


ALT. 2: INTERSIL REGULATOR



ISL6522CB : SOIC

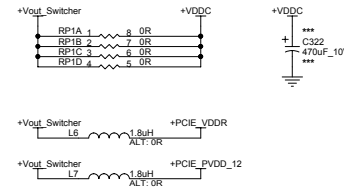
Alt. 1: Separate MOSFETs



must be low impedance

must be low impedance

High current path



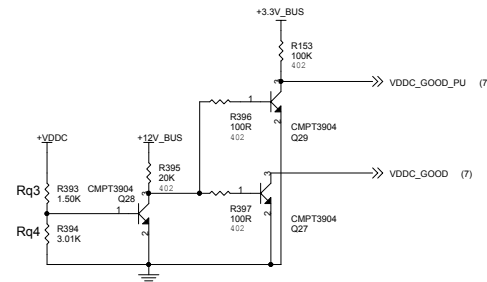
*** Indicate number of power via required for the connection

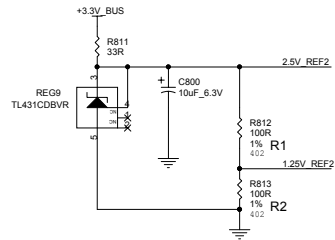
Part	NOTES
MAX1954	Do not install Cc1, Rc1
ISL6522	Install Cc1, Rc1

Part	Vout	R1	R2
MAX1954	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
ISL6522	0.8V Ref	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100

Circuit to hold PCI-E voltage low and wait for +VDDC for proper power sequence

+VDDC	Rq3	Rq4
+1.3V	1.5K	2.4K
+1.2V	1.5K	3K

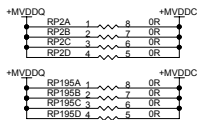




Voltage Req.	R1	R2
0.8V	150R P/N 3160150000 402	71.5R P/N 324075R500
1.25V	100R P/N 3160100000 402	100R P/N 3160100000 402
1.5V	100R P/N 3160100000 402	150R P/N 3160150000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240015200

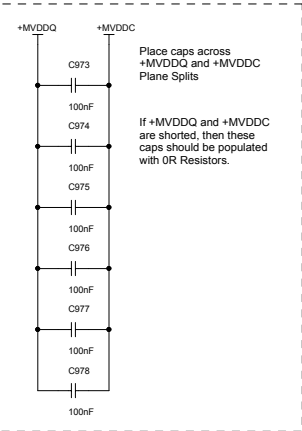
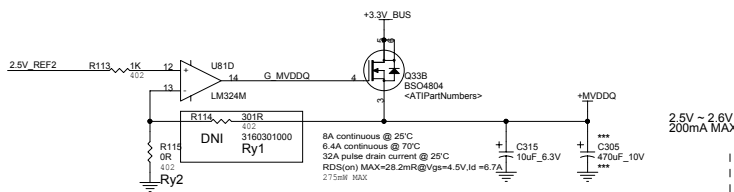
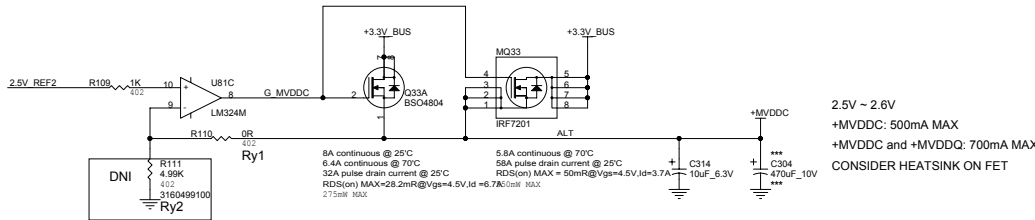
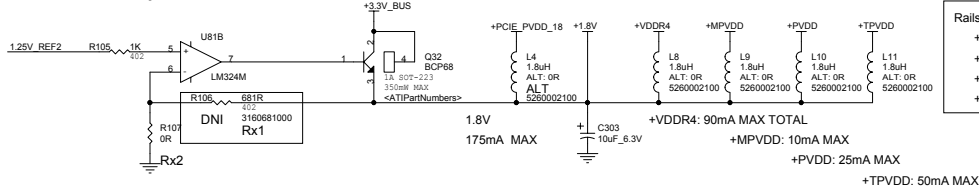
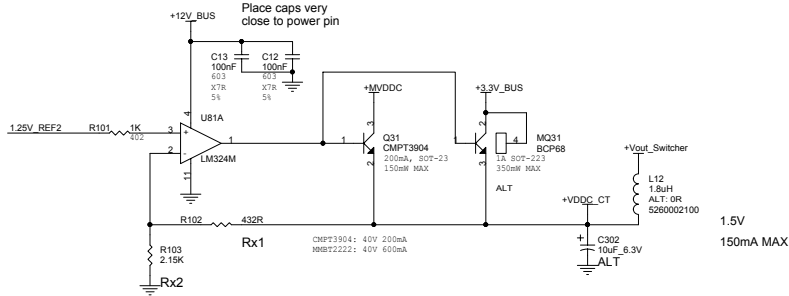
Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.61V	221R (402, 1%) P/N 3160221000	4.99K (402, 1%) P/N 3160499100
2.5V	OR P/N 3230000000 603 P/N 3150000000 402	DNI



Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX

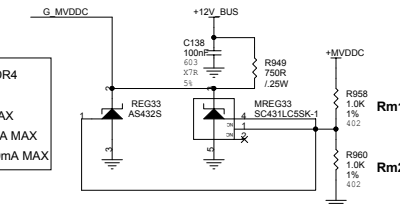
Alt. regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX

Alt. regulator for +TPVDD
Vout = 1.65V ~ 1.85V
Iout = 20mA MAX



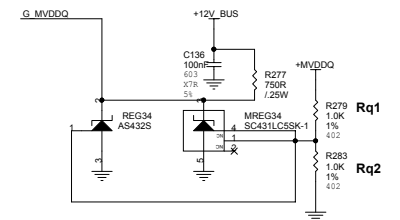
Alt. regulator for +MVDDC
Vout = 2.5V ~ 2.6V
Iout = 500mA MAX

Voltage Req.	Rm1	Rm2
3.34V [-0.04V/+0.04V]	4.32K	2.55K
3.45V [-0.04V/+0.04V]	4.32K	2.43K
2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100

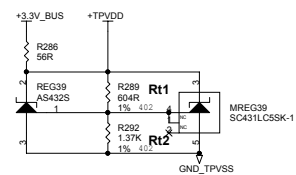
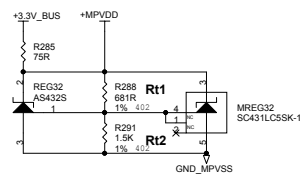
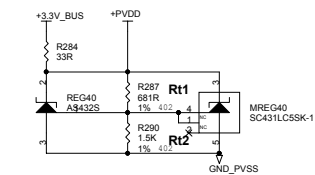
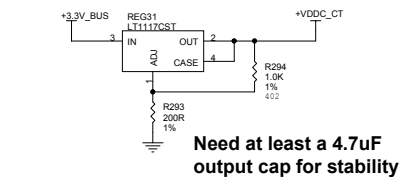


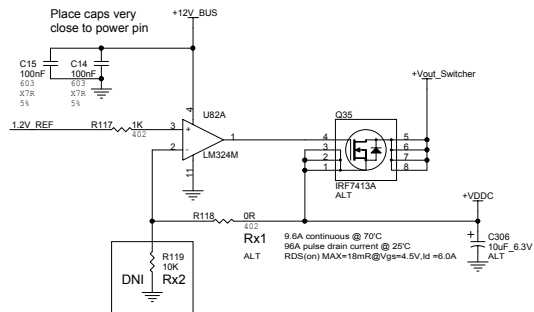
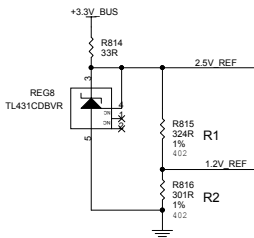
Alt regulator for +MVDDQ
Vout = 2.5V ~ 2.6V
Iout = 200mA MAX

Voltage Req.	Rq1	Rq2
1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
2.5V	1K 3240100100	1K 3240100100
2.6V	4.75K 3240475100	4.32K 3240432100

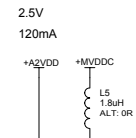


Alt regulator for +VDDC_CT
Vout = 1.5V
Iout = 150mA MAX

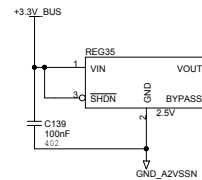




1.3V
8A MAX
MIGHT NEED HEATSINK ON FET

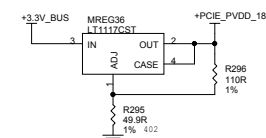


Alt. regulator for +A2VDD
Vout = 2.5V
Iout = 120mA MAX



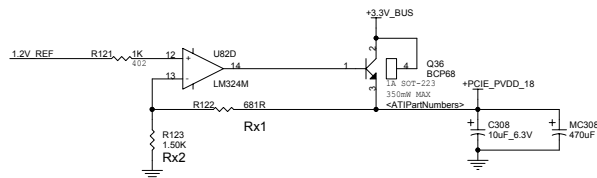
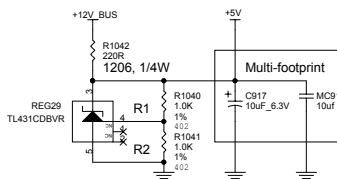
+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.

Alt. regulator for PCIE_PVDD_18
Vout = 1.82V
Iout = 500mA MAX



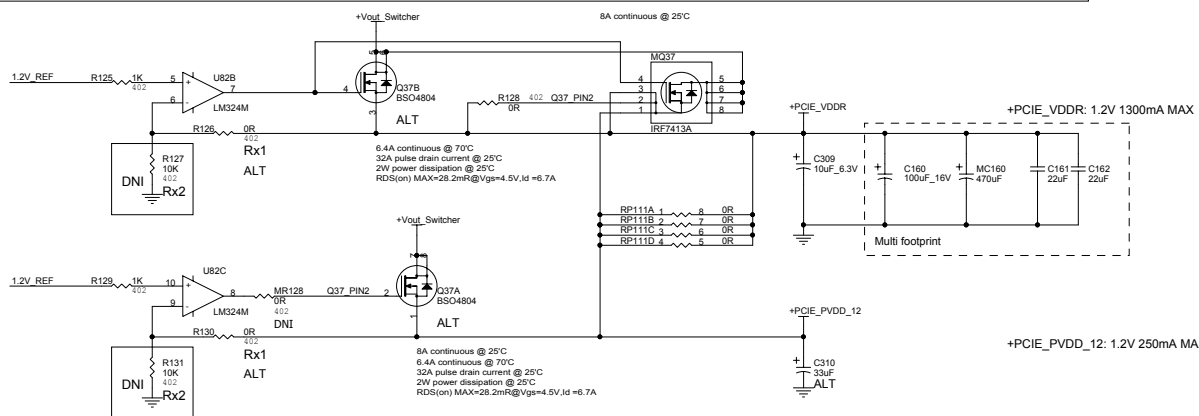
Need at least a 10uF Tant. output cap for stability
Min. Load Current: 10mA

Regulator for +5V
Vout = 5V
Iout = 20mA MAX

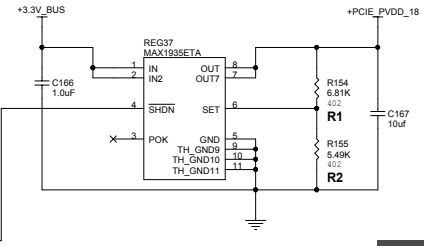
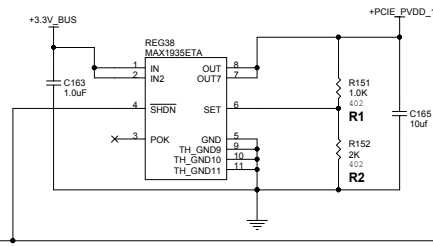
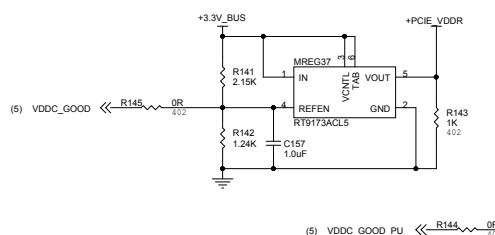


+PCIE_PVDD_18: 1.8V 500mA MAX

Optional when +Vout_Switcher is above 1.2V



+PCIE_PVDD_12: 1.2V 250mA MAX

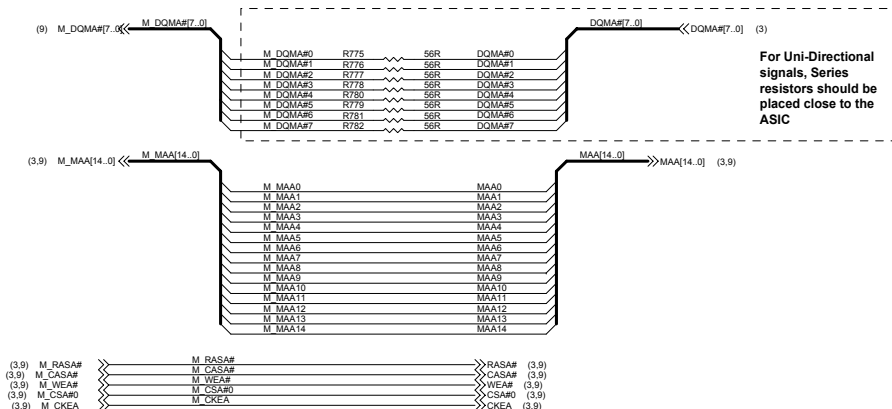
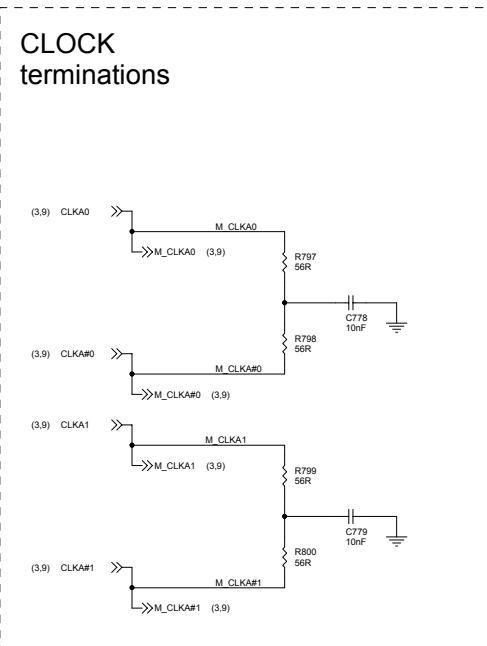
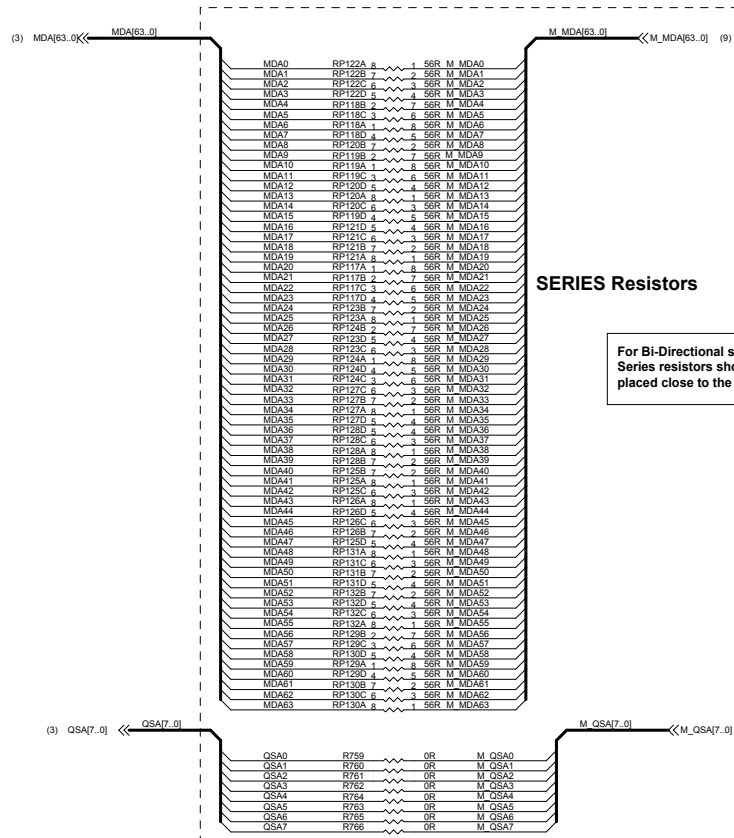


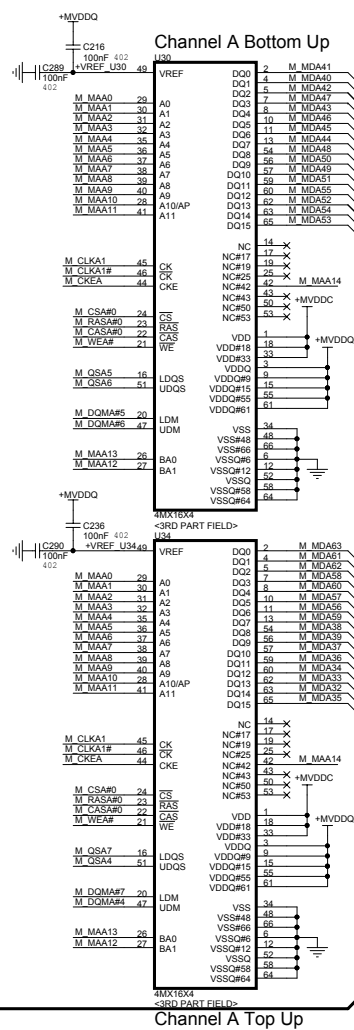
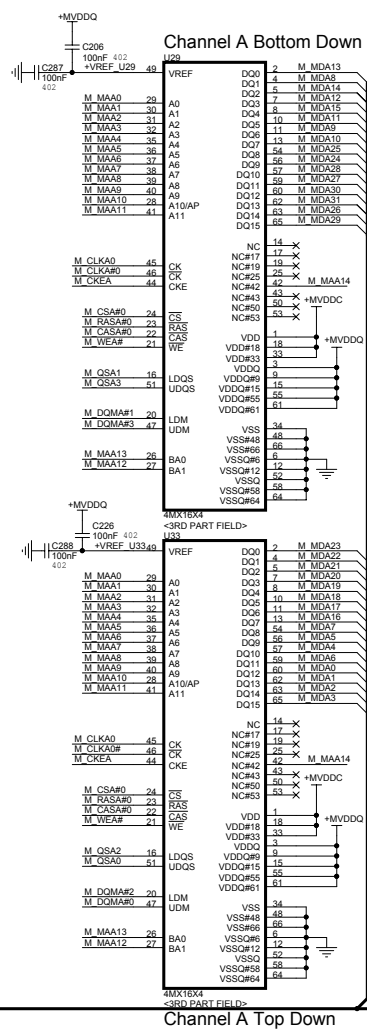
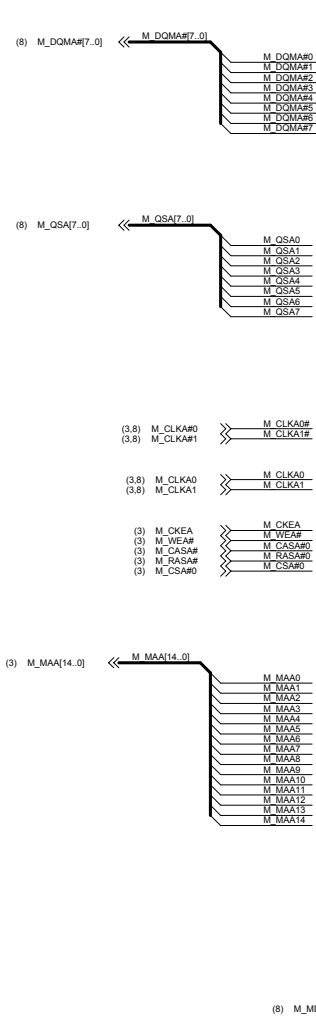
Part	Vout	R1	R2
MAX1935 0.8V Ref	1.2V	1.00K 1% 412 ATI P/N 3160100100	2.00K 1% 402 ATI P/N 3160200100
	1.79V	6.81K 1% ATI P/N 3160681100	5.49K 1% 402 ATI P/N 3160549100



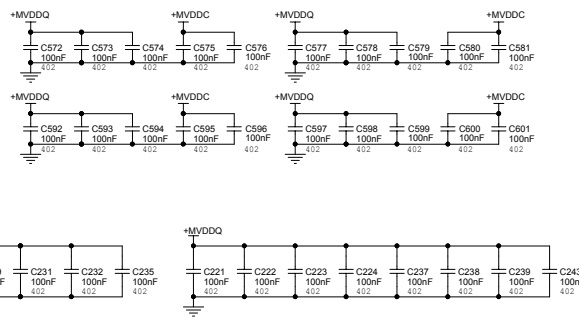
ATI Technologies Inc.
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Markham, Ontario
Canada L3T 7X5
(905) 882-2600

Title	PCIE RV370 128M TSOP VO-SV/DI
Size	Document Number 105-A260xx-00
Custom	
Date	Friday, April 30, 2004
Sheet	7 of 15





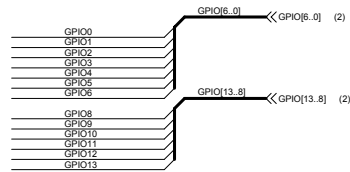
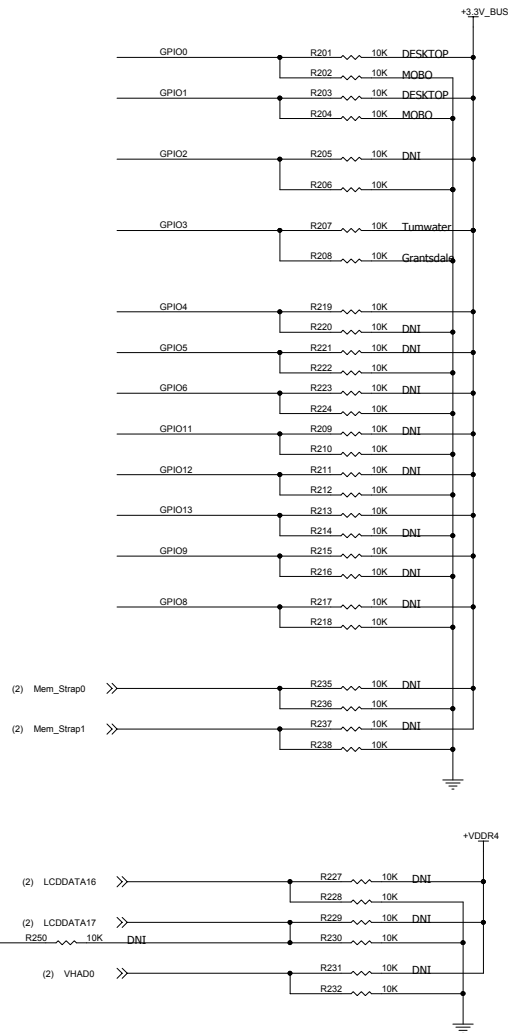
Put 1 uF cap per power pin of memory



DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

OPTION STRAPS

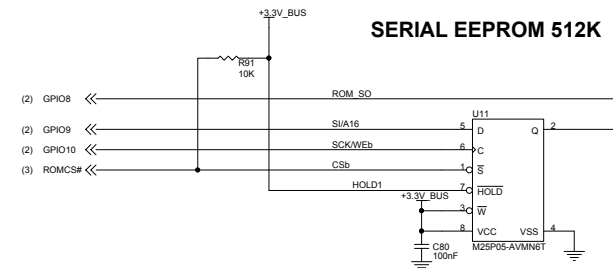


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrre-compatible mode 10: PCI Express 1.0 mode (Turwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHADO net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present 1 - No slave VIP host port devices reporting presence during reset	

STRAP P	INTERRUPT
LOW	ENABLED (DEFAULT)
HIGH	DISABLED

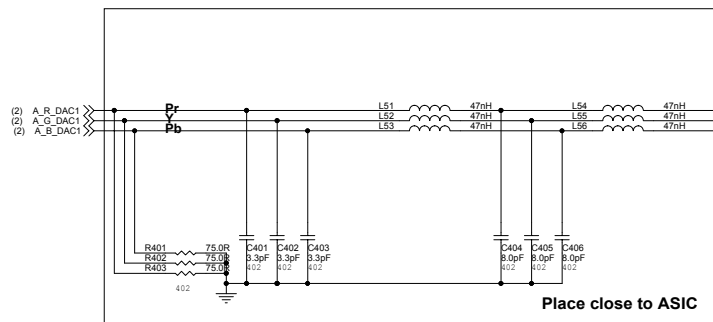
MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	0	0
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K

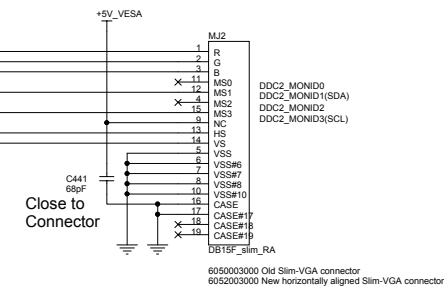
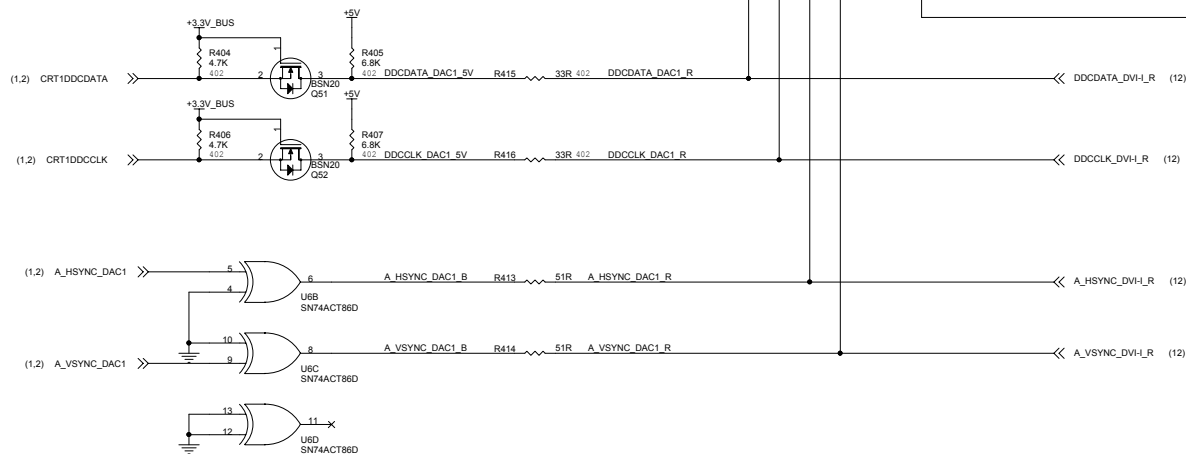
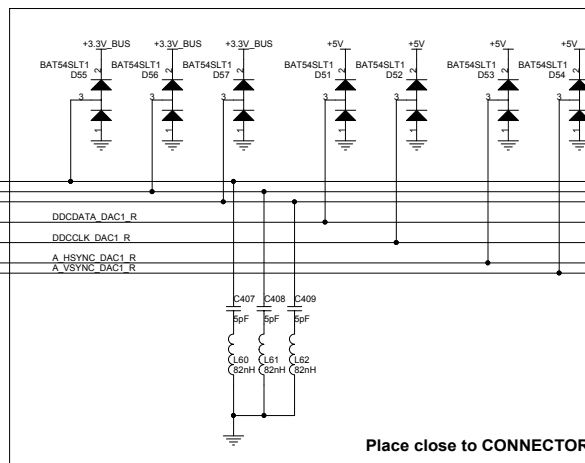


<Variant Name>

PRIMARY CRT

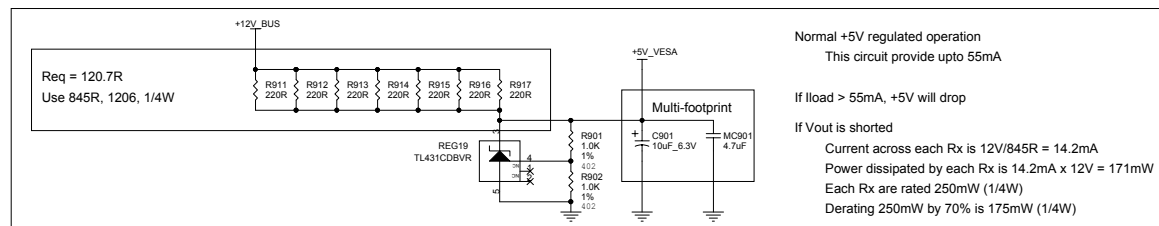
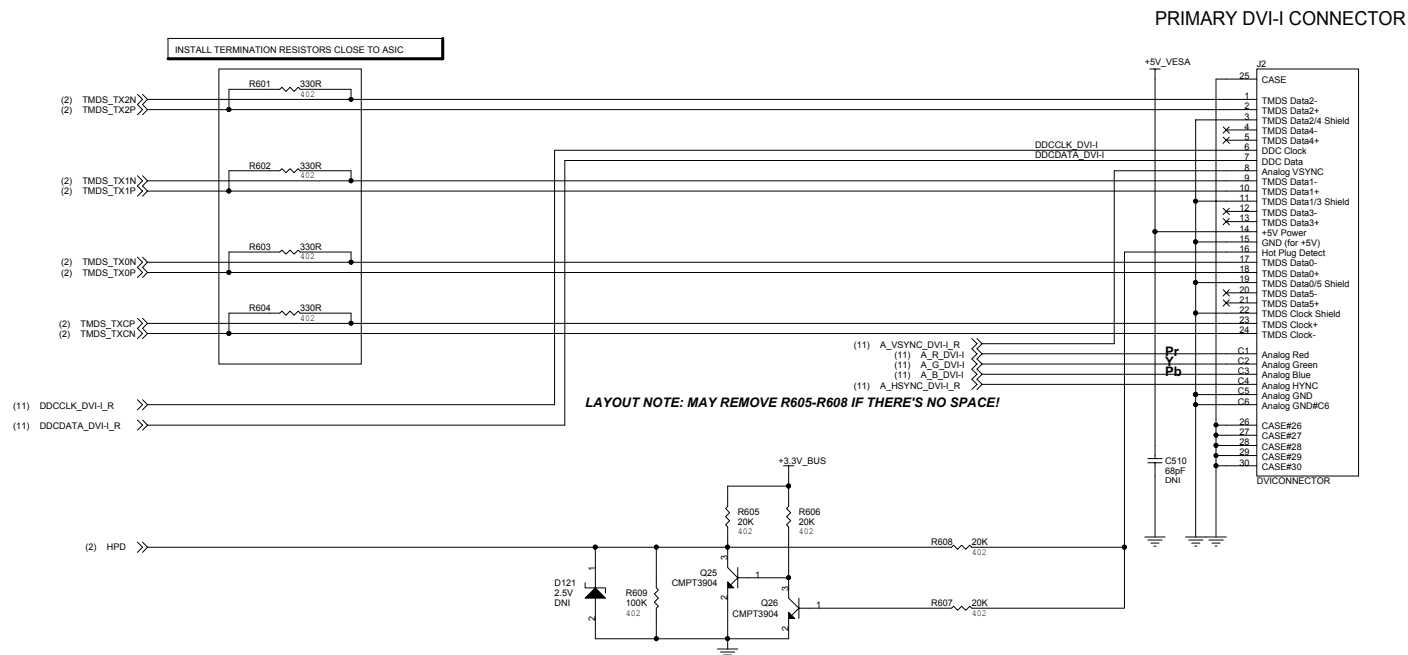


OPTIONAL ESD/HOTPLUG PROTECTION DIODES

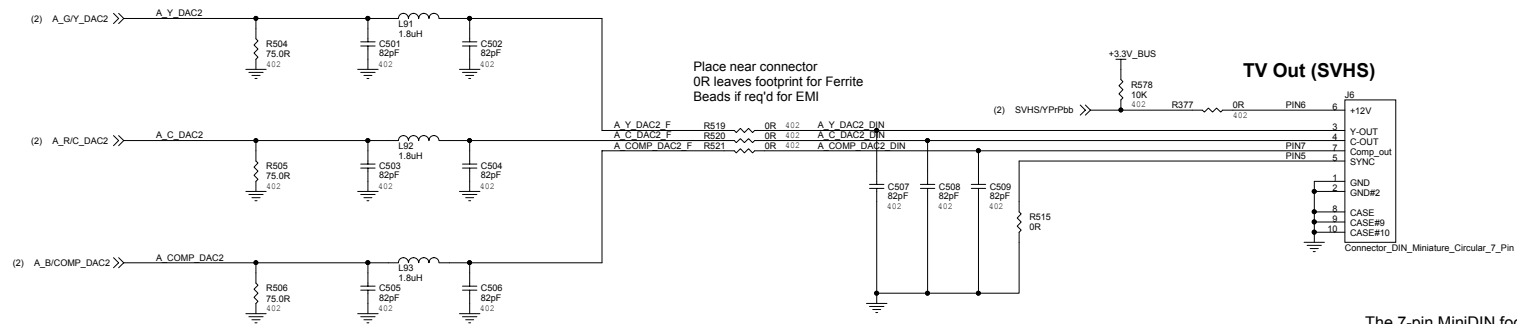


DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional SDA
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional SCL
15	Monitor ID bit 3	Open	SDA	SCL	SCL
9	N/C	+5V	+5V	+5V	Optional
Hardware Support	Mechanical Key	50mA min 1A max	50mA min 1A max	300mA min 1A max	Yes

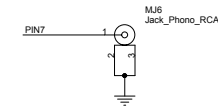
Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



Place Resistors close to ASIC.



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500
- 4-pin Svideo MiniDIN P/N 6070001000



DVI/VGA SCREWS



Bracket Screws



MISC. BOARD PARTS



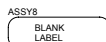
6_X_11



ATI_LOGO_LABEL



ATI_LOGO_LABEL



9050005900;9050005900;9050005900;9050005900;9050005900

ATX Brackets



NO TABS, DVI
80200321A0

DVI ATX



TOP TAB (LP), DIN, DVI
8020033000

DVI+MiniDIN ATX

DNE

Slim-VGA ATX

6052003000 New horizontally aligned Slim-VGA connector



TOP TAB (LP), DIN, VGA
6052003000 New horizontally aligned Slim-VGA connector

Slim-VGA+MiniDIN ATX

LP Brackets



LP, NO TABS, DVI
8020032600

DVI LP



LP, TOP TAB, DIN, DVI
8020032700

DVI+MiniDIN LP



LP, NO TABS, VGA
80200328A0

Slim-VGA LP

No Top Tab

6052003000 New horizontally aligned Slim-VGA connector



TOP TAB, DIN, VGA
80200327A0

Slim-VGA+MiniDIN LP

6052003000 New horizontally aligned Slim-VGA connector



HEATSINK
7120005800



HEATSINK
7120005100



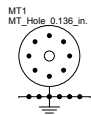
HEATSINK
7120002700



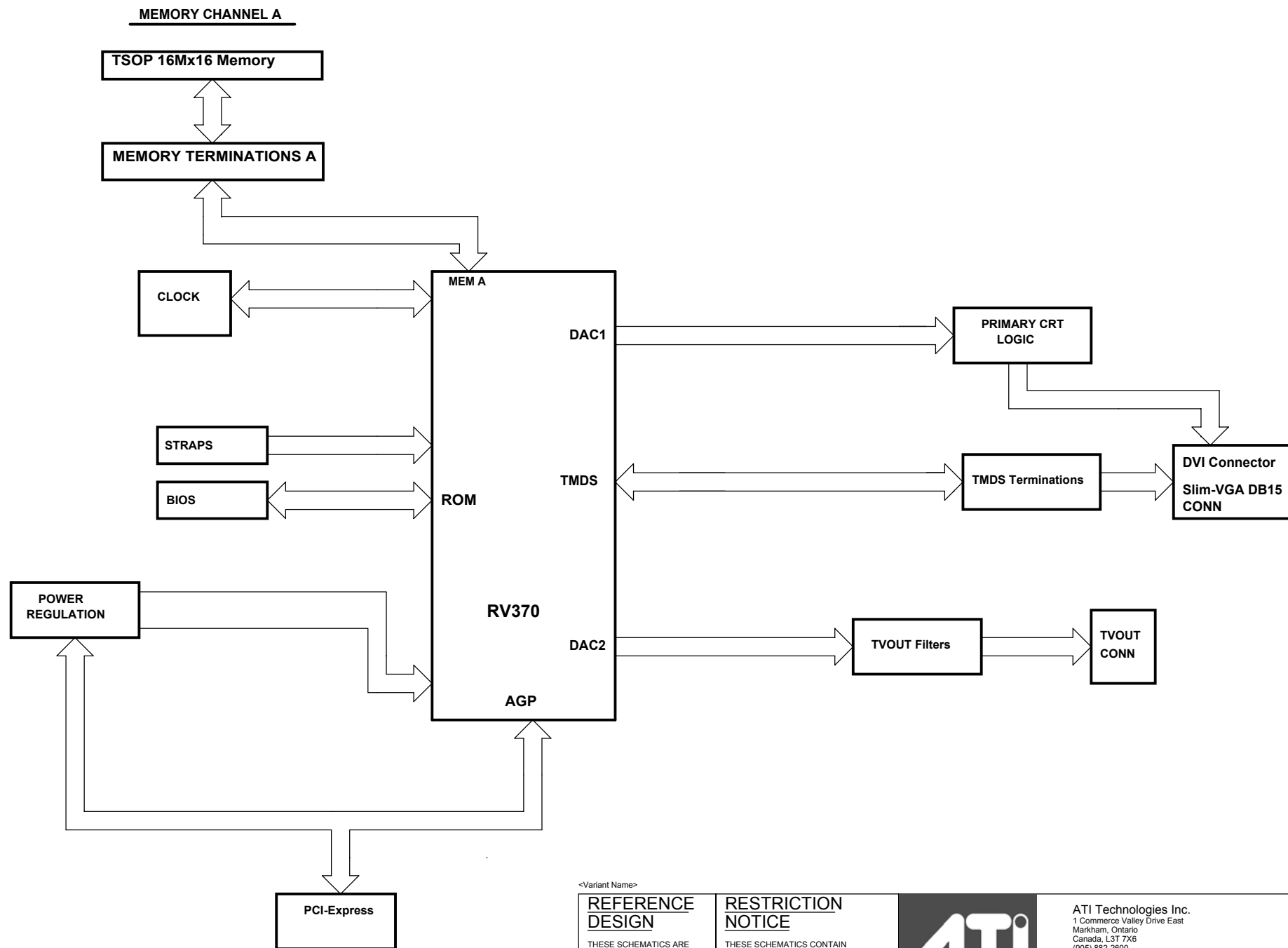
HEATSINK
7120008500

Spring push-pin

ITW push-pin



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Size	Document Number	105-A260xx-00	Rev
Custom			5
Date:	Friday, April 30, 2004	Sheet	14 of 15



<Variant Name>

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Size	Document Number	105-A260xx-00	Rev	5
B	Date: Friday, April 30, 2004	Sheet	15	of 15