PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI

Tall DVI-I + DP + DP + DP/HDMI + DP

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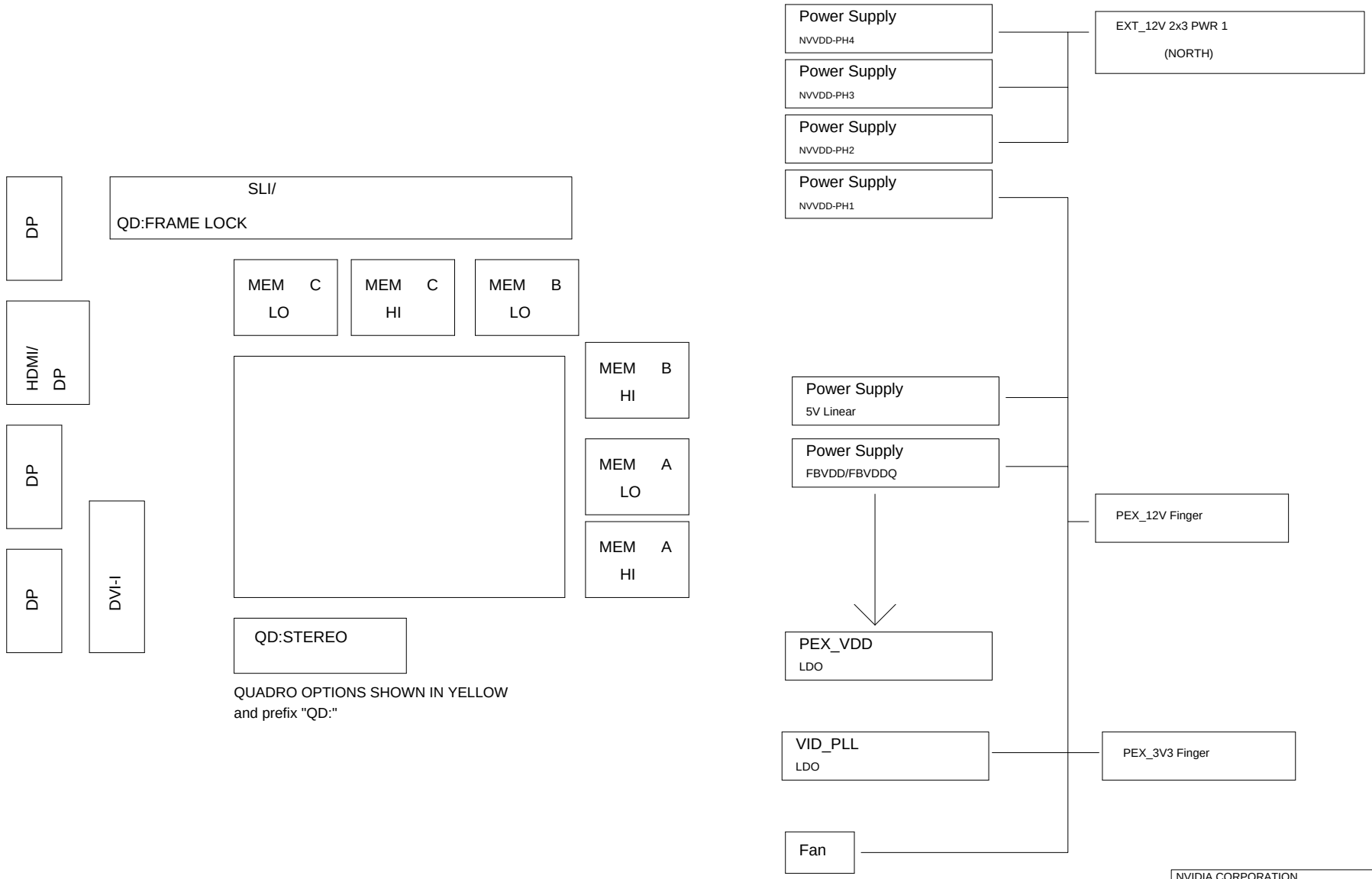
Block Diagram



QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	Block Diagram

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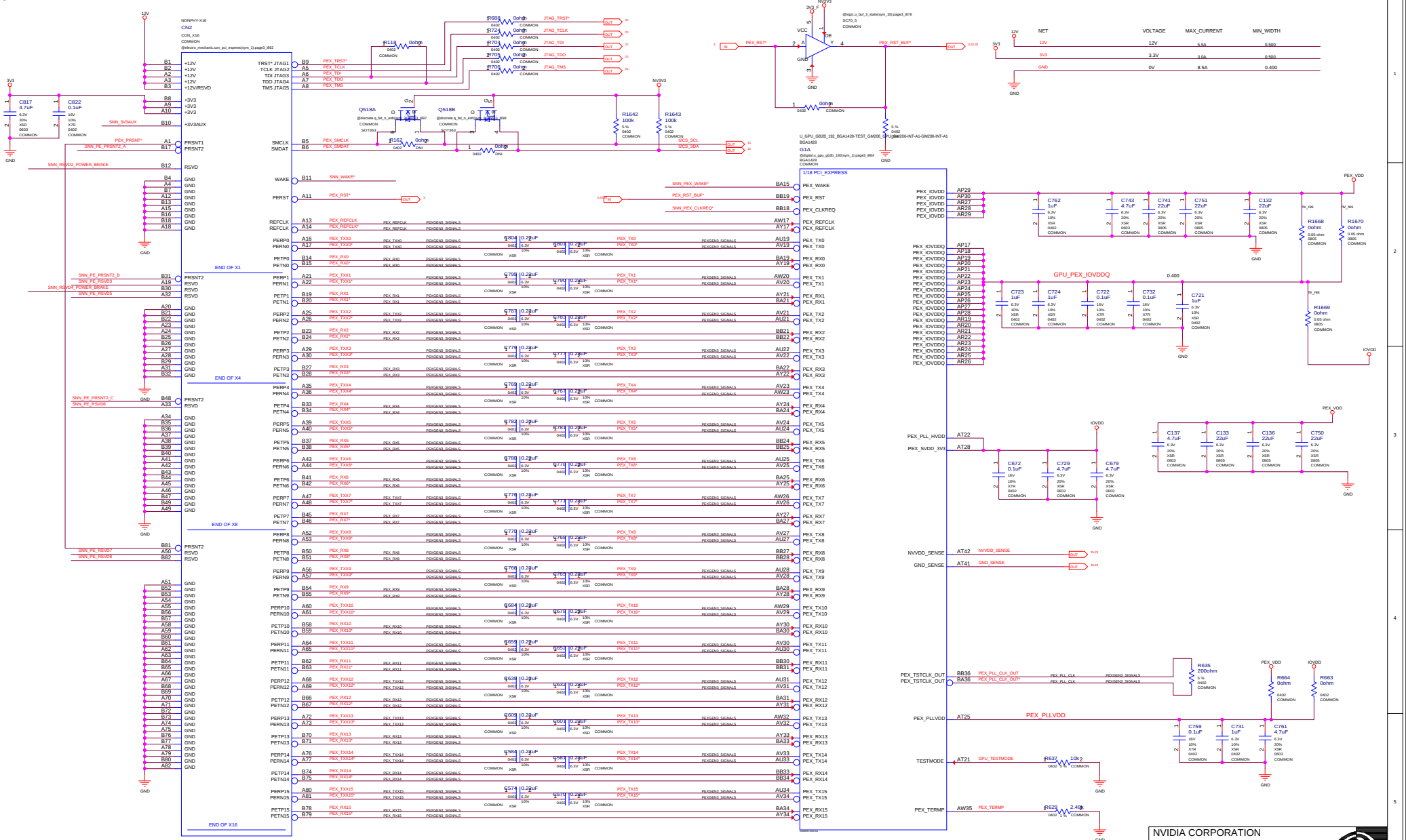
PCI Express



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PCI Express

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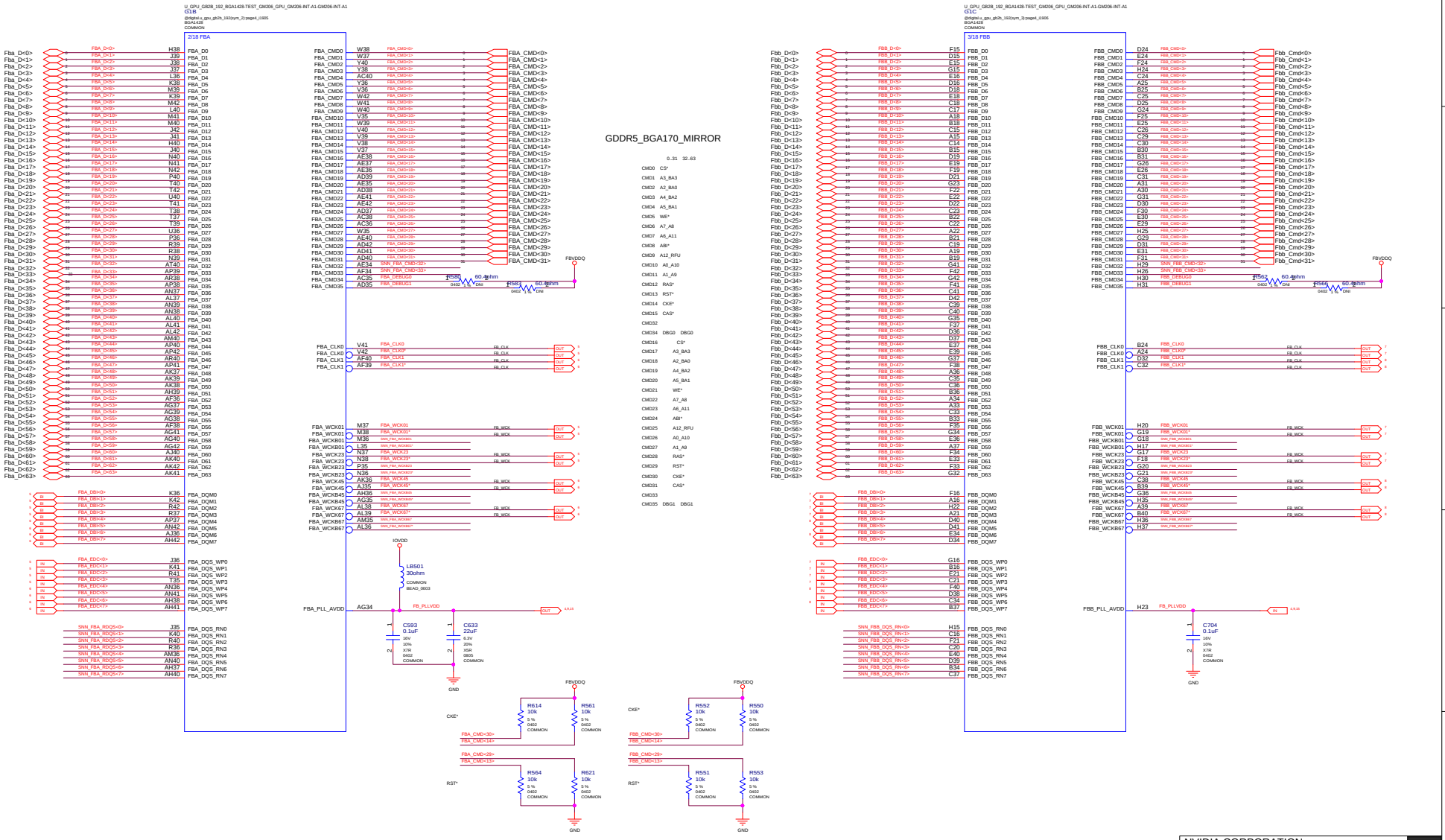
MEMORY: GPU Partition A/B



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: GPU Partition A/B

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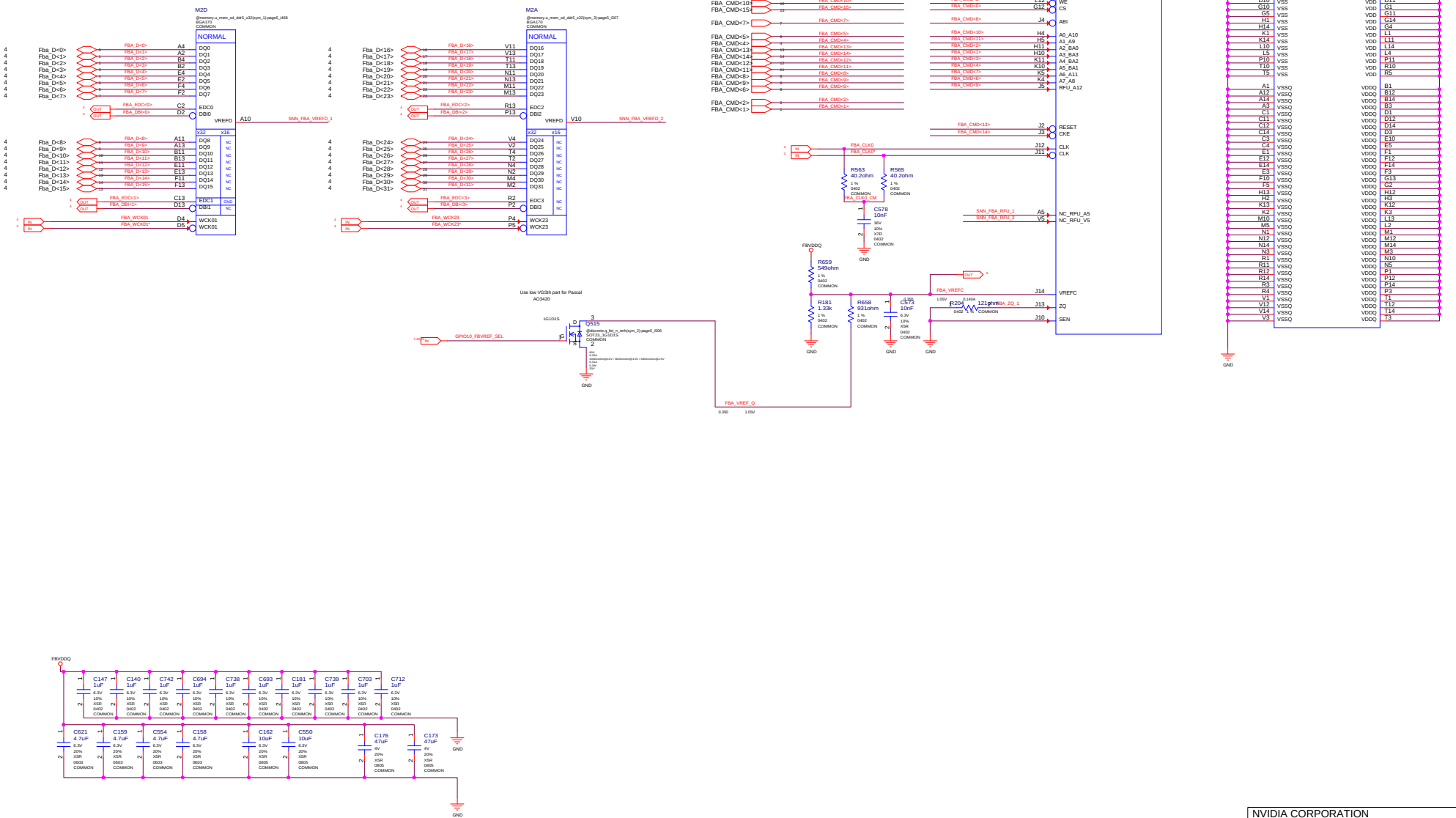
MEMORY: FBA Partition 31..0



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBA[31:0]

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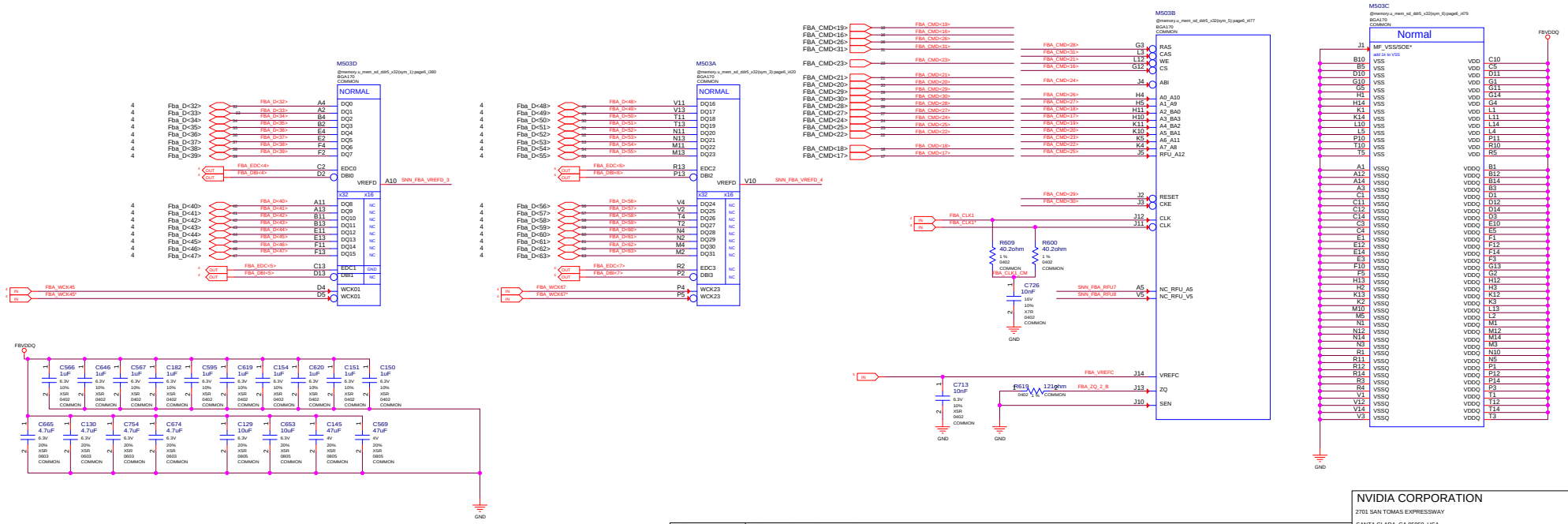
MEMORY: FBA Partition 63..32



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBA[63:32]

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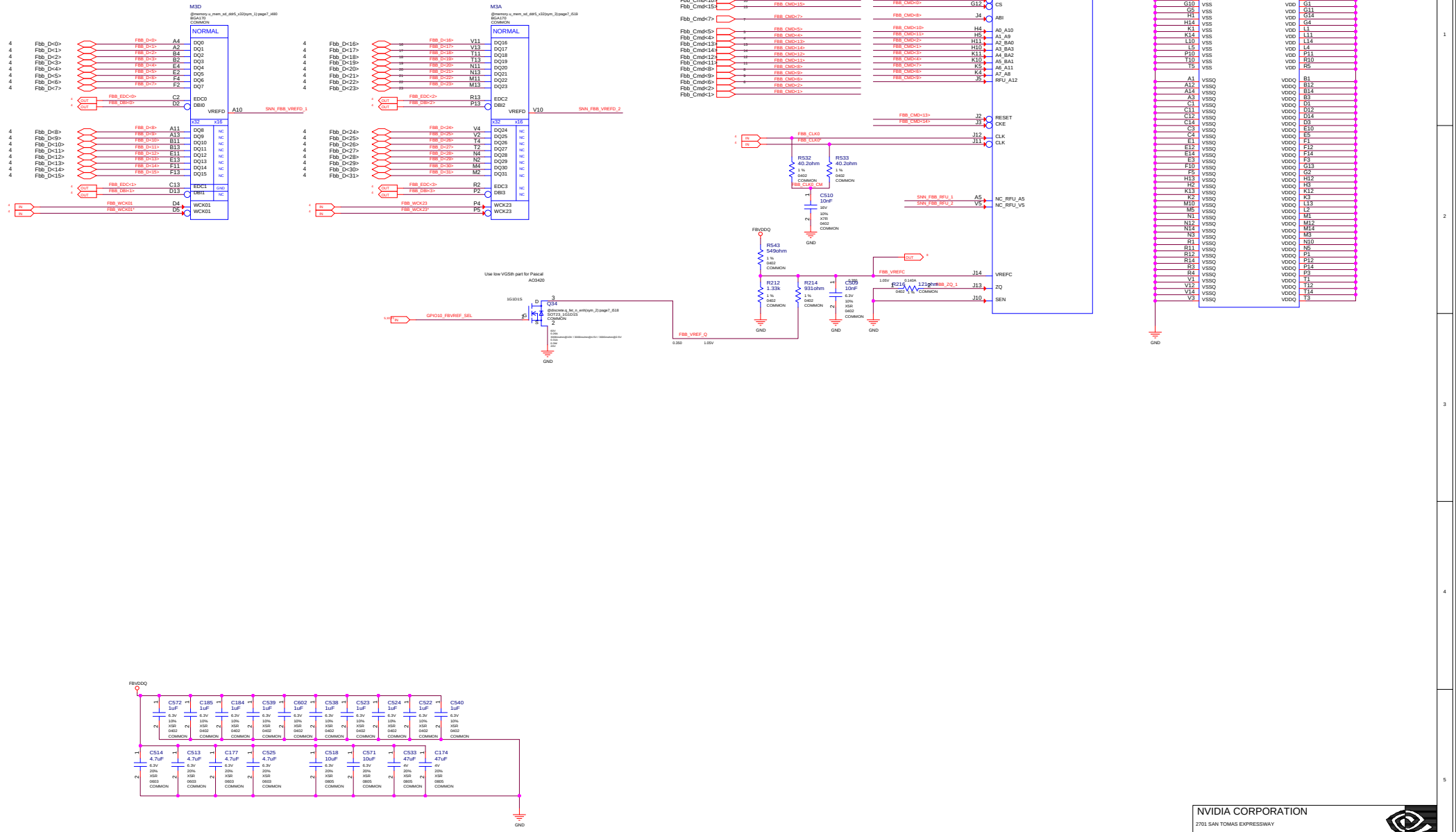
MEMORY: FBB Partition 31..0



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBB[31:0]

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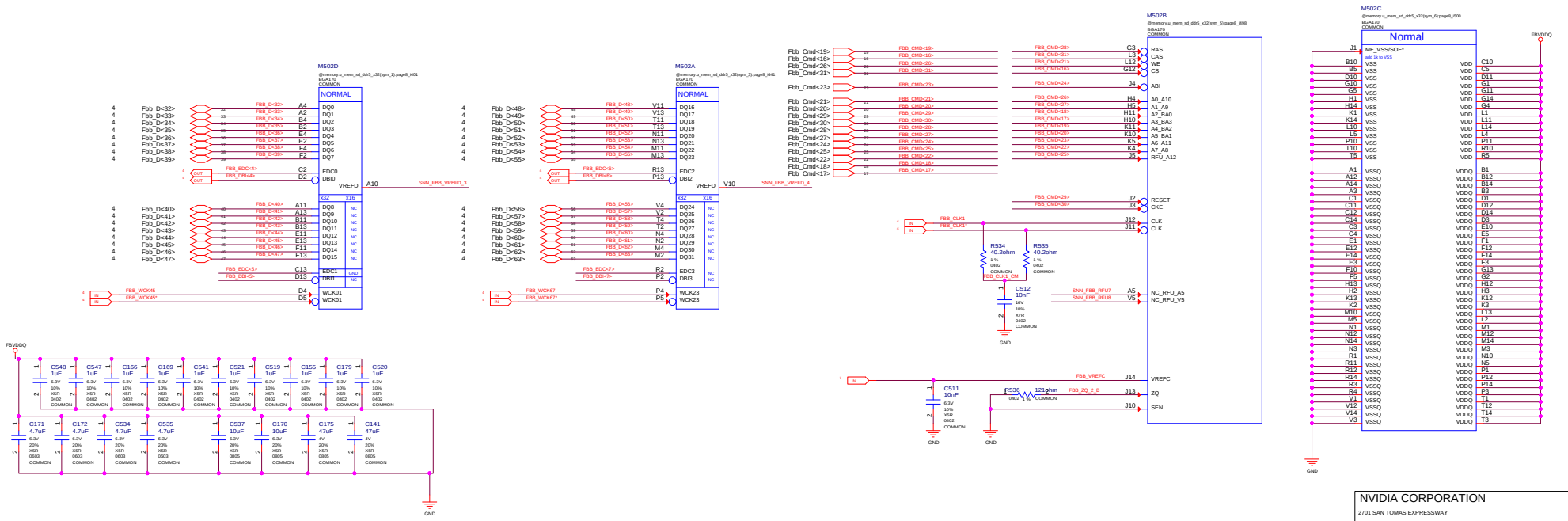
MEMORY: FBB Partition 63..32



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBB[63:32]

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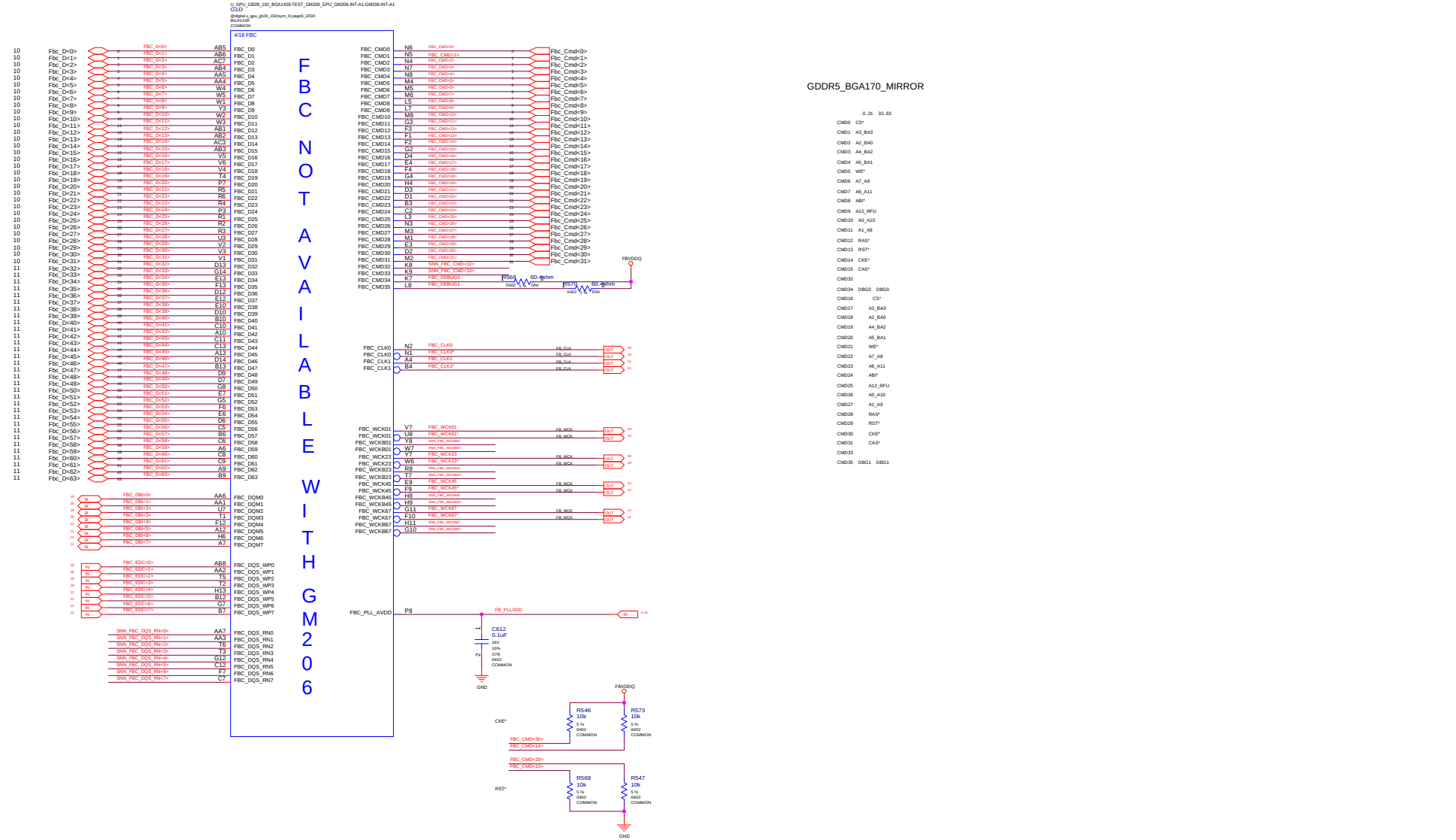
MEMORY: GPU Partition C/D



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: GPU Partition C

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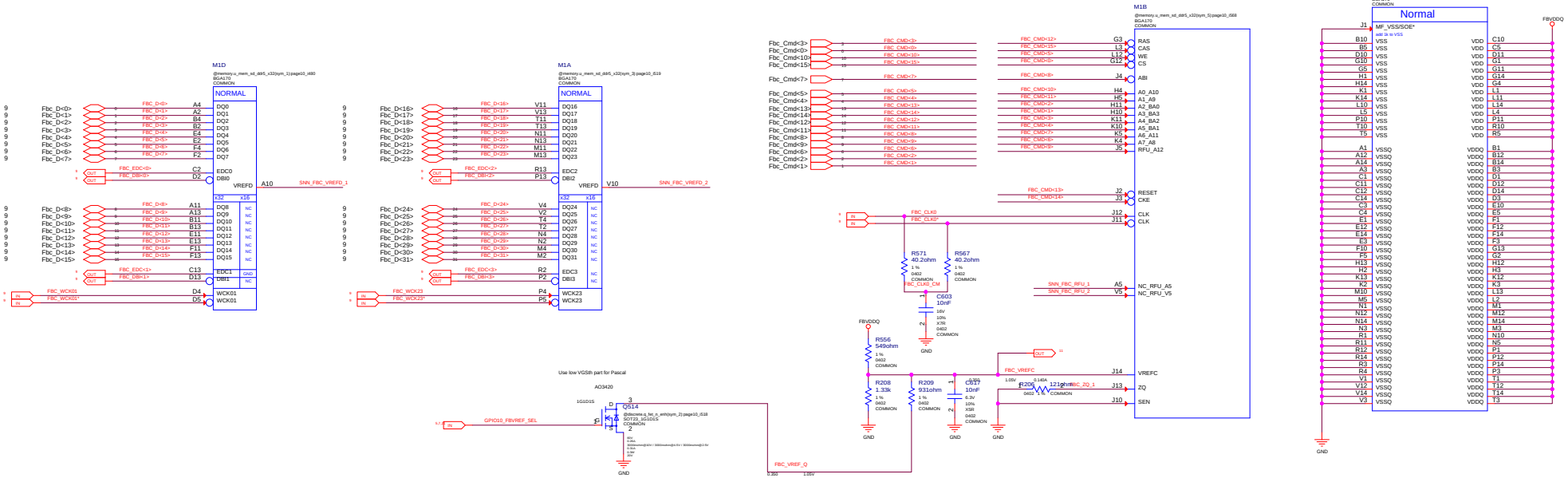
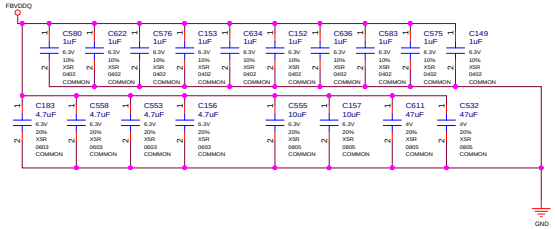
MEMORY: FBC Partition 31..0





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBC[31:0]

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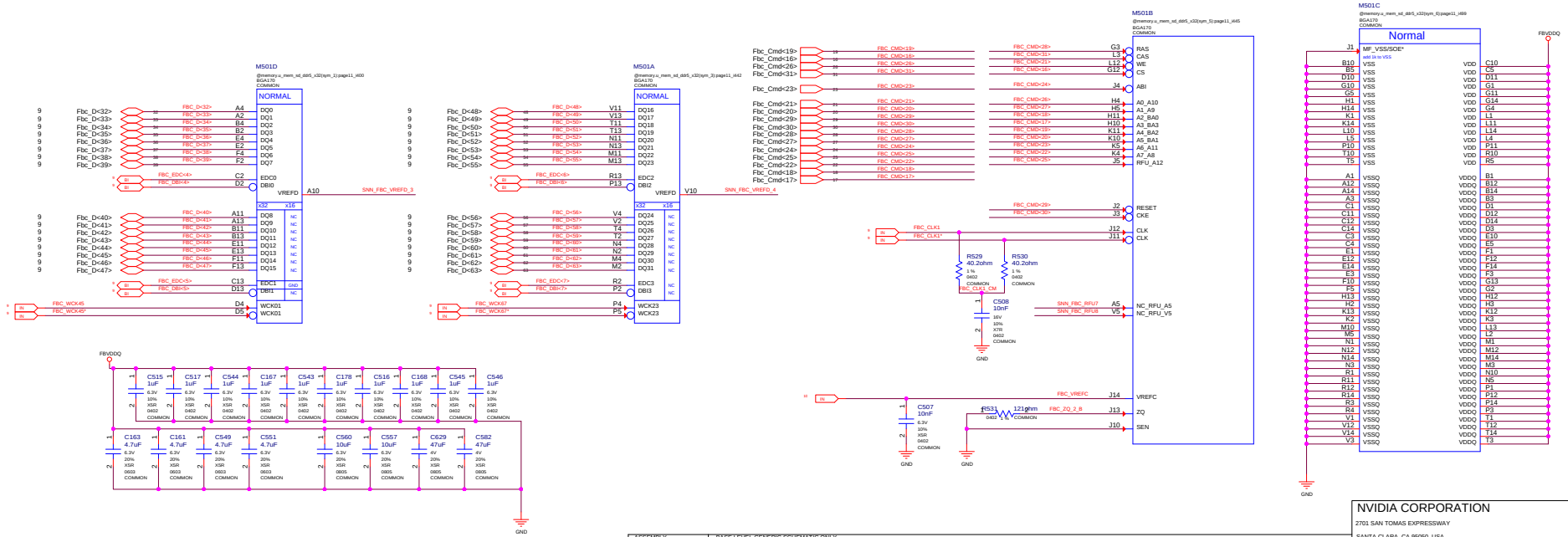
MEMORY: FBC Partition 63..32



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
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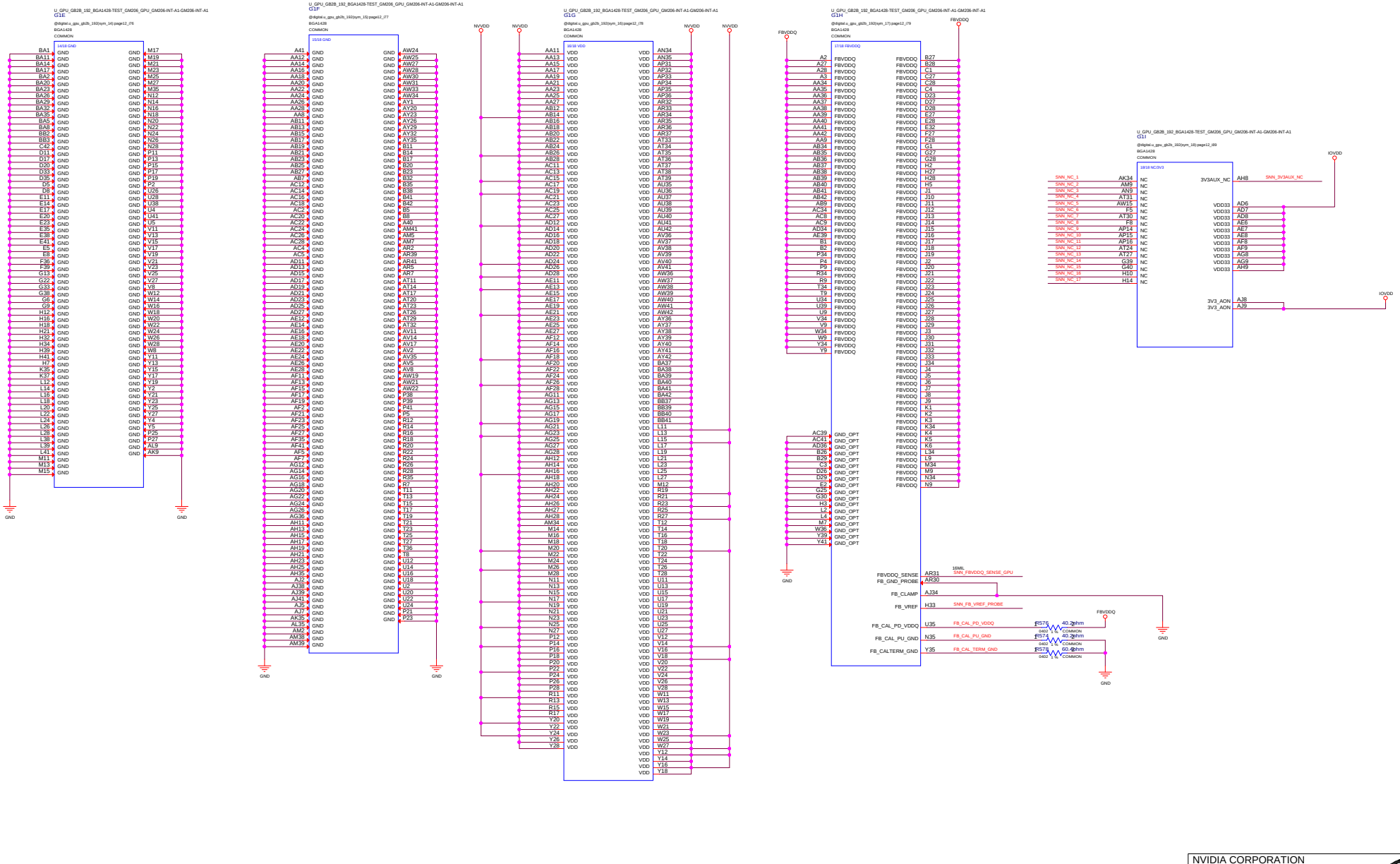
GPU PWR and GND



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU PWR and GND

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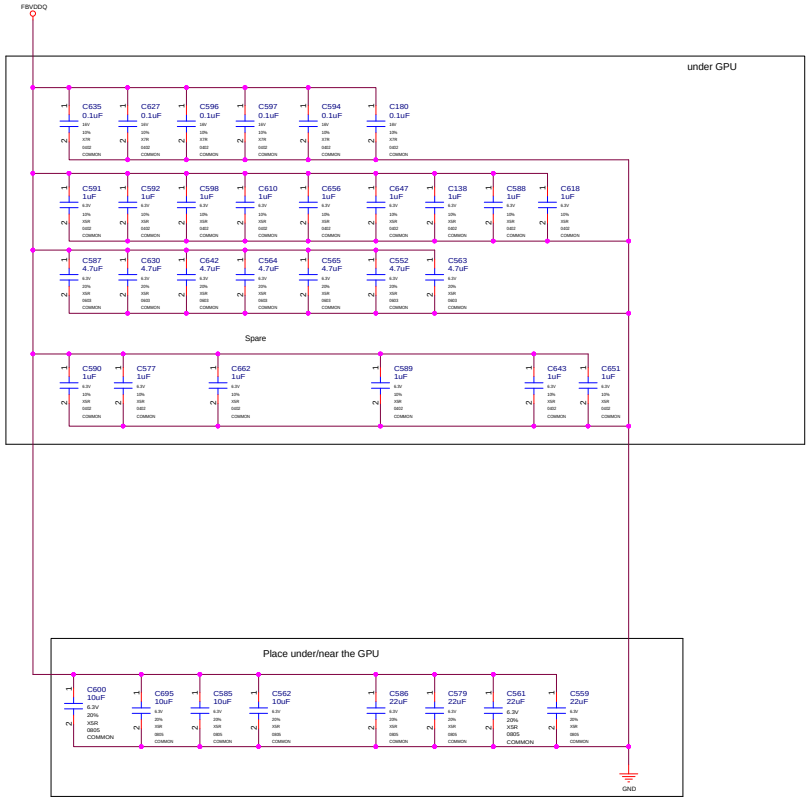
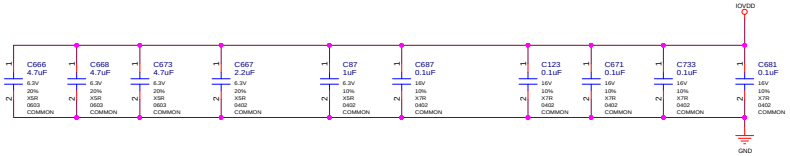
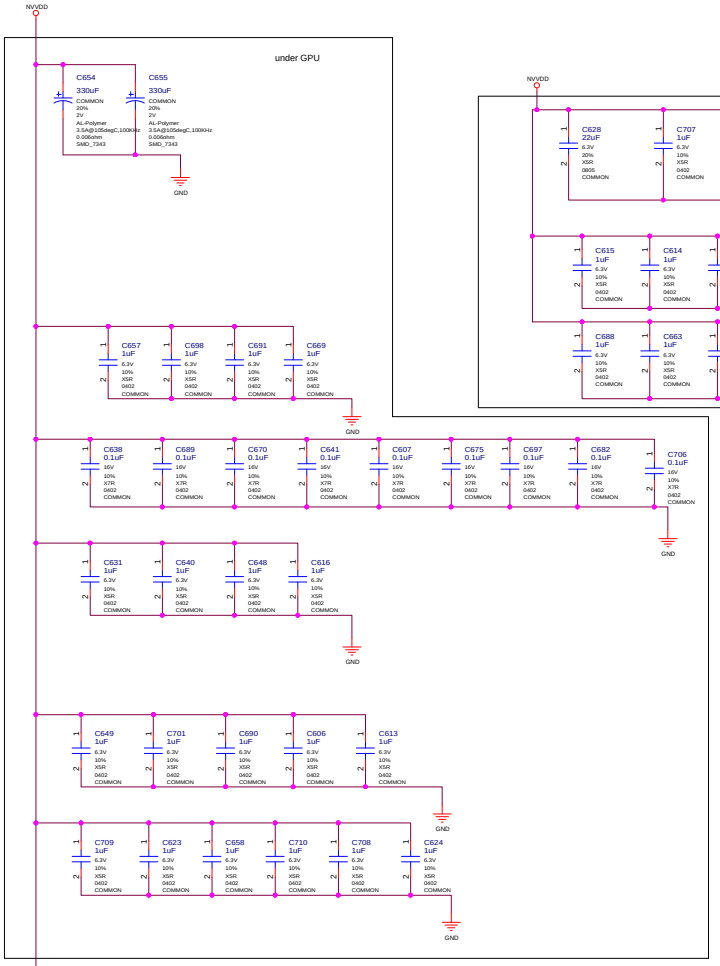
GPU Decoupling

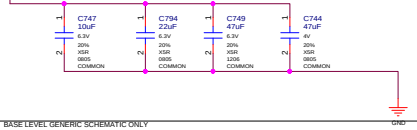
FBVDDQ





NVVDD





	Under GPU	Near GPU
NVVDD	90uF + 1x 330uF	88uF
SVVDD	32uF	22uF
Combined (Maxwell)	122uF + 1x 330uF	110uF

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU Decoupling

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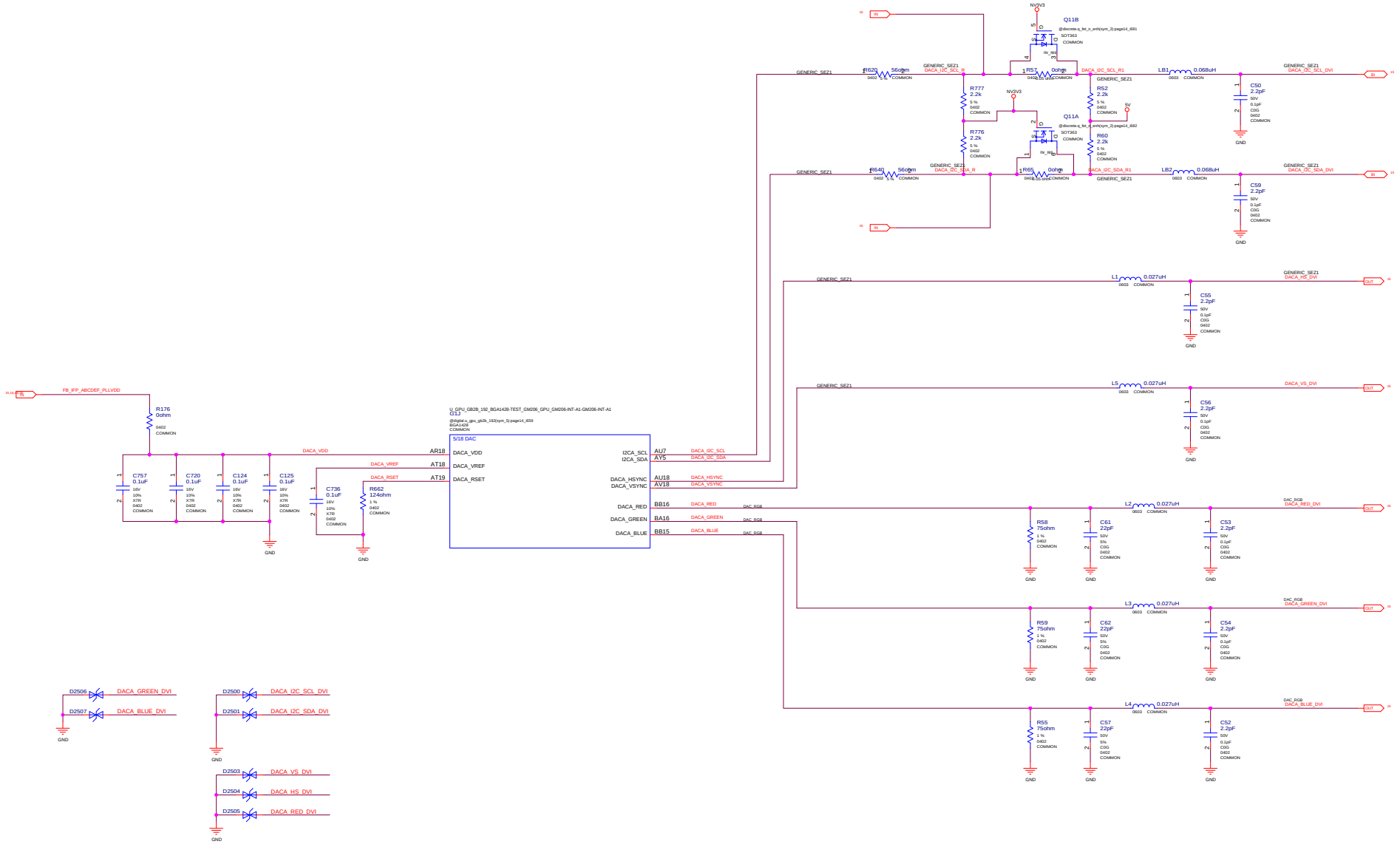
DACA Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DACA Interface

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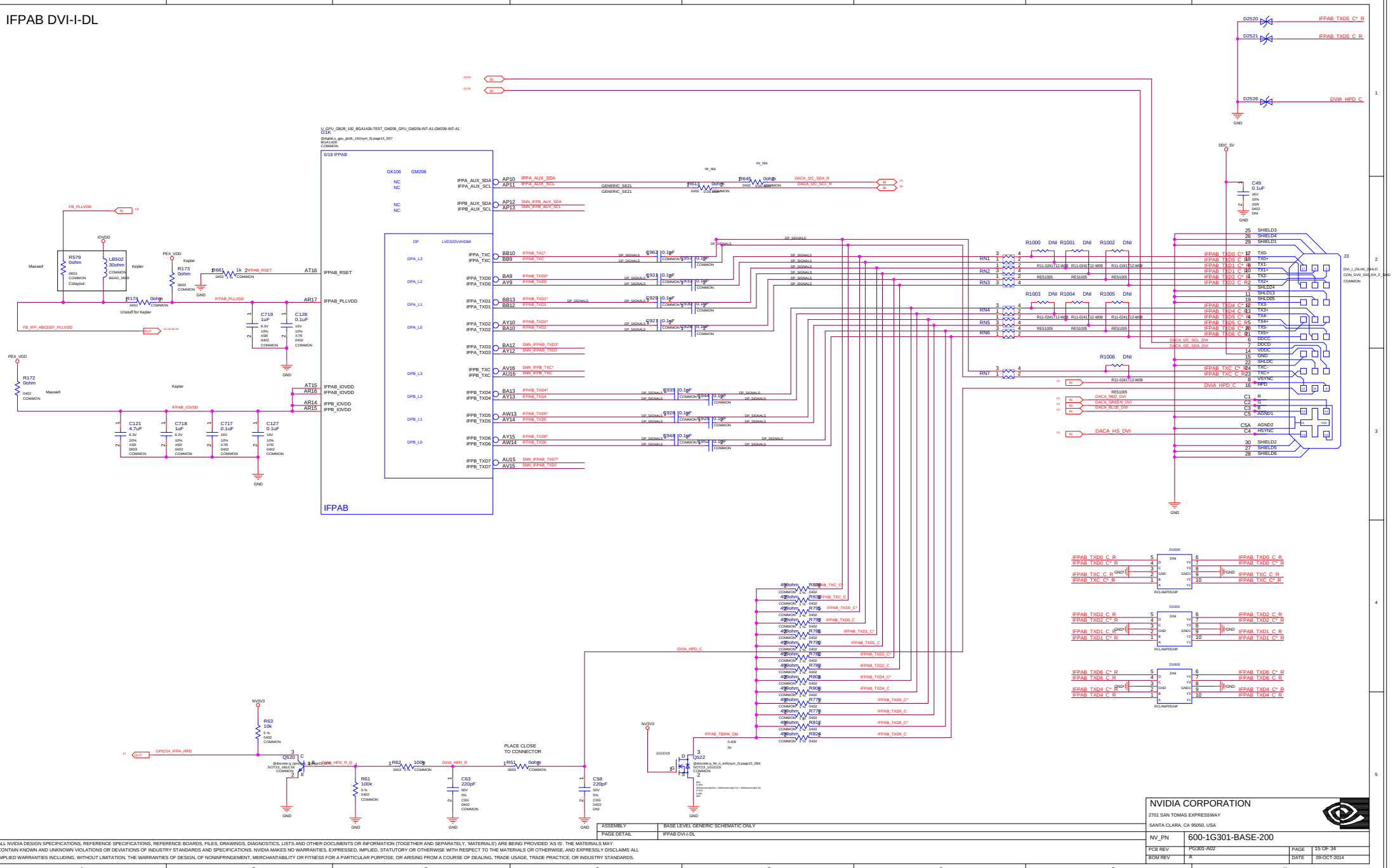
IFPAB DVI-I-DL



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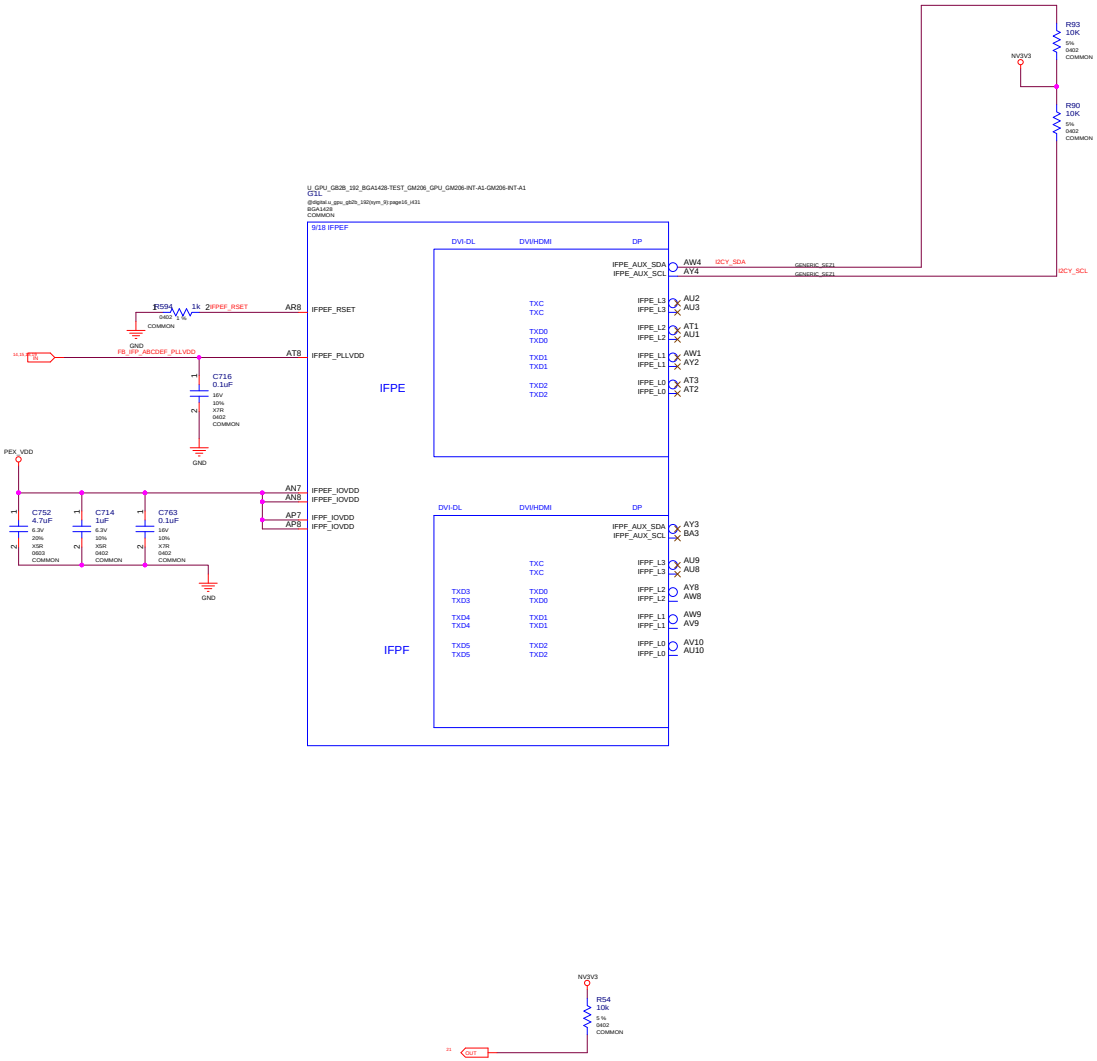
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPAB DVI-I-DL

Page18: IFPEF with IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPEF with IFPE DP

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IFPF DP

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPF DP

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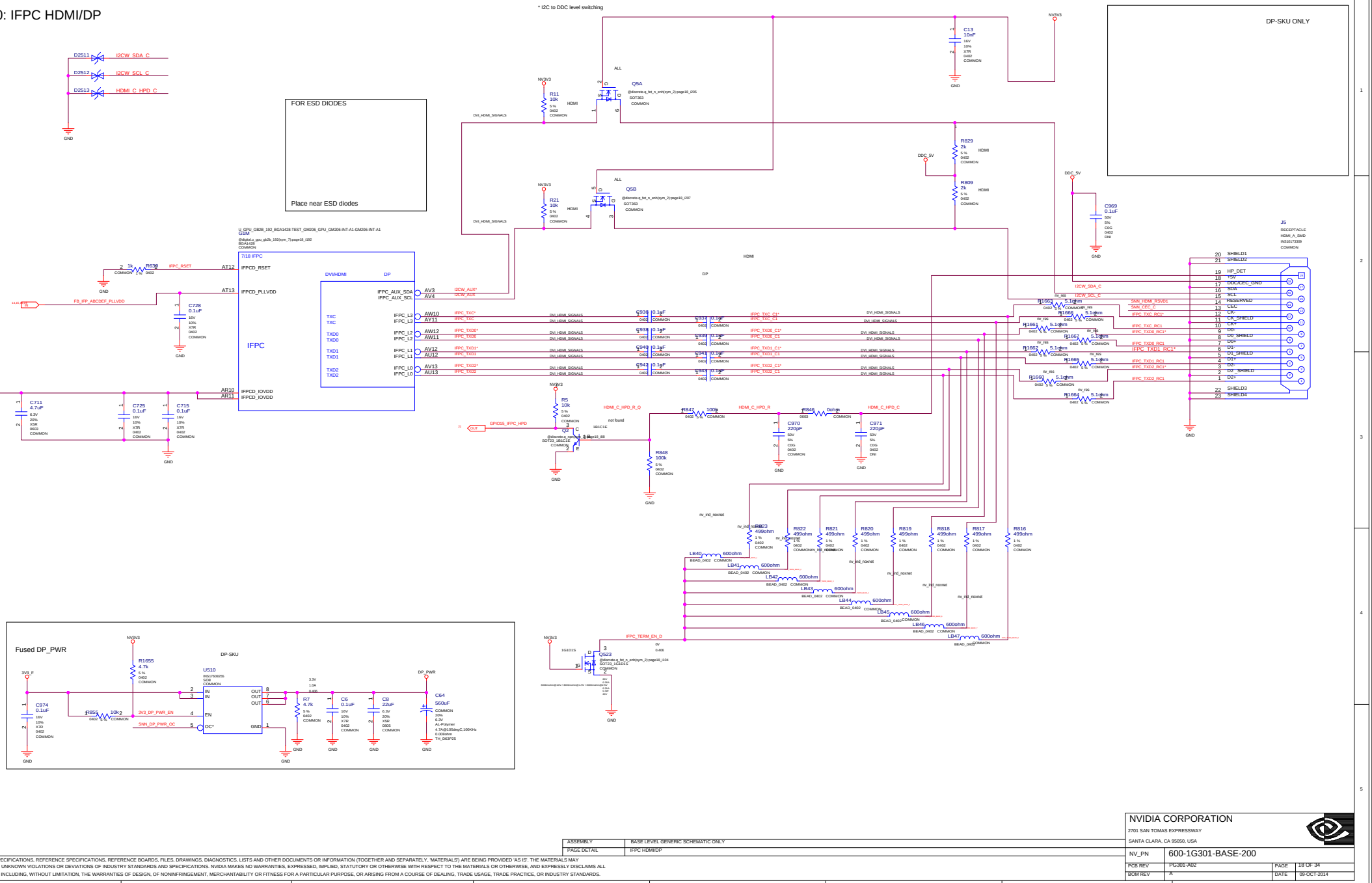
Page20: IFPC HDMI/DP



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPC HDMI/DP

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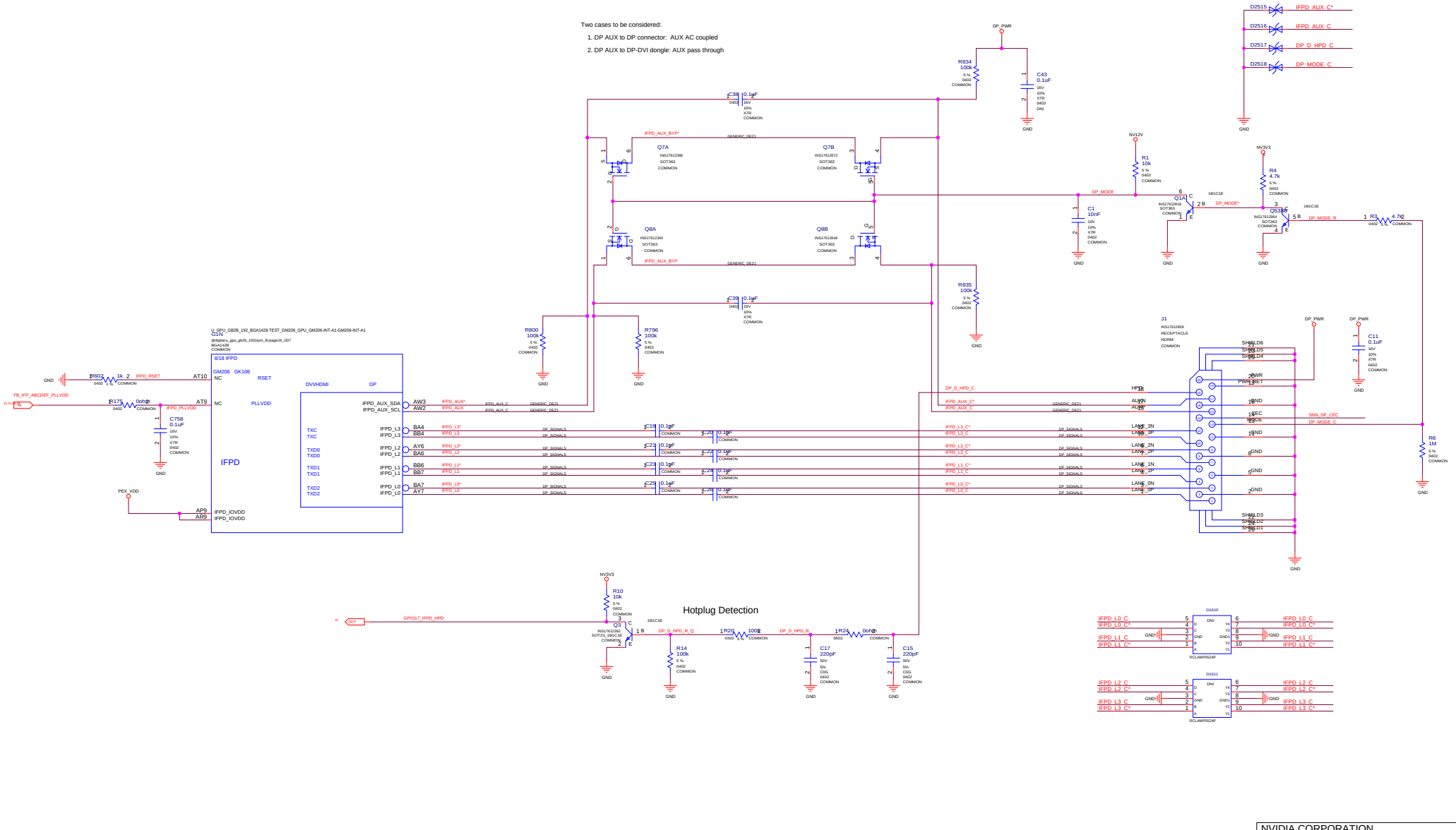
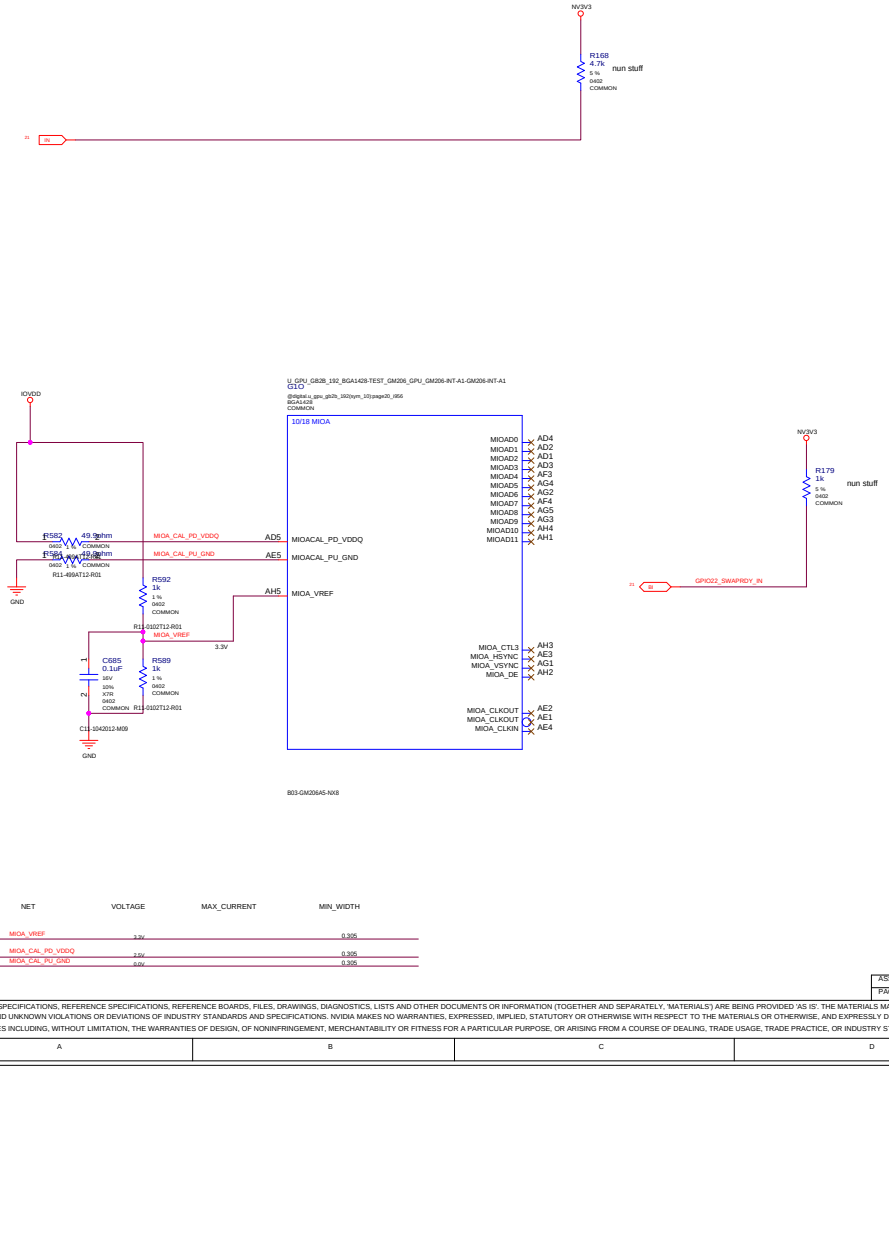
IFPD DP



MIOA/SLI Interface



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	3.3V		0.305
MIOA_CAL_PD_VDDQ	2.5V		0.305
MIOA_CAL_PU_GND	0.0V		0.305

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MIOA

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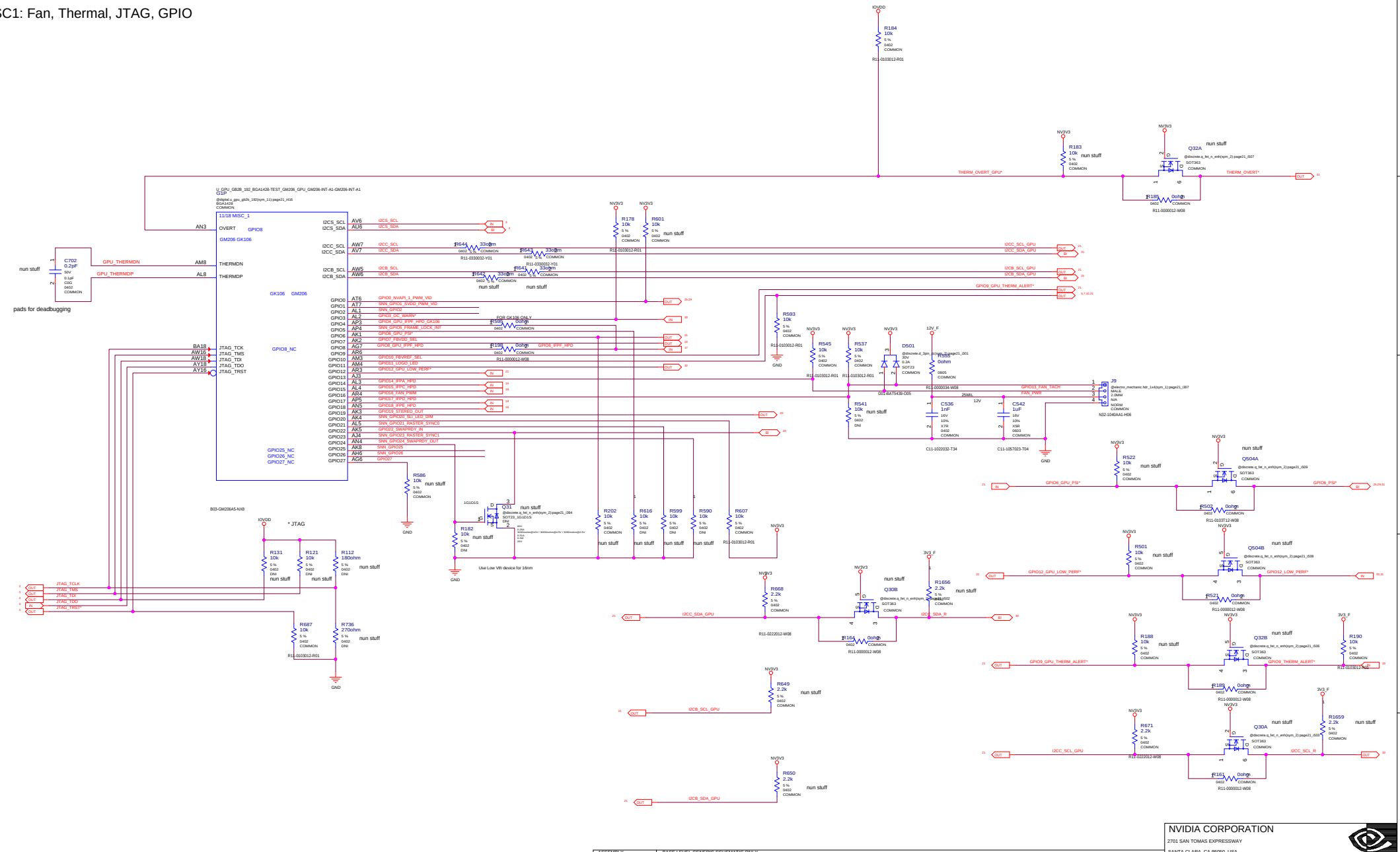
MISC1: Fan, Thermal, JTAG, GPIO



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO

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MISC2: ROM, XTAL, Straps

	KEPLER	MAXWELL
STRAP0	USER_BIT [3:0]*	
STRAP1	3GIO_PADCFG_LUT_ADR*	
STRAP2	PCI_DEVID [3:0]*	
STRAP3	SOR_EXPOSED [3:0]*	
STRAP4	DP_PLL_VDD_33V*	
	PEX_MAX_SPEED*	
	PEX_SPD_CHANGE_GEN3*	
	*	
ROM_SI	RAMCFG[0]*	RAMCFG[0]*
	RAMCFG[1]*	RAMCFG[1]*
	RAMCFG[2]*	RAMCFG[2]*
	RAMCFG[3]*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	VGA_DEVICE*
	SMB_ALT_ADDR*	SMB_ALT_ADDR*
	FB[0]_APERTURE_SIZE*	PCIE_CFG*
	FB[1]_APERTURE_SIZE*	DEVID_SEL*
ROM_SCLK	PEX_PLL_EN_TERM100*	SOR0_EXPOSED*
	PCI_DEVID_EXT[5]*	SOR1_EXPOSED*
	SUB_VENDOR*	SOR2_EXPOSED*
	PCI_DEVID_EXT[4]*	SOR3_EXPOSED*

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

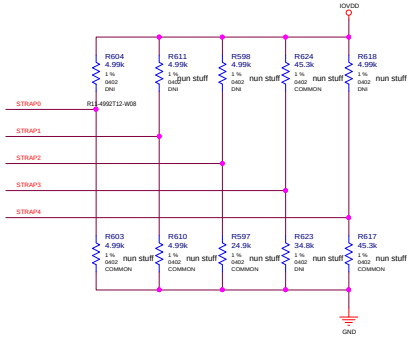
MULTI_STRAP_REF0_GND

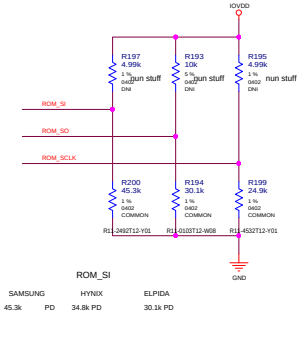
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND

MAXWELL

STRAP0

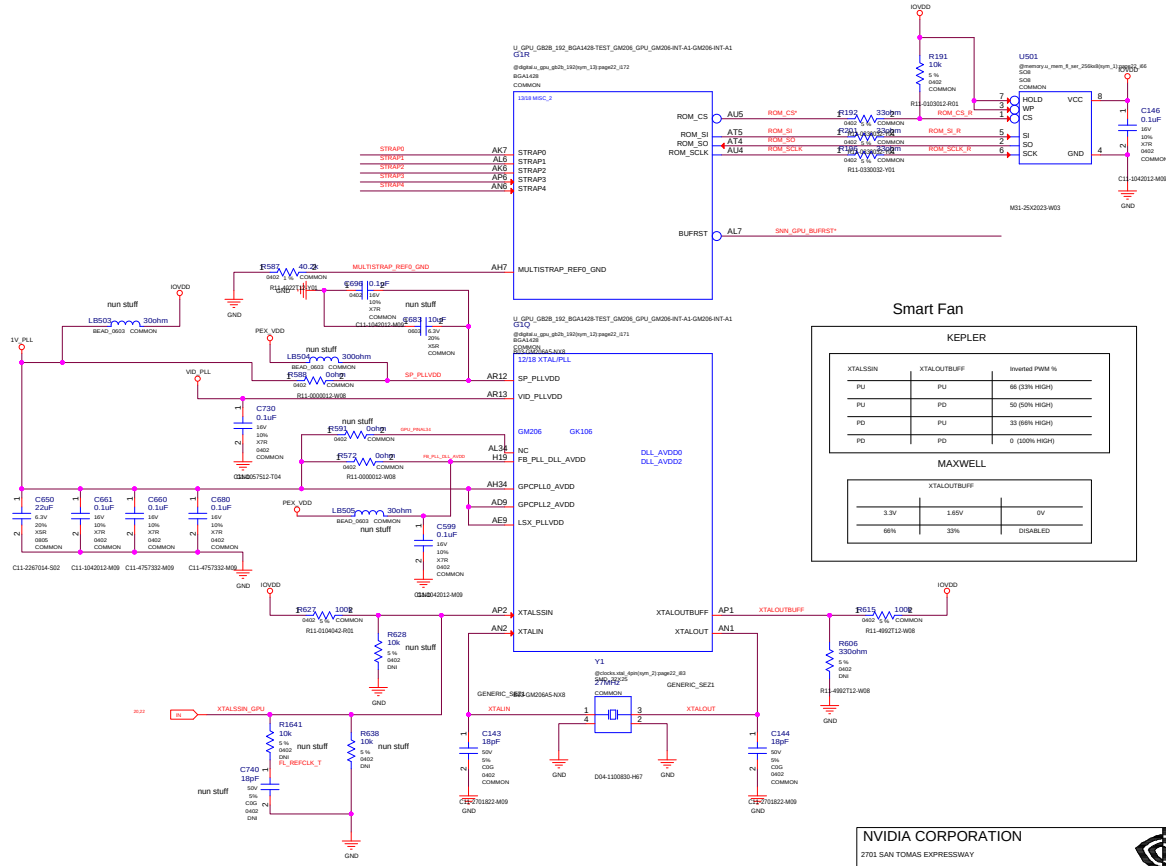
3.3V	1.65V	0V
GC6+ ISLAND ENABLED	GC6+ DEBUG MODE	GC6+ ISLAND DISABLED





ROM_SI

SAMSUNG	HYNIX	ELPIDA
45.3k	PD 34.8k PD	30.1k PD



Smart Fan

KEPLER

XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

MAXWELL

XTALOUTBUFF

3.3V	1.65V	0V
66%	33%	DISABLED

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC2: ROM, XTAL, Straps

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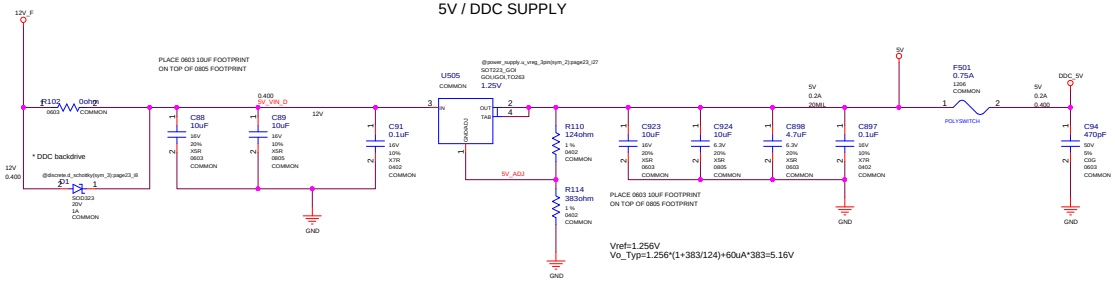
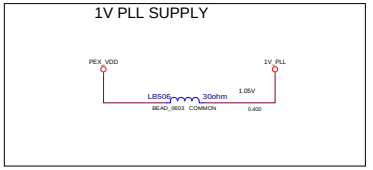
PS: 5V, PEX_VDD

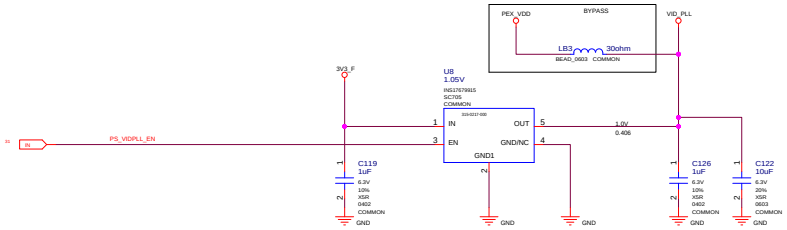
5V / DDC SUPPLY



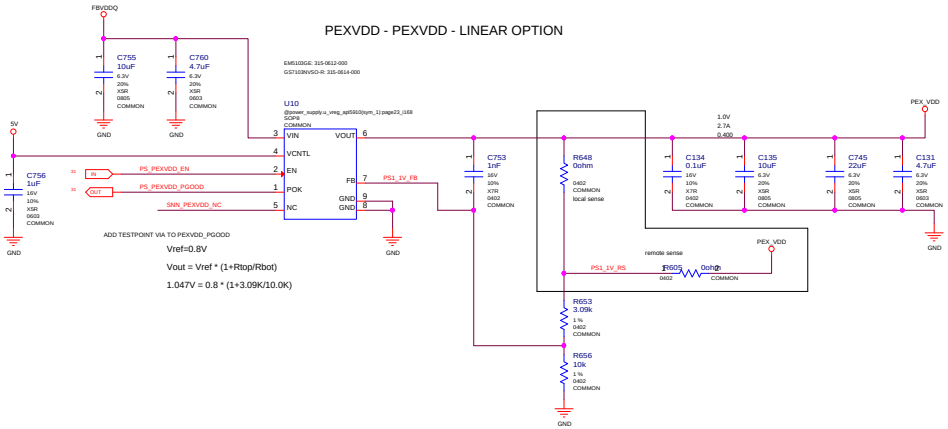
1V PLL SUPPLY



VID PLL SUPPLY



PEXVDD - PEXVDD - LINEAR OPTION



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 5V, PEX_VDD, VID_PLL

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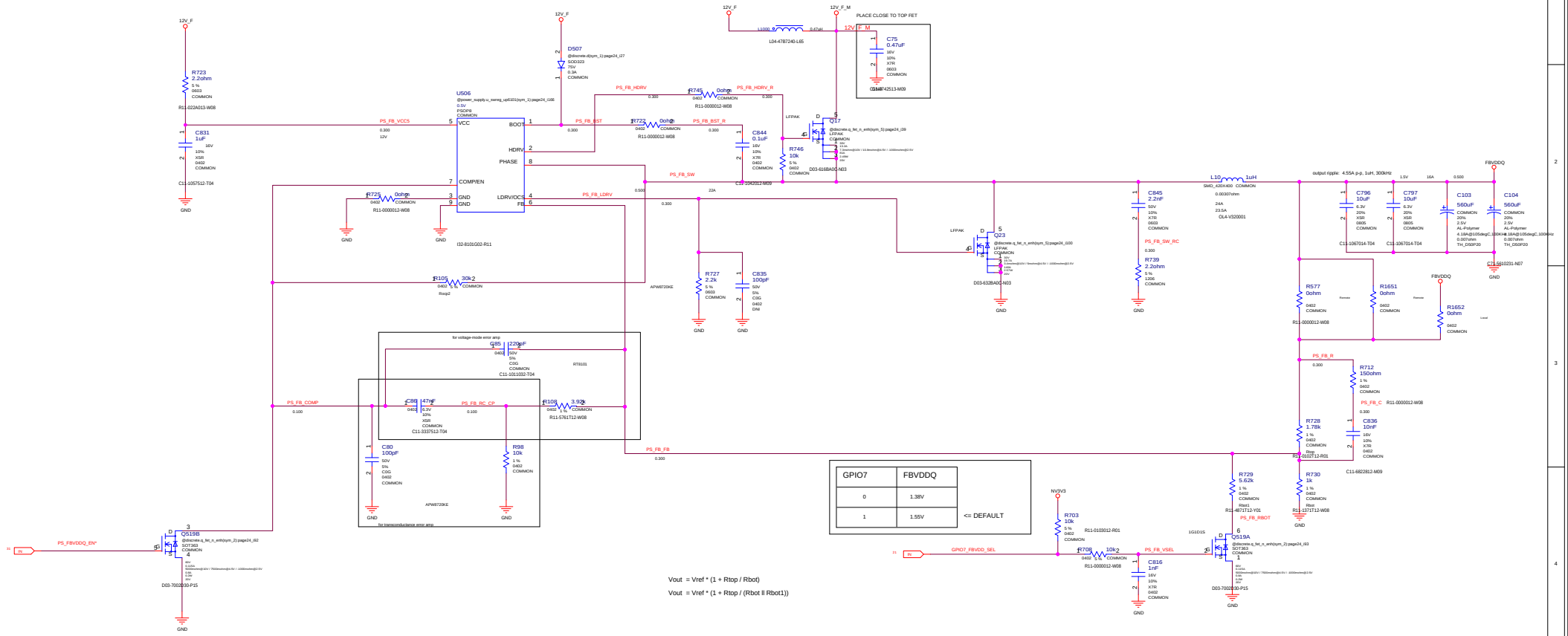
PS: FBVDDQ



GPIO7	FBVDDQ	
0	1.38V	
1	1.55V	<= DEFAULT

Vout = Vref * (1 + Rtop / Rbot)

Vout = Vref * (1 + Rtop / (Rbot ll Rbot1))

	Vref	Vref accuracy	Fosc	GPIO7	
APW8720KE	0.5V	1%	300kHz	0	Vout = .5*(1+1.78k/1k) = 1.39V
				1	Vout = .5*(1+1.78k/(1k|5.62k)) = 1.548V
RT8101GSP	0.8V	1%	300kHz	0	Vout = .8*(1+1k/1.37k) = 1.384V
				1	Vout = .8*(1+1k/(1.37k|4.87k)) = 1.549V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: FBVDDQ

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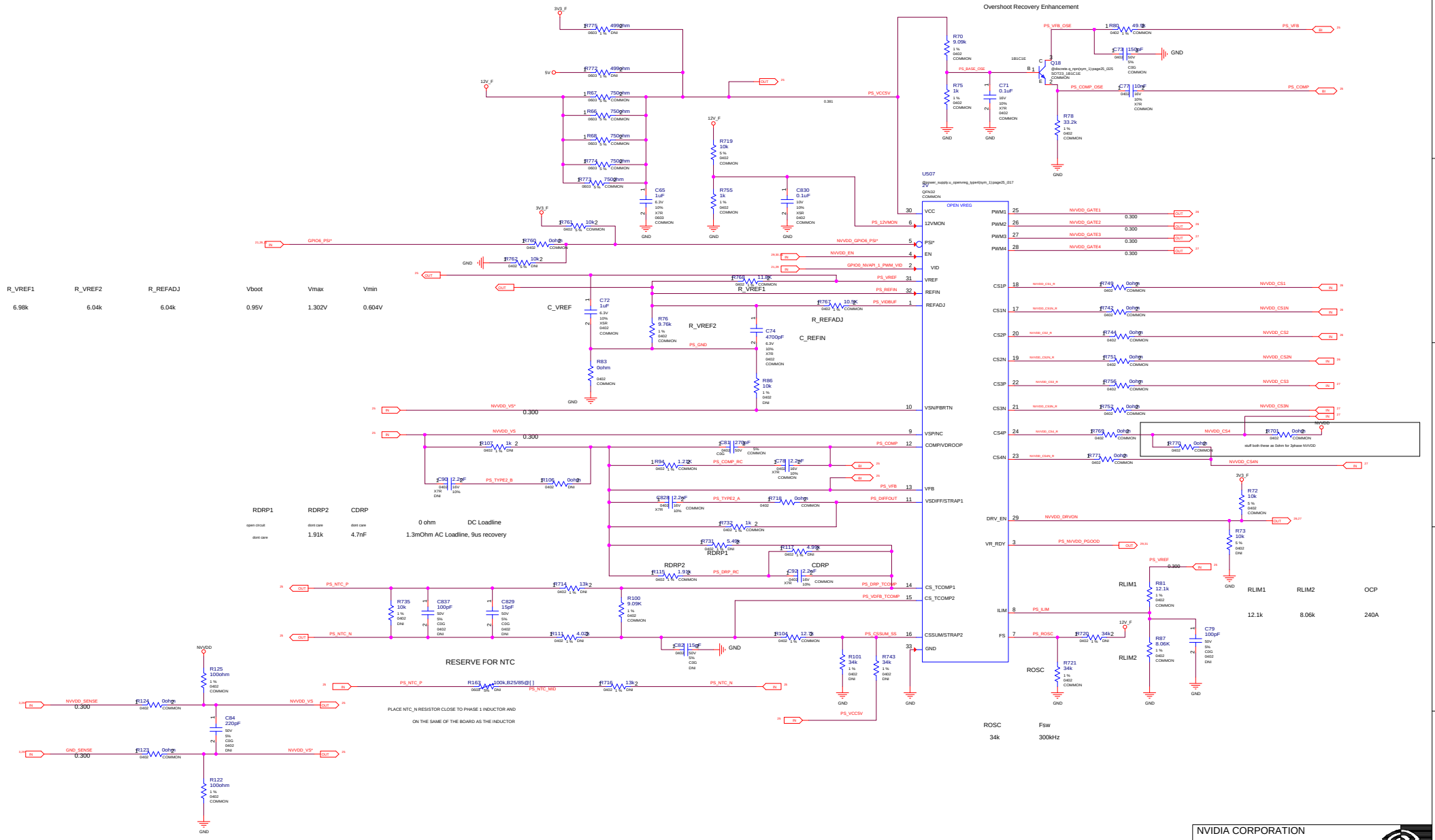
PS: NVVDD Controller



R_VREF1	R_VREF2	R_REFADJ	Vboot	Vmax	Vmin
6.98k	6.04k	6.04k	0.95V	1.302V	0.604V

RDRP1	RDRP2	CDRP		
open circuit	dont care	dont care	0 ohm	DC Loadline
dont care	1.91k	4.7nF	1.3mOhm AC Loadline, 9us recovery	

RLIM1	RLIM2	OCP
12.1k	8.06k	240A

ROSC	Fsw
34k	300kHz

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Controller OVR4 option

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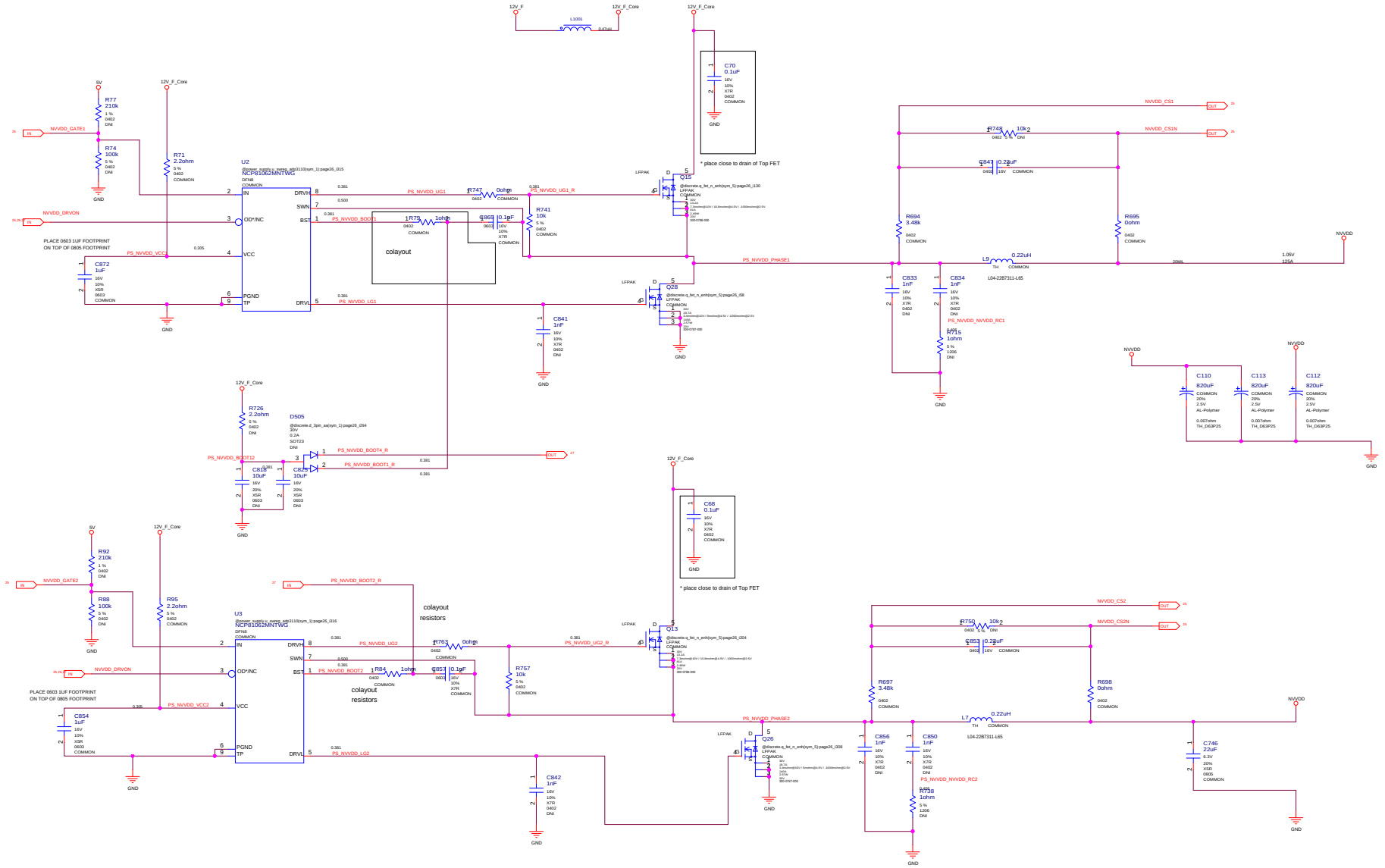
PS: NVVDD Phase 1,2



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 1,2

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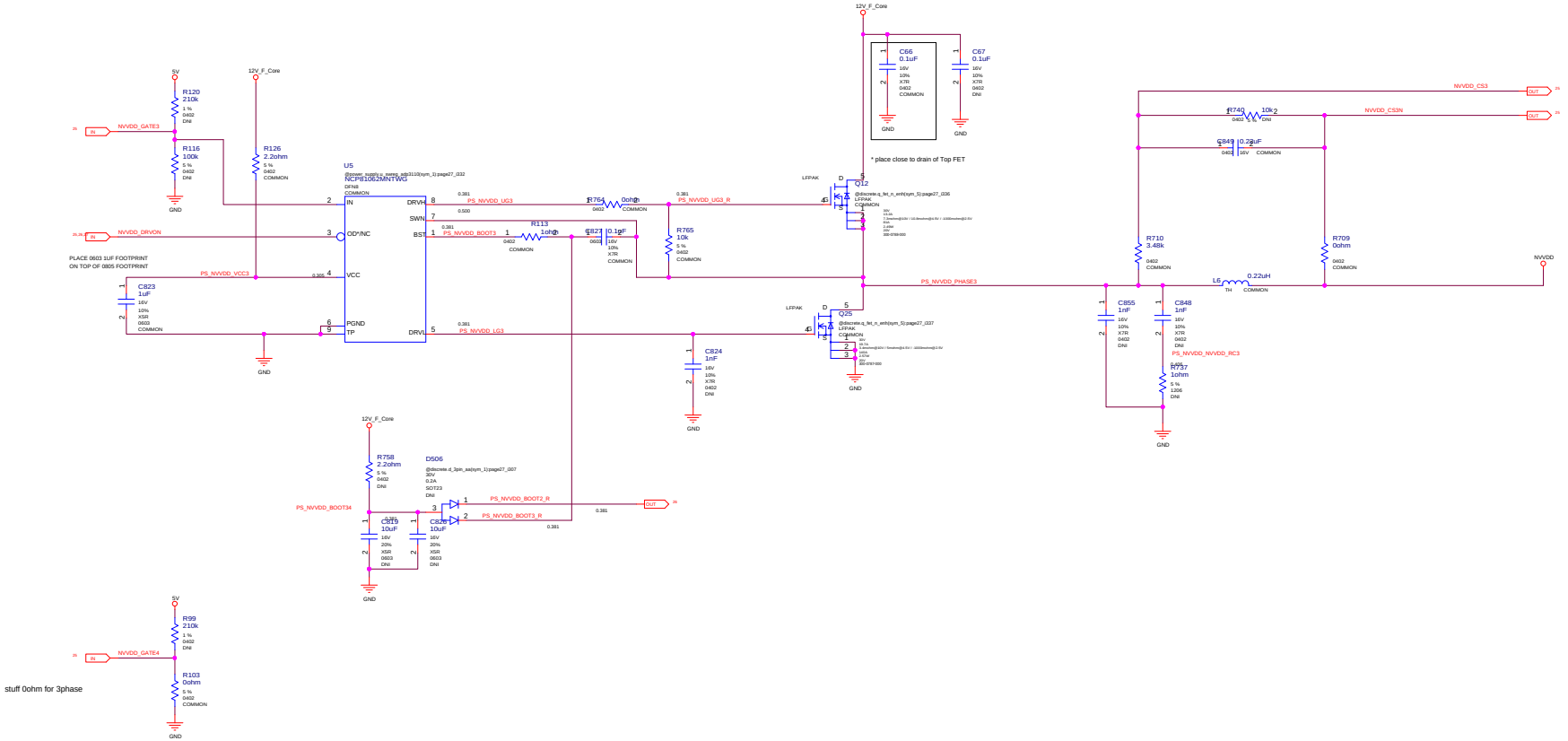
PS: NVVDD Phase 3,4



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 3,4

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[RESERVED]

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	[RESERVED]

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PS: NVVDD OVR2+1 POWER

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD OVR2+1 option

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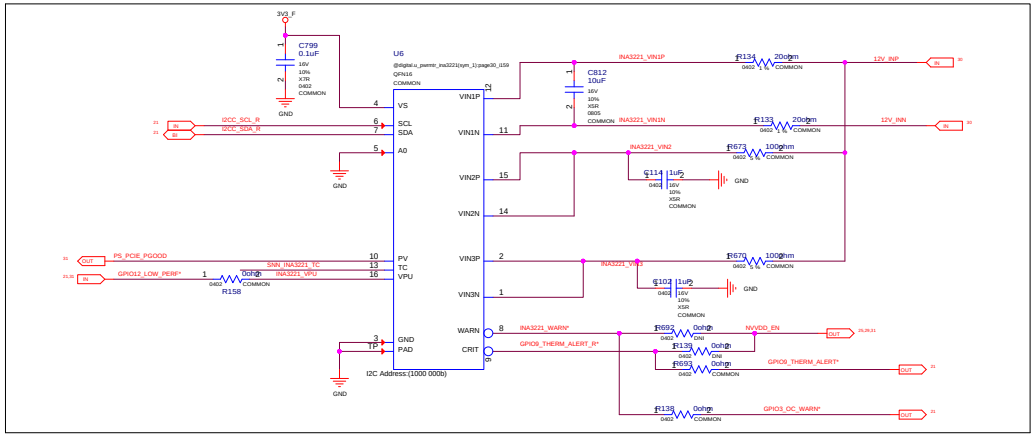
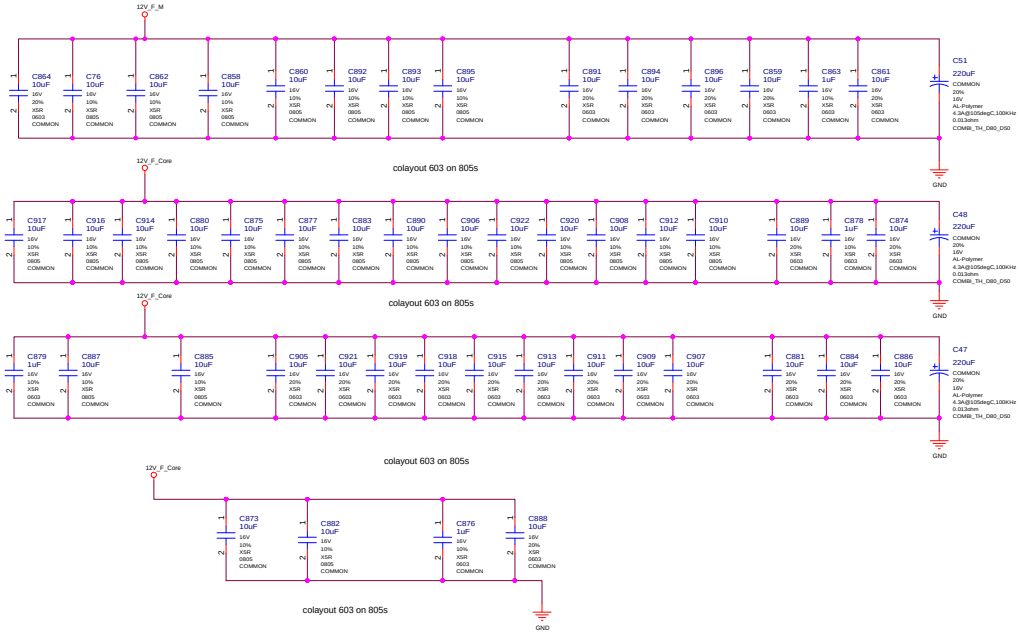
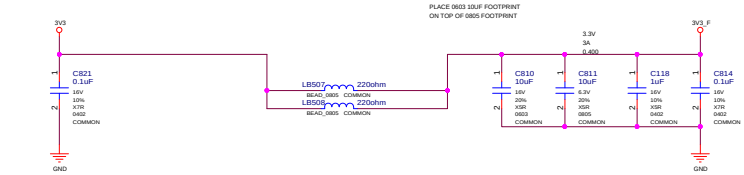
PS: Inputs, Filtering, and Monitoring



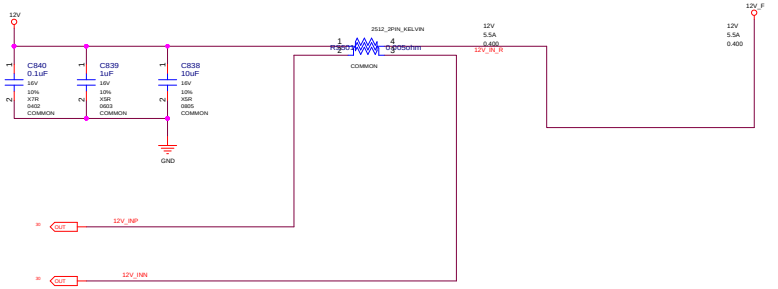


C76 must be low profile component if stuffed with FET heatsink

PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

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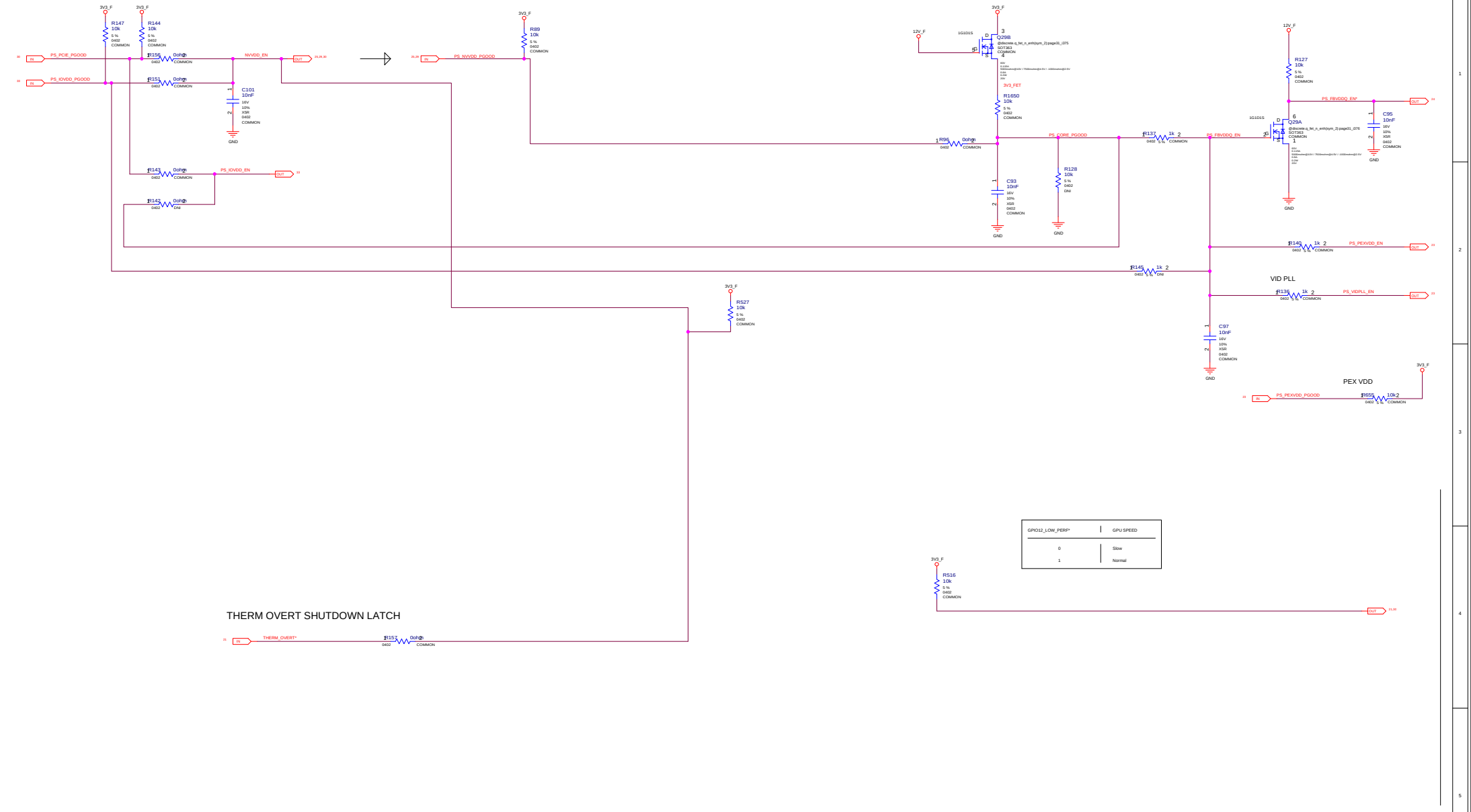
PS: Sequence and Shutdown



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Sequence and Shutdown

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LEDs

IFP_IOVDD (backdrive prevention)

GeForce Logo LED

LED HEADER
(C0MM0N)

SLI LED and Quadro LED

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	LEDs

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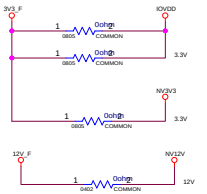
PS: IOVDD, NV3V3, NV12V

OVR0 1.8V REGULATOR. STUFF FOR 16nm

Special Note:
1. Place [C_OUT] close to [L_OUT]
2. Use local FB sense (refer to design guide for details)
3. Place PLL/IO filter ferrite bead to the same position as FB local sense point

BYPASS. STUFF FOR 28nm



Gated rails required for 16nm

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: IOVDD Regulator

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Mechanical: Bracket/Thermal Solution

FET HS

Brackets:

MT1
MT_Hole_0.136 TM 5.5 BM 7.0

GND

SCREW206
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

E41-1304008-P65

HDMI_FEE
HDMI_FEE
Lenovo HDMI FEE
Y01-RHDMI03-000

EM1
1
GND
E23-5611010-RH

PCB1
PCB
142-11310-1000-A01-1
P80-0V32080-T53

For DP Connector

DP SCREWS with top tab

SCREW204
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

E43-1204011-P65

For DVI Connector

DVI/DVI SCREWS with top tab

SCREW202
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

E42-5047012-A43

SCREW203
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

E42-5047012-A43

MEC3
holes_g301
MEC4
holes_g301
MEC5
holes_g301
MEC6
holes_g301
4
GND

Reserve J3 - J20 for Impedance check

DNI
J14
X_PIN1*2
GND

MEM Data
FBC_D<9>
Top
0.126MM / 47ohm +/- 10%
Reference L2 GND

DNI
J15
X_PIN1*2
GND

SLi Data
MIOA_D7
L3
0.101MM / 52ohm +/- 10%
Reference L2 GND

DNI
J17
3 1
4 2
impedence
GND

MEM CLK
FBA_CLK1/FBA_CLK1*
L3_Inner
0.103mm/0.101mm / 80ohm +/- 10%
Reference L2_Inner GND

DNI
J19
3 1
4 2
impedence
GND

HDMI TMDS signals
IFPC_TXC/IFPC_TXC*
L4_Inner
0.104mm/0.26mm / 95ohm +/- 10%
Reference L5_Inner GND

DNI
J13
X_PIN1*2
GND

RGB signal
DACA_GREEN_DVI
Bottom
0.102MM / 52ohm +/- 10%
Reference L5_Inner GND

DNI
J16
X_PIN1*2
GND

MEM Address
FBC_CMD<4>
L4
0.127MM / 47ohm +/- 10%
Reference L5 GND

DNI
J18
3 1
4 2
impedence
GND

PEX_PCEI / DVI IFPEF
PEX_RX13/PEX_RX13* IFPEF_TXC_C*_R/IFPEF_TXC_C_R
TOP
0.101MM/0.123MM / 90ohm +/- 10%
Reference L2_Inner GND

DNI
J20
3 1
4 2
impedence
GND

PEX_PCEI / DVI IFPAB
PEX_TX6/PEX_TX6* IFPAB_TXD1_C*_R/IFPAB_TXD1_C_R
Bottom
0.101MM/0.123MM / 90ohm +/- 10%
Reference L5_Inner GND

1
FM1
SW_FB
F_PAD_X

FM2
SW_FB
F_PAD_X

FM3
SW_FB
F_PAD_X

FM4
SW_FB
F_PAD_X

FM5
SW_FB
F_PAD_X

FM6
SW_FB
F_PAD_X

FM7
SW_FB
F_PAD_X

FM8
SW_FB
F_PAD_X

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MECH: Bracket/Thermal

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