PCI-EXPRESS EDGE CONNECTOR

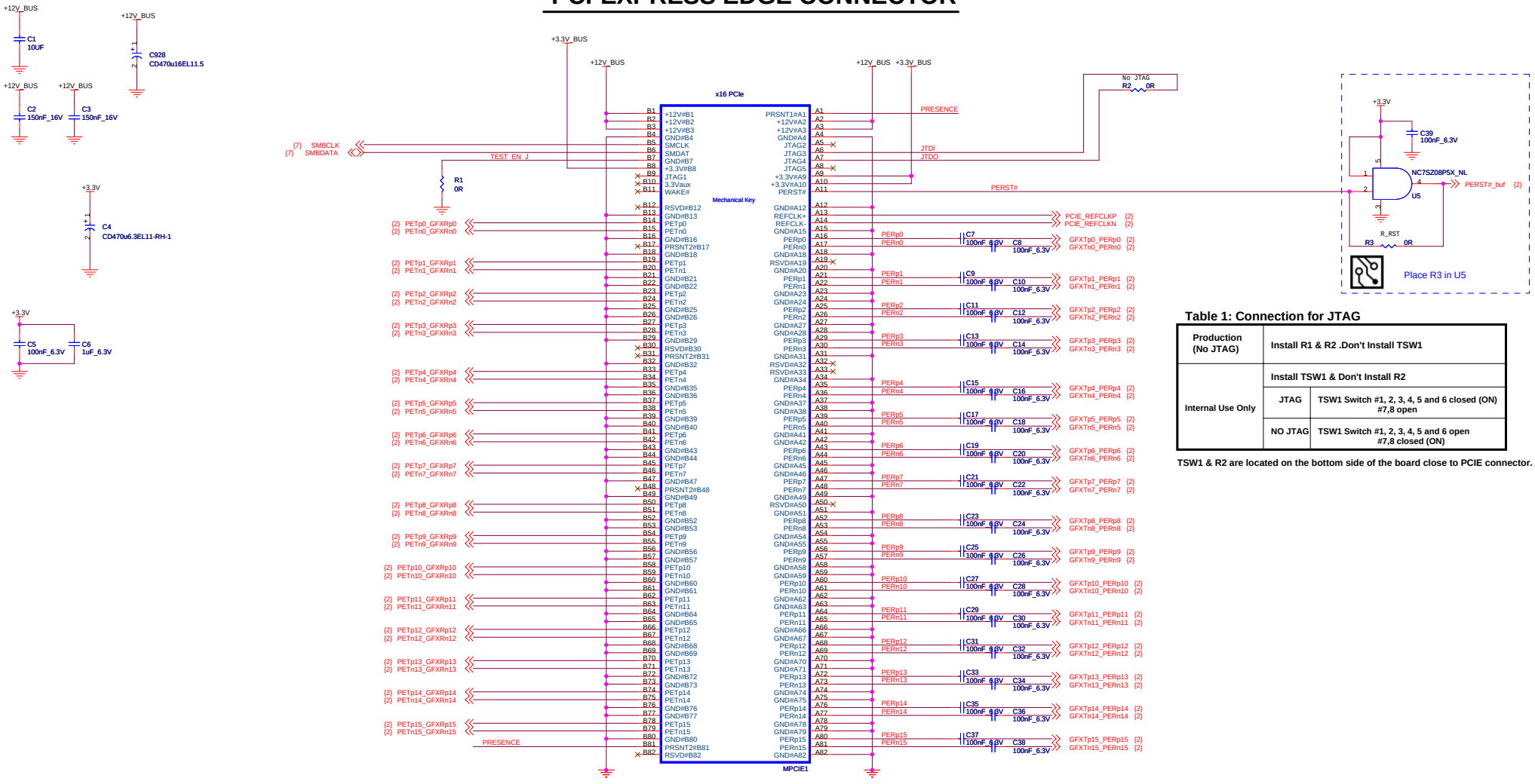

Table 1: Connection for JTAG

Production (No JTAG)	**Install R1 & R2 .Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #7,8 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #7,8 closed (ON)**

TSW1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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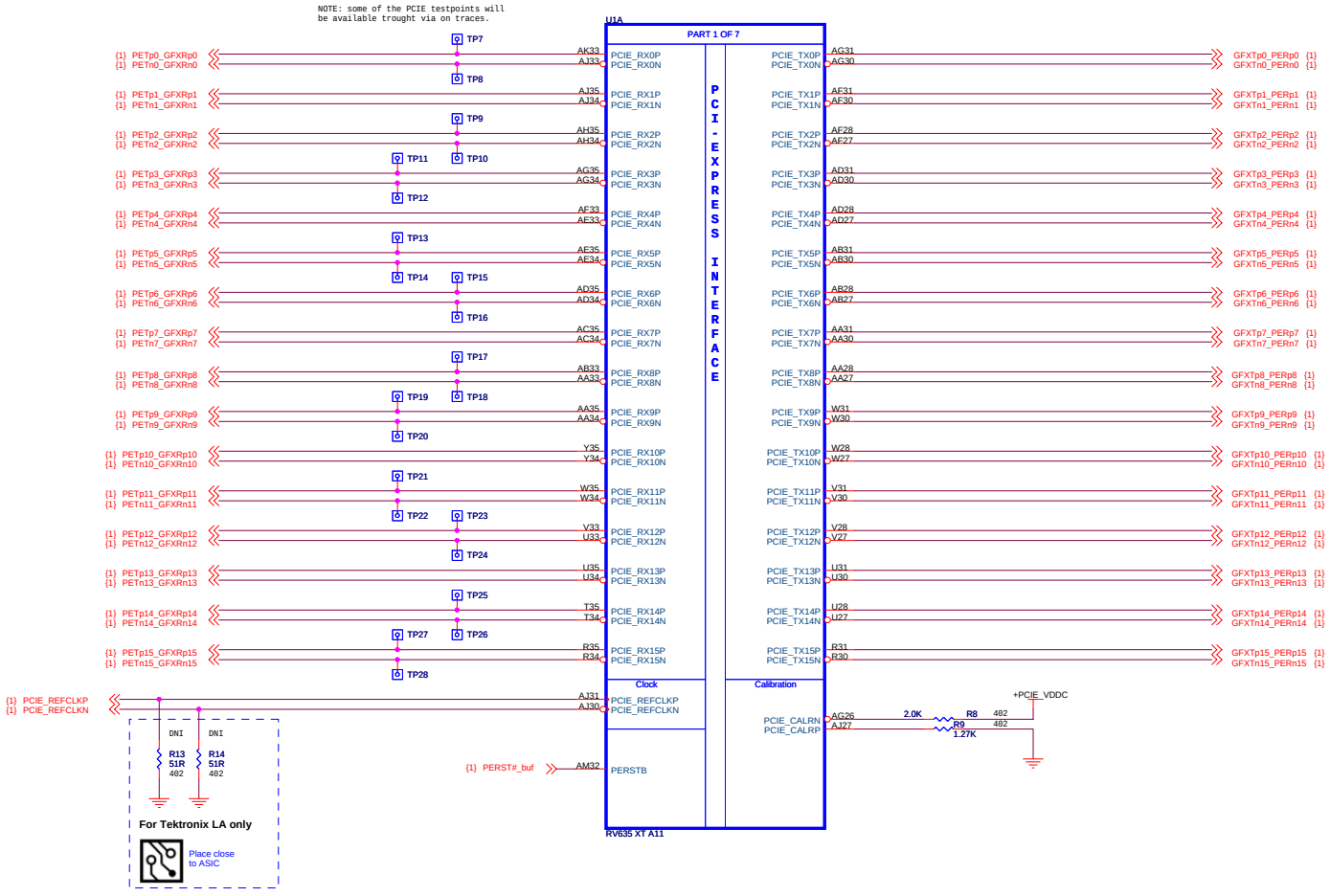
Title RV635 DDR2 - PCI-E Edge Connector

Doc No. 105-B381xx-00A



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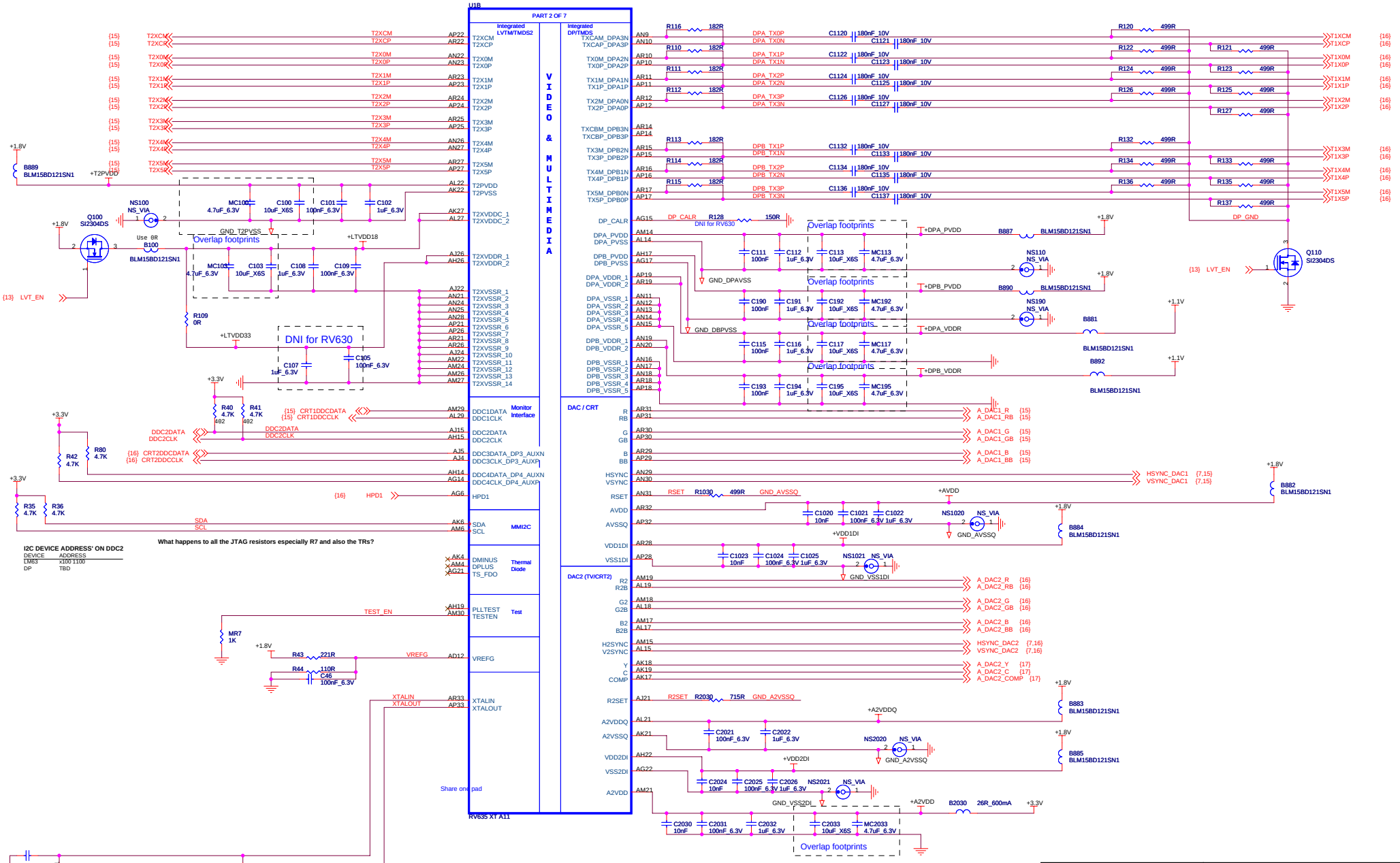
Title	RV635 DDR2 - ASIC PCIE_Interface
Doc No.	105-B381xx-00A

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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Title	RV635 DDR2 - ASIC MAIN
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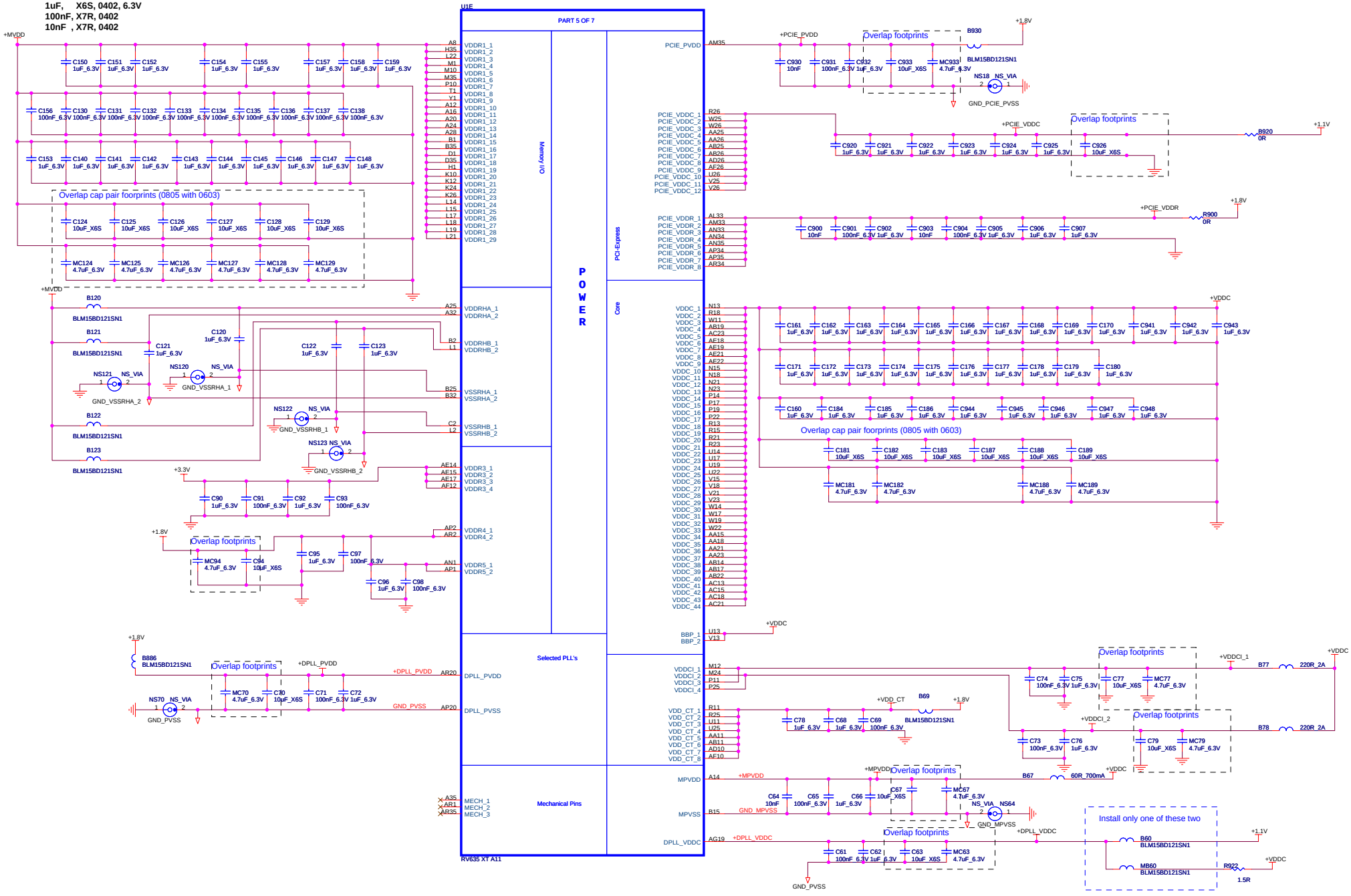
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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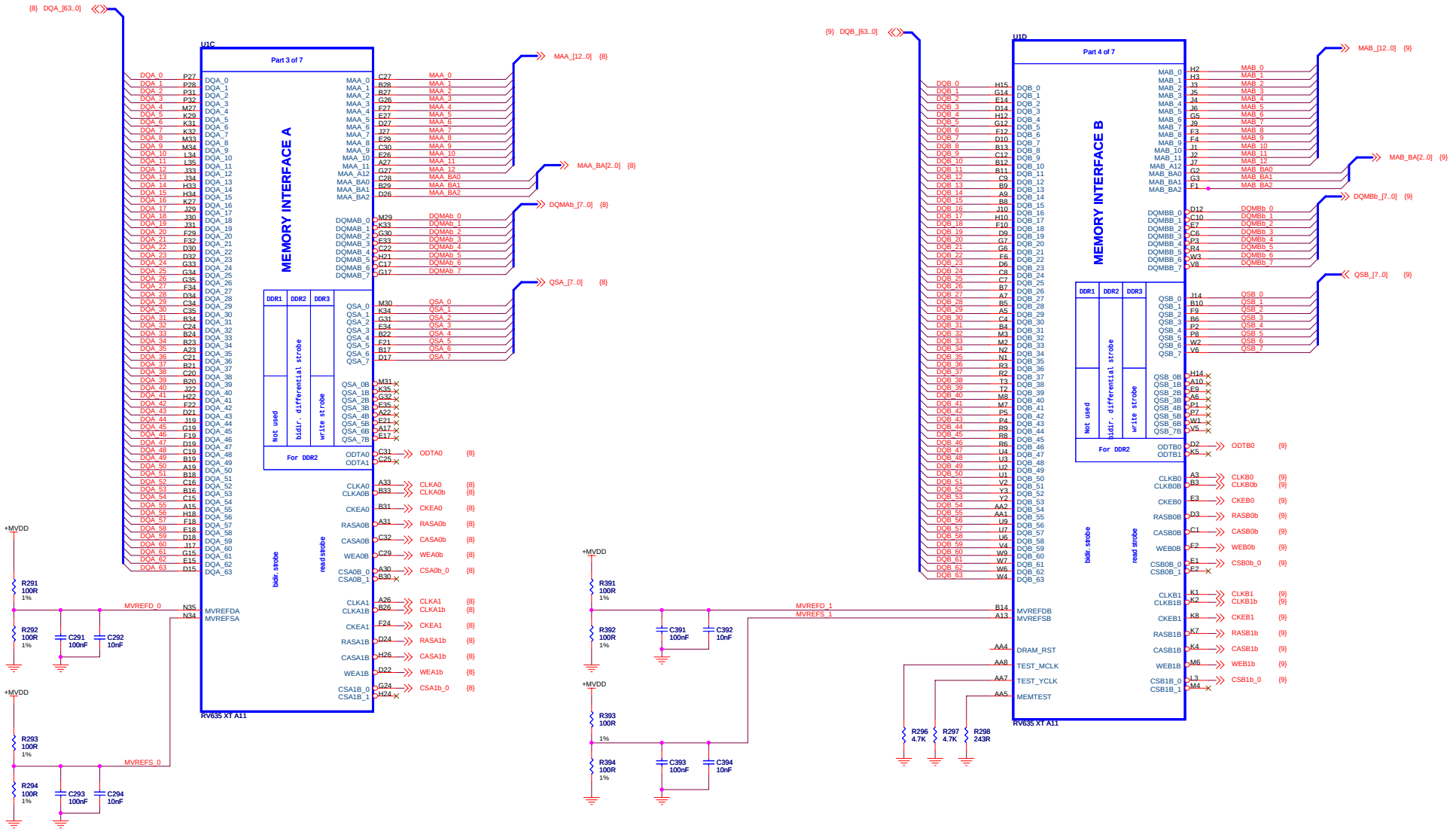
Title	RV635 DDR2 - ASIC Power
Doc No.	105-B381xx-00A



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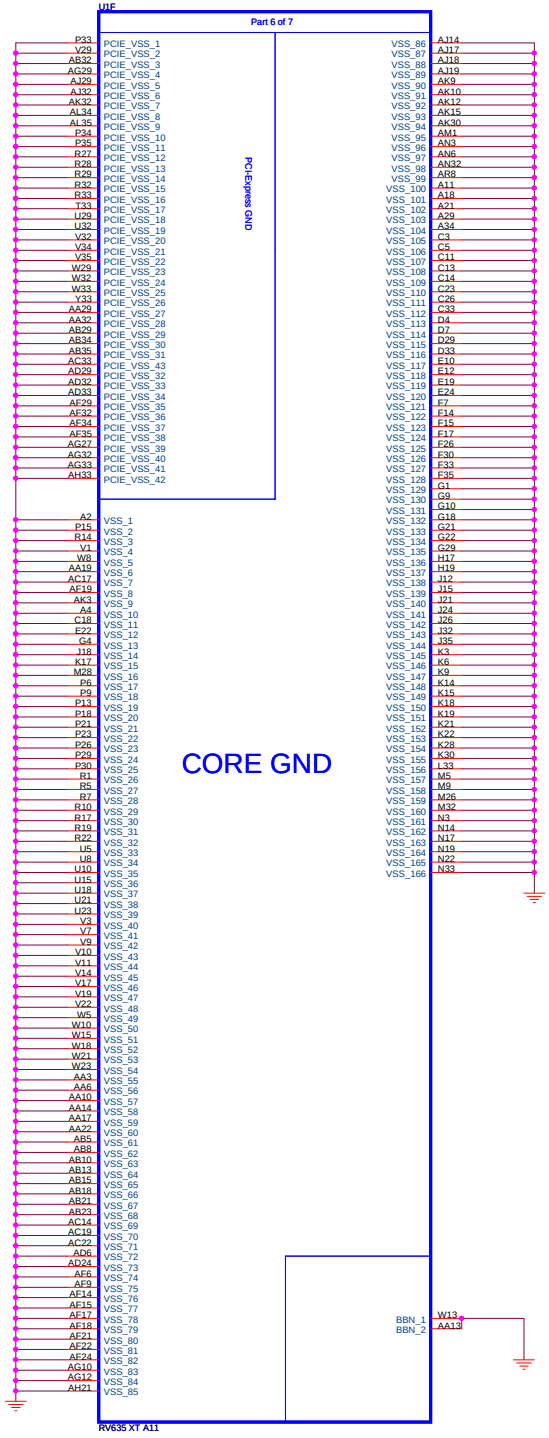
Title	RV635 DDR2 - ASIC Memory Interface (Channel A & B)
Doc No.	105-B381xx-00A



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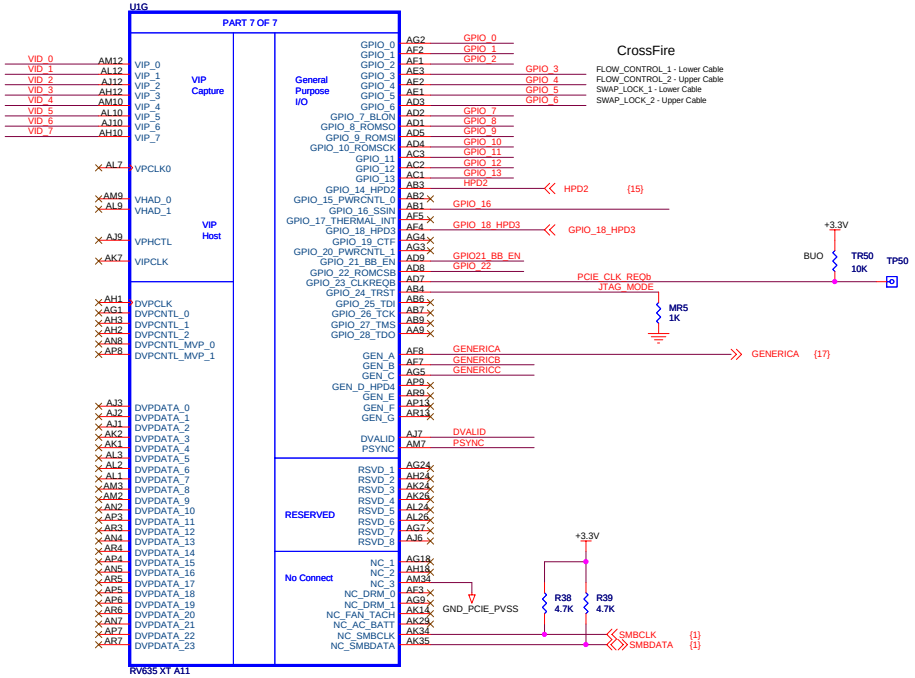
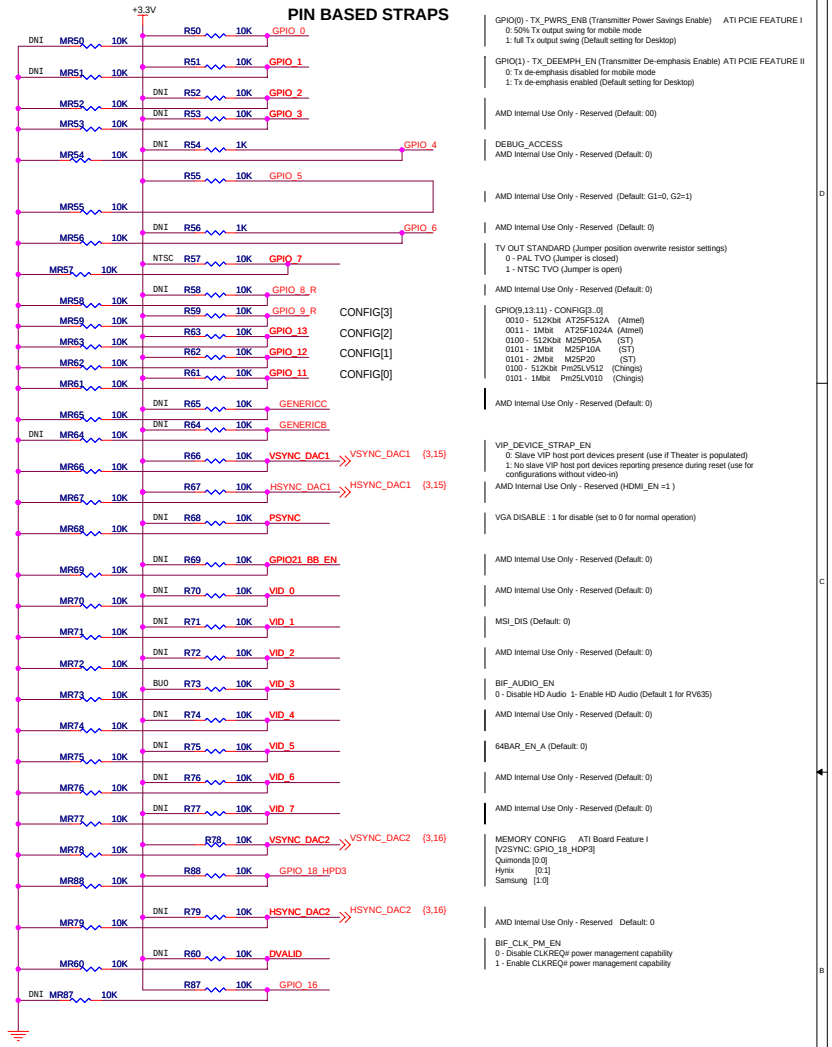
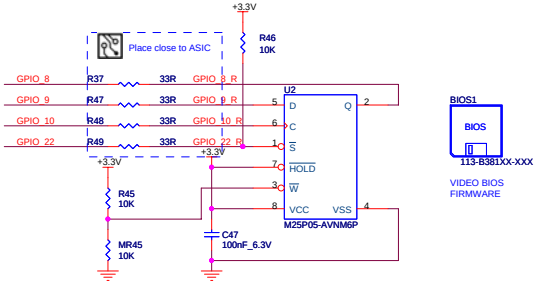
Title RV635 DDR2 - ASIC Grounds

Doc No. 105-B381xx-00A







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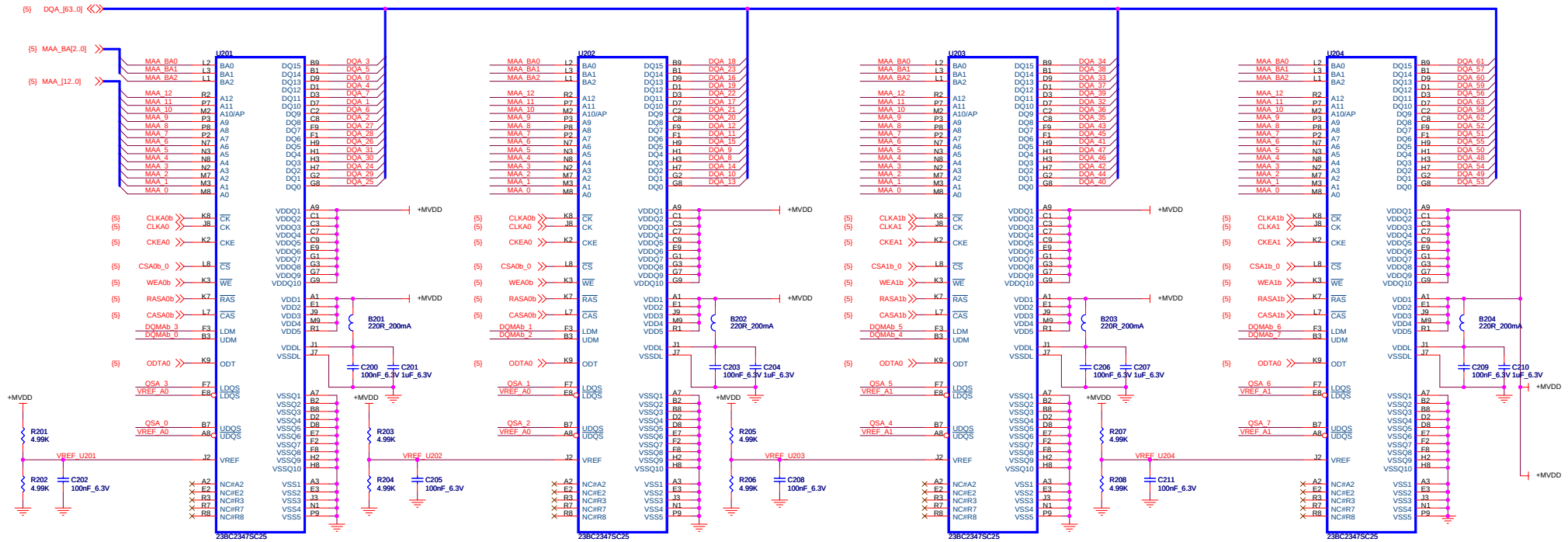
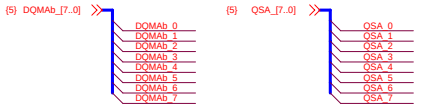
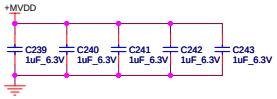
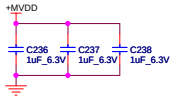
Title RV635 DDR2 - ASIC DVO & GPIOs Doc No. 105-B381xx-00A

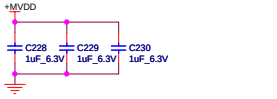
CHANNEL A: 128MB/256MB DDR2

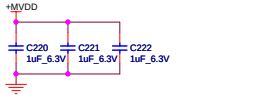


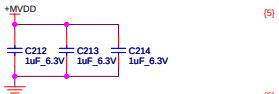


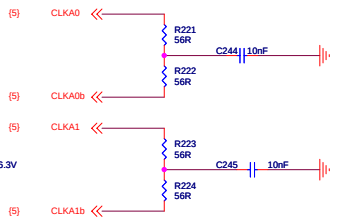


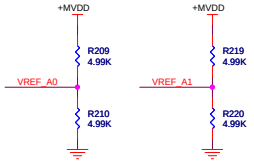












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Title	RV635 DDR2 - MEM CH A
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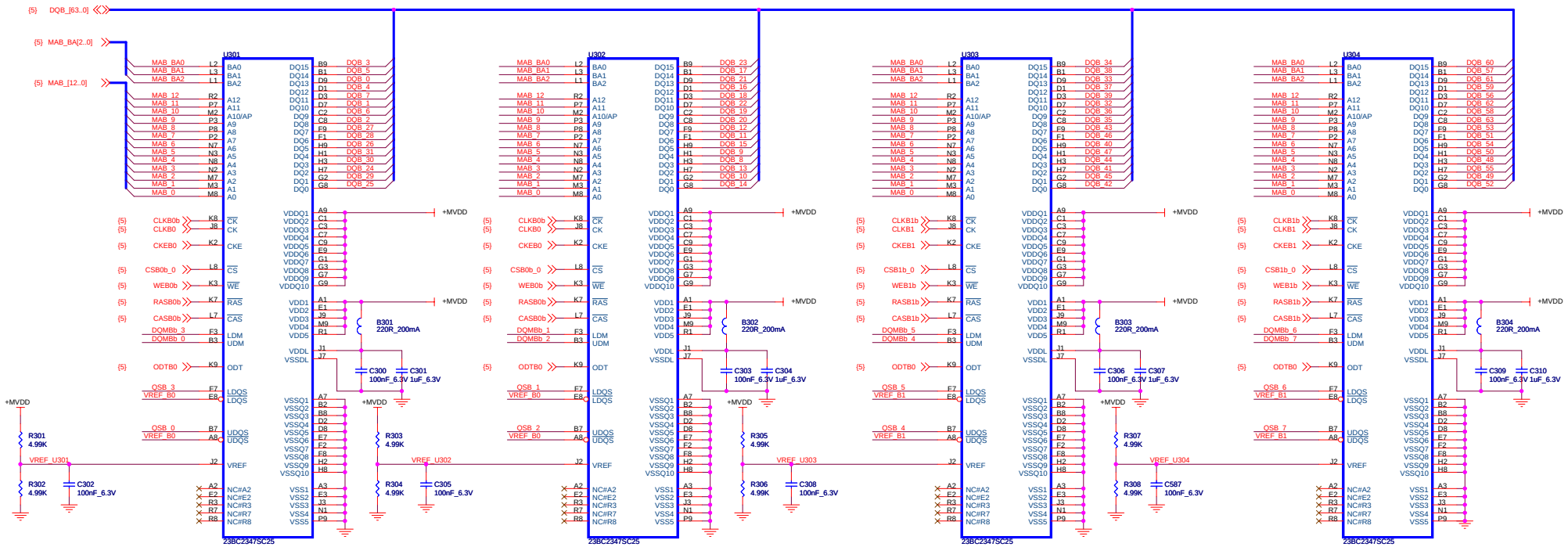
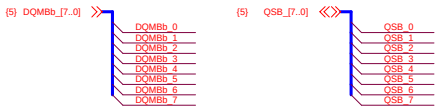
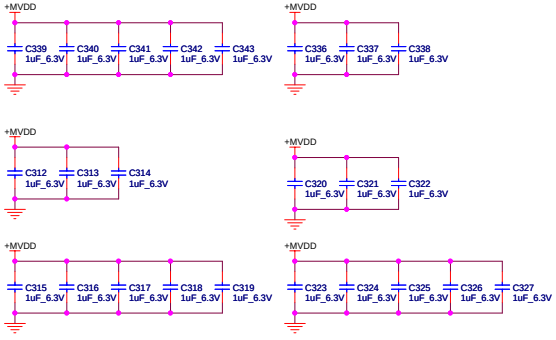
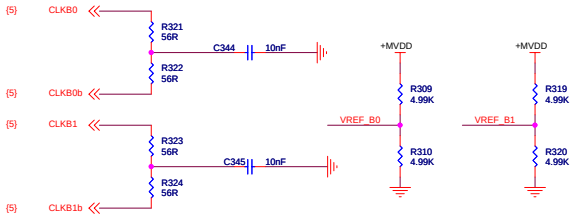
CHANNEL B: 128MB/256MB DDR2









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Title	RV635 DDR2 - MEM CH B
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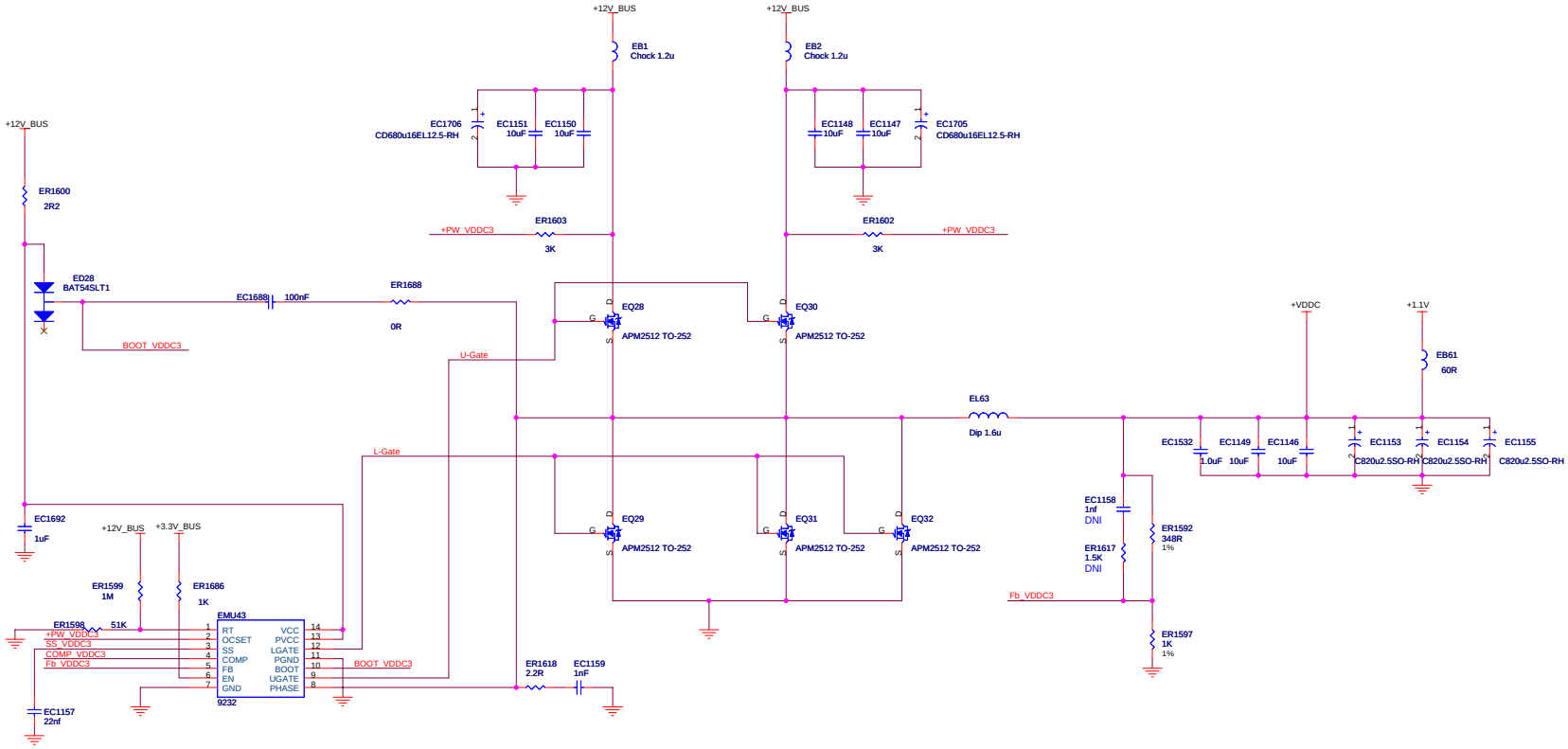
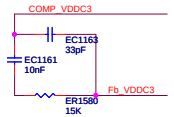
CORE REGULATOR VDDC



+VDDC=0.8*(1+(ER1592 / ER1597))

Compensation Circuit



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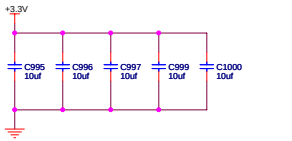
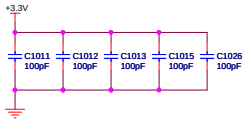
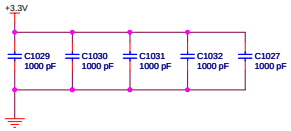
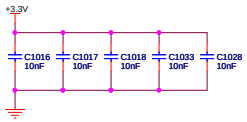
Title	RV635 DDR2 - VDDC SMPS 01
Doc No.	105-B381xx-00A









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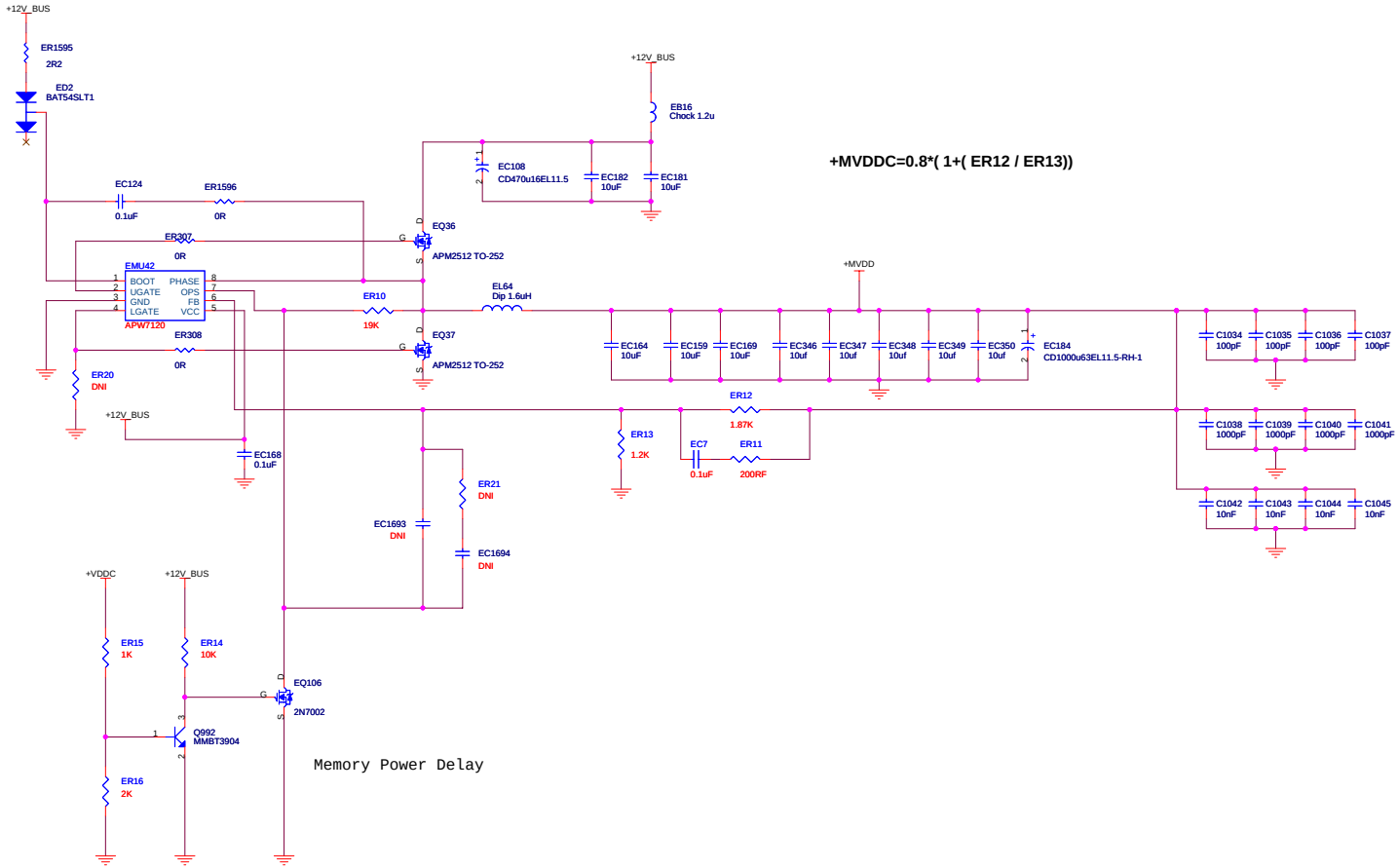
Title RV635 DDR2 - VDDC SMPS 02

Doc No. 105-B381xx-00A



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Title	RV635 DDR2 - MVDD SMPS 01
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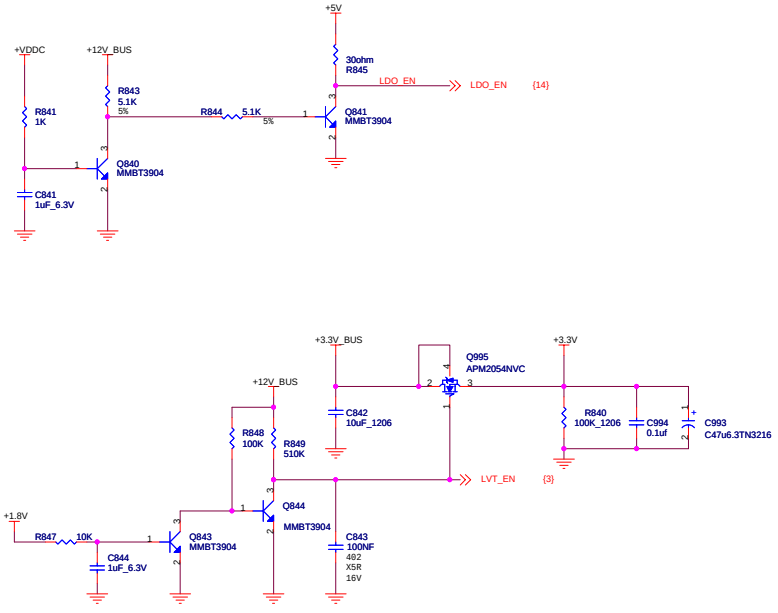
Power up Sequencing



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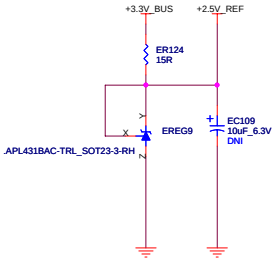
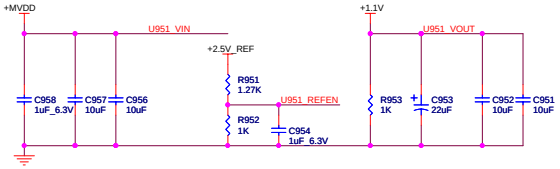
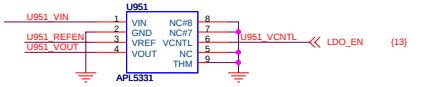
Title: RV635 DDR2 - Power Management | Doc No. 105-B381xx-00A

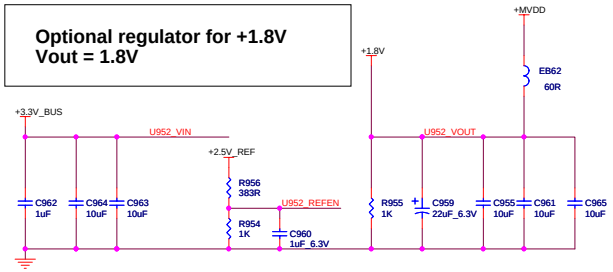


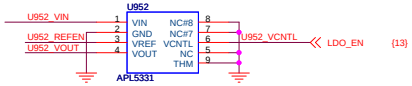
Optional regulator for +1.1V
Vout = 1.1V

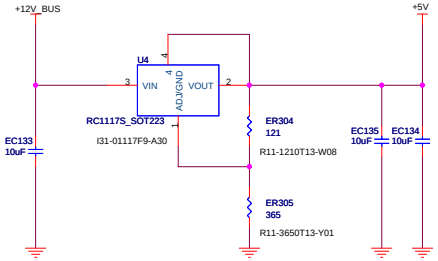




Optional regulator for +1.8V
Vout = 1.8V







Vout=1.25V* [1+(ER305/ER304)]

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Title RV635 DDR2 - Linear Regulators

Doc No. 105-B381xx-00A

See BOM for qualified filters

{3} A_DAC1_R — R1001 75R — C1004 8.0pF — L1001 47nH — A_R_DAC1_M — C1001 12pF_50V — L1004 36NH

{3} A_DAC1_RB — R1027 37.4R

{3} A_DAC1_G — R1002 75R — C1005 8.0pF — L1002 47nH — A_G_DAC1_M — C1002 12pF_50V — L1005 36NH

{3} A_DAC1_GB — R1028 37.4R

{3} A_DAC1_B — R1003 75R — C1006 8.0pF — L1003 47nH — A_B_DAC1_M — C1003 12pF_50V — L1006 36NH

{3} A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

+3.3V — BAT54SLT1 ED62 — BAT54SLT1 ED63 — BAT54SLT1 ED64

+5V — ED71 BAT54SLT1 — ED70 BAT54SLT1 — ED69 BAT54SLT1 — ED68 BAT54SLT1

+5V — EF1 1.5A — +5V_VESA

C1010 104pF

MJ1001 — G3179C219-005

1	R
2	G
3	B
11	MS0
12	MS1
4	MS2
15	MS3
9	NC
13	HS
14	VS
5	VSS
6	VSS#6
7	VSS#7
8	VSS#8
10	VSS#10
16	CASE
17	CASE#17

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

{3} CRT1DDCDATA — +3.3V — R1004 10K — +5V — R1005 2.2K — BSH111 Q1001 — DDCDATA_DAC1_5V — R1006 33R — DDCDATA_DAC1_R

{3} CRT1DDCCLK — +3.3V — R1007 10K — +5V — R1008 2.2K — BSH111 Q1002 — DDCCLK_DAC1_5V — R1009 33R — DDCCLK_DAC1_R

+5V — C1999 100nF_6.3V

{3,7} HSYNC_DAC1 — U1999A SN74HCT125D — HSYNC_DAC1_B — R1010 10R — HSYNC_DAC1_R

SN74HCT125D U1999B

{3,7} VSYNC_DAC1 — VSYNC_DAC1_B — R1011 10R — VSYNC_DAC1_R

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

+5V_VESA

Q1021 MMBT3904 — +3.3V — R1022 10K — {7} HPD2 — R1023 10K — HPD_DVI2

{3} T2X2M	R1012 0R	R102 100R	
{3} T2X2P	R1013 0R		
		R104 100R	
{3} T2X4M	R1014 0R		
{3} T2X4P	R1015 0R		
DDCCLK_DAC1_R			
DDCDATA_DAC1_R			
VSYNC_DAC1_R			
{3} T2X1M	R1016 0R		
{3} T2X1P	R1017 0R	R101 100R	
{3} T2X3M	R1018 0R		
{3} T2X3P	R1019 0R	R103 100R	
{3} T2X0M	R1020 0R		
{3} T2X0P	R1021 0R	R100 100R	
{3} T2X5M	R1024 0R		
{3} T2X5P	R1025 0R	R105 100R	
{3} T2XCP	R1026 0R		
{3} T2XCM	R1031 0R	R106 100R	
A_R_DAC1_F			
A_G_DAC1_F			
A_B_DAC1_F			
HSYNC_DAC1_R			

J1001 — DVI_CONNECTOR

25	CASE
1	TMDS Data2-
2	TMDS Data2+
3	TMDS Data2/4 Shield
4	TMDS Data4-
5	TMDS Data4+
6	DDC Clock
7	DDC Data
8	Analog VSYNC
9	TMDS Data1-
10	TMDS Data1+
11	TMDS Data1/3 Shield
12	TMDS Data3-
13	TMDS Data3+
14	+5V Power
15	GND (for +5V)
16	Hot Plug Detect
17	TMDS Data0-
18	TMDS Data0+
19	TMDS Data0/5 Shield
20	TMDS Data5-
21	TMDS Data5+
22	TMDS Clock Shield
23	TMDS Clock+
24	TMDS Clock-
C1	Analog Red
C2	Analog Green
C3	Analog Blue
C4	Analog HYNC
C5	Analog GND
C6	Analog GND#C6
26	CASE#26
27	CASE#27
28	CASE#28
29	CASE#29
30	CASE#30

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Title: RV635 DDR2 - DAC1&TMDS2 — Doc No. 105-B381xx-00A

See BOM for qualified filters

{3} A_DAC2_R
{3} A_DAC2_RB
R2001 75R 402
R2027 37.4R
C2004 8.0pF 402
C2001 402 12pF_50V
L2001 47nH
L2004 36NH
A_R_DAC2_M

{3} A_DAC2_G
{3} A_DAC2_GB
R2002 75R 402
R2028 37.4R
C2005 8.0pF 402
C2002 402 12pF_50V
L2002 47nH
L2005 36NH
A_G_DAC2_M

{3} A_DAC2_B
{3} A_DAC2_BB
R2003 75R 402
R2029 37.4R
C2006 8.0pF 402
C2003 402 12pF_50V
L2003 47nH
L2006 36NH
A_B_DAC2_M

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

+3.3V
BAT54SLT1 ED67
BAT54SLT1 ED66
BAT54SLT1 ED65
+5V_VESA

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R

MJ2001
1 R
2 G
3 B
11 MS0
12 MS1
4 MS2
15 MS3
9 NC
13 HS
14 VS
5 VSS
6 VSS#6
7 VSS#7
8 VSS#8
10 VSS#10
16 CASE
17 CASE#17
G3179C219-005

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

+5V
ED75 BAT54SLT1
ED74 BAT54SLT1
ED73 BAT54SLT1
ED72 BAT54SLT1

+3.3V
DNI for RV635
R2004 24.3K
{3} CRT2DDCDATA
Q2001 BSH111
+5V
R2005 2.2K 402 DDCDATA_DAC2_5V
R2006 33R 402 DDCDATA_DAC2_R

RV635: no pull up on 3.3V, 2.2K pull up on 5V
RV630: 24.3K pull up on 3.3V, 19.1K on 5V

+3.3V
DNI for RV635
R2007 24.3K
{3} CRT2DDCCLK
Q2002 BSH111
+5V
R2008 2.2K 402 DDCCLK_DAC2_5V
R2009 33R 402 DDCCLK_DAC2_R

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
Hardware	Mechanical Key	1A max	1A max	1A max	
Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

{3,7} HSYNC_DAC2
U1999C SN74HCT125D
HSYNC_DAC2_B
R2010 10R 402 HSYNC_DAC2_R

{3,7} VSYNC_DAC2
U1999D SN74HCT125D
VSYNC_DAC2_B
R2011 10R 402 VSYNC_DAC2_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

+3.3V
Q2021 MMBT3904
R2022 10K
{3} HPD1
R2023 10K
HPD_DVI1

+5V_VESA
J2001
25 CASE
1 TMDS Data2-
2 TMDS Data2+
3 TMDS Data2/4 Shield
4 TMDS Data4-
5 TMDS Data4+
6 DDC Clock
7 DDC Data
8 Analog VSYNC
9 TMDS Data1-
10 TMDS Data1+
11 TMDS Data1/3 Shield
12 TMDS Data3-
13 TMDS Data3+
14 +5V Power
15 GND (for +5V)
16 Hot Plug Detect
17 TMDS Data0-
18 TMDS Data0+
19 TMDS Data0/5 Shield
20 TMDS Data5-
21 TMDS Data5+
22 TMDS Clock Shield
23 TMDS Clock+
24 TMDS Clock-
C1 Analog Red
C2 Analog Green
C3 Analog Blue
C4 Analog HYNC
C5 Analog GND
C6 Analog GND#C6
26 CASE#26
27 CASE#27
28 CASE#28
29 CASE#29
30 CASE#30
DVI_CONNECTOR

{3} T1X2M
{3} T1X2P
{3} T1X4M
{3} T1X4P
DDCCLK_DAC2_R
DDCDATA_DAC2_R
VSYNC_DAC2_R
{3} T1X1M
{3} T1X1P
{3} T1X3M
{3} T1X3P
{3} T1X0M
{3} T1X0P
{3} T1X5M
{3} T1X5P
{3} T1XCP
{3} T1XCM
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
HSYNC_DAC2_R

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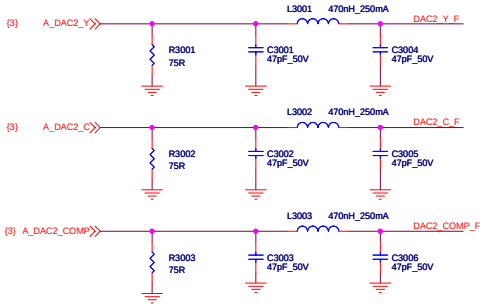
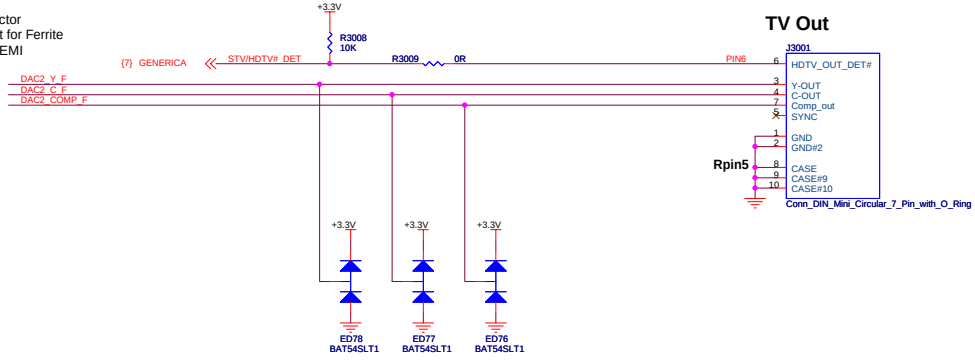
Sheet 16 of 21
Title RV635 DDR2 - DAC2/TMDS1
Doc No. 105-B381xx-00A



Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI



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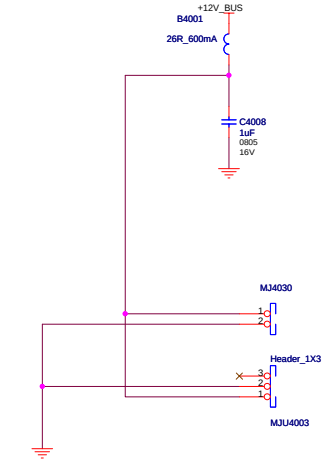
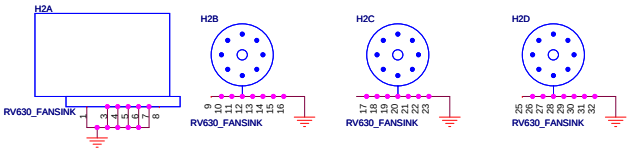
Title RV635 DDR2 - TVO

Doc No. 105-B381xx-00A





See BOM for qualified option.

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Title: RV635 DDR2 - Thermal Management | Doc No. 105-B381xx-00A

DVI/DVI SCREWS with top tab

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

DNI

SK1
SOCKET_880

RV635 Socket

PCB1
PCB
109-GN982-00A

ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET
8020046100G

Need New Bracket

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

MT1
MT_Hole_0.136_in.

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM4 SW_FB
FM5 SW_FB
FM6 SW_FB
FM7 SW_FB
FM8 SW_FB

J1
X_PIN1*2

+MVDD

J4
X_PIN1*2

J2
3 1
4 2
impedence

+MVDD

J5
3 1
4 2
impedence

+MVDD

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Sheet 19 of 21
Title RV635 DDR2 - Mechanical
Doc No. 105-B381xx-00A

<Variant Name>

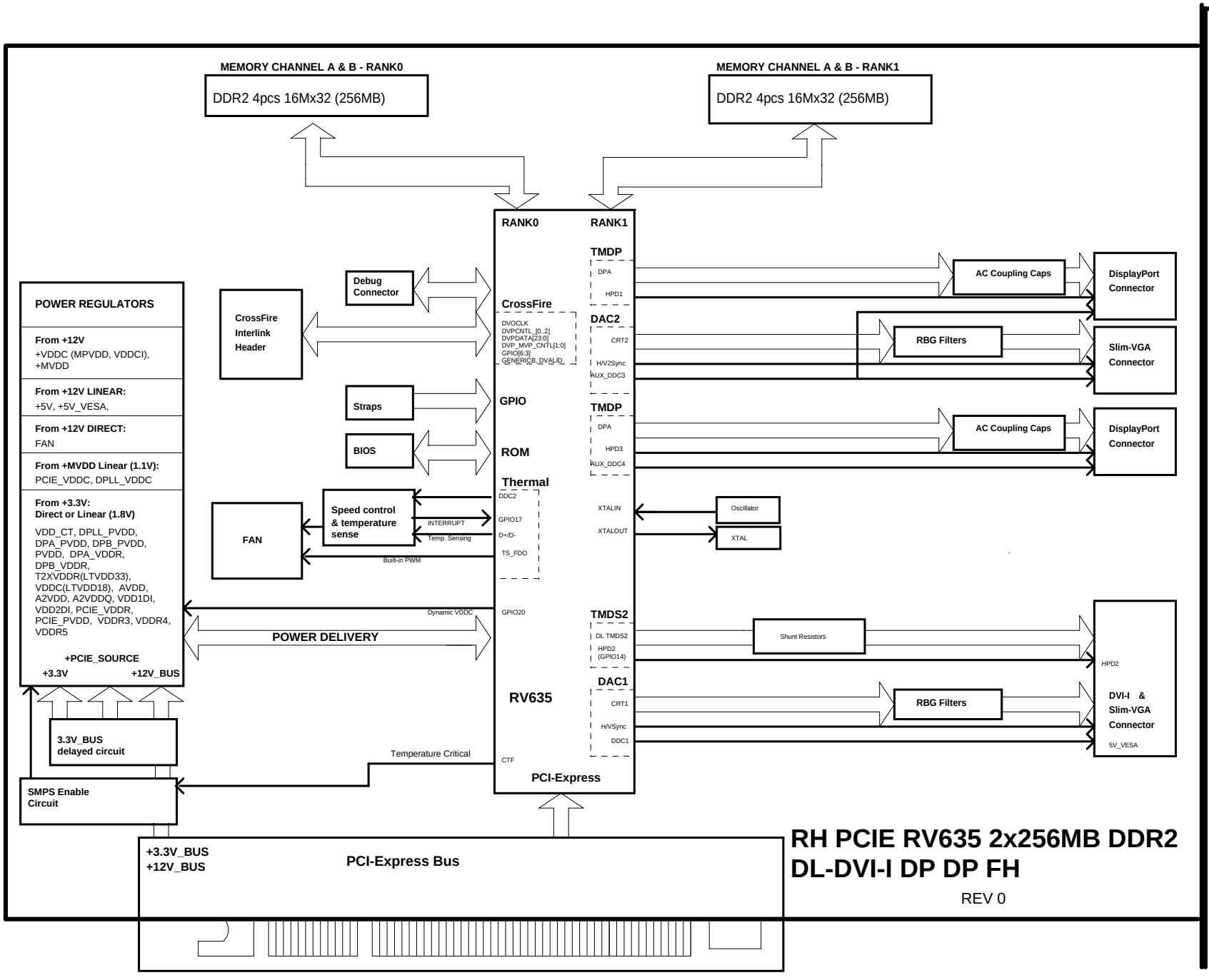
Title	Schematic No.	Date:
RH PCIE RV635 2x256MB DDR2 DUAL DL-DVI-I DL-DVI-I VO FH	105-B381xx-00A	Thursday, January 31, 2008

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	??/??/07	Initial design for RV635 GDDR3



RH PCIE RV635 2x256MB DDR2
DL-DVI-I DP DP FH

REV 0

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Title RV635 DDR2 - BLOCK DIAGRAM	Doc No. 105-B381xx-00A