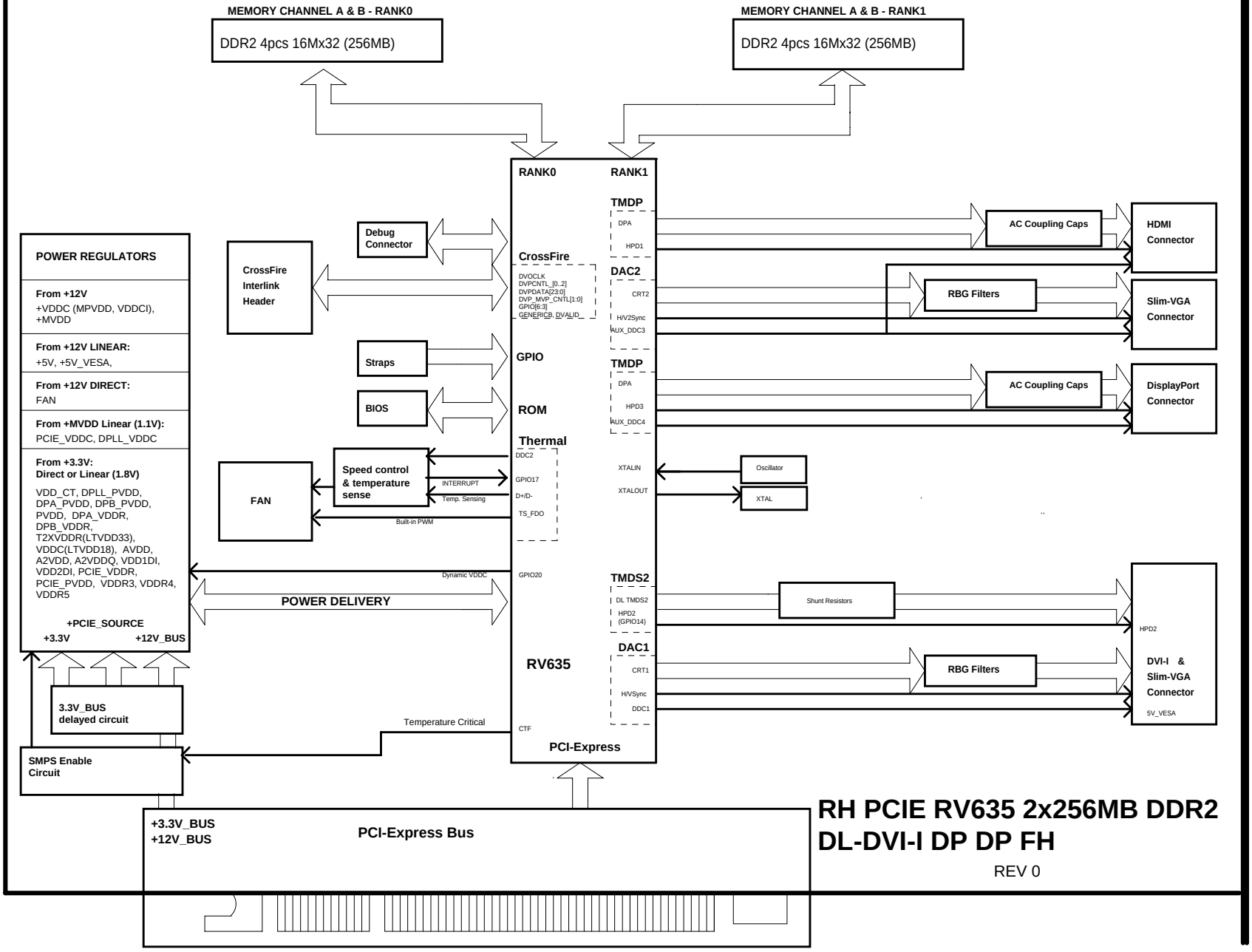
Title	Schematic No.	Date:
RH PCIE RV635 2x256MB DDR2 DUAL DL-DVI-I DL-DVI-I VO FH	105-B382xx-00A	Thursday, November 29, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	29/12/07	Initial design for RV635 GDDR3



RH PCIE RV635 2x256MB DDR2
DL-DVI-I DP DP FH

REV 0

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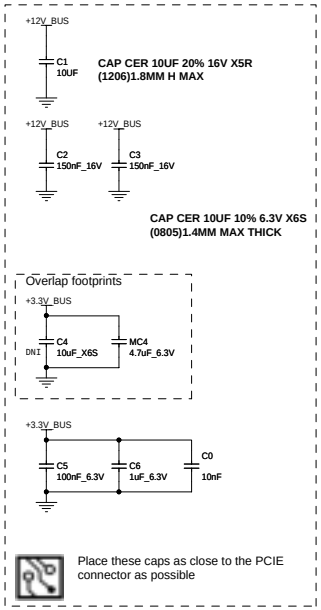
Rev	0
Sheet	21 of 21
Title	RV635 DDR2 - BLOCK DIAGRAM
Doc No.	105-B382xx-00A

PCI-EXPRESS EDGE CONNECTOR



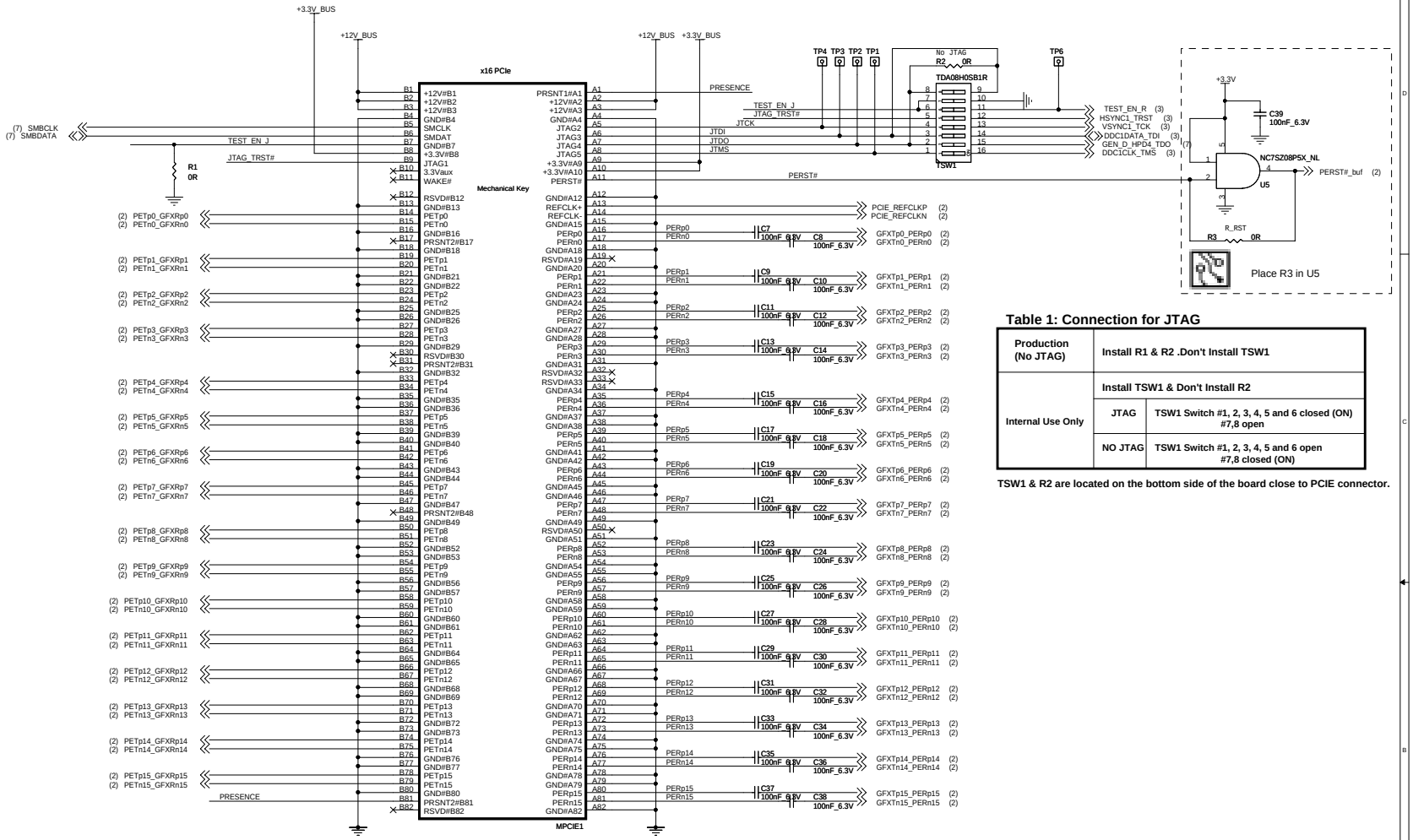


Table 1: Connection for JTAG

Production (No JTAG)	**Install R1 & R2 .Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #7,8 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #7,8 closed (ON)**

TSW1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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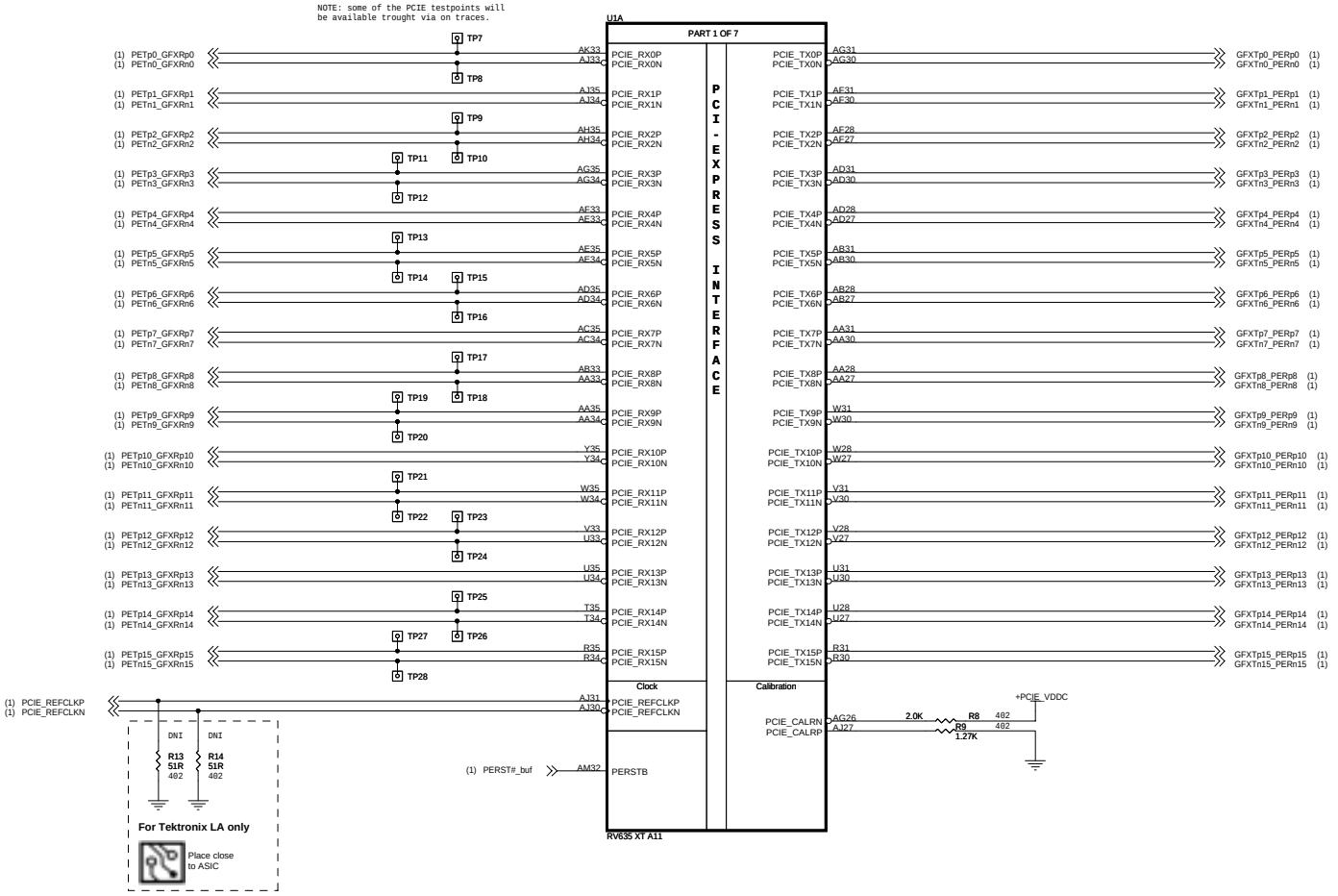
Title RV635 DDR2 - PCI-E Edge Connector

Doc No. 105-B382xx-00A



(1) PETp0_GFXRp0	TP7	AK33	PCIE_RX0P
(1) PETn0_GFXRn0		AJ33	PCIE_RX0N
	TP8		
(1) PETp1_GFXRp1		AJ35	PCIE_RX1P
(1) PETn1_GFXRn1		AJ34	PCIE_RX1N
	TP9		
(1) PETp2_GFXRp2		AH35	PCIE_RX2P
(1) PETn2_GFXRn2		AH34	PCIE_RX2N
	TP11 TP10		
(1) PETp3_GFXRp3		AG35	PCIE_RX3P
(1) PETn3_GFXRn3		AG34	PCIE_RX3N
	TP12		
(1) PETp4_GFXRp4		AF33	PCIE_RX4P
(1) PETn4_GFXRn4		AE33	PCIE_RX4N
	TP13		
(1) PETp5_GFXRp5		AE35	PCIE_RX5P
(1) PETn5_GFXRn5		AE34	PCIE_RX5N
	TP14 TP15		
(1) PETp6_GFXRp6		AD35	PCIE_RX6P
(1) PETn6_GFXRn6		AD34	PCIE_RX6N
	TP16		
(1) PETp7_GFXRp7		AC35	PCIE_RX7P
(1) PETn7_GFXRn7		AC34	PCIE_RX7N
	TP17		
(1) PETp8_GFXRp8		AB33	PCIE_RX8P
(1) PETn8_GFXRn8		AA33	PCIE_RX8N
	TP19 TP18		
(1) PETp9_GFXRp9		AA35	PCIE_RX9P
(1) PETn9_GFXRn9		AA34	PCIE_RX9N
	TP20		
(1) PETp10_GFXRp10		Y35	PCIE_RX10P
(1) PETn10_GFXRn10		Y34	PCIE_RX10N
	TP21		
(1) PETp11_GFXRp11		W35	PCIE_RX11P
(1) PETn11_GFXRn11		W34	PCIE_RX11N
	TP22 TP23		
(1) PETp12_GFXRp12		V33	PCIE_RX12P
(1) PETn12_GFXRn12		U33	PCIE_RX12N
	TP24		
(1) PETp13_GFXRp13		U35	PCIE_RX13P
(1) PETn13_GFXRn13		U34	PCIE_RX13N
	TP25		
(1) PETp14_GFXRp14		T35	PCIE_RX14P
(1) PETn14_GFXRn14		T34	PCIE_RX14N
	TP27 TP26		
(1) PETp15_GFXRp15		R35	PCIE_RX15P
(1) PETn15_GFXRn15		R34	PCIE_RX15N
	TP28		

(1) PCIE_REFCLKP		AJ31	PCIE_REFCLKP
(1) PCIE_REFCLKN		AJ30	PCIE_REFCLKN
(1) PERST#_buf		AM32	PERSTB
		AG26	PCIE_CALRN
		AJ27	PCIE_CALRP

PCIE_TX0P	AG31	GFXTp0_PERp0	(1)
PCIE_TX0N	AG30	GFXTn0_PERn0	(1)
PCIE_TX1P	AF31	GFXTp1_PERp1	(1)
PCIE_TX1N	AF30	GFXTn1_PERn1	(1)
PCIE_TX2P	AF28	GFXTp2_PERp2	(1)
PCIE_TX2N	AF27	GFXTn2_PERn2	(1)
PCIE_TX3P	AD31	GFXTp3_PERp3	(1)
PCIE_TX3N	AD30	GFXTn3_PERn3	(1)
PCIE_TX4P	AD28	GFXTp4_PERp4	(1)
PCIE_TX4N	AD27	GFXTn4_PERn4	(1)
PCIE_TX5P	AB31	GFXTp5_PERp5	(1)
PCIE_TX5N	AB30	GFXTn5_PERn5	(1)
PCIE_TX6P	AB28	GFXTp6_PERp6	(1)
PCIE_TX6N	AB27	GFXTn6_PERn6	(1)
PCIE_TX7P	AA31	GFXTp7_PERp7	(1)
PCIE_TX7N	AA30	GFXTn7_PERn7	(1)
PCIE_TX8P	AA28	GFXTp8_PERp8	(1)
PCIE_TX8N	AA27	GFXTn8_PERn8	(1)
PCIE_TX9P	W31	GFXTp9_PERp9	(1)
PCIE_TX9N	W30	GFXTn9_PERn9	(1)
PCIE_TX10P	W28	GFXTp10_PERp10	(1)
PCIE_TX10N	W27	GFXTn10_PERn10	(1)
PCIE_TX11P	V31	GFXTp11_PERp11	(1)
PCIE_TX11N	V30	GFXTn11_PERn11	(1)
PCIE_TX12P	V28	GFXTp12_PERp12	(1)
PCIE_TX12N	V27	GFXTn12_PERn12	(1)
PCIE_TX13P	U31	GFXTp13_PERp13	(1)
PCIE_TX13N	U30	GFXTn13_PERn13	(1)
PCIE_TX14P	U28	GFXTp14_PERp14	(1)
PCIE_TX14N	U27	GFXTn14_PERn14	(1)
PCIE_TX15P	R31	GFXTp15_PERp15	(1)
PCIE_TX15N	R30	GFXTn15_PERn15	(1)

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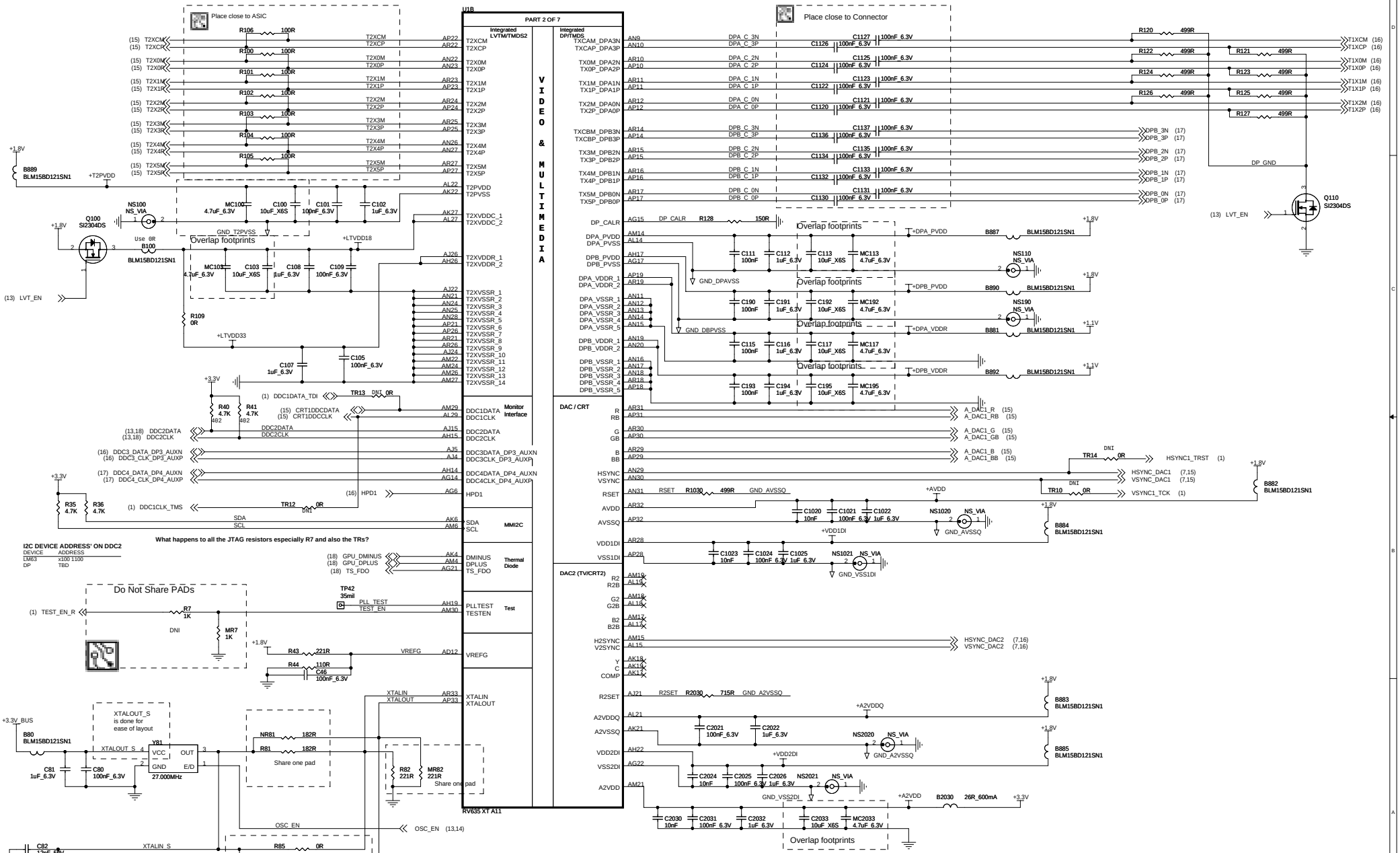
Title RV635 DDR2 - ASIC PCIE_Interface

Doc No. 105-B382xx-00A

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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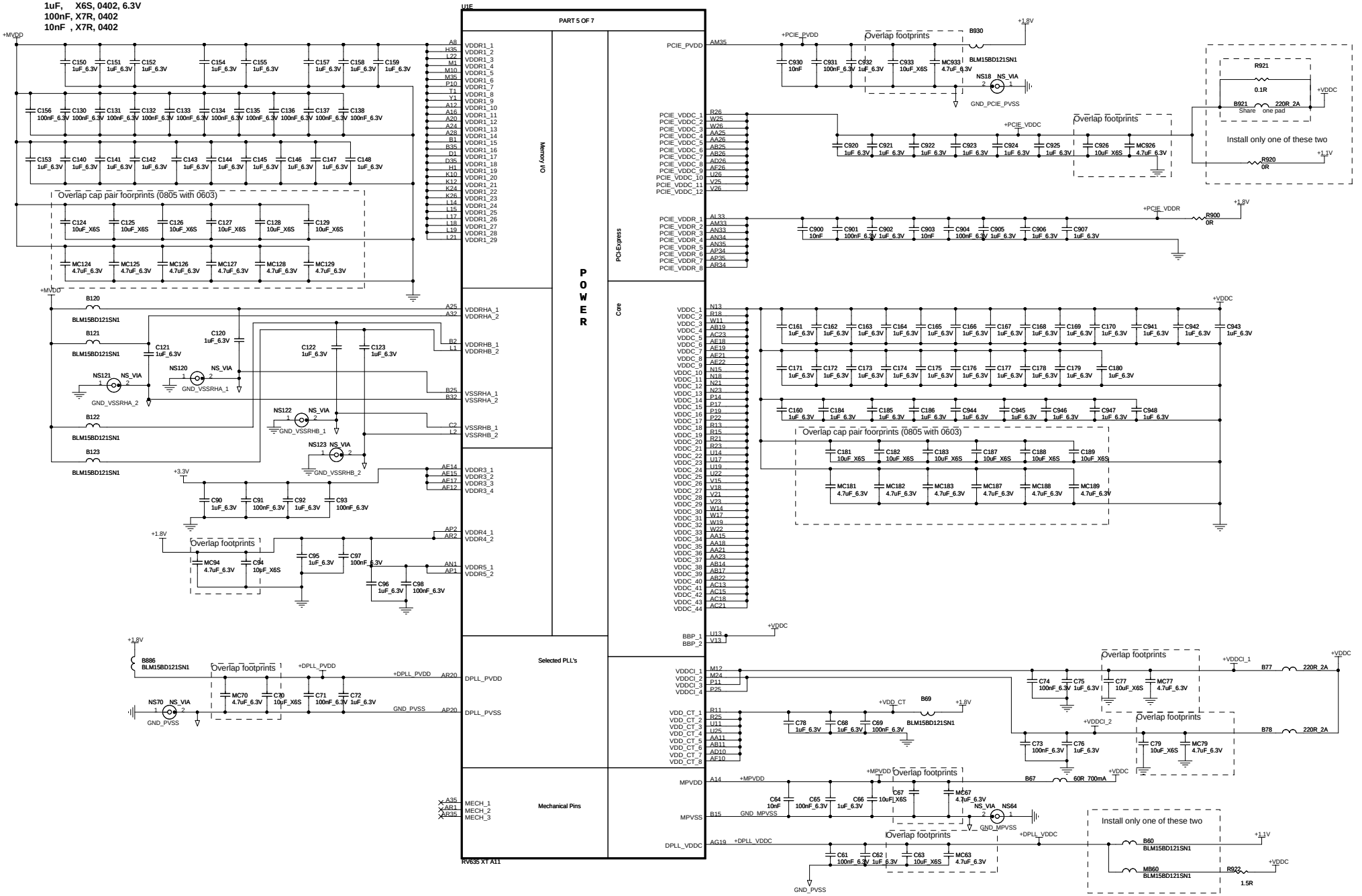
Title	RV635 DDR2 - ASIC MAIN
Doc No.	105-B382xx-00A

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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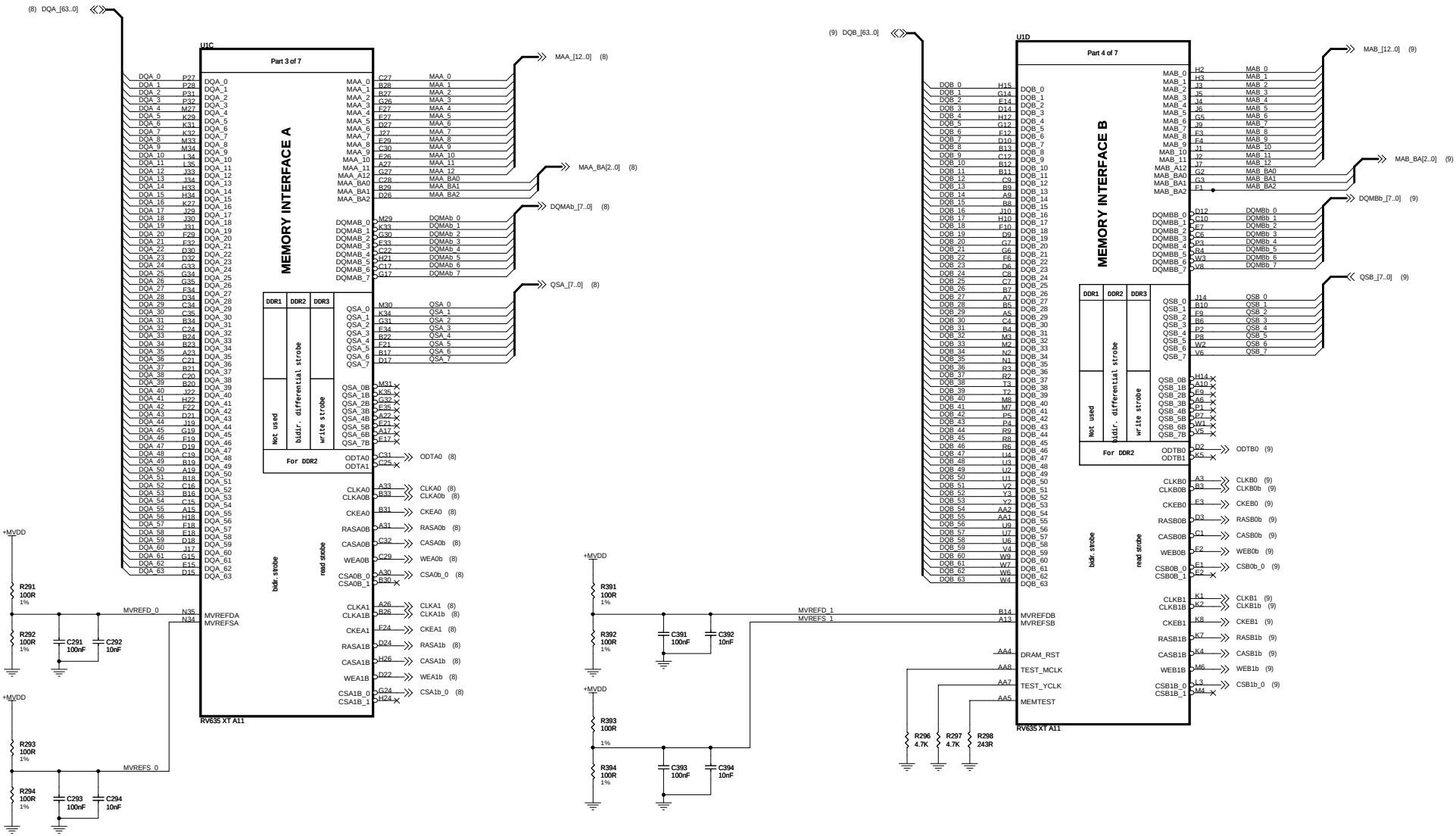
Title	RV635 DDR2 - ASIC Power
Doc No.	105-B382xx-00A



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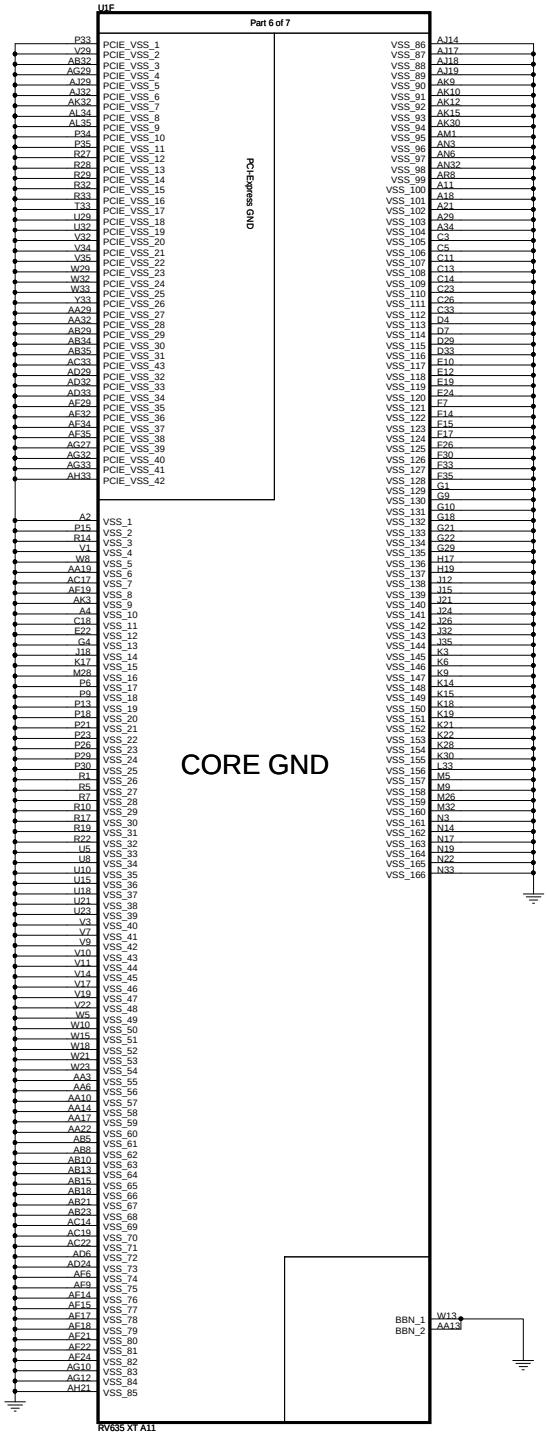
Title RV635 DDR2 - ASIC Memory Interface (Channel A & B)

Doc No. 105-B382xx-00A



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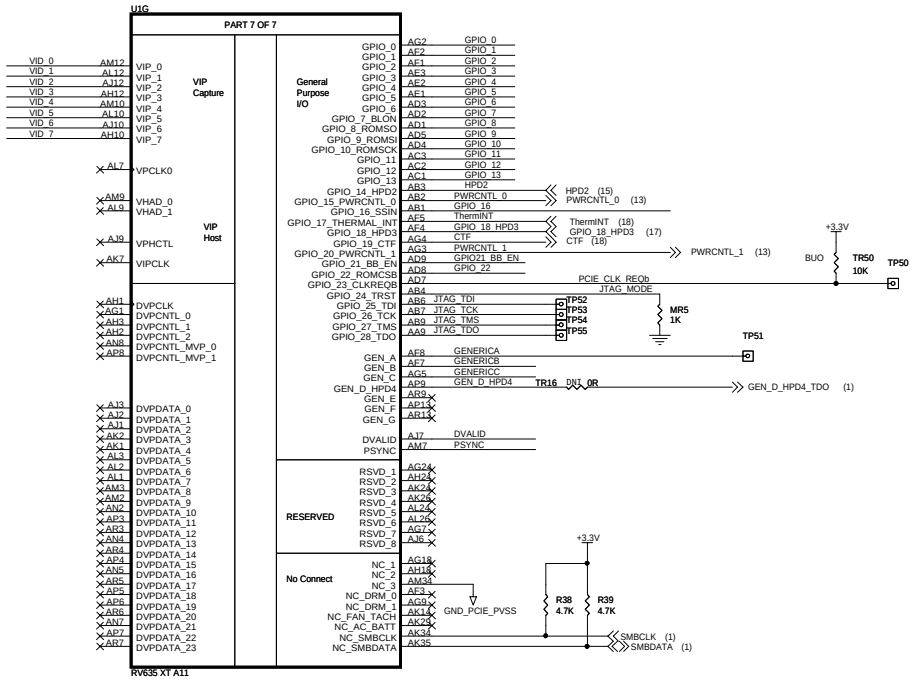
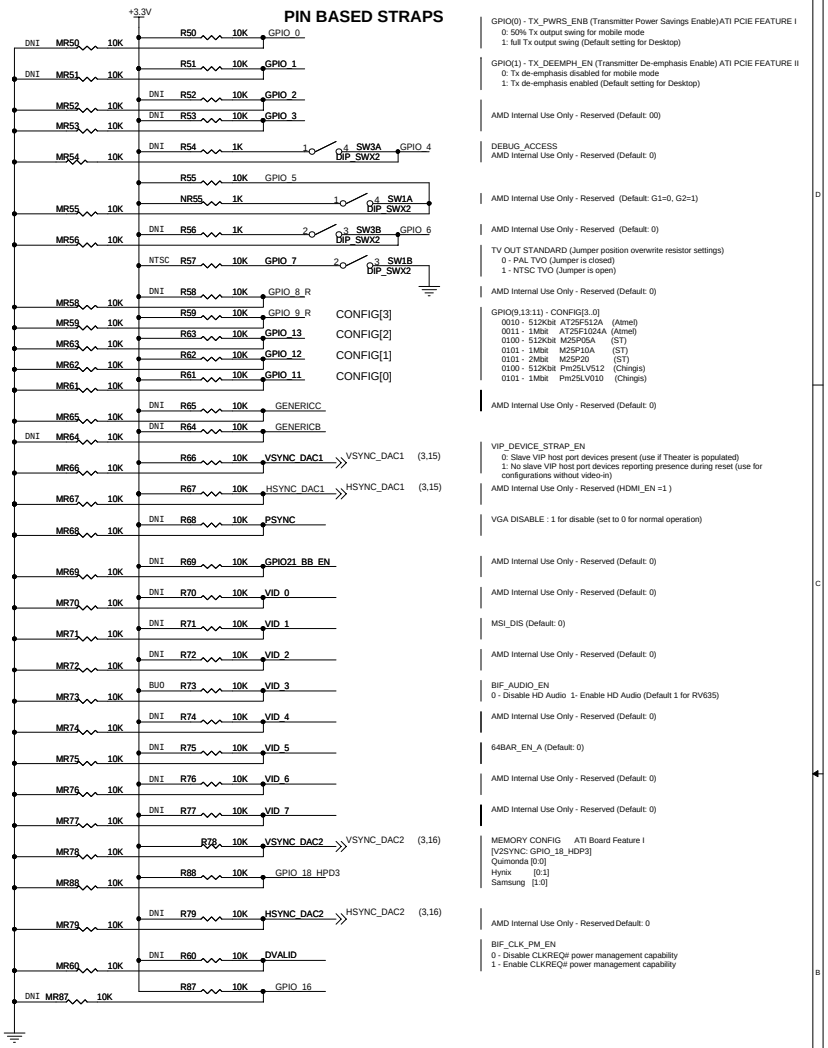
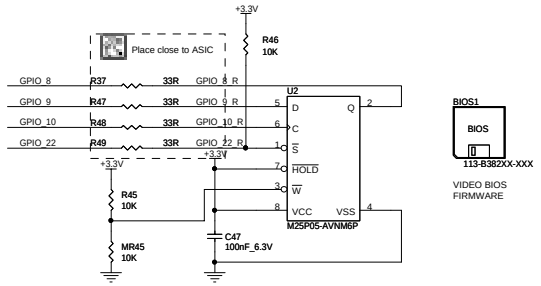
Title RV635 DDR2 - ASIC Grounds

Doc No. 105-B382xx-00A







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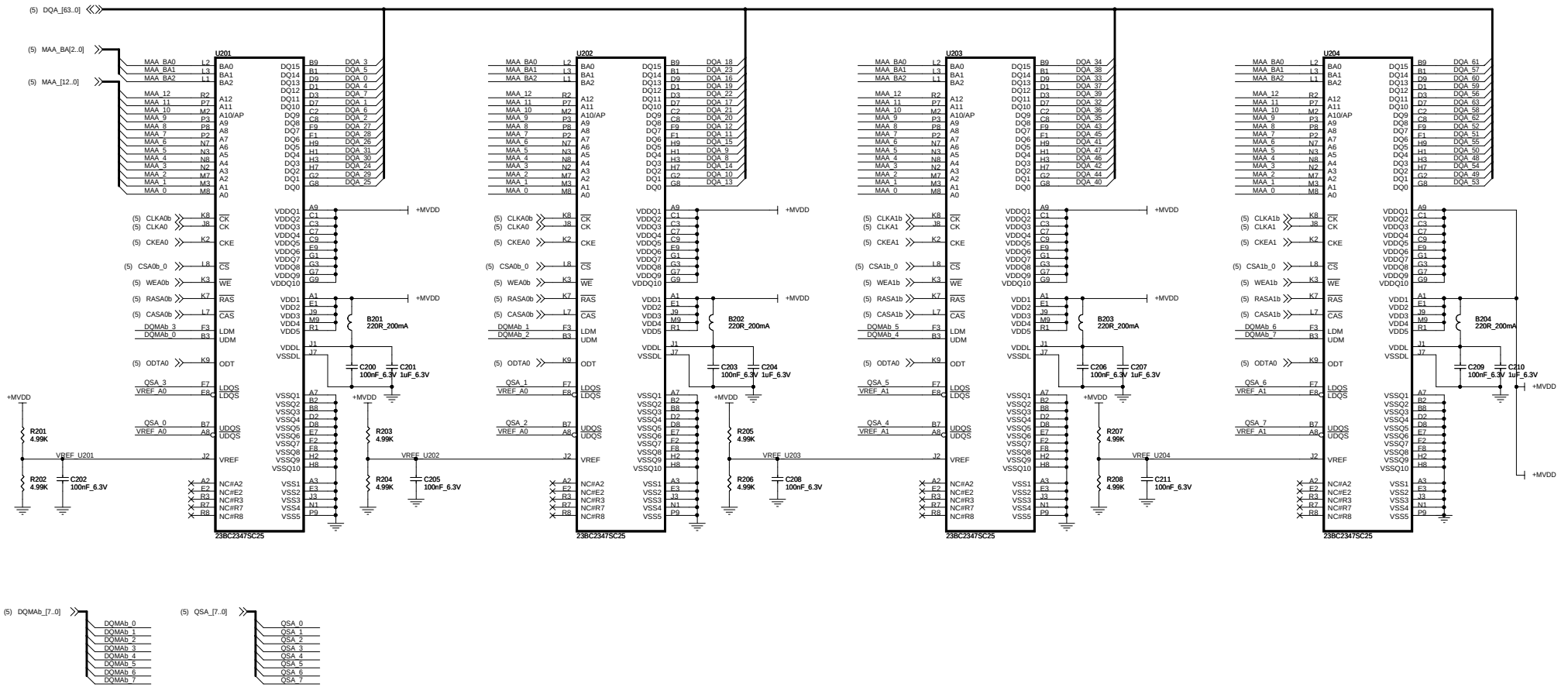
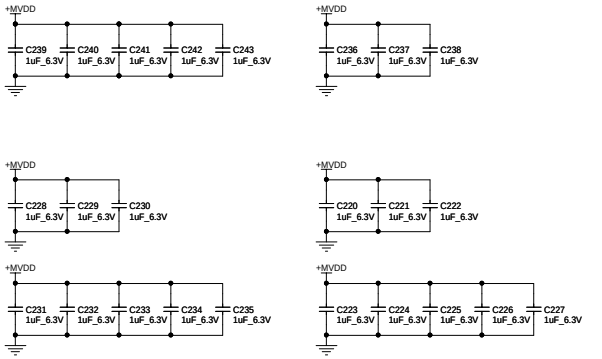
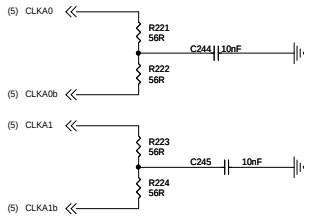
Title RV635 DDR2 - ASIC DVO & GPIOs

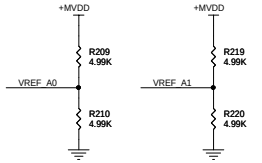
Doc No. 105-B382xx-00A

CHANNEL A: 128MB/256MB DDR2









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Title	RV635 DDR2 - MEM CH A
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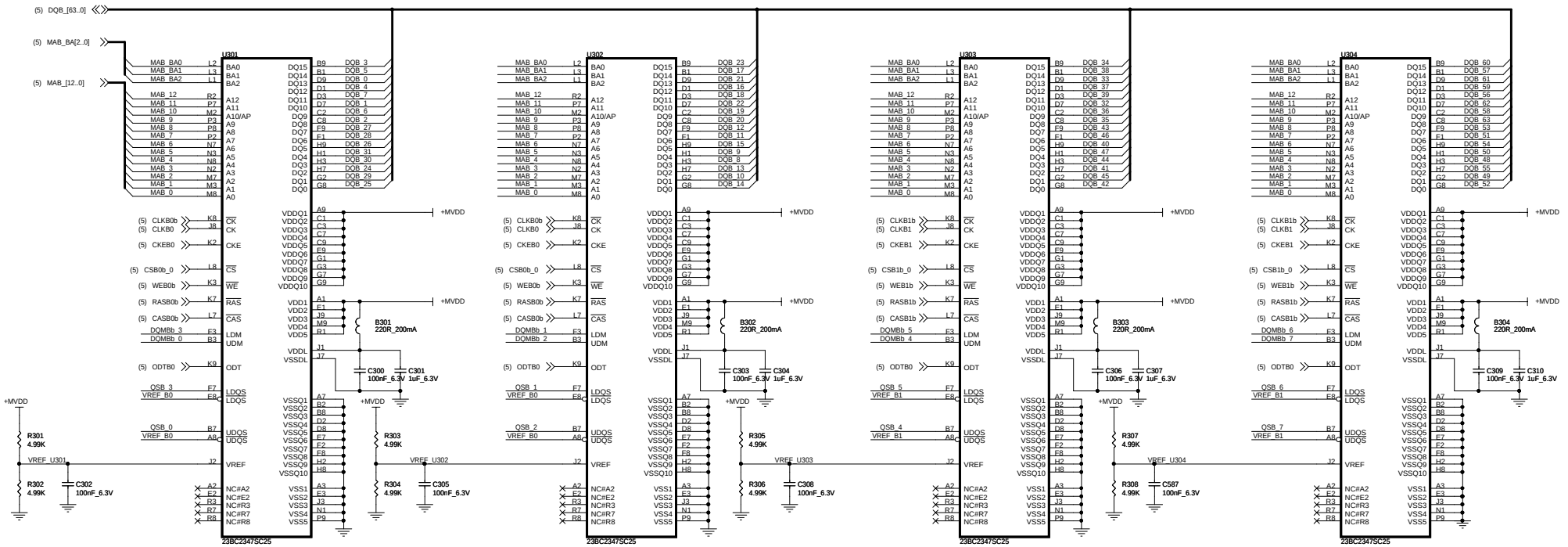
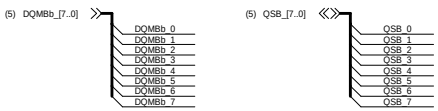
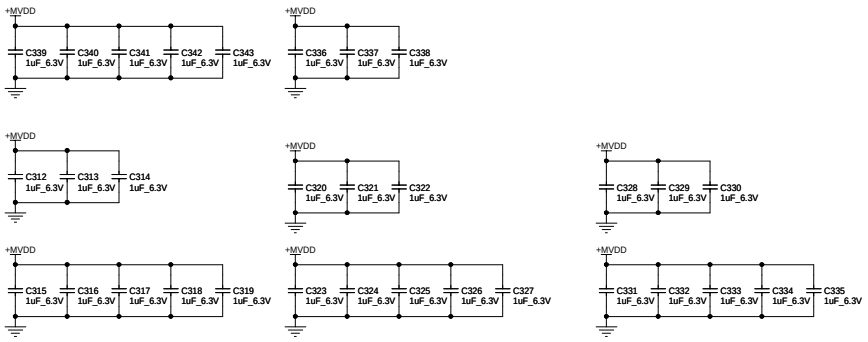
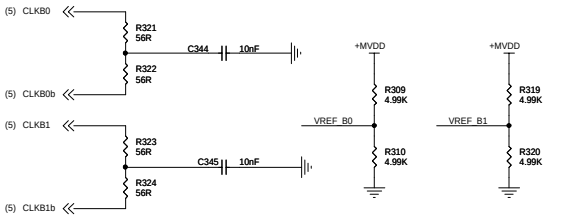
CHANNEL B: 128MB/256MB DDR2









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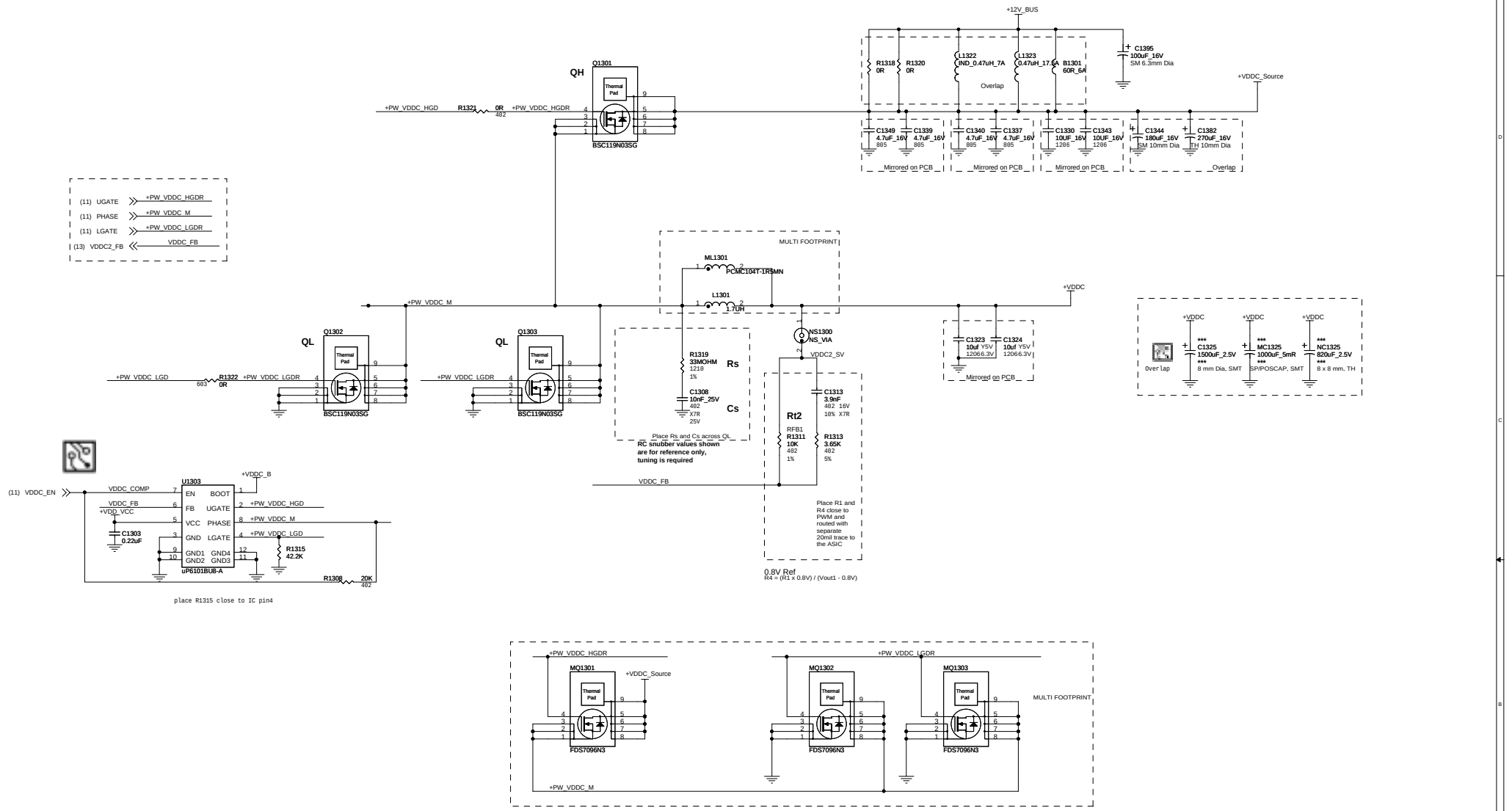
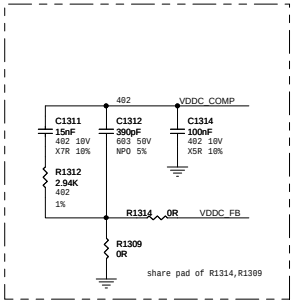
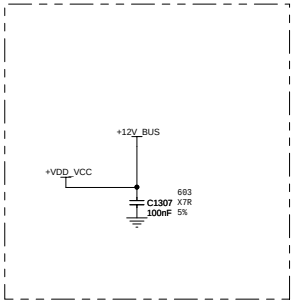


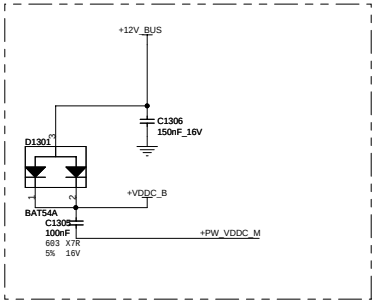
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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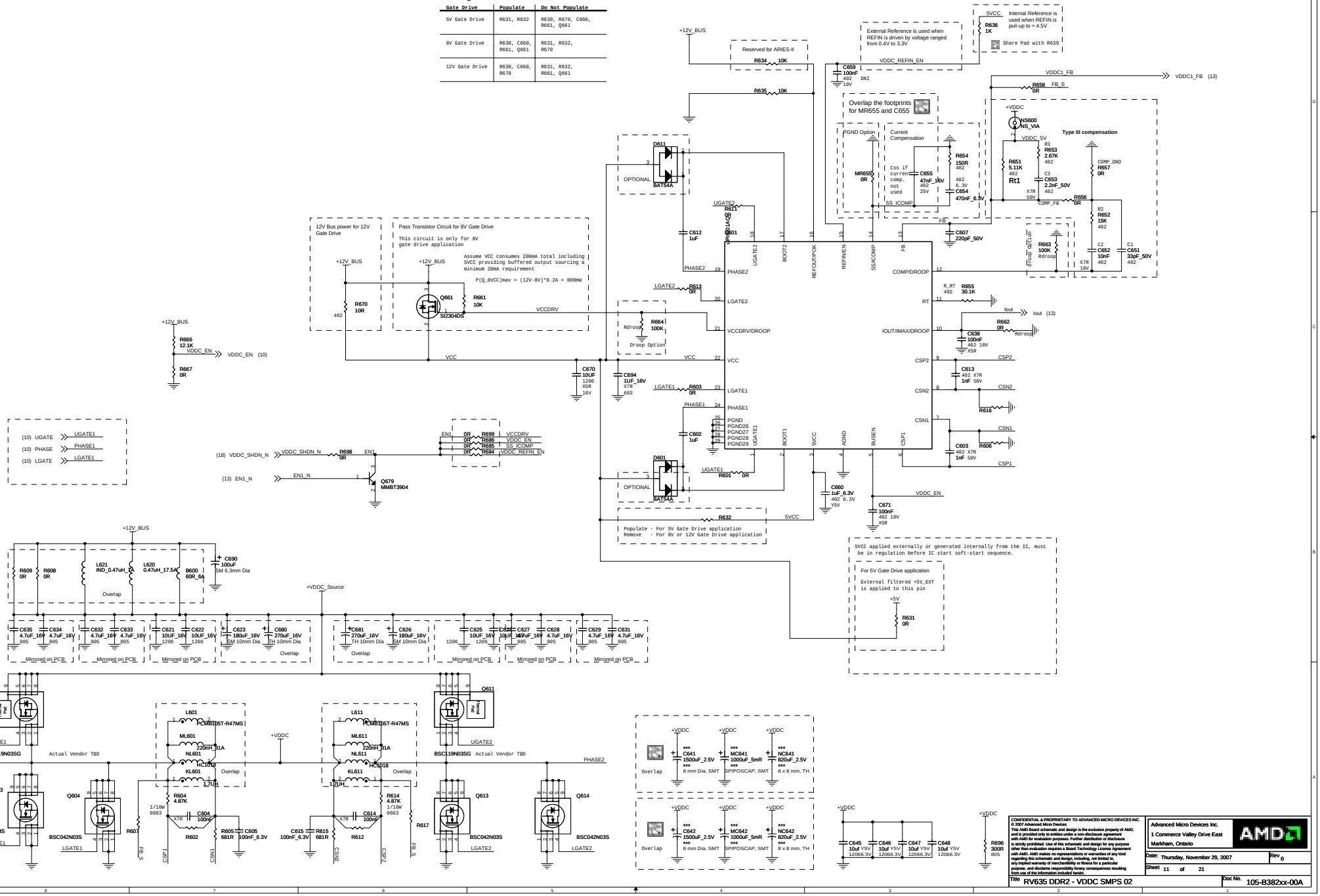
Title RV635 DDR2 - VDDC SMPS 01

Doc No. 105-B382xx-00A

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661



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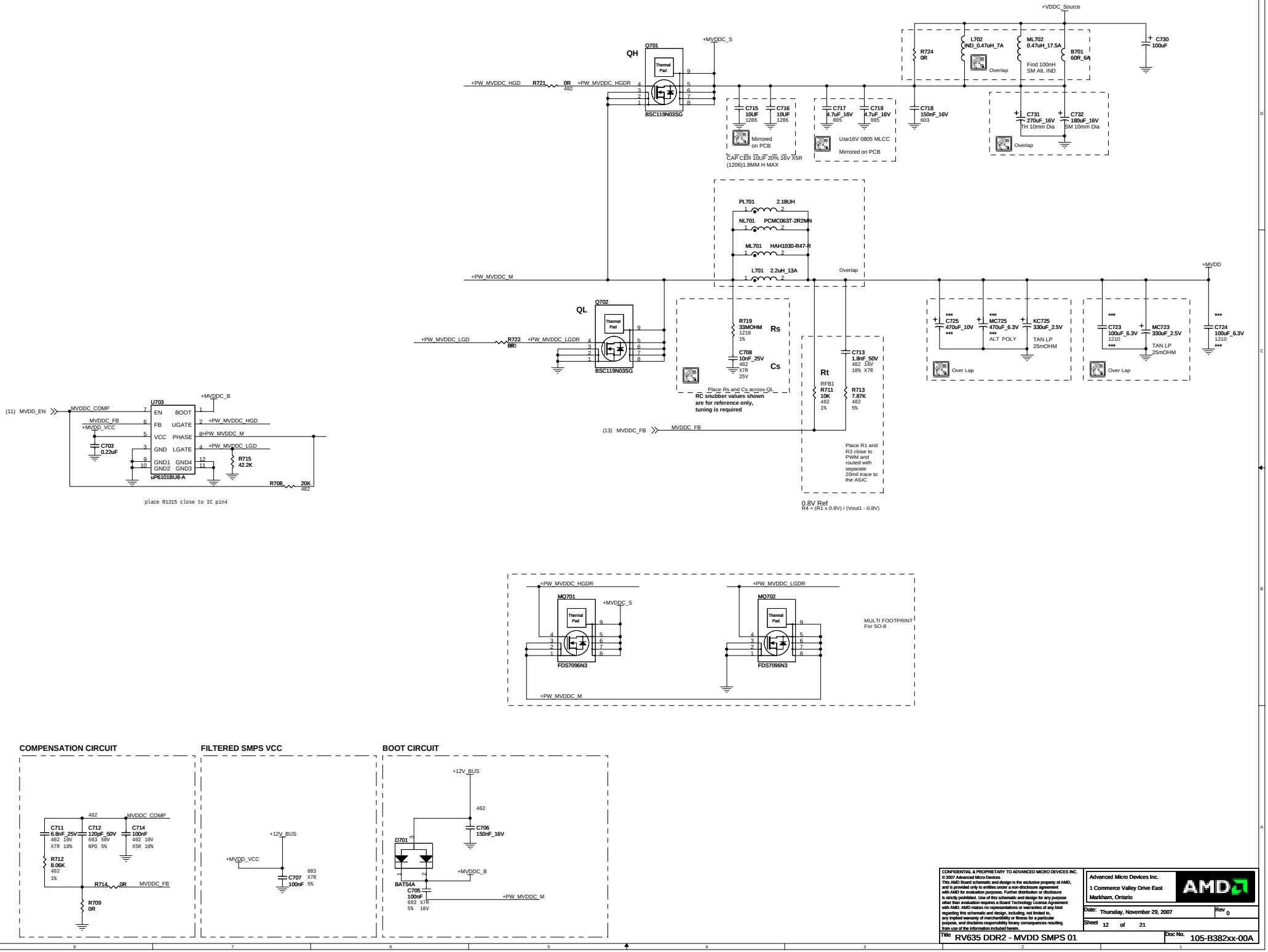
Title: RV635 DDR2 - VDDC SMPS 02

Doc No. 105-B382xx-00A



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Title	RV635 DDR2 - MVDD SMPS 01
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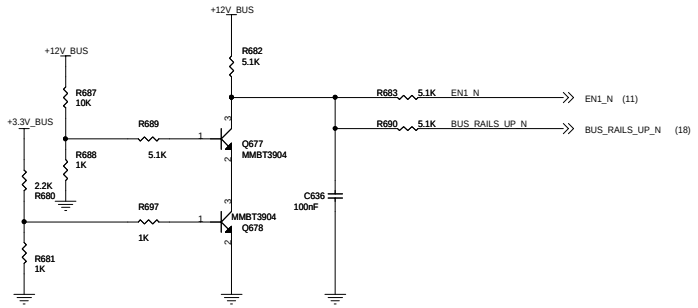
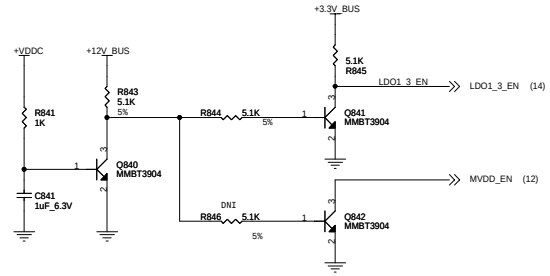
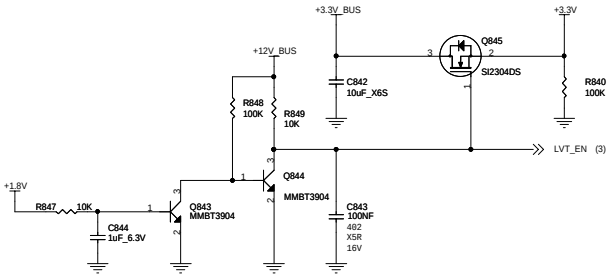
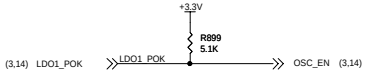
Power up Sequencing



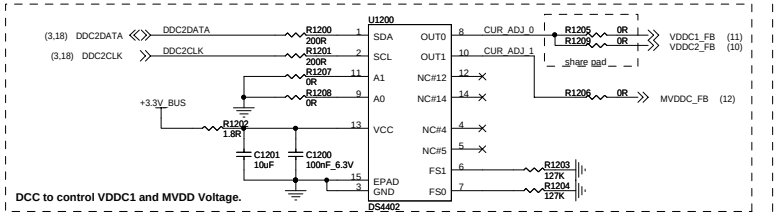
VDDC Enable Circuit

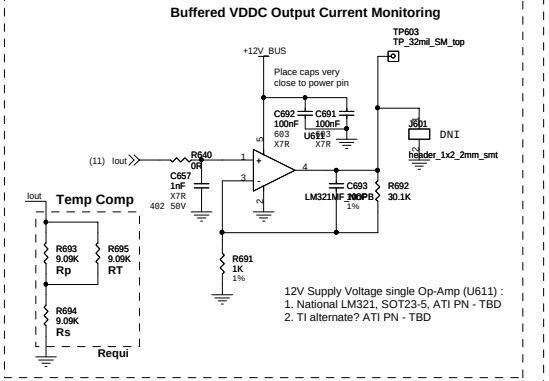






Resistors to set the output voltages for +VDDC and +MVDDC



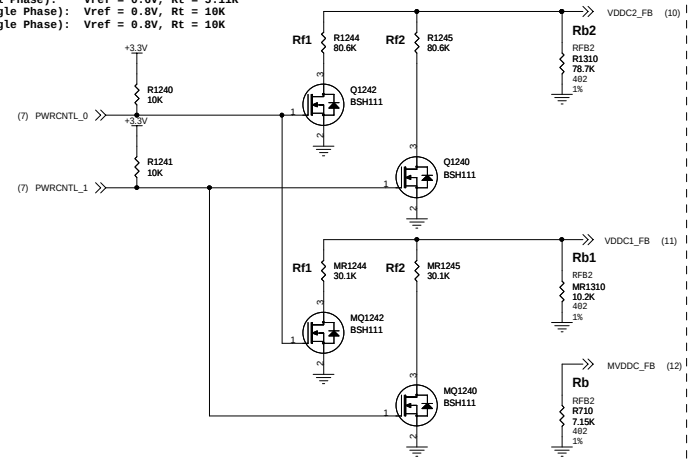


Power Play

VDDC Voltage Settings Using GPIOs (for VDDC1 Dual Phase)

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0	0	0.90V			
0	1	1.00V			
1	0	1.00V			
1	1	1.10			Power-up Default

Vout = Vref * (1+Rt/Rb)
VDDC1 (Dual Phase): Vref = 0.6V, Rt = 5.11K
VDDC2 (Single Phase): Vref = 0.8V, Rt = 10K
MVDDC (Single Phase): Vref = 0.8V, Rt = 10K



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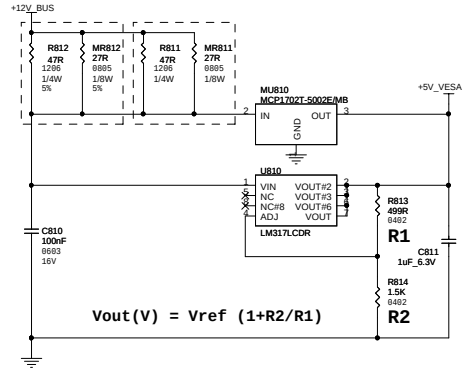
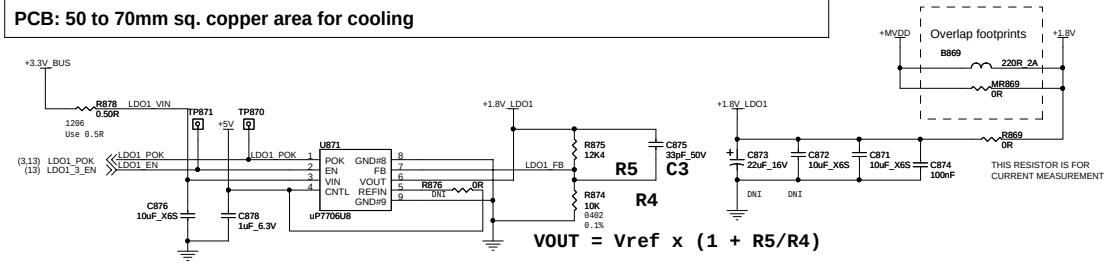
132-
For Testing purposes only

Regulators for +5V, +5V_VESA and +5V_VESA2

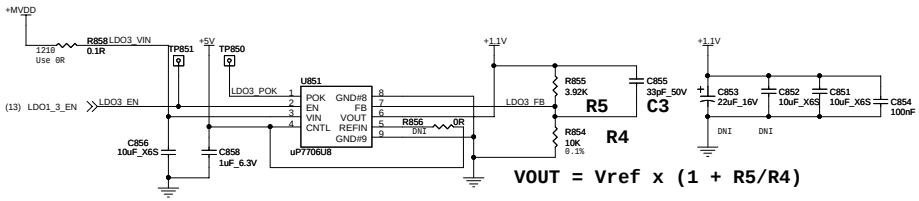


LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

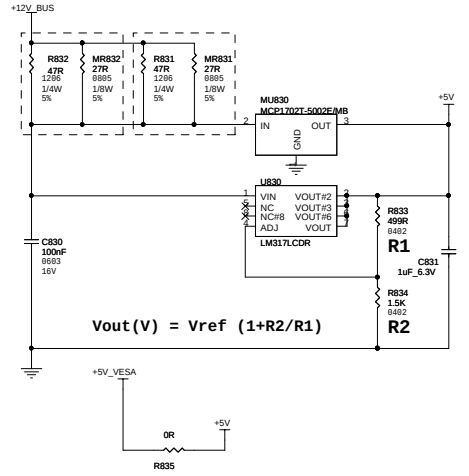


VOUT = Vref x (1 + R5/R4)

LDO #3: Vin = +1.45V to 2.0VMAX Vout = +1.1V +/- 2% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



VOUT = Vref x (1 + R5/R4)



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See BOM for qualified filters

(3) A_DAC1_R — R1001 75R — C1004 8.0pF — L1001 47nH — R1024 0R — A_R_DAC1_M — C1001 12pF_50V — L1004 36NH

(3) A_DAC1_RB — R1027 37.4R

(3) A_DAC1_G — R1002 75R — C1005 8.0pF — L1002 47nH — R1025 0R — A_G_DAC1_M — C1002 12pF_50V — L1005 36NH

(3) A_DAC1_GB — R1028 37.4R

(3) A_DAC1_B — R1003 75R — C1006 8.0pF — L1003 47nH — R1026 0R — A_B_DAC1_M — C1003 12pF_50V — L1006 36NH

(3) A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

For ESD Protection

+3.3V — D1001 CM1213-04 — +5V_VESA — D1002 CM1213-04

+5V_VESA — B1012 30R_3A — R1012 0R — +5V_DAC1_VESA

Overlap pads

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

MJ1001

1	R
2	G
3	B
11	MS0
12	MS1
4	MS2
15	MS3
9	NC
13	HS
14	VS
5	VSS
6	VSS#6
7	VSS#7
8	VSS#8
10	VSS#10
16	CASE
17	CASE#17

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

C1010 68pF 603

G3179C219-005

(3) CRT1DDCDATA — +3.3V — R1004 10K — +5V — R1005 2.2K — Q1001 BSH111 — DDCDATA_DAC1_5V — R1006 33R — DDCDATA_DAC1_R

(3) CRT1DDCCLK — +3.3V — R1007 10K — +5V — R1008 2.2K — Q1002 BSH111 — DDCCLK_DAC1_5V — R1009 33R — DDCCLK_DAC1_R

(3,7) HSYNC_DAC1 — +5V — C1999 100nF_6.3V — U1999A 74VHC125 — HSYNC_DAC1_B — R1010 10R — HSYNC_DAC1_R — C1007 12pF_50V

(3,7) VSYNC_DAC1 — U1999B 74VHC125 — VSYNC_DAC1_B — R1011 10R — VSYNC_DAC1_R — C1008 12pF_50V

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware	Mechanical Key	1A max	1A max	1A max	
Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

U1999C — 74VHC125 — U1999D — 74VHC125

(7) HPD2 — Q1021 MMBT3904 — +3.3V — R1022 10K — R1023 10K — HPD_DVI2

+5V_DAC1_VESA — J1001

25	CASE
1	TMDS Data2-
2	TMDS Data2+
3	TMDS Data2/4 Shield
4	TMDS Data4-
5	TMDS Data4+
6	DDC Clock
7	DDC Data
8	Analog VSYNC
9	TMDS Data1-
10	TMDS Data1+
11	TMDS Data1/3 Shield
12	TMDS Data3-
13	TMDS Data3+
14	+5V Power
15	GND (for +5V)
16	Hot Plug Detect
17	TMDS Data0-
18	TMDS Data0+
19	TMDS Data0/5 Shield
20	TMDS Data5-
21	TMDS Data5+
22	TMDS Clock Shield
23	TMDS Clock+
24	TMDS Clock-
C1	Analog Red
C2	Analog Green
C3	Analog Blue
C4	Analog HYNC
C5	Analog GND
C6	Analog GND#C6
26	CASE#26
27	CASE#27
28	CASE#28
29	CASE#29
30	CASE#30

(3) T2X2M — TMDS Data2-
(3) T2X2P — TMDS Data2+
TMDS Data2/4 Shield
(3) T2X4M — TMDS Data4-
(3) T2X4P — TMDS Data4+
DDCCLK_DAC1_R — DDC Clock
DDCDATA_DAC1_R — DDC Data
VSYNC_DAC1_R — Analog VSYNC
(3) T2X1M — TMDS Data1-
(3) T2X1P — TMDS Data1+
TMDS Data1/3 Shield
(3) T2X3M — TMDS Data3-
(3) T2X3P — TMDS Data3+
+5V Power
GND (for +5V)
HPD_DVI2 — Hot Plug Detect
(3) T2X0M — TMDS Data0-
(3) T2X0P — TMDS Data0+
TMDS Data0/5 Shield
(3) T2X5M — TMDS Data5-
(3) T2X5P — TMDS Data5+
TMDS Clock Shield
(3) T2XCP — TMDS Clock+
(3) T2XCM — TMDS Clock-
A_R_DAC1_F — Analog Red
A_G_DAC1_F — Analog Green
A_B_DAC1_F — Analog Blue
HSYNC_DAC1_R — Analog HYNC
Analog GND
Analog GND#C6
CASE#26
CASE#27
CASE#28
CASE#29
CASE#30

DVI_CONNECTOR

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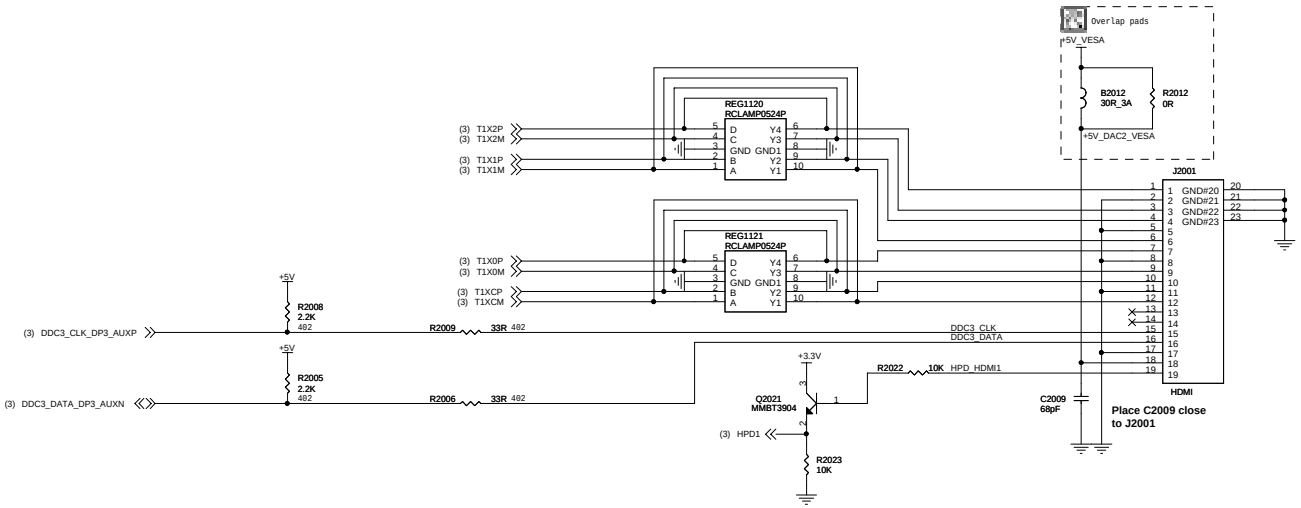

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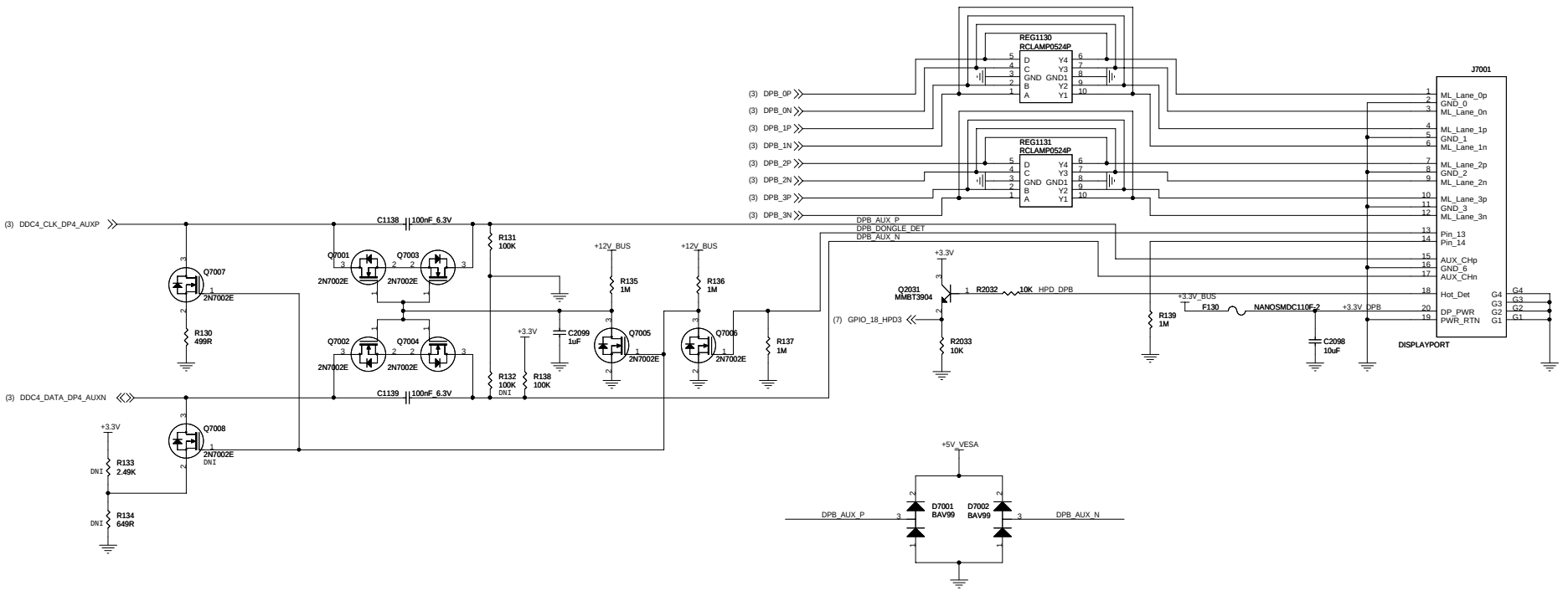

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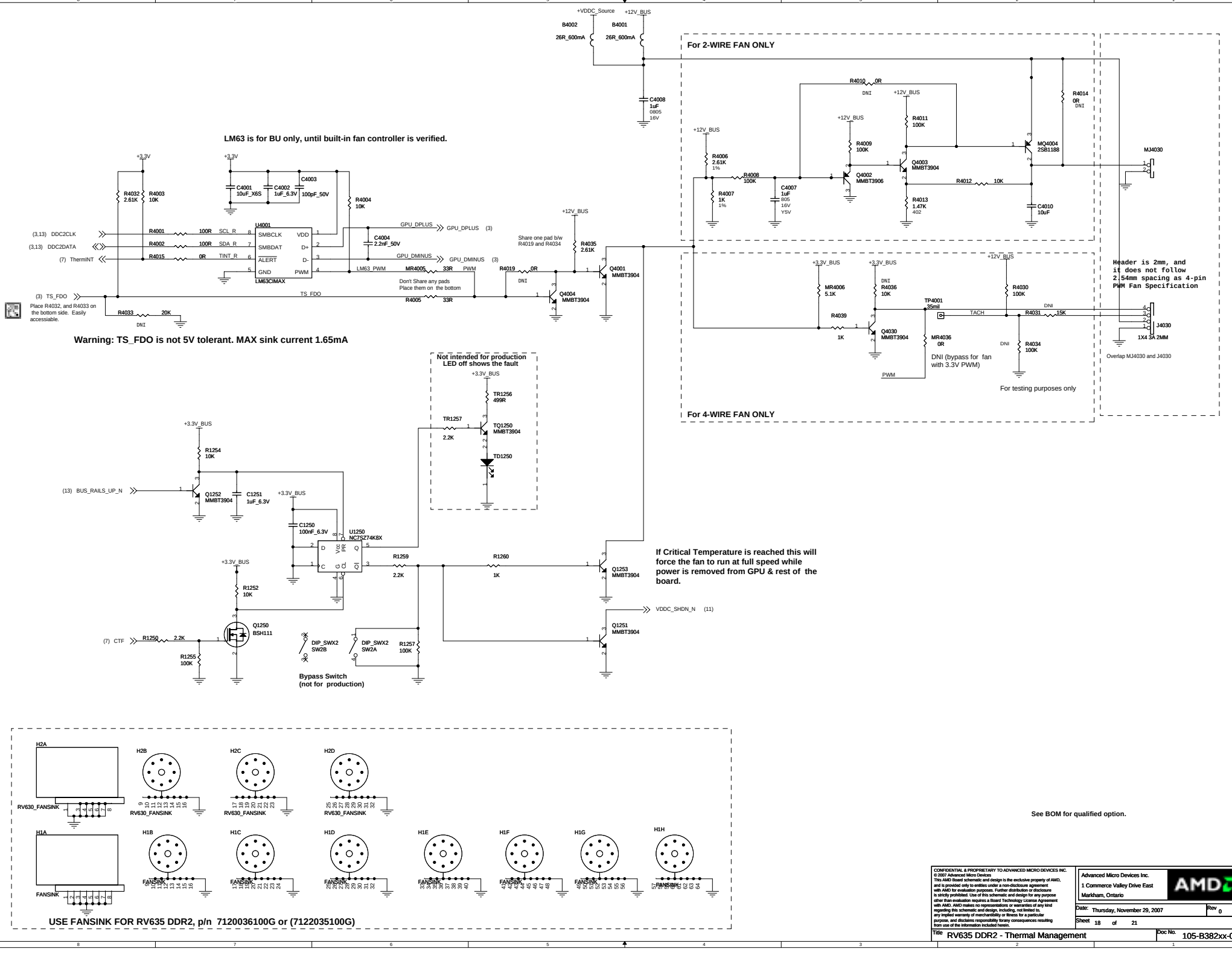

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DVI/DVI SCREWS with top tab

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

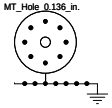
ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET
8020046100G

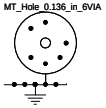
Need New Bracket

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

MT1
MT_Hole_0.136_in.



MT2
MT_Hole_0.136_in_6VIA



DNI

SK1
SOCKET_880

RV635 Socket

PCB1
PCB
109-GN982-00A

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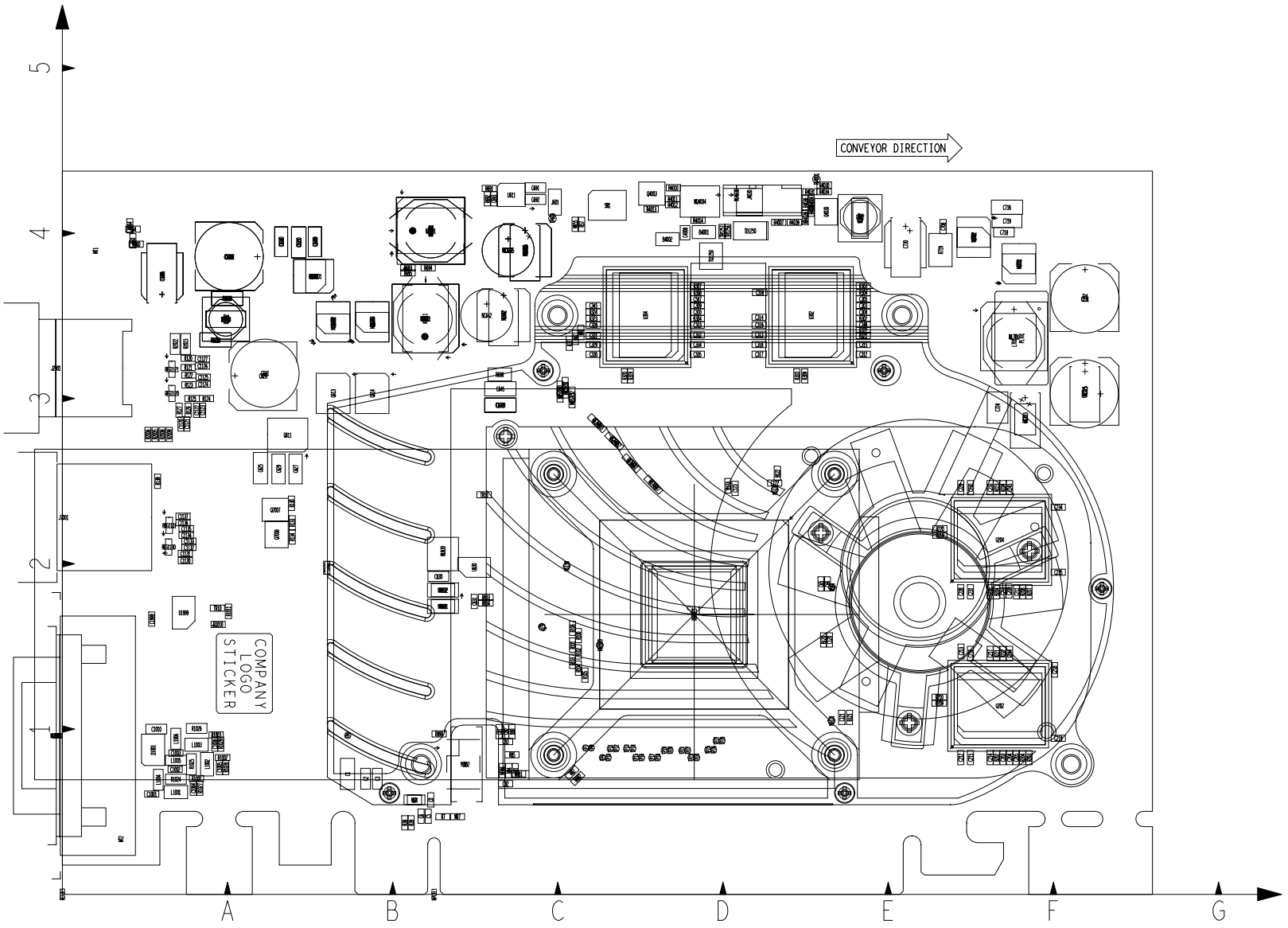

AMD ADVANCED MICRO DEVICES PCBCAD GROUP	RH RV635 512MB DDR2 DL-DVI DP HDMI FH 6 P/N 109-B38231-00A NOV. 01 2007 ASSEMBLY TOP Svetlana Ostrovsky SHEET 1 OF 2

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