PRELIMINARY AND SUBJECT TO CHANGE

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(1) NAVI10 PCIe Edge Connector

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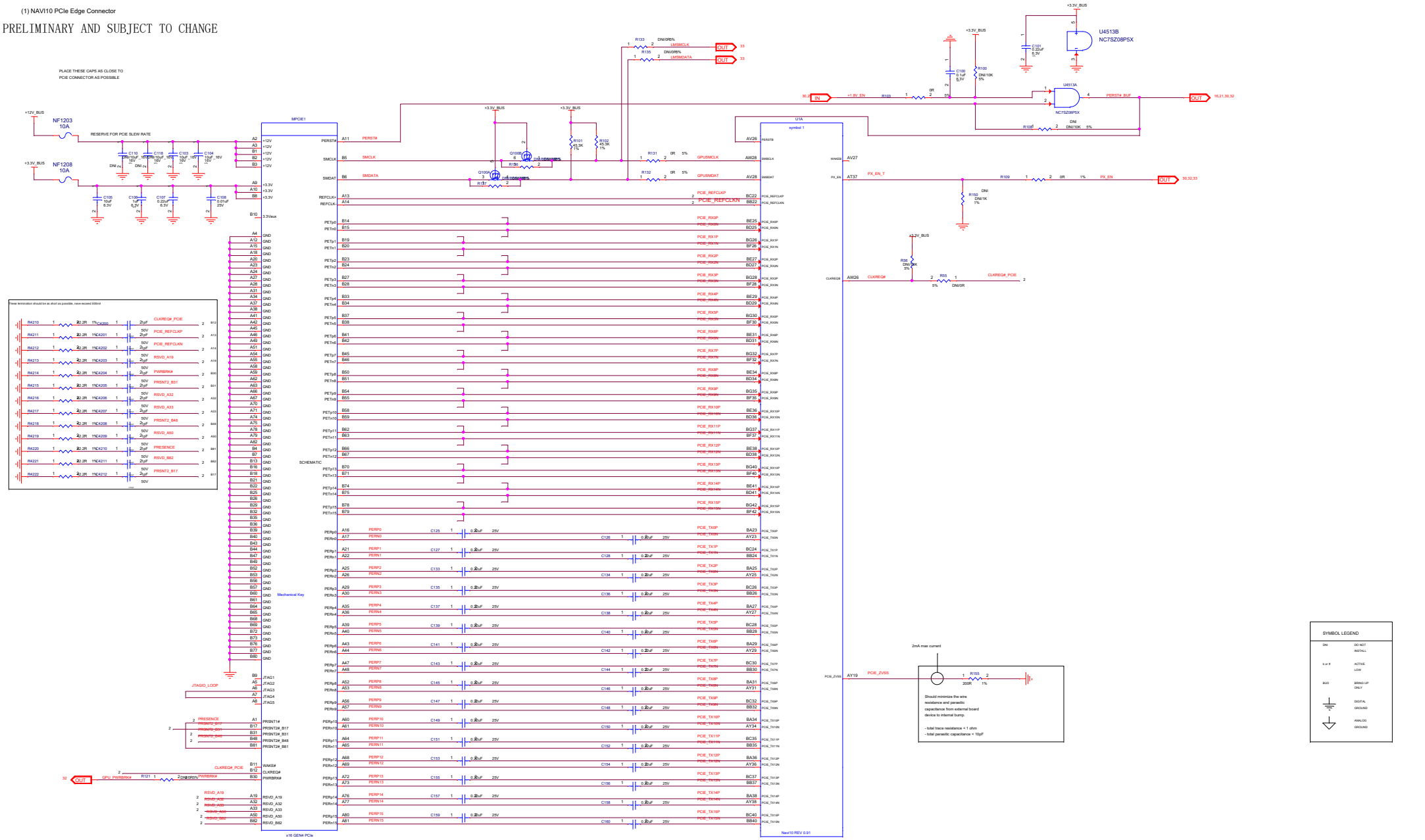

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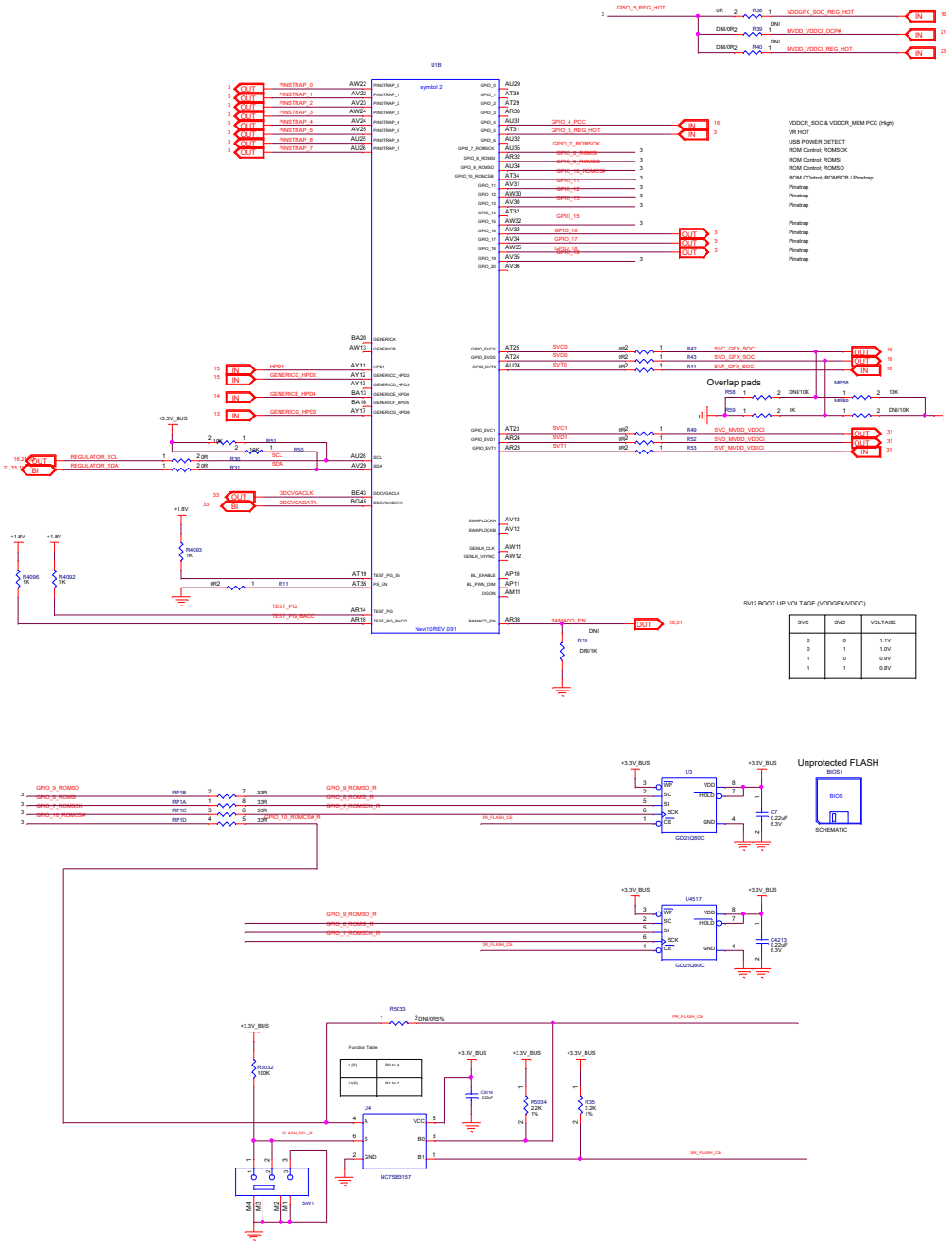

Note: Internal PU/PD at GPIO pad is ~40k strength in 14nm design spec

User		Internal Default Value	Definition
BIF	MR60	0	STRAP_BIF_GEN4_DIS_A 0: PCIe GEN 4 supported 1: PCIe GEN 4 not supported
	MR61	0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled
	MR62	0	PINSTRAP_BIF_LC_TX_SWING
	MR63	0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognised as the system's VGA controller
DCE	MR64	0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected
	MR65	0	
	MR66	0	
	MR67	0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for DisplayPort and native HDMI
	MR68	0	
Platform	MR69	0	
	MR70	0	
	MR71	0	
SMU	MR72	1	
	MR73	0	
	MR74	1	
	MR75		PINSTRAP_SMBUS_ADDR 0: 0x41h 1: 0x43h
	MR76	1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device

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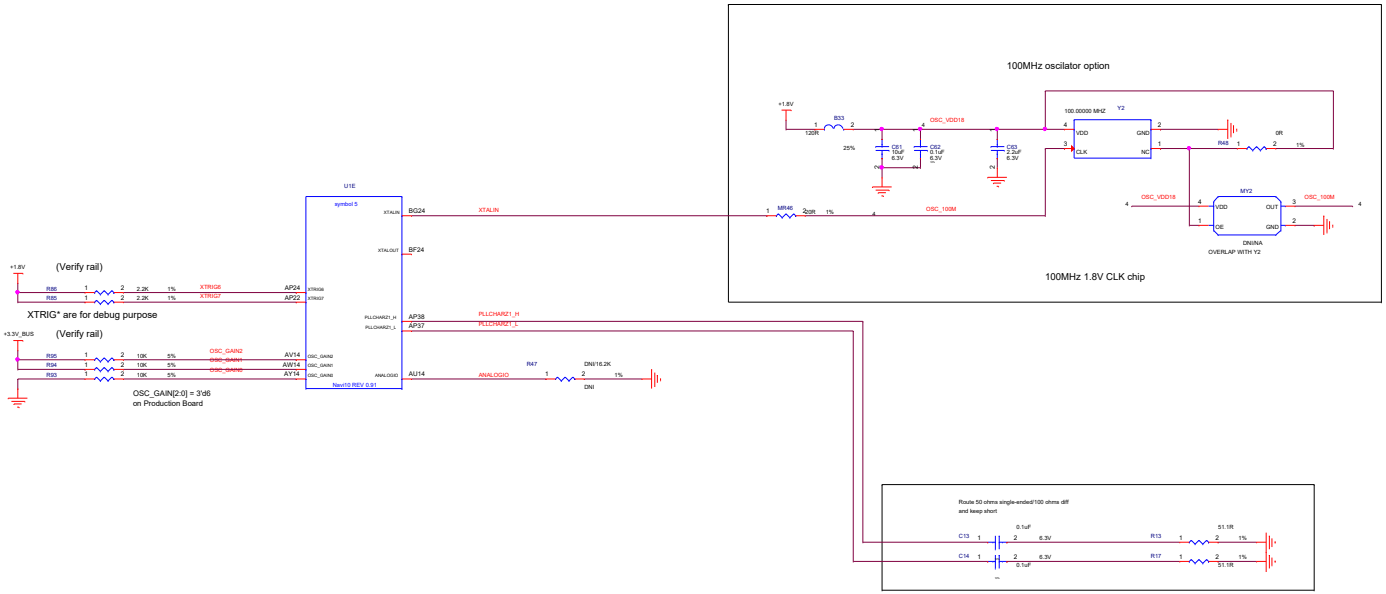

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NAVI 10 MEM INTERFACE CH A/B

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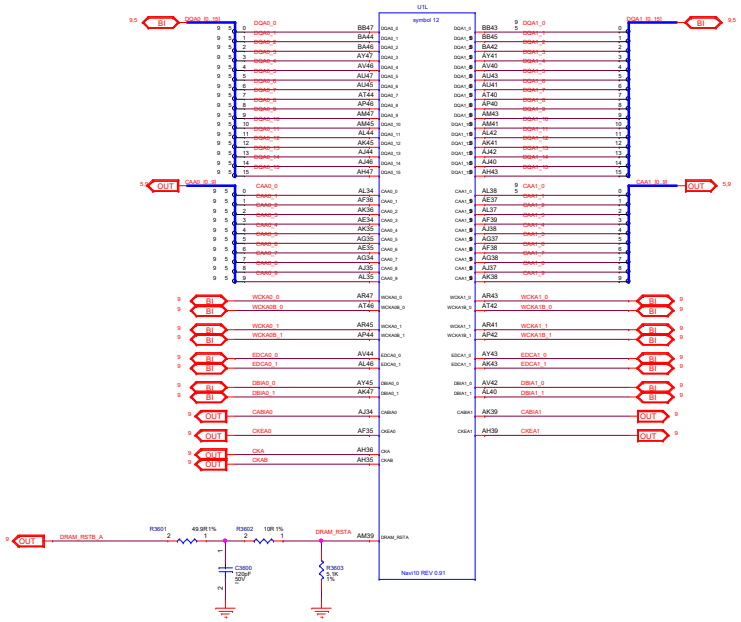

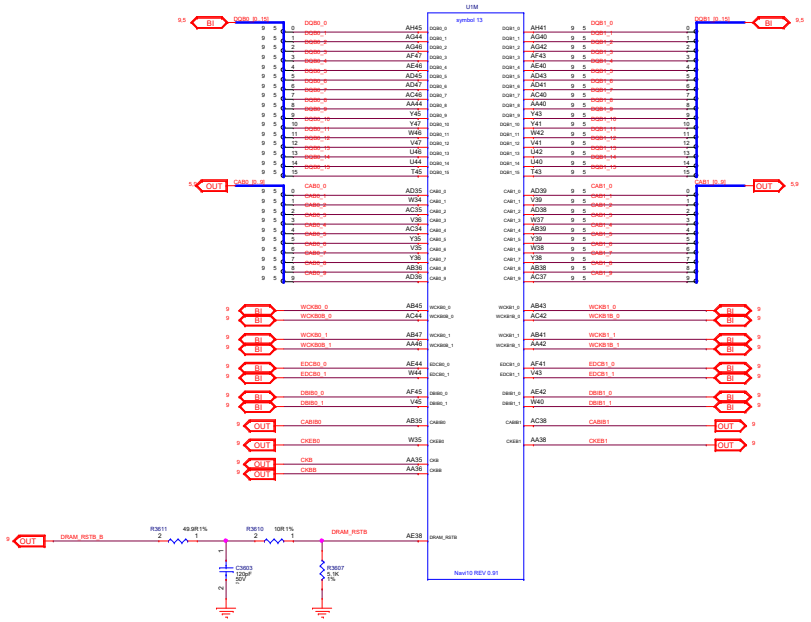

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NAVI 10 MEM INTERFACE CH C/D

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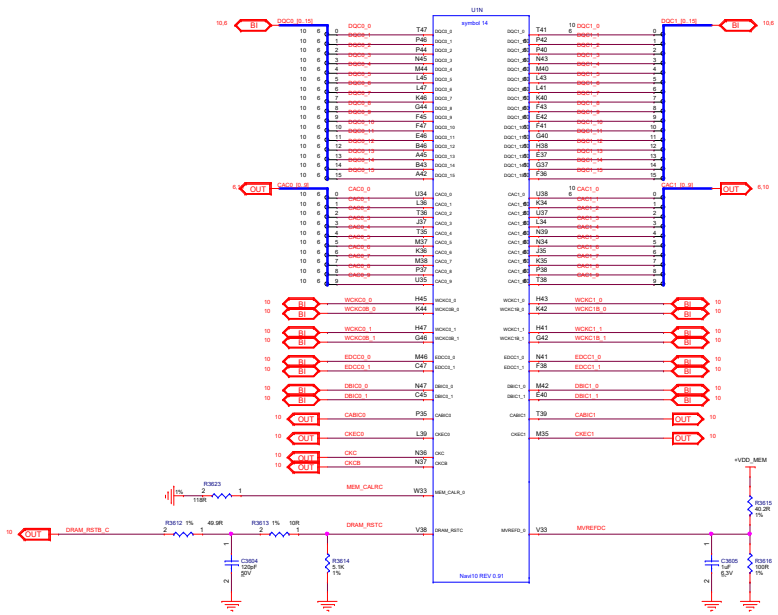

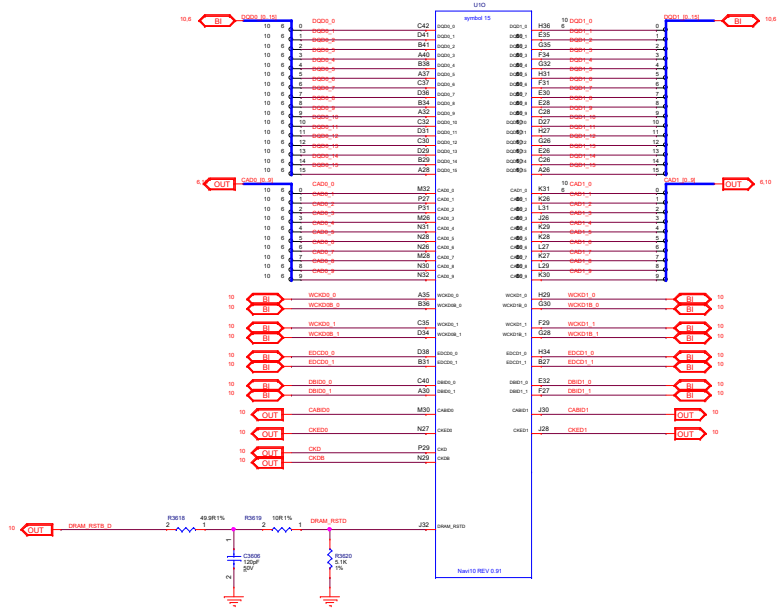

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NAVI 10 MEM INTERFACE CH E/F

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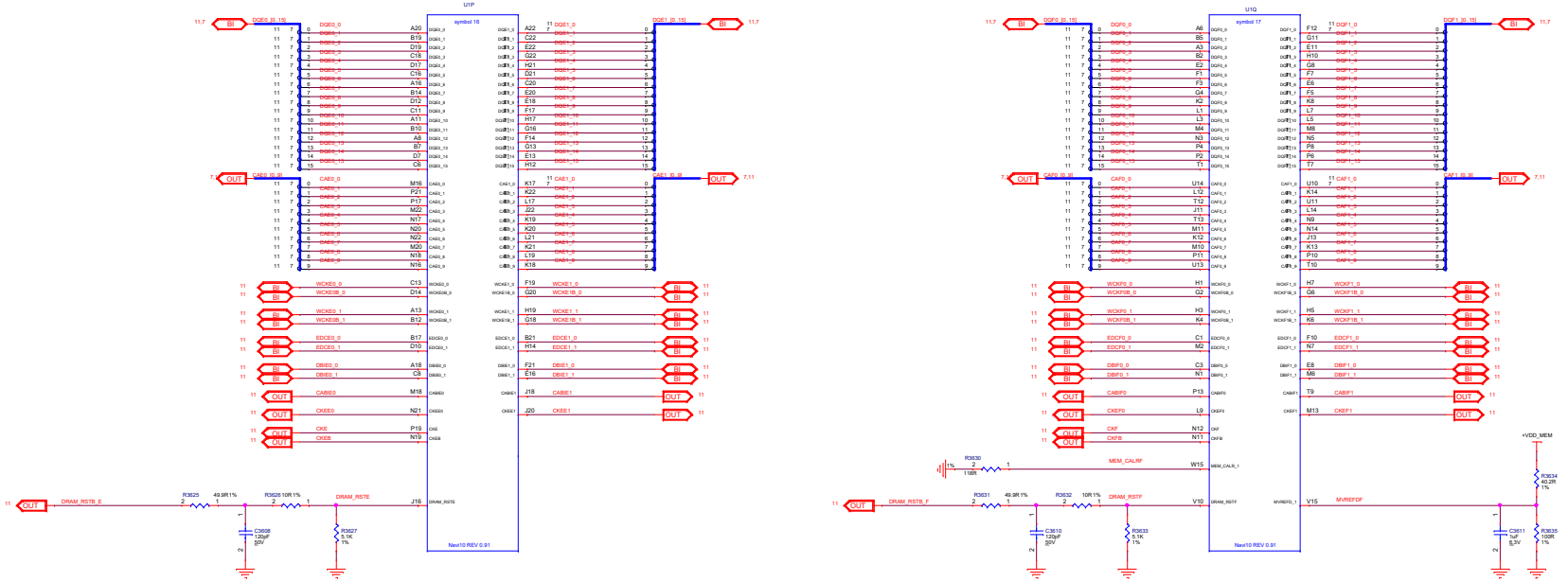

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NAVI 10 MEM INTERFACE CH G/H

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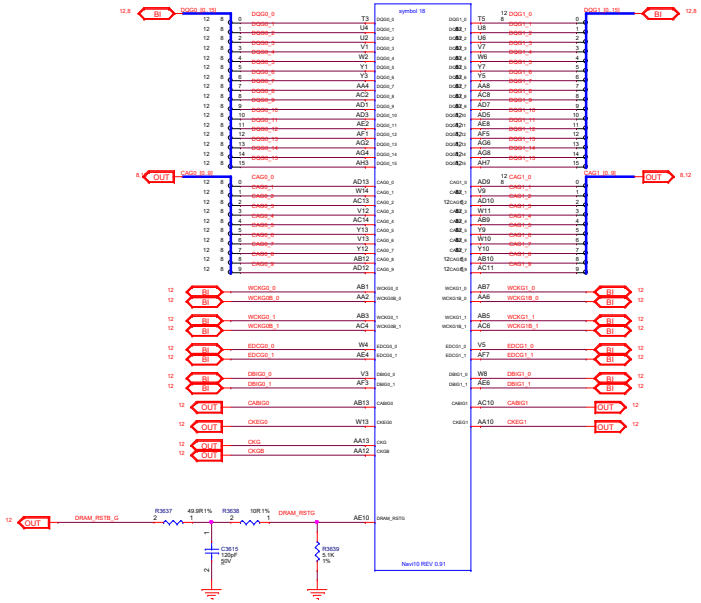

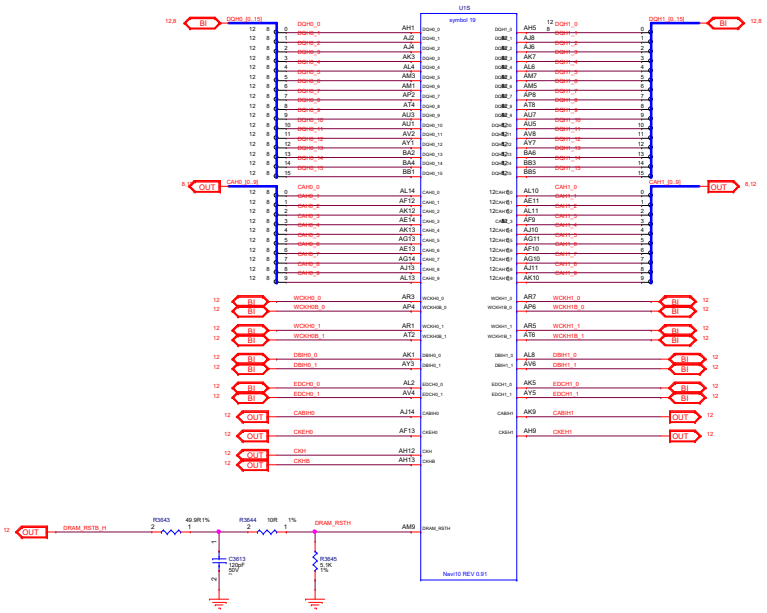

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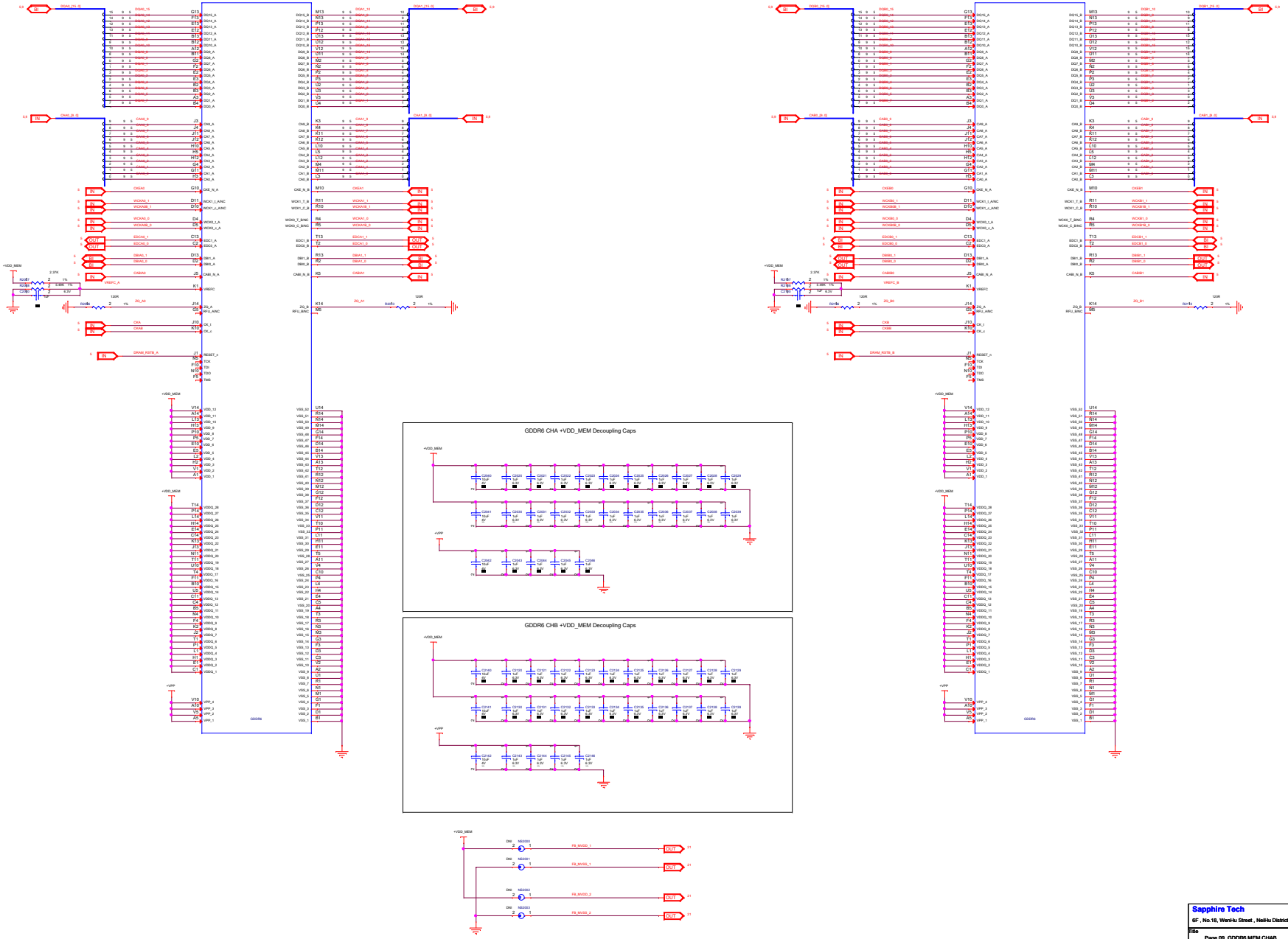

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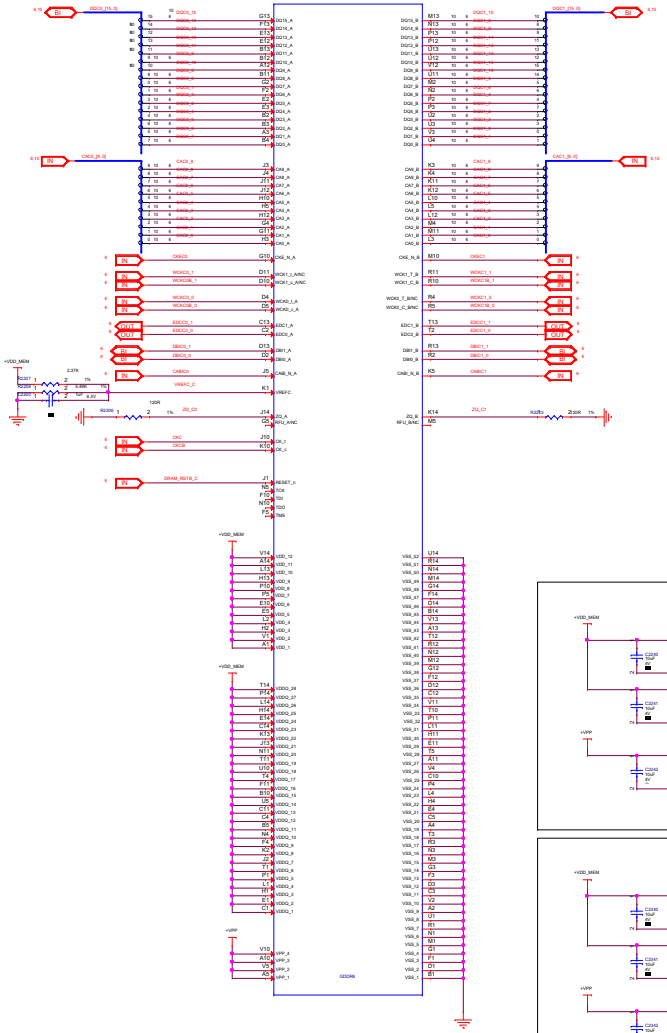

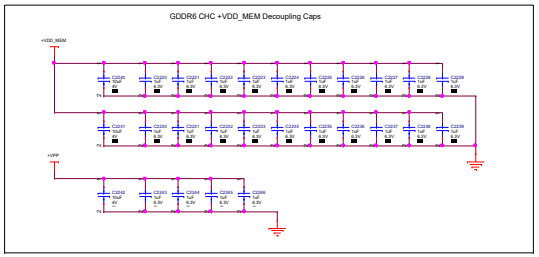

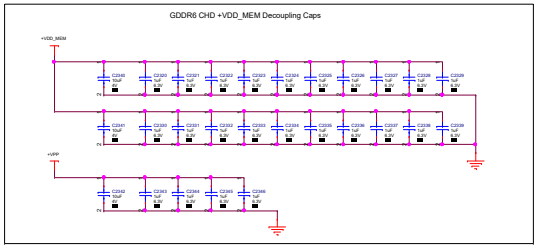

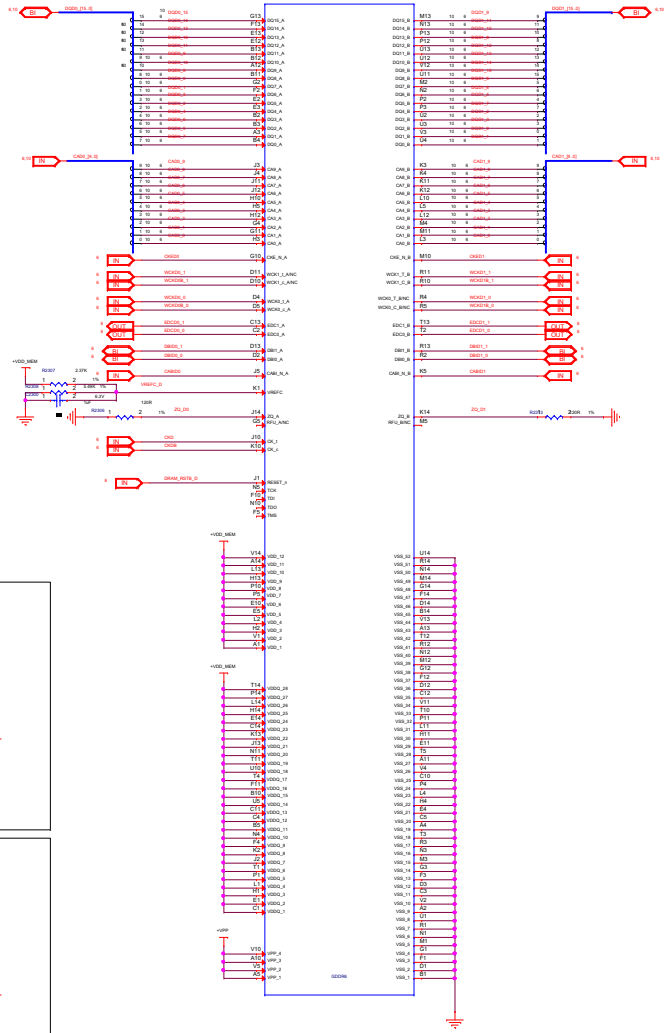

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GDDR6x16 CHEF Memory

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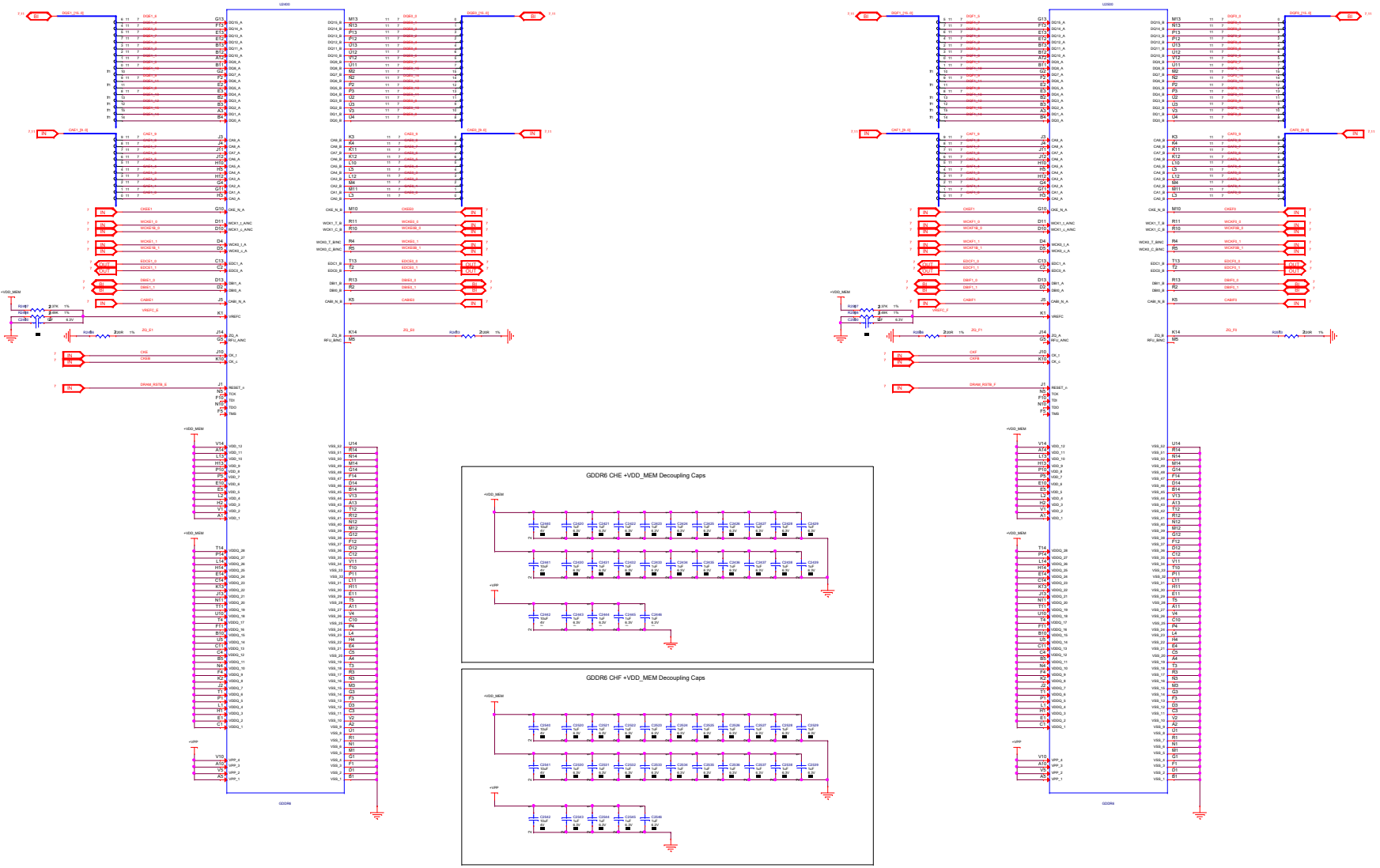

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GDDR6x16 CHGH Memory

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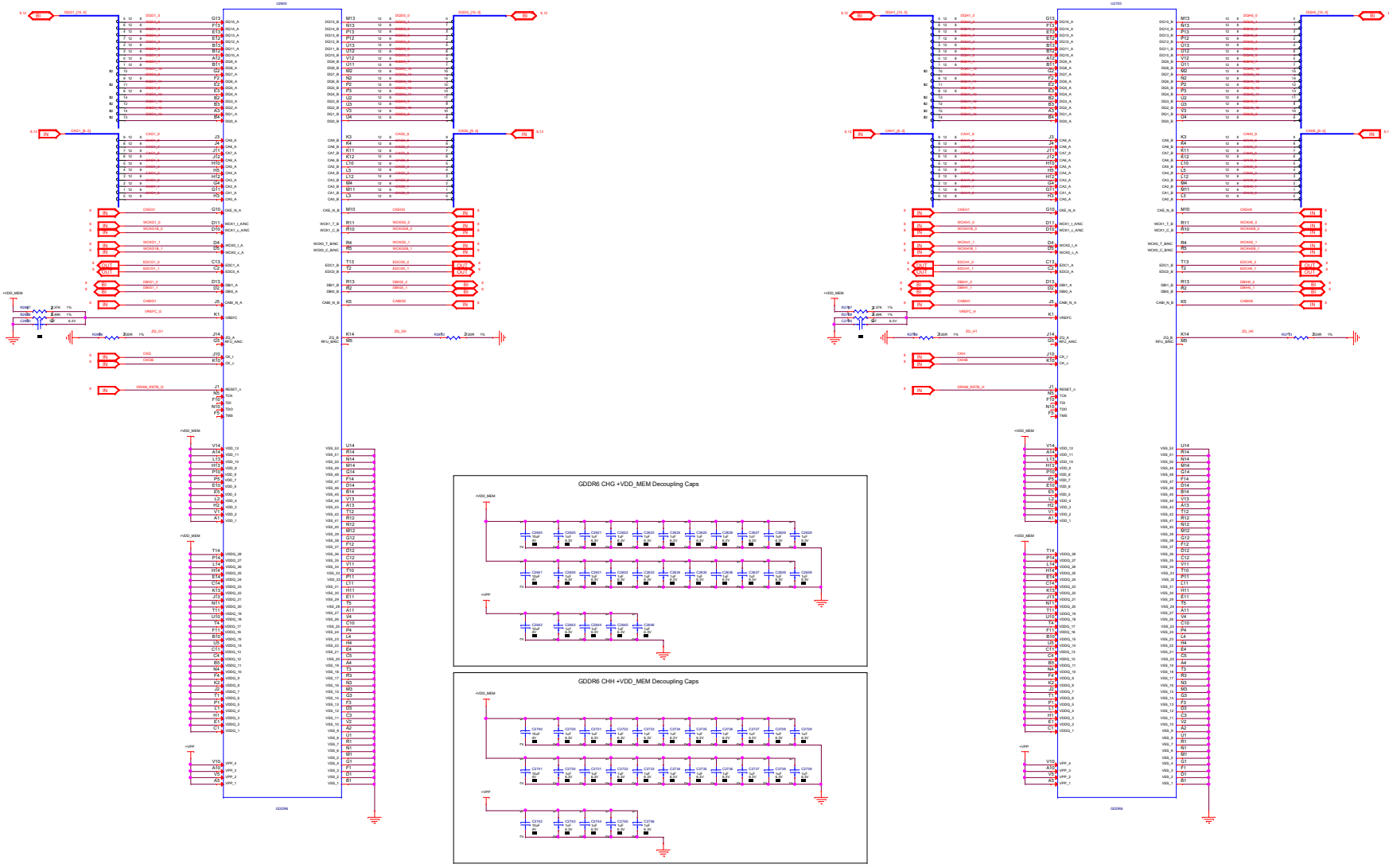

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NAVI10 TMDP A/B

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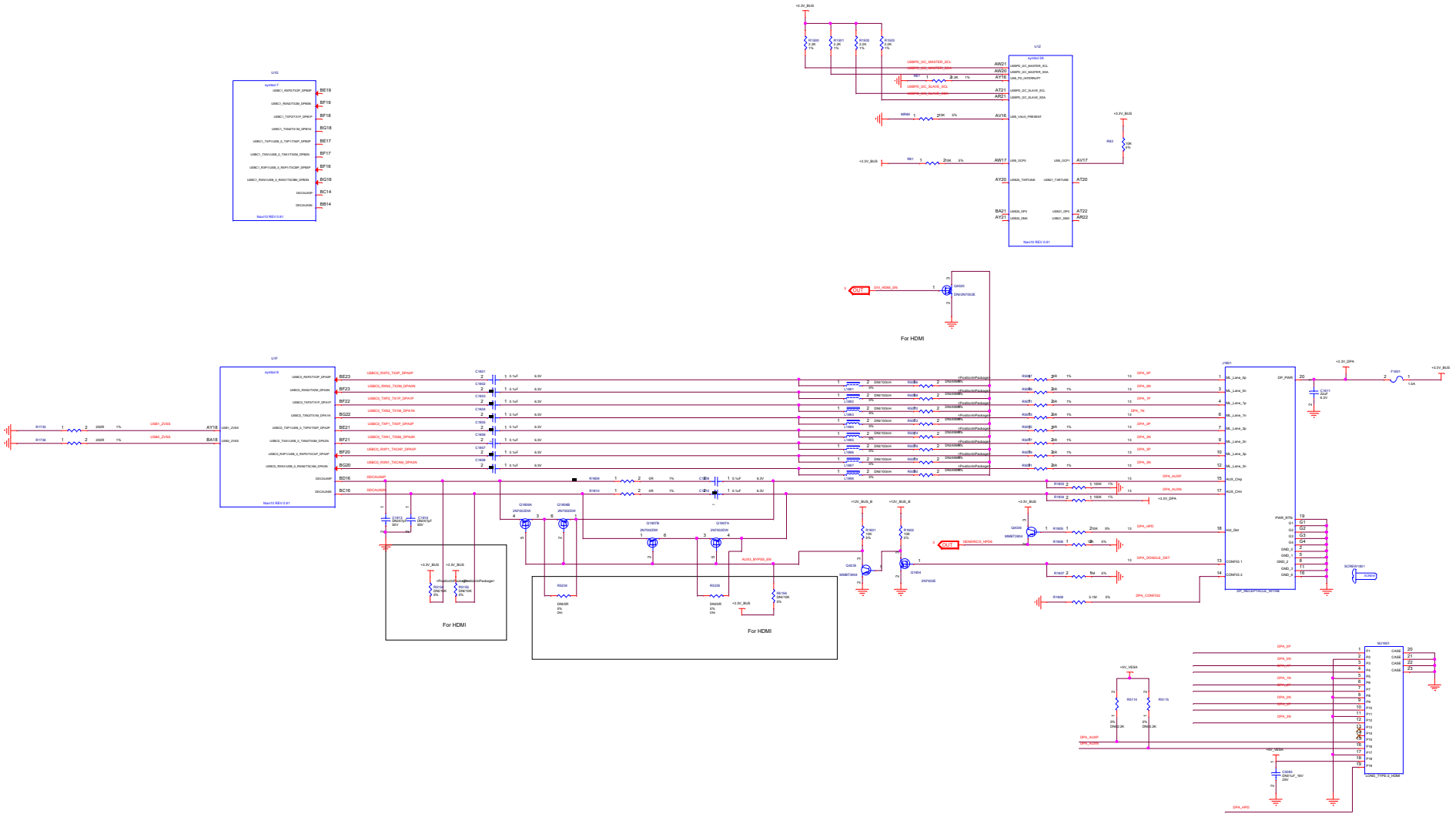

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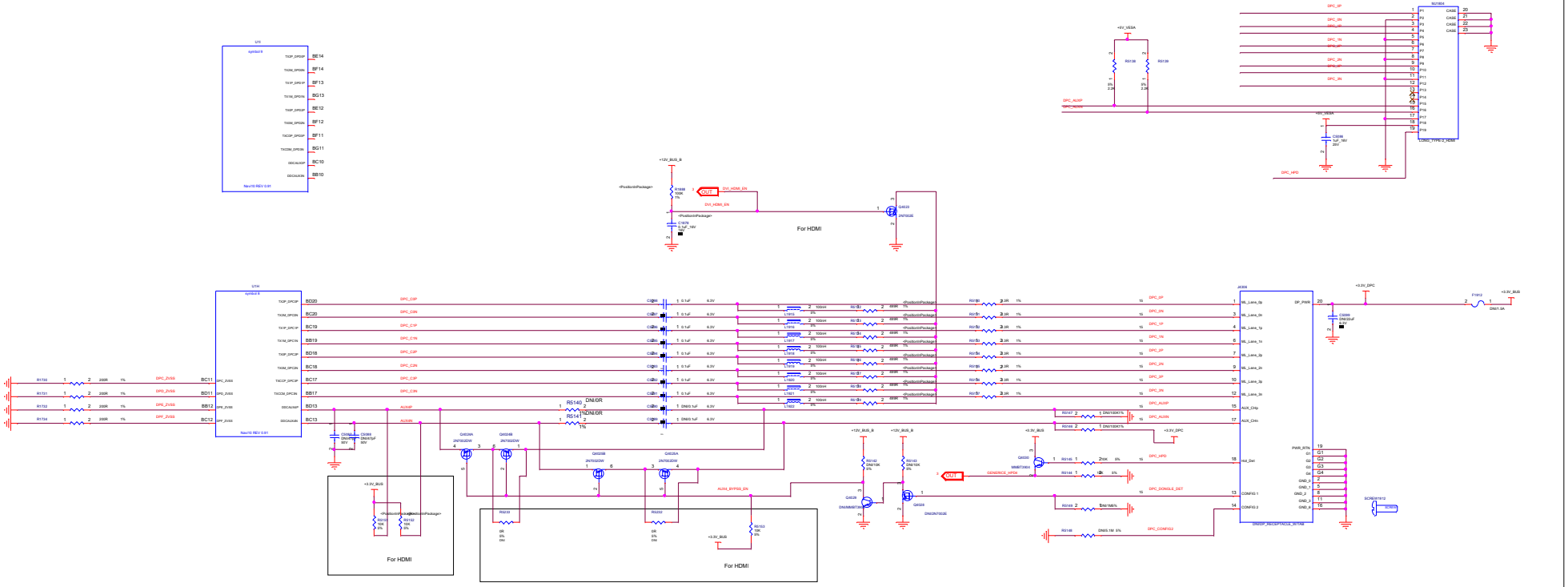
NAVI10 TMDP C/D



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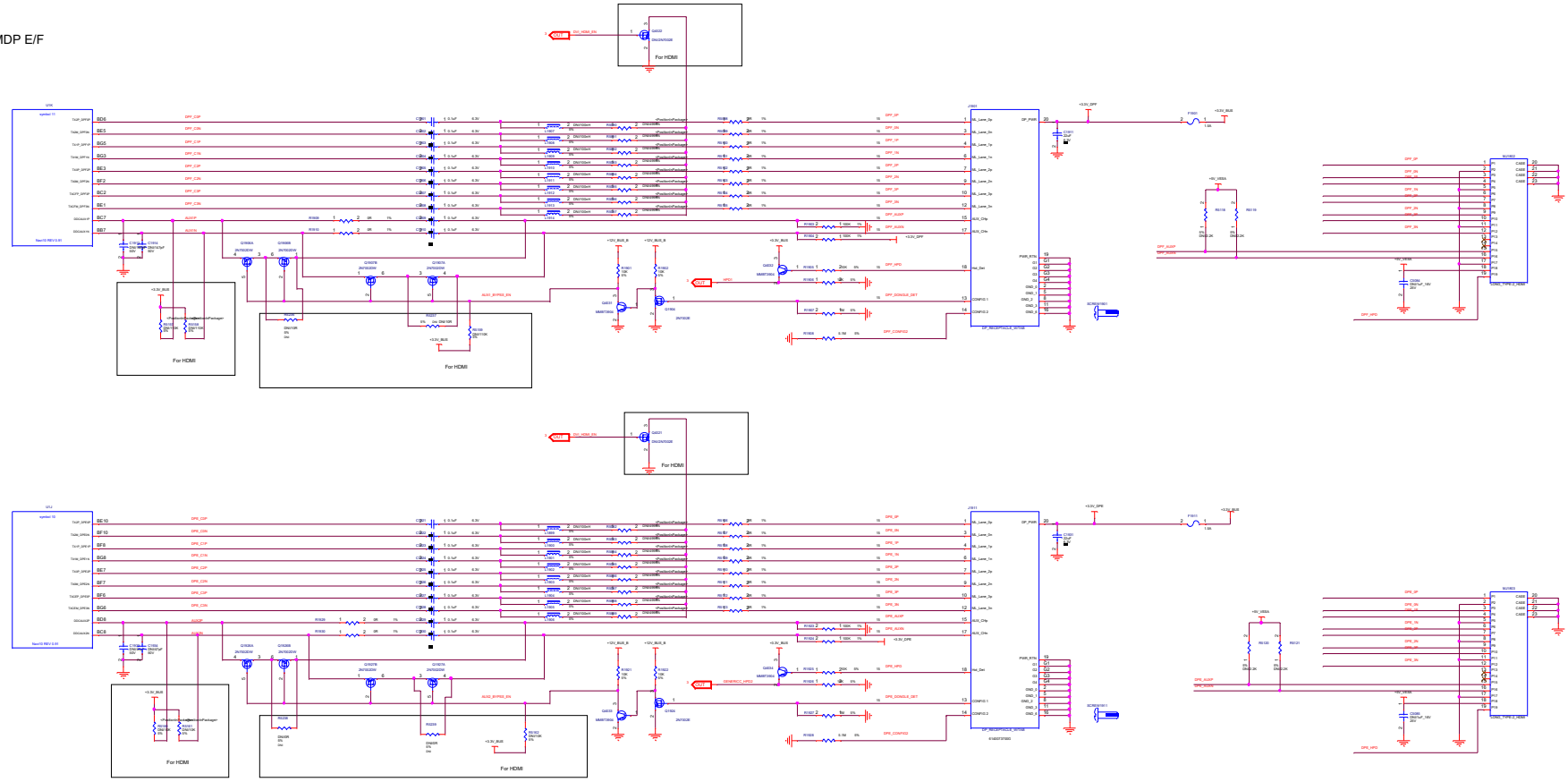
(9) NAVI10 TMDP E/F



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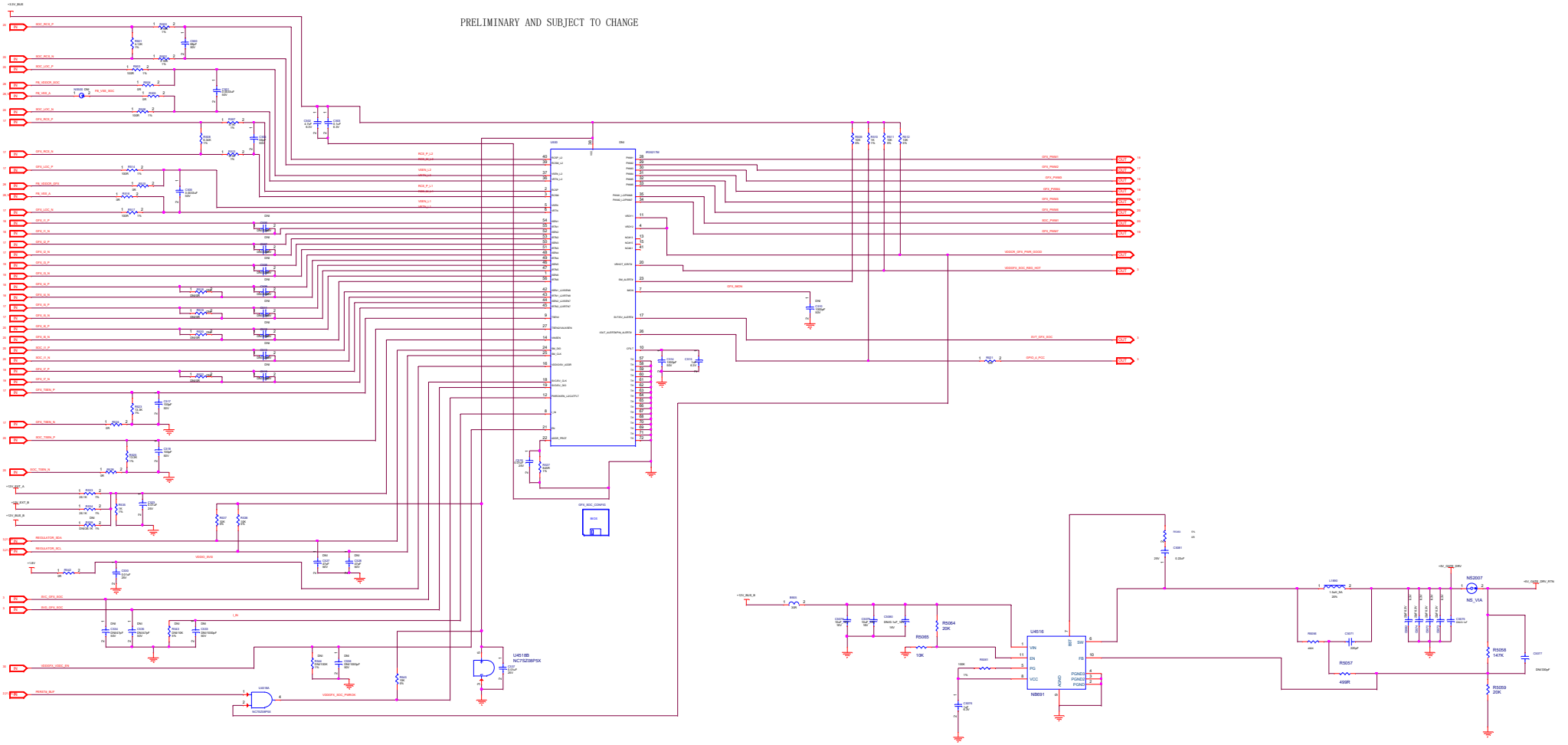

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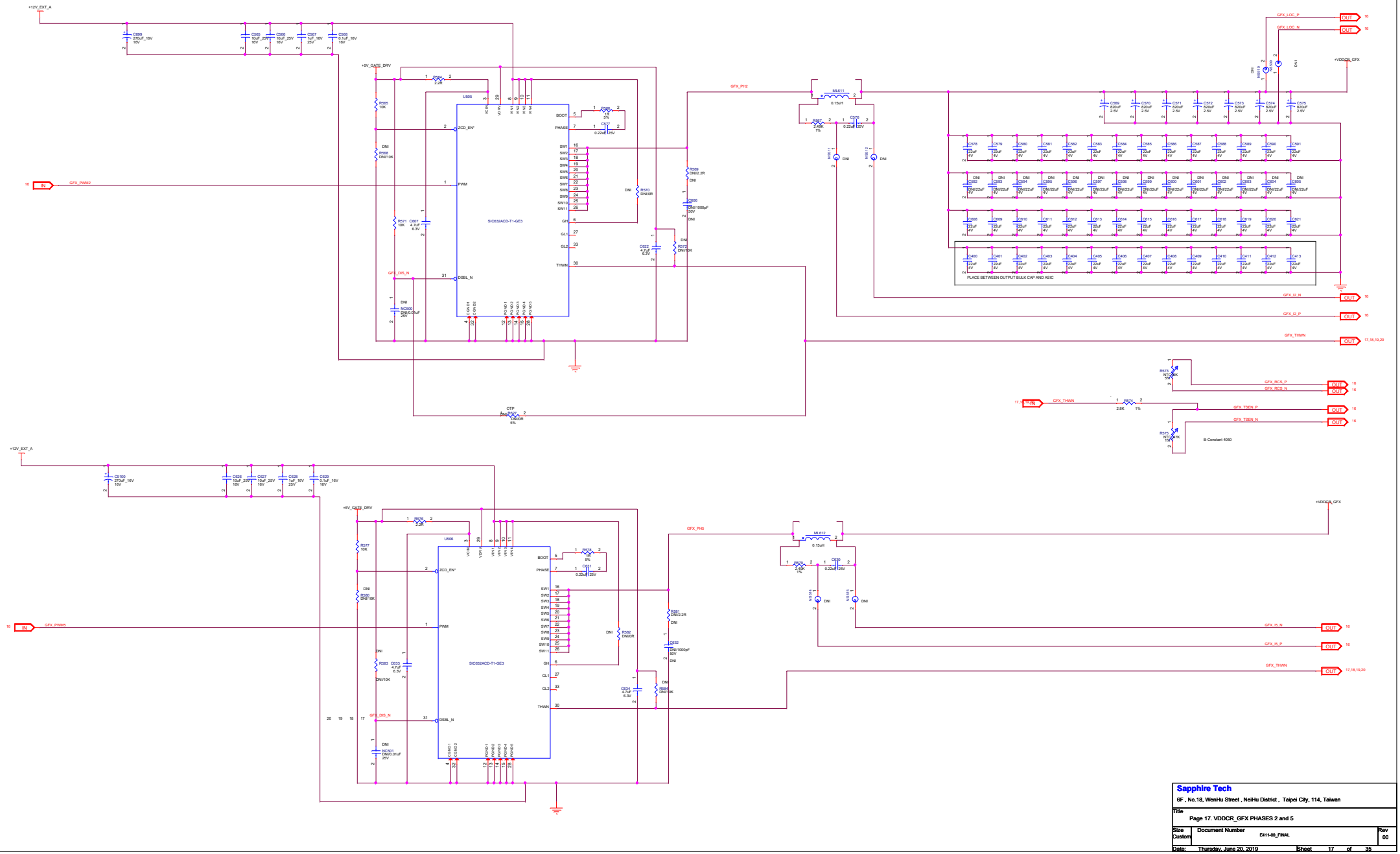

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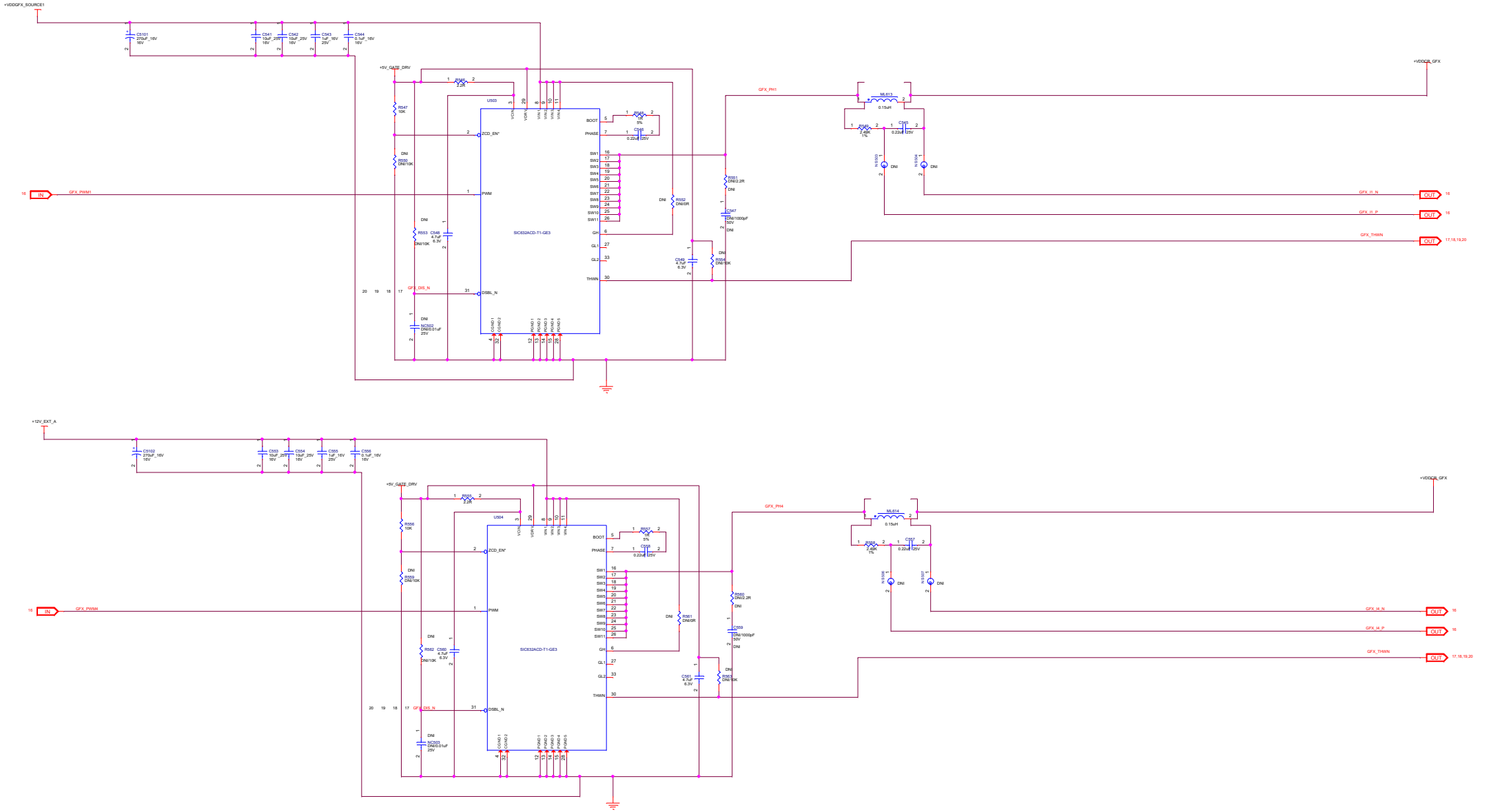

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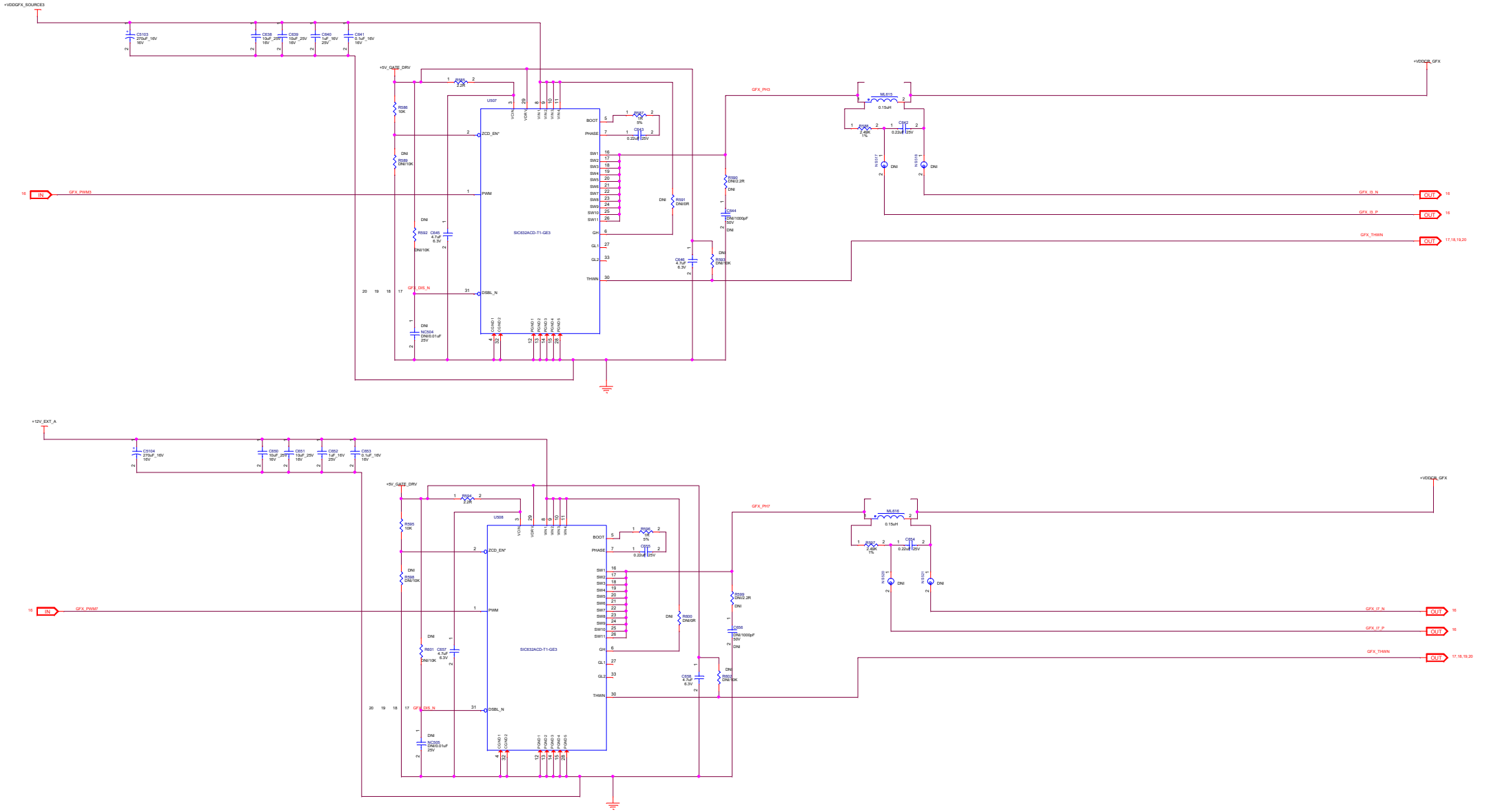

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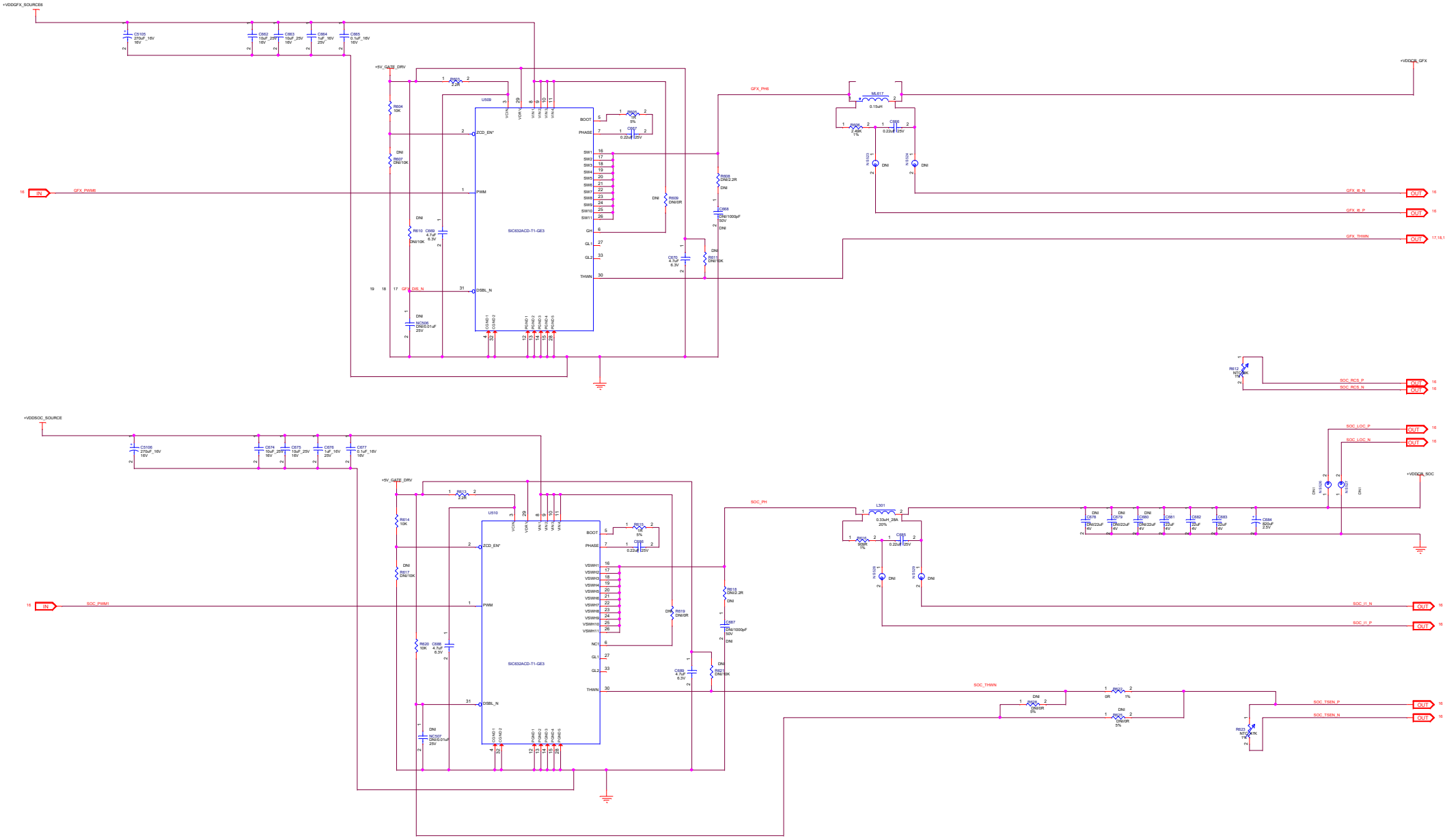

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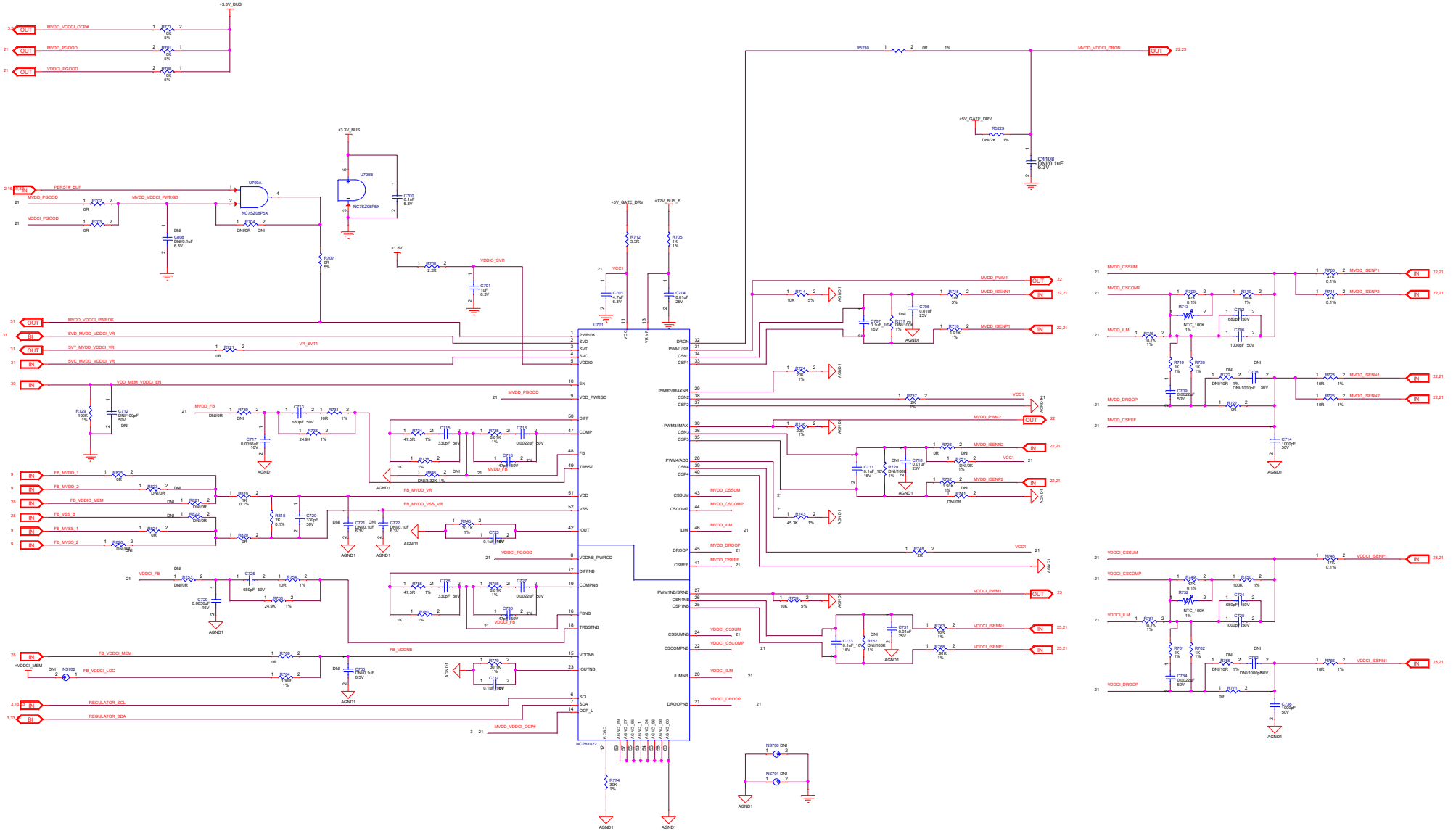

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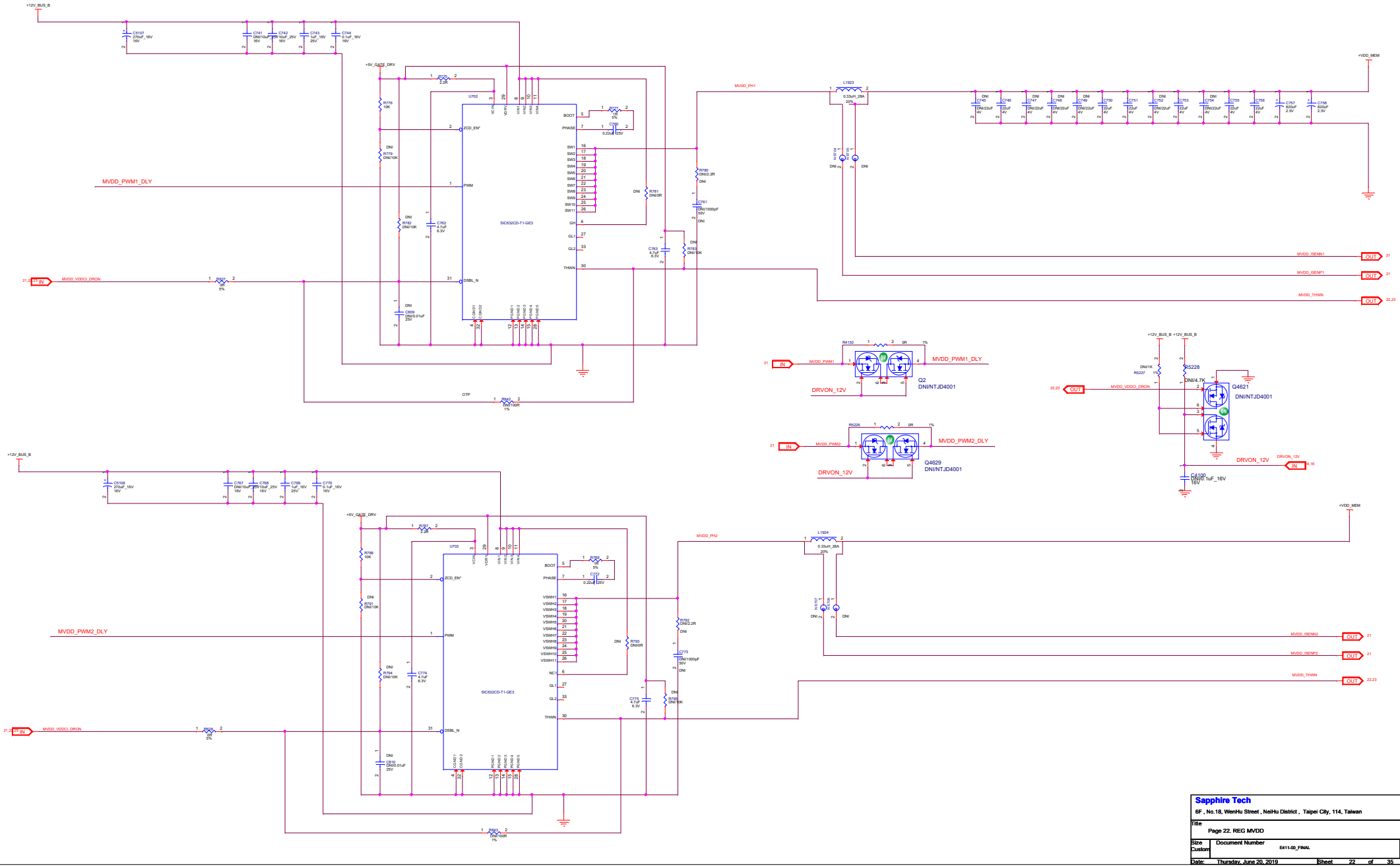

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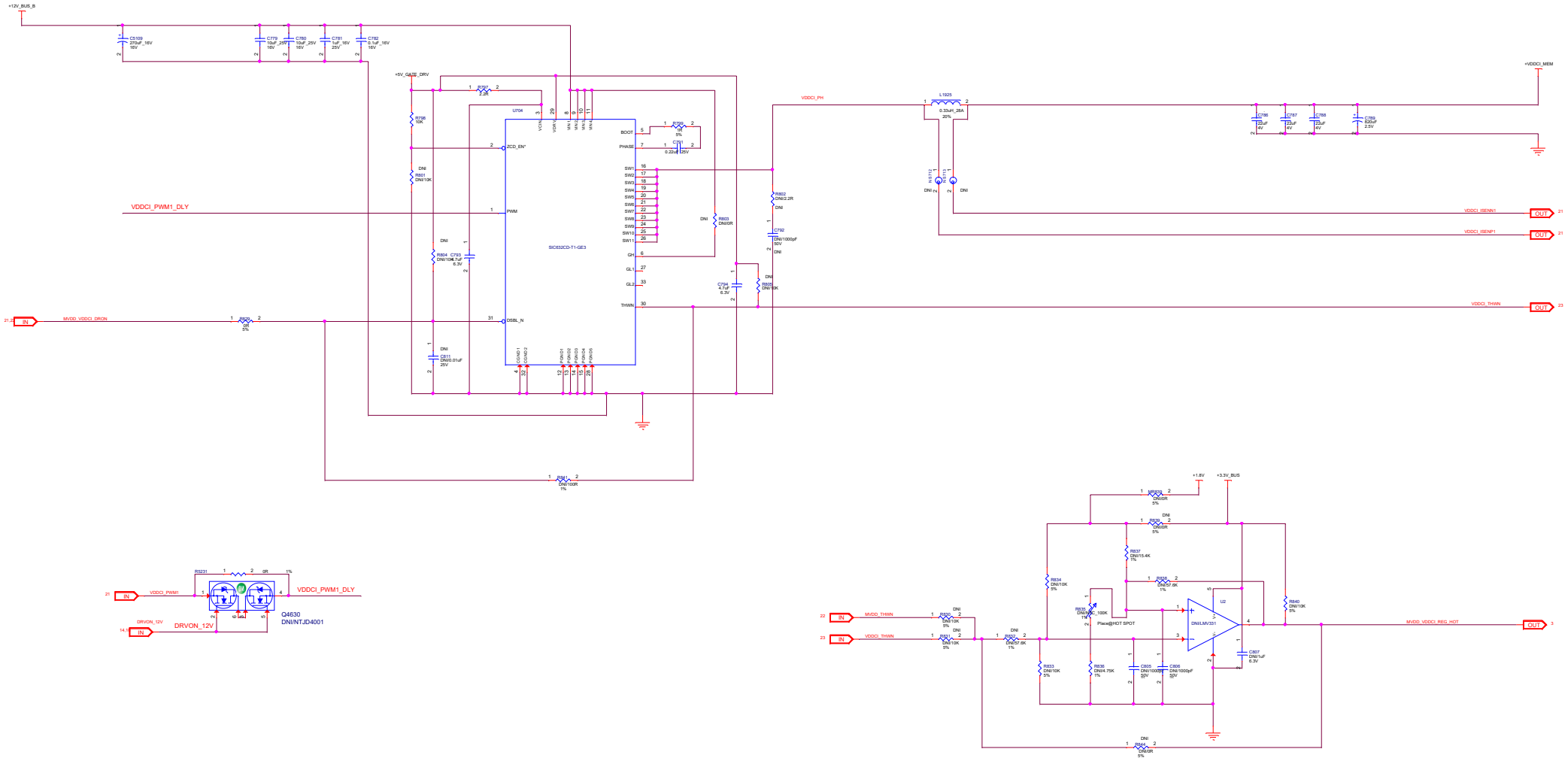

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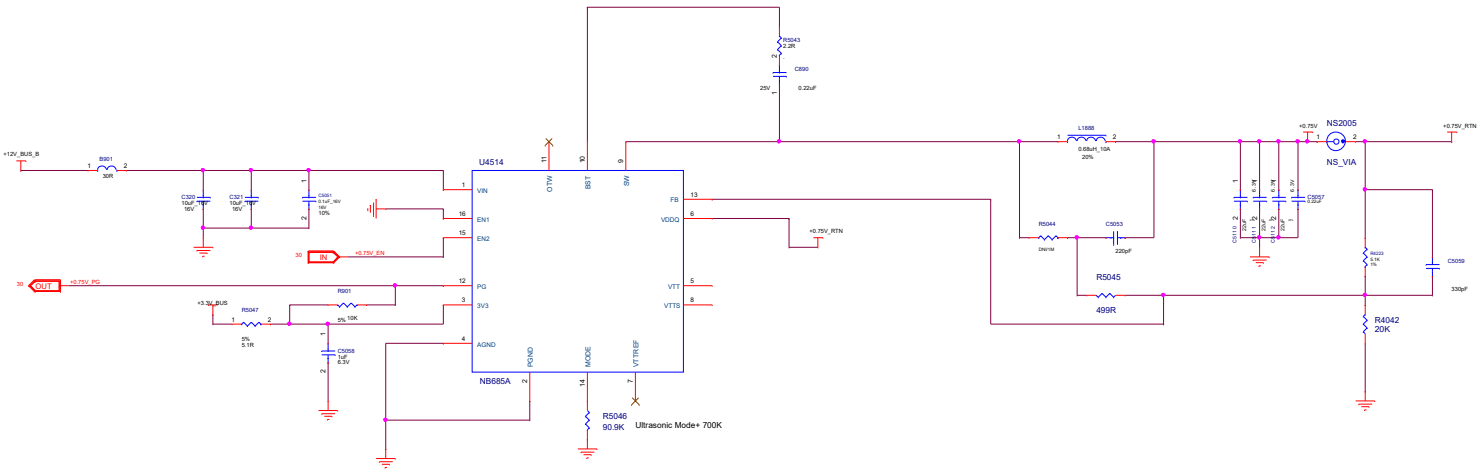

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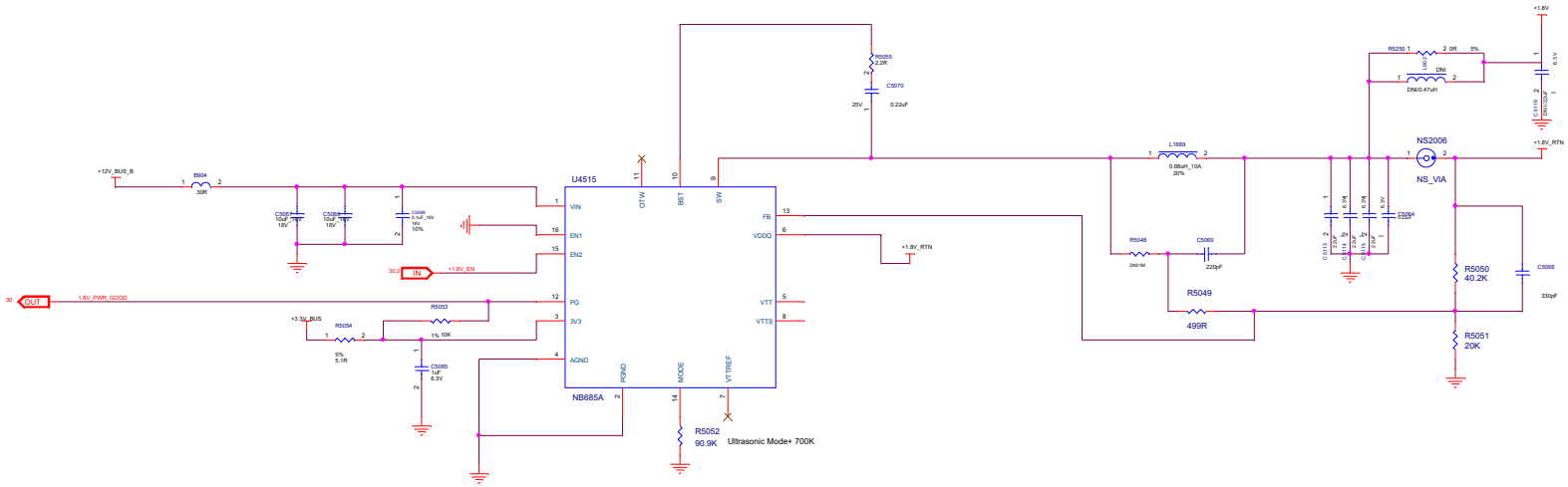

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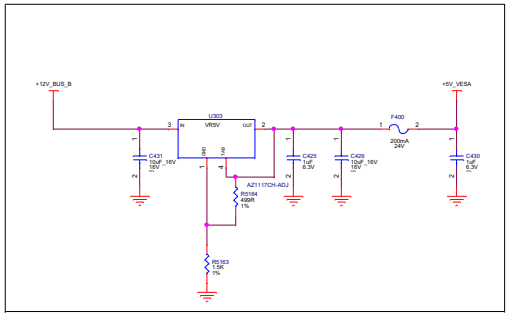
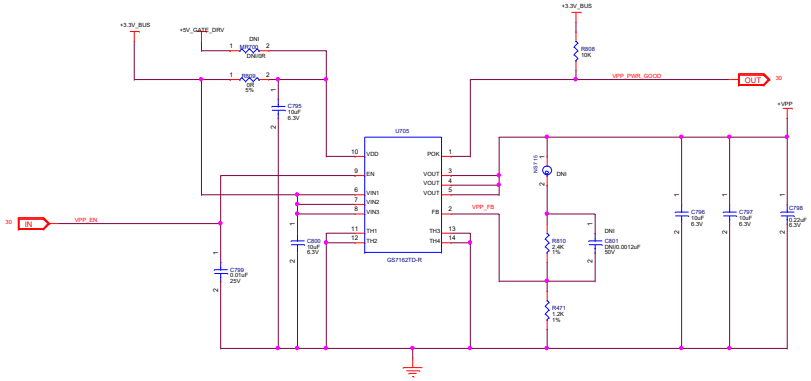
REGULATOR FOR +5V RAILS

IOUT = 50mA





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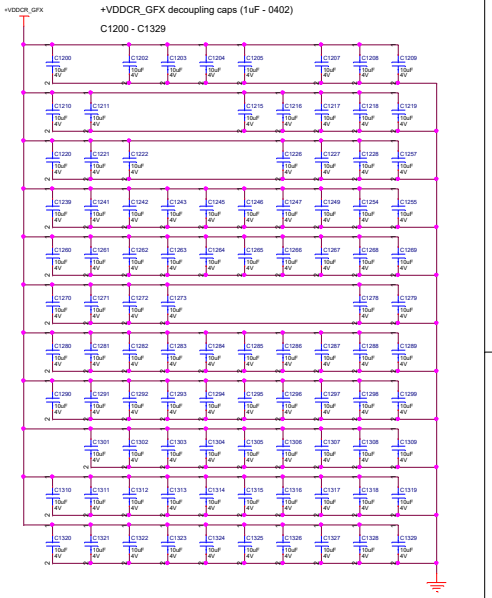
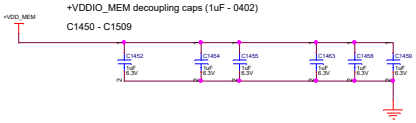
+VDDCR_GFX decoupling caps (1uF - 0402)

C1200 - C1329



+VDDIO_MEM decoupling caps (1uF - 0402)

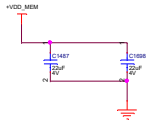
C1450 - C1509



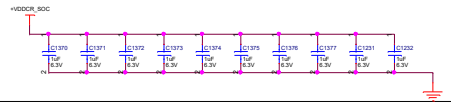
+VDDIO_MEM decoupling caps (22uF)

C1510 - C1539

0805



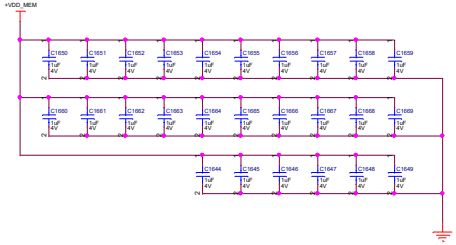
+VDDCR_SOC decoupling caps (1uF - 0402)



+VDDIO_MEM decoupling caps (1uF)

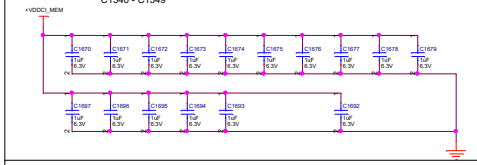
C1650 - C1669

0201



+VDDCI_MEM decoupling caps (1uF - 0402)

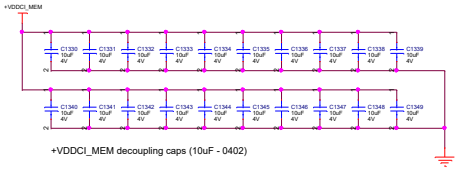
C1540 - C1549



+VDDCI_MEM decoupling caps (22uF - 0805)

C1684 - C1687 C1640 - C1642

+VDDCI_MEM decoupling caps (10uF - 0402)



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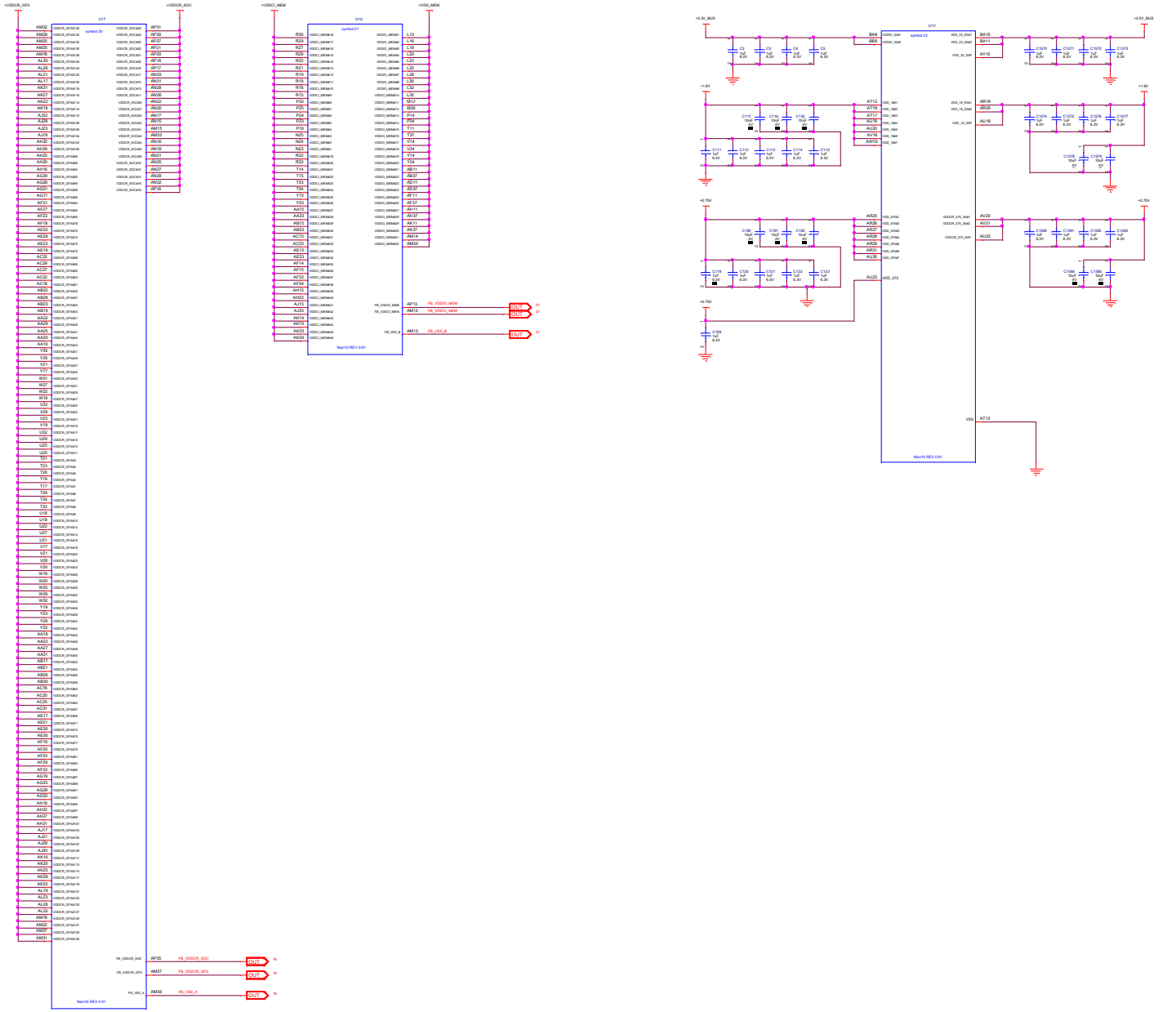

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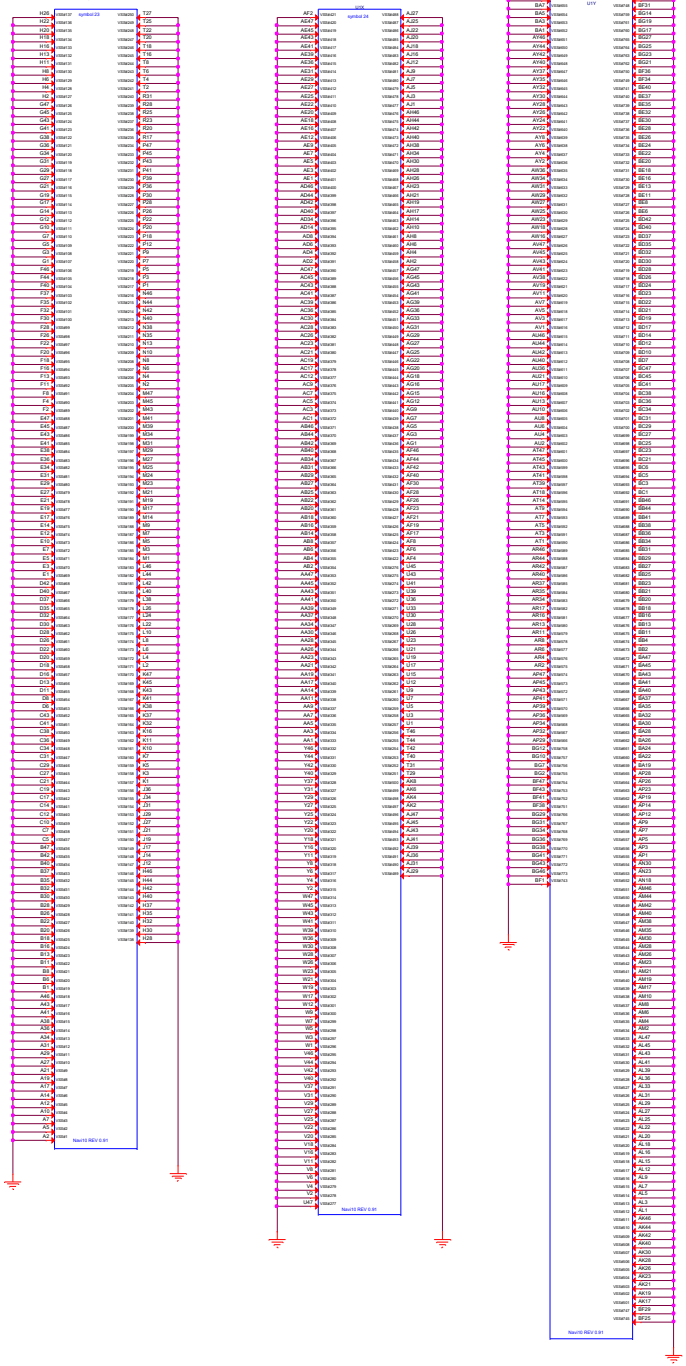

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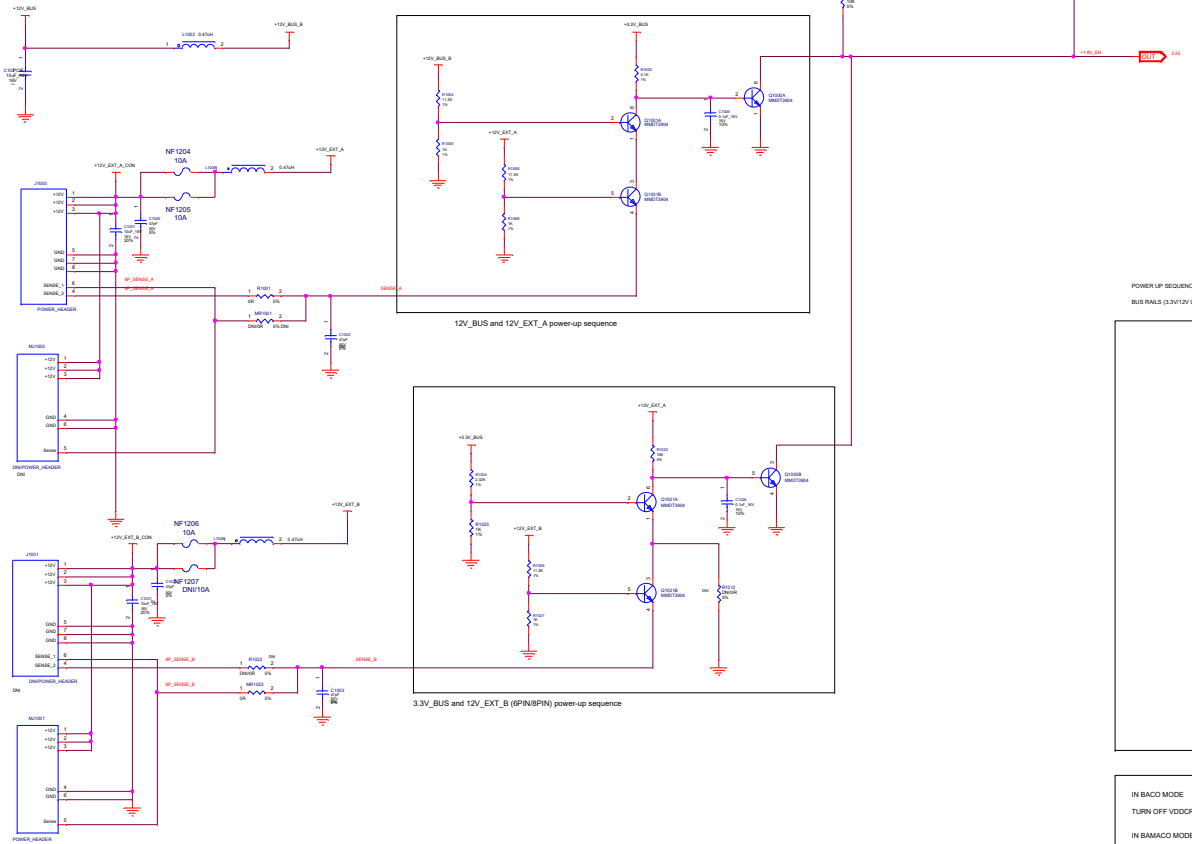
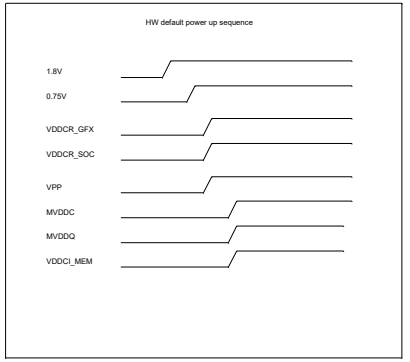
PRELIMINARY AND SUBJECT TO CHANGE

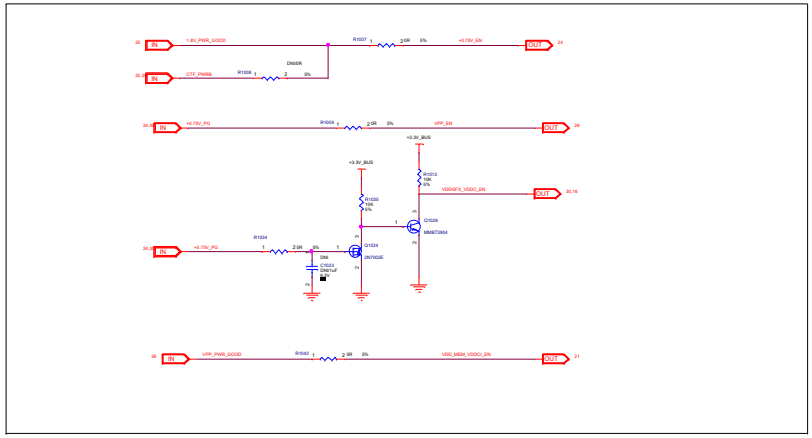




POWER UP SEQUENCE

BUS RAILS (3.3V/12V UP)-> +1.8V -> 0.75V -> VDDGFX/VDDSOC

-> VPP -> VDDCI/MVDD

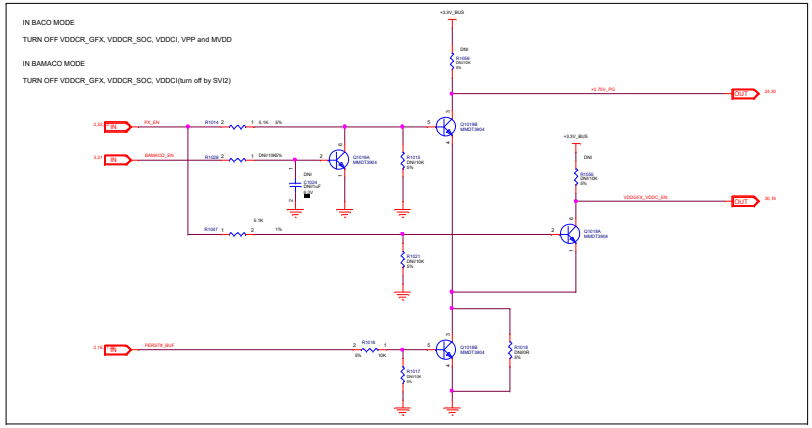


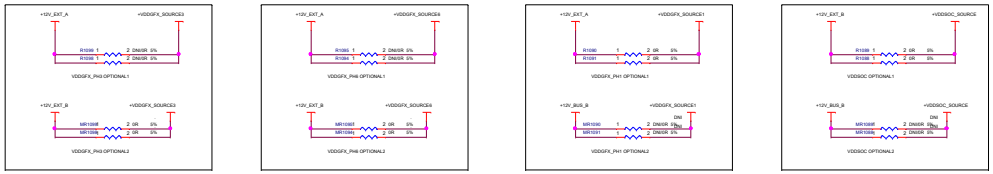
IN BACO MODE

TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI, VPP and MVDD

IN BAMACO MODE

TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI(turn off by SVI2)





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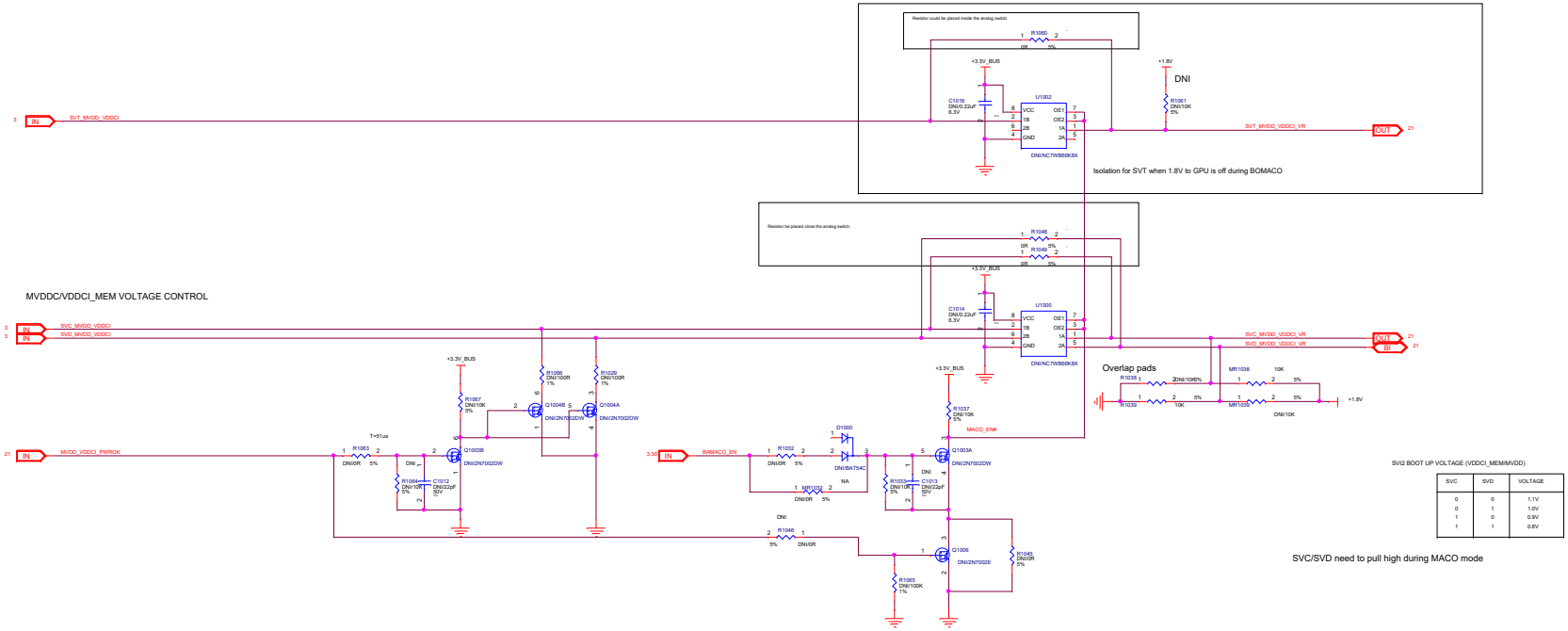

SVC	SVD	VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

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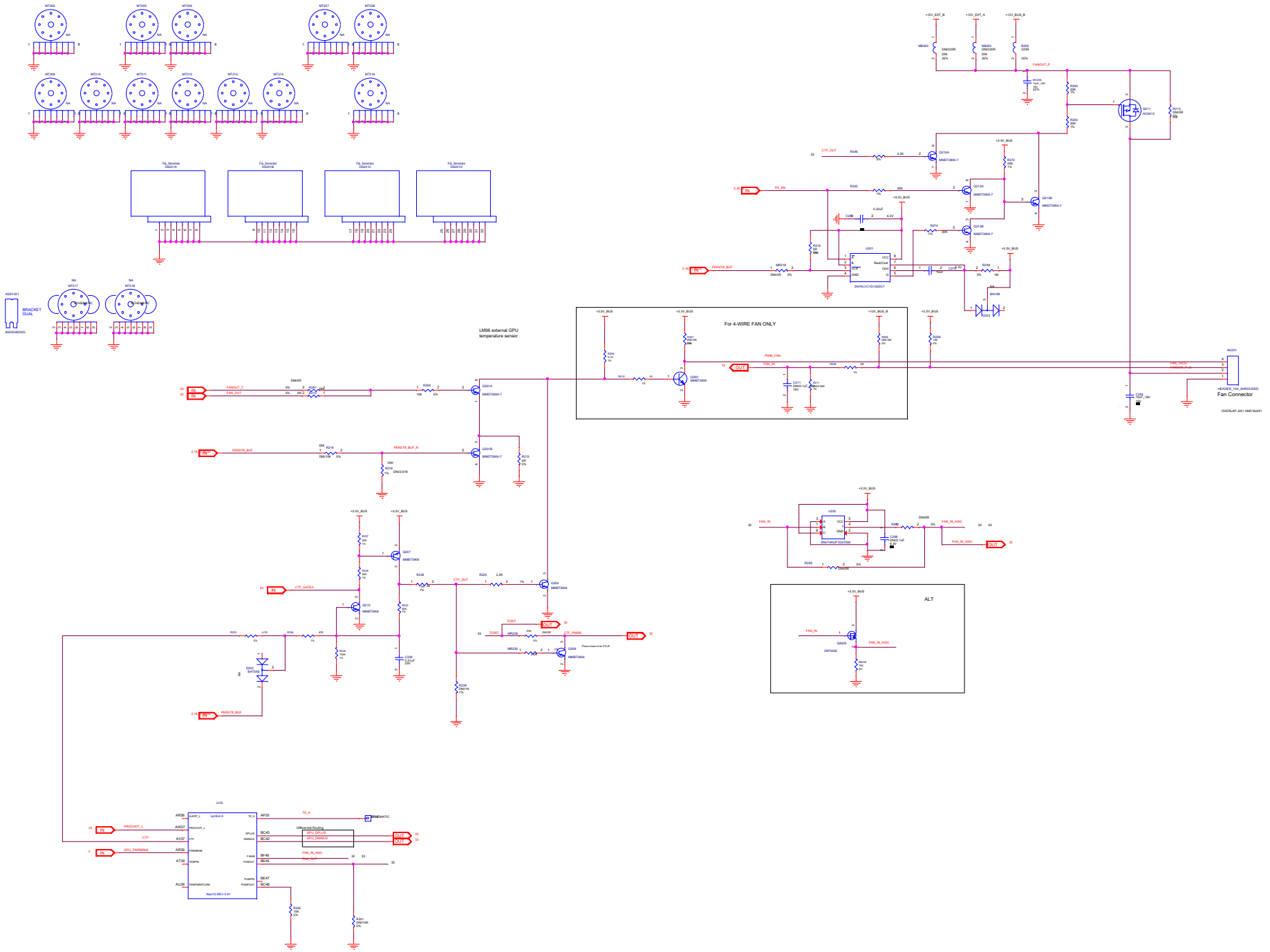

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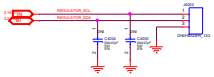

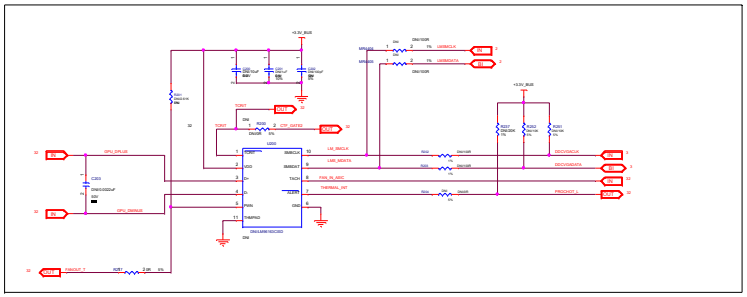

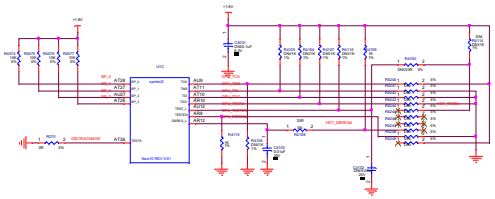

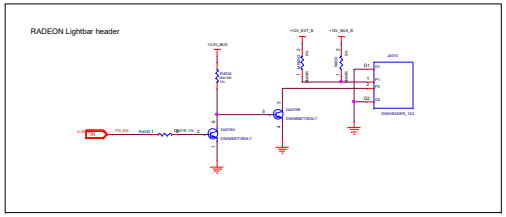

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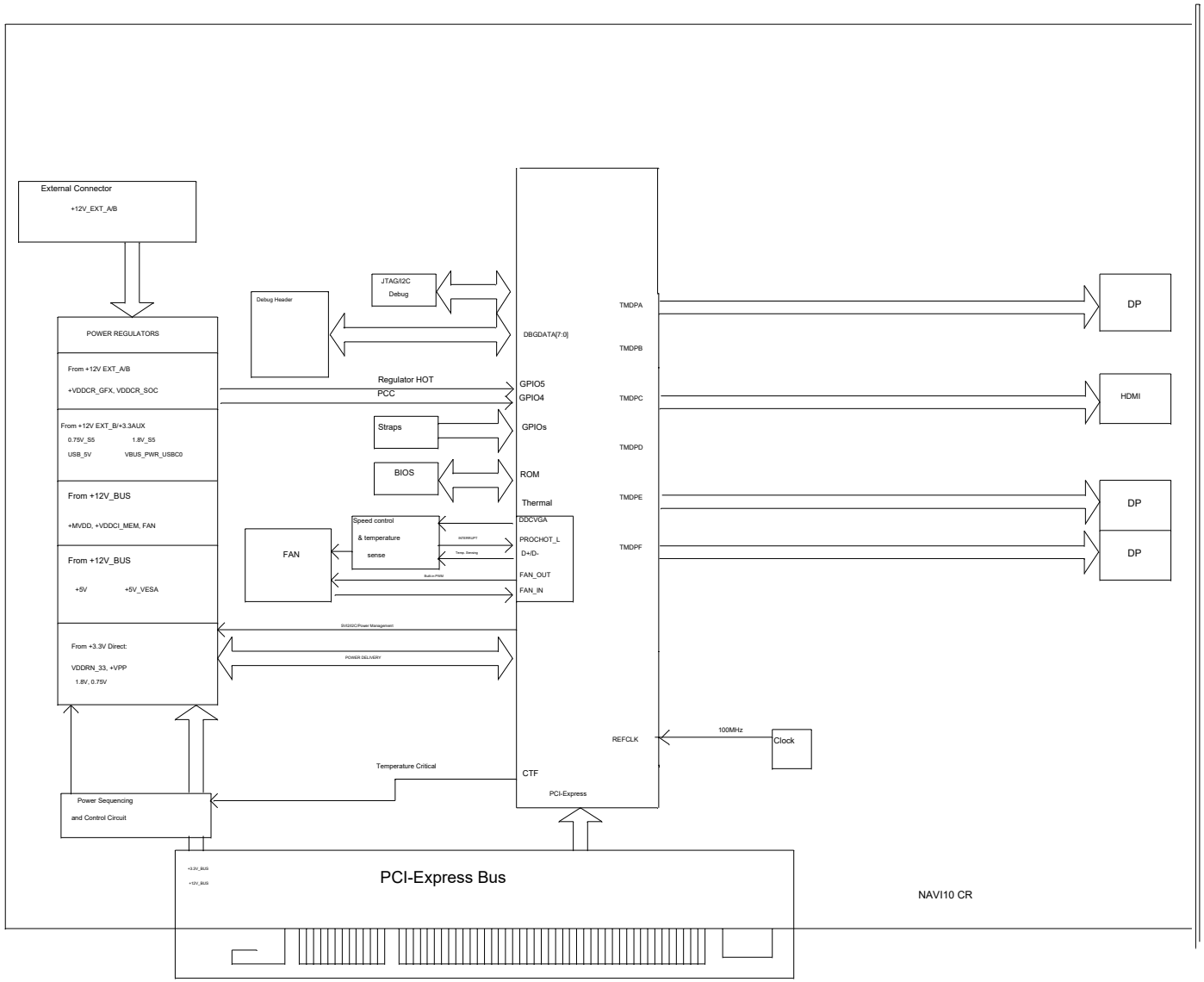

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1	-00A	FEB 11 2019	-00A schematics

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