P555-A00: G84M MXM V2.0 256/512MB 128-BIT GDDR2 LVDS, DVI-A, DVI-B, TV-OUT, VGA, HDMI SLI, HDCP, MXM V2.0 TTP SUPPORT

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	KU	VARI ANT	NVPN	ASSEMBLY
Г	В	BASE	600-10555-9998-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
	1	SKU0001	600-10555-0001-000	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V2.0, HDCP.
	2	SKU0002	600-10555-0002-000	G84M-600 450/400 512MB 128bit GDDR2 32Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V2.0, HDCP.
	3	SKU0003	600-10555-0003-000	G84M-700 700/400 512MB 128bit GDDR2 32Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V2.0, HDCP.
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P407\_A01 to P555\_A00 change list:

1) Change MEC1 JEDEC\_TYPE from MCH\_MXM2\_HOLES to MECH\_MXM2\_HOLES\_103NP\_4VIAS

2) Add pull low resistor to MIOA\_D[0] for straps

3) Add pull up resistor to MIOA\_D[6] for straps

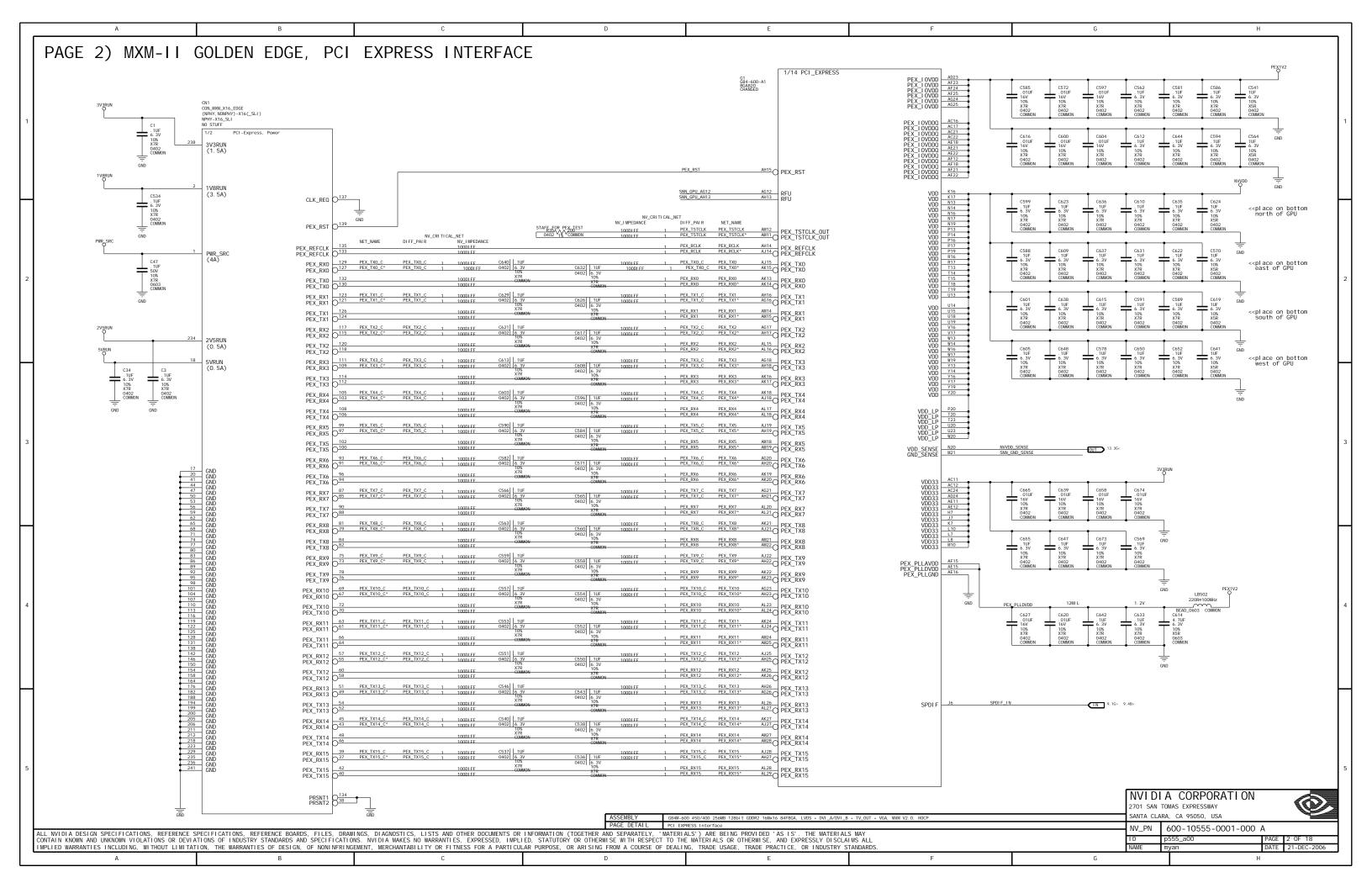
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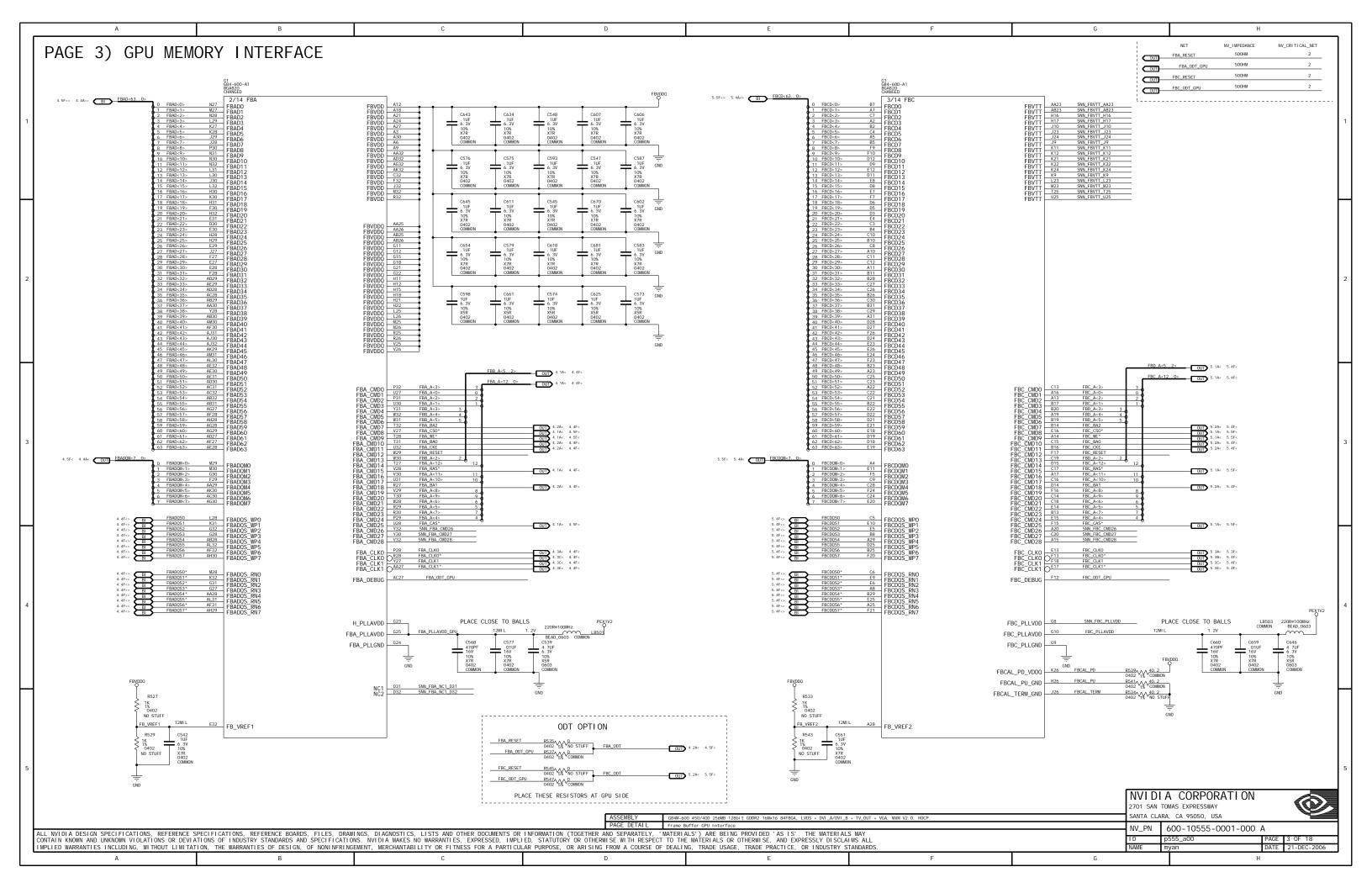
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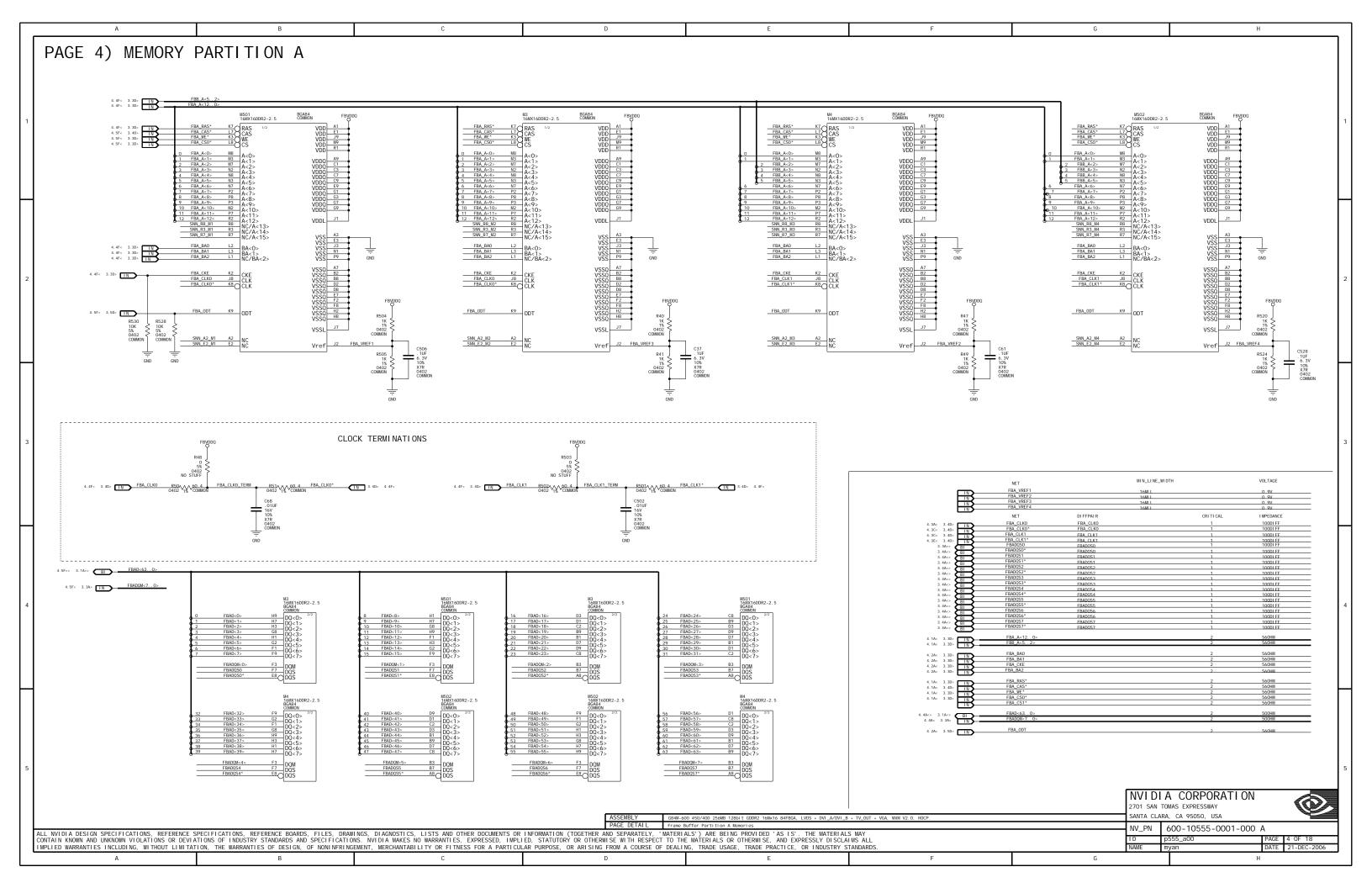
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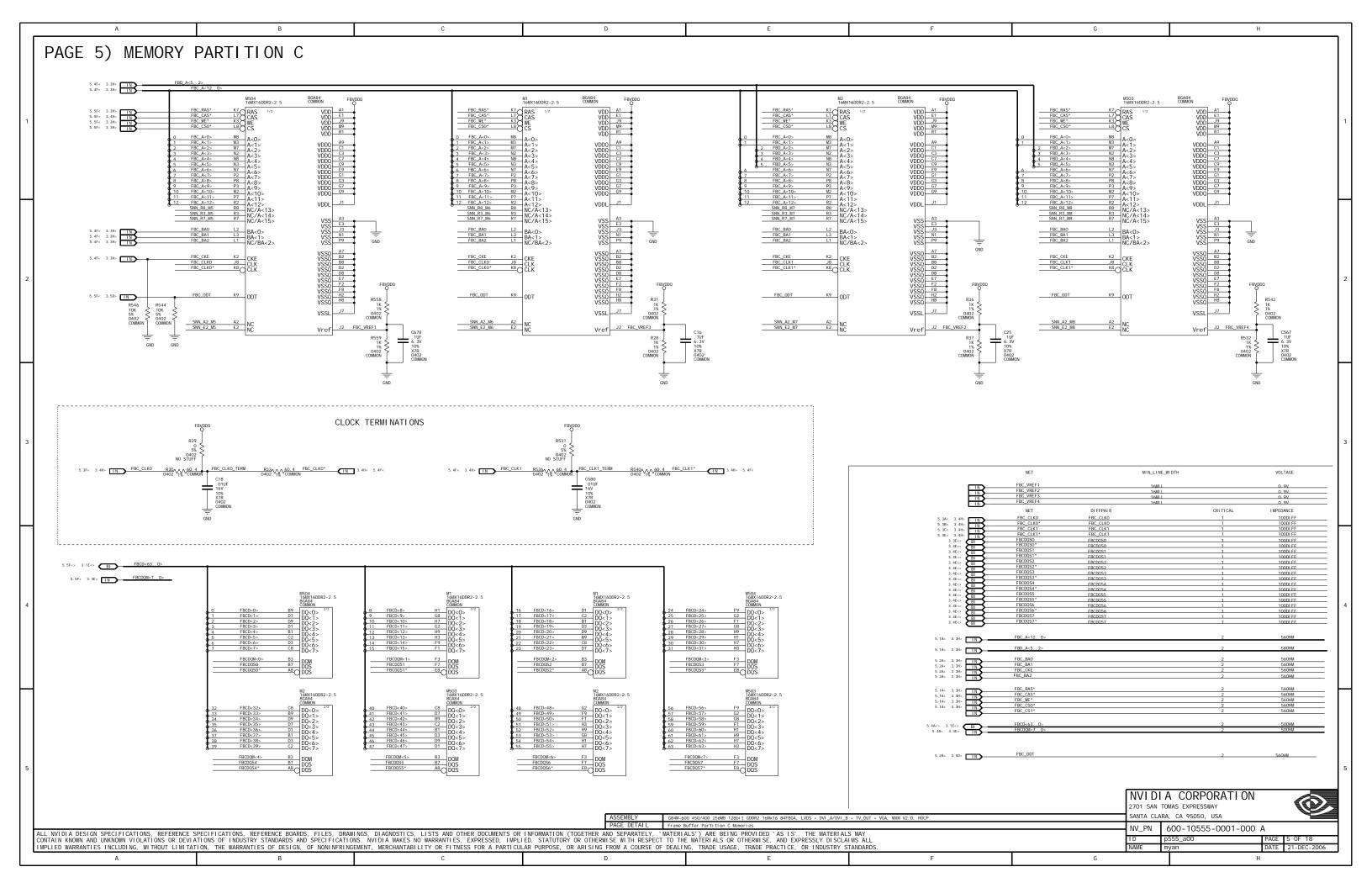
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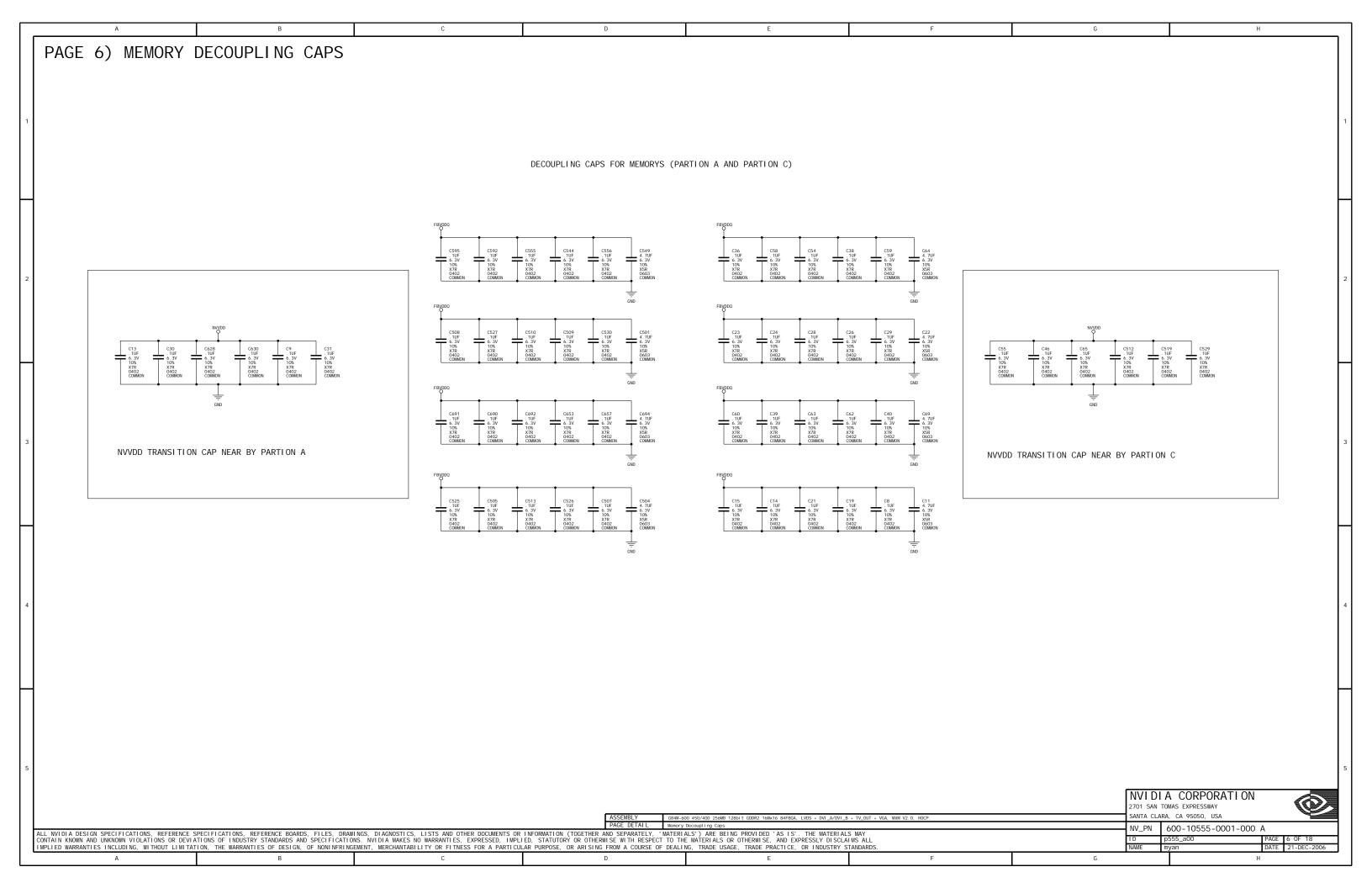
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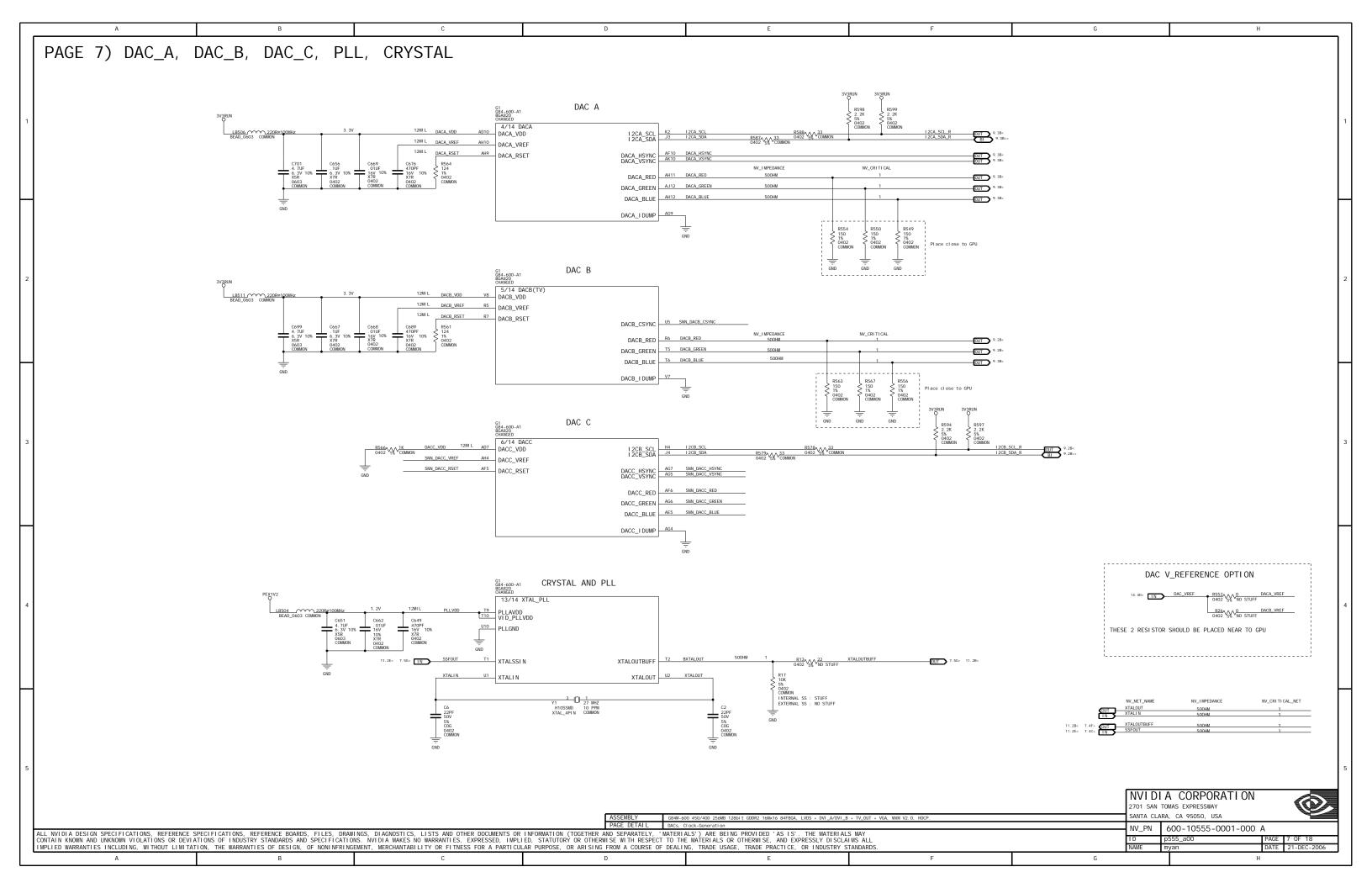


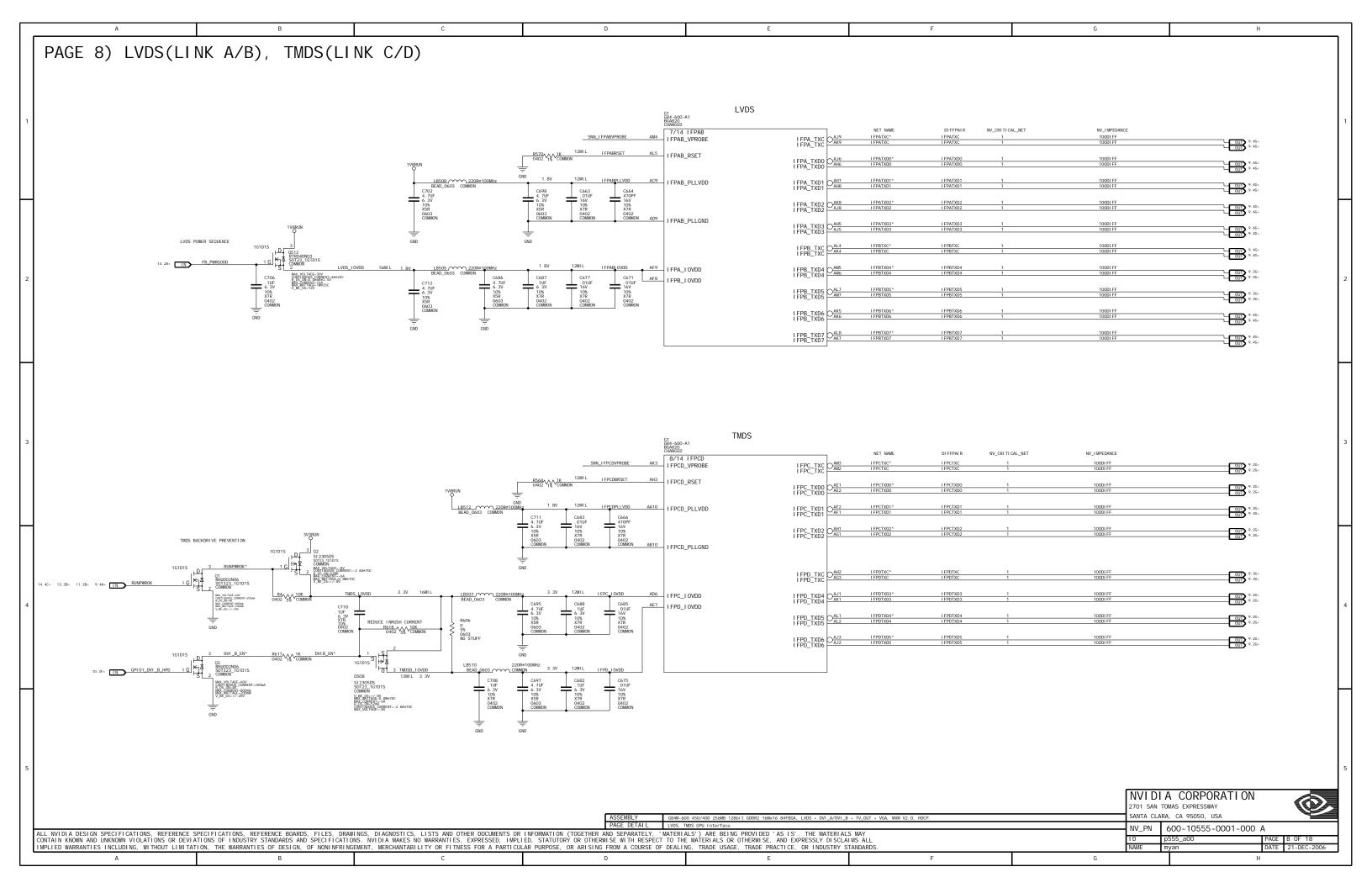


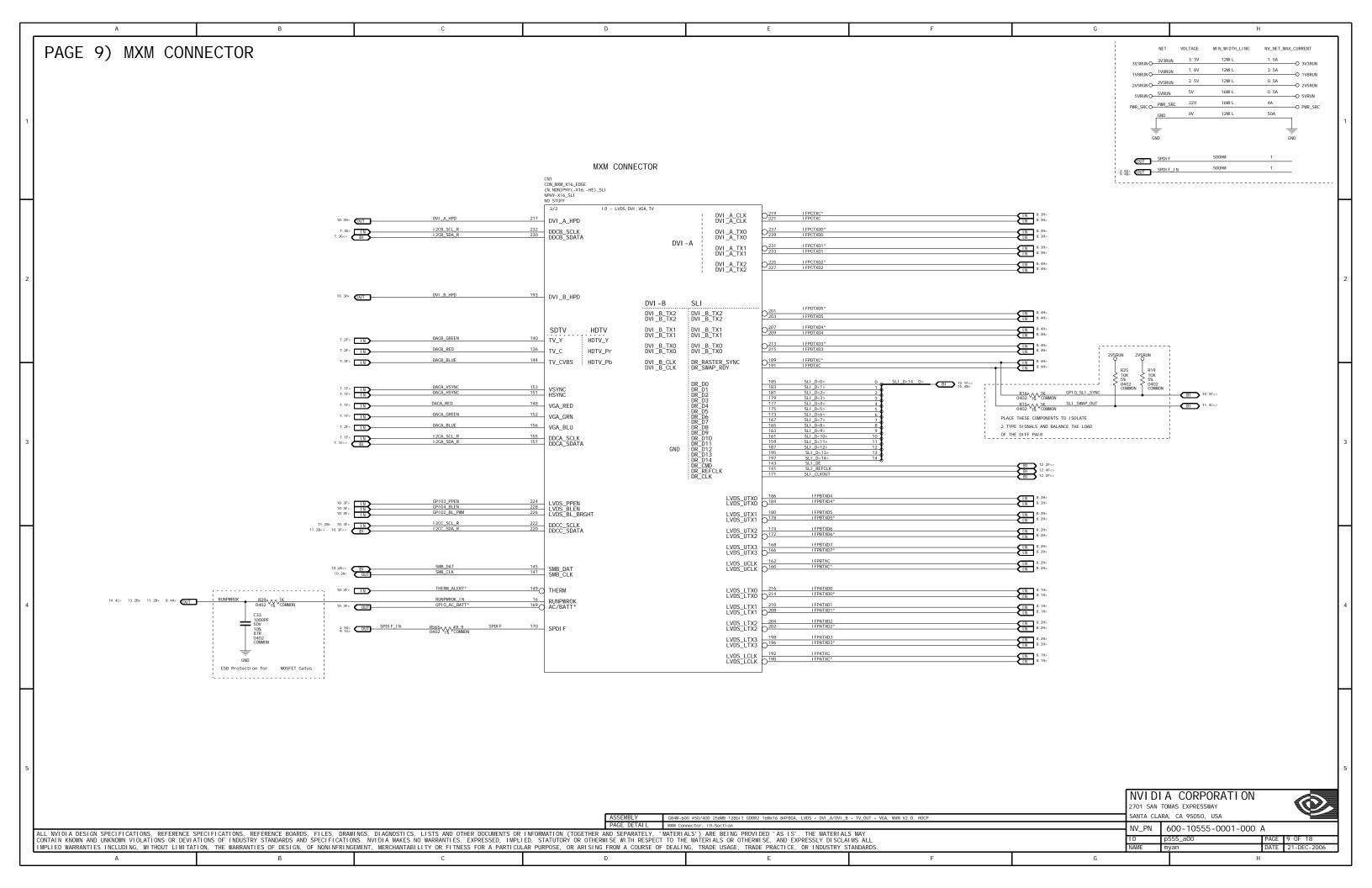


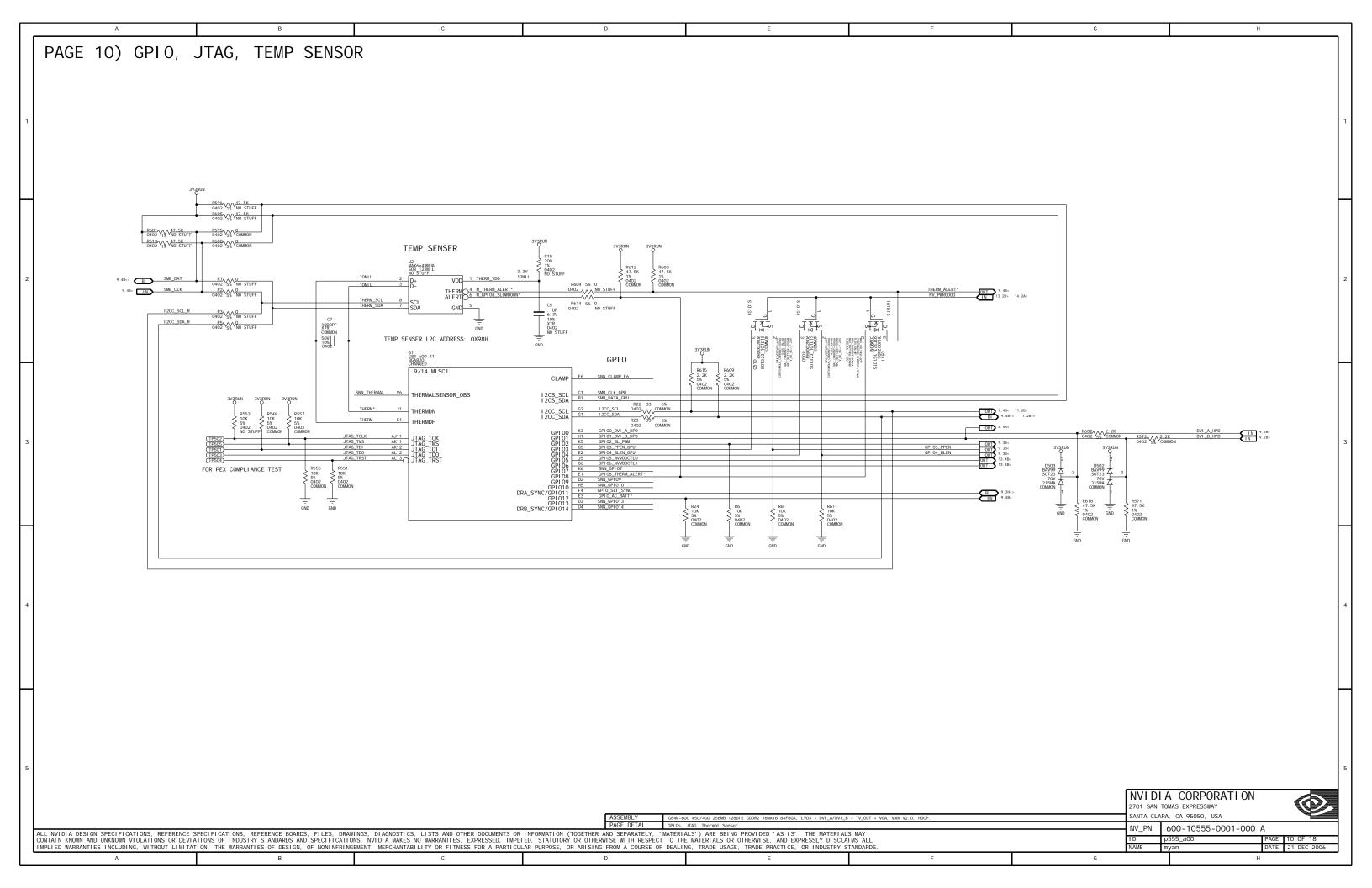


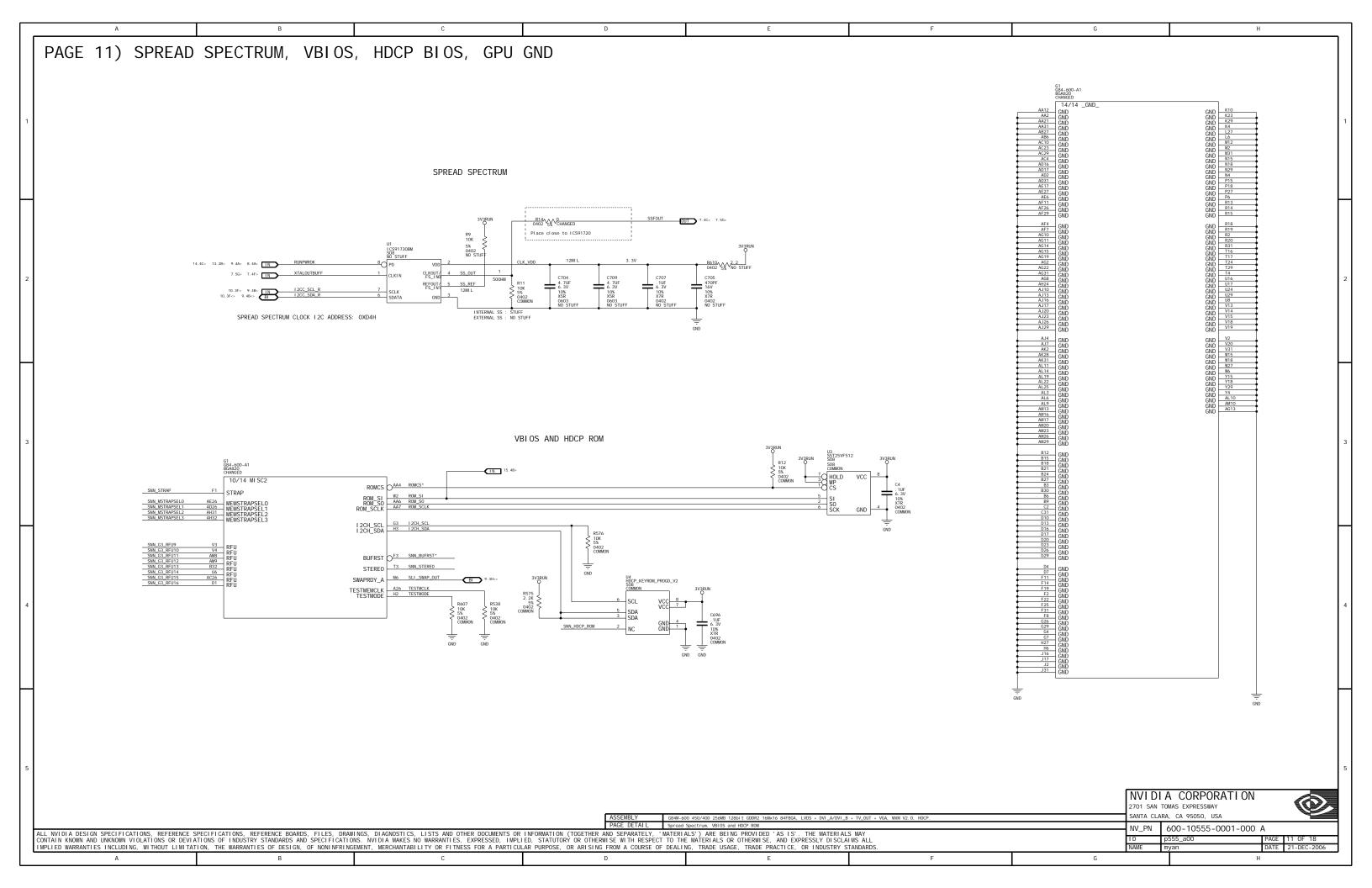


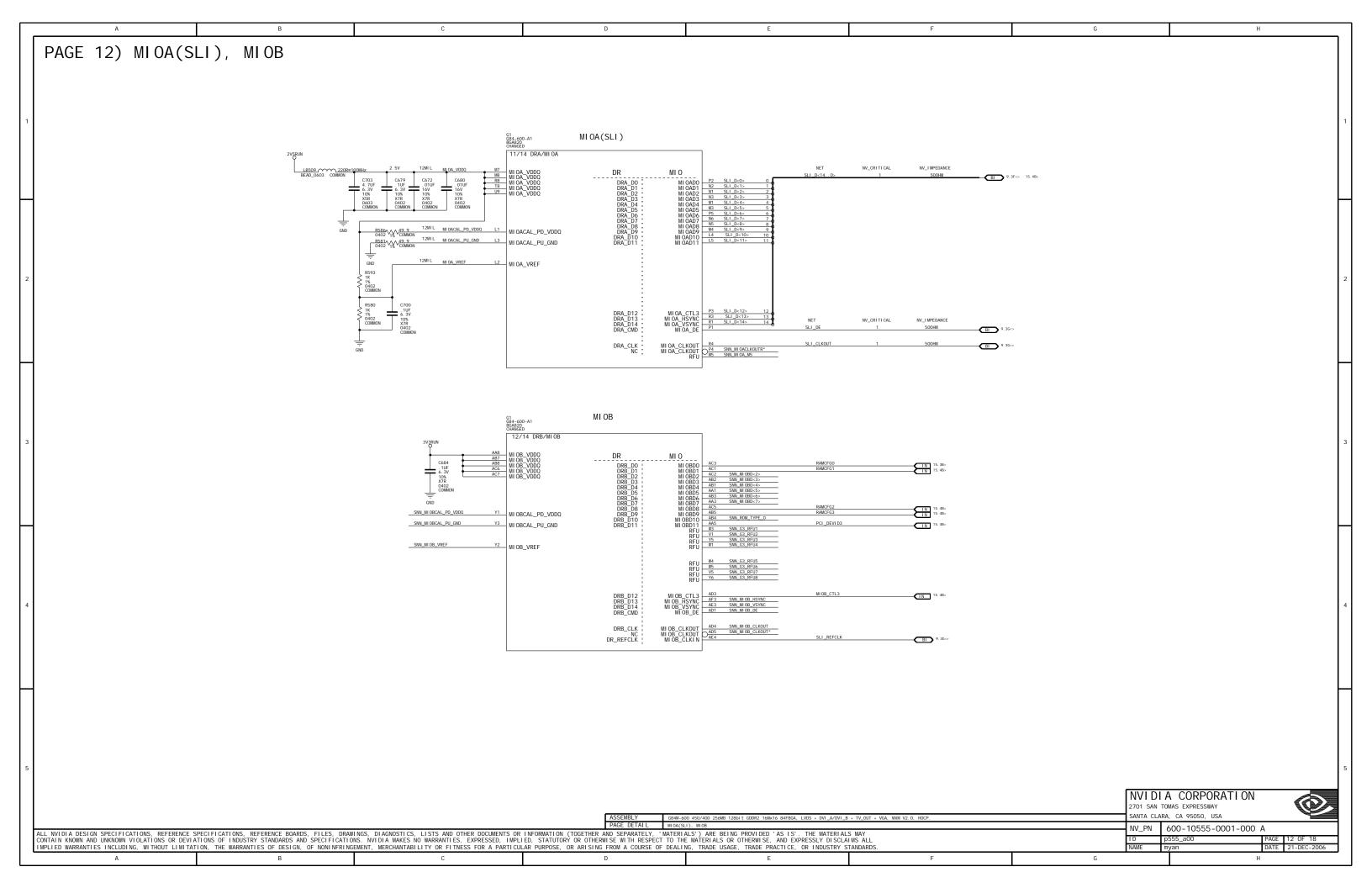


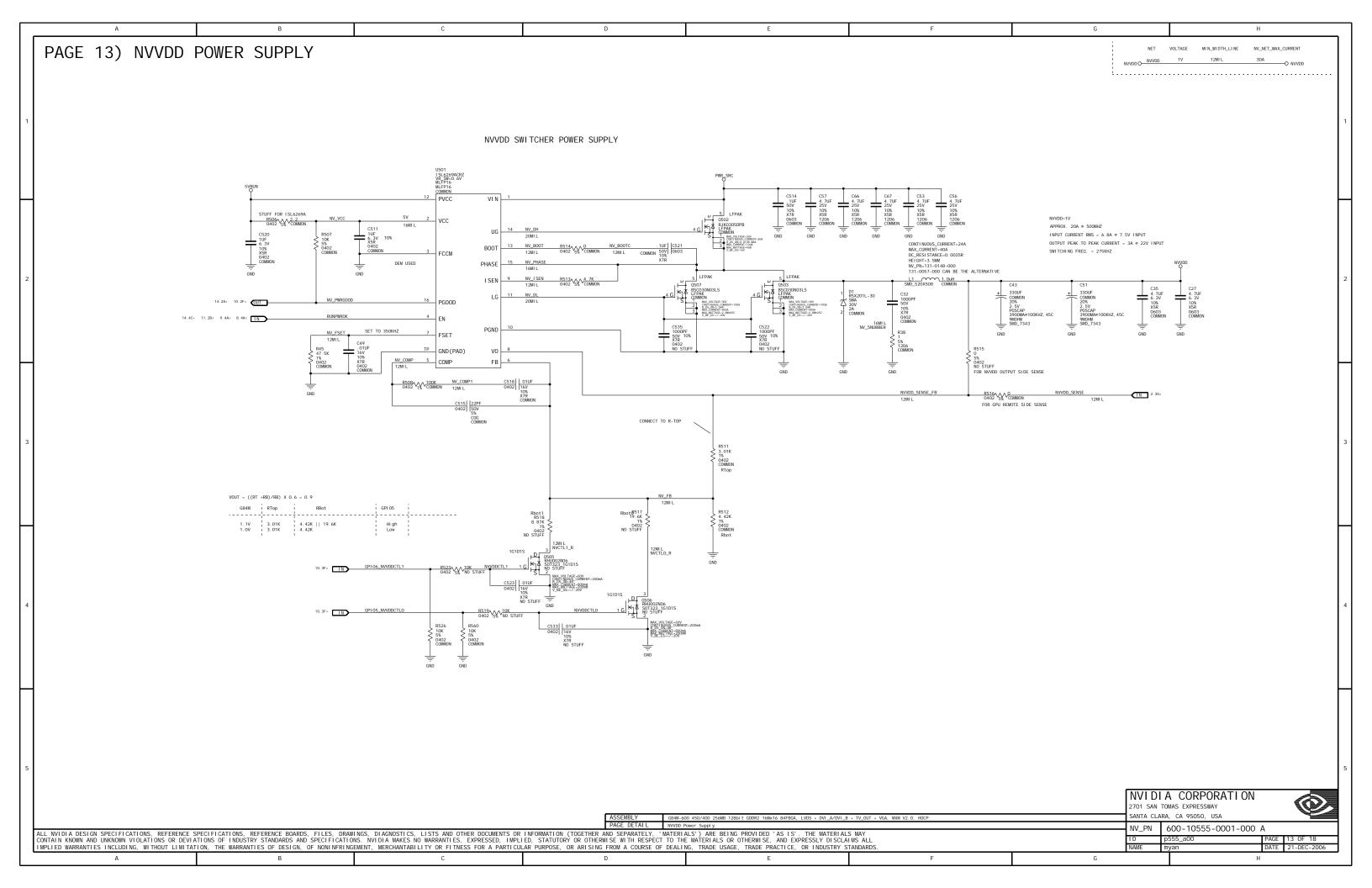


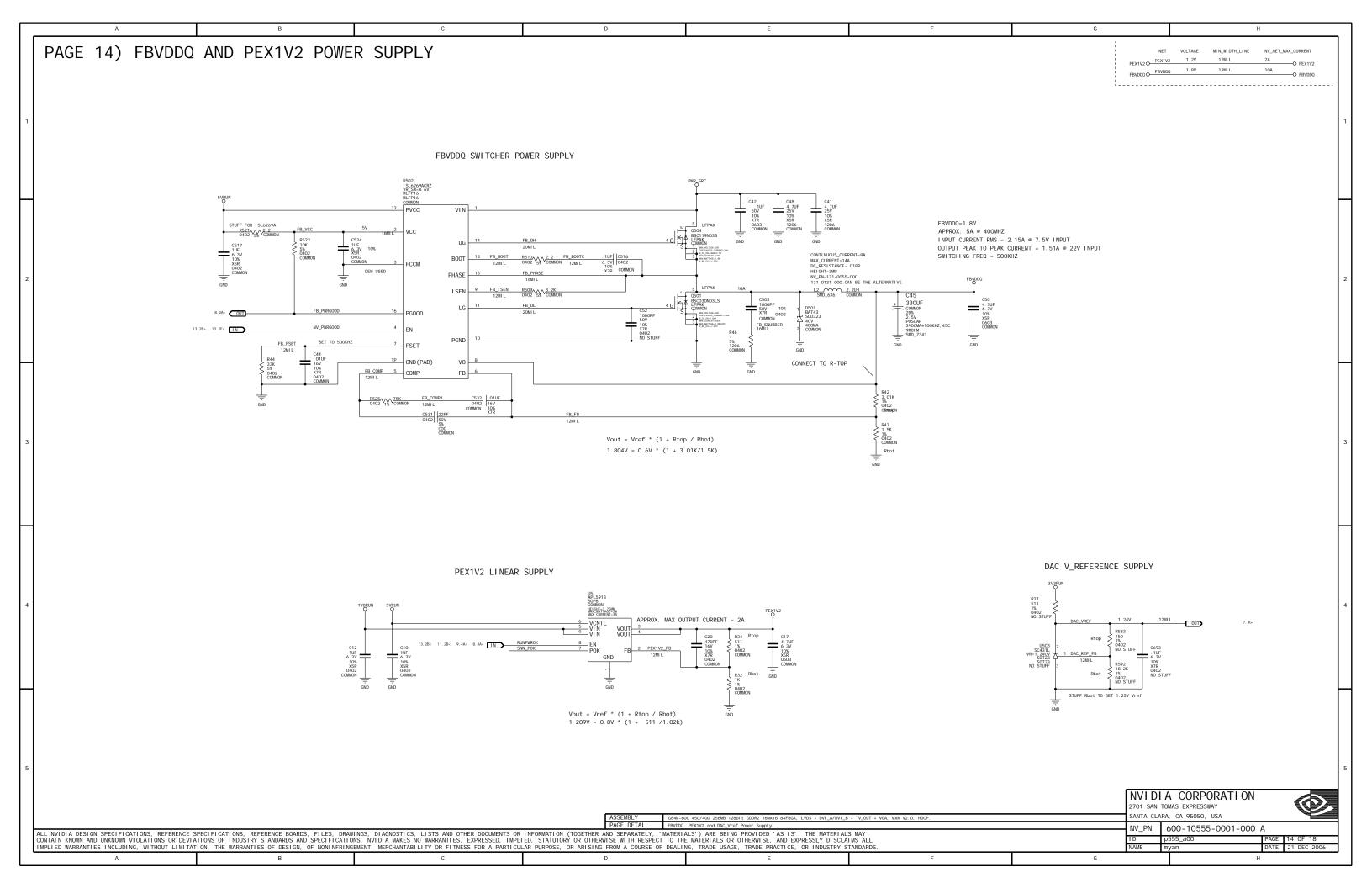


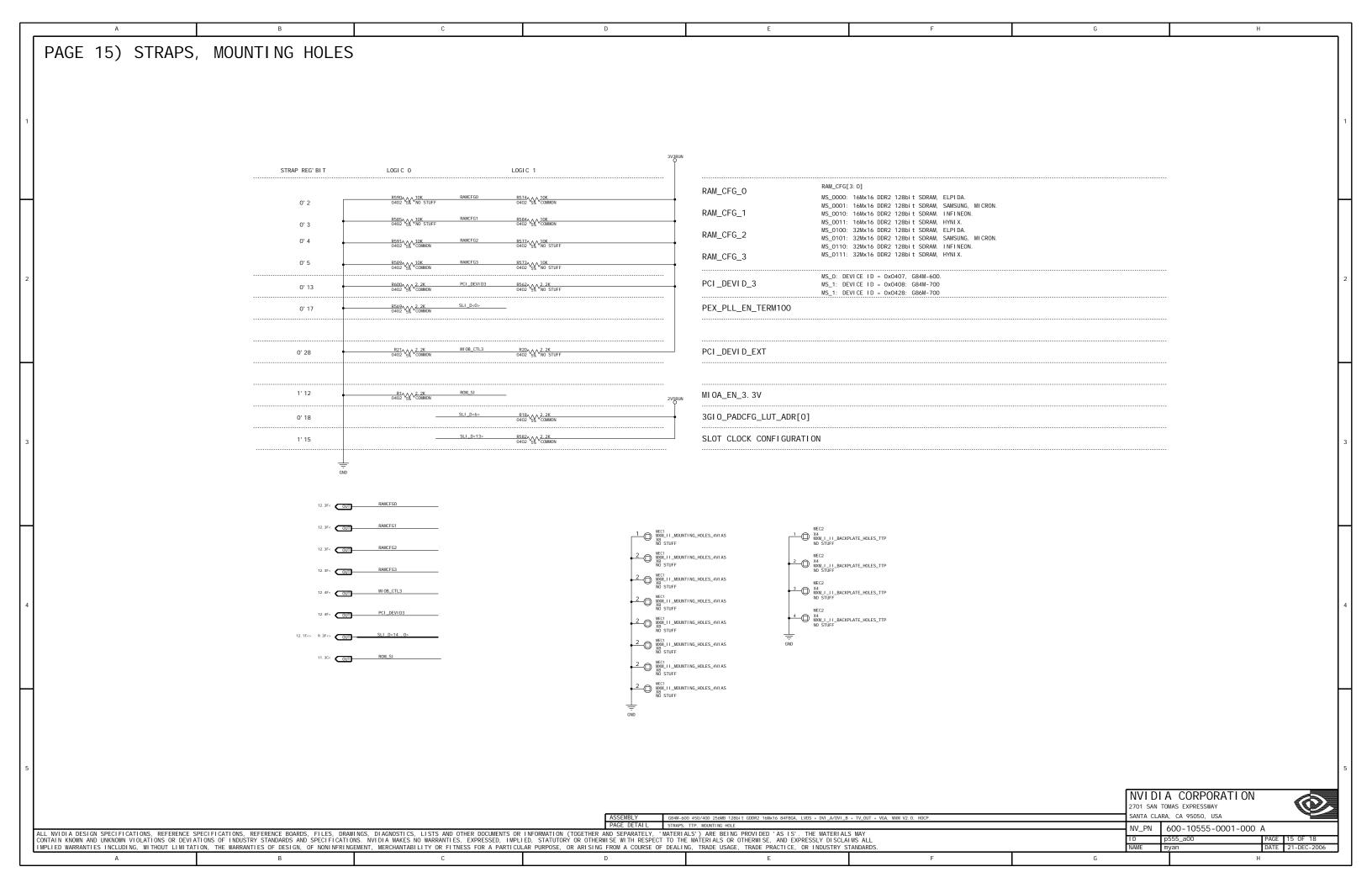












A	D.	6	D	F		
	В	С	D	Ł	F	G H
itle: Basenet Report	FBAD<59> 3. 3A 4. 5D	FBCAL_TERM 3.5G	FBC_A<2> 3.3G 5.1A 5.1C		PEX_RX3* 2. 3E	RAMCFG3 12. 3F< 15. 2C 15. 4B>
esi gn: p555_a00	FBAD<60> 3. 3A 4. 5D	FBCD<0> 3. 3G FBCD<0> 3. 1E 5. 4B	FBC_A<2> 3. 3G 5. 1A 5. 1C FBC_A<3> 3. 3G 5. 1A 5. 1C	12CC_SDA	PEX_RX3 2.3E PEX_RX4 2.3E	ROMCS* 12. 3F< 15. 2C 15. 46>
ate: Nov 30 11:00:17 2006	FBAD<61> 3. 3A 4. 5D FBAD<62> 3. 3A 4. 5D	FBCD<630> 3.1E<> 5.4A<> 5.5F<> FBCD<1> 3.1E 5.4B	FBC_A<4> 3.3G 5.1A 5.1C FBC_A<5> 3.3G 5.1A 5.1C	I 2CC_SDA_R 9. 4B<> 10. 3F<> 11. 2B<>	PEX_RX4* 2. 3E	ROM_SCLK 11. 3C ROM_SI 11. 3C< 15. 3C 15. 4B>
se nets and synonyms for	FBAD<62> 3. 3A 4. 5D FBAD<63> 3. 3A 4. 5D	FBCD<1> 3. 1E 5. 4B FBCD<2> 3. 1E 5. 4B	FBC_A<5> 3. 3G 5. 1A 5. 1C FBC_A<6> 3. 3G 5. 1A 5. 1C 5. 1E	11. 2B<> 12CH_SCL 11. 4C	PEX_RX5 2. 3E PEX_RX5* 2. 3E	ROM_SI 11. 3C< 15. 3C 15. 4B> ROM_SO 11. 3C
07_l i b. P555_A00(@p407_l i b. p555_a00(sch	FBADQM<0> 3.3A 4.4B	FBCD<3> 3. 1E 5. 4B	5. 1G	I 2CH_SDA 11. 4C	PEX_RX6 2. 3E	RUNPWROK 8. 4A< 9. 4A> 11. 2B<
)) se Signal Location([Zone][dir])	FBADOM<70> 3.3A> 4.4A< 4.5F< FBADOM<1> 3.3A 4.4C	FBCD<4> 3. 1E 5. 4B FBCD<5> 3. 1E 5. 4B	FBC_A<7> 3.3G 5.1A 5.1C 5.1E 5.1G	I FPABI OVDD	PEX_RX6* 2. 3E PEX_RX7 2. 3E	13. 2B< 14. 4C<  RUNPWROK* 8. 4B
	FBADQM<2> 3.3A 4.4D	FBCD<6> 3. 1E 5. 4B	FBC_A<8> 3. 3G 5. 1A 5. 1C 5. 1E	I FPABRSET 8. 1D	PEX_RX7* 2. 3E	RUNPWROK_I N 9. 4C
9RUN 9. 1G 5RUN 9. 1G	FBADOM<3> 3. 3A 4. 4D FBADOM<4> 3. 3A 4. 5B	FBCD<7> 3. 1E 5. 4B FBCD<8> 3. 1E 5. 4C	5. 1G FBC_A<9> 3. 3G 5. 1A 5. 1C 5. 1E	I FPATXC	PEX_RX8 2. 4E PEX_RX8* 2. 4E	SLI_CLKOUT 9. 3G<> 12. 2F<> SLI_D<0> 9. 3E 12. 1E
BRUN 9. 1G	FBADQM<5> 3. 3A 4.5C	FBCD<9> 3.1E 5.4C	5. 1G	I FPATXDO 8. 1H> 9. 4G<	PEX_RX9 2. 4E	SLI_D<140> 9.3F<> 12.1F<> 15.4B>
RUN 9. 1G FALOUT 7. 4D	FBADOM<6> 3. 3A 4. 5D FBADOM<7> 3. 3A 4. 5D	FBCD<10> 3. 1E 5. 4C FBCD<11> 3. 1E 5. 4C	FBC_A<10> 3. 3G 5. 1A 5. 1C 5. 1E 5. 1G	I FPATXDO*	PEX_RX9* 2. 4E PEX_RX10 2. 4E	SLI_D<1> 9. 3E 12. 1E SLI_D<2> 9. 3E 12. 1E
C_VDD 11. 2C	FBADQSO 3. 3A<> 4. 4B 4. 4F<>	FBCD<12> 3. 1E 5. 4C	FBC_A<11> 3. 3G 5. 1A 5. 1C 5. 1E	I FPATXD1* 8. 1H> 9. 4G<	PEX_RX10* 2.4E	SLI_D<3> 9. 3E 12. 1E
A_BLUE 7. 2F> 9. 3B< A_GREEN 7. 1F> 9. 3B<	FBADOSO* 3. 4A<> 4. 4B 4. 4F<> FBADOS1 3. 4A<> 4. 4C 4. 4F<>	FBCD<13> 3. 1E 5. 4C FBCD<14> 3. 1E 5. 4C	5. 1G FBC_A<12> 3. 3G 5. 2A 5. 2C 5. 2E	I FPATXD2	PEX_RX11 2. 4E PEX_RX11* 2. 4E	SLI_D<4> 9. 3E 12. 2E SLI_D<5> 9. 3E 12. 2E
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A_VDD 7.1C	FBADQS3 3. 4A<> 4. 4D 4. 4F<>	FBCD<18> 3. 2E 5. 4D	FBC_BA1 3. 3H> 5. 2A< 5. 2C 5. 2E	I FPBTXC* 8. 2H> 9. 4G<	PEX_RX13* 2. 5E	SLI_D<9> 9. 3E 12. 2E
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B_RED 7. 2F> 9. 2B< B_RSET 7. 2C	FBADQS5* 3. 4A<> 4. 4F<> 4. 5C FBADQS6 3. 4A<> 4. 4F<> 4. 5D	FBCD<23> 3. 2E 5. 4D FBCD<24> 3. 2E 5. 4D	5. 1G 5. 5F< FBC_CKE 3. 3H> 5. 2A< 5. 2C 5. 2E	I FPBTXD6	PEX_TSTCLK 2. 2E PEX_TSTCLK* 2. 2E	SLI_D<14> 9. 3E 12. 2E SLI_DE 9. 3G<> 12. 2F<>
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B_VREF 7. 2C 7. 4H C_VDD 7. 3C	FBADOS7 3. 4A<> 4. 4F<> 4. 5D FBADOS7* 3. 4A<> 4. 4F<> 4. 5D	FBCD<26> 3. 2E 5. 4D FBCD<27> 3. 2E 5. 4D	FBC_CLKO 3. 4H> 5. 2A 5. 2C 5. 3A< 5. 3F<	I FPBTXD7*	PEX_TXO* 2. 2E PEX_TXO_C 2. 2B	SLI_SWAP_OUT 9. 3H<> 11. 4C<> SMB_CLK 9. 4B> 10. 2A<
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_B_HPD 9. 2B> 10. 3H< 0<0> 3. 1A 4. 4B	FBA_A<2> 3. 3C 4. 1A 4. 1C FBA_A<3> 3. 3C 4. 1A 4. 1C	FBCD<33> 3. 2E 5. 5B FBCD<34> 3. 2E 5. 5B	FBC_CLK1* 3. 4H> 5. 2E 5. 2G 5. 3E< 5. 4F<	I FPCTXD1	PEX_TX2 2. 2E PEX_TX2* 2. 2E	SNN_A2_M3
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3.1A 4.4B	FBA_A<7> 3. 3C 4. 1A 4. 1C 4. 1E	FBCD<39> 3. 2E 5. 5B	FBC_ODT 3. 5D> 5. 2A< 5. 2C 5. 2E	I FPDTXC*	PEX_TX3_C 2. 3B	SNN_BUFRST* 11.4C
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3. 2A 4. 5B 3. 2A 4. 5B 3. 2A 4. 5B	4. 4F<	FBCDOM<4> 3.3E 5.5B FBCDOM<5> 3.3E 5.5C	FB_SNUBBER 14. 2E	NV_COMP 13. 2C	PEX_TX11 2. 4E	SNN_FBVTT_H17
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3. 2A 4. 5C 3. 2A 4. 5C 3. 2A 4. 5C	FBA_DDT_GPU 3. 1G> 3. 4C 3. 5C FBA_PLLAVDD_GPU 3. 4C	FBCDQS1* 3. 4E<> 5. 4C 5. 4F<> FBCDQS2 3. 4E<> 5. 4D 5. 4F<>	GPI 03_PPEN 9. 3B< 10. 3F> GPI 03_PPEN_GPU 10. 3D	NV_PHASE 13. 2C NV_PWRGOOD 10. 2F< 13. 2B> 14. 2A<	PEX_TX12_C* 2. 4B PEX_TX13 2. 5E	SNN_FBVTT_K12 3.1G SNN_FBVTT_K21 3.1G
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44> 3. 2A 4. 5C 45> 3. 2A 4. 5C	4. 1G 4. 4F< FBA_RESET 3. 1G> 3. 3C 3. 5C	FBCDOS3 3. 4E<> 5. 4D 5. 4F<> FBCDOS3* 3. 4E<> 5. 4D 5. 4F<>	GPI 04_BLEN_GPU 10. 3D GPI 05_NVVDDCTLO 10. 3F> 13. 4B<	NV_VCC 13. 2B PCI_DEVI D3 12. 4F< 15. 2C 15. 4B>	PEX_TX13_C 2.5B PEX_TX13_C* 2.5B	SNN_FBVTT_K24 3. 1G SNN_FBVTT_L23 3. 1G
3. 2A 4. 5C 46> 3. 2A 4. 5C	FBA_RESET 3. 1G> 3. 3C 3. 5C FBA_VREF1 4. 2B 4. 3F<	FBCDQS4 3. 4E<> 5. 4D 5. 4F<> FBCDQS4 3. 4E<> 5. 4F<> 5. 5B	GPI 05_NVVDDCTL0 10. 3F> 13. 4B< GPI 06_NVVDDCTL1 10. 3F> 13. 4B<	PCI_DEVI D3 12. 4F< 15. 2C 15. 4B> PEX1V2 14. 1G	PEX_IX13_C* 2.5B PEX_TX14 2.5E	SNN_FBVTT_M23 3. 1G SNN_FBVTT_M23 3. 1G
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3. 3M 4. 3U	FBCAL_PU 3. 4G	5. 16	12CC_SCL 10. 3D	PEX_RX3 2. 3E	RAMCFG2 12. 3F< 15. 2C 15. 4B>	SNN_G3_RFU10 11. 4A
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				B 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_0	DUT + VGA, MXM V2.O, HDCP.	SANTA CLARA, CA 95050, USA
NIA DESIGN SDECIEICATIONS DEFENDAS SOCOET	CATIONS DEEDENCE DOADNS ELLES DRAWLAGS ST	ACMOSTICS LISTS AND OTHER DOCUMENTS OF INFORMATION	PAGE DETAIL <edit here="" insert<="" td="" to=""><td>page detail&gt;</td><td>DUT + VGA, MXM V2.0, HDCP.</td><td>NV_PN 600-10555-0001-000 A</td></edit>	page detail>	DUT + VGA, MXM V2.0, HDCP.	NV_PN 600-10555-0001-000 A
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G	INVI DI A
F	
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