

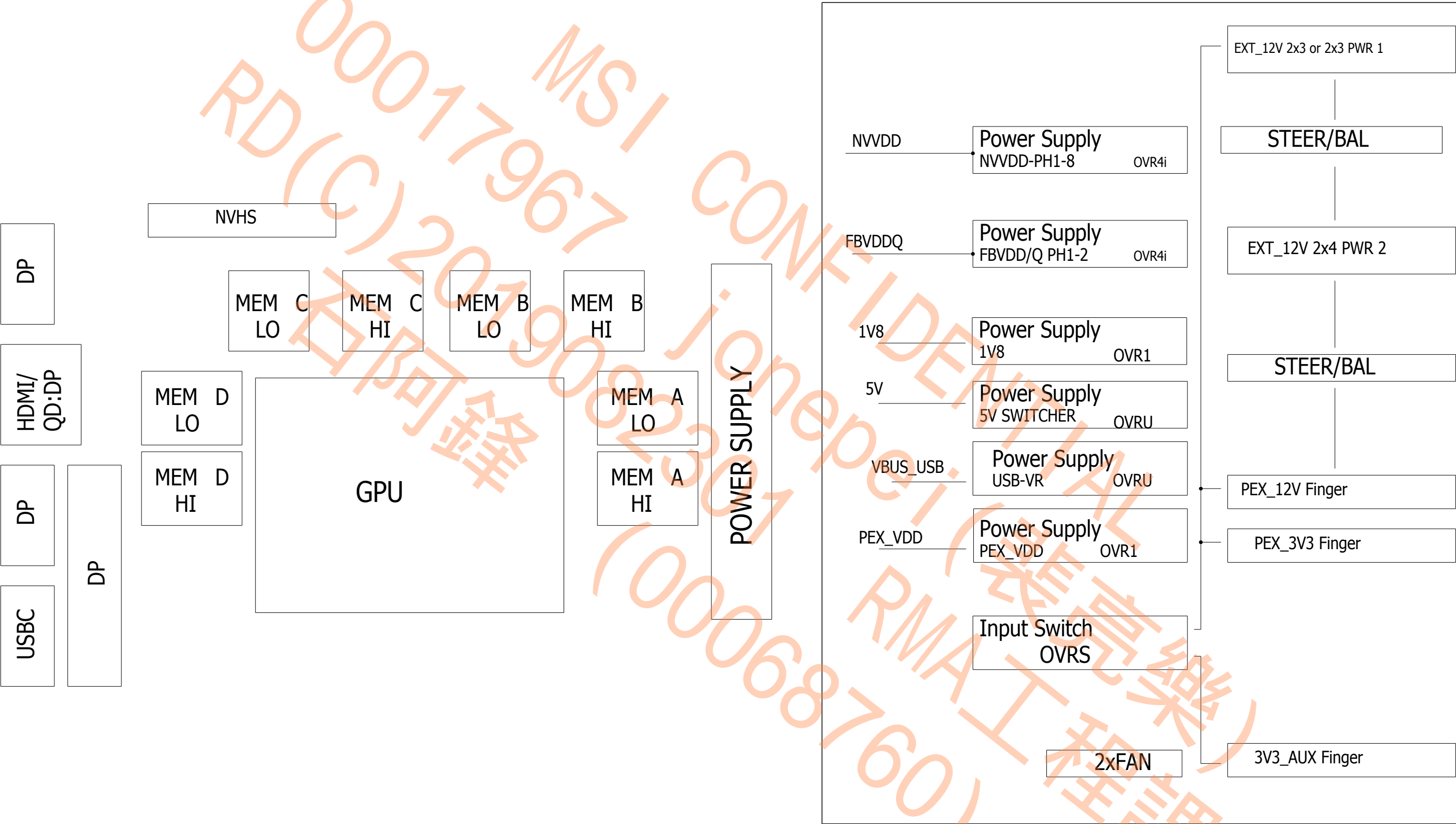
PG180-A03

256b GDDR6 x16  
TALL DP + DP + DP + HDMI/DP + USB

TABLE OF CONTENTS

Page	Description	Page	Description	Page	Description
1	Table of Contents	26	MISC: XTAL, PLL	51	SEQUENCE: MISC
2	Block Diagram	27	MISC: USB PPC	52	LED & FAN HEADERS
3	PCI Express	28	PS: USB VR	53	LED 2
4	PCI Termination	29	PS: 5V, 5V BACKUP	54	Mechanical: Bracket/Thermal Solution
5	MEMORY: GPU Partition A/B	30	PS: PEXVDD, 1V8		
6	MEMORY: FBA Partition 31..0	31	PS: FBVDD CONTROLLER		
7	MEMORY: FBA Partition 63..32	32	PS: FBVDD CONTROLLER OVR3		
8	MEMORY: FBB Partition 31..0	33	PS: FBVDD PHASE 1, 2		
9	MEMORY: FBB Partition 63..32	34	PS: NVVDD CONTROLLER OVR8		
10	MEMORY: GPU Partition C/D	35	PS: NVVDD Phase 1, 2		
11	MEMORY: FBC Partition 31..0	36	PS: NVVDD Phase 3, 4		
12	MEMORY: FBC Partition 63..32	37	PS: NVVDD Phase 5, 6		
13	MEMORY: FBD Partition 31..0	38	PS: NVVDD Phase 7, 8		
14	MEMORY: FBD Partition 63..32	39	PS: INPUT SWITCH RTD3		
15	GPU PWR and GND	40	PS: INPUT SWITCH RTD3 USB		
16	GPU Decoupling	41	PS: INPUT SWITCH RAIL BALANCE		
17	GPU DECOUPLING	42	PS: 12V CURRENT STEERING		
18	IFPAB TALL-DP	43	PS: VR THERMAL PROTECTION		
19	IFPE DP	44	PS: INPUTS, FILTERING AND MONITORING		
20	IFPF USBC	45	PS: CURRENT STEERING,HOT UNPLUG DETECT		
21	IFPC HDMI 2.0/DP	46	PS: PRE-FILTER		
22	IFPD DP	47	SEQUENCE: 5V, 1V8, NV3V3 ENABLE		
23	NVHS INTERFACE	48	SEQUENCE: NV, PEX, FB ENABLE		
24	MISC: FAN,THERMAL,JTAG,GPIO,STEREO	49	SEQUENCE: PCIE VOLTAGE MONITOR		
25	MISC3: ROM, STRAPS	50	SEQUENCE: DISCHARGE		

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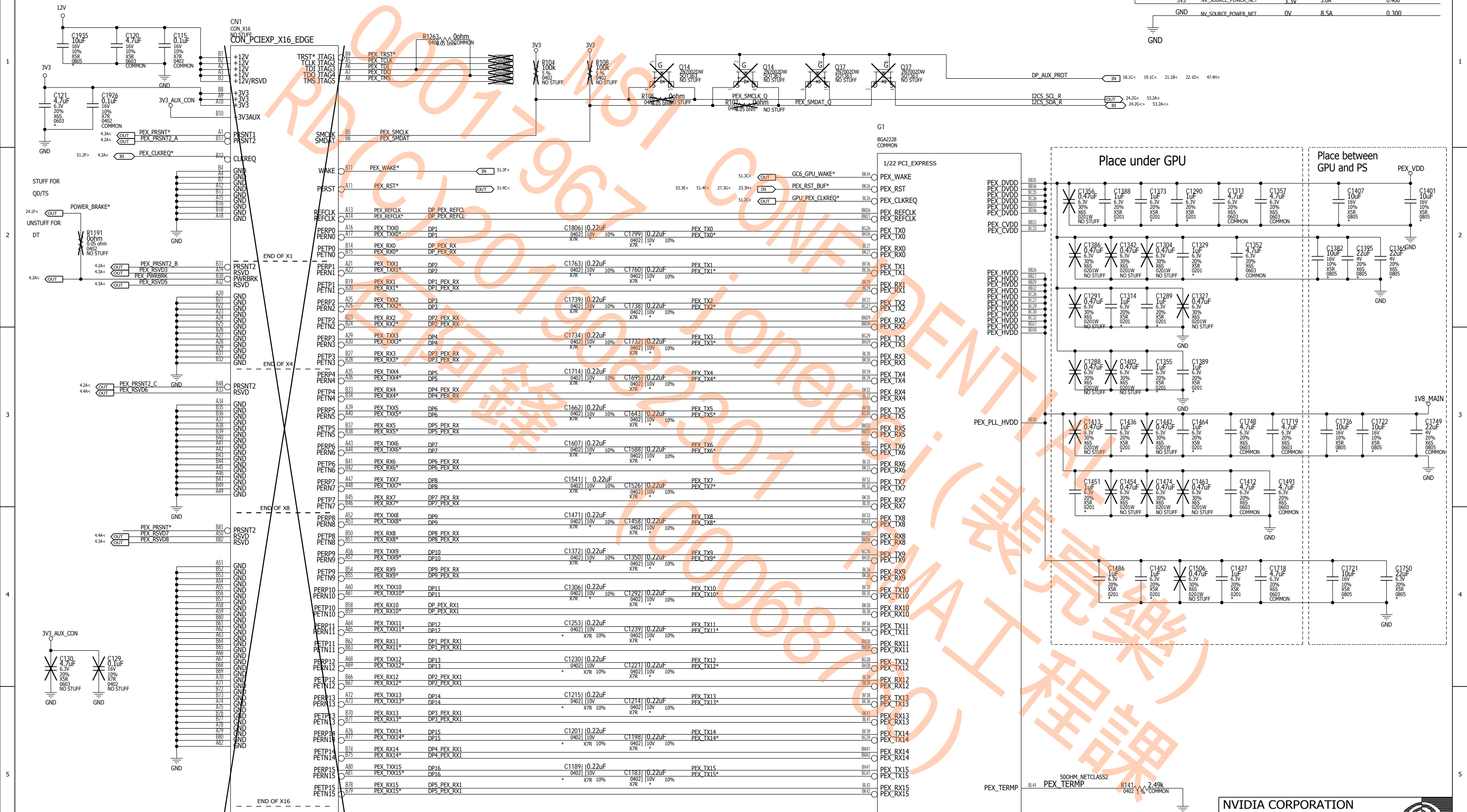


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PAGE DETAIL	Block Diagram

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NV_PN	600-1G180-0003-QS2	PAGE	2 OF 54
PCB REV	PG180-A03	DATE	06-FEB-2019
BOM REV	A		

## Page3: PCI Express



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PAGE DETAIL	PCI Express

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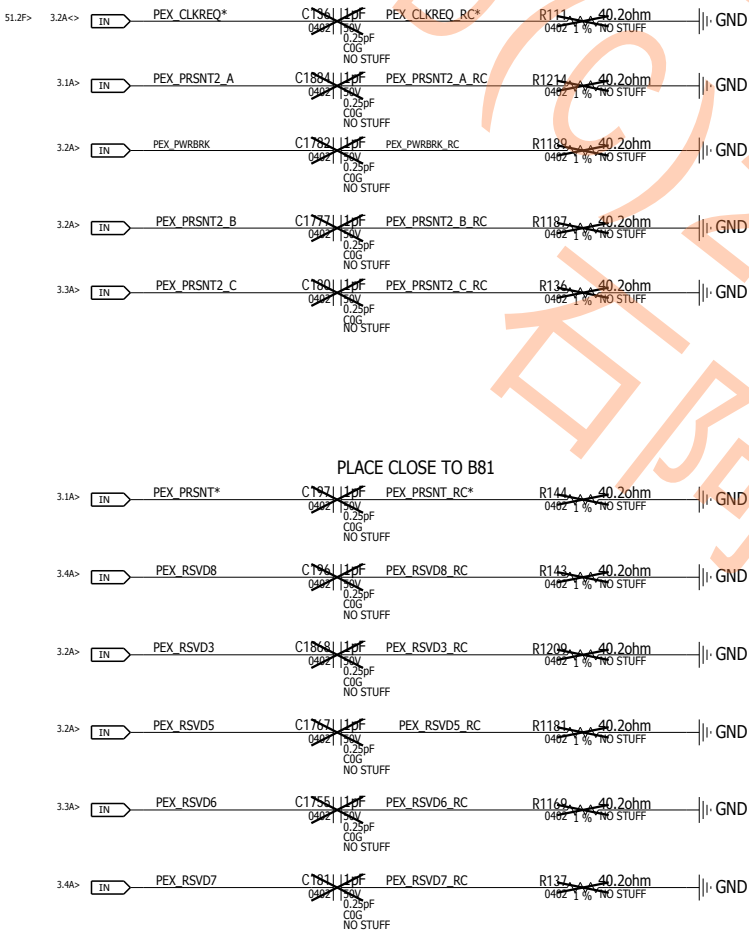
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PCB REV	PG180-A03
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PAGE	3 OF 54
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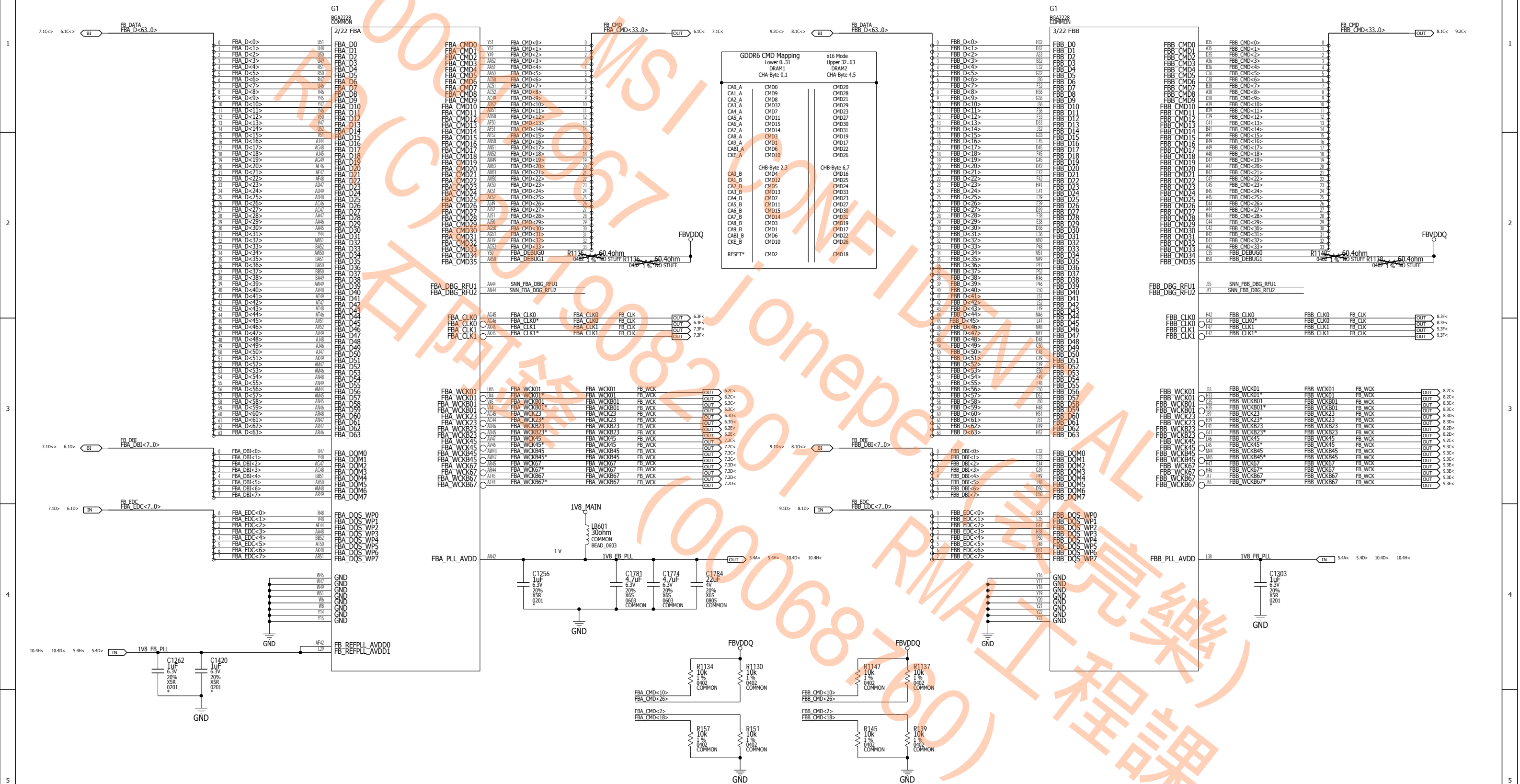


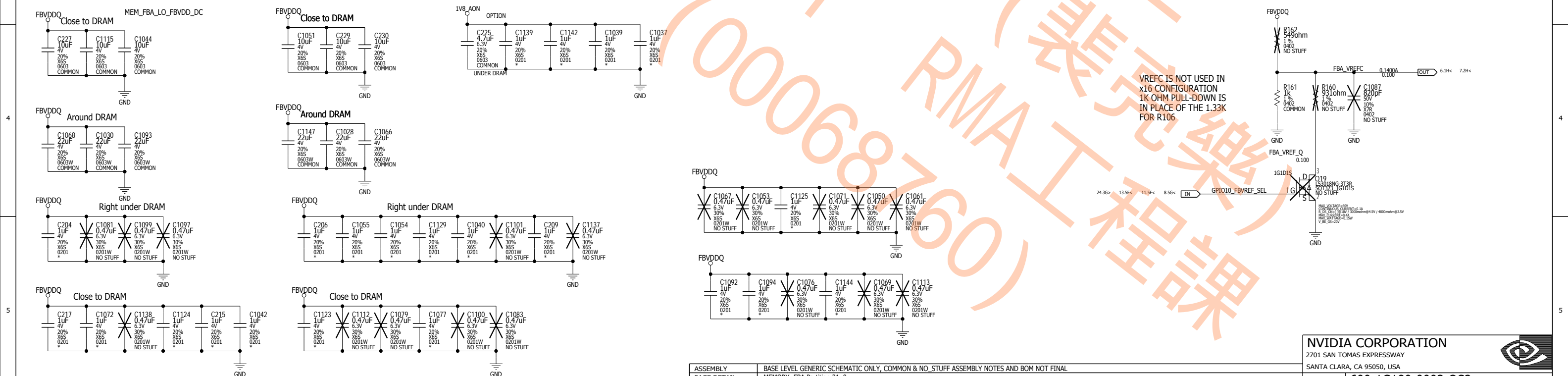
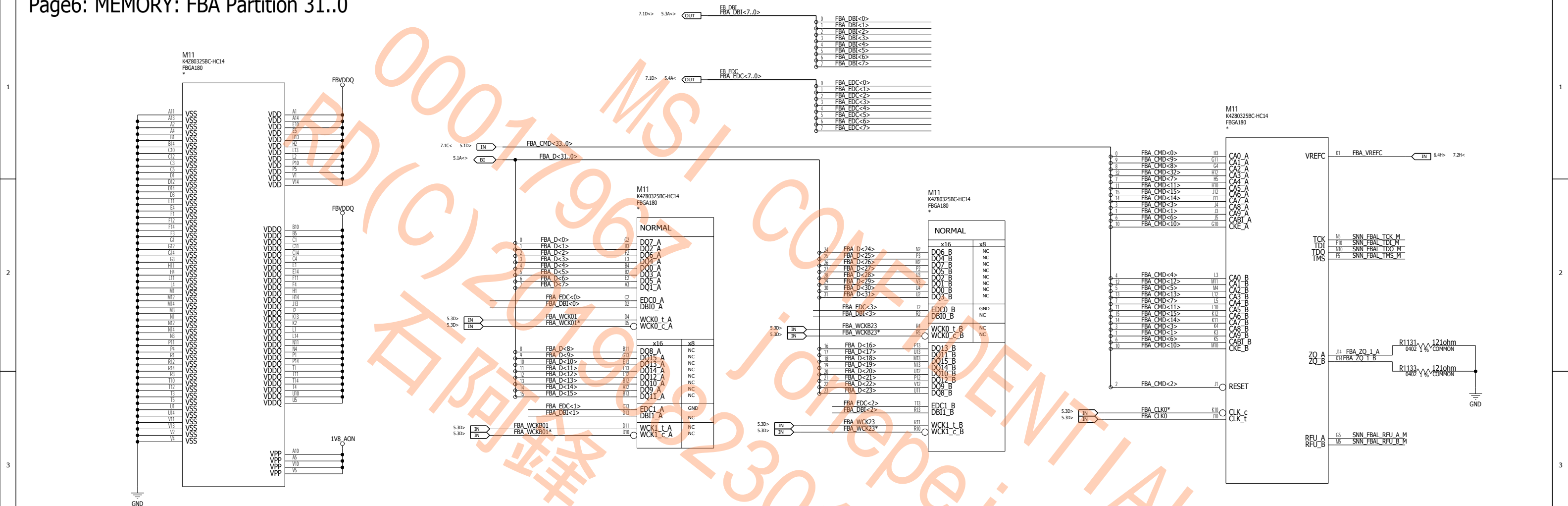
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PCB REV	PG180-A03	PAGE	4 OF 54
BOM REV	A	DATE	06-FEB-2019

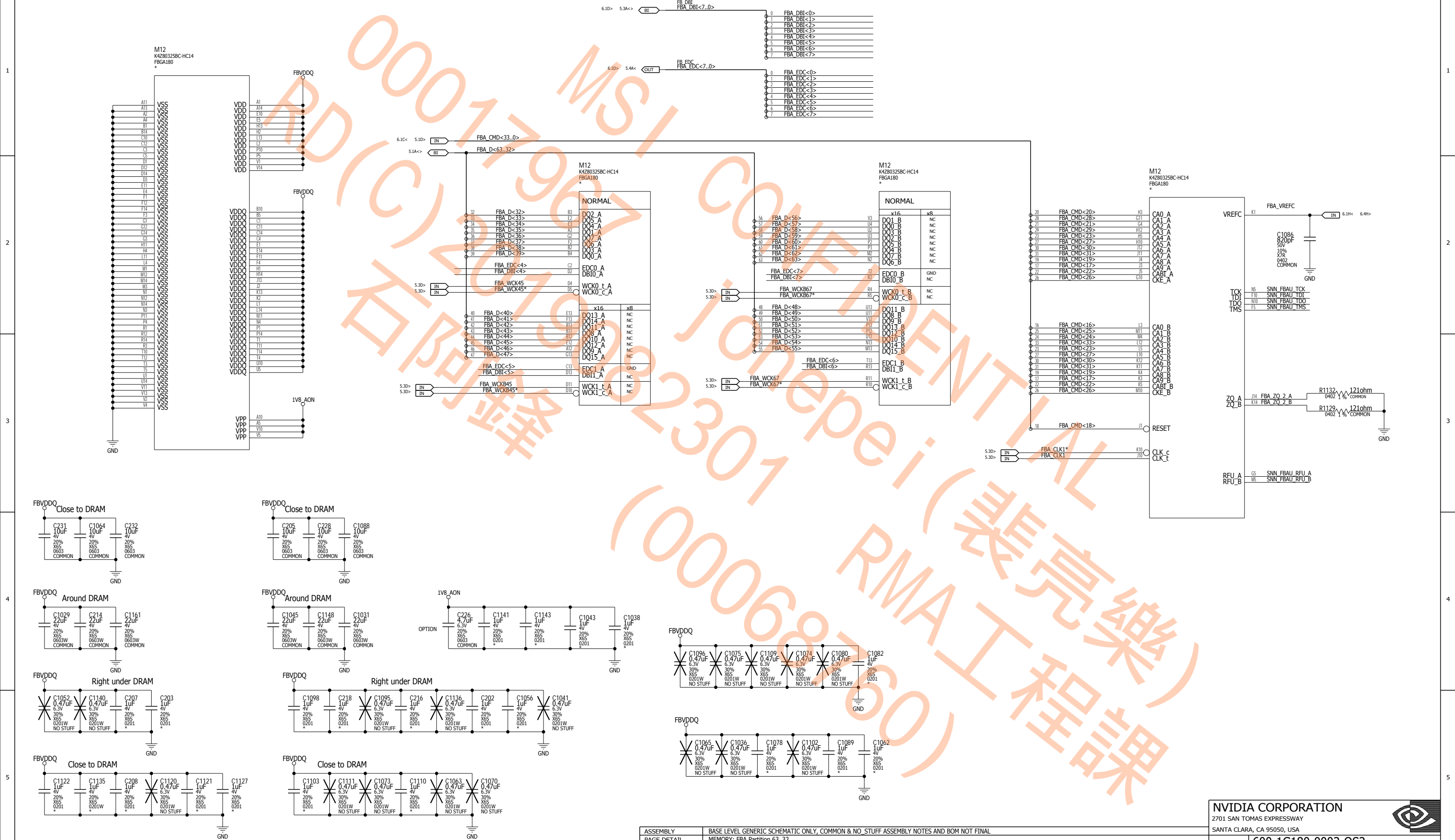


## Page5: MEMORY: GPU Partition A/B

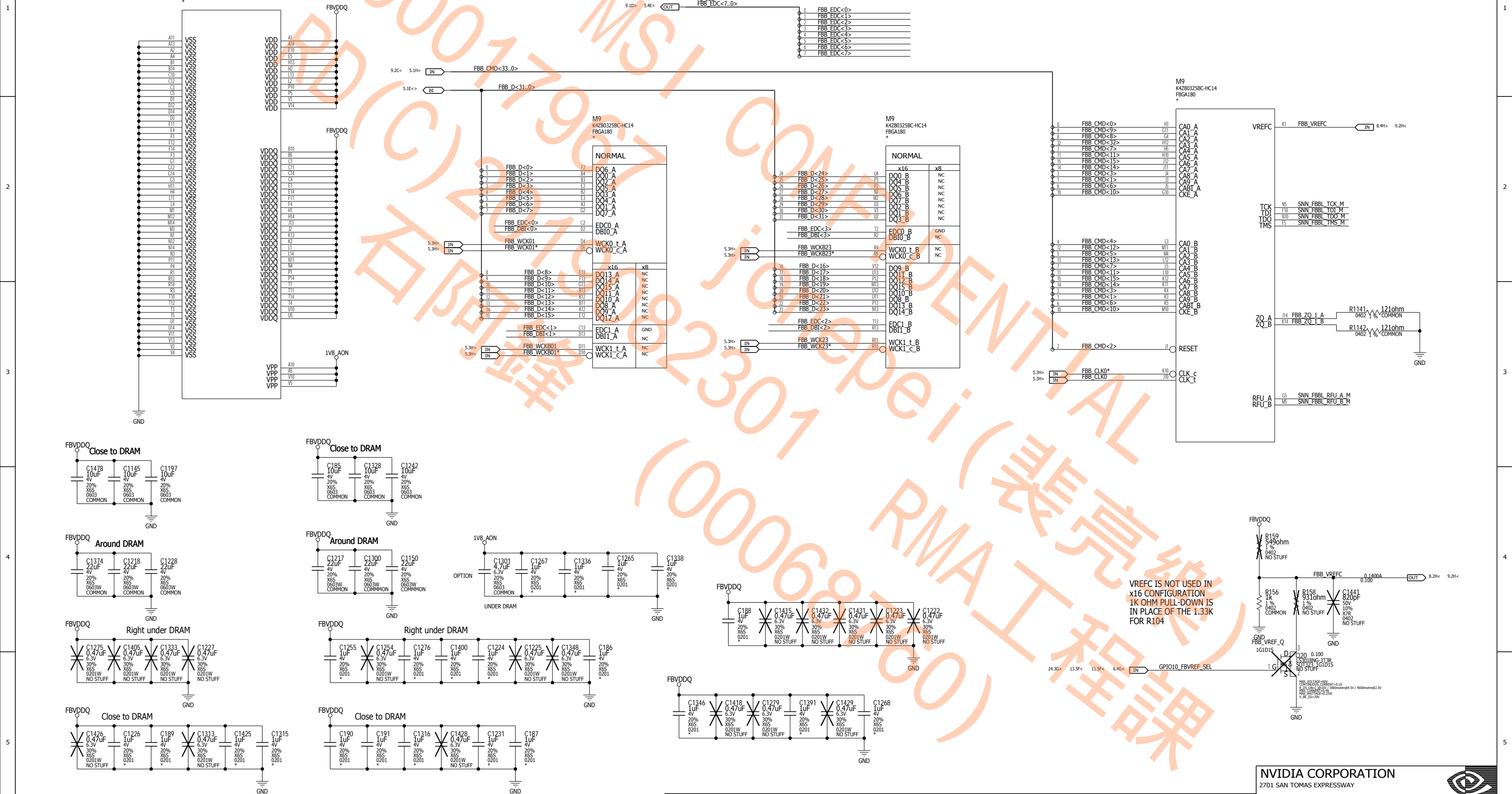




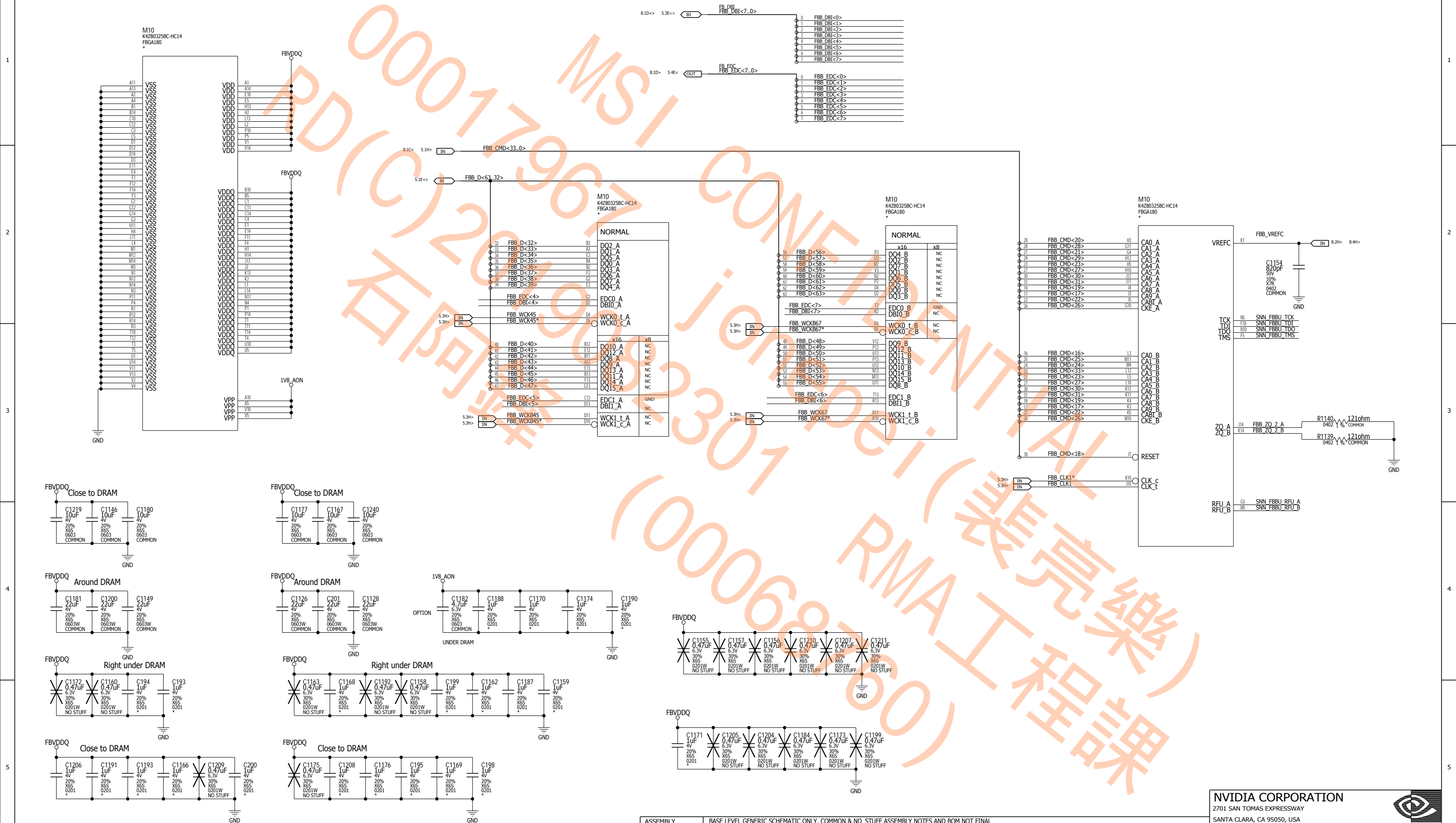
Page7: MEMORY: FBA Partition 63..32



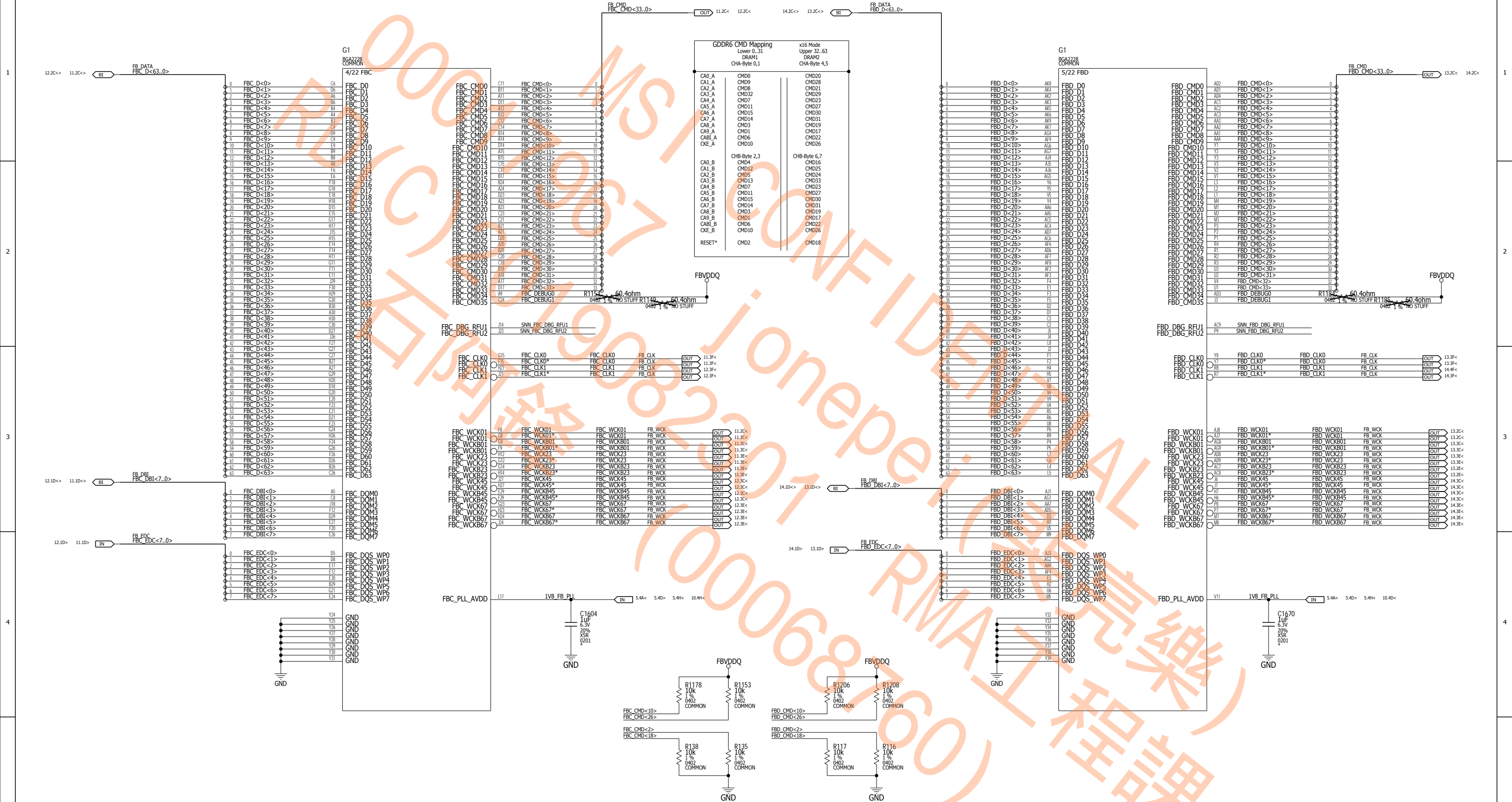








Page10: MEMORY: GPU Partition C/D



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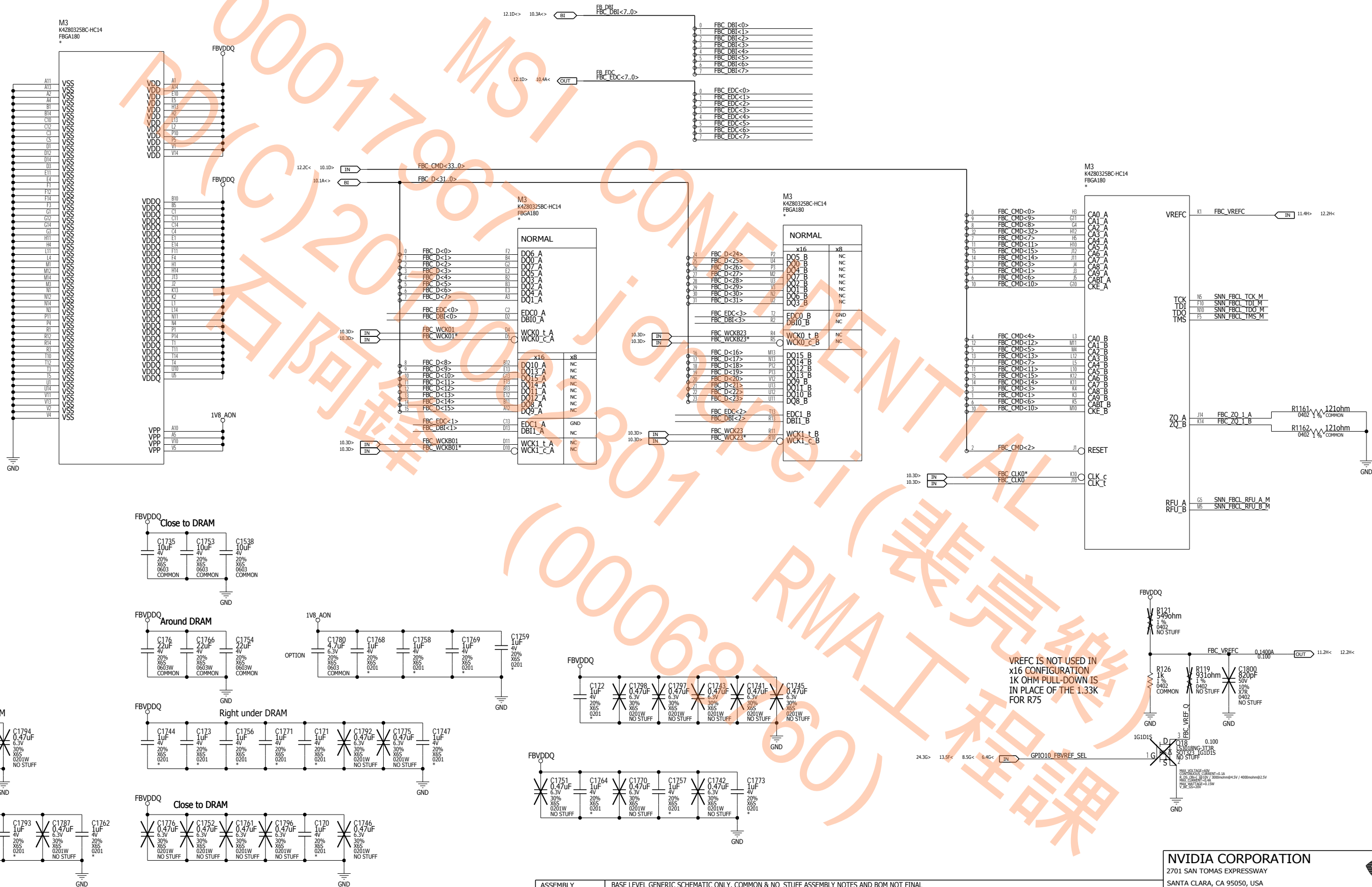
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PAGE 10 OF 54

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## Page11: MEMORY: FBC Partition 31..0



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PAGE DETAIL	MEMORY: FBC Partition 31..0

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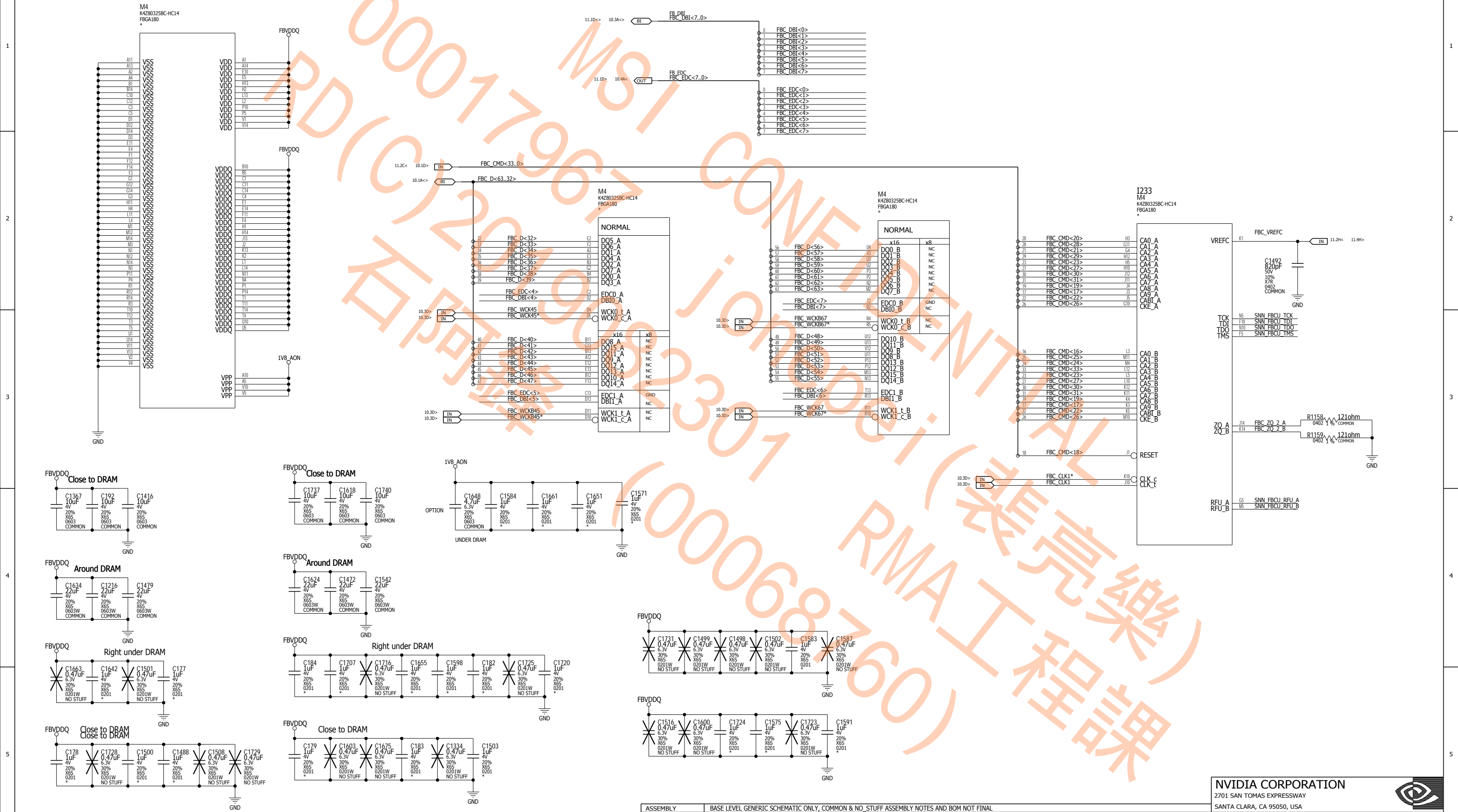
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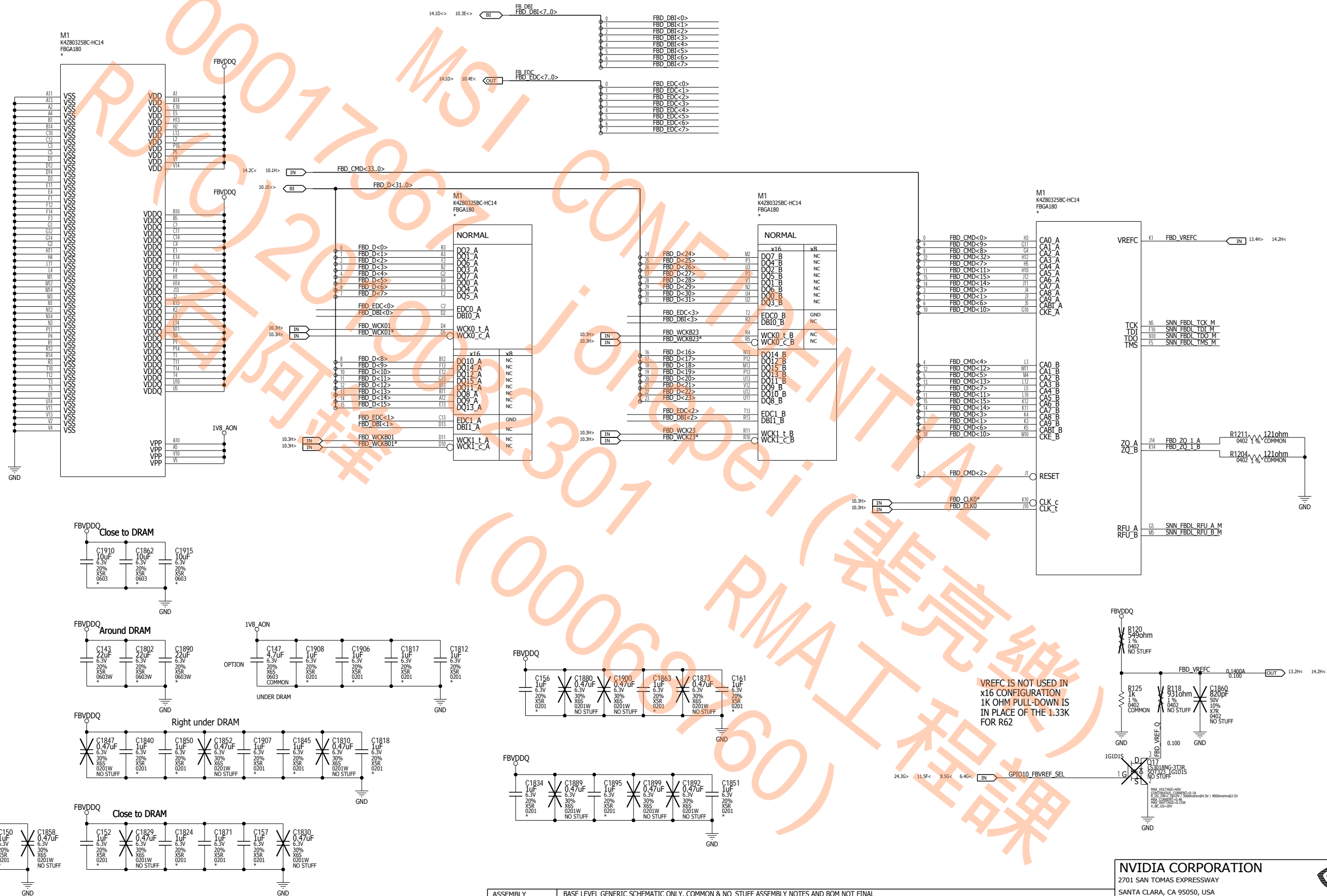
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PCB REV	PG180-A03	PAGE	11 OF 54
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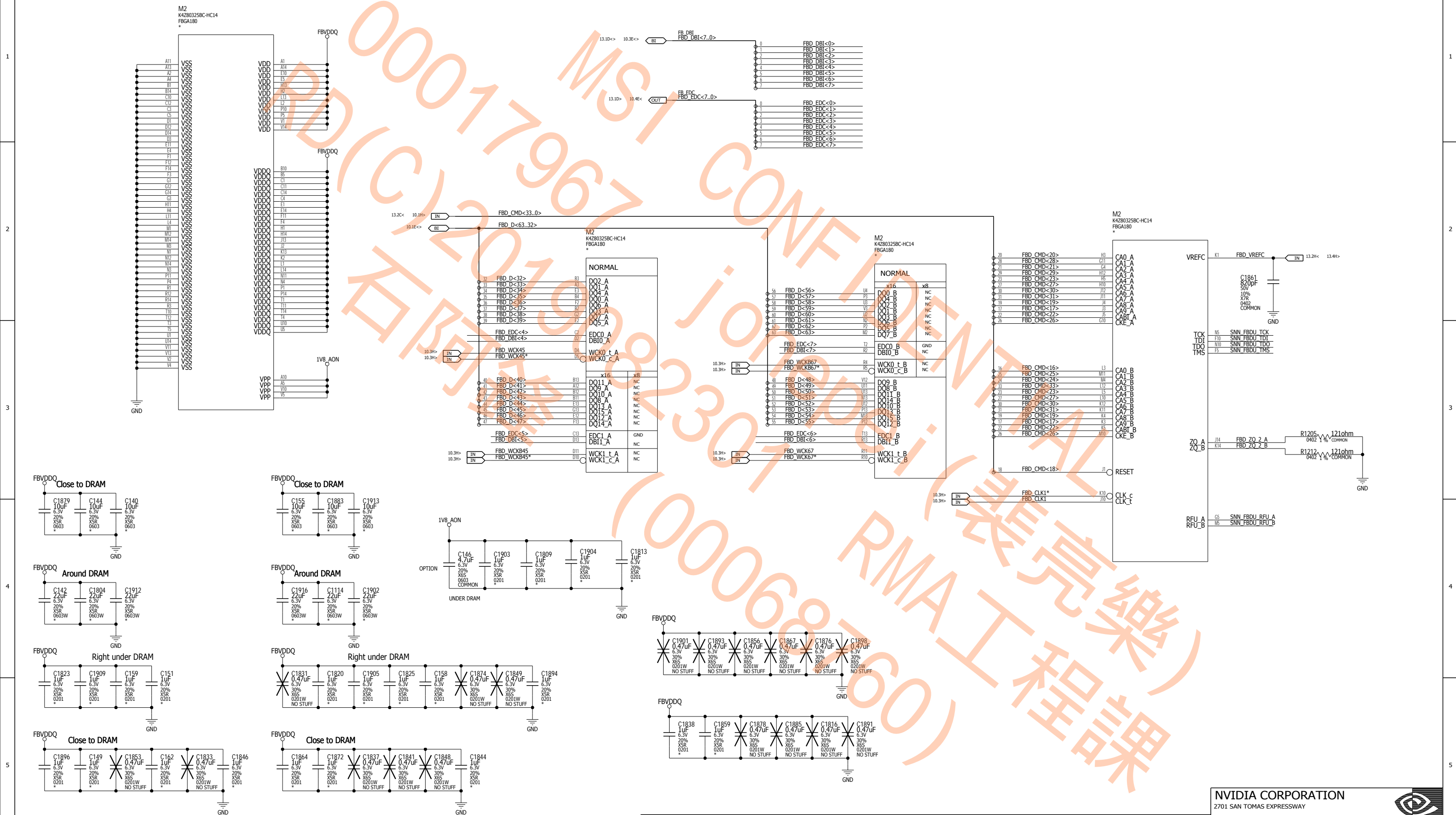


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PAGE DETAIL	MEMORY: FBD Partition 31..0


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NV_PN	600-1G180-0003-QS2		
PCB REV	PG180-A03	PAGE	13 OF 54
BOM REV	A	DATE	06-FEB-2019

## Page14: MEMORY: FBD Partition 63..32



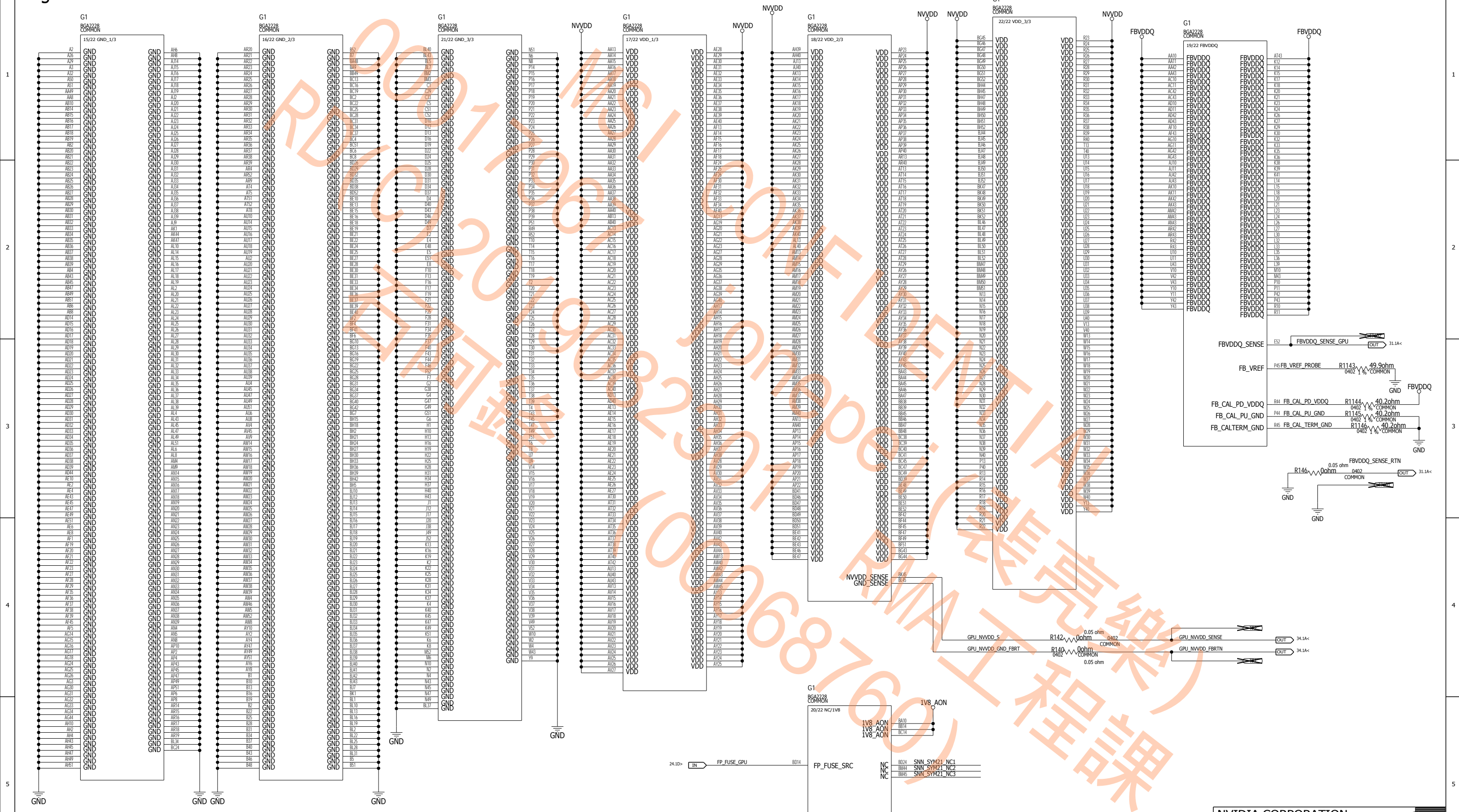
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PAGE DETAIL	MEMORY: FBD Partition 63..32

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<b>PCB REV</b>	<b>P180-A03</b>	<b>PAGE</b>	<b>14 OF 54</b>
<b>BOM REV</b>	<b>A</b>	<b>DATE</b>	<b>06-FEB-2019</b>



## Page15: GPU PWR and GND



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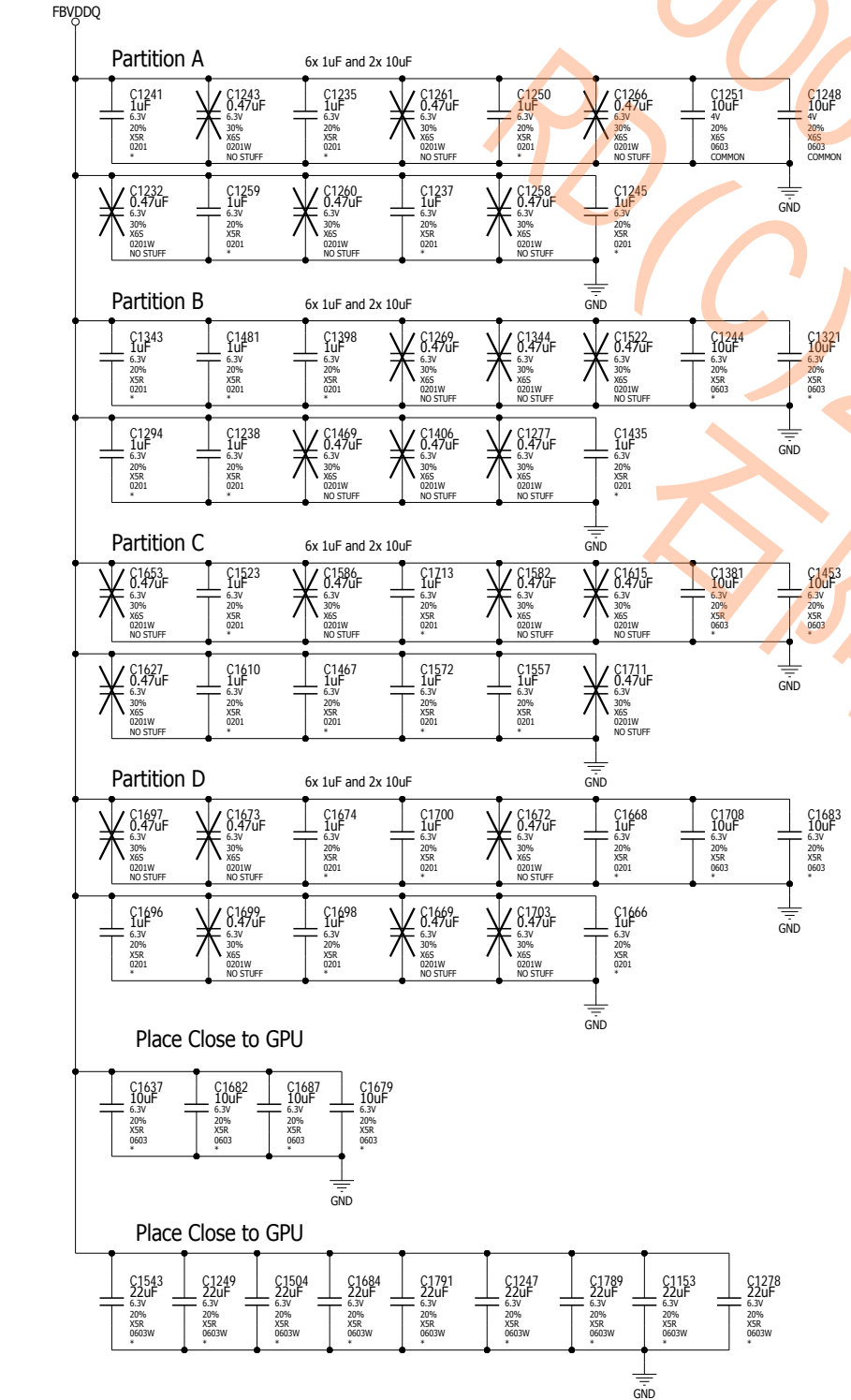
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PCB REV	PG180-A03	PAGE	15 OF 54
BOM REV	A	DATE	06-FEB-2019

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PAGE DETAIL	GPU PWR and GND

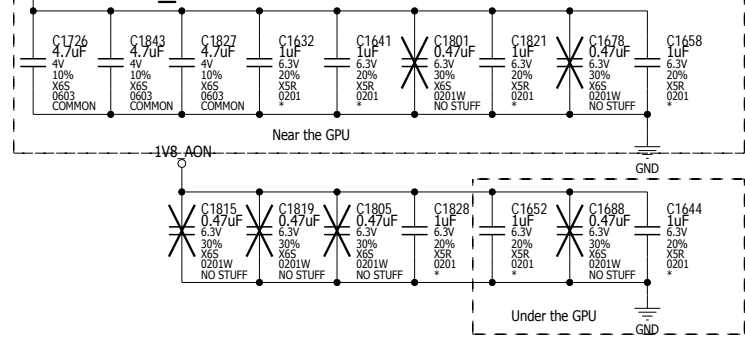
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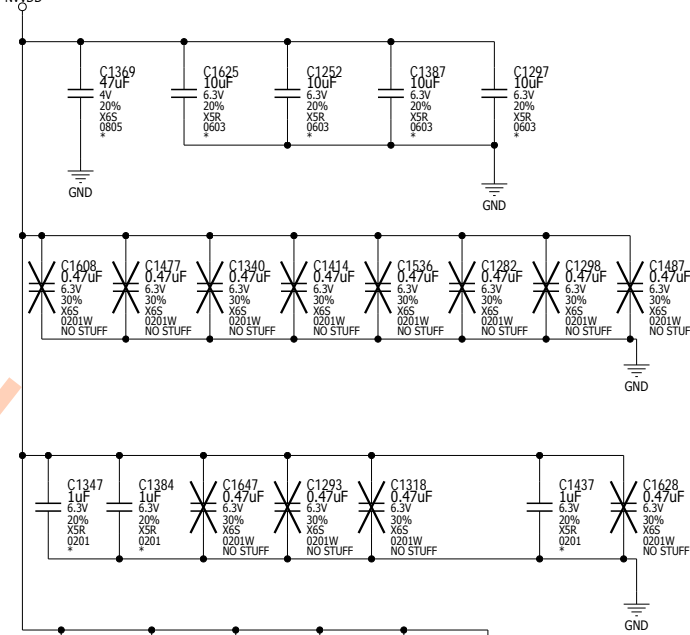
NWDD



1V8\_AON



NWDD



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PAGE DETAIL GPU Decoupling

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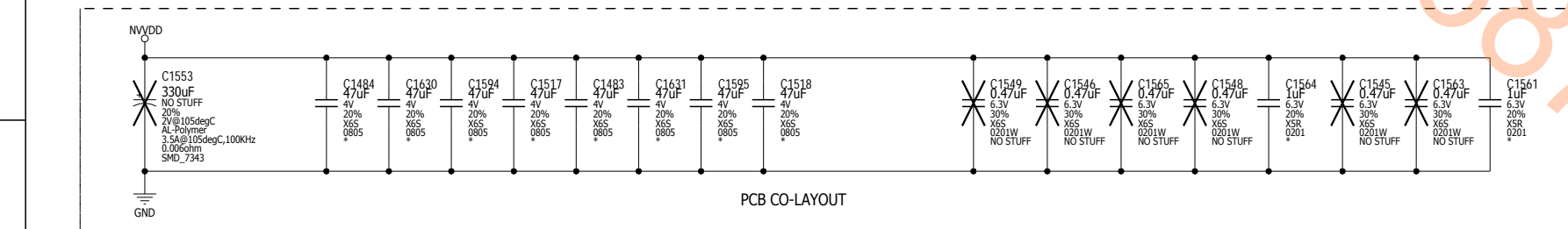
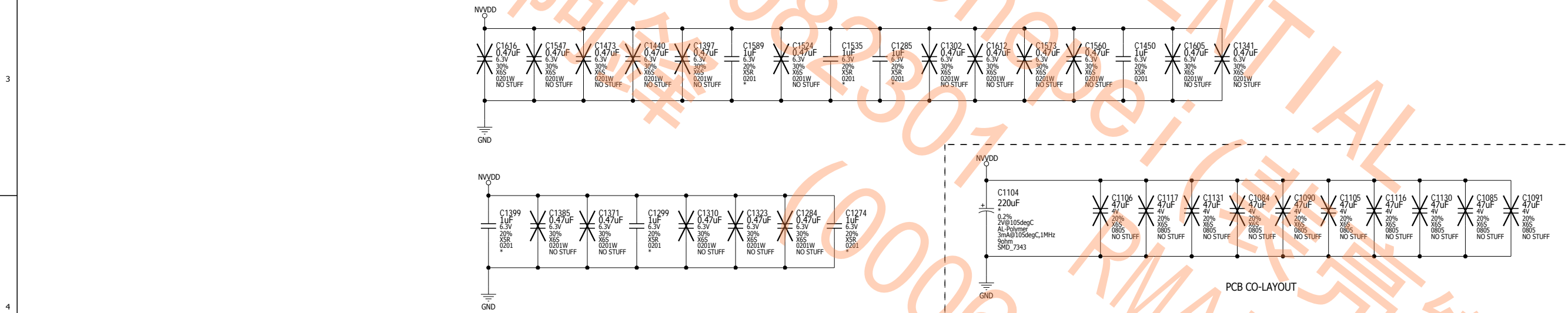
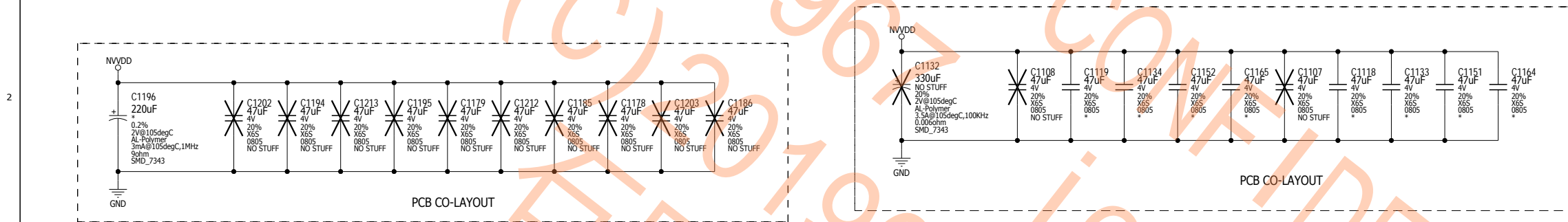
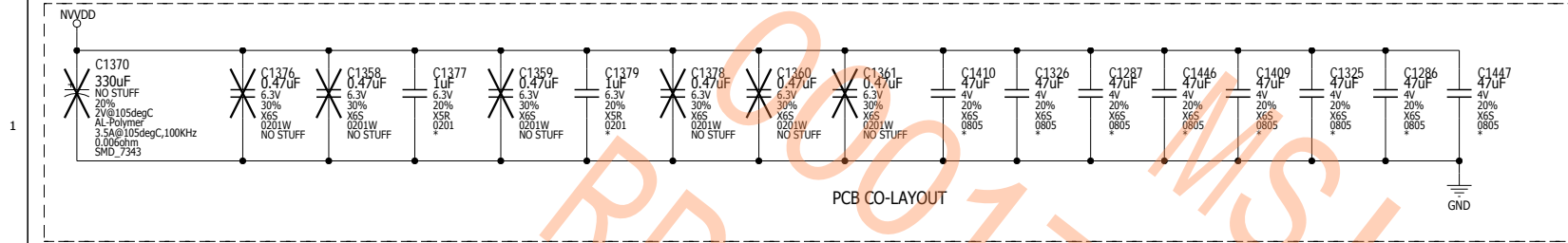
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16 OF 54

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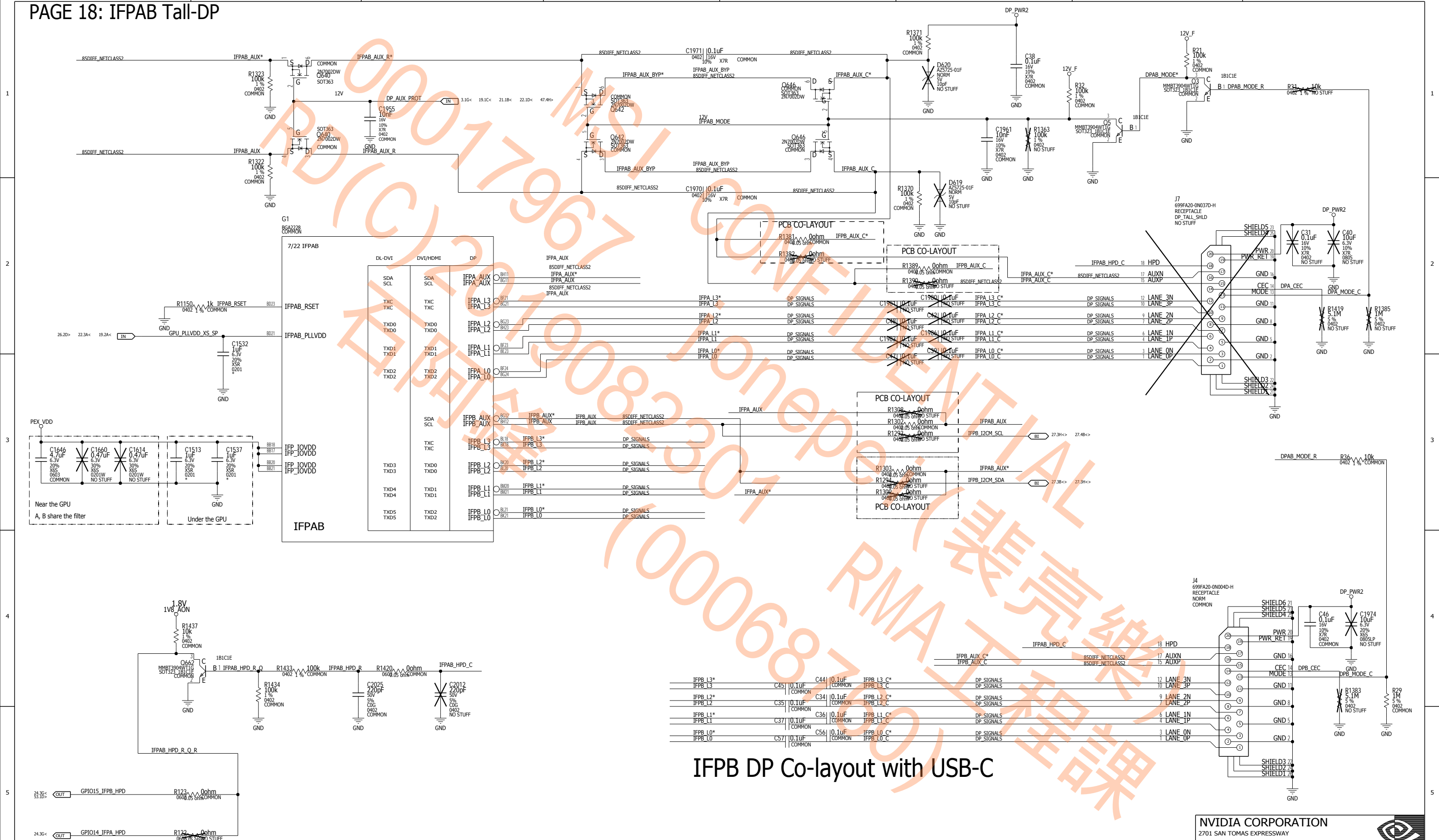
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## Page17: GPU Decoupling

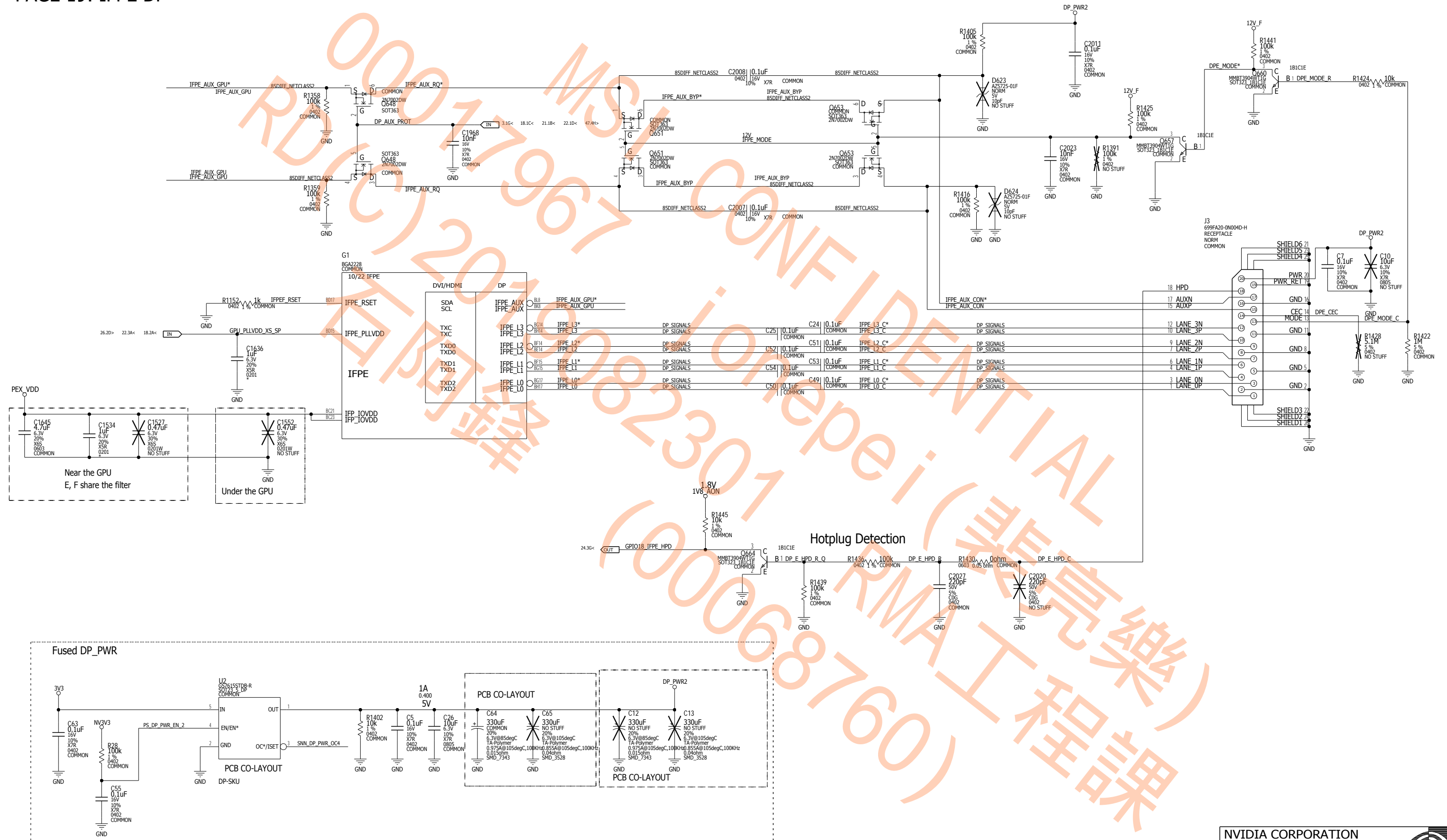


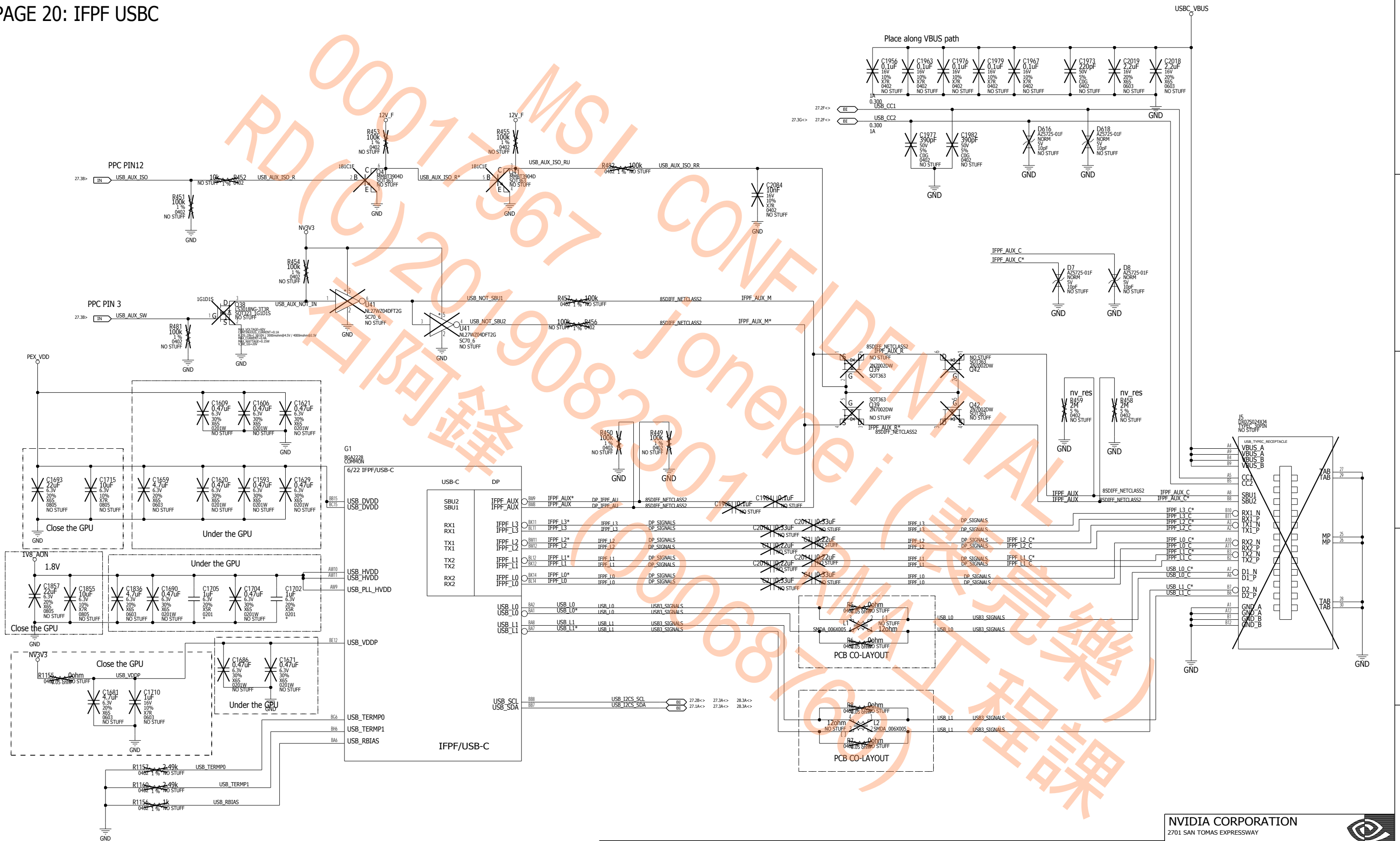


## PAGE 18: IFPAB Tall-DP

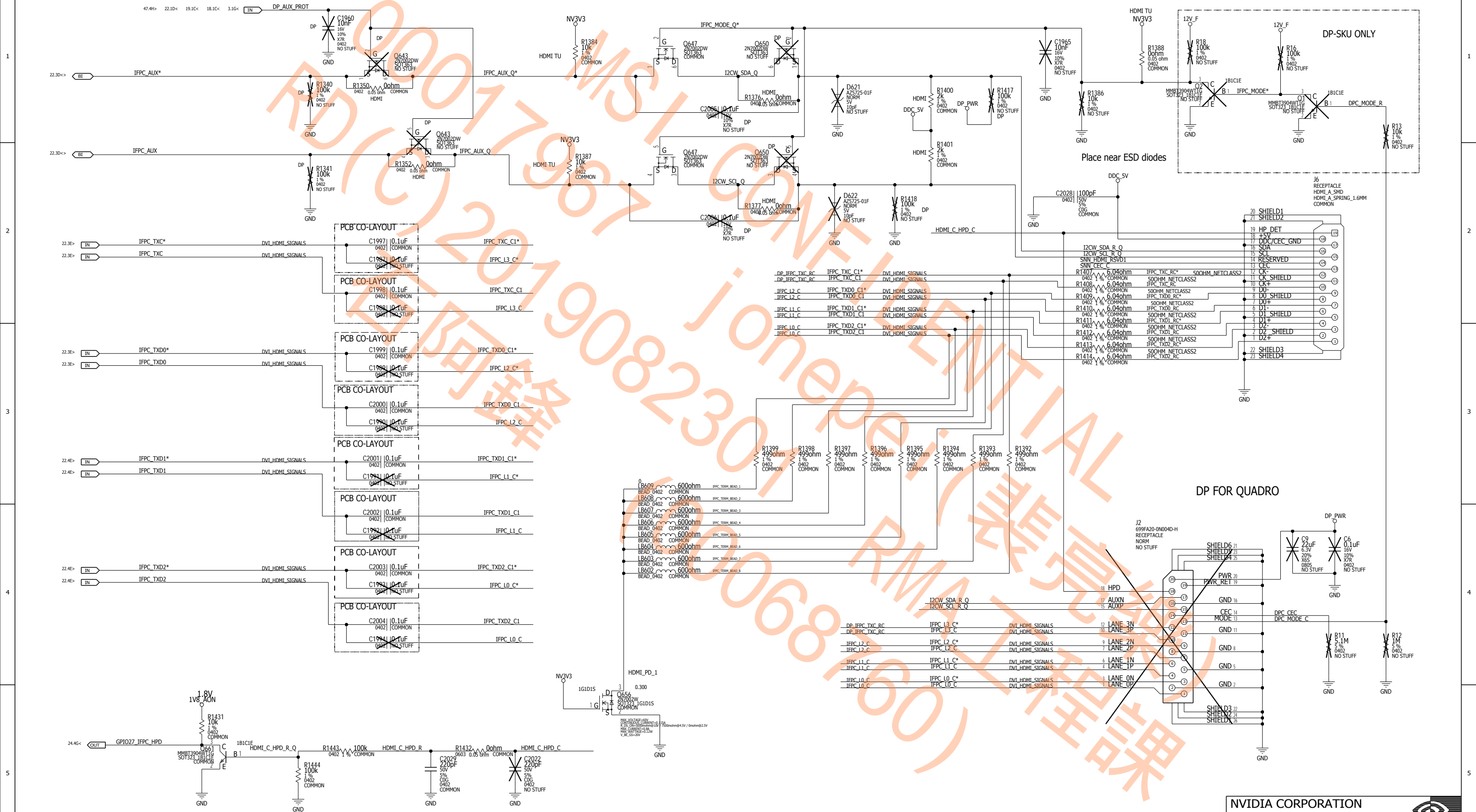


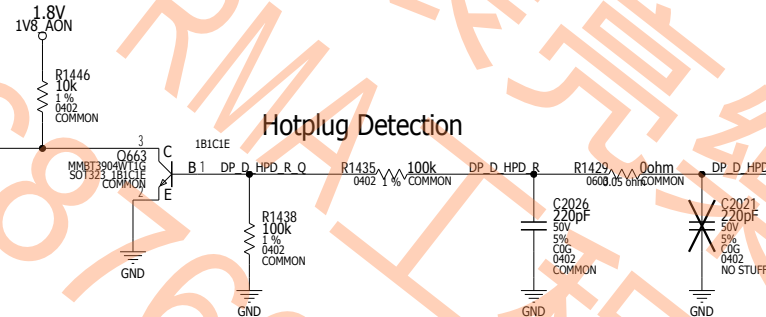
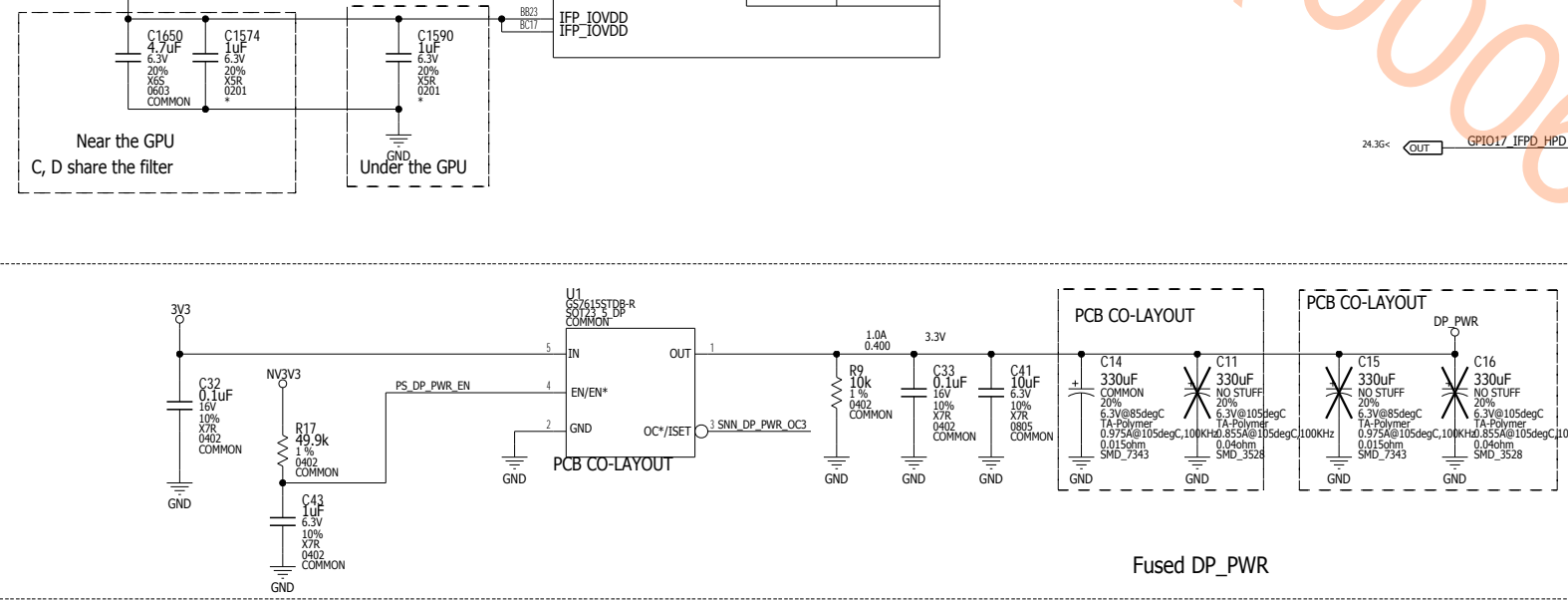
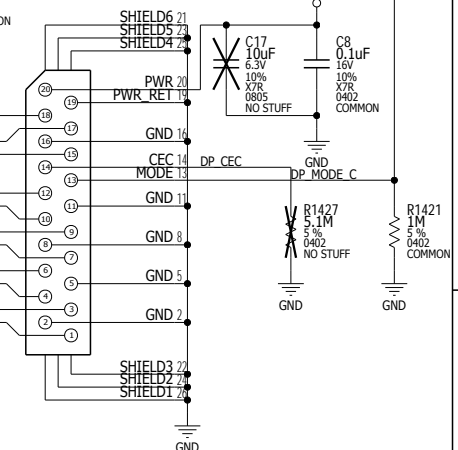
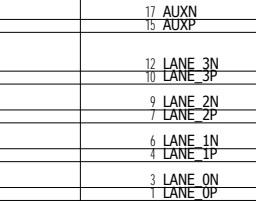
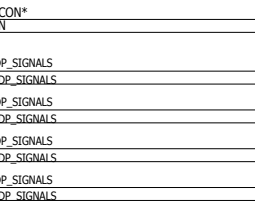
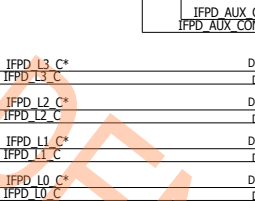
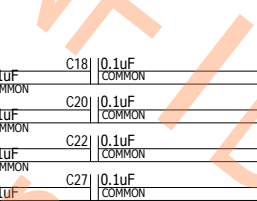
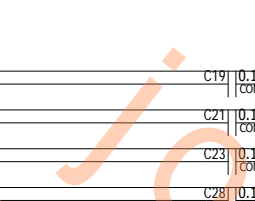
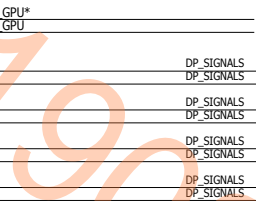
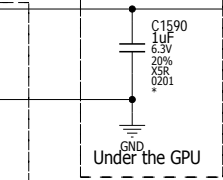
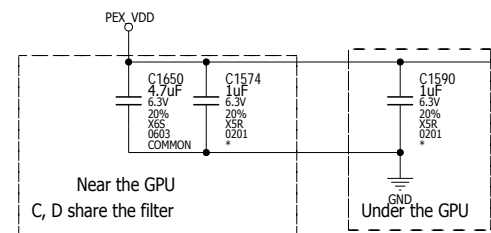
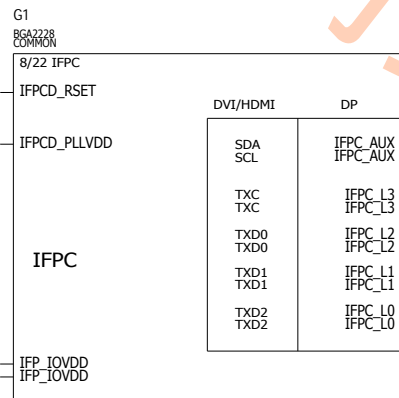
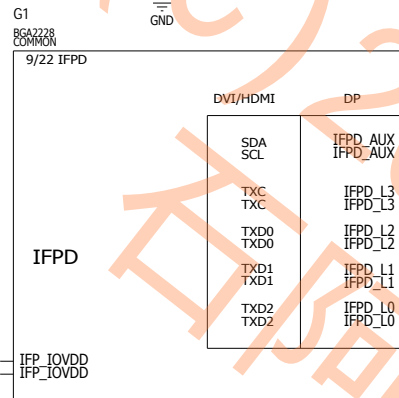
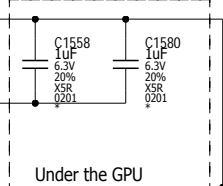
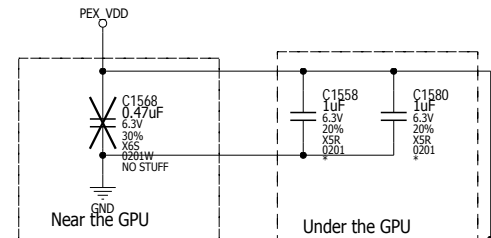
PAGE 19: IFPE DP










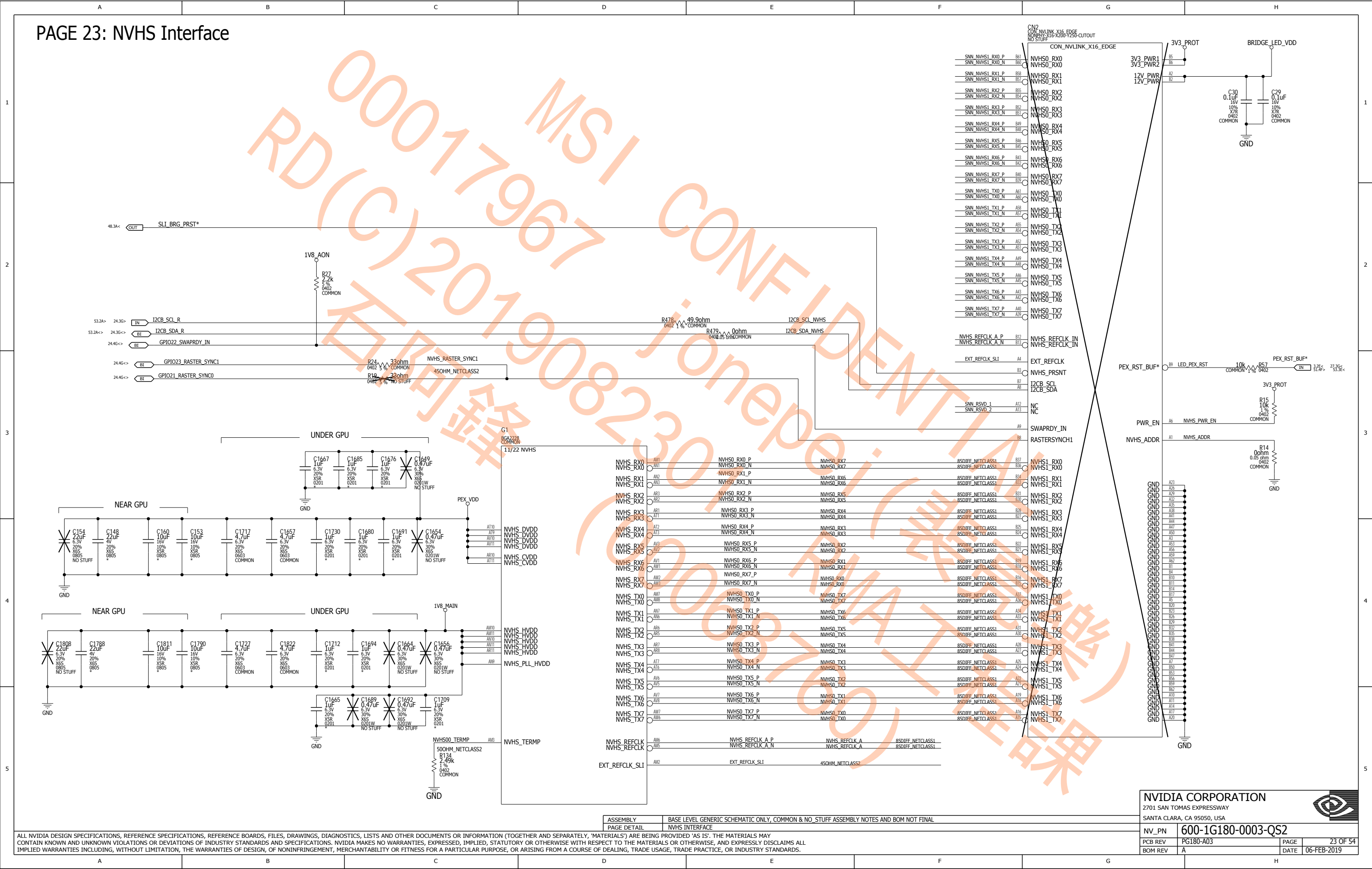


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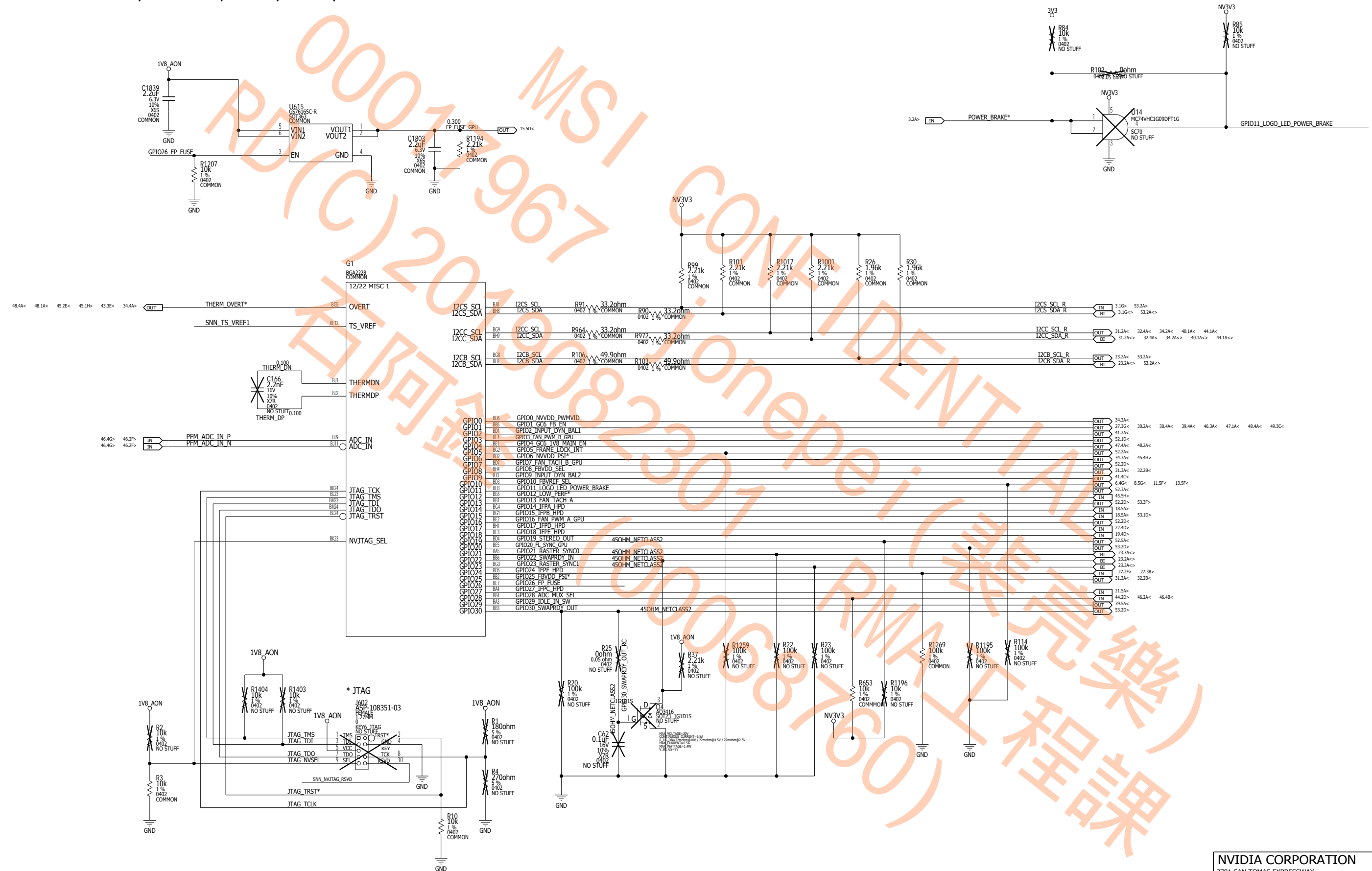
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PCB REV	PG180-A03	PAGE	22 OF 54
BOM REV	A	DATE	06-FEB-2019

## PAGE 23: NVHS Interface





## PAGE 24: MISC: Fan, Thermal, JTAG, GPIO, STEREO



PAGE 25: MISC: ROM, Straps

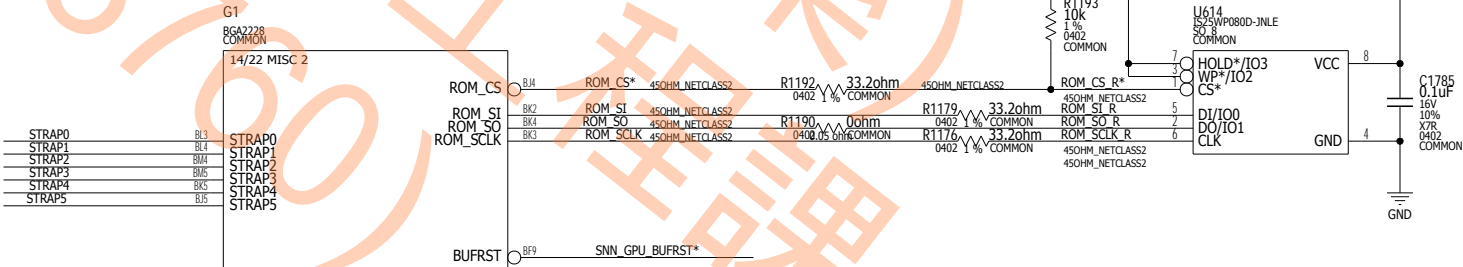
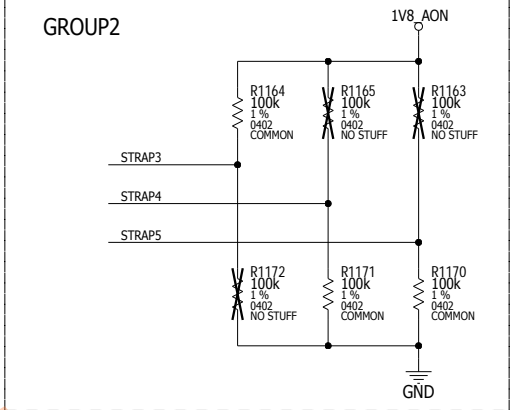
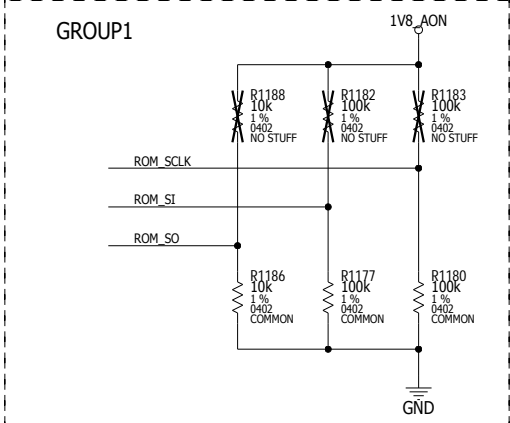
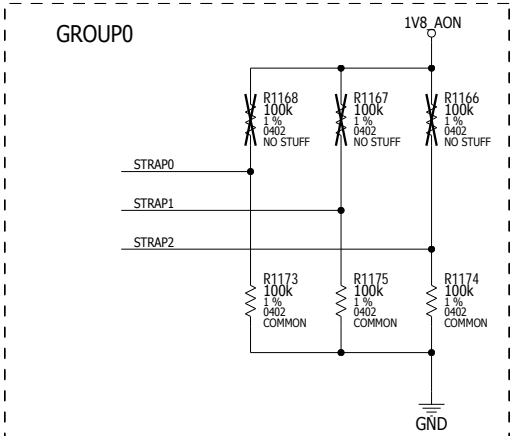
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	RAMCFG TBD	DEFAULT
L	L	L	00000	RAMCFG TBD	
L	L	H	00001	RAMCFG TBD	
L	H	L	00010	RAMCFG TBD	
L	H	H	00011	RAMCFG TBD	
H	H	L	00110	RAMCFG TBD	
H	H	H	00111	RAMCFG TBD	

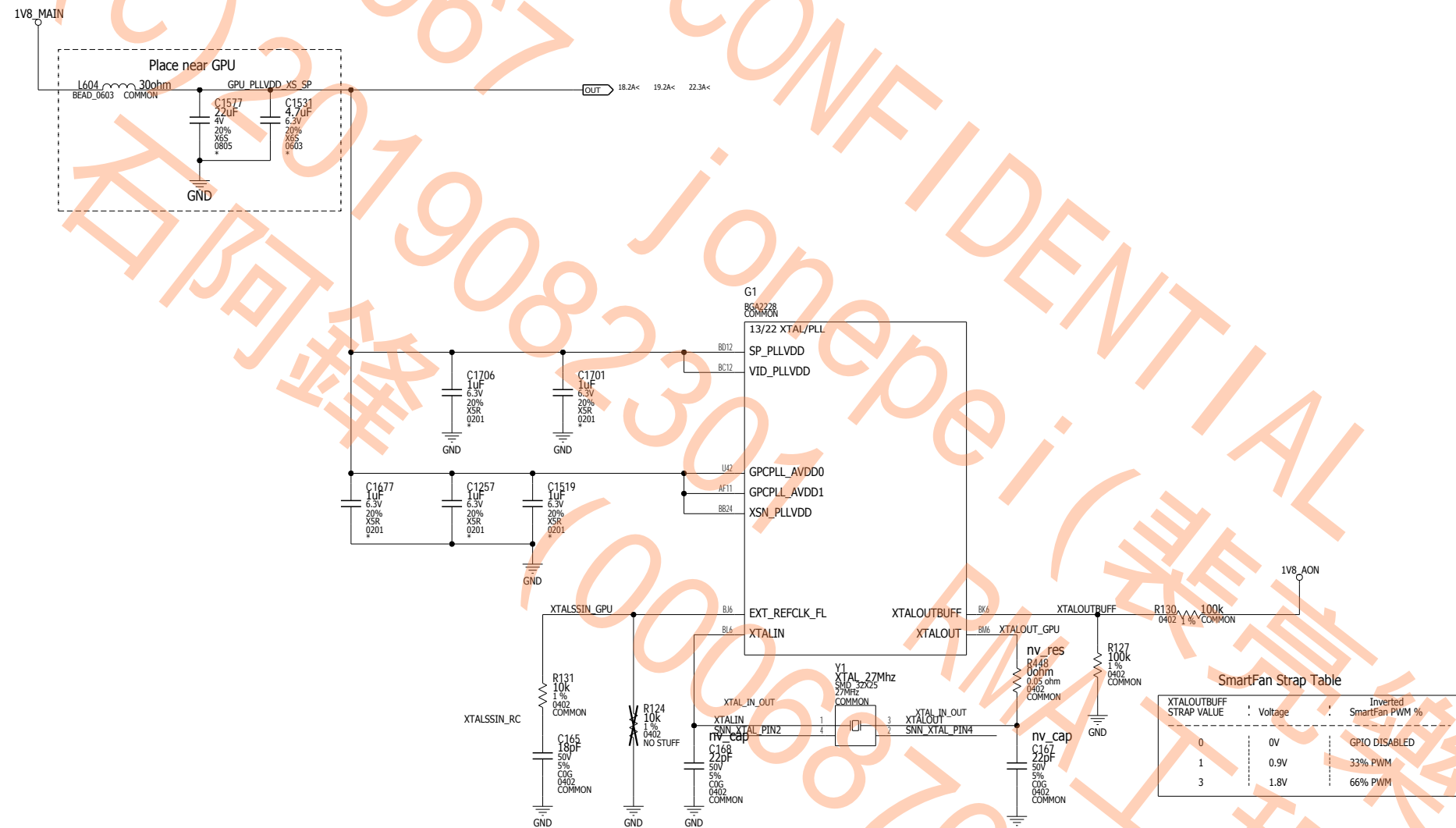
RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	DEFAULT
L	L	L	XXX1	FS_OVERT ENABLE	
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	Default
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	



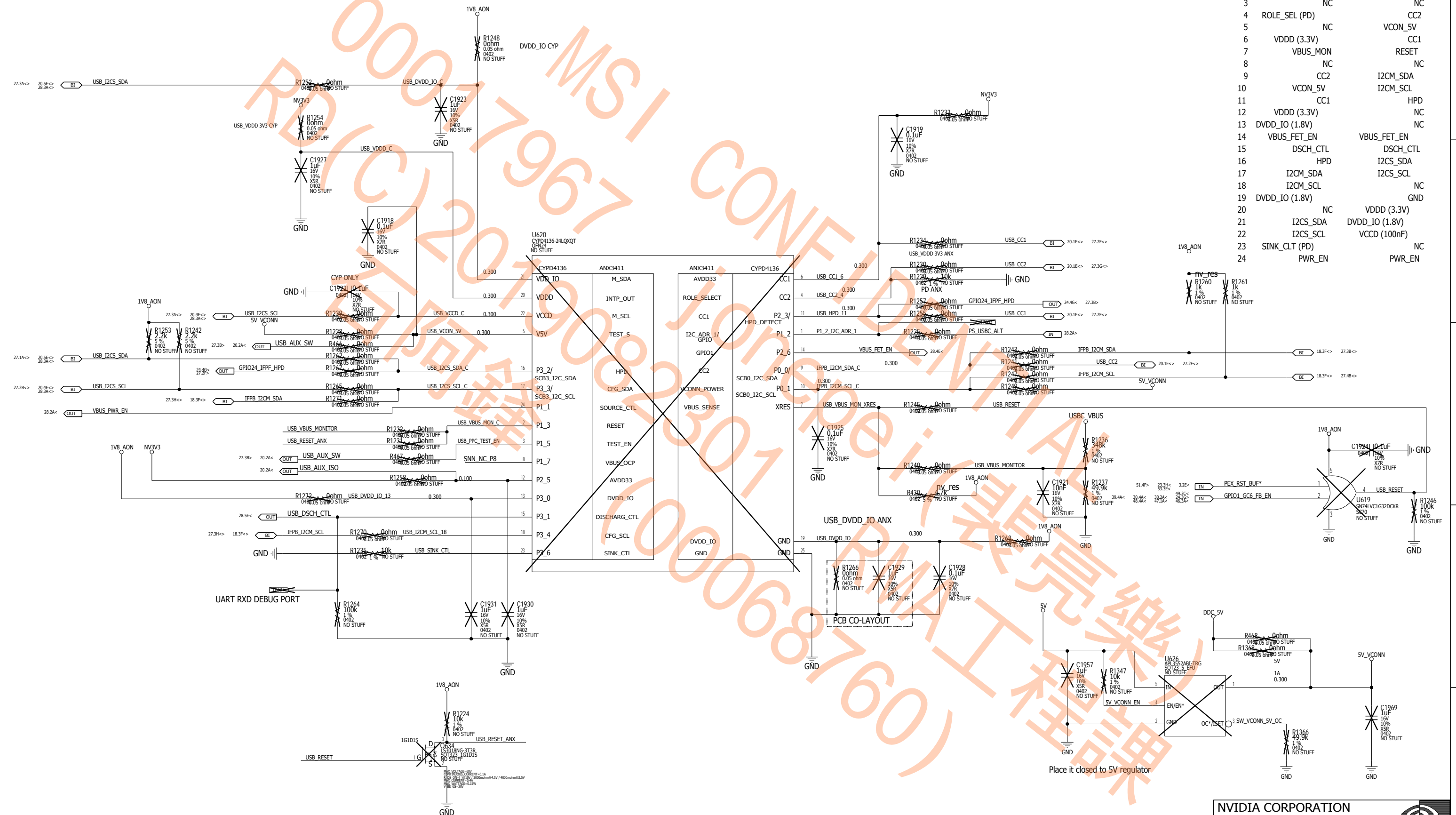
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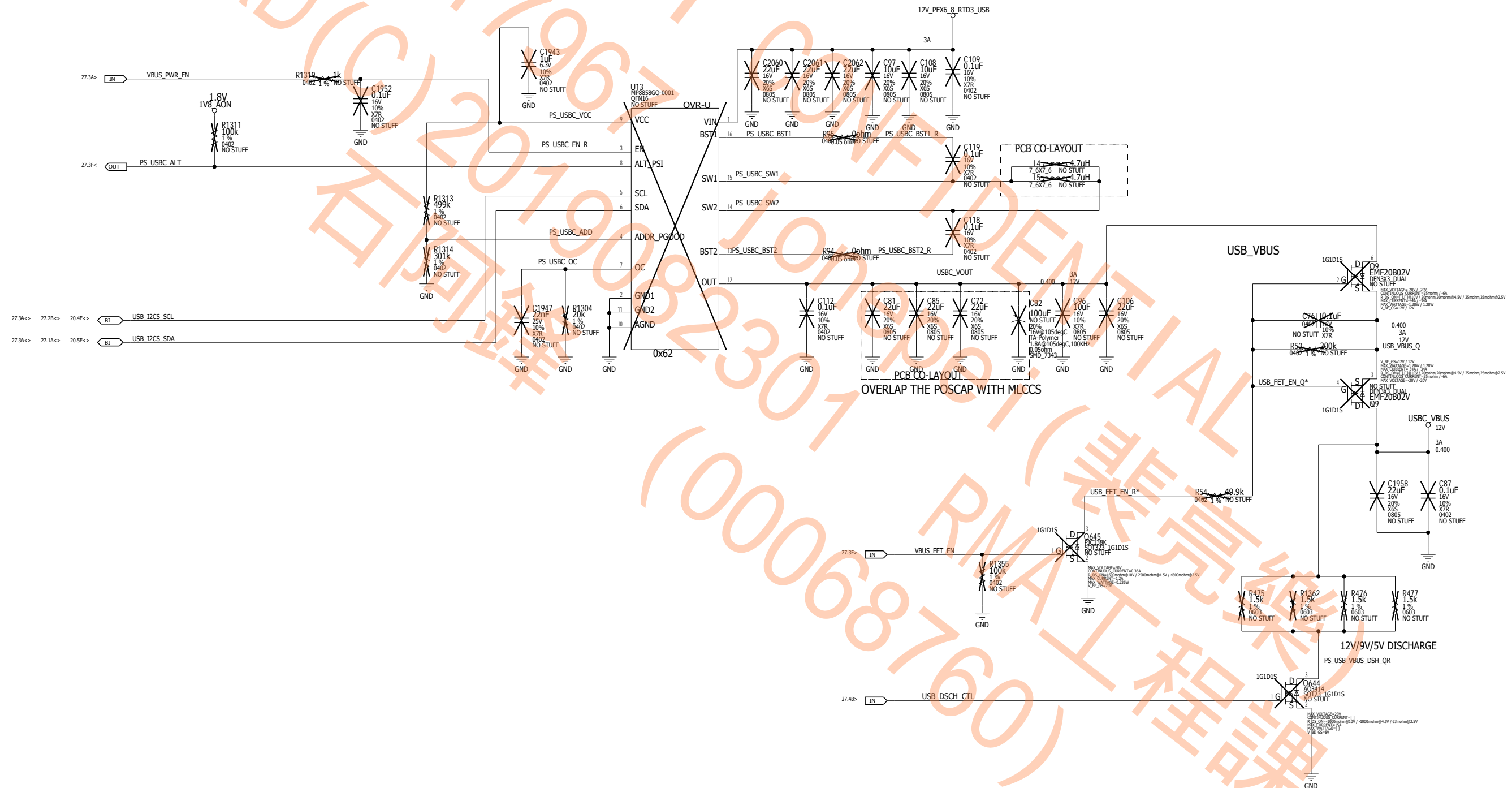
XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	0.9V	33% PWM
3	1.8V	66% PWM



## PAGE 27: MISC: USB PPC

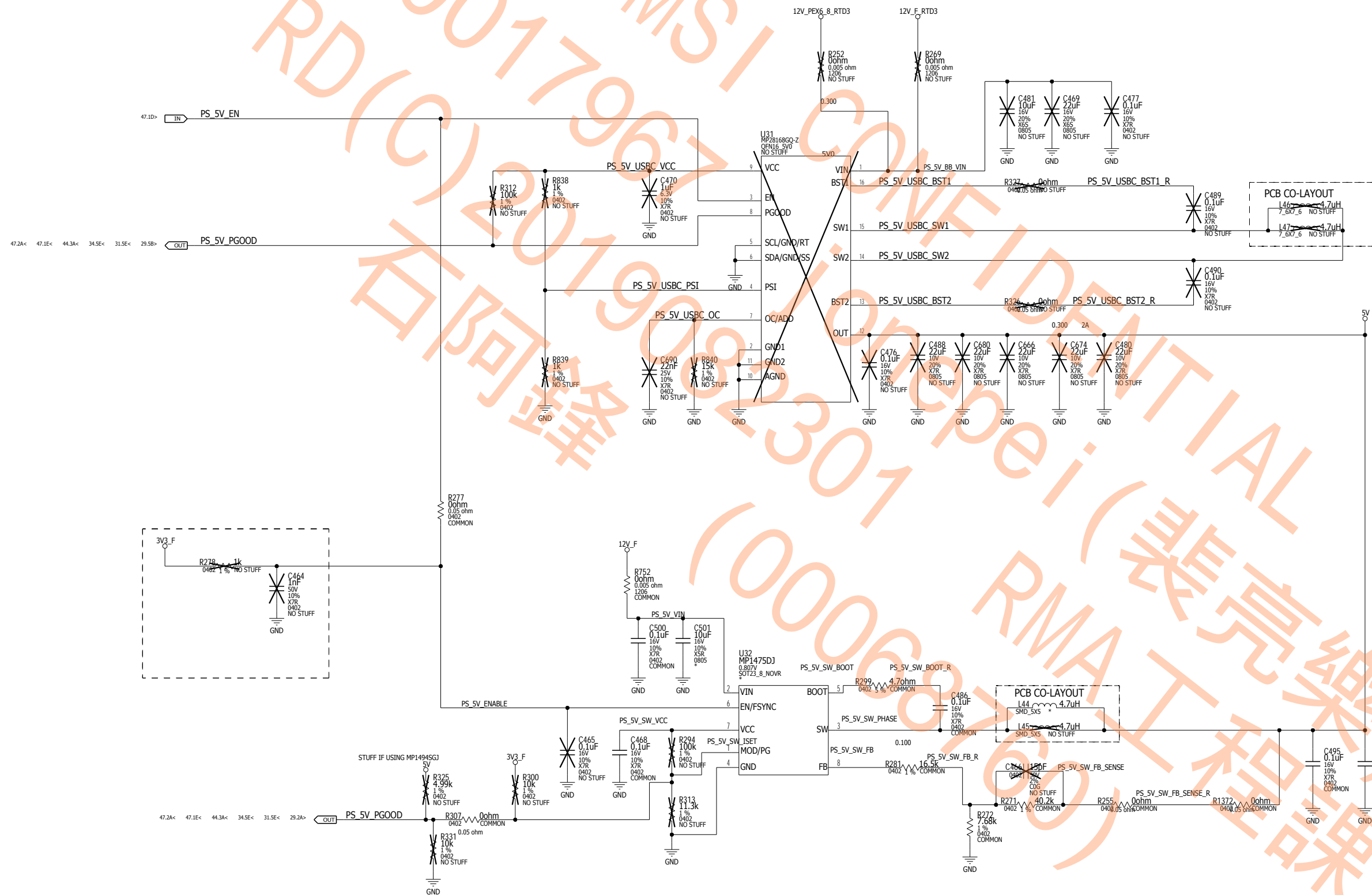


PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_SV
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_SV	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN



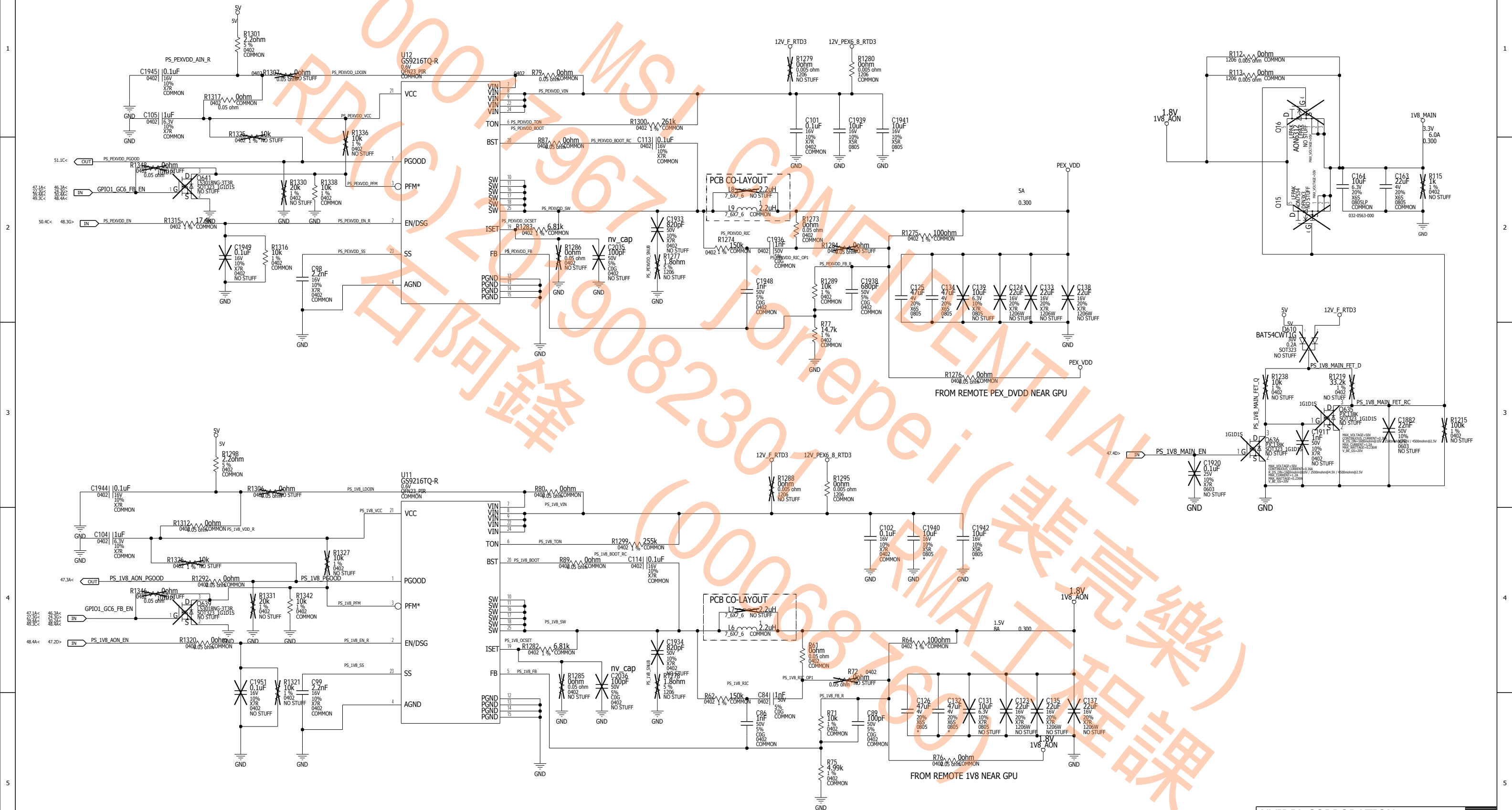
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: USB VR

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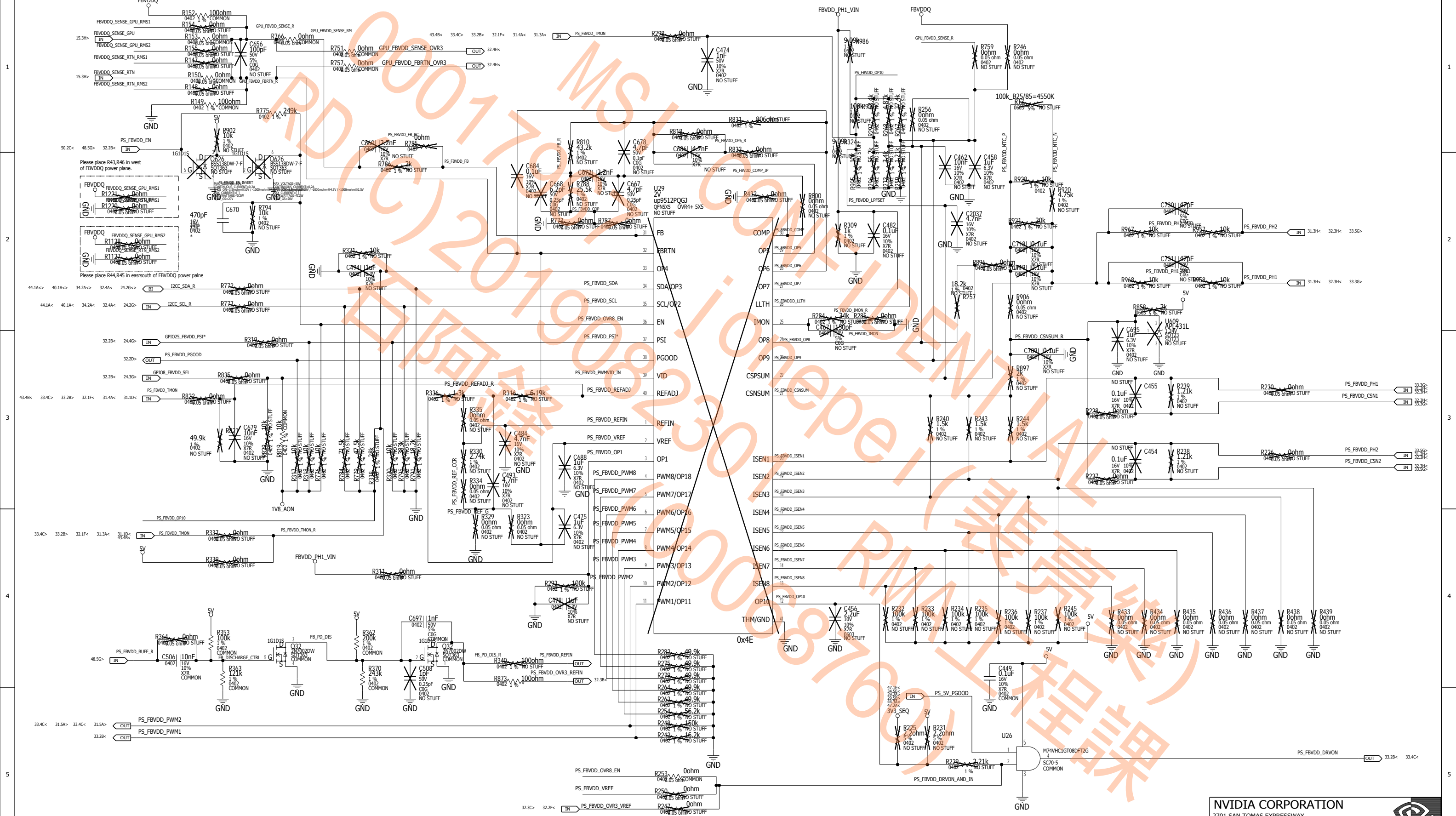
PAGE 30: PS: PEXVDD, 1V8



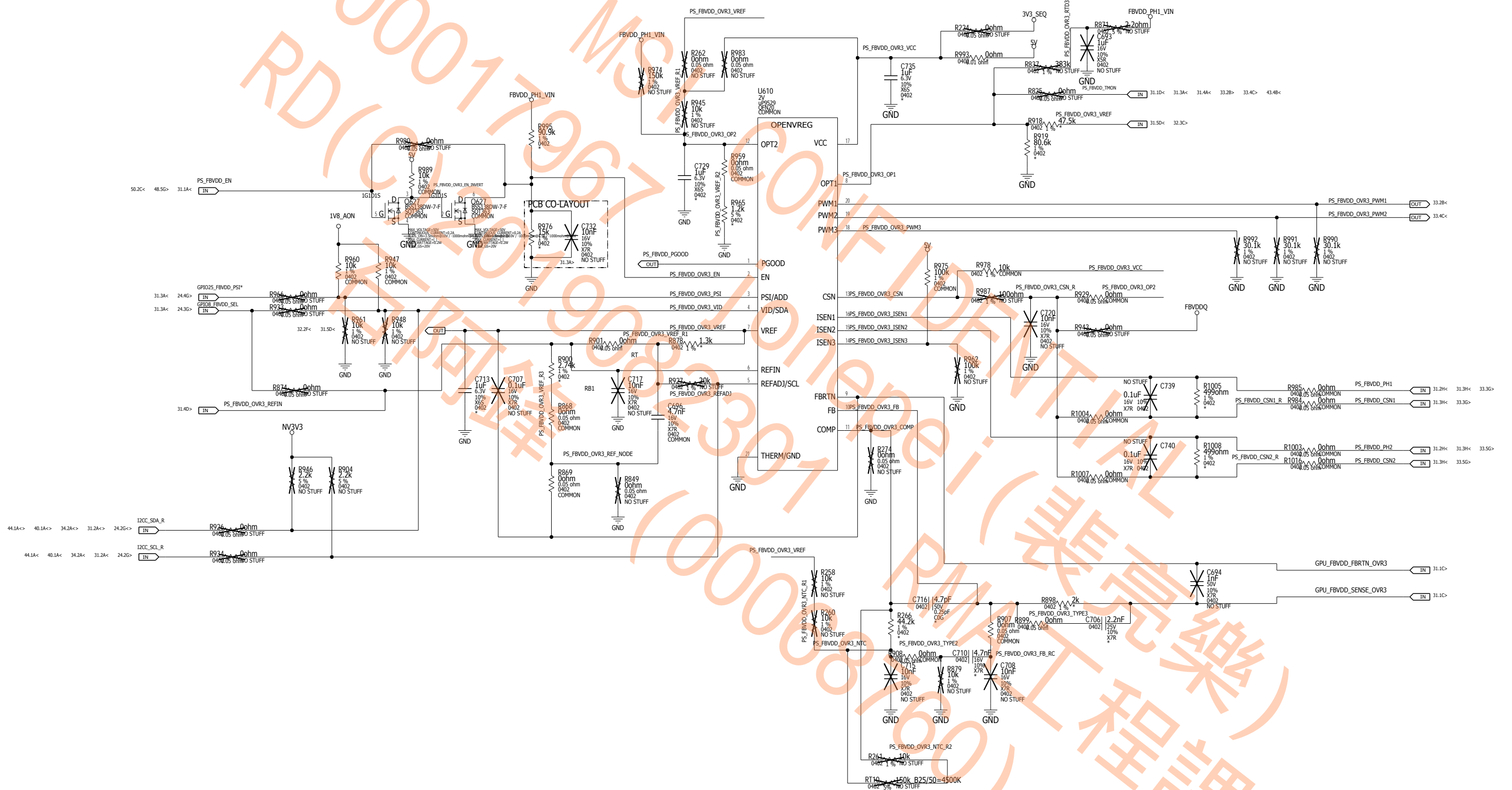
<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
<b>NV_PN</b>		<b>600-1G180-0003-QS2</b>		
<b>PCB REV</b>	<b>P180-A03</b>	<b>PAGE</b>	<b>30 OF 54</b>	
<b>BOM REV</b>	<b>A</b>	<b>DATE</b>	<b>06-FEB-2019</b>	

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PAGE 31: PS: FBVDD Controller




## PAGE 32: PS: FBVDD Controller OVR3



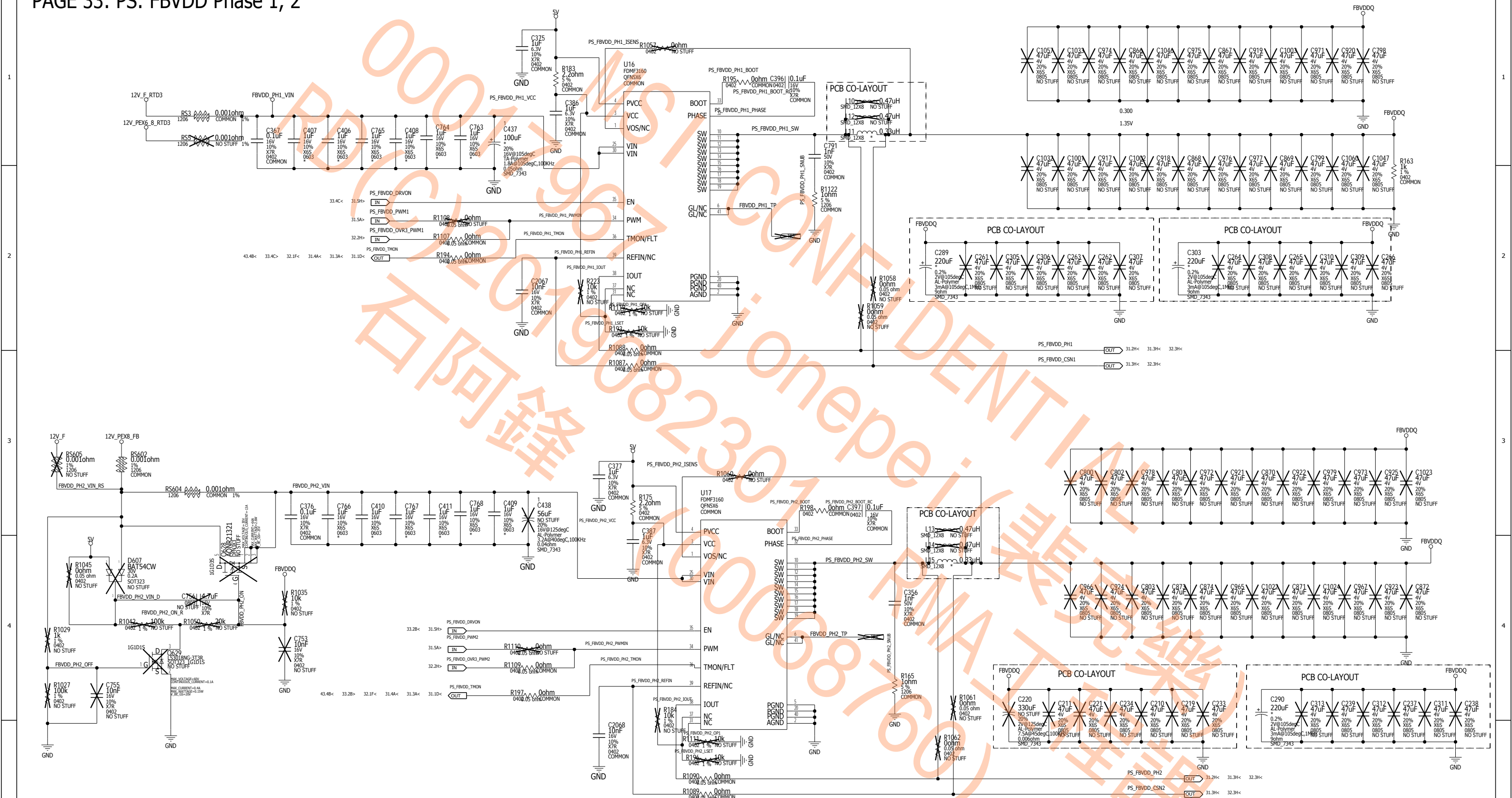
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: FBVDD CONTROLLER OVR3

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BOM REV	A	DATE	06-FEB-2019



## PAGE 33: PS: FBVDD Phase 1, 2



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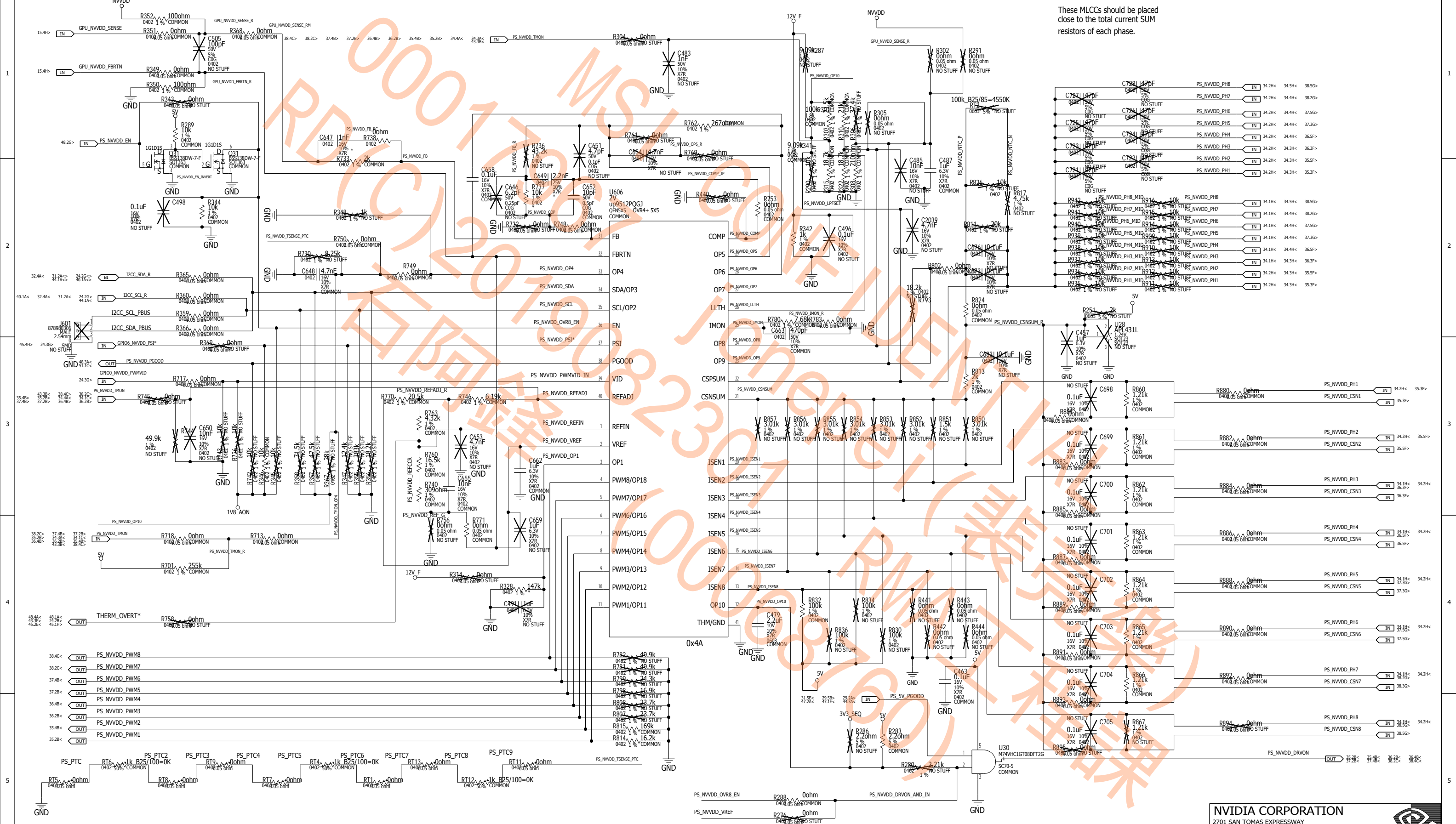


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PCB REV	PG180-A03	PAGE	33 OF 54
BOM REV	A	DATE	06-FEB-2019

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PAGE 34: PS: NVVDD Controller OVR8



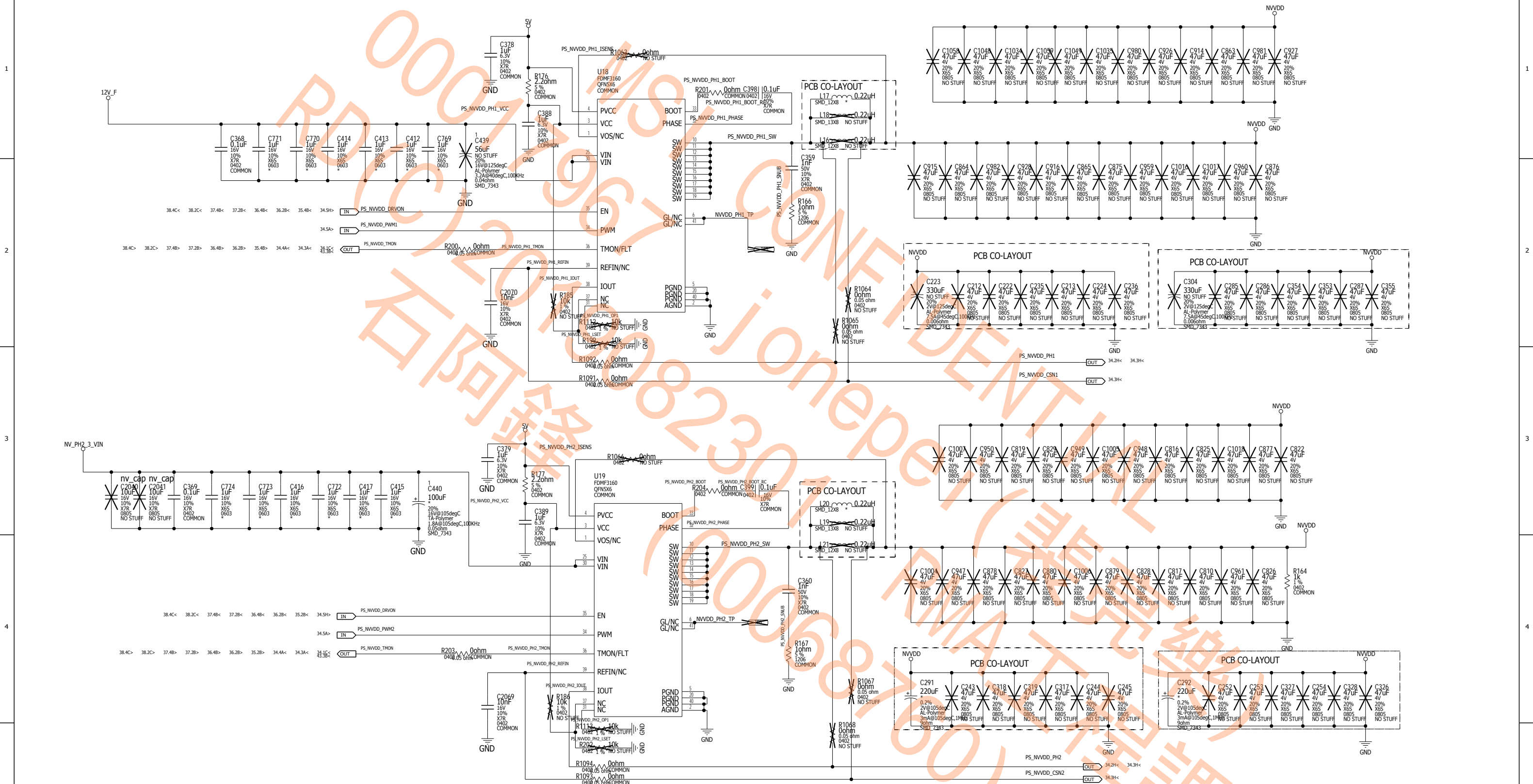
These MLCCs should be placed close to the total current SUM resistors of each phase.

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PAGE DETAIL	PS: NVVDD CONTROLLER OVR8

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PCB REV	PG180-A03	PAGE	34 OF 54
BOM REV	A	DATE	06-FEB-2019

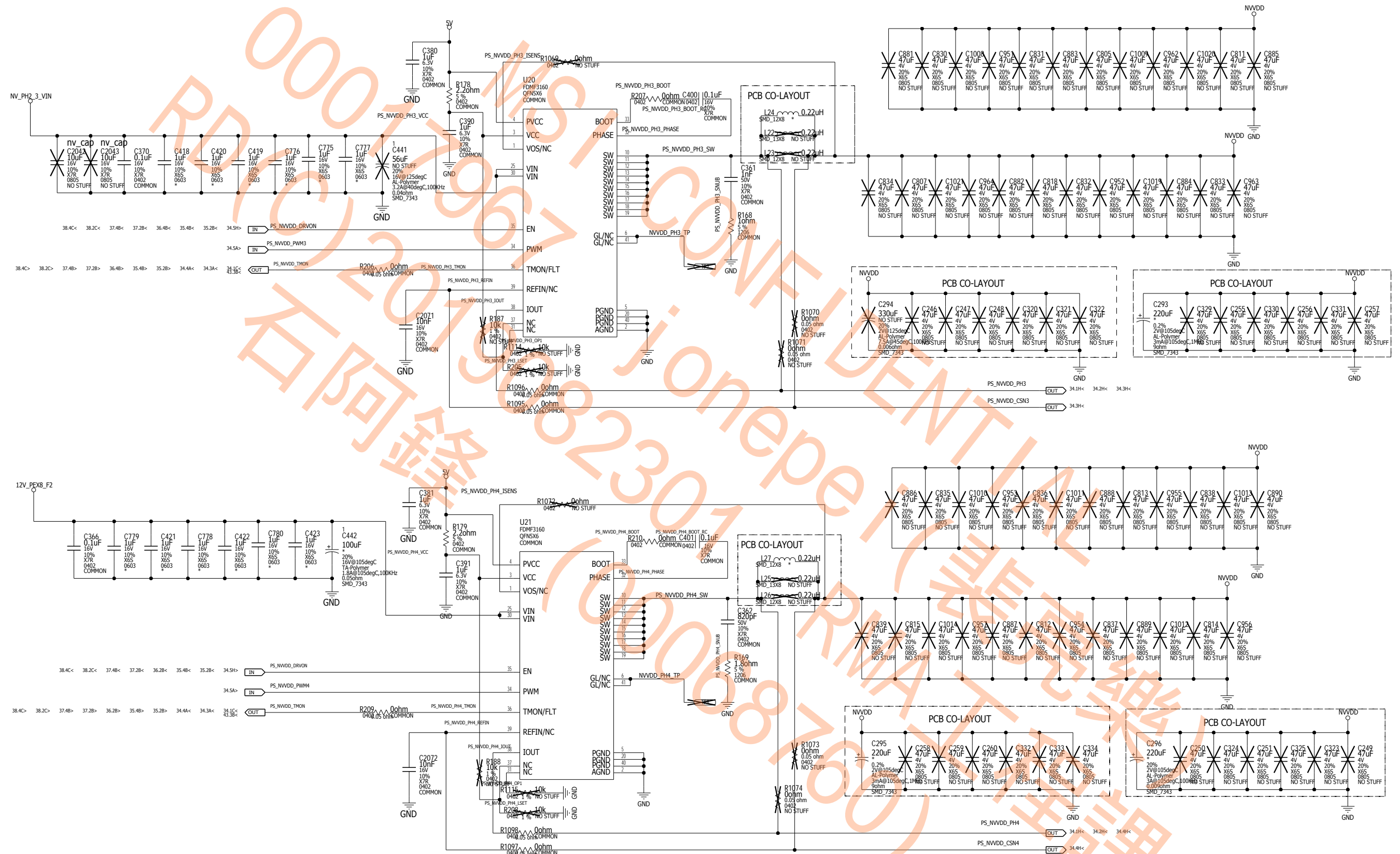




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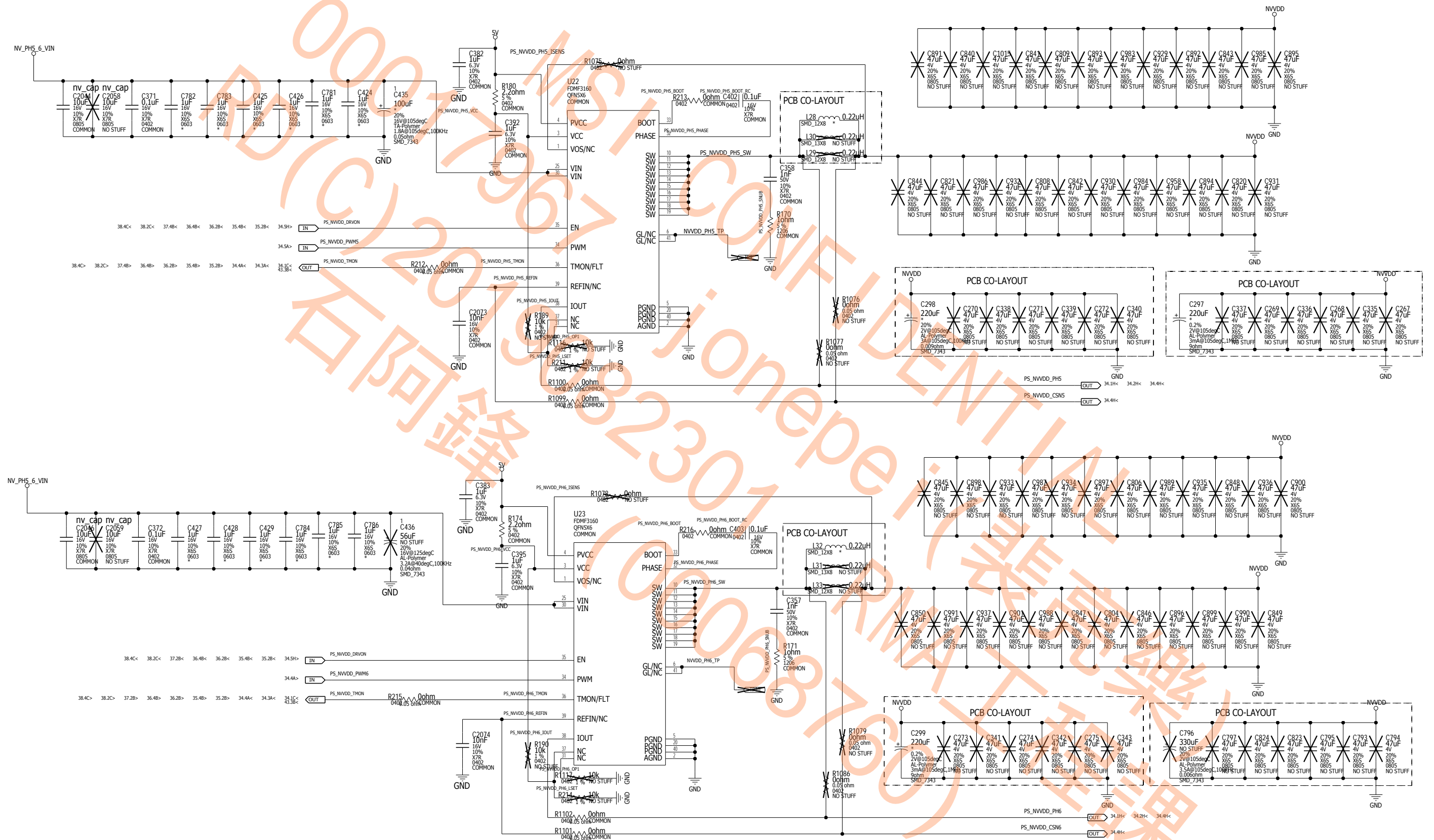
PAGE 36: PS: NVVDD Phase 3, 4

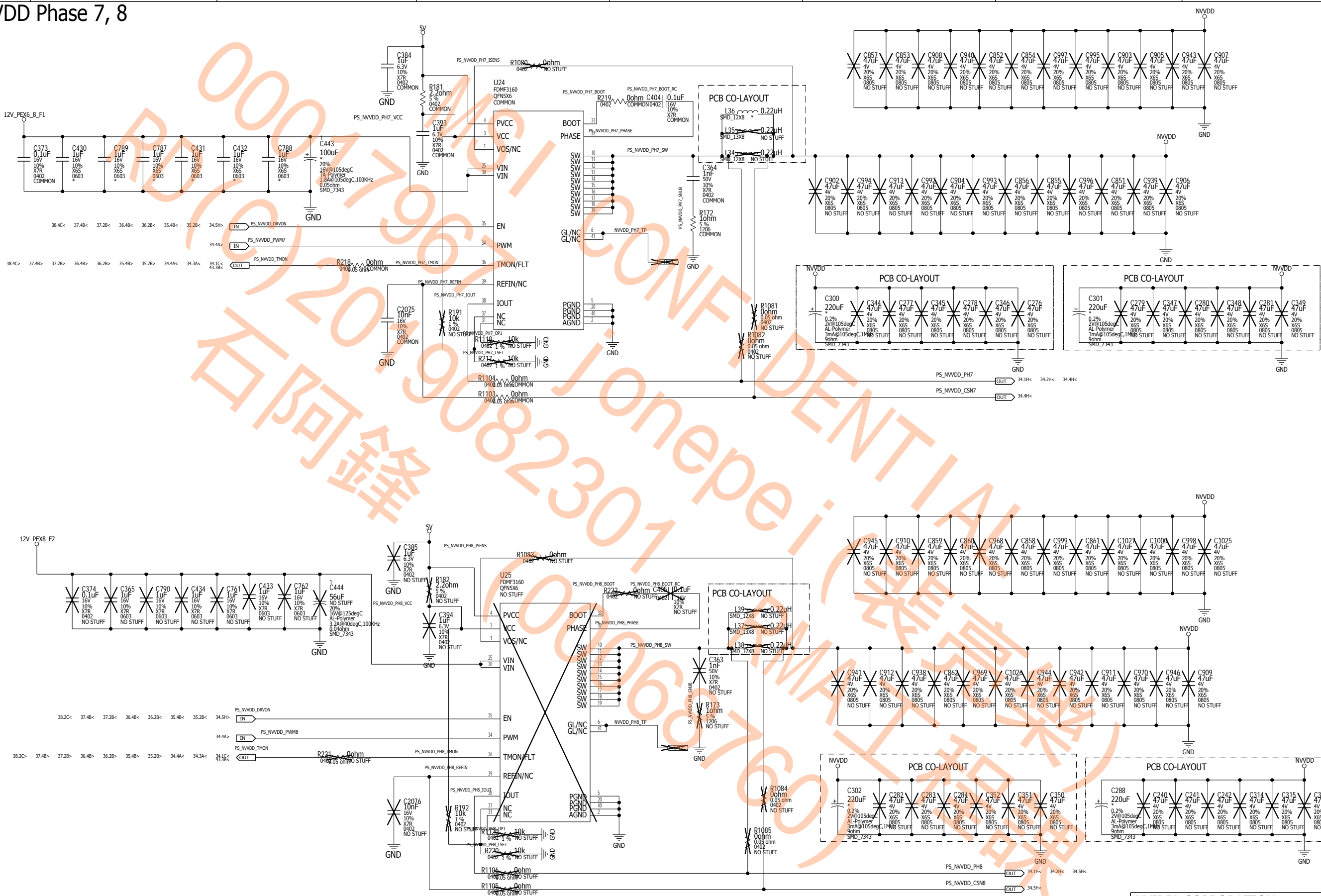


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD Phase 3, 4

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PCB REV	PG180-A03	PAGE	36 OF 54
BOM REV	A	DATE	06-FEB-2019





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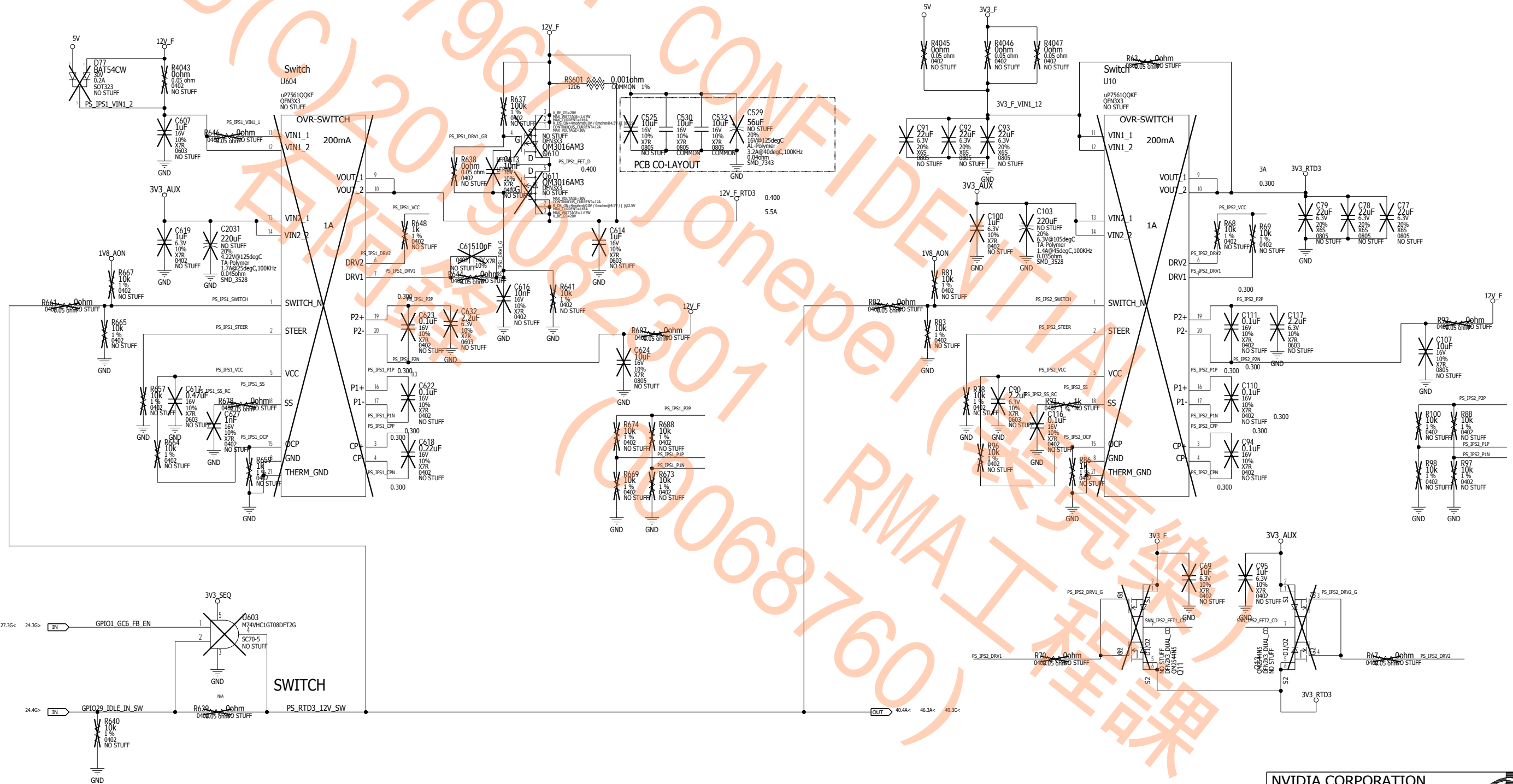
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PAGE DETAIL	PS: NVVDD Phase 7, 8

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PCB REV	PG180-A03	DATE	06-FEB-2019
BOM REV	A		

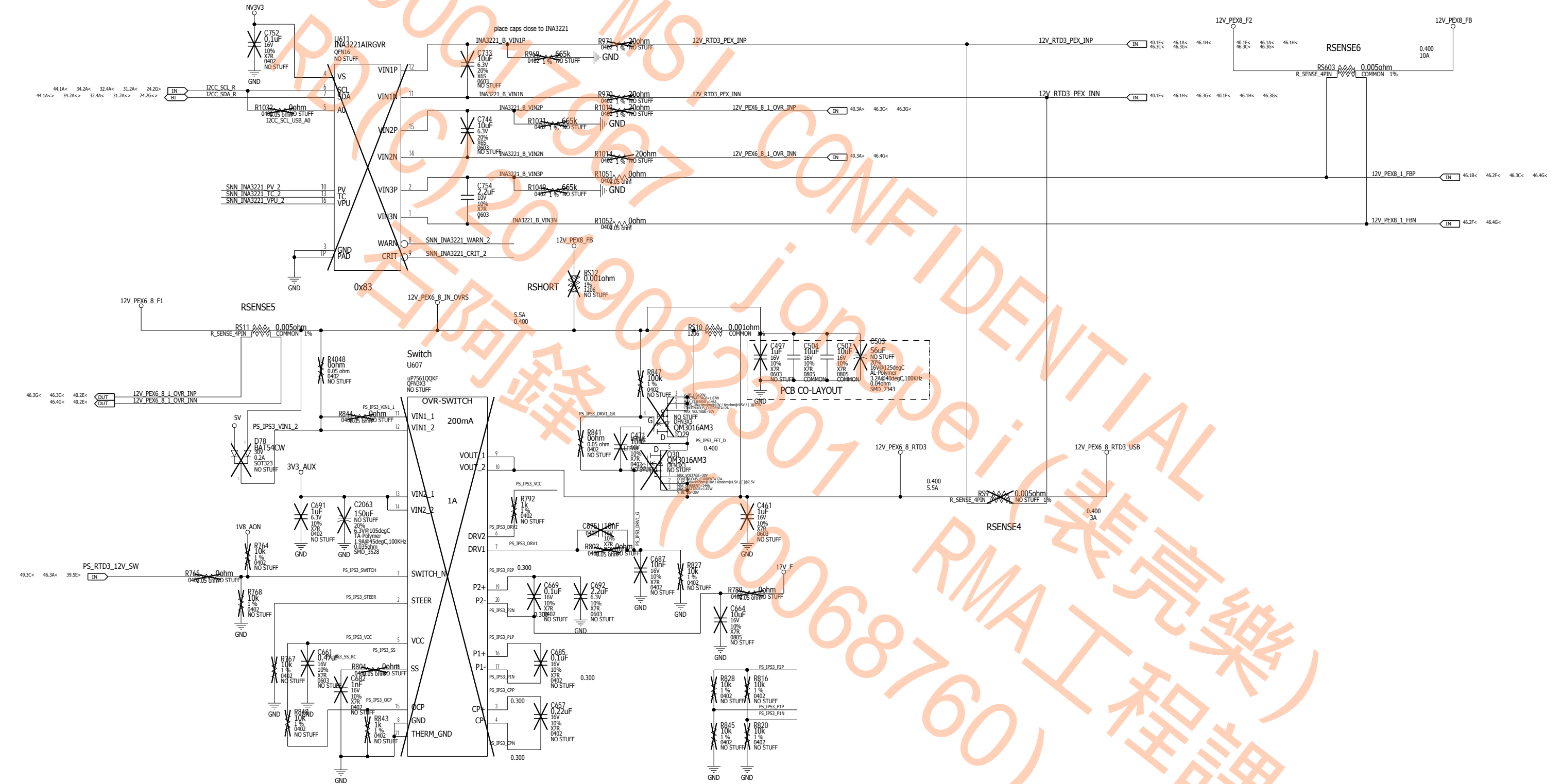


AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A




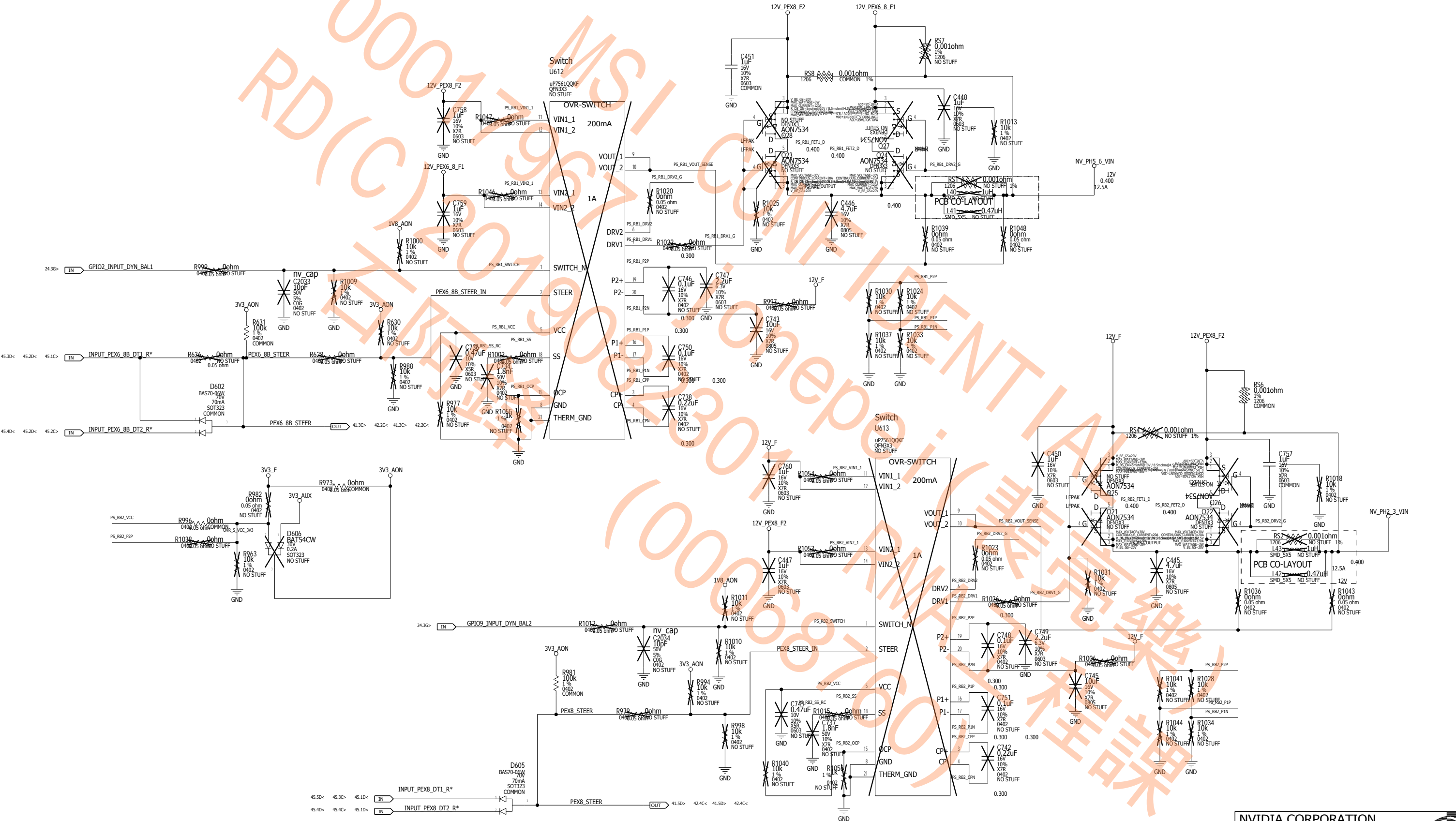
## PAGE 40: PS: INPUT SWITCH RTD3 USB



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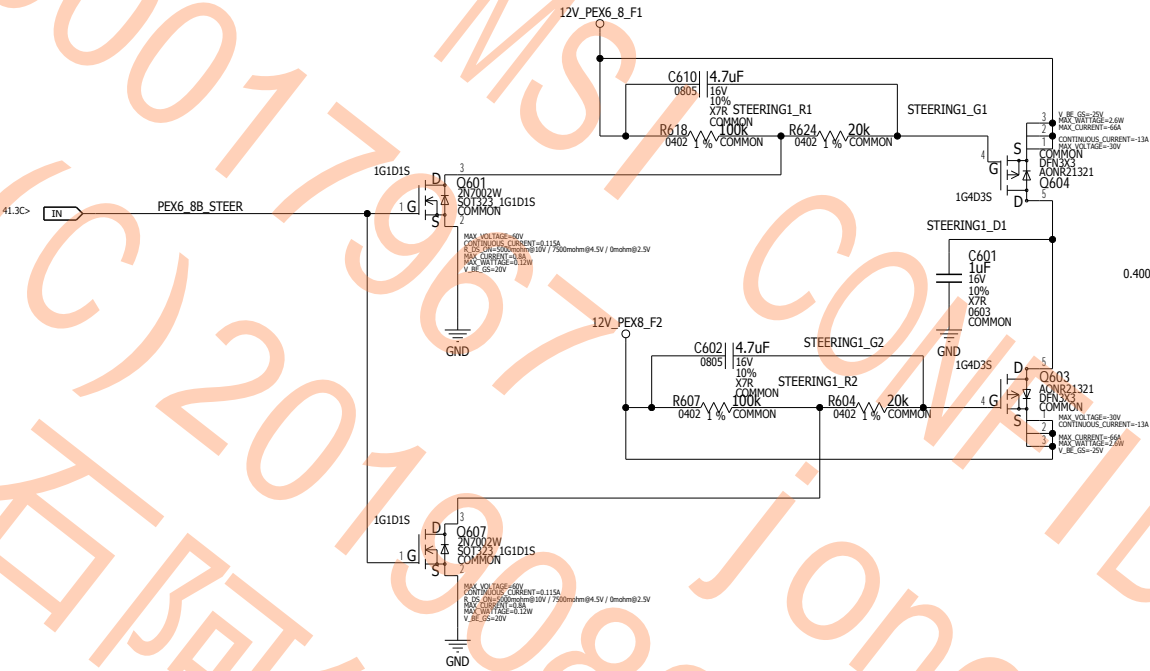
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: INPUT SWITCH RTD3 USB

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PCB REV	PG180-A03	PAGE	40 OF 54
BOM REV	A	DATE	06-FEB-2019

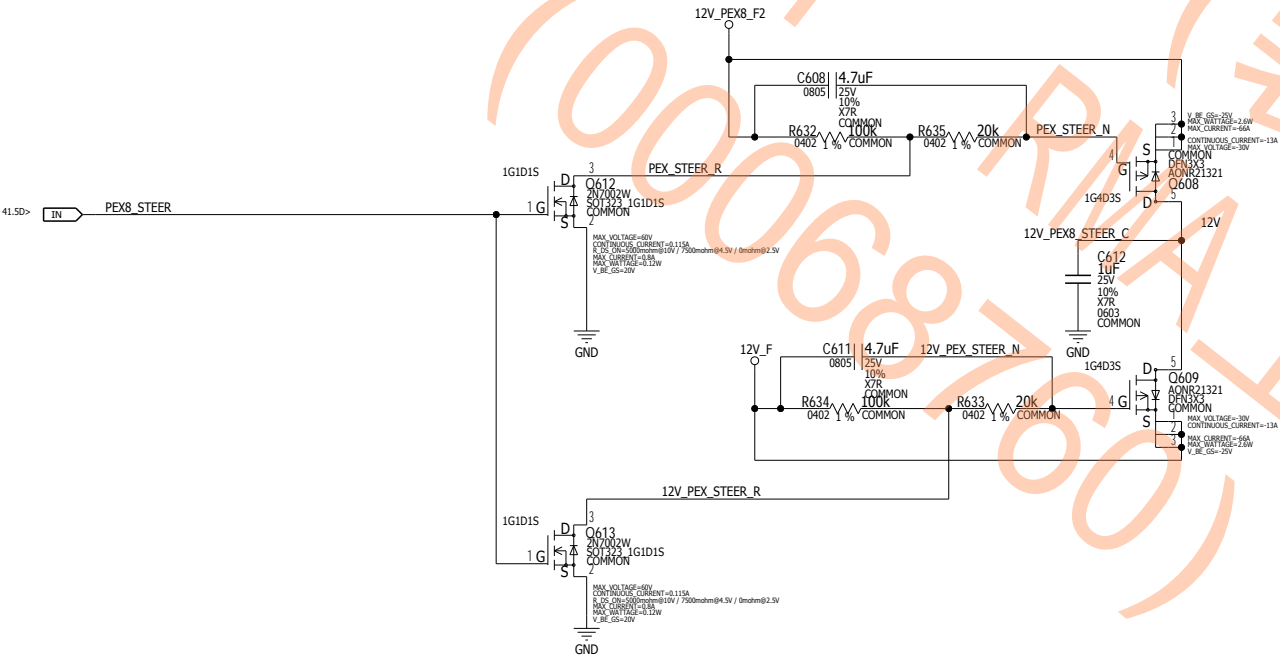




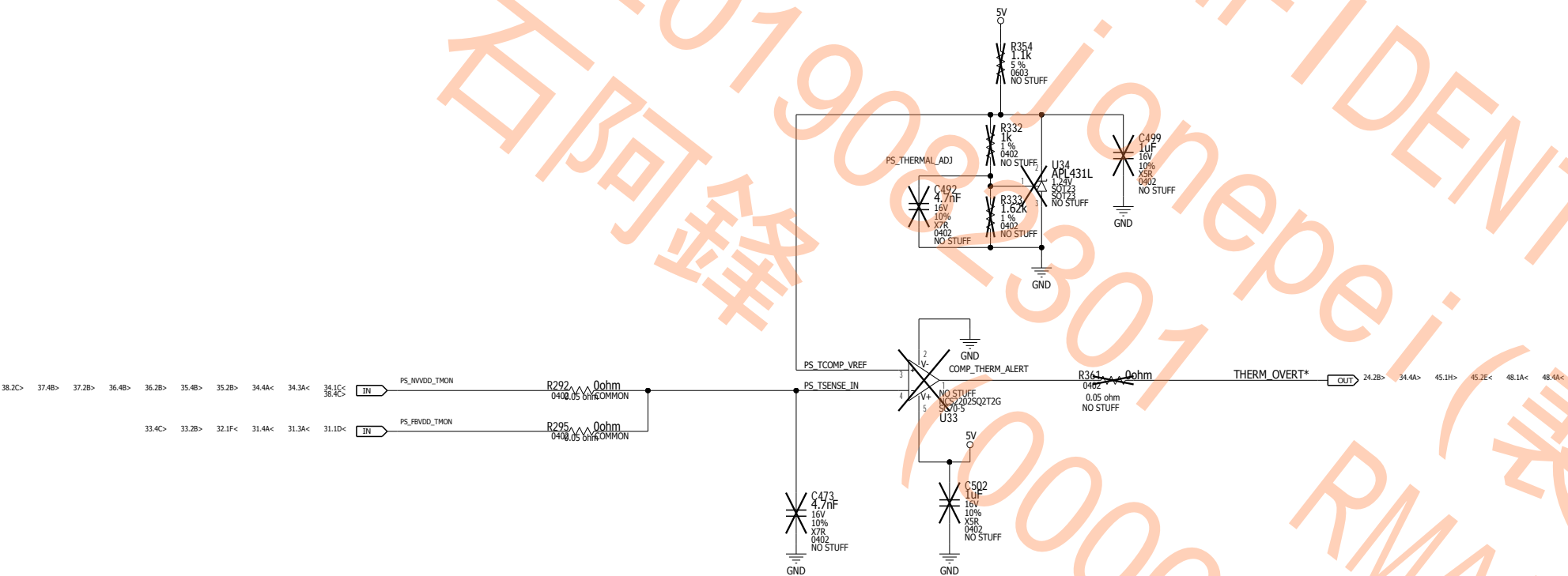
12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

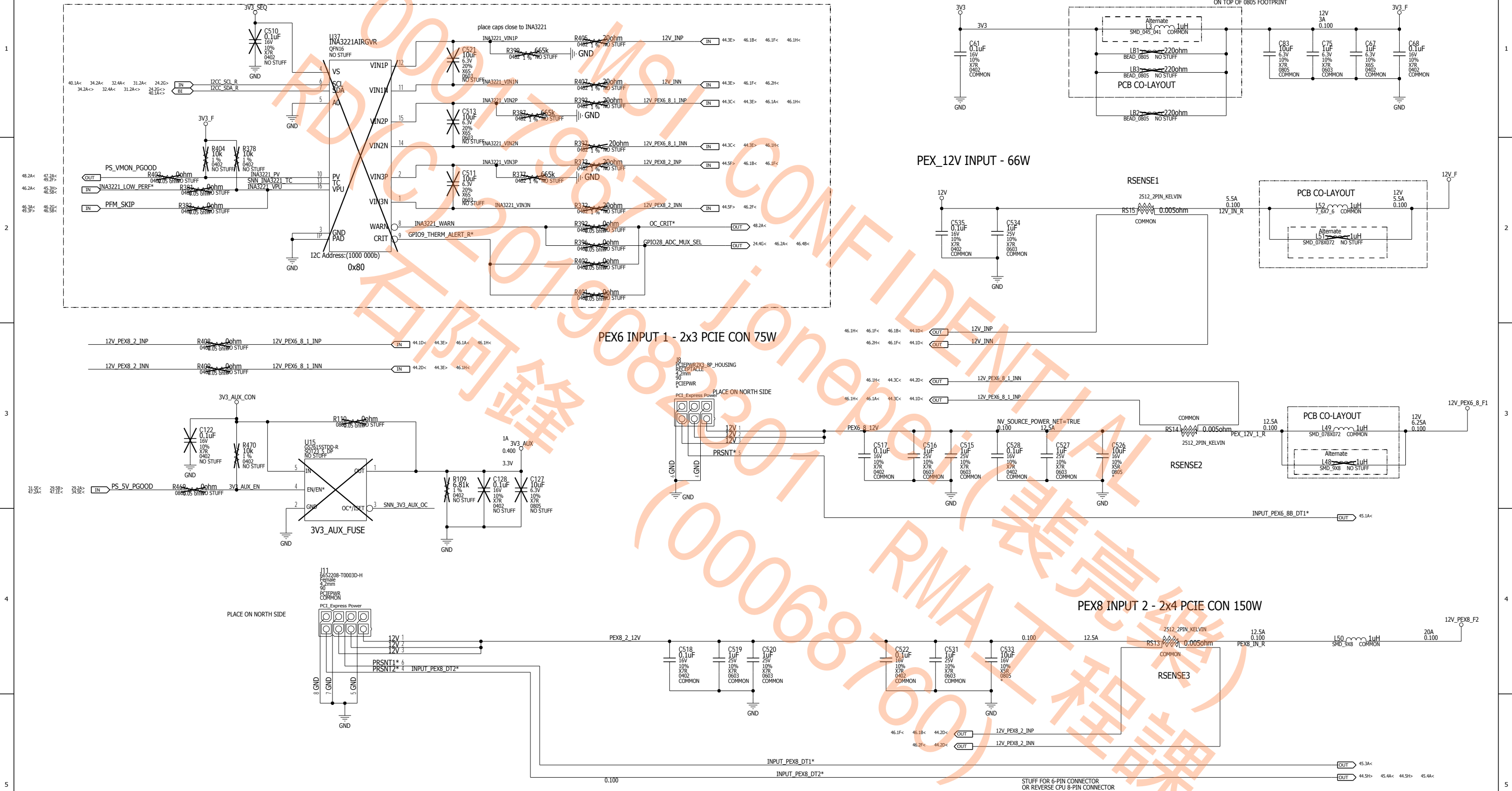


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PAGE 44: PS: Inputs, Filtering, and Monitoring



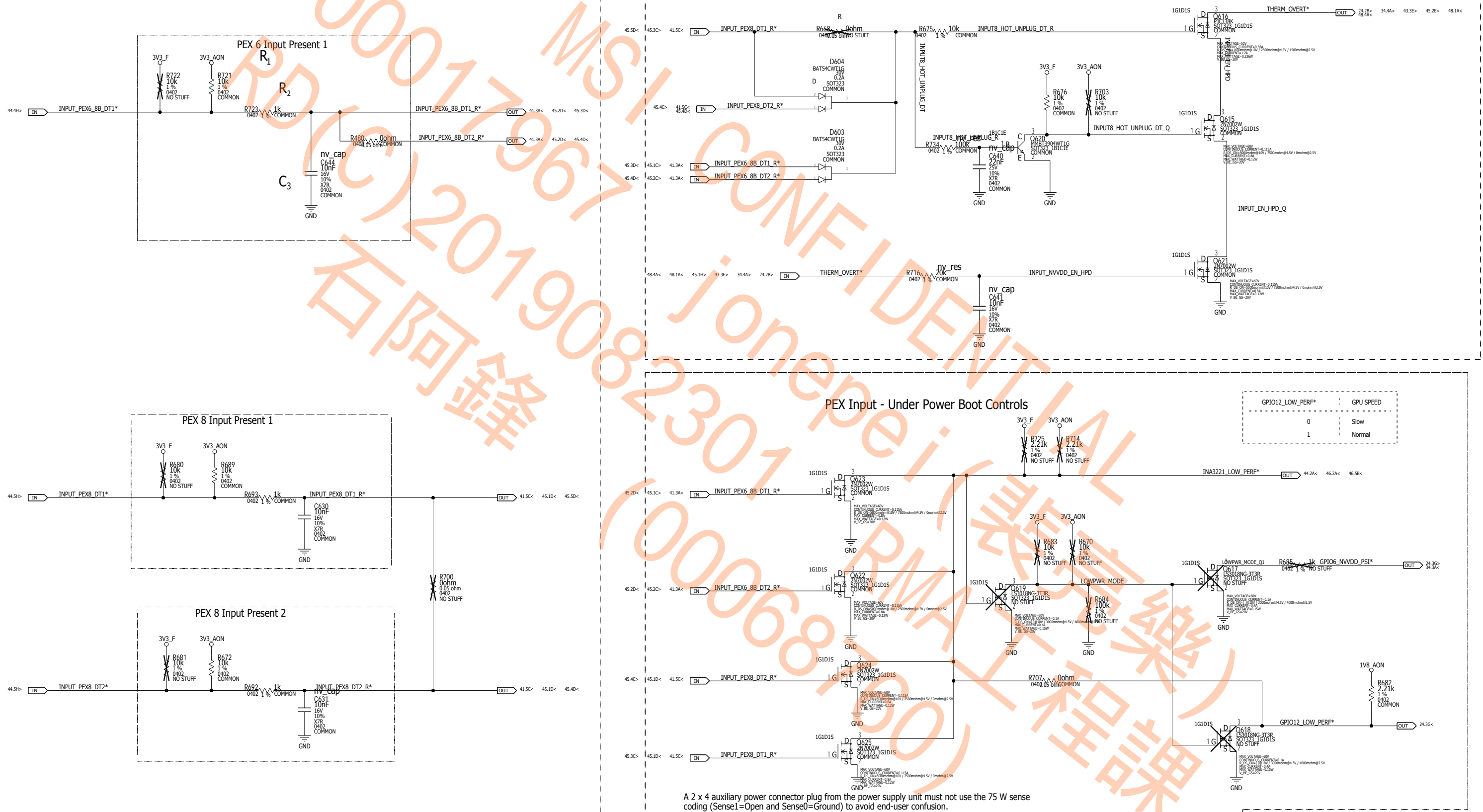
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: INPUTS, FILTERING AND MONITORING

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PCB REV	A180-A03	PAGE	44 OF 54
BOM REV	A	DATE	06-FEB-2019



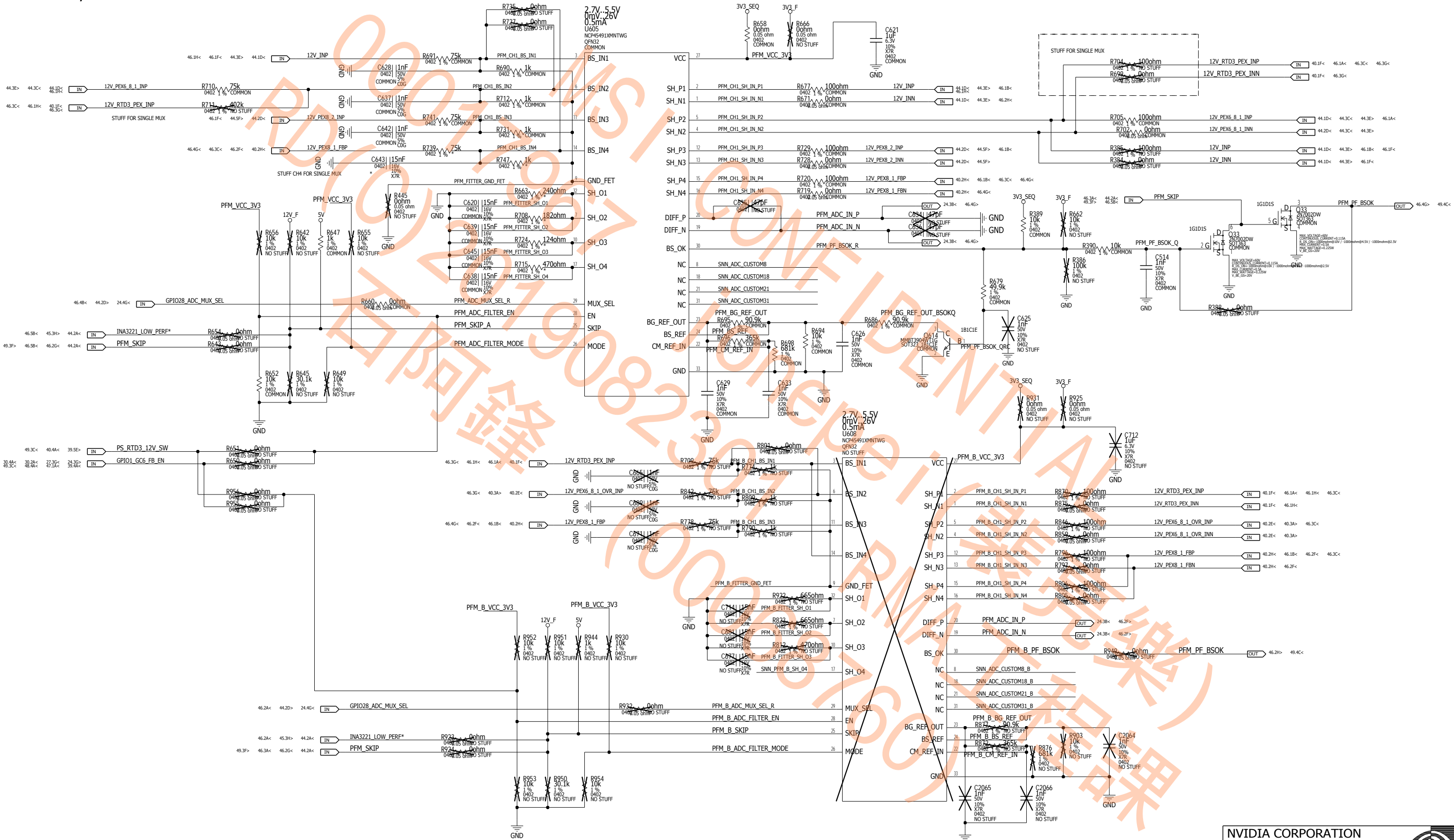
## PAGE 45: PS: Current Steering, Hot Unplug Detect

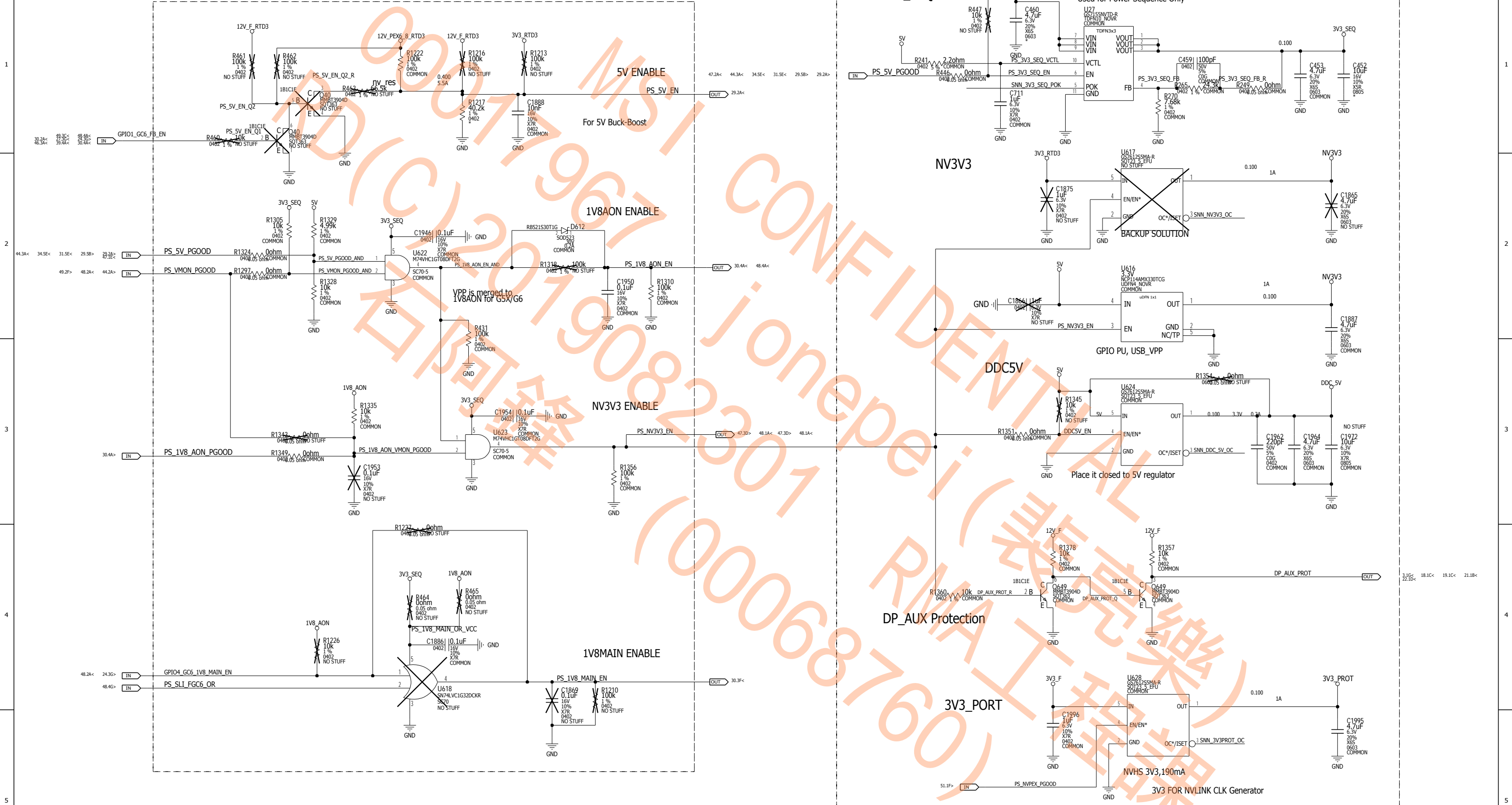


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PCB REV	PG180-A03	PAGE	45 OF 54
BOM REV	A	DATE	06-FEB-2019

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STUFF IF USING 2XMUX

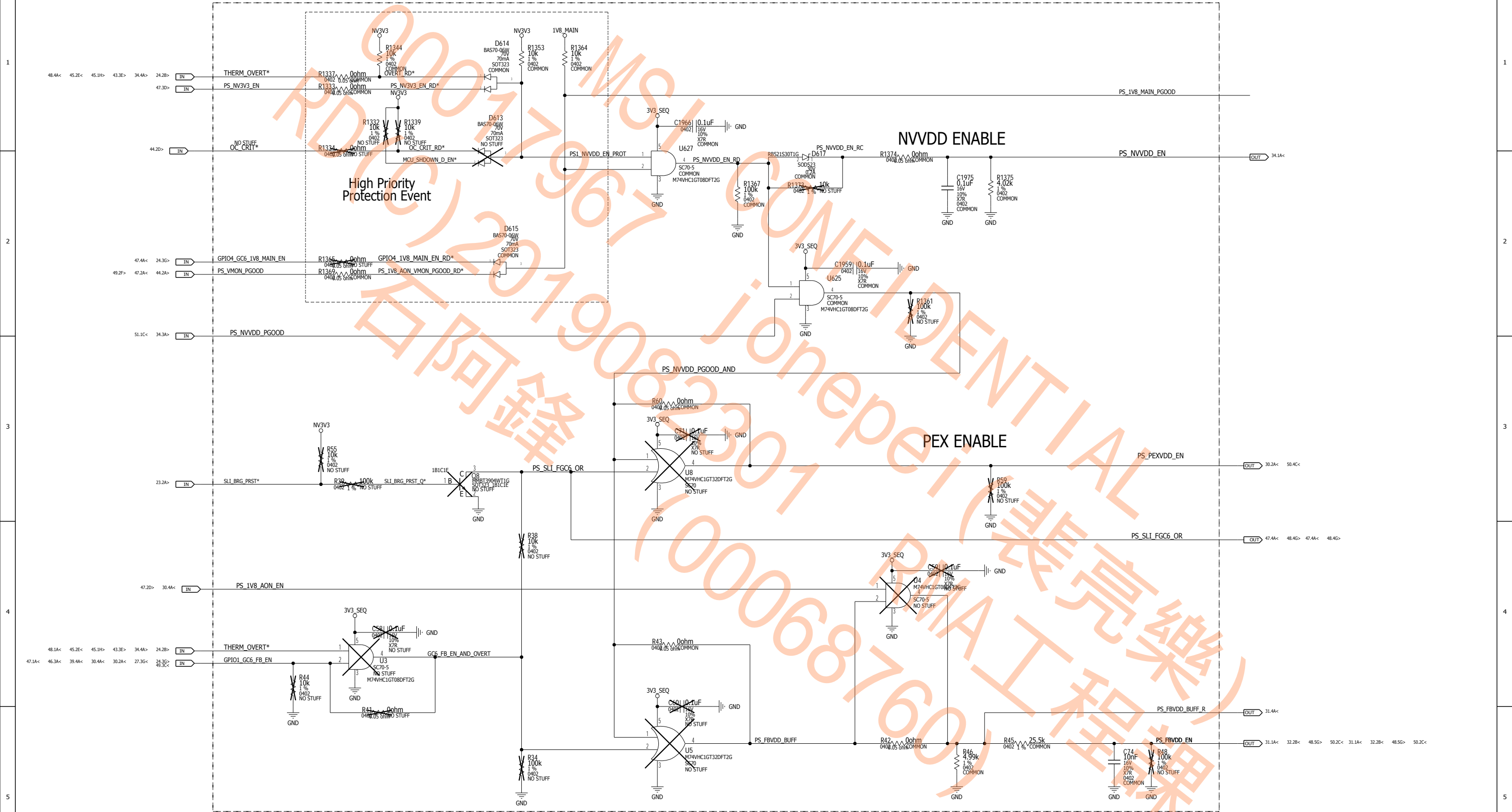




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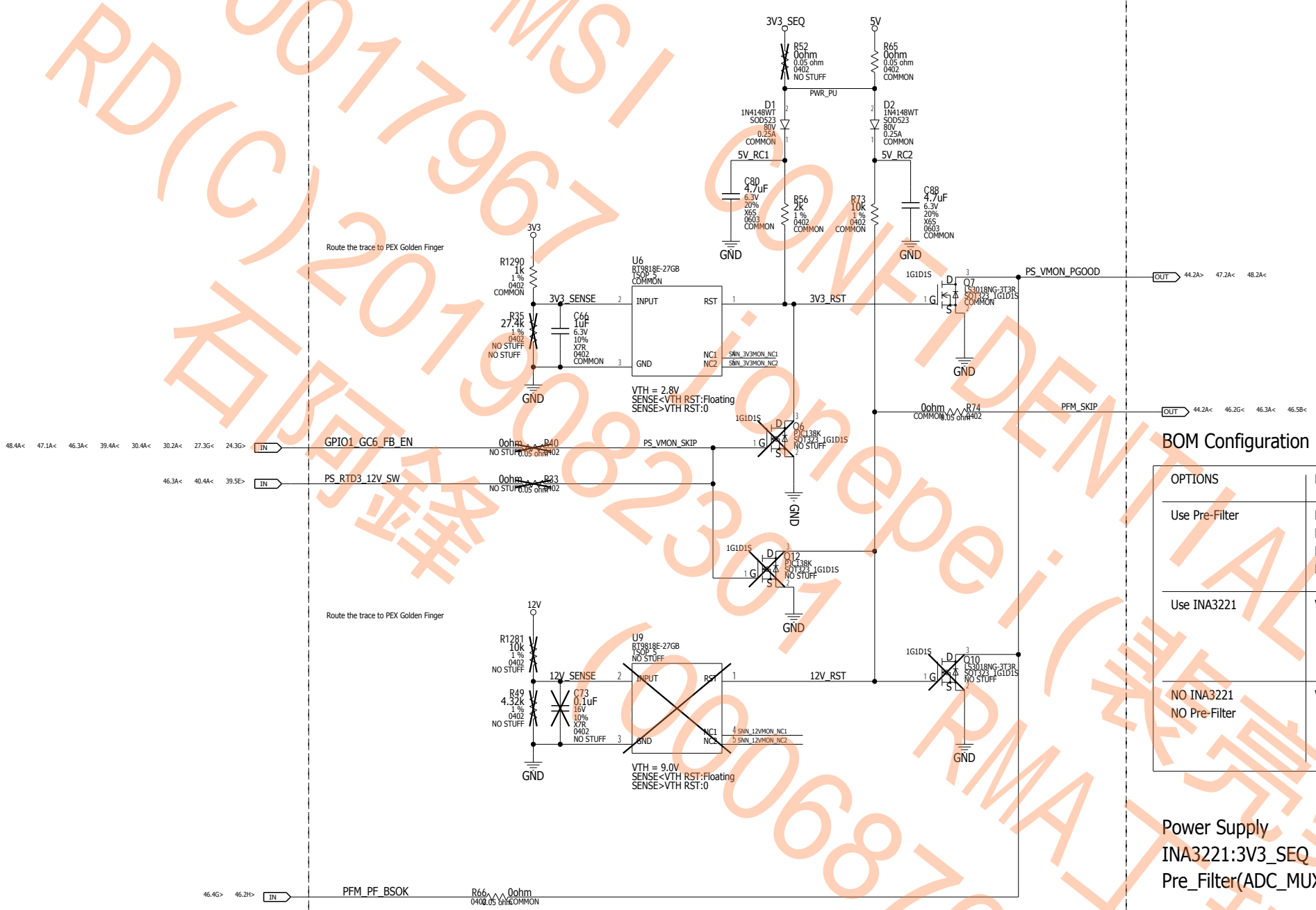


PAGE 48: SEQUENCE:NV,PEX,FB ENABLE



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PCIE Voltage Monitor



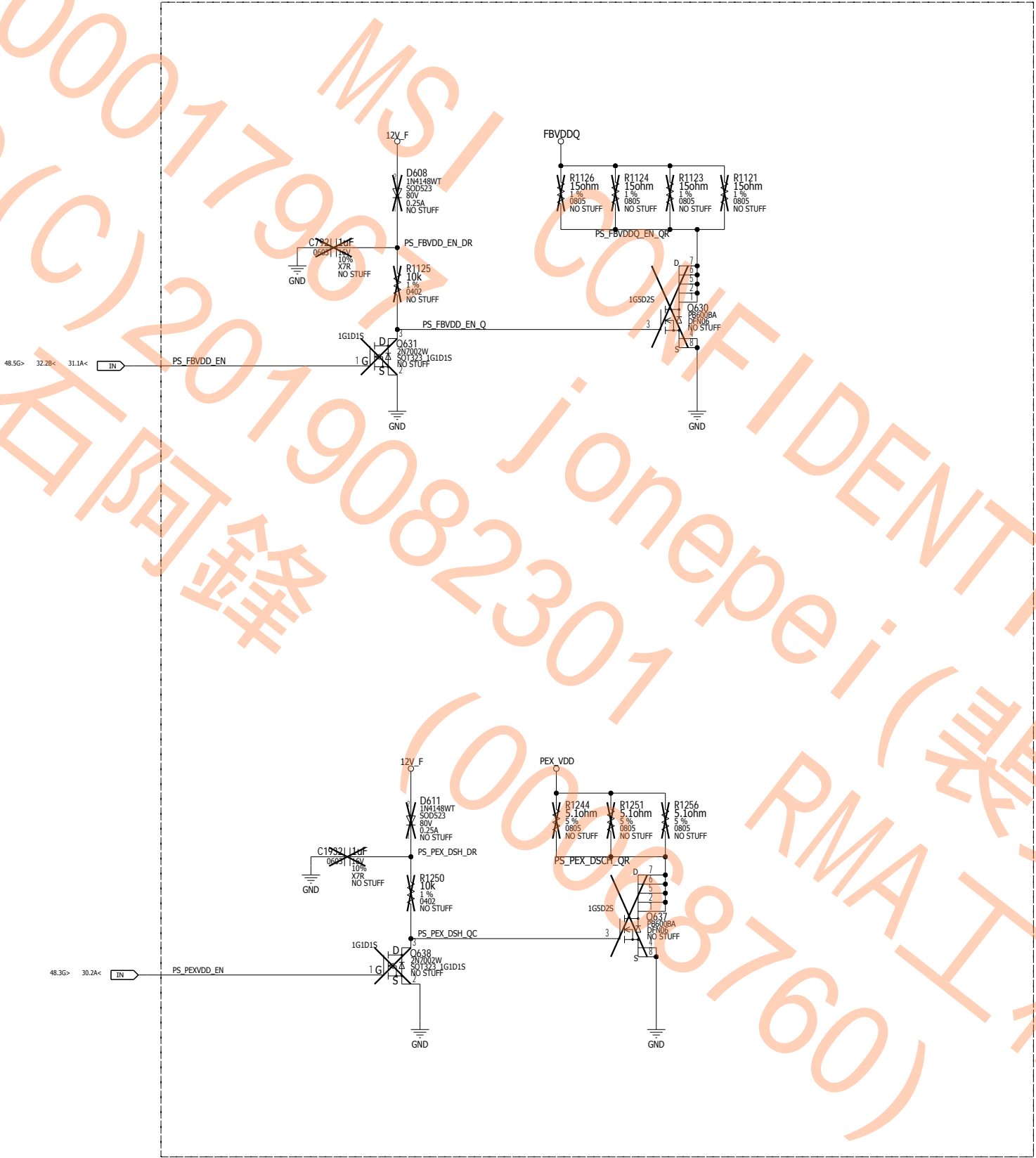
BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply  
INA3221:3V3\_SEQ  
Pre\_Filter(ADC\_MUX):3V3(PEX)

Dual Pre-Filter case:  
Only use the Primary Pre-Filter to sense 3V3PEX  
and All Input 12Vs

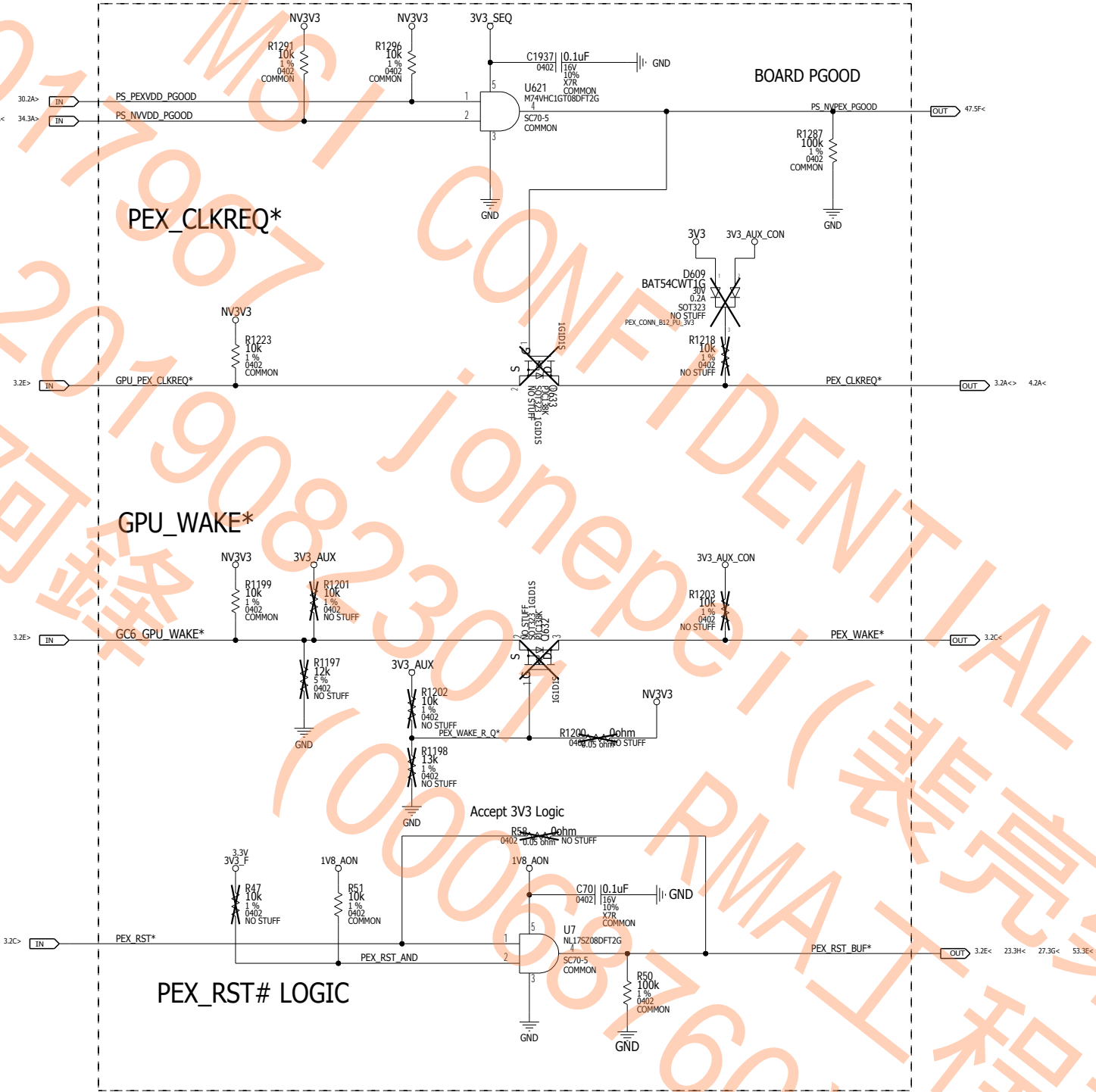
Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOX	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW



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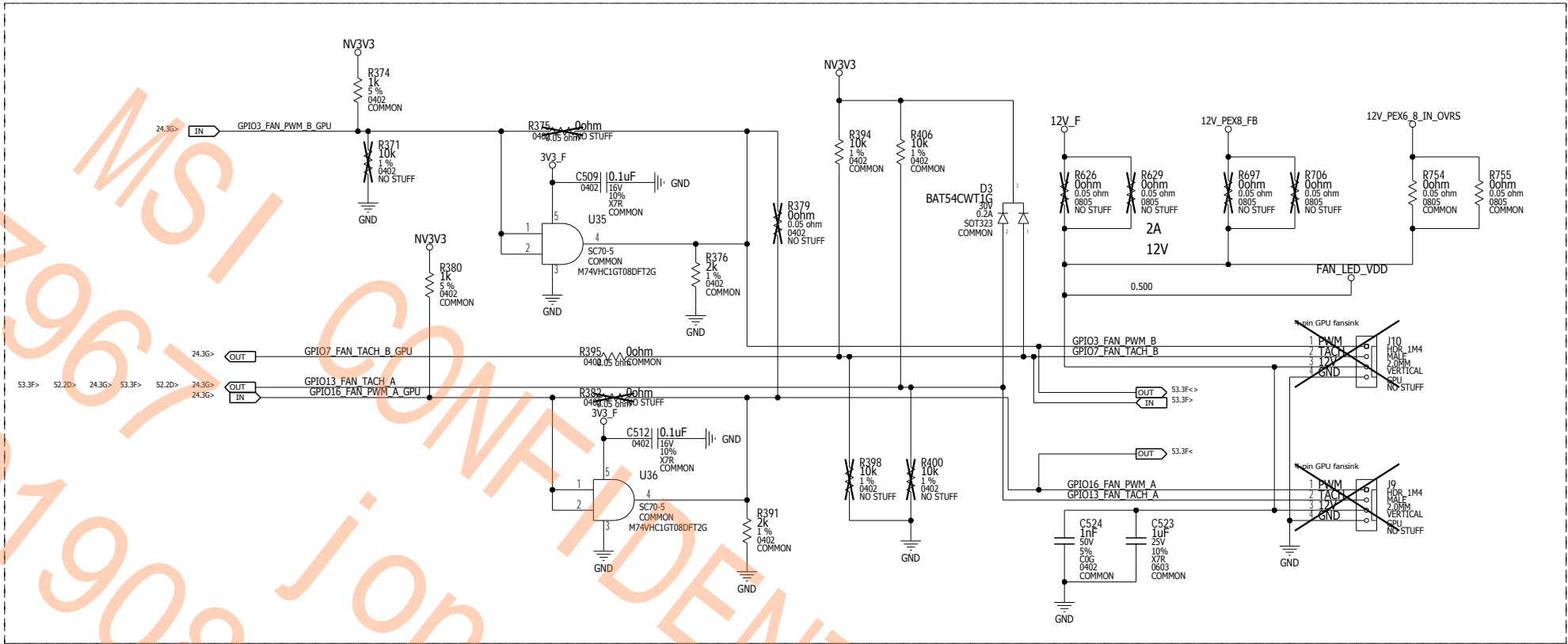
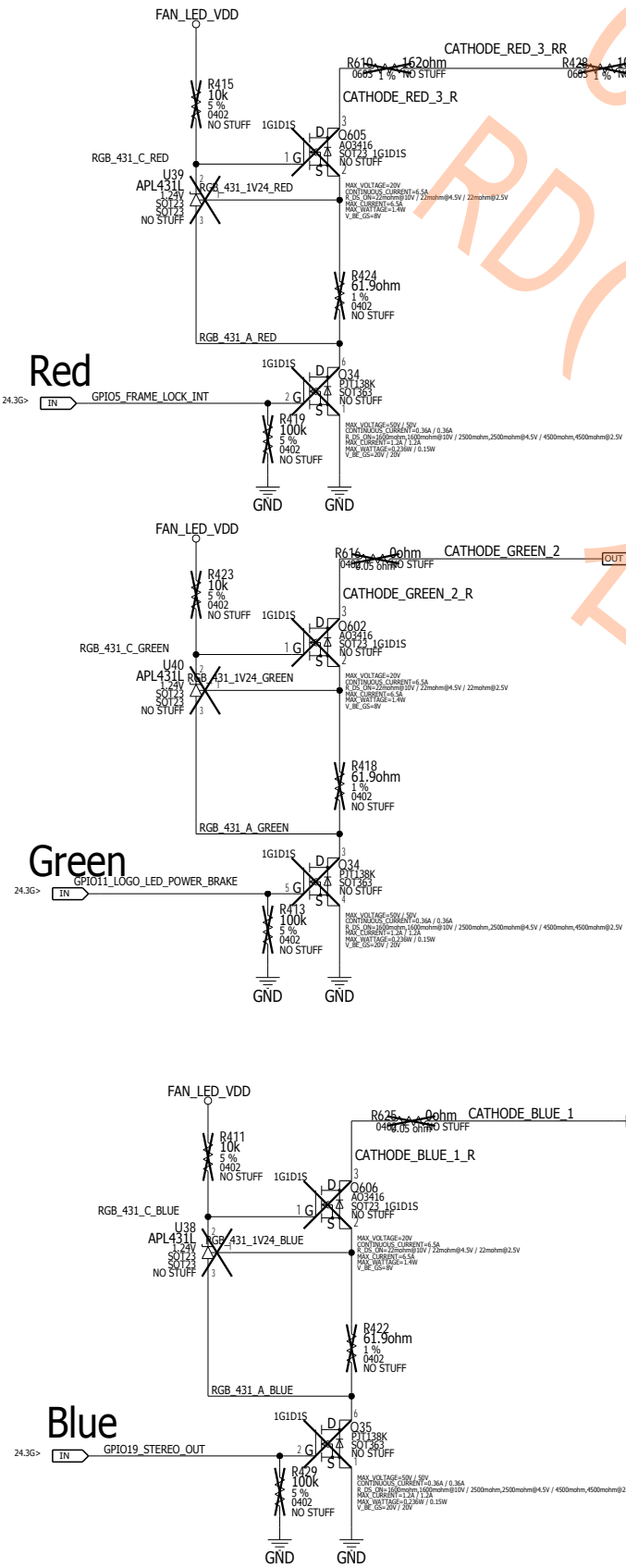
NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-1G180-0003-QS2		
PCB REV	PG180-A03	PAGE	50 OF 54
BOM REV	A	DATE	06-FEB-2019



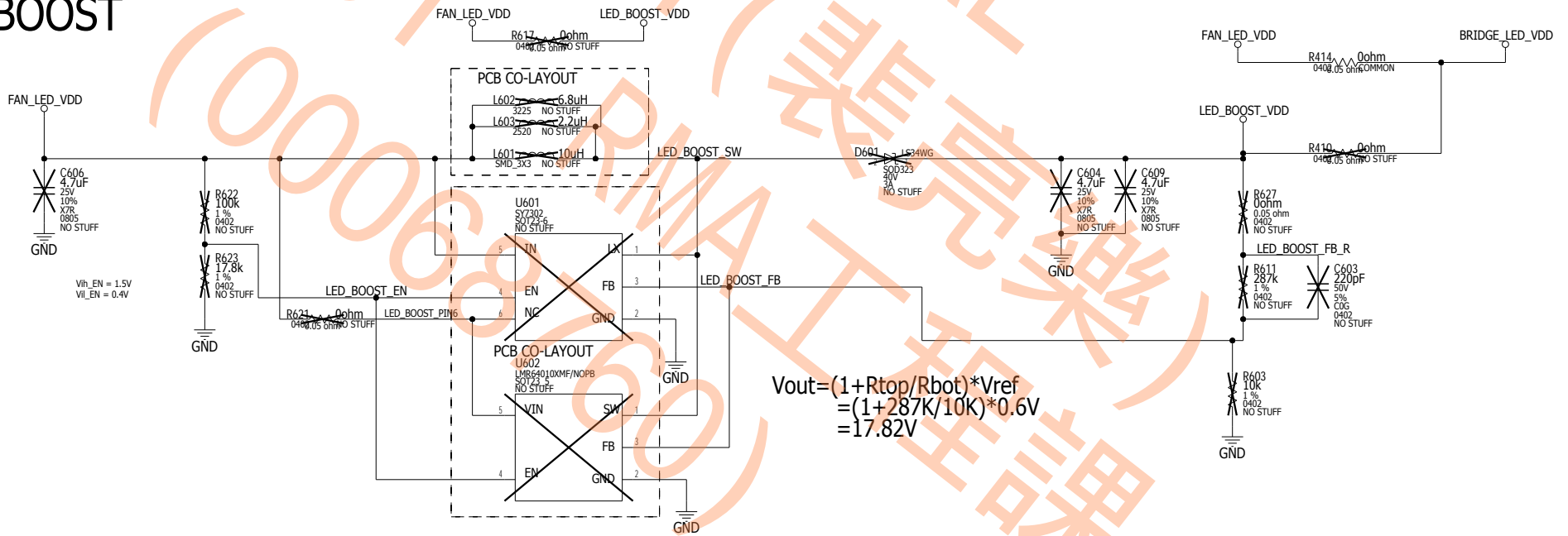


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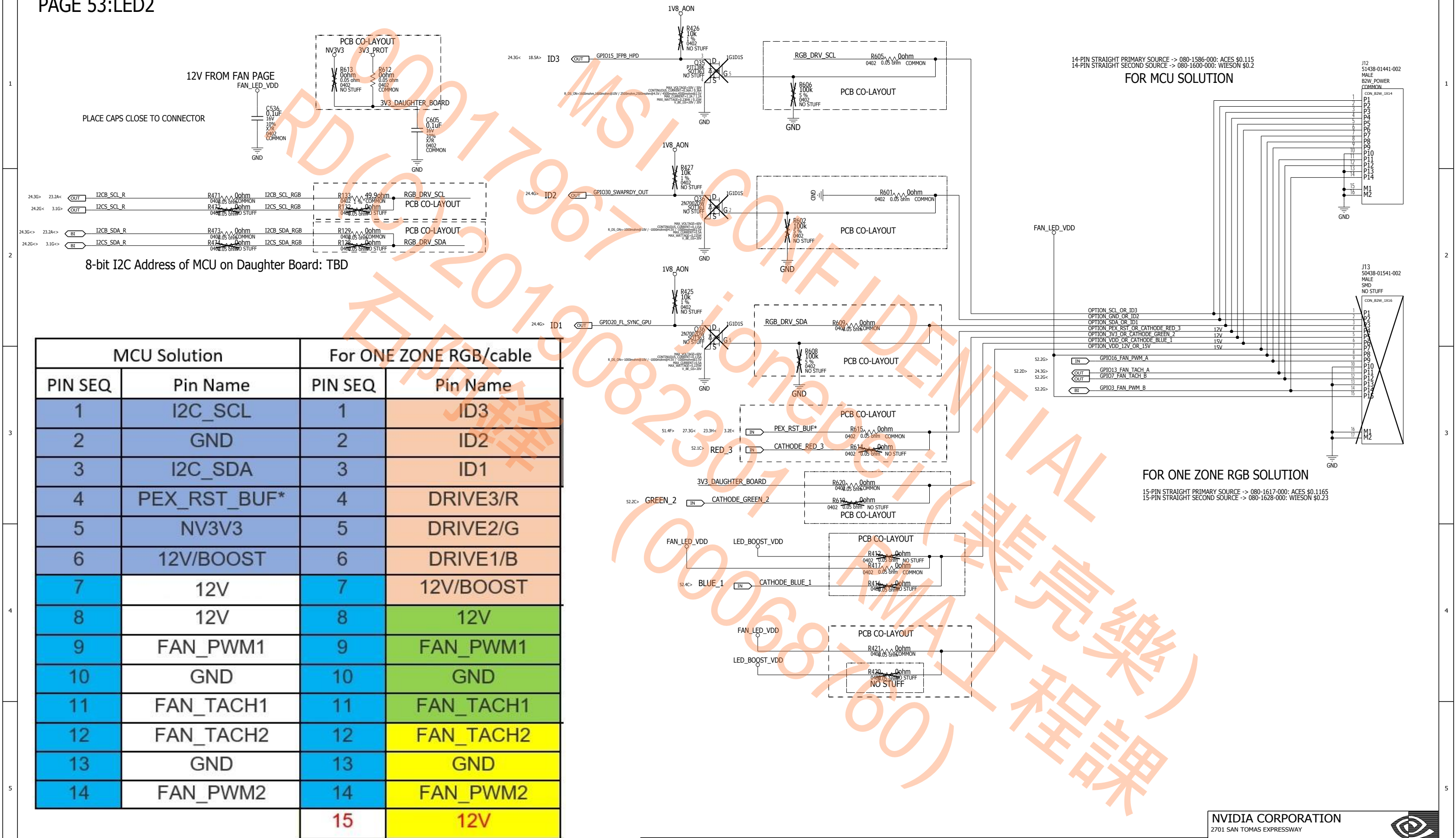
PAGE 52: LED & FAN HEADERS



LED BOOST

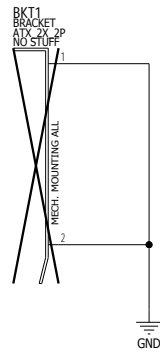


$$V_{out} = (1 + R_{top}/R_{bot}) * V_{ref} = (1 + 287K/10K) * 0.6V = 17.82V$$

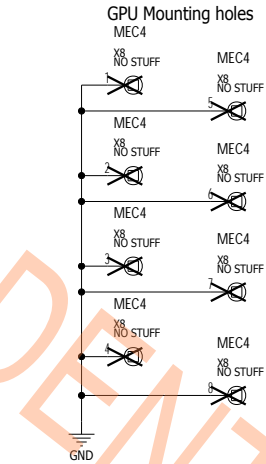
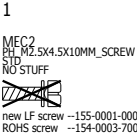




Brackets:

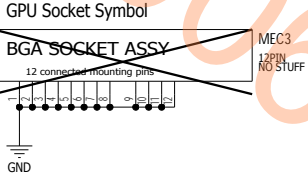
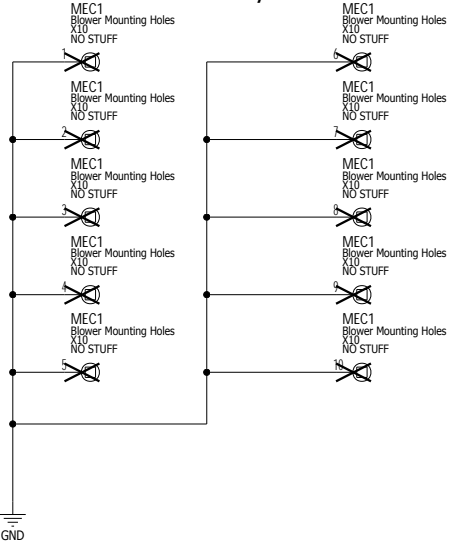


Bracket Screw



STIFFENER

Mechanical Holes Symbol



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