P262: NV44/G3-64, TSOP MEMORY x16

Page1: P262 Overview

Page2: PCI Express Interface Page3: Frame Buffer Interface Page4: Memory 1st bank 0..31 Page5: Memory 1st bank 32..63

Page6: DACA, DACB, DACC, Sync Buffers

Page7: VGA Output, TV Out Page8: TMDS Interface

Page9: MIOA, MIOB Interface, LPC-ROM

Page10: STRAPS, Mechanical Parts Pagel1: XTAL, GPIO, BIOS, Fan Control, JTAG Headers

Page12: VIDEO CAPTURE: SAA7115

Page13: PowerSupplyI: NVVDD, FBVDDQ

Page14: PowerSupplyII: 5V, DDC5V, A3V3, F3V3, TMDS_PLLVDD

Page15: VIDEO CONNECTORS: MiniDIN, 2x6 HDR

Page16: PowerSupplyIII: 5V, F3V3 (Optional for higher current)

SKU	VARIANT	NVPN	ASSEMBLY
В	BASE	600-f0ppp-xxxx-vvv	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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REV HISTORY

A01

- 9/22/2004:

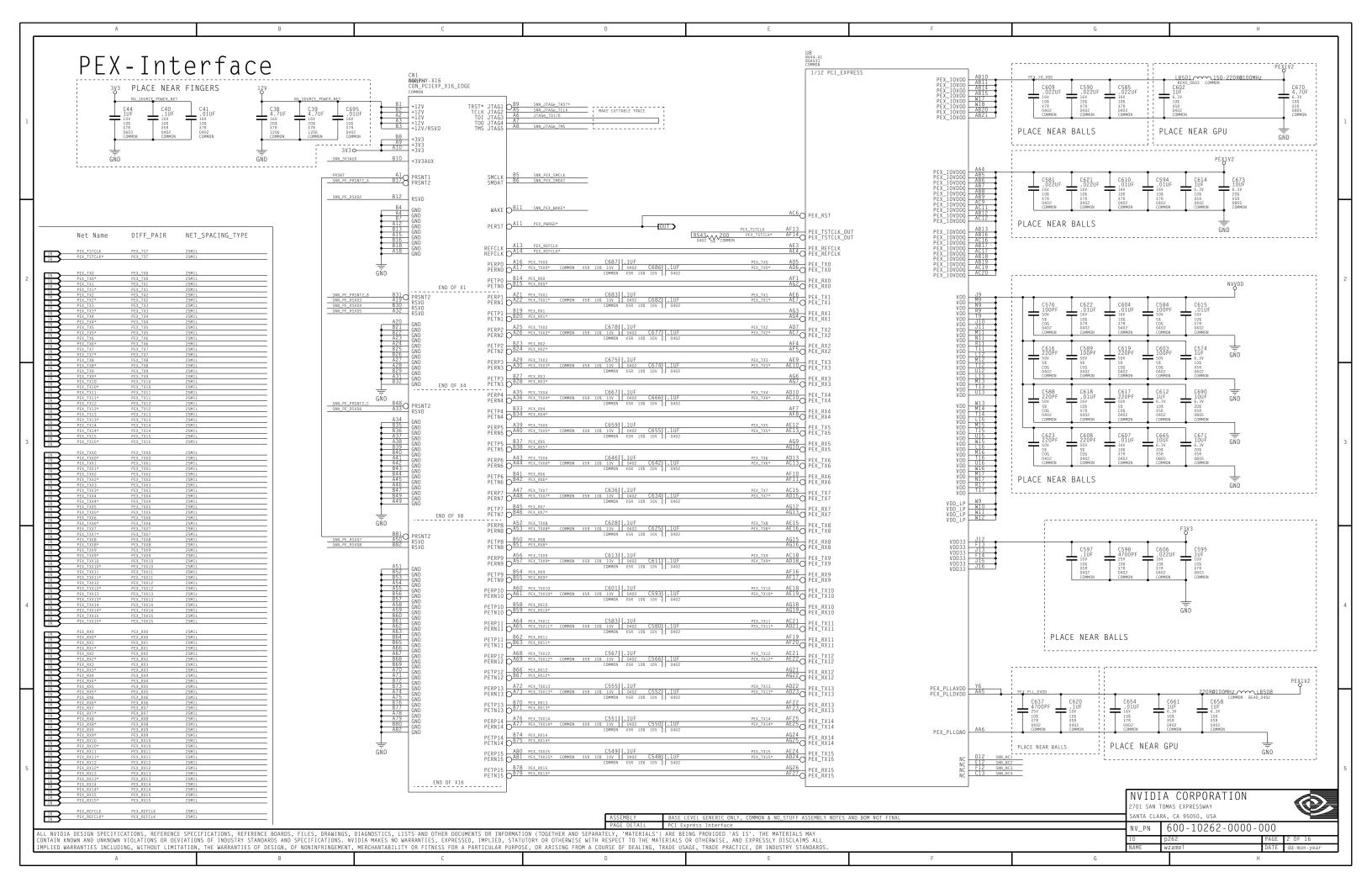
Changed TMDS_PLLVDD to PLLVDD Added bead option to PLLVDD rail of NV44 Changed RSET values for DACA and DACB Changed DACB RSET FET to a dual package with GPI011 control-Macrovision Added F3V3 bypass to PLLVDD linear regulator Changed location of R62

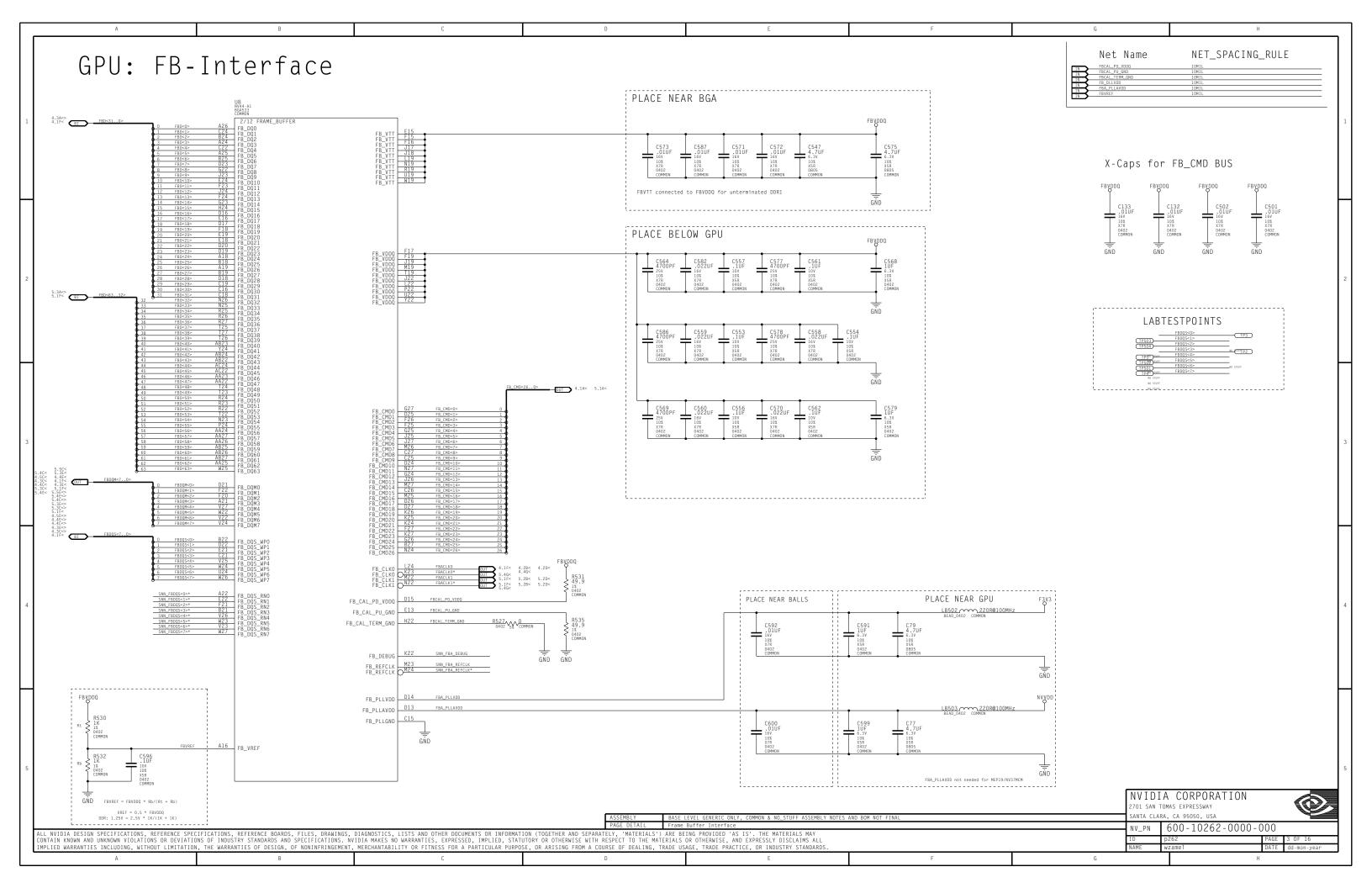
NVIDIA CORPORATION

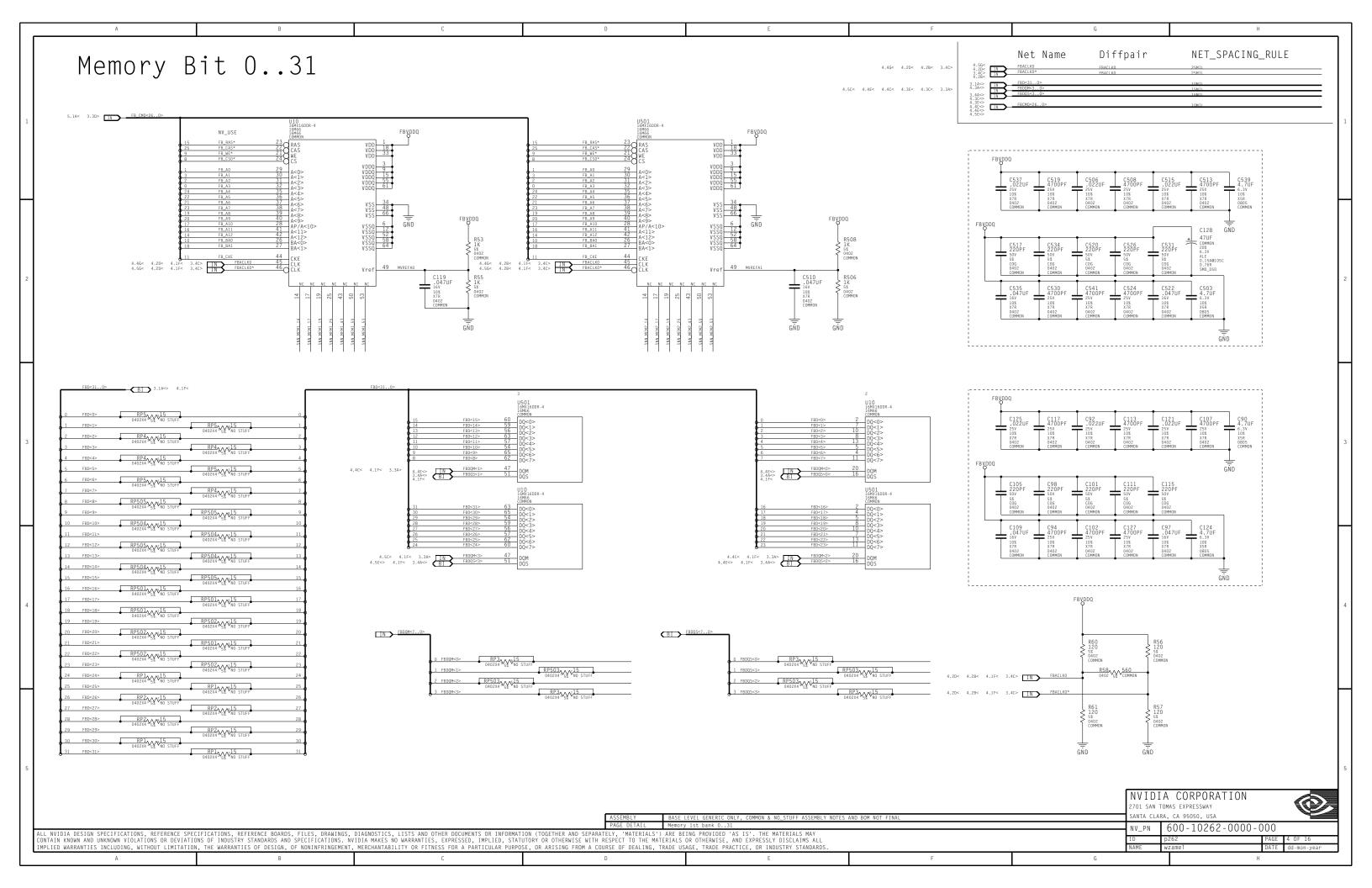
2701 SAN TOMAS EXPRESSWAY

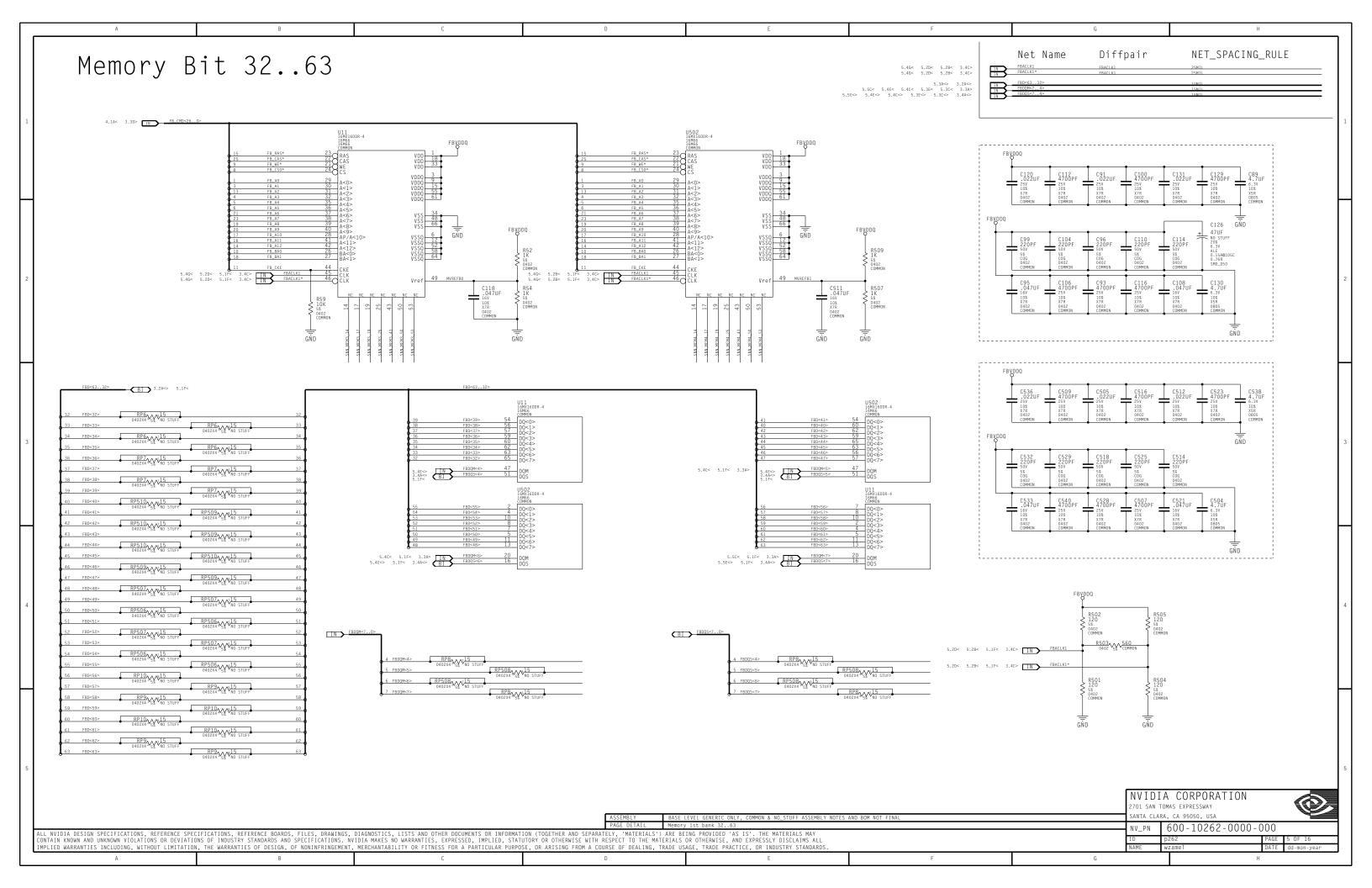
SANTA CLARA. CA 95050. USA 600-10262-0000-000

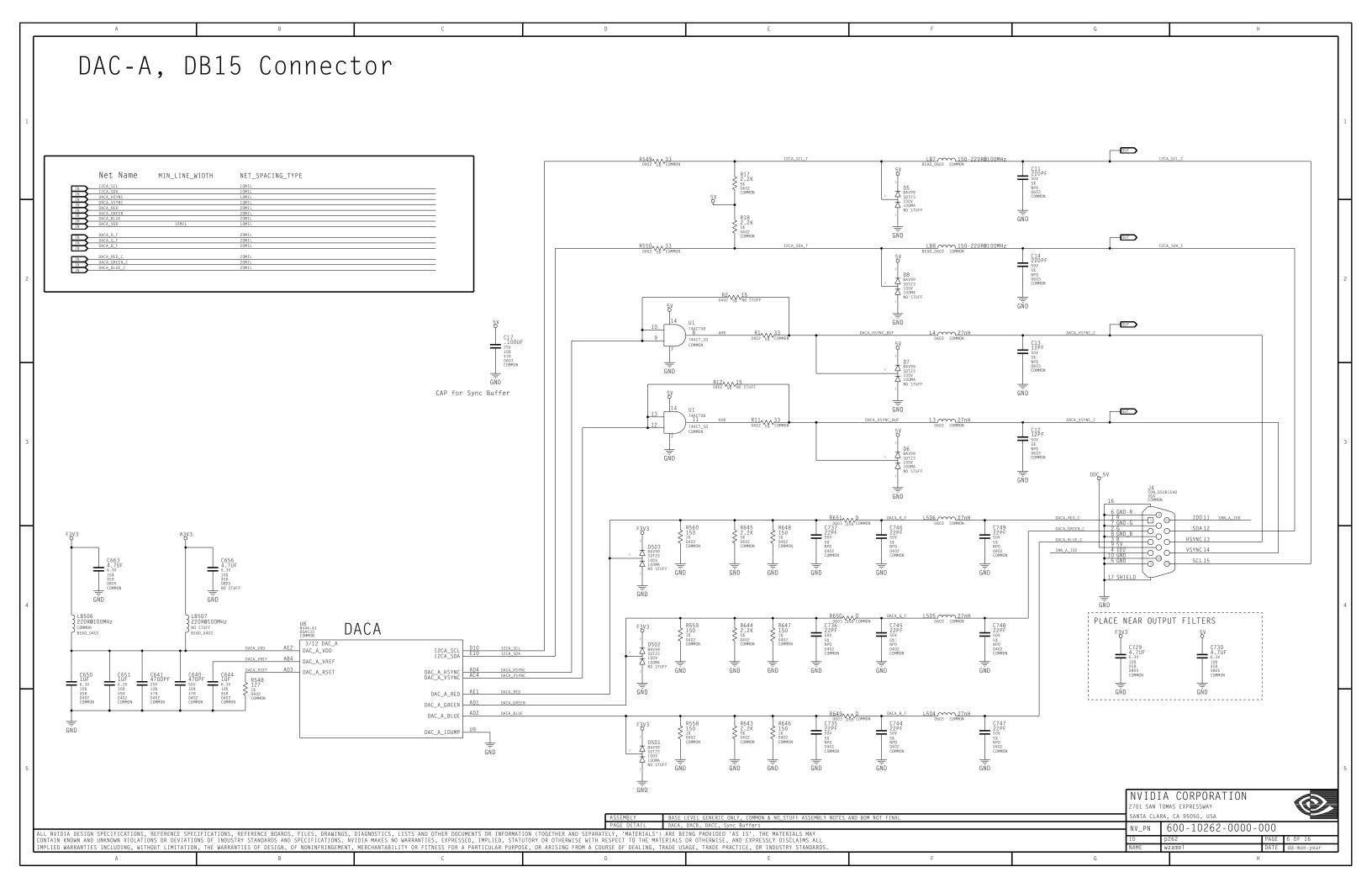
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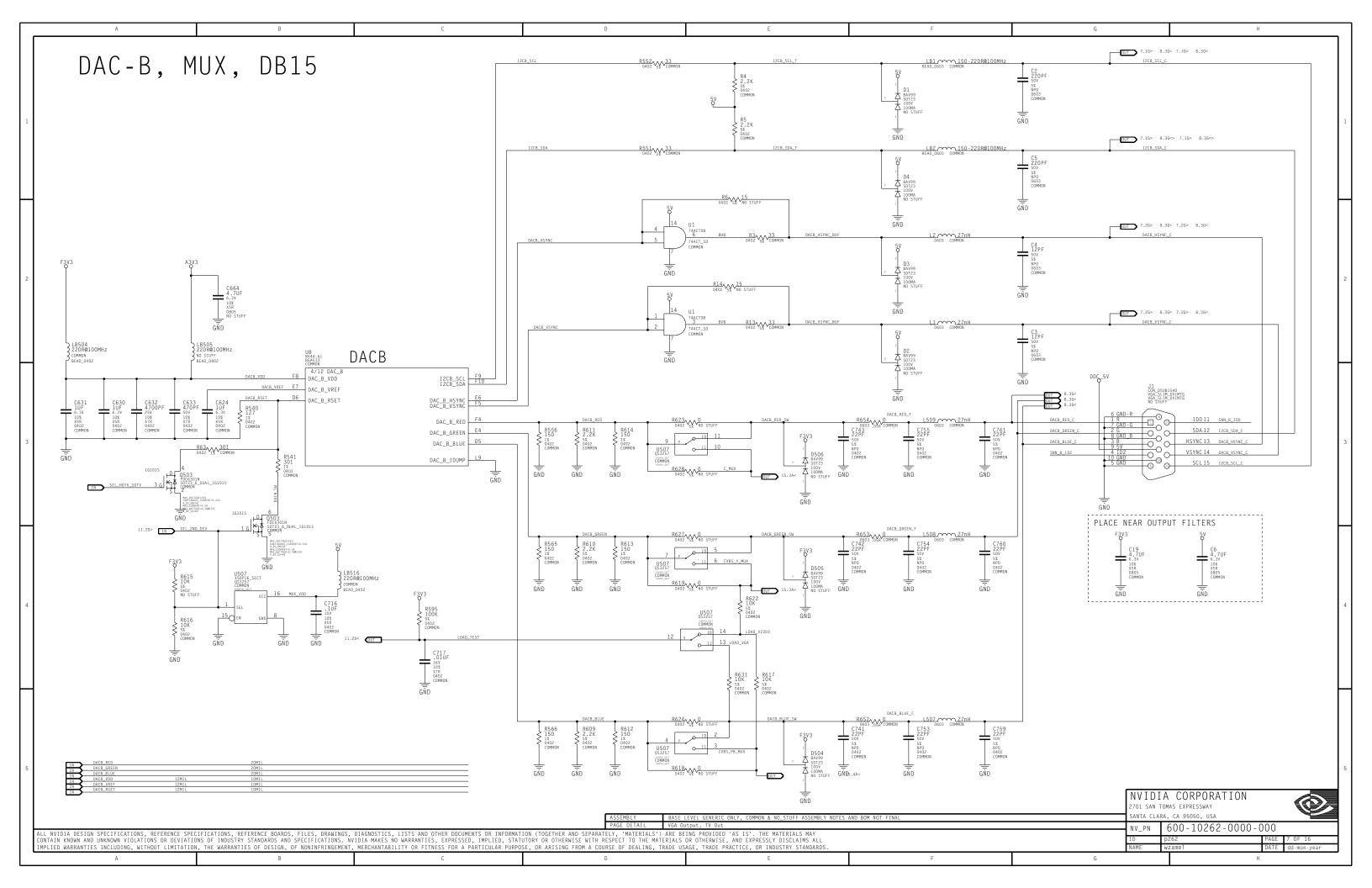


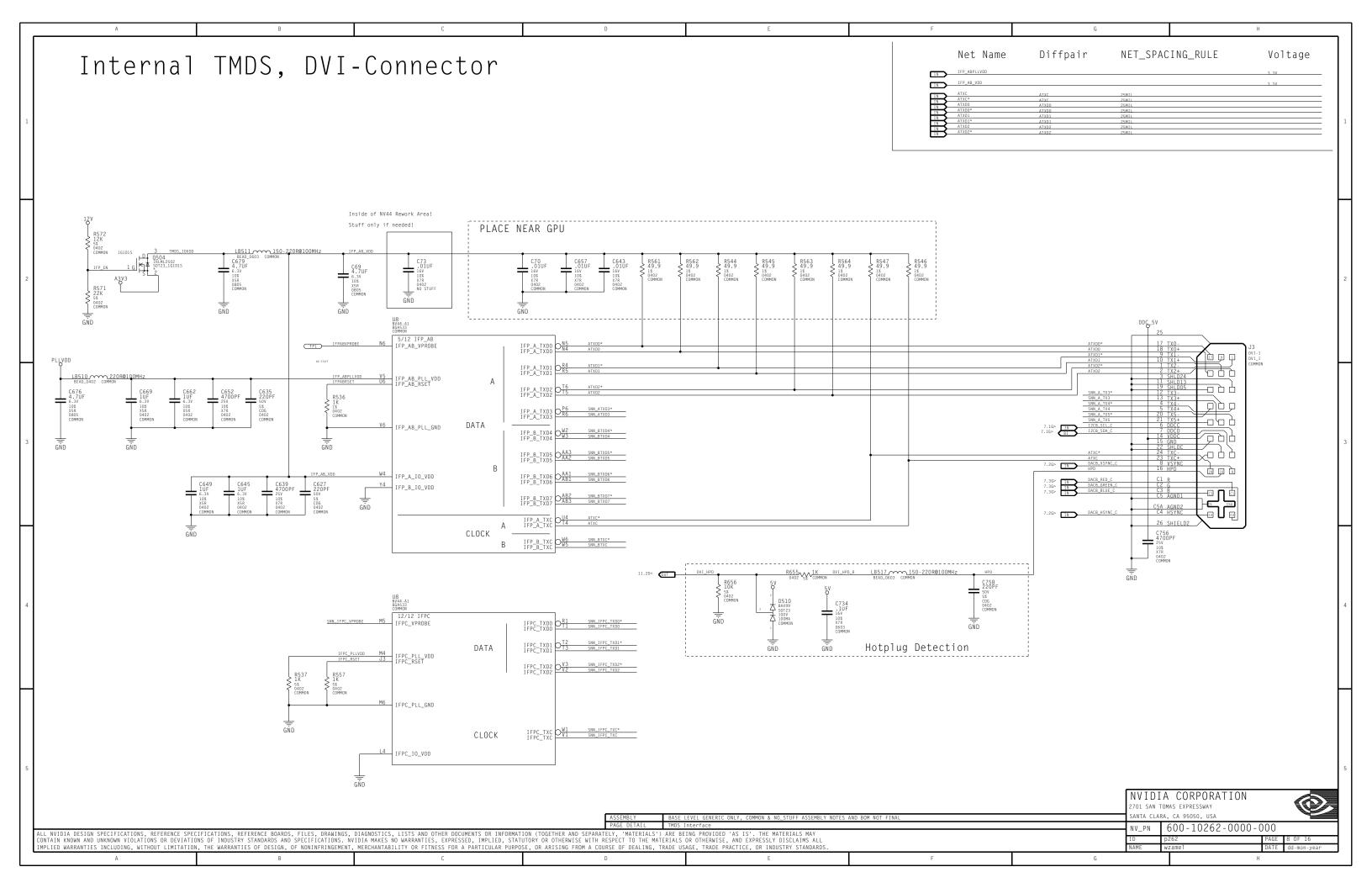


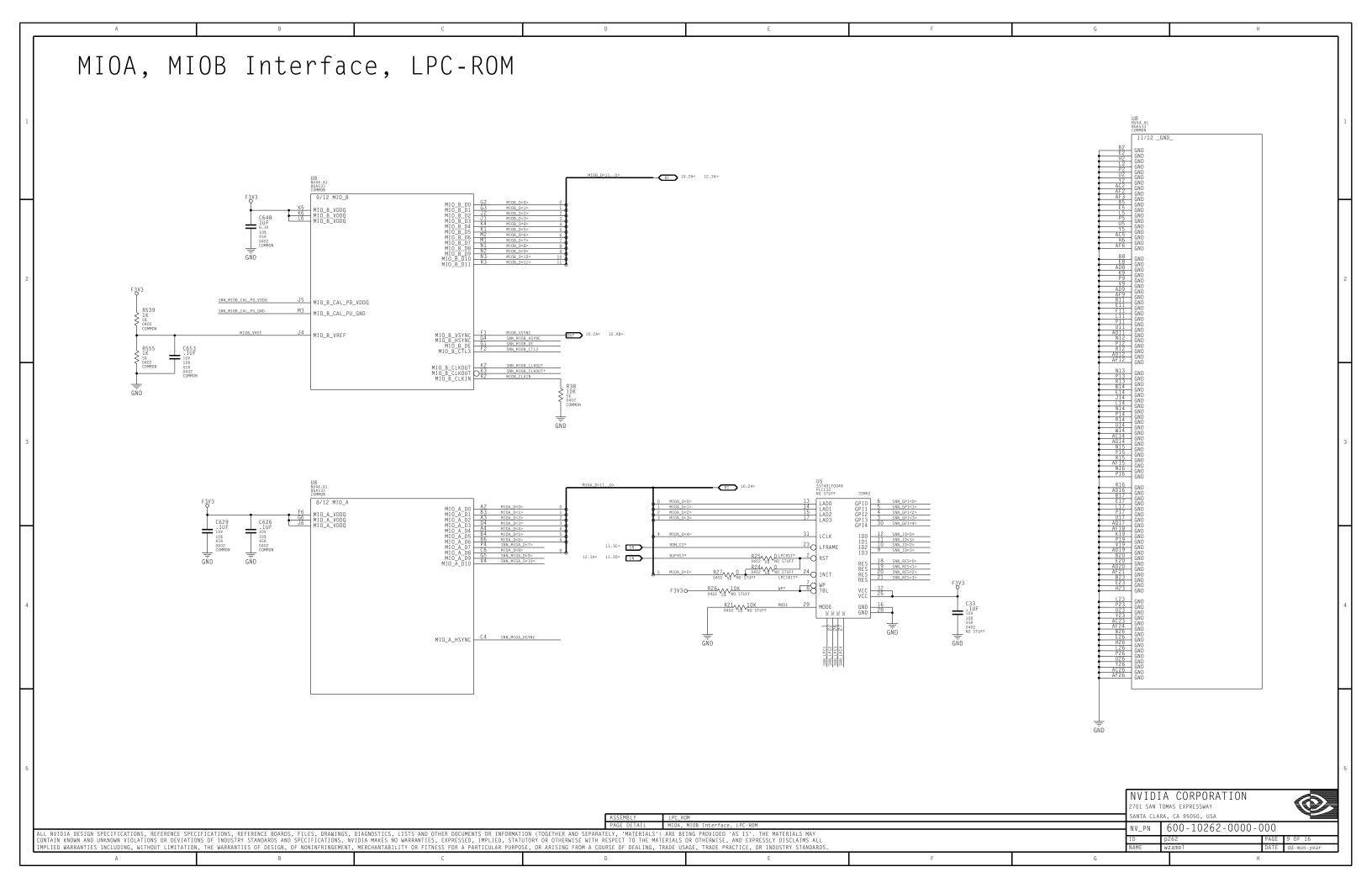


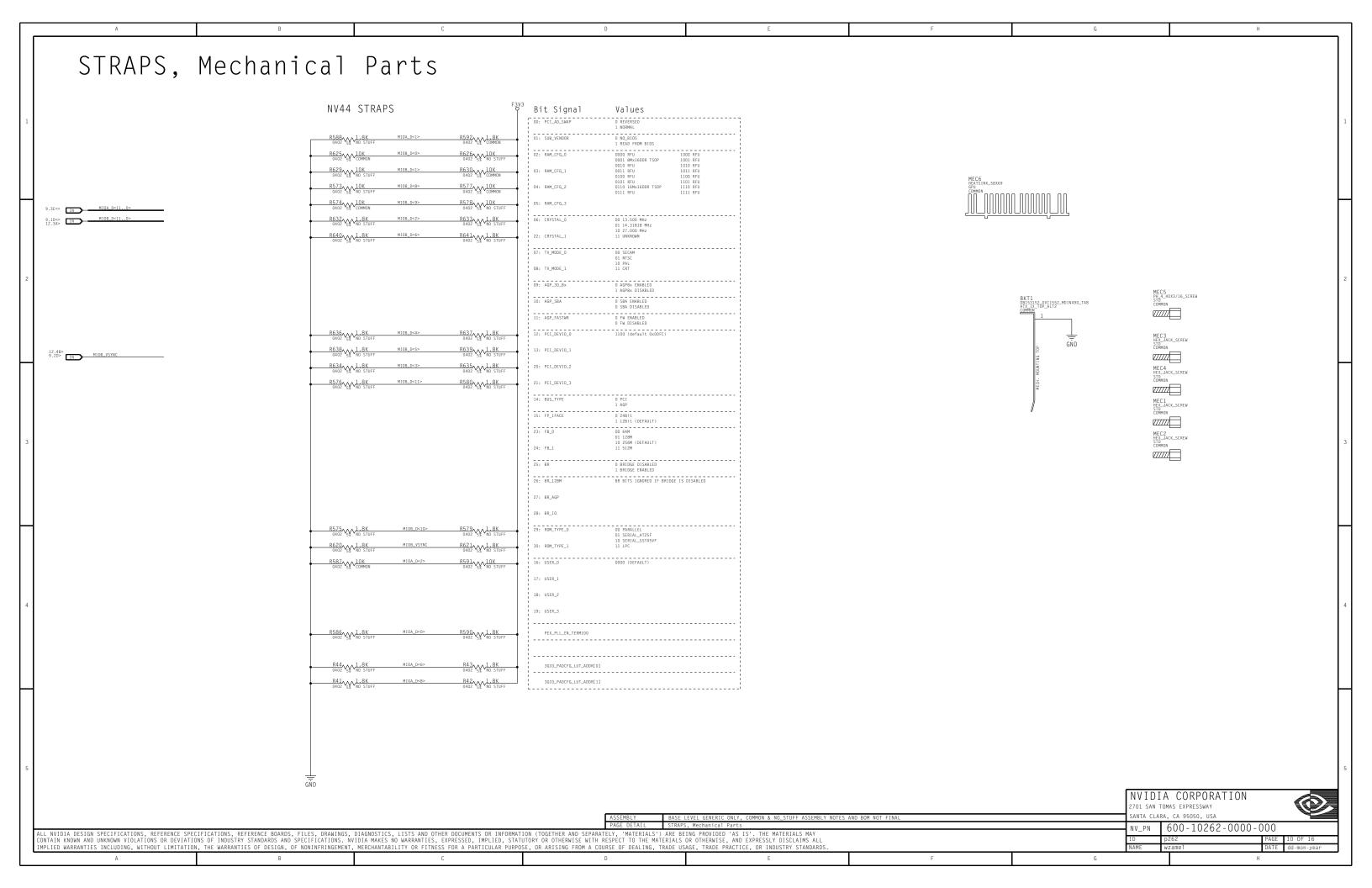


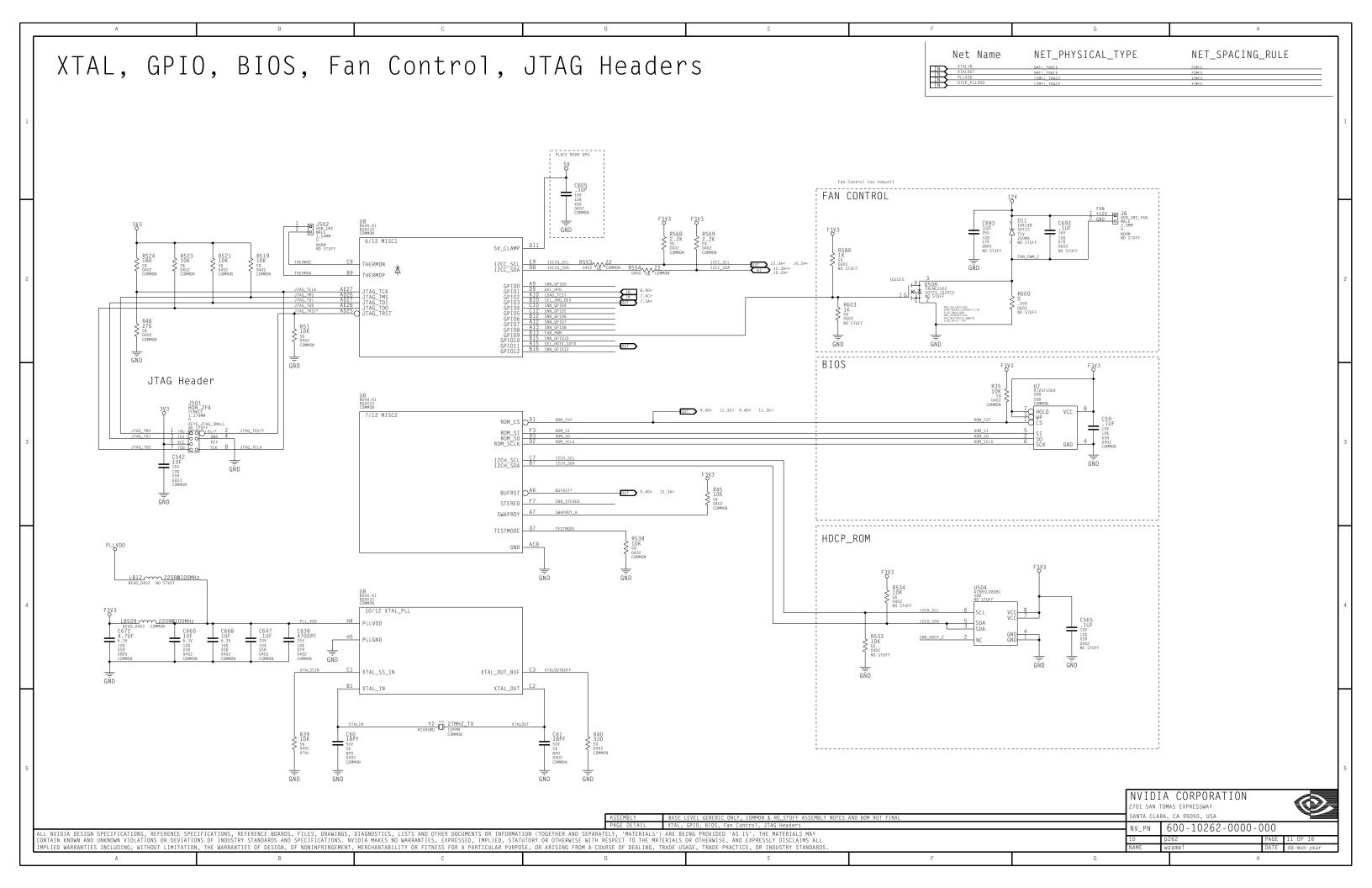


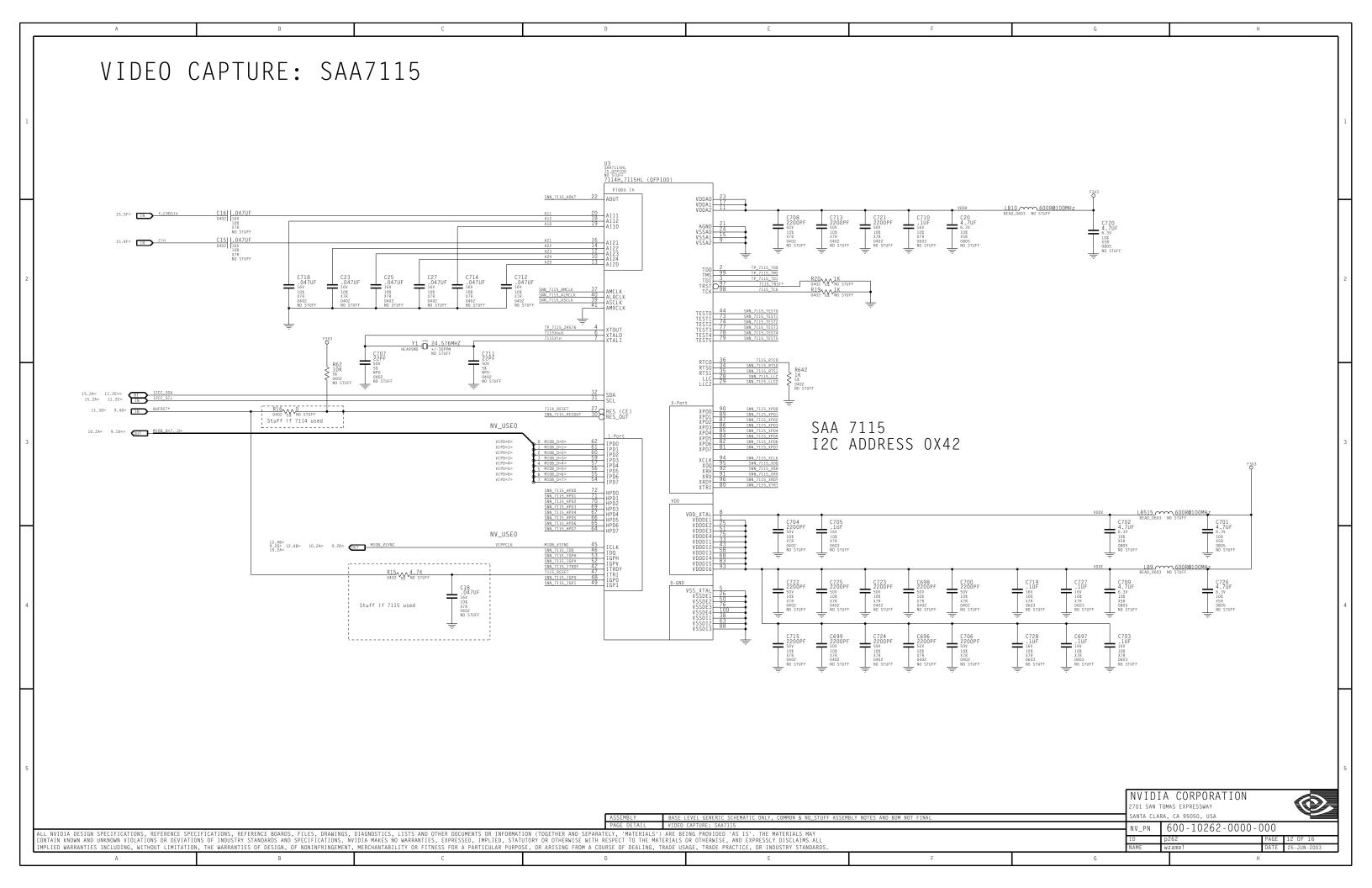


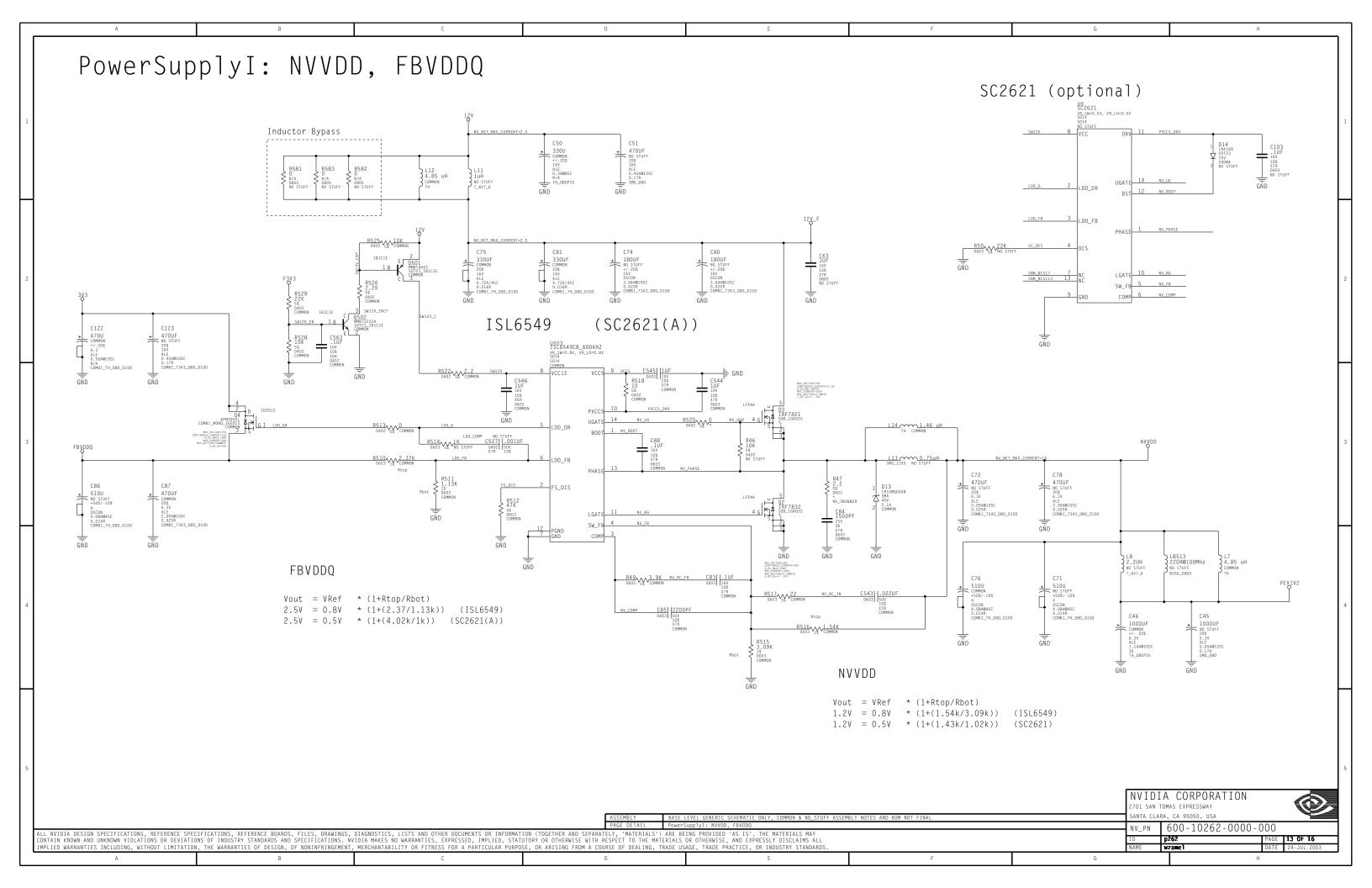




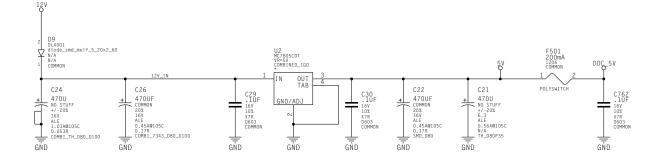


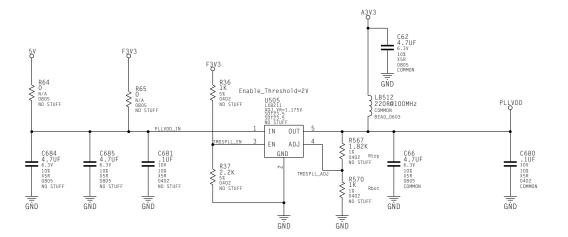




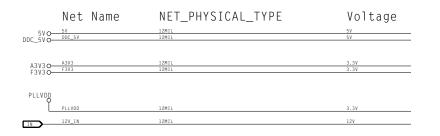


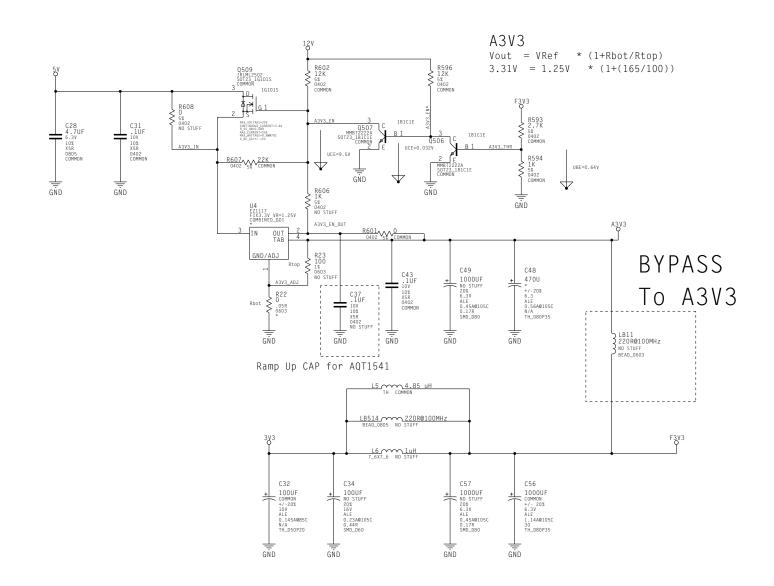
PowerSupplyII: 5V, DDC5V, A3V3, F3V3, TMDS_PLLVDD





TMDS_PLLVDD Vout = VRef * (1+Rtop/Rbot) 3.31V = 1.175V * (1+(1.82k/1k))





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