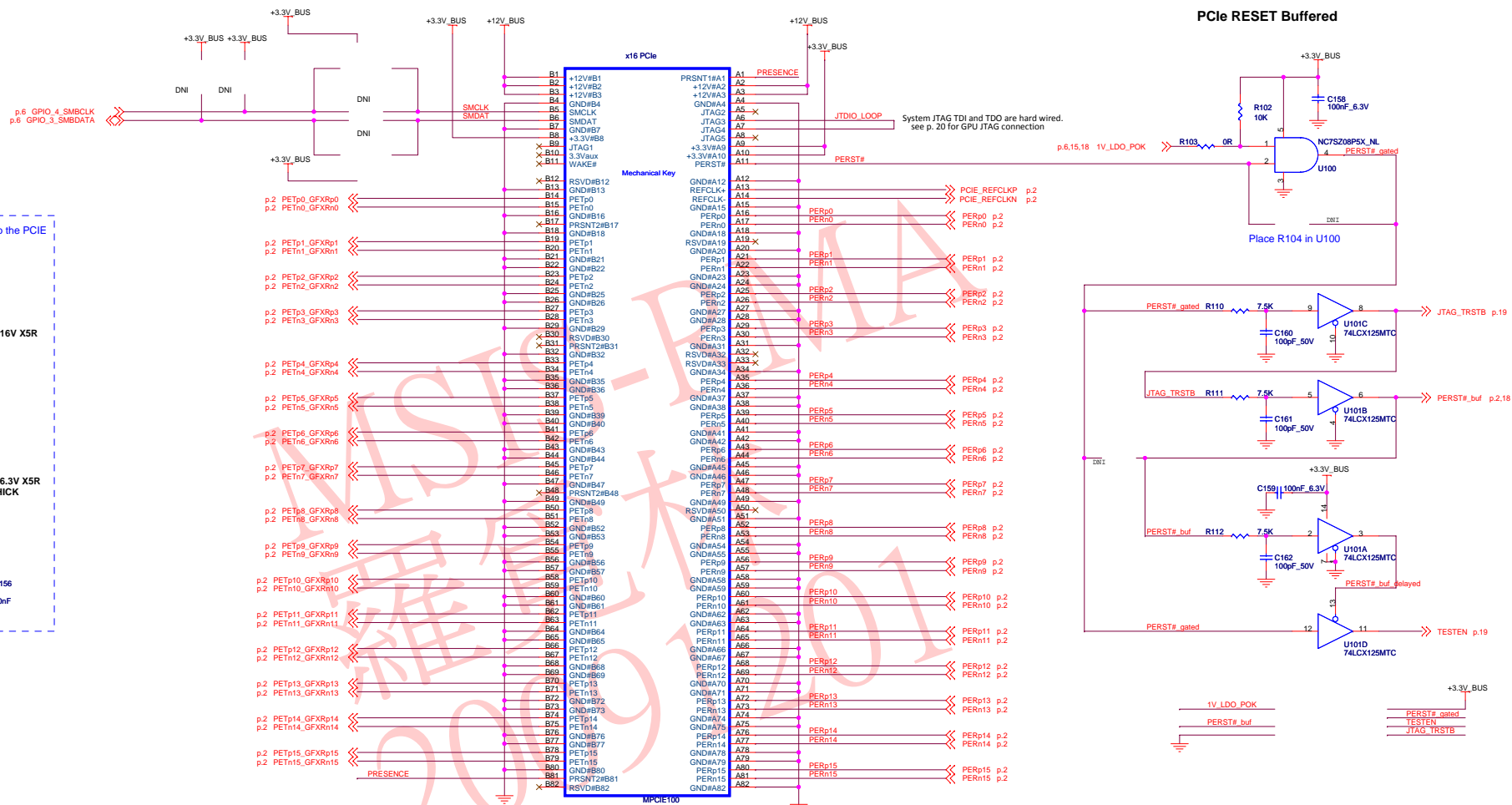
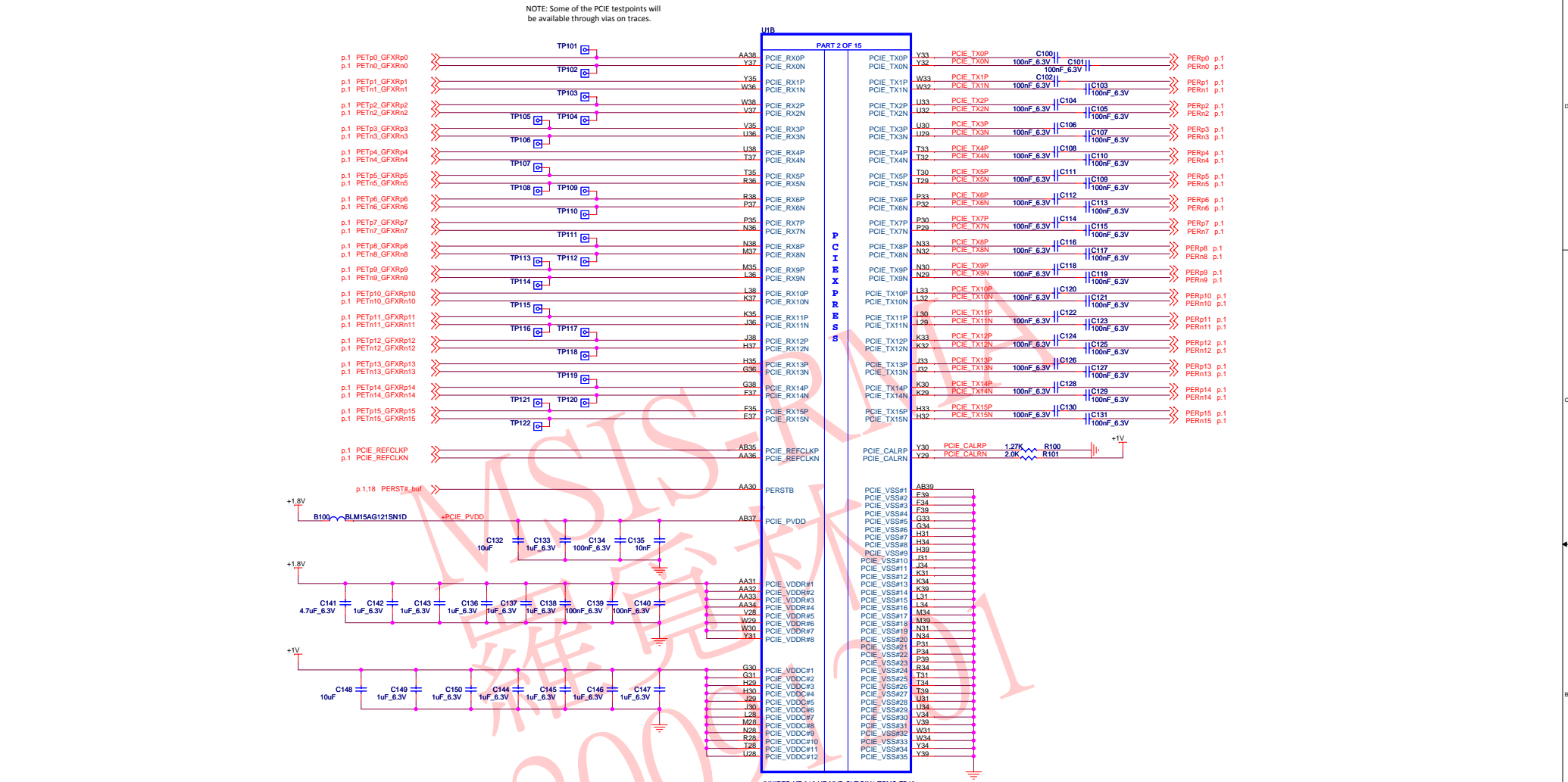


# PCI-EXPRESS EDGE CONNECTOR

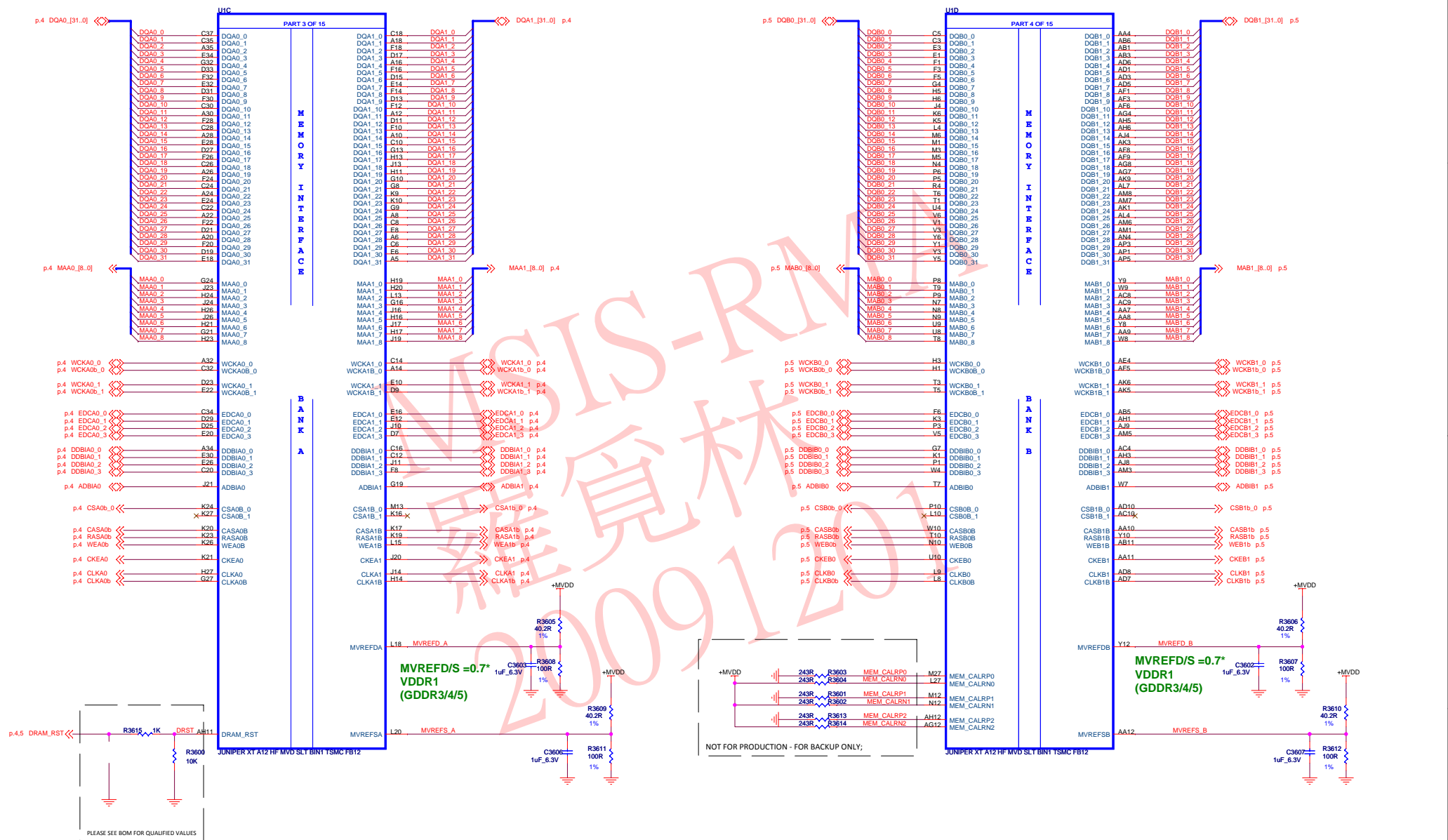
C013



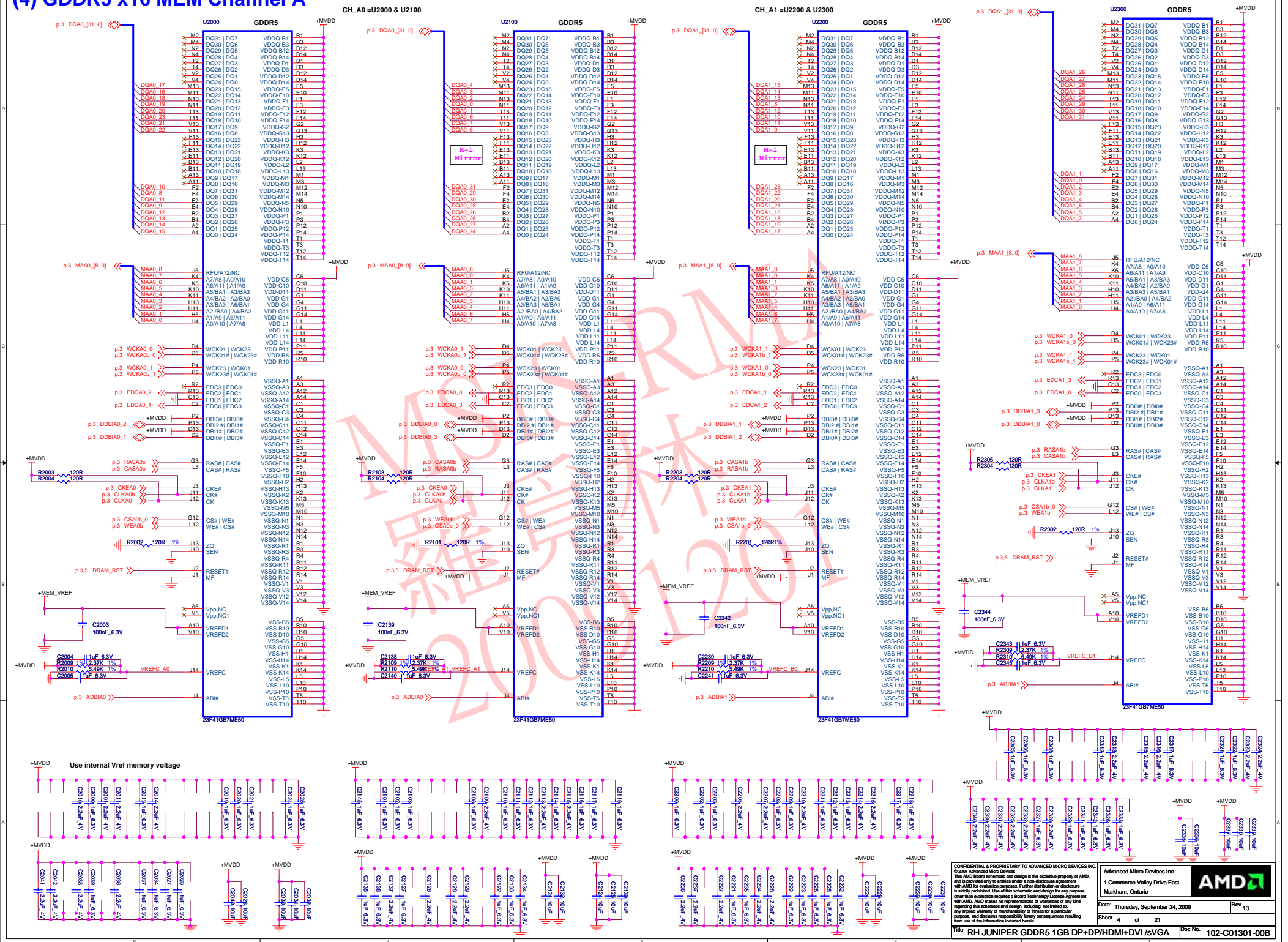
(2) JUNIPER PCIe Interface



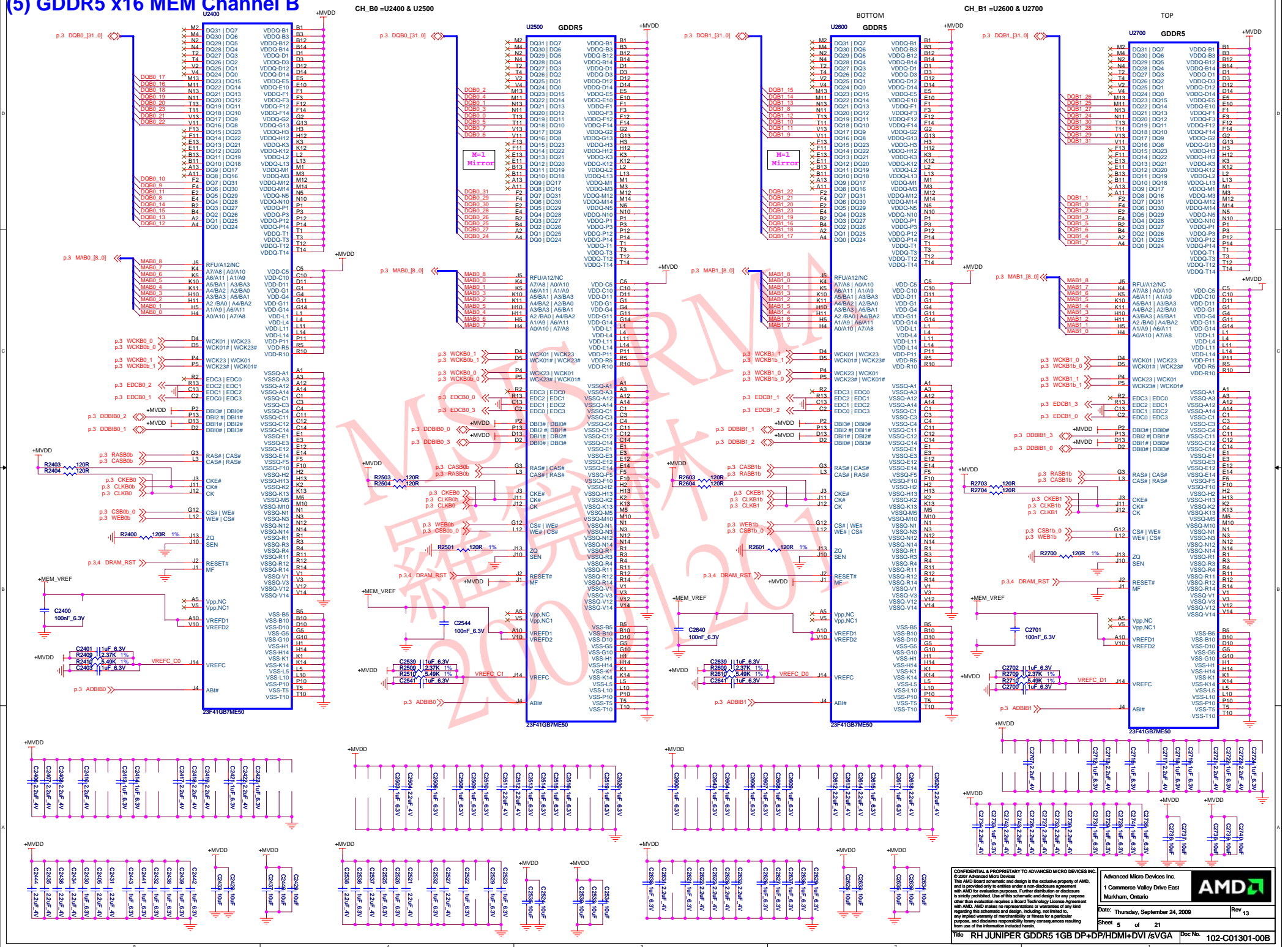
### (3) JUNIPER MEM Interface Ch A&B



#### (4) GDDR5 x16 MEM Channel A

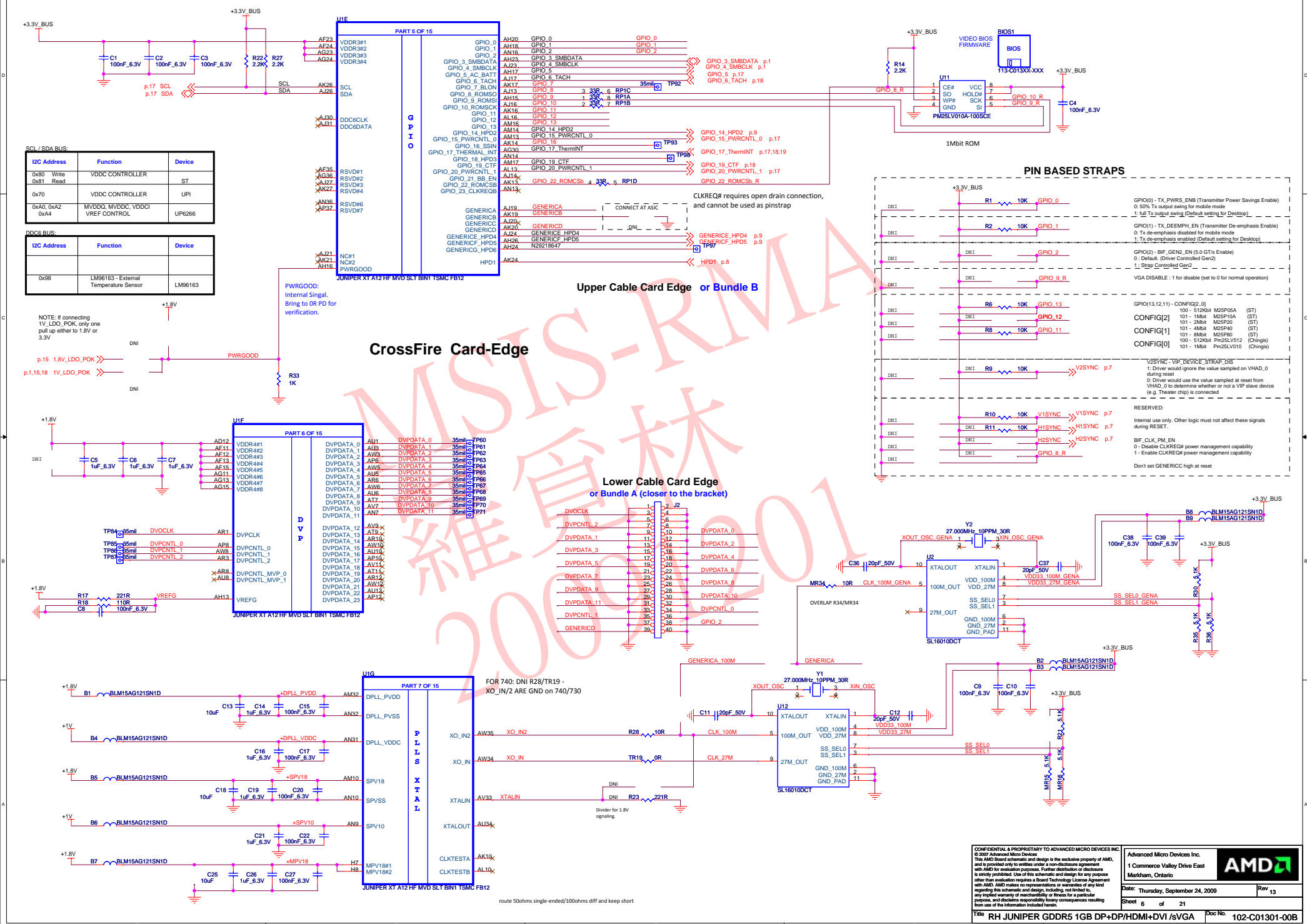


**(5) GDDR5 x16 MEM Channel B**

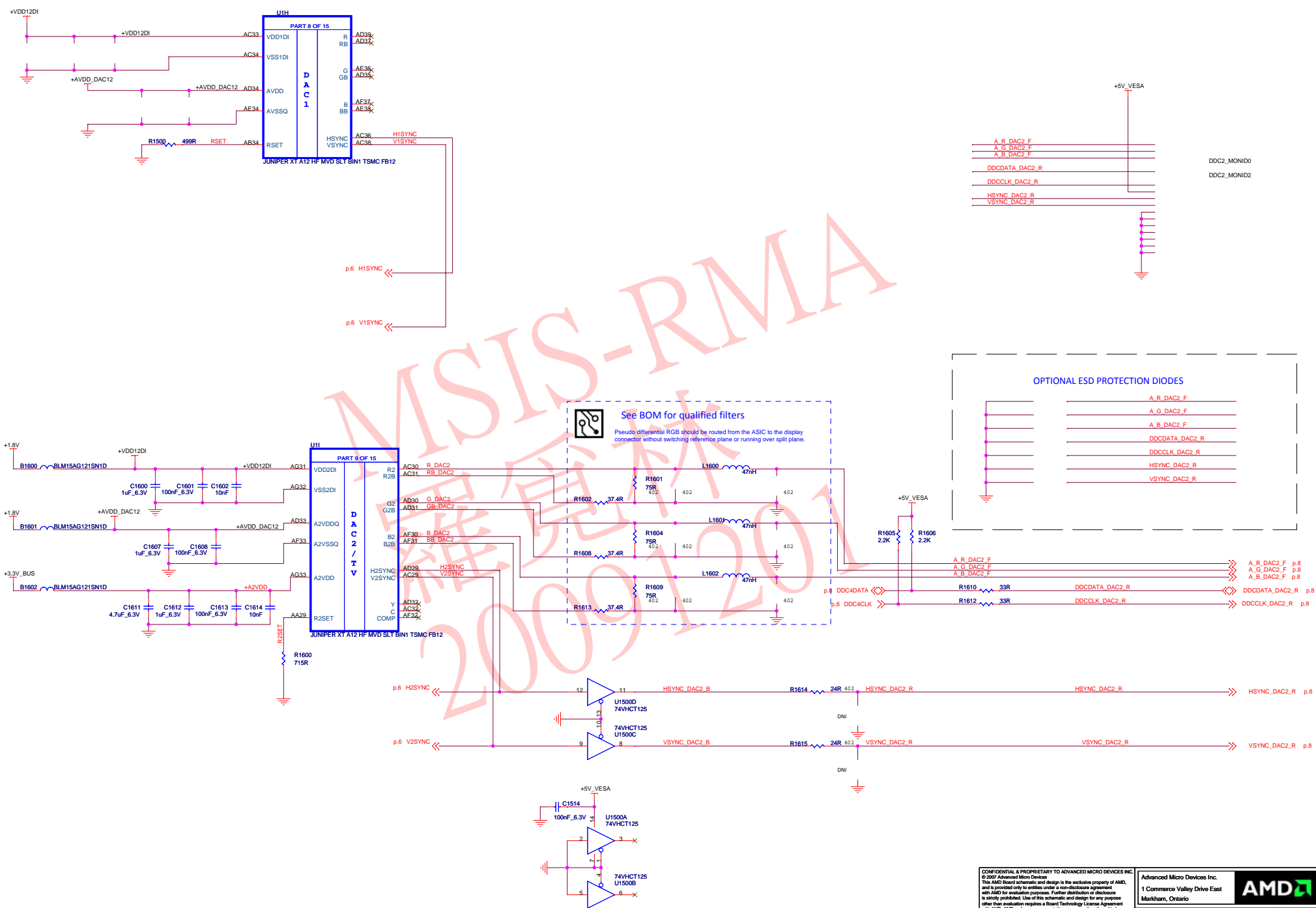





# (06) JUNIPER GPIOs Strap CF XTAL OSC

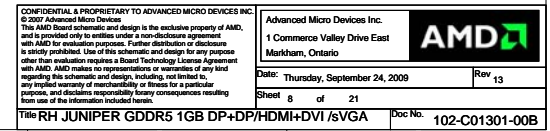


## (07) JUNIPER DAC1 and DAC2



|  |  |   |  |
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| Sheet 7 of 21  |  |   |  |
| Title RH JUNIPER GDDR5 1GB DP-DD/HDMI+DVI s/VSGA   |  | Doc No. 102-C01301-00E  |  |

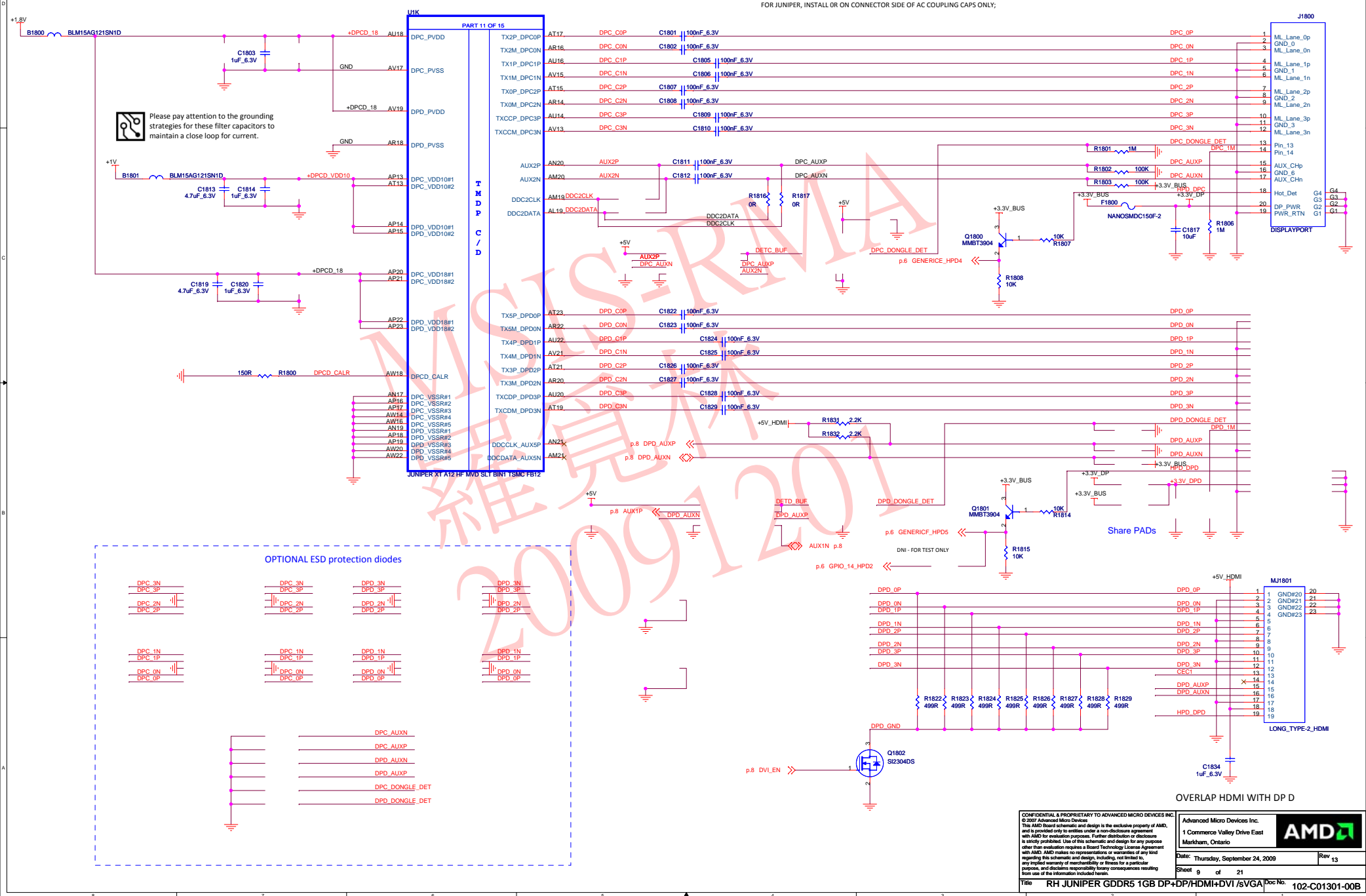
Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.






## (09) JUNIPER Display Port C & Display Port/HDMI D

AUX/DDC:  
FOR 740/730, INSTALL OR ON ASIC-SIDE OF AC COUPLING CAPS ONLY;  
FOR JUNIPER, INSTALL OR ON CONNECTOR SIDE OF AC COUPLING CAPS ONLY;

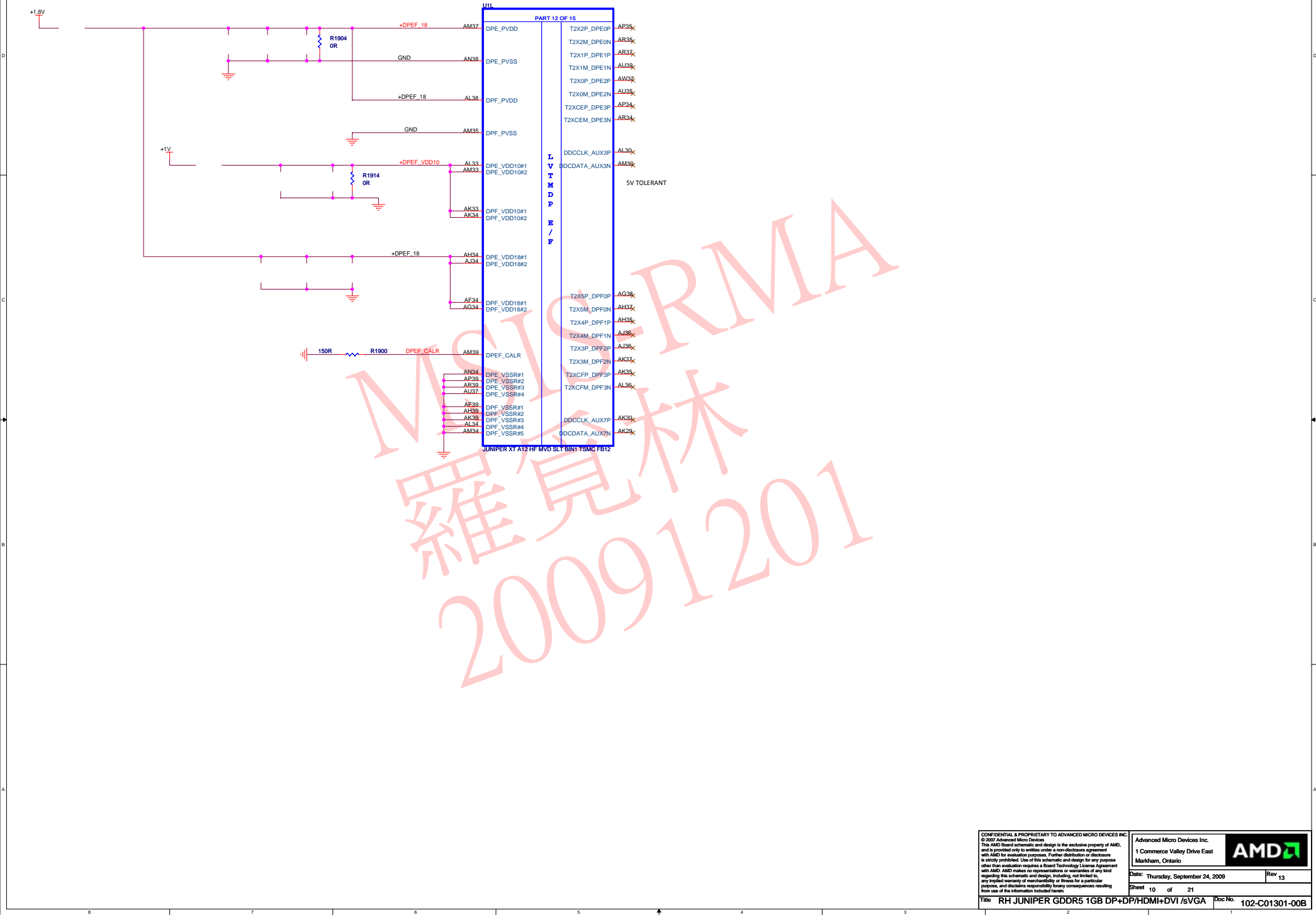


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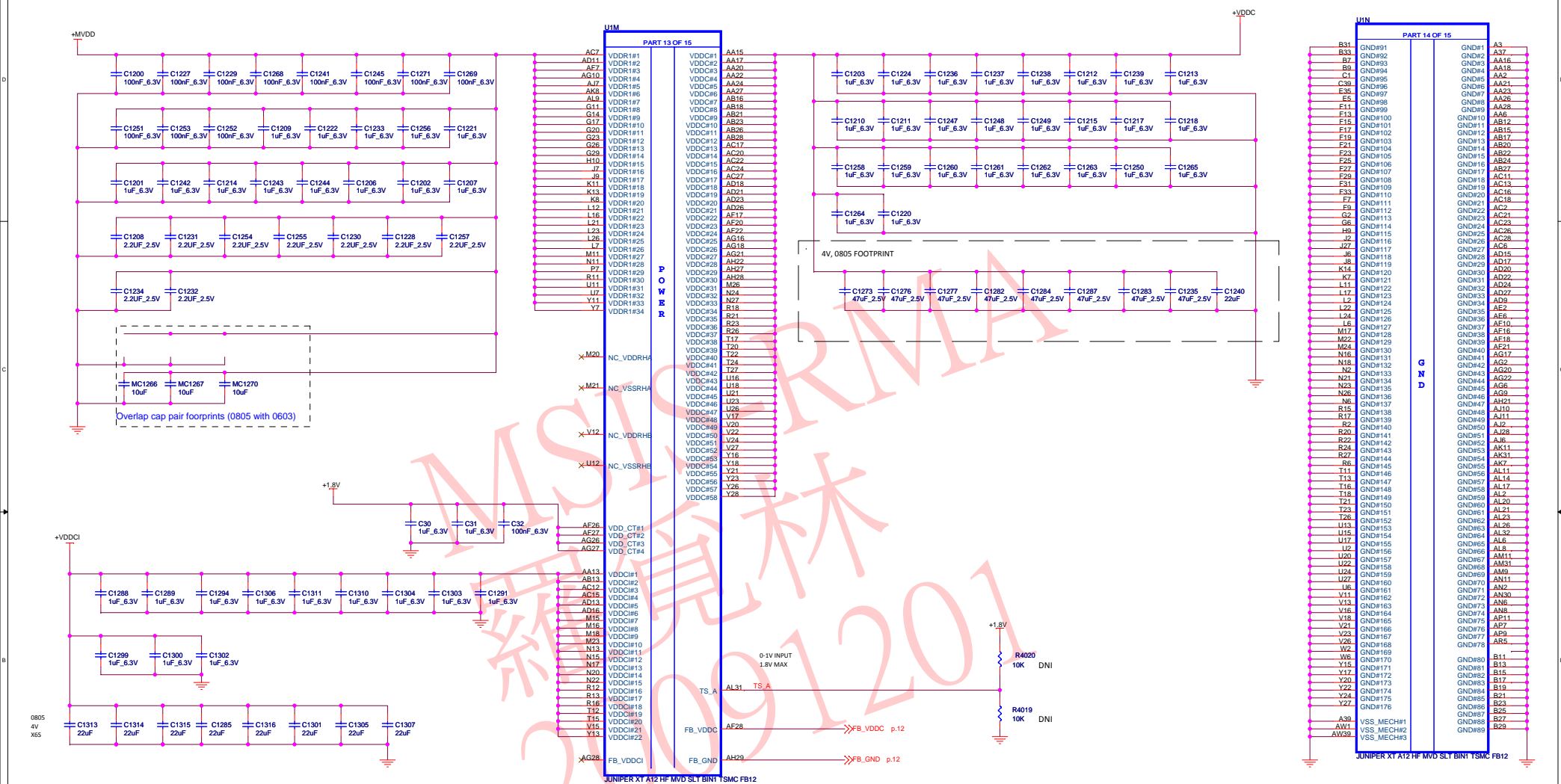
Title RH JUNIPER GDDR5 1GB DP

|  |  |   |  |
|--|--|---|--|
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| Date: Thursday, September 24, 2009   |  | Rev 13  |  |
| Sheet 9 of 21  |  |   |  |
| <b>+DP/HDMI+DVI /sVGA</b>  |  | Doc No. 102-C01301-00B  |  |

(10) JUNIPER LVTMDP E&F



## (11) JUNIPER Power & GND



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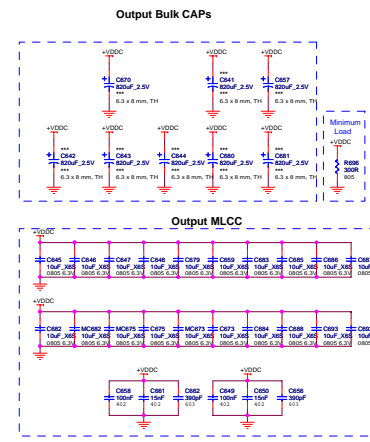
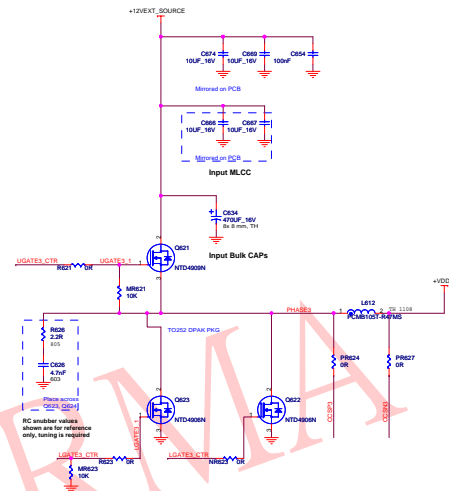
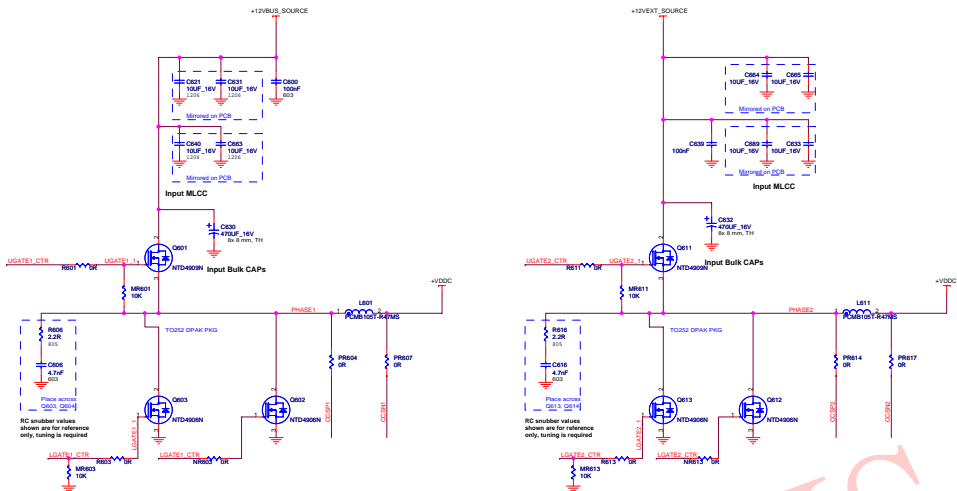
Date: Thursday, September 24, 2009

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Rev 13

|       |   |         |                |
|-------|---|---------|----------------|
| Title | RH JUNIPER GDDR5 1GB DP+DP/HDMI+DVI /sVGA | Doc No. | 102-C01301-00B |
|-------|---|---------|----------------|



Circuitry that has to be placed close to the device:

- current sense,
- compensation network,
- thermal compensation network (Drop, OCP, etc)

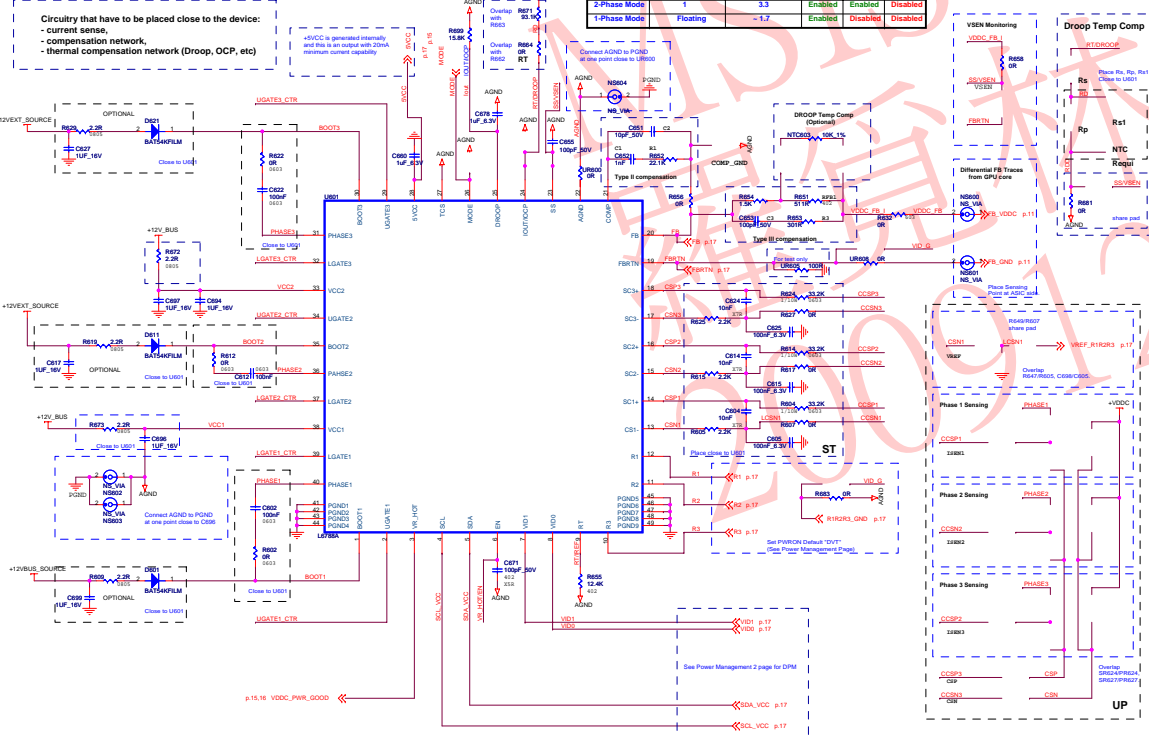


Table 1 MODE Pin Definition Table

| VPM Mode     | Mode Pin Status | Mode Pin Voltage (V) | Phase 1 | Phase 2  | Phase 3  |
|--------------|-----------------|----------------------|---------|----------|----------|
| 3-Phase Mode | 0               | 0                    | Enabled | Enabled  | Enabled  |
| 2-Phase Mode | 1               | 3.3                  | Enabled | Enabled  | Disabled |
| 1-Phase Mode | Floating        | -1.7                 | Enabled | Disabled | Disabled |

Table 1 VRHOT/EN Table

| EN | Q1  | Q2  | VR_HOT/EN | IC       | VR_HOT     | GPIO |
|----|-----|-----|-----------|----------|------------|------|
| 1  | on  | off | 0         | Disabled | /          | 1    |
| 0  | off | on  | 5V        | Enabled  | No Warning | 0    |
| 0  | off | off | 6.45V     | Enabled  | Warning    | 1    |

Table 1 VRHOT/EN Table

| EN | Q1  | Q2  | Q3  | VR_HOT/EN | IC       | VR_HOT     | GPIO |
|----|-----|-----|-----|-----------|----------|------------|------|
| 1  | on  | on  | on  | 0         | Disabled | /          | 0    |
| 0  | on  | on  | on  | 1.5V      | Enabled  | No Warning | 0    |
| 0  | off | off | off | 3.3V      | Enabled  | Warning    | 1    |

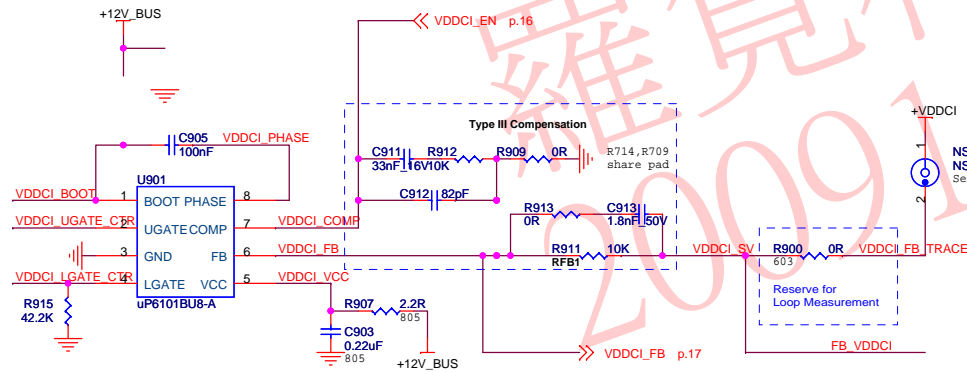
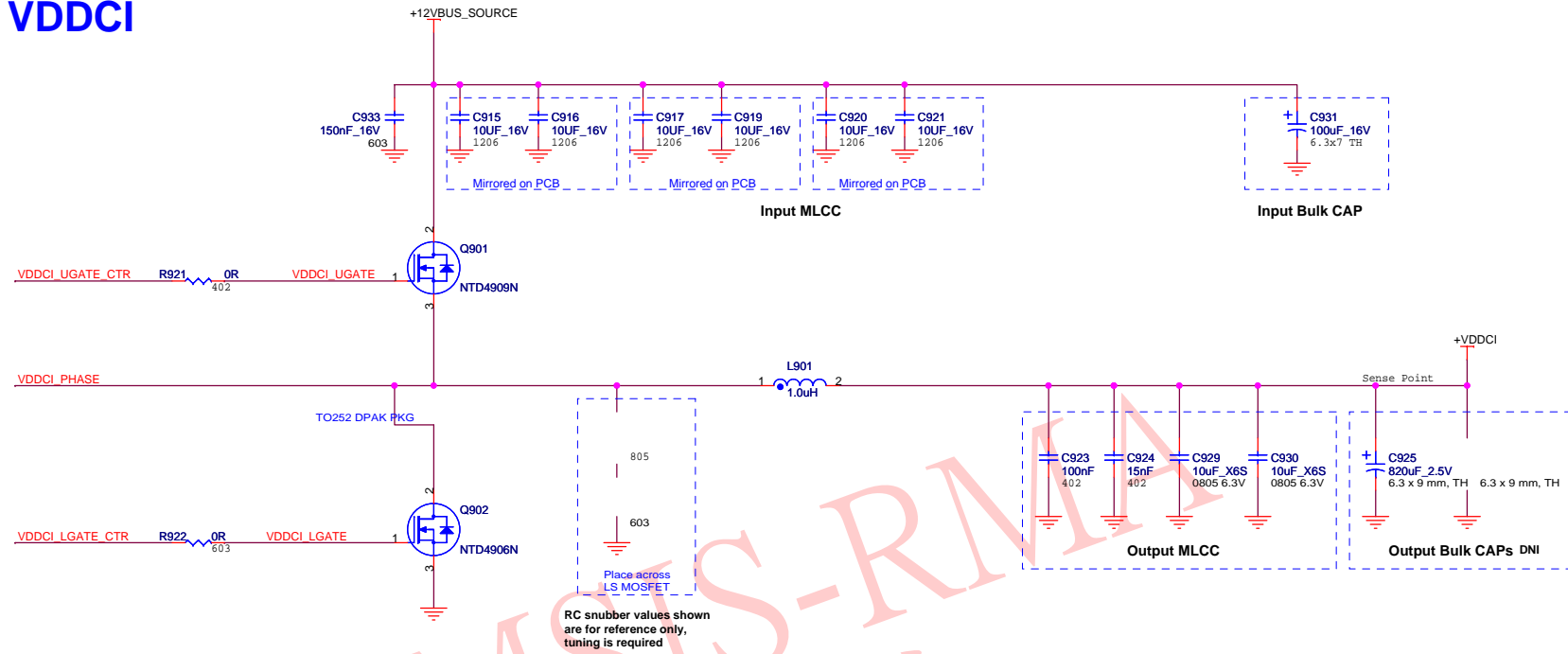
CASE1, CASE3 Special Case Power Up Detection

NOTE: This is for the IC that uses VDDC for EXT. 1.2V Detection.

Table 5 MODE Pin & Phase3 Strip Detection Table

| App    | Condition                       | Mode Pin | VPM Mode  | Phase 3   | IC Behavior  |
|--------|---------------------------------|----------|-----------|-----------|--|
| CASE 1 | PowerUp without EXT. 1.2V Cable | 0        | 2-Ph Mode | Open      | IC enabled without detecting EXT. 1.2V (VDDC) voltage. |
| CASE 3 | PowerUp with EXT. 1.2V Cable    | 1        | 2-Ph Mode | Pull Down | Detect EXT. 1.2V (VDDC) voltage before IC enable.      |

# (13) VDDCI



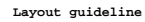
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Date: Thursday, September 24, 2009  
Sheet 13 of 21  
Rev 13

Title RH JUNIPER GDDR5 1GB DP+DP/HDMI+DVI /sVGA  
Doc No. 102-C01301-00B

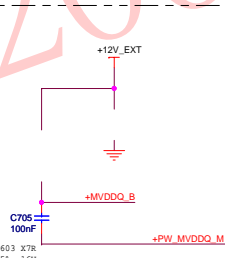
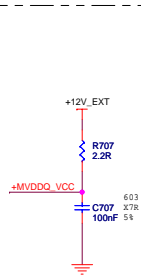
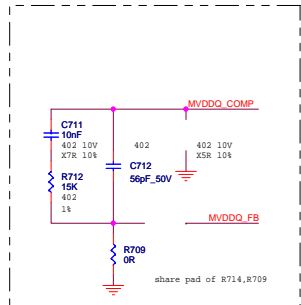
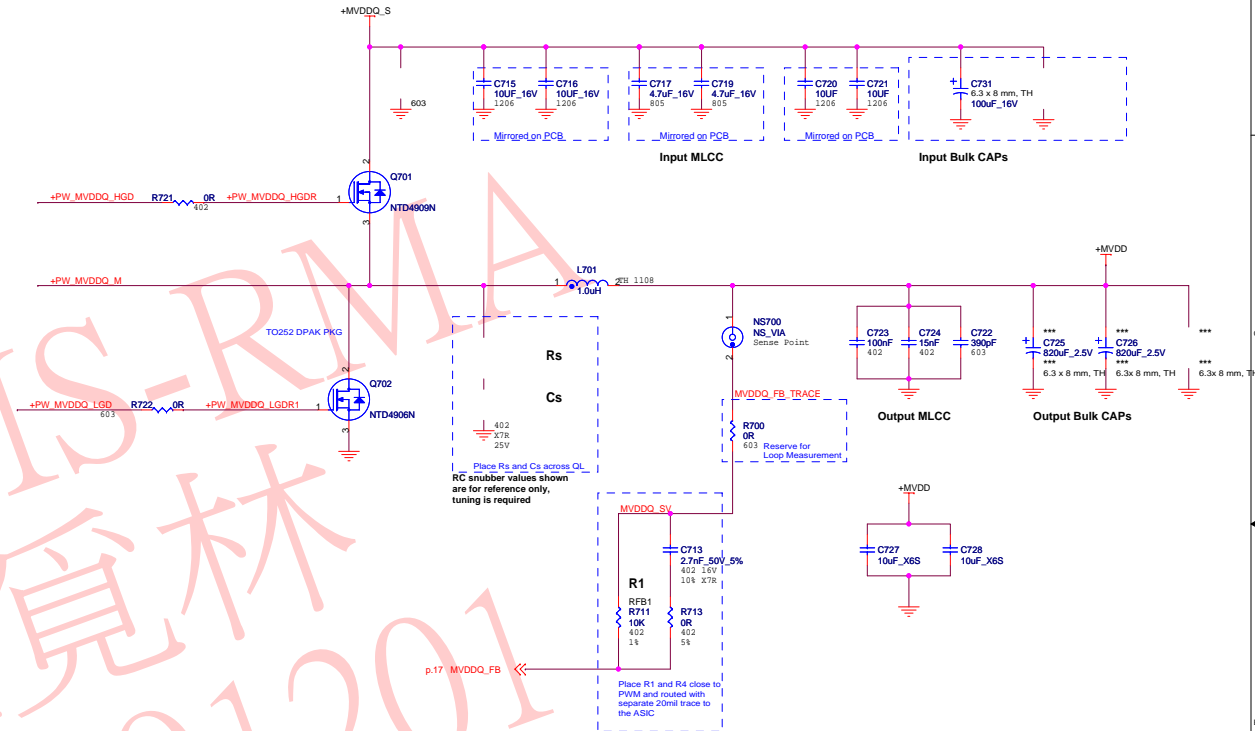




1-Position the controller (U703) such that LdGate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R71 and R722 next to the gate of the MOSFETs. Make the gate drive traces (PW MVDCD GND and PW MVDCD GND) as short and as wide as possible to reduce the trace inductance.


2-Place the bypass capacitors (C701, C702, C703) as close to the boost MOSFET controller as possible. They are as follows:

- Use bypass cap is C703, and Boost cap is C705.
- Use 100nF electrolytic compensation capacitor C701 close to the pin 7. Place the rest of the compensation network close to pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



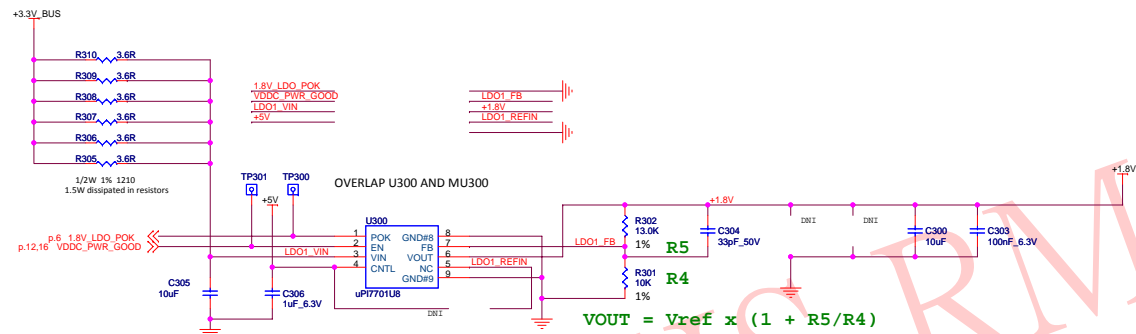
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**Title** RH JUNIPER GDDR5 1GB DP+DP

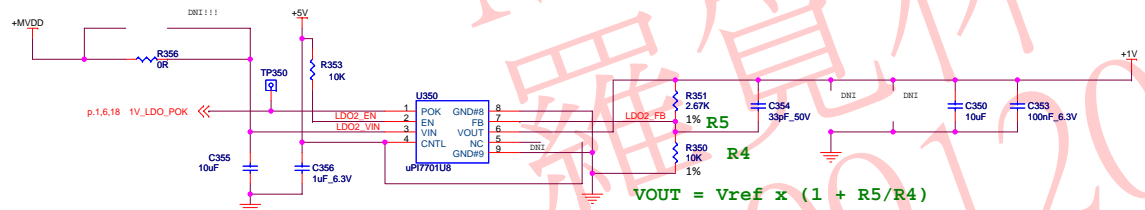
|   |  |   |  |
|---|--|---|--|
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| Date: Thursday, September 24, 2009  |  | Rev 13  |  |
| Sheet 14 of 21  |  |   |  |
| P/HDMI+DVI /sVGA  |  | Doc No. 102-C01301-00B  |  |

## (15) Linear Regulators

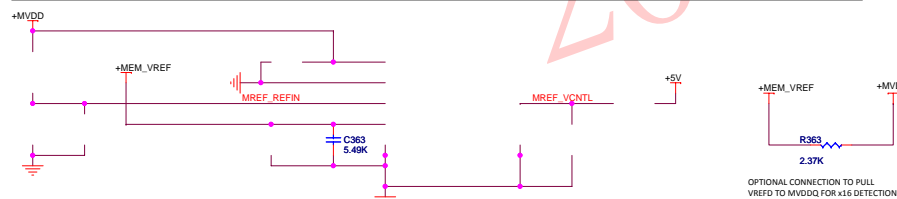
**LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX**  
**PCB: 50 to 70mm sq. copper area for cooling**



**LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX**  
**PCB: 50 to 70mm sq. copper area for cooling**

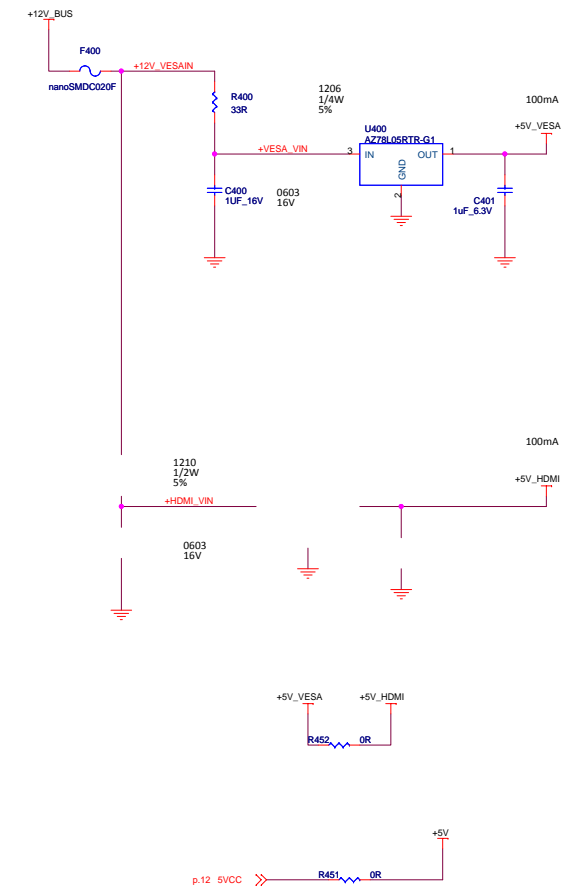


**Memory VREF:**       $V_{in} = MVDDQ$        $V_{out} = 0.7 \times MVDDQ$



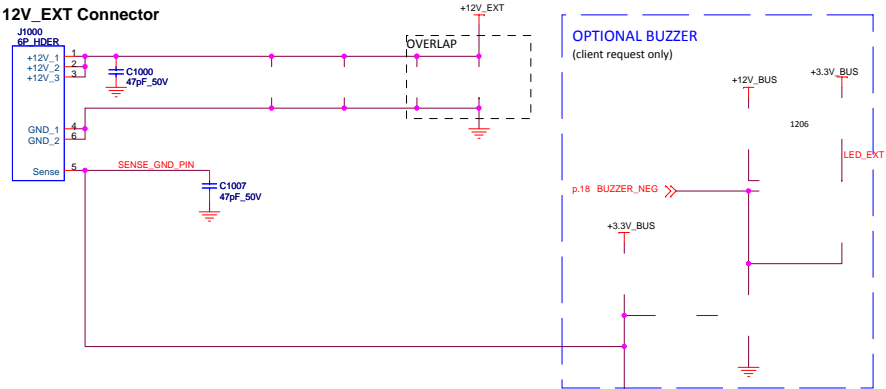
There must be one 100nF at each VREF pin  
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices

### Regulators for +5V, +5V\_VESA and +5V\_HDMI

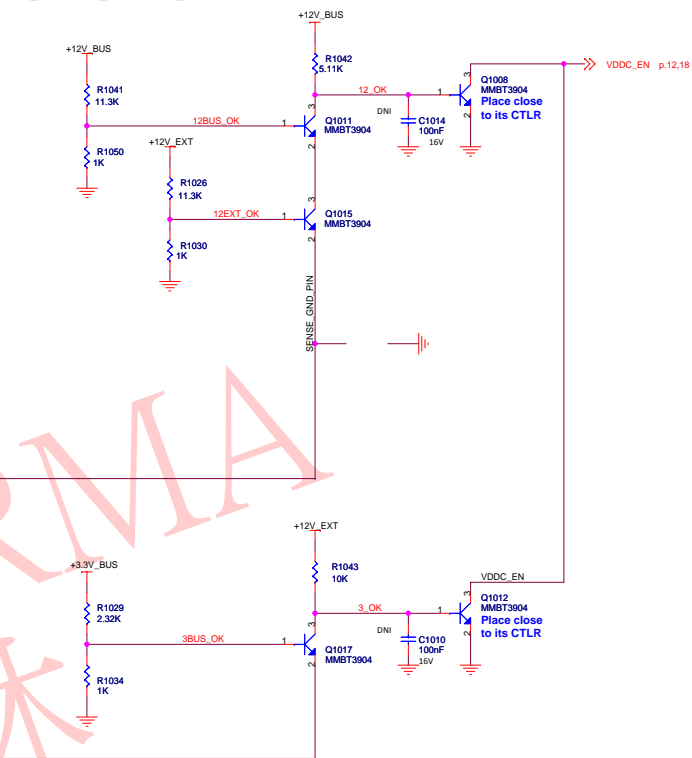


(16) Power Management - Power Gating

12V\_EXT Connector

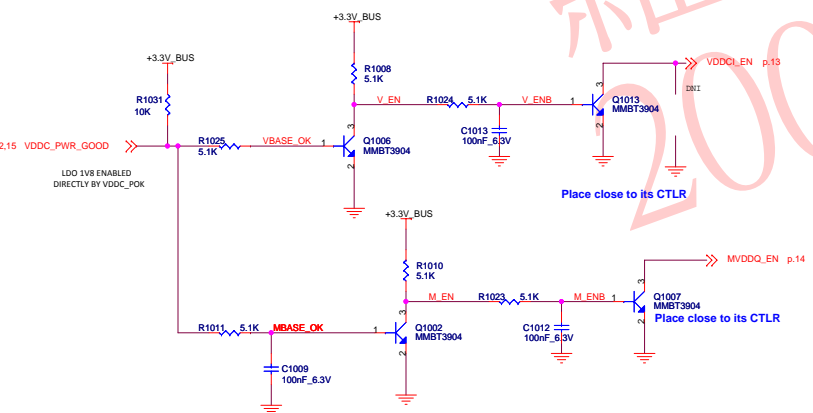


12V\_BUS, 12V\_EXT & 3V3\_BUS POWER SEQUENCING

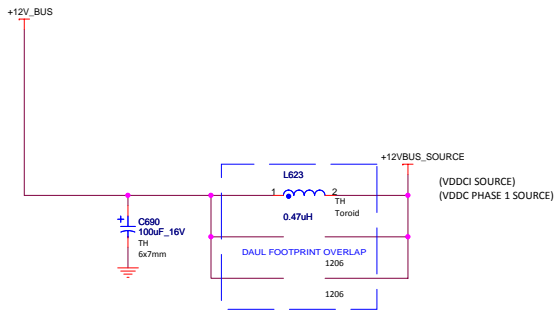


POWER SEQUENCING CIRCUIT

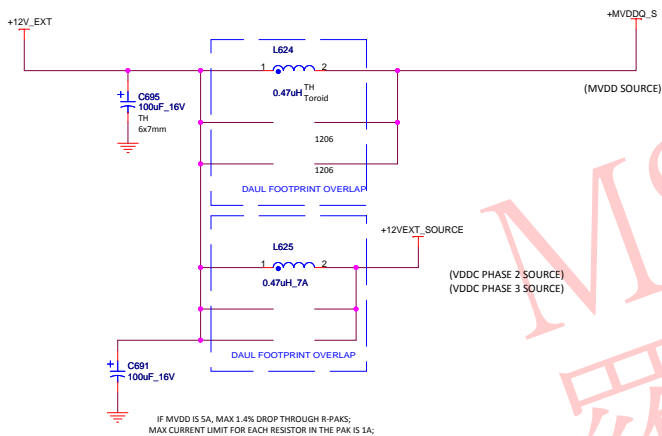
FOR MVDD & VDDCI  
(ENABLES CANNOT BE SHARED SINCE IT IS ALSO THE COMPENSATION PIN OF THE SMPS REGULATOR)



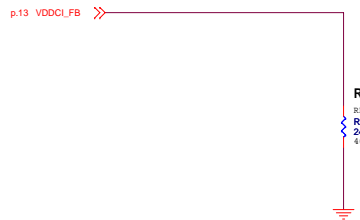
(17) Power Management 2



NOTE: Use ML623 with Fansink P/N 7120084000G



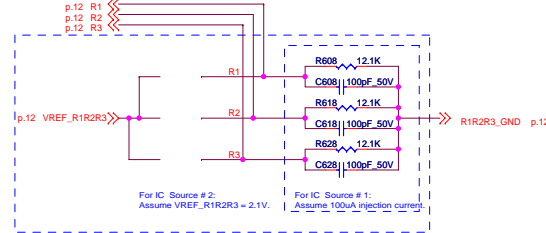
VDDCI Low Side Divider



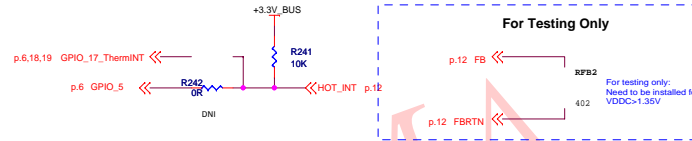
VDDC Setting

Analog Reference (Refer R to AGND)  
Close to U601  
Be careful when changing R655 value (VDDC IREF)

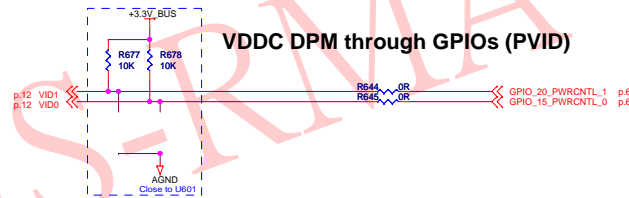
SET DEFAULT VOLTAGE POWER-ON TABLE



For Testing Only



VDDC DPM through GPIOs (PVID)

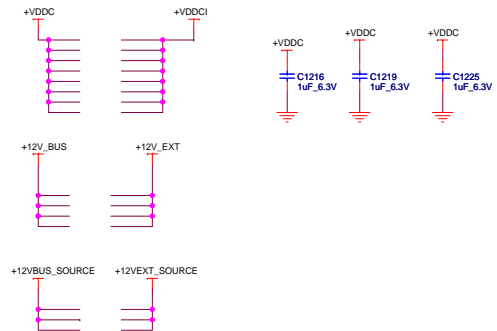
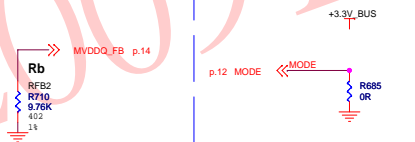


VDDC I2C INTERFACE

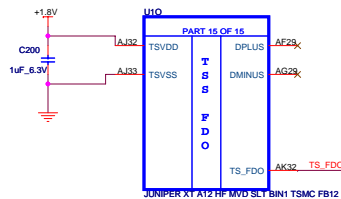


ALL OR RESISTORS TO BE REMOVED FOR PRODUCTION;

MODE Pin Detection Circuit

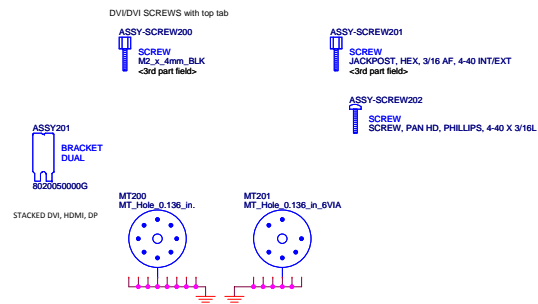
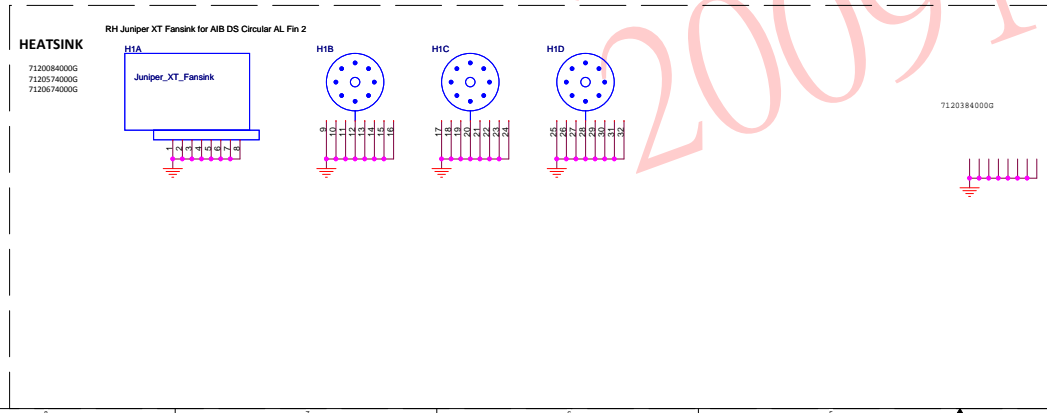
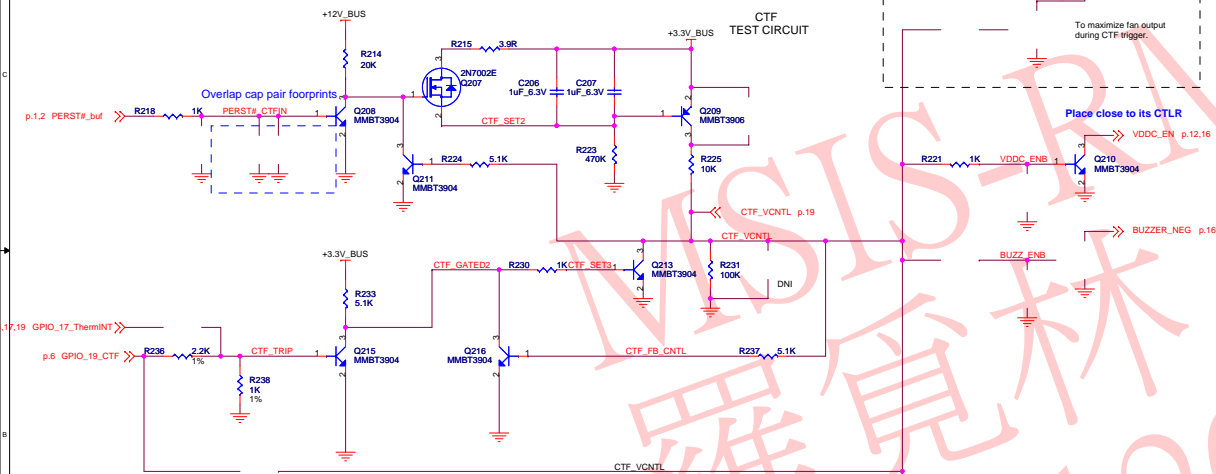
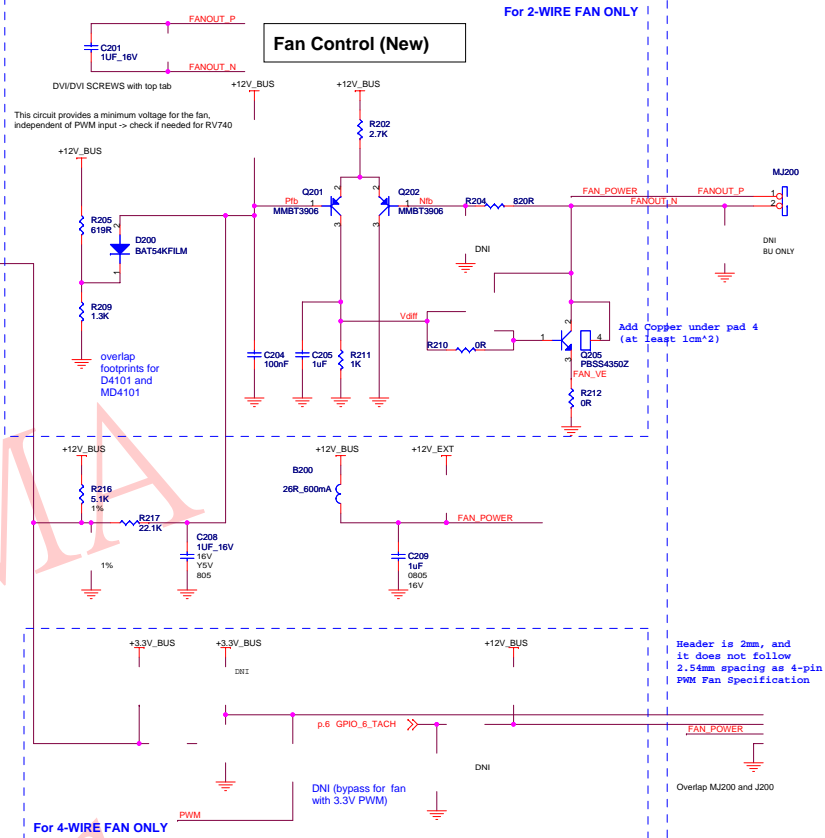
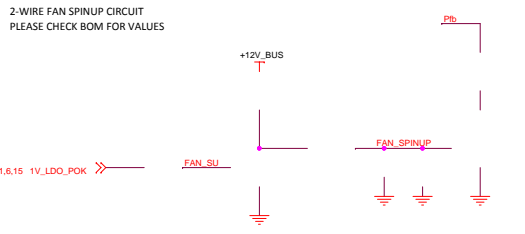


## (18) Mechanical and Thermal Management



**Warning: TS\_FDO is not 5V tolerant. MAX sink current 1.65mA**

**If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.**

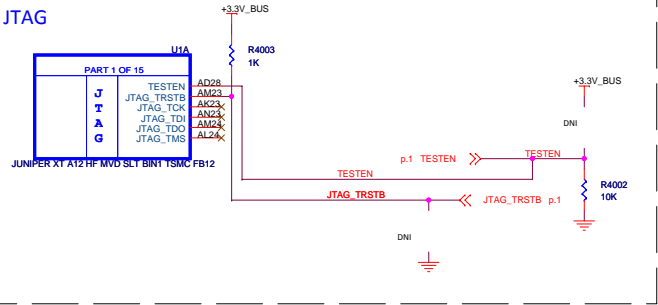


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| <p><b>AMD</b></p>  |  | <p>Date: Thursday, September 24, 2009 Rev 13</p>  |  |
| <p>Sheet 18 of 21</p>  |  | <p>Doc No: 102-C031-00B</p>   |  |
| <p>Title: RH JUNCTION GDDR5 1GB DP+DP/HDMI+DVI s/VSGA</p>  |  |   |  |

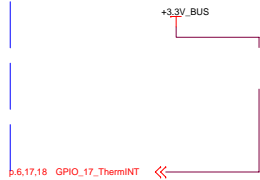


(19) Debug Circuits

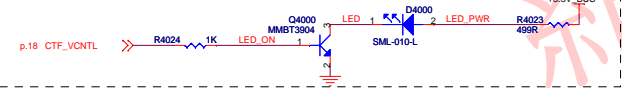
JTAG



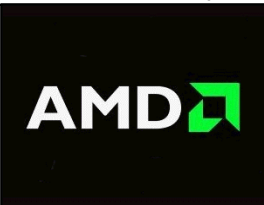
LM96163 FOR BACKUP THERMAL CONTROL



LED RED "ON" shows Fault







**RH JUNIPER GDDR5 1GB DP+DP/HDMI+DVI /sVGA**

102-C01301-00B

Thursday, September 24, 2009

**REVISION HISTORY**

**NOTE:** This schematic represents the PCB, it does not represent any specific SKU.  
 For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.  
 Please contact AMD representative to obtain latest BOM closest to the application desired.

**NOTE:** This schematic represents the PCB, it does not represent any specific SKU.  
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.  
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 13

| Sch Rev | PCB Rev | Date       | REVISION DESCRIPTION  |
|---------|---------|------------|---|
| 00      | 00A     | 2009/07/14 | JUNIPER GDDR5 1GB - BASED ON C010; VDDC/VDDCI/MVDD SMPS CHANGES; OTHER CIRCUITS UPDATED;  |
| 01      | 00B     | 2009/09/10 | p. 2 - remove FB_VDDCI (NC U1.AG28);<br>P. 11- add C670, C657,C673,C675,C682,C684,C688,C692,C693,MC673,MC675,MC682;<br>p. 13- remove FB_VDDCI off-page;<br>p. 19- remove J4004, add TESTEN/JTAG_TRSTB off-page; |
|         |         |            |   |

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20091201