<variant Name>

Title

RV550 LP HDMI VGA 256/512MB DDR2

Schematic No.

105-B173xx-00A

Date:

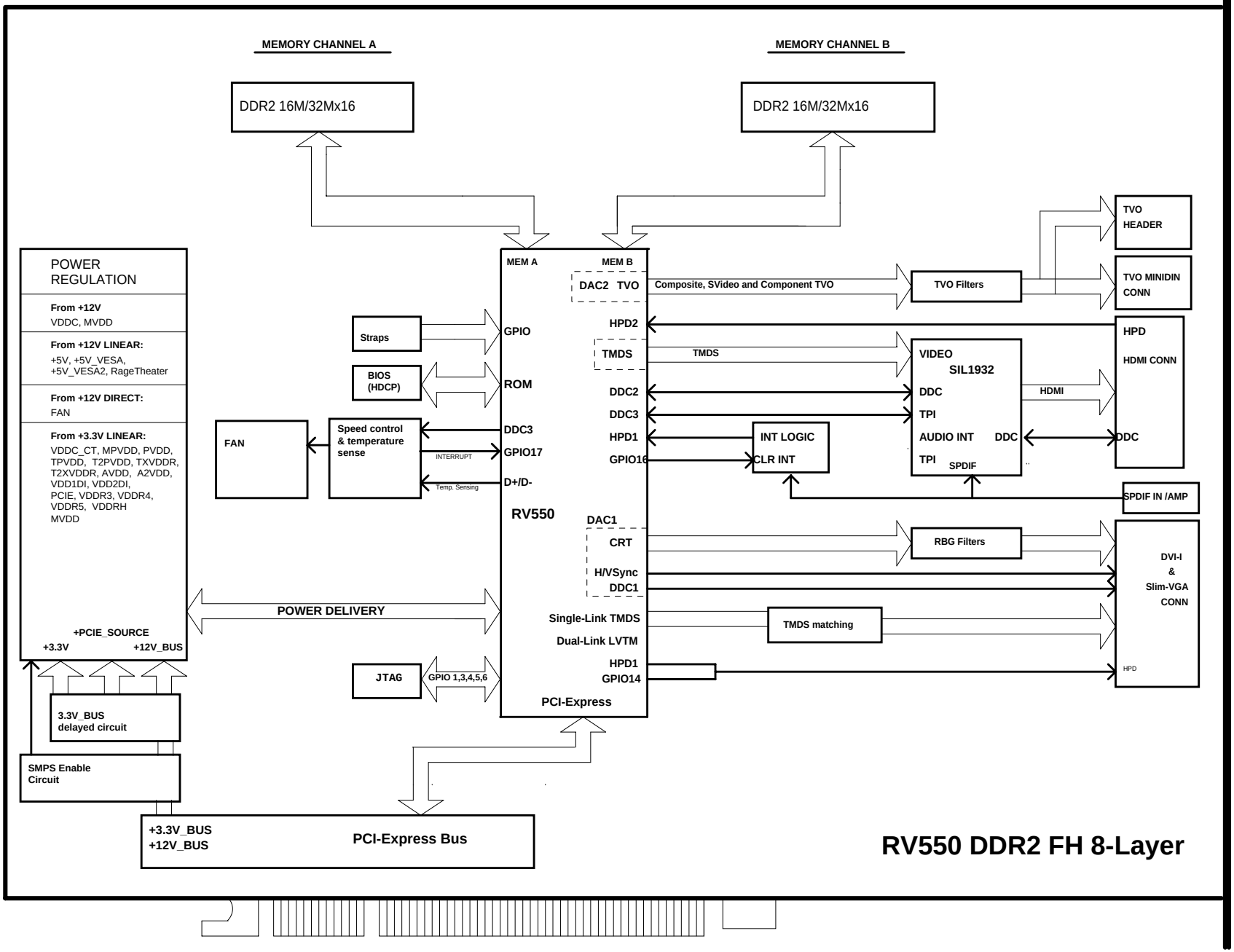
Sunday, November 26, 2006

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.**

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
01	00A	05-12-06	Copied from 105-A676xx-30.



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Canada, L3T 7X6
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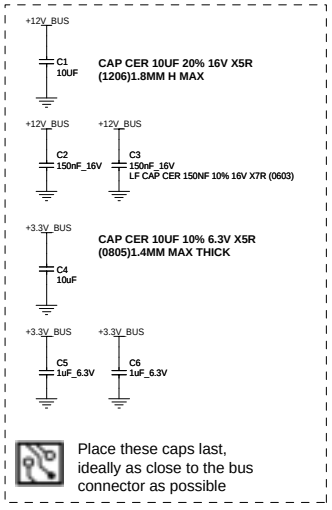
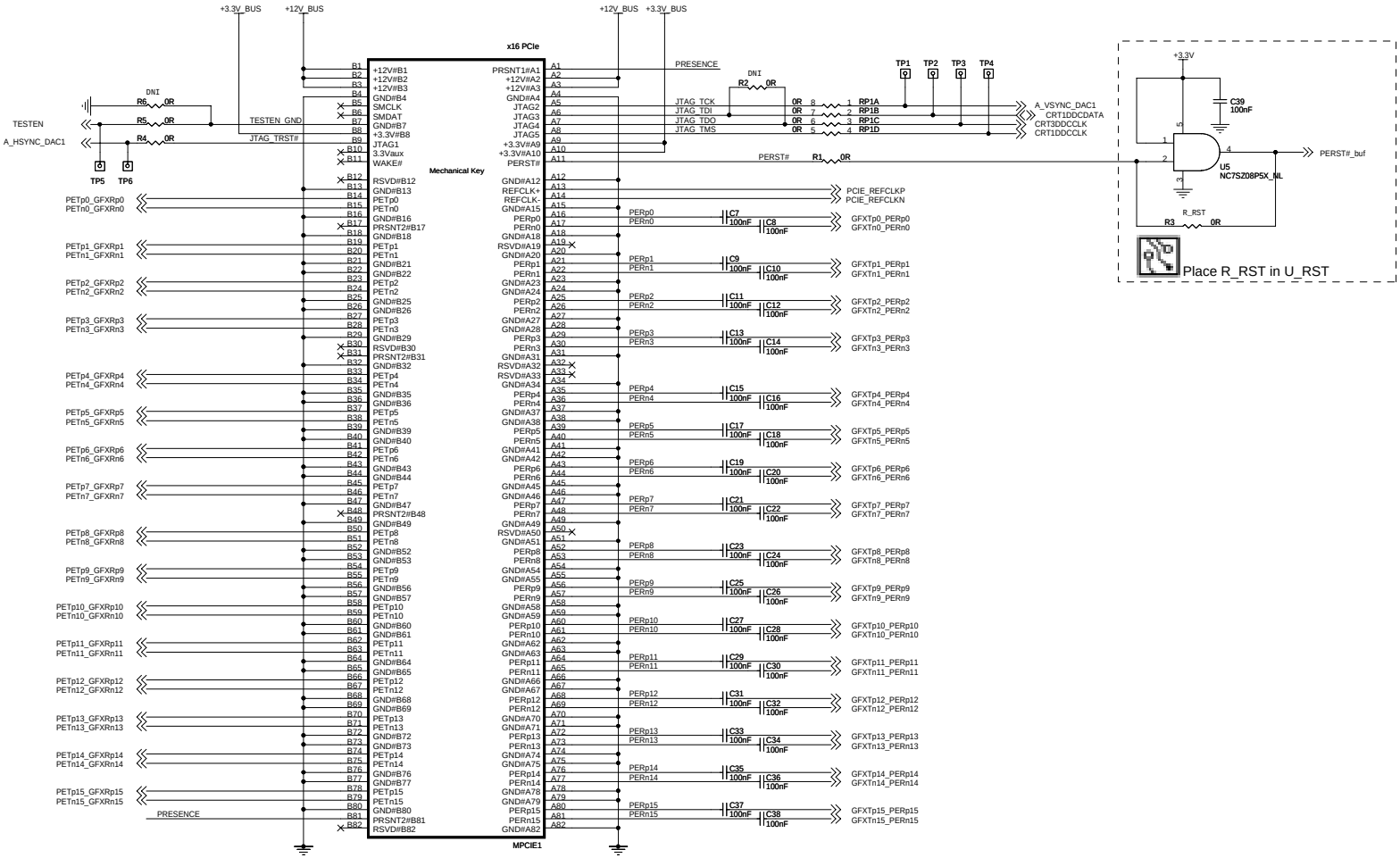
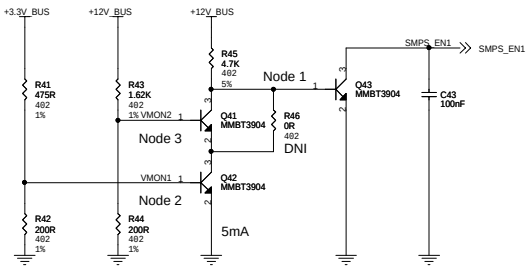
PCI-EXPRESS EDGE CONNECTOR







Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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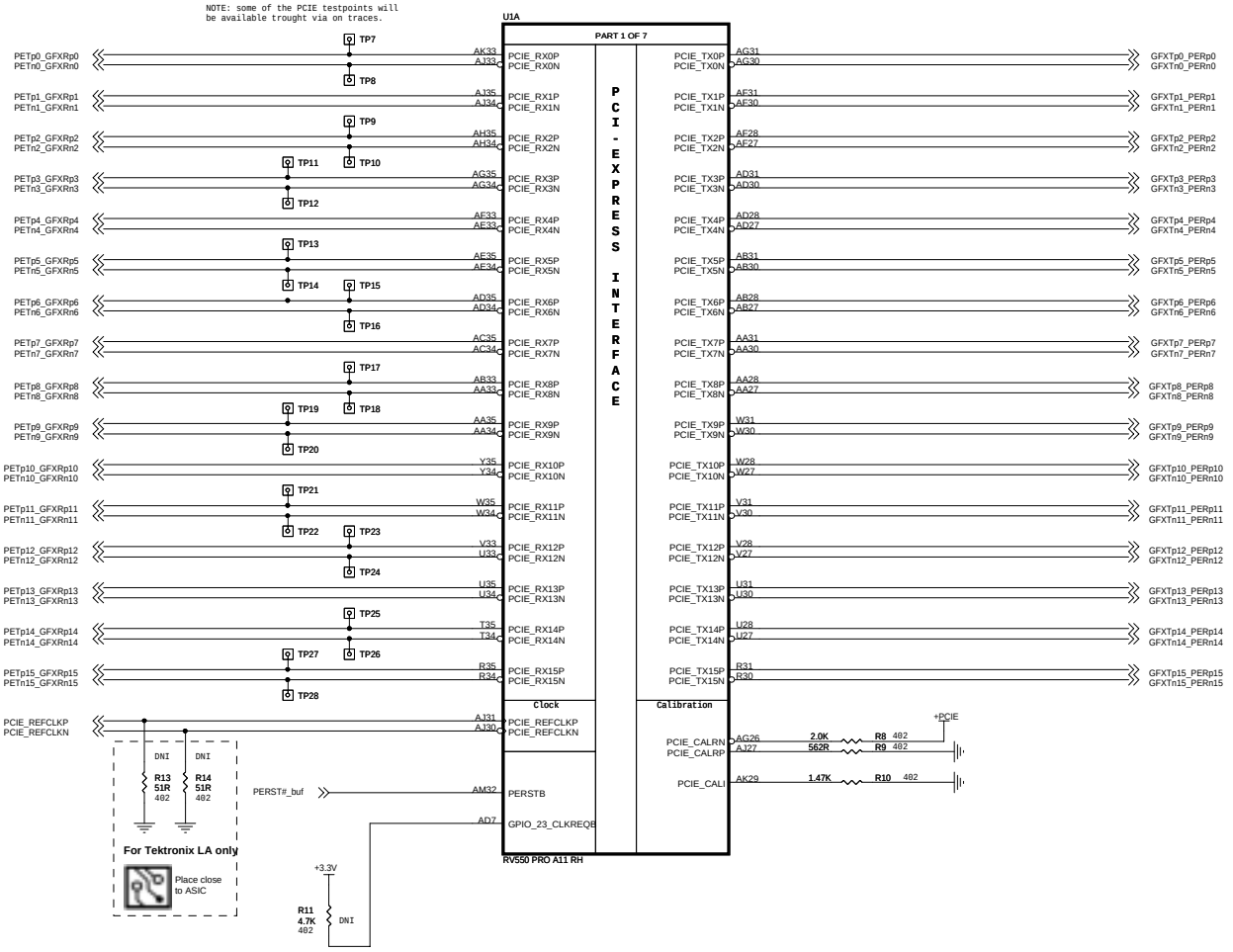

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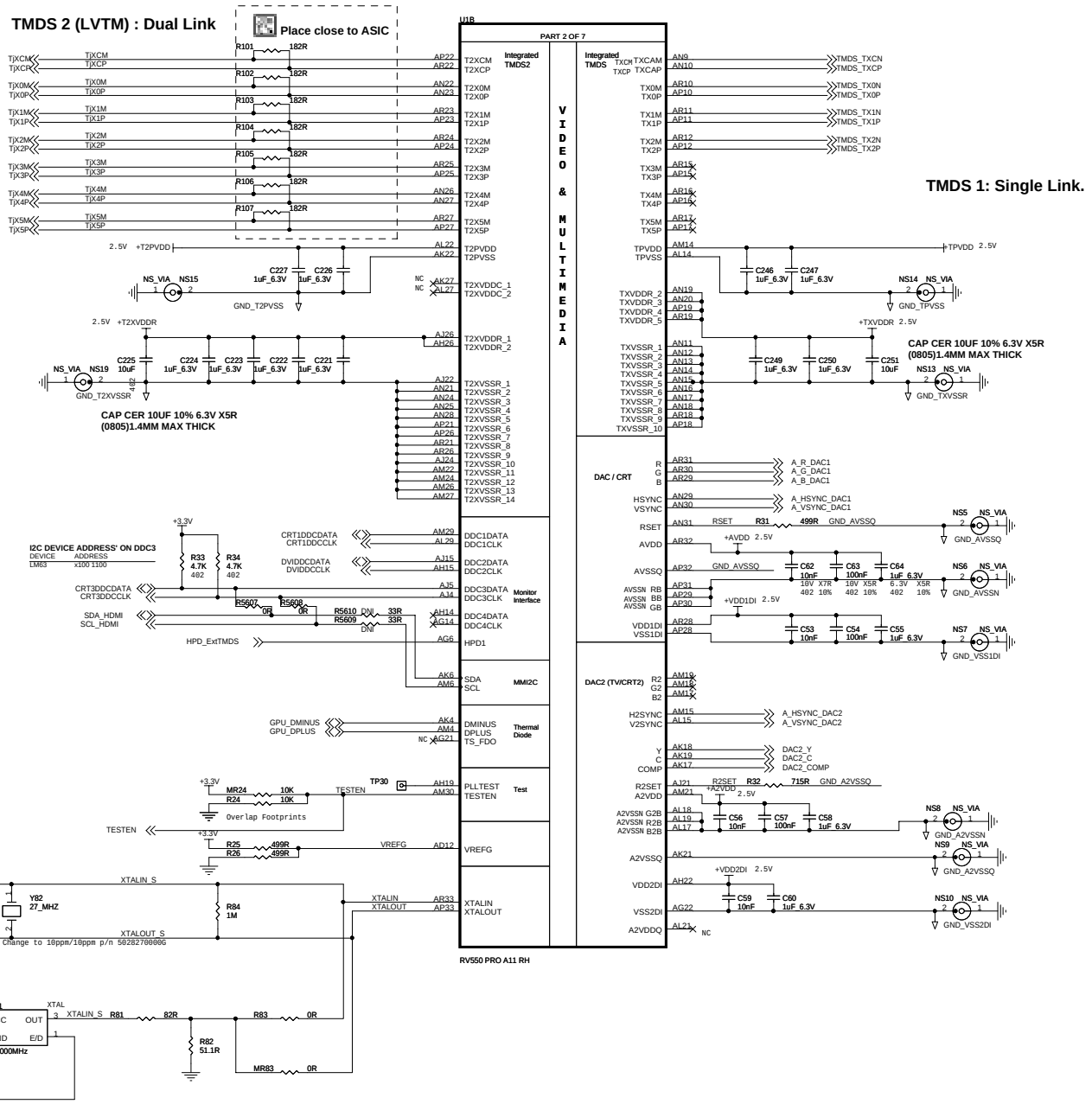
RV550: LVTM (TMDS2) is dual link, the other TMDS (TMDS1) interface is single-link only.



Place R_RTCLK close to XTAL so the main clock line has shortest stub

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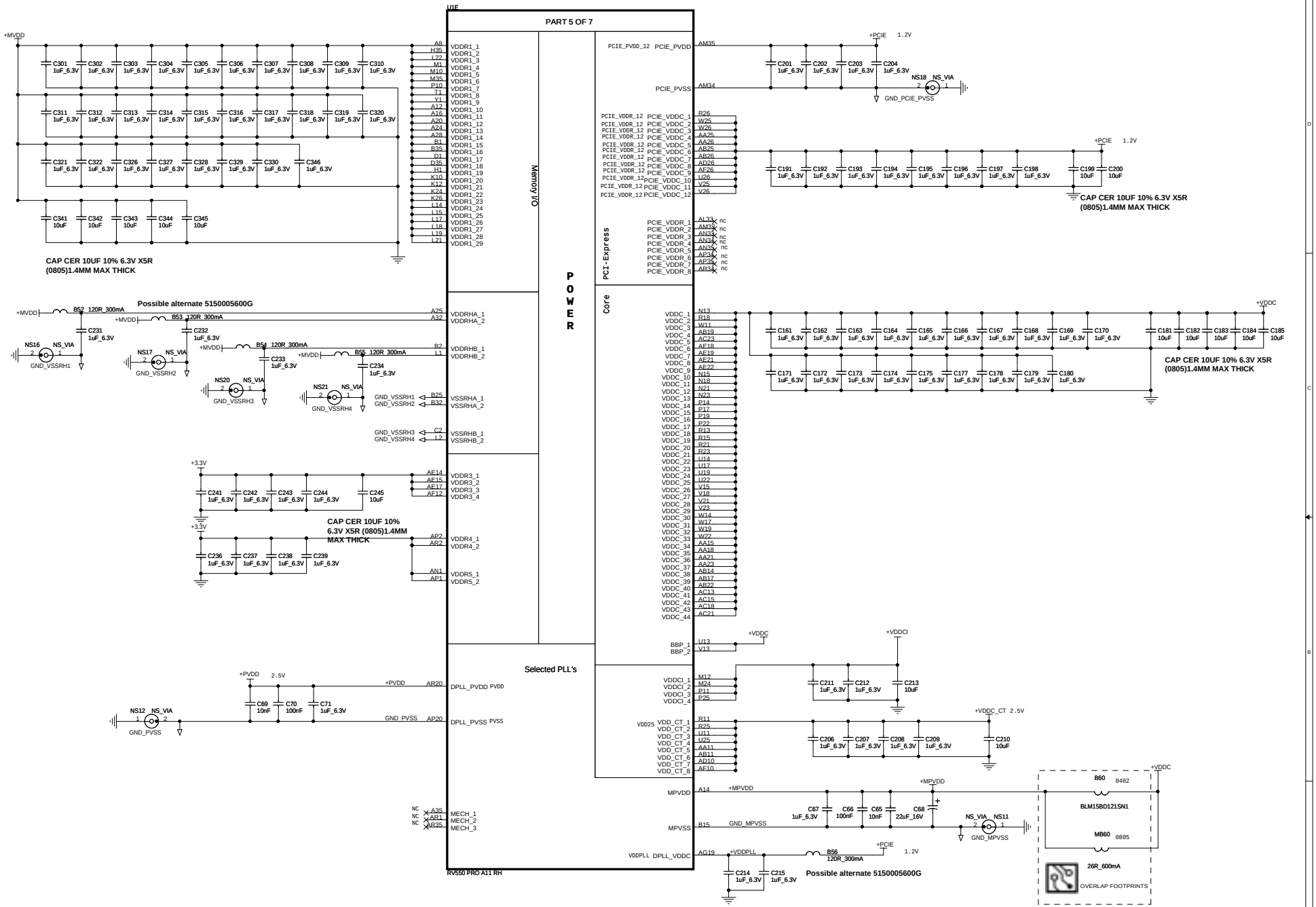

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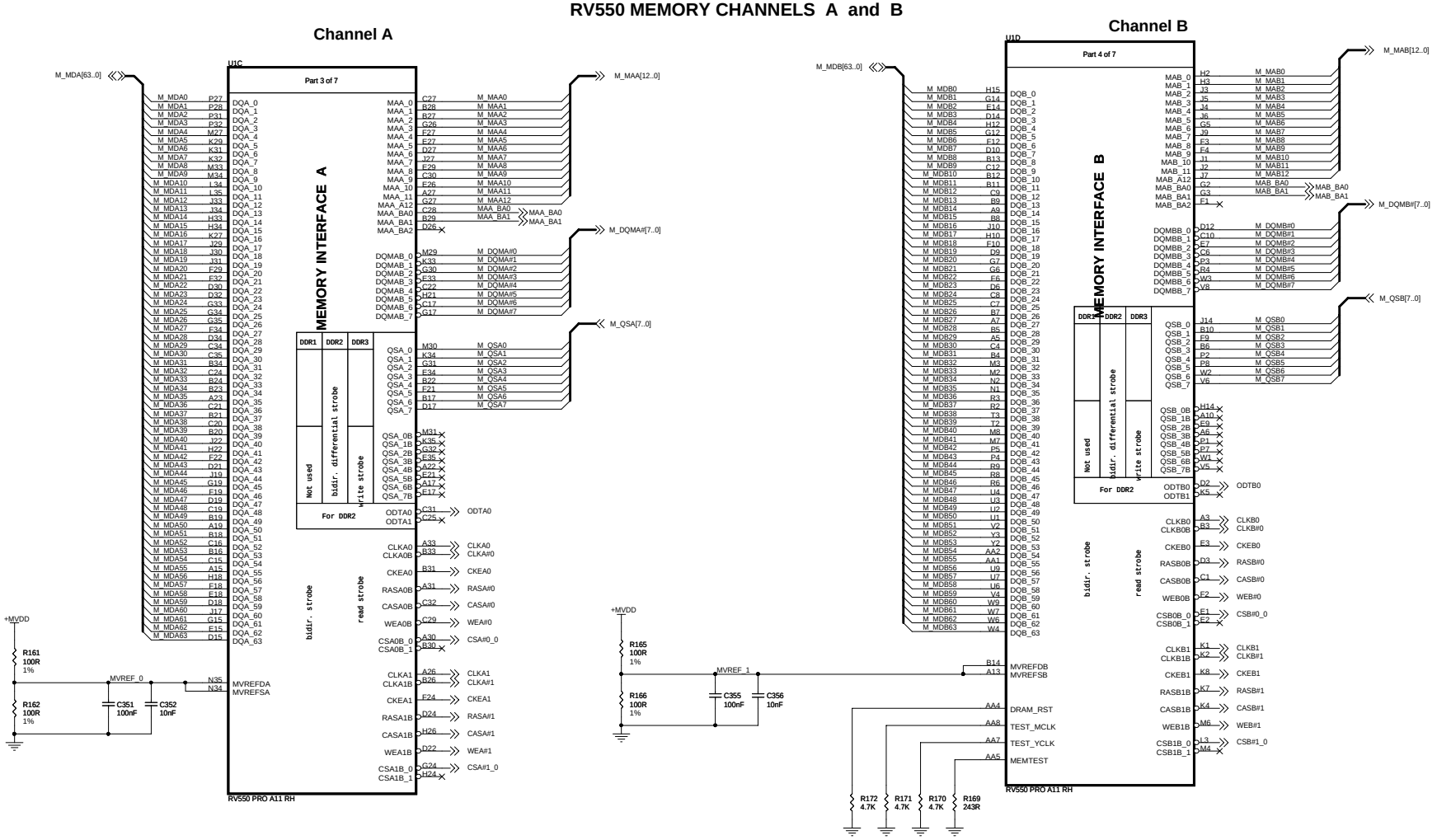
RV550 MEMORY CHANNELS A and B



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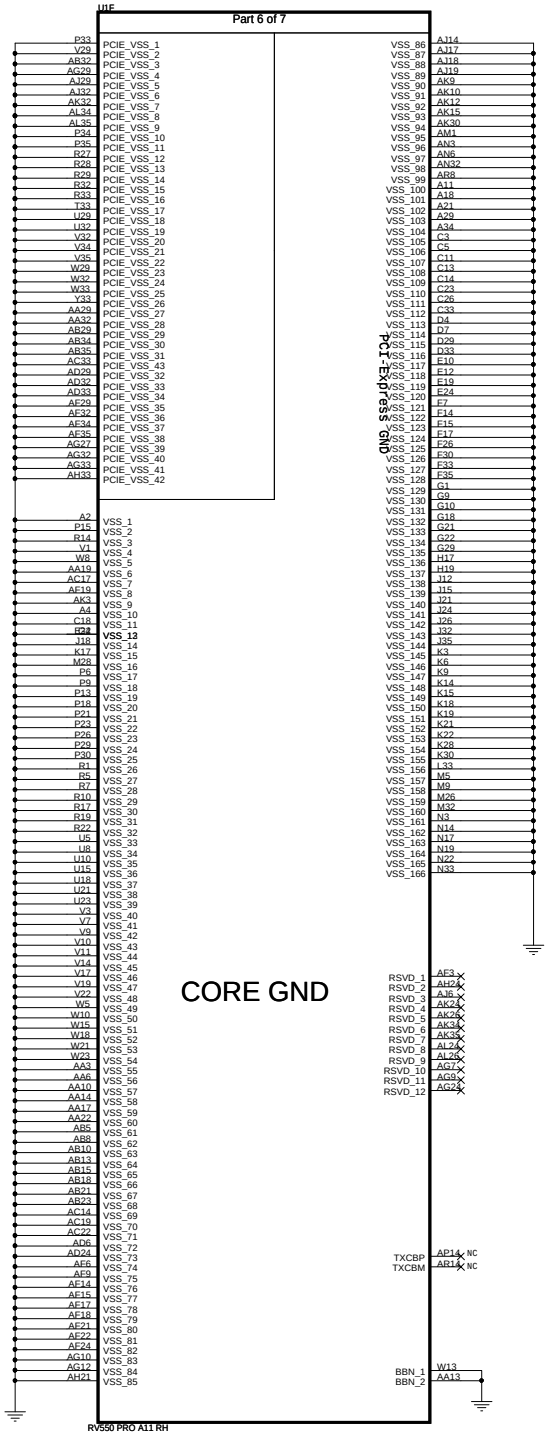

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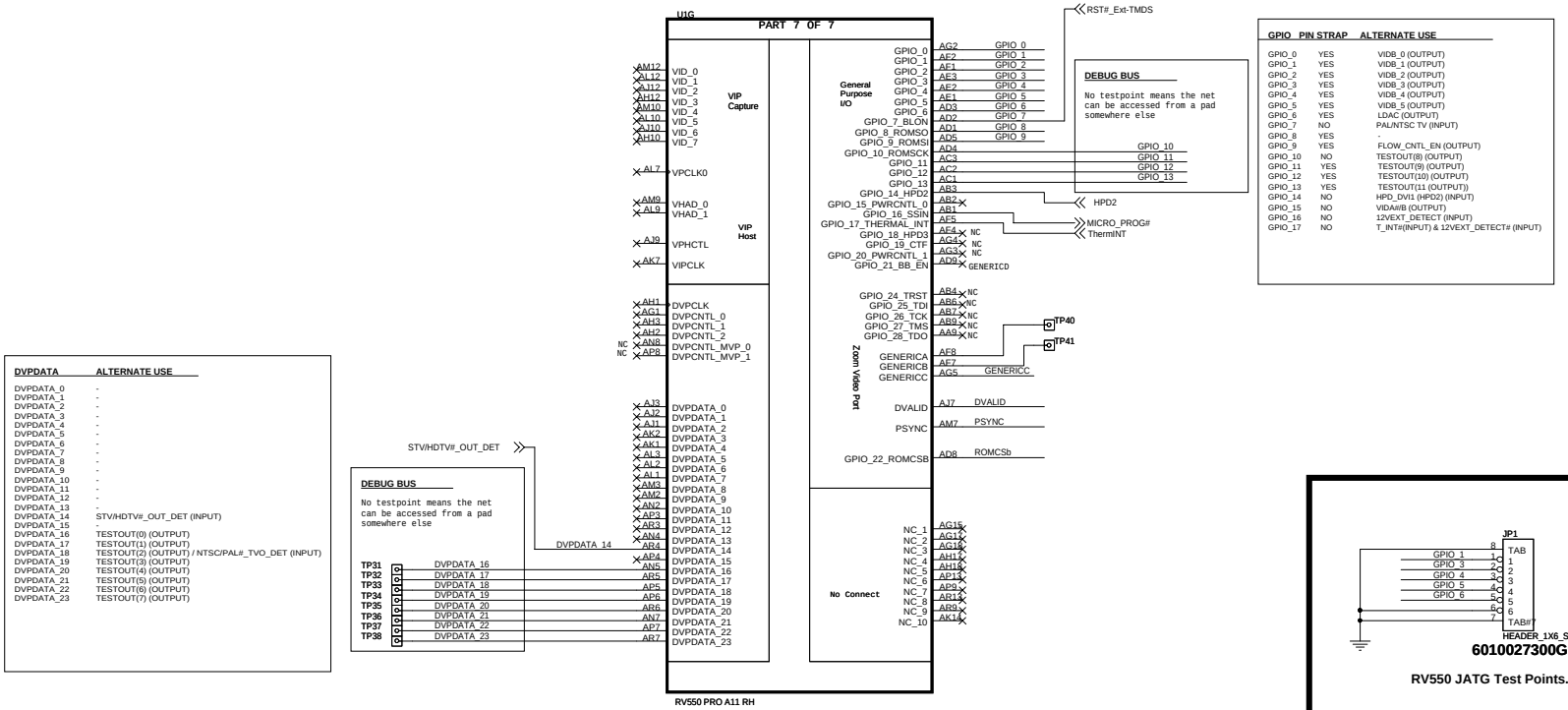
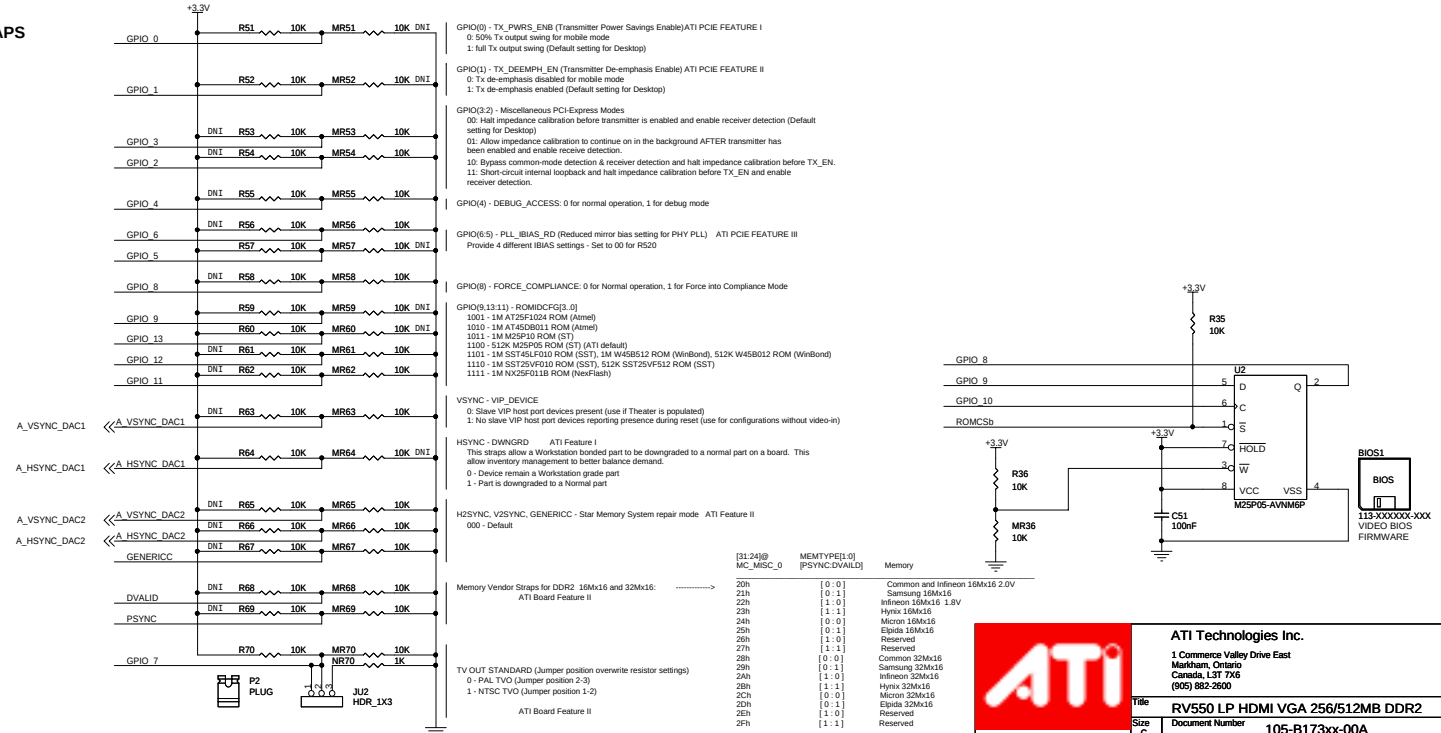


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDA#/B (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

DVPDATA	ALTERNATE USE
DVPDATA_0	-
DVPDATA_1	-
DVPDATA_2	-
DVPDATA_3	-
DVPDATA_4	-
DVPDATA_5	-
DVPDATA_6	-
DVPDATA_7	-
DVPDATA_8	-
DVPDATA_9	-
DVPDATA_10	-
DVPDATA_11	-
DVPDATA_12	-
DVPDATA_13	-
DVPDATA_14	STV/HDTV#_OUT_DET (INPUT)
DVPDATA_15	-
DVPDATA_16	TESTOUT(0) (OUTPUT)
DVPDATA_17	TESTOUT(1) (OUTPUT)
DVPDATA_18	TESTOUT(2) (OUTPUT) / NTSC/PAL#_TVO_DET (INPUT)
DVPDATA_19	TESTOUT(3) (OUTPUT)
DVPDATA_20	TESTOUT(4) (OUTPUT)
DVPDATA_21	TESTOUT(5) (OUTPUT)
DVPDATA_22	TESTOUT(6) (OUTPUT)
DVPDATA_23	TESTOUT(7) (OUTPUT)

PIN BASED STRAPS



[31:24]@ MC_MISC_0	MEMTYPE[1:0] [PSYNC:DVALID]	Memory
20h	[0 : 0]	Common and Infineon 16Mx16 2.0V
21h	[0 : 1]	Samsung 16Mx16
22h	[1 : 0]	Infineon 16Mx16 1.8V
23h	[1 : 1]	Hynix 16Mx16
24h	[0 : 0]	Micron 16Mx16
25h	[0 : 1]	Elpida 16Mx16
26h	[1 : 0]	Reserved
27h	[1 : 1]	Reserved
28h	[0 : 0]	Common 32Mx16
29h	[0 : 1]	Samsung 32Mx16
2Ah	[1 : 0]	Infineon 32Mx16
2Bh	[1 : 1]	Hynix 32Mx16
2Ch	[0 : 0]	Micron 32Mx16
2Dh	[0 : 1]	Elpida 32Mx16
2Eh	[1 : 0]	Reserved
2Fh	[1 : 1]	Reserved

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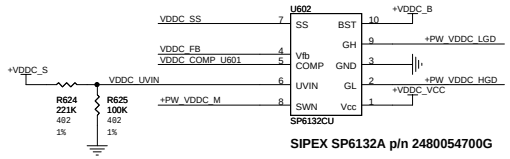
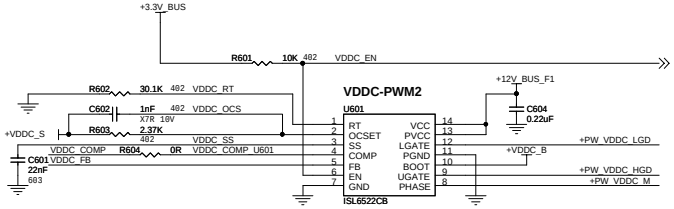
VDDC-PWM1



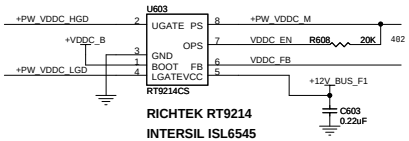
SIPEX SP6132A p/n 2480054700G

VDDC-PWM2



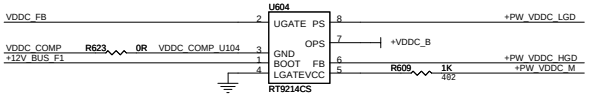
INTERSIL ISL6522/ISL6535
RICHTEK RT9232/RT9232A
ANPEC APW7062A
ANPEC APW7062B

VDDC-PWM3



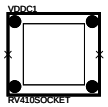
RICHTEK RT9214
INTERSIL ISL6545

VDDC-PWM4

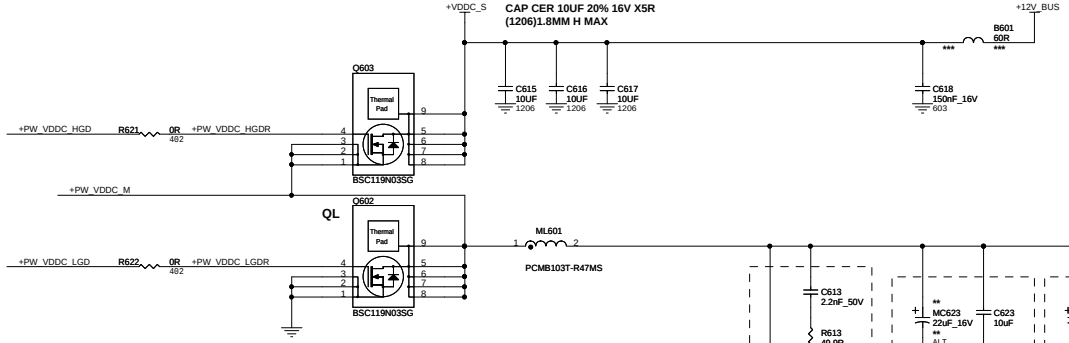


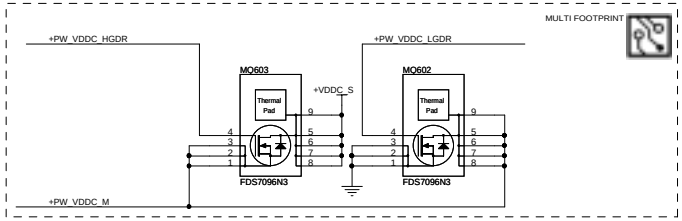
ANPEC APW7061A

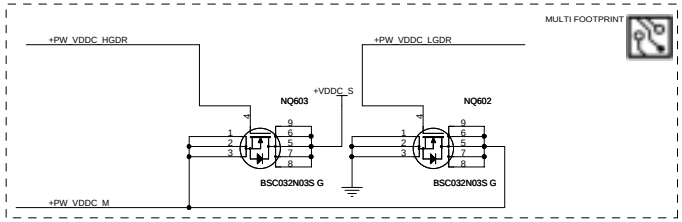
This symbol is used for 103 SMPS p/n.



VDDC_EN R614 0R 402 VDDC_COMP





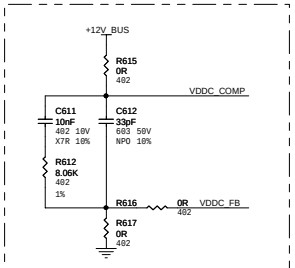


Regulator for VDDC (ASIC Core)

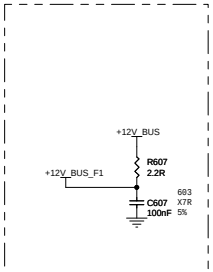
Vout = 1V ~ 1.3V

Part	Vout	R1	R2
0.8V Ref	1.2V	1.00K 1%	2.00K 1%
	1.25V	1.00K 1%	1.78K 1%
	1.3V	1.00K 1%	1.6K 1%

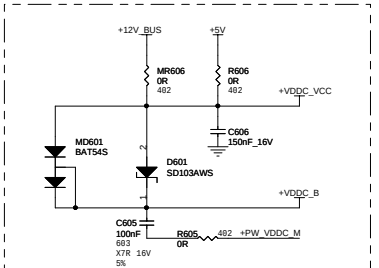
COMPENSATION CIRCUIT



FILTERED +12V_BUS



BOOT CIRCUIT



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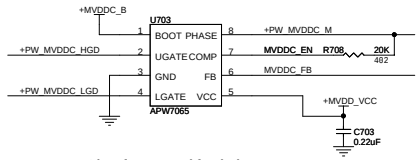
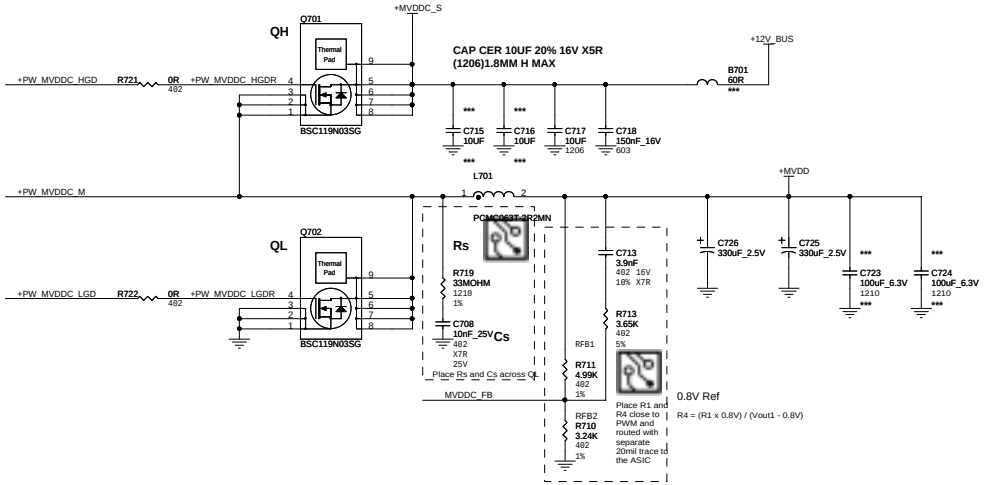


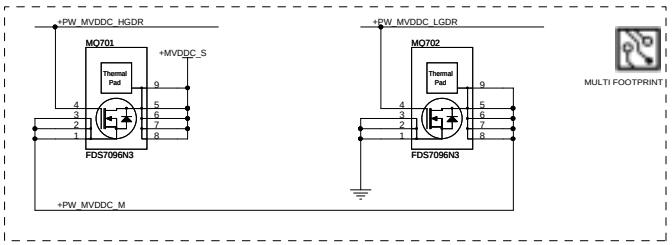
List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7120/APW7065 (12V)
CAT CAT7583 (12V)
INTERSIL ISL6545
NEXSEM NX2114/2307
RICHTEK RT9214/RT8101
OnSemi ON1582



RC snubber values shown are for reference only, tuning is required



SMPS02- Regulator for MVDD

Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G

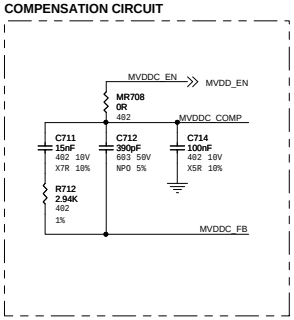
Layout guideline for Nexsem NX2114/2307

1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

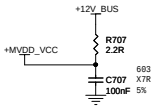
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

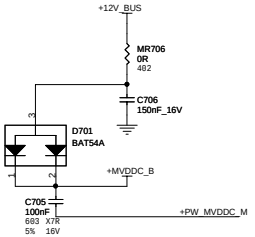
COMPENSATION CIRCUIT



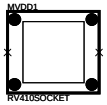
FILTERED SMPS VCC



BOOT CIRCUIT



This symbol is used for 103 SMPS p/n.



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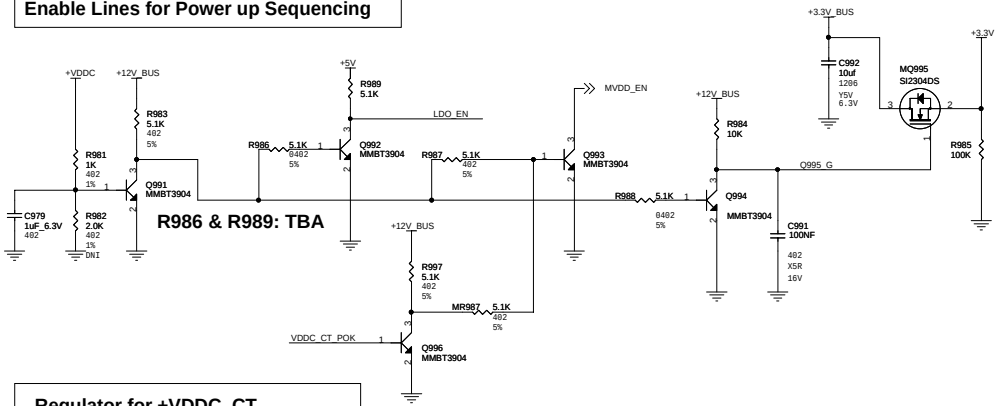
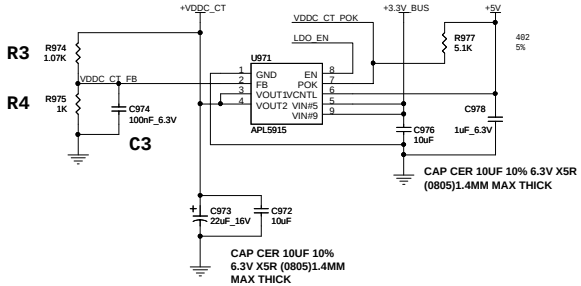
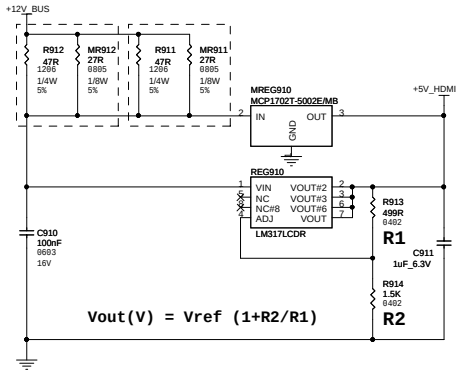
Enable Lines for Power up Sequencing

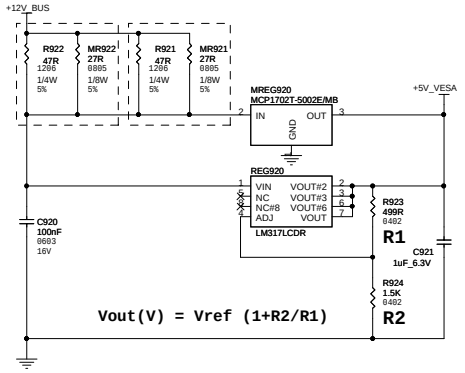


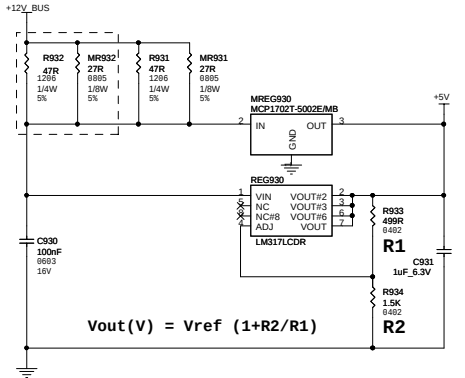
Regulator for +VDDC_CT
Vout = 2.8V +/- 1.5%

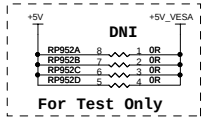


Regulators for +5V, +5V_VESA and +5V_VESA2

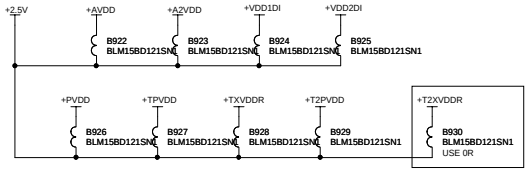


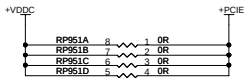


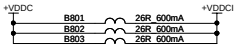




Shared Power Rails







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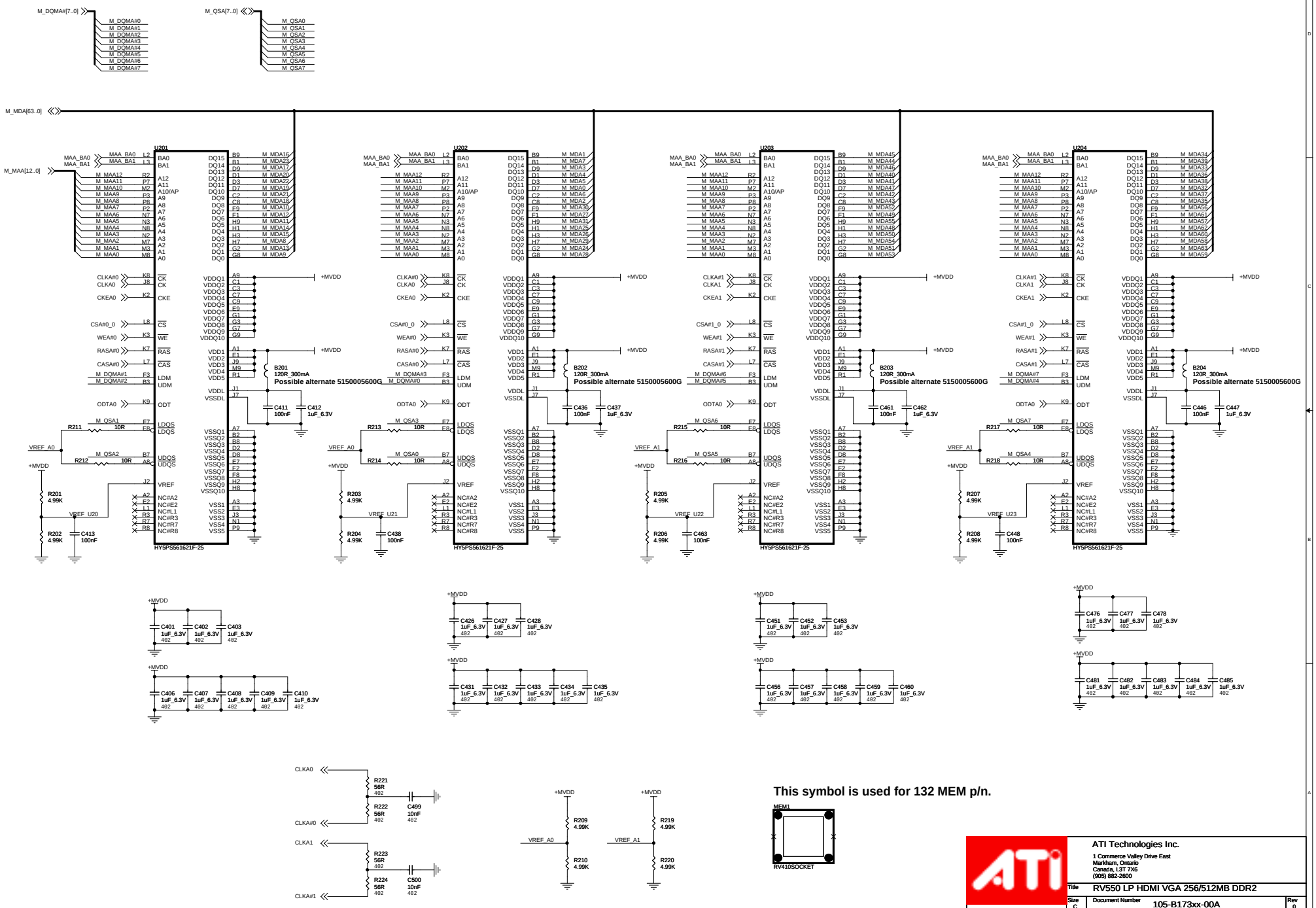
CHANNEL A: RANK 0 128MB DDR2



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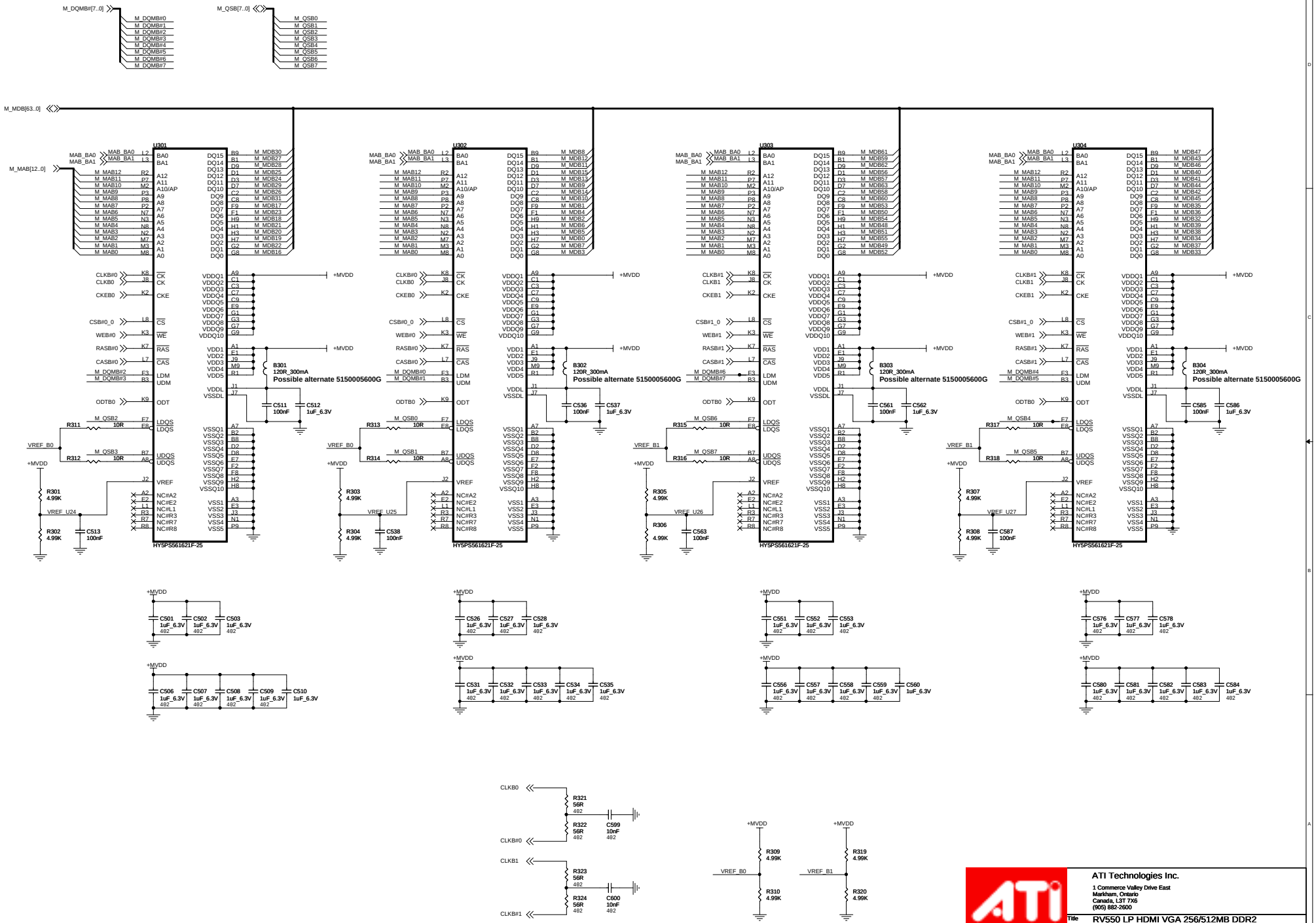
CHANNEL B: RANK 0 128MB DDR2



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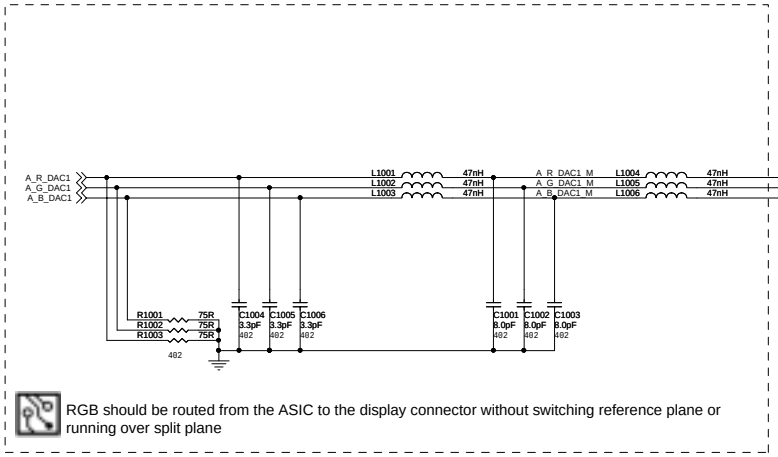
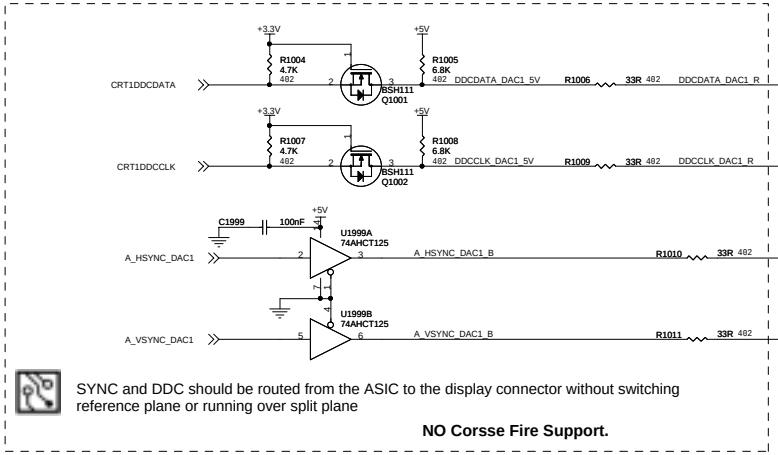
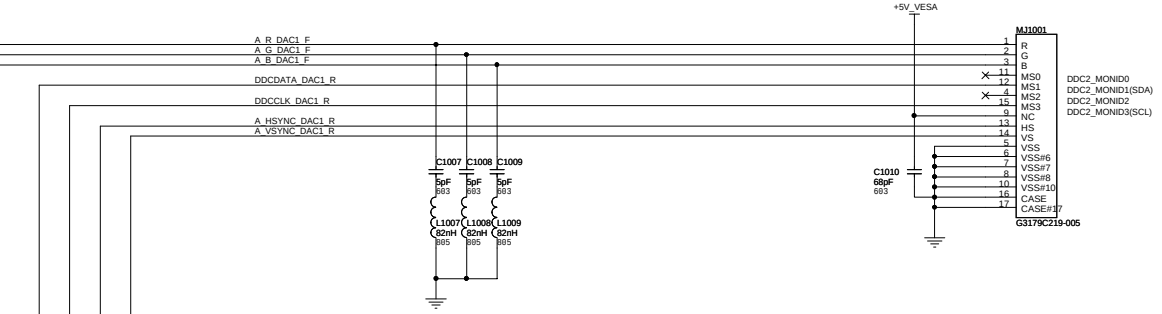


RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane



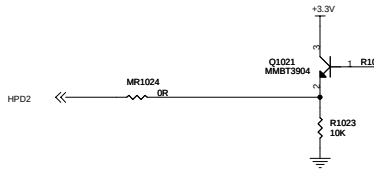
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

NO Corsse Fire Support.

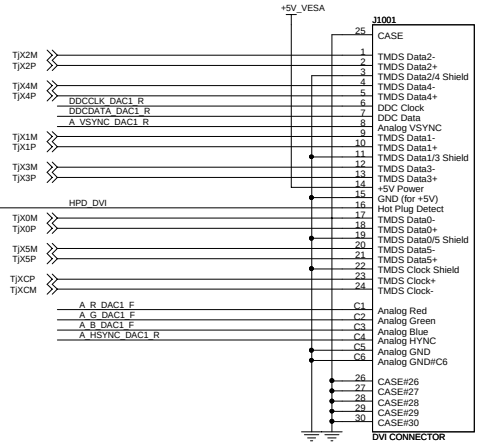


DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

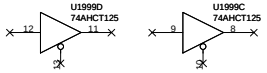
Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



These resistors can be placed close to the ASIC so single net is needed



Spares



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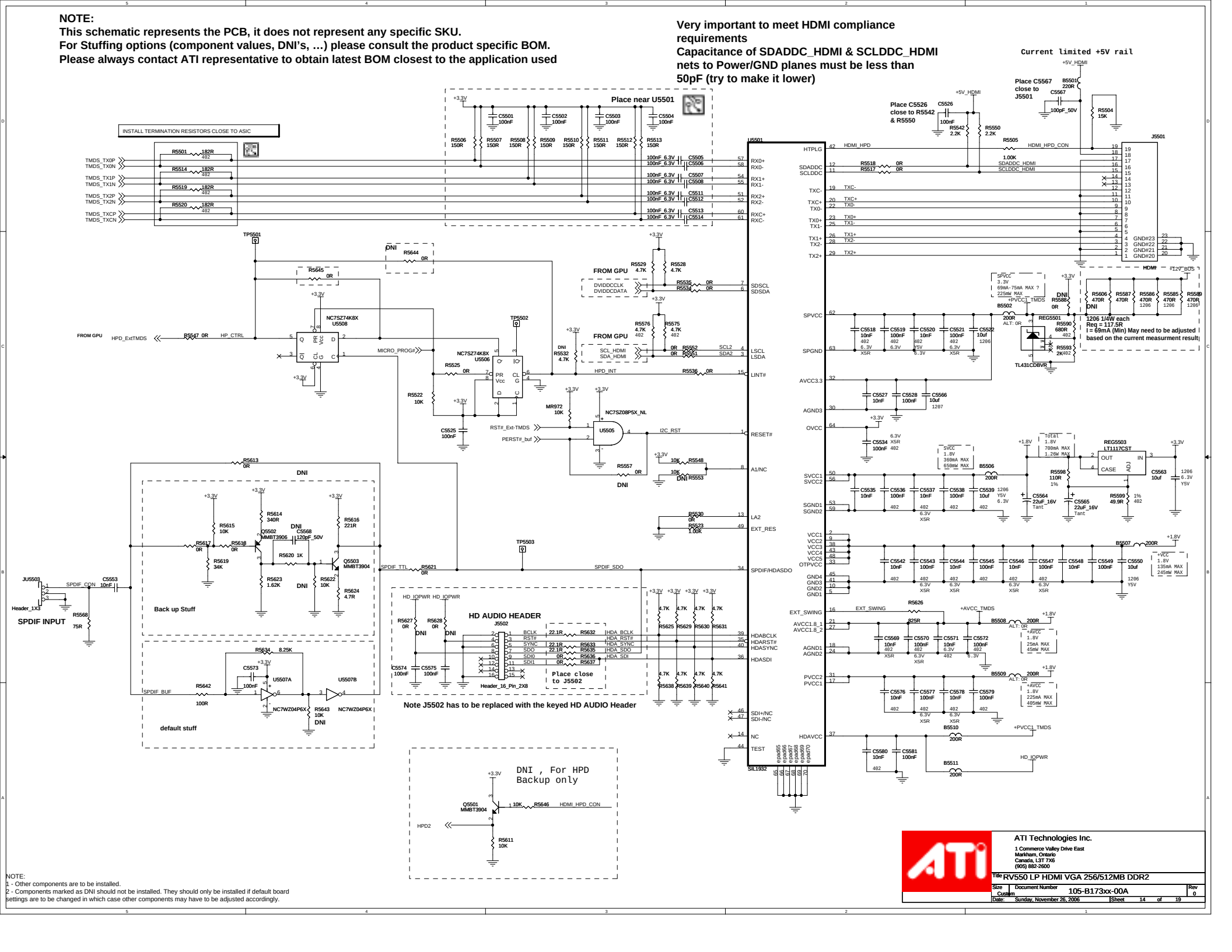
NOTE:
This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI's, …) please consult the product specific BOM.
Please always contact ATI representative to obtain latest BOM closest to the application used

Very important to meet HDMI compliance requirements
Capacitance of SDADDC_HDMI & SCLDDC_HDMI nets to Power/GND planes must be less than 50pF (try to make it lower)



NOTE:
1 - Other components are to be installed.
2 - Components marked as DNI should not be installed. They should only be installed if default board settings are to be changed in which case other components may have to be adjusted accordingly.

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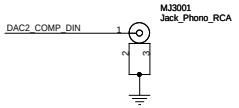
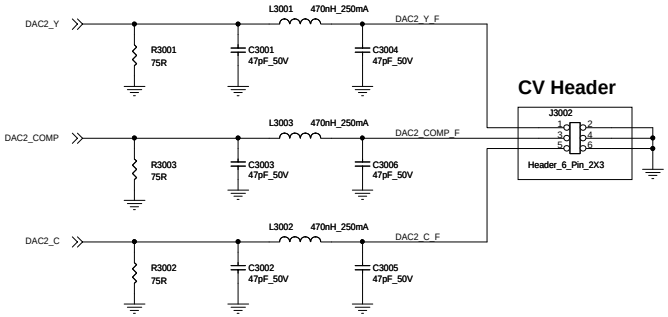
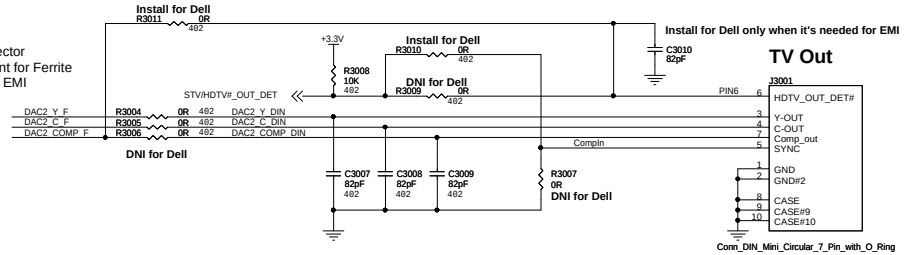




Place near connector
0R leaves footprint for Ferrite Beads if req'd for EMI



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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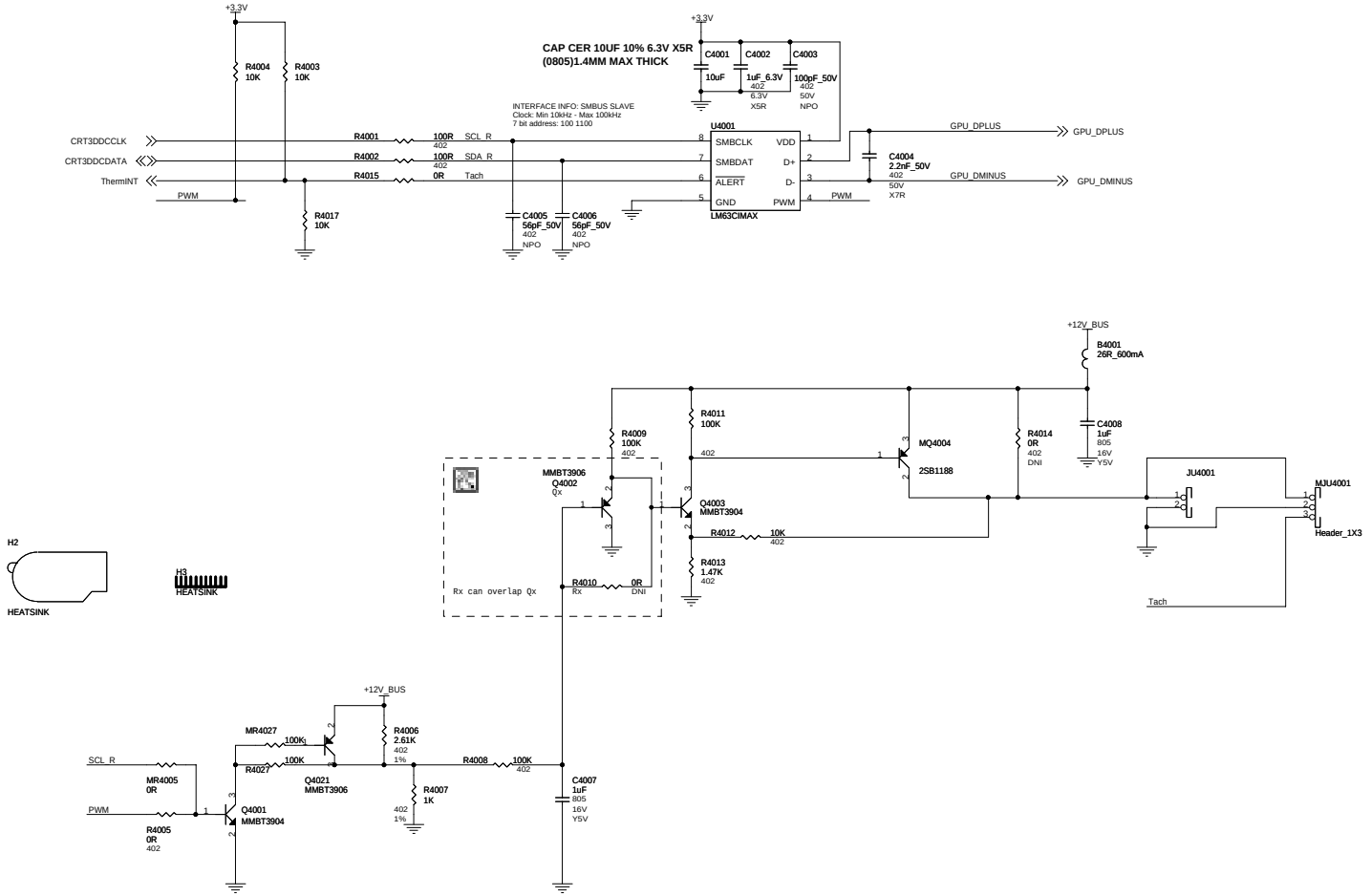

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DVI/VGA SCREWS

ASSY-SCREW1
SCREW
JACKSCREW
ASSY
7020000800

ASSY-SCREW2
SCREW
JACKSCREW
ASSY
7020000800

ASSY-SCREW5
SCREW
PAN_HEAD
7020001700

ASSY-SCREW3
SCREW
JACKSCREW
ASSY
7020000800

ASSY-SCREW4
SCREW
JACKSCREW
ASSY
7020000800

MT1
MT_Hole_0.136_in.
DNI

MT2
MT_Hole_0.136_in_6VIA
DNI

PCB1
PCB
109-41500-20

HDMI1
PCB
109-41500-20

REG1
PCB
109-41500-20

REG2
PCB
109-41500-20

ASSY1
BRACKET
LP
8020040000
HDMI +VGA LP

ASSY2
BRACKET
8020039900
HDMI +VGA

SK1
SOCKET
6090023700

M71 M package.
Make sure Rv550 can use it. 6090023700

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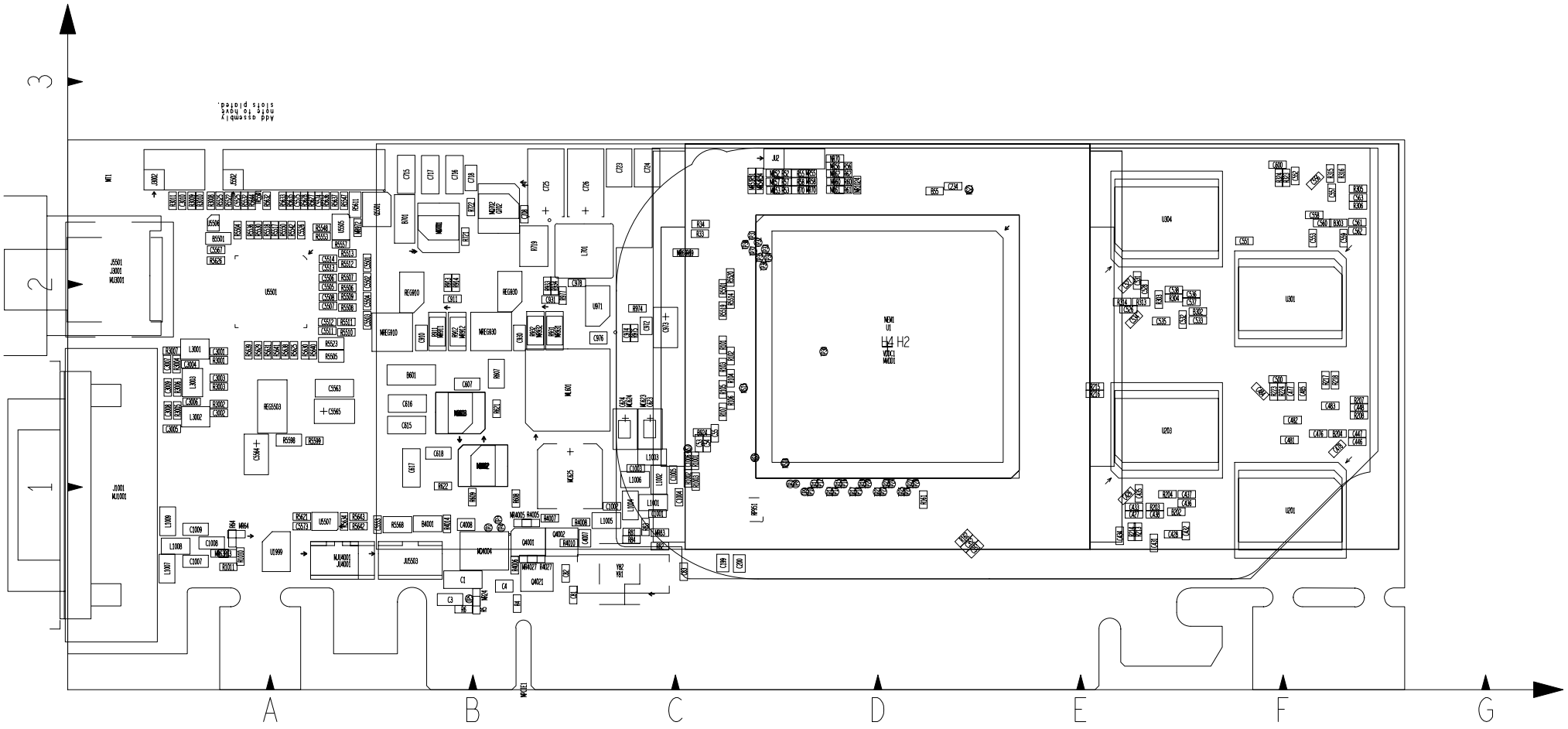
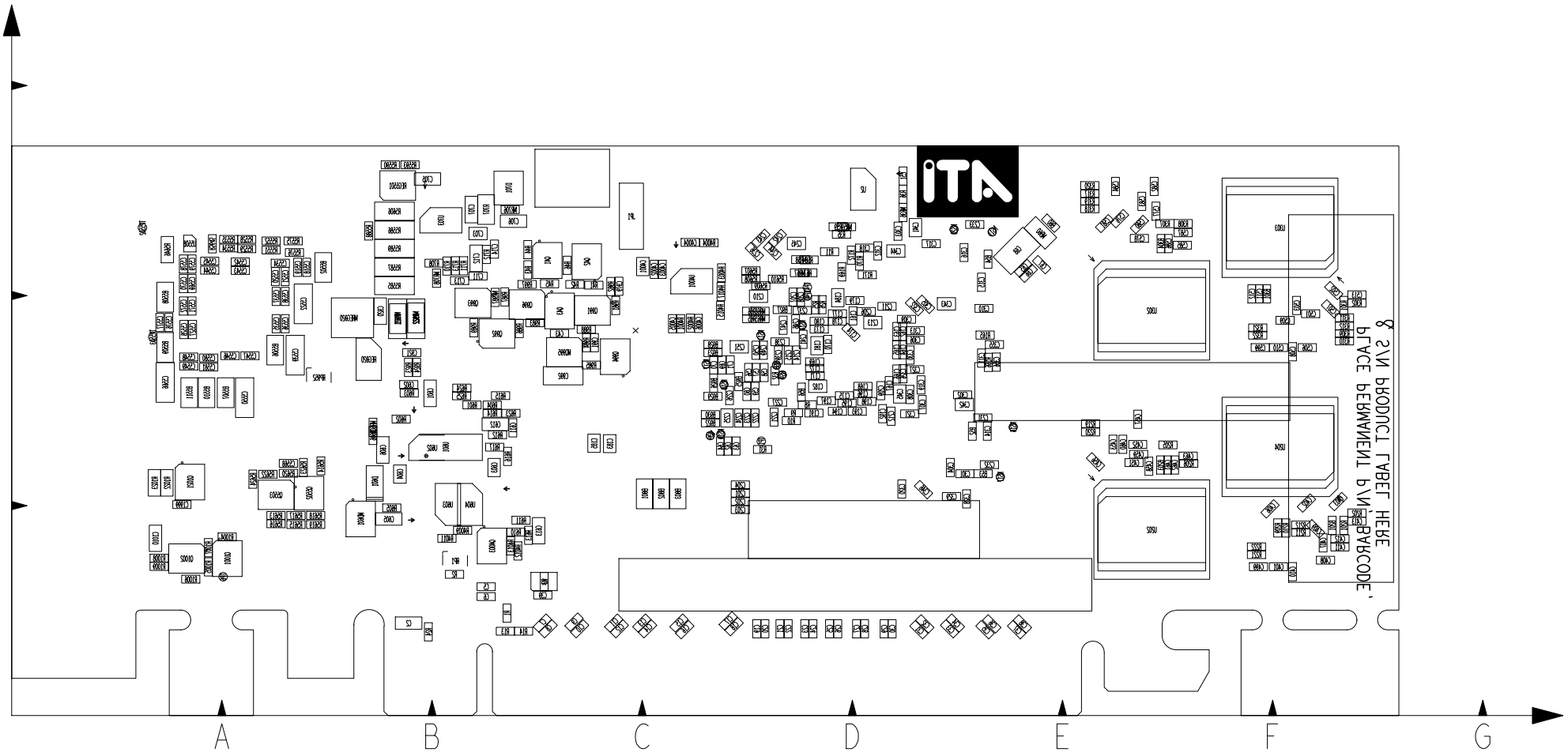


RH RV550 512MB DDR2 HDMI VGA LP 8 (Cristal-lite)
PN 109-B17331-00A
NOV. 22, 2006 ASSEMBLY TOP
DESIGNER DORINA A.\SVETLANA O. SHEET 1 OF 2



RH RV550 512MB DDR2 HDMI VGA LP 8 (Cristal-lite)
PN 109-B17331-00A
NOV. 22, 2006
DESIGNER DORINA A.\SVETLANA O.

ASSEMBLY BOTTOM
SHEET 2 OF 2