MS-V088 VER 10

NV43-PCIE NV43 256MB/128bit, BGA 16MX16 DDR2,VGA,DVI-I,TV-OUT(HT-10)

P295-A00 DESIGN NV43 300/267MHZ 128MB/256MB/512MB DDR2 84-FBGA

PAGE SUMMARY:

DDR2 84-FBGA Clock setting 350MHZ

Page1: P295 Overview

Page2: PCI EXPRESS, NVVDD, VDD33

Page3: FB BANK A, FBVTT TERMINATIONS, FBVDDQ DECOUPLING

Page4: FB BANK C, FBVTT TERMINATIONS

Page5: MEMORY PARTITION A 0..31

Page6: MEMORY PARTITION A 32..63

Page7: MEMORY PARTITION C 0..31

Page8: MEMORY PARTITION C 32..63

Page9: GPU GND

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Page11: DACB - TVOUT, VIDEO IN

Page12: DACC - VGA

Page13: STRAPS, FANSINK, MECHANICALS

Page14: GPIO, HDCP ROM, VBIOS ROM, FAN CONTROL

Page15: INTERNAL TMDS LINK A/B

Page16: INTERNAL TMDS LINK C/D

Page17: MIOA, MIOB, NVPLL

Page18: POWER SUPPLY (RT9218) for NVVDD,FBVDDQ

Page19: Other Powers - A3V3, DDC_5, TMDSPLL, TMDSIO, FBVTT and 5V-3V3 POWER SEQUENCING

BOM	VARIANT	NVPN	ASSEMBLY
B	BASE	602-10295-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	602-10295-0000-000	GF-6600-A04 GEN 300/267MHZ 256MB 84-FBGA DDR2 16MX16 VGA+DVI-I+HDTV
2	SKU001	602-10295-0001-000	GF-6600-A04 GEN 300/267MHZ 128MB 84-FBGA DDR2 8MX16 VGA+DVI-I+HDTV
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

REV HISTORY

A00
-08/04/2005:

1.Page18: change power solution to RT9218 for NVVDD & FBVDDQ

10S
-08/04/2005:

1.Page18: Move C913~C916 out form C910,C911 & Move C930,C931 out form C929

2.Page19: Add C940 near C36

3.Page19: Remove C16, C35, C55

B00
-12/06/2005:

1.ADD G73 circuit

C00
-04/26/2006:

1.Remove NV43 reserve circuit

2.Page14: Add SPDIF circuit

3.Page15: Add TMDS Dual_Link A/B

4.Page17: Add MIOA Feature SLI CON

5.Page18,19: Modify Power solution same as P345

C01
-06/26/2006:

1.Page18:Add MIOA SLI referenc power

2.Page18:Add R0805 NVVDD to PEX1V2

3.Page18:Add NVVDD Choke Footprint

4.Page15/16:Add Bridge R for EMI

AOO
-11/10/2006:V041-3.1 change model name to V088-0A

1.Page17:MIOA/B SLI signals resverve

2.Page13:Straps reserve for G84

3.Page10/11/12:Reserve DAC_VREF for G84 DAC

4.Page3/4:Reserve FBIO ODT for G84 DDR2

5.Page3/4:Reserve FBIO External VREF for G84

6.Page3/4/5/6/7/8:Reserve FBIO Dual Rank Inplementation for G84

7.Page3/4/14:Reserve I/O changes for G84

8.Page3/9/15/16/19:Reserve Power rail for G84

10
-23/01/2007:

1.Page18:change RT9218 power sqence

2.Page18:reserve AWP7120 / RT9218 footprint

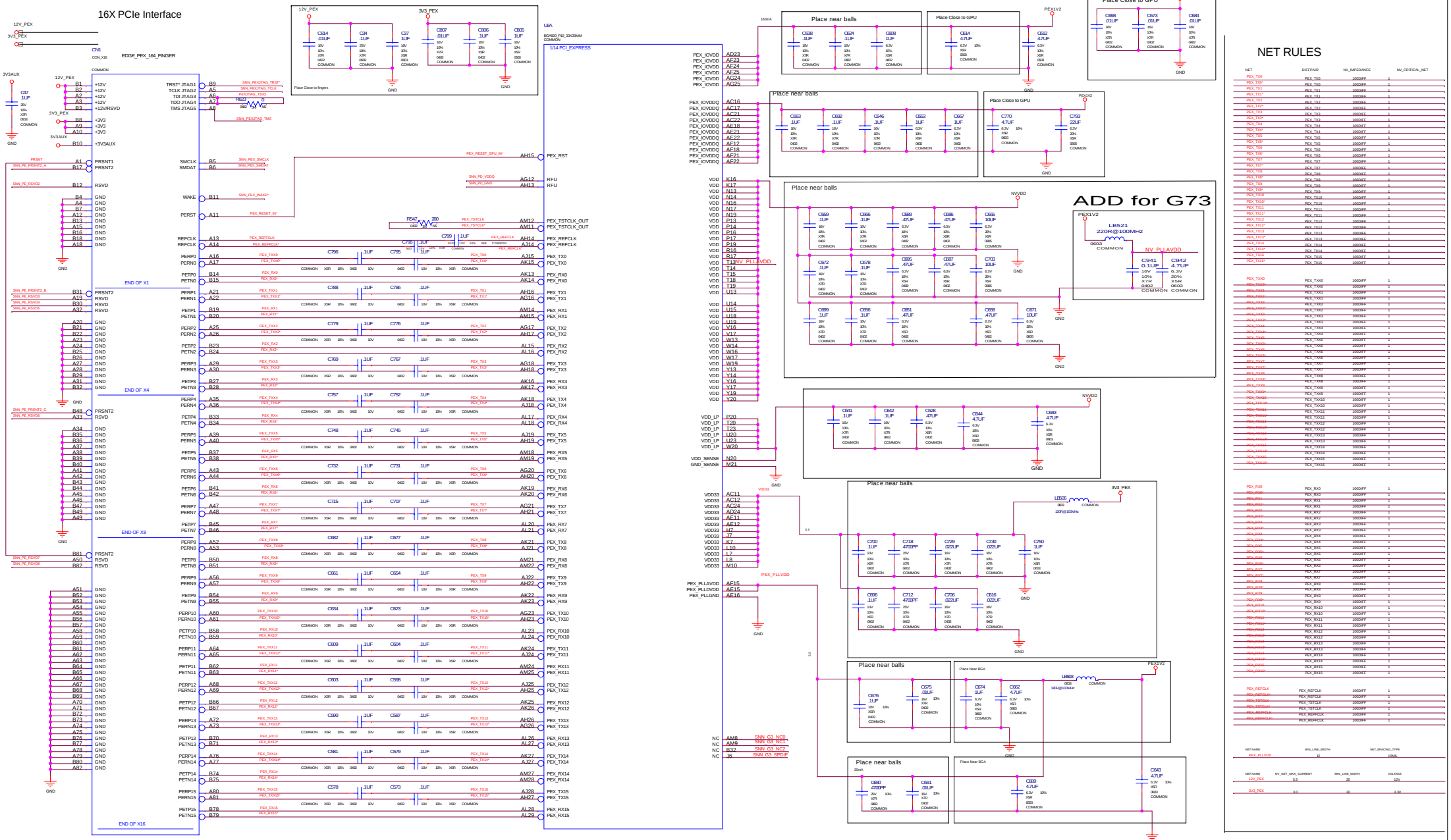
3.Page19:change A2V5 capacitor footprint for A2V5 power issue

4.Page19: change 1V8 431 circuit,using 431+Mos

5.Page5~8: Reserve memory pull high/low R

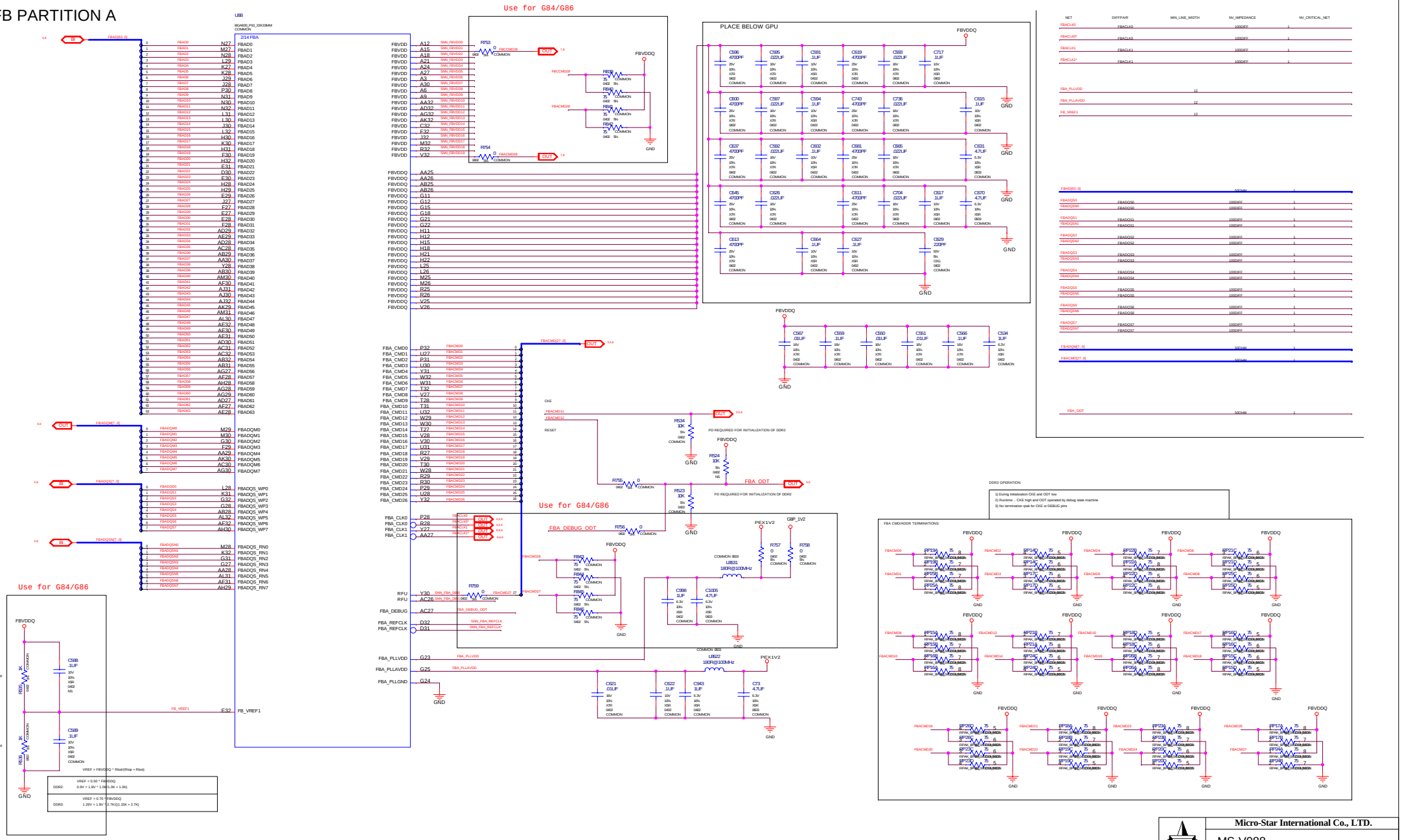
6.Page13: Reserve Heatsink footprint

02 PCI EXPRESS, NVVDD, VDD33



03 FB BANK A, FBVDDQ DECOUPLING

FB PARTITION A



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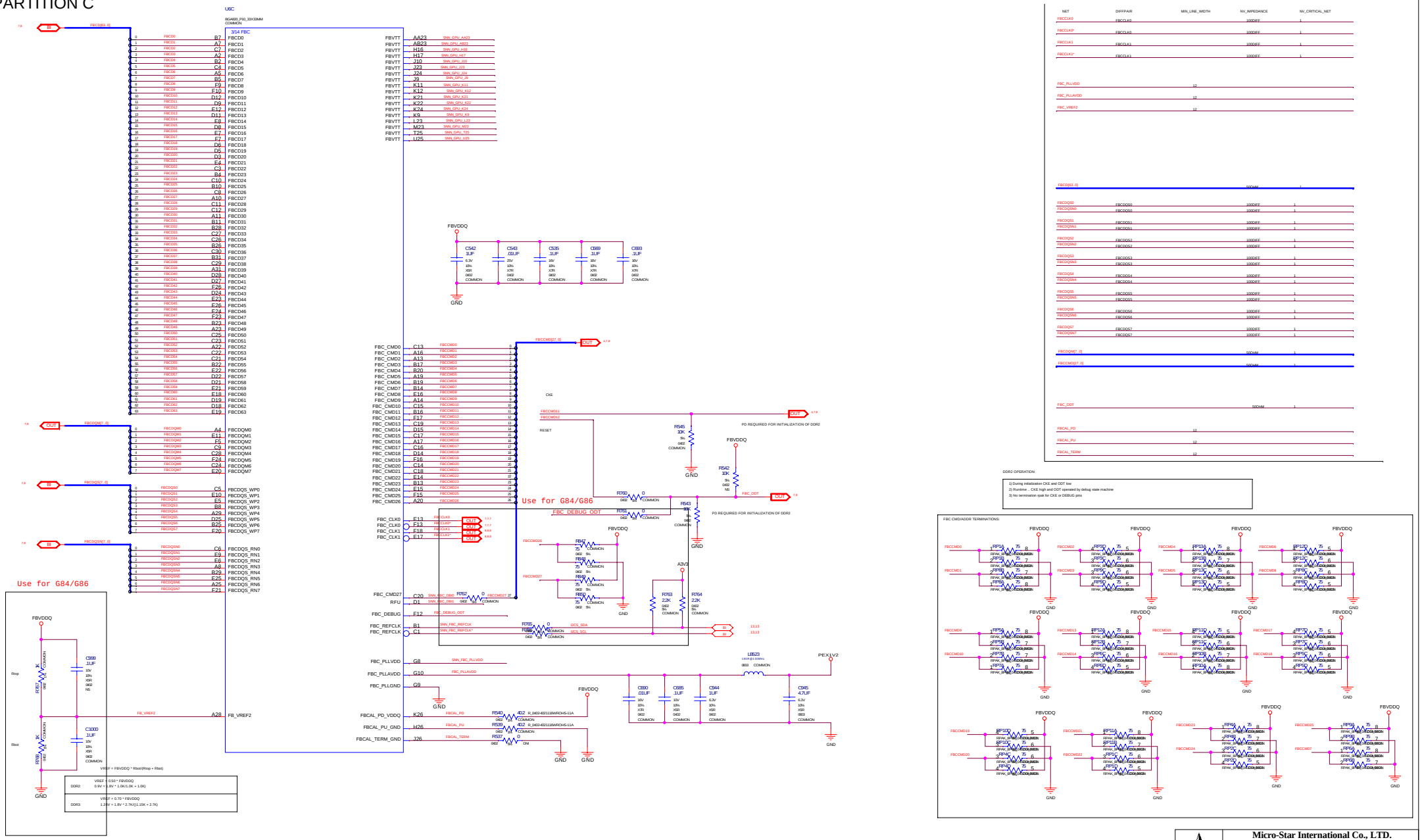
04 FB BANK C, FBVTT TERMINATIONS

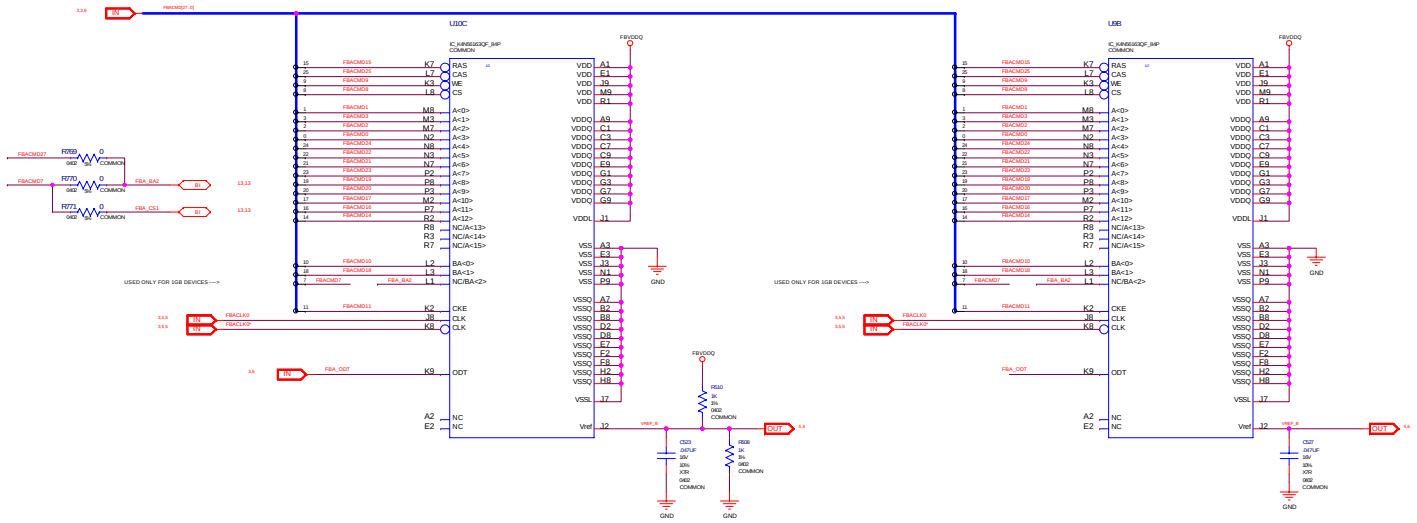
FB PARTITION C

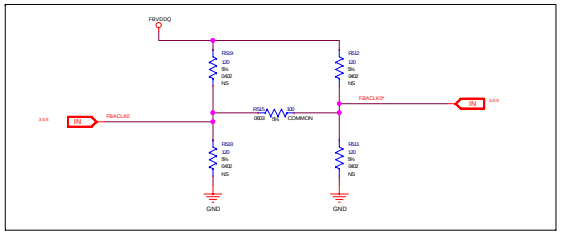


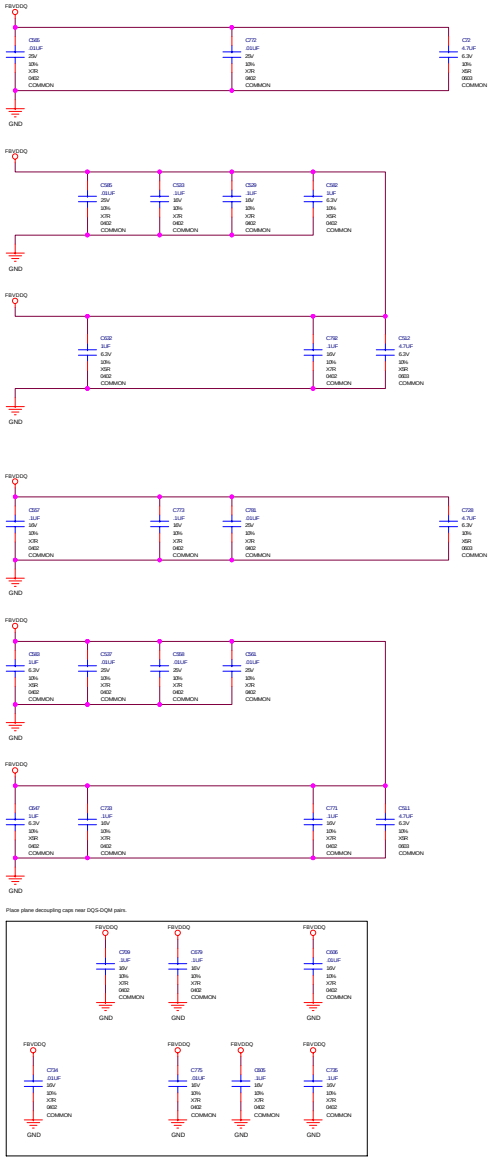
05 MEMORY PARTITION A 0..31

FBA MEMORY 1st bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY







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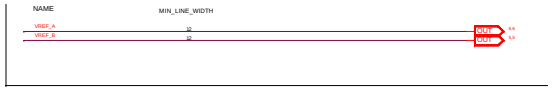
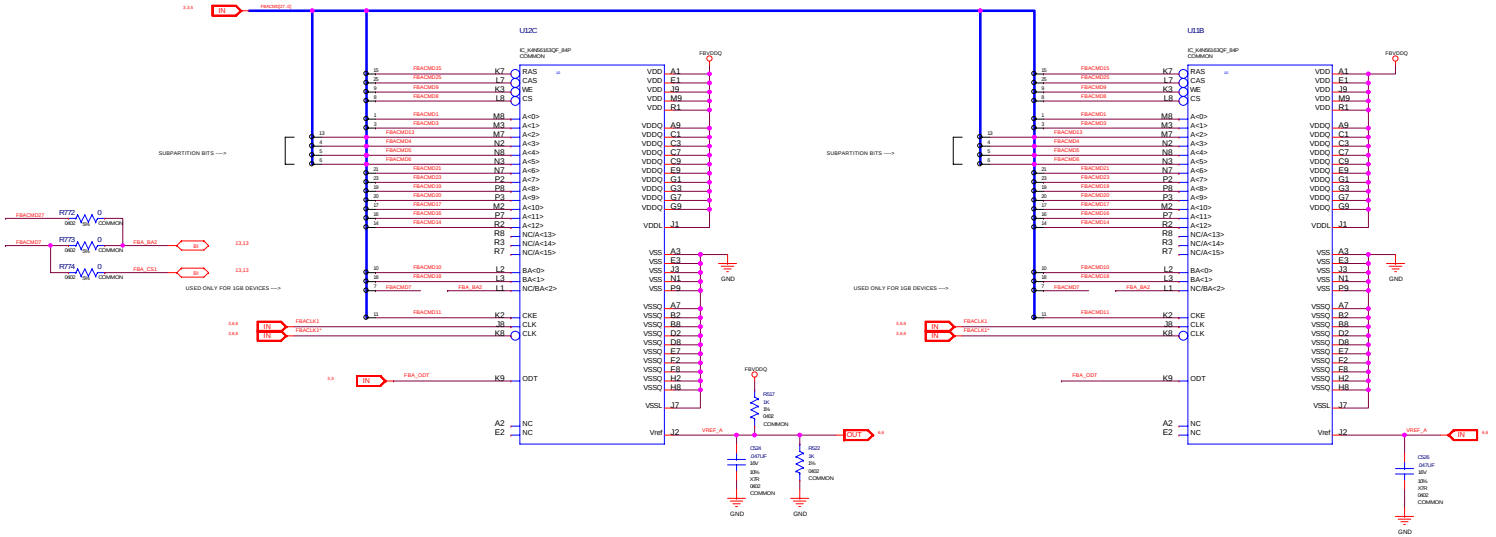
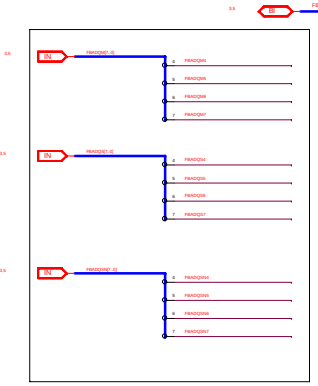
06 MEMORY PARTITION A 32..63

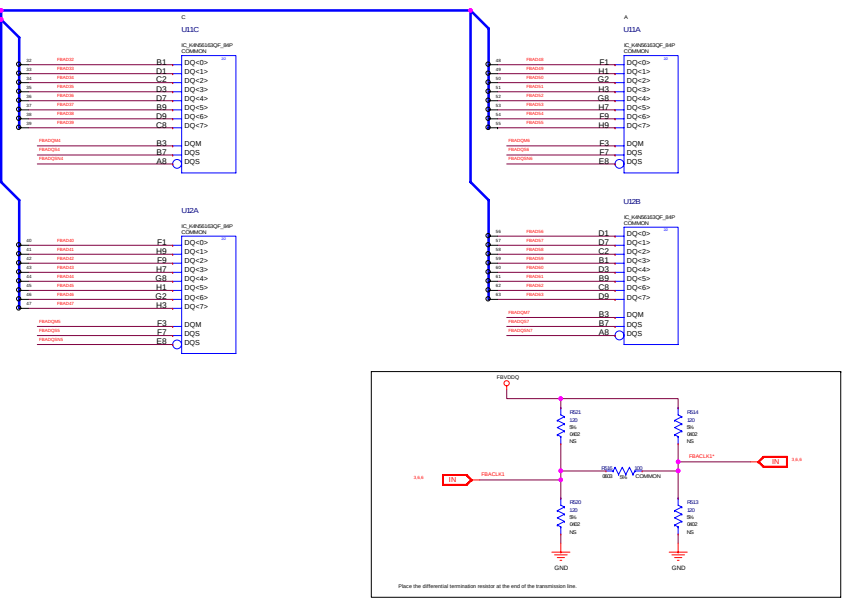
FBA MEMORY 1st bank 32..63

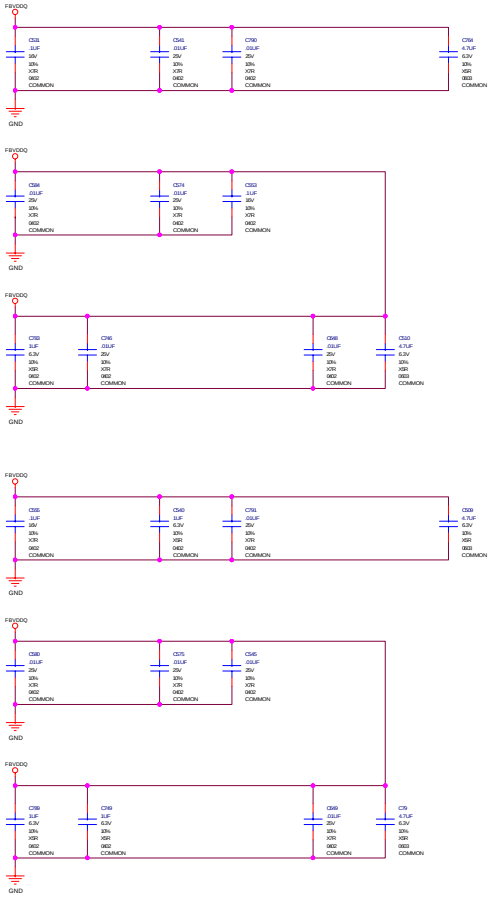
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY











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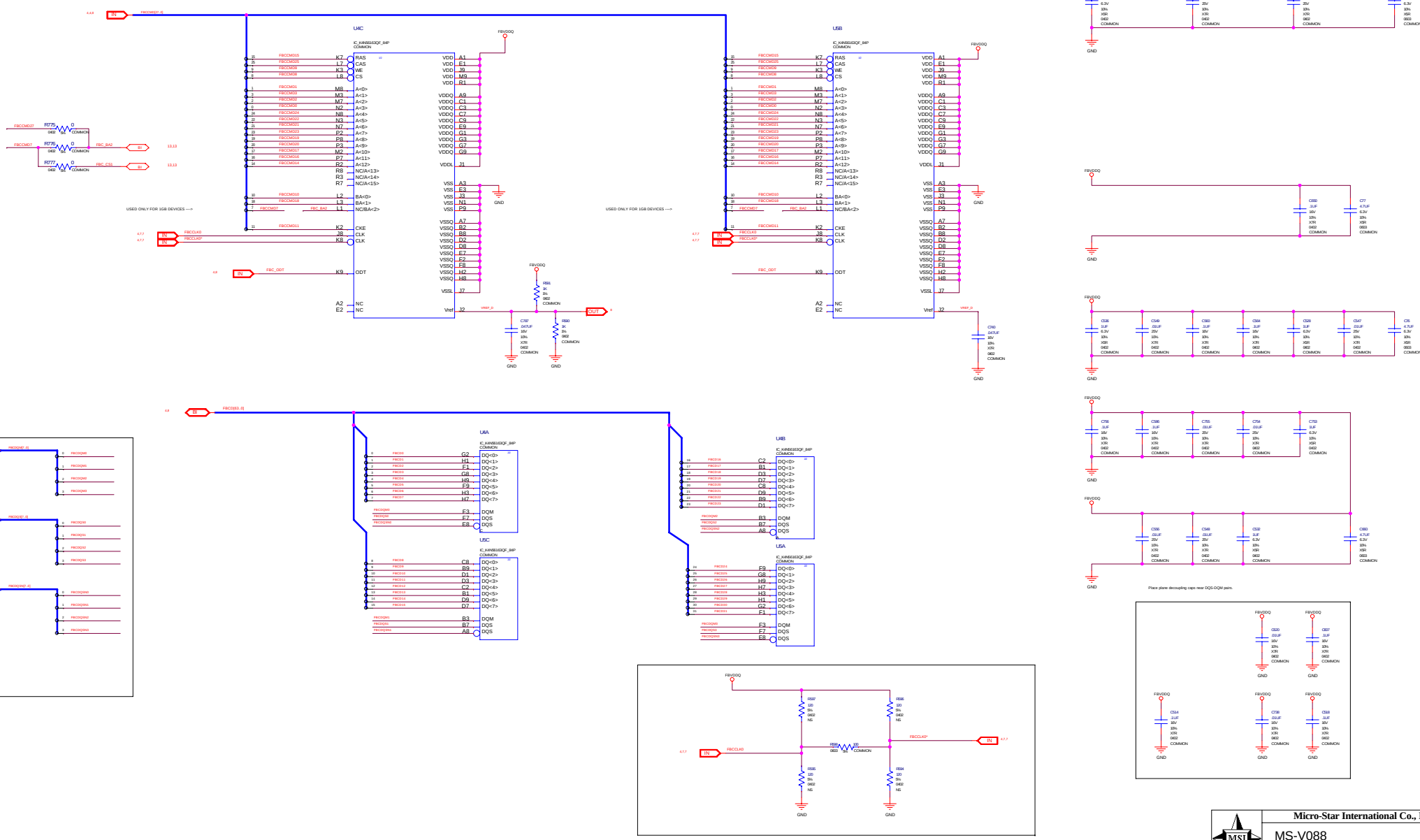
07 MEMORY PARTITION C 0..31

FBC MEMORY 2nd bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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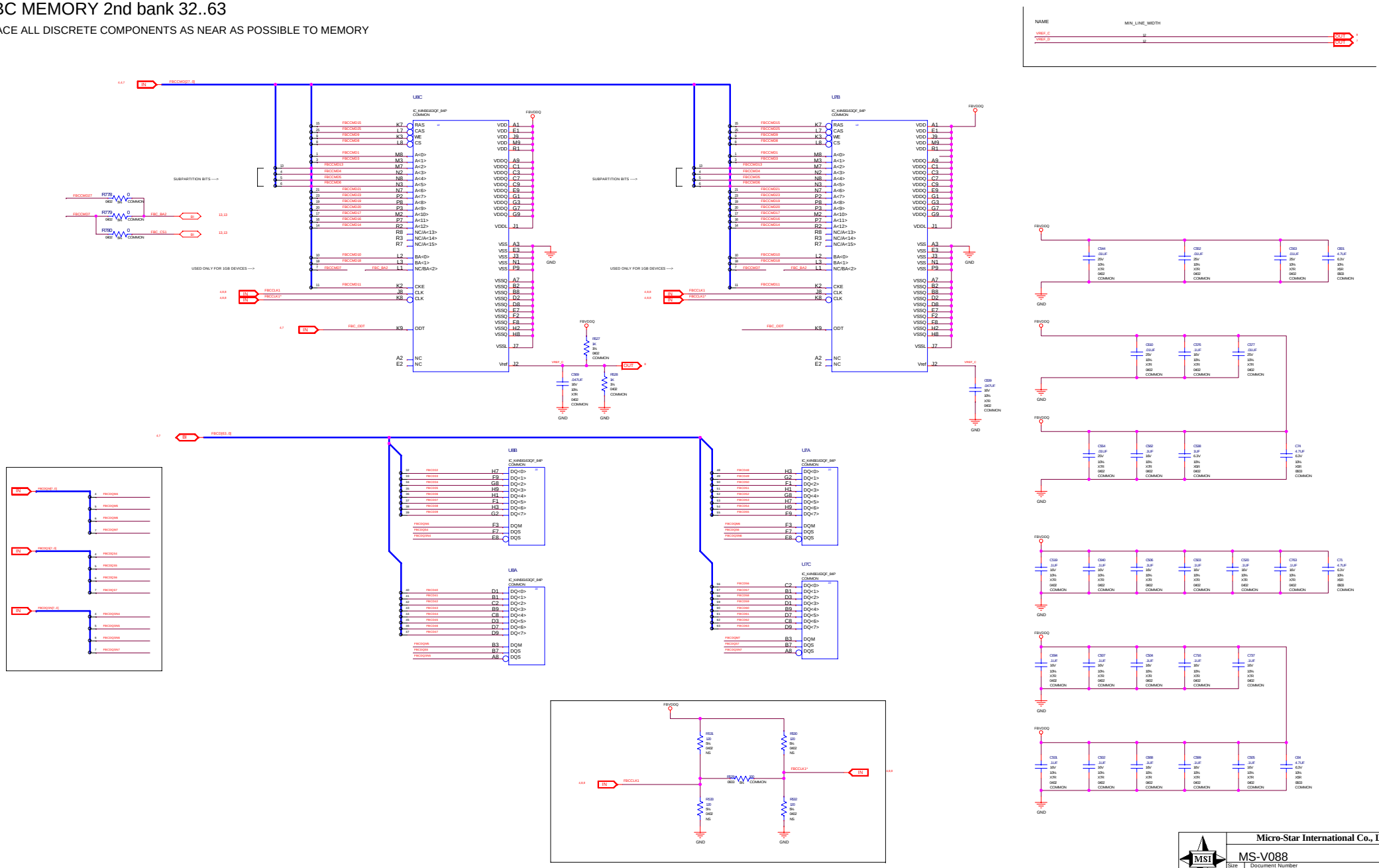
08 MEMORY PARTITION C 32..63

FBC MEMORY 2nd bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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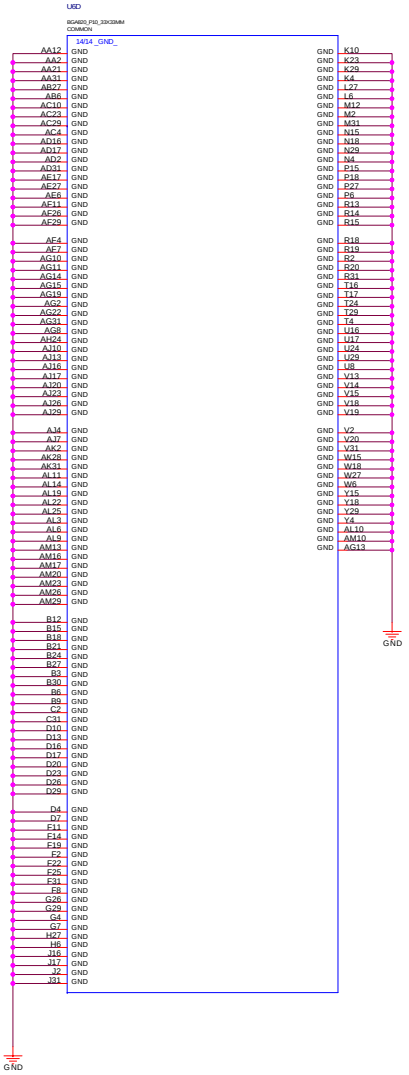
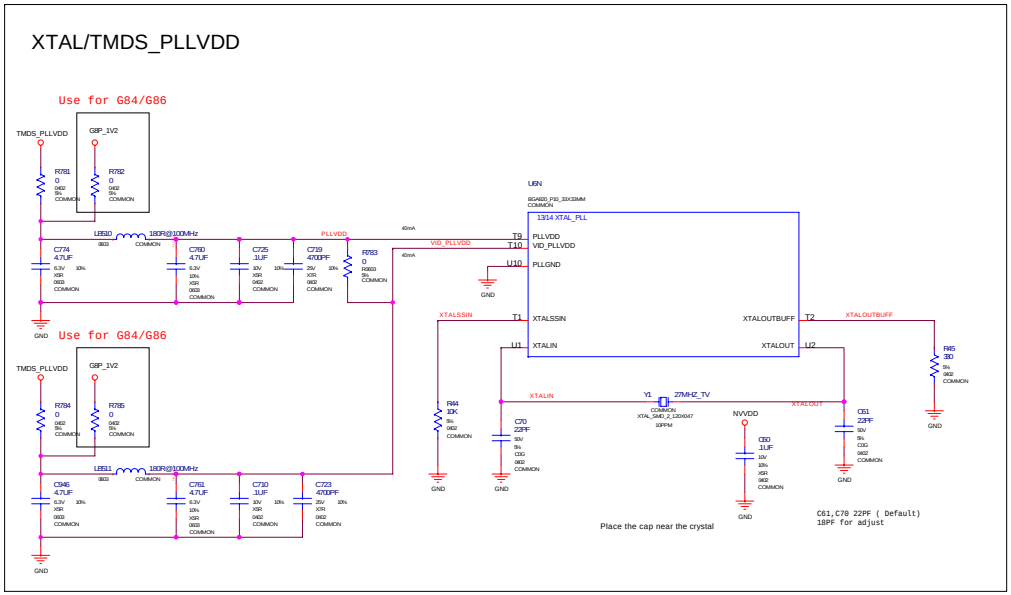
09 GPU GND / TMDS_PLLVDD





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10 DACA - VGA

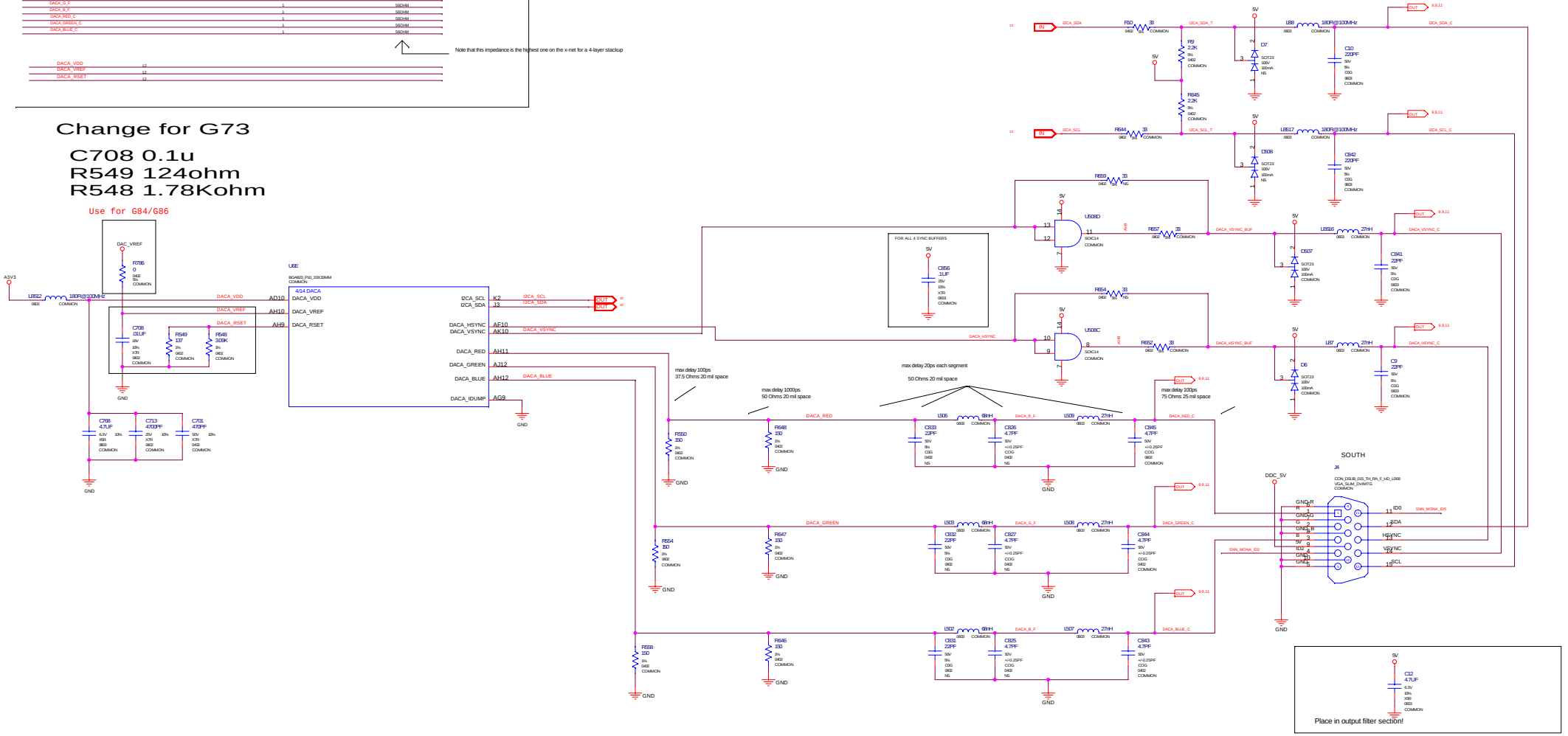
NET_NAME	MIN_LINE_WIDTH	NV_CRITICAL_NET	NV_IMPEDANCE
I2CA_SCL			
I2CA_SDA			
DACA_HSYNC	2		50OHM
DACA_VSYNC	2		50OHM
DACA_HSYNC_BUF	2		50OHM
DACA_VSYNC_BUF	2		50OHM
DACA_VSYNC_C	2		50OHM
DACA_HSYNC_C	2		50OHM
AVIB	2		50OHM
A VIB	2		50OHM
DACA_RED	1		50OHM
DACA_GREEN	1		50OHM
DACA_BLUE	1		50OHM
DACA_G_F	1		50OHM
DACA_R_F	1		50OHM
DACA_RED_C	1		50OHM
DACA_GREEN_C	1		50OHM
DACA_BLUE_C	1		50OHM
DACA_VDD	12		
DACA_VREF	12		
DACA_RSET	12		

Note that this impedance is the highest one on the x-net for a 4-layer stackup

Change for G73

C708 0.1u
R549 124ohm
R548 1.78Kohm

Use for G84/G86



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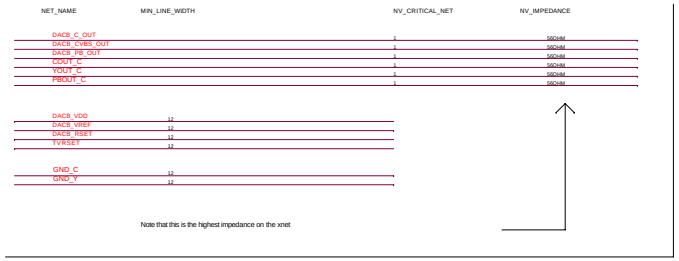
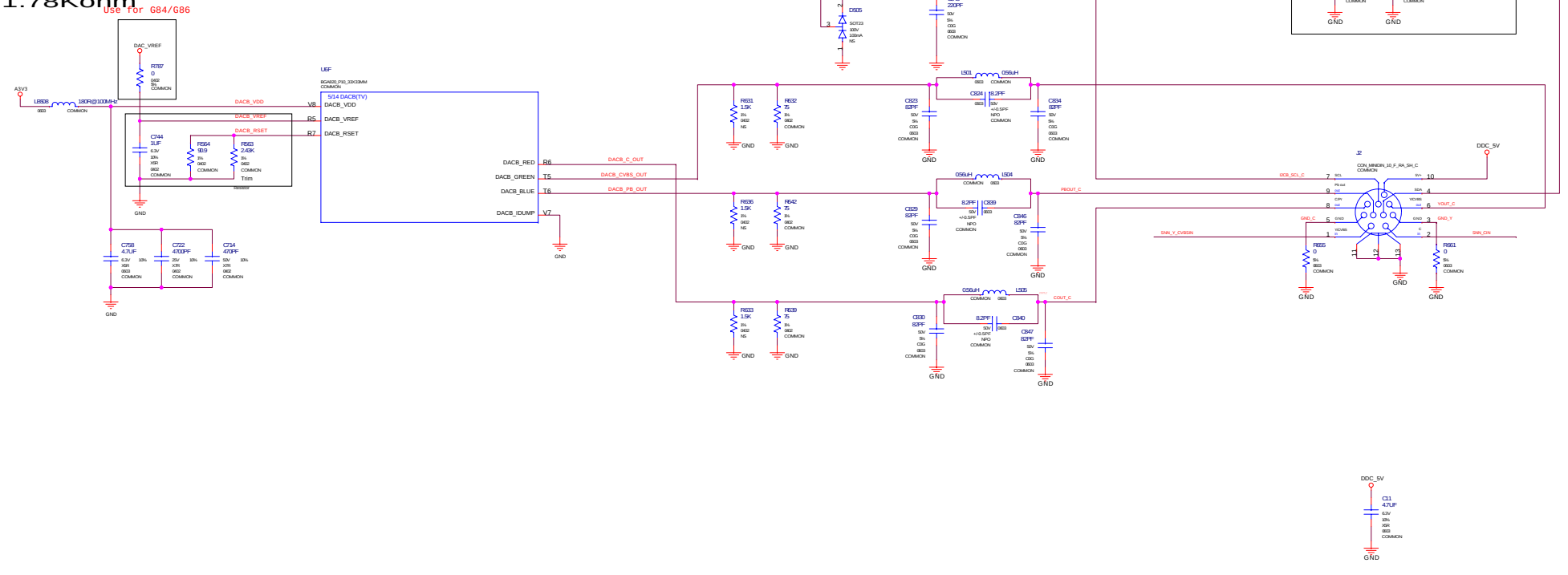
11 DACB - TVOUT, VIDEO IN



Change for G73

C744 0.1u
R564 124ohm
R563 1.78Kohm



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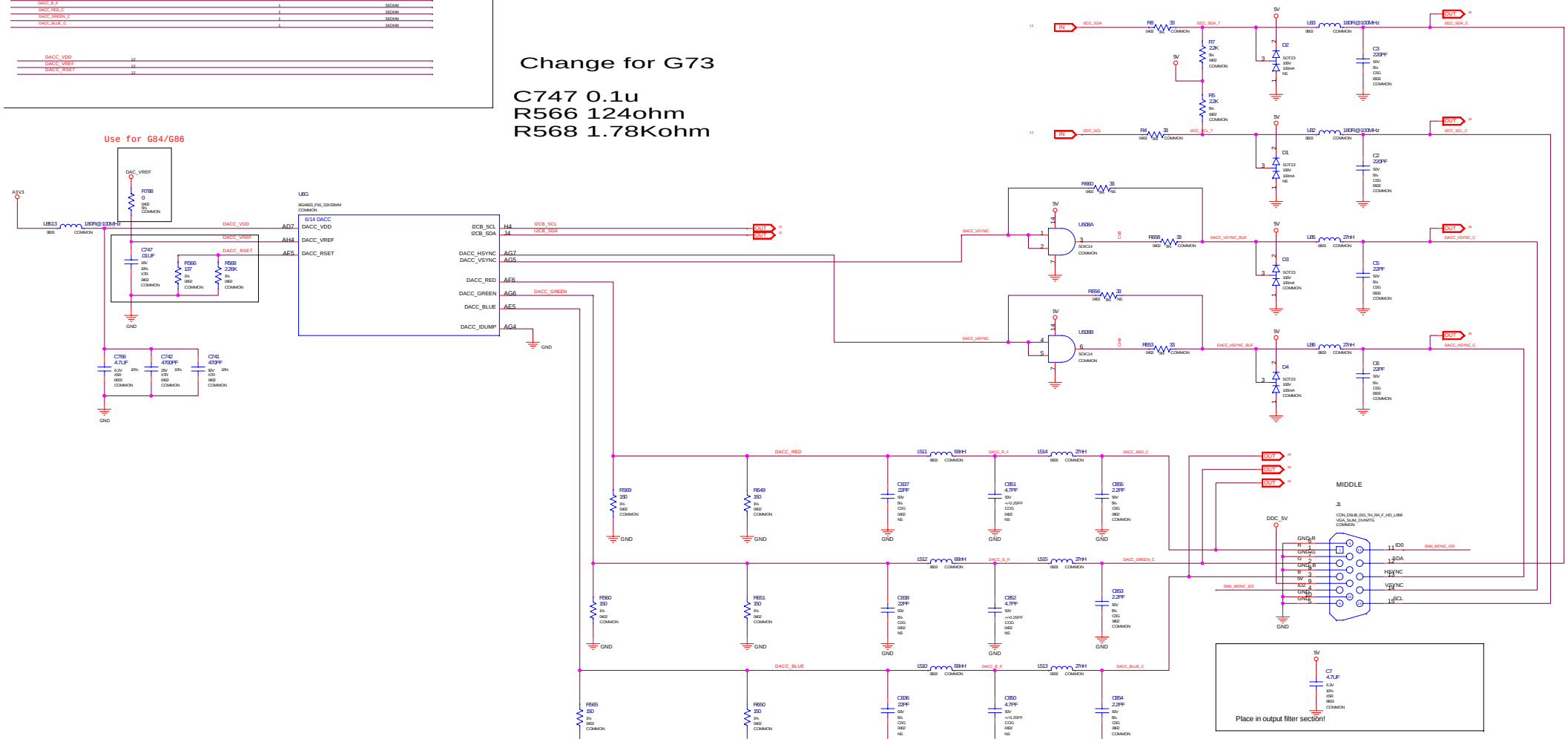
12 DACC - VGA

NET_NAME	MIN_LINE_WIDTH	NET_SPACING_RULE	NV_CRITICAL_NET	NV_IMPEDANCE
I2CB_SCL				
I2CB_SDA				
DACC_HSYNC		2		50OHM
DACC_VSYNC		2		50OHM
DACC_HSYNC_BUF		2		50OHM
DACC_VSYNC_BUF		2		50OHM
DACC_VSYNC_C		2		50OHM
DACC_HSYNC_C		2		50OHM
CHB		2		50OHM
CVB		2		50OHM
DACC_RED		1		50OHM
DACC_GREEN		1		50OHM
DACC_BLUE		1		50OHM
DACC_R_F		1		50OHM
DACC_G_F		1		50OHM
DACC_B_F		1		50OHM
DACC_RED_C		1		50OHM
DACC_GREEN_C		1		50OHM
DACC_BLUE_C		1		50OHM
DACC_VDD	12			
DACC_VREF	12			
DACC_RSET	12			

Change for G73

C747 0.1u
R566 124ohm
R568 1.78Kohm

Use for G84/G86



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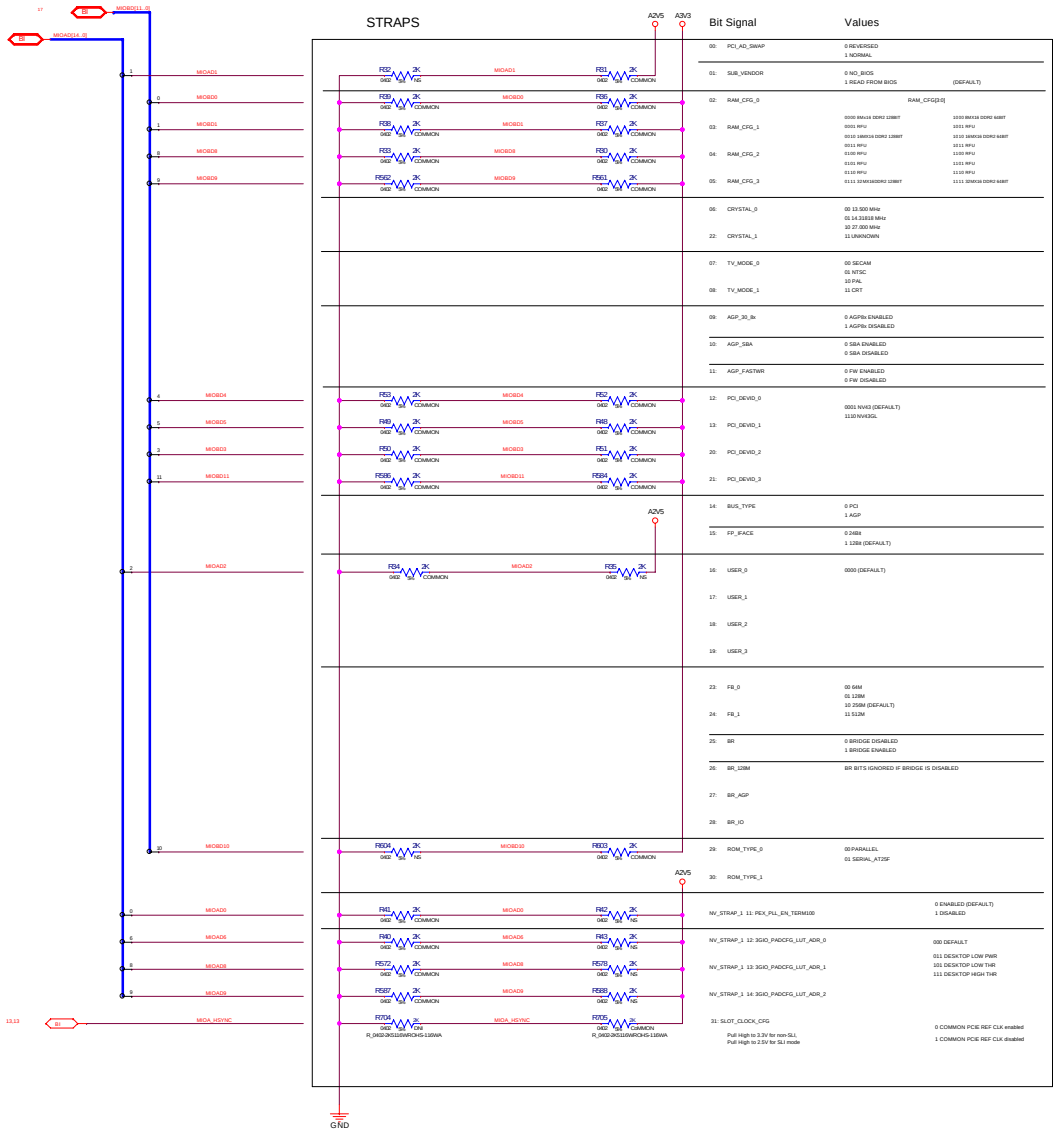
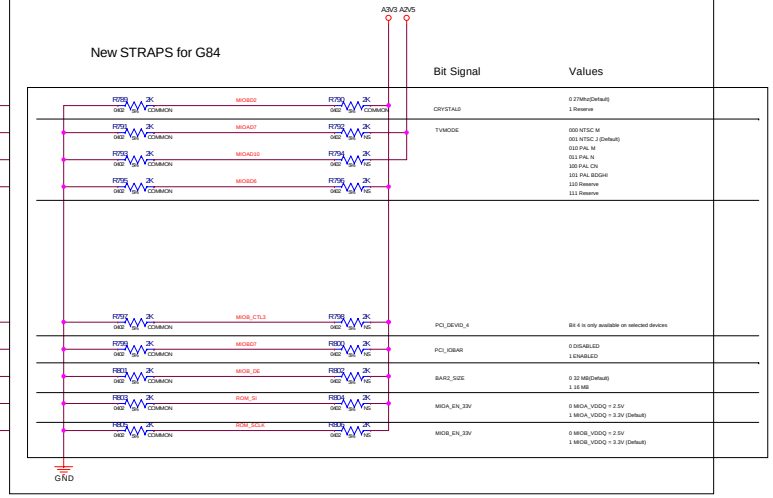
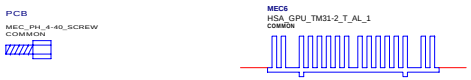
13 STRAPS, FANSINK, MECHANICALS (Strap R using 2K if no specail requred)

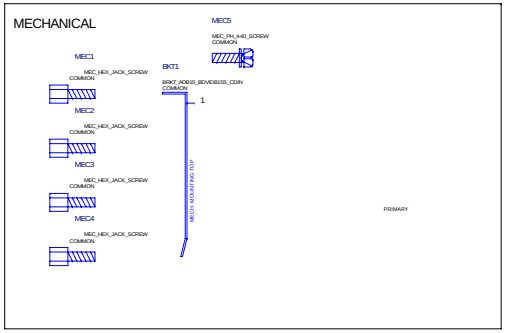


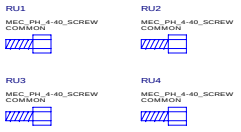
Use for G84/G86



Reserve by PCB placement only







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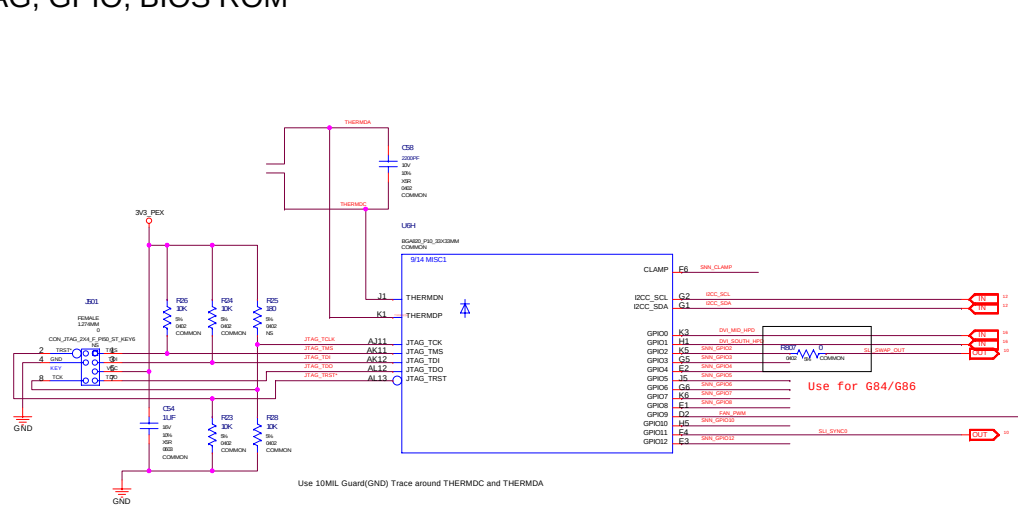
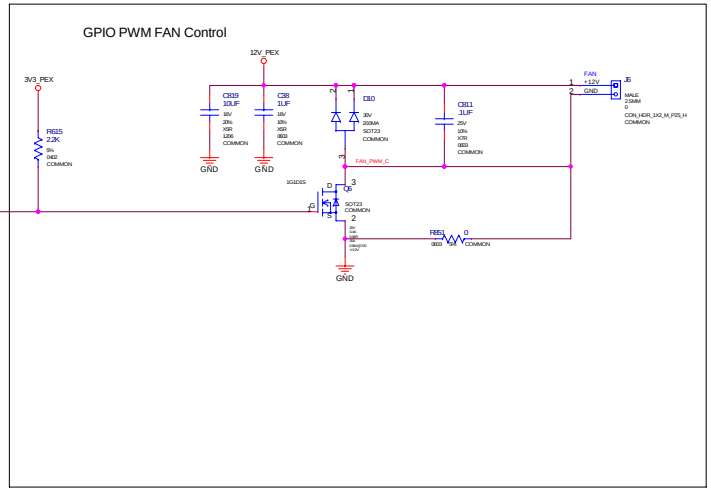
14 GPIO, HDCP, VBIOS, FAN CON

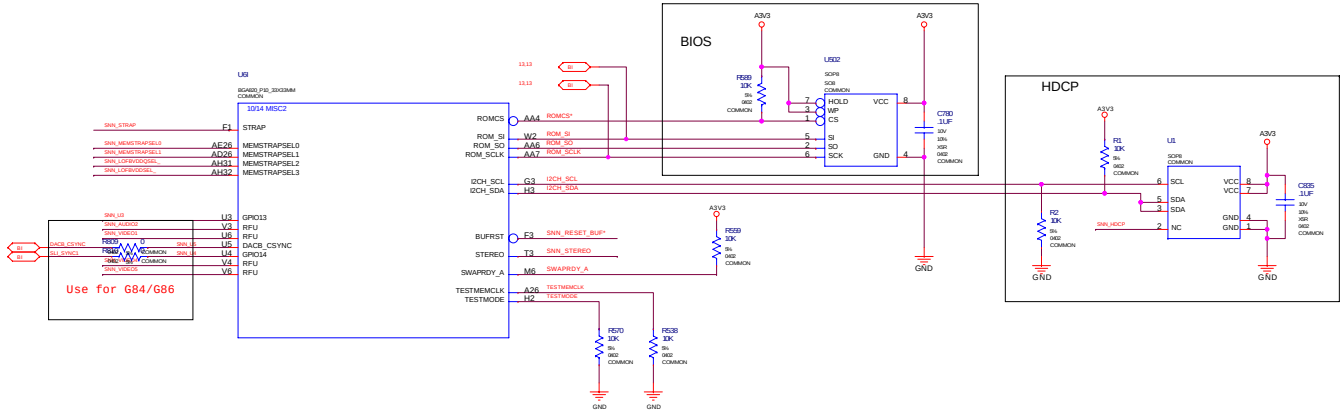
JTAG, GPIO, BIOS ROM



GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	RESERVED
2	IN	RESERVED
3	IN	RESERVED
4	IN	RESERVED
5	IN	RESERVED
6	IN	RESERVED
7	IN	RESERVED
8	IN	THERM ALERT/SLOW
9	OUT	FAN CONTROL
10	IN	RESERVED
11	OUT	HDTV/SDTV SELECT
12	IN	RESERVED



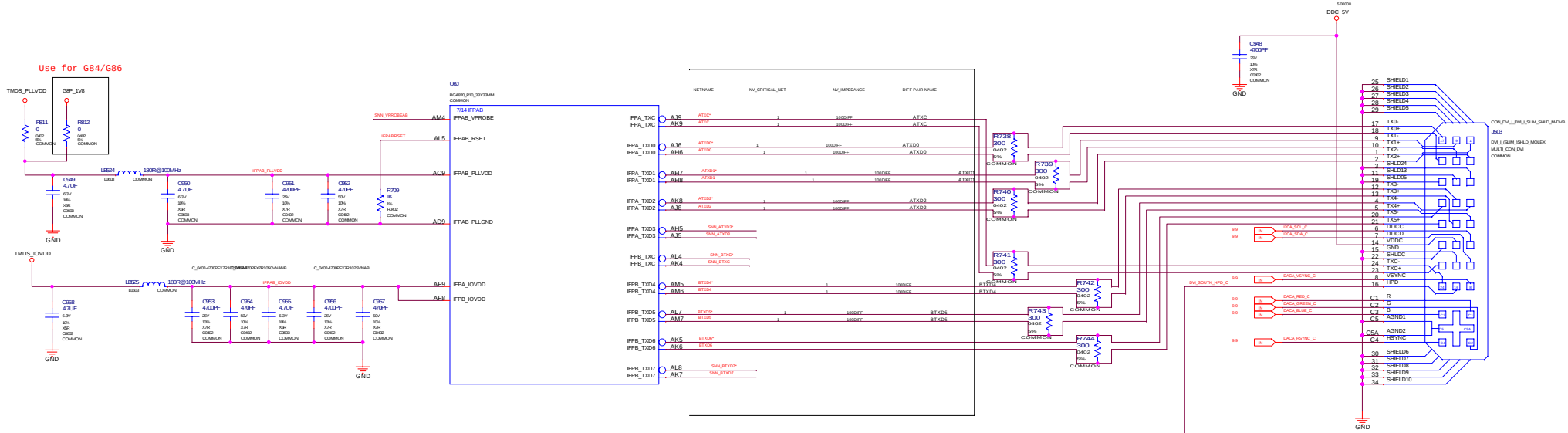


15 INTERNAL TMDS LINK A/B

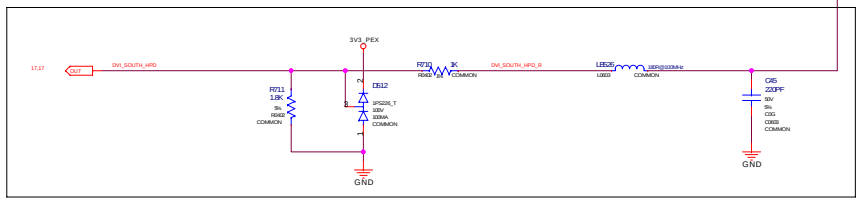
IFPAB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RSET	1	50OHM	
DVI_SOUTH_HPD_C	1	50OHM	
DVI_SOUTH_HPD_R	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLLVDD	3.30000	0.04	16.0
IFPAB_IOVDD	3.30000	0.24	16.0



Hotplug Detection



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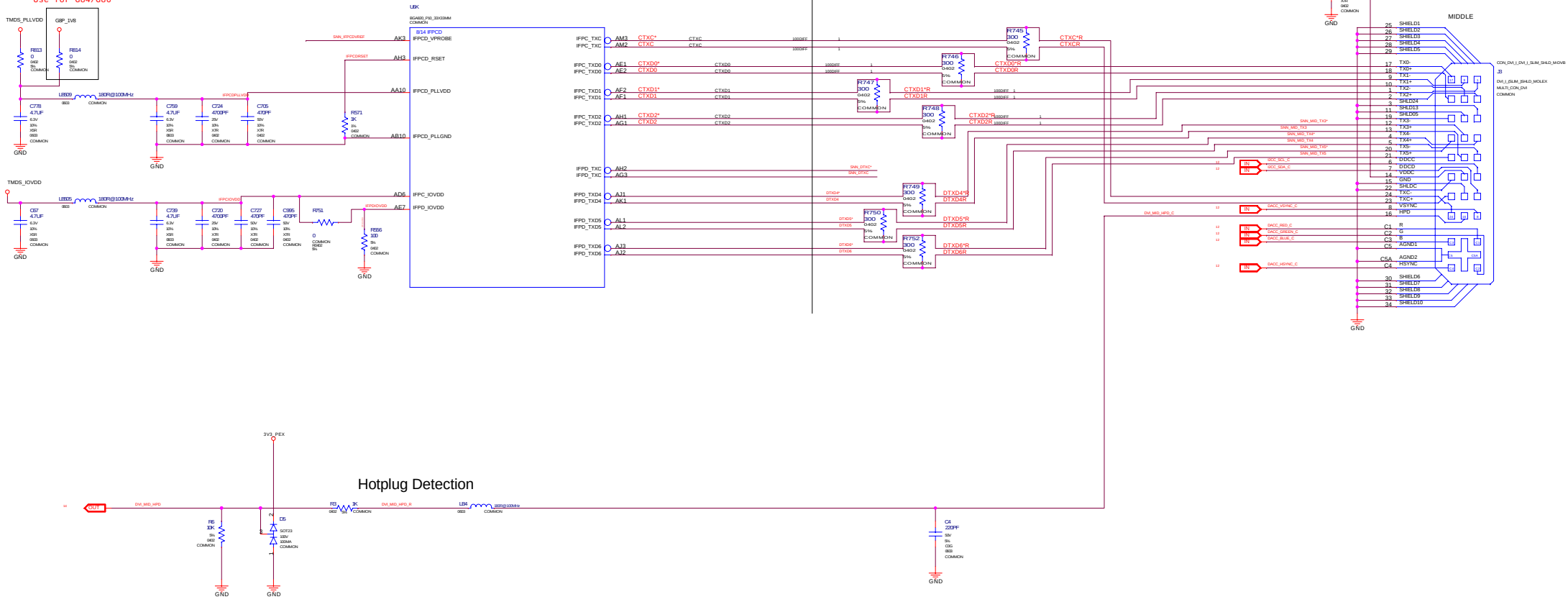
16 INTERNAL TMDS LINK C/D

NET	MIN_LINE_WIDTH	VOLTAGE
IFPCDVREF	12	3.3V
IFPCDPLLVDD	12	3.3V
IFPCIOVDD	12	3.3V
IFPIOVDD	12	3.3V
IFPCDRSET	12	

INTERNAL TMDS ..LINK C

Use for G84/G86

Hotplug Detection



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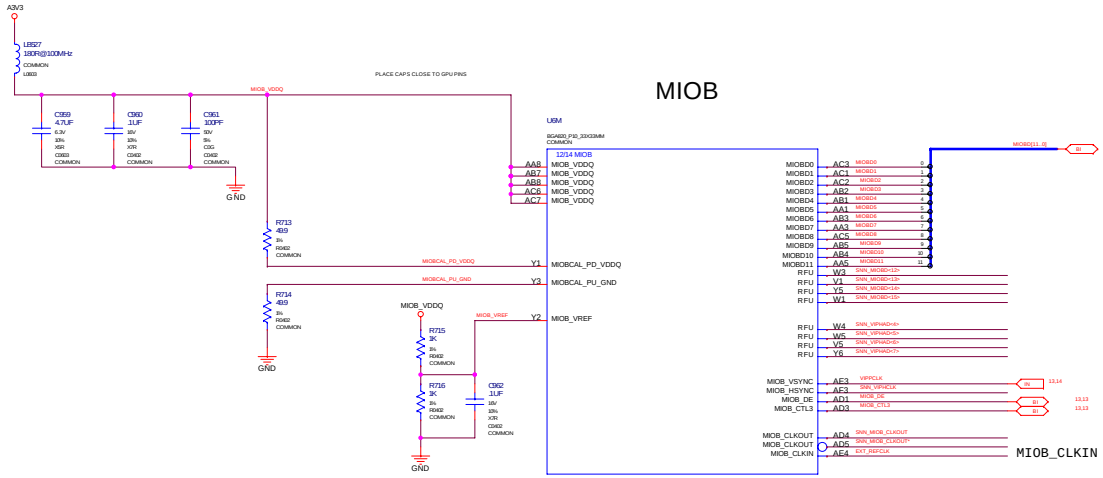
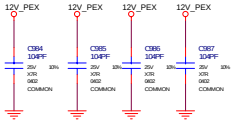
17 MIOA, MIOB, NVPLL

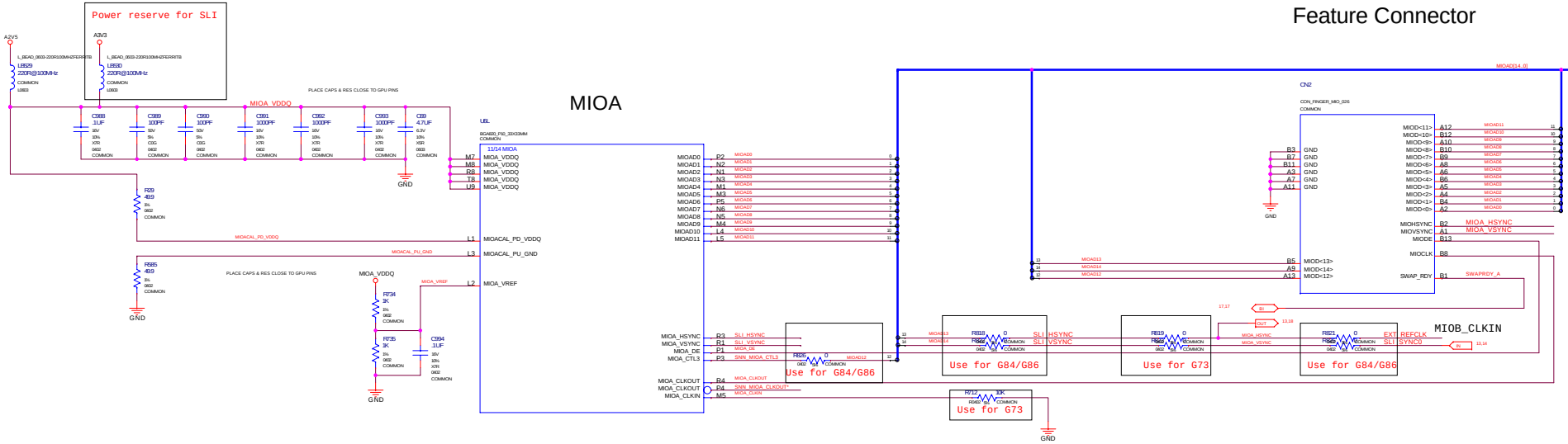
MIO NET RULES

MIOB





MIOA



Feature Connector

Micro-Star International Co., LTD.		
MS-V088		
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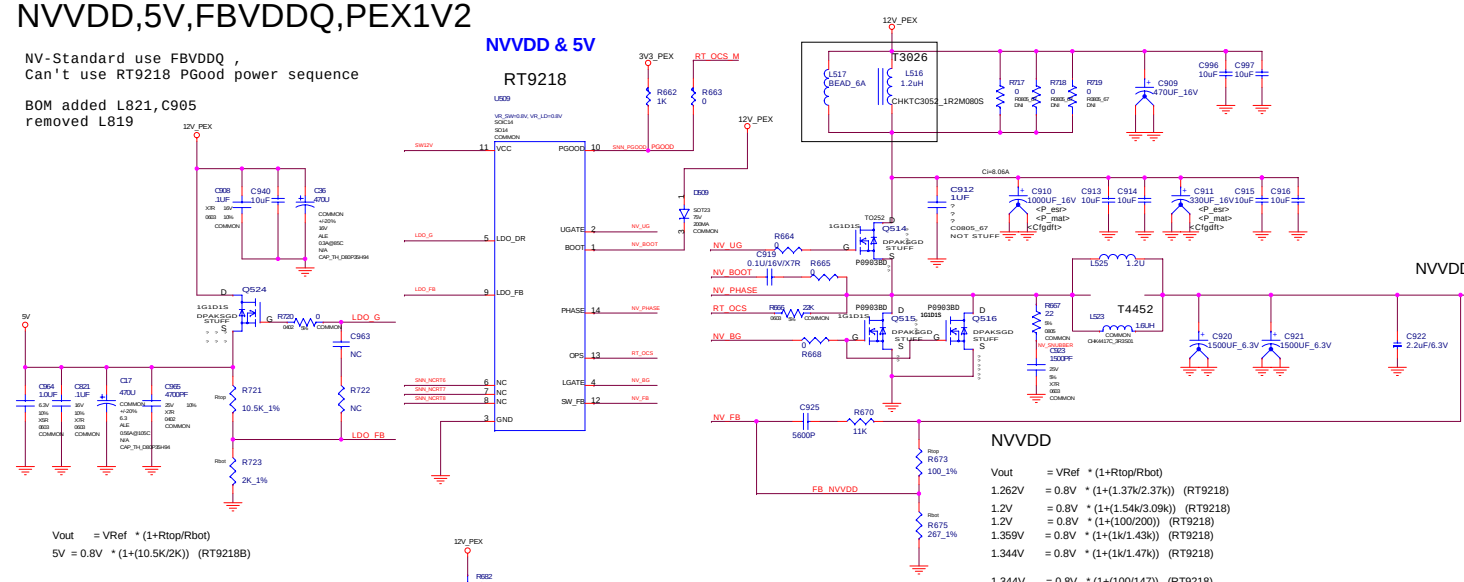
18 Power Supply (RT9218)
NVVDD,5V,FBVDDQ,PEX1V2

NV-Standard use FBVDDQ ,
Can't use RT9218 PGood power sequence

BOM added L821,C905
removed L819

NVVDD & 5V

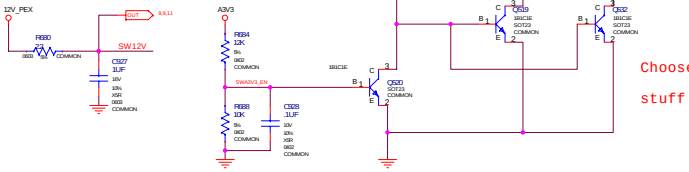
RT9218



NVVDD

Vout	= VRef * (1+Rtop/Rbot)	
1.262V	= 0.8V * (1+(1.37k/2.37k))	(RT9218)
1.2V	= 0.8V * (1+(1.54k/3.09k))	(RT9218)
1.2V	= 0.8V * (1+(100/200))	(RT9218)
1.359V	= 0.8V * (1+(1k/1.43k))	(RT9218)
1.344V	= 0.8V * (1+(1k/1.47k))	(RT9218)
1.344V	= 0.8V * (1+(100/147))	(RT9218)
1.3V	= 0.8V * (1+(100/160))	(RT9218) default
1.099V	= 0.8V * (1+(100/267))	(RT9218) default

Vout = VRef * (1+Rtop/Rbot)
5V = 0.8V * (1+(10.5K/2K)) (RT9218B)

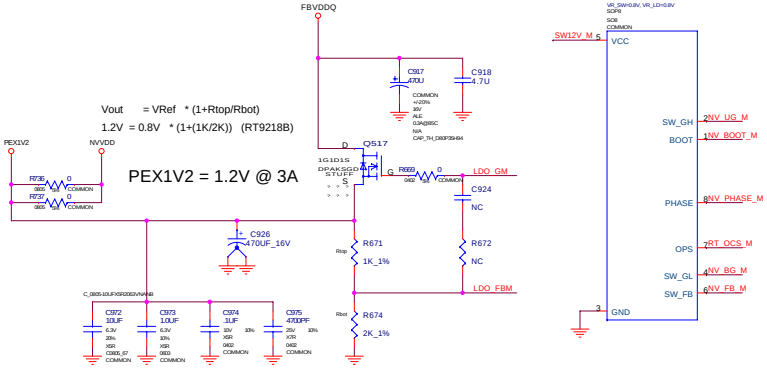


Choose RT9218 PGood power sequence

stuff R663,R690,D510

Use for G84/G86

APW7120 / RT9214

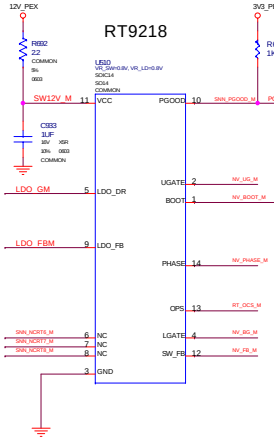


Vout = VRef * (1+Rtop/Rbot)
1.2V = 0.8V * (1+(1K/2K)) (RT9218B)

PEX1V2 = 1.2V @ 3A

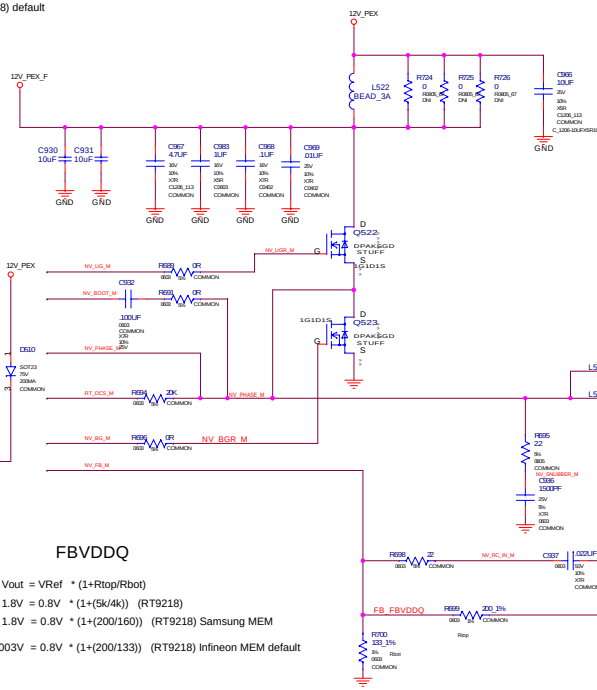
FBVDDQ & PEX1V2

RT9218



FBVDDQ

Vout = VRef * (1+Rtop/Rbot)
1.8V = 0.8V * (1+(5k/4k)) (RT9218)
1.8V = 0.8V * (1+(200/160)) (RT9218) Samsung MEM
2.003V = 0.8V * (1+(200/133)) (RT9218) Infineon MEM default



FBVDDQ = 1.8V @ upto 5A

1.8V/5.0A

Net Name / MIN_LINE_WIDTH / VOLTAGE

Net Name	MIN_LINE_WIDTH	VOLTAGE
5V	16	5V
NVVDD	16	1.35V
12V_PEX	20	12V
PEX1V2	20	1.2V
12V_PEX_FLTRD	20	12V
FBVTT	20	1.5

DRIVE3_1V2	20
UGATE_1	20
LGATE_1	20
UGATE_2	20
LGATE_2	20
NODE_1	20
NODE_2	20
12V_RR	10
ISL12V_VCC	20
COMP1_NVVDD	10
FB1_NVVDD	10
COMP2_5V	10
FB2_5V	10
FB1_1V2	10
REFIN_5V	10
ISL_REFOUT	10
VREF_3V3	10
FB3_RC	10
BOOT_1	20
BOOT_2	20
FREQ_SET	10
SS_NVVDD	10
SS_5V	10
SS_1V2	10
UGATE_1_RG	20
UGATE_2_RG	20
COMP1_RC	10
COMP2_RC	10
NVVDD_RC	10
5V_RC	10
NODE_1_SNUB	20
NODE_2_SNUB	20
CLGATE_1	20
BOOST	20
5VBOOST	20

FM2 FM1 FM4 FM3 FM6 FM5

DC/DC calculator Rev 1.1

Output current Iout 8.00 A
Output voltage Vout 2.10 V
Input voltage Vin 12.00 V
Loss less duty cycle DC 0.18

Switching frequency f 600 kHz

Inductance L 2.200 uH

Ripple current through the inductor Iripple 1.313 A
Maximum inductor current ILMax 8.656 A

Input
Input capacitor ripple current IRMS 3.289 A

Output
Output capacitor total ESR ESR 2.50 mOhm
Output capacitor total capacitance Cout 470.0 uF
Output ripple voltage delta-Vout 3.688 mV

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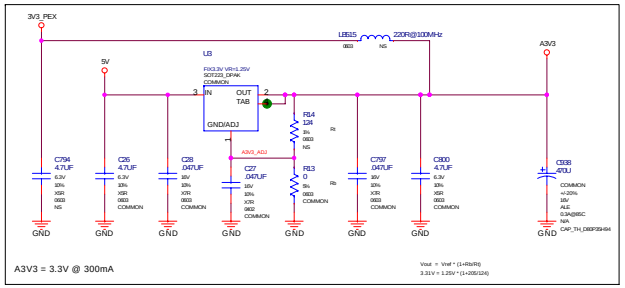
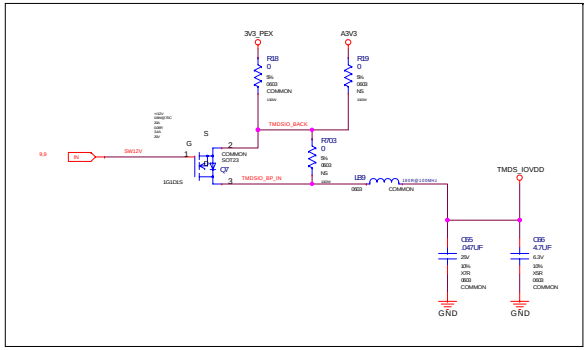
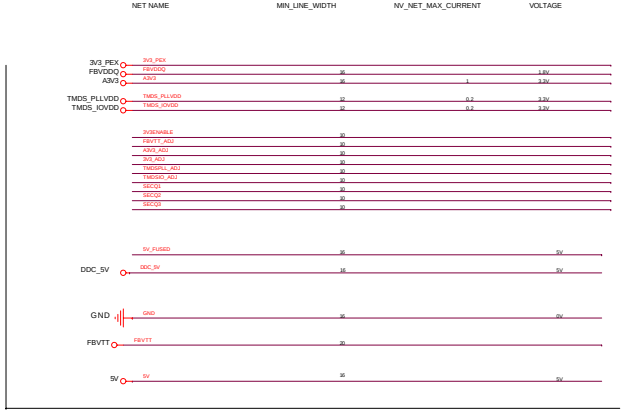
19 Others Power Supply (Linears)
A3V3,A2V5,TMDS_PLLVDD,TMDS_IOVDD

A3V3

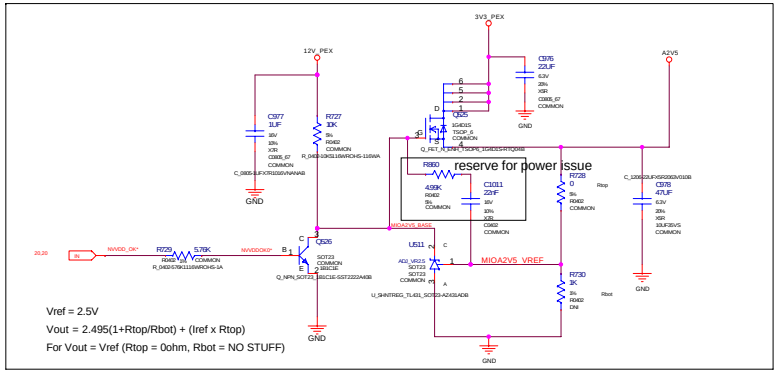


TMDS IO SUPPLY WITH BACKDRIVE PROTECTION

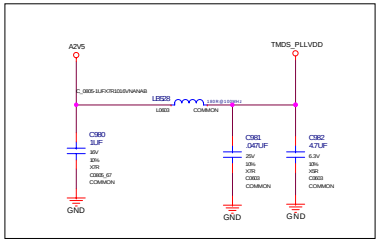




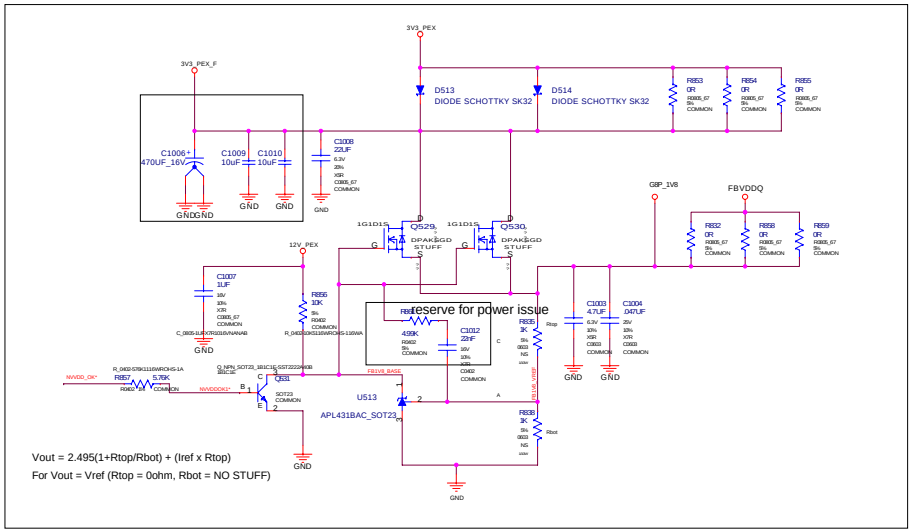
A2V5



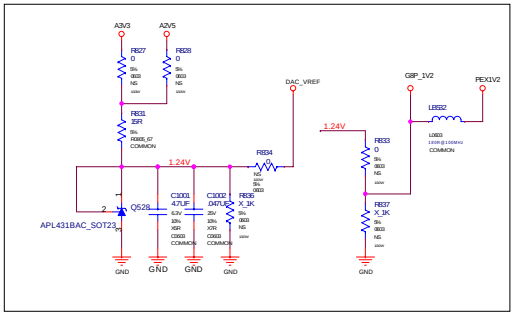
TMDS PLL Supply



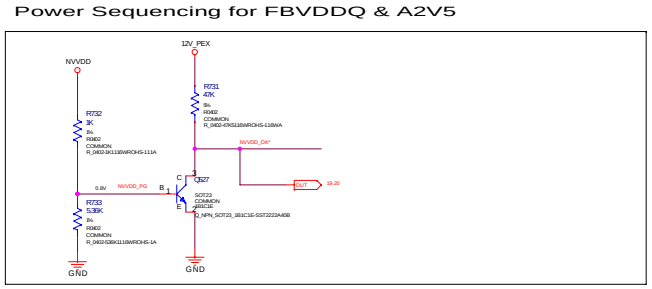
FBVDDQ & 1V8 Use for G84/G86



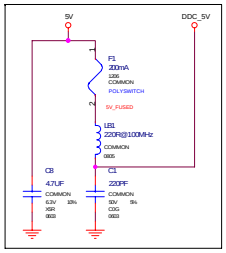
DAC_VREF & 1V2 Use for G84/G86



Power Sequencing for FBVDDQ & A2V5



DDC 5V



MSI	Micro-Star International Co., LTD.		
	MS-V088		
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