

PG142-B00
DP + DP + DP + HDMI/DP

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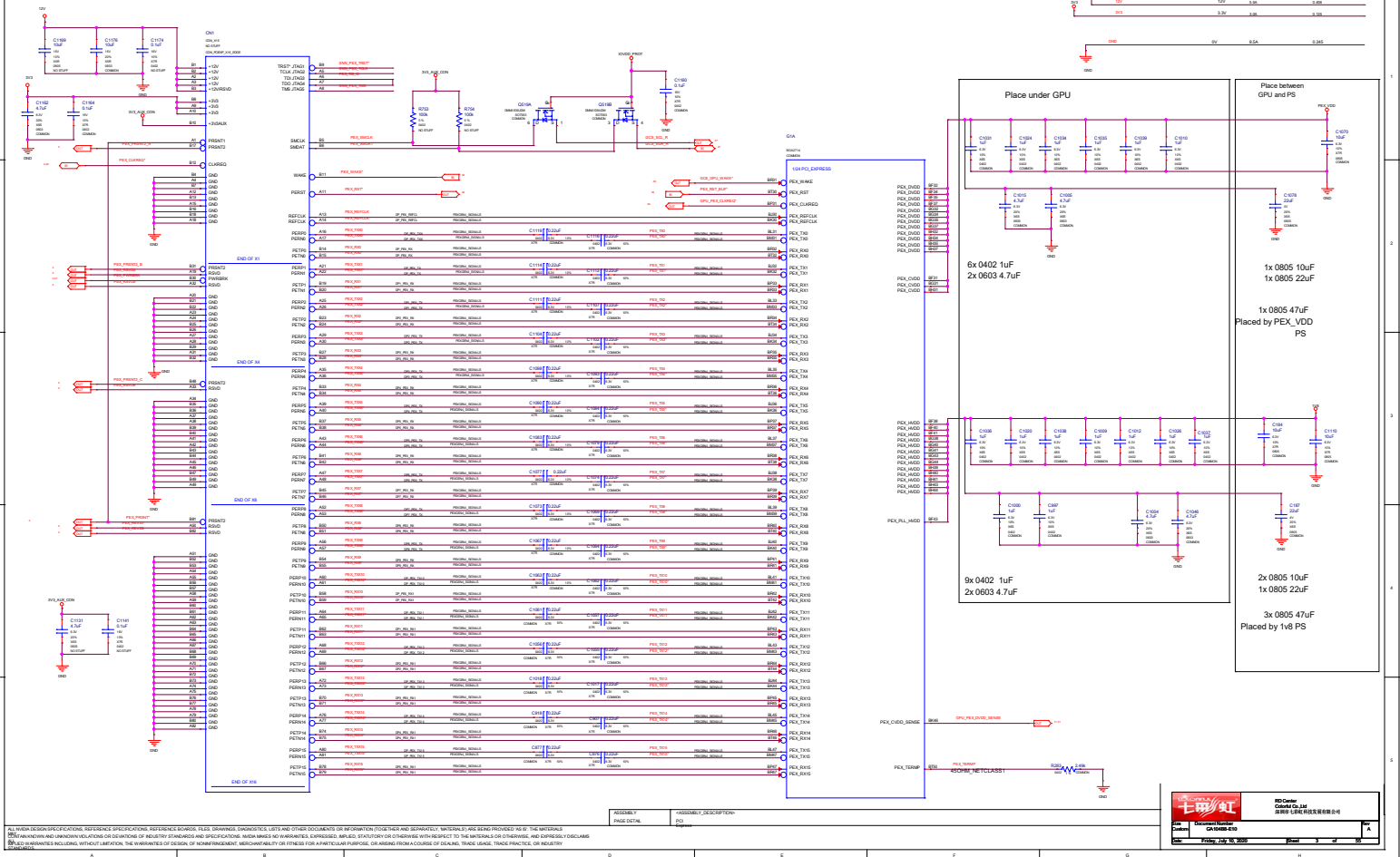
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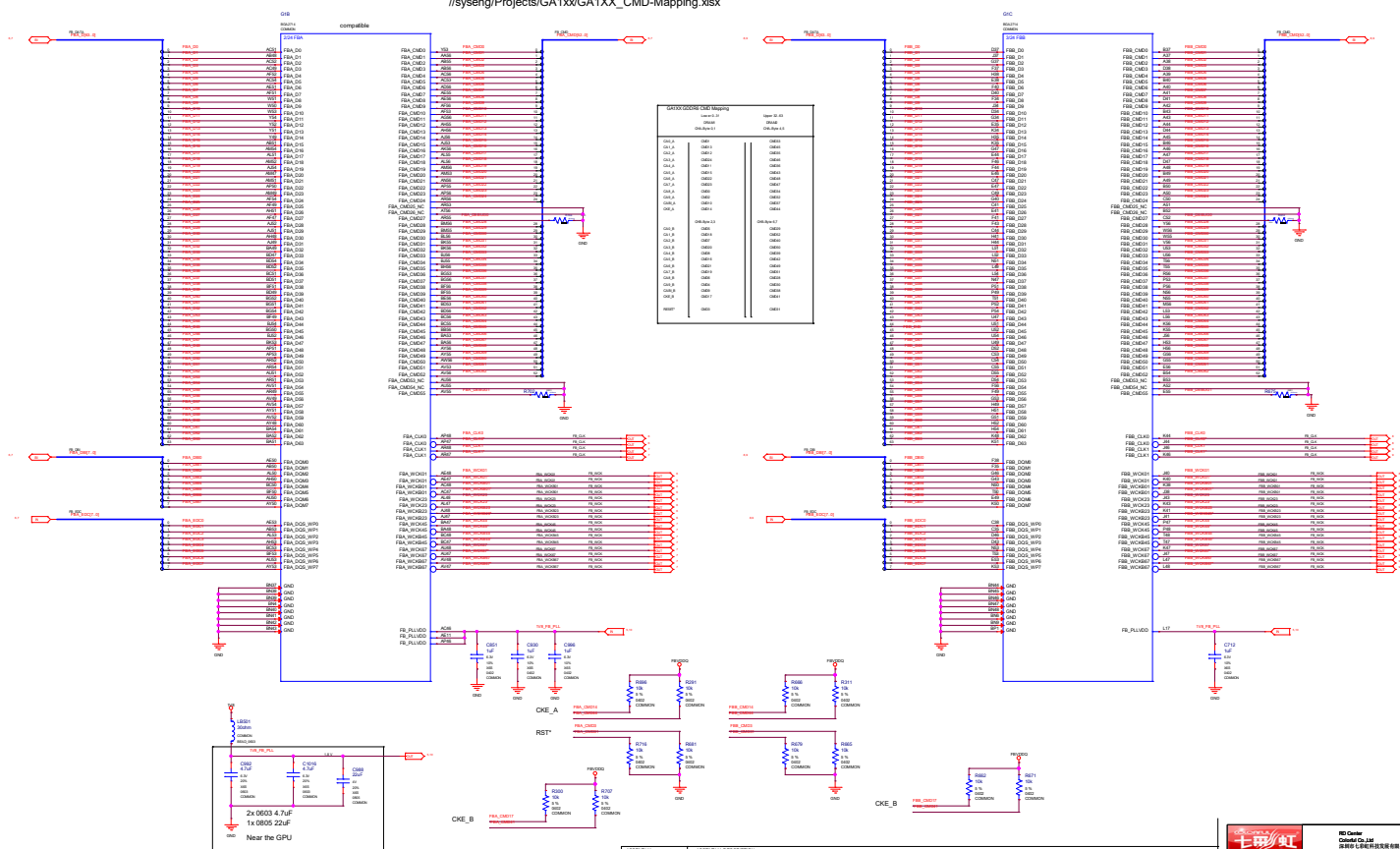




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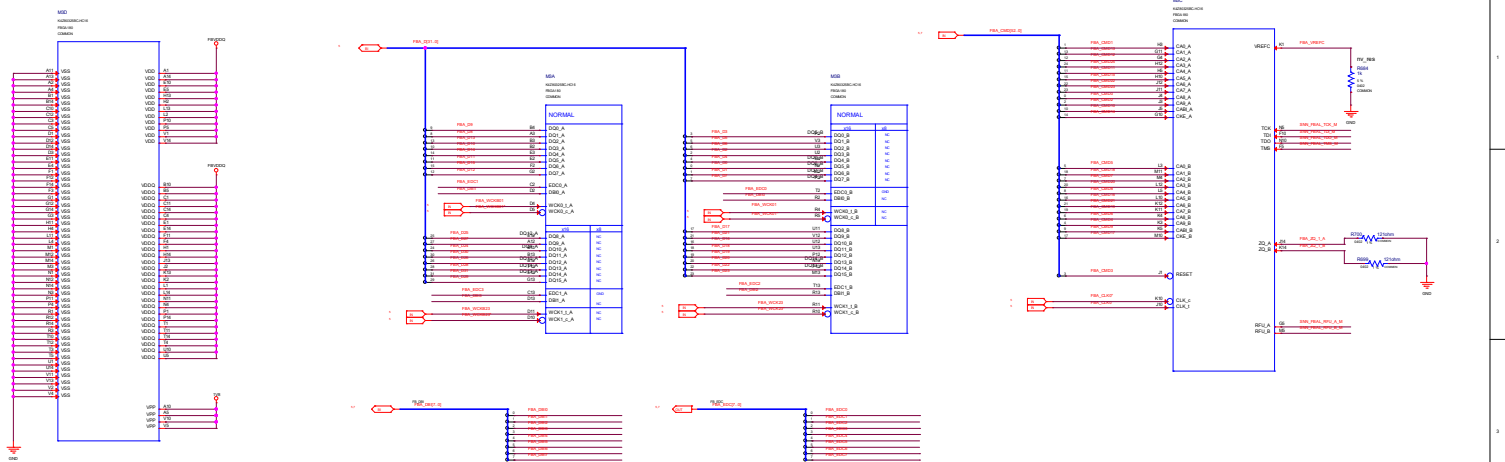

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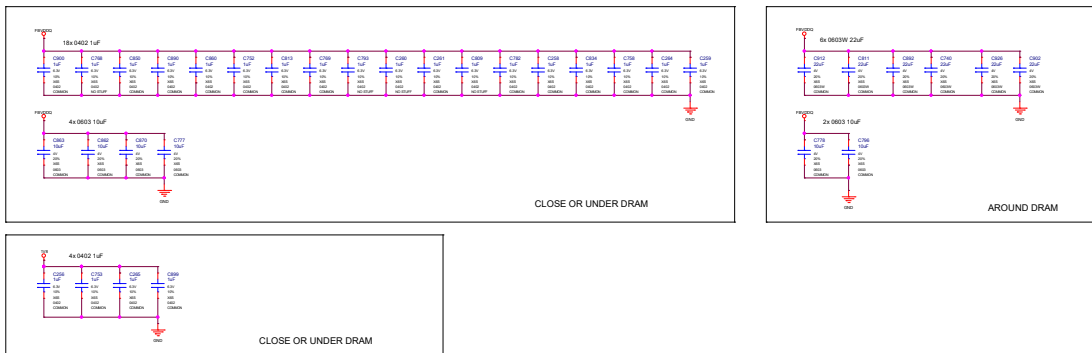
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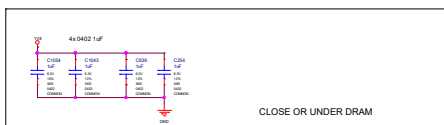
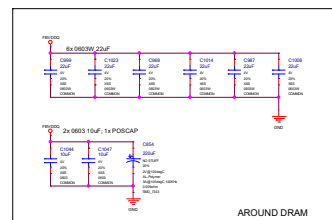
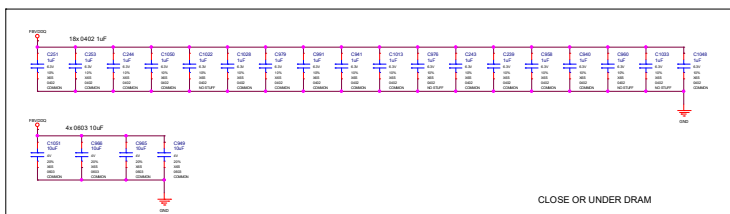
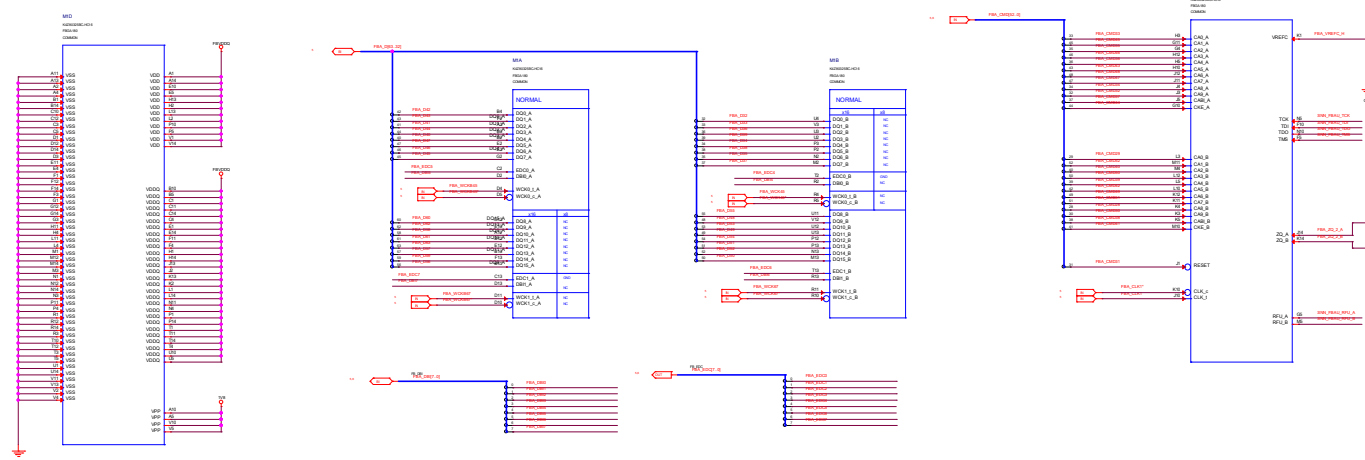
decap via : at least 2 grd via and 2 power via for each cap



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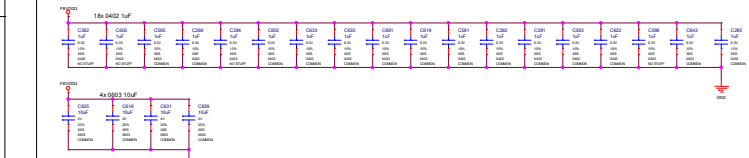
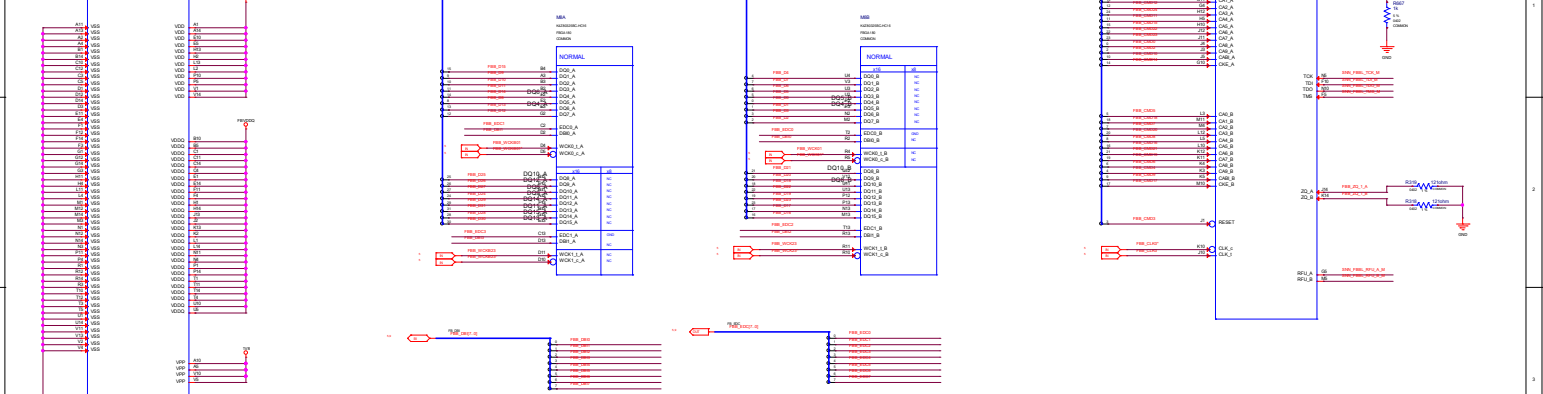
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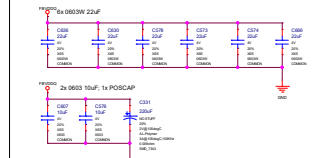


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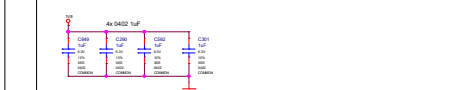
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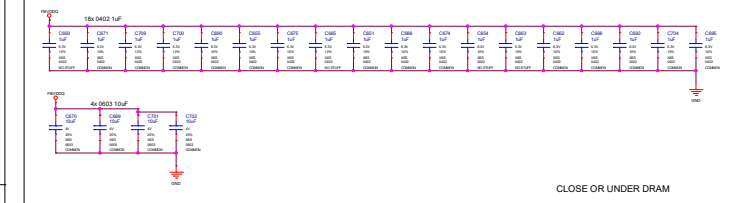
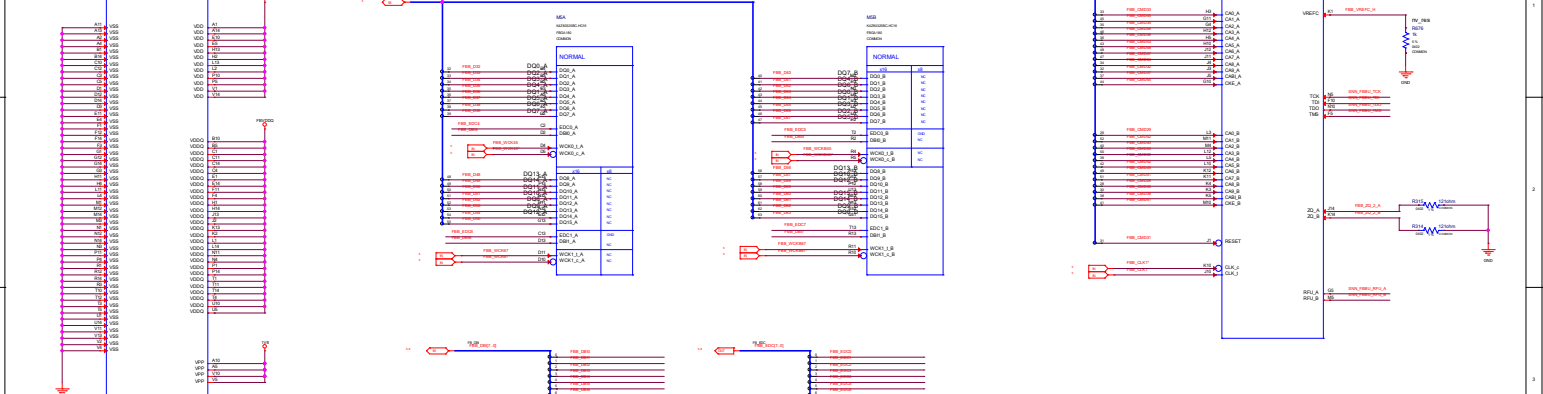
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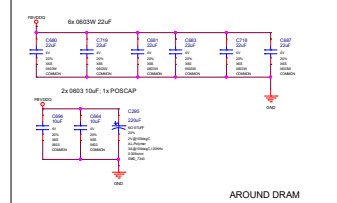
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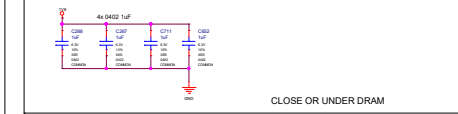
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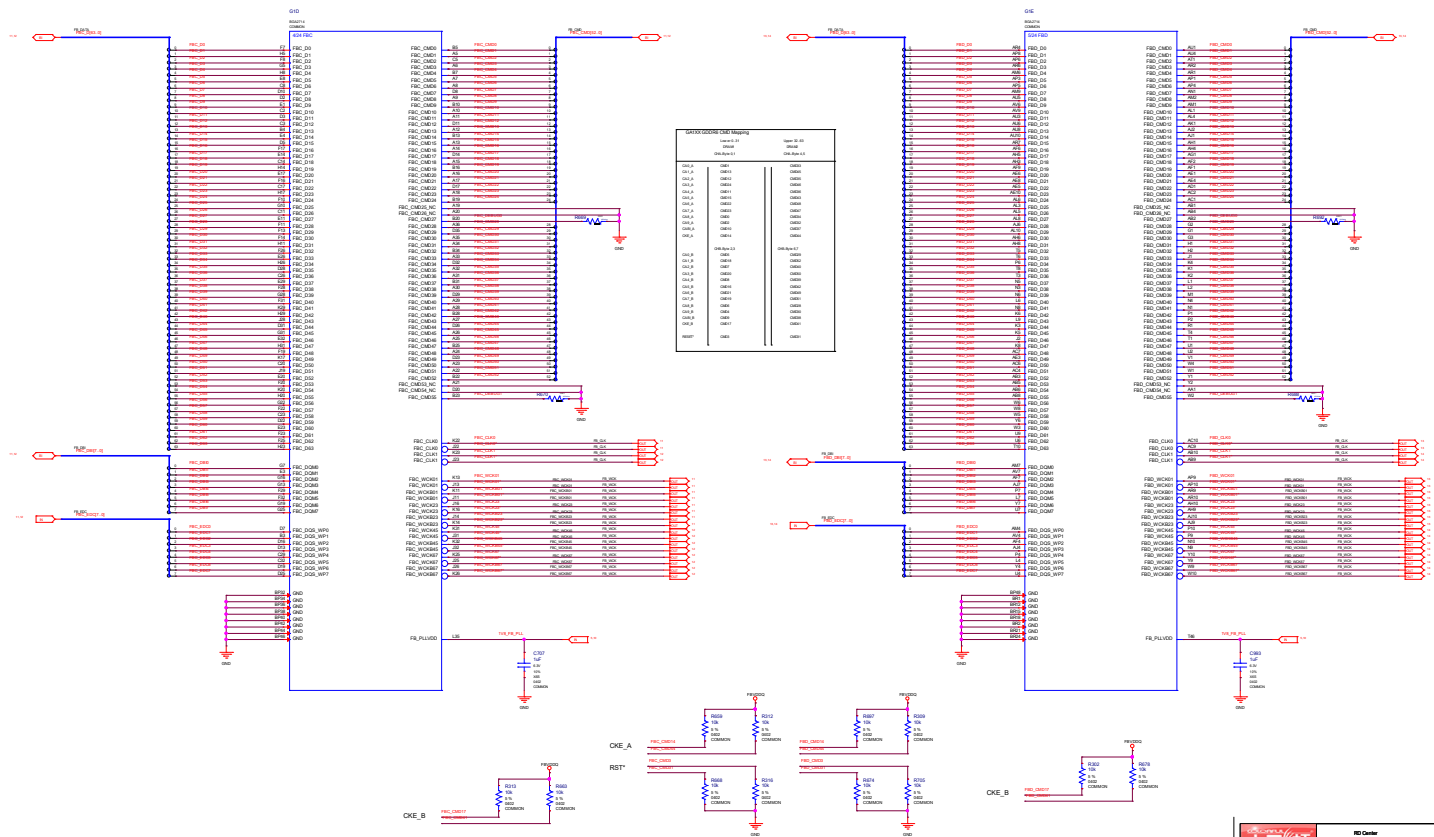
AROUND DRAM



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Date Friday, July 15, 2000	Print 5 of 50		

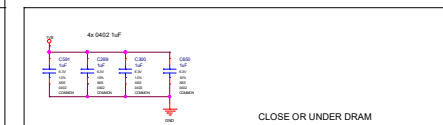
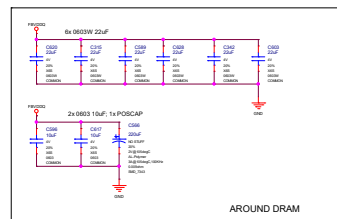
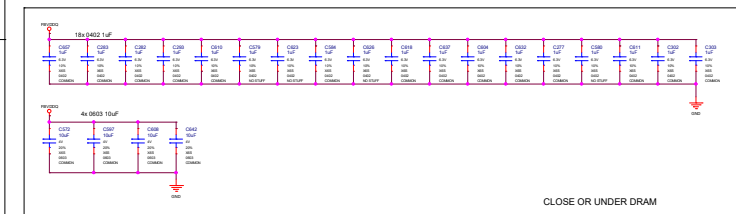
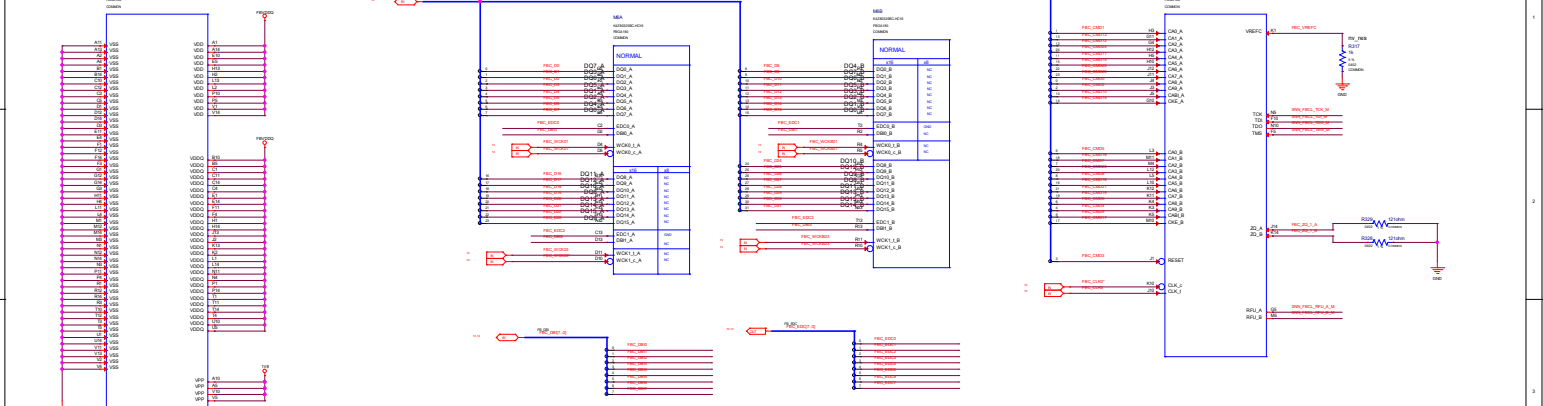


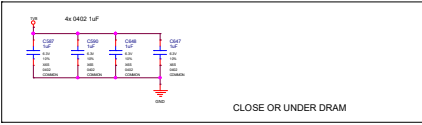
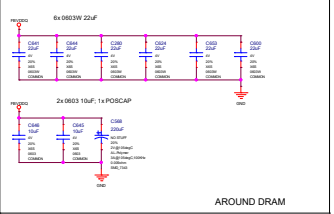
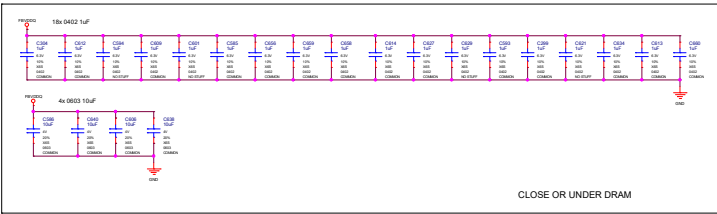
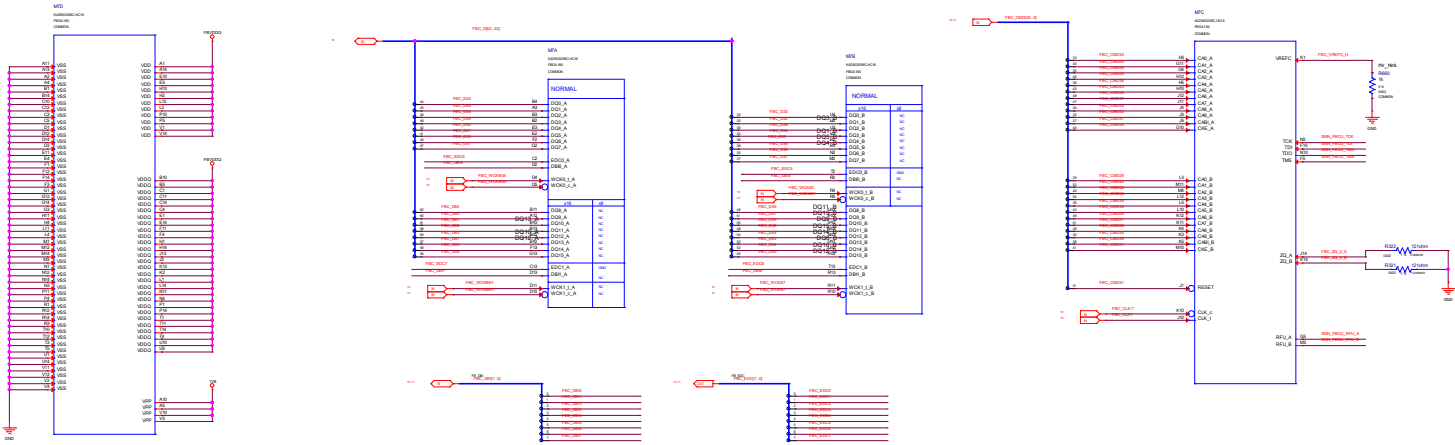
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ASSEMBLY
HARDWARE

PROBABILITY DESCRIPTION
MEMORY (GPU) C/D



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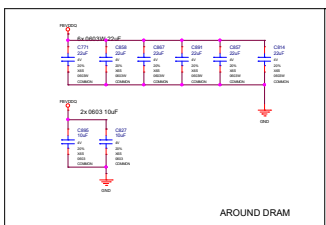
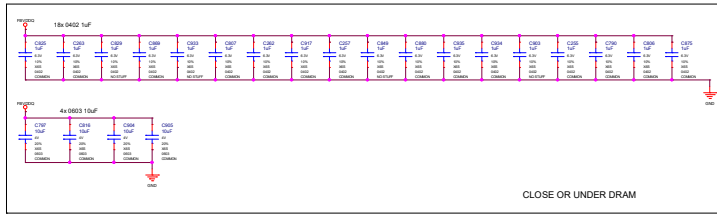
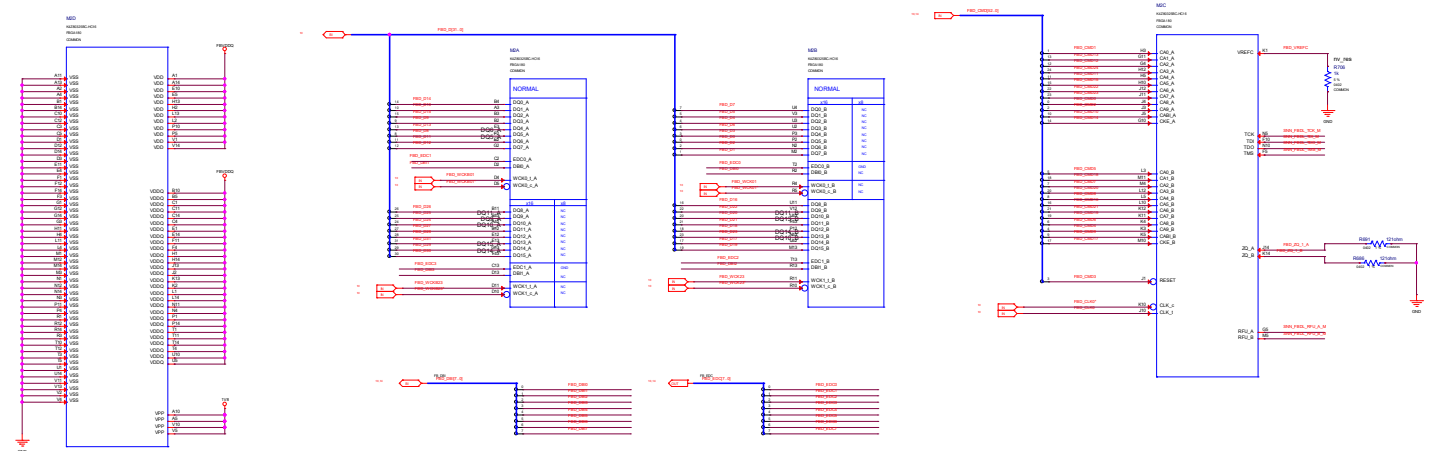
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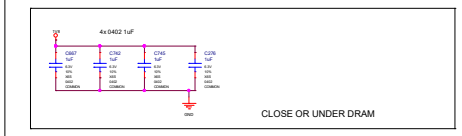
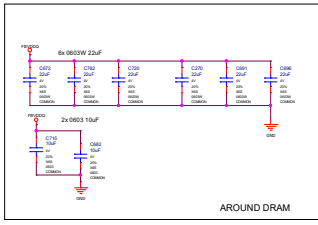
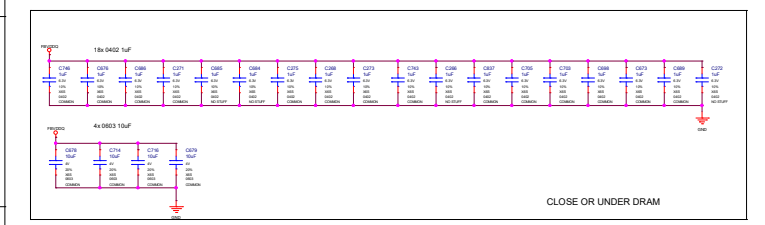
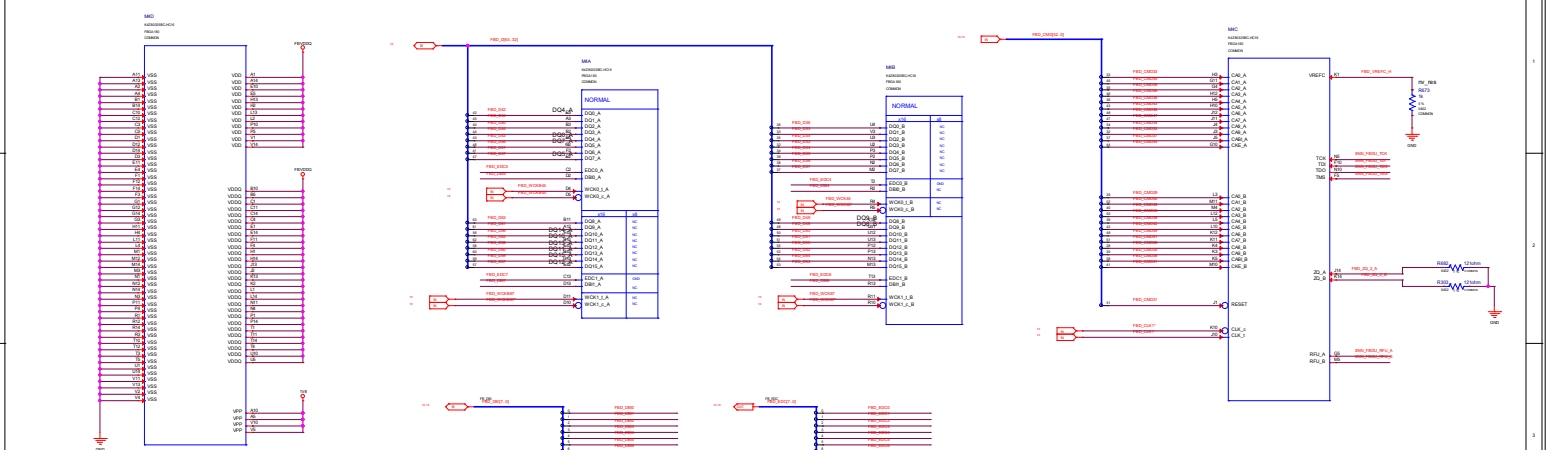
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GA-00000-010

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ASSEMBLY PAGE DETAIL	ASSEMBLY DESCRIPTION MEMORY FB00332	PCI Center Global Co., Ltd. 深圳市七彩虹科技发展有限公司	File Customer Document Number GR1008B-E10 Rev A
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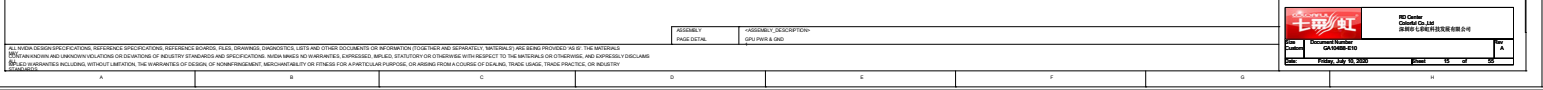
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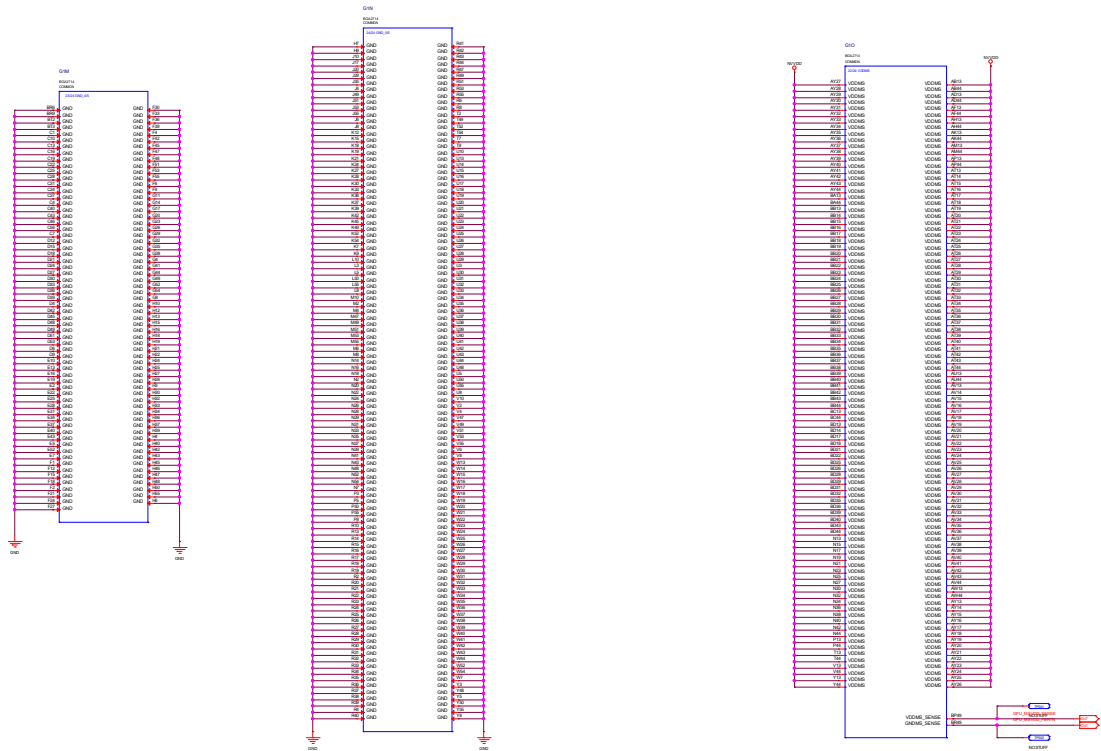
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND

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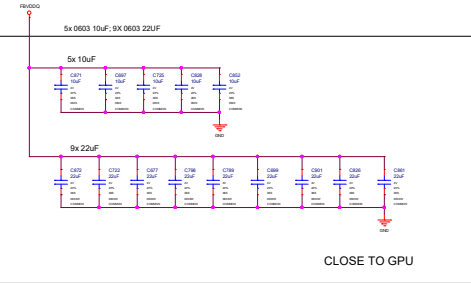
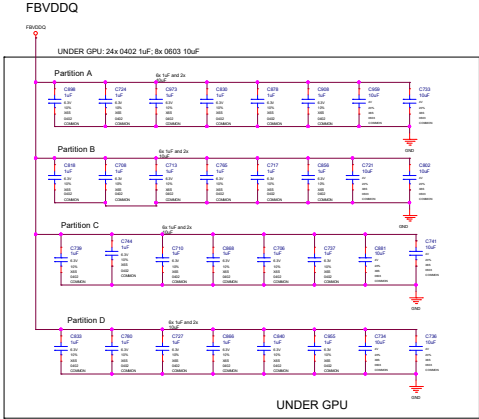
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Date Friday, July 15, 2020		Sheet 15	of 35

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Page18: GPU DECOUPLING FBVDDQ

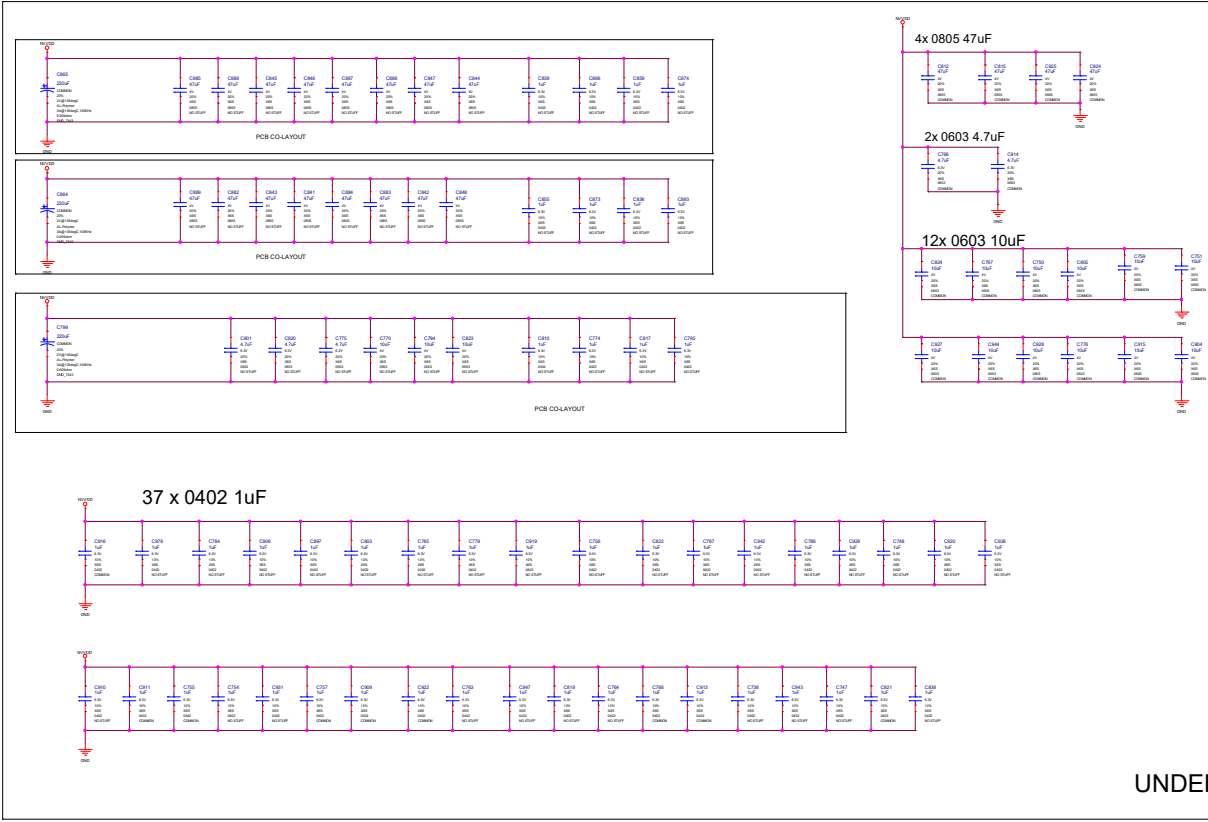


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ASSEMBLY
DESCRIPTION

ASSEMBLY DESCRIPTION
GPU DECOUPLING FBVDDQ

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Document Number CA 00000000		Date Friday, July 11, 2020		



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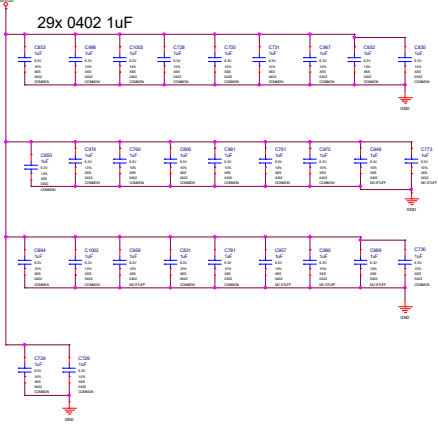
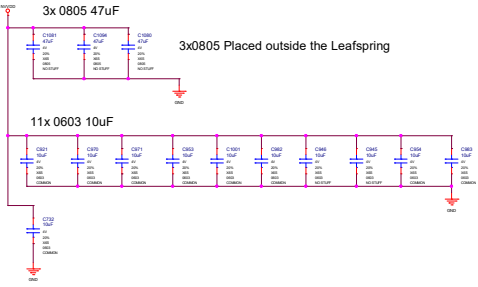
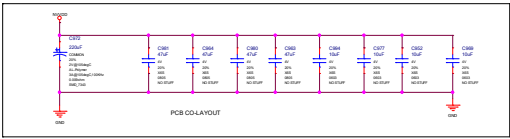
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GPU DECOUPLING NVVDD



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Circuitry Co., Ltd.
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UNDER GPU

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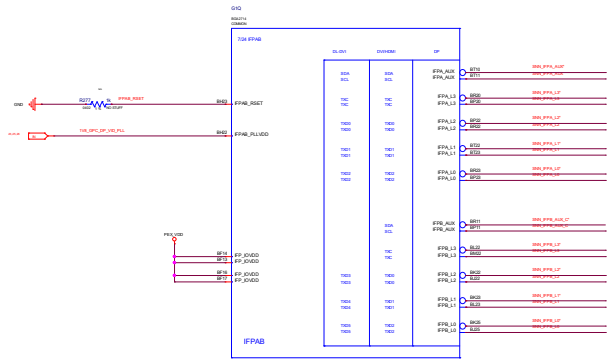
ASSEMBLY	ASSEMBLY DESCRIPTION
PCB CO-LAYOUT	GPU DECOUPLING



GPU Decoupling
Capacitor Co-Layout
NVIDIA Logo

Doc No: GPU-Decoupling-Co-Layout
Date: Friday, July 11, 2014
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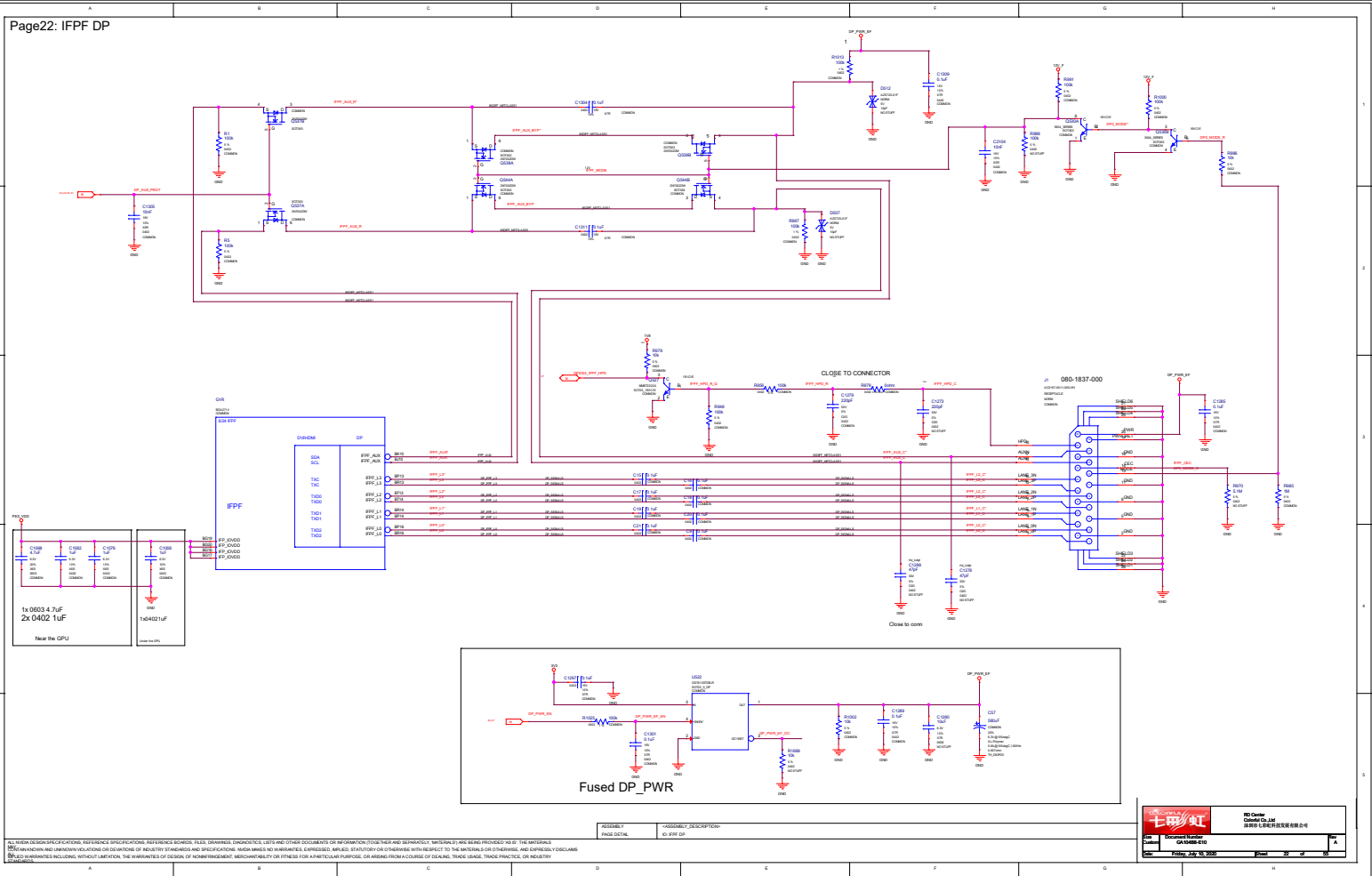
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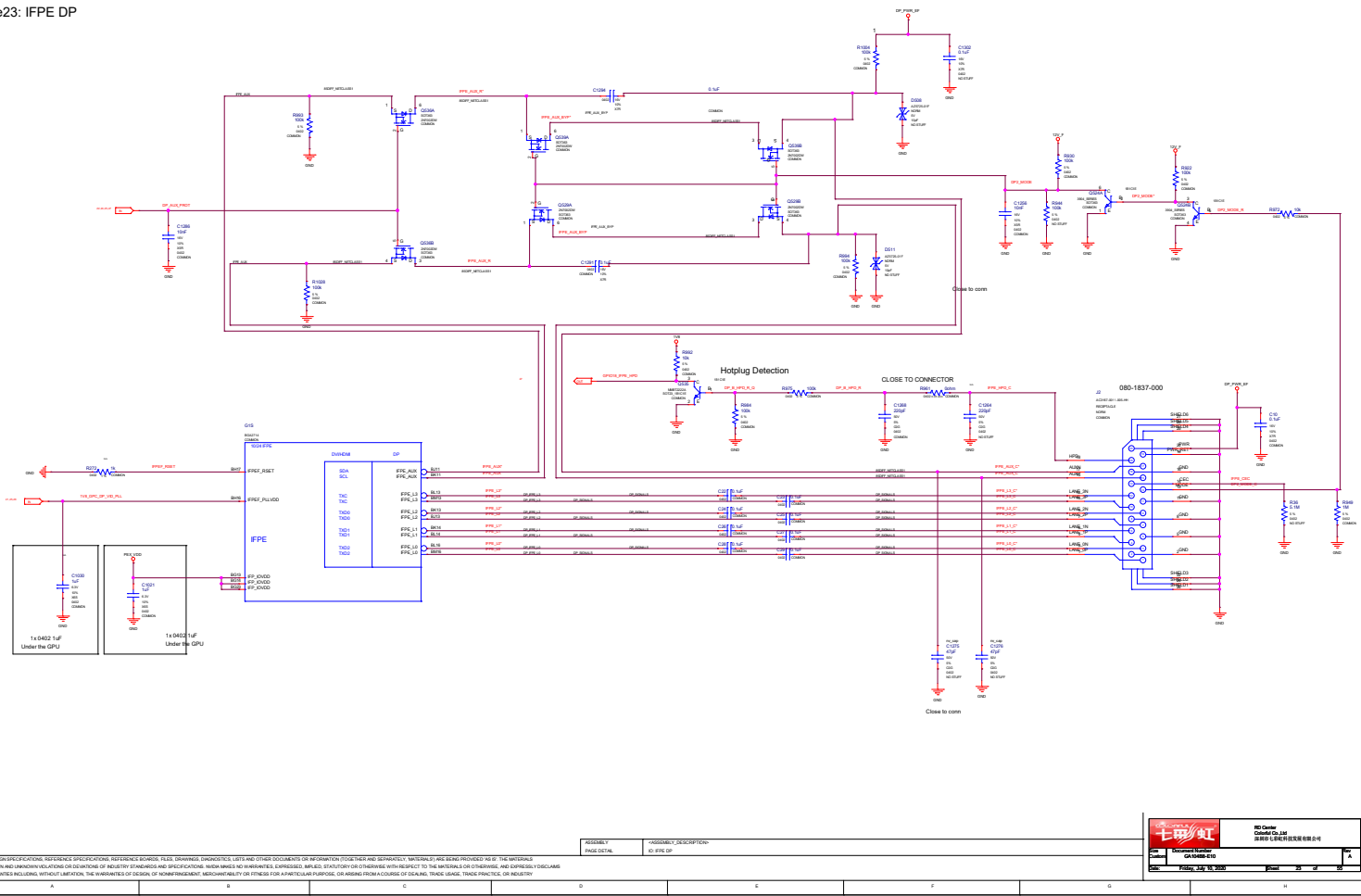


IFPAB DVI-D-DL
IFPAB DVI-D-DL

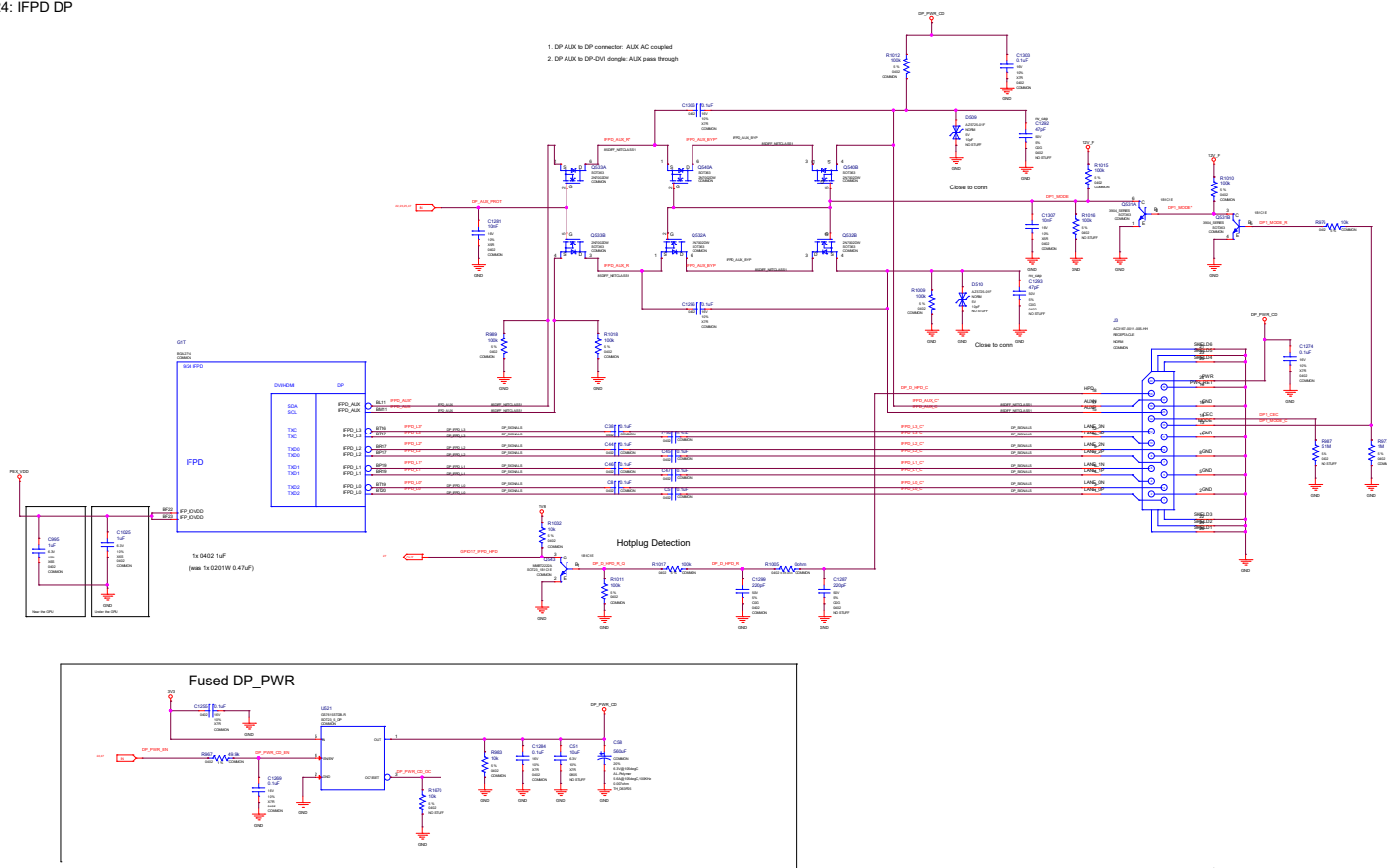
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IFPAB DVI-D-DL






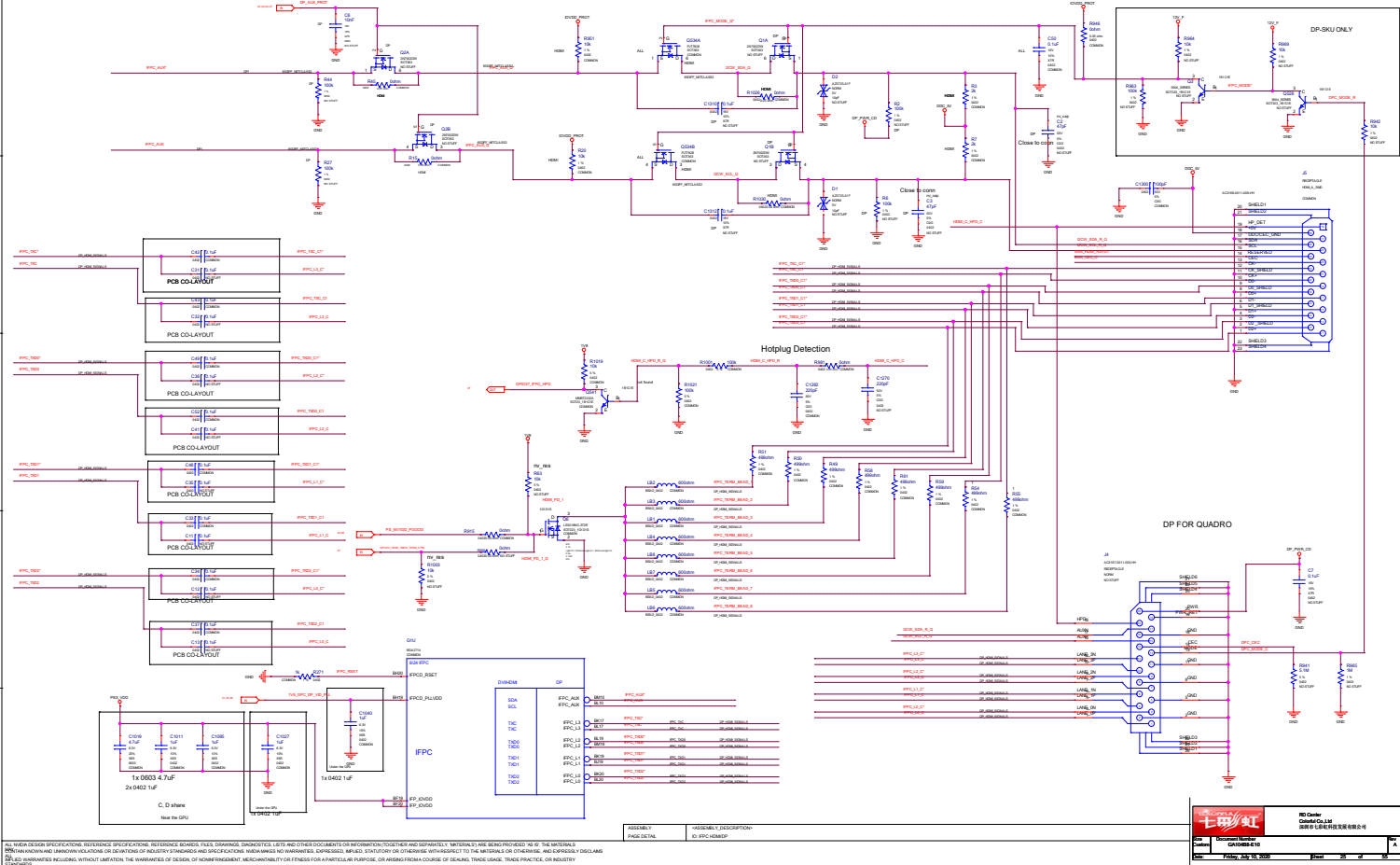
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Date:	Friday, July 10, 2020	Printed:	24 of 50

Page25: IFPC HDMI/DP



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SHI ZHUO HONG ELECTRONICS CO., LTD.

SHI ZHUO HONG ELECTRONICS CO., LTD.

Assembly

Page 25 of 25

Rev. 1.0

2023.08.15

Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	0001	RAMCFG MICRON 8Gb 7GHz
L	H	L	0010	RAMCFG HYNEX 8Gb 7GHz
H	H	L	0011	RAMCFG SAMSUNG 16Gb 8GHz
TBD				

H:High :Tied to 1.8V
M:Middle:Tied to 0.9V
L:Low :Tied to 0V

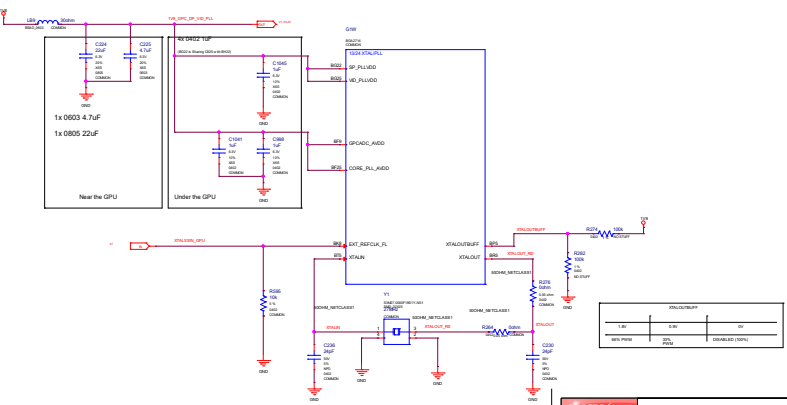
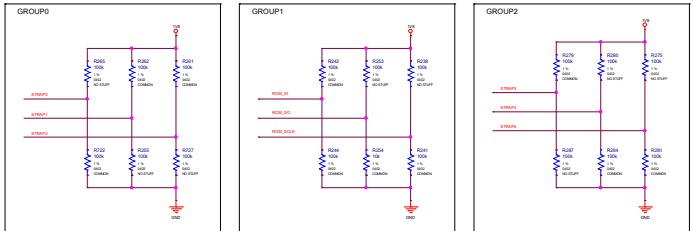
ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0]FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
H	H	M	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
H	L	M	1	0	0	0
H	H	H	0	1	1	1
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

H:High :Tied to 1.8V
M:Middle:Tied to 0.9V
L:Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



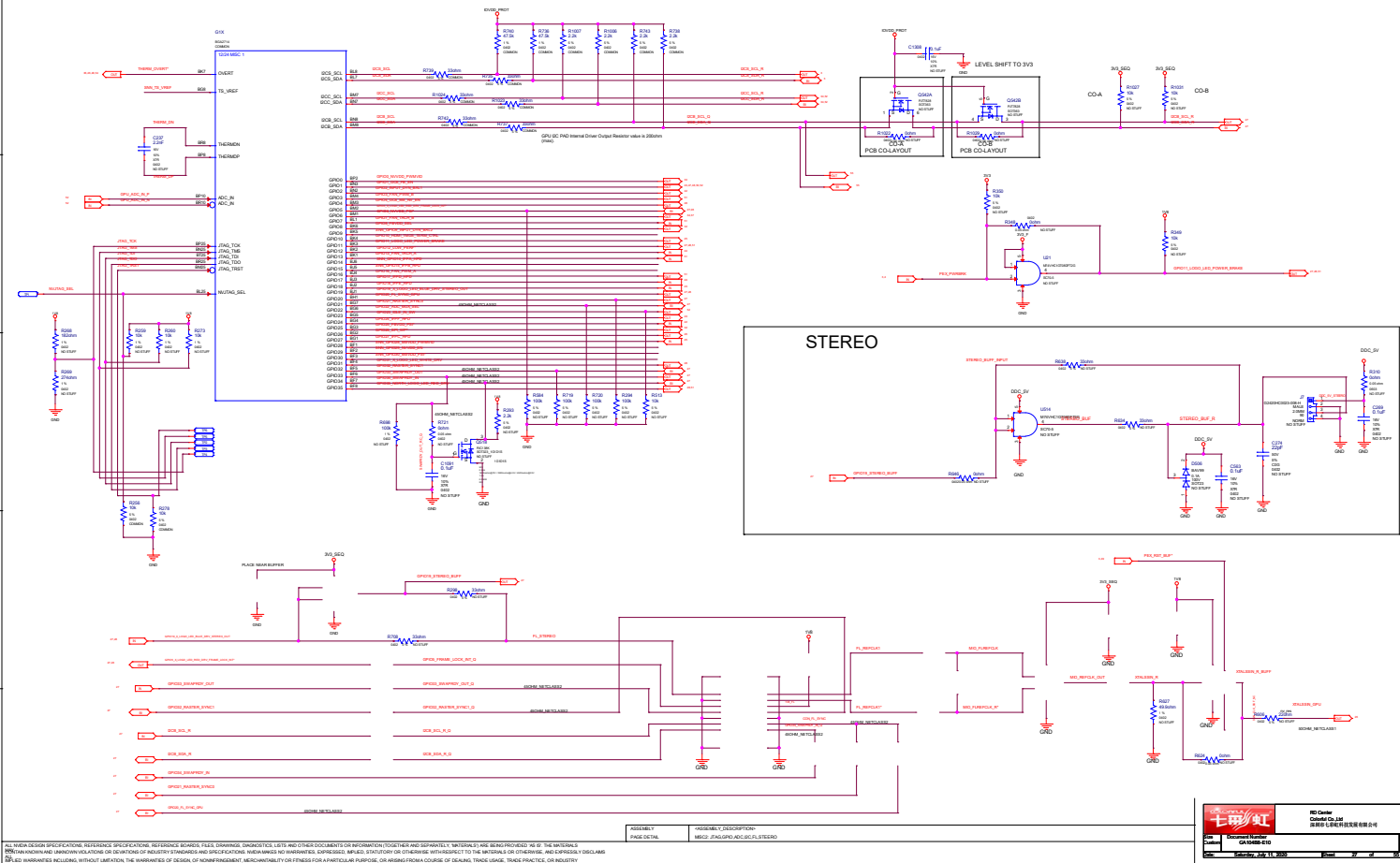
XTALOUT	XTALIN	XTAL
1.8V	0.9V	0V
1.8V	0.9V	0V

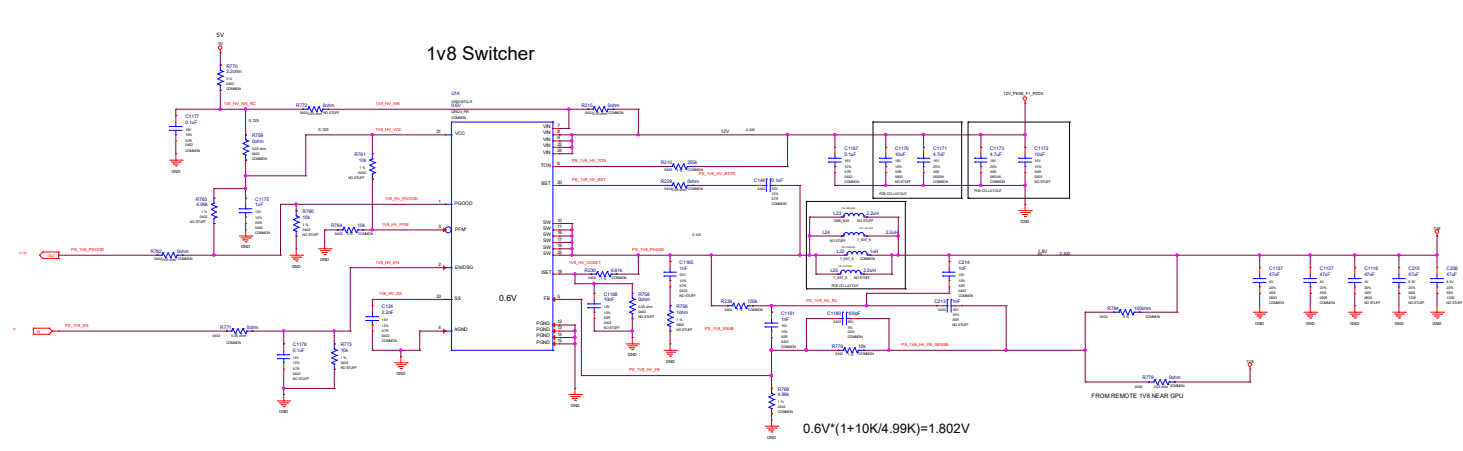


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ASSEMBLY: MISC2: ROM, XTAL, STRAPS

PC Control
Control Co., Ltd.
0A1000-010
Rev. 1.0, 2010

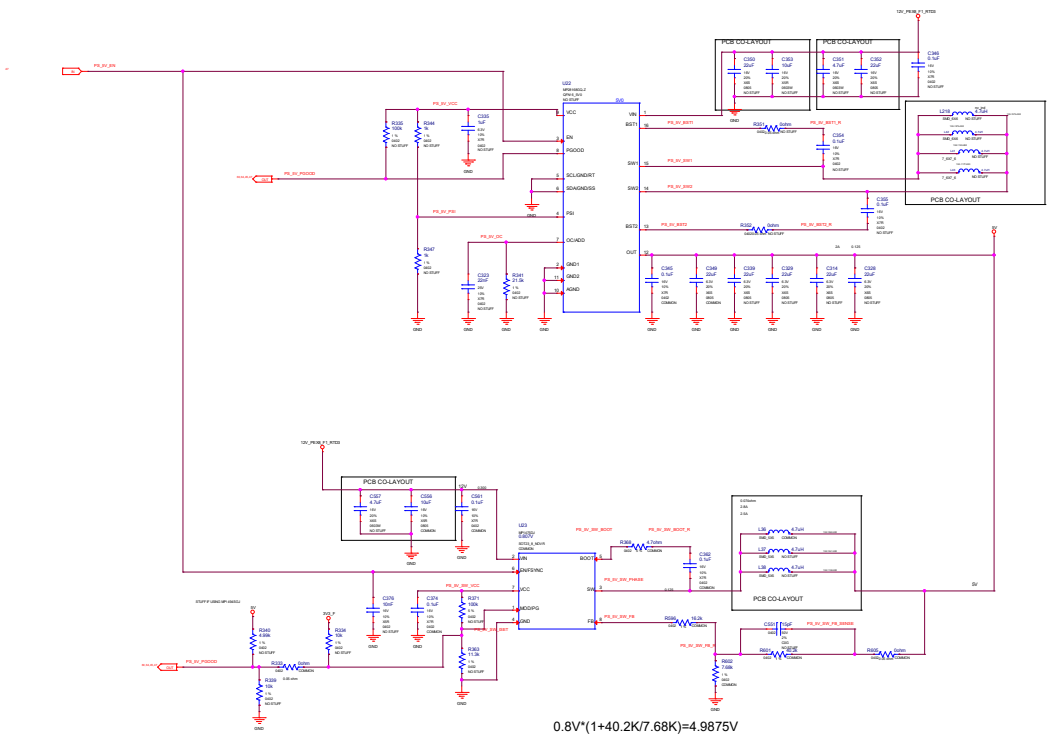




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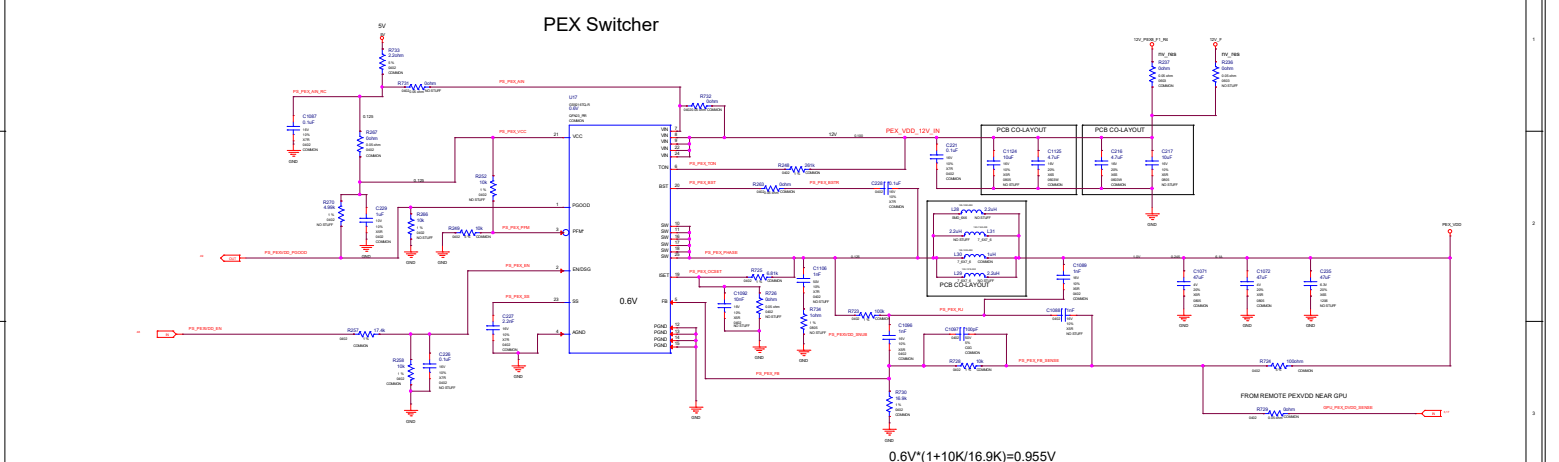
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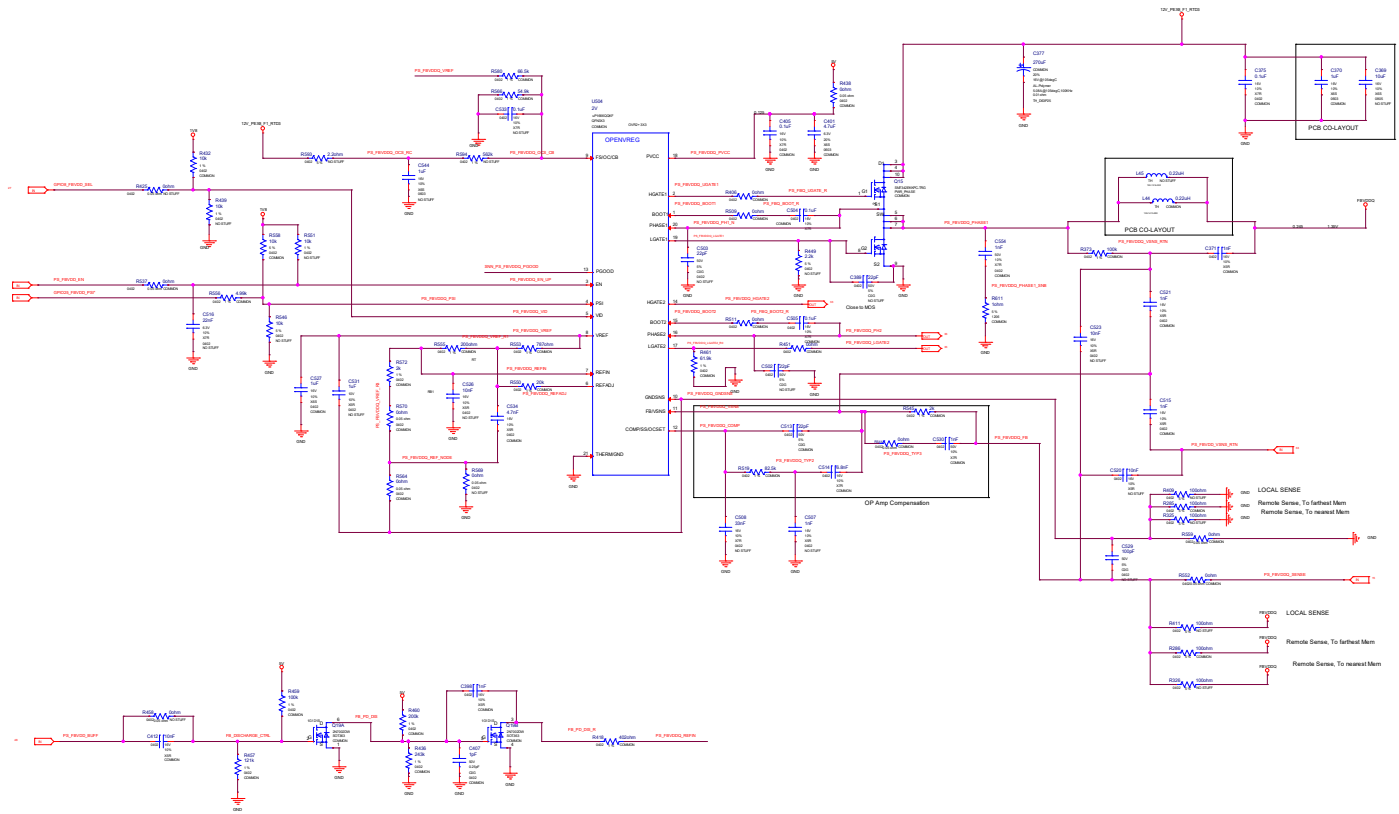
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ASSEMBLY	ASSEMBLY DESCRIPTION
PS: 5V	PS: 5V

PS: 5V	
Shenzhen Qianxin Technology Co., Ltd.	
Shenzhen, China	
Date: 2023.10.10	
Version: 1.0	
Page: 30 of 30	




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<p>DATE: Friday, July 2, 2021</p>		TIME: 10:00	PAGE: 31	OF: 52



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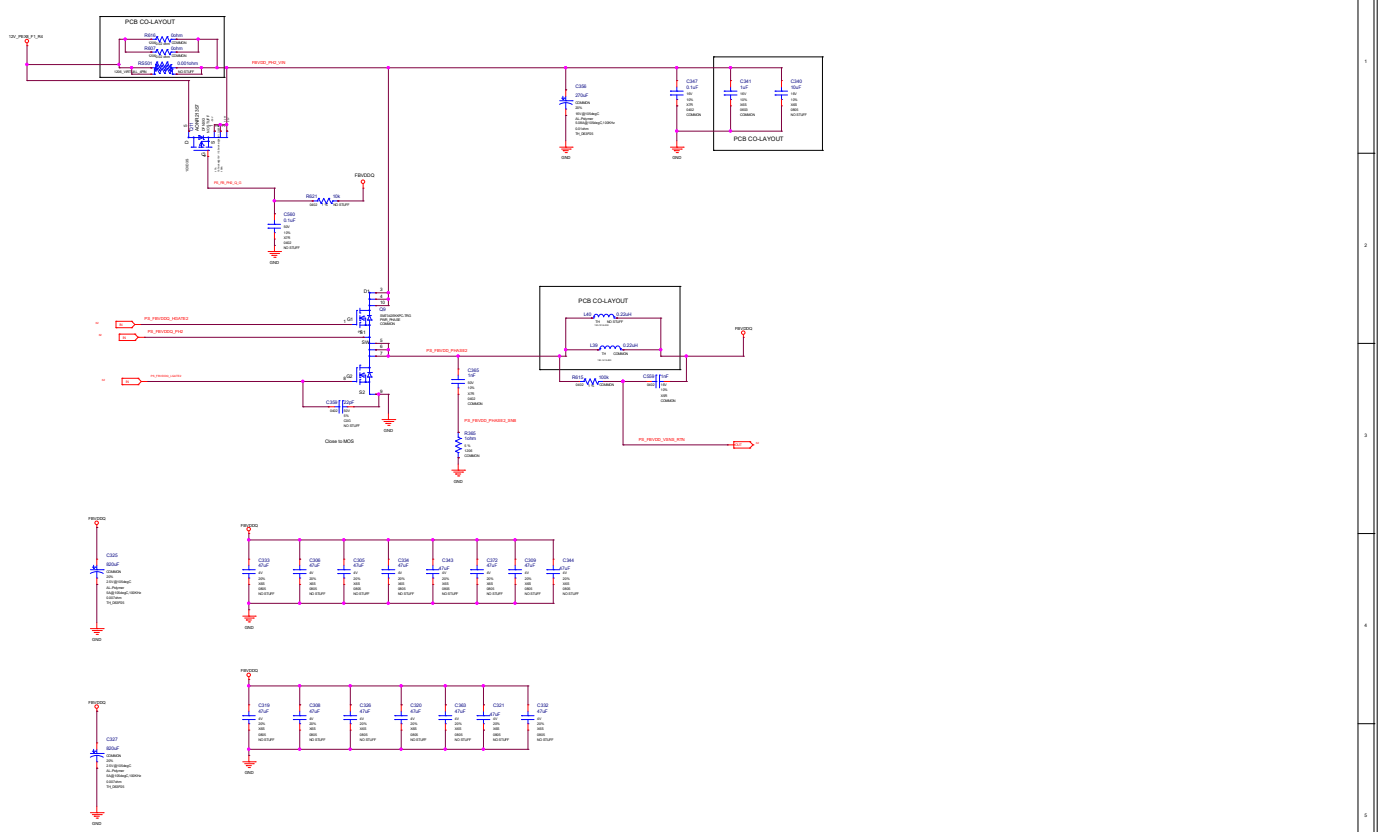



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Version: 1.0

Page 32 of 32

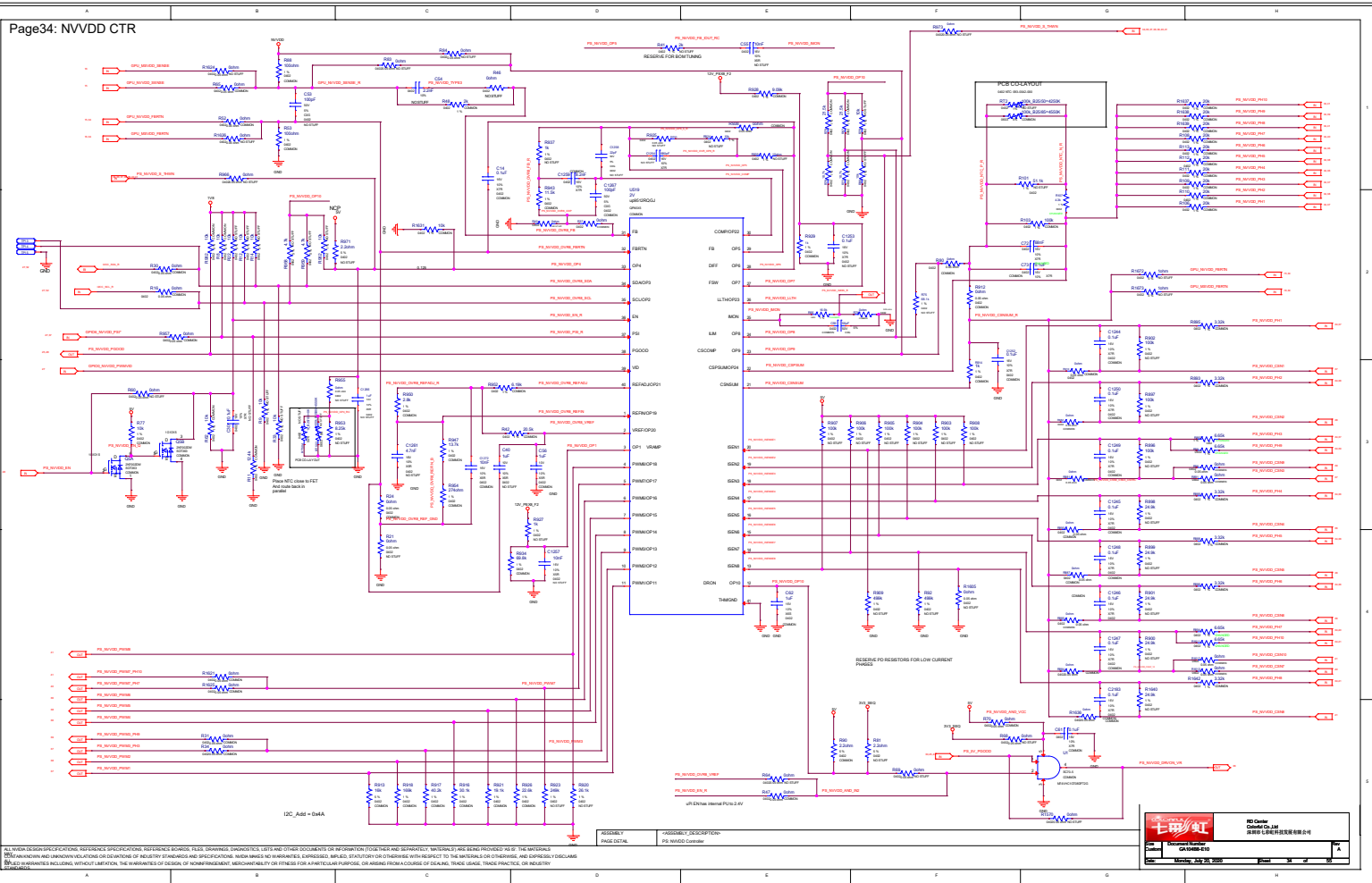
FBVDD PH2 INPUT ANTI-BACKDRIVE



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		<div> Document Number </div> <div> Page </div>

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Date Customer:	Document Number GA1048B-E10	Rev A	
Date:	Friday, July 15, 2020	Sheet	33 of 35



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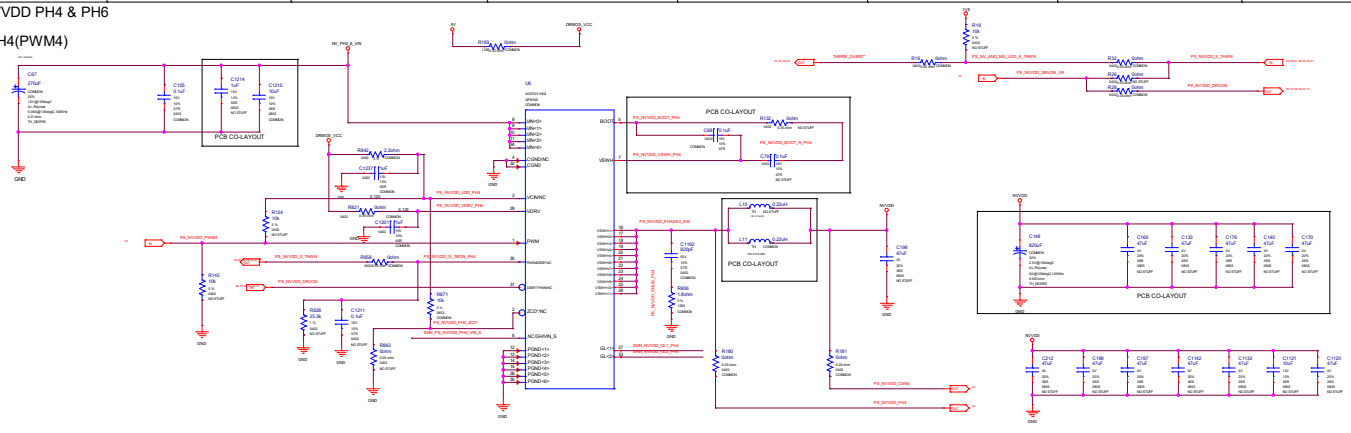
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PAGE 2 OF 2

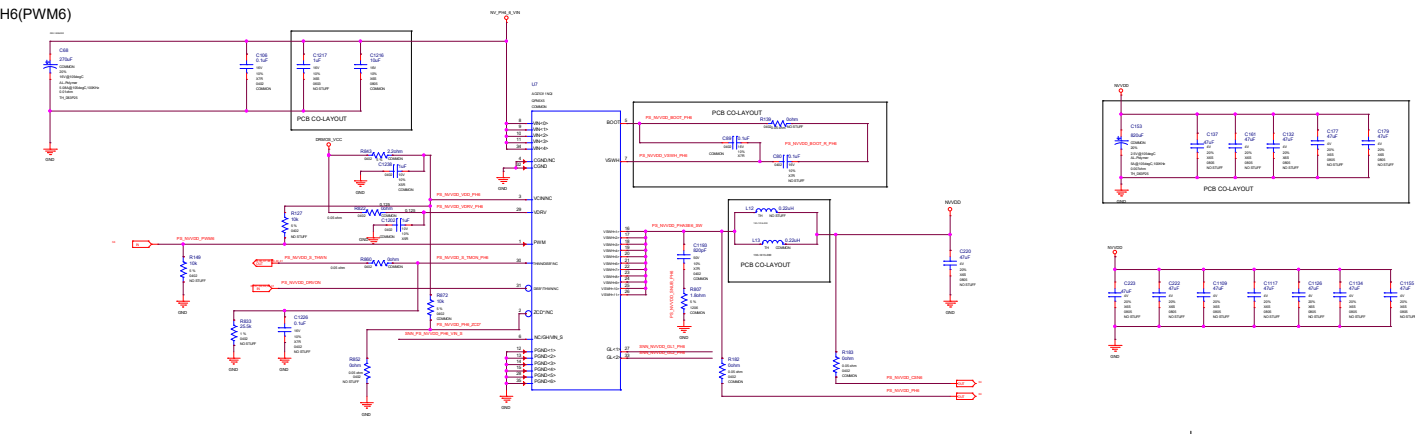
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Page36: NVVDD PH4 & PH6
NVVDD PH4(PWM4)



NVVDD PH6(PWM6)



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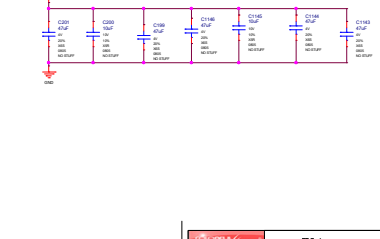
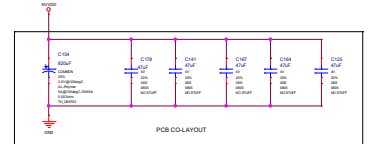
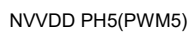
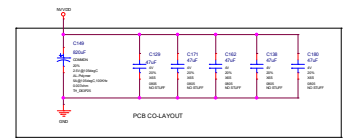
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PH4	PH4



PH4
PH4

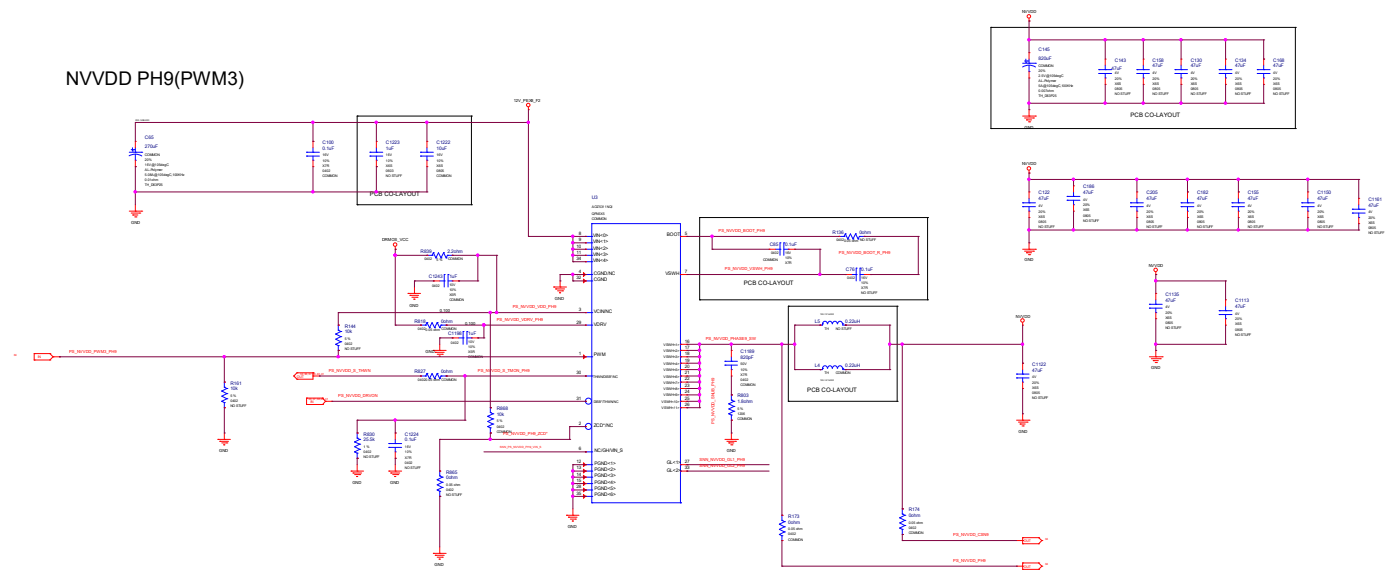
PH4
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PH4	PH4
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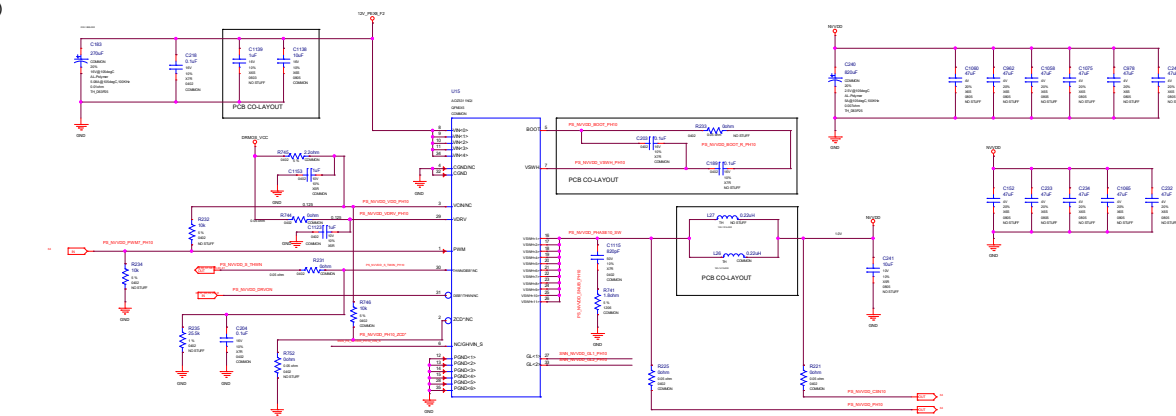
NVVDD PH9(PWM3)



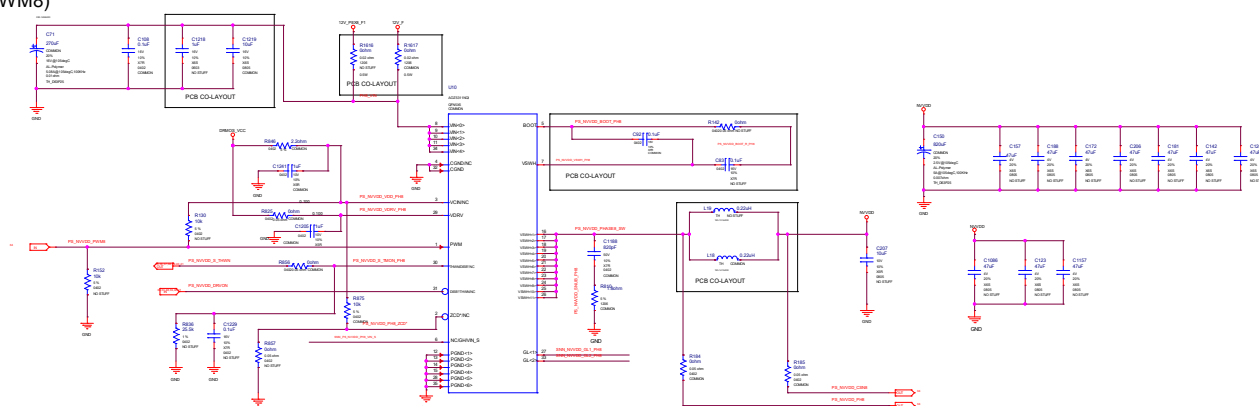
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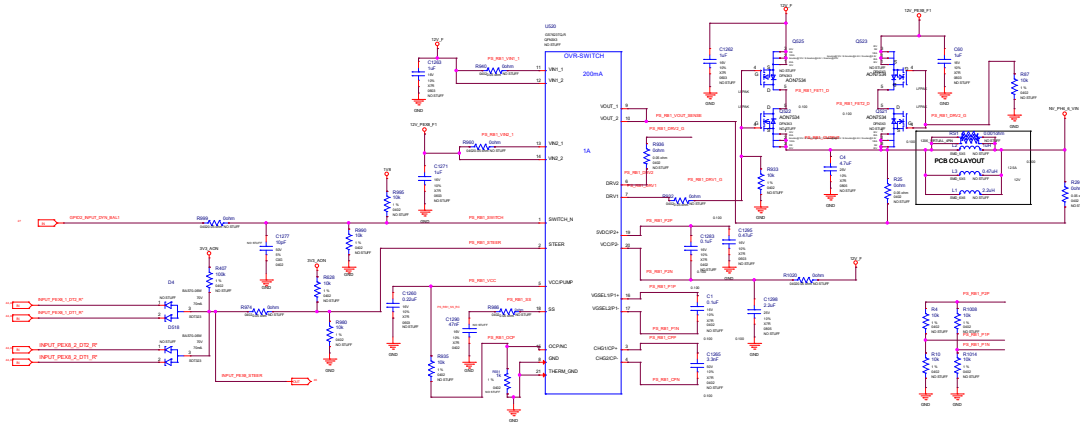
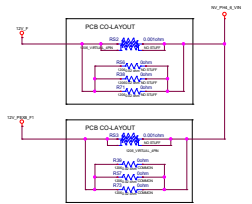
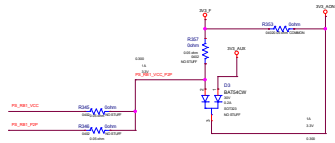


NVVDD PH8(PWM8)



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PAGE DETAIL	PS: NWDD PHH3, PH8

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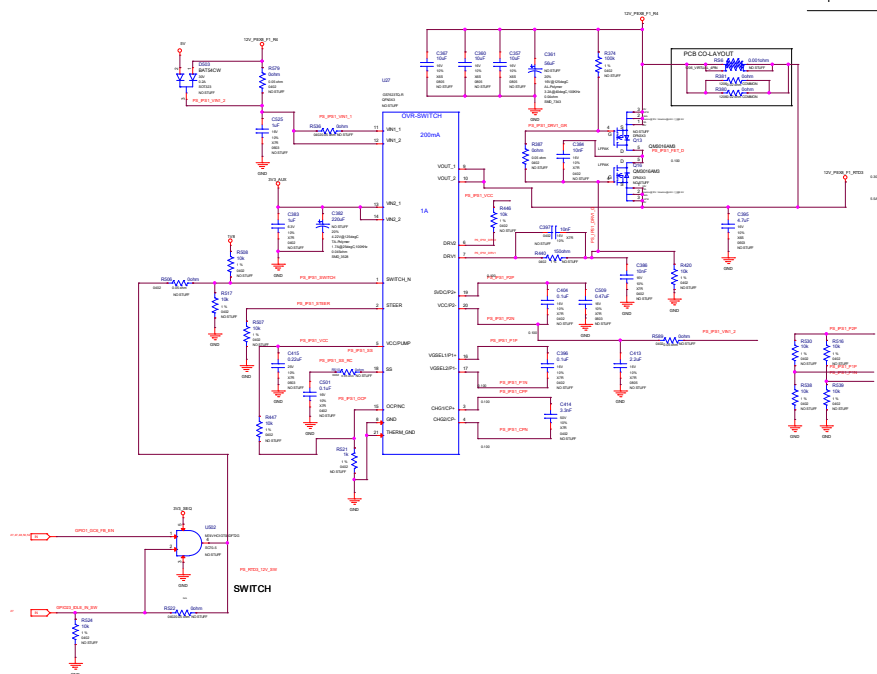


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PAGE DETAIL	P5: OVR5_INPUT POWER



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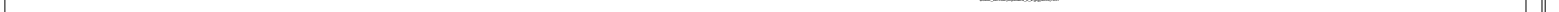
AND GATE LOGIC					
GPI01	GPI029	SWITCH	VOUT	SWITCH	VOUT
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0	1	0	12V	1	VOUT = VIN2
1	0	0	12V		
1	1	1	3V3A		

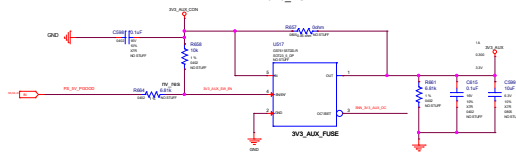
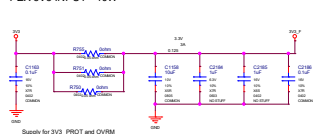
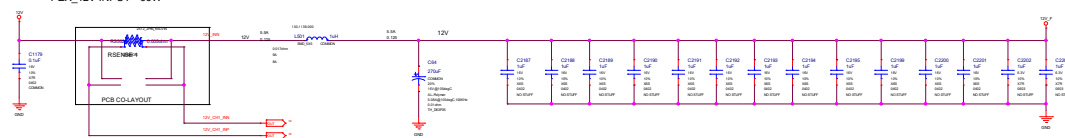


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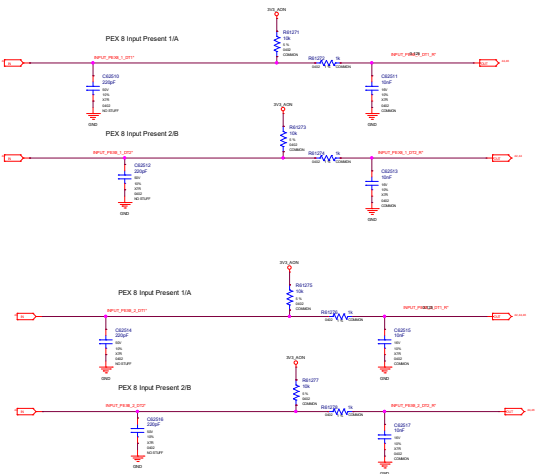
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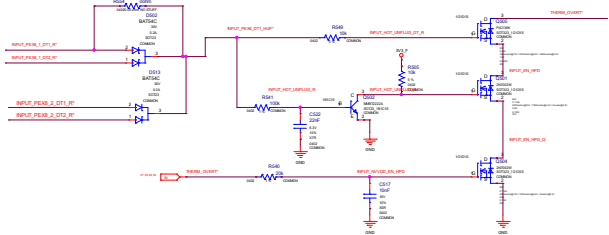


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PAGE DIGITAL	PS: PEX_12V, PEX_3V3 AND A3V3_AUX

Page46: STEERING, UPB, HOT UNPLUG

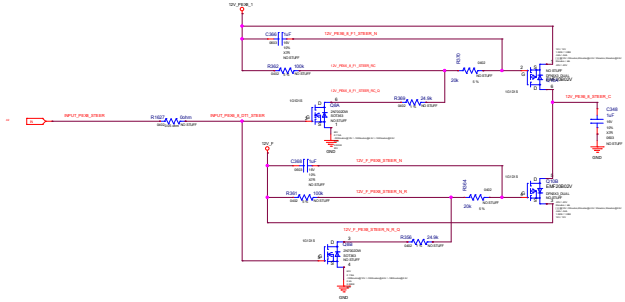


POWER CONNECTOR HOT-UNPLUG DETECT



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

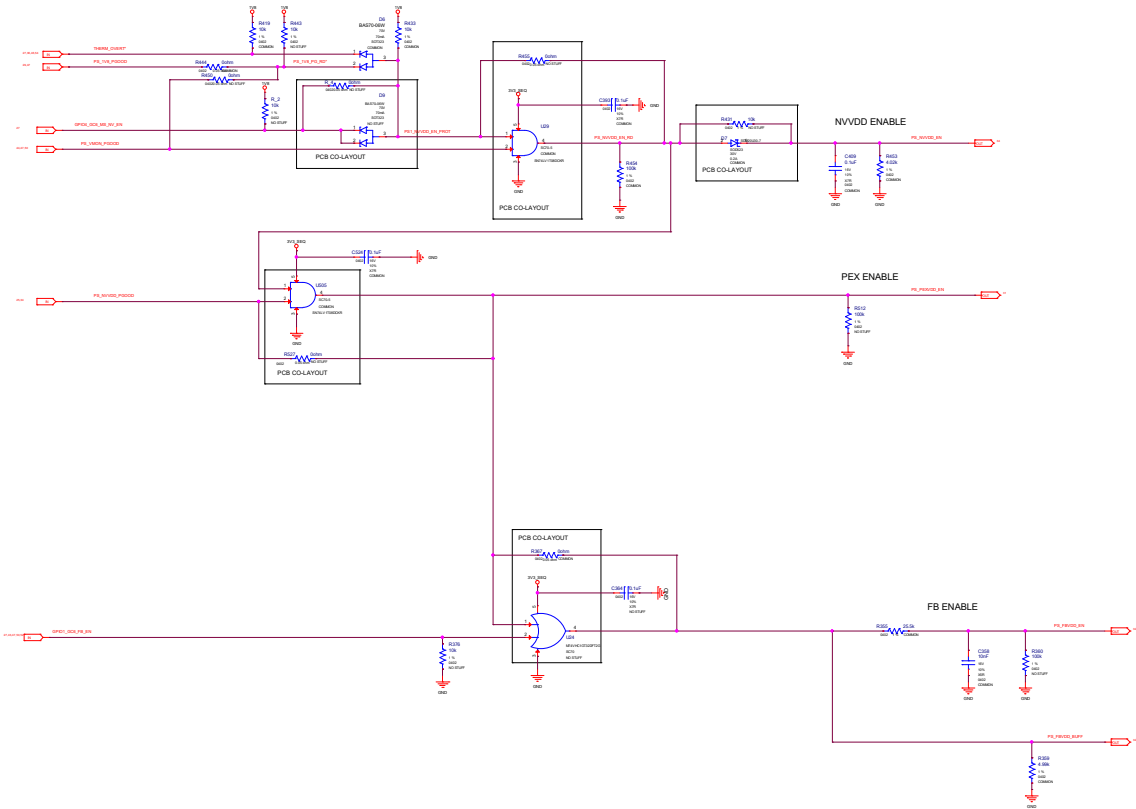


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ASSEMBLY: POWER CONNECTOR
DESCRIPTION: POWER CONNECTOR



Page48: SEQ:NVVDD, PEX, FBVDDQ ENABLE



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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB CO-LAYOUT	SEQ:NVVDD, PEX, FBVDDQ ENABLE



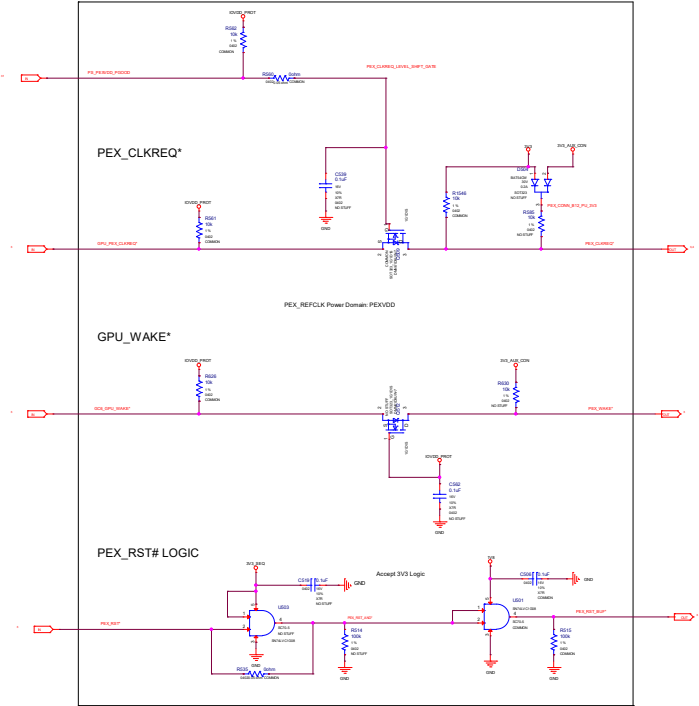
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Document Name
SEQ:NVVDD, PEX, FBVDDQ ENABLE

Rev. 1.0

Date: 2023.03.16

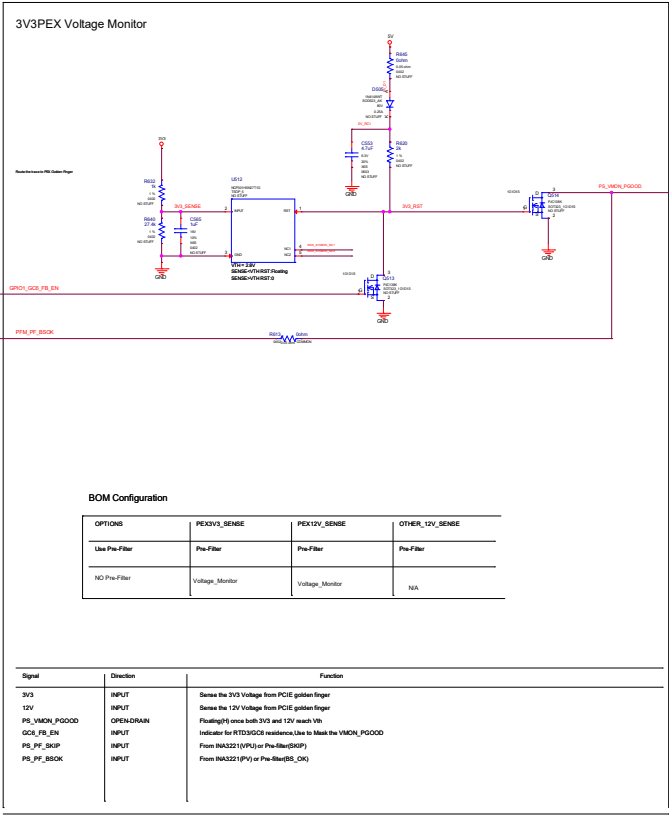
Page: 48 of 48



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ASSEMBLY	ASSEMBLY DESCRIPTION
PEX/CLKREQ	PEX/CLKREQ

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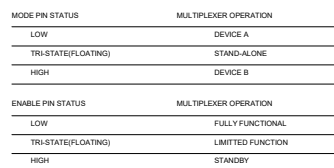
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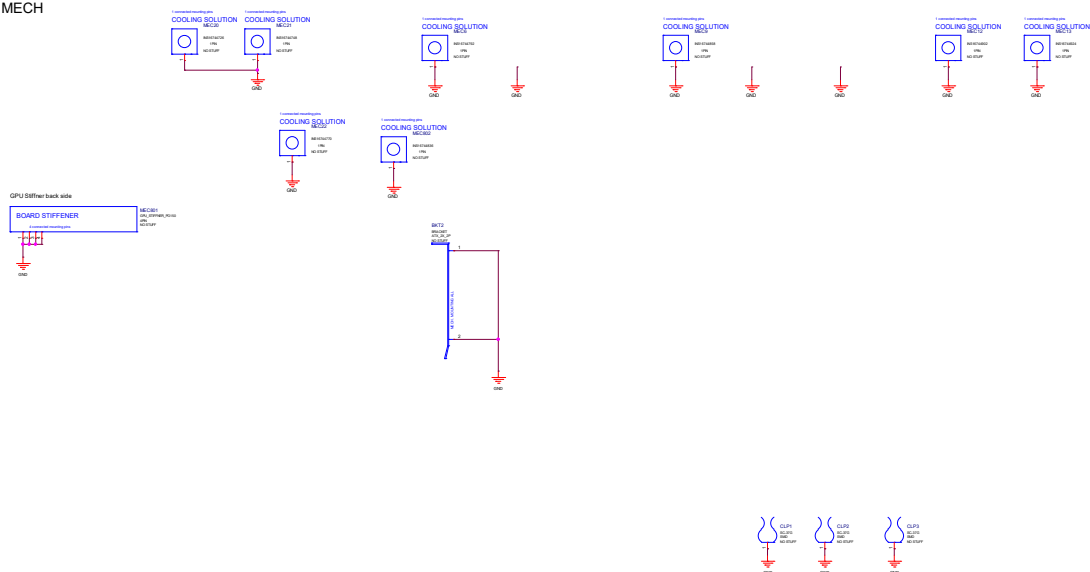
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