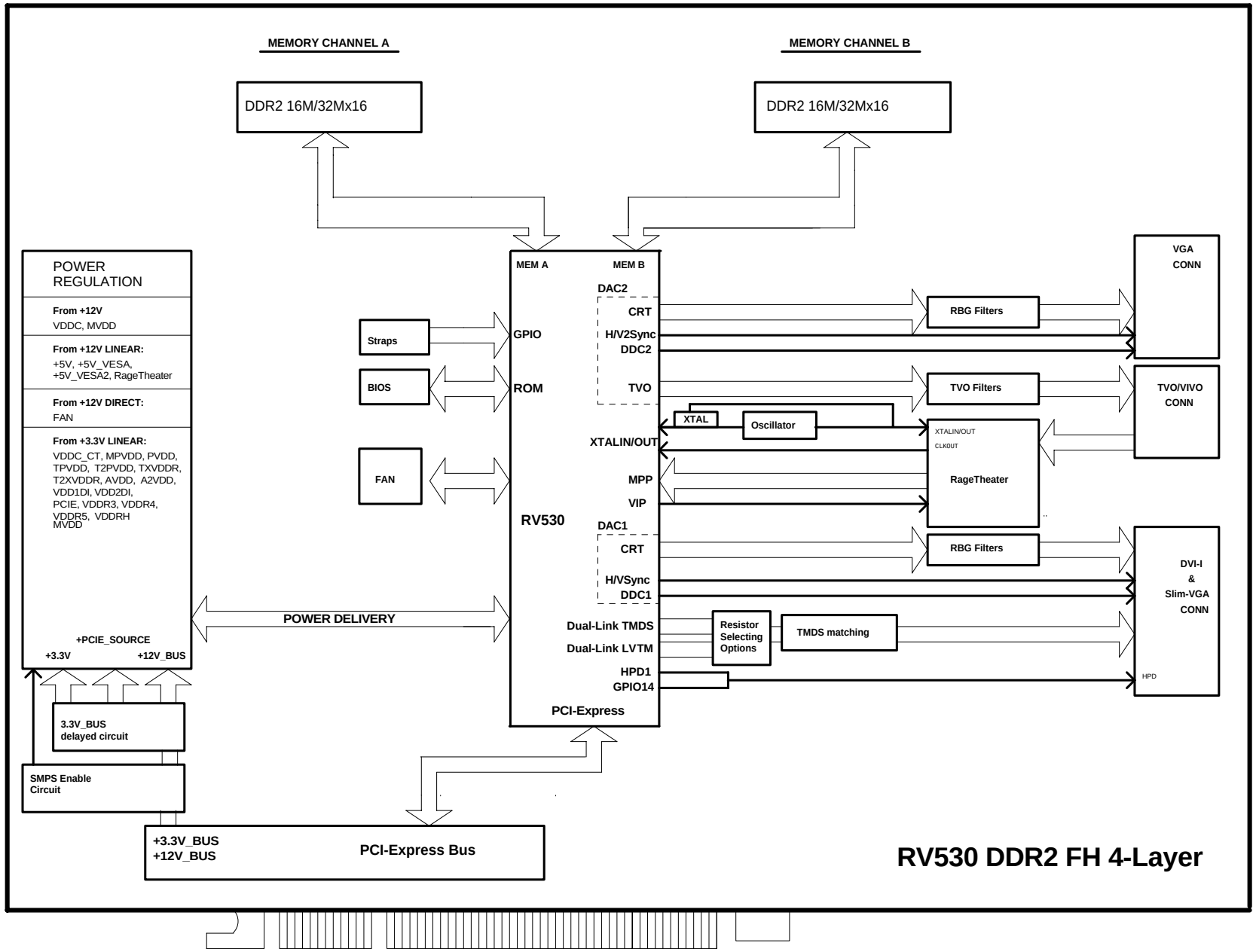


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|---|---|
| Micro-Star International Co., LTD. | |
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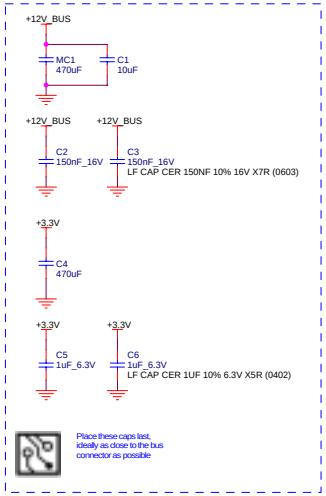
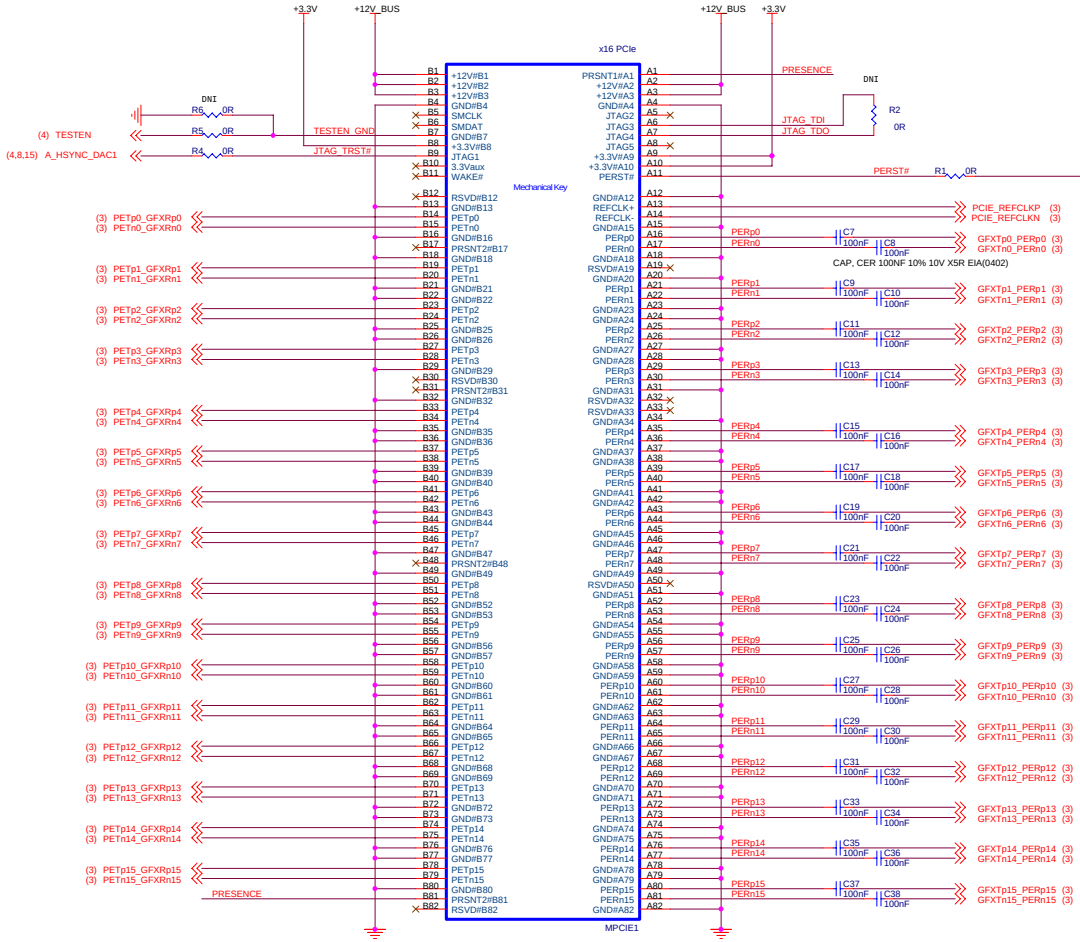
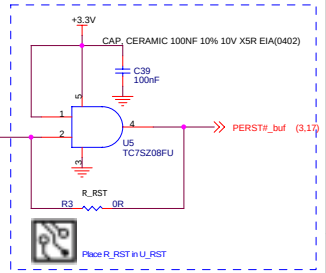
# PCI-EXPRESS EDGE CONNECTOR




Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

| SYMBOL LEGEND | |
|---|---|
| DNI | DO NOT INSTALL |
| # | ACTIVE LOW |
| | DIGITAL GROUND |
| | ANALOG GROUND |

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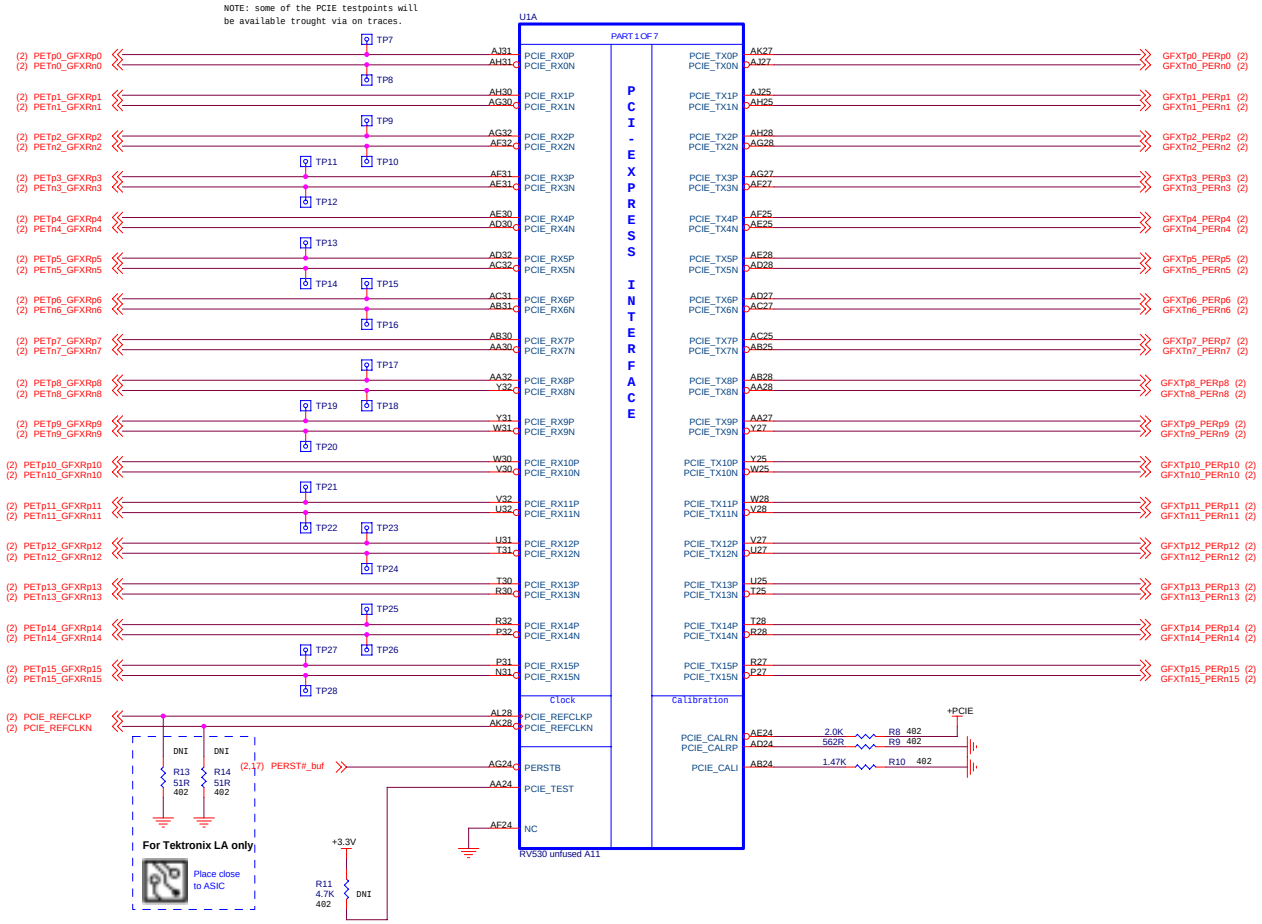


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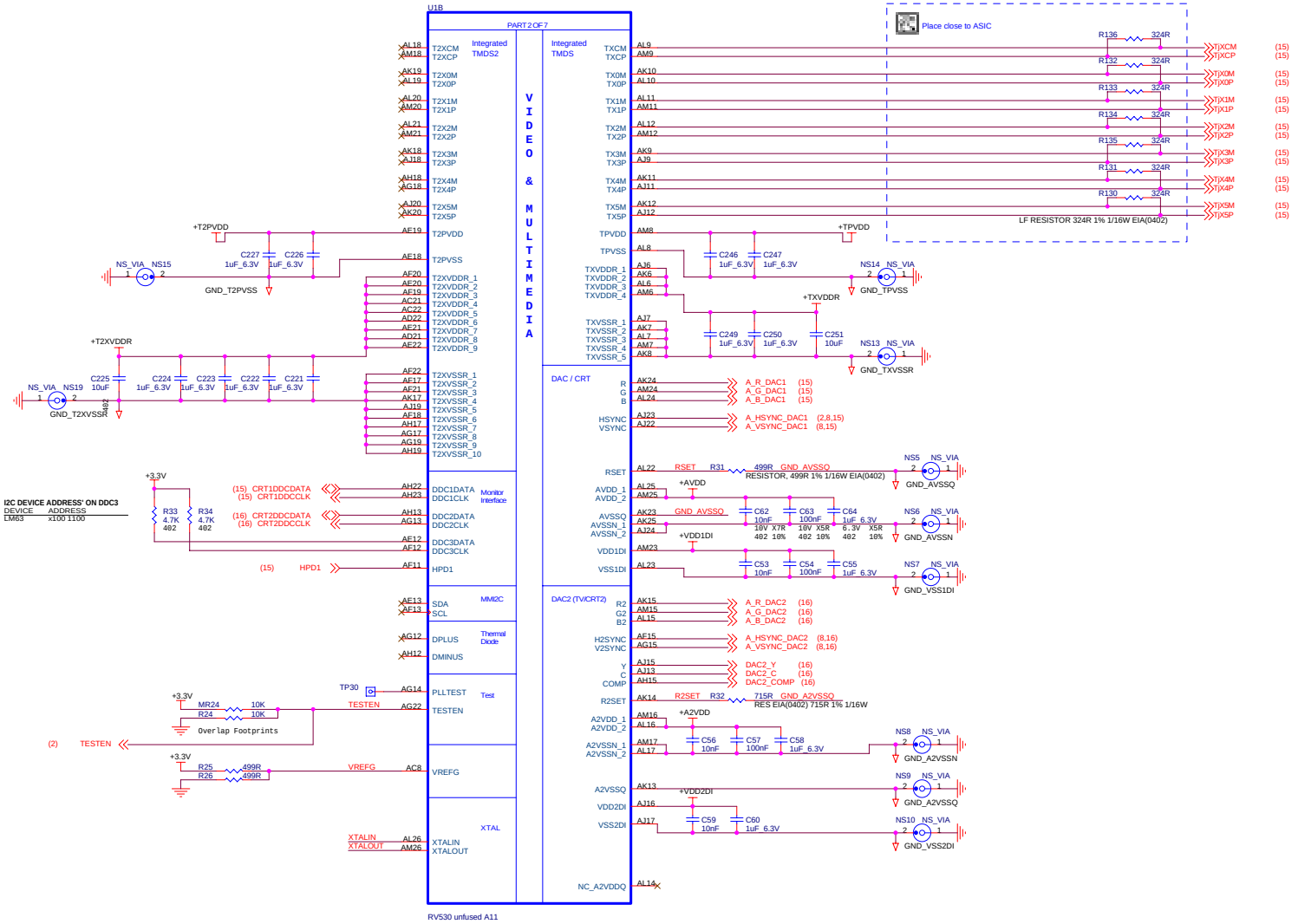
U1B
PART 2 OF 7
VIDEO & MULTIMEDIA
Integrated TMDS2
Integrated TMDS
T2XCM
T2XCP
T2X0M
T2X0P
T2X1M
T2X1P
T2X2M
T2X2P
T2X3M
T2X3P
T2X4M
T2X4P
T2X5M
T2X5P
TXCM
TXCP
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TX3M
TX3P
TX4M
TX4P
TX5M
TX5P
Place close to ASIC
LF RESISTOR 324R 1% 1/16W EIA(0402)
+T2PVDD
+TPVDD
+TXVDDR
+T2XVDDR
+3.3V
+AVDD
+VDD1DI
+VDD2DI
+A2VDD
GND_T2PVSS
GND_TPVSS
GND_TXVSSR
GND_T2XVSSR
GND_AVSSQ
GND_AVSSN
GND_VSS1DI
GND_A2VSSN
GND_A2VSSQ
GND_VSS2DI
T2PVDD
T2PVSS
T2XVDDR_1
T2XVDDR_2
T2XVDDR_3
T2XVDDR_4
T2XVDDR_5
T2XVDDR_6
T2XVDDR_7
T2XVDDR_8
T2XVDDR_9
T2XVSSR_1
T2XVSSR_2
T2XVSSR_3
T2XVSSR_4
T2XVSSR_5
T2XVSSR_6
T2XVSSR_7
T2XVSSR_8
T2XVSSR_9
T2XVSSR_10
TPVDD
TPVSS
TXVDDR_1
TXVDDR_2
TXVDDR_3
TXVDDR_4
TXVSSR_1
TXVSSR_2
TXVSSR_3
TXVSSR_4
TXVSSR_5
DAC / CRT
R
G
B
HSYNC
VSYNC
A_R_DAC1 (15)
A_G_DAC1 (15)
A_B_DAC1 (15)
A_HSYNC_DAC1 (2,8,15)
A_VSYNC_DAC1 (8,15)
RSET
AVDD_1
AVDD_2
AVSSQ
AVSSN_1
AVSSN_2
VDD1DI
VSS1DI
RESISTOR, 499R 1% 1/16W EIA(0402)
DDC1DATA
DDC1CLK
DDC2DATA
DDC2CLK
DDC3DATA
DDC3CLK
HPD1
Monitor Interface
I2C DEVICE ADDRESS' ON DDC3
DEVICE ADDRESS
LM63 x100 1100
(15) CRT1DDCDATA
(15) CRT1DDCCLK
(16) CRT2DDCDATA
(16) CRT2DDCCLK
(15) HPD1
SDA
SCL
MM#2C
DPLUS
DMINUS
Thermal Diode
DAC2 (TV/CRT2)
R2
G2
B2
H2SYNC
V2SYNC
Y
C
COMP
R2SET
A_R_DAC2 (16)
A_G_DAC2 (16)
A_B_DAC2 (16)
A_HSYNC_DAC2 (8,16)
A_VSYNC_DAC2 (8,16)
DAC2_Y (16)
DAC2_C (16)
DAC2_COMP (16)
RES EIA(0402) 715R 1% 1/16W
A2VDD_1
A2VDD_2
A2VSSN_1
A2VSSN_2
A2VSSQ
VDD2DI
VSS2DI
PLLTEST
TESTEN
Test
Overlap Footprints
TP30
VREFG
XTALIN
XTALOUT
XTAL
NC_A2VDDQ
RV530 unfused A11
I2C DEVICE ADDRESS' ON DDC3
Place R_RTCLK close to XTAL so the main clock line has shortest stub
Change to 10ppm/10ppm p/n 50282700006
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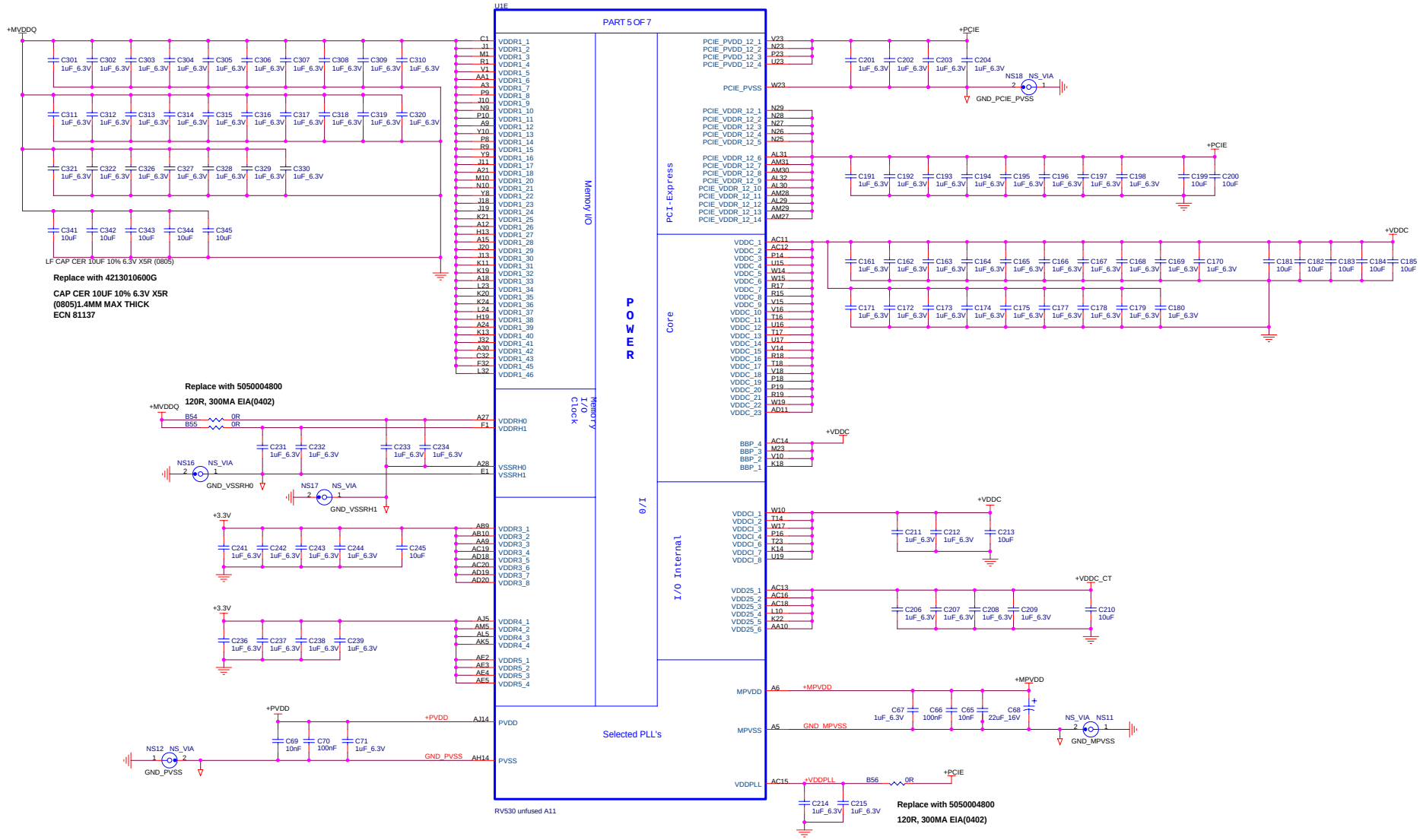


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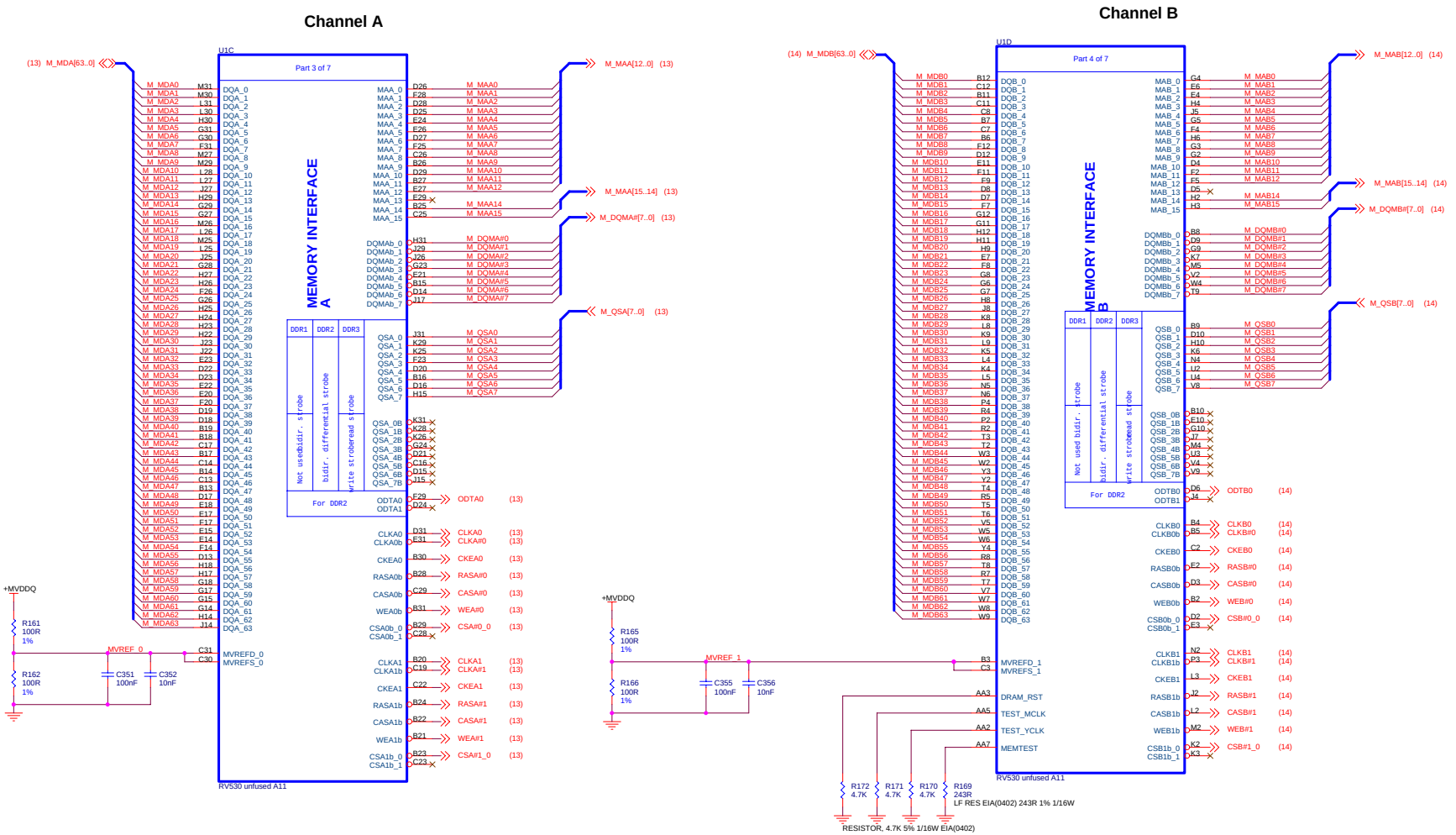
# RV530 MEMORY CHANNELS A and B

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|---|---|---|
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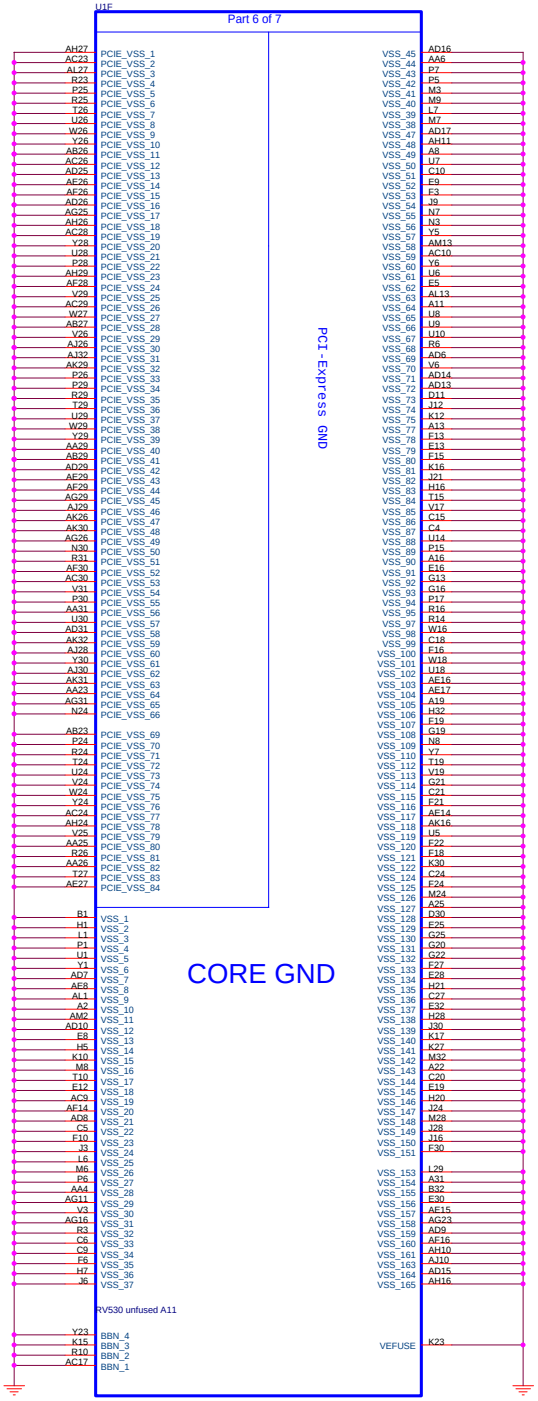


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|---|---|
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| MS-V040 RV530/DDRII | |
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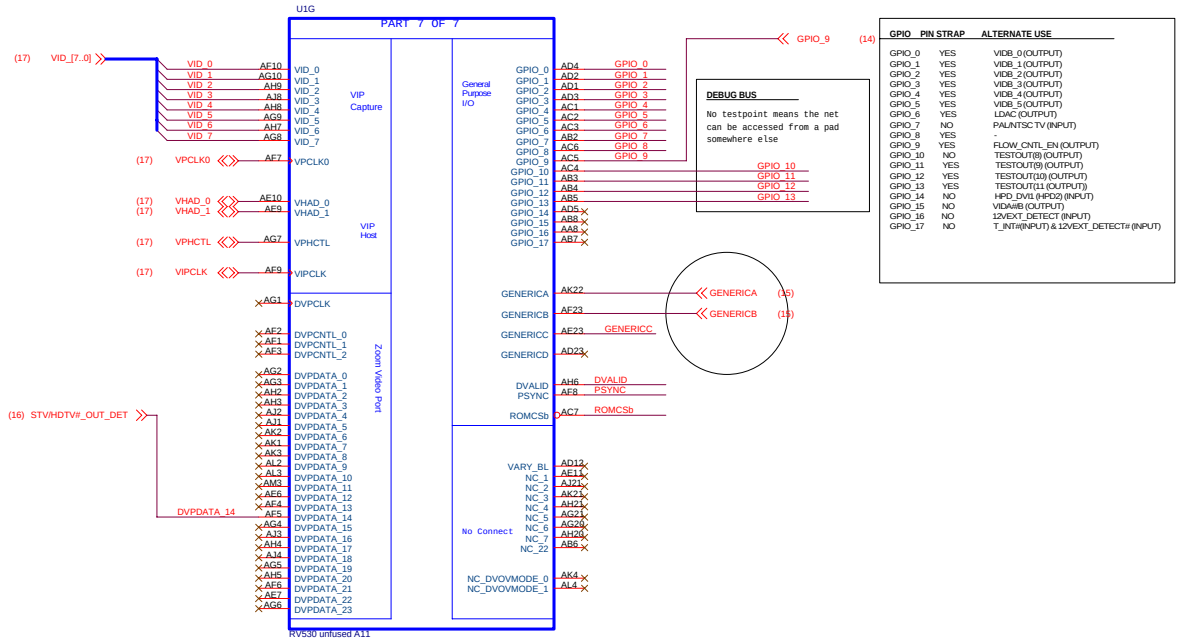
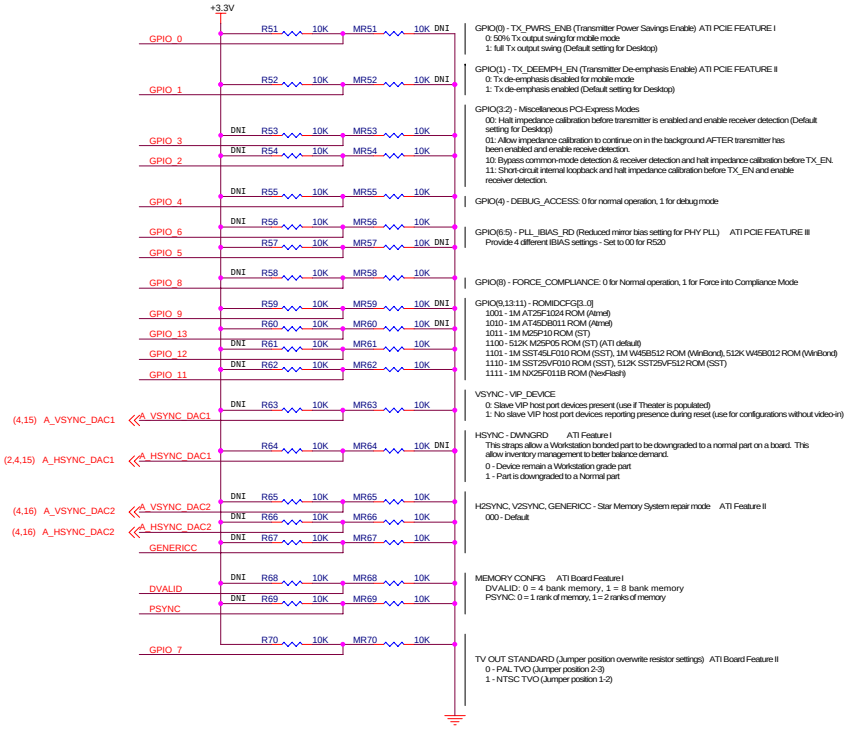
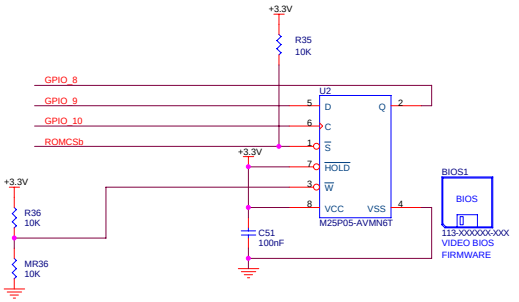



| GPIO | PIN STRAP | ALTERNATE USE |
|---|---|---|
| GPIO_0 | YES | VIDB_0 (OUTPUT) |
| GPIO_1 | YES | VIDB_1 (OUTPUT) |
| GPIO_2 | YES | VIDB_2 (OUTPUT) |
| GPIO_3 | YES | VIDB_3 (OUTPUT) |
| GPIO_4 | YES | VIDB_4 (OUTPUT) |
| GPIO_5 | YES | VIDB_5 (OUTPUT) |
| GPIO_6 | YES | LDAC (OUTPUT) |
| GPIO_7 | NO | PAL/NTSC TV (INPUT) |
| GPIO_8 | YES | - |
| GPIO_9 | YES | FLOW_CNTL_EN (OUTPUT) |
| GPIO_10 | NO | TESTOUT(8) (OUTPUT) |
| GPIO_11 | YES | TESTOUT(9) (OUTPUT) |
| GPIO_12 | YES | TESTOUT(10) (OUTPUT) |
| GPIO_13 | YES | TESTOUT(11 (OUTPUT)) |
| GPIO_14 | NO | HPD_DVI1 (HPD2) (INPUT) |
| GPIO_15 | NO | VIDA/#B (OUTPUT) |
| GPIO_16 | NO | 12VEXT_DETECT (INPUT) |
| GPIO_17 | NO | T_INT#(INPUT) & 12VEXT_DETECT# (INPUT) |

## PIN BASED STRAPS

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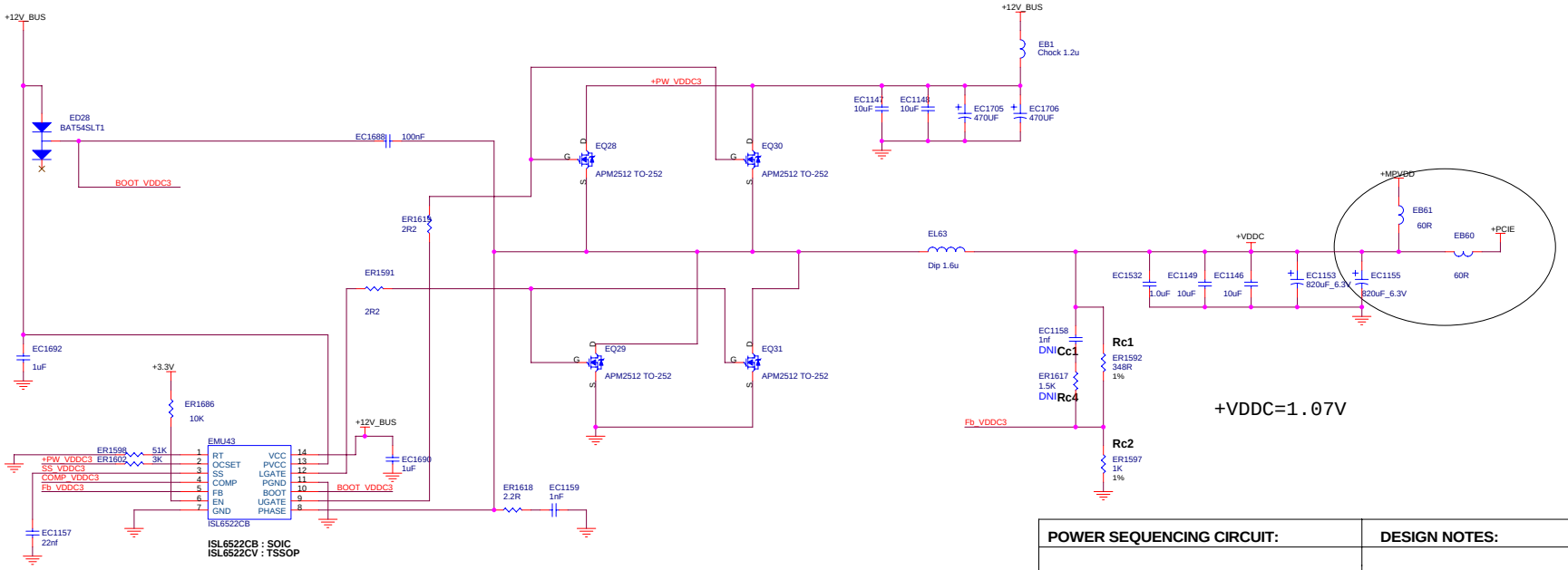
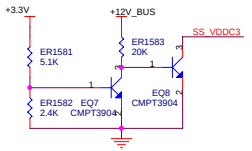
# CORE REGULATOR VDDC




+VDDC=1.07V

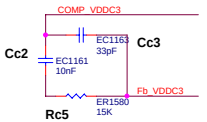
Lower MOSFET should be surrounded by a lot of copper for heat dissipation

**POWER SEQUENCING CIRCUIT:**




**DESIGN NOTES:**

**Compensation Circuit**




## FOR ALTERNATE #1

Remove R374, R375, R371, C168 and U32

Install R370, R112, R954, R305-R308, C166, C159 and MU32

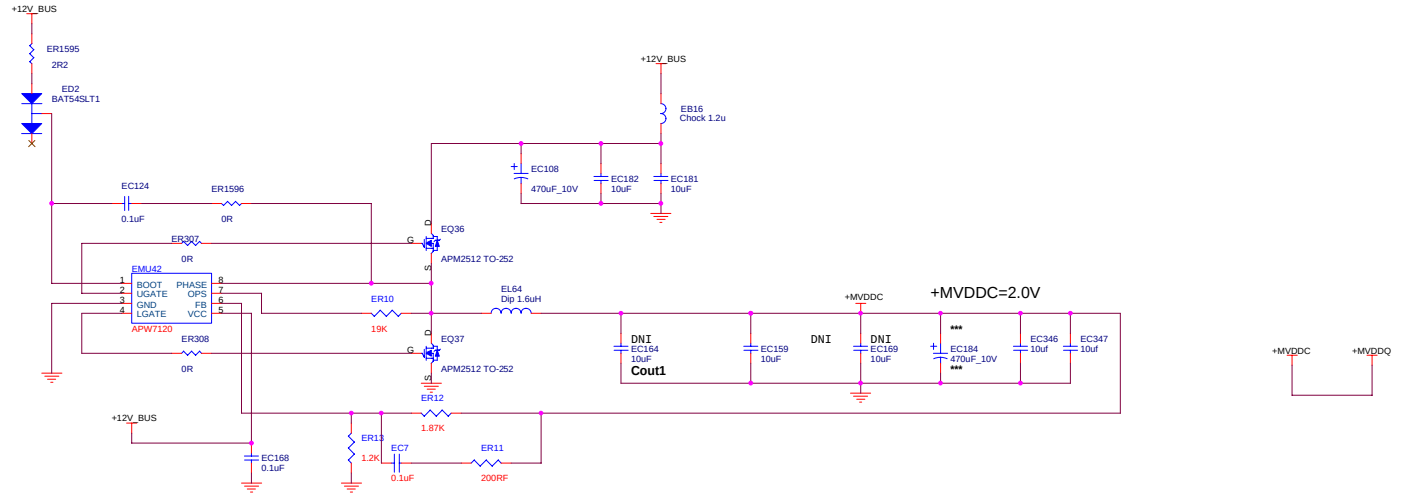
## FOR ALTERNATE #2

Change C157 for 10 uF and C121 for 1 uF
Replace C764 by 0 Ohm resistor
Replace R314 with a bead
Remove R954, R370, R305-R308, C159, R112, C160 and MU32

Install R374, R375, R371, C168 and U32

### Compensation circuit

Rc1 = 10K, Rc2 = 8.06K
R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF







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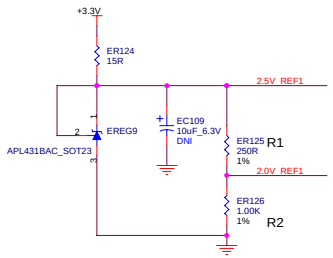


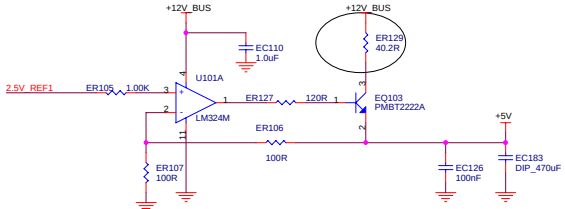


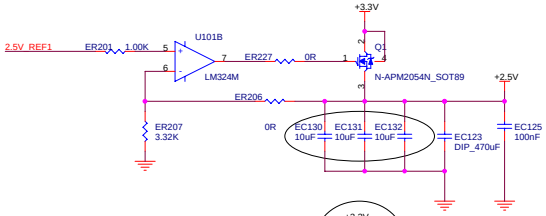


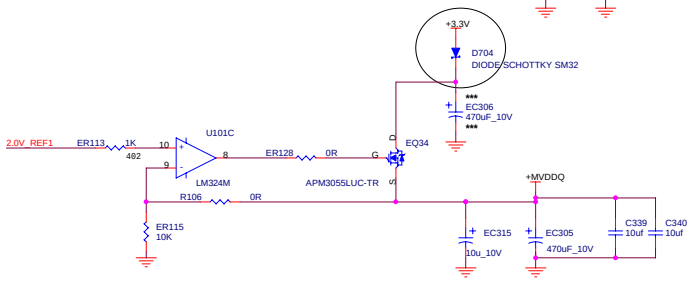


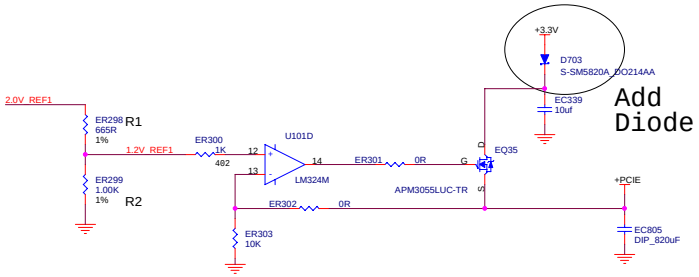



**Replace with 5050004800**
**120R, 300MA EIA(0402)**

| | | |
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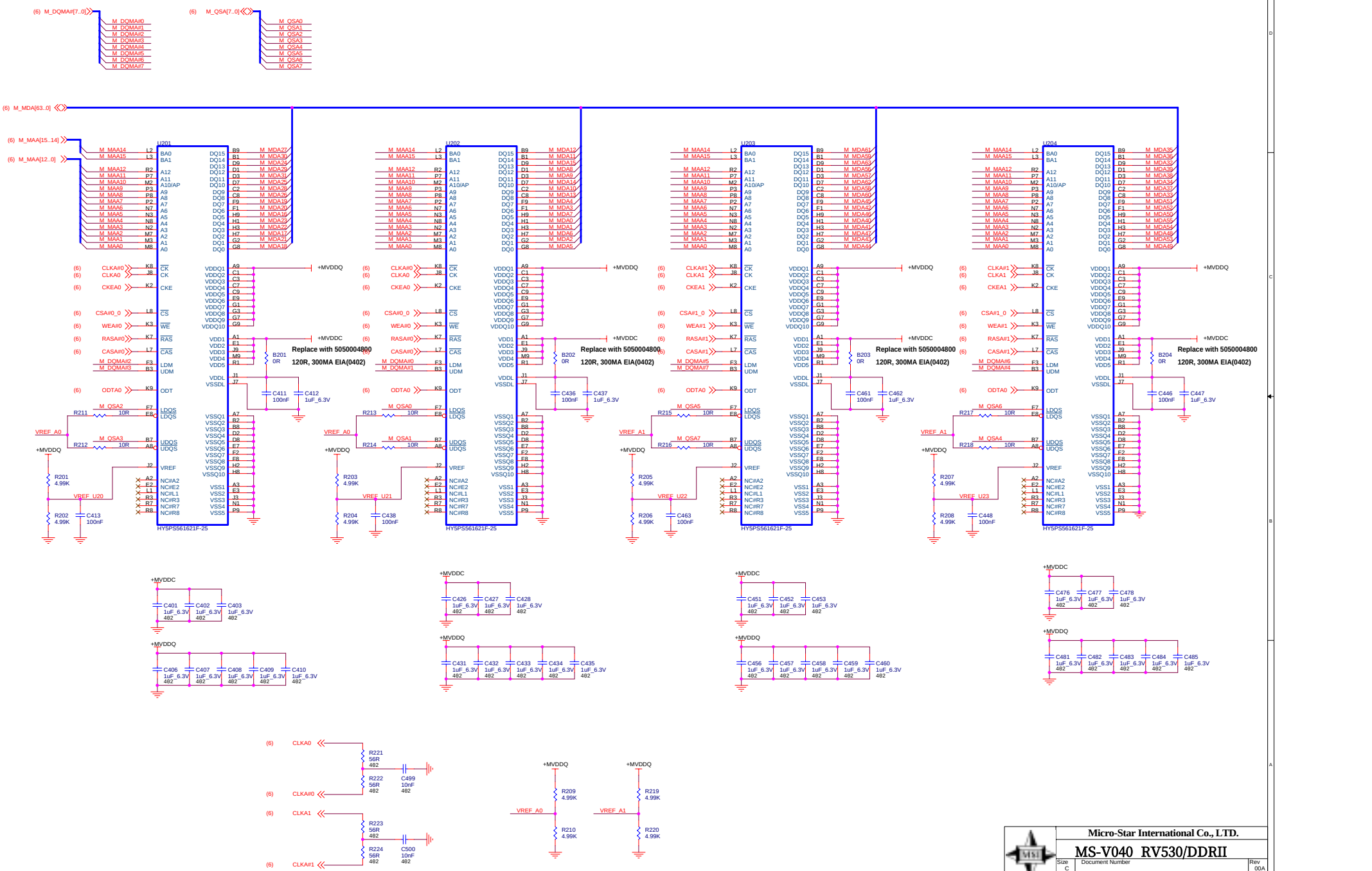
# CHANNEL A: RANK 0 128MB DDR2

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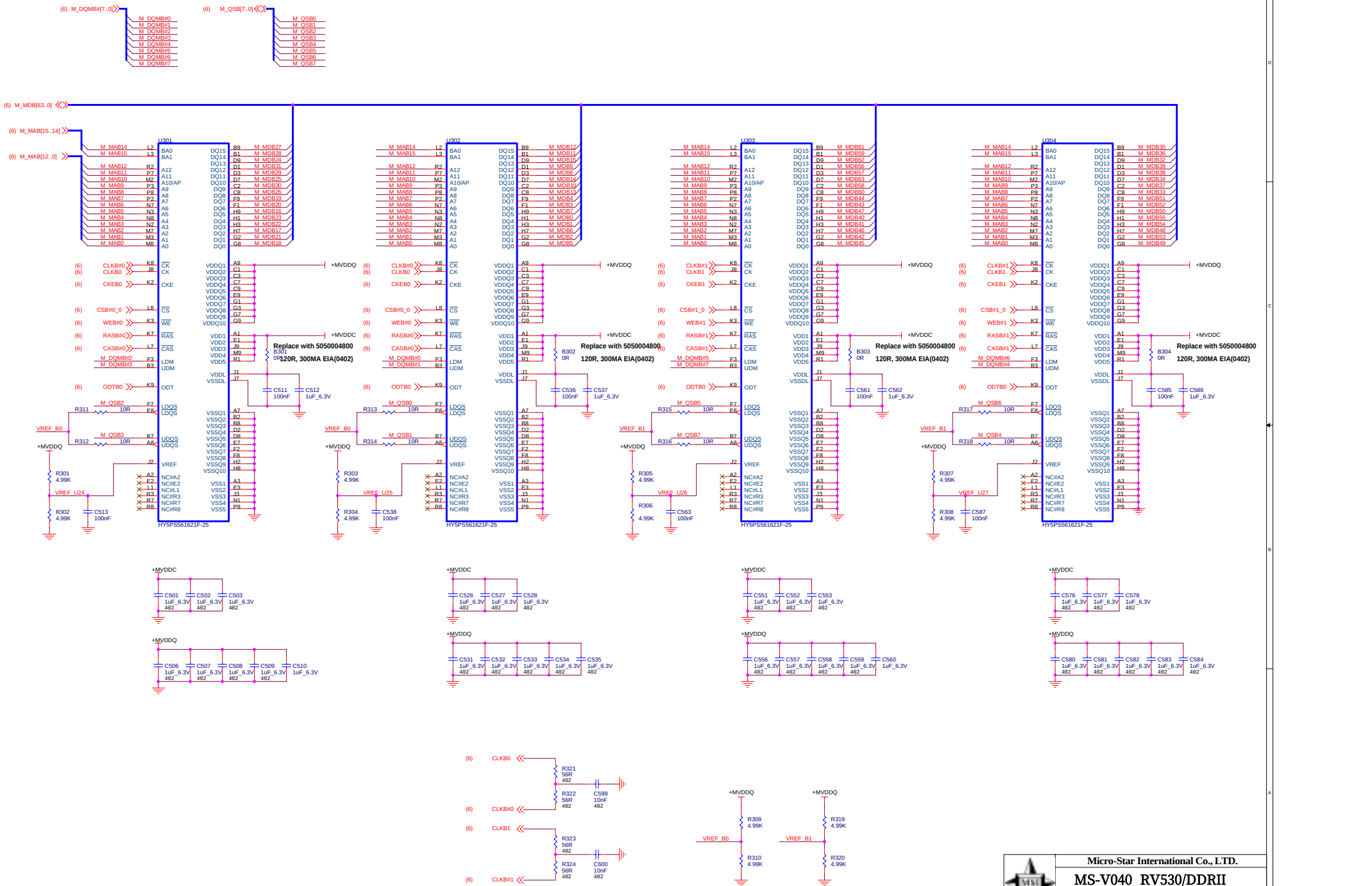
# CHANNEL B: RANK 0 128MB DDR2

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|---|---|---|---|
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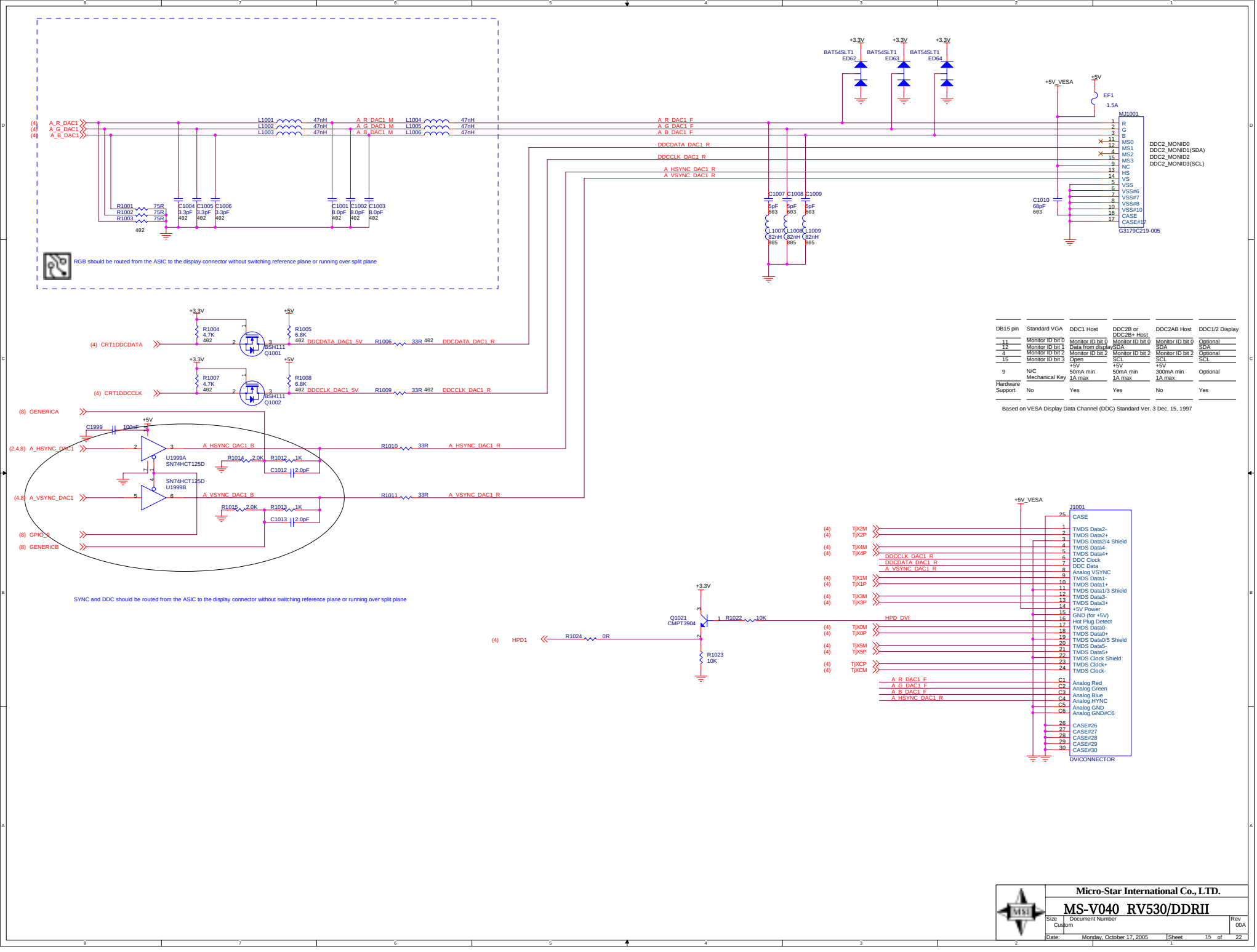


| DB15 pin | Standard VGA | DDC1 Host | DDC2B or DDC2B+ Host | DDC2AB Host | DDC1/2 Display |
|---|---|---|---|---|---|
| 11 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Optional |
| 12 | Monitor ID bit 1 | Data from display | SDA | SDA | SDA |
| 4 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Optional |
| 15 | Monitor ID bit 3 | Open | SCL | SCL | SCL |
| 9 | N/C Mechanical Key | +5V 50mA min 1A max | +5V 50mA min 1A max | +5V 300mA min 1A max | Optional |
| Hardware Support | No | Yes | Yes | No | Yes |

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

| | | | | |
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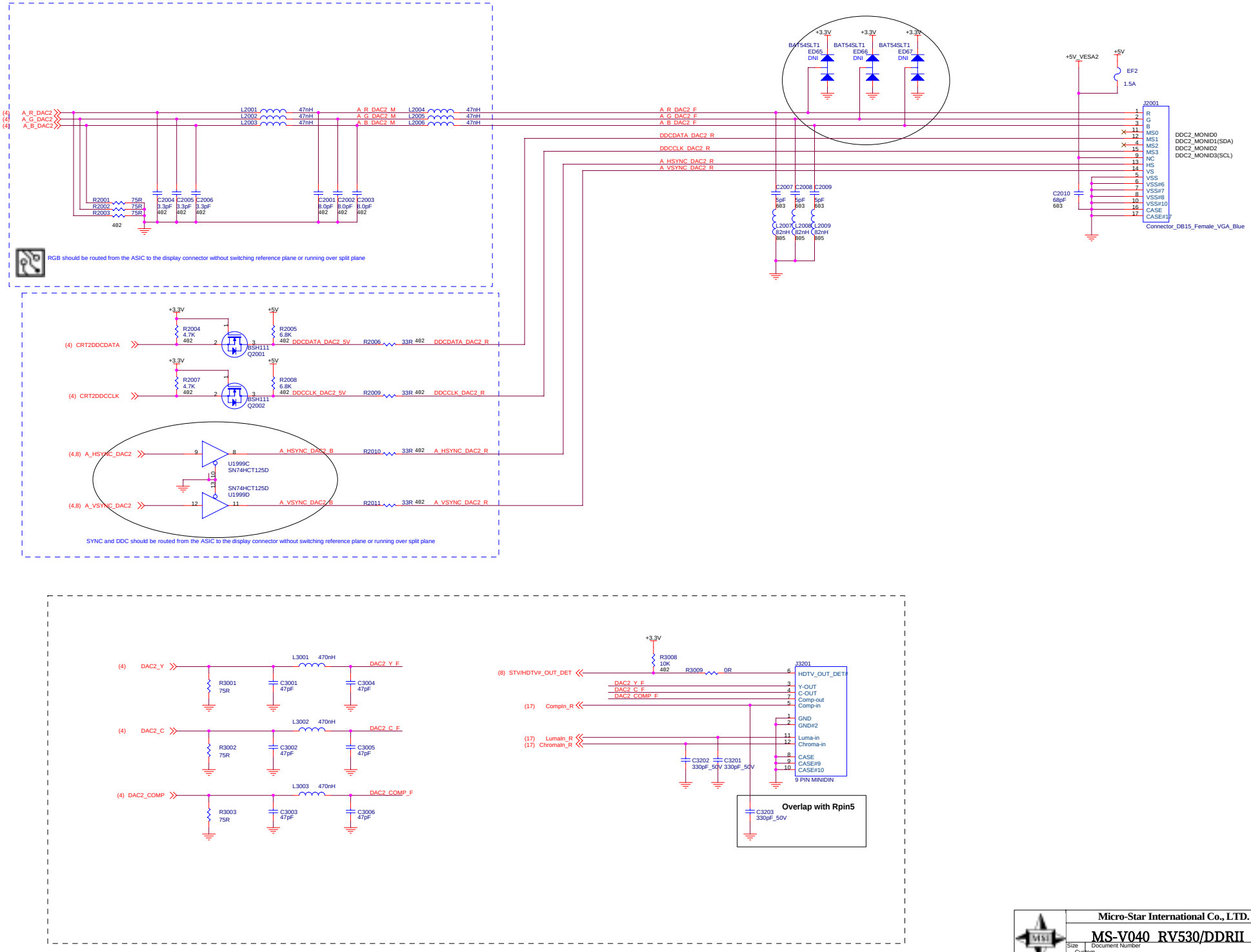


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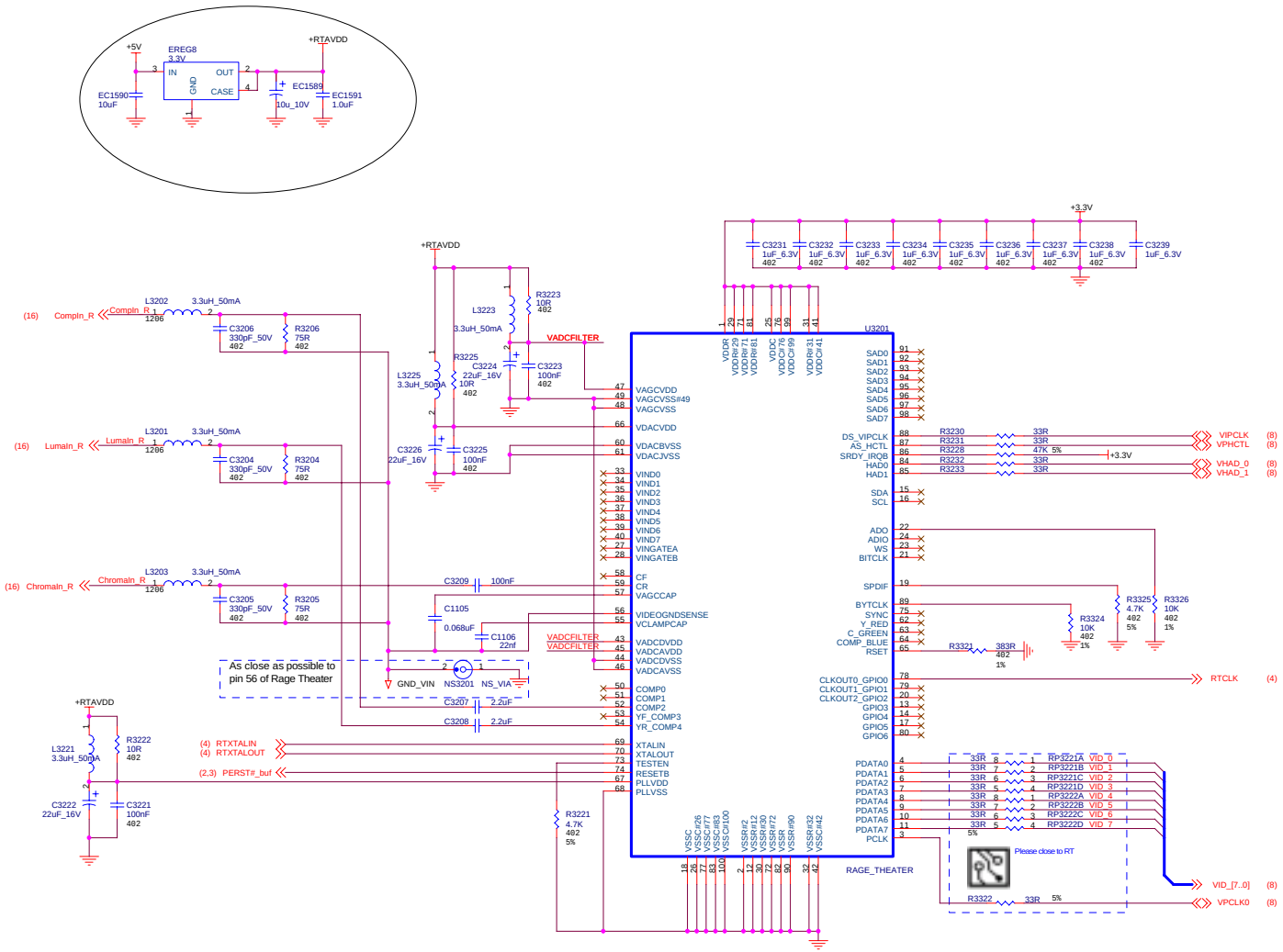


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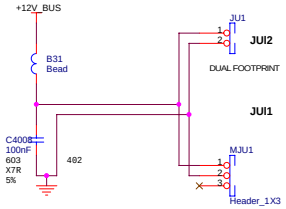


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DVI/VGA SCREWS

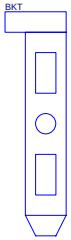
SCREW1
SCREW
JACKSCREW ASSY
7020000800

SCREW2
SCREW
JACKSCREW ASSY
7020000800

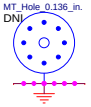
SCREW3
SCREW
JACKSCREW ASSY
7020000800

SCREW4
SCREW
JACKSCREW ASSY
7020000800

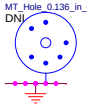
BKT



MT1
MT_Hole_0.136_in.
DNI



MT2
MT_Hole_0.136_in_6VIA
DNI



FM1
SW_FB

FM5
SW_FB

FM2
SW_FB

FM6
SW_FB

FM3
SW_FB

FM4
SW_FB

PCB

H2

LOW PROFILE HS

| | | |
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<variant Name>

| Title | Schematic No. | Date: |
|---|---|---|
| MS-V040 RV5xx DDR2 VGA 2xDVI VIVO FH | MS-V040-11 | **Monday, October 17, 2005** |

# REVISION HISTORY

Rev 1

| Sch Rev | PCB Rev | Date | REVISION DESCRIPTION |
|---|---|---|---|
| 0 | 10 | | |
| 1 | 11 | 05/10/04 | 1:Add Page12 3.3V to PCI-E PWR Diode: D703<br>2:Add Page12 +2.5V 10U Cap, EC130,EC131,EC132 |