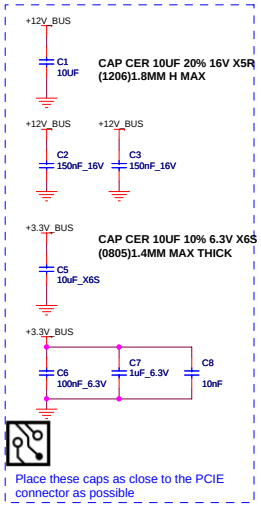
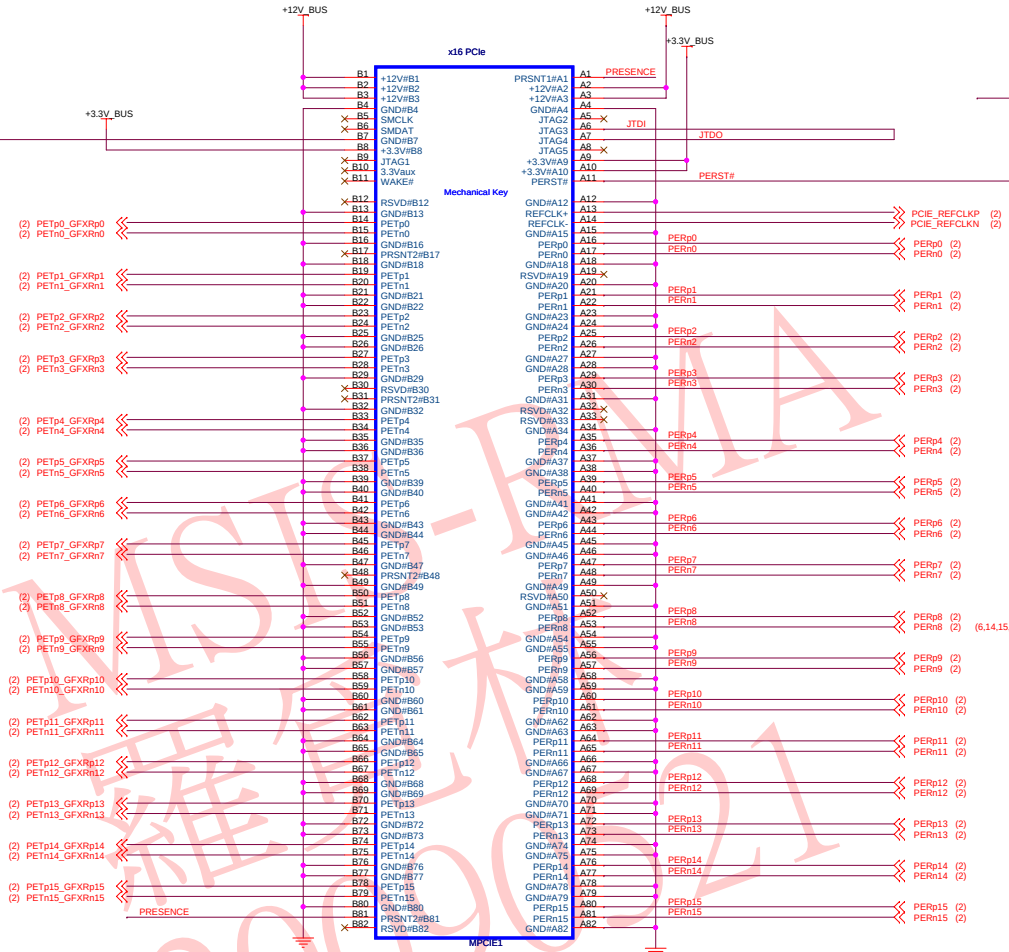
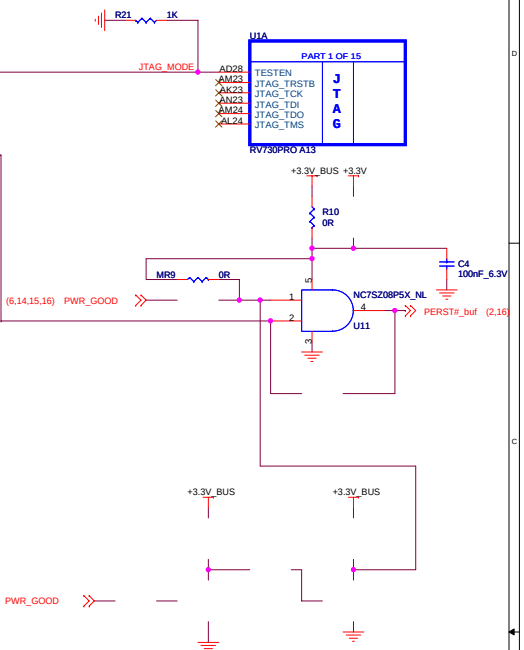
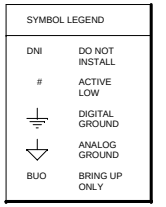
PCI-EXPRESS EDGE CONNECTOR









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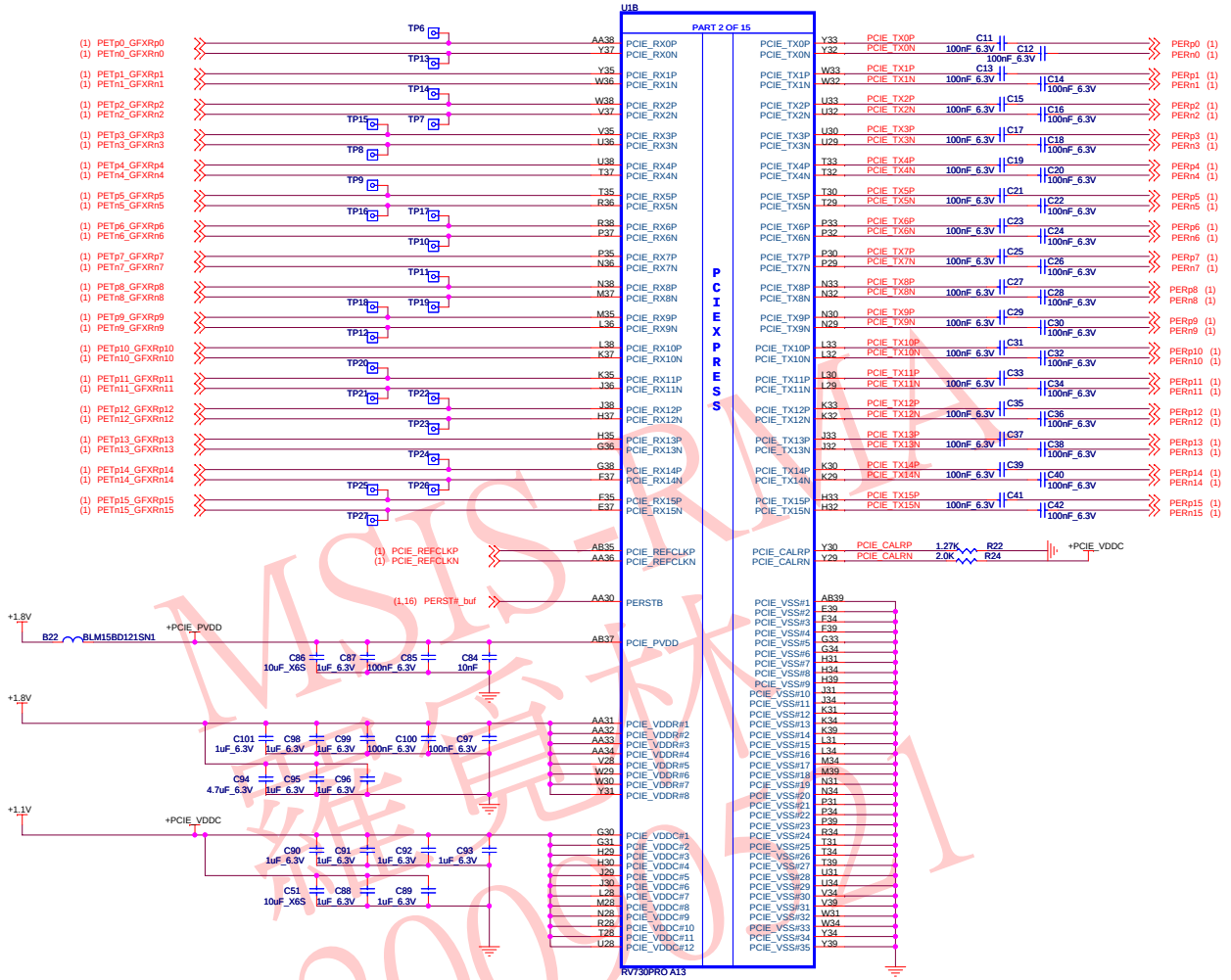
(2) RV730 PCIE Interface

NOTE: some of the PCIE testpoints will
be available trought via on traces.



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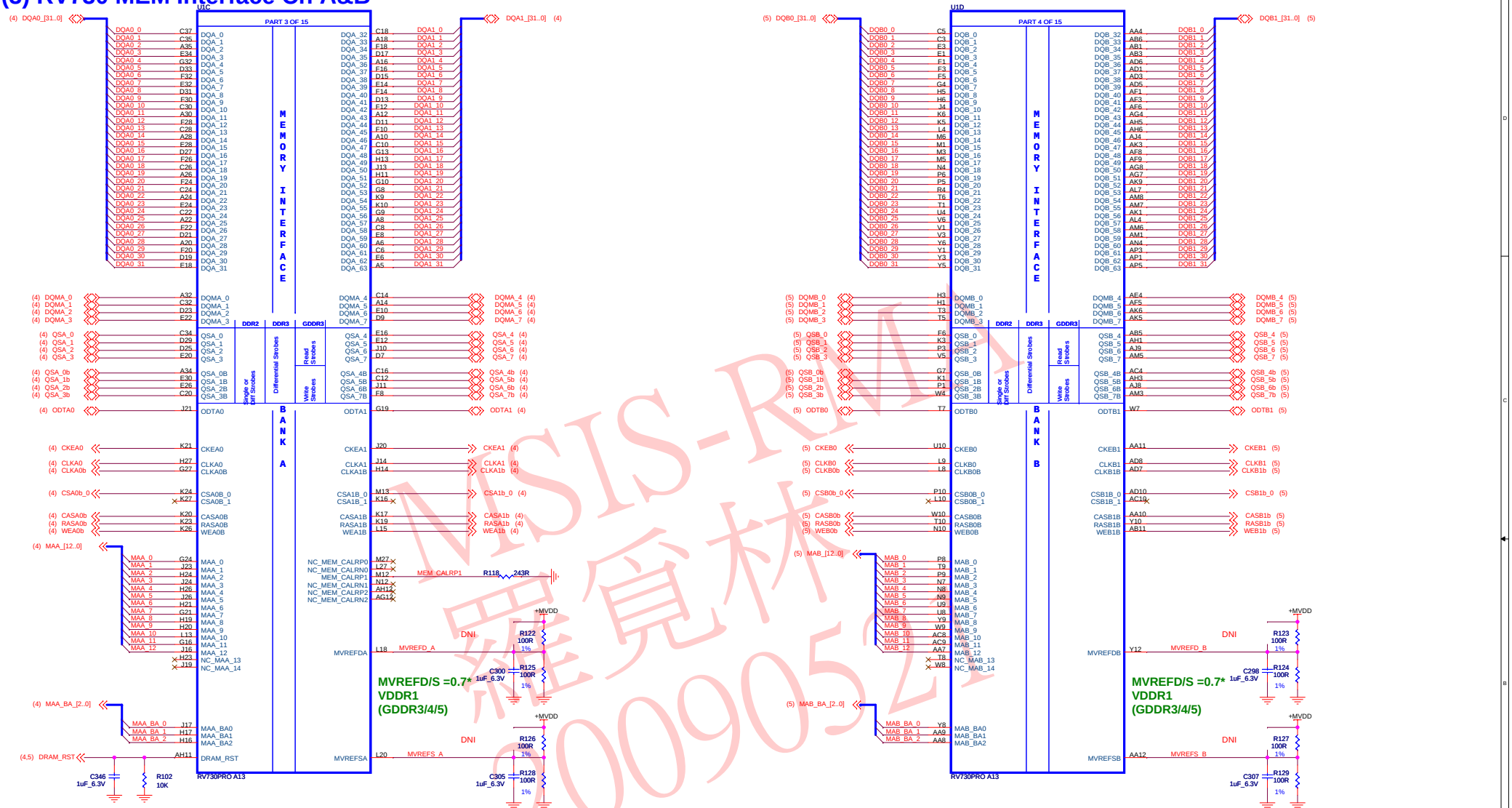
(3) RV730 MEM Interface Ch A&B



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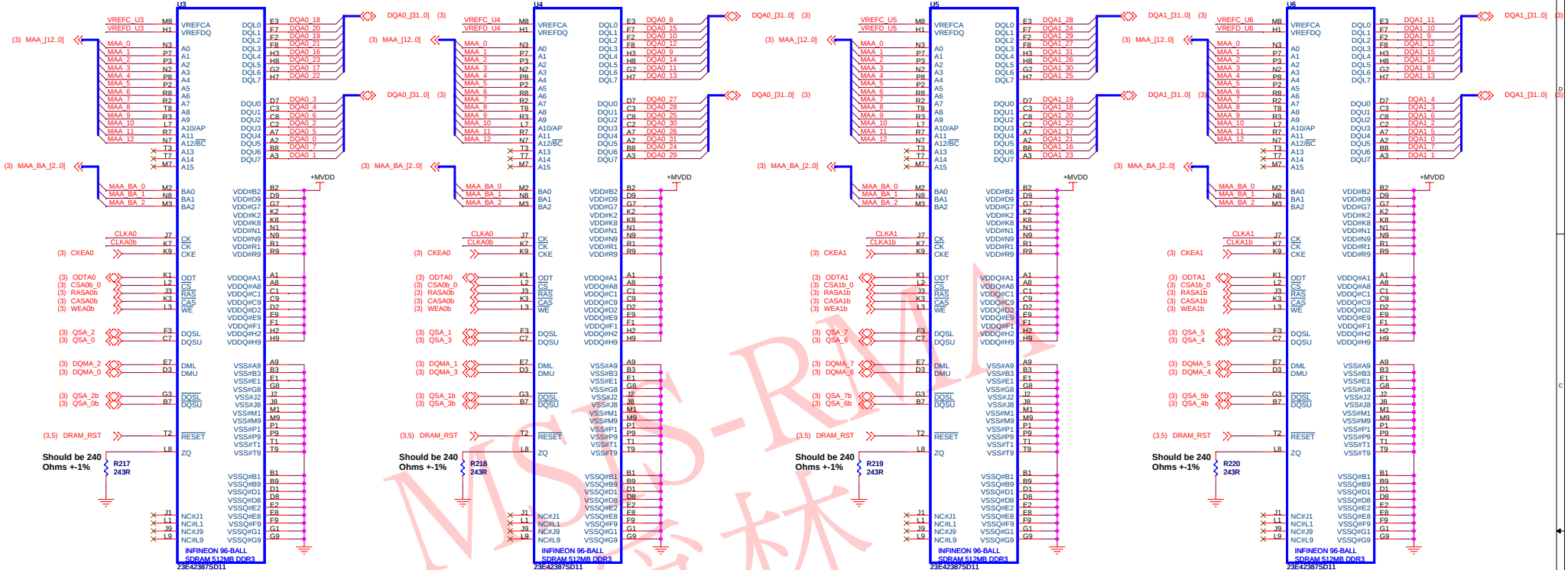
(4) DDR3 Memory Channel A



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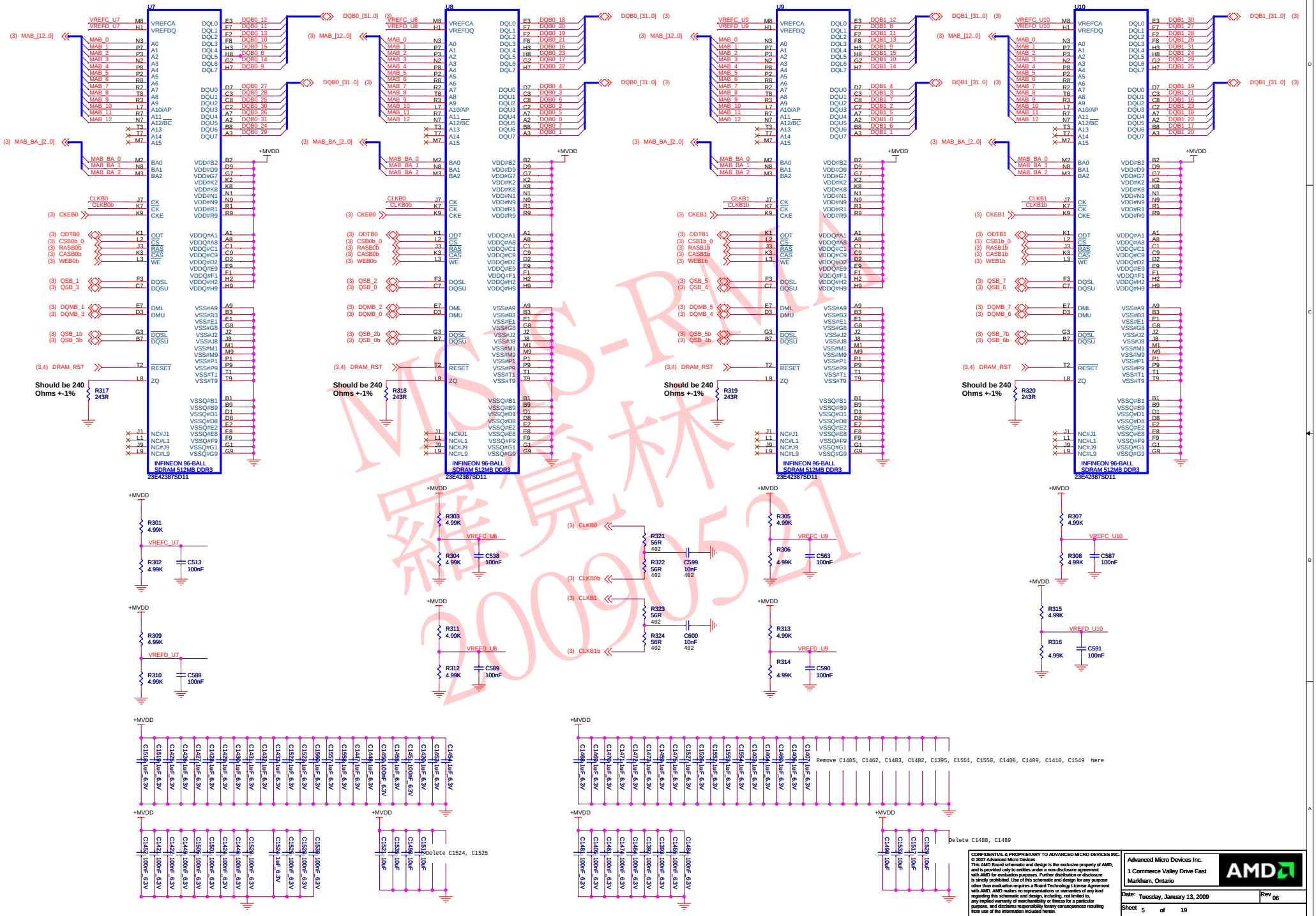
(5) DDR3 Memory Channel B



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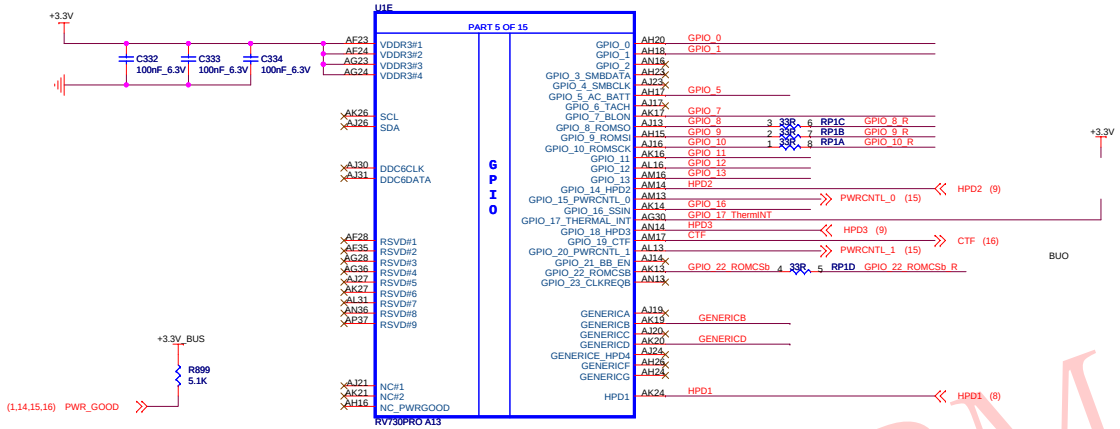
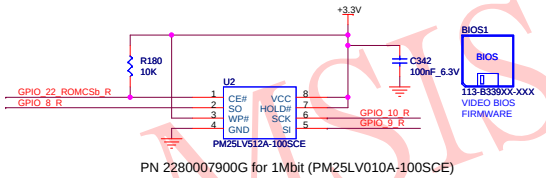
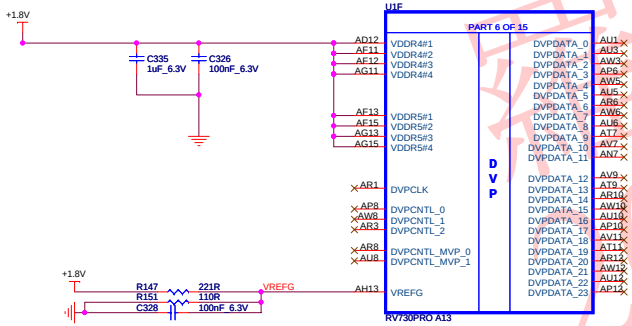
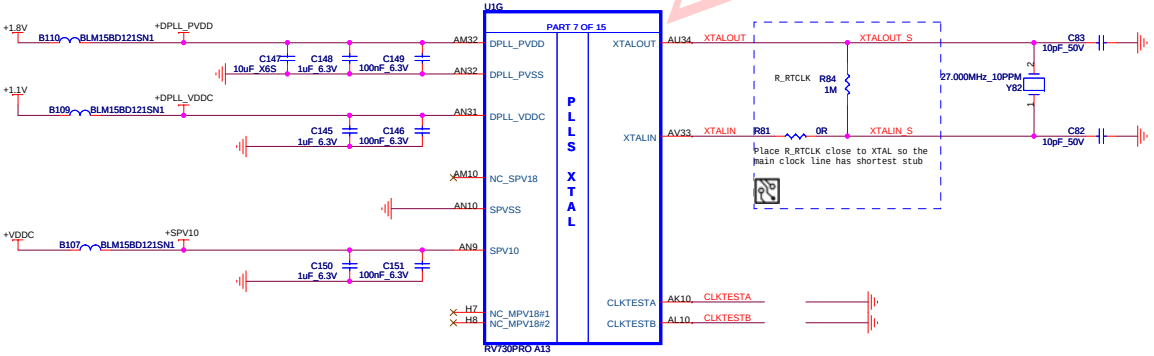
(06) RV730 GPIOs Strap CF XTAL





PN 2280007900G for 1Mbit (PM25LV010A-100SCE)





PIN BASED STRAPS

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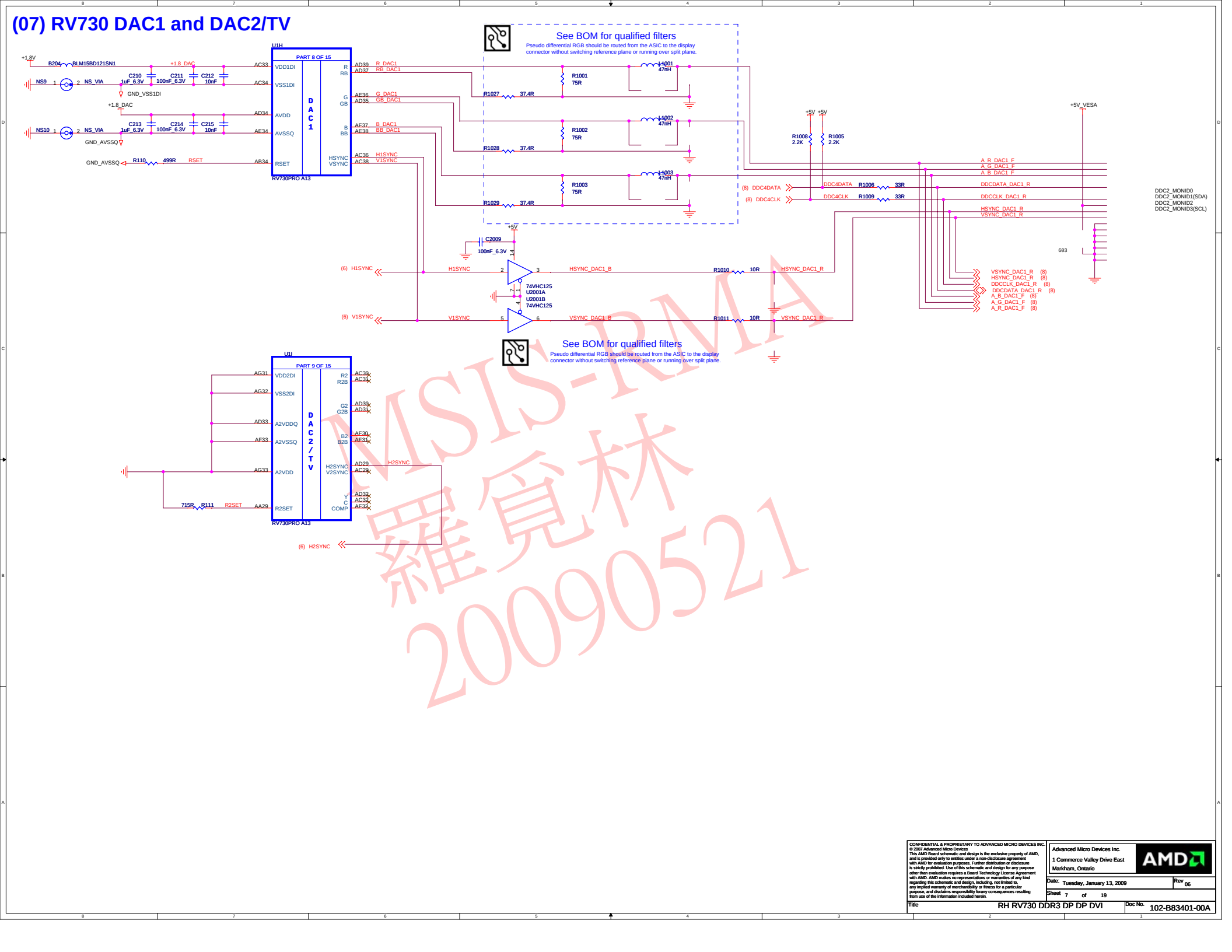
(07) RV730 DAC1 and DAC2/TV



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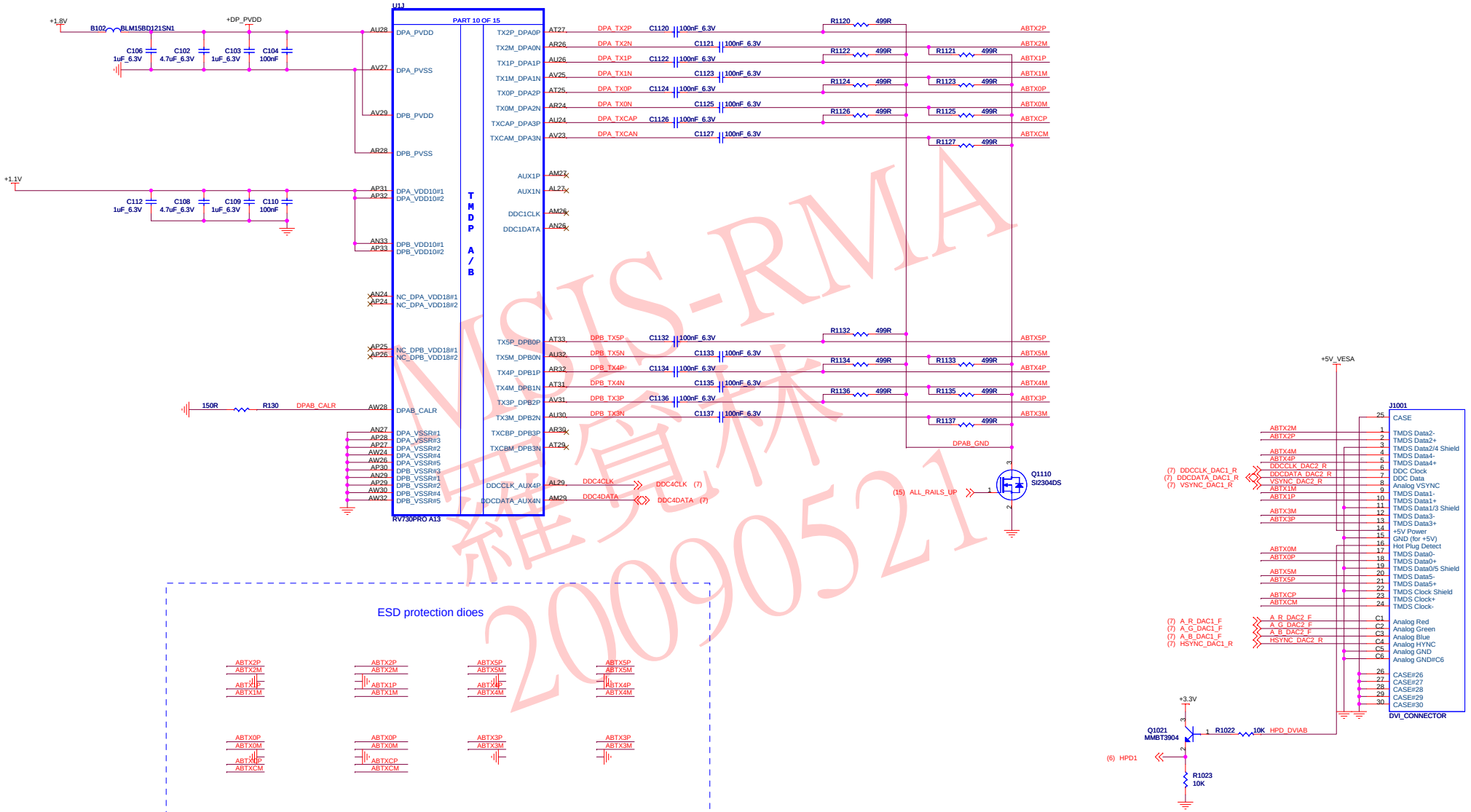
(08) RV730 TMDS A&B



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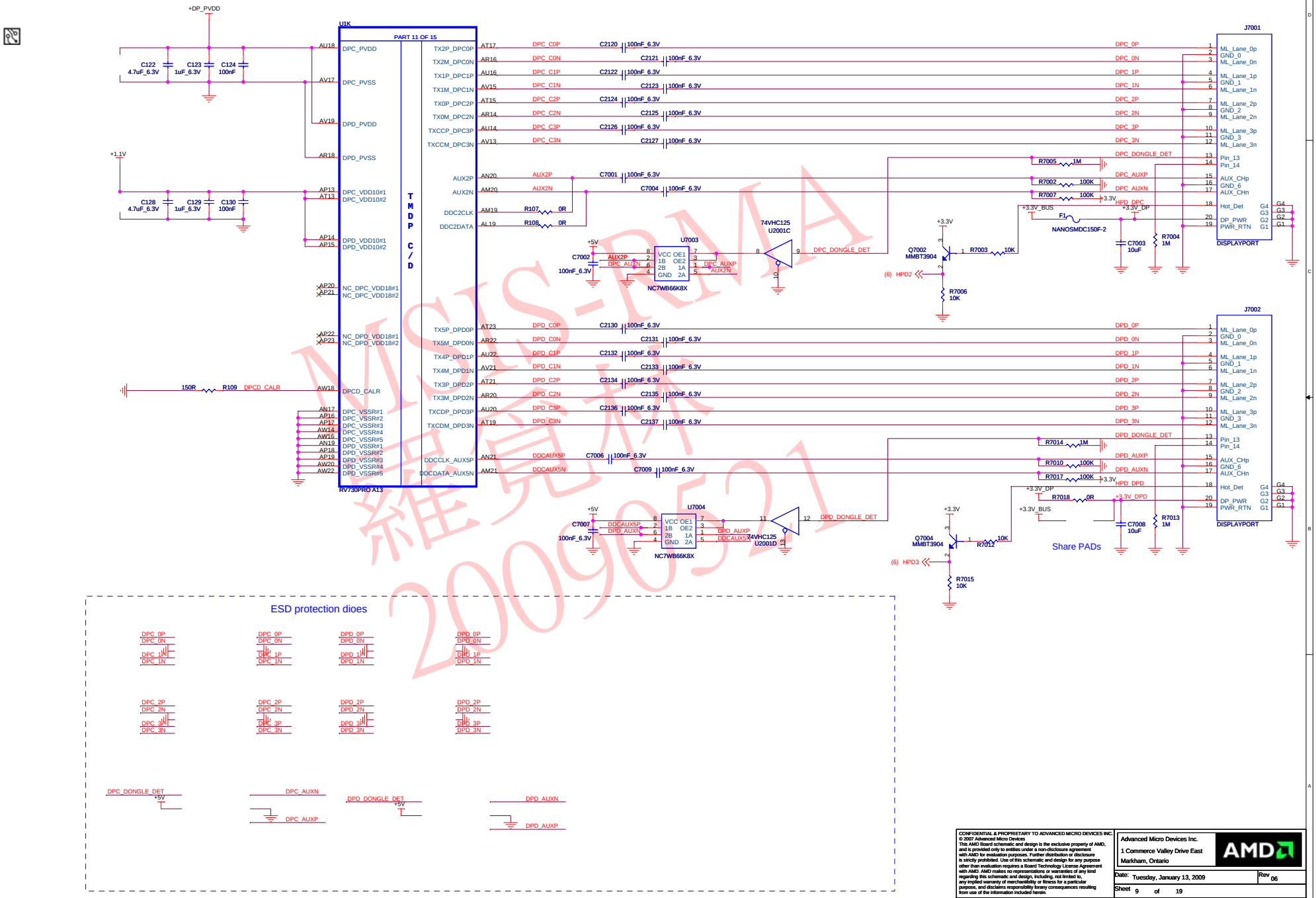
(09) RV730 Display Port C&D



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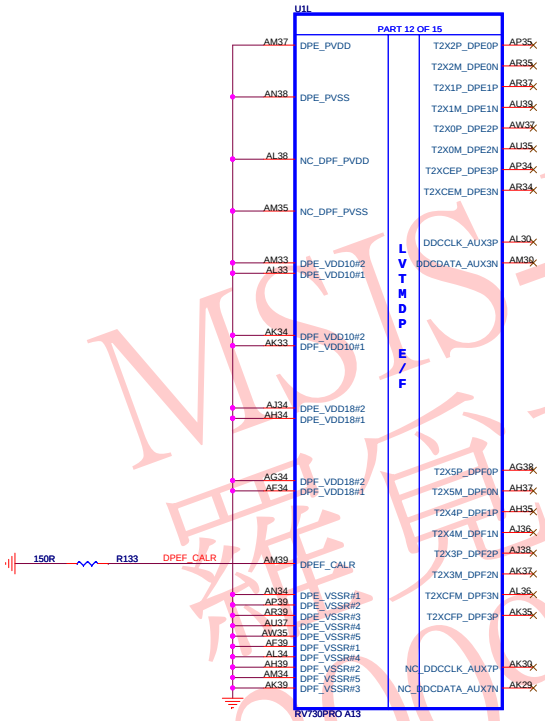
(10) No Connect E&F



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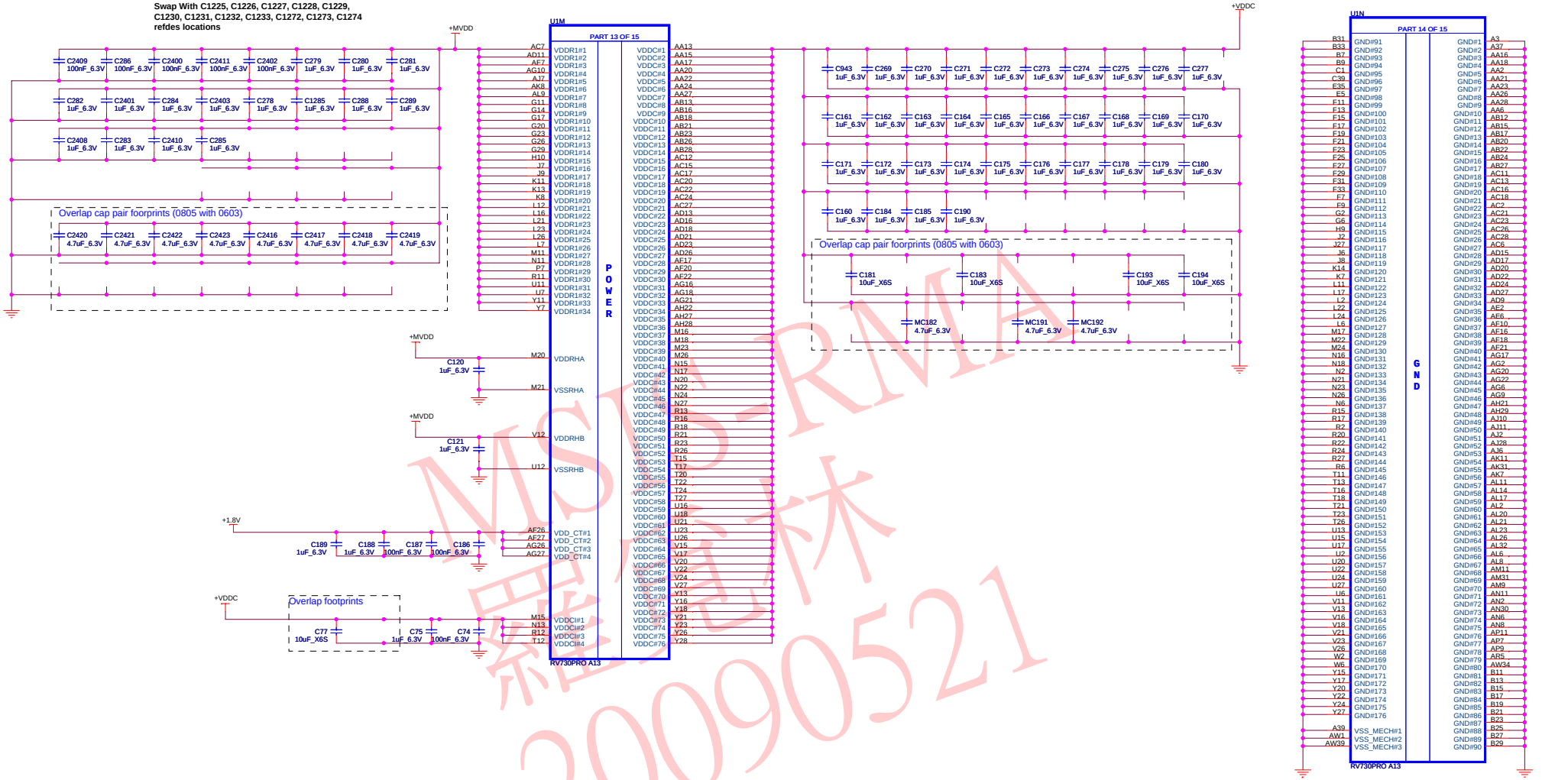
(11) RV730 Power & GND



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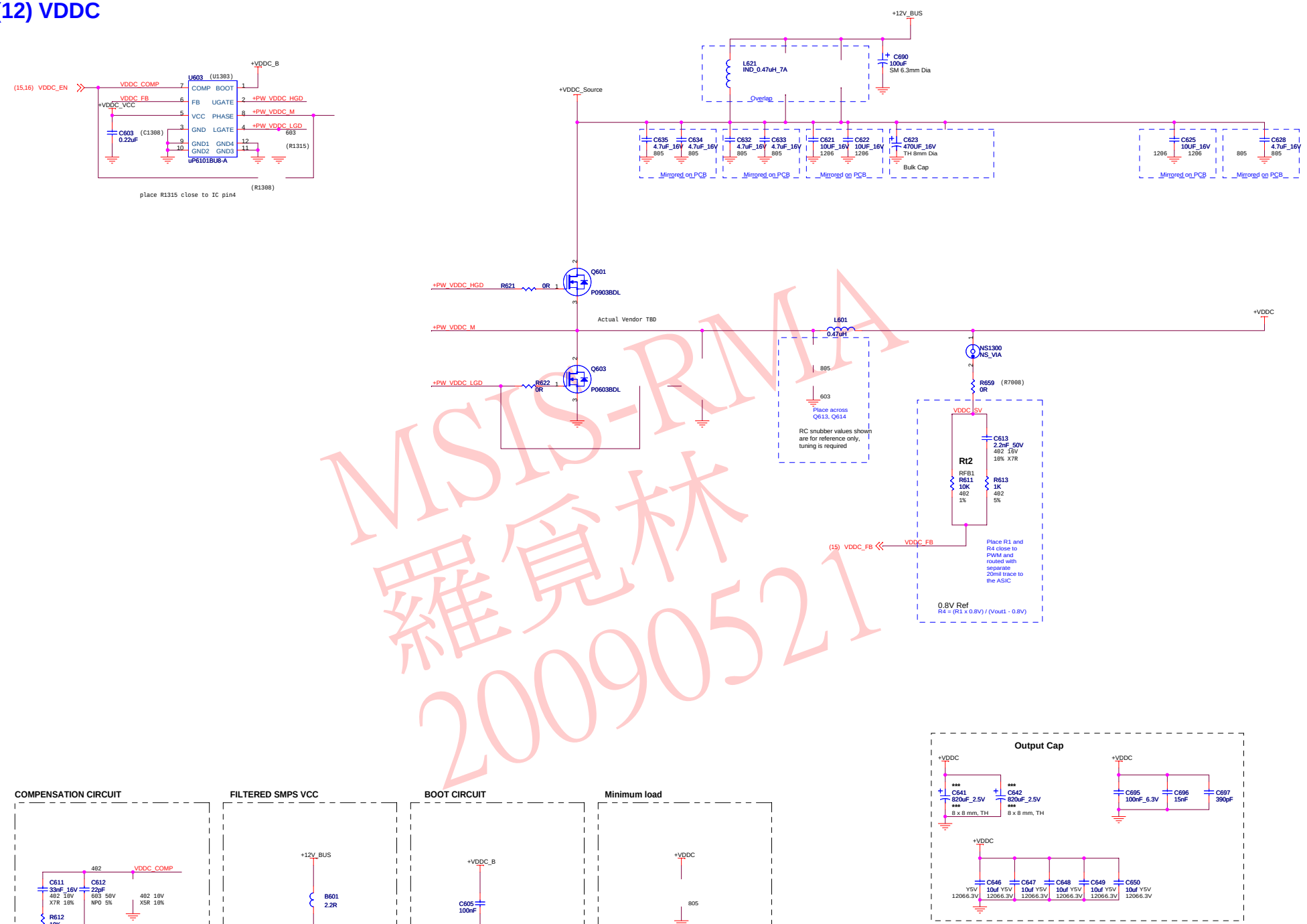
(12) VDDC



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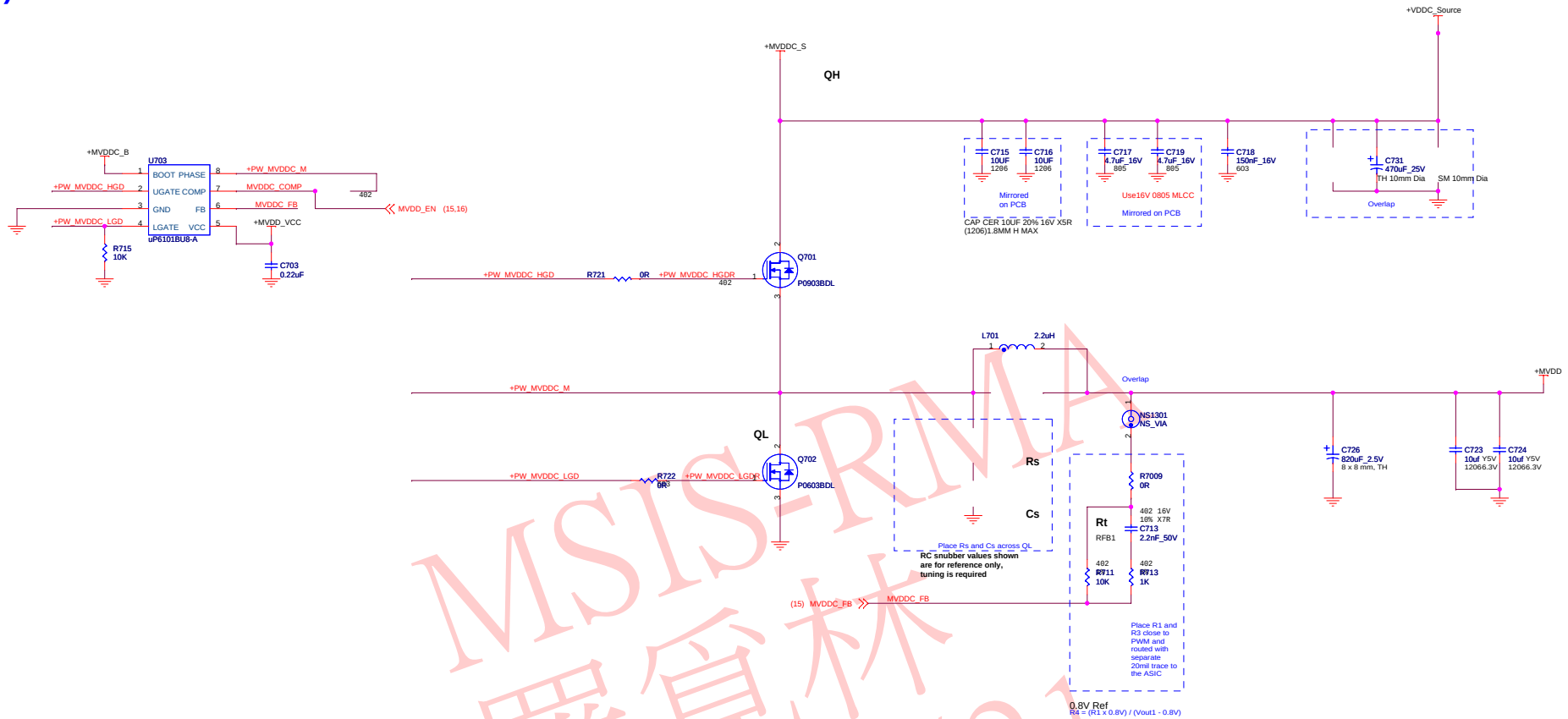
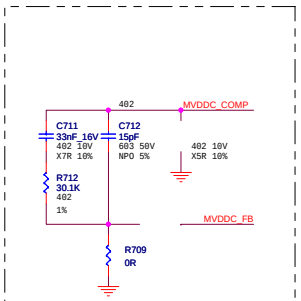
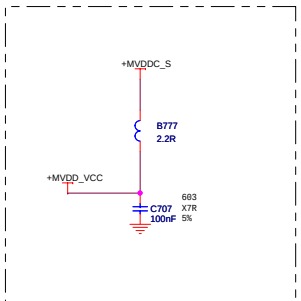
(13) MVDD



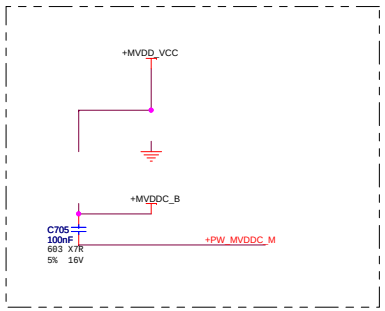
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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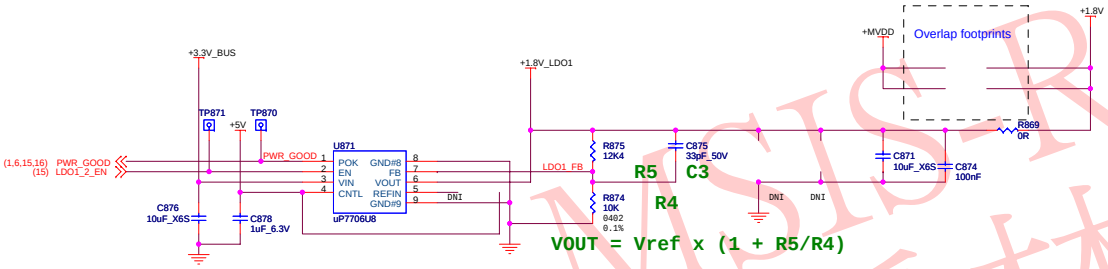
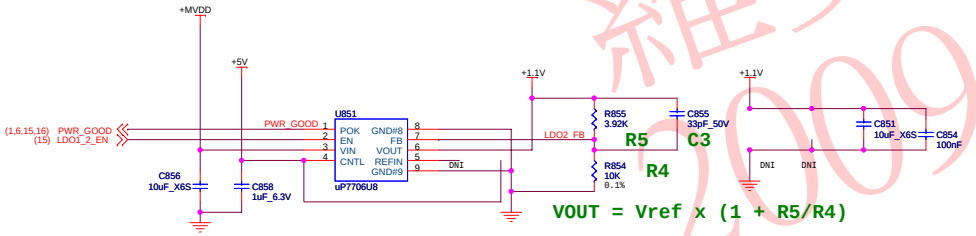
(14) Linear Regulators

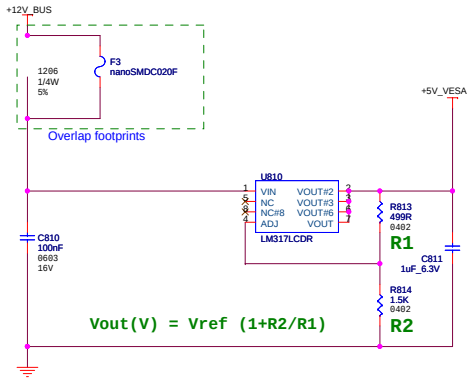
Regulators for +5V, +5V_VESA and +5V_VESA2

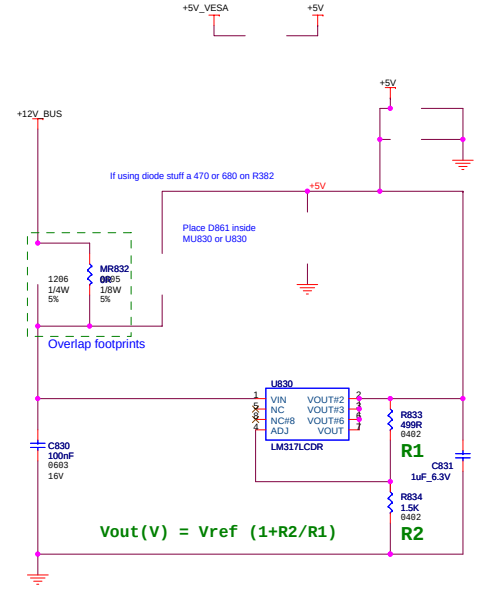
LDO #1: Vin = 3.0V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 1.0A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #2: Vin = +1.5V to 2.0VMAX Vout = +1.1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling







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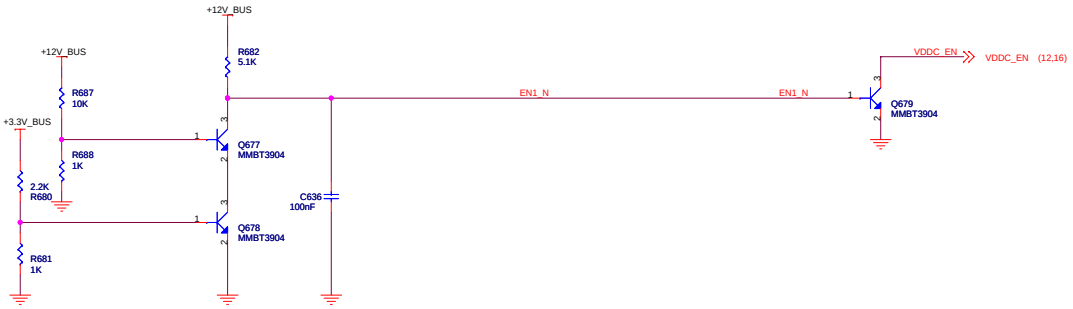
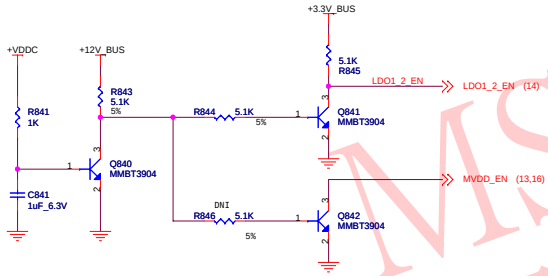
(15) Power Management

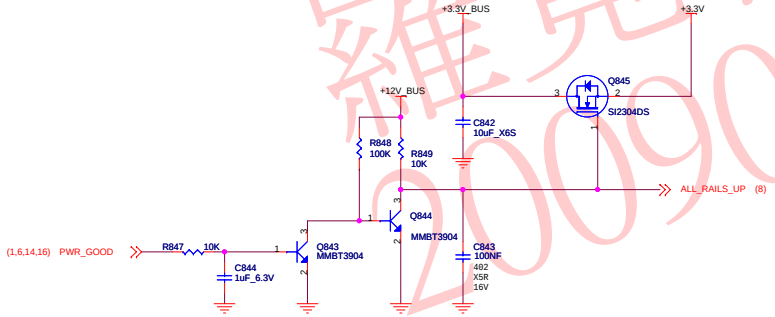
Power up Sequencing



VDDC Enable Circuit



LDOs and MVDD Enable Circuit



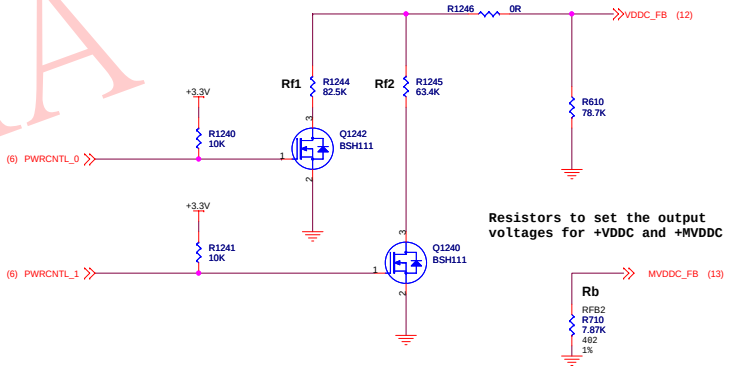
3.3V Enable Circuit

Power Play

VDDC Voltage Settings Using GPIOs (for VDDC1 Dual Phase)

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1=42.2K Rf2=20.5K	Rf1= Rf2=	Rf1= Rf2=
0	0	0.90V		
0	1	1.00V		
1	0	1.15V		
1	1	1.25V		

Vout = Vref * (1+Rt/Rb)
VDDC2 (Single Phase): Vref = 0.8V, Rt = 10K
MVDDC (Single Phase): Vref = 0.8V, Rt = 10K



Resistors to set the output voltages for +VDDC and +MVDDC

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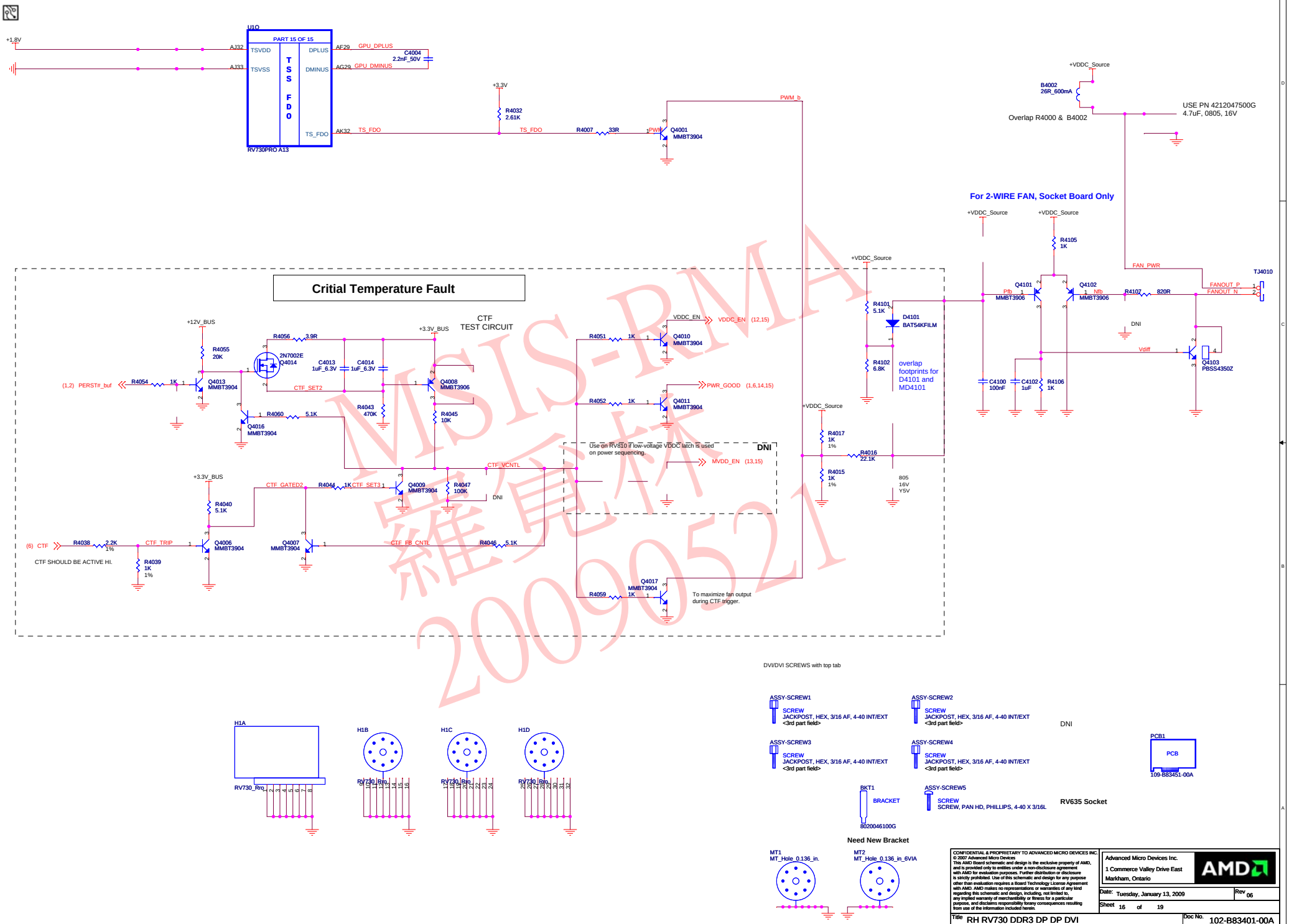
(16) Mechanical and Thermal Management



DVI/DVI SCREWS with top tab

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

DNI

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
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ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
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PCB1
PCB
109-B83451-00A

BKT1
BRACKET
8020046100G

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

RV635 Socket

Need New Bracket

MT1
MT_Hole_0.136_in.

MT2
MT_Hole_0.136_in_6VIA

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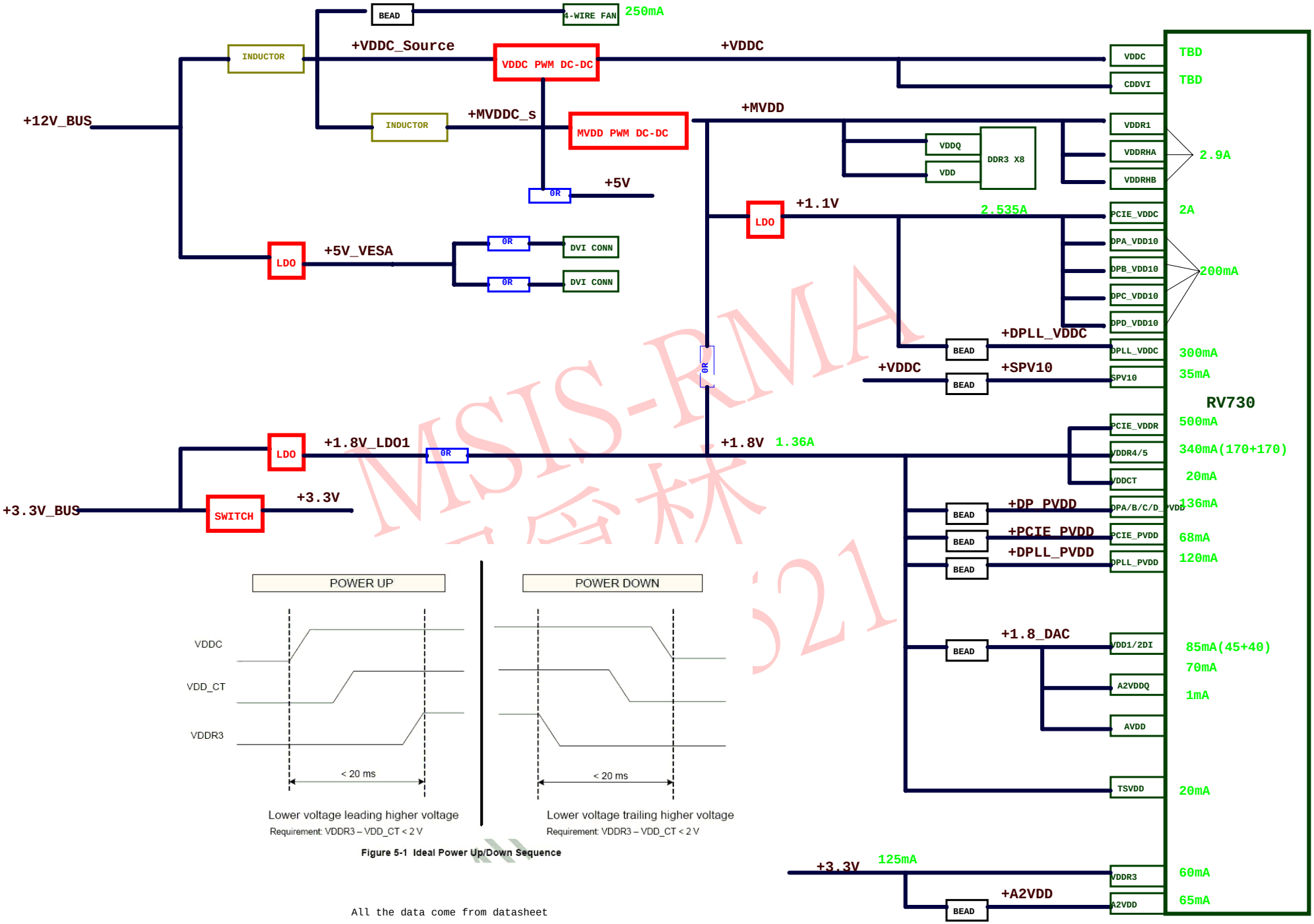

Figure 5-1 Ideal Power Up/Down Sequence

All the data come from datasheet

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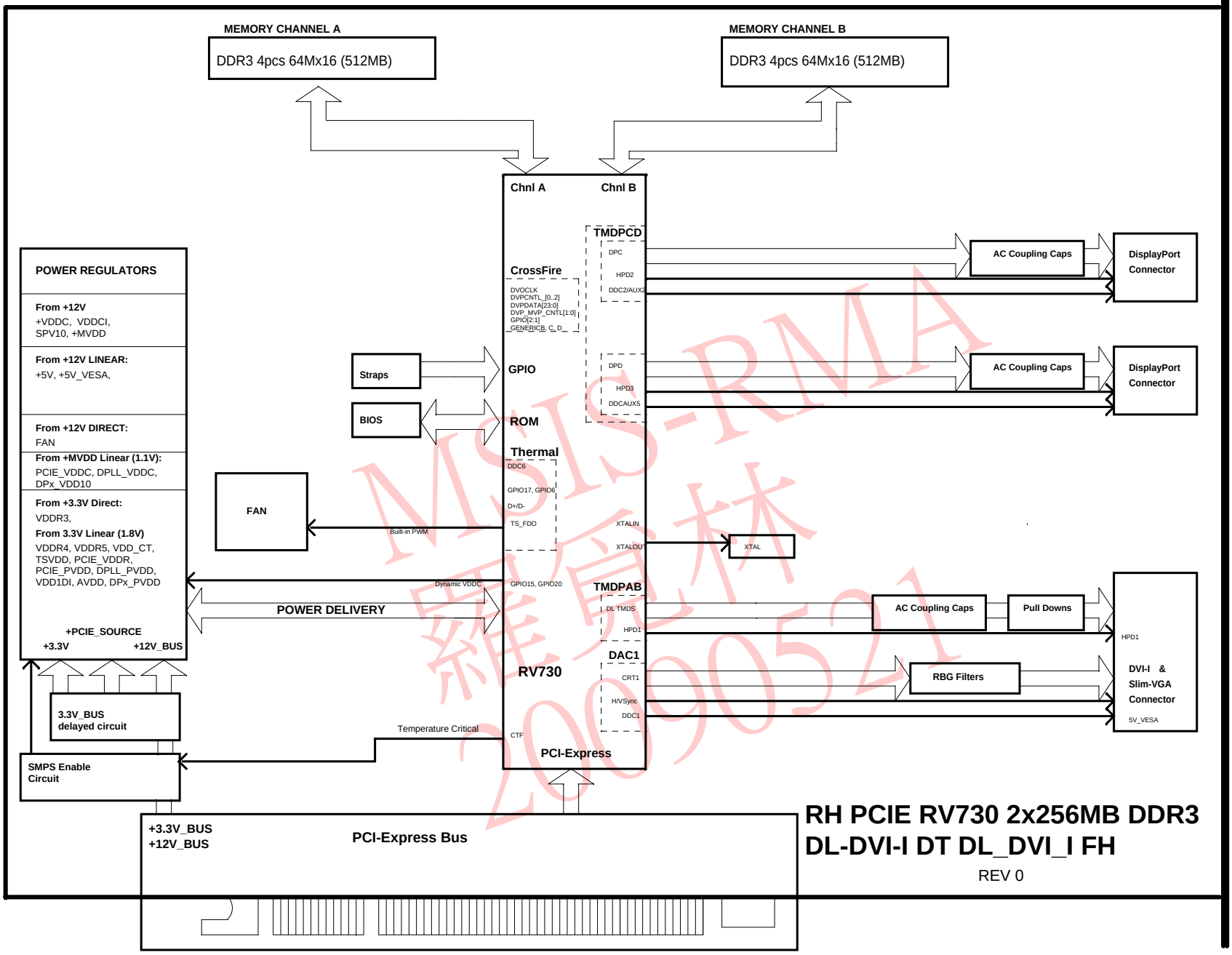

RH PCIE RV730 2x256MB DDR3
DL-DVI-I DT DL_DVI_I FH

REV 0

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RH-RV730 DDR3 DP DP DVI	Size: C	Rev
Sheet	of	Tuesday, January 13, 2009	
Doc No.	102-B83401-00A	18	19

Title	Schematic No.	Date:
RH RV730 DDR3 DP DP DVI	102-B83401-00A	Tuesday, January 13, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 06

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	08/11/11	Initial design for RV730 DDR3