

P727-A01: G96, GB1-128, GDDR3, DL-DVI, DL-DVI/VGA, SD/HDTV

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REV HISTORY

- 2/18 PAGE 2 add SPDIF_IN_M from PCIE's connector PIN_BA2
- PAGE 15 remove DP function
- PAGE 16 remove SLI function
- PAGE 17 add SCART (the same as V096-3.0)
- PAGE 18 add SPDIF_IN_M
- PAGE 19 remove GPIO_11_SLI_SYNC0 / GPIO12_SWAPRDY / GPIO15_DP_HP / GPIO18_DP_MODE / GPIO19_DP_CEC / GPIO22_SWAPRDY_A
- add GPIO2_TV_SCART / GPIO13_TV_SCART_SEL / GPIO14_TV_SCART_SEL / GPIO20_TV_LOAD_TEST / GPIO16_SEL_HDTV_SDTV
- 2/20 PAGE 16 MIOB VDD from 2V5 change to 3V3_F
- 2/21 PAGE 20 remove J5 (HDA function), remove 2V5
- PAGE 19 remove I2CD_SDA and I2CD_SCL (for DP)
- remove GPIO2/GPIO13/GPIO14
- PAGE 17 3V3 chnage to 3V3_F
- remove SCART_TV_SEL function
- remove TV_CVBS_SCART_F
- PAGE 21 remove Q15, C870, R737 (for DP_hotplug_detect_E)
- PAGE 22 remove 2V5 function
- 2/22 PAGE 22 IFPEF_RSET PULL LOW
- PAGE 18 ADD U601,U602,U603,U604 for EMI
- ADD MEC10, MEC11 for external FAN holder
- ADD FM7, FM8

REV	VARIANT	NPVN	ASSEMBLY
B	BASE	600-10727-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	600-10727-0000-100	G96-A02, 650/800MHz 256MB 16MX32 GDDR3, DVI DVI HDTV-Out
2	SKU001	600-10727-0001-100	G96-300, 550/800MHz 256MB 16MX32 GDDR3, DVI DVI HDTV-Out
3	SKU002	600-10727-0002-100	G96-300, 550/800MHz 256MB 16MX32 GDDR3, DVI DVI
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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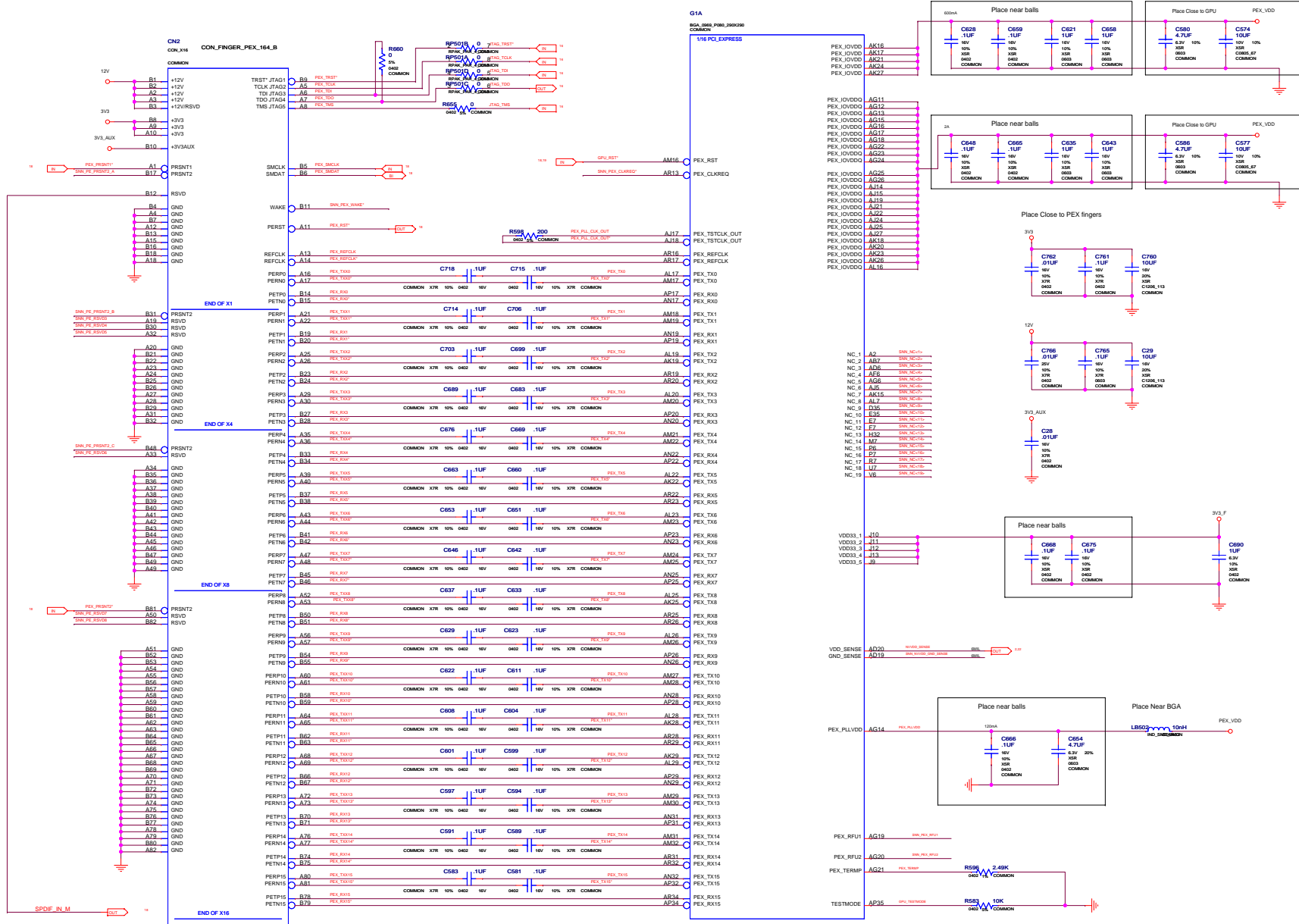
NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



NV_PN	600-10727-base-sch A
ID	
NAME	
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DATE	31 OCT 2007

16X PEX INTERFACE



	NET	DIFFER	NU_IMPEDANCE	NU_CRITICAL
10	PEX-007A	PEX-007A	0.0007	+
11	PEX-007B	PEX-007B	0.0007	+
12	PEX-007C	PEX-007C	0.0007	+
13	PEX-007D	PEX-007D	0.0007	+
14	PEX-007E	PEX-007E	0.0007	+
15	PEX-007F	PEX-007F	0.0007	+
16	PEX-007G	PEX-007G	0.0007	+
17	PEX-007H	PEX-007H	0.0007	+
18	PEX-007I	PEX-007I	0.0007	+
19	PEX-007J	PEX-007J	0.0007	+
20	PEX-007K	PEX-007K	0.0007	+
21	PEX-007L	PEX-007L	0.0007	+
22	PEX-007M	PEX-007M	0.0007	+
23	PEX-007N	PEX-007N	0.0007	+
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25	PEX-007P	PEX-007P	0.0007	+
26	PEX-007Q	PEX-007Q	0.0007	+
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43	PEX-008H	PEX-008H	0.0007	+
44	PEX-008I	PEX-008I	0.0007	+
45	PEX-008J	PEX-008J	0.0007	+
46	PEX-008K	PEX-008K	0.0007	+
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55	PEX-008T	PEX-008T	0.0007	+
56	PEX-008U	PEX-008U	0.0007	+
57	PEX-008V	PEX-008V	0.0007	+
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64	PEX-009C	PEX-009C	0.0007	+
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67	PEX-009F	PEX-009F	0.0007	+
68	PEX-009G	PEX-009G	0.0007	+
69	PEX-009H	PEX-009H	0.0007	+
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256	FEK 100	FEK 100	FEK247	+
257	FEK 095	FEK 095	FEK248	+
258	FEK 096	FEK 096	FEK249	+
259	FEK 097	FEK 097	FEK250	+
260	FEK 098	FEK 098	FEK251	+
261	FEK 099	FEK 099	FEK252	+
262	FEK 100	FEK 100	FEK253	+
263	FEK 095	FEK 095	FEK254	+
264	FEK 096	FEK 096	FEK255	+
265	FEK 097	FEK 097	FEK256	+
266	FEK 098	FEK 0		

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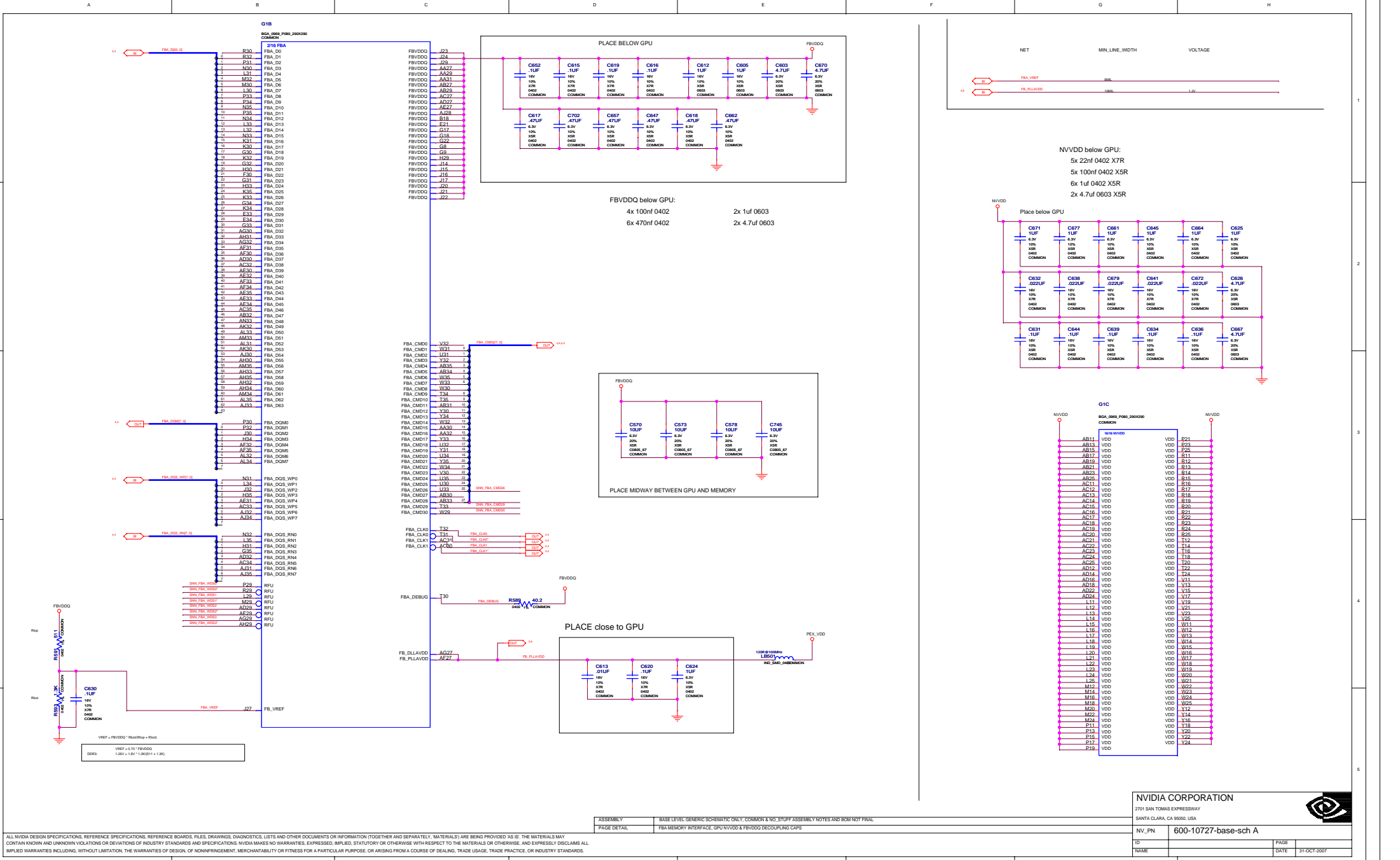
NV_PN	600-10727-base-sch A
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NAME		DATE	31-OCT-2007



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS



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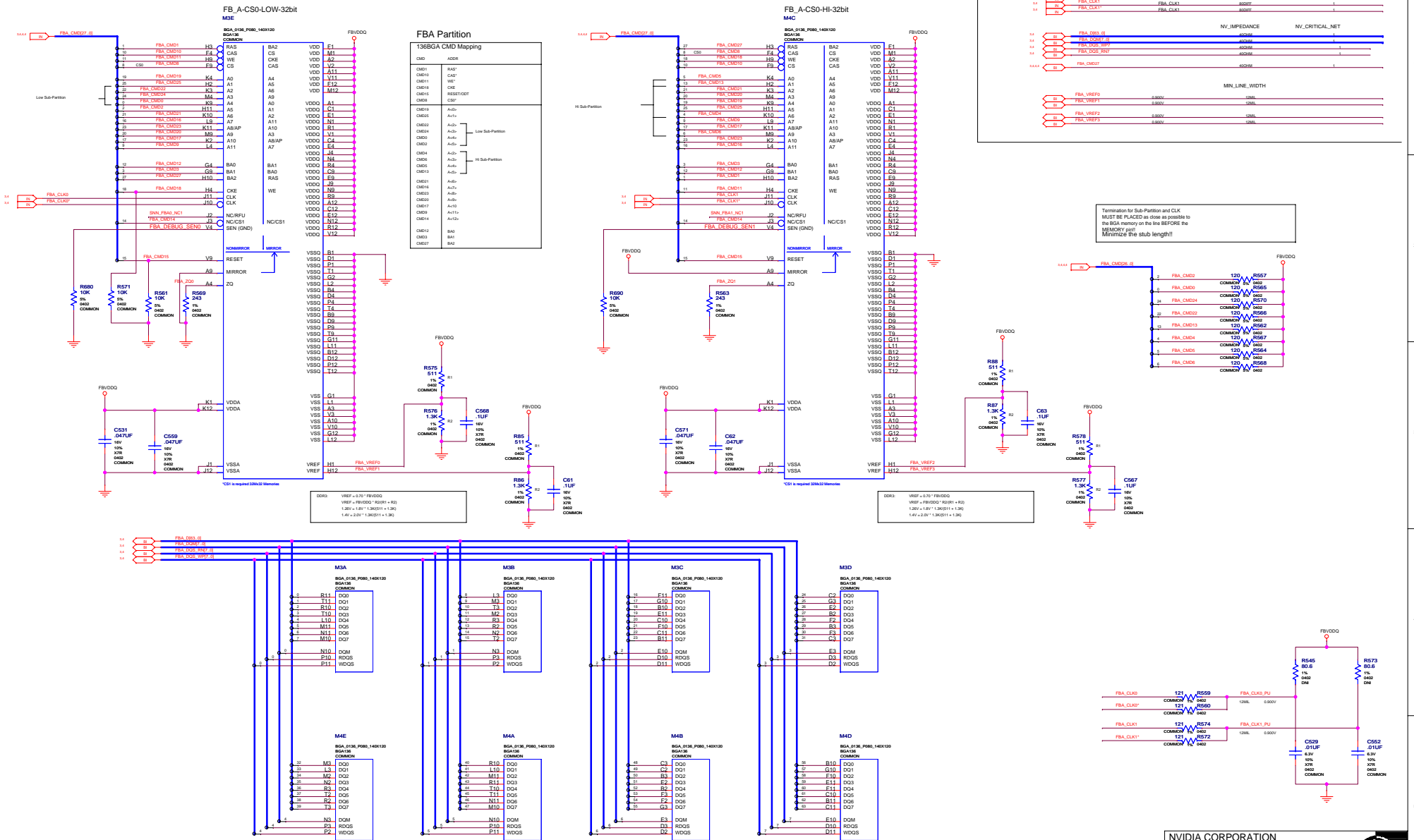
ASSEMBLY	BASE LEVEL GENERIC BOM/MATERIALS ONLY. COMMON & VIO. 31/07/07. ASSEMBLY NOTES AND BOM NOT FINAL.
PAGE: DETAIL	FBA MEMORY INTERFACE, GPU NVDD & FBVDD DECOUPLING CAPS

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ID	PAGE
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FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3



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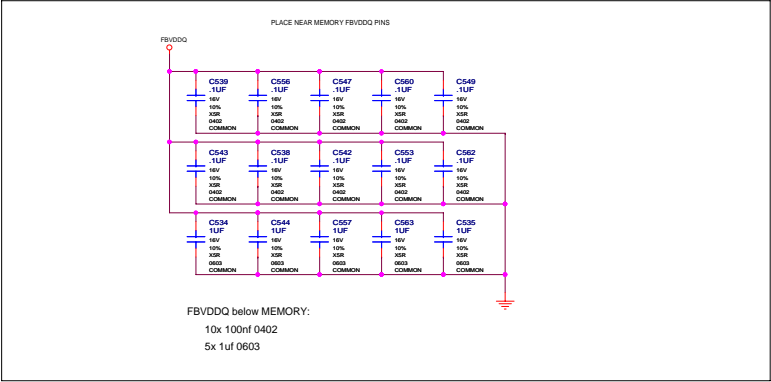
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16/32Mx32 GDOR3 MEMORIES, FBA COMMAND BUS P/U'S, FBA CLK TERMS

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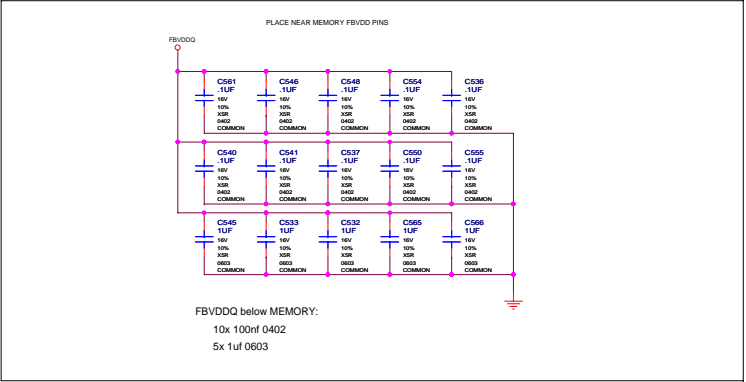


FRAME BUFFER: PARTITION A DECOUPLING

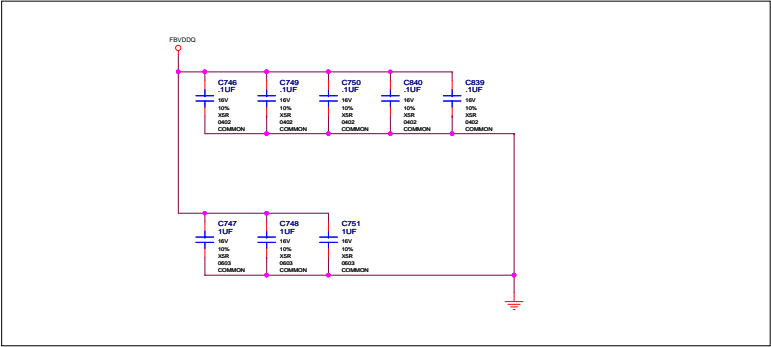
Decoupling for FBA 0..31



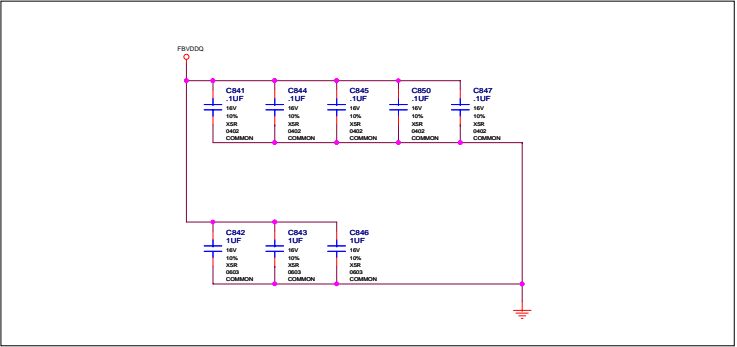
Decoupling for FBA 32..63



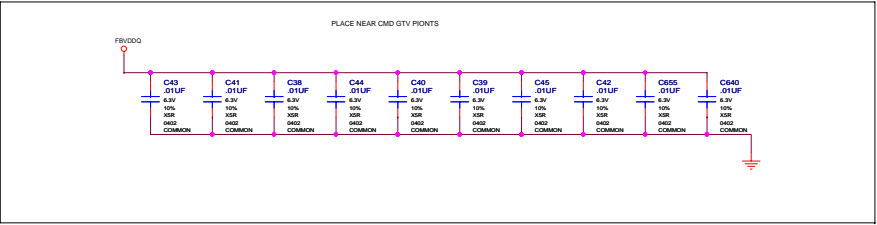
Decoupling for FBA A1 0..31



Decoupling for FBA A1 0..31



Return path coupling GND/FBVDDQ for FBA

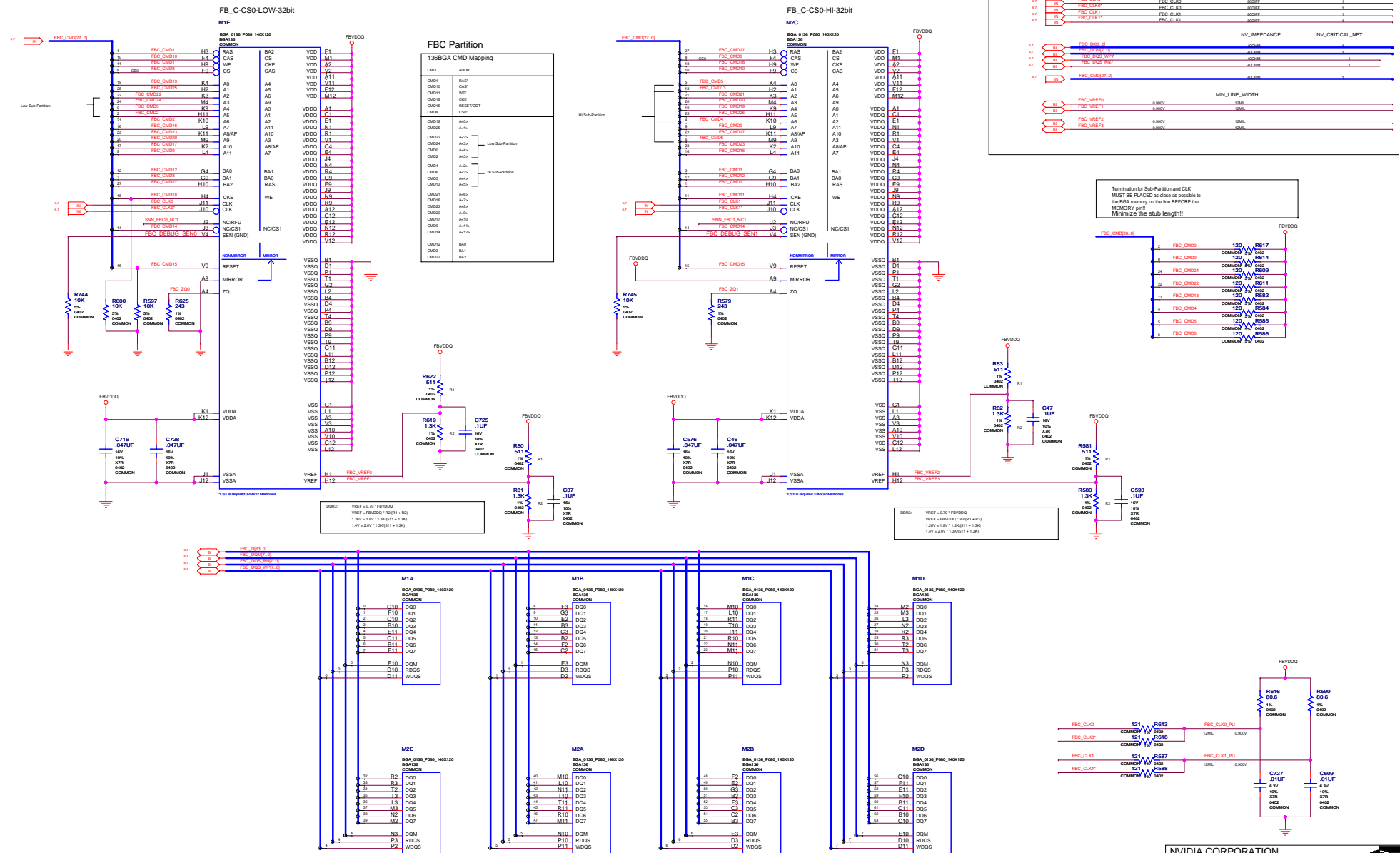


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ASSEMBLY	BASE LEVEL "GENERIC" SCHEMATIC ONLY. COMMON & NO. 3100FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

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FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS PU'S, FBC CLK TERMS

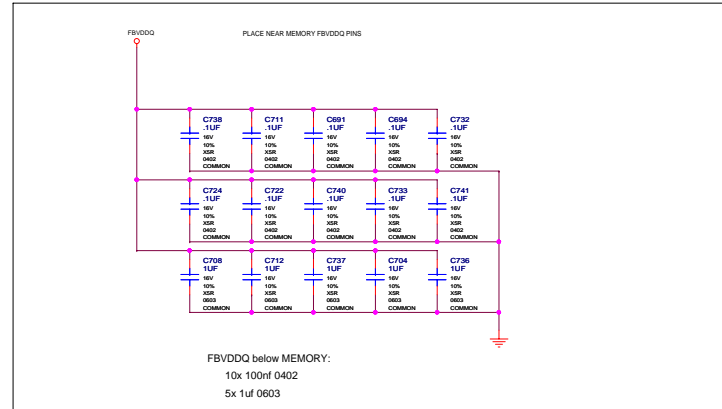
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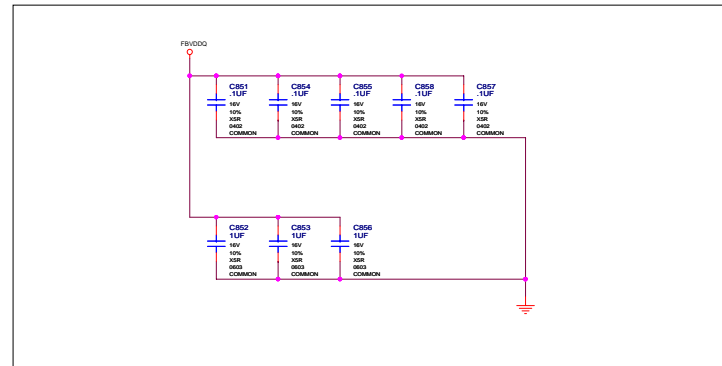


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ID		PAGE	
NAME		DATE	31-OCT-2007

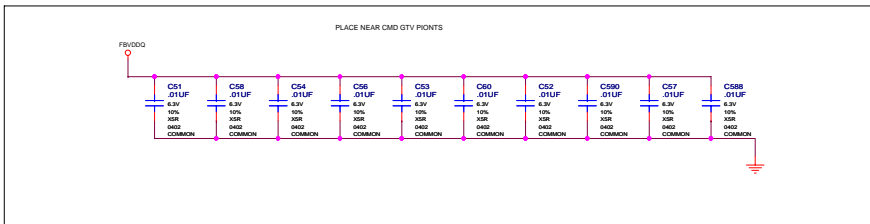
Decoupling for FBC 0..31



Decoupling for FBC C1 0..31

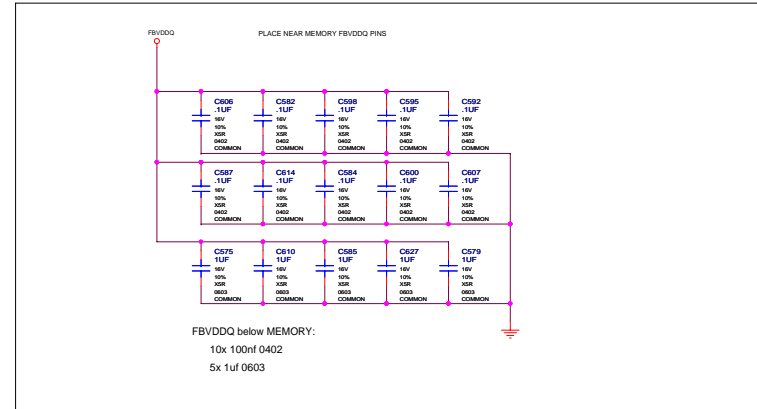


Return path coupling GND/FB/VDDQ for FBC

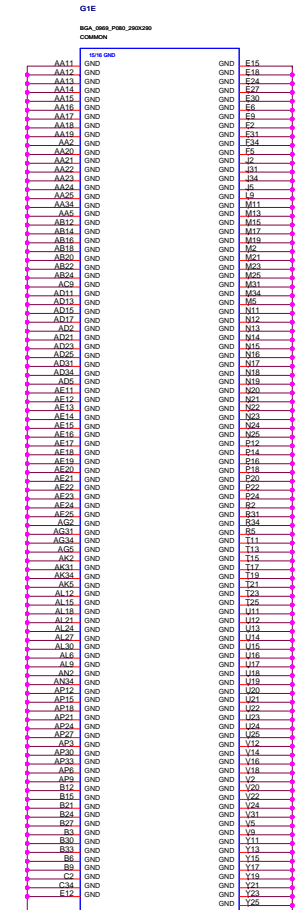
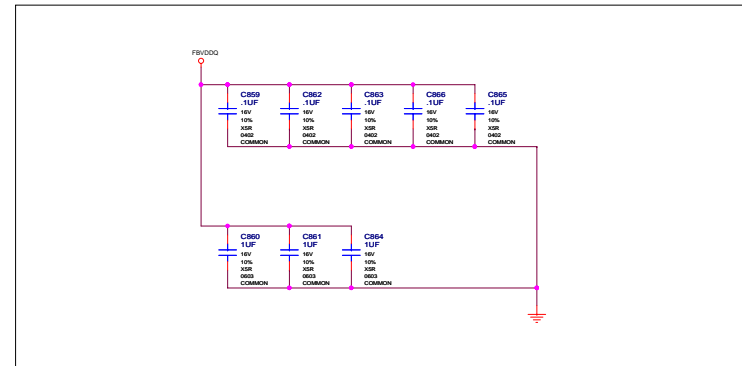


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Decoupling for FBC 32..63



Decoupling for FBC C1 32..63




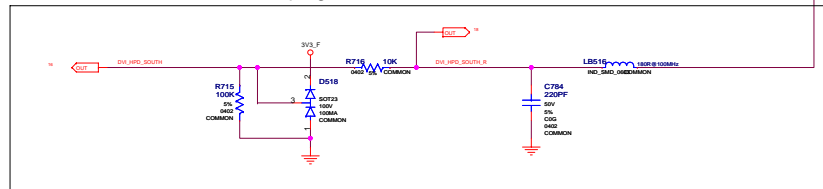
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS, GPU GND CONNECTIONS


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NAME		DATE	31-OCT-2007

DACA RGB-FILTER



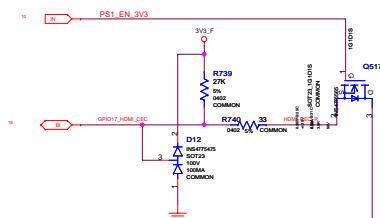
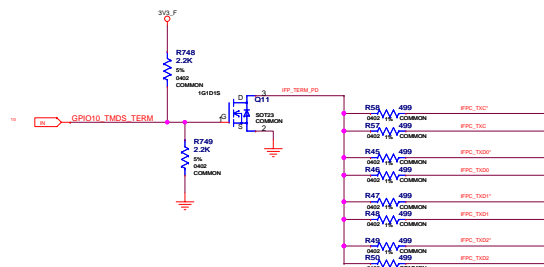
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NAME		DATE	31-OCT-2007

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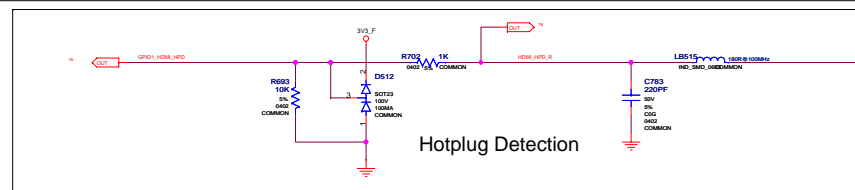
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN		600-10727-base-sch A	
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NAME		DATE	31-OCT-2007

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TMDS LINK: C & D



TMDS C : HDMI



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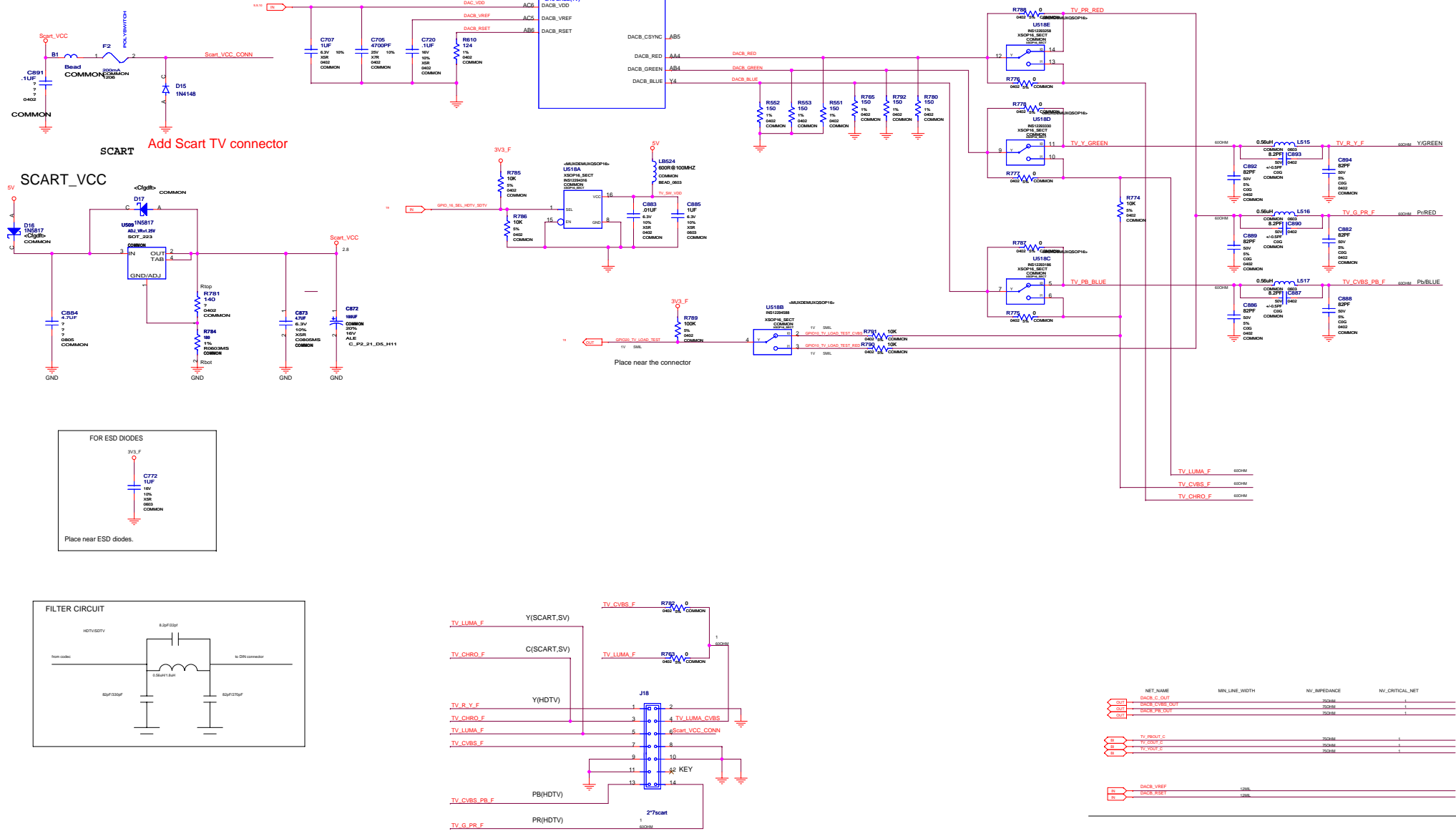
NV_PN	600-10727-base-sch A
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NAME		DATE	31-OCT-200

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK C/D, AC COUPLING, PD's, DVI CONNECTOR MID

DACB: SD/HD VIDEO OUT CONNECTOR



NET_NAME	MIN_LINE_WIDTH	IV_IMPEDANCE	IV_CRITICAL_NET
OUT1	DACR_C_OUT	200R	1
OUT2	DACR_C_OUT	200R	1
OUT3	DACR_P6_OUT	200R	1
OUT4	DACR_P6_OUT	200R	1
IN1	TV_PROD1_C	200R	1
IN2	TV_PROD1_C	200R	1
IN3	TV_PROD1_C	200R	1
IN4	TV_PROD1_C	200R	1
IN5	DACR_VREF	200R	1
IN6	DACR_VREF	200R	1

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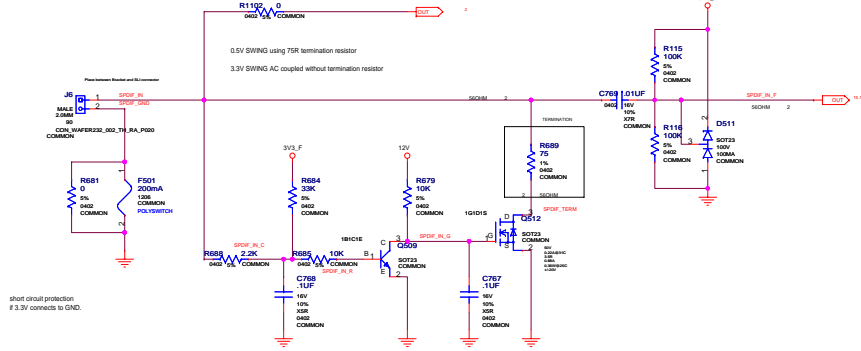
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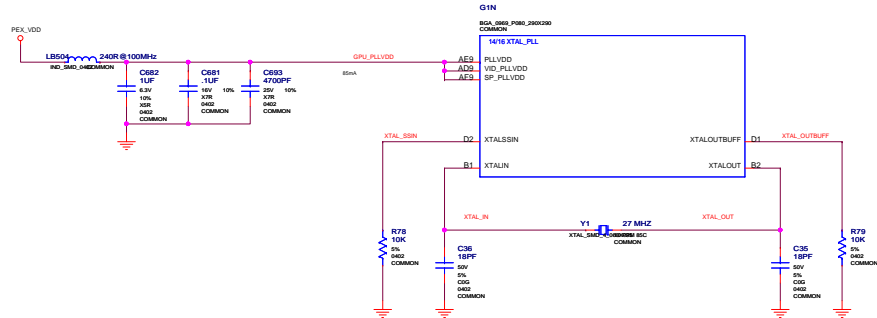
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, MINIDIIN CONNECTOR NORTH, SD/HI VIDEO OUTPUT CONNECTOR

XTAL/PLLVDD/SPDIF IN

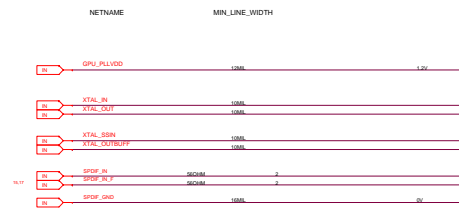
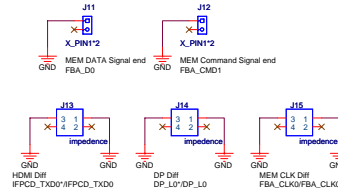
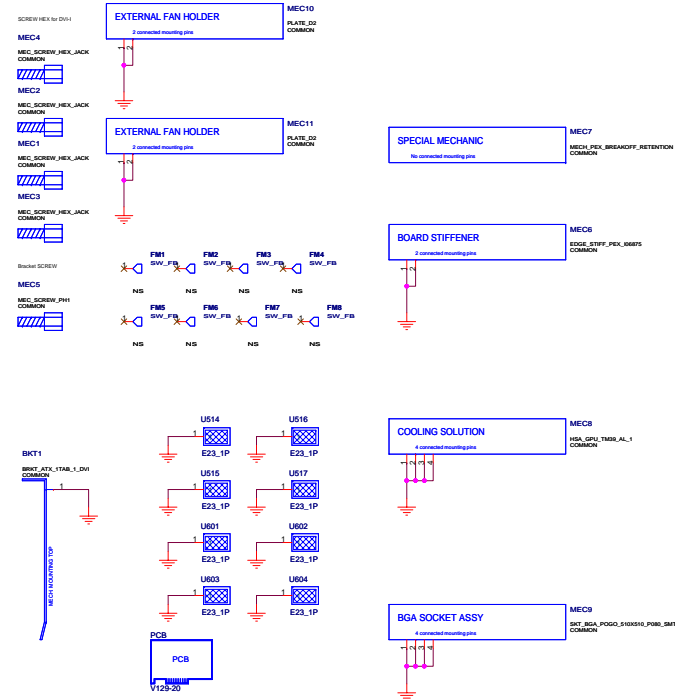
SPDIF IN



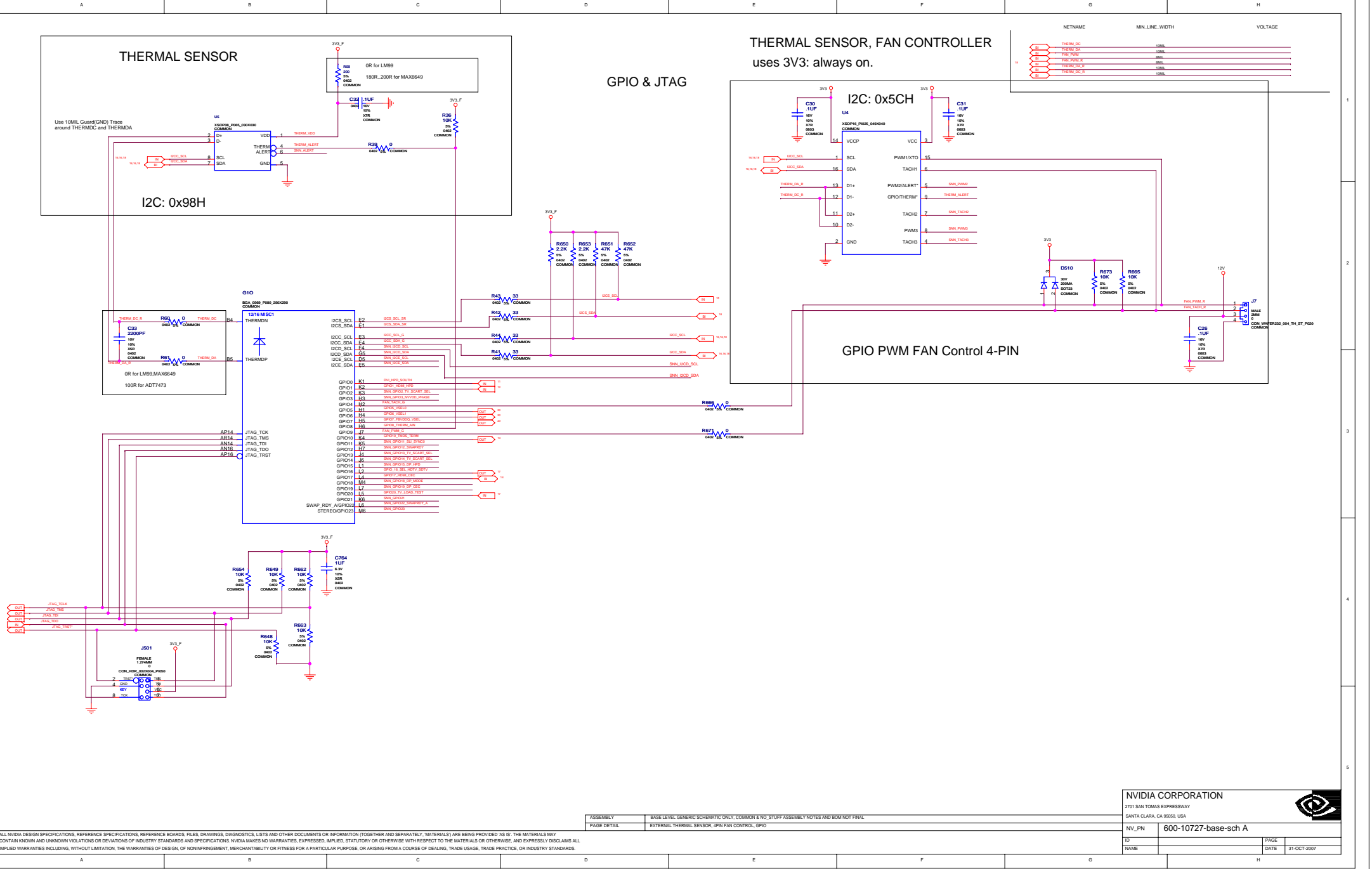
XTAL/GPU_PLLVDD



MECHANICALS & THERMALS



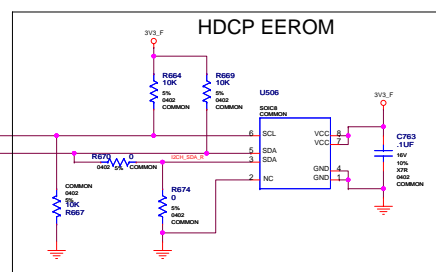
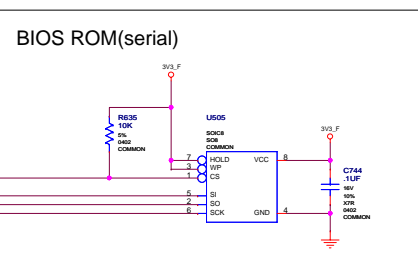
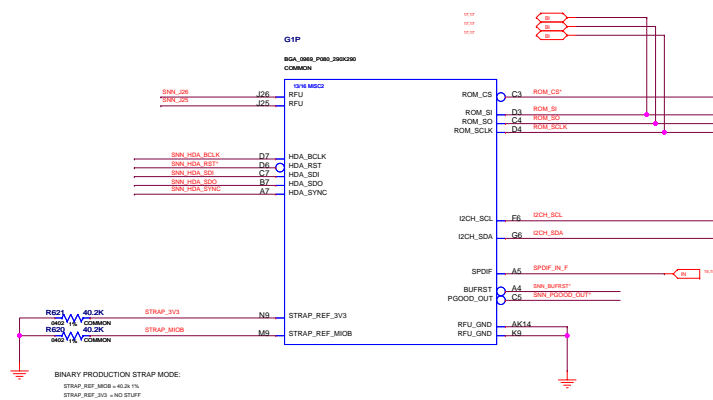
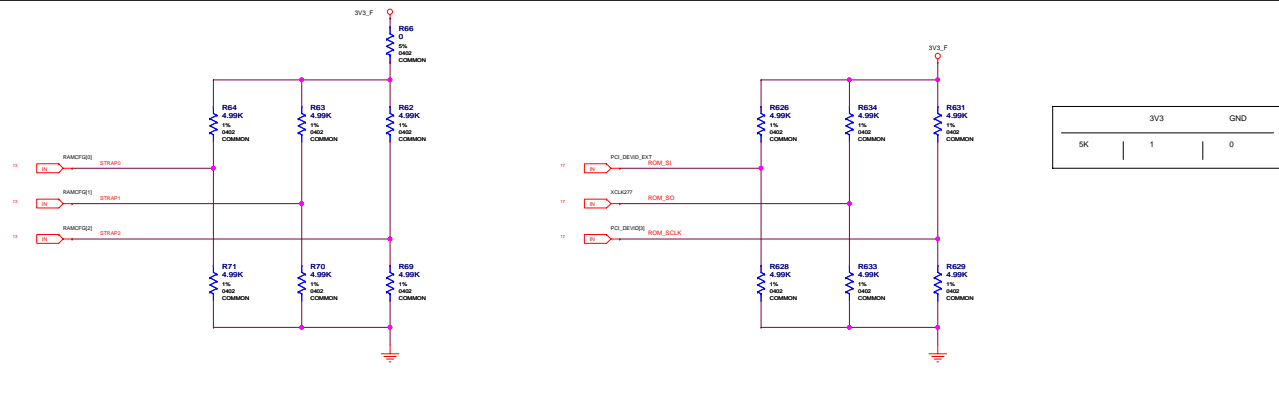
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STRAPPING OPTIONS

Assembly: BIOS



	NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
OUT	HDA_BCLK		50ΩΩM	2
OUT	HDA_RST*		50ΩΩM	2
OUT	HDA_SPS		50ΩΩM	2
OUT	HDA_SSDO		50ΩΩM	2
OUT	HDA_STXNC		50ΩΩM	2

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

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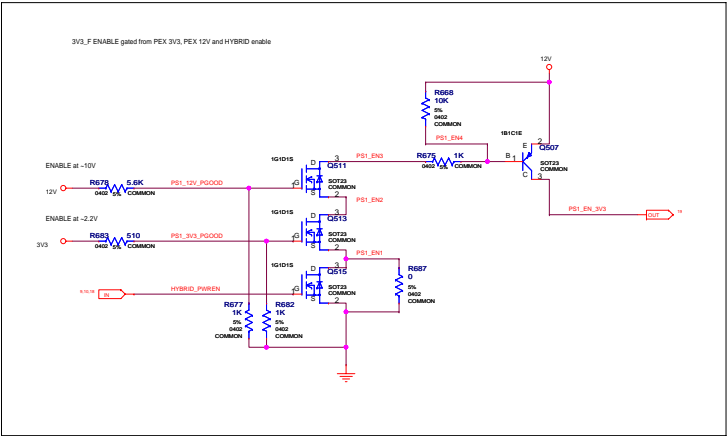
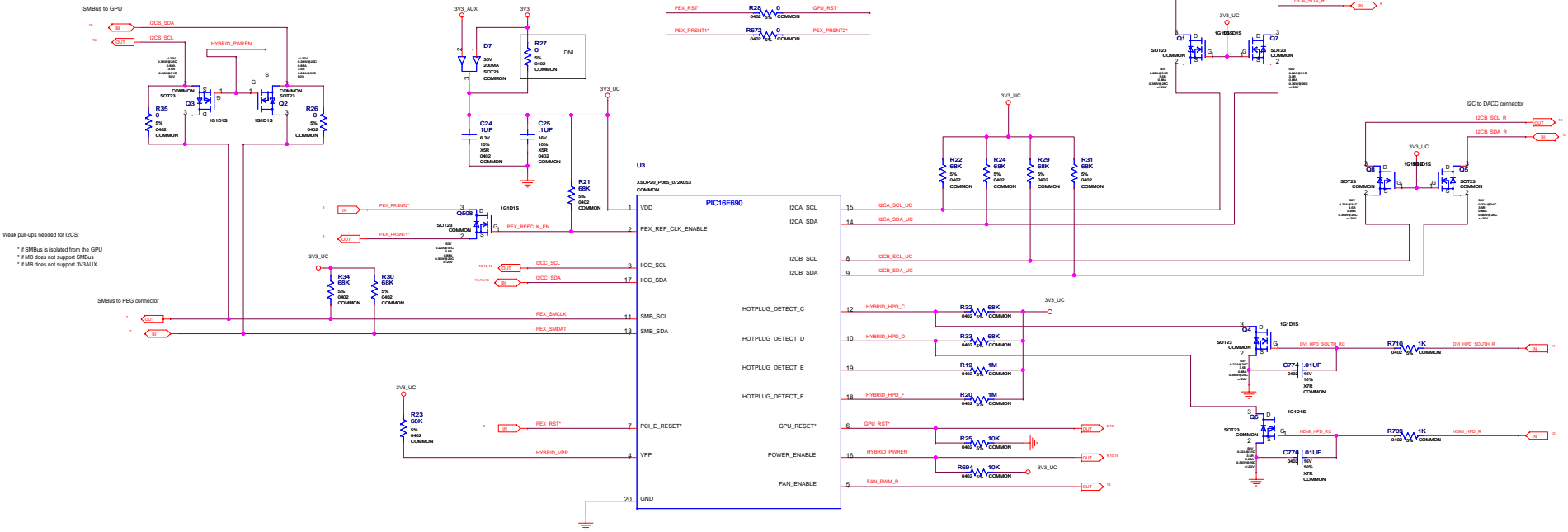
NV_PN	600-10727-base-sch A
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NAME		DATE	31-OCT-2007

HYBRID POWER

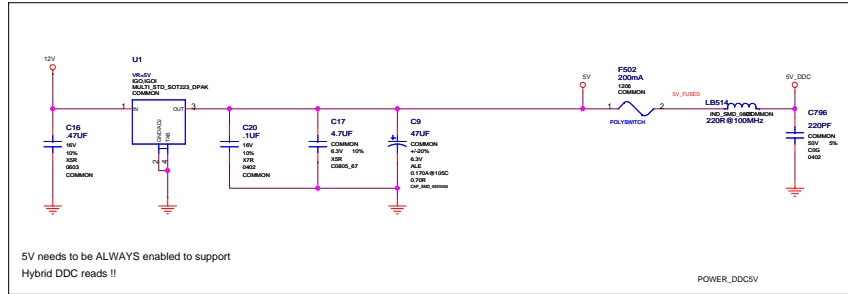
Per Datasheet:
V_I = 400mV at 10mA
* expected current < 2mA

Stuff only to bypass the micro-controller



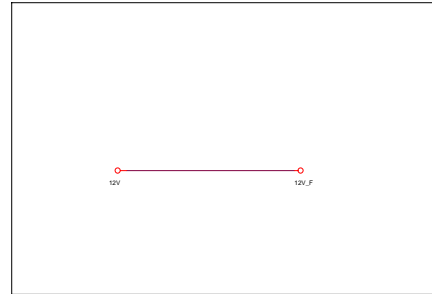
Power Supply: 5V, 5V_DDC, TMDS, MIOA_VDDQ

5V REGULATOR

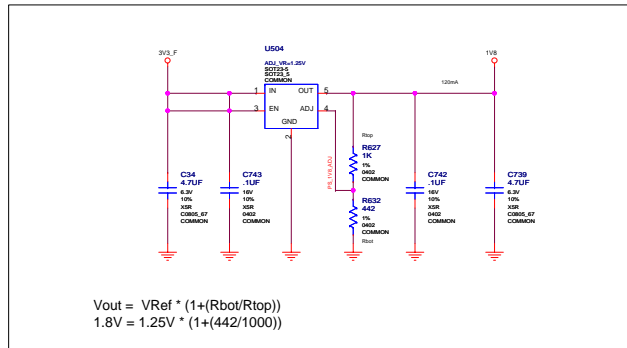


5V DDC

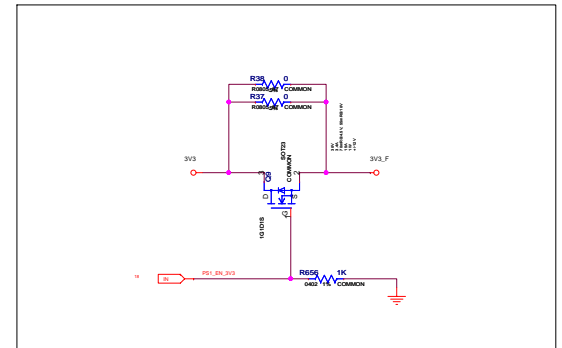
12V filter



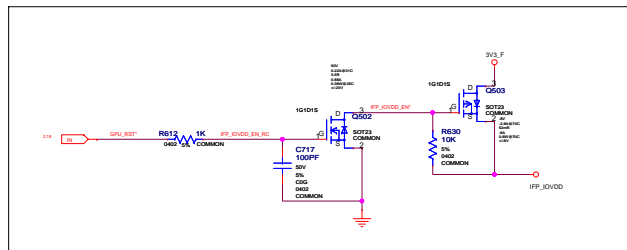
IFP PLL Supply 1.8V












3V3 switch



IFP_IOVDD BACKDRIVE PREVENTION



NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
 5V_PU3ED	0.1A	12800	5V
 5V_D0C	0.1A	12800	5V
5V_D0C			5V
 5V	0.15A	12800	5V
 PS_V1B_A0J			1.80V
PS_V1B_A0J			1.80V
 V1B	0.12A	12800	1.80V
 V1B	0.3A	12800	2.20V
 5V_GND			5V
5V_GND			5V
 V1B_F	3.5A	12800	3.30V
 V1B_F	6A	20400	12V
12V_F			12V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY LINES: 5V, DDC5V, IFF PLLVDD, IFF IOVDD, MIO VDD, 3V3 FILTER, 12V FILTER

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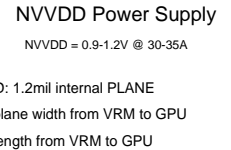


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	Net Name	LINE_WIDTH	Current	Voltage
	N1020	3895L	15A	1.2V
	P2702	3895L	1.5A	1.2000V
L2H	N1000_SENSE	1695L	0.5A	1.2V
	N1000_SENSE_W	1695L	0.5A	1.2V



	GPI06	GPI05
NVDD = 1.00V R7403 1.54K R7329 6.19K	0	0
NVDD = 1.05V R7403 1.54K R7329 6.19K R661 24.3K	0	1
NVDD = 1.10V R7403 1.54K R7329 6.19K R676 12.1K	1	0
NVDD = 1.15V (Underline) R7403 1.54K R7329 6.19K R661 24.3K R676 12.1K	1	1

	GPIO5
NV/VDD = 0.95V R7403 1.00K R7329 5.36K	1
NV/VDD = 1.00V R7403 1.00K R7329 5.36K R861 16.2K	0

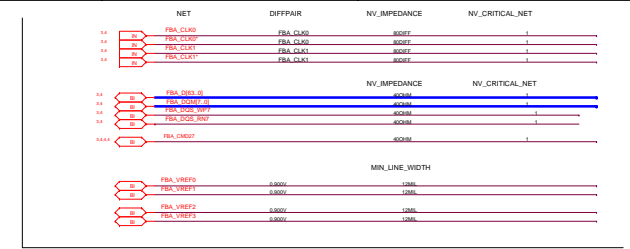
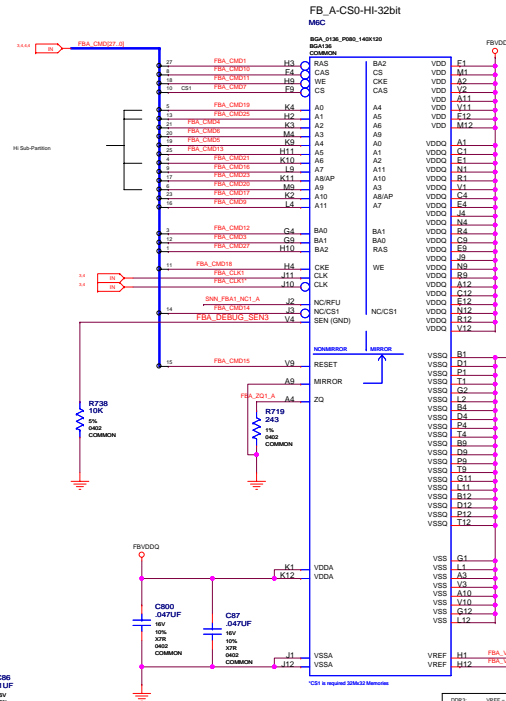
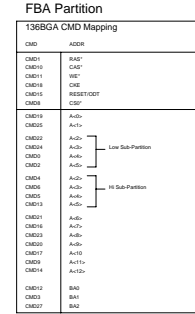
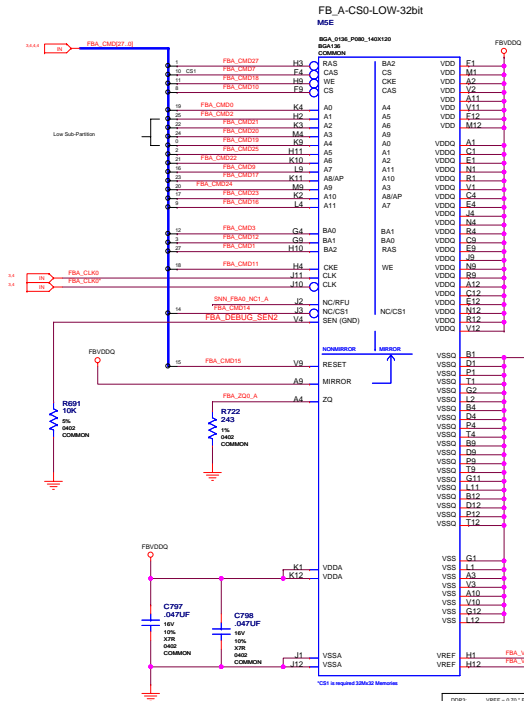
2701 SAN TOMAS EXPRESSWAY
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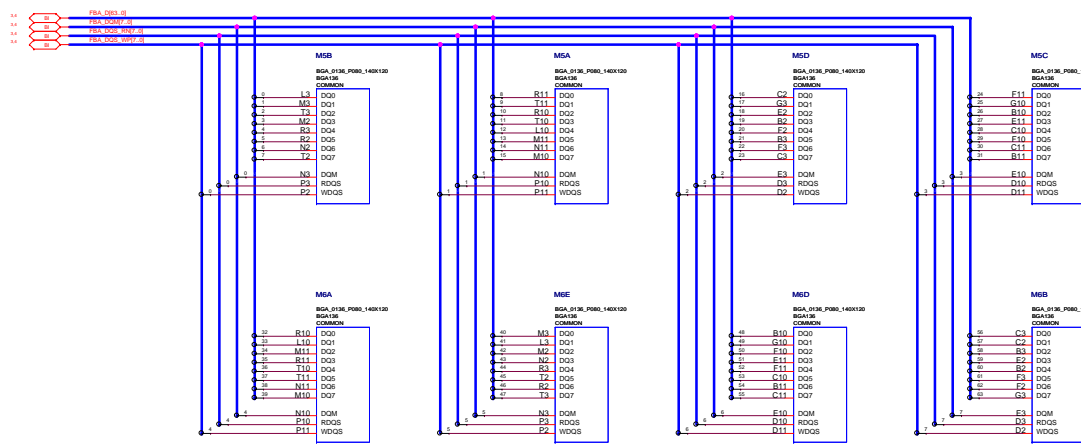
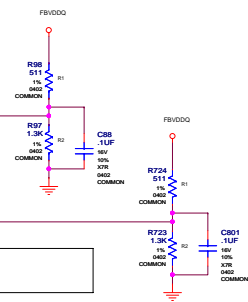
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FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3



Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16/32Mx32 GDOR3 MEMORIES, FBA COMMAND BUS P/U'S, FBA CLK TERMS

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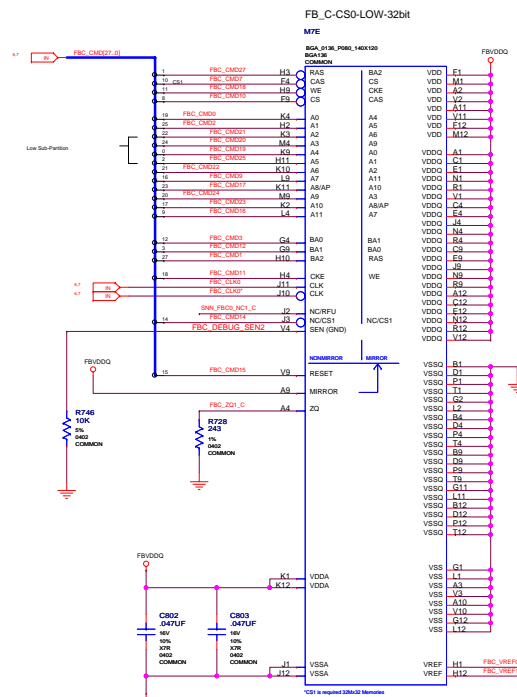
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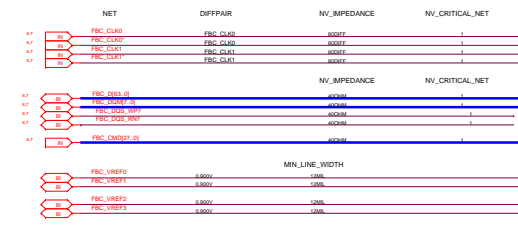
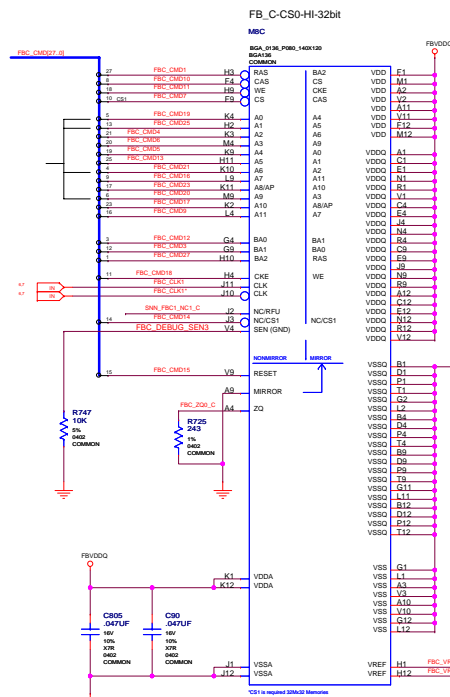
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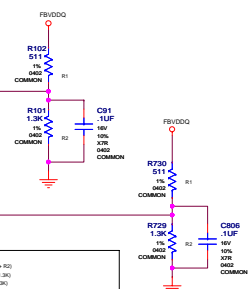
FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3



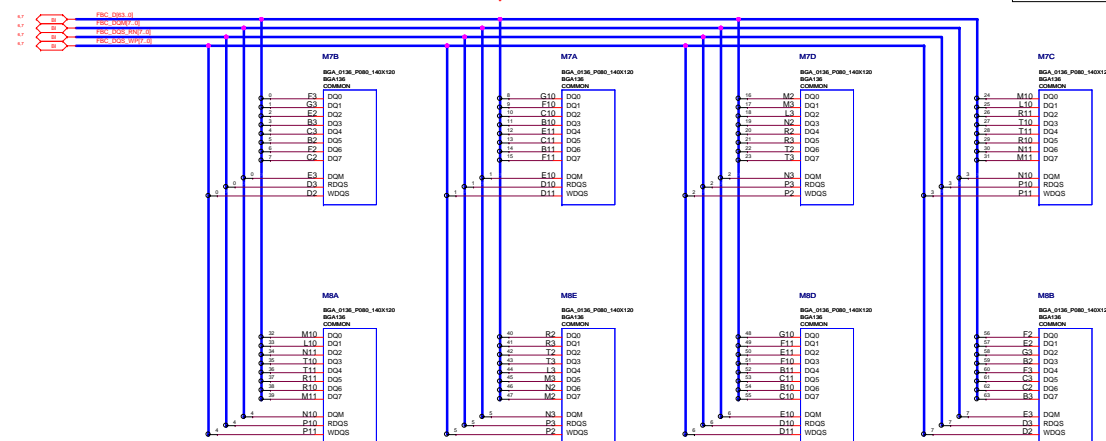
FBC Partition			CSD
CMD	ADDR		
CMD1	RAS*		
CMD2	CAS*		
CMD11	WE*		
CMD18	CKE		
CMD16	RESET/ODT		
CMD8	CS*		
CMD19	Ar1*		
CMD25	Ar2*		
CMD3	Ar3*	} Low Sub-Partition	
CMD4	Ar3*		
CMD0	Ar6*		
CMD2	Ar2*	} H8 Sub-Partition	
CMD4	Ar3*		
CMD6	Ar6*		
CMD8	Ar6*		
CMD13	Ar6*		
CMD21	Ar6*		
CMD16	Ar7*		
CMD23	Ar8*		
CMD30	Ar8*		
CMD17	Ar10		
CMD6	Ar11*		
CMD14	Ar12*		
CMD12	BA0		
CMD3	BA1		
CMD27	BA2		



Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!



COR2: $V_{REF} = 0.70 \cdot FVDDQ$
 $V_{REF} = FVDDQ \cdot R2/(R1 + R2)$
 $1.26V = 1.8V \cdot 1.3K/(511 + 1.3K)$
 $1.4V = 2.6V \cdot 1.3K/(511 + 1.3K)$

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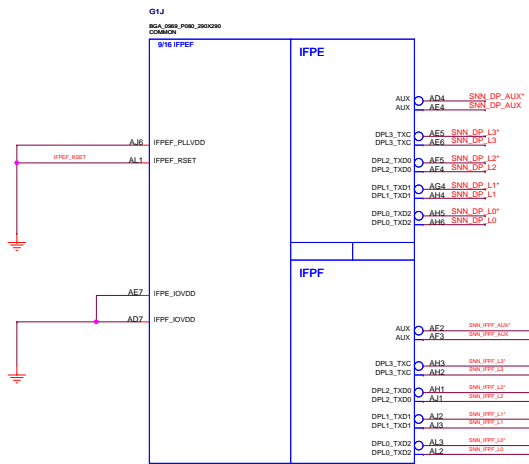
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS P/U'S, FBC CLK TERMS

TMDS E : Display Port



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO STOP ASSEMBLY NOTES AND NOT FINAL
PAGE DETAIL	TMDS LINK C/D, AC COUPLING, PDs, DVI CONNECTOR MID

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