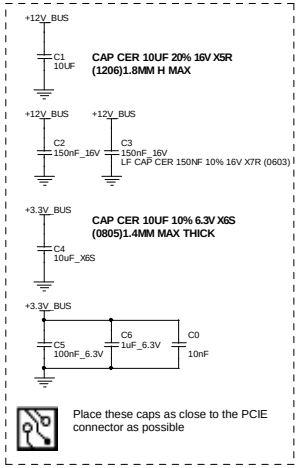
PCI-EXPRESS EDGE CONNECTOR



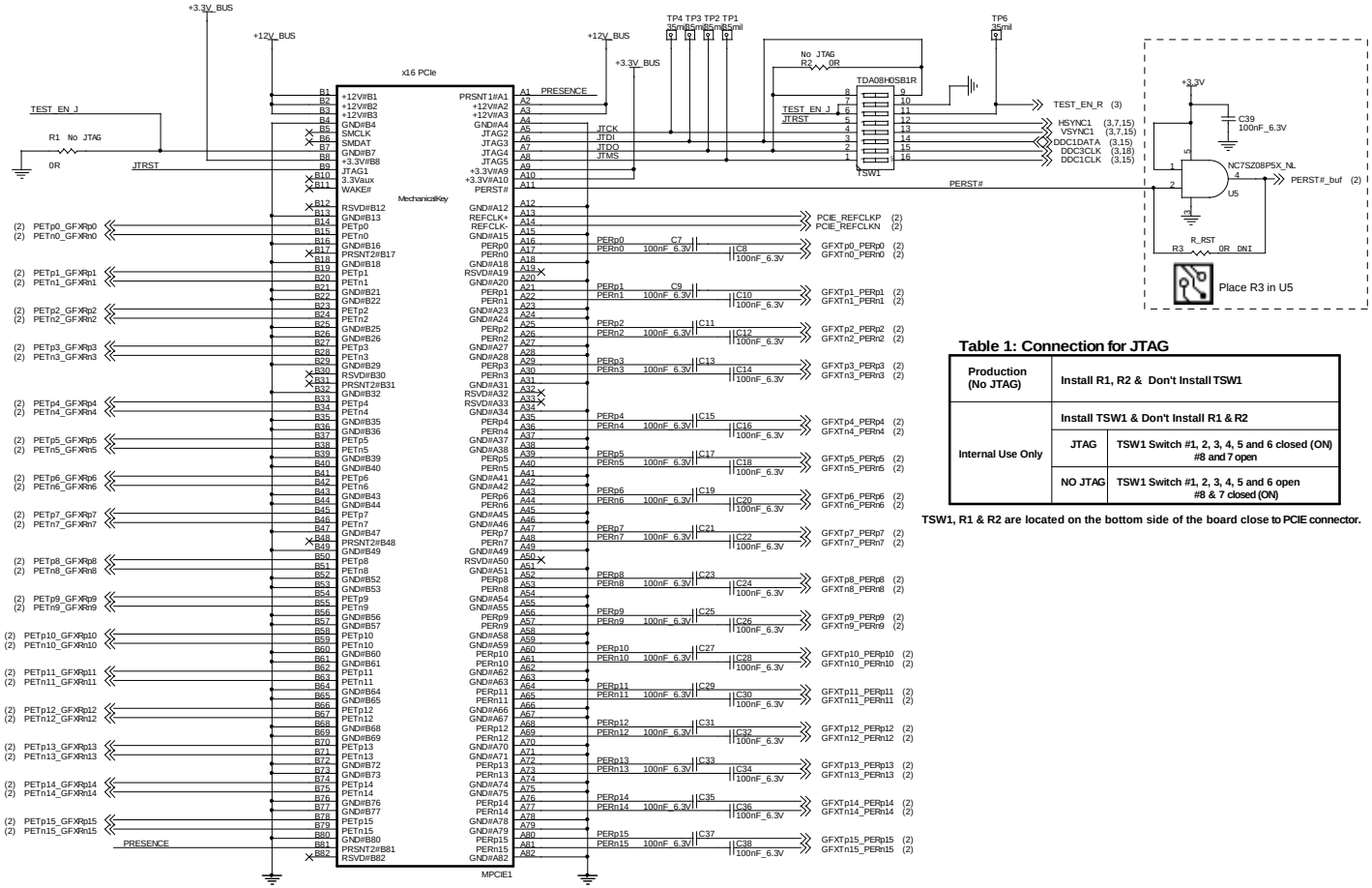


Table 1: Connection for JTAG

Production (No JTAG)	**Install R1, R2 & Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R1 & R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)**

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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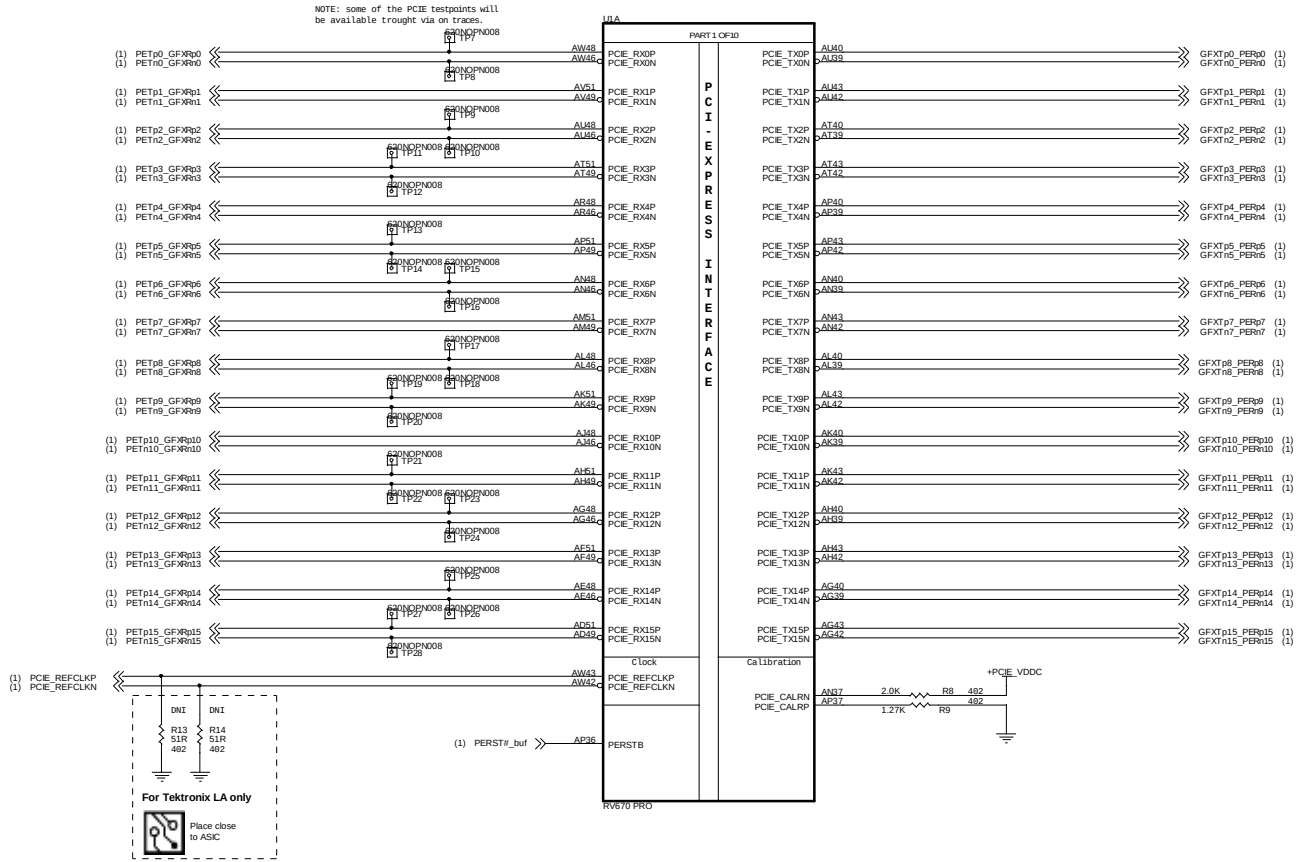
Date: Friday, September 07, 2007 Rev 2

Sheet 1 of 21

Title: RH RV670 - PCI-E Edge Connector

Doc No. 105-B340xx-00



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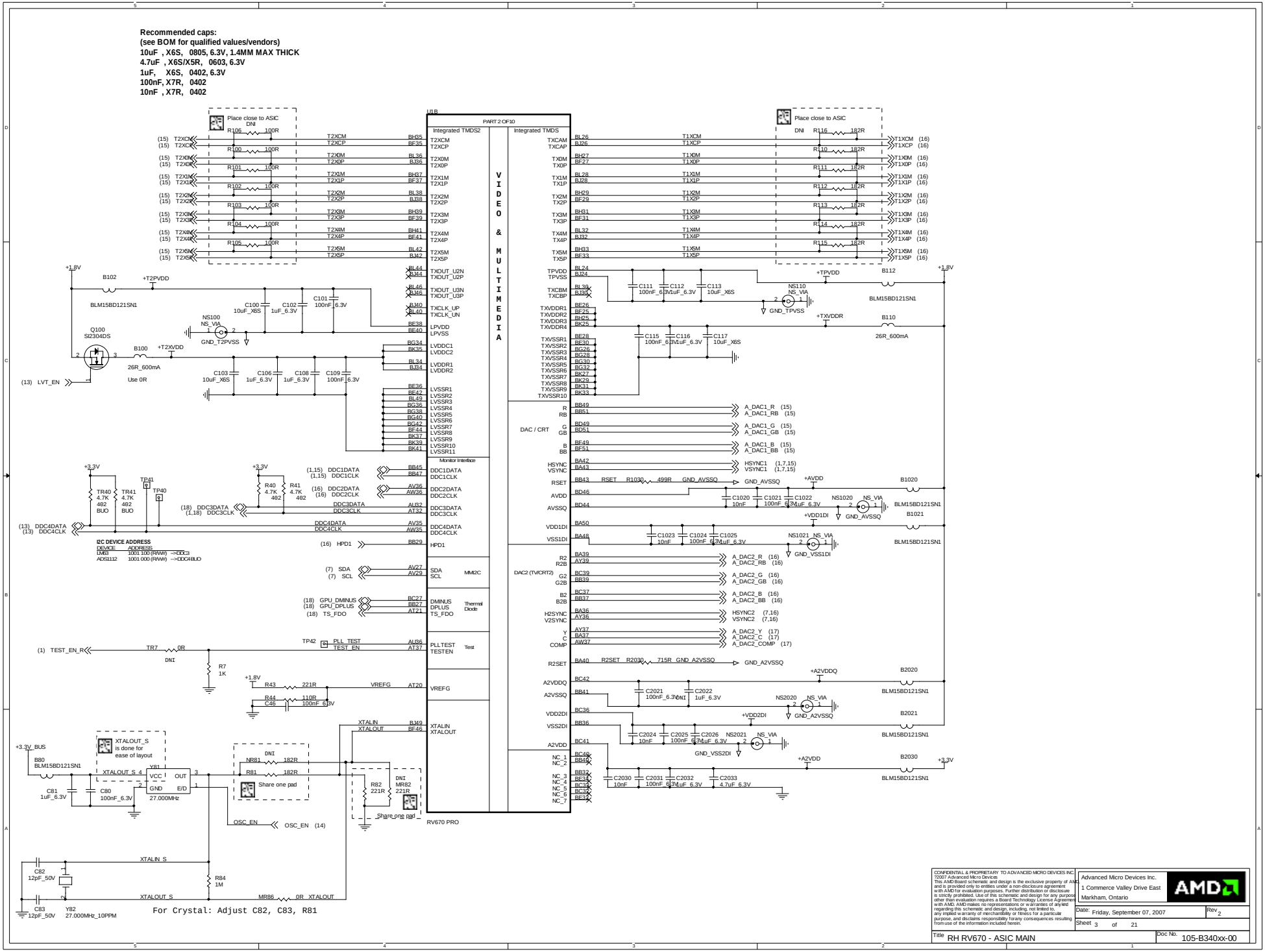
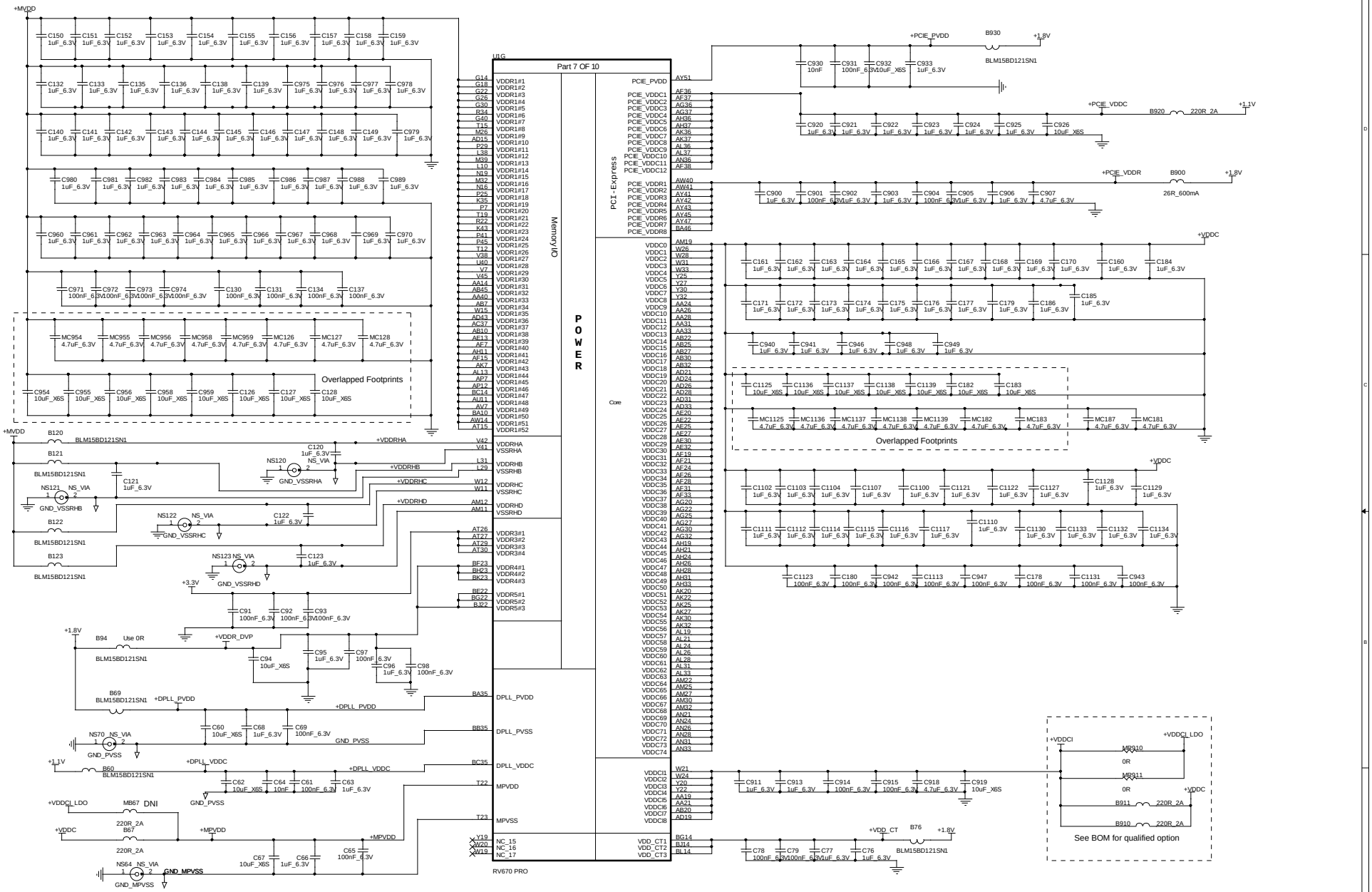
Date: Friday, September 07, 2007 Rev 2

Sheet 2 of 21

Title: RH RV670 - ASIC PCIE_Interface

Doc No. 105-B340xx-00





Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402

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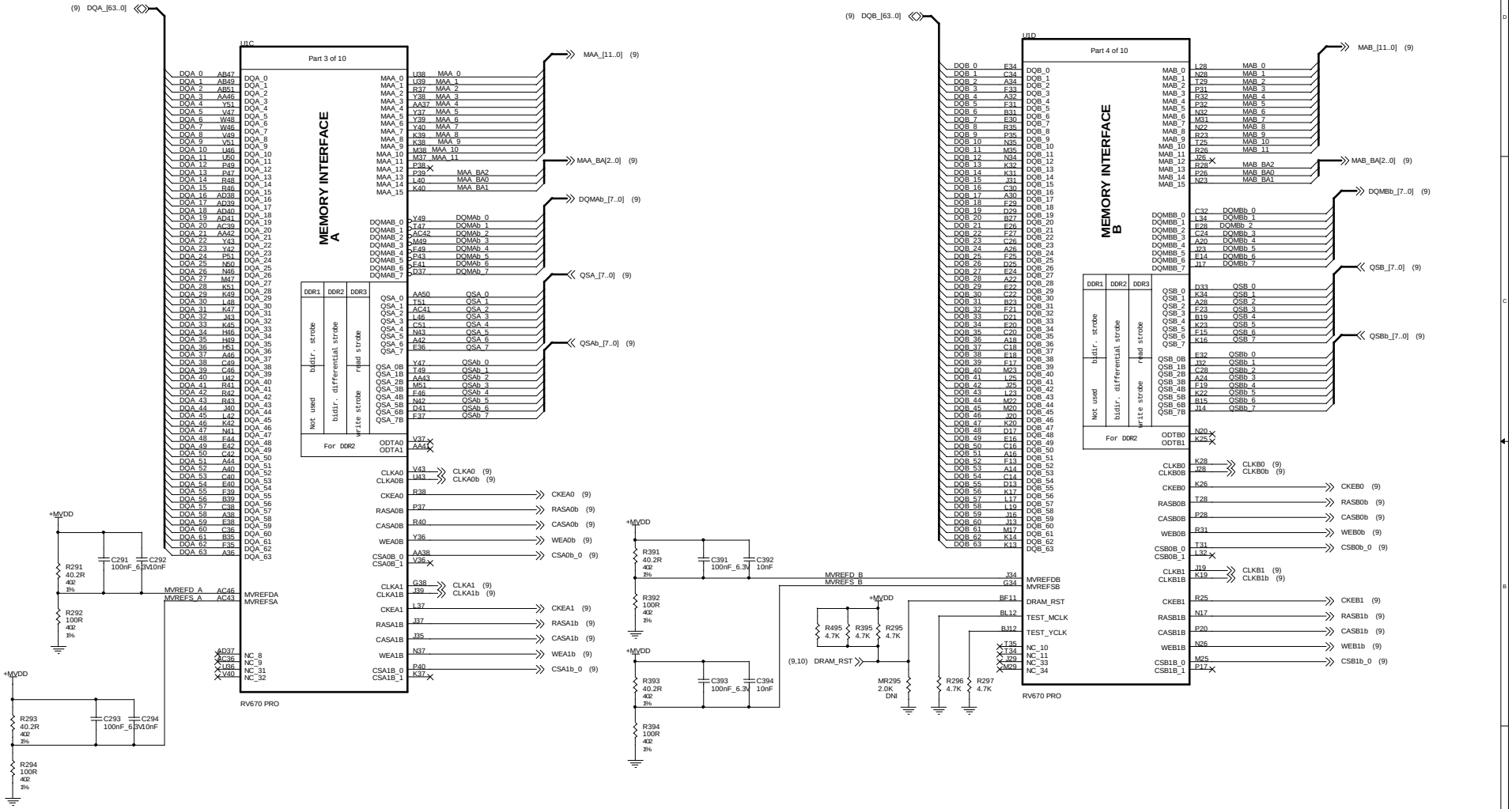
Date: Friday, September 07, 2007 Rev 2

Sheet 4 of 21

Title: RH RV670 - ASIC Power

Doc No. 105-B340xx-00



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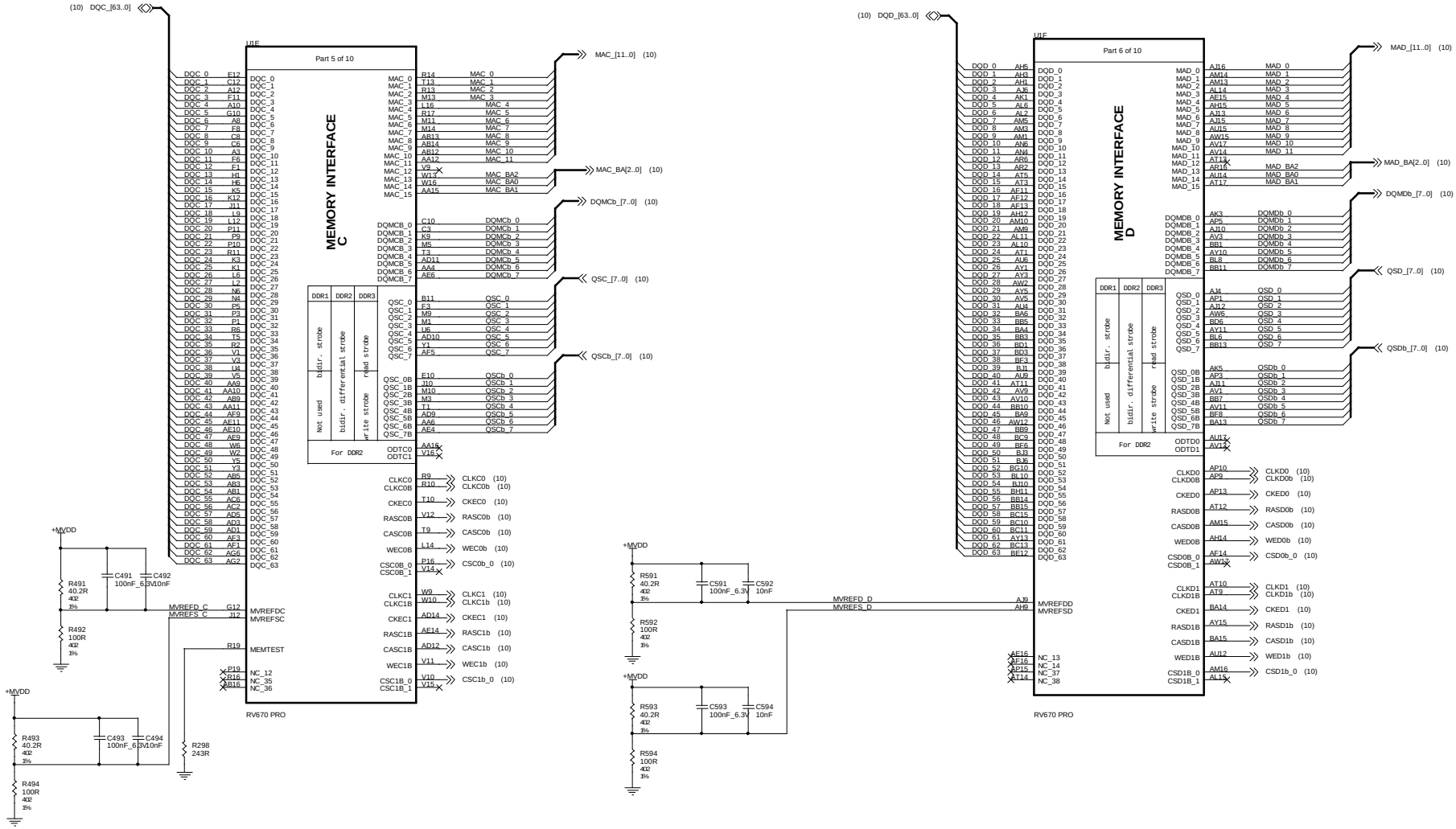
Date: Friday, September 07, 2007 Rev 2

Sheet 5 of 21

Title: RH RV670 - ASIC Memory Interface (Channel A & B)

Doc No. 105-B340xx-00



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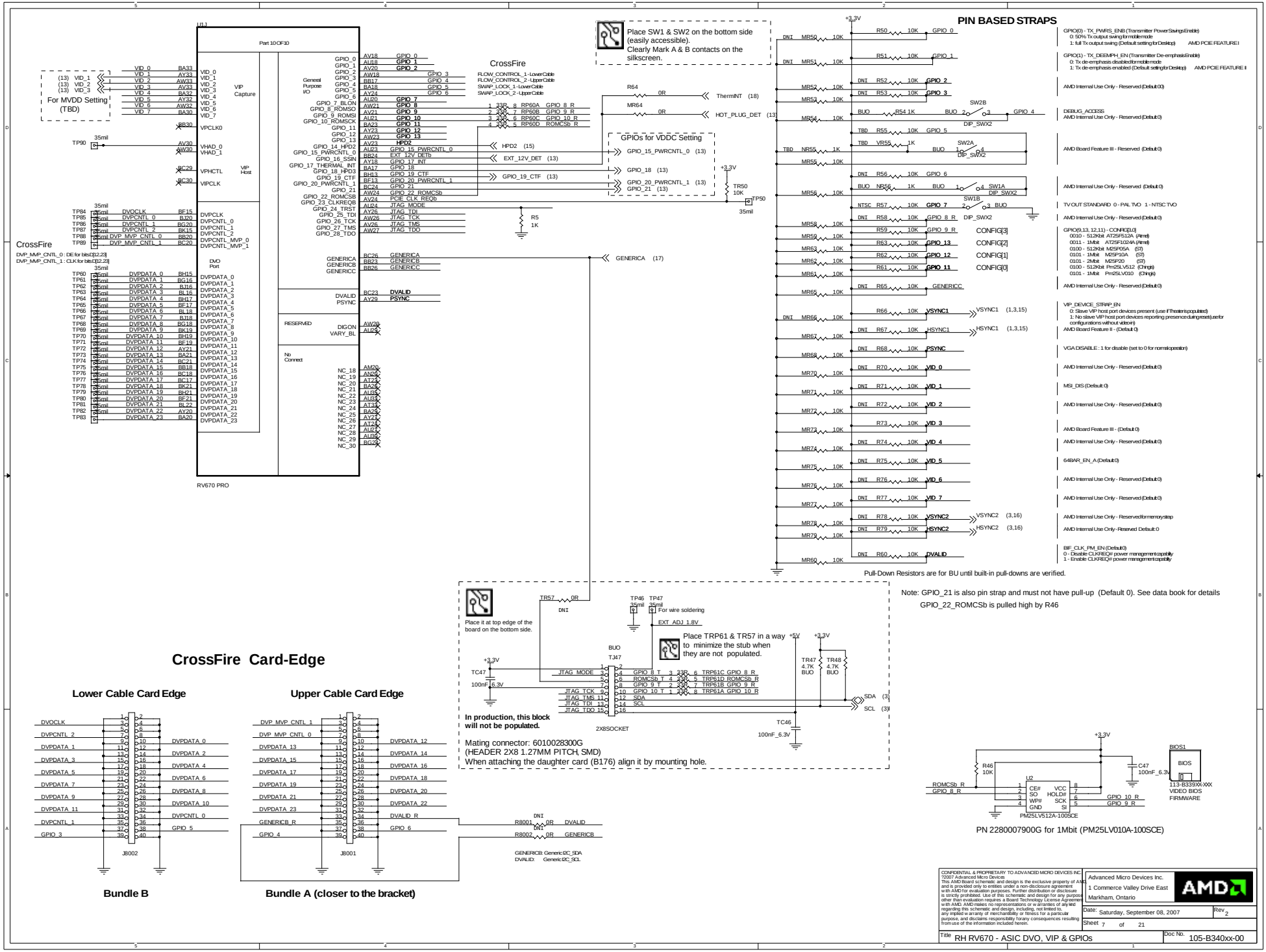
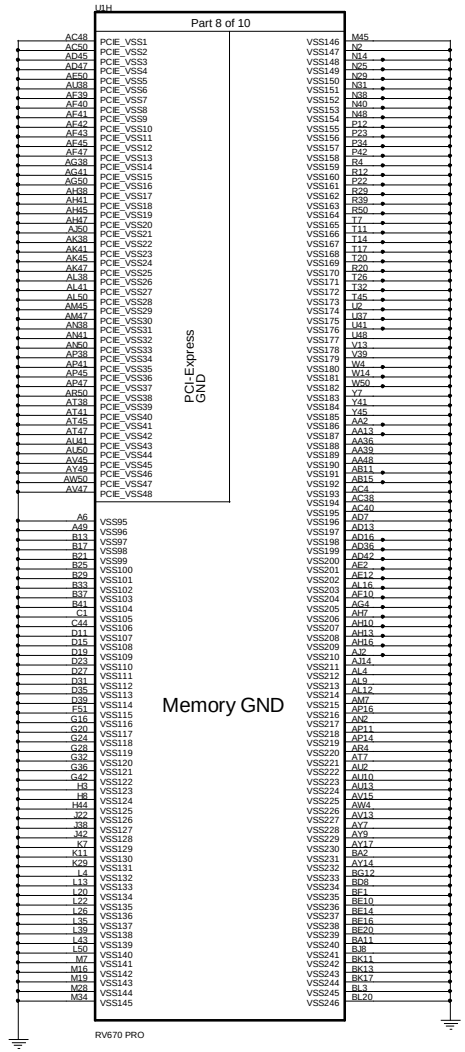
Date: Friday, September 07, 2007 Rev 2

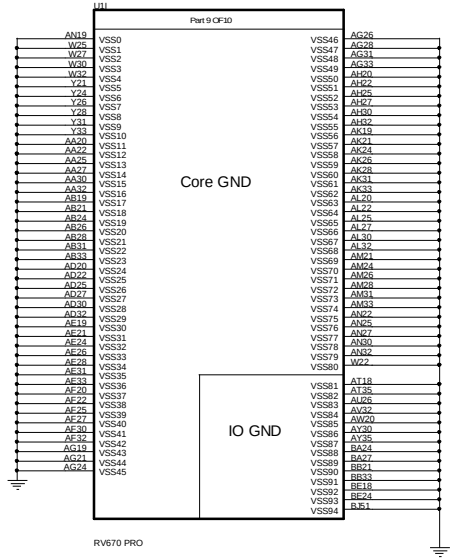
Sheet 6 of 21

Title: RH RV670 - ASIC Memory Interface (Channel C & D)

Doc No. 105-B340xx-00







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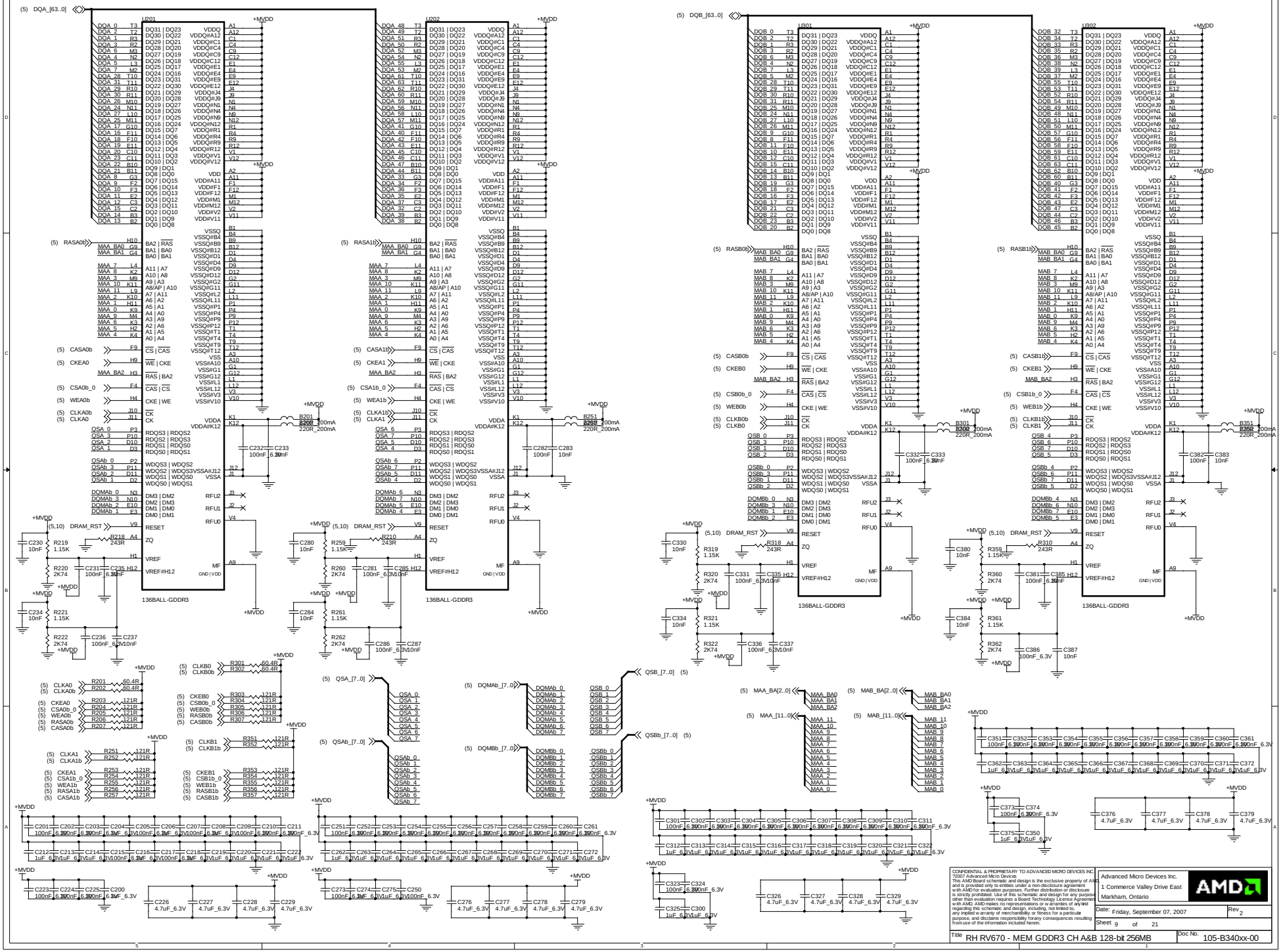
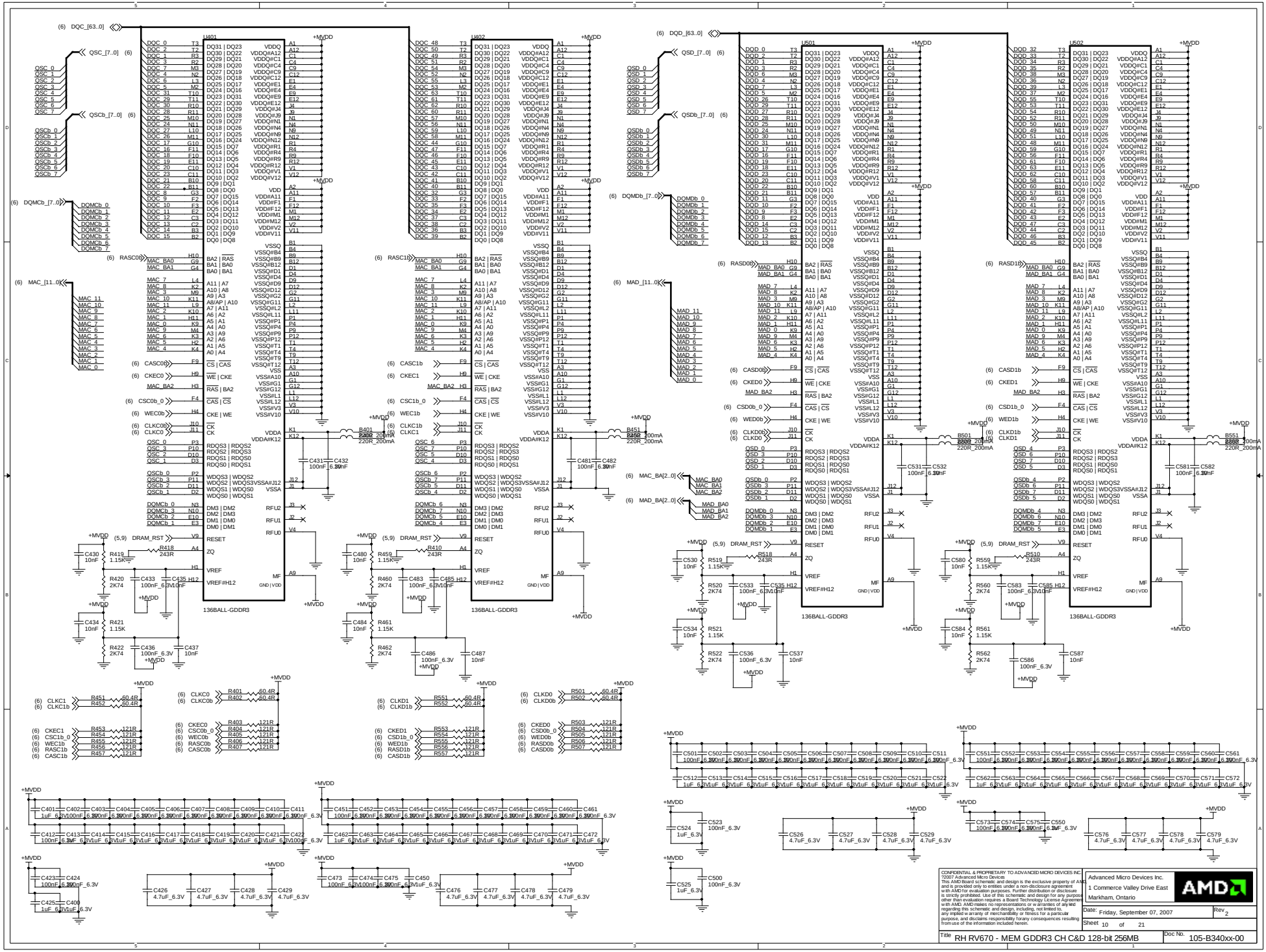
Date: Friday, September 07, 2007 Rev 2

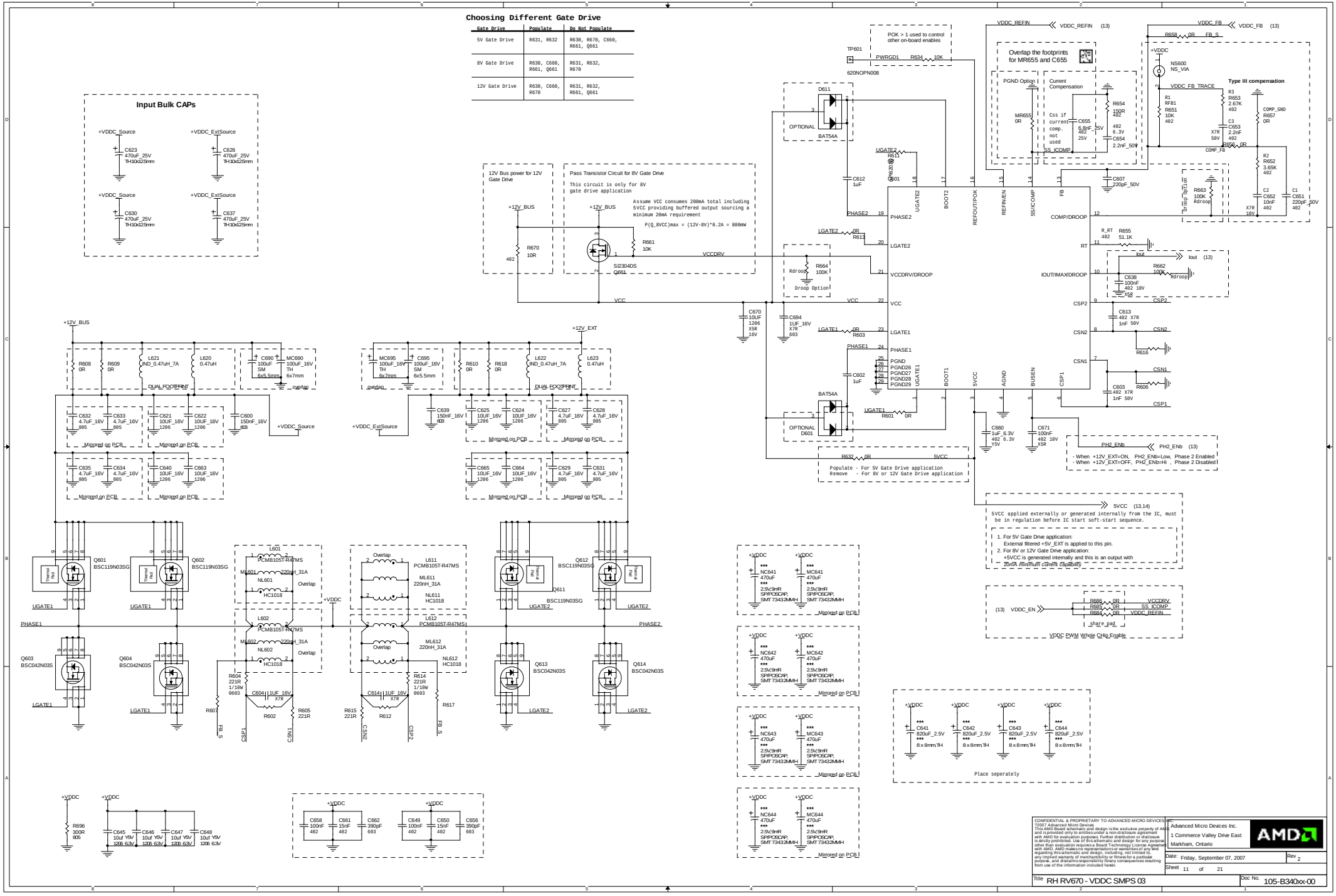
Sheet 8 of 21

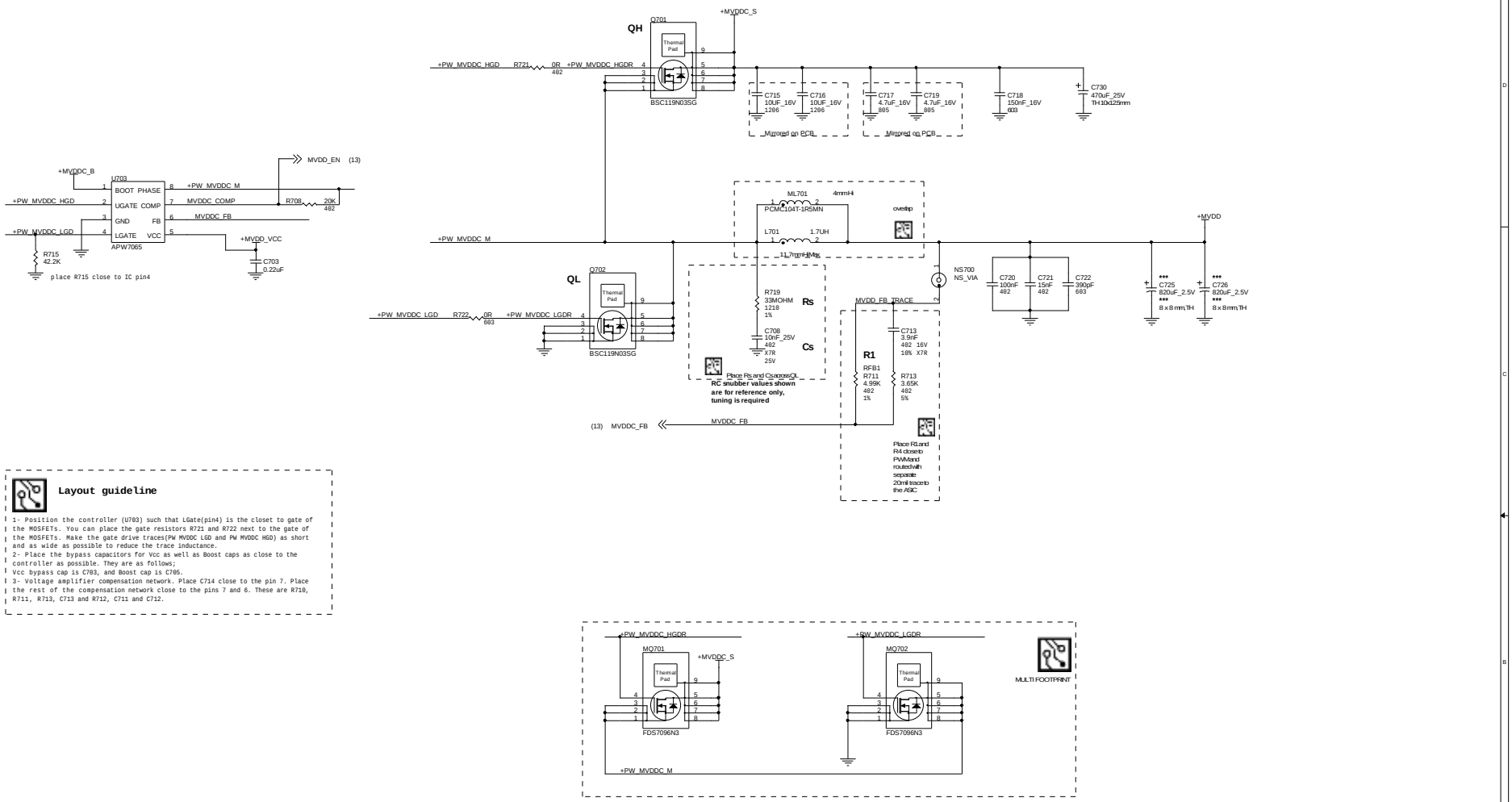
Title: RH RV670 - ASIC Grounds

Doc No. 105-B340xx-00









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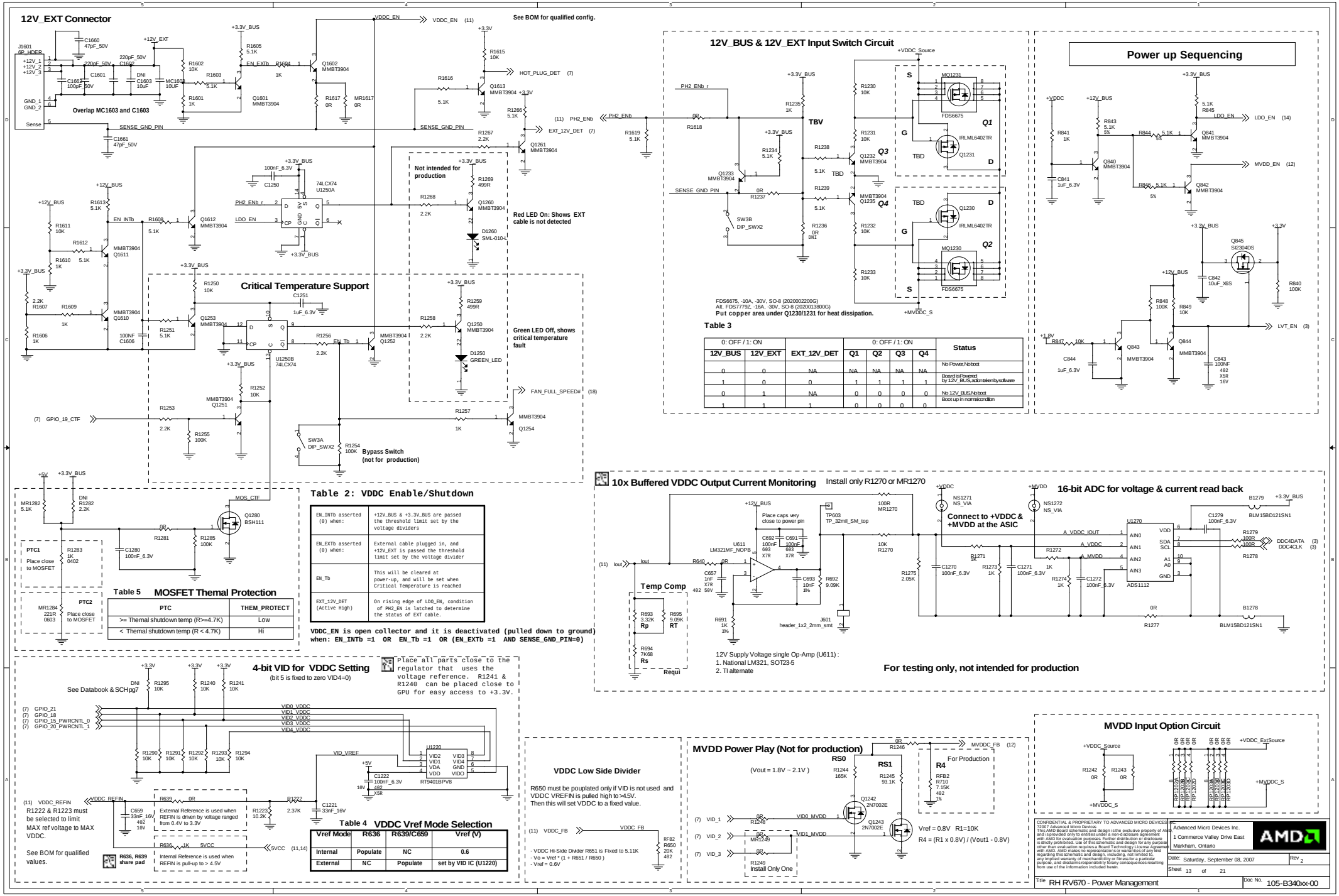
Date:	Friday, September 07, 2007
Rev	2
Sheet	12 of 21
Title	RH RV670 - MVDD SMPS 02
Doc No.	105-B340xx-00



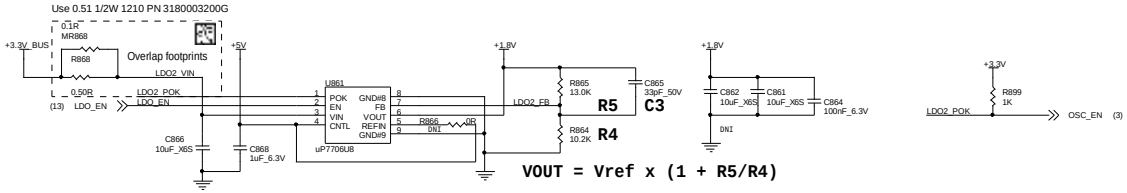
0: OFF / 1: ON			0: OFF / 1: ON				Status
12V_BUS	12V_EXT	EXT_12V_DET	Q1	Q2	Q3	Q4	
0	0	NA	NA	NA	NA	NA	No Power,No boot
1	0	0	1	1	1	1	Board is Powered by 12V_BUS,action taken by software
0	1	NA	0	0	0	0	No 12V_BUS,No boot
1	1	1	0	0	0	0	Boot up in normal condition

EN_INTb asserted (0) when:	+12V_BUS & +3.3V_BUS are passed the threshold limit set by the voltage dividers
EN_EXTb asserted (0) when:	External cable plugged in, and +12V_EXT is passed the threshold limit set by the voltage divider
EN_Tb	This will be cleared at power-up, and will be set when Critical Temperature is reached
EXT_12V_DET (Active High)	On rising edge of LDO_EN, condition of PH2_EN is latched to determine the status of EXT cable.

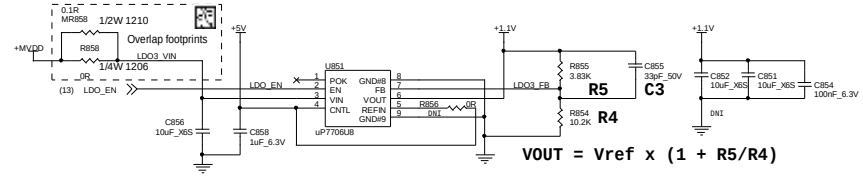
PTC	THEM_PROTECT
>= Themal shutdown temp (R>=4.7K)	Low
< Themal shutdown temp (R < 4.7K)	Hi

Vref Mode	R636	R639/C659	Vref (V)
Internal	Populate	NC	0.6
External	NC	Populate	set by VID IC (U1220)

LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



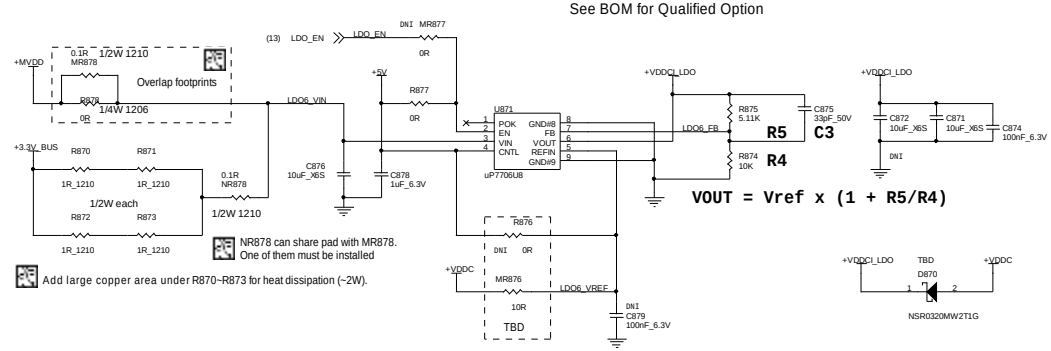
LDO #3: Vin = +1.70V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



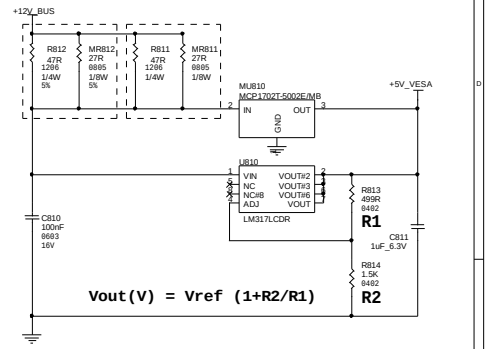
LDO #6: For fixed output voltage: Vin = +1.70V to 2.1V MAX Vout = +1.20V +/- 3% Iout = 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

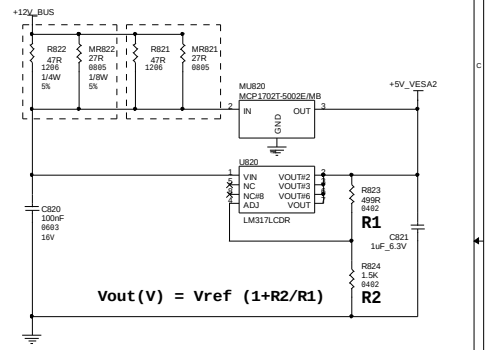
LDO #6: For tracking VDDC: Vin = TBD Vout = TBD Iout = 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

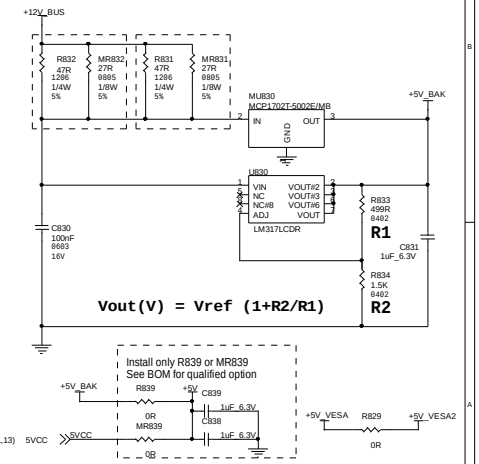
See BOM for Qualified Option



Regulators for +5V, +5V_VESA and +5V_VESA2







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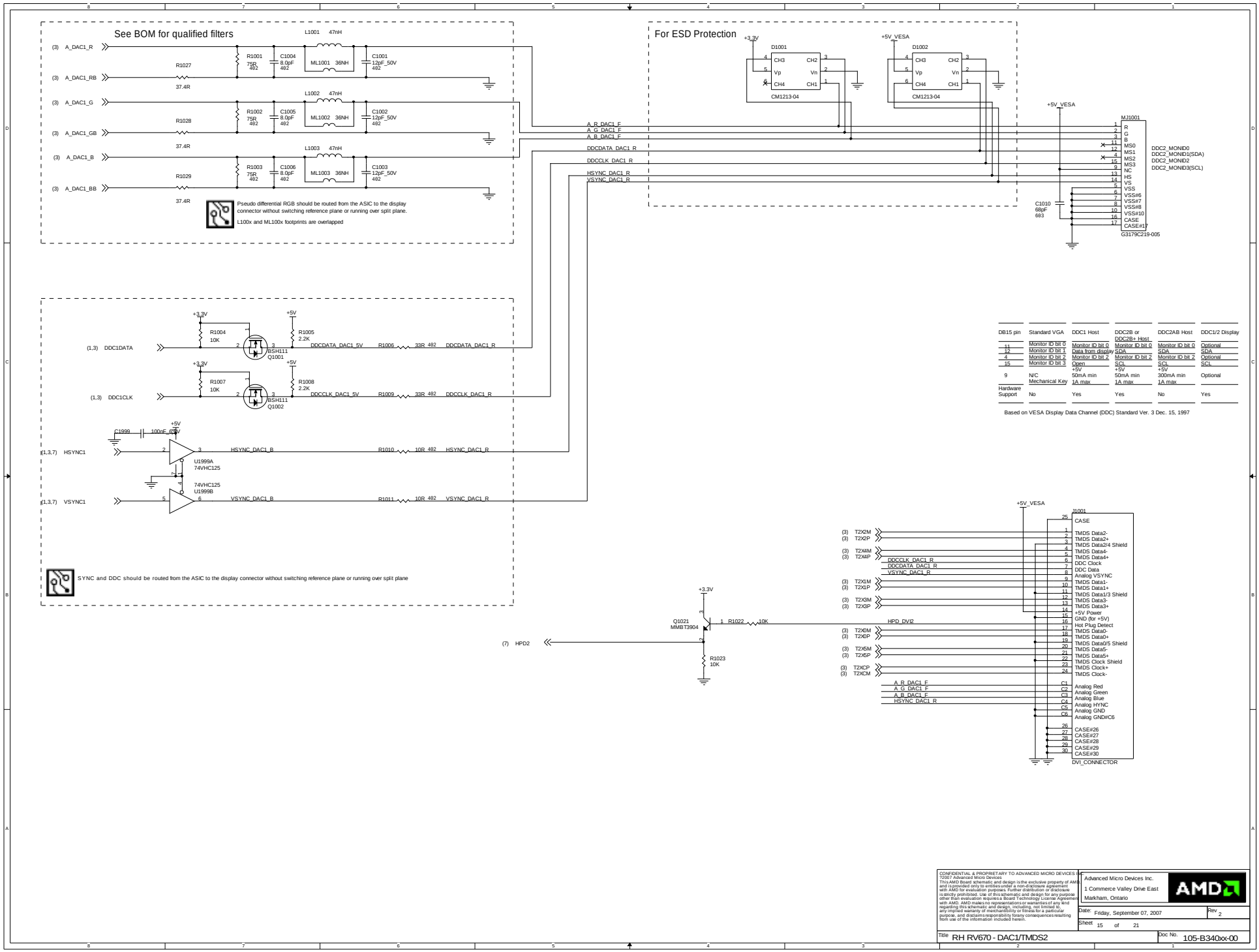
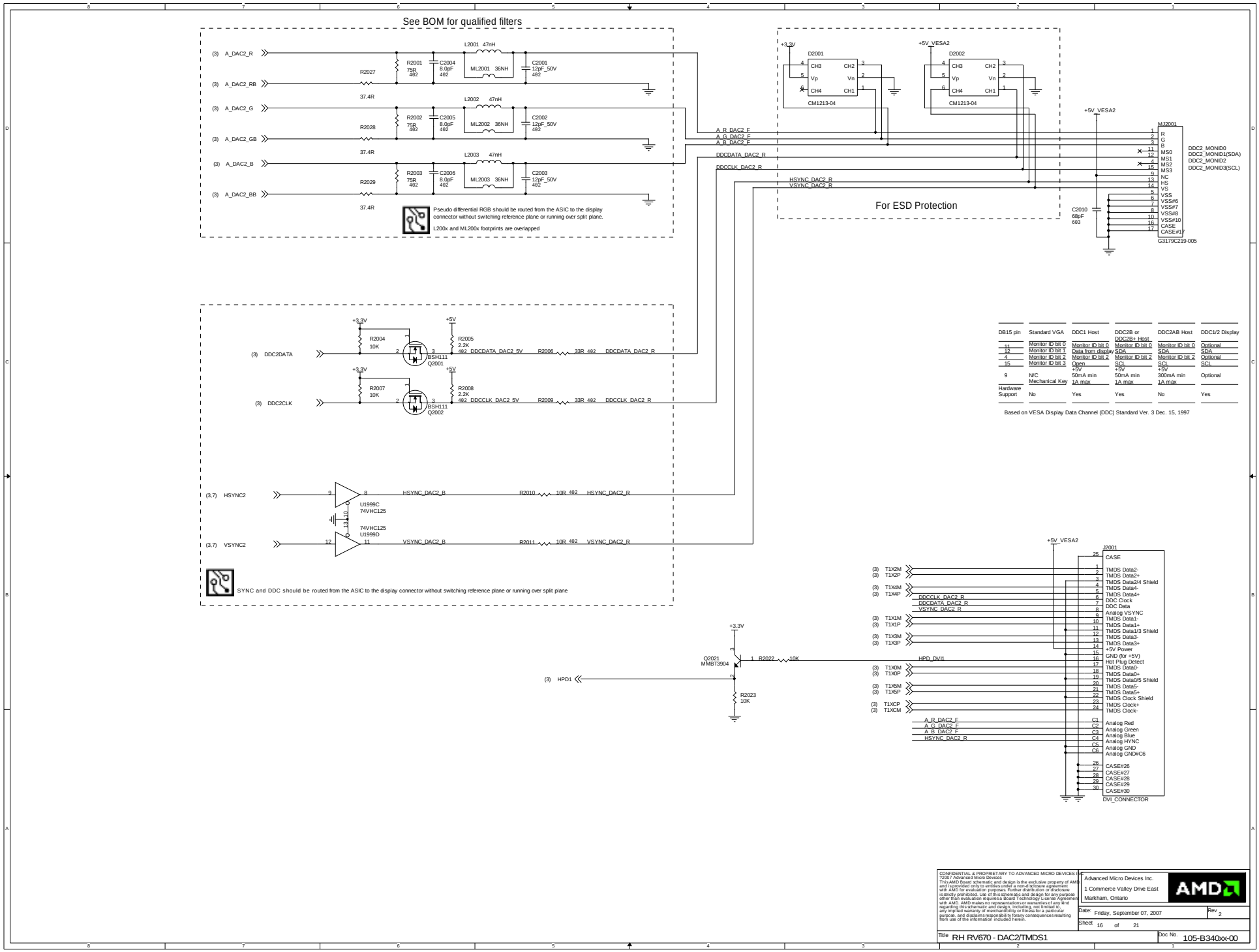
Date: Friday, September 07, 2007 Rev 2
Sheet 14 of 21
Title RH RV670 - Linear Regulators Doc No. 105-B340xx-00





DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C Mechanical Key	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	No	1A max	1A max	1A max	
		Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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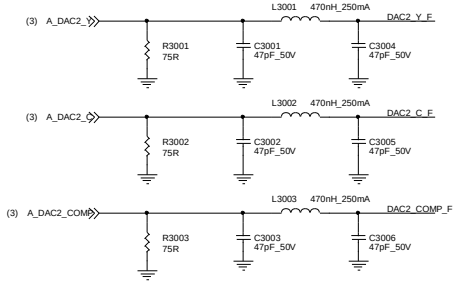
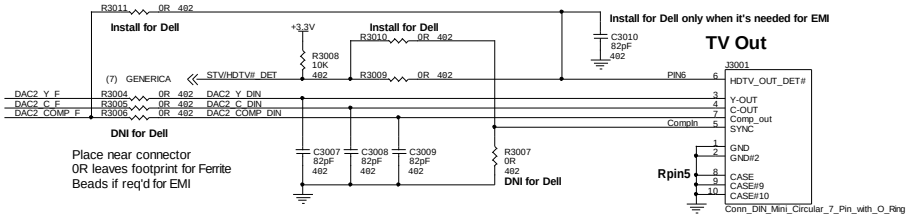
Date:	Friday, September 07, 2007
Rev	2
Sheet	16 of 21
Title	RH RV670 - DAC2/TMDS1
Doc No.	105-B340xx-00





- 4-pin Svideo MiniDIN P/N 6070001000G

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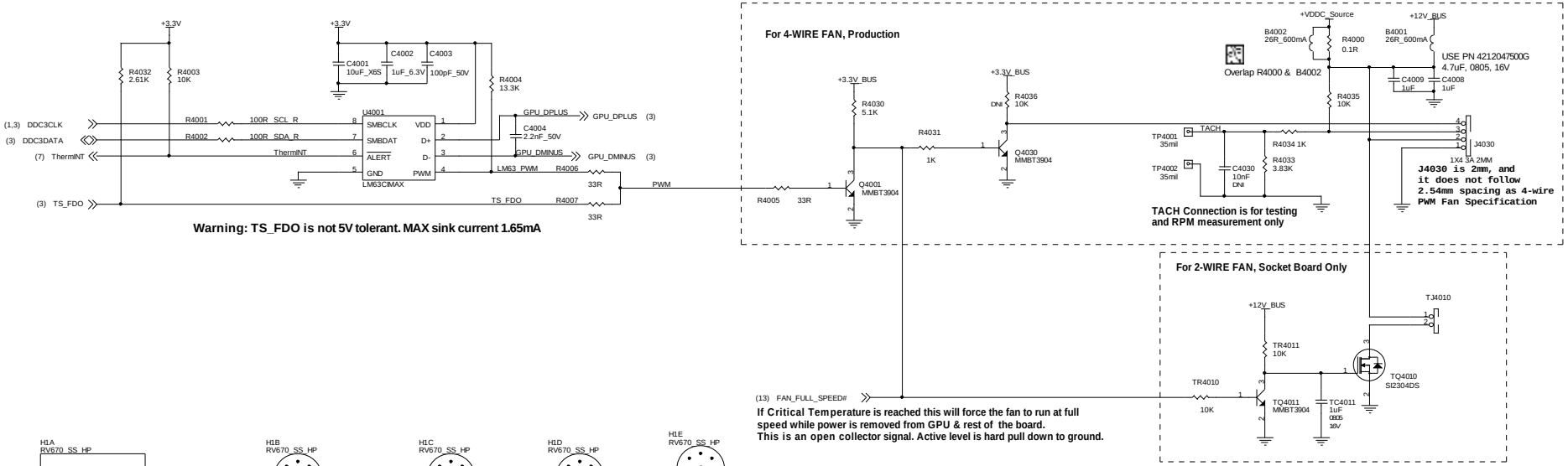
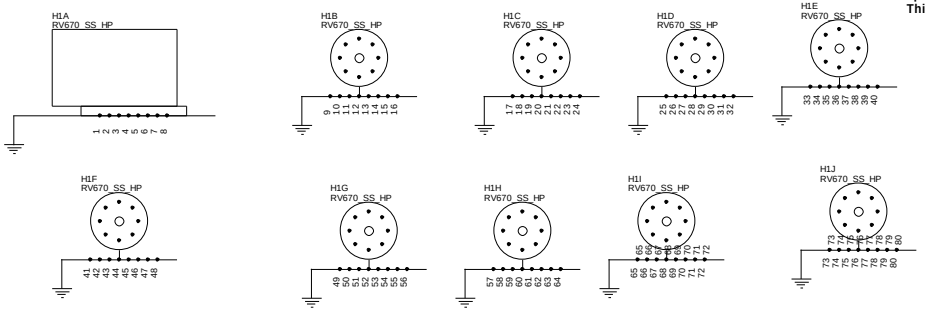
Date: Friday, September 07, 2007 Rev 2

Sheet 17 of 21

Title RH RV670 - TV OUT

Doc No. 105-B340xx-00





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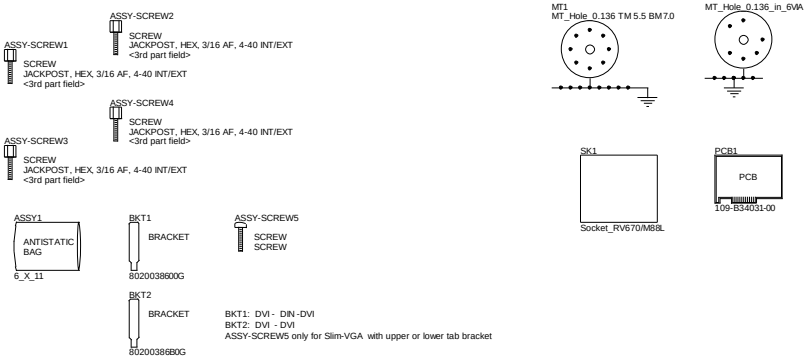
Date:	Friday, September 07, 2007
Rev	2
Sheet	18 of 21
Title	RH RV670 - Thermal Management
Doc No.	105-B340xx-00



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Date: Friday, September 07, 2007	Rev 2
Sheet 19 of 21	
Title: RH RV670 - Mechanical	Doc No. 105-B340xx-00

<Variant Name>

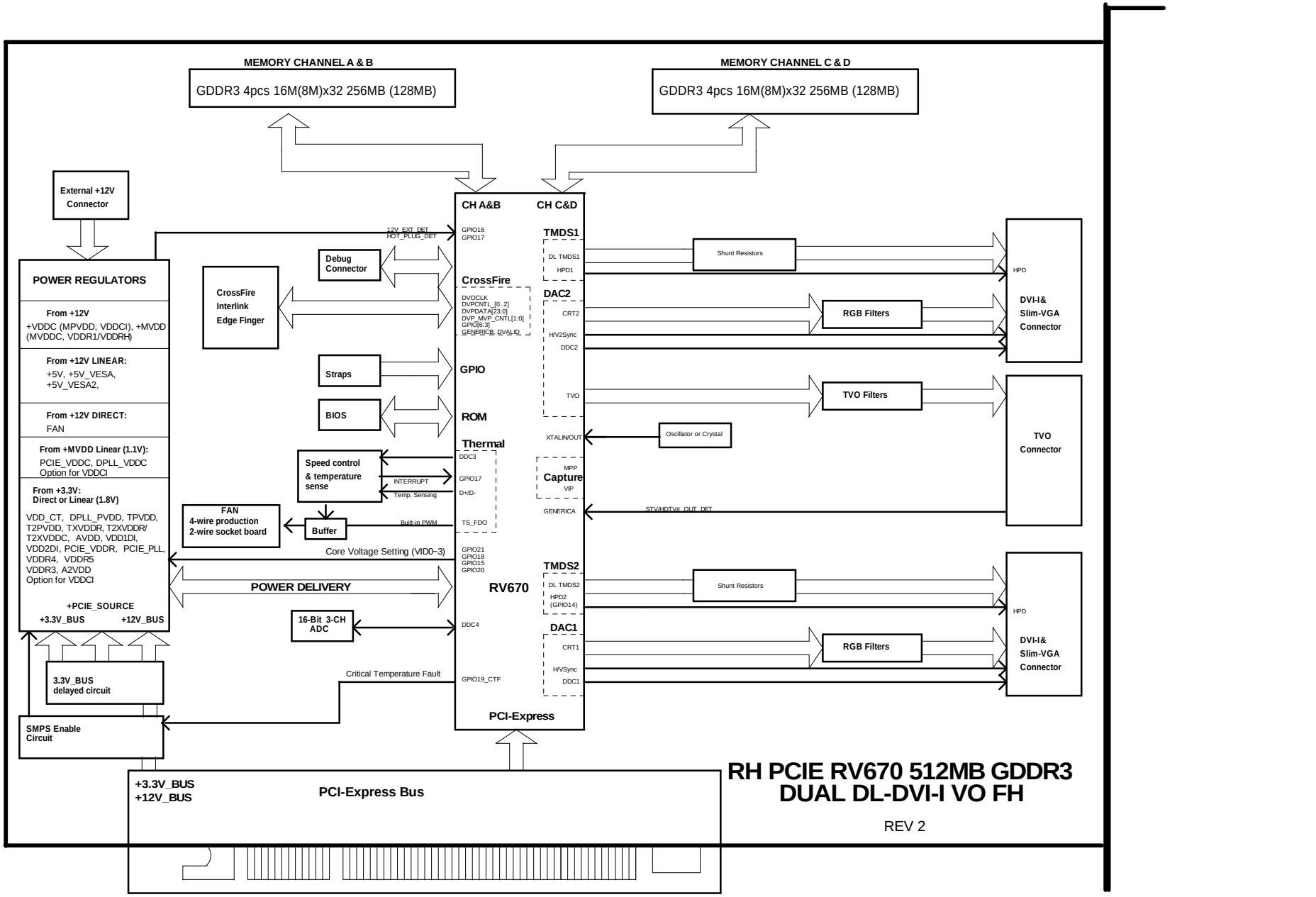
Title	Schematic No.	Date:
RH PCIE RV670 512MB GDDR3 DUAL DL-DVI-I VO FH	105-B340xx-00	Friday, September 07, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/05/11	Initial design for RV670 GDDR3 (Revival) based on B339
1	00B	07/08/1	(pg 1) Adding R1 and connecting switch #7 of TSW1. Some mother boards require B7 to be grounded. Table-1 updated accordingly (pg 7) Adding R64 and MR64 to select HOT_PLUG_DET or ThermINT as the interrupt source. (pg 13) Adding R1617, MR1617, R1616, Q1613, R1615, R1618, and R1619 as option to support hot plug detection of external cable. (pg 13) Adding R1282, MR1282, R1283, MR1283, R1284, MR1284, R1281, R1285, Q1280, and C1280 as option for thermal protection for VDDC SMPS MOSFETs (pg 13) Adding MC1603 (overlapped with C1603) (pg 14) Adding D870 as option for power up sequencing (pg 18) Adding heatsink symbol/footprint (Layout) Increasing spacing between DDC4DATA & DDC4CLK going to U1270 to reduce the crosstalk
2	00	07/09/06	(pg 16) Adding back C2001 (pg 13) Removing overlapped parts R1284, and MR1283 to address DFM (pg 13) Adding C1660, C1661, and C1662 to improve EMI (Layout) Fill in the gap between vias in +MVDD and +VDDC planes



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Date:	Friday, September 07, 2007
Rev	2
Sheet	21 of 21
Title	RH PCIE RV670 512MB GDDR3 DUAL DL-DVI-I VO FH
Doc No.	105-B340xx-00