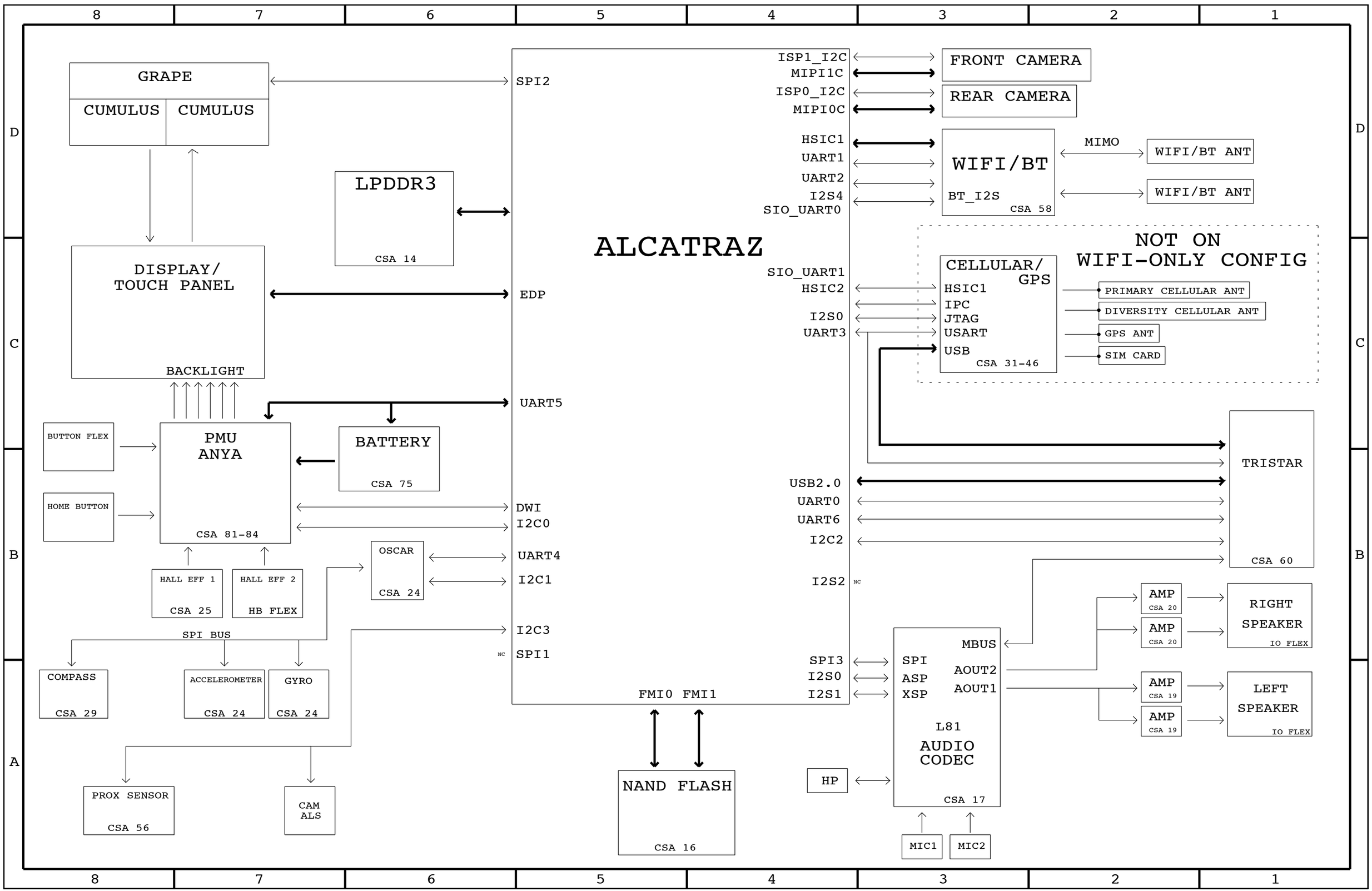
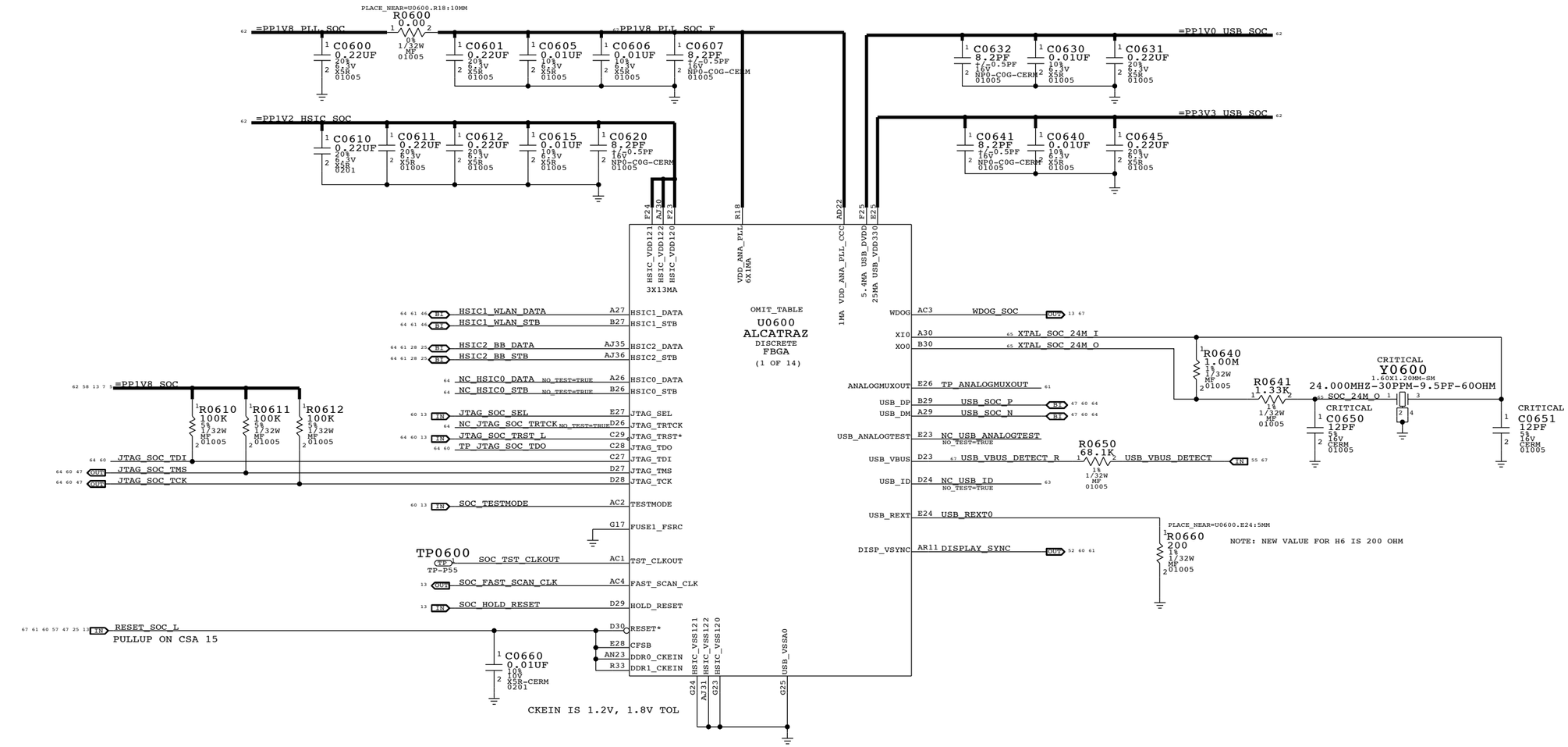
ipad air

DRAWING


GRAPE
CUMULUS
CUMULUS
LPDDR3
CSA 14
DISPLAY/
TOUCH PANEL
BACKLIGHT
BUTTON FLEX
PMU
ANYA
CSA 81-84
BATTERY
CSA 75
HOME BUTTON
HALL EFF 1
CSA 25
HALL EFF 2
HB FLEX
OSCAR
CSA 24
SPI BUS
COMPASS
CSA 29
ACCELEROMETER
CSA 24
GYRO
CSA 24
PROX SENSOR
CSA 56
CAM
ALS
SPI2
EDP
UART5
DWI
I2C0
UART4
I2C1
I2C3
NC
SPI1
ALCATRAZ
FMI0 FMI1
NAND FLASH
CSA 16
ISP1_I2C
MIPI1C
ISP0_I2C
MIPI0C
HSIC1
UART1
UART2
I2S4
SIO_UART0
SIO_UART1
HSIC2
I2S0
UART3
USB2.0
UART0
UART6
I2C2
I2S2
NC
SPI3
I2S0
I2S1
HP
FRONT CAMERA
REAR CAMERA
WIFI/BT
BT_I2S
CSA 58
MIMO
WIFI/BT ANT
WIFI/BT ANT
NOT ON
WIFI-ONLY CONFIG
CELLULAR/
GPS
HSIC1
IPC
JTAG
USART
USB
CSA 31-46
PRIMARY CELLULAR ANT
DIVERSITY CELLULAR ANT
GPS ANT
SIM CARD
TRISTAR
CSA 60
SPI
ASP
XSP
MBUS
AOUT2
AOUT1
L81
AUDIO
CODEC
CSA 17
MIC1
MIC2
AMP
CSA 20
AMP
CSA 20
RIGHT
SPEAKER
IO FLEX
AMP
CSA 19
AMP
CSA 19
LEFT
SPEAKER
IO FLEX


PLACE_NEAR=U0600.R18:10MM
R0600 0.00 0% 1/32W MF 01005
=PP1V8_PLL_SOC
=PP1V8_PLL_SOC_F
C0600 0.22UF 20% 6.3V X5R 01005
C0601 0.22UF 20% 6.3V X5R 01005
C0605 0.01UF 10% 6.3V X5R 01005
C0606 0.01UF 10% 6.3V X5R 01005
C0607 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
=PP1V0_USB_SOC
C0632 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
C0630 0.01UF 10% 6.3V X5R 01005
C0631 0.22UF 20% 6.3V X5R 01005
=PP1V2_HSIC_SOC
C0610 0.22UF 20% 6.3V X5R 0201
C0611 0.22UF 20% 6.3V X5R 01005
C0612 0.22UF 20% 6.3V X5R 01005
C0615 0.01UF 10% 6.3V X5R 01005
C0620 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
=PP3V3_USB_SOC
C0641 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
C0640 0.01UF 10% 6.3V X5R 01005
C0645 0.22UF 20% 6.3V X5R 01005
HSIC_VDD121
HSIC_VDD122
HSIC_VDD120
3X13MA
VDD_ANA_PLL
6X1MA
VDD_ANA_PLL_CCC
1MA
USB_DVDD
5.4MA
USB_VDD330
25MA
OMIT_TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(1 OF 14)
HSIC1_WLAN_DATA
HSIC1_WLAN_STB
HSIC1_DATA
HSIC1_STB
HSIC2_BB_DATA
HSIC2_BB_STB
HSIC2_DATA
HSIC2_STB
NC_HSIC0_DATA
NC_HSIC0_STB
HSIC0_DATA
HSIC0_STB
JTAG_SOC_SEL
NC_JTAG_SOC_TRTCK
JTAG_SOC_TRST_L
TP_JTAG_SOC_TDO
JTAG_SEL
JTAG_TRTCK
JTAG_TRST*
JTAG_TDO
JTAG_TDI
JTAG_TMS
JTAG_TCK
SOC_TESTMODE
TESTMODE
FUSE1_FSRC
TP0600
TP-P55
SOC_TST_CLKOUT
TST_CLKOUT
SOC_FAST_SCAN_CLK
FAST_SCAN_CLK
SOC_HOLD_RESET
HOLD_RESET
RESET_SOC_L
PULLUP ON CSA 15
RESET*
CFSB
DDR0_CKEIN
DDR1_CKEIN
C0660 0.01UF 10% 16V X5R-CERM 0201
CKEIN IS 1.2V, 1.8V TOL
HSIC_VSS121
HSIC_VSS122
HSIC_VSS120
USB_VSSA0
WDOG_SOC
XTAL_SOC_24M_I
XTAL_SOC_24M_O
R0640 1.00M 1% 1/32W MF 01005
R0641 1.33K 1% 1/32W MF 01005
CRITICAL
Y0600
1.6X1.2MM-SM
24.000MHZ-30PPM-9.5PF-60OHM
C0650 12PF 5% 16V CERM 01005
C0651 12PF 5% 16V CERM 01005
TP_ANALOGMUXOUT
USB_SOC_P
USB_SOC_N
NC_USB_ANALOGTEST
USB_VBUS_DETECT_R
USB_VBUS_DETECT
R0650 68.1K 1% 1/32W MF 01005
NC_USB_ID
USB_REXT0
R0660 200 1% 1/32W MF 01005
PLACE_NEAR=U0600.E24:5MM
NOTE: NEW VALUE FOR H6 IS 200 OHM
DISPLAY_SYNC

I2S0 AND I2S2 ARE OPTIMIZED FOR LOW MCK JITTER

R0700 33 1/32W MF 01005

L81 CODEC ASP 1.8V

L81 CODEC XSP 1.8V

UNUSED 1.8V

BT 1.8V

OMIT_TABLE

U0600 ALCATRAZ DISCRETE FBGA (3 OF 14)

I2S0_CODEC_ASP_MCK_R	I2S0_MCK	F28	
I2S0_CODEC_ASP_MCK	I2S0_MCK	F28	
I2S0_CODEC_ASP_BCLK	I2S0_BCLK	AJ32	
I2S0_CODEC_ASP_LRCK	I2S0_LRCK	AH32	
I2S0_CODEC_ASP_DIN	I2S0_DIN	AG32	
I2S0_CODEC_ASP_DOUT	I2S0_DOUT	AJ33	
NC_I2S1_MCK NO_TEST=TRUE	I2S1_MCK	AG33	
I2S1_CODEC_XSP_BCLK	I2S1_BCLK	AH34	
I2S1_CODEC_XSP_LRCK	I2S1_LRCK	AH33	
I2S1_CODEC_XSP_DIN	I2S1_DIN	AG34	
I2S1_CODEC_XSP_DOUT	I2S1_DOUT	AF32	
NC_I2S2_MCK NO_TEST=TRUE	I2S2_MCK	F26	
NC_I2S2_BCLK NO_TEST=TRUE	I2S2_BCLK	AG35	
NC_I2S2_LRCK NO_TEST=TRUE	I2S2_LRCK	AE32	
NC_I2S2_DIN NO_TEST=TRUE	I2S2_DIN	AE33	
NC_I2S2_DOUT NO_TEST=TRUE	I2S2_DOUT	AF34	
BB_JTAG_TRST_L	I2S3_MCK	AD32	
BB_JTAG_TDI	I2S3_BCLK	AF36	
BB_JTAG_TDO	I2S3_LRCK	AG36	
BB_JTAG_TCK	I2S3_DIN	AC32	
BB_JTAG_TMS	I2S3_DOUT	AD33	
NC_I2S4_MCK NO_TEST=TRUE	I2S4_MCK	AD34	
I2S4_SOC2BT_BCLK	I2S4_BCLK	AE36	
I2S4_SOC2BT_LRCK	I2S4_LRCK	AE35	
I2S4_BT2SOC_DATA	I2S4_DIN	AB32	
I2S4_SOC2BT_DATA	I2S4_DOUT	AC33	
GPIO_BOARD_ID_2	SPI0_MISO	AN4	
GPIO_BOARD_ID_1	SPI0_MOSI	AP2	
GPIO_BOARD_ID_0	SPI0_SCLK	AN3	
NC_SPI0_SSIN NO_TEST=TRUE	SPI0_SSIN	AM9	
NC_SPI1_MISO NO_TEST=TRUE	SPI1_MISO	AN1	
NC_SPI1_MOSI NO_TEST=TRUE	SPI1_MOSI	AM4	
NC_SPI1_SCLK NO_TEST=TRUE	SPI1_SCLK	AM5	
NC_SPI1_SSIN NO_TEST=TRUE	SPI1_SSIN	AM7	
SPI2_GRAPE_MISO	SPI2_MISO	AN8	
SPI2_GRAPE_MOSI	SPI2_MOSI	AN7	
SPI2_GRAPE_SCLK	SPI2_SCLK	AN5	
SPI2_GRAPE_CS_L	SPI2_SSIN	AN9	
SPI3_CODEC_MISO	SPI3_MISO	AN13	
SPI3_CODEC_MOSI	SPI3_MOSI	AT6	
SPI3_CODEC_SCLK	SPI3_SCLK	AR7	
SPI3_CODEC_CS_L	SPI3_SSIN	AP10	

I2C0_SCL	I2C0_SCL_1V8	AN6	
I2C0_SDA	I2C0_SDA_1V8	AP4	
I2C1_SCL	I2C1_SOC2OSCAR_SWDCLK_1V8	AP5	
I2C1_SDA	I2C1_SOC2OSCAR_SWDIO_1V8	AR3	
I2C2_SCL	I2C2_SCL_1V8	AR14	
I2C2_SDA	I2C2_SDA_1V8	AT7	
I2C3_SCL	I2C3_SCL_1V8	AA35	
I2C3_SDA	I2C3_SDA_1V8	AA36	
DWI_CLK	DWI_AP_CLK	AT17	
DWI_DI	SOC_TST_CPUSWITCH_OUT	AT16	
DWI_DO	DWI_AP_DO	AR16	
SEP_7816UART0_RST	NC_SEP_7816UART0_RST NO_TEST=TRUE	AL1	
SEP_7816UART0_SCL	SEP_I2C0_SCL	AK5	
SEP_7816UART0_SDA	SEP_I2C0_SDA	AK3	
SEP_7816UART1_RST	NC_SEP_7816UART1_RST NO_TEST=TRUE	AM1	
SEP_7816UART1_SCL	NC_SEP_7816UART1_SCL NO_TEST=TRUE	AL4	
SEP_7816UART1_SDA	NC_SEP_7816UART1_SDA NO_TEST=TRUE	AL2	
SIO_7816UART0_RST	HSIC1_WLAN2SOC_REMOTE_WAKE	Y32	
SIO_7816UART0_SCL	HSIC1_WLAN2SOC_DEVICE_RDY	AB33	
SIO_7816UART0_SDA	HSIC1_SOC2WLAN_HOST_RDY	AA32	
SIO_7816UART1_RST	HSIC2_BB2SOC_REMOTE_WAKE	AA34	
SIO_7816UART1_SCL	HSIC2_BB2SOC_DEVICE_RDY	AC36	
SIO_7816UART1_SDA	HSIC2_SOC2BB_HOST_RDY	AA33	
SOCHOT0	SOCHOT0_L	AM20	
SOCHOT1	SOCHOT1_L	AM19	

TO: ANYA PMU 0111100X

TO: OSCAR SWD
NOTE: I2C1 IS ASSUMED TO USE PUSH-PULL INSTEAD OF OPEN-DRAIN

TO: TRISTAR 0011010X

TO: AD7149 PROX 0101101X
FF CAM CT817 ALS 0111001X

TP0700 TP-P55

OMIT_TABLE

U0600 ALCATRAZ DISCRETE FBGA (2 OF 14)

GPIO_BTN_HOME_L	GPIO0	AB6
GPIO_BTN_ONOFF_L	GPIO1	AD1
GPIO_BTN_VOL_DOWN_L	GPIO2	AB5
GPIO_BTN_VOL_UP_L	GPIO3	AC5
GPIO_CAM_ALS2SOC_IRQ_L	GPIO4	AC6
GPIO_BT_WAKE	GPIO5	AD3
GPIO_SOC2BB_WAKE_MODEM	GPIO6	AD4
NC_GPIO7 NO_TEST=TRUE	GPIO7	AE1
GPIO_SOC2BB_RST_L	GPIO8	AE2
GPIO_SOC2BB_RADIO_ON_L	GPIO9	AD5
GPIO_BB2SOC_RESET_DET_L	GPIO10	AF1
NC_GPIO11 NO_TEST=TRUE	GPIO11	AF2
GPIO_SOC2OSCAR_DBGEN	GPIO12	AE4
GPIO_SOC2GRAPE_RESET_L	GPIO13	AF3
NC_GPIO14 NO_TEST=TRUE	GPIO14	AE5
GPIO_BB2SOC_GSM_TXBURST	GPIO15	AE6
GPIO_BOARD_ID_3	GPIO16	AG1
GPIO_TS2SOC2PMU_INT	GPIO17	AF4
GPIO_BOOT_CONFIG_0	GPIO18	AG3
GPIO_BB2SOC_GPS_SYNC	GPIO19	AF5
GPIO_PROX2SOC_IRQ_L	GPIO20	AH1
GPIO_SOC2LCD_PWREN	GPIO21	AG4
GPIO_SOC2PMU_KEEPACT	GPIO22	AR10
GPIO_PMU2SOC_IRQ_L	GPIO23	AN14
GPIO_CODEC2SOC_IRQ_L	GPIO24	AR9
GPIO_BOOT_CONFIG_1	GPIO25	AP13
GPIO_FORCE_DFU	GPIO26	AT14
TP_GPIO_DFU_STATUS	GPIO27	AT8
GPIO_BOOT_CONFIG_2	GPIO28	AM17
GPIO_BOOT_CONFIG_3	GPIO29	AT9
GPIO_BTN_SRL_L	GPIO30	AP14
GPIO_GRAPE2SOC_IRQ_L	GPIO31	AN16
NC_GPIO32 NO_TEST=TRUE	GPIO32	AT11
GPIO_HS3_SHUNT_EN	GPIO33	AT10
GPIO_HS4_SHUNT_EN	GPIO34	AP11
GPIO_BRD_REV3	GPIO35	AN17
GPIO_BRD_REV2	GPIO36	AR13
GPIO_BRD_REV1	GPIO37	AP16
GPIO_BRD_REV0	GPIO38	AT13

TMR32_PWM0	OSCAR_TIME_SYNC_HOST_INT	AD35	
TMR32_PWM1	NC_TMR32_PWM1 NO_TEST=TRUE	AC34	
TMR32_PWM2	CLK_32K_SOC2CUMULUS	AD36	
UART0_RXD	UART0_SOC_RXD	AR17	SOC DEBUG 1.8V
UART0_TXD	UART0_SOC_TXD	AP17	
UART1_CTSN	UART1_BT2SOC_RTS_L	AH4	TO BT UART BCM4330
UART1_RTSN	UART1_SOC2BT_RTS_L	AH2	
UART1_RXD	UART1_BT2SOC_TX	AG6	
UART1_TXD	UART1_SOC2BT_TX	AG5	
UART2_CTSN	NC_GPIO_UART2_CTSN NO_TEST=TRUE	AJ3	
UART2_RTSN	NC_GPIO_UART2_RTSN NO_TEST=TRUE	AH5	
UART2_RXD	UART2_WLAN2SOC_TX	AJ2	WIFI DEBUG
UART2_TXD	UART2_SOC2WLAN_TX	AJ1	
UART3_CTSN	UART3_BB2SOC_RTS_L	AK1	TO BB UART MDM9600
UART3_RTSN	UART3_SOC2BB_RTS_L	AJ6	
UART3_RXD	UART3_BB2SOC_TX	AJ5	
UART3_TXD	UART3_SOC2BB_TX	AJ4	
UART4_CTSN	PMU_GPIO_OSCAR2PMU_HOST_WAKE	AM3	TO OSCAR
UART4_RTSN	GPIO_OSCAR_RESET_L	AM2	
UART4_RXD	UART4_OSCAR2SOC_RXD	AL5	
UART4_TXD	UART4_SOC2OSCAR_TXD	AL6	
UART5_RTXD	UART5_BATT_TRXD	AK4	
UART6_RXD	UART6_TS_ACC_RXD	AB36	ACCESSORY UART 1.8V
UART6_TXD	UART6_TS_ACC_TXD	AB35	

BUTTON PULLUPS

=PP1V8_ALWAYS
=PP1V8_S2R_MISC

R0722 100K 5% 1/32W MF 01005
R0720 100K 5% 1/32W MF 01005
NOSTUFF R0723 100K 5% 1/32W MF 01005
R0721 100K 5% 1/32W MF 01005

GPIO_BTN_SRL_L
GPIO_BTN_HOME_L
GPIO_BTN_ONOFF_L

=PP1V8_S2R_MISC
=PP1V8_SOC

R0760 100K 5% 1/32W MF 01005
R0761 100K 5% 1/32W MF 01005

SOCHOT1_L
SOCHOT0_L

SEP EEPROM

UNPROGRAMMED P/N: 335S0894

=PP1V8_EEPROM
C9000 0.22UF 20% 6.3V X5R 01005

U9000 CAT24C08C4A WLCSP
CRITICAL
VCC A1
SCL B1
SDA B2
VSS A2

SEP_I2C0_SCL
SEP_I2C0_SDA

R0730 100K 5% 1/32W MF 01005
R0731 100K 5% 1/20W MF 201
NOSTUFF R0733 100K 5% 1/32W MF 01005
R0734 100K 5% 1/32W MF 01005

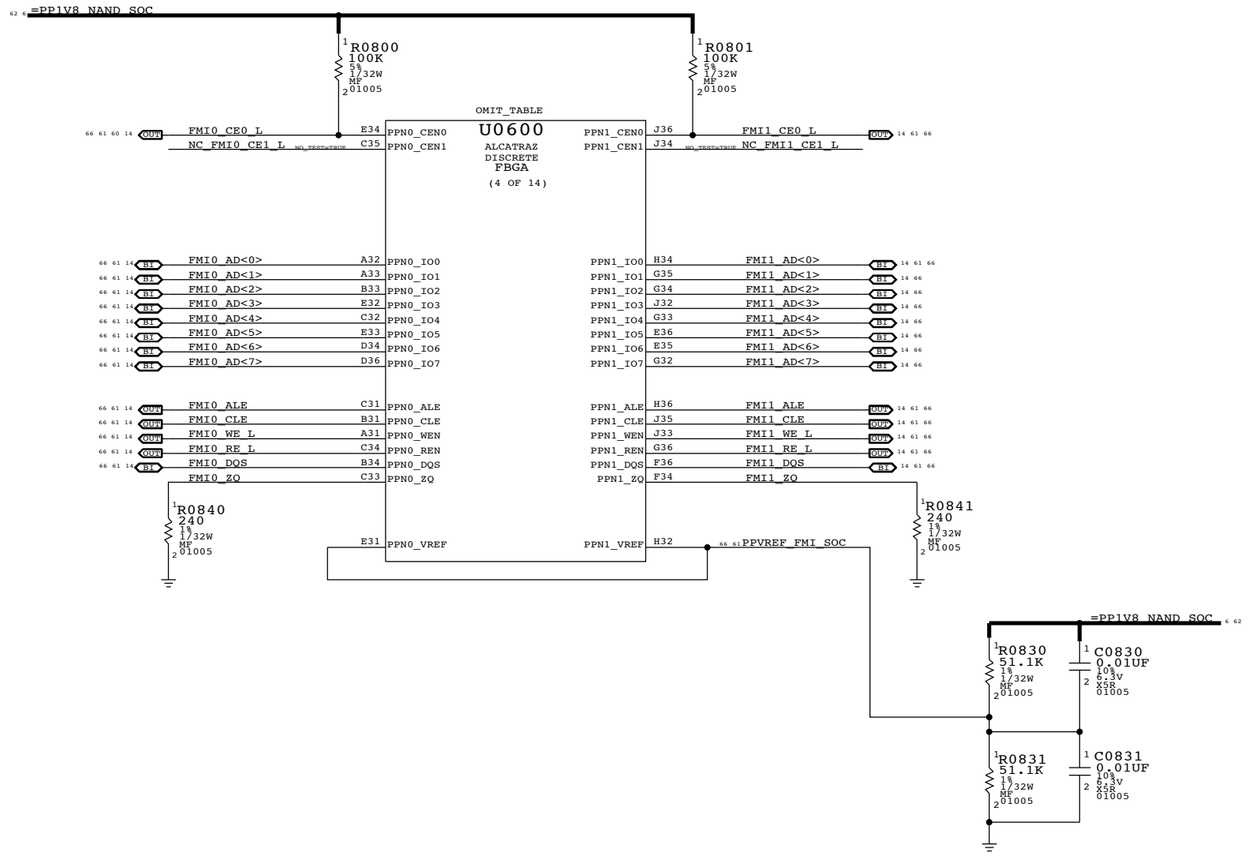
GPIO_SOC2PMU_KEEPACT
GPIO_FORCE_DFU
GPIO_SOC2BB_RADIO_ON_L
HSIC1_SOC2WLAN_HOST_RDY

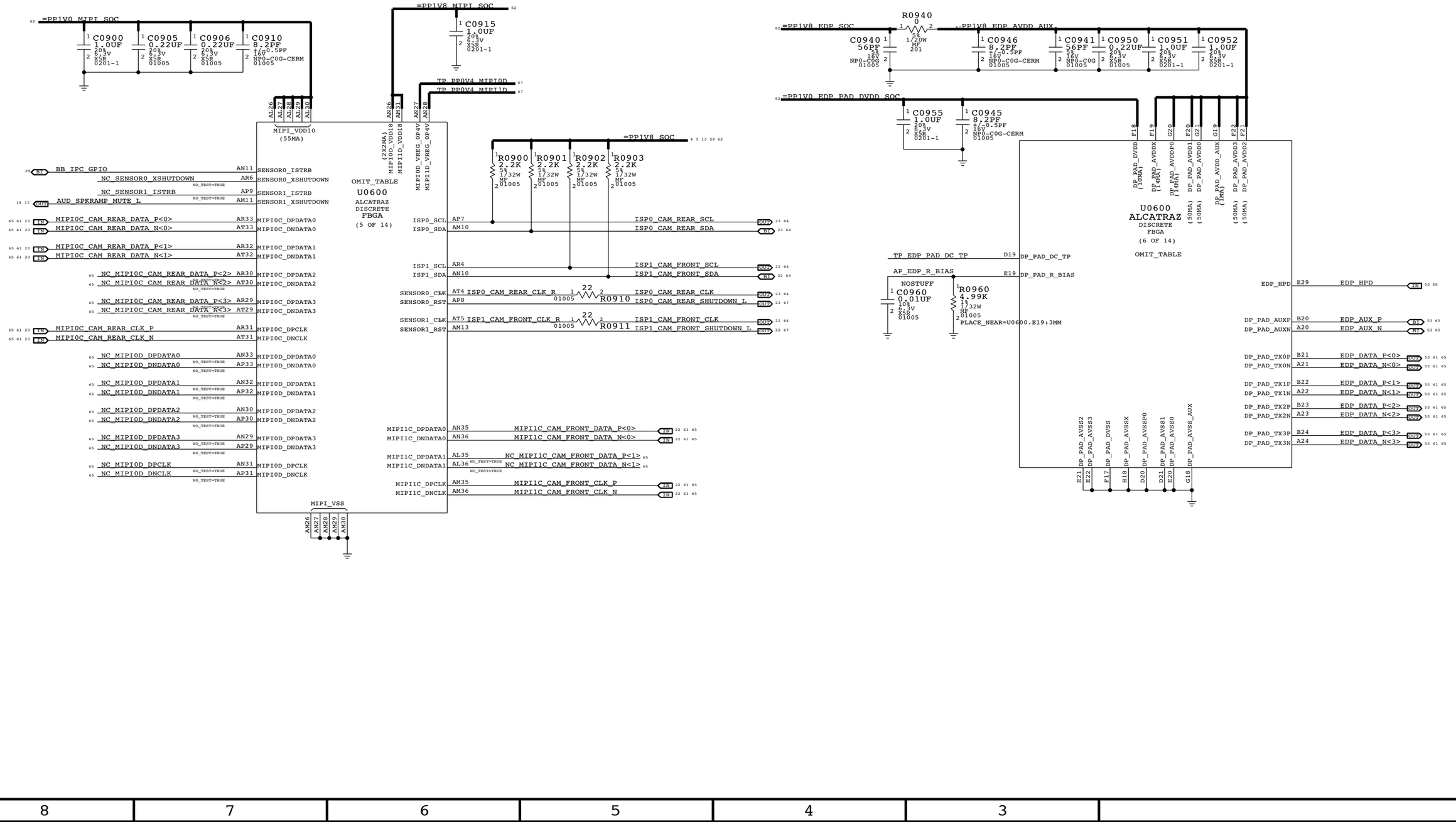
I2C PULL-UPS

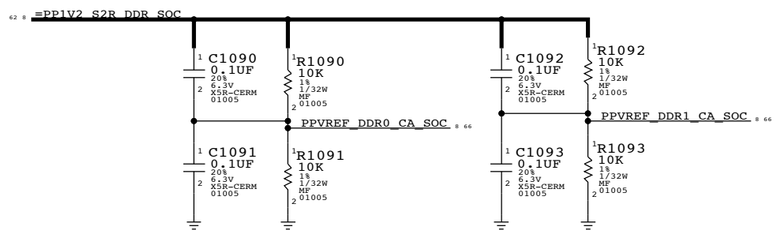
=PP1V8_SOC

R0750 2.2K 5% 1/32W MF 01005
R0751 2.2K 5% 1/32W MF 01005
R0752 2.2K 5% 1/32W MF 01005
R0753 2.2K 5% 1/32W MF 01005
R0754 2.2K 5% 1/32W MF 01005
R0755 2.2K 5% 1/32W MF 01005
R0756 2.2K 5% 1/32W MF 01005
R0757 2.2K 5% 1/32W MF 01005
NOSTUFF R0758 2.2K 5% 1/32W MF 01005
NOSTUFF R0759 2.2K 5% 1/32W MF 01005

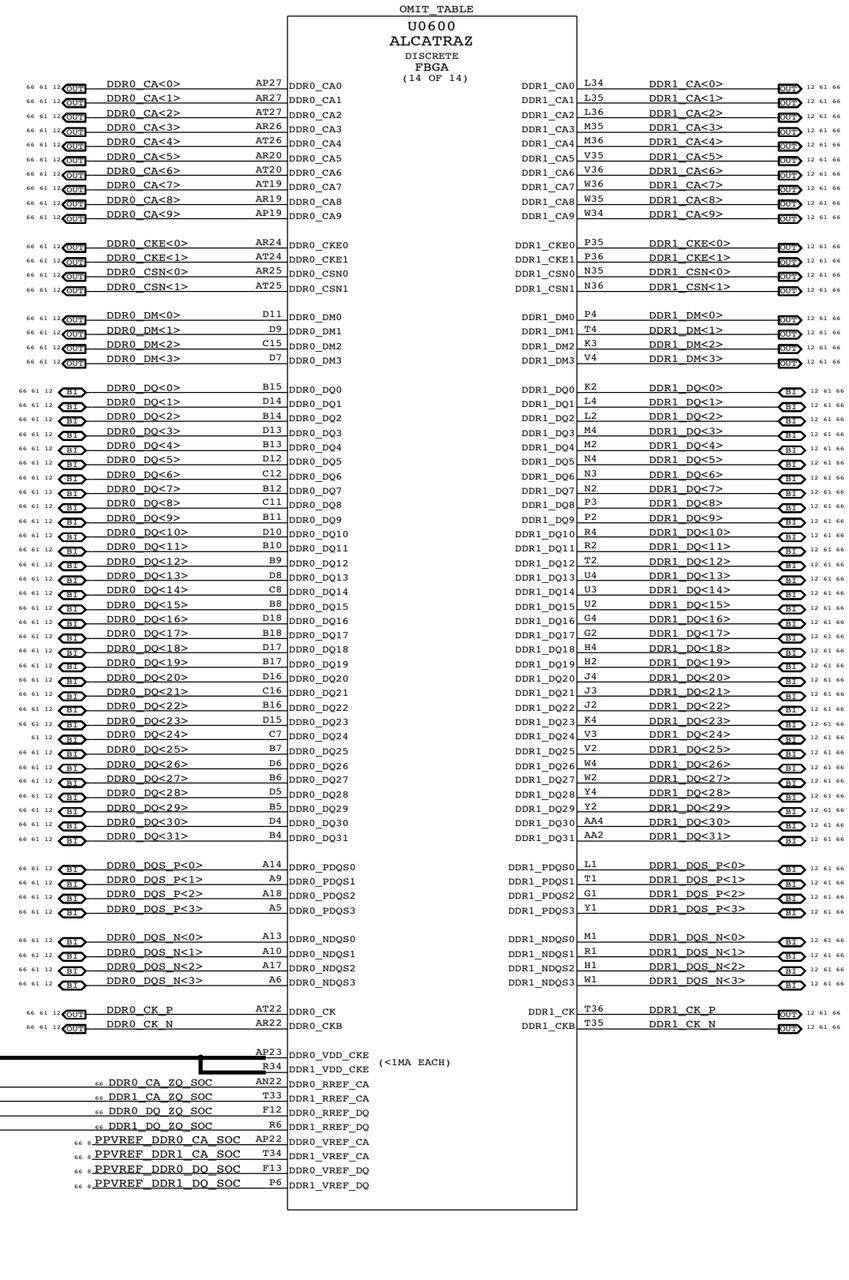
I2C0_SDA_1V8
I2C0_SCL_1V8
I2C3_SDA_1V8
I2C3_SCL_1V8
I2C2_SDA_1V8
I2C2_SCL_1V8
SEP_I2C0_SDA
SEP_I2C0_SCL
I2C1_SOC2OSCAR_SWDCLK_1V8
I2C1_SOC2OSCAR_SWDIO_1V8

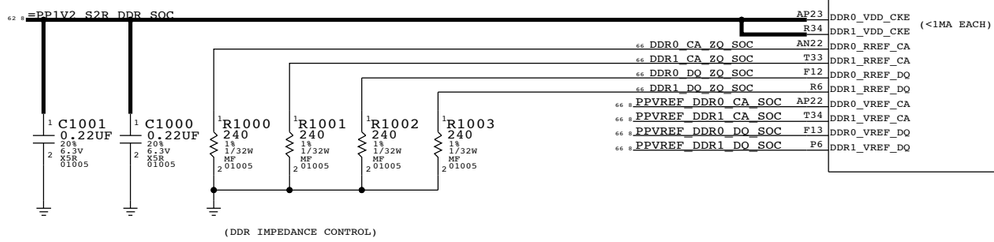

=PP1V8_NAND_SOC
R0800
100K
1%
1/32W
MF
01005
R0801
100K
1%
1/32W
MF
01005
OMIT_TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(4 OF 14)
FMI0_CE0_L
NC_FMI0_CE1_L
FMI1_CE0_L
NC_FMI1_CE1_L
PPN0_CEN0
PPN0_CEN1
PPN1_CEN0
PPN1_CEN1
FMI0_AD<0>
FMI0_AD<1>
FMI0_AD<2>
FMI0_AD<3>
FMI0_AD<4>
FMI0_AD<5>
FMI0_AD<6>
FMI0_AD<7>
FMI1_AD<0>
FMI1_AD<1>
FMI1_AD<2>
FMI1_AD<3>
FMI1_AD<4>
FMI1_AD<5>
FMI1_AD<6>
FMI1_AD<7>
FMI0_ALE
FMI0_CLE
FMI0_WE_L
FMI0_RE_L
FMI0_DQS
FMI0_ZQ
FMI1_ALE
FMI1_CLE
FMI1_WE_L
FMI1_RE_L
FMI1_DQS
FMI1_ZQ
R0840
240
1%
1/32W
MF
01005
R0841
240
1%
1/32W
MF
01005
PPVREF_FMI_SOC
=PP1V8_NAND_SOC
R0830
51.1K
1%
1/32W
MF
01005
C0830
0.01UF
10%
6.3V
X5R
01005
R0831
51.1K
1%
1/32W
MF
01005
C0831
0.01UF
10%
6.3V
X5R
01005

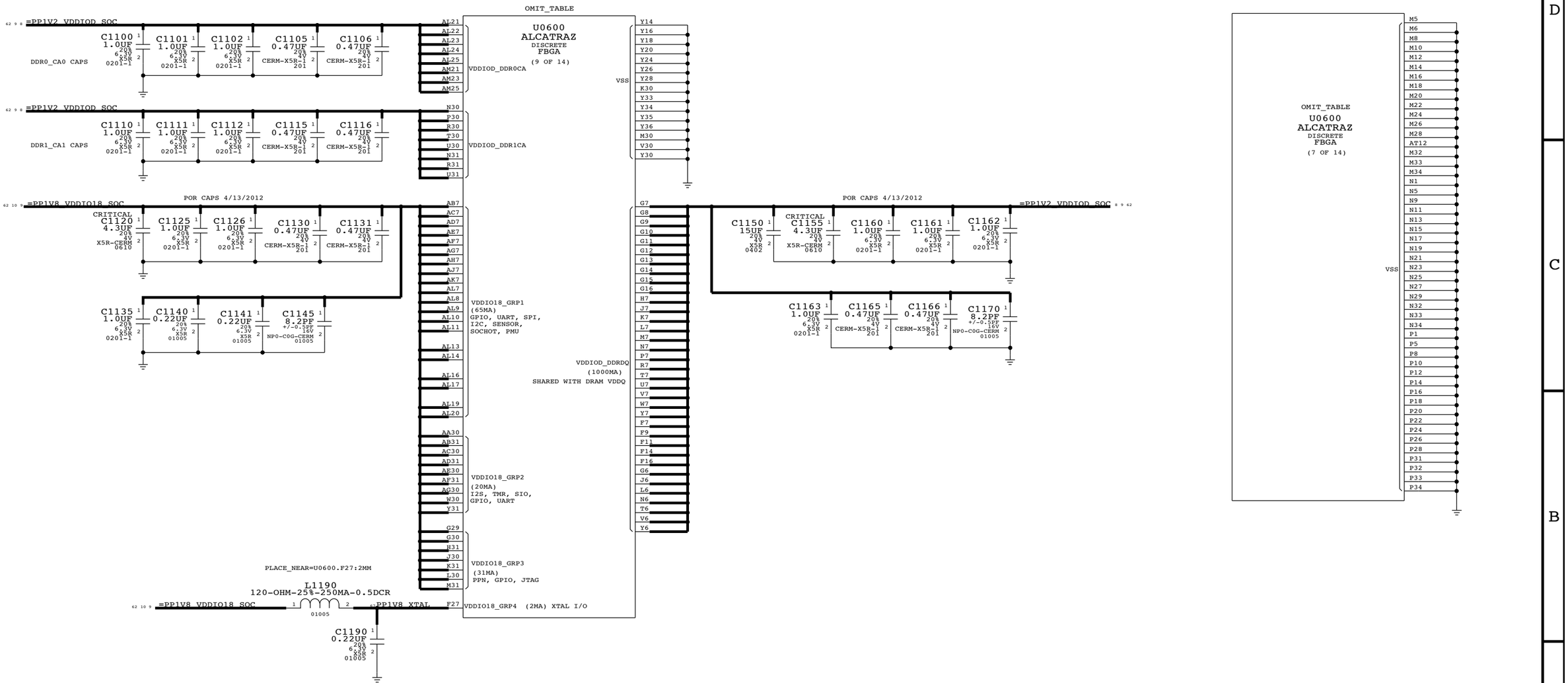

=PP1V0_MIPI_SOC
C0900 1.0UF 20% 6.3V X5R 0201-1
C0905 0.22UF 20% 6.3V X5R 01005
C0906 0.22UF 20% 6.3V X5R 01005
C0910 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
=PP1V8_MIPI_SOC
C0915 1.0UF 20% 6.3V X5R 0201-1
TP_PP0V4_MIPI0D
TP_PP0V4_MIPI1D
MIPI_VDD10 (55MA)
(2X2MA)
MIPI0D_VDD18
MIPI1D_VDD18
MIPI0D_VREG_0P4V
MIPI1D_VREG_0P4V
=PP1V8_SOC
R0900 2.2K 5% 1/32W MF 01005
R0901 2.2K 5% 1/32W MF 01005
R0902 2.2K 5% 1/32W MF 01005
R0903 2.2K 5% 1/32W MF 01005
OMIT_TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(5 OF 14)
BB_IPC_GPIO
NC_SENSOR0_XSHUTDOWN
NC_SENSOR1_ISTRB
AUD_SPKRAMP_MUTE_L
SENSOR0_ISTRB
SENSOR0_XSHUTDOWN
SENSOR1_ISTRB
SENSOR1_XSHUTDOWN
MIPI0C_CAM_REAR_DATA_P<0>
MIPI0C_CAM_REAR_DATA_N<0>
MIPI0C_CAM_REAR_DATA_P<1>
MIPI0C_CAM_REAR_DATA_N<1>
NC_MIPI0C_CAM_REAR_DATA_P<2>
NC_MIPI0C_CAM_REAR_DATA_N<2>
NC_MIPI0C_CAM_REAR_DATA_P<3>
NC_MIPI0C_CAM_REAR_DATA_N<3>
MIPI0C_CAM_REAR_CLK_P
MIPI0C_CAM_REAR_CLK_N
NC_MIPI0D_DPDATA0
NC_MIPI0D_DNDATA0
NC_MIPI0D_DPDATA1
NC_MIPI0D_DNDATA1
NC_MIPI0D_DPDATA2
NC_MIPI0D_DNDATA2
NC_MIPI0D_DPDATA3
NC_MIPI0D_DNDATA3
NC_MIPI0D_DPCLK
NC_MIPI0D_DNCLK
NO_TEST=TRUE
ISP0_SCL
ISP0_SDA
ISP1_SCL
ISP1_SDA
SENSOR0_CLK
SENSOR0_RST
SENSOR1_CLK
SENSOR1_RST
ISP0_CAM_REAR_CLK_R
R0910 22 01005
ISP0_CAM_REAR_SCL
ISP0_CAM_REAR_SDA
ISP1_CAM_FRONT_SCL
ISP1_CAM_FRONT_SDA
ISP0_CAM_REAR_CLK
ISP0_CAM_REAR_SHUTDOWN_L
ISP1_CAM_FRONT_CLK_R
R0911 22 01005
ISP1_CAM_FRONT_CLK
ISP1_CAM_FRONT_SHUTDOWN_L
MIPI1C_DPDATA0
MIPI1C_DNDATA0
MIPI1C_DPDATA1
MIPI1C_DNDATA1
MIPI1C_DPCLK
MIPI1C_DNCLK
MIPI1C_CAM_FRONT_DATA_P<0>
MIPI1C_CAM_FRONT_DATA_N<0>
NC_MIPI1C_CAM_FRONT_DATA_P<1>
NC_MIPI1C_CAM_FRONT_DATA_N<1>
MIPI1C_CAM_FRONT_CLK_P
MIPI1C_CAM_FRONT_CLK_N
MIPI_VSS
=PP1V8_EDP_SOC
R0940 0 1/20W MF 201
=PP1V8_EDP_AVDD_AUX
C0940 56PF 5% 16V NP0-C0G 01005
C0946 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
C0941 56PF 5% 16V NP0-C0G 01005
C0950 0.22UF 20% 6.3V X5R 01005
C0951 1.0UF 20% 6.3V X5R 0201-1
C0952 1.0UF 20% 6.3V X5R 0201-1
=PP1V0_EDP_PAD_DVDD_SOC
C0955 1.0UF 20% 6.3V X5R 0201-1
C0945 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
DP_PAD_DVDD (10MA)
DP_PAD_AVDDX (1MA)
DP_PAD_AVDDP0 (1MA)
DP_PAD_AVDD1 (50MA)
DP_PAD_AVDD0 (50MA)
DP_PAD_AVDD_AUX (1MA)
DP_PAD_AVDD3 (50MA)
DP_PAD_AVDD2 (50MA)
U0600
ALCATRAZ
DISCRETE
FBGA
(6 OF 14)
OMIT_TABLE
TP_EDP_PAD_DC_TP
DP_PAD_DC_TP
AP_EDP_R_BIAS
DP_PAD_R_BIAS
NOSTUFF
C0960 0.01UF 10% 6.3V X5R 01005
R0960 4.99K 1% 1/32W MF 01005
PLACE_NEAR=U0600.E19:3MM
EDP_HPD
DP_PAD_AUXP
DP_PAD_AUXN
DP_PAD_TX0P
DP_PAD_TX0N
DP_PAD_TX1P
DP_PAD_TX1N
DP_PAD_TX2P
DP_PAD_TX2N
DP_PAD_TX3P
DP_PAD_TX3N
EDP_AUX_P
EDP_AUX_N
EDP_DATA_P<0>
EDP_DATA_N<0>
EDP_DATA_P<1>
EDP_DATA_N<1>
EDP_DATA_P<2>
EDP_DATA_N<2>
EDP_DATA_P<3>
EDP_DATA_N<3>
DP_PAD_AVSS2
DP_PAD_AVSS3
DP_PAD_DVSS
DP_PAD_AVSSX
DP_PAD_AVSSP0
DP_PAD_AVSS1
DP_PAD_AVSS0
DP_PAD_AVSS_AUX

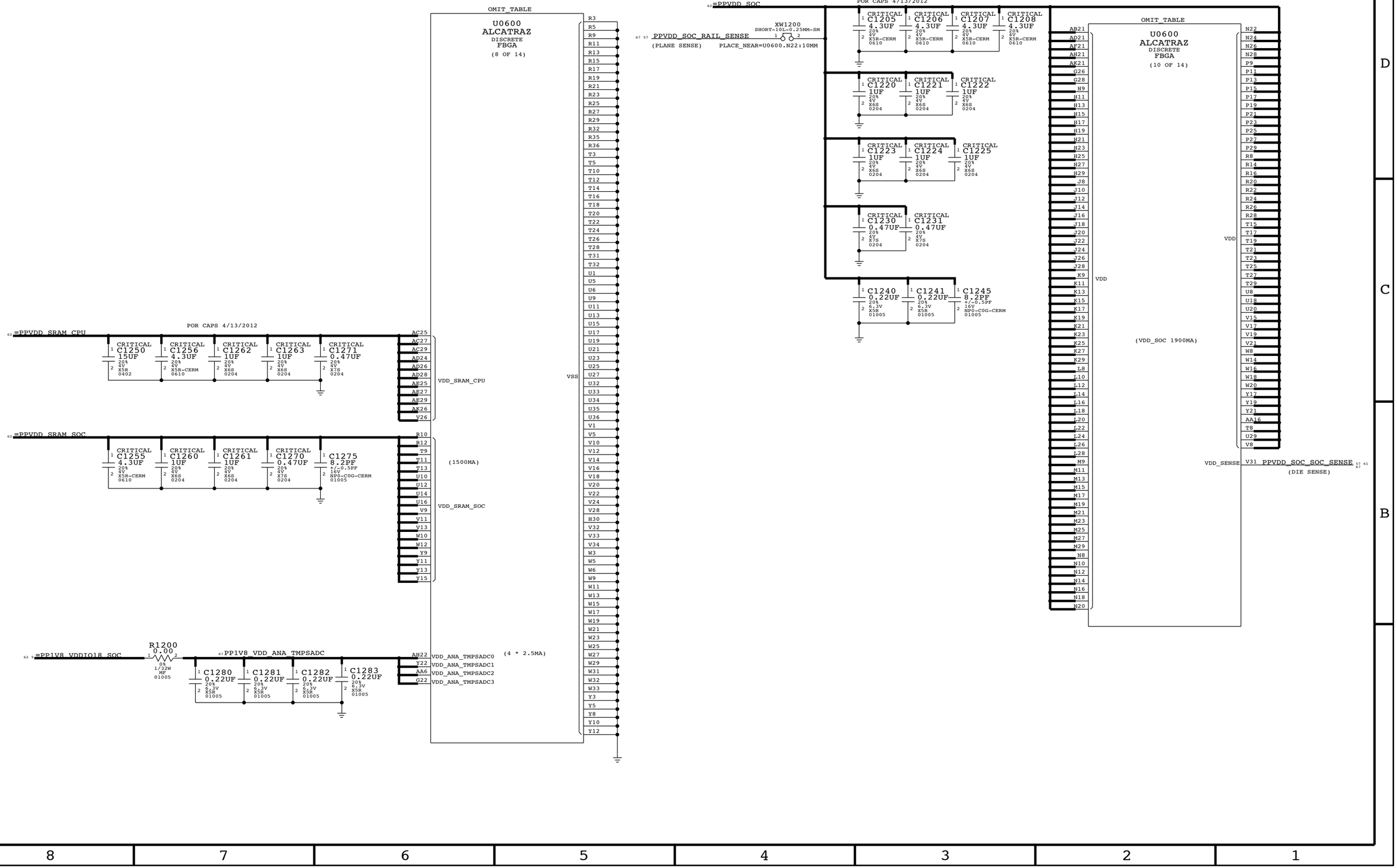

=PP1V2_S2R_DDR_SOC
C1090 0.1UF 20% 6.3V X5R-CERM 01005
R1090 10K 1% 1/32W MF 01005
C1092 0.1UF 20% 6.3V X5R-CERM 01005
R1092 10K 1% 1/32W MF 01005
PPVREF_DDR0_CA_SOC
PPVREF_DDR1_CA_SOC
C1091 0.1UF 20% 6.3V X5R-CERM 01005
R1091 10K 1% 1/32W MF 01005
C1093 0.1UF 20% 6.3V X5R-CERM 01005
R1093 10K 1% 1/32W MF 01005

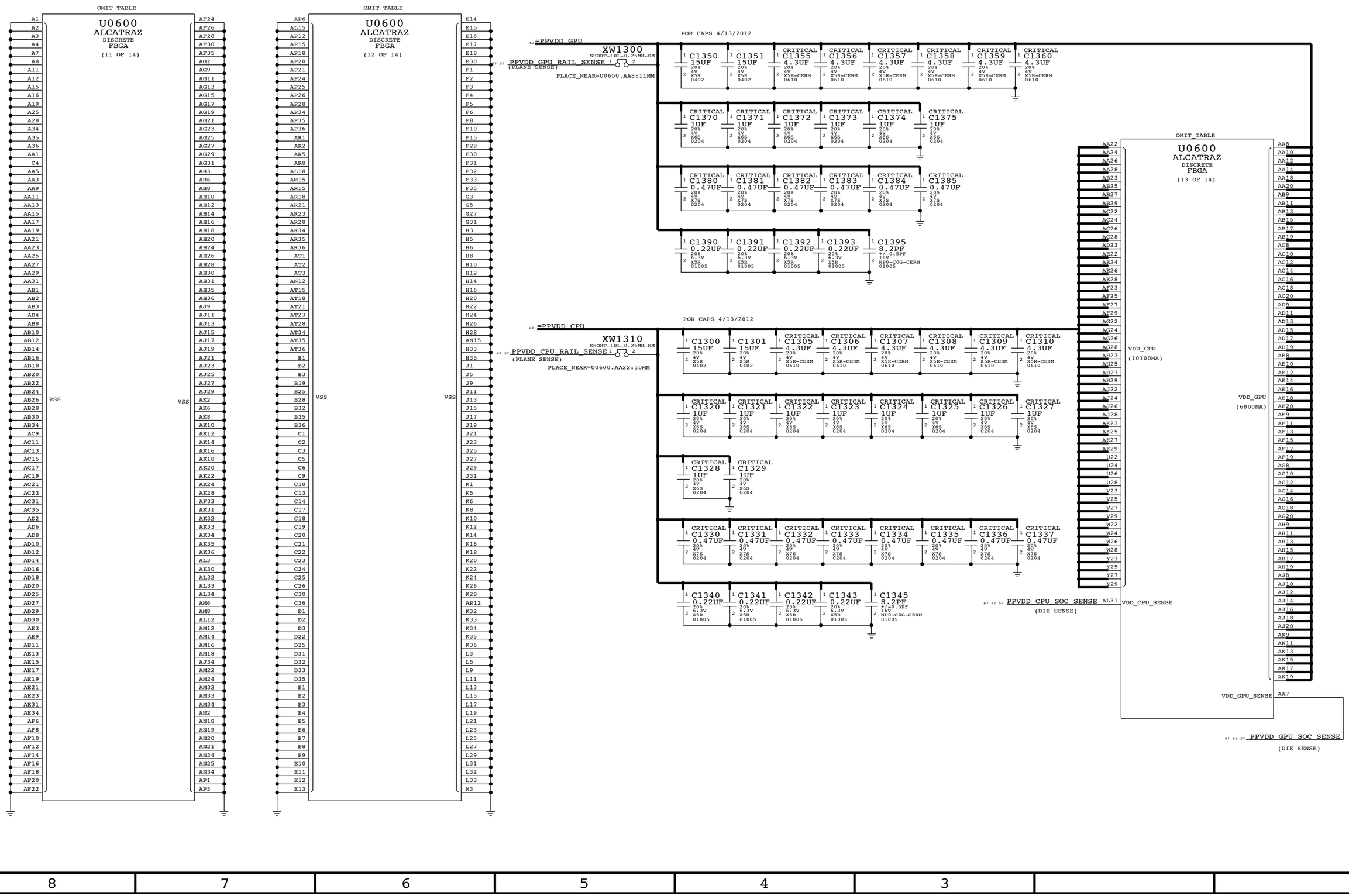
=PP1V2_VDDIOD_SOC
C1094 0.1UF 20% 6.3V X5R-CERM 01005
R1094 4.7K 1% 1/32W MF 01005
C1096 0.1UF 20% 6.3V X5R-CERM 01005
R1096 4.7K 1% 1/32W MF 01005
PPVREF_DDR0_DQ_SOC
PPVREF_DDR1_DQ_SOC
C1095 0.1UF 20% 6.3V X5R-CERM 01005
R1095 4.7K 1% 1/32W MF 01005
C1097 0.1UF 20% 6.3V X5R-CERM 01005
R1097 4.7K 1% 1/32W MF 01005

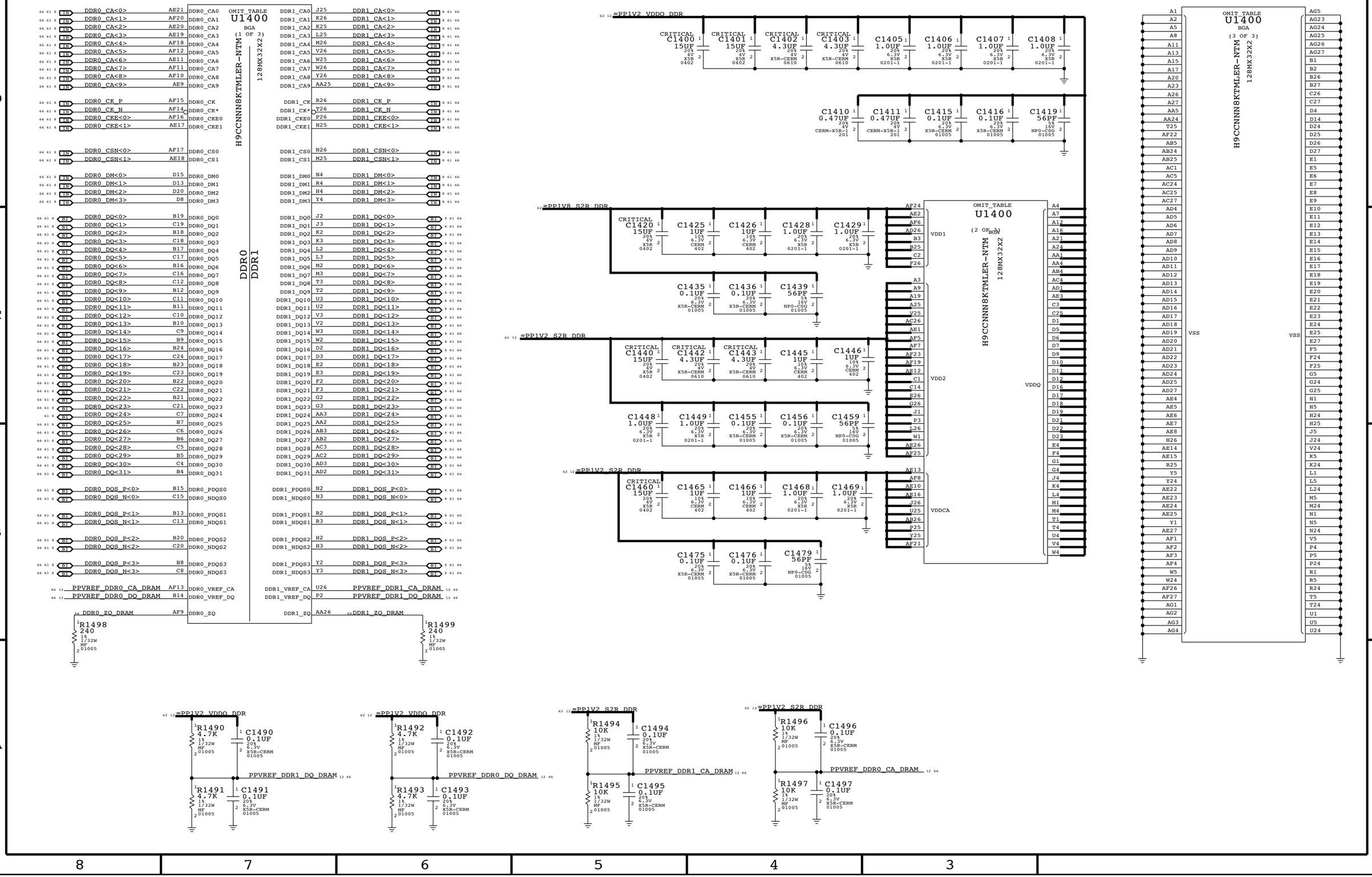

OMIT_TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(14 OF 14)
DDR0_CA<0> AP27 DDR0_CA0
DDR0_CA<1> AR27 DDR0_CA1
DDR0_CA<2> AT27 DDR0_CA2
DDR0_CA<3> AR26 DDR0_CA3
DDR0_CA<4> AT26 DDR0_CA4
DDR0_CA<5> AR20 DDR0_CA5
DDR0_CA<6> AT20 DDR0_CA6
DDR0_CA<7> AT19 DDR0_CA7
DDR0_CA<8> AR19 DDR0_CA8
DDR0_CA<9> AP19 DDR0_CA9
DDR0_CKE<0> AR24 DDR0_CKE0
DDR0_CKE<1> AT24 DDR0_CKE1
DDR0_CSN<0> AR25 DDR0_CSN0
DDR0_CSN<1> AT25 DDR0_CSN1
DDR0_DM<0> D11 DDR0_DM0
DDR0_DM<1> D9 DDR0_DM1
DDR0_DM<2> C15 DDR0_DM2
DDR0_DM<3> D7 DDR0_DM3
DDR0_DQ<0> B15 DDR0_DQ0
DDR0_DQ<1> D14 DDR0_DQ1
DDR0_DQ<2> B14 DDR0_DQ2
DDR0_DQ<3> D13 DDR0_DQ3
DDR0_DQ<4> B13 DDR0_DQ4
DDR0_DQ<5> D12 DDR0_DQ5
DDR0_DQ<6> C12 DDR0_DQ6
DDR0_DQ<7> B12 DDR0_DQ7
DDR0_DQ<8> C11 DDR0_DQ8
DDR0_DQ<9> B11 DDR0_DQ9
DDR0_DQ<10> D10 DDR0_DQ10
DDR0_DQ<11> B10 DDR0_DQ11
DDR0_DQ<12> B9 DDR0_DQ12
DDR0_DQ<13> D8 DDR0_DQ13
DDR0_DQ<14> C8 DDR0_DQ14
DDR0_DQ<15> B8 DDR0_DQ15
DDR0_DQ<16> D18 DDR0_DQ16
DDR0_DQ<17> B18 DDR0_DQ17
DDR0_DQ<18> D17 DDR0_DQ18
DDR0_DQ<19> B17 DDR0_DQ19
DDR0_DQ<20> D16 DDR0_DQ20
DDR0_DQ<21> C16 DDR0_DQ21
DDR0_DQ<22> B16 DDR0_DQ22
DDR0_DQ<23> D15 DDR0_DQ23
DDR0_DQ<24> C7 DDR0_DQ24
DDR0_DQ<25> B7 DDR0_DQ25
DDR0_DQ<26> D6 DDR0_DQ26
DDR0_DQ<27> B6 DDR0_DQ27
DDR0_DQ<28> D5 DDR0_DQ28
DDR0_DQ<29> B5 DDR0_DQ29
DDR0_DQ<30> D4 DDR0_DQ30
DDR0_DQ<31> B4 DDR0_DQ31
DDR0_DQS_P<0> A14 DDR0_PDQS0
DDR0_DQS_P<1> A9 DDR0_PDQS1
DDR0_DQS_P<2> A18 DDR0_PDQS2
DDR0_DQS_P<3> A5 DDR0_PDQS3
DDR0_DQS_N<0> A13 DDR0_NDQS0
DDR0_DQS_N<1> A10 DDR0_NDQS1
DDR0_DQS_N<2> A17 DDR0_NDQS2
DDR0_DQS_N<3> A6 DDR0_NDQS3
DDR0_CK_P AT22 DDR0_CK
DDR0_CK_N AR22 DDR0_CKB
AP23 DDR0_VDD_CKE
R34 DDR1_VDD_CKE (<1MA EACH)
DDR0_CA_ZQ_SOC AN22 DDR0_RREF_CA
DDR1_CA_ZQ_SOC T33 DDR1_RREF_CA
DDR0_DQ_ZQ_SOC F12 DDR0_RREF_DQ
DDR1_DQ_ZQ_SOC R6 DDR1_RREF_DQ
PPVREF_DDR0_CA_SOC AP22 DDR0_VREF_CA
PPVREF_DDR1_CA_SOC T34 DDR1_VREF_CA
PPVREF_DDR0_DQ_SOC F13 DDR0_VREF_DQ
PPVREF_DDR1_DQ_SOC P6 DDR1_VREF_DQ
DDR1_CA0 L34 DDR1_CA<0>
DDR1_CA1 L35 DDR1_CA<1>
DDR1_CA2 L36 DDR1_CA<2>
DDR1_CA3 M35 DDR1_CA<3>
DDR1_CA4 M36 DDR1_CA<4>
DDR1_CA5 V35 DDR1_CA<5>
DDR1_CA6 V36 DDR1_CA<6>
DDR1_CA7 W36 DDR1_CA<7>
DDR1_CA8 W35 DDR1_CA<8>
DDR1_CA9 W34 DDR1_CA<9>
DDR1_CKE0 P35 DDR1_CKE<0>
DDR1_CKE1 P36 DDR1_CKE<1>
DDR1_CSN0 N35 DDR1_CSN<0>
DDR1_CSN1 N36 DDR1_CSN<1>
DDR1_DM0 P4 DDR1_DM<0>
DDR1_DM1 T4 DDR1_DM<1>
DDR1_DM2 K3 DDR1_DM<2>
DDR1_DM3 V4 DDR1_DM<3>
DDR1_DQ0 K2 DDR1_DQ<0>
DDR1_DQ1 L4 DDR1_DQ<1>
DDR1_DQ2 L2 DDR1_DQ<2>
DDR1_DQ3 M4 DDR1_DQ<3>
DDR1_DQ4 M2 DDR1_DQ<4>
DDR1_DQ5 N4 DDR1_DQ<5>
DDR1_DQ6 N3 DDR1_DQ<6>
DDR1_DQ7 N2 DDR1_DQ<7>
DDR1_DQ8 P3 DDR1_DQ<8>
DDR1_DQ9 P2 DDR1_DQ<9>
DDR1_DQ10 R4 DDR1_DQ<10>
DDR1_DQ11 R2 DDR1_DQ<11>
DDR1_DQ12 T2 DDR1_DQ<12>
DDR1_DQ13 U4 DDR1_DQ<13>
DDR1_DQ14 U3 DDR1_DQ<14>
DDR1_DQ15 U2 DDR1_DQ<15>
DDR1_DQ16 G4 DDR1_DQ<16>
DDR1_DQ17 G2 DDR1_DQ<17>
DDR1_DQ18 H4 DDR1_DQ<18>
DDR1_DQ19 H2 DDR1_DQ<19>
DDR1_DQ20 J4 DDR1_DQ<20>
DDR1_DQ21 J3 DDR1_DQ<21>
DDR1_DQ22 J2 DDR1_DQ<22>
DDR1_DQ23 K4 DDR1_DQ<23>
DDR1_DQ24 V3 DDR1_DQ<24>
DDR1_DQ25 V2 DDR1_DQ<25>
DDR1_DQ26 W4 DDR1_DQ<26>
DDR1_DQ27 W2 DDR1_DQ<27>
DDR1_DQ28 Y4 DDR1_DQ<28>
DDR1_DQ29 Y2 DDR1_DQ<29>
DDR1_DQ30 AA4 DDR1_DQ<30>
DDR1_DQ31 AA2 DDR1_DQ<31>
DDR1_PDQS0 L1 DDR1_DQS_P<0>
DDR1_PDQS1 T1 DDR1_DQS_P<1>
DDR1_PDQS2 G1 DDR1_DQS_P<2>
DDR1_PDQS3 Y1 DDR1_DQS_P<3>
DDR1_NDQS0 M1 DDR1_DQS_N<0>
DDR1_NDQS1 R1 DDR1_DQS_N<1>
DDR1_NDQS2 H1 DDR1_DQS_N<2>
DDR1_NDQS3 W1 DDR1_DQS_N<3>
DDR1_CK T36 DDR1_CK_P
DDR1_CKB T35 DDR1_CK_N


=PP1V2_S2R_DDR_SOC
C1001 0.22UF 20% 6.3V X5R 01005
C1000 0.22UF 20% 6.3V X5R 01005
R1000 240 1% 1/32W MF 01005
R1001 240 1% 1/32W MF 01005
R1002 240 1% 1/32W MF 01005
R1003 240 1% 1/32W MF 01005
(DDR IMPEDANCE CONTROL)


=PP1V2_VDDIOD_SOC
C1100 1.0UF 20% 6.3V X5R 0201-1
C1101 1.0UF 20% 6.3V X5R 0201-1
C1102 1.0UF 20% 6.3V X5R 0201-1
C1105 0.47UF 20% 4V CERM-X5R-1 201
C1106 0.47UF 20% 4V CERM-X5R-1 201
DDR0_CA0 CAPS
C1110 1.0UF 20% 6.3V X5R 0201-1
C1111 1.0UF 20% 6.3V X5R 0201-1
C1112 1.0UF 20% 6.3V X5R 0201-1
C1115 0.47UF 20% 4V CERM-X5R-1 201
C1116 0.47UF 20% 4V CERM-X5R-1 201
DDR1_CA1 CAPS
=PP1V8_VDDIO18_SOC
POR CAPS 4/13/2012
CRITICAL
C1120 4.3UF 20% 4V X5R-CERM 0610
C1125 1.0UF 20% 6.3V X5R 0201-1
C1126 1.0UF 20% 6.3V X5R 0201-1
C1130 0.47UF 20% 4V CERM-X5R-1 201
C1131 0.47UF 20% 4V CERM-X5R-1 201
C1135 1.0UF 20% 6.3V X5R 0201-1
C1140 0.22UF 20% 6.3V X5R 01005
C1141 0.22UF 20% 6.3V X5R 01005
C1145 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
OMIT_TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(9 OF 14)
VDDIOD_DDR0CA
VDDIOD_DDR1CA
VDDIO18_GRP1
(65MA)
GPIO, UART, SPI,
I2C, SENSOR,
SOCHOT, PMU
VDDIOD_DDRDQ
(1000MA)
SHARED WITH DRAM VDDQ
VDDIO18_GRP2
(20MA)
I2S, TMR, SIO,
GPIO, UART
VDDIO18_GRP3
(31MA)
PPN, GPIO, JTAG
VDDIO18_GRP4 (2MA) XTAL I/O
VSS
PLACE_NEAR=U0600.F27:2MM
L1190
120-OHM-25%-250MA-0.5DCR
01005
=PP1V8_XTAL
C1190 0.22UF 20% 6.3V X5R 01005
POR CAPS 4/13/2012
=PP1V2_VDDIOD_SOC
C1150 15UF 20% 4V X5R 0402
CRITICAL
C1155 4.3UF 20% 4V X5R-CERM 0610
C1160 1.0UF 20% 6.3V X5R 0201-1
C1161 1.0UF 20% 6.3V X5R 0201-1
C1162 1.0UF 20% 6.3V X5R 0201-1
C1163 1.0UF 20% 6.3V X5R 0201-1
C1165 0.47UF 20% 4V CERM-X5R-1 201
C1166 0.47UF 20% 4V CERM-X5R-1 201
C1170 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
OMIT_TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(7 OF 14)
VSS


OMIT_TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(8 OF 14)
VSS
=PPVDD_SRAM_CPU
POR CAPS 4/13/2012
CRITICAL C1250 15UF 20% 4V X5R 0402
CRITICAL C1256 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1262 1UF 20% 4V X6S 0204
CRITICAL C1263 1UF 20% 4V X6S 0204
CRITICAL C1271 0.47UF 20% 4V X7S 0204
AC25 AC27 AC29 AD24 AD26 AD28 AE25 AE27 AE29 AK26 V26
VDD_SRAM_CPU
=PPVDD_SRAM_SOC
CRITICAL C1255 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1260 1UF 20% 4V X6S 0204
CRITICAL C1261 1UF 20% 4V X6S 0204
CRITICAL C1270 0.47UF 20% 4V X7S 0204
C1275 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
R10 R12 T9 T11 T13 U10 U12 U14 U16 V9 V11 V13 W10 W12 Y9 Y11 Y13 Y15
(1500MA)
VDD_SRAM_SOC
=PP1V8_VDDIO18_SOC
R1200 0.00 0% 1/32W MF 01005
=PP1V8_VDD_ANA_TMPSADC
C1280 0.22UF 20% 6.3V X5R 01005
C1281 0.22UF 20% 6.3V X5R 01005
C1282 0.22UF 20% 6.3V X5R 01005
C1283 0.22UF 20% 6.3V X5R 01005
AH22 Y22 AA6 G22
VDD_ANA_TMPSADC0
VDD_ANA_TMPSADC1
VDD_ANA_TMPSADC2
VDD_ANA_TMPSADC3
(4 * 2.5MA)
R3 R5 R9 R11 R13 R15 R17 R19 R21 R23 R25 R27 R29 R32 R35 R36 T3 T5 T10 T12 T14 T16 T18 T20 T22 T24 T26 T28 T31 T32 U1 U5 U6 U9 U11 U13 U15 U17 U19 U21 U23 U25 U27 U32 U33 U34 U35 U36 V1 V5 V10 V12 V14 V16 V18 V20 V22 V24 V28 H30 V32 V33 V34 W3 W5 W6 W9 W11 W13 W15 W17 W19 W21 W23 W25 W27 W29 W31 W32 W33 Y3 Y5 Y8 Y10 Y12
=PPVDD_SOC
POR CAPS 4/13/2012
XW1200 SHORT-10L-0.25MM-SM
PPVDD_SOC_RAIL_SENSE
(PLANE SENSE)
PLACE_NEAR=U0600.N22:10MM
CRITICAL C1205 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1206 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1207 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1208 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1220 1UF 20% 4V X6S 0204
CRITICAL C1221 1UF 20% 4V X6S 0204
CRITICAL C1222 1UF 20% 4V X6S 0204
CRITICAL C1223 1UF 20% 4V X6S 0204
CRITICAL C1224 1UF 20% 4V X6S 0204
CRITICAL C1225 1UF 20% 4V X6S 0204
CRITICAL C1230 0.47UF 20% 4V X7S 0204
CRITICAL C1231 0.47UF 20% 4V X7S 0204
C1240 0.22UF 20% 6.3V X5R 01005
C1241 0.22UF 20% 6.3V X5R 01005
C1245 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
OMIT_TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(10 OF 14)
VDD
(VDD_SOC 1900MA)
AB21 AD21 AF21 AH21 AK21 G26 G28 H9 H11 H13 H15 H17 H19 H21 H23 H25 H27 H29 J8 J10 J12 J14 J16 J18 J20 J22 J24 J26 J28 K9 K11 K13 K15 K17 K19 K21 K23 K25 K27 K29 L8 L10 L12 L14 L16 L18 L20 L22 L24 L26 L28 M9 M11 M13 M15 M17 M19 M21 M23 M25 M27 M29 N8 N10 N12 N14 N16 N18 N20
N22 N24 N26 N28 P9 P11 P13 P15 P17 P19 P21 P23 P25 P27 P29 R8 R14 R16 R20 R22 R24 R26 R28 T15 T17 T19 T21 T23 T25 T27 T29 U8 U18 U20 V15 V17 V19 V21 W8 W14 W16 W18 W20 Y17 Y19 Y21 AA16 T8 U29 V8
VDD
VDD_SENSE
V31 PPVDD_SOC_SOC_SENSE
(DIE SENSE)


OMIT_TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(11 OF 14)
VSS
OMIT_TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(12 OF 14)
VSS
=PPVDD_GPU
XW1300
SHORT-10L-0.25MM-SM
PPVDD_GPU_RAIL_SENSE
(PLANE SENSE)
PLACE_NEAR=U0600.AA8:11MM
POR CAPS 4/13/2012
C1350 15UF 20% 4V X5R 0402
C1351 15UF 20% 4V X5R 0402
CRITICAL C1355 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1356 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1357 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1358 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1359 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1360 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1370 1UF 20% 4V X6S 0204
CRITICAL C1371 1UF 20% 4V X6S 0204
CRITICAL C1372 1UF 20% 4V X6S 0204
CRITICAL C1373 1UF 20% 4V X6S 0204
CRITICAL C1374 1UF 20% 4V X6S 0204
CRITICAL C1375 1UF 20% 4V X6S 0204
CRITICAL C1380 0.47UF 20% 4V X7S 0204
CRITICAL C1381 0.47UF 20% 4V X7S 0204
CRITICAL C1382 0.47UF 20% 4V X7S 0204
CRITICAL C1383 0.47UF 20% 4V X7S 0204
CRITICAL C1384 0.47UF 20% 4V X7S 0204
CRITICAL C1385 0.47UF 20% 4V X7S 0204
C1390 0.22UF 20% 6.3V X5R 01005
C1391 0.22UF 20% 6.3V X5R 01005
C1392 0.22UF 20% 6.3V X5R 01005
C1393 0.22UF 20% 6.3V X5R 01005
C1395 8.2PF +/-0.5PF 16V NPO-COG-CERM 01005
=PPVDD_CPU
XW1310
SHORT-10L-0.25MM-SM
PPVDD_CPU_RAIL_SENSE
(PLANE SENSE)
PLACE_NEAR=U0600.AA22:10MM
POR CAPS 4/13/2012
C1300 15UF 20% 4V X5R 0402
C1301 15UF 20% 4V X5R 0402
CRITICAL C1305 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1306 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1307 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1308 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1309 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1310 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1320 1UF 20% 4V X6S 0204
CRITICAL C1321 1UF 20% 4V X6S 0204
CRITICAL C1322 1UF 20% 4V X6S 0204
CRITICAL C1323 1UF 20% 4V X6S 0204
CRITICAL C1324 1UF 20% 4V X6S 0204
CRITICAL C1325 1UF 20% 4V X6S 0204
CRITICAL C1326 1UF 20% 4V X6S 0204
CRITICAL C1327 1UF 20% 4V X6S 0204
CRITICAL C1328 1UF 20% 4V X6S 0204
CRITICAL C1329 1UF 20% 4V X6S 0204
CRITICAL C1330 0.47UF 20% 4V X7S 0204
CRITICAL C1331 0.47UF 20% 4V X7S 0204
CRITICAL C1332 0.47UF 20% 4V X7S 0204
CRITICAL C1333 0.47UF 20% 4V X7S 0204
CRITICAL C1334 0.47UF 20% 4V X7S 0204
CRITICAL C1335 0.47UF 20% 4V X7S 0204
CRITICAL C1336 0.47UF 20% 4V X7S 0204
CRITICAL C1337 0.47UF 20% 4V X7S 0204
C1340 0.22UF 20% 6.3V X5R 01005
C1341 0.22UF 20% 6.3V X5R 01005
C1342 0.22UF 20% 6.3V X5R 01005
C1343 0.22UF 20% 6.3V X5R 01005
C1345 8.2PF +/-0.5PF 16V NPO-COG-CERM 01005
OMIT_TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(13 OF 14)
VDD_CPU
(10100MA)
VDD_GPU
(6800MA)
PPVDD_CPU_SOC_SENSE
(DIE SENSE)
VDD_CPU_SENSE
VDD_GPU_SENSE
PPVDD_GPU_SOC_SENSE
(DIE SENSE)


U1400
H9CCNNN8KTMLER-NTM
128MX32X2
DDR0
DDR1
OMIT_TABLE
BGA
(1 OF 3)
(2 OF 3)
(3 OF 3)
DDR0_CA<0>
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DDR0_CA<2>
DDR0_CA<3>
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DDR0_CK_P
DDR0_CK_N
DDR0_CKE<0>
DDR0_CKE<1>
DDR0_CSN<0>
DDR0_CSN<1>
DDR0_DM<0>
DDR0_DM<1>
DDR0_DM<2>
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DDR0_DQ<31>
DDR0_DQS_P<0>
DDR0_DQS_N<0>
DDR0_DQS_P<1>
DDR0_DQS_N<1>
DDR0_DQS_P<2>
DDR0_DQS_N<2>
DDR0_DQS_P<3>
DDR0_DQS_N<3>
PPVREF_DDR0_CA_DRAM
PPVREF_DDR0_DQ_DRAM
DDR0_ZQ_DRAM
DDR0_CA0
DDR0_CA1
DDR0_CA2
DDR0_CA3
DDR0_CA4
DDR0_CA5
DDR0_CA6
DDR0_CA7
DDR0_CA8
DDR0_CA9
DDR0_CK
DDR0_CK*
DDR0_CKE0
DDR0_CKE1
DDR0_CS0
DDR0_CS1
DDR0_DM0
DDR0_DM1
DDR0_DM2
DDR0_DM3
DDR0_DQ0
DDR0_DQ1
DDR0_DQ2
DDR0_DQ3
DDR0_DQ4
DDR0_DQ5
DDR0_DQ6
DDR0_DQ7
DDR0_DQ8
DDR0_DQ9
DDR0_DQ10
DDR0_DQ11
DDR0_DQ12
DDR0_DQ13
DDR0_DQ14
DDR0_DQ15
DDR0_DQ16
DDR0_DQ17
DDR0_DQ18
DDR0_DQ19
DDR0_DQ20
DDR0_DQ21
DDR0_DQ22
DDR0_DQ23
DDR0_DQ24
DDR0_DQ25
DDR0_DQ26
DDR0_DQ27
DDR0_DQ28
DDR0_DQ29
DDR0_DQ30
DDR0_DQ31
DDR0_PDQS0
DDR0_NDQS0
DDR0_PDQS1
DDR0_NDQS1
DDR0_PDQS2
DDR0_NDQS2
DDR0_PDQS3
DDR0_NDQS3
DDR0_VREF_CA
DDR0_VREF_DQ
DDR0_ZQ
DDR1_CA0
DDR1_CA1
DDR1_CA2
DDR1_CA3
DDR1_CA4
DDR1_CA5
DDR1_CA6
DDR1_CA7
DDR1_CA8
DDR1_CA9
DDR1_CK
DDR1_CK*
DDR1_CKE0
DDR1_CKE1
DDR1_CS0
DDR1_CS1
DDR1_DM0
DDR1_DM1
DDR1_DM2
DDR1_DM3
DDR1_DQ0
DDR1_DQ1
DDR1_DQ2
DDR1_DQ3
DDR1_DQ4
DDR1_DQ5
DDR1_DQ6
DDR1_DQ7
DDR1_DQ8
DDR1_DQ9
DDR1_DQ10
DDR1_DQ11
DDR1_DQ12
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DDR1_DQ25
DDR1_DQ26
DDR1_DQ27
DDR1_DQ28
DDR1_DQ29
DDR1_DQ30
DDR1_DQ31
DDR1_PDQS0
DDR1_NDQS0
DDR1_PDQS1
DDR1_NDQS1
DDR1_PDQS2
DDR1_NDQS2
DDR1_PDQS3
DDR1_NDQS3
DDR1_VREF_CA
DDR1_VREF_DQ
DDR1_ZQ
PPVREF_DDR1_CA_DRAM
PPVREF_DDR1_DQ_DRAM
DDR1_ZQ_DRAM
R1498 240 1% 1/32W MF 01005
R1499 240 1% 1/32W MF 01005
=PP1V2_VDDQ_DDR
=PP1V8_S2R_DDR
=PP1V2_S2R_DDR
C1400 15UF 20% 4V X5R 0402 CRITICAL
C1401 15UF 20% 4V X5R 0402 CRITICAL
C1402 4.3UF 20% 4V X5R-CERM 0610 CRITICAL
C1403 4.3UF 20% 4V X5R-CERM 0610 CRITICAL
C1405 1.0UF 20% 6.3V X5R 0201-1
C1406 1.0UF 20% 6.3V X5R 0201-1
C1407 1.0UF 20% 6.3V X5R 0201-1
C1408 1.0UF 20% 6.3V X5R 0201-1
C1410 0.47UF 20% 4V CERM-X5R-1 201
C1411 0.47UF 20% 4V CERM-X5R-1 201
C1415 0.1UF 20% 6.3V X5R-CERM 01005
C1416 0.1UF 20% 6.3V X5R-CERM 01005
C1419 56PF 5% 16V NP0-C0G 01005
C1420 15UF 20% 4V X5R 0402 CRITICAL
C1425 1UF 10% 6.3V CERM 402
C1426 1UF 10% 6.3V CERM 402
C1428 1.0UF 20% 6.3V X5R 0201-1
C1429 1.0UF 20% 6.3V X5R 0201-1
C1435 0.1UF 20% 6.3V X5R-CERM 01005
C1436 0.1UF 20% 6.3V X5R-CERM 01005
C1439 56PF 5% 16V NP0-C0G 01005
C1440 15UF 20% 4V X5R 0402 CRITICAL
C1442 4.3UF 20% 4V X5R-CERM 0610 CRITICAL
C1443 4.3UF 20% 4V X5R-CERM 0610 CRITICAL
C1445 1UF 10% 6.3V CERM 402
C1446 1.0UF 20% 6.3V X5R 0201-1
C1448 1.0UF 20% 6.3V X5R 0201-1
C1449 1.0UF 20% 6.3V X5R 0201-1
C1455 0.1UF 20% 6.3V X5R-CERM 01005
C1456 0.1UF 20% 6.3V X5R-CERM 01005
C1459 56PF 5% 16V NP0-C0G 01005
C1460 15UF 20% 4V X5R 0402 CRITICAL
C1465 1UF 10% 6.3V CERM 402
C1466 1UF 10% 6.3V CERM 402
C1468 1.0UF 20% 6.3V X5R 0201-1
C1469 1.0UF 20% 6.3V X5R 0201-1
C1475 0.1UF 20% 6.3V X5R-CERM 01005
C1476 0.1UF 20% 6.3V X5R-CERM 01005
C1479 56PF 5% 16V NP0-C0G 01005
VDD1
VDD2
VDDQ
VDDCA
VSS
R1490 4.7K 1% 1/32W MF 01005
C1490 0.1UF 20% 6.3V X5R-CERM 01005
R1491 4.7K 1% 1/32W MF 01005
C1491 0.1UF 20% 6.3V X5R-CERM 01005
R1492 4.7K 1% 1/32W MF 01005
C1492 0.1UF 20% 6.3V X5R-CERM 01005
R1493 4.7K 1% 1/32W MF 01005
C1493 0.1UF 20% 6.3V X5R-CERM 01005
R1494 10K 1% 1/32W MF 01005
C1494 0.1UF 20% 6.3V X5R-CERM 01005
R1495 10K 1% 1/32W MF 01005
C1495 0.1UF 20% 6.3V X5R-CERM 01005
R1496 10K 1% 1/32W MF 01005
C1496 0.1UF 20% 6.3V X5R-CERM 01005
R1497 10K 1% 1/32W MF 01005
C1497 0.1UF 20% 6.3V X5R-CERM 01005

BOOT CONFIG ID

62 58 13 7 5 4 =PP1V8_SOC

NOSTUFF R1500 10K 5% 1/32W MF 01005	NOSTUFF R1501 10K 5% 1/32W MF 01005	R1502 10K 5% 1/32W MF 01005	NOSTUFF R1503 10K 5% 1/32W MF 01005

BOOT_CONFIG[3] ← GPIO_BOOT_CONFIG_3
BOOT_CONFIG[2] ← GPIO_BOOT_CONFIG_2
BOOT_CONFIG[1] ← GPIO_BOOT_CONFIG_1
BOOT_CONFIG[0] ← GPIO_BOOT_CONFIG_0

BOOT_CONFIG[3:0]	MODE
0000	SPI
0001	SPI W/TEST
0010	NAND <-- CURRENT SETTING
0011	NAND W/TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

JTAG

R1510 240 1% 1/32W MF 01005

JTAG_SOC_SEL → OUT 4 60

R1560 240 1% 1/32W MF 01005

SOC_TESTMODE → OUT 4 60

SOC_FAST_SCAN_CLK → OUT 4 (MAKE_BASE=TRUE)

SOC_HOLD_RESET → OUT 4

BOARD ID

62 58 13 7 5 4 =PP1V8_SOC

NOSTUFF	MLB_C	MLB_B	DEV
R1504 10K 5% 1/32W MF 01005	R1505 10K 5% 1/32W MF 01005	R1506 10K 5% 1/32W MF 01005	R1507 10K 5% 1/32W MF 01005

BOARD_ID[3] ← GPIO_BOARD_ID_3
BOARD_ID[2] ← GPIO_BOARD_ID_2
BOARD_ID[1] ← GPIO_BOARD_ID_1
BOARD_ID[0] ← GPIO_BOARD_ID_0

BOARD_ID[3-0]	
0000	MLB_A AP
0001	MLB_A DEV
0010	MLB_B AP
0011	MLB_B DEV
0100	MLB_C AP
0101	MLB_C DEV

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION

GPIO_BRD_REV3
GPIO_BRD_REV2
GPIO_BRD_REV1
GPIO_BRD_REV0

NOSTUFF	NOSTUFF	NOSTUFF	
R1520 10K 5% 1/32W MF 01005	R1521 10K 5% 1/32W MF 01005	R1522 10K 5% 1/32W MF 01005	R1523 10K 5% 1/32W MF 01005

BRD_REV[3-0]	
0000	PROTO 0
0001	PROTO 0 + T2
0010	PROTO 1 + T2
0011	PROTO 1 + T1
0100	PROTO 1 + T1 + B0
0101	PROTO 2 + T2 + B0
0110	EVT + T2 + B0
CURRENT SETTING ---> 0111	DVT + T2 + B1

S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

ALIASED NETS TO ALLOW BREAKING ON DEV BOARD

GPIO_PROX2SOC_IRQ_L → =GPIO_ADUX1049_PROX2SOC_IRQ_L, =GPIO_AD7149_PROX2SOC_IRQ_L 45
(MAKE_BASE=TRUE)

64 61 22 5 I2C3_SCL_1V8 → =I2C3_PROX_ADUX1049_SCL_1V8, =I2C3_PROX_AD7149_SCL_1V8 45
64 61 22 5 I2C3_SDA_1V8 → =I2C3_PROX_ADUX1049_SDA_1V8, =I2C3_PROX_AD7149_SDA_1V8 45
(MAKE_BASE=TRUE)

67 4 WDOG_SOC → R1530 0.00 1% 1/32W MF 01005 → WDOG_SOC2PMU_RESET_IN 57 67

62 58 13 7 5 4 =PP1V8_SOC

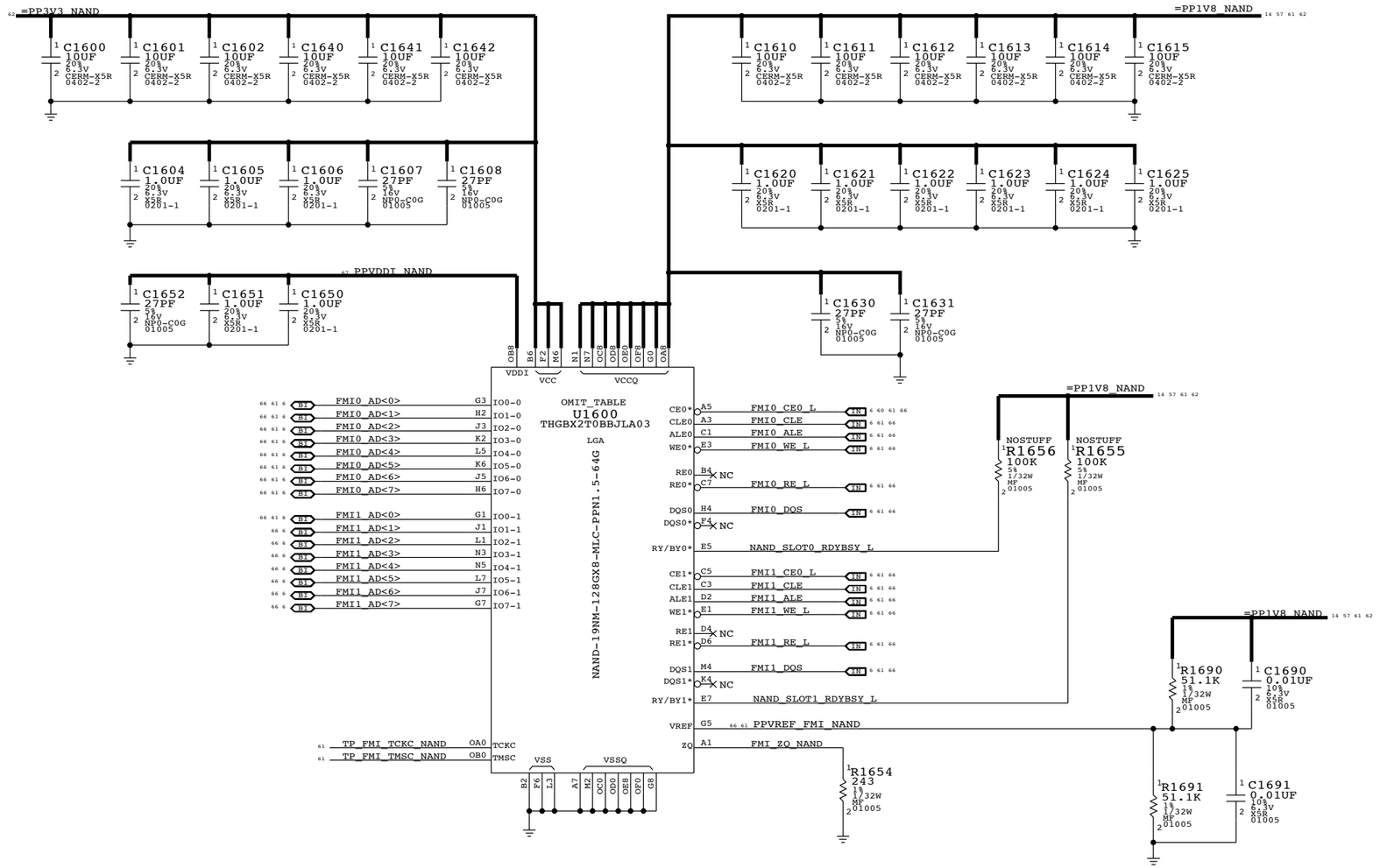
R0620 10K 5% 1/32W MF 01005

67 61 60 57 47 25 4 RESET_SOC_L → NOSTUFF R1535 0.00 1% 1/32W MF 01005 → JTAG_SOC_TRST_L 4 60 64

NOSTUFF R1536 240 1% 1/32W MF 01005

SHORTING RESET TO TRST HERE SO THEY CAN BE SEPARATED ON DEV BOARD

NOTE: WHEN USING A0 SOC
STUFF R1535
NOSTUFF R1536
CHANGE R0620 TO 4.7K


=PP3V3_NAND
C1600 10UF 20% 6.3V CERM-X5R 0402-2
C1601 10UF 20% 6.3V CERM-X5R 0402-2
C1602 10UF 20% 6.3V CERM-X5R 0402-2
C1640 10UF 20% 6.3V CERM-X5R 0402-2
C1641 10UF 20% 6.3V CERM-X5R 0402-2
C1642 10UF 20% 6.3V CERM-X5R 0402-2
C1604 1.0UF 20% 6.3V X5R 0201-1
C1605 1.0UF 20% 6.3V X5R 0201-1
C1606 1.0UF 20% 6.3V X5R 0201-1
C1607 27PF 5% 16V NP0-C0G 01005
C1608 27PF 5% 16V NP0-C0G 01005
PPVDDI_NAND
C1652 27PF 5% 16V NP0-C0G 01005
C1651 1.0UF 20% 6.3V X5R 0201-1
C1650 1.0UF 20% 6.3V X5R 0201-1
=PP1V8_NAND
C1610 10UF 20% 6.3V CERM-X5R 0402-2
C1611 10UF 20% 6.3V CERM-X5R 0402-2
C1612 10UF 20% 6.3V CERM-X5R 0402-2
C1613 10UF 20% 6.3V CERM-X5R 0402-2
C1614 10UF 20% 6.3V CERM-X5R 0402-2
C1615 10UF 20% 6.3V CERM-X5R 0402-2
C1620 1.0UF 20% 6.3V X5R 0201-1
C1621 1.0UF 20% 6.3V X5R 0201-1
C1622 1.0UF 20% 6.3V X5R 0201-1
C1623 1.0UF 20% 6.3V X5R 0201-1
C1624 1.0UF 20% 6.3V X5R 0201-1
C1625 1.0UF 20% 6.3V X5R 0201-1
C1630 27PF 5% 16V NP0-C0G 01005
C1631 27PF 5% 16V NP0-C0G 01005
OBB VDDI
B6 F2 M6 VCC
N1 N7 OC8 OD8 OB8 OF8 G8 OA8 VCCQ
OMIT_TABLE
U1600
THGBX2T0BBJLA03
LGA
NAND-19NM-128GX8-MLC-PPN1.5-64G
FMI0_AD<0> G3 IO0-0
FMI0_AD<1> H2 IO1-0
FMI0_AD<2> J3 IO2-0
FMI0_AD<3> K2 IO3-0
FMI0_AD<4> L5 IO4-0
FMI0_AD<5> K6 IO5-0
FMI0_AD<6> J5 IO6-0
FMI0_AD<7> H6 IO7-0
FMI1_AD<0> G1 IO0-1
FMI1_AD<1> J1 IO1-1
FMI1_AD<2> L1 IO2-1
FMI1_AD<3> N3 IO3-1
FMI1_AD<4> N5 IO4-1
FMI1_AD<5> L7 IO5-1
FMI1_AD<6> J7 IO6-1
FMI1_AD<7> G7 IO7-1
CE0* A5 FMI0_CE0_L
CLE0 A3 FMI0_CLE
ALE0 C1 FMI0_ALE
WE0* E3 FMI0_WE_L
RE0 B4 NC
RE0* C7 FMI0_RE_L
DQS0 H4 FMI0_DQS
DQS0* F4 NC
RY/BY0* E5 NAND_SLOT0_RDYBSY_L
CE1* C5 FMI1_CE0_L
CLE1 C3 FMI1_CLE
ALE1 D2 FMI1_ALE
WE1* E1 FMI1_WE_L
RE1 D4 NC
RE1* D6 FMI1_RE_L
DQS1 M4 FMI1_DQS
DQS1* K4 NC
RY/BY1* E7 NAND_SLOT1_RDYBSY_L
VREF G5 PPVREF_FMI_NAND
ZQ A1 FMI_ZQ_NAND
TP_FMI_TCKC_NAND OA0 TCKC
TP_FMI_TMSC_NAND OB0 TMSC
VSS VSSQ
B2 F6 L3 A7 M2 OC0 OD0 OB8 OF0 G8
R1654 243 1% 1/32W MF 01005
NOSTUFF R1656 100K 5% 1/32W MF 01005
NOSTUFF R1655 100K 5% 1/32W MF 01005
=PP1V8_NAND
R1690 51.1K 1% 1/32W MF 01005
C1690 0.01UF 10% 6.3V X5R 01005
R1691 51.1K 1% 1/32W MF 01005
C1691 0.01UF 10% 6.3V X5R 01005

NOTE: U1900 DECAPS CHANGED ON 5/24/12 PER RDAR://PROBLEM/11485846

MIKEY BUS FILTER

SIGNAL_MODEL=EMPTY
C1730 100PF 5% 25V NPO-CERM 0201
R1730 12 5% 1/20W MF 201 — PLACE_NEAR=U1700.J4:10MM — L81_MBUS_P — MIKEY_TS_P
R1731 12 5% 1/20W MF 201 — PLACE_NEAR=U1700.K4:10MM — L81_MBUS_N — MIKEY_TS_N
NOSTUFF C1731 100PF 5% 25V NPO-CERM 0201
SIGNAL_MODEL=EMPTY
C1732 100PF 5% 25V NPO-CERM 0201

=PPVCC_MAIN_AUDIO
=PP1V8_AUDIO
C1702 0.1UF 20% 6.3V X5R-CERM 01005
C1715 0.1UF 20% 6.3V X5R-CERM 01005
C1704 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL C1740 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C1741 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C1742 10UF 20% 6.3V CERM-X5R 0402
VOLTAGE=1.7V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.15MM
R1750 1.00 1% 1/20W MF-LF 0201
=PP1V7_VCP
CRITICAL C1750 4.7UF 20% 6.3V X5R 402
CRITICAL C1751 1.0UF 20% 6.3V X5R 0201-1
=PP1V7_VA_VCP
CRITICAL C1701 4.7UF 20% 6.3V X5R 402
CRITICAL C1703 0.1UF 10% 6.3V CERM-X5R 0201
GND_AUDIO_CODEC
VOLTAGE=4.2V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.15MM
PPVCC_VPROG_CP
R1751 1.00 1% 1/20W MF-LF 0201
C1714 0.1UF 10% 6.3V CERM-X5R 0201
VOLTAGE=4.2V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.15MM
PPVCC_VPROG_MB_F
R1752 255K 1% 1/20W MF 201
C1713 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL C1705 4.7UF 20% 6.3V X5R-CERM1 402
L81_FLYP MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.15MM
CRITICAL C1706 4.7UF 20% 6.3V X5R-CERM1 402
L81_FLYC MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.15MM
L81_FLYN MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.15MM

CRITICAL U1700 CS42L81-CWZR-A1 WLCSP SYM 1 OF 2

VA	G1	
VCP0	G8	
VCP1	G9	
VD	A9	
VL	A8	
VP0	E8	
VP1	E9	
VPROG_CP	G10	
VPROG_MB	H1	
FLYP	H10	
FLYC	J10	
FLYN	K10	
+VCP_FILT	H9	L81_PVCP
GNDCP	J9	
-VCP_FILT	K9	L81_NVCP
NC_MIC1_BIAS (NO_TEST=TRUE)	H2	MIC1_BIAS
AIN1P	E3	AIN1+
AIN1N	E4	AIN1-
MIC1_BIAS_FILT	H3	MIC1_BIAS_FILT
AOUT1+	F10	LEFT_CH_OUT_P (OUT)
AOUT1_M	F9	LEFT_CH_OUT_N (OUT)
AOUT2+	D10	RIGHT_CH_OUT_P (OUT)
AOUT2-	D9	RIGHT_CH_OUT_N (OUT)
	J3	MIC2_BIAS_IN
	G4	MIC2_BIAS
	K3	MIC2_BIAS_FILT_IN
L81_MIC2_BIAS_FILT	F3	MIC2_BIAS_FILT
L81_AIN2_POS	C1	AIN2+
L81_AIN2_NEG	D1	AIN2M
NC_MIC3_BIAS (NO_TEST=TRUE)	H4	MIC3_BIAS
AIN3P	C3	AIN3+
AIN3N	C2	AIN3-
MIC3_BIAS_FILT	G3	MIC3_BIAS_FILT
NC_MIC4_BIAS (NO_TEST=TRUE)	F4	MIC4_BIAS
AIN4P	D2	AIN4+
AIN4N	E2	AIN4-
MIC4_BIAS_FILT	F2	MIC4_BIAS_FILT
L81_SPEAKER_VQ	C10	SPEAKER_VQ
DP	J4	L81_MBUS_P
DN	K4	L81_MBUS_N
HPOUTA	J8	CODEC_HP_LEFT
HPOUTB	K8	CODEC_HP_RIGHT
HS3	J1	CODEC_HP_HS3
HS4	K1	CODEC_HP_HS4
HS3_REF	K7	
HS4_REF	J7	
HPDETECT	H8	CODEC_HP_DET
LINEOUTA (NO_TEST=TRUE)	K6	NC_CODEC_LINE_OUT_L
LINEOUTB (NO_TEST=TRUE)	J6	NC_CODEC_LINE_OUT_R
LINEOUT_REF	H6	
FILT+	E1	L81_FILT
FILT-	F1	
GNDP	E10	
GNDD	A10	
GNDHS	K2	
GNDHS	J2	
GNDA	G2	

R1701 2.21K 1% 1/20W MF 201 — L81_MIC2_BIAS_IN
L81_MIC2_BIAS
CRITICAL C1711 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C1712 4.7UF 20% 6.3V X5R-CERM1 402
L81_MIC2_BIAS_FILT_IN
XW1702 SHORT-8L-0.25MM-SM — CODEC_HP_HS4_REF — HP_MIC_POS
C1716 0.1UF 10% 6.3V CERM-X5R 0201
XW1703 SHORT-8L-0.25MM-SM — CODEC_HP_HS3_REF — HP_MIC_NEG
C1717 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL C1718 4.7UF 20% 6.3V X5R-CERM1 402
GND_AUDIO_CODEC
C1710 10UF 20% 6.3V CERM-X5R 0402-2
XW1700 SM — GND_AUDIO_CODEC

CRITICAL C1707 4.7UF 20% 6.3V X5R-CERM1 402 — 0.15MM 0.30MM
CRITICAL C1708 4.7UF 20% 6.3V X5R-CERM1 402 — 0.15MM 0.30MM
GND_AUDIO_CODEC

R1720 3.3K 5% 1/32W MF 01005 — CODEC_HP_DET — CODEC_HP_DET_R
L1720 240-OHM-0.2A-0.8-OHM 0201-2 — CONN_HP_HEADSET_DET_FILT (IN)
NOSTUFF C1720 4700PF 10% 10V X7R 201

CRITICAL L1700 FERR-33-OHM-0.8A-0.09-OHM 0201 — CONN_HP_LEFT_FILT (OUT) — PLACE_NEAR=J1800.3:10MM — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM
CRITICAL L1701 FERR-33-OHM-0.8A-0.09-OHM 0201 — CONN_HP_RIGHT_FILT (OUT) — PLACE_NEAR=J1800.1:10MM — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM
CRITICAL L1702 FERR-33-OHM-0.8A-0.09-OHM 0201 — CONN_HP_HS3_FILT (IN) — PLACE_NEAR=J1800.14:10MM — MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.20MM
CRITICAL L1703 FERR-33-OHM-0.8A-0.09-OHM 0201 — CONN_HP_HS4_FILT (IN) — PLACE_NEAR=J1800.13:10MM — MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.20MM
CRITICAL L1704 FERR-33-OHM-0.8A-0.09-OHM 0201 — CONN_HP_HS3_REF_FILT (IN) — PLACE_NEAR=J1800.12:10MM
CRITICAL L1705 FERR-33-OHM-0.8A-0.09-OHM 0201 — CONN_HP_HS4_REF_FILT (IN) — PLACE_NEAR=J1800.11:10MM

CODEC_HP_HS3_REF
CODEC_HP_HS4_REF

TO HEADPHONE JACK

AIN3P — C1792 0.01UF 10% 6.3V X5R 01005
AIN3N — C1793 0.01UF 10% 6.3V X5R 01005

CODEC_AIN (MAKE_BASE=TRUE) — AIN1P, AIN1N, AIN4P, AIN4N
C1790 0.01UF 10% 6.3V X5R 01005

CODEC_MIC_BIAS_FILT (MAKE_BASE=TRUE) — MIC1_BIAS_FILT, MIC3_BIAS_FILT, MIC4_BIAS_FILT
C1791 0.01UF 10% 6.3V X5R 01005

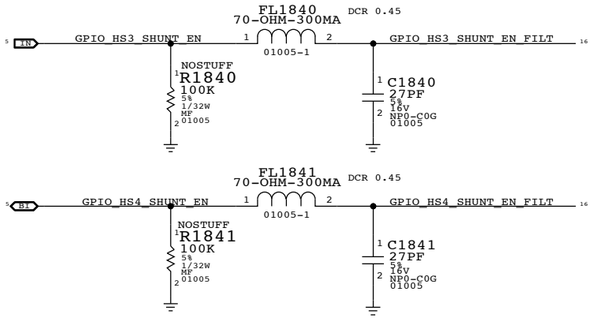
DIGITAL MIC
DMIC1_FF_SD — R1712 22 1/32W 5% MF 01005 — L81_DMIC1_FF_SD
DMIC1_FF_SCLK — R1713 22 1/32W 5% MF 01005 — L81_DMIC1_FF_SCLK

CRITICAL U1700 CS42L81-CWZR-A1 WLCSP SYM 2 OF 2

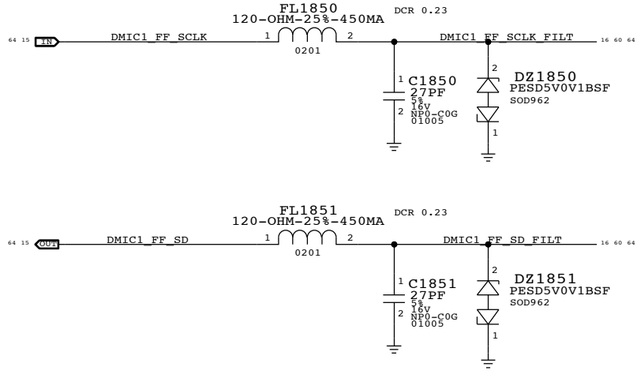
DMIC1_SD	B1	
DMIC1_SCLK	B2	
DMIC2_SD	B7	
DMIC2_SCLK	B6	NC_DMIC2_SCLK (NO_TEST=TRUE)
MCLK	C8	I2S0_CODEC_ASP_MCK_R
ASP_SCLK	A3	I2S0_CODEC_ASP_BCLK
ASP_LRCK	B3	I2S0_CODEC_ASP_LRCK
ASP_SDIN	A2	I2S0_CODEC_ASP_DOUT
ASP_SDOUT	A1	I2S0_CODEC_ASP_DIN — R1710 22 1/32W 5% MF 01005 — I2S0_CODEC_ASP_SDOUT
XSP_SCLK	B4	I2S1_CODEC_XSP_BCLK
XSP_LRCK_FSYNC	B5	I2S1_CODEC_XSP_LRCK
XSP_SDIN_DAC2_MUTE	A5	I2S1_CODEC_XSP_DOUT
XSP_SDOUT	A4	I2S1_CODEC_XSP_DIN — R1711 22 1/32W 5% MF 01005 — I2S1_CODEC_XSP_SDOUT
MBUS_REF	K5	L81_MBUS_REF
CS*	C5	SPI3_CODEC_CS_L
CCLK	A6	SPI3_CODEC_SCLK
CDIN	B8	SPI3_CODEC_MOSI
CDOUT	A7	SPI3_CODEC_MISO
INT*	B9	GPIO_CODEC2SOC_IRQ_L
WAKE*	B10	PMU_GPIO_CODEC_HS_INT_L
RESET*	C9	PMU_GPIO_CODEC_RST_L
GND0	C6	
GND1	D3	
GND2	D5	
GND3	D6	
GND4	D7	
GND5	D8	
GND6	E5	
GND7	E6	
GND8	E7	
GND9	F5	
GND10	F6	
GND11	F7	
GND12	F8	
GND13	G5	
GND14	G6	
GND15	G7	
GND16	H5	
GND17	H7	
GND18	J5	
TSTI0	C4	
TSTI1	C7	
TSTI2	D4	

=PP1V8_AUDIO
NOSTUFF R1740 1.00K 5% 1/32W MF 01005

SHUNT FILTERS



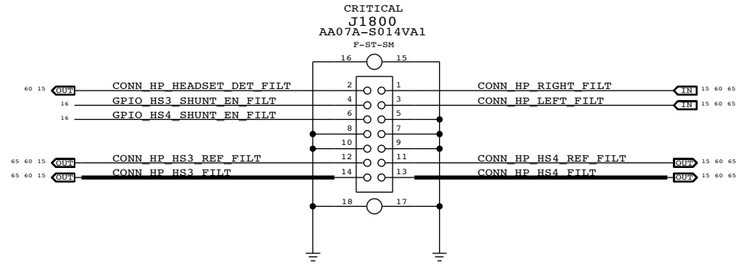
DMIC FILTERS



HP JACK B2B CONNECTOR

J1800 MATCHES AUDIO_JACK_FLEX_3.0.0 1/9/13

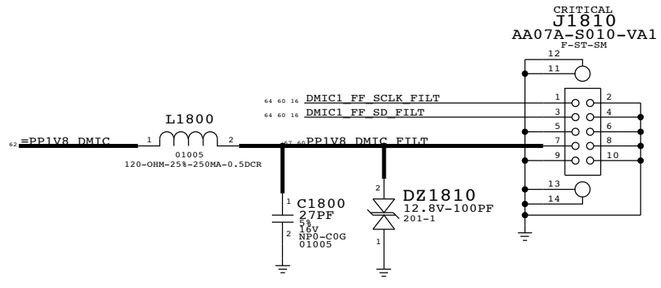
MLB: 516S1084
FLEX: 516S1085



MICROPHONE FLEX B2B CONNECTOR

J1810 MATCHES MIC_FLEX_2.0.0 1/7/13

MLB APN: 516S0899
FLEX APN: 516S0900



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0077	377S0111	?		?

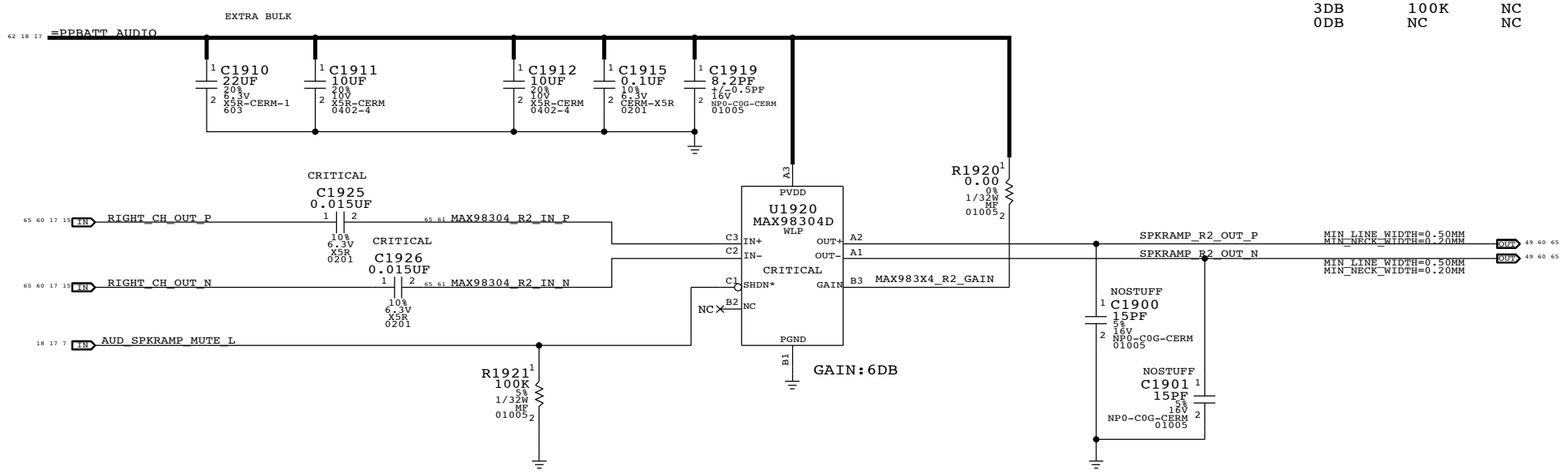
DZ1850,DZ1851

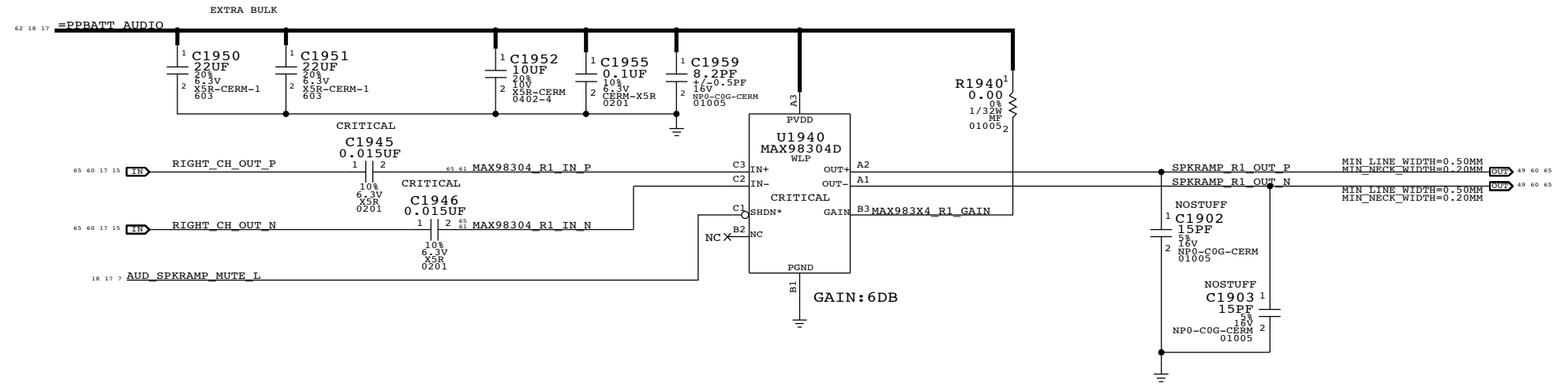
SPEAKER AMPLIFIER

APN:353S3445
TURN ON TIME: 3.5MS
TURN ON DELAY: ?MS

75HZ +/- XXX%

GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC





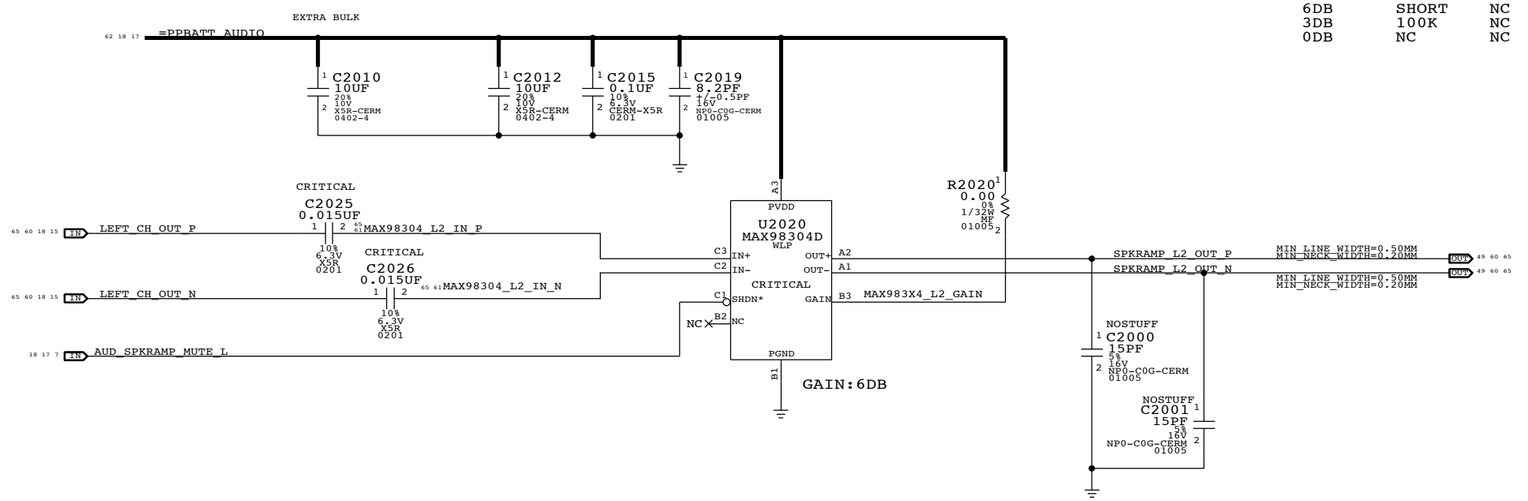
SPEAKER AMPLIFIER

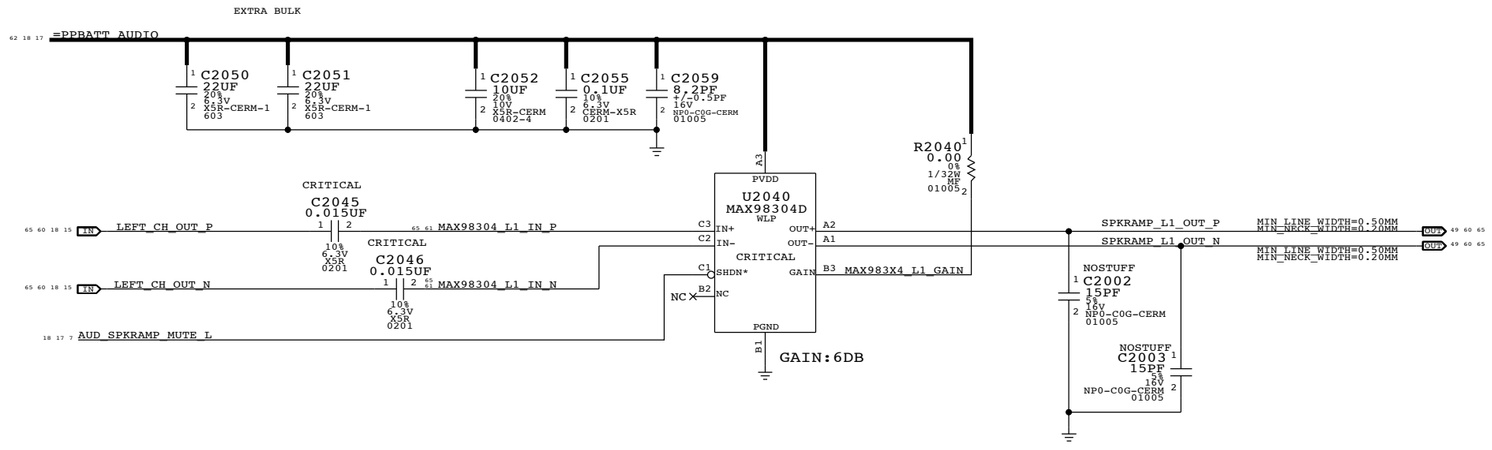
APN:353S3445

TURN ON TIME: 3.5MS

75HZ +/- XXX% TURN ON DELAY: ?MS

GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC

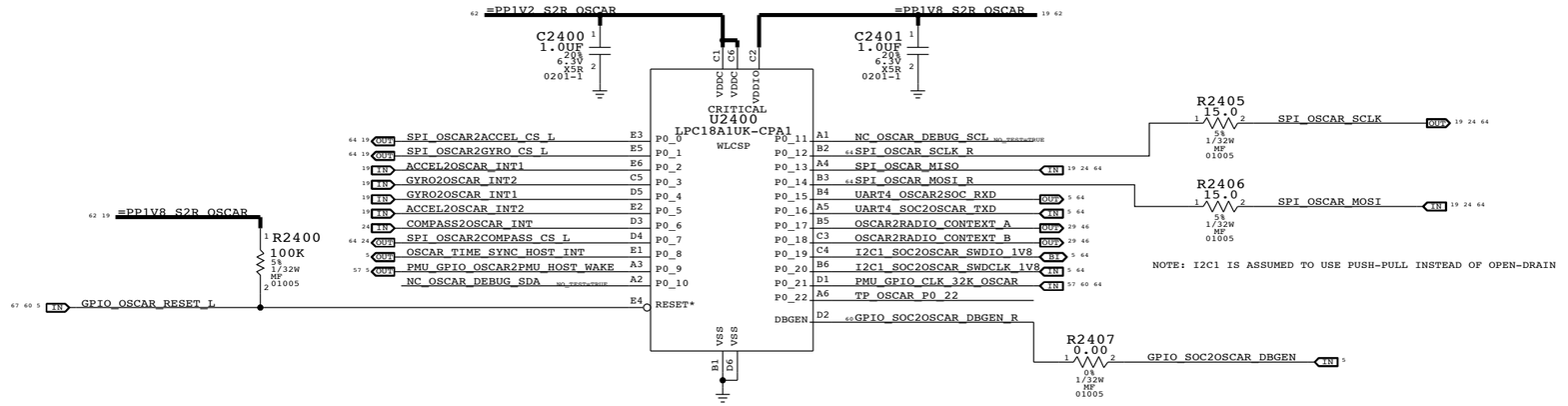




OSCAR

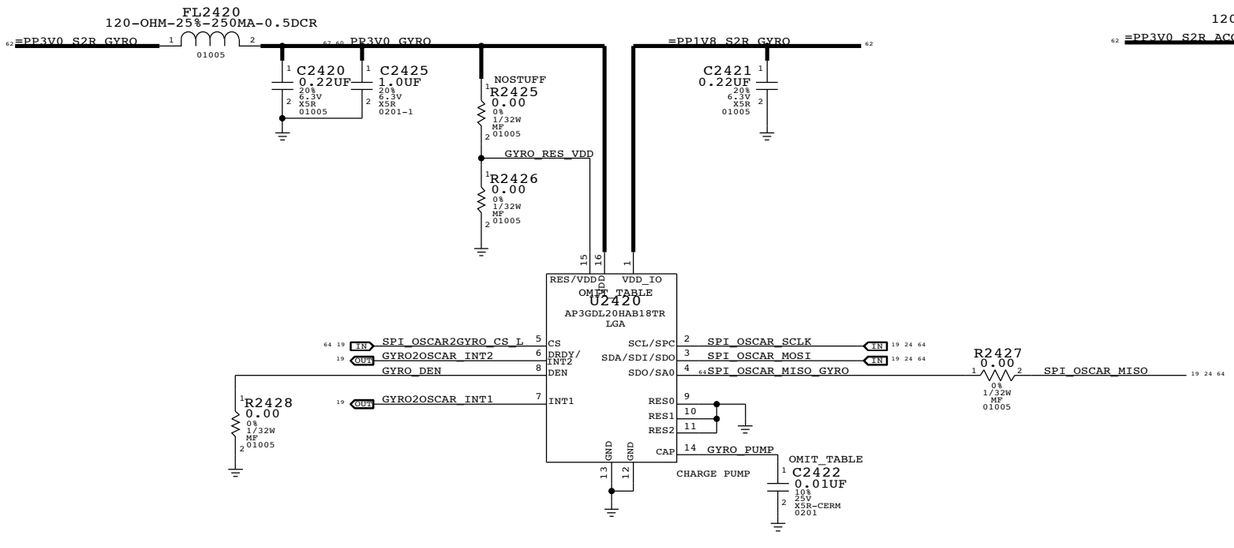
APN 337S4416 (A1)

OSCAR VDDIO = 1.8V HIBERNATE (NEED TO WAKE HOST)
OSCAR CORE = 1.2V HIBERNATE (NEED TO RUN IN S2R)

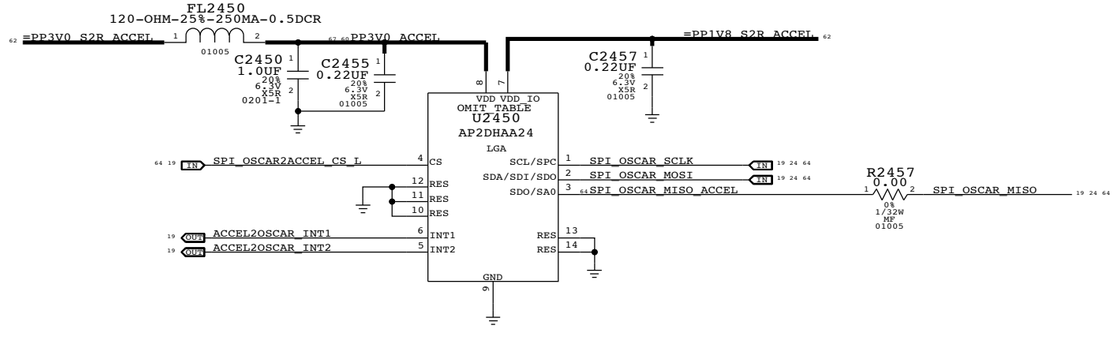


NOTE: I2C1 IS ASSUMED TO USE PUSH-PULL INSTEAD OF OPEN-DRAIN

GYRO



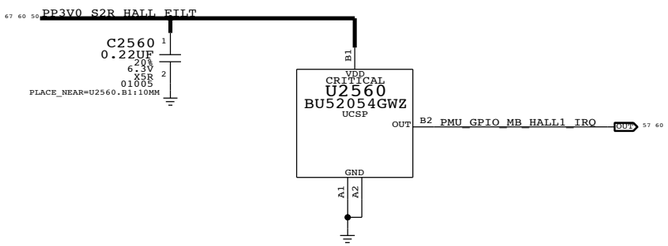
ACCELEROMETER



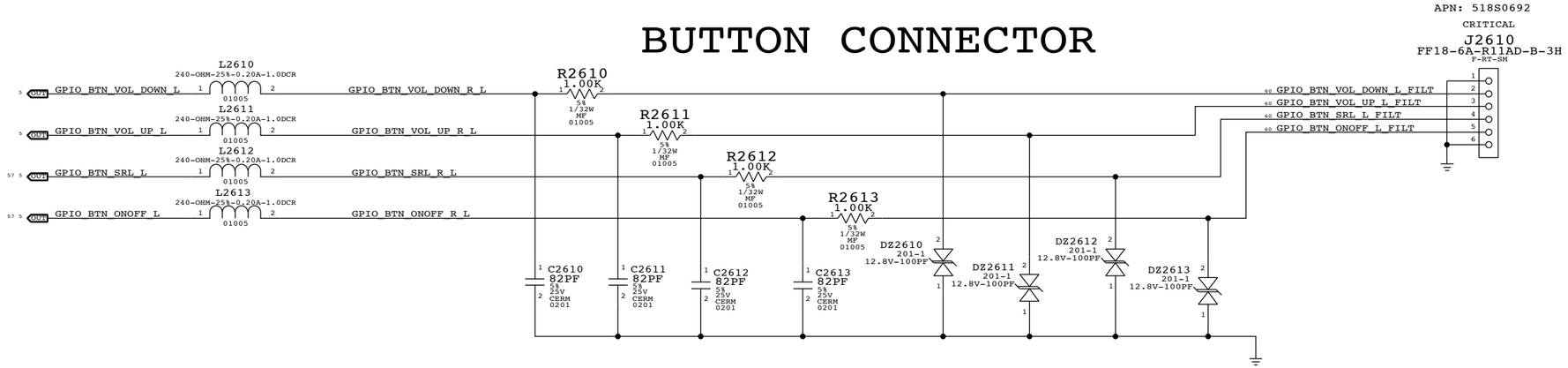
HALL EFFECT

BIPOLAR ONE OUTPUT APN 353S3687

C-PANEL HALL EFFECT SENSOR
(B-PANEL HALL EFFECT SENSOR ON HB)



BUTTON CONNECTOR



FRONT CAMERA CONNECTOR

J65 CAMERA CONNECTOR

APN:MLB 516S0876
APN:FLEX 516S0869

CRITICAL
J2700
503548-1820
F-ST-SM

64 60 22	I2C3_CAM_ALS_SCL_1V8_F	2	1	I2C3_CAM_ALS_SDA_1V8_F	22 60 64
60 22	GPIO_CAM_ALS2SOC_IRQ_L_F	4	3	ISP1_CAM_FRONT_CLK_F	22 60 64
67 60 22	PP3V0_ALS_FILT	6	5		
		8	7	ISP1_CAM_FRONT_SHUTDOWN_L_F	22 60 67
65 61 22	MIPI1C_CAM_FRONT_DATA_FILT_P<0>	10	9	ISP1_CAM_FRONT_SDA_F	22 60 64
65 61 22	MIPI1C_CAM_FRONT_DATA_FILT_N<0>	12	11	ISP1_CAM_FRONT_SCL_F	22 60 64
		14	13	PP2V9_AVDD_CAM_FRONT_FILT	22 60 67
65 61 22	MIPI1C_CAM_FRONT_CLK_FILT_P	16	15	GND_AVDD_CAM_FRONT	22 67
65 61 22	MIPI1C_CAM_FRONT_CLK_FILT_N	18	17	PP1V8_CAM_FRONT_FILT	22 60 67
		22	21		

62 =PP1V8_CAM_FRONT — L2780 80-OHM-25%-500MA 0201 — PP1V8_CAM_FRONT_FILT 22 60 67

- C2780 100PF 5% 16V NP0-C0G 01005
- C2781 1.0UF 20% 6.3V X5R 0201-1
- XW2780 SM — 67 GND_PP1V8_CAM_FRONT
- XW2781 SM

62 =PP2V9_CAM_FRONT — L2700 80-OHM-25%-500MA 0201 — PP2V9_AVDD_CAM_FRONT_FILT 22 60 67

- C2700 100PF 5% 16V NP0-C0G 01005
- C2701 1.0UF 20% 6.3V X5R 0201-1
- XW2700 SM — 67 GND_PP2V9_CAM_FRONT
- XW2701 SM — GND_AVDD_CAM_FRONT 22 67

62 =PP3V0_ALS — L2702 80-OHM-25%-500MA 0201 — PP3V0_ALS_FILT 22 60 67

- C2706 100PF 5% 16V NP0-C0G 01005
- C2707 1.0UF 20% 6.3V X5R 0201-1

CRITICAL
L2710

65 61 22 MIPI1C_CAM_FRONT_CLK_FILT_P — 2 — 3 — MIPI1C_CAM_FRONT_CLK_P — OUT 7 61 65
65 61 22 MIPI1C_CAM_FRONT_CLK_FILT_N — 1 — 4 — MIPI1C_CAM_FRONT_CLK_N — OUT 7 61 65
TCM0605-1
90-OHM-50MA

CRITICAL
L2711

65 61 22 MIPI1C_CAM_FRONT_DATA_FILT_P<0> — 2 — 3 — MIPI1C_CAM_FRONT_DATA_P<0> — OUT 7 61 65
65 61 22 MIPI1C_CAM_FRONT_DATA_FILT_N<0> — 1 — 4 — MIPI1C_CAM_FRONT_DATA_N<0> — OUT 7 61 65
TCM0605-1
90-OHM-50MA

64 61 13 5 IN I2C3_SCL_1V8 — FL2730 70-OHM-300MA DCR 0.45 01005-1 — I2C3_CAM_ALS_SCL_1V8_F 22 60 64

- C2730 27PF 5% 16V NP0-C0G 01005

64 61 13 5 IN I2C3_SDA_1V8 — FL2731 70-OHM-300MA DCR 0.45 01005-1 — I2C3_CAM_ALS_SDA_1V8_F 22 60 64

- C2731 27PF 5% 16V NP0-C0G 01005

67 7 IN ISP1_CAM_FRONT_SHUTDOWN_L — FL2740 70-OHM-300MA DCR 0.45 01005-1 — ISP1_CAM_FRONT_SHUTDOWN_L_F 22 60 67

- R2740 100K 5% 1/32W MF 01005
- C2740 27PF 5% 16V NP0-C0G 01005

64 7 IN ISP1_CAM_FRONT_SCL — FL2750 70-OHM-300MA DCR 0.45 01005-1 — ISP1_CAM_FRONT_SCL_F 22 60 64

- C2750 27PF 5% 16V NP0-C0G 01005

64 7 IN ISP1_CAM_FRONT_SDA — FL2751 70-OHM-300MA DCR 0.45 01005-1 — ISP1_CAM_FRONT_SDA_F 22 60 64

- C2751 27PF 5% 16V NP0-C0G 01005

64 7 IN ISP1_CAM_FRONT_CLK — FL2760 150OHM-25%-200MA-0.7DCR DCR 0.70 01005 — ISP1_CAM_FRONT_CLK_F 22 60 64

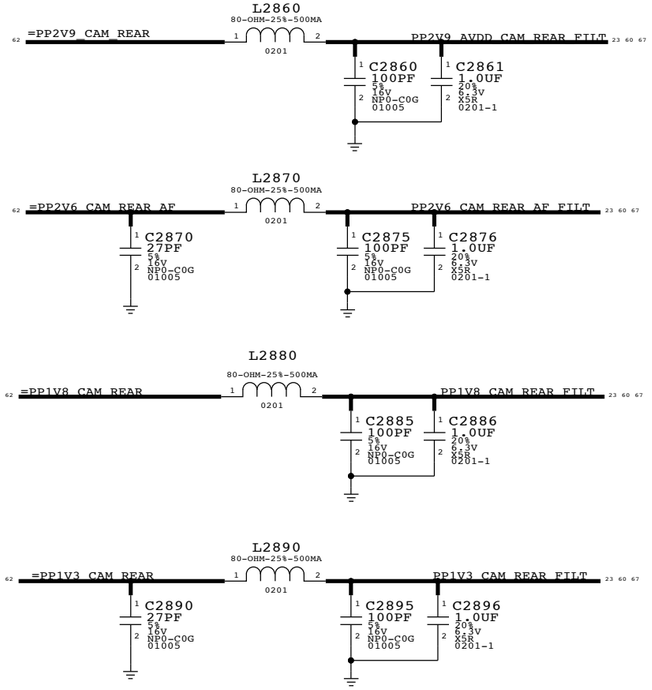
- C2760 56PF 5% 16V NP0-C0G 01005

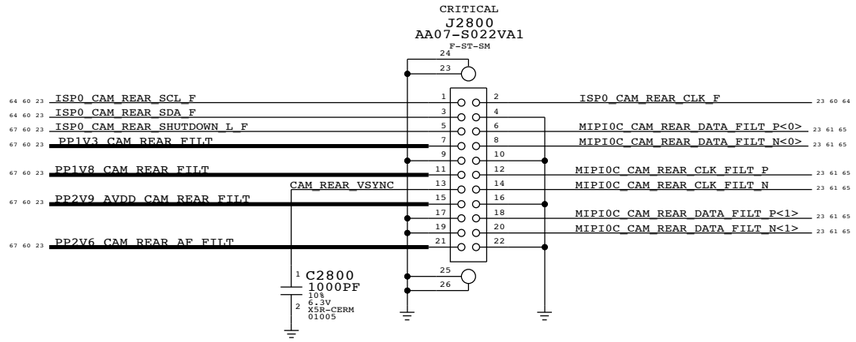
5 IN GPIO_CAM_ALS2SOC_IRQ_L — FL2770 70-OHM-300MA DCR 0.45 01005-1 — GPIO_CAM_ALS2SOC_IRQ_L_F 22 60

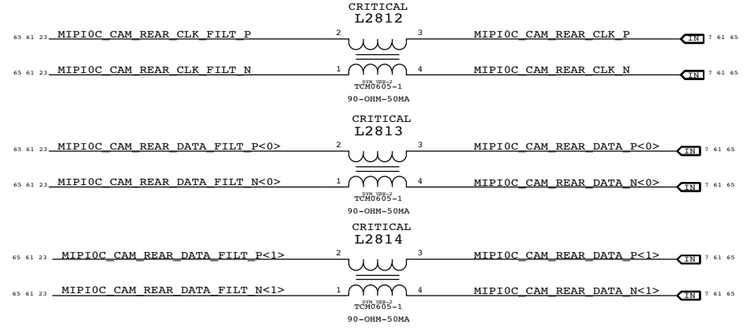
REAR CAMERA CONNECTOR

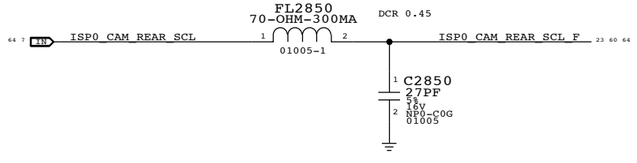
FLEX: 516S0974

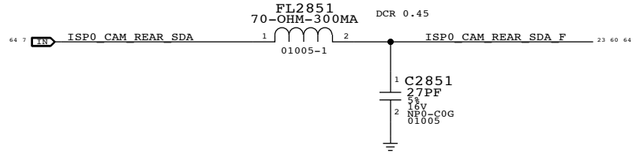
MLB: 516S0973

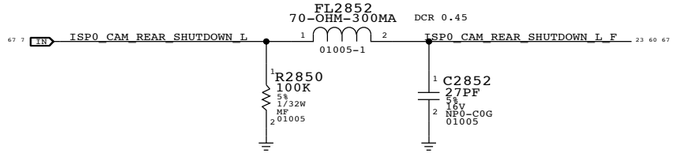


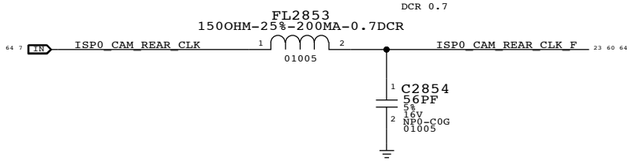






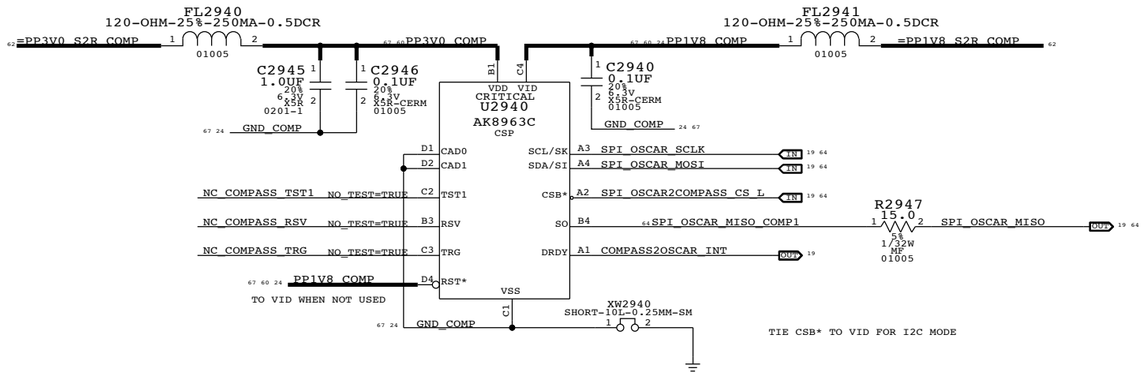






COMPASS

APN 338S1014



AP INTERFACE & DEBUG CONNECTOR

PROBE POINTS

PP3000 P4MM SM — 1 BB_ERROR_FLAG — 29 68
PP3001 P4MM SM — 1 SLEEP_CLK_32K — 27 28 68
PP3002 P4MM SM — 1 PMIC_SSBI — 27 28 68
PP3003 P4MM SM — 1 19P2M_MDM — 27 28 68
PP3008 P4MM SM — 1 WTR_SSBI_TX_GPS — 29 30
PP3009 P4MM SM — 1 WTR_SSBI_PRX_DRX — 29 30
PP3010 P4MM SM — 1 WTR_RX_ON — 29 30 68
PP3011 P4MM SM — 1 WTR_RF_ON — 29 30 68
PP3012 P4MM SM — 1 UART_WLAN2BB_LTE_COEX — 29 46
PP3013 P4MM SM — 1 UART_BB2WLAN_LTE_COEX — 29 46

DEBUG CONNECTOR

=PPBATT_VCC_BB IN 26 34 35 36 37 38 39 40 62

NOSTUFF
J3303
AXE654124
M-ST-SM

	56	55	
	2	1	
	4	3	
	6	5	
60 27 OUT PS_HOLD_PMIC	8	7	GPIO_SOC2BB_RST_L OUT 5 27 60 67
60 27 5 OUT GPIO_SOC2BB_RADIO_ON_L	10	9	PP_SMPS3_MSME_1V8 IN 25 26 28 29 31 60
67 60 57 27 OUT PMU_GPIO_PMU2BBPMU_RST_L	12	11	RESET_SOC_L OUT 4 13 47 57 60 61 67
68 28 27 IN PMIC_RESOUT_L	14	13	
	16	15	UART3_BB2SOC_TX IN 5 29 47 64
	18	17	GPIO_DEBUG_LED IN 29
	20	19	
	22	21	UART3_SOC2BB_TX OUT 5 29 47 64
67 61 28 OUT DEBUG_RST_L	24	23	UART3_BB2SOC_RTS_L IN 5 29 64
64 61 28 5 OUT BB_JTAG_TMS	26	25	UART3_SOC2BB_RTS_L OUT 5 29 64
64 61 28 5 OUT BB_JTAG_TRST_L	28	27	
64 61 28 5 OUT BB_JTAG_TCK	30	29	
64 61 28 5 IN BB_JTAG_TDO	32	31	
64 61 28 5 OUT BB_JTAG_TDI	34	33	PMU_GPIO_BB_VBUS_DET OUT 28 57 61 67
28 OUT BB_JTAG_RTCLK	36	35	
	38	37	
68 29 25 OUT LAT_SW1_CTL — GPIO48/BOOT_CONFIG_6	40	39	
	42	41	
68 40 29 OUT 2G_FEM_S1 — GPIO54/BOOT_CONFIG_0	44	43	
60 57 29 IN PMU_GPIO_BB2PMU_HOST_WAKE	46	45	HSIC2_BB2SOC_DEVICE_RDY IN 5 29 64
68 40 29 25 OUT 2G_FEM_S4 — GPIO53/BOOT_CONFIG_1	48	47	
29 OUT GPIO_51 — GPIO51/BOOT_CONFIG_3	50	49	GPIO_BB2SOC_RESET_DET_L IN 5 29 67
	52	51	HSIC2_SOC2BB_HOST_RDY IN 5 29 64
	54	53	
	58	57	

XW3002 SHORT-10L-0.25MM-SM
64 47 BI USB_BB_N
64 61 28 BI USB_BB_DEBUG_N
64 61 28 BI USB_BB_DEBUG_P

XW3003 SHORT-10L-0.25MM-SM
64 47 BI USB_BB_P

PP_SMPS3_MSME_1V8 25 26 28 29 31 60

NOSTUFF R3002 10K 5% 1/32W MF 01005
NOSTUFF R3003 10K 5% 1/32W MF 01005

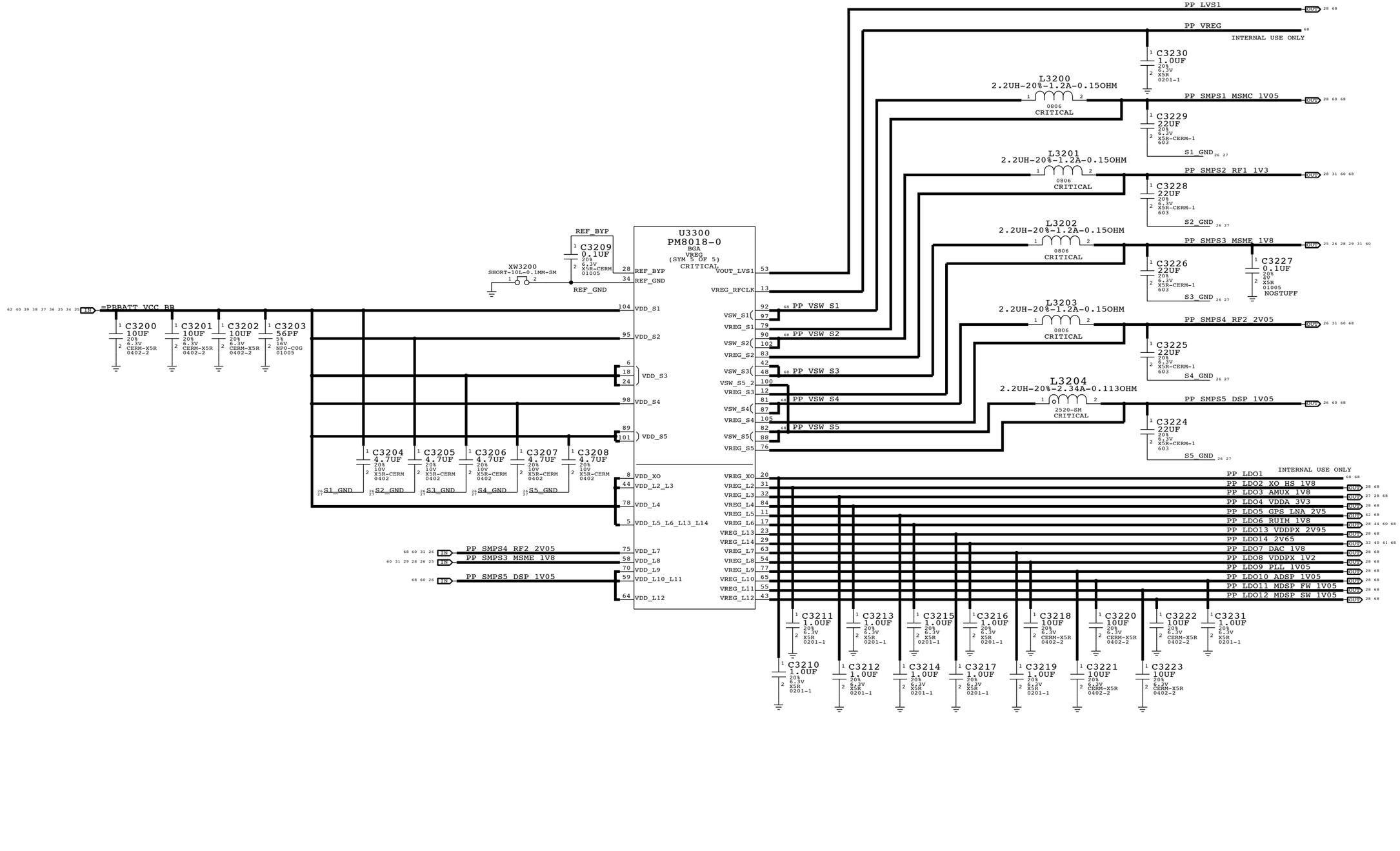
68 29 25 LAT_SW1_CTL — GPIO48/BOOT_CONFIG_6
68 40 29 25 2G_FEM_S4 — GPIO53/BOOT_CONFIG_1

BOOT OPTIONS	BOOT_CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION 6 (47)	5 (48)	4 (49)	3 (50)	2 (51)	1 (52)	0 (53)	(54)	(55)
BOOT_DEFAULT_OPTION	0X00	X	0	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0X01	X	1	0	0	0	0	0	1	X
BOOT_HSIC_OPTION	0X02	X	1	0	0	0	0	1	0	X
BOOT_USB_OPTION	0X03	X	1	0	0	0	0	1	1	X
ENABLE SAHARA PROTOCOL	0X08	X	1	0	0	1	0	X	X	X

J3002
MM4829-2702
F-ST-SM
NOSTUFF 1 — HSIC2_BB_DATA — 4 28 61 64
2 3 4

J3001
MM4829-2702
F-ST-SM
NOSTUFF 1 — HSIC2_BB_STB — 4 28 61 64
2 3 4

BASEBAND PMU (1 OF 2)

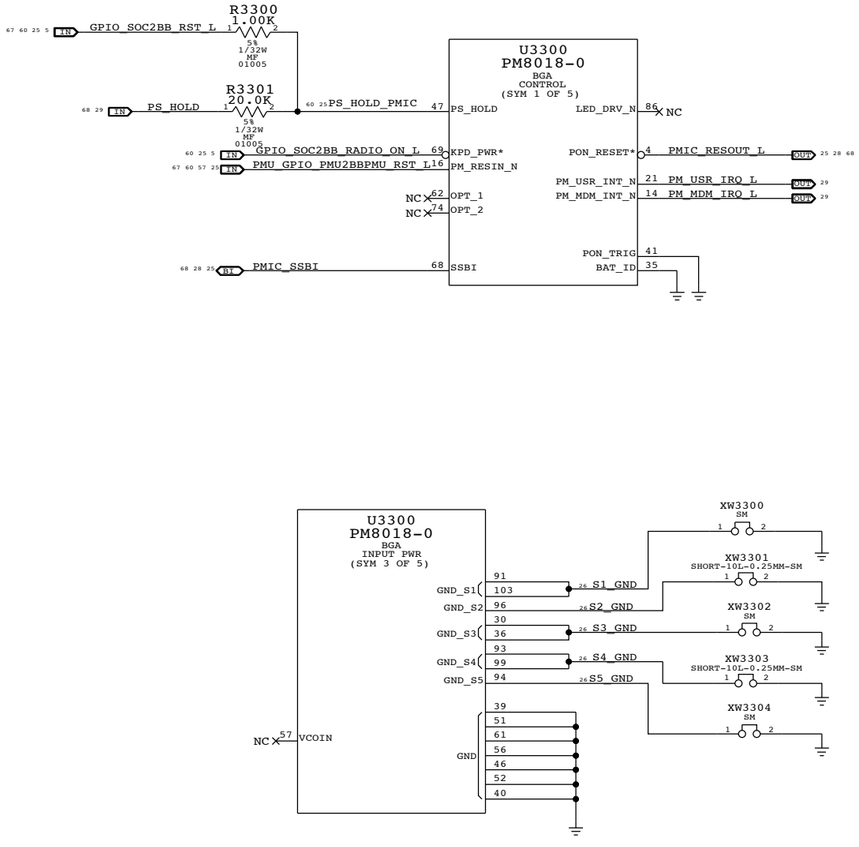


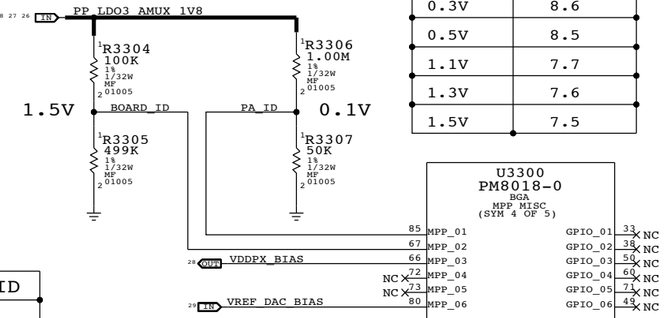
BASEBAND PMU (2 OF 2)

BOARD_ID	REVISION
0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT

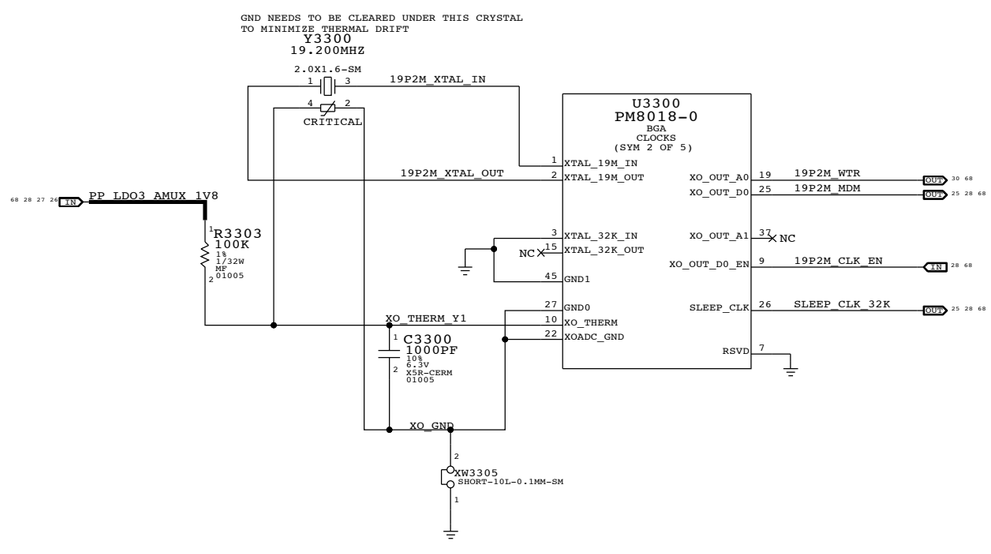
BB GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX

PA_ID	MAV VER
0.1V	8.7
0.3V	8.6
0.5V	8.5
1.1V	7.7
1.3V	7.6
1.5V	7.5





PA THERMISTOR REMOVED TO MATCH N41, AP SECTION
NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.



BASEBAND (1 OF 2)

PP_SMPS1_MSMC_1V05 — C3400 1.0UF, C3401 1.0UF, C3402 1.0UF, C3403 1.0UF, C3404 1.0UF (20% 6.3V X5R 0201-1)

PP_LDO8_VDDPX_1V2 — C3431 1.0UF, C3432 0.22UF (20% 6.3V X5R 01005)

PP_LDO4_VDDA_3V3 — C3433 1.0UF, C3434 0.22UF (20% 6.3V X5R 0201)

PP_LDO9_PLL_1V05 — C3405 1.0UF, C3406 1.0UF, C3407 1.0UF, C3408 1.0UF (20% 6.3V X5R 0201-1)

PP_LDO10_ADSP_1V05 — C3413 1.0UF, C3414 1.0UF (20% 6.3V X5R 0201-1)

PP_LDO11_MDSP_FW_1V05 — C3418 1.0UF, C3419 1.0UF, C3420 1.0UF (20% 6.3V X5R 0201-1)

PP_SMPS3_MSME_1V8 — C3409 1.0UF, C3410 1.0UF (20% 6.3V X5R 0201-1)

PP_SMPS3_MSME_1V8 — C3411 1.0UF, C3412 1.0UF (20% 6.3V X5R 0201-1)

PP_LDO12_MDSP_SW_1V05 — C3415 1.0UF, C3416 1.0UF, C3417 1.0UF (20% 6.3V X5R 0201-1)

U3400 MDM9615M BGA (5 OF 6) PWR

PP_SMPS1_MSMC_1V05 — C3421 1.0UF (20% 6.3V X5R 0201-1)

VDD_CORE: F8, F9, F12, F13, F14, G9, G12, H9, H12, J8, J9, J12, J13, K8, K9, K12, K13, L8, L9, L12, L13, M8, M9, M12, M13, N8, N9, N12, N13, P9, P12, R9, R12, T8, T9

VDD_MEM: C17, C18, E17, F17, G7, G8, G13, G14, H7, H8, H13, H14, P7, P8, P13, P14, R7, R8, R13, R14

VDD_P1: A14, A19, F21, M1, M21

VDD_P2: K21 — PP_LDO13_VDDPX_2V95

VDD_DDR: AA20, B19, F20, M20 — PP_SMPS3_MSME_1V8

VDD_ADSP: C5, C6, E6, E7, F5 — PP_LDO10_ADSP_1V05

VDD_MDSP_FW: T15, T16, T17, U14, U15, U16, U17, U19, T19 — PP_LDO11_MDSP_FW_1V05

VDD_MDSP_SW: N15, N16, N17, N19, P15, P16, P17, P19 — PP_LDO12_MDSP_SW_1V05; PP_LVS1; R3400 470K (5% 1/32W MF 01005)

VDD_QFUSE_PRG: B13

VDD_USB_1P8: E12 — PP_LDO2_XO_HS_1V8; C3422 1.0UF (20% 6.3V X5R 0201-1)

VDD_USB_3P3: E10 — PP_LDO4_VDDA_3V3

VDD_HVPAD_BIAS: E16 — VDDPX_BIAS; C3423 0.1UF (20% 4V X5R 01005 NOSTUFF)

VDD_PLL1: K17 — PP_LDO9_PLL_1V05

VDD_PLL2: L17 — PP_LDO3_AMUX_1V8

VDD_A2: U6, U7 — PP_LDO7_DAC_1V8

GND: AA11, AA18

VDD_A1: W9, AA7 — PP_SMPS2_RF1_1V3; C3424 1.0UF, C3425 1.0UF (20% 6.3V X5R 0201-1)

GND: AA15

VDD_P3: A15, G1, G21, L1, U1, W19 — PP_SMPS3_MSME_1V8; C3426 1.0UF (20% 6.3V X5R 0201-1)

VDD_P4: A2 — PP_LDO6_PHIM_1V8

VDD_P5: A3 — PP_SMPS3_MSME_1V8

VDD_P6: A7 — PP_LDO8_VDDPX_1V2

VDD_P7: A11 — PP_SMPS3_MSME_1V8

U3400 MDM9615M BGA (6 OF 6) GND CRITICAL

GND: A21, AA1, AA21, B2, B7, B11, B14, B15, C19, F6, F7, F10, F15, F16, F19, G2, G6, G10, G11, G15, G16, G17, G20, H6, H10, H11, H15, H16, J6, J7, J10, J11, J14, J15, K6, K7, K10, K11, K14, K15, K20, L2, L6, L7, L10, L11, L14, L15, M6, M7, M10, M11

GND: M14, M15, M16, M17, M19, N6, N7, N10, N11, N14, P6, P10, P11, R6, R10, R11, R15, R16, R17, R19, T10, T12, T13, T14, U2, V19

GND_ANA: F11, J16, K16, L16, T6, T7, T11, U9, U12, W7, W14, Y7, Y11, Y15, Y18, U13, W13

U3400 MDM9615M BGA (2 OF 6) EBI1_EBI2

EBI1_CAL — C21 EBI1_CAL — R3403 240 (1% 1/32W MF 01005)

NC	G21 EBI2_NAND_CS*	EBI2_AD_0 J20	NC
NC	K19 EBI2_OE*	EBI2_AD_1 J19	NC
NC	G20 EBI2_WE*	EBI2_AD_2 G19	NC
NC	J19 EBI2_BUSY*	EBI2_AD_3 H20	NC
		EBI2_AD_4 J21	NC
		EBI2_AD_5 H19	NC
NC	G20 EBI2_CLE*	EBI2_AD_6 H21	NC
NC	K20 EBI2_ALE*	EBI2_AD_7 E21	NC

U3400 MDM9615M BGA (1 OF 6) DIGITAL

PMIC_RESOUT_L	Y20	RESIN*	RESOUT* U20 NC
DEBUG_RST_L	Y4	SRST*	
SLEEP_CLK_32K	AA19	SLEEP_CLK	
BB_JTAG_TCK	Y3	TCK	TDO AA3 BB_JTAG_TDO (MUX)
BB_JTAG_TDI	AA2	TDI	RTCK Y2 BB_JTAG_RTCLK (MUX)
BB_JTAG_TMS	W4	TMS	HSIC_CAL A8 50_HSIC_CAL — R3402 240 (1% 1/32W MF 01005)
BB_JTAG_TRST_L	AA4	TRST*	HSIC_DATA C7 HSIC2_BB_DATA (BI)
TP_BB_TEST_MODE_0	W20	MODE_0	HSIC_STB B8 HSIC2_BB_STB (BI)
TP_BB_TEST_MODE_1	Y19	MODE_1	
19P2M_MDM	V20	CXO	
19P2M_CLK_EN	U21	CXO_EN	
PMIC_SSBI	Y21	SSBI_PMIC	
USB_BB_DEBUG_P	C11	USB_HS_DP	
USB_BB_DEBUG_N	E11	USB_HS_DM	
RREFEXT	A12	USB_HS_REXT	
	C12	USB_HS_ID	NCX
PMU_GPIO_BB_VBUS_DET	B12	USB_HS_SYSCLK	
	C10	USB_HS_VBUS	

R3401 200 (1% 1/32W MF 01005)

DNC: E8, C8, B9, A9 — NC

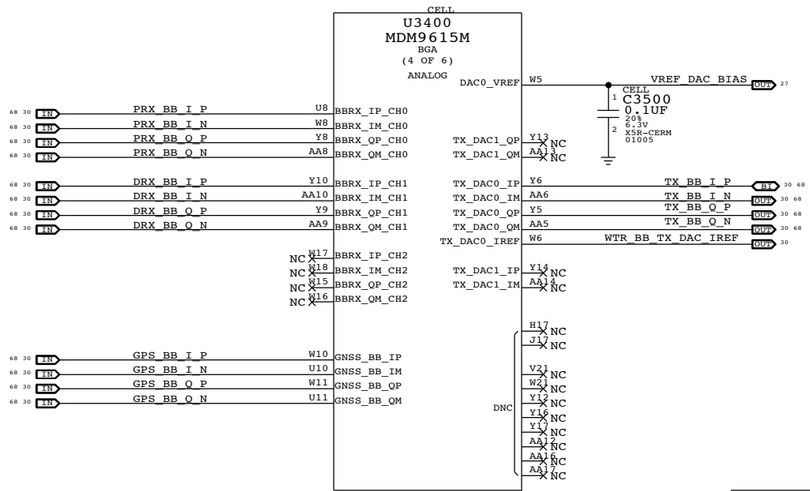
DNC: E9, C9, B10, A10 — NC

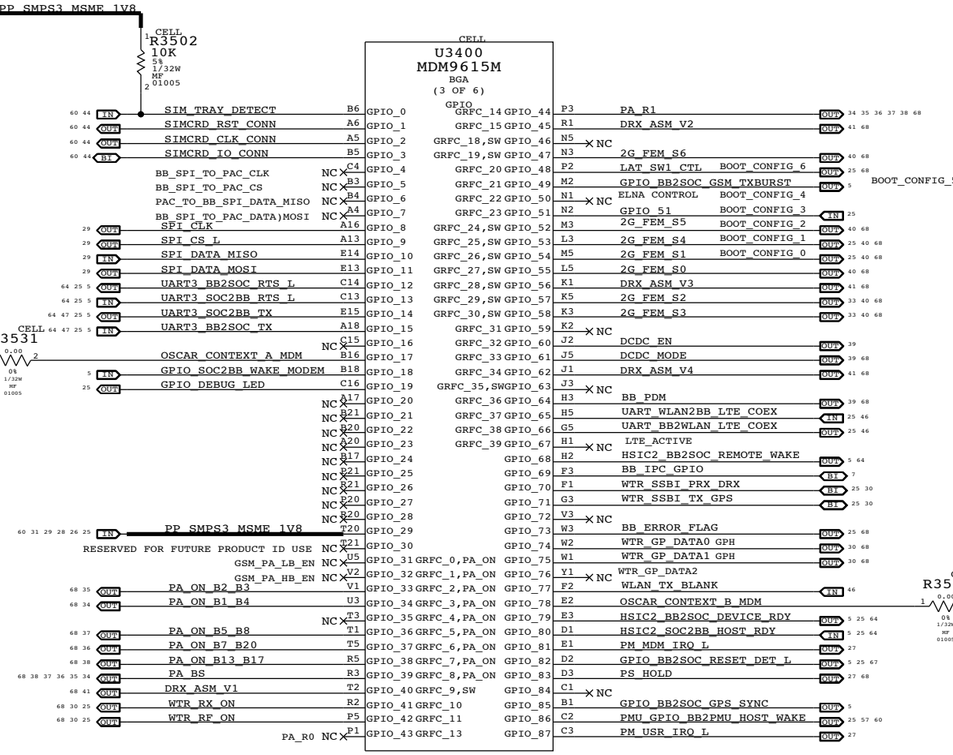
SDC1_CMD K19 NC; SDC1_CLK L21 NC

SDC1_DATA0 L19 NC; SDC1_DATA1 L20 NC; SDC1_DATA2 N20 NC; SDC1_DATA3 N21 NC

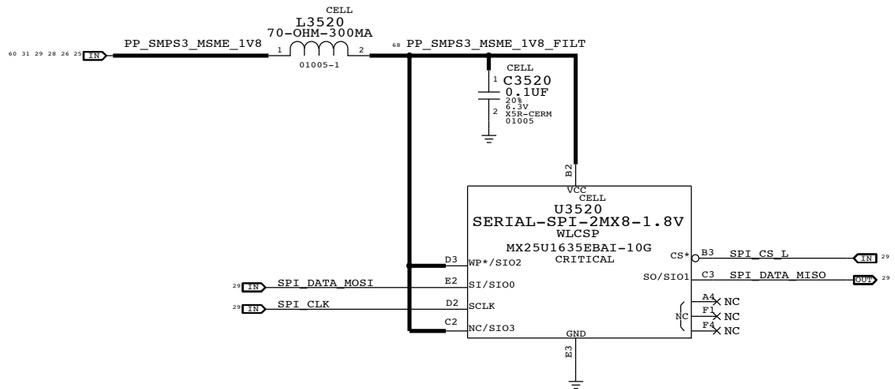
BASEBAND (2 OF 2)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.





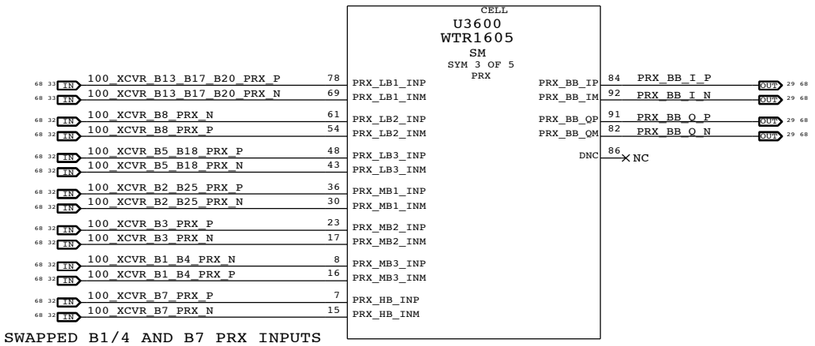
GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX



RF TRANSCEIVER (1 OF 2)

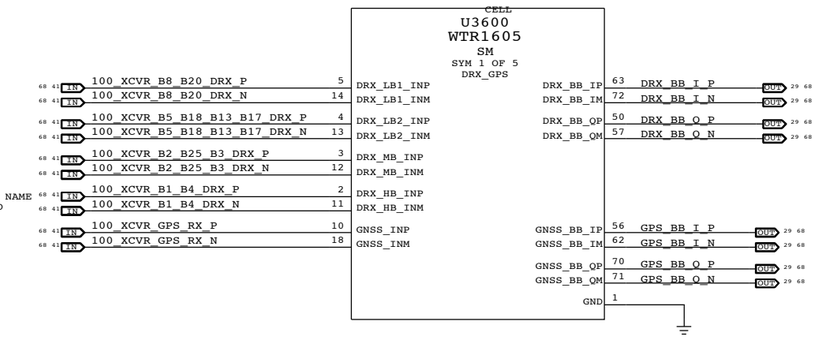
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

PRX TRANSCEIVER RF AND IQ PORTS



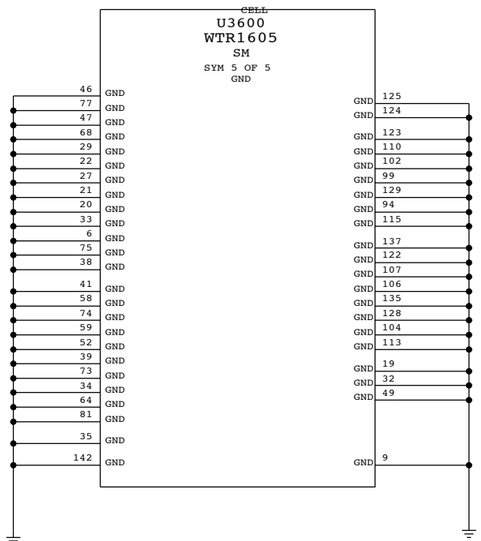
SWAPPED B1/4 AND B7 PRX INPUTS

DRX TRANSCEIVER RF AND IQ PORTS

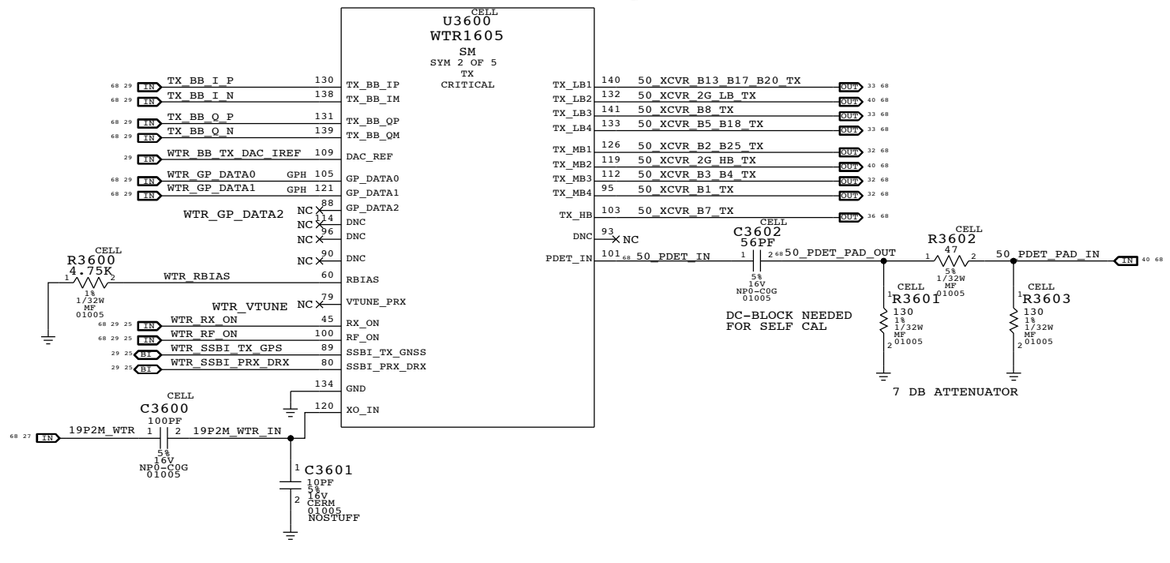


B7 DIFF PAIR NET NAME TO BE UPDATED

TRANSCEIVER GROUND CONNECTIONS



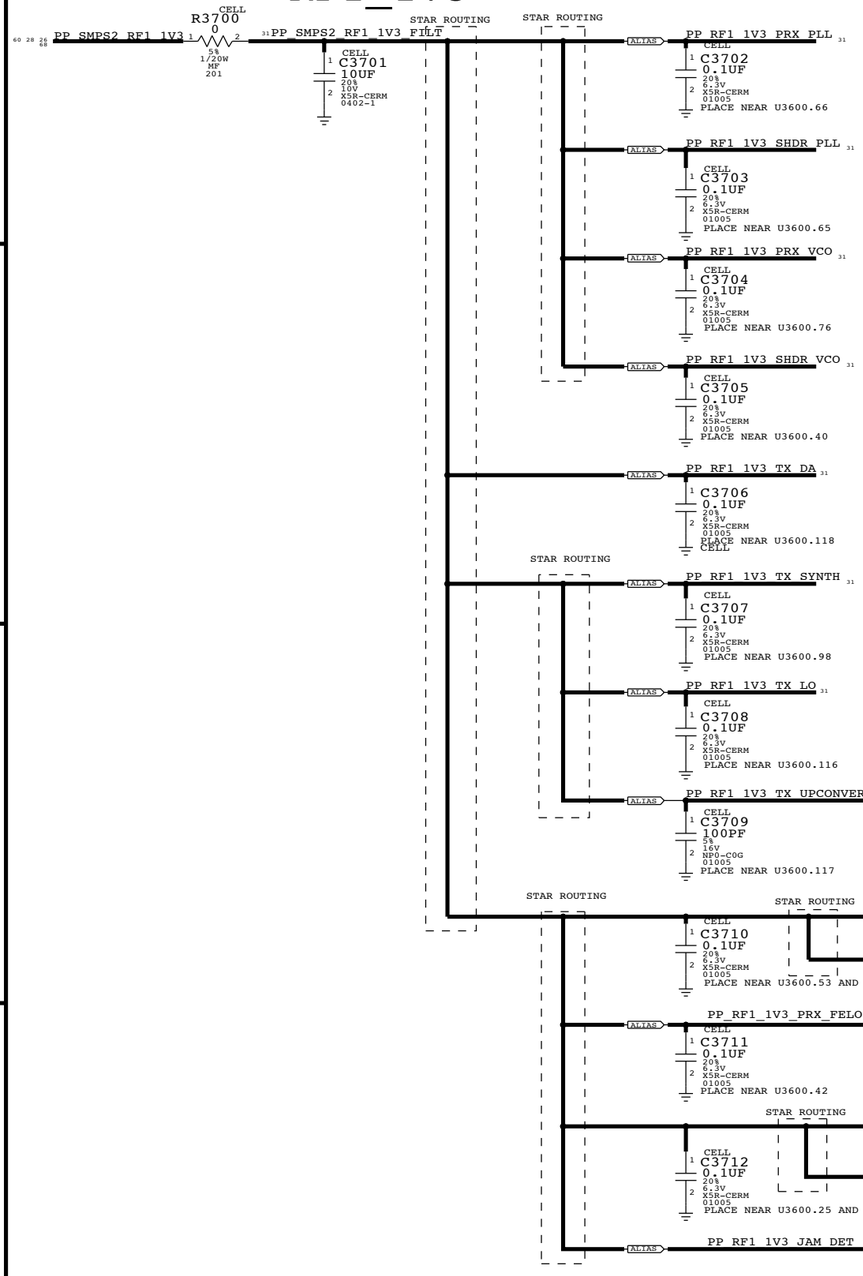
TRANSCEIVER PHASE CONTROL, TX RF & IQ PORTS



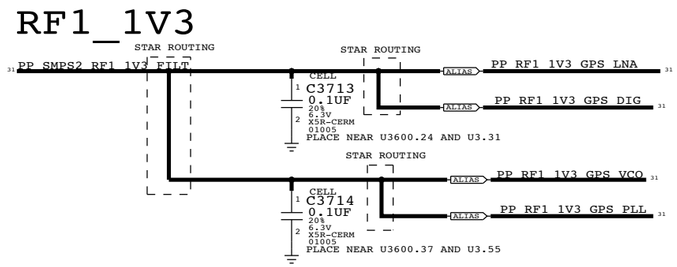
RF TRANSCEIVER (2 OF 2)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

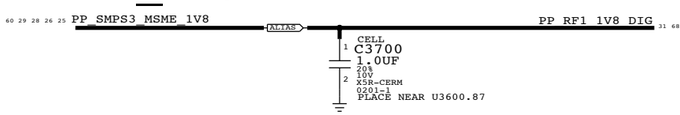
RF1_1V3



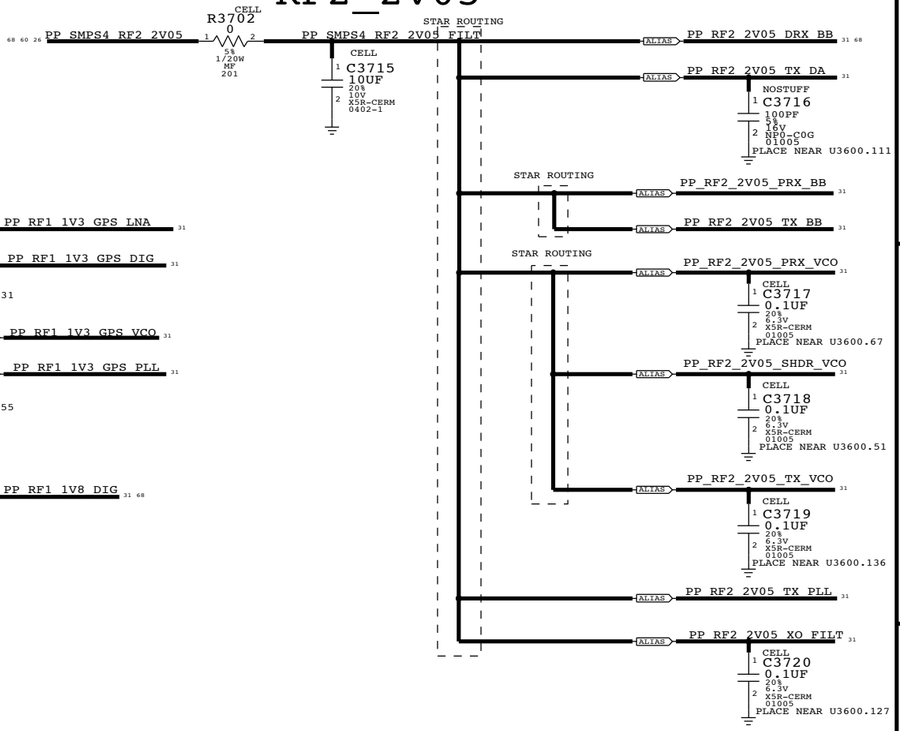
RF1_1V3



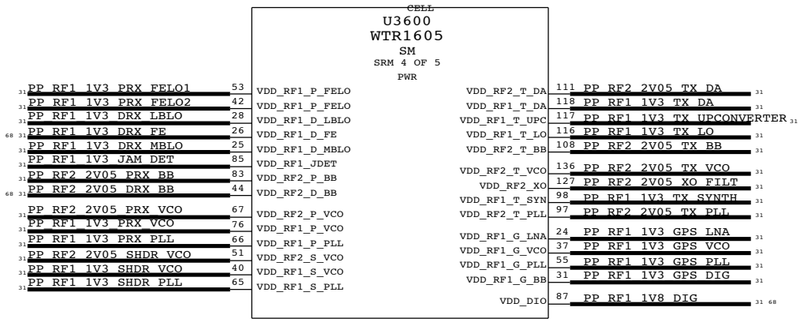
RF1_1V8



RF2_2V05

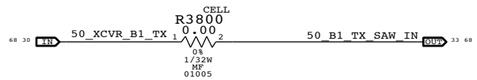


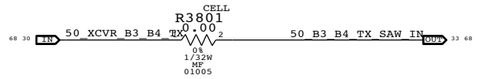
TRANSCEIVER POWER CONNECTIONS

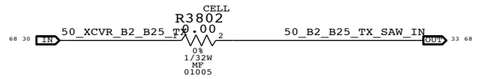


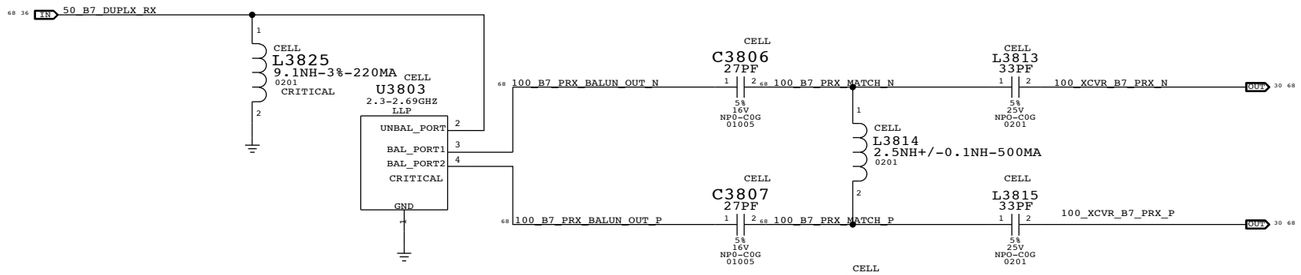
TRANSCEIVER TX AND RX MATCHING NETWORKS

TX MATCHING NETWORKS

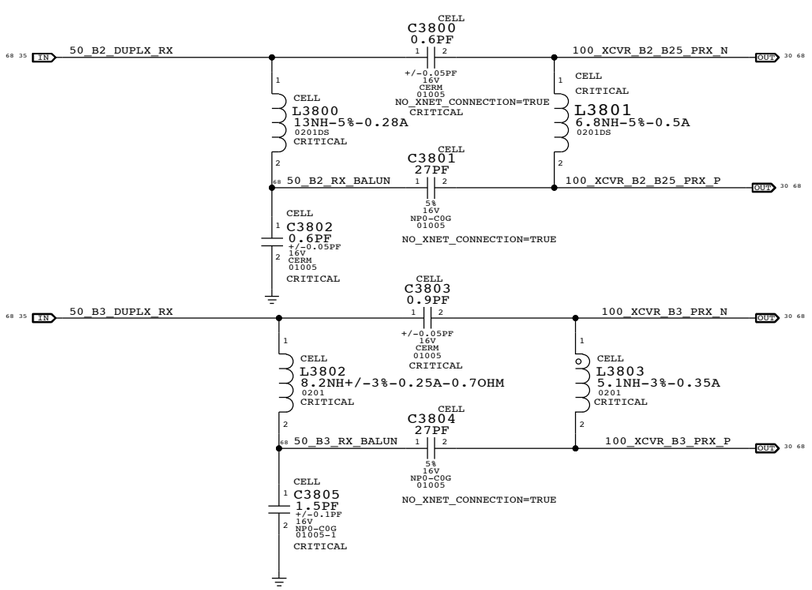


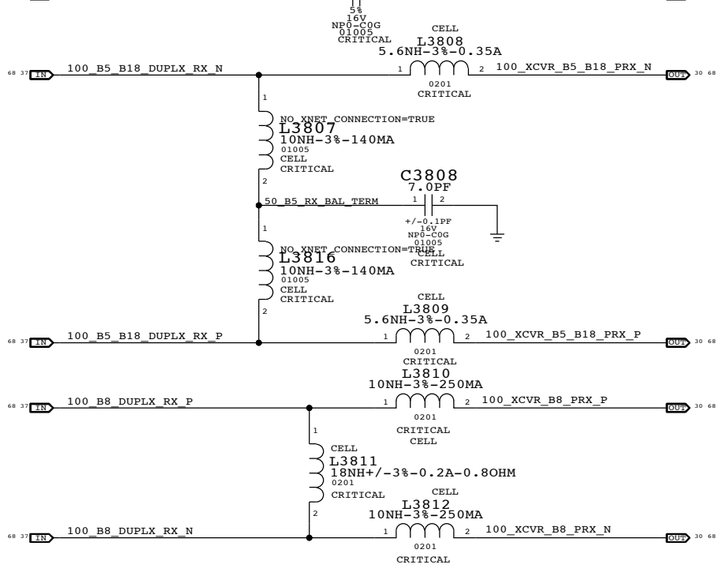






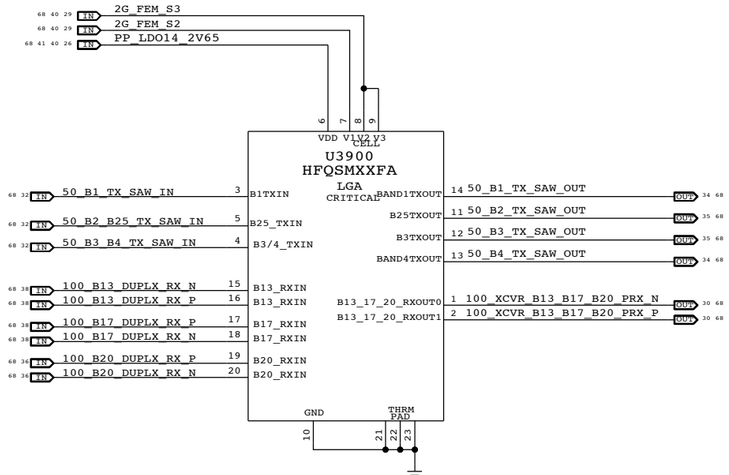
RX MATCHING NETWORKS





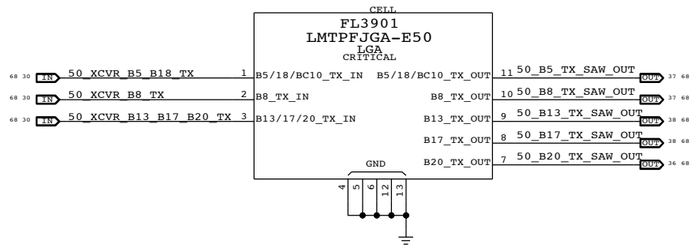
SAW BANK

HB TX SAW BANK +
B13/B17/B20 DP6T SWITCH AND MATCHING

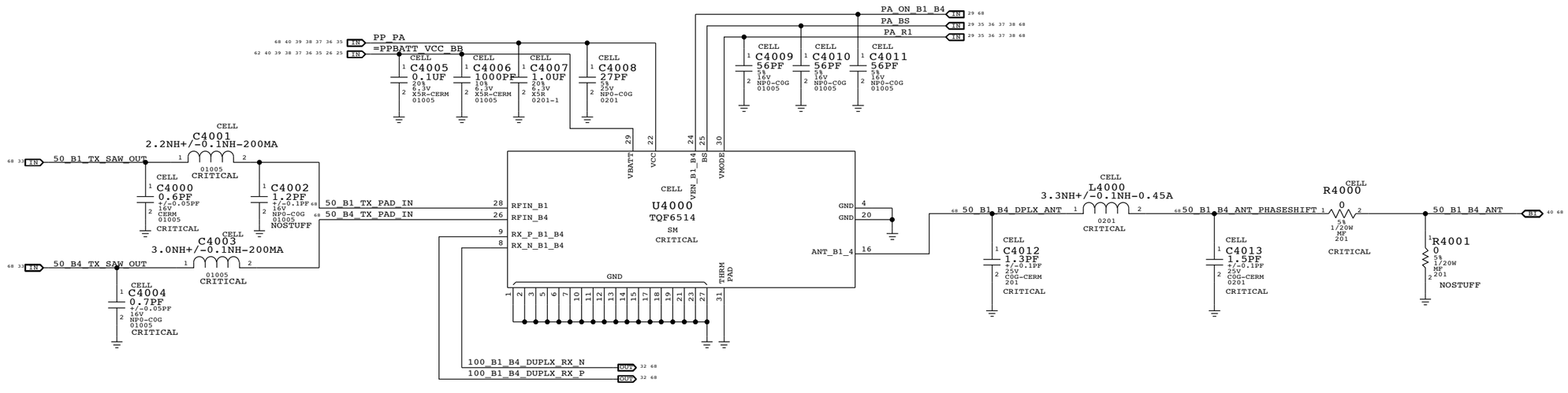


BAND	V3=V2	V1
B3 TX	HIGH	X
B4 TX	LOW	X
B13 RX	HIGH	HIGH
B17 RX	HIGH	LOW
B20 RX	LOW	HIGH

LB TX SAW BANK

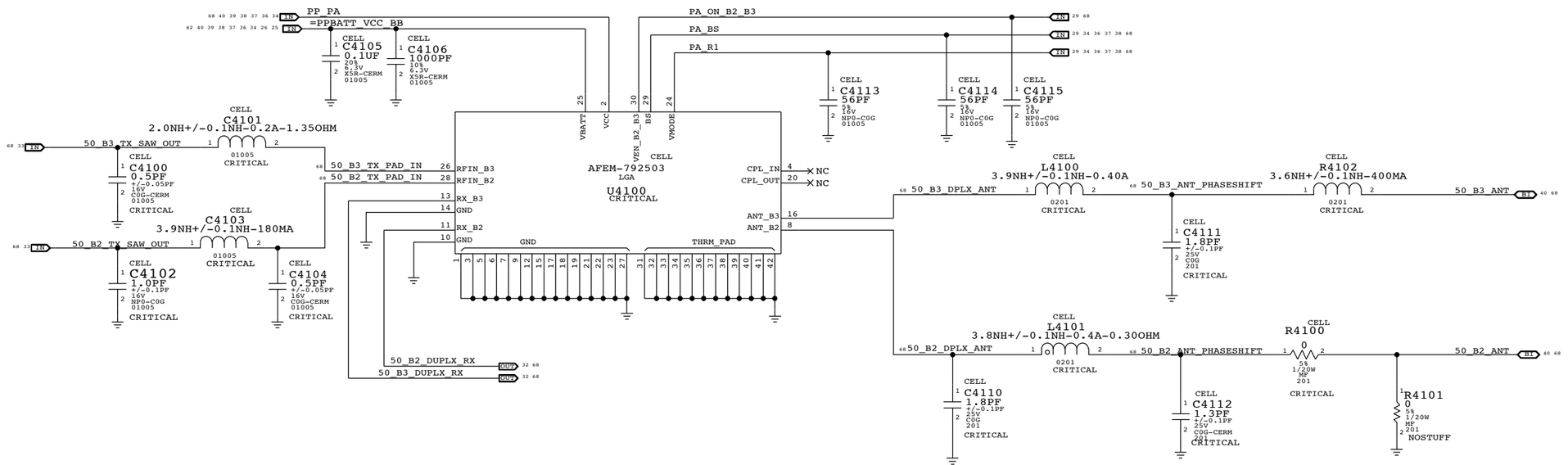


BAND 1/4 PAD



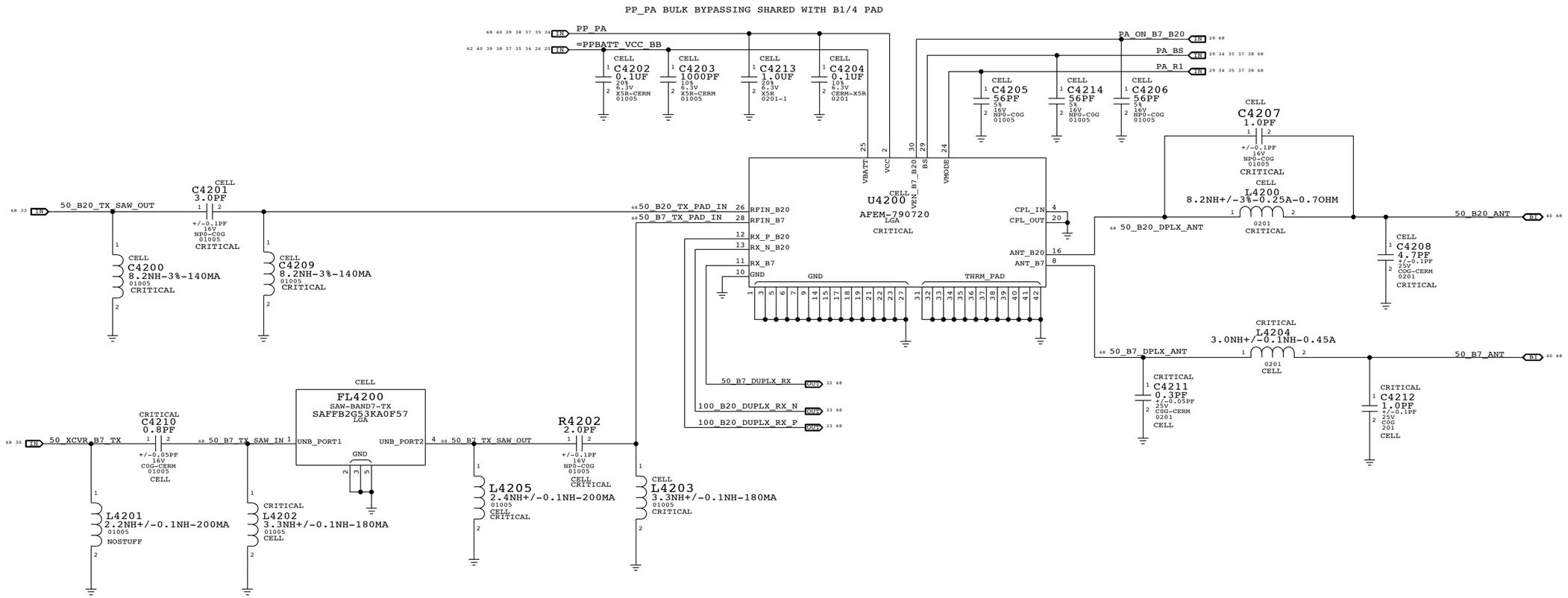
BAND	PA POWER MODE	PA_BS	PA_ON_B1_B4	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B4	HPM	0	1	0
B4	LPM	0	1	1
B1	HPM	1	1	0
B1	LPM	1	1	1

BAND 2/3 PAD



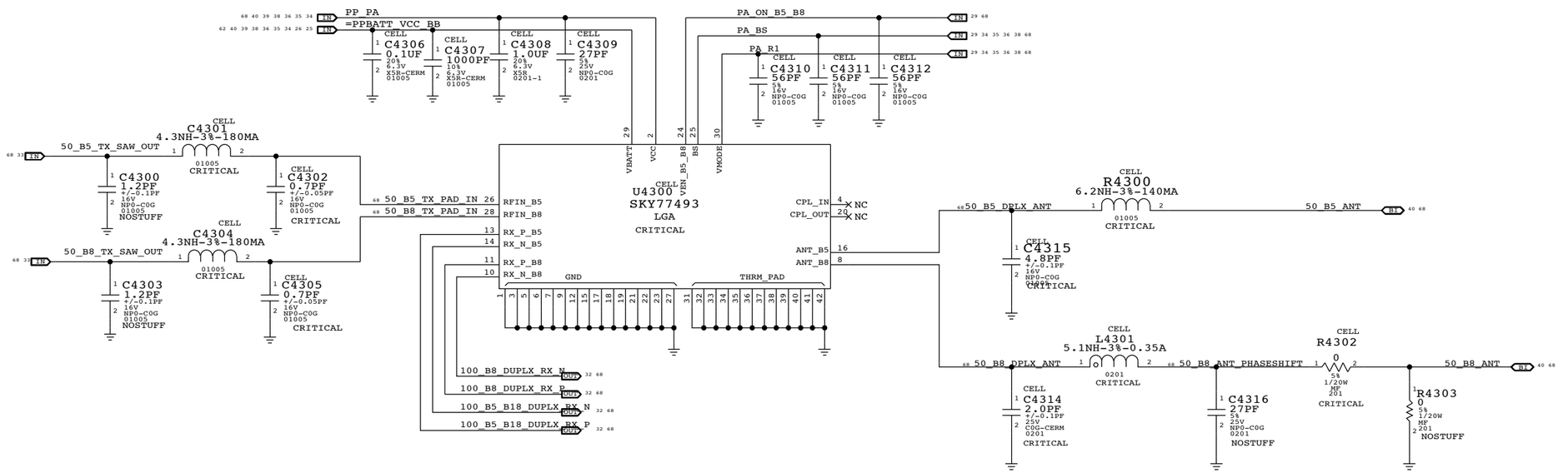
BAND	PA POWER MODE	PA_BS	PA_ON_B2_B3	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B3	HPM	0	1	0
B3	LPM	0	1	1
B2	HPM	1	1	0
B2	LPM	1	1	1

BAND 20/7 PAD



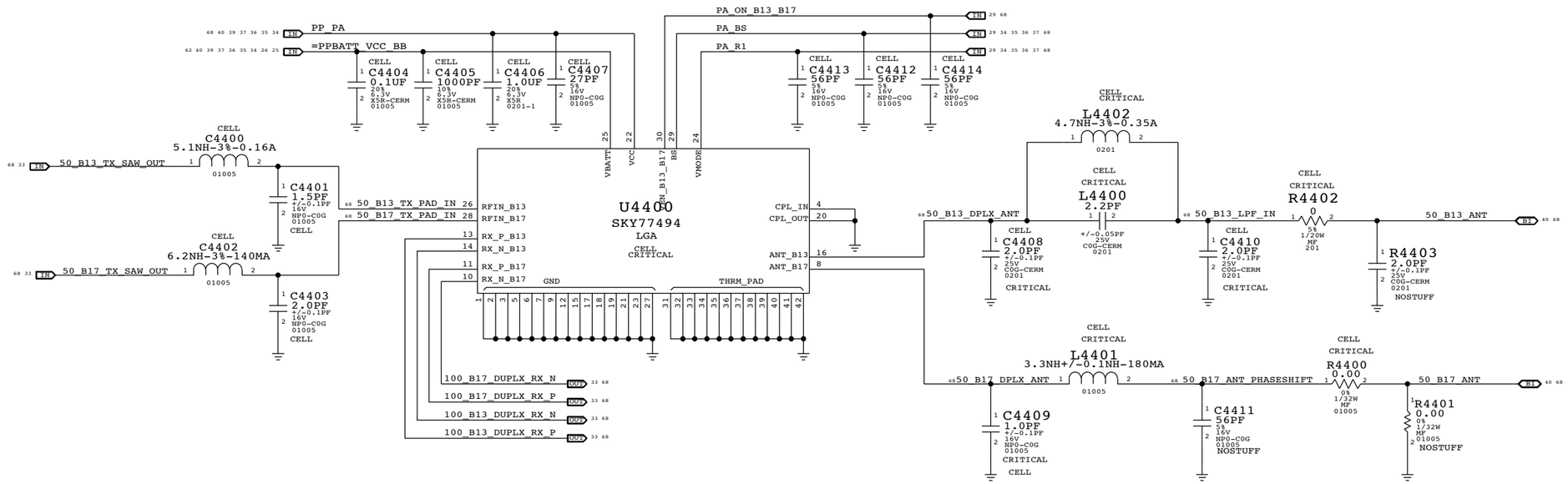
BAND	PA POWER MODE	PA_ON_B20	PA_R1
POWER DOWN	LPM	0	0
STANDBY	X	0	X
B20	HPM	1	0
B20	LPM	1	1

BAND 5/8 PAD



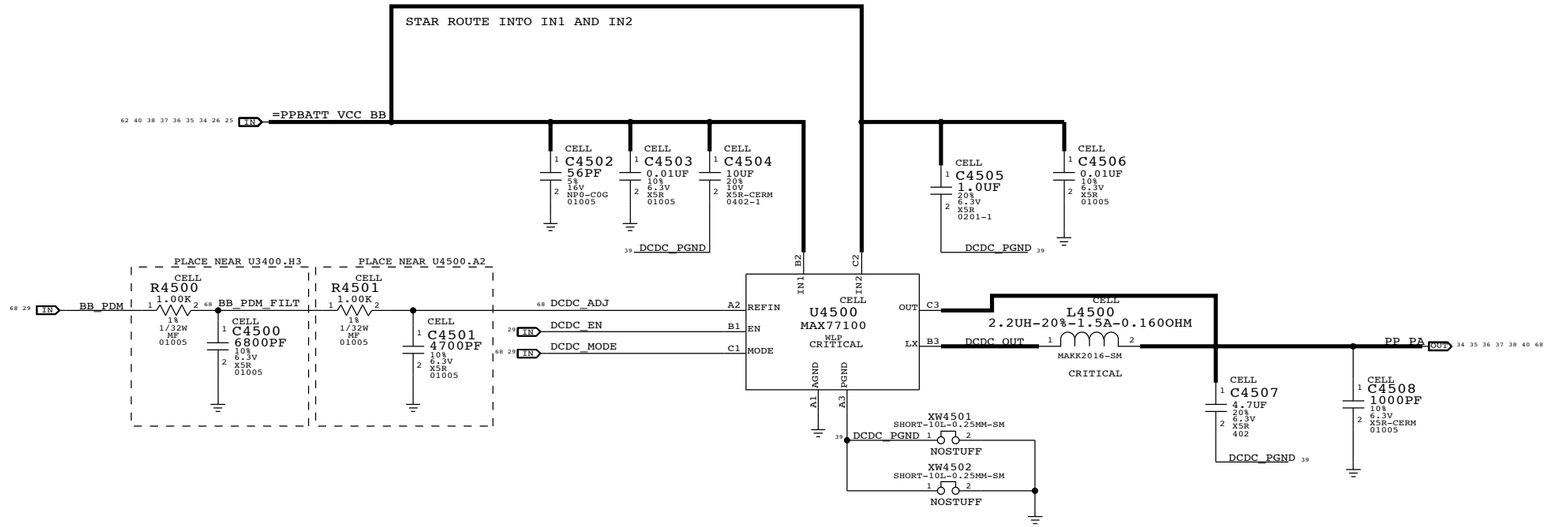
BAND	PA POWER MODE	PA_BS	PA_ON_B5_B8	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B5	HPM	0	1	0
B5	LPM	0	1	1
B8	HPM	1	1	0
B8	LPM	1	1	1

BAND 13/17 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B13_B17	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B17	HPM	0	1	0
B17	LPM	0	1	1
B13	HPM	1	1	0
B13	LPM	1	1	1

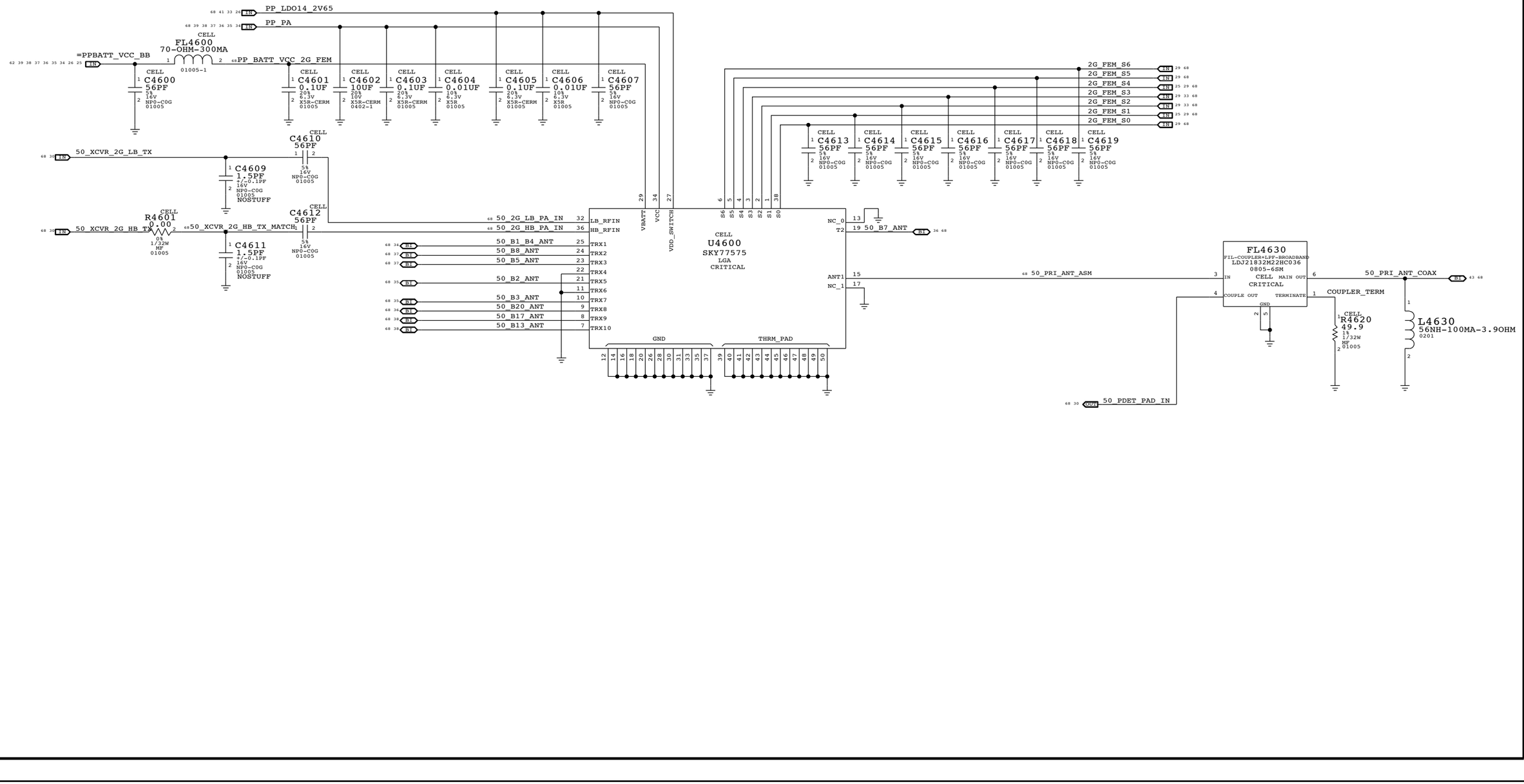
PA DC/DC CONVERTER



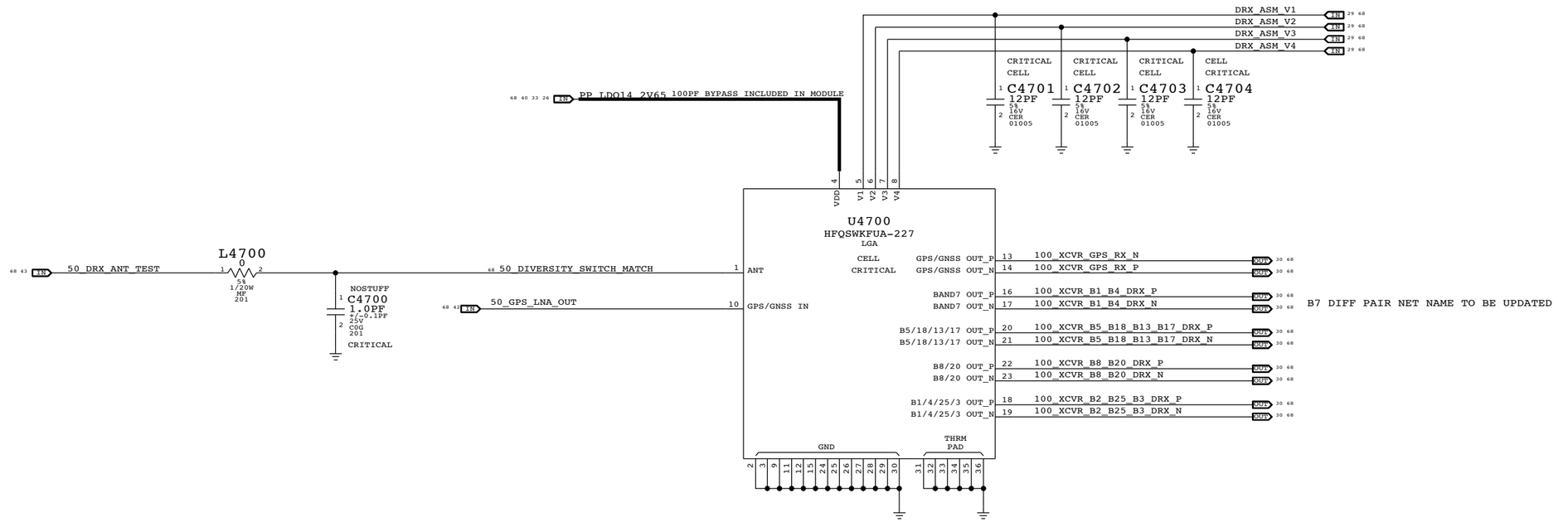
2G FEM

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

2G FEM



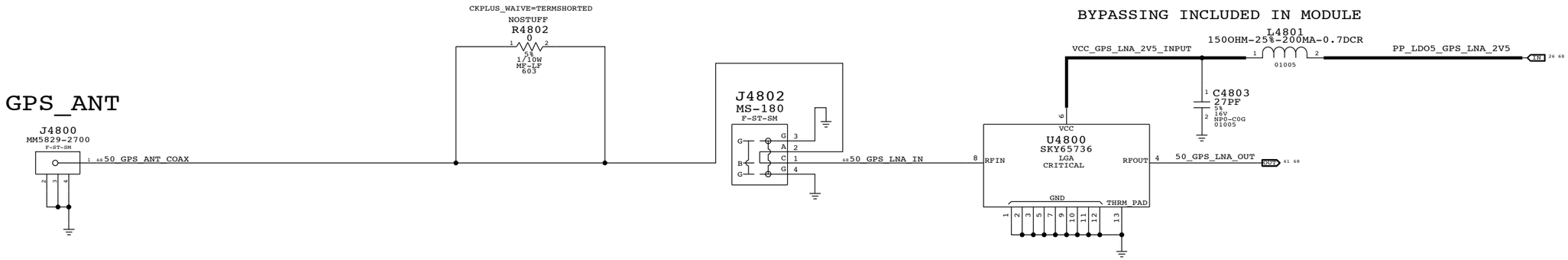
RX DIVERSITY



NEED TO UPDATE

BAND	DRX_ASM_V4	DRX_ASM_V3	DRX_ASM_V2	DRX_ASM_V1
B1/B4	LOW	LOW	LOW	LOW
B2/25	LOW	HIGH	LOW	LOW
B3	HIGH	LOW	LOW	LOW
B5/6/18	LOW	LOW	HIGH	LOW
B8	LOW	LOW	LOW	HIGH
B13/17	LOW	HIGH	HIGH	HIGH
B20	LOW	HIGH	HIGH	LOW
OFF	LOW	LOW	HIGH	HIGH
SWITCH IS TERMINATED IN ALL OTHER POSSIBLE STATES				

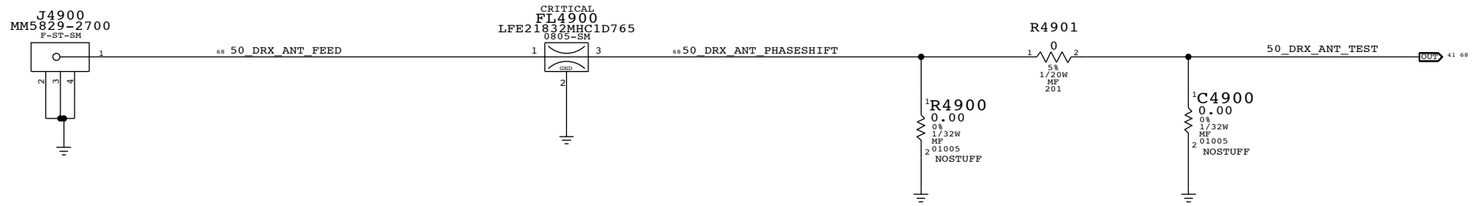
GPS



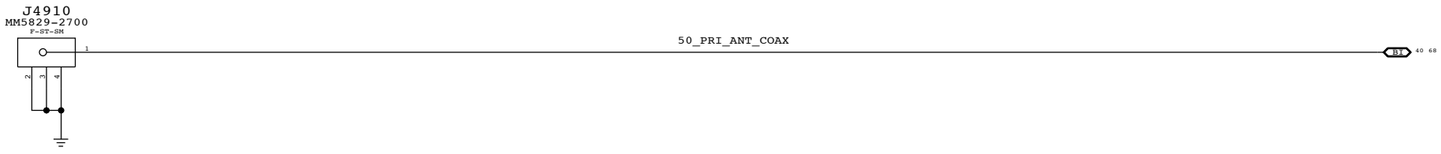
BOTTOM MOUNT TOP MOUNT

ANTENNA FEEDS

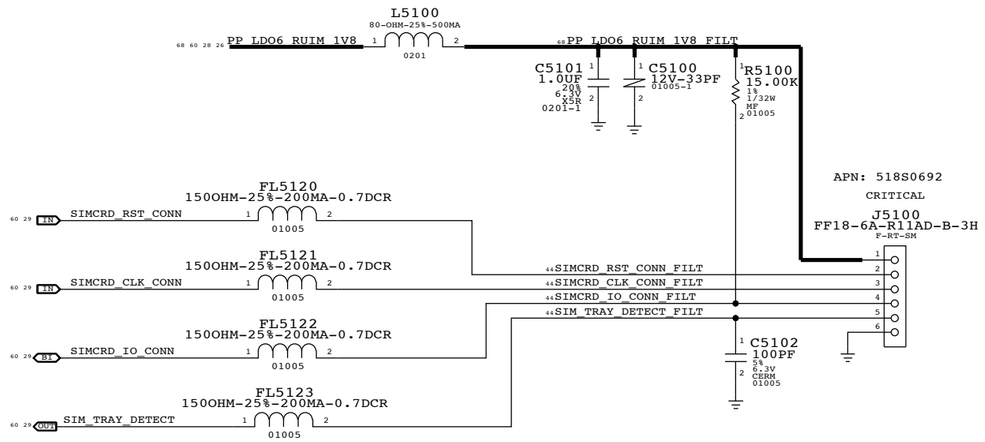
DRX_ANT COAX



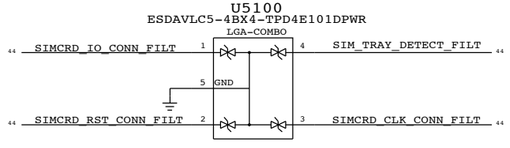
PRI_ANT COAX



SIM CARD FLEX CONN

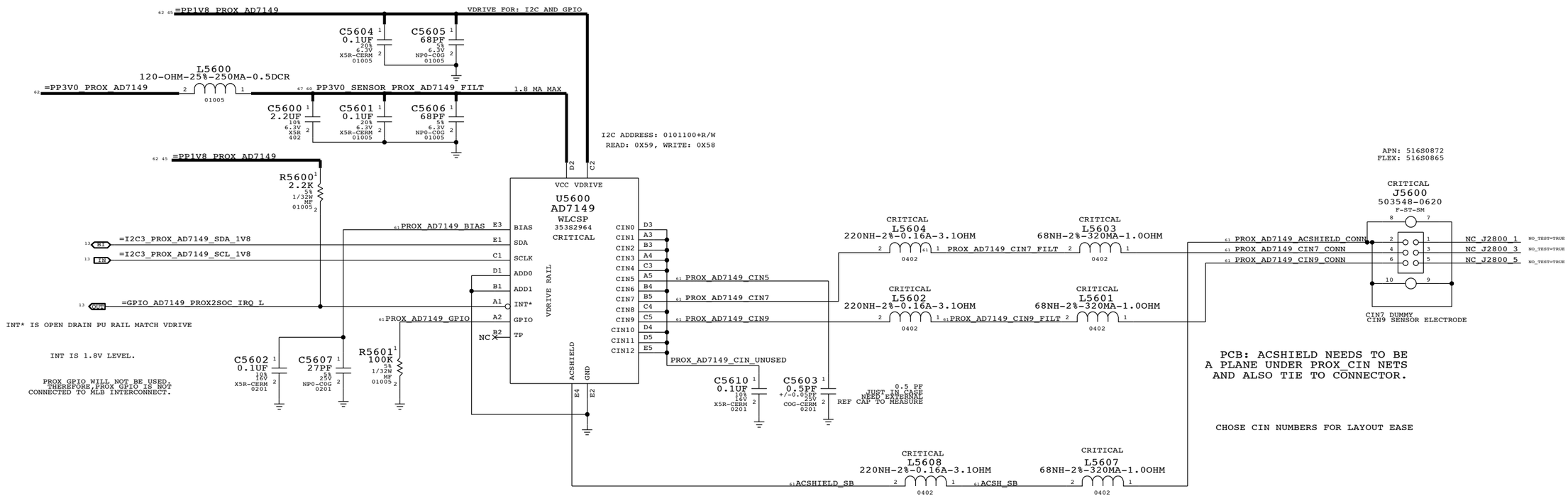


SIM CARD ESD PROTECTION



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0130	377S0159	?	U5100	RDAR://PROBLEM/12840016

PROX SENSOR



PCB: ENSURE ACSHIELD PLANE UNDER
U3200, NO GND PLANE NEAR PROX_CIN NETS..

WIFI/BT: MODULE

MODULE ISOLATION

XW5890 SHORT-10L-0.25MM-SM
61 57 IN PMU_GPIO_WLAN_REG_ON — PMU_GPIO_WLAN_REG_ON_R 46 60

XW5891 SHORT-10L-0.25MM-SM
61 57 IN PMU_GPIO_BT_REG_ON — PMU_GPIO_BT_REG_ON_R 46 60

XW5892 SHORT-10L-0.25MM-SM
64 57 IN PMU_GPIO_CLK_32K_WLAN — PMU_GPIO_CLK_32K_WLAN_R 46 60

XW5893 SHORT-10L-0.25MM-SM
29 25 OUT UART_WLAN2BB_LTE_COEX — UART_WLAN2BB_LTE_COEX_R 46 61

XW5894 SHORT-10L-0.25MM-SM
29 25 IN UART_BB2WLAN_LTE_COEX — UART_BB2WLAN_LTE_COEX_R 46 61

XW5895 SHORT-10L-0.25MM-SM
64 5 OUT UART2_WLAN2SOC_TX — UART2_WLAN2SOC_TX_R 46 61 64

XW5896 SHORT-10L-0.25MM-SM
64 5 IN UART2_SOC2WLAN_TX — UART2_SOC2WLAN_TX_R 46 61 64

XW5897 SHORT-10L-0.25MM-SM
64 5 IN HSIC1_SOC2WLAN_HOST_RDY — HSIC1_SOC2WLAN_HOST_RDY_R 46 61 64

62 =PPVCC_MAIN_WLAN

C5880 10UF 20% 6.3V CERM-X5R 0402-2
C5881 10UF 20% 6.3V CERM-X5R 0402-2
C5882 10UF 20% 6.3V CERM-X5R 0402-2

=PP3V3_S2R_WIFI_PA 61 62

C5800 4.7UF 20% 6.3V X5R-CERM1 402
C5801 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL
U5800
WIFI-BT-DOPPELBOCK
LGA

60 46 PMU_GPIO_CLK_32K_WLAN_R	33	CLK_32K
60 46 PMU_GPIO_WLAN_REG_ON_R	4	WL_REG_ON
60 46 PMU_GPIO_BT_REG_ON_R	3	BT_REG_ON
61 JTAG_WLAN_SEL	23	JTAG_SEL
64 61 4 BT HSIC1_WLAN_DATA	13	HSIC_DATA
64 61 4 BT HSIC1_WLAN_STB	14	HSIC_STROBE
NC	7	SDIO_CLK
NC	6	SDIO_CMD
NC	8	SDIO_DATA0
NC	9	SDIO_DATA1
NC	10	SDIO_DATA2
NC	11	SDIO_DATA3
NC	77	RF_SW_CTRL11
NC	47	I2SWS
NC	46	I2SDO
NC	48	I2SDI
NC	49	I2SCLK
	67	RF_A_0
	79	RF_A_1
	62	RF_G_0
	74	RF_G_1
	16 17	VBAT
	70 71	RF_VCC_FEM

R5800 10K 5% 1/32W MF 01005

BT_GPIO5/LTE_COEX_UART_TX	51	UART_WLAN2BB_LTE_COEX_R 46 61
BT_GPIO4/LTE_COEX_UART_RX	50	UART_BB2WLAN_LTE_COEX_R 46 61
BT_GPIO1/HOSTWAKE	55	PMU_GPIO_BT_HOST_WAKE OUT 57
BT_GPIO0/BTWAKE	56	GPIO_BT_WAKE IN 5 61
BT_UART_RXD	37	UART1_SOC2BT_TX IN 5 64
BT_UART_TXD	38	UART1_BT2SOC_TX OUT 5 64
BT_UART_RTS*	36	UART1_BT2SOC_RTS_L OUT 5 64
BT_UART_CTS*	39	UART1_SOC2BT_RTS_L IN 5 64
BT_PCM_CLK	41	I2S4_SOC2BT_BCLK IN 5 64
BT_PCM_SYNC	42	I2S4_SOC2BT_LRCK IN 5 64
BT_PCM_OUT	43	I2S4_BT2SOC_DATA OUT 5 64
BT_PCM_IN	44	I2S4_SOC2BT_DATA IN 5 64
GPIO0/WL_HOST_WAKE	22	PMU_GPIO_WLAN_HOST_WAKE OUT 57
GPIO1/HOST_READY	20	HSIC1_SOC2WLAN_HOST_RDY_R 46 61 64
GPIO2/WL_TCK	27	TP_JTAG_WLAN_TCK 61 64
GPIO3/WL_TMS	28	JTAG_WLAN_TMS_TX_BLANK
GPIO4/WL_TDI	26	JTAG_WLAN_TDI_OSCAR_A
GPIO5/WL_TDO	24	JTAG_WLAN_TDO_OSCAR_B
GPIO12/WL_TRST*	25	TP_JTAG_WLAN_TRST_L 61 64
GPIO9/AGG_CHANNEL	19	NC
GPIO10/HSIC_DEVICE_READY	1	HSIC1_WLAN2SOC_DEVICE_RDY OUT 5 61 64
GPIO11/HSIC_RESUME	2	HSIC1_WLAN2SOC_REMOTE_WAKE OUT 5 61 64
GPIO15/WLAN_UART_TX	52	UART2_WLAN2SOC_TX_R 46 61 64
GPIO14/WLAN_UART_RX	53	UART2_SOC2WLAN_TX_R 46 61 64
GPIO6	30	NC
GPIO7	29	WLAN_GPIO7
GPIO8	31	NC
VIO	35	=PP1V8_S2R_VDDIO_WLAN_BT 46 62
DUMMY	57	NC

GND_SIGNAL: 5 12 15 18 21 32 34 40 45 54 58 59 60 61 63 64 65 66 68 69 72 73 75 76 78 80 81 82 83 84 85 86 87 88

R5804 0.00 0% 1/32W MF 01005 — 1 2 WLAN_TX_BLANK IN 29

R5801 0.00 0% 1/32W MF 01005 — 1 2 OSCAR2RADIO_CONTEXT_A IN 19 29

R5802 0.00 0% 1/32W MF 01005 — 1 2 OSCAR2RADIO_CONTEXT_B IN 19 29

=PP1V8_S2R_VDDIO_WLAN_BT 46 62

R5803 10K 5% 1/32W MF 01005

CRITICAL
U5810
2.4-5.0GHZ
SM
LOW(2.4GHZ) 3
HIGH(5.0GHZ) 1
ANT(COMMON) 5
GND 6 4 2

CRITICAL R5811 0.00 1% 1/20W MF 0201
69 RF_G_0_DIPLEXER — 1 2 — 69 RF_G_0_BAW_ANT

CRITICAL L5811 10NH-3%-250MA 0201
RF_G_0_BAW_ANT — 1 2

CRITICAL
U5811
BAW-2436MHZ
885061
LGA
RF_G_0_BAW_ANT — 4 IN
GND 5 3 2
OUT 1 — RF_G_0_BAW_MOD

CRITICAL C5811 2.5NH+/-0.1NH-500MA 0201
RF_G_0_BAW_MOD — 1 2 — RF_G_0_MATCH_MOD

CRITICAL L5810 8.2NH+/-3%-0.25A-0.7OHM 0201
RF_G_0_BAW_MOD — 1 2

CRITICAL C5810 0.5PF +/-0.05PF 25V COG-CERM 201
RF_G_0_MATCH_MOD — 1 2

CRITICAL
J5810
MM4829-2702
F-ST-SM
1 2 3 4

CRITICAL R5810 0.00 1% 1/20W MF 0201
69 RF_0_ANT — 1 2 — 69 RF_0_ANT_MATCH_T

NOSTUFF C5817 0.2PF +/-0.1PF 25V COG-CERM 201
1 2 — RF_0_ANT

NOSTUFF C5816 0.2PF +/-0.1PF 25V COG-CERM 201
1 2 — RF_0_ANT_MATCH_T

CRITICAL C5814 1.0NH+/-0.1NH-0.75A 0201
69 RF_A_0_DIPLEXER — 1 2 — 69 RF_A_0_MATCH

NOSTUFF C5815 0.2PF +/-0.1PF 25V COG-CERM 201
1 2 — RF_A_0_DIPLEXER

CRITICAL C5813 0.2PF +/-0.05PF 25V COG-CERM 0201
1 2 — RF_A_0_MATCH

CRITICAL
J5820
MM4829-2702
F-ST-SM
1 2 3 4

CRITICAL R5820 0.00 1% 1/20W MF 0201
69 RF_1_ANT — 1 2 — 69 RF_1_ANT_MATCH_T

NOSTUFF C5827 0.2PF +/-0.1PF 25V COG-CERM 201
1 2 — RF_1_ANT

NOSTUFF C5826 0.2PF +/-0.1PF 25V COG-CERM 201
1 2 — RF_1_ANT_MATCH_T

CRITICAL
U5820
DPX205850DT-9038A1SJ
SM
COM 5
HI 1
LO 3
GND 6 4 2

CRITICAL C5821 0.00 1% 1/20W MF 0201
69 RF_G_1_DIPLEXER — 1 2 — 69 RF_G_1_MATCH_MOD

NOSTUFF C5822 0.2PF +/-0.1PF 25V COG-CERM 201
1 2 — RF_G_1_DIPLEXER

CRITICAL C5820 1.0PF +/-0.05PF 25V COG-CERM 0201
1 2 — RF_G_1_MATCH_MOD

CRITICAL C5824 0.8NH-+/-0.1NH-0.8MA 0201
69 RF_A_1_DIPLEXER — 1 2 — 69 RF_A_1_MATCH

CRITICAL C5825 0.2PF +/-0.05PF 25V COG-CERM 0201
1 2 — RF_A_1_DIPLEXER

NOSTUFF C5823 0.2PF +/-0.05PF 25V COG-CERM 0201
1 2 — RF_A_1_MATCH

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0155	377S0104	?		RDAR://PROBLEM/12840267

DZ6000,DZ6001,DZ6002,DZ6003,DZ6090

62 =PP3V0_S2R_TRISTAR

C6030 1.0UF 20% 6.3V X5R 0201-1

C6035 0.22UF 20% 6.3V X5R 0201

C6040 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005

62 =PP1V8_S2R_TRISTAR

C6031 0.22UF 20% 6.3V X5R 0201

C6041 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005

62 =PP3V3_ACC

C6042 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005

C6032 0.22UF 20% 6.3V X5R 0201

PPVBUS_PROT 55 60 67

C6043 8.2PF +/-0.25PF 25V NP0-C0G 0201

C6034 1UF 10% 25V X5R 0402

C6045 1UF 10% 25V X5R 0402

U6000
CBTL1610A1UK
WLCSP

		F3	VDD_1V8		
		F4	VDD_3V0		
		D5	ACC_PWR		
65 15 BI	MIKEY_TS_P	C3	DIG_DP	P_IN	F6
65 15 BI	MIKEY_TS_N	C4	DIG_DN	ACC1	C5 PPOUT_E75_ACC_ID1 48 67
				ACC2	E5 PPOUT_E75_ACC_ID2 48 67
64 29 BI	USB_BB_P	A1	USB1_DP	DP1	A2 64 E75_DPAIR1_P
64 29 BI	USB_BB_N	B1	USB1_DN	DN1	B2 64 E75_DPAIR1_N
57 OUTPU	PMU_USB_BRICKID	C2	BRICK_ID		
64 60 4 BI	USB_SOC_P	A3	USB0_DP	DP2	A4 64 E75_DPAIR2_P
64 60 4 BI	USB_SOC_N	B3	USB0_DN	DN2	B4 64 E75_DPAIR2_N
				CON_DET_L	E3 60 TS_E75_ACC_DET_L
64 5 IN	UART6_TS_ACC_TXD	E2	UART0_TX		
64 5 OUTPU	UART6_TS_ACC_RXD	E1	UART0_RX	POW_GATE_EN*	D6 OVP_SW_EN_L OUTP 55
64 60 5 IN	UART0_SOC_TXD	F2	UART1_TX	SWITCH_EN	E4 RESET_SOC_L IN 4 13 25 57 60 61 67
64 60 5 OUTPU	UART0_SOC_RXD	F1	UART1_RX	HOST_RESET	B6 TS2PMU_RESET_IN OUTP 57 67
64 29 25 5 IN	UART3_BB2SOC_TX	D2	UART2_TX	SDA	D3 I2C2_SDA_1V8 BIDIR 5 64
64 29 25 5 OUTPU	UART3_SOC2BB_TX	D1	UART2_RX	SCL	D4 I2C2_SCL_1V8 IN 5 64
				INT	C6 GPIO_TS2SOC2PMU_INT OUTP 5 57
	JTAG_SOC_TCK_R	A5	JTAG_CLK	BYPASS	E6 BYPASS_U5900
	JTAG_SOC_TMS_R	B5	JTAG_DIO		
				DVSS	F5
				DVSS	C1
				DVSS	A6

TO BB USB

ACCESSORY USB

ACCESSORY UART

AP DEBUG UART

BB DEBUG UART

(T'S OFF TO SOC UART3)

64 60 4 OUTPU JTAG_SOC_TCK — R6030 0.00 0% 1/32W MF 01005

64 60 4 BI JTAG_SOC_TMS — R6031 0.00 0% 1/32W MF 01005

C6033 1.0UF 20% 6.3V X5R 0201-1

TRISTAR 2:
AS OF 10/11/12 STILL PLAN TO STUFF CAP EVEN WITH TRISTAR2
RDAR://PROBLEM/12580126

15 OUTPU L81_MBUS_REF — XW6000 SHORT-10L-0.25MM-SM

PLACE_NEAR=U6000.F5:5MM

CRITICAL
L6030
90-OHM-50MA
TCM0605-1

E75_DPAIR1_CONN_P BI 49 60 64

E75_DPAIR1_CONN_N BI 49 60 64

CRITICAL DZ6000 ESD0P2RF-02LS TSSLP-2-1 0.4PF

CRITICAL DZ6001 ESD0P2RF-02LS TSSLP-2-1 0.4PF

CRITICAL
L6031
90-OHM-50MA
TCM0605-1

E75_DPAIR2_CONN_P BI 49 60 64

E75_DPAIR2_CONN_N BI 49 60 64

CRITICAL DZ6002 ESD0P2RF-02LS TSSLP-2-1 0.4PF

CRITICAL DZ6003 ESD0P2RF-02LS TSSLP-2-1 0.4PF

PPVCC_MAIN 55 56 57 58 60 62 67

NOSTUFF R6091 100K 5% 1/32W MF 01005

C6091 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005

R6090 10K 5% 1/32W MF 01005

E75_ACC_DET_R_L

FL6090 120-OHM-25%-250MA-0.5DCR 01005

E75_ACC_DET_CONN_L IN 49 60

NOSTUFF C6090 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005

CRITICAL DZ6090 ESD0P2RF-02LS TSSLP-2-1

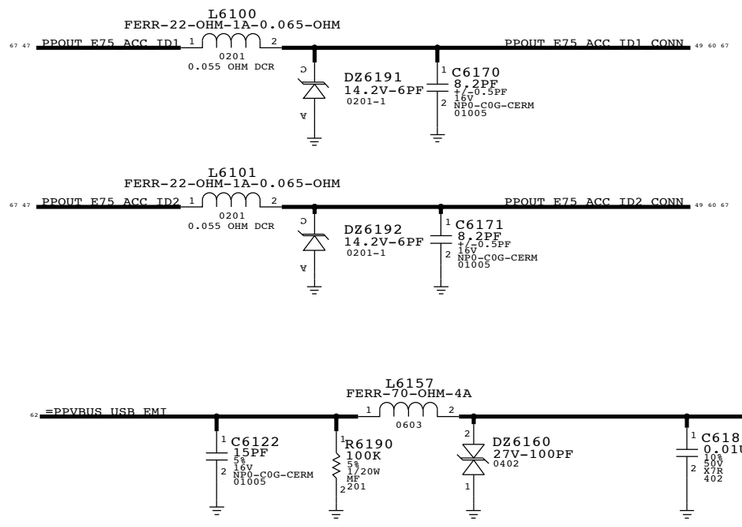
K CRITICAL D6090 SM-201 DSF01S30SC A

TRISTAR 2:
FOR PULSED CON_DET_L SUPPORT
NOSTUFF R6080, STUFF R6081

60 57 PMU_E75_ACC_DET_L

NOSTUFF R6080 0.00 0% 1/32W MF 01005

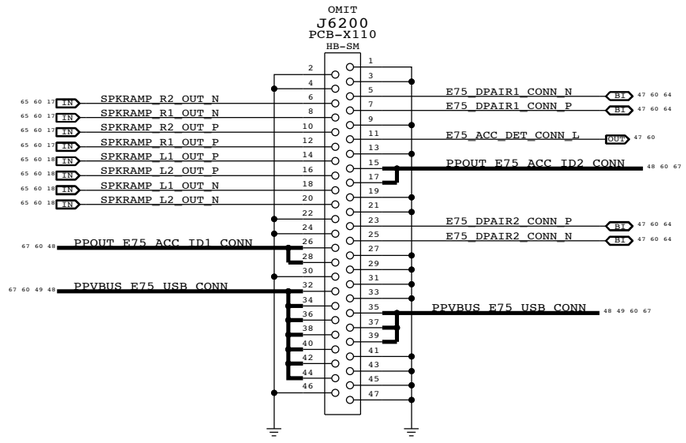
R6081 0.00 0% 1/32W MF 01005



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0116	377S0108		DZ6160	RDAR:8370432
155S0320	155S0513		L6100,L6101	RDAR://PROBLEM/9625601
155S0741	155S0397		L6157	RDAR://PROBLEM/11238851

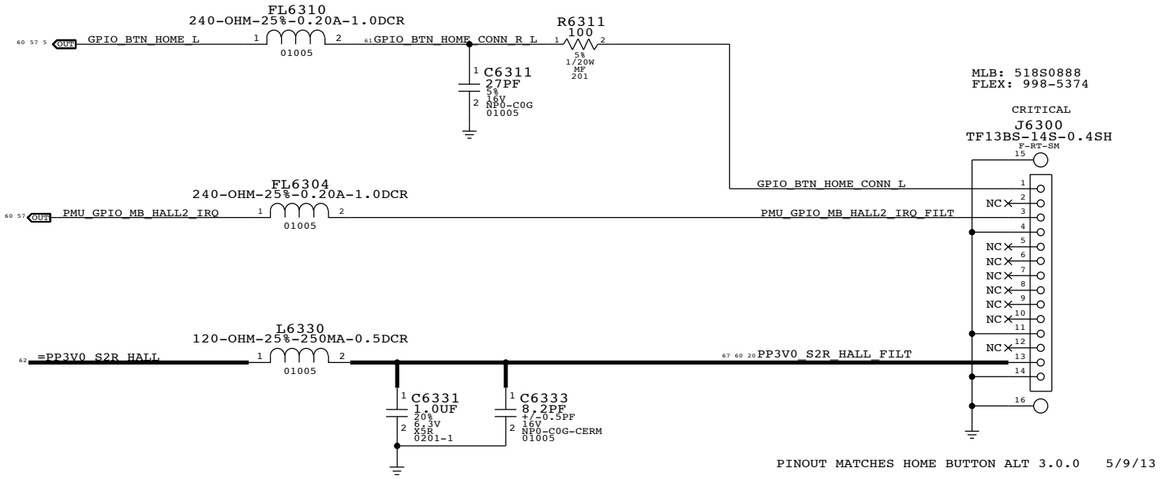
IO FLEX HOTBAR PADS

MLB 998-5877
FLEX 998-5876

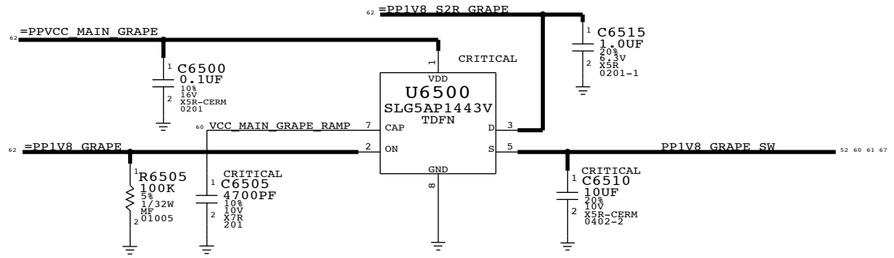


PINOUT MATCHES IO_FLEX 4.2.0 3/12/13

HOME BUTTON FILTERS



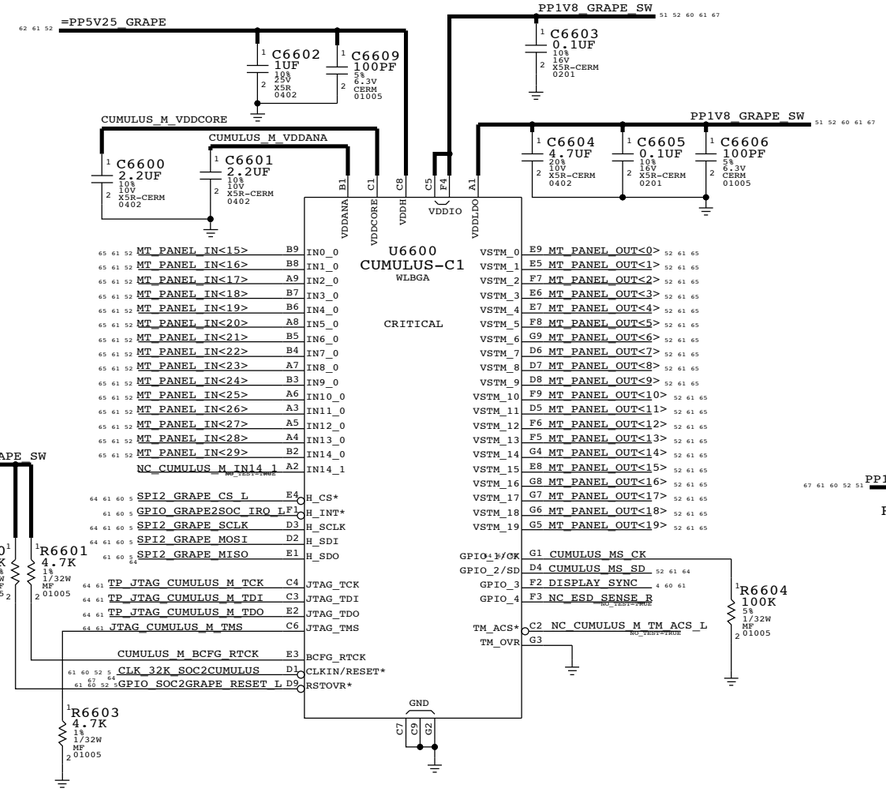
GRAPE CONNECTOR SUPPORT



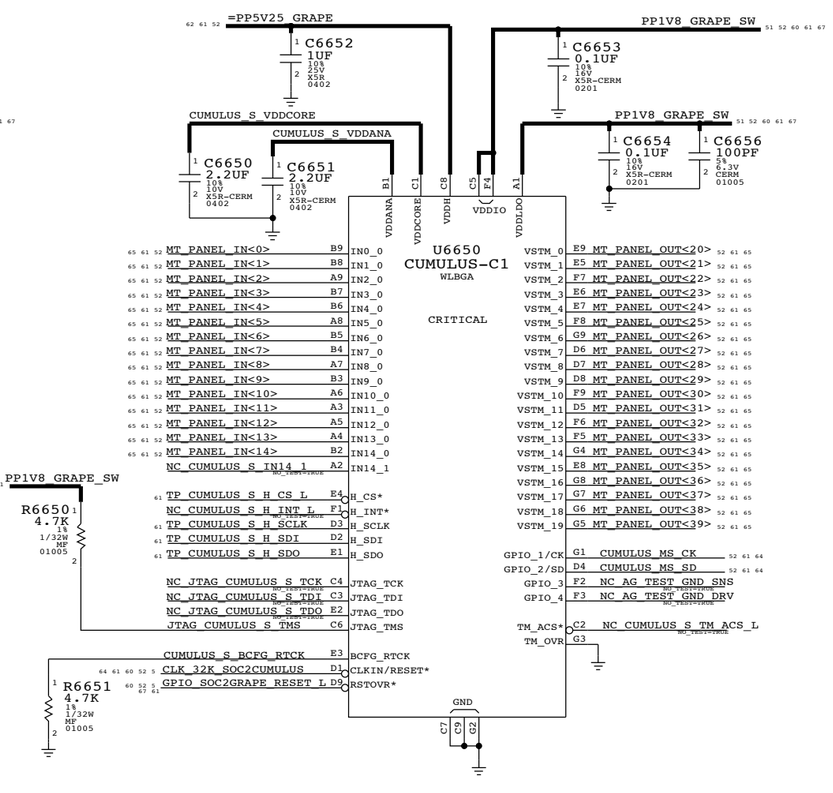
LAYOUT NOTE:
PUT THERMAL VIAS AROUND U2300 IN CASE OF SHORTED CONDITION

CUMULUS C1 (CSP) IN MASTER-SLAVE CONFIG

MASTER CUMULUS



SLAVE CUMULUS



PINOUT MATCHES GRAPE_FLEX_DRIVE_ALT 0.1.0 1/8/13

CRITICAL

J6620
AA03-S042VA1
F-ST-SM

MT_PANEL_OUT<12>	3	4	MT_PANEL_OUT<13>
MT_PANEL_OUT<11>	5	6	MT_PANEL_OUT<14>
MT_PANEL_OUT<10>	7	8	MT_PANEL_OUT<15>
MT_PANEL_OUT<9>	9	10	MT_PANEL_OUT<16>
MT_PANEL_OUT<8>	11	12	MT_PANEL_OUT<17>
MT_PANEL_OUT<7>	13	14	MT_PANEL_OUT<18>
MT_PANEL_OUT<6>	15	16	MT_PANEL_OUT<19>
MT_PANEL_OUT<5>	17	18	MT_PANEL_OUT<20>
MT_PANEL_OUT<4>	19	20	MT_PANEL_OUT<21>
MT_PANEL_OUT<3>	21	22	MT_PANEL_OUT<22>
MT_PANEL_OUT<2>	23	24	MT_PANEL_OUT<23>
MT_PANEL_OUT<1>	25	26	MT_PANEL_OUT<24>
MT_PANEL_OUT<0>	27	28	MT_PANEL_OUT<25>
MT_PANEL_OUT<26>	29	30	MT_PANEL_OUT<39>
MT_PANEL_OUT<27>	31	32	MT_PANEL_OUT<38>
MT_PANEL_OUT<28>	33	34	MT_PANEL_OUT<37>
MT_PANEL_OUT<29>	35	36	MT_PANEL_OUT<36>
MT_PANEL_OUT<30>	37	38	MT_PANEL_OUT<35>
MT_PANEL_OUT<31>	39	40	MT_PANEL_OUT<34>
MT_PANEL_OUT<32>	41	42	MT_PANEL_OUT<33>

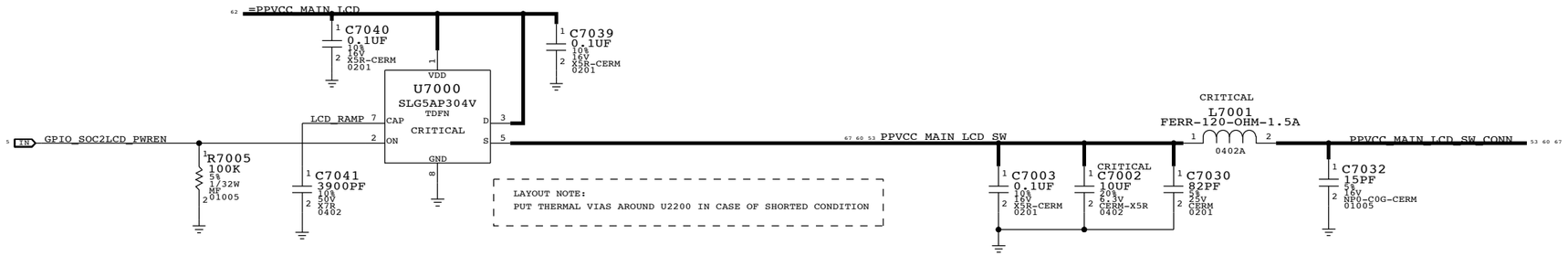
PINOUT MATCHES GRAPE_FLEX_SENSE_ALT 0.1.0 1/8/13

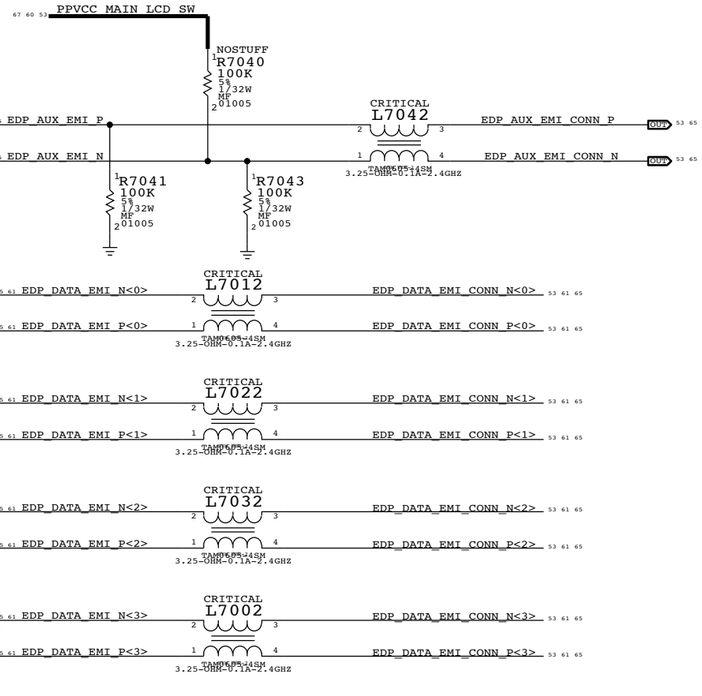
CRITICAL

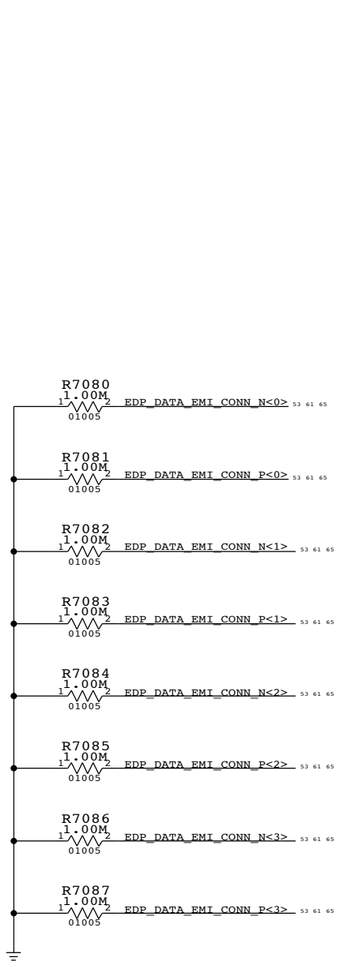
J6640
AA03-S034VA1
F-ST-SM

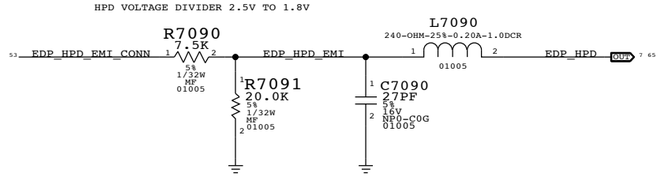
MT_PANEL_IN<14>	3	4	MT_PANEL_IN<29>
MT_PANEL_IN<13>	5	6	MT_PANEL_IN<28>
MT_PANEL_IN<12>	7	8	MT_PANEL_IN<27>
MT_PANEL_IN<11>	9	10	MT_PANEL_IN<26>
MT_PANEL_IN<10>	11	12	MT_PANEL_IN<25>
MT_PANEL_IN<9>	13	14	MT_PANEL_IN<24>
MT_PANEL_IN<8>	15	16	MT_PANEL_IN<23>
MT_PANEL_IN<7>	17	18	MT_PANEL_IN<22>
MT_PANEL_IN<6>	19	20	MT_PANEL_IN<21>
MT_PANEL_IN<5>	21	22	MT_PANEL_IN<20>
MT_PANEL_IN<4>	23	24	MT_PANEL_IN<19>
MT_PANEL_IN<3>	25	26	MT_PANEL_IN<18>
MT_PANEL_IN<2>	27	28	MT_PANEL_IN<7>
MT_PANEL_IN<16>	29	30	MT_PANEL_IN<0>
MT_PANEL_IN<15>	31	32	MT_PANEL_IN<1>

EDP CONNECTOR SUPPORT



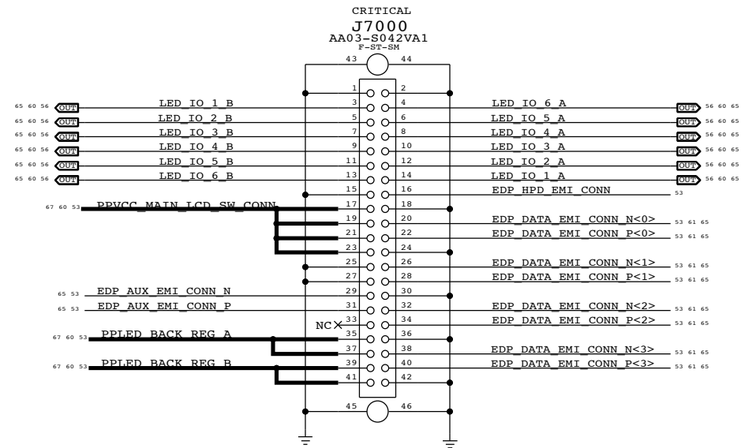






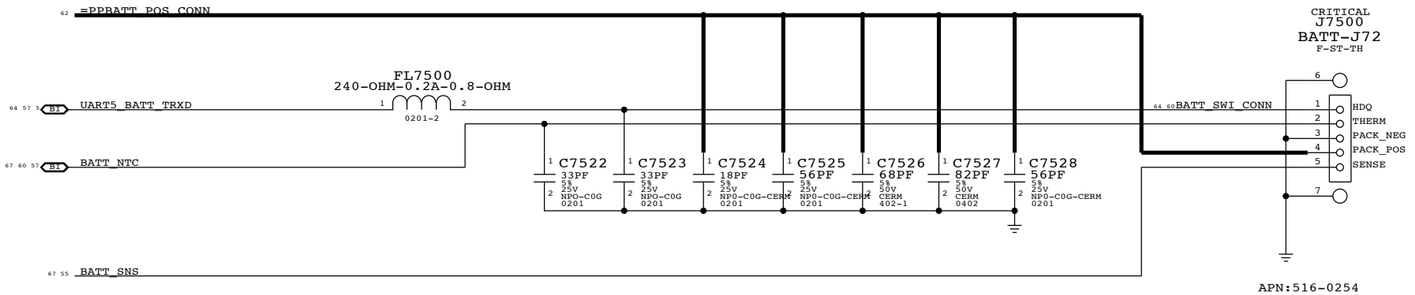
EDP CONNECTOR

PINOUT MATCHES DISPLAY_EDP_FLEX 1.0.0 1/7/13



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0823	?		RDAR://PROBLEM/11282371

FL7500,L1920



APN:516-0254

PLACEMENT_NOTE=PLACE NEAR L8225.1

PPVCC_MAIN 47 55 56 57 58 60 62 67

C8140 CRITICAL 150UF 20% 6.3V TANT-1 B15G — ESR MAX=70MOHM
C8141 CRITICAL 150UF 20% 6.3V TANT-1 B15G — ESR MAX=70MOHM
C8150–C8159 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8142 82PF 5% 25V CERM 0201
C8143 18PF 5% 25V NP0-C0G-CERM 0201
C8144 CRITICAL 1.0UF 20% 6.3V X5R 0201-1
C8160–C8172 CRITICAL 10UF 20% 6.3V CERM-X5R 0402

VCC_MAIN BYPASS
PLACE TWO 10UF CAP
AT EACH VDD INPUT

L8112 CRITICAL 2.2UH-20%-5.6A-0.03OHM PILE101D-SM DCR=30MOHM MAX

PPVCC_MAIN 67 62 60 58 57 56 55 47

R8170 NOSTUFF 4.7K 5% 1/20W MF 201 — OVP_SW_EN_L 55 47

Q8104 CRITICAL FDMC6683 MLP3.3X3.3 — RDSON=0.0136@VGS=-2.5V ID=12.0A

PPBATT_VCC 67 62 60 55

ACT_DIO — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.1 MM, NET_SPACING_TYPE=ANLG

D8100 CRITICAL SOD-123W PMEG4030ER — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.20 MM, NET_SPACING_TYPE=PWR, DIDT=TRUE, SWITCH_NODE=TRUE

SW_CHGA 67 61

R8172 0 5% 1/20W MF 201 — PLACE_NEAR=U8100.R17:2MM

BATT_SNS 67 54 — R8173 499 1% 1/20W MF 201 — BATT_SNS_R 67 — PLACE_NEAR=U8100.R17:10MM

C8149 NOSTUFF 0.022UF 10% 25V X7R 0402 — PLACE_NEAR=U8100.R17:10MM

LAYOUT NOTE -
R8172- PLACE NEAR PMU
C8149- PLACE NEAR PMU
R8173- PLACE NEAR PMU

XW8114 SHORT-0201

USB_VBUS_DETECT 67 4 — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM, VOLTAGE=6.0V

C8148 CRITICAL 4.7UF 10% 35V X5R-CERM 0603 — PLACE_NEAR=U8100.F18:2MM
C8147 CRITICAL 4.7UF 10% 35V X5R-CERM 0603 — PLACE_NEAR=U8100.L18:2MM

PMU_VCENTER 67 60 — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM, VOLTAGE=6.0V

LAYOUT NOTE: PLACE RIGHT AT THE PIN

PPVBUS_PROT 67 60 62

C8145 CRITICAL 2.2UF 10% 25V X5R-CERM 2 603 — PLACE_NEAR=U8100.F16:10MM

LAYOUT NOTE: PLACE RIGHT AT THE PIN

NOSTUFF R8116 470K 1% 1/20W MF 201 — Q8123 CRITICAL FDMC6676BZ MLP3.3X3.3

DZ8120 CRITICAL BZT52C10LP LLP — NOTE: 10V ZENER

VBUS_PROT_G 60 — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.1MM, NET_SPACING_TYPE=ANLG

R8130 220K 1% 1/20W MF 201 — PPVBUS_USB_DCIN 67 62 60

USB REVERSE VOLTAGE PROTECTION

R8146 4.7K 5% 1/20W MF 201 — OVP_SW_EN_L 55 47 — OVP_SW_EN_L_R

C8146 NOSTUFF 0.01UF 10% 25V X5R-CERM 0201

LAYOUT NOTE:
R8146, C8146 CAN BE
ANYWHERE BET.TRISTAR
AND PMU

TP_HV_CHG_EN

=PPVCC_MAIN_CPU 62 55
=PPVCC_MAIN_GPU 62 55
=PPVCC_MAIN_SOC 62 55
PPVCC_MAIN 67 62 60 58 57 56 55 47

OMIT_TABLE

U8100 D2089A0 FCBGA SYM 1 OF 4

CHG_LX0	G19
CHG_LX1	H19
CHG_LX2	J19
CHG_LX3	K19
VBAT	R17
IBAT_S	P17
IBAT0	M19
IBAT1	N19
IBAT2	P19
IBAT3	R19
ACT_DIO	N17
VCENTER	F18, F19, G18, H18, J18, K18, L18, L19
VBUS	F16, F17, G16, G17, H16, H17, J17, K16, K17, L16, L17
VBUS_OVP_OFF	C16
HV_CHG_DIS	D17
VDD_BUCK0_01	F1, F2
VDD_BUCK0_23	K1, K2
VDD_BUCK1_01	P1, P2
VDD_BUCK1_2	V1, V2, V3
VDD_BUCK2	U8, V8
VDD_BUCK3	A4, B4
VDD_BUCK4	A8, B8
VDD_BUCK5	U4, V4
VDD_BUCK6	B1, B2, B3
VCC_MAIN_S	T16
VCC_MAIN	M18, N18, P18, R18
BUCK0_LX0	E1, E2
BUCK0_LX1	G1, G2
BUCK0_LX2	J1, J2
BUCK0_LX3	L1, L2
BUCK0_FB	H6
BUCK1_LX0	N1, N2
BUCK1_LX1	R1, R2
BUCK1_LX2	U1, U2
BUCK1_FB	M6
BUCK2_LX0	U7, V7
BUCK2_FB	P7
BUCK3_LX0	A5, B5
BUCK3_FB	E6
BUCK4_LX0	A7, B7
BUCK4_FB	E7
BUCK5_LX0	U5, V5
BUCK5_FB	P6
BUCK6_LX0	C1, C2
BUCK6_FB	F6
BUCK6_BYP0	A1
BUCK6_BYP1	A2
BUCK6_BYP2	A3
VBUCK3	B13, B14, C14, A12
BUCK3_SW1	B12, C12, C13, A13
BUCK3_SW2	A14
BUCK3_SW3	B10
VBUCK4	B11, C11, A9
BUCK4_SW1	B9, C9, C10, A10
BUCK4_SW2	A11
VPUMP	

USB/BAT BUCK

VCC-MAIN SWITCHED POWER

BUCK0_LX0 67 — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=0.5 MM, DIDT=TRUE, SWITCH_NODE=TRUE
L8100 CRITICAL 1.0UH-3.51A-0.036OHM PILE25201D
C8100–C8104 CRITICAL 15UF 20% 4V X5R 0402

BUCK0_LX1 67 — L8101 CRITICAL 1.0UH-3.51A-0.036OHM PILE25201D
C8105–C8109 CRITICAL 15UF 20% 4V X5R 0402

BUCK0_LX2 67 — L8102 CRITICAL 1.0UH-3.51A-0.036OHM PILE25201D
C8110–C8111 CRITICAL 15UF 20% 4V X5R 0402

BUCK0_LX3 67 — L8103 CRITICAL 1.0UH-3.51A-0.036OHM PILE25201D
XW8101 SM
BUCK0_FB 67 — MIN_LINE_WIDTH=0.25MM, MIN_NECK_WIDTH=0.20MM

BUCK1_LX0 67 — L8104 CRITICAL 1.0UH-3.51A-0.036OHM PILE25201D
C8112–C8116 CRITICAL 15UF 20% 4V X5R 0402

BUCK1_LX1 67 — L8105 CRITICAL 1.0UH-3.51A-0.036OHM PILE25201D
C8117–C8120 CRITICAL 15UF 20% 4V X5R 0402

BUCK1_LX2 67 — L8106 CRITICAL 1.0UH-3.51A-0.036OHM PILE25201D
XW8102 SM
BUCK1_FB 67 — MIN_LINE_WIDTH=0.25MM, MIN_NECK_WIDTH=0.20MM

BUCK2_LX0 67 — L8107 CRITICAL 1.0UH-3.51A-0.036OHM PILE25201D
C8121–C8123 CRITICAL 15UF 20% 4V X5R 0402

BUCK2_FB 67 — XW8103 SM
BUCK3_LX0 67 — L8108 CRITICAL 1.0UH-3.51A-0.036OHM PILE25201D
C8124–C8126 CRITICAL 15UF 20% 4V X5R 0402

BUCK3_FB 67 — XW8104 SM
BUCK4_LX0 67 — L8109 CRITICAL 1.0UH-3.51A-0.036OHM PILE25201D
C8127–C8129 CRITICAL 15UF 20% 4V X5R 0402

BUCK4_FB 67 — XW8105 SM
BUCK5_LX0 67 — L8110 CRITICAL 1.0UH-3.7A-0.055OHM PILE20161D-SM
C8130–C8132 CRITICAL 15UF 20% 4V X5R 0402

BUCK5_FB 67 — XW8106 SM
BUCK6_LX0 67 — L8111 CRITICAL 2.2UH-2.35A-0.073OHM PILE25201D
C81A0–C81A3 CRITICAL 10UF 20% 6.3V CERM-X5R 0402

BUCK6_FB 67 — XW8107 SM
C81A4–C81A7 CRITICAL 10UF 20% 6.3V CERM-X5R 0402

PPVDD_CPU 60 62 67 — ADDITIONAL DISTRIBUTED 27UF (NO DERATING)
PPVDD_GPU 60 62 67 — ADDITIONAL DISTRIBUTED 27UF (NO DERATING)
PPVDD_SOC 60 62 67 — ADDITIONAL DISTRIBUTED 64UF (NO DERATING)
PP1V8_S2R 55 56 60 62 67 — ADDITIONAL DISTRIBUTED 27UF (NO DERATING)
PP1V2_S2R 55 56 60 62 67 — ADDITIONAL DISTRIBUTED 64UF (NO DERATING)
PPVDD_SRAM 60 62 67 — ADDITIONAL DISTRIBUTED 32UF (NO DERATING)
PP3V3_S2R 60 62 67

PP1V8_S2R 55 56 60 62 67
PP1V8_SW1 37 59 60 62 67
PP1V8_SW2 60 62 67
PP1V8_S2R_SW3 60 62 67
PP1V2_S2R 55 56 60 62 67
PP1V2_SW1 60 62 67
PP1V2_S2R_SW2 60 62 67

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

NOTE: FOR NO BATTERY SITUATION

PPBATT_VCC 67 62 60 55
C8193 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8194 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
PPBATT_POS_RC 60 — MIN_LINE_WIDTH=0.30MM, MIN_NECK_WIDTH=0.20MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM, VOLTAGE=4.7V
R8100 0.5 1% 1/16W MF 402

PMU_VPUMP — MIN_LINE_WIDTH=0.30MM, MIN_NECK_WIDTH=0.20MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM, VOLTAGE=4.6V
C8196 0.22UF 20% 6.3V X5R 0201
C8135 1.0UF 20% 6.3V X5R 0201-1
C8136 1UF 10% 6.3V CERM 402
C8137 1.0UF 20% 6.3V X5R 0201-1
C81A8 1.0UF 20% 6.3V X5R 0201-1
C8138 1.0UF 20% 6.3V X5R 0201-1
C8139 1UF 10% 6.3V CERM 402
C81A9 1.0UF 20% 6.3V X5R 0201-1

C8137 0201 OKAY IF GRAPE HAS EXT FET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0339	128S0279	?	C8140,C8141	RDAR://PROBLEM/8967213

LDO INPUTS

PP1V8_S2R
1 CAP PER PIN
C8200 1UF 10% 6.3V CERM 402
C8203 1UF 10% 6.3V CERM 402
PP1V2_S2R
C8201 1UF 10% 6.3V CERM 402
PPVCC_MAIN
PPVCC_MAIN
PPVCC_MAIN

CRITICAL L8225 4.7UH-3.4A-0.075OHM
=PPVCC_MAIN_LED
PILE051D-SM-COMBO-J72
DCR=106MOHM MAX
CRITICAL C8226 10UF 20% 6.3V CERM-X5R 0402
CRITICAL D8228 PMEG4010BEA SOD-323
WLED_LX_A
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20 MM
NET_SPACING_TYPE=PWR
(PPLED_OUT_A)
PPLED_OUT_A
CRITICAL C8250 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8251 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8252 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8253 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8254 4.7UF 10% 35V X5R-CERM 0603
C8259 56PF 2% 50V NPO-C0G-CERM 0201

LED_IO_1_A — R8270 1.00 1% 1/32W MF 01005 — C8271 56PF 2% 50V NPO-C0G-CERM 0201 — C8270 56PF 2% 50V NPO-C0G-CERM 0201
LED_IO_2_A — R8271 1.00 1% 1/32W MF 01005
LED_IO_3_A — R8272 1.00 1% 1/32W MF 01005 — C8273 56PF 2% 50V NPO-C0G-CERM 0201 — C8272 56PF 2% 50V NPO-C0G-CERM 0201
LED_IO_4_A — R8273 1.00 1% 1/32W MF 01005
LED_IO_5_A — R8274 1.00 1% 1/32W MF 01005 — C8275 56PF 2% 50V NPO-C0G-CERM 0201 — C8274 56PF 2% 50V NPO-C0G-CERM 0201
LED_IO_6_A — R8275 1.00 1% 1/32W MF 01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1837	152S1789	?	L8225,L8255	RDAR://PROBLEM/13487208

OMIT_TABLE

U8100
D2089A0
FCBGA
SYM 2 OF 4

LDO INPUT / LDO
VDD_LDO1_3_4 T18
VDD_LDO2 B16
VDD_LDO5 U9
VDD_LDO6 U10
VDD_LDO7 U14
VDD_LDO8 U15
VDD_LDO9 B15
VDD_LDO10 B17
VDD_LDO11 U16
VDD_LDO13 T17

LCD BACKLIGHT / LCM/GRAPE
WLED_LXA0 C18
WLED_LXA1 C19
VOUT_WLED_A D16
WLED1_A E14
WLED2_A F14
WLED3_A G14
WLED4_A H14
WLED5_A J14
WLED6_A J16
WLED_LXB0 E18
WLED_LXB1 E19
VOUT_WLED_B E16
WLED1_B K14
WLED2_B L14
WLED3_B M14
WLED4_B M16
WLED5_B N14
WLED6_B P14

XTAL
XTAL1 V18
XTAL2 V17

LED_IO1_A_R
LED_IO2_A_R
LED_IO3_A_R
LED_IO4_A_R
LED_IO5_A_R
LED_IO6_A_R
NET_SPACING_TYPE=PWR
LED_IO1_B_R
LED_IO2_B_R
LED_IO3_B_R
LED_IO4_B_R
LED_IO5_B_R
LED_IO6_B_R

LDO OUTPUTS

VLDO1 U19 (50MA; 2.5-3.3V) PP3V0_SPARE1
VLDO2 A16 (100MA; 1.65-1.805V; BUCK3) PP1V7_VA_VCP
VLDO3 U18 (50MA; 2.5-3.3V) PP3V0_S2R_SENSOR
VLDO4 T19 (50MA; 2.5-3.3V) PP3V0_ALS
VLDO5 V9 (1000MA; 2.5-3.6V) PP3V0_UVLO
VLDO6 V10 (150MA; 2.5-3.6V) PP3V3_ACC
VLDO7 V14 (300MA; 1.7-3.0V) PP3V0_S2R_TRISTAR
VLDO8 V15 (300MA; 1.7-3.0V) PP3V0_S2R_HALL
VLDO9 A15 (300MA; 1.2-3.0V) PP1V3_CAM
VLDO10 A17 (150MA; 0.6-1.3V) PP1V0_SOC
VLDO11 V16 (300MA; 1.7-3.0V) PP2V6_CAM_AF
VLDO13 U17 (300MA; 1.7-3.0V) PP2V9_CAM
ON_BUF T10 (5MA; 1.8V; ON BUFF) PP1V8_ALWAYS

VDD_LCM_SW C17 =PPVCC_MAIN_VDD_LCM
VDD_BOOST_LCM A18 PP6V0_LCM_HI (NOTE: 2MHZ)
BOOST_LCM_LX B19 LCM_LX
LCM_FB C15
VDD_LCM U11 PP6V0_LCM_VBOOST
VLCM1 V11 (100MA; 5.0-6.0V) PP5V25_GRAPE
VLCM2 V12 (100MA; 5.0-6.0V) NO_TEST=TRUE NC_VLCM2
LCM2_EN E8 LCM2_EN
VLCM3 U12 (5MA; 5.0-6.0V) NO_TEST=TRUE NC_VLCM3

CRITICAL L8229 2.2UH-1.05A-0.195OHM MLS201612E-SM
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
CRITICAL D8230 PMEG2005AEL SOD882
MAKE_BASE=TRUE VOLTAGE=6.0V MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM
C8212 10UF 20% 6.3V X5R-CERM 0603
C8210 2.2UF 10% 6.3V X5R-CERM 402
CRITICAL C8211 10UF 20% 6.3V X5R-CERM 0402-2

R8250 1K 5% 1/20W MF 201

CRITICAL Y8200 32.768K-20PPM-12.5PF 2012-1
CRITICAL C8215 18PF 5% 25V C0G-CERM 0201
CRITICAL C8216 18PF 5% 25V C0G-CERM 0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392	?	Y8200	RDAR://PROBLEM/9936684

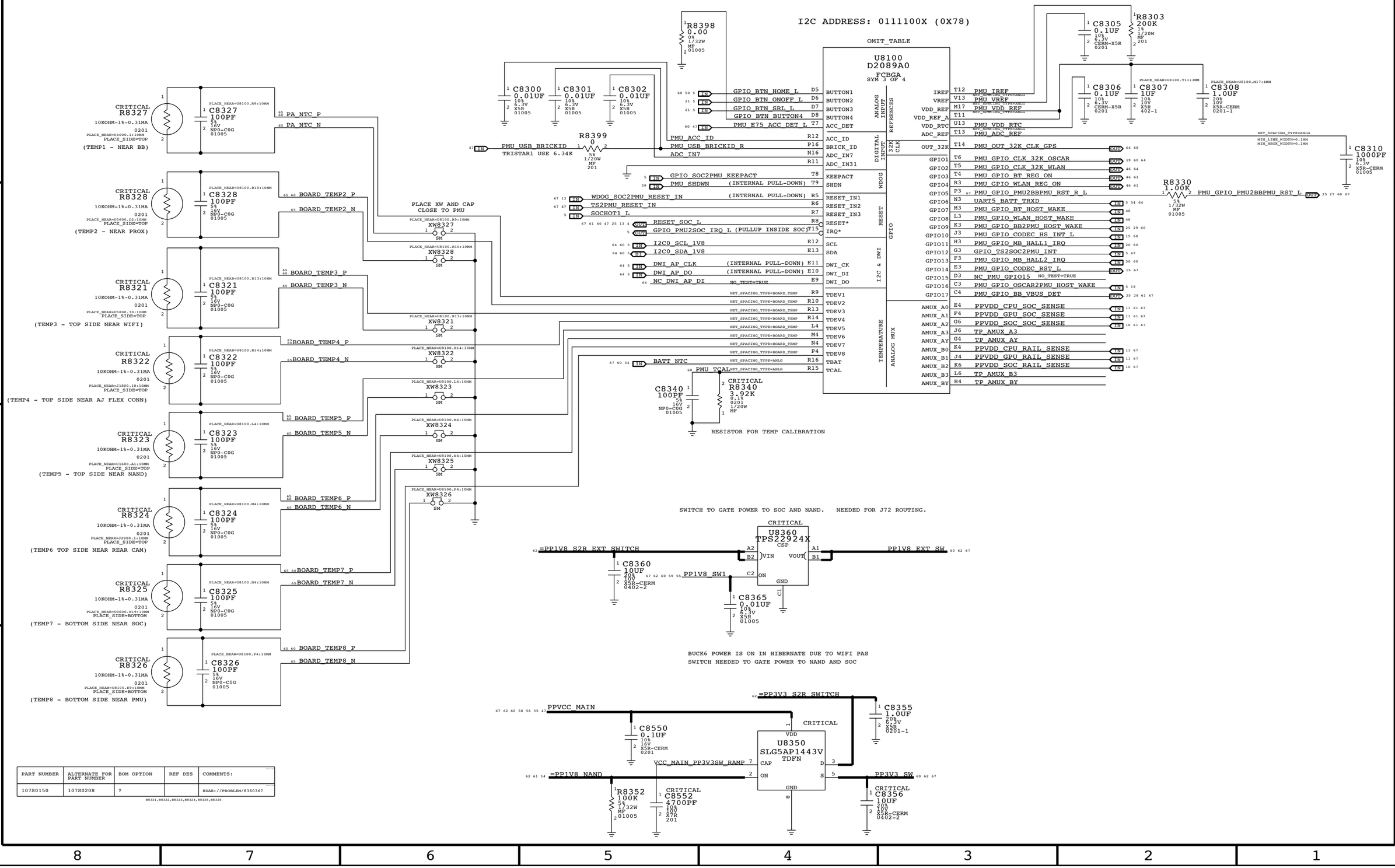
LDO BYPASS

PP3V0_SPARE1
PP1V7_VA_VCP
PP3V0_S2R_TRISTAR
PP3V0_ALS
PP3V0_UVLO
PP3V3_ACC
PP3V0_S2R_HALL
PP3V0_S2R_SENSOR
CRITICAL C8237 2.2UF 10% 6.3V X5R 402
CRITICAL C8236 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8235 4.7UF 20% 6.3V X5R-CERM 402
CRITICAL C8234 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8233 2.2UF 10% 6.3V X5R 402
CRITICAL C8232 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8231 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8230 2.2UF 10% 6.3V X5R 402

PP1V3_CAM
PP1V0_SOC
PP2V6_CAM_AF
PP2V9_CAM
PP1V8_ALWAYS
C8242 0.22UF 10% 6.3V X5R 0201
CRITICAL C8241 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8240 4.7UF 20% 6.3V X5R-CERM 402
CRITICAL C8239 4.7UF 20% 6.3V X5R-CERM 402
CRITICAL C8238 4.7UF 20% 6.3V X5R-CERM 402

CRITICAL L8255 4.7UH-3.4A-0.075OHM
=PPVCC_MAIN_LED
PILE051D-SM-COMBO-J72
DCR=106MOHM MAX
CRITICAL C8256 10UF 20% 6.3V CERM-X5R 0402
CRITICAL D8258 PMEG4010BEA SOD-323
WLED_LX_B
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20 MM
(PPLED_OUT_B)
PPLED_OUT_B
CRITICAL C8260 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8261 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8262 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8263 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8264 4.7UF 10% 35V X5R-CERM 0603
C8269 56PF 2% 50V NPO-C0G-CERM 0201

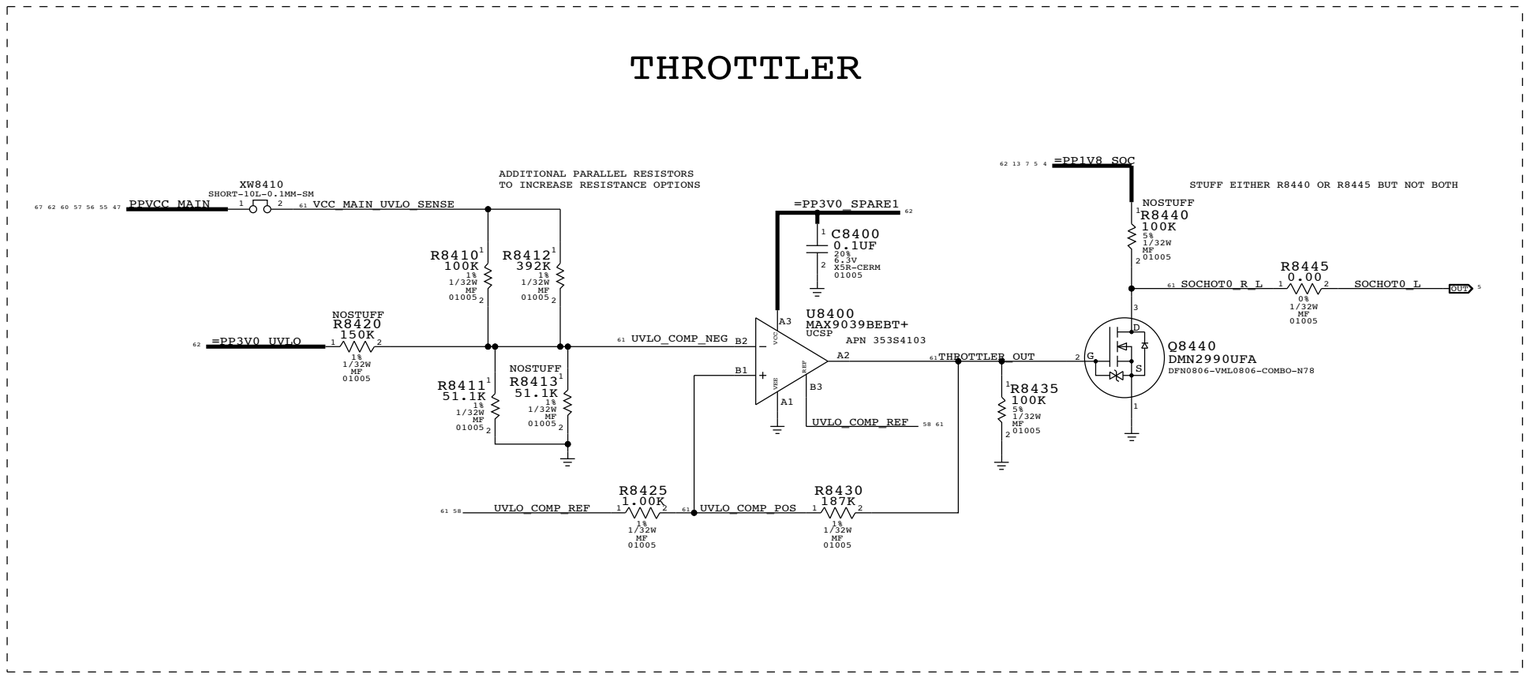
LED_IO_1_B — R8280 1.00 1% 1/32W MF 01005
LED_IO_2_B — R8281 1.00 1% 1/32W MF 01005 — C8280 56PF 2% 50V NPO-C0G-CERM 0201 — C8281 56PF 2% 50V NPO-C0G-CERM 0201 — C8282 56PF 2% 50V NPO-C0G-CERM 0201
LED_IO_3_B — R8282 1.00 1% 1/32W MF 01005
LED_IO_4_B — R8283 1.00 1% 1/32W MF 01005
LED_IO_5_B — R8284 1.00 1% 1/32W MF 01005 — C8283 56PF 2% 50V NPO-C0G-CERM 0201 — C8284 56PF 2% 50V NPO-C0G-CERM 0201 — C8285 56PF 2% 50V NPO-C0G-CERM 0201
LED_IO_6_B — R8285 1.00 1% 1/32W MF 01005

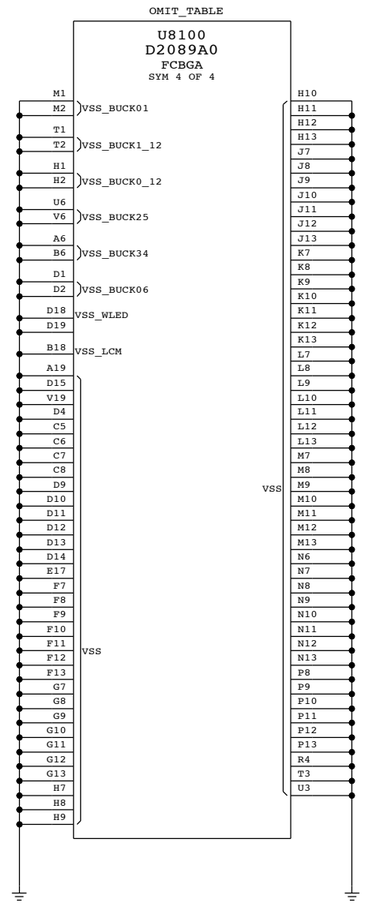


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	?		RDAR://PROBLEM/8380367

R8321,R8322,R8323,R8324,R8325,R8326

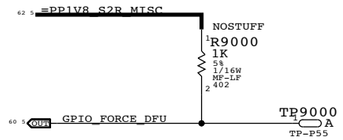
THROTTLER

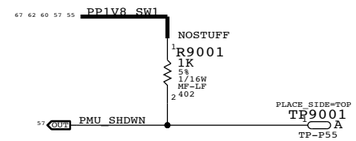




ADD A VIA PER PIN FOR ALL VSS_* AND VSSA_* PINS

DEBUG RESET ACCESS





SMT TEST FIXTURE TP

POWER

PPVDD_CPU	FUNC_TEST=TRUE	55 62 67
PPVDD_GPU	FUNC_TEST=TRUE	55 62 67
PPVDD_SOC	FUNC_TEST=TRUE	55 62 67
PP1V8_S2R	FUNC_TEST=TRUE	55 56 62 67
PP1V8_SW1	FUNC_TEST=TRUE	55 57 59 62 67
PP1V8_SW1_FOREHEAD	FUNC_TEST=TRUE	62 67
PP1V8_EXT_SW	FUNC_TEST=TRUE	57 62 67
PP1V8_SW2	FUNC_TEST=TRUE	55 62 67
PP1V8_S2R_SW3	FUNC_TEST=TRUE	55 62 67
PP1V8_S2R_SW3_COMP	FUNC_TEST=TRUE	62 67
PP1V2_S2R	FUNC_TEST=TRUE	55 56 62 67
PP1V2_SW1	FUNC_TEST=TRUE	55 62 67
PP1V2_S2R_SW2	FUNC_TEST=TRUE	55 62 67
PPVDD_SRAM	FUNC_TEST=TRUE	55 62 67
PP3V3_S2R	FUNC_TEST=TRUE	55 62 67
PP3V3_SW	FUNC_TEST=TRUE	57 62 67
PP3V0_SPARE1	FUNC_TEST=TRUE	56 62 67
PP1V7_VA_VCP	FUNC_TEST=TRUE	56 62 67
PP3V0_S2R_SENSOR	FUNC_TEST=TRUE	56 62 67
PP3V0_ALS	FUNC_TEST=TRUE	56 62 67
PP3V3_ACC	FUNC_TEST=TRUE	56 62 67
PP3V0_S2R_TRISTAR	FUNC_TEST=TRUE	56 62 67
PP3V0_S2R_HALL	FUNC_TEST=TRUE	56 62 67
PP1V3_CAM	FUNC_TEST=TRUE	56 62 67
PP1V0_SOC	FUNC_TEST=TRUE	56 62 67
PP2V6_CAM_AF	FUNC_TEST=TRUE	56 62 67
PP2V9_CAM	FUNC_TEST=TRUE	56 62 67
PP5V25_GRAPE	FUNC_TEST=TRUE	56 60 62 67
PPVCC_MAIN	FUNC_TEST=TRUE	47 55 56 57 58 62 67
PPBATT_VCC	FUNC_TEST=TRUE	55 60 62 67
PPVBUS_USB_DCIN	FUNC_TEST=TRUE	55 62 67
PP1V8_ALWAYS	FUNC_TEST=TRUE	56 62 67
PPLED_OUT_A	FUNC_TEST=TRUE	56 62 67
PPLED_OUT_B	FUNC_TEST=TRUE	56 62 67
PP6V0_LCM_VBOOST	FUNC_TEST=TRUE	56 67

PPBATT_POS_RC	FUNC_TEST=TRUE	55
PMU_VCENTER	FUNC_TEST=TRUE	55 67
PPVBUS_PROT	FUNC_TEST=TRUE	47 55 67
VBUS_PROT_G	FUNC_TEST=TRUE	55

PP1V2_CAM_FRONT_FILT	FUNC_TEST=TRUE	67
PP1V3_CAM_REAR_FILT	FUNC_TEST=TRUE	23 67
PP1V7_VCP	FUNC_TEST=TRUE	15 67
PP1V8_CAM_FRONT_FILT	FUNC_TEST=TRUE	22 67
PP1V8_CAM_REAR_FILT	FUNC_TEST=TRUE	23 67
PP1V8_DMIC_FILT	FUNC_TEST=TRUE	16 67
PP1V8_GRAPE_SW	FUNC_TEST=TRUE	51 52 61 67
PP1V8_COMP	FUNC_TEST=TRUE	24 67
PP2V6_CAM_REAR_AF_FILT	FUNC_TEST=TRUE	23 67
PP2V9_AVDD_CAM_FRONT_FILT	FUNC_TEST=TRUE	22 67
PP2V9_AVDD_CAM_REAR_FILT	FUNC_TEST=TRUE	23 67
PP3V0_ALS_FILT	FUNC_TEST=TRUE	22 67
PP3V0_HP_ALS_FILT	FUNC_TEST=TRUE	67
PP3V0_IO_ALS_FILT	FUNC_TEST=TRUE	67
PP3V0_S2R_HALL_FILT	FUNC_TEST=TRUE	20 50 67

PP3V0_GYRO	FUNC_TEST=TRUE	19 67
PP3V0_ACCEL	FUNC_TEST=TRUE	19 67
PP3V0_COMP	FUNC_TEST=TRUE	24 67
PP3V0_SENSOR_PROX_FILT	FUNC_TEST=TRUE	67
PP3V0_SENSOR_PROX_ADUX1049_FILT	FUNC_TEST=TRUE	67
PP3V0_SENSOR_PROX_AD7149_FILT	FUNC_TEST=TRUE	45 67
PP5V25_GRAPE	FUNC_TEST=TRUE	56 60 62 67
PPVCC_MAIN_LCD_SW_CONN	FUNC_TEST=TRUE	53 67
PPVCC_MAIN_LCD_SW	FUNC_TEST=TRUE	53 67

PP_SMPS1_MSMC_1V05	FUNC_TEST=TRUE	26 28 68
PP_SMPS2_RF1_1V3	FUNC_TEST=TRUE	26 28 31 68
PP_SMPS3_MSME_1V8	FUNC_TEST=TRUE	25 26 28 29 31
PP_SMPS4_RF2_2V05	FUNC_TEST=TRUE	26 31 68
PP_SMPS5_DSP_1V05	FUNC_TEST=TRUE	26 68

PP_LDO1	FUNC_TEST=TRUE	26 68

PP3V0_UVLO	FUNC_TEST=TRUE	56 62 67

TP_BB_TEST_MODE_0	FUNC_TEST=TRUE	28
TP_BB_TEST_MODE_1	FUNC_TEST=TRUE	28

GPIO_SOC2OSCAR_DBGEN_R	FUNC_TEST=TRUE	19

TP9300 A TP-1P0-TOP — PPBATT_VCC — PLACE_NEAR=J7500.4:10MM — 55 60 62 67

TP9301 A TP-1P0-TOP — PPBATT_VCC — PLACE_NEAR=J7500.4:10MM — 55 60 62 67

TP9302 A TP-1P0-TOP — PPBATT_VCC — PLACE_NEAR=J7500.4:10MM — 55 60 62 67

TP9305 A TP-1P0-TOP — PLACE_NEAR=J7500.3:10MM

TP9306 A TP-1P0-TOP — PLACE_NEAR=J7500.3:10MM

TP9307 A TP-1P0-TOP — PLACE_NEAR=J7500.3:10MM

TP9310 A TP-1P0-TOP — PPVBUS_E75_USB_CONN — PLACE_NEAR=J6200.9:20MM — 48 49 60 67

TP9311 A TP-1P0-TOP — PPVBUS_E75_USB_CONN — PLACE_NEAR=J6200.9:20MM — 48 49 60 67

TP9312 A TP-1P0-TOP — PPVBUS_E75_USB_CONN — PLACE_NEAR=J6200.9:20MM — 48 49 60 67

TP9315 A TP-1P0-TOP — PLACE_NEAR=TP9310.1:30MM

TP9316 A TP-1P0-TOP — PLACE_NEAR=TP9310.1:30MM

TP9317 A TP-1P0-TOP — PLACE_NEAR=TP9310.1:30MM

GPIO

GPIO_CAM_ALS2SOC_IRQ_L_F	FUNC_TEST=TRUE	22
GPIO_FORCE_DFU	FUNC_TEST=TRUE	5 59
GPIO_GRAPE2SOC_IRQ_FILT_L	FUNC_TEST=TRUE	
GPIO_SOC2BB_RADIO_ON_L	FUNC_TEST=TRUE	5 25 27
GPIO_SOC2BB_RST_L	FUNC_TEST=TRUE	5 25 27 67
GPIO_SOC2GRAPE_RESET_FILT_L	FUNC_TEST=TRUE	5 52 61 67
GPIO_OSCAR_RESET_L	FUNC_TEST=TRUE	5 19 67
CLK_32K_SOC2CUMULUS_FILT	FUNC_TEST=TRUE	64
HP_ALS_IRQ_L_CONN_FILT	FUNC_TEST=TRUE	

PMU GPIO

PMU_GPIO_BB2PMU_HOST_WAKE	FUNC_TEST=TRUE	25 29 57
PMU_GPIO_BT_REG_ON_R	FUNC_TEST=TRUE	46
PMU_GPIO_CLK_32K_OSCAR	FUNC_TEST=TRUE	19 57 64
PMU_GPIO_CLK_32K_WLAN_R	FUNC_TEST=TRUE	46
PMU_GPIO_CODEC_HS_INT_L	FUNC_TEST=TRUE	15 57
PMU_GPIO_PMU2BBPMU_RST_L	FUNC_TEST=TRUE	25 27 57 67
PMU_GPIO_WLAN_REG_ON_R	FUNC_TEST=TRUE	46
PMU_TCAL	FUNC_TEST=TRUE	57
PMU_E75_ACC_DET_L	FUNC_TEST=TRUE	47 57
TS_E75_ACC_DET_L	FUNC_TEST=TRUE	47
PMU_GPIO_MB_HALL1_IRQ	FUNC_TEST=TRUE	20 57
PMU_GPIO_MB_HALL2_IRQ	FUNC_TEST=TRUE	50 57

AUDIO

CONN_HP_HEADSET_DET_FILT	FUNC_TEST=TRUE	15 16
CONN_HP_HS3_FILT	FUNC_TEST=TRUE	15 16 60 65
CONN_HP_HS3_REF_FILT	FUNC_TEST=TRUE	15 16 60 65
CONN_HP_HS3_FILT	FUNC_TEST=TRUE	15 16 60 65
CONN_HP_HS3_REF_FILT	FUNC_TEST=TRUE	15 16 60 65
CONN_HP_HS4_FILT	FUNC_TEST=TRUE	15 16 65
CONN_HP_HS4_REF_FILT	FUNC_TEST=TRUE	15 16 65
CONN_HP_LEFT_FILT	FUNC_TEST=TRUE	15 16 65
CONN_HP_RIGHT_FILT	FUNC_TEST=TRUE	15 16 65
SPKRAMP_L1_OUT_N	FUNC_TEST=TRUE	18 49 65
SPKRAMP_L1_OUT_P	FUNC_TEST=TRUE	18 49 65
SPKRAMP_R1_OUT_N	FUNC_TEST=TRUE	17 49 65
SPKRAMP_R1_OUT_P	FUNC_TEST=TRUE	17 49 65
SPKRAMP_L2_OUT_N	FUNC_TEST=TRUE	18 49 65
SPKRAMP_L2_OUT_P	FUNC_TEST=TRUE	18 49 65
SPKRAMP_R2_OUT_N	FUNC_TEST=TRUE	17 49 65
SPKRAMP_R2_OUT_P	FUNC_TEST=TRUE	17 49 65
LEFT_CH_OUT_P	FUNC_TEST=TRUE	15 18 65
LEFT_CH_OUT_N	FUNC_TEST=TRUE	15 18 65
RIGHT_CH_OUT_P	FUNC_TEST=TRUE	15 17 65
RIGHT_CH_OUT_N	FUNC_TEST=TRUE	15 17 65
AIN3P	FUNC_TEST=TRUE	15
AIN3N	FUNC_TEST=TRUE	15
GND_AUDIO_CODEC	FUNC_TEST=TRUE	15 67
DMIC1_FF_SCLK_FILT	FUNC_TEST=TRUE	16 64
DMIC1_FF_SD_FILT	FUNC_TEST=TRUE	16 64
L81_SPEAKER_VO	FUNC_TEST=TRUE	15

GRAPE

GPIO_GRAPE2SOC_IRQ_L	FUNC_TEST=TRUE	5 52 61
GPIO_SOC2GRAPE_RESET_L	FUNC_TEST=TRUE	5 52 61 67
CLK_32K_SOC2CUMULUS	FUNC_TEST=TRUE	5 52 61 64
DISPLAY_SYNC	FUNC_TEST=TRUE	5 52 61
SPI2_GRAPE_SCLK	FUNC_TEST=TRUE	5 52 61 64
SPI2_GRAPE_MISO	FUNC_TEST=TRUE	5 52 61 64
SPI2_GRAPE_MOSI	FUNC_TEST=TRUE	5 52 61 64
SPI2_GRAPE_CS_L	FUNC_TEST=TRUE	5 52 61 64
VCC_MAIN_GRAPE_RAMP	FUNC_TEST=TRUE	51

UART

UART0_SOC_RXD	FUNC_TEST=TRUE	5 47 64
UART0_SOC_TXD	FUNC_TEST=TRUE	5 47 64

TEST POINT RULES:
CENTER TO CENTER SPACING >= 1MM
DIAMETER >= 0.5MM
EDGE TO SHIELD >=0.55MM

BACKLIGHT

PPLED_BACK_REG_A	FUNC_TEST=TRUE	53 67
LED_IO_1_A	FUNC_TEST=TRUE	53 56 65
LED_IO_2_A	FUNC_TEST=TRUE	53 56 65
LED_IO_3_A	FUNC_TEST=TRUE	53 56 65
LED_IO_4_A	FUNC_TEST=TRUE	53 56 65
LED_IO_5_A	FUNC_TEST=TRUE	53 56 65
LED_IO_6_A	FUNC_TEST=TRUE	53 56 65

PPLED_BACK_REG_B	FUNC_TEST=TRUE	53 67
LED_IO_1_B	FUNC_TEST=TRUE	53 56 65
LED_IO_2_B	FUNC_TEST=TRUE	53 56 65
LED_IO_3_B	FUNC_TEST=TRUE	53 56 65
LED_IO_4_B	FUNC_TEST=TRUE	53 56 65
LED_IO_5_B	FUNC_TEST=TRUE	53 56 65
LED_IO_6_B	FUNC_TEST=TRUE	53 56 65

BATTERY

BATT_SWI_CONN	FUNC_TEST=TRUE	54 64
BATT_NTC	FUNC_TEST=TRUE	54 57 60 67

E75

E75_ACC_DET_CONN_L	FUNC_TEST=TRUE	47 49 60
PPOUT_E75_ACC_ID1_CONN	FUNC_TEST=TRUE	48 49 60 67
PPOUT_E75_ACC_ID2_CONN	FUNC_TEST=TRUE	48 49 60 67
E75_DPAIR1_CONN_P	FUNC_TEST=TRUE	47 49 60 64
E75_DPAIR1_CONN_N	FUNC_TEST=TRUE	47 49 60 64
E75_DPAIR2_CONN_P	FUNC_TEST=TRUE	47 49 60 64
E75_DPAIR2_CONN_N	FUNC_TEST=TRUE	47 49 60 64
PPVBUS_E75_USB_CONN	FUNC_TEST=TRUE	48 49 60 67

REEST JTAG/CONFIG

JTAG_SOC_SEL	FUNC_TEST=TRUE	4 13
JTAG_SOC_TCK	FUNC_TEST=TRUE	4 47 64
JTAG_SOC_TDI	FUNC_TEST=TRUE	4 64
TP_JTAG_SOC_TDO	FUNC_TEST=TRUE	4 64
JTAG_SOC_TMS	FUNC_TEST=TRUE	4 47 64
JTAG_SOC_TRST_L	FUNC_TEST=TRUE	4 13 64
SOC_TESTMODE	FUNC_TEST=TRUE	4 13
RESET_SOC_L	FUNC_TEST=TRUE	4 13 25 47 57 61 67
PS_HOLD_PMIC	FUNC_TEST=TRUE	25 27

BUTTONS

GPIO_BTN_ONOFF_L_FILT	FUNC_TEST=TRUE	21
GPIO_BTN_HOME_L	FUNC_TEST=TRUE	5 50 57
GPIO_BTN_VOL_UP_L_FILT	FUNC_TEST=TRUE	21
GPIO_BTN_VOL_DOWN_L_FILT	FUNC_TEST=TRUE	21
GPIO_BTN_SRL_L_FILT	FUNC_TEST=TRUE	21

BOARD TEMP

PA_NTC_P	FUNC_TEST=TRUE	57 65
BOARD_TEMP2_P	FUNC_TEST=TRUE	57 65
BOARD_TEMP3_P	FUNC_TEST=TRUE	57 65
BOARD_TEMP4_P	FUNC_TEST=TRUE	57 65
BOARD_TEMP5_P	FUNC_TEST=TRUE	57 65
BOARD_TEMP6_P	FUNC_TEST=TRUE	57 65
BOARD_TEMP7_P	FUNC_TEST=TRUE	57 65
BOARD_TEMP8_P	FUNC_TEST=TRUE	57 65

USB

USB_SOC_N	FUNC_TEST=TRUE	4 47 64
USB_SOC_P	FUNC_TEST=TRUE	4 47 64

CAMERA

ISP0_CAM_REAR_CLK_F	FUNC_TEST=TRUE	23 64
ISP0_CAM_REAR_SCL_F	FUNC_TEST=TRUE	23 64
ISP0_CAM_REAR_SDA_F	FUNC_TEST=TRUE	23 64
ISP0_CAM_REAR_SHUTDOWN_L_F	FUNC_TEST=TRUE	23 67
ISP1_CAM_FRONT_CLK_F	FUNC_TEST=TRUE	22 64
ISP1_CAM_FRONT_SCL_F	FUNC_TEST=TRUE	22 64
ISP1_CAM_FRONT_SDA_F	FUNC_TEST=TRUE	22 64
ISP1_CAM_FRONT_SHUTDOWN_L_F	FUNC_TEST=TRUE	22 67

NAND

FMI0_CE0_L	FUNC_TEST=TRUE	6 14 61 66

DISPLAY

DISPLAY_SYNC_FILT	FUNC_TEST=TRUE	

I2C

I2C3_CAM_ALS_SCL_1V8_F	FUNC_TEST=TRUE	22 64
I2C3_CAM_ALS_SDA_1V8_F	FUNC_TEST=TRUE	22 64
I2C0_HP_ALS_SCL_1V8_FILT	FUNC_TEST=TRUE	64
I2C0_HP_ALS_SDA_1V8_FILT	FUNC_TEST=TRUE	64
I2C0_SCL_1V8	FUNC_TEST=TRUE	5 57 64
I2C0_SDA_1V8	FUNC_TEST=TRUE	5 57 64

SIM

SIMCRD_RST_CONN	FUNC_TEST=TRUE	29 44
SIMCRD_CLK_CONN	FUNC_TEST=TRUE	29 44
SIMCRD_IO_CONN	FUNC_TEST=TRUE	29 44
SIM_TRAY_DETECT	FUNC_TEST=TRUE	29 44
PP_LDO6_RUIM_1V8	FUNC_TEST=TRUE	26 28 44 68

RF FIXTURE

E75_DPAIR1_CONN_N	FUNC_TEST=TRUE	47 49 60 64
E75_DPAIR1_CONN_P	FUNC_TEST=TRUE	47 49 60 64
E75_DPAIR2_CONN_N	FUNC_TEST=TRUE	47 49 60 64
E75_DPAIR2_CONN_P	FUNC_TEST=TRUE	47 49 60 64
PPVBUS_E75_USB_CONN	FUNC_TEST=TRUE	48 49 60 67
PPOUT_E75_ACC_ID1_CONN	FUNC_TEST=TRUE	48 49 60 67
PPOUT_E75_ACC_ID2_CONN	FUNC_TEST=TRUE	48 49 60 67
E75_ACC_DET_CONN_L	FUNC_TEST=TRUE	47 49 60
BATT_NTC	FUNC_TEST=TRUE	54 57 60 67

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

SL9300 TH-NSP 1 — SL-1.1X0.4-1.4X0.7
SL9301 TH-NSP 1 — SL-1.1X0.4-1.4X0.7
SL9302 TH-NSP 1 — SL-1.1X0.4-1.4X0.7
SL9310 TH-NSP 1 — SL-1.1X0.4-1.4X0.7
SL9311 TH-NSP 1 — SL-1.1X0.4-1.4X0.7

FOREHEAD B2B STANDOFFS

STD9300 STDOFF-3.3X1.8R1.17H-SM-1 1
STD9301 STDOFF-3.3X1.8R1.17H-SM-1 1
STD9302 STDOFF-3.3X1.8R1.02H-SM 1 — NOTE: BOTTOM OF FOREHEAD

GRAPE AND DISPLAY B2B STANDOFFS

STD9305 STDOFF-3.3X1.8R1.17H-SM-1 1
STD9306 STDOFF-3.3X1.8R1.17H-SM-1 1
STD9307 STDOFF-3.3X1.8R1.17H-SM-1 1

FID9300 FID 0P5SM1POSQ-NSP 1
FID9301 FID 0P5SM1POSQ-NSP 1
FID9302 FID 0P5SM1POSQ-NSP 1
FID9303 FID 0P5SM1POSQ-NSP 1
FID9304 FID 0P5SM1POSQ-NSP 1
FID9305 FID 0P5SM1POSQ-NSP 1

EE CHARACTERIZATION TP

NAND

BOTTOM SIDE PP9460 P4MM SM (PP) 1 FMI0_AD<0> PLACE_SIDE=BOTTOM PLACE_NEAR=U0600.AJ32:2MM 6 14 61 66
NO_XNET_CONNECTION=TRUE

BOTTOM SIDE PP9461 P4MM SM (PP) 1 FMI0_DQS PLACE_SIDE=BOTTOM PLACE_NEAR=U0600.BJ34:2MM 6 14 61 66
NO_XNET_CONNECTION=TRUE

FMI0_AD<0..7>	EE_TEST=TRUE	FUNC_TEST=TRUE	6 14 61 66
FMI0_CE0_L		FUNC_TEST=TRUE	6 14 60 66
FMI0_ALE		FUNC_TEST=TRUE	6 14 66
FMI0_CLE		FUNC_TEST=TRUE	6 14 66
FMI0_WE_L		FUNC_TEST=TRUE	6 14 66
FMI0_RE_L		FUNC_TEST=TRUE	6 14 66
FMI0_DQS		FUNC_TEST=TRUE	6 14 61 66
FMI1_AD<0>		FUNC_TEST=TRUE	6 14 66
FMI1_CE0_L			6 14 66
FMI1_ALE			6 14 66
FMI1_CLE			6 14 66
FMI1_WE_L			6 14 66
FMI1_RE_L			6 14 66
FMI1_DQS			6 14 66
PPVREF_FMI_SOC		FUNC_TEST=TRUE	6 66
PPVREF_FMI_NAND		FUNC_TEST=TRUE	14 66

TOP SIDE PP9440 P4MM SM (PP) 1 TP_FMI_TCKC_NAND PLACE_SIDE=TOP 14

TOP SIDE PP9441 P4MM SM (PP) 1 TP_FMI_TMSC_NAND PLACE_SIDE=TOP 14

TOP SIDE PP9442 P4MM SM (PP) 1 =PP1V8_NAND PLACE_SIDE=TOP 14 57 62

TOP SIDE PP9443 P4MM SM (PP) 1 GND PLACE_SIDE=TOP

EE

TOP SIDE PP9450 P4MM SM (PP) 1 RESET_SOC_L 4 13 25 47 57 60 67

PP9451 P4MM SM (PP) 1 TP_ANALOGMUXOUT 4

TOP SIDE PP9452 P4MM SM (PP) 1 SOCHOT0_R_L 58

TP_GPIO_DFU_STATUS	FUNC_TEST=TRUE	5

CAMERA

PP9470 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_CLK_P PLACE_NEAR=U0600.AM35:3MM 7 22 61 65
NO_XNET_CONNECTION=TRUE

PP9471 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_CLK_N PLACE_NEAR=U0600.AM36:3MM 7 22 61 65
NO_XNET_CONNECTION=TRUE

PP9472 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_DATA_P<0> PLACE_NEAR=U0600.AN35:3MM 7 22 61 65
NO_XNET_CONNECTION=TRUE

PP9473 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_DATA_N<0> PLACE_NEAR=U0600.AN36:3MM 7 22 61 65
NO_XNET_CONNECTION=TRUE

PP9474 P4MM SM (PP) 1 MIPI0C_CAM_REAR_CLK_P PLACE_NEAR=U0600.AR31:3MM 7 23 61 65
NO_XNET_CONNECTION=TRUE

PP9475 P4MM SM (PP) 1 MIPI0C_CAM_REAR_CLK_N PLACE_NEAR=U0600.AT31:3MM 7 23 61 65
NO_XNET_CONNECTION=TRUE

PP9476 P4MM SM (PP) 1 MIPI0C_CAM_REAR_DATA_P<0> PLACE_NEAR=U0600.AR33:3MM 7 23 61 65
NO_XNET_CONNECTION=TRUE

PP9477 P4MM SM (PP) 1 MIPI0C_CAM_REAR_DATA_N<0> PLACE_NEAR=U0600.AT33:3MM 7 23 61 65
NO_XNET_CONNECTION=TRUE

FOR FRANK (SEG)

PP9400 P4MM SM (PP) 1 PPVDD_SOC_SOC_SENSE PLACE_NEAR=U0600.V31:1MM 10 57 67

PP9401 P4MM SM (PP) 1 PPVDD_CPU_SOC_SENSE PLACE_NEAR=U0600.AL31:1MM 11 57 67

PP9402 P4MM SM (PP) 1 PPVDD_GPU_SOC_SENSE PLACE_NEAR=U0600.AA7:1MM 11 57 67

DRAM

NEAR DRAM

PP9410 P4MM SM (PP) 1 DDR0_CK_N PLACE_NEAR=U1400.AF14:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9411 P4MM SM (PP) 1 DDR0_CK_P PLACE_NEAR=U1400.AF15:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9412 P4MM SM (PP) 1 DDR0_CKE<0> PLACE_NEAR=U1400.AF16:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9413 P4MM SM (PP) 1 DDR0_CKE<1> PLACE_NEAR=U1400.AE17:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9414 P4MM SM (PP) 1 DDR0_CA<0> PLACE_NEAR=U1400.AE21:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9415 P4MM SM (PP) 1 DDR0_DQ<2> PLACE_NEAR=U1400.B18:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9416 P4MM SM (PP) 1 DDR0_DQS_N<3> PLACE_NEAR=U1400.C8:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9417 P4MM SM (PP) 1 DDR0_DQS_P<3> PLACE_NEAR=U1400.B8:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9418 P4MM SM (PP) 1 DDR0_DQS_N<0> PLACE_NEAR=U1400.C15:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9419 P4MM SM (PP) 1 DDR0_DQS_P<0> PLACE_NEAR=U1400.B15:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9420 P4MM SM (PP) 1 DDR1_CK_N PLACE_NEAR=U1400.T26:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9421 P4MM SM (PP) 1 DDR1_CK_P PLACE_NEAR=U1400.R26:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9422 P4MM SM (PP) 1 DDR1_CKE<0> PLACE_NEAR=U1400.P26:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9423 P4MM SM (PP) 1 DDR1_CKE<1> PLACE_NEAR=U1400.N25:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9424 P4MM SM (PP) 1 DDR1_CA<0> PLACE_NEAR=U1400.J25:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9425 P4MM SM (PP) 1 DDR1_CA<1> PLACE_NEAR=U1400.K26:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9426 P4MM SM (PP) 1 DDR1_CA<2> PLACE_NEAR=U1400.K25:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9427 P4MM SM (PP) 1 DDR1_CA<3> PLACE_NEAR=U1400.L25:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9428 P4MM SM (PP) 1 DDR1_CSN<0> PLACE_NEAR=U1400.N35:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

NEAR SOC

PP9435 P4MM SM (PP) 1 DDR0_DQ<28> PLACE_NEAR=U0600.D5:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9436 P4MM SM (PP) 1 DDR0_DQS_N<3> PLACE_NEAR=U0600.A6:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9437 P4MM SM (PP) 1 DDR0_DQS_P<3> PLACE_NEAR=U0600.A5:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

GRAPE

CONVERT TO PROBE POINTS IF NOT ABLE TO PLACE TESTPOINT

TP_JTAG_CUMULUS_M_TCK	52 64
TP_JTAG_CUMULUS_M_TDI	52 64
JTAG_CUMULUS_M_TMS	52 64
TP_JTAG_CUMULUS_M_TDO	52 64
DISPLAY_SYNC	4 52 60
CUMULUS_MS_CK	52 64
CUMULUS_MS_SD	52 64
GPIO_GRAPE2SOC_IRQ_L	5 52 60
GPIO_SOC2GRAPE_RESET_L	5 52 60 67
CLK_32K_SOC2CUMULUS	5 52 60 64
SPI2_GRAPE_MOSI	5 52 60 64
SPI2_GRAPE_MISO	5 52 60 64
SPI2_GRAPE_SCLK	5 52 60 64
SPI2_GRAPE_CS_L	5 52 60 64
TP_CUMULUS_S_H_CS_L	52
TP_CUMULUS_S_H_SCLK	52
TP_CUMULUS_S_H_SDI	52
TP_CUMULUS_S_H_SDO	52
=PP5V25_GRAPE	52 62
PP1V8_GRAPE_SW	51 52 60 67

GRAPE NO_TEST

MT_PANEL_IN<0..29>	NO_TEST=TRUE	52 65
MT_PANEL_OUT<0..39>	NO_TEST=TRUE	52 65

AUDIO

L81_DMIC1_FF_SD FUNC_TEST=TRUE 15

WIFI

JTAG_WLAN_TMS_TX_BLANK	FUNC_TEST=TRUE	46 64
TP_JTAG_WLAN_TCK	FUNC_TEST=TRUE	46 64
JTAG_WLAN_TDI_OSCAR_A	FUNC_TEST=TRUE	46 64
JTAG_WLAN_TDO_OSCAR_B	FUNC_TEST=TRUE	46 64
TP_JTAG_WLAN_TRST_L	FUNC_TEST=TRUE	46 64
JTAG_WLAN_SEL	FUNC_TEST=TRUE	46
UART2_SOC2WLAN_TX_R	FUNC_TEST=TRUE	46 64
UART2_WLAN2SOC_TX_R	FUNC_TEST=TRUE	46 64
UART_BB2WLAN_LTE_COEX_R	FUNC_TEST=TRUE	46
UART_WLAN2BB_LTE_COEX_R	FUNC_TEST=TRUE	46
=PP3V3_S2R_WIFI_PA	FUNC_TEST=TRUE	46 62
HSIC1_SOC2WLAN_HOST_RDY_R	FUNC_TEST=TRUE	46 64
HSIC1_WLAN2SOC_DEVICE_RDY	FUNC_TEST=TRUE	5 46 64
HSIC1_WLAN2SOC_REMOTE_WAKE	FUNC_TEST=TRUE	5 46 64

FOR HSIC CHARACTERIZATION

PP9480 P4MM SM (PP) 1 HSIC1_WLAN_DATA PLACE_NEAR=U0600.A27:3MM 4 46 61 64

PP9481 P4MM SM (PP) 1 HSIC1_WLAN_STB PLACE_NEAR=U0600.B27:3MM 4 46 61 64

PP9482 P4MM SM (PP) 1 HSIC1_WLAN_DATA PLACE_NEAR=U5800.13:3MM 4 46 61 64

PP9483 P4MM SM (PP) 1 HSIC1_WLAN_STB PLACE_NEAR=U5800.14:3MM 4 46 61 64

PMU_GPIO_WLAN_REG_ON	FUNC_TEST=TRUE	46 57
PMU_GPIO_BT_REG_ON	FUNC_TEST=TRUE	46 57
GPIO_BT_WAKE	FUNC_TEST=TRUE	5 46

BASEBAND

BB_JTAG_TMS	FUNC_TEST=TRUE	5 25 28 64
BB_JTAG_TCK	FUNC_TEST=TRUE	5 25 28 64
BB_JTAG_TDI	FUNC_TEST=TRUE	5 25 28 64
BB_JTAG_TDO	FUNC_TEST=TRUE	5 25 28 64
BB_JTAG_TRST_L	FUNC_TEST=TRUE	5 25 28 64
USB_BB_DEBUG_P	FUNC_TEST=TRUE	25 28 64
USB_BB_DEBUG_N	FUNC_TEST=TRUE	25 28 64
DEBUG_RST_L	FUNC_TEST=TRUE	25 28 67
PMU_GPIO_BB_VBUS_DET	FUNC_TEST=TRUE	25 28 57 67

FOR HSIC CHARACTERIZATION

PP9485 P4MM SM (PP) 1 HSIC2_BB_DATA PLACE_NEAR=U0600.AJ35:3MM 4 25 28 61 64

PP9486 P4MM SM (PP) 1 HSIC2_BB_STB PLACE_NEAR=U0600.AJ36:3MM 4 25 28 61 64

PP9487 P4MM SM (PP) 1 HSIC2_BB_DATA PLACE_NEAR=U3400.C7:3MM 4 25 28 61 64

PP9488 P4MM SM (PP) 1 HSIC2_BB_STB PLACE_NEAR=U3400.B8:3MM 4 25 28 61 64

HIGH SPEED, NO TEST

DDR0_CA<0..9>	NO_TEST=TRUE	8 12 61 66
DDR0_CK_P	NO_TEST=TRUE	8 12 61 66
DDR0_CK_N	NO_TEST=TRUE	8 12 61 66
DDR0_CA<0..9>	NO_TEST=TRUE	8 12 61 66
DDR0_CKE<0..1>	NO_TEST=TRUE	8 12 61 66
DDR0_CSN<0..1>	NO_TEST=TRUE	8 12 66
DDR0_DM<0..3>	NO_TEST=TRUE	8 12 66
DDR0_DQ<0..31>	NO_TEST=TRUE	8 12 61 66
DDR0_DQS_P<0..3>	NO_TEST=TRUE	8 12 61 66
DDR0_DQS_N<0..3>	NO_TEST=TRUE	8 12 61 66
DDR1_CA<0..9>	NO_TEST=TRUE	8 12 61 66
DDR1_CK_P	NO_TEST=TRUE	8 12 61 66
DDR1_CK_N	NO_TEST=TRUE	8 12 61 66
DDR1_CA<0..9>	NO_TEST=TRUE	8 12 61 66
DDR1_CKE<0..1>	NO_TEST=TRUE	8 12 61 66
DDR1_CSN<0..1>	NO_TEST=TRUE	8 12 61 66
DDR1_DM<0..3>	NO_TEST=TRUE	8 12 66
DDR1_DQ<0..31>	NO_TEST=TRUE	8 12 66
DDR1_DQS_P<0..3>	NO_TEST=TRUE	8 12 66
DDR1_DQS_N<0..3>	NO_TEST=TRUE	8 12 66

MIPI0C_CAM_REAR_CLK_P	NO_TEST=TRUE	7 23 61 65
MIPI0C_CAM_REAR_CLK_N	NO_TEST=TRUE	7 23 61 65
MIPI0C_CAM_REAR_DATA_P<0..1>	NO_TEST=TRUE	7 23 61 65
MIPI0C_CAM_REAR_DATA_N<0..1>	NO_TEST=TRUE	7 23 61 65
MIPI0C_CAM_REAR_CLK_FILT_P	NO_TEST=TRUE	23 65
MIPI0C_CAM_REAR_CLK_FILT_N	NO_TEST=TRUE	23 65
MIPI0C_CAM_REAR_DATA_FILT_P<0..3>	NO_TEST=TRUE	23 65
MIPI0C_CAM_REAR_DATA_FILT_N<0..3>	NO_TEST=TRUE	23 65
MIPI1C_CAM_FRONT_CLK_P	NO_TEST=TRUE	7 22 61 65
MIPI1C_CAM_FRONT_CLK_N	NO_TEST=TRUE	7 22 61 65
MIPI1C_CAM_FRONT_DATA_P<0>	NO_TEST=TRUE	7 22 61 65
MIPI1C_CAM_FRONT_DATA_N<0>	NO_TEST=TRUE	7 22 61 65
MIPI1C_CAM_FRONT_CLK_FILT_P	NO_TEST=TRUE	22 65
MIPI1C_CAM_FRONT_CLK_FILT_N	NO_TEST=TRUE	22 65
MIPI1C_CAM_FRONT_DATA_FILT_P<0>	NO_TEST=TRUE	22 65
MIPI1C_CAM_FRONT_DATA_FILT_N<0>	NO_TEST=TRUE	22 65

EDP_DATA_P<0..3>	NO_TEST=TRUE	7 53 65
EDP_DATA_N<0..3>	NO_TEST=TRUE	7 53 65
EDP_DATA_EMI_P<0..3>	NO_TEST=TRUE	53 65
EDP_DATA_EMI_N<0..3>	NO_TEST=TRUE	53 65
EDP_DATA_EMI_CONN_P<0..3>	NO_TEST=TRUE	53 65
EDP_DATA_EMI_CONN_N<0..3>	NO_TEST=TRUE	53 65

POWER, NO TEST

PP6V0_LCM_HI	NO_TEST=TRUE	56 67
SW_CHGA	NO_TEST=TRUE	55 67
WLED_LX_A	NO_TEST=TRUE	56 67
WLED_LX_B	NO_TEST=TRUE	56 67
L81_PVCP	NO_TEST=TRUE	15 65
L81_NVCP	NO_TEST=TRUE	15 65

CHARGE PUMP OUTPUTS

L81_FLYC	NO_TEST=TRUE	15 65
L81_FLYN	NO_TEST=TRUE	15 65
L81_FLYP	NO_TEST=TRUE	15 65

THROTTLER_OUT	NO_TEST=TRUE	58
UVLO_COMP_NEG	NO_TEST=TRUE	58
UVLO_COMP_POS	NO_TEST=TRUE	58
UVLO_COMP_REF	NO_TEST=TRUE	58
VCC_MAIN_UVLO_SENSE	NO_TEST=TRUE	58

NO TEST DUE TO LAYOUT

I2C3 TP AT ALS FILTER SIDE

I2C3_SCL_1V8	NO_TEST=TRUE	5 13 22 64
I2C3_SDA_1V8	NO_TEST=TRUE	5 13 22 64
MAX98304_L1_IN_N	NO_TEST=TRUE	18 65
MAX98304_L1_IN_P	NO_TEST=TRUE	18 65
MAX98304_R1_IN_N	NO_TEST=TRUE	17 65
MAX98304_R1_IN_P	NO_TEST=TRUE	17 65
MAX98304_L2_IN_N	NO_TEST=TRUE	18 65
MAX98304_L2_IN_P	NO_TEST=TRUE	18 65
MAX98304_R2_IN_N	NO_TEST=TRUE	17 65
MAX98304_R2_IN_P	NO_TEST=TRUE	17 65
GPIO_BTN_HOME_CONN_R_L	NO_TEST=TRUE	50

NO TEST ON PROX

PROX_AD7149_CIN5	NO_TEST=TRUE	45
PROX_AD7149_CIN7	NO_TEST=TRUE	45
PROX_AD7149_CIN9	NO_TEST=TRUE	45
PROX_AD7149_CIN7_FILT	NO_TEST=TRUE	45
PROX_AD7149_CIN9_FILT	NO_TEST=TRUE	45
PROX_AD7149_CIN7_CONN	NO_TEST=TRUE	45
PROX_AD7149_CIN9_CONN	NO_TEST=TRUE	45
PROX_AD7149_ACSHIELD_CONN	NO_TEST=TRUE	45
PROX_AD7149_BIAS	NO_TEST=TRUE	45
ACSHIELD_SB	NO_TEST=TRUE	45
ACSH_SB	NO_TEST=TRUE	45
PROX_AD7149_GPIO	NO_TEST=TRUE	45

POWER CONNECTIONS

BUCK0

67 60 55 PPVDD_CPU (MAKE_BASE=TRUE) = =PPVDD_CPU 11

BUCK1

67 60 55 PPVDD_GPU (MAKE_BASE=TRUE) = =PPVDD_GPU 11

BUCK2

67 60 55 PPVDD_SOC (MAKE_BASE=TRUE) = =PPVDD_SOC 10

BUCK3

67 60 56 55 PP1V8_S2R (MAKE_BASE=TRUE)
- = =PP1V8_S2R_MISC 5 59
- = =PP1V8_S2R_VDDIO_WLAN_BT 46
- = =PP1V8_S2R_TRISTAR 47
- = =PP1V8_S2R_DDR 12
- = =PP1V8_S2R_GRAPE 51
- = =PP1V8_S2R_EXT_SWITCH 57

BUCK3_SW

67 60 59 57 55 PP1V8_SW1 (MAKE_BASE=TRUE) = =PP1V8_AUDIO 15

XWC130 SM 1 — 2 PP1V8_SW1_FOREHEAD 60 62 67

67 62 60 PP1V8_SW1_FOREHEAD (MAKE_BASE=TRUE)
- = =PP1V8_DMIC 16
- = =PP1V8_CAM_FRONT 22
- = =PP1V8_CAM_REAR 23
- = =PP1V8_PROX_AD7149 45

67 60 57 PP1V8_EXT_SW (MAKE_BASE=TRUE)
- = =PP1V8_VDDIO18_SOC 9 10
- = =PP1V8_SOC 4 5 7 13 58
- = =PP1V8_MIPI_SOC 7
- = =PP1V8_EDP_SOC 7
- = =PP1V8_NAND_SOC 6
- = =PP1V8_NAND 14 57 61
- = =PP1V8_PLL_SOC 4
- = =PP1V8_EEPROM 5

67 60 55 PP1V8_SW2 (MAKE_BASE=TRUE) = =PP1V8_GRAPE 51

67 60 55 PP1V8_S2R_SW3 (MAKE_BASE=TRUE)
- = =PP1V8_S2R_GYRO 19
- = =PP1V8_S2R_ACCEL 19
- = =PP1V8_S2R_OSCAR 19

XWC133 SM 1 — 2 PP1V8_S2R_SW3_COMP 60 62 67

67 62 60 PP1V8_S2R_SW3_COMP (MAKE_BASE=TRUE) = =PP1V8_S2R_COMP 24

BUCK4

67 60 56 55 PP1V2_S2R (MAKE_BASE=TRUE)
- = =PP1V2_S2R_DDR 12
- = =PP1V2_S2R_DDR_SOC 8

BUCK4_SW

67 60 55 PP1V2_SW1 (MAKE_BASE=TRUE)
- = =PP1V2_VDDQ_DDR 12
- = =PP1V2_VDDIOD_SOC 8 9
- = =PP1V2_HSIC_SOC 4

67 60 55 PP1V2_S2R_SW2 (MAKE_BASE=TRUE) = =PP1V2_S2R_OSCAR 19

BUCK5

67 60 55 PPVDD_SRAM (MAKE_BASE=TRUE)
- = =PPVDD_SRAM_CPU 10
- = =PPVDD_SRAM_SOC 10

BUCK6

67 60 55 PP3V3_S2R (MAKE_BASE=TRUE)
- = =PP3V3_S2R_SWITCH 57
- = =PP3V3_S2R_WIFI_PA 46 61

67 60 57 PP3V3_SW (MAKE_BASE=TRUE)
- = =PP3V3_EDP_PU
- = =PP3V3_NAND 14
- = =PP3V3_USB_SOC 4

LDO1

67 60 56 PP3V0_SPARE1 (MAKE_BASE=TRUE) = =PP3V0_SPARE1 58

LDO2

67 60 56 PP1V7_VA_VCP (MAKE_BASE=TRUE) = =PP1V7_VA_VCP 15

LDO3

67 60 56 PP3V0_S2R_SENSOR (MAKE_BASE=TRUE)
- = =PP3V0_S2R_GYRO 19
- = =PP3V0_S2R_ACCEL 19
- = =PP3V0_S2R_COMP 24

LDO4

67 60 56 PP3V0_ALS (MAKE_BASE=TRUE)
- = =PP3V0_ALS 22
- = =PP3V0_PROX_AD7149 45

LDO5

67 60 56 PP3V0_UVLO (MAKE_BASE=TRUE) = =PP3V0_UVLO 58

LDO6

67 60 56 PP3V3_ACC (MAKE_BASE=TRUE) = =PP3V3_ACC 47

LDO7

67 60 56 PP3V0_S2R_TRISTAR (MAKE_BASE=TRUE) = =PP3V0_S2R_TRISTAR 47

LDO8

67 60 56 PP3V0_S2R_HALL (MAKE_BASE=TRUE) = =PP3V0_S2R_HALL 50

LDO9

BACKUP RAIL. CAN BE BOOSTED TO MEET 1.1V MIN ON CAMERA IF NEEDED.

67 60 56 PP1V3_CAM (MAKE_BASE=TRUE) = =PP1V3_CAM_REAR 23

LDO10

67 60 56 PP1V0_SOC (MAKE_BASE=TRUE)
- = =PP1V0_USB_SOC 4
- = =PP1V0_MIPI_SOC 7
- = =PP1V0_EDP_PAD_DVDD_SOC 7

LDO11

67 60 56 PP2V6_CAM_AF (MAKE_BASE=TRUE) = =PP2V6_CAM_REAR_AF 23

LDO13

67 60 56 PP2V9_CAM (MAKE_BASE=TRUE)
- = =PP2V9_CAM_FRONT 22
- = =PP2V9_CAM_REAR 23

VLCM1

67 60 56 PP5V25_GRAPE (MAKE_BASE=TRUE) = =PP5V25_GRAPE 52 61

CHARGER MAIN

67 60 58 57 56 55 47 PPVCC_MAIN (MAKE_BASE=TRUE)
- = =PPVCC_MAIN_AUDIO 15
- = =PPVCC_MAIN_LED 56
- = =PPVCC_MAIN_CPU 55
- = =PPVCC_MAIN_GPU 55
- = =PPVCC_MAIN_SOC 55
- = =PPVCC_MAIN_GRAPE 51
- = =PPVCC_MAIN_LCD 53
- = =PPVCC_MAIN_VDD_LCM 56
- = =PPVCC_MAIN_WLAN 46

BATTERY

67 60 55 PPBATT_VCC (MAKE_BASE=TRUE)
- = =PPBATT_POS_CONN 54
- = =PPBATT_VCC_BB 25 26 34 35 36 37 38 39 40
- = =PPBATT_AUDIO 17 18

USB POWER INPUT

67 60 55 PPVBUS_USB_DCIN (MAKE_BASE=TRUE) = =PPVBUS_USB_EMI 48

ON_BUF

67 60 56 PP1V8_ALWAYS (MAKE_BASE=TRUE) = =PP1V8_ALWAYS 5

BACKLIGHT BOOST

67 60 56 PPLED_OUT_A (MAKE_BASE=TRUE) = =PPLED_REG_A 53

67 60 56 PPLED_OUT_B (MAKE_BASE=TRUE) = =PPLED_REG_B 53

MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,BOTTOM	NO_TYPE,BGA	MM	16.5

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	0.105 MM	0.105 MM	0 MM	0 MM	0 MM
DEFAULT	ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9	Y	0.053 MM	0.053 MM	0 MM	0 MM	0 MM

45 OHM SINGLE-ENDED PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM	0 MM		
45_OHM_SE	ISL5	Y	0.055 MM	0.055 MM	0 MM		
45_OHM_SE	ISL7	Y	0.058 MM	0.058 MM	0 MM		
45_OHM_SE	ISL9	Y	0.052 MM	0.052 MM	0 MM		
45_OHM_SE	*	N	0.110 MM	0.110 MM	0 MM		

90 OHM DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.081 MM	0.081 MM	0 MM	0.100 MM	0.100 MM
90_OHM_DIFF	ISL5	Y	0.052 MM	0.052 MM	0 MM	0.130 MM	0.130 MM
90_OHM_DIFF	ISL7	Y	0.052 MM	0.052 MM	0 MM	0.110 MM	0.110 MM
90_OHM_DIFF	ISL9	Y	0.049 MM	0.049 MM	0 MM	0.150 MM	0.150 MM
90_OHM_DIFF	*	N	0.081 MM	0.081 MM	0 MM	0.100 MM	0.100 MM

50 OHM RF SINGLE-ENDED PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
50_OHM_RF	TOP	Y	0.240 MM	0.089 MM	40 MM			(NOTE: TOP LAYER REF L3, CLEAR L2, NECK REF ADJACENT)
50_OHM_RF	ISL3	Y	0.062 MM	0.062 MM	0 MM			(NOTE: L3 LAYER REF L1 AND L4, CLEAR L2)
50_OHM_RF	ISL4	Y	0.065 MM	0.046 MM	40 MM			(NOTE: L4 LAYER REF L2 AND L5, CLEAR L3, NECK REF ADJACENT)
50_OHM_RF	ISL7	Y	0.065 MM	0.046 MM	40 MM			(NOTE: L7 LAYER REF L5 AND L8, CLEAR L6, NECK REF ADJACENT)
50_OHM_RF	BOTTOM	Y	0.240 MM	0.089 MM	0 MM			(NOTE: BOT LAYER REF L8, CLEAR L9, NECK REF ADJACENT)
50_OHM_RF	*	N	0.240 MM	0.240 MM	0 MM			

100 OHM RF DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
100_OHM_RF	TOP	Y	0.072 MM	0.072 MM	0 MM	0.140 MM	0.140 MM	(NOTE: REF ADJACENT)
100_OHM_RF	ISL4	Y	0.056 MM	0.044 MM	20 MM	0.130 MM	0.160 MM	(NOTE: L4 LAYER REF L3 AND L6, CLEAR L5, NECK REF ADJACENT)
100_OHM_RF	ISL7	Y	0.056 MM	0.044 MM	20 MM	0.130 MM	0.160 MM	(NOTE: L7 LAYER REF L5 AND L8, CLEAR L6, NECK REF ADJACENT)
100_OHM_RF	*	N	0.072 MM	0.072 MM	0 MM	0.140 MM	0.140 MM	

DRAM SINGLE-ENDED PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
DRAM_SE	ISL5,ISL7,ISL9	Y	0.050 MM	0.050 MM	0 MM			(NOTE: L5 46 OHMS. L7 48 OHMS, L9 45 OHMS)
DRAM_SE	*	N	0.050 MM	0.050 MM	0 MM			

DRAM DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
DRAM_DIFF	ISL5,ISL7,ISL9	Y	0.051 MM	0.051 MM	0 MM	0.100 MM	0.100 MM	(NOTE: L5 89 OHMS. L7 91 OHMS, L9 86 OHMS)
DRAM_DIFF	*	N	0.051 MM	0.051 MM	0 MM	0.100 MM	0.100 MM	

GRAPE PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GRAPE_SE	TOP,BOTTOM	Y	0.1 MM	0.06 MM	5 MM	0 MM	0 MM
GRAPE_SE	ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9	Y	0.1 MM	0.06 MM	5 MM	0 MM	0 MM

TCF VERSION (USING SPACING RULE)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TCF_VERSION	*	0.020 MM	?

0.020 - 12/17/2012

TCF_VERSION — NC_USB_ID — ASSIGNING RULE TO NC NET

SPACING CONSTRAINTS

DEFAULT SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.2:1_SPACING	*	0.060 MM	?
1.5:1_SPACING	*	0.075 MM	?
2:1_SPACING	*	0.100 MM	?
2.4:1_SPACING	*	0.120 MM	?
3:1_SPACING	*	0.150 MM	?
4:1_SPACING	*	0.200 MM	?
5:1_SPACING	*	0.250 MM	?

POWER/GND SPACING RULES

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	1.5:1_SPACING
PWR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND
PP_PWR	*	PWR_PMU

POWER

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND	*	Y	0.2MM	0.06 MM	10.0 MM		
PWR_0P1MM	*	Y	0.10MM	0.10 MM	3.0 MM		
PWR_0P2MM	*	Y	0.2MM	0.15 MM	3.0 MM		
PWR_0P25MM	*	Y	0.25MM	0.15 MM	3.0 MM		
PWR_0P3MM	*	Y	0.3MM	0.20 MM	3.0 MM		
PWR_0P4MM	*	Y	0.4MM	0.20 MM	3.0 MM		
PWR_0P5MM	*	Y	0.5MM	0.20 MM	3.0 MM		
PWR_PMU	*	Y	0.6MM	0.20 MM	3.0 MM		
PWR_0P75MM	*	Y	0.75MM	0.20 MM	3.0 MM		
PWR_1MM	*	Y	1.0MM	0.20 MM	3.0 MM		
PWR_1P2MM	*	Y	1.2MM	0.20 MM	3.0 MM		
PWR_2MM	*	Y	2.0MM	0.20 MM	3.0 MM		
PWR_10MM	*	Y	10.0MM	0.20 MM	3.0 MM		
PWR_15MM	*	Y	15.0MM	0.20 MM	3.0 MM		
PWR_RF	*	Y	0.2MM	0.1 MM	3.0 MM		

MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPEAKER	*	Y	0.3 MM	0.06 MM	15 MM	0.10 MM	0.10 MM
AUDIO_DIFF	*	Y	0.1 MM	0.09 MM	3 MM	0.10 MM	0.10 MM
LED	*	Y	0.1 MM	0.09 MM	3 MM	0.08 MM	0.08 MM
TEMP_SENSE	*	Y	0.1 MM	0.06 MM	35 MM	0.08 MM	0.08 MM
PWR_SENSE	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM
RF_DIFF	*	Y	0.06 MM	0.06 MM	3 MM	0.06 MM	0.06 MM

MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	3:1_SPACING
ANLG	*	*	3:1_SPACING

MAX_LINE_WIDTH=1 MM

0V — GND — GND — GND

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
B6	CLK_50S	CLK	CLK_32K_SOC2CUMULUS 5 52 60 61
B5	CLK_50S	CLK	CLK_32K_SOC2CUMULUS_FILT 60
B4	CLK_50S	CLK	CUMULUS_MS_CK 52 61
B3	CLK_50S	CLK	CUMULUS_MS_SD 52 61
B1	CLK_50S	CLK	PMU_GPIO_CLK_32K_WLAN 46 57
A1	CLK_50S	CLK	PMU_GPIO_CLK_32K_OSCAR 19 57 60
A2	CLK_50S	CLK	PMU_OUT_32K_CLK_GPS 57 68
B8	CLK_50S	CLK	ISP1_CAM_FRONT_CLK_R 7
B7	CLK_50S	CLK	ISP1_CAM_FRONT_CLK 7 22
B6	CLK_50S	CLK	ISP1_CAM_FRONT_CLK_F 22 60
A8	CLK_50S	CLK	ISP0_CAM_REAR_CLK_R 7
A7	CLK_50S	CLK	ISP0_CAM_REAR_CLK 7 23
A6	CLK_50S	CLK	ISP0_CAM_REAR_CLK_F 23 60

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	3:1_SPACING
UART	UART	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
D10	UART_50S	UART	UART0_SOC_RXD 5 47 60
D9	UART_50S	UART	UART0_SOC_TXD 5 47 60
D11	UART_50S	UART	UART3_SOC2BB_RTS_L 5 25 29
D12	UART_50S	UART	UART3_BB2SOC_RTS_L 5 25 29
D13	UART_50S	UART	UART3_SOC2BB_TX 5 25 29 47
D14	UART_50S	UART	UART3_BB2SOC_TX 5 25 29 47
D15	UART_50S	UART	UART4_OSCAR2SOC_RXD 5 19
D16	UART_50S	UART	UART4_SOC2OSCAR_TXD 5 19
E13	UART_50S	UART	UART1_SOC2BT_RTS_L 5 46
E14	UART_50S	UART	UART1_BT2SOC_RTS_L 5 46
E15	UART_50S	UART	UART1_SOC2BT_TX 5 46
E16	UART_50S	UART	UART1_BT2SOC_TX 5 46
E11	UART_50S	UART	UART2_SOC2WLAN_TX 5 46
E12	UART_50S	UART	UART2_WLAN2SOC_TX 5 46
D17	UART_50S	UART	UART2_SOC2WLAN_TX_R 46 61
D18	UART_50S	UART	UART2_WLAN2SOC_TX_R 46 61
E10	UART_50S	UART	UART6_TS_ACC_RXD 5 47
E9	UART_50S	UART	UART6_TS_ACC_TXD 5 47
D19		UART	UART5_BATT_TRXD 5 54 57
D20		UART	BATT_SWI_CONN 54 60

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
B17	I2S_50S	CLK	I2S0_CODEC_ASP_MCK_R 5 15
B18	I2S_50S	CLK	I2S0_CODEC_ASP_MCK 5
B16	I2S_50S	I2S	I2S0_CODEC_ASP_BCLK 5 15
B13	I2S_50S	I2S	I2S0_CODEC_ASP_LRCK 5 15
B12	I2S_50S	I2S	I2S0_CODEC_ASP_DIN 5 15
B11	I2S_50S	I2S	I2S0_CODEC_ASP_DOUT 5 15
B10	I2S_50S	I2S	I2S0_CODEC_ASP_SDOUT 15
B15	I2S_50S	I2S	NC_I2S1_MCK 5
B14	I2S_50S	I2S	I2S1_CODEC_XSP_BCLK 5 15
B19	I2S_50S	I2S	I2S1_CODEC_XSP_LRCK 5 15
B20	I2S_50S	I2S	I2S1_CODEC_XSP_DIN 5 15
B21	I2S_50S	I2S	I2S1_CODEC_XSP_DOUT 5 15
B9	I2S_50S	I2S	I2S1_CODEC_XSP_SDOUT 15
A24	I2S_50S	CLK	NC_I2S2_MCK_R
A25	I2S_50S	CLK	NC_I2S2_MCK 5
A24	I2S_50S	I2S	NC_I2S2_BCLK 5
A23	I2S_50S	I2S	NC_I2S2_LRCK 5
A22	I2S_50S	I2S	NC_I2S2_DIN 5
A21	I2S_50S	I2S	NC_I2S2_DOUT 5
F25	I2S_50S	I2S	NC_I2S4_MCK 5
F24	I2S_50S	I2S	I2S4_SOC2BT_BCLK 5 46
F23	I2S_50S	I2S	I2S4_SOC2BT_LRCK 5 46
F22	I2S_50S	I2S	I2S4_SOC2BT_DATA 5 46
F21	I2S_50S	I2S	I2S4_BT2SOC_DATA 5 46

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
B22		DWI	DWI_AP_CLK 5 57
B24		DWI	NC_DWI_AP_DI 57
B26		DWI	DWI_AP_DO 5 57

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
A5	I2C_50S	I2C	I2C0_SDA_1V8 5 57 60
A4	I2C_50S	I2C	I2C0_SCL_1V8 5 57 60
A3	I2C_50S	I2C	I2C3_CAM_ALS_SDA_1V8_F 22 60
A2	I2C_50S	I2C	I2C3_CAM_ALS_SCL_1V8_F 22 60
B5	I2C_50S	I2C	I2C0_HP_ALS_SDA_1V8_FILT 60
B4	I2C_50S	I2C	I2C0_HP_ALS_SCL_1V8_FILT 60
B25	I2C_50S	I2C	I2C1_SOC2OSCAR_SWDCLK_1V8 5 19
B24	I2C_50S	I2C	I2C1_SOC2OSCAR_SWDIO_1V8 5 19
B3	I2C_50S	I2C	I2C2_SDA_1V8 5 47
B2	I2C_50S	I2C	I2C2_SCL_1V8 5 47
B23	I2C_50S	I2C	I2C3_SDA_1V8 5 13 22 61
B22	I2C_50S	I2C	I2C3_SCL_1V8 5 13 22 61
D25	I2C_50S	I2C	DMIC1_FF_SD_FILT 16 60
D24	I2C_50S	I2C	DMIC1_FF_SCLK_FILT 16 60
D23	I2C_50S	I2C	DMIC1_FF_SD 15 16
D22	I2C_50S	I2C	DMIC1_FF_SCLK 15 16
D21	I2C_50S	I2C	SEP_I2C0_SCL 5
D20	I2C_50S	I2C	SEP_I2C0_SDA 5
A8	I2C_50S	I2C	ISP0_CAM_REAR_SCL 7 23
A9	I2C_50S	I2C	ISP0_CAM_REAR_SDA 7 23
A10	I2C_50S	I2C	ISP0_CAM_REAR_SCL_F 23 60
A11	I2C_50S	I2C	ISP0_CAM_REAR_SDA_F 23 60
B8	I2C_50S	I2C	ISP1_CAM_FRONT_SCL 7 22
B9	I2C_50S	I2C	ISP1_CAM_FRONT_SDA 7 22
B10	I2C_50S	I2C	ISP1_CAM_FRONT_SCL_F 22 60
B11	I2C_50S	I2C	ISP1_CAM_FRONT_SDA_F 22 60

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
B26	SPI_50S	SPI	SPI3_CODEC_MISO 5 15
B27	SPI_50S	SPI	SPI3_CODEC_MOSI 5 15
B28	SPI_50S	SPI	SPI3_CODEC_SCLK 5 15
B29	SPI_50S	SPI	SPI3_CODEC_CS_L 5 15
B31	SPI_50S	SPI	SPI2_GRAPE_MISO 5 52 60 61 64
B30	SPI_50S	SPI	SPI2_GRAPE_MOSI 5 52 60 61 64
B32	SPI_50S	SPI	SPI2_GRAPE_SCLK 5 52 60 61 64
A26	SPI_50S	SPI	SPI2_GRAPE_CS_L 5 52 60 61 64
B31	SPI_50S	SPI	SPI2_GRAPE_MISO 5 52 60 61 64
B30	SPI_50S	SPI	SPI2_GRAPE_MOSI 5 52 60 61 64
B32	SPI_50S	SPI	SPI2_GRAPE_SCLK 5 52 60 61 64
A26	SPI_50S	SPI	SPI2_GRAPE_CS_L 5 52 60 61 64
B31	SPI_50S	SPI	SPI_OSCAR_MISO 19 24
B30	SPI_50S	SPI	SPI_OSCAR_MOSI 19 24
B32	SPI_50S	SPI	SPI_OSCAR_SCLK 19 24
B33	SPI_50S	SPI	SPI_OSCAR_MISO_GYRO 19
B34	SPI_50S	SPI	SPI_OSCAR_MISO_ACCEL 19
A27	SPI_50S	SPI	SPI_OSCAR_MISO_COMP1 24
B30	SPI_50S	SPI	SPI_OSCAR_MOSI_R 19
B32	SPI_50S	SPI	SPI_OSCAR_SCLK_R 19
B35	SPI_50S	SPI	SPI_OSCAR2ACCEL_CS_L 19
B36	SPI_50S	SPI	SPI_OSCAR2GYRO_CS_L 19
A28	SPI_50S		SPI_OSCAR2COMPASS_CS_L 19 24

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E1		JTAG	JTAG_SOC_TCK 4 47 60
E2		JTAG	JTAG_SOC_TMS 4 47 60
E3		JTAG	JTAG_SOC_TDI 4 60
E4		JTAG	TP_JTAG_SOC_TDO 4 60
E5		RST	JTAG_SOC_TRST_L 4 13 60
E6		JTAG	NC_JTAG_SOC_TRTCK 4
D1		JTAG	BB_JTAG_TMS 5 25 28 61
D2		JTAG	BB_JTAG_TCK 5 25 28 61
D3		JTAG	BB_JTAG_TDO 5 25 28 61
D4		JTAG	BB_JTAG_TDI 5 25 28 61
D5		RST	BB_JTAG_TRST_L 5 25 28 61
D6		JTAG	JTAG_WLAN_TMS_TX_BLANK 46 61
C1		JTAG	TP_JTAG_WLAN_TCK 46 61
C2		JTAG	JTAG_WLAN_TDO_OSCAR_B 46 61
C3		JTAG	JTAG_WLAN_TDI_OSCAR_A 46 61
C4		RST	TP_JTAG_WLAN_TRST_L 46 61
C5		JTAG	TP_JTAG_CUMULUS_M_TCK 52 61
C6		JTAG	TP_JTAG_CUMULUS_M_TDI 52 61
C7		JTAG	JTAG_CUMULUS_M_TMS 52 61
C8		JTAG	TP_JTAG_CUMULUS_M_TDO 52 61

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
A1	USB_90D	USB	USB_SOC_P 4 47 60
A2	USB_90D	USB	USB_SOC_N 4 47 60
B26	USB_90D	USB	USB_BB_P 25 47
B25	USB_90D	USB	USB_BB_N 25 47
B24	USB_90D	USB	USB_BB_DEBUG_P 25 28 61
B23	USB_90D	USB	USB_BB_DEBUG_N 25 28 61
F26	USB_90D	USB	E75_DPAIR1_CONN_P 47 49 60
F25	USB_90D	USB	E75_DPAIR1_CONN_N 47 49 60
F24	USB_90D	USB	E75_DPAIR2_CONN_P 47 49 60
F23	USB_90D	USB	E75_DPAIR2_CONN_N 47 49 60
F22	USB_90D	USB	E75_DPAIR1_P 47
F21	USB_90D	USB	E75_DPAIR1_N 47
F20	USB_90D	USB	E75_DPAIR2_P 47
F19	USB_90D	USB	E75_DPAIR2_N 47

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	4:1_SPACING
HSIC	GND	*	1.5:1_SPACING
HSIC_RDY	*	*	2:1_SPACING
HSIC_RDY	GND	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
F31	HSIC	HSIC	HSIC1_WLAN_DATA 4 46 61
F34	HSIC	HSIC	HSIC1_WLAN_STB 4 46 61
F33	HSIC	HSIC	HSIC2_BB_DATA 4 25 28 61
F32	HSIC	HSIC	HSIC2_BB_STB 4 25 28 61
F27	HSIC	HSIC	NC_HSIC0_DATA 4
F28	HSIC	HSIC	NC_HSIC0_STB 4
F35	HSIC	HSIC_RDY	HSIC1_WLAN2SOC_REMOTE_WAKE 5 46 61
F36	HSIC	HSIC_RDY	HSIC1_WLAN2SOC_DEVICE_RDY 5 46 61
F37	HSIC	HSIC_RDY	HSIC1_SOC2WLAN_HOST_RDY 5 46
F38	HSIC	HSIC_RDY	HSIC1_SOC2WLAN_HOST_RDY_R 46 61
F30	HSIC	HSIC_RDY	HSIC2_BB2SOC_REMOTE_WAKE 5 29
F29	HSIC	HSIC_RDY	HSIC2_BB2SOC_DEVICE_RDY 5 25 29
F26	HSIC	HSIC_RDY	HSIC2_SOC2BB_HOST_RDY 5 25 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI0C	*	*	4:1_SPACING
MIPI1C	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_CLK_P	7 23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_CLK_N	7 23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_P<0>	7 23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_N<0>	7 23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_P<1>	7 23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_N<1>	7 23 61
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_P<2>	7
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_N<2>	7
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_P<3>	7
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_N<3>	7
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_CLK_FILT_P	23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_CLK_FILT_N	23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_FILT_P<0>	23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_FILT_N<0>	23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_FILT_P<1>	23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_FILT_N<1>	23 61
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_FILT_P<2>	
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_FILT_N<2>	
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_FILT_P<3>	
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_FILT_N<3>	
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_CLK_P	7 22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_CLK_N	7 22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_DATA_P<0>	7 22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_DATA_N<0>	7 22 61
	MIPI_90D	MIPI1C	NC_MIPI1C_CAM_FRONT_DATA_P<1>	7
	MIPI_90D	MIPI1C	NC_MIPI1C_CAM_FRONT_DATA_N<1>	7
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_CLK_FILT_P	22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_CLK_FILT_N	22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_DATA_FILT_P<0>	22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_DATA_FILT_N<0>	22 61
	MIPI_90D	MIPI1C	NC_MIPI0D_DPCLK	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DNCLK	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DPDATA0	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DNDATA0	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DPDATA1	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DNDATA1	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DPDATA2	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DNDATA2	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DPDATA3	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DNDATA3	7
	MIPI_90D	MIPI0C	MIPI_CAM0_CLKCON_P	
	MIPI_90D	MIPI0C	MIPI_CAM0_CLKCON_N	
	MIPI_90D	MIPI0C	MIPI_CAM0_D0CON_P	
	MIPI_90D	MIPI0C	MIPI_CAM0_D0CON_N	
	MIPI_90D	MIPI0C	MIPI_CAM0_D1CON_P	
	MIPI_90D	MIPI0C	MIPI_CAM0_D1CON_N	
	MIPI_90D	MIPI0C	MIPI_CAM0_D2CON_P	
	MIPI_90D	MIPI0C	MIPI_CAM0_D2CON_N	
	MIPI_90D	MIPI0C	MIPI_CAM0_D3CON_P	
	MIPI_90D	MIPI0C	MIPI_CAM0_D3CON_N	
	MIPI_90D	MIPI1C	MIPI_CAM1_CLKCON_P	
	MIPI_90D	MIPI1C	MIPI_CAM1_CLKCON_N	
	MIPI_90D	MIPI1C	MIPI_CAM1_D0CON_P	
	MIPI_90D	MIPI1C	MIPI_CAM1_D0CON_N	
	MIPI_90D	MIPI1C	MIPI_CAM1_D1CON_P	
	MIPI_90D	MIPI1C	MIPI_CAM1_D1CON_N	

DEV

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LEDA	*	*	2.4:1_SPACING
LEDB	*	*	2.4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	LED	LEDA	LED_IO1_A_R	56
	LED	LEDB	LED_IO1_B_R	56
	LED	LEDA	LED_IO2_A_R	56
	LED	LEDB	LED_IO2_B_R	56
	LED	LEDA	LED_IO3_A_R	56
	LED	LEDB	LED_IO3_B_R	56
	LED	LEDA	LED_IO4_A_R	56
	LED	LEDB	LED_IO4_B_R	56
	LED	LEDA	LED_IO5_A_R	56
	LED	LEDB	LED_IO5_B_R	56
	LED	LEDA	LED_IO6_A_R	56
	LED	LEDB	LED_IO6_B_R	56
	LED	LEDA	LED_IO_1_A	53 56 60
	LED	LEDB	LED_IO_1_B	53 56 60
	LED	LEDA	LED_IO_2_A	53 56 60
	LED	LEDB	LED_IO_2_B	53 56 60
	LED	LEDA	LED_IO_3_A	53 56 60
	LED	LEDB	LED_IO_3_B	53 56 60
	LED	LEDA	LED_IO_4_A	53 56 60
	LED	LEDB	LED_IO_4_B	53 56 60
	LED	LEDA	LED_IO_5_A	53 56 60
	LED	LEDB	LED_IO_5_B	53 56 60
	LED	LEDA	LED_IO_6_A	53 56 60
	LED	LEDB	LED_IO_6_B	53 56 60

AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING
AUDIO	AUDIO	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_L1_OUT_P	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_L1_OUT_N	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_L2_OUT_P	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_L2_OUT_N	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_R1_OUT_P	17 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_R1_OUT_N	17 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_R2_OUT_P	17 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_R2_OUT_N	17 49 60
	USB_90D	USB	MIKEY_TS_P	15 47
	USB_90D	USB	MIKEY_TS_N	15 47
	USB_90D	USB	L81_MBUS_P	15
	USB_90D	USB	L81_MBUS_N	15
SPKR_DIFF	AUDIO_DIFF	AUDIO	LEFT_CH_OUT_P	15 18 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	LEFT_CH_OUT_N	15 18 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	RIGHT_CH_OUT_P	15 17 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	RIGHT_CH_OUT_N	15 17 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_L1_IN_P	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_L1_IN_N	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_R1_IN_P	17 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_R1_IN_N	17 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_L2_IN_P	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_L2_IN_N	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_R2_IN_P	17 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_R2_IN_N	17 61
	AUDIO_DIFF	AUDIO	SPKR_L1_VSNS_P	
	AUDIO_DIFF	AUDIO	SPKR_L1_VSNS_N	
	AUDIO_DIFF	AUDIO	SPKR_R1_VSNS_P	
	AUDIO_DIFF	AUDIO	SPKR_R1_VSNS_N	
	PWR_0P5MM	AUDIO	CODEC_HP_HS3	15
	PWR_0P5MM	AUDIO	CODEC_HP_HS4	15
	PWR_0P5MM	AUDIO	CONN_HP_HS3_FILT	15 16 60
	PWR_0P5MM	AUDIO	CONN_HP_HS4_FILT	15 16 60
	PWR_0P2MM	AUDIO	CODEC_HP_LEFT	15
	PWR_0P2MM	AUDIO	CODEC_HP_RIGHT	15
	PWR_0P2MM	AUDIO	CONN_HP_LEFT_FILT	15 16 60
	PWR_0P2MM	AUDIO	CONN_HP_RIGHT_FILT	15 16 60
	PP_PWR	PWR	L81_NVCP	15 61
	PP_PWR	PWR	L81_PVCP	15 61
	PP_PWR	PWR	L81_FLYP	15 61
	PP_PWR	PWR	L81_FLYN	15 61
	PP_PWR	PWR	L81_FLYC	15 61
	PP_PWR	PWR	SPEAKER_VQ	
	PP_PWR	PWR	L81_FILT	15
	PWR_0P1MM	AUDIO	HP_MIC_POS	15
	PWR_0P1MM	AUDIO	HP_MIC_NEG	15
	PWR_0P1MM	AUDIO	L81_AIN2_POS	15
	PWR_0P1MM	AUDIO	L81_AIN2_NEG	15
	PWR_0P1MM	AUDIO	CODEC_HP_HS3_REF	15
	PWR_0P1MM	AUDIO	CODEC_HP_HS4_REF	15
	PWR_0P1MM	AUDIO	CONN_HP_HS3_REF_FILT	15 16 60
	PWR_0P1MM	AUDIO	CONN_HP_HS4_REF_FILT	15 16 60

MAXIMUM NECK LENGTH=0.5 MM
MIN_NECK_WIDTH=0.06 MM

MAXIMUM NECK LENGTH=15 MM

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		CRYSTAL	XTAL_SOC_24M_I	4
		CRYSTAL	XTAL_SOC_24M_O	4
		CRYSTAL	SOC_24M_O	4
		CRYSTAL	PMU_XTAL	56
		CRYSTAL	PMU_EXTAL	56

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	EDP_90D	EDP	EDP_AUX_P	7 53
	EDP_90D	EDP	EDP_AUX_N	7 53
	EDP_50S	EDP	EDP_HPD	7 53
EDP	EDP_90D	EDP	EDP_DATA_P<0>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_N<0>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_P<1>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_N<1>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_P<2>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_N<2>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_P<3>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_N<3>	7 53 61
	EDP_90D	EDP	EDP_AUX_EMI_P	53
	EDP_90D	EDP	EDP_AUX_EMI_N	53
EDP	EDP_90D	EDP	EDP_DATA_EMI_P<0>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_N<0>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_P<1>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_N<1>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_P<2>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_N<2>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_P<3>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_N<3>	53 61
	EDP_90D	EDP	EDP_AUX_EMI_CONN_P	53
	EDP_90D	EDP	EDP_AUX_EMI_CONN_N	53
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_P<0>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_N<0>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_P<1>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_N<1>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_P<2>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_N<2>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_P<3>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_N<3>	53 61

TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
BOARD_TEMP	*	TEMP_SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BOARD_TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	BOARD_TEMP	BOARD_TEMP	PA_NTC_P	57 60
	BOARD_TEMP	BOARD_TEMP	PA_NTC_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP2_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP2_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_N	57

MIN_NECK_WIDTH=0.053 MM

GRAPE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GRAPE	*	GRAPE_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GRAPE	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	GRAPE	GRAPE	MT_PANEL_IN<0..29>	52 61
	GRAPE	GRAPE	MT_PANEL_OUT<0..39>	52 61

DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	DRAM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DRAM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I333	DDR_50S	DDR	DDR0_CA<0> 8 12 61
I221	DDR_50S	DDR	DDR0_CA<9..1> 8 12 61
I222	DDR_50S	DDR	DDR0_DM<3..0> 8 12 61
I223	DDR_90D	DDR	DDR0_CK_P 8 12 61
I225	DDR_90D	DDR	DDR0_CK_N 8 12 61
I226	DDR_50S	DDR	DDR0_CKE<1..0> 8 12 61
I224	DDR_50S	DDR	DDR0_CSN<1..0> 8 12 61
I329		DDR	DDR0_CA_ZQ_SOC 8
I327		DDR	DDR0_DQ_ZQ_SOC 8
I264		DDR	DDR0_ZQ_DRAM 12
I230	DDR_50S	DDR	DDR0_DQ<1..0> 8 12 61
I335	DDR_50S	DDR	DDR0_DQ<2> 8 12 61
I334	DDR_50S	DDR	DDR0_DQ<7..3> 8 12 61
I228	DDR_90D	DDR	DDR0_DQS_P<0> 8 12 61
I231	DDR_90D	DDR	DDR0_DQS_N<0> 8 12 61
I232	DDR_50S	DDR	DDR0_DQ<15..8> 8 12 61
I233	DDR_90D	DDR	DDR0_DQS_P<1> 8 12 61
I235	DDR_90D	DDR	DDR0_DQS_N<1> 8 12 61
I234	DDR_50S	DDR	DDR0_DQ<23..16> 8 12 61
I236	DDR_90D	DDR	DDR0_DQS_P<2> 8 12 61
I237	DDR_90D	DDR	DDR0_DQS_N<2> 8 12 61
I331	DDR_50S	DDR	DDR0_DQ<27..25> 8 12 61
I238	DDR_50S	DDR	DDR0_DQ<28> 8 12 61
I330	DDR_50S	DDR	DDR0_DQ<31..29> 8 12 61
I239	DDR_90D	DDR	DDR0_DQS_P<3> 8 12 61
I240	DDR_90D	DDR	DDR0_DQS_N<3> 8 12 61
I338	DDR_50S	DDR	DDR1_CA<3..0> 8 12 61
I201	DDR_50S	DDR	DDR1_CA<9..4> 8 12 61
I202	DDR_50S	DDR	DDR1_DM<3..0> 8 12 61
I207	DDR_90D	DDR	DDR1_CK_P 8 12 61
I205	DDR_90D	DDR	DDR1_CK_N 8 12 61
I206	DDR_50S	DDR	DDR1_CKE<1..0> 8 12 61
I204	DDR_50S	DDR	DDR1_CSN<0> 8 12 61
I339	DDR_50S	DDR	DDR1_CSN<1> 8 12 61
I330		DDR	DDR1_CA_ZQ_SOC 8
I331		DDR	DDR1_DQ_ZQ_SOC 8
I332		DDR	DDR1_ZQ_DRAM 12
I210	DDR_50S	DDR	DDR1_DQ<7..0> 8 12 61
I209	DDR_90D	DDR	DDR1_DQS_P<0> 8 12 61
I211	DDR_90D	DDR	DDR1_DQS_N<0> 8 12 61
I212	DDR_50S	DDR	DDR1_DQ<15..8> 8 12 61
I213	DDR_90D	DDR	DDR1_DQS_P<1> 8 12 61
I215	DDR_90D	DDR	DDR1_DQS_N<1> 8 12 61
I214	DDR_50S	DDR	DDR1_DQ<23..16> 8 12 61
I216	DDR_90D	DDR	DDR1_DQS_P<2> 8 12 61
I217	DDR_90D	DDR	DDR1_DQS_N<2> 8 12 61
I218	DDR_50S	DDR	DDR1_DQ<31..24> 8 12 61
I219	DDR_90D	DDR	DDR1_DQS_P<3> 8 12 61
I220	DDR_90D	DDR	DDR1_DQS_N<3> 8 12 61

VREF (DDR/FMI)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	MIN_NECK_WIDTH=0.15 MM		
I199 0.6V	PP_PWR	PWR	PPVREF_DDR0_CA_SOC 8
I198 0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ_SOC 8
I196 0.6V	PP_PWR	PWR	PPVREF_DDR1_CA_SOC 8
I197 0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ_SOC 8
I194 0.6V	PP_PWR	PWR	PPVREF_DDR0_CA_DRAM 12
I193 0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ_DRAM 12
I195 0.6V	PP_PWR	PWR	PPVREF_DDR1_CA_DRAM 12
I192 0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ_DRAM 12
I191 0.9V	PP_PWR	VREF	PPVREF_FMI_SOC 6 61
I190 0.9V	PP_PWR	VREF	PPVREF_FMI_NAND 14 61

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I48	FMI0_AD_CTRL_PP	NAND_50S	NAND FMI0_AD<0> 6 14 61
I49	FMI0_AD_CTRL	NAND_50S	NAND FMI0_AD<1> 6 14 61
I50	FMI0_AD_CTRL	NAND_50S	NAND FMI0_AD<2> 6 14 61
I51	FMI0_AD_CTRL	NAND_50S	NAND FMI0_AD<3> 6 14 61
I52	FMI0_AD_CTRL	NAND_50S	NAND FMI0_AD<4> 6 14 61
I53	FMI0_AD_CTRL	NAND_50S	NAND FMI0_AD<5> 6 14 61
I54	FMI0_AD_CTRL	NAND_50S	NAND FMI0_AD<6> 6 14 61
I55	FMI0_AD_CTRL	NAND_50S	NAND FMI0_AD<7> 6 14 61
I56	FMI0_AD_CTRL	NAND_50S	NAND FMI0_ALE 6 14 61
I57	FMI0_CE	NAND_50S	NAND FMI0_CE0_L 6 14 60 61
I58	FMI0_AD_CTRL	NAND_50S	NAND FMI0_CLE 6 14 61
I59		NAND_50S	NAND FMI0_DQS 6 14 61
I60	FMI0_AD_CTRL	NAND_50S	NAND FMI0_RE_L 6 14 61
I61	FMI0_AD_CTRL	NAND_50S	NAND FMI0_WE_L 6 14 61
I335	FMI1_AD_CTRL	NAND_50S	NAND FMI1_AD<0> 6 14 61
I136	FMI1_AD_CTRL	NAND_50S	NAND FMI1_AD<1> 6 14
I137	FMI1_AD_CTRL	NAND_50S	NAND FMI1_AD<2> 6 14
I138	FMI1_AD_CTRL	NAND_50S	NAND FMI1_AD<3> 6 14
I139	FMI1_AD_CTRL	NAND_50S	NAND FMI1_AD<4> 6 14
I140	FMI1_AD_CTRL	NAND_50S	NAND FMI1_AD<5> 6 14
I141	FMI1_AD_CTRL	NAND_50S	NAND FMI1_AD<6> 6 14
I142	FMI1_AD_CTRL	NAND_50S	NAND FMI1_AD<7> 6 14
I143	FMI1_AD_CTRL	NAND_50S	NAND FMI1_ALE 6 14 61
I144	FMI1_CE	NAND_50S	NAND FMI1_CE0_L 6 14 61
I152	FMI1_AD_CTRL	NAND_50S	NAND FMI1_CLE 6 14 61
I154	FMI1_AD_CTRL	NAND_50S	NAND FMI1_DQS 6 14 61
I156	FMI1_AD_CTRL	NAND_50S	NAND FMI1_RE_L 6 14 61
I165	FMI1_AD_CTRL	NAND_50S	NAND FMI1_WE_L 6 14 61

NAND DEV

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I985	NAND_50S	NAND	FMI0_AD_BUF<0>
I987	NAND_50S	NAND	FMI0_AD_BUF<1>
I986	NAND_50S	NAND	FMI0_AD_BUF<2>
I988	NAND_50S	NAND	FMI0_AD_BUF<3>
I989	NAND_50S	NAND	FMI0_AD_BUF<4>
I990	NAND_50S	NAND	FMI0_AD_BUF<5>
I992	NAND_50S	NAND	FMI0_AD_BUF<6>
I994	NAND_50S	NAND	FMI0_AD_BUF<7>
I993	NAND_50S	NAND	FMI0_ALE_BUF
I995	NAND_50S	NAND	FMI0_CE0_BUF_L
I996	NAND_50S	NAND	FMI0_CLE_BUF
I998	NAND_50S	NAND	FMI0_DQS_BUF
I997	NAND_50S	NAND	FMI0_DQSN_BUF
I999	NAND_50S	NAND	FMI0_REP_BUF
I998	NAND_50S	NAND	FMI0_RE_BUF_L
I910	NAND_50S	NAND	FMI0_WE_BUF_L
I111	NAND_50S	NAND	FMI1_AD_BUF<0>
I112	NAND_50S	NAND	FMI1_AD_BUF<1>
I114	NAND_50S	NAND	FMI1_AD_BUF<2>
I113	NAND_50S	NAND	FMI1_AD_BUF<3>
I115	NAND_50S	NAND	FMI1_AD_BUF<4>
I116	NAND_50S	NAND	FMI1_AD_BUF<5>
I117	NAND_50S	NAND	FMI1_AD_BUF<6>
I118	NAND_50S	NAND	FMI1_AD_BUF<7>
I119	NAND_50S	NAND	FMI1_ALE_BUF
I120	NAND_50S	NAND	FMI1_CE0_BUF_L
I122	NAND_50S	NAND	FMI1_CLE_BUF
I123	NAND_50S	NAND	FMI1_DQS_BUF
I121	NAND_50S	NAND	FMI1_DQSN_BUF
I124	NAND_50S	NAND	FMI1_REP_BUF
I125	NAND_50S	NAND	FMI1_RE_BUF_L
I126	NAND_50S	NAND	FMI1_WE_BUF_L

PWR

	VOLTAGE	NET_TYPE PHYSICAL	SPACING	
BUCKS				
J22	4.7V	PP_PWR	PWR	BUCK0_LX0 55
J1	4.7V	PP_PWR	PWR	BUCK0_LX1 55
J2	4.7V	PP_PWR	PWR	BUCK0_LX2 55
J3	4.7V	PP_PWR	PWR	BUCK0_LX3 55
J4	1.1V	PP_PWR	PWR	BUCK0_FB 55
J5	4.7V	PP_PWR	PWR	BUCK1_LX0 55
J6	4.7V	PP_PWR	PWR	BUCK1_LX1 55
J7	4.7V	PP_PWR	PWR	BUCK1_LX2 55
J8	1.1V	PP_PWR	PWR	BUCK1_FB 55
J9	4.7V	PP_PWR	PWR	BUCK2_LX0 55
J12	1.0V	PP_PWR	PWR	BUCK2_FB 55
J13	4.7V	PP_PWR	PWR	BUCK3_LX0 55
J10	1.8V	PP_PWR	PWR	BUCK3_FB 55
J15	4.7V	PP_PWR	PWR	BUCK4_LX0 55
J15	1.2V	PP_PWR	PWR	BUCK4_FB 55
J14	4.7V	PP_PWR	PWR	BUCK5_LX0 55
J16	1.0V	PP_PWR	PWR	BUCK5_FB 55
J17	4.7V	PP_PWR	PWR	BUCK6_LX0 55
J19	3.3V	PP_PWR	PWR	BUCK6_FB 55
RAILS				
J268	1.1V	MIN_NECK_WIDTH=0.15 MM PWR_15MM	PWR	PPVDD_CPU 55 60 62
J19	1.1V	MIN_NECK_WIDTH=0.15 MM PWR_10MM	PWR	PPVDD_GPU 55 60 62
J20	1.0V	MIN_NECK_WIDTH=0.15 MM PWR_2MM	PWR	PPVDD_SOC 55 60 62
J21	1.8V	MAXIMUM_NECK_LENGTH=5 MM PP_PWR	PWR	PP1V8_S2R 55 56 60 62
J26	1.8V	MAX_LINE_WIDTH=0.6 MM PWR_DP1MM	PWR	PP1V8_SW1 55 57 59 60 62
J264	1.8V	MAXIMUM_NECK_LENGTH=10 MM PWR_DP5MM	PWR	PP1V8_SW1_FOREHEAD 60 62
J28	1.8V	MIN_NECK_WIDTH=0.15 MM PP_PWR	PWR	PP1V8_EXT_SW 57 60 62
J29	1.8V	PWR_DP1MM	PWR	PP1V8_SW2 55 60 62
J24	1.8V	PP_PWR	PWR	PP1V8_S2R_SW3 55 60 62
J265	1.8V	MAX_LINE_WIDTH=0.5 MM MAXIMUM_NECK_LENGTH=10 MM PWR_DP3MM	PWR	PP1V8_S2R_SW3_COMP 60 62
J32	1.2V	MAXIMUM_NECK_LENGTH=5 MM PP_PWR	PWR	PP1V2_S2R 55 56 60 62
J19	1.2V	PWR_1MM	PWR	PP1V2_SW1 55 60 62
J167	1.2V	MAXIMUM_NECK_LENGTH=15 MM PP_PWR	PWR	PP1V2_S2R_SW2 55 60 62
J22	3.3V	MIN_NECK_WIDTH=0.1 MM PWR_1MM	PWR	PPVDD_SRAM 55 60 62
J24	3.3V	PWR_1P2MM	PWR	PP3V3_S2R 55 60 62
J25	3.3V	MAXIMUM_NECK_LENGTH=15 MM PP_PWR	PWR	PP3V3_SW 57 60 62
LDOS				
J263	3.0V	MAXIMUM_NECK_LENGTH=20 MM PP_PWR	PWR	PP3V0_SPARE1 56 60 62
J31	1.7V	PP_PWR	PWR	PP1V7_VA_VCP 56 60 62
J26	3.0V	MAX_LINE_WIDTH=0.5 MM MAXIMUM_NECK_LENGTH=10 MM PWR_DP5MM	PWR	PP3V0_S2R_SENSOR 56 60 62
J221	3.0V	MAXIMUM_NECK_LENGTH=10 MM PWR_DP5MM	PWR	PP3V0_ALS 56 60 62
J265	3.0V	PWR_0P4MM	PWR	PP3V0_UVLO 56 60 62
J222	3.3V	PP_PWR	PWR	PP3V3_ACC 56 60 62
J37	3.0V	PWR_0P3MM	PWR	PP3V0_S2R_TRISTAR 56 60 62
J37	3.0V	PWR_0P3MM	PWR	PP3V0_S2R_HALL 56 60 62
J37	1.3V	MAXIMUM_NECK_LENGTH=7 MM PP_PWR	PWR	PP1V3_CAM 56 60 62
J38	1.0V	MAXIMUM_NECK_LENGTH=15 MM PP_PWR	PWR	PP1V0_SOC 56 60 62
J39	2.6V	MAXIMUM_NECK_LENGTH=45 MM PP_PWR	PWR	PP2V6_CAM_AF 56 60 62
J40	2.9V	MAXIMUM_NECK_LENGTH=40 MM PP_PWR	PWR	PP2V9_CAM 56 60 62
J274	5.25V	MAXIMUM_NECK_LENGTH=5 MM PP_PWR	PWR	PP5V25_GRAPE 56 60 62
INPUT/MAIN/ALWAYS				
J43	4.7V	MIN_NECK_WIDTH=0.15 MM PWR_15MM	PWR	PPVCC_MAIN 47 55 56 57 58 60 62
J44	4.7V	MAXIMUM_NECK_LENGTH=15 MM PWR_10MM	PWR	PPBATT_VCC 55 60 62
J45	6.0V	PWR_2MM	PWR	PPVBUS_USB_DCIN 55 60 62
J46	1.8V	MAX_LINE_WIDTH=0.6 MM PWR_DP2MM	PWR	PP1V8_ALWAYS 56 60 62
J395	4.7V	PWR_10MM	PWR	PPBATT_AUDIO_AMP
PMU				
J51	20.4V	PP_PWR	PWR	WLED_LX_B 56 61
J47	20.4V	PP_PWR	PWR	WLED_LX_A 56 61
J48	20.4V	MAX_LINE_WIDTH=0.6 MM PWR_DP5MM	PWR	PPLED_OUT_A 56 60 62
J49	20.4V	MAX_LINE_WIDTH=0.6 MM PWR_DP5MM	PWR	PPLED_OUT_B 56 60 62
J229	20.4V	PWR_PMU	PWR	PPLED_BACK_REG_A 53 60
J230	20.4V	PWR_PMU	PWR	PPLED_BACK_REG_B 53 60
J54	6.0V	PP_PWR	PWR	PP6V0_LCM_VBOOST 56 60
J55	6.0V	PWR_0P2MM	PWR	PPVBUS_PROT 47 55 60
J57	6.0V	PP_PWR	PWR	PMU_VCENTER 55 60
J53	6.0V	PP_PWR	PWR	PP6V0_LCM_HI 56 61
J52	20.4V	PP_PWR	PWR	LCM_LX 56
J49	4.7V	PP_PWR	PWR	SW_CHGA 55 61
J56	6.0V	PWR_0P2MM	PWR	USB_VBUS_DETECT 4 55
J389	6.0V	PWR_0P2MM	PWR	USB_VBUS_DETECT_R 4
J58	6.0V		PWR	PMU_GPIO_BB_VBUS_DET 25 28 57 61

	VOLTAGE	NET_TYPE PHYSICAL	SPACING	
J4	1.8V	PP_PWR	PWR	PP1V8_PLL_SOC_F 4
J6	1.8V	PP_PWR	PWR	PP1V8_EDP_AVDD_AUX 7
J6	0.4V	PP_PWR	PWR	TP_PP0V4_MIPI0D 7
J6	0.4V	PP_PWR	PWR	TP_PP0V4_MIPI1D 7
J10	1.8V	PWR_0P2MM	PWR	PP1V8_XTAL 9
J10	1.8V	PP_PWR	PWR	PP1V8_VDD_ANA_TMPSADC 10
J14	1.2V	PP_PWR	PWR	PPVDDI_NAND 14
J16	1.8V	PP_PWR	PWR	PP1V8_DMIC_FILT 16 60
J16	3.0V	PP_PWR	PWR	PP3V0_HP_ALS_FILT 60
J17	8.75V	PP_PWR	PWR	SPKR_L1_SWITCH
J17	8.75V	PP_PWR	PWR	SPKR_R1_SWITCH
J17	1.8V	PP_PWR	PWR	PPDVDD_SPKRAMP
J18	1.7V	PP_PWR	PWR	PP1V7_VCP 15 60
J20	4.2V	PP_PWR	PWR	PPVCC_VPROG_CP 15
J20	4.2V	PP_PWR	PWR	PPVCC_VPROG_MB
J20	4.2V	PP_PWR	PWR	PPVCC_VPROG_MB_F 15
J24	4.7V	PWR_1MM	PWR	PPVCC_MAIN_LCD_SW 53 60
J24	4.7V	PWR_1MM	PWR	PPVCC_MAIN_LCD_SW_CONN 53 60
J25	4.7V	PWR_1MM	PWR	PPVCC_MAIN_GRAPE_FILT
J25	5.25V	PP_PWR	PWR	PP5V25_GRAPE_FILT
J26	1.8V	PP_PWR	PWR	PP1V8_GRAPE_SW 51 52 60 61
J26	1.8V	PP_PWR	PWR	PP1V8_GRAPE_FILT
J28	3.0V	PP_PWR	PWR	PP3V0_GYRO 19 60
J28	3.0V	PP_PWR	PWR	PP3V0_ACCEL 19 60
J29	3.0V	PWR_0P3MM	PWR	PP3V0_S2R_HALL_FILT 20 50 60
J30	1.2V	PWR_0P3MM	PWR	PP1V2_CAM_FRONT_FILT 60
J30	1.8V	PP_PWR	PWR	PP1V8_CAM_FRONT_FILT 22 60
J30	2.9V	PP_PWR	PWR	PP2V9_AVDD_CAM_FRONT_FILT 22 60
J30	3.0V	PWR_0P3MM	PWR	PP3V0_ALS_FILT 22 60
J33	2.6V	PP_PWR	PWR	PP2V6_CAM_REAR_AF_FILT 23 60
J33	1.28V	PP_PWR	PWR	PP1V3_CAM_REAR_FILT 23 60
J33	1.8V	PP_PWR	PWR	PP1V8_CAM_REAR_FILT 23 60
J33	1.28V	PP_PWR	PWR	PP1V3_CAM_REAR
J33	2.8V	PP_PWR	PWR	PP2V9_AVDD_CAM_REAR_FILT 23 60
J34	3.0V	PP_PWR	PWR	PP3V0_COMP 24 60
J34	1.8V	PP_PWR	PWR	PP1V8_COMP 24 60
J263	3.0V	PP_PWR	PWR	PP3V0_SENSOR_PROX_FILT 60
J36	3.0V	PP_PWR	PWR	PP3V0_SENSOR_PROX_ADUX1049_FILT 60
J36	3.0V	PP_PWR	PWR	PPAVDD_SENSOR_PROX_ADUX1049
J36	3.0V	PP_PWR	PWR	PP3V0_SENSOR_PROX_AD7149_FILT 45 60
J43	6.0V	PWR_2MM	PWR	PPVBUS_E75_USB_CONN 48 49 60
J47	3.3V	PP_PWR	PWR	PPOUT_E75_ACC_ID1_CONN 48 49 60
J47	3.3V	PP_PWR	PWR	PPOUT_E75_ACC_ID2_CONN 48 49 60
J47	3.3V	PP_PWR	PWR	PPOUT_E75_ACC_ID1 47 48
J47	3.3V	PP_PWR	PWR	PPOUT_E75_ACC_ID2 47 48
J49	3.0V	PP_PWR	PWR	PP3V0_IO_ALS_FILT 60
J50			ANLG	BATT_NTC 54 57 60
J50		MAXIMUM_NECK_LENGTH=20 MM PP_PWR	ANLG	BATT_SNS 54 55
J50		MAXIMUM_NECK_LENGTH=5 MM PP_PWR	ANLG	BATT_SNS_R 55

GND

	VOLTAGE	NET_TYPE PHYSICAL	SPACING	
J265	0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_AUDIO_CODEC 15 60
J167	0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_AVDD_CAM_FRONT 22
J167	0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_PP1V8_CAM_FRONT 22
J167	0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_PP2V9_CAM_FRONT 22
J265	0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_COMP 24
J265	0V	GND	GND	GND_PMU
J265	0V	GND	GND	GND_SPKR_AMP_L1
J265	0V	GND	GND	GND_SPKR_AMP_L2
J265	0V	GND	GND	GND_SPKR_AMP_R1
J265	0V	GND	GND	GND_SPKR_AMP_R2

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	3:1_SPACING

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
J165			RST	BB_TRST_L	
J166			RST	DBG_RST	DEV
J167			RST	DEBUG_RST_L 25 28 61	
J171			RST	GSM_TXBURST_IND	
J170			RST	RST_AP_1V8_L	
J168			RST	RESET_SOC_L 4 13 25 47 57 60 61	
J172			RST	GPIO_SOC2BB_RST_L 5 25 27 60	
J174			RST	RST_BB_PMU_L	
J173			RST	RST_BT_L	
J175			RST	RST_DET_L	
J176			RST	GPIO_SOC2GRAPE_RESET_L 5 52 60 61	
J177			RST	PMU_GPIO_CODEC_RST_L 15 57	
J178			RST	TS2PMU_RESET_IN 47 57	
J179			RST	GPIO_BB2SOC_RESET_DET_L 5 25 29	
J181			RST	SIMCRD_RST	
J261			RST	WDOG_SOC	
J262			RST	WDOG_SOC2PMU_RESET_IN 13 57	
J275			RST	GPIO_OSCAR_RESET_L 5 19 60	
J182			RST	ISP1_CAM_FRONT_SHUTDOWN_L 7 22	
J183			RST	ISP0_CAM_REAR_SHUTDOWN_L 7 23	
J267			RST	ISP1_CAM_FRONT_SHUTDOWN_L_F 22 60	
J268			RST	ISP0_CAM_REAR_SHUTDOWN_L_F 23 60	
J321			RST	PMU_GPIO_PMU2BBPMU_RST_L 25 27 57 60	
J322			RST	PMU_GPIO_PMU2BBPMU_RST_R_L 57	
J273			RST	JTAG_AP_TRST_L	
J274			RST	GPIO_BB_RST_L	
J325			RST	RST_PMU_IN	
J327			RST	UD881_RST	DEV
J324			RST	UD882_RST	DEV

PMU SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PMU_SENSE	*	*	3:1_SPACING
PMU_SENSE	GND	*	1.5:1_SPACING

	VOLTAGE	NET_TYPE PHYSICAL	SPACING	
J46	1.1V	PWR_SENSE	PMU_SENSE	PPVDD_CPU_SOC_SENSE 11 57 61
J46	1.1V	PWR_SENSE	PMU_SENSE	PPVDD_GPU_SOC_SENSE 11 57 61
J46	1.0V	PWR_SENSE	PMU_SENSE	PPVDD_SOC_SOC_SENSE 10 57 61
J46	1.1V	PWR_SENSE	PMU_SENSE	PPVDD_CPU_RAIL_SENSE 11 57
J46	1.1V	PWR_SENSE	PMU_SENSE	PPVDD_GPU_RAIL_SENSE 11 57
J46	1.0V	PWR_SENSE	PMU_SENSE	PPVDD_SOC_RAIL_SENSE 10 57
J46	1.05V	MIN_NECK_WIDTH=0.058 MM PWR_SENSE	PMU_SENSE	ADC_SMPS1_MSMC_1V05
J46	1.8V	MIN_NECK_WIDTH=0.058 MM PWR_SENSE	PMU_SENSE	ADC_SMPS3_MSME_1V8

RF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
RF_50S	*	50_OHM_RF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
RF_100D	*	100_OHM_RF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
100_RF	*	*	100_RF_CLEAR_SPACING
50_RF	*	*	50_RF_SPACING
50_RF_CLEAR	*	*	50_RF_CLEAR_SPACING
RF_60	*	*	1.2:1_SPACING

	VOLTAGE	NET_TYPE PHYSICAL	SPACING	
B5	4.7V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_BATT_VCC_2G_FEM 40
B6	3.8V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_PA 34 35 36 37 38 39 40
B7	1.8V	MIN_NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_DP1MM	PWR_RF	PP_LVS1 26 28
B8	1.3V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_RF1_1V3_DRX_FE 31
B9	4.7V UNDEFINED	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VREG 26
B10	2.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_RF2_2V05_DRX_BB 31
B11	4.7V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_BATT_VCC_PA_DCDC
B12	1.8V	MIN_NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_DP1MM	PWR_RF	PP_LDO1 26 60
B13	1.8V	MAX_LINE_WIDTH=1 MM PWR_DP1MM	PWR_RF	PP_LDO2_XO_HS_1V8 26 28
B14	1.8V	MAX_LINE_WIDTH=1 MM PWR_DP1MM	PWR_RF	PP_LDO3_AMUX_1V8 26 27 28
B15	3.3V	MAX_LINE_WIDTH=1 MM PWR_DP25MM	PWR_RF	PP_LDO4_VDDA_3V3 26 28
B16	2.5V	MIN_NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_DP1MM	PWR_RF	PP_LDO5_GPS_LNA_2V5 26 42
B17	1.8V	MAXIMUM_NECK_LENGTH=5 MM MIN_NECK_WIDTH=0.15 MM MAX_LINE_WIDTH=1 MM PWR_DP3MM	PWR_RF	PP_LDO6_RUIM_1V8 26 28 44 60
B18	1.8V	MIN_NECK_WIDTH=0.15 MM MAX_LINE_WIDTH=1 MM PWR_DP1MM	PWR_RF	PP_LDO6_RUIM_1V8_FILT 44
B19	1.8V	MAX_LINE_WIDTH=1 MM PWR_DP25MM	PWR_RF	PP_LDO7_DAC_1V8 26 28
B20	1.2V	MAXIMUM_NECK_LENGTH=9 MM MAX_LINE_WIDTH=1 MM PWR_DP3MM	PWR_RF	PP_LDO8_VDDPX_1V2 26 28
B21	1.05V	MAX_LINE_WIDTH=1 MM PWR_DP75MM	PWR_RF	PP_LDO9_PLL_1V05 26 28
B22	1.05V	MAX_LINE_WIDTH=1 MM PWR_DP75MM	PWR_RF	PP_LDO10_ADSP_1V05 26 28
B23	1.05V	MAX_LINE_WIDTH=1 MM PWR_DP75MM	PWR_RF	PP_LDO11_MDSP_FW_1V05 26 28
B24	1.05V	MAX_LINE_WIDTH=1 MM PWR_DP75MM	PWR_RF	PP_LDO12_MDSP_SW_1V05 26 28
B25	2.95V	MAX_LINE_WIDTH=1 MM PWR_DP1MM	PWR_RF	PP_LDO13_VDDPX_2V95 26 28
B27	2.65V	MAXIMUM_NECK_LENGTH=4 MM MAX_LINE_WIDTH=1 MM PWR_DP1MM	PWR_RF	PP_LDO14_2V65 26 33 40 41
B26	1.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VSW_S1 26
B27	1.05V	MAX_LINE_WIDTH=1 MM PWR_DP75MM	PWR_RF	PP_SMPS1_MSMC_1V05 26 28 60
B28	1.3V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VSW_S2 26
B29	1.3V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_SMPS2_RF1_1V3 26 28 31 60
B30	1.8V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VSW_S3 26
B31	1.8V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_RF1_1V8_DIG 31
B32	1.8V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_SMPS3_MSME_1V8_FILT 29
B33	2.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VSW_S4 26
B34	2.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_SMPS4_RF2_2V05 26 31 60
B35	1.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VSW_S5 26
B36	1.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_SMPS5_DSP_1V05 26 60
B34	4.7V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_BATT_VCC_PA_DCDC_IN2

	NET_TYPE PHYSICAL	SPACING	
B37	45_OHM_SE	RF_60	50_HSIC_CAL 28
B38	RF_50S	50_RF_CLEAR	50_XCVR_B13_B17_B20_TX 30 33
B39	RF_50S	50_RF	50_XCVR_2G_LB_TX 30 40
B40	RF_50S	50_RF_CLEAR	50_XCVR_B8_TX 30 33
B41	RF_50S	50_RF_CLEAR	50_XCVR_B5_B18_TX 30 33
B42	RF_50S	50_RF_CLEAR	50_XCVR_B2_B25_TX 30 32
B43	RF_50S	50_RF	50_XCVR_2G_HB_TX 30 40
B44	RF_50S	50_RF_CLEAR	50_XCVR_B3_B4_TX 30 32
B45	RF_50S	50_RF_CLEAR	50_XCVR_B1_TX 30 32
B46	RF_50S	50_RF	50_PDET_IN 30
B47	RF_50S	50_RF_CLEAR	50_PDET_PAD_OUT 30
B48	RF_50S	50_RF_CLEAR	50_PDET_PAD_IN 30 40
B49	RF_50S	50_RF_CLEAR	50_B1_TX_SAW_IN 32 33
B50	RF_50S	50_RF_CLEAR	50_B3_B4_TX_SAW_IN 32 33
B51	RF_50S	50_RF_CLEAR	50_B2_B25_TX_SAW_IN 32 33
A1	RF_50S	50_RF_CLEAR	50_B1_TX_SAW_OUT 33 34
A2	RF_50S	50_RF_CLEAR	50_B2_TX_SAW_OUT 33 35
A3	RF_50S	50_RF_CLEAR	50_B3_TX_SAW_OUT 33 35
A4	RF_50S	50_RF_CLEAR	50_B4_TX_SAW_OUT 33 34
A5	RF_50S	50_RF_CLEAR	50_B5_TX_SAW_OUT 33 37
A6	RF_50S	50_RF_CLEAR	50_B8_TX_SAW_OUT 33 37
A7	RF_50S	50_RF_CLEAR	50_B13_TX_SAW_OUT 33 38
A8	RF_50S	50_RF_CLEAR	50_B17_TX_SAW_OUT 33 38
A9	RF_50S	50_RF_CLEAR	50_B20_TX_SAW_OUT 33 36
A10	RF_50S	50_RF_CLEAR	50_PCS_RX
A11	RF_50S	50_RF	50_PCS_RX_MATCH
A12	RF_50S	50_RF_CLEAR	50_DCS_RX
A13	RF_50S	50_RF_CLEAR	50_DCS_RX_MATCH

	NET_TYPE PHYSICAL	SPACING	
B52	RF_50S	50_RF_CLEAR	50_B1_TX_PAD_IN 34
B53	RF_50S	50_RF_CLEAR	50_B4_TX_PAD_IN 34
B54	RF_50S	50_RF_CLEAR	50_B1_B4_DPLX_ANT 34
B55	RF_50S	50_RF_CLEAR	50_B1_B4_ANT 34 40
B56	RF_50S	50_RF_CLEAR	50_B1_B4_ANT_PHASESHIFT 34
B45	RF_50S	50_RF_CLEAR	50_B2_TX_PAD_IN 35
B46	RF_50S	50_RF_CLEAR	50_B3_TX_PAD_IN 35
B47	RF_50S	50_RF_CLEAR	50_B2_DUPLX_RX 32 35
B48	RF_50S	50_RF_CLEAR	50_B3_DUPLX_RX 32 35
B49	RF_50S	50_RF_CLEAR	50_B2_DPLX_ANT 35
B50	RF_50S	50_RF_CLEAR	50_B3_DPLX_ANT 35
B51	RF_50S	50_RF_CLEAR	50_B2_ANT 35 40
B52	RF_50S	50_RF_CLEAR	50_B3_ANT 35 40
B53	RF_50S	50_RF_CLEAR	50_B2_RX_BALUN 32
B54	RF_50S	50_RF_CLEAR	50_B3_RX_BALUN 32
B27	RF_50S	50_RF_CLEAR	50_B2_ANT_PHASESHIFT 35
B28	RF_50S	50_RF_CLEAR	50_B3_ANT_PHASESHIFT 35
B58	RF_50S	50_RF_CLEAR	50_B20_TX_PAD_IN 36
B59	RF_50S	50_RF_CLEAR	50_B20_DPLX_ANT 36
B60	RF_50S	50_RF_CLEAR	50_B20_ANT 36 40
B29	RF_50S	50_RF_CLEAR	50_B20_ANT_PHASESHIFT
B102	RF_50S	50_RF_CLEAR	50_B5_TX_PAD_IN 37
B103	RF_50S	50_RF_CLEAR	50_B8_TX_PAD_IN 37
B104	RF_50S	50_RF_CLEAR	50_B5_DPLX_ANT 37
B103	RF_50S	50_RF_CLEAR	50_B8_DPLX_ANT 37
B105	RF_50S	50_RF_CLEAR	50_B5_ANT 37 40
B106	RF_50S	50_RF_CLEAR	50_B8_ANT 37 40
B107	RF_50S	50_RF_CLEAR	50_B5_ANT_PHASESHIFT
B233	RF_50S	50_RF_CLEAR	50_B8_ANT_PHASESHIFT 37
B233	RF_50S	50_RF_CLEAR	50_B7_ANT 36 40
B234	RF_50S	50_RF_CLEAR	50_B7_BALUN_IN_RX
B235	RF_50S	50_RF_CLEAR	50_B7_DPLX_ANT 36
B236	RF_50S	50_RF_CLEAR	50_B7_DUPLX_RX 32 36
B237	RF_50S	50_RF_CLEAR	50_B7_TX_PAD_IN 36
B238	RF_50S	50_RF_CLEAR	50_B7_TX_SAW_IN 36
B239	RF_50S	50_RF_CLEAR	50_B7_TX_SAW_OUT 36
B262	RF_50S	50_RF_CLEAR	50_XCVR_B7_TX 30 36
B122	RF_50S	50_RF_CLEAR	50_B13_TX_PAD_IN 38
B124	RF_50S	50_RF_CLEAR	50_B17_TX_PAD_IN 38
B126	RF_50S	50_RF_CLEAR	50_B13_DPLX_ANT 38
B125	RF_50S	50_RF_CLEAR	50_B17_DPLX_ANT 38
B127	RF_50S	50_RF_CLEAR	50_B13_LPF_IN 38
B130	RF_50S	50_RF_CLEAR	50_B13_ANT 38 40
B129	RF_50S	50_RF_CLEAR	50_B17_ANT 38 40
B232	RF_50S	50_RF_CLEAR	50_B13_ANT_PHASESHIFT
B231	RF_50S	50_RF_CLEAR	50_B17_ANT_PHASESHIFT 38
B135	RF_50S	50_RF_CLEAR	50_XCVR_2G_LB_TX_MATCH
B134	RF_50S	50_RF_CLEAR	50_XCVR_2G_HB_TX_MATCH 40
B132	RF_50S	50_RF_CLEAR	50_2G_LB_PA_IN 40
B133	RF_50S	50_RF_CLEAR	50_2G_HB_PA_IN 40
B265	RF_50S	50_RF_CLEAR	50_PRI_ANT_ASM 40
B140	RF_50S	50_RF_CLEAR	50_DRX_ANT_TEST 41 43
B141	RF_50S	50_RF_CLEAR	50_DRX_ANT_PHASESHIFT 43
B227	RF_50S	50_RF_CLEAR	50_DRX_ANT_FEED 43
B157	RF_50S	50_RF_CLEAR	50_COUPLER_TERM
B158	RF_50S	50_RF_CLEAR	50_DIVERSITY_SWITCH_MATCH 41
B159	RF_50S	50_RF_CLEAR	50_GPS_LNA_OUT 41 42
B158	RF_50S	50_RF_CLEAR	50_GPS_ANT_COAX 42
B160	RF_50S	50_RF_CLEAR	50_GPS_ANT_MATCH
B227	RF_50S	50_RF_CLEAR	50_GPS_ANT_TEST
B229	RF_50S	50_RF_CLEAR	50_GPS_LNA_IN 42
B260	RF_50S	50_RF_CLEAR	50_PRI-ANT_COUPLER
B261	RF_50S	50_RF_CLEAR	50_PRI-ANT_PHASE
B270	RF_50S	50_RF_CLEAR	50_PRI_ANT_TEST
B270	RF_50S	50_RF_CLEAR	50_PRI_ANT_TEST_IN
B270	RF_50S	50_RF_CLEAR	50_PRI_ANT_COAX 40 43
B266	RF_50S	50_RF_CLEAR	50_ANT2_TERM
B266	RF_50S	50_RF_CLEAR	50_DRX_ANT_TERM
B223	RF_60		2G_FEM_S0 29 40
B224	RF_60		2G_FEM_S1 25 29 40
B225	RF_60		2G_FEM_S2 29 33 40
B226	RF_60		2G_FEM_S3 29 33 40
B241	RF_60		2G_FEM_S4 25 29 40
B242	RF_60		2G_FEM_S5 29 40
B243	RF_60		2G_FEM_S6 29 40
B244	RF_60		BB_PDM 29 39
B245	RF_60		BB_PDM_FILT 39
B246	RF_60		DCDC_ADJ 39
B247	RF_60		PA_R1 29 34 35 36 37 38

	NET_TYPE PHYSICAL	SPACING	
B270	RF_60		WTR_GP_DATA0 29 30
B271	RF_60		WTR_GP_DATA1 29 30
B272	RF_60		BB_ERROR_FLAG 25 29
B273	RF_60		PA_ON_B1_B4 29 34
B274	RF_60		PA_ON_B2_B3 29 35
B275	RF_60		PA_ON_B5_B8 29 37
B276	RF_60		PA_ON_B7_B20 29 36
B277	RF_60		PA_ON_B13_B17 29 38
B280	RF_60		PA_BS 29 34 35 36 37 38
B281	RF_60		LAT_SW1_CTL 25 29
B282	RF_60		PS_HOLD 27 29
B283	RF_60		WTR_RF_ON 25 29 30
B284	RF_60		WTR_RX_ON 25 29 30
B285	RF_60		DCDC_MODE 29 39
B286	RF_60		DCDC_ENABLE
B287	RF_60		DRX_ASM_V1 29 41
B288	RF_60		DRX_ASM_V2 29 41
B289	RF_60		DRX_ASM_V3 29 41
B290	RF_60		DRX_ASM_V4 29 41
B291	RF_60		19P2M_CLK_EN 27 28
B292	RF_60		PMIC_RESOUT_L 25 27 28
B293	RF_60		PMIC_SSBI 25 27 28

	NET_TYPE PHYSICAL	SPACING	
B107	RF_DIFF	RF_DIFF	RF_60 TX_BB_Q_P 29 30
B109	RF_DIFF	RF_DIFF	RF_60 TX_BB_Q_N 29 30
B108	RF_DIFF	RF_DIFF	RF_60 DRX_BB_Q_P 29 30
B110	RF_DIFF	RF_DIFF	RF_60 DRX_BB_Q_N 29 30
B112	RF_DIFF	RF_DIFF	RF_60 GPS_BB_Q_P 29 30
B111	RF_DIFF	RF_DIFF	RF_60 GPS_BB_Q_N 29 30
B113	RF_DIFF	RF_DIFF	RF_60 PRX_BB_Q_P 29 30
B114	RF_DIFF	RF_DIFF	RF_60 PRX_BB_Q_N 29 30
B115	RF_DIFF	RF_DIFF	RF_60 DRX_BB_I_P 29 30
B116	RF_DIFF	RF_DIFF	RF_60 DRX_BB_I_N 29 30
B117	RF_DIFF	RF_DIFF	RF_60 GPS_BB_I_P 29 30
B118	RF_DIFF	RF_DIFF	RF_60 GPS_BB_I_N 29 30
B119	RF_DIFF	RF_DIFF	RF_60 PRX_BB_I_P 29 30
B120	RF_DIFF	RF_DIFF	RF_60 PRX_BB_I_N 29 30
B122	RF_DIFF	RF_DIFF	RF_60 TX_BB_I_P 29 30
B121	RF_DIFF	RF_DIFF	RF_60 TX_BB_I_N 29 30
B169	RF_DIFF	RF_100D	100_RF 100_XCVR_B13_B17_B20_PRX_P 30 33
B170	RF_DIFF	RF_100D	100_RF 100_XCVR_B13_B17_B20_PRX_N 30 33
B171	RF_DIFF	RF_100D	100_RF 100_XCVR_B8_PRX_P 30 32
B172	RF_DIFF	RF_100D	100_RF 100_XCVR_B8_PRX_N 30 32
B173	RF_DIFF	RF_100D	100_RF 100_XCVR_B5_B18_PRX_P 30 32
B174	RF_DIFF	RF_100D	100_RF 100_XCVR_B5_B18_PRX_N 30 32
B175	RF_DIFF	RF_100D	100_RF 100_XCVR_B2_B25_PRX_P 30 32
B176	RF_DIFF	RF_100D	100_RF 100_XCVR_B2_B25_PRX_N 30 32
B177	RF_DIFF	RF_100D	100_RF 100_XCVR_B3_PRX_P 30 32
B178	RF_DIFF	RF_100D	100_RF 100_XCVR_B3_PRX_N 30 32
B179	RF_DIFF	RF_100D	100_RF 100_XCVR_DCS_PCS_PRX_P
B181	RF_DIFF	RF_100D	100_RF 100_XCVR_DCS_PCS_PRX_N
B182	RF_DIFF	RF_100D	100_RF 100_XCVR_B1_B4_PRX_P 30 32
B180	RF_DIFF	RF_100D	100_RF 100_XCVR_B1_B4_PRX_N 30 32
B184	RF_DIFF	RF_100D	100_RF 100_XCVR_B8_B20_DRX_P 30 41
B183	RF_DIFF	RF_100D	100_RF 100_XCVR_B8_B20_DRX_N 30 41
B185	RF_DIFF	RF_100D	100_RF 100_XCVR_B5_B18_B13_B17_DRX_P 30 41
B187	RF_DIFF	RF_100D	100_RF 100_XCVR_B5_B18_B13_B17_DRX_N 30 41
B186	RF_DIFF	RF_100D	100_RF 100_XCVR_B2_B25_B3_DRX_P 30 41
B188	RF_DIFF	RF_100D	100_RF 100_XCVR_B2_B25_B3_DRX_N 30 41
B190	RF_DIFF	RF_100D	100_RF 100_XCVR_B1_B4_DRX_P 30 41
B189	RF_DIFF	RF_100D	100_RF 100_XCVR_B1_B4_DRX_N 30 41
B152	RF_DIFF	RF_100D	100_RF 100_XCVR_GPS_RX_P 30 41
B151	RF_DIFF	RF_100D	100_RF 100_XCVR_GPS_RX_N 30 41
B195	RF_DIFF	RF_100D	100_RF 100_B13_DUPLX_RX_P 33 38
B193	RF_DIFF	RF_100D	100_RF 100_B13_DUPLX_RX_N 33 38
B194	RF_DIFF	RF_100D	100_RF 100_B17_DUPLX_RX_P 33 38
B197	RF_DIFF	RF_100D	100_RF 100_B17_DUPLX_RX_N 33 38
B198	RF_DIFF	RF_100D	100_RF 100_B20_DUPLX_RX_P 33 36
B199	RF_DIFF	RF_100D	100_RF 100_B20_DUPLX_RX_N 33 36
B138	RF_DIFF	RF_100D	100_RF 100_DCS_PCS_RX_FILTER_P
B139	RF_DIFF	RF_100D	100_RF 100_DCS_PCS_RX_FILTER_N
B205	RF_DIFF	RF_100D	100_RF 100_B1_B4_DUPLX_RX_P 32 34
B206	RF_DIFF	RF_100D	100_RF 100_B1_B4_DUPLX_RX_N 32 34
B207	RF_DIFF	RF_100D	100_RF 100_B8_DUPLX_RX_P 32 37
B210	RF_DIFF	RF_100D	100_RF 100_B8_DUPLX_RX_N 32 37
B211	RF_DIFF	RF_100D	100_RF 100_B5_B18_DUPLX_RX_P 32 37
B209	RF_DIFF	RF_100D	100_RF 100_B5_B18_DUPLX_RX_N 32 37
B265	RF_DIFF	RF_100D	100_RF 100_B7_PRX_BALUN_OUT_P 32
B264	RF_DIFF	RF_100D	100_RF 100_B7_PRX_BALUN_OUT_N 32
B263	RF_DIFF	RF_100D	100_RF 100_B7_PRX_MATCH_P 32
B267	RF_DIFF	RF_100D	100_RF 100_B7_PRX_MATCH_N 32
B268	RF_DIFF	RF_100D	100_RF 100_XCVR_B7_PRX_P 30 32
B266	RF_DIFF	RF_100D	100_RF 100_XCVR_B7_PRX_N 30 32
B250			RF_CLK SLEEP_CLK_32K 25 27 28
B252			RF_CLK 19P2M_WTR 27 30
B251			RF_CLK 19P2M_MDM 25 27 28

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
50_RF_SPACING	TOP,BOTTOM	0.178 MM	?
50_RF_SPACING	ISL3	0.130 MM	?
50_RF_SPACING	*	0.092 MM	?
50_RF_CLEAR_SPACING	TOP,BOTTOM	0.178 MM	?
50_RF_CLEAR_SPACING	ISL3	0.130 MM	?
50_RF_CLEAR_SPACING	*	0.138 MM	?
100_RF_CLEAR_SPACING	TOP,BOTTOM	0.143 MM	?
100_RF_CLEAR_SPACING	*	0.118 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	50_RF	*	50_RF_CLEAR_SPACING
GND	50_RF_CLEAR	*	50_RF_CLEAR_SPACING
GND	100_RF	*	100_RF_CLEAR_SPACING
GND	RF_60	*	1.2:1_SPACING
GND	PWR_RF	*	1.2:1_SPACING
PWR_RF	PWR_RF	*	1.2:1_SPACING
RF_CLK	*	*	3:1_SPACING
RF_CLK	GND	*	1.2:1_SPACING

NC_PMU_OUT_32K_CLK_GPS = PMU_OUT_32K_CLK_GPS IN 57 64
NO_TEST=TRUE
MAKE_BASE=TRUE

RF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
WIFI_50S	*	50_OHM_RF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
WIFI	*	*	4:1_SPACING