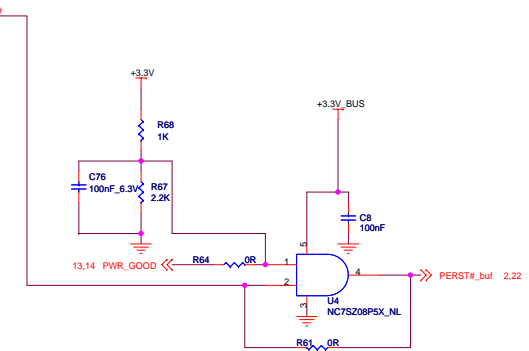
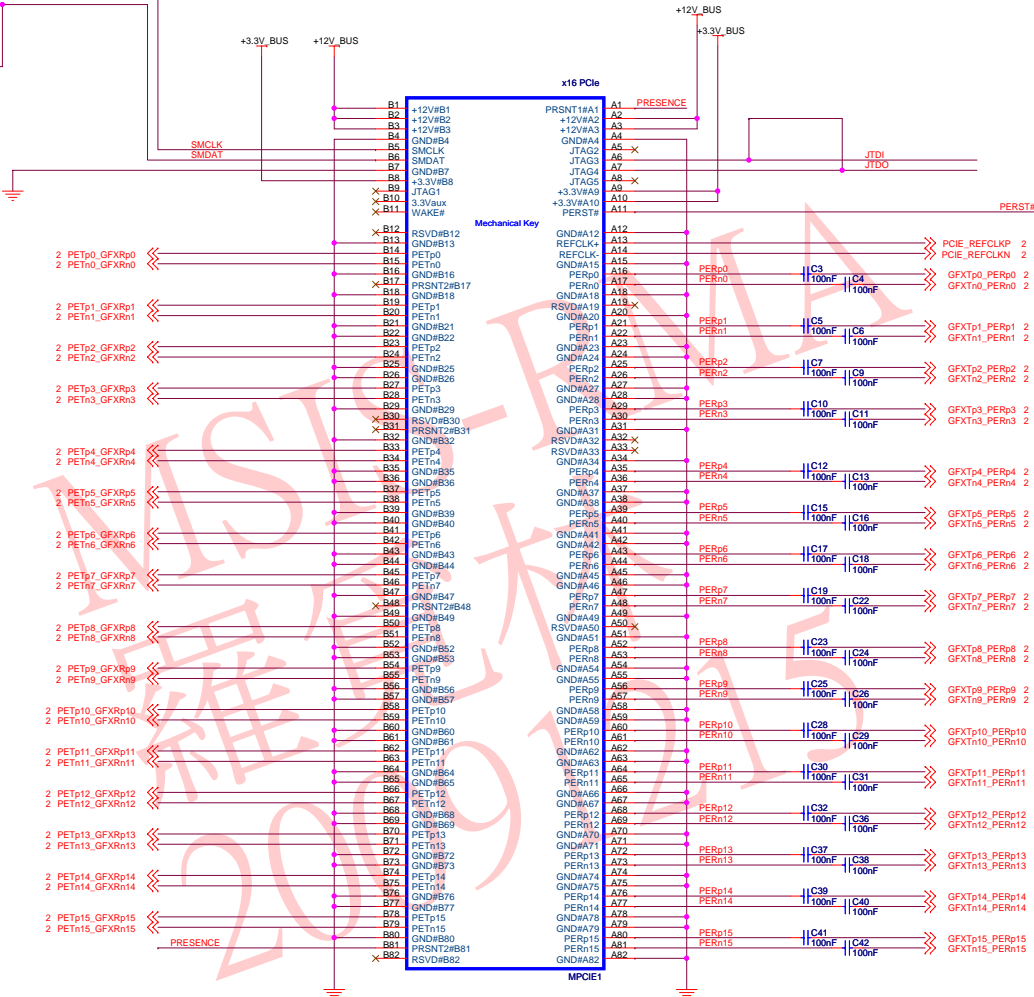
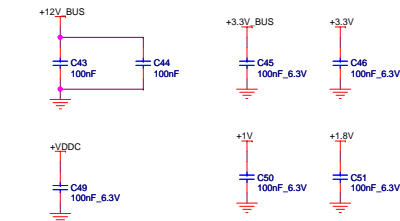
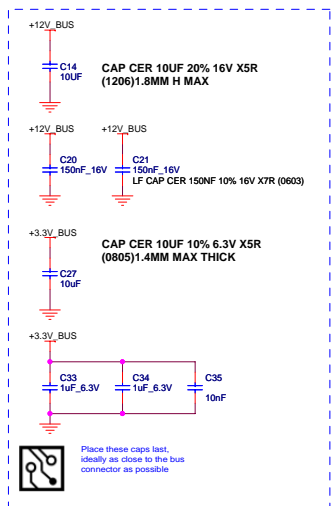
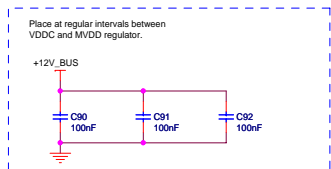
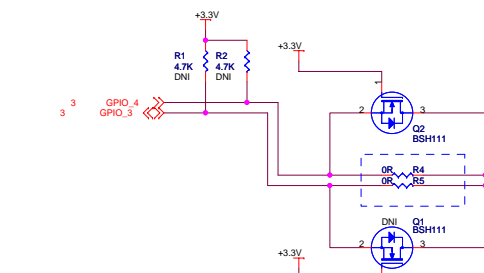


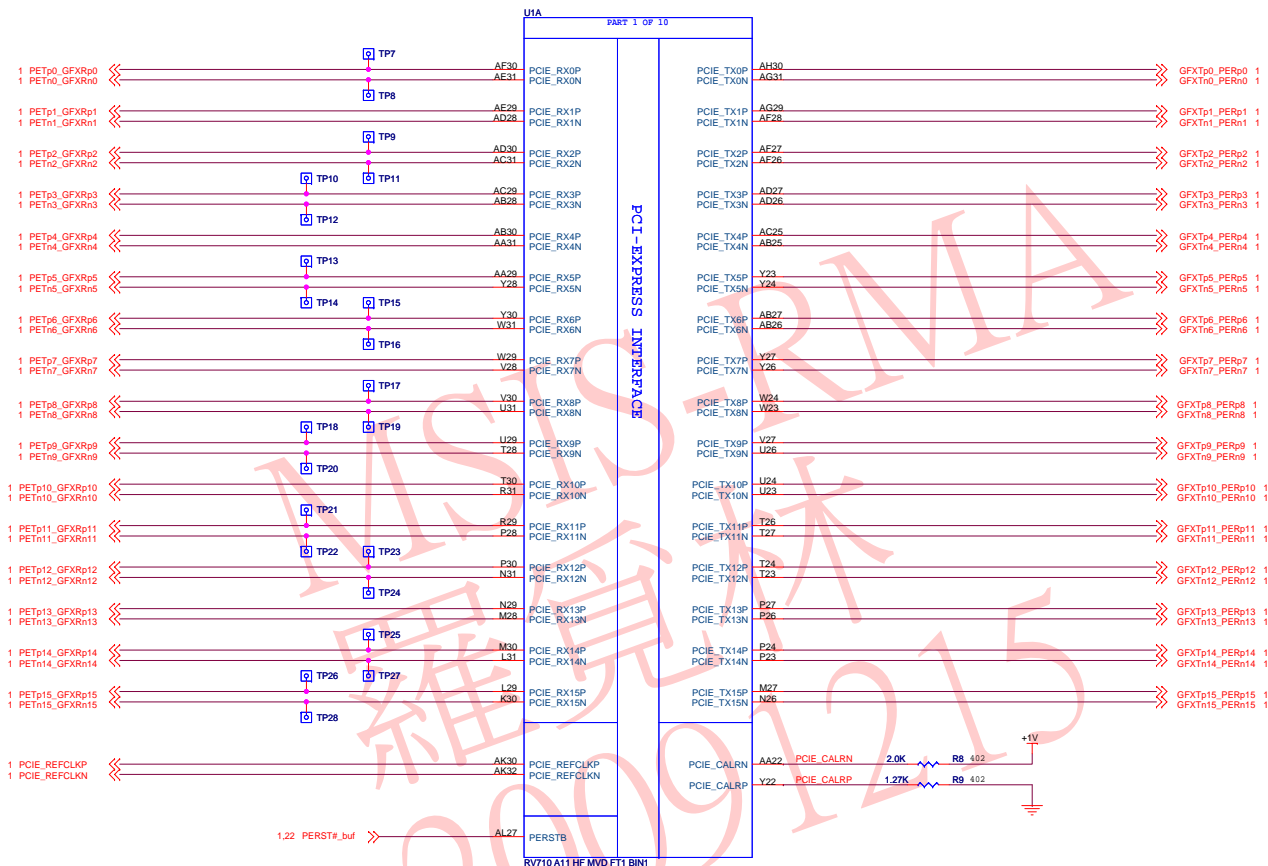
PCI-EXPRESS EDGE CONNECTOR



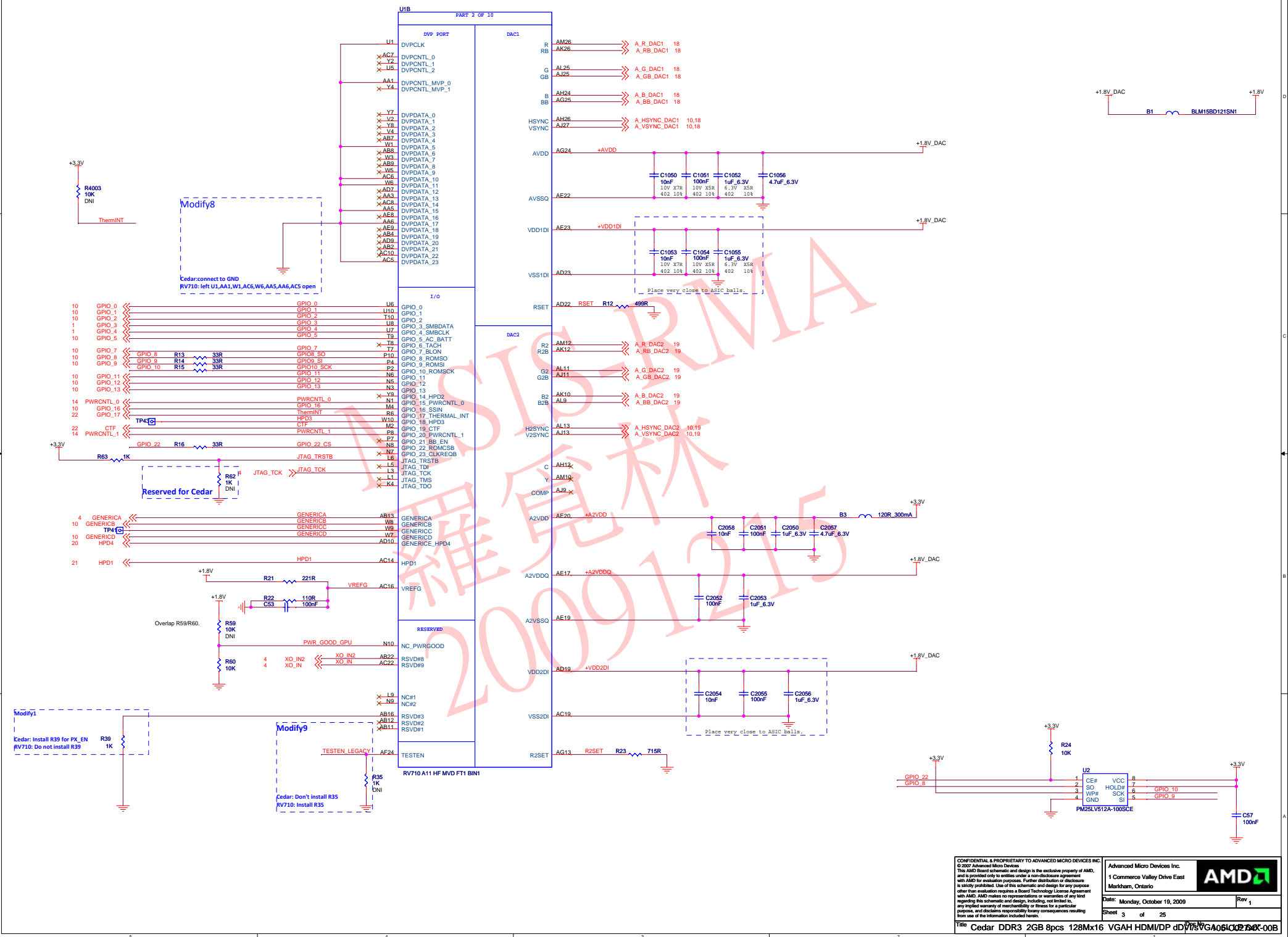
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

(2) Cedar PCIE Interface

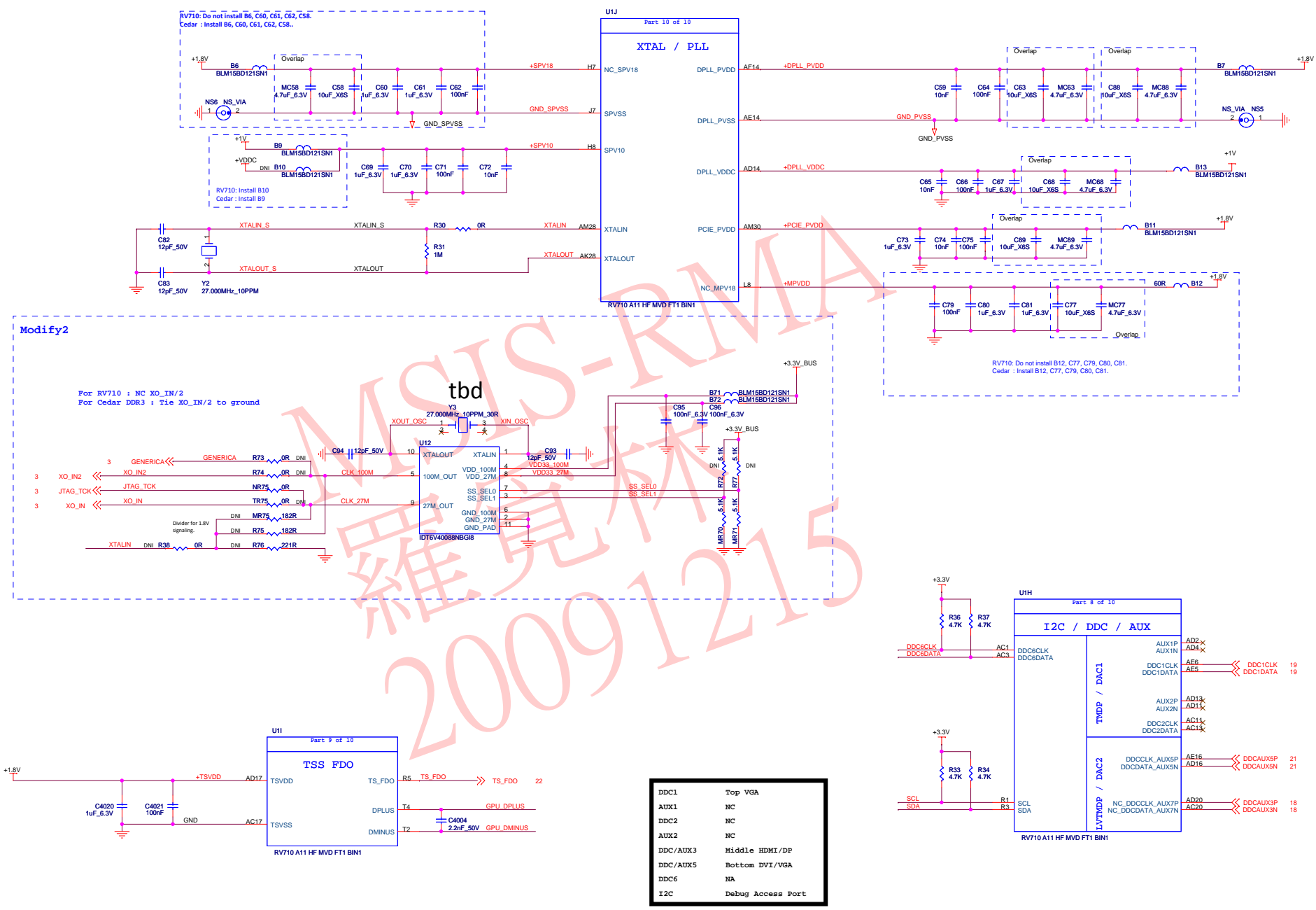
NOTE: some of the PCIE testpoints will be available through via on traces.



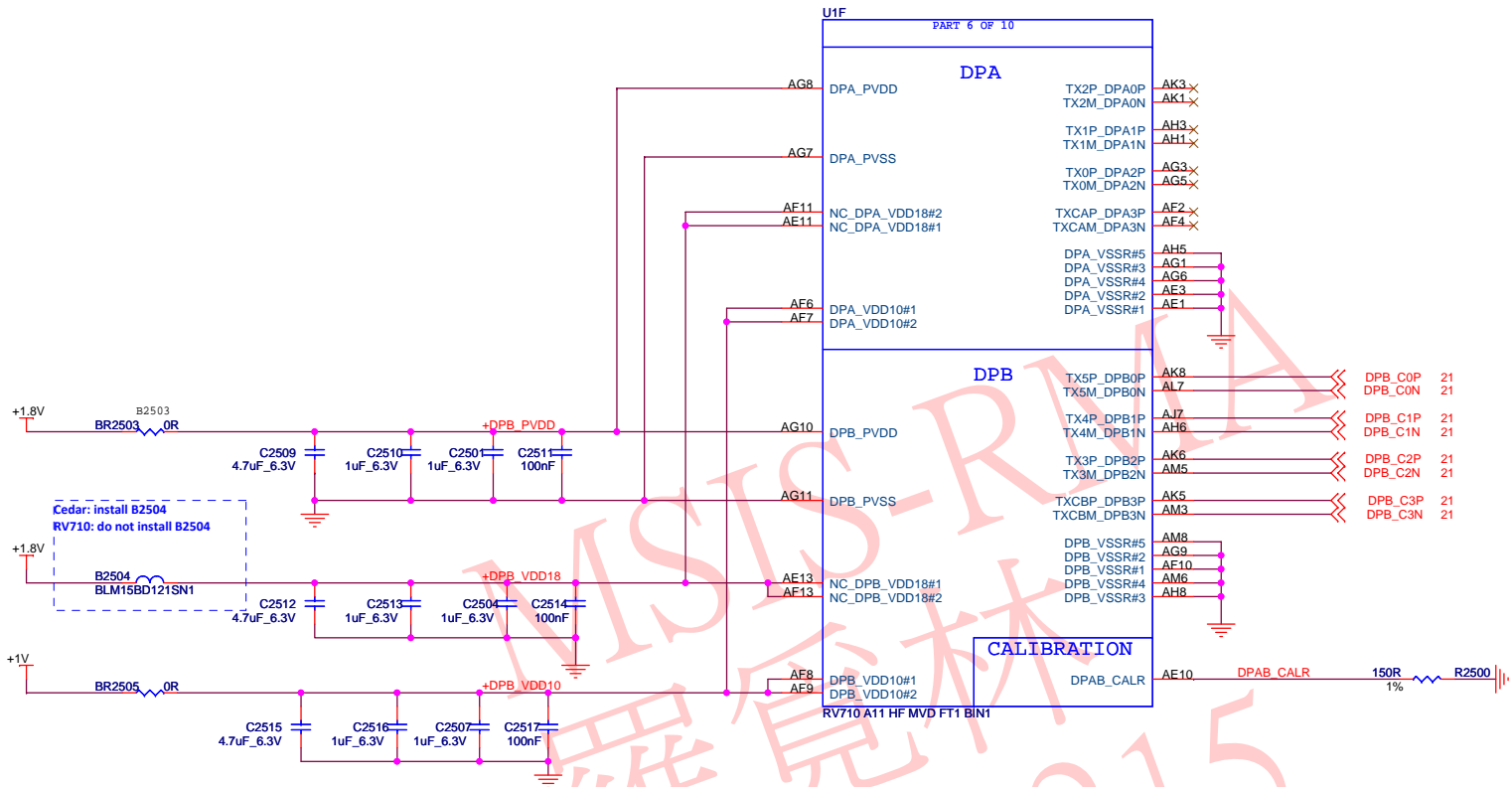
(3) Cedar Main



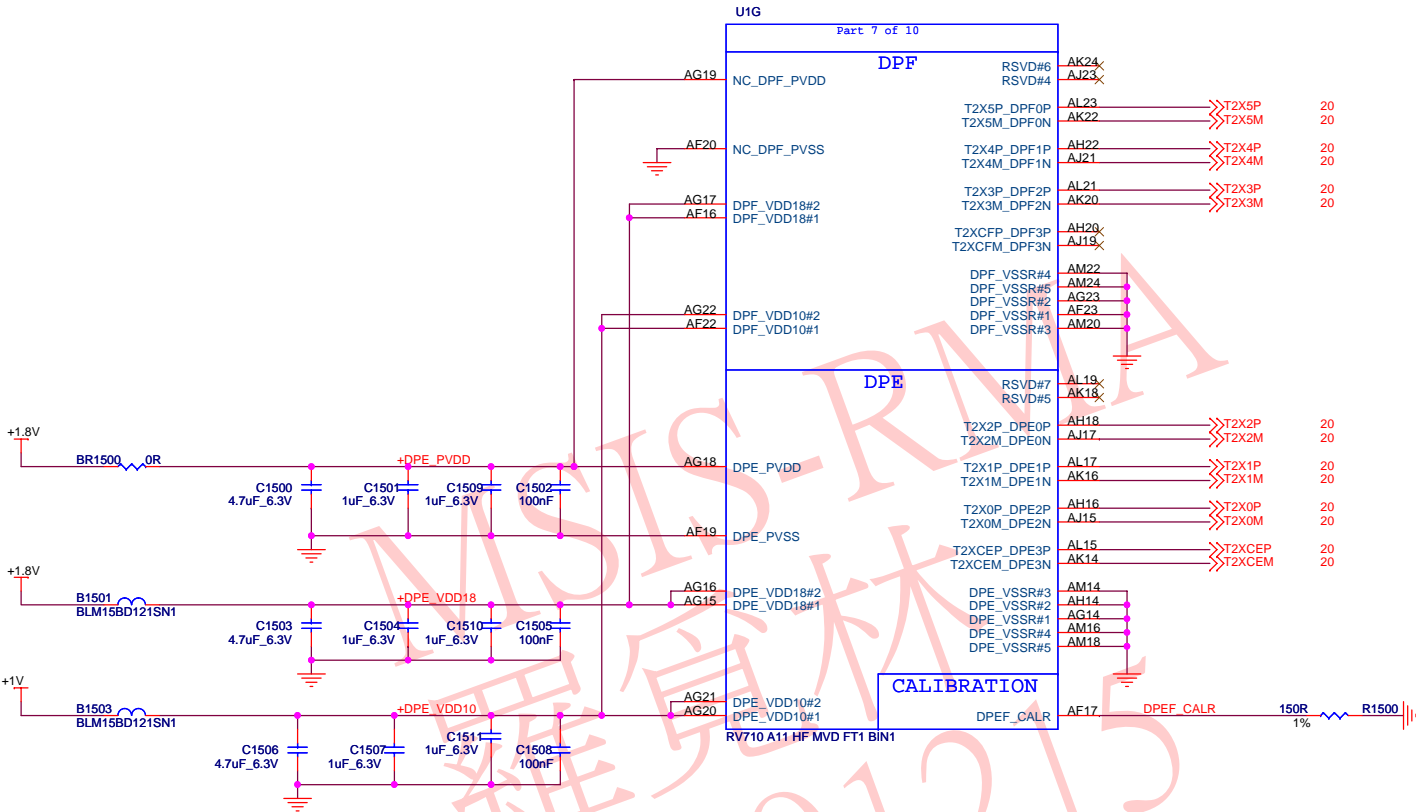
(04) Cedar GPIOs CF XTAL



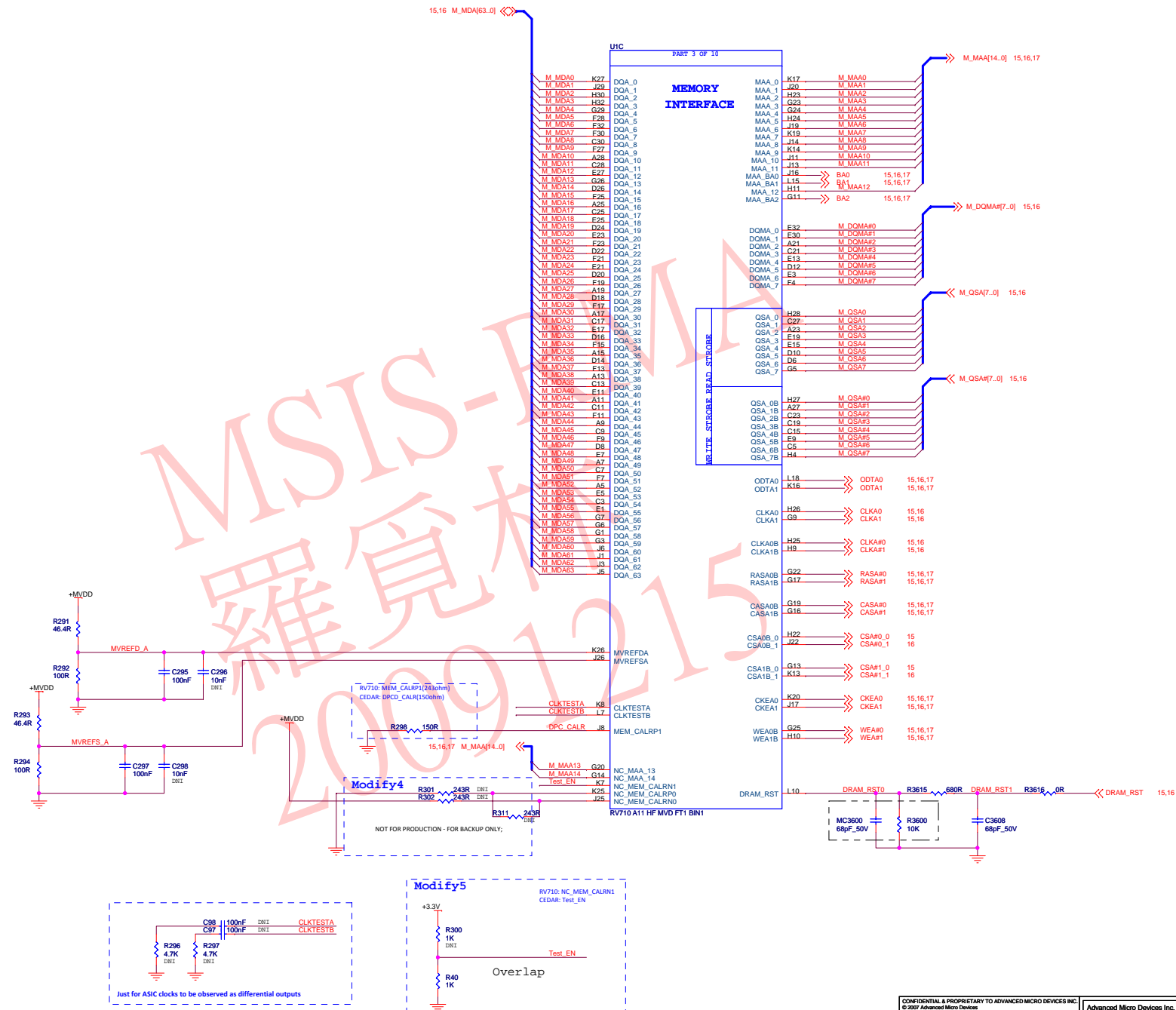
TMDP INTERFACE



LVTMDP INTERFACE



MEMORY INTERFACE



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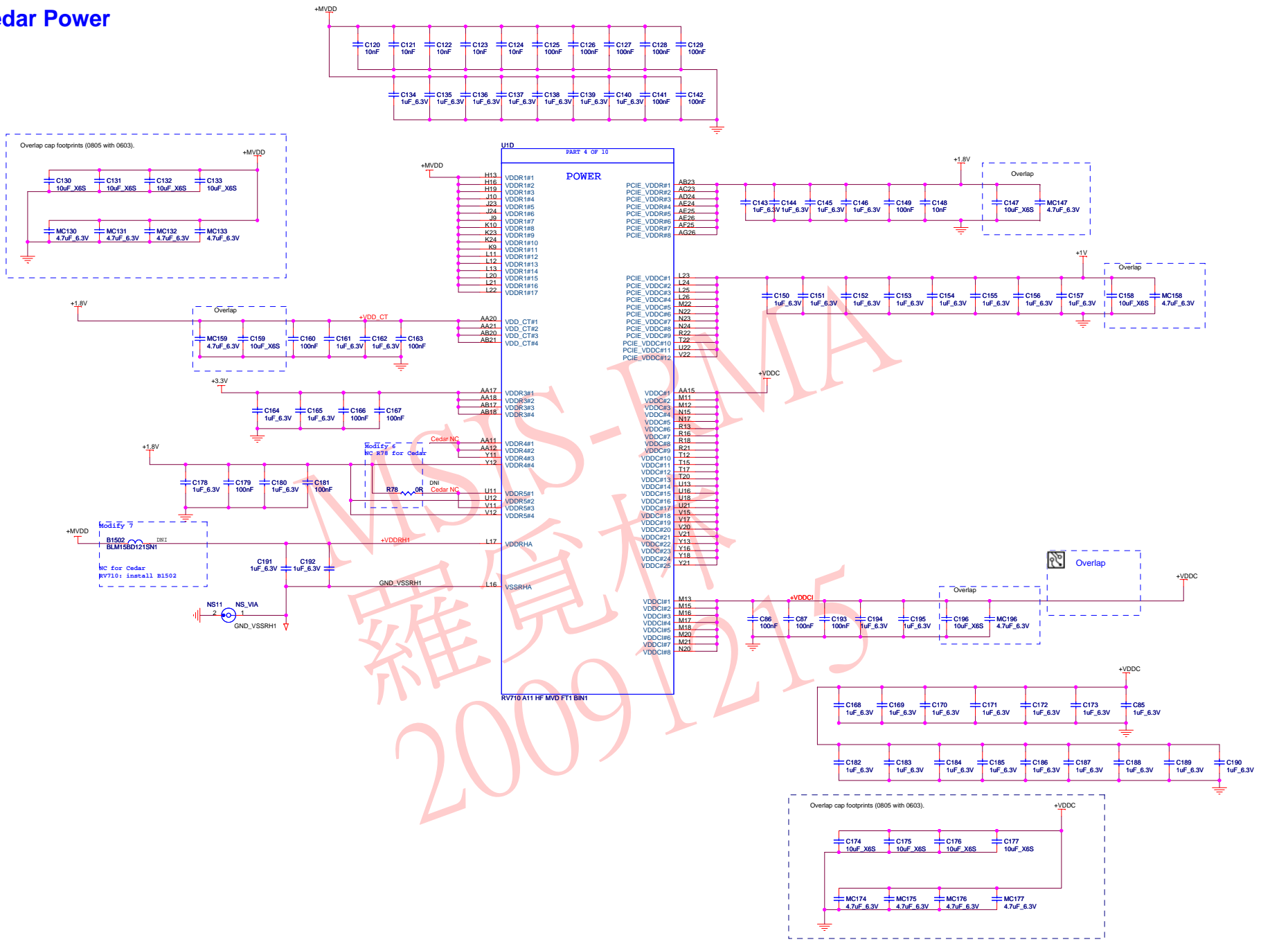
Date: Monday, October 19, 2009

Rev 2

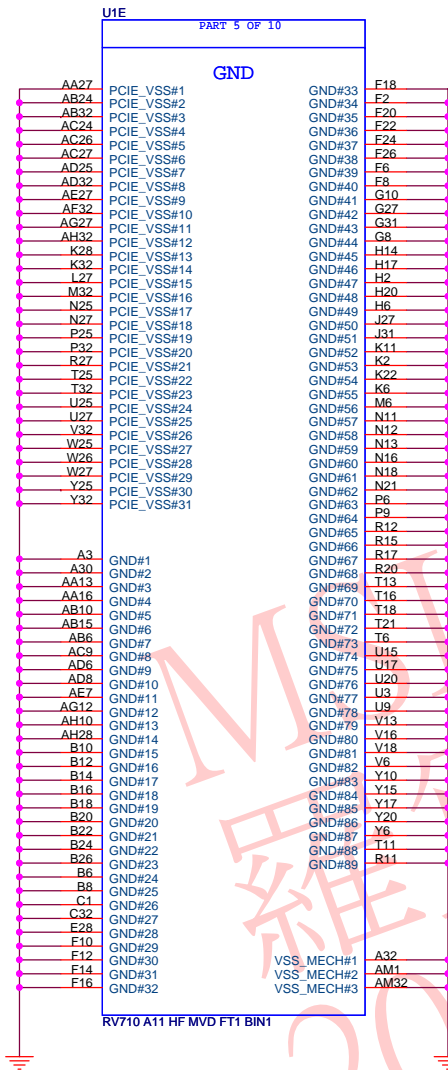
Sheet 7 of 25

25

(08) Cedar Power



(09) Cedar GND



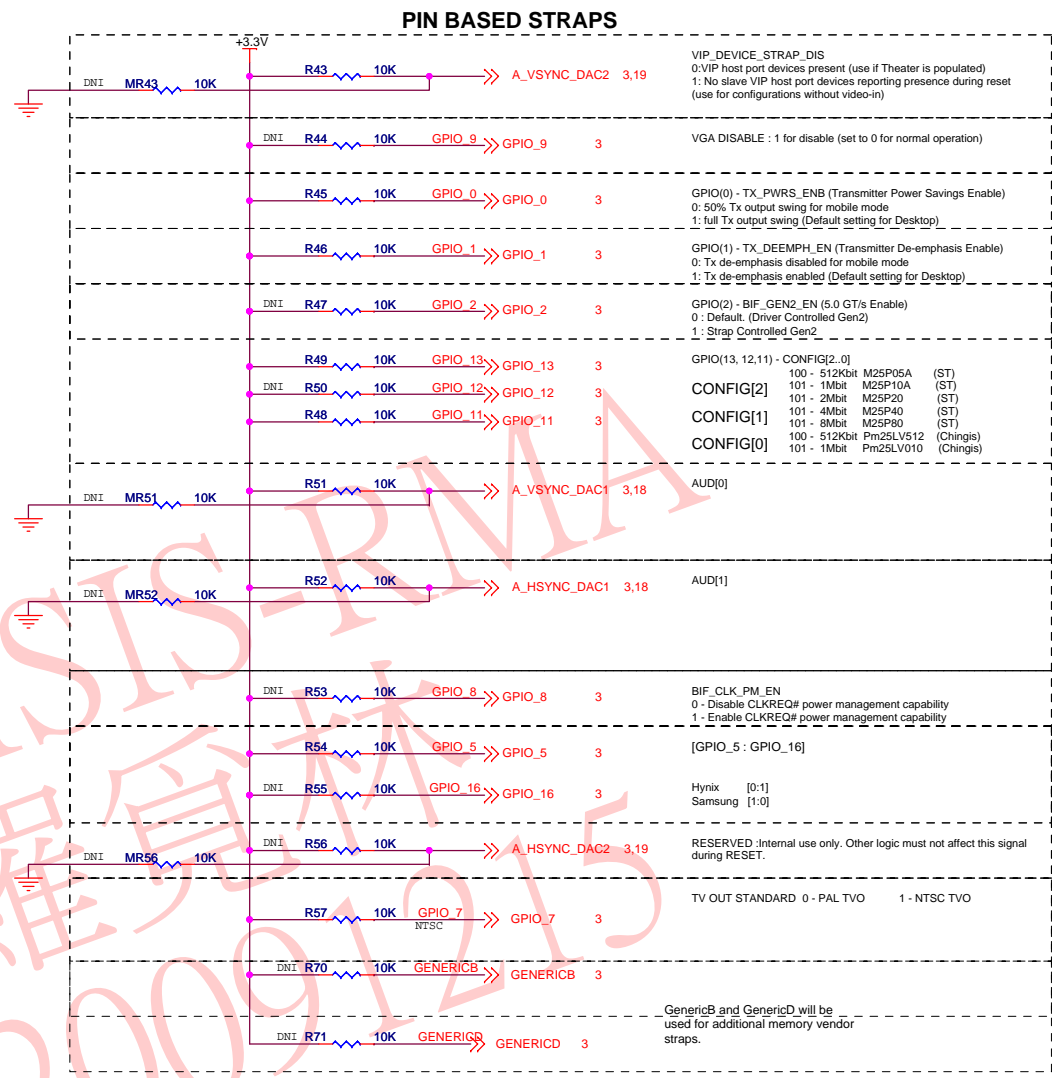
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Title Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI7/SVGA/15.5" LCD/20" W-00

(10) Cedar STRAPS



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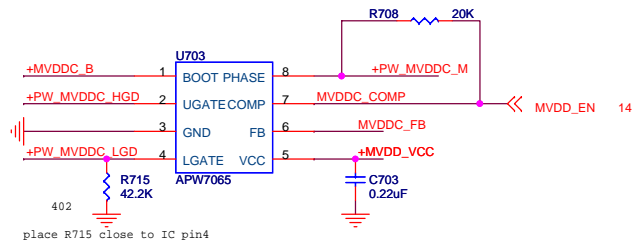
Rev 2

AMD

Doc No: 105-00708-00

Title: Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDV7/SVGA105-00708-00

(12) MVDD

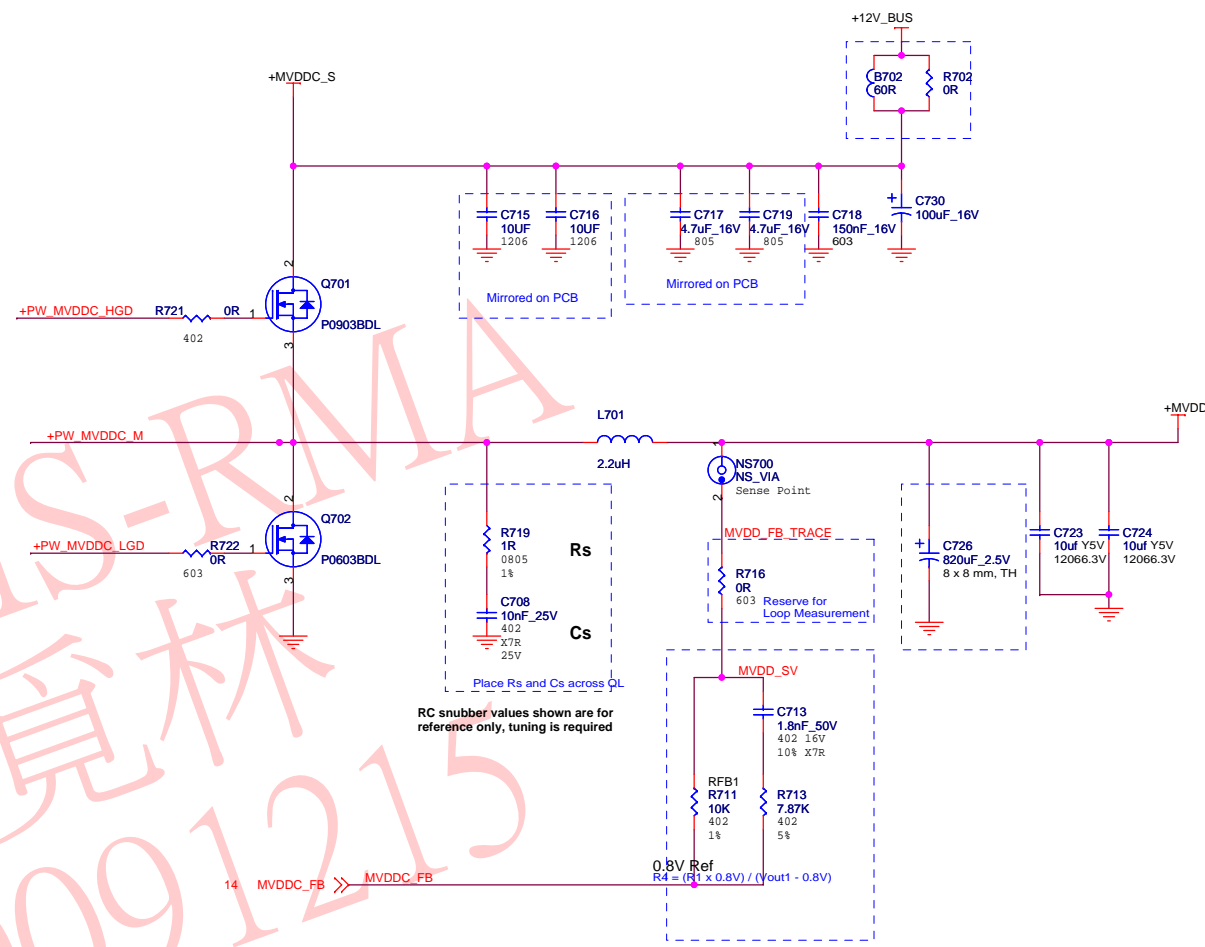


Layout guideline

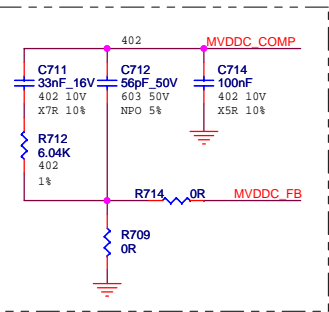
1-Position the controller (U703) such that LGate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.

2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows:

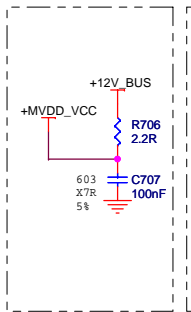
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



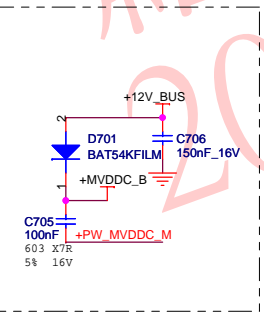
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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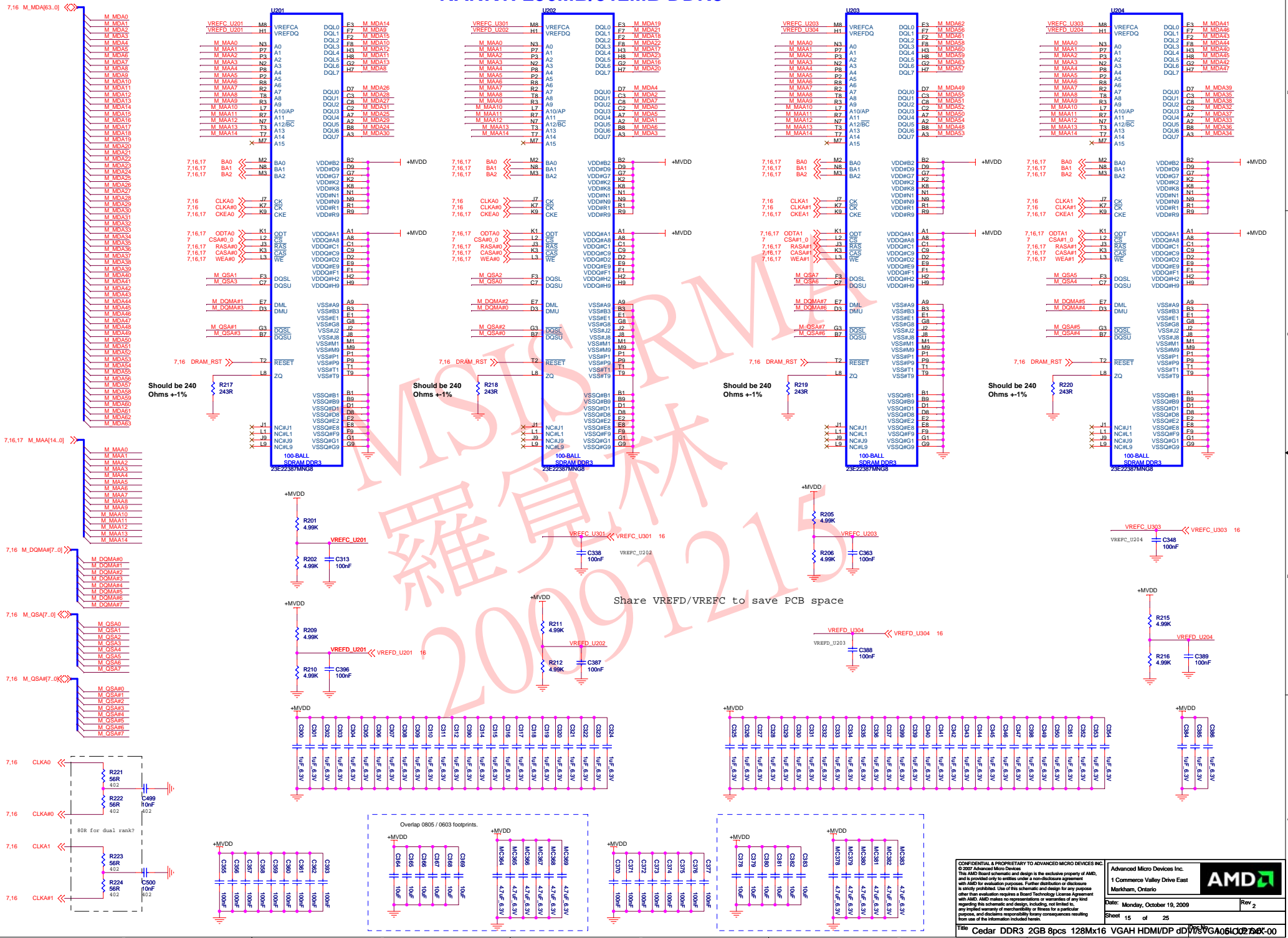
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Date: Monday, October 19, 2009 Rev 2
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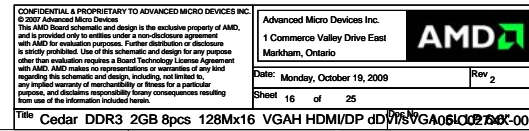
Title Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDV7/SVG105C027K&00

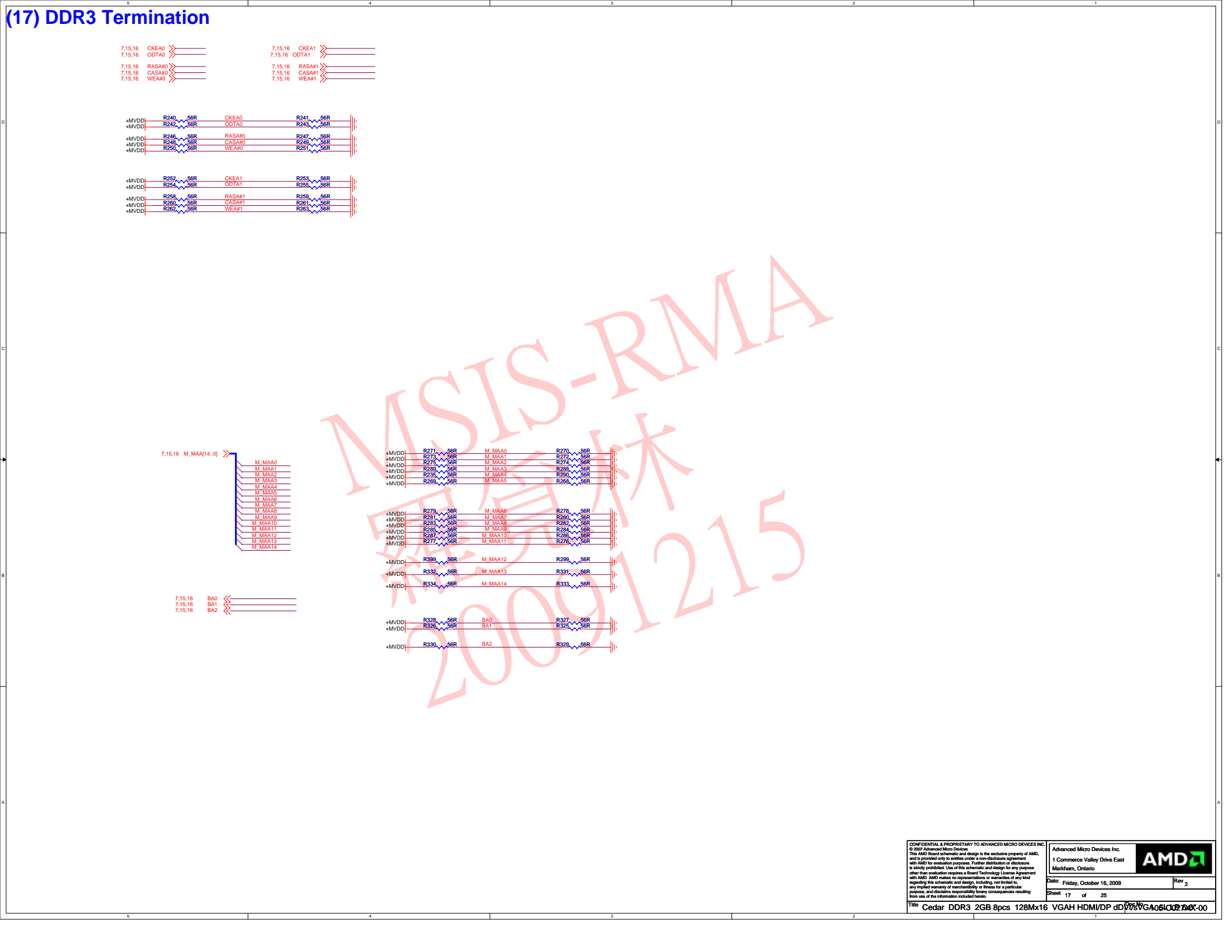
(15) DDR3 RANK1

RANK1: 256MB/512MB DDR3

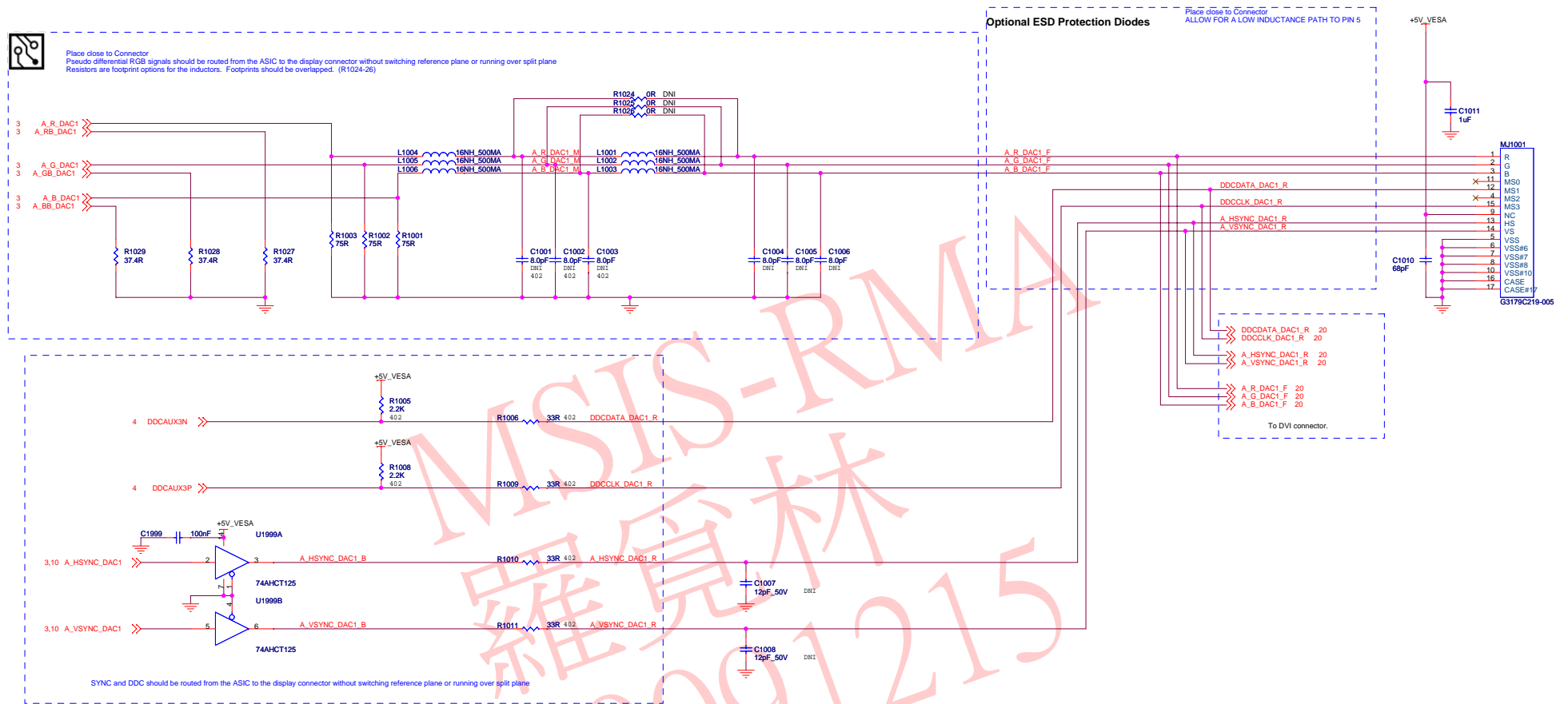


RANK2: 256MB/512MB DDR3





DAC 1 OUTPUT



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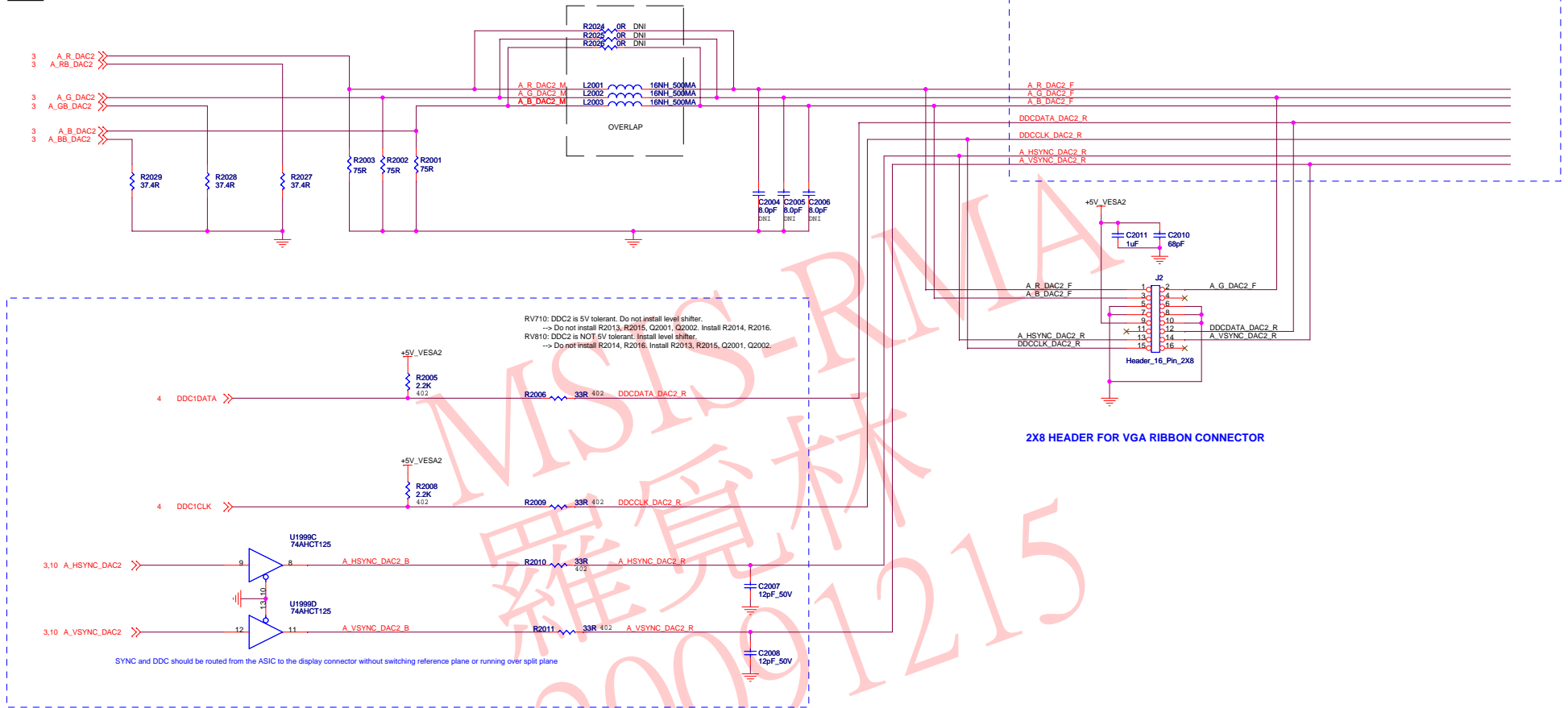
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Title Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP d0175VGA061002100-00

DAC 2 OUTPUT



Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane



Optional ESD Protection Diods

Place near D2002, D2003, D2004, D2005

2X8 HEADER FOR VGA RIBBON CONNECTOR

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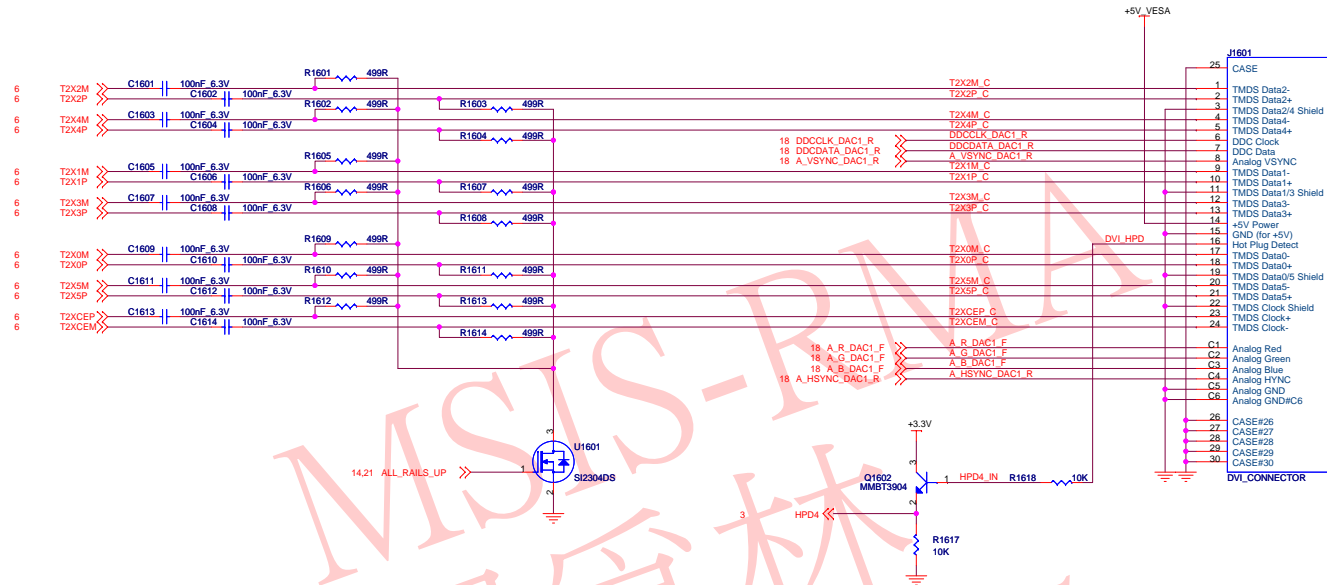
Rev 2

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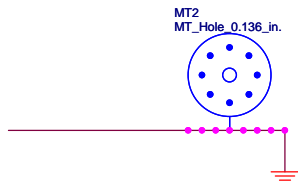
25

Title	Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI/VGA06L02200-00
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DPE / DPF OUTPUT







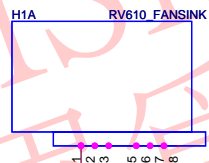
SKU	P/N	CONFIGURATION	Form Factor
PERCH	8020051300G	DVI + DP + VGA	FH / SS
BASS	8020051400G	DVI +HDMI+ VGA	FH / SS
PERCH	8020051600G	DVI + DP	LP / SS
BASS	80200516A0G	DVI +HDMI	LP / SS
PERCH	8020051700G	DVI + DP + VGA	FH / DS
BASS	80200517A0G	DVI +HDMI+ VGA	FH / DS



Square Fansink 12W

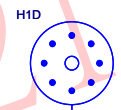
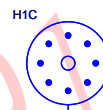
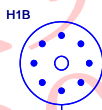
7120036200G BLACK

7120336200G RED



Rectangular Fansink 22W

7120035100G



Dual-slot Heatsink 14W

7120181000G

For DVI Connector

ASSY-SCREW200

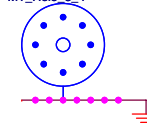
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW201

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

Bracket Components

MT200
MT_Hole 3.4



ASSY-SCREW202

SCREW
SCREW

7020005200G

ASSY1

BRACKET

8020040100G

ASSY2

BRACKET
LP

8020040400G

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Rev 1

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Title Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI/SVG 105C0270&~00B

<div>AMD</div>			Title			Schematic No.		Date:	
			Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI/sVGA 6L LP 6.6"			105-C027XX-00		Friday, October 16, 2009	
			REVISION HISTORY					NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.	
Sch Rev	PCB Rev	Date	Cedar 1GB DDR3 Walleye			REVISION DESCRIPTION			
0	00A	2008.12.30	Sch no change. just modify HDMI connector location on PCB						
1	00B	2009.08.24	Page 1:remove C1,C2,R3,U3,Add Q1,Q2 Page 7:Add C97,C98 Page 10:Add MR43,MR51,MR52,MR56 Page 18:Add L1004,L1005,L1006 Page 19:Remove R2013,R2014,R2015,R2016,Q2001,Q2002						
2	00	2009.09.23	Change HDMI/DP DDC line to DDCAUX3						

MSIS-RMA

羅覓林

20091215

5

4

3

2

1

MSIS-RMA
羅覓林
20091215