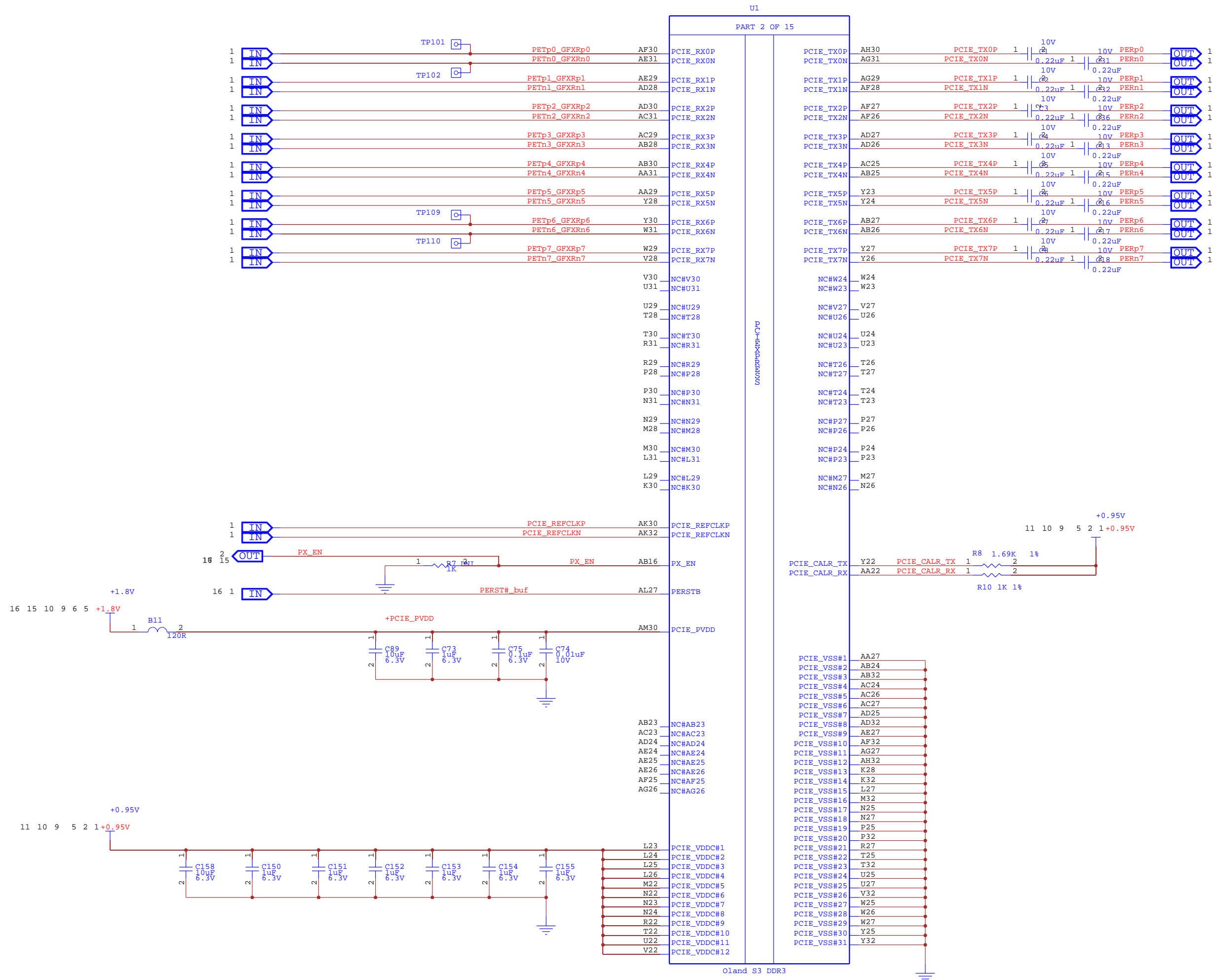


DOCUMENT NUMBER: 105_C553xx_00

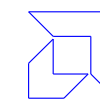
Yu Yuan

OLAND PCIe Interface

NOTE: Some of the PCIE testpoints will be available through vias on traces.



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SHEET: Oland PCIEx8 Interface

DATE: Tue Dec 03 11:30:02 2013

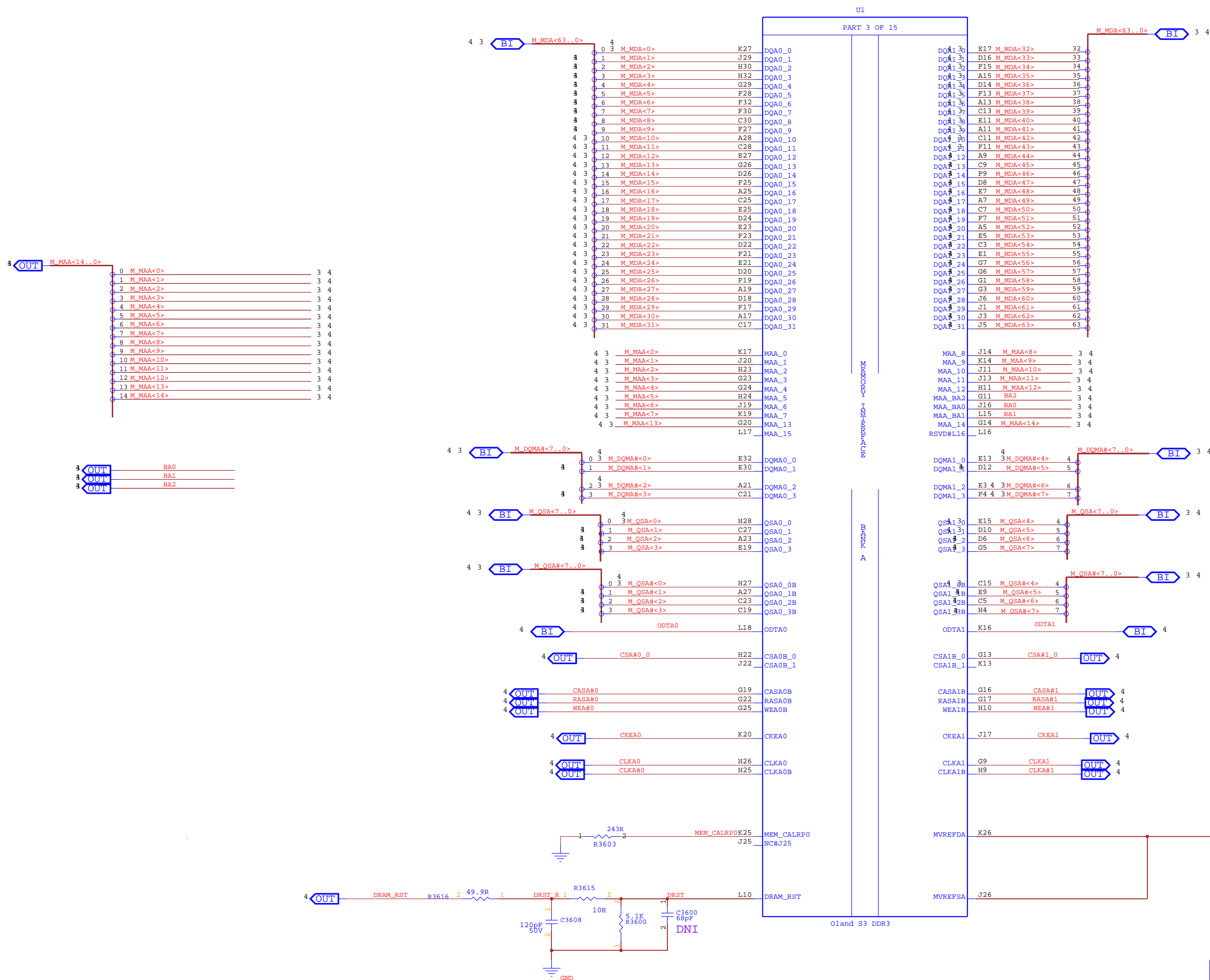
SHEET NUMBER: 2 OF 19

DOCUMENT NUMBER: 105_C553xx_00

TITLE:

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Oland S3 MEM Interface Ch A&B



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SHEET: Oland MEM I/F CHA

DATE: Tue Dec 03 11:30:02 2013

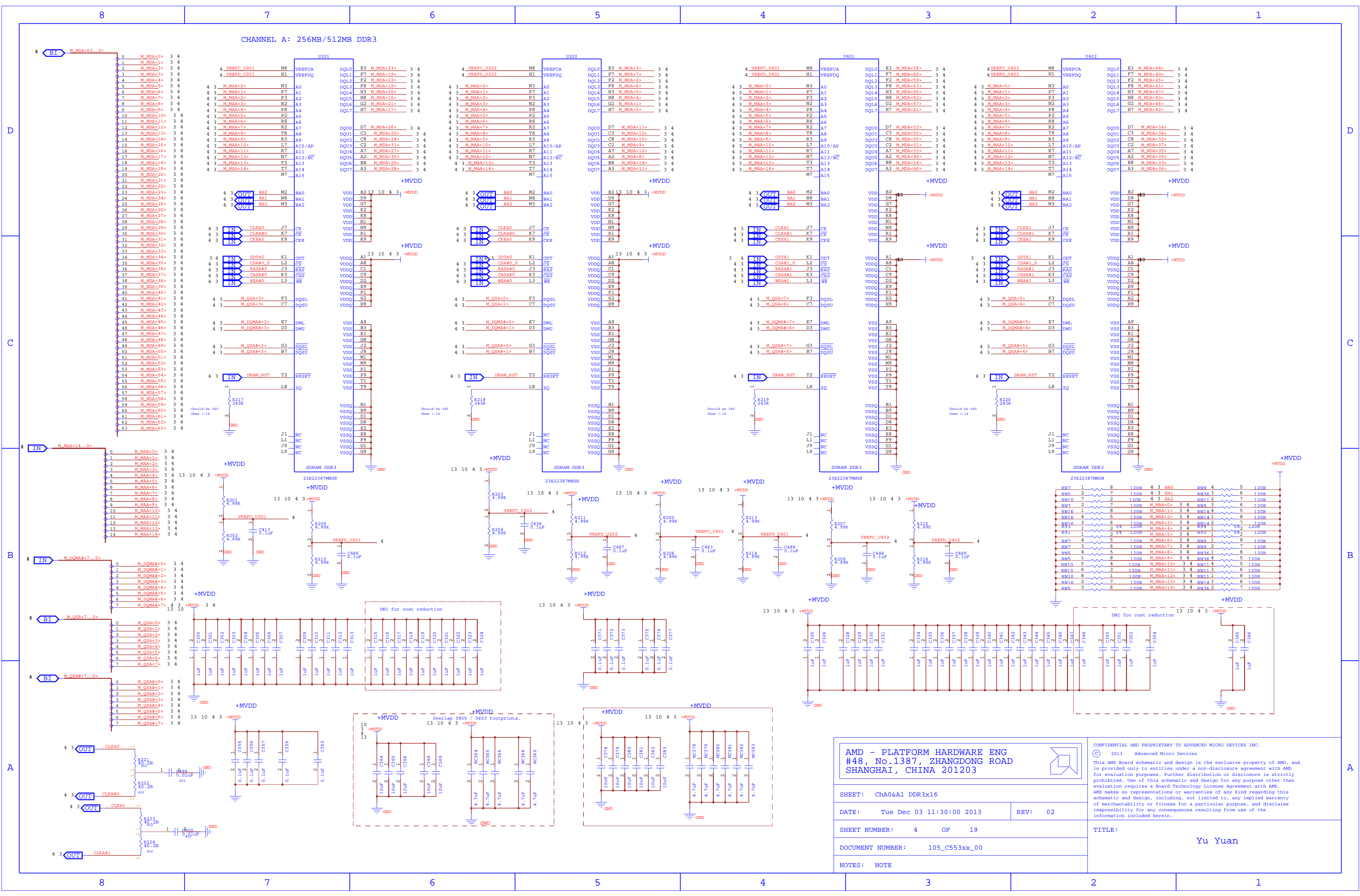
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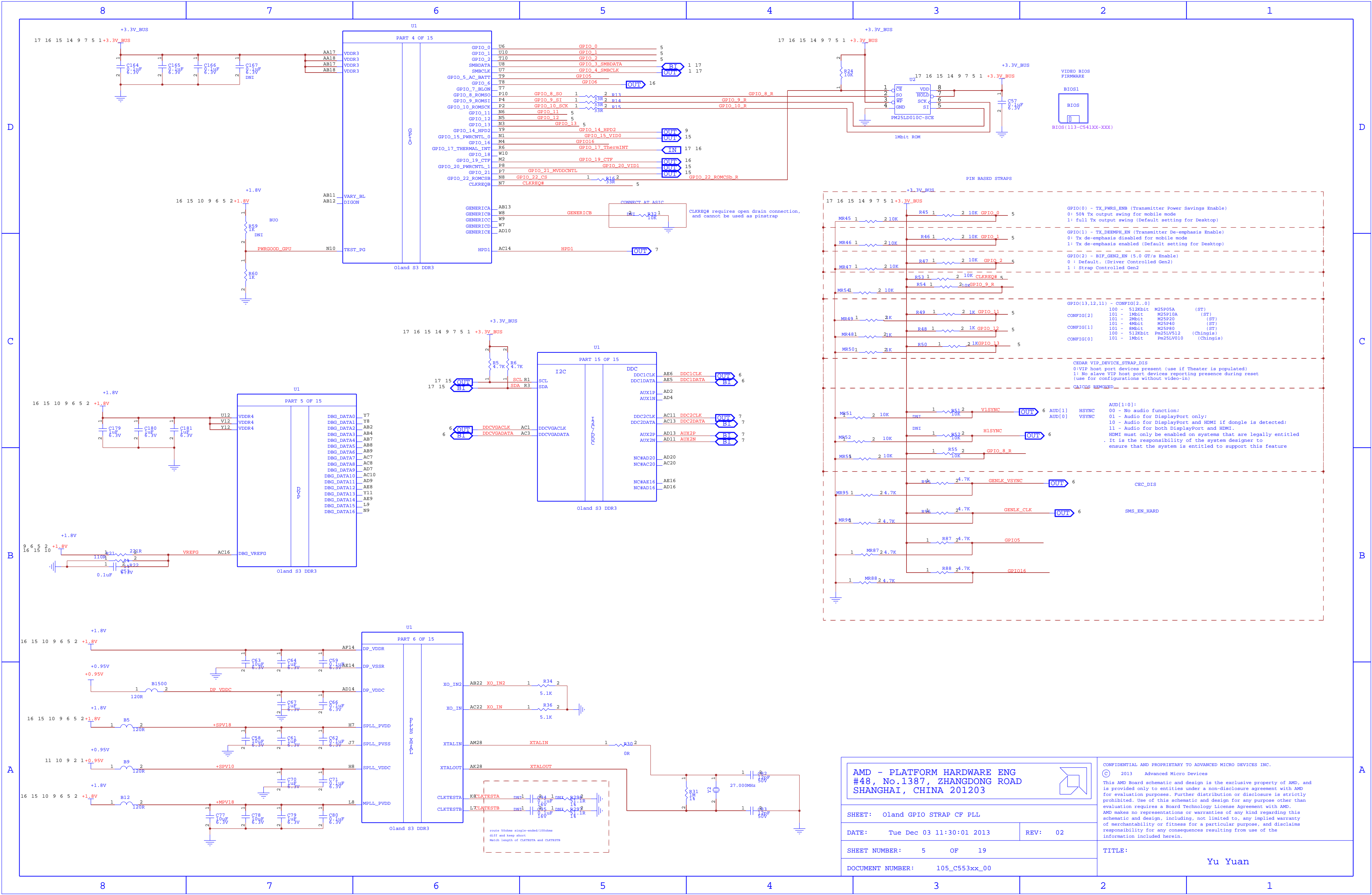
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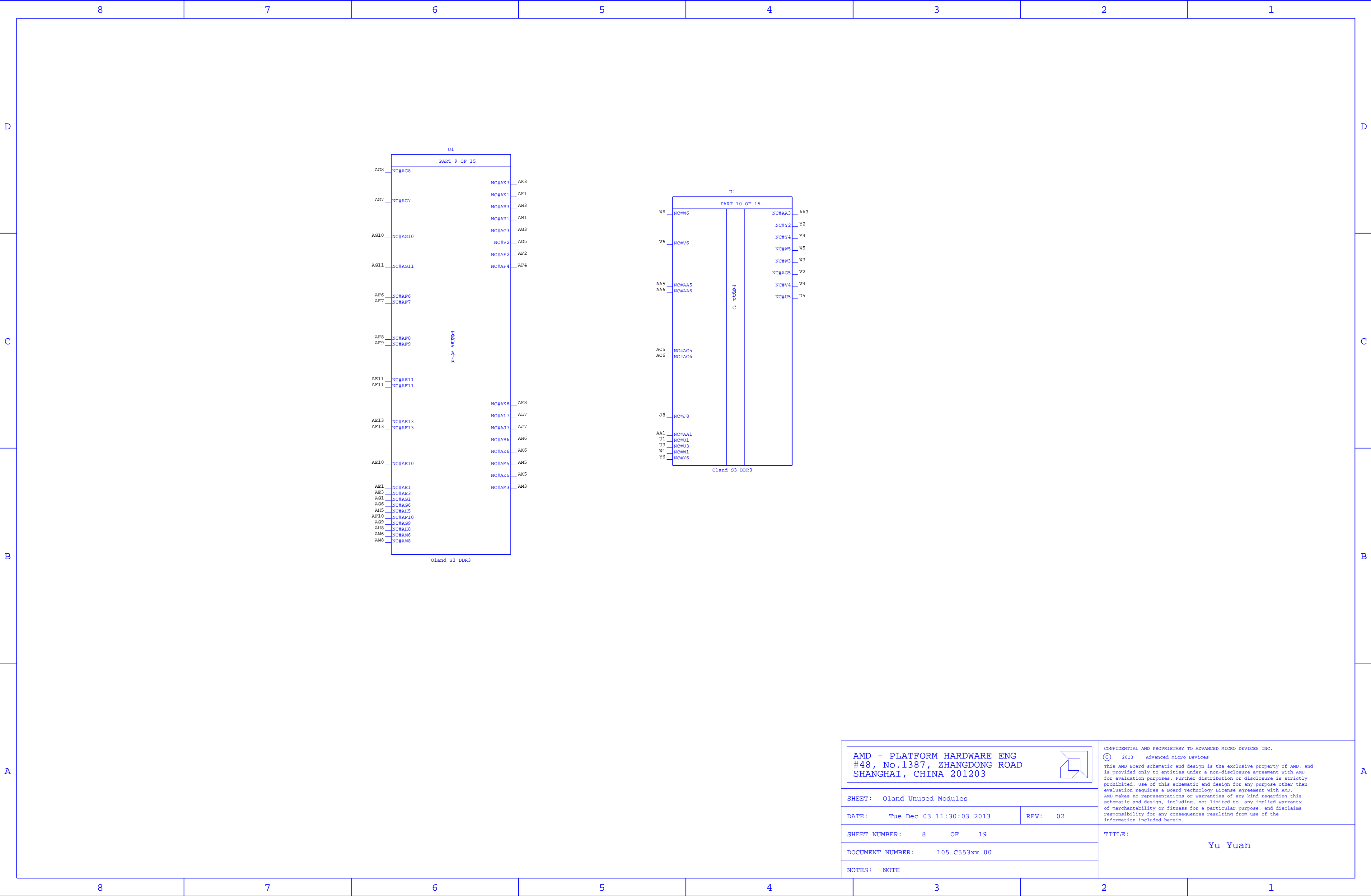
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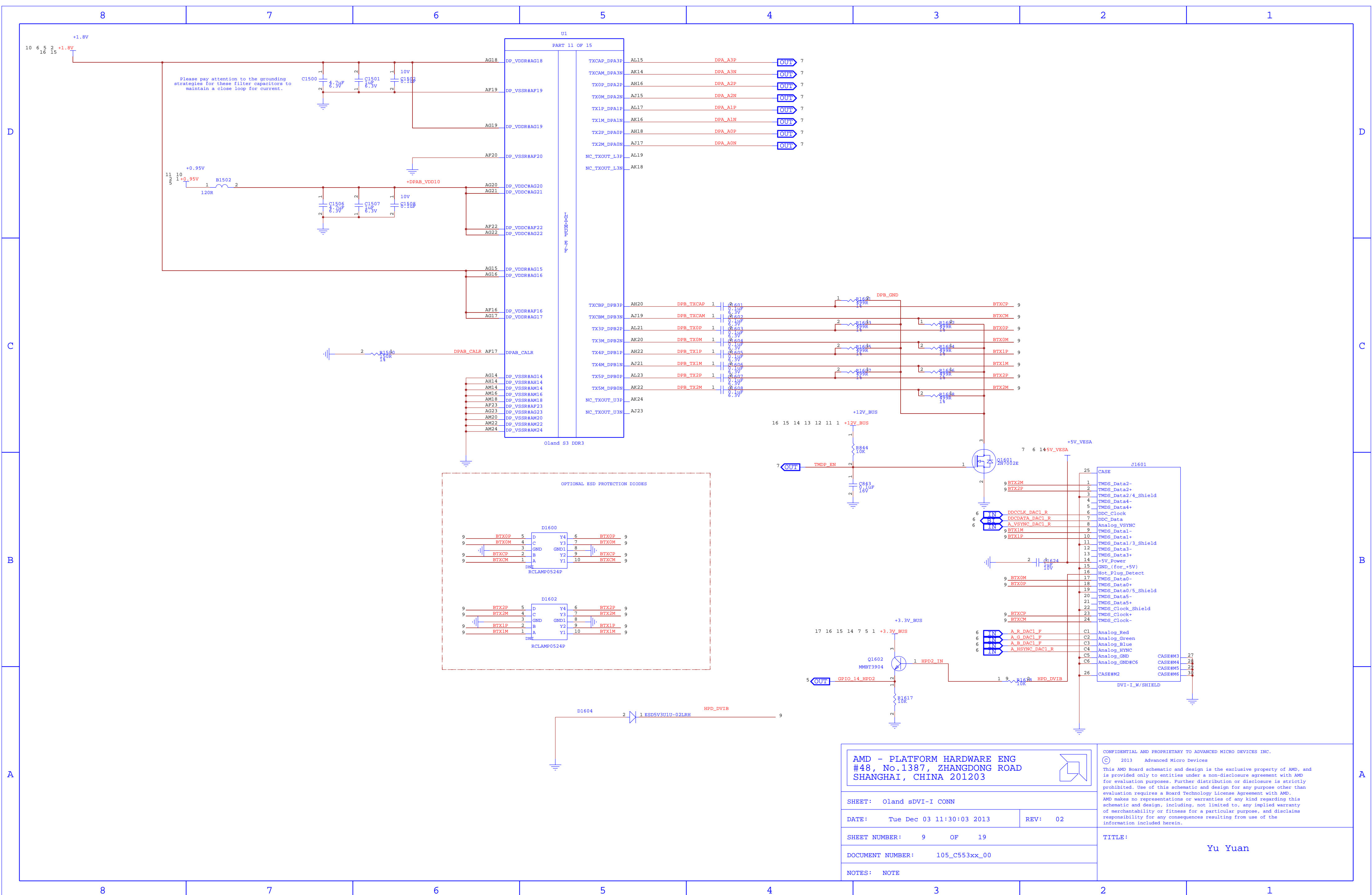
TITLE: Yu Yuan

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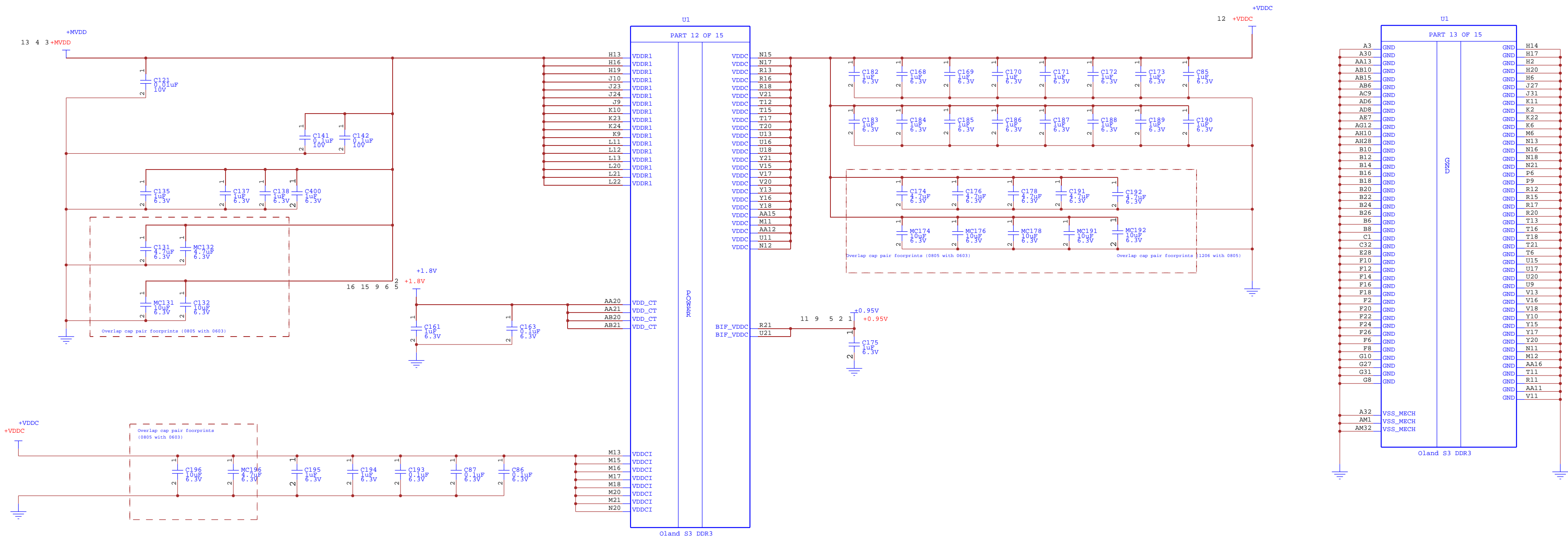








OLAND S3 Power & GND



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SHEET: Oland Power&GND

DATE: Tue Dec 03 11:30:03 2013

REV: 02

SHEET NUMBER: 10 OF 19

DOCUMENT NUMBER: 105_C553xx_00

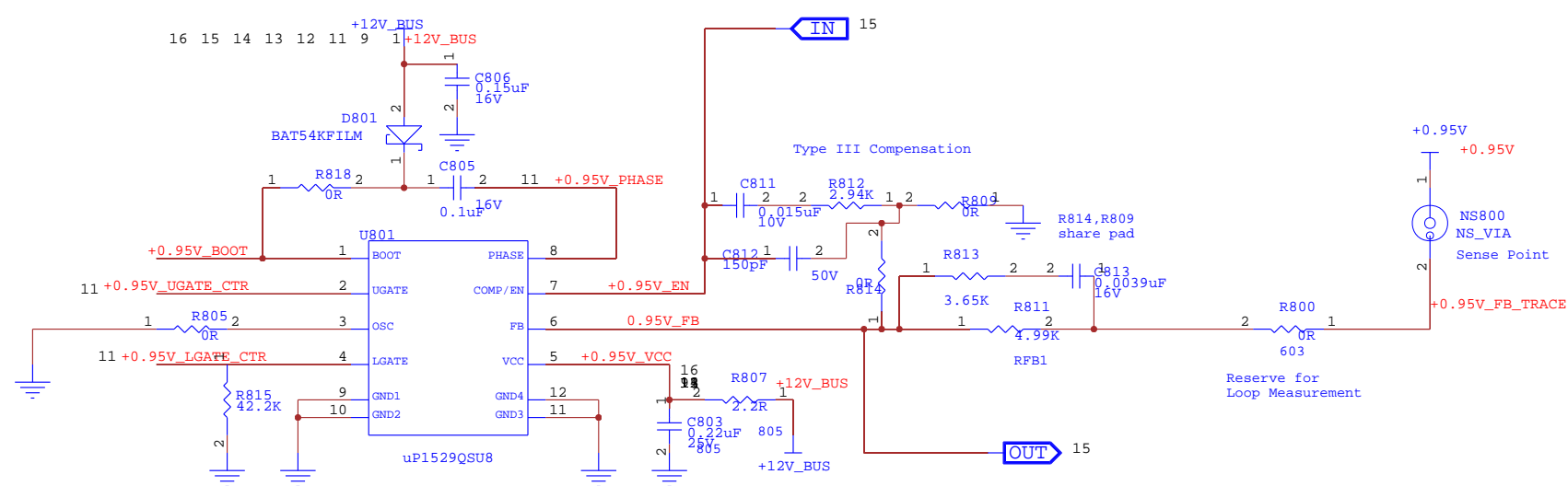
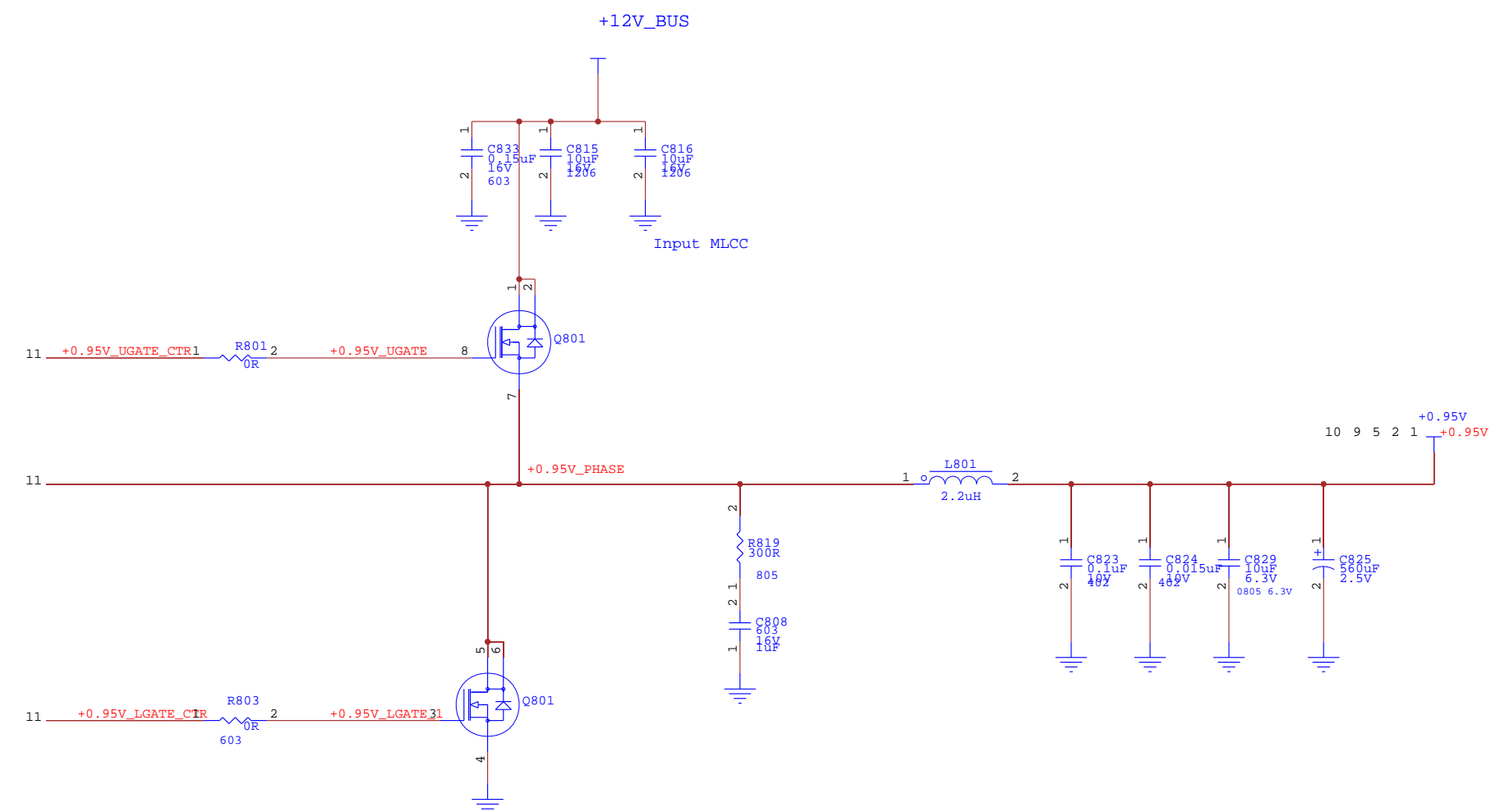
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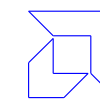
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SHEET: 0.95V

DATE: Tue Dec 03 11:30:02 2013

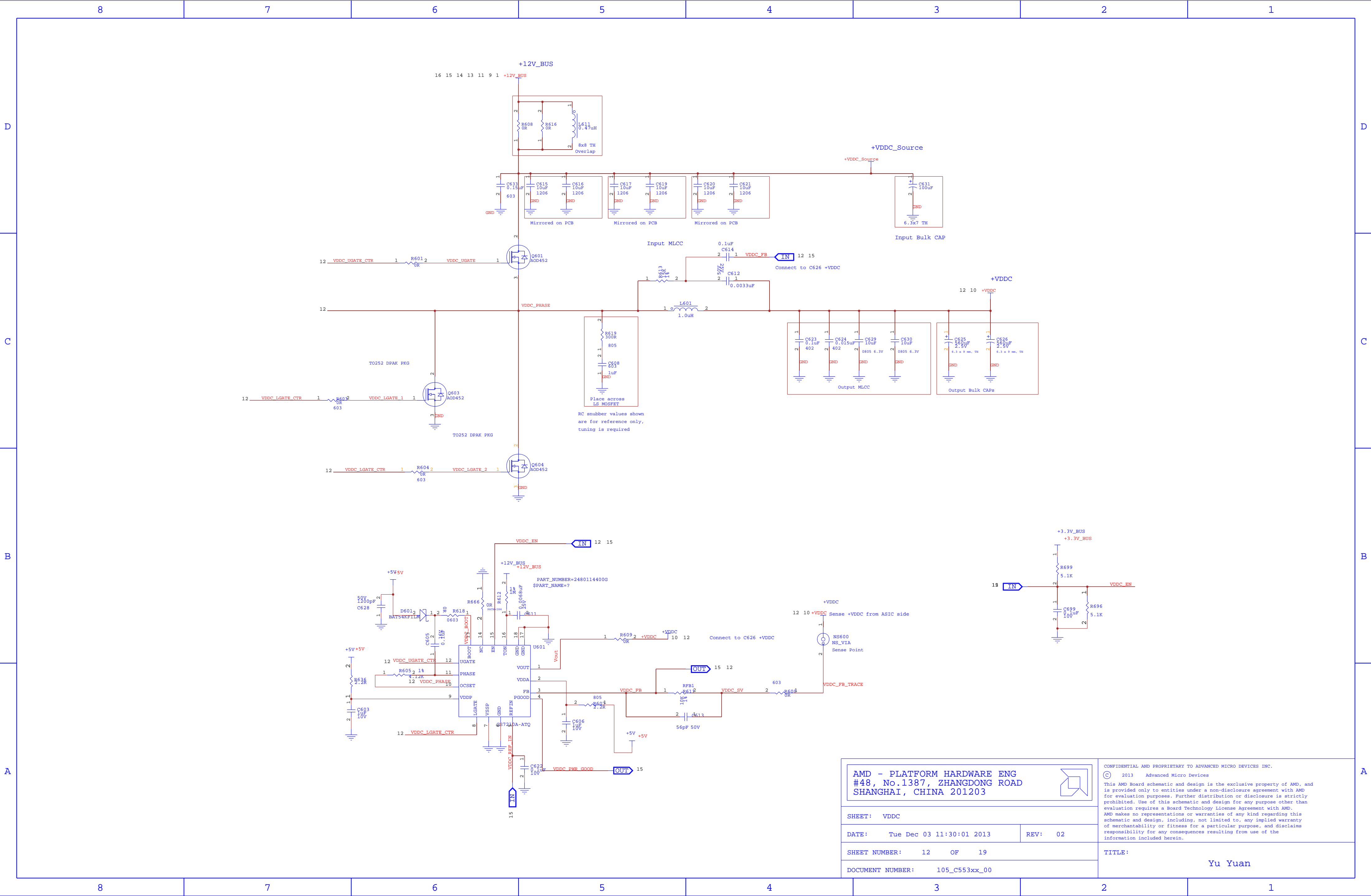
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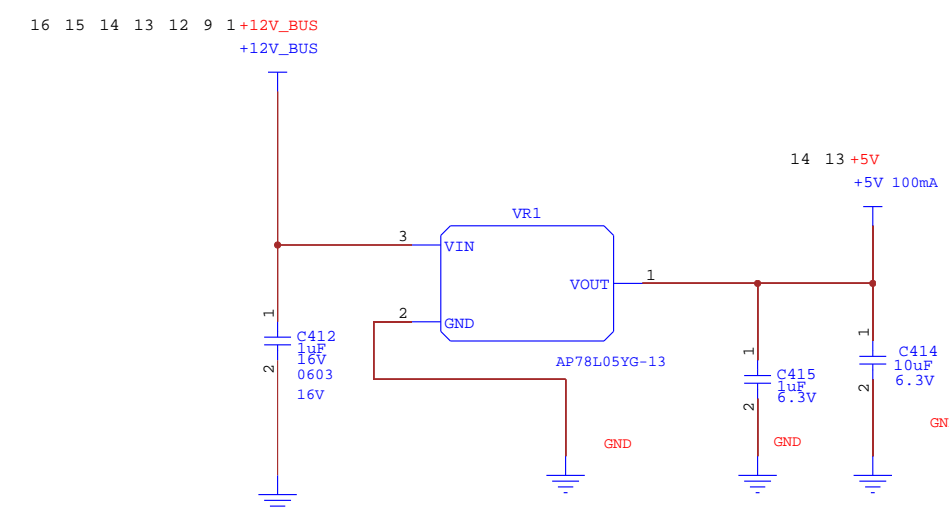
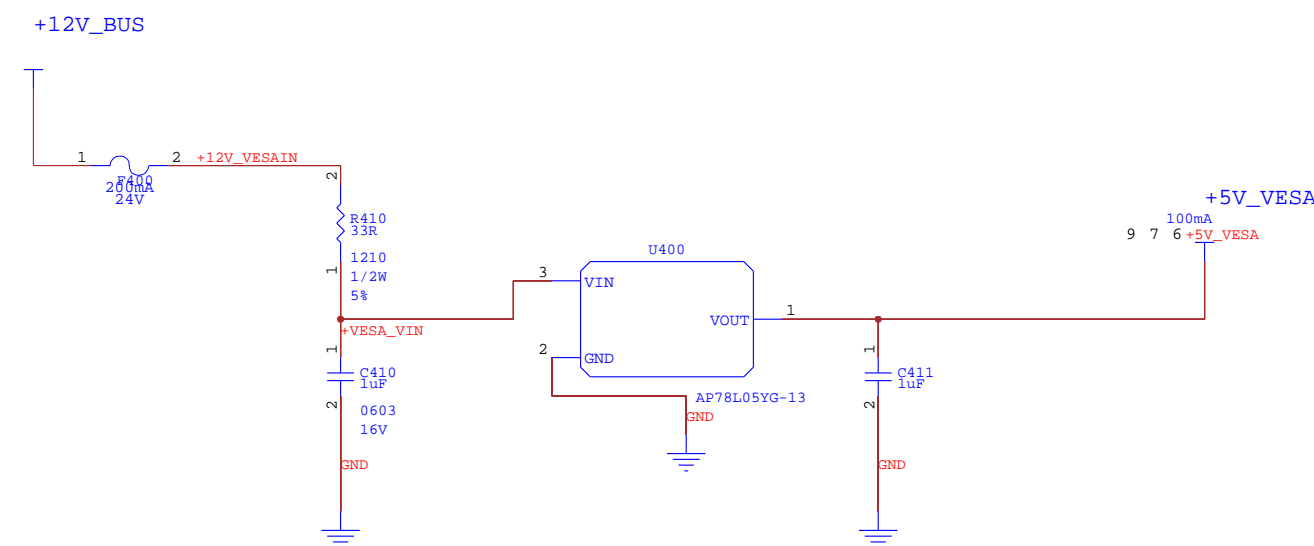
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Yu Yuan

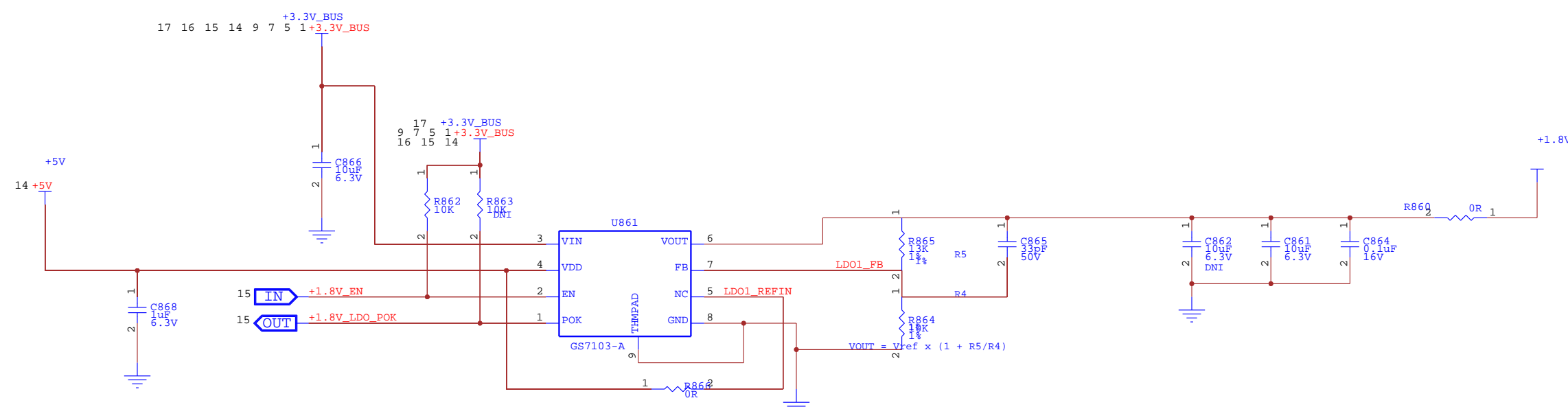




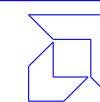
Linear Regulators

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



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SHEET: Linear Regulators

DATE: Tue Dec 03 11:30:01 2013

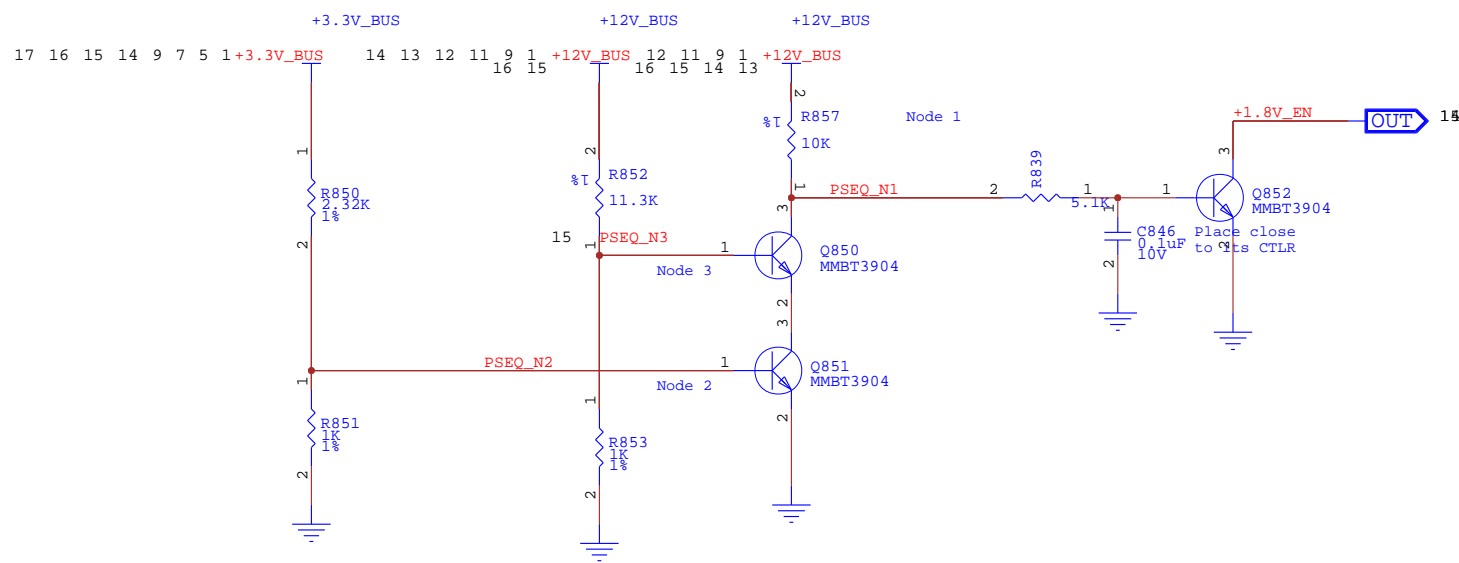
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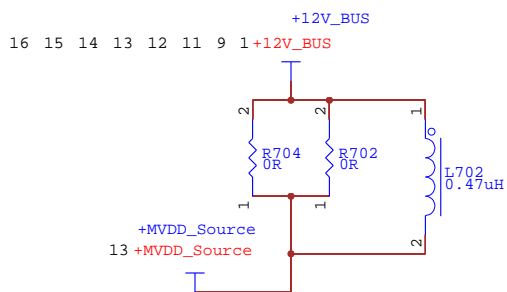
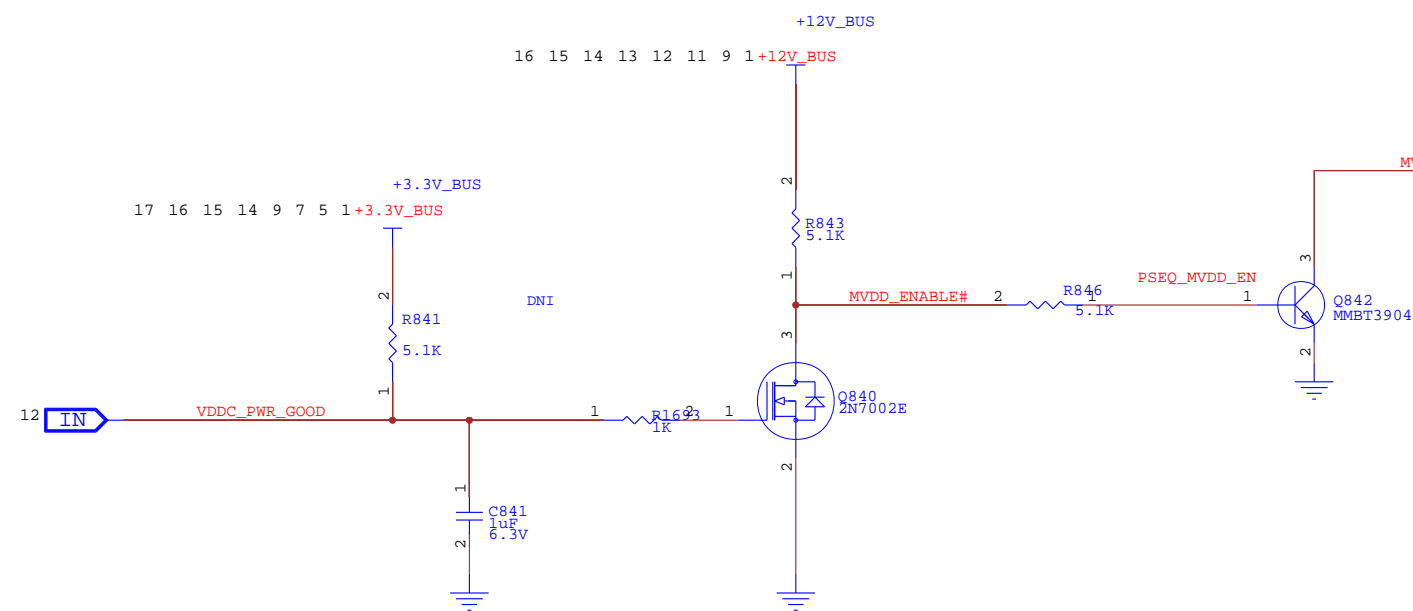
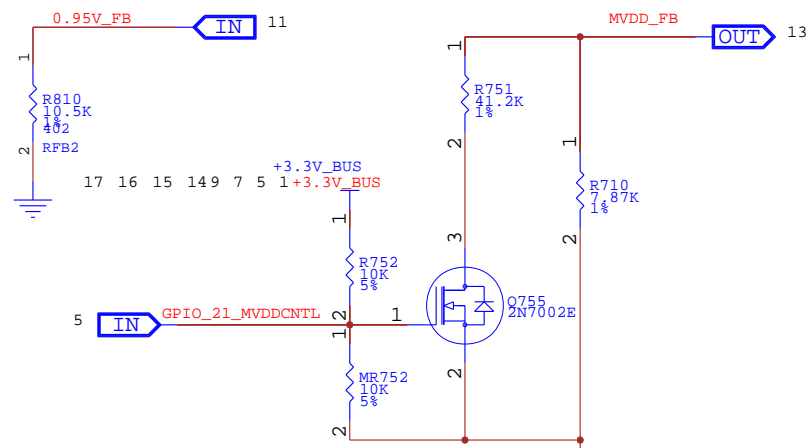
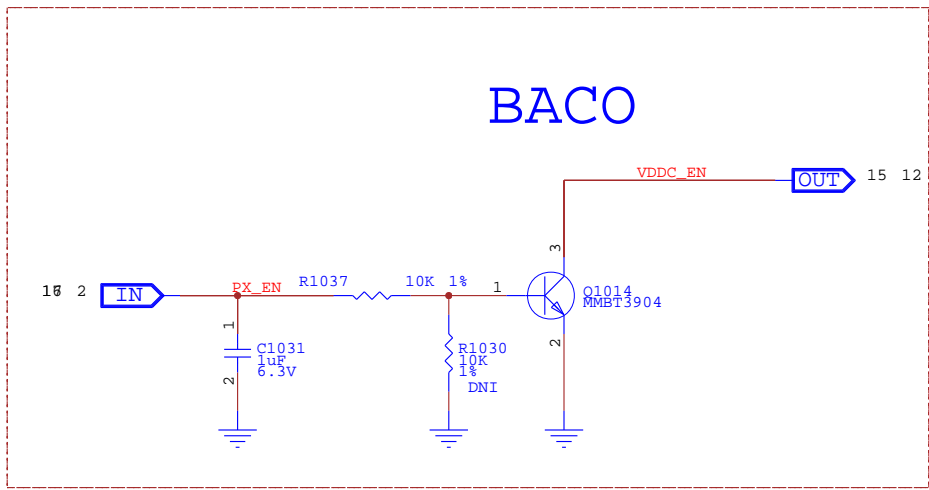
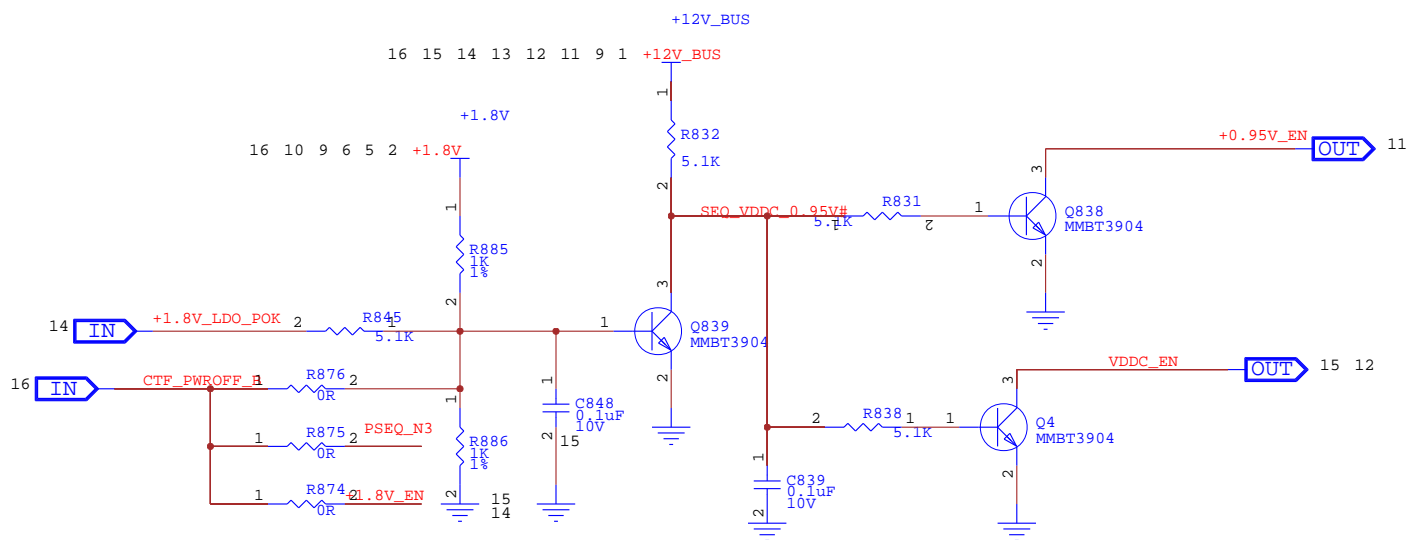
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Yu Yuan

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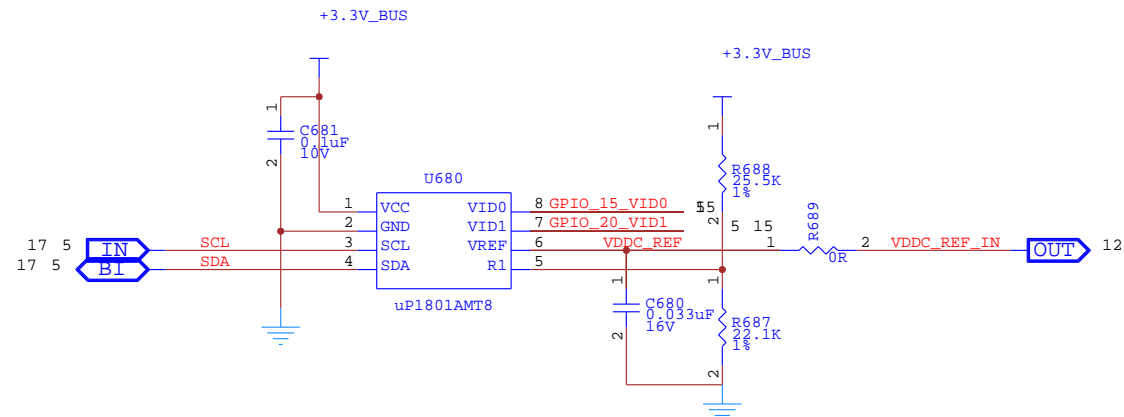


C



A

VDDC Low Side Divider

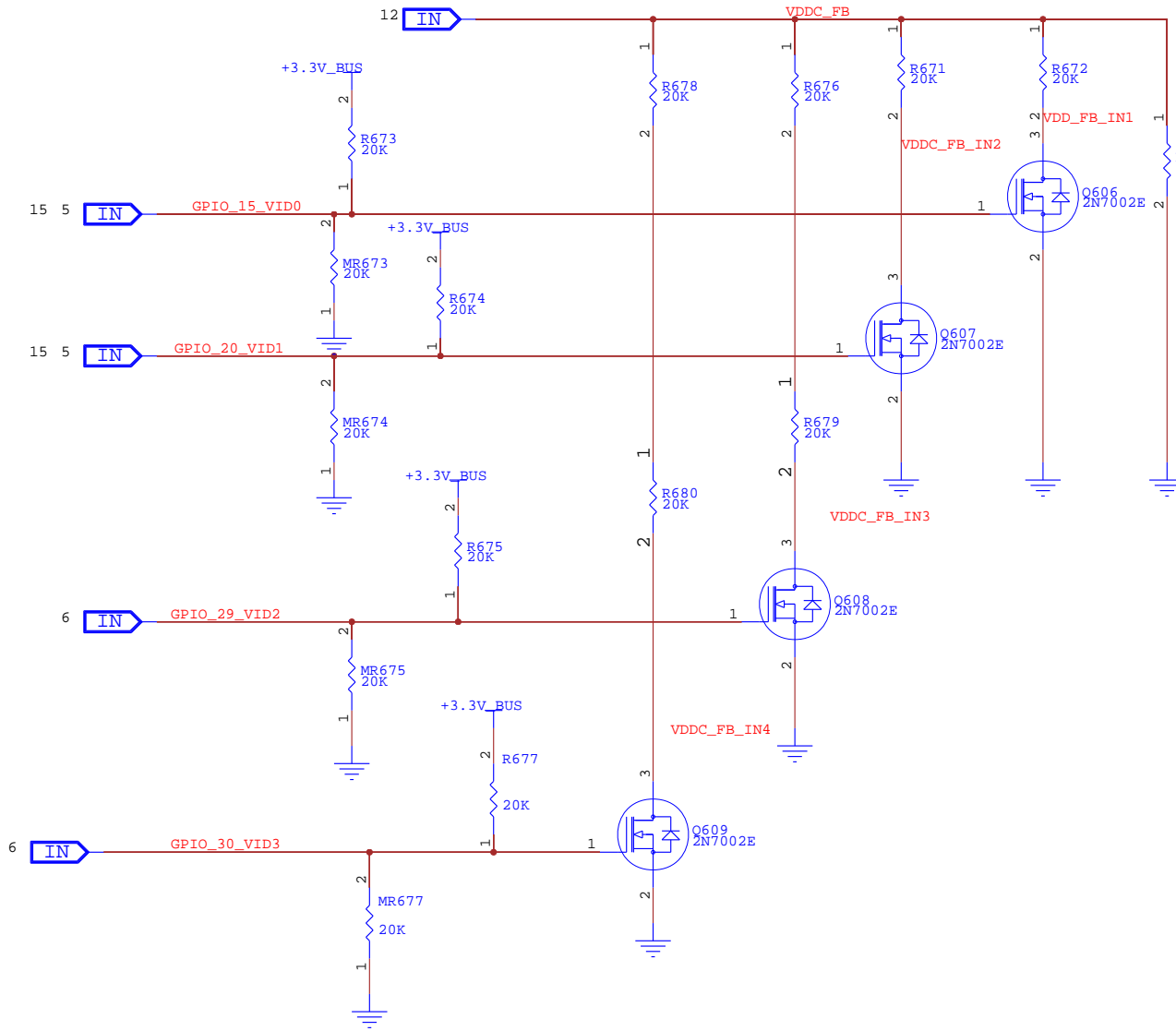


D

C

B

A



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SHEET: PWR SEQ

DATE: Tue Dec 03 11:30:02 2013

REV: 02

SHEET NUMBER: 15 OF 19

DOCUMENT NUMBER: 105_C553xx_00

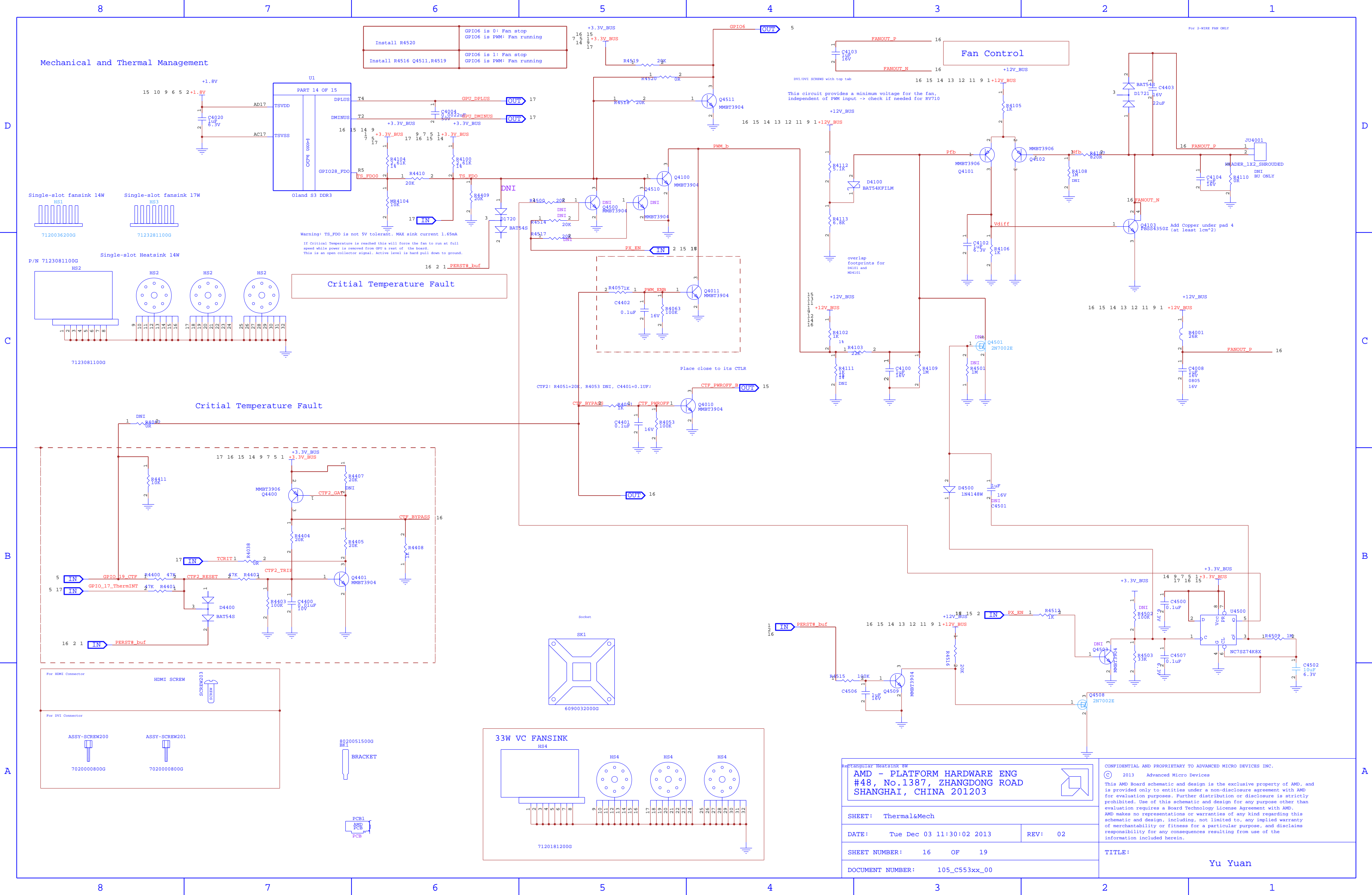
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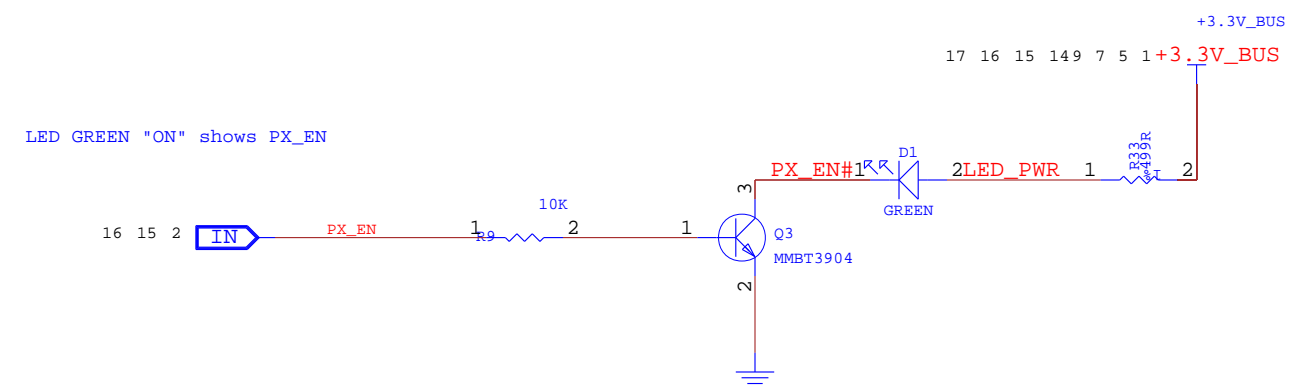
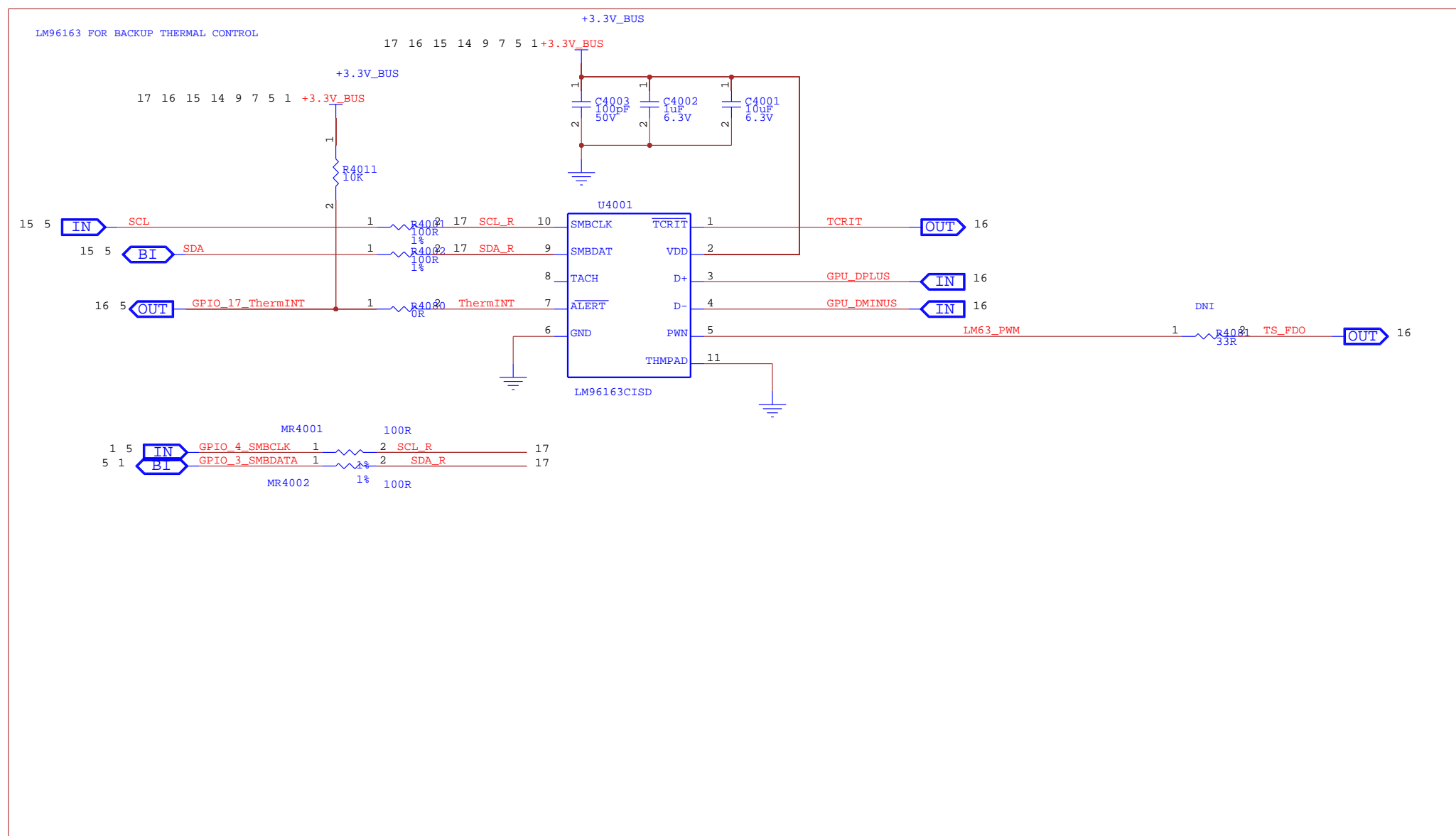
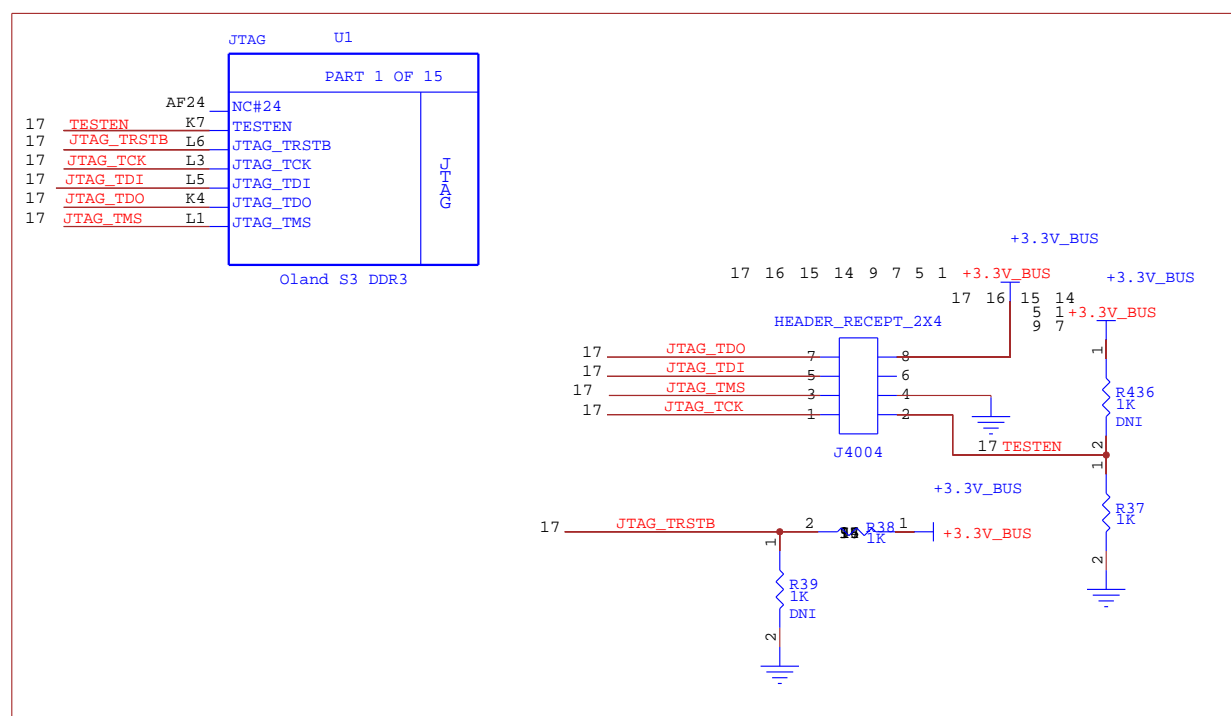
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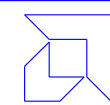
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(19) Debug Circuits



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SHEET: Debug

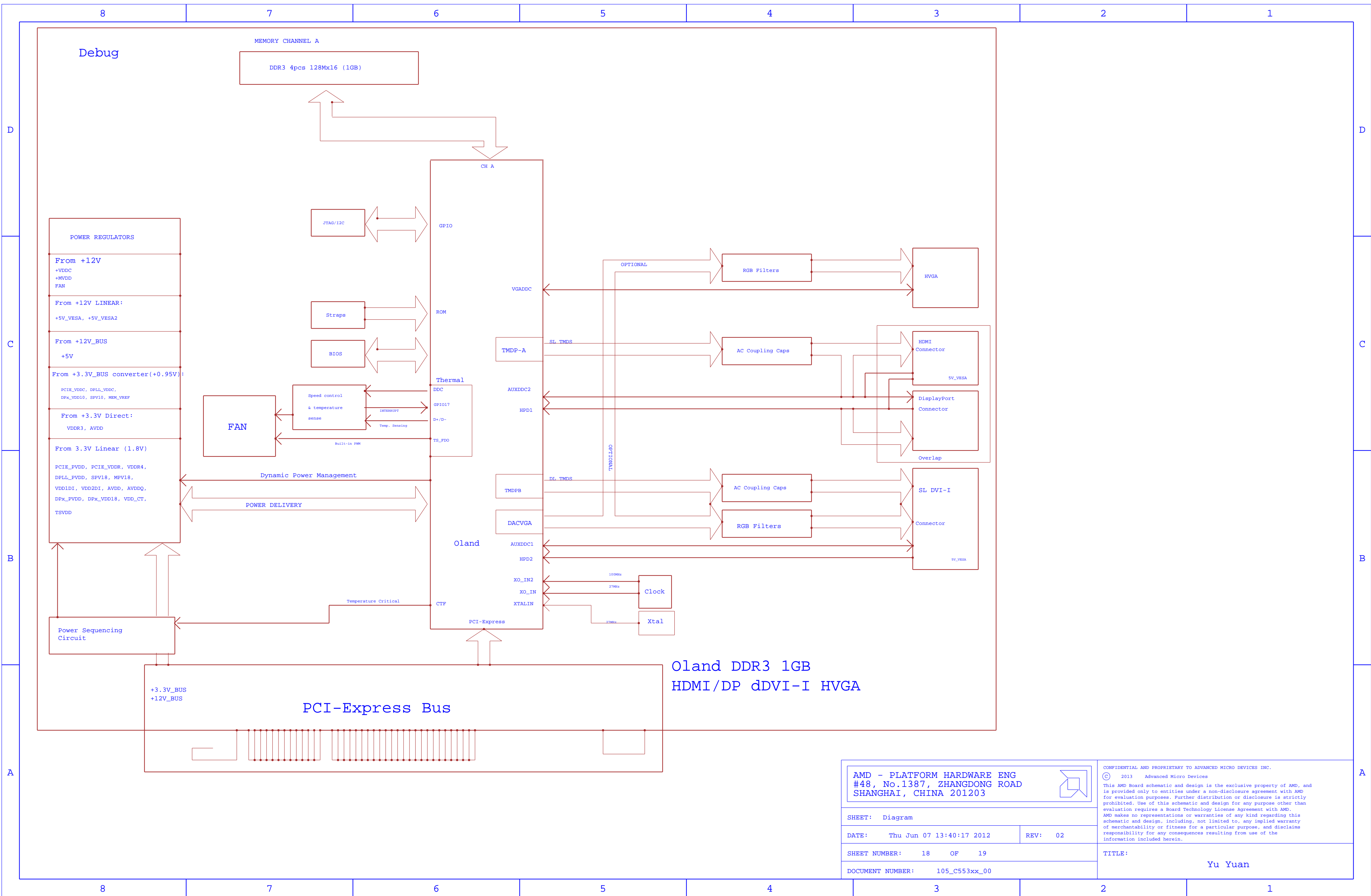
DATE: Tue Dec 03 11:30:02 2013

REV: 02

SHEET NUMBER: 17 OF 19

TITLE:

Yu Yuan



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D	<table><tr><td colspan="3"></td><td>TITLE</td><td>SCHEMATIC NO.</td><td colspan="3">DATE</td></tr><tr><td colspan="3"></td><td>Oland GDDR5 1GB sVGA+HDMI/DP+dDVI-I</td><td>105-C553XX-00</td><td colspan="3"></td></tr><tr><td colspan="3"></td><td>REVISION HISTORY</td><td>NOTE:</td><td colspan="2">REV</td></tr><tr><td colspan="3"></td><td></td><td>THIS SCHEMATIC REPRESENTS THE PCB. IT DOES NOT REPRESENT ANY SPECIFIC SKU. FOR STUFFING OPTIONS (COMPONENT VALUES, DNI PLEASE CONSULT THE PRODUCT SPECIFIC BOM. PLEASE CONTACT AMD REPRESENTATIVE TO OBTAIN LATEST BOM CLOSEST TO THE APPLICATION DESIRED.</td><td colspan="2">P02</td></tr><tr><td>SCH REV</td><td>PCB REV</td><td>DATE</td><td colspan="5">REVISION DESCRIPTION</td></tr><tr><td>00</td><td>00A</td><td>2012/01/12</td><td colspan="5">Initial Oland C553 schematic, based on C367XX-00A</td></tr><tr><td>01</td><td>00B</td><td>2013/04/23</td><td colspan="5">Removed PCIe redundant fingers to save cost, modify DDC1 for HDMI</td></tr><tr><td>02</td><td>00</td><td>2013/12/03</td><td colspan="5">change nothing base on 00B</td></tr><tr><td colspan="8"></td></tr></table>											TITLE	SCHEMATIC NO.	DATE						Oland GDDR5 1GB sVGA+HDMI/DP+dDVI-I	105-C553XX-00							REVISION HISTORY	NOTE:	REV						THIS SCHEMATIC REPRESENTS THE PCB. IT DOES NOT REPRESENT ANY SPECIFIC SKU. FOR STUFFING OPTIONS (COMPONENT VALUES, DNI PLEASE CONSULT THE PRODUCT SPECIFIC BOM. PLEASE CONTACT AMD REPRESENTATIVE TO OBTAIN LATEST BOM CLOSEST TO THE APPLICATION DESIRED.	P02		SCH REV	PCB REV	DATE	REVISION DESCRIPTION					00	00A	2012/01/12	Initial Oland C553 schematic, based on C367XX-00A					01	00B	2013/04/23	Removed PCIe redundant fingers to save cost, modify DDC1 for HDMI					02	00	2013/12/03	change nothing base on 00B													D
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DATE: Tue Dec 03 11:29:02 2013REV: 02

SHEET NUMBER: 19 OF 19

DOCUMENT NUMBER: 105_C553xx_00

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