電子類元件 零件承認書文件 CHECK LIST

零件廠商：ON Semiconductor **品名規格：BUS SWI IC NCP45491XMNTWG ON**

技嘉料號：10TA1-084549-00R

項次	文件項目
	Data Sheet 檢核項目
1	DATASHEET (含機構尺寸、**端子腳鍍層材質**、**MSL Report**)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2**
8	零件樣品 20PCS(Chipset 等高單價，至少 1PCS)
9	**電子零件承認基本調查表。註 3**
10	以上資料電子檔為 PDF 檔，且是同 1 個 File
	GSCM 綠色產品管理系統-物料管制文件檢核清單
物料管制文件 1	GSCM 綠色產品管理系統：零件照片
物料管制文件 2	GSCM 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4**
物料管制文件 3	GSCM 綠色產品管理系統：Data Sheet
	GSCM 綠色產品管理系統-MCD 表格
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
	其他文件 (僅適用電阻、電容類之系列元件)
附件 1	危害物質測試報告 Test Report of Hazardous Substances。**註 5**
附件 2	元件調查表 Component Composition Table

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等

※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)

2.1. 基本需符合 JEDEC 規範

2.2. Ambient Temp. (Reflow Temp endurace): >225℃, 70 sec. 零件塑膠材質需 PA9T(含)等級以上

2.3. PASTE IN HOLE 零件塑膠材質需 PA9T(含)等級以上

※ **3. 電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G*,11T***

非 IC 類：10C*,11C*,10L*,11L*,10X*,11X*,10R*,11B*

※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”

※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

電子零件承認基本調查表

一、原物料規格/來源			
項次	部位名稱/規格	材質	原物料來源產地
1	Die	Wafer	ON-Thailand
2	Die Attach	Adhesives	ON-Thailand
3	Lead Frame	Metal	ON-Thailand
4	Mold Compound-Black	Epoxy Resin	ON-Thailand
5	Plating	Metal Plating Layer	ON-Thailand
6	Wire Bond - Cu	Metal	ON-Thailand

二、晶圓廠(非 IC 類免填)					
項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	ON Semiconductor	Thailand			

三、封裝廠(IC 類)；成品之生產製造工廠(非 IC 類)				
項次	工廠名稱	生產產地	投產比率(%)	自有/外包
1	ON Semiconductor	Thailand		
2				
3				

四、產能	
總產能(月/PCS)	可供技嘉產能(月/PCS)

※ 1. IC 類之晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動（包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 2. 非 IC 類零件之成品生產製造工廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動（包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 3. 以上資訊欄位若有不足，可自行增加行數

文曄科技
WT MICROELECTRONICS
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14F., NO.738,CHUNG CHENG ROAD ., CHUNG HO CITY ,
TAIPEI HSIEN, TAIWAN, R.O.C
TEL:(02)8226-9088 FAX:(02)8226-9099

承 認 書
APPROVAL SHEET

□	送測日期 ： TEST DATE	31-Jul-18
□	客戶名稱 ： CUSTOMER	技嘉科技股份有限公司
□	品 名 ： PART NAME	**NCP45491XMNTWG** **10TA1-084549-00R**
□	廠 牌 ： BRAND	**ON**
□	包 裝 ： PACKAGE	**QFN32**
□	承認日期 ： APPROVED DATE	31-Jul-18

NCP45491

26V, 4-Channel Voltage Bus and 4-Channel High-Side Current Shunt Monitor

The NCP45491 is a high−performance monolithic IC which can be used to monitor bus voltage and current on four high−voltage power supplies simultaneously. The HV bus voltages and currents are translated to a low−voltage power domain and multiplexed onto a single differential output for measurement externally by common ADCs. The device is configurable to operate either standalone or as a pair, permitting up to eight separate HV power supplies to be monitored and measured.

Features

- Translates and Scales Shunt and Bus Voltages up to 26 V
- Single Device Monitors Four Supplies
- May Be Paired for Monitoring Up To Eight Supplies
- Very Low Powerdown Current
- All Channels Individually Gain Programmable by External Resistor Selection
- Fast Settling Time
- Real−Time Indication of All Bus Voltages Valid
- Adjustable Output Common−Mode Voltage Adapts to Most External ADCs
- Lead−Free Device

Applications

- Computers/Notebooks
- Graphical Cards
- Power Management/Power Control Loops
- Battery Chargers

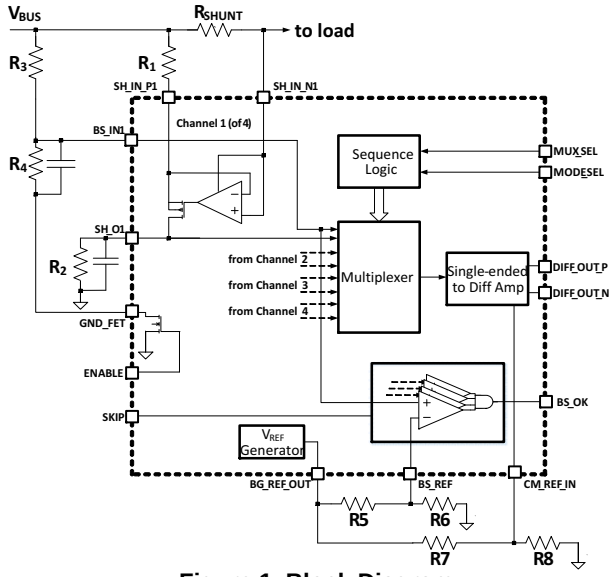

Figure 1. Block Diagram

ON Semiconductor™

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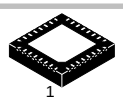
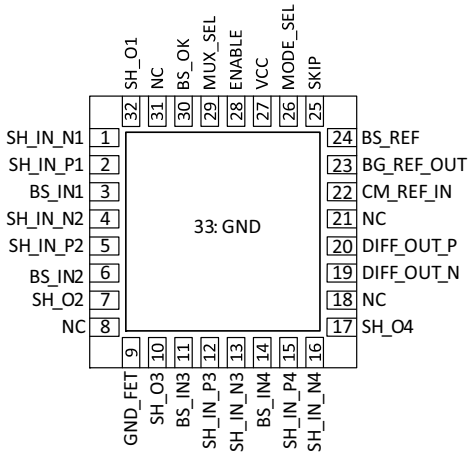


QFN32 4x4
CASE 485CD

MARKING DIAGRAM

45491 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
CCCCC = Country of Assembly

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP45491XMNTWG	QFN32 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Function
2, 5, 12, 15	SH_IN_Px	AI	Shunt Resistor Sense +, High Voltage
1, 4, 13, 16	SH_IN_Nx	AI	Shunt Resistor Sense −, High Voltage
32, 7, 10, 17	SH_Ox	AO	Shunt Voltage Gain Set / Filter, Current Output
3, 6, 11, 14	BS_INx	AI	Bus Voltage Sense, High Impedance Input
20	DIFF_OUT_P	AO	Differential Output, Positive
19	DIFF_OUT_N	AO	Differential Output, Negative
22	CM_REF_IN	AI	Common−Mode Reference for Differential Output
29	MUX_SEL	DI	Multiplexer Select Input
24	BS_REF	AI	Bus OK Reference Input
30	BS_OK	DO	Bus OK output (open−drain; high impedance = BUS OK)
28	ENABLE	DI	Device Enable. When low, places device in low−power state
23	BG_REF_OUT	AO	Buffered Bandgap Voltage Output
9	GND_FET	AO	Low−side GND ref for resistor dividers (open drain type)
25	SKIP	DI	Skip Function control (see description)
26	MODE_SEL	AI	Multi−level Input for single−device, device A, or device B modes
8, 18, 21,31	NC		Pins must be floated
27	VCC	PWR	Device Power
PAD	GND	GND	Device Ground

Table 2. MAXIMUM RATINGS

Rating	Pins	Condition	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	GND = 0 V	V_{CC}	−0.3 to 5.5	V
Shunt Input Voltage Range	SH_IN_Px, SH_IN_Nx	GND = 0 V	$V_{SH\_IN\_X}$	−0.3 to 30	V
Bus Input Voltage Range	BS_INx	GND = 0 V	V_{BS_IN}	−0.3 to 30	V
Grounding FET Range	GND_FET	GND = 0 V	V_{GND_FET}	−0.3 to 30	V
Shunt Output Voltage Range	SH_Ox	GND = 0 V	V_{SH_Ox}	−0.3 to 5.5	V
Digital Input Voltage Range	MUX_SEL, ENABLE, SKIP, MODE_SEL	GND = 0 V	V_{EN}	−0.3 to 5.5	V
Low Voltage I/O Range	BS_REF, CM_REF_IN, MODE_SEL, DIFF_OUT_P, DIFF_OUT_N, BS_OK, BG_REF_OUT	GND = 0 V	V_{LV}	−0.3 to 5.5	V
Thermal Resistance, Junction−to−Air			$R_{\theta JA}$	40	°C/W
Thermal Resistance, Junction−to−Case (V_{IN} Paddle)			$R_{\theta JC}$	5	°C/W
Operating Temperature Range			T_{A1}	−40 to 105	°C
Functional Temperature Range			T_{A2}	−40 to 125	°C
Maximum Junction Temperature			T_J	125	°C
Storage Temperature Range			T_{STG}	−40 to 150	°C
Lead Temperature, Soldering (10 sec.)			T_{SLD}	260	°C
Moisture Sensitivity Level			MSL	1	−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. ESD RATINGS

Rating	Symbol	Value	Unit
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	>2.0	kV
ESD Capability, Charged Device Model (Note 1)	ESD_{CDM}	>0.5	kV
Latch−up Immunity (Note 1)	I_{LU}	100	mA

1. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114).
   ESD Charged Device Model per JESD22−C101.
   Latch−up testing per JEDEC78E.

Table 4. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage Range	V_{CC}	2.8	3.8	V
Shunt Input Voltage Range	$V_{SH\_IN\_X}$	5	26	V
Shunt Output Voltage Range (operating)	V_{SH_Ox}	0	0.5	V
Shunt Output Voltage Range (floating)	V_{SH_Ox}	2.8	3.8	V
Bus Input Pin Voltage Range (Standby Mode)	V_{BS_INX}	0	26	V
Bus Input Pin Voltage Range (Full Function or Limited Function Mode)	V_{BS_INX}	0	0.5	V
Grounding FET Range	V_{GND_FET}	0	26	V
Low Voltage I/O Range	V_{LV}	0	3.8	V
Ambient Temperature	T_A	−40	85	°C
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. AC CHARACTERISTICS ($V_{SH\_IN\_X}$ = 15 V, V_{EN} = 0 V, V_{CC} = 3.3 V, unless indicated otherwise. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +105°C unless noted otherwise and are guaranteed by test, design, characterization, or statistical correlation. Typical values are referenced to T_J = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Multiplexer Settling Time (to 9.375 mV)	T_{STAB1}			100	ns
Multiplexer Settling Time (to 3.125 mV)	T_{STAB2}			300	ns
MUX_SEL Period (normal operation)	T_{MSP}	0.185		11	μs
MUX_SEL Reset Period	T_{RP}	35			μs
Power−up Time (STANDBY or Limited Function to Full Function)	T_{PWR_UP}			40	μs
Differential Amplifier Capacitive Load Capability (Note 2)	C_{DIFF}			82	pF

2. Differential Output C_{LOAD} (i.e.: DIFF_OUT_x to GND) appears as a series RC with lumped equivalent R (0.86−8.6 Ω) and C (8.2−82 pF).

Table 6. DC CHARACTERISTICS ($V_{SH\_IN\_X}$ = 15 V, V_{EN} = 0 V, V_{CC} = 3.3 V, unless indicated otherwise. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +105°C unless noted otherwise and are guaranteed by test, design, characterization, or statistical correlation. Typical values are referenced to T_J = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
MUX_SEL, SKIP, MODE_SEL, ENABLE Logic High	V_{IH}	1.4			V
MUX_SEL, SKIP, MODE_SEL, ENABLE Logic Low	V_{IL}			0.4	V
Input Impedance (MODE_SEL, ENABLE pins)	R_{FLOAT}	100k			Ω
SH_O Pin Current Source Capability	$I_{SH\_O\_MAX}$			5	mA
Fixed Current for Detection of SH_Ox Open	I_{SH_LEAK}			1	μA
GND_FET ON Resistance (measured @ 1 mA)	R_{GND_FET}			10	Ω
BG_REF_OUT Voltage	V_{BG}	1.274	1.3	1.326	V
BG_REF_OUT Load	IV_{BG_OUT}			100	μA
BS_OK Logic Low Impedance	R_{BS_OK}			300	Ω
VCC range for BS_OK low impedance	V_{LI}	1		3.8	V
VCC Threshold Reference for BS_OK Input (POR) (Note 3)	V_{BS_TH}	2.6		2.8	V
Shunt Monitor Offset Voltage (Note 4)	V_{SM_OV}			±150	μV
Shunt Monitor Offset Voltage Drift (Note 4)	SM_VD			2	μV/°C
Shunt Monitor CMRR ($V_{SH\_IN\_Px}$ in valid range, see above) (Note 5)	SM_CMRR	80			dB
Valid SH_O resistance	R_{SH_O}			2000	Ω
Differential Amp Input Offset Voltage, room temperature (Note 6)	V_{D_OVRT}			±2	mV
Differential Amp Input Offset Voltage Drift, −40°C to +105°C (Note 6)	V_{D_OVT}			±6	mV
Differential Amp PSRR (V_{CC} = 2.8 V to 3.8 V)	DA_PSRR	60			dB
Differential Amp Common−Mode Voltage	V_{CMRR}	565		885	mV
Differential Amp Closed Loop Gain	G_{DA}		2		V/V
Differential Full Scale Output	V_{FSO}			800	mV_{pp}
I_VCC (Fully Functional, V_{EN} = 0)	I_{VCC_F}			1.5	mA
I_VCC (Limited Function, V_{EN} = 0)	I_{VCC_L}			400	μA
I_VCC (STANDBY) (Note 7)	I_{VCC_S}			180	μA
I_SHO (STANDBY, non−floated SH_Ox pin) (Note 7)	I_{SHO_S}			100	μA
I_SH_IN_N (VBUS current in Full Function)	I_{VBUS}			300	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Vcc detection for BS_OK must trip in this range. Device can be either operational or not operational in this range.
4. Shunt Monitor Offset Voltage and Offset Voltage Drift are referred to the SH_IN_Px and SH_IN_Nx pins.
5. Input Offset voltage at T_J = 25°C.
6. Differential Amplifier Offset Voltage and Offset Voltage Drift are referred to the multiplexer input pins (e.g. BS_INx or SH_Ox).
7. V_{EN} = V_{CC}; Total V_{CC} standby current is I_{VCC_S} plus an additional I_{SHO_S} for every SH_Ox channel that is not floating.

APPLICATIONS INFORMATION

Differential Output Amplifier

A differential output amplifier provides a scaled representation of multiple bus voltages and currents to an external device on the DIFF_OUT_P and DIFF_OUT_N pins. These voltages and currents are presented *sequentially* (under control of the Sequence Logic block) via the Multiplexer. The common−mode voltage of the differential output amplifier is established by the voltage on the CM_REF_IN pin.

Current Shunt Monitor (one of four identical instances)

The differential voltage across an external shunt resistor (R_{SHUNT}) is converted to a current by a transconductor stage implemented by an op−amp and external resistor R1. This current is supplied to the SH_Ox pin where it is converted back to a ground−referenced voltage by external resistor R2. The conversion gain from differential voltage across the shunt resistor to that ground−referred voltage on SH_Ox may then be set directly as the ratio of R_{SHUNT} to R1. A capacitor may be connected across R2 in order to provide noise filtering if required in the application. Note that bias current for the op−amp is taken from the "load" side of the shunt resistor so that it is included in the load current measurement.

Current Shunt Resistors

The external resistors labeled R_{SHUNT}, R1, and R2 in Figure 1 are used to define the full dynamic range of the shunt current monitoring and are user application dependent. Resistors R_{SHUNT} and R1 are chosen based on the maximum load current (I_{LOAD}) to define the SH_Ox current (I_{SH_Ox}) using the equation;

$$I_{SH\_Ox} = \frac{R_{SHUNT}}{R_1} I_{LOAD} \qquad \text{(eq. 1)}$$

I_{SH_Ox} is also user defined and is not to exceed $I_{SH\_O\_MAX}$. Ideally, the SH_Ox current is around 2 mA. The resistance of R2 is found with the relationship;

$$R_2 = \frac{V_{SH\_Ox}}{I_{SH\_Ox}} \qquad \text{(eq. 2)}$$

Regardless of the values of I_{LOAD} or I_{SH_Ox}, the maximum voltage of the SH_Ox pin shall not exceed V_{SH_Ox}, indicated in the operating range table.

Bus Voltage Monitor (one of four identical instances)

An external voltage divider is used to scale the voltage on the BS_INx pin to an appropriate full−scale range for the differential output amplifier. Resistors R3 and R4 form a resistor divider to define the full dynamic range of the bus voltage monitor with;

$$\frac{R_4}{R_3 + R_4} \times V_{BUS} = V_{BS\_INx} \qquad \text{(eq. 3)}$$

Multiplexer Select

The multiplier selection is controlled by a single digital input (MUX_SEL pin). The device will monitor this pin and cycle through the different measured parameters in a fixed sequence. The sequence will repeat cycle as shown in the tables until either a timeout condition is detected or the device is disabled. The MUX_SEL pin needs to be pulsed at least once before normal MUX_SEL cycles begin. The delay between the falling edge of the last initial MUX_SEL pulse and the first rising edge of the normal MUX_SEL cycle needs to be 14.75 μs > Td > 24.25 μs.

Operating Modes

There are two operating modes – stand−alone (one to four channels) and paired operation (up to eight channels). In paired operation, MODE_SEL is used to designate a "Device A" and "Device B" of a pair. When paired, the differential output amplifiers of the two devices are expected to be "wire−or'ed" together, and the table logic insures that only one device will actively drive DIFF_OUT_P and DIFF_OUT_N at any given time. See description in the Auxiliary Functions section for details. Additionally, devices can be configured to operate with a reduced channel count. See description in the Auxiliary Functions section for details.

Four−Channel Stand−Alone Operation	
MUX_SEL Cycle	**Differential Amp Output**
Standby	Hi−Z
1	Channel 1 Bus Voltage
2	Channel 1 Shunt Current
3	Channel 2 Bus Voltage
4	Channel 2 Shunt Current
5	Channel 3 Bus Voltage
6	Channel 3 Shunt Current
7	Channel 4 Bus Voltage
8	Channel 4 Shunt Current
9→1	Channel 1 Bus Voltage
10→2	Channel 1 Shunt Current
….	Repeat cycle until reset or timeout

Six−Channel Paired Operation		
MUX_SEL Cycle	**Differential Amp Output (Device A)**	**Differential Amp Output (Device B)**
Standby	Hi−Z	Hi−Z
1	Ch 1 Bus Voltage	Hi−Z
2	Ch 1 Shunt Current	Hi−Z
3	Ch 2 Bus Voltage	Hi−Z
4	Ch 2 Shunt Current	Hi−Z
5	Ch 3 Bus Voltage	Hi−Z
6	Ch 3 Shunt Current	Hi−Z
7	Hi−Z	Ch 1 Bus Voltage
8	Hi−Z	Ch 1 Shunt Current
9	Hi−Z	Ch 2 Bus Voltage
10	Hi−Z	Ch 2 Shunt Current
11	Hi−Z	Ch 3 Bus Voltage
12	Hi−Z	Ch 3 Shunt Current
13→1	Ch 1 Bus Voltage	Hi−Z
14→2	Ch 1 Shunt Current	Hi−Z
….	Repeat cycle until reset or timeout	Repeat cycle until reset or timeout

APPLICATIONS DIAGRAMS

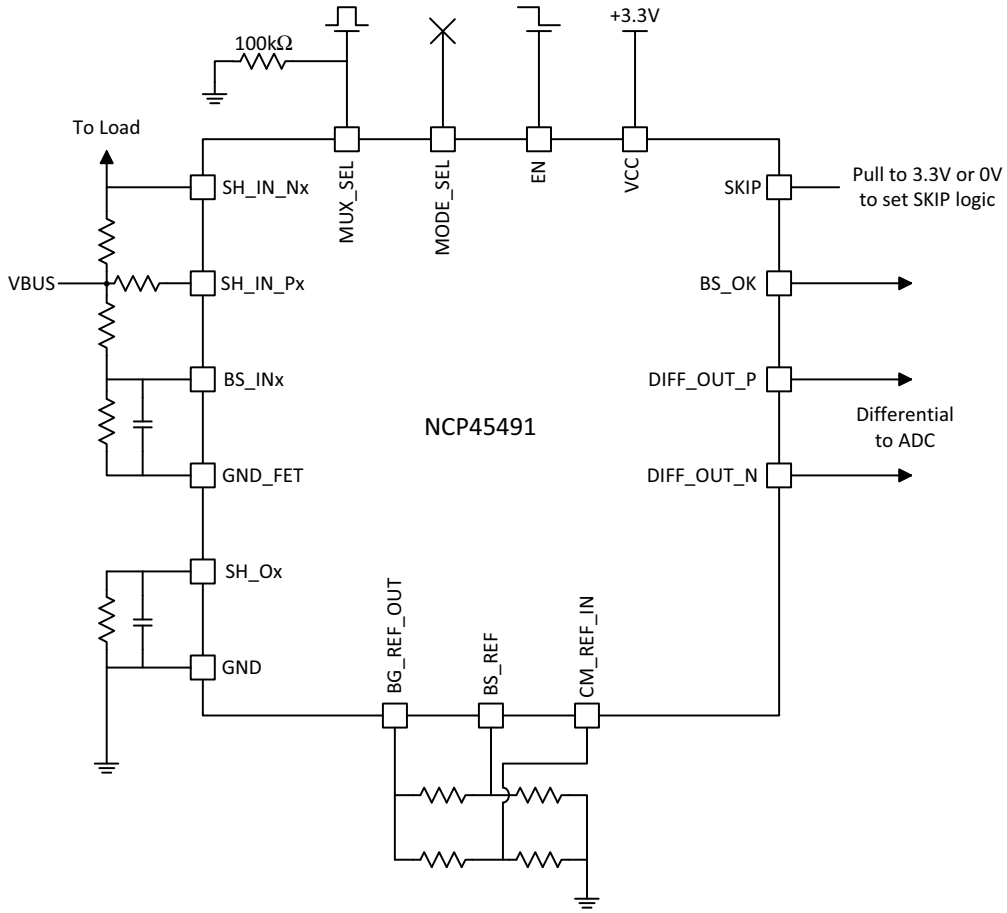


Figure 2. Stand Alone Device Operation

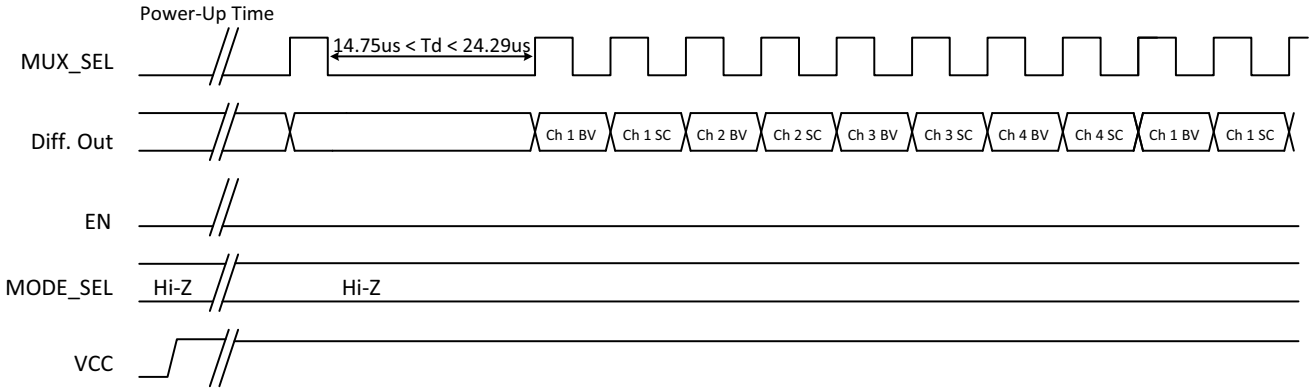


Figure 3. Stand Alone Timing Characteristics

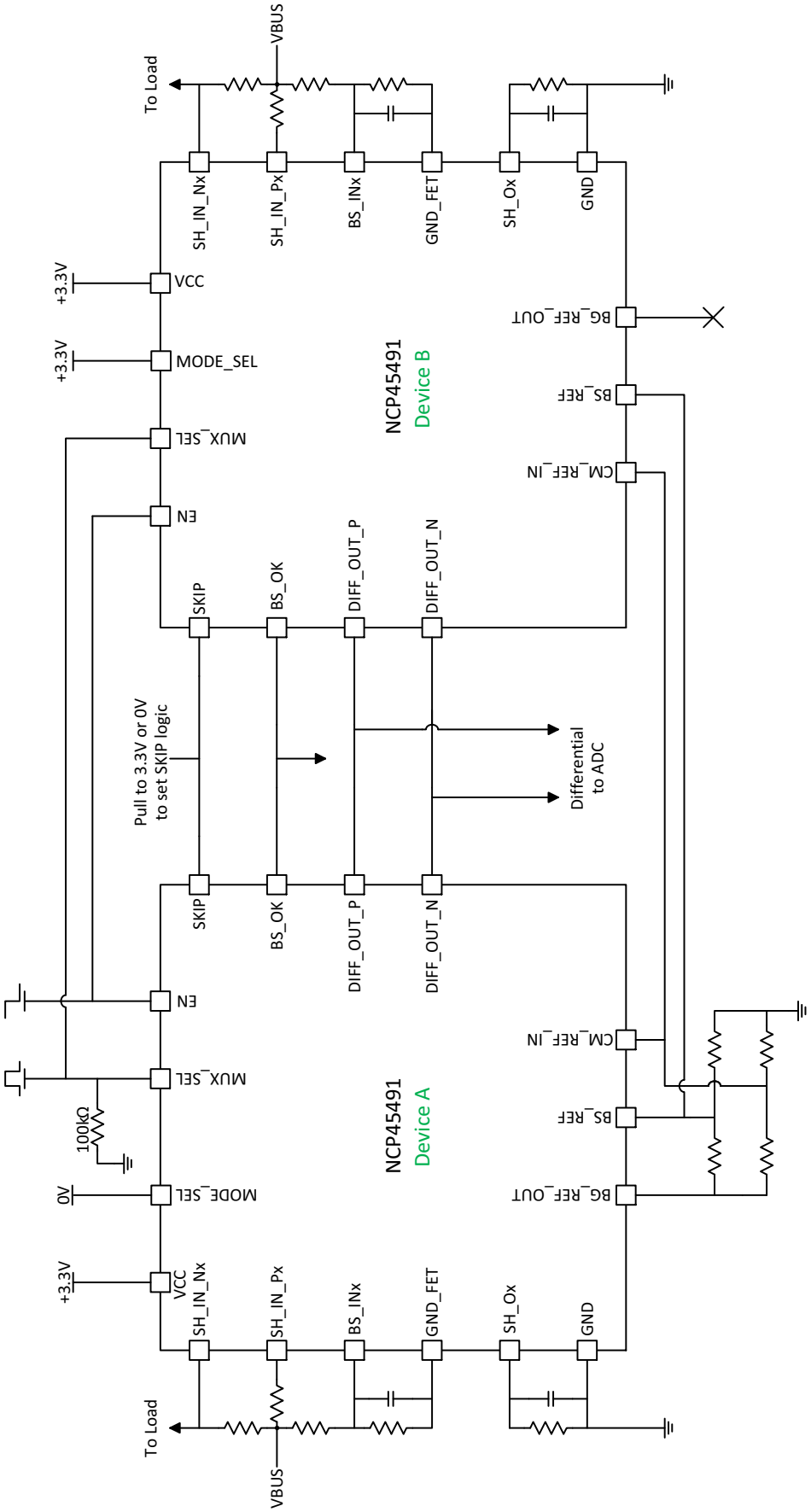


Figure 4. Six−Channel Paired Device Operation

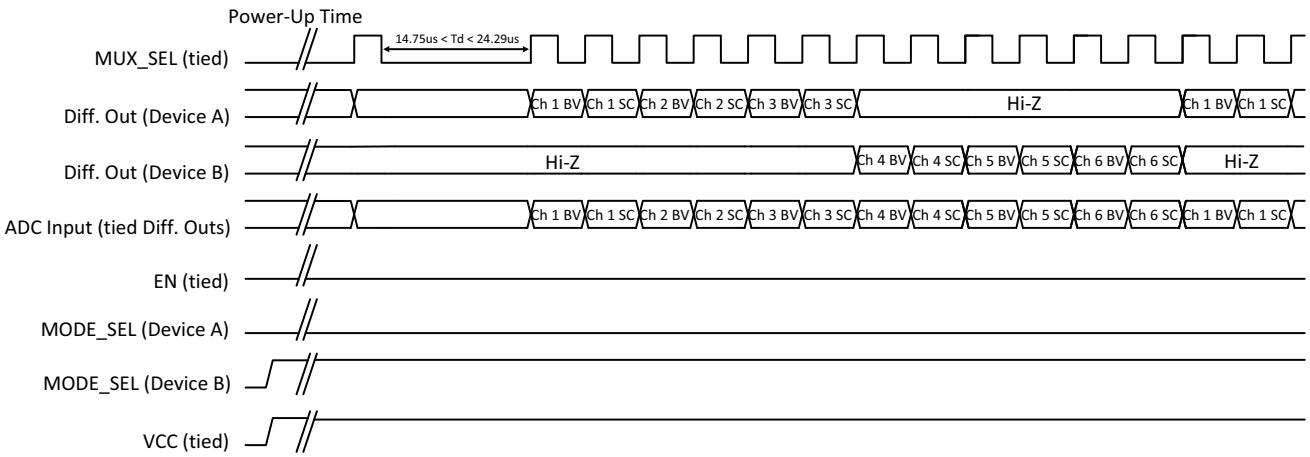


Figure 5. Six−Channel Paired Device Timing Characteristics

AUXILIARY FUNCTIONS

Bus Comparator (BS_OK)

A real−time indication that V_{CC} and all bus voltages (as measured on the BS_INx pins) are valid is provided on the BS_OK pin. BS_OK remains low until all used BS_INx pins are above a user−defined threshold voltage. The threshold voltage for the valid condition of BS_INx pins is set by the voltage provided to the BS_REF pin and must be less than 0.2 V. This can be done via an external resistor divider and the bandgap reference. If desired, the user can use the SKIP pin to modify the logic as shown in the corresponding table (H=high, L=low, Z=tristate, X=don't care). The SKIP pin can also be used to hold BS_OK = L in the absence of VCC.

Reset/Timeout

Normal operation can be interrupted and device returned to standby mode by holding the MUX_SEL pin HIGH or LOW longer than the reset period T_{RP}.

Bandgap Reference

The BG_REF_OUT pin provides a high−accuracy voltage from which BS_REF and CM_REF_IN voltages can be supplied via external voltage dividers.

Ground FET

The GND_FET pin is a switch that connects the bus voltage dividers to ground. In order that these voltage dividers not consume current when not needed (as in device shutdown), a low−impedance open−drain FET disconnects the low−side of these resistor dividers when the EN pin is at a logic HIGH level.

Enable Function

The EN pin controls device operation according to the corresponding table.

Mode Select Function

The MODE_SEL pin controls multiplexer operation according to the corresponding table. Note that MODE_SEL is left floating in stand−alone operation.

Reduced Channel Count

If the SH_O pin is left floating on any channel, that channel and all channels of a higher number in the sequence will be bypassed by the multiplexer logic. For example, if SH_O3 is left floating, SH_O3 and SH_O4 will be bypassed. If devices are in paired mode, the number of unused channels on both devices must be matched. However, bus voltage on those unused channels (as measured on the BS_INx pins) will still be compared to the BS_REF voltage and included in the BS_OK output logic. Detection of SH_O pin as floating is accomplished by way of a small leakage current from VCC, so as not to excessively disturb measurement precision.

SKIP Logic

EN	VCC	BS_INx	SKIP	BS_OK
X	Z(unpowered)	X	H	L
X	L (POR)	X	X	L
H	X	X	X	L
Z/L	H	L	H	L
Z/L	H	H	H	H (open drain)
Z/L	H	X	L	H (open drain)

EN Logic

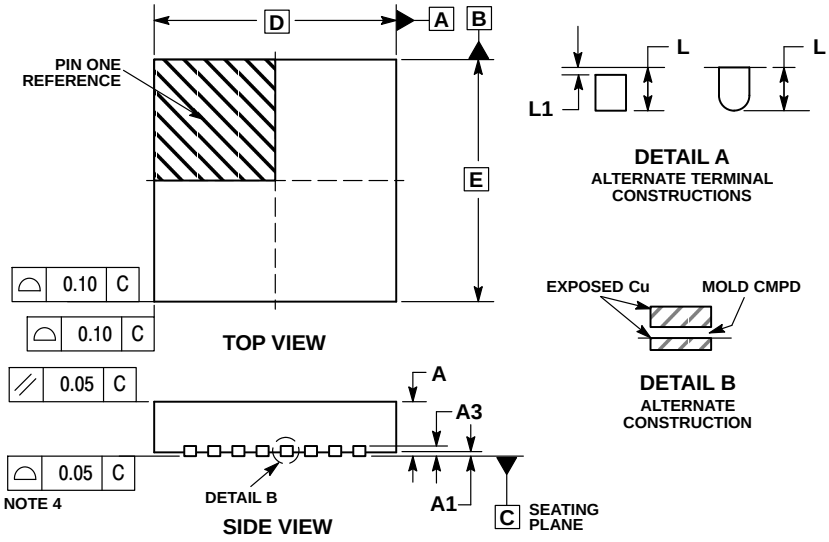
Level	Device Operation
LOW	Fully Functional
Tri−state (floating)	Limited Function: BG_REF_OUT is valid, GND_FET is turned ON, BS_OK comparators and output are functional. All other functions to be disabled. DIFF_OUT to be Hi−Z and multiplexer select logic is held in reset.
HIGH	Standby: As described in Limited Function above with GND_FET turned OFF

MODE_SEL Logic

Level	Multiplexer Operation
LOW	Device A
Tri−state (floating)	Stand−Alone
HIGH	Device B

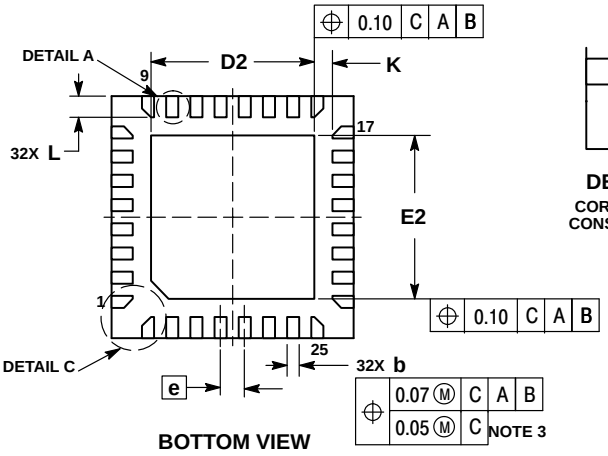
PACKAGE DIMENSIONS

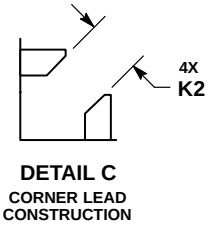
QFN32 4x4, 0.4P
CASE 485CD
ISSUE A

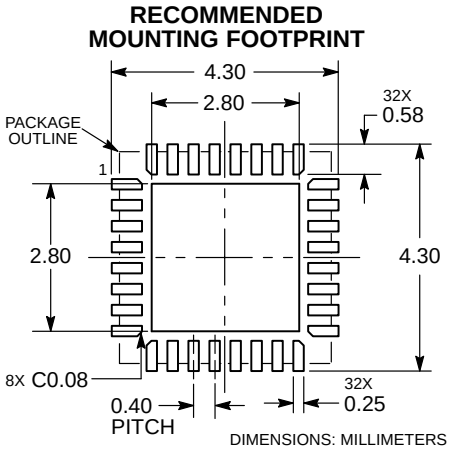


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	4.00 BSC	
D2	2.60	2.80
E	4.00 BSC	
E2	2.60	2.80
e	0.40 BSC	
K	0.30 REF	
K2	0.45 REF	
L	0.25	0.45
L1	–––	0.15







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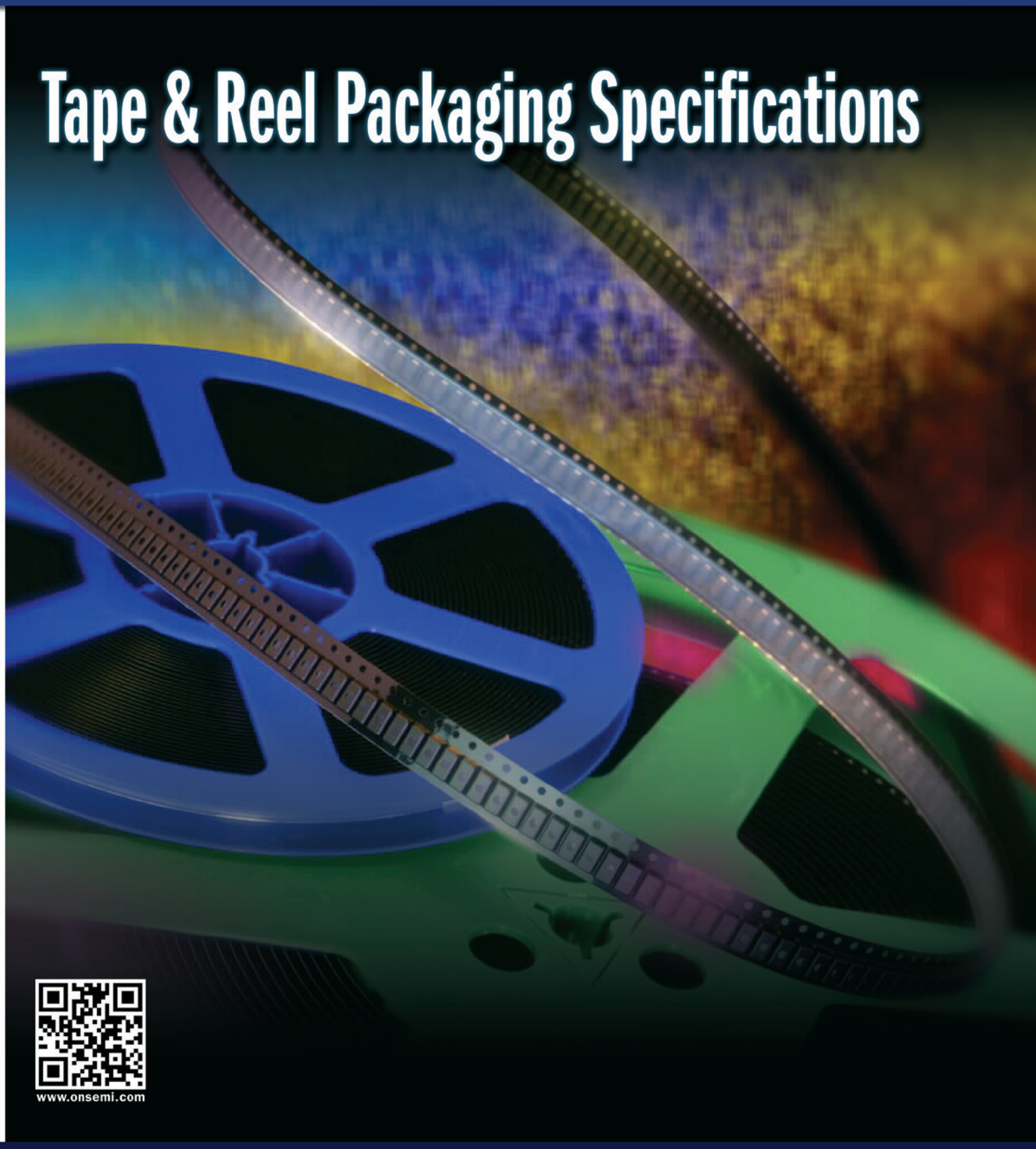
Tape & Reel Packaging Specifications



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Tape and Reel Packaging Specifications

BRD8011/D
Rev. 15, September−2012

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ON Semiconductor
Tape and Reel Packaging Specifications

In Brief . . .

This booklet has been offered to assist those looking to coordinate packaging specifications with assembly line requirements. Additionally, dimensional and ordering information is supplied for those discrete devices that take the form of axial−leaded parts.

Tape and Reel Packaging Specifications

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the “peel−back” cover tape.

- Two Reel Sizes Available (7″ and 13″)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, −1, −2 Series
- 8 mm Tape: 6−Bump, 9−Bump, 10−Bump, MicroLeadless™, ChipFET, DFN/QFN packages ≤ 3.3x3.3, DSN, Flip−Chip, SOD−123, SC−59, SC−70, SC−74, SC−74A, SC−75, SC−82, SC−82AB, SC−88, SC−88A, SC−89, SOD−123, SOD−323, SOD−523, SOD−723, SOD−923, SOT−143, SOT−23, SOT−23L, SOT−323, SOT−353, SOT−553/563, SOT−723, SOT−883, TSOP−5, TSOP−6, US8, WLCSP−4, WLCSP−5, X3DFN, XLLGA
- 12 mm Tape: DFN/QFN packages > 3.3x3.3 and ≤ 7x7, FCBGA−16, Micro10, Micro8™, PowerFLEX™, POWERMITE™, QSOP−16, SMA, SMB, SO−8 (SOIC 8), SOT−223, SOT−89, SSOP−8, TSSOP−8, TSSOP−10, TSSOP−14, TSSOP−16
- 16 mm Tape: DFN/QFN packages > 7x7, DPAK, FCBGA−16, PLCC−20, QSOP−24, SMC, SO−14 (SOIC 14), SO−16 (SOIC 16), SO−16 Wide (SOIC 16W), SOEIAJ14, SOEIAJ16, SOP−16, SSOP−14 Wide, TQFP−32, TSSOP−20
- 24 mm Tape: D^2PAK, FCBGA−81, LQFP−52, LQFP−64, PLCC−28, SO−18 Wide (SOIC 18W), SO−20 Wide (SOIC 20W), SO−24 Wide (SOIC 24W), SOEIAJ−20, TQFP−52, TQFP−64, TSSOP−48
- 32 mm Tape: PLCC−44, PLCC−52, SO−28L Wide (SOIC 28W), SO−28 Wide (SOIC 28W), SO−32 Wide (SOIC 32W),
- 44 mm Tape: PLCC−98, PLCC−84
- For Leadless Package Pin 1 Orientation, please see Figure 38 (Effective January 2007).

Use the standard device title and add the required suffix as listed in the option table on the following page. Note that the individual reels have a finite number of devices depending on the type of product contained in the tape. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

Embossed Tape and Reel Ordering Information

Package	Tape Width mm	Pitch mm (Dimension P_1) (inch)	Reel Size		Devices Per Reel and Min Order Quantity	Tape and Reel Suffix	Fig No	Page No
			(mm)	(in)				
6−Bump (1.489x0.989)	8	4.0 ± 0.1 (0.158 ± 0.004)	178	7	3,000	T1 − TMOS	7	14
9−Bump (1.489x1.489)	8	4.0 ± 0.1 (0.158 ± 0.004)	178	7	3,000	T1 − TMOS	7	14
10−Bump	8	4.0 ± 0.1 (0.158 ± 0.004)	178	7	3,000	T1 − Discrete	7	14
Axial Leaded	See Axial Leaded package specifications beginning on page 27							
ChipFET	8	4.0 ± 0.1 (0.158 ± 0.004)	178	7	3,000	T1 − TMOS	11	15
D^2PAK 3 Lead	24	16.0 ± 0.1 (0.630 ± 0.004)	330	13	800	R4 Analog T4 − Discrete	1	13
D^2PAK 5 Lead	24	16.0 ± 0.1 (0.630 ± 0.004)	330	13	800	R4 − Analog T4 − Discrete	1	13
D^2PAK 7 Lead	24	16.0 ± 0.1 (0.630 ± 0.004)	330	13	750	R7 − Analog	1	13
DFN/QFN ≤ 1.4x1.4mm	8	2.0 ± 0.1 (0.079 ± 0.004)	178	7	See Data Sheet	Various	36−38	19,20
DFN/QFN ≤ 3.3x3.3mm	8 8	4.0 ± 0.1 (0.158 ± 0.004) 4.0 ± 0.1 (0.158 ± 0.004)	178 330	7 13	See Data Sheet See Data Sheet	See Data Sheet See Data Sheet	36−38	19,20
DFN/QFN > 3.3x3.3mm and ≤ 7x7mm	12 12	8.0 ± 0.1 (0.315 ± 0.004) 8.0 ± 0.1 (0.315 ± 0.004)	178 330	7 13	See Data Sheet See Data Sheet	See Data Sheet See Data Sheet	36−38	19,20
DFN/QFN 7x7mm	12 12	16.0 ± 0.1 (0.630 ± 0.004) 16.0 ± 0.1 (0.630 ± 0.004)	178 330	7 13	See Data Sheet See Data Sheet	See Data Sheet See Data Sheet	36−38	19,20
DFN/QFN 9x9mm	16 16	12.0 ± 0.1 (0.471 ± 0.004) 12.0 ± 0.1 (0.471 ± 0.004)	178 330	7 13	See Data Sheet See Data Sheet	See Data Sheet See Data Sheet	36−38	19,20
DFN/QFN 10.5x10.5mm	16 16	16.0 ± 0.1 (0.630 ± 0.004) 16.0 ± 0.1 (0.630 ± 0.004)	178 330	7 13	See Data Sheet See Data Sheet	See Data Sheet See Data Sheet	36−38	19,20
DO−41	79	5.08 ± 0.508	356	14	5,000	RL − Discrete	N/A	32
DPAK	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,800	RL − Discrete	4	13
DPAK	16	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	T4, T5 − Discrete RK, T5 − Analog	2, 3	13
DSN	8	2.0 ± 0.05 (0.079 ± 0.002)	178	7	5,000	T5 − Discrete	6	14
FCBGA−16	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500/500	R2 − Clock & Data Mgmt	35	19
FCBGA−49	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	2,000/500	R2 − Clock & Data Mgmt	35	19
FCBGA−81	24	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,500/500	R2 − Clock & Data Mgmt	35	19
Flip−Chip	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Discrete	N/A	N/A
LQFP − 48	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	2,000	R48 − Analog	8	14
LQFP−32	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1800 or 2000	R2 − Analog, Clock & Data Mgmt	8	14
LQFP−52	24	16.0 ± 0.1 (0.630 ± 0.004)	330	13	1,500	R2 − Clock & Data Mgmt	8	14
LQFP−64	24	16.0 ± 0.1 (0.630 ± 0.004)	330	13	1,500	R2 − Clock & Data Mgmt	8	14
Micro10	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	4,000	R2 − Analog, Discrete	31	18
Micro8™	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	R2, T − Analog	31	18
Micro8	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	4,000	R2 − Analog, Discrete	31	18

Embossed Tape and Reel Ordering Information

Package	Tape Width mm	Pitch mm (Dimension P_1) (inch)	Reel Size		Devices Per Reel and Min Order Quantity	Tape and Reel Suffix	Fig No	Page No
			(mm)	(in)				
PLCC−20	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,000	R2 − Clock & Data Mgmt	9	14
PLCC−28	24	16.0 ± 0.1 (0.630 ± 0.004)	330	13	500	R2 − Clock & Data Mgmt	9	14
PLCC−44	32	24.0 ± 0.1 (0.942 ± 0.004)	330	13	500	R2 − Clock & Data Mgmt, Analog	9	14
PLCC−44	32	24.0 ± 0.1 (0.942 ± 0.004)	330	13	500	R44 − Analog	9	14
PLCC−52	32	24.0 ± 0.1 (0.942 ± 0.004)	330	13	500	R2 − Clock & Data Mgmt, Analog	9	14
PLCC−68	44	32.0 ± 0.1 (1.256 ± 0.004)	330	13	250	R2 − Clock & Data Mgmt, Analog	9	14
PLCC−84	44	36.0 ± 0.1 (1.418 ± 0.004)	330	13	250	R2 − Clock & Data Mgmt, Analog	9	14
PowerFLEX™	12	24.0 ± 0.1 (0.942 ± 0.004)	330	13	2,000	R7 − Analog	1	13
POWERMITE®	12	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, TR7 − Discrete	20	16
POWERMITE	12	4.0 ± 0.1 (0.157 ± 0.004)	330	13	12,000	T3, TR13 − Discrete	20	16
SC−59	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, T2 − Discrete	13	15
SC−59	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3 − Discrete	13	15
SC−70	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Discrete	13	15
SC−70	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3 − Discrete	13	15
SC−70 5 Lead	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Analog	15	15
SC−70 6 Lead	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Analog	22	17
SC−70 6 Lead	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3 − Analog	22	17
SC−74	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Discrete	14	15
SC−74A	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Discrete	12	15
SC−75	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Discrete	13	15
SC−82	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	TR − Analog	10	15
SC−82AB	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Analog, Discrete	10	15
SC−88	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3 − Discrete	22	17
SC−88	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, T2 − Discrete T1 − Analog	22	17
SC−88A	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, T2 − Discrete	15	15
SC−88A	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3, T4 − Discrete	15	15
SC−89	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Discrete	13	15
SC−89	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3 − Discrete	13	15
SMA	12	4.0 ± 0.1 (0.157 ± 0.004)	178	7	1,500	T1 − Discrete	21	16
SMA	12	4.0 ± 0.1 (0.157 ± 0.004)	330	13	5,000	T3 − Discrete	21	16
SMB	12	8.0 ± 0.1 (0.315 ± 0.004)	178	7	1,000	T1 − Discrete	21	16
SMB	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	T3 − Discrete	21	16
SMC	16	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	T3 − Discrete	21	16
SO−14 (SOIC 14)	16	8.0 ± 0.1 (0.315 ± 0.004)	330	13	3,000	R14 − Analog E.G.*	31	18
SO−14 (SOIC 14)	16	8.0 ± 0.1 (0.315 ± 0.004)	330	13	3,000	R2 − Clock & Data Mgmt, Logic, Analog	31	18
SO−16 (SOIC 16)	16	8.0 ± 0.1 (0.315 ± 0.004)	330	13	3,000	R2 − Clock & Data Mgmt, Logic, Analog	31	18
SO−16 (SOIC 16)	16	8.0 ± 0.1 (0.315 ± 0.004)	330	13	3,000	R16 − Analog E.G.*	31	18
SO−16 Wide (SOIC 16W)	16	8.0 ± 0.1 (0.315 ± 0.004)	330	13	1,500	R2 − Clock & Data Mgmt, Logic, Analog	31	18
SO−16 Wide (SOIC 16W)	16	8.0 ± 0.1 (0.315 ± 0.004)	330	13	1,500	R16 − Analog E.G.*	31	18

* Applies to Analog devices manufactured at the East Greenwich, Rhode Island, USA facility.

Embossed Tape and Reel Ordering Information

Package	Tape Width mm	Pitch mm (Dimension P_1) (inch)	Reel Size		Devices Per Reel and Min Order Quantity	Tape and Reel Suffix	Fig No	Page No
			(mm)	(in)				
SO−18 Wide (SOIC 18W)	24	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,000	R2 − Clock & Data Mgmt	31	18
SO−18 Wide (SOIC 18W)	24	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,000	R18 − Analog E.G.*	31	18
SO−20 Wide (SOIC 20W)	24	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,500	R2 − Analog, Clock & Data Mgmt	31	18
SO−20 Wide (SOIC 20W)	24	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,500	R20 − Analog E.G.*	31	18
SO−24 Wide (SOIC 24W)	24	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,500	R2 − Analog, Clock & Data Mgmt	31	18
SO−24 Wide (SOIC 24W)	24	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,500	R24 − Analog E.G.*	31	18
SO−28 Wide (SOIC 28W)	24	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,000	R2 − Analog, Clock & Data Mgmt	32	18
SO−28L Wide (SOIC 28W)	32	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,000	R3 − Analog	32	18
SO−28 Wide (SOIC 28W)	32	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,000	R28− Analog E.G.*	32	18
SO−32 Wide (SOIC 32W)	32	12.0 ± 0.1 (0.471 ± 0.004)	330	13	1,000	R32− Analog E.G.*	31	18
SO−8 (SOIC 8)	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500 / 3,000	R8 − Analog E.G.*	31	18
SO−8 (SOIC 8)	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500 / 3,000	R2 − TMOS, Analog, Clock & Data Mgmt	31	18
SO−8 (SOIC 8)	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500 / 3,000	T3 − EEPROM	31	18
SOD−123	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, T2 − Discrete	26	17
SOD−123	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3 − Discrete	26	17
SOD−323	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Discrete	26	17
SOD−323	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3 − Discrete	26	17
SOD−523	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Discrete	28	18
SOD−523	8	2.0 ± 0.05 (0.079 ± 0.002)	178	7	8,000	T5 − Discrete	28	18
SOD−723	8	2.0 ± 0.05 (0.079 ± 0.002)	178	7	8,000	T5 − Discrete	29	18
SOD−923	8	2.0 ± 0.05 (0.079 ± 0.002)	178	7	8,000	T5 − Discrete	29	18
SOEIAJ14	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	2,000	EL − Logic	N/A	N/A
SOEIAJ16	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	2,000	EL − Logic	N/A	N/A
SOEIAJ20	24	12.0 ± 0.1 (0.471 ± 0.004)	330	13	2,000	EL − Logic	N/A	N/A
SON−6	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Analog	27	17
SON−8	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Analog	N/A	N/A
SOP−16	16	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	R2 − Analog	31	18
SOT−143	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3, T4 − Discrete	25	17
SOT−143	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, T2, Discrete T − Analog	25	17
SOT−223	12	8.0 ± 0.1 (0.315 ± 0.004)	178	7	1,000	T1 − Discrete, Analog	30	18
SOT−223	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	R3 or T3 − Analog E.G.*	30	18
SOT−223	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	4,000	T3 − Discrete, TMOS T3 − Analog	30	18
SOT−23	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, − Discrete TR, T1 − Analog	13	15
SOT−23	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3 − Discrete	13	15
SOT−23 5 Lead	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, TR, T − Analog	12	15
SOT−23 6 Lead	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, R1 − Analog	14	15

* Applies to Analog devices manufactured at the East Greenwich, Rhode Island, USA facility.

Embossed Tape and Reel Ordering Information

Package	Tape Width mm	Pitch mm (Dimension P_1) (inch)	Reel Size		Devices Per Reel and Min Order Quantity	Tape and Reel Suffix	Fig No	Page No
			(mm)	(in)				
SOT−23L	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	4,000	R2− Analog	13	15
SOT−323	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1 − Discrete	13	15
SOT−323	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3 − Discrete	13	15
SOT−353	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, T2 − Discrete	15	15
SOT−353	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3, T4 − Discrete	15	15
SOT−553/563	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	4,000	T1 − Discrete, Logic	16,17	16
SOT−553/563	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	4,000	T2 − Discrete, Logic, Analog	16,17	16
SOT−553/563	8	2.0 ± 0.05 (0.079 ± 0.002)	178	7	8,000	T5 − Discrete, Logic	16,17	16
SOT−553/563	8	2.0 ± 0.05 (0.079 ± 0.002)	178	7	8,000	T6 − Discrete, Logic	16,17	16
SOT−723	8	2.0 ± 0.05 (0.079 ± 0.002)	178	7	8,000	T5 − Discrete	13	15
SOT−89	12	8.0 ± 0.1 (0.315 ± 0.004)	178	7	1,000	T1, R1 − Discrete T1 − Analog	23	17
SOT−883	8	2.0 ± 0.1 (0.158 ± 0.004)	178	7	8,000	T5 − Discrete	5	14
SOT−953/963	8	2.0 ± 0.05 (0.079 ± 0.002)	178	7	8,000	T5 − Discrete, Logic	18,19	16
SSOP−14	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	2,000	R14 − Analog E.G.*	31	18
SSOP−16	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	2,000	R16 − Analog E.G.*	31	18
SSOP−20	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	2,000	R20 − Analog E.G.*	31	18
SSOP−24 Wide	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	2,000	R24 − Analog E.G.*	31	18
SSOP−8	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	3,000	T1− Analog	31	18
TO−92	See TO−92 and other Axial Leaded package specifications beginning on page 27							
TQFP−32	16	12.0 ± 0.1 (0.471 ± 0.004)	330	13	2,000	R2 − Analog, Clock & Data Mgmt	8	14
TQFP−52	24	16.0 ± 0.1 (0.630 ± 0.004)	330	13	1,500	R2 − Clock & Data Mgmt	8	14
TQFP−64	24	16.0 ± 0.1 (0.630 ± 0.004)	330	13	1,500	R2 − Clock & Data Mgmt	8	14
TSOP−5	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, T2 − Discrete T1, T2, TR − Analog	12	15
TSOP−5	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3 − Discrete	12	15
TSOP−6	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	T1, T2 − Analog, Discrete	14	15
TSOP−6	8	4.0 ± 0.1 (0.157 ± 0.004)	330	13	10,000	T3 − Analog, Discrete	14	15
TSSOP−10	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	R2 − Clock & Data Mgmt	31	18
TSSOP−14	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	R2 − Analog, Clock & Data Mgmt	31	18
TSSOP−16	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	R2 − Analog, Clock & Data Mgmt	31	18
TSSOP−20	16	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	R2 − Analog, Clock & Data Mgmt	31	18
TSSOP−24	16	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	R2 − Analog, Clock & Data Mgmt	31	18
TSSOP−48	24	12.0 ± 0.1 (0.471 ± 0.004)	330	13	2,500	R2 − Clock & Data Mgmt	31	18
TSSOP−8	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	2,500	R2 − Analog, Clock & Data Mgmt	31	18
TSSOP−8	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	4,000	R2 − Discrete, MOS	31	18
TSSOP−8	12	8.0 ± 0.1 (0.315 ± 0.004)	330	13	3,000	R3 − Discrete, MOS	31	18
US8	8	4.0 ± 0.1 (0.157 ± 0.004)	178	7	3,000	US − Logic	24	17
WLCSP ≤ 0.86x0.84mm	8	2.0 ± 0.1 (0.079 ± 0.004)	178	7	5000	TR	36−38	19,20
WLCSP ≤ 1.4x1.4mm	8	2.0 ± 0.1 (0.079 ± 0.004)	178	7	See Data Sheet	Various	36−38	19,20

WLCSP ≤ 3.3x3.3mm	8 8	4.0 ± 0.1 (0.158 ± 0.004) 4.0 ± 0.1 (0.158 ± 0.004)	178 330	7 13	See Data Sheet See Data Sheet	Various Various	36–38	19,20
WLCSP > 3.3x3.3mm and ≤ 7x7mm	12 12	8.0 ± 0.1 (0.315 ± 0.004) 8.0 ± 0.1 (0.315 ± 0.004)	178 330	7 13	See Data Sheet See Data Sheet	Various Various	36–38	19,20
WLCSP > 7x7mm and ≤ 8x8mm	12 12	16.0 ± 0.1 (0.630 ± 0.004) 16.0 ± 0.1 (0.630 ± 0.004)	178 330	7 13	See Data Sheet See Data Sheet	Various Various	36–38	19,20
WLCSP> 8x8mm and ≤ 10.5x10.5mm	16 16	12.0 ± 0.1 (0.471 ± 0.004) 12.0 ± 0.1 (0.471 ± 0.004)	178 330	7 13	See Data Sheet See Data Sheet	Various Various	36–38	19,20
WLCSP >10.5x10.5mm	16 16	16.0 ± 0.1 (0.630 ± 0.004) 16.0 ± 0.1 (0.630 ± 0.004)	178 330	7 13	See Data Sheet See Data Sheet	Various Various	36–38	19,20
XLLGA	8	2.0 ± 0.1 (0.158 ± 0.004)	178	7	8,000	T5 – Discrete	34	19

***** Applies to Analog devices manufactured at the East Greenwich, Rhode Island, USA facility.

Former CMD Tape & Reel Specifications, by Package

Former CMD Tape and Reel Specificaions by Package

Package	Package Size (mm)	Tape Width	Reel Diameter	Quantity per Reel	P_0	P_1	Orientation Quadrant
CSP, 2−Bump	0.60 x 0.30 x 0.275	8 mm	178 mm (7”)	15,000	4 mm	4 mm	Top
CSP, 4−Bump	0.8 x 0.8 x 0.50	8 mm	178 mm (7”)	10,000	4 mm	2 mm	B
CSP, 4−Bump	0.8 x 0.8 x 0.60	8 mm	178 mm (7”)	5000	4 mm	4 mm	B
CSP, 4−Bump	0.96 x 0.96 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 4−Bump	0.96 x 0.96 x 0.65	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 5−Bump	1.05 x 0.76 x 0.615	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 5−Bump	1.20 x 0.80 x 0.60	8 mm	178 mm (7”)	5000	4 mm	4 mm	B
CSP, 5−Bump	1.33 x 0.96 x 0.606	8 mm	178 mm (7”)	3500	4 mm	4 mm	A
CSP, 5−Bump	1.33 x 0.96 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	A
CSP, 5−Bump	1.41 x 0.93 x 0.606	8 mm	178 mm (7”)	3500	4 mm	4 mm	A
CSP, 5−Bump	1.41 x 0.95 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	A
CSP, 5−Bump	1.59 x 1.22 x 0.64	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 6−Bump	1.46 x 0.96 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 6−Bump	1.72 x 1.22 x 0.64	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 6−Bump	1.804 x 1.154 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 8−Bump	1.16 x 1.16 x 0.60	8 mm	178 mm (7”)	5000	4 mm	4 mm	B
CSP, 8−Bump	1.20 x 1.20 x 0.60	8 mm	178 mm (7”)	5000	4 mm	4 mm	B
CSP, 8−Bump	1.43 x 1.41 x 0.605	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 8−Bump	1.60 x 1.60 x 0.65	8 mm	178 mm (7”)	5000	4 mm	4 mm	B
CSP, 9−bump	2.470 x 0.970 x 0.606	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 9−bump	2.470 x 0.970 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 10−Bump	1.56 x 1.053 x 0.615	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 10−Bump	1.67 x 1.11 x 0.615	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 10−Bump	1.67 x 1.14 x 0.615	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 10−Bump	1.96 x 1.33 x 0.606	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 10−Bump	1.96 x 1.33 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	A
CSP, 10−Bump	2.46 x 0.96 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 10−Bump	3.104 x 1.154 x 0.682	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 11−Bump	1.46 x 1.96 x 0.65	8 mm	178 mm (7”)	5000	4 mm	4 mm	B
CSP, 11−Bump	2.05 x 1.44 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 14−Bump	2.00 x 1.10 x 0.58	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 15−Bump	2.36 x 1.053 x 0.262	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 15−Bump	2.36 x 1.053 x 0.615	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 15−Bump	2.36 x 1.053 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 15−Bump	2.47 x 1.11 x 0.615	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 15−Bump	2.47 x 1.14 x 0.615	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 15−Bump	2.96 x 1.33 x 0.605	8 mm	178 mm (7”)	3500	4 mm	4 mm	B

For orientation and dimension specifications, see diagrams on page 21.

Former CMD Tape and Reel Specificaions by Package

Package	Package Size (mm)	Tape Width	Reel Diameter	Quantity per Reel	P_0	P_1	Orientation Quadrant
CSP, 15−Bump	2.96 x 1.33 x 0.615	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 15−Bump	2.96 x 1.33 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 15−Bump	3.16 x 1.053 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 15−Bump	3.006 x 1.376 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 15−Bump	3.01 x 1.38 x 0.644	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 18−Bump	1.96 x 1.56 x 0.60	8 mm	178 mm (7”)	5000	4 mm	4 mm	B
CSP, 20−Bump	3.16 x 1.053 x 0.615	8 mm	178 mm (7”)	3500	4 mm	4 mm	B
CSP, 20−Bump	3.27 x 1.11 x 0.615	12 mm	330 mm (13”)	3500	4 mm	4 mm	B
CSP, 20−Bump	3.96 x 1.33 x 0.644	8 mm	178 mm (7”)	3500	4 mm	8 mm	B
CSP, 20−Bump	3.96 x 1.586 x 0.640	12 mm	330 mm (13”)	3500	4 mm	4 mm	B
CSP, 20−Bump	4.00 x 1.46 x 0.605	12 mm	330 mm (13”)	3500	4 mm	4 mm	B
CSP, 20−Bump	4.00 x 1.46 x 0.606	12 mm	330 mm (13”)	3500	4 mm	8 mm	B
CSP, 20−Bump	4.00 x 1.46 x 0.644	12 mm	330 mm (13”)	3500	4 mm	8 mm	B
CSP, 20−Bump	4.006 x 1.376 x 0.644	12 mm	330 mm (13”)	3500	4 mm	4 mm	B
CSP, 24−Bump	1.96 x 1.96 x 0.60	8 mm	178 mm (7”)	5000	4 mm	4 mm	B
CSP, 24−Bump	2.06 x 2.06 x 0.6	8 mm	178 mm (7”)	5000	4 mm	4 mm	B
CSP, 24−Bump	2.60 x 2.60 x 0.65	8 mm	178 mm (7”)	500	4 mm	4 mm	B
CSP, 25−Bump	2.00 x 2.00 x 0.60	8 mm	178 mm (7”)	500	4 mm	4 mm	B
CSP, 49−Bump	2.80 x 2.80 x 0.50	8 mm	178 mm (7”)	500	4 mm	4 mm	B
CSP, 49−Bump	2.80 x 2.80 x 0.60	8 mm	178 mm (7”)	500	4 mm	4 mm	B
MSOP−8	3.00 x 3.00 x 0.85	12 mm	330 mm (13”)	4000	4 mm	8 mm	A
MSOP−10	3.00 x 3.00 x 0.85	12 mm	330 mm (13”)	4000	4 mm	8 mm	A
QSOP−16	4.90 x 3.89 x 1.55	12 mm	330 mm (13”)	2500	4 mm	8 mm	A
QSOP−24	8.65 x 3.90 x 1.35	16 mm	178 mm (7”)	1000	4 mm	8 mm	A
QSOP−24	8.65 x 3.90 x 1.35	16 mm	330 mm (13”)	2500	4 mm	8 mm	A
SC70−3	2.05 x 1.25 x 0.95	8 mm	178 mm (7”)	3000	4 mm	4 mm	C
SC70−5	2.05 x 1.25 x 0.95	8 mm	178 mm (7”)	3000	4 mm	4 mm	C
SC70−5	2.05 x 1.25 x 0.95	8 mm	178 mm (7”)	3000	4 mm	4 mm	C
SC70−6	2.05 x 1.25 x 0.95	8 mm	178 mm (7”)	3000	4 mm	4 mm	C
SOD−882	1.00 x 0.60 x 0.50	8 mm	178 mm (7”)	5000	4 mm	4 mm	A
SOIC−8	4.90 x 3.99 x 1.55	12 mm	330 mm (13”)	2500	4 mm	8 mm	A
SOIC−8	4.90 x 6.00 x 1.55	12 mm	330 mm (13”)	2500	4 mm	8 mm	A
SOT143	2.92 x 2.37 x 1.01	8 mm	178 mm (7”)	3000	4 mm	4 mm	C
SOT143−4	2.92 x 2.37 x 1.01	8 mm	178 mm (7”)	3000	4 mm	4 mm	C
SOT23−3	2.92 x 2.37 x 1.01	8 mm	178 mm (7”)	3000	4 mm	4 mm	C
SOT23−5	2.92 x 2.79 x 1.24	8 mm	178 mm (7”)	3000	4 mm	4 mm	C
SOT23−6	2.90 x 2.80 x 1.45	8 mm	178 mm (7”)	3000	4 mm	4 mm	C
SOT−553	1.60 x 1.60 x 0.55	8 mm	178 mm (7”)	5000	4 mm	4 mm	C
SOT−563	1.60 x 1.60 x 0.55	8 mm	178 mm (7”)	5000	4 mm	4 mm	C
SOT−593	1.00 x 0.80 x 0.45	8 mm	178 mm (7”)	8000	4 mm	4 mm	B

For orientation and dimension specifications, see diagrams on page 21.

Former CMD Tape and Reel Specificaions by Package

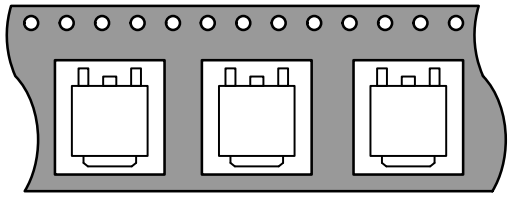
Package	Package Size (mm)	Tape Width	Reel Diameter	Quantity per Reel	P_0	P_1	Orientation Quadrant
CUDFN−6	1.60 x 1.60 x 0.60	8 mm	178 mm (7”)	2500	4 mm	4 mm	A
CUDFN−6	2.00 x 2.00 x 0.65	8 mm	178 mm (7”)	2500	4 mm	4 mm	A
TDFN−8	1.70 x 1.35 x 0.75	8 mm	178 mm (7”)	3000	4 mm	4 mm	A
TDFN−8	2.00 x 2.00 x 0.75	8 mm	178 mm (7”)	3000	4 mm	4 mm	A
TDFN−8	3.00 x 3.00 x .075	12 mm	330 mm (13”)	3000	4 mm	8 mm	A
TDFN−12	3.00 x 1.35 x 0.75	8 mm	178 mm (7”)	3000	4 mm	4 mm	A
TDFN−16	4.00 x 1.60 x 0.75	12 mm	178 mm (7”)	3000	4 mm	4 mm	A
TDFN−16	4.00 x 1.70 x 0.75	12 mm	330 mm (13”)	3000	4 mm	8 mm	A
TDFN−16	6.00 x 4.00 x 0.75	12 mm	330 mm (13”)	3000	4 mm	8 mm	A
TSSOP−8	3.00 x 6.38 x 1.10	12 mm	330 mm (13”)	2500	4 mm	8 mm	A
TSSOP−38	9.70 x 6.40 x 1.20	16 mm	330 mm (13”)	2500	4 mm	12 mm	A
UDFN−6	1.25 x 1.0 x 0.50	8 mm	178 mm (7”)	3000	4 mm	4 mm	A
UDFN−8	1.70 x 1.35 x 0.50	8 mm	178 mm (7”)	3000	4 mm	4 mm	A
UDFN−8	1.70 x 1.35 x 0.50	8 mm	178 mm (7”)	3000	4 mm	4 mm	A
UDFN−8	2.00 x 2.00 x 0.55	8 mm	178 mm (7”)	3000	4 mm	4 mm	A
UDFN−12	2.50 x 1.20 x 0.50	8 mm	178 mm (7”)	3000	4 mm	4 mm	A
UDFN−12	2.50 x 1.35 x 0.50	8 mm	178 mm (7”)	3000	4 mm	4 mm	A
UDFN−16	3.30 x 1.35 x 0.50	8 mm	178 mm (7”)	3000	4 mm	4 mm	A
uUDFN−10	2.50 x 1.00 x 0.50	8 mm	178 mm (7”)	3000	4 mm	4 mm	A
X3DFN	0.62 x 0.62 x 0.32	8 mm	178 mm (7”)	15,000	2 mm	2 mm	Top

For orientation and dimension specifications, see diagrams on page 21.

Product Orientation

Direction of Feed

Figure 1. D^{2}PAK
24 mm (Tape Width, Typical)

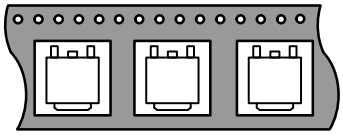


5 Lead – T4 Discrete
R4, R5 Analog

7 Lead – R7 Analog
PowerFLEX–7 – R7 Analog

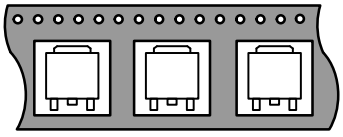
3 Lead – T4 Discrete
R3, R4 Analog

Figure 2. DPAK
16 mm



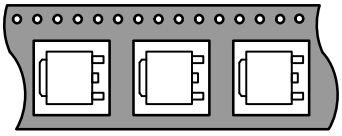
Discrete Suffix – T4
Analog Suffix – R or RK

Figure 3. DPAK
16 mm



Discrete, Analog
Suffix – T5

Figure 4. DPAK
16 mm

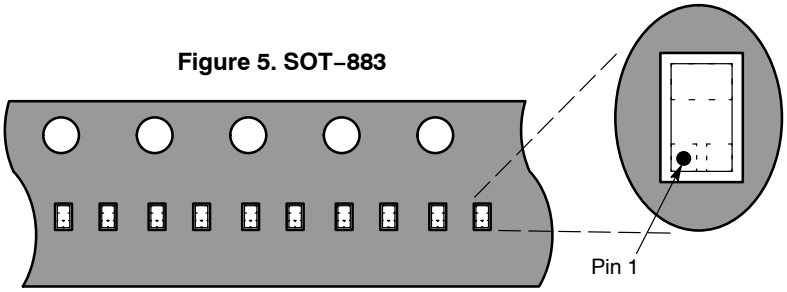


Discrete Suffix – RL

Product Orientation (continued)

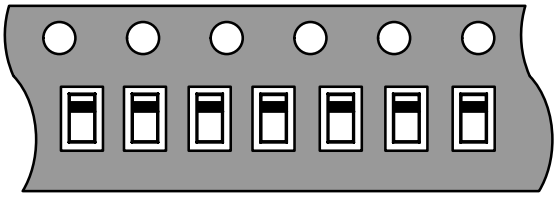
Direction of Feed

Figure 5. SOT−883



"T5" Pin One Opposing Sprocket Hole (8k Reel)

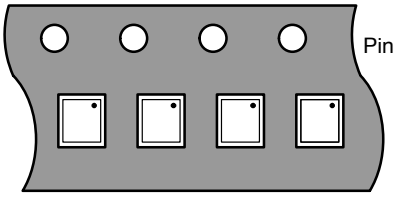
Figure 6. DSN



Die orientation in tape with pads down
"T5" Pin One Towards Sprocket Hole (5k Reel)

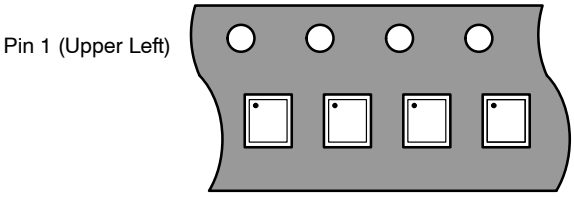
Figure 7. 6−Bump, 9−Bump, 10−Bump
Flip−Chip/DCA

Option 1, 3



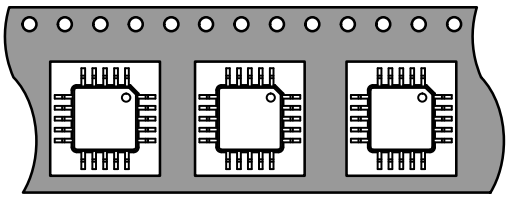
Die orientation in tape with bumps down
"T1" Pin One Towards Sprocket Hole (3k Reel)
"T3" Pin One Towards Sprocket Hole (10k Reel)

Option 2, 4



Die orientation in tape with bumps down
"T2" Pin One Towards Sprocket Hole (3k Reel)
"T4" Pin One Towards Sprocket Hole (10k Reel)

Figure 8. LQFP, TQFP

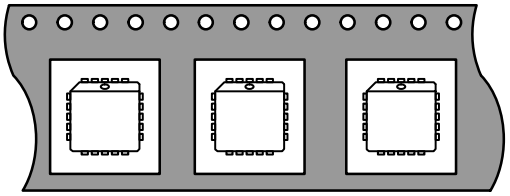


Pin 1 (Upper Right)

R2, R48 − Analog
R2 − Clock & Data Mgt.

Figure 9. PLCC

PLCC−20	**PLCC−28**	**PLCC−44, PLCC−52**	**PLCC−68, PLCC−84**
16 mm	24 mm	32 mm	44 mm



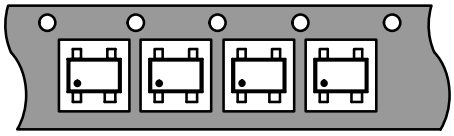
Pin 1 (Upper Center)

R2, R28, R44 − Analog
R2 − Clock & Data Mgt.

Product Orientation (continued)

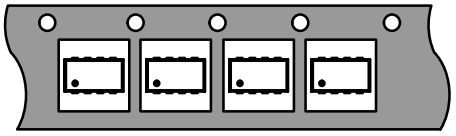
Direction of Feed

Figure 10. SC82 / SC82−AB
"TR" Suffix − Option 1, 3



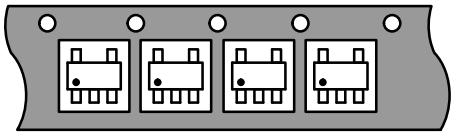
"T1" Pin One Opposing Sprocket Hole (3k Reel)
"T3" Pin One Opposing Sprocket Hole (10k Reel)

Figure 11. ChipFET (8−Lead)
"T1" Suffix − Option 1



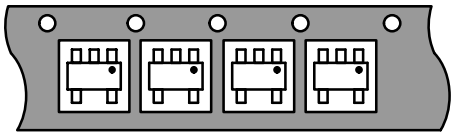
"T1" Pin One Opposing Sprocket Hole (3k Reel)

Figure 12. TSOP−5 / SOT23−5 / SC−74A
"T" or "TR" Suffix − Option 1, 3



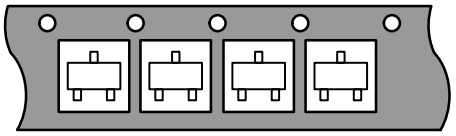
"T1" Pin One Opposing Sprocket Hole (3k Reel)
"T3" Pin One Opposing Sprocket Hole (10k Reel)

Option 2



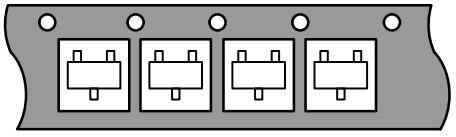
"T2" Pin One Toward Sprocket Hole (3k Reel)

Figure 13. SOT−23 / SOT−23L / SOT−323 / SOT−723 / SC−59 / SC−70 / SC−75 / SC−89
"T5", "TR" or "R2" Suffix − Option 1, 3



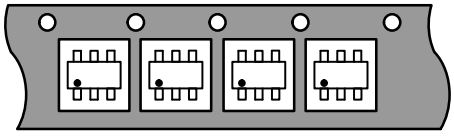
"T1" Single Lead Toward Sprocket Hole (3k Reel)
"T5" Single Lead Toward Sprocket Hole (8k Reel)
"T3" Single Lead Toward Sprocket Hole (10k Reel)

Option 2



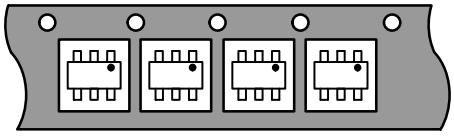
"T2" Single Lead Opposing Sprocket Hole (3k Reel)
(This Orientation Applies to SC−59 Only)

Figure 14. TSOP−6 / SOT23−6 / SC−74
"T" or "TR" Suffix − Option 1, 3



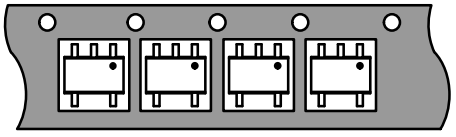
"T1" Pin One Opposing Sprocket Hole (3k Reel)
"T3" Pin One Opposing Sprocket Hole (10k Reel)

Option 2



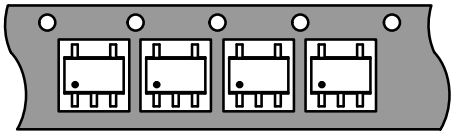
"T2" Pin One Toward Sprocket Hole (3k Reel)

Figure 15. SC−88A / SC70−5 / SOT−353
Option 1, 3



"T1" Pin One Toward Sprocket Hole (3k Reel)
"T3" Pin One Toward Sprocket Hole (10k Reel)

Option 2, 4



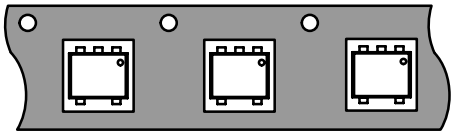
"T2" Pin One Opposing Sprocket Hole (3k Reel)
"T4" Pin One Opposing Sprocket Hole (10k Reel)

Product Orientation (continued)

Direction of Feed

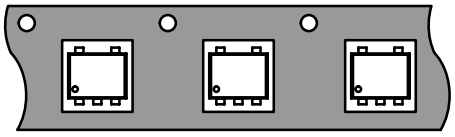
Figure 16. SOT−553

Option 1



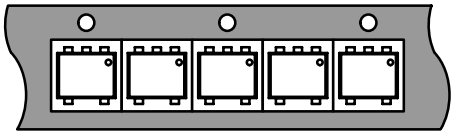
"T1" Pin One Toward Sprocket Hole (4k Reel)

Option 2



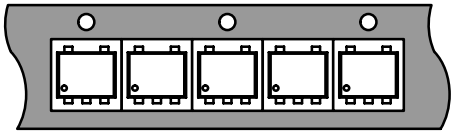
"T2" Pin One Opposing Sprocket Hole (4k Reel)

Option 5



"T5" Pin One Toward Sprocket Hole (8k Reel)

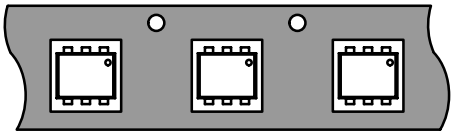
Option 6



"T6" Pin One Opposing Sprocket Hole (8k Reel)

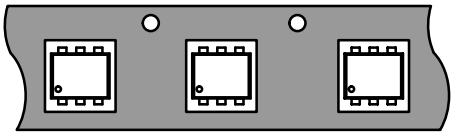
Figure 17. SOT−563

Option 1



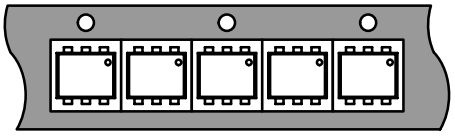
"T1" Pin One Toward Sprocket Hole (4k Reel)

Option 2



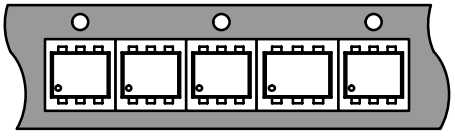
"T2" Pin One Opposing Sprocket Hole (4k Reel)

Option 5



"T5" Pin One Toward Sprocket Hole (8k Reel)

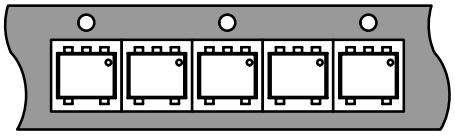
Option 6



"T6" Pin One Opposing Sprocket Hole (8k Reel)

Figure 18. SOT−953

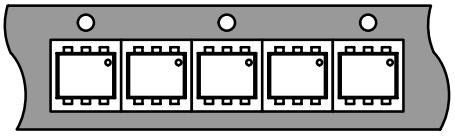
Option 5



"T5" Pin One Toward Sprocket Hole (8k Reel)

Figure 19. SOT−963

Option 5



"T5" Pin One Toward Sprocket Hole (8k Reel)

Figure 20. POWERMITE®

"T1" Suffix − Option 1

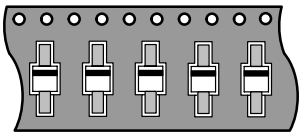
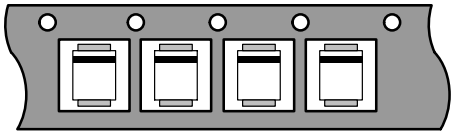


Figure 21. SMA, SMB, SMC

"TR" or "R2" Suffix − Option 1, 3



Unidirectional

SMA: "T1" Cathode Toward Sprocket Hole (1.5k Reel)
"T3" Cathode Toward Sprocket Hole (5k Reel)

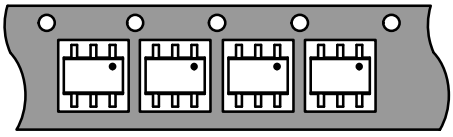
SMB/SMC: "T1" Cathode Toward Sprocket Hole (1k Reel)
"T3" Cathode Toward Sprocket Hole (2.5k Reel)

Bidirectional

Same as above except no orientation

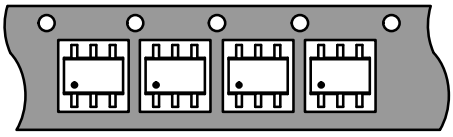
Direction of Feed

Figure 22. SC−88 / SC70−6 / SOT−363
Option 1, 3



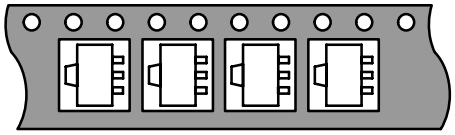
"T1" Pin One Toward Sprocket Hole (3k Reel)
"T3" Pin One Toward Sprocket Hole (10k Reel)

Option 2



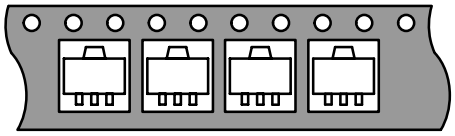
"T2" Pin One Opposing Sprocket Hole (3k Reel)

Figure 23. SOT−89
"R1" Suffix



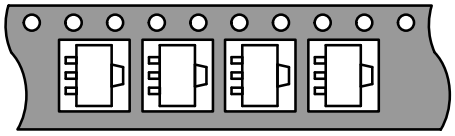
"R1" Pin One Opposing Sprocket Hole (1k Reel)

"T1" Suffix



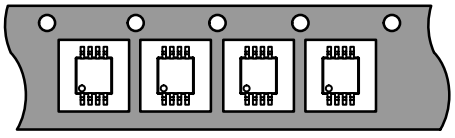
"T1" Single Lead Toward Sprocket Hole (1k Reel)

"T2" Suffix



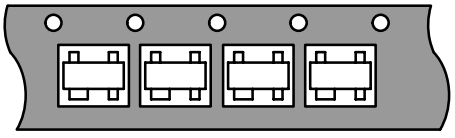
"T2" Single Lead Opposing Sprocket Hole (1k Reel)

Figure 24. ULTRA SMALL 8



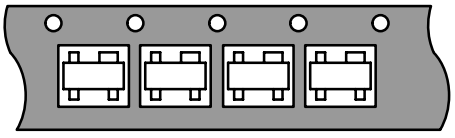
Pin One Opposing Sprocket Hole (3k Reel)

Figure 25. SOT−143
"T" or "TR" Suffix − Option 1, 3



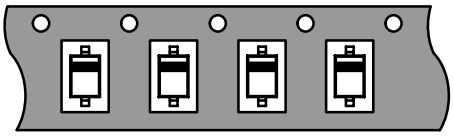
"T1" Wide Lead Tape Opposing Sprocket Hole (3k Reel)
"T3" Wide Lead Tape Opposing Sprocket Hole (10k Reel)

Option 2, 4



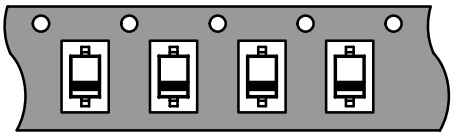
"T2" Wide Lead Tape Toward Sprocket Hole (3k Reel)
"T4" Wide Lead Tape Toward Sprocket Hole (10k Reel)

Figure 26. SOD−123 / SOD−323
Option 1, 3



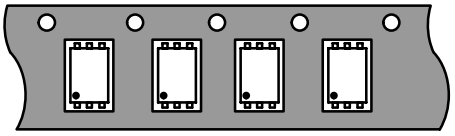
"T1" Cathode Lead Toward Sprocket Hole (3k Reel)
"T3" Cathode Lead Toward Sprocket Hole (10k Reel)

Option 2



"T2" Cathode Lead Opposing Sprocket Hole (3k Reel)

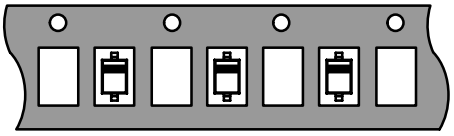
Figure 27. SON−6



Product Orientation (continued)

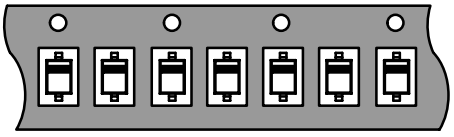
Direction of Feed

Figure 28. SOD−523
Option 1



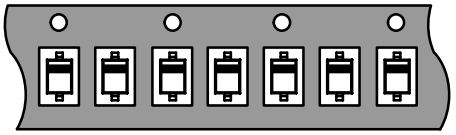
"T1" Cathode Lead Toward Sprocket Hole (3k Reel)

Option 5



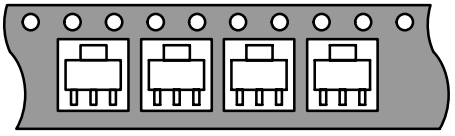
"T5" Cathode Lead Toward Sprocket Hole (8k Reel)

Figure 29. SOD−723, SOD−923
Option 5



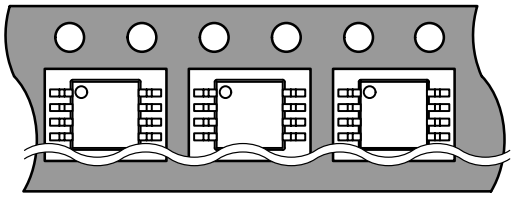
"T5" Cathode Lead Toward Sprocket Hole (8k Reel)

Figure 30. SOT−223



"T1" Single Lead Toward Sprocket Hole (1k Reel)
"T3" Single Lead Toward Sprocket Hole (4k Reel)
"R3" Single Lead Toward Sprocket Hole (2.5k Reel)

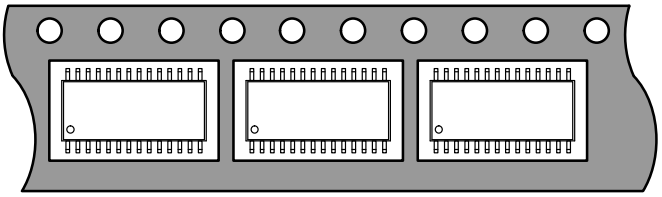
Figure 31. Micro8™ / Micro10 / SOIC / SO / TSSOP / SOP / SSOP



Pin 1 (Upper Left)

R2 − Clock & Data Mgt.
R or R2 − Analog
T3 − EEPROM

Figure 32. SO−28W
32 mm



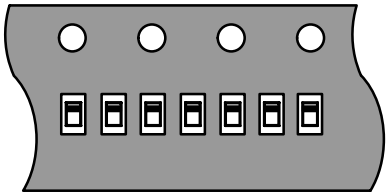
R3 − Analog

Product Orientation (continued)

Direction of Feed

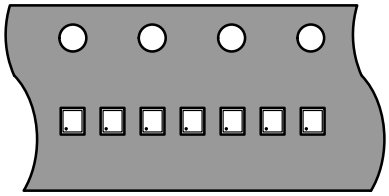
Leadless Packages

Figure 33. X3DFN



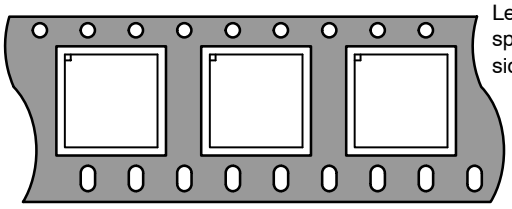
T5 − Cathode Band Toward Sprocket Hole (15k Reel)

Figure 34. XLLGA



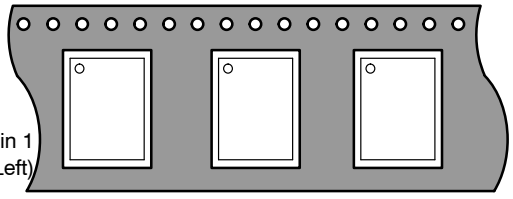
T5 − Pin One Opposing Sprocket Hole (8k Reel)

Figure 35. FCBGA (BGA)



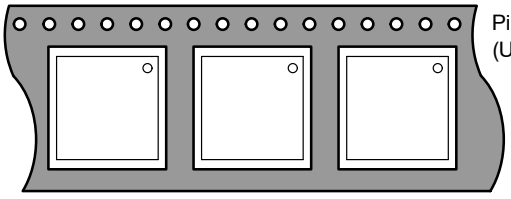
TA, TW

Figure 36. DFN/QFN/WLCSP−4



TA, TW, TR

Figure 37. DFN/QFN (LPCC)/WLCSP−5



TB, TX, TR

Package	Pre Jan 2007	Post Jan 2007
DFN / QFN Square (LPCC)	T1	TB, TX
	T4	TB, TX
	R2	TB, TX
DFN / QFN Rectangular (LPCC)	T1	TA, TW
	R2	TA, TW
DFN / QFN	T2	TA, TW
	R2	TA, TW
FCBGA / BGA	R2	TA, TW
WLCSP	−	TR

Leadless Package Pin 1 Orientation for Tape and Reel (QFN, DFN, FCBGA, BGA, LPCC)

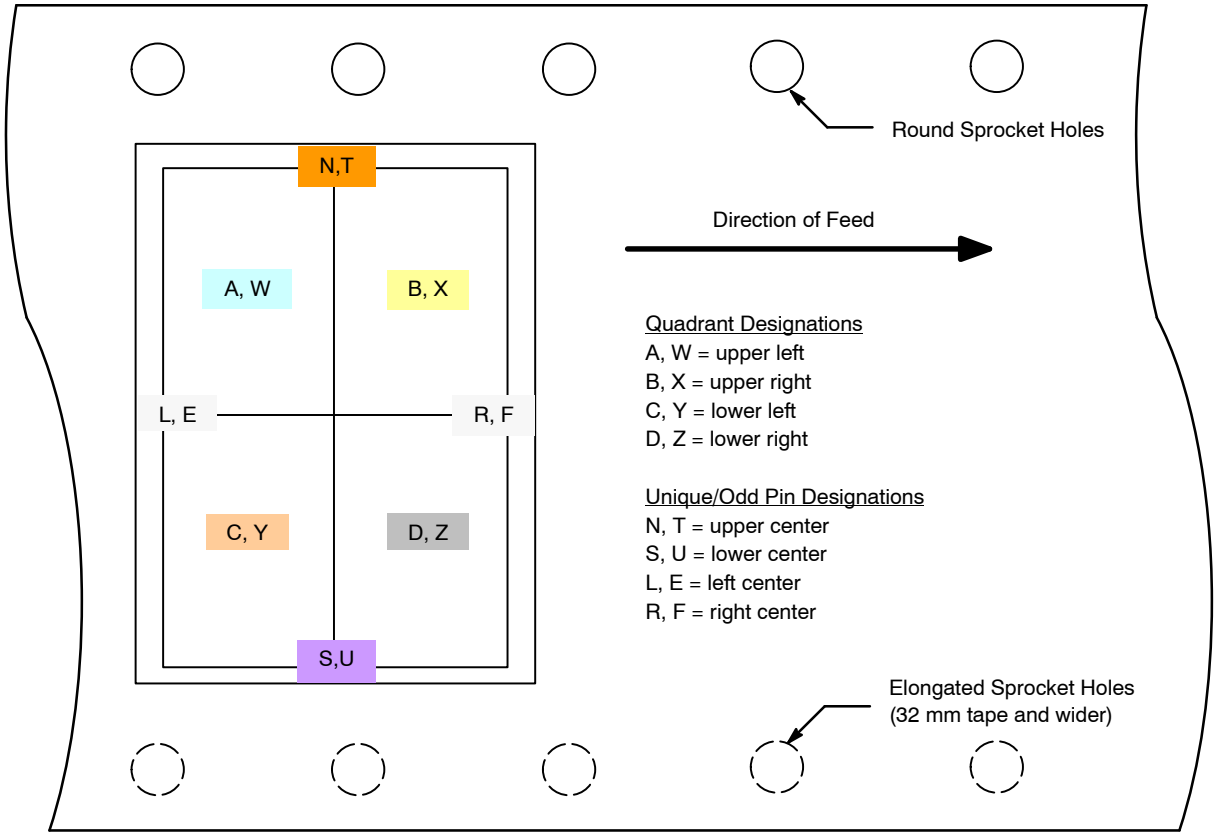
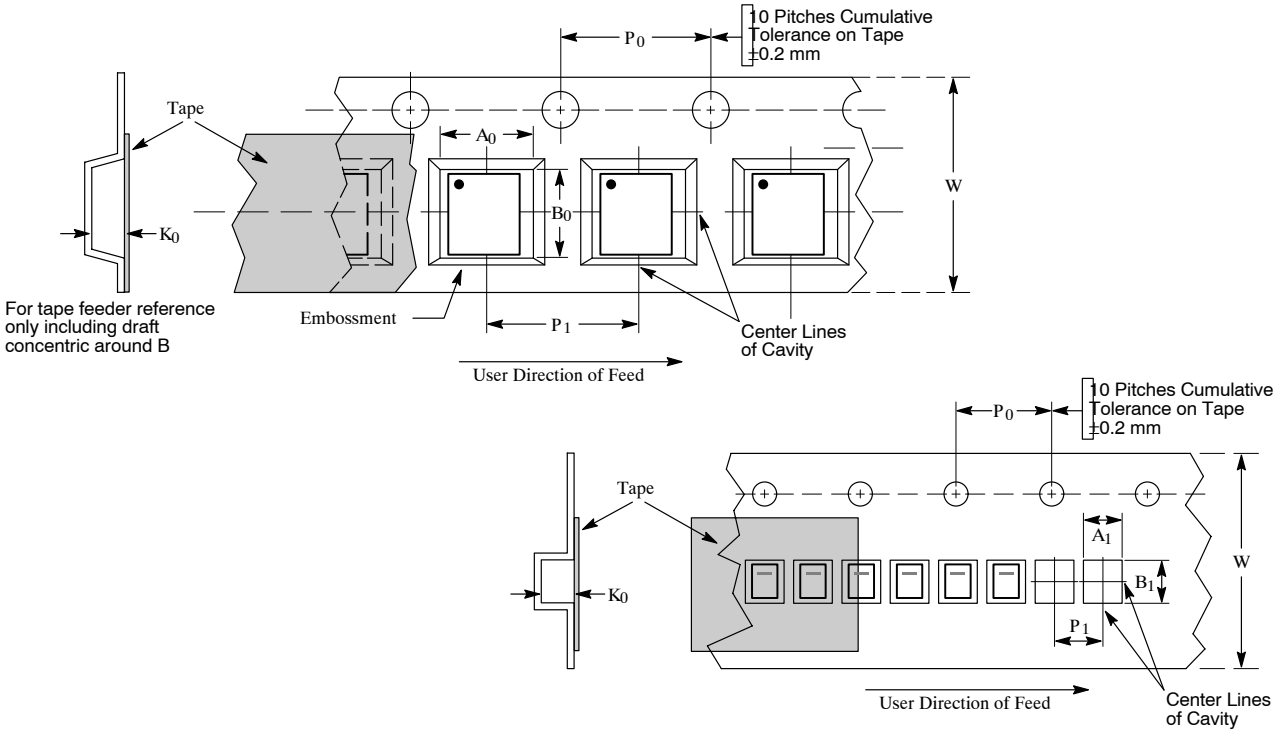


Figure 38. Leadless Package Pin 1 Orientation for Tape and Reel (Effective January 2007)

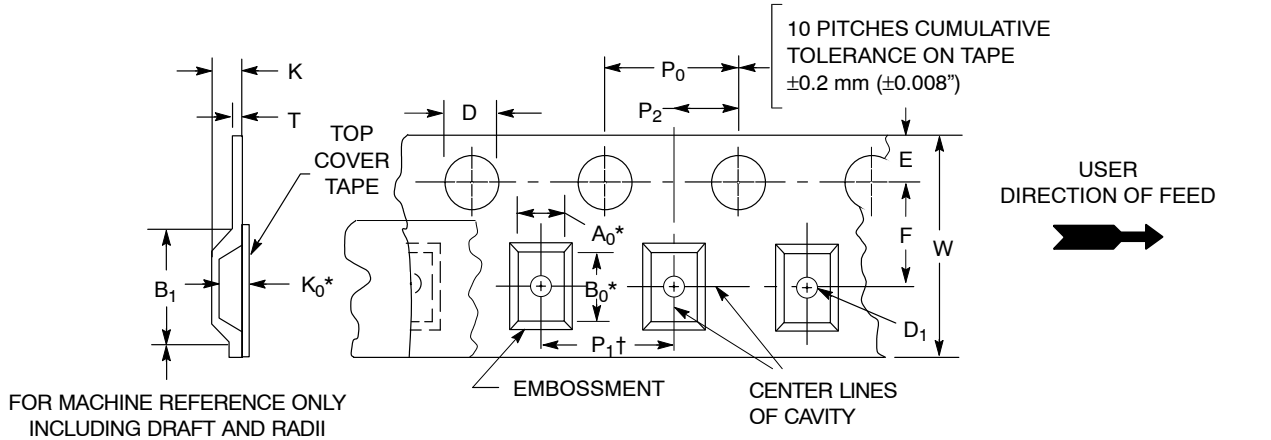
Part Number Suffix				
Shipping Type*	**Pin1 Location**	**Blank or Pb−Free**	**Remark:**	**Reel Size (mm) diameter**
T	A	G	Quadrant 1−upper left	177
T	B	G	Quadrant 2−−upper right	178
T	C	G	Quadrant 3−−lower left	178
T	D	G	Quadrant 4−−lower right	178
T	W	G	Quadrant 1−upper left	330
T	X	G	Quadrant 2−−upper right	330
T	Y	G	Quadrant 3−−lower left	330
T	Z	G	Quadrant 4−−lower right	330
T	N	G	North (upper center)	178
T	S	G	South (lower center)	178
T	T	G	Top (upper center)	330
T	U	G	Under (lower center)	330
T	L	G	Left center	178
T	R	G	Right center	178
T	E	G	Left center	330
T	F	G	Right center	330

*T = Tape

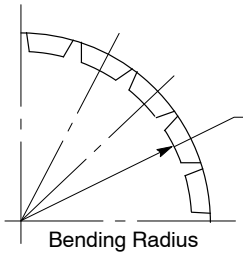
Tape and Reel Dimensions and Orientation for Former CMD Devices

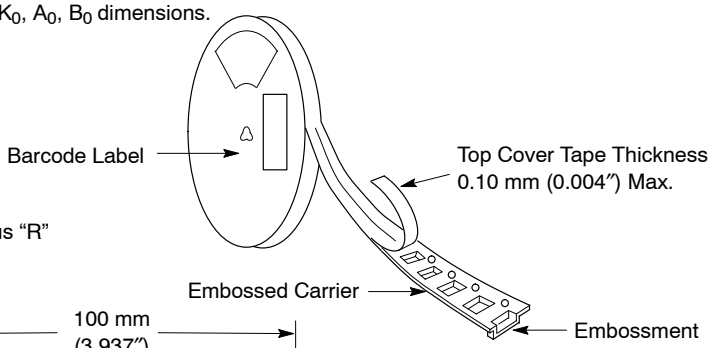


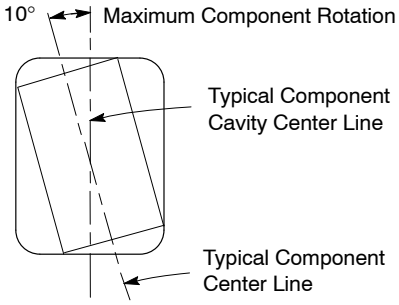
Embossed Tape and Reel Data Carrier Tape Specifications

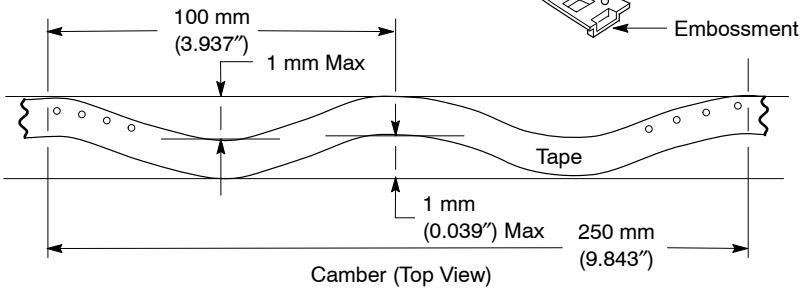


†See Note 1 below for P_1 dimension.
*See Note 2 below for K_0, A_0, B_0 dimensions.









Camber (Top View)
Allowable Camber To Be 1 mm/100 mm Nonaccumulative Over 250 mm

DIMENSIONS

Tape Size (W)	B_1 Max (Note 1)	D	D_1	E	F	K	P_0	P_2	R Min	T Max	W Max
8 mm	4.55 mm (0.179″)	1.5 + 0.1 mm − 0.0 (0.059 + 0.004″ − 0.0)	1.0 Min (0.039″) or 0.5 mm Min (0.020″) or 0.2 mm Min (0.008″)	1.75 ± 0.1 mm (0.069 ± 0.004″)	3.5 ± 0.05 mm (0.138 ± 0.002″)	2.4 mm Max (0.094″)	4.0 ± 0.1 mm (0.157 ± 0.004″)	2.0 ± 0.1 mm (0.079 ± 0.002″)	25 mm (0.98″)	0.6 mm (0.024″)	8.3 mm (0.327″)
12 mm	8.2 mm (0.323″)		1.5 mm Min (0.060″)		5.5 ± 0.05 mm (0.217 ± 0.002″)	6.4 mm Max (0.252″)			30 mm (1.18″)		12 ± 0.30 mm (0.470 ± 0.012″)
16 mm	12.1 mm (0.476″)				7.5 ± 0.10 mm (0.295 ± 0.004″)	7.9 mm Max (0.311″)					16.3 mm (0.642″)
24 mm	20.1 mm (0.791)				11.5 ± 0.1 mm (0.453 ± 0.004″)	11.9 mm Max (0.468″)					24.3 mm (0.957″)

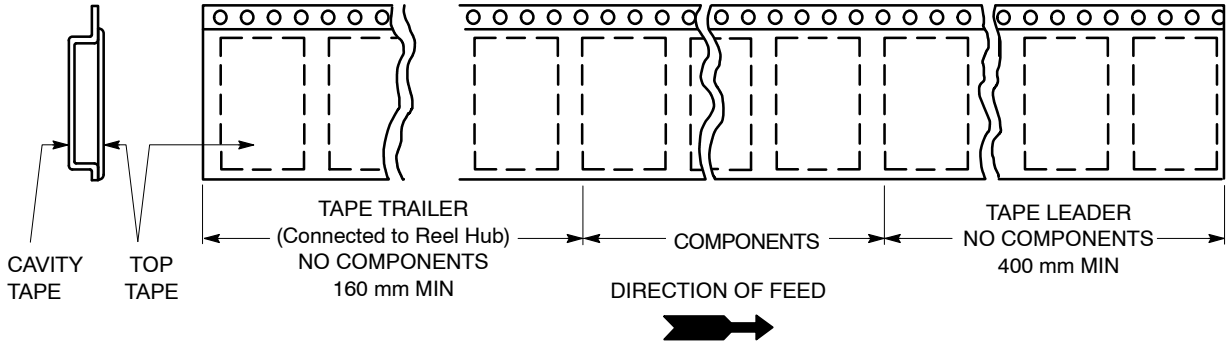
Metric dimensions govern − English are in parentheses for reference only.

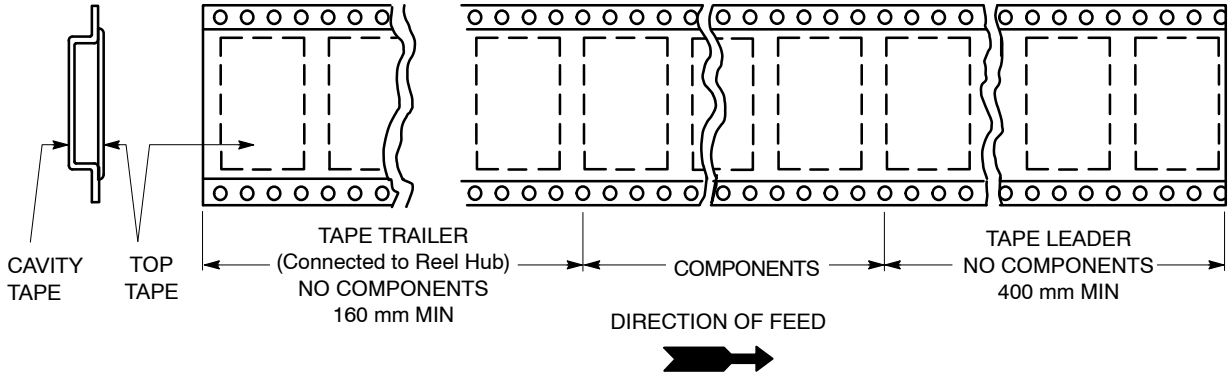
1. Pitch information (dimension P_1) is contained in the embossed tape and reel ordering information beginning on Page 5.
2. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity.

Tape Ends for Finished Goods

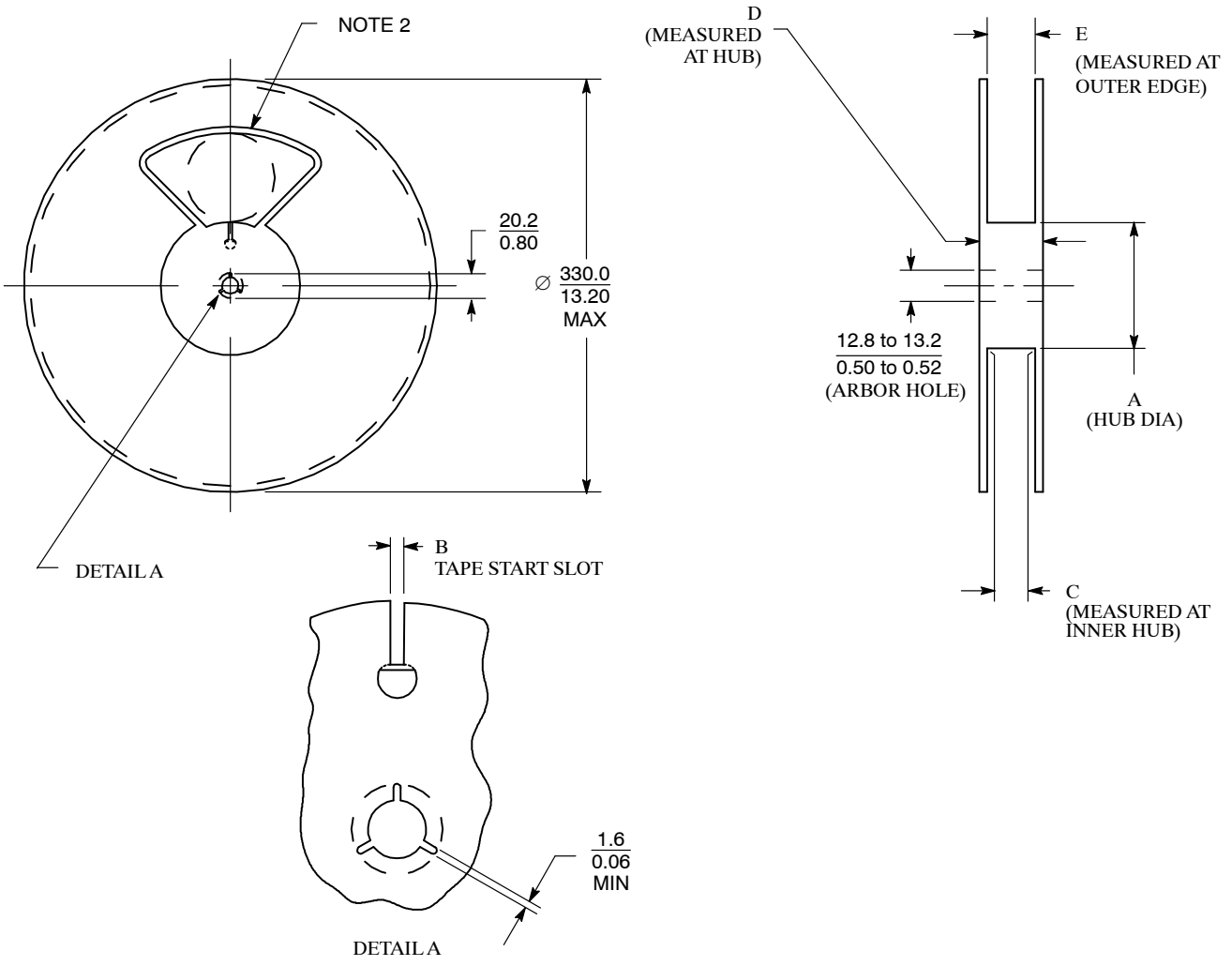
Leader and Trailer

The TRAILER is a minimum of 160 mm in length and it consists of empty cavities with sealed cover tape.
The LEADER is a minimum of 400 mm in length and it consists of empty cavities with sealed cover tape.





Reel Dimensions



Reel Diameter	Tape Size	A mm (inches)		B mm (inches)		C mm (inches)		D	E
		Min	Max	Min	Max	Min	Max	(Max)	(Max)
178.0 (7.01)	16.0 (0.63)		50.0 (1.97)	6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)	178.0 (7.01)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	56.0 (2.20)	150.0 (5.91)		10.0 (0.39)	11.0 (0.43)	56.4 (2.22)	58.4 (2.30)	62.4 (2.46)	59.4 (2.34)
330.0 (12.99)	44.0 (1.73)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	44.4 (1.75)	46.4 (1.83)	62.4 (2.46)	47.4 (1.87)
330.0 (12.99)	32.0 (1.26)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	32.4 (1.28)	34.4 (1.35)	38.4 (1.51)	35.4 (1.39)
330.0 (12.99)	24.0 (0.94)	60.0 (2.36)		9.5 (0.37)	10.5 (0.41)	24.4 (0.96)	26.4 (1.04)	30.4 (1.51)	27.4 (1.08)
330.0 (12.99)	16.0 (0.63)			6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)			4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.01)	12.0 (0.47)	50.0 (1.97)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.47)	10.9 (0.43)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)

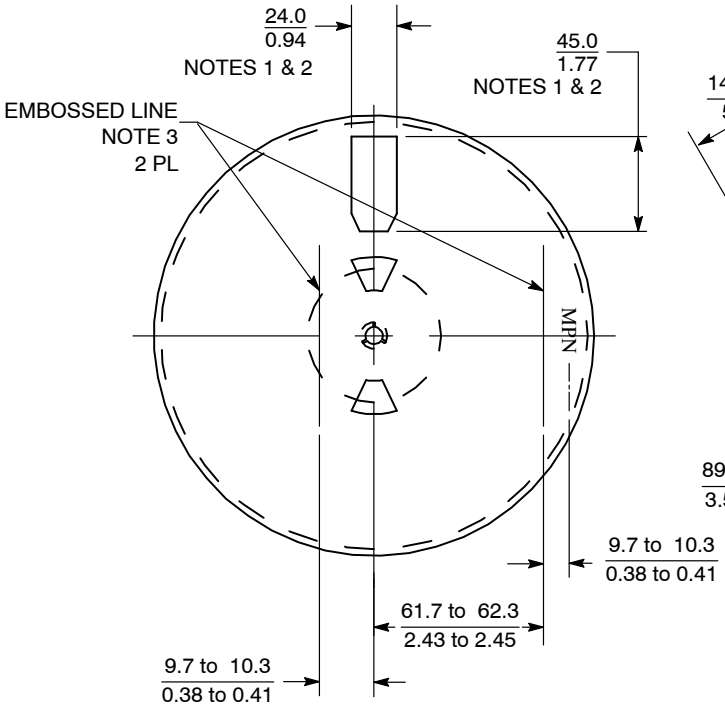


Figure 39. Front View of 178 mm (7.0 in) Reel

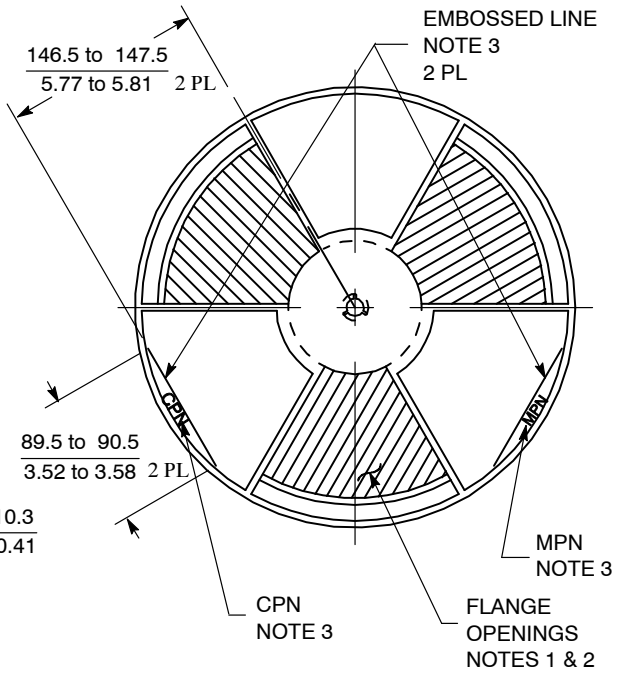


Figure 40. Front View of 330 mm (12.99 in) Reel

NOTES:

1. LABEL PLACEMENT AREA:
   - All reels must have flat area on the front flange of the reel that will fit two 41.3 mm (1.65 in) by 125 mm (4.90 in) ON Semiconductor barcode labels.
   - If there are any flange openings on the front side of the 178 mm (7.00 in) reel they must be designed in locations so that two of the 41.3 mm (1.65 in) ON Semiconductor barcode labels can be applied parallel to each other as in Figure 39.
   - If there are any flange opening on the front flange of the 330 mm (13.0 in) reel they must be designed in locations so that two of the 41.3 mm (1.65 in) by 125 mm (4.90 in) ON Semiconductor barcode labels can be applied parallel to each other as in Figure 40.
2. FLANGE OPENINGS
   - Flange opening on the front and the back of the reel are a supplier option but must meet all of the requirements in Note 1. The preferred size for the 176 mm (7.0 in) reel is shown in Figure 39.
   - The tape loading opening must be as in Detail A.
3. GRAPHICS:
   - The letters MPN and CPN are a option. The size and thickness of the letters are the manufacturer's option and are not to be used for inspection criteria.
   - The embossed lines on the reel are a option. If the lines are used they must be located as in Figure 39 and 40. They must be a minimum 38 mm (1.50 in) long. The thickness is a manufacturer's option and not to be used for inspection criteria.

Reel Labeling

Place the reel on an ESD protective surface so that the round sprocket holes are on the bottom. The direction of travel when unwound should be from the top right quadrant. See illustration below.

REEL WINDING DIRECTION

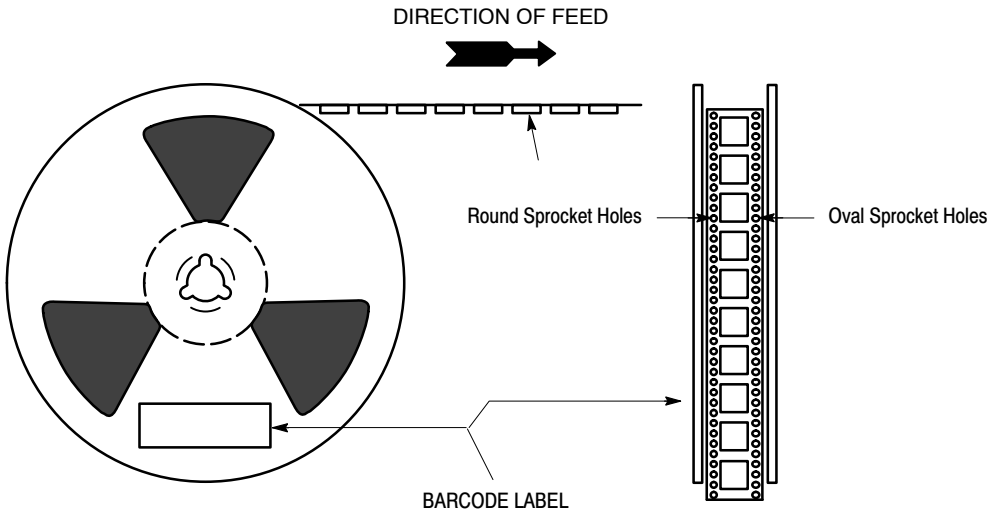


Figure 41. Round and Oval Sprocket Holes Used with 32 mm, 42 mm, 44 mm and 52 mm Tape (holes on both sides)

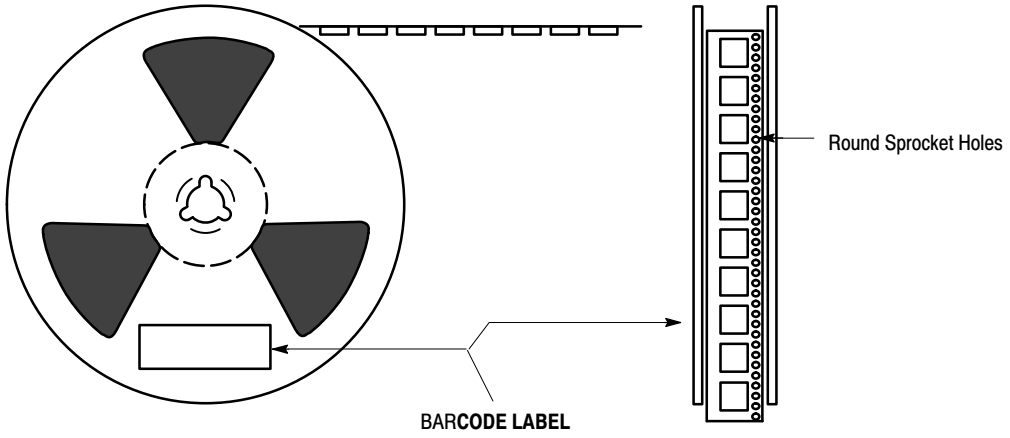
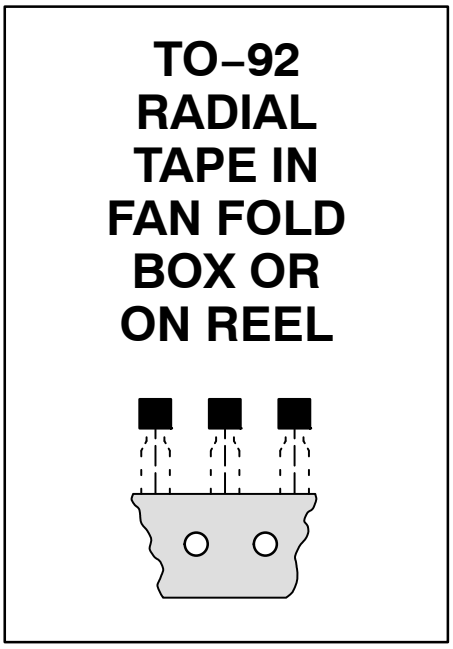


Figure 42. Round Sprocket Holes Used with 8 mm, 12 mm,16 mm and 24 mm Tape (holes on one side only)

TO−92 EIA, IEC, EIAJ Radial Tape in Fan Fold Box or On Reel



Radial tape in fan fold box or on reel of the reliable TO−92 package are the best methods of capturing devices for automatic insertion in printed circuit boards. These methods of taping are compatible with various equipment for active and passive component insertion.

- Available in Fan Fold Box
- Available on 365 mm Reels
- Accommodates All Standard Inserters
- Allows Flexible Circuit Board Layout
- 2.5 mm Pin Spacing for Soldering
- EIA−468, IEC 286−2, EIAJ RC1008B

Ordering Notes:

When ordering radial tape in fan fold box or on reel, specify the style per Figures 44, 45, 51 and 52. Add the suffix “RLR” and “Style” to the device title, i.e. 2N5060RLRA. This will be a standard 2N5060 radial taped and supplied on a reel. Some products only utilize the last 2 digits. Please refer to the ON Semiconductor device data sheet for exact ordering information.

- Fan Fold Box Information − Minimum order quantity 1 Box. Order in increments of 2000.
- Reel Information − Minimum order quantity 1 Reel. Order in increments of 2000.

US/EUROPEAN SUFFIX CONVERSIONS

U.S.	Europe	Package Style
RLRA, RA	RL	Reel
RLRE, RE	RL1	Reel
RLRM, RM	ZL1	Fan Fold
RLRP, RP	–	Fan Fold

TO−92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL

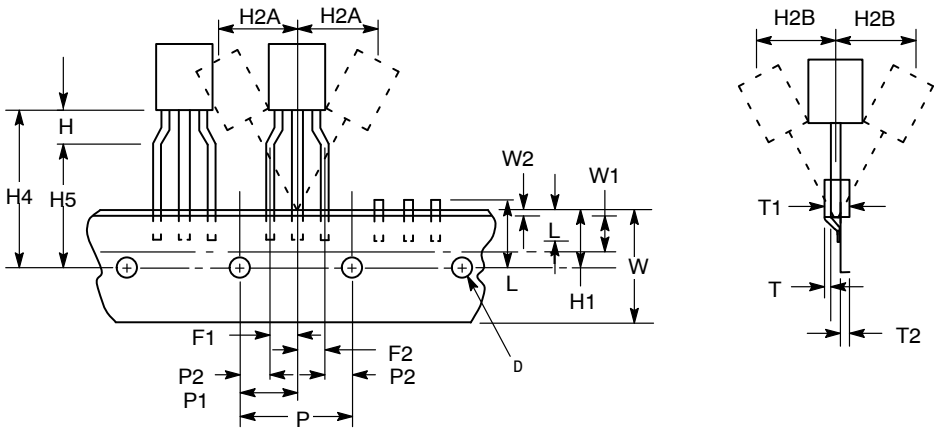


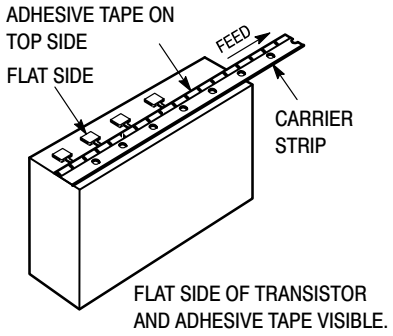
Figure 43. Device Positioning on Tape

Symbol	Item	Specification			
		Inches		Millimeter	
		Min	Max	Min	Max
D	Tape Feedhole Diameter	0.1496	0.1653	3.8	4.2
D2	Component Lead Thickness Dimension	0.015	0.020	0.38	0.51
F1, F2	Component Lead Pitch	0.0945	0.110	2.4	2.8
H	Bottom of Component to Seating Plane	0.059	0.156	1.5	4.0
H1	Feedhole Location	0.3346	0.3741	8.5	9.5
H2A	Deflection Left or Right	0	0.039	0	1.0
H2B	Deflection Front or Rear	0	0.051	0	1.0
H4	Feedhole to Bottom of Component	0.7086	0.768	18	19.5
H5	Feedhole to Seating Plane	0.610	0.649	15.5	16.5
L	Defective Unit Clipped Dimension	0.3346	0.433	8.5	11
L1	Lead Wire Enclosure	0.09842	–	2.5	–
P	Feedhole Pitch	0.4921	0.5079	12.5	12.9
P1	Feedhole Center to Center Lead	0.2342	0.2658	5.95	6.75
P2	First Lead Spacing Dimension	0.1397	0.1556	3.55	3.95
T	Adhesive Tape Thickness	0.06	0.08	0.15	0.20
T1	Overall Taped Package Thickness	–	0.0567	–	1.44
T2	Carrier Strip Thickness	0.014	0.027	0.35	0.65
W	Carrier Strip Width	0.6889	0.7481	17.5	19
W1	Adhesive Tape Width	0.2165	0.2841	5.5	6.3
W2	Adhesive Tape Position	0.0059	0.01968	0.15	0.5

3. Maximum alignment deviation between leads not to be greater than 0.2 mm.
4. Defective components shall be clipped from the carrier tape such that the remaining protrusion (L) does not exceed a maximum of 11 mm.
5. Component lead to tape adhesion must meet the pull test requirements established in Figures 47, 48 and 49.
6. Maximum non−cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
7. Hold down tape not to extend beyond the edge(s) of carrier tape and there shall be no exposure of adhesive.
8. No more than 1 consecutive missing component is permitted.
9. A tape trailer and leader, having at least three feed holes is required before the first and after the last component.
10. Splices will not interfere with the sprocket feed holes.

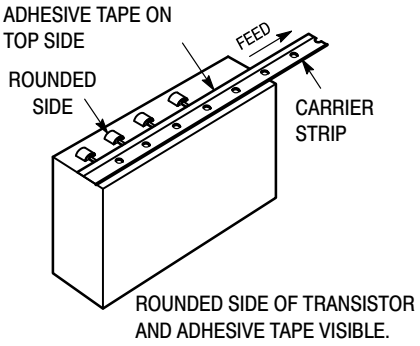
TO−92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL

FAN FOLD BOX STYLES



Style M fan fold box is equivalent to styles E and F of reel pack dependent on feed orientation from box.

Figure 44. Style RLRM, RM



Style P fan fold box is equivalent to styles A and B of reel pack dependent on feed orientation from box.

Figure 45. Style RLRP, RP

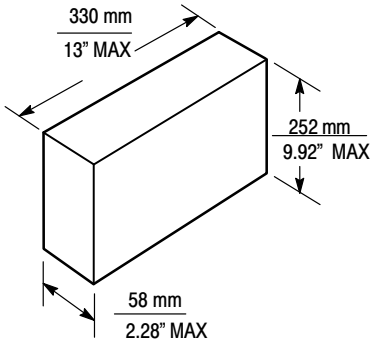
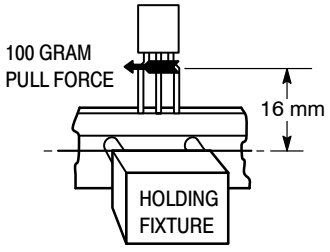


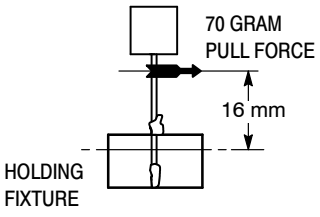
Figure 46. Fan Fold Box Dimensions

ADHESION PULL TESTS



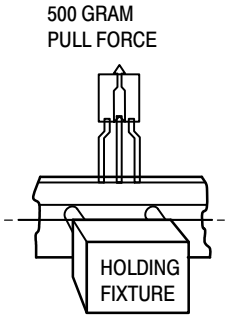
The component shall not pull free with a 300 gram load applied to the leads for 3 ± 1 second.

Figure 47. Test #1



The component shall not pull free with a 70 gram load applied to the leads for 3 ± 1 second.

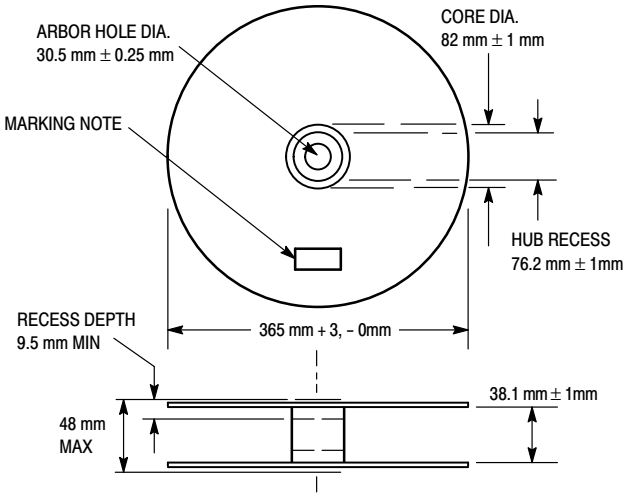
Figure 48. Test #2



There shall be no deviation in the leads and no component leads shall be pulled free of the tape with a 500 gram load applied to the component body for 3 ± 1 second.

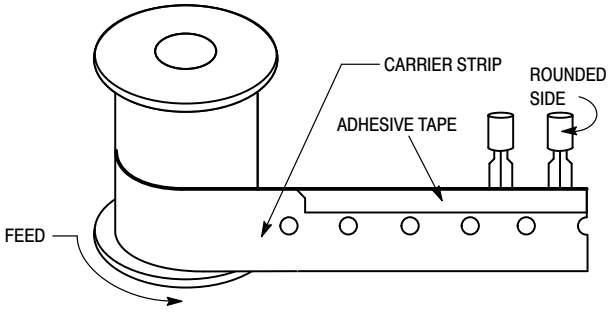
Figure 49. Test #3

TO−92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL: REEL STYLES



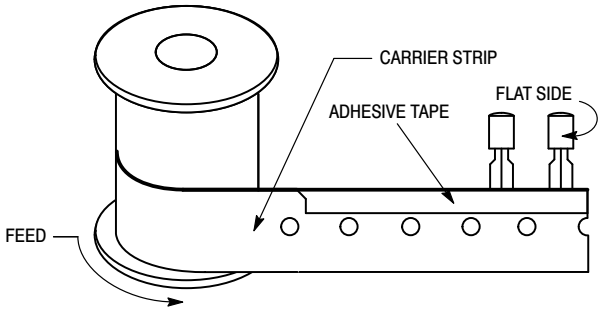
Material used must not cause deterioration of components or degrade lead solderability

Figure 50. Reel Specifications



Rounded side of transistor and adhesive tape visible.

Figure 51. Style RLRA, RA



Flat side of transistor and adhesive tape visible.

Figure 52. Style RLRE, RE

Lead Tape Packaging Standards for Axial−Lead Components

1.0 SCOPE

This section covers packaging requirements for the following axial-lead component's use in automatic testing and assembly equipment: ON Semiconductor Case 17-02, Case 41A-02, Case 51-02 (DO-7), Case 59-03 (DO-41), Case 59-04, Case 194-04 and Case 299-02 (DO-35). Packaging, as covered in this section, shall consist of axial-lead components mounted by their leads on pressure sensitive tape, wound onto a reel.

2.0 PURPOSE

This section establishes ON Semiconductor standard practices for lead-tape packaging of axial-lead components and meets the requirements of EIA Standard RS-296-D "Lead-taping of Components on Axial Lead Configuration for Automatic Insertion," level 1.

3.0 REQUIREMENTS

3.1 Component Leads

3.1.1 – Component leads shall not be bent beyond dimension E from their normal position. See Figure 54.

3.1.2 – The "C" dimension shall be governed by the overall length of the reel packaged component. The distance between flanges shall be 0.059 inch to 0.315 inch greater than the overall component length. See Figures 54 and 55.

3.1.3 – Cumulative dimension "A" tolerance shall not exceed 0.059 over 6 in consecutive components.

3.2 Orientation

All polarized components must be oriented in one direction. The cathode lead tape shall be any color except white and the anode tape shall be white. See Figure 53.

3.3 Reeling

3.3.1 – Components on any reel shall not represent more than two date codes when date code identification is required.

3.3.2 – Component's leads shall be positioned perpendicularly between pairs of 0.250 inch tape. See Figure 54.

3.3.3 – A minimum 12 inch leader of tape shall be provided before the first and last component on the reel.

3.3.4 – 50 lb. Kraft paper is wound between layers of components as far as necessary for component protection.

3.3.5 – Components shall be centered between tapes such that the difference between D1 and D2 does not exceed 0.055.

3.3.6 – Staples shall not be used for splicing. No more than four layers of tape shall be used in any splice area and no tape shall be offset from another by more than 0.031 inch noncumulative. Tape splices shall overlap at least 6 inches for butt joints and at least 3 inches for lap joints and shall not be weaker than unspliced tape.

3.3.7 – Quantity per reel shall be as indicated in Table 1. Orders for tape and reeled product will only be processed and shipped in full reel increments. Scheduled orders must be in releases of full reel increments or multiples thereof.

3.3.8 – A maximum of 0.25% of the components per reel quantity may be missing without consecutive missing per level 1 of RS-296-D.

3.3.9 – The single face roll pad shall be placed around the finished reel and taped securely. Each reel shall then be placed in an appropriate container.

3.4 Marking

Minimum reel and carton marking shall consist of the following (see Figure 55):

ON Semiconductor part number

Quantity

Manufacturer's name

Date codes (when applicable; see note **3.3.1**)

4.0

Requirements differing from this ON Semiconductor standard shall be negotiated with the factory.

The packages indicated in the following table are suitable for lead tape packaging. Table 1 indicates the specific devices (transient voltage suppressors and/or Zeners) that can be obtained from ON Semiconductor in reel packaging and provides the appropriate packaging specification.

Lead Tape Packaging Standards for Axial−Lead Components

Table 1. PACKAGING DETAILS (all dimensions in inches)

Case Type	Product Category	Device Title Suffix	MPQ Quantity Per Reel	Component Spacing A Dimension	Tape Spacing B Dimension	Reel Dimension C	Reel Dimension D (Max)	Max Off Alignment E
Case 17	Surmetic 40 & 600 Watt TVS	RL	4000	0.2 ± 0.015	2.062 ± 0.059	3	14	0.047
Case 41A	1500 Watt TVS	RL4	1500	0.4 ± 0.02	2.062 ± 0.059	3	14	0.047
Case 59	DO−41 Glass & DO−41 Surmetic 30	RL	6000	0.2 ± 0.015	2.062 ± 0.059	3	14	0.047
	Rectifier							
Case 59	500 Watt TVS	RL	500	0.2 ± 0.02	2.062 ± 0.059	3	14	0.047
	Rectifier							
Case 194	110 Amp TVS (Automotive)	RL	800	0.4 ± 0.02	1.875 ± 0.059	3	14	0.047
	Rectifier							
Case 267	Rectifier	RL	1500	0.4 ± 0.02	2.062 ± 0.059	3	14	0.047
Case 299	DO−35 Glass	RL	5000	0.2 ± 0.02	2.062 ± 0.059	3	14	0.047
Case 267	Schottky & Ultrafast Rectifiers	RL	1500	0.4 ± 0.02	2.062 ± 0.059	3	14	0.047
Case 267	Fast Recovery & General Purpose Rectifiers	RL	1200	0.4 ± 0.02	2.062 ± 0.059	3	14	0.047

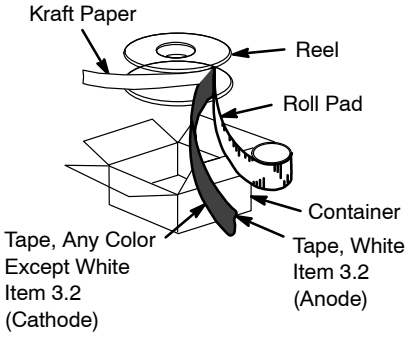


Figure 53. Reel Packing

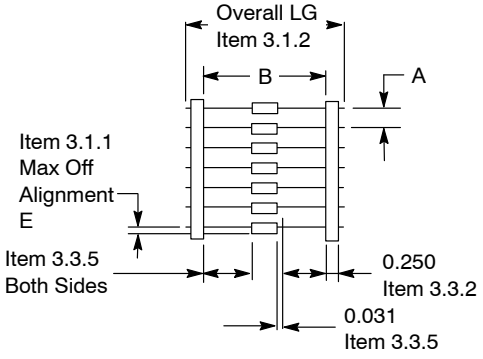


Figure 54. Component Spacing

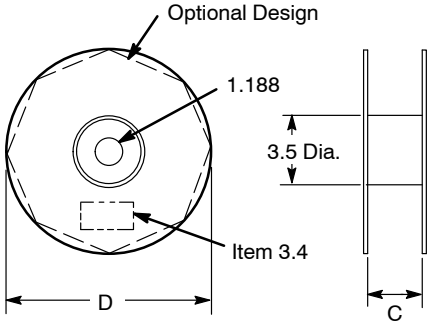


Figure 55. Reel Dimensions (Item references appear on Page 31)

INFORMATION FOR USING SURFACE MOUNT PACKAGES

RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain/collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating ambient temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For example, for a SOT−223 device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{156°C/W} = 800 \text{ milliwatts}$$

The 156°C/W for the SOT−223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 800 milliwatts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain/collector pad. By increasing the area of the drain/collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figures 56, 57 and 58.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

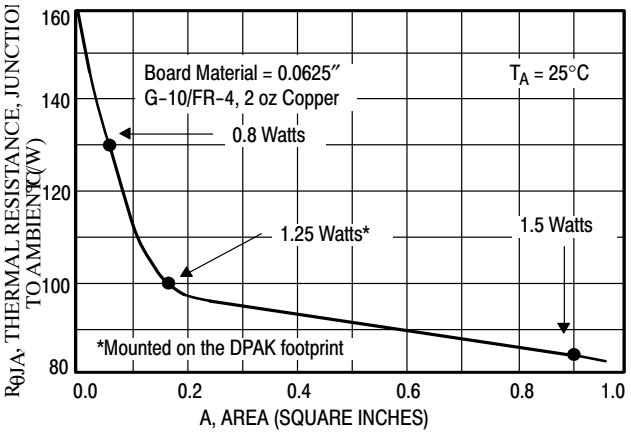


Figure 56. Thermal Resistance versus Drain Pad Area for the SOT−223 Package (Typical)

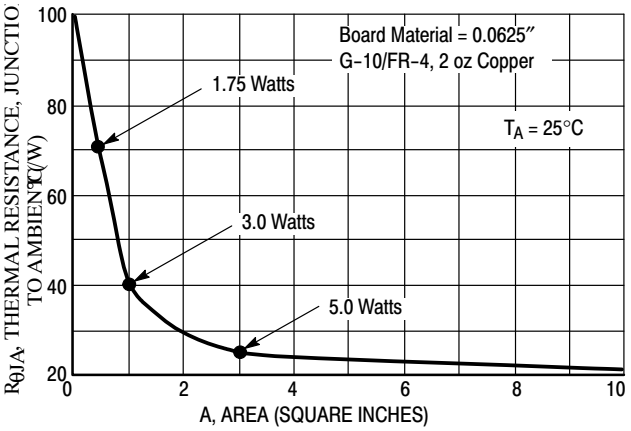


Figure 57. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)

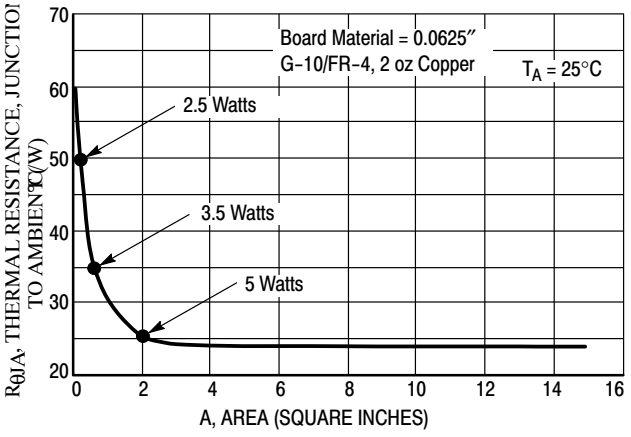


Figure 58. Thermal Resistance versus Drain Pad Area for the D²PAK Package (Typical)

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC−59, SC−70/SOT−323, SOD−123, SOT−23, SOT−143, SOT−223, SO−8, SO−14, SO−16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D^2PAK packages. If a 1:1 opening is used to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 59 shows a typical stencil for the DPAK and D^2PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

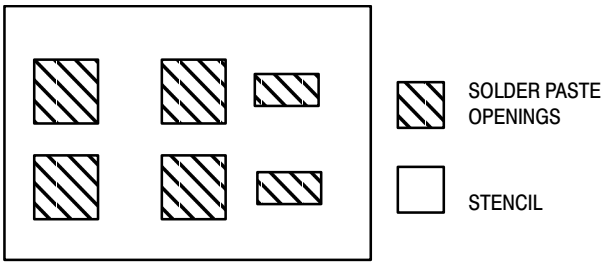


Figure 59. Typical Stencil for DPAK and D^2PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- For wave soldering, the soldering temperature and time should not exceed 260°C for more than 10 seconds. For other reflow methods such as convection and IR ovens, refer to the reflow profiles on the following pages.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used since the use of forced cooling will increase the temperature gradient and will result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 60 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177−189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

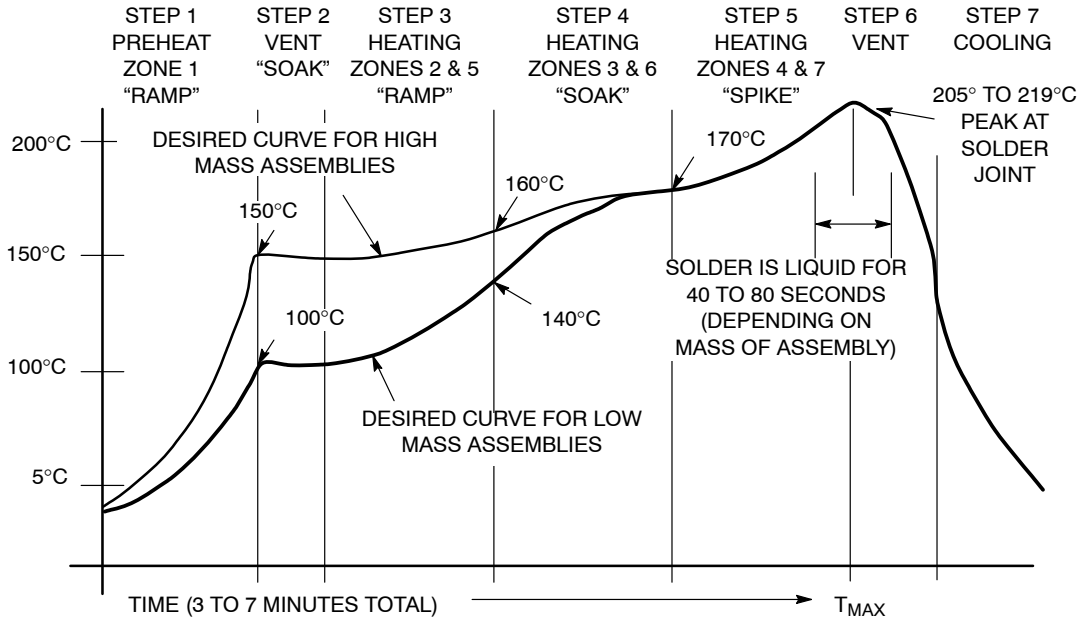


Figure 60. Typical Tin Lead (SnPb) Solder Heating Profile

TYPICAL SOLDER HEATING PROFILE (continued)

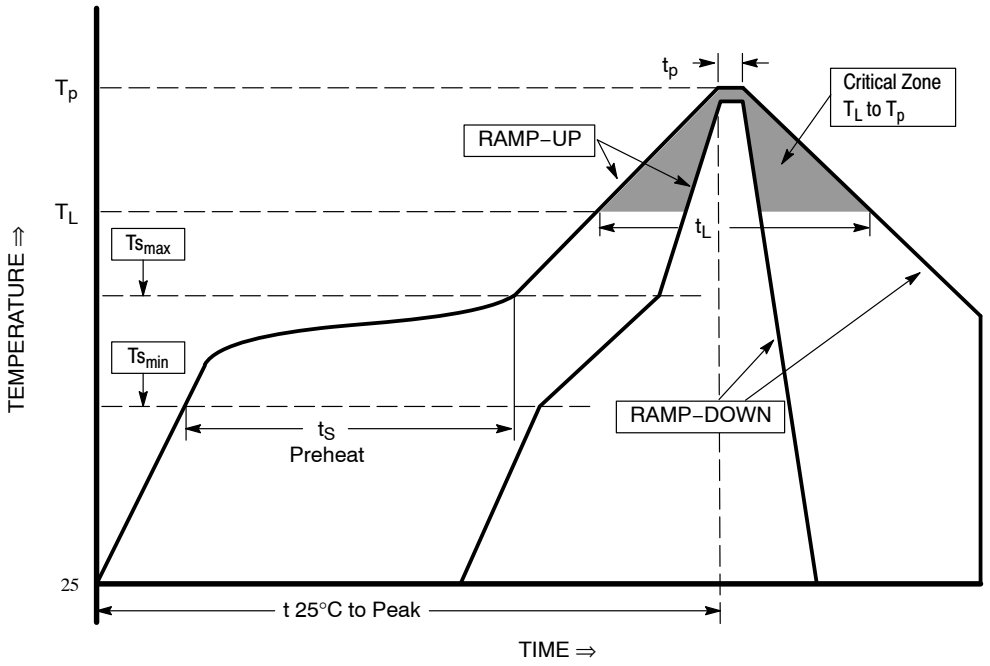


Figure 61. Typical Pb−Free Solder Heating Profile

Profile Feature	Pb−Free Assembly
Average Ramp−Up Rate (Ts_{max} to Tp)	3°C/second max
Preheat Temperature Min (Ts_{min}) Temperature Max (Ts_{max}) Time (ts_{min} to ts_{max})	 150°C 200°C 60−180 seconds
Time maintained above Temperature (T_T) Time (t_T)	 217°C 60−150 seconds
Peak Classification Temperature (Tp)	260°C +5/−0
Time within 5°C of actual Peak Temperature (tp)	20−40 seconds
Ramp−Down Rate	6°C/second max
Time 25°C to Peak Temperature	8 minutes max

AMBIENT MOUNTING DATA

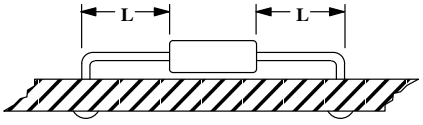
Data shown for thermal resistance junction−to−ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

Mounting Method		Lead Length, L (IN)				Units
		1/8	1/4	1/2	3/4	
1	$R_{\theta JA}$	50	51	53	55	°C/W
2		58	59	61	63	°C/W
3		28				°C/W

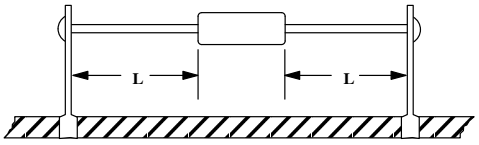
MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.



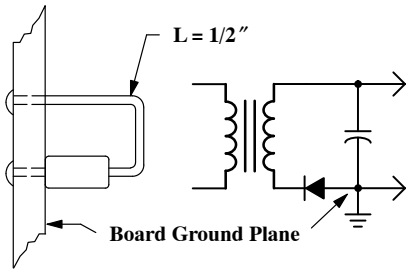
MOUNTING METHOD 2

Vector Push−In Terminals T−28



MOUNTING METHOD 3

P.C. Board with 1−1/2 ″ x 1−1/2 ″ Copper Surface



Humidity Indicator Card: Type HIC−0560

Objective

The objective of this information brief is to provide the customer with a general understanding of the humidity indicator cards (HIC) basic functions and a reaction plan based on the level of dryness as indicated on the card.

Introduction

The HIC is printed with moisture sensitive spots which will respond to variations of different levels of humidity with perceptible change in color typically from blue (dry) to pink (wet). The HIC is packed inside moisture barrier bags, which monitor the moisture inside the barrier bag. When the bag is opened, the HIC can be examined to determine the degree of dryness of the parts inside the bag.

Humidity Indicator Cards: HIC-0515 and HIC-0560

Excess humidity in the dry pack is noted by the HIC. It can occur due to misprocessing (e.g. missing or inadequate desiccant), mishandling (e.g. tears or rips in the moisture barrier bag) or improper storage.

The HIC should be read immediately upon removal from the moisture barrier bag. For best accuracy, the HIC should be read at 23±5°C. The following conditions apply regardless of the storage time (whether or not the shelf life has exceeded).

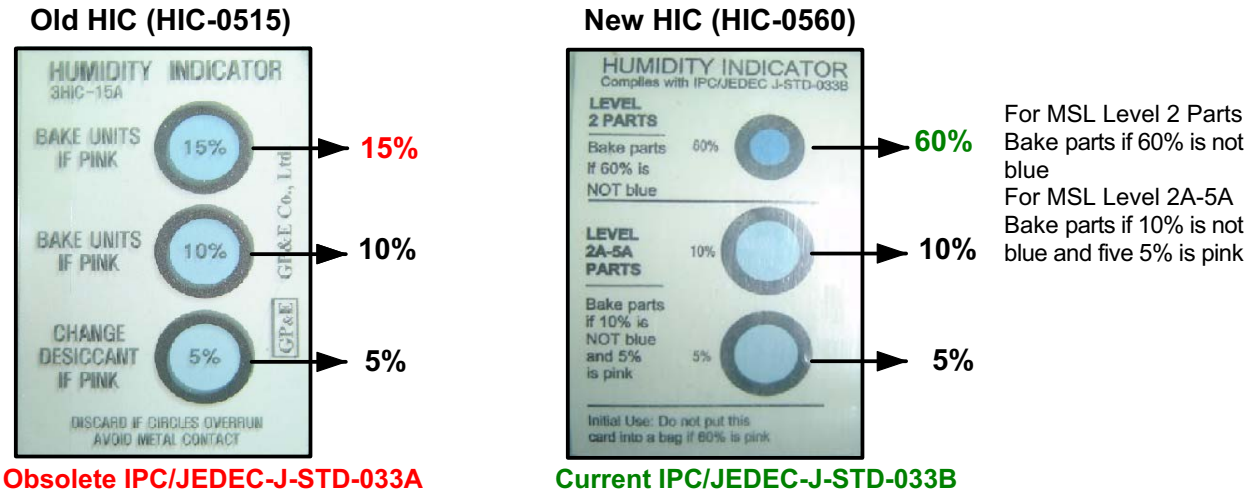


Figure 62. Humidity Indicator Card

Table 2: HIC Conditions and Corresponding Actions for HIC-0560

HIC Conditions	5%	10%	60%	Action	Remarks
Condition 1	Blue	Blue	Blue	No bake	Parts are dry
Condition 2	Pink	Blue	Blue	No bake	Only indicates that parts have 5% level of moisture
Condition 3	Pink	Pink	Blue	Bake required, refer to Table 2	Bake parts MSL levels 2a, 3, 4, 5, and 5a No need to bake MSL level 2
Condition 4	Pink	Pink	Pink	Bake required, refer to Table 2	All were parts were affected by moisture

Bake Duration for Exposed Parts

AMIS recommends that bake duration of exposed parts should comply with the existing provisions as mandated by Joint Industry Standard IPC/JEDEC-STD-033B entitled "Handling, Packing and Use of Moisture/Reflow Sensitive Surface Mount Devices" Bake Duration for Exposed Parts as shown in Table 3.

Table 3: Reference Conditions for Drying Mounted or Unmounted SMD Packages (User bake: floor life beings counting at time = 0 after bake)

Package Body	Level	Bake @ 125°C		Bake @ 90°C ≤ 5% RH		Bake @ 40°C ≤ 5% RH	
		Exceeding Floor Life by > 72 h	Exceeding Floor Life by > 72 h	Exceeding Floor Life by > 72 h	Exceeding Floor Life by > 72 h	Exceeding Floor Life by > 72 h	Exceeding Floor Life by > 72 h
Thickness ≤ 1.4mm	2	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	2a	7 hours	5 hours	23 hours	13 hours	9 days	7 days
	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days
Thickness > 1.4mm ≤ 2.0mm	2	18 hours	15 hours	63 hours	2 days	25 days	20 days
	2a	21 hours	16 hours	3 days	2 days	29 days	22 days
	3	27 hours	17 hours	4 days	2 days	37 days	23 days
	4	34 hours	20 hours	5 days	3 days	47 days	28 days
	5	40 hours	25 hours	6 days	4 days	57 days	35 days
	5a	48 hours	40 hours	8 days	6 days	79 days	56 days
Thickness > 2.0mm ≤ 4.5mm	2	48 hours	48 hours	10 days	7 days	79 days	67 days
	2a	48 hours	48 hours	10 days	7 days	79 days	67 days
	3	48 hours	48 hours	10 days	8 days	79 days	67 days
	4	48 hours	48 hours	10 days	10 days	79 days	67 days
	5	48 hours	48 hours	10 days	10 days	79 days	67 days
	5a	48 hours	48 hours	10 days	10 days	79 days	67 days
BGA package > 17mm x 17mm or any stacked die package (Note 12)	2-6	96 hours	As above per package thickness and moisture level	Not applicable	As above per package thickness and moisture level	Not applicable	As above per package thickness and moisture level

NOTES:

11. Table 3 is based on worst-case molded lead frame SMD packages. Users may reduce the actual back time if technically justified (e.g. absorption/desorption data, etc.). In most cases it is applicable to other nonhermetic surface mount SMD packages.
12. For BGA packages > 17mm x >17 mm that do not have internal planes that block the moisture diffusion path in the substrate they may use bake times based on the thickness/moisture level portion of the table.

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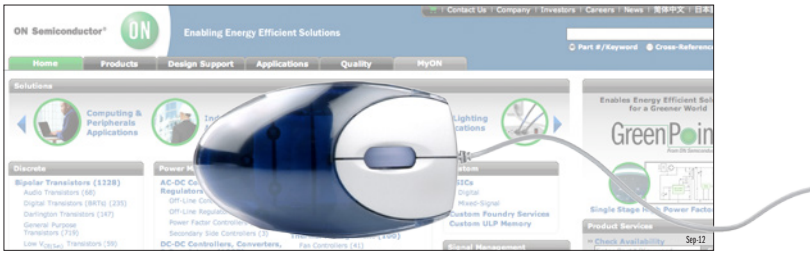
Oregon	Portland	SiFore Technical	(503) 977-6267
Puerto Rico	Countrywide	e-Components	(888) 468-2444
Rhode Island	Statewide	Paragon Electronic Systems	(603) 645-7630
Vermont	Statewide	Paragon Electronic Systems	(603) 645-7630
Washington	Bellevue	SiFore Technical	(425) 990-4701
Wisconsin	Evansville	Stan Clothier Company	(608) 882-0686
	Oconomowoc	Stan Clothier Company	(608) 882-0686



PUBLICATION ORDERING INFORMATION

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Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Email: orderlit@onsemi.com

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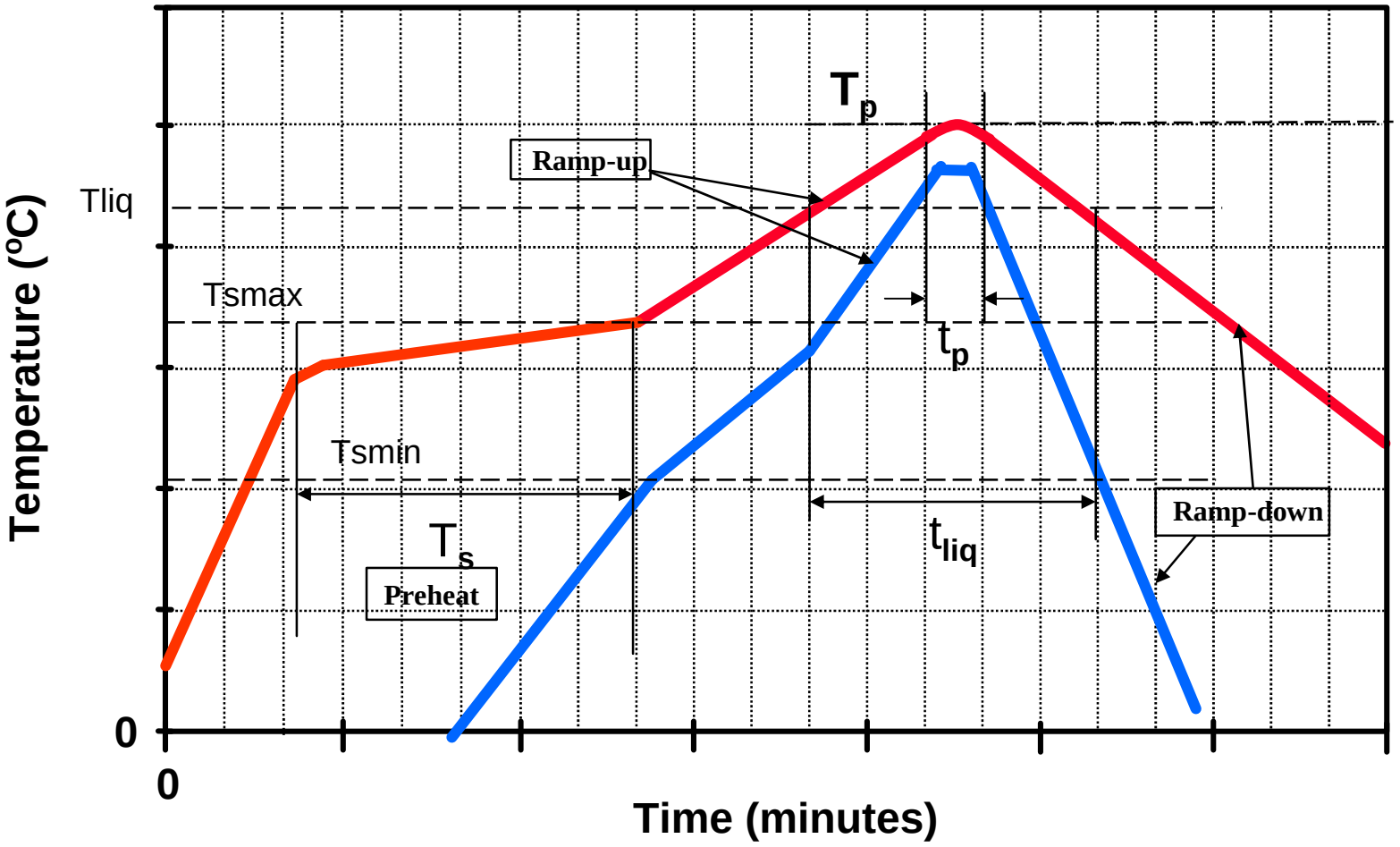
ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

Standard Pb-Free Plating Reflow Profile



Reflow Profile For Lead-Free ONSEMI vs JEDEC

Profile Feature	JEDEC Pb-Free Profiles		ON Semi Pb-Free Profiles	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (Tliq to Tp)	3ºC/ second max		1.68ºC/ second	
Preheat - Temperature Min(Tsmin) - Temperature Max(Tsmax) - Time(min to max) (ts)	 150ºC 200ºC 60-180 seconds		 150ºC 180ºC 200 seconds max	
Tsmax to Tliq - Ramp-up Rate	3ºC/ second max		2.8ºC/second	
Time maintained above: - Temperature(Tliq) - Time(tliq)	 217ºC 60-150 seconds		 217ºC 90 seconds	
Peak Temperature(Tp)	245 +0/-5ºC	250 +0/-5ºC	260-265ºC	
Time within 5ºC of actual Peak Temperature(tp)	10-30 seconds	20-40 seconds	20 seconds	
Ramp-down Rate	6ºC/second max		1.2ºC/second	
Time 25ºC to Peak Temperature	8 minute max		5.2 -6 minutes	

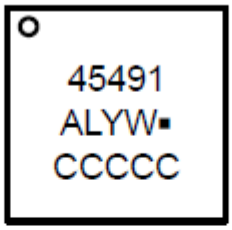
- Large Body : Pkg Volume> 350 mm³; Small Body: Pkg Volume < 350 mm³
- 90% of ON Semi Packages < 350 mm³ in Volume

料號說明：

NCP → Produce class
45491 → Stem number
XMN → package
TW → Tape & Reel
G → Green

產地：Thailand

MARKING DIAGRAM



45491	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package
CCCCC	= Country of Assembly