

A	B	C	D	E	F	G	H
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2

3

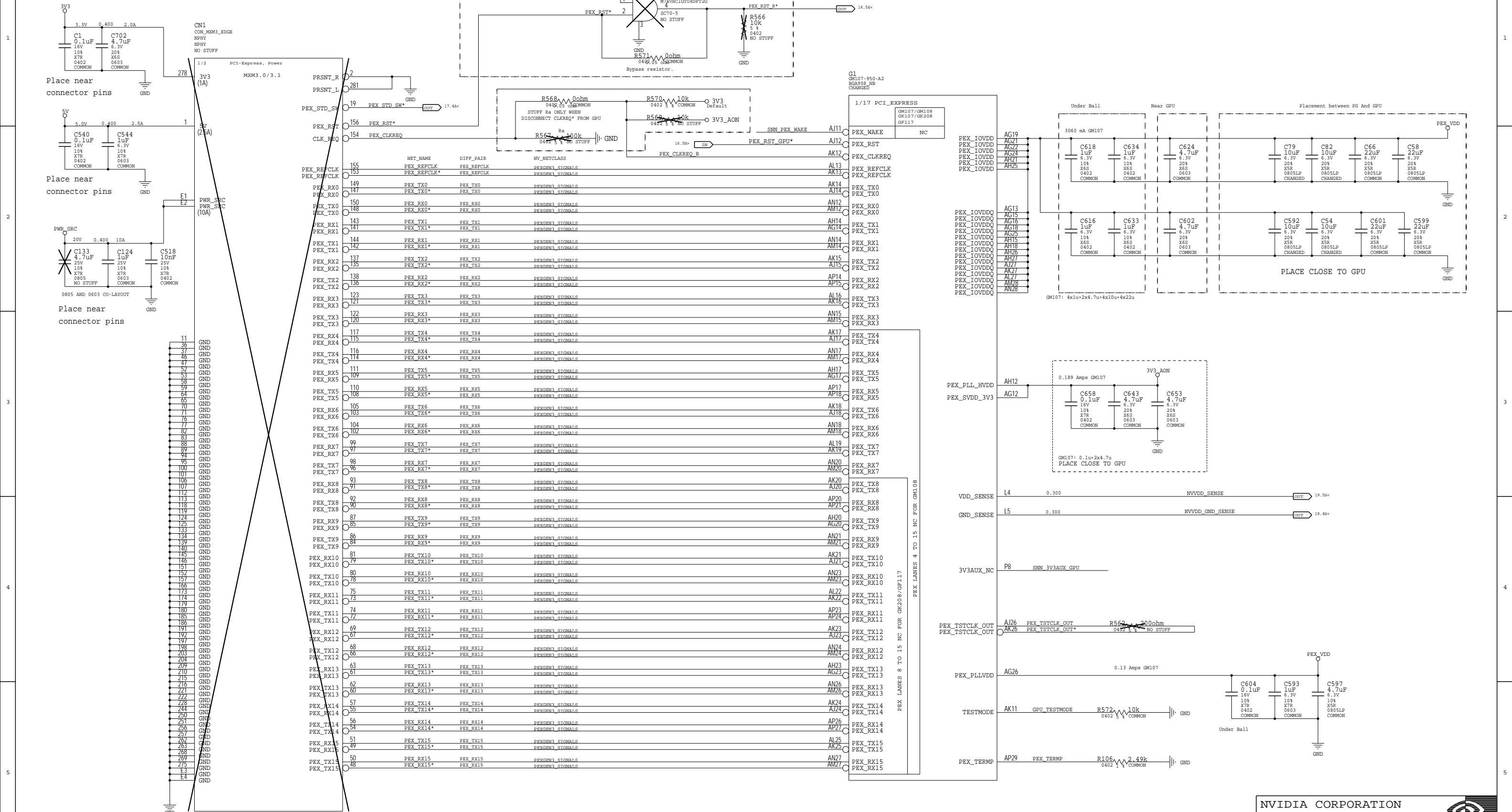
NV	PN	600-52757-
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5

PCI EXPRESS INTERFACE



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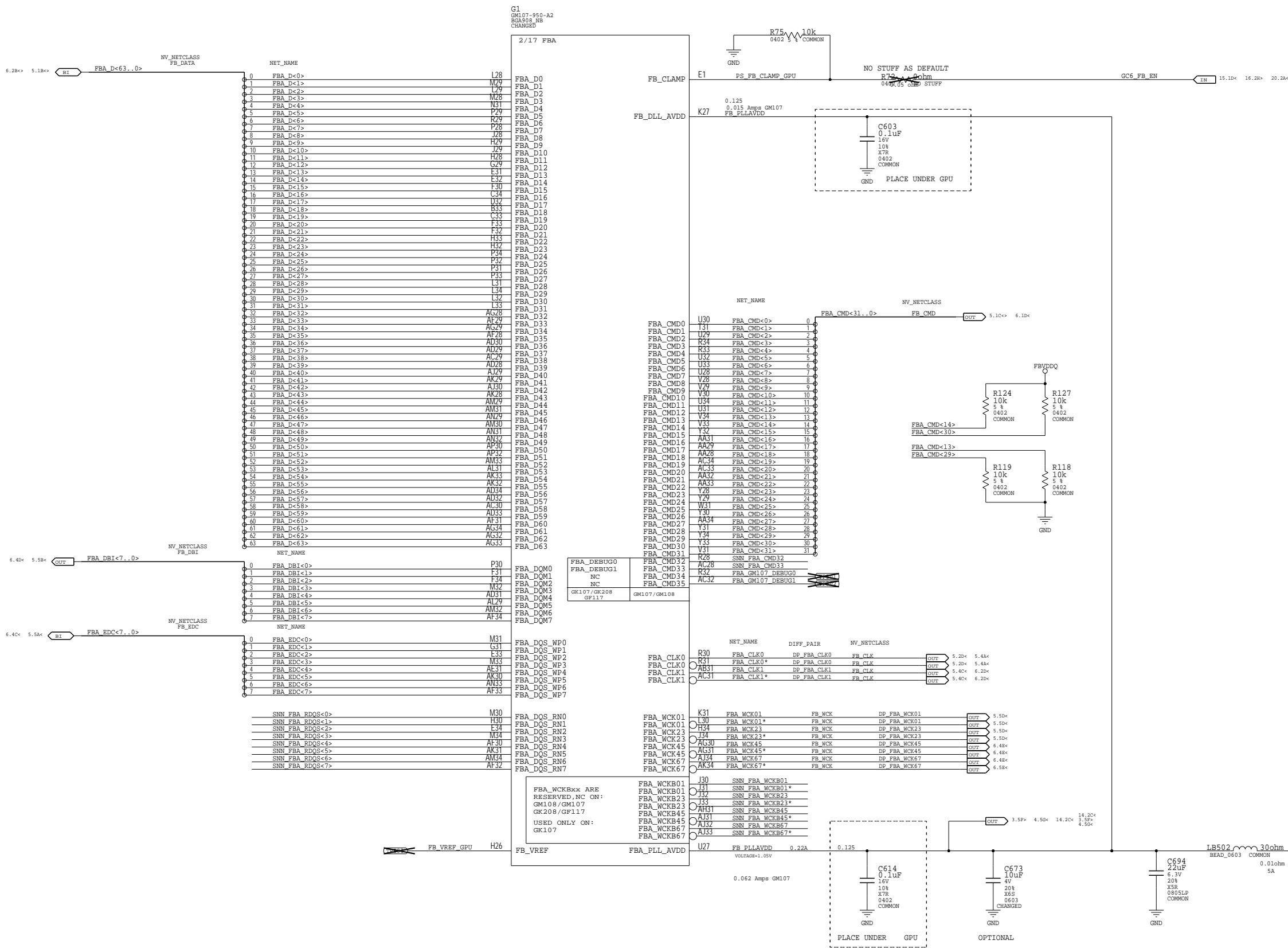
PAGE

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DATE

10-FEB-2015

FRAME BUFFER A GPU INTERFACE



GDDR5_BGA170_MIRR COMMAND MAP

CMD0	CS*
CMD1	A3_BA3
CMD2	A2_BA0
CMD3	A4_BA2
CMD4	A5_BA1
CMD5	WE*
CMD6	A7_A8
CMD7	A6_A11
CMD8	AB1*
CMD9	A12_RFU
CMD10	A0_A10
CMD11	A1_A9
CMD12	RAS*
CMD13	RST*
CMD14	CKE*
CMD15	CAS*
CMD16	
CMD17	A3_BA3
CMD18	A2_BA0
CMD19	A4_BA2
CMD20	A5_BA1
CMD21	WE*
CMD22	A7_A8
CMD23	A6_A11
CMD24	AB1*
CMD25	A12_RFU
CMD26	A0_A10
CMD27	A1_A9
CMD28	RAS*
CMD29	RST*
CMD30	CKE*
CMD31	CAS*

ASSEMBLY	SKU502 GM107 128bit X32 GDDR5 MEMORY
PAGE DETAIL	FRAME BUFFER A GPU INTERFACE

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DATE 10-FEB-2015

FRAME BUFFER B GPU INTERFACE

G1
GM107-950-A2
BGA908_NB
CHANGED

GDDR5_BGA170_MIRR COMMAND MAP

	D...31	32...63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB1*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17	A3_BA3	
CMD18	A2_BA0	
CMD19	A4_BA2	
CMD20	A5_BA1	
CMD21	WE*	
CMD22	A7_A8	
CMD23	A6_A11	
CMD24	AB1*	
CMD25	A12_RFU	
CMD26	A0_A10	
CMD27	A1_A9	
CMD28	RAS*	
CMD29	RST*	
CMD30	CKE*	
CMD31	CAS*	

8.28<> 7.1A<> BI FBB_D<63...0>

NV_NETCLASS
FB_DATA

NET_NAME

0	FBB_D<0>	G9
1	FBB_D<1>	G8
2	FBB_D<2>	F9
3	FBB_D<3>	F8
4	FBB_D<4>	F11
5	FBB_D<5>	G11
6	FBB_D<6>	F12
7	FBB_D<7>	G12
8	FBB_D<8>	G6
9	FBB_D<9>	F5
10	FBB_D<10>	E6
11	FBB_D<11>	F6
12	FBB_D<12>	F4
13	FBB_D<13>	G4
14	FBB_D<14>	E2
15	FBB_D<15>	F3
16	FBB_D<16>	C2
17	FBB_D<17>	D4
18	FBB_D<18>	D3
19	FBB_D<19>	C1
20	FBB_D<20>	B3
21	FBB_D<21>	C4
22	FBB_D<22>	B5
23	FBB_D<23>	C5
24	FBB_D<24>	A11
25	FBB_D<25>	C11
26	FBB_D<26>	D11
27	FBB_D<27>	B11
28	FBB_D<28>	D8
29	FBB_D<29>	A8
30	FBB_D<30>	C8
31	FBB_D<31>	B8
32	FBB_D<32>	F24
33	FBB_D<33>	G24
34	FBB_D<34>	E24
35	FBB_D<35>	G24
36	FBB_D<36>	D21
37	FBB_D<37>	E21
38	FBB_D<38>	G21
39	FBB_D<39>	F21
40	FBB_D<40>	G27
41	FBB_D<41>	D27
42	FBB_D<42>	G26
43	FBB_D<43>	E27
44	FBB_D<44>	E29
45	FBB_D<45>	F29
46	FBB_D<46>	E30
47	FBB_D<47>	D30
48	FBB_D<48>	A32
49	FBB_D<49>	C31
50	FBB_D<50>	C32
51	FBB_D<51>	B32
52	FBB_D<52>	D29
53	FBB_D<53>	A29
54	FBB_D<54>	C29
55	FBB_D<55>	B29
56	FBB_D<56>	B21
57	FBB_D<57>	C23
58	FBB_D<58>	A21
59	FBB_D<59>	C21
60	FBB_D<60>	B24
61	FBB_D<61>	C24
62	FBB_D<62>	B26
63	FBB_D<63>	C26

3/17 FBB
ALL PINS NC FOR GM108/
GK208/GP117

FBB_CMD0	D13	FBB_CMD<0>	0
FBB_CMD1	E14	FBB_CMD<1>	1
FBB_CMD2	F14	FBB_CMD<2>	2
FBB_CMD3	A12	FBB_CMD<3>	3
FBB_CMD4	B12	FBB_CMD<4>	4
FBB_CMD5	C14	FBB_CMD<5>	5
FBB_CMD6	B14	FBB_CMD<6>	6
FBB_CMD7	G15	FBB_CMD<7>	7
FBB_CMD8	F15	FBB_CMD<8>	8
FBB_CMD9	D15	FBB_CMD<9>	9
FBB_CMD10	A14	FBB_CMD<10>	10
FBB_CMD11	E14	FBB_CMD<11>	11
FBB_CMD12	D14	FBB_CMD<12>	12
FBB_CMD13	A15	FBB_CMD<13>	13
FBB_CMD14	B15	FBB_CMD<14>	14
FBB_CMD15	C17	FBB_CMD<15>	15
FBB_CMD16	D18	FBB_CMD<16>	16
FBB_CMD17	F18	FBB_CMD<17>	17
FBB_CMD18	B20	FBB_CMD<18>	18
FBB_CMD19	A20	FBB_CMD<19>	19
FBB_CMD20	B20	FBB_CMD<20>	20
FBB_CMD21	C18	FBB_CMD<21>	21
FBB_CMD22	B18	FBB_CMD<22>	22
FBB_CMD23	G18	FBB_CMD<23>	23
FBB_CMD24	G17	FBB_CMD<24>	24
FBB_CMD25	F17	FBB_CMD<25>	25
FBB_CMD26	D16	FBB_CMD<26>	26
FBB_CMD27	A18	FBB_CMD<27>	27
FBB_CMD28	D17	FBB_CMD<28>	28
FBB_CMD29	A17	FBB_CMD<29>	29
FBB_CMD30	B17	FBB_CMD<30>	30
FBB_CMD31	E17	FBB_CMD<31>	31
FBB_CMD32	G14	SNN_FBB_CMD32	
FBB_CMD33	G20	SNN_FBB_CMD33	
FBB_CMD34	C12	FBB_CMD34	
FBB_CMD35	C20	FBB_CMD35	

FBB_DEBUG0	GM107
FBB_DEBUG1	GM107
NC	
NC	

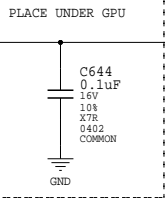
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D12	FBB_CLK0	DP_FBB_CLK0
E12	FBB_CLK0*	DP_FBB_CLK0
E20	FBB_CLK1	DP_FBB_CLK1
F20	FBB_CLK1*	DP_FBB_CLK1

F8	FBB_WCK01	FB_WCK	DP_FBB_WCK01	7.50<
A8	FBB_WCK01*	FB_WCK	DP_FBB_WCK01	7.50<
A5	FBB_WCK23	FB_WCK	DP_FBB_WCK23	7.50<
A6	FBB_WCK23*	FB_WCK	DP_FBB_WCK23	7.50<
D24	FBB_WCK45	FB_WCK	DP_FBB_WCK45	8.58<
D25	FBB_WCK45*	FB_WCK	DP_FBB_WCK45	8.58<
B27	FBB_WCK67	FB_WCK	DP_FBB_WCK67	8.58<
C27	FBB_WCK67*	FB_WCK	DP_FBB_WCK67	8.58<

FBB_WCKB01	D6	SNN_FBB_WCKB01
FBB_WCKB01	D7	SNN_FBB_WCKB01*
FBB_WCKB23	C6	SNN_FBB_WCKB23
FBB_WCKB23	C6	SNN_FBB_WCKB23*
FBB_WCKB45	F76	SNN_FBB_WCKB45
FBB_WCKB45	E26	SNN_FBB_WCKB45*
FBB_WCKB67	A26	SNN_FBB_WCKB67
FBB_WCKB67	A27	SNN_FBB_WCKB67*

FBB_PLL_AVDD

0.062 Amps GM107



8.4D< 7.5B< IN FBB_DBI<7...0>
FB_DBI

8.50< 7.5A< OUT FBB_EDC<7...0>
FB_EDC

0	FBB_DBI<0>	E11
1	FBB_DBI<1>	E3
2	FBB_DBI<2>	A3
3	FBB_DBI<3>	C9
4	FBB_DBI<4>	F23
5	FBB_DBI<5>	F27
6	FBB_DBI<6>	C30
7	FBB_DBI<7>	A24

0	FBB_EDC<0>	D10
1	FBB_EDC<1>	D6
2	FBB_EDC<2>	C3
3	FBB_EDC<3>	B9
4	FBB_EDC<4>	E23
5	FBB_EDC<5>	E28
6	FBB_EDC<6>	B30
7	FBB_EDC<7>	A23

SNN_FBB_DQS_RN<0>	D9
SNN_FBB_DQS_RN<1>	E4
SNN_FBB_DQS_RN<2>	B2
SNN_FBB_DQS_RN<3>	A9
SNN_FBB_DQS_RN<4>	D22
SNN_FBB_DQS_RN<5>	D28
SNN_FBB_DQS_RN<6>	A30
SNN_FBB_DQS_RN<7>	B23

FBB_WCKBxxx ARE
RESERVED, NC ON:
GM108/GM107
USED ONLY ON:
GK107

ASSEMBLY	SKU502 GM107 128Bit X32 GDDR5 MEMORY
PAGE DETAIL	FRAME BUFFER B GPU INTERFACE

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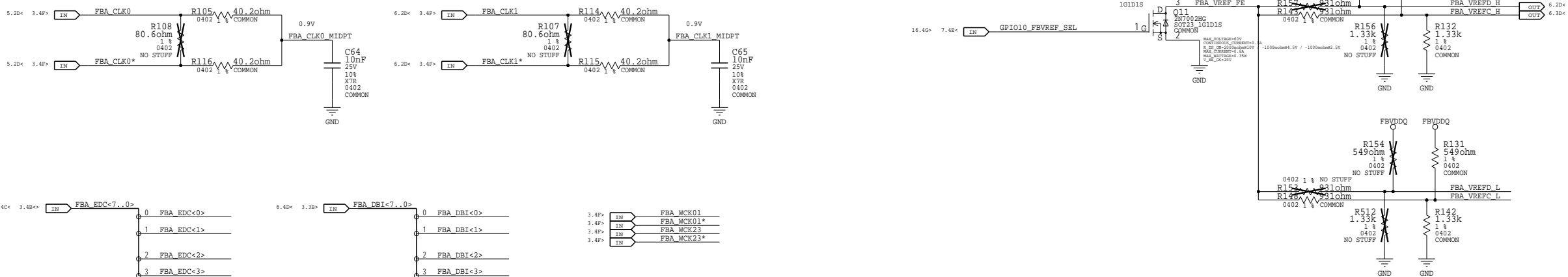
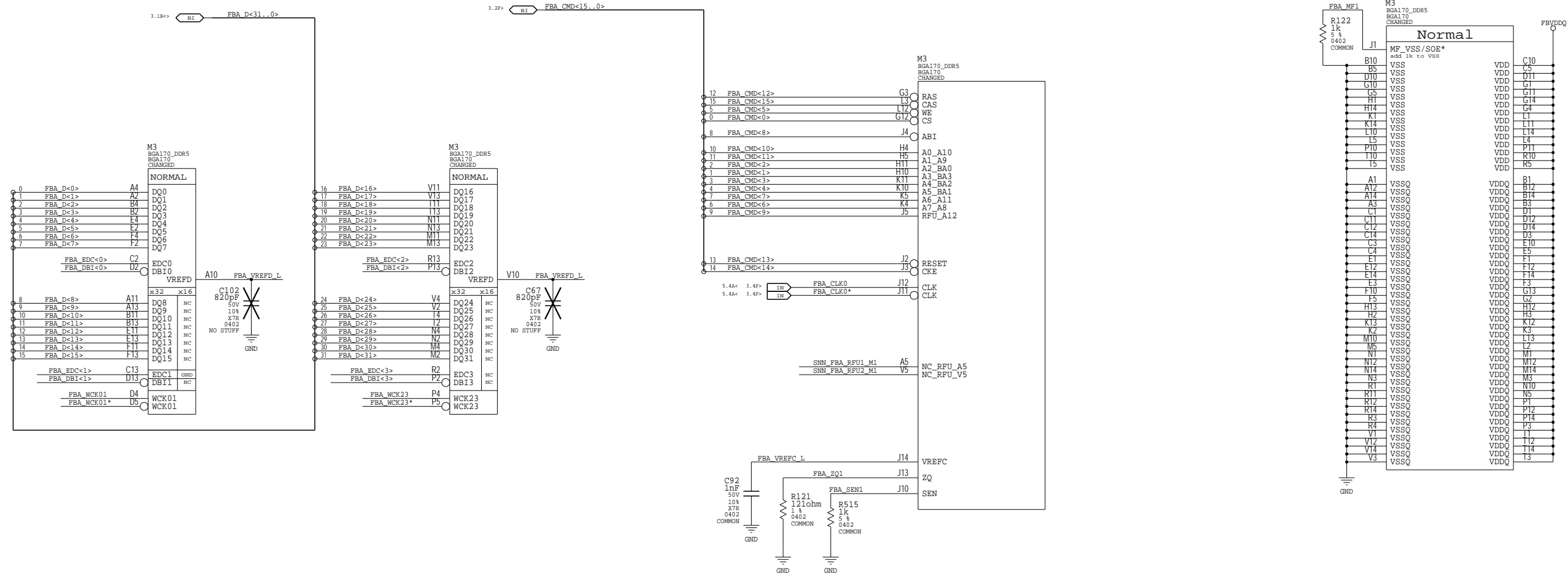
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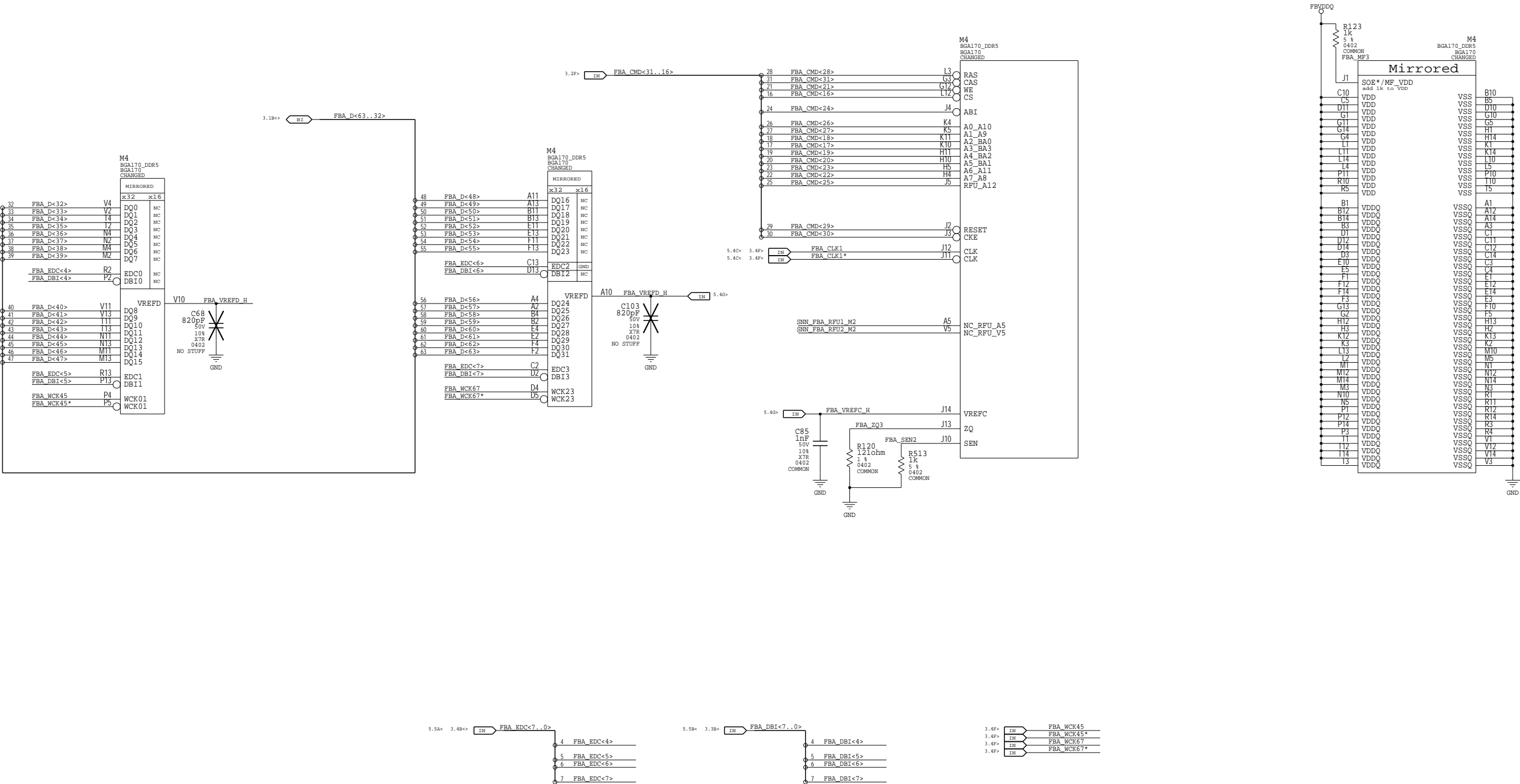
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FRAME BUFFER PARTITION A [31..0]



FRAME BUFFER PARTITION A [63..32]



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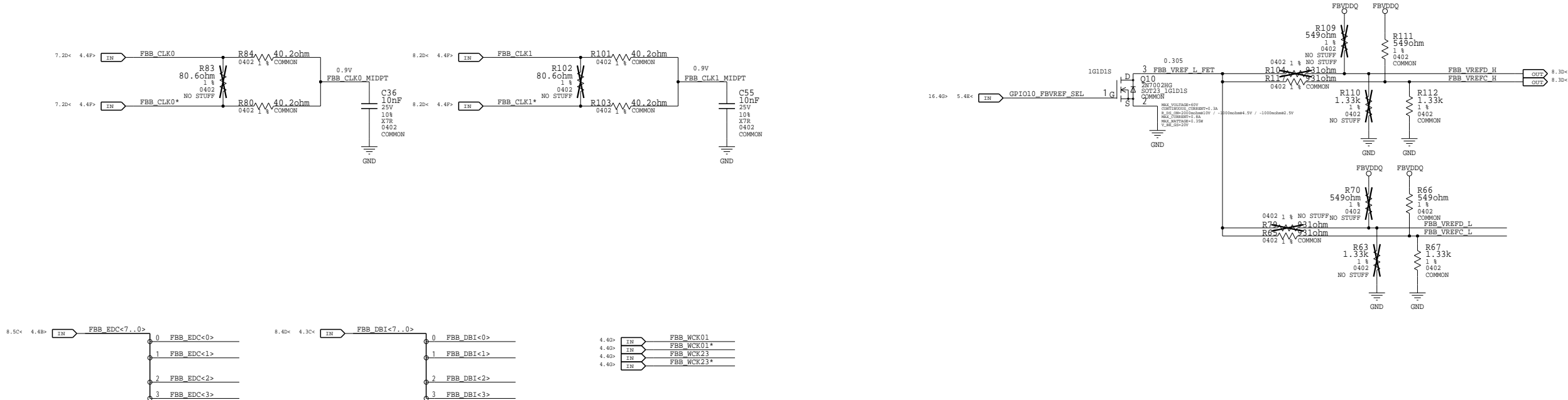
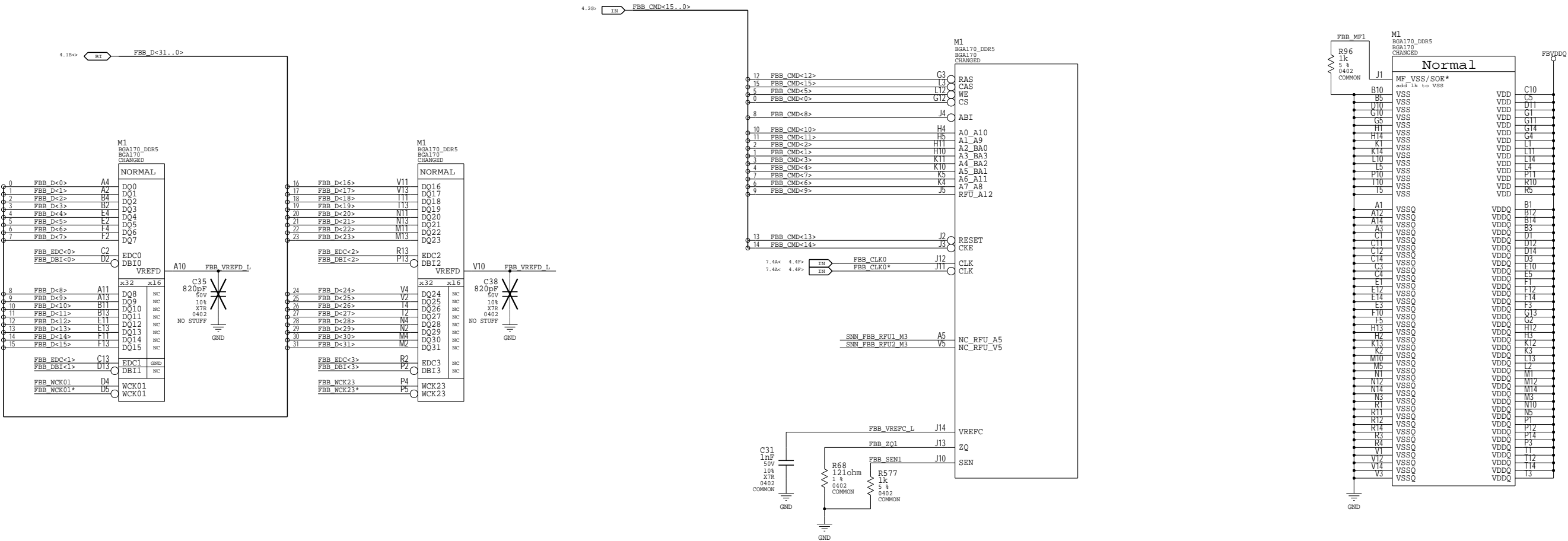
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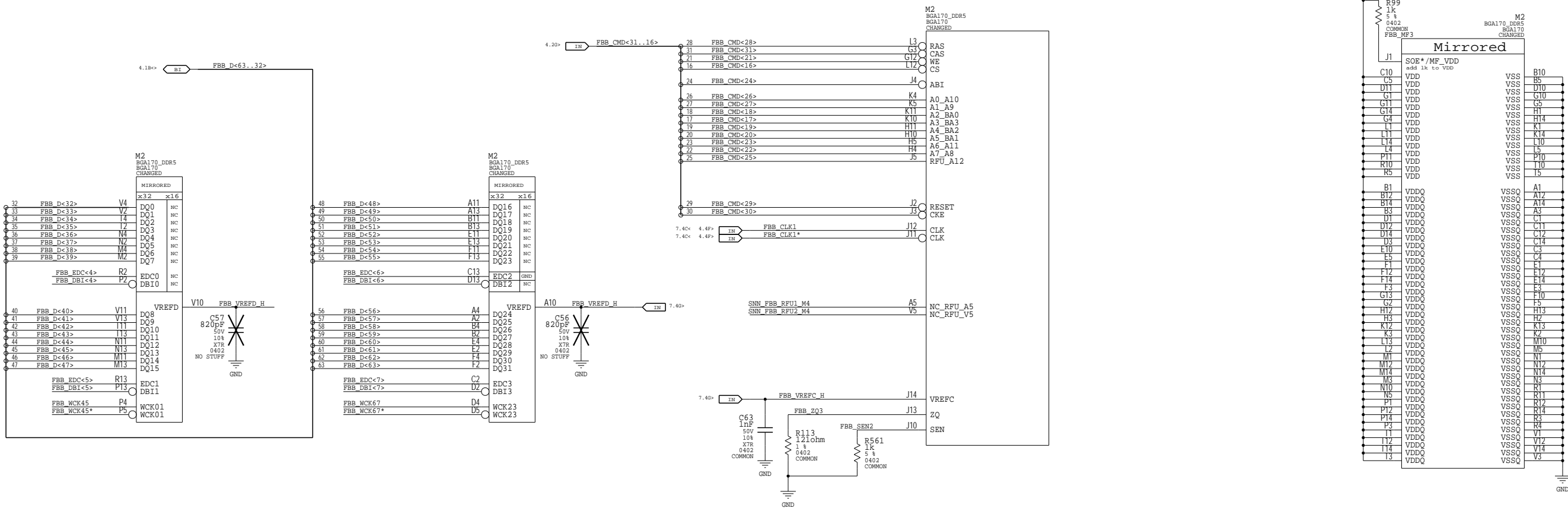
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FRAME BUFFER PARTITION B [31..0]



FRAME BUFFER PARTITION B [63..32]



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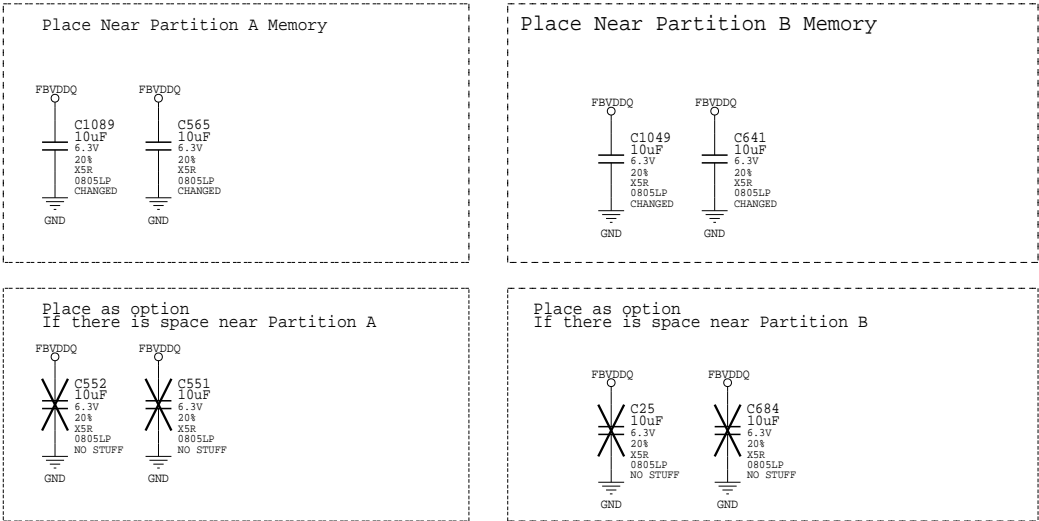
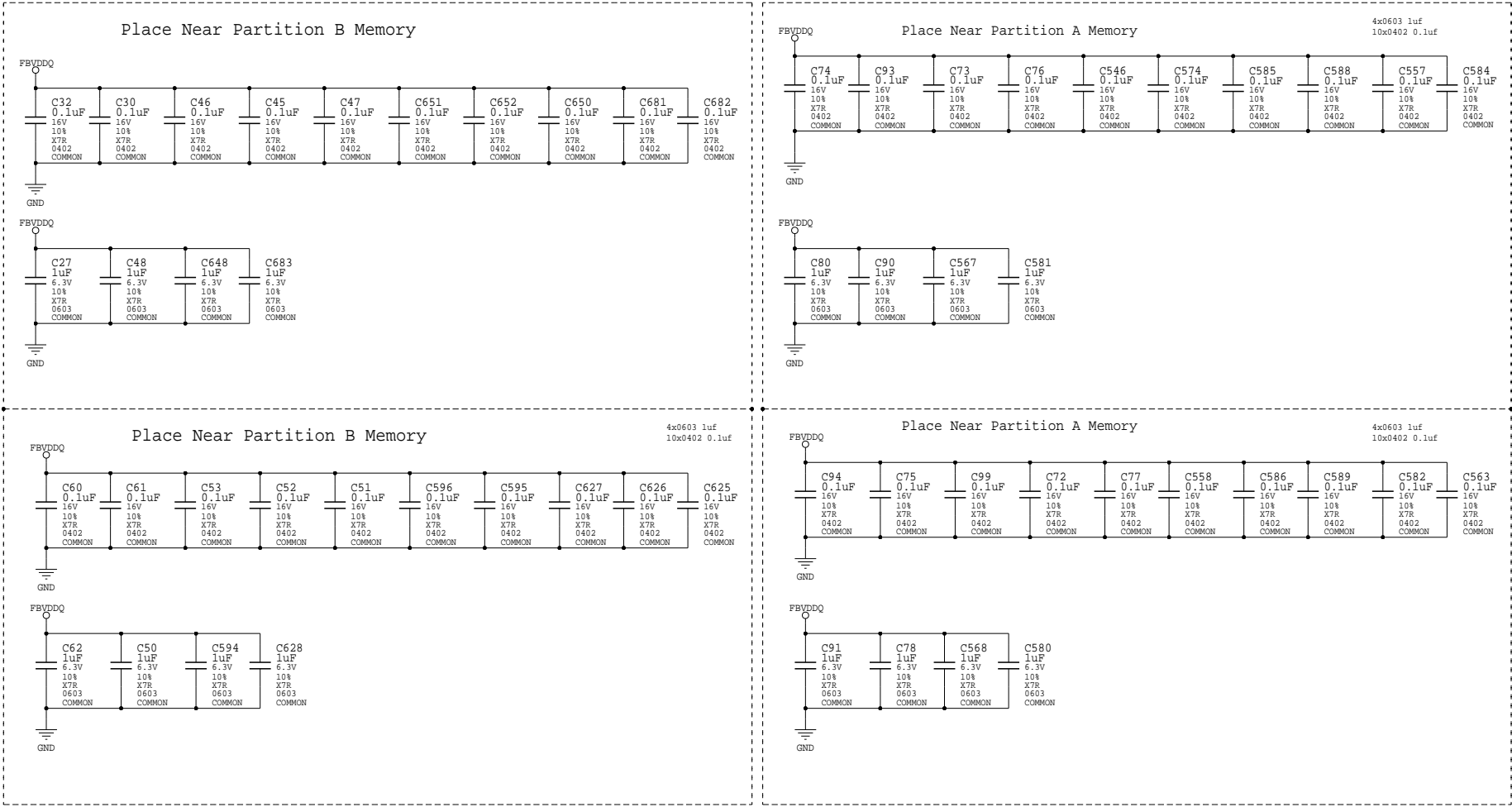
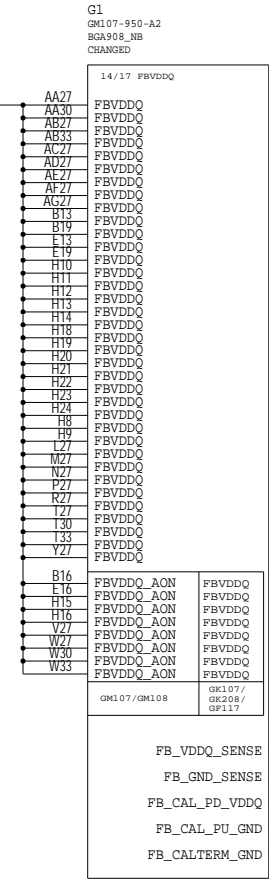
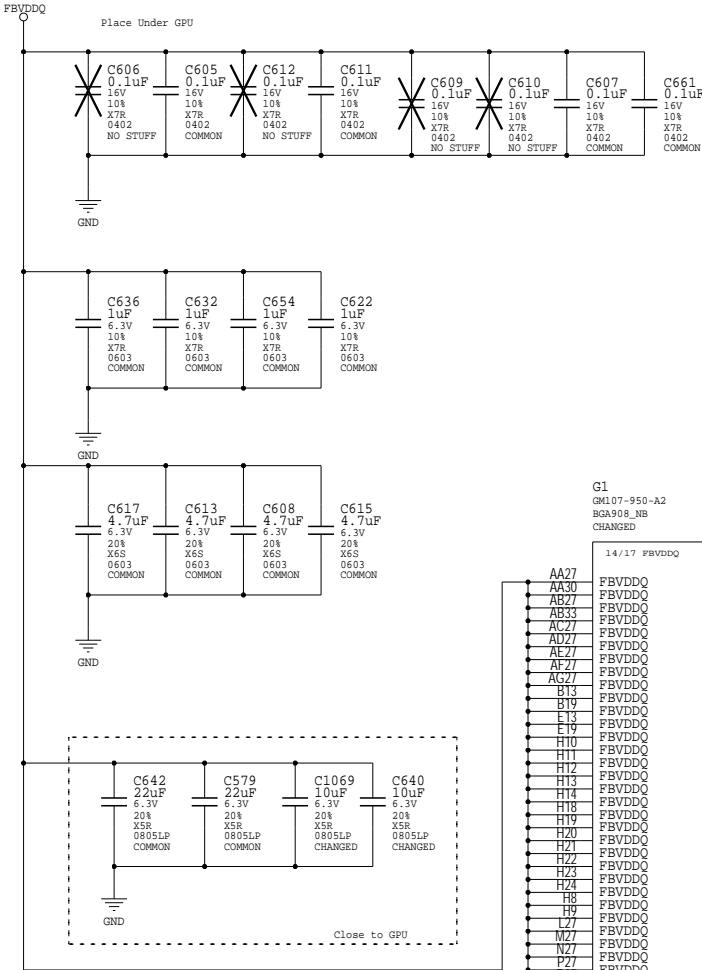
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MEMORY DECOUPLING CAPS

0402 x 0.1uF x4(4pcs Option)
0603 x 1uF x4
0603 x 4.7uF x4
0805 X 10uF x2
0805 X 22uF x2



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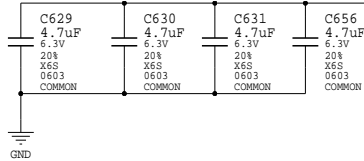
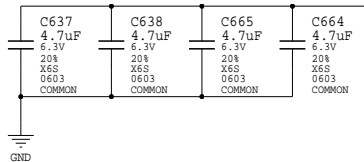
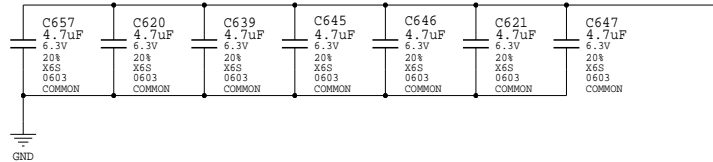
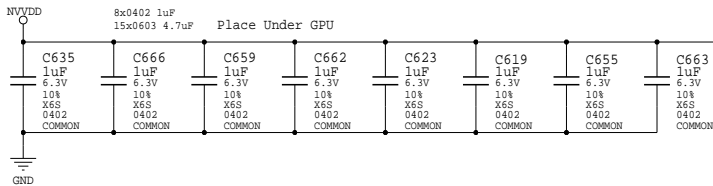
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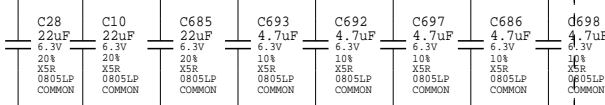
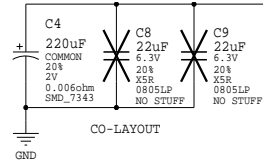
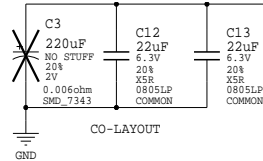
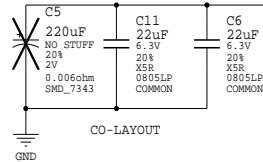
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GPU VDD\DCPLNG\GND

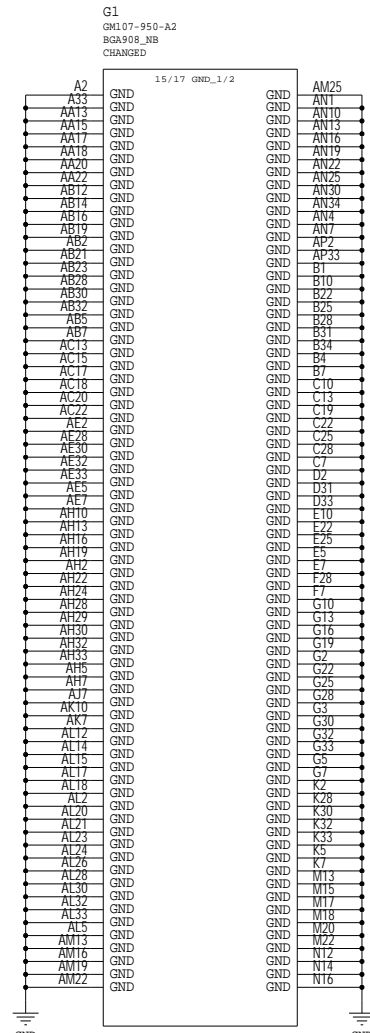
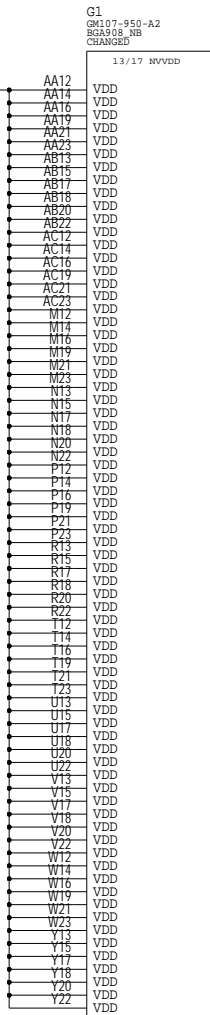
GM107-Under GPU(default)
0603x15x4.7uF X6S
0402x8x1.0uF X6S



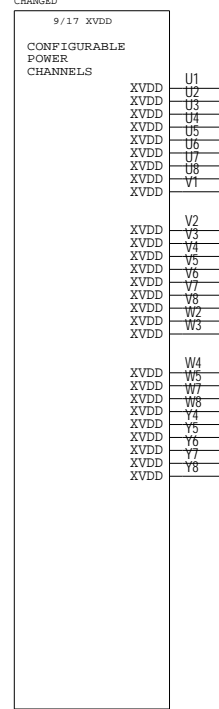
GM107-Near GPU(default)
7 x 0805 22uF X5R
5 x 0805 4.7uF X5R
1x 220uF POSCAP(3 X 7343 Footprint)



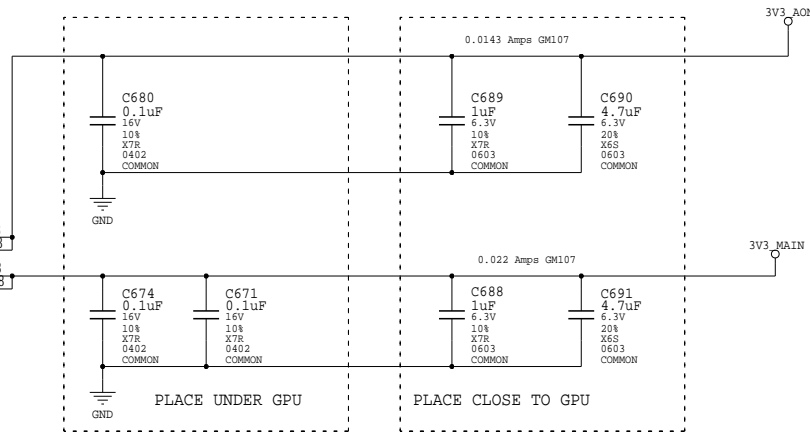
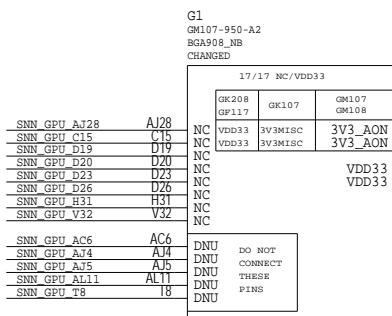
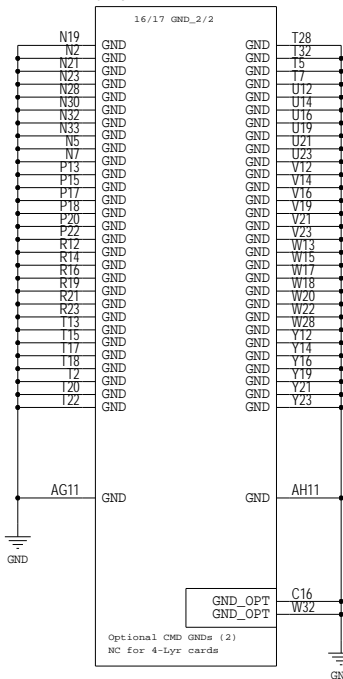
Place Near GPU



G1
GM107-950-A2
BG9A908_NB
CHANGED



G1
GM107-950-A2
BG9A908_NB
CHANGED



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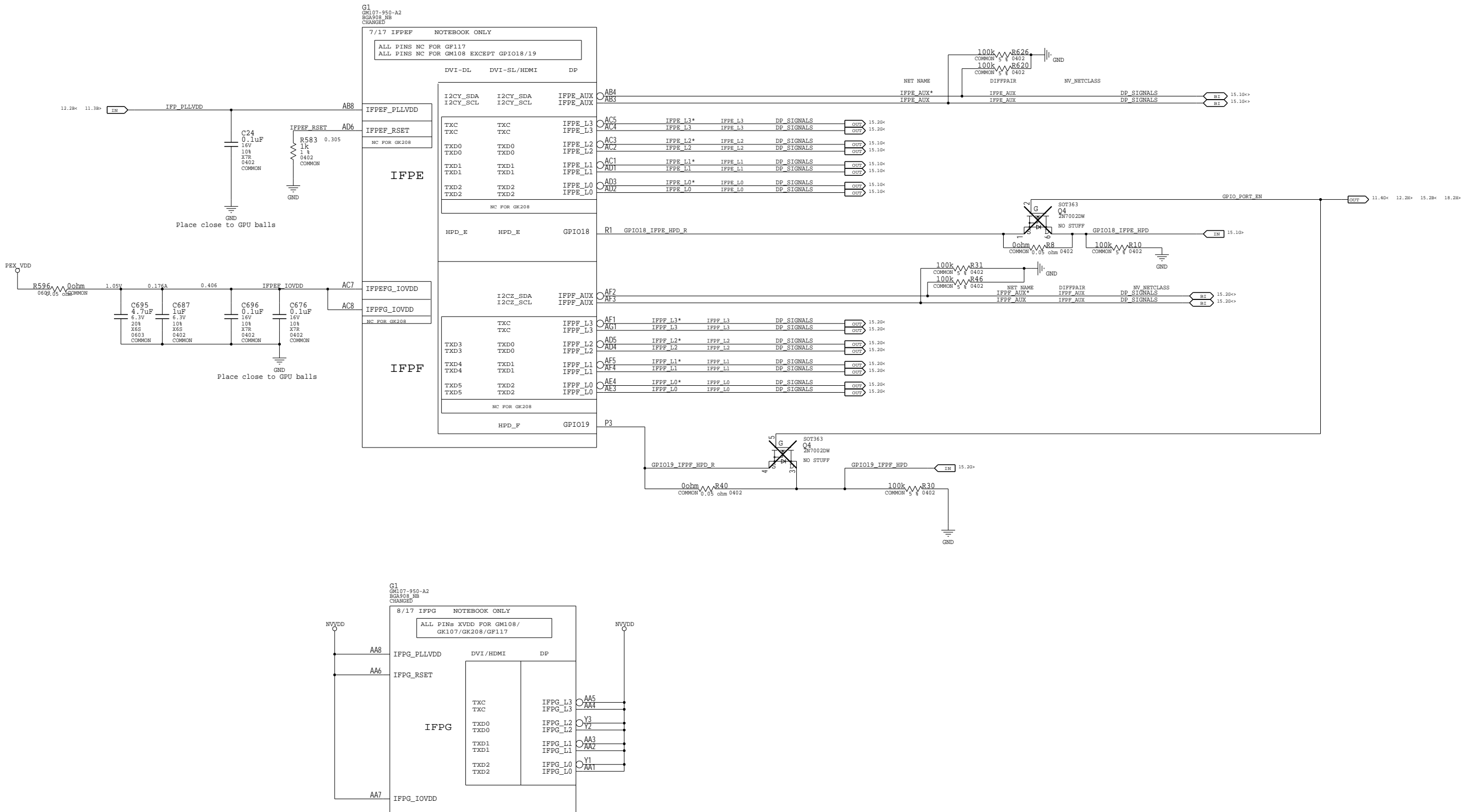
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DP LINKS E,F,G



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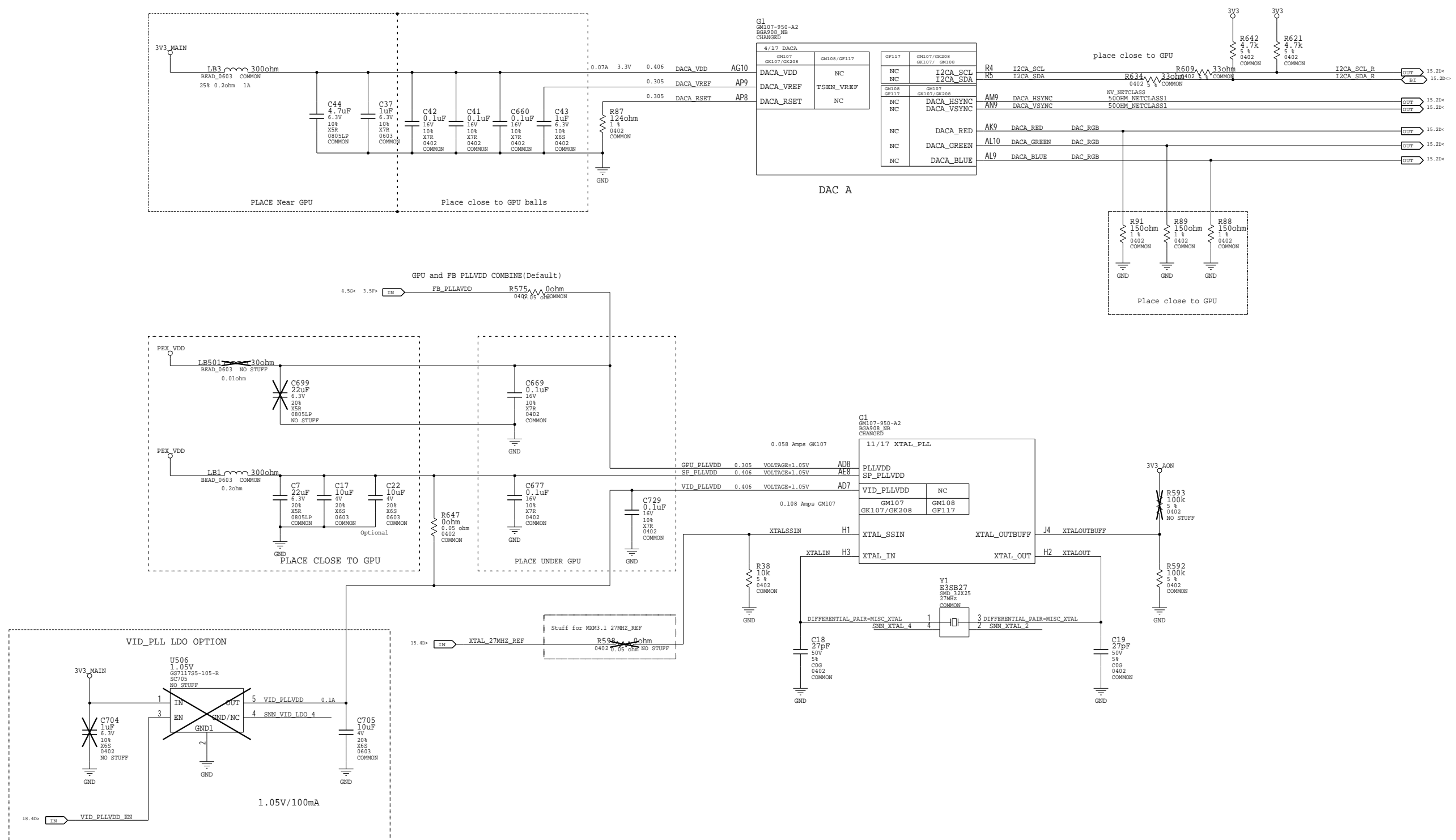
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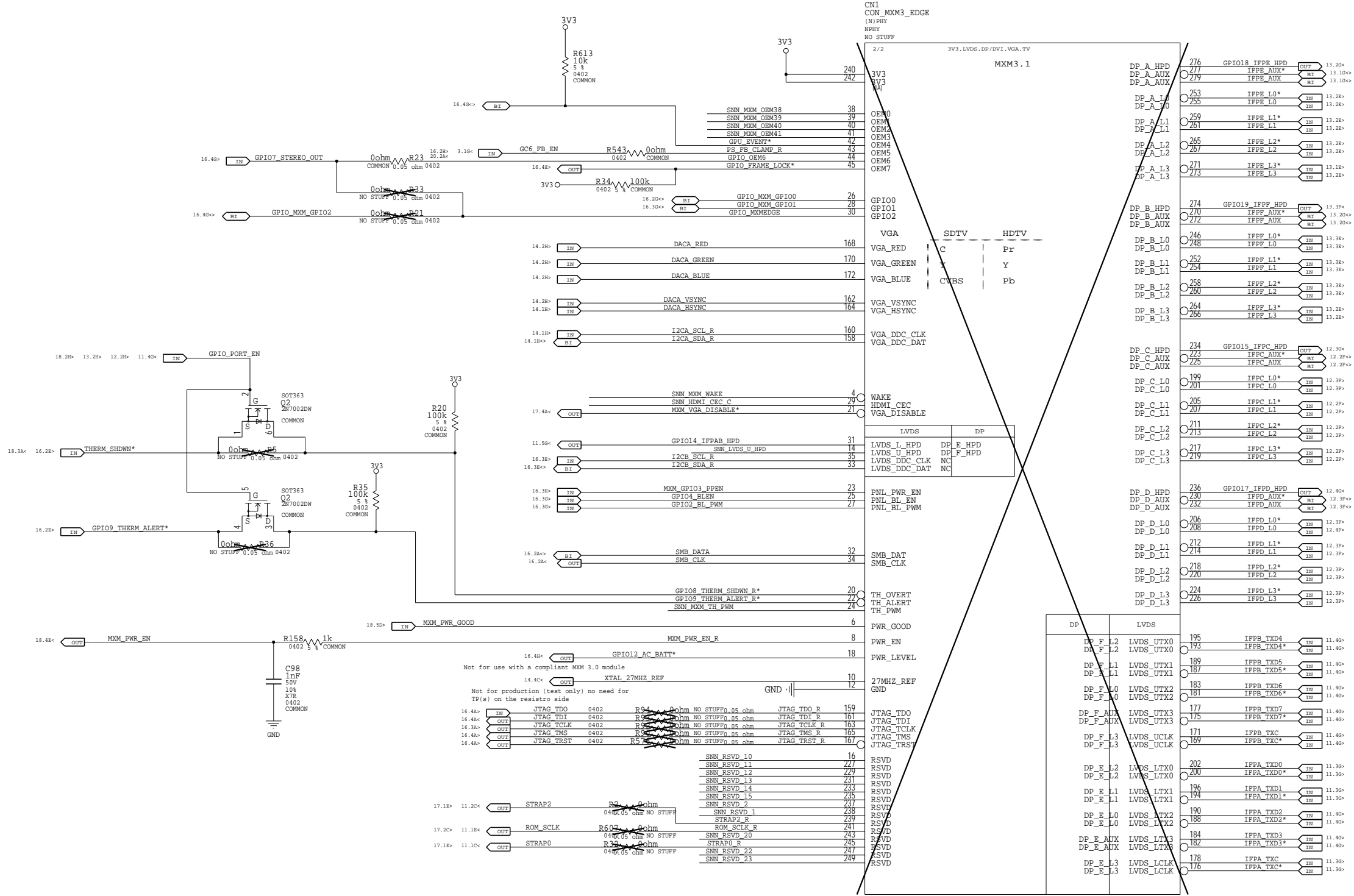
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DATE 10-FEB-2015

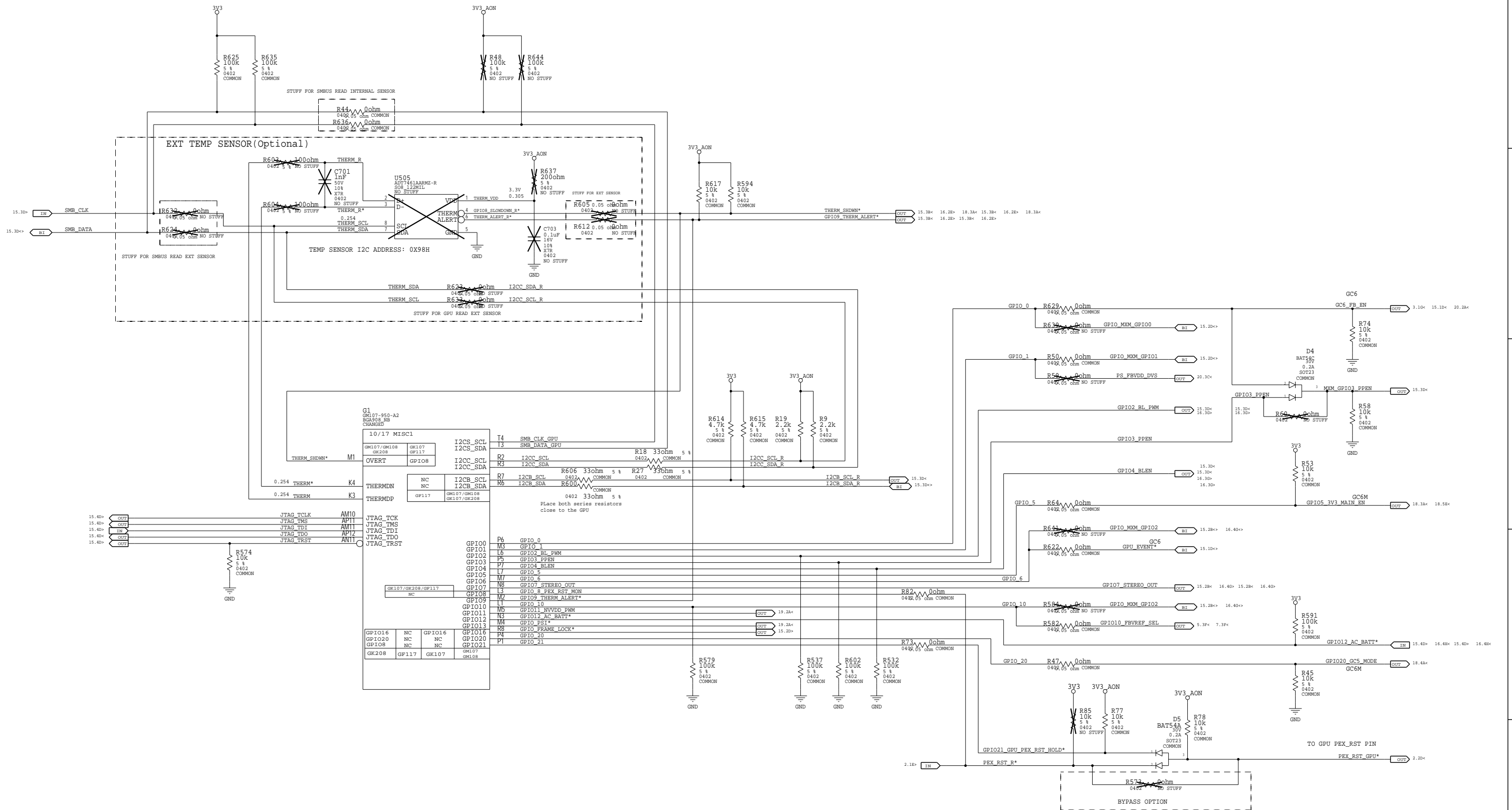
DACA PLL, CRYSTAL



MXM CONNECTOR, IO-SECTION



GPIO, JTAG, TEMP SENSOR



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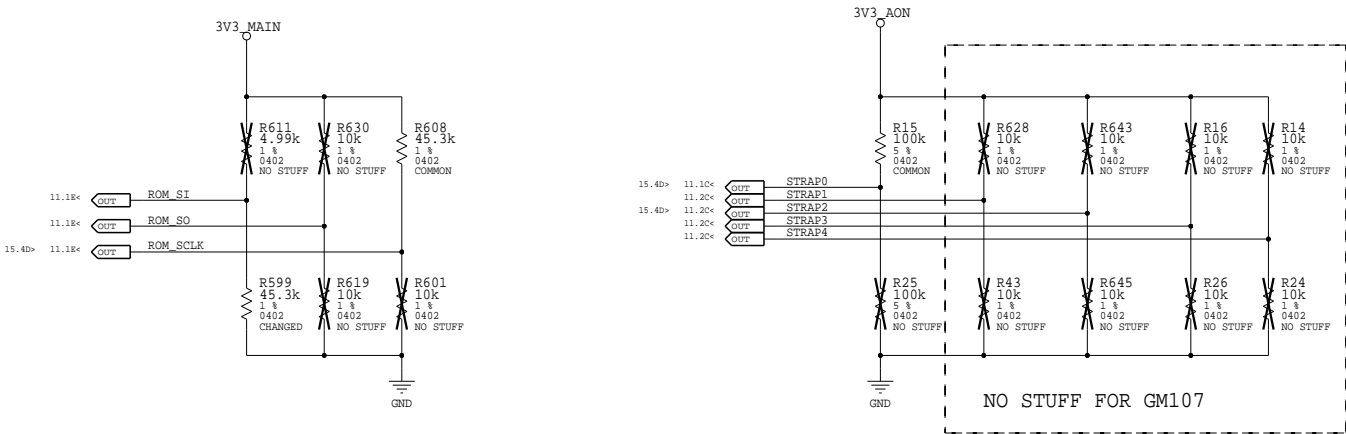
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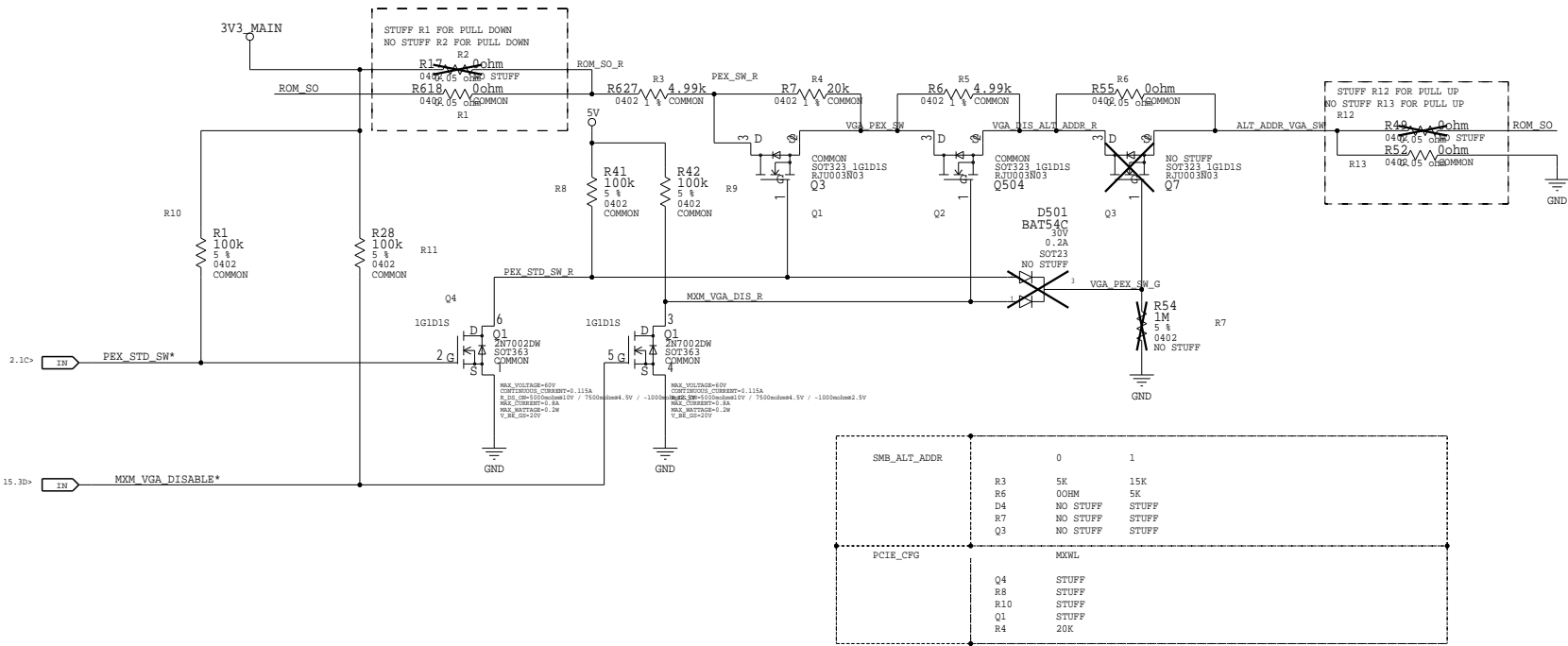
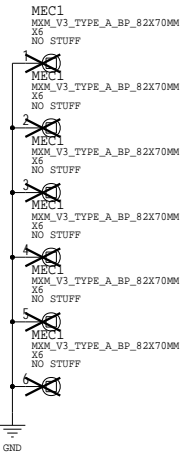
STRAPS AND MOUNTING HOLES



GB4B-128 Straps

Maxwell	Bit Signal	Values
ROM_SI	03: RAMCFG[3]	
	02: RAMCFG[2]	
	01: RAMCFG[1]	0111 128Mx32 128bit Samsung Primary
	00: RAMCFG[0]	0010 128Mx32 128bit Hynix-A Second
ROM_SO	03: DEVID_SEL	0 DEFAULT
	02: PCIE_CFG	0 HS 1 LS
	01: SMB_ALT_ADDR	0 DISABLED 1 ENABLED
	00: VGA_DEVICE	0 DISABLED 1 ENABLED
ROM_SCLK	03: SOR3_EXPOSED	0 DISABLED 1 ENABLED
	02: SOR2_EXPOSED	0 DISABLED 1 ENABLED
	01: SOR1_EXPOSED	0 DISABLED 1 ENABLED
	00: SOR0_EXPOSED	0 DISABLED 1 ENABLED
STRAP0		100kOHM PULL UP TO 3V3_AON
STRAP1		RESERVED
STRAP2		RESERVED
STRAP3		RESERVED
STRAP4		RESERVED

Multilevel Straps			
0000	4.99K to GND	1000	4.99K to VCC
0001	10K to GND	1001	10K to VCC
0010	15K to GND	1010	15K to VCC
0011	20K to GND	1011	20K to VCC
0100	24.9K to GND	1100	24.9K to VCC
0101	30.1K to GND	1101	30.1K to VCC
0110	34.8K to GND	1110	34.8K to VCC
0111	45.3K to GND	1111	45.3K to VCC



SMB_ALT_ADDR		0	1
R3	5K	15K	
R6	00HM	5K	
D4	NO STUFF	STUFF	
R7	NO STUFF	STUFF	
Q3	NO STUFF	STUFF	
PCIE_CFG		MXWL	
Q4	STUFF		
R8	STUFF		
R10	STUFF		
Q1	STUFF		
R4	20K		

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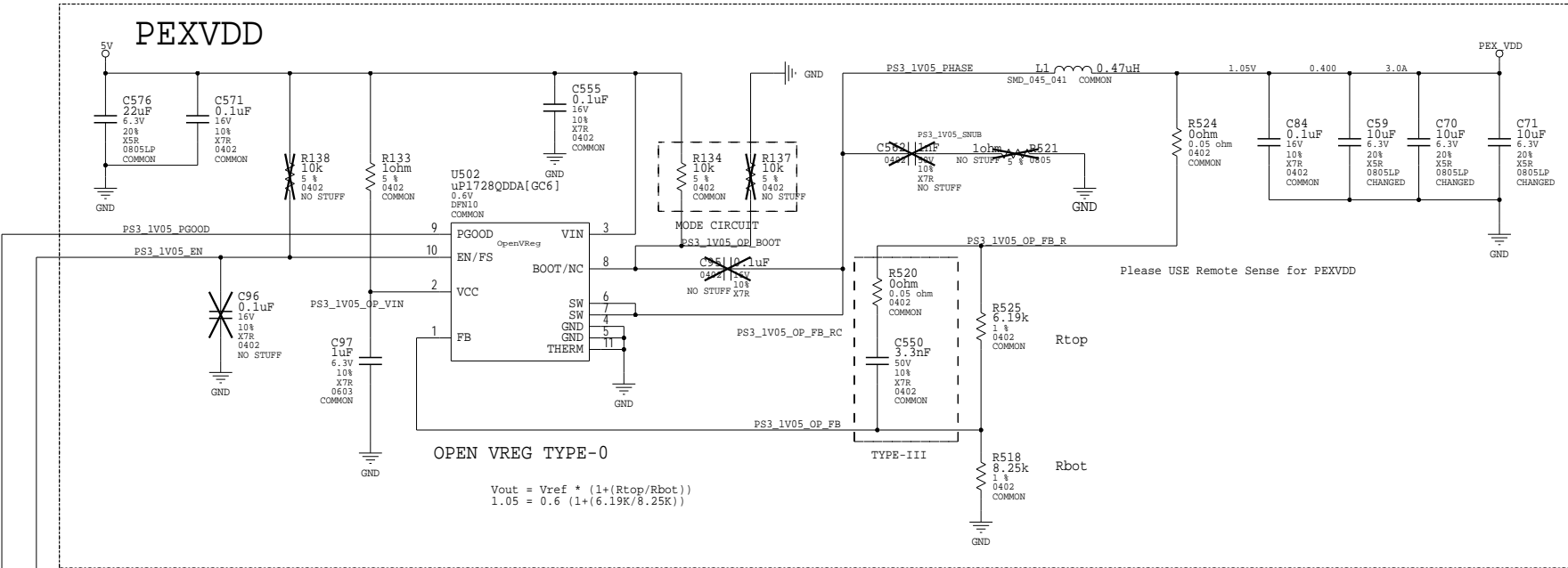
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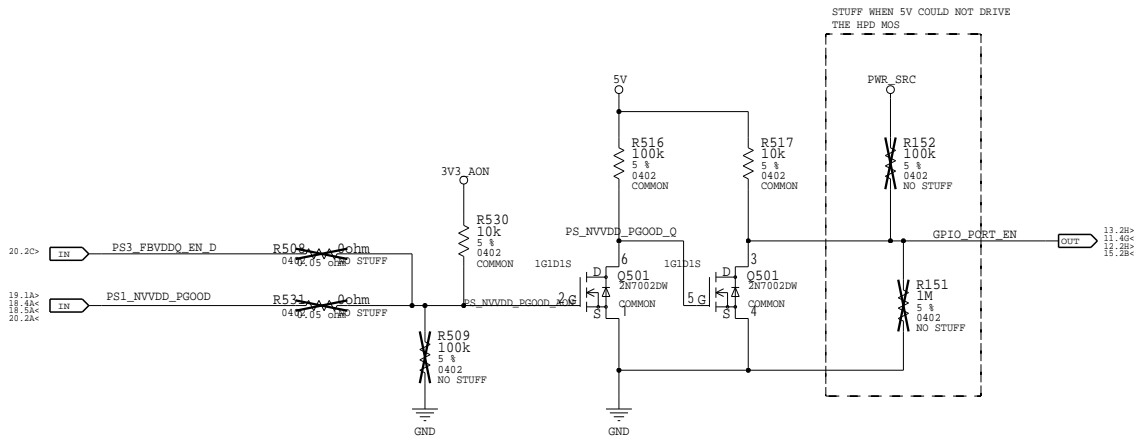
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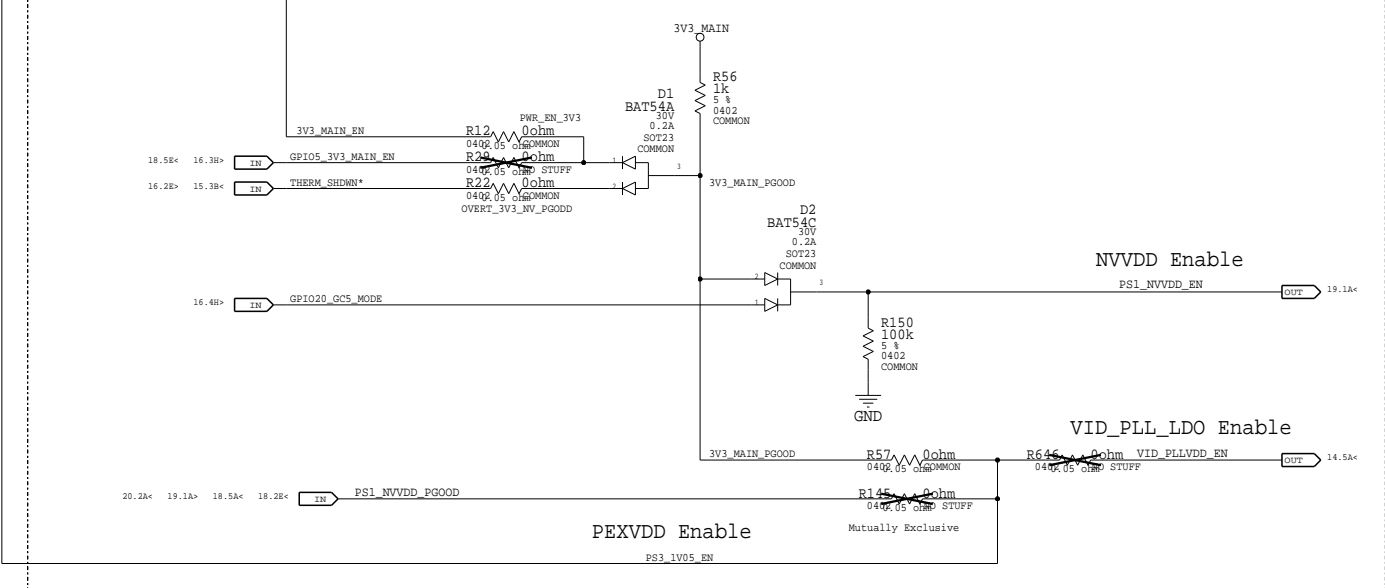
PEXVDD 3V3_AON 3V3_MAIN



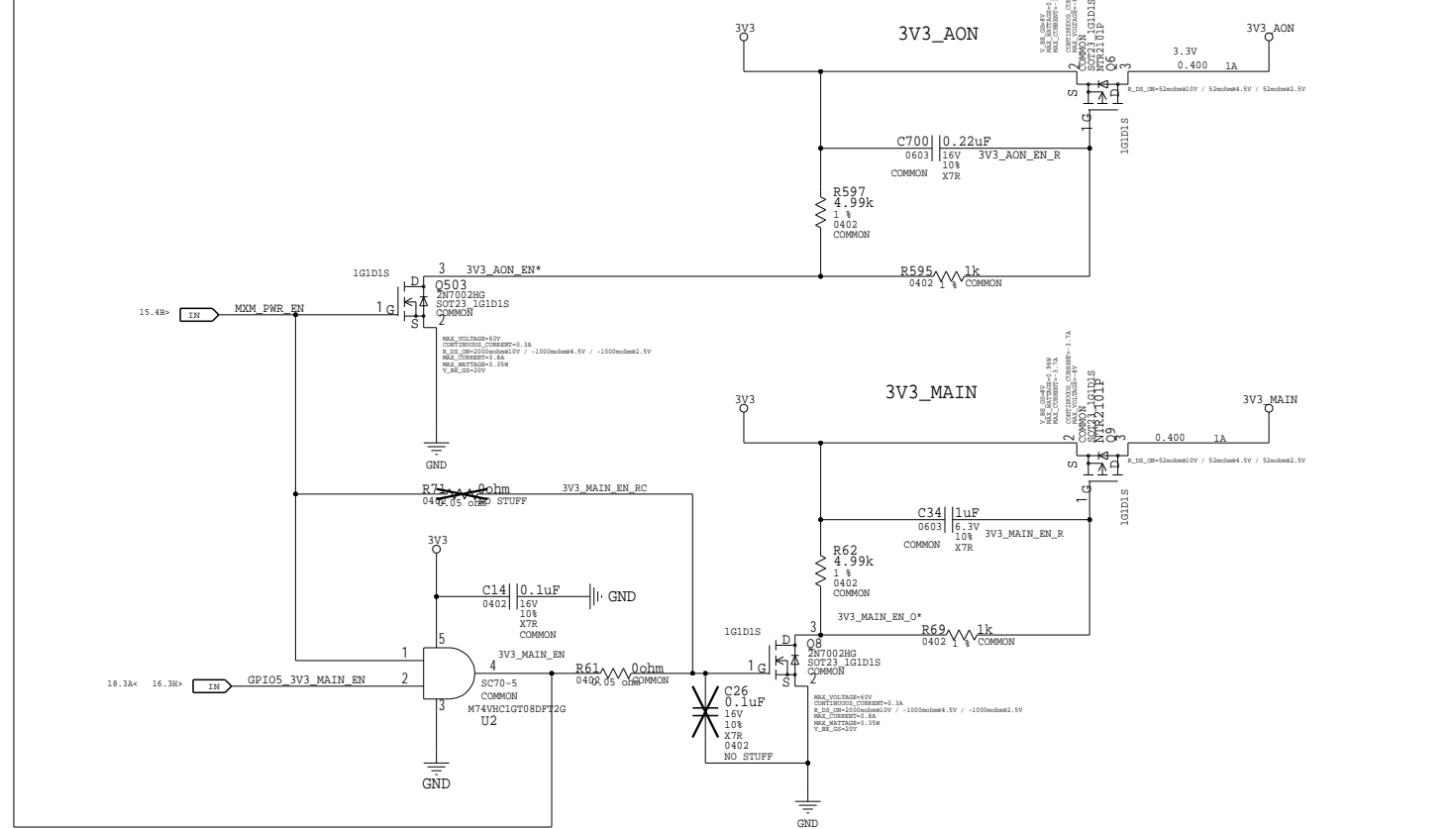
GPIO PROTECT ENABLE



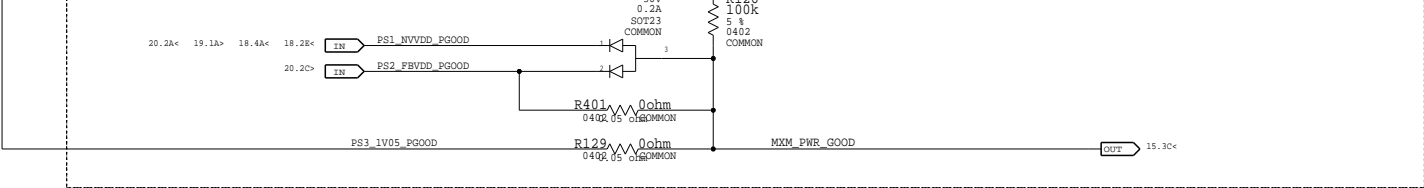
NVVDD&PEXVDD ENABLE



3V3_MAIN&3V3_AON ENABLE



MXM POWER GOOD



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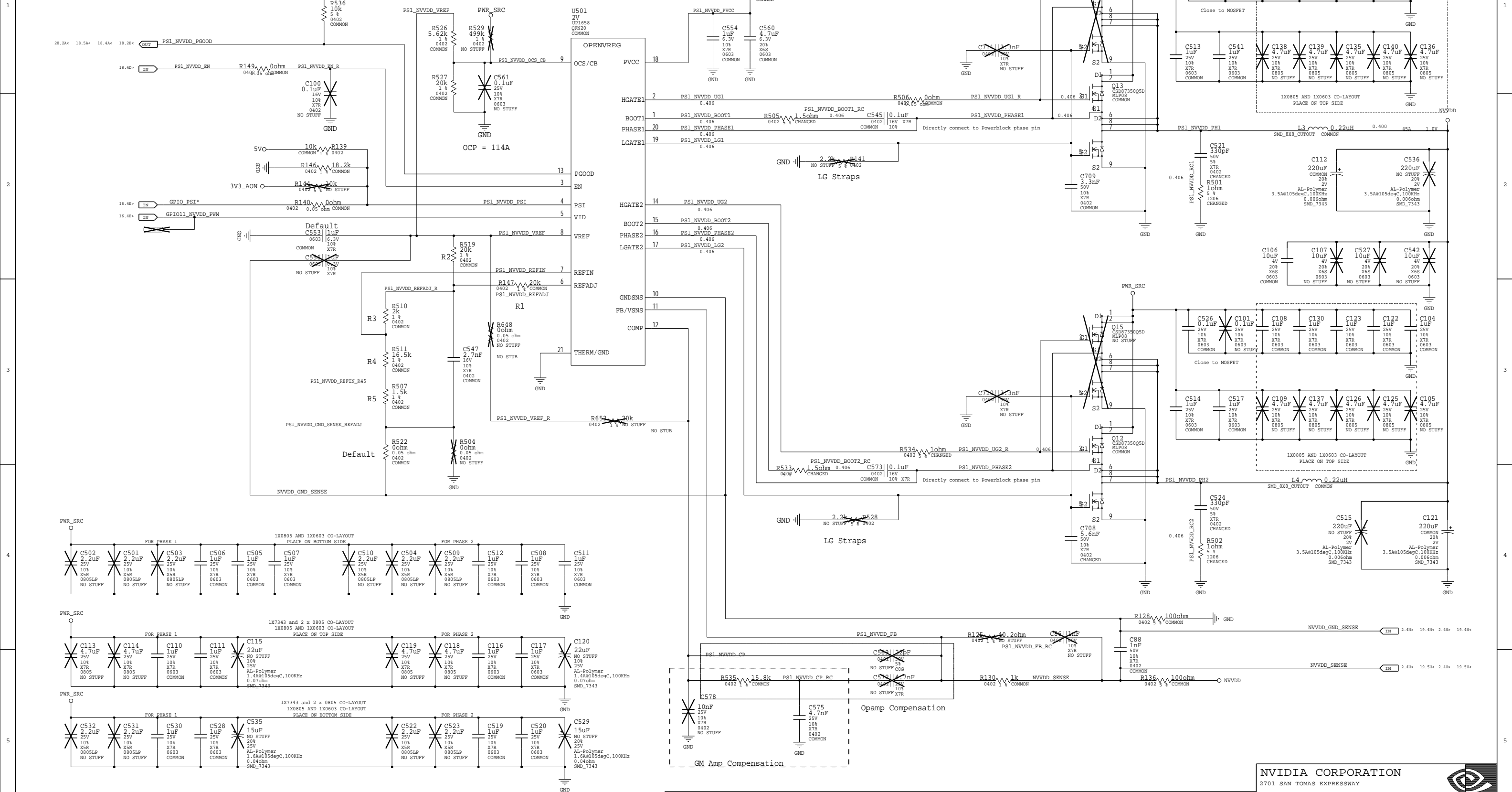
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NVVDD POWER SUPPLY

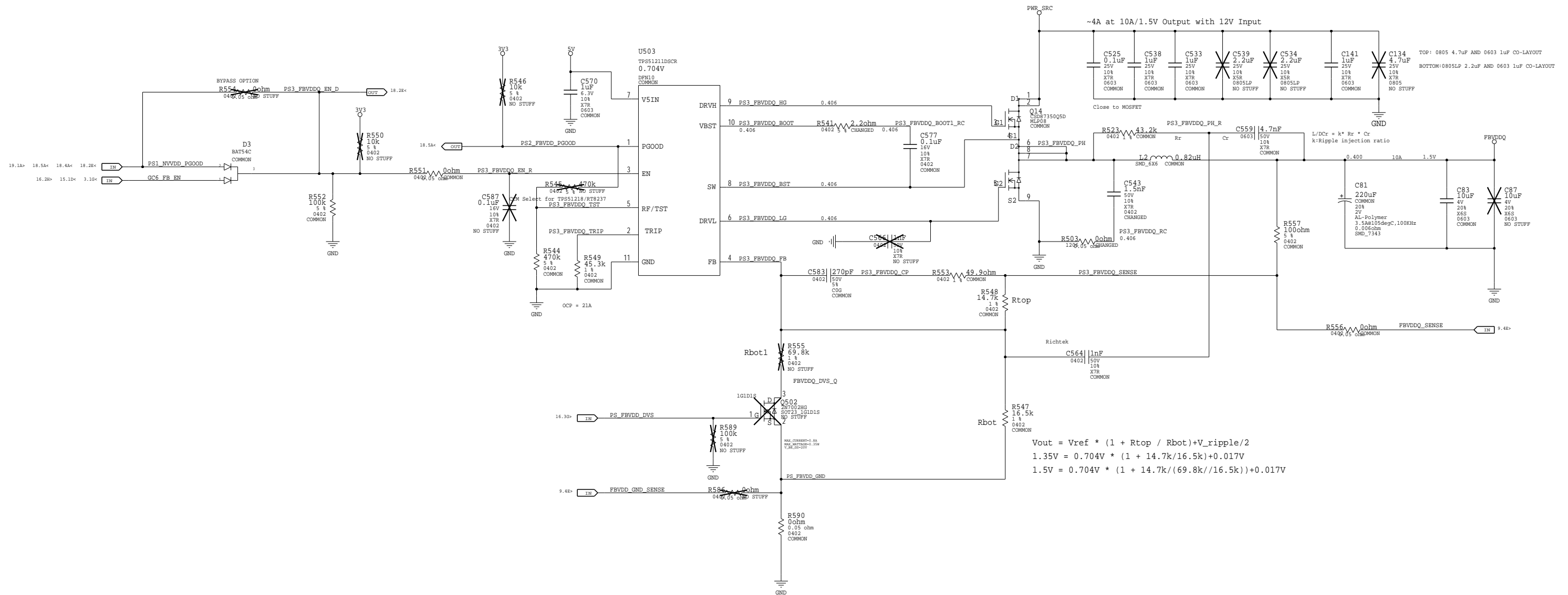



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ASSEMBLY	SKU502 GM107 128Bit X32 GDDR5 MEMORY
PAGE DETAIL	NVDD POWER SUPPLY

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FBVDDQ POWER SUPPLY


$$\begin{aligned} V_{out} &= V_{ref} * (1 + R_{top} / R_{bot}) + V_{ripple}/2 \\ 1.35V &= 0.704V * (1 + 14.7k/16.5k) + 0.017V \\ 1.5V &= 0.704V * (1 + 14.7k/(69.8k//16.5k)) + 0.017V \end{aligned}$$

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		DATE		10-FEB-2015

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