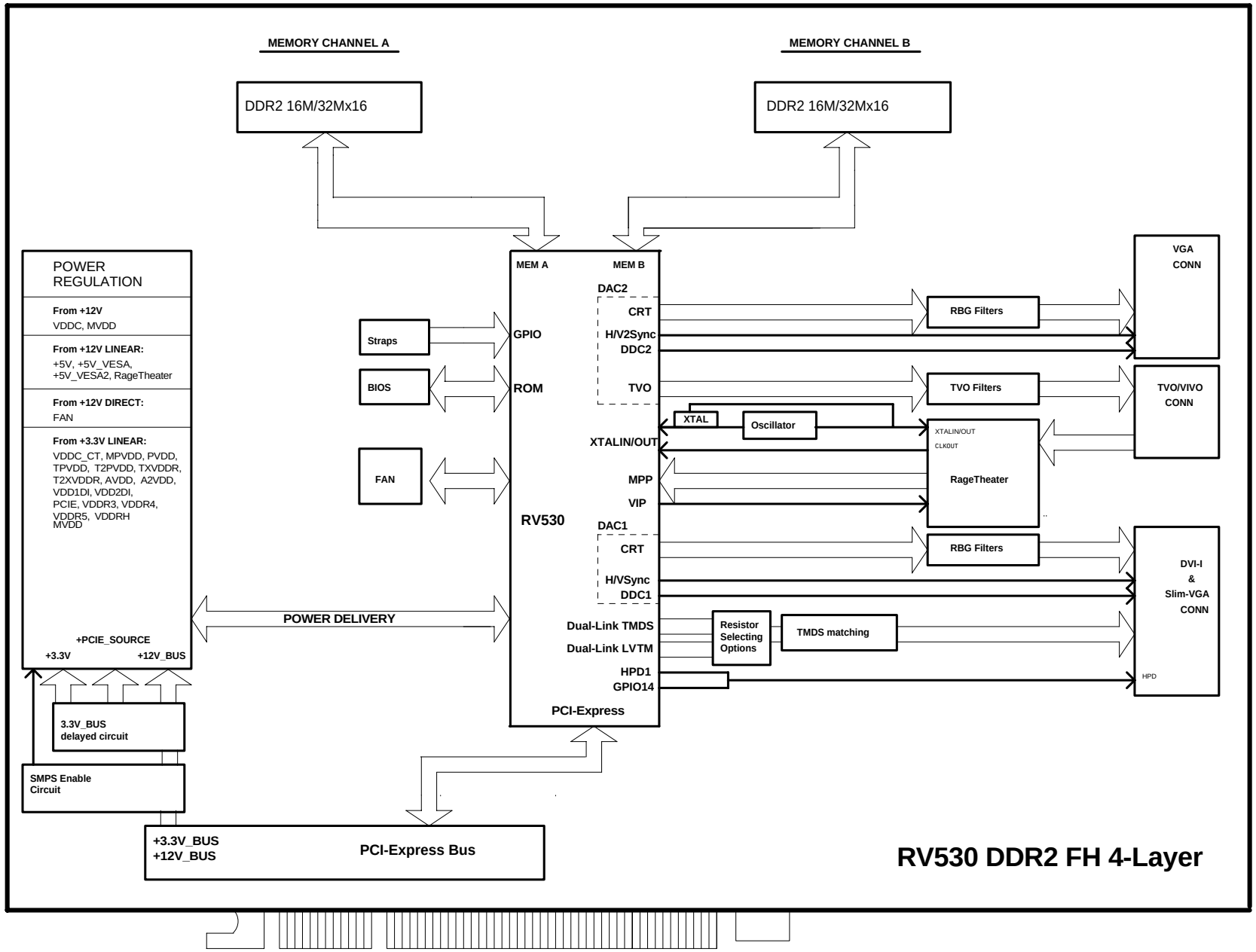
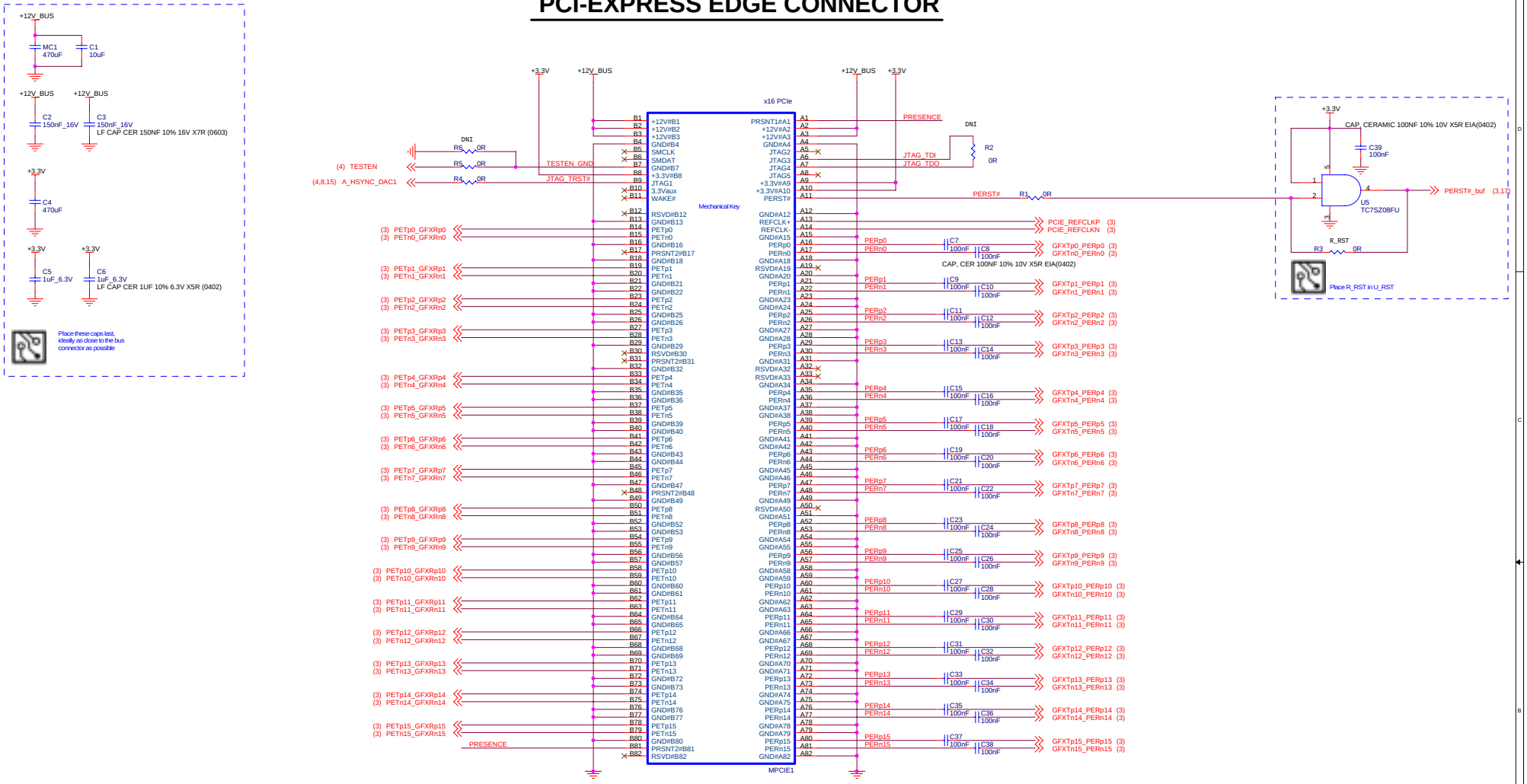


Micro-Star International Co., LTD.		
MS-V040 RV530/DDRII		
Size C	Document Number	Rev 00A
Date: Monday, November 28, 2005	Sheet 1 of 19	

PCI-EXPRESS EDGE CONNECTOR



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

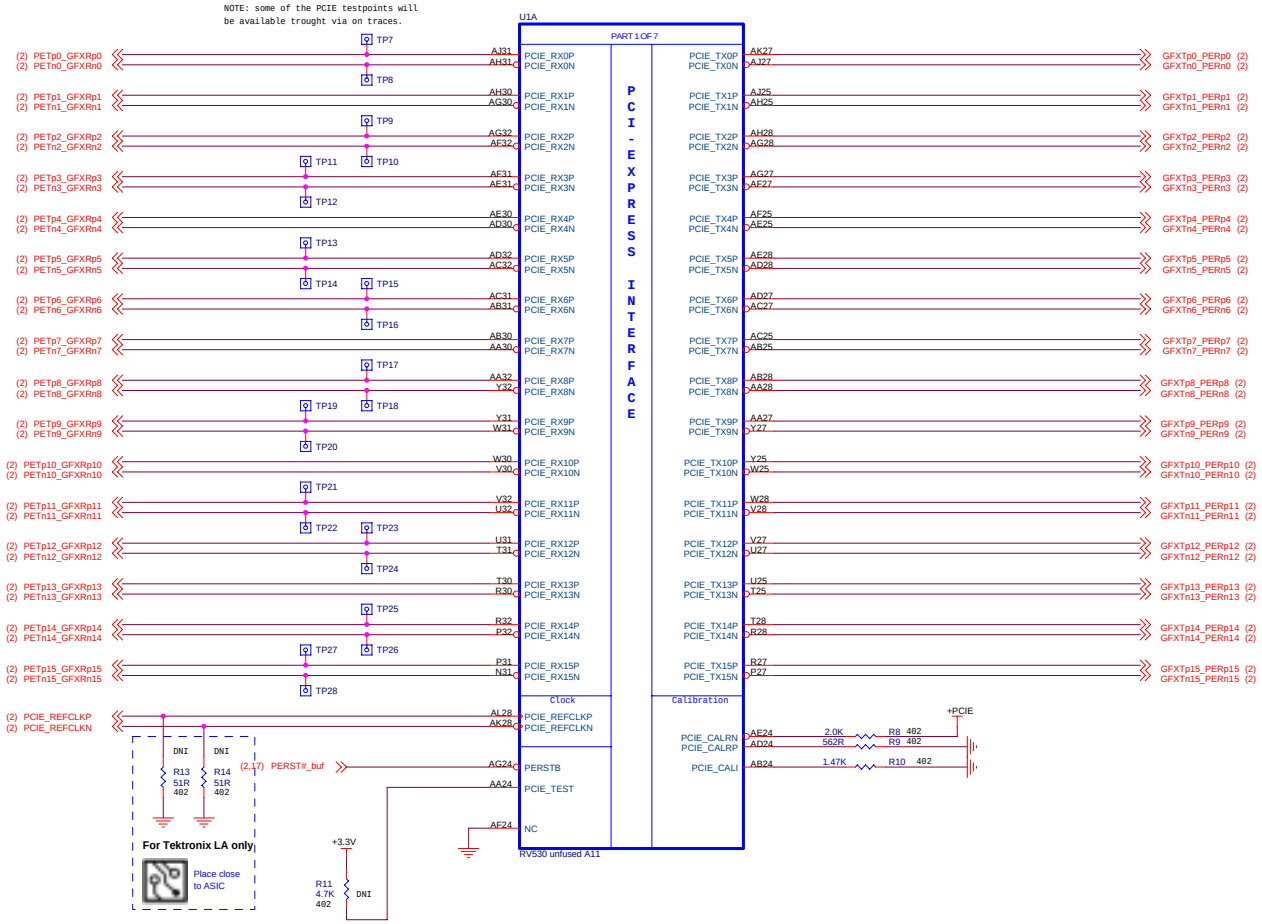
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

Micro-Star International Co., LTD.

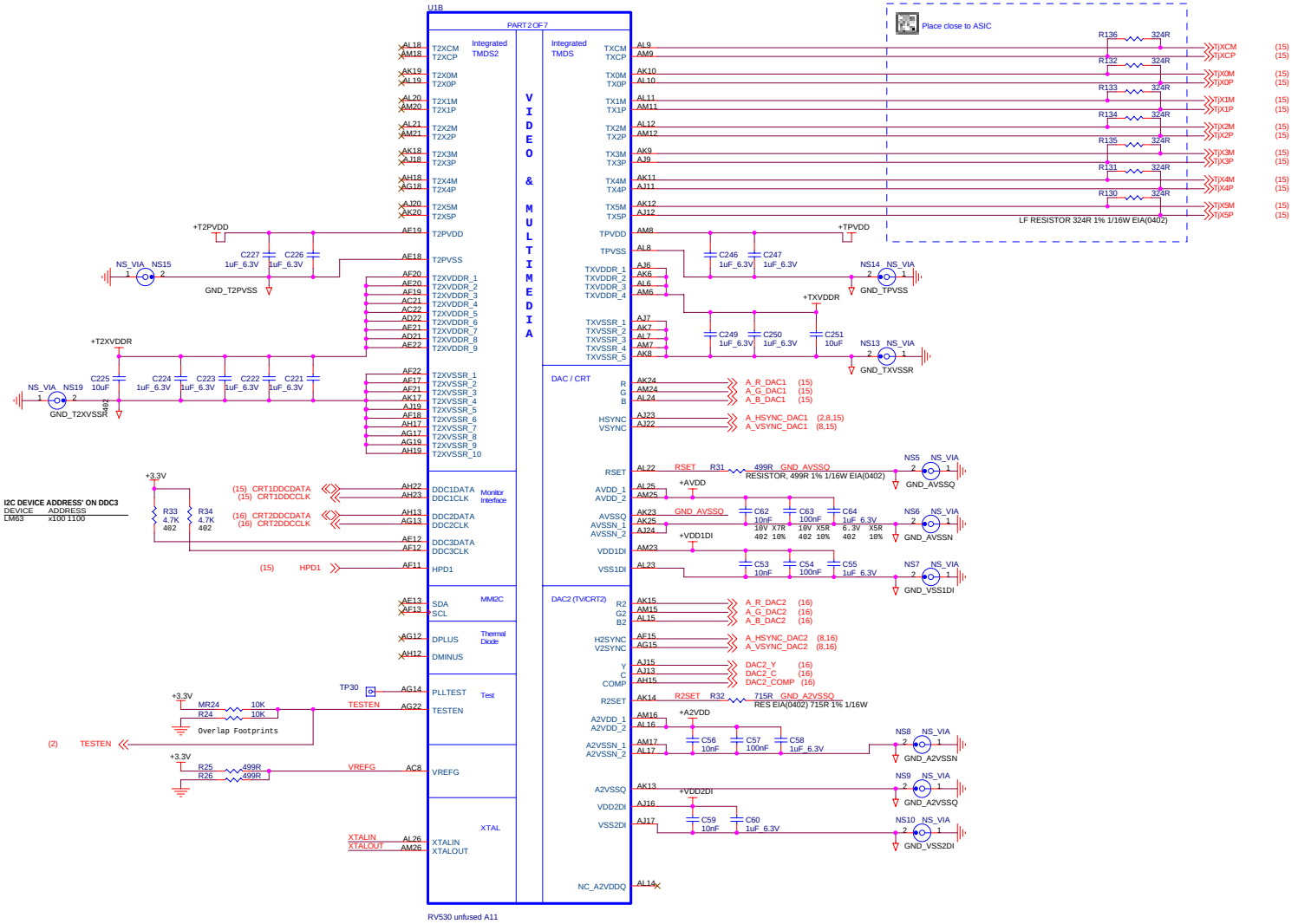
MS-V040 RV530/DDRII

Size	Document Number	Rev
C		0A

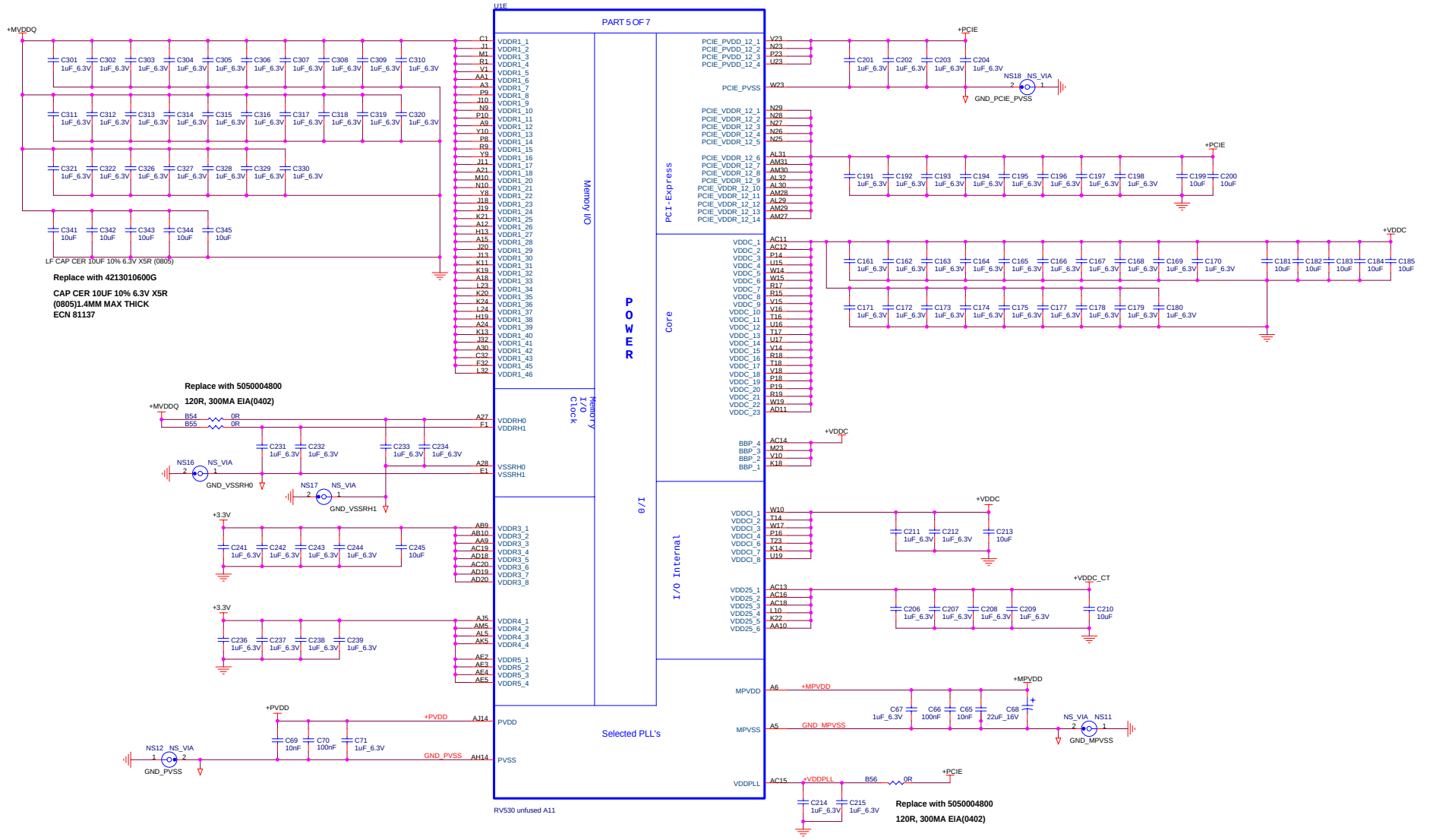
Date: Monday, November 28, 2005 Sheet 2 of 19



Micro-Star International Co., LTD.			
MS-V040 RV530/DDRII			
Size C	Document Number		Rev 00A
Date: Monday, November 28, 2005		Sheet 3 of 22	

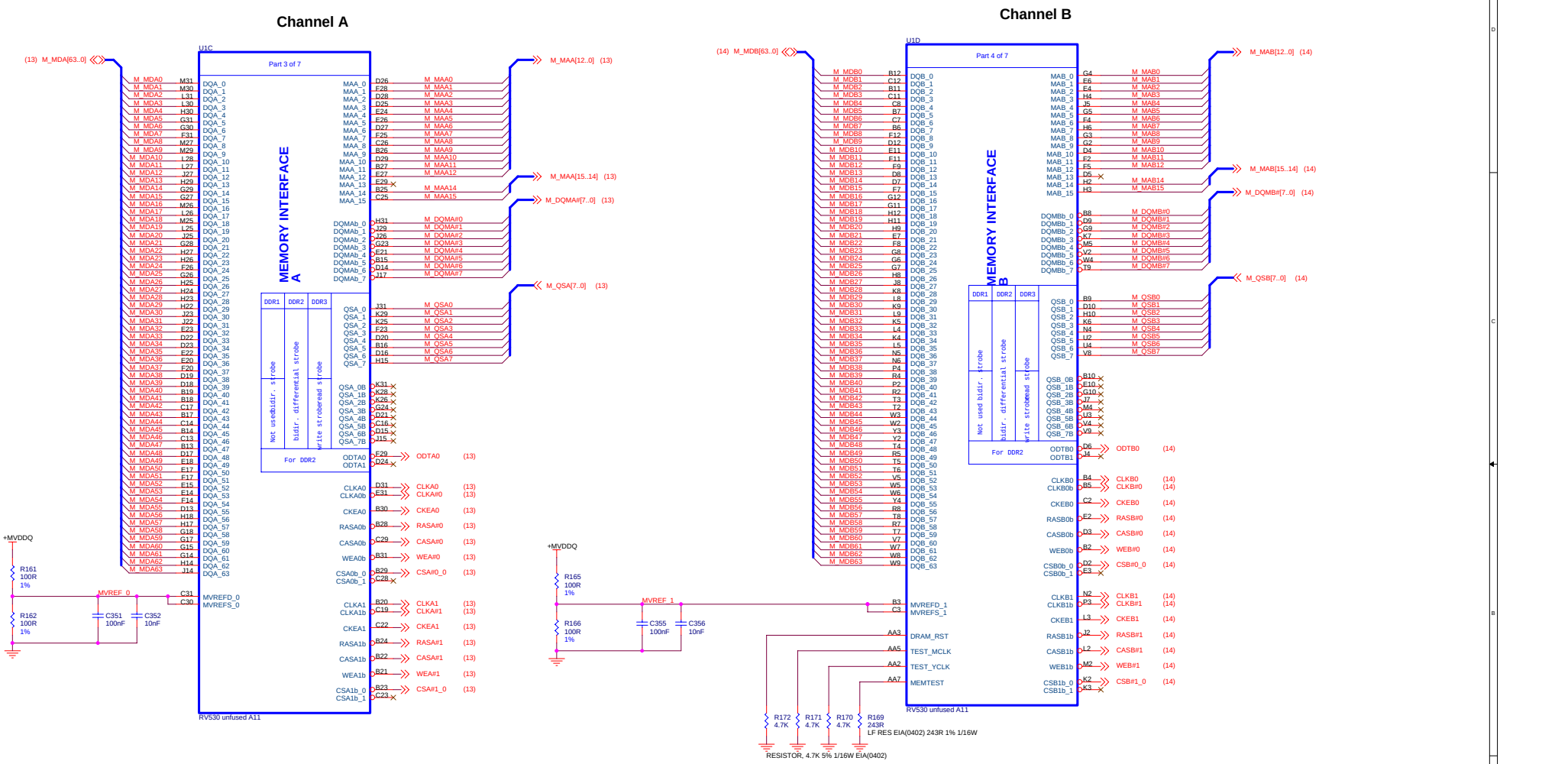


Micro-Star International Co., LTD.			
MS-V040 RV530/DDRII			
Size: Custom	Document Number		Rev: 00A
Date: Monday, November 28, 2005	Sheet 4 of 22		

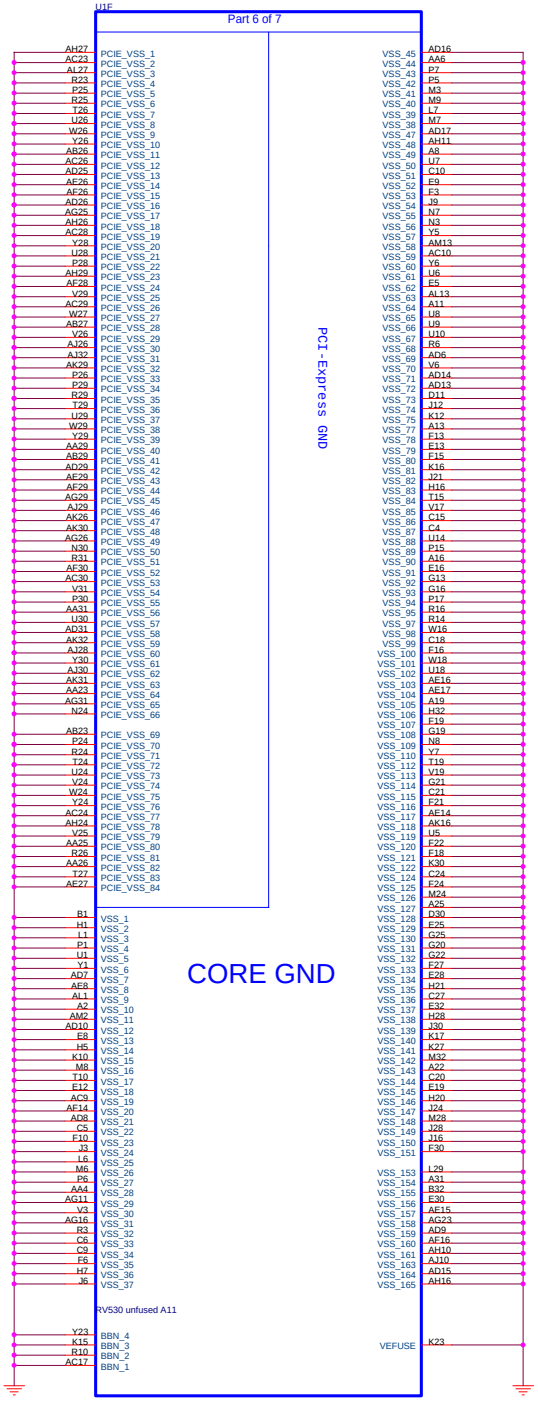


Micro-Star International Co., LTD.			
MS-V040 RV530/DDRII			
Size C	Document Number		Rev 00A
Date: Monday, November 28, 2005	Sheet 5 of 22		

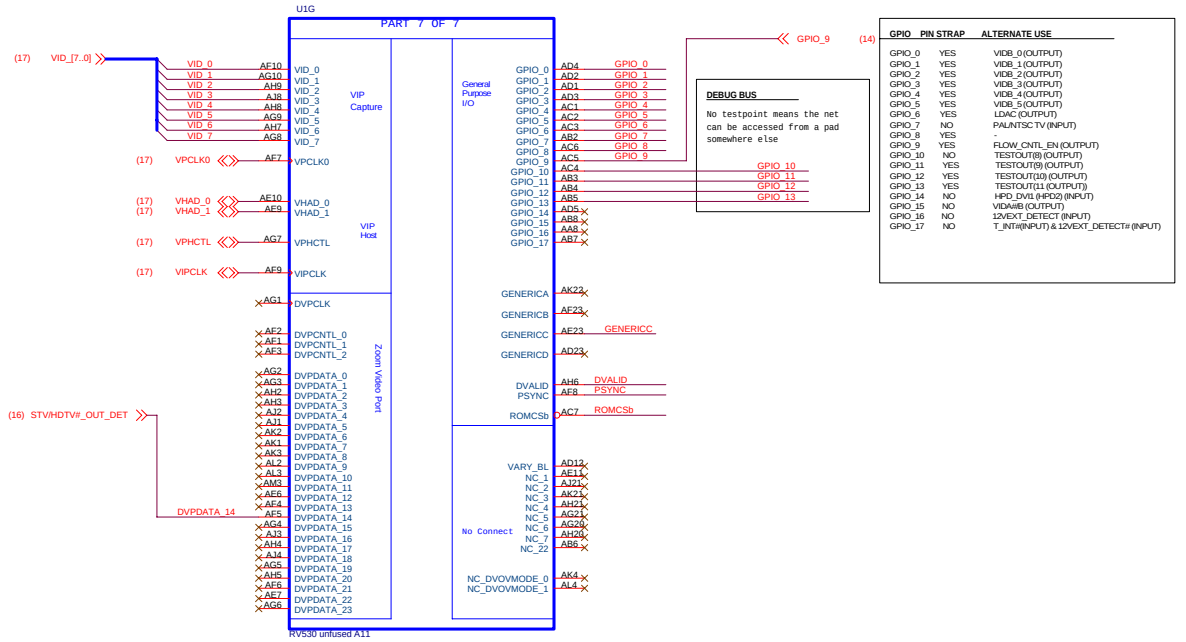
RV530 MEMORY CHANNELS A and B



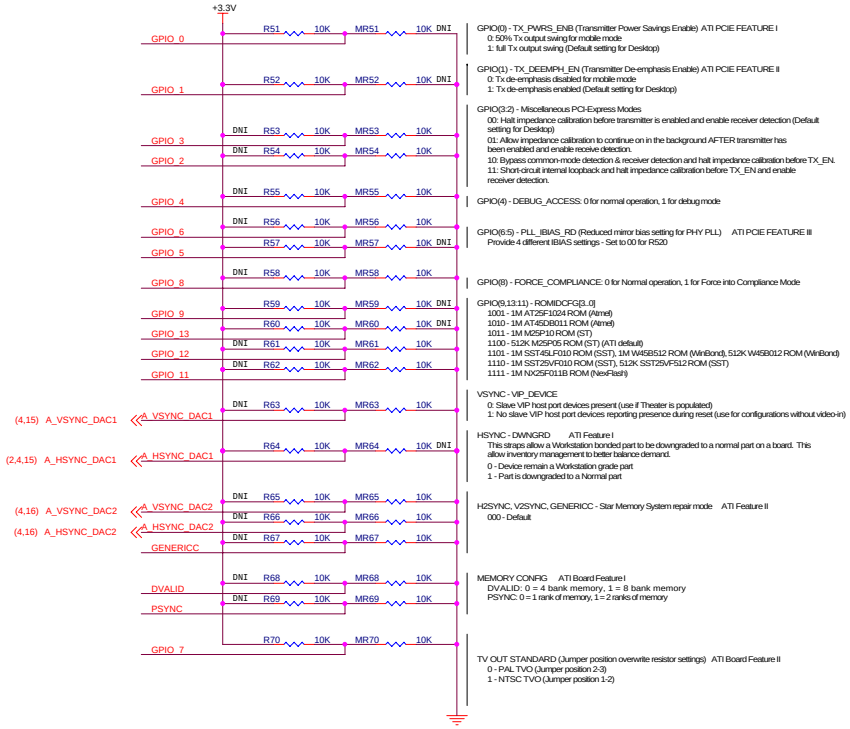
Micro-Star International Co., LTD.			
MS-V040 RV530/DDRII			
Size C	Document Number		Rev 00A
Date: Monday, November 28, 2005	Sheet 6 of 22		

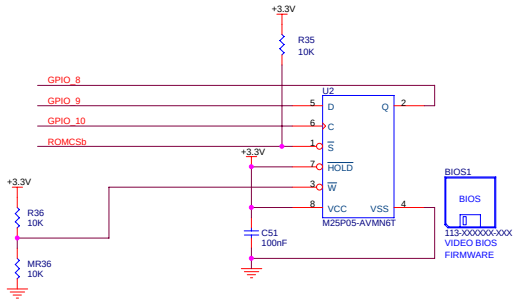


Micro-Star International Co., LTD.	
MS-V040 RV530/DDRII	
Size: C	Document Number
Rev: 00A	
Date: Monday, November 28, 2005	Sheet 7 of 22



PIN BASED STRAPS





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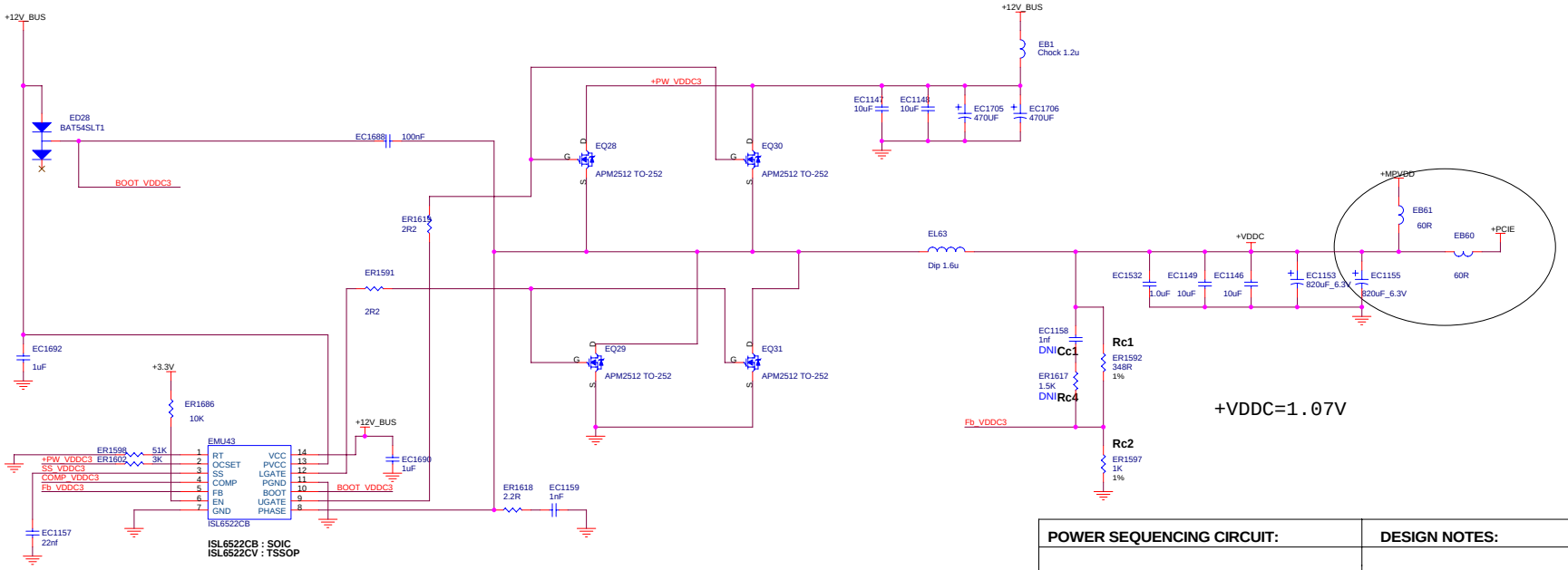
MS-V040 RV530/DDRII

Size	Document Number	Rev
C		0A

Date: Monday, November 28, 2005 Sheet 8 of 19

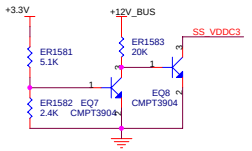
CORE REGULATOR VDDC



+VDDC=1.07V

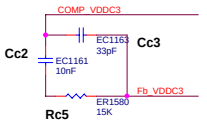
Lower MOSFET should be surrounded by a lot of copper for heat dissipation

POWER SEQUENCING CIRCUIT:



DESIGN NOTES:

Compensation Circuit



FOR ALTERNATE #1

Remove R374, R375, R371, C168 and U32

Install R370, R112, R954, R305-R308, C166, C159 and MU32

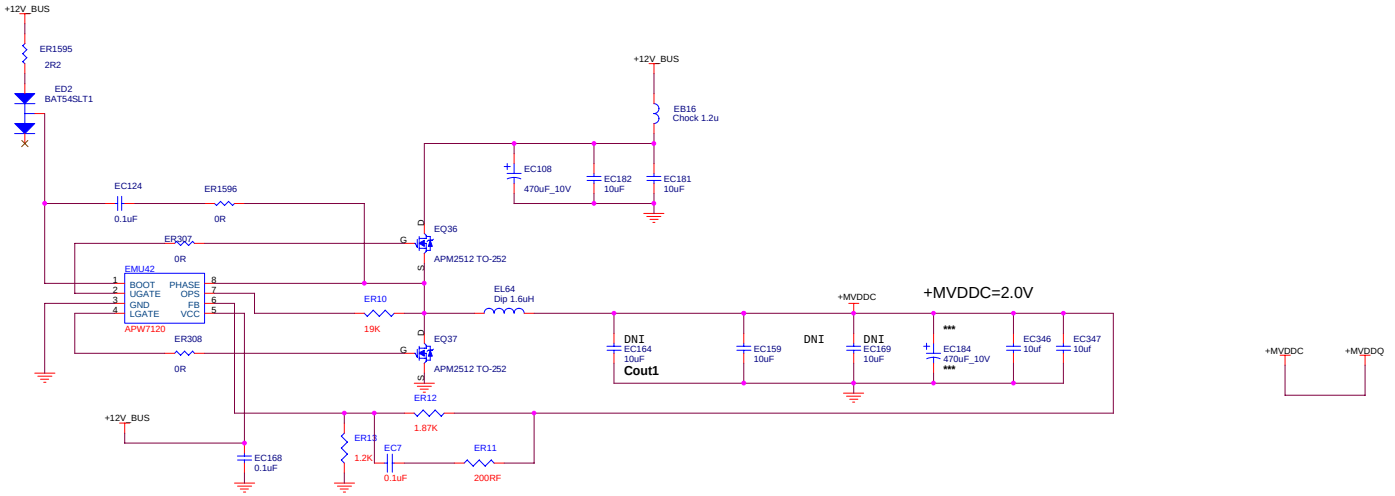
FOR ALTERNATE #2

Change C157 for 10 uF and C121 for 1 uF
Replace C764 by 0 Ohm resistor
Replace R314 with a bead
Remove R954, R370, R305-R308, C159, R112, C160 and MU32

Install R374, R375, R371, C168 and U32

Compensation circuit

Rc1 = 10K, Rc2 = 8.06K
R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF



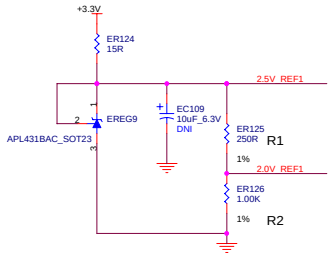
Micro-Star International Co., LTD.	
MS-V040 RV530/DDRII	
Size: Custom	Document Number:
Rev: 0A	
Date: Monday, November 28, 2005	Sheet 10 of 19

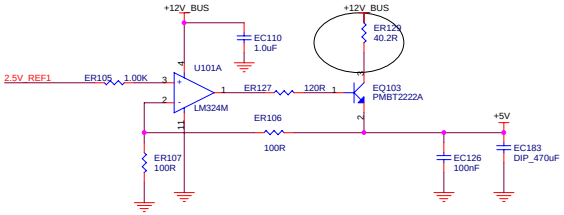
Micro-Star International Co., LTD.

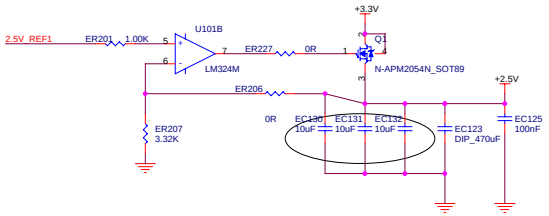
MS-V040 RV530/DDRII

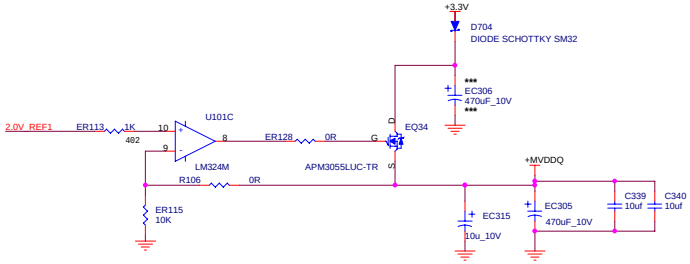
Size	Document Number	Rev
Custom		0A

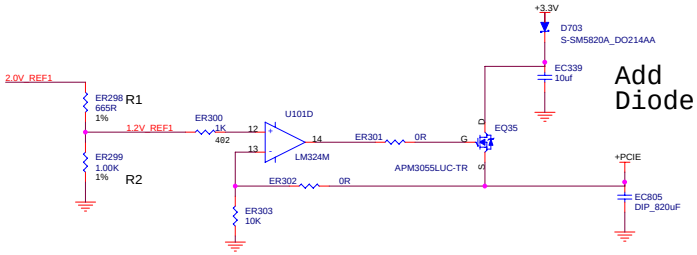
Date: Monday, November 28, 2005 Sheet 11 of 19

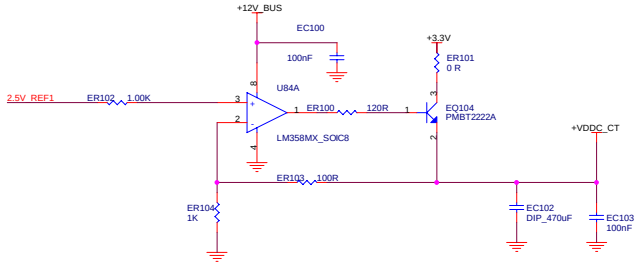


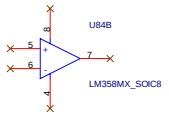








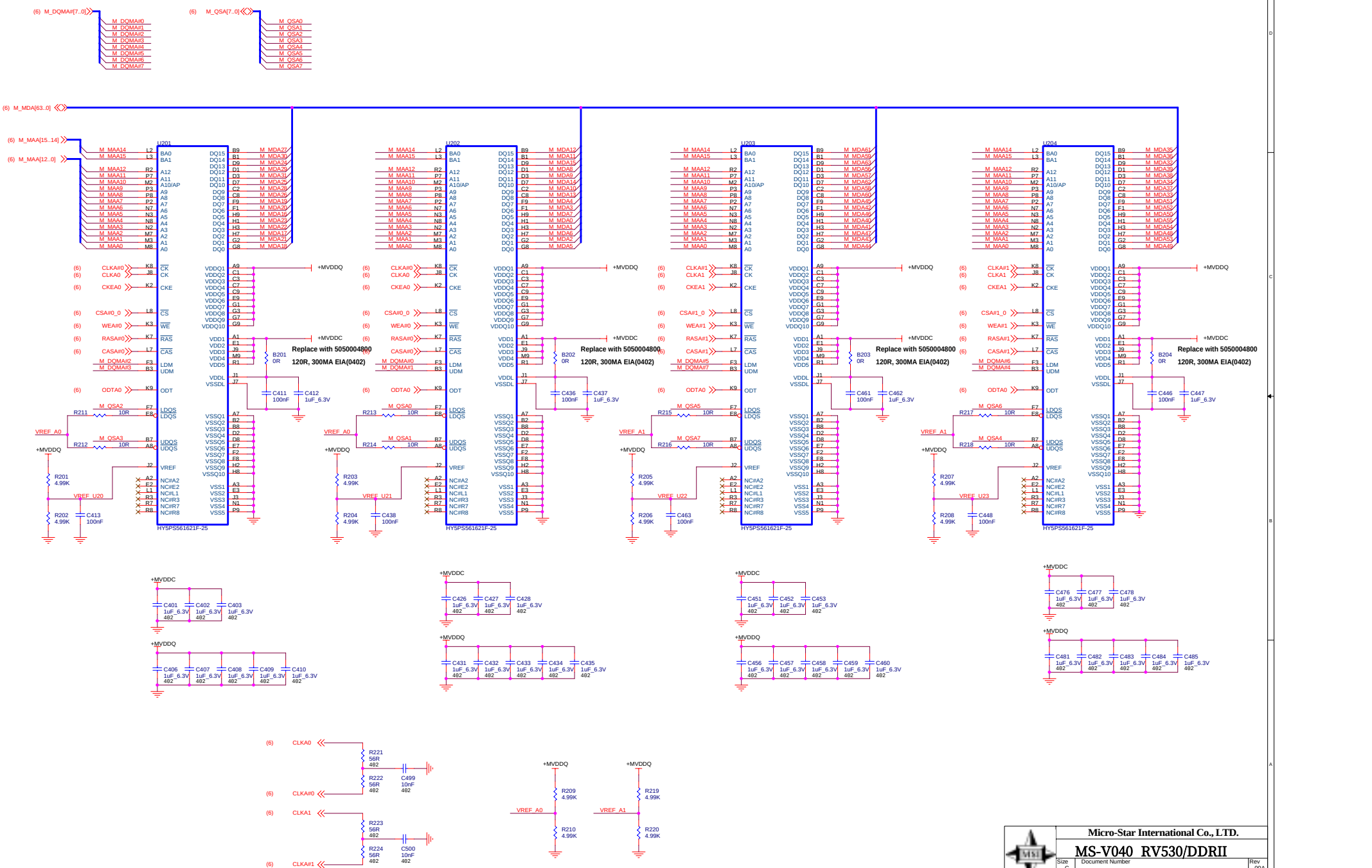




Replace with 5050004800
120R, 300MA EIA(0402)

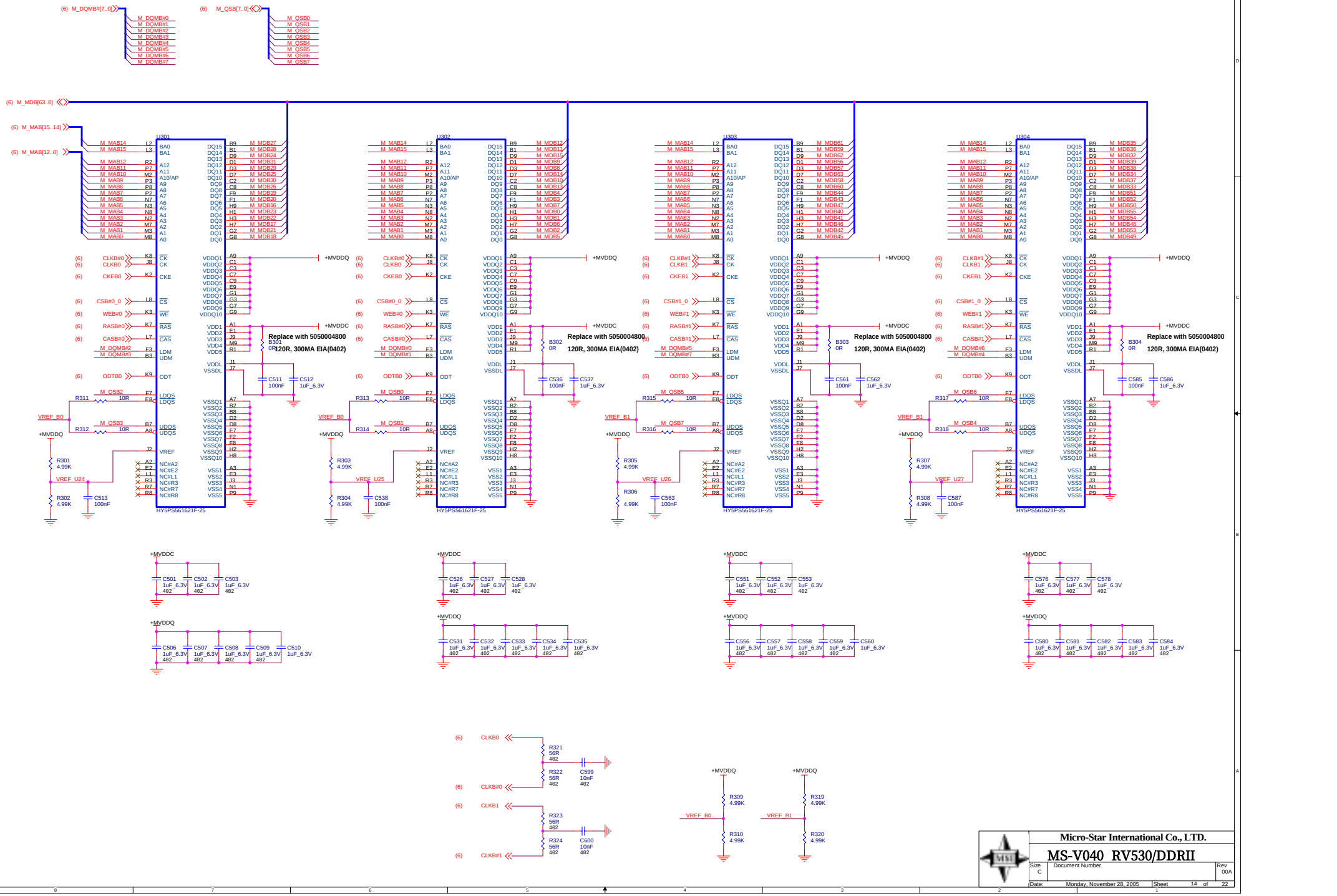
Micro-Star International Co., LTD.			
MS-V040 RV530/DDRII			
Size C	Document Number		Rev 00A
Date: Monday, November 28, 2005		Sheet 12 of 22	

CHANNEL A: RANK 0 128MB DDR2

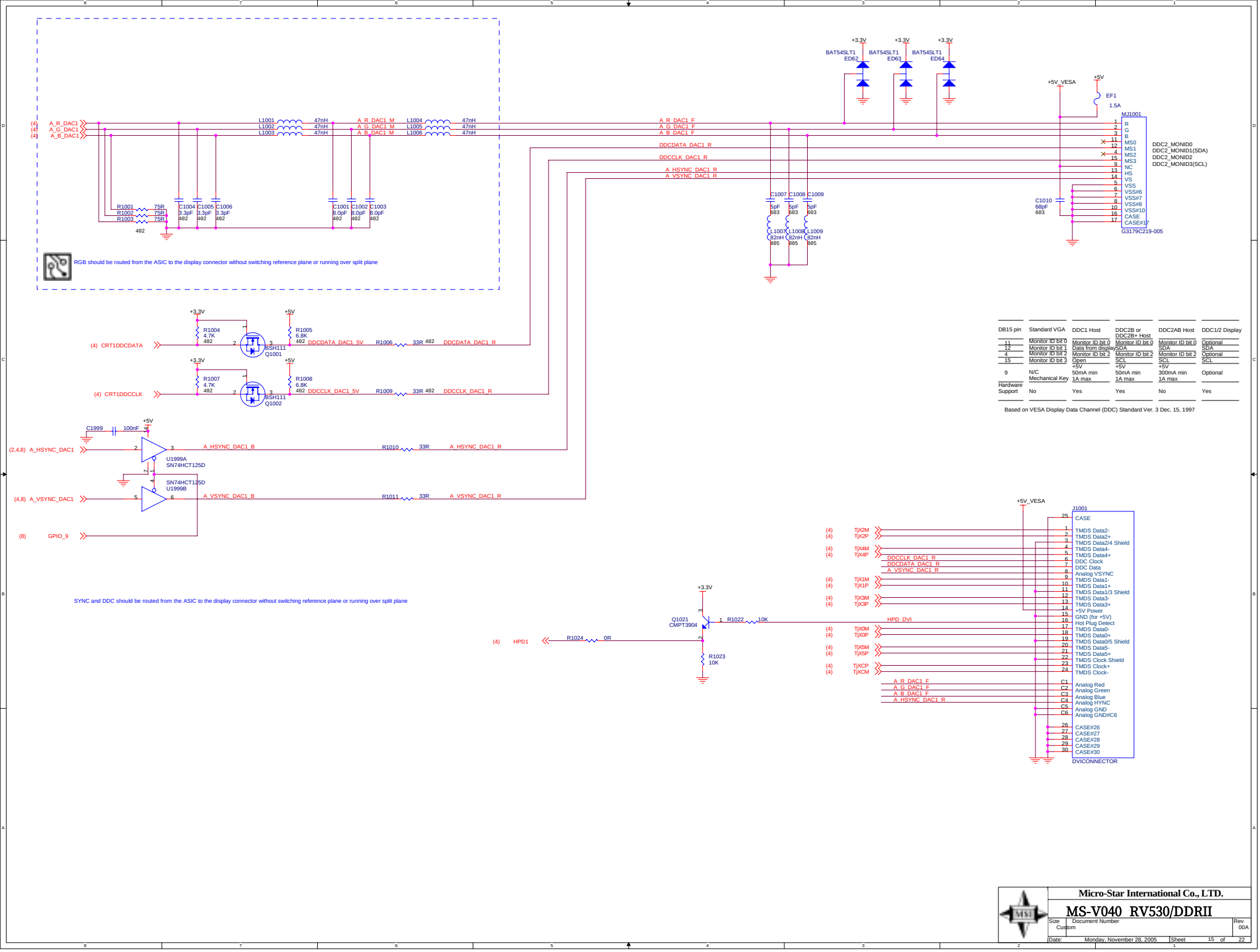


Micro-Star International Co., LTD.		
MS-V040 RV530/DDRII		
Size C	Document Number	Rev 00A
Date: Monday, November 28, 2005	Sheet 13 of 22	

CHANNEL B: RANK 0 128MB DDR2



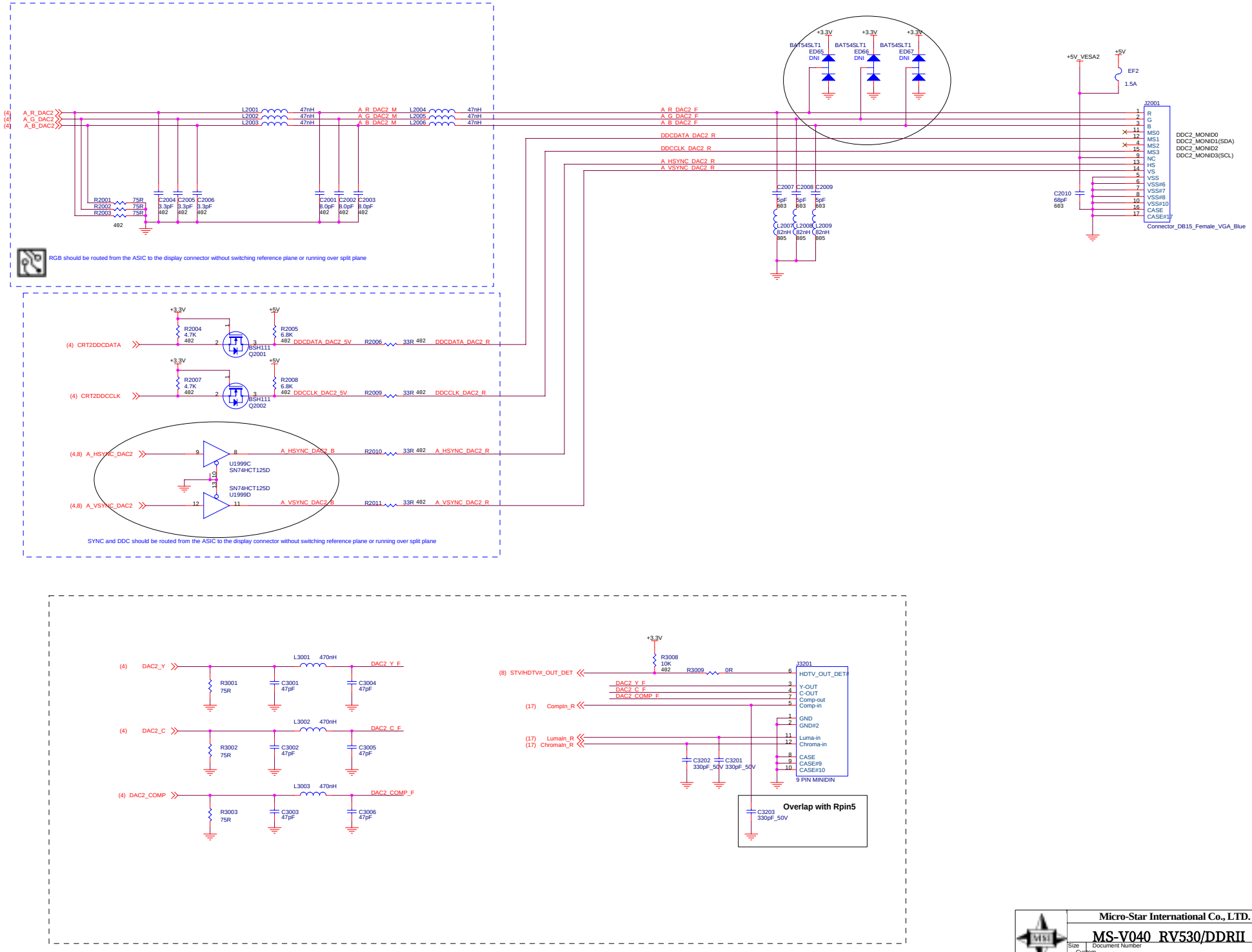
Micro-Star International Co., LTD.	
MS-V040 RV530/DDRII	
Size C	Document Number — Rev 00A
Date: Monday, November 28, 2005	Sheet 14 of 22



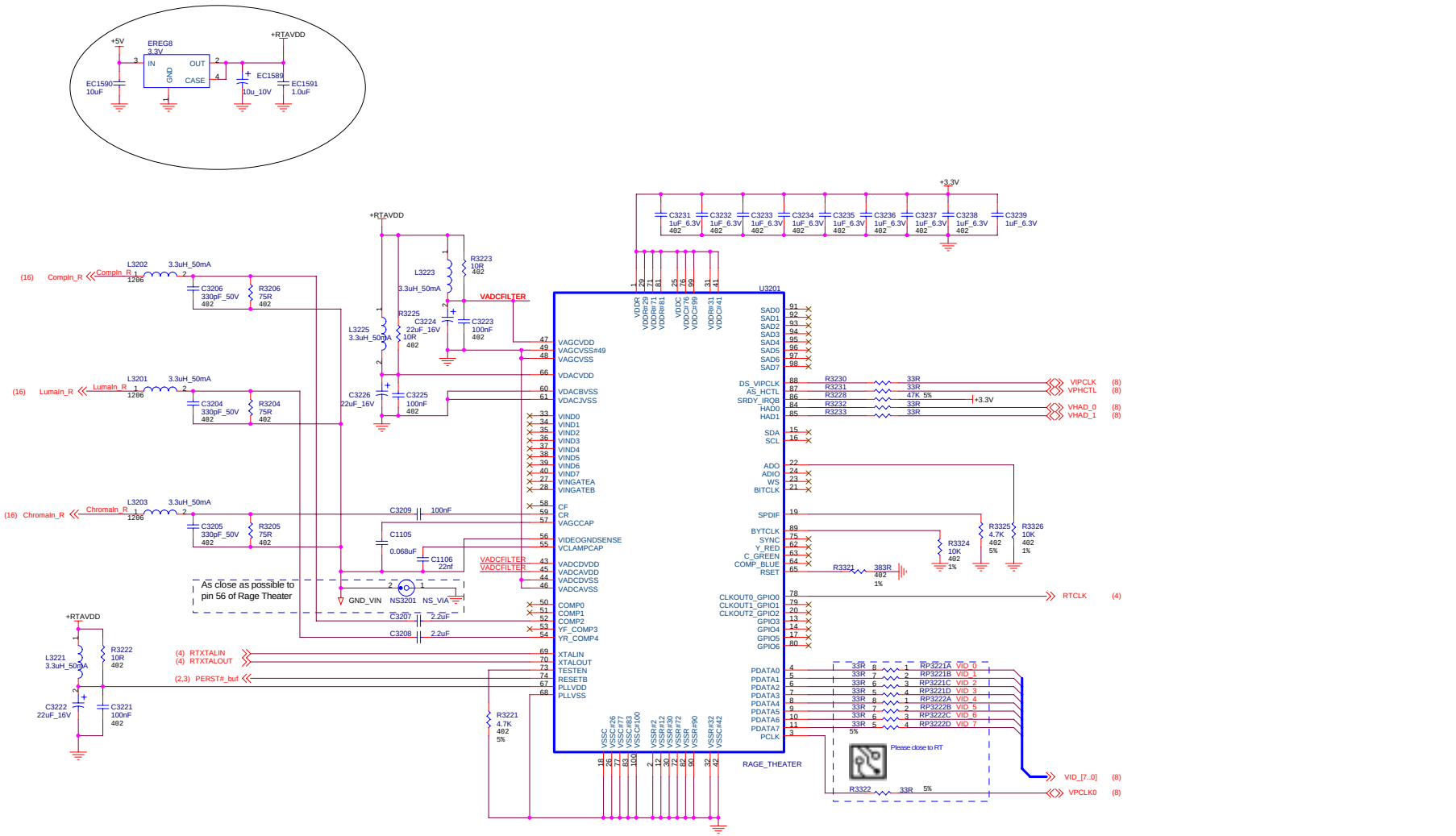
DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V	+5V	+5V	Optional
	Mechanical Key	50mA min 1A max	50mA min 1A max	300mA min 1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

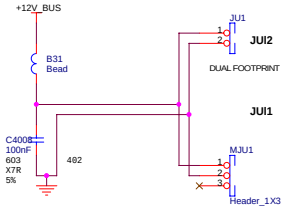
Micro-Star International Co., LTD.					
MS-V040 RV530/DDRII					
Size: Custom	Document Number				Rev: 00A
Date: Monday, November 28, 2005			Sheet 15 of 22		



Micro-Star International Co., LTD.		
MS-V040_RV530/DDRII		
Size: Custom	Document Number	Rev: 00A
Date: Monday, November 28, 2005	Sheet 16 of 22	



Micro-Star International Co., LTD.			
MS-V040 RV530/DDRII			
Size C	Document Number		Rev 00A
Date: Monday, November 28, 2005	Sheet 17 of 18		



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MS-V040 RV530/DDRII

Size	Document Number	Rev
C		0A

Date: Monday, November 28, 2005 Sheet 18 of 19

DVI/VGA SCREWS

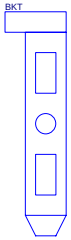
SCREW1
SCREW
JACKSCREW ASSY
7020000800

SCREW2
SCREW
JACKSCREW ASSY
7020000800

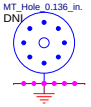
SCREW3
SCREW
JACKSCREW ASSY
7020000800

SCREW4
SCREW
JACKSCREW ASSY
7020000800

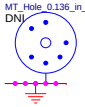
BKT



MT1
MT_Hole_0.136_in.
DNI



MT2
MT_Hole_0.136_in_6VIA
DNI



FM1 SW_FB
FM5 SW_FB
FM2 SW_FB
FM6 SW_FB
FM3 SW_FB
FM4 SW_FB

PCB

H2

LOW PROFILE HS

J1 X_PIN1*2
J3 X_PIN1*2
J2 X_PIN1*2
J4 X_PIN1*2

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MS-V040 RV530/DDRII

Size	Document Number	Rev
C		00A

Date: Monday, November 28, 2005 Sheet 19 of 22

<variant Name>

Title	Schematic No.	Date:
MS-V040 RV5xx DDR2 VGA 2xDVI VIVO FH	MS-V040-11	**Monday, November 28, 2005**

REVISION HISTORY

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	10		
1	11	05/10/04	1:Add Page12 3.3V to PCI-E PWR Diode: D703 2:Add Page12 +2.5V 10U Cap, EC130,EC131,EC132