1. VS1 added between GND to AGND and placed close to Pin 33 of U503 on page 33(6/12)

PG165-B01

TU116 6GB GDDR5, 192b, X32
DVI-D + DP + HDMI

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2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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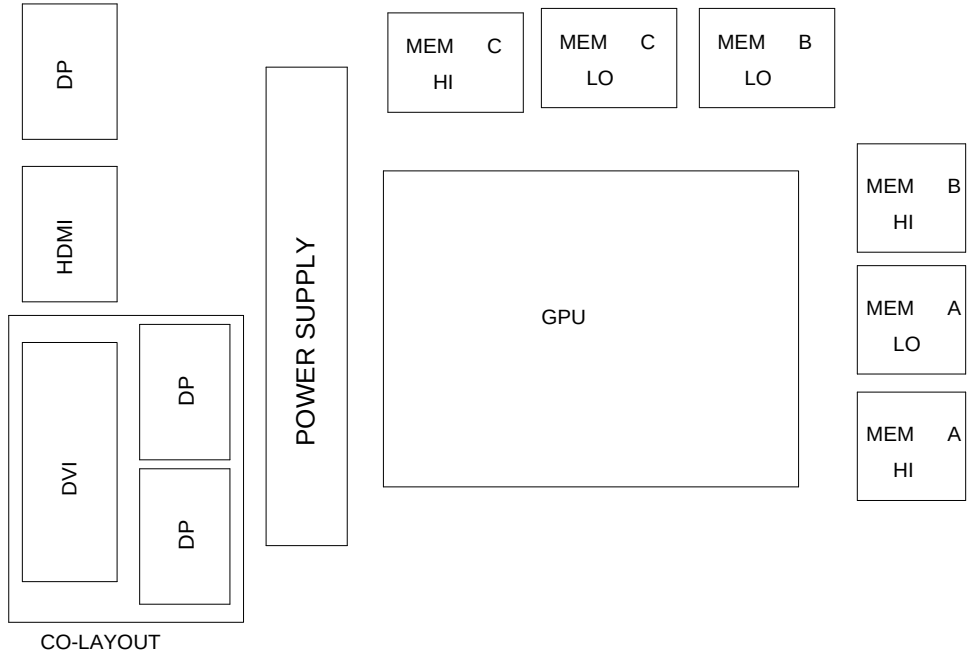
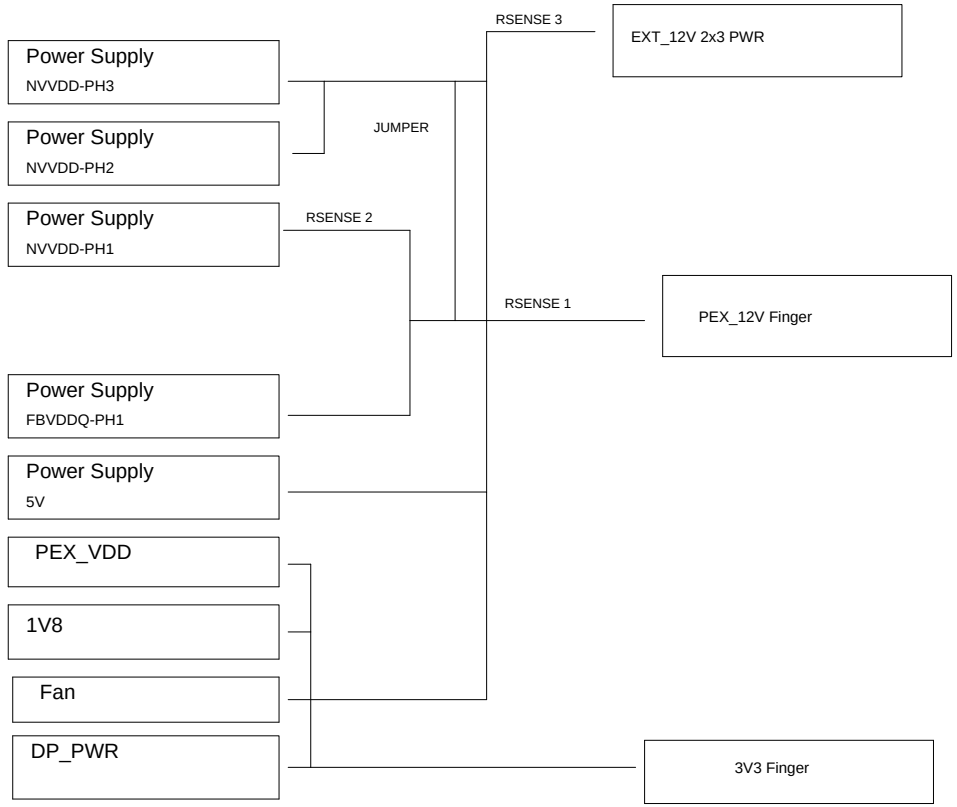
Page2: Block Diagram



CO-LAYOUT

Power Supply:

NVVDD = RSENSE 2 * 3
FBVDD = (RSENSE 1-RSENSE 2)
TGP = RSENSE 1 + RSENSE 3



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Block Diagram

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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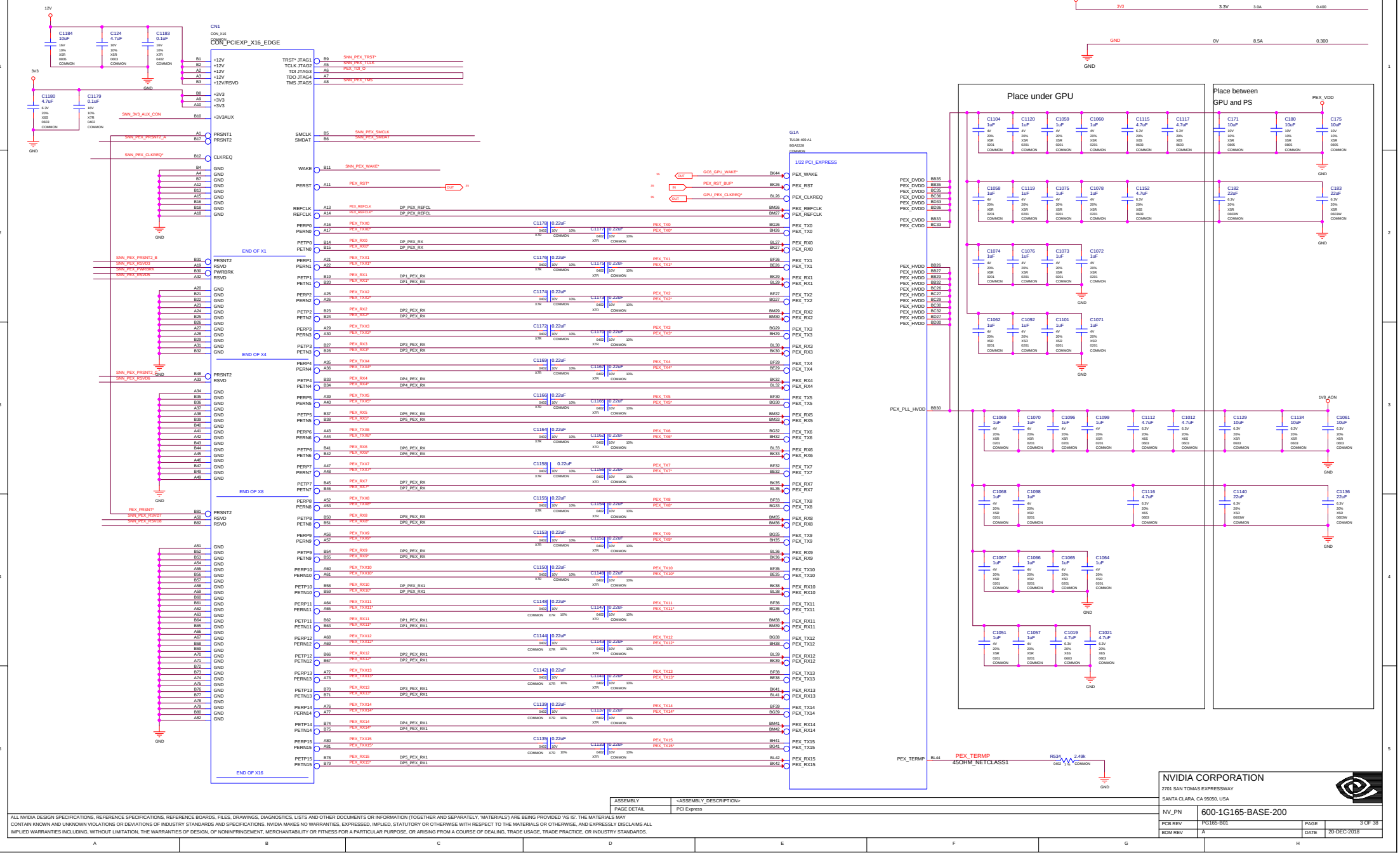
Page3: PCI Express



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.406
3V3	3.3V	3.0A	0.400
GND	0V	8.5A	0.300

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI Express

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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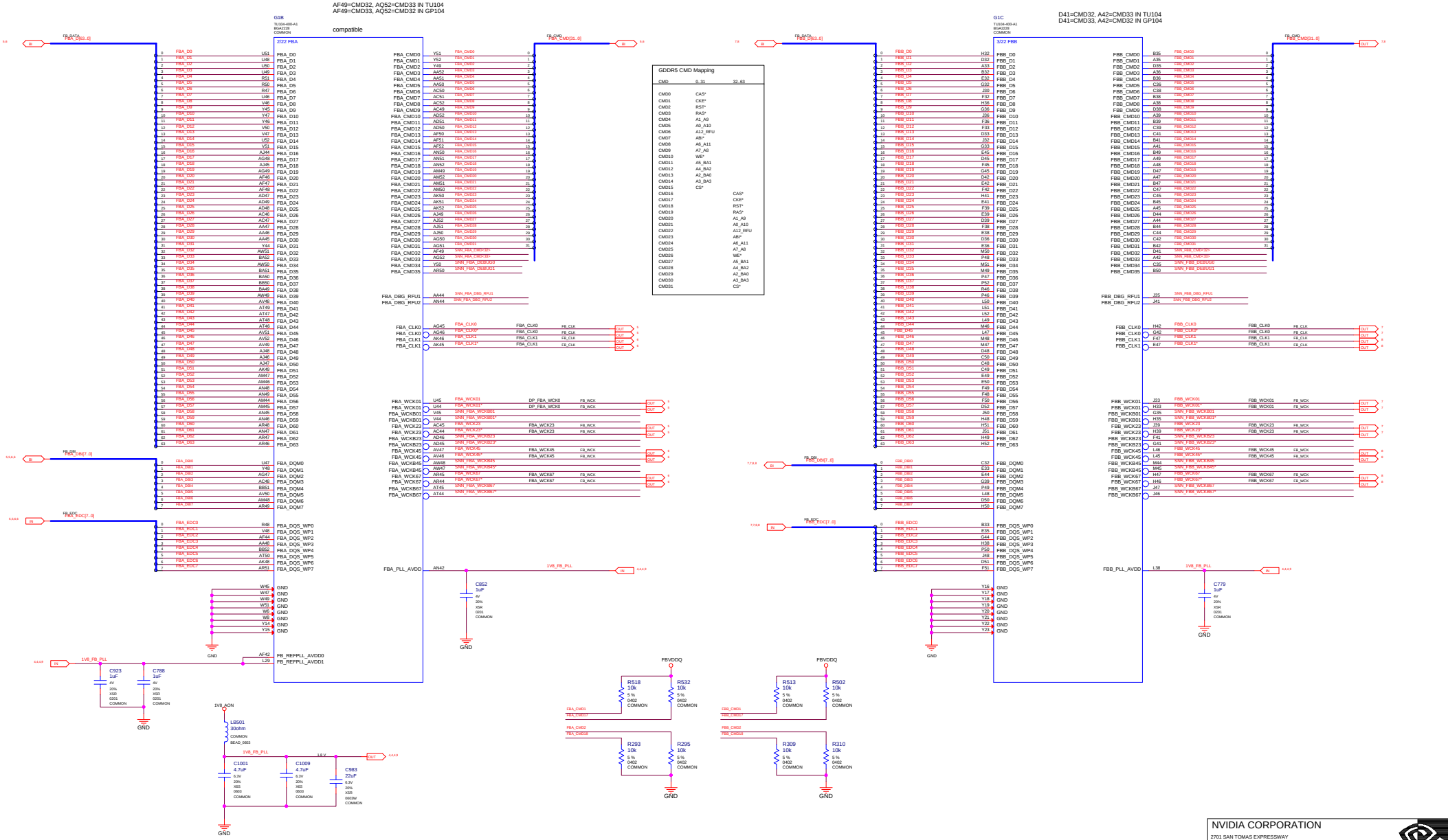
Page4: MEMORY: GPU Partition A/B



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: GPU FB_AB

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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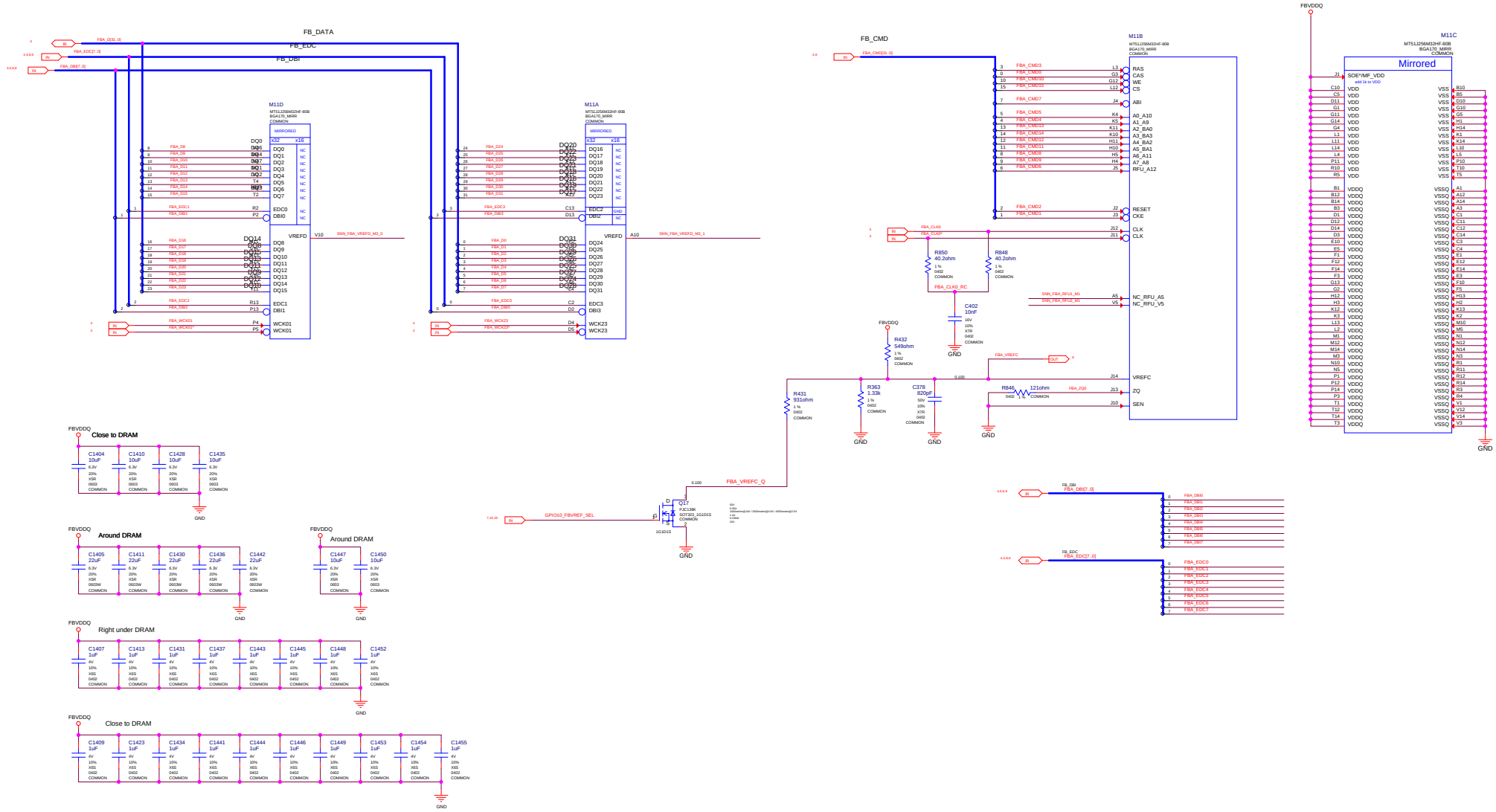
Page5: MEMORY: FBA Partition 31..0



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBA[31:0]

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2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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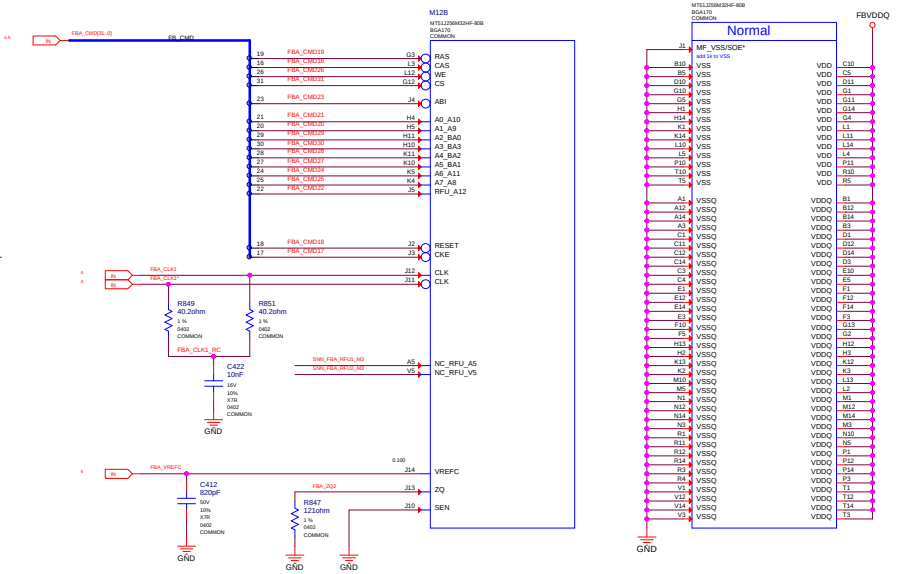
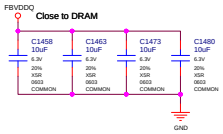
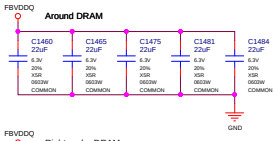
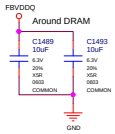
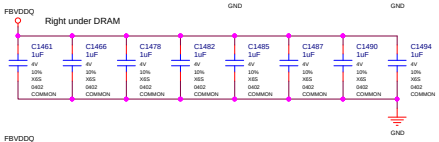
Page6: MEMORY: FBA Partition 63..32

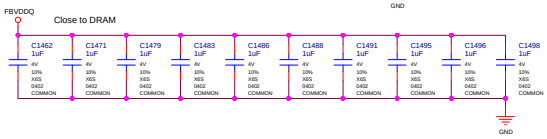


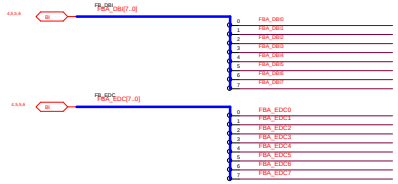












ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBA[63:32]

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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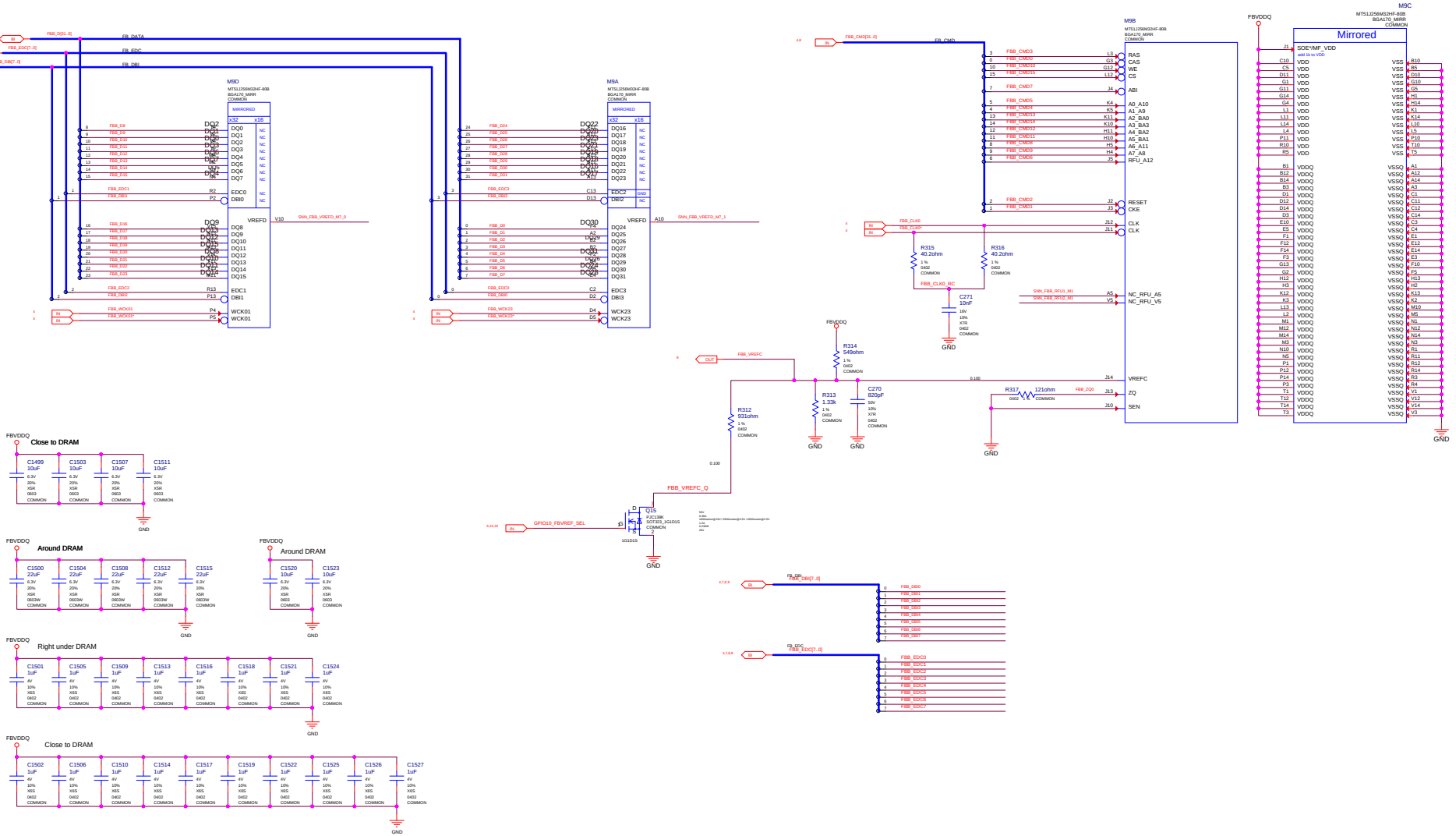
Page7: MEMORY: FBB Partition 31..0



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB[31:0]

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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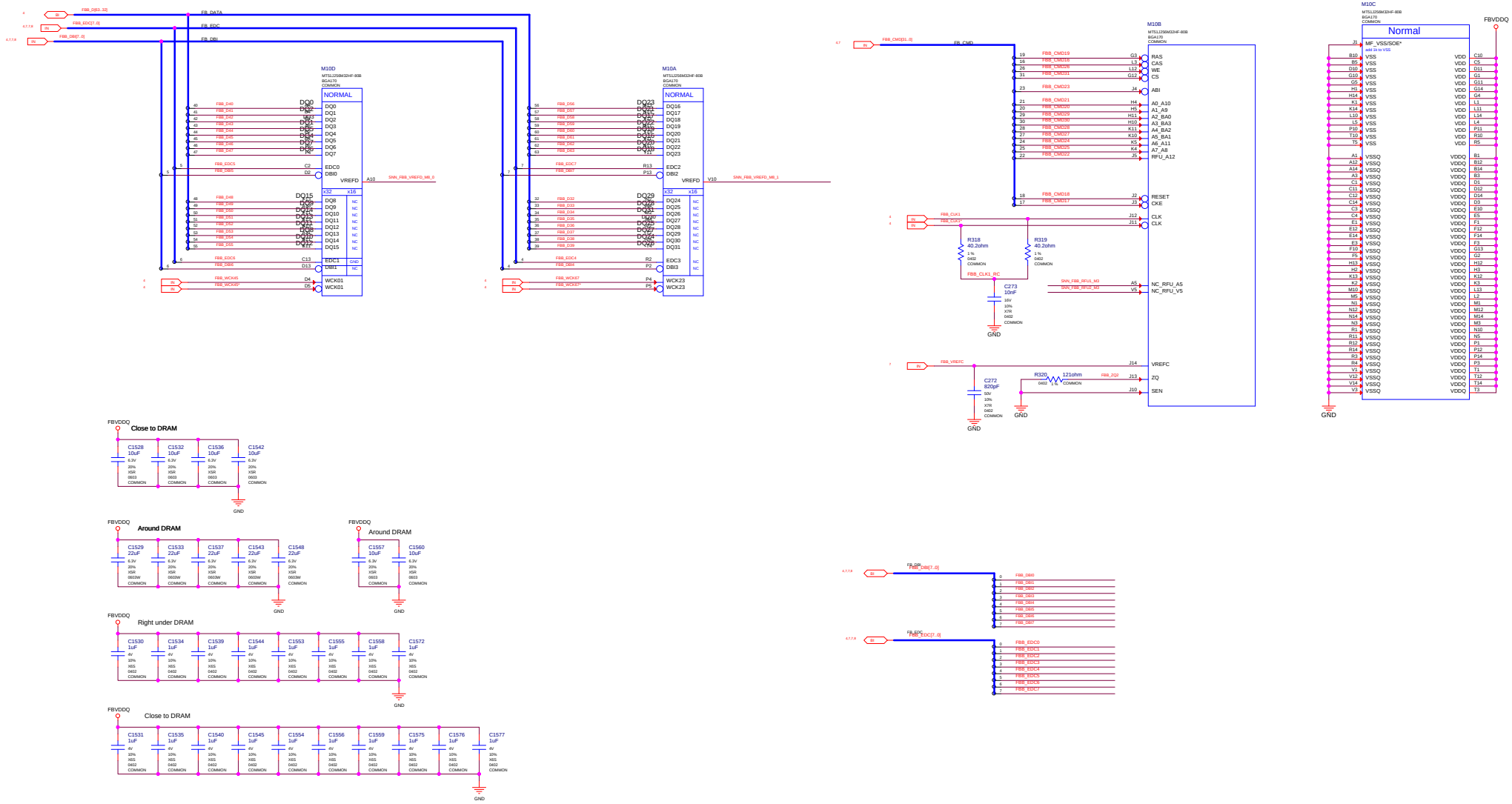
Page8: MEMORY: FBB Partition 63..32



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB[63:32]

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Page9: MEMORY: GPU Partition C/D

A17=CMD32, D17=CMD33 IN TU104
A17=CMD33, D17=CMD32 IN GP104

G1D
TU104-400-A1
BGA2220
COMMON

4/22 FBC

FBC_D0	C6	FBC_CMD0	C11
FBC_D1	D6	FBC_CMD1	B11
FBC_D2	A6	FBC_CMD2	A11
FBC_D3	B6	FBC_CMD3	D11
FBC_D4	B4	FBC_CMD4	A12
FBC_D5	A4	FBC_CMD5	B12
FBC_D6	B3	FBC_CMD6	C12
FBC_D7	C4	FBC_CMD7	C14
FBC_D8	D9	FBC_CMD8	B14
FBC_D9	C9	FBC_CMD9	A14
FBC_D10	E9	FBC_CMD10	D14
FBC_D11	B9	FBC_CMD11	A15
FBC_D12	B8	FBC_CMD12	B15
FBC_D13	A8	FBC_CMD13	C15
FBC_D14	F6	FBC_CMD14	C17
FBC_D15	E6	FBC_CMD15	B17
FBC_D16	F18	FBC_CMD16	B24
FBC_D17	G18	FBC_CMD17	A24
FBC_D18	E18	FBC_CMD18	D23
FBC_D19	H18	FBC_CMD19	A23
FBC_D20	D15	FBC_CMD20	B23
FBC_D21	E15	FBC_CMD21	C23
FBC_D22	G17	FBC_CMD22	C21
FBC_D23	H17	FBC_CMD23	B21
FBC_D24	J15	FBC_CMD24	A21
FBC_D25	H15	FBC_CMD25	D20
FBC_D26	E14	FBC_CMD26	A20
FBC_D27	F14	FBC_CMD27	B20
FBC_D28	H11	FBC_CMD28	C20
FBC_D29	G11	FBC_CMD29	C18
FBC_D30	F11	FBC_CMD30	B18
FBC_D31	E11	FBC_CMD31	A18
FBC_D32	J29	FBC_CMD32	A17
FBC_D33	F30	SNN_FBC_CMD33	D17
FBC_D34	H29	SNN_FBC_DEBUG0	A9
FBC_D35	G30	SNN_FBC_DEBUG1	C24
FBC_D36	B30		
FBC_D37	A30		
FBC_D38	H30		
FBC_D39	C30		
FBC_D40	D27		
FBC_D41	J26		
FBC_D42	F27		
FBC_D43	G27		
FBC_D44	C27		
FBC_D45	B27		
FBC_D46	A27		
FBC_D47	G29		
FBC_D48	H20		
FBC_D49	D18		
FBC_D50	G20		
FBC_D51	E20		
FBC_D52	F23		
FBC_D53	E21		
FBC_D54	D21		
FBC_D55	E23		
FBC_D56	G24		
FBC_D57	H26		
FBC_D58	F24		
FBC_D59	G26		
FBC_D60	F26		
FBC_D61	D26		
FBC_D62	B26		
FBC_D63	C26		

FB_DATA
FBC_D[63..0]

FB_CMD
FBC_CMD[31..0]

FBC_DBG_RFU1 J14 SNN_FBC_DBG_RFU1
FBC_DBG_RFU2 J23 SNN_FBC_DBG_RFU2

FBC_CLK0	G15	FBC_CLK0	FBC_CLK0	FB_CLK
FBC_CLK0	F15	FBC_CLK0*	FBC_CLK0	FB_CLK
FBC_CLK1	H21	FBC_CLK1	FBC_CLK1	FB_CLK
FBC_CLK1	J21	FBC_CLK1*	FBC_CLK1	FB_CLK

FBC_WCK01	F8	FBC_WCK01	FBC_WCK01	FB_WCK
FBC_WCK01	G8	FBC_WCK01*	FBC_WCK01	FB_WCK
FBC_WCKB01	G9	SNN_FBC_WCKB01		
FBC_WCKB01	F9	SNN_FBC_WCKB01*		
FBC_WCK23	H12	FBC_WCK23	FBC_WCK23	FB_WCK
FBC_WCK23	G12	FBC_WCK23*	FBC_WCK23	FB_WCK
FBC_WCKB23	G14	SNN_FBC_WCKB23		
FBC_WCKB23	H14	SNN_FBC_WCKB23*		
FBC_WCK45	J27	FBC_WCK45	FBC_WCK45	FB_WCK
FBC_WCK45	H27	FBC_WCK45*	FBC_WCK45	FB_WCK
FBC_WCKB45	E29	SNN_FBC_WCKB45		
FBC_WCKB45	F29	SNN_FBC_WCKB45*		
FBC_WCK67	G23	FBC_WCK67	FBC_WCK67	FB_WCK
FBC_WCK67	H23	FBC_WCK67*	FBC_WCK67	FB_WCK
FBC_WCKB67	H24	SNN_FBC_WCKB67		
FBC_WCKB67	J24	SNN_FBC_WCKB67*		

FB_DBI
FBC_DBI[7..0]

FBC_DBI0	A5	FBC_DQM0	
FBC_DBI1	C8	FBC_DQM1	
FBC_DBI2	J18	FBC_DQM2	
FBC_DBI3	F12	FBC_DQM3	
FBC_DBI4	D29	FBC_DQM4	
FBC_DBI5	E27	FBC_DQM5	
FBC_DBI6	F20	FBC_DQM6	
FBC_DBI7	E24	FBC_DQM7	

FB_EDC
FBC_EDC[7..0]

FBC_EDC0	D5	FBC_DQS_WP0	
FBC_EDC1	D8	FBC_DQS_WP1	
FBC_EDC2	E17	FBC_DQS_WP2	
FBC_EDC3	E12	FBC_DQS_WP3	
FBC_EDC4	E30	FBC_DQS_WP4	
FBC_EDC5	B29	FBC_DQS_WP5	
FBC_EDC6	G21	FBC_DQS_WP6	
FBC_EDC7	E24	FBC_DQS_WP7	

FBC_PLL_AVDD L17 1V8_FB_PLL

C1000
1uF
4V
20%
X5R
0201
COMMON

Y24	GND
Y25	GND
Y26	GND
Y27	GND
Y28	GND
Y29	GND
Y30	GND
Y31	GND

GDDR5 CMD Mapping

CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

FBVDDQ
R514 10k 5 % 0402 COMMON
R503 10k 5 % 0402 COMMON
FBC_CMD01
FBC_CMD17
FBC_CMD02
FBC_CMD18
R311 10k 5 % 0402 COMMON
R306 10k 5 % 0402 COMMON
GND

Use NC pin to Improve NVVDD,FBVDDQ,1V8 PDN
FOR TU116 Only

V4=CMD32, U1=CMD33 IN TU104
V4=CMD33, U1=CMD32 IN GP104

G1E
TU104-400-A1
BGA2220
COMMON

5/22 FBD

FBD_D0	AK8	FBD_CMD0	AD2
FBD_D1	AK4	FBD_CMD1	AD1
FBD_D2	AK2	FBD_CMD2	AD4
FBD_D3	AK3	FBD_CMD3	AC1
FBD_D4	AK5	FBD_CMD4	AC2
FBD_D5	AK8	FBD_CMD5	AC3
FBD_D6	AK9	FBD_CMD6	AA3
FBD_D7	AK7	FBD_CMD7	AA2
FBD_D8	AG4	FBD_CMD8	AA1
FBD_D9	AF9	FBD_CMD9	AA4
FBD_D10	AG6	FBD_CMD10	Y1
FBD_D11	AG7	FBD_CMD11	Y2
FBD_D12	AJ4	FBD_CMD12	Y3
FBD_D13	AJ5	FBD_CMD13	V3
FBD_D14	AJ6	FBD_CMD14	V2
FBD_D15	AG5	FBD_CMD15	V1
FBD_D16	Y6	FBD_CMD16	L3
FBD_D17	Y5	FBD_CMD17	L2
FBD_D18	V5	FBD_CMD18	L1
FBD_D19	Y4	FBD_CMD19	M4
FBD_D20	AA6	FBD_CMD20	M1
FBD_D21	AA5	FBD_CMD21	M2
FBD_D22	AC5	FBD_CMD22	M3
FBD_D23	AC4	FBD_CMD23	P3
FBD_D24	AD7	FBD_CMD24	P2
FBD_D25	AC6	FBD_CMD25	P1
FBD_D26	AF6	FBD_CMD26	R4
FBD_D27	AD6	FBD_CMD27	R1
FBD_D28	AF7	FBD_CMD28	R2
FBD_D29	AF8	FBD_CMD29	R3
FBD_D30	AF2	FBD_CMD30	U3
FBD_D31	AF3	FBD_CMD31	U2
FBD_D32	F4	FBD_CMD32	V4
FBD_D33	E1	FBD_CMD33	U1
FBD_D34	F3	WE*	AD3
FBD_D35	F5	FBD_CMD35	J3
FBD_D36	D2		
FBD_D37	D1		
FBD_D38	C3		
FBD_D39	C2		
FBD_D40	J5		
FBD_D41	J4		
FBD_D42	L8		
FBD_D43	J2		
FBD_D44	F1		
FBD_D45	F2		
FBD_D46	H4		
FBD_D47	H5		
FBD_D48	V7		
FBD_D49	V8		
FBD_D50	V6		
FBD_D51	V9		
FBD_D52	U4		
FBD_D53	R5		
FBD_D54	R6		
FBD_D55	U8		
FBD_D56	P6		
FBD_D57	R9		
FBD_D58	P4		
FBD_D59	P5		
FBD_D60	L7		
FBD_D61	L6		
FBD_D62	L4		
FBD_D63	L5		

FBD_DBG_RFU1 AC9
FBD_DBG_RFU2 P9

FBD_CLK0	Y8	FBD_WCK01	AJ8
FBD_CLK0	Y7	FBD_WCK01	AJ7
FBD_CLK1	R8	FBD_WCKB01	AG8
FBD_CLK1	R7	FBD_WCKB01	AG9
		FBD_WCK23	AD8
		FBD_WCK23	AD9
		FBD_WCKB23	AC7
		FBD_WCKB23	AC8
		FBD_WCK45	J6
		FBD_WCK45	J7
		FBD_WCKB45	H7
		FBD_WCKB45	H6
		FBD_WCK67	P8
		FBD_WCK67	P7
		FBD_WCKB67	M7
		FBD_WCKB67	M8

FBD_DQM0	AJ1	FBD_DQS_WP0	A23
FBD_DQM1	AG1	FBD_DQS_WP1	AG2
FBD_DQM2	AA7	FBD_DQS_WP2	AA9
FBD_DQM3	AD5	FBD_DQS_WP3	AF4
FBD_DQM4	D3	FBD_DQS_WP4	E3
FBD_DQM5	H3	FBD_DQS_WP5	H2
FBD_DQM6	U5	FBD_DQS_WP6	U6
FBD_DQM7	M9	FBD_DQS_WP7	M5

FBD_PLL_AVDD V11

Y32	GND
Y33	GND
Y34	GND
Y35	GND
Y36	GND
Y37	GND
Y38	GND
Y39	GND

NVVDD
FBVDDQ
GND

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: GPU FB_CD

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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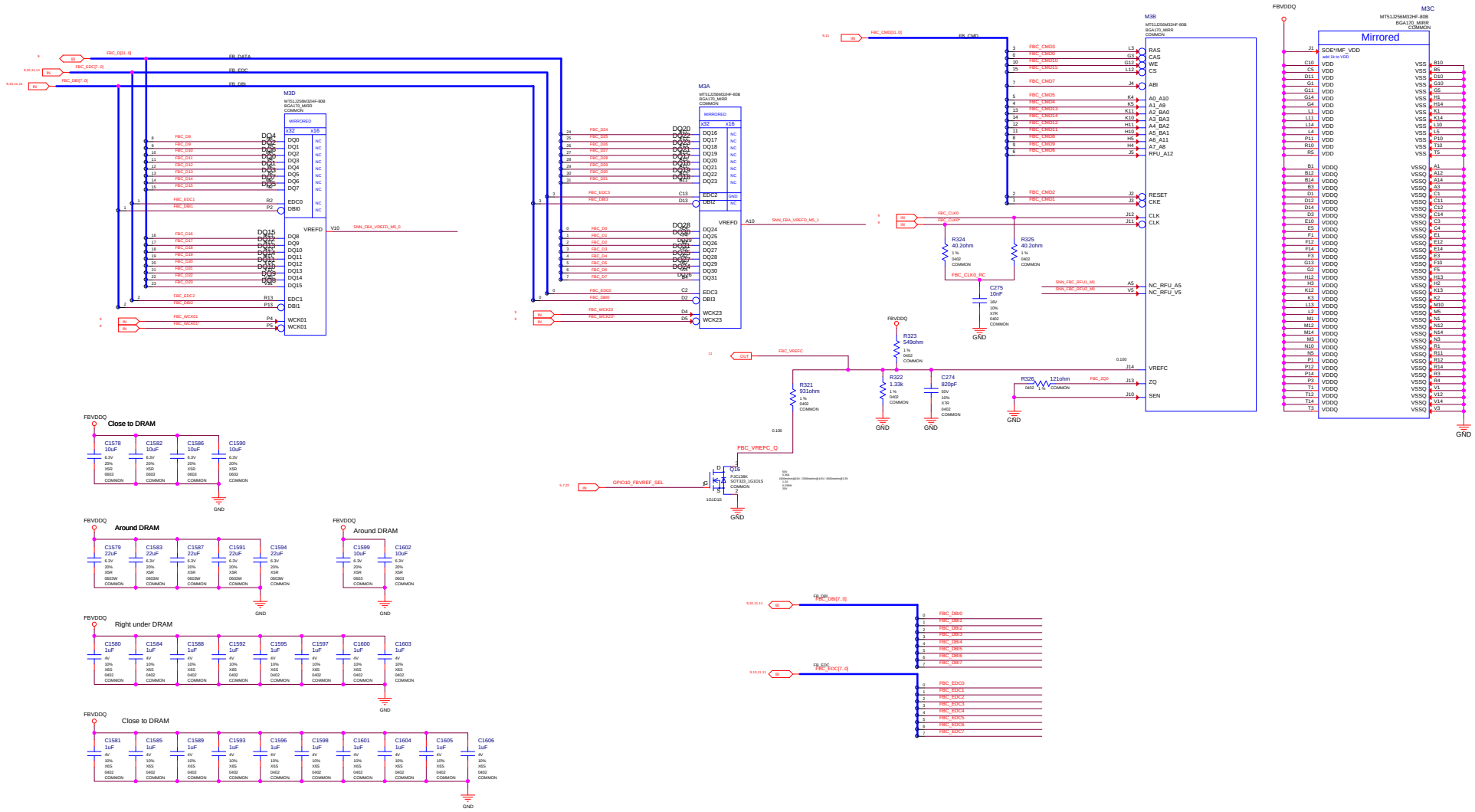
Page10: MEMORY: FBC Partition 31..0



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBC[31:0]

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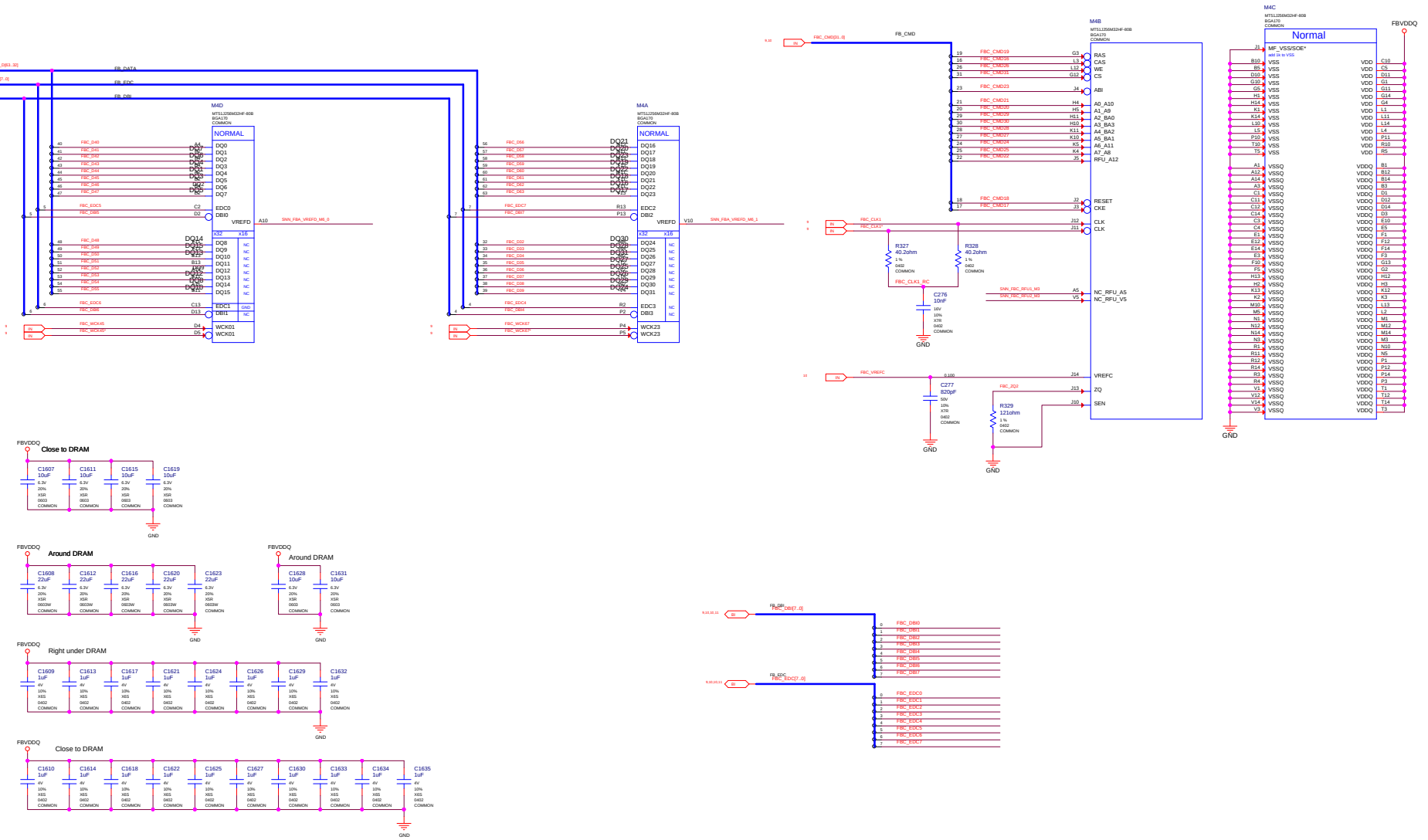
Page11: MEMORY: FBC Partition 63..32



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBC[63:32]

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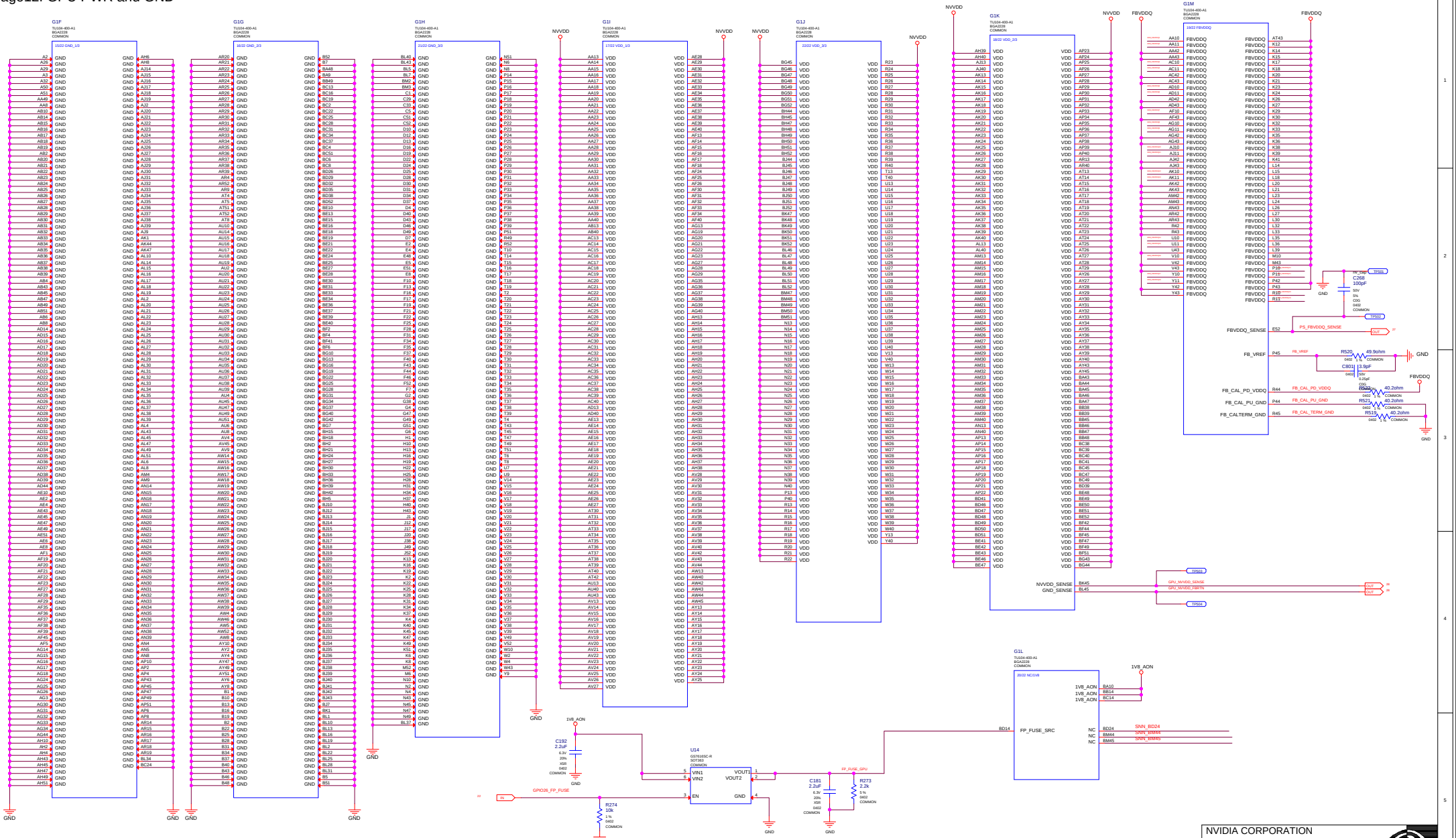
Page12: GPU PWR and GND



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G165-BASE-200		
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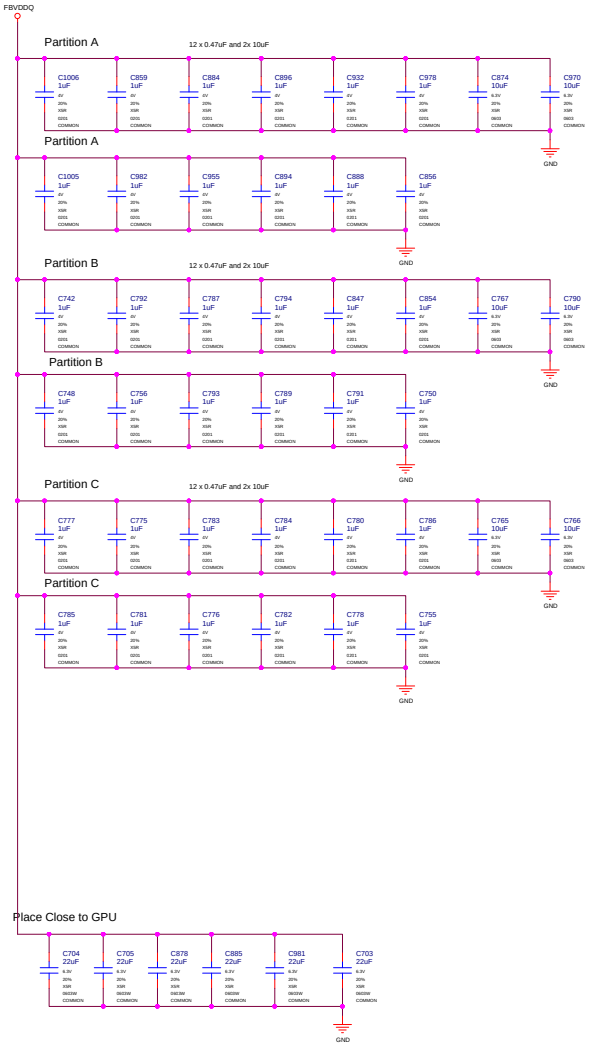
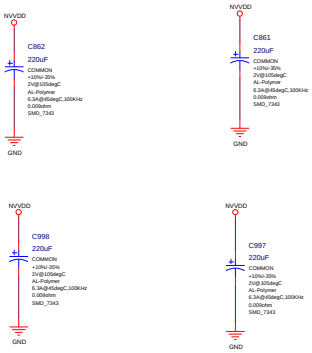
BOM REV	A	DATE	20-DEC-2018

Page13: GPU DECOUPLING 1

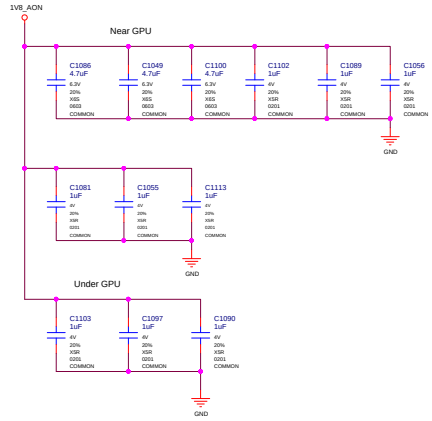
FBVDDQ



NVVDD



1V8_AON



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING 1

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
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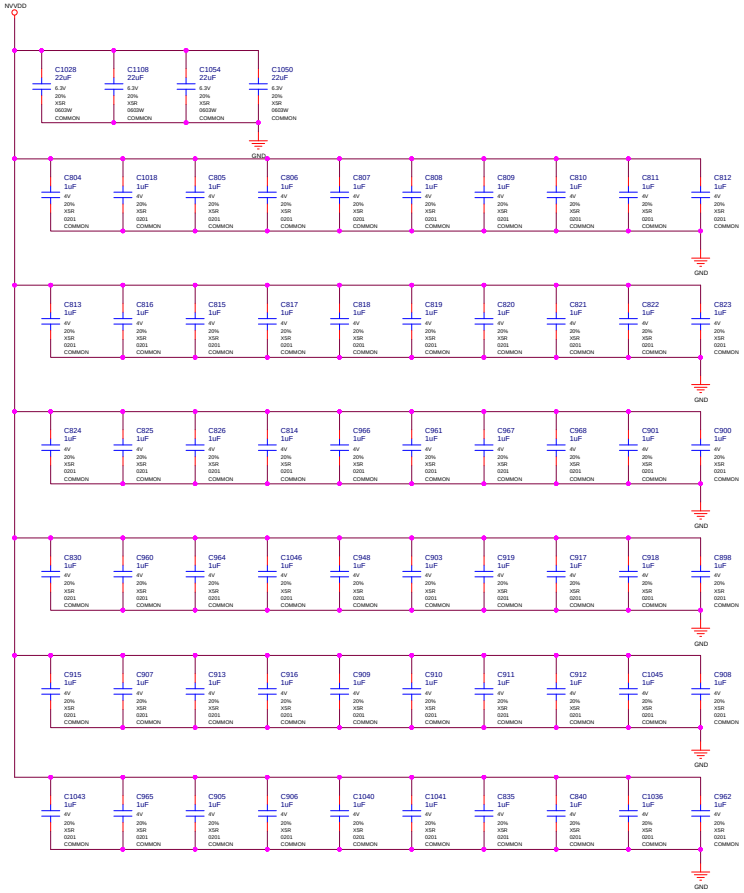
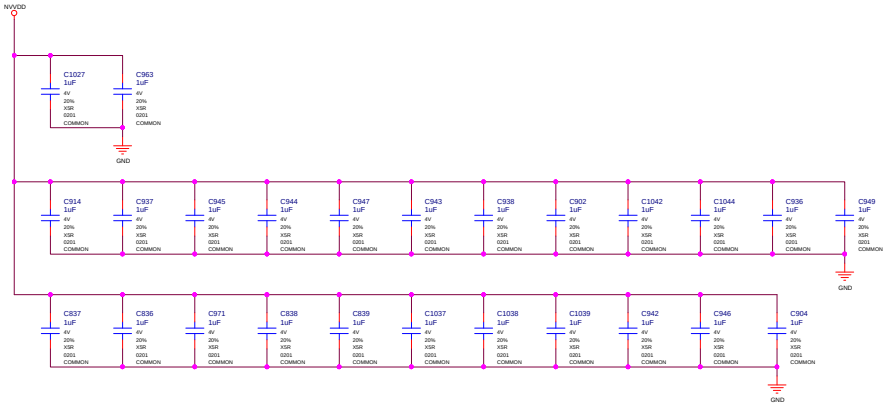
Page14: GPU DECOUPLING 2

NVVDD





ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING 2

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
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NV_PN	600-1G165-BASE-200		
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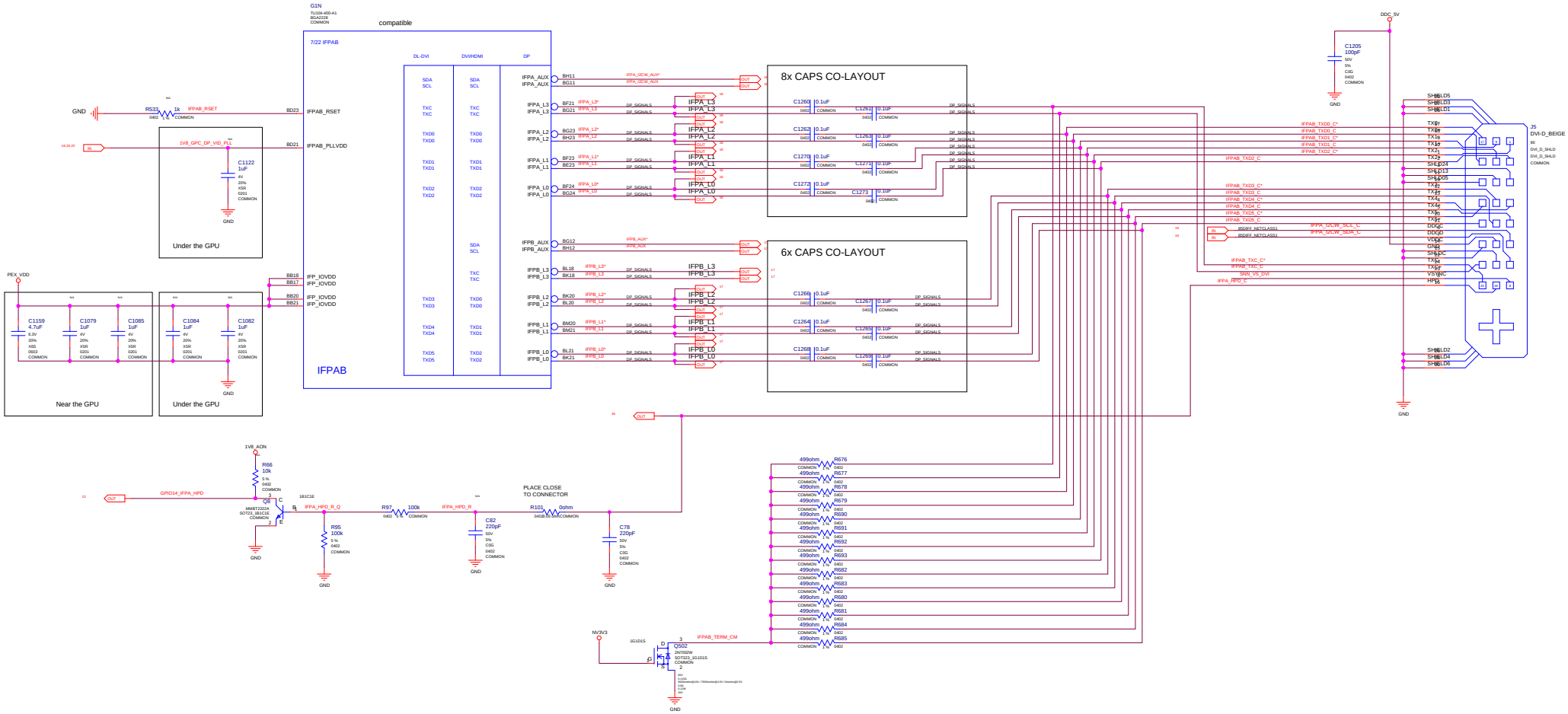
Page15: IFPAB DVI-D-DL



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPAB DVI-D-DL

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
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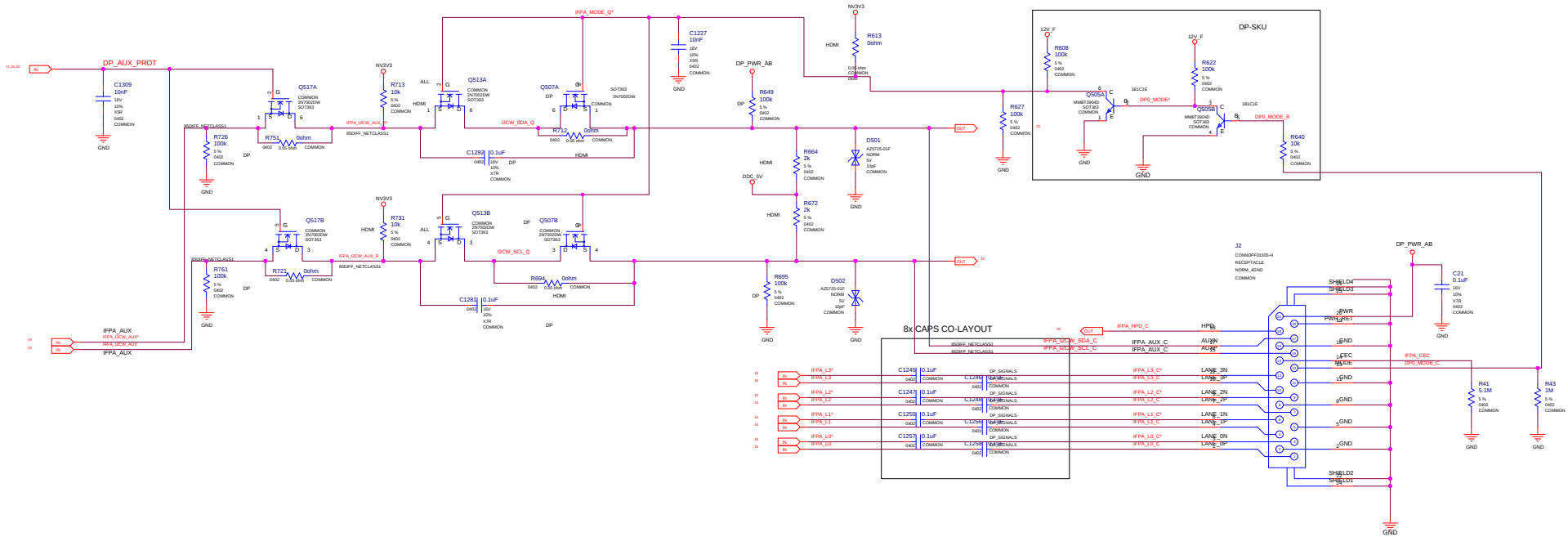
Page16: IFPA DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPA DP

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
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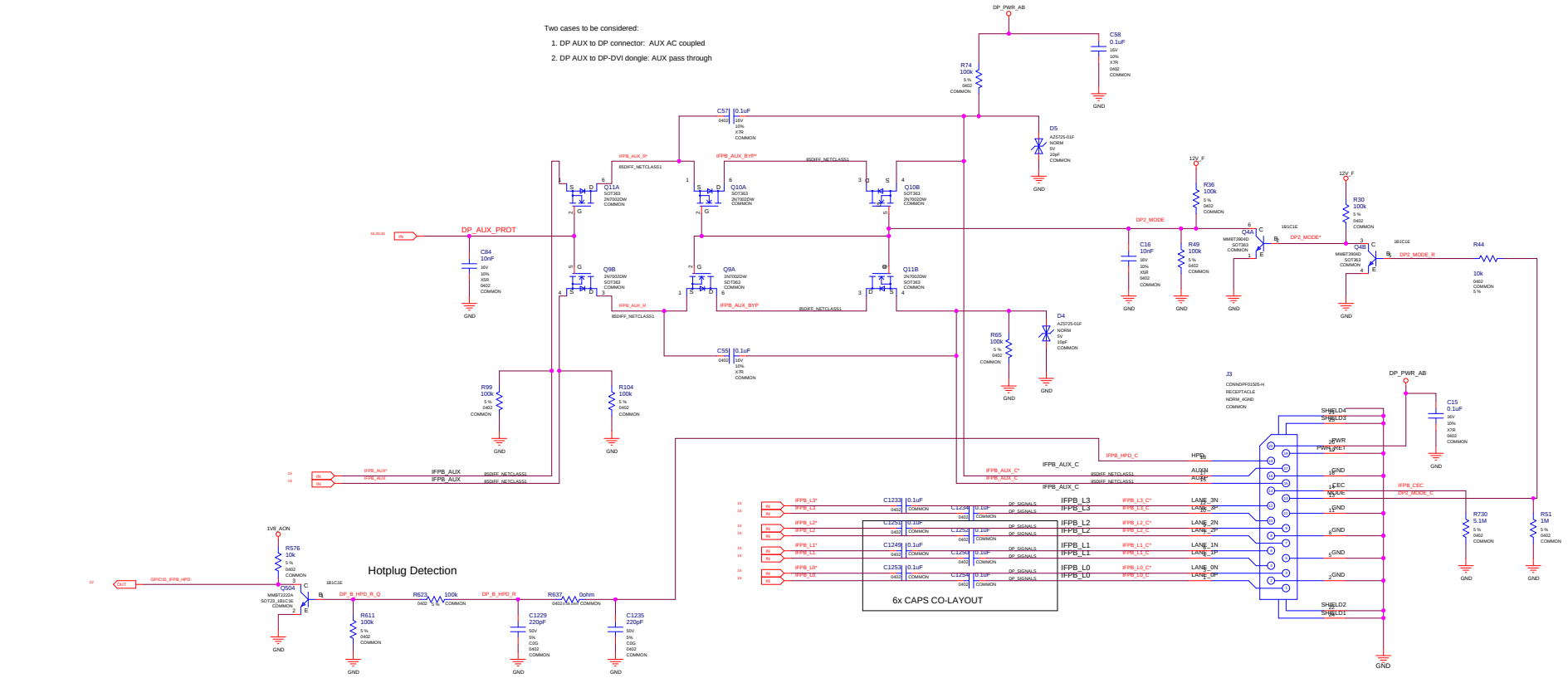
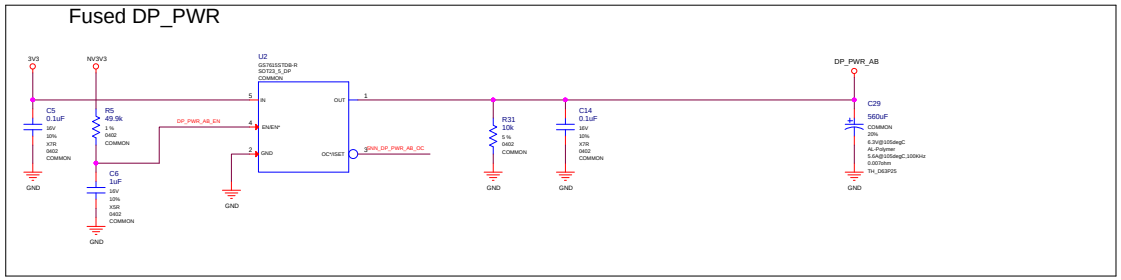
Page17: IFPB DP





ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPB DP

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
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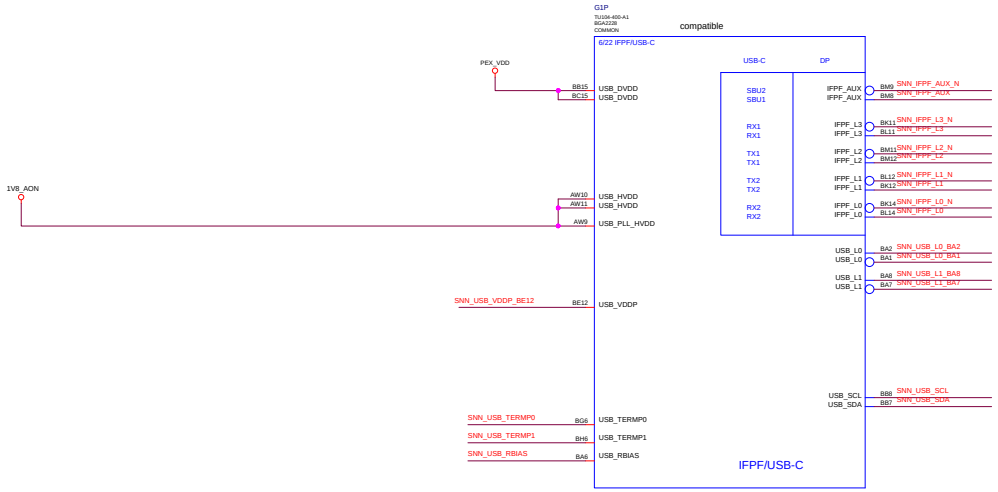
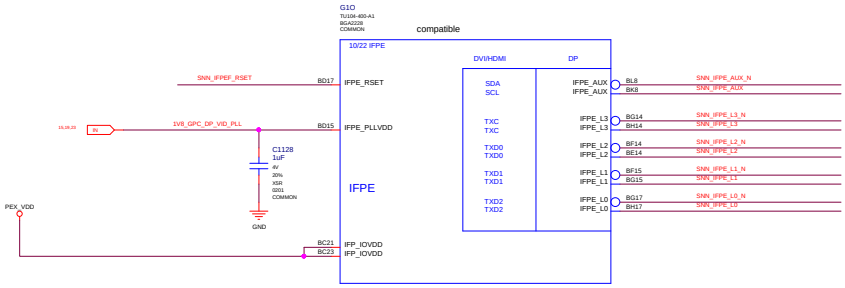
Page18: IFPE & IFPF NC





IO: IFPE & IFPF NC

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
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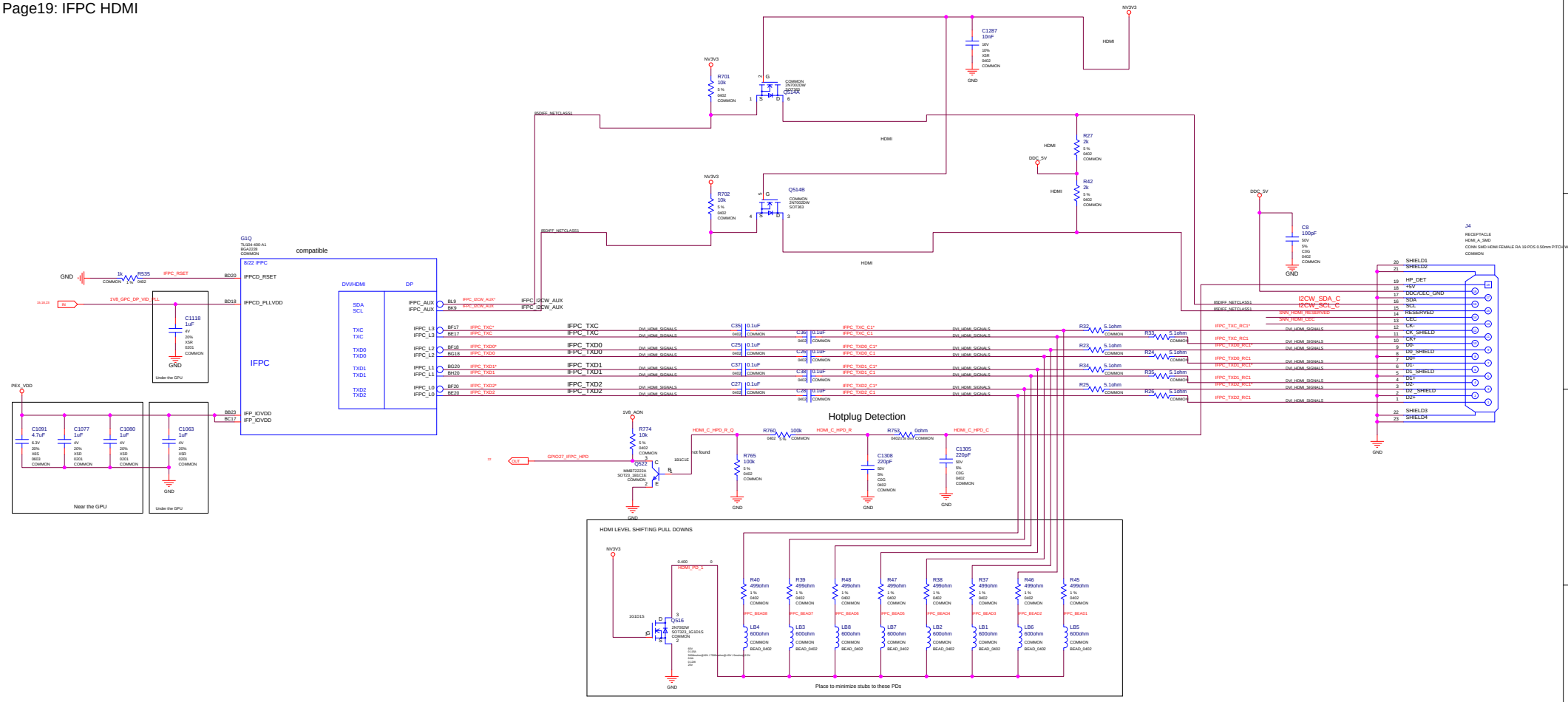
BOM REV	A	DATE	20-DEC-2018

Page19: IFPC HDMI



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPC HDMI

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
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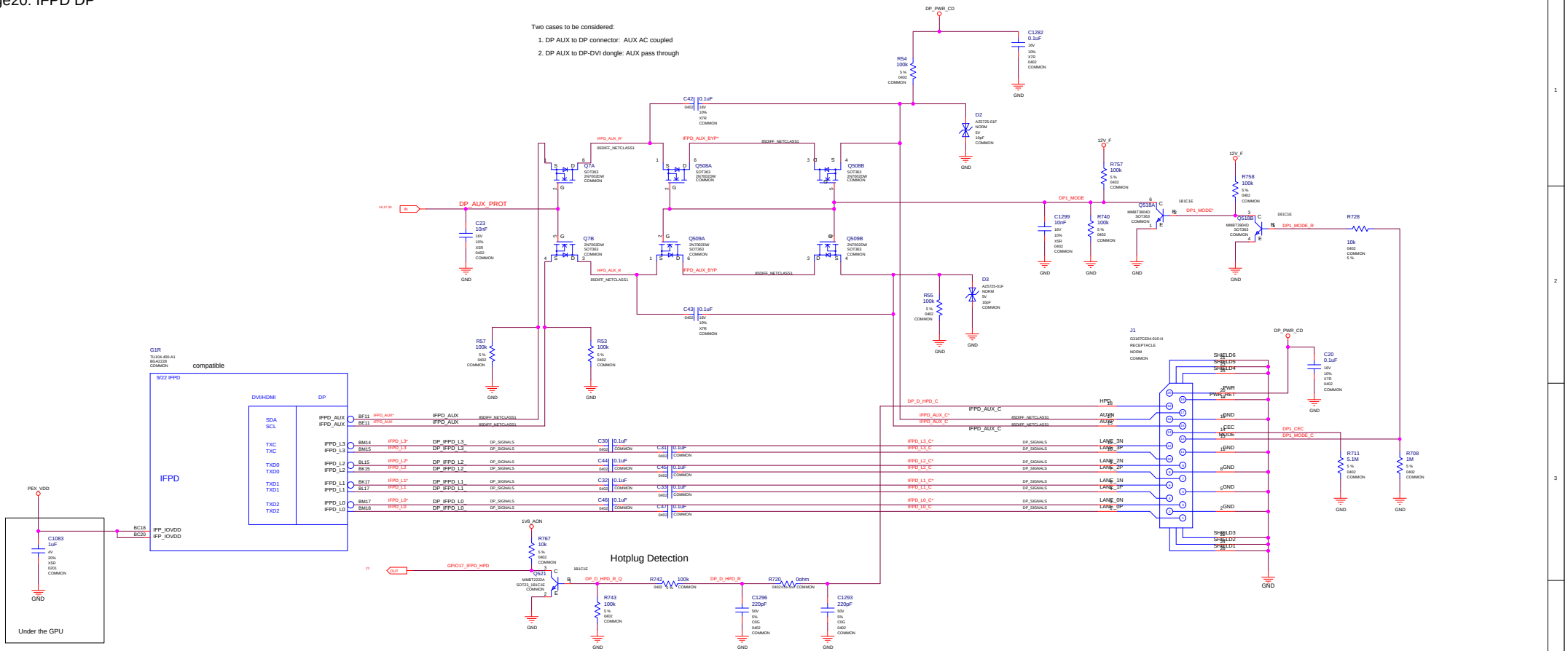
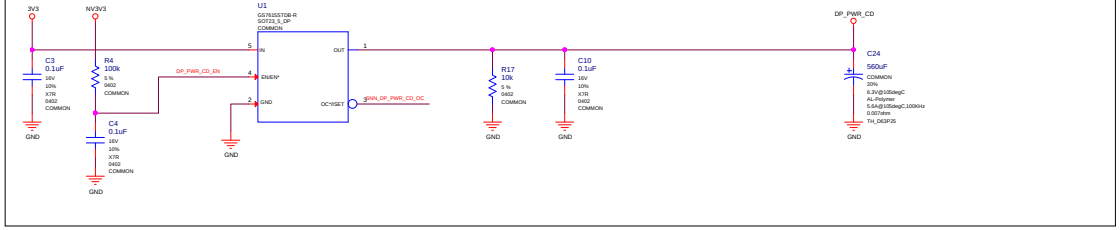
Page20: IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPD DP

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
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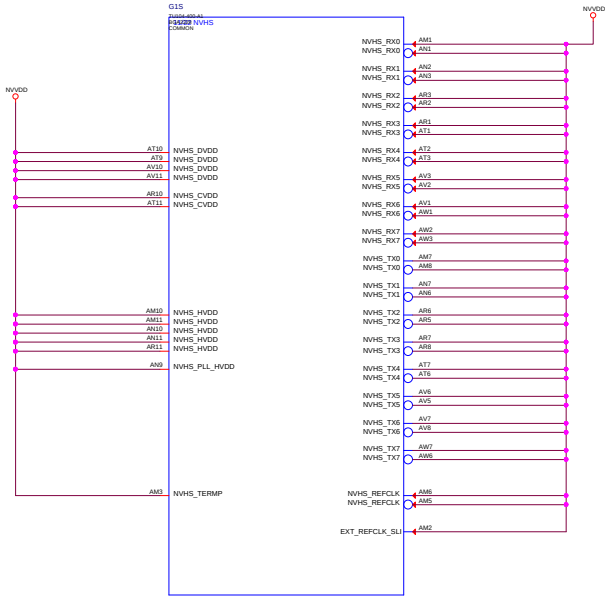
Use NC pin to Improve NVVDD,FBVDDQ,1V8 PDN

For TU116 Only



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: NVHS INTERFACE AND FRAME LOCK

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
PCB REV	PG165-B01	PAGE	21 OF 38
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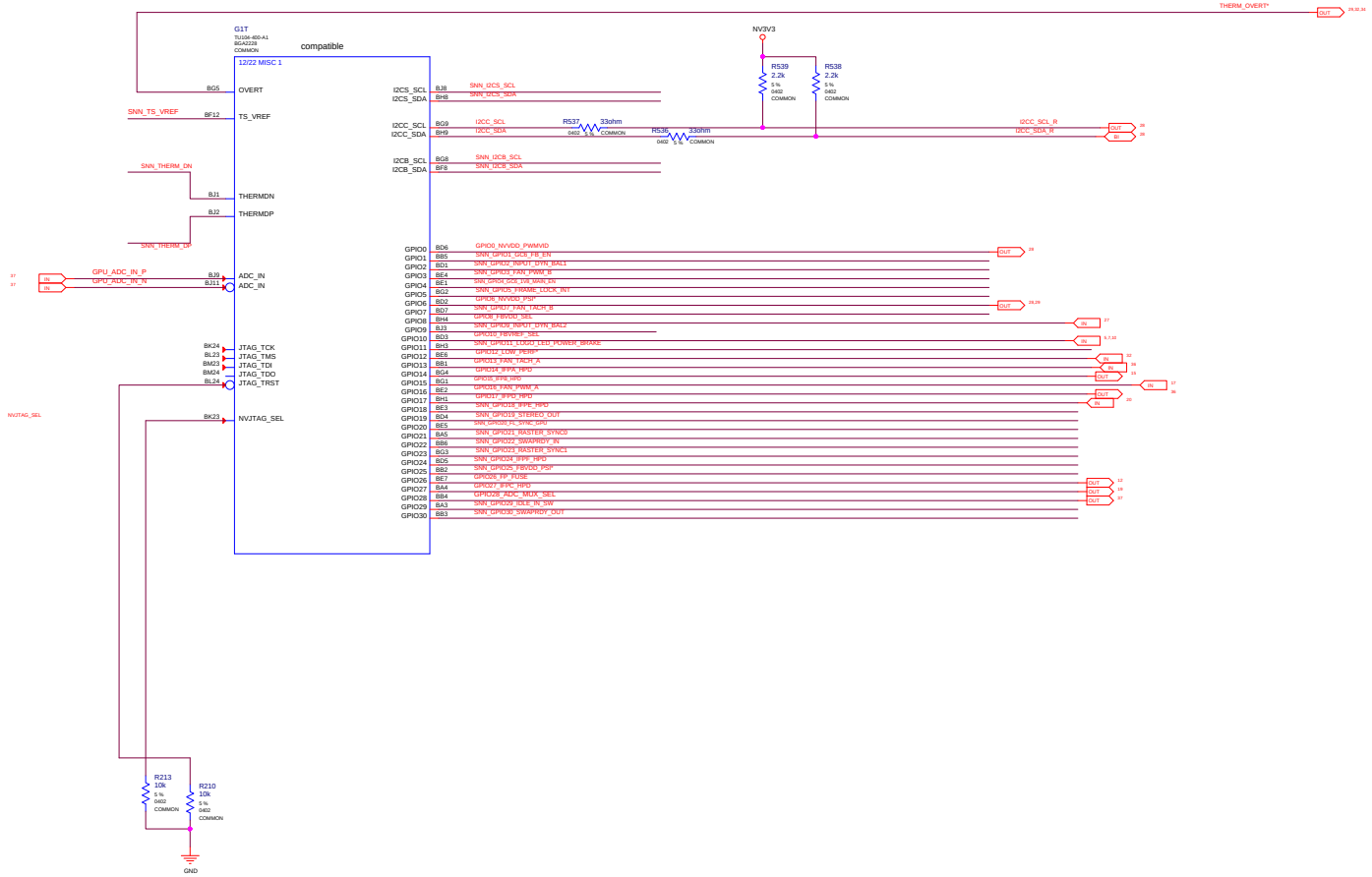
Page22: MISC1: JTAG, GPIO, ADC, I2C, OVERT



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: JTAG,GPIO,ADC,I2C,OVERT

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NV_PN	600-1G165-BASE-200		
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Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung 8Gb 256Mx32 K4G80325FC-HC25
L	L	H	0001	Micron 8Gb 256Mx32 MT51J256M32HF-80:B
L	H	L	0010	Hynix 8Gb 256Mx32 H5GC8H24AJR-R2C
L	H	H	0011	Hynix 8Gb 256Mx32 H5GQ8H24MJR-R4C
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

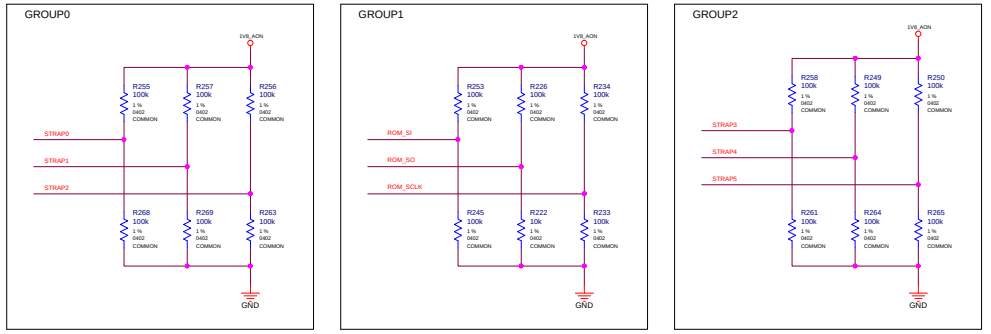
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

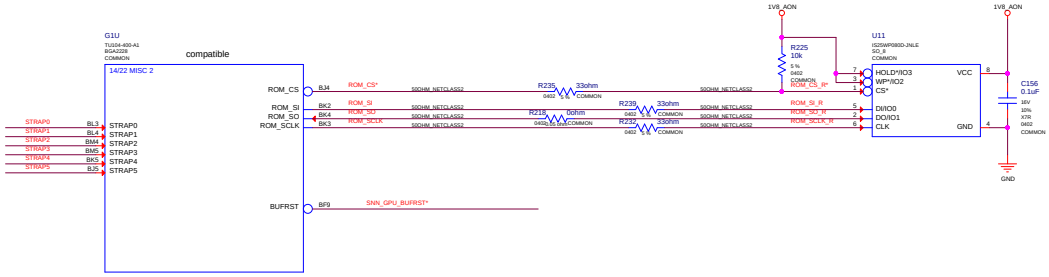
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

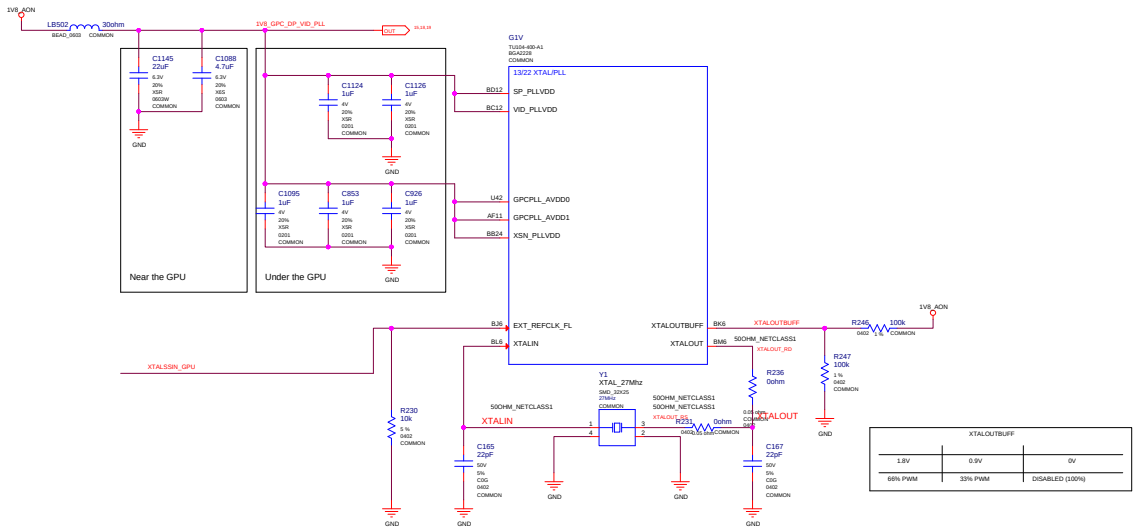
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL,STRAPS

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NV_PN	600-1G165-BASE-200		
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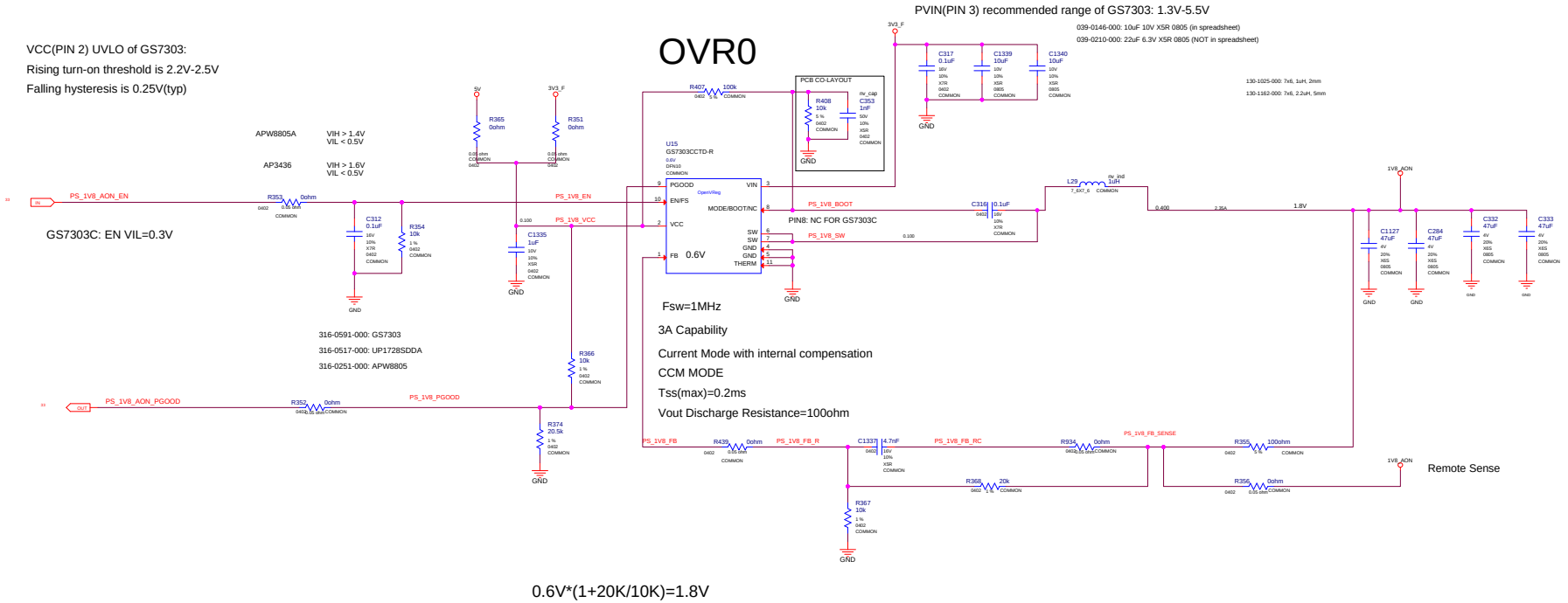
Use 5V as 1V8 OVR0 VCC(PIN 2), can make 1V8_AON power down later(hold more time during power down).
And no glitch on 1V8_PGOOD.

1v8 Switcher



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 1V8_AON

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
PCB REV	PG165-B01	PAGE	24 OF 38
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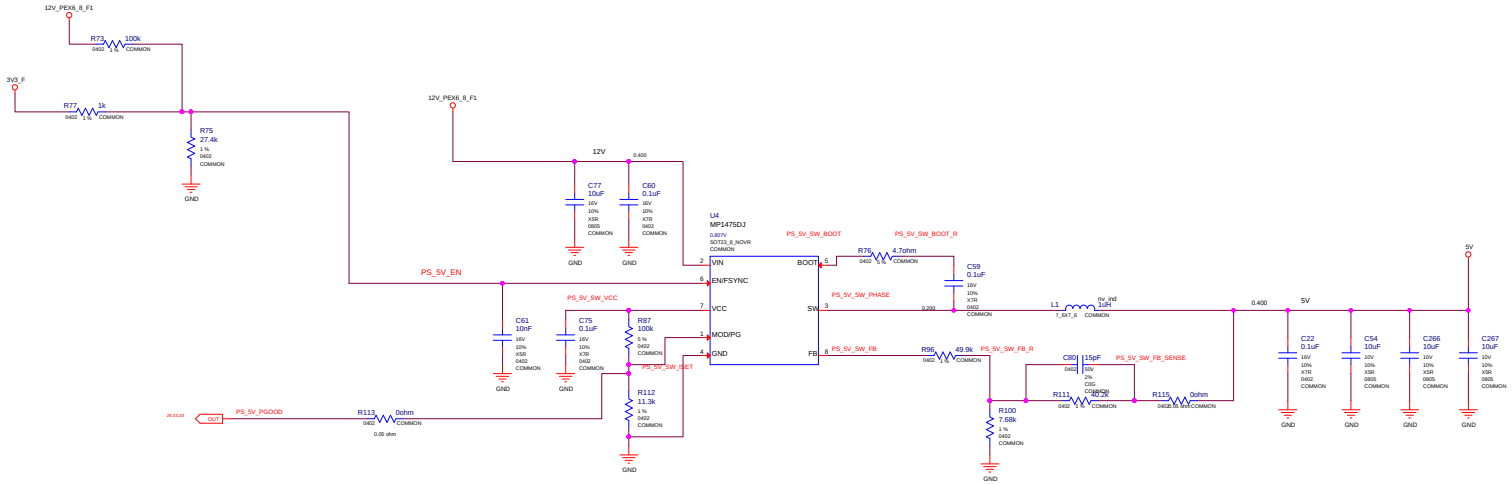
Page25: PS: 5V



0.8V*(1+40.2K/7.68K)=4.9875V

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 5V

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
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DUE

Use 5V as PEX_VDD OVR0 VCC(PIN 2),
enable PEX_VDD OVR0 internal discharge(100ohm typ), making PEX_VDD power down faster.

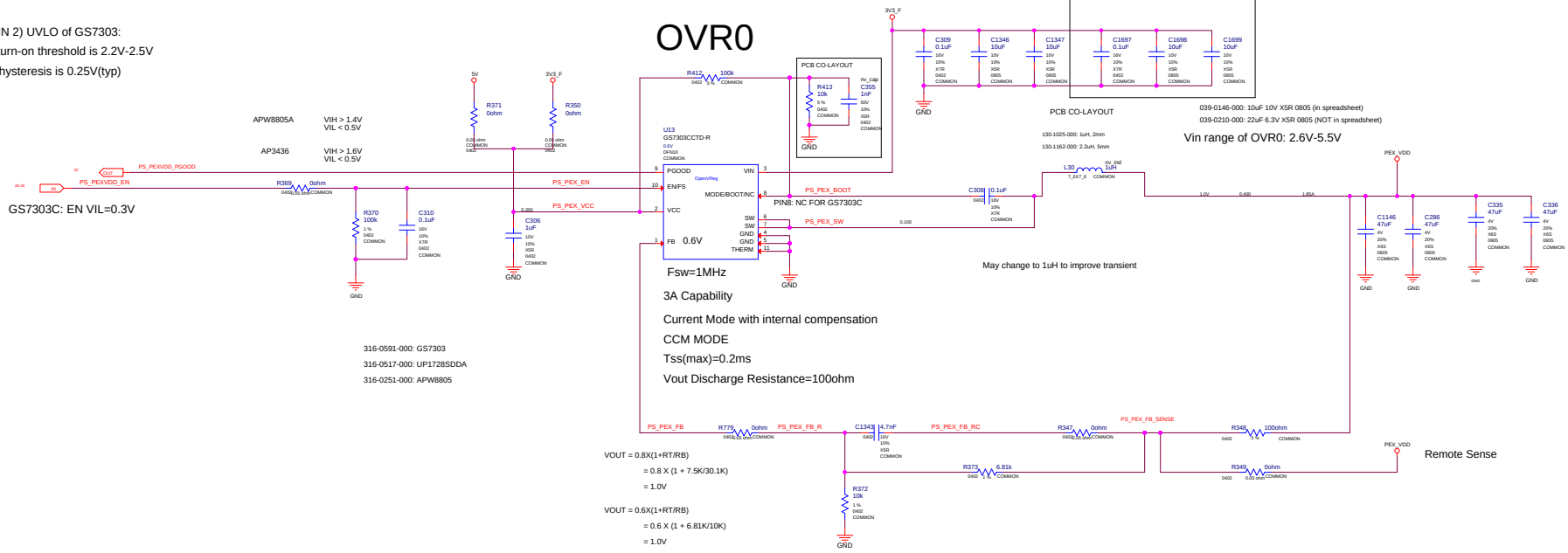
PEX_VDD Switcher

VCC(PIN 2) UVLO of GS7303:
Rising turn-on threshold is 2.2V-2.5V
Falling hysteresis is 0.25V(typ)

APW8805A VIH > 1.4V VIL < 0.5V
AP3436 VIH > 1.6V VIL < 0.5V

GS7303C: EN VIL=0.3V

OVR0



316-0591-000: GS7303
316-0517-000: UP1728SDDA
316-0251-000: APW8805

Fsw=1MHz
3A Capability
Current Mode with internal compensation
CCM MODE
Tss(max)=0.2ms
Vout Discharge Resistance=100ohm

May change to 1uH to improve transient

ADD 3 MORE MLCC
3V3_F is Far Away From Source

PCB CO-LAYOUT

039-0146-000: 10uF 10V X5R 0805 (in spreadsheet)
039-0210-000: 22uF 6.3V X5R 0805 (NOT in spreadsheet)

130-1025-000: 1uH, 2mm
130-1162-000: 2.2uH, 5mm

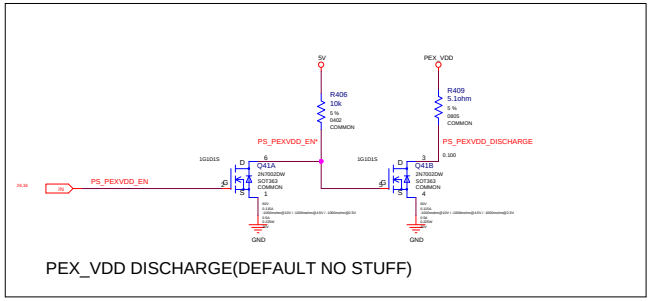
Vin range of OVR0: 2.6V-5.5V

Remote Sense

VOUT = 0.8X(1+RT/RB)
= 0.8 X (1 + 7.5K/30.1K)
= 1.0V

VOUT = 0.6X(1+RT/RB)
= 0.6 X (1 + 6.81K/10K)
= 1.0V

0.6V*(1+6.81K/10K)=1.008V



PEX_VDD DISCHARGE(DEFAULT NO STUFF)

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEXVDD

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NV_PN	600-1G165-BASE-200		
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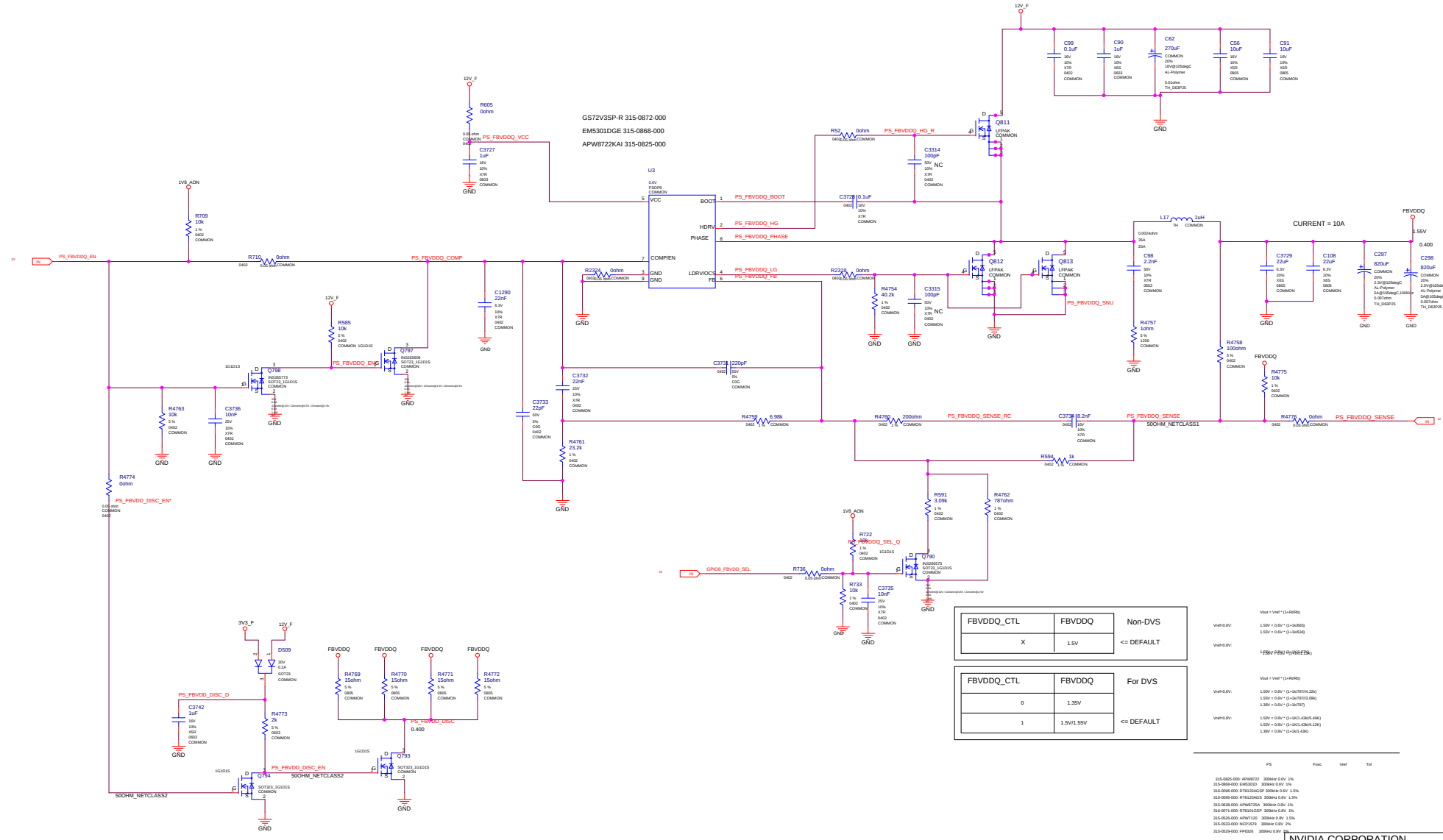
Page27: PS: FBVDDQ changed



FBVDDQ_CTL	FBVDDQ	Non-DVS
X	1.5V	<= DEFAULT

FBVDDQ_CTL	FBVDDQ	For DVS
0	1.35V	
1	1.5V/1.55V	<= DEFAULT

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDDQ

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NV_PN	600-1G165-BASE-200		
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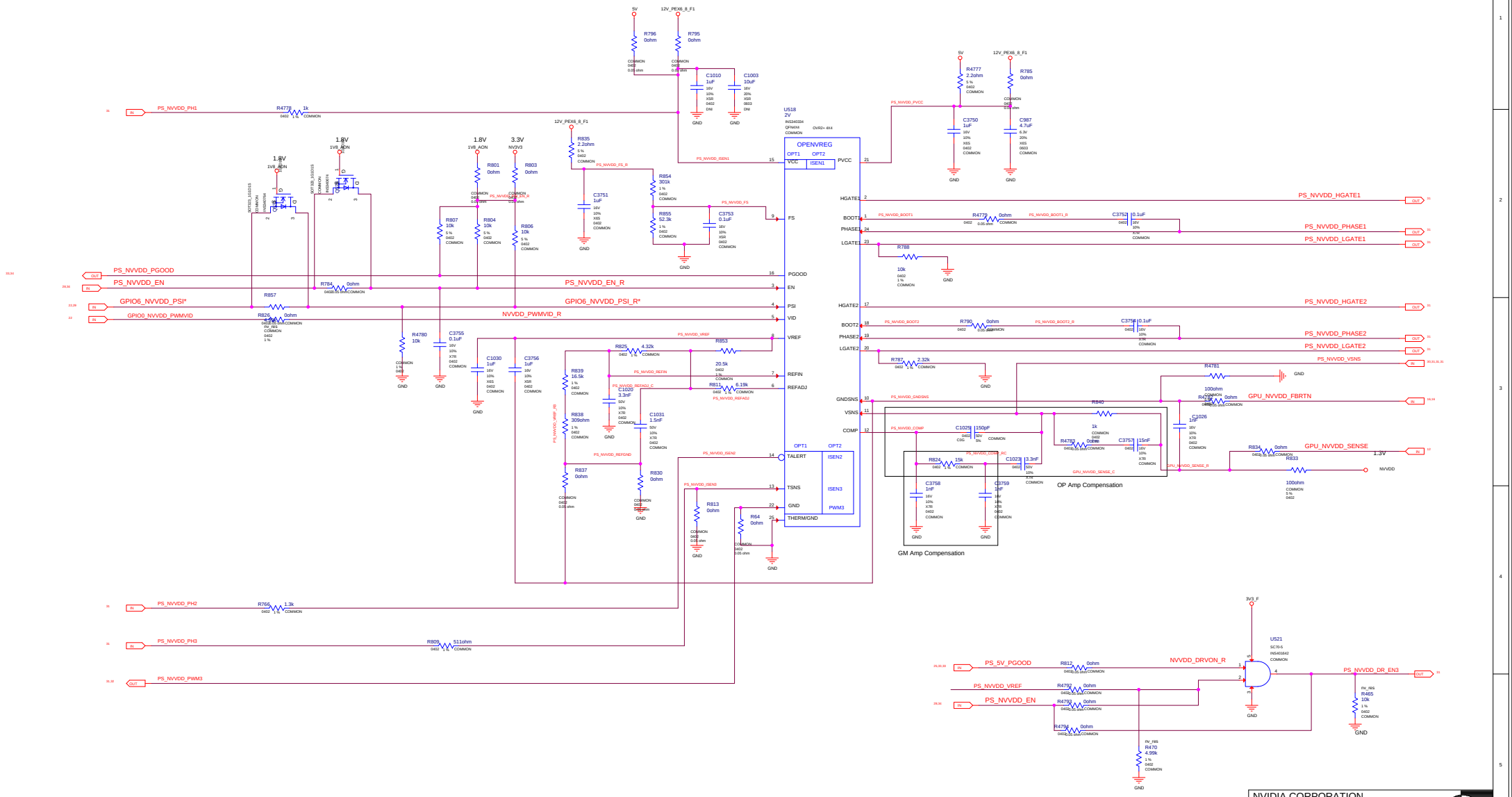
Page28: PS: NVVDD CTR(changed)



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Controller

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
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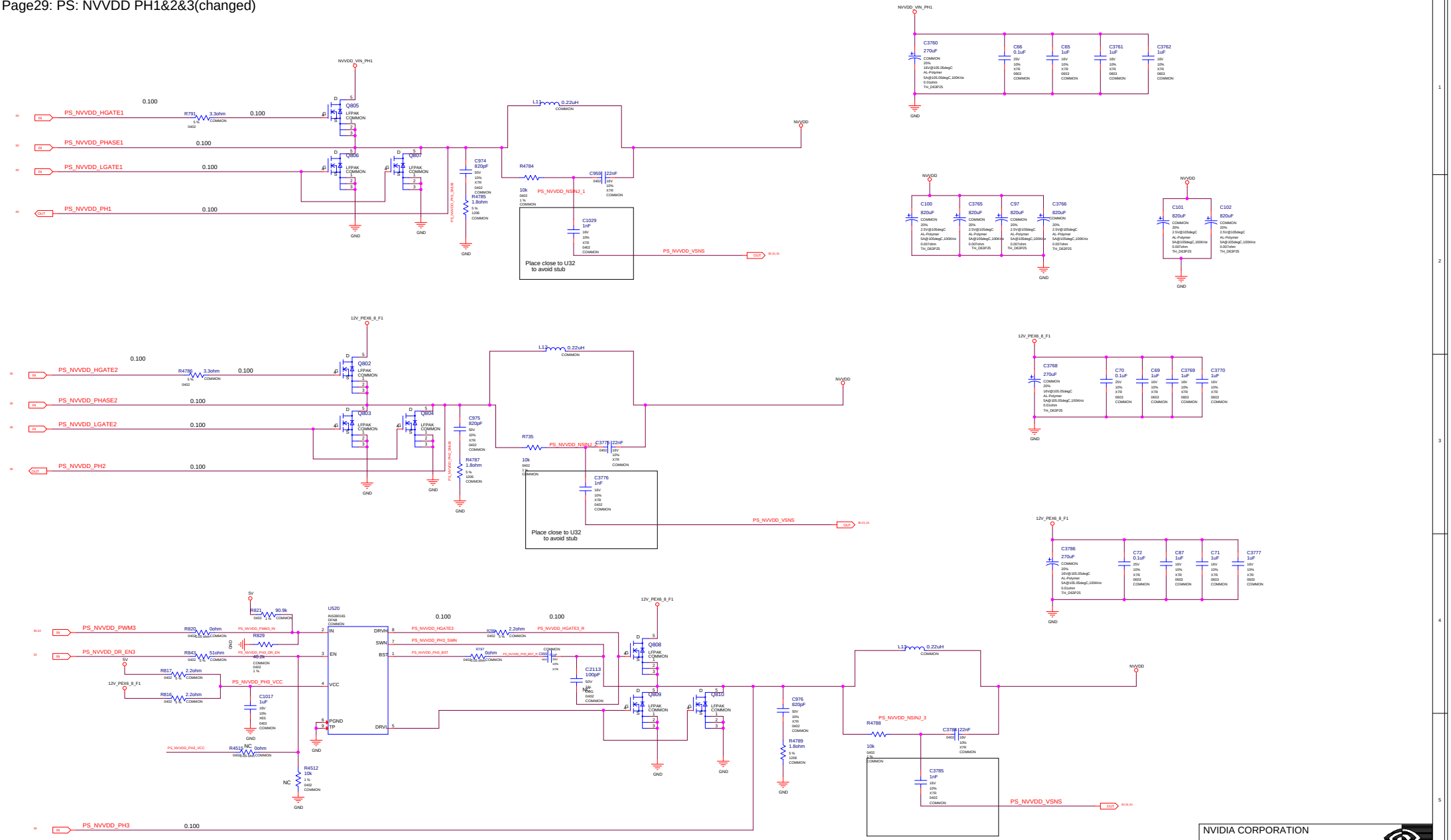
Page29: PS: NVVDD PH1&2&3(changed)



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 1,2

NVIDIA CORPORATION
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NV_PN	600-1G165-BASE-200		
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Page30: PS: NVVDD PH 3

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 3

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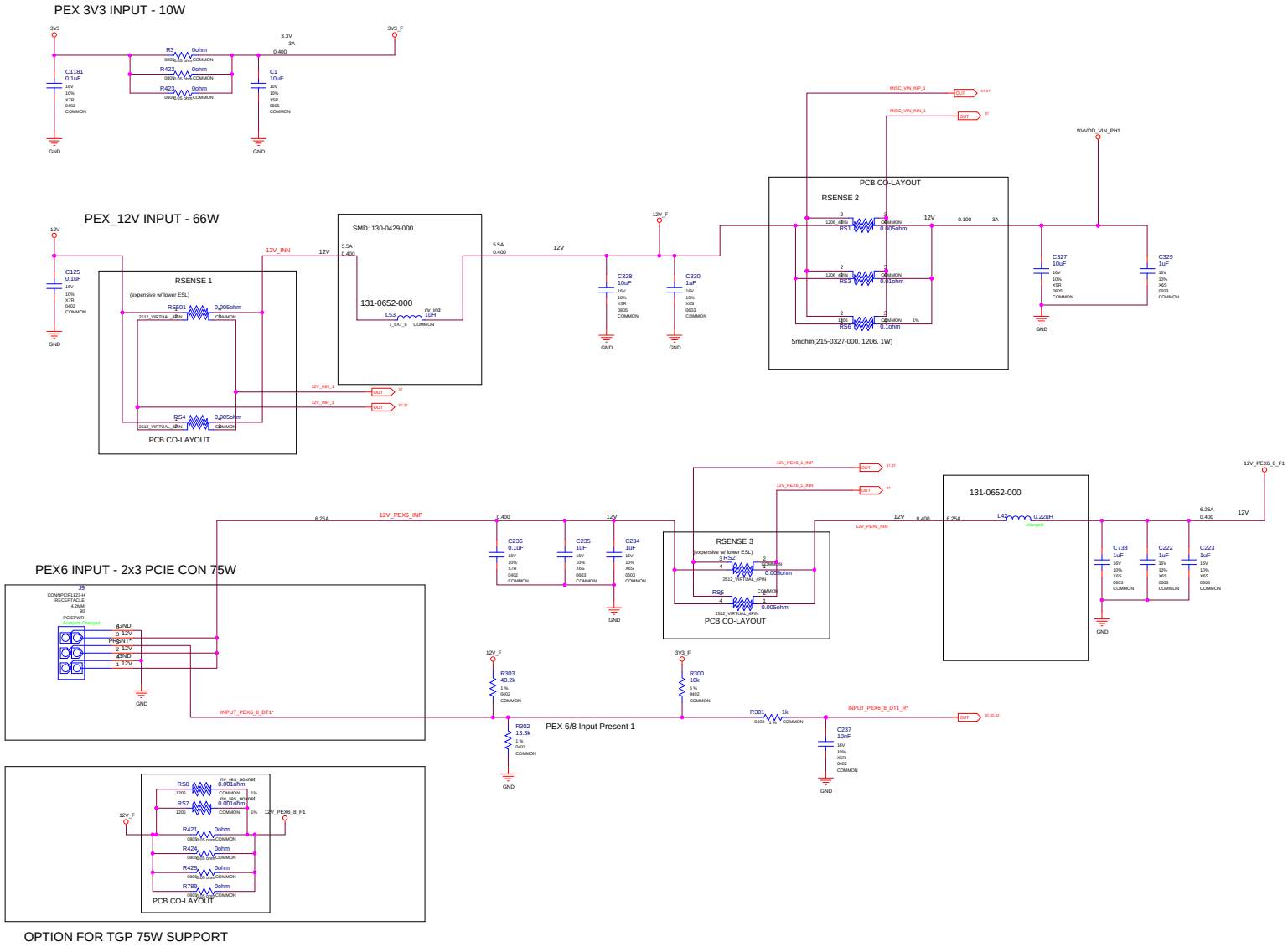
NV_PN	600-1G165-BASE-200		
PCB REV	PG165-B01	PAGE	30 OF 38
BOM REV	A	DATE	20-DEC-2018

Page31: PS: Inputs, Filtering, and Monitoring



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Input, Filtering, and Monitoring

NVIDIA CORPORATION
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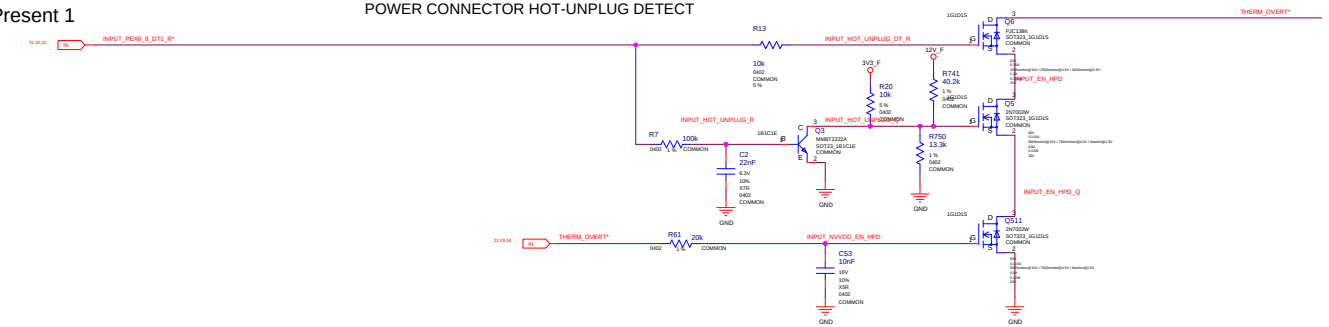
Page32: PS: HOT-UNPLUG, UNDER POWER BOOT, CURRENT STEERING

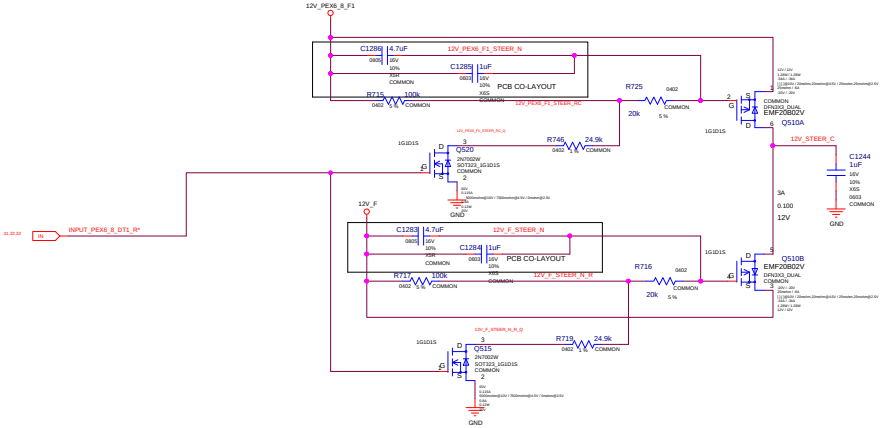
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

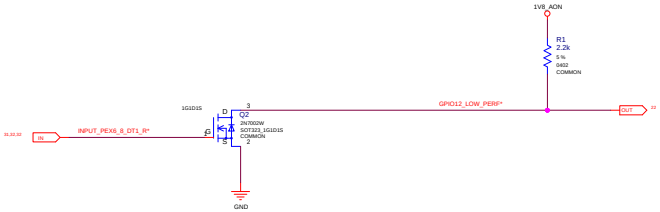


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: STEERING, UPB & HOT-UNPLUG

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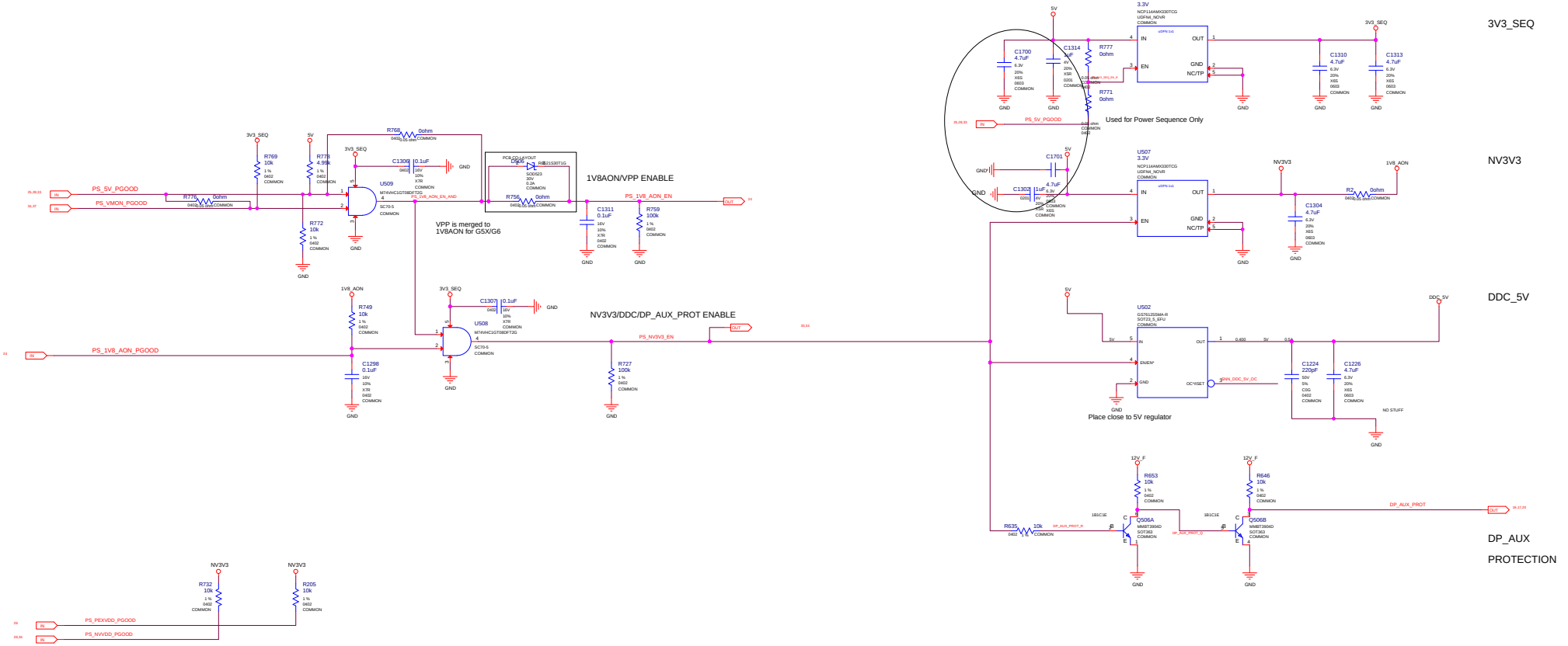
Page33: SEQ:1V8_AON, 3V3_SEQ, NV3V3, DDC_5V, DP_AUX_PROT



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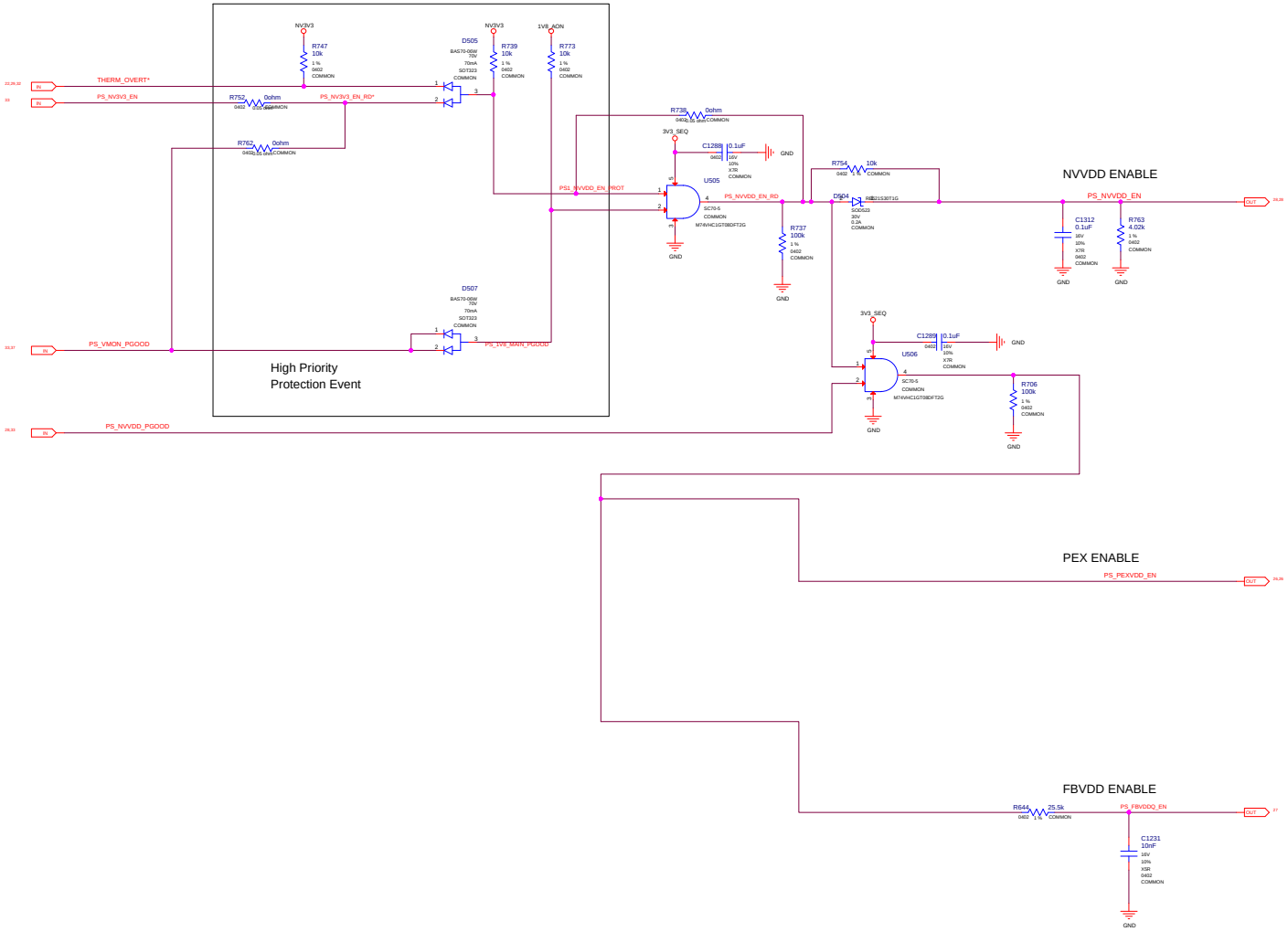
Page34: SEQ:NVVDD, PEX, FBVDDQ ENABLE



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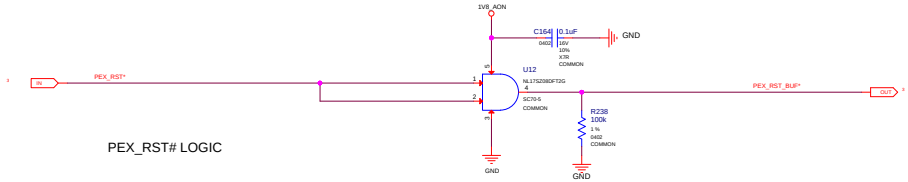
Page35: SEQ:MISC

PU ON GPU SIDE
NC ON GOLD FINGER SIDE

PU ON GPU SIDE
NC ON GOLD FINGER SIDE



PEX_RST# LOGIC

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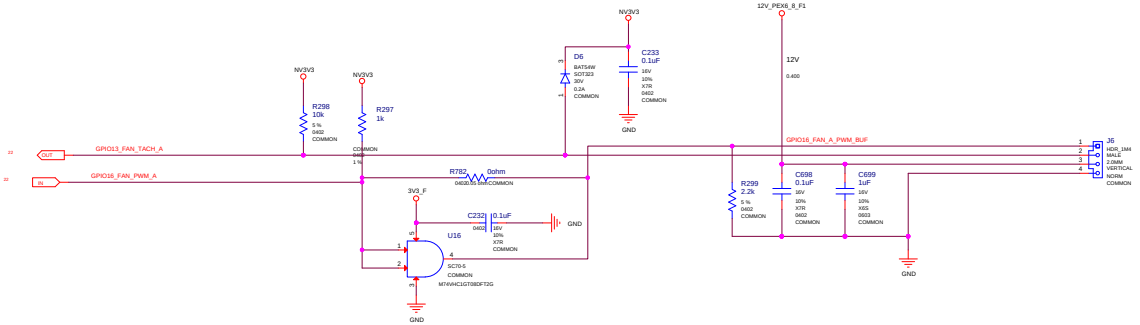
Page36: FAN



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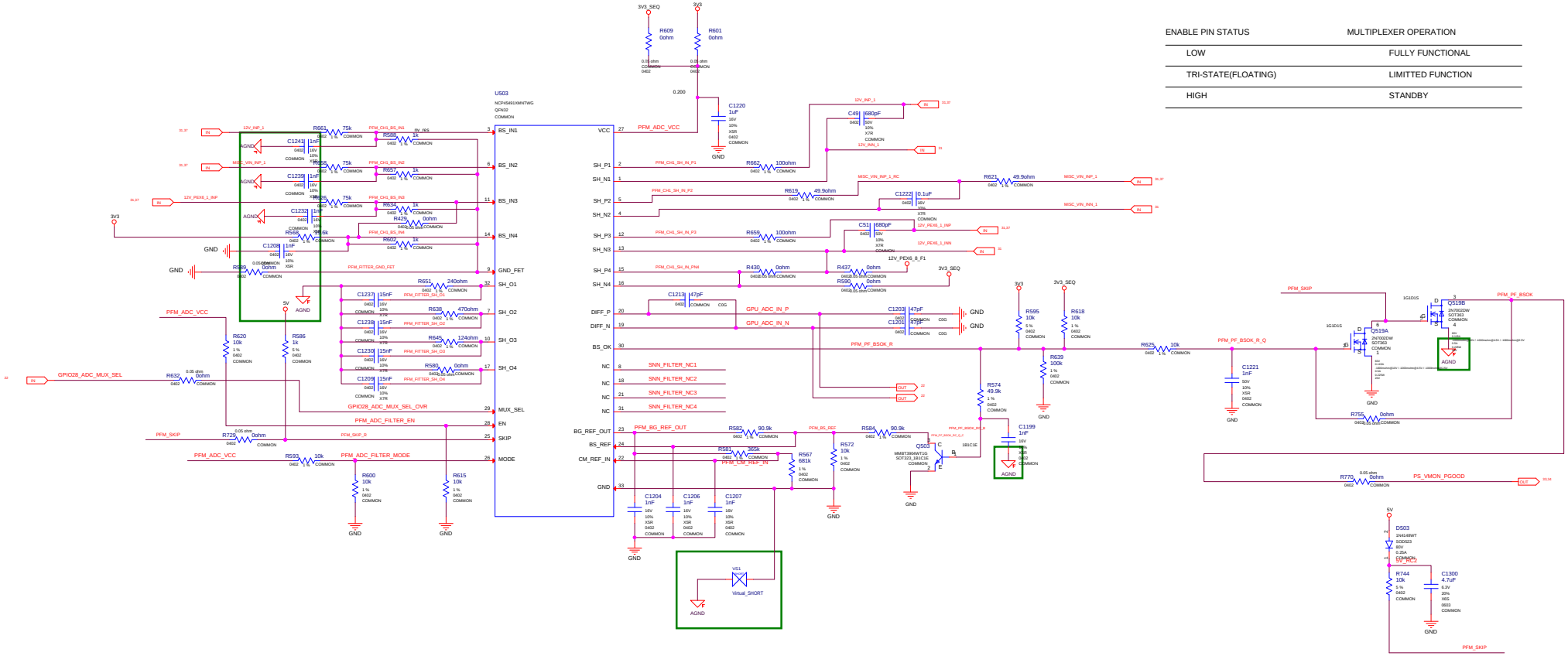
Page37: OVRM_PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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PAGE DETAIL	PS: OVRM_PWR SENSE

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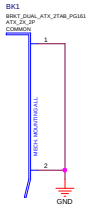
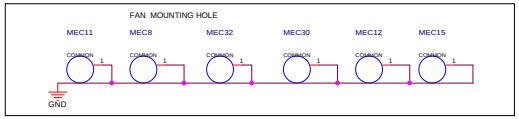
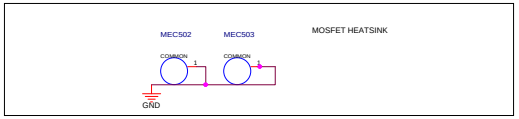
Page38: MECH

Bracket:







BACK STIFFENER:

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH

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