

電子類元件 零件承認書文件 CHECK LIST

零件廠商: Infineon(代理商:品佳)

品名規格 : PWM IR35217MGB02TRP IR

技嘉料號 : 10TA1-603521-10R

項次	文件項目
Data Sheet 檢核項目	
1	DATASHEET (含機構尺寸、 端子腳鍍層材質、MSL Report)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。 註 2
8	零件樣品 20PCS(Chipset 等高單價，至少 1PCS)
9	電子零件承認基本調查表 。 註 3
10	以上資料電子檔為 PDF 檔，且是同 1 個 File
GSCM 綠色產品管理系統-物料管制文件檢核清單	
物料管制文件 1	GSCM 綠色產品管理系統：零件照片
物料管制文件 2	GSCM 綠色產品管理系統：不使用禁用物質證明書 (保證書)。 註 4
物料管制文件 3	GSCM 綠色產品管理系統：Data Sheet
GSCM 綠色產品管理系統-MCD 表格	
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
其他文件 (僅適用電阻、電容類之系列元件)	
附件 1	危害物質測試報告 Test Report of Hazardous Substances。 註 5
附件 2	元件調查表 Component Composition Table

- ※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等
- ※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)
 - 2.1. 基本需符合 JEDEC 規範
 - 2.2. Ambient Temp. (Reflow Temp endurace): >225°C, 70 sec. 零件塑膠材質需 PA9T(含)等級以上
 - 2.3. PASTE IN HOLE 零件塑膠材質需 PA9T(含)等級以上
- ※ 3. **電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G*,11T***
非 IC 類：10C*,11C*,10L*,11L*,10X*,11X*,10R*,11B*
- ※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”
- ※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

電子零件承認基本調查表

一、原物料規格/來源			
項次	部位名稱/規格	材質	原物料來源產地
1	chip	Wafer	Singapore(因英飛凌將各部位原物料來源皆列為機密,故以產品出貨地 Singapore 代表)
2	leadframe	inorganic material	Singapore(因英飛凌將各部位原物料來源皆列為機密,故以產品出貨地 Singapore 代表)
3	wire	Metal	Singapore(因英飛凌將各部位原物料來源皆列為機密,故以產品出貨地 Singapore 代表)
4	encapsulation	organic material	Singapore(因英飛凌將各部位原物料來源皆列為機密,故以產品出貨地 Singapore 代表)
5	plating	palladium	Singapore(因英飛凌將各部位原物料來源皆列為機密,故以產品出貨地 Singapore 代表)
6	solder	silver	Singapore(因英飛凌將各部位原物料來源皆列為機密,故以產品出貨地 Singapore 代表)

二、晶圓廠(非 IC 類免填)					
項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	Infineon	Germany	8	80	自有

三、封裝廠(IC 類)；成品之生產製造工廠(非 IC 類)				
項次	工廠名稱	生產產地	投產比率(%)	自有/外包
3	Amkor	Philippines	80%	外包

四、產能	
總產能(月/PCS)	可供技嘉產能(月/PCS)
6M	1M

- ※ 1. IC 類之晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件
- ※ 2. 非 IC 類零件之成品生產製造工廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件
- ※ 3. 以上資訊欄位若有不足，可自行增加行數

品 佳 股 份 有 限 公 司
SILICON APPLICATION CORP.
地址: 中和市建八路 2 號 18F
電話: 02-8226-1500
傳真: 02-8226-1502

樣 品 確 認 書

客 戶 名 稱 : 技嘉科技股份有限公司

製 造 廠 商: Infineon

產 品 編 號: IR35217MGB02TRP

確 認 結 果 : 可用 不可用

說 明:

確 認 者 職 稱 :

確 認 者 簽 章 :

確 認 日 期 : 年 月 日

IR35217 Digital Multi-phase Controller

8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller

Quality Requirement Category: Industrial

Features

- Ultra Low Quiescent Power Dual output 8 phase (8+0/7+1/ 6+2) PWM Controller
- Intel® VR12 Rev 1.7, VR12.5 Rev 1.5, IMVP8 Rev 1.2, AMD SVI2 Rev 1.06 & Memory VR modes
- Fast Overcurrent Flag output to warn CPU/GPU of VR overcurrent condition
- IR Efficiency Shaping Features including Dynamic Phase Control and Automatic Power State Switching
- Programmable 1-phase or 2-phase operation for Light Loads and Active Diode Emulation for very Light Loads
- IR Adaptive Transient Algorithm (ATA) on both loops minimizes output bulk capacitors and system cost
- Auto-Phase Detection with PID Coefficient auto-scaling
- Fault Protection: OVP, UVP, OCP, OTP, CATFLT
- I₂C/SMBus/PMBus system interface for reporting of Temperature, Voltage, Current & Power telemetry for both loops
- Multiple Time Programming (MTP) with integrated charge pump for easy non-volatile programming
- Compatible with 3.3V tri-state drivers
- +3.3V supply voltage; -40°C to 85°C ambient operation; -40°C to 125°C junction
- Pb-Free, RoHS, 7x7mm 56-pin, 0.4mm pitch QFN

Applications

- Intel® VR12, VR12.5 and IMVP8 (overclocking only), AMD SVI2 based systems
- High End Desktop CPU and GPU VR
- High Performance Graphics Processors, Memory VR

Description

The IR35217 is a dual-loop digital multi-phase buck controller designed for CPU and GPU voltage regulation, and is fully compliant with Intel® VR12 Rev 1.7, VR12.5 Rev 1.5, IMVP8² Rev 1.2, and AMD SVI2 REV 1.06 specifications.

The IR35217 includes IR's Efficiency Shaping Technology to deliver exceptional efficiency at minimum cost across the entire load range. IR's Dynamic Phase Control adds/drops phases based upon load current. The IR35217 can be configured to enter 1 or 2-phase PS1 operation and active diode emulation mode automatically or by command.

IR's unique Adaptive Transient Algorithm (ATA), based on proprietary non-linear digital PWM algorithms, minimizes output bulk capacitors.

IR35217 has 127 possible address values for both the PMBus and I₂C bus interfaces. The device configuration can be easily defined using the IR PowIRCenter GUI, and is stored in the on-chip Non-Volatile Memory (NVM). This reduces external components and minimizes the package size.

The IR35217 provides extensive OVP, UVP, OCP, OTP & CATFLT fault protection, and includes thermistor based temperature sensing or per phase temperature reporting when using the IR PowIRstage. The controller is designed to work with either Rdson current sense PowIRstages or with DCR current sense.

The IR35217 also includes numerous VR design simplifying and differentiating features, like register diagnostics, which enable fast time-to-market.

Table of Contents

Features	1
Applications	1
Description	1
Table of Contents	2
1 Ordering Information	5
2 Functional Block Diagram	7
3 Typical Application Diagram	8
4 Pin Descriptions	9
5 Absolute Maximum Ratings	13
6 Electrical Specifications	14
7 General Description	19
7.1 Operating Modes	19
7.2 Digital Controller and PWM	19
7.3 Adaptive Transient Algorithm (ATA)	19
7.4 Multiple Time Programming Memory	19
7.5 Internal Oscillator	19
7.6 High-precision Voltage Reference	20
7.7 Output Voltage Sense	21
7.8 Output Current Sense	21
7.9 VID Decode	21
7.10 MOSFET Driver and Power Stage Compatibility	21
7.11 I ₂ C and PMBus Interface	21
7.12 PowIRCenter GUI	21
7.13 Programming	22
7.14 Real-time Monitoring	22
8 Theory of Operation	24
8.1 Operating Mode	24
8.2 Device Power-on and Initialization	24
8.3 Test Mode	25
8.4 Supply Voltages	25
8.4.1 CFILT	25
8.4.2 VIN	25
8.4.3 VAUX	26
8.5 Power-on Sequence	27
8.6 Power-off Sequence	28
8.7 AMD SVI2 Mode	29
8.7.1 Vboot and Slew Rate	29
8.7.2 PSI[x]_L and TFN Control Bits	30
8.7.3 SVT Telemetry	30
8.7.4 Load Line Slope Trim	30
8.7.5 Offset Trim	31
8.7.6 Ispike/Dual OCP Support	31
8.7.7 Thermal Based Protection	31
8.7.8 AMD SVI2 Address Programming	32
8.9 Intel Mode	36
8.9.1 Boot Voltage and Slew Rate	36
8.9.2 Intel SVID Interface	36
8.9.3 Intel SVID Addressing	36
8.9.4 Intel VID Offset	37

8.9.5	Intel Reporting Offset.....	37
8.9.6	All Call Support.....	38
8.9.7	VR12.5 Operation	38
8.9.8	IMVP8 Operation.....	38
8.9.8.1	IVID Registers	38
8.9.9	SVID Registers.....	38
8.10	Loop Start-up Sequence and Delay	45
8.11	Memory (MPoL) Mode	45
8.12	Phasing.....	46
8.13	Switching Frequency	48
8.14	MOSFET Driver and Power Stage Selection	49
8.15	Output Voltage Differential Sensing.....	49
8.16	Input Current Sensing.....	50
8.17	Output Current Sensing.....	50
8.17.1	Output Current Balance & Offset.....	51
8.17.2	Output Current Calibration.....	53
8.18	Load Line for Active Voltage Positioning.....	53
8.18.1	DCR Current Sense	53
8.18.2	Rds(on) Current Sense	55
8.18.3	Setting a $\text{om}\Omega$ Load Line	56
8.19	Digital Feedback Loop and PWM Control	56
8.20	Adaptive Transient Algorithm (ATA)	57
8.21	Dynamic Output Voltage Control	59
8.21.1	Slew Rate	59
8.21.2	Dynamic Output Voltage Compensation	60
8.22	Efficiency Shaping	60
8.22.1	Power States	60
8.22.2	Dynamic Phase Control (DPC) in PSo	61
8.22.3	Discontinuous Mode of Operation – PS ₂ , PS ₃	64
8.22.4	PS ₄ Mode	65
8.22.4.1	Ps ₄ Register Support	65
8.23	Variable Frequency with Load (Loop1 Only)	65
9	Faults and Protections	67
9.1	Output Over-voltage Protection (OVP)	67
9.2	Output Under-voltage Protection (UVP)	69
9.3	Output Over-current Protection (OCP).....	70
9.3.1	Current Limit	70
9.3.2	Slow Current Limit.....	70
9.4	FAST Over-current Protection and IOUT_ALERT#.....	70
9.5	Over-temperature Protection (OTP).....	71
9.5.1	NTC Temperature Sensing	71
9.5.2	Power Stage Temperature Sensing (TOUT).....	72
9.6	Input Over-voltage Protection.....	73
9.7	Phase Faults	73
9.8	Warning Flags.....	73
9.8.1	VRHOT_ICRIT# Pin Functionality	73
9.8.2	Icritical Flag	74
9.8.3	PIN_ALERT#	74
10	Telemetry Monitoring Functions.....	75
10.1	Real-time Telemetry.....	75
10.2	Min/Max Telemetry	75
10.3	Accuracy Optimization Registers.....	76

11	I ₂ C/PMBus Communication	78
11.1	Addressing	78
11.2	I ₂ C Security	79
11.2.1	Password Protection	79
11.2.1.1	Pin Protection	80
11.3	I ₂ C Protocol.....	80
11.4	PMBus Protocol.....	80
11.5	PMBus Command Set.....	83
11.6	11-bit Linear Format	88
11.7	16-bit Linear Format.....	88
12	Package	90
12.1	Marking Information	90
12.2	Dimensions.....	90
12.3	Environmental Qualifications	91
13	References.....	92
	Revision History	93

Downloaded by
FXDMZpar-yangtsun
12/06/2019 10:11:22

Ordering Information

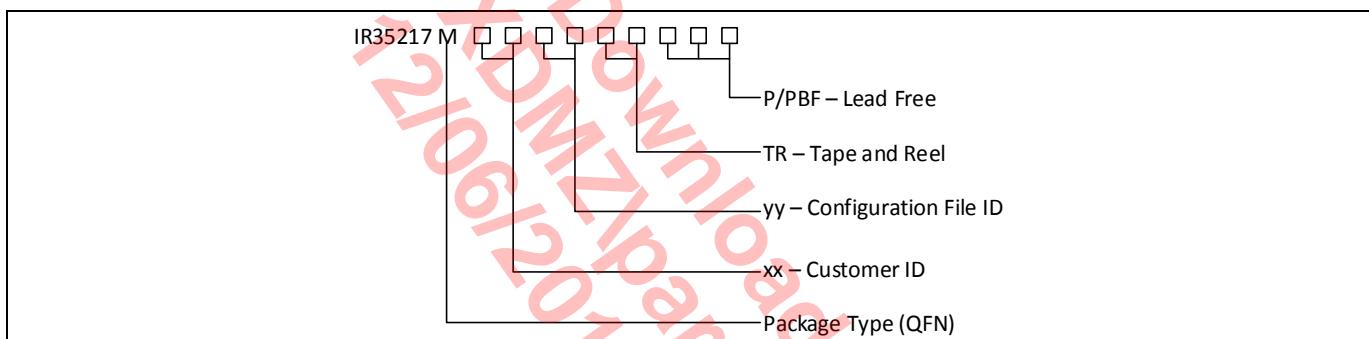
1 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Standard Pack Form and Qty		Orderable Part Number
IR35217	QFN 7mm x 7mm	Tape and Reel	3000	IR35217MxxyyTRP ¹
IR35217	QFN 7mm x 7mm	Tape and Reel	3000	IR35217MTRPBF

Note:

- 1) Customer Specific Configuration File, where xx = Customer ID and yy = Configuration File (Codes assigned by IFX Marketing).
 2) The IR35217 is not intended for applications where ultra-low power PS4 shutdown functionality is required



Restricted

IR35217 Digital Multi-phase Controller

8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller



Ordering Information

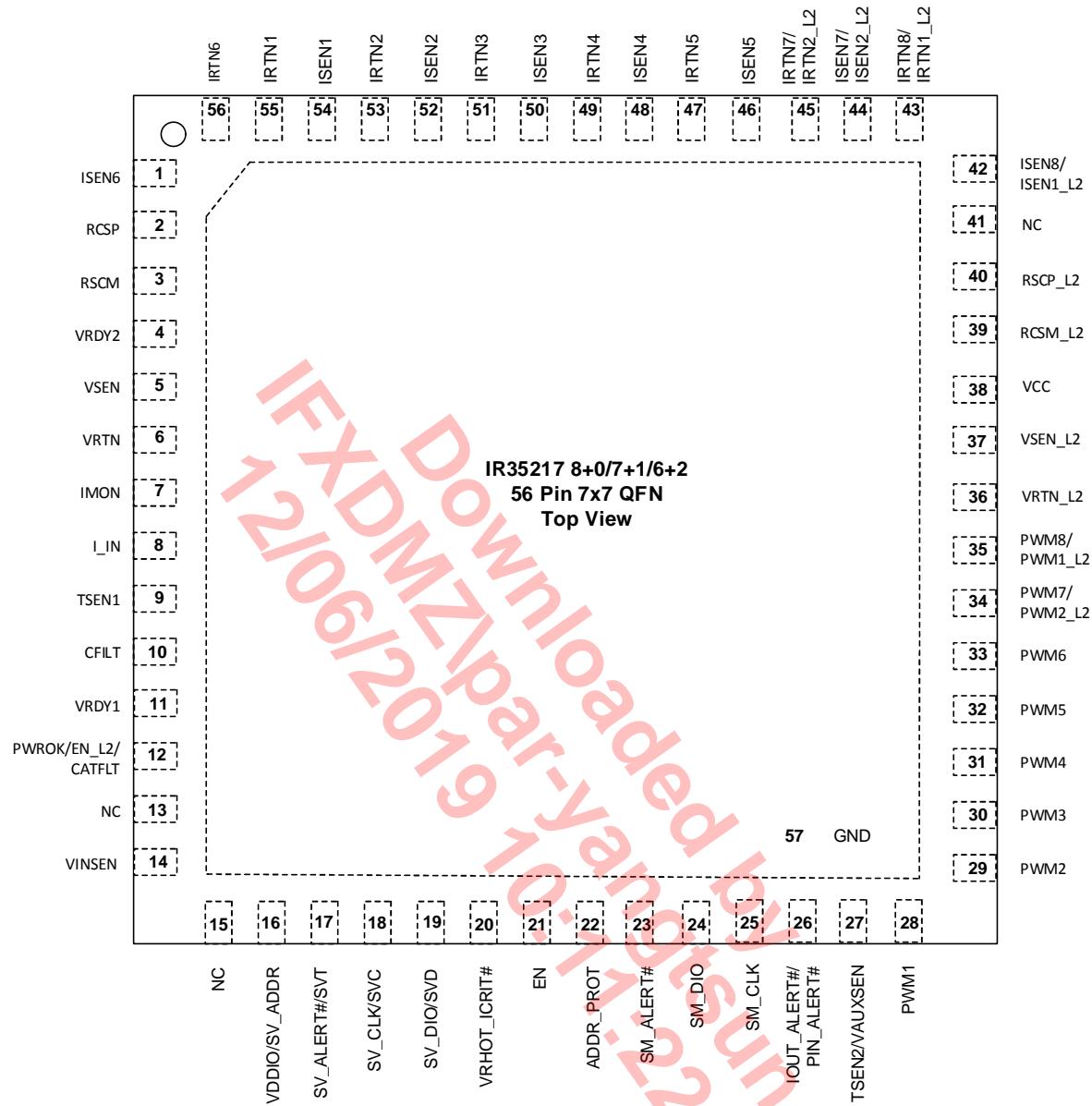


Figure 1 Pin Diagram

Functional Block Diagram

2 Functional Block Diagram

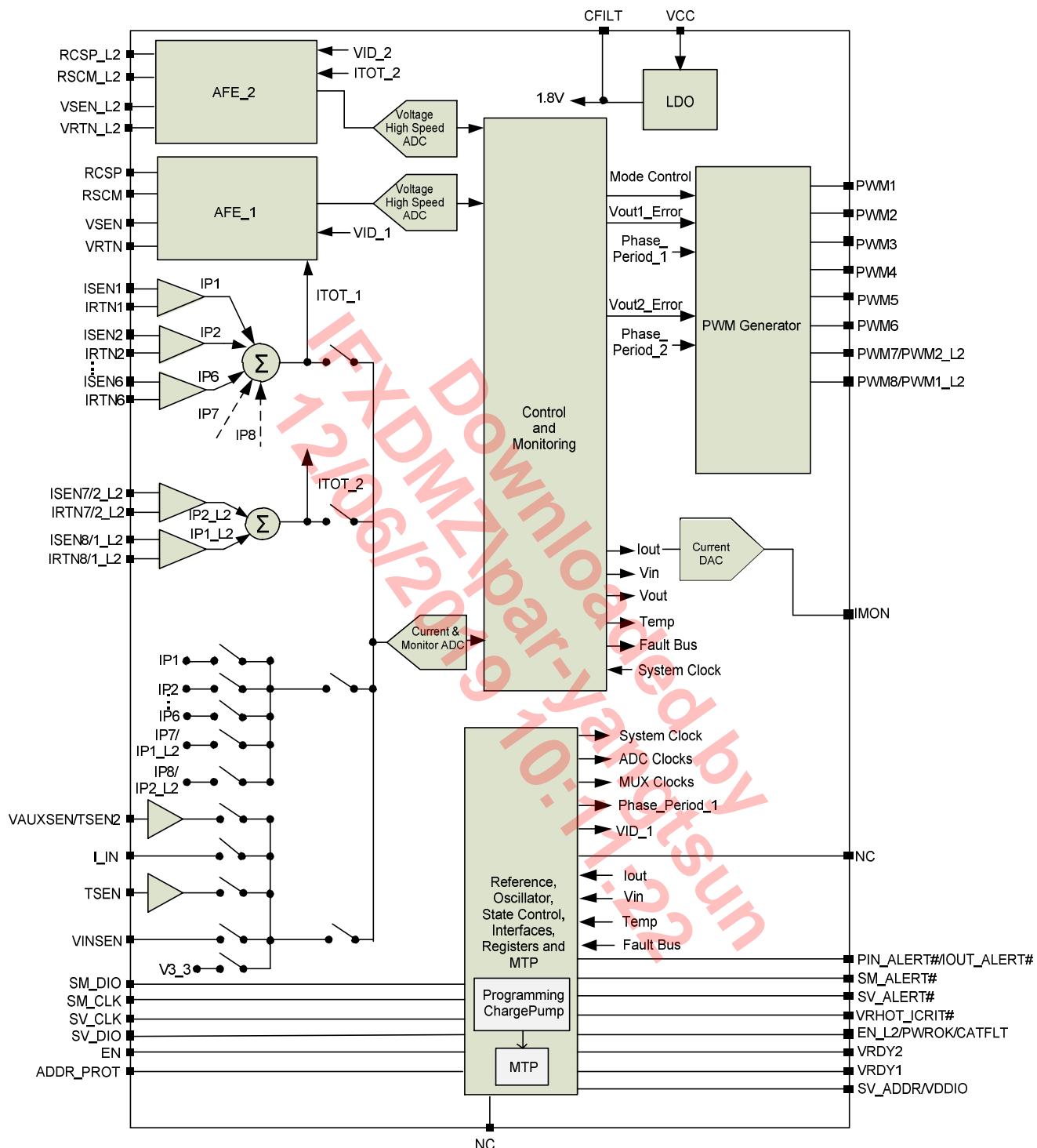


Figure 2 Block Diagram

Typical Application Diagram

3 Typical Application Diagram

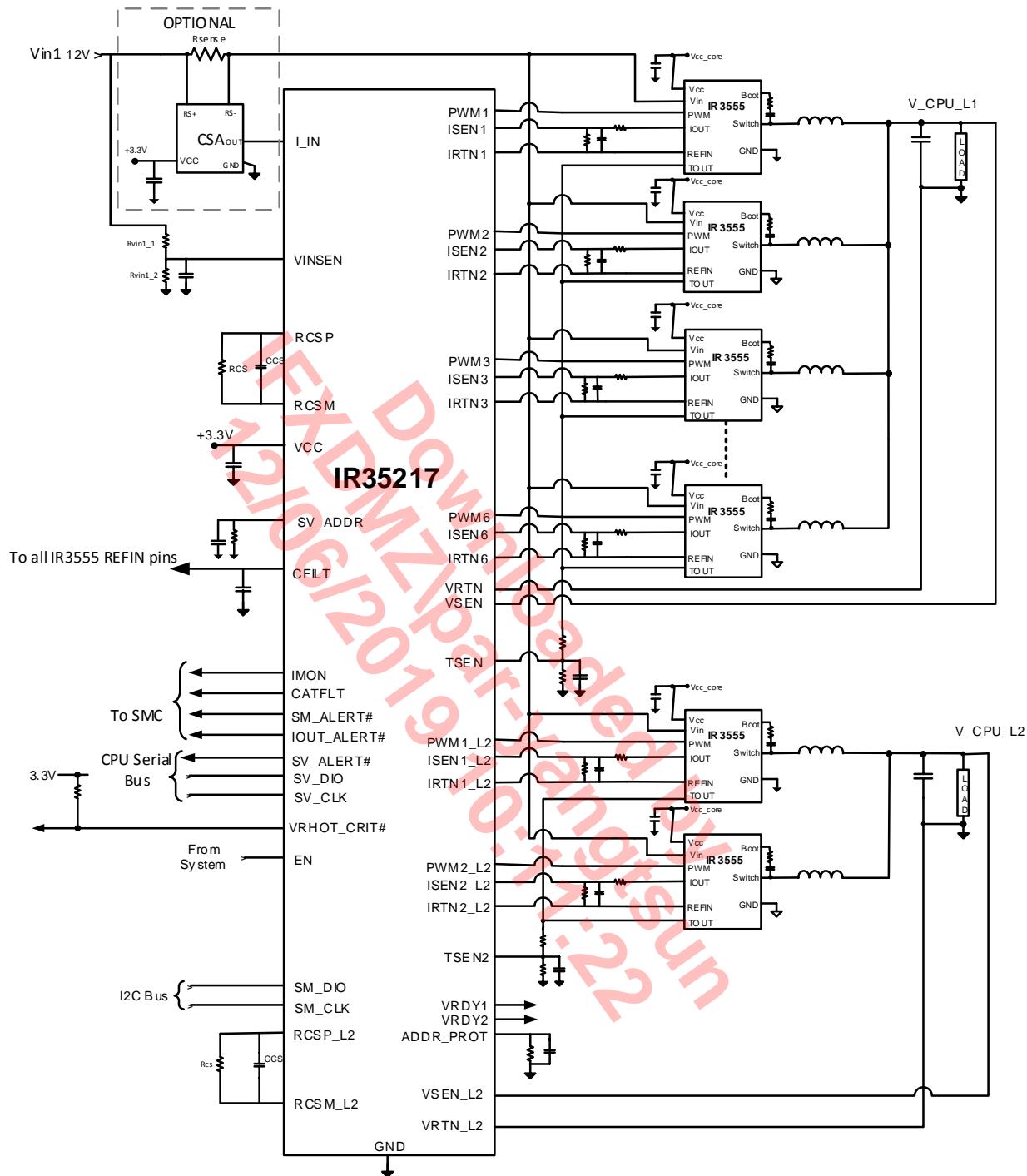


Figure 3 Dual Loop VR using IR35217 Controller and IR3555 Power Stage in 6+2 Phase Configuration

Pin Descriptions

4 Pin Descriptions

Table 2 Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	ISEN6	A [I]	Phase 6 Current Sense Input. Phase 6 sensed current input (+).GND if not used.
2	RCSP	A [O]	Resistor Current Sense Positive. This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop 1.
3	RCSM	A [O]	Resistor Current Sense Minus. This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop 1.
4	VRDY2	D [O]	Voltage Regulator Ready Output (Loop #2). Open-drain output that asserts high when the VR has completed soft-start to Loop #2 boot voltage. Pull-up to an external voltage through a resistor.
5	VSEN	A [I]	Voltage Sense Input. This pin is connected directly to the VR output voltage of Loop #1 at the load and should be routed differentially with VRTN.
6	VRTN	A [I]	Voltage Sense Return Input. This pin is connected directly to Loop#1 ground at the load and should be routed differentially with VSEN.
7	IMON	A [O]	Output Current Monitor. This pin puts out an analog output voltage corresponding to average output current. $0.8V = 0$ load, $2.5V = 255A$. The maximum current for this pin is $+/- 100\mu A$. An output capacitor on this pin is not required but if a capacitor is used, its value must be limited to a maximum of $1nF$.
8	I_IN	A [I]	I_in. Input current signal that ranges from 0 to 1.25Vdc. Used for applications that require an external input current measurement to drive the PIN ALERT# output pin and SVID input Power reporting register
9	TSEN1	A [I]	Temperature Sense Input Loop 1. An NTC network or the temperature reporting output from an IR PowRstage can be connected to this pin to measure temperature for VRHOT and OTP shutdown. When connected to the IR PowRstage's temperature output; the scaled input voltage to the controller needs to be at a gain of 4.88mV per degC and an offset of 0.365 Vdc so the controller can correctly report temperature. Typically a 10kohm and 6.39kohm resistive divider is used to accomplish the scaling between the power stage and the controller.
10	CFILT	A [O]	1.8V Decoupling. A $1\mu F$ capacitor on this pin provides decoupling for the internal 1.8V supply.
11	VRDY1	D [O]	Voltage Regulator Ready Output (Loop #1). Open-drain output that asserts high when the VR has completed soft-start to Loop #1 boot voltage. Pull-up to an external voltage through a resistor.
12	PWROK/ EN_L2/ CATFLT	D [I]	Power OK Input (AMD). An input that when low indicates to return to the Boot voltage and when high indicates to use the SVI bus.
			VR Enable for Loop 2. When configured, ENABLE for Loop 2 is an active high system input to power-on Loop 2, provided Vin and Vcc are present. ENABLE is not pulled up on the controller. When ENABLE is pulled low, the controller de-asserts VR READY2 and shuts down loop 2 only.
			Catastrophic Fault Output Pin. This pin may be used as a Catastrophic Fault CMOS Output Pin that is driven to VCC under output OVP, NVM CRC errors or a TSENx fault input.
13	NC		Do Not Connect
14	VINSEN	A [I]	Voltage Sense Input. This is used to detect and measure a valid input supply voltage (typically 4.5V-13.2V) to the VR.
15	NC		Do Not Connect
16	VDDIO/	A [P]/	VDDIO Input (AMD). This pin provides the voltage to which the SVT line and the SVD Acknowledge are

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
	SV_ADDR	A [I]	driven high. SVID Address Input (INTEL). A resistor to ground on this pin defines the SVID address which is latched when Vcc becomes valid. Requires a 0.01μF bypass capacitor.
17	SVT/ SV_ALERT#	D [O]	SVI Telemetry Output (AMD). Telemetry and VOTF information output by the IR35217 Serial VID ALERT# (INTEL). SVID ALERT# is pulled low by the controller to alert the CPU of new VR12/12.5/IMVP8 Status. Pull-up to an external voltage through a resistor.
18	SVC/ SV_CLK	D [I]	Serial VID Clock Input. Clock input driven by the CPU Master.
19	SVD/ SV_DIO	D [B]	Serial VID Data I/O. Is a bi-directional serial line over which the CPU Master issues commands to slave/s and receives data back.
20	VRHOT_ICRIT #	D [O]	VRHOT_ICRIT# Output. Active low alert pin that can be programmed to assert if temperature or average load current exceeds user-definable thresholds. Pull-up to an external voltage through a resistor.
21	EN	D [I]	VR Enable Input. ENABLE is used to power-on the regulator, provided Vin and Vcc are present. ENABLE is not pulled up in the controller. The polarity of the chip enable function is bit-settable to either an active high or an active low configuration. ENABLE pin cannot be left floating. ENABLE pin must be pulled high or low.
22	ADDR_PROT	D [B]/	Bus Address & I₂C Bus Protection. A resistor to ground on this pin sets the offset to the NVM value of the I ₂ C address if configured to do so. Subsequently, this pin becomes a logic input to enable or disable communication on the I ₂ C bus when protection is enabled. Requires a 0.01μF to ground for noise filtering.
23	SM_ALERT#	D [O]	SMBus/PMBus Alert Line. Active low alert pin to indicate that the regulator status has changed. Requires a pull-up. Ground if not used.
24	SM_DIO	D [B]	Serial Data Line I/O. I ₂ C/SMBus/PMBus bi-directional serial data line. Ground if not used.
25	SM_CLK	D [I]	Serial Clock Line Input. I ₂ C/SMBus/PMBus clock input. The interface is rated to 1 MHz. Ground if not used.
26	IOUT_ALERT# PIN_ALERT#	D [O]	IOUT_ALERT# Output. Active low alert pin that can be programmed to assert if the output current exceeds user-defined threshold. Pull-up to an external voltage through a resistor. PIN_ALERT# Output. Active low alert pin that can be programmed to assert if the input power exceeds a user defined threshold. Pull-up to an external voltage through a resistor
27	TSEN2 VAUXSEN	A [I] A [I]	Temperature Sense Input Loop #2. An NTC network or the temperature reporting output from an IR PowIRstage can be connected to this pin to measure temperature for VRHOT. Float if not used. Auxiliary Voltage Sense Input. Monitors an additional power supply to ensure that both the IR35217 Vcc and other voltages (such as VCC to the driver) are operational. Float if not used.
28 - 33	PWM1 – PWM6	A [O]	Phase 1-6 Pulse Width Modulation Outputs. PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active. Float if not used.
34	PWM7/ PWM2_L2	A [O]	Phase 7 Pulse Width Modulation Outputs. PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active. Float if not used. Loop 2 Phase 2 Pulse Width Modulation Outputs. PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active.
35	PWM8/	A [O]	Phase 8 Pulse Width Modulation Outputs. PWM signal pin which is connected to the

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
	PWM1_L2		input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active. Float if not used.
			Loop 2 Phase 1 Pulse Width Modulation Outputs. PWM signal pin which is connected to the input of an external MOSFET gate driver. The power-up state is high-impedance until ENABLE goes active.
36	VRTN_L2	A [I]	Voltage Sense Return Input Loop#2. This pin is connected directly to Loop 2 ground at the load and should be routed differentially with VSEN_L2. GND if not used.
37	VSEN_L2	A [I]	Voltage Sense Input Loop#2. This pin is connected directly to the VR output voltage of Loop 2 at the load and should be routed differentially with VRTN_L2. GND if not used.
38	VCC	A [P]	Input Supply Voltage. 3.3V supply to power the device.
39	RCSM_L2	A [I]	Resistor Current Sense Minus Loop#2. This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop 2. Connect 10K to RCSP if not used
40	RCSP_L2	A [I]	Resistor Current Sense Positive Loop#2. This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop 2.
41	NC		Do Not Connect
42	ISEN 1_L2/ ISEN8	A [I]	Loop 2 Phase 1 Current Sense Input. Loop 2 Phase 1 sensed current input (+). GND if not used.
			Phase 8 Current Sense Input. Phase 8 sensed current input (+).GND if not used.
43	IRTN 1_L2/ IRTN8	A [I]	Loop 2 Phase 1 Current Sense Return Input. Loop 2 Phase 1 sensed current input return (-). GND if not used.
			Phase 8 Current Sense Return Input. Phase 8 sensed current input return (-).GND if not used.
44	ISEN 2_L2/ ISEN7	A [I]	Loop 2 Phase 2 Current Sense Input. Loop 2 Phase 2 sensed current input (+).GND if not used.
45	IRTN 2_L2/ IRTN7	A [I]	Loop 2 Phase 2 Current Sense Return Input. Loop 2 Phase 2 sensed current input return (-).GND if not used.
			Phase 7 Current Sense Return Input. Phase 7 sensed current input return (-).GND if not used.
46	ISEN 5	A [I]	Phase 5 Current Sense Input. Phase 5 sensed current input (+).GND if not used.
47	IRTN 5	A [I]	Phase 5 Current Sense Return Input. Phase 5 sensed current input return (-). GND if not used.
48	ISEN 4	A [I]	Phase 4 Current Sense Input. Phase 4 sensed current input (+).GND if not used.
49	IRTN 4	A [I]	Phase 4 Current Sense Return Input. Phase 4 sensed current input return (-).GND if not used.
50	ISEN 3	A [I]	Phase 3 Current Sense Input. Phase 3 sensed current input (+).GND if not used.
51	IRTN 3	A [I]	Phase 3 Current Sense Return Input. Phase 3 sensed current input return (-).GND if not used.
52	ISEN 2	A [I]	Phase 2 Current Sense Input. Phase 2 sensed current input (+).GND if not used.
53	IRTN 2	A [I]	Phase 2 Current Sense Return Input. Phase 2 sensed current input return (-).GND if not used.
54	ISEN 1	A [I]	Phase 1 Current Sense Input. Phase 1 sensed current input (+).GND if not used.
55	IRTN 1	A [I]	Phase 1 Current Sense Return Input. Phase 1 sensed current input return (-).GND if not used.
56	IRTN6	A [I]	Phase 6 Current Sense Return Input. Phase 6 sensed current input return (-).GND if not used.

Restricted

IR35217 Digital Multi-phase Controller

8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller



Pin Descriptions

Pin#	Pin Name	Type	Pin Description
57 (PAD)	GND		Ground. Ground reference for the IC. The large metal pad on the bottom must be connected to Ground.

A-Analog; D-Digital; [I]-Input; [O]-Output; [P]-Power

Downloaded by
IFXDMZpar-yangtsun
12/06/2019 10:11:22

Absolute Maximum Ratings

5 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Supply Voltage (VCC)	GND-0.3V to 4.0V
RCSPx, RCSMx	0 to 2.2V
VSENx, VRTNx, ISENx, IRTNx, IMON	GND-0.2V to VCC + 0.3V
CFILT, VINSEN, I_IN	GND-0.2V to 2.2V
TSENx, PWROK, VDDIO, IOUT_ALERT#, PIN_ALERT#	GND-0.3V to VCC
SV_CLK, SV_DIO, SV_ALERT#, SV_ADDR	GND-0.3V to VCC
VRDYx, ENx, ADDR_PROT, VRHOT_ICRIT#, CATFLT	GND-0.3V to VCC
PWMx	GND-0.3V to 4.1V
SM_DIO, SM_CLK, SM_ALERT#	GND-0.3V to 5.5V
ESD Rating	
Human Body Model	2000V
Machine Model	200V
Charge Device Model	1000V
Thermal Information	
Thermal Resistance (θ_{JA} & θ_{JC}) ¹	29°C/W & 3°C/W
Maximum Operating Junction Temperature	-40°C to 125°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

Note: ¹ θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Electrical Specifications

6 Electrical Specifications

Table 4 Recommended Operating Conditions for Reliable Operation with Margin

Recommended Operating Ambient Temperature Range	-40°C to 85°C
Supply Voltage Range	+2.90V to +3.6V

The electrical characteristics table lists the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

Table 5 Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply	VCC, CFILT, GND					
Supply Voltage	V _{cc}		2.90	3.3	3.6	V
Supply Current	I _{vcc}		-	44	52	mA
3.3V UVLO Turn-on Threshold			-	2.80	2.9	V
3.3V UVLO Turn-off Threshold	V _{ccuvlo}		2.6	2.65	-	V
1.8V Supply	CFILT		-	1.8	-	
1.8V Supply Current ¹	I _{cfilt}			10	40	mA
Input voltage Sense Input	VINSEN					
Input Impedance			-	1	-	MΩ
Input Range ¹	V ₁₂	With 14:1 divider	0	0.857	1.1	V
UVLO Turn-on Programmable Range ¹			-	4.5 – 13.2	-	V
UVLO Turn-off Programmable Range ¹	V _{inuvlo}		-	4.5 – 13.2	-	V
OVP Threshold (if enabled) ¹	V _{inov}	With 14:1 divider	14.3	14.6	14.9	V
Auxiliary Voltage Sense Input	VAUXSEN					
Input Impedance			-	1	-	MΩ
Input Range ¹	Vauxsen		0	0.781	1.2	V
Turn-on Threshold ¹		VAUXSEN_on	0.642	0.664	0.686	V
UVLO Threshold ¹		VAUXSEN_off	0.564	0.586	0.608	V
Reference Voltage and DAC						
Vboot Range ¹	V _{OUT}	Intel® VR12, VR12.5, IMVP8 mode, and AMD SVI2	Meets Spec			V
Voltage Accuracy ¹	V _{OUT}	0°C to 85°C Temp Range				
		DAC = 2.005V – 3.04V	-1.1	-	1.1	%VID
		DAC = 1.0V – 2.0V	-0.5	-	0.5	%VID
		DAC = 0.8 – 0.995V	-5	-	5	mV
		DAC = 0.25 – 0.795V	-8	-	8	mV
		-40°C to 0°C Temp Range				
		DAC = 2.005V – 3.04V	-1.65	-	1.65	%VID

Restricted**IR35217 Digital Multi-phase Controller**

8+o/7+1/6+2 Dual Output Digital Multi-Phase Controller

**Electrical Specifications**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		DAC = 1.0V–2.3V	-0.75	-	0.75	%VID
		DAC = 0.8 – 0.995V	-7.5	-	7.5	mV
		DAC = 0.25 – 0.795V	-12	-	12	mV
Oscillator and PWM Generator						
Internal Oscillator			-	96	-	MHz
Frequency Accuracy			-2.5	-	2.5	%
			-5	-	5	%
PWM Frequency Range ¹	Fsw	-40°C to 125°C	194	-	2000	kHz
PWM Resolution ¹			-	163	-	ps
Temperature Sense Input - NTC	TSENx					
Output Current		For TSEN = 0 to 1.2V	96	100	104	µA
Accuracy		at 100°C (ideal NTC)	96	-	104	°C
Temperature Sense Input - TOUT	TSENx					
Input Voltage		For TSENx = 0 to 1.2V	-	4.88	-	mV/°C
Offset Voltage			-	0.365	-	V
Divider Ratio		To interface with Power Stage TOUT	-	1.64:1	-	
Digital Inputs – Low Vth Type 1	ENx (Intel), VRHOT_ICRIT# (during POR)					
Input High Voltage			0.7	-	-	V
Input Low Voltage			-	-	0.35	V
Input Leakage		Vpad = 0 to 2V	-	-	±5	µA
Digital Inputs – Low Vth Type 2	SV_CLK, SV_DIO					
Input High Voltage			0.65	-	-	V
Input Low Voltage			-	-	0.45	V
Hysteresis			-	0.95	-	V
Input Leakage		Vpad = 0 to 2V	-	-	±5	µA
Digital Inputs – LVTTL	ENx (AMD), SM_DIO, SM_CLK, ADDR_PROT					
Input High Voltage			2.1	-	-	V
Input Low Voltage			-	-	0.8	V
Input Leakage		Vpad = 0 to 3.6V	-	-	±1	µA
Remote Voltage Sense Inputs	VSENx, VRTNx					
VSEN Input Current		VSEN = 0.5V to 3.04V	-	-25 to +100	-	µA
VRTN Input Current			-	-50	-	µA
Differential Input Voltage Range ¹		VRTN = ±100mV	-	0 to 3.04	-	V
VRTN Input CM Voltage ¹			-	-100 to 100	-	mV
Phase Current Sense Inputs	ISENx, IRTNx					
Voltage Range ¹			-	-0.1 TO VCC - 0.65	-	V
Input Current Sense Input	I_IN					
Input Impedance			-	1	-	MΩ

Restricted**IR35217 Digital Multi-phase Controller****8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller****Electrical Specifications**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Voltage Range			-	0 to 1.25	-	V
Output Current Monitor	IMON					
Voltage Range		Iout = 0A to 255A	-	0.8 to 2.55	-	V
Resolution			-	5	-	mV
Output Leakage		Vpad = 0 to 3.6V	-	± 100	-	μA
Analog Address/Level Inputs	ADDR_PROT, SV_ADDR					
Output Current ¹		Vpad = 0 to 1.2V	96	100	104	μA
Open-drain Outputs – 4mA Drive	VRDYx, SM_DIO, SM_ALERT#					
Output Low Voltage		4mA	-	-	0.3	V
Output Leakage		Vpad = 0 to 3.6V	-	-	± 5	μA
Open-drain Outputs – 20mA Drive	VRHOT_ICRIT#, SV_DIO, SV_ALERT#, IOUT_ALERT#, PIN_ALERT#					
Output Low Voltage		I = 20mA	-	-	0.26	V
On Resistance		I = 20mA	7	9	13	Ω
Output Leakage		Vpad = 0 to 3.6V	-	-	± 5	μA
Output - VDDIO	SVT, SV_DIO (AMD)					
Output Low Voltage		I = 20mA	-	-	0.4	V
Pull-up ON Resistance ¹			-	12	-	Ω
CMOS Output – 3.3V	CATFLT					
Output Low Voltage		IoL = -20mA	-	-	0.4	V
Output High Voltage		IoH = 20mA	VCC – 0.4V	-	-	V
PWM Outputs	PWMx					
Output Low Voltage (Tri-state mode)		I = -4mA	-	-	0.4	V
Output High Voltage (Tri-state mode)		I = +4mA	2.9	-	-	V
Tri-State Leakage		loop_x_pwm_en_ats = 0, Vpad = 0 to Vcc	-	-	± 1	μA
PWM Auto-Detect Inputs	PWM2 – PWM8 (when 3.3V Vcc is applied) – if enabled					
Input High Voltage			0.7	-	-	V
Input Low Voltage			-	-	0.35	V
AMD SVI2 Bus Speed	SVC					
Tperiod (SVC Period) ¹			47.6		10,000	nsec
SVI2 SVC Frequency ¹			0.1	20.0	21.0	MHz
AMD SVT Telemetry						
IOUT Filter Rate ¹	SVT			11		KHz
VOUT Filter Rate ¹	SVT	Selectable	-	0.69, 1.39, 2.78, 5.55, 11.1, 22.2, 44.6, 89.5	-	Hz

Restricted**IR35217 Digital Multi-phase Controller****8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller****Electrical Specifications**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I₂C/PMBus & Telemetry						
Bus Speed ¹		Normal	-	100	-	kHz
		Fast	-	400	-	kHz
		Maximum	-	1000	-	kHz
I _{out} , V _{out} , I _{in} , V _{in} , and Temperature Filter Rate ¹		Selectable (Selected Frequency applies to all parameters)	0.69	-	89.5	Hz
I _{out} Update Rate			-	250	-	kHz
V _{out} , V _{in} , I _{in} , Temperature Update Rate ¹			-	35.7	-	kHz
V _{in} and Temperature Update Rate ¹			-	38.5	-	kHz
V _{in} Range Reporting ¹		With 14:1 divider	-	0 to 13.2	-	V
V _{in} Accuracy Reporting		With 1% resistors Range 5V to 12V	-2	-	+2	%
V _{in} Resolution Reporting - PMBus ¹			-	31.25	-	mV
V _{in} Resolution Reporting - I ₂ C ¹			-	125	-	mV
V _{out} Range Reporting ¹			-	-	4	V
V _{out} Accuracy Reporting ¹		No load-line		±0.5		%
V _{out} Resolution Reporting - PMBus ¹		V _{out} <2V	-	1.95	-	mV
V _{out} Resolution Reporting - I ₂ C ¹		V _{out} <4V	-	15.6	-	mV
I _{out} Per Phase Range Reporting ¹			0	-	62	A
I _{out} Accuracy Reporting ¹		Maximum load, all phase active (based on Rdson current sense and # active phases)	-	±2	-	%
Loop1 I _{out} Resolution Reporting - PMBus ¹		0.5A < I _{out} < 255.75A I _{out} > 255.75A	-	0.25 0.50	-	A
Loop2 I _{out} Resolution Reporting - PMBus ¹			-	0.25	-	A
Loop1 I _{out} Resolution Reporting - I ₂ C ¹			-	1	-	A
Loop2 I _{out} Resolution Reporting - I ₂ C ¹			-	0.50	-	A
Loop1 I _{in} Resolution Reporting - PMBus ¹			-	31.25	-	mA
Loop2 I _{in} Resolution Reporting - PMBus ¹			-	31.25	-	mA
Loop1 I _{in} Resolution Reporting - I ₂ C ¹			-	125	-	mA
Loop2 I _{in} Resolution Reporting - I ₂ C ¹			-	62.5	-	mA
P _{in} Resolution Reporting-PMBUS ¹			-	0.5	-	W
P _{out} Resolution Reporting-PMBUS ¹			-	0.5	-	W
Temperature Range Reporting ¹	TOUT	0	-	158	-	°C
Temperature Accuracy Reporting ¹	TOUT	-3.5	-	+3.5	-	%
Temperature Range Reporting ¹	NTC	0	-	134	-	°C
Temperature Accuracy Reporting ¹	NTC	-4	-	+4	-	%
Temperature Resolution Reporting ¹			-	1	-	°C

Restricted**IR35217 Digital Multi-phase Controller****8+o/7+1/6+2 Dual Output Digital Multi-Phase Controller****Electrical Specifications**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Fault Protections						
Fixed OVP Threshold During Startup (until Vout reaches 1V)		Selectable	-	1.2, 1.275, 1.35, 2.45	-	V
OVP Operating Threshold (programmable)		Relative to DAC	-	50 to 400	-	mV
OVP Filter Delay ¹			-	160	-	ns
Output UVLP Threshold (programmable)		Relative to DAC	-	-50 to -400	-	mV
UVLP Filter Delay ¹			-	160	-	ns
IOUT_ALERT# Delay		Delayed from summed inductor current over threshold	-	-	4	us
OCP Range (per phase) ¹			-	0 to 62	-	A
OCP Filter Bandwidth ¹			-	60	-	kHz
Slow OCP Filter Bandwidth ¹		Selectable	0.69	-	89.5	Hz
OCP System Accuracy ¹		System excluding DCR/Sense resistor	-	±2	-	%
VRHOT Range ¹			-	64 to 127	-	°C
OTP Range ^{1,2}		OTP Range (added to VR_HOT level)	-	0 to 31	-	°C
PIN_ALERT# Bandwidth			-	2	-	kHz
Dynamic Phase Control						
Current Filter Bandwidth ¹		For Phase drop	-	4	-	kHz
Timing Information						
Automatic Configuration from MTP ¹	$t_3 - t_2$	3.3V ready to end of configuration	-	-	1	ms
Automatic Trim Time ¹	$t_4 - t_3$		-	-	4	ms

Note:

1. By Design
2. Maximum OTP setting with NTC is 134 °C

7 General Description

The IR35217 is a flexible, dual-loop, digital multiphase PWM buck controller optimized to convert a 12V input supply to the core voltage required by Intel and AMD high performance microprocessors and DDR memory. It is easily configurable for 1 to 8 phases of operation on Loop #1 and 0 to 2 phase operation on Loop #2. However, at a single time, a total of only 8 phases can be in operation.

The unique partitioning of analog and digital circuits within the IR35217 provides the user with easy configuration capability while maintaining the required accuracy and performance. Access to on-chip Multiple Time Programming memory (MTP) to store the IR35217 configuration parameters enables power supply designers to optimize their designs without changing external components.

7.1 Operating Modes

The IR35217 can be used for Intel® VR12, VR_{12.5}, IMPVP8 designs, AMD SVI₂, and DDR Memory without significant changes to the Bill of Materials (BOM). The required mode is selected in MTP and the pin-out, output voltage, and other relevant functions are automatically configured. This greatly reduces time-to-market and eliminates the need to manage and inventory different PWM controllers.

7.2 Digital Controller and PWM

A linear Proportional-Integral-Derivative (PID) digital controller provides the loop compensation for system regulation. The digitized error voltage from the high-speed voltage error ADC is processed by the digital compensator. The digital PWM generator uses the outputs of the PID and the phase current balance control signals to determine the pulse width for each phase on each loop. The PWM generator has enough resolution to ensure that there are no limit cycles. The compensator coefficients are user configurable to optimize the system response. The compensation algorithm uses a PID with two additional programmable poles. This provides the digital equivalent of a Type III analog compensator.

7.3 Adaptive Transient Algorithm (ATA)

Dynamic load step-up and load step-down transients require fast system response to maintain the output voltage within specification limits. This is achieved by a unique adaptive non-linear digital transient control loop based on a proprietary algorithm.

7.4 Multiple Time Programming Memory

The multiple time programming memory (MTP) stores the device configuration. At power-up, MTP contents are transferred to operating registers for access during device operation. MTP allows customization during both design and high-volume manufacturing. MTP integrity is verified by Cyclic Redundancy Code (CRC) checking on each power up. The controller will not start up in the event of a CRC error.

The IR35217 offers up to 6 writes to configure basic device parameters such as frequency, fault operation characteristics, and boot voltage. This represents a significant size and component saving compared to traditional analog methods.

7.5 Internal Oscillator

The IR35217 has a single 96MHz internal oscillator that generates all the internal system clock frequencies required for proper device function. The oscillator frequency is factory trimmed for precision, and has extremely low jitter (Figure 4) even in light-load mode (Figure 5). The single internal oscillator is used to set the same switching frequency on each loop.

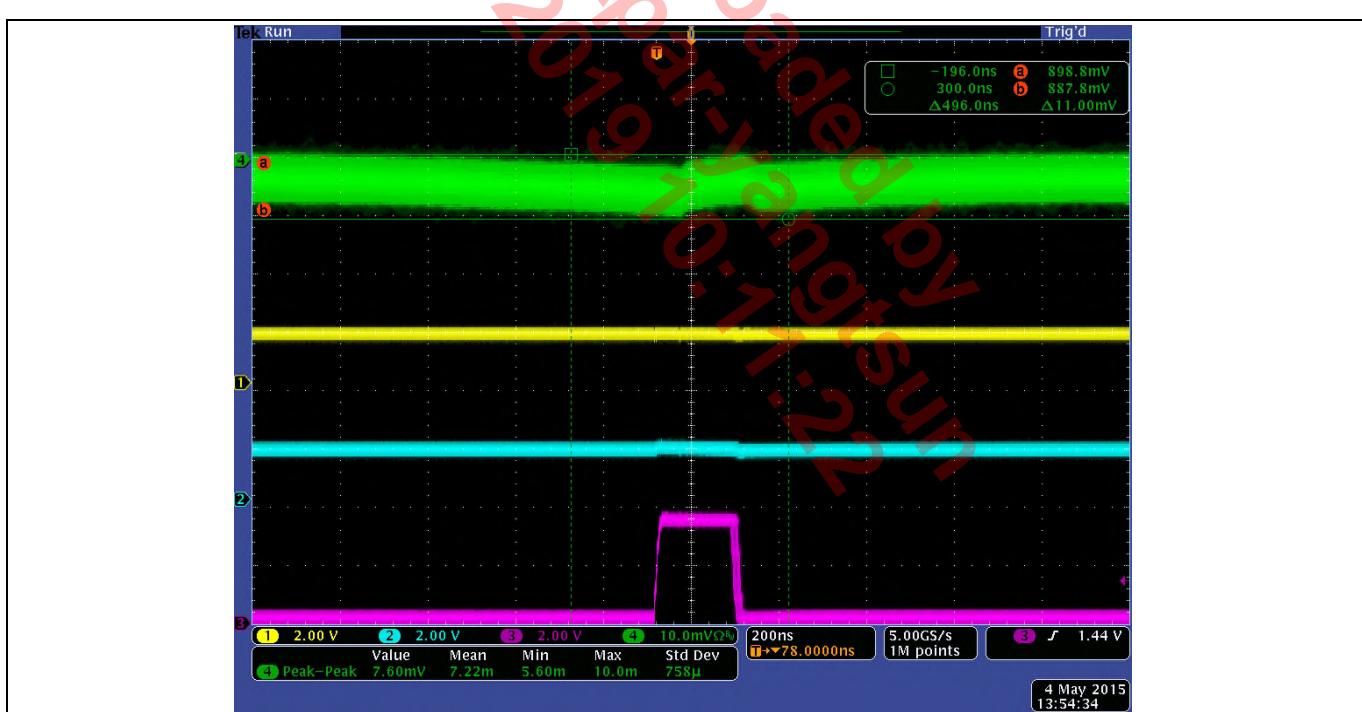
Restricted

IR35217 Digital Multi-phase Controller

8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller



General Description



7.6

High-precision Voltage Reference

The internal high-precision voltage reference supplies the required reference voltages to the VID DACs, ADCs and other analog circuits. This factory trimmed reference is guaranteed over temperature and manufacturing variations.

General Description

7.7 Output Voltage Sense

An error voltage is generated from the difference between the target voltage, defined by the VID and the differentially sensed output voltage (remote sense). For each loop, the error voltage is digitized by a high-speed, high-precision ADC. An anti-alias filter provides the necessary high frequency noise rejection. The gain and offset of the voltage sense circuitry for each loop is factory trimmed to deliver the required accuracy.

7.8 Output Current Sense

Lossless inductor DCR or precision resistor current sensing is used to accurately measure individual phase currents. Using a simple off-chip thermistor, resistor and capacitor network for each loop, a thermally compensated load line is generated to meet the given power system requirement. A filtered voltage, which is a function of the total load current and the target load line resistance, is summed into each voltage sense path to accomplish the Active Voltage Positioning (AVP) function.

The IR35217 can also be used with Rdson current sensing from Power Stages. This algorithm helps reduce components by eliminating the need for the R-C sense components. Also, the thermistor used for thermal compensation would no longer be required, as this function is inherently designed into the Rdson sensing of the Power Stages. The R-C network across the pins would still be required.

7.9 VID Decode

The VID decoder receives a VID code from the CPU that is converted to an internal code representing the VID voltage. This block also outputs the signal for VR disable if a VID shutdown code has been received. The 8 bit VID code supports Intel® VR12 & VR12.5 modes and VID settings are selectable as either 5mV/code or 10mV/code on each loop independently. When AMD SVI2 mode is chosen, both loops will be set to 6.25mV/code

7.10 MOSFET Driver and Power Stage Compatibility

The output PWM signals of the IR35217 are designed for compatibility with industry standard +3.3V Tri-State MOSFET drivers.

7.11 I₂C and PMBus Interface

An I₂C or PMBus interface is used to communicate with the IR35217. This two-wire serial interface consists of clock and data signals, and operates as fast as 1MHz. The bus provides read & write access to the internal registers for configuration, and for monitoring of operating parameters. The bus is also used to program on-chip non-volatile memory (MTP) to store operating parameters.

To ensure operation with multiple devices on the bus, an exclusive address for the IR35217 is programmed into MTP.

To protect customer configuration and information, the I₂C interface can be configured for either limited access or locked with a 16-bit software password. Limited access includes both write and read protection options. In addition, there is a telemetry-only mode which only allows reads from the telemetry registers.

The IR35217 supports the Packet Error Checking (PEC) protocol and a number of PMBus commands to monitor voltages and currents. Refer to the PMBus Command Codes in Table 51 for more information.

7.12 PowIRCenter GUI

The PowIRCenter GUI provides the designer with a comprehensive design environment that includes interactive tools to calculate VR efficiency and DC error budget, design thermal compensation & feedback loop networks, generate system loop response (Bode plots) & output impedance plots. The GUI environment is a key utility for

General Description

design optimization, debug, and validation of designs that saves the designer significant time and allowing faster time-to-market (TTM).

The PowIRCenter GUI allows real-time design optimization and monitoring of key parameters such as output current and power, input current and power, efficiency, phase currents, temperature, and faults.

The PowIRCenter GUI also allows access to the system configuration settings for switching frequency, soft start rate, output voltage setting, power savings settings, loop compensation, transient control system parameters, input under-voltage, output over-voltage, output under-voltage, output over-current and over-temperature.

7.13 Programming

Once a design is complete, the PowIRCenter GUI produces a complete configuration file.

The configuration file can be re-coded into an I₂C/PMBus master (e.g. a Test System) and loaded into the IR35217 using the bus protocols described on Page 80. The IR35217 has a special in-circuit programming mode that allows the MTP to be loaded at board test in mass production without powering on the entire board.

7.14 Real-time Monitoring

The IR35217 can be accessed through the use of PMBus Command codes (described in Table 51), to read the real time status of the VR system including input voltage, output voltage, input and output current, input and output power, efficiency and temperature.

In addition, the IMON pin puts out an analog output voltage corresponding to the total average output current according to Figure 6. This internally generated signal provides the user with additional flexibility in making decisions based on the reported output current. Care needs to be taken to ensure that this pin is not loaded, as the source capability of this pin is limited to 100uA. An output capacitor on this pin is not required but if a capacitor is used, its value must be limited to a maximum of 1nF.

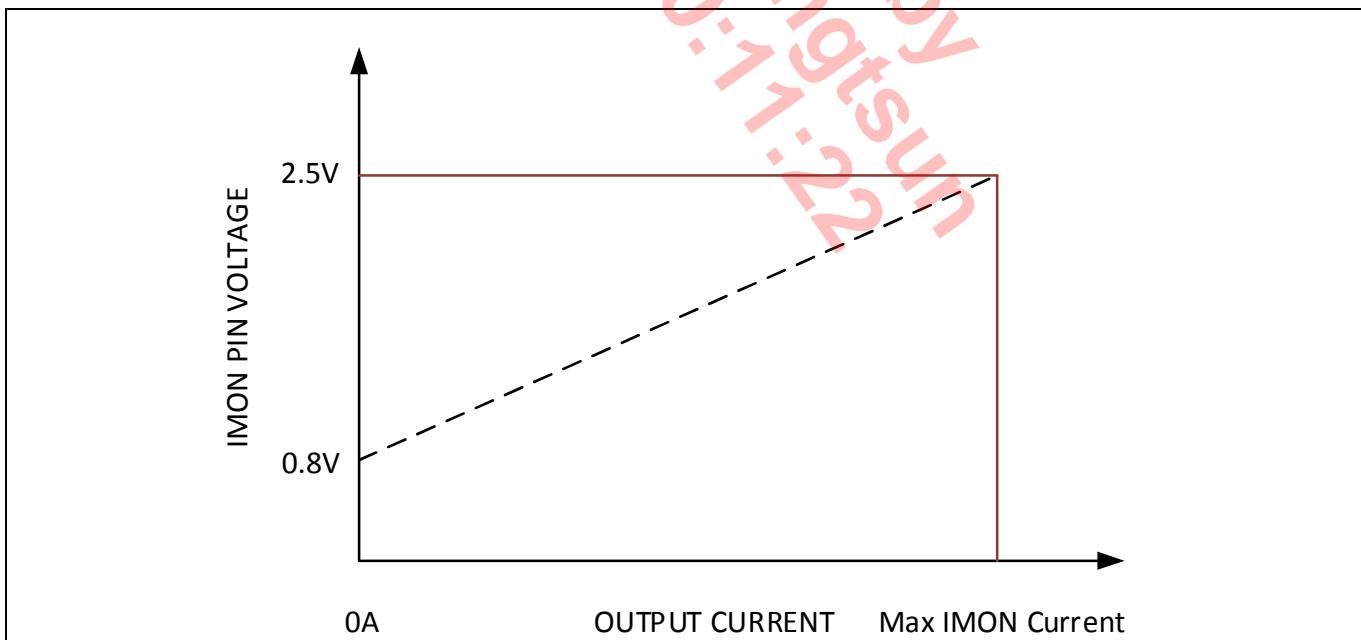


Figure 6 IMON Voltage (V) versus Output Current (A)

General Description



Figure 7 Response time IMON Voltage (V) versus Output Current (A)

8 Theory of Operation

8.1 Operating Mode

The IR35217 changes its functionality based on the user-selected operating mode, allowing one device to be used for multiple applications without significant BoM changes. This greatly reduces the user's design cycles and time-to-market (TTM).

The functionality for each operating mode is completely configurable by simple selections in MTP. The mode configuration is shown in Table 6.

Table 6 Mode Selection

Mode	Description
VR12	Intel® VR12 (Selected via MTP).
VR12.5	Intel® VR12.5 (Selected via MTP).
IMVP8	Intel® IMVP8 (Selected via MTP).
SVI2	AMD SVI2 (Selected via MTP).
mPOL	Memory Mode, with Loop 2 output voltage = $\frac{1}{2}$ Loop 1 output voltage.

8.2 Device Power-on and Initialization

The IR35217 is powered from a 3.3V DC supply. Figure 8 shows the timing diagram during device initialization. An internal regulator generates a 1.8V rail to power the control logic within the device. During initial startup, the 1.8V rail follows the rising 3.3V supply voltage, proportional to an internal resistor tree. The internal oscillator becomes active at t_1 as the 1.8V rail is ramping up. Until soft-start begins, the IR35217 PWM outputs are disabled in a high impedance state to ensure that the system comes up in a known state.

The controller comes out of power-on reset (POR) at t_2 when the 3.3V supply is high enough for the internal bias control to generate 1.8V. After a delay of ($t_3 - t_2$), the trims are read and the automatic trim routines are completed by time t_4 . Upon completing the loading of trim registers, the user configuration registers will be initiated at t_4 and complete by t_5 . At this time; if enabled in MTP and when the VINSEN voltage is valid, the controller will initiate soft-start if there is no fault in the system.

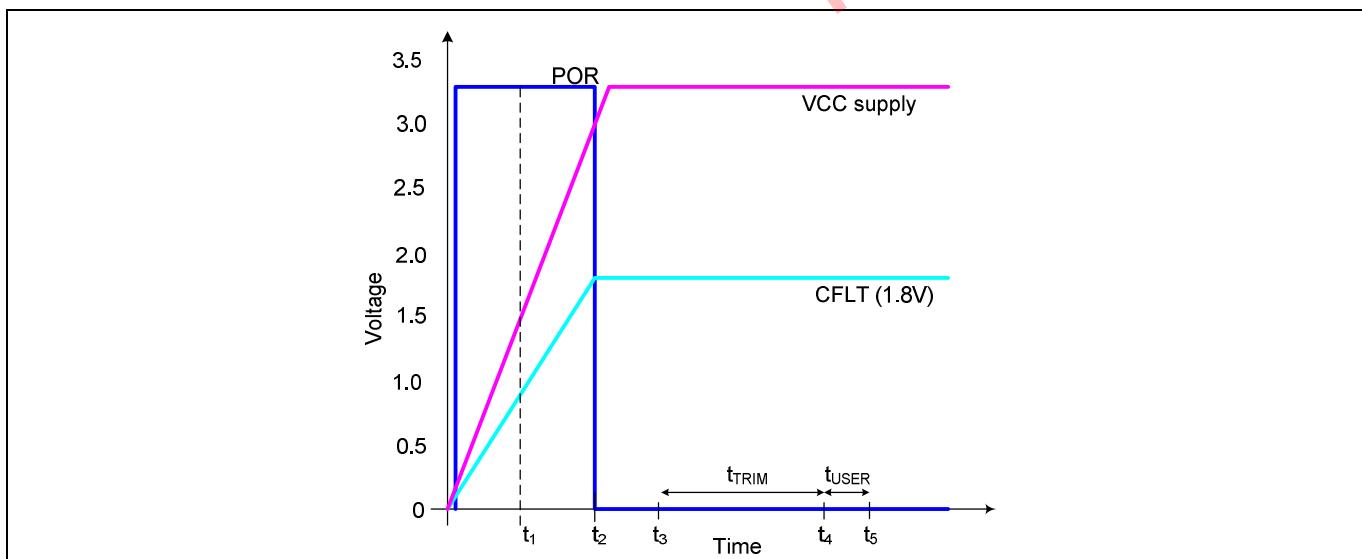


Figure 8 Controller Startup and Initialization

Theory of Operation

8.3 Test Mode

Driving the ADDR_PROT pin high (+3.3V) engages a special test mode in which the I₂C address changes to 0Ah. This allows individual in-circuit programming of the controller. This is specifically useful in multi-controller systems that use a single I₂C bus. *Note that MTP will not load to the working registers when the device powers up in test mode.*

8.4 Supply Voltages

The controller is powered by a 3.3V supply rail VCC, and has an internal 1.8V LDO (CFLT) that is used to power internal circuitry. The power phases in the voltage regulator are powered by VIN while the Power Stages/MOSFET Drivers that control the VR are supplied by a lower voltage VAUX supply, typically 5V.

The recommended decoupling for the 3.3V is shown in Figure 9. The Vcc pin should have a 0.1μF and 1μF X5R-type ceramic capacitors placed as close as possible to the package.

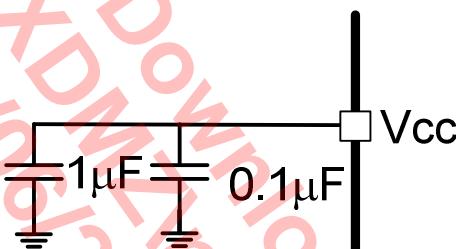


Figure 9 VCC 3.3V Decoupling

8.4.1 CFLT

The CFLT pin must have a 1μF, X5R type decoupling capacitor connected close to the package as shown in Figure 10.

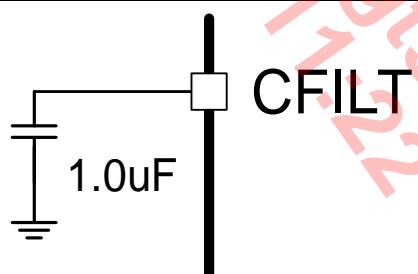


Figure 10 CFLT 1.8V Decoupling

8.4.2 VIN

The IR35217 is designed to accommodate a wide variety of input power supplies & applications and allows user to program the VINSEN turn-on/off voltages.

Table 7 VINSEN Turn-on/off Voltage Range

Threshold	Range
Turn-on	4.5V to 13.1875V in 1/16V steps ¹
Turn-off	4.5V to 13.1875V in 1/16V steps ¹

Theory of Operation

Note: ¹ Must not be programmed below 4.5V

The VIN supply voltage on the VINSEN pin is compared against a programmable threshold. Once the rising VINSEN voltage crosses the turn-on threshold and ENx is asserted, all PWM outputs become active. The VINSEN supply voltage is valid until it falls below the programmed turn-off level.

A 14:1 attenuation network is connected to the VINSEN pin as shown in Figure 11. Recommended values for a 12V system are $R_{VIN_1} = 13k\Omega$ and $R_{VIN_2} = 1k\Omega$, with a 1% tolerance or better. CVINSEN is required to have a minimum 1nF for noise suppression, with a maximum value of 10nF.

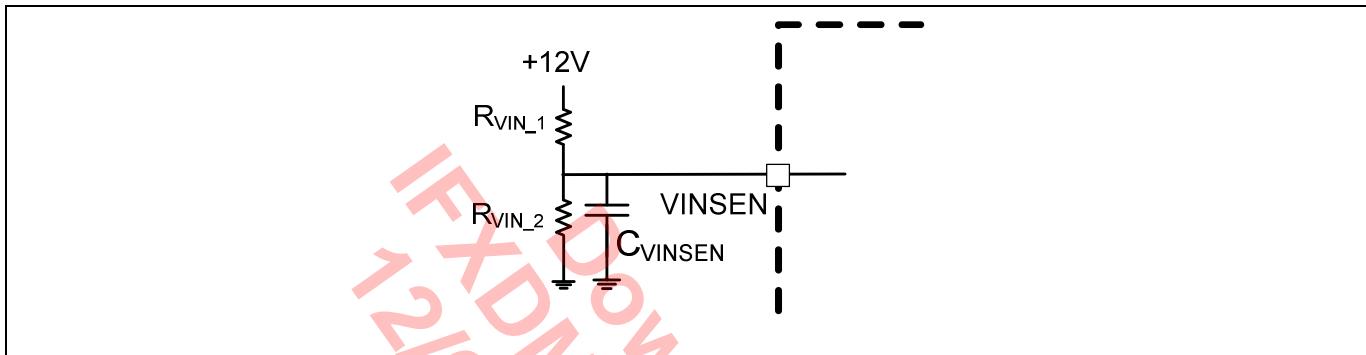


Figure 11 VINSEN Resistor Divider Network

8.4.3 VAUX

The IR35217 also supports monitoring of an auxiliary supply rail (typically used to monitor Power Stage VCC to control sequencing). The supply voltage on the VAUXSEN pin is compared against a programmable threshold. Once the rising VAUXSEN voltage crosses the turn-on threshold and ENx is asserted, all PWM outputs become active when there are no faults in the VR. The VAUXSEN supply voltage is valid until it falls below the programmed turn-off level.

The desired ON and OFF thresholds are adjusted by setting the correct divider network, R1 and R2, as shown in Figure 12. C1 is added to suppress noise at the VAUXSEN pin. A minimum value of 1nF is required, with a maximum value of 10nF.

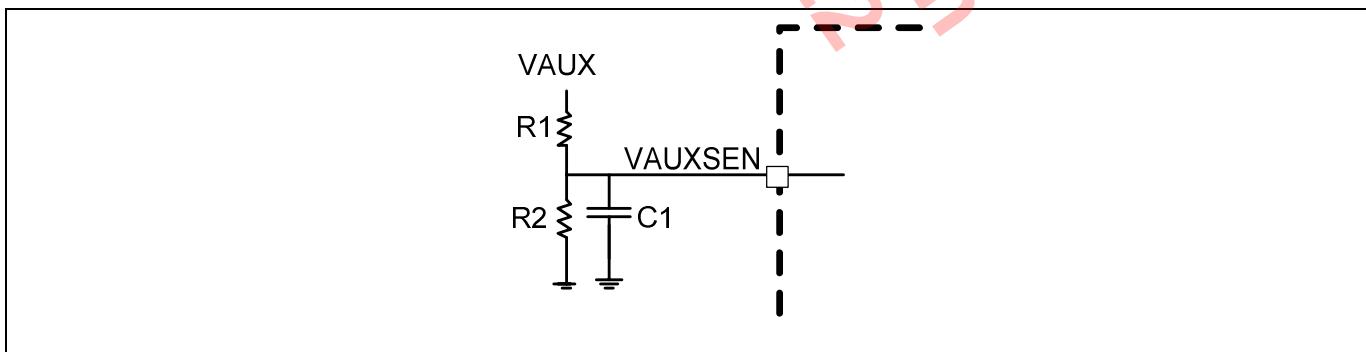


Figure 12 VAUXSEN Resistor Divider Network

The VAUX ON and OFF thresholds are defined as:

$$VAUX_ON = vauxsen_on \times \left(1 + \frac{R1}{R2}\right)$$

Theory of Operation

$$VAUX_{OFF} = vauxsen_{off} \times \left(1 + \frac{R1}{R2}\right)$$

Where $vaux_on = 0.664V$, and $vaux_off = 0.586V$. With $R2$ set to 1kohm, Table 8 shows the ON and OFF thresholds for various values of $R1$.

Table 8 VAUXSEN Turn-on/off Voltages

R1	VAUX_ON	VAUX_OFF
5.76kohm	4.5V	3.97V
8.87kohm	6.56V	5.75V
11.8kohm	8.5V	7.5V
14.7kohm	10.44V	9.2V

The VAUX UV function can be disabled so that VAUXSEN input can be used for voltage monitoring without shutting down the VR. The telemetry for VAUX is provided by an 8-bit read only register, $vaux_supply$. The reported VAUX voltage can be translated with the following formula:

$$VAUX = vaux_supply(dec) \times 4.88mV \times \left(1 + \frac{R1}{R2}\right)$$

8.5 Power-on Sequence

Once initialization of the device is complete, the ENx signal is used to begin the soft start sequence by enabling the PWMs once the 3.3V and Input Supply rails (VIN and VAUX) are within the defined operating bands.

The VR power-on sequence is initiated when all of the following conditions are satisfied:

- IR35217 Vcc (+3.3V rail) > VCC Start Threshold (2.8V)
- Input Voltage (VINSEN rail) > Vin Start Threshold
- Vaux Voltage (if enabled) > VAUX_ON
- ENABLE is HIGH
- The VR has no Over-current, Over-voltage, Over-temperature, Under-voltage, TSEN high or VAUX UVLO faults (when monitored)
- MTP transfer to configuration registers occurred without parity error

Once the above conditions are cleared, start-up behavior as shown in Figure 13 is controlled by the operating mode.

Theory of Operation



Figure 13 Enable-based Startup

8.6

Power-off Sequence

When the controller is disabled by deactivating the ENx signal, it de-asserts VR READY and shuts down the regulator as shown in Figure 14. The output voltage ramps down to 0V using the set slew rate. When VIN goes below the controller's turn-off threshold, the controller tri-states all PWM's, and the output voltage decays to 0V as shown in Figure 15.



Figure 14 Enabled-based Shutdown (Ramping)

Theory of Operation



Figure 15 VIN-based Shutdown (Decay)

8.7 AMD SVI2 Mode

8.7.1 Vboot and Slew Rate

When the power-on sequence is initiated, both rails will ramp to the configured Vboot voltage shown in Table 9 and assert the VRDYY signal on each loop. The soft-start occurs at the $\frac{1}{2}$ or $\frac{1}{4}$ multiplier slew rate as selected in Table 10. Note: VCC and VDDIO must be stable a minimum 5msec prior to the assertion of enable to ensure the Boot Voltage is decoded from the SVC and SVD pins correctly. SVT also must be stable and above its High Threshold at the assertion of enable for the controller to properly operate in AMD SVI2 mode.

Table 9 AMD SVI2 Boot Table

Boot Voltage	SVC	SVD
1.1V	0	0
1.0V	0	1
0.9V	1	0
0.8V	1	1

Table 10 Slew Rates – mV/usec

FAST Rate	$\frac{1}{2}$ Multiplier	$\frac{1}{4}$ Multiplier
10	5.0	2.50
15	7.5	3.75
20	10	5.00
25	12.5	6.25

Theory of Operation

Alternatively, the AMD boot voltage can be set by an MTP register instead of decoding the SVC, SVD pins as shown in Table 11. Boot values are shown in Table 13 and Table 14.

Table 11 AMD Mode Boot Options

MTP Boot Register	Boot Location
Bit[7] = Low	Decode SVC, SVD per Table 9
Bit[6:0] = High	Use the MTP Boot Register per Table 14

8.7.2 PSI[x]_L and TFN Control Bits

PSIo_L is Power State Indicator Level o. When this bit is asserted the IR35217 will drop to 1 phase. This will only occur if the output current is low enough (typically <20A) to enter PSIo, else the VR will remain in full phase operation.

PSI1_L is Power State Indicator Level 1. When this bit is asserted along with the PSIo_L bit, the IR35217 will enter diode emulation mode. This will only occur if the output current is low enough (typically <5A) to enter PSI1, else the VR will enter PSIo_L mode of operation.

TFN is an active high signal that allows the processor to control the telemetry functionality of the VR. If TFN=1, then the VR telemetry will be configured per Table 12.

Table 12

VDD1, VDD2 Domain Selector Bits	Meaning
0, 0	Telemetry in voltage mode Only
0, 1	Telemetry in voltage & current mode
1, 0	Telemetry is disabled
1, 1	Reserved

8.7.3 SVT Telemetry

The IR35217 has the ability to sample and report voltage and current for the VDD1 and VDD2 domains. The IR35217 reports this telemetry serially over the SVT wire which is clocked by the processor driven SVC. If in voltage only telemetry mode then the sampled voltage for VDD1 and VDD2 are sent together in every SVT telemetry packet at a rate of 20kHz. If in voltage and current mode then the sampled voltage and current for VDD1 is sent out in one SVT telemetry packet followed by the sampled voltage and current for VDD2 in the next SVT telemetry packet at a rate of 40kHz. The voltage and current are moving averages based on the filters and update rates specified in the Electrical Specification Table. The voltage is reported as a function of the Set VID minus lout times the Load Line Resistance. The current is reported as a percentage of the lcc_max register, where a value of FFh represents 100% and 00h represents 0% of the lcc_max setting. Resolution of the current reporting is 0.39% (1/256).

8.7.4 Load Line Slope Trim

The IR35217 has the ability for the processor to change the load line slope of each loop independently through the SVI2 bus while ENABLE and PWROK are asserted via the serial VID interface. The slope change applies to initial

Theory of Operation

load line slope as set by the external RCSP/RCSM resistor network. The load line slope can be disabled or adjusted by -40%, -20%, 0%, +20%, +40%, +60%, or +80%.

8.7.5 Offset Trim

The IR35217 has the ability for the processor to change the offset of each loop independently while ENABLE and PWROK are asserted via the serial VID interface. The offset can be left unchanged, disabled, or changed +25mV or -25mV.

8.7.6 Ispike/Dual OCP Support

The IR35217 has two current limit thresholds. One threshold is for short duration current spikes (Fast OCP). When this threshold, typically a percentage above the peak processor current, is exceeded the VR quickly shuts down. The other threshold, typically a percentage above the thermal design current (TDC), is heavily filtered (Slow OCP) and shuts down the VR when the average current exceeds it. To meet AMD specifications, exceeding both thresholds will assert the OCP_L (VR_HOT) pin and delay the over-current shut down by 1usec for FAST threshold and 2usec for the SLOW threshold, typically. Figure 16 shows the delay action of the OCP shutdown with the OCP_L (VR_HOT) and PWRGD pins.

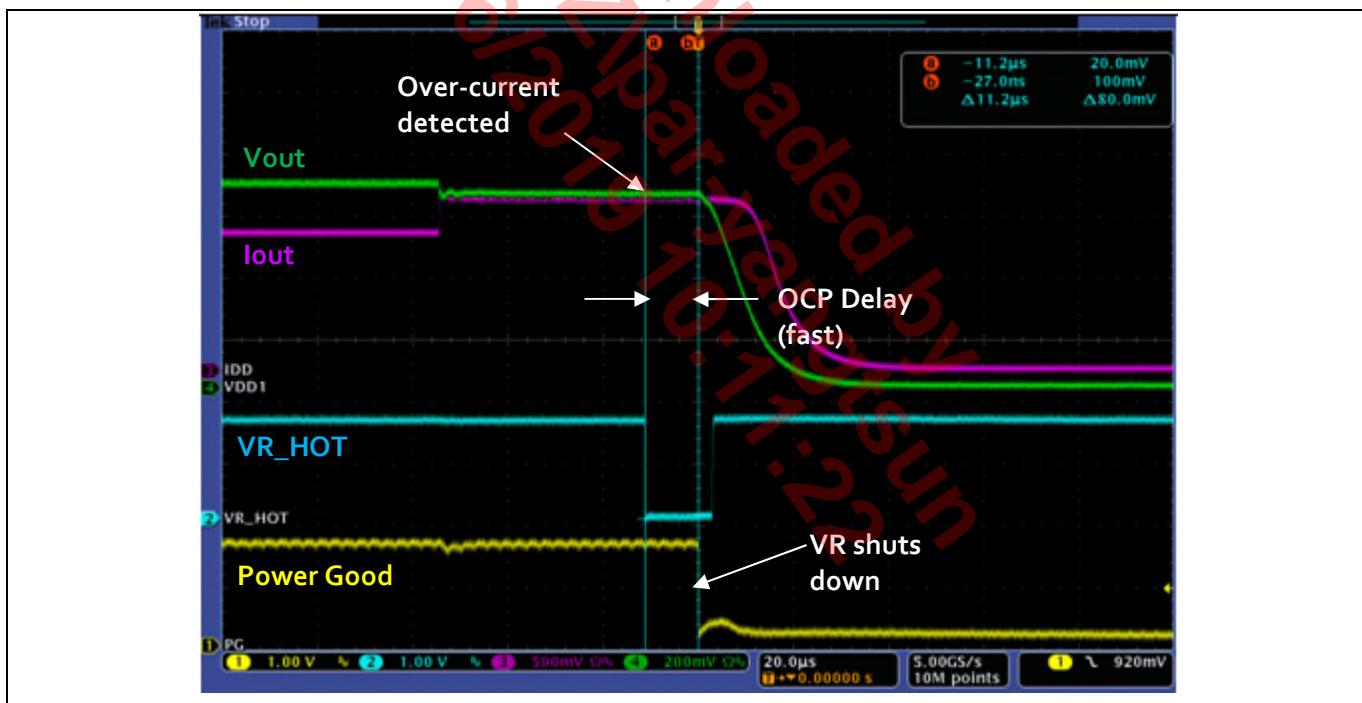


Figure 16 OCP_L (VR_HOT) assertion with OCP_spike (Fast) threshold. OCP delay action (11usec)

8.7.7 Thermal Based Protection

The IR35217 can also assert the PROC_HOT_L (VR_HOT) pin when the temperature of the VR exceeds a configurable temp_max threshold (typically 100°C). If the temperature continues to rise and exceeds a second configurable threshold (OTP_thresh) then the VR will shut down and latch off. The VR can only be restarted if ENABLE or VCC is cycled.

8.7.8 AMD SVI2 Address Programming

By default, loop 1 is addressed as the VDD1 rail and loop 2 is addressed as the VDD2 rail which is sufficient for most applications. The IR35217 however, can also be configured with a single bit change to swap this addressing scheme so that loop 1 can be addressed as the VDD2 rail and loop 2 can be addressed as the VDD1 rail. This is for application where the VDD2 requires more than two phases and VDD1 only requires two.

Downloaded by
IFXDMZpar-yangtsun
12/06/2019 10:11:22

Theory of Operation

Table 13 AMD SVI2 VID Table

VID (hex)	Voltage (V)								
0	1.55000	32	1.23750	64	0.92500	96	0.61250	C8	0.30000
1	1.54375	33	1.23125	65	0.91875	97	0.60625	C9	0.29375
2	1.53750	34	1.22500	66	0.91250	98	0.60000	CA	0.28750
3	1.53125	35	1.21875	67	0.90625	99	0.59375	CB	0.28125
4	1.52500	36	1.21250	68	0.90000	9A	0.58750	CC	0.27500
5	1.51875	37	1.20625	69	0.89375	9B	0.58125	CD	0.26875
6	1.51250	38	1.20000	6A	0.88750	9C	0.57500	CE	0.26250
7	1.50625	39	1.19375	6B	0.88125	9D	0.56875	CF	0.25625
8	1.50000	3A	1.18750	6C	0.87500	9E	0.56250	Do	0.25000
9	1.49375	3B	1.18125	6D	0.86875	9F	0.55625	D1	0.24375
A	1.48750	3C	1.17500	6E	0.86250	A0	0.55000	D2	0.23750
B	1.48125	3D	1.16875	6F	0.85625	A1	0.54375	D3	0.23125
C	1.47500	3E	1.16250	70	0.85000	A2	0.53750	D4	0.22500
D	1.46875	3F	1.15625	71	0.84375	A3	0.53125	D5	0.21875
E	1.46250	40	1.15000	72	0.83750	A4	0.52500	D6	0.21250
F	1.45625	41	1.14375	73	0.83125	A5	0.51875	D7	0.20625
10	1.45000	42	1.13750	74	0.82500	A6	0.51250	D8	0.20000
11	1.44375	43	1.13125	75	0.81875	A7	0.50625	D9	0.19375
12	1.43750	44	1.12500	76	0.81250	A8	0.50000	DA	0.18750
13	1.43125	45	1.11875	77	0.80625	A9	0.49375	DB	0.18125
14	1.42500	46	1.11250	78	0.80000	AA	0.48750	DC	0.17500
15	1.41875	47	1.10625	79	0.79375	AB	0.48125	DD	0.16875
16	1.41250	48	1.10000	7A	0.78750	AC	0.47500	DE	0.16250
17	1.40625	49	1.09375	7B	0.78125	AD	0.46875	DF	0.15625
18	1.40000	4A	1.08750	7C	0.77500	AE	0.46250	E0	0.15000
19	1.39375	4B	1.08125	7D	0.76875	AF	0.45625	E1	0.14375
1A	1.38750	4C	1.07500	7E	0.76250	Bo	0.45000	E2	0.13750
1B	1.38125	4D	1.06875	7F	0.75625	B1	0.44375	E3	0.13125
1C	1.37500	4E	1.06250	80	0.75000	B2	0.43750	E4	0.12500
1D	1.36875	4F	1.05625	81	0.74375	B3	0.43125	E5	0.11875
1E	1.36250	50	1.05000	82	0.73750	B4	0.42500	E6	0.11250
1F	1.35625	51	1.04375	83	0.73125	B5	0.41875	E7	0.10625
20	1.35000	52	1.03750	84	0.72500	B6	0.41250	E8	0.10000
21	1.34375	53	1.03125	85	0.71875	B7	0.40625	E9	0.09375
22	1.33750	54	1.02500	86	0.71250	B8	0.40000	EA	0.08750
23	1.33125	55	1.01875	87	0.70625	B9	0.39375	EB	0.08125
24	1.32500	56	1.01250	88	0.70000	BA	0.38750	EC	0.07500
25	1.31875	57	1.00625	89	0.69375	BB	0.38125	ED	0.06875
26	1.31250	58	1.00000	8A	0.68750	BC	0.37500	EE	0.06250
27	1.30625	59	0.99375	8B	0.68125	BD	0.36875	EF	0.05625
28	1.30000	5A	0.98750	8C	0.67500	BE	0.36250	F0	0.05000
29	1.29375	5B	0.98125	8D	0.66875	BF	0.35625	F1	0.04375
2A	1.28750	5C	0.97500	8E	0.66250	Co	0.35000	F2	0.03750
2B	1.28125	5D	0.96875	8F	0.65625	C1	0.34375	F3	0.03125
2C	1.27500	5E	0.96250	90	0.65000	C2	0.33750	F4	0.02500
2D	1.26875	5F	0.95625	91	0.64375	C3	0.33125	F5	0.01875
2E	1.26250	60	0.95000	92	0.63750	C4	0.32500	F6-FF	OFF
2F	1.25625	61	0.94375	93	0.63125	C5	0.31875		

Theory of Operation

VID (hex)	Voltage (V)								
30	1.25000	62	0.93750	94	0.62500	C6	0.31250		
31	1.24375	63	0.93125	95	0.61875	C7	0.30625		
0	1.55000	32	1.23750	64	0.92500	96	0.61250		
1	1.54375	33	1.23125	65	0.91875	97	0.60625		
2	1.53750	34	1.22500	66	0.91250	98	0.60000		
3	1.53125	35	1.21875	67	0.90625	99	0.59375		
4	1.52500	36	1.21250	68	0.90000	9A	0.58750		
5	1.51875	37	1.20625	69	0.89375	9B	0.58125		
6	1.51250	38	1.20000	6A	0.88750	9C	0.57500		
7	1.50625	39	1.19375	6B	0.88125	9D	0.56875		
8	1.50000	3A	1.18750	6C	0.87500	9E	0.56250		
9	1.49375	3B	1.18125	6D	0.86875	9F	0.55625		
A	1.48750	3C	1.17500	6E	0.86250	A0	0.55000		
B	1.48125	3D	1.16875	6F	0.85625	A1	0.54375		
C	1.47500	3E	1.16250	70	0.85000	A2	0.53750		
D	1.46875	3F	1.15625	71	0.84375	A3	0.53125		
E	1.46250	40	1.15000	72	0.83750	A4	0.52500		
F	1.45625	41	1.14375	73	0.83125	A5	0.51875		
10	1.45000	42	1.13750	74	0.82500	A6	0.51250		
11	1.44375	43	1.13125	75	0.81875	A7	0.50625		
12	1.43750	44	1.12500	76	0.81250	A8	0.50000		
13	1.43125	45	1.11875	77	0.80625	A9	0.49375		
14	1.42500	46	1.11250	78	0.80000	AA	0.48750		
15	1.41875	47	1.10625	79	0.79375	AB	0.48125		
16	1.41250	48	1.10000	7A	0.78750	AC	0.47500		
17	1.40625	49	1.09375	7B	0.78125	AD	0.46875		
18	1.40000	4A	1.08750	7C	0.77500	AE	0.46250		
19	1.39375	4B	1.08125	7D	0.76875	AF	0.45625		
1A	1.38750	4C	1.07500	7E	0.76250	Bo	0.45000		

Note: If `null_below_zoomV` is set to 1, VID settings below `zoomV` (grey area) are not allowed, except for oV (off).

Theory of Operation

Table 14 Boot Register Table

Reg Value (hex)	Voltage (V)						
80	1.5500	A0	1.1500	C0	0.7500	E0	0.3500
81	1.5375	A1	1.1375	C1	0.7375	E1	0.3375
82	1.5250	A2	1.1250	C2	0.7250	E2	0.3250
83	1.5125	A3	1.1125	C3	0.7125	E3	0.3125
84	1.5000	A4	1.1000	C4	0.7000	E4	0.3000
85	1.4875	A5	1.0875	C5	0.6875	E5	0.2875
86	1.4750	A6	1.0750	C6	0.6750	E6	0.2750
87	1.4625	A7	1.0625	C7	0.6625	E7	0.2625
88	1.4500	A8	1.0500	C8	0.6500	E8	0.2500
89	1.4375	A9	1.0375	C9	0.6375	E9	0.2375
8A	1.4250	AA	1.0250	CA	0.6250	EA	0.2250
8B	1.4125	AB	1.0125	CB	0.6125	EB	0.2125
8C	1.4000	AC	1.0000	CC	0.6000	EC	0.2000
8D	1.3875	AD	0.9875	CD	0.5875	ED	0.1875
8E	1.3750	AE	0.9750	CE	0.5750	EE	0.1750
8F	1.3625	AF	0.9625	CF	0.5625	EF	0.1625
90	1.3500	B0	0.9500	Do	0.5500	F0	0.1500
91	1.3375	B1	0.9375	D1	0.5375	F1	0.1375
92	1.3250	B2	0.9250	D2	0.5250	F2	0.1250
93	1.3125	B3	0.9125	D3	0.5125	F3	0.1125
94	1.3000	B4	0.9000	D4	0.5000	F4	0.1000
95	1.2875	B5	0.8875	D5	0.4875	F5	0.0875
96	1.2750	B6	0.8750	D6	0.4750	F6	0.0750
97	1.2625	B7	0.8625	D7	0.4625	F7	0.0625
98	1.2500	B8	0.8500	D8	0.4500	F8	0.0500
99	1.2375	B9	0.8375	D9	0.4375	F9	0.0375
9A	1.2250	BA	0.8250	DA	0.4250	FA	0.0250
9B	1.2125	BB	0.8125	DB	0.4125	FB	OFF
9C	1.2000	BC	0.8000	DC	0.4000	FC	OFF
9D	1.1875	BD	0.7875	DD	0.3875	FD	OFF
9E	1.1750	BE	0.7750	DE	0.3750	FE	OFF
9F	1.1625	BF	0.7625	DF	0.3625	FF	OFF

Note: If `null_below_zoomV` is set to 1, Vboot settings below zoomV (grey area) are not allowed, except for oV (off).

Theory of Operation

8.9 Intel Mode

8.9.1 Boot Voltage and Slew Rate

When the power-on sequence is initiated, and with VBOOT set to > 0V, the output voltage will ramp to its configured boot voltage and assert VR_READY. The slew rate to VBOOT is programmed per Table 16. If Vboot = 0V, the VR will stay at 0V and will not soft-start until the CPU issues a VID command to the loop.

The IR35217 Vboot voltage is fully programmable in MTP to the range specified in the Intel VID tables. Table 22 and Table 23 show the Intel VID tables for 5mV and 10mV VID steps respectively.

Table 15 Intel Boot Voltage

Loop	Boot Voltage
Loop1	Per Intel VR12 or VR12.5 VID Table
Loop2	Per Intel VR12 or VR12.5 VID Table

Table 16 Slew Rate – mV/usec

FAST Rate	$\frac{1}{2}$ Multiplier	$\frac{1}{4}$ Multiplier
10	5.0	2.50
15	7.5	3.75
20	10	5.00
25	12.5	6.25

8.9.2 Intel SVID Interface

The IR35217 implements a fully compliant Intel® VR12, VR12.5, IMVP8 Serial VID (REV 1.7 SVID specification) interface. This is a three-wire interface between an Intel® VR12, VR12.5, IMVP8 compliant processor and a VR that consists of clock, data and alert# signals.

The IR35217 architecture is based upon a digital core and hence lends itself very well to digital communications. As such, the IR35217 implements many of the required SVID registers and commands. The IR35217 also implements most of the optional commands and registers with very few exceptions. The Intel CPU is able to detect and recognize the extra functionality that the IR35217 provides and thus gives the Intel® VR 13/12/12.5/IMVP8 CPU unparalleled ability to monitor and optimize its power.

8.9.3 Intel SVID Addressing

The SVID address of the IR35217 defaults to 0. This address may be re-programmed in MTP and optionally, the IR35217 may be offset with an external resistor at the SV_ADDR pin.

Note that a 0.01μF capacitor must be placed across the resistor (Figure 18). An address lock function prevents accidental overwrites of the address.

Table 17 SVID Address Offset Options

SVID Address Offset Bit	SVID Offset
0	Disabled
1	Enabled

Theory of Operation

Table 18 SVID Address Offsets

SV_ADDR Resistor	SVID Address Offset
845 ohm	0
1.30 kohm	+1
1.78 kohm	+2
2.32 kohm	+3
2.87 kohm	+4
3.48 kohm	+5
4.12 kohm	+6
4.75 kohm	+7
5.49 kohm	+8
6.19 kohm	+9
6.98 kohm	+10
7.87 kohm	+11

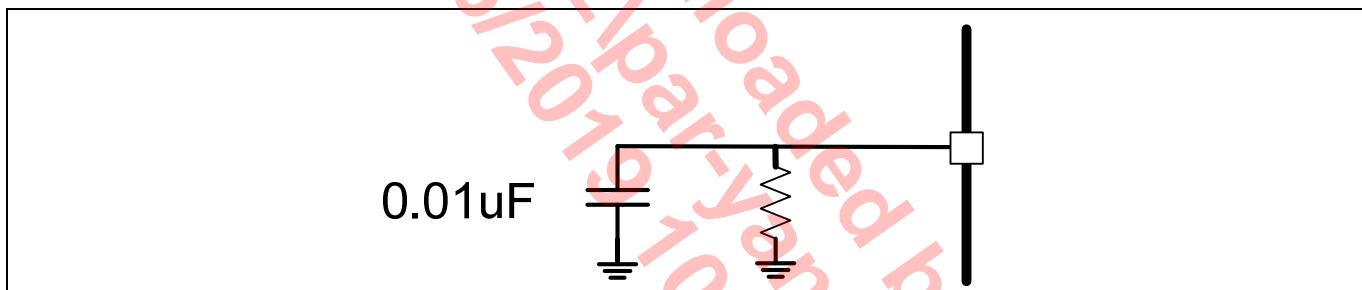


Figure 18 SV_ADDR Pin Components

8.9.4 Intel VID Offset

The output voltage can be offset instead of setting a manual VID value, according to Table 19. This is especially useful for memory applications where voltages higher than the standard VID table may be required.

Table 19 VID Offset

Parameter	Memory	Range	Step Size
Output Voltage	R/W	-128 to +127	1 VID Code

Note: Maximum allowable voltage is 3.04V (VR12.5)

The Vmax register must be set appropriately to allow the required output voltage offset.

8.9.5 Intel Reporting Offset

In addition to the mandatory features of the SVID bus, the IR35217 provides optional volatile SVID registers which allow the user to offset the reporting on the SVID interface as detailed in Table 20.

Theory of Operation

Table 20 SVID Offset Registers

Parameter	Memory	Range	Step Size
Output Current	NVM	-4A to +3.75A	0.25A
Temperature	R/W	-32°C to +31°C	1°C

8.9.6 All Call Support

All Call for each loop of IR35217 can be configured in following ways:

- oxoE and oxoF.
- oxoE only.
- oxoF only.
- No All Call

IR35217 can be configured to be used as VR for CPU which is All Call oxoF or Memory which is All Call oxoE.

8.9.7 VR12.5 Operation

VR12.5 mode is selectable via a MTP bit. The boot voltage in VR12.5 is also selectable and can be taken from the boot registers (Table 22 or Table 23)

8.9.8 IMVP8 Operation

IMVP8 mode is selectable via a MTP bit. The boot voltage in IMVP8 mode is configured in the boot register in 5mV steps compatible to VR12 mode VID table i.e. Table 22 or in 10mV steps compatible to VR12.5 mode VID table i.e. Table 23 . In IMVP8 mode, bit 3 of SVID register "Status 1" (1oh) is defined as "VID DAC high". This bit when set is an indicator to the CPU that the VR VID DAC is greater than 30mV above a new VID recently set by a SetVID command.

In IMVP8 mode, IR35217 does support PS4 command, however, it does not shut down the circuitry to reduce quiescent power consumption to <1mW. Thus, IR35217 is meant to be operated in IMVP8 mode for overclocking applications only where it is not expected for the VR to shut down its circuitry to reduce quiescent power consumption.

8.9.8.1 IVID Registers

IVID efficiency registers are a new addition to the family of SVID registers of IMVP8 specification. When sent an SVID command associated with IVID registers, IR35217 acknowledges the command and stores the received information into the IVID registers. However, IR35217 does not use the information received in IVID registers for any purpose. Instead, it uses the user set-up phase shed function to optimize the VR's efficiency across the entire operating current range.

8.9.9 SVID Registers

A list of all the SVID registers is given in Table 21. SVID registers supported by IR35217 in VR12.5 and IMVP8 mode conform to VR12.5 and IMVP8 specifications respectively.

Theory of Operation

Table 21 SVID Registers

Register Address	Name	Access	VR12.5 Mode	IMVP8
00	Vendor ID	RO	Supported	Supported
01	Product ID	RO	Supported	Supported
02	Product Revision	RO	Supported	Supported
03	Product Date Code	-	Not Supported	Not Supported
04	Lot Code	-	Not Supported	Not Supported
05	Protocol ID	RO	Supported	Supported
06	Capability	RO	Supported	Supported
07	Vendor-Timeout	RW	Supported	Supported
08	Vendor Use	RO	Supported	Supported
09	Vendor Use	-	Not Supported	Not Supported
0A	Vendor Use	-	Not Supported	Not Supported
0B	Vendor Use	-	Not Supported	Not Supported
0C	Vendor Use	-	Not Supported	Not Supported
0D	Vendor Use	RO	Supported, For Factor Use Only	Supported, For Factor Use Only
0E	Vendor Use	RW	Supported, For Factor Use Only	Supported, For Factor Use Only
0F	Vendor Use	RW	Supported, For Factor Use Only	Supported, For Factor Use Only
10	Status_1	RO	Supported	Supported
11	Status_2	RO	Supported	Supported
12	Temperature Zone	RO	Supported	Supported
13	Reserved	-	Not Supported	Not Supported
14	Reserved	-	Not Supported	Not Supported
15	Output Current	RO	Supported	Supported
16	Output Voltage	RO	Supported	Supported
17	VR Temperature	RO	Supported	Supported
18	Output Power	RO	Supported	Supported
19	Input Current	RO	Supported	Supported
1A	Input Voltage	RO	Supported	Supported
1B	Input Power	RO	Supported	Supported
1C	Status 2 Last Read	RO	Supported	Supported
1D	Future Command	-	Not Supported	Not Supported
1E	Future Command	-	Not Supported	Not Supported
1F	Future Command	-	Not Supported	Not Supported
20	Future Command	-	Not Supported	Not Supported
21	ICC Max	RO	Supported	Supported
22	Temp Max	RO	Supported	Supported
23	DC_LL	RO	Supported	Supported
24	SR_Fast	RO	Supported	Supported
25	SR_Slow	RO	Supported	Supported
26	Vboot	RO	Supported	Supported
27	VR Tolerance	-	Not Supported	Not Supported
28	Current-Offset	RO	Supported	Supported
29	Temperature Offset	RO	Supported	Supported
2A	Slow Slew Rate Select	RO	Not Supported	Supported
2B	PS4 Exit Latency	RO	Not Supported	Supported
2C	PS3 Exit Latency	RO	Not Supported	Supported
2D	Enable to Ready	RO	Not Supported	Supported
2E	Pin Max	RO	Not Supported	Supported
2F	Pin Alert Threshold	RW	Not Supported	Supported
30	V _{OUT} Max	RW	Supported	Supported

Theory of Operation

Register Address	Name	Access	VR12.5 Mode	IMVP8
31	VID Setting	RW	Supported	Supported
32	Pwr State	RW	Supported	Supported
33	Offset	RW	Supported	Supported
34	Multi VR Config	RW	Supported	Supported
35	Set RegADR	RW	Supported	Supported
36	Future Command	-	Not Supported	Not Supported
37	Future Command	-	Not Supported	Not Supported
38	Future Command	-	Not Supported	Not Supported
39	Future Command	-	Not Supported	Not Supported
3A	Work Point 0	RW	Not Supported	Not Supported
3B	Work Point 1	RW	Not Supported	Not Supported
3C	Work Point 2	RW	Not Supported	Not Supported
3D	Work Point 3	RW	Not Supported	Not Supported
3E	Work Point 4	RW	Not Supported	Not Supported
3F	Work Point 5	-	Not Supported	Not Supported
40	Work Point 6	-	Not Supported	Not Supported
41	Work Point 7	-	Not Supported	Not Supported
42	IVID1-VID	RW	Not Supported	Supported
43	IVID1-I	RW	Not Supported	Supported
44	IVID2-VID	RW	Not Supported	Supported
45	IVID2-I	RW	Not Supported	Supported
46	IVID3-VID	RW	Not Supported	Supported
47	IVID3-I	RW	Not Supported	Supported

Theory of Operation

Table 22 Intel VR12 VID Table – 5mV VID Steps

VID (hex)	Voltage (V)								
FF	1.52	C6	1.235	8D	0.95	54	0.665	1B	0.38
FE	1.515	C5	1.23	8C	0.945	53	0.66	1A	0.375
FD	1.51	C4	1.225	8B	0.94	52	0.655	19	0.37
FC	1.505	C3	1.22	8A	0.935	51	0.65	18	0.365
FB	1.5	C2	1.215	89	0.93	50	0.645	17	0.36
FA	1.495	C1	1.21	88	0.925	4F	0.64	16	0.355
F9	1.49	C0	1.205	87	0.92	4E	0.635	15	0.35
F8	1.485	BF	1.2	86	0.915	4D	0.63	14	0.345
F7	1.48	BE	1.195	85	0.91	4C	0.625	13	0.34
F6	1.475	BD	1.19	84	0.905	4B	0.62	12	0.335
F5	1.47	BC	1.185	83	0.9	4A	0.615	11	0.33
F4	1.465	BB	1.18	82	0.895	49	0.61	10	0.325
F3	1.46	BA	1.175	81	0.89	48	0.605	0F	0.32
F2	1.455	B9	1.17	80	0.885	47	0.6	0E	0.315
F1	1.45	B8	1.165	7F	0.88	46	0.595	0D	0.31
F0	1.445	B7	1.16	7E	0.875	45	0.59	0C	0.305
EF	1.44	B6	1.155	7D	0.87	44	0.585	0B	0.3
EE	1.435	B5	1.15	7C	0.865	43	0.58	0A	0.295
ED	1.43	B4	1.145	7B	0.86	42	0.575	09	0.29
EC	1.425	B3	1.14	7A	0.855	41	0.57	08	0.285
EB	1.42	B2	1.135	79	0.85	40	0.565	07	0.28
EA	1.415	B1	1.13	78	0.845	3F	0.56	06	0.275
E9	1.41	B0	1.125	77	0.84	3E	0.555	05	0.27
E8	1.405	AF	1.12	76	0.835	3D	0.55	04	0.265
E7	1.4	AE	1.115	75	0.83	3C	0.545	03	0.26
E6	1.395	AD	1.11	74	0.825	3B	0.54	02	0.255
E5	1.39	AC	1.105	73	0.82	3A	0.535	01	0.25
E4	1.385	AB	1.1	72	0.815	39	0.53	00	0
E3	1.38	AA	1.095	71	0.81	38	0.525		
E2	1.375	A9	1.09	70	0.805	37	0.52		
E1	1.37	A8	1.085	6F	0.8	36	0.515		
E0	1.365	A7	1.08	6E	0.795	35	0.51		
DF	1.36	A6	1.075	6D	0.79	34	0.505		
DE	1.355	A5	1.07	6C	0.785	33	0.5		
DD	1.35	A4	1.065	6B	0.78	32	0.495		
DC	1.345	A3	1.06	6A	0.775	31	0.49		
DB	1.34	A2	1.055	69	0.77	30	0.485		
DA	1.335	A1	1.05	68	0.765	2F	0.48		
D9	1.33	A0	1.045	67	0.76	2E	0.475		
D8	1.325	9F	1.04	66	0.755	2D	0.47		
D7	1.32	9E	1.035	65	0.75	2C	0.465		
D6	1.315	9D	1.03	64	0.745	2B	0.46		
D5	1.31	9C	1.025	63	0.74	2A	0.455		
D4	1.305	9B	1.02	62	0.735	29	0.45		
D3	1.3	9A	1.015	61	0.73	28	0.445		
D2	1.295	99	1.01	60	0.725	27	0.44		
D1	1.29	98	1.005	5F	0.72	26	0.435		
D0	1.285	97	1	5E	0.715	25	0.43		

Restricted

IR35217 Digital Multi-phase Controller

8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller



Theory of Operation

VID (hex)	Voltage (V)								
CF	1.28	96	0.995	5D	0.71	24	0.425		
CE	1.275	95	0.99	5C	0.705	23	0.42		
CD	1.27	94	0.985	5B	0.7	22	0.415		
CC	1.265	93	0.98	5A	0.695	21	0.41		
CB	1.26	92	0.975	59	0.69	20	0.405		
CA	1.255	91	0.97	58	0.685	1F	0.4		
C9	1.25	90	0.965	57	0.68	1E	0.395		
C8	1.245	8F	0.96	56	0.675	1D	0.39		
C7	1.24	8E	0.955	55	0.67	1C	0.385		

Downloaded by
IFXDMZpar-yangtsun
12/06/2019 10:11:22

Restricted**IR35217 Digital Multi-phase Controller****8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller****Theory of Operation****Table 23 Intel VR12.5 VID Table – 10mV VID Steps**

VID (hex)	Voltage (V)								
FF	3.04	C6	2.47	8D	1.9	54	1.33	1B	0.76
FE	3.03	C5	2.46	8C	1.89	53	1.32	1A	0.75
FD	3.02	C4	2.45	8B	1.88	52	1.31	19	0.74
FC	3.01	C3	2.44	8A	1.87	51	1.3	18	0.73
FB	3	C2	2.43	89	1.86	50	1.29	17	0.72
FA	2.99	C1	2.42	88	1.85	4F	1.28	16	0.71
F9	2.98	C0	2.41	87	1.84	4E	1.27	15	0.7
F8	2.97	BF	2.4	86	1.83	4D	1.26	14	0.69
F7	2.96	BE	2.39	85	1.82	4C	1.25	13	0.68
F6	2.95	BD	2.38	84	1.81	4B	1.24	12	0.67
F5	2.94	BC	2.37	83	1.8	4A	1.23	11	0.66
F4	2.93	BB	2.36	82	1.79	49	1.22	10	0.65
F3	2.92	BA	2.35	81	1.78	48	1.21	0F	0.64
F2	2.91	B9	2.34	80	1.77	47	1.2	0E	0.63
F1	2.9	B8	2.33	7F	1.76	46	1.19	0D	0.62
F0	2.89	B7	2.32	7E	1.75	45	1.18	0C	0.61
EF	2.88	B6	2.31	7D	1.74	44	1.17	0B	0.6
EE	2.87	B5	2.3	7C	1.73	43	1.16	0A	0.59
ED	2.86	B4	2.29	7B	1.72	42	1.15	09	0.58
EC	2.85	B3	2.28	7A	1.71	41	1.14	08	0.57
EB	2.84	B2	2.27	79	1.7	40	1.13	07	0.56
EA	2.83	B1	2.26	78	1.69	3F	1.12	06	0.55
E9	2.82	B0	2.25	77	1.68	3E	1.11	05	0.54
E8	2.81	AF	2.24	76	1.67	3D	1.1	04	0.53
E7	2.8	AE	2.23	75	1.66	3C	1.09	03	0.52
E6	2.79	AD	2.22	74	1.65	3B	1.08	02	0.51
E5	2.78	AC	2.21	73	1.64	3A	1.07	01	0.5
E4	2.77	AB	2.2	72	1.63	39	1.06	00	0
E3	2.76	AA	2.19	71	1.62	38	1.05		
E2	2.75	A9	2.18	70	1.61	37	1.04		
E1	2.74	A8	2.17	6F	1.6	36	1.03		
E0	2.73	A7	2.16	6E	1.59	35	1.02		
DF	2.72	A6	2.15	6D	1.58	34	1.01		
DE	2.71	A5	2.14	6C	1.57	33	1		
DD	2.7	A4	2.13	6B	1.56	32	0.99		
DC	2.69	A3	2.12	6A	1.55	31	0.98		
DB	2.68	A2	2.11	69	1.54	30	0.97		
DA	2.67	A1	2.1	68	1.53	2F	0.96		
D9	2.66	A0	2.09	67	1.52	2E	0.95		
D8	2.65	9F	2.08	66	1.51	2D	0.94		
D7	2.64	9E	2.07	65	1.5	2C	0.93		
D6	2.63	9D	2.06	64	1.49	2B	0.92		
D5	2.62	9C	2.05	63	1.48	2A	0.91		
D4	2.61	9B	2.04	62	1.47	29	0.9		
D3	2.6	9A	2.03	61	1.46	28	0.89		
D2	2.59	99	2.02	60	1.45	27	0.88		
D1	2.58	98	2.01	5F	1.44	26	0.87		
D0	2.57	97	2	5E	1.43	25	0.86		

Restricted

IR35217 Digital Multi-phase Controller

8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller



Theory of Operation

VID (hex)	Voltage (V)								
CF	2.56	96	1.99	5D	1.42	24	0.85		
CE	2.55	95	1.98	5C	1.41	23	0.84		
CD	2.54	94	1.97	5B	1.4	22	0.83		
CC	2.53	93	1.96	5A	1.39	21	0.82		
CB	2.52	92	1.95	59	1.38	20	0.81		
CA	2.51	91	1.94	58	1.37	1F	0.8		
C9	2.5	90	1.93	57	1.36	1E	0.79		
C8	2.49	8F	1.92	56	1.35	1D	0.78		
C7	2.48	8E	1.91	55	1.34	1C	0.77		

Downloaded by
IFXDMZpar-yangtsun
12/06/2019 10:11:22

Theory of Operation

8.10 Loop Start-up Sequence and Delay

IR35217 can be configured to enable both loops in following sequence:

- Both loops start together.
- Loop 2 follows Loop 1.
- Loop1 follows Loop 2.

If IR35217 is configured such that one loop follows the other, the delay between the two loops can be adjusted for following pre-defined intervals:

- 0 mS, 0.25 mS, 0.5 mS, 1 mS, 2.5 mS, 5 mS, 10 mS.

8.11 Memory (MPoL) Mode

In MPoL mode the IR35217 configures Loop 2 VID to 50% of Loop 1. Communication with and control of the IR35217 may occur either through the SVID interface when an Intel SVID Master is present, or alternatively through the I₂C/SMBus/PMBus interface for non-Intel applications.

The IR35217 follows startup and timing requirements as shown in Figure 19 and Table 24 . When the power-on sequence is initiated, and with VBOOT set to > 0V, both rails will ramp to their configured voltages and assert VR_READY_L1 and VR_READY_L2. The slew rates for both loops are set independently per Table 16 . If tracking is required during the slew, then care must be taken to ensure that the Loop 2 slew rate is set to ½ of the Loop 1 slew rate. Typical MPoL start-up and shut-down waveforms are shown in Figure 20 and Figure 21.

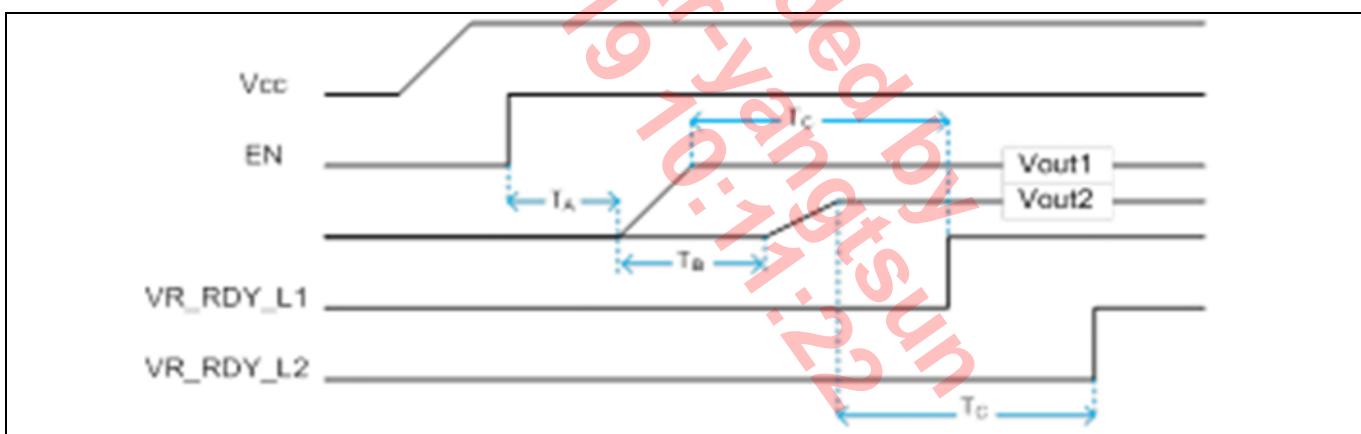


Figure 19 MPoL Startup

Table 24

Time	Description	Value
T _A	VR_EN to Loop 1 Start	3usec Typical
T _B	Loop2 Delay	0 to 678.3usec in 2.66usec Steps
T _C	Voltage ramp complete to VR_RDY_L1/L2	1usec Max

Theory of Operation



Figure 20 MPoL Tracking Startup



Figure 21 MPoL Tracking Shutdown

8.12 Phasing

The number of phases enabled on each loop of the IR35217 is shown in Table 25. The phase of the PWM outputs is automatically adjusted to optimize phase interleaving for minimum output ripple. Phase interleaving results in a ripple frequency that is the product of the switching frequency and the number of phases. A high ripple frequency results in reduced ripple voltage thereby minimizing the output filter capacitance requirements, resulting in significant total BOM cost reduction.

Theory of Operation

Phases are disabled based upon the configuration used. Disabled PWM outputs should be left floating. Typical PWM pulse phase relationships are shown in Table 26, and Figure 22.

Table 25 Loop Configuration

Configuration	Loop1	Loop2
8+0	8-phases	-
7+0	7-phases	-
6+0	6-phases	-
5+0	5-phases	-
4+0	4-phases	-
3+0	3-phases	-
2+0	2-phases	-
1+0	1-phase	-
7+1	7-phases	1-phase
6+1	6-phases	1-phase
5+1	5-phases	1-phase
4+1	4-phases	1-phase
3+1	3-phases	1-phase
2+1	2-phases	1-phase
1+1	1-phase	1-phase
6+2	6-phases	2-phase
5+2	5-phases	2-phase
4+2	4-phases	2-phase
3+2	3-phases	2-phase
2+2	2-phases	2-phase
1+2	1-phase	2-phase

Table 26 Phase Relationship

Phases	Phase Angle
1	-
2	180°
3	120°
4	90°
5	72°
6	60°
7	51.43°
8	45°

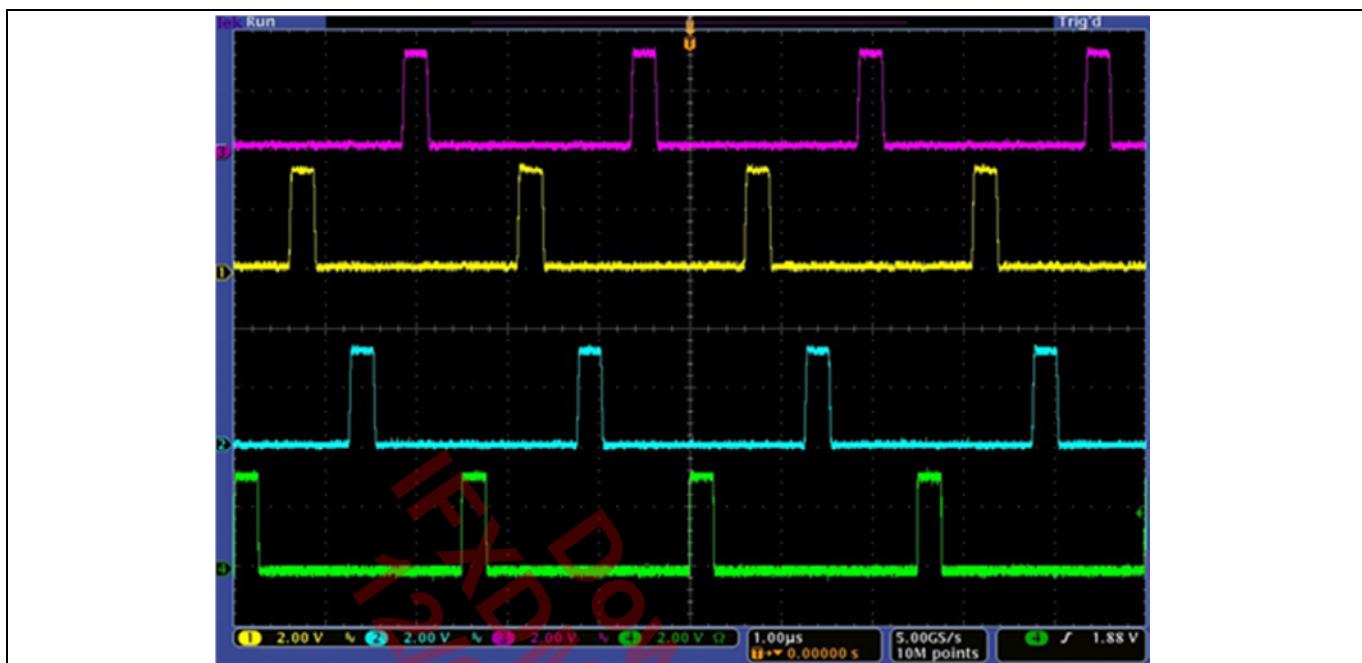


Figure 22 PWM Interleaving for 4 phases

8.13 Switching Frequency

The phase switching frequency (F_{sw}) of the IR35217 is set by a user configurable register. The switching frequency variation with register setting has been plotted in Figure 23.

The IR35217 oscillator is factory trimmed to guarantee high accuracy and very low jitter compared to analog controllers.

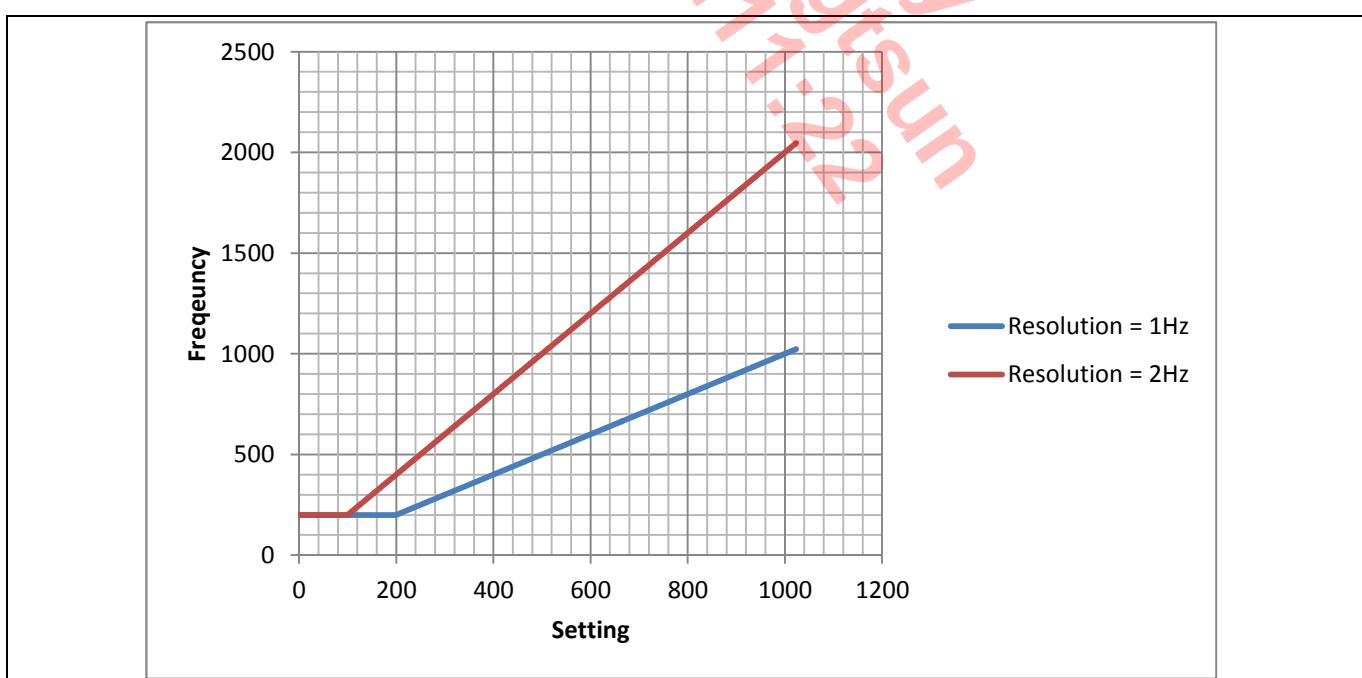


Figure 23 Switching Frequency versus register setting

8.14 MOSFET Driver and Power Stage Selection

The PWM signals from the active phases of the IR35217 are designed to operate with industry standard tri-state type drivers or PowIRstage devices. The logic operation for these types of tri-state drivers is depicted in Figure 24.

When in tri-state, the IR35217 floats the outputs so that the voltage level is determined by an external voltage divider which is typically inside the MOSFET driver.

Note that the PWM outputs are tri-stated whenever the controller is disabled (EN = low), the shut-down ramp has completed or prior to soft-start.

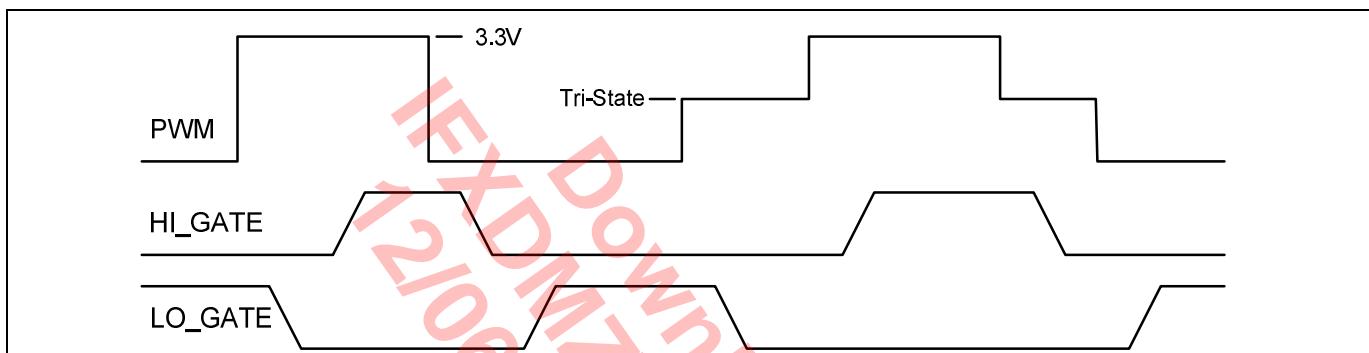


Figure 24 3.3V Tri-state Driver Logic Levels

8.15 Output Voltage Differential Sensing

The IR35217's VSEN and VRTN pins for each loop are connected to the load sense pins of the output voltage to provide true differential remote voltage sensing with high common-mode rejection. Each loop has a high bandwidth error amplifier that generates the error voltage between this remote sense voltage and the target voltage. The error voltage is digitized by a fast, high-precision ADC.

As shown in Figure 25, the VSEN and VRTN inputs have a $20\text{k}\Omega$ pull-up to an internal 1V rail. This causes some current flow in the VSEN and VRTN lines. To minimize the offset created by this current flow, the external series impedance on these lines needs to be kept to a minimum.

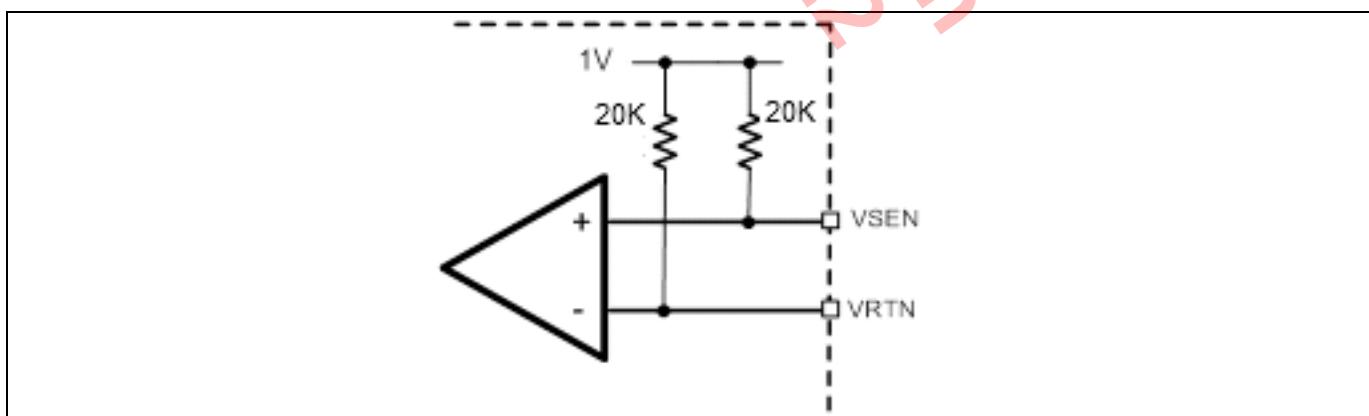


Figure 25 Output Voltage Sensing Impedance

Theory of Operation

8.16 Input Current Sensing

The IR35217 supports a proprietary “lossless input current sensing” scheme. The controller can accurately estimate the actual input current on a per loop basis, as it knows the value of output current, output voltage, and pulse width of each phase. This eliminates the need for a dedicated IINSEN pin and also simplifies the board layout by eliminating the external amplifier and shunt.

In addition to this, the IR35217 also supports input current sensing through a dedicated IINSEN pin. A precision current sense resistor is connected in series with the input path as shown in Figure 26. The voltage across the current sense resistor is differentially amplified by a current sense amplifier and fed to the IINSEN pin of IR35217. An internal ADC converts the sensed voltage into its digital equivalent. The IINSEN pin’s input voltage range is 0 to 1.25V.

$$I_{IN(V)} = I_{in} \times R_{SENSE} \times CSA_GAIN$$

Here IR35217 offers four full-scale ranges for input current depending upon the level of input to ADC.

1. 20mV/A => 0 – 62.5A
2. 40mV/A => 0 – 31.25A
3. 50mV/A => 0 – 25A
4. 100mV/A => 0 – 12.5A

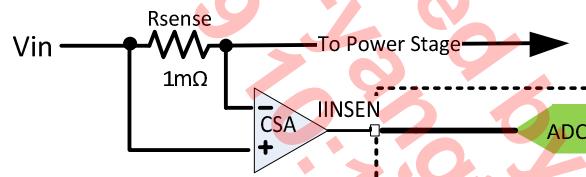


Figure 26 Input Current Sense

8.17 Output Current Sensing

The IR35217 supports individual output current sensing for each phase to support accurate Adaptive Voltage Positioning (AVP), current balancing, and over-current protection. The IR35217 supports both lossless inductor DCR and RDS (ON) current sensing techniques.

For DCR sensing, a suitable resistor-capacitor network of Rsen and Csen is connected across the inductor in each phase as shown in Figure 27 below. The time constant of this RC network should be set to equal the inductor time constant (L/DCR) such that the voltage across the capacitor Csen is equal to the voltage across the inductor DCR.

The recommended value for Csen is 220nF, with an NPO type dielectric. To prevent undershooting of the output voltage during load transients, the Rsen resistor can be calculated by:

Theory of Operation

$$R_{sen} = \frac{1.05 * L_{out}}{C_{sen} * DCR}$$

Note: Use thick film resistor (0603) for Rsen

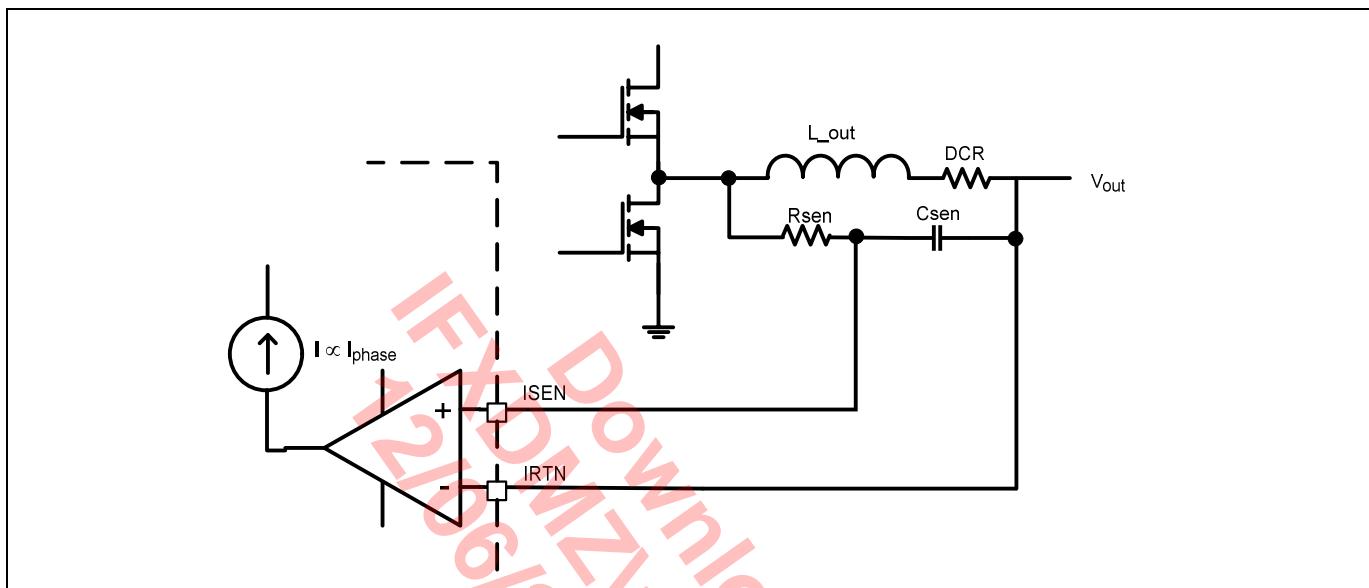


Figure 27 DCR Current Sense

Additionally, the current sense inputs to the IR35217 can also be directly fed the current information from a PowIRstage having RDS (ON) sensing capability, thereby eliminating the need for the R-C sense components, RSEN and CSEN as shown in Figure 28.

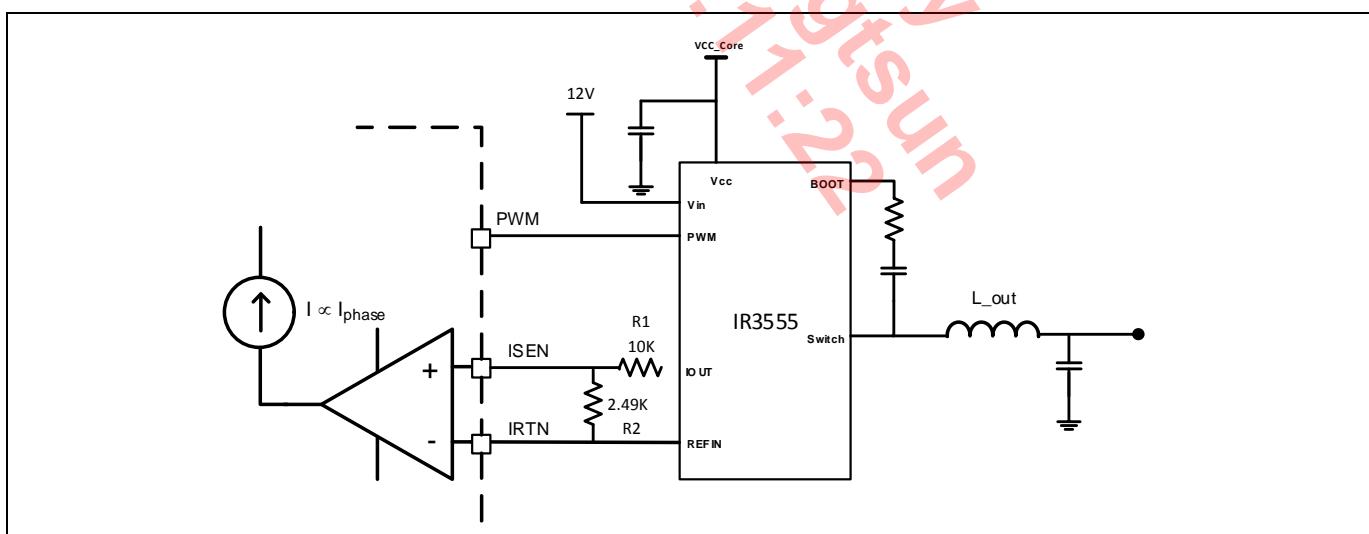


Figure 28 Rds(on) Current Sense

8.17.1 Output Current Balance & Offset

The IR35217 provides accurate digital phase current balancing in any phase configuration. Current balancing equalizes the current across all the phases. This improves efficiency, prevents hotspots and reduces the possibility of inductor saturation.

Theory of Operation

The sensed currents for each phase are converted to a voltage and are multiplexed into the monitoring ADC. The digitized currents are low-pass filtered and passed through a proprietary current balance algorithm to enable the equalization of the phase currents as shown in Figure 29.

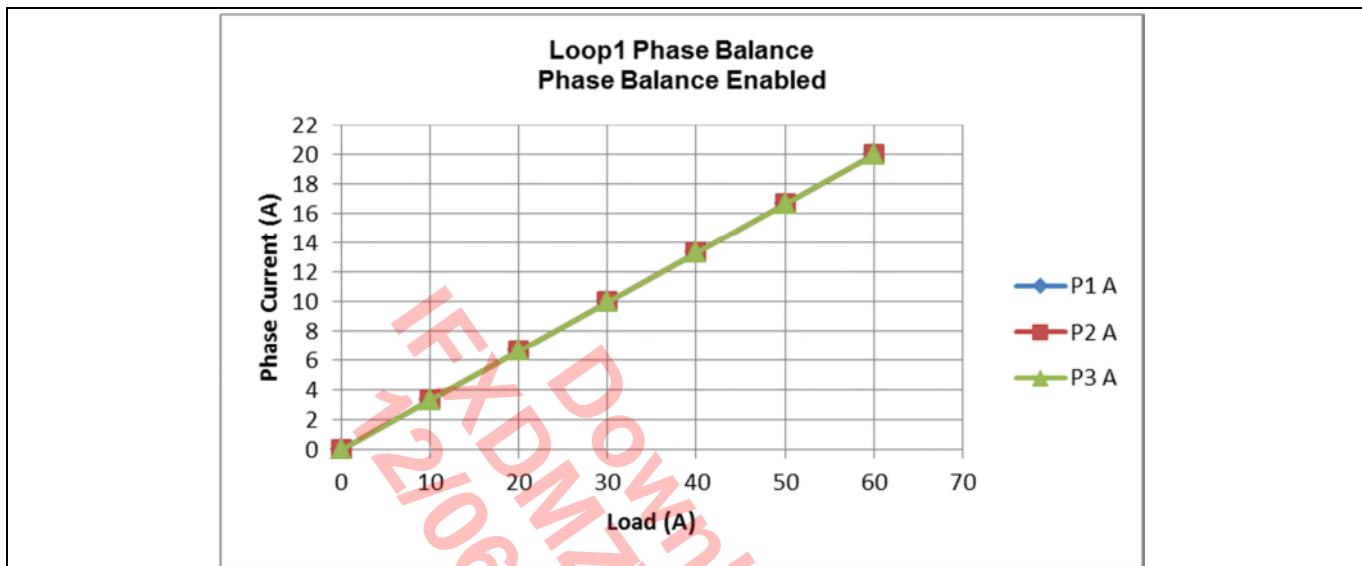


Figure 29 Typical Phase Current Balance

The proprietary high-speed active phase current balance operates during load transients to eliminate current imbalance that can result from a load current oscillating near the switching frequency. The order in which the phases output PWM pulses is decided based on an adaptive High Speed Phase Balance (HSPB) to ensure that the phases remain balanced during high frequency load transients.

In addition, the IR35217 allows the user to offset phase currents to optimize the thermal solution. Figure 30 shows Phase 1 current gain offset to a value of 6. This scales the current in phase 1 to have approximately 30% more current than the other phases.

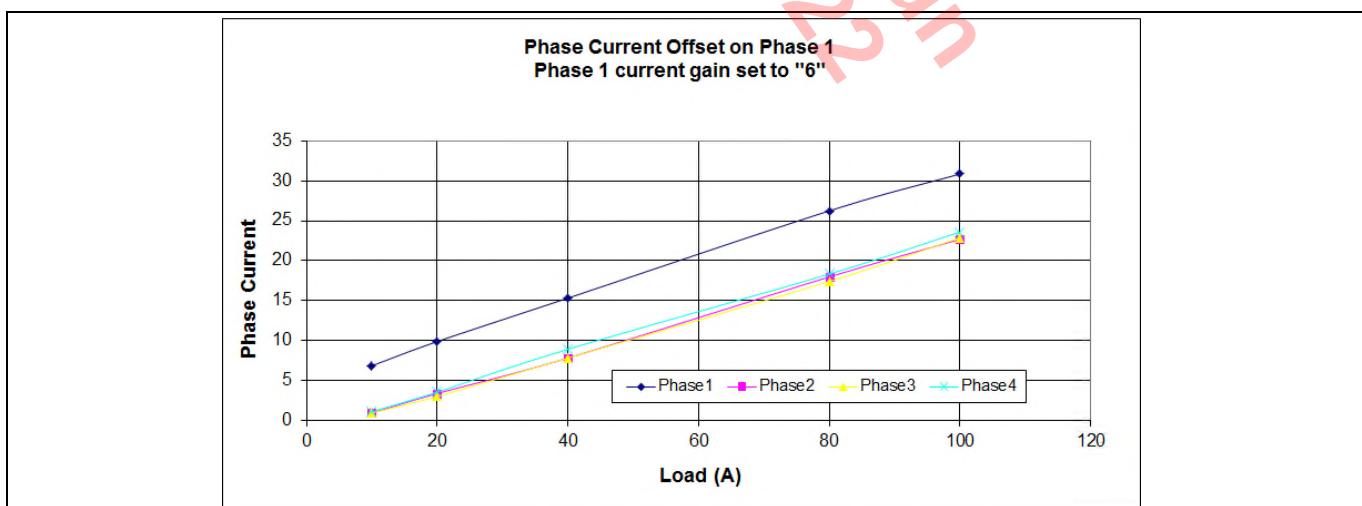


Figure 30 Phase 1 Current Offset

8.17.2 Output Current Calibration

For optimizing the current measurement accuracy of a design, the IR35217 contains a register in MTP, which can store a user-programmed per phase Current Offset, to zero out the no-load current reading. Refer to Table 45 for output current calibration registers.

8.18 Load Line for Active Voltage Positioning

The IR35217 enables the implementation of an accurate, temperature compensated load line.

The nominal load line is set by an external resistor RCS, as shown in Figure 30. This load line value also needs to be stored in MTP. The stored values for load line, scaling and gain provide the scaling factors required for digital computation of the total current, in order to determine the true current, OCP threshold, and output voltage telemetry registers.

For each loop, the sensed current from all the active phases is summed and applied differentially to a resistor network across the RSCP and RCSM pins as shown in Figure 30. This generates a precise proportional voltage, which is summed with the sensed output voltage and VID DAC reference to form the error voltage.

IR35217 supports two types of current sense techniques.

- DCR Current Sensing
- Rds(on) Current Sensing

The load line range for IR35217 is shown in Table 27

Table 27 Load Line Settings

	Loop 1	Loop 2
Minimum	0 mΩ	0 mΩ
Maximum	6.375 mΩ	12.75 mΩ
Resolution	0.025 mΩ	0.050 mΩ

8.18.1 DCR Current Sense

DCR current sense technique measures the voltage drop across the DCR of the inductor as shown in Figure 27. The IR35217 creates a load line for Active Voltage Positioning using the network shown in Figure 31. The DCR of the inductor has a positive temperature coefficient of resistance. Hence, to compensate for the increase in DCR with respect to temperature a thermistor, R_{Th} , having a negative temperature coefficient of resistance is also part of the network. For proper load line temperature compensation, the thermistor is placed near the phase one inductor to accurately sense the inductor temperature.

The resistor R_{CS} is calculated using the following procedure:

Theory of Operation

- Calculate the $R_{CS_{effective}}$ or the total effective parallel resistance across the RSCP and RCSM pins as defined by:

$$R_{CS_{effective}} = 8 \times R_{ISEN} \times \frac{RLL}{DCR}$$

Where, RLL is the desired load line, DCR is DC resistance of the phase inductor, and R_{ISEN} is the internal series resistor = 1000 ohm.

- Select a suitable NTC thermistor, R_{Th} . This is typically selected to have the lowest thermal coefficient and tightest tolerance in a standard available package. A typical NTC used in these applications is a 10kΩ, 1% tolerance device. Recommended thermistors are shown in Table 28 .

Table 28 10 kohm 1% NTC Thermister

Manufacturer	Manufacturer P/N
Murata	NCP18XH103F03RB
Panasonic	ERTJ1VG103FA
TDK	NTCG163JF103F

- Calculate R_{CS} using the following equation:

$$R_{CS} = \frac{1}{\frac{1}{R_{CS_{effective}}} - 2 \times \frac{1}{R_{series}} \times \frac{1}{R_{Th}}}$$

R_{series} is selected to achieve minimum load line error over temperature. The IR PowIRCenter GUI provides a graphical tool that allows the user to easily calculate the resistor values for minimum error.

The capacitor C_{CS} is defined by the following equation:

$$C_{CS} = \frac{1}{2\pi \times R_{CS_{effective}} \times f_{AVP}}$$

Where, f_{AVP} is the user selectable current sense AVP bandwidth. The recommended bandwidth is typically in the range of 200kHz to 300kHz.

The voltage from the RCSM to RCSP terminals (V_{avp}) is equal to $2 \times I_{OUT} \times \text{Load Line (R}_{LL}\text{)}$

Theory of Operation

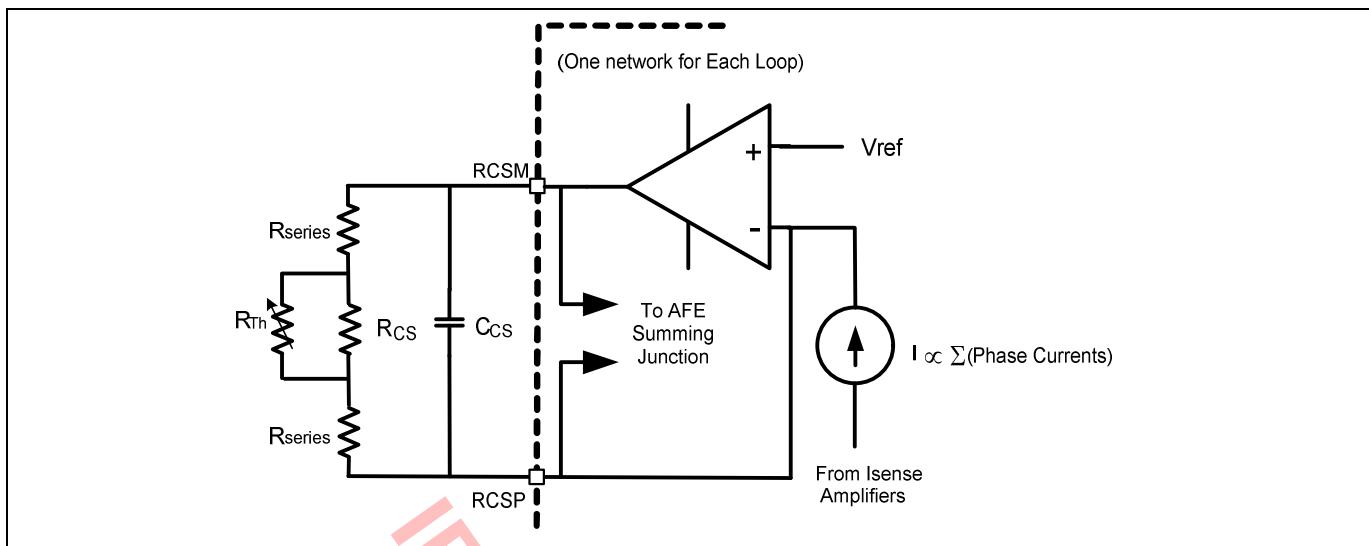


Figure 31 Load Line & Thermal Compensation for DCR Current Sense

8.18.2 Rds(on) Current Sense

R35217 reads the current value from individual power stages as shown in Figure 28. The power stage measures the output current by sensing the voltage drop across lower side MOSFET. The current sensed by the power stage is thermally compensated hence there is no need of an external thermistor for temperature compensation. Thus, Rds (on) current sense reduces the component count required for loadline measurement as shown in Figure 32.

The resistor Rcs for Rds(on) current sense is calculated by using the following formula:

$$R_{CS} = 8 \times R_{ISEN} \times \frac{R_{LL}}{I_{RdsonScale} \times \text{Divider Ratio}}$$

Where $I_{RDS\ ON}$ Scale = current scale of Power Stage in V/A, and the Divider Ratio is calculated as:

$$\text{Divider Ratio} = \frac{R2}{R1 + R2}$$

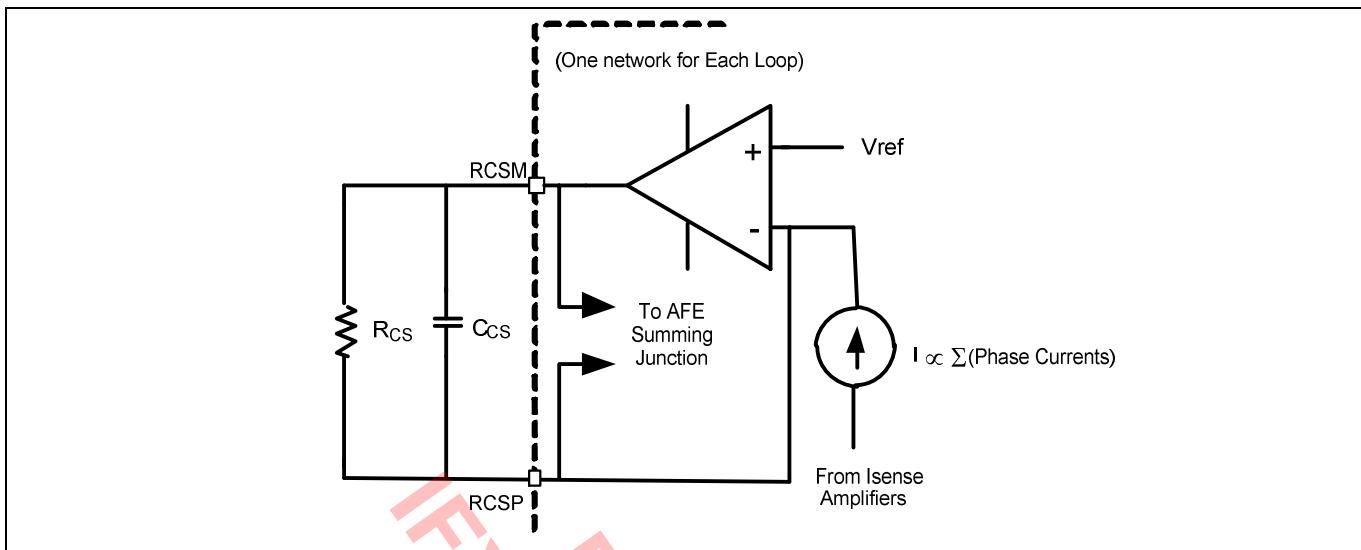
Refer Figure 28.

The capacitor Ccs is defined by the following equation:

$$C_{CS} = \frac{1}{2\pi \times R_{CS} \times f_{AVP}}$$

Where, f_{AVP} is the user selectable current sense AVP bandwidth. The recommended bandwidth is typically in the range of 200kHz to 300kHz.

Theory of Operation

Figure 32 Load Line for $R_{ds(on)}$ Current Sense

8.18.3 Setting a $0\text{m}\Omega$ Load Line

The load line is turned off by setting the Loadline Enable bit low. This is a separate bit from the load line settings for each loop.

Even though the load line is disabled digitally, the load-line resistors and scaling registers should be set such that the load line is at least 3 times the value of low ohmic DCR inductors ($<0.5\text{m}\Omega$) or equal to the DCR value for high ohmic inductors ($>0.5\text{m}\Omega$). For example, if the inductor(s) DCR is $0.3\text{m}\Omega$, a nominal $0.9\text{ m}\Omega$ load line should be set. For accurate current measurement and OCP threshold with the load line disabled, the output current gain and scaling registers must be set to the same value as the load line set with the external resistor network. With load line disabled, the thermistor and Ccs capacitor must still be installed to insure accuracy of the current measurement.

8.19 Digital Feedback Loop and PWM Control

The IR35217 uses a digital feedback loop to minimize the requirement for output decoupling, and to maintain a tightly regulated output voltage. The error between the target and the output voltage is digitized and passed through a low pass filter. This filtered signal is then passed through an initial single-pole filter stage, followed by the PID (Proportional Integral Derivative) compensator, and an additional single-pole filter stage. The loop compensation parameters K_p (proportional coefficient), K_i (integral coefficient), and K_d (derivative coefficient), as well as the low-pass filter pole locations are user-configurable to optimize the VR design for the chosen external components.

The adaptive PID control used in IR35217 intelligently scales the coefficients and the low-pass filters in real-time, to maintain optimum stability, as phases are added and dropped dynamically in the application. This auto-scaling feature significantly reduces design time by virtue of having to design the PID coefficients design only for one loop combination (Figure 33).

Theory of Operation

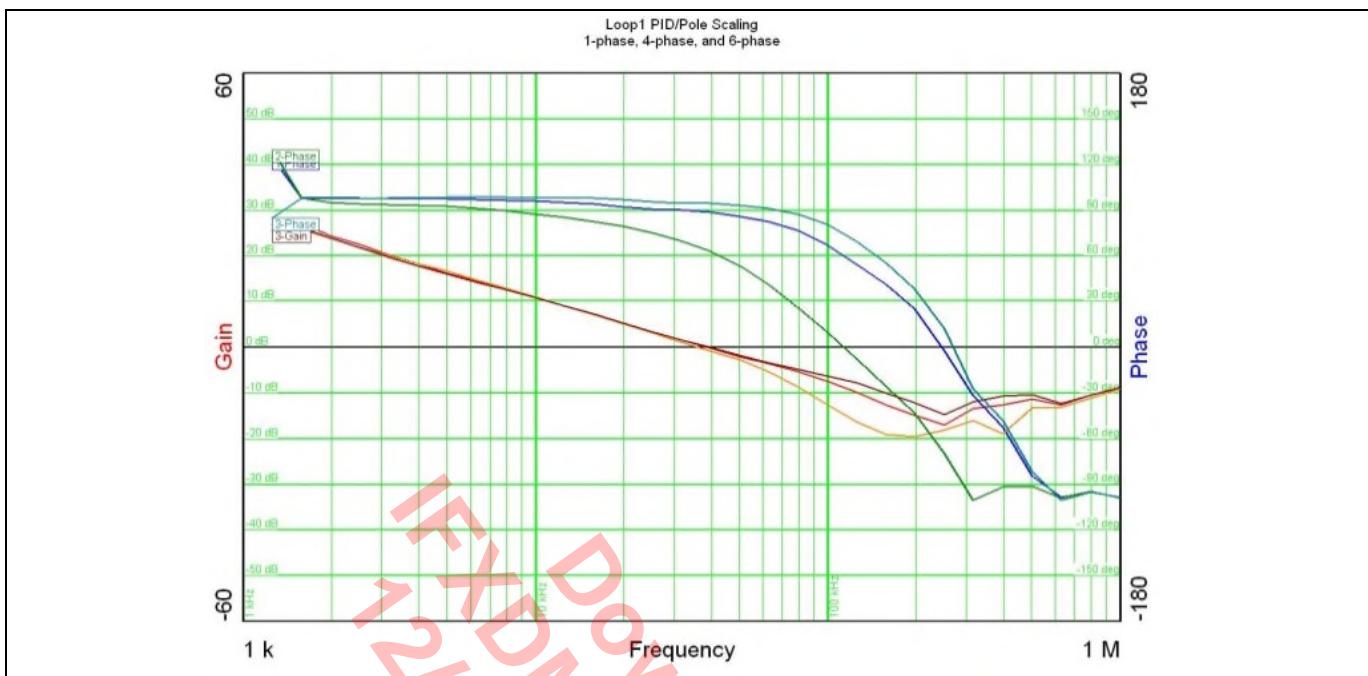


Figure 33 Stability With Phase Add/Drop

Each of the proportional, integral and derivative terms is a 6-bit value stored in MTP that is decoded by the IC's digital core. This allows the designer to set the converter bandwidth and phase margin to the desired values.

The compensator's transfer function is defined as:

$$(K_p + \frac{K_i}{s} + K_d \cdot s) \cdot \left(\frac{1}{1 + \frac{s}{\omega_{p1}}} \right) \cdot \left(\frac{1}{1 + \frac{s}{\omega_{p2}}} \right)$$

Where ω_{p1} and ω_{p2} are the two configurable poles, typically positioned to filter noise, and to roll off the high-frequency gain that the K_d term creates.

The outputs of the compensator and the phase current balance block are fed into a digital PFM pulse generator to generate the PFM pulses for the active phases. The digital PFM generator has a native time resolution of 1.3ns which is combined with digital dithering to provide an effective PFM resolution of 163ps. This ensures that there is no limit cycling when operating at the highest switching frequency.

8.20 Adaptive Transient Algorithm (ATA)

The IR35217 Adaptive Transient Algorithm (ATA) is a high speed non-linear control technique that allows compliance with CPU voltage transient load regulation requirements, with minimum output bulk capacitance for reduced system cost.

A high-speed digitizer measures both the magnitude and slope of the error signal to predict the load current transient. This prediction is used to control the phase relationships of the PWM pulses. The ATA is a wide-band non-linear control loop which can react faster to load transients and ensures that the output voltage is within the regulation limits even during fast dynamic load and voltage change events. Figure 34 illustrates the transient performance improvement provided by the ATA showing the clear reduction in undershoot and overshoot. Figure 35 is a zoomed-in scope capture of a load step, illustrating the fast reaction time of the ATA, and how the algorithm changes the pulse phase relationships. IR35217 provides the option to enable or disable this feature, using a digitally programmable bit.

Theory of Operation

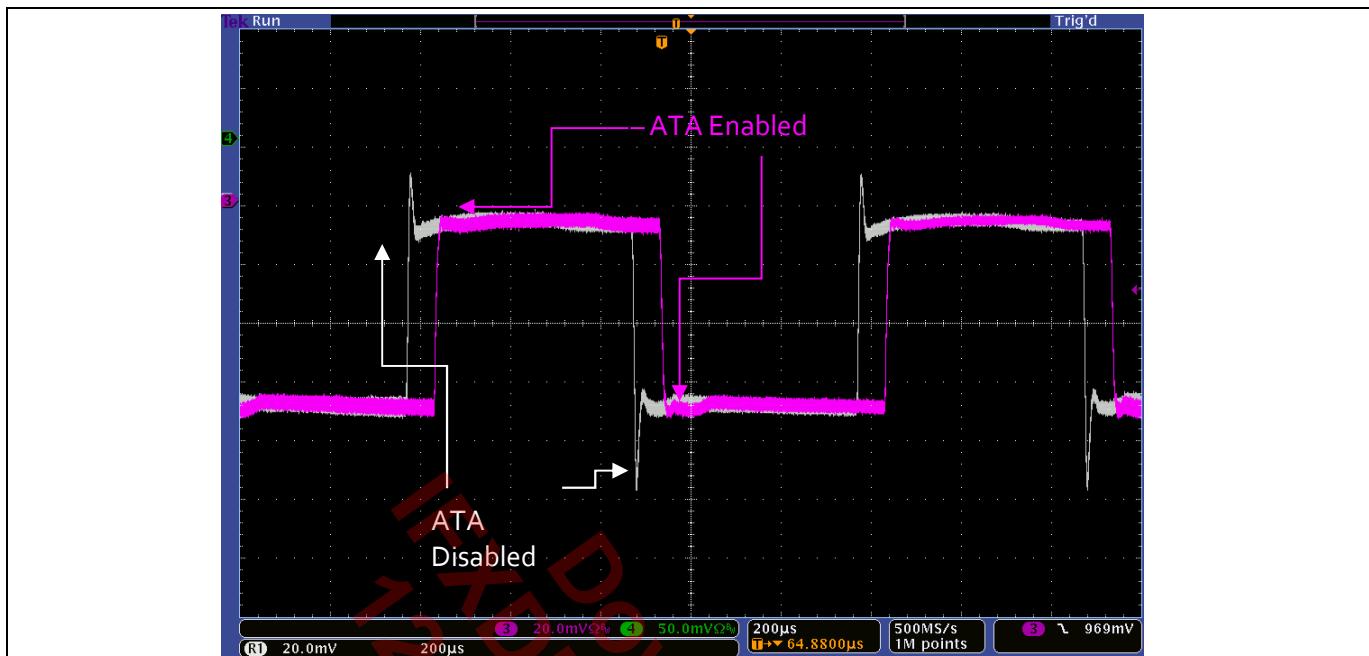


Figure 34 ATA Enable/Disable Comparison



Figure 35 ATA Feature – Zoomed In

In addition, during load release events, the ATA may also be programmed to turn off the low-side MOSFETS instead of leaving them on. This forces the load current to flow through the larger FET body diode, and helps to reduce the overshoot created during a load release, as shown in Figure 36 below.

Theory of Operation

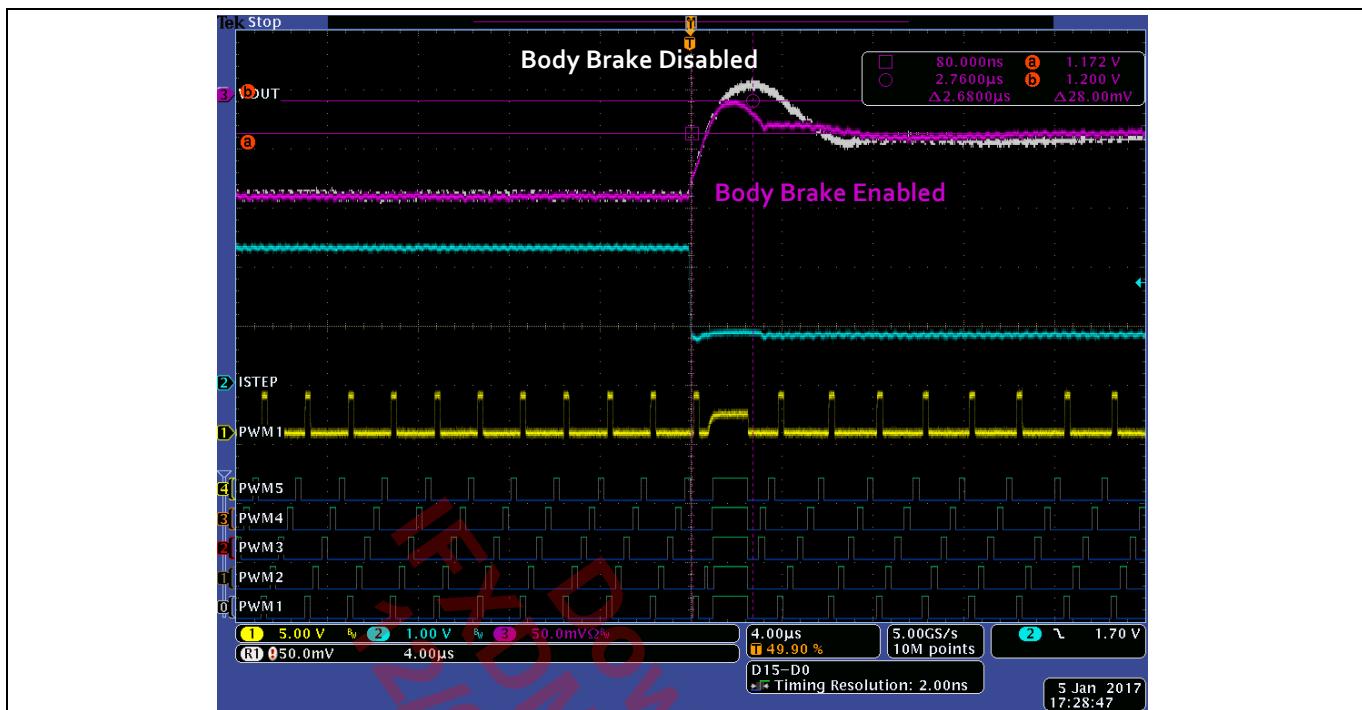


Figure 36 Body Braking during Load Release

8.21 Dynamic Output Voltage Control

8.21.1 Slew Rate

The IR35217 provides the VR designer 16 fast slew rates each of which can be further configured to 4 different slow slew rates by selecting a slew rate setting as shown in Table 29. These slew rates can be further reduced by 1/2, 1/4, and 1/8 by a register setting.

Table 29 Slew Rates – mV/usec

Fast Rate	$\frac{1}{2}$ Factor	$\frac{1}{4}$ Factor	$\frac{1}{8}$ Factor	$\frac{1}{16}$ Factor
10	5.0	2.50	1.25	0.625
15	7.5	3.75	1.875	0.94
20	10	5.00	2.50	1.25
25	12.5	6.25	3.125	1.56
30	15	7.5	3.75	1.88
35	17.5	8.75	4.375	2.19
40	20	10	5.0	2.5
45	22.5	11.25	5.625	2.81
50	25	12.5	6.25	3.125
55	27.5	13.75	6.875	3.4375
60	30	15	7.5	3.75
65	32.5	16.25	8.125	4.0625
70	35	17.5	8.75	4.375
80	40	20	10	5
85	42.5	21.25	10.625	5.3125
95	47.5	23.75	11.875	5.9375

Theory of Operation

Note: The maximum DVID rate is limited by the inductor current available to charge the output capacitors. High DVID rates may not be possible if the output capacitor and inductor combination does not allow the output voltage to change at the selected rate.

8.21.2 Dynamic Output Voltage Compensation

The IR35217 can compensate for the error produced by the current feedback in a system with AVP (Active Voltage Positioning) when the output voltage is ramping to a higher voltage. An output capacitance term is provided in the MTP registers to help model the effects of variation in output voltage during a voltage ramp, due to the inrush current into the output bulk capacitors. Once properly modeled, the output voltage will follow the DAC more closely during a positive dynamic output voltage change, and provide better dynamic response. Figure 31 shows the effects that Dynamic Output Voltage Compensation has on the output voltage.

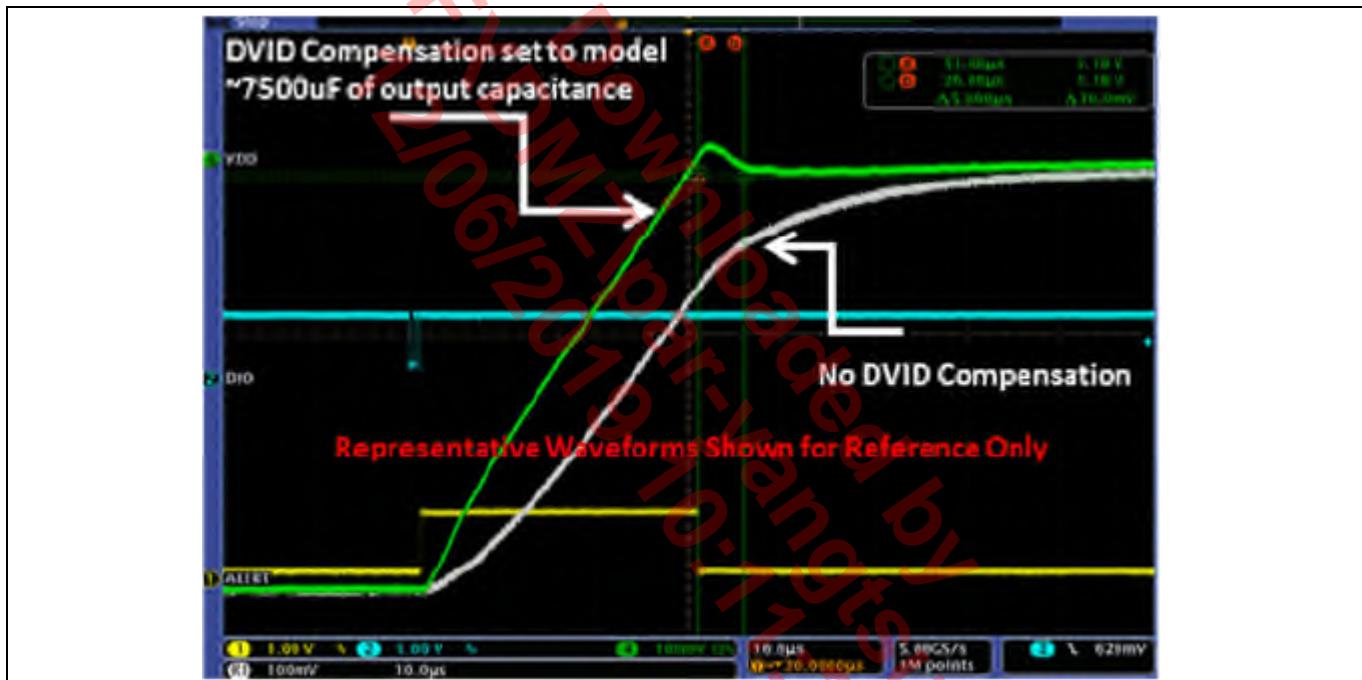


Figure 37 Dynamic Output Voltage Compensation

8.22 Efficiency Shaping

In addition to CPU-specified Power States, the IR35217 features Efficiency Shaping Technology that enables VR designers to cost-effectively maximize system efficiency. Efficiency Shaping Technology consists of Dynamic Phase Control to achieve the best VR efficiency at a given cost point.

8.22.1 Power States

The IR35217 uses Power States to set the power-savings mode. These are summarized in Table 30.

Table 30 Power States

Power State	Mode	Recommended Current
PS0	Full Power	Maximum
PS1	Light Load 1-2Φ	<20A

Theory of Operation

Power State	Mode	Recommended Current
PS2	1Φ Active Discontinuous (Diode Emulation)	<5A
PS3	1Φ Passive Discontinuous (Diode Emulation)	<1A
PS4	Output Voltage DVID or Decay Down to zero depending upon configuration in “ps4_dvid_or_decay” register. PWM signals of all phases are tristated.	Near OFF

The Power States may be commanded through I₂C/PMBus, the SVID interface, or the IR35217 can autonomously step through the Power States based upon the regulator conditions as summarized in Table 31. PS4 can only be commanded with an SVID command.

Table 31 Power State Entry/Exit

Power State	Command Mode	Auto Mode
PS1 Entry	a) Command	n/a if Phase Shed enabled
PS1 Exit	a) Command to PS0 b) During DVID event c) Current limit to PS0	n/a if Phase Shed enabled
PS2 Entry	a) Command	Current level in 1Φ
PS2 Exit	a) Command to PS1/0 b) During DVID event c) Current limit to PS0	F _{sw} > F _{sw_desired} to PS0, DVID to PS0, Current limit to PS0

8.22.2 Dynamic Phase Control (DPC) in PSo

IR35217 optionally supports the ability to autonomously adjust the number of phases with load current, thus optimizing efficiency over a wide range of loads. The output current level at which a phase is added can be programmed individually for each phase for optimum results (Table 32).

Table 32 DPC Thresholds

Register (2A steps)	Function
Phase1_thresh	2Φ when I _{out} > Phase1_thresh
Phase2_delta	3Φ when I _{out} > Phase1_thresh + Phase2_delta
Phase3_delta	4Φ when I _{out} > Phase1_thresh + Phase2_delta + Phase3_delta
Phase4_delta	5Φ when I _{out} > Phase1_thresh + Phase2_delta + Phase3_delta + Phase4_delta
Phase5_delta	6Φ when I _{out} > Phase1_thresh + Phase2_delta + Phase3_delta + Phase4_delta + Phase5_delta
Phase6_delta	7Φ or 8Φ when I _{out} > Phase1_thresh + Phase2_delta + Phase3_delta + Phase4_delta + Phase5_delta + Phase6_delta

As shown in Figure 38 (loop one, 6-phase example shown), the designer can configure the VR to dynamically add or shed phases as the load current varies. Both control loops of the IR35217 have the DPC feature.

Theory of Operation

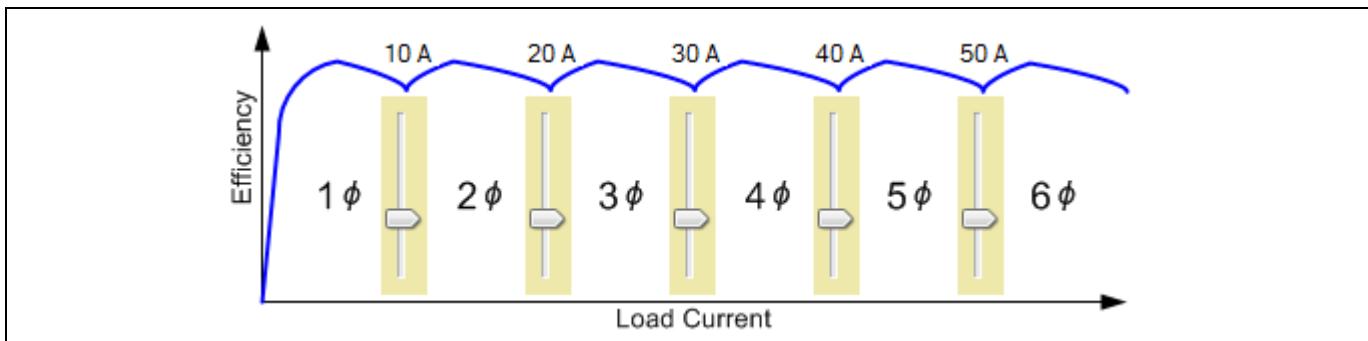


Figure 38 Dynamic Phase Control Regions

The IR35217 Dynamic Phase Control reduces the number of phases (Figure 39) based upon monitoring both the filtered total current and the error voltage over the DPC filter window. Monitoring the error voltage ensures that the VR does not drop phases during large load oscillations.

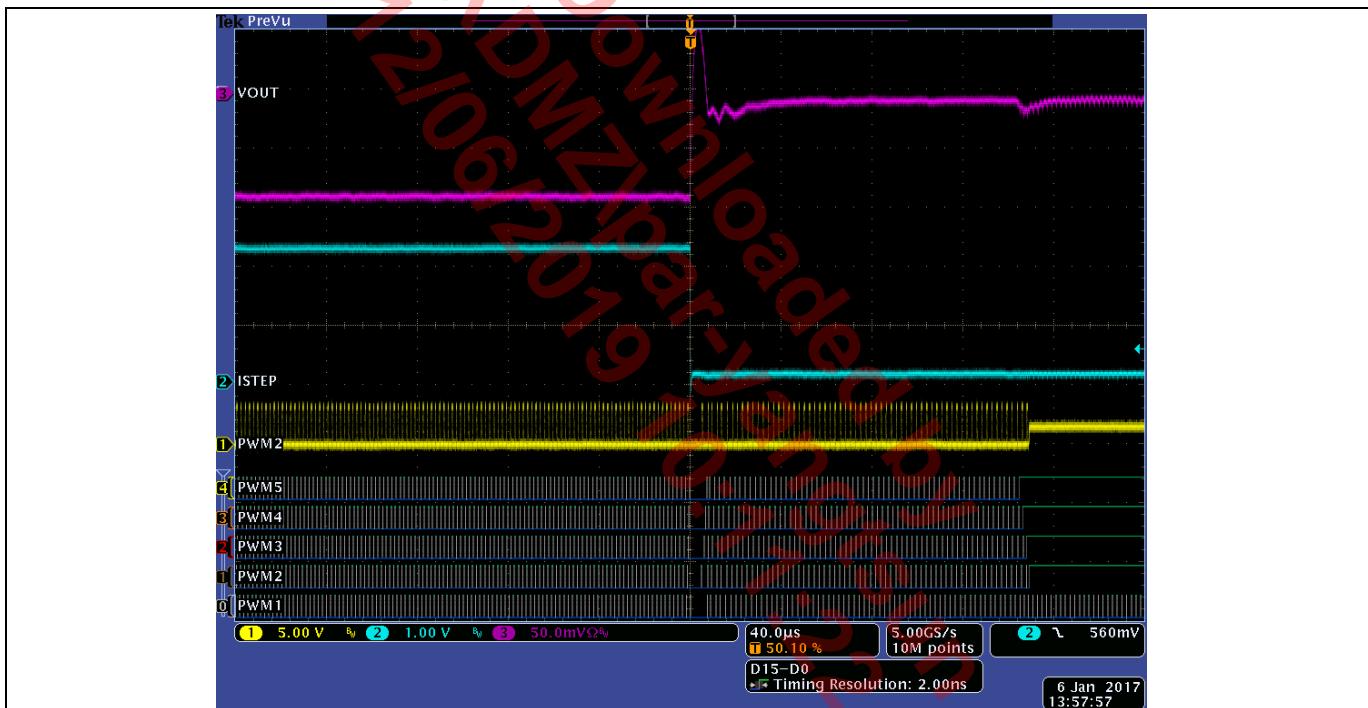


Figure 39 Phase Shed 5 to 1

During a large load step, and based on the error voltage, the controller instantly goes to the maximum number of phases. It remains at this level for a period equivalent to the DPC filter delay, after which phases get dropped depending on the load current. The Dynamic Phase Control (DPC) algorithm is designed to meet customer specifications even if the VR experiences a large load transient when operating with a lower number of phases. The ATA circuitry ensures that the idle phases are activated with optimum timing during a load step as shown in Figure 40 and Figure 41 below.

Theory of Operation



Figure 40 Phase Add 1 to 5

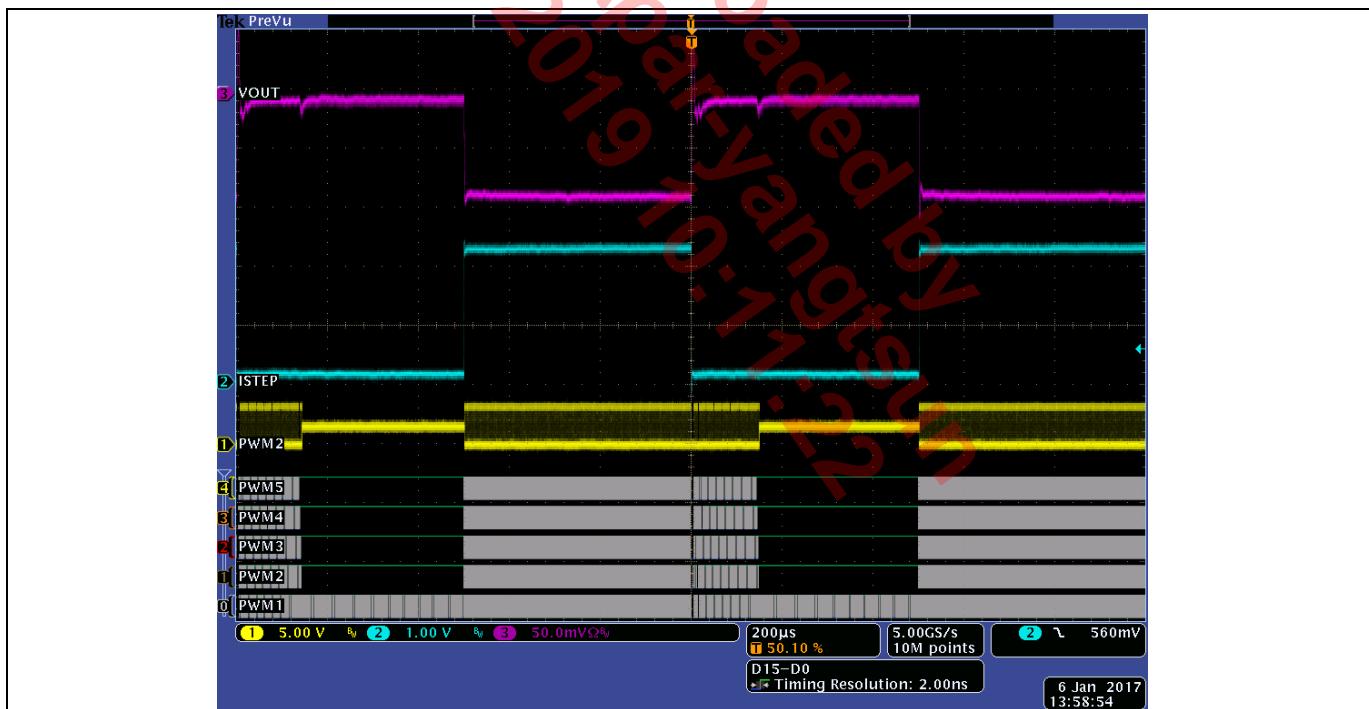


Figure 41 Zoomed-out View of Phase Shed/Add

Current limit and current balancing circuits remain active during ATA events to prevent inductor saturation and maintain even distribution of current across the active phases.

The add/drop points for each phase can be set in 2A increments from 0 to 62A per phase, with a fixed 4A hysteresis. This results in a uniform per-phase current density as the load increases or decreases.

Having DPC enabled optimizes the number of phases used in real time, providing significant light and medium-load efficiency improvements, as shown in Figure 42.

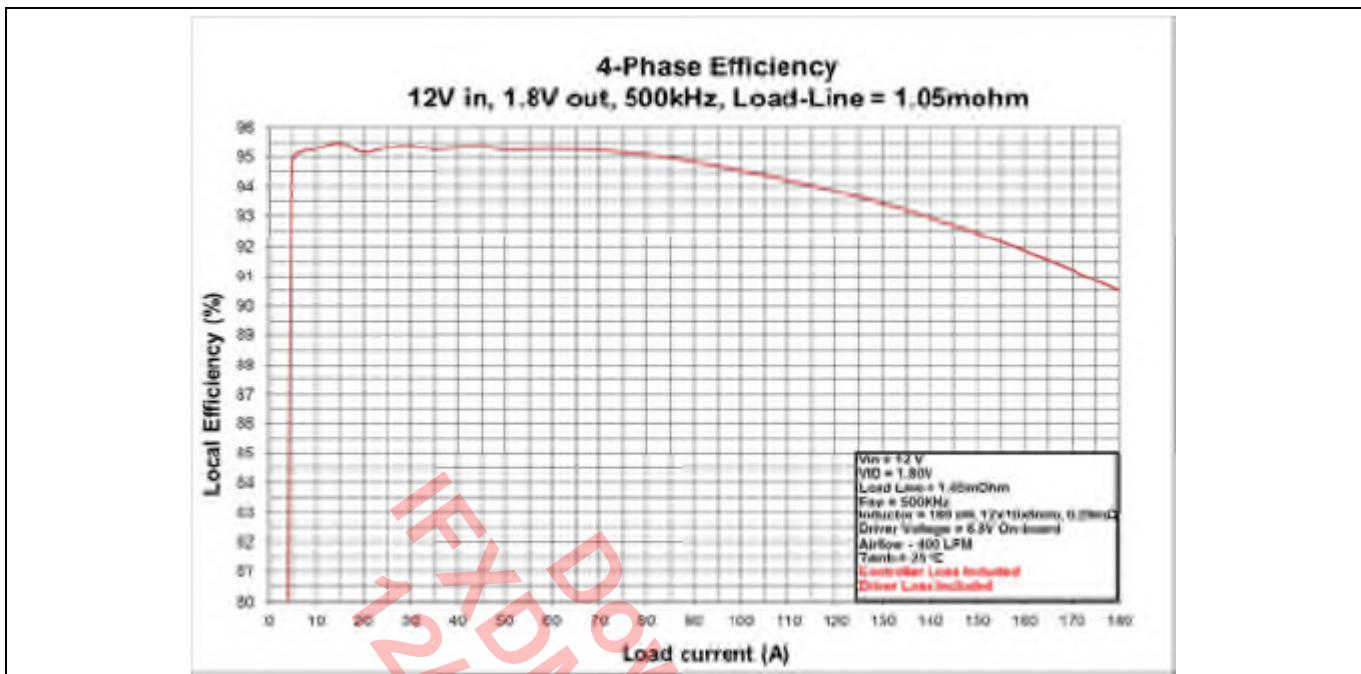


Figure 42 Light Load Efficiency Improvements with DPC

8.22.3 Discontinuous Mode of Operation – PS2, PS3

Under very light loads, the VR efficiency is dominated by MOSFET switching losses. In PS2 mode, the IR35217 operates as a constant on-time controller where the user sets the desired peak-to-peak ripple by programming an error threshold and the on-time duration (Table 33). PS3 operation is identical to PS2, with the additional ability to disable the internal current sense amplifiers within the controller for further reduction in power consumption.

Table 33 PS2 Mode Constant On-time Control

Register Variable	Function
ni_thresh	Sets the current level below which PS2 is entered.
de_thresh	Sets the error threshold to start a pulse during diode emulation, in 3mV resolution.
DE_On_Pulse_Width	Sets the duration of the ON time pulse in 40ns steps during diode emulation.
Reduce_DE_Off_Time	Reduces the calculated low-side FET ON time during diode emulation in 60ns steps. Useful for compensating for Power Stage or other drivers' tri-state delay for better zero-crossing prediction.

In PS2 mode (Active Diode Emulation Mode), the internal circuitry estimates when the inductor current declines to zero on a cycle-by-cycle basis, and shuts off the low-side MOSFET at an appropriate time in each cycle (Figure 43). This effectively lowers the switching frequency, resulting in lowered switching losses and improved efficiency.

Industry standard tri-state drivers typically have delays when entering tri-state, typically 150ns to 300ns, which allows negative current to build up, causing switch node ringing and reducing efficiency. The Reduce_DE_Off_Time variable allows for compensation of the tri-state delay by reducing the low-side FET on-time by an equivalent amount.

Theory of Operation

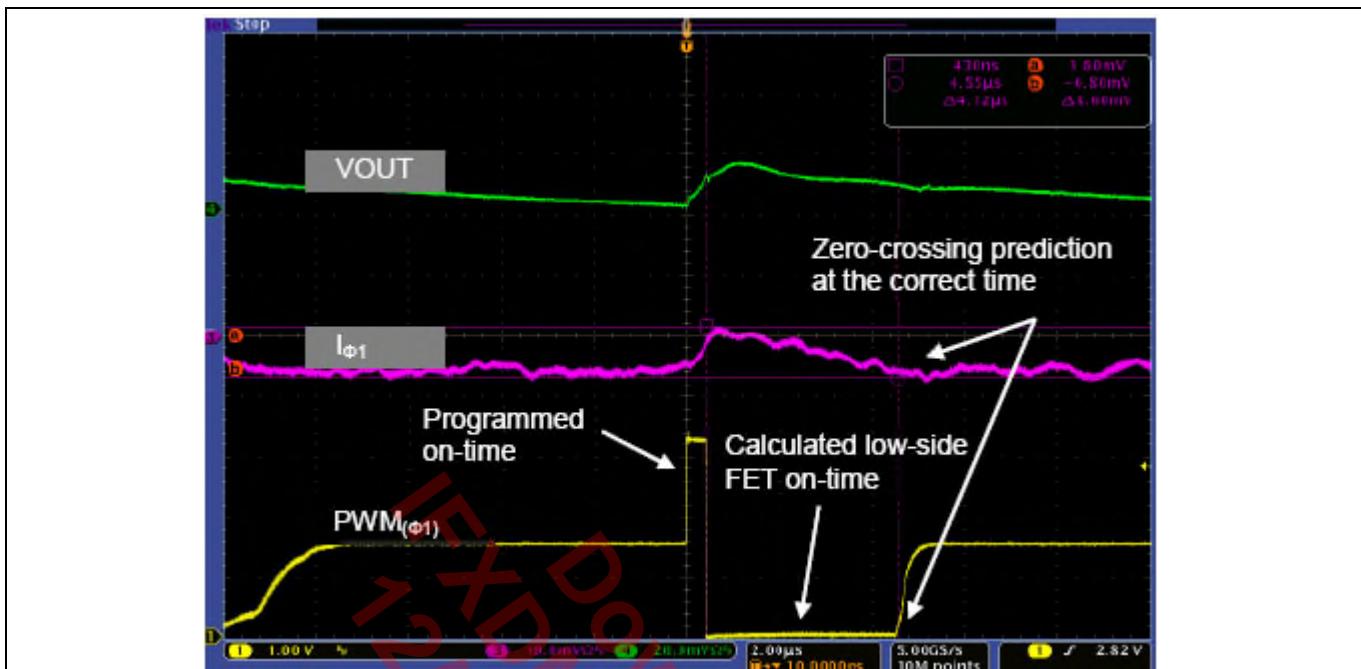


Figure 43 PS2 Active Diode Emulation Mode

8.22.4 PS4 Mode

The IR35217 controller supports the PS4 command but does not reduce controller power consumption.

When a valid PS4 command is received by the controller, the IR35217 does the following:

- Acknowledge the command.
- Output voltage is DVID or Decay down to 0 Vdc depending upon the configuration in "ps4_dvid_or_decay" register.
- PWM signals of all phases are tristated.

The controller does not shutdown the circuitry for lowest power consumption.

PS4 wake up can be set to wake on any SVID clock or alternatively on any SVID Set_VID or SetPS0/1/2/3 command.

8.22.4.1 Ps4 Register Support

IR35217 controller supports SVID register "PS4 Exit Latency" (2B). This register holds the encoded value for PS4 exit latency calculated as:

$$\text{Latency}(\text{usec}) = \frac{x}{16} \times 2y$$

Where x = bits[3:0], y = bits[7:4]

8.23 Variable Frequency with Load (Loop1 Only)

In addition, the controller can be made to operate at a high frequency when only a few phases are running, and lower the frequency as more phases are added. This skew feature is based on monitoring the per-phase current. The different skews of the switching frequency available are:

Theory of Operation

Table 34

Switching Period Skew Range	Per-phase Starting Current
Fsw to 2 x Fsw	8A
Fsw to 2 x Fsw	12A
Fsw to 2 x Fsw	16A
Fsw to 0.5 x Fsw	8A
Fsw to 0.5 x Fsw	12A
Fsw to 0.5 x Fsw	16A

Note: Per-phase Current is limited to 62A in normal mode, and 124A in Doubler Mode.

Using the above feature, the switching frequency can be skewed based on the different register settings and per-phase currents – the switching frequency skew factor versus per-phase currents have been plotted in Figure 44 below for 3 of the register settings for reference.

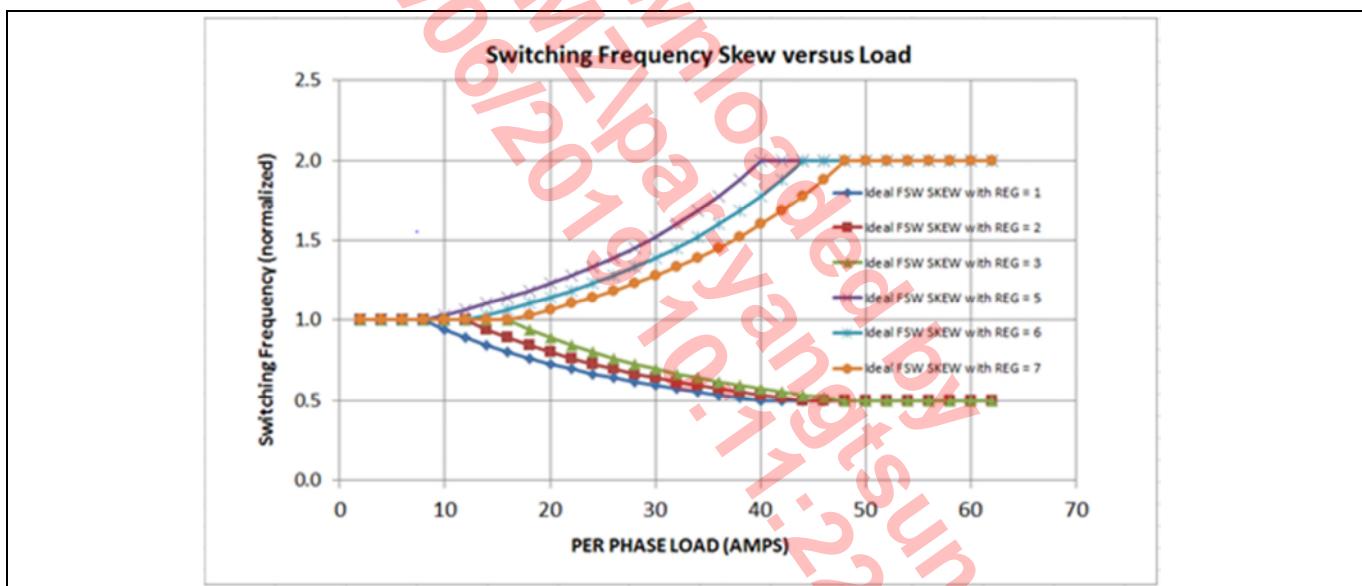


Figure 44 Normalized Switching Frequency Skew

Faults and Protections

9 Faults and Protections

The comprehensive fault coverage of the IR35217 protects the VR against a variety of fault conditions. Faults can be configured and monitored through the IR PowIRCenter GUI. There are two types of fault monitoring registers. In addition to real-time fault registers, there are "sticky" fault registers that can only be cleared with an I_C command or 3.3V power cycle. These will indicate if any fault has occurred since the last power cycle, even if the fault has cleared itself and the VR has resumed normal operation. Below is a list available faults.

- Output Over-voltage
- Output Under-voltage
- Output Over-current
- Over-temperature
- Input Under-voltage
- Input Over-voltage

There are also several Warning Flags available with the IR35217. They warn the system through an output pin that a set threshold has been exceeded. They do not shutdown the VR.

- VRHOT
- ICRITICAL
- IOUP_ALERT
- PIN_ALERT

9.1 Output Over-voltage Protection (OVP)

When the VR is disabled and during soft-start, a Fixed OVP Threshold is enabled and can be programmed to one of the thresholds shown in Table 35. If the output voltage happens to exceed this fixed threshold, the IR35217 will detect an output over-voltage fault and turn on the low-side MOSFETS to limit the output voltage rise. Once soft-start is complete and the output voltage has reached its regulation point, the Fixed OVP Threshold is disabled.

The IR35217 now monitors the output voltage to a relative OVP Threshold that is user-programmable values shown in Table 36. If the output voltage goes above the Output Voltage Set point by the programmed threshold, the IR35217 will detect an output over-voltage fault and turn on the low-side MOSFETS to limit the output voltage rise. The OVP action on the low-side MOSFETS is programmable to either Latch the low-side MOSFETS ON indefinitely, or keep the low-side MOSFETS ON and release them when the output voltage drops to less than 248mV.

Table 35 Fixed OVP Thresholds

Value	Threshold
0	2.5V
1	1.2V
2	1.275V
3	1.35V

Table 36 Relative OVP & UVP Thresholds

Value	Threshold
0	50mV
1	100mV

Faults and Protections

Value	Threshold
2	150mV
3	200mV
4	250mV
5	300mV
6	350mV
7	400mV

The ability to release the low-side MOSFETS reduces the undershoot of the output voltage during recovery from an OVP condition (See comparison of Figure 45 and Figure 46). If the output voltage rises above the OVP threshold during recovery, the low side MOSFET's will again be turned on until Vout drops below the release threshold level. Note that OVP is disabled during a DVID-down event to prevent false triggering.



Figure 45 OVP – MOSFET Latched ON



Figure 46 OVP – MOSFET Released when Output < 248mV

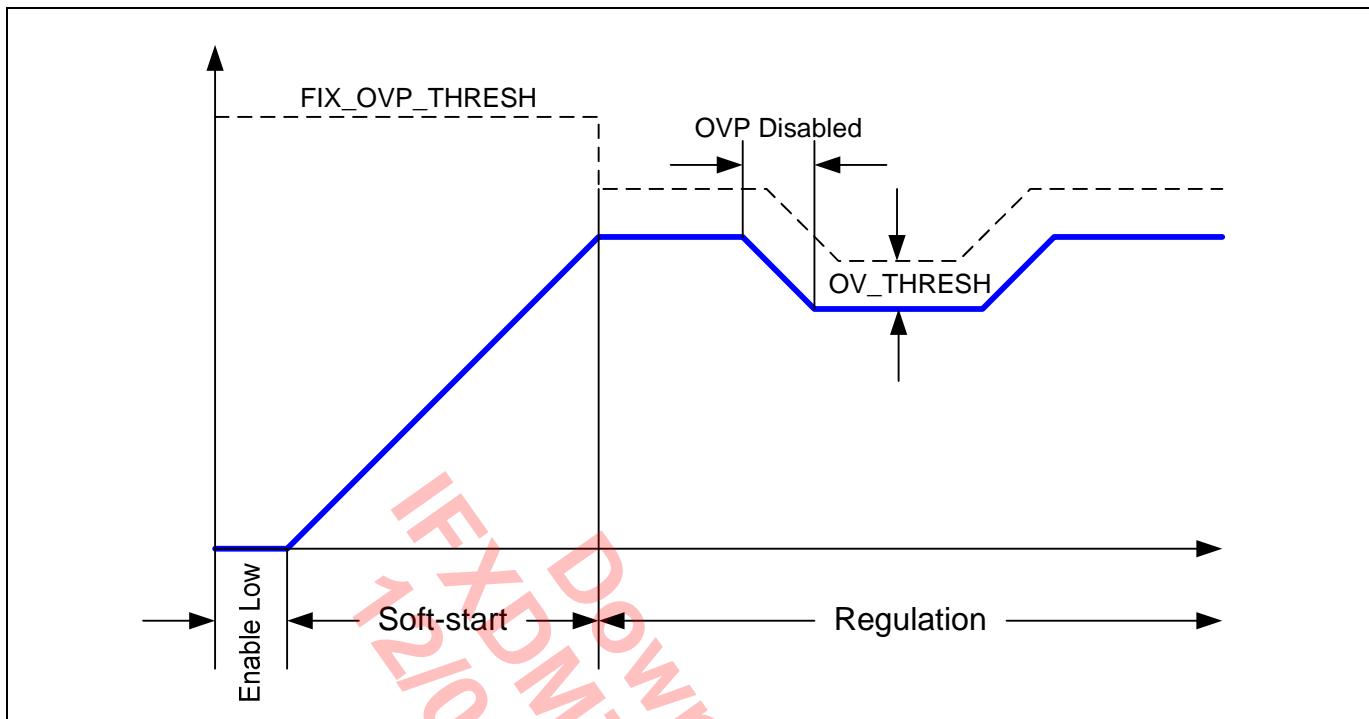


Figure 47 Mode of Operation with Fixed to Relative OVP Hand-off

9.2

Output Under-voltage Protection (UVP)

The IR35217 detects an output under-voltage condition if the sensed voltage is below the user-programmable Relative UVP Threshold shown in Table 36 or below a fixed 248mV if ADC detection is used instead of comparator detection. The relative thresholds will only be enabled if comparator detection is enabled. The UVP mode of operation is shown in Figure 48. UVP shutdown behavior can be set as shown in Table 37

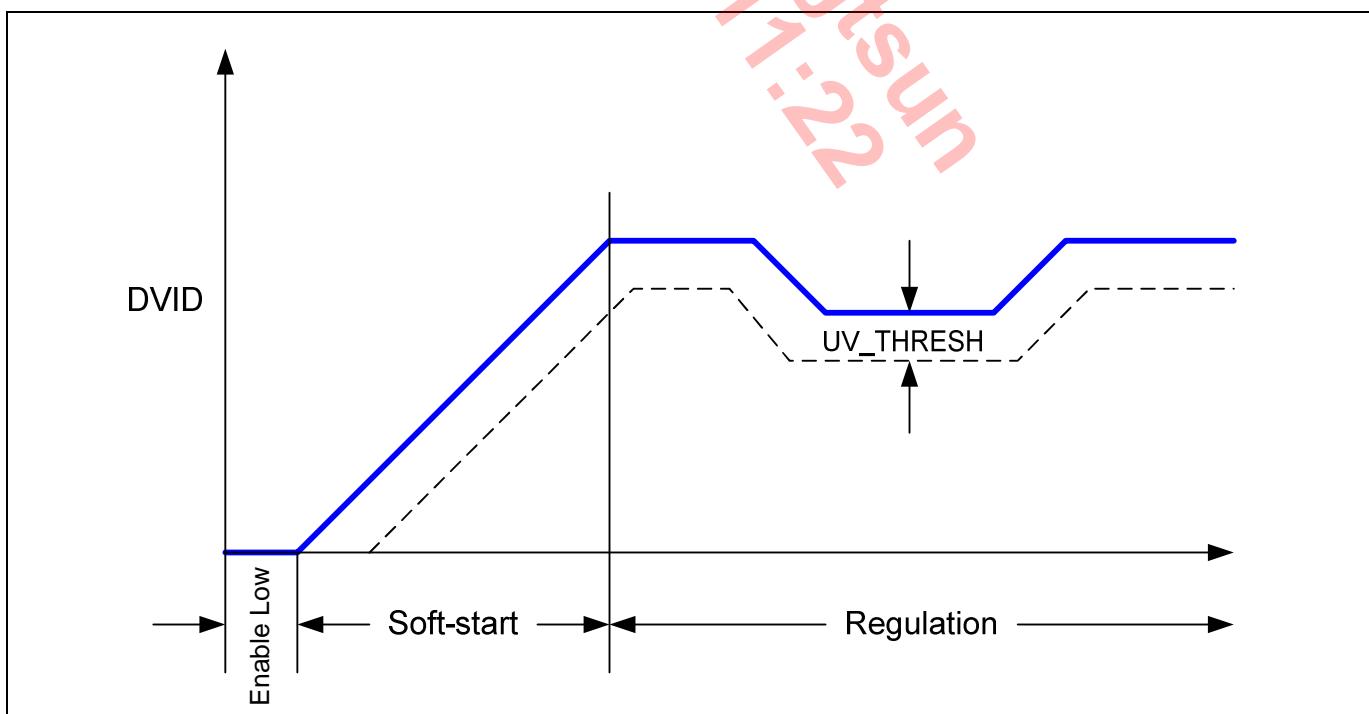


Figure 48 UVP Mode of Operation

Faults and Protections

9.3 Output Over-current Protection (OCP)

9.3.1 Current Limit

The IR35217 provides a programmable output over-current protection threshold of up to 62A per phase for a Total OC Limit of:

$$OC\ Limit = Per\ Phase\ OC\ Threshold \times \#Phases$$

The action that the controller can take when an OC condition is detected is shown in Table 37. Note that the OCP protection is disabled during start up and during VOUT transitions. The Per Phase OC Threshold also increases to 2x in Doubler Mode.

Table 37 OCP & UVP Behavior

OCP Behavior
Shutdown Immediately
Hiccup Forever
Hiccup 6 times then shutdown

9.3.2 Slow Current Limit

In addition to the Current Limit, a Slow Current Limit can be programmed to monitor and protect against the thermal effects of the average current over time. This allows the system designer to operate close to the TDP level of the system. The slow current limit bandwidth is set by the telemetry bandwidth to one of the following options:

Table 38

Value	Bandwidth
0	0.69
1	1.39
2	2.78
3	5.55
4	11.1
5	22.2
6	44.6
7	89.5

When the slow OCP threshold is exceeded, the VR will shut down based upon the OCP behavior programmed. Note that the slow OCP protection is disabled during start up and during VID transitions.

9.4 FAST Over-current Protection and IOUT_ALERT#

The IR35217 can detect and flag an output overcurrent condition in less than 6uS using the IOUT_ALERT# pin. The threshold is user settable between 2A and 510A. The typical setpoint accuracy is +/- 5%. For a VR that has 8 phases and uses 1% tolerance shunt resistors, the worst case OCP setpoint tolerance will be +/- 2.7%. The alert assertion time is based on a comparator looking directly at the summed inductor current so all internal filtering is bypassed. The maximum delay from the time the summed inductor current exceeds the user set threshold to the time the IOUT_ALERT# pin asserts is 4usec. This comparator can also be used for fast over current protection.

Table 39

Register	Function
fast_ocp_warn_timer	Sets the de-assertion delay after IOUT drops below the warning hysteresis . Range is 0uS to 327mS
fast_ocp_fault_hys	Specifies the reduction in IOUT that will reset OCP. Range is 4A to 32A
fast_ocp_warn_hys	Specifies the reduction in IOUT that will cause the IOUT_ALERT# flag to de-assert. Range is 4A to 32A
fast_ocp_fault_limit	Sets the IOUT level that will cause OCP. 2A/LSB, 510A range
fast_ocp_warn_limit	Sets the IOUT level that will cause IOUT_ALERT# to assert. 2A/LSB, 510A range
fast_ocp_enable	Enable bit for the IOUT_ALERT# and FAST OCP feature
fast_ocp_fault_delay	Sets the delay from IOUT crossing OCP limit to VR shutdown. 5uS/LSB, 0 to 155uS range

9.5 Over-temperature Protection (OTP)

The IR35217 can measure the temperature via TSEN_N pin that is used for over temperature protection, the VR_HOT flag and temperature monitoring. The temperature is measured with either the Power stage temperature output (TOUT) or using an NTC network. The thresholds are programmable in 1°C increments within the range shown in Table 40.

Table 40 OT Warning and Fault Threshold Range

Function	Range
OT Warning (VRHOT#)	64°C to 127°C
OT Fault	0°C to 30°C + OT Warning.

Note: Maximum OT Fault Limit is 134°C with NTC temperature sensing.

The OT Warning threshold is set through the Temp_max Threshold. When the temperature monitored on either TSEN1 or TSEN2 exceeds the threshold, the VRHOT# pin is asserted (Active-low). It will remain asserted until the temperature drops below 95% of the set threshold.

If the measured temperature exceeds the OT Threshold (Temp_max + ovtp_thresh), the IR35217 will latch off the VR, requiring a system power recycle or an ENABLE recycle to resume operation.

9.5.1 NTC Temperature Sensing

The IR35217 includes a pre-programmed look-up table that is optimized for the recommended NTC options shown in Table 41. The NTC network is connected to the TSEN_N pin as shown in Figure 49. The NTC should be placed near the hottest spot of the VR for good temperature protection.

A 0.01μF capacitor is recommended for filtering when used with the NTC sense network.

Faults and Protections

Table 41 NTC Temperature Sense

NTC	R_{NTC}	$R_{parallel}$
Murata NCP15WB473F03RC or Panasonic ERT-J0EP473J	47KΩ	13KΩ

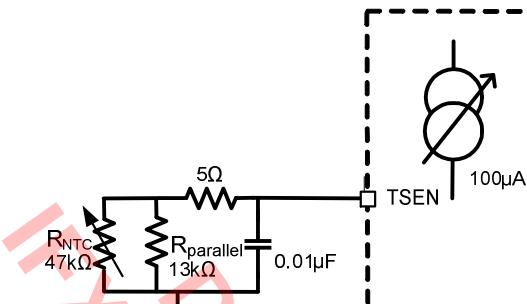


Figure 49 Temperature Sense NTC Network

9.5.2 Power Stage Temperature Sensing (TOUT)

The controller is designed to interface with the Power Stage to receive temperature and fault information via the TSEN_x pin (Figure 50). The power stage temperature output is scaled to 8mV/°C ($0^{\circ}\text{C}=0.6\text{V}$) and a 1:1.64 divider is required to scale this down to the 4.88mV/C gain of the controller input. Any failure within the Power Stage is communicated by pulling its temperature sense output to 3.3V. A 3.3V at the controller's TSEN_x pin indicates one of the following has occurred in the Power Stage:

- 1) A power stage phase fault
- 2) An over temperature
- 3) A persistent overcurrent
- 4) An over voltage condition

The controller can shut down or continue operating and assert the CATFLT pin upon receiving the power stage fault.

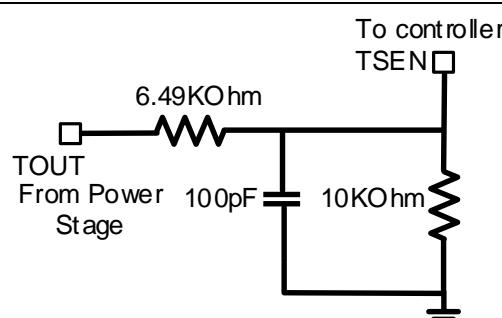


Figure 50 Temperature Sensing using TOUT

Faults and Protections

9.6 Input Over-voltage Protection

The IR35217 offers protection against input supply over-voltage. When enabled, the VINSEN pin is compared to a fixed threshold of 14.5V with a 14:1 divider, and shuts down the VR if the threshold is exceeded.

9.7 Phase Faults

The IR35217 can detect and declare a phase fault when the current in one or more phases is too high or too low. It detects the fault when the duty cycle of a particular phase is 5% higher or lower than the average duty cycle of all the phases. This feature helps detect severe imbalances in the phase currents, an unpowered or damaged MOSFET driver, or a phase that is disconnected from Vin. The phase fault feature can be enabled or disabled through an MTP bit. When a phase fault occurs, the controller shuts down the loop where the fault occurred, and sets register bits to display which phase had the fault and whether it faulted high or low. The phase fault registers are cleared via a register bit and the VR will restart once ENABLE or Vcc is cycled.

Table 42 Phase Fault Registers

Register	Function
pi_fault_en	Enables phase current fault shutdown.
clear_phase_faults	Clears all phase faults for each loop.
pi_fault	Indicates which phase has a phase current fault. 0 – phase1, 1 – phase2, 2 – phase3, 3 – phase4...7-phase 8
max_cond	Indicates one or more phase currents are too high.
min_cond	Indicates one or more phase currents are too low.

9.8 Warning Flags

9.8.1 VRHOT_ICRIT# Pin Functionality

The functionality of the VR_HOT_ICRIT# pin can be set to assert when levels of Temp_max, Icc_max, and/or OCP levels are exceeded. Table 43 shows the multiple configurations of the VR_HOT_ICRIT# pin.

Table 43 VRHOT_ICRIT# Pin Options

Value	Pin Option
0	Temp_max Only
1	Temp_max or Icc_max
2	Temp_max or OCP
3	Icc_max Only

Faults and Protections

9.8.2 Icritical Flag

The IR35217 VR_HOT_ICRIT# pin can be optionally programmed to assert when a user programmable output current level is exceeded. The assertion is not a fault and the VR continues to regulate. I_CRITICAL monitors an output current through a 966 Hz filter. It has a 5% hysteresis level so the VR_HOT_ICRIT pin will de-assert when the average output current level drops below 95% of the programmed current level threshold.

9.8.3 PIN_ALERT#

The IR35217 has a PIN_ALERT# pin to alert the system when the input power has exceeded a preset threshold. The pin is an open drain output that is high until the input power threshold is exceeded at which point it pulls low. The output stays low until the input power drops below 90% of the Pin_Alert threshold. The PIN_ALERT# pin will de-assert 100mS after the input power drops below 90% of the PIN_ALERT threshold. In an Intel system the Pin_alert pin is pulled up with a 4.99kohm resistor to 3.3 Vdc. The PIN filtered by a 2KHz BW filter. The PIN_ALERT# pin assertion will be delayed by up to 300uS.

Downloaded by TXDMZpar-yangtsun
12/06/2019 10:11:22

10 Telemetry Monitoring Functions

IR35217 can provide real-time accurate measurement of input voltage, input current, output voltage, output current, phase current, and temperature, and provides this information over the I₂C/PMBus interface.

10.1 Real-time Telemetry

Below is a list of Real-time Telemetry information available in the IR35217.

- Input Voltage
- Input Current
- Output Voltage
- Output Current
- Temperature (TSEN1 and TSEN2)
- Phase Currents
- Input Power
- Output Power

10.2 Min/Max Telemetry

Min/Max registers for IOUT, IIN, VOUT, VIN, and TEMPERATURE are available. The data is read by setting a pointer and reading the value from a register that contains the minimum and maximum data. These registers store high and low values from startup or the last read, whichever was the latest to occur. The registers are automatically cleared when the data is read back from the controller.

The minmax_sel[4:0] register is the pointer used to select the appropriate signal and the minmax_val[7:0] register will show the min or max value of what has been selected. The list of available min/max values, bandwidth, and resolutions are shown in Table 44.

Table 44 Min/Max Registers

Pointer Value	Parameter	Signal Bandwidth	Resolution
0	loop_1_current_min	62 KHz/3.93 KHz (based on minmax_output_i_bw)	2A
1	loop_1_current_max		
2	loop_2_current_min		0.5A
3	loop_2_current_max		
4	loop_1_input_current_min	102Hz	0.125A
5	loop_1_input_current_max		
6	loop_2_input_current_min		0.0625A
7	loop_2_input_current_max		
8	loop_1_output_voltage_min	Telemetry_bw	0.0625V
9	loop_1_output_voltage_max		
10	loop_2_output_voltage_min		0.125V
11	loop_2_output_voltage_max		
12	input_voltage_min	760Hz	0.125V
13	input_voltage_max		
14	temp1_min	Telemetry_bw	1C
15	temp1_max		
16	temp2_min	Telemetry_bw	1C
17	temp2_max		

10.3 Accuracy Optimization Registers

The IR35217 provides excellent factory-trimmed chip accuracy. In addition, the designer has calibration capability that can be used to optimize reporting accuracy for a given design, with minimum component changes. Once a design is optimized, the IR35217 provides excellent repeatability from board to board. The IR35217 also provides capability for individual board calibration and programming in production for best accuracy. Table 45 shows the MTP registers used to fine tune the accuracy of the reported measurements. Figure 51 to Figure 53 show the typical accuracy of the output current, input voltage and output voltage measurements using the IR35217.

Table 45 Accuracy Optimization Registers

NVM Register	Function
IIN Fixed Offset	Offsets the input current in $1/32A$ steps.
IIN Per Phase Offset	Offsets the input current dependent upon the number of active phases in $1/128A$ steps e.g. the drive current for the MOSFET's. This current increases every time a new phase is added.
Duty Cycle Adjust	Adjusts the input current calculation to compensate for a non-ideal driver.
IOUT Current Offset	Offsets the total output current from $-16A$ to $+15.75A$ at $0.25A$ steps
Vout Offset	Offsets the output voltage $+40mV$ to $-35mV$ in $5mV$ steps
Temperature Offset	Offsets the temperature $-32^{\circ}C$ to $+31^{\circ}C$ in $1^{\circ}C$ steps to compensate for offset between the hottest component and the NTC sensing location.

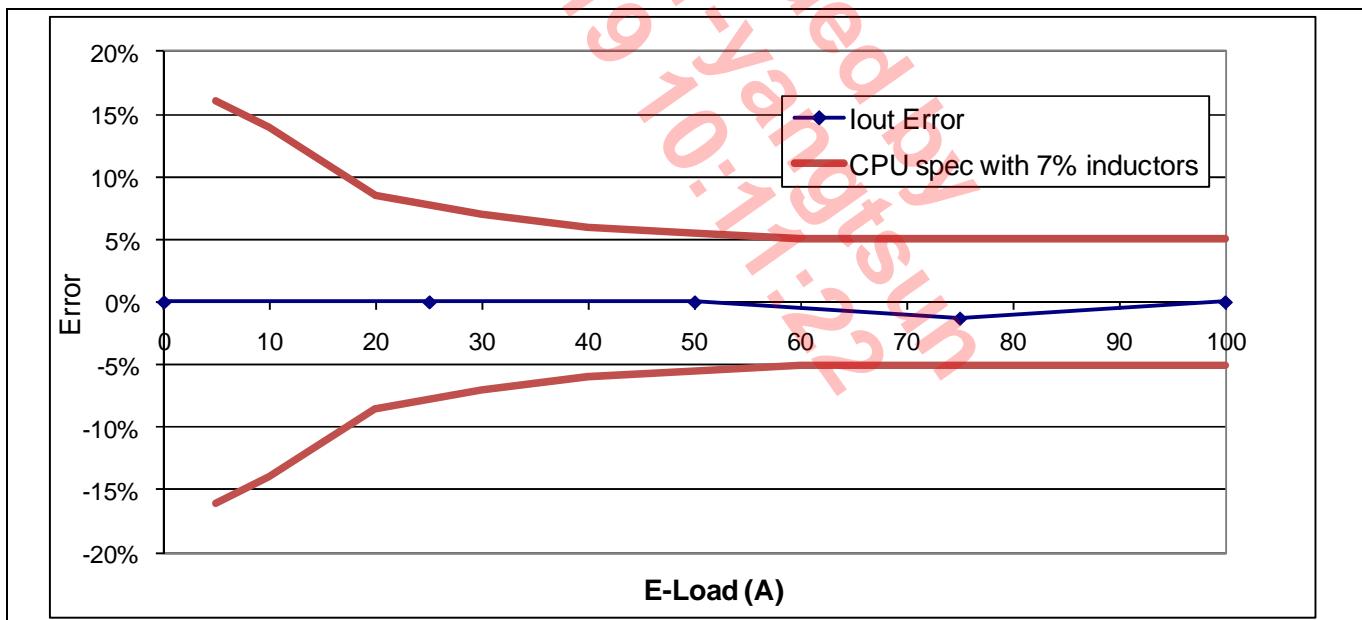


Figure 51 IOUT Error using 7% DCR Inductors

Telemetry Monitoring Functions

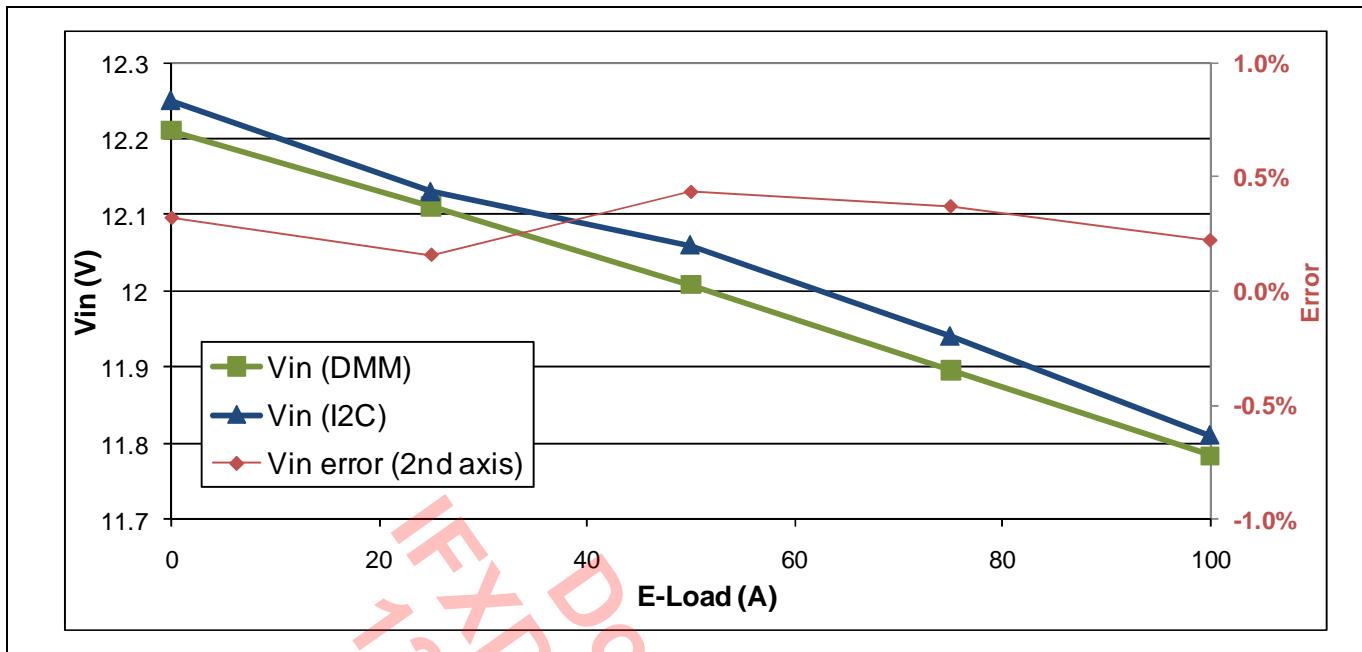


Figure 52 Input Voltage Measurement

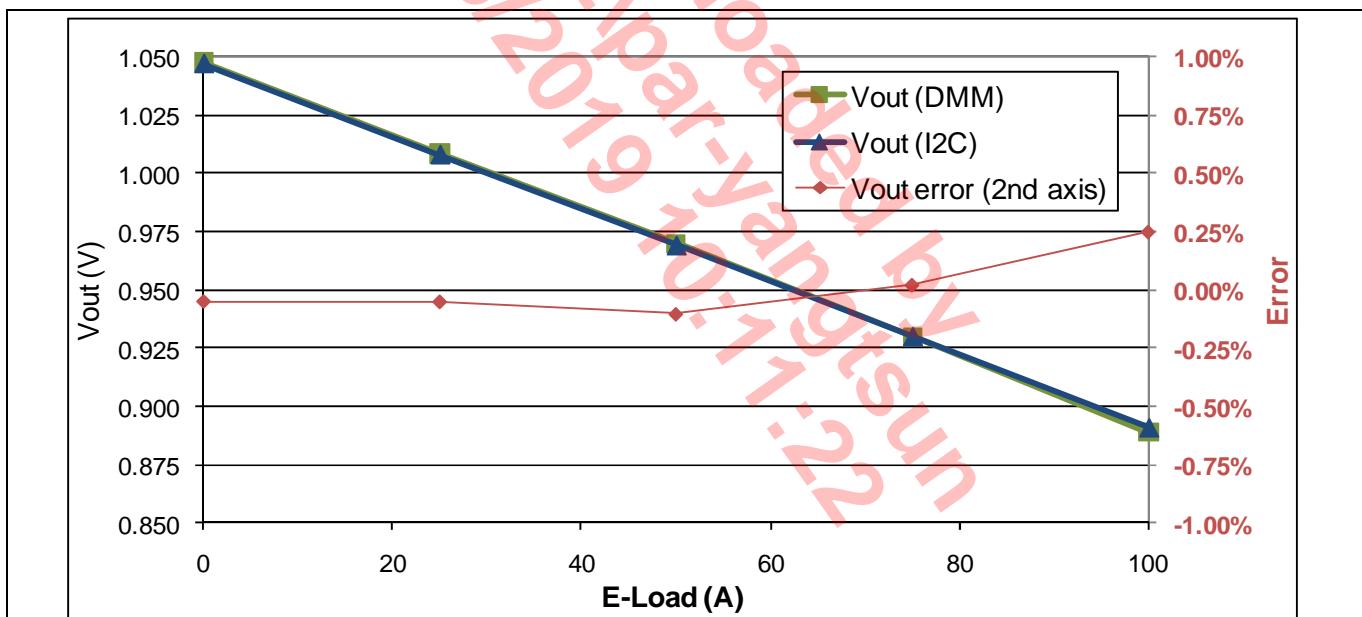


Figure 53 Output Voltage Measurement

11 I₂C/PMBus Communication

11.1 Addressing

The IR35217 simultaneously supports I₂C and PMBus through the use of exclusive addressing. By using a 7-bit address, the user can configure the device to any one of 127 different I₂C/PMBus addresses. Once the address of the IR35217 is set, it can be locked to protect it from being overridden. Optionally, a resistor can be tied to the ADDR_PROT pin to generate an offset as shown in Table 46 (note that a 0.01μF capacitor is required across the resistor per Figure 54).

As an example, setting a base 7-bit I₂C address of 28h with a resistor offset of +15 sets the 7-bit I₂C address to 37h. Similarly, setting a base 7-bit PMBus address of 40h with a resistor offset of +15 sets the 7-bit PMBus address to 4Fh.

For default programmed devices, the I₂C/PMBus address can be temporarily forced to 0Ah for I₂C and 0Dh for PMBus by setting the EN=VR_HOT=Low.

Table 46 ADDR_PROT Resistor Offset

Resistor	I ₂ C Address Offset
0.845kΩ	+0
1.30kΩ	+1
1.78kΩ	+2
2.32kΩ	+3
2.87kΩ	+4
3.48kΩ	+5
4.12kΩ	+6
4.75kΩ	+7
5.49kΩ	+8
6.19kΩ	+9
6.98kΩ	+10
7.87kΩ	+11
8.87kΩ	+12
10.00kΩ	+13
11.00kΩ	+14
12.10kΩ	+15

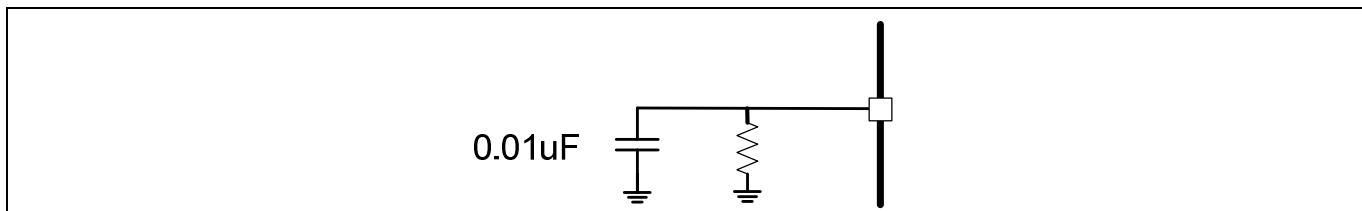


Figure 54 ADDR_PROT Pin Components

11.2 I₂C Security

The IR35217 provides robust and flexible security options to meet a wide variety of customer applications. A combination of hardware pin and software passwords prevent accidental overwrites, discourages hackers, and secures custom configurations and operating data. The Read and Write Security can be set in MTP (Table 47 and Table 48) with the protection methods shown in Table 49.

Table 47 Read Security

Setting	Description
0	No Protection
1	Configuration Registers Only
2	Protect All Registers but Telemetry
3	Protect All

Table 48 Write Security

Setting	Description
0	No Protection
1	Configuration Registers Only
2	Protect All

Table 49 Read or Write Unlock Options

Setting	Description
0	Password Only
1	Pin Only
2	Pin & Password
3	Lock Forever

11.2.1 Password Protection

The system designer can set any 16-bit password (other than ooh). This password is stored in MTP. To unlock the security, a user must write the correct password into the "Password Try" register, which is a volatile read/write register. After four incorrect tries, the IC will lock up to prevent unauthorized access.

Table 50 Password Registers

Register	Length	Location
Password	16 bit (2 bytes)	MTP
Try	16 bit (2 bytes)	R/W

The following pseudo-code illustrates how to change a password:

```
# first unlock the IC
Write old password to the Try register
# now write new password into MTP
Write new password to the Password register
# password has changed, status is locked
# Need to write new password to the Try register to unlock
```

11.2.1.1 Pin Protection

The ADDR/PROTECT pin is a dual function pin. When the IC is enabled, the resistor value is latched and stored for use in the I₂C address offset function. Thereafter, the pin acts entirely as a PROTECT pin. If enabled, the PROTECT pin must be driven high to unlock and low to lock. If the resistor address offset function is being used, care must be taken to allow the IC to read the resistor value before driving the pin high or low to set the security state. Failure to follow this precaution may result in an erroneous address offset value being latched in. The user should at least wait until the completion of the auto-trim time t₄ in Figure 8.

11.3 I₂C Protocol

All registers may be accessed using either I₂C or PMBus protocols. I₂C allows the use of a simple format whereas PMBus provides error checking capability. Figure 55 shows the I₂C format employed by the IR35217.

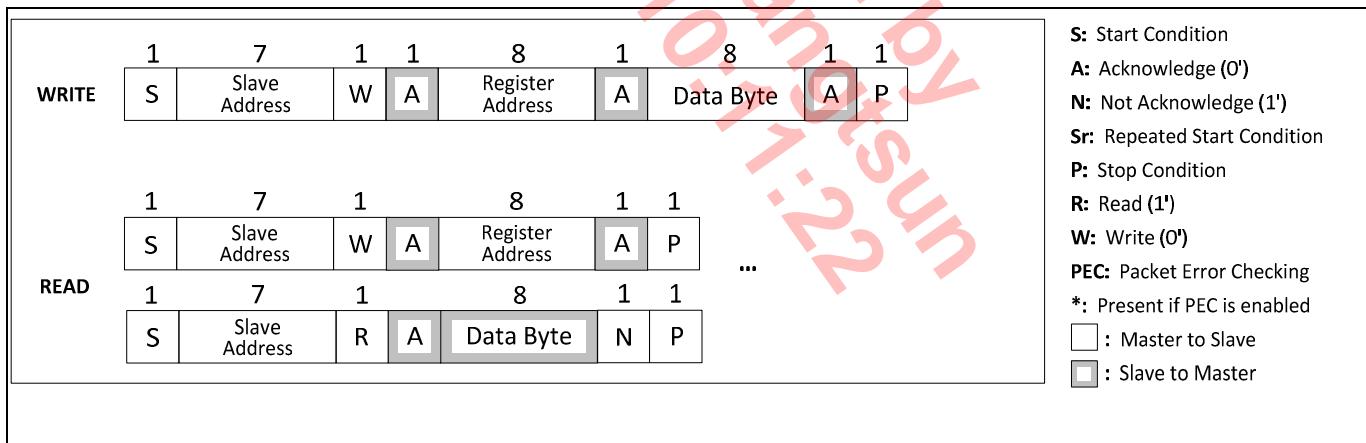


Figure 55 I₂C Format

11.4 PMBus Protocol

To access the device's configuration and monitoring registers, 4 different protocols are required:

- the PMBus Send Byte protocol with/without PEC (for CLEAR_FAULTS only)
- the PMBus Read/Write Byte/Word protocol with/without PEC (for status and monitoring)

I₂C/PMBus Communication

- the PMBus Block Read and Block Write protocols with Byte Count = 1 and Byte Count = 2
- the PMBus Block Read Process call (for accessing Configuration Registers)

An explanation of which command codes and protocols that are required to access them are given in Table 51.

In addition, the IR35217 supports:

- Alert Response Address (ARA)
- Bus timeout (30ms)
- Group Command for writing to many VRs within one command

S: Start Condition A: Acknowledge(0') N: Not Acknowledge(1') Sr: P: Stop Condition R: Read(1') W: Write(0') PEC: Calculated from Command $*$: Data is optional <input type="checkbox"/> : Master to Slave <input checked="" type="checkbox"/> : Slave to Master Note: PEC is required for the MFR_REG_ACCESS command

Figure 56 PMBus Protocol Legend

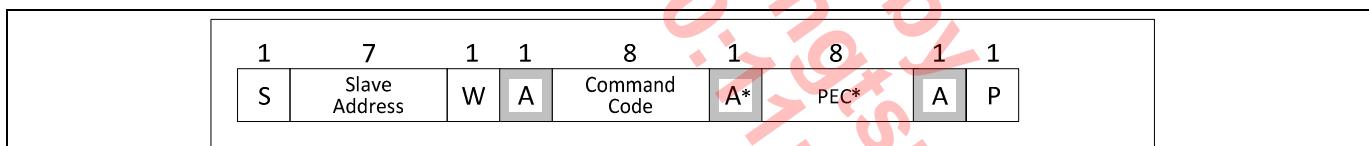


Figure 57 PMBus Send Byte

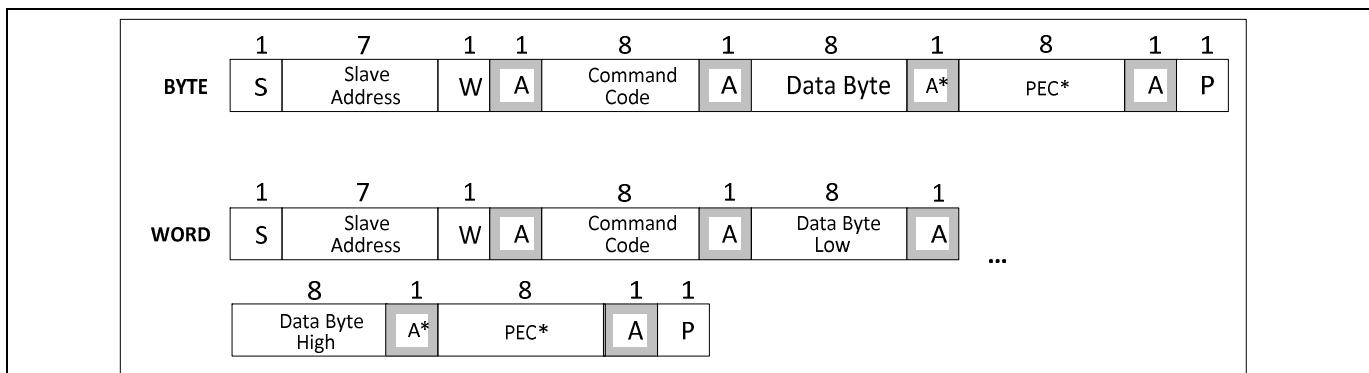


Figure 58 PMBus Write Byte/Word

Restricted

IR35217 Digital Multi-phase Controller

8+o/7+1/6+2 Dual Output Digital Multi-Phase Controller



I₂C/PMBus Communication

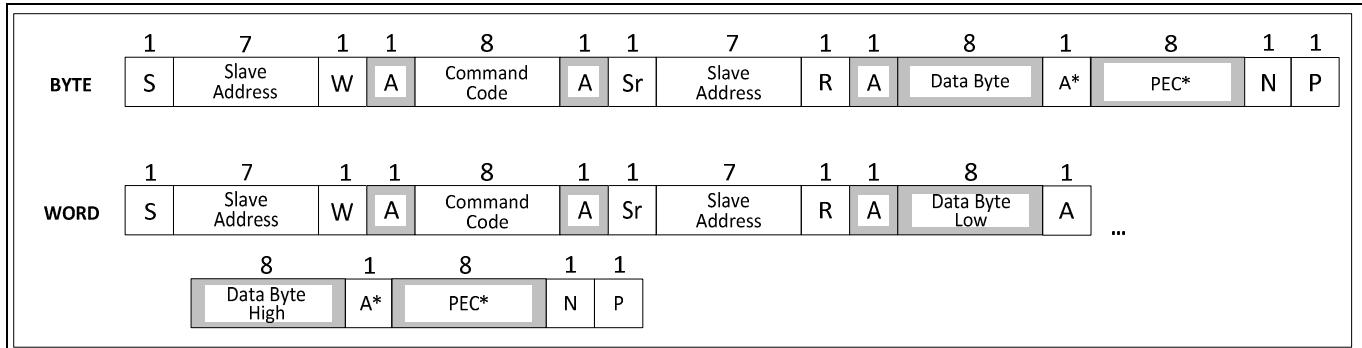


Figure 59 PMBus Read Byte/Word

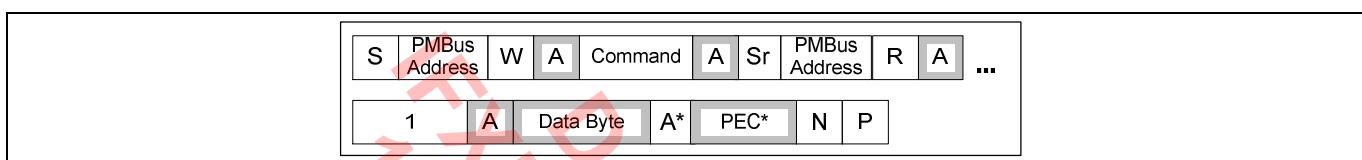


Figure 60 PMBus Block Read with Byte Count = 1

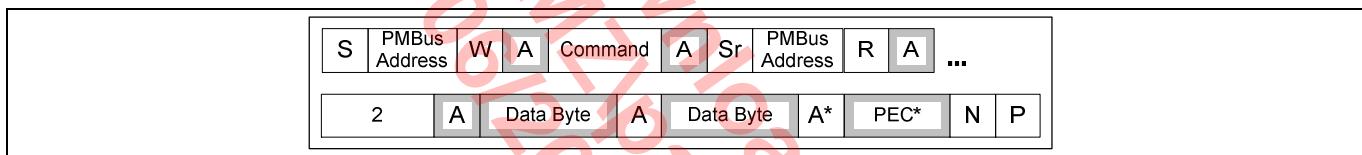


Figure 61 PMBus Block Read with Byte Count = 2

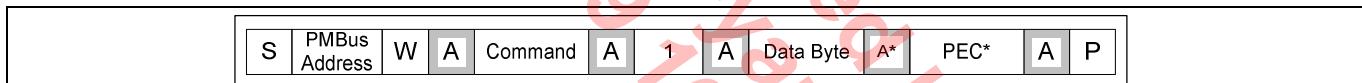


Figure 62 PMBus Block Write with Byte Count = 1

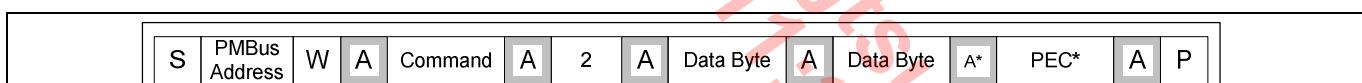


Figure 63 PMBus Block Write with Byte Count = 2



Figure 64 MFR_WRITE_REG

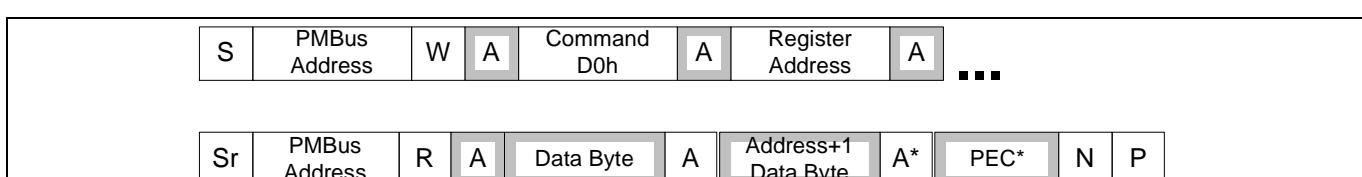


Figure 65 MFR_READ_REG

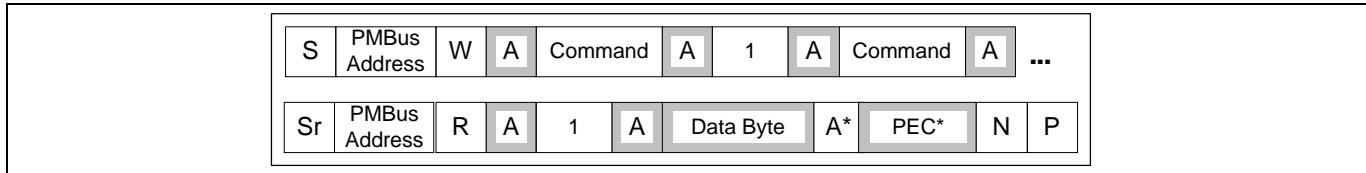
I₂C/PMBus Communication

Figure 66 Block Read Process Call

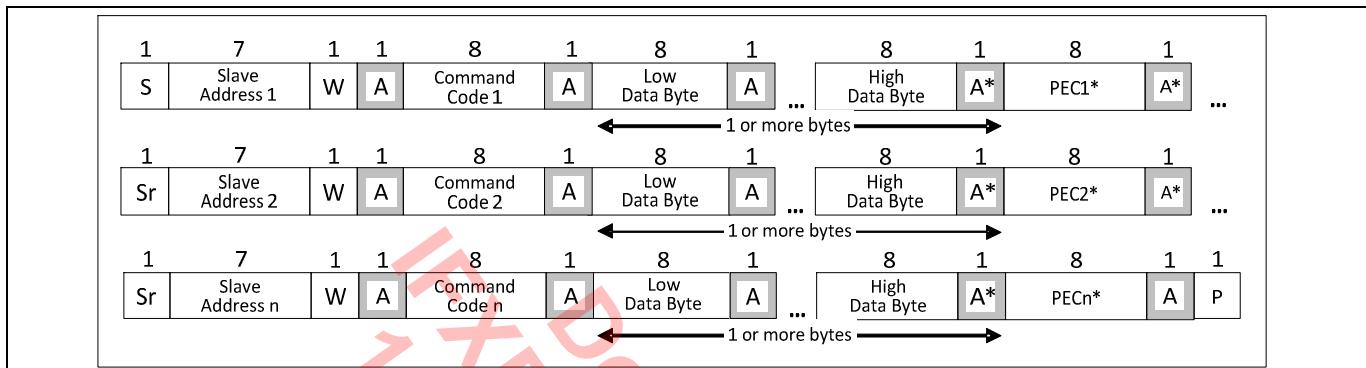


Figure 67 Group Command

11.5 PMBus Command Set

Table 51 PMBus Command Set

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
OPERATION	Read/Write Byte	01h	Enables or disables the output and controls margining. Ignores OVP on Margin High, UVP on Margin Low.
ON_OFF_CONFIG	Read/Write Byte	02h	Configures the combination of CONTROL pin and OPERATION command needed to turn the unit on and off.
CLEAR FAULTS	Send Byte	03h	Clear contents of Fault registers
WRITE_PROTECT	Read/Write Byte	10h	Provides protection from accidental changes
RESTORE_DEFAULT_ALL	Send Byte	12h	Reloads the OTP
CAPABILITY	Read Byte	19h	Returns 1010xxxx to indicate Packet Error Checking is supported and Maximum bus speed is 400kHz
SMBALERT_MASK	Block Write/ Block Read Process Call	1Bh	Set to prevent warning or fault conditions from asserting the SMBALERT# signal. Write command code for STATUS register to be masked in the low byte, the bit to be masked in the High byte.
VOUT_MODE	Read/Write Byte	20h	Sets the format for VOUT related commands. Linear mode, -8 and -9 exponents supported.
VOUT_COMMAND	Read/Write Word	21h	Sets the voltage to which the device should set the output. Format according to VOUT_MODE.
VOUT_TRIM	Read/Write Word	22h	Applies a fixed offset to the output voltage command value. Format according to

Restricted**IR35217 Digital Multi-phase Controller****8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller****I₂C/PMBus Communication**

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
			VOUT_MODE.
VOUT_MAX	Read/Write Word	24h	Sets an upper limit on the output voltage the unit can command. Format according to VOUT_MODE.
VOUT_MARGIN_HIGH	Read/Write Word	25h	Sets the margin high voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE.
VOUT_MARGIN_LOW	Read/Write Word	26h	Sets the margin low voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE.
VOUT_TRANSITION_RATE	Read/Write Word	27h	Sets the rate at which the output changes voltage due to VOUT_COMMAND or OPERATION commands. mV/ μ s; exp = [0..-1,-2,-3,-4]
VOUT_DROOP	Read/Write Word	28h	Sets the rate at which the output voltage decreases or increases with increasing or decreasing output current for use with Adaptive Voltage Positioning.
VOUT_SCALE_LOOP	Read/Write Word	29h	Sets the gain of the output voltage sensing circuitry to take into account an external resistor divider. Fixed to E8 08h
FREQUENCY_SWITCH	Read/Write Word	33h	Sets the switching frequency in KHz per table found in user note AN00031. Exp = 0, 1
VIN_ON	Read/Write Word	35h	Sets the value of the input voltage at which the unit should begin power conversion. Exp = -1.
VIN_OFF	Read/Write Word	36h	Sets the value of the input voltage that the unit, once operation has started, should stop power conversion. Exp = -1.
INTERLEAVE	Read/Write Word	37h	The INTERLEAVE command is used to arrange multiple units so that their switching periods can be distributed in time. This may be used to facilitate paralleling of multiple units or to reduce ac currents injected into the power bus. Only available on parts with the SYNC function.
IOUT_CAL_OFFSET	Read/Write Word	39h	Used to null out any offsets in the output current sensing circuitry. Exp = -2.
VOUT_OV_FAULT_LIMIT	Read Only	40h	Returns the value of the output voltage, measured at the sense or output pins, that causes an output overvoltage fault.
VOUT_OV_FAULT_RESPONSE	Read/Write Byte	41h	Instructs the device on what action to take in response to an output overvoltage fault. Only shutdown and ignore are supported.
VOUT_OV_WARN_LIMIT	Read/Write Word	42h	Sets the value of the output voltage, measured at the sense or output pins, that causes an output overvoltage warning. Format as determined by VOUT_MODE.
VOUT_UV_WARN_LIMIT	Read/Write Word	43h	Sets the value of the output voltage, measured at the sense or output pins, that causes an output

Restricted**IR35217 Digital Multi-phase Controller****8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller****I₂C/PMBus Communication**

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
			voltage low warning. Format as determined by VOUT_MODE.
VOUT_UV_FAULT_LIMIT	Read Only	44h	Returns the value of the output voltage, measured at the sense or output pins, that causes an output undervoltage fault.
VOUT_UV_FAULT_RESPONSE	Read/Write Byte	45h	Instructs the device on what action to take in response to an output undervoltage fault. Only shutdown and ignore are supported.
IOUT_OC_FAULT_LIMIT	Read/Write Word	46h	Sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. Set by writing this command in Linear format with a -1 exponent.
IOUT_OC_FAULT_RESPONSE	Read/Write Byte	47h	Instructs the device on what action to take in response to an output overcurrent fault. Only Coh (shutdown immediately), F8h (hiccup forever), and D8 (hiccup 3 times) are supported.
IOUT_OC_WARN_LIMIT	Read/Write Word	4Ah	Sets the value of the output current that causes an output overcurrent warning. Set by writing this command in Linear format with a -1 exponent.
OT_FAULT_LIMIT	Read/Write Word	4Fh	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an overtemperature fault. Exp = 0.
OT_FAULT_RESPONSE	Read/Write Byte	50h	Instructs the device on what action to take in response to an overtemperature fault. Only shutdown and ignore are supported.
OT_WARN_LIMIT	Read/Write Word	51h	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an Overtemperature Warning alarm. Exp = 0.
VIN_OV_FAULT_LIMIT	Read/Write Word	55h	Sets the value of the input voltage that causes an input overvoltage fault. Exp = -4.
VIN_OV_FAULT_RESPONSE	Read/Write Byte	56h	Instructs the device on what action to take in response to an input overvoltage fault. Only shutdown and ignore are supported.
VIN_UV_WARN_LIMIT	Read/Write Word	58h	Sets the value of the input voltage that causes an input voltage low warning. Exp = -4.
IIN_OC_WARN_LIMIT	Read/Write Word	5Dh	Sets the value of the input current, in amperes, that causes a warning that the input current is high. Exp = -1.
POWER_GOOD_ON	Read/Write Word	5Eh	Sets the output voltage at which an optional POWER_GOOD signal should be asserted. Format according to VOUT_MODE.
POWER_GOOD_OFF	Read/Write Word	5Fh	Sets the output voltage at which an optional POWER_GOOD signal should be negated. Format according to VOUT_MODE.
TON_DELAY	Read/Write Word	60h	Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output

Restricted**IR35217 Digital Multi-phase Controller****8+o/7+1/6+2 Dual Output Digital Multi-Phase Controller****I₂C/PMBus Communication**

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
			voltage starts to rise. Exp = o.
TON_RISE	Read/Write Word	61h	Sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. Exp = o.
TON_MAX_FAULT_LIMIT	Read/Write Word	62h	Sets an upper limit, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit. Exp = o.
TON_MAX_FAULT_RESPONSE	Read/Write Byte	63h	Instructs the device on what action to take in response to a TON_MAX fault. Only shutdown and ignore are supported.
TOFF_DELAY	Read/Write Word	64h	Sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output. Exp = o.
TOFF_FALL	Read/Write Word	65h	Sets the time, in milliseconds, from the end of the turn-off delay time until the voltage is commanded to zero. Exp = o.
STATUS_BYTE	Read/Write Byte	78h	Returns 1 byte where the bit meanings are: Bit <7> Reserved Bit <6> Output off (due to fault or enable) Bit <5> Output over-voltage fault Bit <4> Output over-current fault Bit <3> Input Under-voltage fault Bit <2> Temperature fault Bit <1> Communication/Memory/Logic fault Bit <0>: Reserved
STATUS_WORD	Read/Write Word	79h	Returns 2 bytes where the Low byte is the same as the STATUS_BYTE data. The High byte has bit meanings are: Bit <7> Output high or low fault Bit <6> Output over-current fault Bit <5> Input under-voltage fault Bit <4> MFR_SPECIFIC Bit <3> POWER_GOOD# Bit <2:0> Reserved
STATUS_VOUT	Read/Write Byte	7Ah	Bit <7> Output Overvoltage Fault Bit <6> Output Overvoltage Warning Bit <5> Output Undervoltage Warning Bit <4> Output Undervoltage Fault Bit <3> VOUT_MAX Warning Bit <2> TON_MAX_FAULT Bit <1> Reserved Bit <0> Reserved
STATUS_IOUT	Read/Write Byte	7Bh	Bit <7> Output Overcurrent Fault Bit <6> Reserved Bit <5> Output Overcurrent Warning Bit <4> Reserved

Restricted**IR35217 Digital Multi-phase Controller****8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller****I₂C/PMBus Communication**

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
			Bit <3> Current Share Fault Bit <2:0> Reserved
STATUS_INPUT	Read/Write Byte	7Ch	Bit <7> Input Overvoltage Fault Bit <6> Reserved Bit <5> Input Undervoltage Warning Bit <4> Input Undervoltage Fault Bit <3> Unit Off For Insufficient Input Voltage Bit <2> Reserved Bit <1> Input Overcurrent Warning Bit <0> Reserved
STATUS_TEMPERATURE	Read/Write Byte	7Dh	Bit <7> Over Temperature Fault Bit <6> Over Temperature Warning Bit <5:0> Reserved
STATUS_CML	Read/Write Byte	7Eh	Returns 1 byte where the bit meanings are: Bit <7> Invalid or unsupported command Bit <6> Invalid or unsupported data Bit <5> PEC fault Bit <4:2> Reserved Bit <1> Other communication fault not listed here Bit <0> Reserved
STATUS_MFR_SPECIFIC	Read/Write Byte	80h	Returns 1 byte where the bit meanings are: Bit <7:4> Reserved Bit <3> Loss of SYNC Bit <2> Driver Fault Bit <1> Unpopulated Phase Bit <0> External Overtemperature Fault
READ_VIN	Read Word	88h	Returns the input voltage in Volts
READ_IIN	Read Word	89h	Returns the input current in Amperes
READ_VOUT	Read Word	8Bh	Returns the output voltage in the format set by VOUT_MODE
READ_IOUT	Read Word	8Ch	Returns the output current in Amperes
READ_TEMPERATURE_1	Read Word	8Dh	Returns the addressed loop NTC temperature in degrees Celsius
READ_TEMPERATURE_2	Read Word	8Eh	Returns the other loop NTC temperature in degrees Celsius
READ_DUTY_CYCLE	Read Word	94h	Returns the duty cycle of the PMBus device's main power converter in percent.
READ_POUT	Read Word	96h	Returns the output power in Watts
READ_PIN	Read Word	97h	Returns the input power in Watts
PMBUS_REVISION	Read Byte	98h	Reports PMBus Part I rev 1.1 & PMBUs Part II rev 1.2(draft)
MFR_ID	Block Read/Write Byte count = 2	99h	The MFR_ID is set to IR (ASCII 52 49) unless programmed different in the USER registers of the controller.
MFR_MODEL	Block Read, byte count = 1	9Ah	The MFR_Model is the same as the device ID if the USER register for Manufacturer model is 00. Otherwise MFR_Model command returns the value in the USER register for MFR_Model.

I₂C/PMBus Communication

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
MFR_REVISION	Block Read, byte count = 2	9Bh	The MFR_Revision is the same as the device revision if the USER register for Manufacturer revision is 00. Otherwise MFR_Revision command returns the value in the USER register for MFR_Revision.
MFR_DATE	Block Read/Write Byte count = 2	9Dh	The MFR_DATE command returns the value in the USER register called MFR_DATE
IC_DEVICE_ID	Block Read	ADh	Returns a 1 byte code with the following values: 5F = IR35217
IC_DEVICE_REV	Block Read	AEh	The IC revision that is stored inside the IC
MFR_READ_REG	Custom MFR protocol	D0h	Read I ₂ C registers
MFR_WRITE_REG	Write Word	D1h	Write to I ₂ C registers, High Byte is reg, low byte is data

11.6 11-bit Linear Format

Monitored parameters use the Linear Data Format (Figure 68) encoding into 1 Word (2 bytes), where:

$$\text{Value} = Y \times 2^N$$

Note N and Y are "signed" values. All commands, other than those using the format described by VOUT_MODE, use this format.

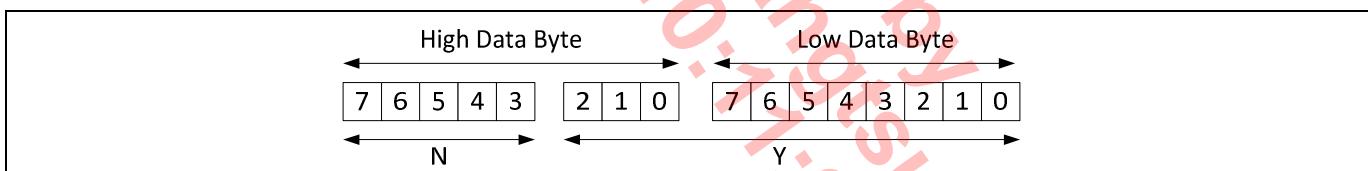


Figure 68 11-bit Linear Data Format

11.7 16-bit Linear Format

This format is only used for VOUT related commands (i.e. READ_VOUT, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, POWER_GOOD_ON, POWER_GOOD_OFF):

$$\text{Value} = Y \times 2^N$$

Note N and Y are "signed" values. If VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.

Restricted

IR35217 Digital Multi-phase Controller

8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller

I₂C/PMBus Communication

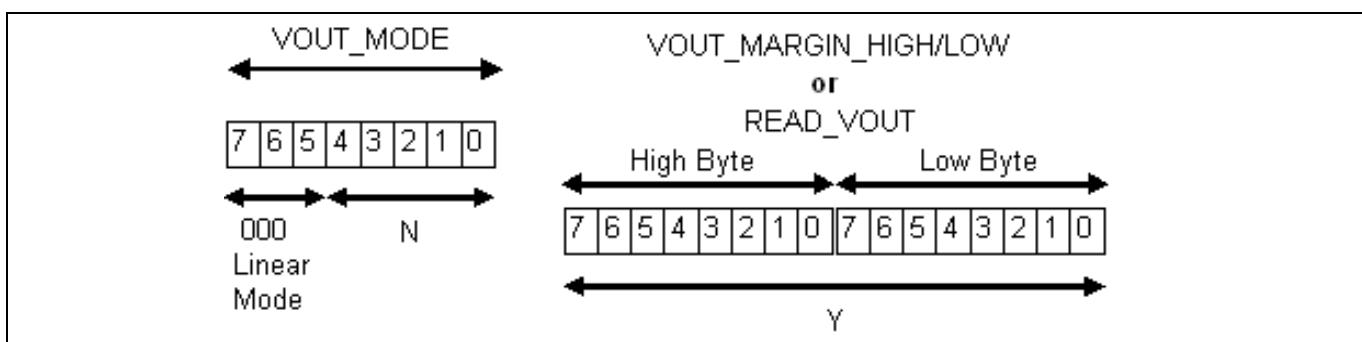


Figure 69 16-bit Linear Data Format

Downloaded by
IFXDMZpar-yangtsun
12/06/2019 10:11:22

Restricted

IR35217 Digital Multi-phase Controller

8+o/7+1/6+2 Dual Output Digital Multi-Phase Controller



Package

12 Package

12.1 Marking Information

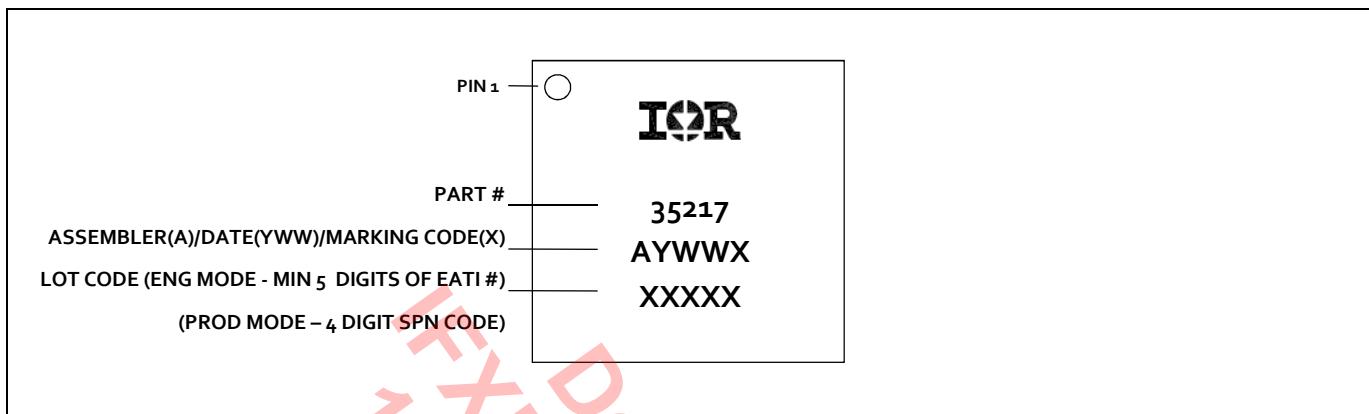


Figure 70 Package Marking

12.2 Dimensions

QFN 7x7mm, 56-pin

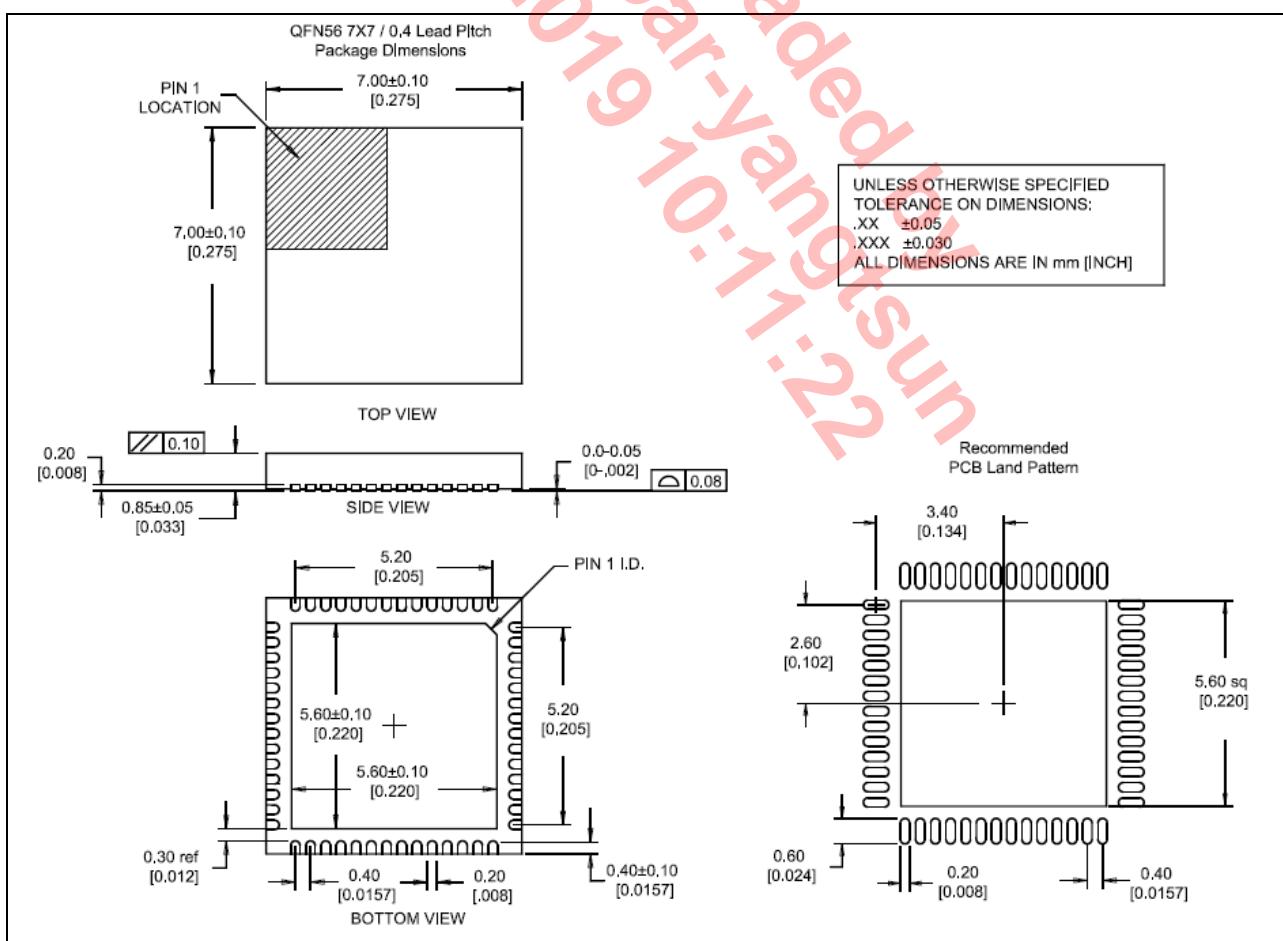


Figure 71 Package Dimensions

12.3 Environmental Qualifications

Table 52

Qualification Level		Industrial	
Moisture Sensitivity		QFN Package	MSL ₂
ESD	Human Body Model	JESD22-A114-E	
	Machine Model	JESD22-A115-A	
	Charged Device Model	JESD22-C101-C	
	Latch-up	JESD78	
RoHS Compliant		Yes	

Downloaded by
IFXDMZpar-yangtsun
12/06/2019 10:11:22

13 References

[1] UN0053 Salem IR35217 Customer Register Map

[2] UN0044 Salem PMBus Command Set

[3] AN0041 IR35217_IR3599_Doubler Mode

Downloaded by
IFXDMZpar-yangtsun
12/06/2019 10:11:22

Revision History

Revision History

Major changes since the last revision

Revision	Description of change	Date	Modified by	Approved by
2.0	Add AMD telemetry BW infor to ELEC CHAR table	2/7/2018	D Caron	D Williams
1.9	Change to Infineon Format Update table 13 'off' values to F6-FF	11/27/2017	T. Bellefeuille	D. Caron D. Williams
1.8	Add PWROK and SVT/SVD ratings to ELEC CHAR Table	8/10/2017	D. Caron	
1.7	Page 12: Update IOUT_ALERT# assert timing in Electrical characteristics Table Page 19: Update Table 3 with standard resistor values Page 35: Add AVP voltage as a function of IOUT Page 47: Add max IOUT_ALERT# timing delay and max OCP set point tolerance details to FAST OCP and IOUT_ALERT#	8/30/2016	D. Caron	David Williams Vijay Viswanathan
1.6	-Add ICC max rating...52mA -Change ICC typ from 48mA to 44mA -Update APPs drawing to show CFILT connected to REFIN pins on IR3555	7/8/2016	D. Caron	D. Williams
1.5	Remove References to VR13, SETWP, and ATL Mode, ADD ESD rating Table,	1/17/2016	D. Caron	D. Williams
1.4	Fix 51 typo and formatting errors per R. Baake review	10/7/2015	D. Caron	
1.3	Page 9; add GBD note to input OVP Page 10; change IR3555 temp slope from 0.488 to 4.88mV/C, change fault min to 1.45V (from 1.4V)	9/25/2015	D. Caron	
1.2	Change Header from Final to Preliminary Page 23; change SV_ALERT# to VR_READY Page 24; update SetWP paragraph, Page 25; reword start-up sequence description Page 30; update unused phases description Page 34; update Table 47 reference Page 42; update table 26 register names, fix off_time_adjust, add PSx command to PS4 exit description Page 46: Table 43 update register names Page 58; fix 11 bit linear format info, fix 16 bit format issue, add VOUT_COMMAND to list	8/11/2015	D. Caron	
1.1	Page 1; update IMVP8 REV to 1.2, remove reference to DPDC GUI Page 14; add 6.25mV/code detail Page 25; complete WP example table Page 32; add 100mS de-assert detail, Page 33; add R1, R2 to Figure 27 Page 59; Change Table 51 to Table 54 in description sentence	8/7/2015	D. Caron	
1.0	Change header to Final R4 Si Page 10 – change SVID HIGH min to 0.65V Page 12 – Remove note 3	7/15/15	D. Caron	
0.2	Page 1 – add -40 to 125 Junction; REV 03 Si Page 1 – add Fast overcurrent flag bullet Page 2 – Pin Diagram...change VCPU to VSEN Page 4-Application Diagram (Figure 3) Add 'optional' box around I_IN sense circuit Fix VSEN VRTN polarity Add R divider to TSEN and TSEN2 Page 9 – increase system accuracy range to -40 to 125 Junction	6/09/15	Don Caron	David Williams Vijay Viswanathan

Restricted

IR35217 Digital Multi-phase Controller

8+0/7+1/6+2 Dual Output Digital Multi-Phase Controller



Revision History

Revision	Description of change	Date	Modified by	Approved by
	Page 10 – change SVID HIGH min to 0.665V Page 12-remove note 2 (freq change with # phases) add note 2 (OTP limit = 134 with NTC), Page 12 -add NOTE 3 disclaimer on SVID HIGH SPEC Page 15 – update Figure 6, update Real Time Monitoring Page 14--Replace Figure 4 and Figure 5 Page 18--Replace figure 12 and 13 Page 37--Replace Figure 34 and 35 Page 38--Replace Figure 37 Page 40--Replace Figure 39, 40, 41 Page 45--Update TABLE 41 Page 46—Add table of FAST IOUT_ALERT# registers Page 54—remove reference to UN0030. Use AN0031 Update Figures 57 and 58...PMBUS BLOCK READ commands Update Table #'s and Figure #'s...out of sequence			
0.1	Advanced Release	2/09/15	Don Caron	

Trademarks of Infineon Technologies AG

μHVIC™, μPM™, μPFC™, AU-ConvertIR™, AURIX™, C166™, CanPAK™, CIPOST™, CIPURSE™, CoolIDP™, CoolGaN™, COOLiR™, CoolMOS™, CoolSET™, CoolSiC™, DAVE™, DI-POL™, DirectFET™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, GaNpowIR™, HEXFET™, HITFET™, HybridPACK™, iMOTION™, IRAM™, ISOFACE™, IsoPACK™, LEDrivIR™, LITIX™, MIPAO™, ModSTACK™, my-d™, NovalithIC™, OPTIGA™, OptiMOS™, ORIGA™, PowIRaudio™, PowIRStage™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SIL™, RASIC™, REAL3™, SmartLEWIS™, SOLID FLASH™, SPOCT™, StrongIRFET™, SupIRBuck™, TEMPFET™, TRENCHSTOP™, TriCore™, UHVIC™, XHP™, XMC™

Trademarks updated November 2015

Other Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2018-02-07

Published by

Infineon Technologies AG
81726 München, Germany

© 2018 Infineon Technologies AG.
All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

IR35217

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

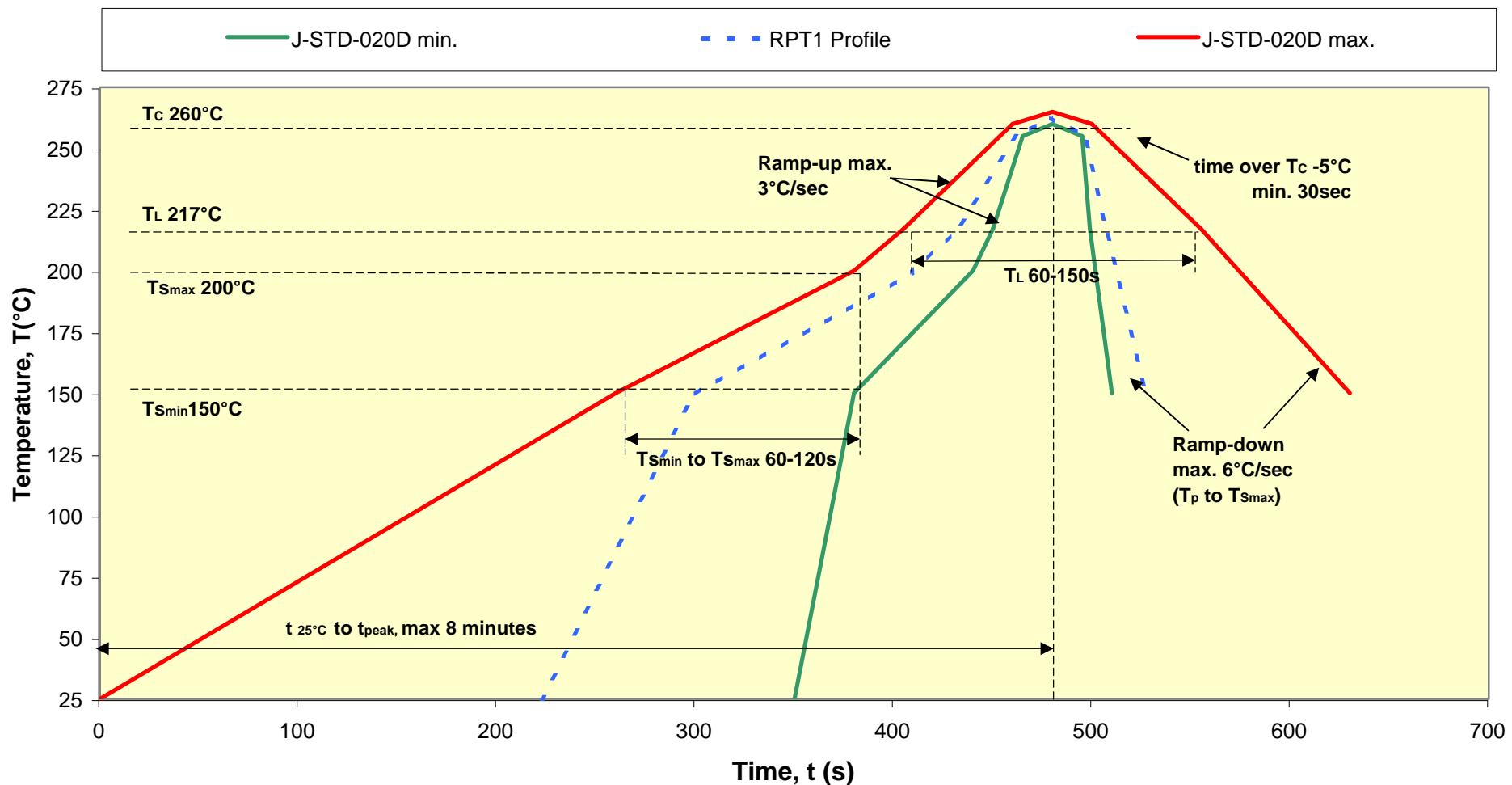
For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

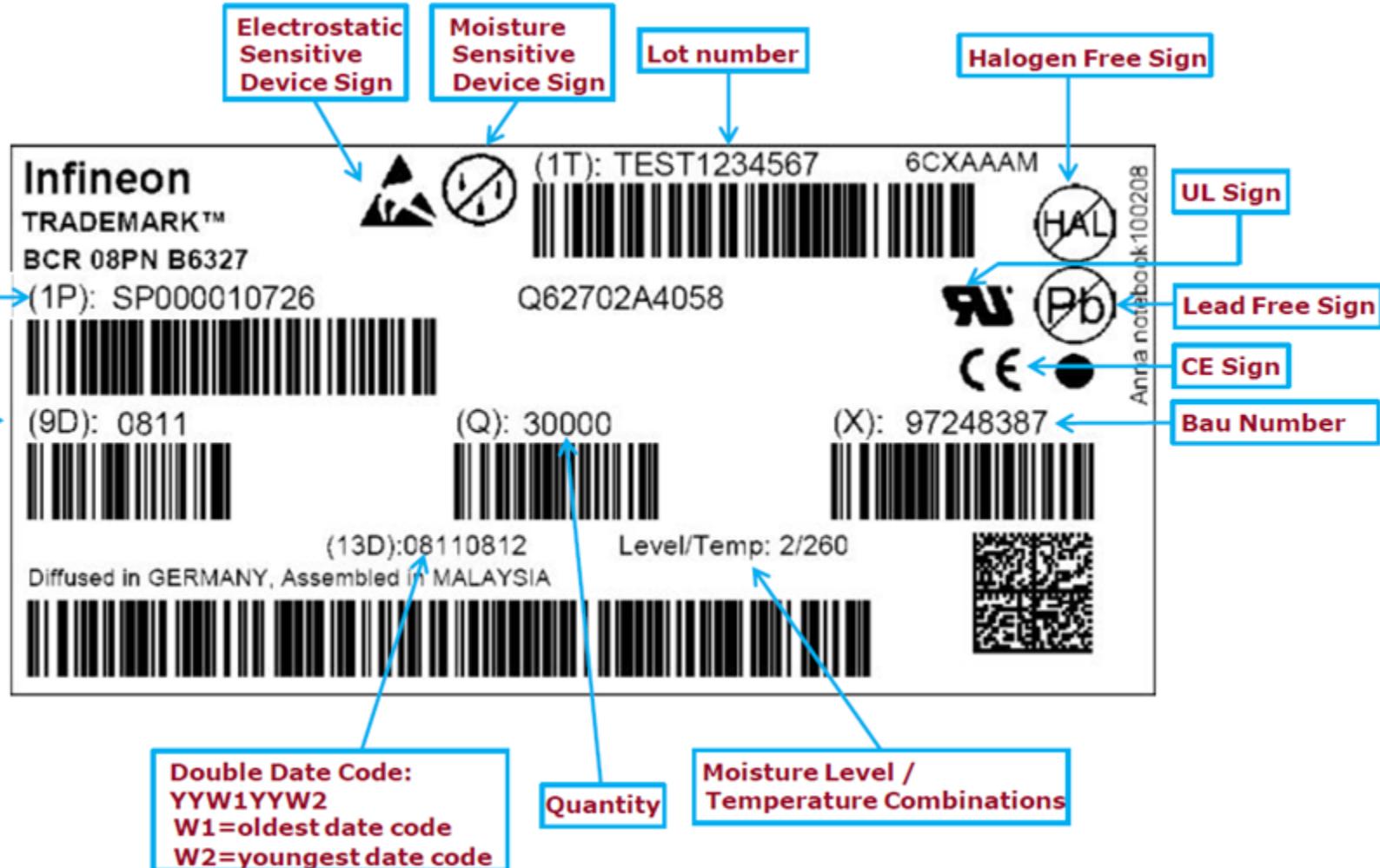
Reflow Profile according J-STD-020D 260°C (-0), Pbfree Assembly



Infineon Barcode Product Label & Merging Rule



Example of Barcode Product Label



Merging Rule

- Maximum 2 date codes can be merged to a Merged Label Lot (MLL).
- The older lot number is shown at (9D), whereas 2 date codes of the merged lots are shown at (13D).
- The printed label may contain 2 date codes and is applied for one batch of packing, which several reels can be packed. The parts in reels may be one date code in some reels, but also may be 2 date codes in a reel.
- Infineon logistic system is able to trace back the merged date codes if the label lot number at (1T) is provided.



Description	ALL	Remark
Maximum number of Date Codes in a Merged Label Lot	2	If the date code is visible marked on devices then max 2 date codes can be merged to a MLL
Date code	YYW1	YYW1 = date code of the oldest lot number; id = (9D) will be generate automatically within MRLT
Date code for merged lot numbers	YYW1YYW2	Oldest DC (YYW1) by id = (9D) and Human readable only (YYW1YYW2) by id = (13D)