

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
A	0011206598	PRODUCTION RELEASED	2018-02-13

J71B MLB\_A

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-02542	1	SCHEM,MLB-A,YN,J71B	SCH1	CRITICAL	
820-00996	1	PCBF,MLB-A,YN,J71B	PCB1	CRITICAL	

LAST\_MODIFICATION= Tue Feb 13 14:37:32 2018

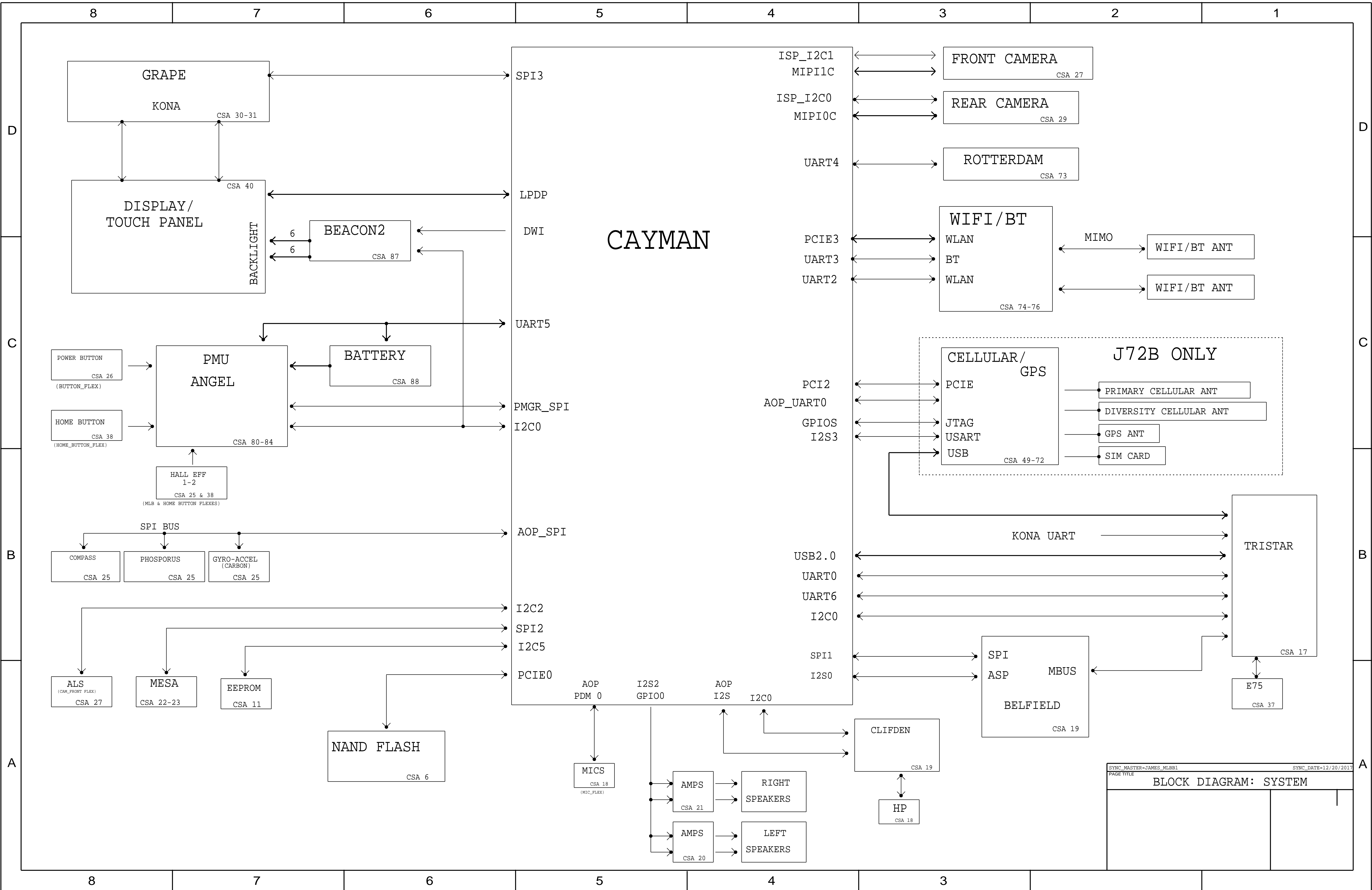
PAGE	CSA	CONTENTS	SYNC	DATE
1	1	TABLE OF CONTENTS		
2	2	BLOCK DIAGRAM: SYSTEM	JAMES_MLBB1	12/20/2017
3	4	BOM TABLES	J71S_MLB_B	01/27/2017
4	5	SOC: MISC & ALIASES	JAMES_MLBB1	12/20/2017
5	6	NAND	JAMES_MLBB1	12/20/2017
6	7	SOC:JTAG,USB,XTAL	JAMES_MLBB1	12/20/2017
7	8	SOC:PCIE	JAMES_MLBB	08/21/2017
8	9	SOC:MIPI AND ISP	JAMES_MLBB1	12/20/2017
9	10	SOC:LPDP	JAMES_MLBB1	12/20/2017
10	11	SOC:SERIAL	JAMES_MLBB1	12/20/2017
11	12	SOC:GPIO & UART	JAMES_MLBB1	12/20/2017
12	13	SOC:AOP	JAMES_MLBB1	12/20/2017
13	14	SOC:POWER (1/3)	JAMES_MLBB1	12/20/2017
14	15	SOC:POWER (2/3)	JAMES_MLBB1	12/20/2017
15	16	SOC:POWER (3/3)	JAMES_MLBB1	12/20/2017
16	17	IO: TRISTAR	JAMES_MLBB1	12/20/2017
17	18	AUDIO: HP/DMIC FLEX CONNS	JAMES_MLBB1	12/20/2017
18	19	AUDIO: CLIFDEN & BELFIELD	JAMES_MLBB1	12/20/2017
19	20	AUDIO: SPEAKER AMPS LEFT	JAMES_MLBB1	12/20/2017
20	21	AUDIO: SPEAKER AMPS RIGHT	JAMES_MLBB1	12/20/2017
21	22	SENSOR: MESA SUPPORT	JAMES_MLBB1	12/20/2017
22	23	SENSOR: MESA BOOST	JAMES_MLBB1	12/20/2017
23	25	SENSOR: HALL, CARBON, COMPASS, PHOS	JAMES_MLBB1	12/20/2017
24	26	IO: BUTTON FLEX CONN	JAMES_MLBB1	12/20/2017
25	27	CAMERA: FF AND ALS CONN	JAMES_MLBB1	12/20/2017
26	29	CAMERA: REAR CONN & FILTERS	JAMES_MLBB1	12/20/2017
27	30	TOUCH: KONA #1	JAMES_MLBB1	12/20/2017
28	31	TOUCH: KONA #2	JAMES_MLBB1	12/20/2017
29	32	TOUCH: CONNS	JAMES_MLBB1	12/20/2017
30	37	IO: FLEX HOTBAR & FILTERS	JAMES_MLBB1	12/20/2017
31	38	SENSOR-BTN: HALL, HOME & MESA	JAMES_MLBB1	12/20/2017
32	41	DISPLAY: EDP CONN	JAMES_MLBB1	12/20/2017
33	49	RADIOS: ALIASES	J71S_MLB_B	01/27/2017
34	74	SECURE ELEMENT	SECUREELEMENT	02/13/2018
35	75	WIFI/BT: MODULE	WIFI_MLB	11/16/2017
36	76	WIFI/BT: J71B FRONT END	WIFI_MLB	11/16/2017
37	81	POWER: ANGEL (1/5)	JAMES_MLBB1	12/20/2017
38	82	POWER: ANGEL (2/5)	JAMES_MLBB1	12/20/2017
39	83	POWER: ANGEL (3/5)	J71S_MLB_B	01/27/2017
40	84	POWER: ANGEL (4/5)	JAMES_MLBB1	12/20/2017
41	85	POWER: ANGEL (5/5)	JAMES_MLBB1	12/20/2017
42	86	POWER: EXTERNAL SWITCHES & LDOS	JAMES_MLBB1	12/20/2017
43	87	POWER: BUCKS 4,5,8	JAMES_MLBB1	12/20/2017
44	88	BEACON2	JAMES_MLBB1	12/20/2017
45	89	POWER: BATTERY CONNECTOR	JAMES_MLBB1	12/20/2017

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## TABLE OF CONTENTS

SYNC_MASTER=J71S_MLB_B	SYNC_DATE=01/27/2017
DRAWING TITLE	

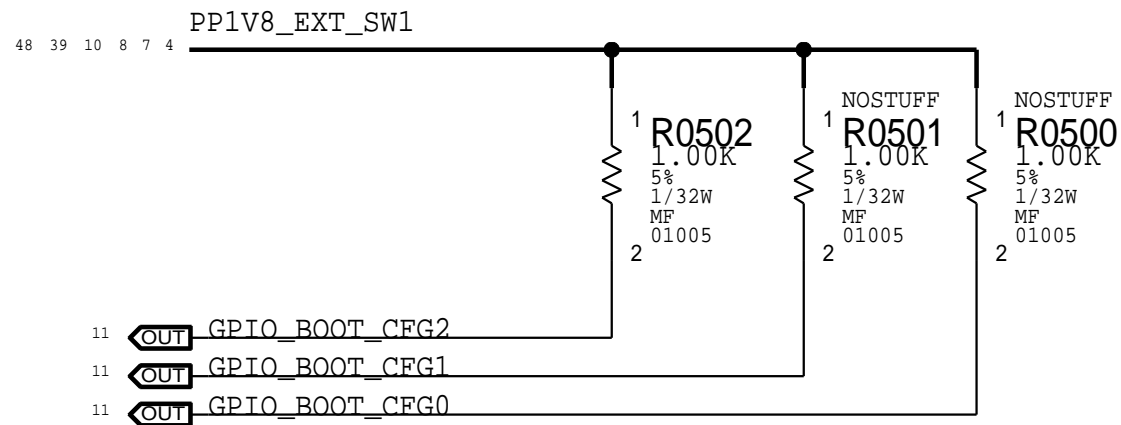
SCHEM,MLB-A,YN,J71B		



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D	<div>Page Notes</div> <div>Power aliases required by this page: (NONE)</div> <div>Signal aliases required by this page: (NONE)</div> <div>BOM options provided by this page:</div>			<div>SOC</div> <table><tr><th>PART#</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DESIGNATOR(S)</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>339S00485</td><td>1</td><td>POP,C39988+208 2088-BJ,A12,180J,H,C395467</td><td>U0700</td><td>CRITICAL</td><td></td></tr></table> <div>S H</div> <table><tr><th>PART NUMBER</th><th>ALTERNATE FOR PART NUMBER</th><th>BOM OPTION</th><th>REF DES</th><th>COMMENTS:</th></tr><tr><td>339S00486</td><td>339S00485</td><td></td><td>U0700</td><td></td></tr><tr><td>339S00487</td><td>339S00485</td><td></td><td>U0700</td><td></td></tr></table>		PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	339S00485	1	POP,C39988+208 2088-BJ,A12,180J,H,C395467	U0700	CRITICAL		PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	339S00486	339S00485		U0700		339S00487	339S00485		U0700				<div>RDAR #22886293</div> <table><tr><th>PART NUMBER</th><th>ALTERNATE FOR PART NUMBER</th><th>BOM OPTION</th><th>REF DES</th><th>COMMENTS:</th></tr><tr><td>155S00007</td><td>155S0667</td><td></td><td></td><td>L2710,L2711,L2910,L2911,L2912,L2913,L2920</td></tr></table> <div>138S00049</div> <table><tr><td>138S00049</td><td>138S0831</td><td></td><td>C0610,C0800,....</td><td>2.20P 0201</td></tr></table> <div>138S00006</div> <table><tr><td>138S00006</td><td>138S0835</td><td></td><td>C0900,C0800,....</td><td>4.30P</td></tr></table> <div>138S00048</div> <table><tr><td>138S00048</td><td>138S00003</td><td></td><td>C0140,C0141,....</td><td>150P</td></tr></table> <div>138S0945</div> <table><tr><td>138S0945</td><td>138S0739</td><td></td><td>C1760,....</td><td>10P</td></tr></table> <div>138S0706</div> <table><tr><td>138S0706</td><td>138S0739</td><td></td><td>C1760,....</td><td>10P</td></tr></table> <div>376S00071</div> <table><tr><td>376S00071</td><td>376S00070</td><td></td><td>Q0504</td><td></td></tr></table> <div>376S00159</div> <table><tr><td>376S00159</td><td>376S1211</td><td></td><td>Q0550</td><td></td></tr></table> <div>376S0948</div> <table><tr><td>376S0948</td><td>376S00076</td><td></td><td>Q0900</td><td></td></tr></table>		PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	155S00007	155S0667			L2710,L2711,L2910,L2911,L2912,L2913,L2920	138S00049	138S0831		C0610,C0800,....	2.20P 0201	138S00006	138S0835		C0900,C0800,....	4.30P	138S00048	138S00003		C0140,C0141,....	150P	138S0945	138S0739		C1760,....	10P	138S0706	138S0739		C1760,....	10P	376S00071	376S00070		Q0504		376S00159	376S1211		Q0550		376S0948	376S00076		Q0900																		
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A	<div>MECHANICAL PARTS</div> <table><tr><th>PART#</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DESIGNATOR(S)</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>806-13579</td><td>1</td><td>FENCE,AP,J71B</td><td>PD_FENCE_AP</td><td>CRITICAL</td><td></td></tr><tr><td>806-13581</td><td>1</td><td>CAN,TINY,J71B</td><td>PD_TINY_CAN</td><td>CRITICAL</td><td></td></tr></table> <div>PART NUMBER</div> <div>ALTERNATE FOR PART NUMBER</div> <div>BOM OPTION</div> <div>REF DES</div> <div>COMMENTS:</div>			PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	806-13579	1	FENCE,AP,J71B	PD_FENCE_AP	CRITICAL		806-13581	1	CAN,TINY,J71B	PD_TINY_CAN	CRITICAL		<div>BARCODE LABEL/EEEE CODES</div> <table><tr><th>PART#</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DESIGNATOR(S)</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>825-7639</td><td>1</td><td>EEEE FOR BETTER</td><td>HWTW</td><td>CRITICAL</td><td>EEEE_J71B_BETTER</td></tr><tr><td>825-7639</td><td>1</td><td>EEEE FOR BEST</td><td>J8YQ</td><td>CRITICAL</td><td>EEEE_J71B_BEST</td></tr><tr><td>825-7639</td><td>1</td><td>EEEE FOR ULTIMATE</td><td>HYQQ</td><td>CRITICAL</td><td>EEEE_J71B_ULTIMATE</td></tr><tr><td>825-7639</td><td>1</td><td>EEEE FOR SUPREME</td><td>J8YR</td><td>CRITICAL</td><td>EEEE_J71B_SUPREME</td></tr></table>		PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	825-7639	1	EEEE FOR BETTER	HWTW	CRITICAL	EEEE_J71B_BETTER	825-7639	1	EEEE FOR BEST	J8YQ	CRITICAL	EEEE_J71B_BEST	825-7639	1	EEEE FOR ULTIMATE	HYQQ	CRITICAL	EEEE_J71B_ULTIMATE	825-7639	1	EEEE FOR SUPREME	J8YR	CRITICAL	EEEE_J71B_SUPREME	<div>SYNC_MASTER=J71S_MLB_B PAGE TITLE</div> <div>BOM TABLES</div>																																																	
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION																																																																																																		
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION																																																																																																		
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825-7639	1	EEEE FOR BEST	J8YQ	CRITICAL	EEEE_J71B_BEST																																																																																																		
825-7639	1	EEEE FOR ULTIMATE	HYQQ	CRITICAL	EEEE_J71B_ULTIMATE																																																																																																		
825-7639	1	EEEE FOR SUPREME	J8YR	CRITICAL	EEEE_J71B_SUPREME																																																																																																		
	8	7	6	5	4	3																																																																																																	

D

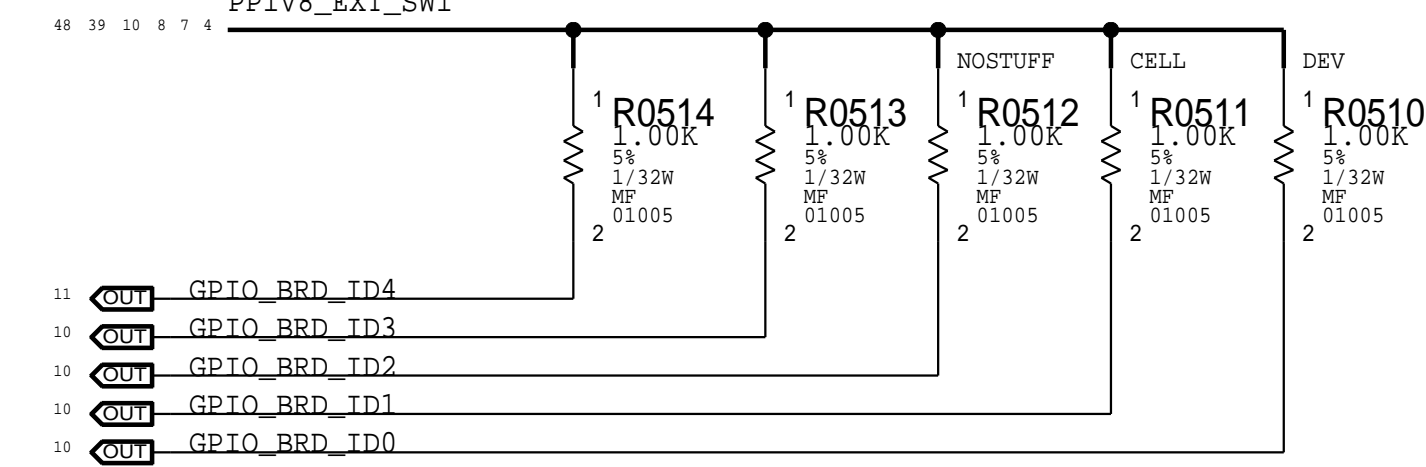
BOOT CONFIG ID



BOOT_CFG[2:0]	MODE	S/W READ FLOW
000	SPI0 TEST MODE	1. SET GPIO AS INPUT
001	SPI0 TEST MODE	2. DISABLE PU AND ENABLE PD
010	NVME0 X2 MODE	3. READ
011	NVME0 X2 TEST MODE	
100	NVME0 X1 MODE	
101	NVME0 X1 TEST MODE	
110	SLOW SPI0 TEST MODE	
111	FAST SPI0 TEST MODE	

C

BOARD ID

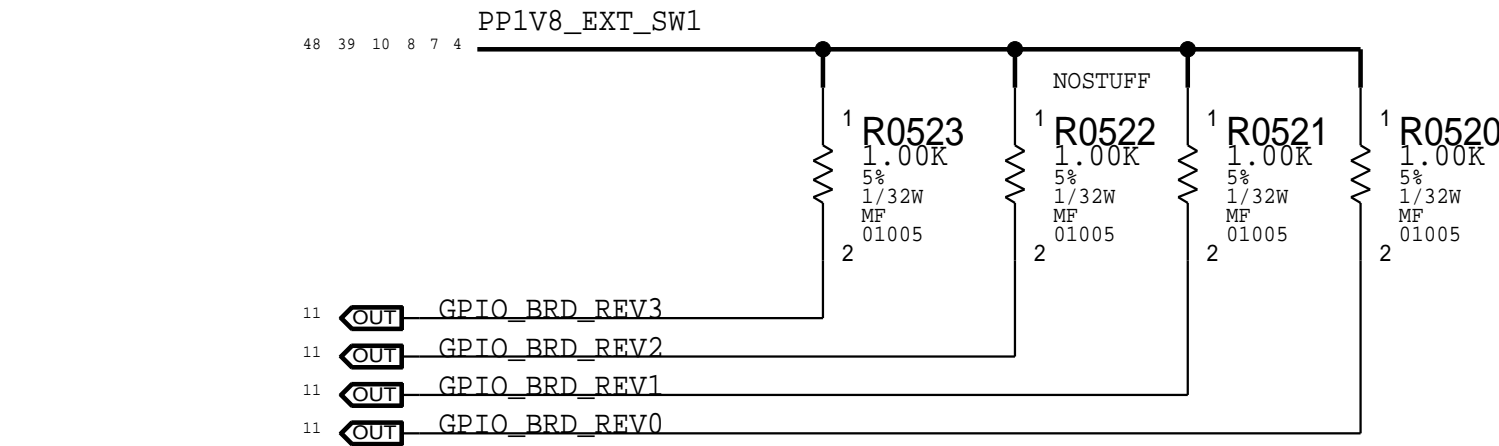


BRD_ID[4-0]
11000 J71B AP (WIFI)
11001 J71B DEV
11010 J72B AP (CELL)
11011 J72B DEV

RDAR//PROBLEM/29855408

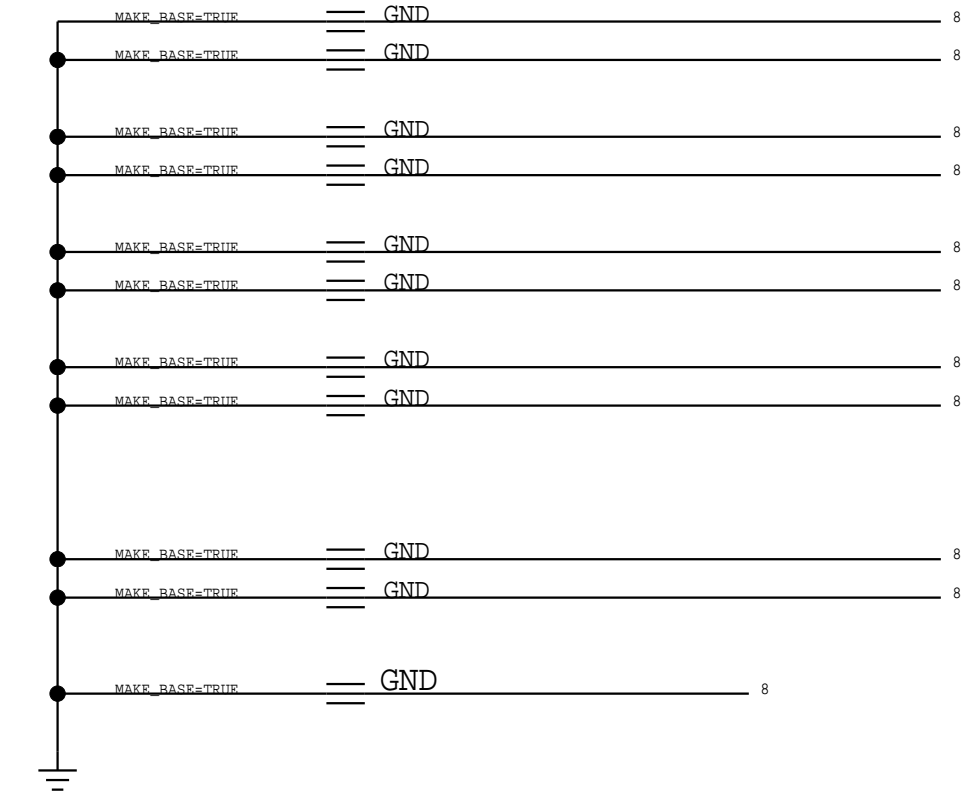
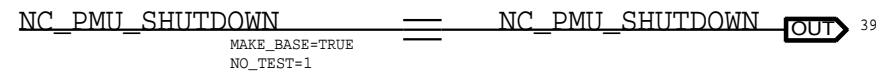
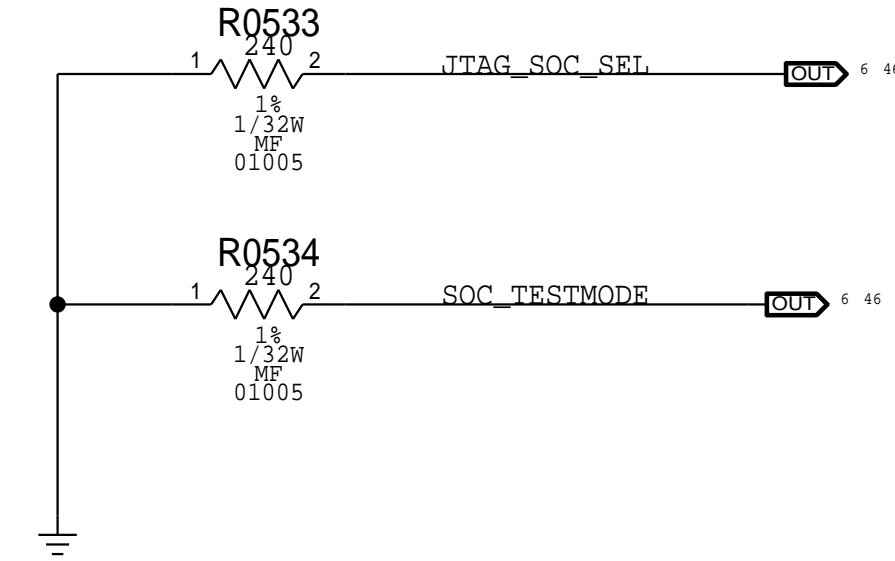
B

BOARD REVISION



BRD_REV[3-0]	S/W READ FLOW
1111 PROTO 0	1. SET GPIO AS INPUT
1110 PROTO 1	2. ENABLE PD AND DISABLE PU
1101 EVT	3. READ
1100 DVT	
----> 1011 PVT	

A



DC RESISTANCE FAI REQUIRED MEASUREMENTS			
FROM PIN (REFDES.PN)	TO PIN (REFDES.PN)	VALUE (MILIOHM) (OPTIONAL)	TOLERANCE (+/-) (OPTIONAL)
U8100.W19	J8900.4	3.75	10%
U8100.H16	L2700.1	187.0	10%

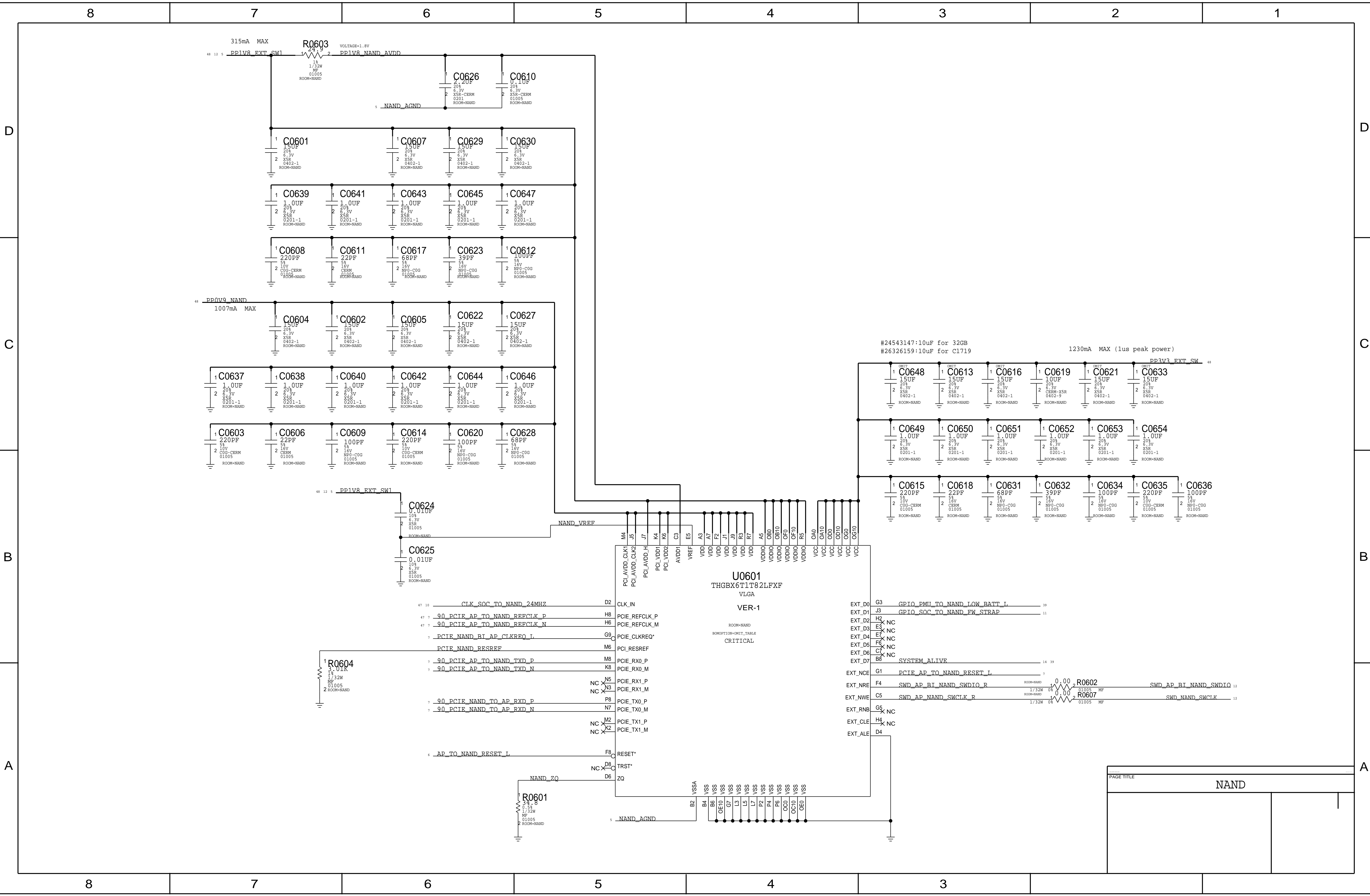
D

C

B

A



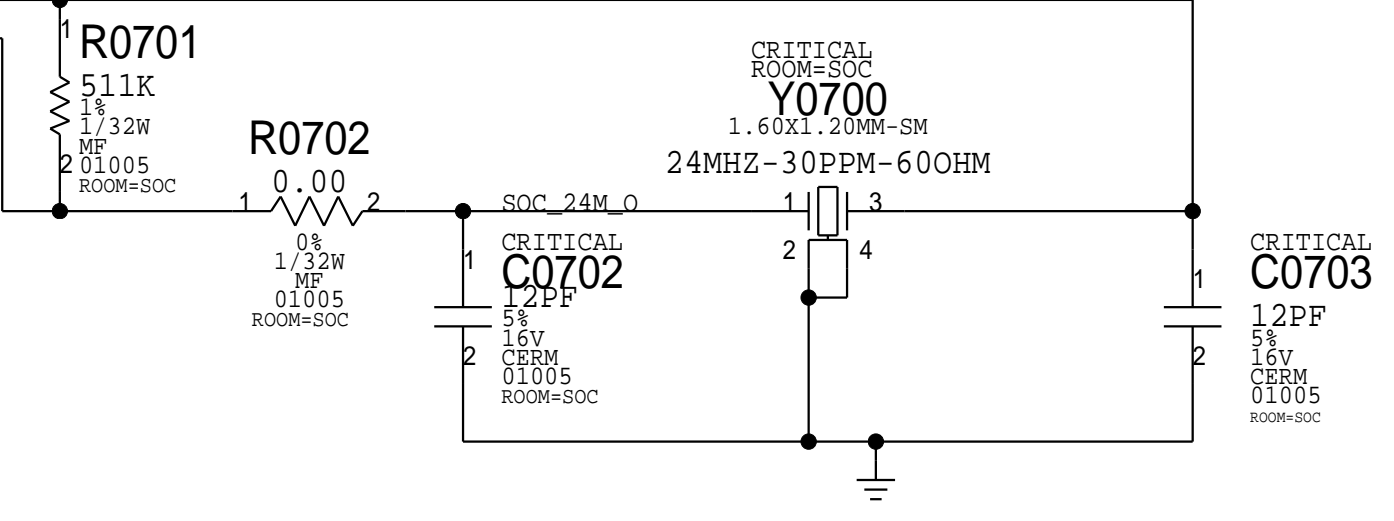
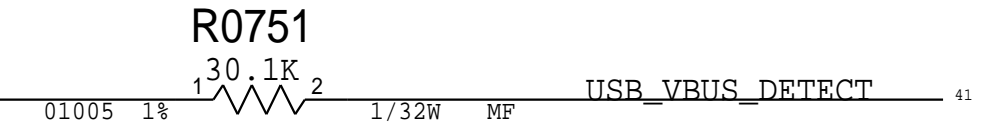
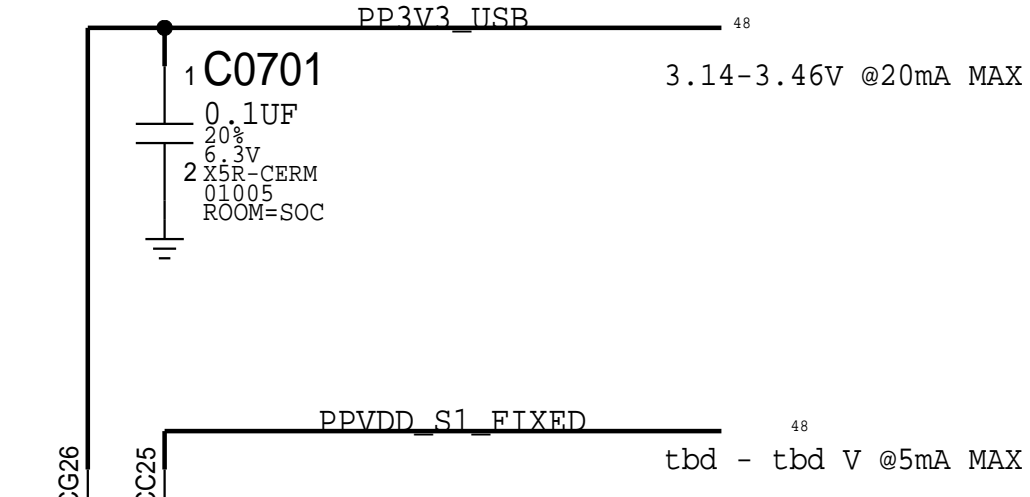
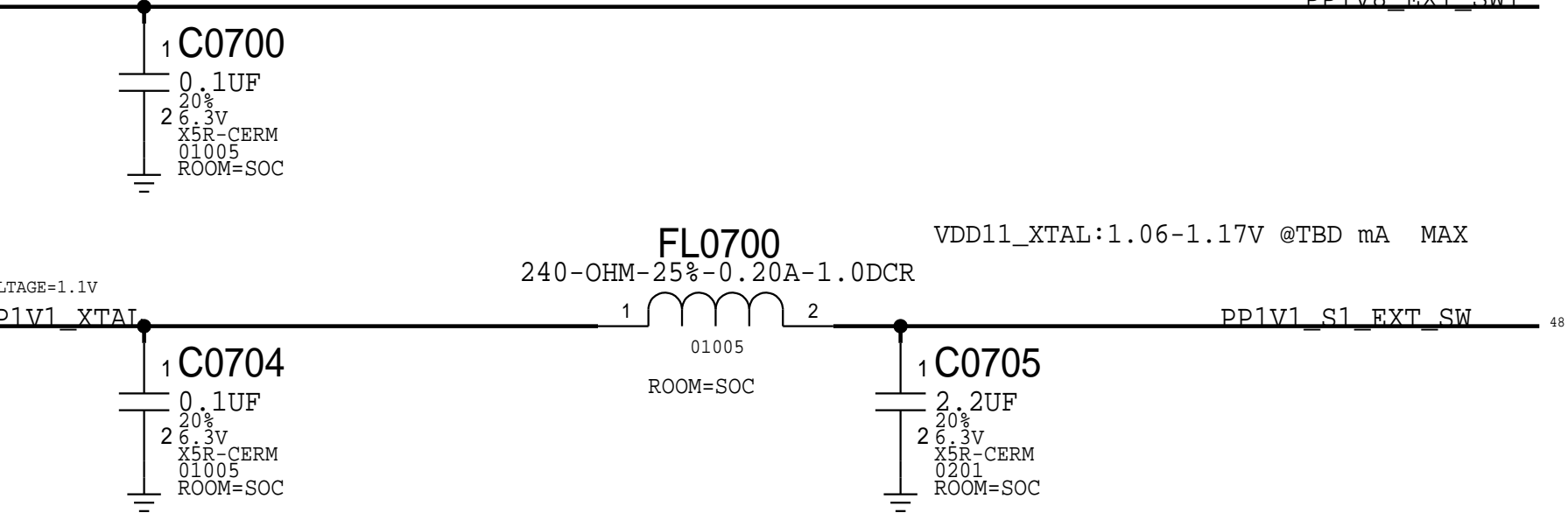
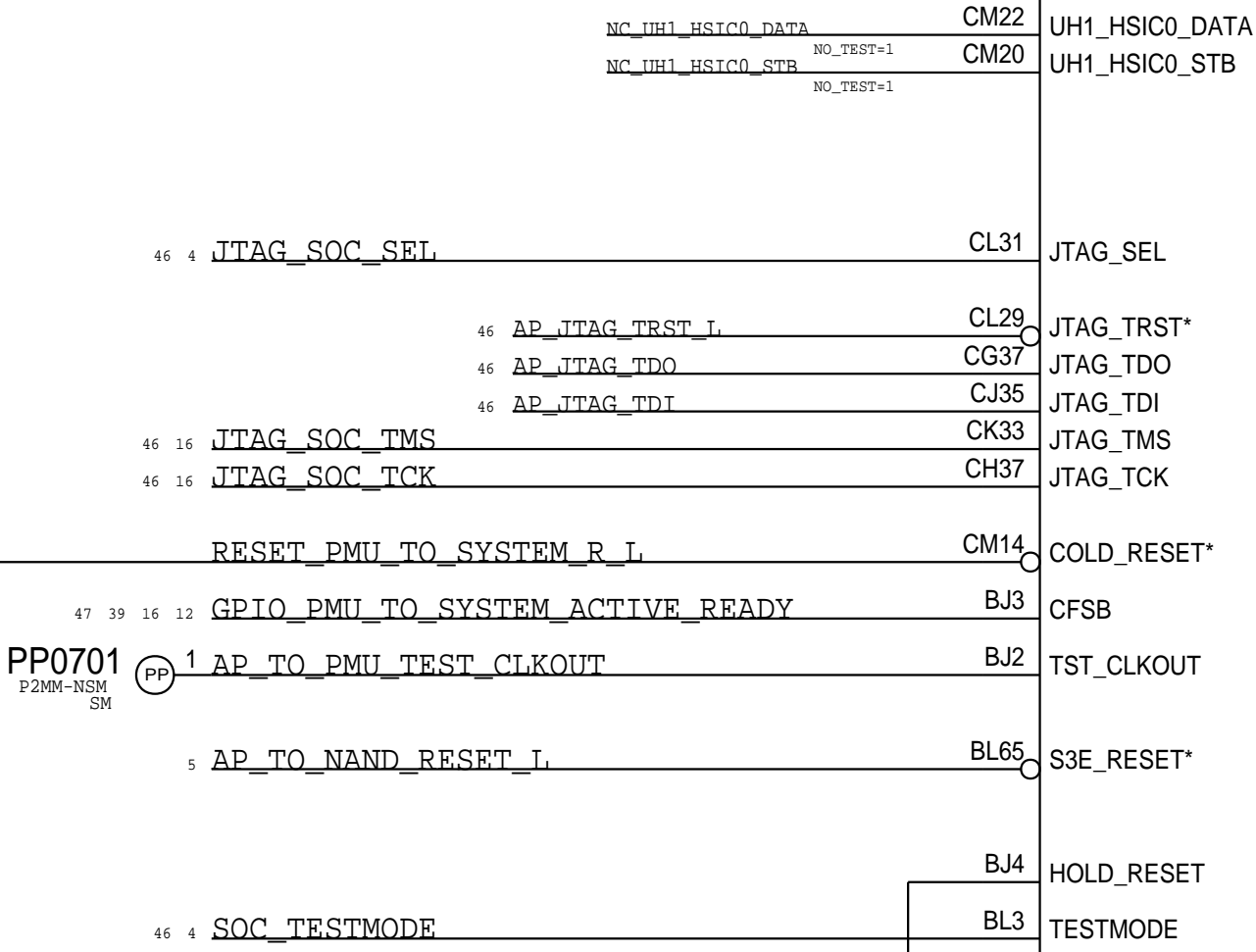
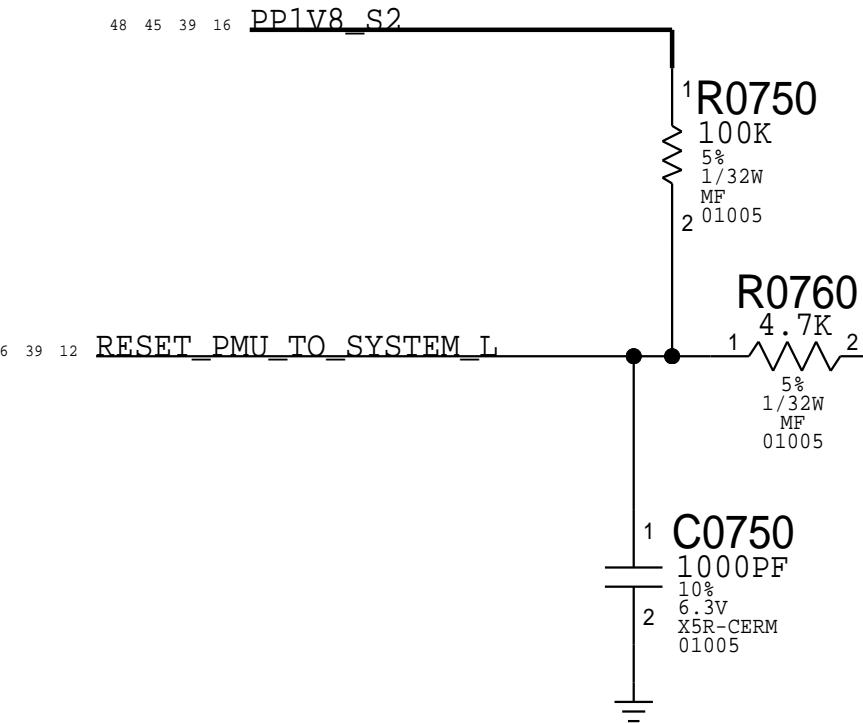


SOC - USB, JTAG, XTAL

VDD18\_USB: 1.71-1.89V @20mA MAX

VDD18\_AMUX: 1.62-1.98V @1mA MAX

VDD11\_XTAL:1.06-1.17V @TBD mA MAX



PAGE TITLE	
SOC:JTAG,USB,XTAL	

SOC - PCIE INTERFACES

D

C

B

A

D

C

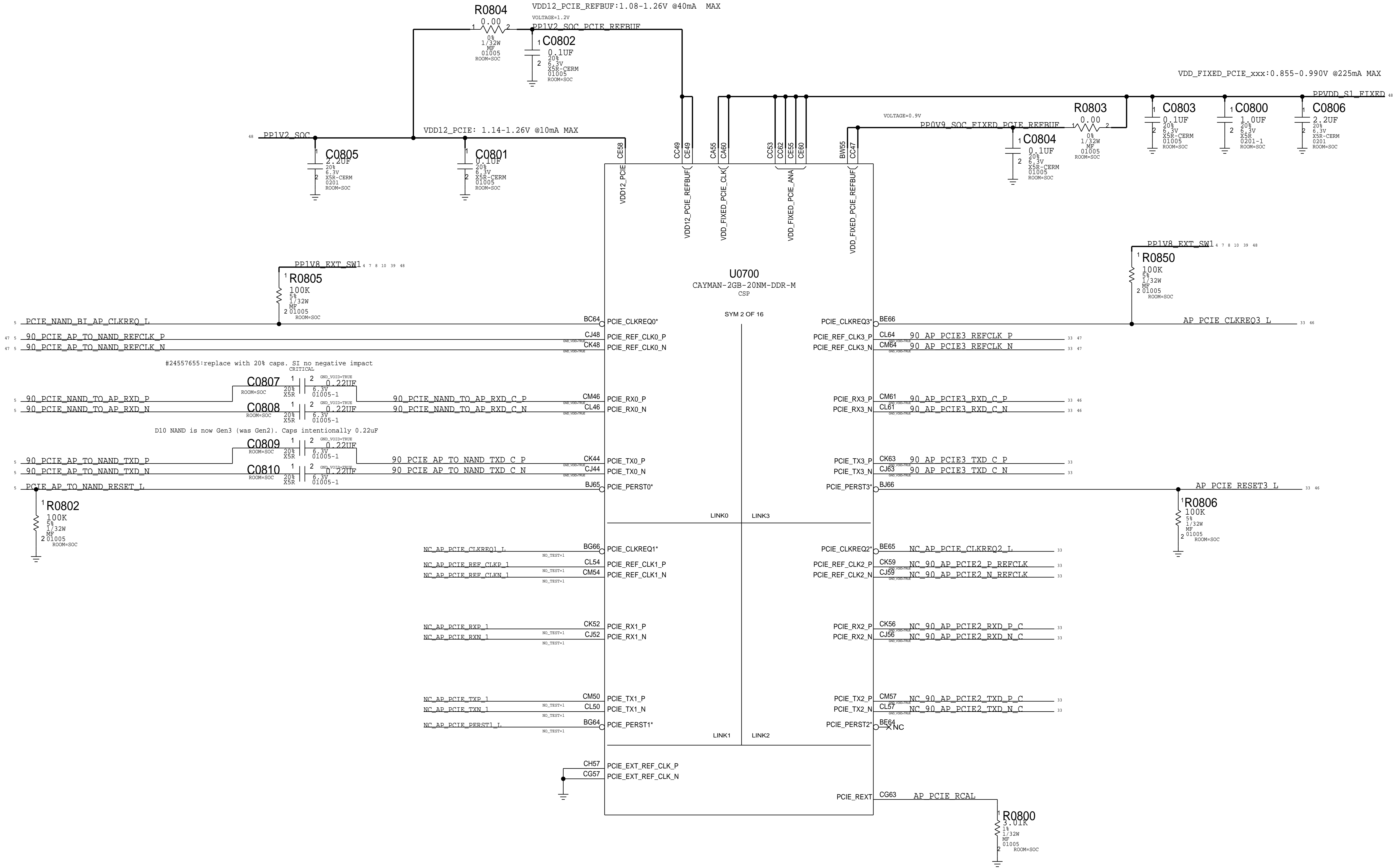
B

A

PCIE LINK 0

PCIE LINK 3

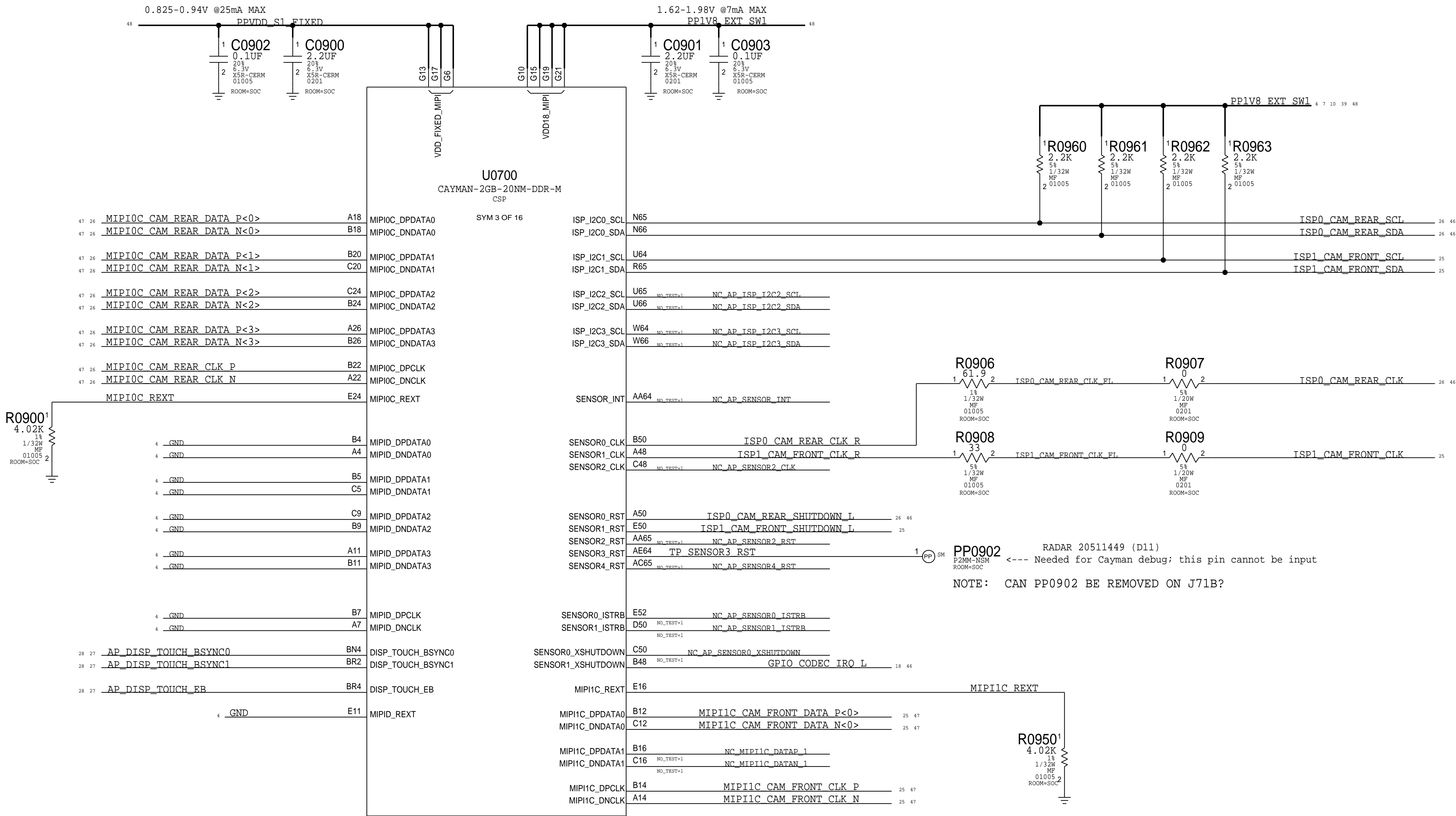
PCIE LINK 2



PAGE TITLE		
SOC:PCIE		



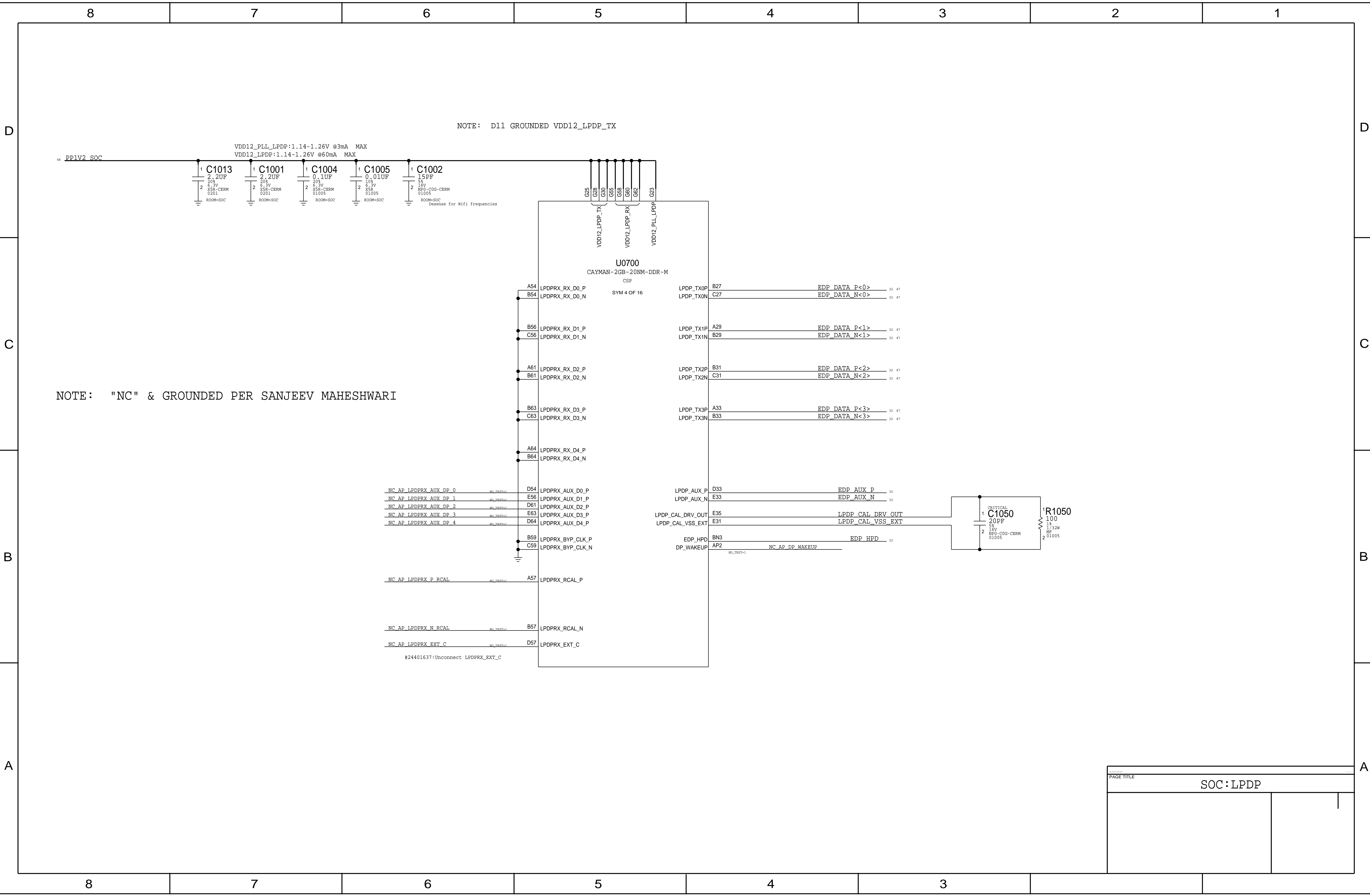
SOC - MIPI & ISP INTERFACES



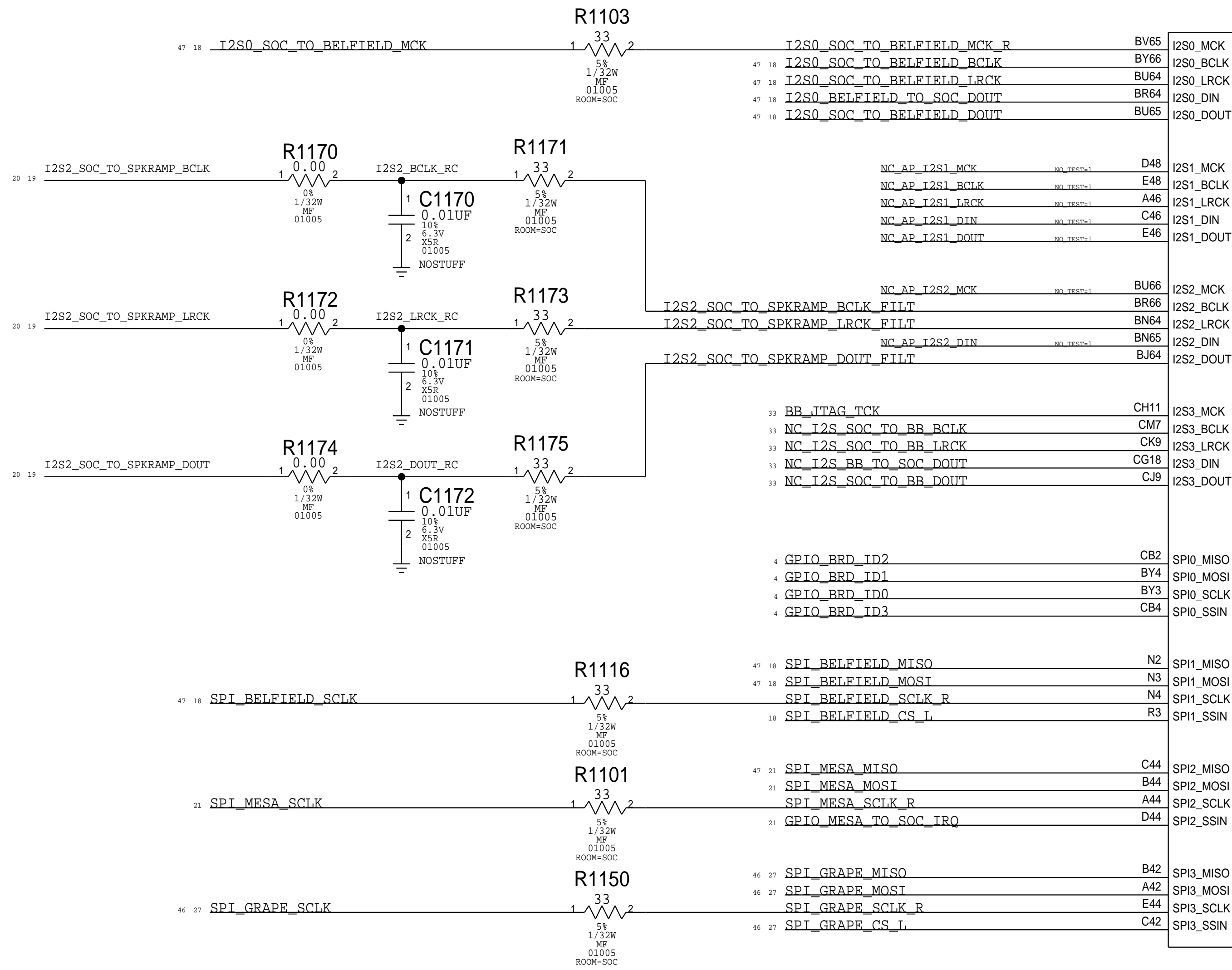
TO BE REVIEWED

PAGE TITLE	
SOC:MIPI AND ISP	





SOC - SERIAL INTERFACES



U0700  
CAYMAN-2GB-20NM-DDR-M  
CSP  
SYM 6 OF 16

I2S0\_MCK  
I2S0\_BCLK  
I2S0\_LRCK  
I2S0\_DIN  
I2S0\_DOUT

I2S1\_MCK  
I2S1\_BCLK  
I2S1\_LRCK  
I2S1\_DIN  
I2S1\_DOUT

I2S2\_MCK  
I2S2\_BCLK  
I2S2\_LRCK  
I2S2\_DIN  
I2S2\_DOUT

SPI0\_MISO  
SPI0\_MOSI  
SPI0\_SCLK  
SPI0\_SSIN

SPI1\_MISO  
SPI1\_MOSI  
SPI1\_SCLK  
SPI1\_SSIN

SPI2\_MISO  
SPI2\_MOSI  
SPI2\_SCLK  
SPI2\_SSIN

SPI3\_MISO  
SPI3\_MOSI  
SPI3\_SCLK  
SPI3\_SSIN

I2C0\_SCL  
I2C0\_SDA  
I2C1\_SCL  
I2C1\_SDA  
I2C2\_SCL  
I2C2\_SDA  
I2C3\_SCL  
I2C3\_SDA

SPI4\_SCLK  
SPI4\_MISO  
SPI4\_MOSI

I2C5\_SCL  
I2C5\_SDA

GPIO\_42  
GPIO\_43

PMU\_SCLK  
PMU\_MISO  
PMU\_MOSI  
DWT\_CLK  
DWT\_DO

DROOP  
GPU\_TRIGGER  
SOCHOT

CLK32K\_OUT  
NAND\_SYS\_CLK

I2C0\_SCL\_1V8  
I2C0\_SDA\_1V8  
NC\_AP\_I2C1\_SCL  
NC\_AP\_I2C1\_SDA  
I2C2\_SCL\_1V8  
I2C2\_SDA\_1V8  
NC\_AP\_I2C3\_SCL  
NC\_AP\_I2C3\_SDA

NC\_AP\_SPI4\_SCLK  
NC\_AP\_SPI4\_MISO  
NC\_AP\_SPI4\_MOSI

I2C5\_SCL  
I2C5\_SDA

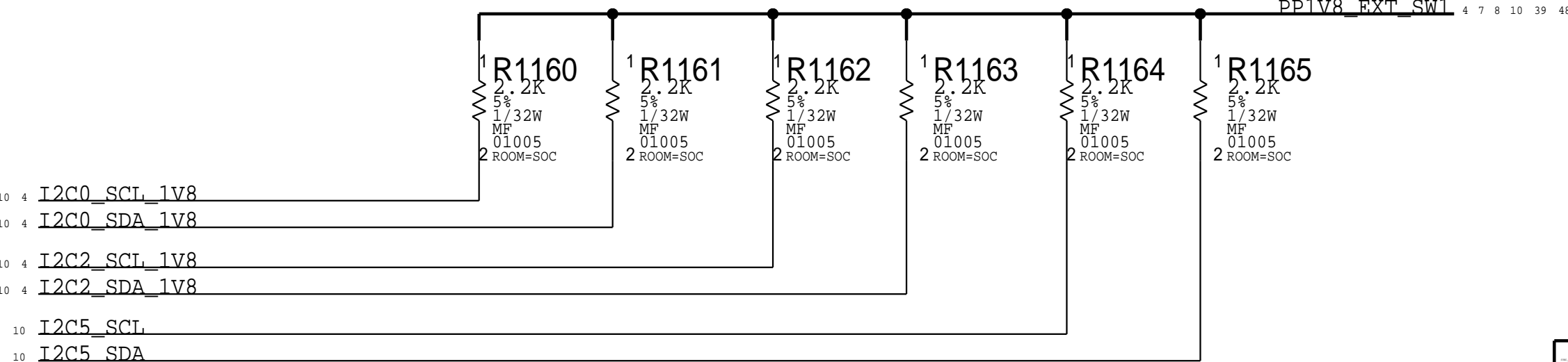
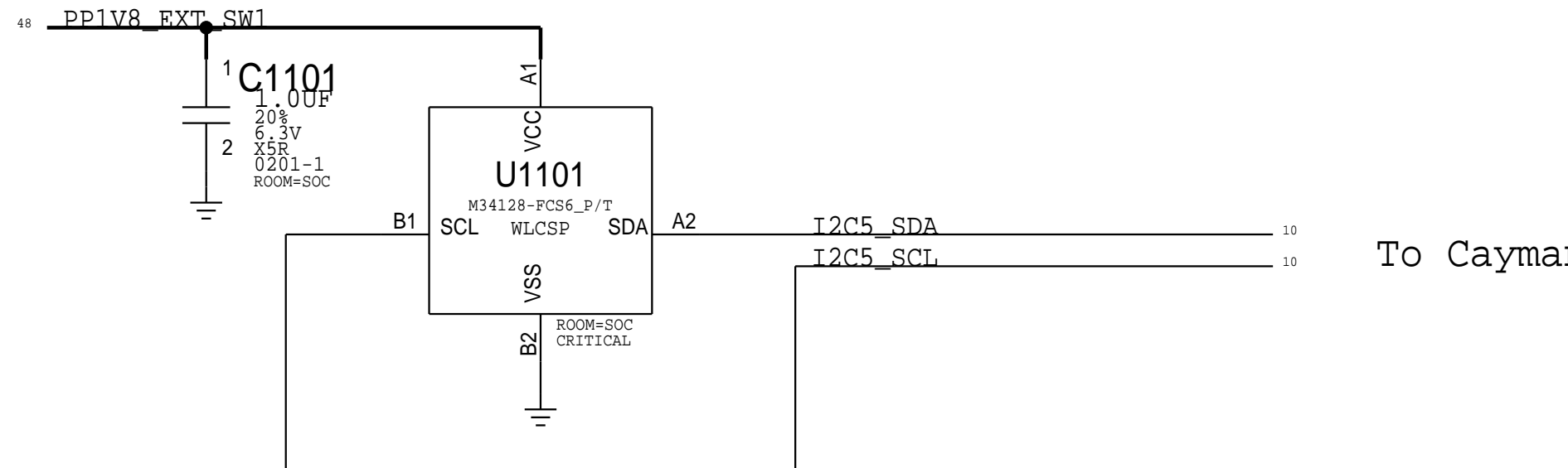
NC\_AP\_GPIO\_42  
NC\_AP\_GPIO\_43

SPI\_SOC\_TO\_PMU\_SCLK  
SPI\_PMU\_TO\_SOC\_DATA  
SPI\_SOC\_TO\_PMU\_DATA  
DWT\_SOC\_TO\_BEACON2\_CLK  
DWT\_SOC\_TO\_BEACON2\_DATA

SOCHOT0\_PMU\_TO\_SOC\_L  
THROTTLE\_GPU\_SOC\_TO\_PMU\_L  
SOCHOT1\_SOC\_TO\_PMU\_L

CLK\_SOC\_TO\_TOUCH\_24MHZ\_R  
CLK\_SOC\_TO\_TOUCH\_24MHZ  
CLK\_SOC\_TO\_NAND\_24MHZ

I2C5  
See Radar#25316444 for Details

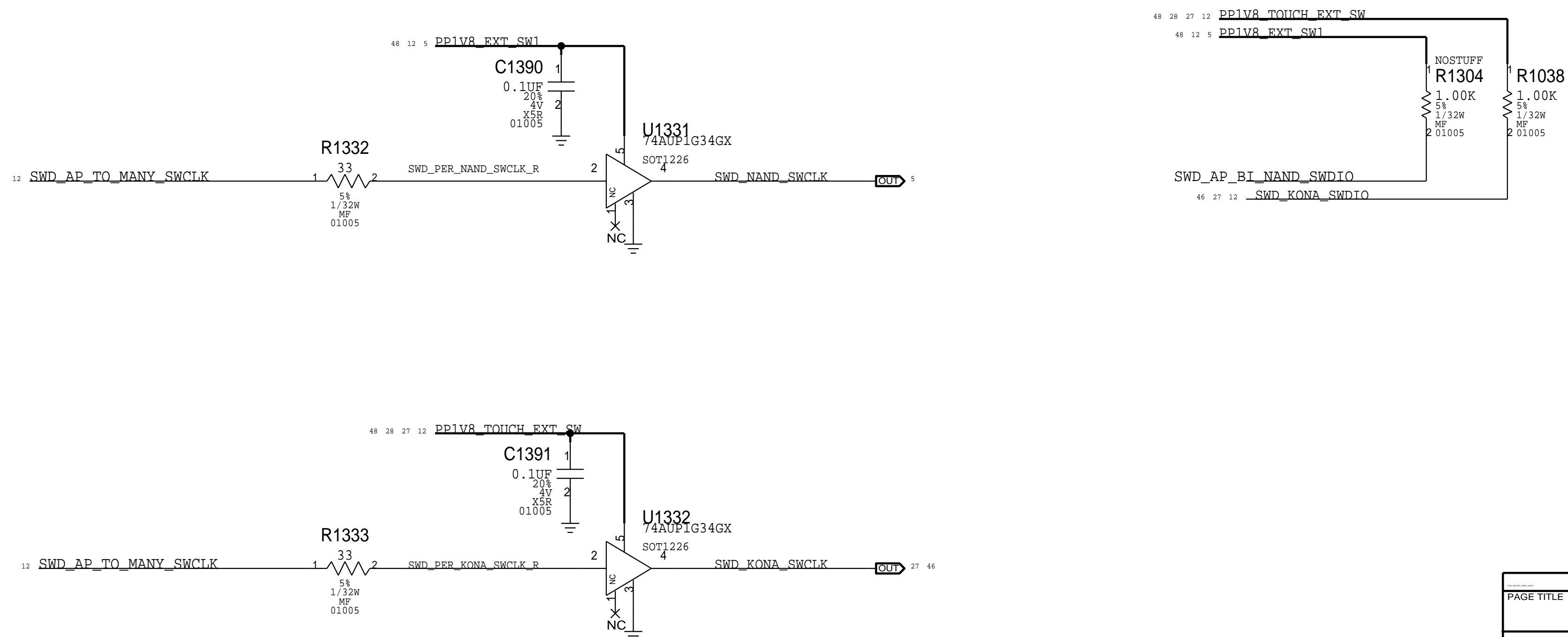
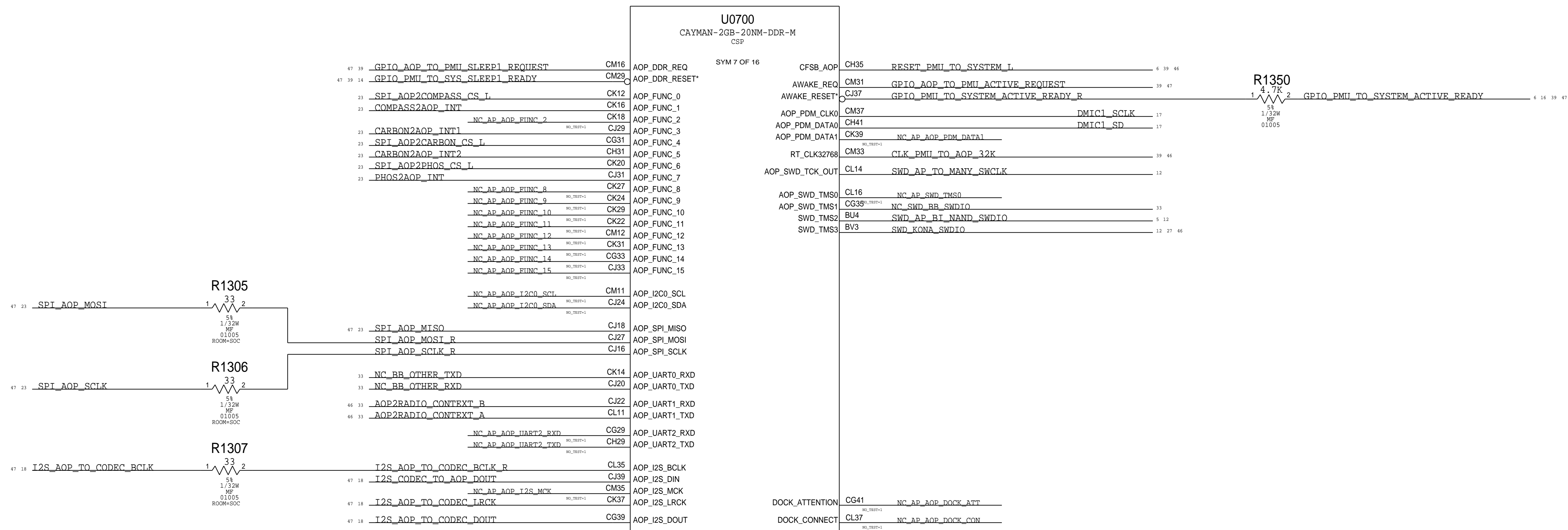


PAGE TITLE		
SOC:SERIAL		





## SOC - AOP



SOC - CPU, GPU & SOC RAILS

D

C

B

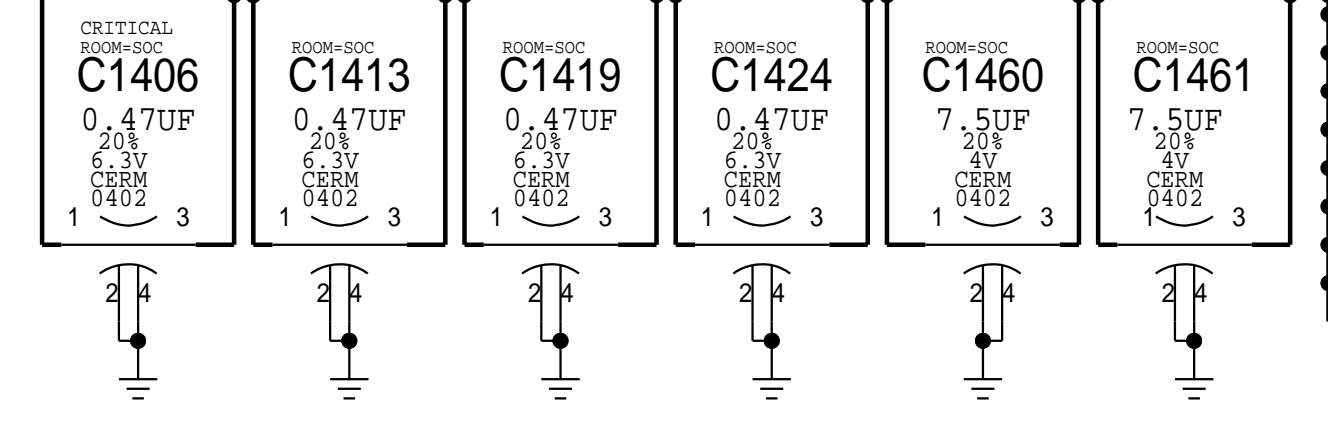
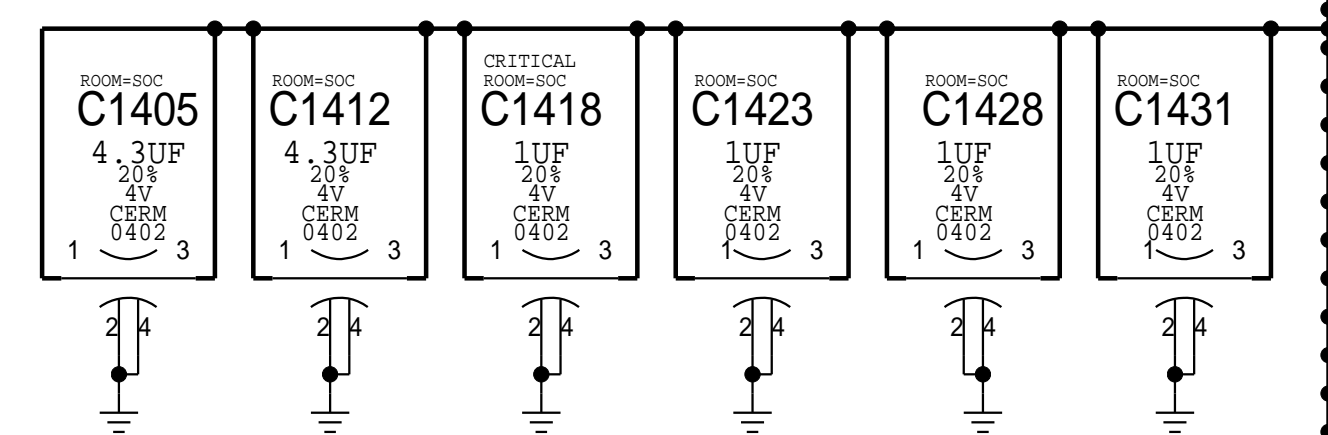
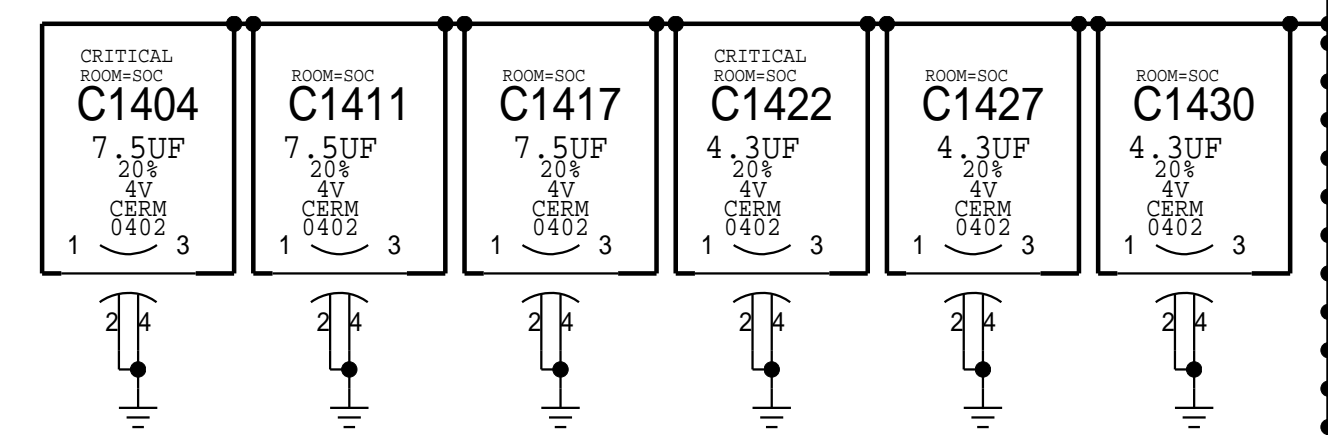
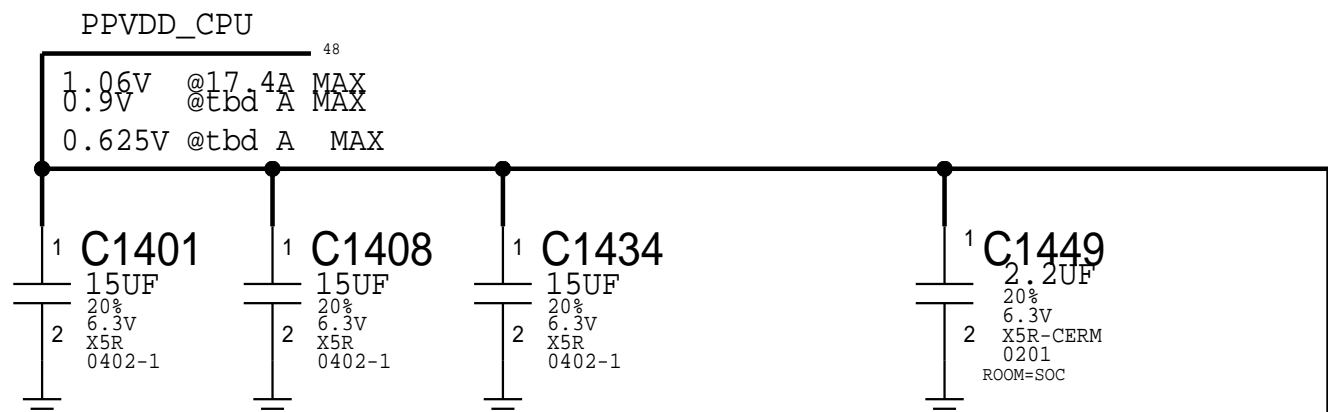
A

D

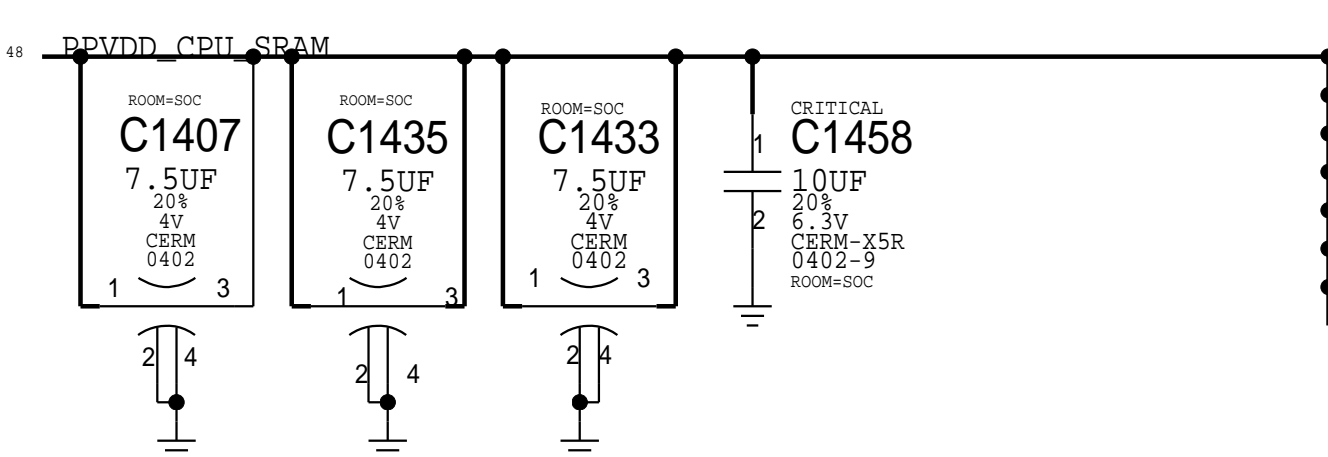
C

B

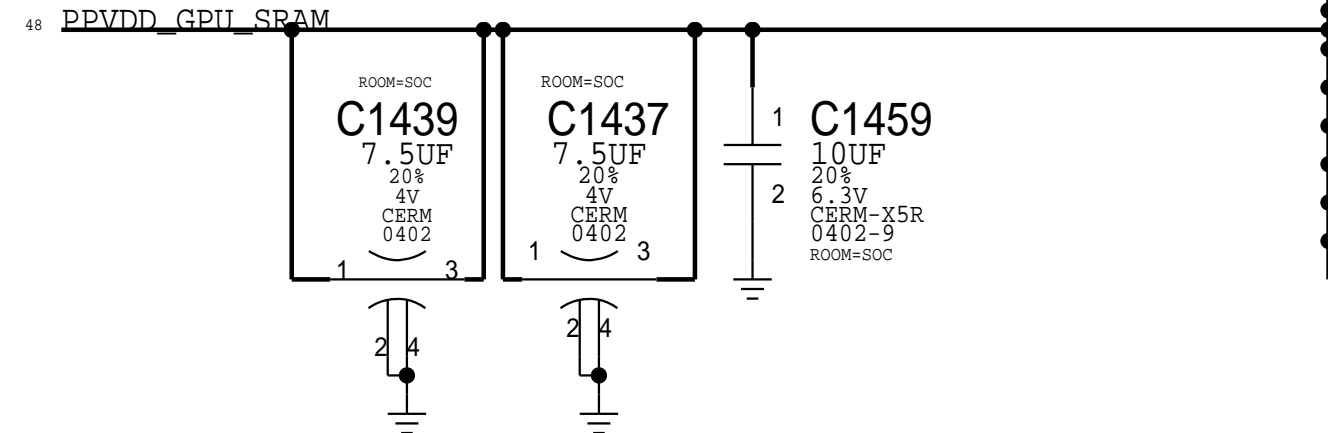
A



1.06V @1.0A MAX  
0.80V @TBDA MAX



1.03V @1.44A MAX  
0.92V @1.50A MAX  
0.80V @TBD A MAX



U0700  
CAYMAN-2GB-20NM-DDR-M  
CSP  
SYM 8 OF 16

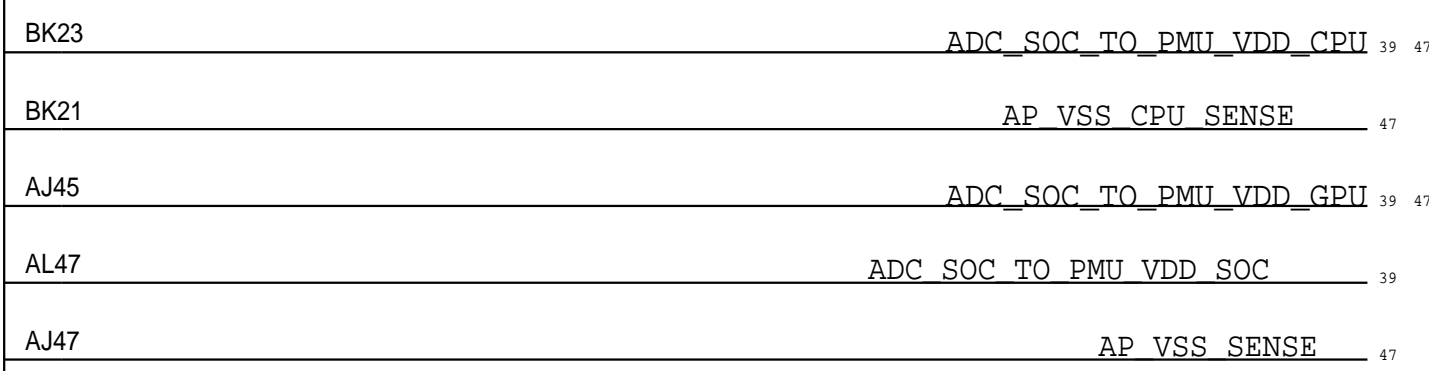
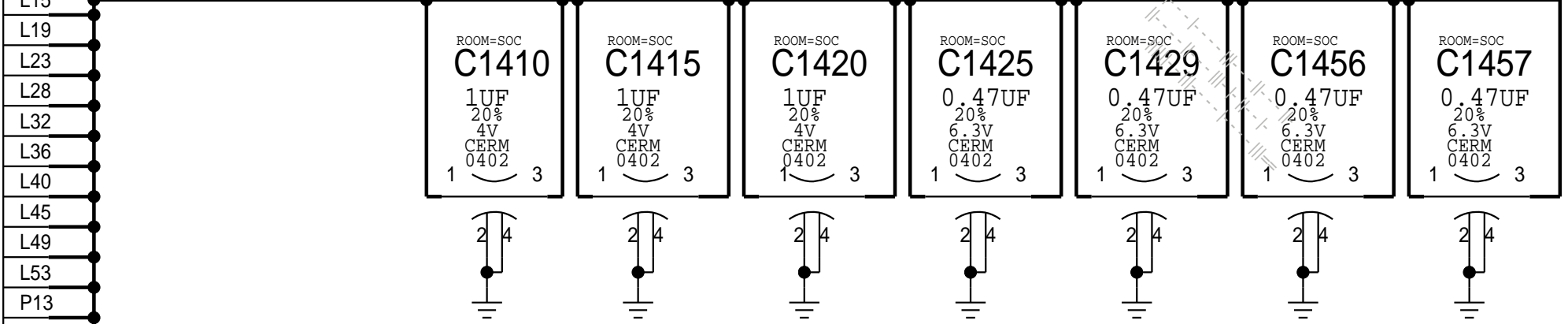
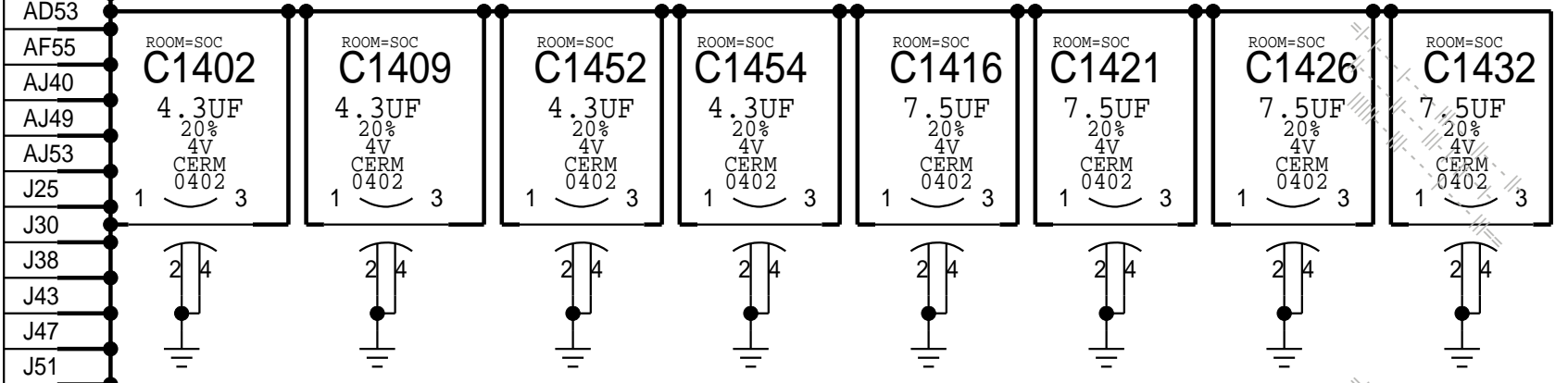
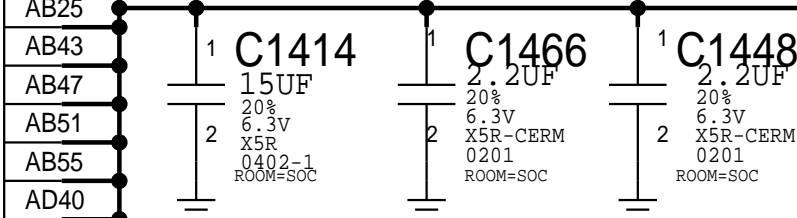
VDD\_CPU

VDD\_GPU

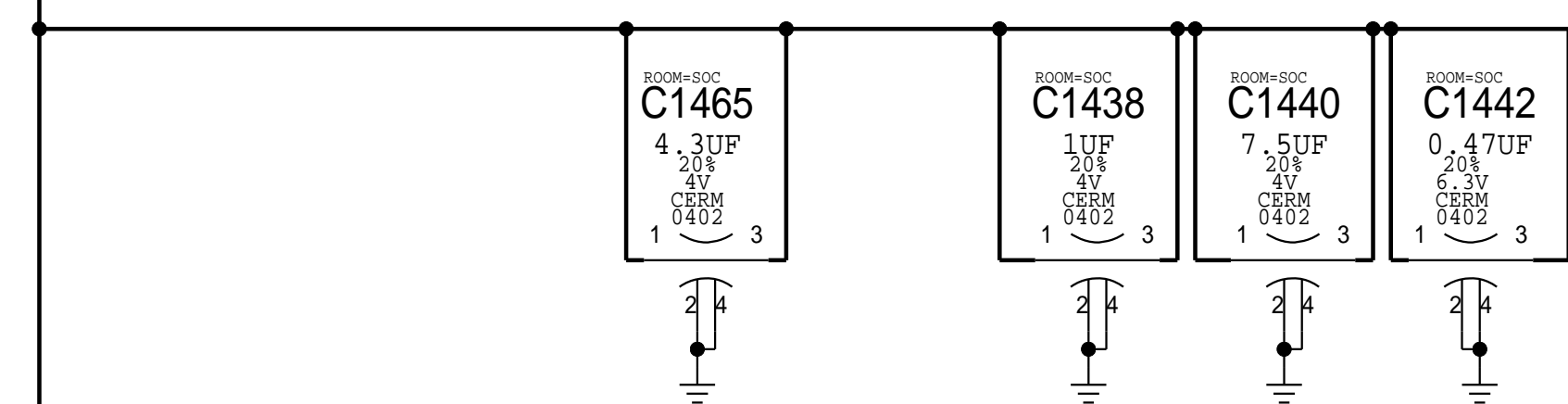
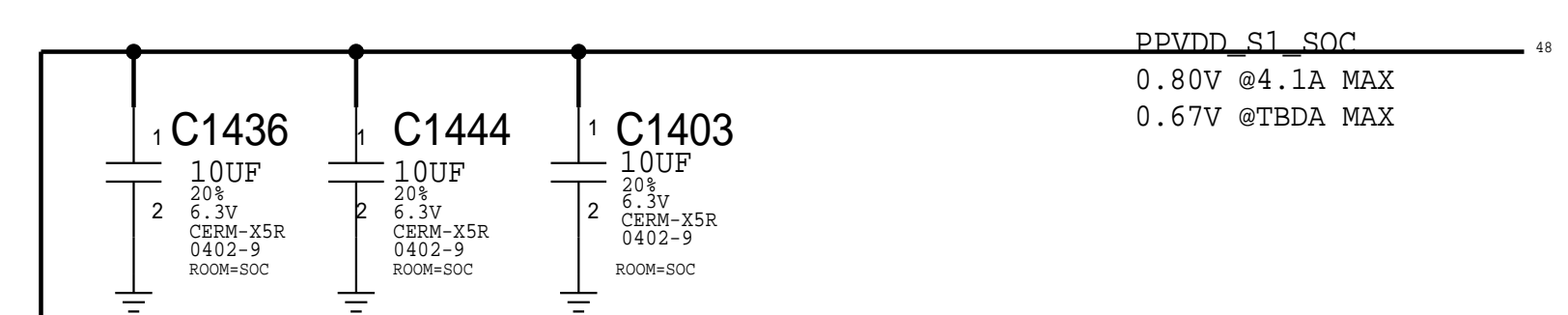
VDD\_CPU\_SRAM

VDD\_GPU\_SRAM

- AB13
- AB17
- AB21
- AB25
- AB43
- AB47
- AB51
- AB55
- AD40
- AD45
- AD49
- AD53
- AF55
- AJ40
- AJ49
- AJ53
- J25
- J30
- J38
- J43
- J47
- J51
- L15
- L19
- L23
- L28
- L32
- L36
- L40
- L45
- L49
- L53
- P13
- T15
- T36
- T40
- T53
- V13
- V25
- V34
- V38
- V51
- V55
- Y28



1.03V @12.9A MAX  
0.92V @10.7A MAX  
0.80V @TBD A MAX  
0.67V @TBD A MAX  
PPVDD\_GPU



U0700  
CAYMAN-2GB-20NM-DDR-M  
CSP  
SYM 9 OF 16

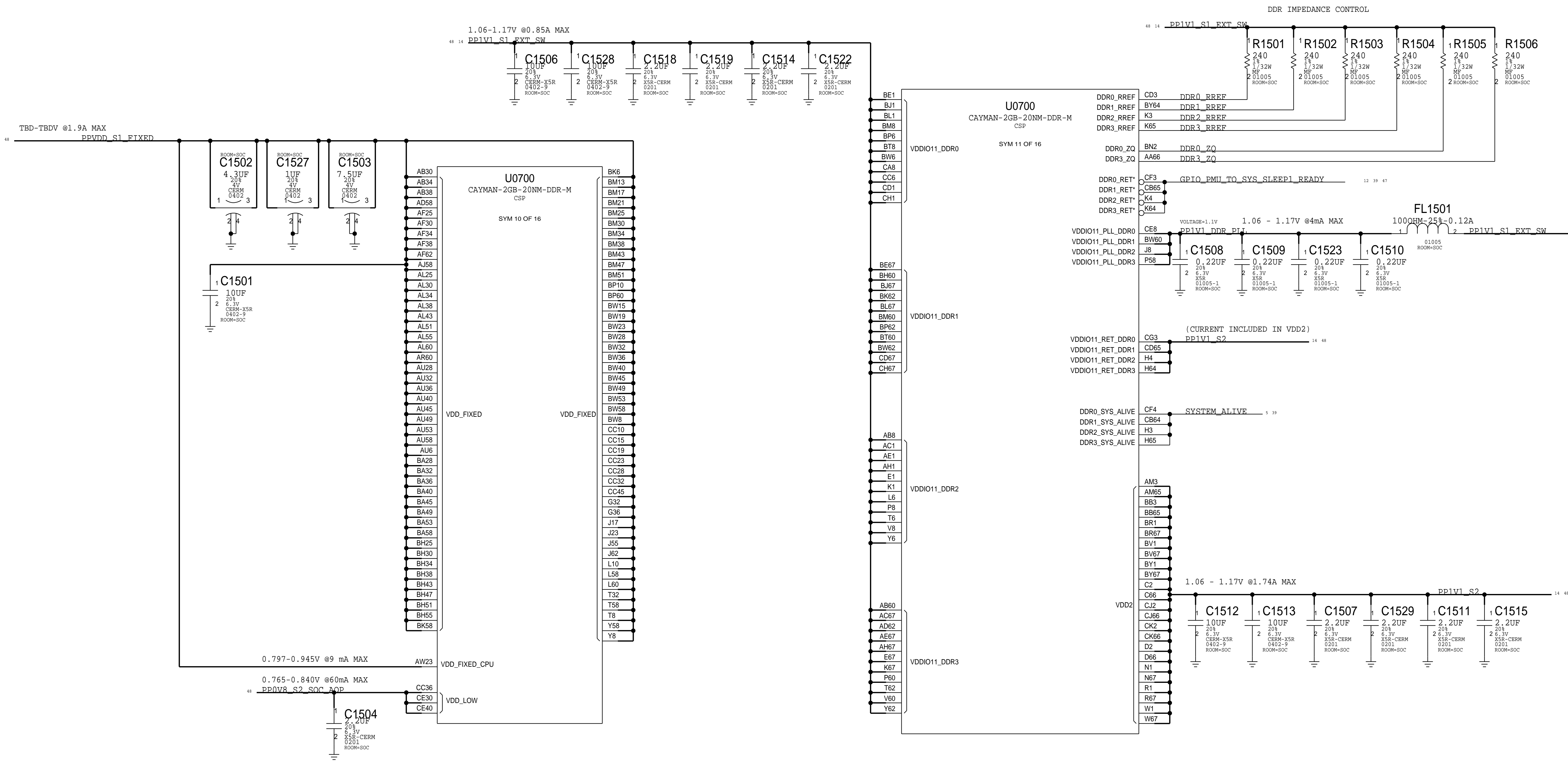
VDD\_SOC

VDD\_SOC

- AD28
- AD32
- AF60
- AJ28
- AJ32
- AJ36
- AL6
- AN28
- AN32
- AN36
- AN40
- AN45
- AN49
- AN53
- AN58
- AR25
- AR30
- AR34
- AR38
- AR43
- AR47
- AR51
- AR55
- AW30
- AW34
- AW38
- AW43
- AW47
- AW51
- AW55
- AW60
- BD25
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- BD38
- BD43
- BD47
- BD51
- BD55
- BD6
- BD60
- BF28
- BF32
- BF36
- BF45
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- BF53
- BF58
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- BT38
- BT43
- BT47
- BT51
- BT55
- BW10
- CA13
- CA17
- CA21
- CA25
- CA30
- CA34
- CA38
- CA43
- CA47
- CE13
- CE17
- CE45
- J13
- J21
- J34
- P55
- T10
- T60
- V30
- Y10
- Y36
- Y60
- BF40
- J60
- AW25

SOC - POWER SUPPLIES





SOC - POWER SUPPLIES

D

C

B

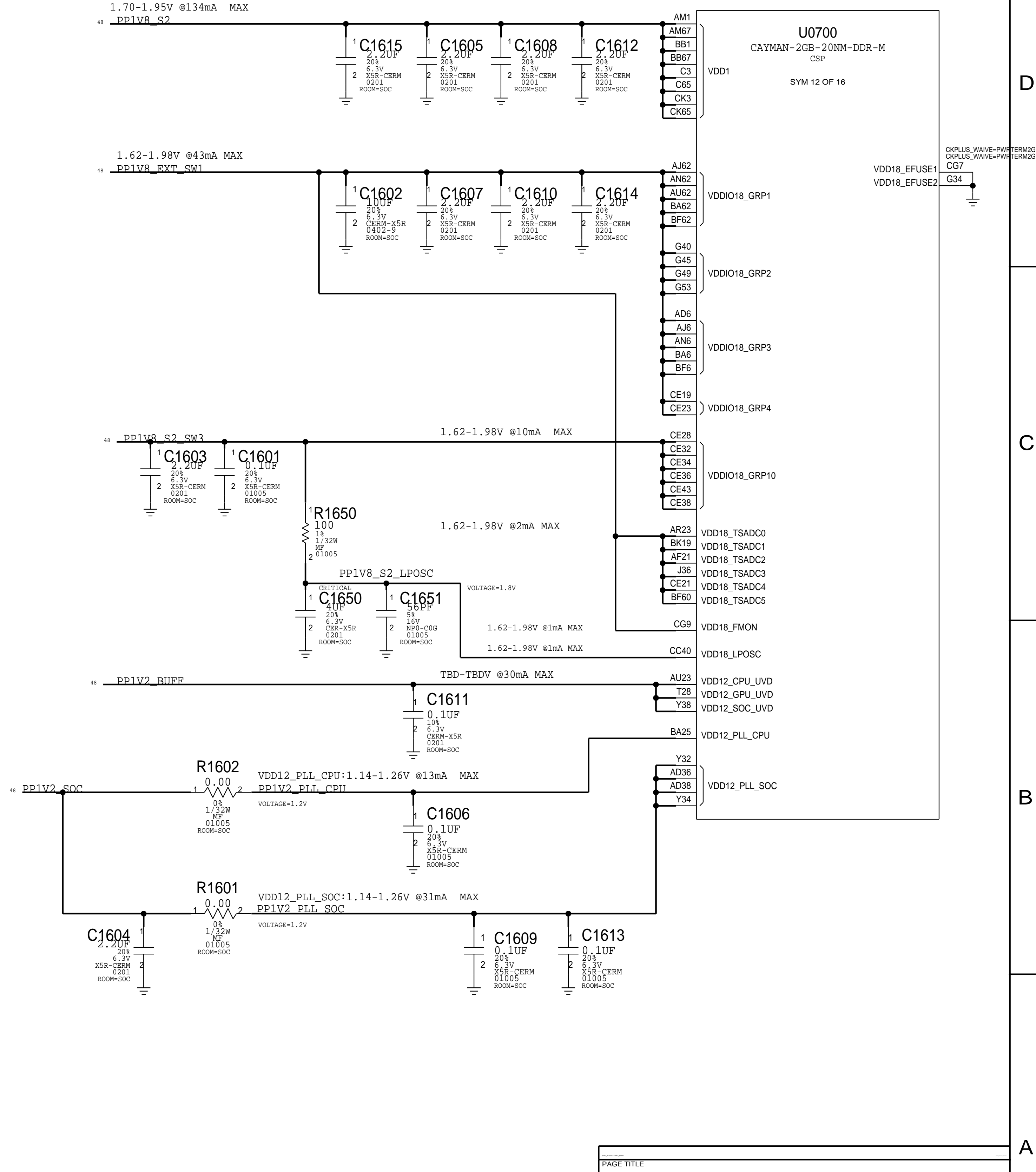
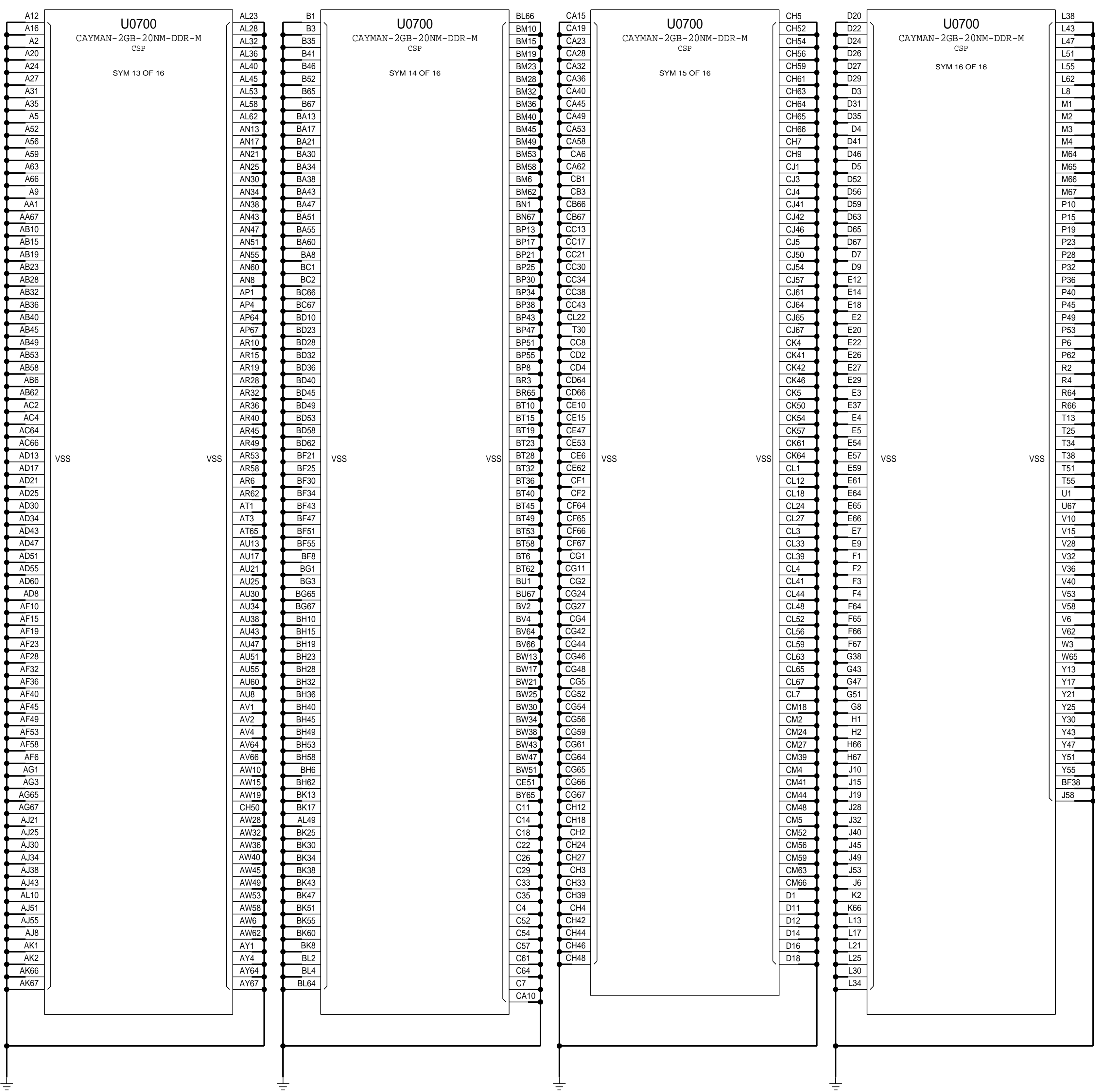
A

D

C

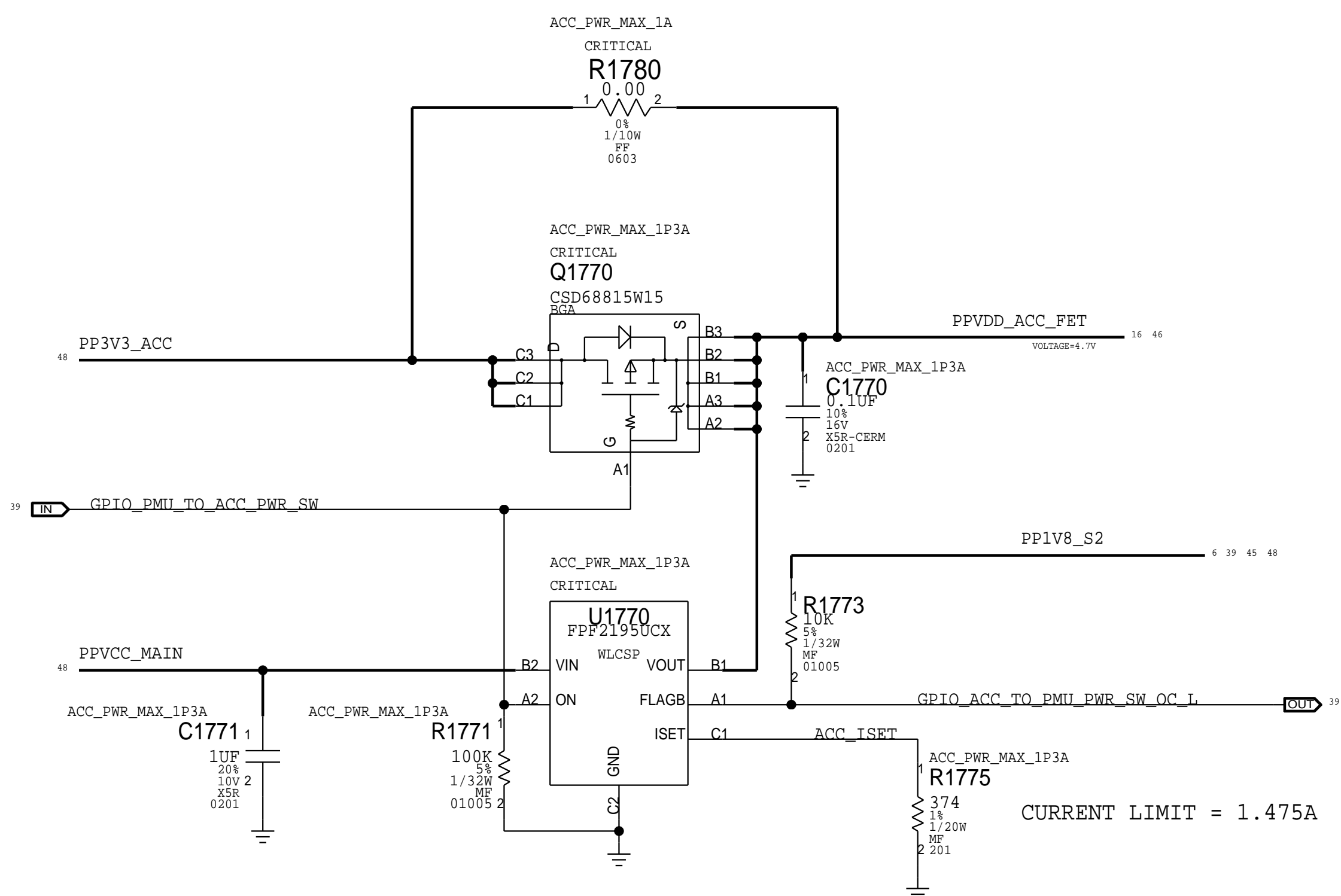
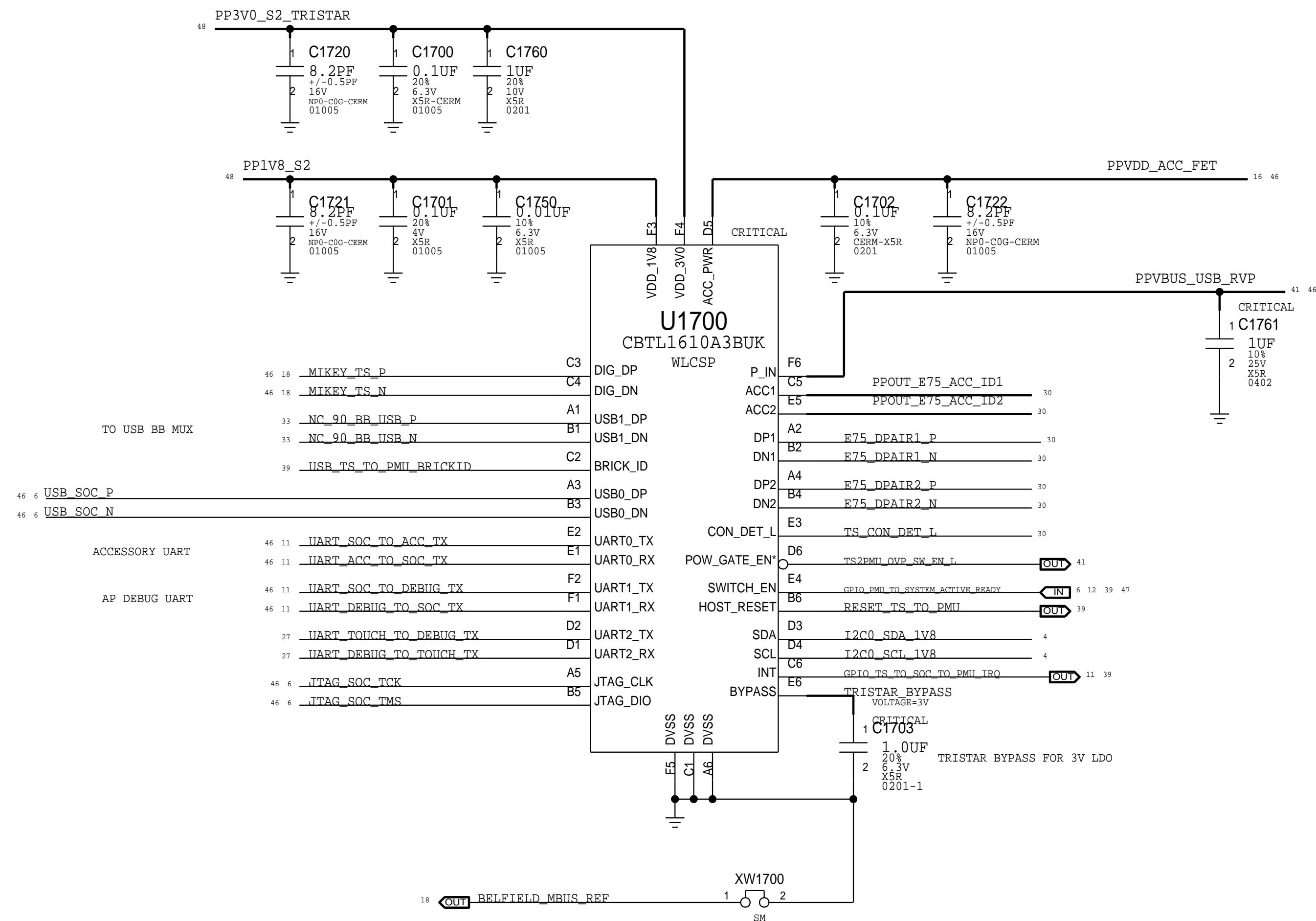
B

A



PAGE TITLE		
SOC:POWER (3/3)		

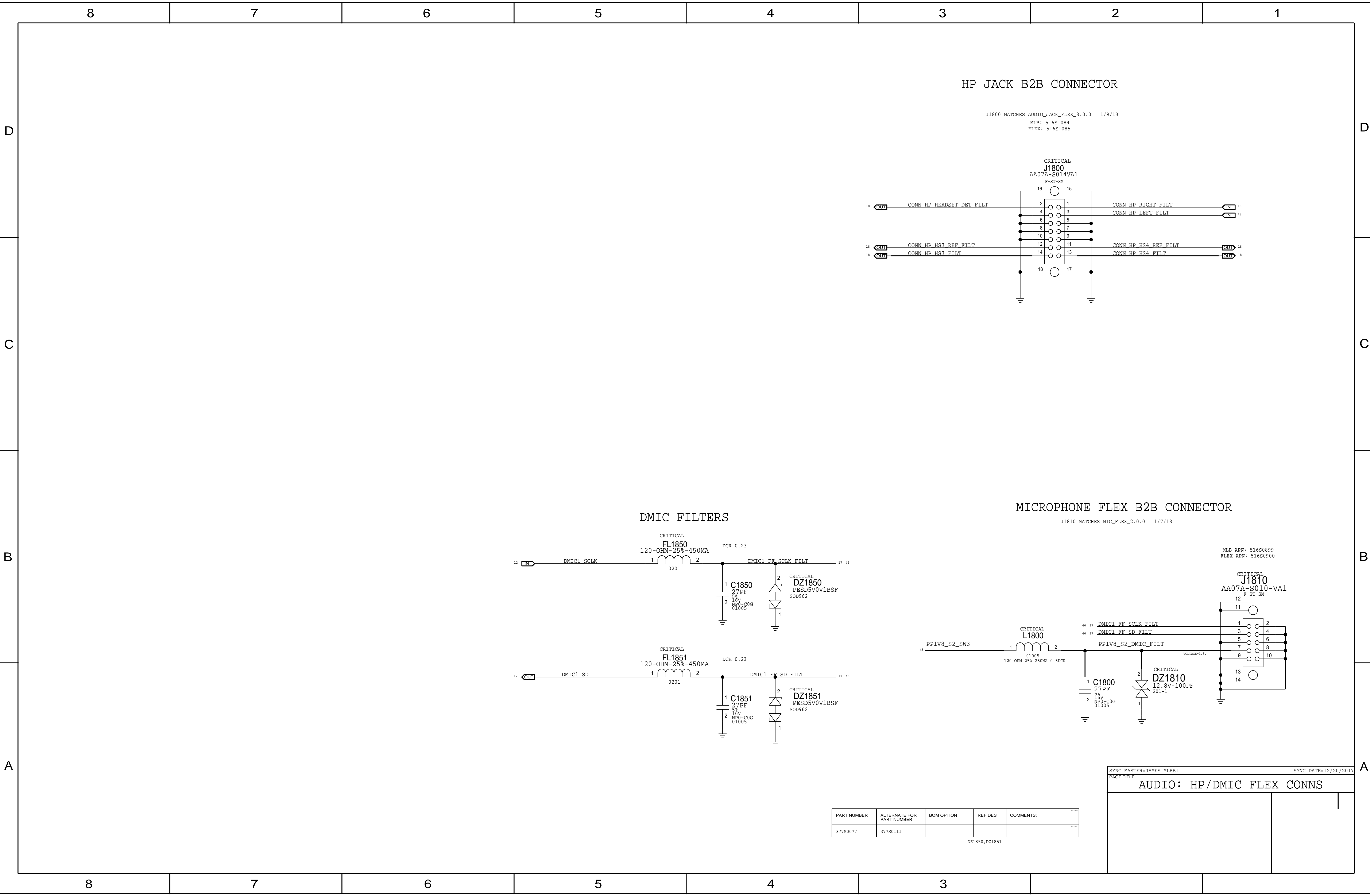
# TRISTAR



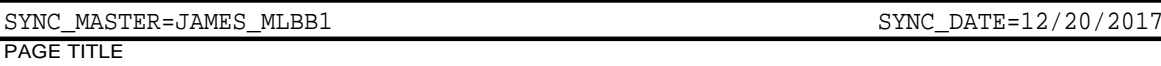
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343S0658 = TRISTAR 2, A1  
  
998-5855 = TRISTAR 2, TC  
343S0639 = TRISTAR 2, A0  
  
343S0614 = TRISTAR 1  
  
NOTE: A2 ONLY USED ON IPHONES

SYNC_MASTER=JAMES_MLBBI	SYNC_DATE=12/20/2017
PAGE TITLE	

IO: TRISTAR



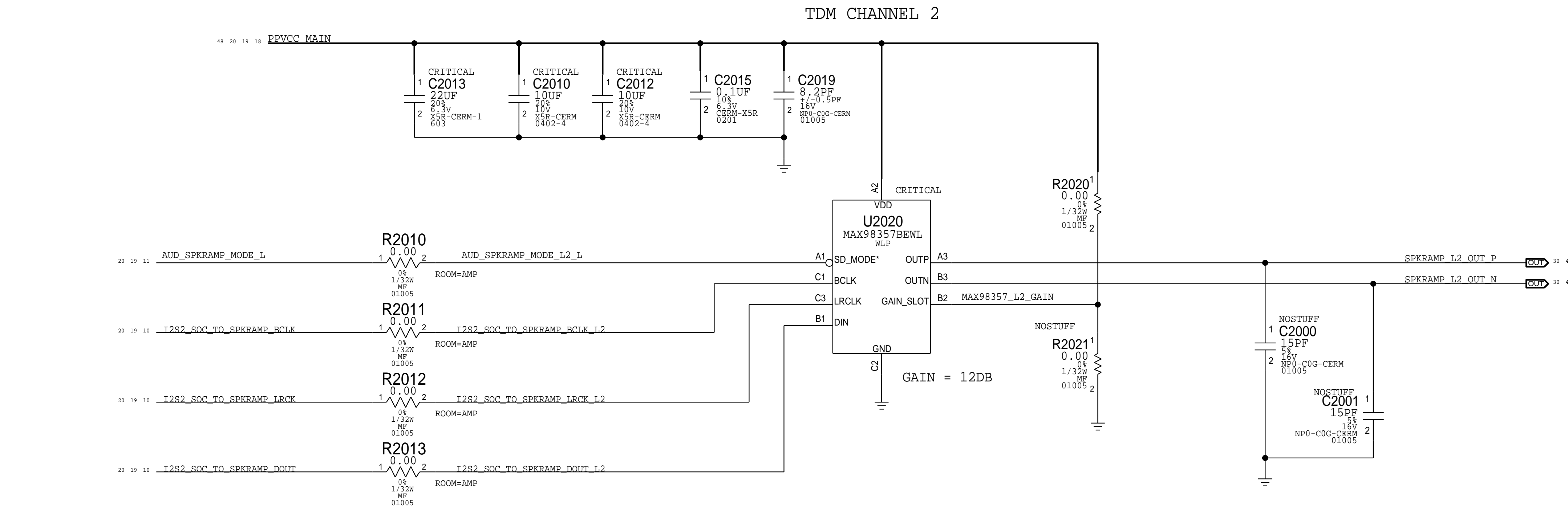
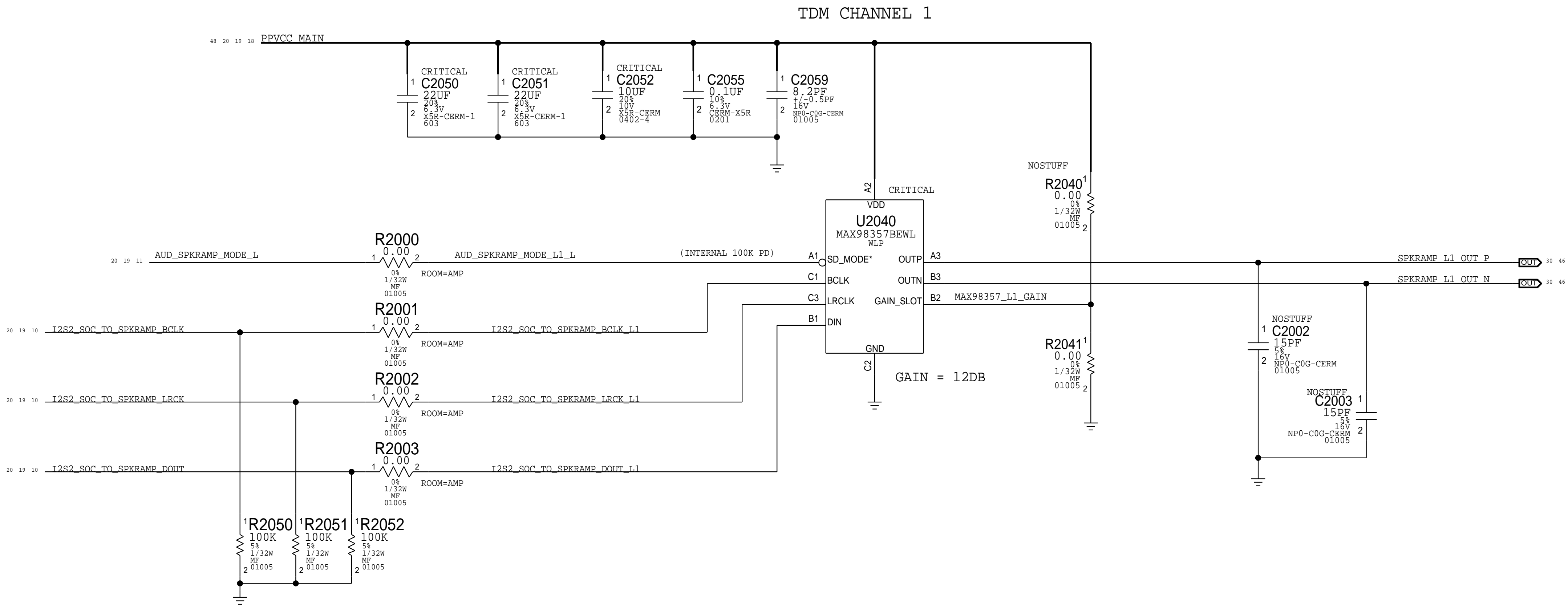




AUDIO: CLIFDEN & BELFIELD

SPEAKER AMPLIFIERS

APN: 353S4265



SD_MODE#	TDM CHANNEL	GAIN_SLOT
H	1	PULLED TO GND
H	2	PULLED WITH 0-OHM TO VDD
H	3	FLOAT
H	4	PULLED WITH 100K-OHM TO VDD

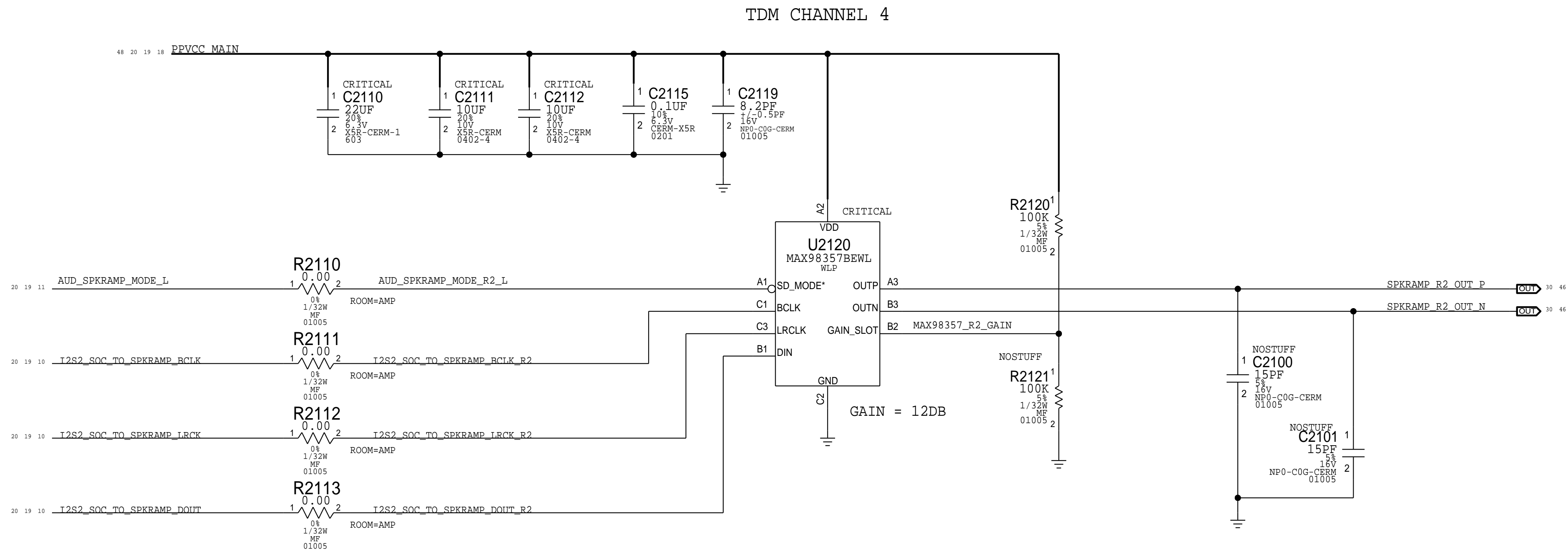
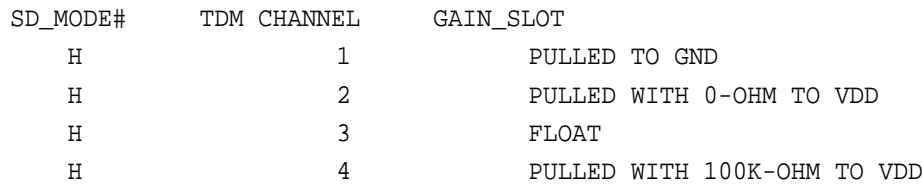
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SYNC\_DATE=12/20/2017

PAGE TITLE

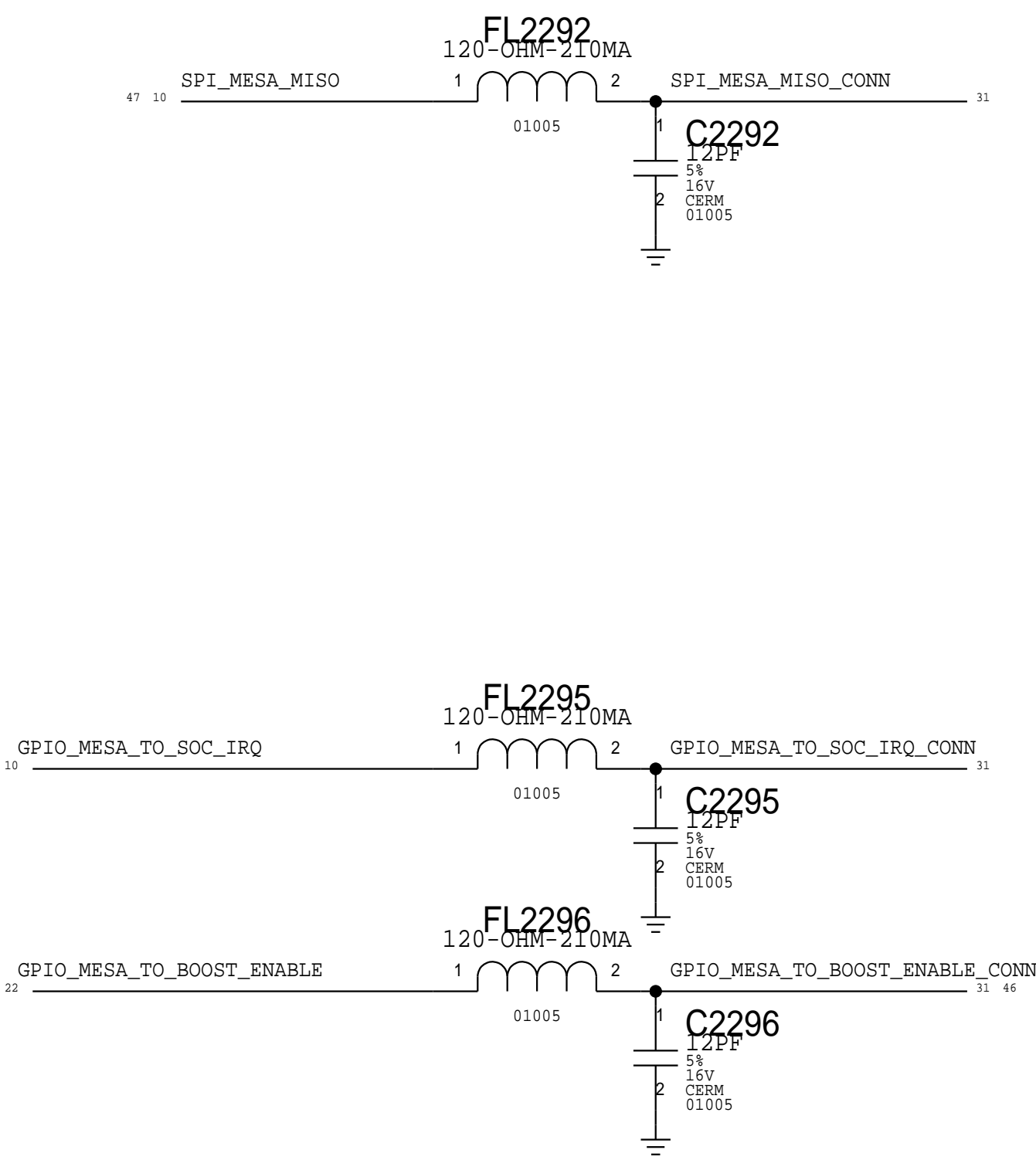
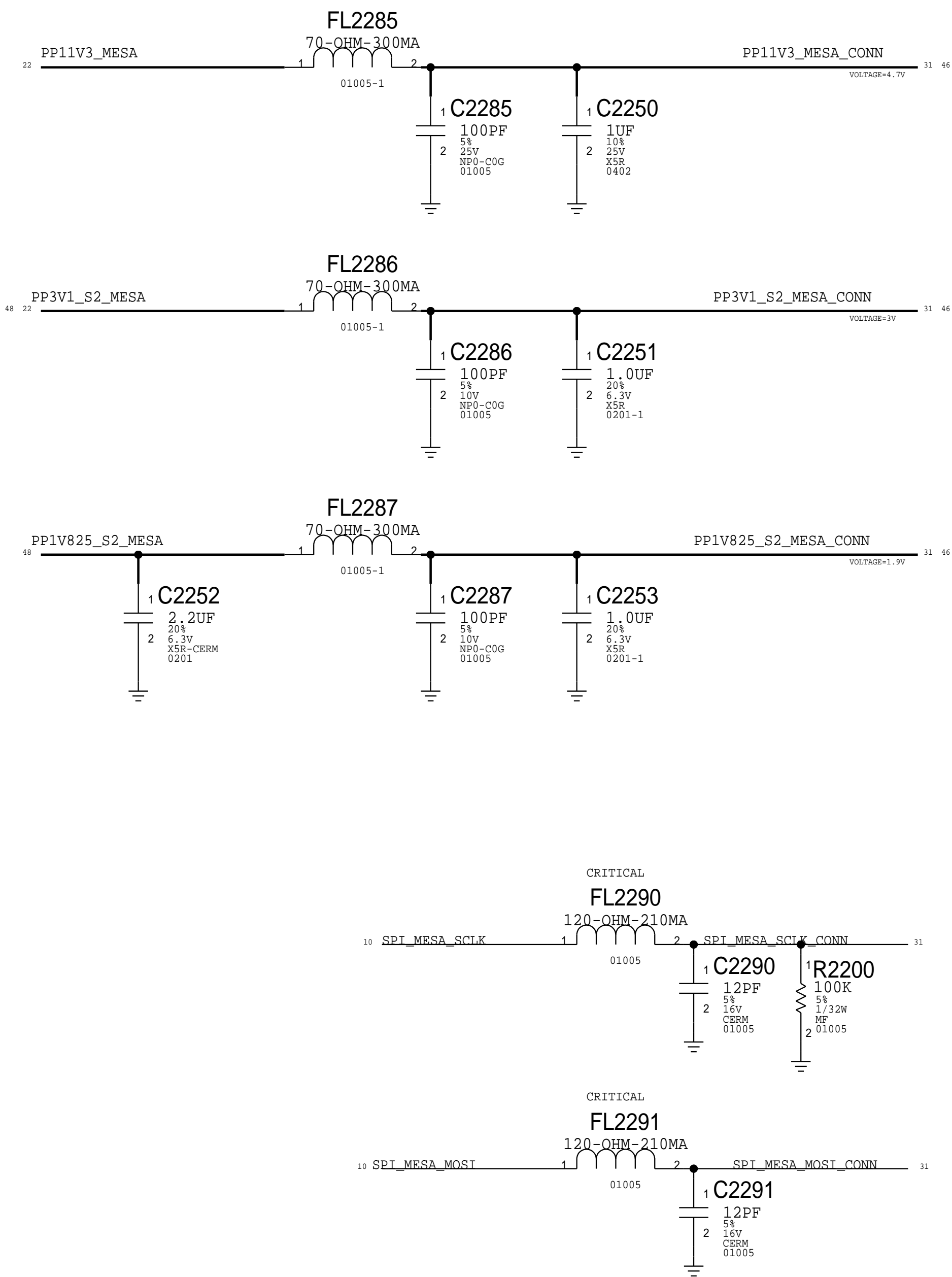
AUDIO: SPEAKER AMPS LEFT

APN: 353S4265





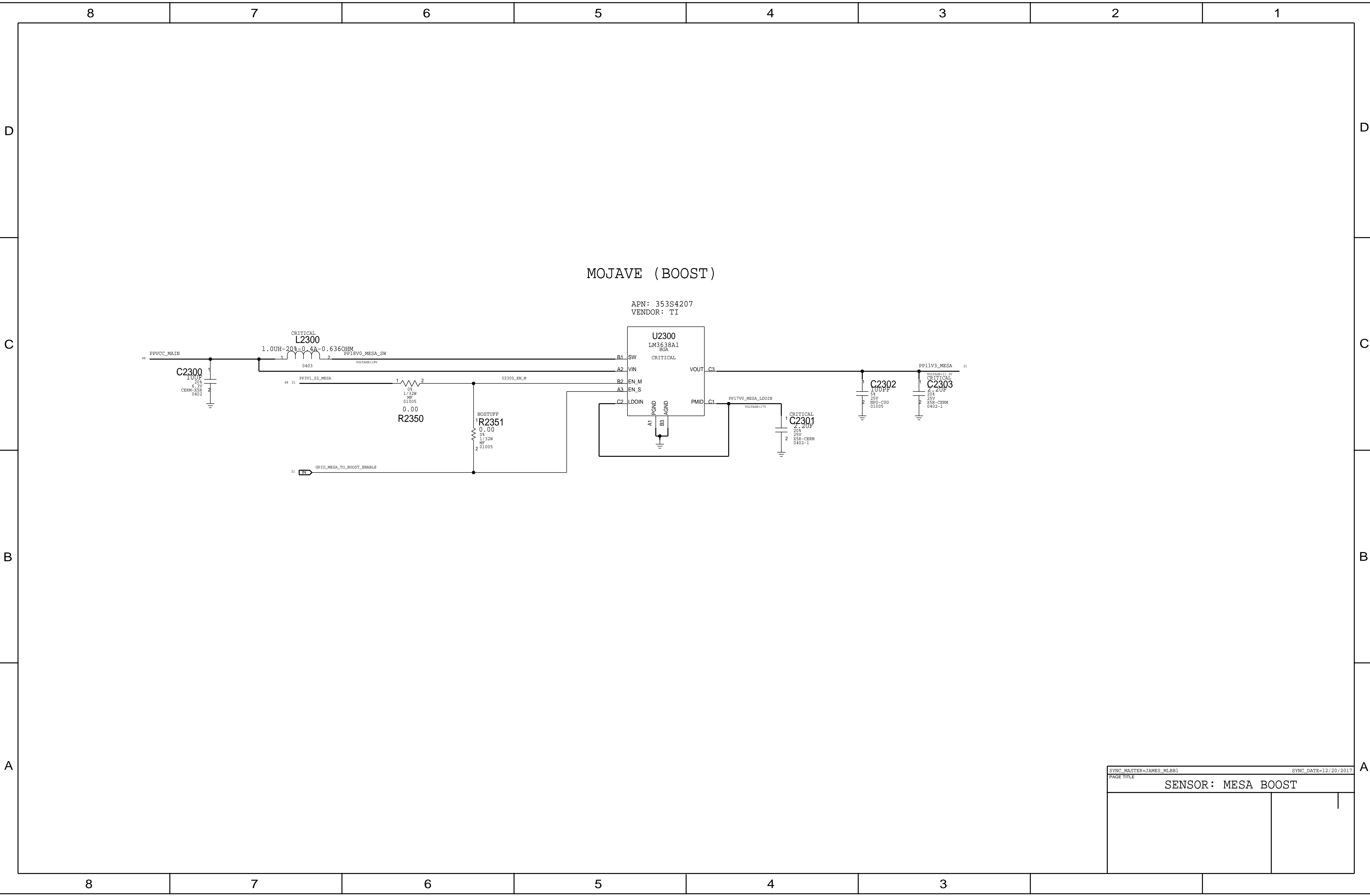
MESA SUPPORT

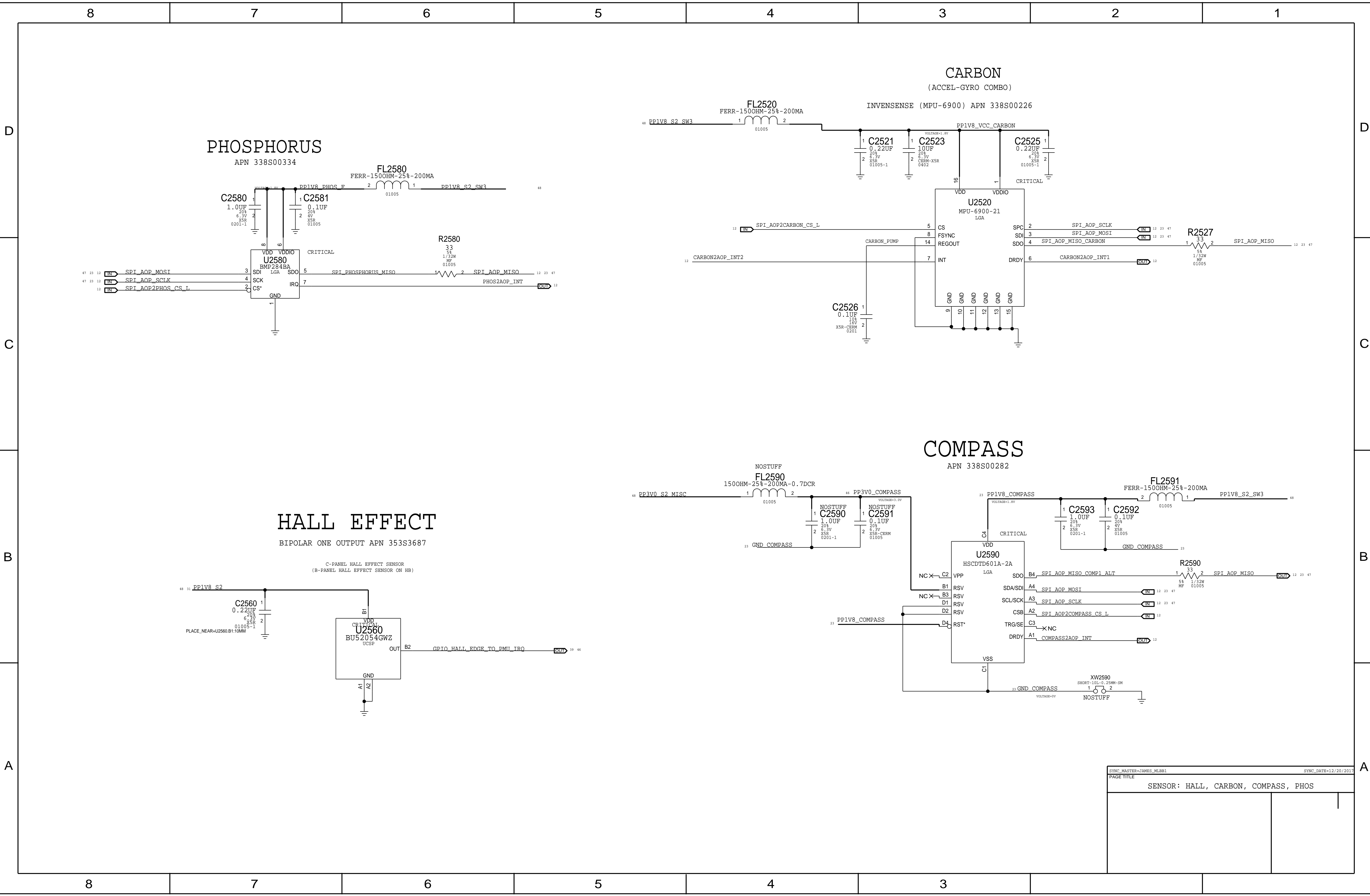


SYNC\_MASTER=JAMES\_MLB1 SYNC\_DATE=12/20/2017

PAGE TITLE

SENSOR: MESA SUPPORT







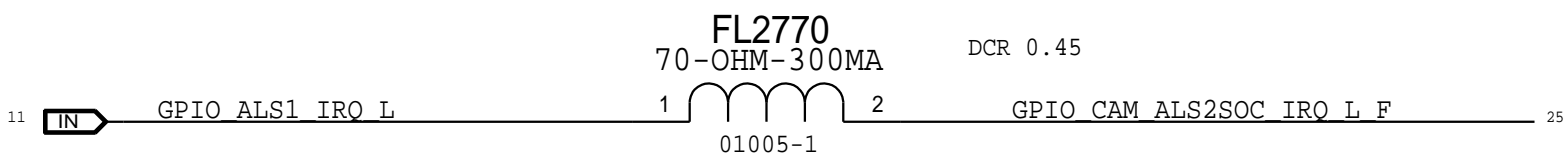
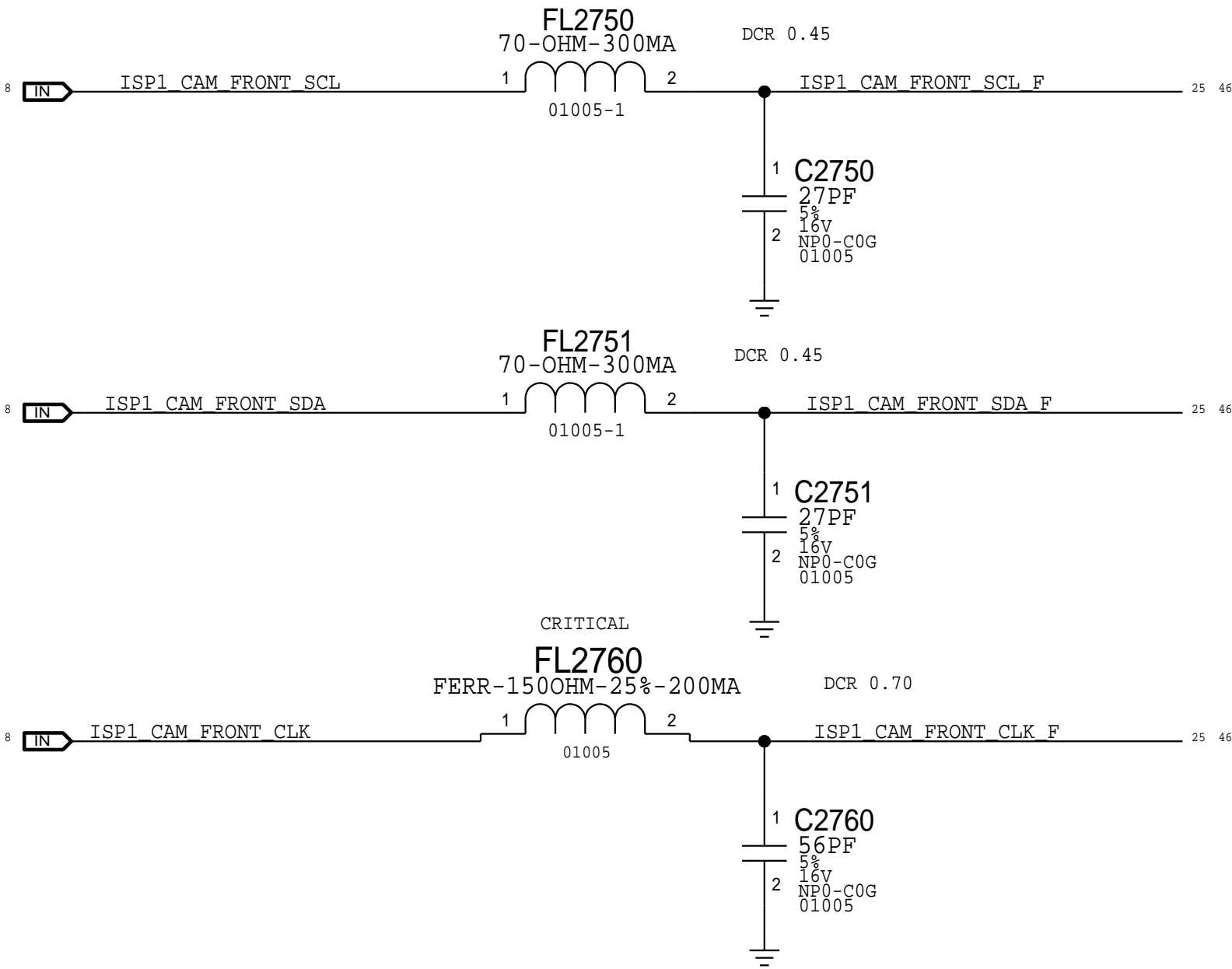
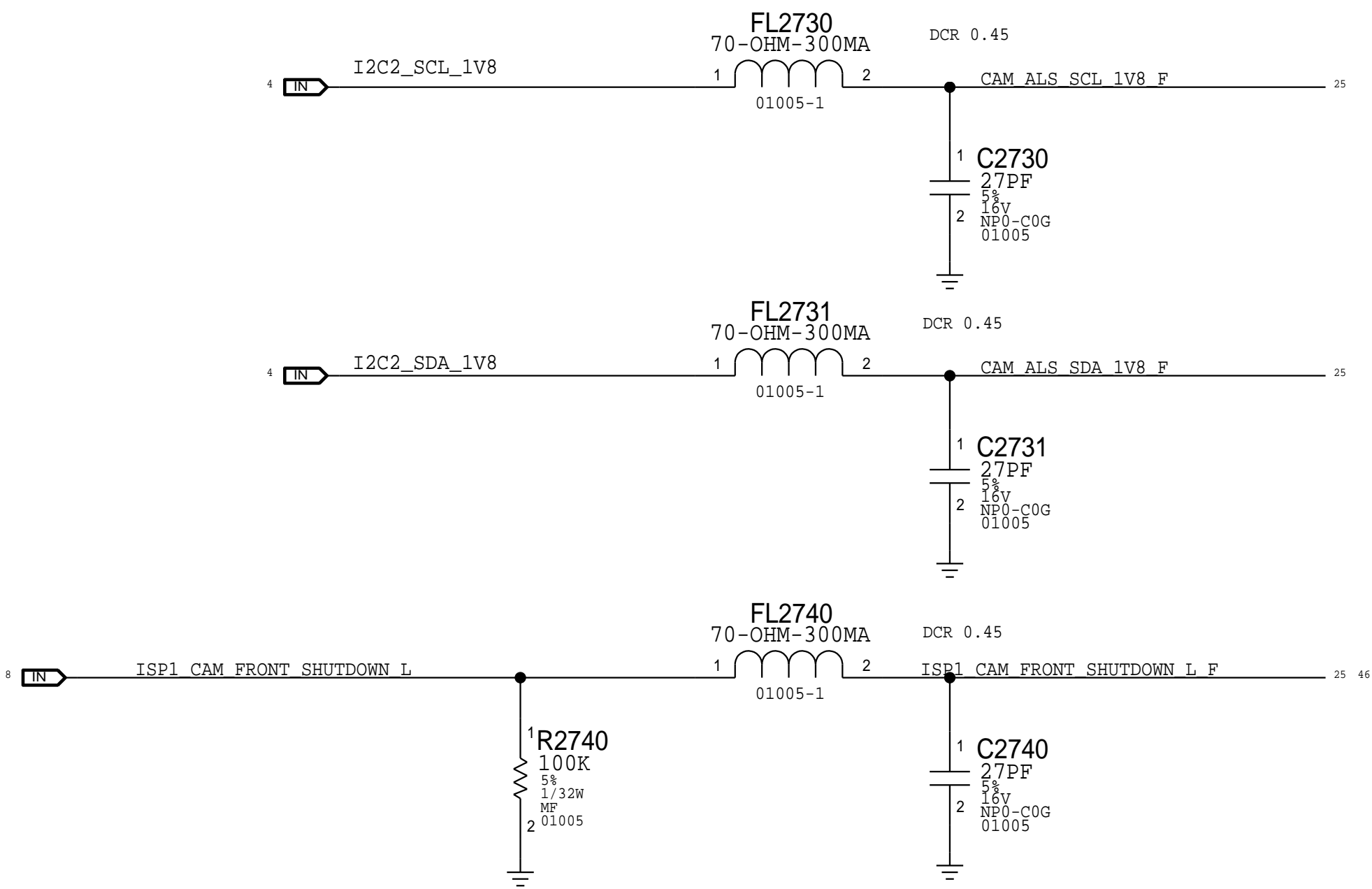
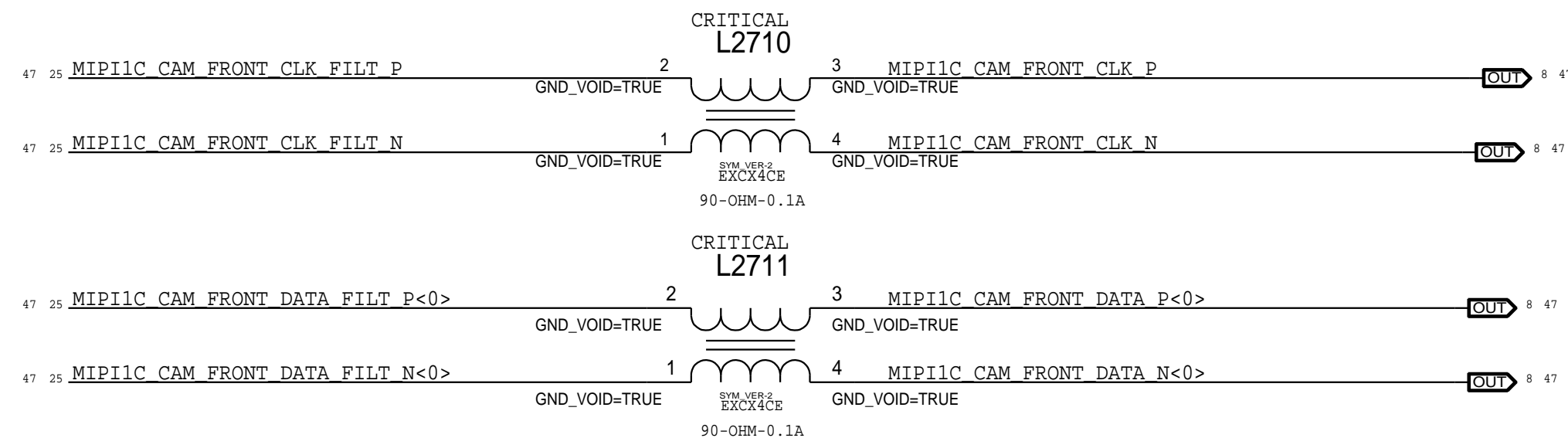
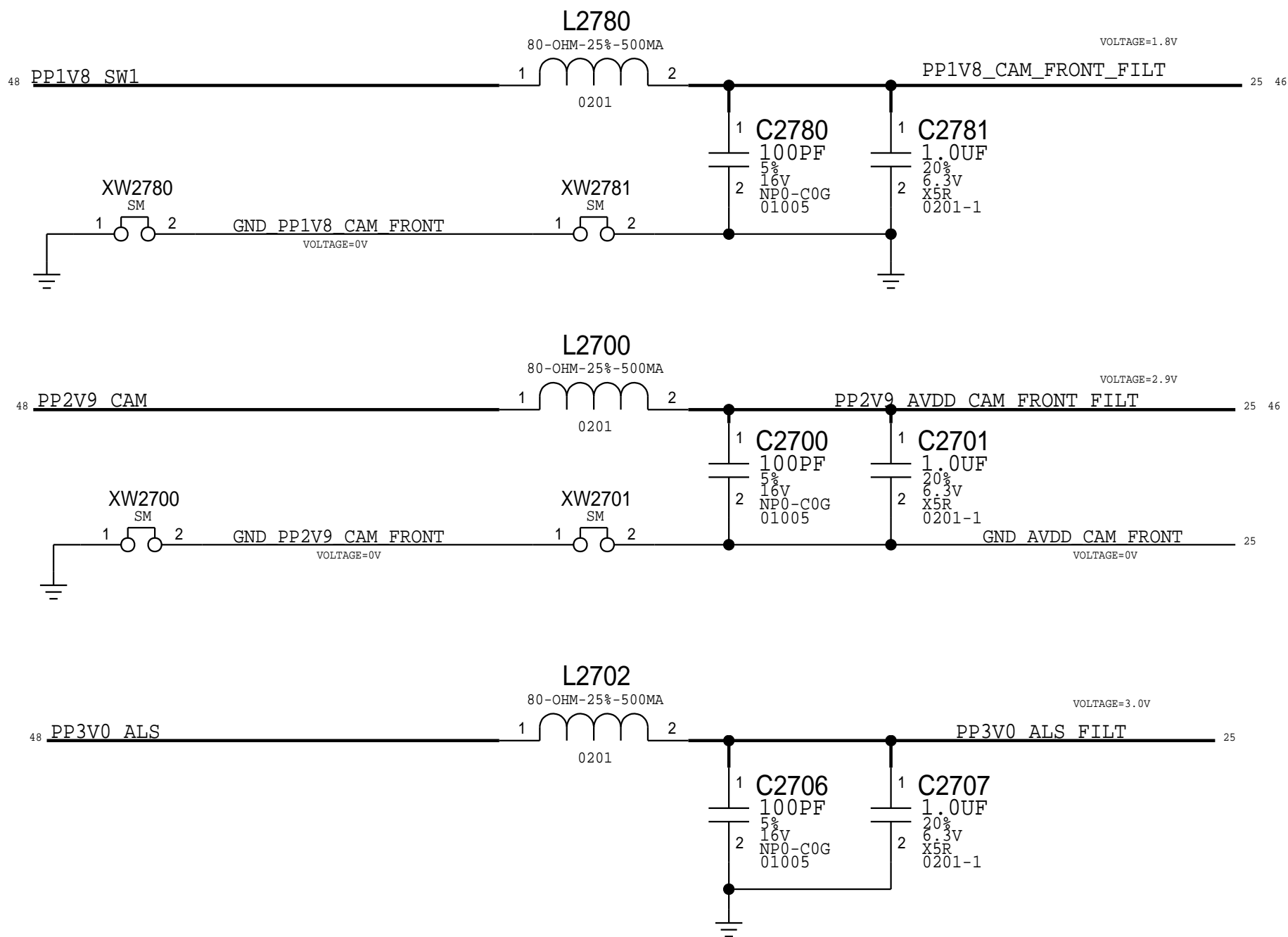
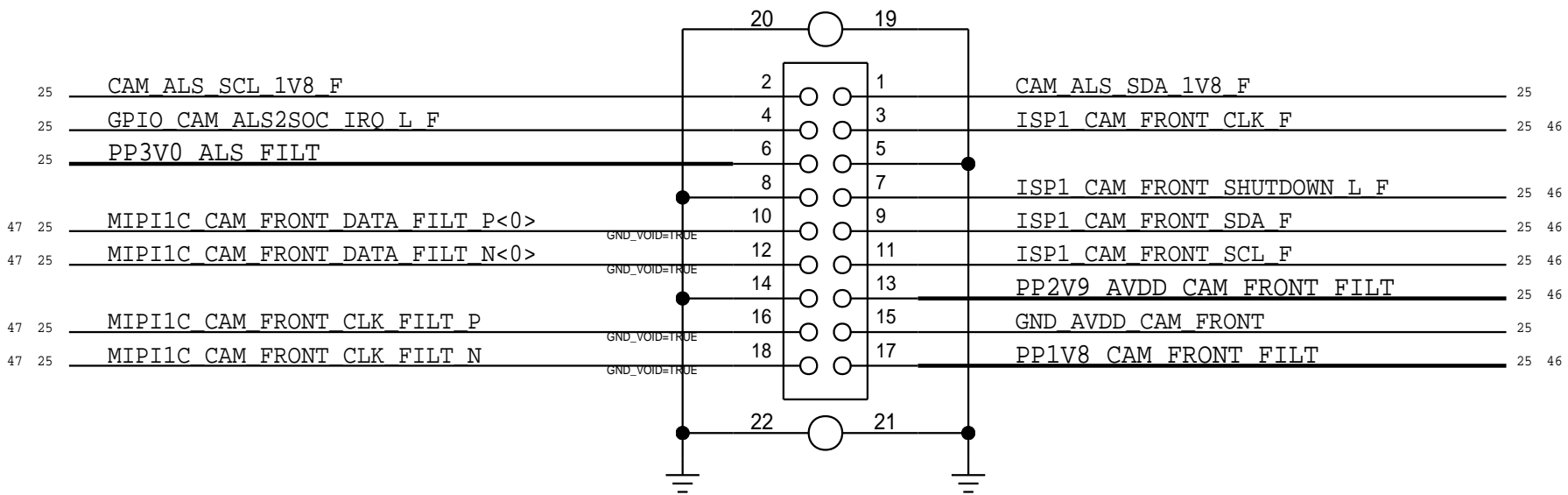


FRONT CAMERA CONNECTOR

J65 CAMERA CONNECTOR

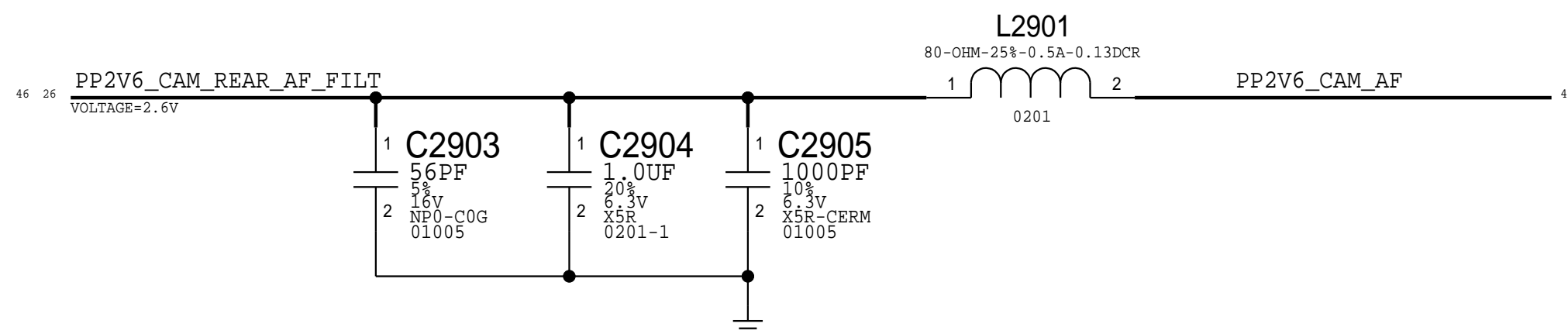
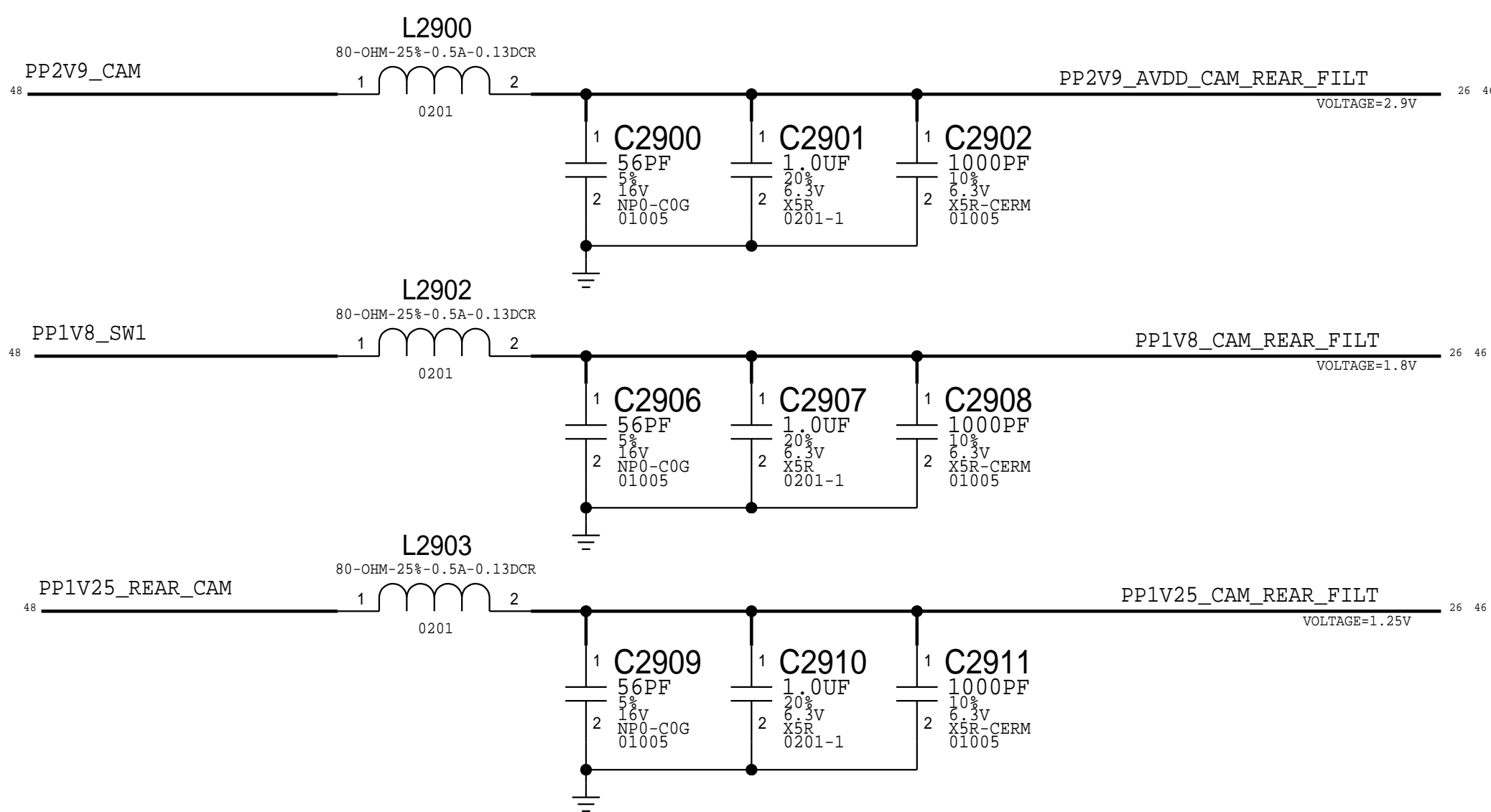
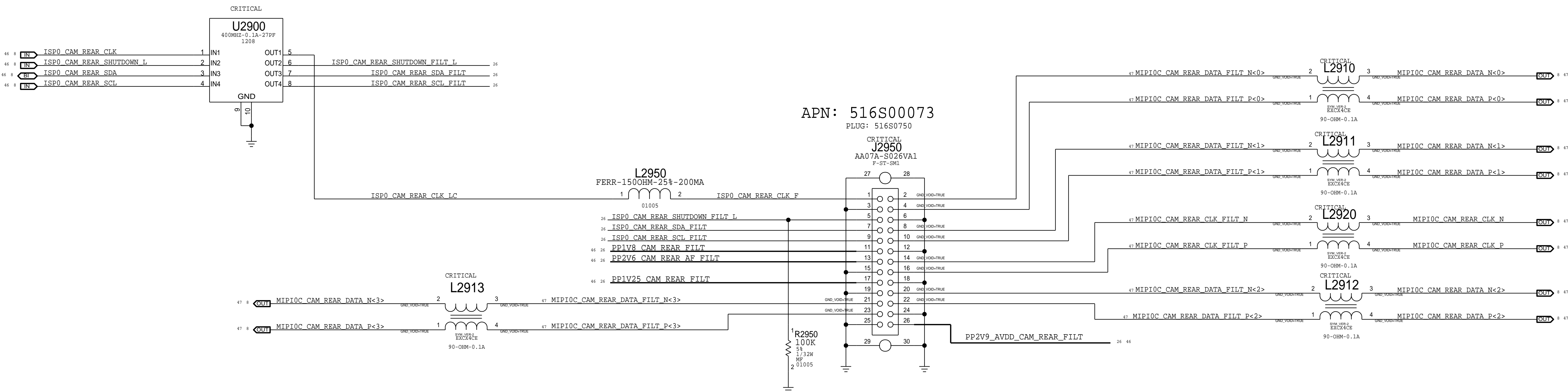
APN:MLB 516S0876  
APN:PLEX 516S0869

CRITICAL  
J2700  
503548-1820  
P-ST-SM



SYNC\_MASTER=JAMES\_MLB1  
PAGE TITLE  
CAMERA: FF AND ALS CONN

# REAR CAMERA CONNECTOR

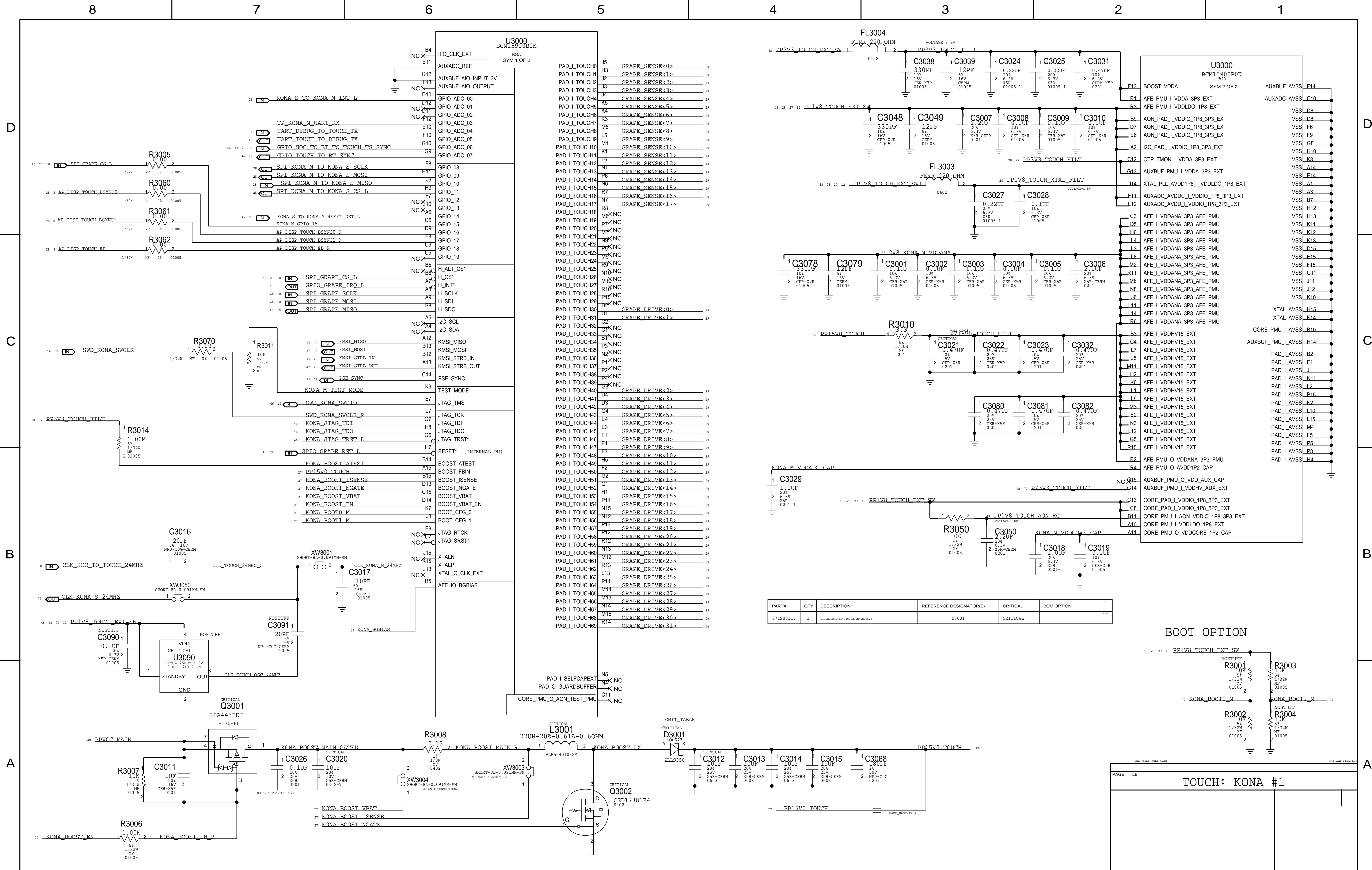


SYNC\_MASTER=JAMES\_MLBBI SYNC\_DATE=12/20/2017

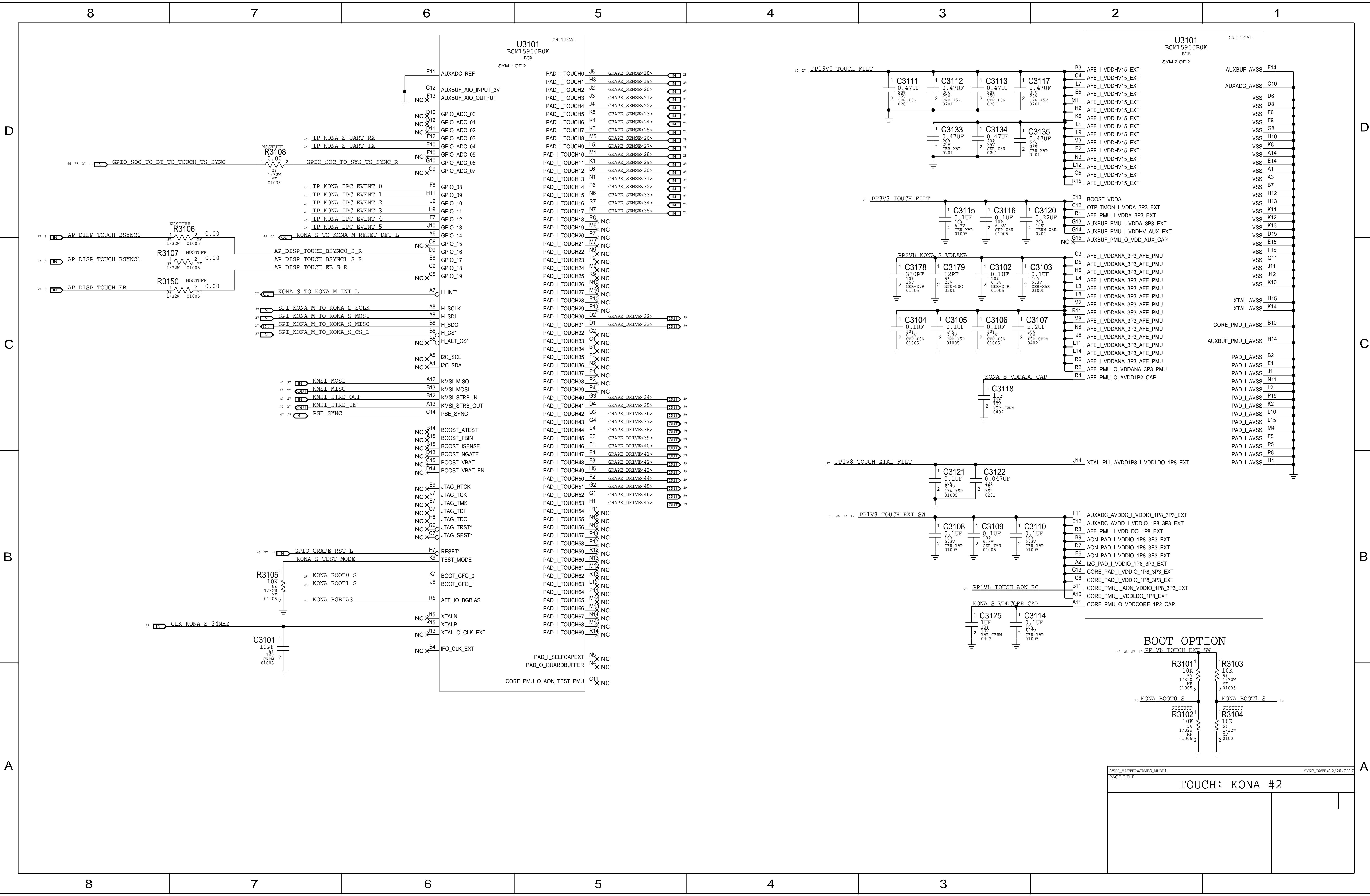
PAGE TITLE

CAMERA: REAR CONN & FILTERS









SYNC\_MASTER=JAMES\_MLB1 SYNC\_DATE=12/20/2017

PAGE TITLE

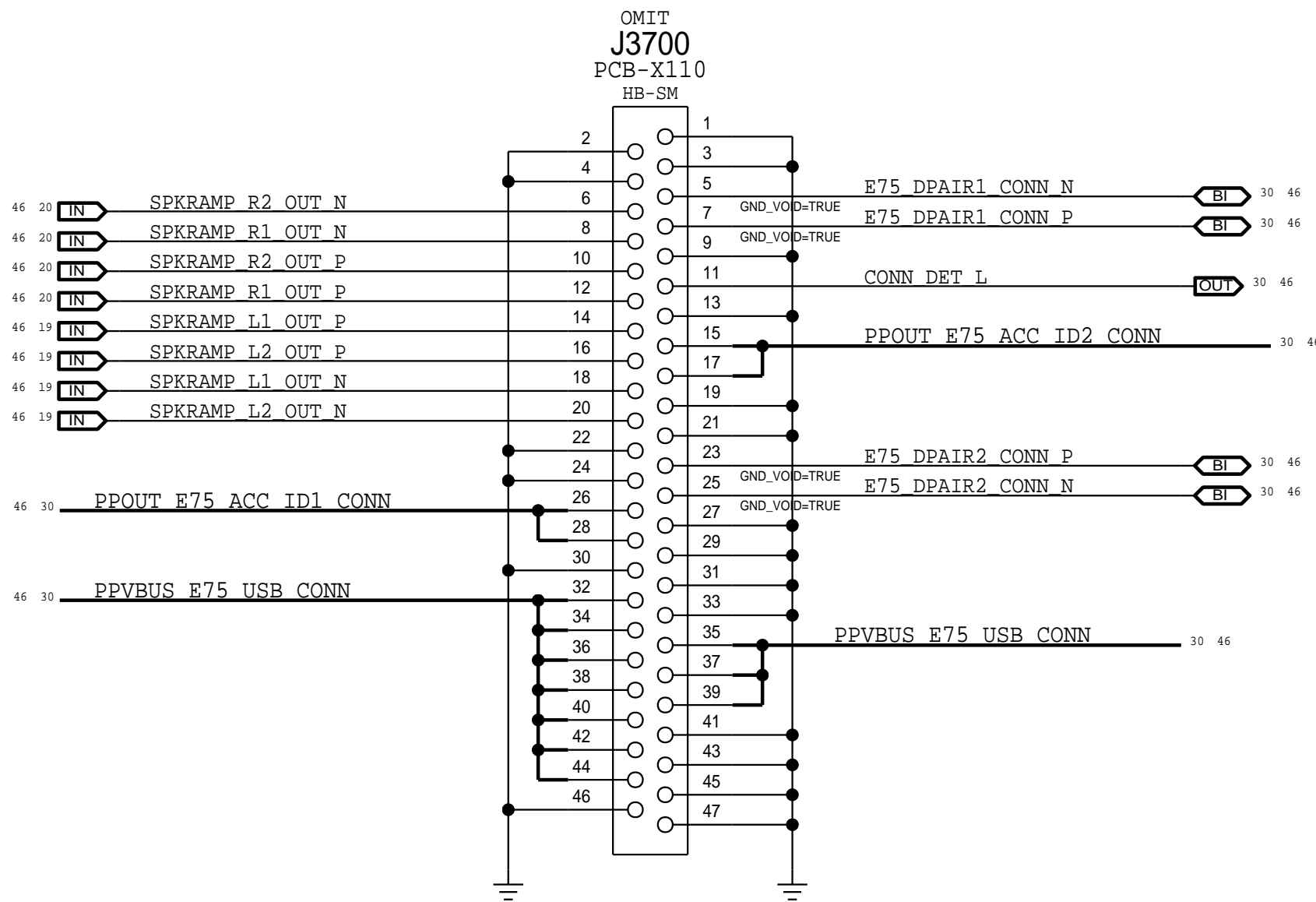
TOUCH: KONA #2



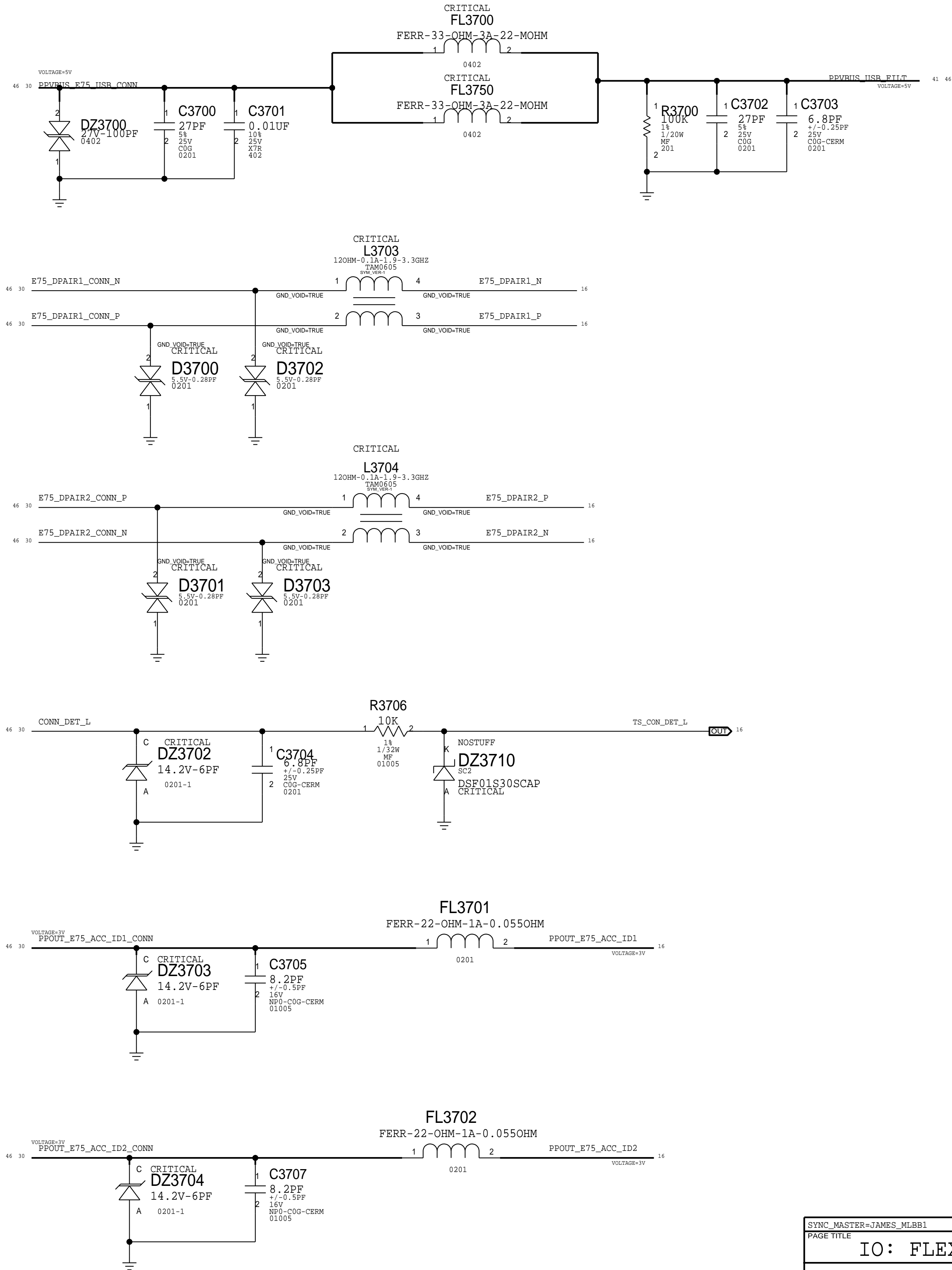


IO FLEX HOTBAR PADS

MLB 998-5877  
FLEX 998-5876



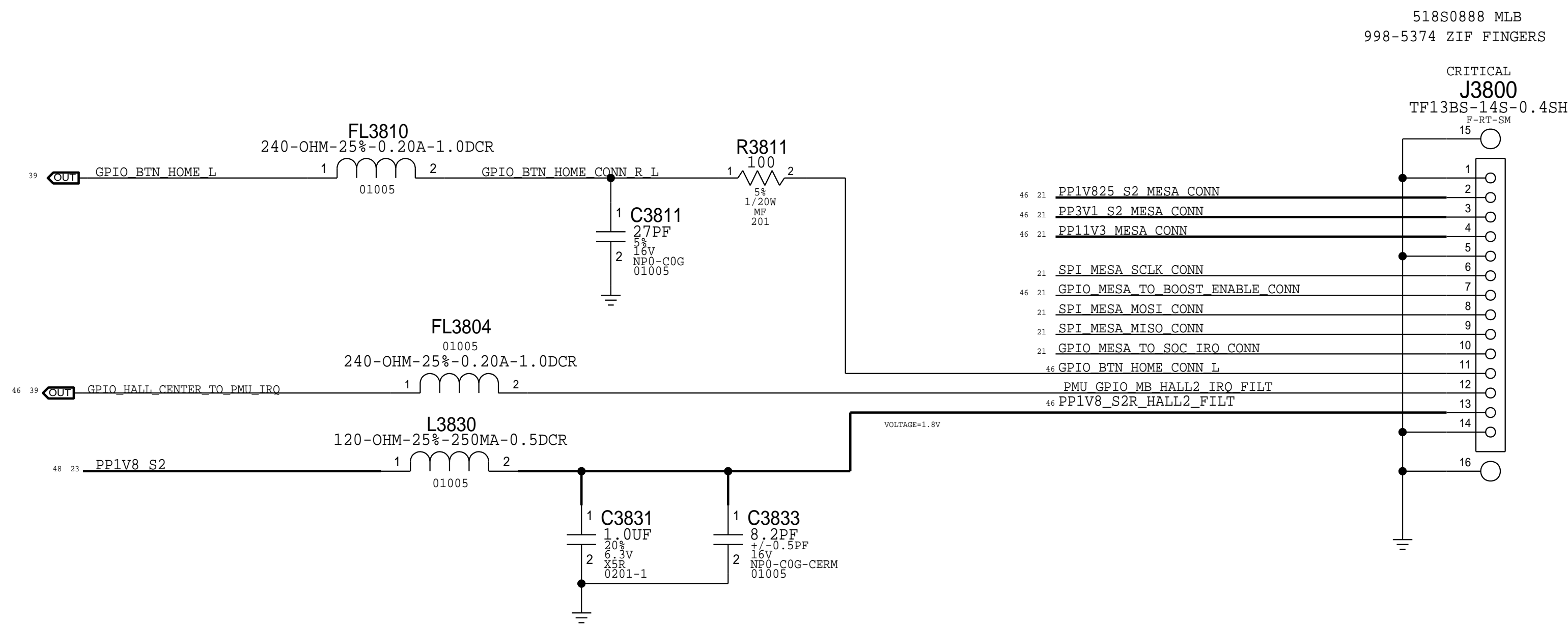
PINOUT MATCHES IO\_FLEX 4.2.0 3/12/13



SYNC\_MASTER=JAMES\_MLB1  
PAGE TITLE

IO: FLEX HOTBAR & FILTERS

HALL-SENSOR-HOME-BUTTON-MESA FLEX CONN

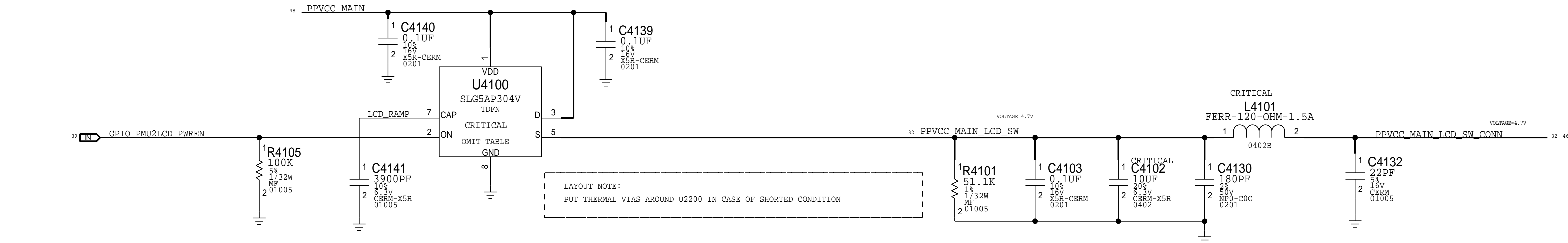


SYNC\_MASTER=JAMES\_MLBB1 SYNC\_DATE=12/20/2017

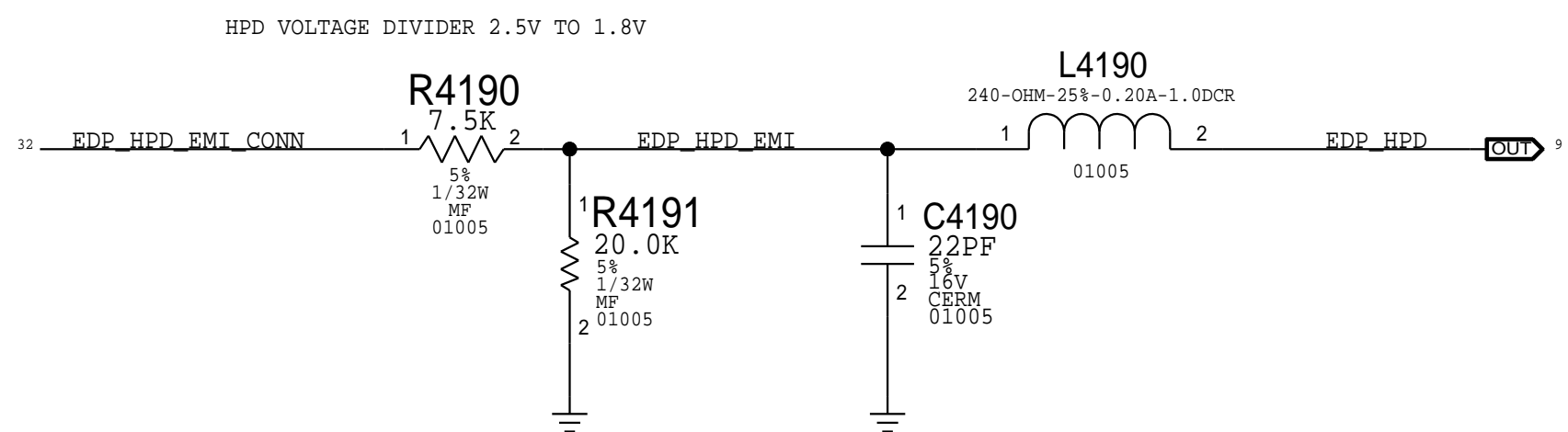
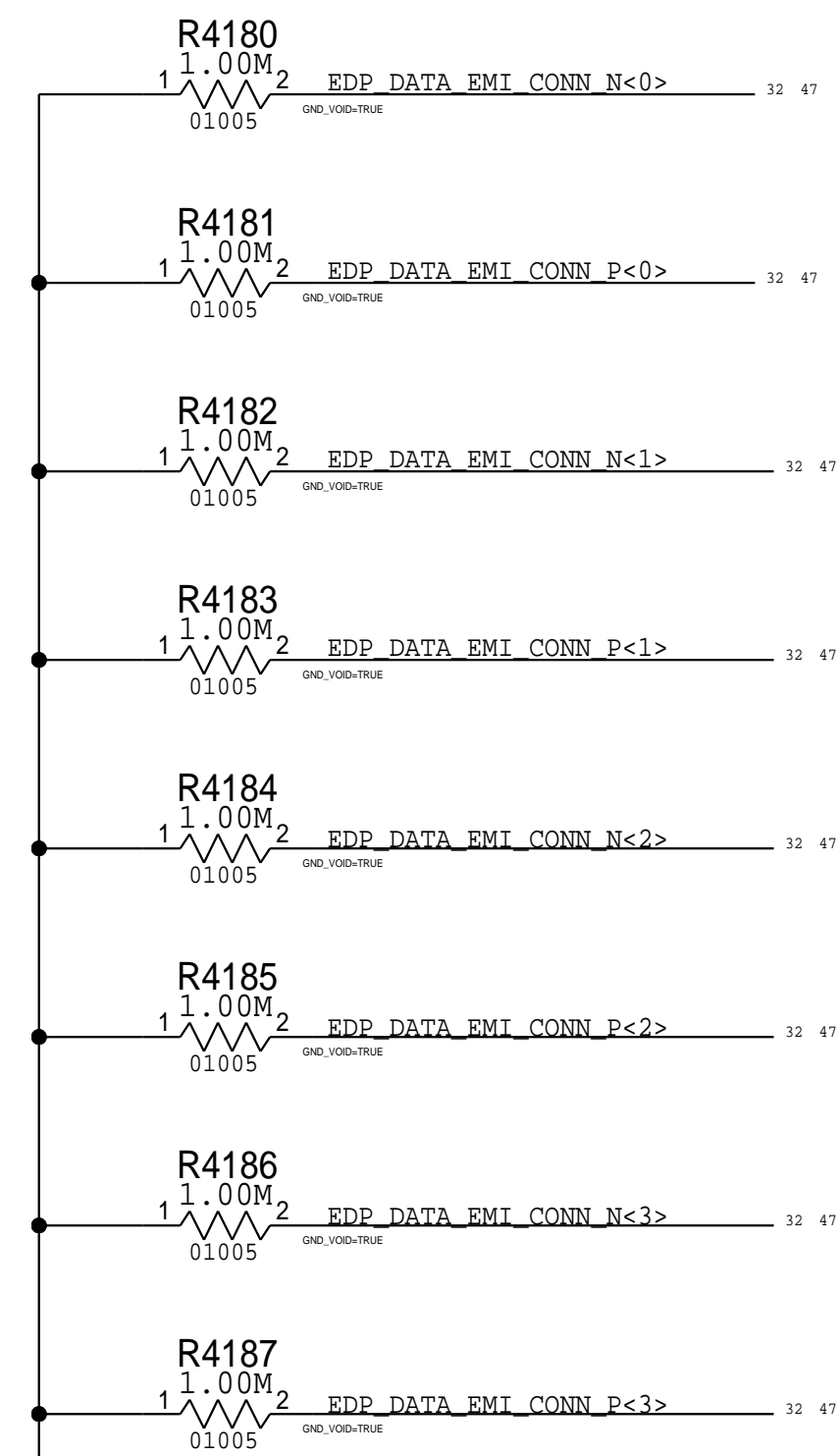
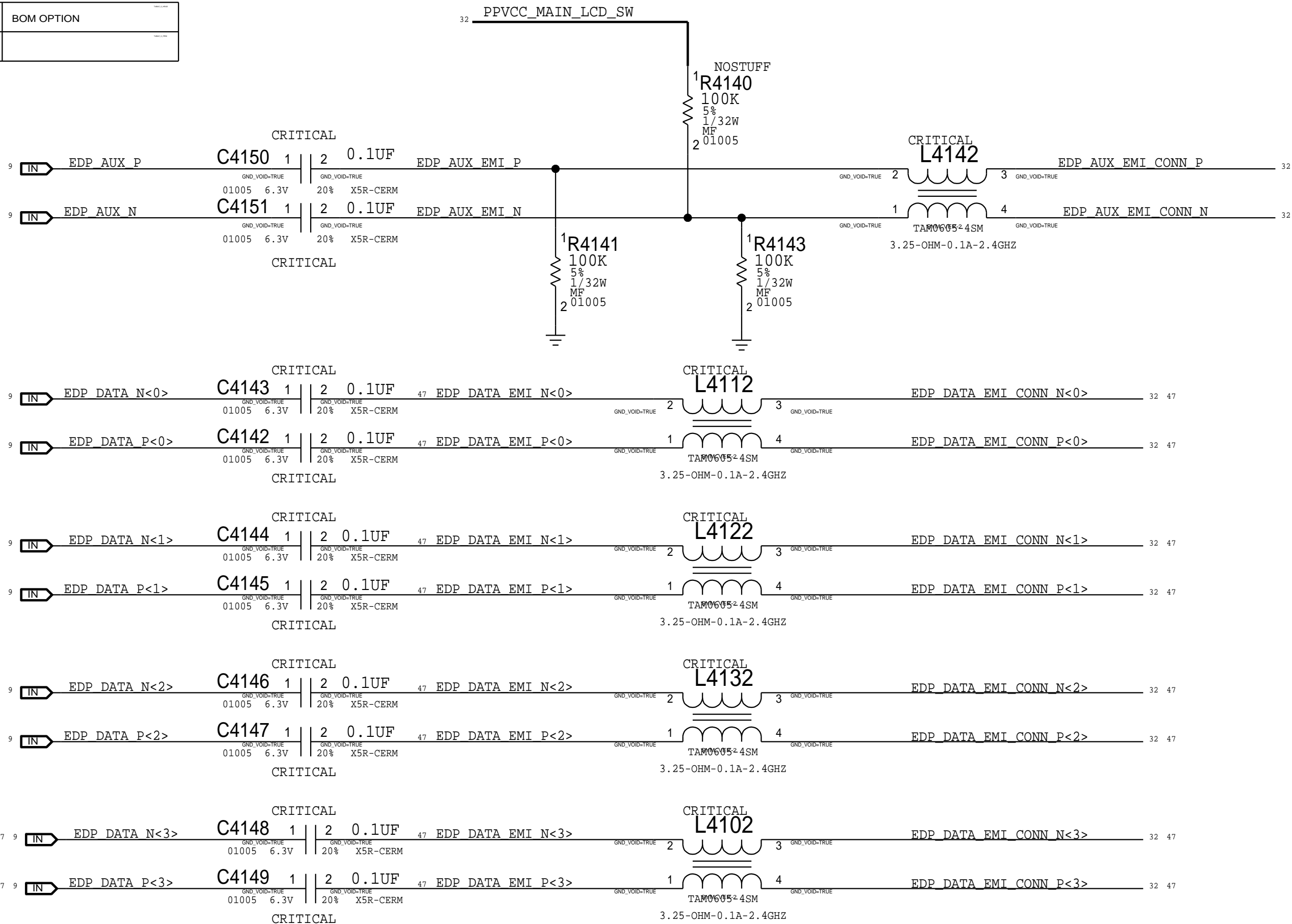
PAGE TITLE

SENSOR-BTN: HALL, HOME & MESA

EDP CONNECTOR SUPPORT

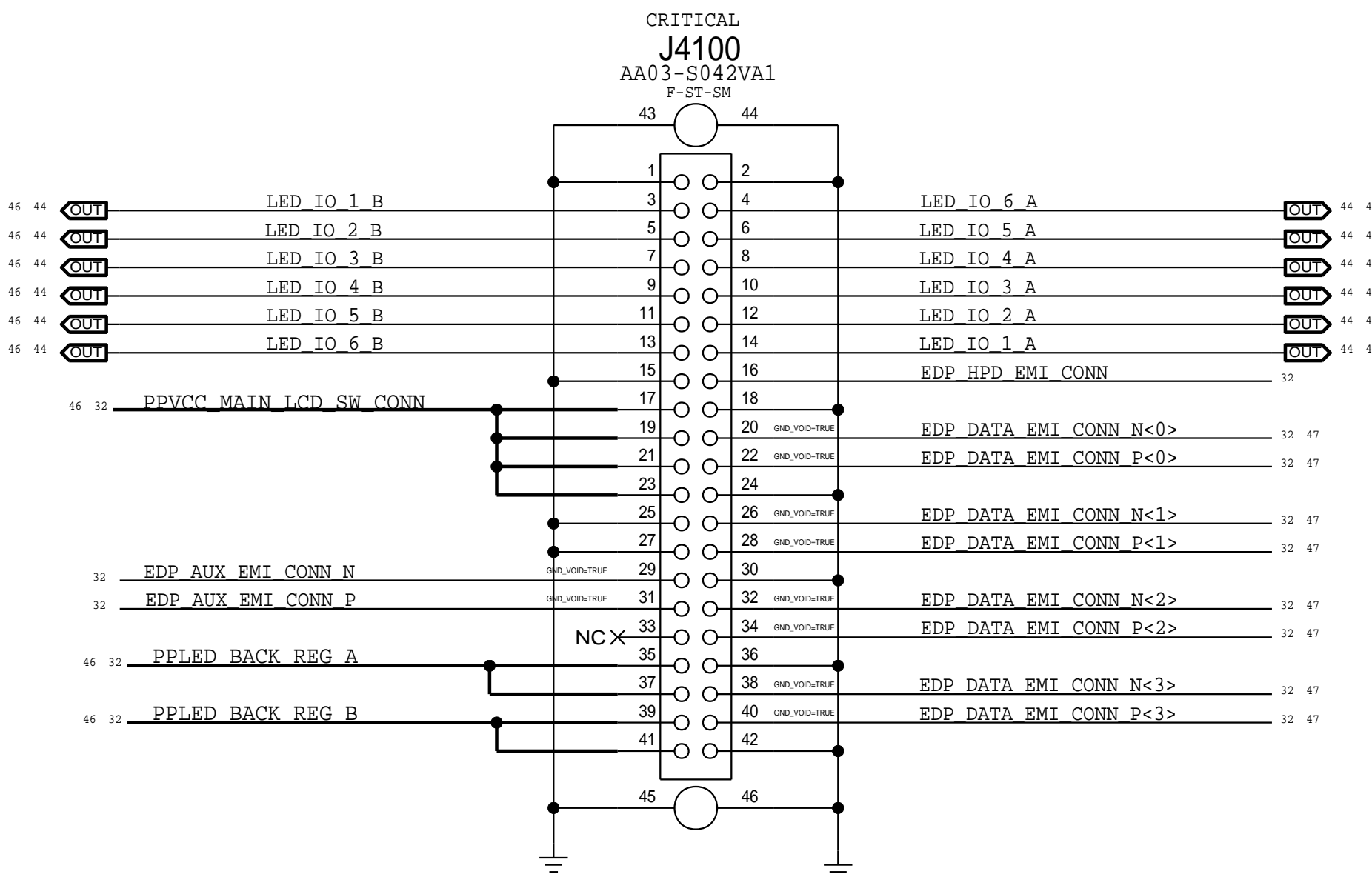


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4272	1	IC,SLG5AP1423V	U4100	CRITICAL	



EDP CONNECTOR

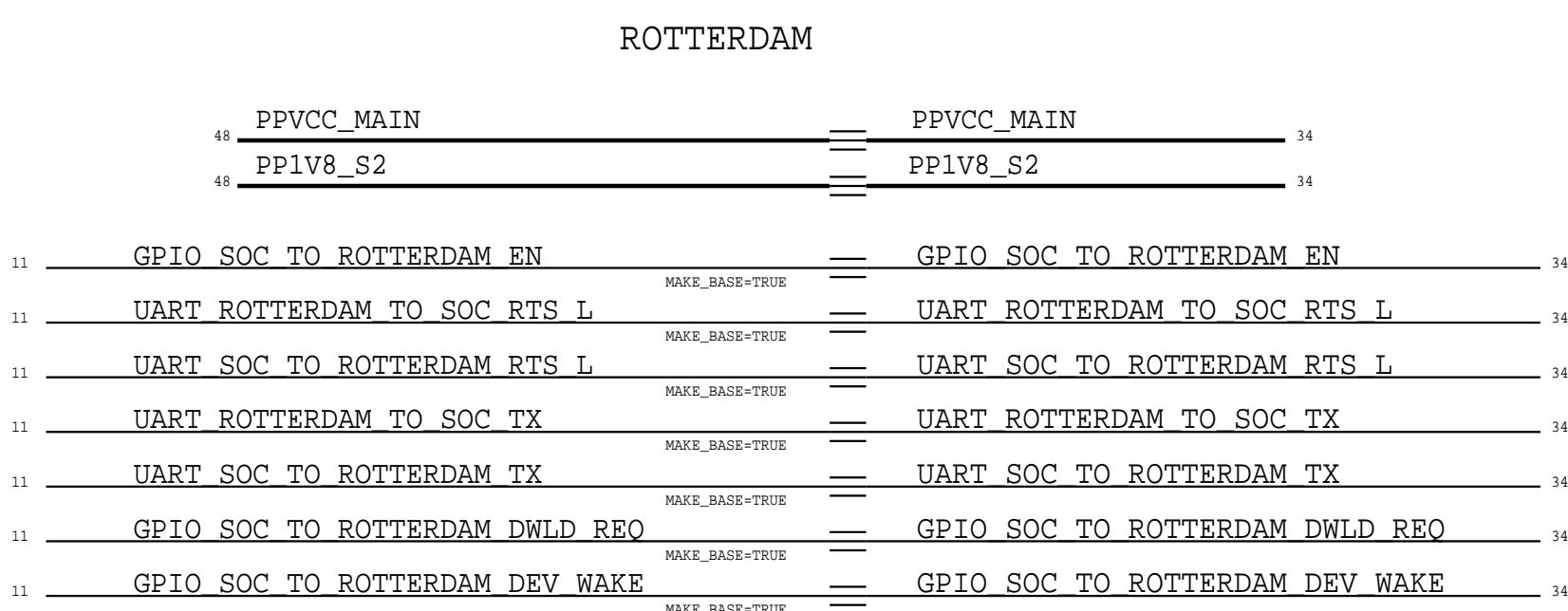
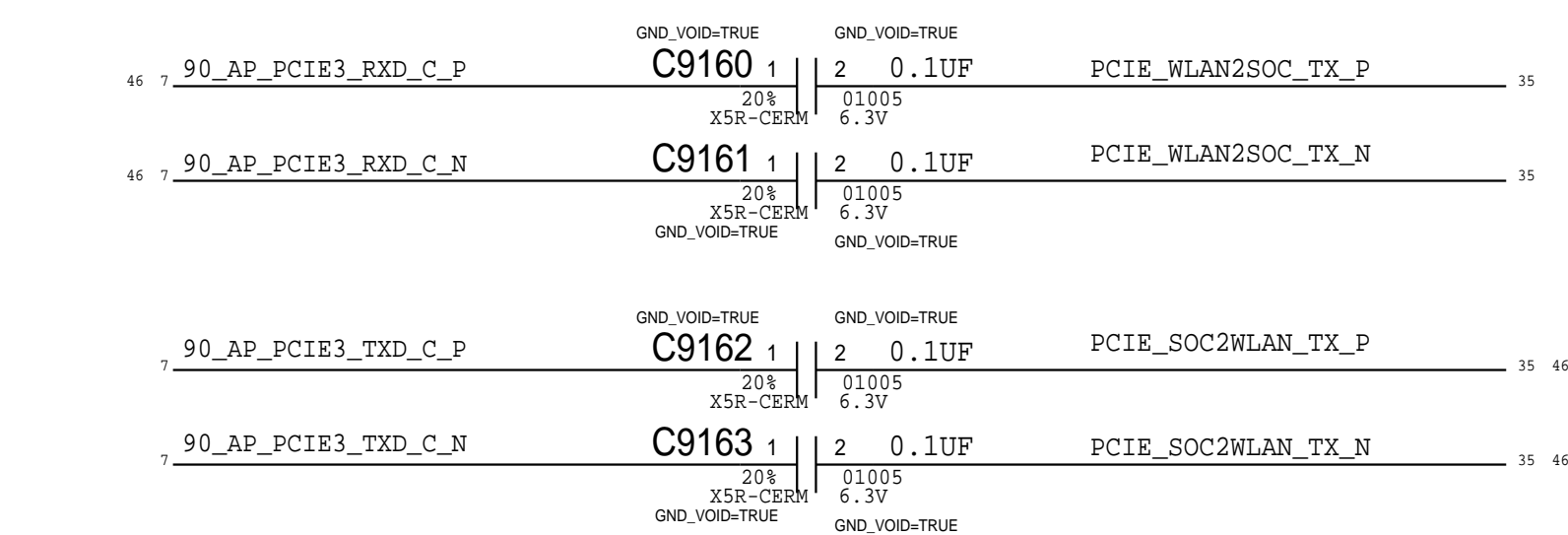
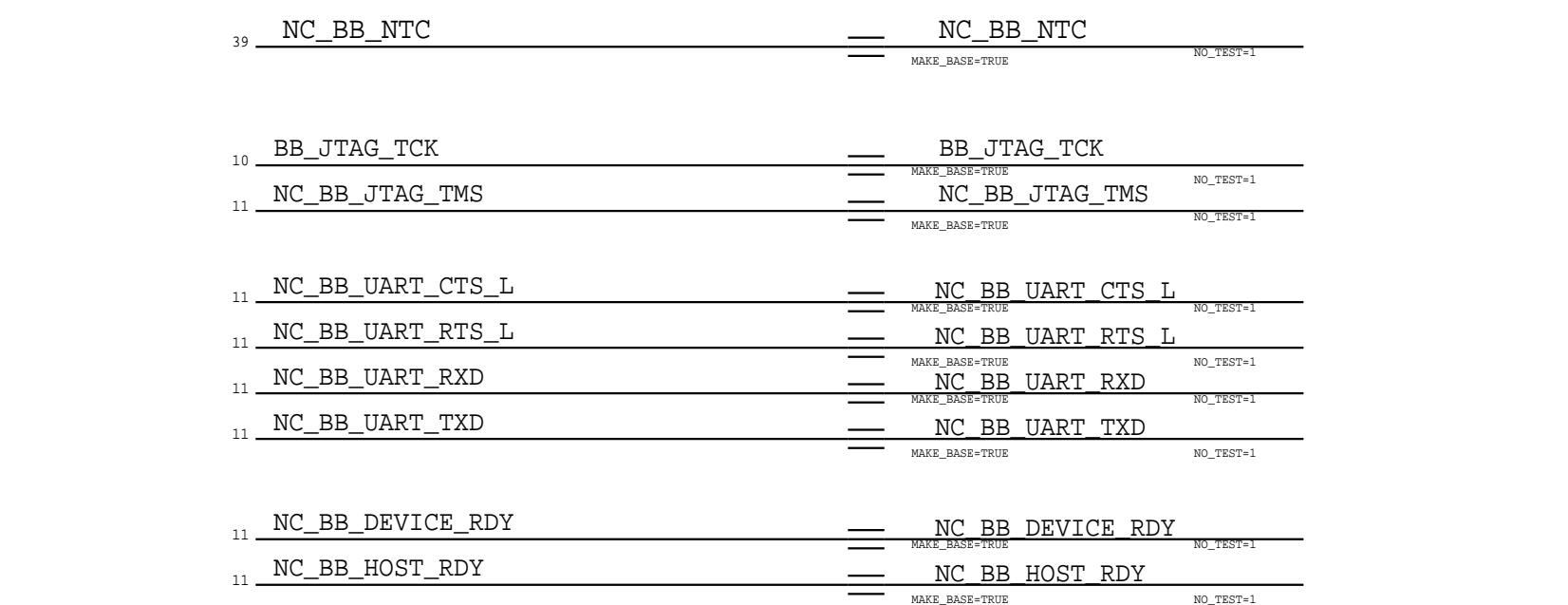
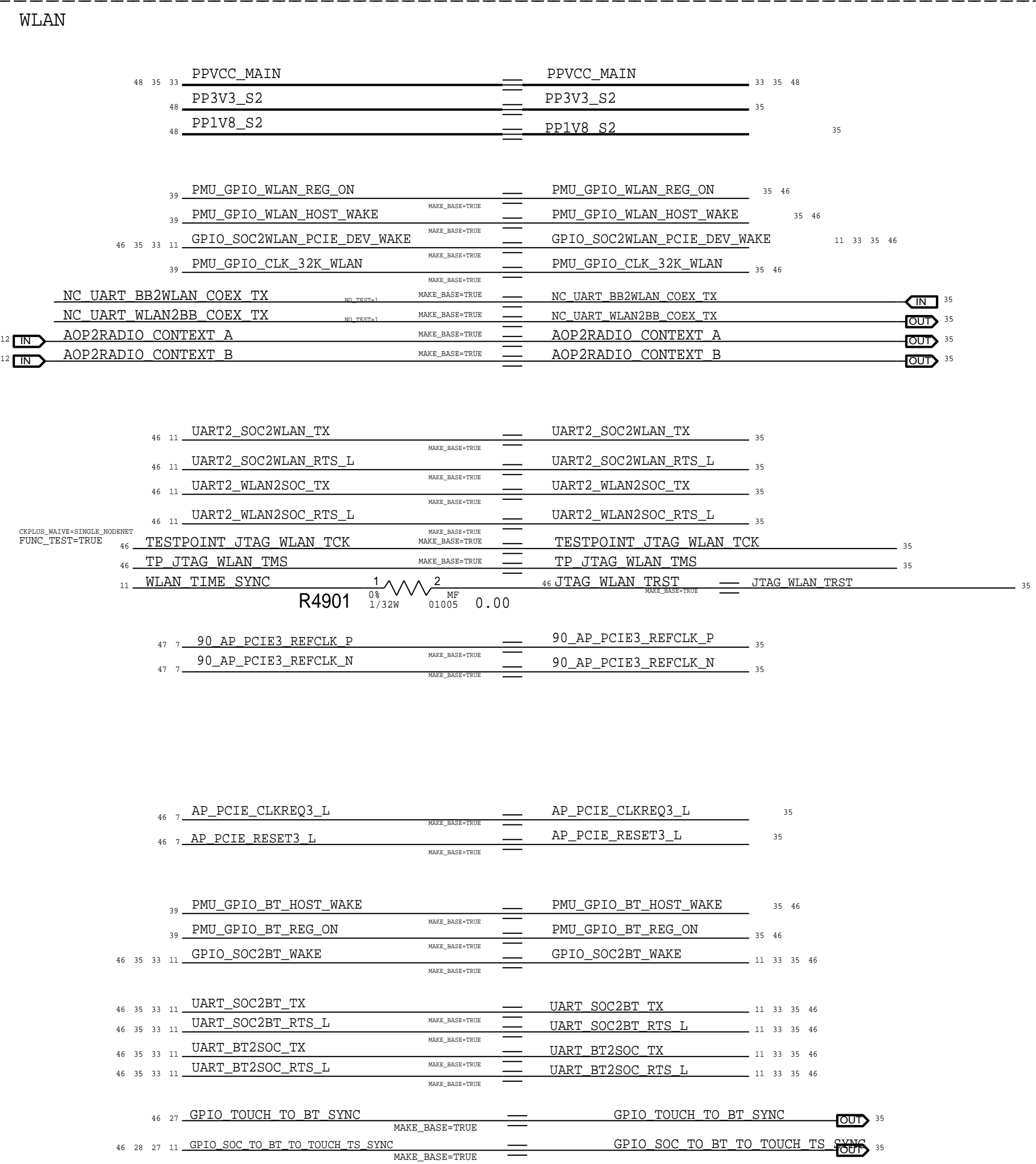
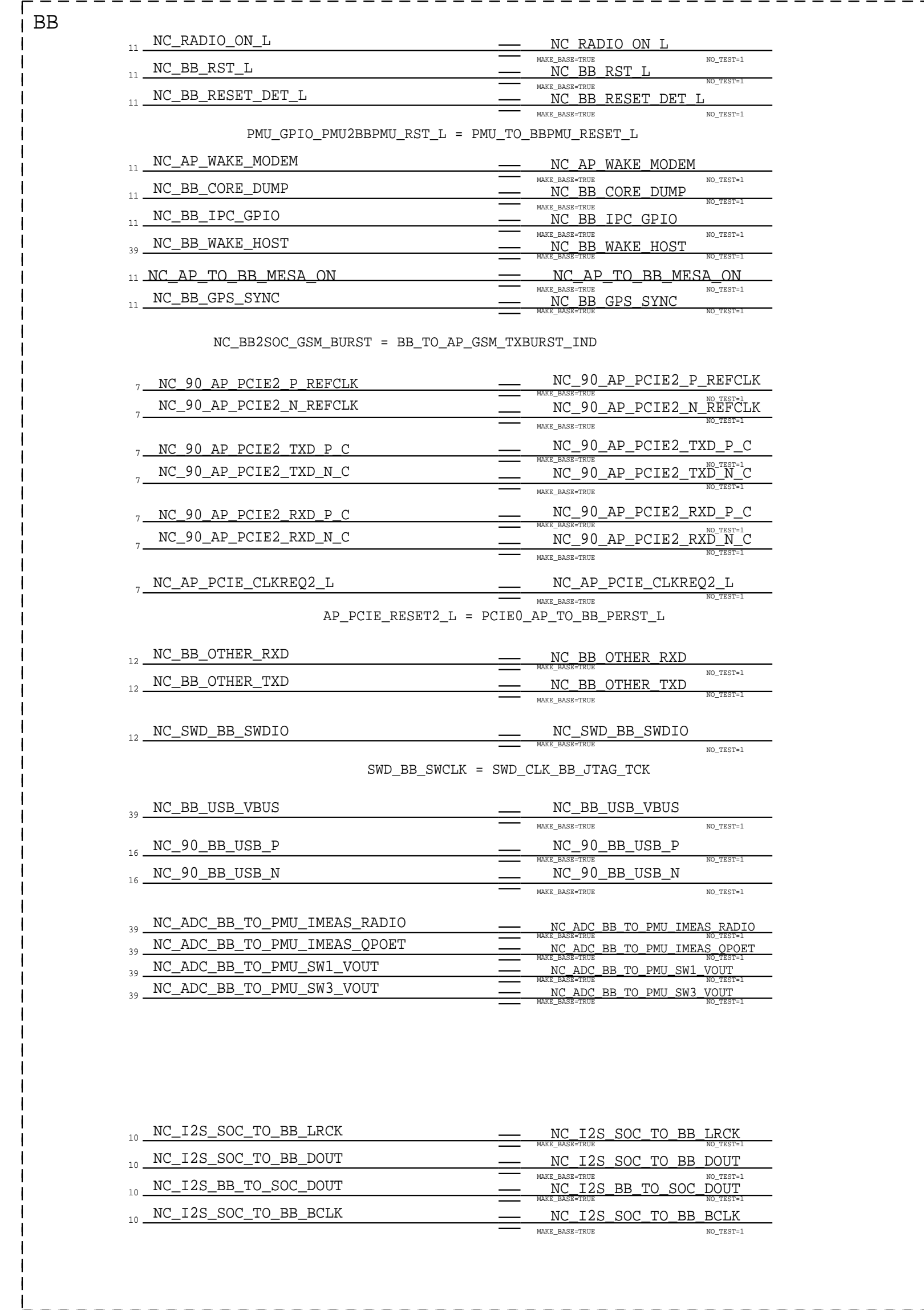
PINOUT MATCHES DISPLAY\_EDP\_FLEX 1.0.0 1/7/13  
APN 516S0784



SYNC\_MASTER=JAMES\_MLB81 SYNC\_DATE=12/20/2017

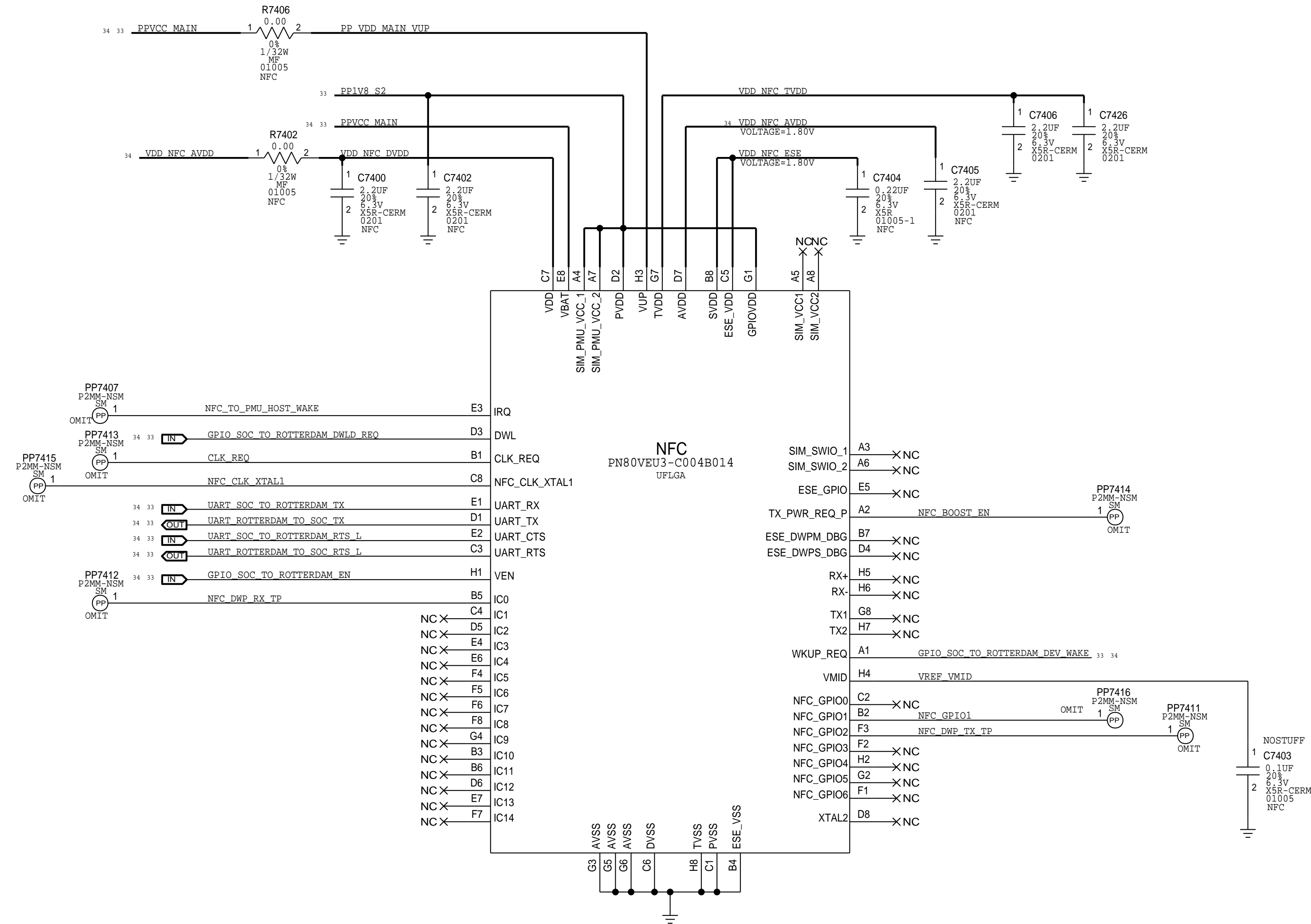
PAGE TITLE  
DISPLAY: EDP CONN



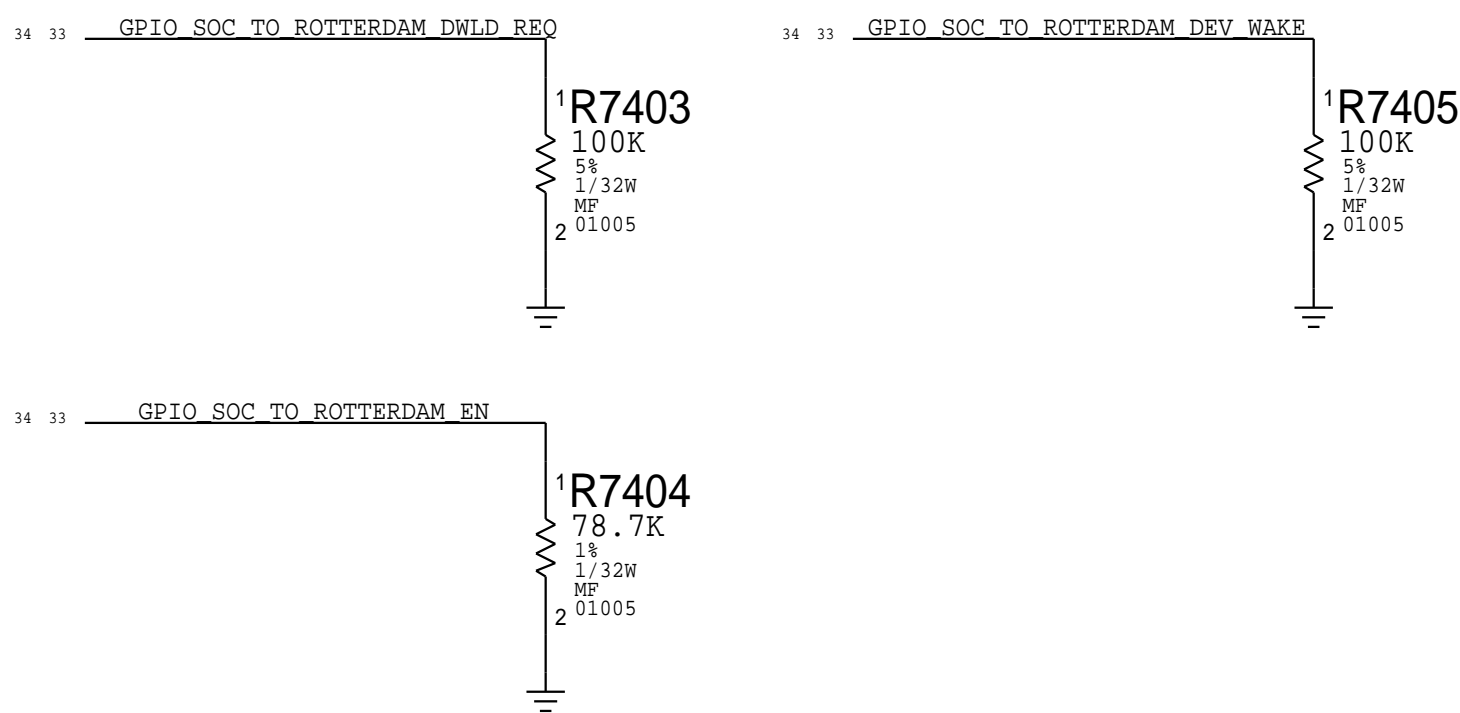


# STOCKHOLM

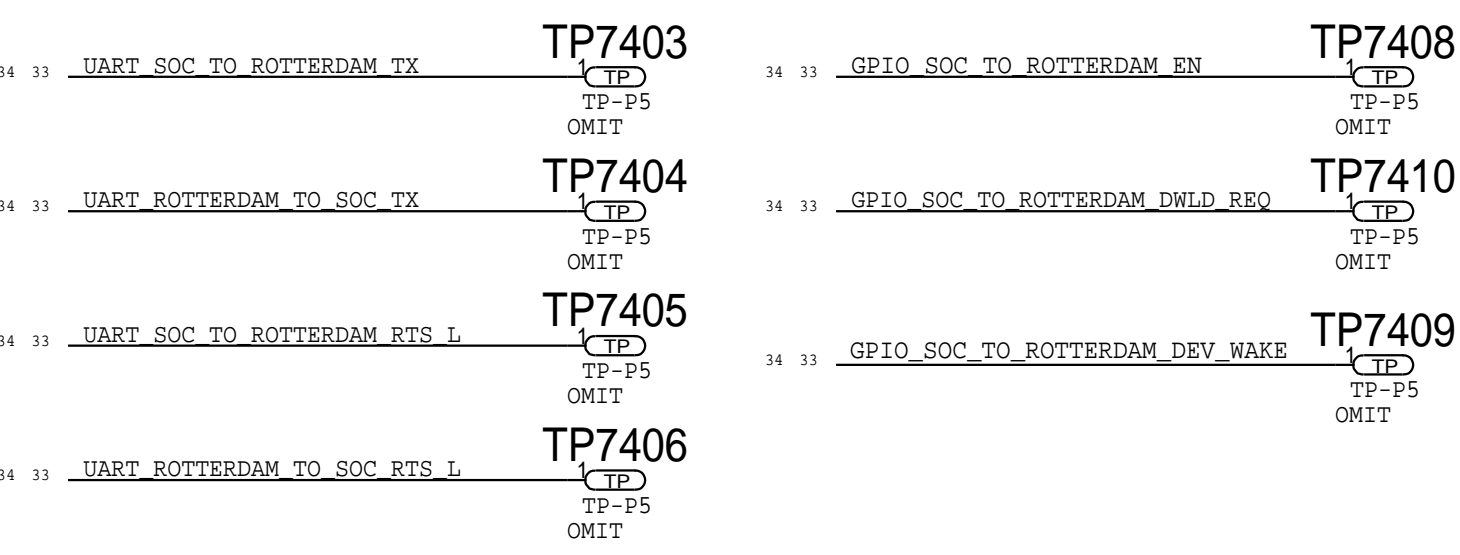
## SECURE ELEMENT CONTROLLER



## PULL DOWN

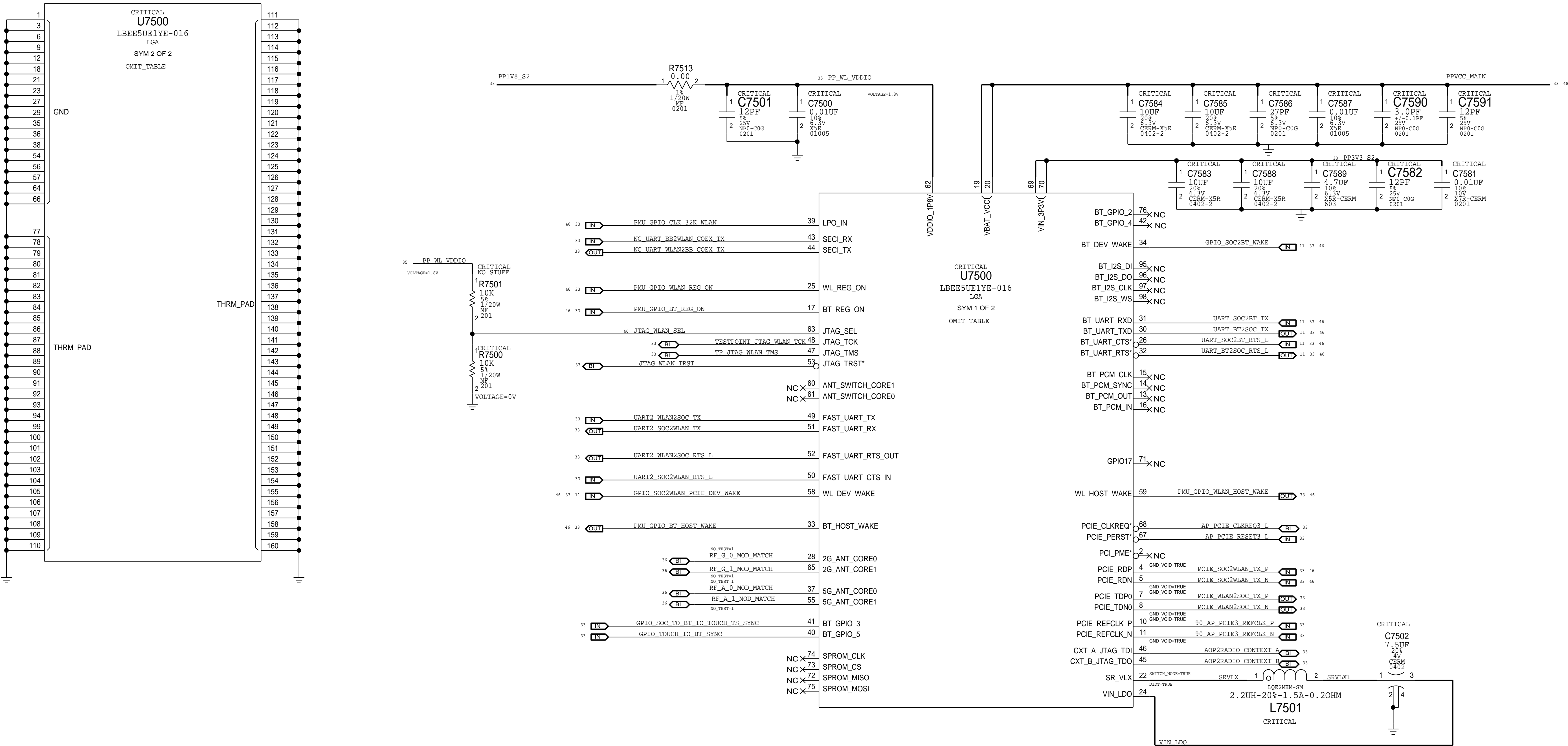


## PROBE POINTS



SYNC_MASTER=SECUREELEMENT		SYNC_DATE=02/13/2018	
PAGE TITLE			
SECURE ELEMENT			

WIFI/BT: J71B/72B: YEBISU MODULE, POWER, I/O



MODULE: USI ALTERNATES FOR MUR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00447	339S00445		U7500	USI ALT FOR MUR
339S00448	339S00446		U7500	CIDRE USI ALT FOR MUR

MODULE: BOM OPTION FOR CIDRE IN MLB\_A, NOT IN MLB\_B

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00445	1	YEBISU MURATA ES2	U7500	CRITICAL	MLB_B
339S00446	1	YEBISU CIDRE MURATA ES2	U7500	CRITICAL	MLB_A

LAST UPDATED: 06/15/2017

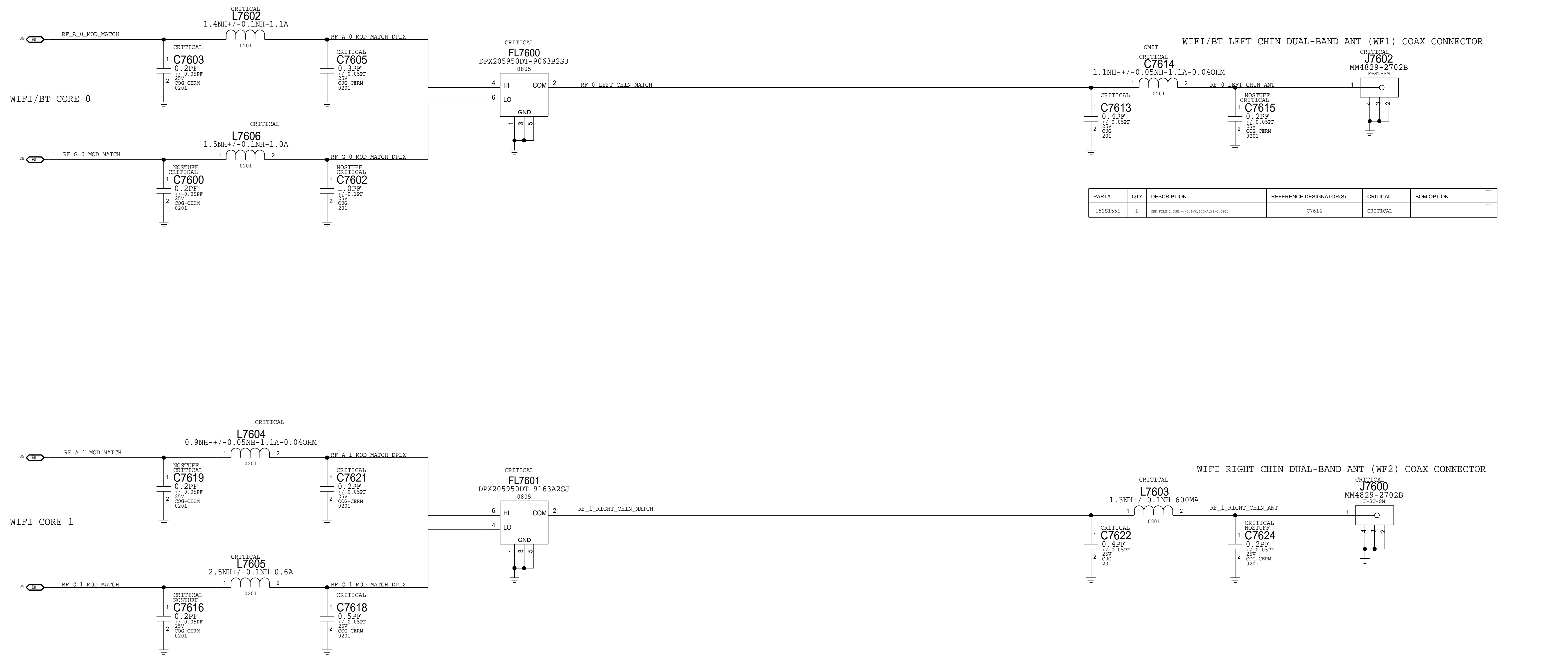
SYNC\_MASTER=WIFI\_MLB SYNC\_DATE=11/16/2017

PAGE TITLE

WIFI/BT: MODULE



WIFI/BT: J71B (WIFI/BT ONLY) RF FRONT END



LAST UPDATED: 06/12/2017

SYNC\_MASTER=WIFI\_MLB SYNC\_DATE=11/16/2017

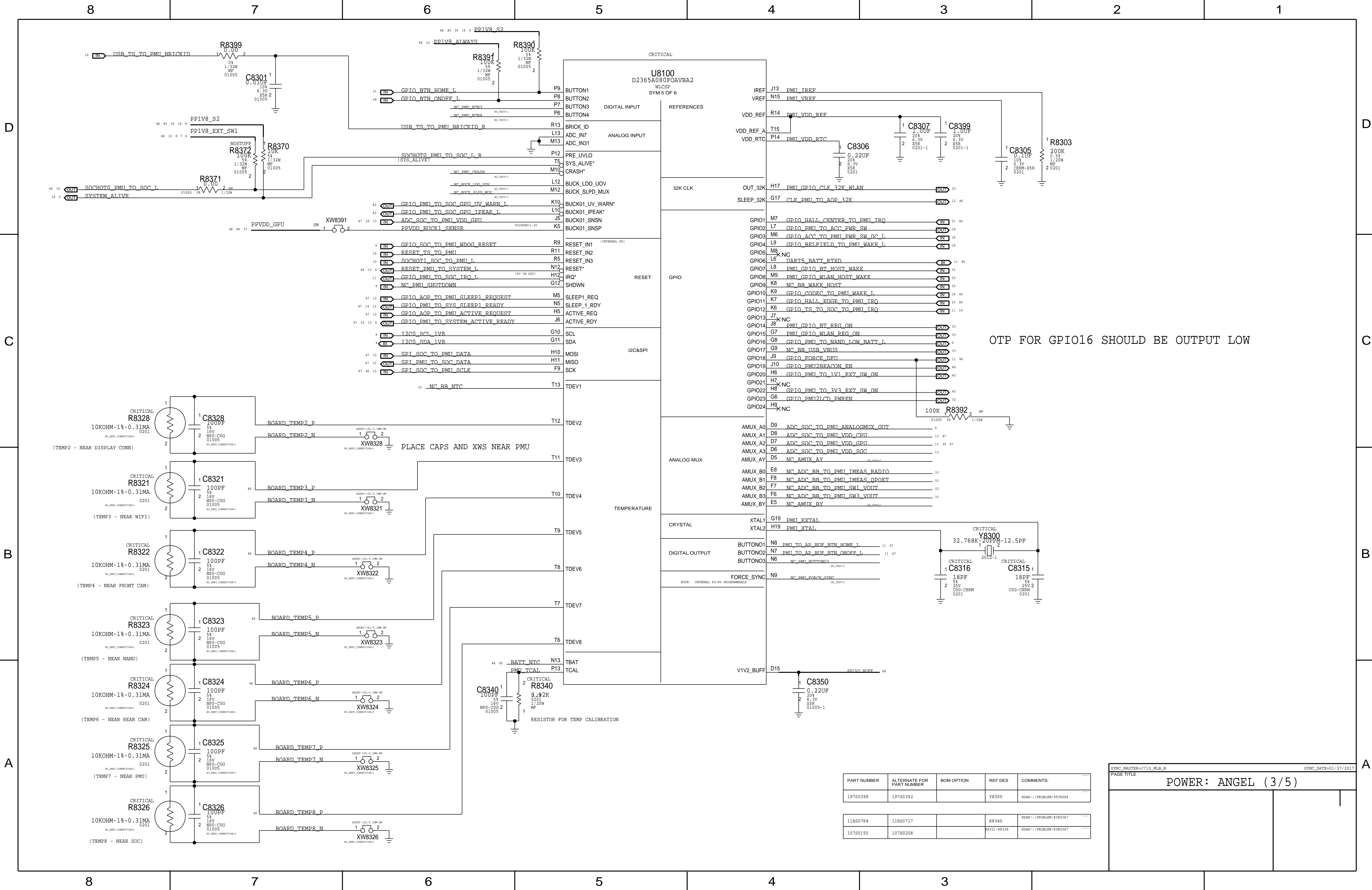
PAGE TITLE

WIFI/BT: J71B FRONT END









OTP FOR GPIO16 SHOULD BE OUTPUT LOW

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392		Y8300	RDAR: //PROBLEM/9936684
118S0764	118S0717		R8340	RDAR: //PROBLEM/6380367
107S0150	107S0208		R8321-R8328	RDAR: //PROBLEM/6380367

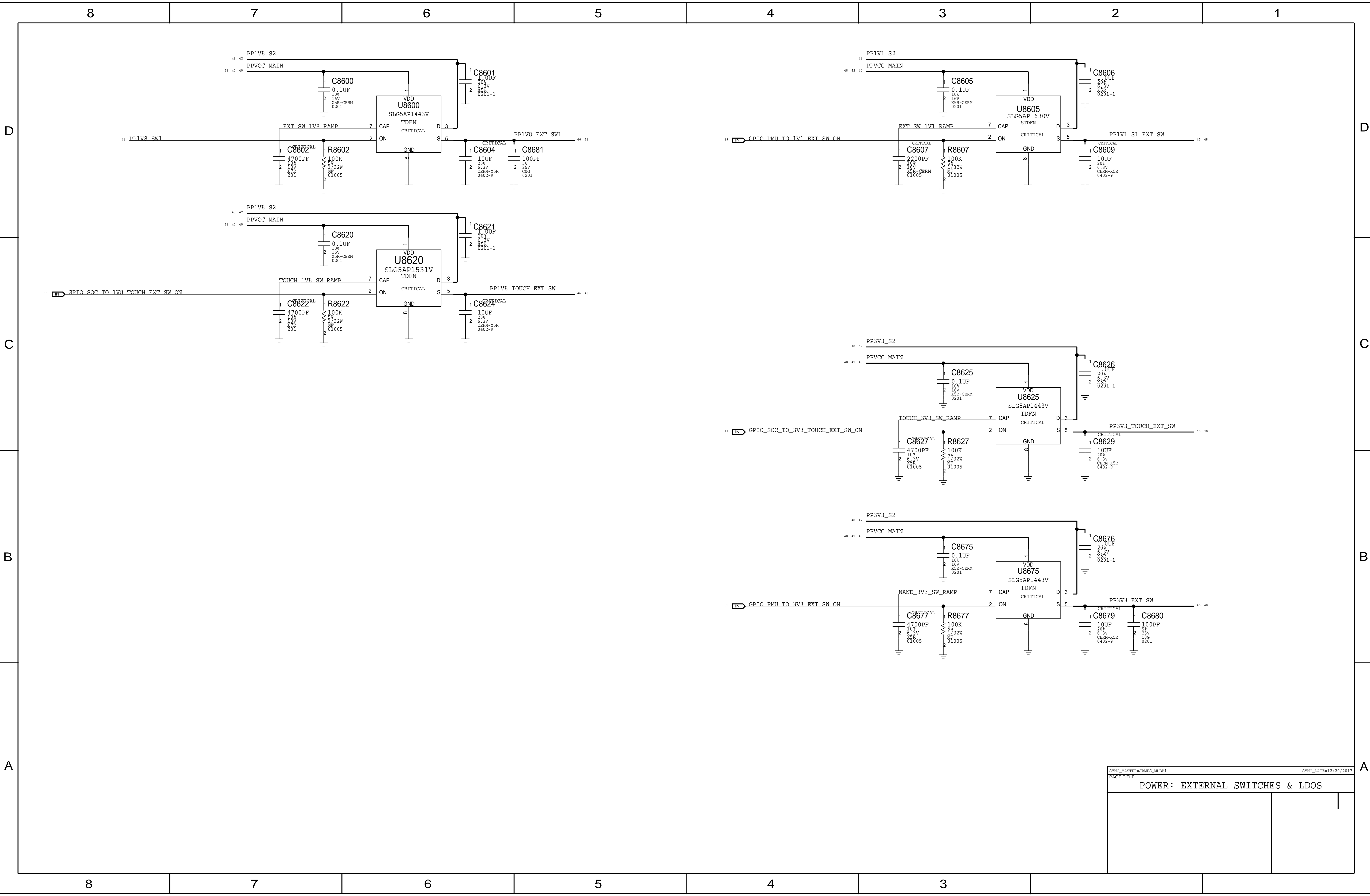
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PAGE TITLE

POWER: ANGEL (3/5)





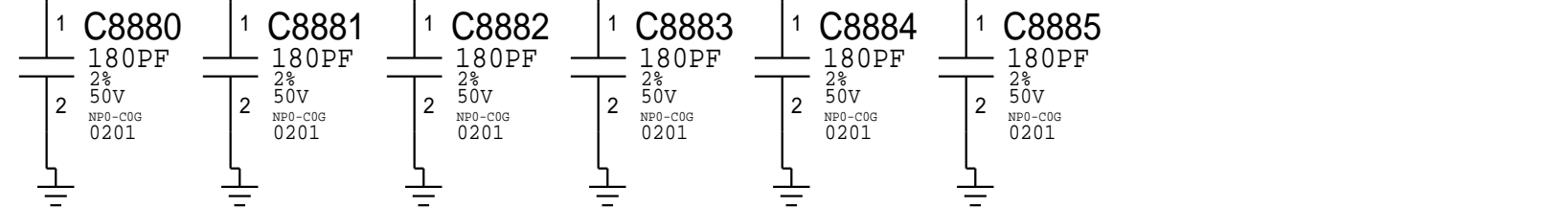
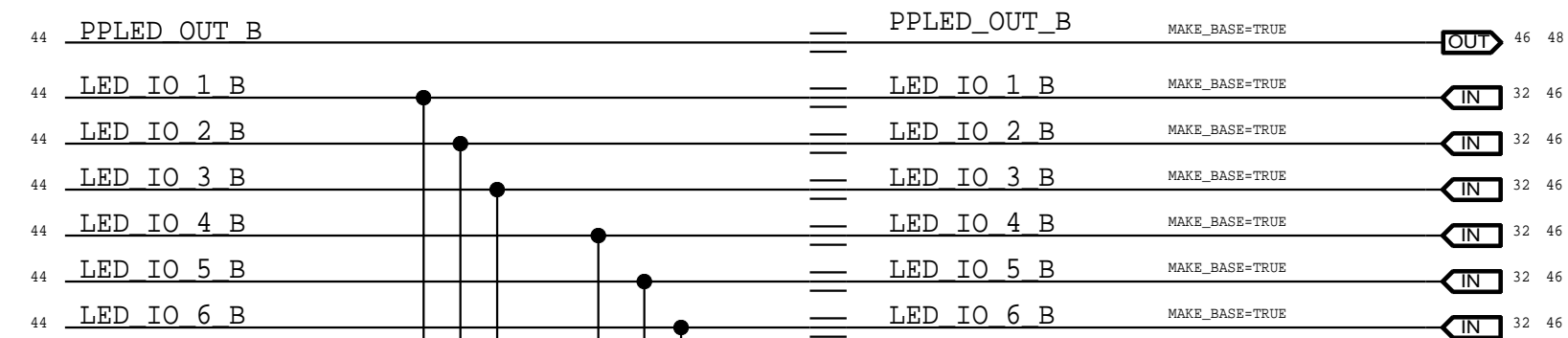
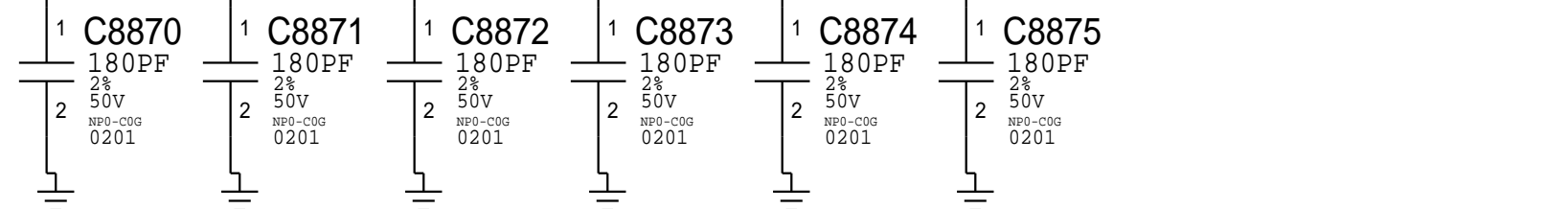
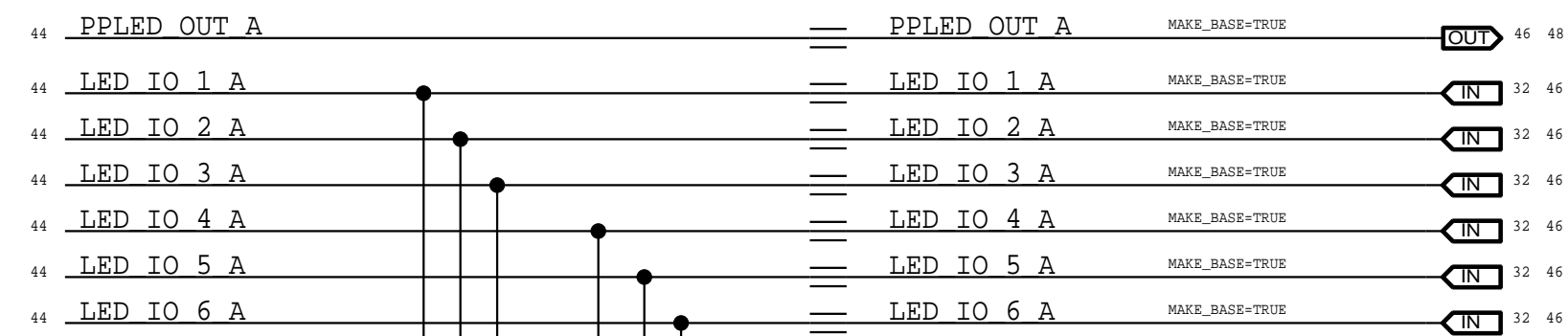
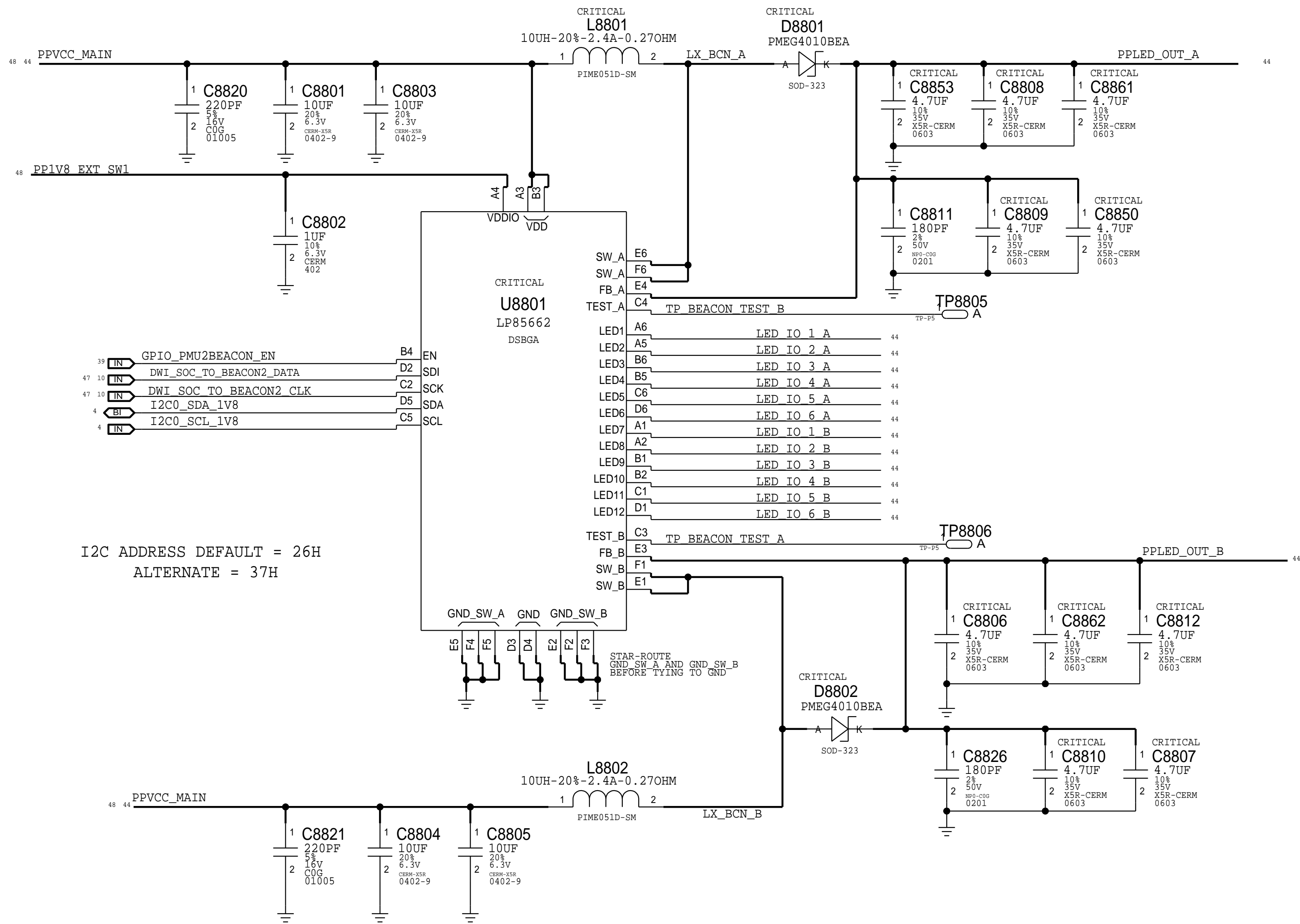








BEACON 2



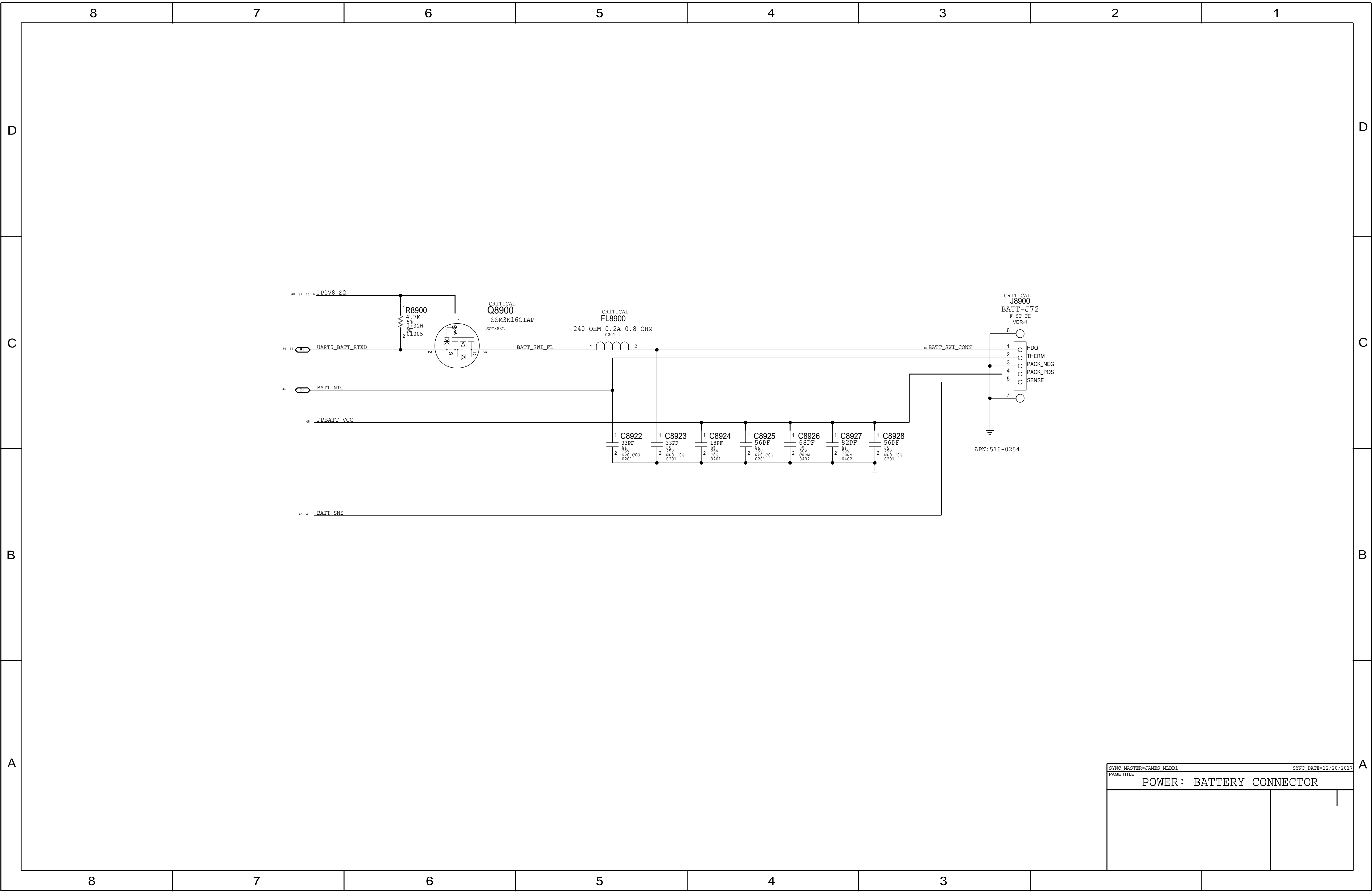
DIODE ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

SYNC\_MASTER=JAMES\_MLB11 SYNC\_DATE=12/20/2017

PAGE TITLE

BEACON2









8

7

6

5

4

3

2

1

EE CHARACTERIZATION PP

NAND

PLACE NEAR U0601	PP9402	PP	1	90_PCIE_AP_TO_NAND_REFCLK_P	5	7
	PP9403	PP	1	90_PCIE_AP_TO_NAND_REFCLK_N	5	7
	PP9434	PP	1	CLK_SOC_TO_NAND_24MHZ	5	10

PMU/BEACON2 SPI/DWI

PLACE NEAR U8100	PP9407	PP	1	SPI_SOC_TO_PMU_DATA	10	39
PLACE NEAR U8801	PP9408	PP	1	DWI_SOC_TO_BEACON2_CLK	10	44
	PP9409	PP	1	DWI_SOC_TO_BEACON2_DATA	10	44
PLACE NEAR U0600	PP940A	PP	1	SPI_SOC_TO_PMU_SCLK	10	39 46
	PP940B	PP	1	SPI_PMU_TO_SOC_DATA	10	39

PP9441	PP	1	GPIO_AOP_TO_PMU_SLEEP1_REQUEST	12	39
PP9442	PP	1	GPIO_PMU_TO_SYS_SLEEP1_READY	12	14 39
PP9443	PP	1	GPIO_AOP_TO_PMU_ACTIVE_REQUEST	12	39
PP9444	PP	1	GPIO_PMU_TO_SYSTEM_ACTIVE_READY	6	12 16 39

AUDIO

PLACE NEAR U1900	PP9421	PP	1	I2S0_SOC_TO_BELFIELD_MCK	10	18
PLACE NEAR U1900	PP9422	PP	1	I2S0_SOC_TO_BELFIELD_BCLK	10	18
PLACE NEAR U1900	PP9423	PP	1	I2S0_SOC_TO_BELFIELD_LRCK	10	18
PLACE NEAR U1900	PP9424	PP	1	I2S0_SOC_TO_BELFIELD_DOUT	10	18
PLACE NEAR U0600	PP9425	PP	1	I2S0_BELFIELD_TO_SOC_DOUT	10	18
PLACE NEAR U1900	PP9426	PP	1	SPI_BELFIELD_SCLK	10	18
PLACE NEAR U1900	PP9427	PP	1	SPI_BELFIELD_MOSI	10	18
PLACE NEAR U0600	PP9428	PP	1	SPI_BELFIELD_MISO	10	18
PLACE NEAR U1900	PP9460	PP	1	I2S_AOP_TO_CODEC_BCLK	12	18
PLACE NEAR U1900	PP9461	PP	1	I2S_AOP_TO_CODEC_LRCK	12	18
PLACE NEAR U1900	PP9462	PP	1	I2S_AOP_TO_CODEC_DOUT	12	18
PLACE NEAR U0600	PP9463	PP	1	I2S_CODEC_TO_AOP_DOUT	12	18
PLACE NEAR U2040	PP9464	PP	1	I2S2_SOC_TO_SPKRAMP_BCLK_L1	19	
PLACE NEAR U2040	PP9465	PP	1	I2S2_SOC_TO_SPKRAMP_LRCK_L1	19	
PLACE NEAR U2040	PP9466	PP	1	I2S2_SOC_TO_SPKRAMP_DOUT_L1	19	

SENSORS

PLACE NEAR U2590	PP9429	PP	1	SPI_AOP_SCLK	12	23 47
PLACE NEAR U2590	PP9430	PP	1	SPI_AOP_MOSI	12	23 47
PLACE NEAR U2580	PP9431	PP	1	SPI_AOP_SCLK	12	23 47
PLACE NEAR U2580	PP9432	PP	1	SPI_AOP_MOSI	12	23 47
PLACE NEAR U0600	PP9433	PP	1	SPI_AOP_MISO	12	23

MESA SPI

PLACE NEAR U0600	PP940C	PP	1	SPI_MESA_MISO	10	21
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CAMERA - FRONT

PP940D	PP	1	MIPI1C_CAM_FRONT_CLK_P	8	25 47
PP940E	PP	1	MIPI1C_CAM_FRONT_CLK_N	8	25 47
PP940F	PP	1	MIPI1C_CAM_FRONT_DATA_P<0>	8	25 47
PP9410	PP	1	MIPI1C_CAM_FRONT_DATA_N<0>	8	25 47

CAMERA - REAR

PP9411	PP	1	MIPI0C_CAM_REAR_CLK_P	8	26 47
PP9412	PP	1	MIPI0C_CAM_REAR_CLK_N	8	26 47
PP9413	PP	1	MIPI0C_CAM_REAR_DATA_P<0>	8	26 47
PP9414	PP	1	MIPI0C_CAM_REAR_DATA_N<0>	8	26 47

WIFI

PP9417	PP	1	90_AP_PCIE3_REFCLK_P	7	33
PP9418	PP	1	90_AP_PCIE3_REFCLK_N	7	33

SOC

PP9450	PP	1	ADC_SOC_TO_PMU_VDD_CPU	13	39
PP9451	PP	1	AP_VSS_CPU_SENSE	13	
PP9452	PP	1	ADC_SOC_TO_PMU_VDD_GPU	13	39
PP9453	PP	1	AP_VSS_SENSE	13	
PP9480	PP	1	PMU_TO_AP_BUP_BTN_HOME_L	11	39
PP9481	PP	1	PMU_TO_AP_BUP_BTN_ONOFF_L	11	39
PP9482	PP	1	PEVDD_CPU_SRAM	37	46 48

TOUCH

PP9454	PP	1	TP_KONA_S_UART_RX	28	
PP9455	PP	1	TP_KONA_S_UART_TX	28	
PP9456	PP	1	TP_KONA_IPC_EVENT_0	28	
PP9457	PP	1	TP_KONA_IPC_EVENT_1	28	
PP9458	PP	1	TP_KONA_IPC_EVENT_2	28	
PP9459	PP	1	TP_KONA_IPC_EVENT_3	28	
PP945A	PP	1	TP_KONA_IPC_EVENT_4	28	
PP945B	PP	1	TP_KONA_IPC_EVENT_5	28	
PP945C	PP	1	KONA_S_TO_KONA_M_RESET_DET_L	27	28
PP945D	PP	1	KMSI_MISO	27	28
PP945E	PP	1	KMSI_MOSI	27	28
PP945F	PP	1	KMSI_STRB_IN	27	28
PP9470	PP	1	KMSI_STRB_OUT	27	28
PP9471	PP	1	PSE_SYNC	27	28

HIGH SPEED, NO TEST

MIPI0C_CAM_REAR_CLK_P	NO_TEST=1	8	26	47
MIPI0C_CAM_REAR_CLK_N	NO_TEST=1	8	26	47
MIPI0C_CAM_REAR_DATA_P<0..3>	NO_TEST=TRUE	8	26	47
MIPI0C_CAM_REAR_DATA_N<0..3>	NO_TEST=TRUE	8	26	47
MIPI0C_CAM_REAR_CLK_FILT_P	NO_TEST=1	26		
MIPI0C_CAM_REAR_CLK_FILT_N	NO_TEST=1	26		
MIPI0C_CAM_REAR_DATA_FILT_P<0..3>	NO_TEST=TRUE	26		
MIPI0C_CAM_REAR_DATA_FILT_N<0..3>	NO_TEST=TRUE	26		
MIPI1C_CAM_FRONT_CLK_P	NO_TEST=1	8	25	47
MIPI1C_CAM_FRONT_CLK_N	NO_TEST=1	8	25	47
MIPI1C_CAM_FRONT_DATA_P<0>	NO_TEST=1	8	25	47
MIPI1C_CAM_FRONT_DATA_N<0>	NO_TEST=1	8	25	47
MIPI1C_CAM_FRONT_CLK_FILT_P	NO_TEST=1	25		
MIPI1C_CAM_FRONT_CLK_FILT_N	NO_TEST=1	25		
MIPI1C_CAM_FRONT_DATA_FILT_P<0>	NO_TEST=1	25		
MIPI1C_CAM_FRONT_DATA_FILT_N<0>	NO_TEST=1	25		
EDP_DATA_P<0..3>	NO_TEST=TRUE	9	32	
EDP_DATA_N<0..3>	NO_TEST=TRUE	9	32	
EDP_DATA_EMI_P<0..3>	NO_TEST=TRUE	32		
EDP_DATA_EMI_N<0..3>	NO_TEST=TRUE	32		
EDP_DATA_EMI_CONN_P<0..3>	NO_TEST=TRUE	32		
EDP_DATA_EMI_CONN_N<0..3>	NO_TEST=TRUE	32		

POWER CONNECTIONS

D

C

B

A

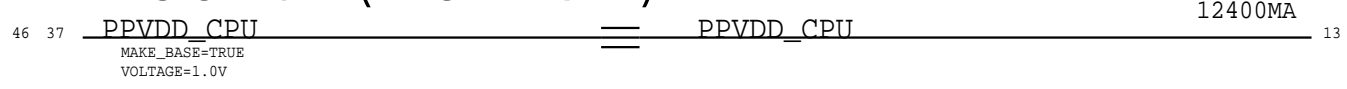
D

C

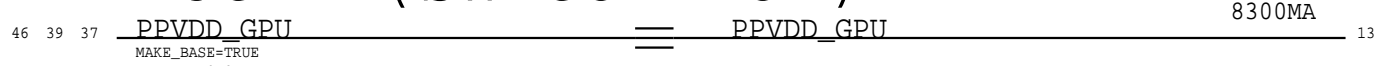
B

A

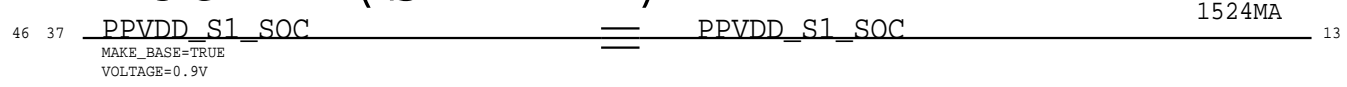
BUCK0 (ACTIVE)



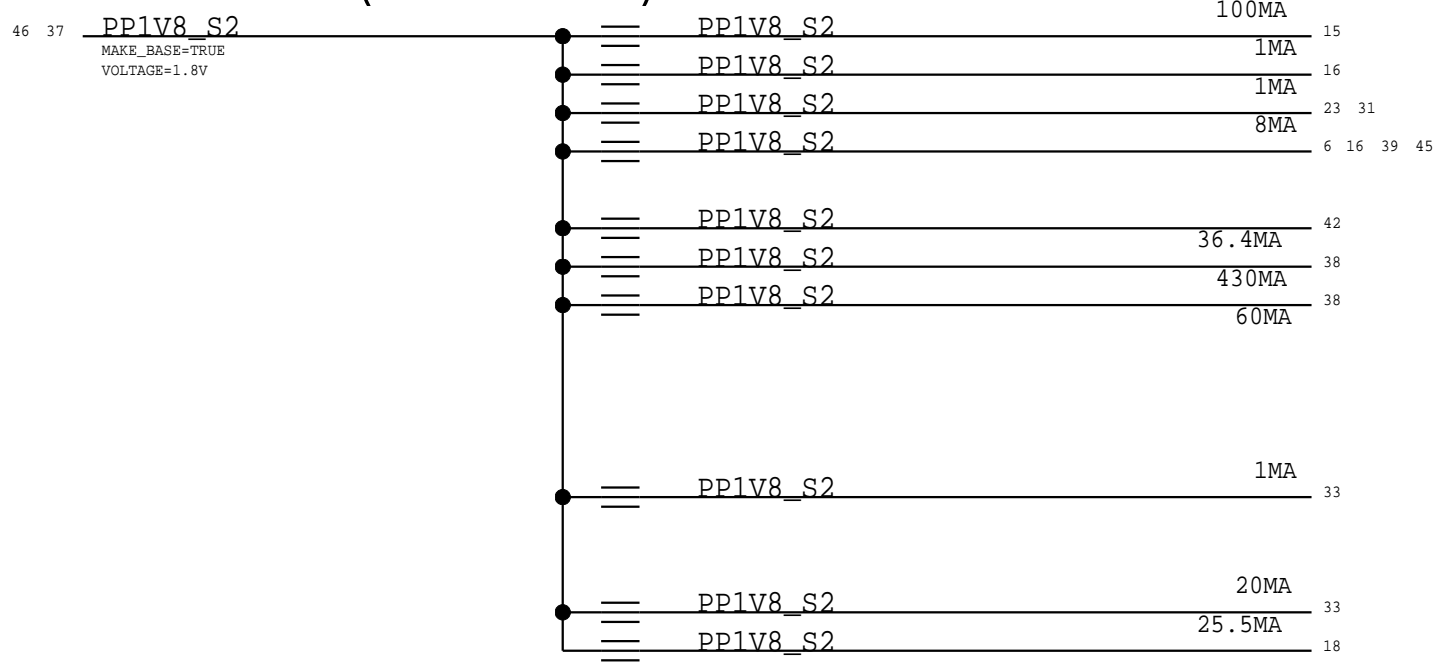
BUCK1 (SW CONTROL)



BUCK2 (SLEEP1)

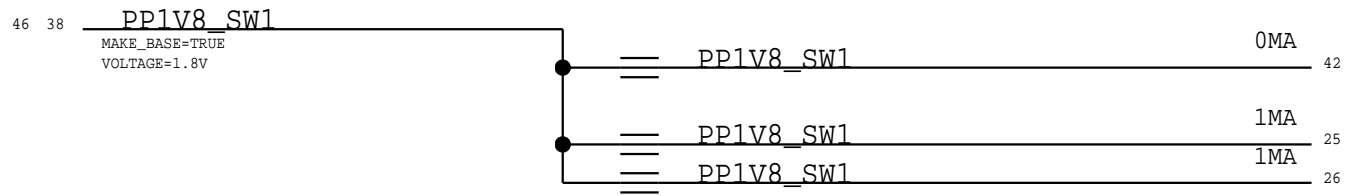


BUCK3 (SLEEP2)

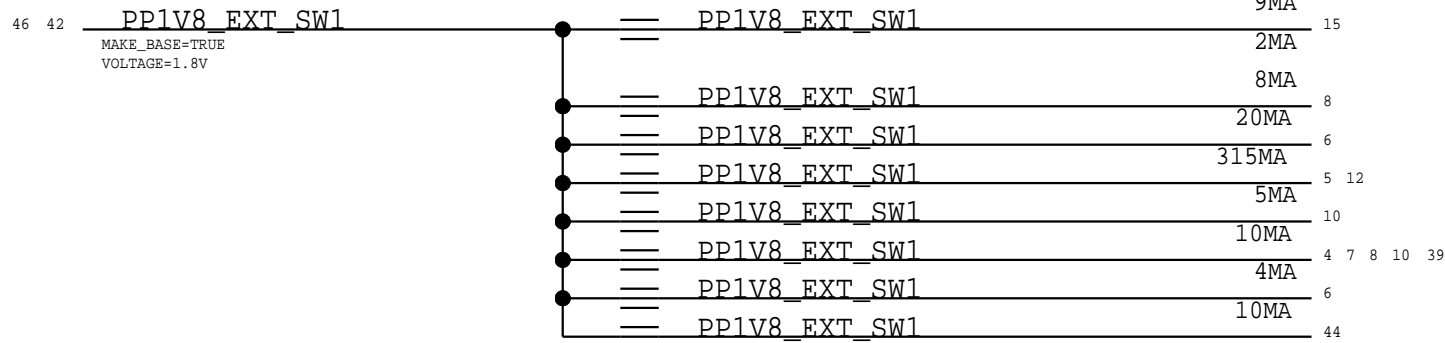


BUCK3\_SW

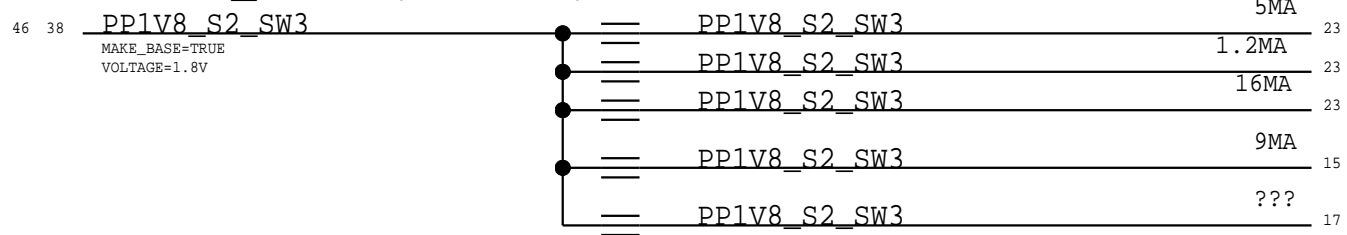
BUCK3\_SW1 (ACTIVE)



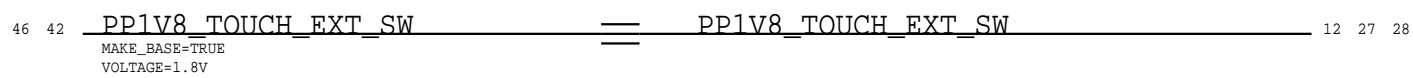
BUCK3\_EXT\_SW1 (ACTIVE)



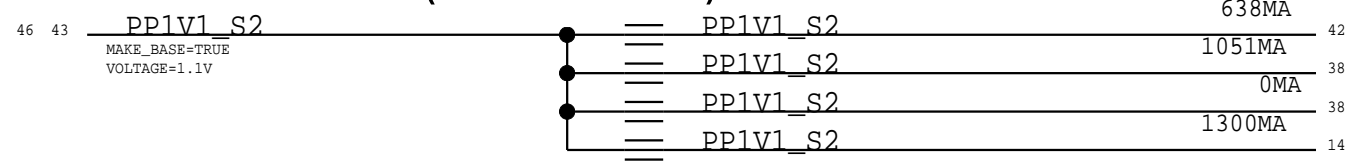
BUCK3\_SW3 (SLEEP2)



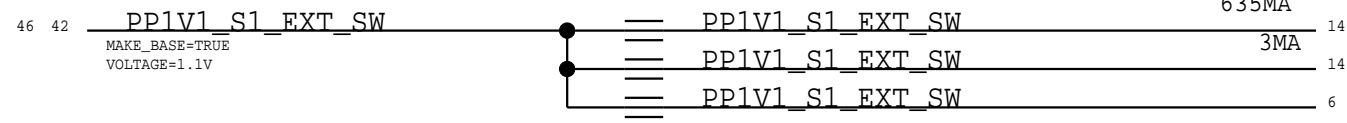
BUCK3\_EXT\_SW TOUCH



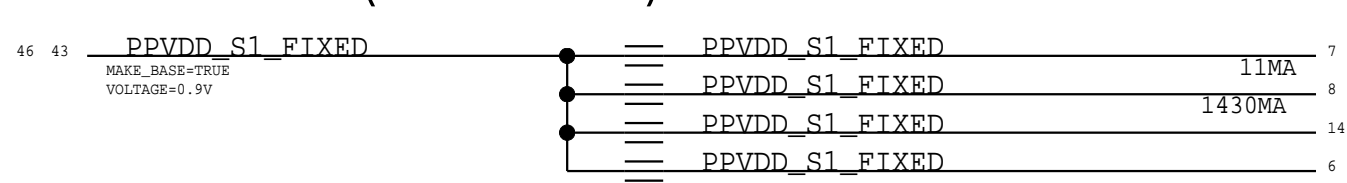
BUCK4 (SLEEP2)



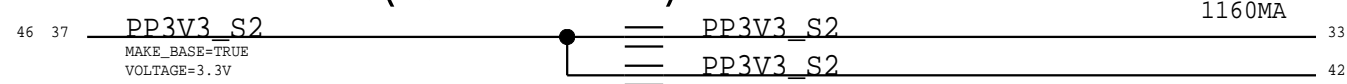
BUCK4\_EXT\_SW (SLEEP1)



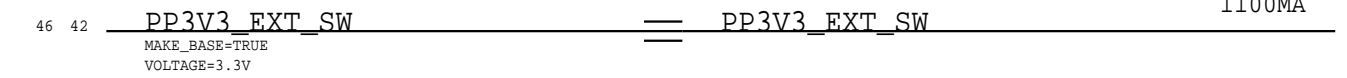
BUCK5 (SLEEP1)



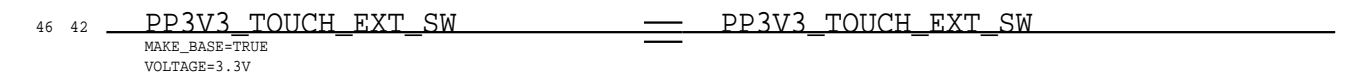
BUCK6 (SLEEP2)



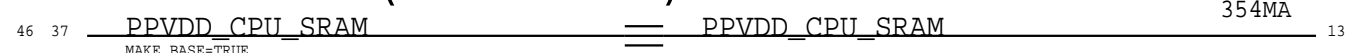
EXT SW (ACTIVE)



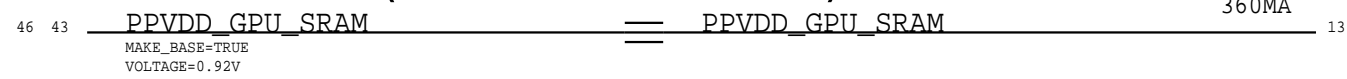
TOUCH EXT SW (SW CONTROL)



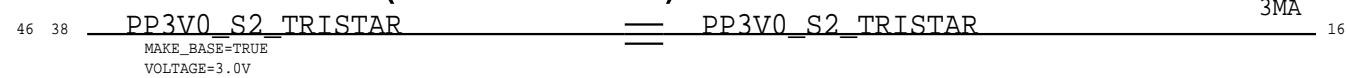
BUCK7 (ACTIVE)



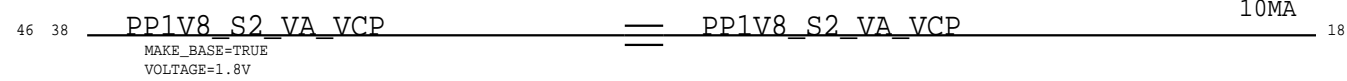
BUCK8 (SW CONTROL)



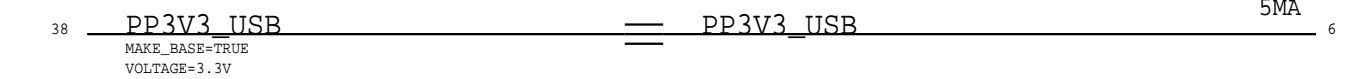
LDO1 (SLEEP2)



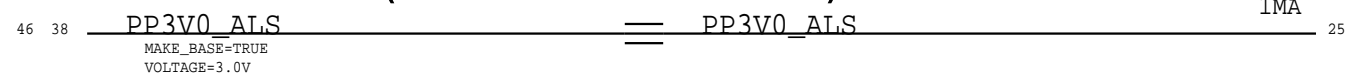
LDO2



LDO3

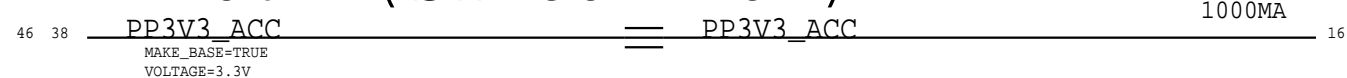


LDO4 (SW CONTROL)

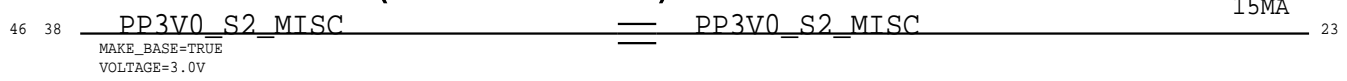


LDO5 (SPARE)

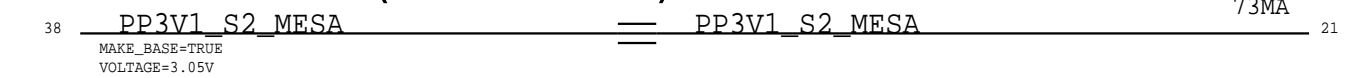
LDO6 (SW CONTROL)



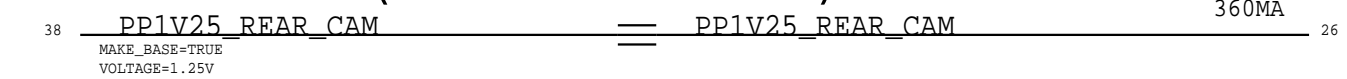
LDO7 (SLEEP2)



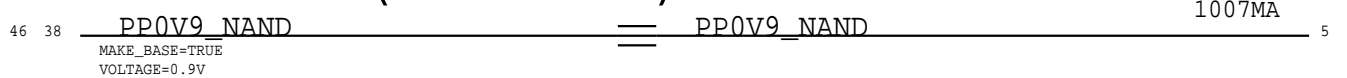
LDO8 (SLEEP2)



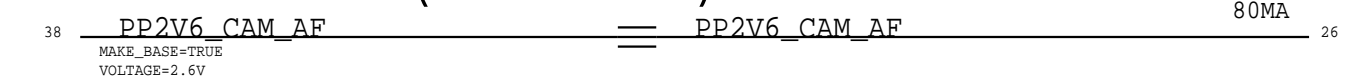
LDO9 (SW CONTROL)



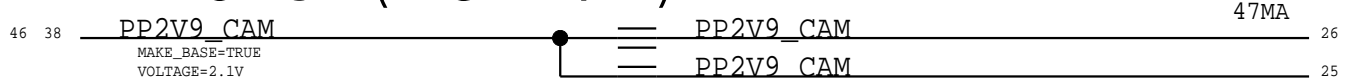
LDO10 (ACTIVE)



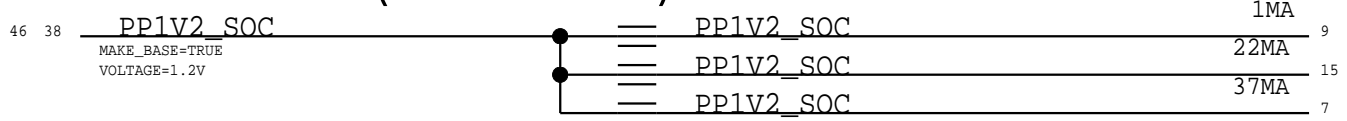
LDO11 (ACTIVE)



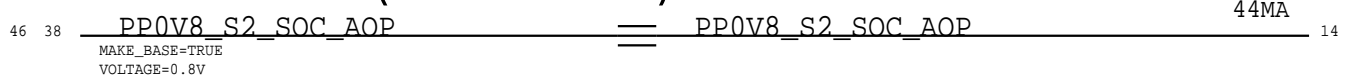
LDO13 (ACTIVE)



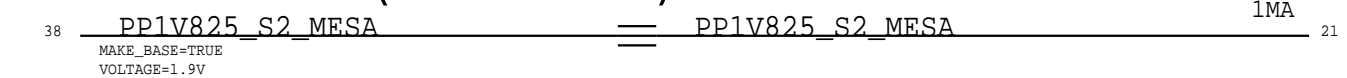
LDO14 (ACTIVE)



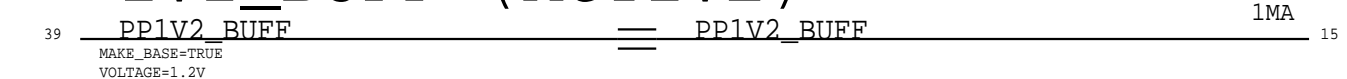
LDO15 (SLEEP2)



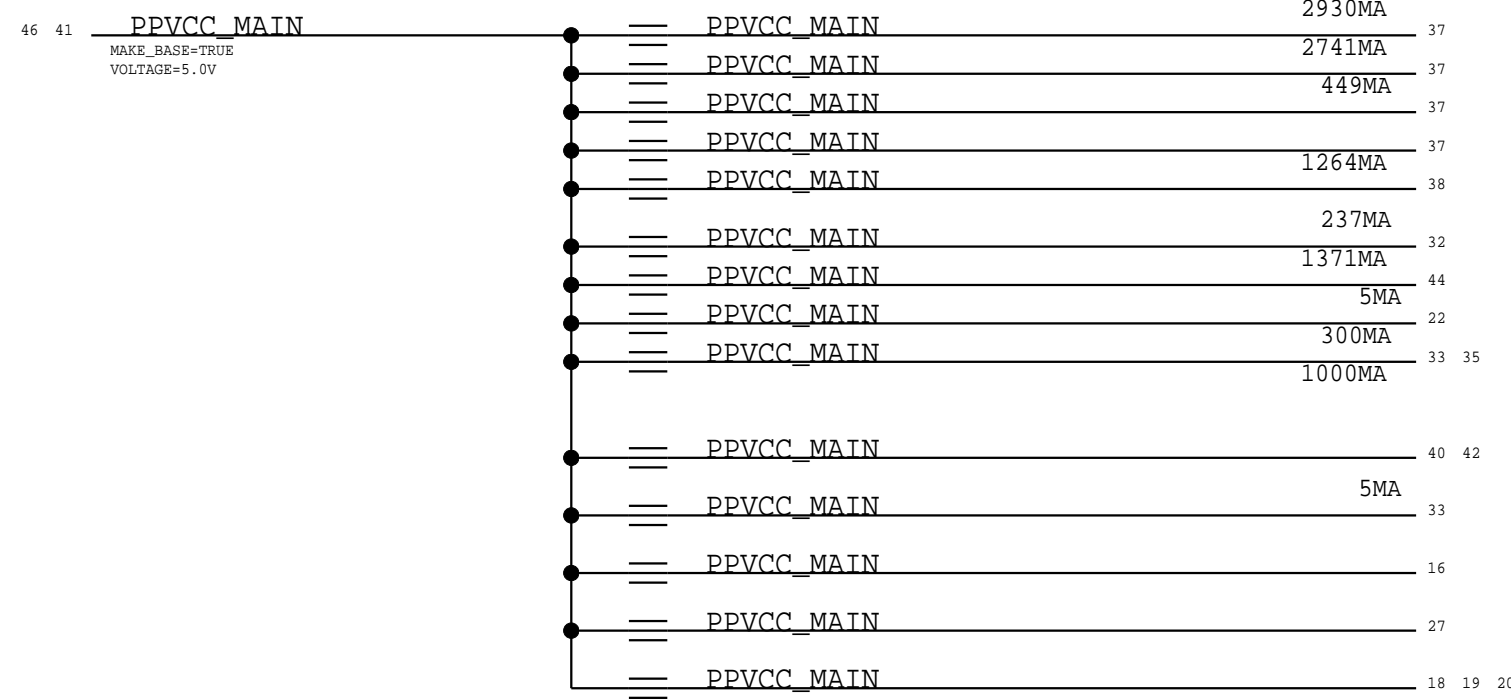
LDO16 (SLEEP2)



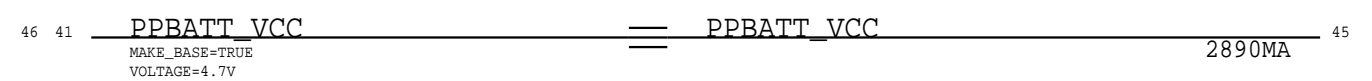
1V2\_BUFF (ACTIVE)



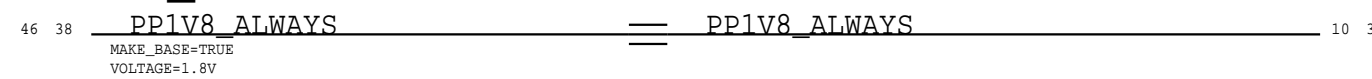
CHARGER MAIN



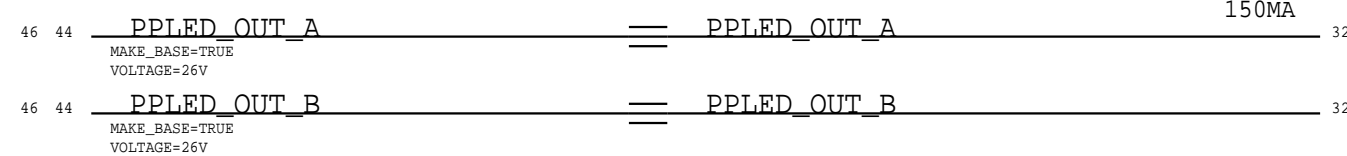
BATTERY



ON\_BUF



BACKLIGHT BOOST



SYNC\_MASTER=771S\_MLB\_B SYNC\_DATE=01/27/2017

POWER: ALIASES