

PG132-A02

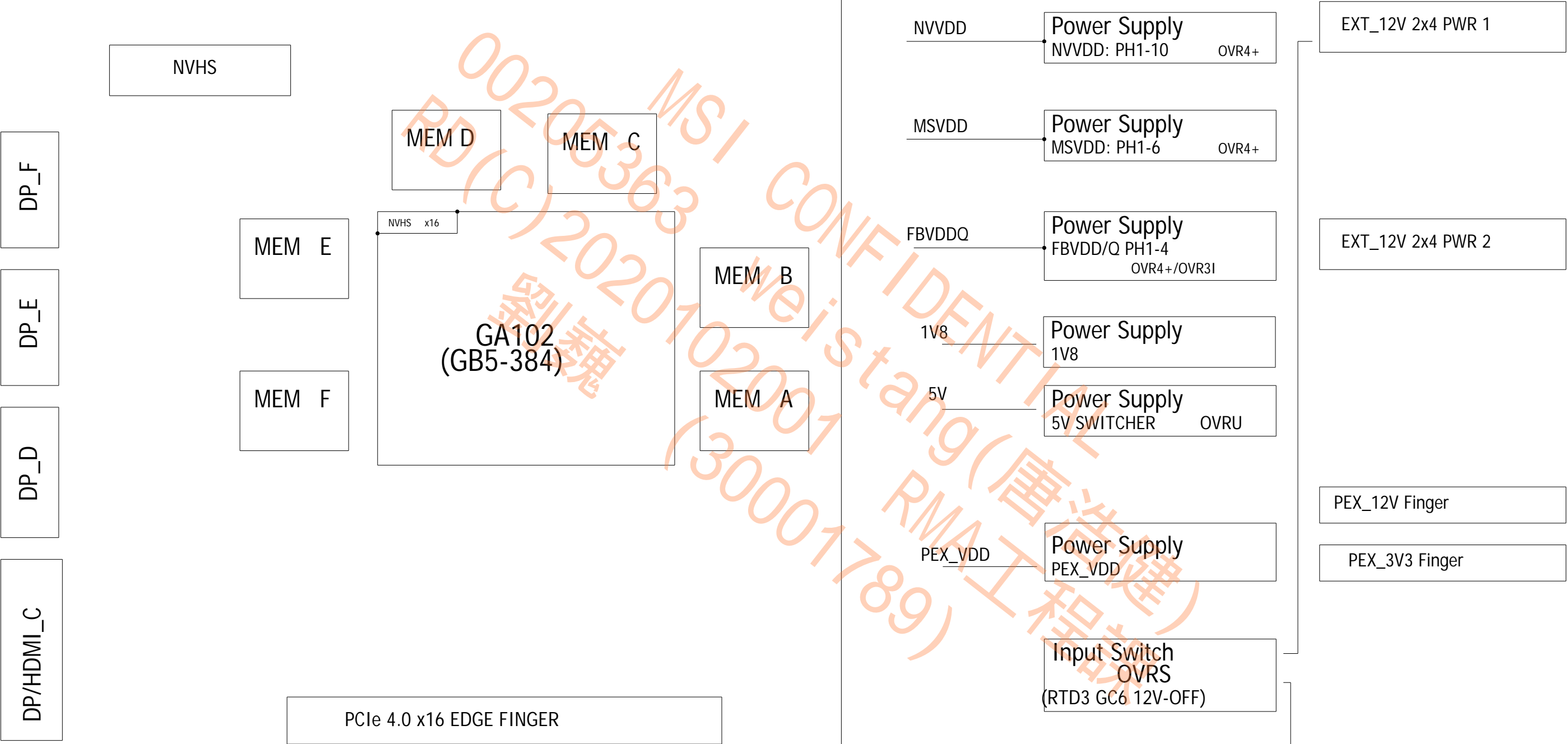
320W, FH Std PCB, 320b, GDDR6X 2CH x16
DP + DP + DP + HDMI

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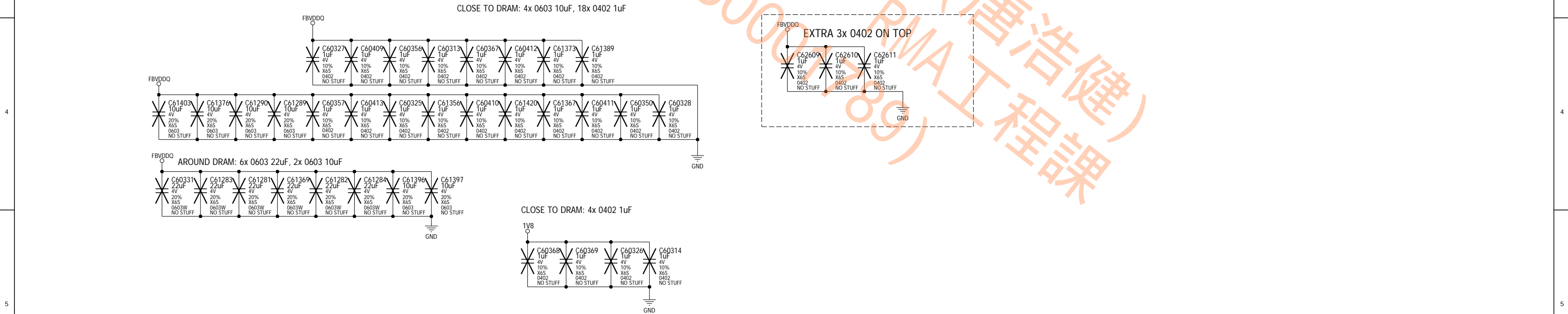
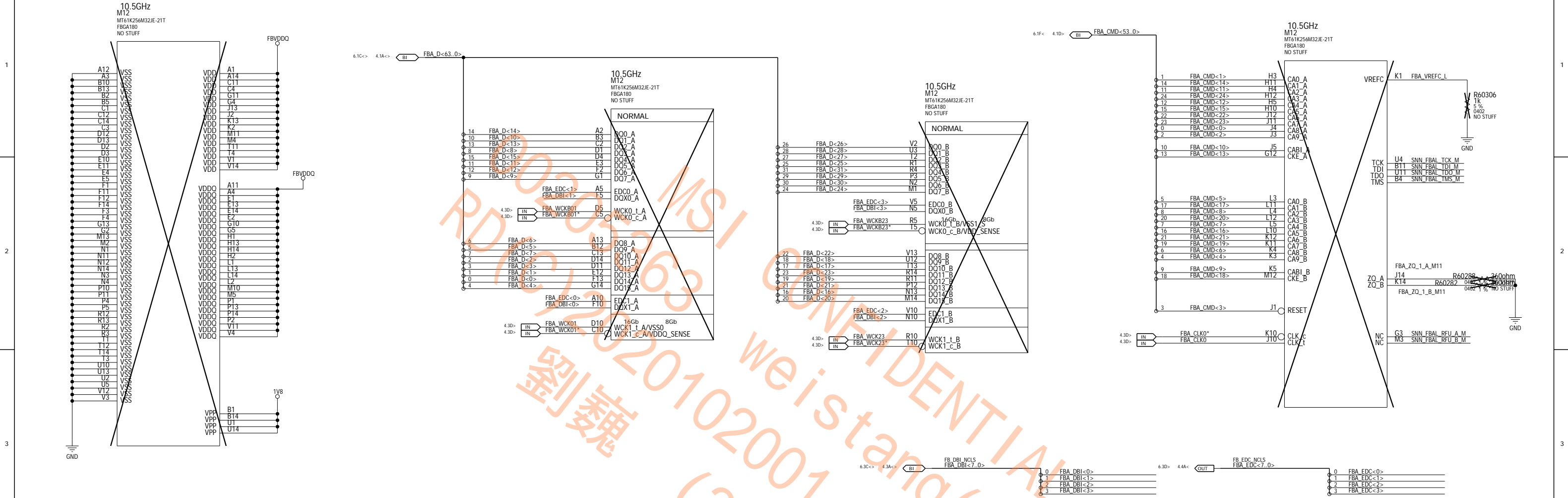
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Block Diagram

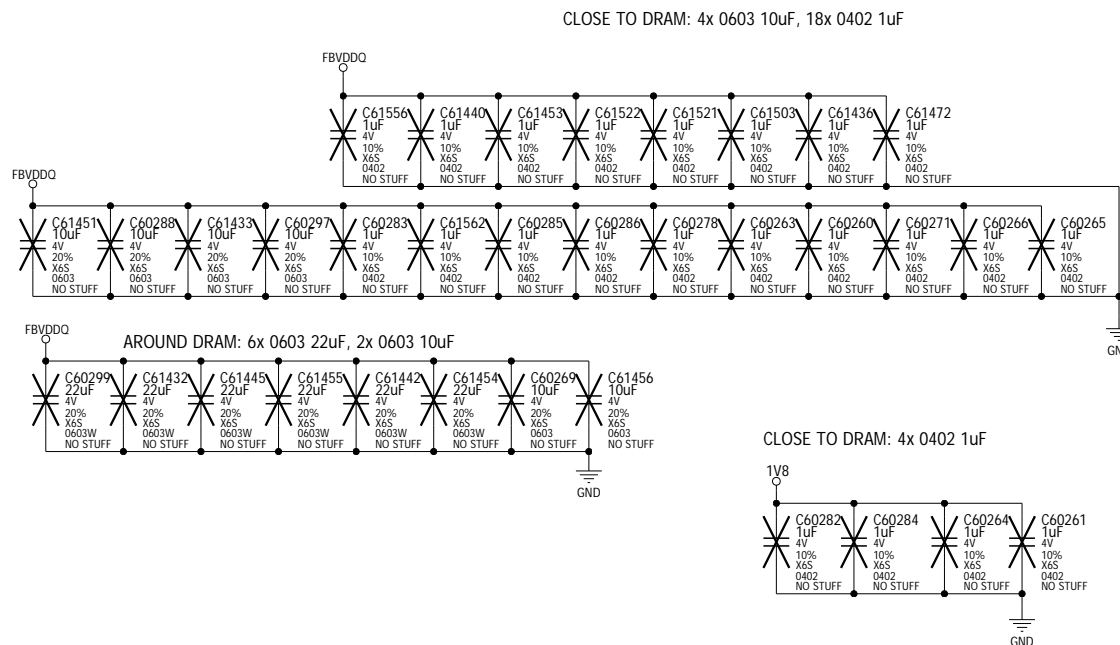
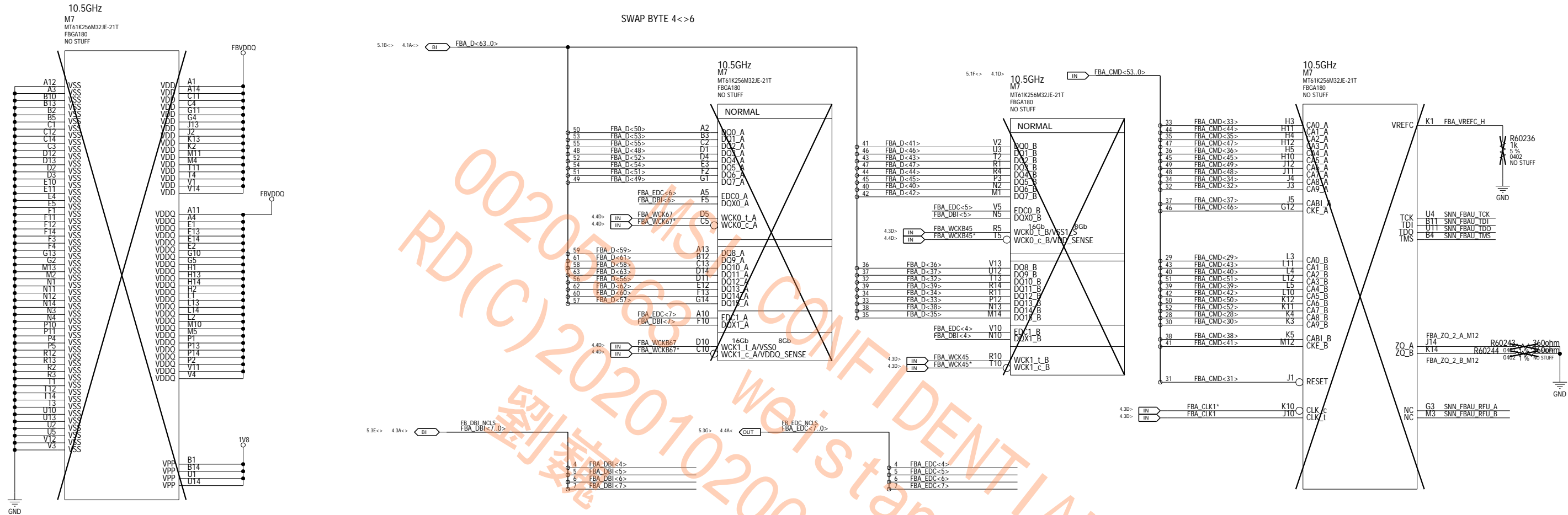


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MEMORY: FBA Partition 31..0



MEMORY: FBA Partition 63..32



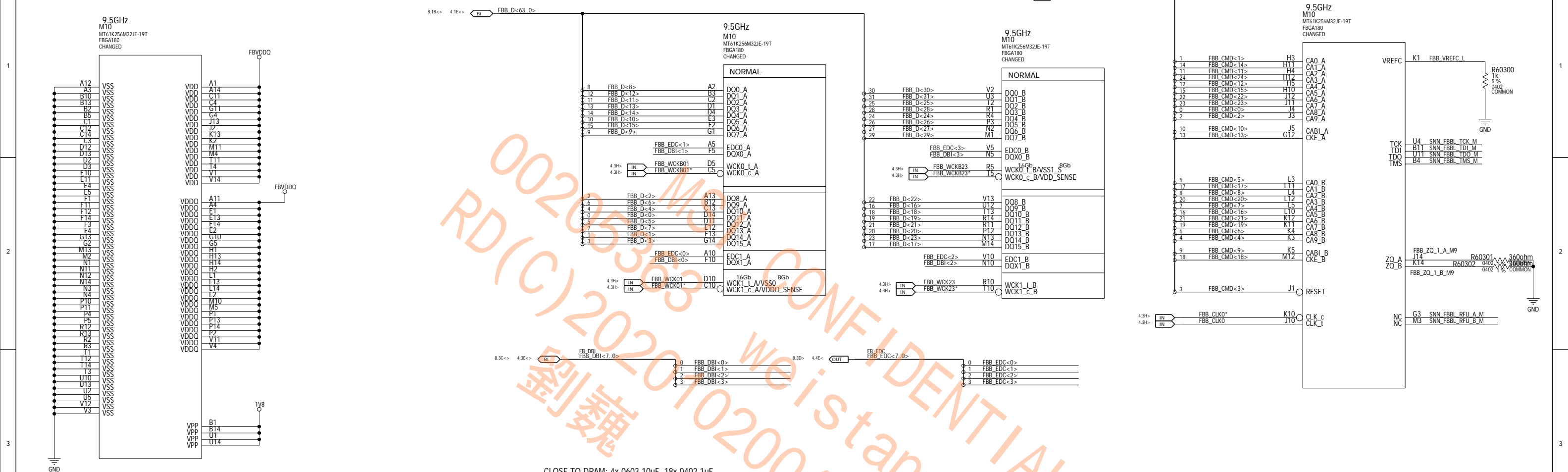
EXTRA 1x 0402 ON BOT



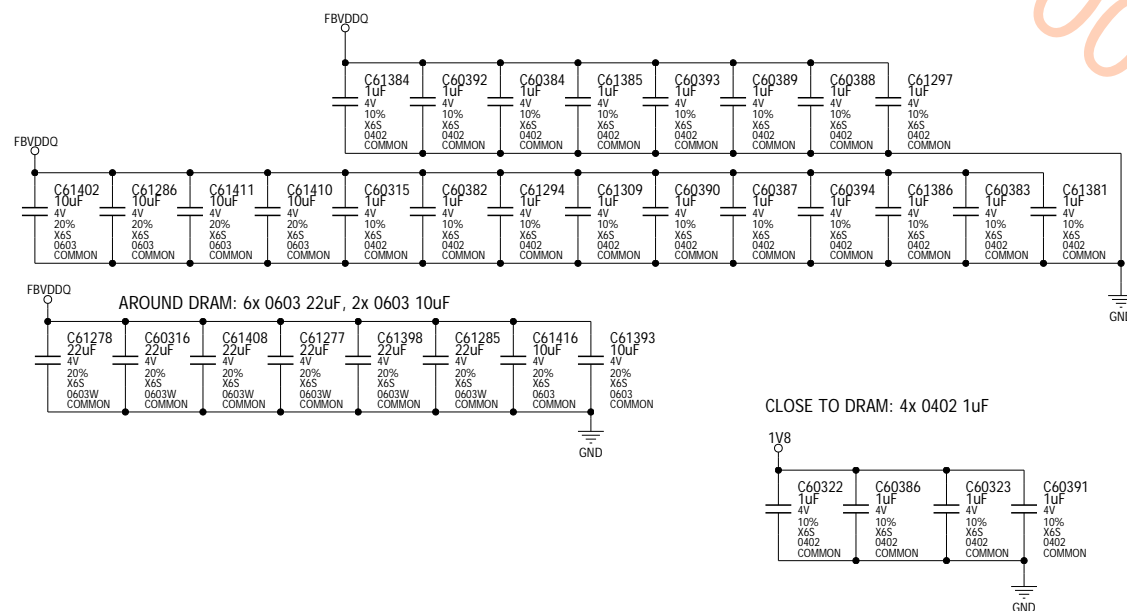
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MEMORY: FBB Partition 31..0



CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



CLOSE TO DRAM: 4x 0402 1uF

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PAGE DETAIL	MEMORY: FBB PARTITION[31:0]

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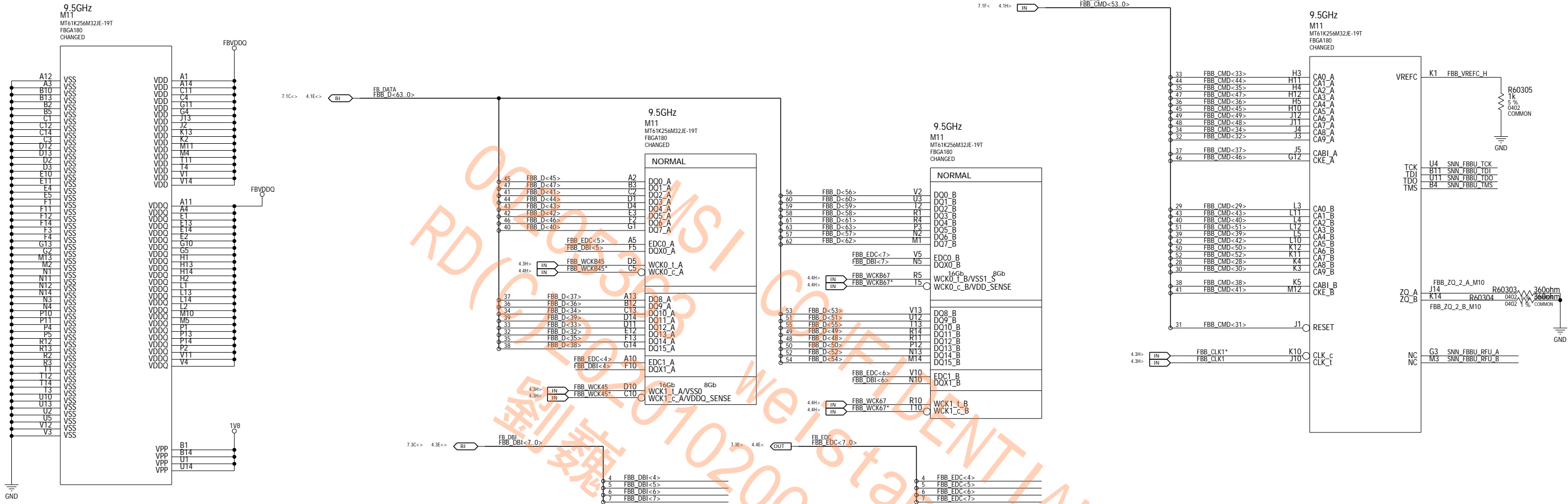
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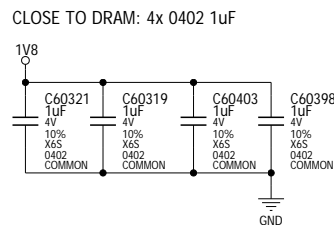
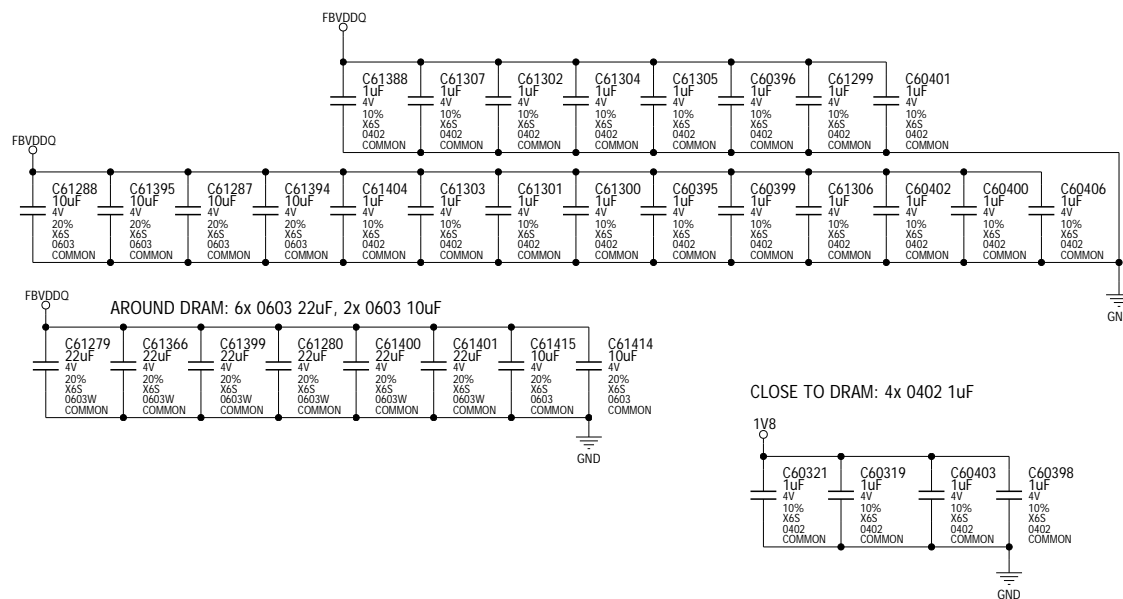
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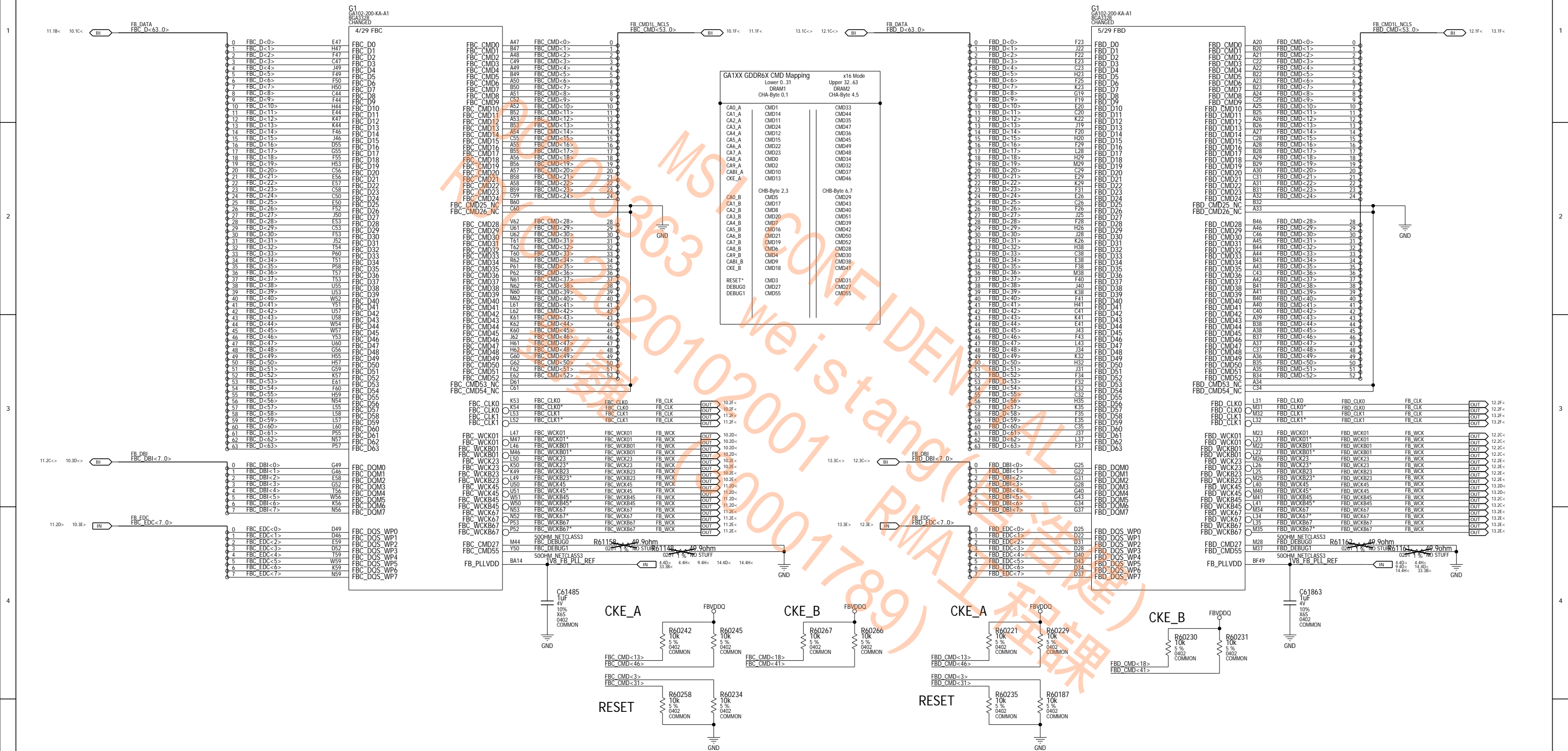
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CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



MEMORY: GPU Partition C/D



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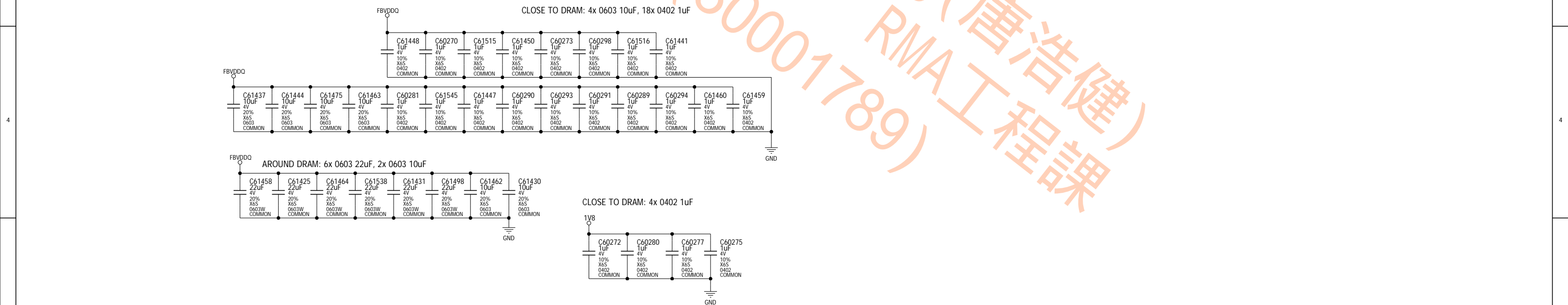
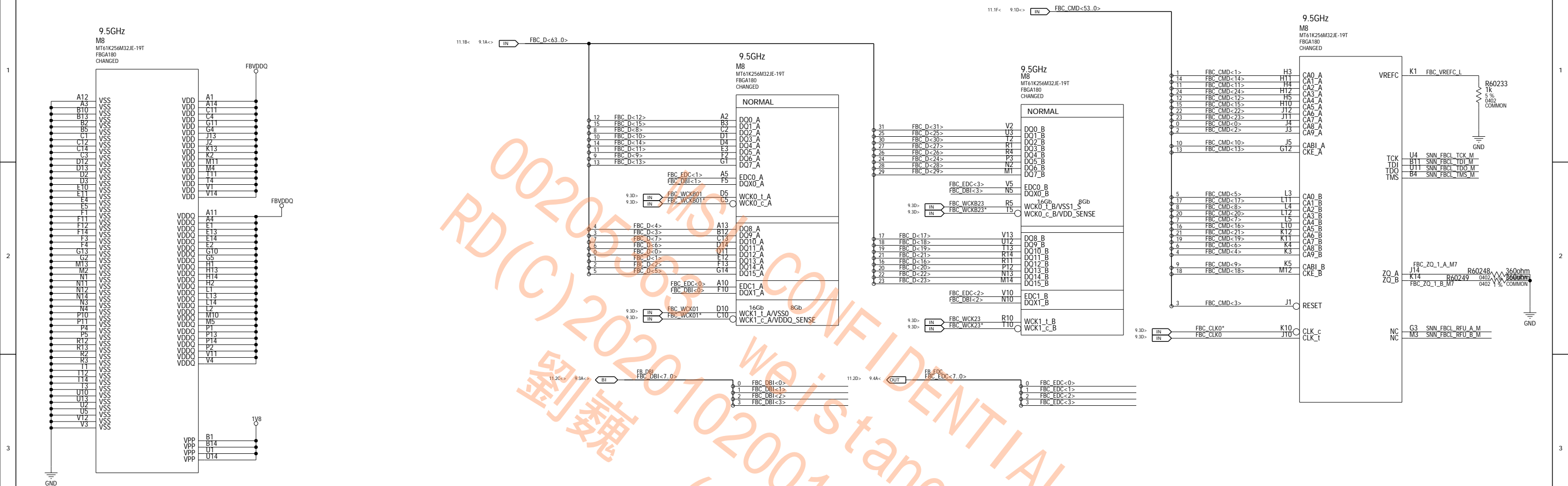
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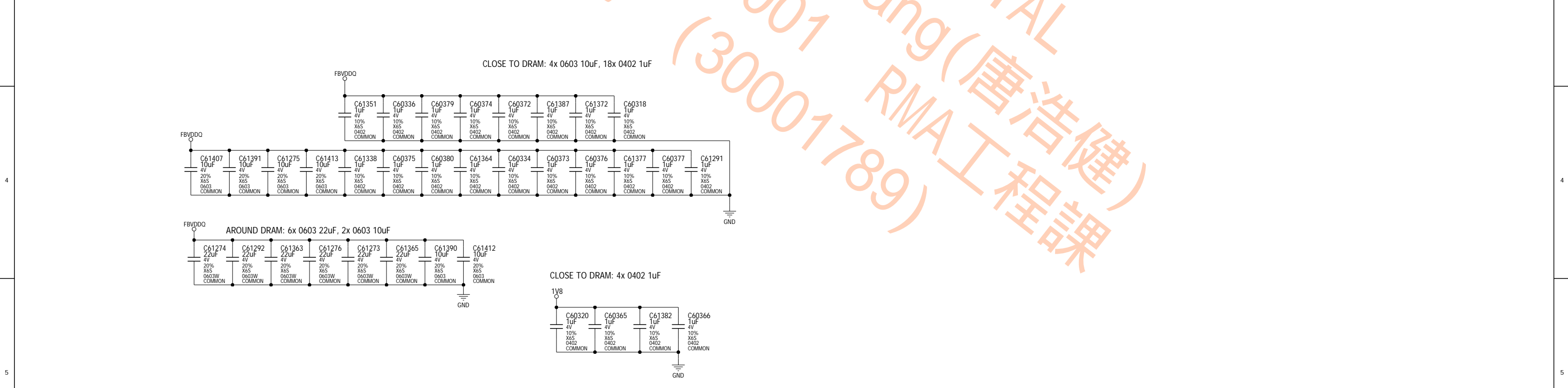
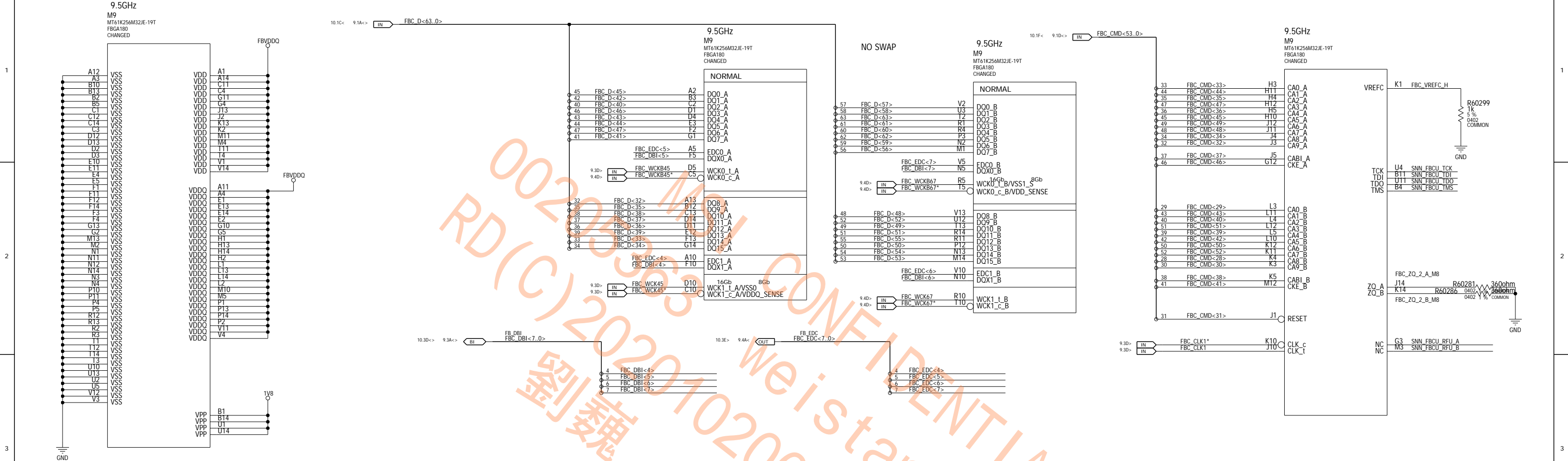
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PAGE DETAIL	MEMORY: GPU PARTITION C/D

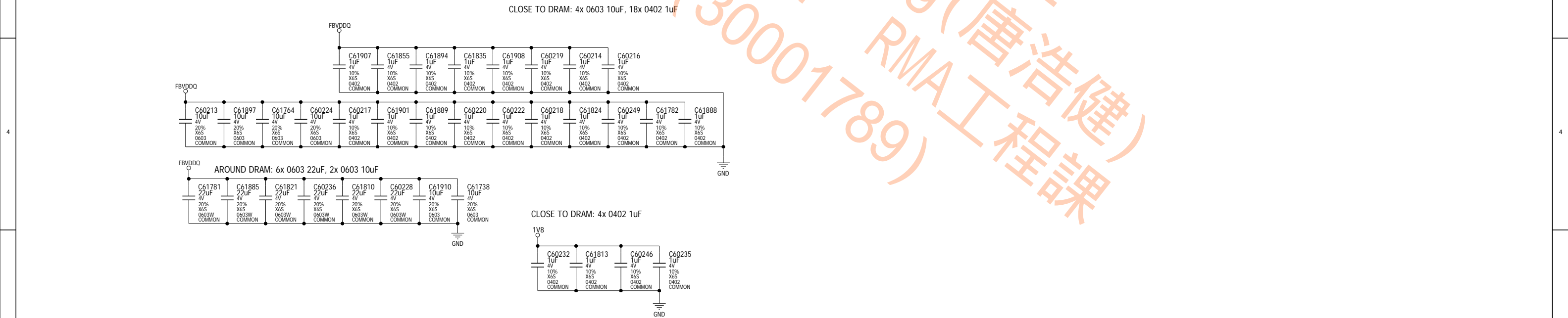
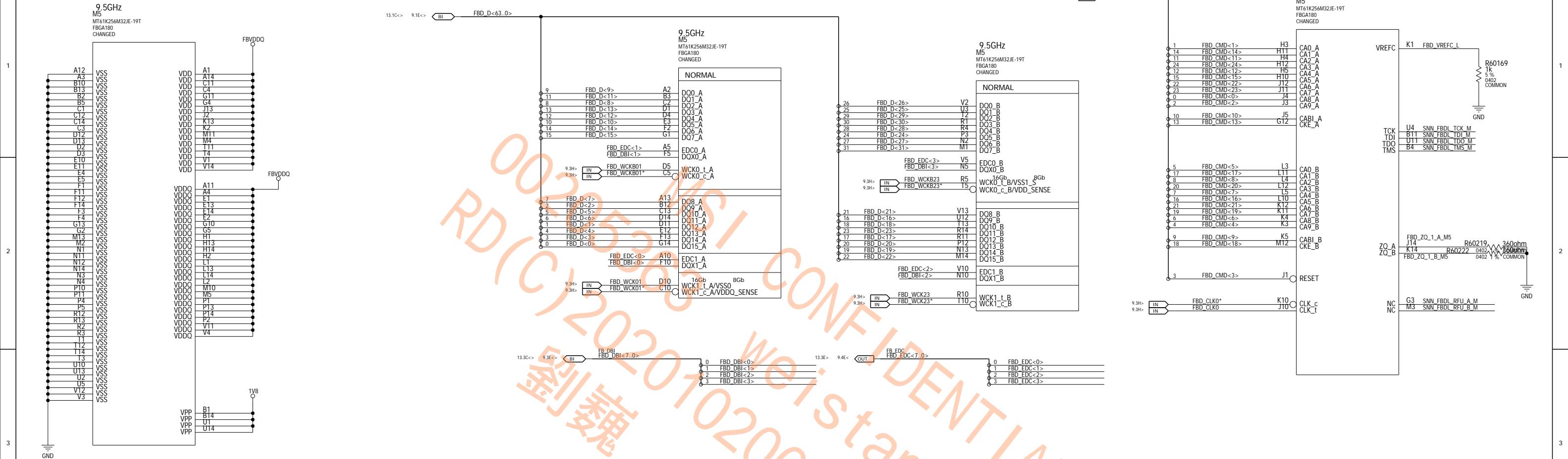
MEMORY: FBC Partition 31..0



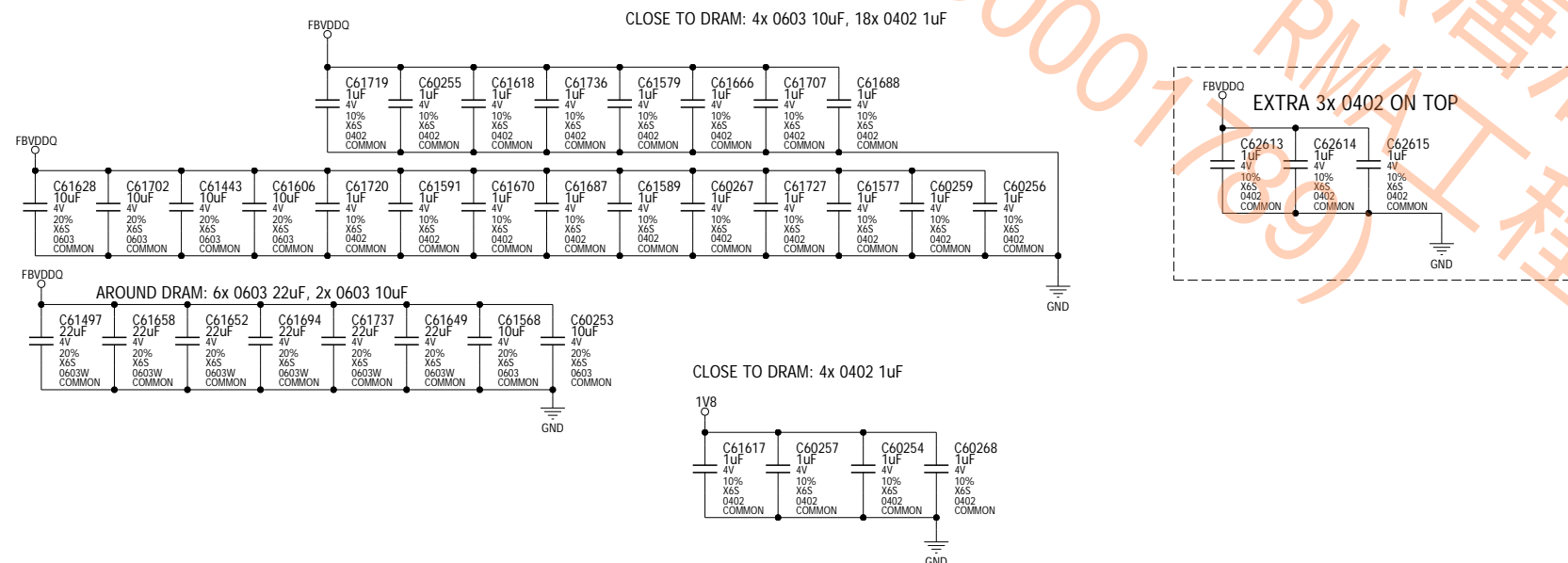
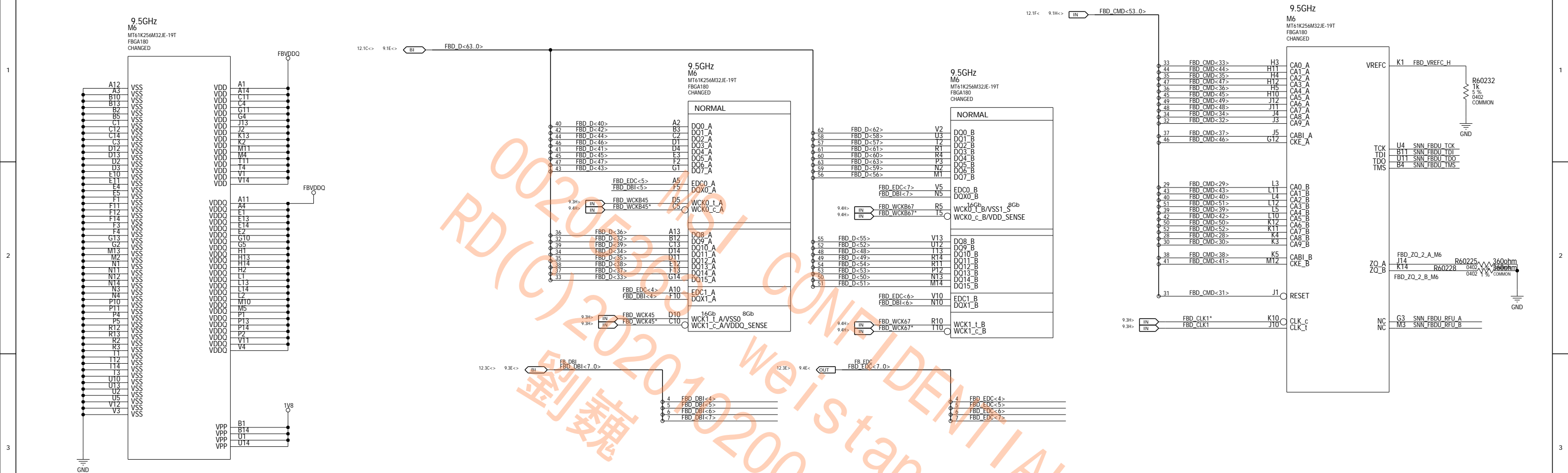
MEMORY: FBC Partition 63..32




MEMORY: FBD Partition 31..0



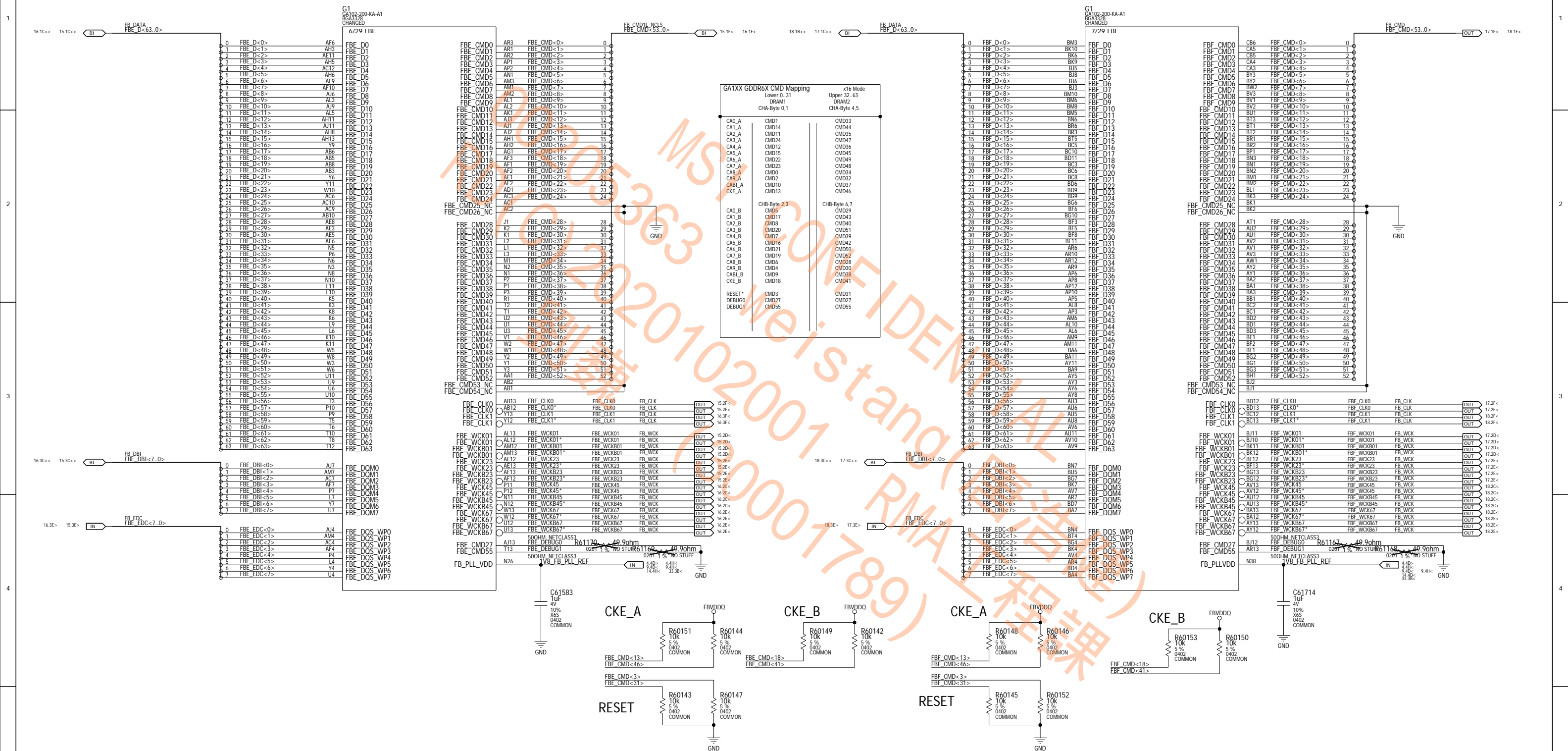
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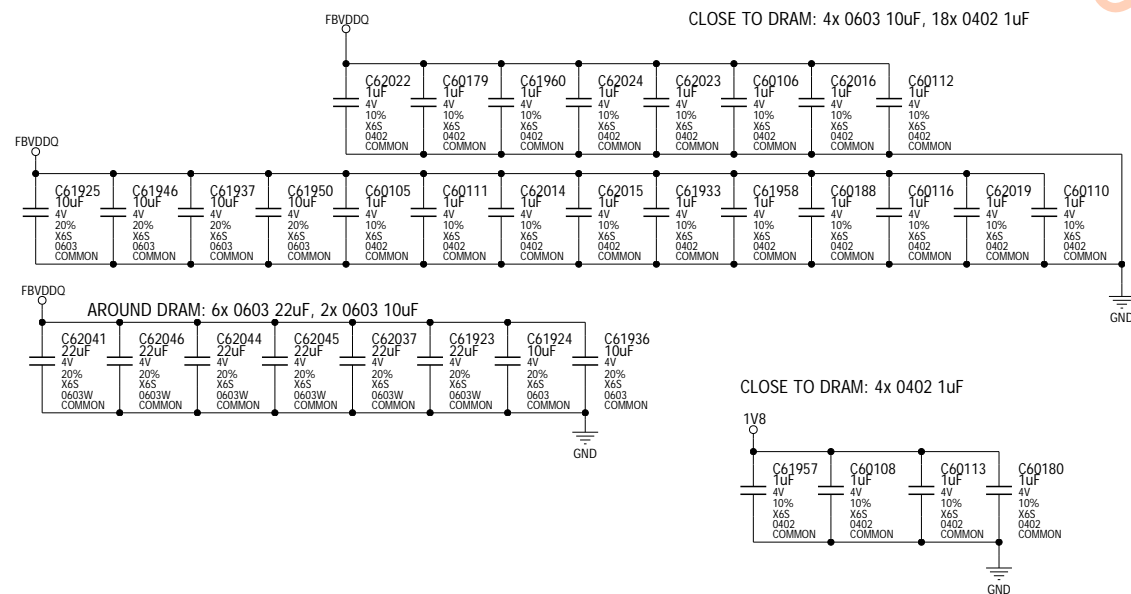
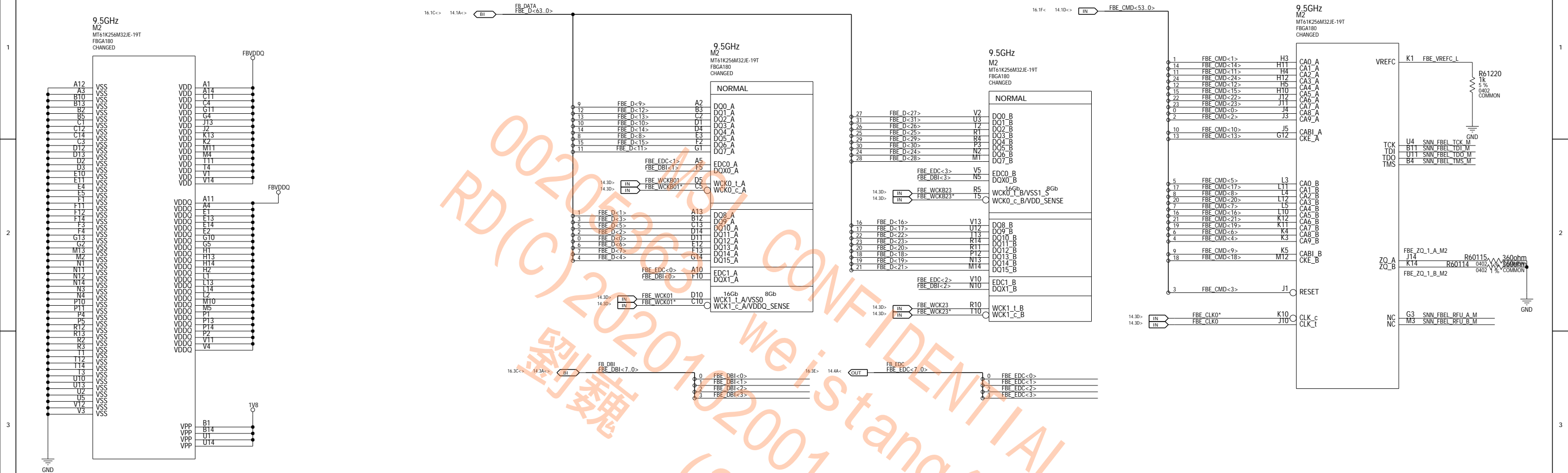
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MEMORY: GPU Partition E/F



MEMORY: FBE Partition 31..0



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PAGE DETAIL	MEMORY: FBE PARTITION[31:0]

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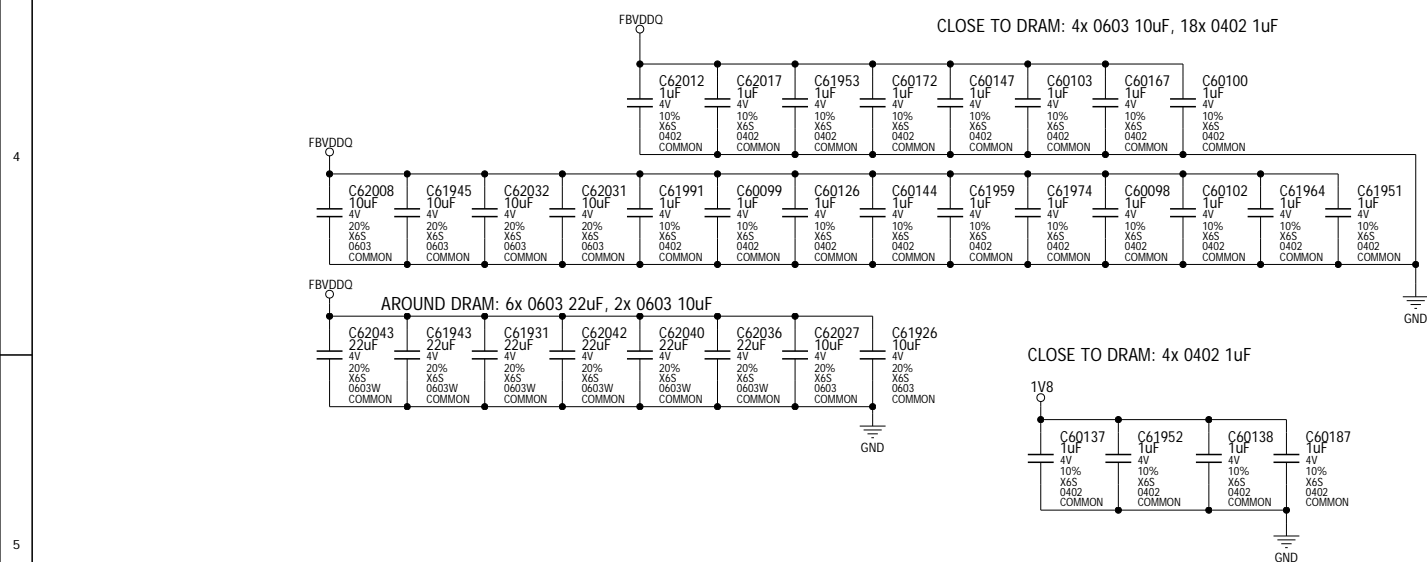
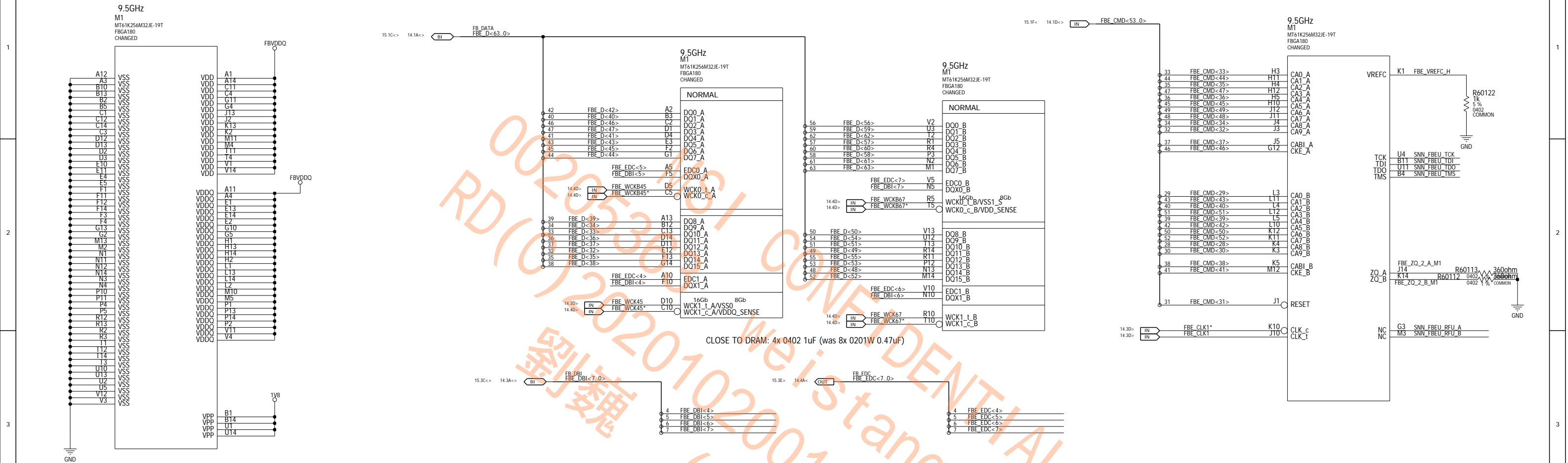
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NV_PN	600-1G132-0030-300
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MEMORY: FBE Partition 63..32



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: FBE PARTITION[63:32]

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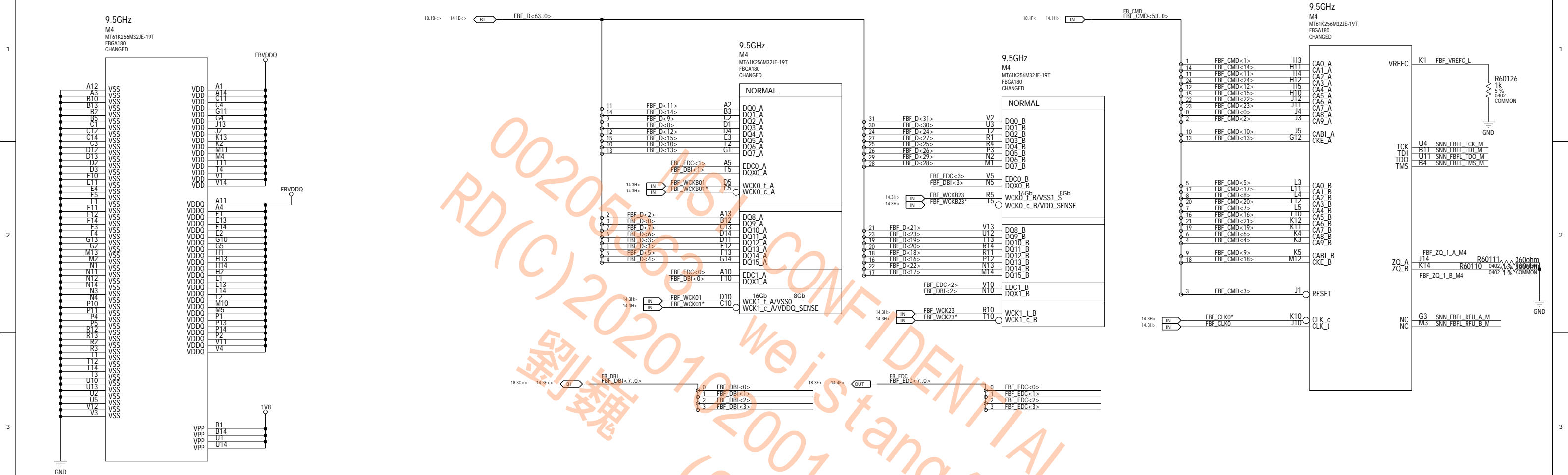
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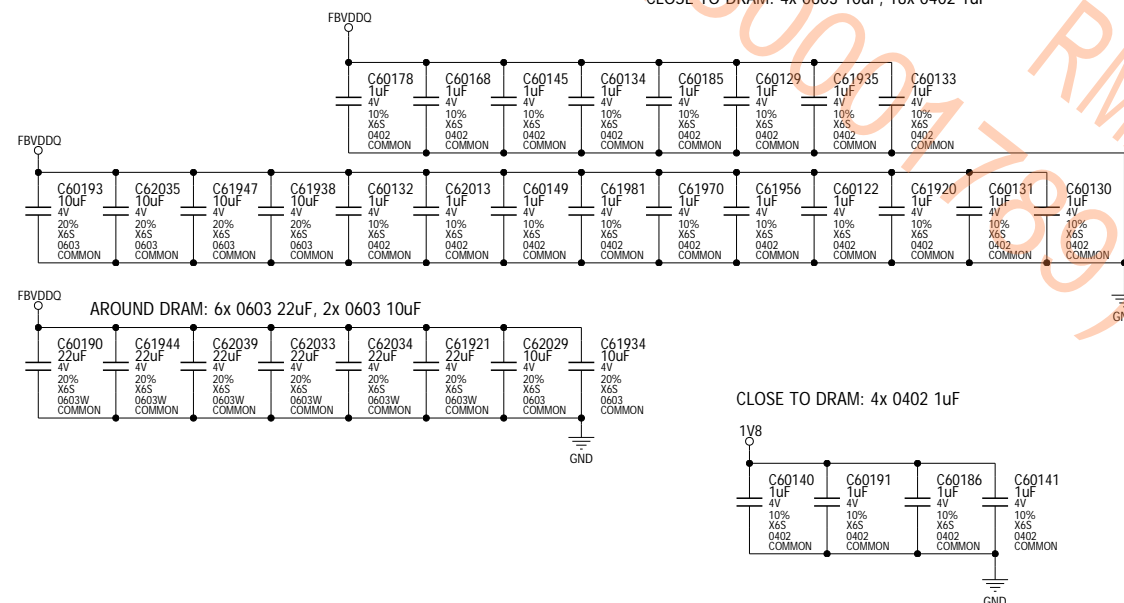
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MEMORY: FBF Partition 31..0



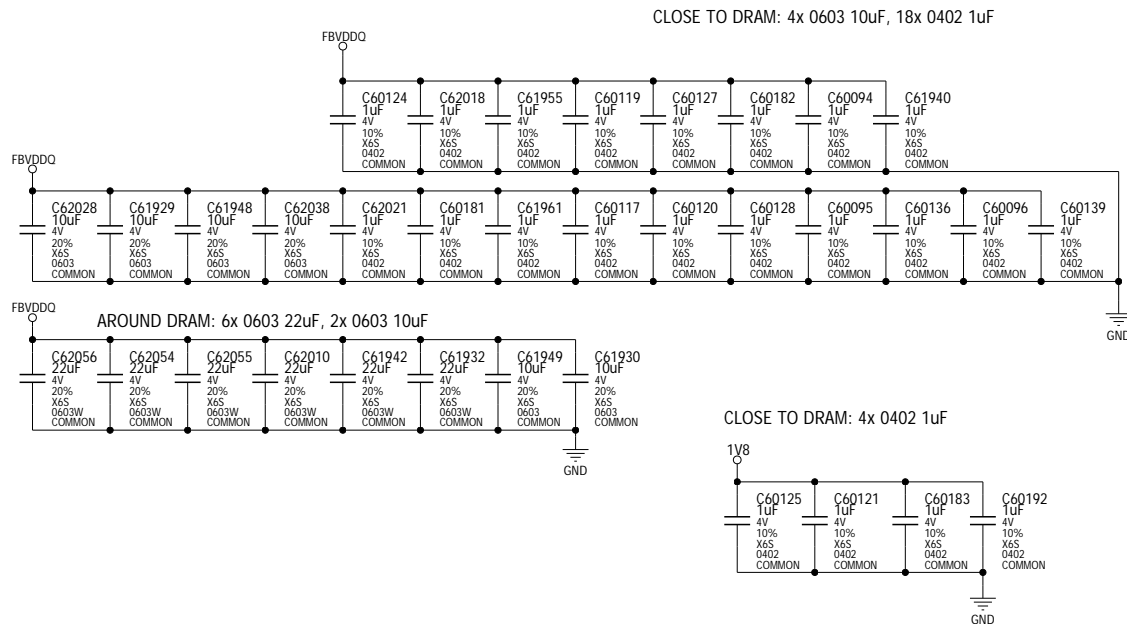
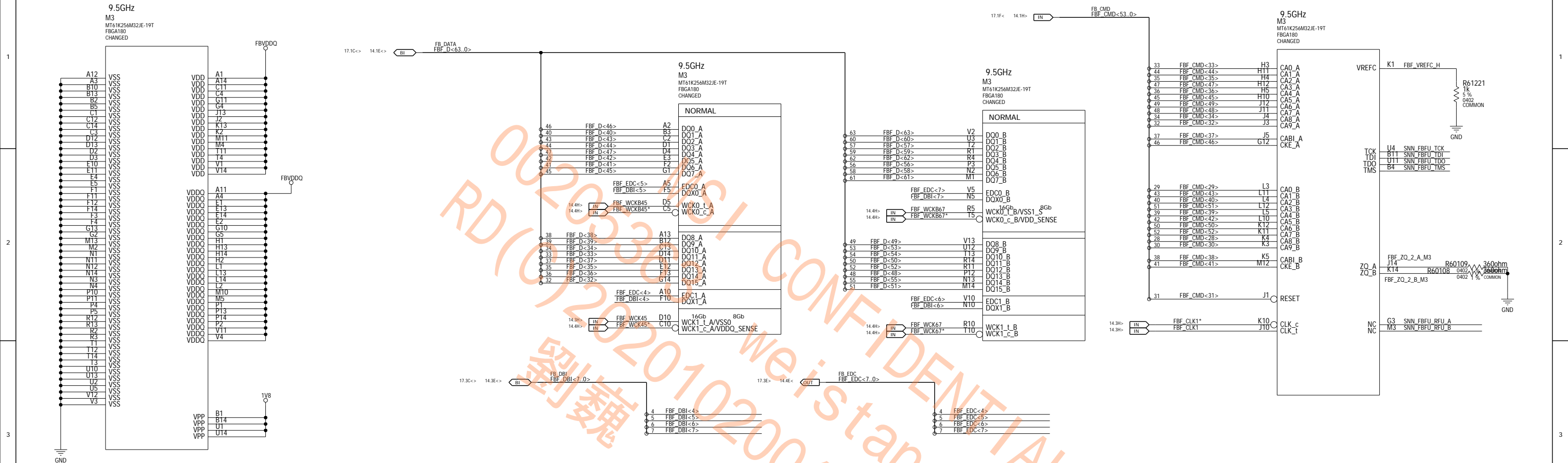
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



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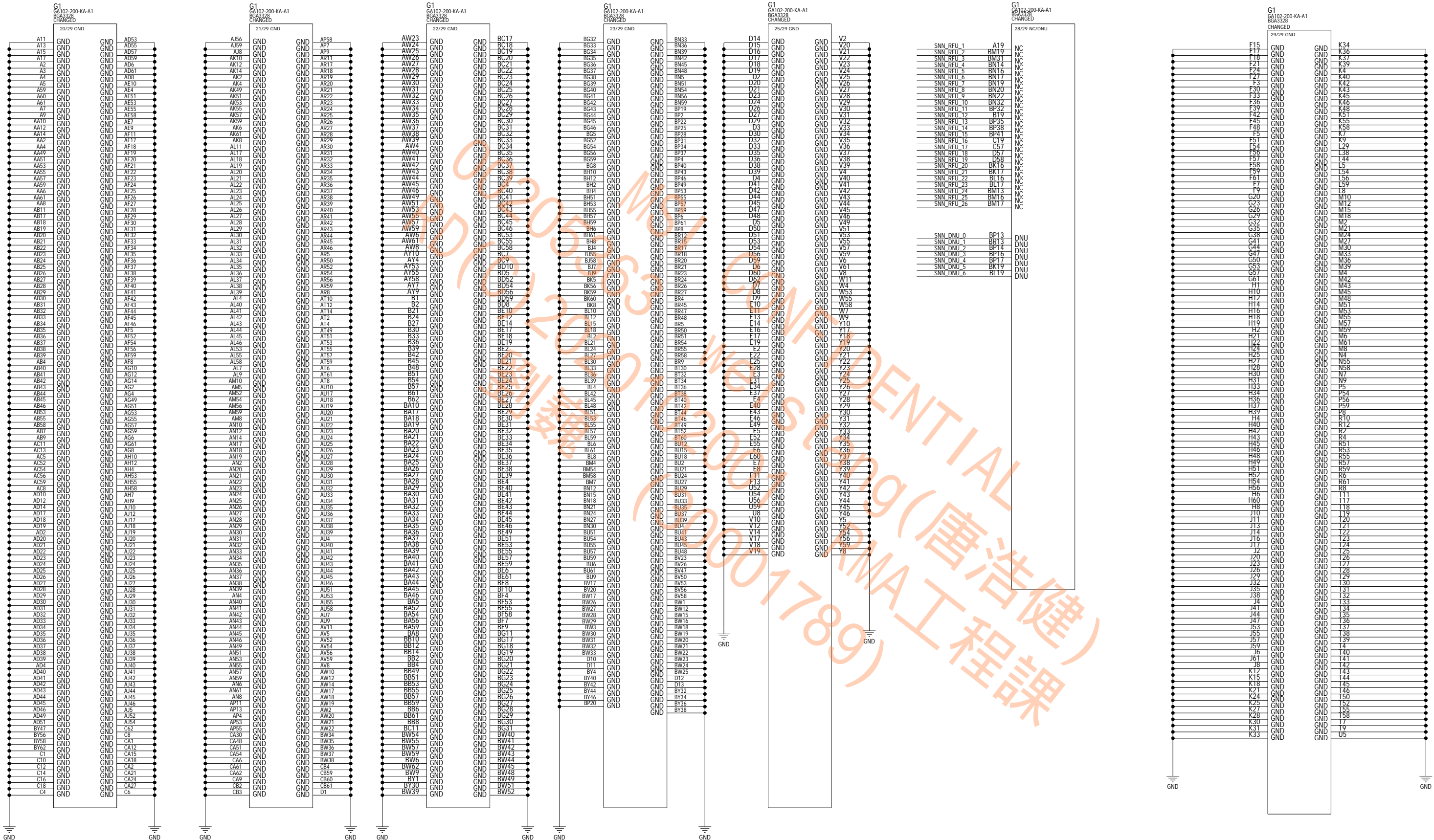
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MEMORY: FBF Partition 63..32



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GPU GND, RFUs & RSVD



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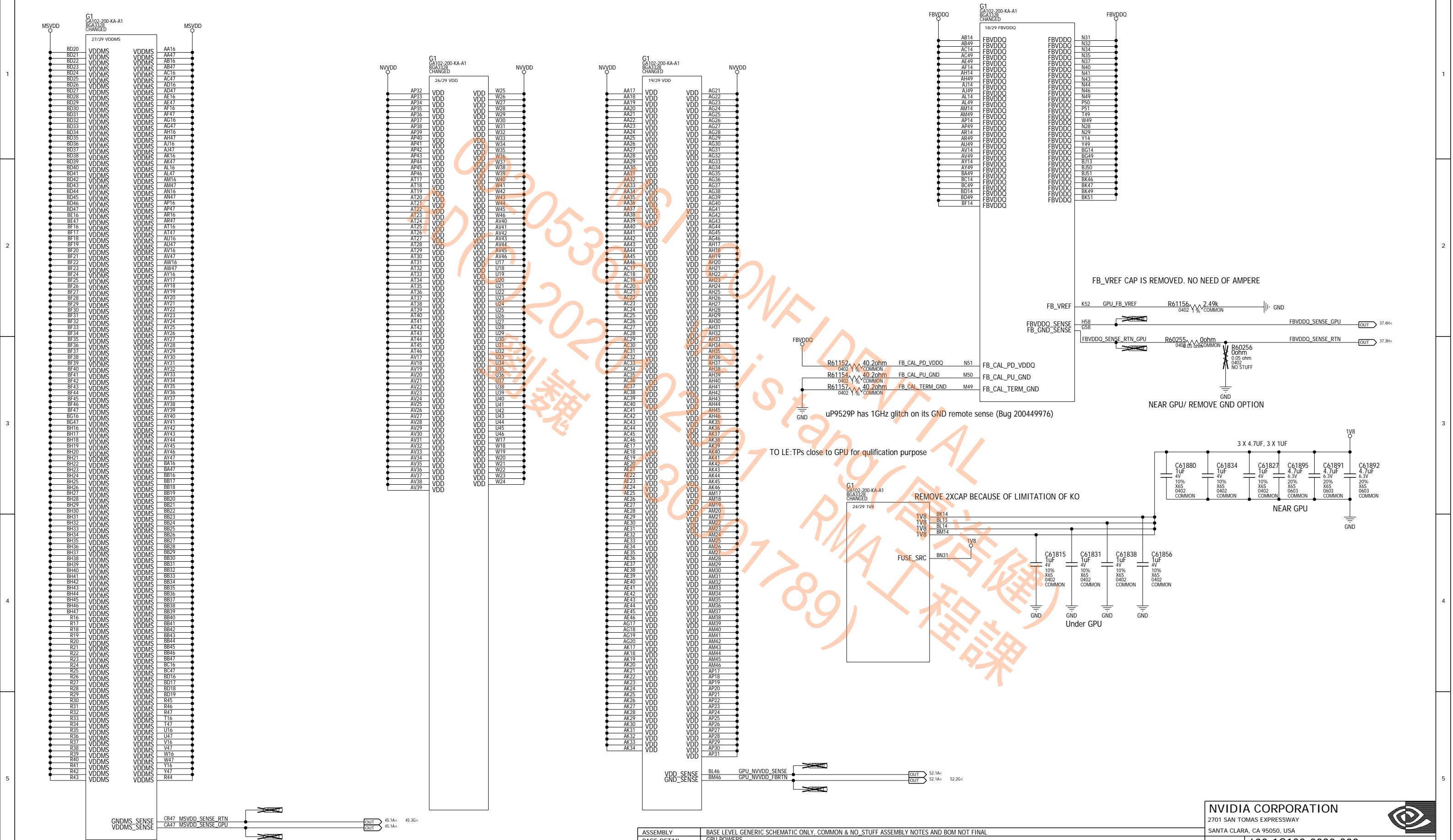
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PAGE DETAIL	GPU GND, RFUS & RSVD

GPU PWR and GND

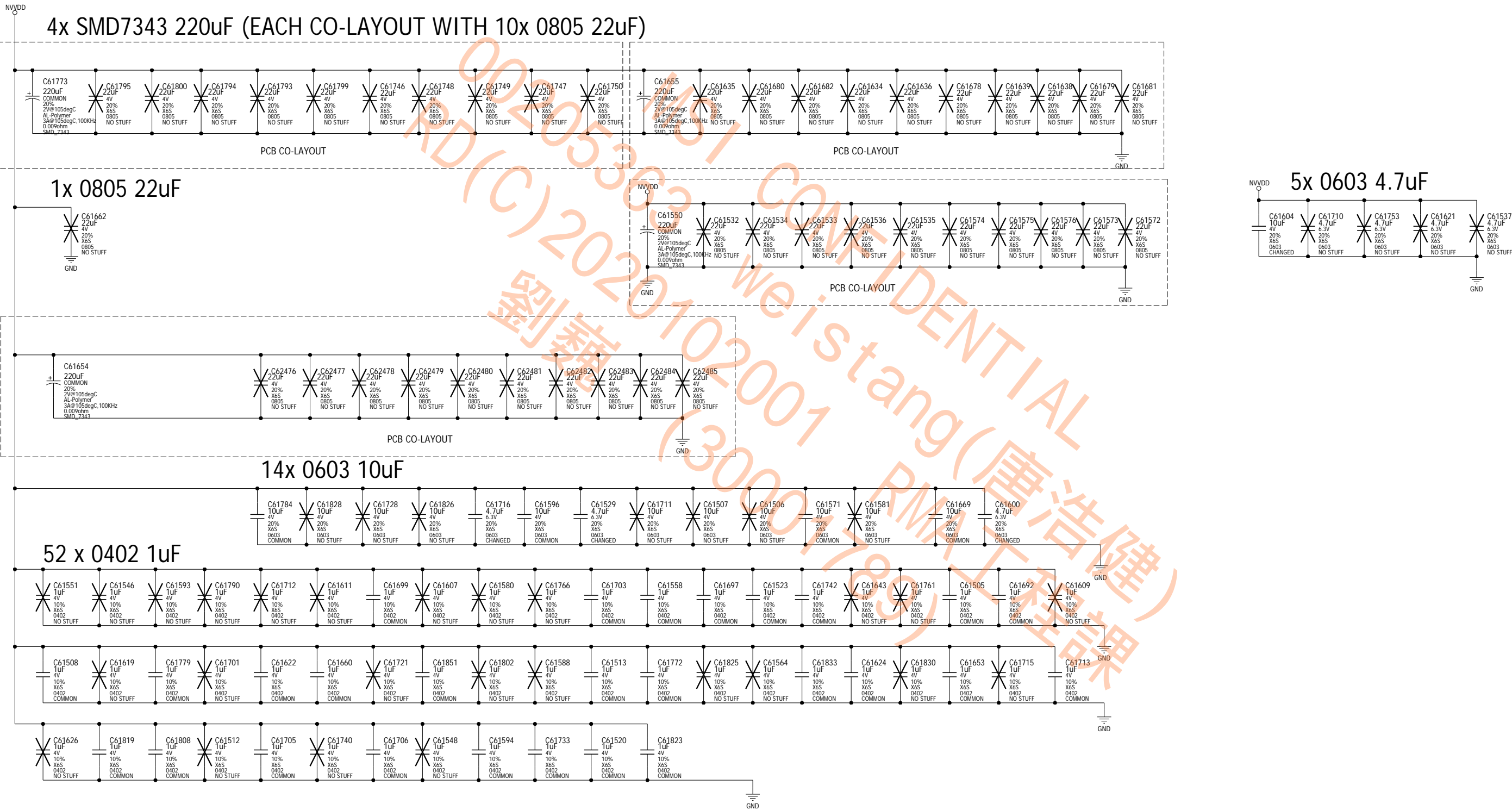


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	GPU POWERS

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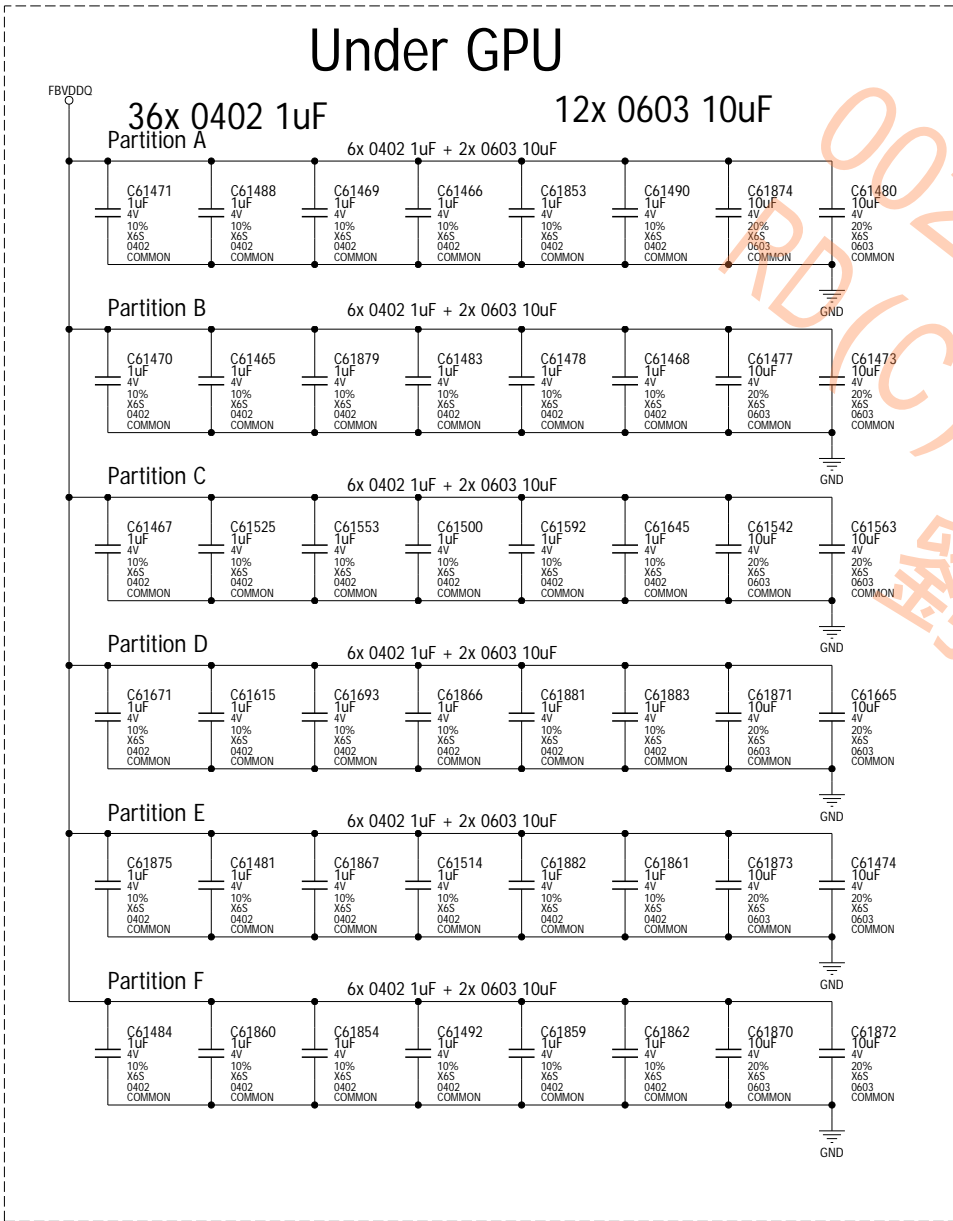
NVVDD UNDER GPU



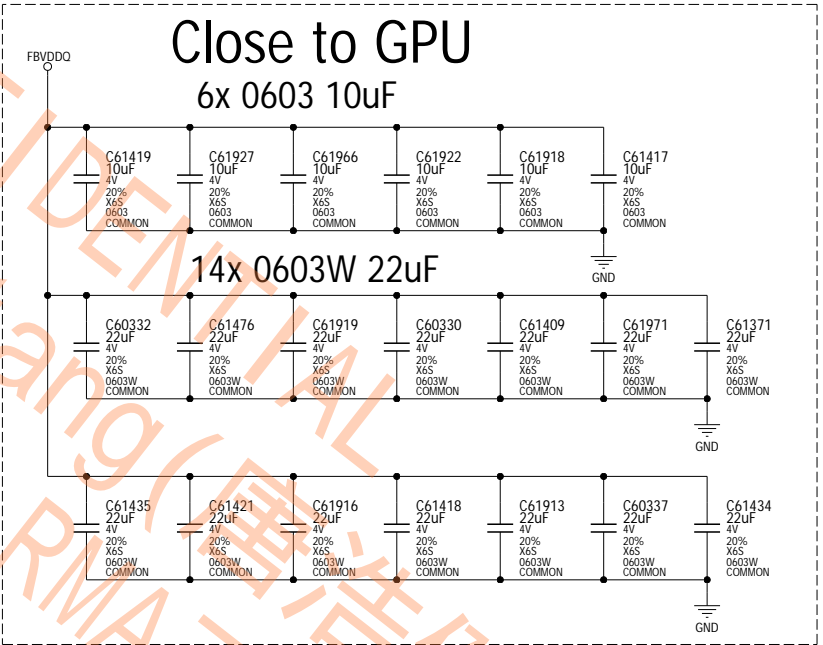
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FBVDDQ

Under GPU



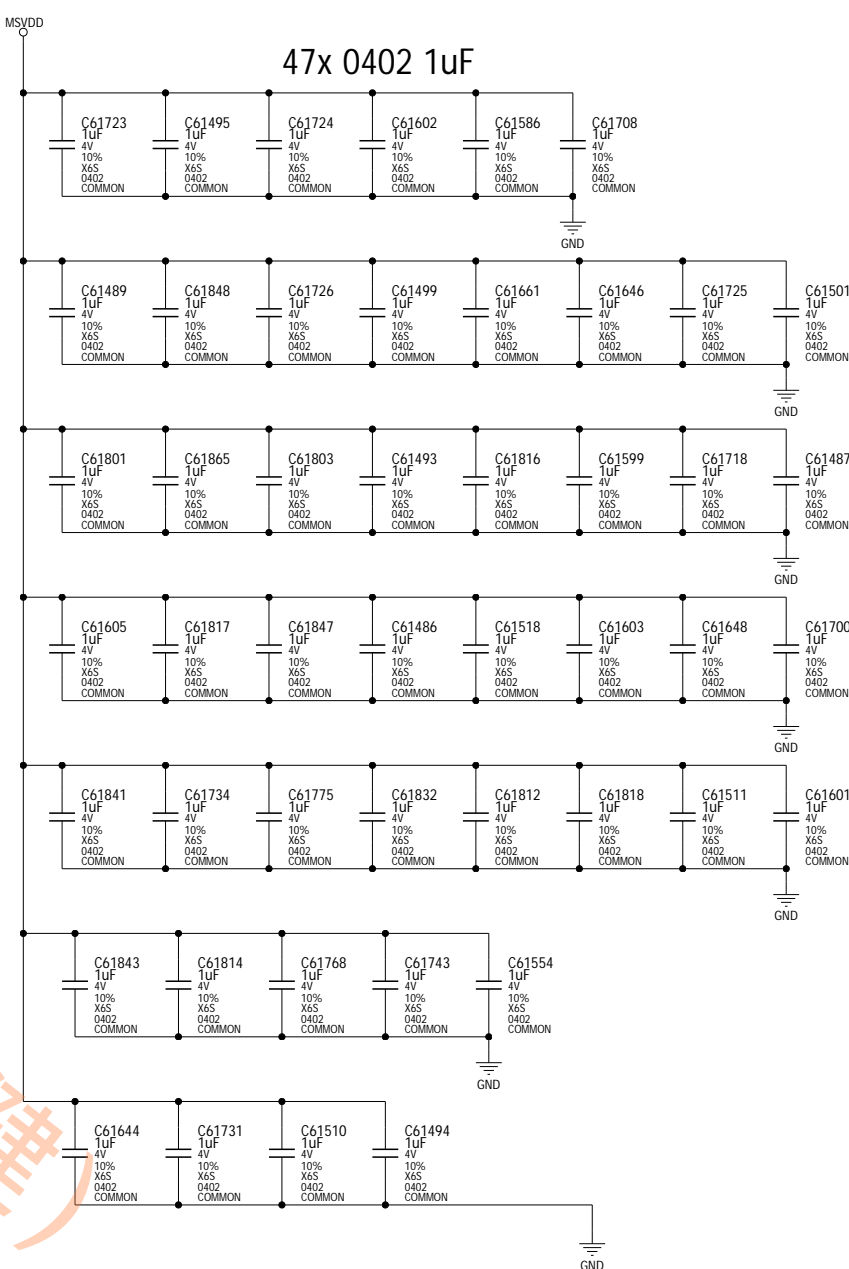
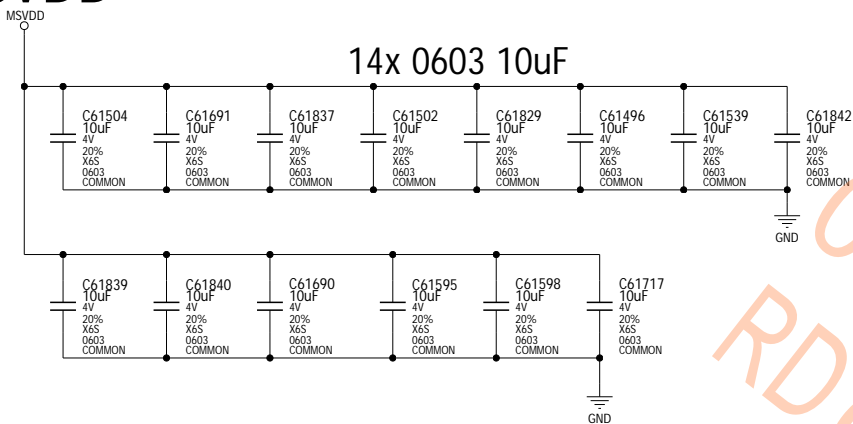
Close to GPU



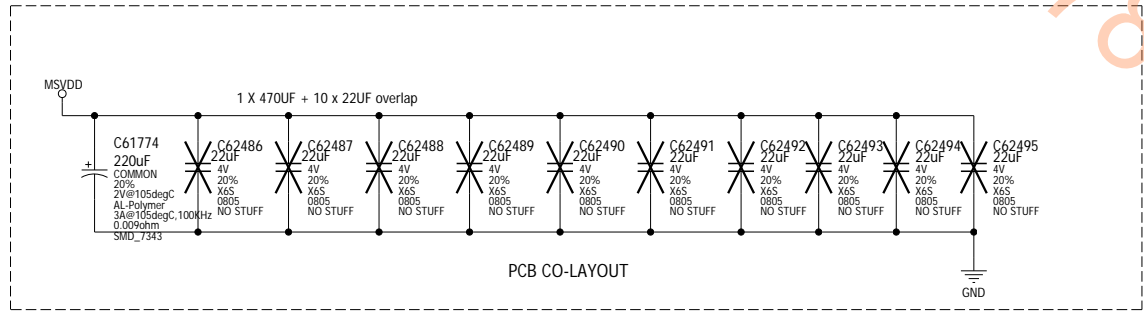
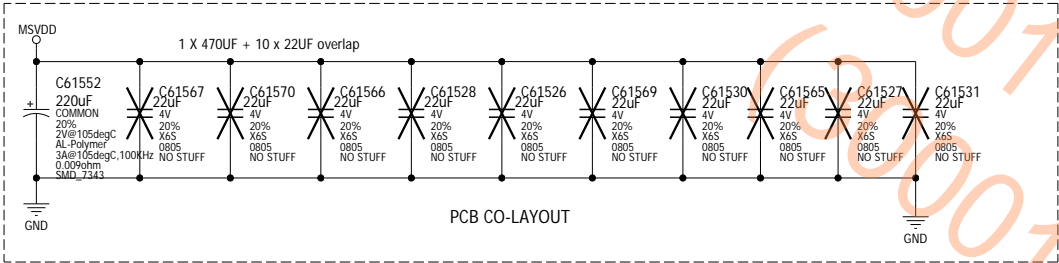
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UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

	A	B	C	D	E	F	G	H
1								
2								
3								
4								
5								

00205363 MS1 CONFIDENTIAL
RD(C) 2020102001 RMA工程課
唐浩健 (30001789)

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PAGE DETAIL	BLANK

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NVHS Interface and FRAME LOCK



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PAGE DETAIL	NVHS x16

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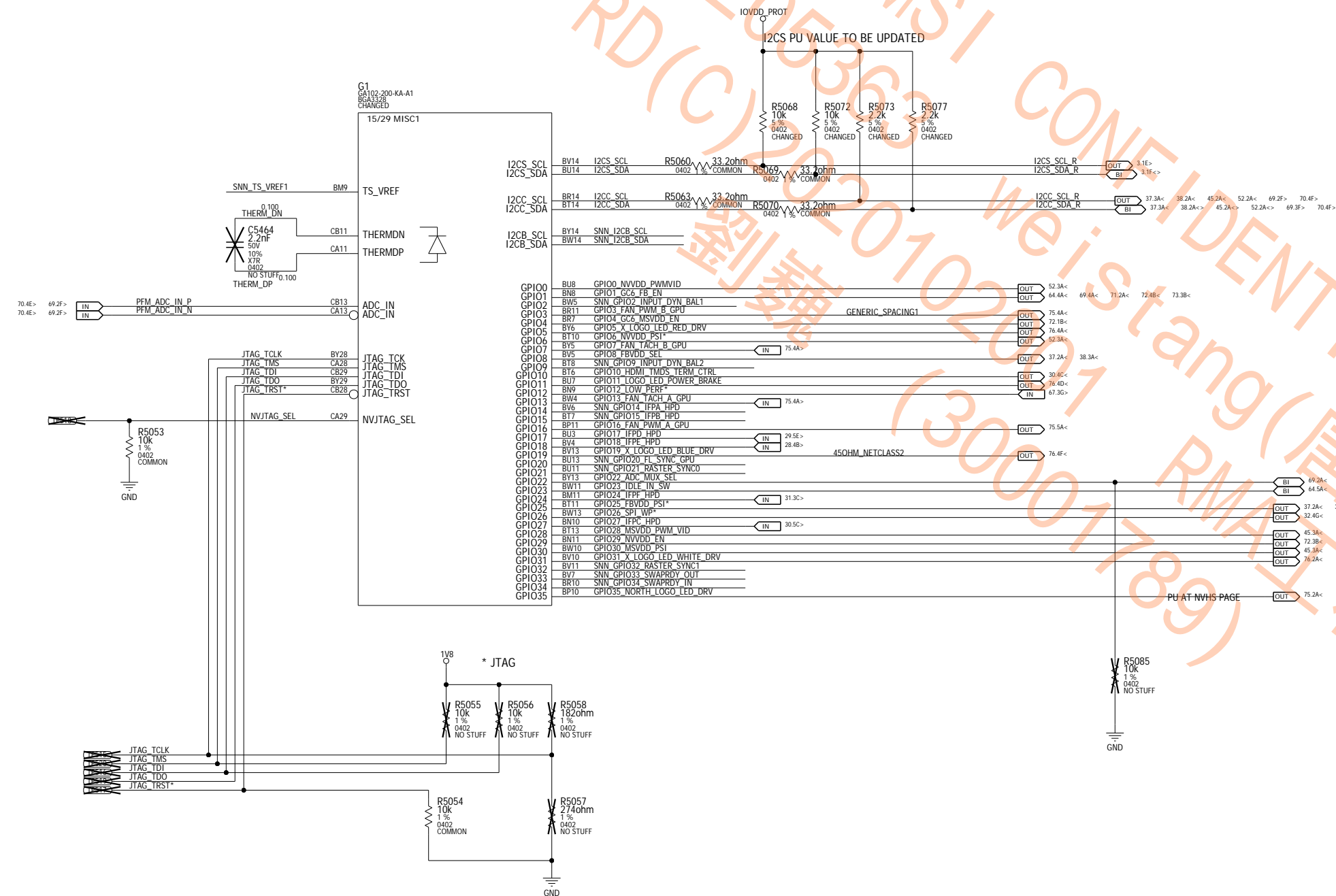
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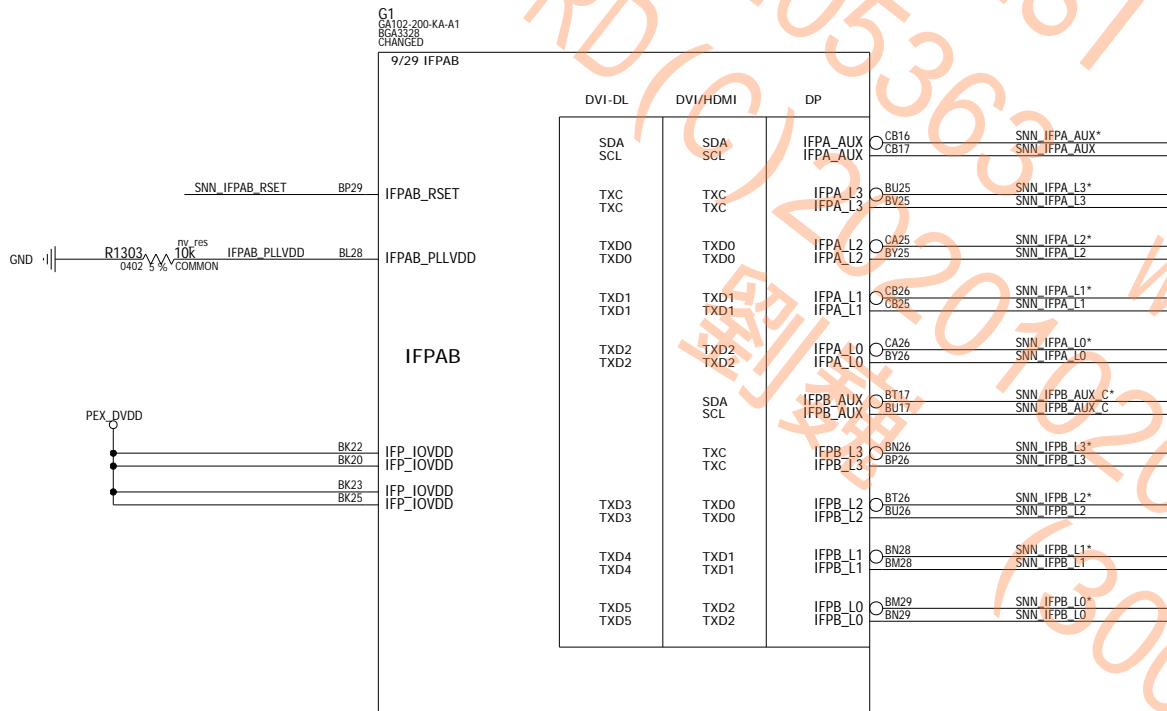
MISC1: Fan, Thermal, JTAG, GPIO, STEREO



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NV_PN 600-1G132-0030-300			
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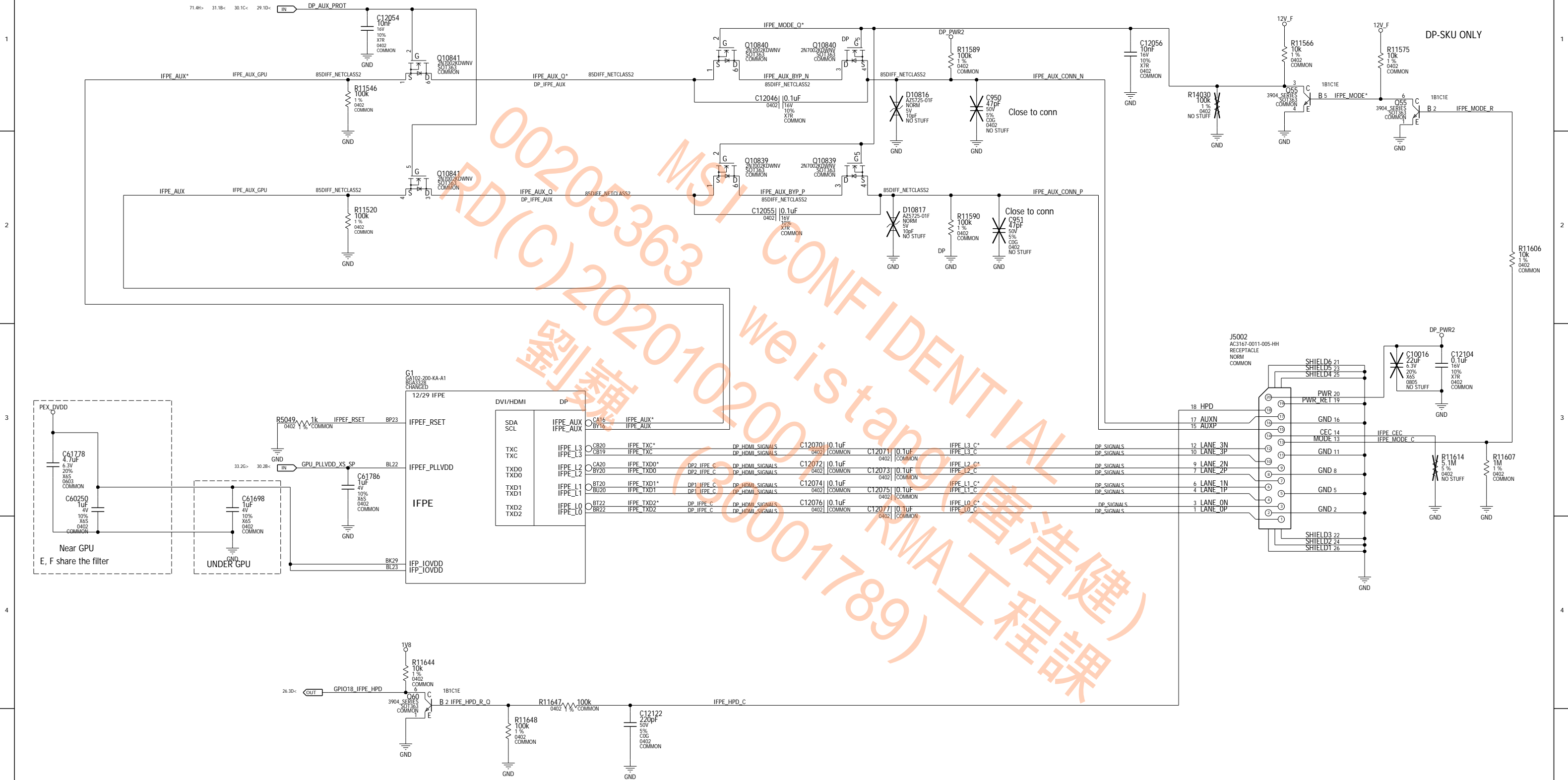
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IFPA UNUSED, IFPB UNUSED



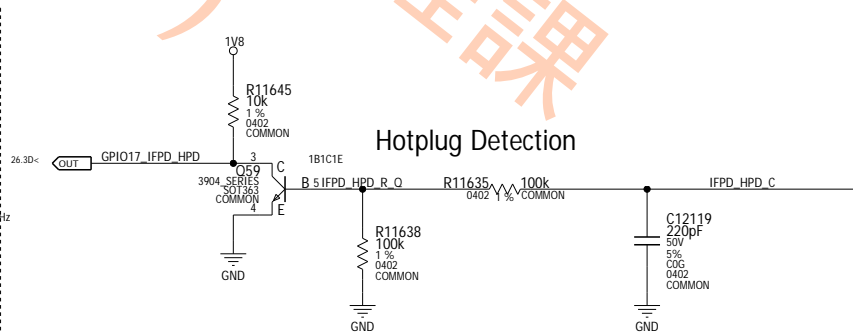
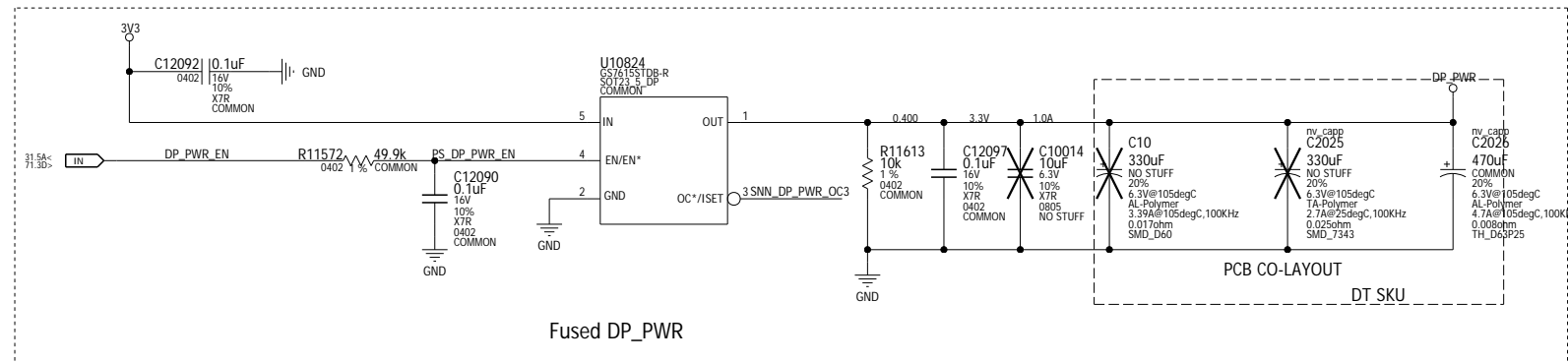
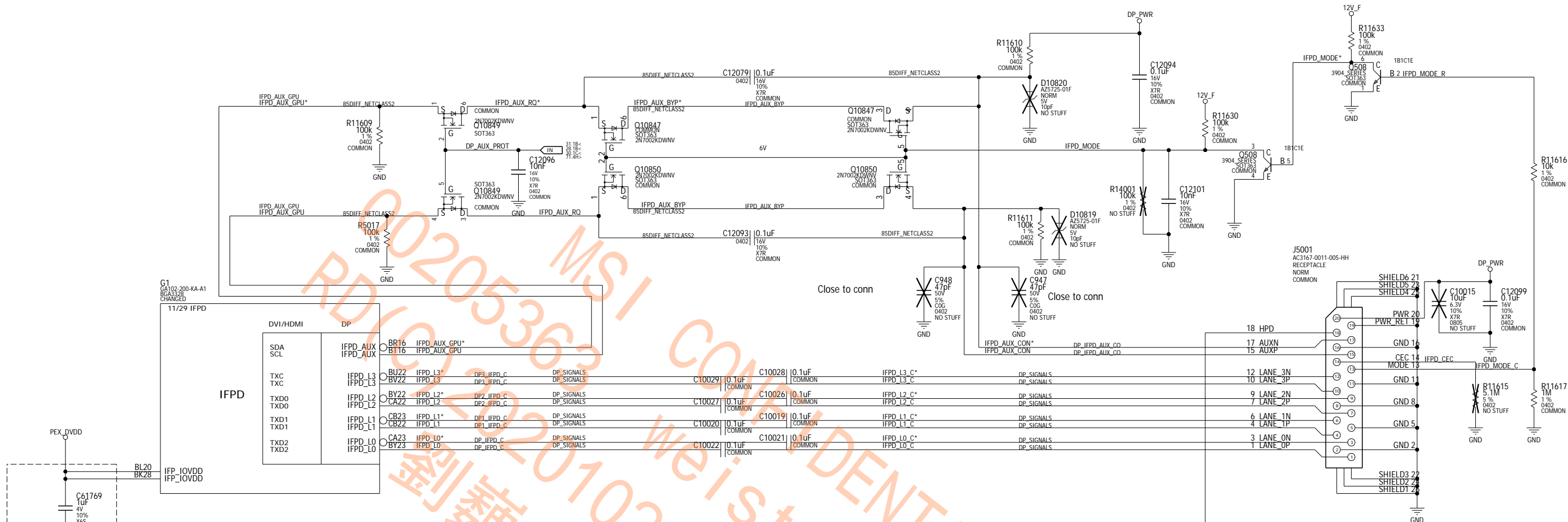
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IFPE DP



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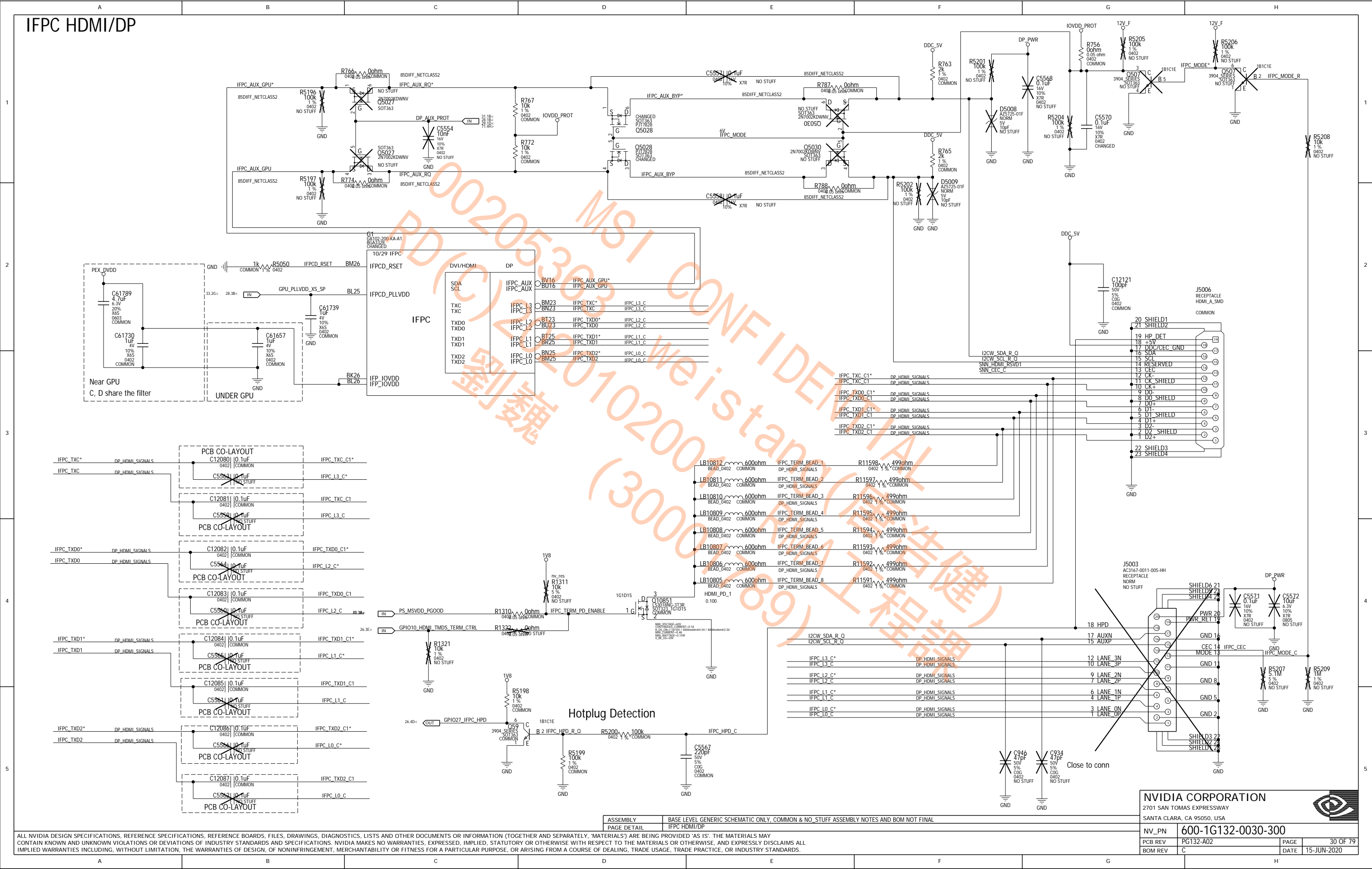
IFPD DP



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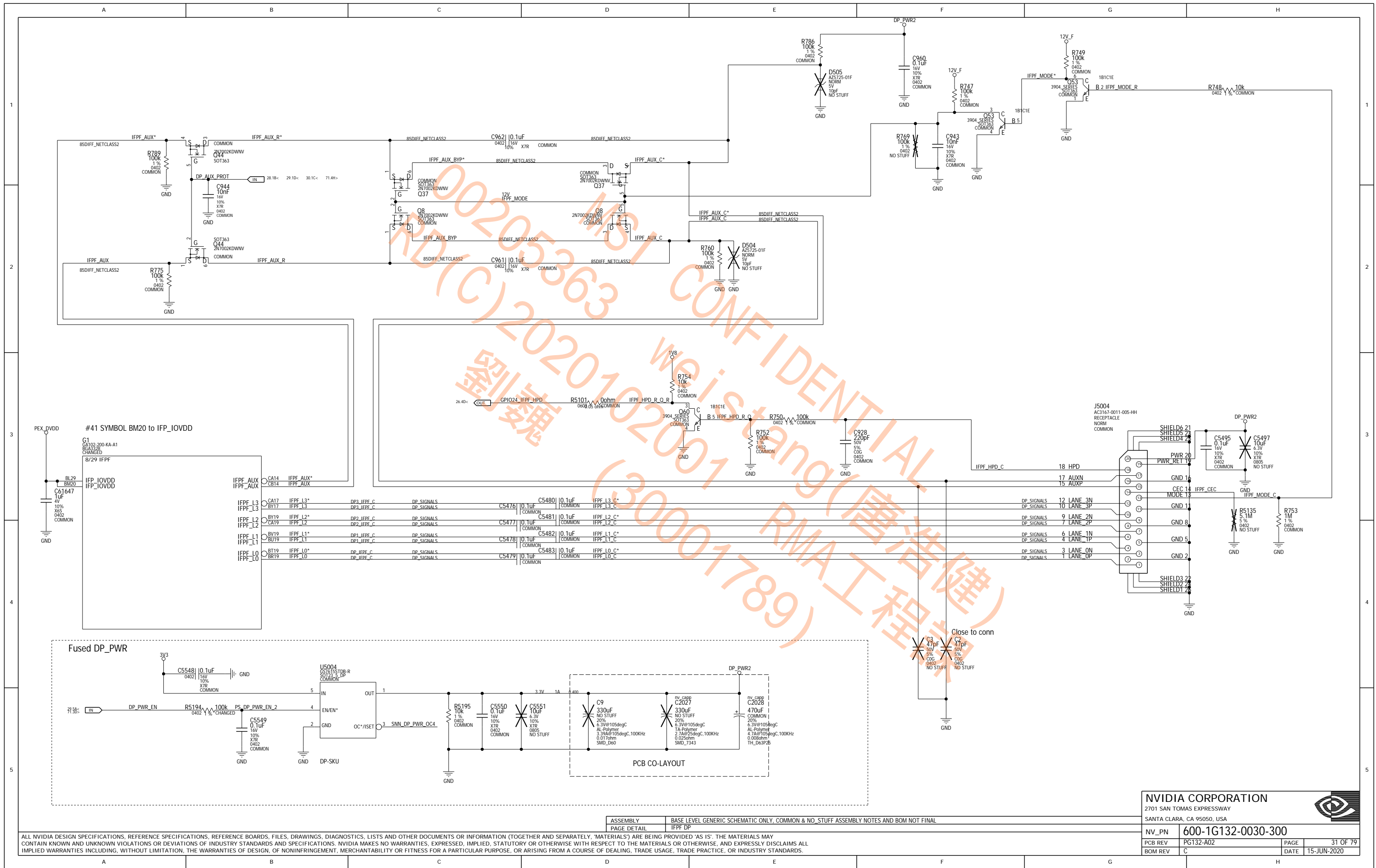
IFPC HDMI/DP



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PAGE DETAIL	IFPC HDMI/DP

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MISC: ROM, Straps

GROUP0 STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
H	H	H	0111	FS_OVERT ENABLE	DEFAULT
L	L	L	0000	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

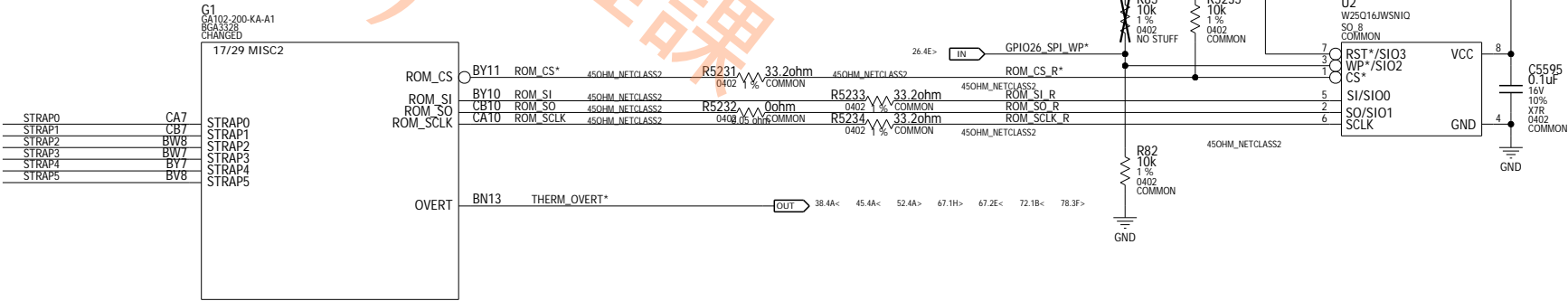
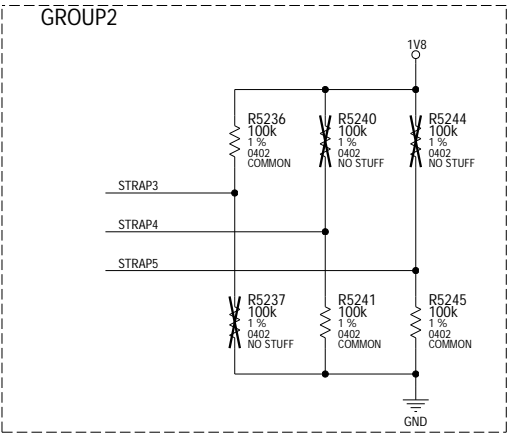
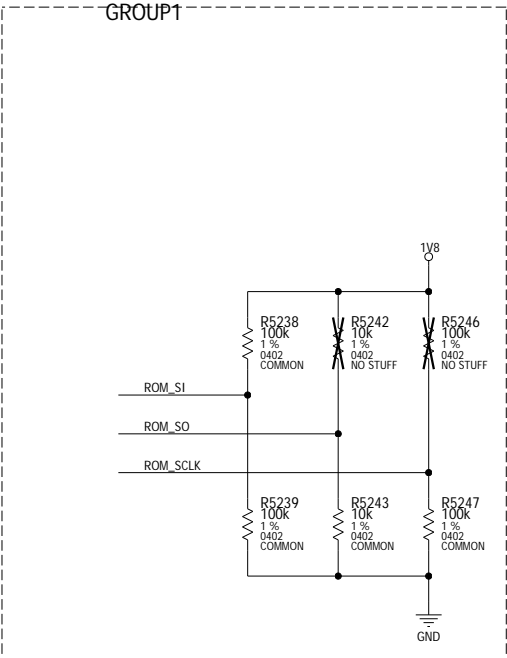
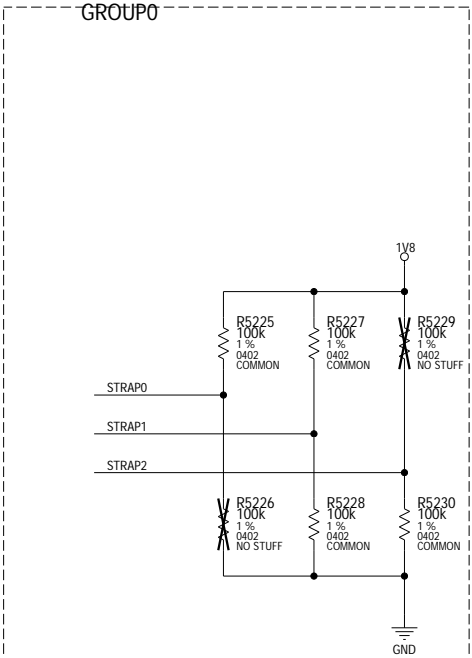
Default

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

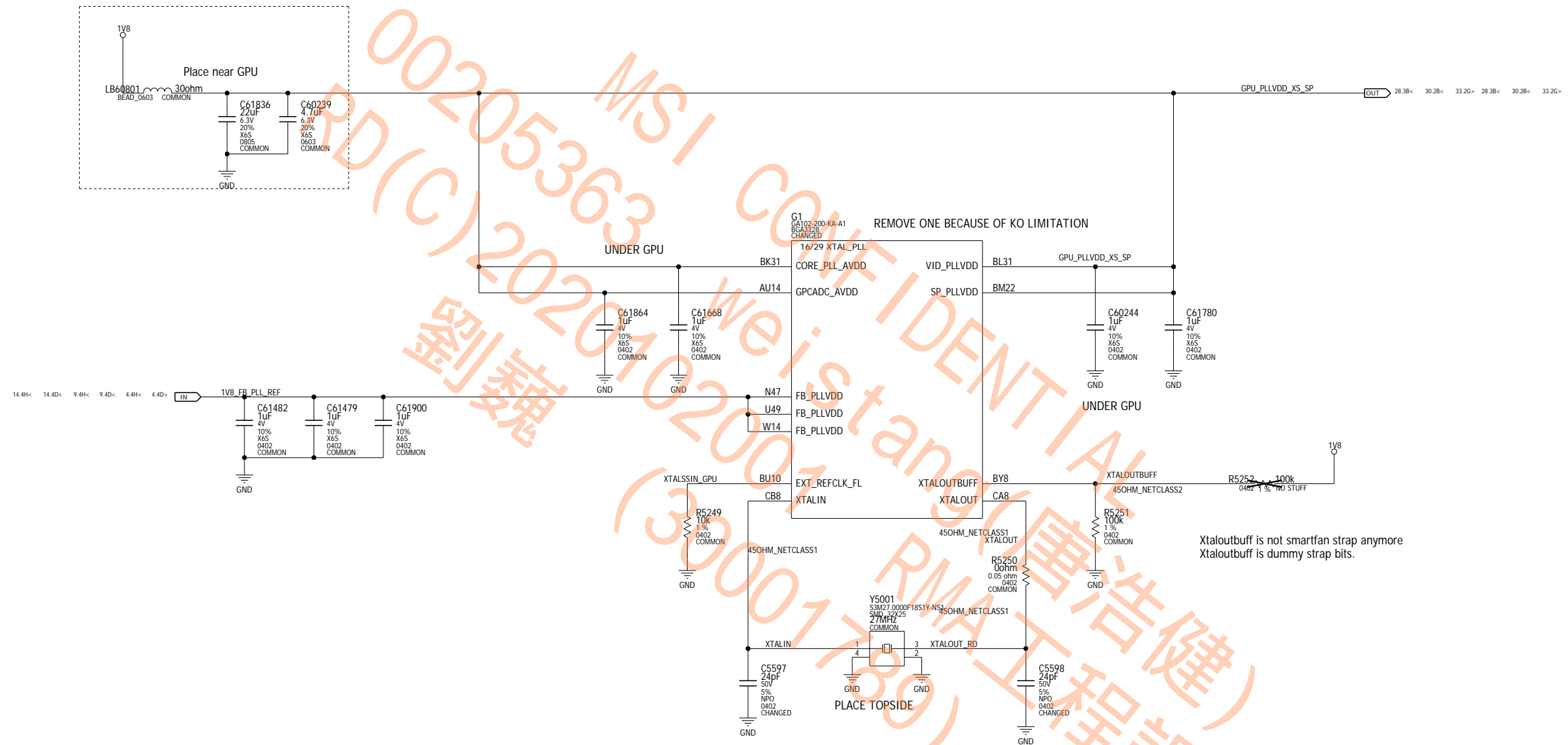
<-A01 PCB


<-OLD

<-LATEST A02 PCB



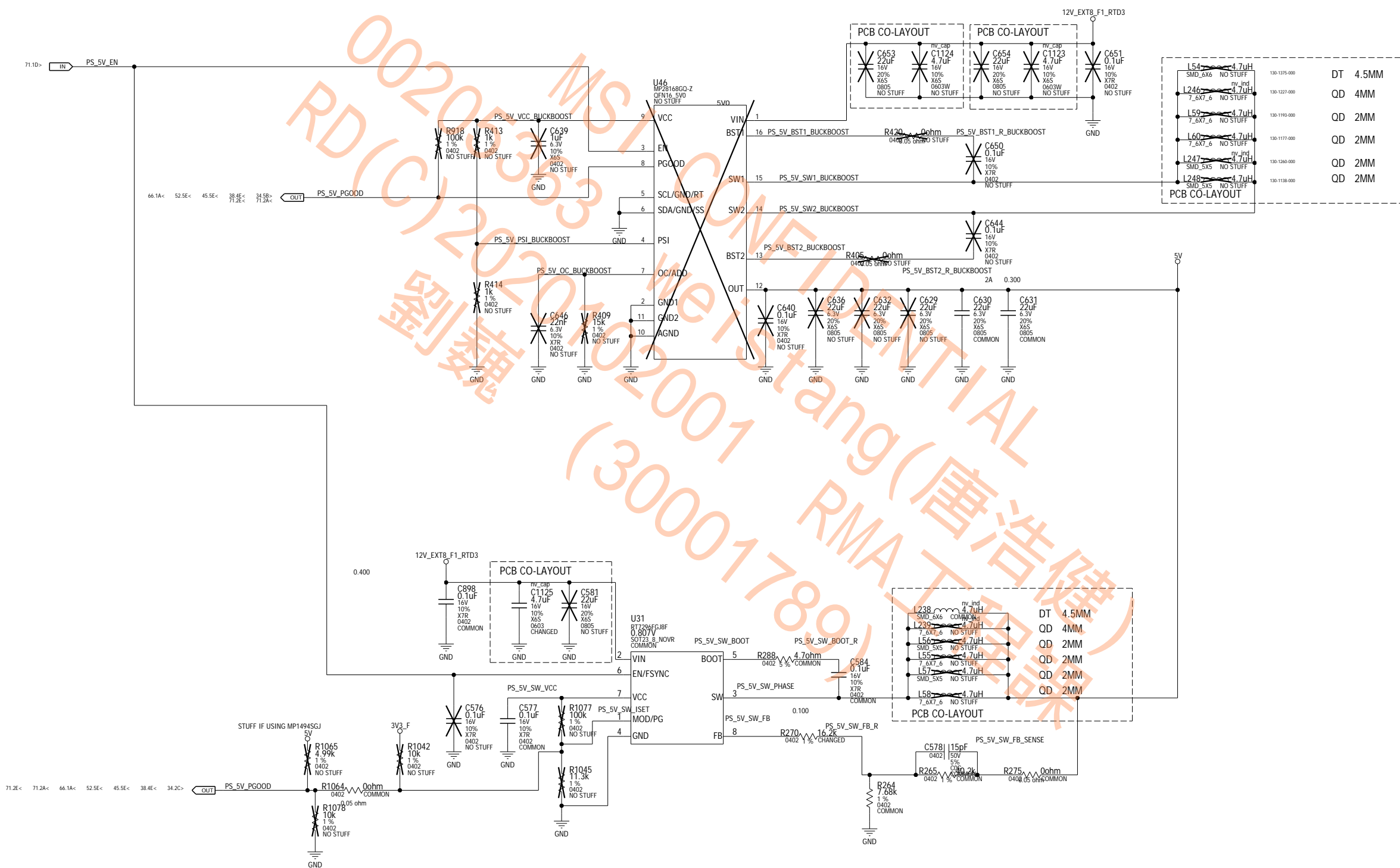
MISC: XTAL. PLL



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NV_PN		600-1G132-0030-300	
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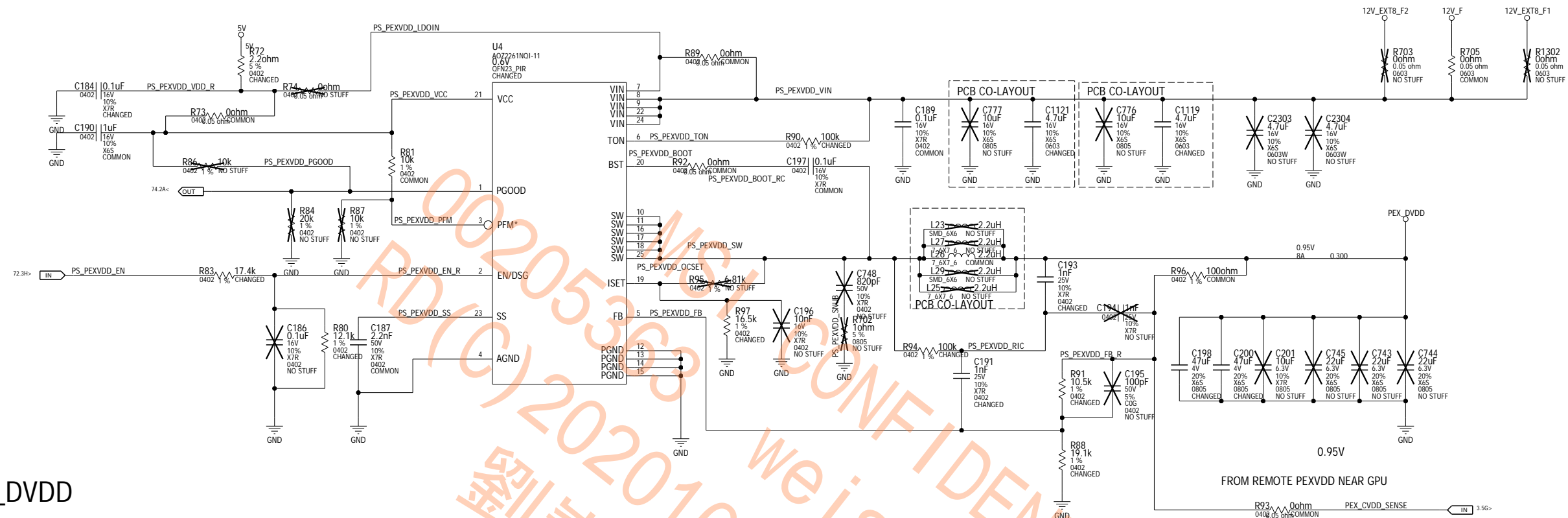
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PS: 5V, 5V_BACKUP

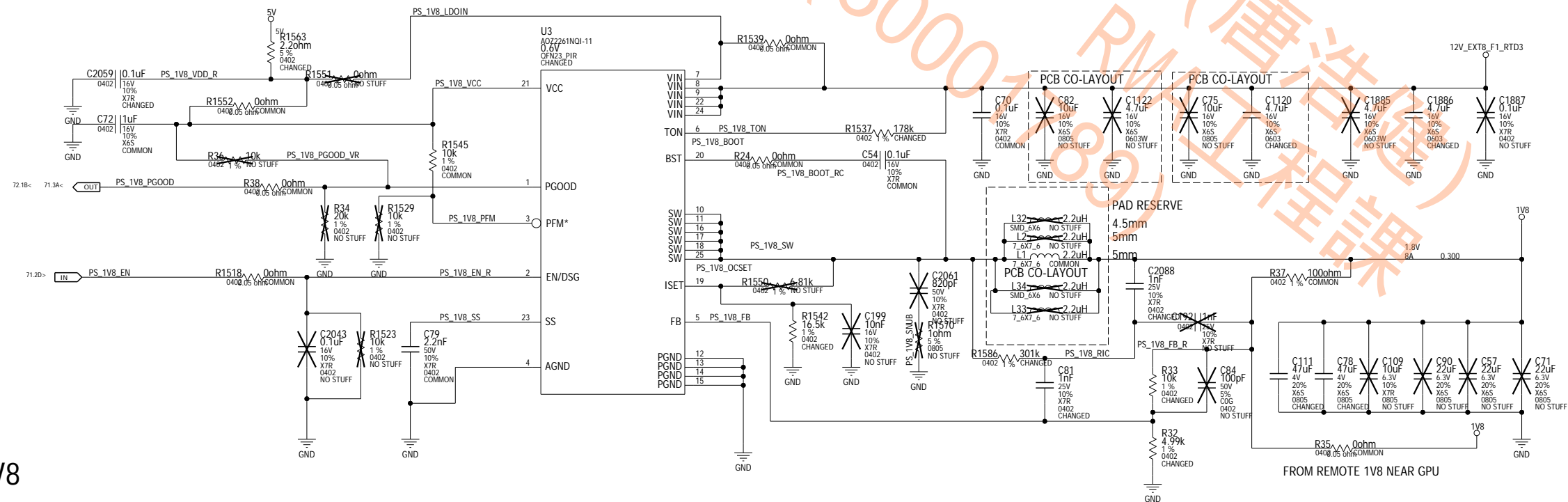


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PS: PEX_DVDD 1V8 Rail



PEX_DVDD



1V8

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PAGE DETAIL	PS: PEX_DVDD and 1V8

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3								
4								
5								

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RD(C) 2020102001 Weistang (唐浩健)
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(30001789) RMA工程課


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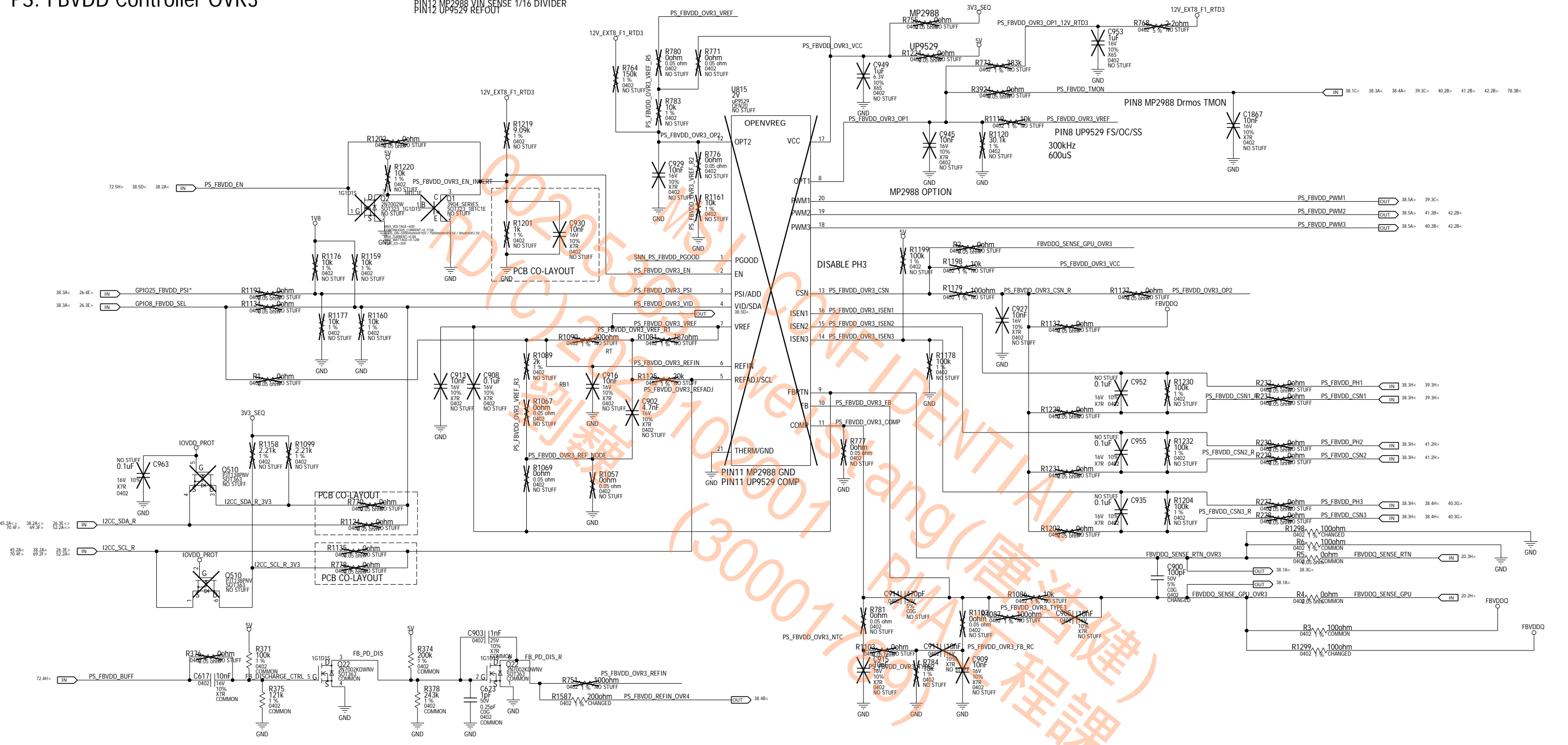
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PS: FBVDD Controller OVR3

PIN12 MP2988 VIN SENSE 1/16 DIVIDER
PIN12 UP9529 REFOUT

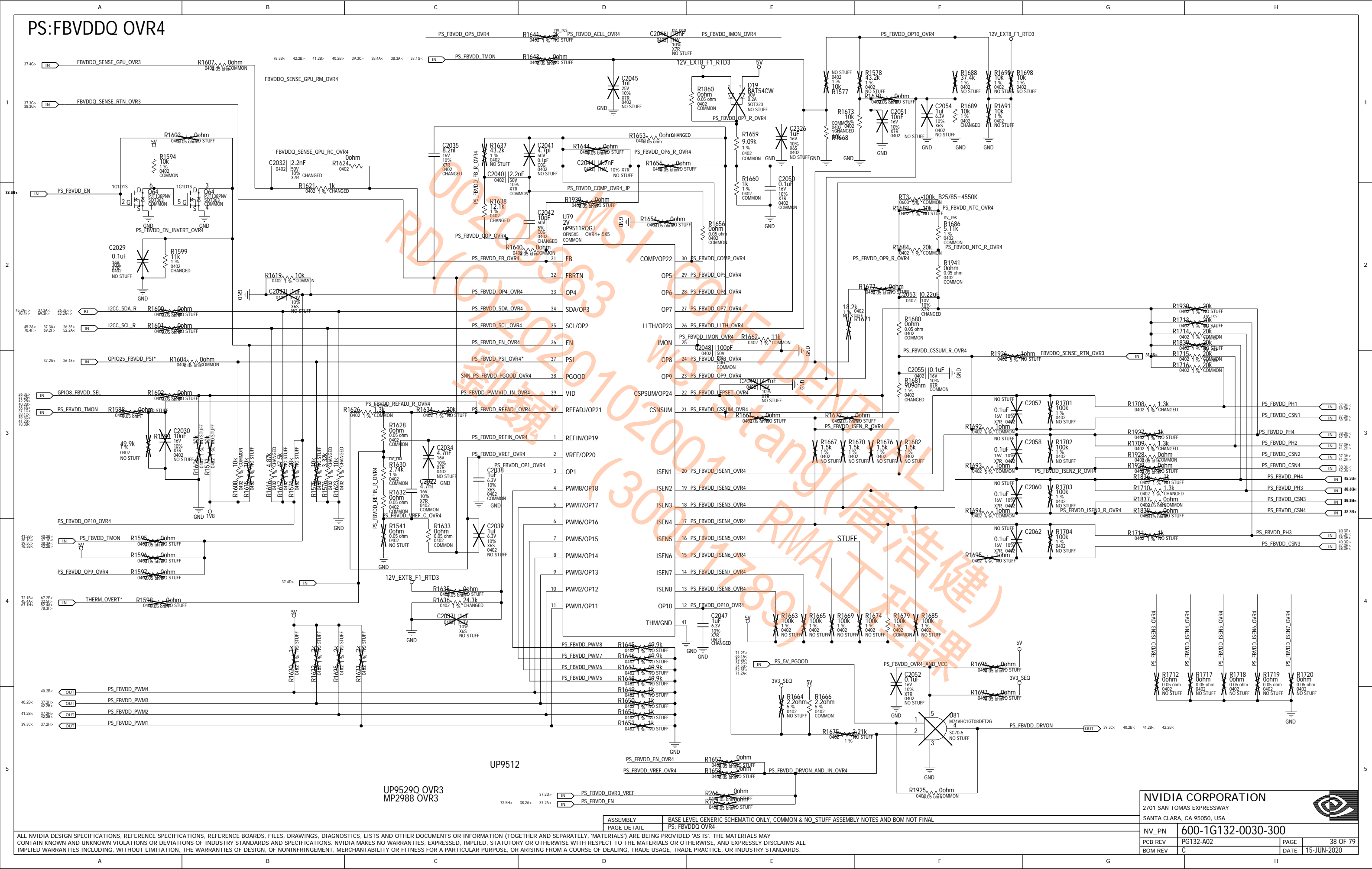
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PAGE DETAIL	PS: FBVDD Controller OVR3

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PS:FBVDDQ OVR4



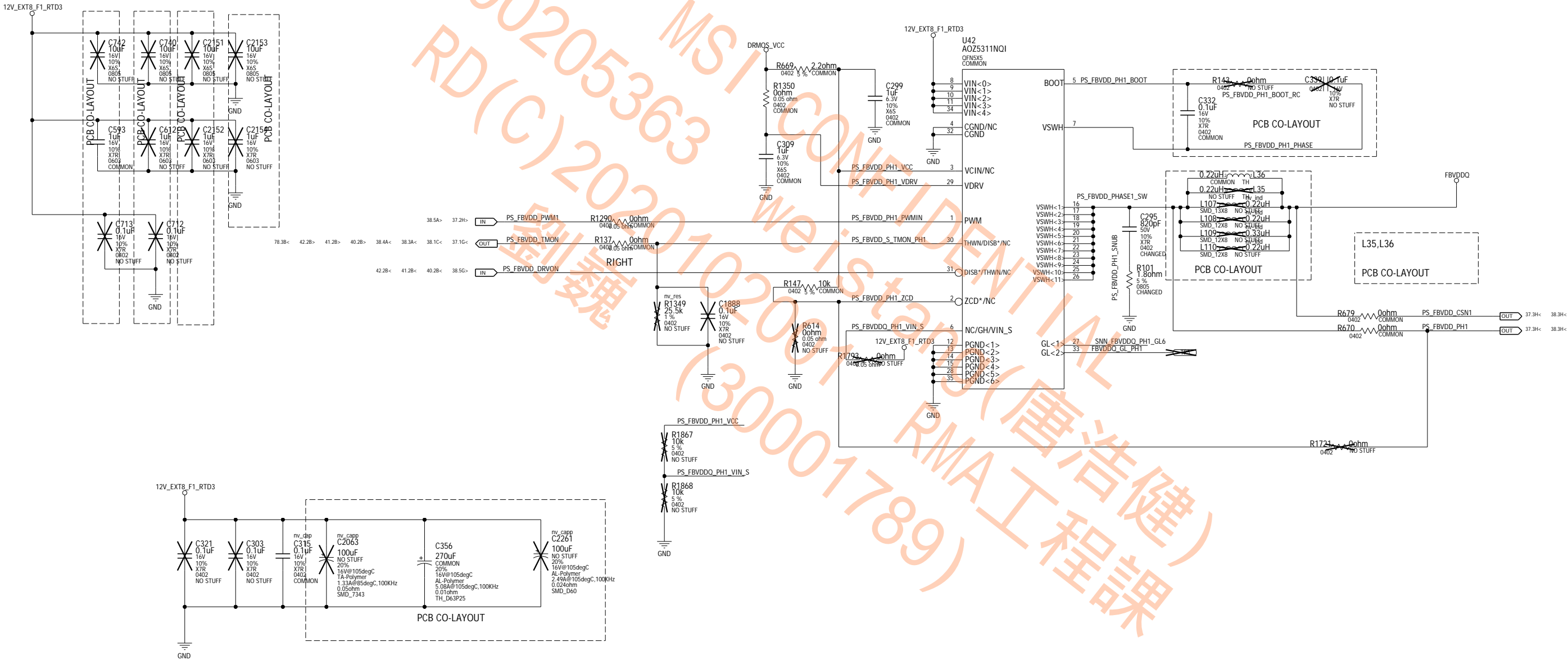
UP9529Q OVR3
MP2988 OVR3

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: FBVDDQ OVR4

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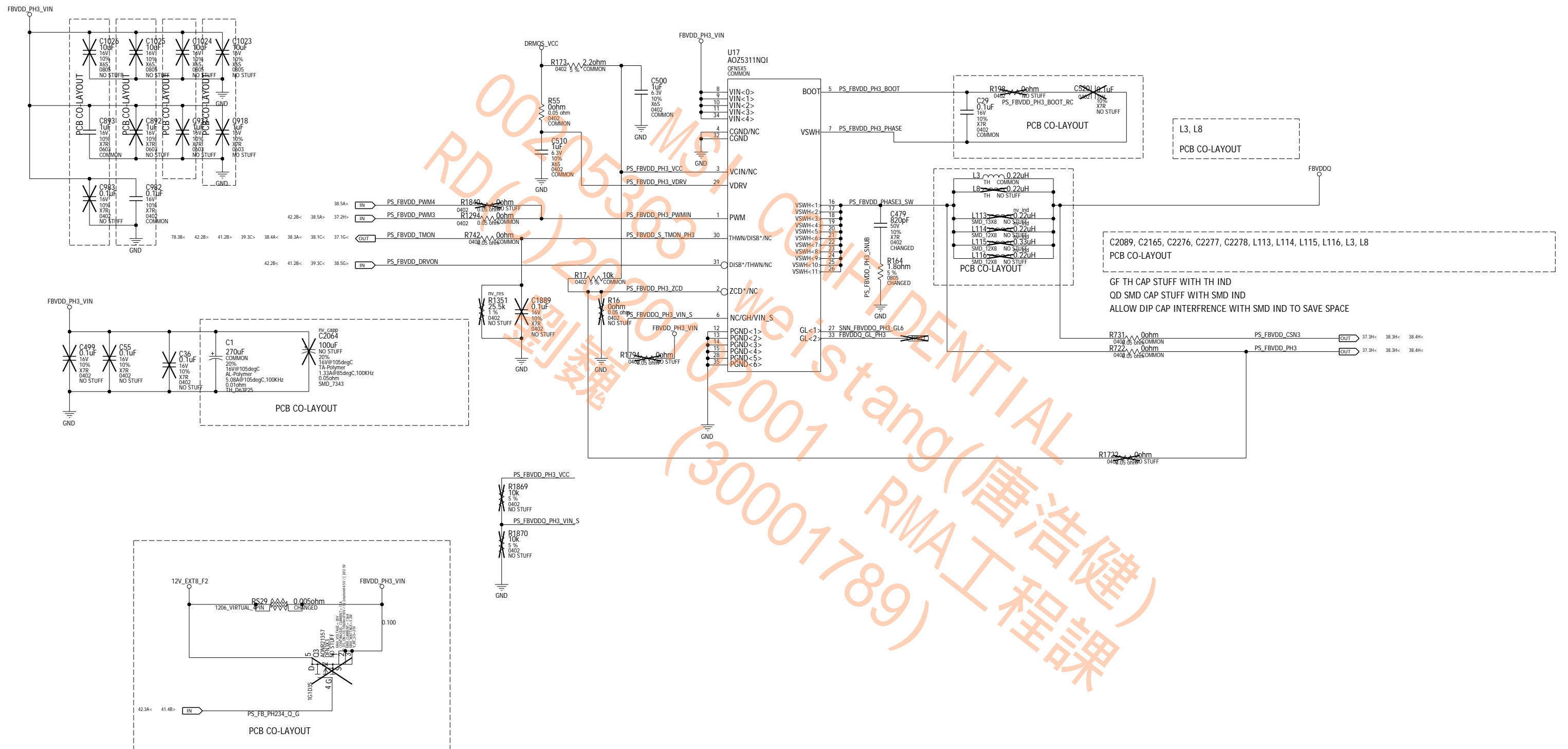
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PS: FBVDD PH1



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PS: FBVDD PH3



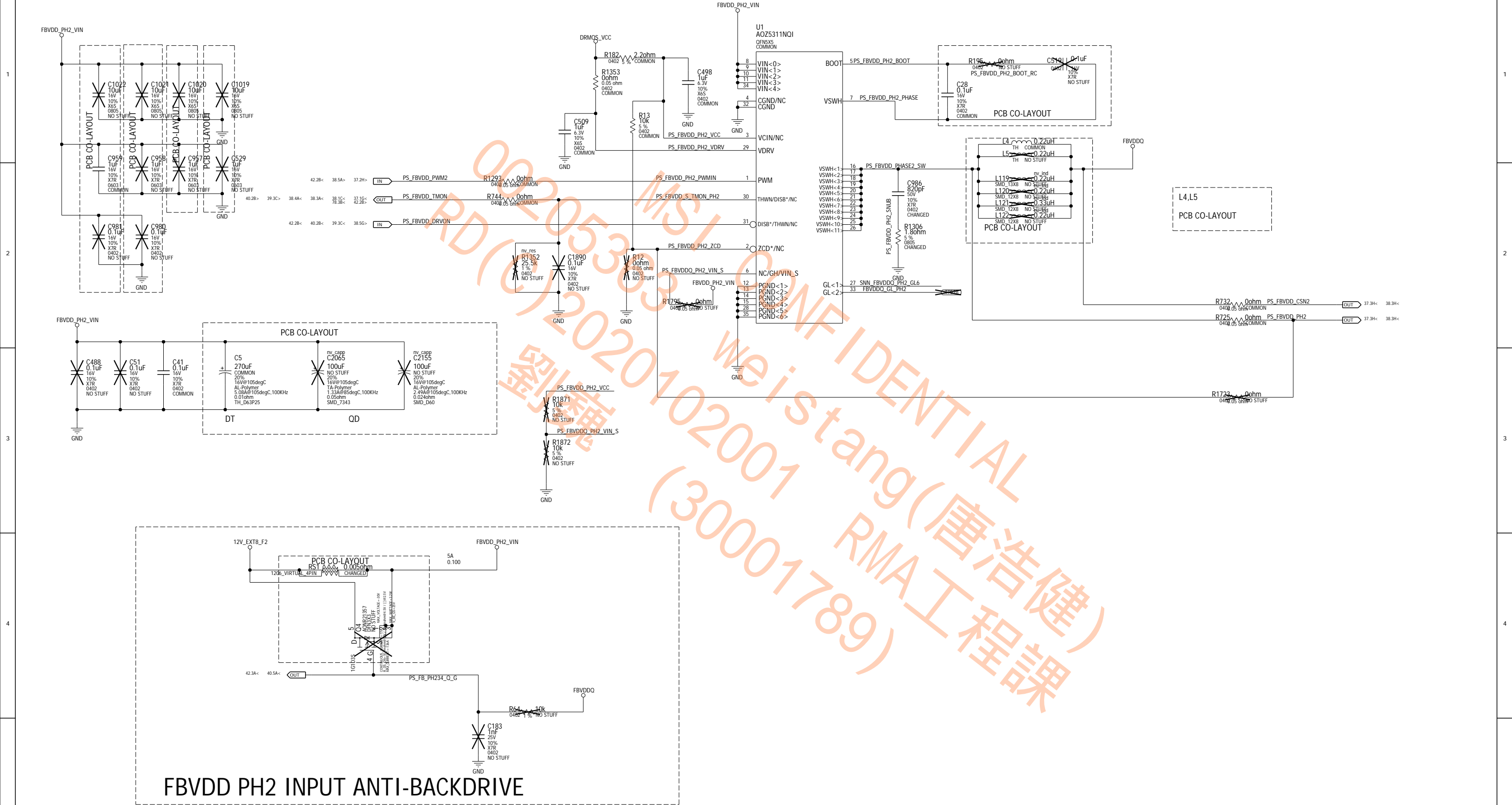
FBVDD PH3 INPUT ANTI-BACKDRIVE

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PAGE DETAIL	PS: FBVDD PH3

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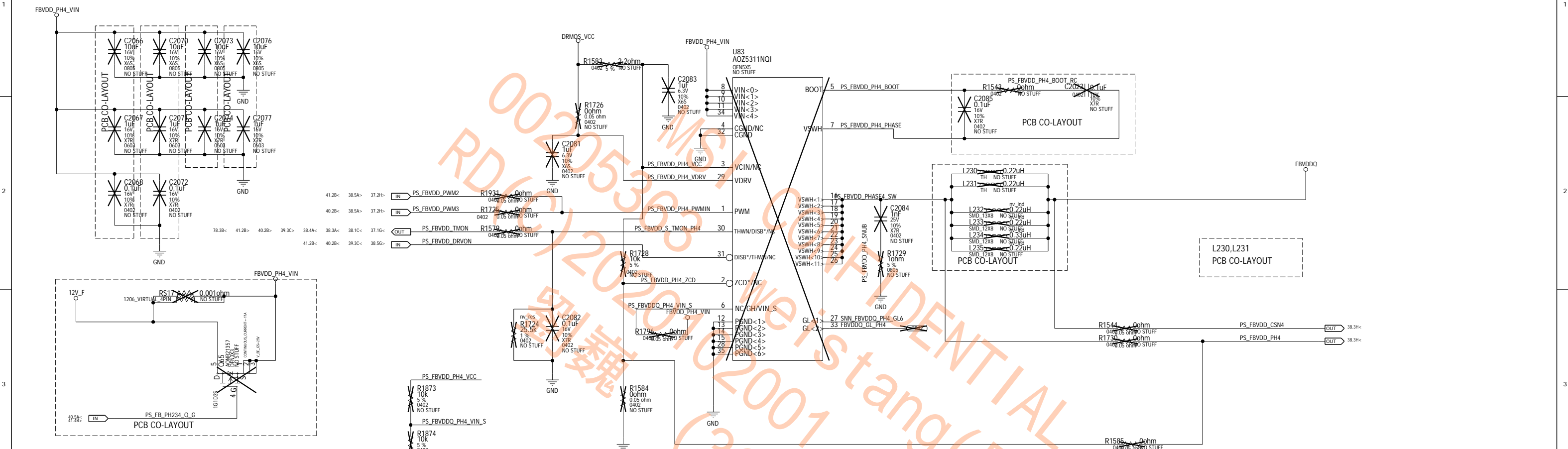
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN		600-1G132-0030-300		
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PS: FBVDD PH2

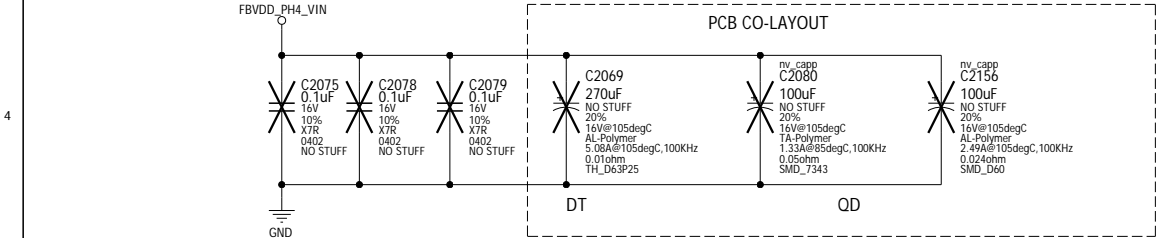


FBVDD PH2 INPUT ANTI-BACKDRIVE

PS: FBVDD PH4



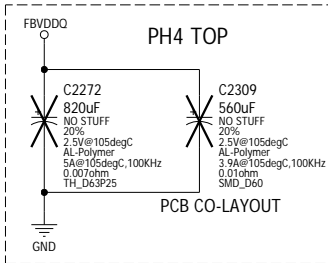
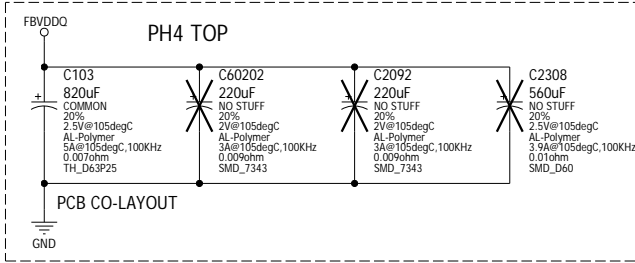
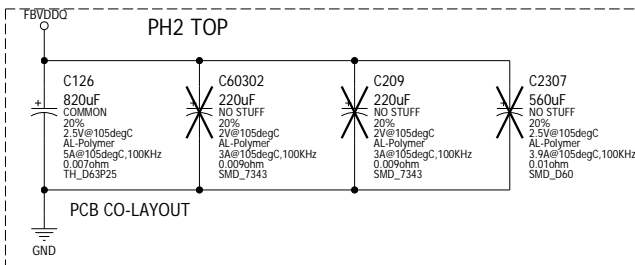
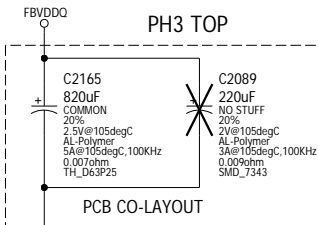
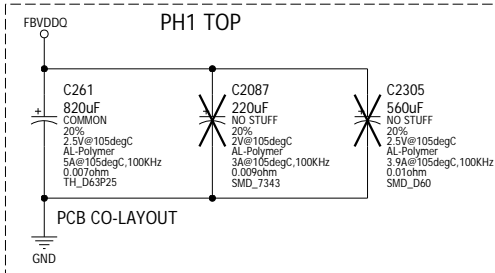
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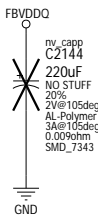
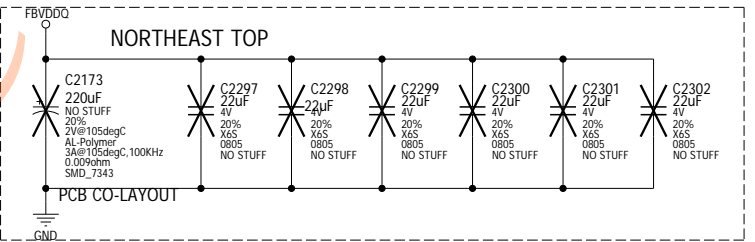
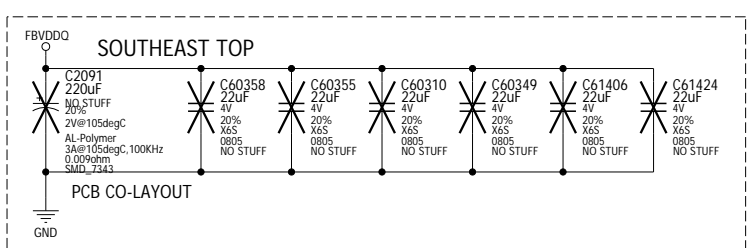
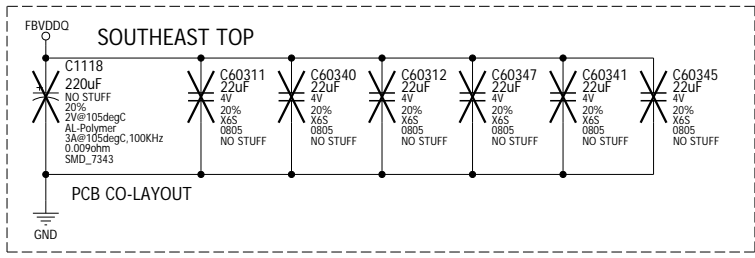
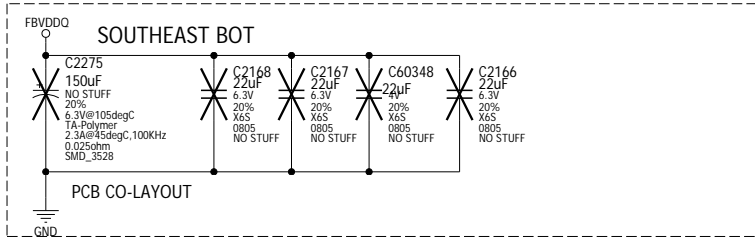
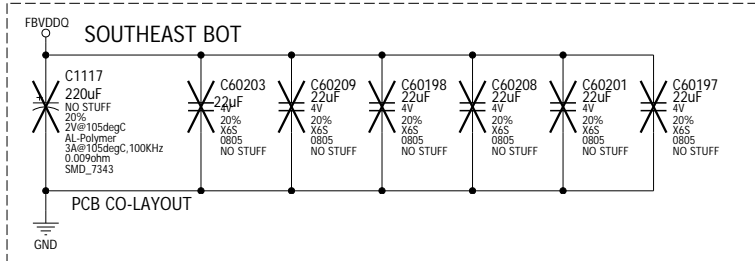
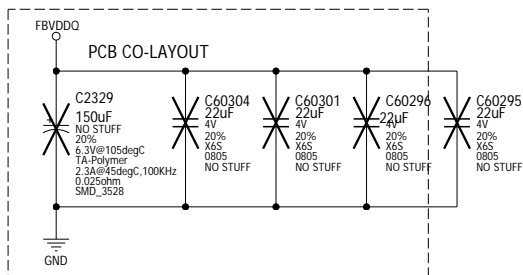
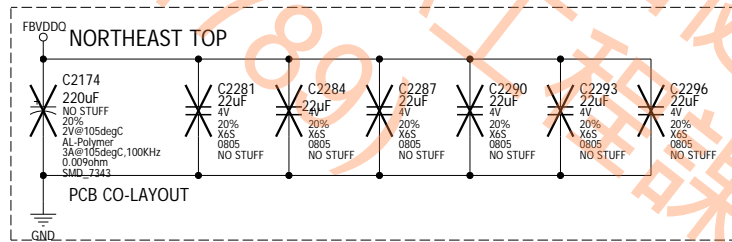
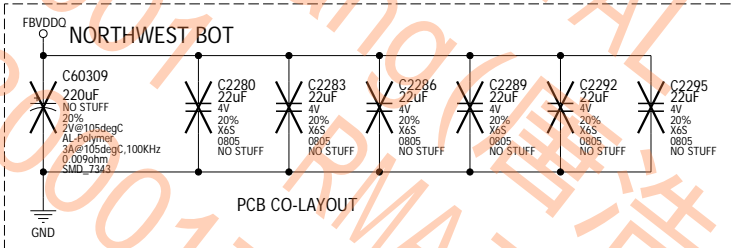
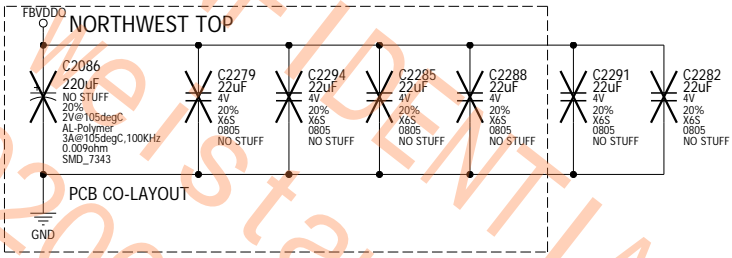
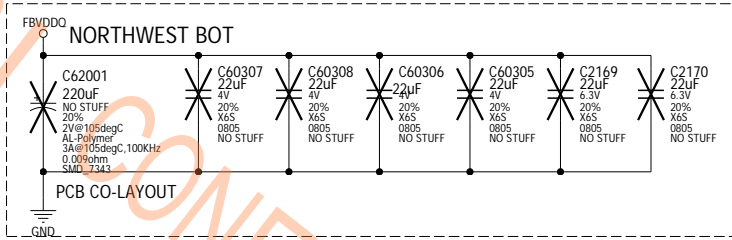
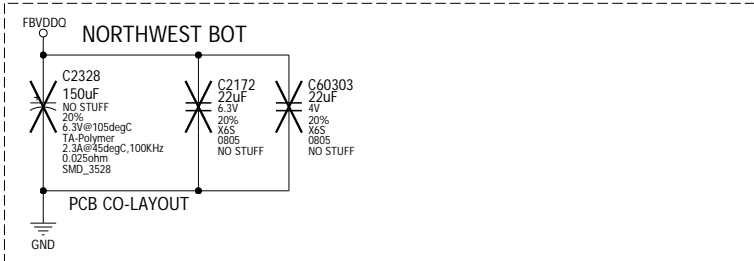
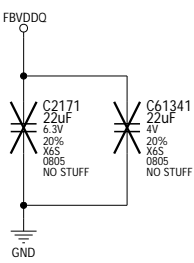
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PS: FBVDD OUTPUT CAP

3x 820uF TH FBVDD OUTPUT BULK CAPS



CLOSE TO FB PH3 OUTPUT STUFF





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PAGE DETAIL	PS: FBVDD_OUTPUT_CAP_NEAR_MEMORY

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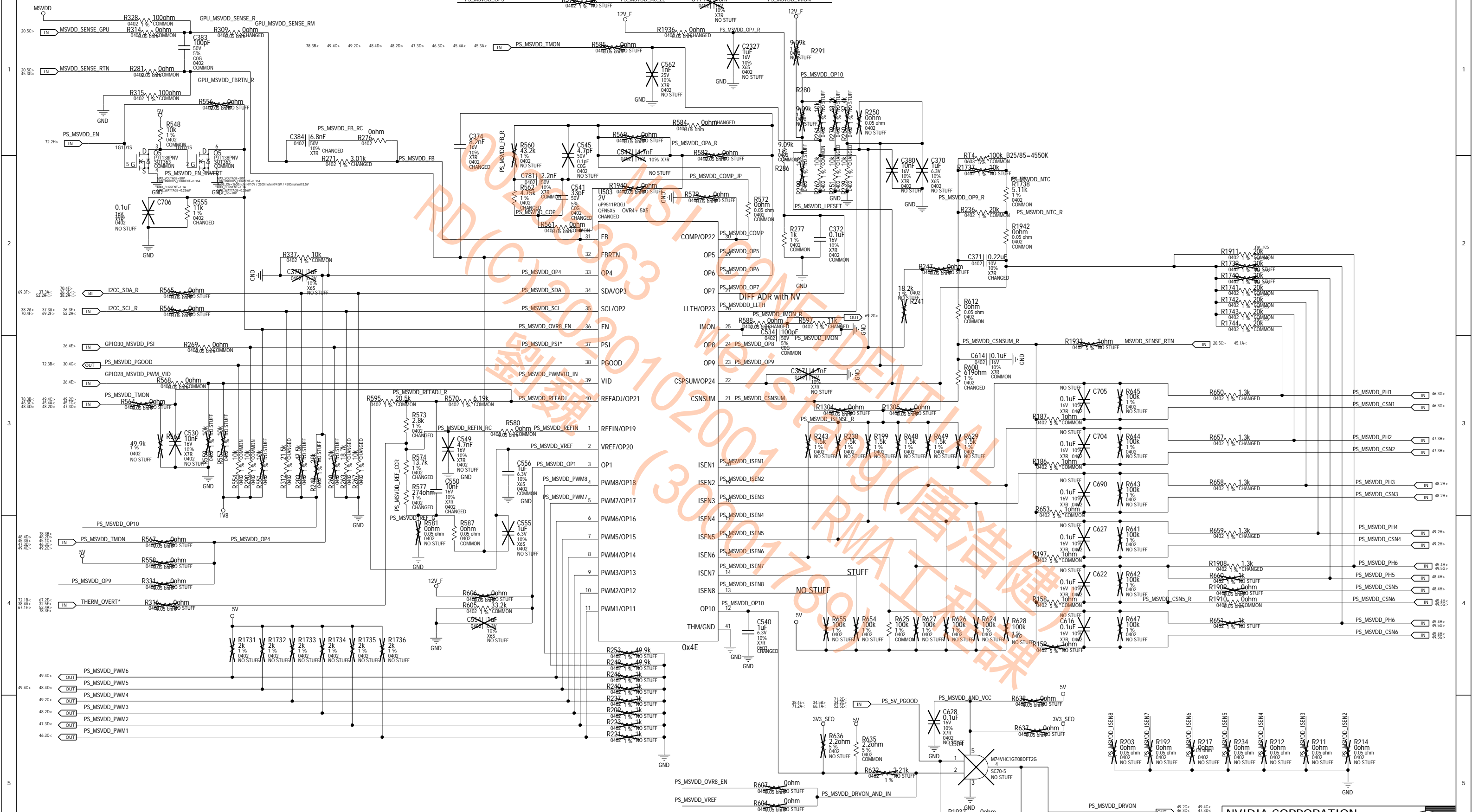
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PS: MSVDD



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PAGE DETAIL	PS: MSVDD CONTROLLER

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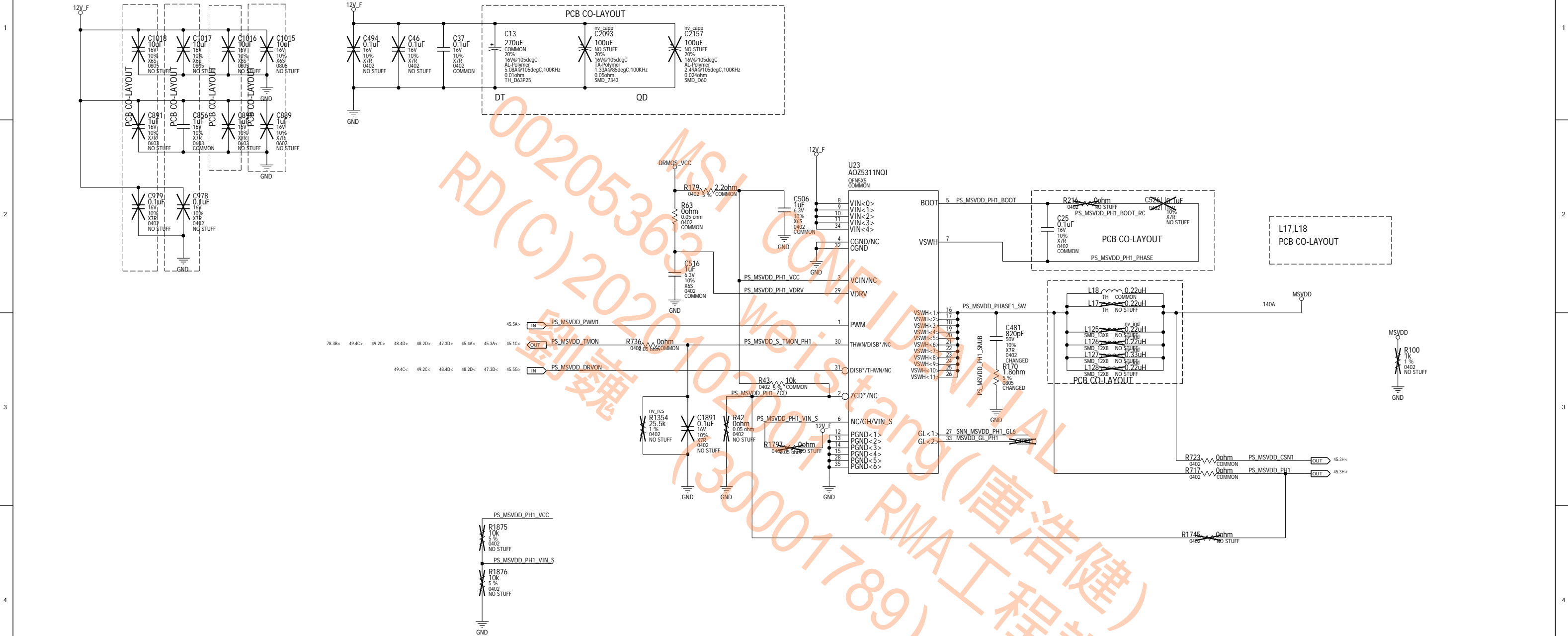
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DATE	15-JUN-2020
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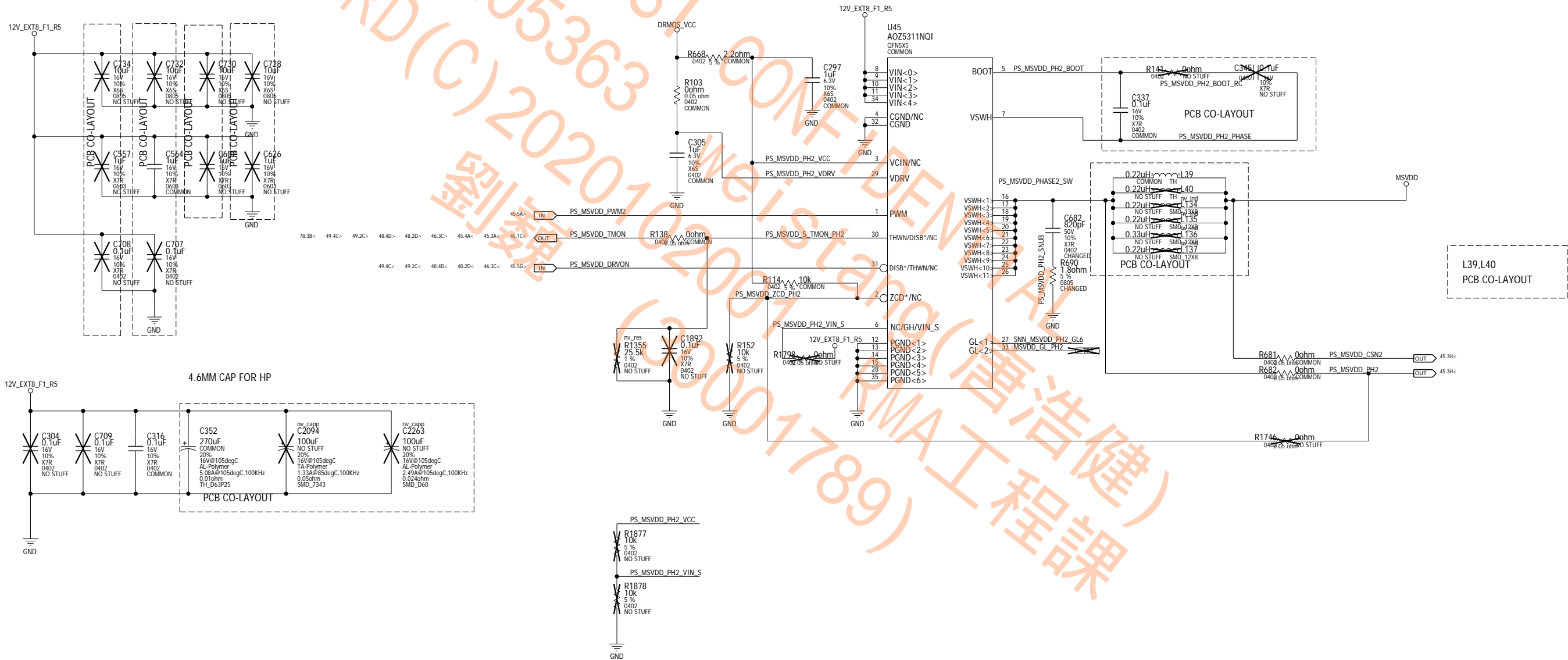


PS: MSVDD Phase 1



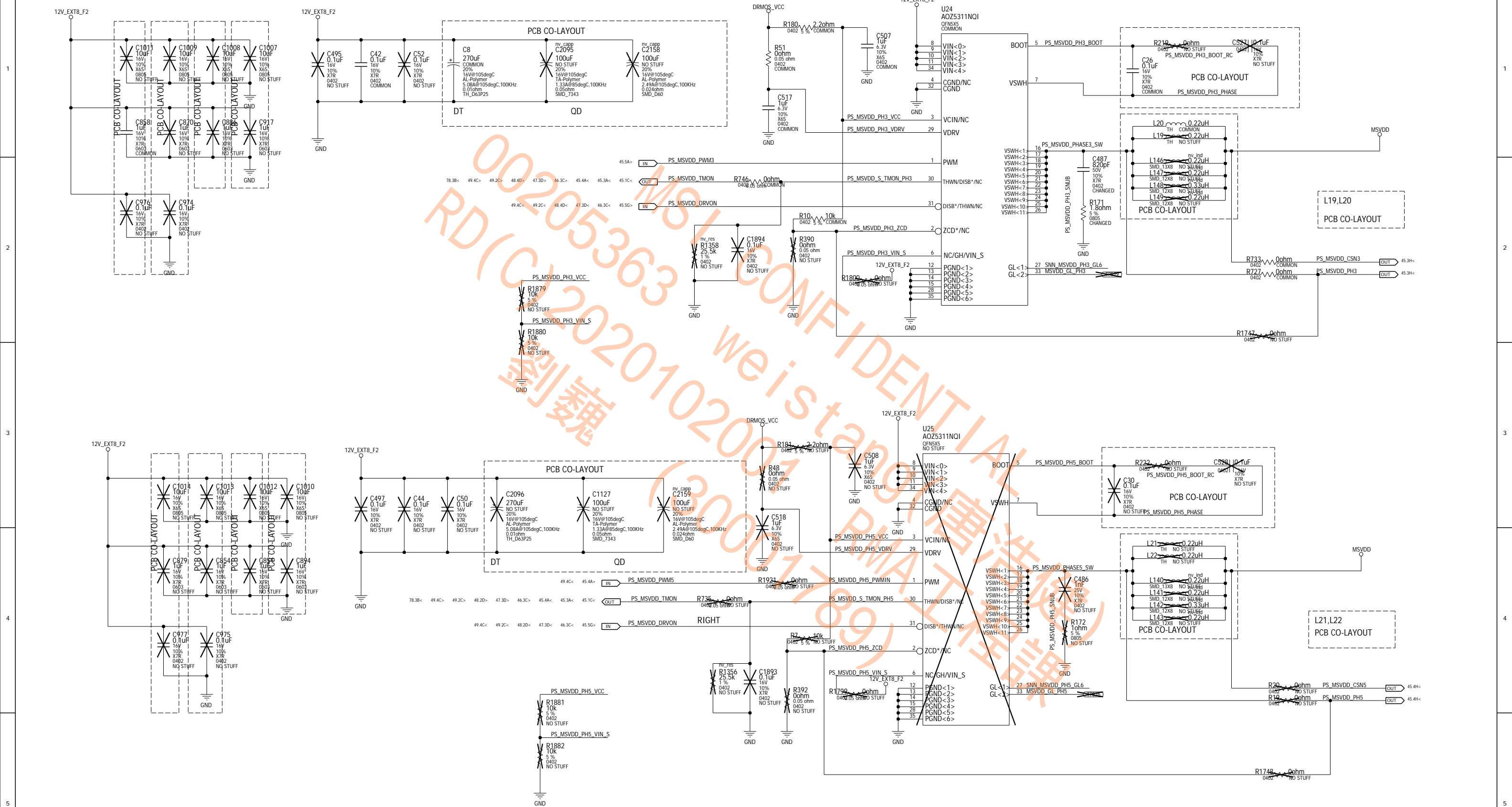
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PS: MSVDD PH 2




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PS:MSVDD Phase 3, 5

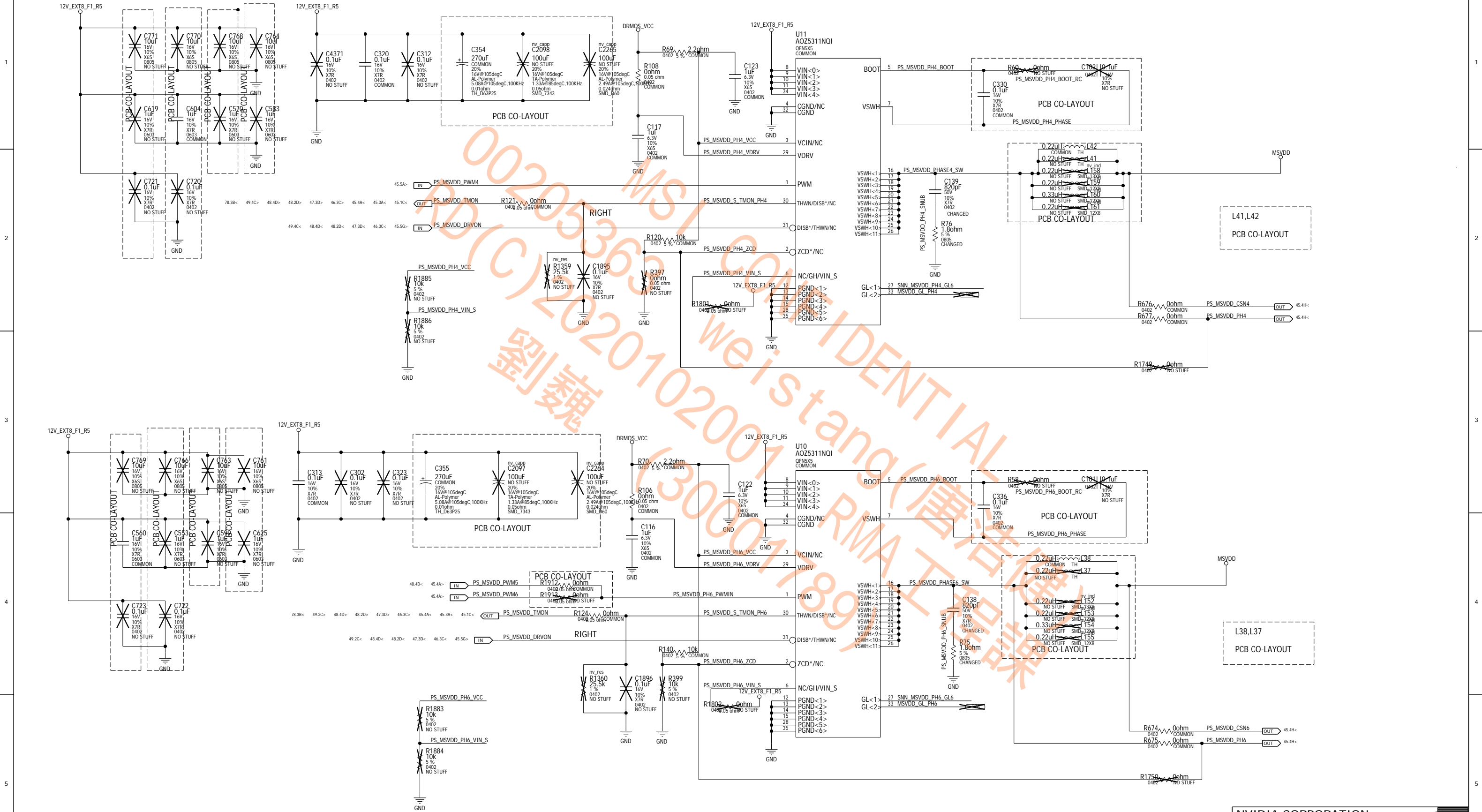


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PAGE DETAIL	PS: MSVDD PH3 and PH5

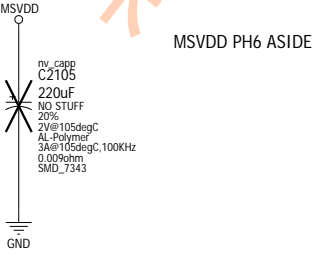
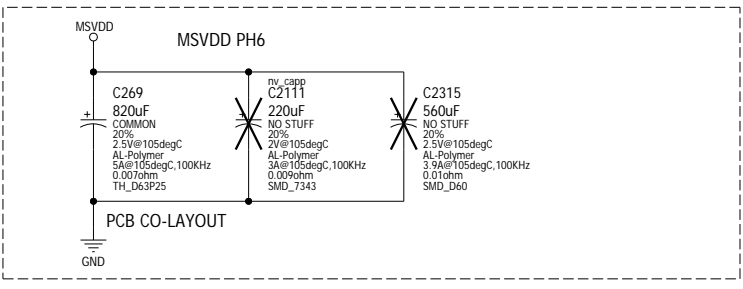
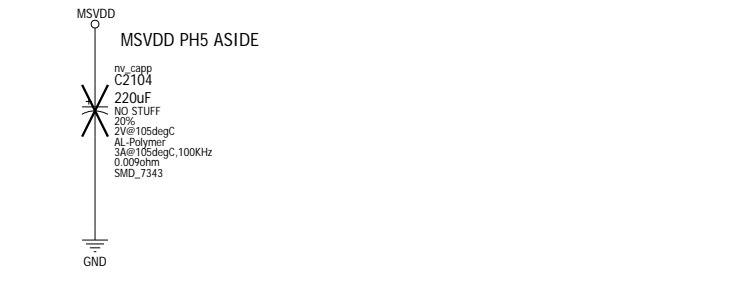
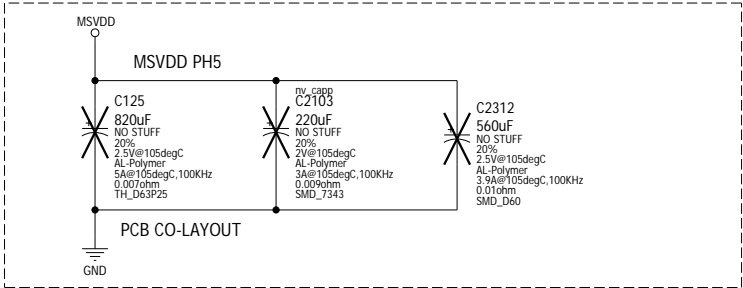
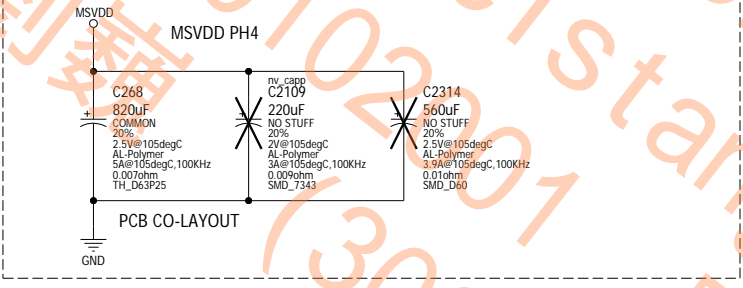
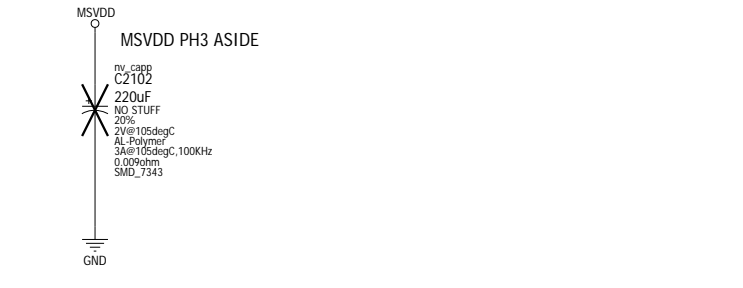
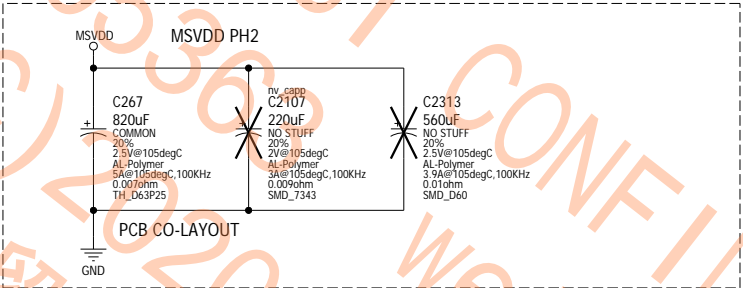
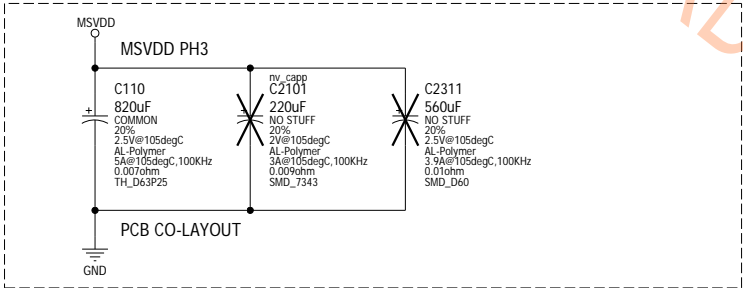
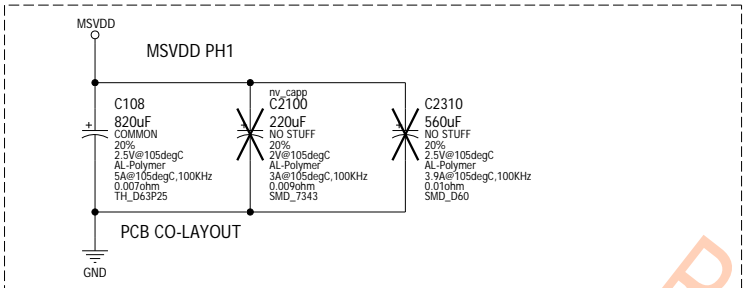
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PS: MSVDD PH 4,6



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PS:MSVDD OUTPUT CAP (TOP)



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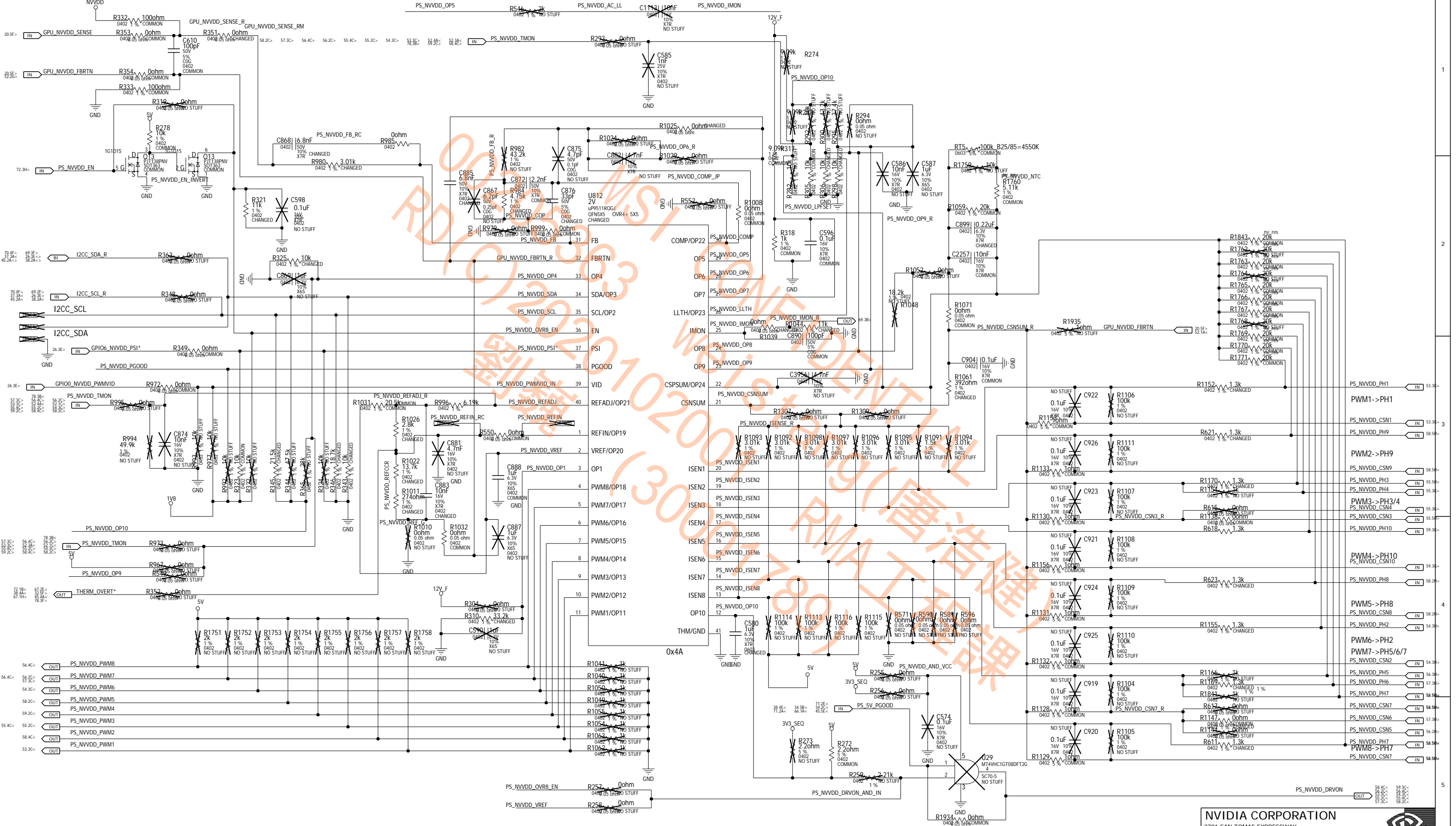
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PS: NVVDD Controller_OVR8



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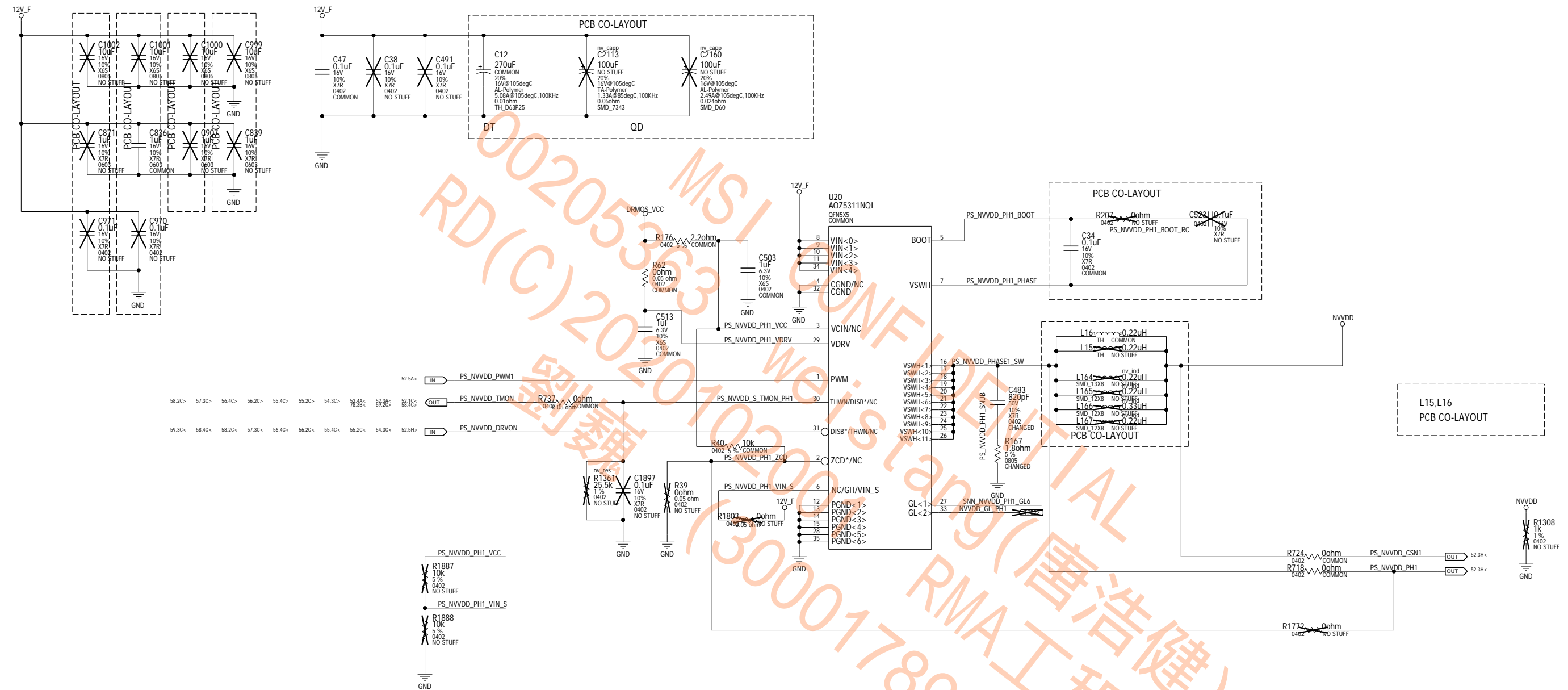
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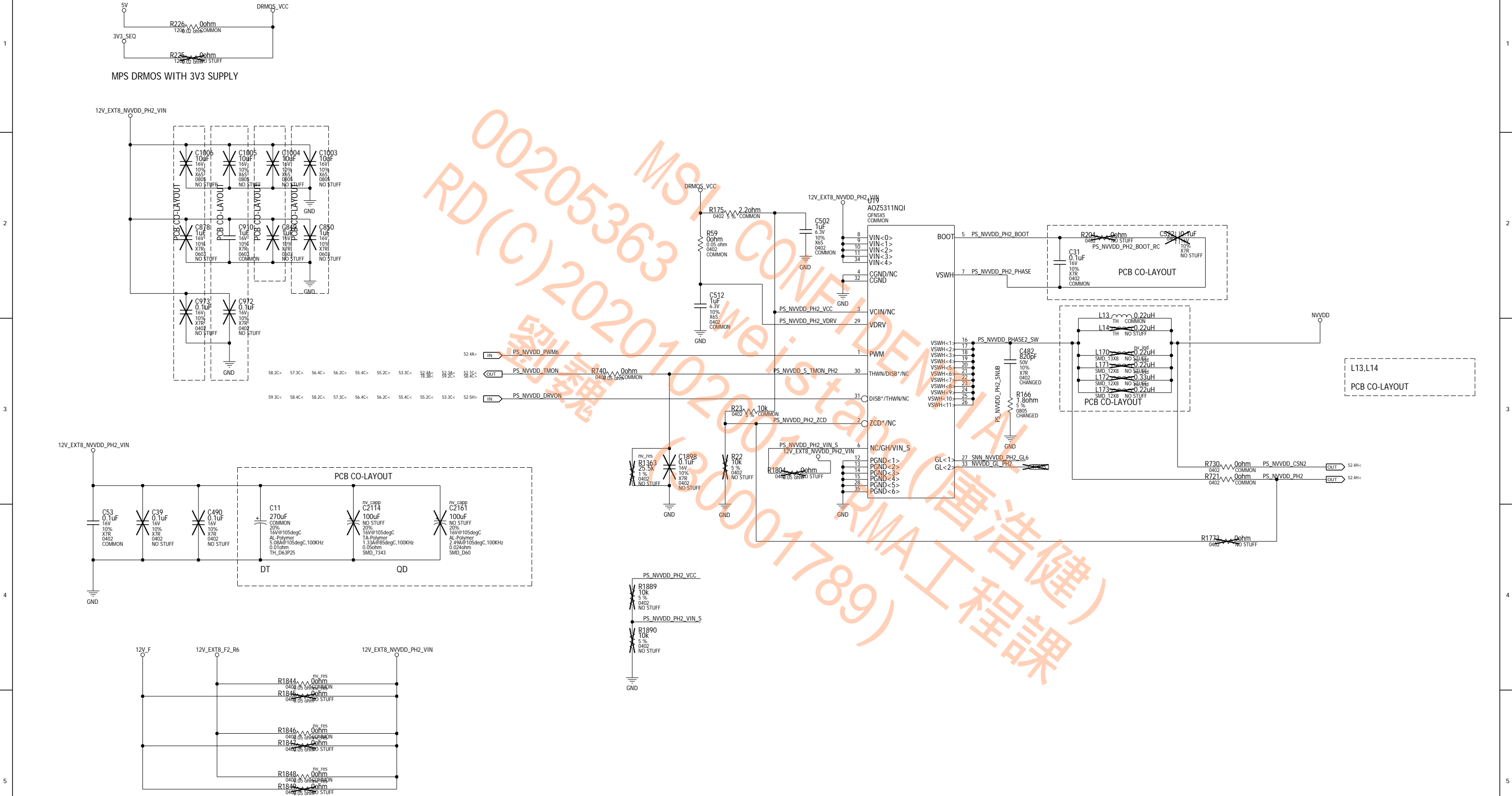
PS: NVVDD Phase 1



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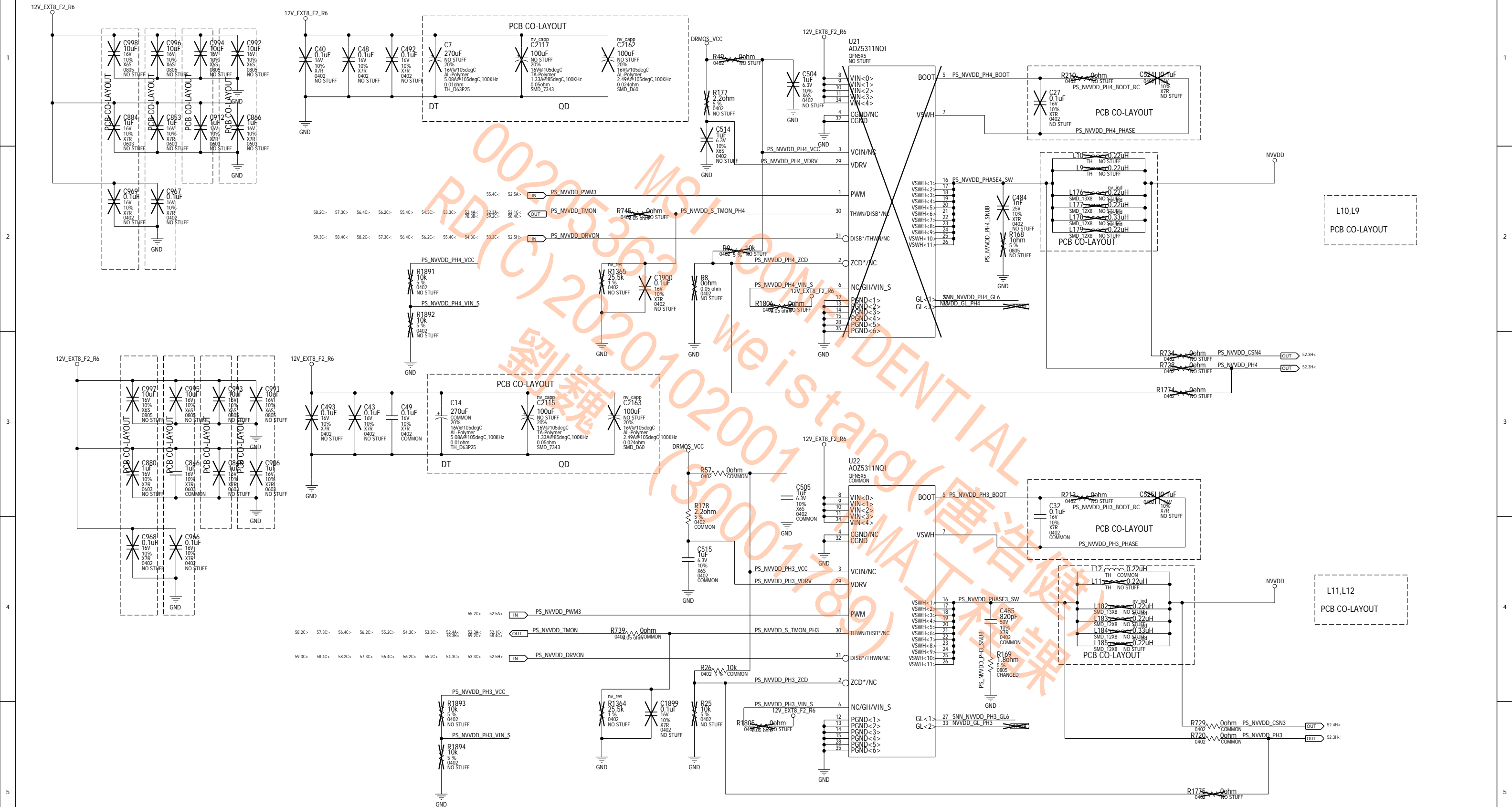
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PS: NVVDD Phase 2



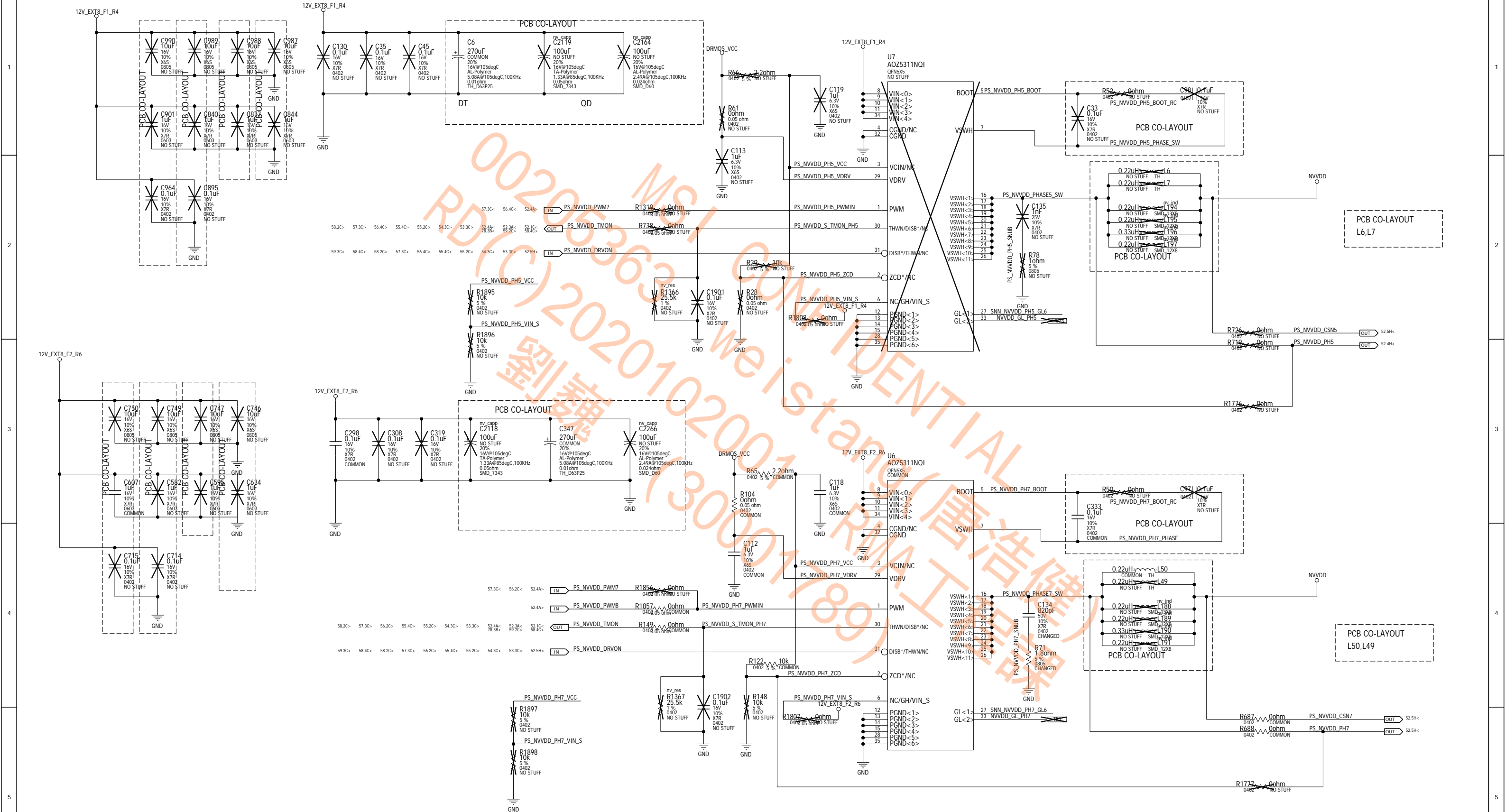
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PS: NVVDD Phase 3 (PWM6), PHASE 4(PWM2)




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PS: NVVDD PH 5(PWM2), PH7(PWM3)

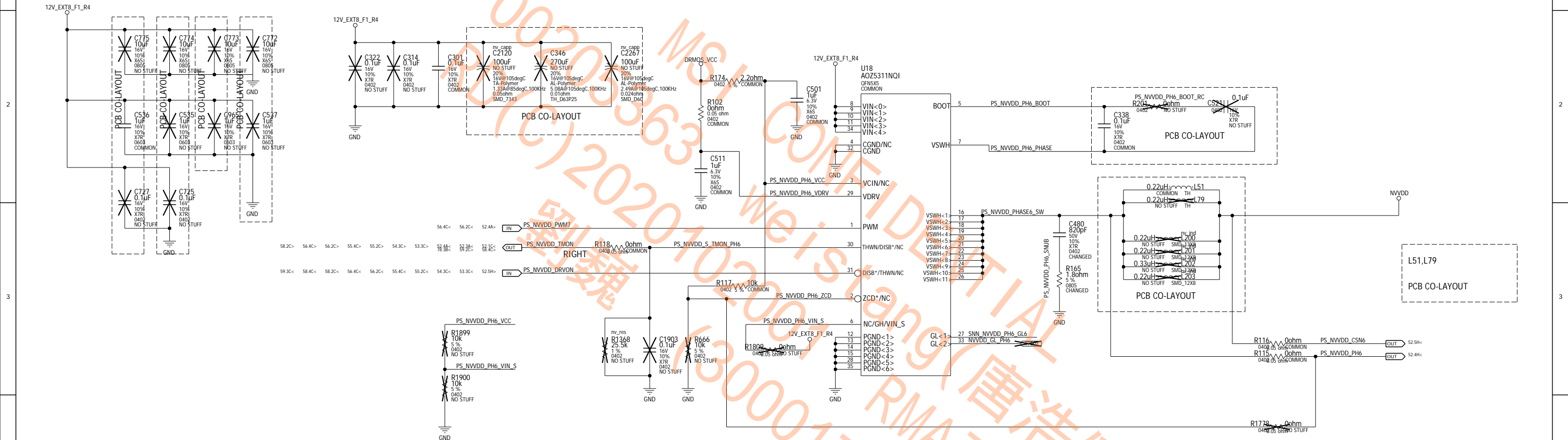


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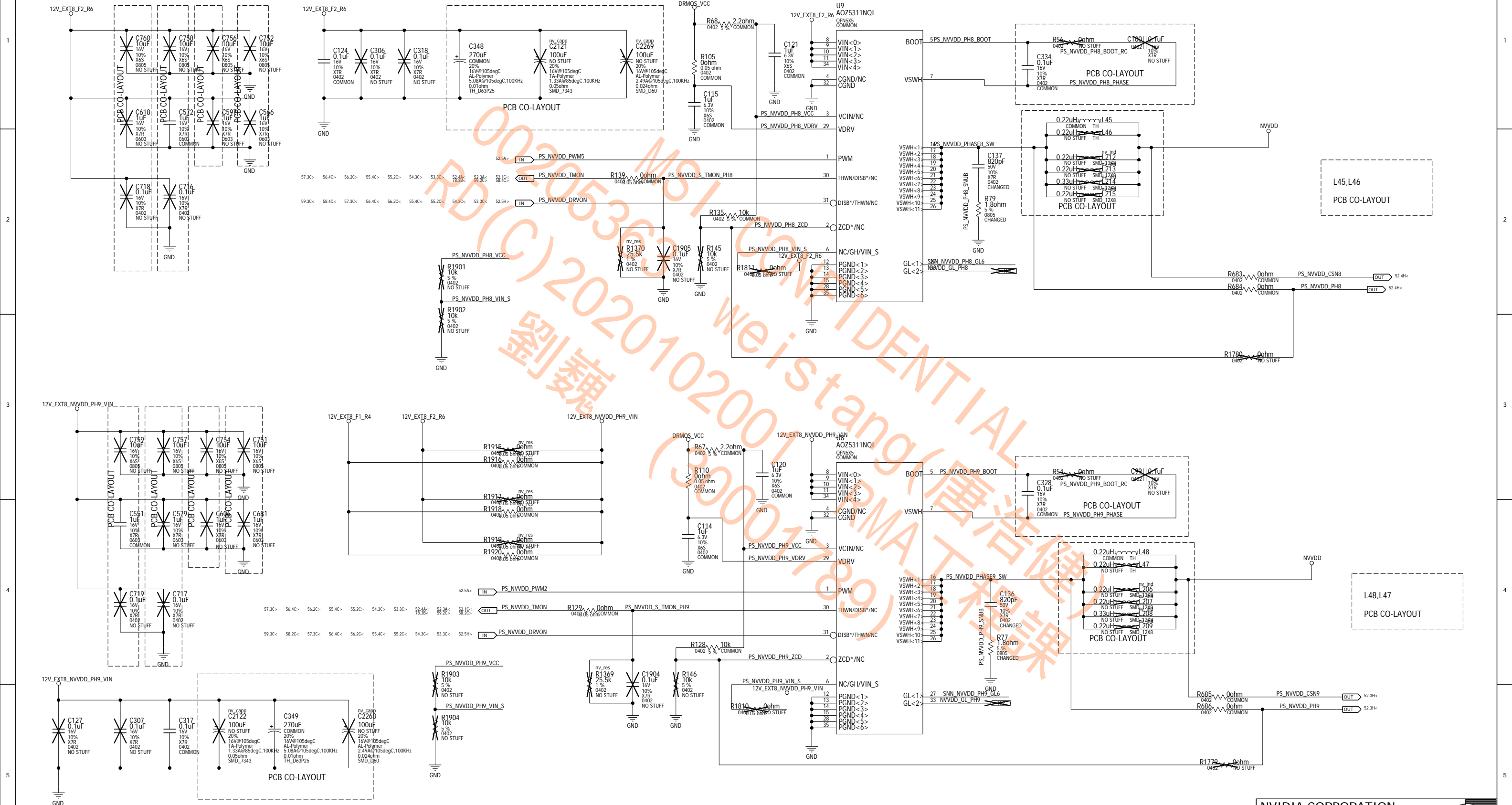
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PS: NVVDD Phase 6(PWM7)

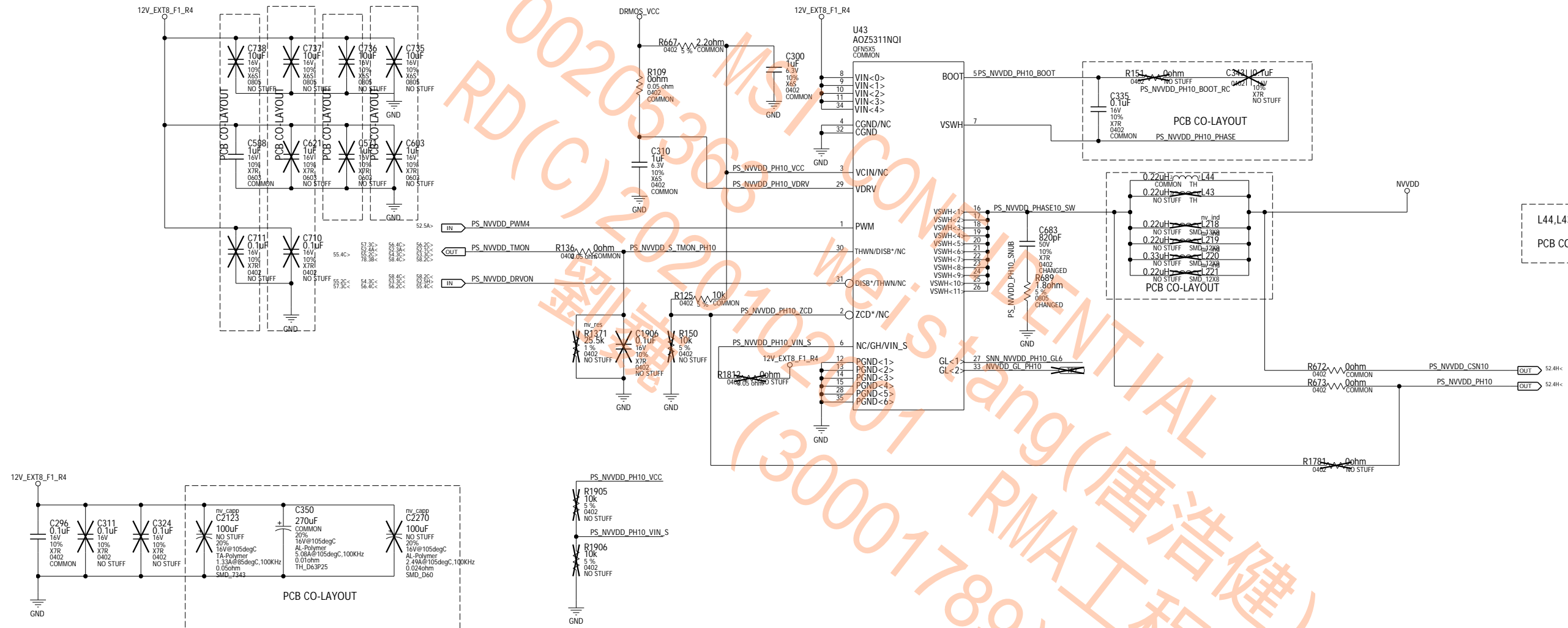


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PS: NVVDD PH 8 (PWM5), PH 9(PWM8)



PS: NVVDD Phase 10 (PWM8)



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PCB CO-LAYOUT
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C163, C164, C166, C167, C2087, C2105, C2109, C2110, C2111, C224, C225, C261, C268, C269, C60354, C61428, C62, C63, C89, C91, C96

PCB CO-LAYOUT

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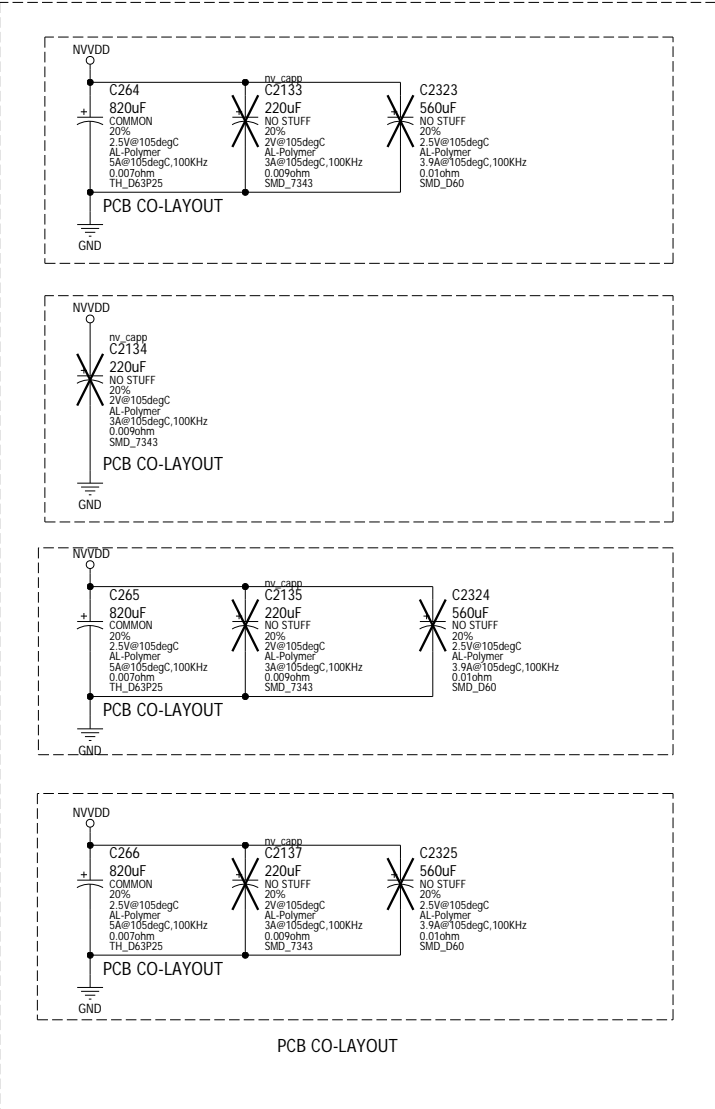
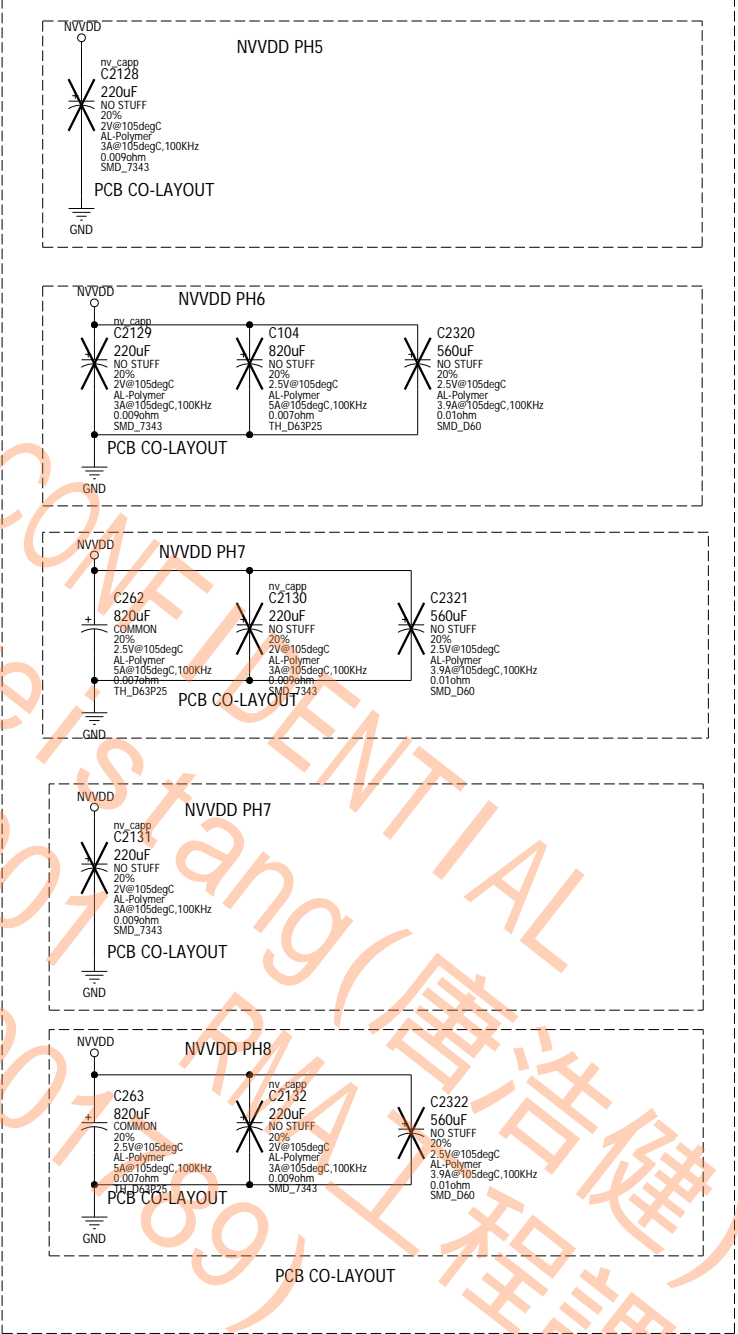
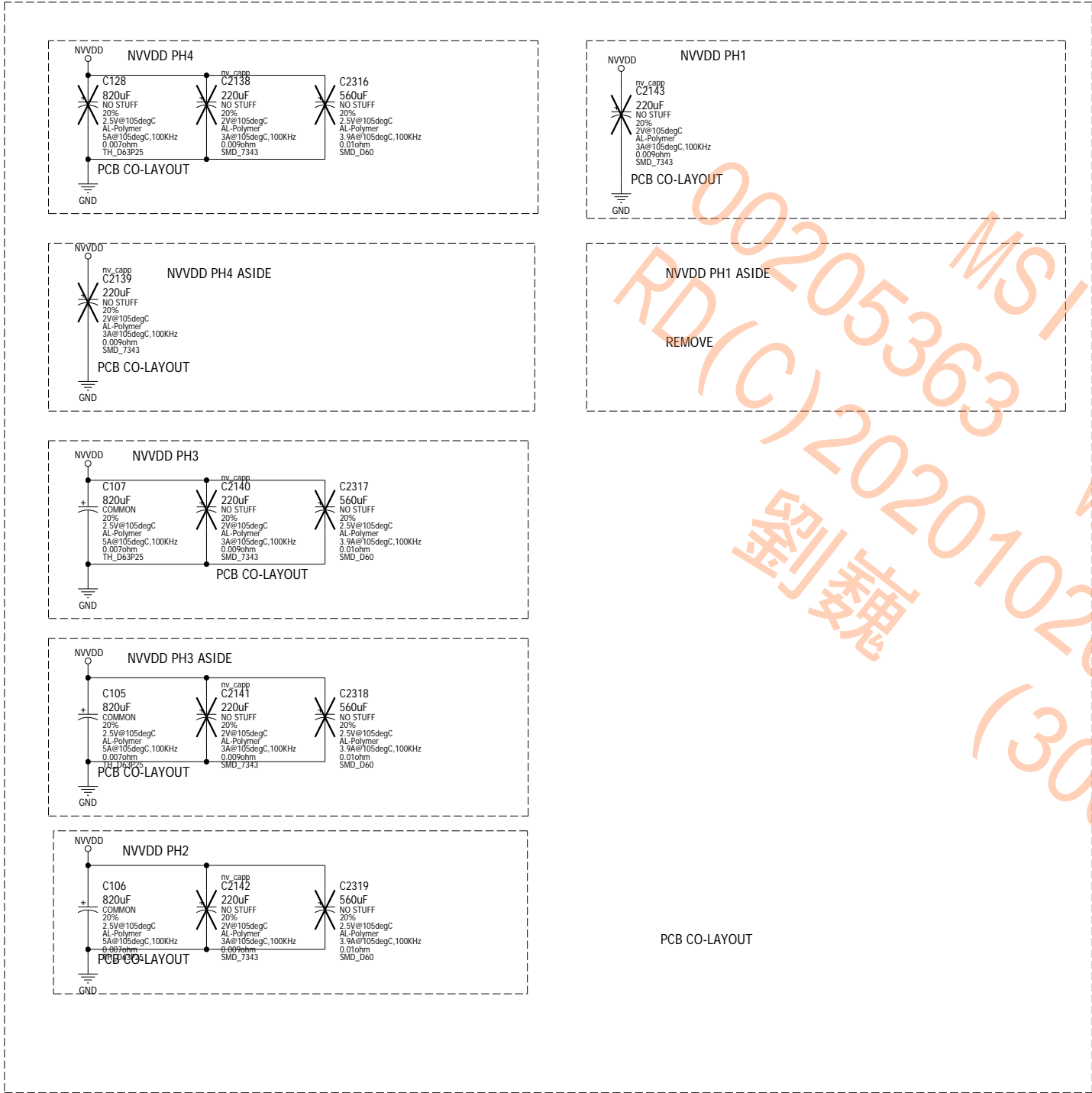
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PS: NVVDD OUTPUT CAP(TOP)



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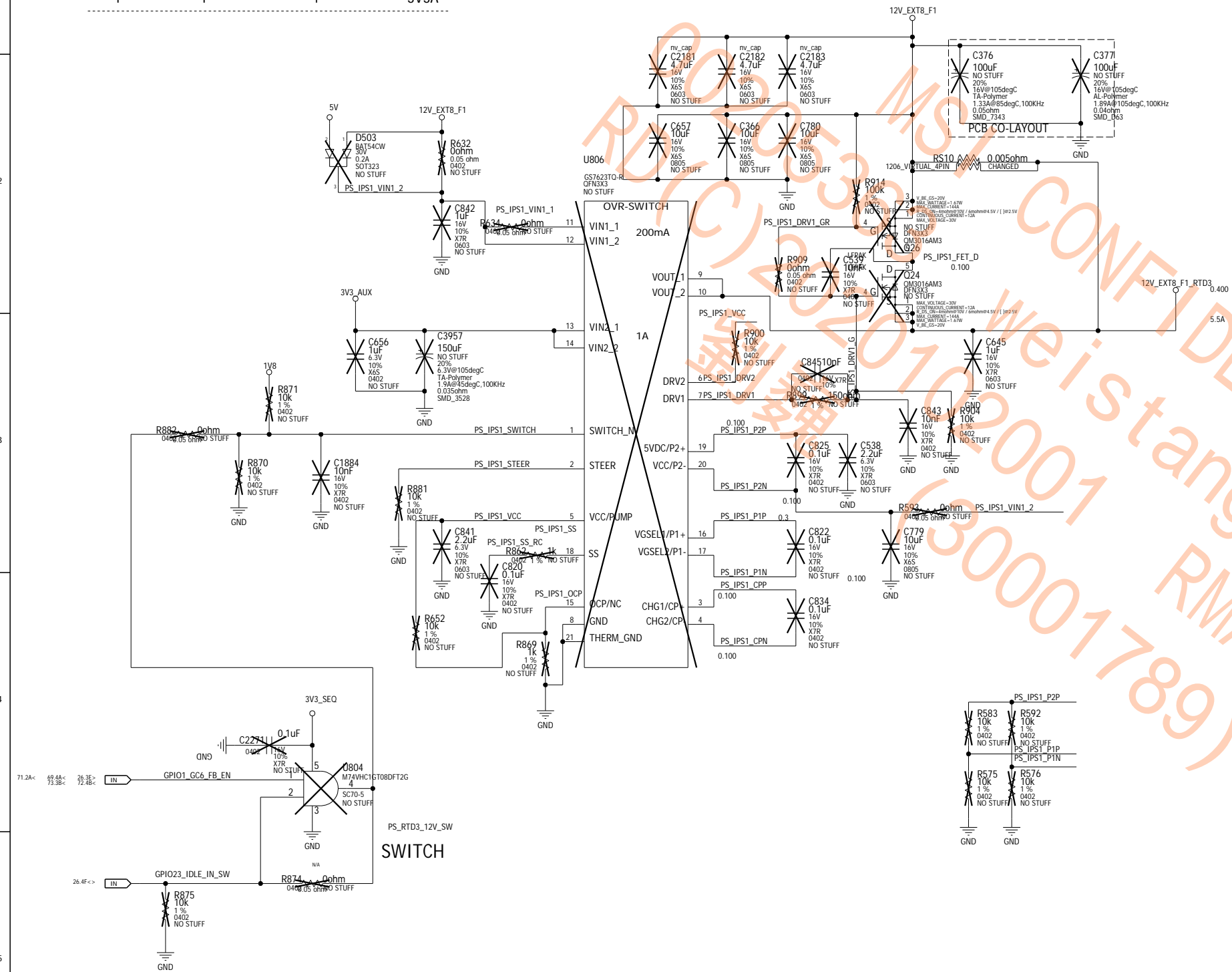


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PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO23	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



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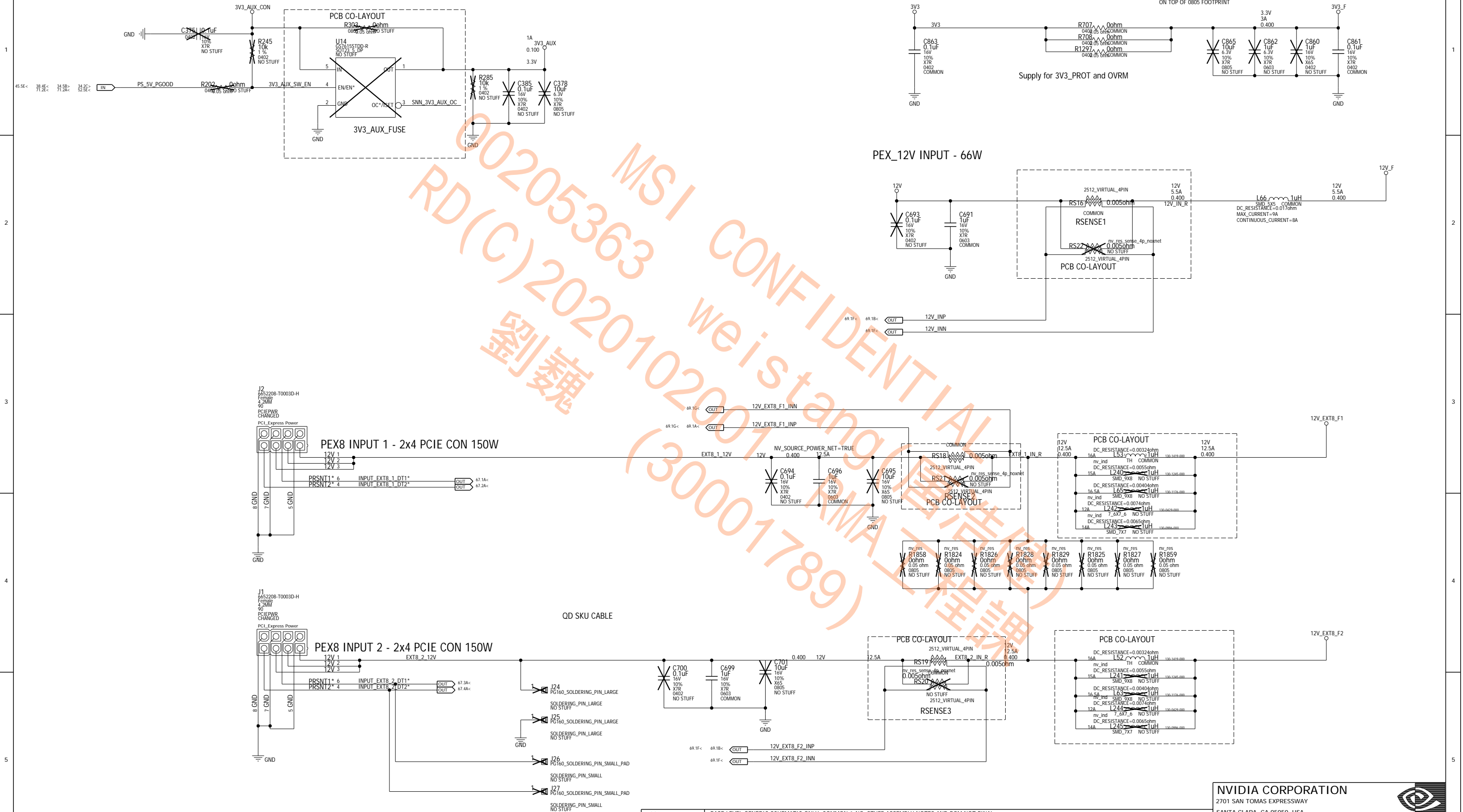
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PS: Inputs, Filtering, and Monitoring

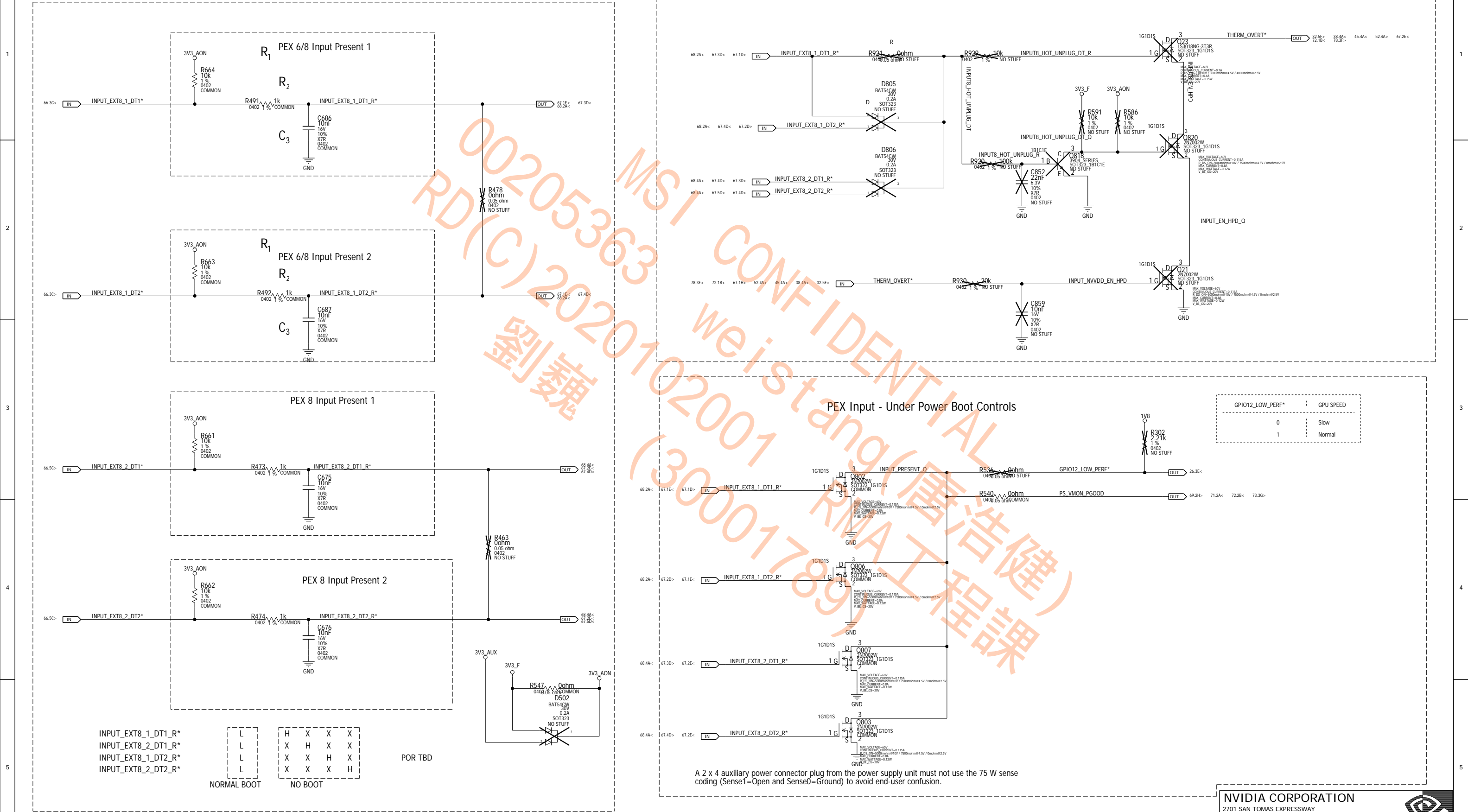


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PAGE DETAIL	PS: INPUTS, FILTERING, and, MONITORING

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PS: 12V Current Steering & Hot Unplug Detect

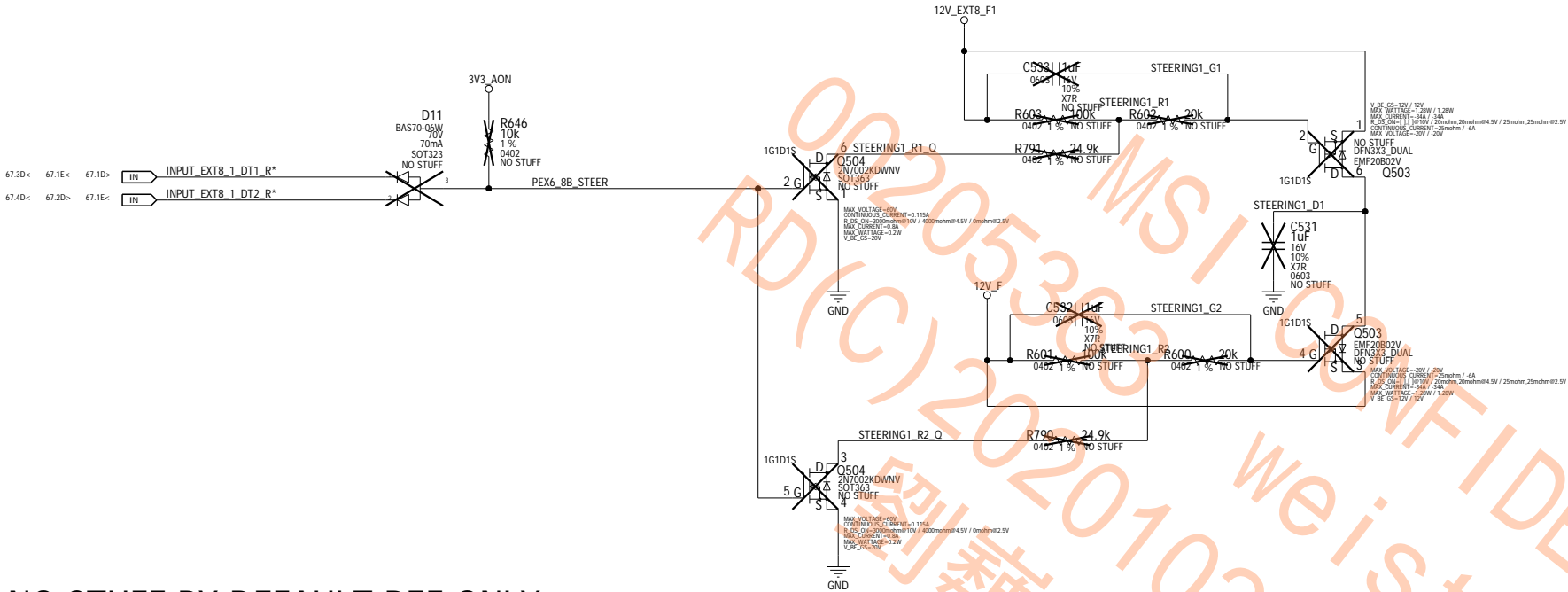


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PS: Discrete Steering

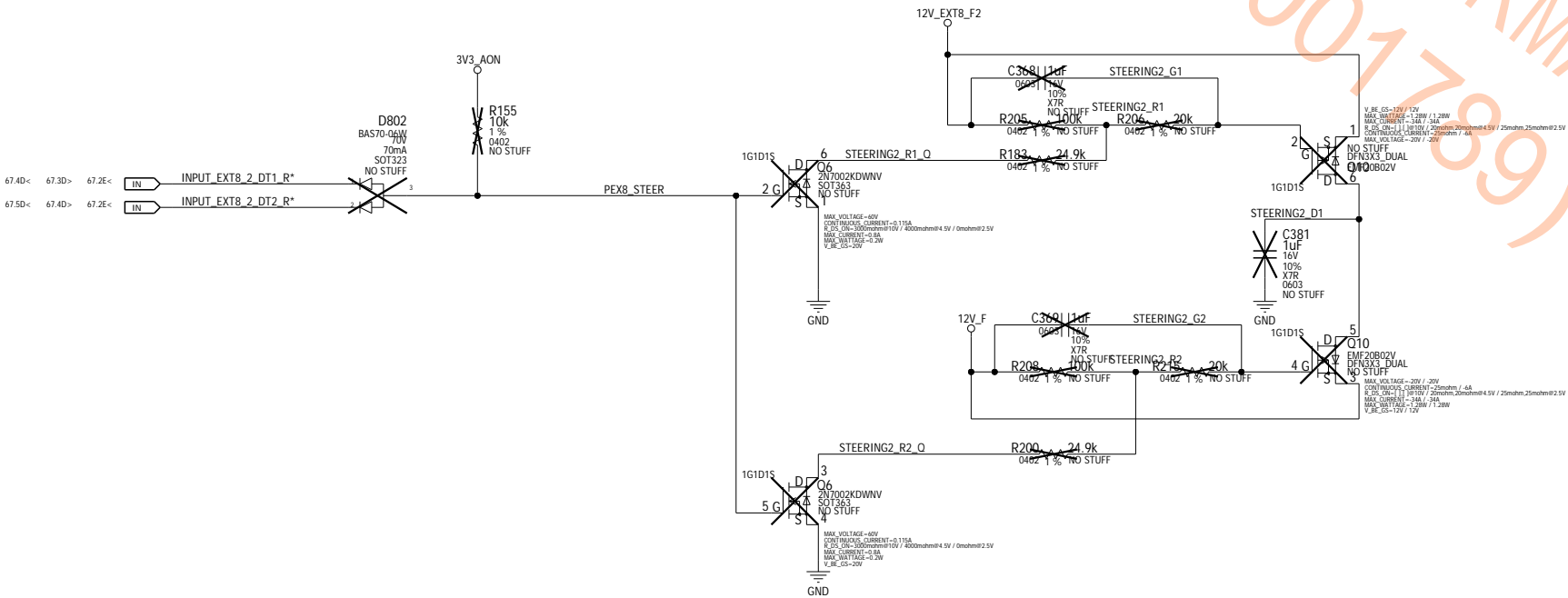
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1

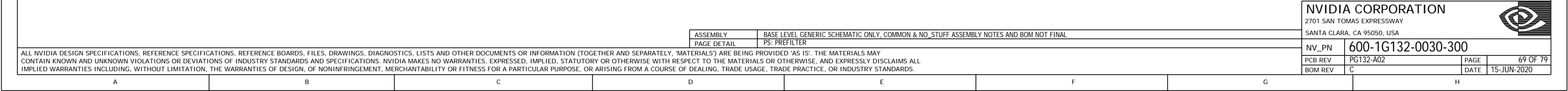


NO STUFF BY DEFAULT REF ONLY

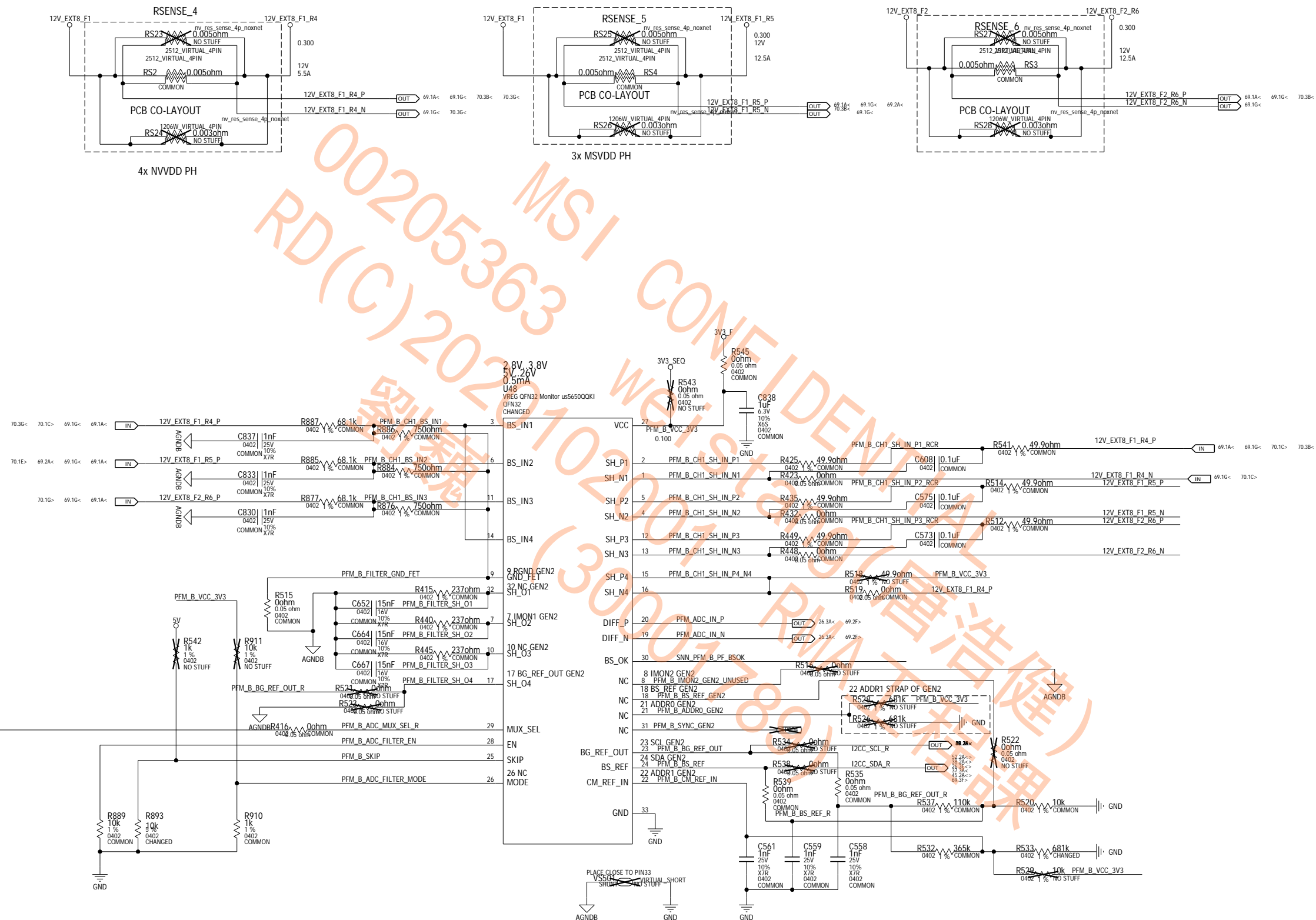
PEX12V AND 12V_EXT8_F2



Route the trace to PEX Golden Finger



PS: Pre-Filter B



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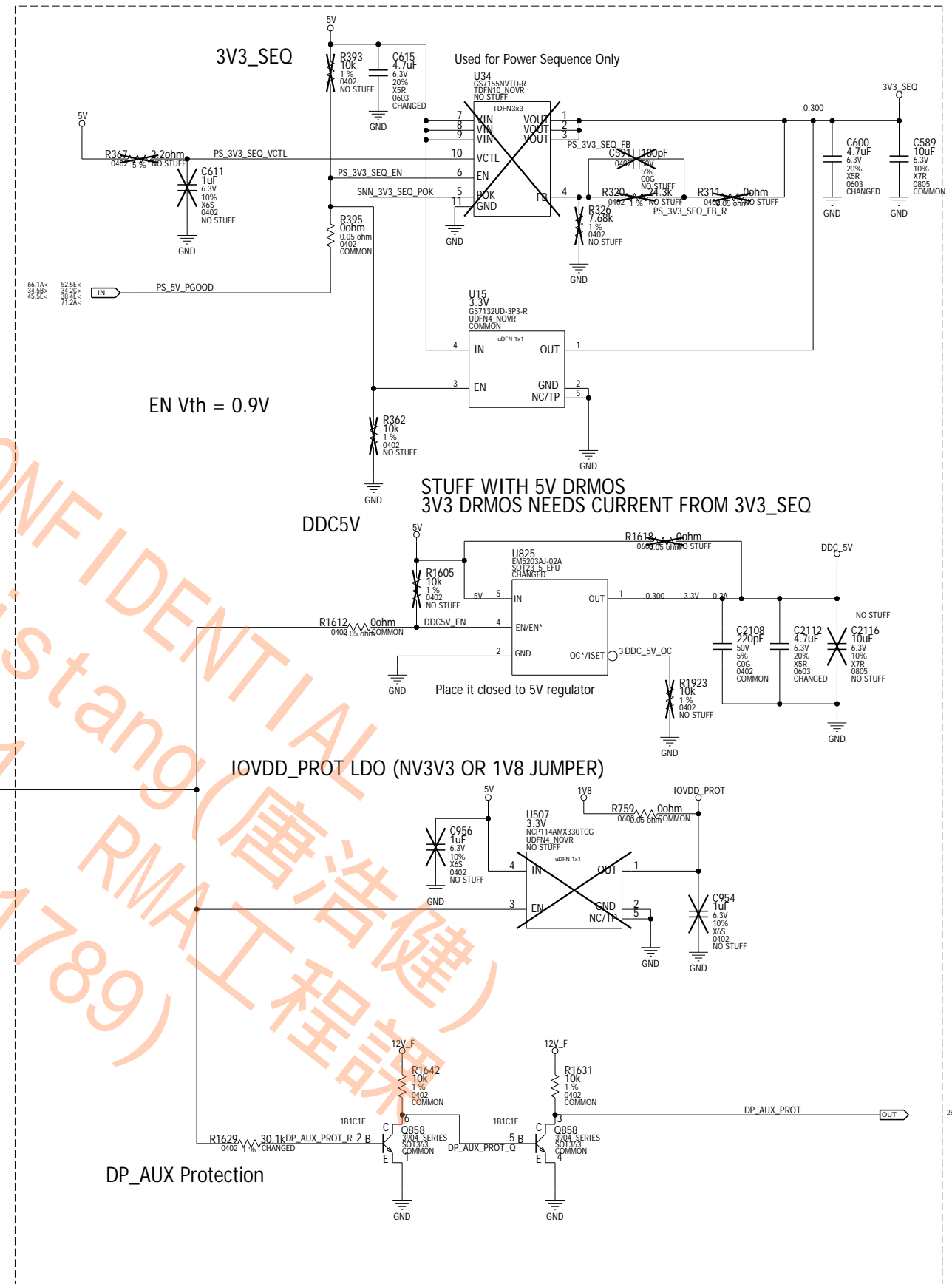
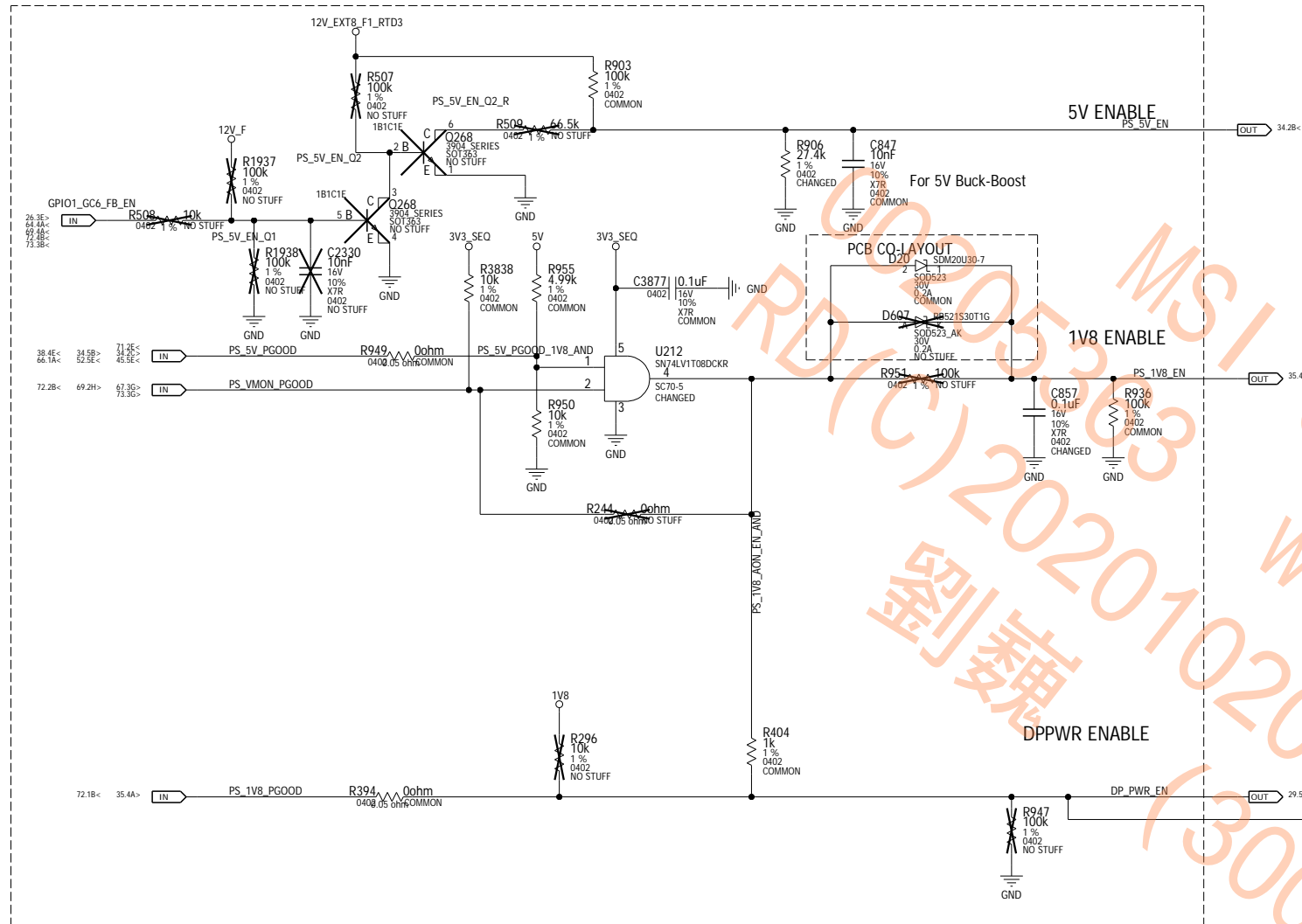
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SEQUENCE:5V,1V8,3V3_SEQ ENABLE



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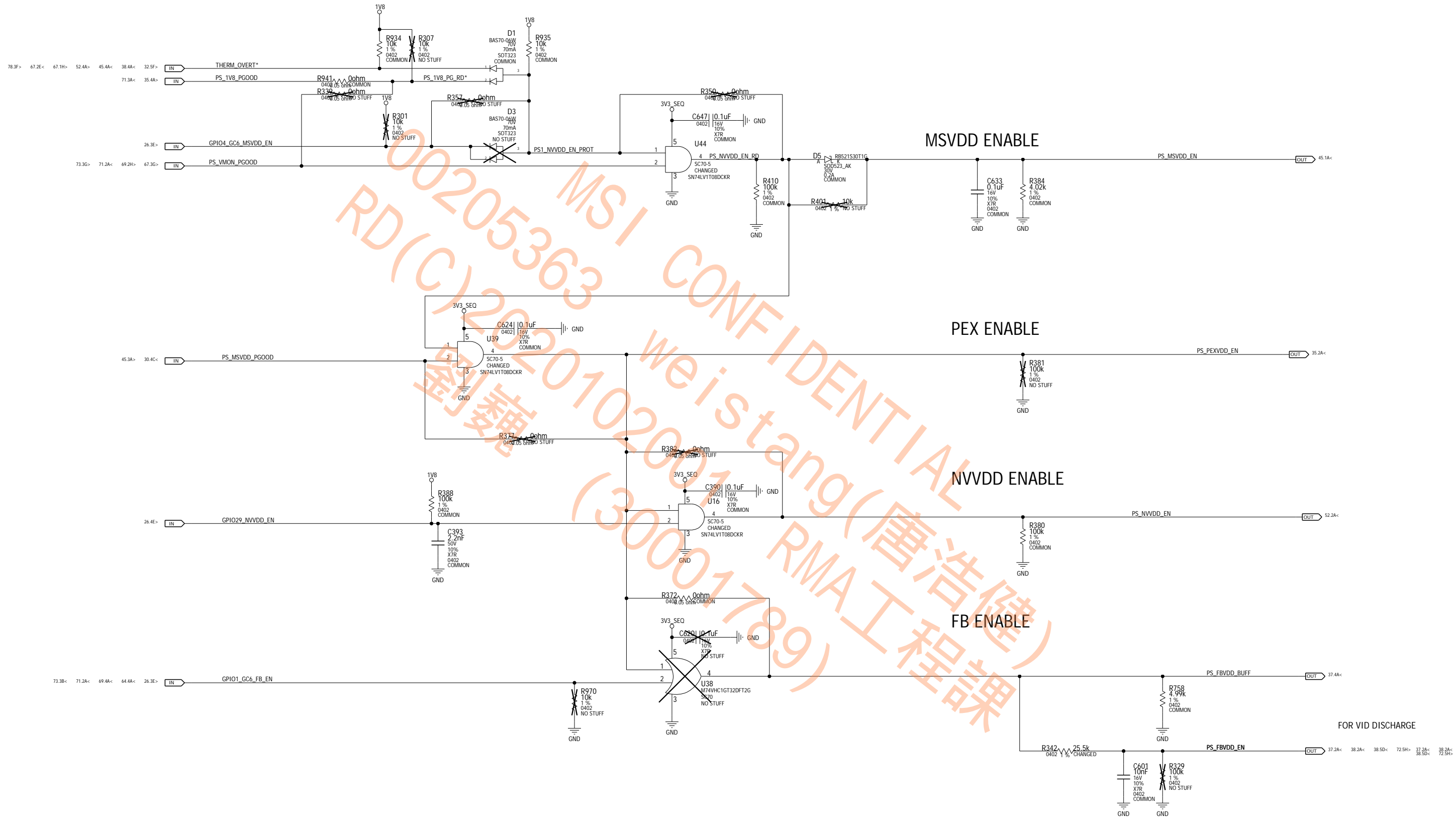
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SEQUENCE:NV,PEX,FB ENABLE



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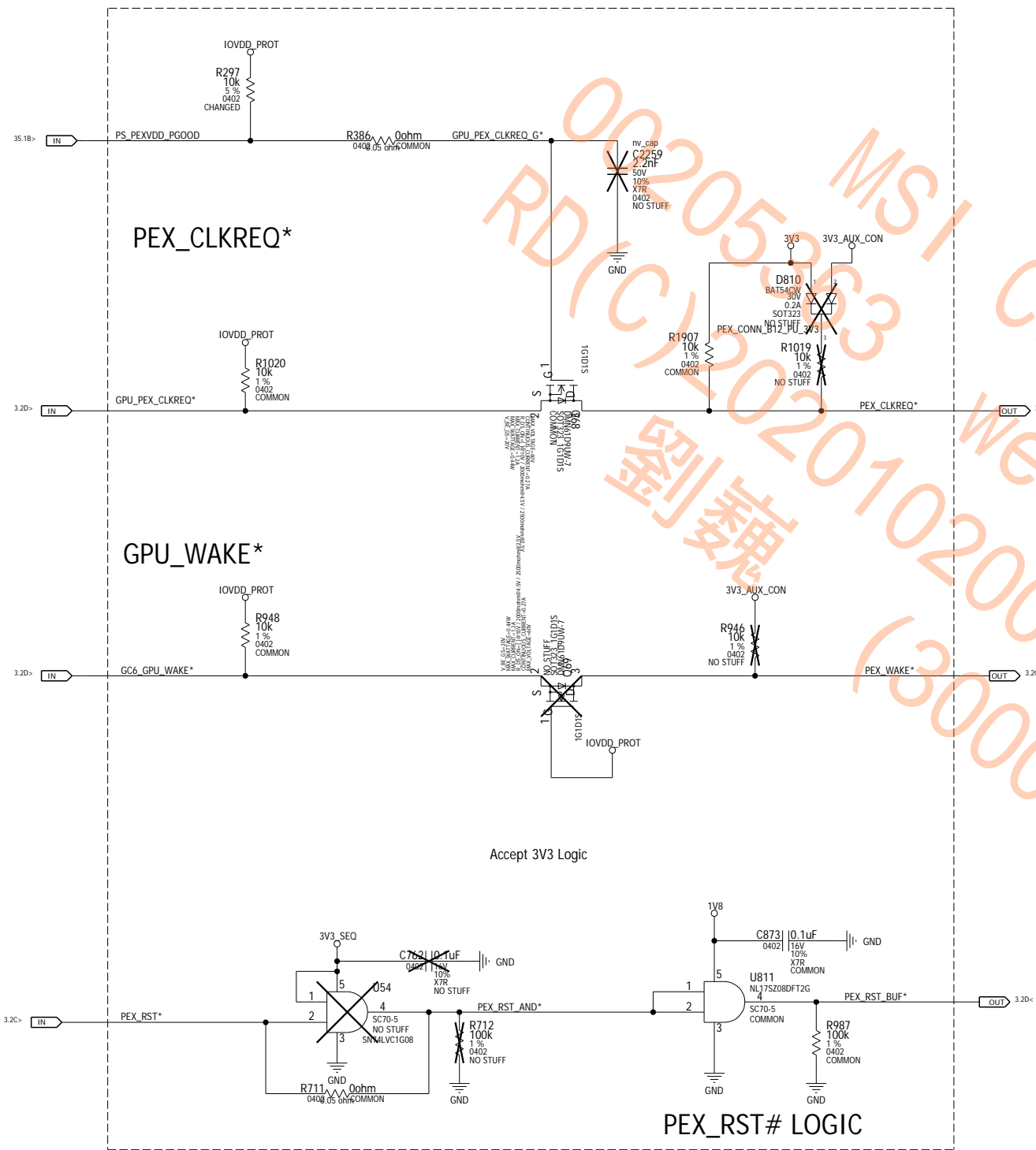
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SEQUENCE:MISC

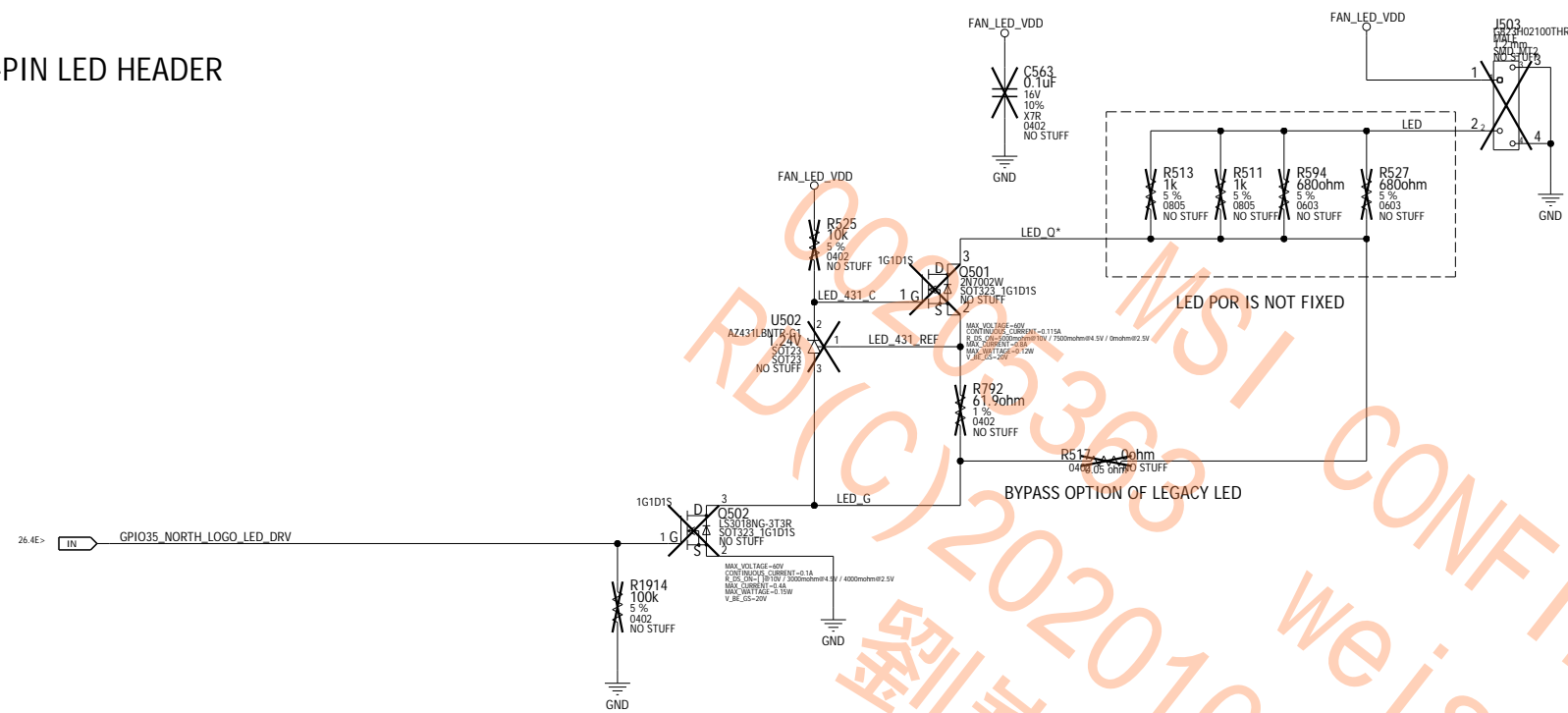


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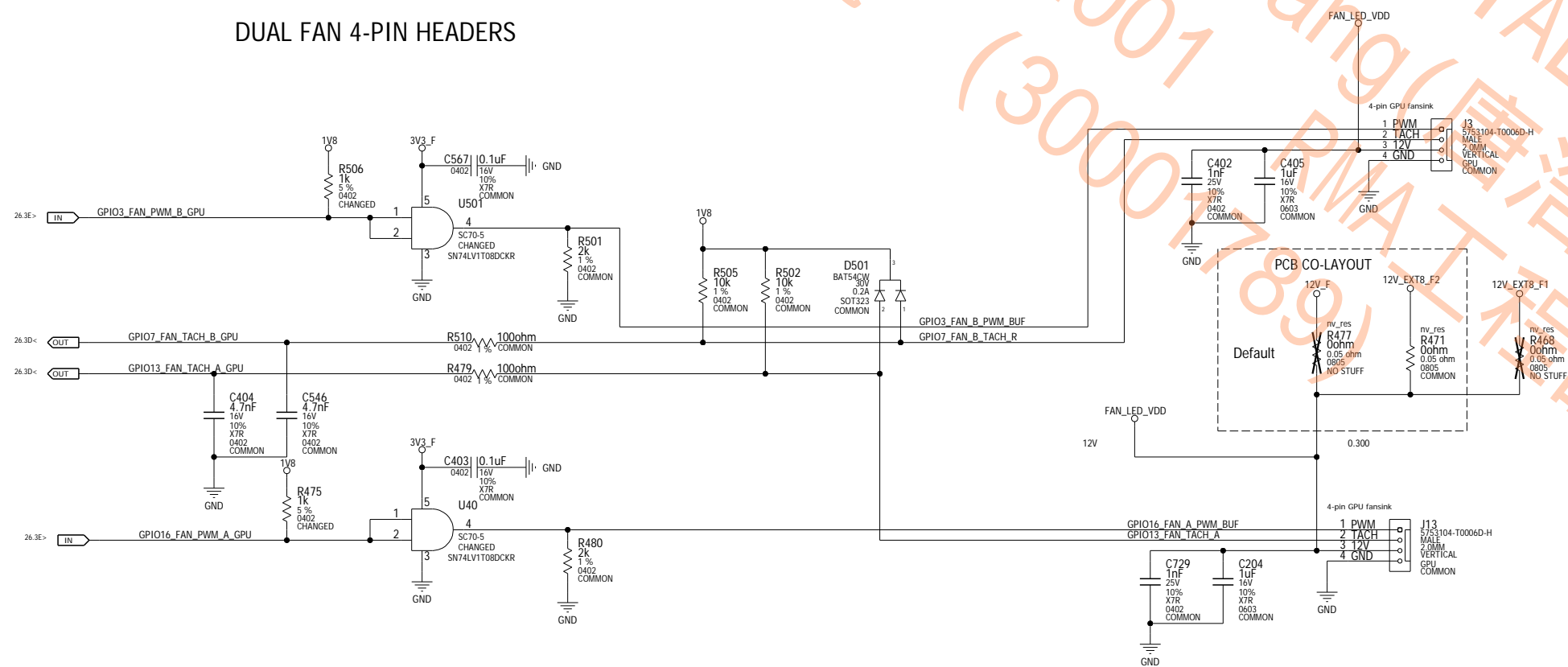
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MISC: LED & FAN

2-PIN LED HEADER



DUAL FAN 4-PIN HEADERS



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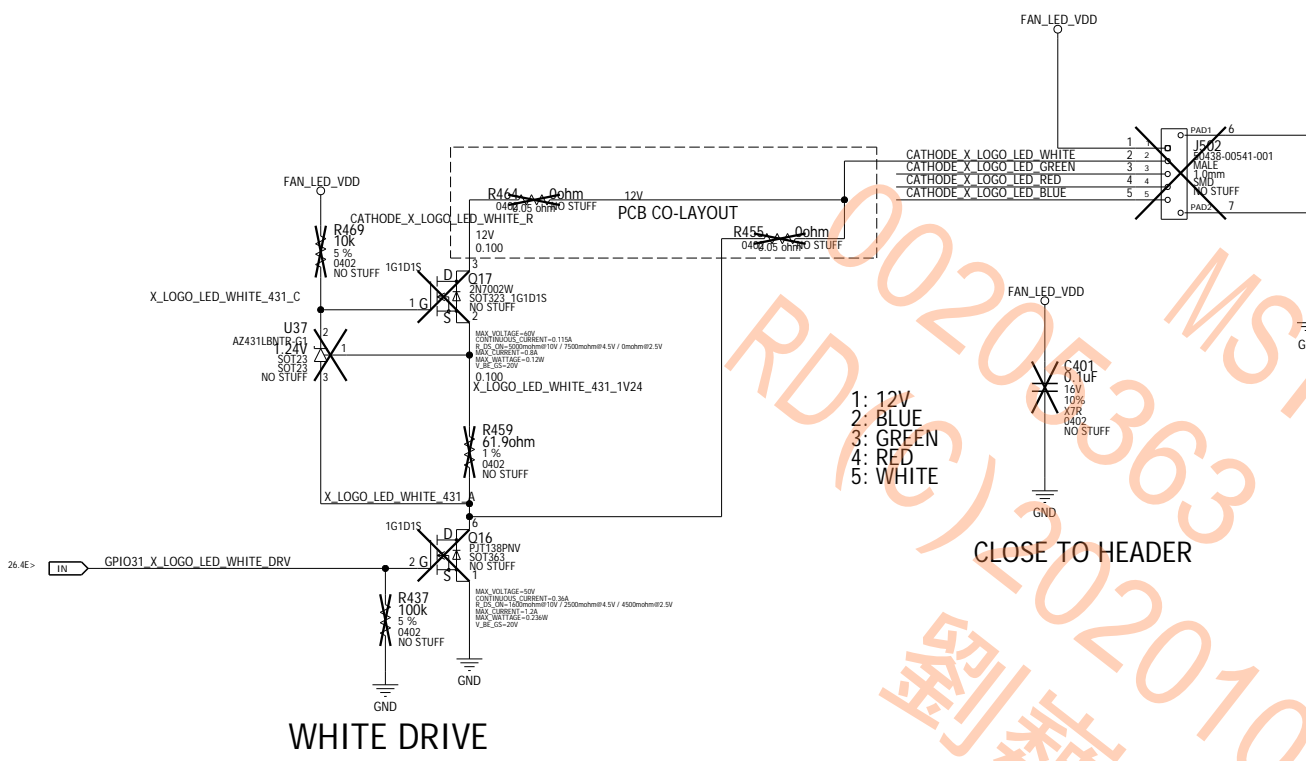
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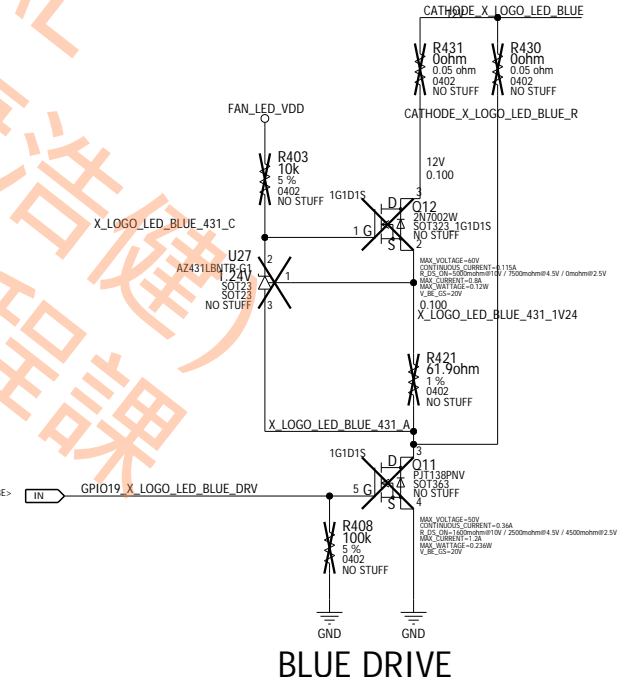
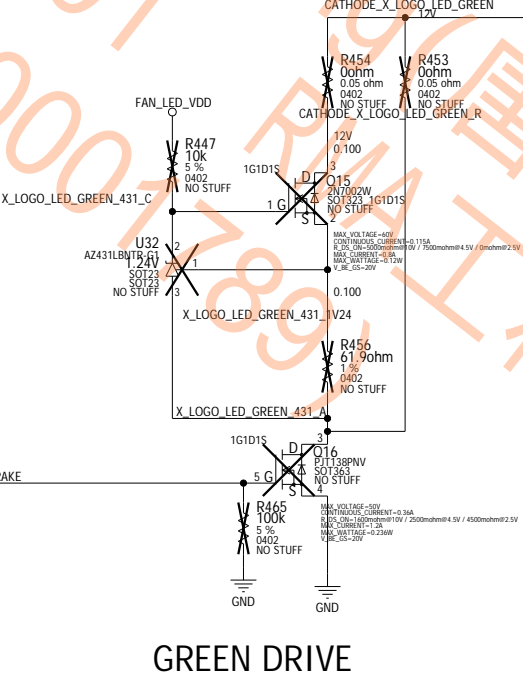
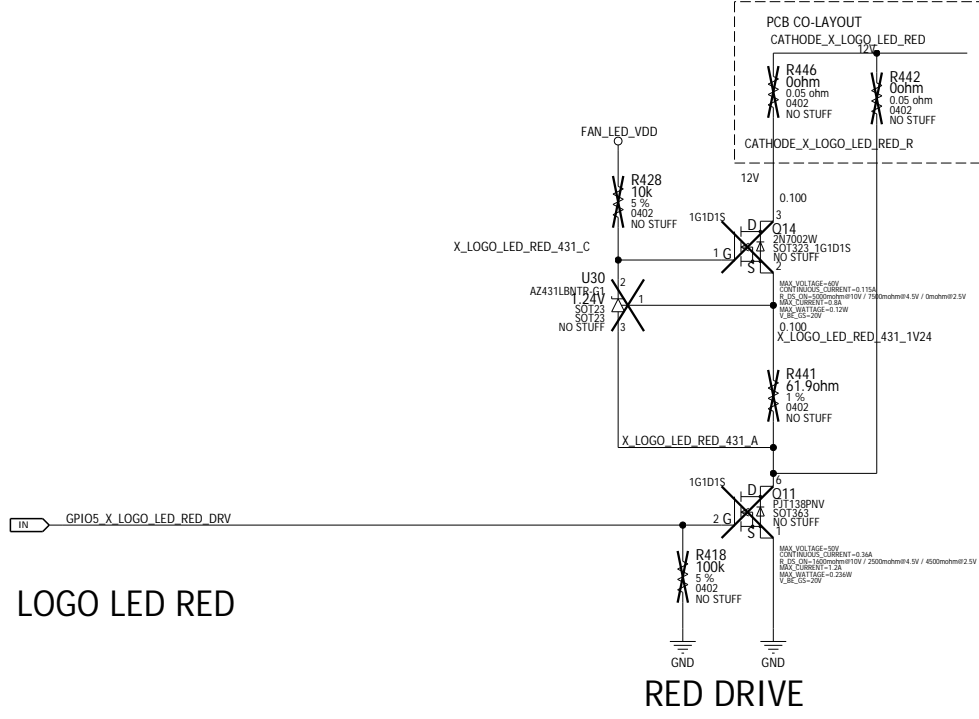
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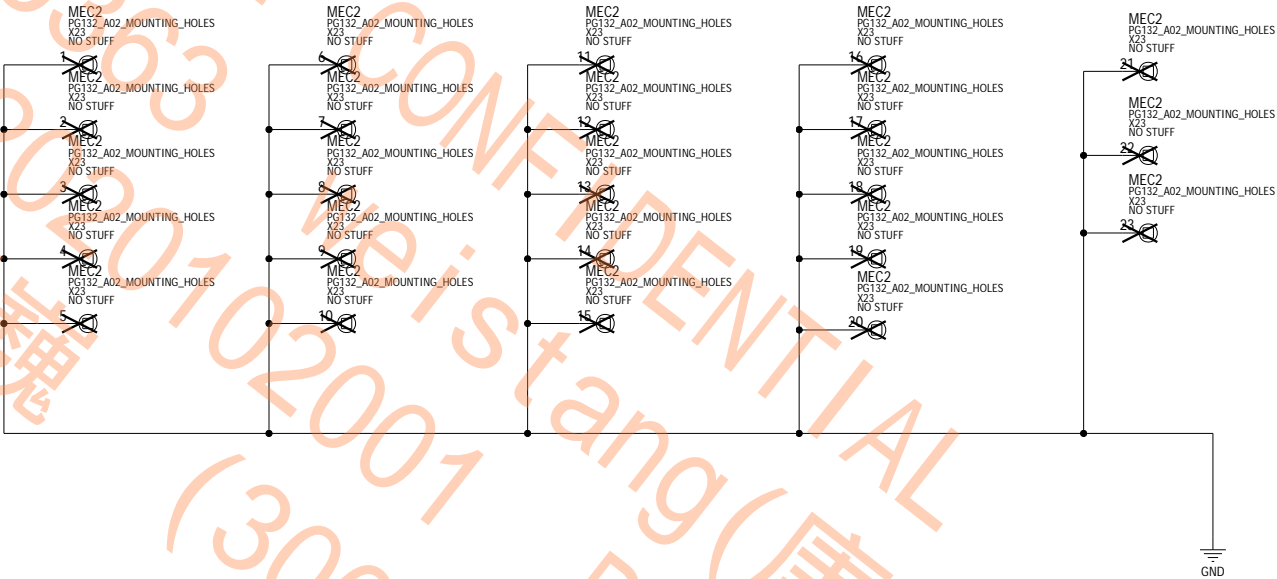
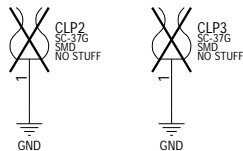
MISC: RGBW LED REF



CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALINGN WITH PASH
IF ADDITIONAL POWER CONSUPTION R
NEEDED, IT SHOULD BE ON LED MOD.

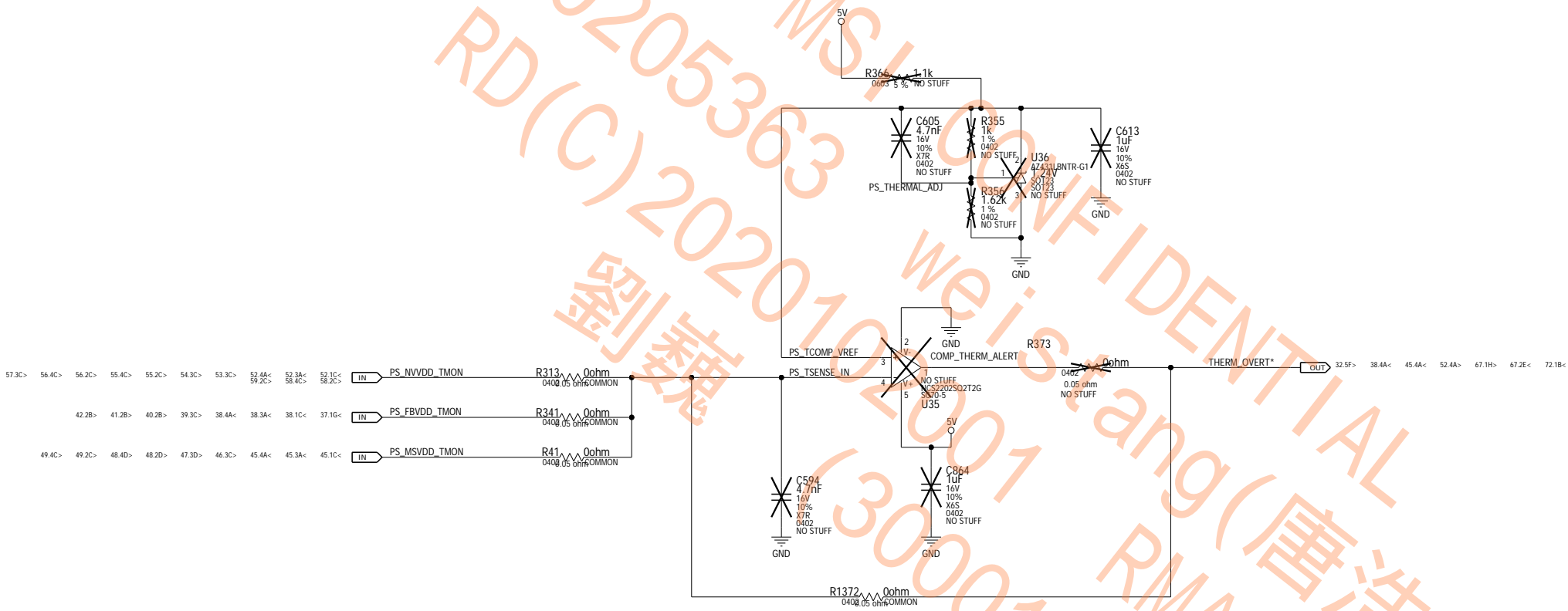


Mechanical: Mounting holes



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