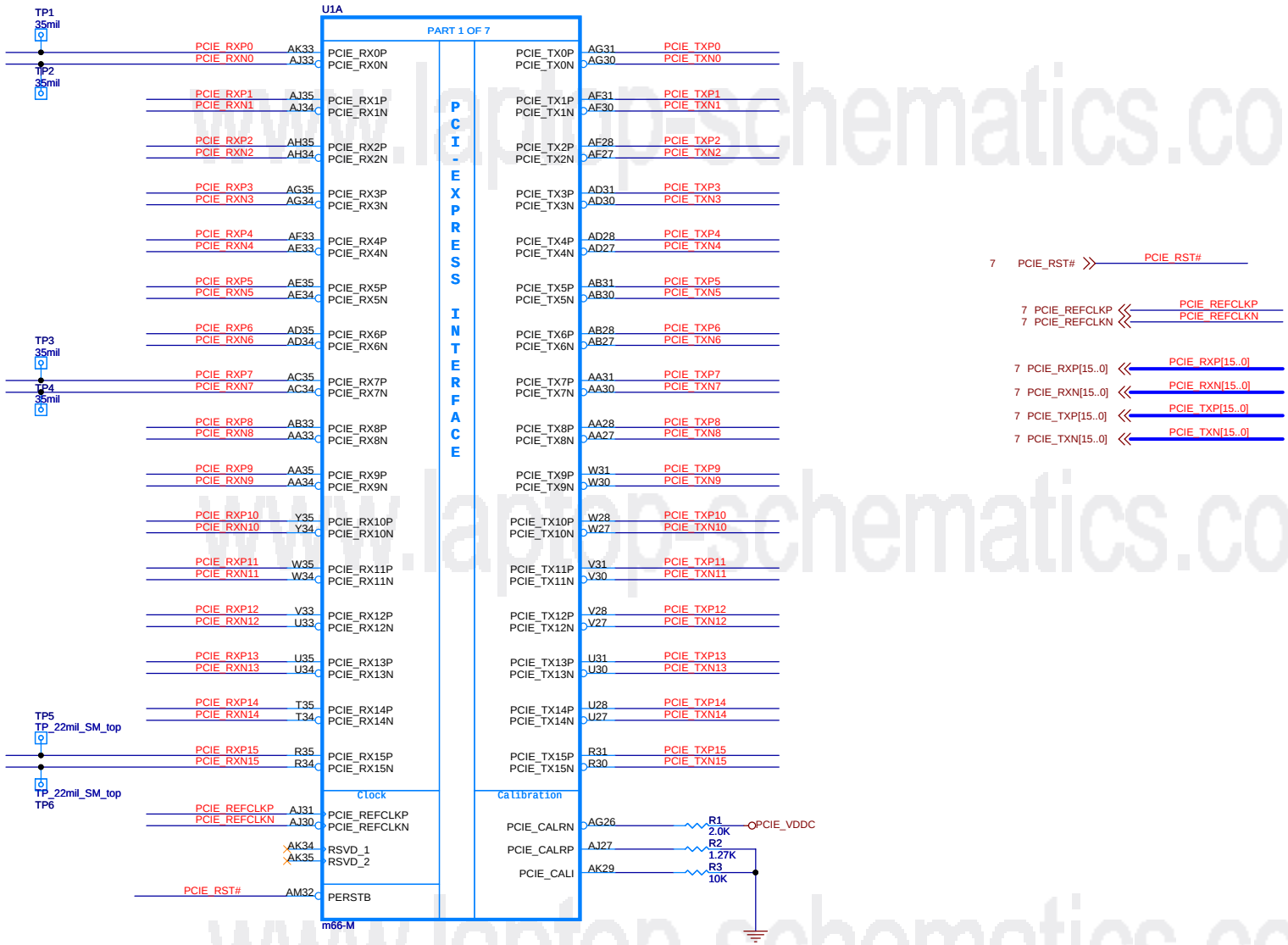

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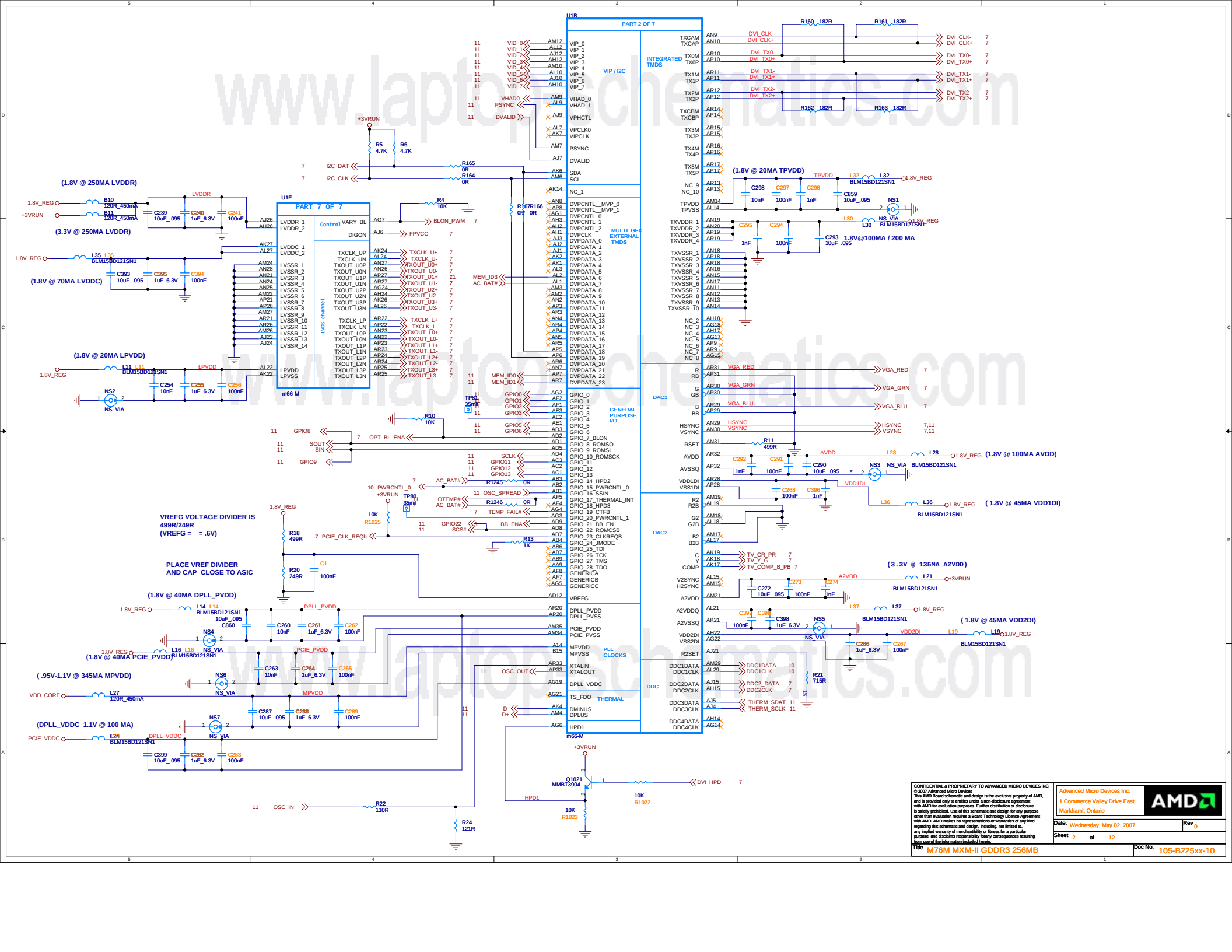
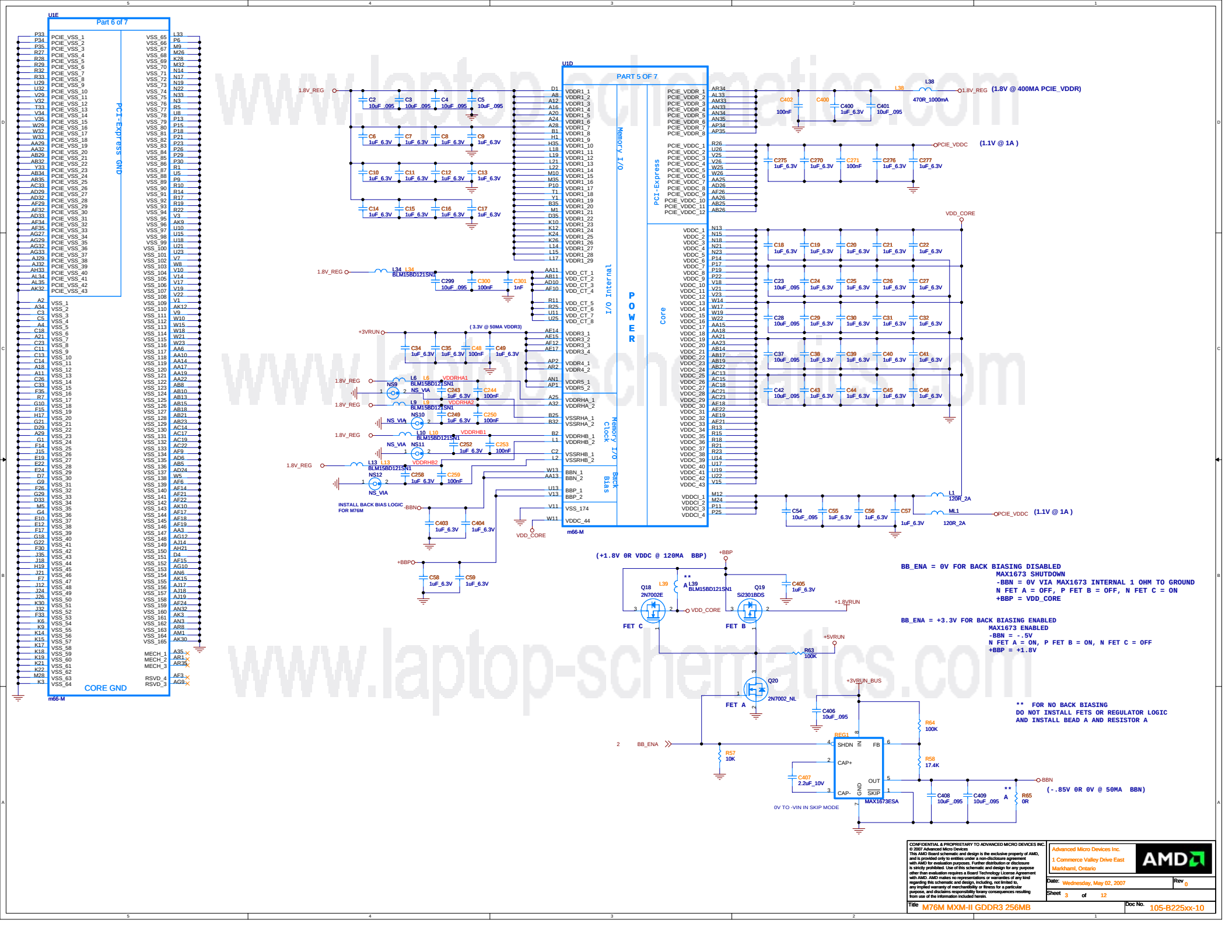
Date:	Wednesday, May 02, 2007
Rev	0
Sheet	1 of 12
Title	M76M MXM-II GDDR3 256MB
Doc No.	105-B225xx-10





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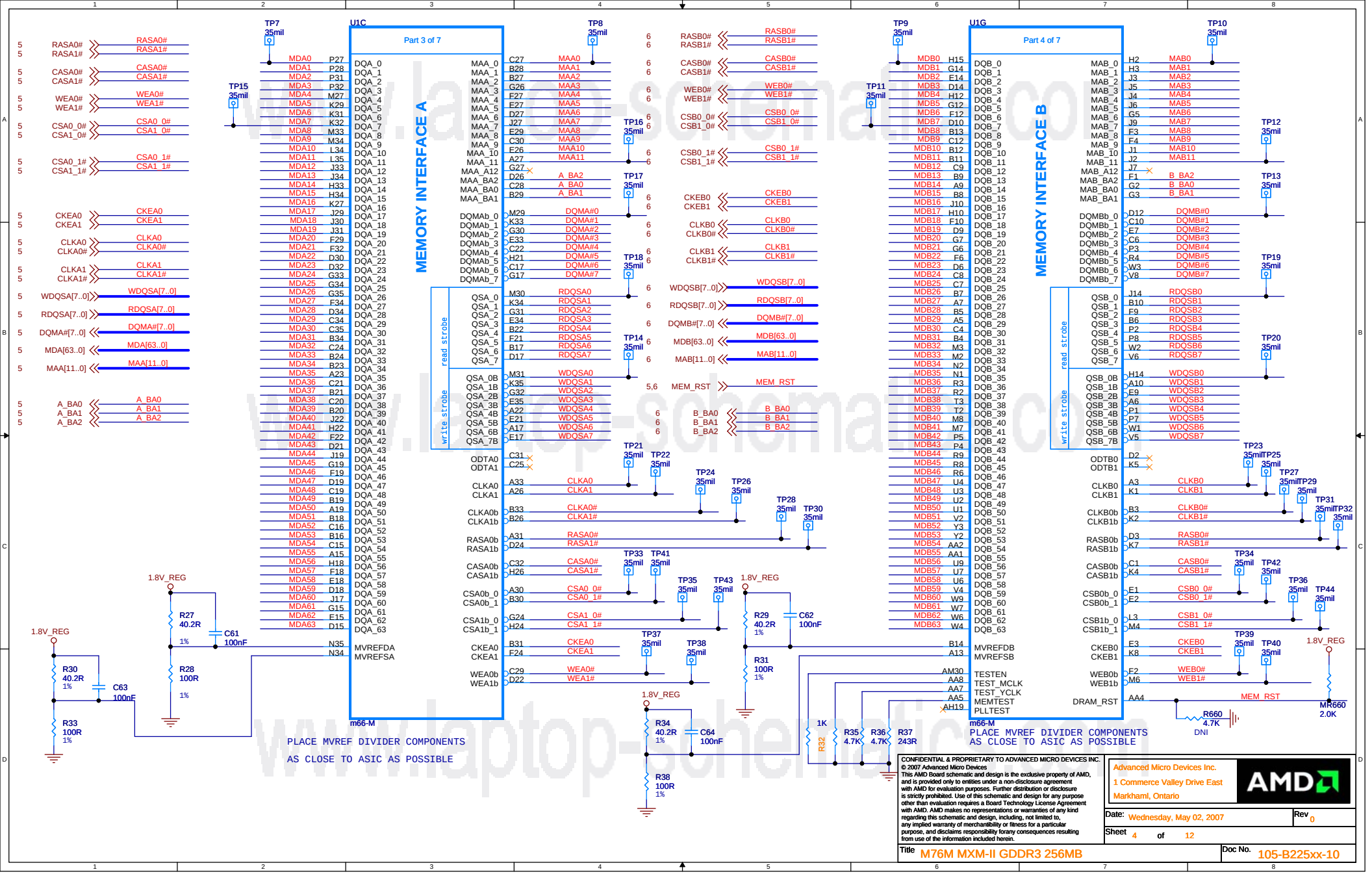
Date:	Wednesday, May 02, 2007
Rev	0
Sheet	3 of 12
Title	M76M MXM-II GDDR3 256MB
Doc No.	105-B225xx-10



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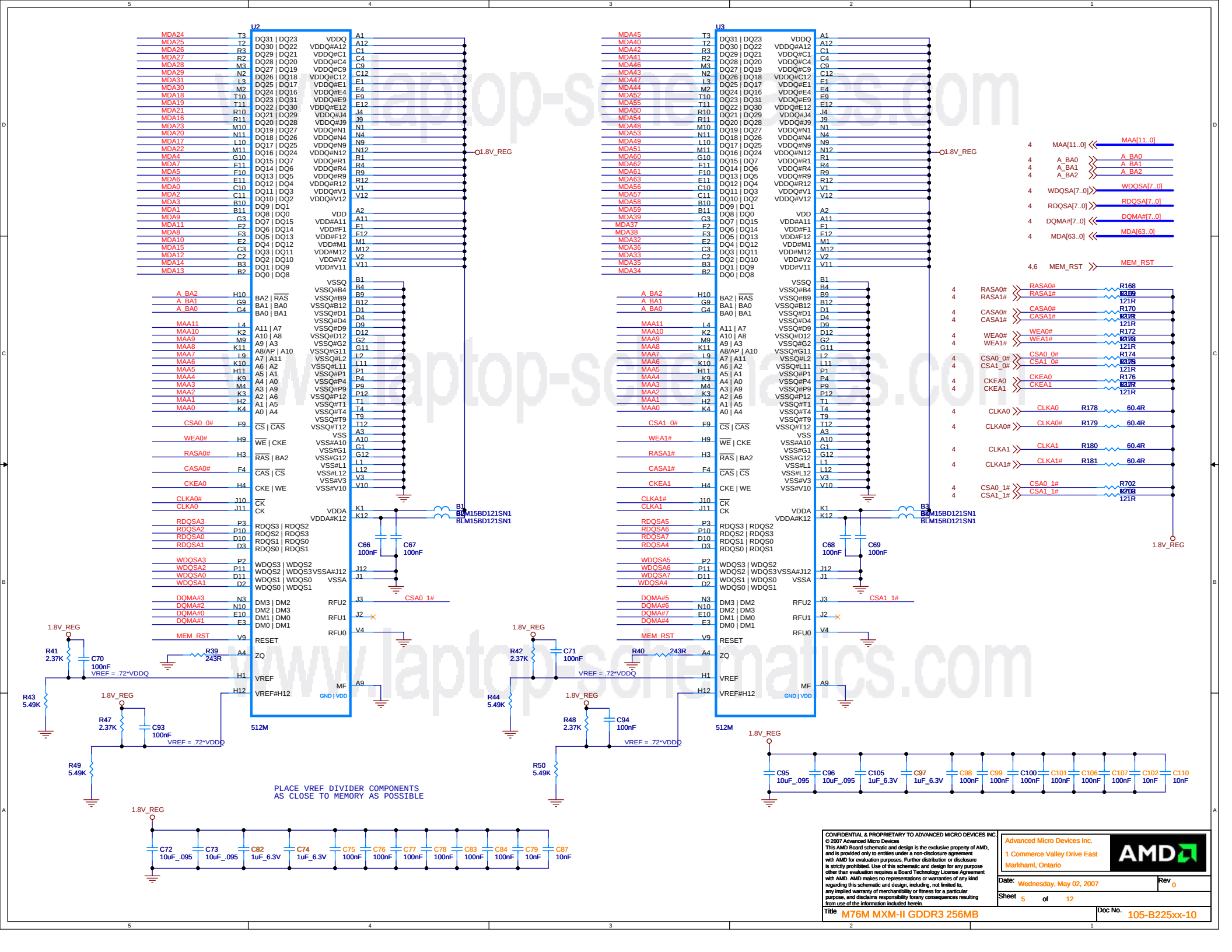
Date: Wednesday, May 02, 2007 Rev 0

Sheet 4 of 12

Title M76M MXM-II GDDR3 256MB

Doc No. 105-B225xx-10



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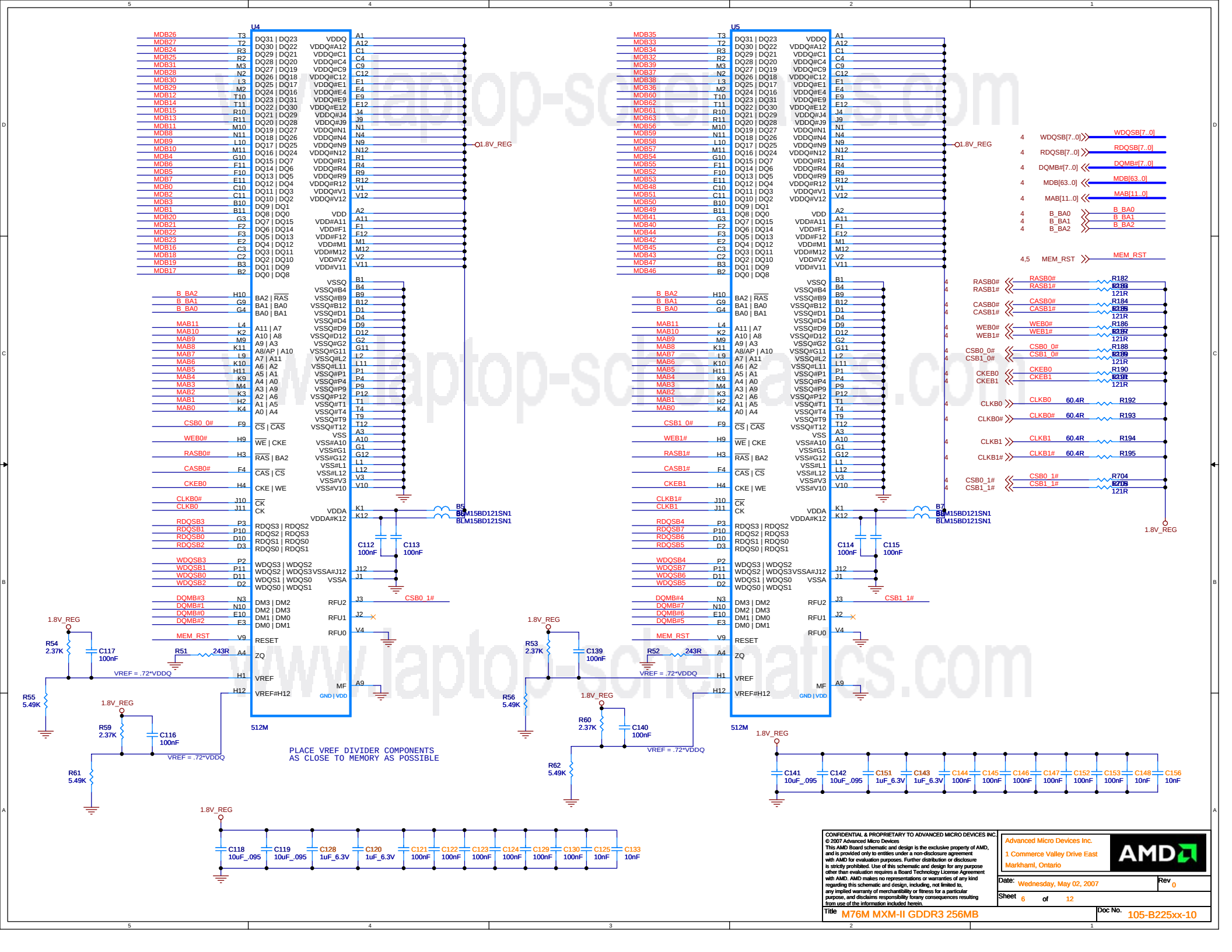
Date:	Wednesday, May 02, 2007
Rev	0
Sheet	5 of 12
Title	M76M MXM-II GDDR3 256MB
Doc No.	105-B225xx-10


U4
U5
512M
1.8V_REG
VREF = .72*VDDQ
PLACE VREF DIVIDER COMPONENTS
AS CLOSE TO MEMORY AS POSSIBLE
BLM15BD121SN1
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Date: Wednesday, May 02, 2007
Rev 0
Sheet 6 of 12
Title M76M MXM-II GDDR3 256MB
Doc No. 105-B225xx-10

PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE

MPCIE1

Mechanical Key

PCIE_PLUS

Power up Glitch control CKT

PLACE TERMINATIONS CLOSE TO CONNECTOR

SM BUS 3V/5V LEVEL SHIFT

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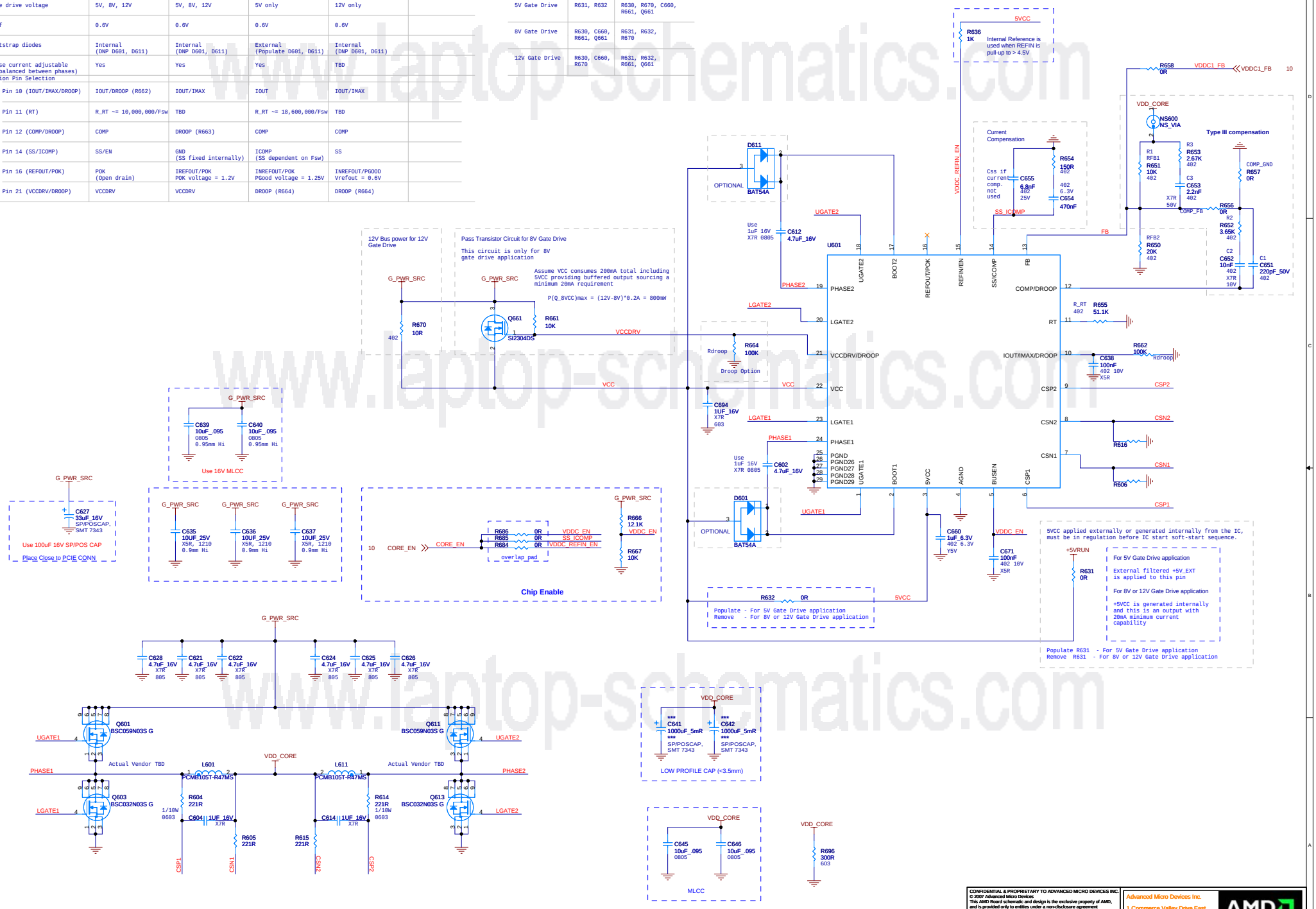
Date:	Wednesday, May 02, 2007
Rev	0
Sheet	7 of 12
Title	M76M MXM-II GDDR3 256MB
Doc No.	105-B225xx-10

Information on Compatable Controller Parts

	PWM IC #1	PWM IC #2	PWM IC #3	PWM IC #4	
Gate drive voltage	5V, 8V, 12V	5V, 8V, 12V	5V only	12V only	
Vref	0.6V	0.6V	0.6V	0.6V	
Bootstrap diodes	Internal (DNP D601, D611)	Internal (DNP D601, D611)	External (Populate D601, D611)	Internal (DNP D601, D611)	
Phase current adjustable (unbalanced between phases) Option Pin Selection	Yes	Yes	Yes	TBD	
Pin 10 (IOUT/IMAX/DROOP)	IOUT/DROOP (R662)	IOUT/IMAX	IOUT	IOUT/IMAX	
Pin 11 (RT)	R_RT ~= 10,000,000/Fsw	TBD	R_RT ~= 18,600,000/Fsw	TBD	
Pin 12 (COMP/DROOP)	COMP	DROOP (R663)	COMP	COMP	
Pin 14 (SS/ICOMP)	SS/EN	GND (SS fixed internally)	ICOMP (SS dependent on Fsw)	SS	
Pin 16 (REFOUT/POK)	POK (Open drain)	IREFOUT/POK POK voltage = 1.2V	INREFOUT/POK PGood voltage = 1.25V	INREFOUT/PGOOD Vrefout = 0.6V	
Pin 21 (VCCDRV/DROOP)	VCCDRV	VCCDRV	DROOP (R664)	DROOP (R664)	

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661



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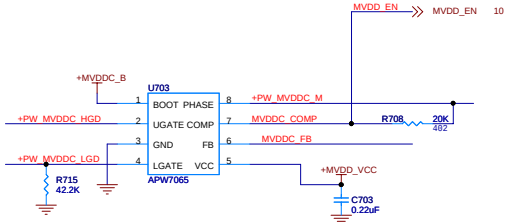
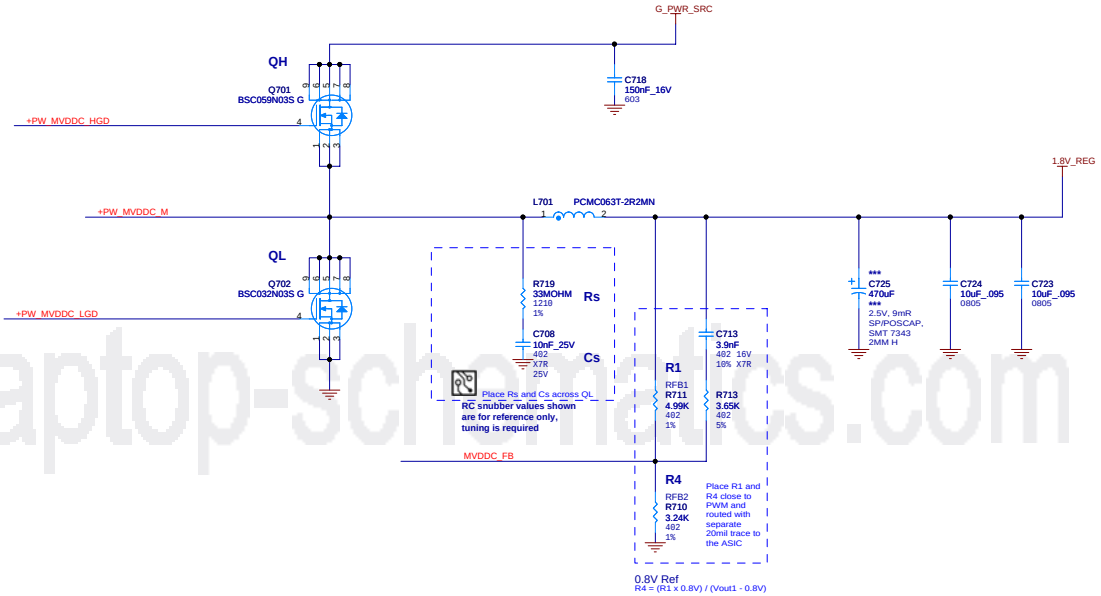
Date: Wednesday, May 02, 2007 Rev 0

Sheet 8 of 12

Title M76M MXM-II GDDR3 256MB

Doc No. 105-B225xx-10





List of supported foodprint

The following ICs are not necessarily evaluated by AMD, please refer to BOM for evaluation status

- **ANPEC APW7120/APW7065 (12V)**
- **CAT CAT7583 (12V)**
- **INTERSIL ISL6545**
- **NEXSEM NX2114/2307**
- **RICHTEK RT9214/RT8101**
- **OnSemi ON1582**
- **uPI UP6101 (No Ext_Vref in)**
- **uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**

SMPS02- Regulator for MVDD

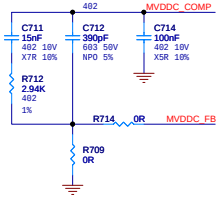
Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G

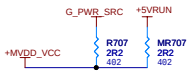
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

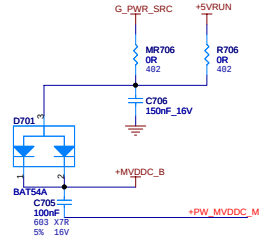
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



Layout guideline for Nexsem NX2114/2307

1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

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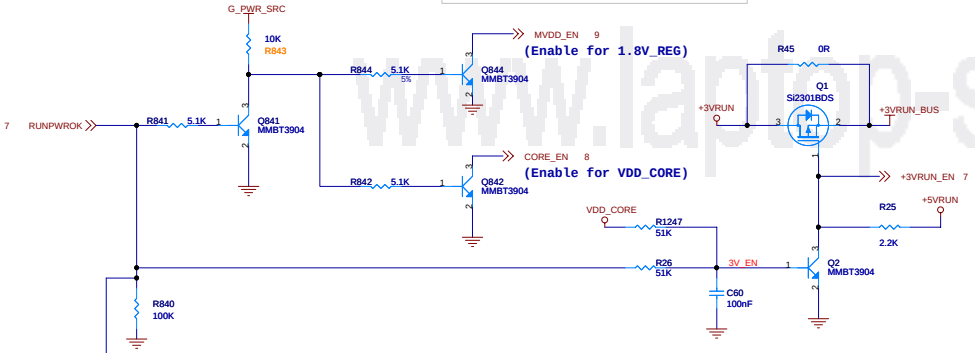
Date: Wednesday, May 02, 2007 Rev 0

Sheet 9 of 12

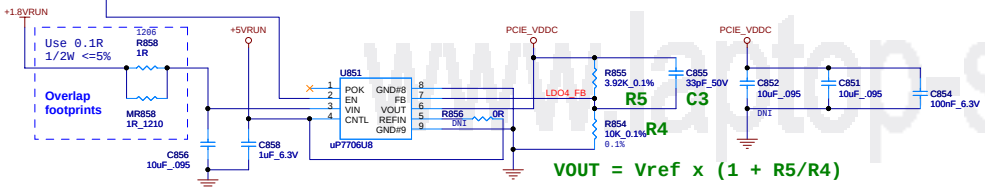
Title M76M MXM-II GDDR3 256MB Doc No. 105-B225xx-10

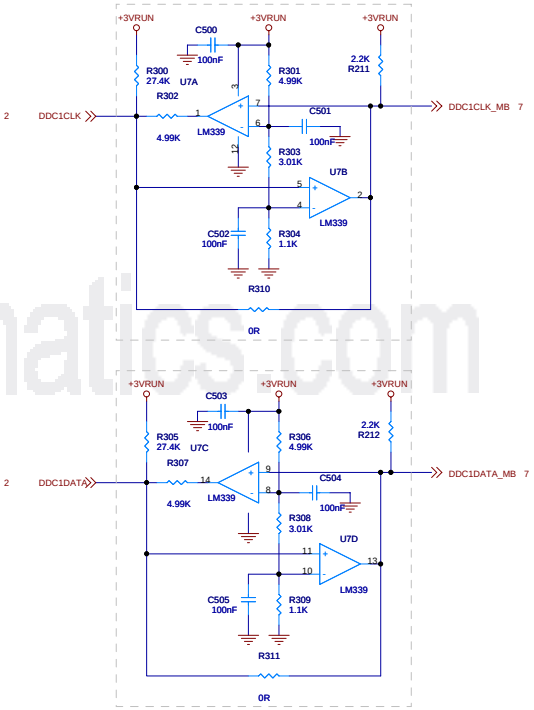
Power Up Sequencing



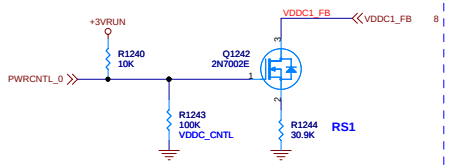
LDO #4: Vin = +1.8V +/-5% Vout = +1.1V +/- 3% Iout = 2A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

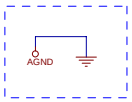




VDDC Voltage Control



	VDDC	RS1	PWRCNTL_0
0.6V Ref	.9V	N/A	LOW
	1.0V	59.0K 1% ATI # 3160590200G	HIGH
	1.1V	30.9K 1% ATI # 3160309200G	HIGH
	1.2V	20.0K 1% ATI # 3160200200G	HIGH



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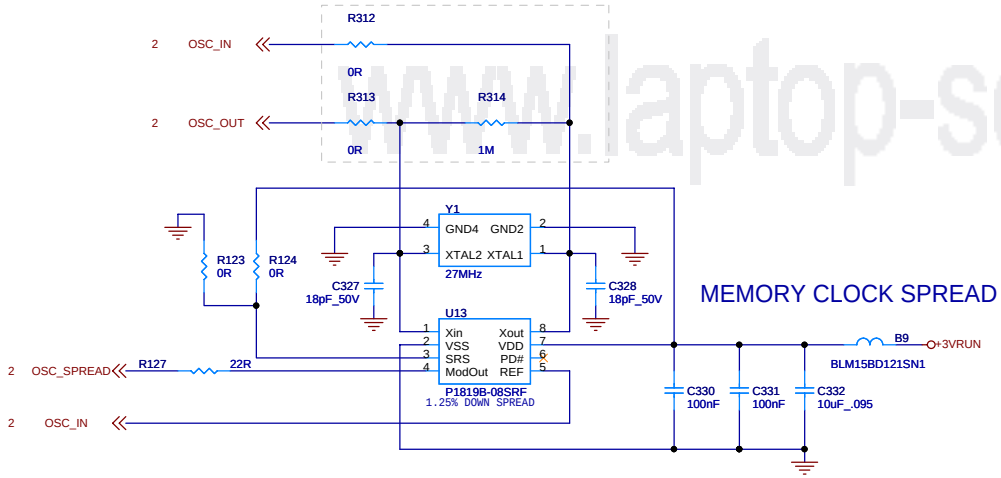
Date: Wednesday, May 02, 2007 Rev 0

Sheet 10 of 12

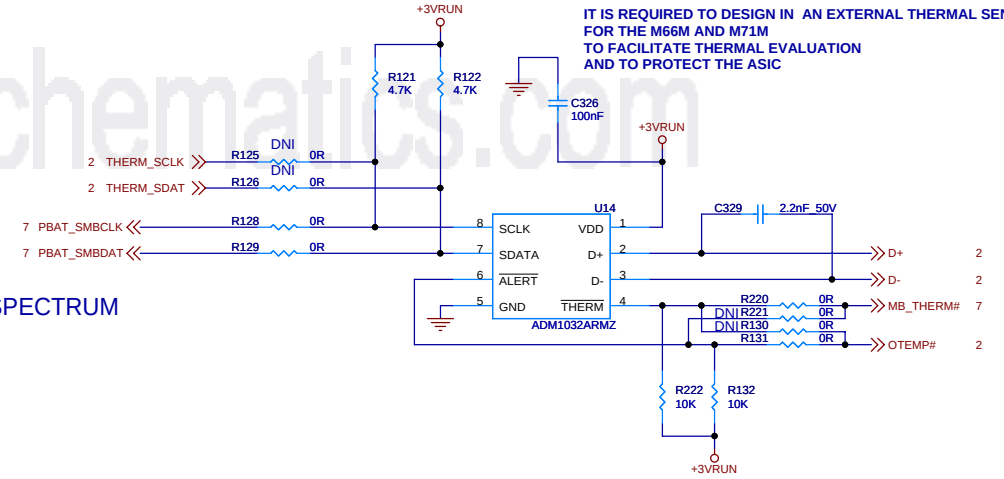
Title M76M MXM-II GDDR3 256MB Doc No. 105-B225xx-10

Crystal Option only



MEMORY CLOCK SPREAD SPECTRUM

IT IS REQUIRED TO DESIGN IN AN EXTERNAL THERMAL SENSOR FOR THE M66M AND M71M TO FACILITATE THERMAL EVALUATION AND TO PROTECT THE ASIC

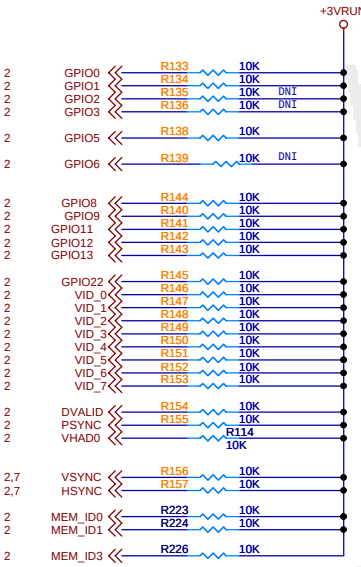


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M66M,M71M	M72M,M76M
BIF_MSI_DIS	VID1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_64BAR_EN_A	VID5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MUXED OUT	0	0
PLL_IBIAS_RD_1	GPIO6	(M66/71)BIAS CURRENT FOR PCIE PHY PLL MSBIT (M72/76)RSVD	0	0
PLL_IBIAS_RD_0	GPIO5	Internal Use - Reserved	1	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1	1
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERATURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	X	X
BIF_VGA DIS	PSYNC	VGA ENABLED	NA	O
MEM_TYPE	UNUSED GPIO	MEMORY TYPE,MAKE AND SIZE INFO	X X X	X X X



AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

VID0 VID2 VID3 VID4 VID6 VID7 HSYNC DVALID GPIO2 GPIO3 GPIO5 GPIO6 GPIO8 VHAD0

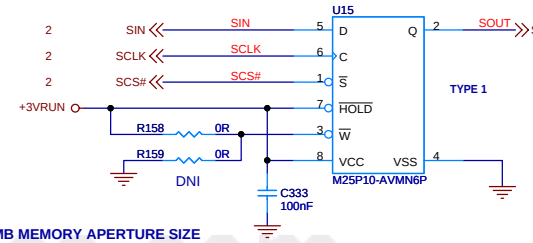
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GENERICC GPIO21_BB_EN GPIO_23_CLKREQB (DRIVES LOW DURING RESET) H2SYNC V2SYNC

GPIO(9,13:11) - CONFIG[3..0]

0010 - 512Kbit AT25F512A (Atmel)
0011 - 1Mbit AT25F1024A (Atmel)
0100 - 512Kbit M25P05A (ST)
0101 - 1Mbit M25P10A (ST)
0101 - 2Mbit M25P20 (ST)
0100 - 512Kbit Pm25LV512 (Chingis)
0101 - 1Mbit Pm25LV010 (Chingis)

FLASH ROM



A 256MB MEMORY APERTURE SIZE CAN BE DEFINED USING A SEPARATE ROM OR STRAPPING

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Date: Wednesday, May 02, 2007 Rev 0

Sheet 11 of 12

Title M76M MXM-II GDDR3 256MB Doc No. 105-B225xx-10

AMD

Title
M76M MXM-II GDDR3 256MB

Schematic No.
105-B225xx-10

Date:
Wednesday, May 02, 2007

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	27/12/06	Initial Design Based on B131
1	00B	27/03/07	Q2 REPLACE TO 2021390400G R1245 ADD 3150000000 (option to connect AC/BAT# to GPIO14) R1246 ADD 3150000000 (option to connect AC/BAT# to GPIO17) R709 ADD 3150000000G (MVDD TO SUPPORT NEW PART) R714 ADD 3150000000G (MVDD TO SUPPORT NEW PART) R715 ADD 3160422200G (MVDD TO SUPPORT NEW PART) R1247 ADD 3150051300G (OPTION TO USE VDD_CORE TO SWITCH +3.3RUN)
2	00	24/04/07	Q15 REPLACE TO 2021390400G (now NPN for +3VRUN_EN inverter) U6 ADD 2430003000G (DUAL SPST) R202 REPLACE TO 3150010400G (now 100K pull up) C859 ADD 4214010600G (10uF on TPVDD) C860 ADD 4214010600G (10uF on DPLL_PVDD) R201 REMOVED R229 ADD 3150000000G (Option to Bypass U6) R230 ADD 3150000000G (Option to Bypass U6) R228 ADD 3150010300G (Pull down on BL_BRIGHT_MB) R227 ADD 3150010400G (Q15 base resistor) R25 REPLACE TO 3150022200G (change to 2.2K so Q15 base load doesn't cuase too much voltage drop) C861 ADD 4170010400G (U6 Decupling cap)
3	10	01/05/07	U7 ADD 2480001900G (Active level shifter for DDC1) R304 ADD 3160110100G (Active level shifter for DDC1) R309 ADD 3160110100G (Active level shifter for DDC1) R300 ADD 3160274200G (Active level shifter for DDC1) R305 ADD 3160274200G (Active level shifter for DDC1) R303 ADD 3160301100G (Active level shifter for DDC1) R308 ADD 3160301100G (Active level shifter for DDC1) R301 ADD 3160499100G (Active level shifter for DDC1) R302 ADD 3160499100G (Active level shifter for DDC1) R306 ADD 3160499100G (Active level shifter for DDC1) R307 ADD 3160499100G (Active level shifter for DDC1) C500 ADD 4170010400G (Active level shifter for DDC1) C501 ADD 4170010400G (Active level shifter for DDC1) C502 ADD 4170010400G (Active level shifter for DDC1) C503 ADD 4170010400G (Active level shifter for DDC1) C504 ADD 4170010400G (Active level shifter for DDC1) C505 ADD 4170010400G (Active level shifter for DDC1) R310 ADD 3150000000G (Bypass Active level shifter for DDC1) R311 ADD 3150000000G (Bypass Active level shifter for DDC1) R312 ADD 3150000000G (Crystal only option) R313 ADD 3150000000G (Crystal only option) R314 ADD 3160100400G (Crystal only option)