31P141, NV31, 4(8,16)Mx16, 64(128,256)MB, VIDEO IN/OUT, DVI-I, VGA

Page Overview

HISTORY:

A00

X00: INITIAL VERSION

X01: First Review

- Replaced series resistors in sync lines with 33ohms
- Moved clamping diodes next to GPU
- Added parallel caps to EMI filter DACB
- Removed not needed strap on SAA7114
- Connected RESET and WP of SST ROM t o ROMVCC
- Added parallel ROM and Strapps
- Added FBVDD regulator
- Added STEREO glasses circuit
- Removed Decoupling CAPs on VIP VDD, covered by Caps on page 2
- Added ROM_VCC for cleaner planes
- Changed used TMDS lines of IFPA and IFPB to TP from NTP
- Changed Resistor for AGP Vref circuit to 158k

X02: Final Review

- Added clock termination resistors
- Added net name for FBCALxxx
- Added cap on filter input for FB_DLLVDD, DACA_VDD & DACB_VDD
- Changed netnames for SAA7114 NTPs to NTP_x xx
- Added 1uF cap parallel to fan connector
- Changed all xxCALxx resistors to 50 Ohms
- Changed all FBxDQS*<x> to NTP_FBxDQS*<x> with NO_TEST p roperty

8912 01091600

- page 14 delete original FAN control and TEMP sensor
- page 15 add twin bios for MSi function
- page 18 add HW monitor

8912 01110820

- page 13 delete S port TV-ou and changed with Composite TV-out.

8912 01131251

- Deleted NVIDIA page 14 R580 and R582.
- Deleted all useless net line.
- Replaced all OFFPAGE_sym with ORCAD OFFPAGE.
- Replaced all NVIDIA title block with ROCAD title block.

602-10141-0000-000 Base Schematic

Title: OVERVIEW		
Size: Custom	Document Number: MS-8912	Rev: 200
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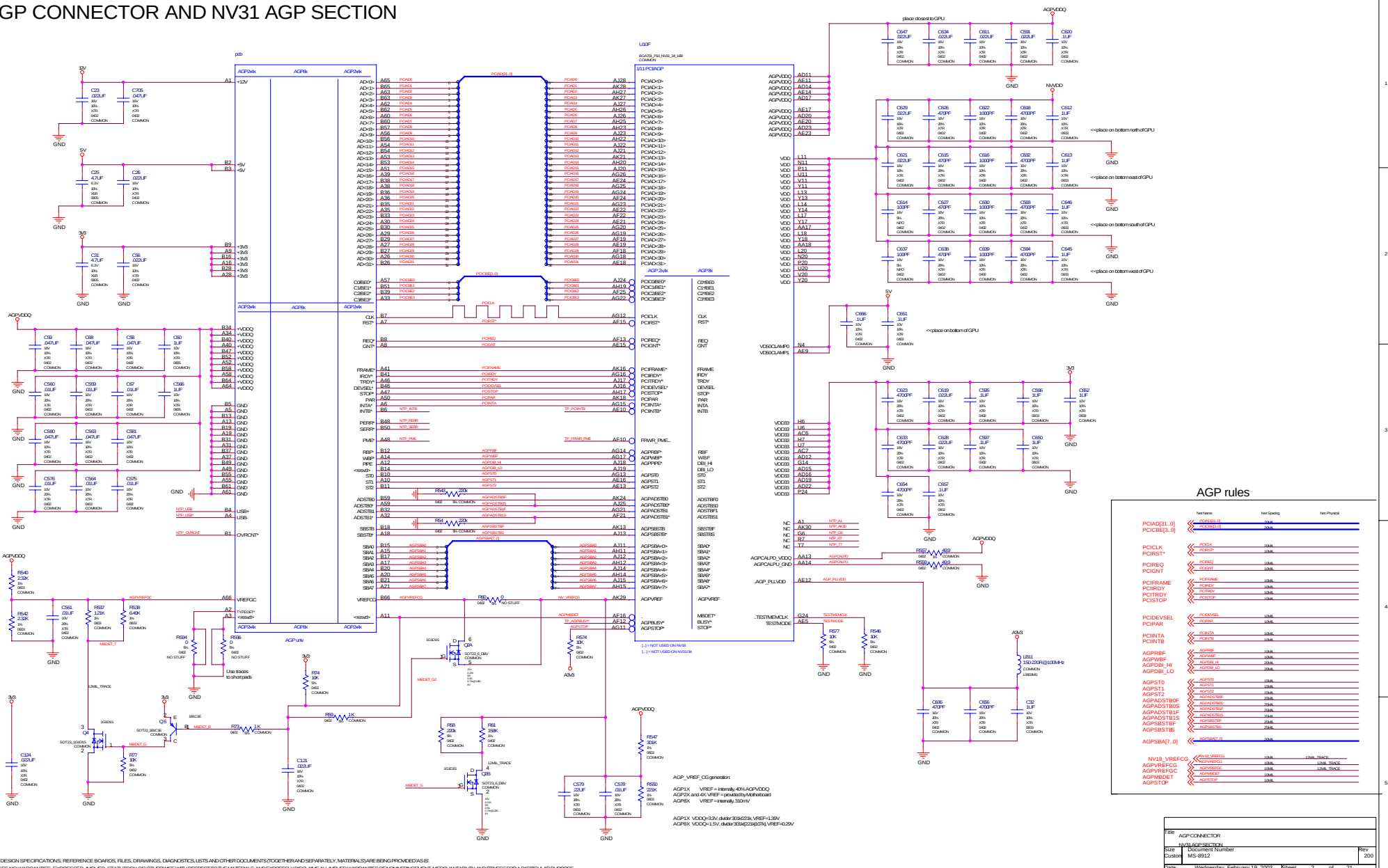
AGP CONNECTOR AND NV31 AGP SECTION



Title	AGP CONNECTOR
	NV31 AGP SECTION
Size: Custom	Document Number: MS-8912
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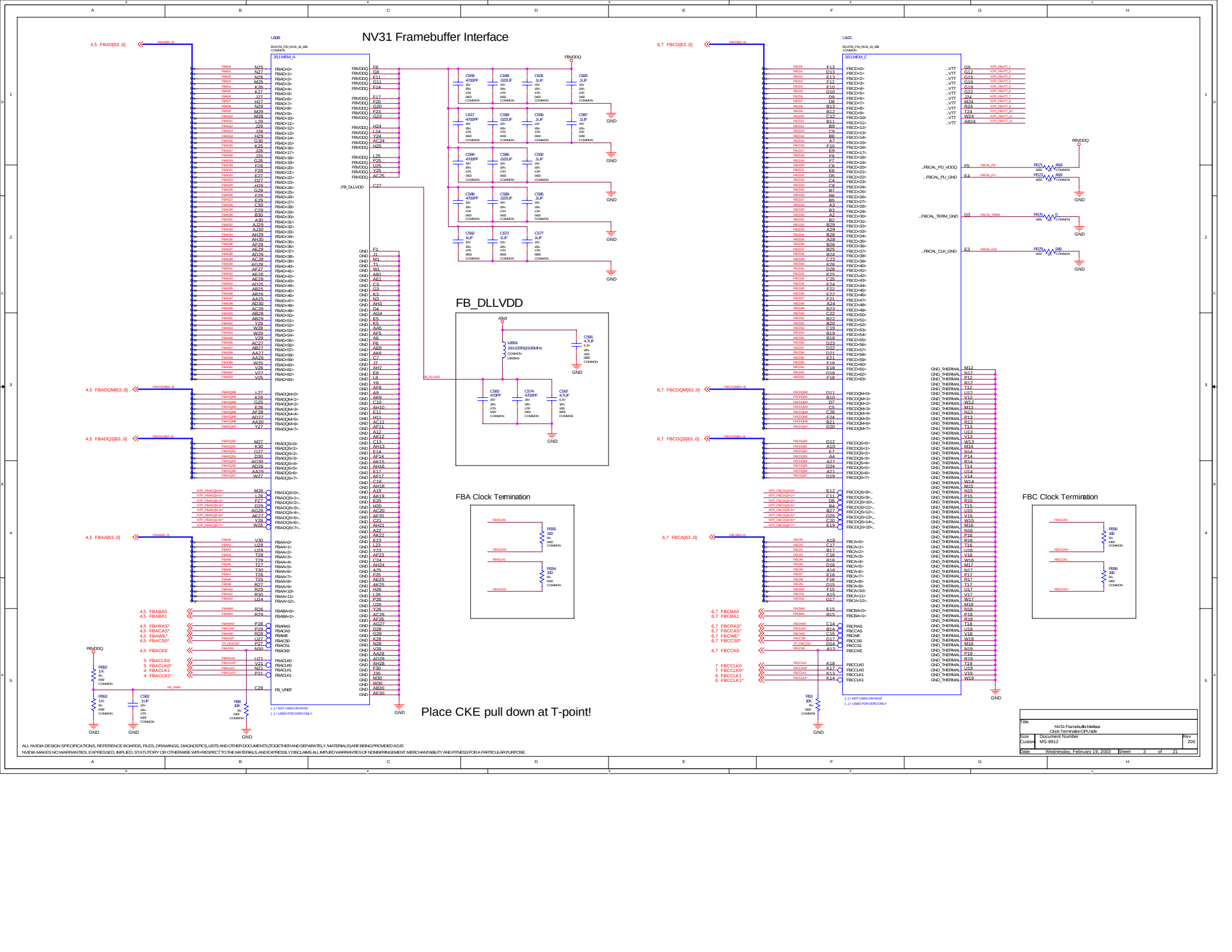
NV31 Framebuffer Interface
FB_DLLVDD
FBA Clock Termination
FBC Clock Termination
Place CKE pull down at T-point!
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Title
NV31 Framebuffer Interface
Clock Termination GPU side
Size
Custom
Document Number
MS-8912
Rev
200
Date: Wednesday, February 19, 2003
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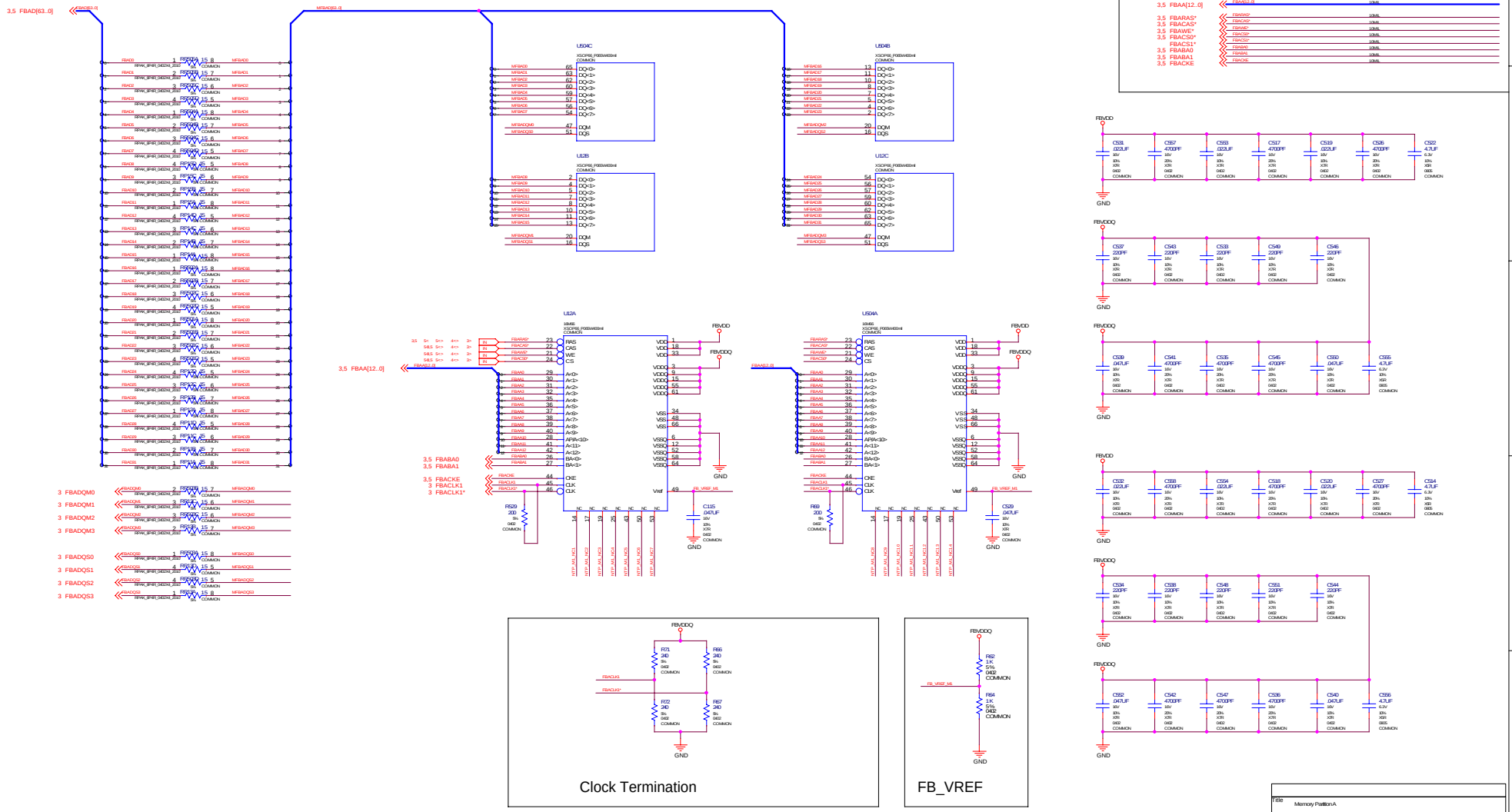
MEMORY 8(16)Mx16DDR Partition A , Bits 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

NET	Diffpair	NET_SPACING_RULE
3 FBACLK1	FBACLK0	10MIL_G2C_25MIL
3 FBACLK1*	FBACLK0	10MIL_G2C_25MIL
3 FBAD[31..0]	FBADQS[3..0]	10MIL
3 FBADQM[3..0]	FBADQS[3..0]	10MIL
3 FBADQS[3..0]	FBADQS[3..0]	10MIL
MFBAD[31..0]	MFBADQS[3..0]	10MIL
MFBADQM[3..0]	MFBADQS[3..0]	10MIL
MFBADQS[3..0]	MFBADQS[3..0]	10MIL
3,5 FBAA[12..0]	FBAA12	10MIL
3,5 FBARAS*	FBARAS*	10MIL
3,5 FBACAS*	FBACAS*	10MIL
3,5 FBAWE*	FBAWE*	10MIL
3,5 FBACS0*	FBACS0*	10MIL
FBACS1*	FBACS1*	10MIL
3,5 FBABA0	FBABA0	10MIL
3,5 FBABA1	FBABA1	10MIL
3,5 FBACKE	FBACKE	10MIL



Title	Memory Partition A Bits 0..31		
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MEMORY 8(16)Mx16DDR Partition A , Bits 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

NET	Diffpair	NET_SPACING_RULE
3 FBACLK0	FBACLK0	10MIL_G2G_20MIL
3 FBACLK0*	FBACLK0*	10MIL_G2G_20MIL
3 FBAD[63..32]	FBAD[63..32]	10MIL
3 FBADQM[7..4]	FBADQM[7..4]	10MIL
3 FBADQS[7..4]	FBADQS[7..4]	10MIL
MFBAD[63..32]	MFBAD[63..32]	10MIL
MFBADQM[7..4]	MFBADQM[7..4]	10MIL
MFBADQS[7..4]	MFBADQS[7..4]	10MIL
3,4 FBAA[12..0]	FBAA[12..0]	10MIL
3,4 FBARAS*	FBARAS*	10MIL
3,4 FBACAS*	FBACAS*	10MIL
3,4 FBAWE*	FBAWE*	10MIL
3,4 FBACS0*	FBACS0*	10MIL
3,4 FBABA0	FBABA0	10MIL
3,4 FBABA1	FBABA1	10MIL
3,4 FBACKE	FBACKE	10MIL

Clock Termination

FB_VREF

Title	Memory Partition A Bits 32:63		
Size	Document Number		Rev
Custom	MS-8912		200
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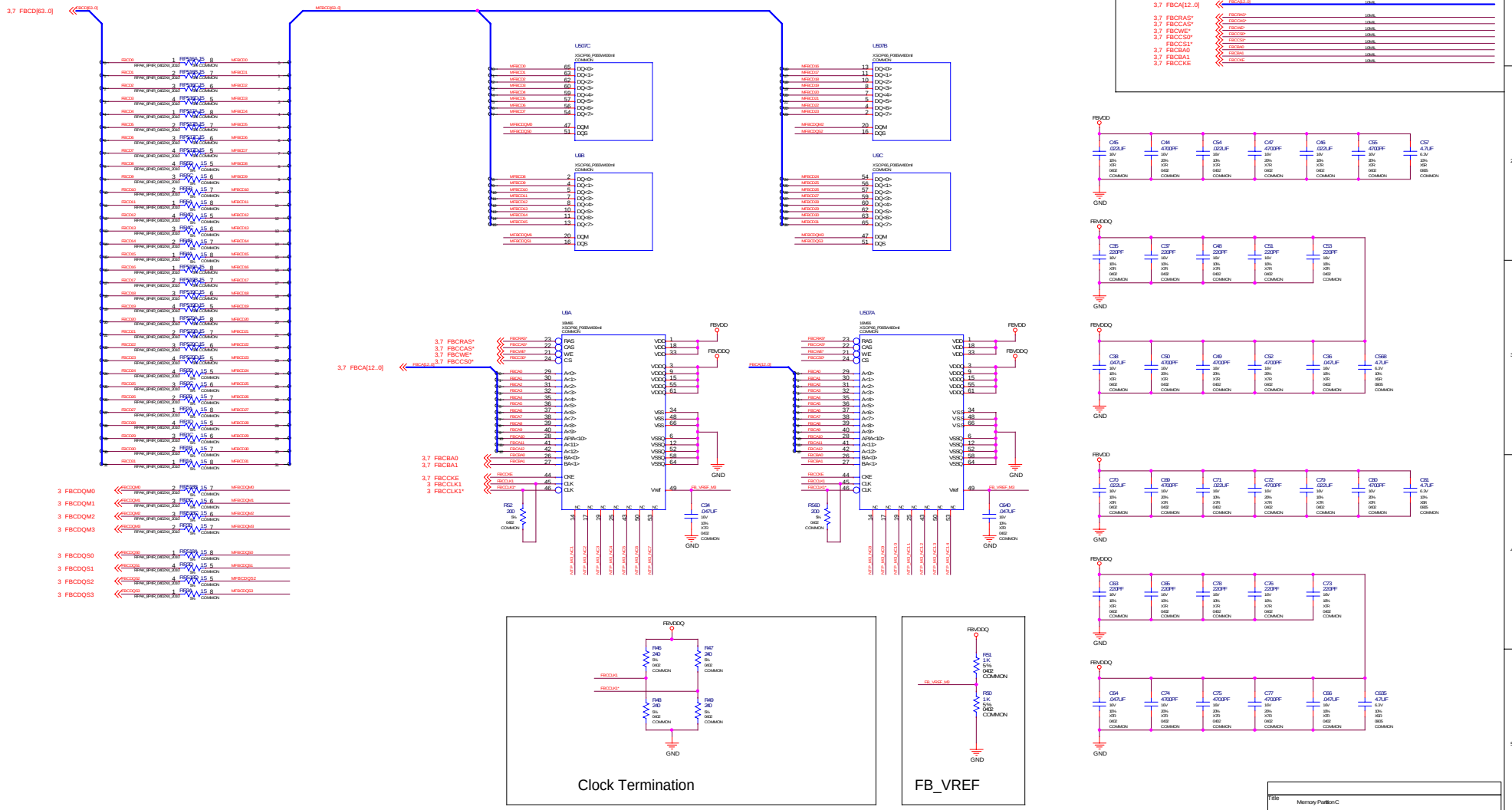
MEMORY 8(16)Mx16DDR Partition C , Bits 0..31

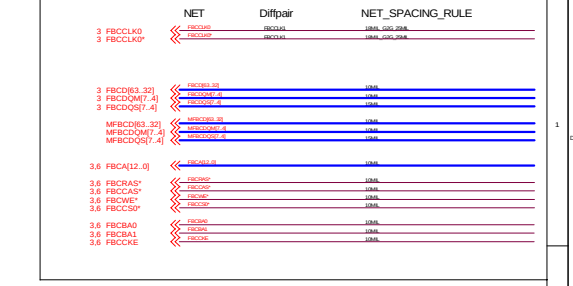
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

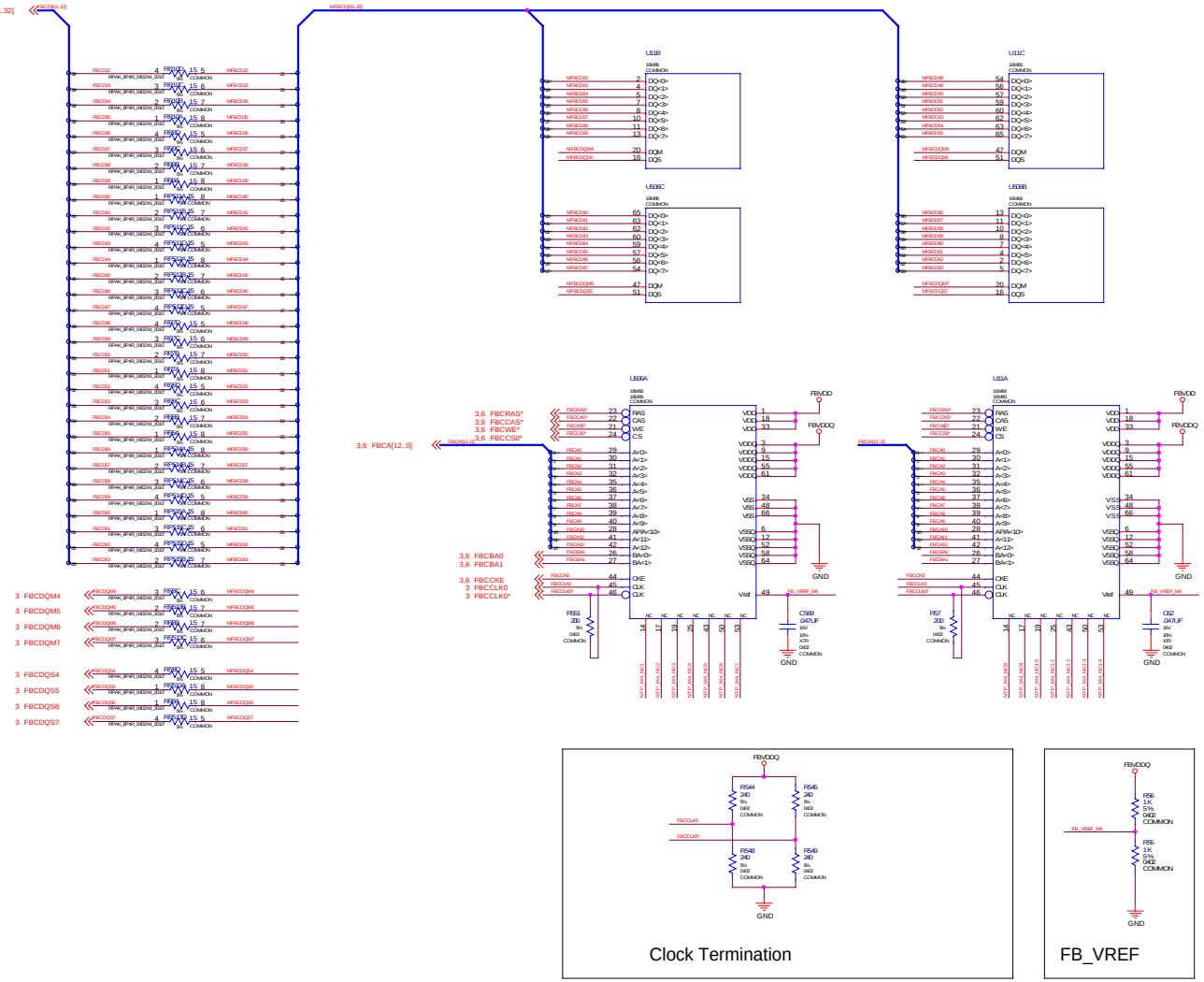


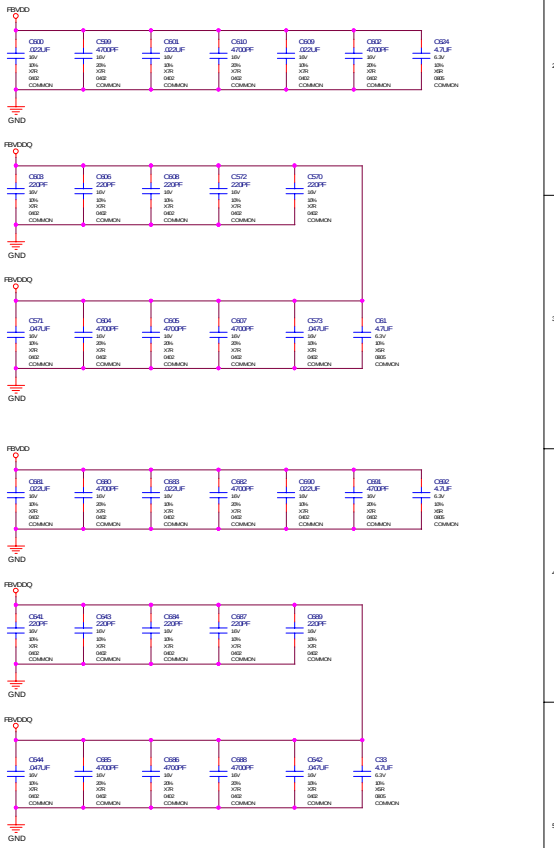
Title	Memory Partition C Bits 0..31		
Size	Document Number		Rev
Custom	MS-8912		200
Date:	Wednesday, February 19, 2003	Sheet 6 of 21	

MEMORY 8(16)Mx16DDR Partition C , Bits 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!







Title	Memory Partition C Bits 32:63	
Size: Custom	Document Number: MS-8912	Rev: 200
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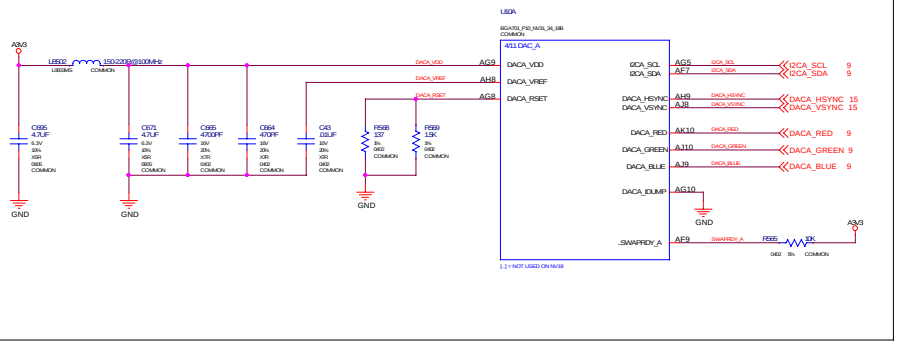
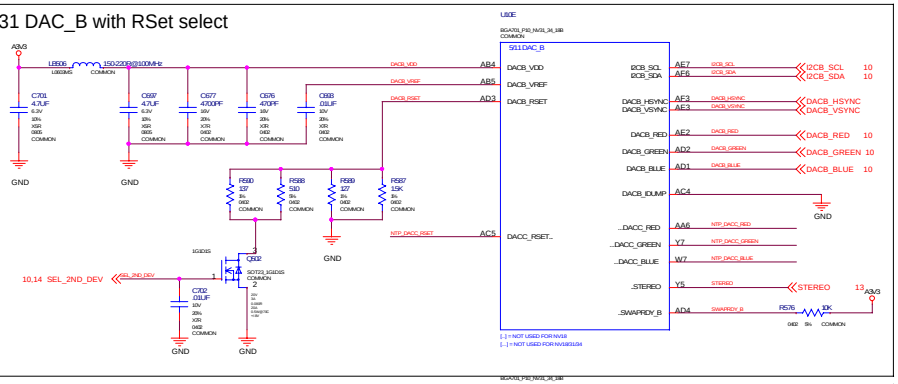
NV31 DAC_A, DAC_B, PLL, SYNC Buffer

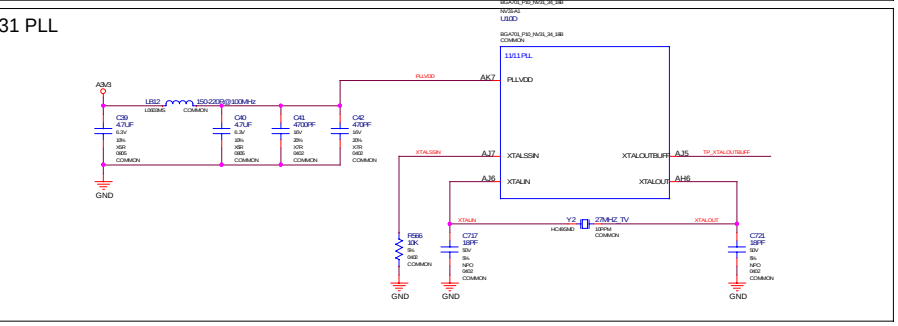
NV31 DAC_A



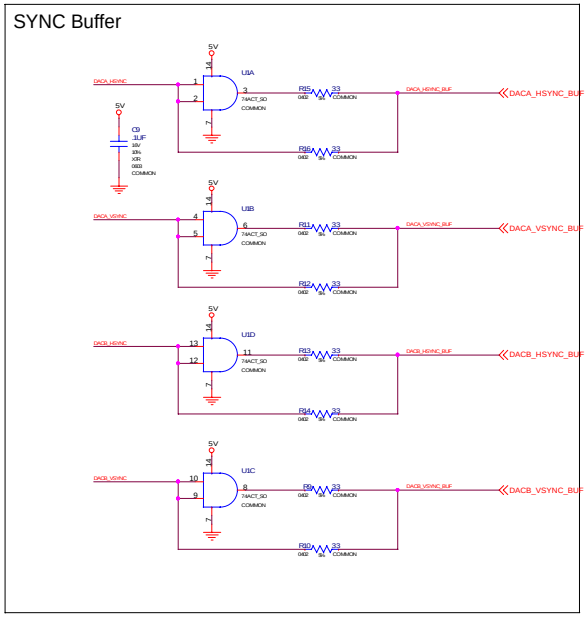
NV31 DAC_B with RSet select



NV31 PLL



SYNC Buffer



NET	NET_PHYSICAL_TYPE	VOLTAGE
DACA_VDD	12MIL_TRACE	3.3V
DACA_VREF	5MIL_TRACE	
DACA_RSET	5MIL_TRACE	
DACB_VDD	12MIL_TRACE	3.3V
DACB_VREF	5MIL_TRACE	
DACB_RSET	5MIL_TRACE	
PLLVDD	12MIL_TRACE	3.3V

NET	NET_PHYSICAL_TYPE	NET_SPACING_RULE
XTALIN	5MIL_TRACE	10MIL
XTALOUT	5MIL_TRACE	10MIL

NET	NET_SPACING_RULE
9 DACA_RED	20MIL_G2G_20MIL
9 DACA_GREEN	20MIL_G2G_20MIL
9 DACA_BLUE	20MIL_G2G_20MIL
10 DACB_RED	20MIL_G2G_20MIL
10 DACB_GREEN	20MIL_G2G_20MIL
10 DACB_BLUE	20MIL_G2G_20MIL

Title	NV31 DAC A & B PLL and Sync Buffer		
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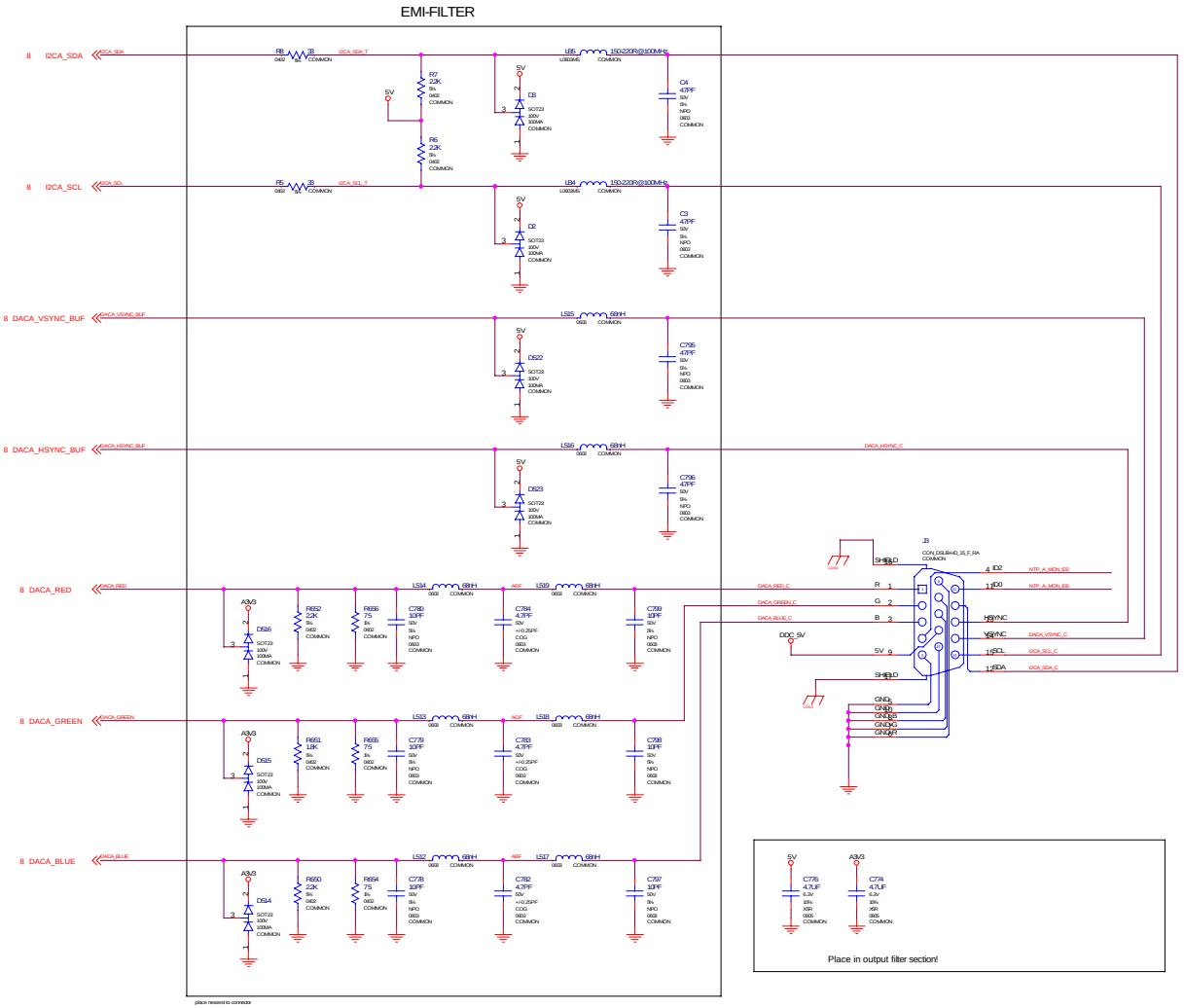
Primary Display (DACA), DB15 only!

NET	NET_SPACING_RULE
ARF	ARF — XMIL_G2C_XMIL
AGF	AGF — XMIL_G2C_XMIL
ABF	ABF — XMIL_G2C_XMIL
DACA_RED_C	DACA_RED_C — XMIL_G2C_XMIL
DACA_GREEN_C	DACA_GREEN_C — XMIL_G2C_XMIL
DACA_BLUE_C	DACA_BLUE_C — XMIL_G2C_XMIL



Place all filter components on the side nearest to the reference GND plane!

Route all signals only on layers referenced to GND!

Don't split the reference GND plane beneath a RGB signal!

Title	Primary Display RGB Filter and DB15 connector	
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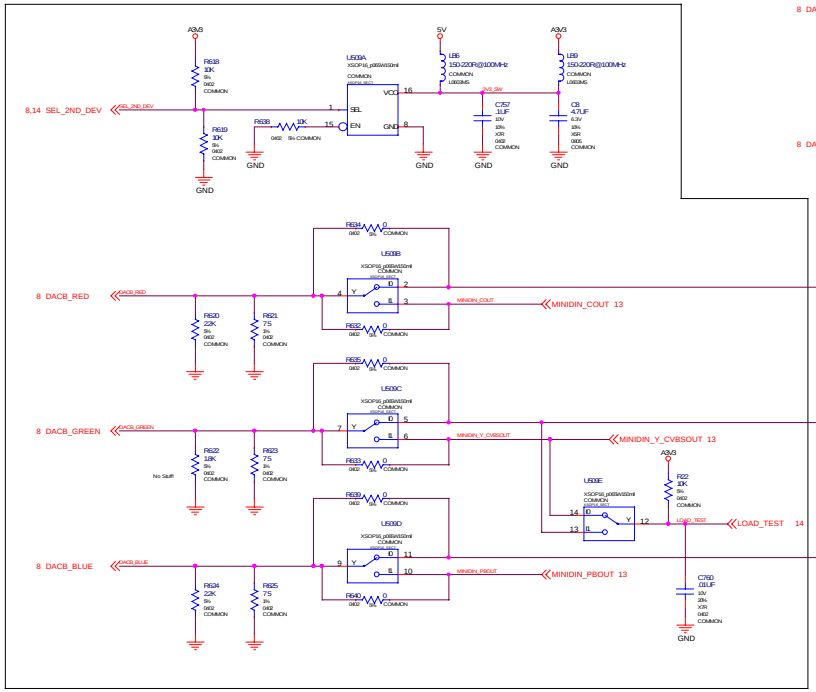
Secondary Display (DACB), long DB15 optional DVI-I

Place all filter components on the side nearest to the reference GND plane!

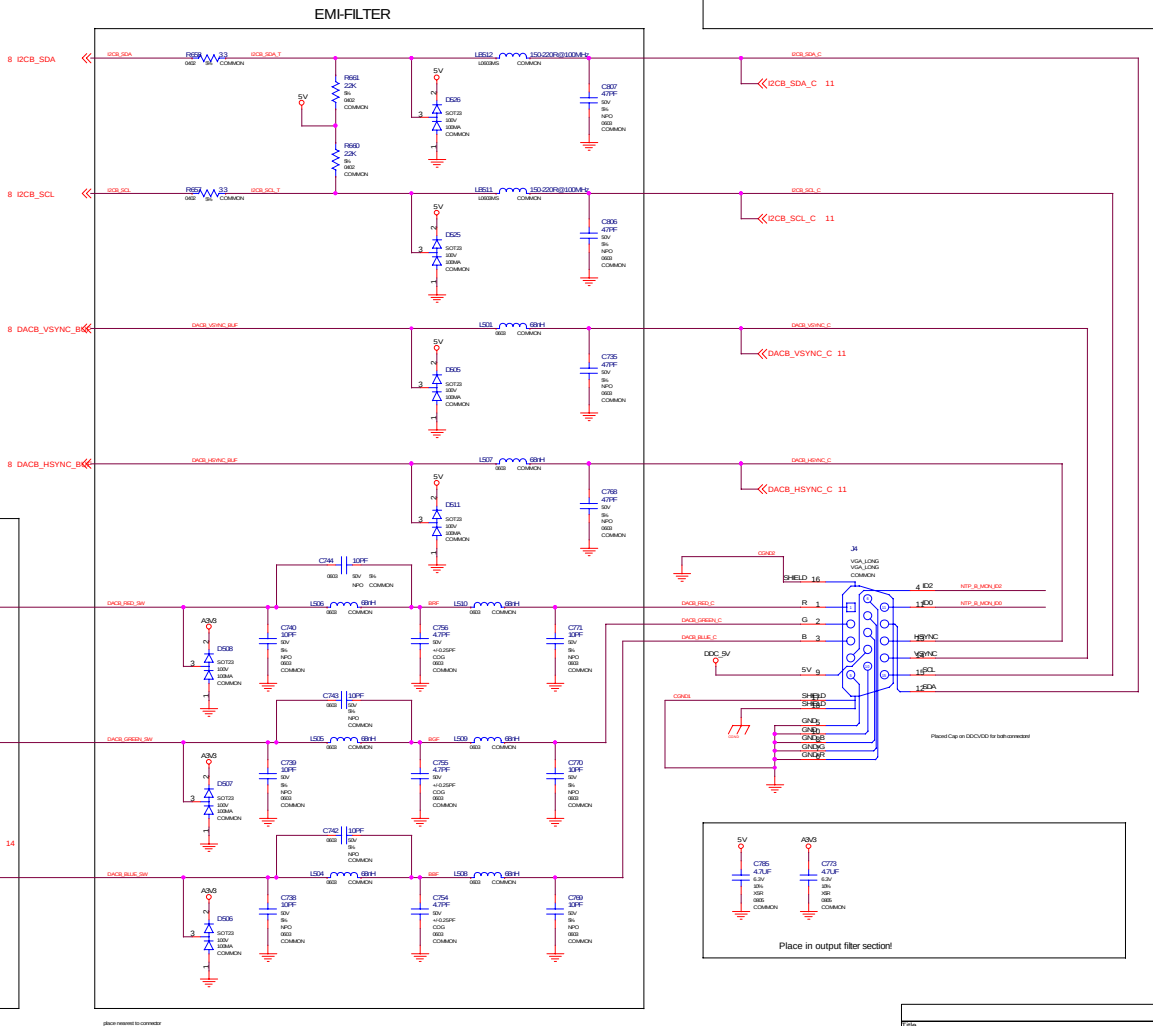
Route all signals only on layers referenced to GND!

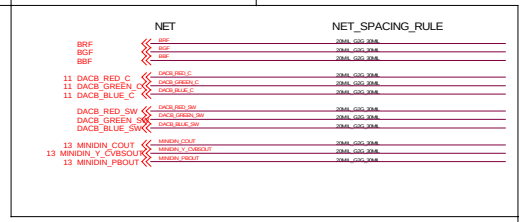
Don't split the reference GND plane beneath a RGB signal!

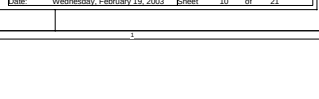
DACB Multiplexer



EMI-FILTER

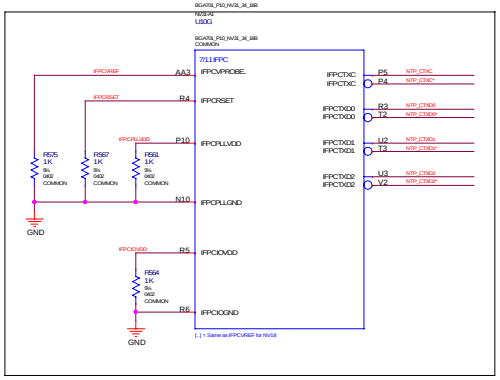




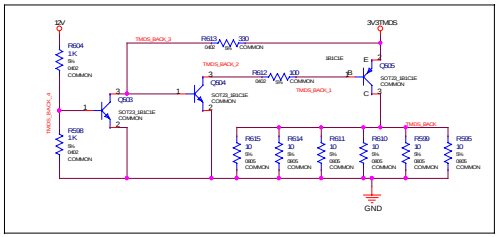


INTERNAL DUAL LINK TMDS POWER AND DECOUPLING

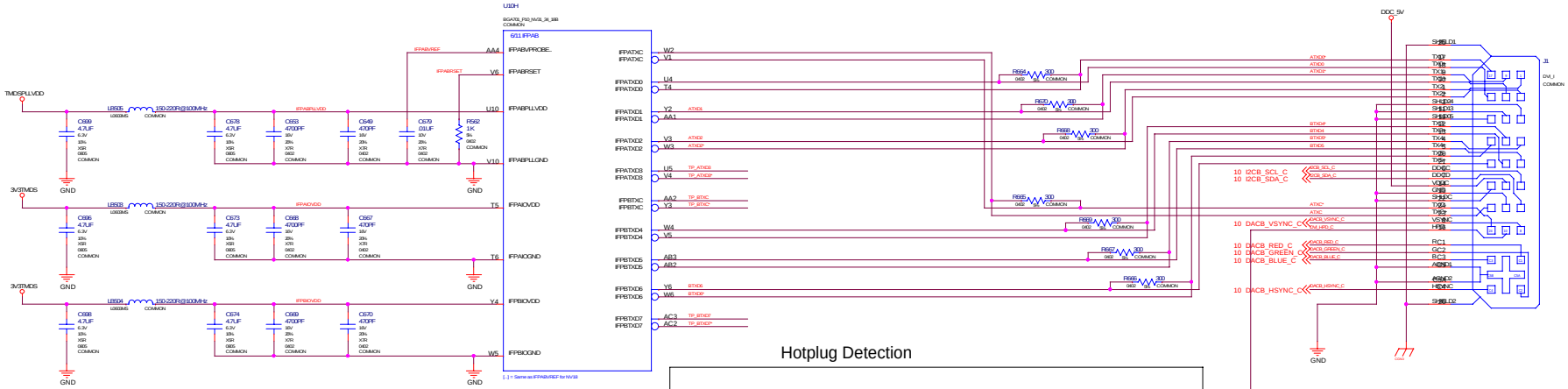
Unused Transmitter



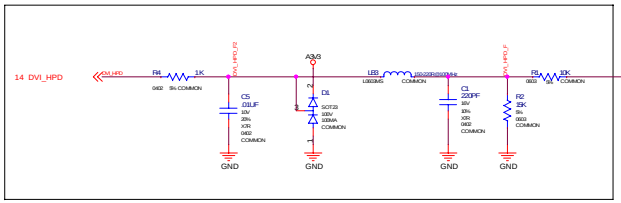
TMDS backdrive prevention



DualLink Transmitter



Hotplug Detection



NET	NET_PHYSICAL_TYPE	VOLTAGE
IFPABVREF	12MIL TRACE	3.3V
IFPABPLLVDD	12MIL TRACE	3.3V
IFPAIOVDD	12MIL TRACE	3.3V
IFPBIOVDD	12MIL TRACE	3.3V
IFPCVREF	12MIL TRACE	3.3V
IFPCPLLVDD	12MIL TRACE	3.3V
IFPCIOVDD	12MIL TRACE	3.3V
FAN_RETURN	12MIL TRACE	3.3V
TMDS_BACK	12MIL TRACE	3.3V

NET	Diffpair	NET_SPACING_RULE
ATXD0	ATX0	XMIL_G2G_XMIL
ATXD0*	ATX0*	XMIL_G2G_XMIL
ATXD1	ATX1	XMIL_G2G_XMIL
ATXD1*	ATX1*	XMIL_G2G_XMIL
ATXD2	ATX2	XMIL_G2G_XMIL
ATXD2*	ATX2*	XMIL_G2G_XMIL
ATXC	ATXC	XMIL_G2G_XMIL
ATXC*	ATXC*	XMIL_G2G_XMIL
BTXD4	BTX4	XMIL_G2G_XMIL
BTXD4*	BTX4*	XMIL_G2G_XMIL
BTXD5	BTX5	XMIL_G2G_XMIL
BTXD5*	BTX5*	XMIL_G2G_XMIL
BTXD6	BTX6	XMIL_G2G_XMIL
BTXD6*	BTX6*	XMIL_G2G_XMIL

Title	Nv31 Internal TMDS Tiesmitter
	DVI-Connector and Backdrive Prevention
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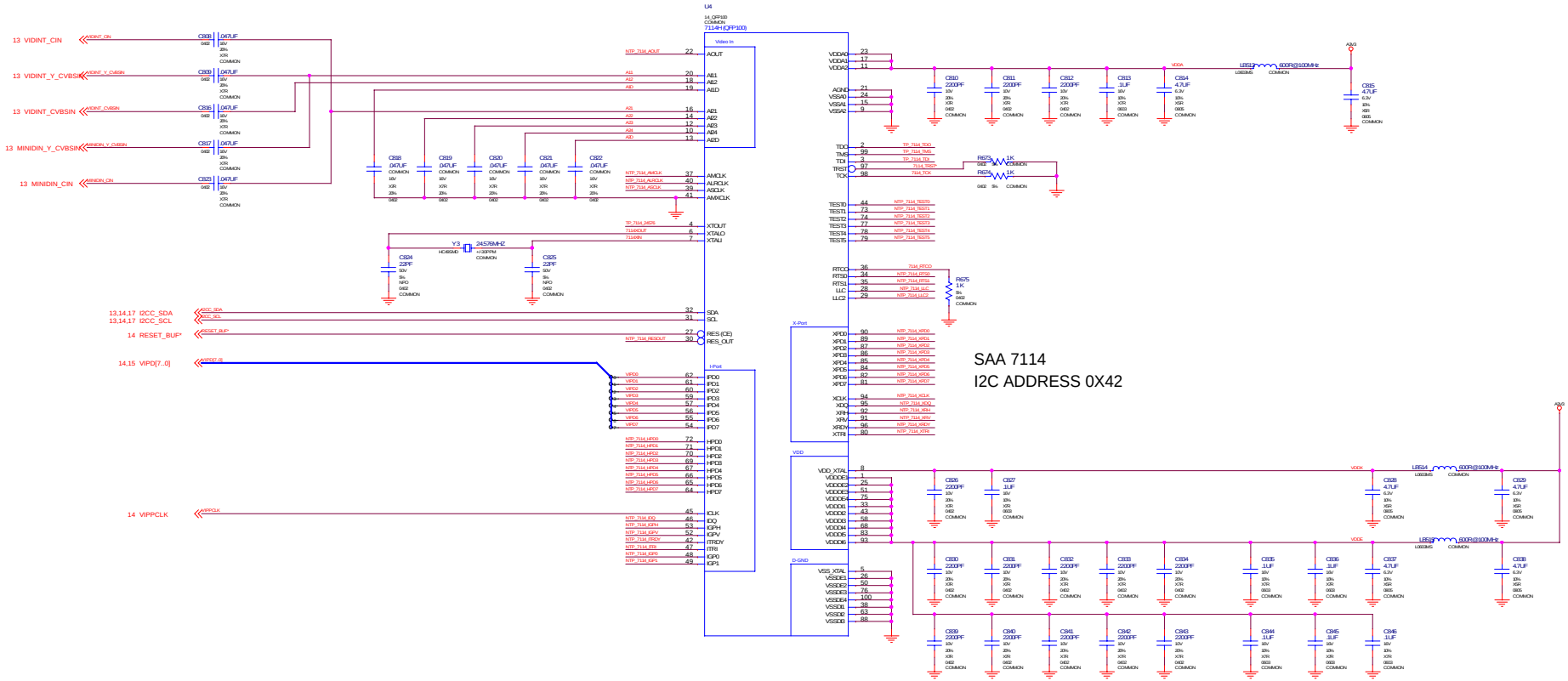
VIDEO CAPTURE



Title	Video Capture SAA7114
Size: Custom	Document Number: MS-8912
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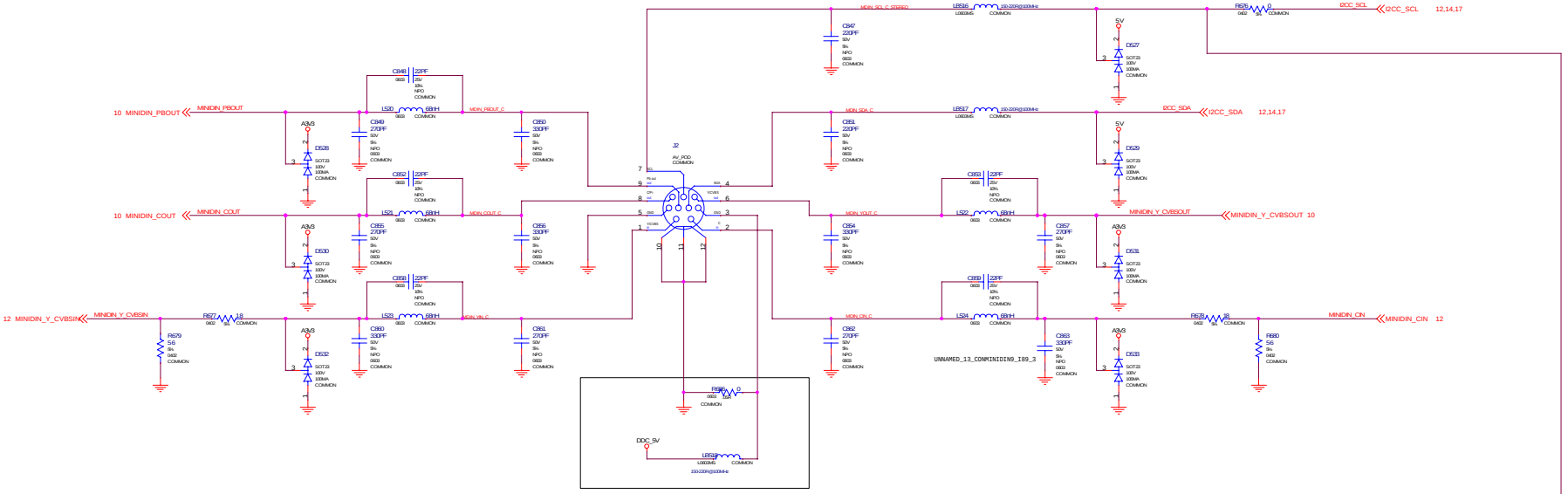
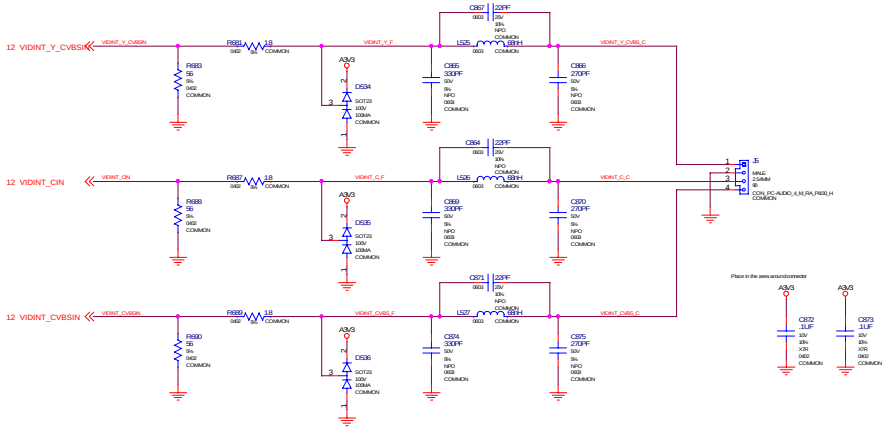
MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES



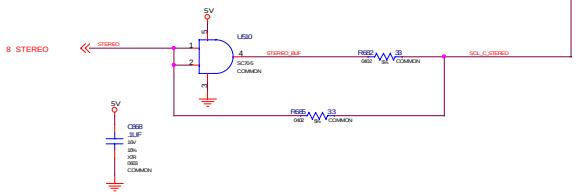
For STEREO GLASSES 3pin MiniDIN only:
Stuff bead!
And replace 0 Ohm resistor wit 220PF cap!

INTERNAL VIDEO IN CONNECTOR



STEREO GLASSES BUFFER

Place close to MiniDIN connector!



Title	VIVO/STEREO MiniDIN connector		
	Internal Video In connector		
Size	Document Number		Rev
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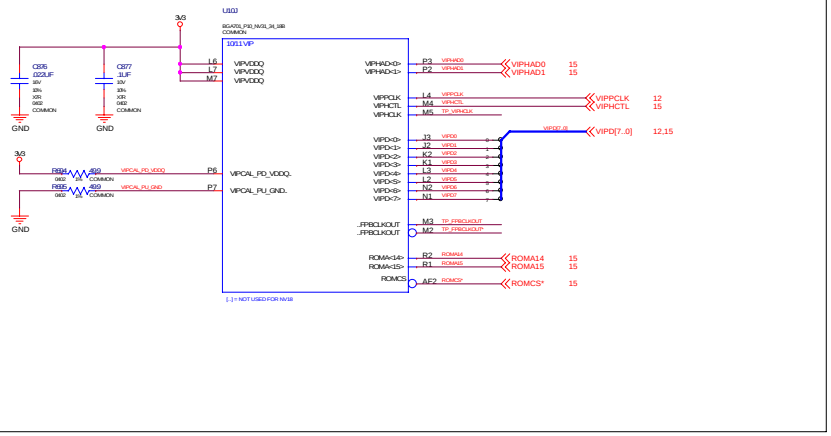
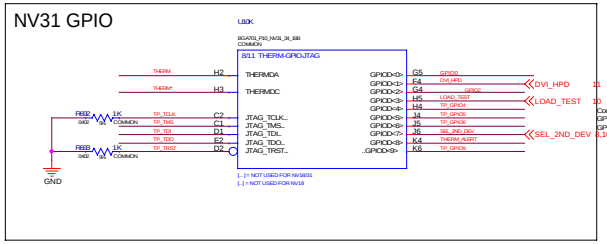
NV31 DVO, VIP AND GPIO SECTION

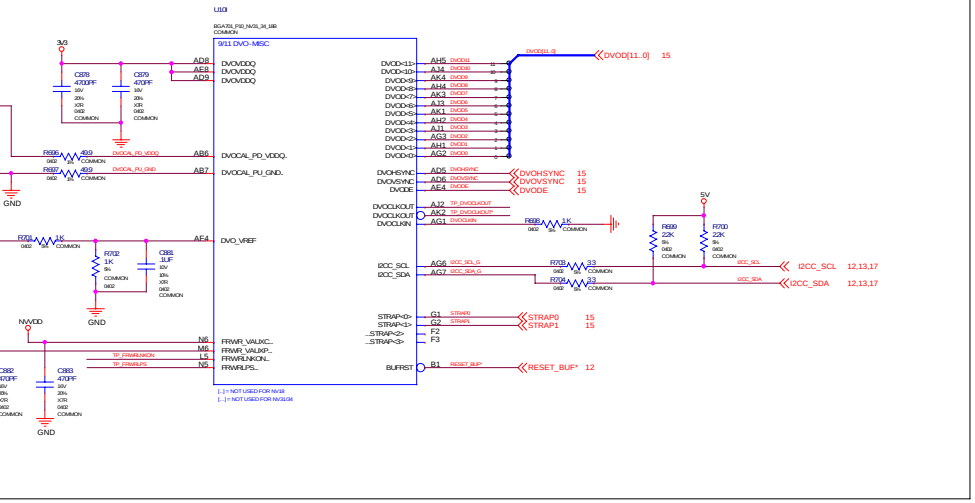
NV31 VIP



NV31 GPIO



NV31 DVO



NET | NET_PHYSICAL_TYPE | VOLTAGE

NET	NET_PHYSICAL_TYPE	VOLTAGE
FAN_RETURN	FAN_RETURN 10MIL_TRACE	3.3V
THERM	THERM 10MIL_TRACE	
THERM*	THERM 10MIL_TRACE	

NET | NET_SPACING_RULE

NET	NET_SPACING_RULE
12,15 VIPD[7..0]	VIPD7..0 10MIL
12 VIPPCLK	VIPPCLK 20MIL_CSC_10MIL

Title	NV31, DVO,VIP and GPIO Interface	
	FAN control, Tampersensor	
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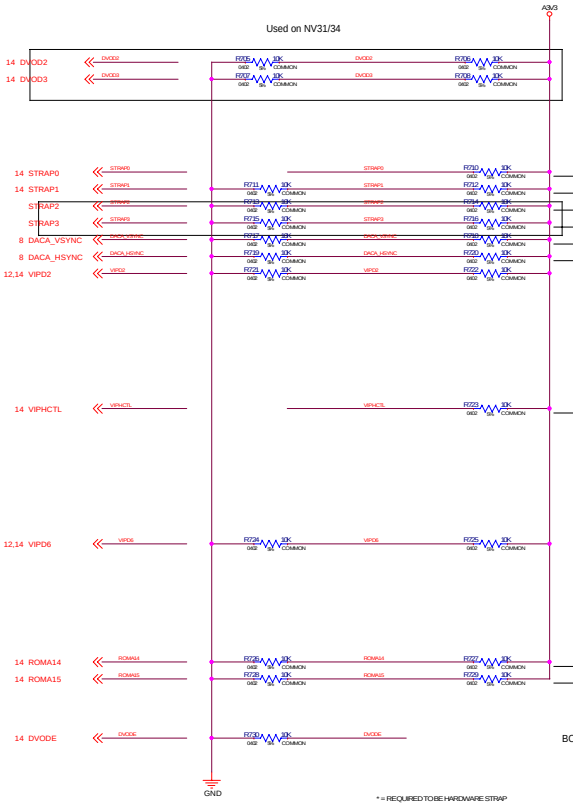
NV31 BIOS STRAPPING

ANDMASK
1 -> HARDWARE STRAP
0 -> BIOS STRAP

ORMASK
1 -> DESIRED=1,ANDMASK=0

Used on NV31/34

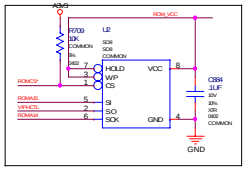


* = REQUIRED TO BE HARDWARE STRAP

SKU#	0000			0001			0002			0003		
	DESIRED	AND MASK	OR MASK	DESIRED	AND MASK	OR MASK	DESIRED	AND MASK	OR MASK	DESIRED	AND MASK	OR MASK
BOOT_0_STRAP_0												
* 00: PCI_AD_SWAP	1	1	0	1	1	0	1	1	0	1	1	0
* 01: SUB_VENDOR	1	1	0	1	1	0	1	1	0	1	1	0
02: RAM_CFG_0	1	1	0	1	1	0	1	1	0	1	1	0
03: RAM_CFG_1	1	1	0	1	1	0	1	1	0	1	1	0
04: RAM_CFG_2	0	1	0	0	1	0	0	1	0	0	1	0
05: RAM_CFG_3	0	1	0	0	1	0	0	1	0	0	1	0
06: CRYSTAL_0	0	1	0	0	1	0	0	1	0	0	1	0
07: TV_MODE_0	1	0	1	1	0	1	1	0	1	1	0	1
08: TV_MODE_1	0	0	0	0	0	0	0	0	0	0	0	0
09: AGPIntBx	0	0	0	0	0	0	0	0	0	0	0	0
10: AGP_SBA	0	0	0	0	0	0	0	0	0	0	0	0
11: AGP_FASTWR	0	0	0	0	0	0	0	0	0	0	0	0
12: PCI_DEVID_0	0	0	0	0	0	0	0	0	0	1	0	0
13: PCI_DEVID_1	1	0	1	1	0	1	1	0	1	0	0	1
* 14: BUS_TYPE	1	1	0	1	1	0	1	1	0	1	1	0
15: FP_IFACE	1	0	1	1	0	1	1	0	1	1	0	1
16: USER_0	0	0	0	0	0	0	0	0	0	0	0	0
17: USER_1	0	0	0	0	0	0	0	0	0	0	0	0
18: USER_2	0	0	0	0	0	0	0	0	0	0	0	0
19: USER_3	0	0	0	0	0	0	0	0	0	0	0	0
20: PCI_DEVID_2	0	0	0	0	0	0	0	0	0	0	0	0
21: PCI_DEVID_3	0	0	0	0	0	0	0	0	0	0	0	0
22: CRYSTAL_1	1	1	0	1	1	0	1	1	0	1	1	0
23: FIL_0	0	0	0	0	0	0	0	0	0	0	0	0
24: FIL_1	0	0	0	0	0	0	0	0	0	0	0	0
25: BR	0	0	0	0	0	0	0	0	0	0	0	0
26: BR_128M	0	0	0	0	0	0	0	0	0	0	0	0
27: BR_AGP	0	0	0	0	0	0	0	0	0	0	0	0
28: BR_IO	0	0	0	0	0	0	0	0	0	0	0	0
* 29: ROM_TYPE_0	1	1	0	1	1	0	1	1	0	1	1	0
* 30: ROM_TYPE_1	0	1	0	0	1	0	0	1	0	0	1	0
31: STRAP_0_OVERWRITE	0	0	0	0	0	0	0	0	0	0	0	0
BOOT_3_STRAP_1												
0: 1394	0	0	0	0	0	0	0	0	0	0	0	0
1: 1394_PHY	0	0	0	0	0	0	0	0	0	0	0	0
2: 1394_PHY_PWRCLASS[0]	0	0	0	0	0	0	0	0	0	0	0	0
3: 1394_PHY_PWRCLASS[1]	0	0	0	0	0	0	0	0	0	0	0	0
4: VGA_DEVICE	1	0	1	1	0	1	1	0	1	1	0	1
5: MCM_LSB_SWAP	0	0	0	0	0	0	0	0	0	0	0	0
6: BR_LAST_DEV	0	0	0	0	0	0	0	0	0	0	0	0
7: BR_BARS_BCASTONLY	0	0	0	0	0	0	0	0	0	0	0	0
31: STRAP_1_OVERWRITE	0	0	0	0	0	0	0	0	0	0	0	0

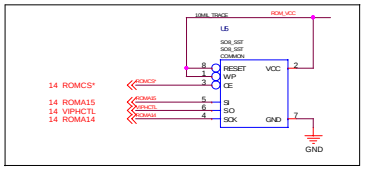
NV Register Description	NV Address	BIOS Address	Data SKU#0000-0002 (600-0161-0000, 600-0161-0001, 600-0161-0002)	Data SKU#0003 (600-0161-0003)
BOOT_0_STRAP_0 0x00101000			0x2040E08F	0x2040C08F
BOOT_1_STRAP_0_ANDMASK 0x00101004		0x58	0x6040407F	0x6040407F
BOOT_2_STRAP_0_ORMASK 0x00101008		0x5C	0x00008080	0x00008080
BOOT_3_STRAP_1 0x0010100C			0x00000010	0x00000010
BOOT_4_STRAP_1_ANDMASK 0x00101010		0x60	0x00000000	0x00000000
BOOT_5_STRAP_1_ORMASK 0x00101014		0x64	0x00000010	0x00000010

BIOS (serial)

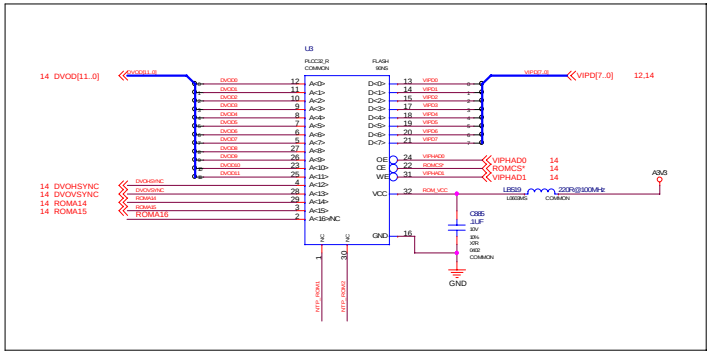


U2 AND U5
DUAL
LAYOUT

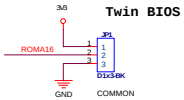
BIOS (serial alternative)



BIOS (parallel alternative)



Twin BIOS



Title	NV31 Strapps Serial and Parallel BIOS ROM
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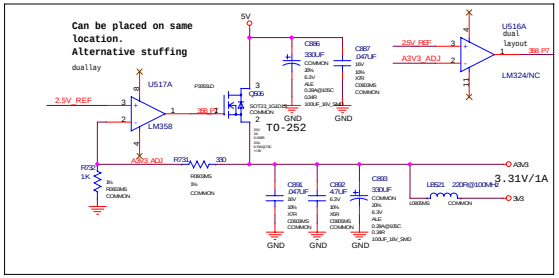
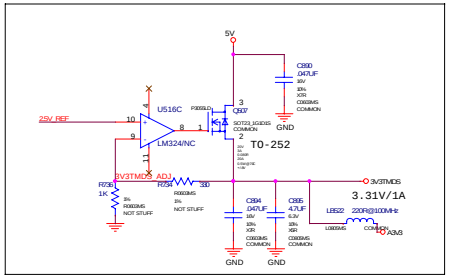
POWER SUPPLY

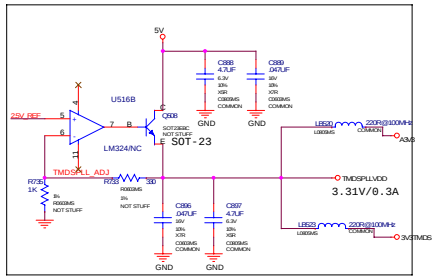
ANALOG 3V3

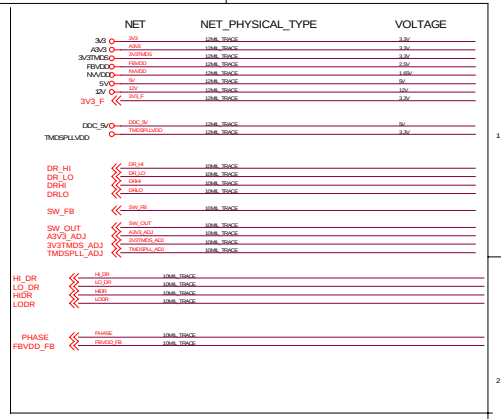


TMDS 3V3 Supply



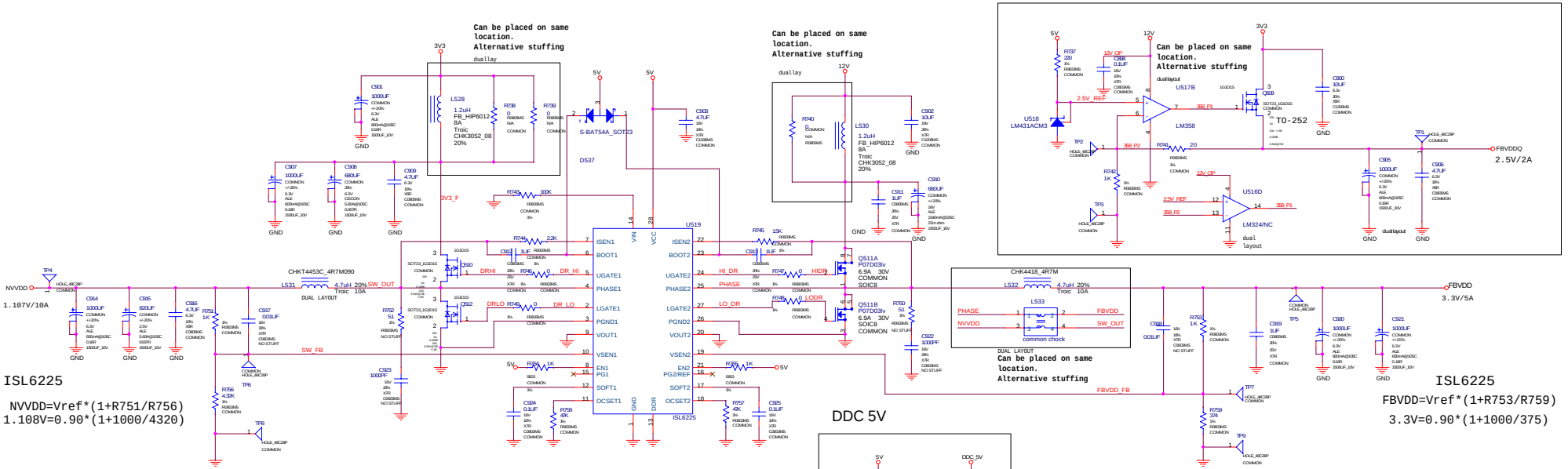
TMDS PLL Supply





NVVDD-SWITCHER / FBVDDQ-LDO CONTROLER

Replaced ISL6529 with ISL6225.
Replaced P07D03LV with APM7312.



Title	Power Supplies	
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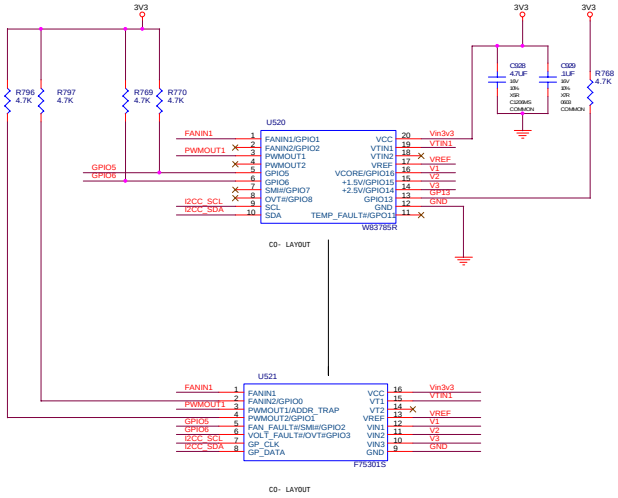
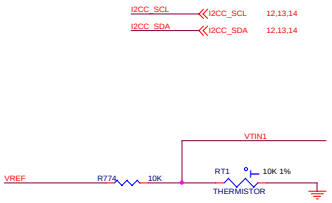
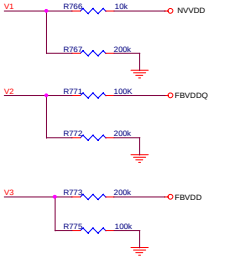
H/W MONITOR

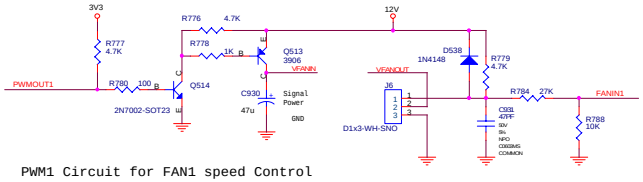




TEMPERATURE SENSORING CIRCUIT

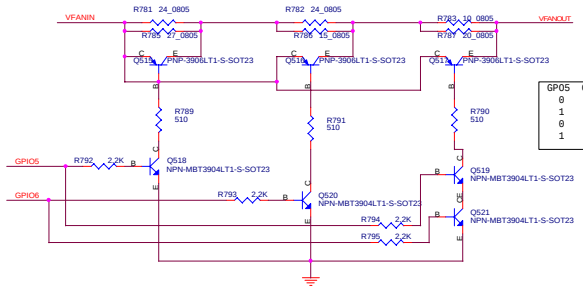


VOLTAGE SENSORING CIRCUIT



PWM1 Circuit for FAN1 speed Control

FOR 12V FAN



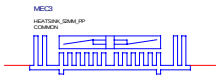
GP05	GP06	Q1	Q2	Q3	Vout
0	0	off	off	off	9V
1	0	on	off	off	10V
0	1	off	on	off	11V
1	1	on	on	on	12V

MECHANICAL COMPONENTS

BRACKET

SCREWS

HEATSINK



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*** Signal Cross-Reference for the entire design ***

3V3TMDS_ADJ 16.1G<> 16.3C
3V3_F 16.1G<> 16.3C
5V_FUSED 16.1G<> 17.4G
12V_F 16.1G<>
A3V3_ADJ 16.1G<> 16.2A
ABF 9.1G<> 9.5C
AGF 9.1G<> 9.6C
AGPADSTB8F 2.3C 2.5G<>
AGPADSTB8S 2.3C 2.5G<>
AGPADSTB9F 2.3C 2.5G<>
AGPADSTB9S 2.3C 2.5G<>
AGPDBI_HI 2.3C 2.4E<>
AGPDBI_LO 2.3C 2.6G<>
AGPMBDET 2.4D 2.5C 2.6G<>
AGPRBF 2.3C 2.4G<>
AGPSBA<0> 2.4C 2.6D
AGPSBA<7..0> 2.4C 2.5G<>
AGPSBA<1> 2.4C 2.6D
AGPSBA<2> 2.4C 2.6D
AGPSBA<3> 2.4C 2.6D
AGPSBA<4> 2.4C 2.6D
AGPSBA<5> 2.4C 2.6D
AGPSBA<6> 2.4C 2.6D
AGPSBA<7> 2.4C 2.6D
AGPSBSTB8F 2.4C 2.5G<>
AGPSBSTB8S 2.4C 2.5G<>
AGPST0 2.3C 2.4G<>
AGPST1 2.3C 2.4G<>
AGPST2 2.3C 2.5G<>
AGPUTOP 2.4D 2.5G<>
AGPVREFCG 2.4C 2.5G<>
AGPVREFGC 2.4A 2.5G<>
AGPWBF 2.3C 2.4G<>
ARF 9.1G<> 9.3C
ATXC 11.1G<> 11.3D 11.4G
ATXC* 11.1G<> 11.3D 11.4G
ATXD0 11.1G<> 11.3D 11.3G
ATXD0* 11.1G<> 11.3D 11.3G
ATXD1 11.1G<> 11.3D 11.3G
ATXD1* 11.1G<> 11.3D 11.3G
ATXD2 11.1G<> 11.3D 11.4D
ATXD2* 11.1G<> 11.3D 11.4D
BBF 10.1G<> 10.5E
BGF 10.1G<> 10.4E
BOOT 17.1G<> 17.2C 17.2H
BRF 10.1G<> 10.4E
BTXD4 11.2G<> 11.4D 11.4G
BTXD4* 11.2G<> 11.3D 11.4D
BTXD5 11.2G<> 11.4D 11.4G
BTXD5* 11.2G<> 11.4D 11.4G
BTXD6 11.2G<> 11.4D 11.4G
BTXD6* 11.2G<> 11.4D 11.4G
DACA_BLUE 8.1G<> 8.2D> 9.5A<
DACA_BLUE_C 9.1G<> 9.4D
DACA_GREEN 8.1G<> 8.2D> 9.4A<
DACA_GREEN_C 9.1G<> 9.3D
DACA_HSYNC 8.1D> 8.3F 15.2A<> 15.2B
DACA_HSYNC_BUF 8.2G<> 9.0A<
DACA_RED 8.1G<> 8.2D> 9.3A<
DACA_RED_C 9.1G<> 9.3D
DACA_RSET 8.1C 8.1G<>
DACA_VDD 8.1C 8.1G<>
DACA_VREF 8.1C 8.1G<>
DACA_VSYNC 8.2D> 8.3F 15.2A<> 15.2B
DACA_VSYNC_BUF 8.2G> 9.0A<
DACB_BLUE 8.1G<> 8.2D> 10.5A<
DACB_BLUE_C 10.1G<> 10.4F 11.4G<
DACB_BLUE_SW 10.1G<> 10.5D
DACB_GREEN 8.1G<> 8.3D> 10.4A<
DACB_GREEN_C 10.1G<> 10.4F 11.4G<
DACB_GREEN_SW 10.1G<> 10.4D
DACB_HSYNC 8.3D> 8.3F
DACB_HSYNC_BUF 8.3G> 9.0D<
DACB_HSYNC_C 10.3G> 10.3G> 11.4G<
DACB_RED 8.1G<> 8.3D> 10.4A<
DACB_RED_C 10.1G<> 10.4F 11.4G<
DACB_RED_SW 10.1G<> 10.4D
DACB_RSET 8.1G<> 8.3C
DACB_VDD 8.1G<> 8.3C
DACB_VREF 8.1G<> 8.3C
DACB_VSYNC 8.3D> 8.4F
DACB_VSYNC_BUF 8.4G> 10.0D<
DACB_VSYNC_C 10.3G> 10.3G> 11.4G<
DRHI 16.1G<> 16.4D
DRLO 16.1G<> 16.4D
DR_HI 16.1G<> 16.3H 16.4D
DR_LO 16.1G<> 16.3H 16.4D
DVI_HPD 11.5D> 14.3H<
DVOD<0> 14.4C 15.3F
DVOD<11..0> 14.3D> 15.3F<
DVOD<1> 14.4C 15.3F
DVOD<2> 14.4C 15.1A<> 15.1B 15.4F
DVOD<3> 14.4C 15.1A<> 15.1B 15.4F
DVOD<4> 14.4C 15.4F
DVOD<5> 14.4C 15.4F
DVOD<6> 14.4C 15.4F
DVOD<7> 14.4C 15.4F
DVOD<8> 14.4C 15.4F
DVOD<9> 14.3C 15.4F
DVOD<10> 14.3C 15.4F
DVOD<11> 14.3C 15.4F
DVODE 14.4C> 15.4A<> 15.4B
DVOHSYNC 14.4C> 15.4F<
DVOVSYNC 14.4C> 15.4F<
FAN_RETURN 11.1G<> 14.1G<> 14.3F
FBAA<0> 3.4B 4.3C 4.3E 5.2C 5.3C
FBAA<12..0> 4.1G<> 4.3C> 4.3E 5.1G<> 5.2C< 5.3E<
FBAA<63..0> 3.4A>
FBAA<1> 3.4B 4.3C 4.3E 5.3C 5.3E
FBAA<2> 3.4B 4.3C 4.3E 5.3C 5.3E
FBAA<3> 3.4B 4.3C 4.3E 5.3C 5.3E
FBAA<4> 3.4B 4.3C 4.3E 5.3C 5.3E
FBAA<5> 3.4B 4.3C 4.3E 5.3C 5.3E
FBAA<6> 3.4B 4.3C 4.3E 5.3C 5.3E
FBAA<7> 3.4B 4.3C 4.3E 5.3C 5.3E
FBAA<8> 3.4B 4.3C 4.3E 5.3C 5.3E
FBAA<9> 3.4B 4.3C 4.3E 5.3C 5.3E
FBAA<10> 3.4B 4.3C 4.3E 5.3C 5.3E
FBAA<11> 3.4B 4.3C 4.3E 5.3C 5.3E
FBAA<12> 3.4B 4.3C 4.3E 5.3C 5.3E
FBABA<0> 3.5B> 4.1G<> 4.4C> 4.4E 5.1G<> 5.4C< 5.4E
FBABA<1> 3.5B> 4.1G<> 4.4C> 4.4E 5.1G<> 5.4C< 5.4E
FBACKE 3.5B> 4.2G<> 4.4C> 4.4E 5.2G<> 5.4C< 5.4E
FBACLK0 3.4D 3.5B> 5.1G<> 5.4C< 5.4E 5.5D
FBACLK0* 3.4D 3.5B> 5.1G<> 5.4C< 5.4E 5.5D
FBACLK1 3.4D 3.5B> 4.1G<> 4.4C< 4.4E 4.5D
FBACLK1* 3.4D 3.5B> 4.1G<> 4.4C< 4.4E 4.5D
FBACS0* 3.5B> 4.1G<> 4.3C< 4.3E 5.1G<> 5.3C< 5.3E
FBACS1* 4.1G<>
FBAD<0> 3.1B 4.1A
FBAD<31..0> 4.1G<>
FBAD<63..0> 3.1A<> 4.1A<>
FBAD<1> 3.1B 4.2A
FBAD<2> 3.1B 4.2A
FBAD<3> 3.1B 4.2A
FBAD<4> 3.1B 4.2A
FBAD<5> 3.1B 4.2A
FBAD<6> 3.1B 4.2A
FBAD<7> 3.1B 4.2A
FBAD<8> 3.1B 4.2A
FBAD<9> 3.1B 4.2A
FBAD<10> 3.1B 4.2A
FBAD<11> 3.1B 4.2A
FBAD<12> 3.1B 4.2A
FBAD<13> 3.1B 4.2A
FBAD<14> 3.1B 4.2A
FBAD<15> 3.1B 4.2A
FBAD<16> 3.1B 4.3A
FBAD<17> 3.1B 4.3A
FBAD<18> 3.1B 4.3A
FBAD<19> 3.1B 4.3A
FBAD<20> 3.2B 4.3A
FBAD<21> 3.2B 4.3A
FBAD<22> 3.2B 4.3A
FBAD<23> 3.2B 4.3A
FBAD<24> 3.2B 4.3A
FBAD<25> 3.2B 4.3A
FBAD<26> 3.2B 4.3A
FBAD<27> 3.2B 4.3A
FBAD<28> 3.2B 4.3A
FBAD<29> 3.2B 4.3A
FBAD<30> 3.2B 4.3A
FBAD<31> 3.2B 4.4A
FBAD<32> 3.2B 5.1A
FBAD<63..32> 5.1A<> 5.1G<>
FBAD<33> 3.2B 5.2A
FBAD<34> 3.2B 5.2A
FBAD<35> 3.2B 5.2A
FBAD<36> 3.2B 5.2A
FBAD<37> 3.2B 5.2A
FBAD<38> 3.2B 5.2A
FBAD<39> 3.2B 5.2A
FBAD<40> 3.2B 5.2A
FBAD<41> 3.2B 5.2A
FBAD<42> 3.2B 5.2A
FBAD<43> 3.2B 5.2A
FBAD<44> 3.2B 5.2A
FBAD<45> 3.2B 5.2A
FBAD<46> 3.2B 5.2A
FBAD<47> 3.2B 5.2A
FBAD<48> 3.2B 5.3A
FBAD<49> 3.2B 5.3A
FBAD<50> 3.2B 5.3A
FBAD<51> 3.2B 5.3A
FBAD<52> 3.2B 5.3A
FBAD<53> 3.2B 5.3A
FBAD<54> 3.2B 5.3A
FBAD<55> 3.2B 5.3A
FBAD<56> 3.2B 5.3A
FBAD<57> 3.2B 5.3A
FBAD<58> 3.2B 5.3A
FBAD<59> 3.2B 5.3A
FBAD<60> 3.2B 5.3A
FBAD<61> 3.2B 5.3A
FBAD<62> 3.2B 5.3A
FBAD<63> 3.2B 5.4A
FBADQM<3..0> 4.1G<>
FBADQM<63..0> 3.3A>
FBADQM<1> 3.3B 4.4A<
FBADQM<2> 3.3B 4.4A<
FBADQM<3> 3.3B 4.4A<
FBADQM<4> 3.3B 5.4A<
FBADQM<7..4> 5.1G<>
FBADQM<5> 3.3B 5.4A<
FBADQM<6> 3.3B 5.4A<
FBADQM<7> 3.3B 5.4A<
FBADQS<7..0> 4.1G<>
FBADQS<63..0> 3.3A<>
FBADQS<1> 3.3B 4.4A<>
FBADQS<2> 3.3B 4.4A<>
FBADQS<3> 3.3B 4.4A<>
FBADQS<4> 3.4B 5.4A<>
FBADQS<7..4> 5.1G<>
FBADQS<5> 3.4B 5.4A<>
FBADQS<6> 3.4B 5.4A<>
FBADQS<7> 3.4B 5.4A<>
FBAQSG<7> 3.4B 5.4A<>
FBARAS* 3.5B> 4.1G<> 4.3C< 4.3E 5.1G<> 5.3C< 5.3E
FBAWE* 3.5B> 4.1G<> 4.3C< 4.3E 5.1G<> 5.3C< 5.3E
FBCA<0> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<12..0> 6.1G<> 6.3C< 6.3E 7.1G<> 7.3C< 7.3E
FBCA<63..0> 3.4E>
FBCA<1> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<2> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<3> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<4> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<5> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<6> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<7> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<8> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<9> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<10> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<11> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCA<12> 3.4F 6.3C 6.3E 7.3C 7.3E
FBCBA<0> 3.5E> 6.1G<> 6.4C< 6.4E 7.1G<> 7.4C< 7.4E
FBCBA<1> 3.5E> 6.1G<> 6.4C< 6.4E 7.1G<> 7.4C< 7.4E
FBCCAS* 3.5E> 6.1G<> 6.3C< 6.3E 7.1G<> 7.3C< 7.3E
FBCCKE 3.5E> 6.2G<> 6.4C< 6.4E 7.2G<> 7.4C< 7.4E
FBCCLK0 3.4G 3.5E> 7.1G<> 7.4C< 7.4E 7.5D
FBCCLK0* 3.4G 3.5E> 7.1G<> 7.4C< 7.4E 7.5D
FBCCLK1 3.4G 3.5E< 6.1G<> 6.4C< 6.4E 6.5D
FBCCLK1* 3.4G 3.5E< 6.1G<> 6.4C< 6.4E 6.5D
FBCCS0* 3.5E> 6.1G<> 6.3C< 6.3E 7.1G<> 7.3C< 7.3E
FBCCS1* 6.1G<>
FBCD<0> 3.1F 6.1A
FBCD<31..0> 6.1G<>
FBCD<63..0> 3.1E<> 6.1A<>
FBCD<1> 3.1F 6.2A
FBCD<2> 3.1F 6.2A
FBCD<3> 3.1F 6.2A
FBCD<4> 3.1F 6.2A
FBCD<5> 3.1F 6.2A
FBCD<6> 3.1F 6.2A
FBCD<7> 3.1F 6.2A
FBCD<8> 3.1F 6.2A
FBCD<9> 3.1F 6.2A
FBCD<10> 3.1F 6.2A
FBCD<11> 3.1F 6.2A
FBCD<12> 3.1F 6.2A
FBCD<13> 3.1F 6.2A
FBCD<14> 3.1F 6.2A
FBCD<15> 3.1F 6.2A
FBCD<16> 3.1F 6.3A
FBCD<17> 3.1F 6.3A
FBCD<18> 3.1F 6.3A
FBCD<19> 3.1F 6.3A
FBCD<20> 3.2F 6.3A
FBCD<21> 3.2F 6.3A
FBCD<22> 3.2F 6.3A
FBCD<23> 3.2F 6.3A
FBCD<24> 3.2F 6.3A
FBCD<25> 3.2F 6.3A
FBCD<26> 3.2F 6.3A
FBCD<27> 3.2F 6.3A
FBCD<28> 3.2F 6.3A
FBCD<29> 3.2F 6.3A
FBCD<30> 3.2F 6.3A
FBCD<31> 3.2F 6.4A
FBCD<32> 3.2F 7.1A
FBCD<63..32> 7.1A<> 7.1G<>
FBCD<33> 3.2F 7.2A
FBCD<34> 3.2F 7.2A
FBCD<35> 3.2F 7.2A
FBCD<36> 3.2F 7.2A
FBCD<37> 3.2F 7.2A
FBCD<38> 3.2F 7.2A
FBCD<39> 3.2F 7.2A
FBCD<40> 3.2F 7.2A
FBCD<41> 3.2F 7.2A
FBCD<42> 3.2F 7.2A
FBCD<43> 3.2F 7.2A
FBCD<44> 3.2F 7.2A
FBCD<45> 3.2F 7.2A
FBCD<46> 3.2F 7.2A
FBCD<47> 3.2F 7.2A
FBCD<48> 3.2F 7.3A
FBCD<49> 3.2F 7.3A
FBCD<50> 3.2F 7.3A
FBCD<51> 3.2F 7.3A
FBCD<52> 3.2F 7.3A
FBCD<53> 3.2F 7.3A
FBCD<54> 3.2F 7.3A
FBCD<55> 3.2F 7.3A
FBCD<56> 3.2F 7.3A
FBCD<57> 3.2F 7.3A
FBCD<58> 3.2F 7.3A
FBCD<59> 3.2F 7.3A
FBCD<60> 3.2F 7.3A
FBCD<61> 3.2F 7.3A
FBCD<62> 3.2F 7.3A
FBCD<63> 3.2F 7.4A
FBCDQM<0> 3.3F 6.4A<
FBCDQM<3..0> 6.1G<>
FBCDQM<63..0> 3.3E>
FBCDQM<1> 3.3F 6.4A<
FBCDQM<2> 3.3F 6.4A<
FBCDQM<3> 3.3F 6.4A<
FBCDQM<4> 3.3F 7.4A<
FBCDQM<7..4> 7.1G<>
FBCDQM<5> 3.3F 7.4A<
FBCDQM<6> 3.3F 7.4A<
FBCDQM<7> 3.3F 7.4A<
FBCDQS<0> 3.3F 6.4A<
FBCDQS<63..0> 3.3E>
FBCDQS<1> 3.3F 6.4A<
FBCDQS<2> 3.3F 6.4A<
FBCDQS<3> 3.3F 6.4A<
FBCDQS<4> 3.4F 7.4A<
FBCDQS<7..4> 7.1G<>
FBCDQS<5> 3.4F 7.4A<
FBCDQS<6> 3.4F 7.4A<
FBCDQS<7> 3.4F 7.4A<
FBCRAS* 3.5E> 6.1G<> 6.3C< 6.3E 7.1G<> 7.3C< 7.3E
FBCWE* 3.5E> 6.1G<> 6.3C< 6.3E 7.1G<> 7.3C< 7.3E
FBVDD 16.1G<>
FBVDD_FB 17.1G<> 17.2C 17.2H
HIDR 17.1G<> 17.2C
HP_12V 17.1A 17.1G<> 17.2G
HP_COMP 17.2C<> 17.2C 17.2G
HP_RT 17.1G<> 17.2B
HP_SS 17.1G<> 17.2B 17.2G
HL_DR 17.1G<> 17.2C 17.2H
I2CA_SCL 8.1D> 9.2A<
I2CA_SDA 8.1D> 9.1A<
I2CB_SCL 8.3D> 10.0D<
I2CB_SCL_C 10.2G> 10.2G> 11.4G<
I2CB_SDA 8.3D> 10.1D<
I2CB_SDA_C 10.2G> 10.2G> 11.4G<
I2CC_SCL 12.3B< 13.1G< 14.4D< 14.4F
I2CC_SDA 12.3A<> 13.2F<> 14.4D<> 14.4F
IFPABPLLVDD 11.1G<> 11.3B
IFPAIVREF 11.1G<> 11.3C
IFPAIOVDD 11.1G<> 11.4B
IFPBIOVDD 11.1G<> 11.4B
IFPCIOVDD 11.1G<> 11.3A
IFPCPLLVDD 11.1G<> 11.3A
IFPCVREF 11.1G<> 11.2A
LOAD_TEST 10.5D> 14.2H<
LODR 17.1G<> 17.2C
LO_DR 17.1G<> 17.2C 17.2H
MFBAD<0> 4.1B 4.2C
MFBAD<31..0> 4.1G<>
MFBAD<63..0> 4.1B
MFBAD<1> 4.2B 4.2C
MFBAD<2> 4.2B 4.2C
MFBAD<3> 4.2B 4.2C
MFBAD<4> 4.2B 4.2C
MFBAD<5> 4.2B 4.2C
MFBAD<6> 4.2B 4.2C
MFBAD<7> 4.2B 4.2C
MFBAD<8> 4.2B 4.2C
MFBAD<9> 4.2B 4.2C
MFBAD<10> 4.2B 4.2C
MFBAD<11> 4.2B 4.2C
MFBAD<12> 4.2B 4.2C
MFBAD<13> 4.2B 4.2C
MFBAD<14> 4.2B 4.2C
MFBAD<15> 4.2B 4.2C
MFBAD<16> 4.3C 4.3B
MFBAD<17> 4.3C 4.3B
MFBAD<18> 4.3C 4.3B
MFBAD<19> 4.3C 4.3B
MFBAD<20> 4.3C 4.3B
MFBAD<21> 4.3C 4.3B
MFBAD<22> 4.3C 4.3B
MFBAD<23> 4.3C 4.3B
MFBAD<24> 4.3C 4.3B
MFBAD<25> 4.3C 4.3B
MFBAD<26> 4.3C 4.3B
MFBAD<27> 4.3C 4.3B
MFBAD<28> 4.3C 4.3B
MFBAD<29> 4.3C 4.3B
MFBAD<30> 4.3C 4.3B
MFBAD<31> 4.3C 4.4B
MFBAD<32> 5.1B 5.2C
MFBAD<63..32> 5.1B 5.1G<>
MFBAD<33> 5.2B 5.2C
MFBAD<34> 5.2B 5.2C
MFBAD<35> 5.2B 5.2C
MFBAD<36> 5.2B 5.2C
MFBAD<37> 5.2B 5.2C
MFBAD<38> 5.2B 5.2C
MFBAD<39> 5.2B 5.3C
MFBAD<40> 5.3B 5.3C
MFBAD<41> 5.3B 5.3C
MFBAD<42> 5.3B 5.3C
MFBAD<43> 5.3B 5.3C
MFBAD<44> 5.3B 5.3C
MFBAD<45> 5.3B 5.3C
MFBAD<46> 5.3B 5.3C
MFBAD<47> 5.3B 5.3C
MFBAD<48> 5.3C 5.3B
MFBAD<49> 5.3C 5.3B
MFBAD<50> 5.3C 5.3B
MFBAD<51> 5.3C 5.3B
MFBAD<52> 5.3C 5.3B
MFBAD<53> 5.3C 5.3B
MFBAD<54> 5.3C 5.3B
MFBAD<55> 5.3C 5.3B
MFBAD<56> 5.3C 5.3B
MFBAD<57> 5.3C 5.3B
MFBAD<58> 5.3C 5.3B
MFBAD<59> 5.3C 5.3B
MFBAD<60> 5.3C 5.3B
MFBAD<61> 5.3C 5.3B
MFBAD<62> 5.3C 5.3B
MFBAD<63> 5.3C 5.4B
MFBADQM<0> 4.2C 4.4B
MFBADQM<3..0> 4.1G<>
MFBADQM<1> 4.2C 4.4B
MFBADQM<2> 4.2C 4.4B
MFBADQM<3> 4.2C 4.4B
MFBADQM<4> 5.2C 5.4B
MFBADQM<7..4> 5.1G<>
MFBADQM<5> 5.2C 5.4B
MFBADQM<6> 5.2C 5.4B
MFBADQM<7> 5.2C 5.4B
MFBADQS<0> 4.2C 4.4B
MFBADQS<3..0> 4.1G<>
MFBADQS<1> 4.2C 4.4B
MFBADQS<2> 4.2C 4.4B
MFBADQS<3> 4.2C 4.4B
MFBADQS<4> 5.2C 5.4B
MFBADQS<7..4> 5.1G<>
MFBADQS<5> 5.2C 5.4B
MFBADQS<6> 5.2C 5.4B
MFBADQS<7> 5.2C 5.4B
MFBCD<0> 6.3B 6.3C
MFBCD<31..0> 6.1G<>
MFBCD<63..0> 6.1B
MFBCD<1> 6.3B 6.3C
MFBCD<2> 6.3B 6.3C
MFBCD<3> 6.3B 6.3C
MFBCD<4> 6.3B 6.3C
MFBCD<5> 6.3B 6.3C
MFBCD<6> 6.3B 6.3C
MFBCD<7> 6.3B 6.3C
MFBCD<8> 6.3B 6.3C
MFBCD<9> 6.3B 6.3C
MFBCD<10> 6.3B 6.3C
MFBCD<11> 6.3B 6.3C
MFBCD<12> 6.3B 6.3C
MFBCD<13> 6.3B 6.3C
MFBCD<14> 6.3B 6.3C
MFBCD<15> 6.3B 6.3C
MFBCD<16> 6.3B 6.3C
MFBCD<17> 6.3C 6.3B
MFBCD<18> 6.3C 6.3B
MFBCD<19> 6.3C 6.3B
MFBCD<20> 6.3C 6.3B
MFBCD<21> 6.3C 6.3B
MFBCD<22> 6.3C 6.3B
MFBCD<23> 6.3C 6.3B
MFBCD<24> 6.3C 6.3B
MFBCD<25> 6.3C 6.3B
MFBCD<26> 6.3C 6.3B
MFBCD<27> 6.3C 6.3B
MFBCD<28> 6.3C 6.3B
MFBCD<29> 6.3C 6.3B
MFBCD<30> 6.3C 6.3B
MFBCD<31> 6.3C 6.4B
MFBCD<32> 7.1B 7.1G<>
MFBCD<33> 7.2B 7.2C
MFBCD<34> 7.2B 7.2C
MFBCD<35> 7.2B 7.2C
MFBCD<36> 7.2B 7.2C
MFBCD<37> 7.2B 7.2C
MFBCD<38> 7.2B 7.2C
MFBCD<39> 7.2B 7.2C
MFBCD<40> 7.2B 7.2C
MFBCD<41> 7.2B 7.2C
MFBCD<42> 7.2B 7.2C
MFBCD<43> 7.2B 7.2C
MFBCD<44> 7.2B 7.2C
MFBCD<45> 7.2B 7.2C
MFBCD<46> 7.2B 7.2C
MFBCD<47> 7.2B 7.2C
MFBCD<48> 7.2C 7.3B
MFBCD<49> 7.2C 7.3B
MFBCD<50> 7.2C 7.3B
MFBCD<51> 7.2C 7.3B
MFBCD<52> 7.2C 7.3B
MFBCD<53> 7.2C 7.3B
MFBCD<54> 7.2C 7.3B
MFBCD<55> 7.2C 7.3B
MFBCD<56> 7.2C 7.3B
MFBCD<57> 7.2C 7.3B
MFBCD<58> 7.2C 7.3B
MFBCD<59> 7.2C 7.3B
MFBCD<60> 7.2C 7.3B
MFBCD<61> 7.2C 7.3B
MFBCD<62> 7.2C 7.3B
MFBCD<63> 7.2C 7.4B
MFBCDQM<0> 6.2C 6.4B
MFBCDQM<3..0> 6.1G<>
MFBCDQM<1> 6.2C 6.4B
MFBCDQM<2> 6.2C 6.4B
MFBCDQM<3> 6.2C 6.4B
MFBCDQM<4> 7.2C 7.4B
MFBCDQM<7..4> 7.1G<>
MFBCDQM<5> 7.2C 7.4B
MFBCDQM<6> 7.2C 7.4B
MFBCDQM<7> 7.2C 7.4B
MFBCDQS<0> 6.2C 6.4B
MFBCDQS<3..0> 6.1G<>
MFBCDQS<1> 6.2C 6.4B
MFBCDQS<2> 6.2C 6.4B
MFBCDQS<3> 6.2C 6.4B
MFBCDQS<4> 7.2C 7.4B
MFBCDQS<7..4> 7.1G<>
MFBCDQS<5> 7.2C 7.4B
MFBCDQS<6> 7.2C 7.4B
MFBCDQS<7> 7.2C 7.4B
MINDN_ON 12.2H> 13.2G>
MINDN_OUT 10.1G<> 10.4C> 13.2B<
MINDN_RBOUT 10.1G<> 10.5C> 13.2B<
MINDN_V_CVBSIN 12.2H> 13.2B<
MINDN_V_CVBSOUT 10.1G<> 10.4C> 13.2F<
NVSB_VREFCG 2.5G<>
NVVDD 16.1G<>
OCSET 17.1G<> 17.2C
PCIAD<0> 2.1C 2.1D
PCIAD<31..0> 2.1D 2.4G<>

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BKT1 BRACKET 17
C1 C 2
C2 C 2
C3 C 2
C4 C 2
C5 C 2
C6 C 2
C7 C 2
C8 C 2
C9 C 2
C10 C 2
C11 C 2
C12 C 2
C13 C 2
C14 C 2
C15 C 2
C16 C 2
C17 C 2
C18 C 2
C19 C 2
C20 C 2
C21 C 2
C22 C 2
C23 C 2
C24 C 14
C25 C 2
C26 C 2
C27 C 2
C28 C 2
C29 C 2
C30 C 2
C31 C 2
C32 C 2
C33 C 14
C34 C 2
C35 C 2
C36 C 2
C37 C 2
C38 C 2
C39 C 2
C40 C 2
C41 C 2
C42 C 2
C43 C 2
C44 C 2
C45 C 2
C46 C 2
C47 C 2
C48 C 2
C49 C 2
C50 C 2
C51 C 3
C52 C 3
C53 C 2
C54 C 3
C55 C 2
C56 C 3
C57 C 3
C58 C 3
C59 C 3
C60 C 3
C61 C 2
C62 C 2
C63 C 2
C64 C 2
C65 C 2
C66 C 2
C67 C 3
C68 C 3
C69 C 3
C70 C 3
C71 C 3
C72 C 3
C73 C 3
C75 C 3
C76 C 3
C77 C 3
C78 C 3
C79 C 3
C80 C 3
C82 C 4
C83 C 4
C84 C 4
C85 C 4
C86 C 4
C87 C 4
C88 C 4
C89 C 4
C90 C 4
C91 C 4
C92 C 4
C93 C 4
C94 C 4
C95 C 4
C96 C 4
C97 C 4
C98 C 4
C99 C 4
C100 C 4
C101 C 4
C102 C 4
C103 C 4
C104 C 4
C105 C 4
C106 C 4
C107 C 4
C108 C 4
C109 C 4
C110 C 4
C111 C 4
C112 C 4
C113 C 4
C114 C 4
C115 C 4
C116 C 4
C117 C 4
C118 C 4
C119 C 4
C120 C 5
C121 C 5
C122 C 5
C123 C 5
C124 C 5
C125 C 5
C126 C 5
C127 C 5
C128 C 5
C129 C 5
C130 C 5
C131 C 5
C132 C 5
C133 C 5
C134 C 5
C135 C 5
C136 C 5
C137 C 5
C138 C 5
C139 C 5
C140 C 5
C141 C 5
C142 C 5
C143 C 5
C144 C 5
C145 C 5
C146 C 5
C147 C 5
C148 C 5
C149 C 5
C150 C 5
C151 C 5
C152 C 5
C153 C 5
C154 C 5
C155 C 5
C156 C 5
C157 C 5
C158 C 6
C159 C 6
C160 C 6
C161 C 6
C162 C 6
C163 C 6
C164 C 6
C165 C 6
C166 C 6
C167 C 6
C168 C 6
C169 C 6
C170 C 6
C171 C 6
C172 C 6
C173 C 6
C174 C 6
C175 C 6
C176 C 6
C177 C 6
C178 C 6
C179 C 6
C180 C 6
C181 C 6
C182 C 6
C183 C 6
C184 C 6
C185 C 6
C186 C 6
C187 C 6
C188 C 6
C189 C 6
C190 C 6
C191 C 6
C192 C 6
C193 C 6
C194 C 6
C195 C 6
C196 C 7
C197 C 7
C198 C 7
C199 C 7
C200 C 7
C201 C 7
C202 C 7
C203 C 7
C204 C 7
C205 C 7
C206 C 7
C207 C 7
C208 C 7
C209 C 7
C210 C 7
C211 C 7
C212 C 7
C213 C 7
C214 C 7
C215 C 7
C216 C 7
C217 C 7
C218 C 7
C219 C 7
C220 C 7
C221 C 7
C222 C 7
C223 C 7
C224 C 7
C225 C 7
C226 C 7
C227 C 7
C228 C 7
C229 C 7
C230 C 7
C231 C 7
C232 C 7
C233 C 7
C234 C 8
C235 C 8
C236 C 8
C237 C 8
C238 C 8
C239 C 8
C240 C 8
C241 C 8
C242 C 8
C243 C 8
C244 C 8
C245 C 8
C246 C 8
C247 C 8
C248 C 8
C249 C 9
C250 C 9
C251 C 9
C252 C 9
C253 C 9
C254 C 9
C255 C 9
C256 C 9
C257 C 9
C258 C 9
C259 C 9
C260 C 9
C261 C 9
C262 C 9
C263 C 9
C264 C 10
C265 C 10
C266 C 10
C267 C 10
C268 C 10
C269 C 10
C270 C 10
C271 C 10
C272 C 10
C273 C 10
C274 C 10
C275 C 10
C276 C 10
C277 C 10
C278 C 10
C279 C 10
C280 C 10
C281 C 10
C282 C 11
C283 C 11
C284 C 11
C285 C 11
C286 C 11
C287 C 11
C288 C 11
C289 C 11
C290 C 11
C291 C 11
C292 C 11
C293 C 11
C294 C 11
C295 C 11
C296 C 11
C297 C 12
C298 C 12
C299 C 12
C300 C 12
C301 C 12
C302 C 12
C303 C 12
C304 C 12
C305 C 12
C306 C 12
C307 C 12
C308 C 12
C309 C 12
C310 C 12
C311 C 12
C312 C 12
C313 C 12
C314 C 12
C315 C 12
C316 C 12
C317 C 12
C318 C 12
C319 C 12
C320 C 12
C321 C 12
C322 C 12
C323 C 12
C324 C 12
C325 C 12
C326 C 12
C327 C 12
C328 C 12
C329 C 12
C330 C 12
C331 C 12
C332 C 12
C333 C 12
C334 C 12
C335 C 12
C336 C 13
C337 C 13
C338 C 13
C339 C 13
C340 C 13
C341 C 13
C342 C 13
C343 C 13
C344 C 13
C345 C 13
C346 C 13
C347 C 13
C348 C 13
C349 C 13
C350 C 13
C351 C 13
C352 C 13
C353 C 13
C354 C 13
C355 C 13
C356 C 13
C357 C 13
C358 C 13
C359 C 13
C360 C 13
C361 C 13
C362 C 13
C363 C 13
C364 C 14
C366 C 14
C368 C 14
C369 C 14
C371 C 14
C372 C 14
C373 C 14
C374 C_POL 16
C375 C_POL 16
C376 C_POL 16
C377 C 16
C378 C_POL 16
C379 C_POL 16
C380 C_POL 16
C381 C 16
C382 C 16
C383 C 16
C384 C 16
C385 C 16
C386 C_POL 16
C387 C 16
C388 C_POL 16
C389 C_POL 16
C390 C 16
C391 C_POL 16
C392 C_POL 16
C393 C 16
C394 C 16
C395 C 16
C396 C 16
C397 C 16
C398 C 16
C399 C_POL 16
C400 C 16
C401 C 16
C402 C 16
C403 C 16
C404 C 16
C405 C 16
C406 C 16
C407 C 16
C408 C 16
C409 C_POL 16
C410 C_POL 16
C411 C 16
C412 C_POL 16
C413 C_POL 16
C414 C 17
C415 C 17
C416 C 10
C417 C 10
C418 C 10
C419 C 14
C420 C 14
C421 C 13
C422 C 15
C424 C_POL 16
C425 C_POL 16
C426 C 15
C427 C_POL 16
C428 C_POL 16
C429 C 17
C430 C 17
C431 C 17
C432 C 8
C434 C 17
C436 C 17
C438 C 17
C439 C 17
C440 C_POL 17
C441 C 17
C442 C 17
C443 C 17
C444 C_POL 17
C446 C_POL 17
C448 C 17
C447 C 17
C448 C 17
C566 C 2
C567 C 2
C569 C 2
C570 C 2
C572 C 2
C574 C 2
C575 C 2
C580 C 2
C591 C 2
C724 C 2
CN1 CON_AGP 2
D1 D_3PIN_AC9
D2 D_3PIN_AC9
D3 D_3PIN_AC9
D4 D_3PIN_AC9
D5 D_3PIN_AC9
D6 D_3PIN_AC9
D7 D_3PIN_AC9
D8 D_3PIN_AC10
D9 D_3PIN_AC10
D10 D_3PIN_AC10
D11 D_3PIN_AC10
D12 D_3PIN_AC10
D13 D_3PIN_AC10
D14 D_3PIN_AC10
D15 D_3PIN_AC11
D16 D_3PIN_AC13
D17 D_3PIN_AC13
D18 D_3PIN_AC13
D19 D_3PIN_AC13
D20 D_3PIN_AC13
D21 D_3PIN_AC13
D22 D_3PIN_AC13
D23 D_3PIN_AC13
D24 D 14
D25 D_SCHOTTKY16
D26 D 16
D27 D_SCHOTTKY16
D28 D 16
D29 D_SCHOTTKY16
D30 D_3PIN_AC13
D31 D_3PIN_AC13
D33 D 17
D34 D_SCHOTTKY17
F1 F_FOLYSW 17
J1 CON_DSUBSHD9
J2 CON_DSUBSHD10
J3 CON_DVI_I 11
J4 CON_MINIDIN_9 13
J5 HDR_DX4 13
J6 HDR_DX2 14
J7 HDR_DX2 14
L1 L 9
L2 L 9
L3 L 9
L4 L 9
L5 L 9
L6 L 9
L7 L 9
L8 L 9
L9 L 10
L10 L 10
L11 L 10
L12 L 10
L13 L 10
L14 L 10
L15 L 10
L16 L 10
L17 L 13
L18 L 13
L19 L 13
L20 L 13
L21 L 13
L22 L 13
L23 L 13
L24 L 13
L25 L 16
L26 L 16
L27 L 17
LB1 L 2
LB2 L 3
LB3 L 8
LB4 L 8
LB5 L 8
LB6 L 9
LB7 L 9
LB8 L 10
LB9 L 10
LB10 L 10
LB11 L 10
LB12 L 11
LB13 L 11
LB14 L 11
LB15 L 11
LB16 L 12
LB17 L 12
LB18 L 12
LB19 L 13
LB20 L 13
LB21 L 16
LB22 L 17
LB23 L 13
LB24 L 15
ME1 HEATSINK 17
ME2 ME2_SCREW17
ME3 ME2_SCREW17
ME4 ME2_SCREW17
ME5 ME2_SCREW17
Q1 Q_FET_N_ENH 2
Q2 Q_PNP 2
Q3 Q_FET_N_ENH 2
Q4 Q_FET_N_ENH 8
Q5 Q_NPN 11
Q6 Q_NPN 11
Q7 Q_PNP 11
Q8 Q_FET_N_ENH 14
Q9 Q_FET_N_ENH 16
Q10 Q_FET_N_ENH 16
Q11 Q_FET_N_ENH 16
Q12 Q_FET_N_ENH 17
R1 R 2
R2 R 2
R3 R 2

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PCIAD<1> 2.1C 2.1D
PCIAD<2> 2.1C 2.1D
PCIAD<3> 2.1C 2.1D
PCIAD<4> 2.1C 2.1D
PCIAD<5> 2.1C 2.1D
PCIAD<6> 2.1C 2.1D
PCIAD<7> 2.1C 2.1D
PCIAD<8> 2.1C 2.1D
PCIAD<9> 2.1C 2.1D
PCIAD<10> 2.1C 2.1D
PCIAD<11> 2.1C 2.1D
PCIAD<12> 2.1C 2.1D
PCIAD<13> 2.1C 2.1D
PCIAD<14> 2.1C 2.1D
PCIAD<15> 2.2C 2.2D
PCIAD<16> 2.2C 2.2D
PCIAD<17> 2.2C 2.2D
PCIAD<18> 2.2C 2.2D
PCIAD<19> 2.2C 2.2D
PCIAD<20> 2.2C 2.2D
PCIAD<21> 2.2C 2.2D
PCIAD<22> 2.2C 2.2D
PCIAD<23> 2.2C 2.2D
PCIAD<24> 2.2C 2.2D
PCIAD<25> 2.2C 2.2D
PCIAD<26> 2.2C 2.2D
PCIAD<27> 2.2C 2.2D
PCIAD<28> 2.2C 2.2D
PCIAD<29> 2.2C 2.2D
PCIAD<30> 2.2C 2.2D
PCIAD<31> 2.2C 2.2D
PCICBE<0> 2.2C 2.2D
PCICBE<3..0> 2.2C 2.4G>
PCICBE<1> 2.2C 2.2D
PCICBE<2> 2.2C 2.2D
PCICBE<3> 2.2C 2.2D
PCICLK 2.2C 2.4G>
PCIDEVSEL 2.3C 2.4G>
PCIFRAME 2.2C 2.4G>
PCIGNT 2.3C 2.4G>
PCIINTA 2.3C 2.4G>
PCINTB 2.4G>
PCIIRDY 2.3C 2.4G>
PCIPAR 2.3C 2.4G>
PCIREQ 2.2C 2.4G>
PCIRST* 2.2C 2.4G>
PCISTOP 2.3C 2.4G>
PCITRDY 2.3C 2.4G>
PHASE 17.1G> 17.2C
PLLVDD 8.1G> 8.4C
RESET_BUF* 12.3B< 14.5C>
ROMA14 14.2C> 15.3F 15.3A<> 15.3B 15.3F< 15.4F<
ROMA15 14.2C> 15.3F 15.3F< 15.4A<> 15.4B 15.4F<
ROMCS* 14.2C> 15.3F 15.3F< 15.4G>
SEL_2ND_DEV 8.4B< 10.2A< 14.3A>
STEREO 8.4D> 13.4F<
STRAP<0> 14.4C> 15.2A<> 15.2B
STRAP<1> 14.4C> 15.2A<> 15.2B
STRAP<2> 14.5C> 15.2A<> 15.2B
STRAP<3> 14.5C> 15.2A<> 15.2B
SW_5V 16.1G<> 16.3G 16.4C
SW_12V 16.1G<> 16.3H 16.4D
SW_COMP 16.1G<> 16.4D
SW_FB 16.1G<> 16.3H 16.4D
THERM 14.1G<> 14.2F 14.4F
THERM* 14.1G<> 14.2F 14.4F
TMDSPLL_ADJ 16.2F 16.2G<>
TMDS_BACK 11.1G<> 11.3F
VDINT_ON 12.1A< 13.4A>
VDINT_CVBSIN 12.2A< 13.5A>
VDINT_Y_CVBSIN 12.2A< 13.4A>
VIPD<0> 12.3D 14.2C 15.3G
VIPD<7..0> 12.3B< 14.1C<> 14.2D<> 15.3H<>
VIPD<1> 12.3D 14.2C 15.3G
VIPD<2> 12.3D 14.2C 15.2A<> 15.3B 15.4G
VIPD<3> 12.3D 14.2C 15.4G
VIPD<4> 12.3D 14.2C 15.4G
VIPD<5> 12.3D 14.2C 15.4G
VIPD<6> 12.3D 14.2C 15.3A<> 15.3B 15.4G
VIPD<7> 12.3D 14.2C 15.4G
VIPHAD<0> 14.2C> 15.4G<
VIPHAD<1> 14.2C> 15.4G<
VIPHCTL 14.2D< 15.2A<> 15.2B 15.2F 15.3F>
VIPPCLK 12.4B> 14.1C<> 14.2D<
XTALIN 8.1G<> 8.5C
XTALOUT 8.1G<> 8.5D

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R4	R	2
R5	R	2
R6	R	2
R7	R	2
R8	R	2
R9	R	2
R10	R	2
R11	R	2
R12	R	2
R13	R	2
R14	R	2
R15	R	2
R16	R	2
R17	R	2
R18	R	2
R19	R	2
R20	R	3
R21	R	3
R22	R	3
R23	R	3
R24	R	3
R25	R	3
R26	R	16
R27	R	3
R28	R	4
R29	R	4
R30	R	4
R31	R	17
R32	R	17
R33	R	4
R34	R	4
R35	R	17
R36	R	17
R37	R	4
R38	R	4
R39	R	4
R40	R	5
R41	R	5
R42	R	5
R43	R	17
R44	R	17
R45	R	5
R46	R	5
R47	R	17
R48	R	17
R49	R	5
R50	R	5
R51	R	5
R52	R	6
R53	R	6
R54	R	6
R55	R	17
R56	R	17
R57	R	17
R58	R	17
R59	R	6
R60	R	6
R61	R	6
R62	R	2
R63	R	6
R64	R	6
R65	R	7
R66	R	7
R67	R	7
R68	R	17
R69	R	17
R70	R	17
R71	R	17
R72	R	7
R73	R	7
R74	R	7
R75	R	7
R76	R	7
R77	R	8
R78	R	8
R79	R	8
R80	R	8
R81	R	8
R82	R	8
R83	R	8
R84	R	8
R85	R	8
R86	R	8
R87	R	8
R88	R	8
R89	R	8
R90	R	8
R91	R	8
R92	R	8
R93	R	8
R94	R	9
R95	R	9
R96	R	9
R97	R	9
R98	R	9
R99	R	9
R100	R	9
R101	R	9
R102	R	9
R103	R	9
R104	R	9
R105	R	9
R106	R	10
R107	R	10
R108	R	10
R109	R	10
R110	R	10
R111	R	10
R112	R	10
R113	R	10
R114	R	10
R115	R	10
R116	R	10

R117	R	10
R118	R	10
R119	R	10
R120	R	10
R121	R	10
R122	R	10
R123	R	10
R124	R	10
R125	R	10
R126	R	11
R127	R	11
R128	R	11
R129	R	11
R130	R	11
R131	R	11
R132	R	11
R133	R	11
R134	R	11
R135	R	11
R136	R	11
R137	R	11
R138	R	11
R139	R	11
R140	R	11
R141	R	11
R142	R	11
R143	R	11
R144	R	11
R145	R	11
R146	R	11
R147	R	11
R148	R	11
R149	R	11
R150	R	11
R151	R	12
R152	R	15
R153	R	12
R154	R	12
R155	R	13
R156	R	13
R157	R	13
R158	R	13
R159	R	13
R160	R	13
R161	R	13
R162	R	13
R163	R	13
R164	R	13
R165	R	13
R166	R	14
R167	R	14
R168	R	14
R169	R	14
R170	R	14
R171	R	14
R172	R	14
R173	R	14
R174	R	14
R175	R	14
R176	R	14
R177	R	14
R178	R	14
R179	R	14
R180	R	14
R181	R	16
R182	R	16
R183	R	16
R184	R	16
R185	R	16
R186	R	16
R187	R	16
R188	R	16
R189	R	16
R190	R	16
R191	R	16
R192	R	16
R193	R	16
R194	R	16
R195	R	16
R196	R	16
R197	R	16
R198	L	16
R199	R	16
R200	R	16
R201	R	16
R202	R	16
R203	R	16
R204	R	16
R205	R	16
R206	L	16
R207	R	16
R208	R	10
R209	R	10
R210	R	15
R211	R	15
R212	R	15
R213	R	15
R214	R	15
R215	R	15
R216	R	15
R217	R	15
R218	R	15
R219	R	15
R220	R	15
R221	R	15
R222	R	15
R223	R	15
R224	R	15
R225	R	15
R226	R	15
R227	R	15
R228	R	15
R229	R	15

R230	R	15
R231	R	15
R232	R	15
R233	R	11
R234	R	15
R235	R	3
R239	R	14
R240	R	14
R241	R	15
R242	R	13
R243	R	13
R244	R	13
R245	R	13
RS48	R	2
RS81	R	2
RP1	R_PAK	4
RP2	R_PAK	4
RP3	R_PAK	4
RP4	R_PAK	4
RP5	R_PAK	4
RP6	R_PAK	4
RP7	R_PAK	4
RP8	R_PAK	4
RP9	R_PAK	4
RP10	R_PAK	5
RP11	R_PAK	5
RP12	R_PAK	5
RP13	R_PAK	5
RP14	R_PAK	5
RP15	R_PAK	5
RP16	R_PAK	5
RP17	R_PAK	5
RP18	R_PAK	5
RP19	R_PAK	4
RP20	R_PAK	5
RP21	R_PAK	6
RP22	R_PAK	6
RP23	R_PAK	6
RP24	R_PAK	6
RP25	R_PAK	6
RP26	R_PAK	6
RP27	R_PAK	6
RP28	R_PAK	6
RP29	R_PAK	6
RP30	R_PAK	6
RP31	R_PAK	7
RP32	R_PAK	7
RP33	R_PAK	7
RP34	R_PAK	7
RP35	R_PAK	7
RP36	R_PAK	7
RP37	R_PAK	7
RP38	R_PAK	7
RP39	R_PAK	7
RP40	R_PAK	7
TP1	TESTPOINT	17
TP2	TESTPOINT	17
TP3	TESTPOINT	17
TP4	TESTPOINT	16
TP5	TESTPOINT	16
TP6	TESTPOINT	16
TP7	TESTPOINT	16
TP8	TESTPOINT	16
TP9	TESTPOINT	16
U1	U_GPU_DDR2M64X2_V1.2.B1116	
U2	U_M64M_SD_DDR_4_8MX16I5	
U3	U_M64M_SD_DDR_4_8MX16I4	
U4	U_M64M_SD_DDR_4_8MX16I4	
U5	U_M64M_SD_DDR_4_8MX16I5	
U6	U_M64M_SD_DDR_4_8MX16I6	
U7	U_M64M_SD_DDR_4_8MX16I7	
U8	U_M64M_SD_DDR_4_8MX16I7	
U9	U_M64M_SD_DDR_4_8MX16I6	
U10	U_TEMP_ADI03214I	
U11	U_ANG_2IN16	
U12	U_SW_ANA_3S710	
U13	U_VDEC_SAA7114X12	
U14	U_M0M_FL_SER_128K16I15	
U15	U_M0M_FL_SER_128K16I15	
U16	U_VREG_3PIN16	
U17	U_SWREG_ISL6529I16	
U18	U_VREG_3PIN16	
U19	U_VREG_5PIN16	
U20	U_SWREG_SC3610I16	
U21	U_AND_2IN13	
U22	U_SWREG_LM2622I17	
U23	U_SWREG_SC2612I17	
U24	U_M0M_ROM_128K0I15	
Y1	XTAL	8
Y2	XTAL	12

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