P360-A00 Base Design

P360-A00, G92, 16Mx32 GDDR3 (900MHz),TV(OPTION)
DVI-I-DL, DVI-I-DL

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V186-1.0 Base on P360

1.PAGE11: ADD VGA display connector
2.PAGE12: Move IFP C/D HMDI to page 13
3.PAGE13: Unused DACB Interface, ADD IFP C/D HMDI interface
4.PAGE15: Use I2CC for HDMI control, add GPIO10/14 for HDMI control
5.PAGE18:Add FM1~FM6

V186-1.1 Base on V186-1.0

V186-1.1 Base on V186-1.0 remove the reference place of the 6.1 mil RGB signal.

V186-1.2 Base on V186-1.1

V186-1.2 Base on V186-1.1 change PCB color from RED to Coffee

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SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10360-base-000	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0050	600-10360-0050-000	P360 G92-287 512MB GDDR3 16Mx32 DVI-I+DVI-I
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3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview

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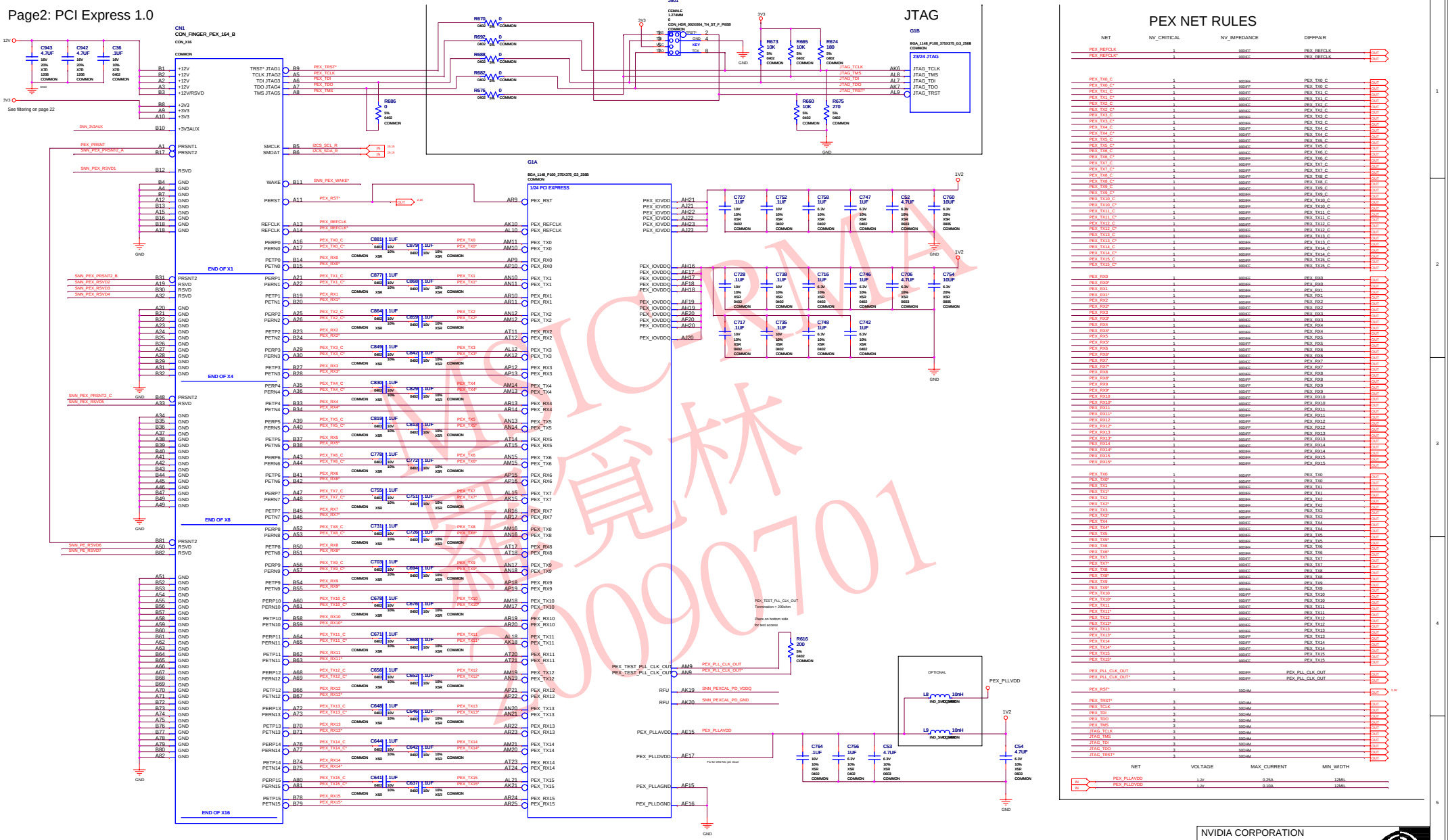

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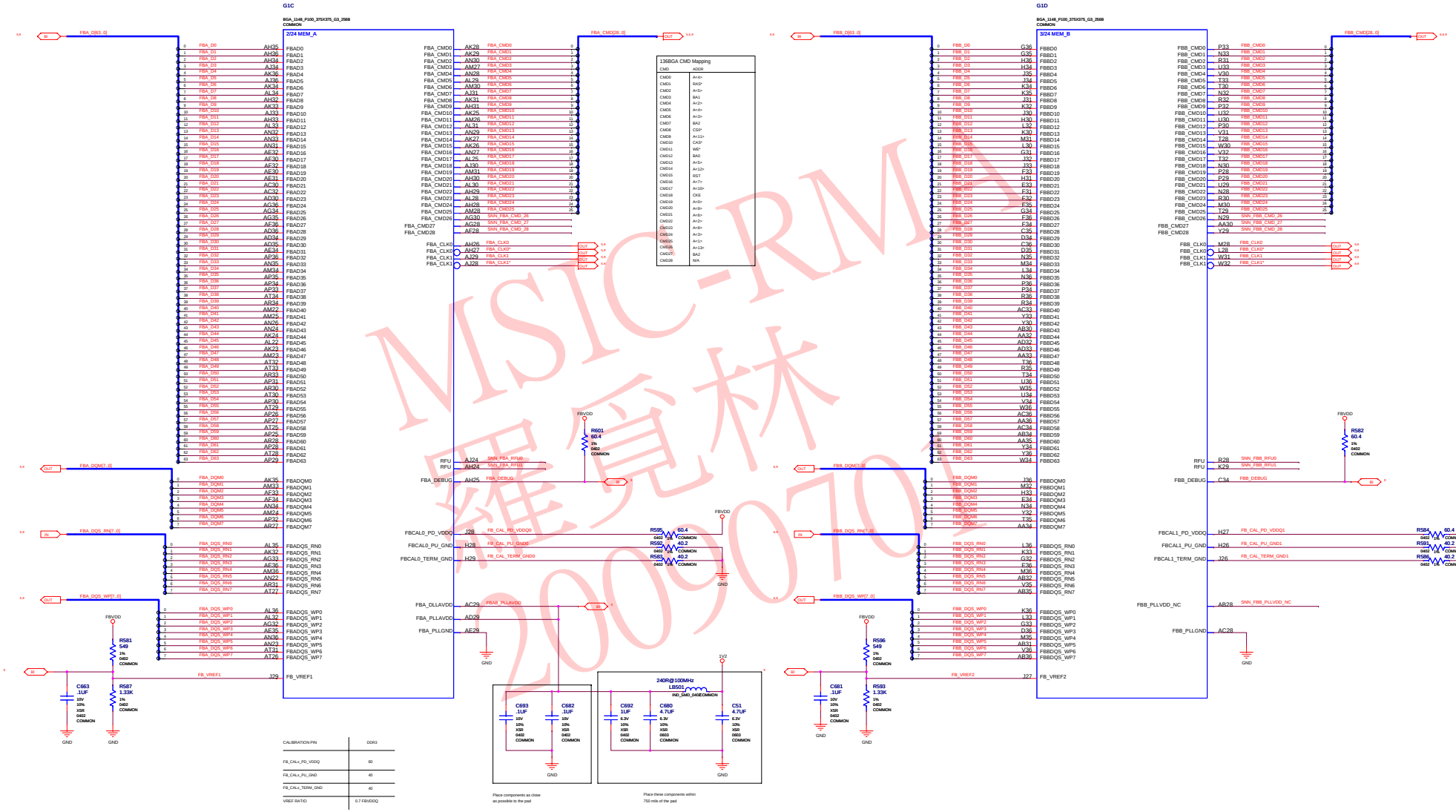
Page3: MEMORY: GPU Partition A/B



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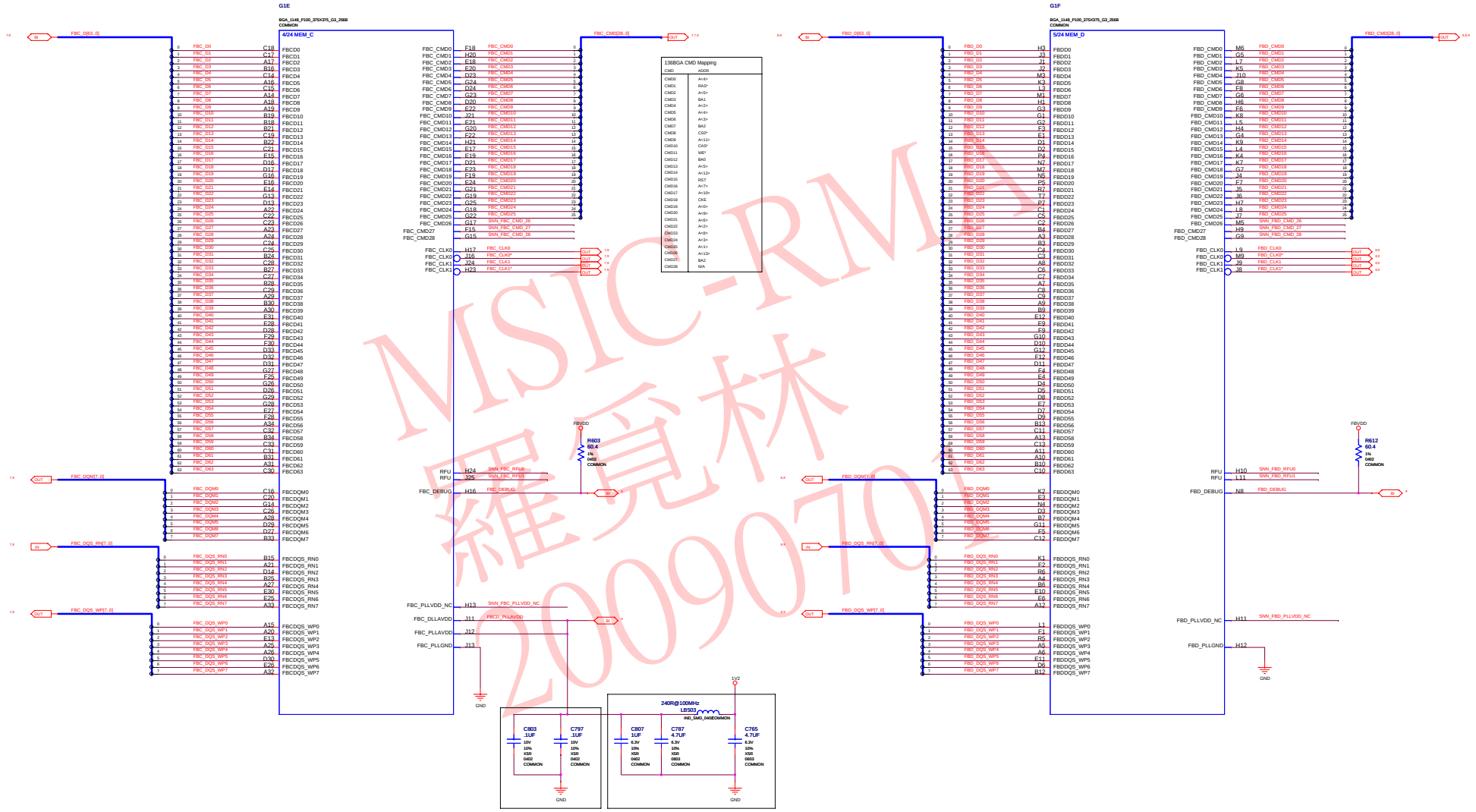
Page4: MEMORY: GPU Partition C/D



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PAGE DETAIL	MEMORY: GPU Partition C/D
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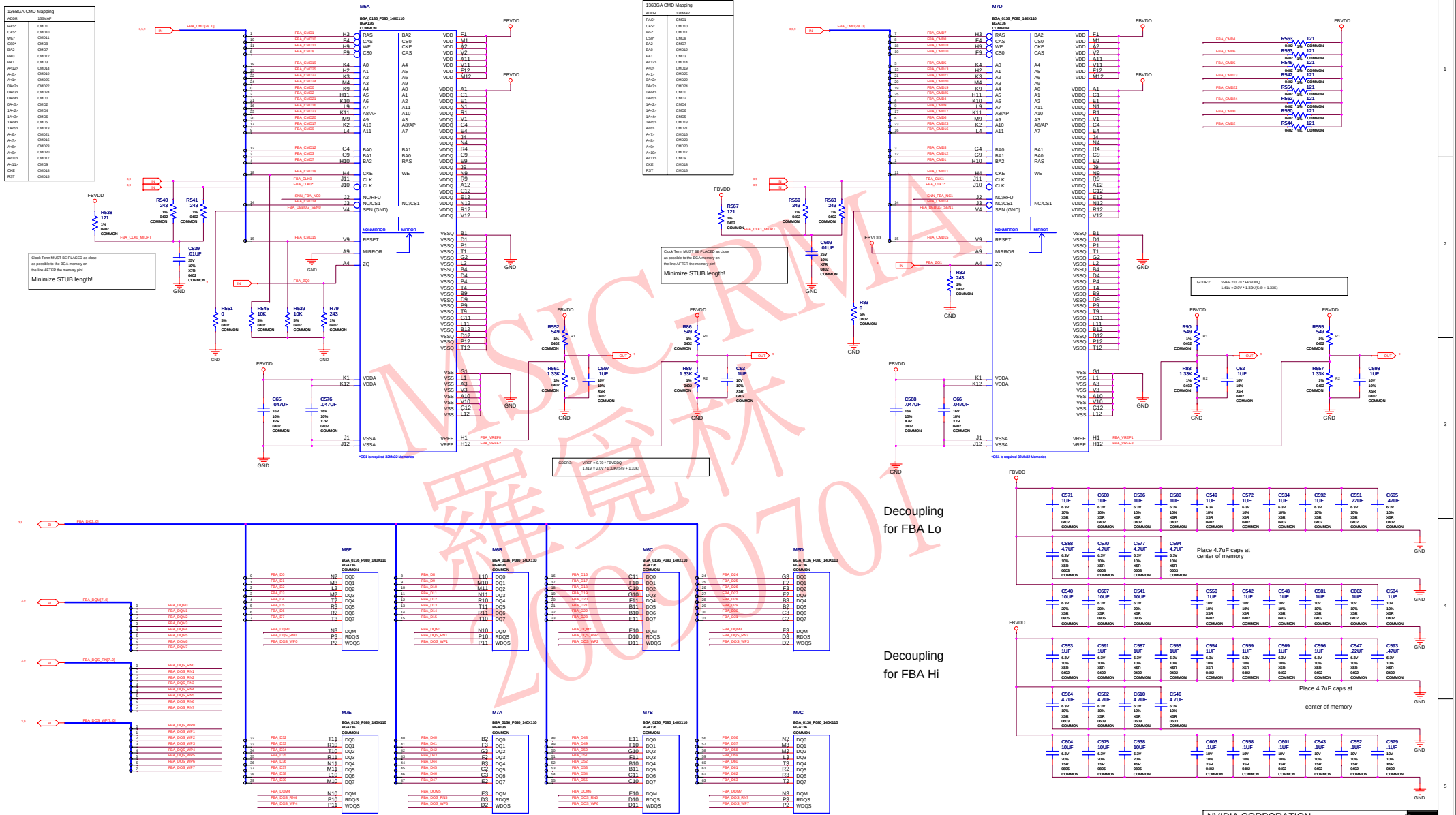
Page5: FBA Partition



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PAGE DETAIL	FBA Partition

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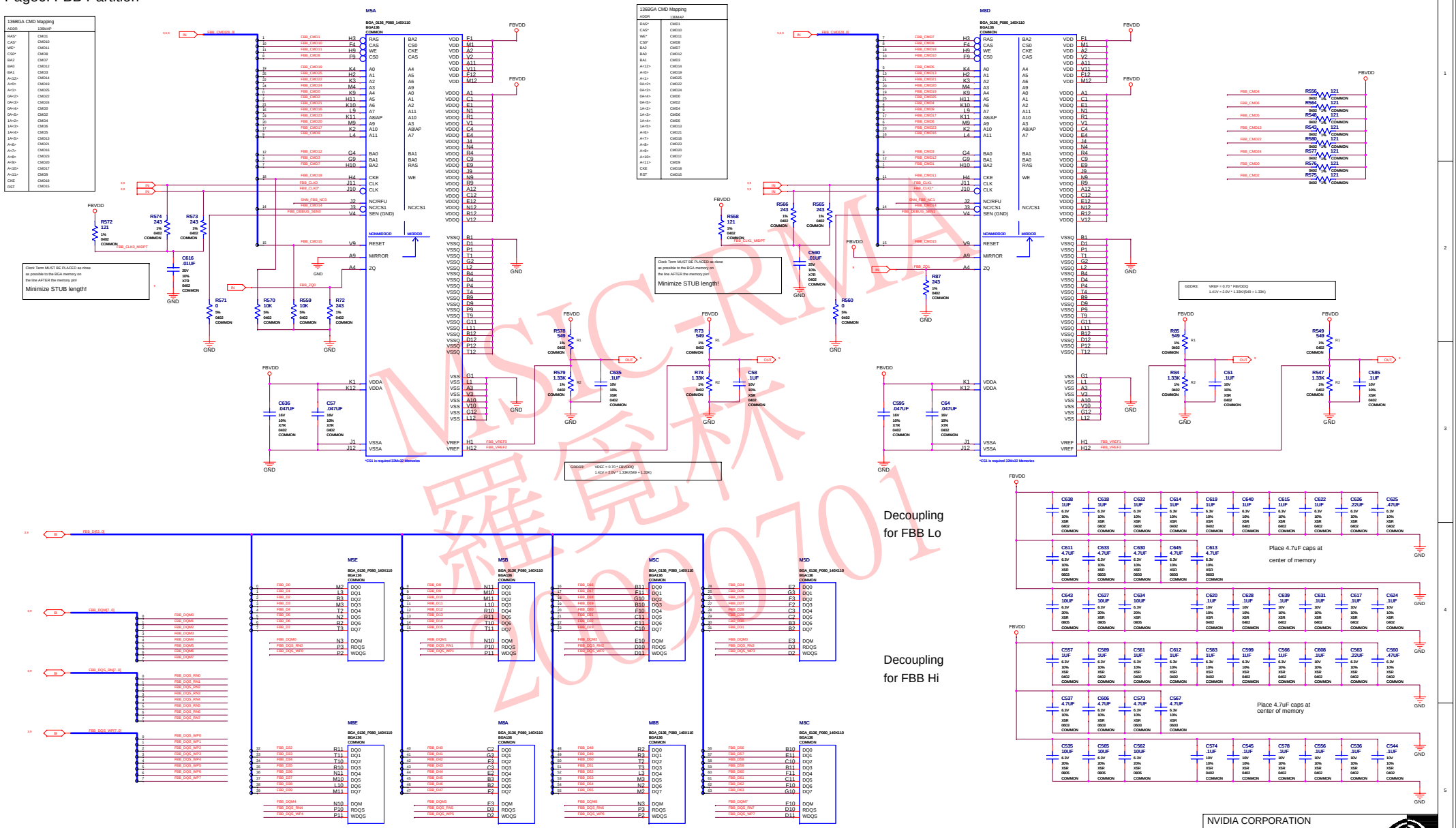
Page6: FBB Partition



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PAGE DETAIL	FBB Partition

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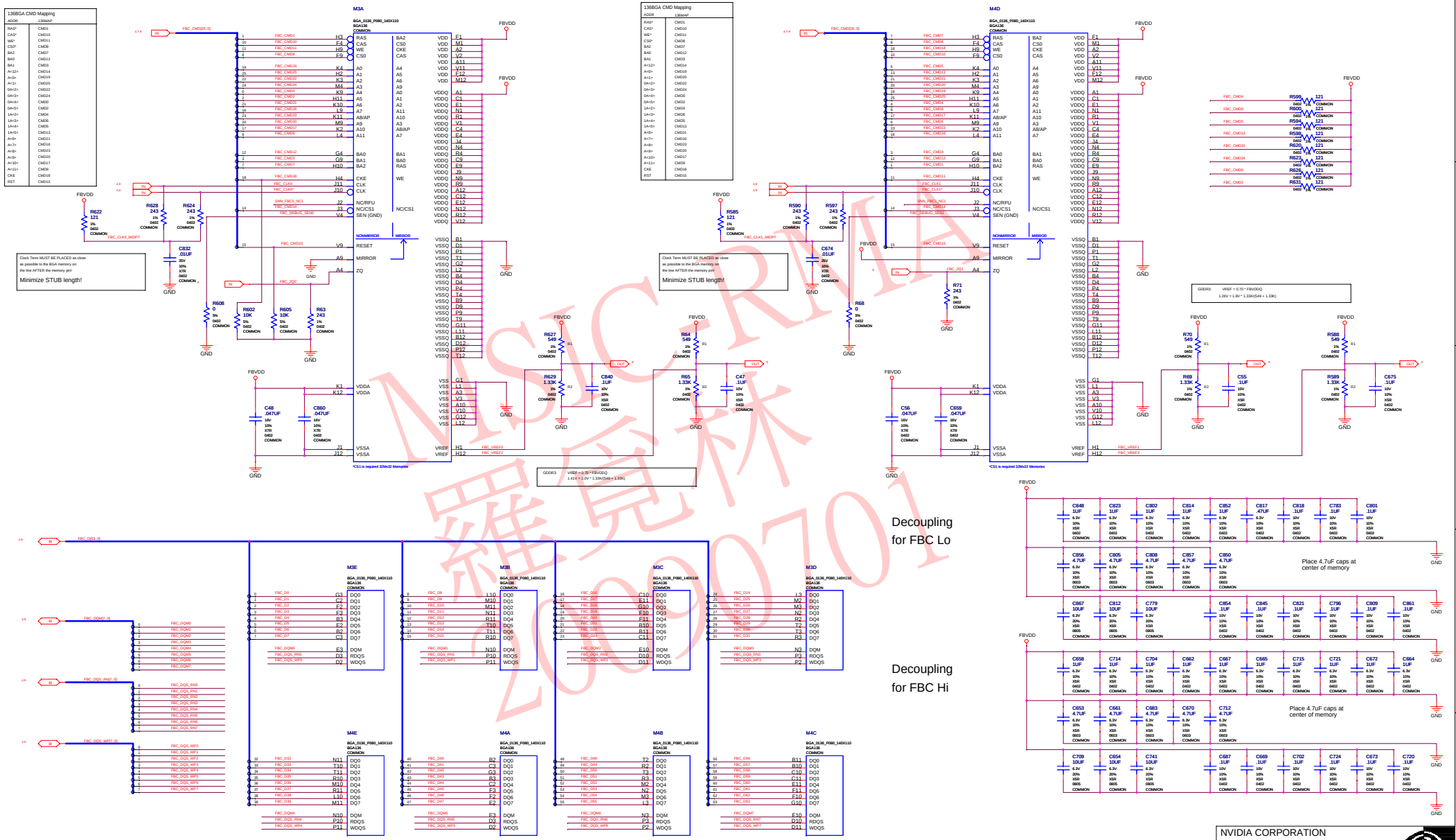
Page7: FBC Partition



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PAGE DETAIL	FBC Partition

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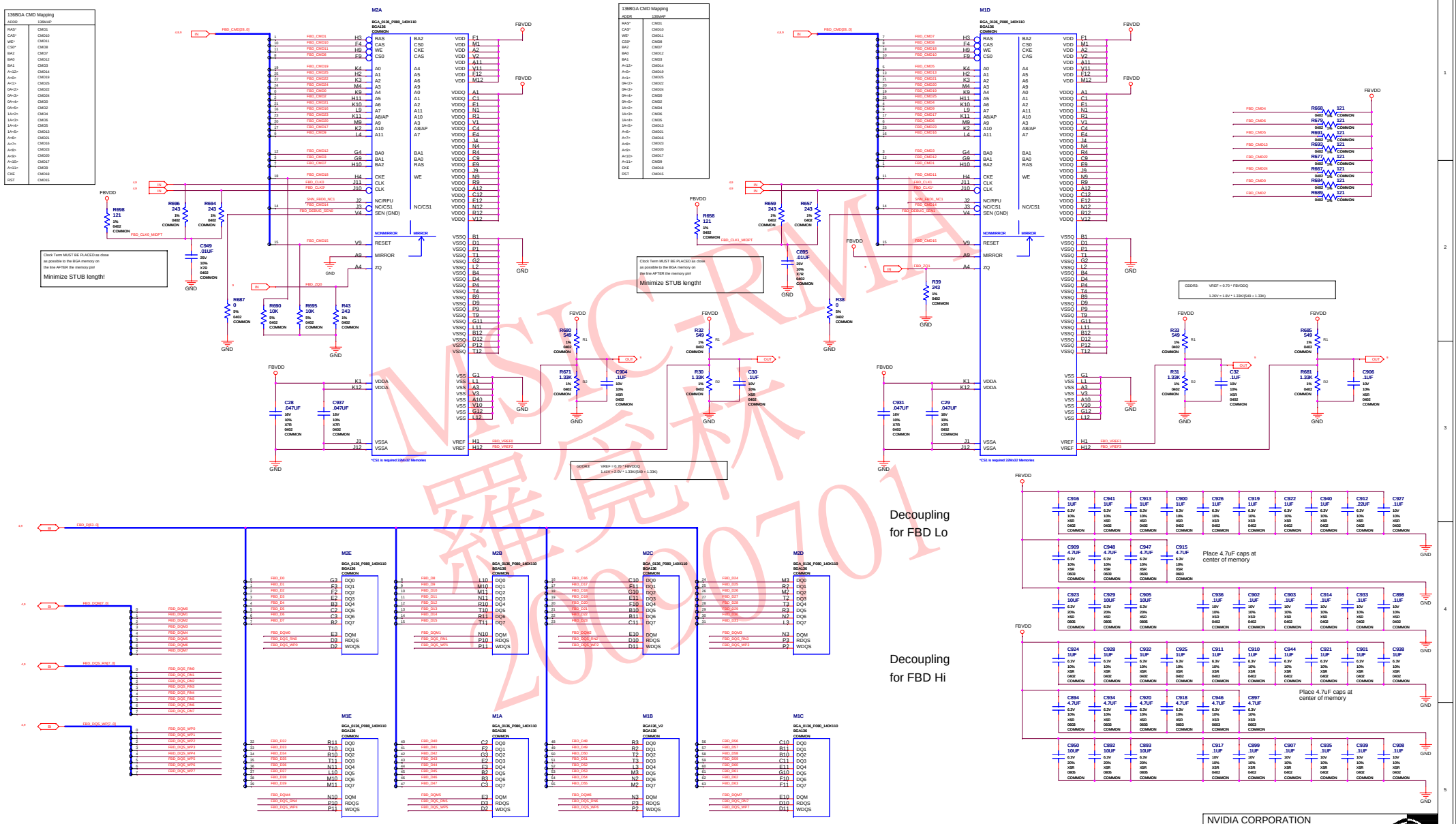
Page8: FBD Partition



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PAGE DETAIL	FBD Partition

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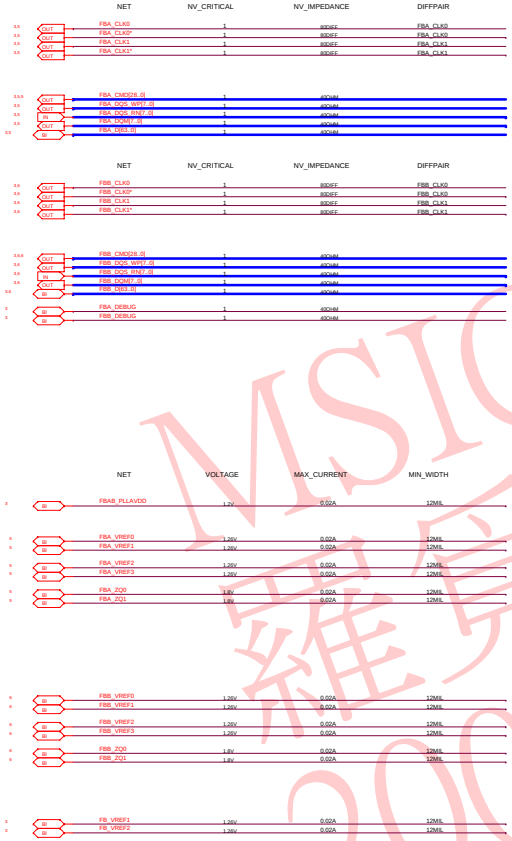
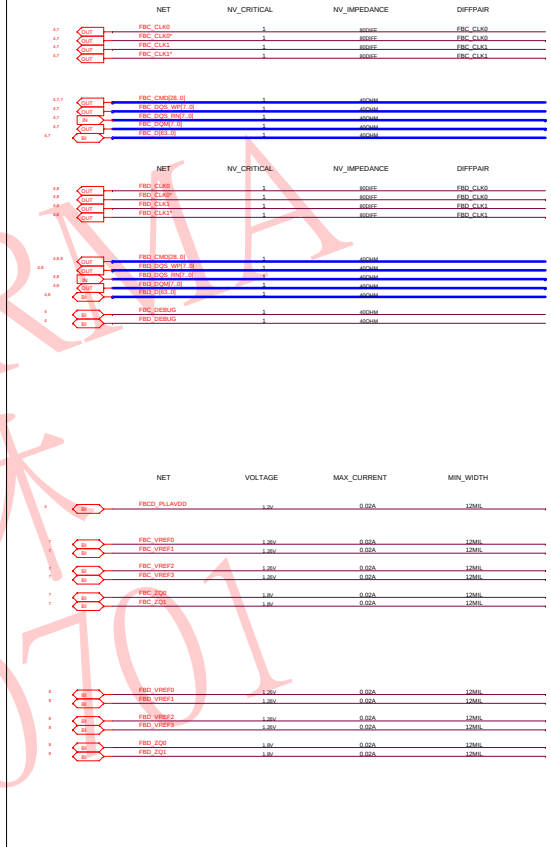
NAME		DATE	22-JAN-2009

Page9: FrameBuffer Net Rules

NET RULES for FrameBuffer A/B



NET RULES for FrameBuffer C/D



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PAGE DETAIL	FrameBuffer Net Rules

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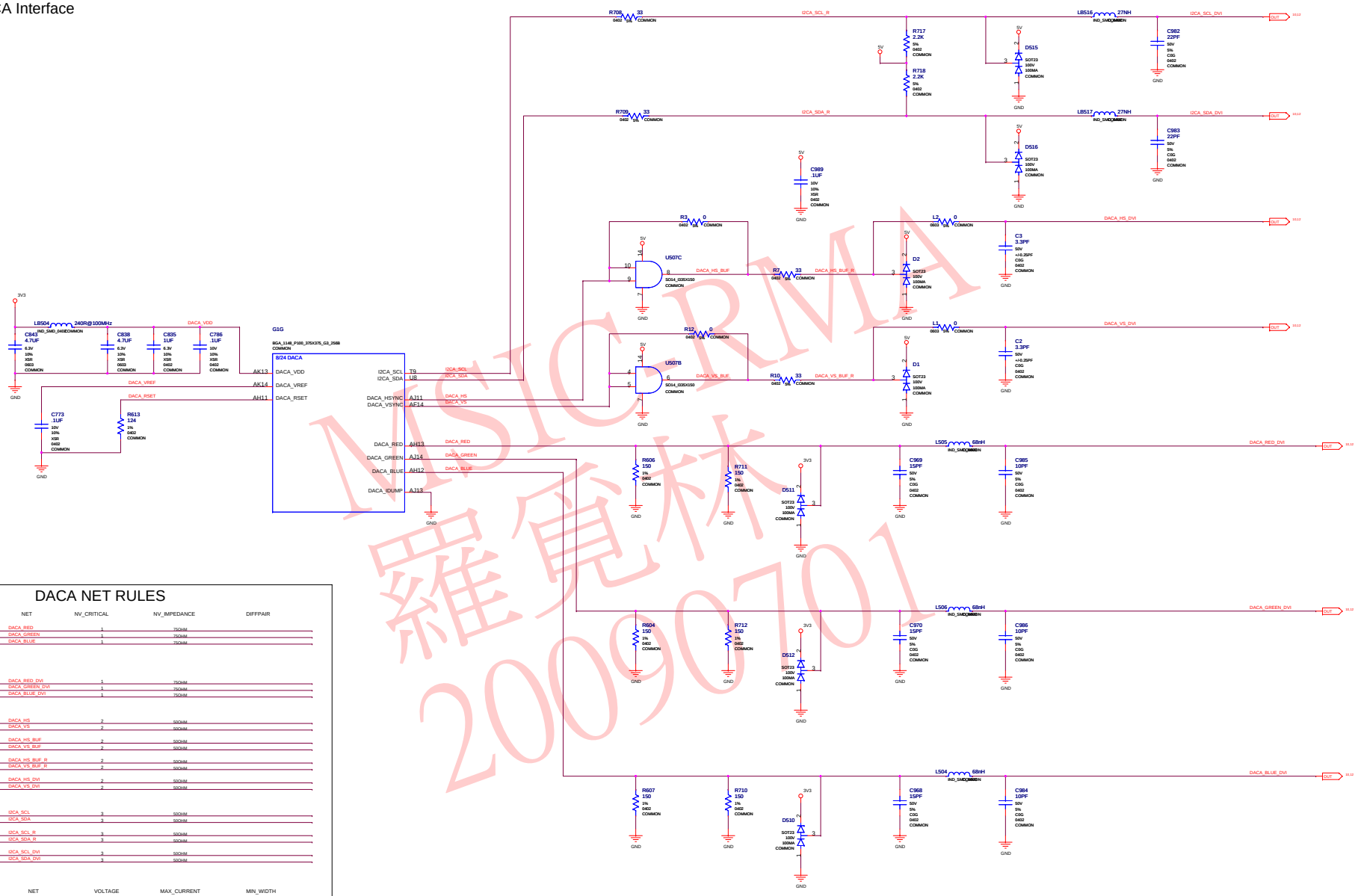
Page10: DACA Interface



DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACA_RED	1	75OHM	
DACA_GREEN	1	75OHM	
DACA_BLUE	1	75OHM	
DACA_RED_DVI	1	75OHM	
DACA_GREEN_DVI	1	75OHM	
DACA_BLUE_DVI	1	75OHM	
DACA_HS	2	50OHM	
DACA_VS	2	50OHM	
DACA_HS_BUF	2	50OHM	
DACA_VS_BUF	2	50OHM	
DACA_HS_BUF_R	2	50OHM	
DACA_VS_BUF_R	2	50OHM	
DACA_HS_DVI	2	50OHM	
DACA_VS_DVI	2	50OHM	
I2CA_SCL	3	50OHM	
I2CA_SDA	3	50OHM	
I2CA_SCL_R	3	50OHM	
I2CA_SDA_R	3	50OHM	
I2CA_SCL_DVI	3	50OHM	
I2CA_SDA_DVI	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACA_VREF			12MIL
DACA_RSET			12MIL
DACA_VDD	3.3V	0.100A	18MIL

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PAGE DETAIL	DACA Interface

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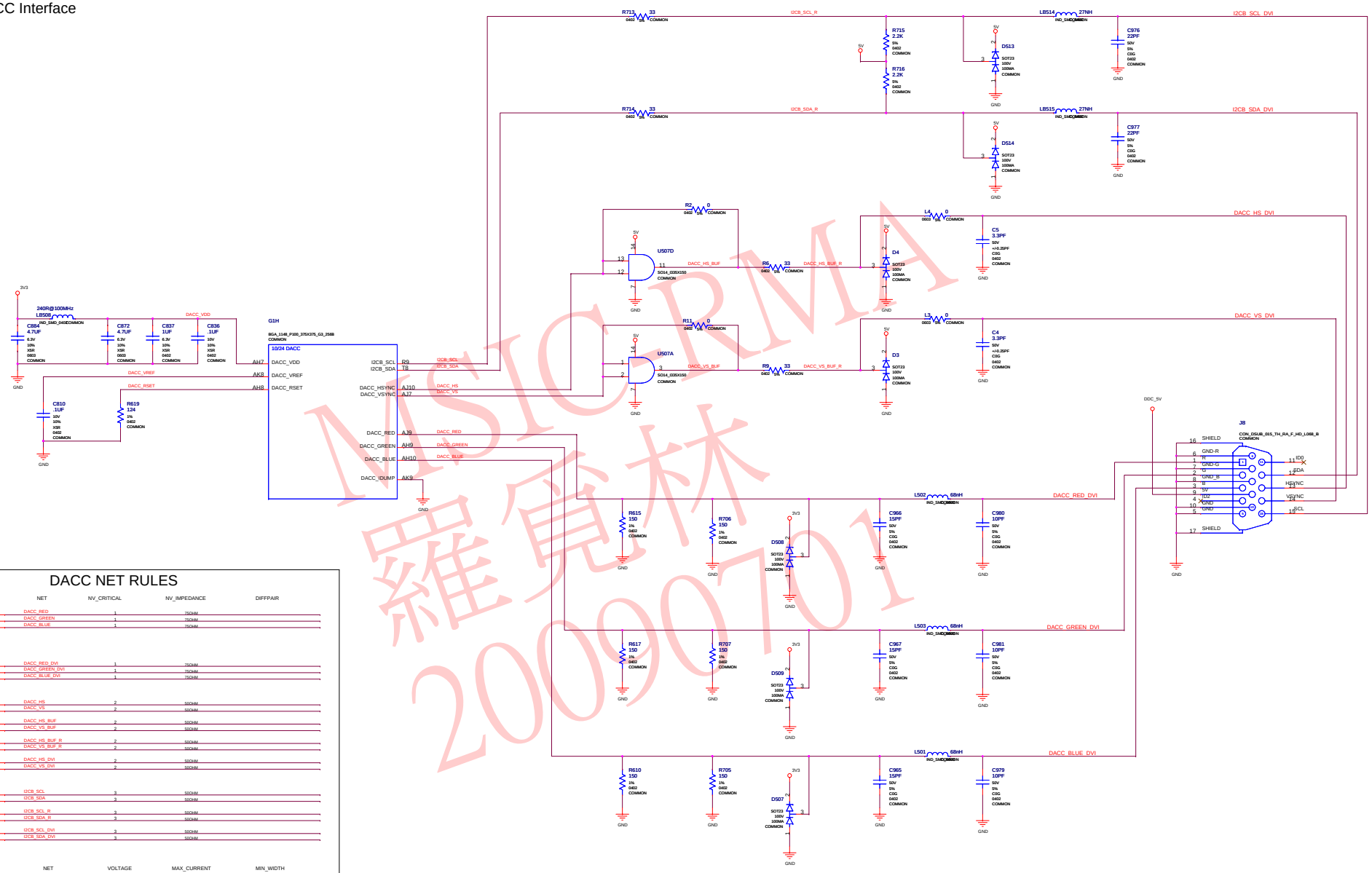
Page11: DACC Interface



DACC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACC_RED	1	75OHM	
DACC_GREEN	1	75OHM	
DACC_BLUE	1	75OHM	
DACC_RED_DVI	1	75OHM	
DACC_GREEN_DVI	1	75OHM	
DACC_BLUE_DVI	1	75OHM	
DACC_HS	2	50OHM	
DACC_VS	2	50OHM	
DACC_HS_BUF	2	50OHM	
DACC_VS_BUF	2	50OHM	
DACC_HS_BUF_R	2	50OHM	
DACC_VS_BUF_R	2	50OHM	
DACC_HS_DVI	2	50OHM	
DACC_VS_DVI	2	50OHM	
I2CB_SCL	3	50OHM	
I2CB_SDA	3	50OHM	
I2CB_SCL_R	3	50OHM	
I2CB_SDA_R	3	50OHM	
I2CB_SCL_DVI	3	50OHM	
I2CB_SDA_DVI	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACC_VREF			12MIL
DACC_RSET			12MIL
DACC_VDD	3.3V	0.100A	18MIL

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PAGE DETAIL	DACC Interface

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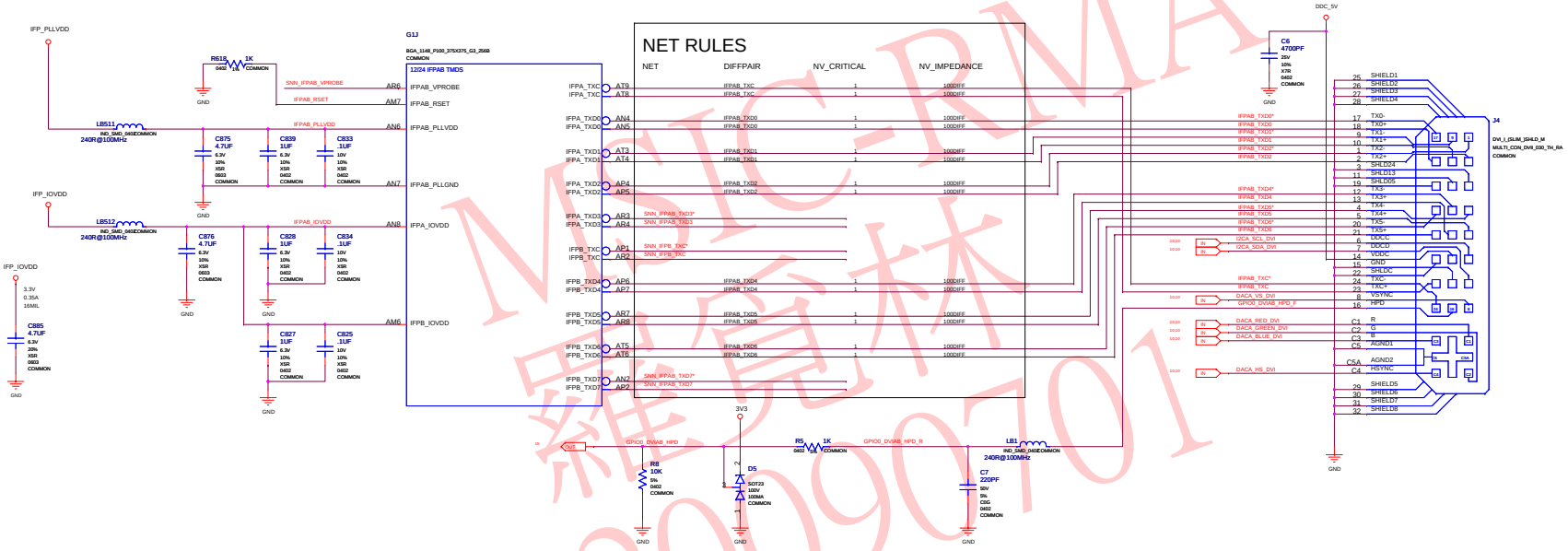
Page12: IFP A/B DVI Interface

IFPABCD NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RSET			12MIL
GPIO0_DVIAB_HPD_F	3	50OHM	
GPIO0_DVIAB_HPD_R	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLLVDD	1.8V	0.03A	16MIL
IFPAB_IOVDD	3.3V	0.09A	16MIL



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PAGE DETAIL	IFP A/B and C/D Interface

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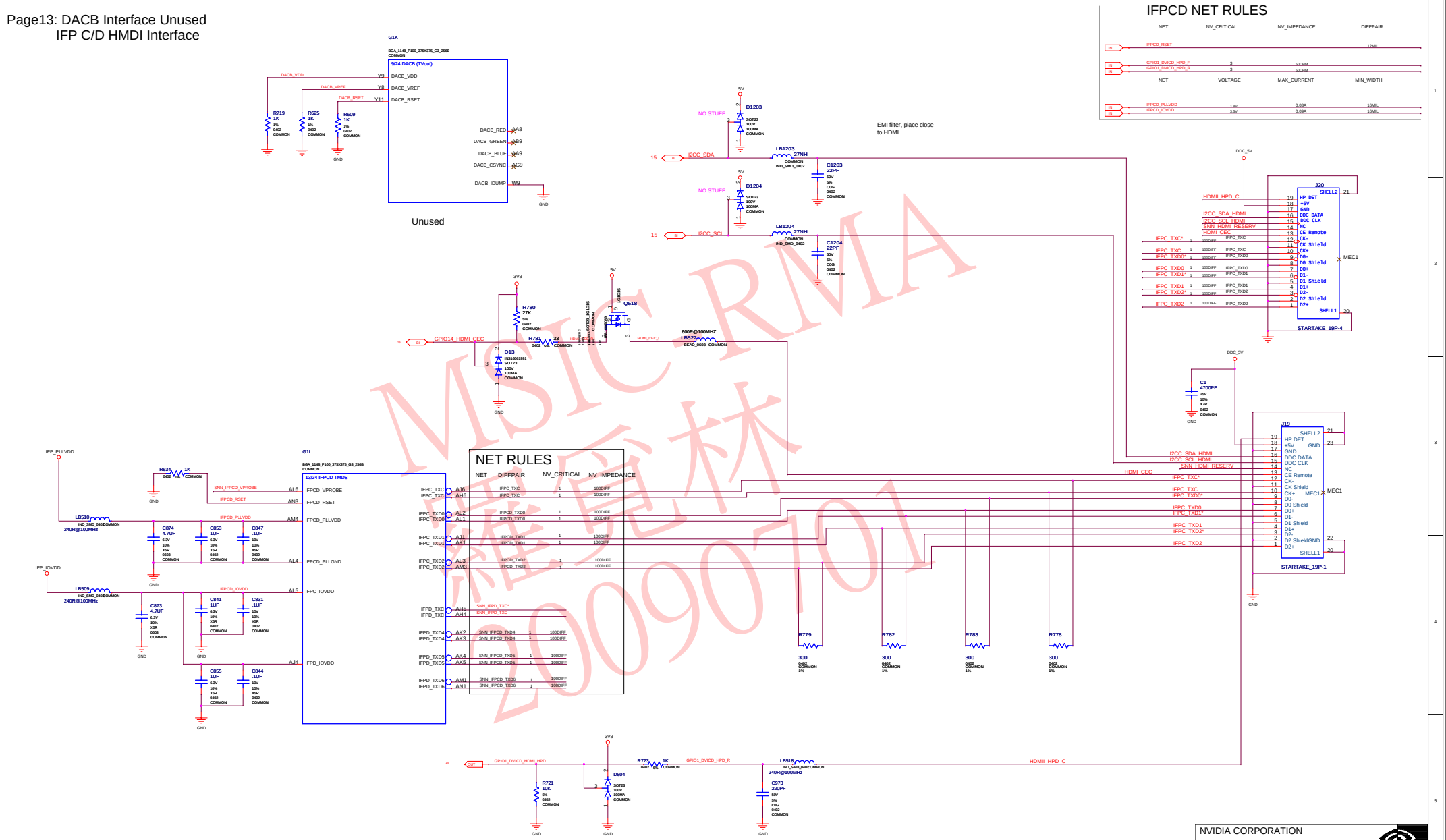
Page13: DACB Interface Unused
IFP C/D HMDI Interface



ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB Interface

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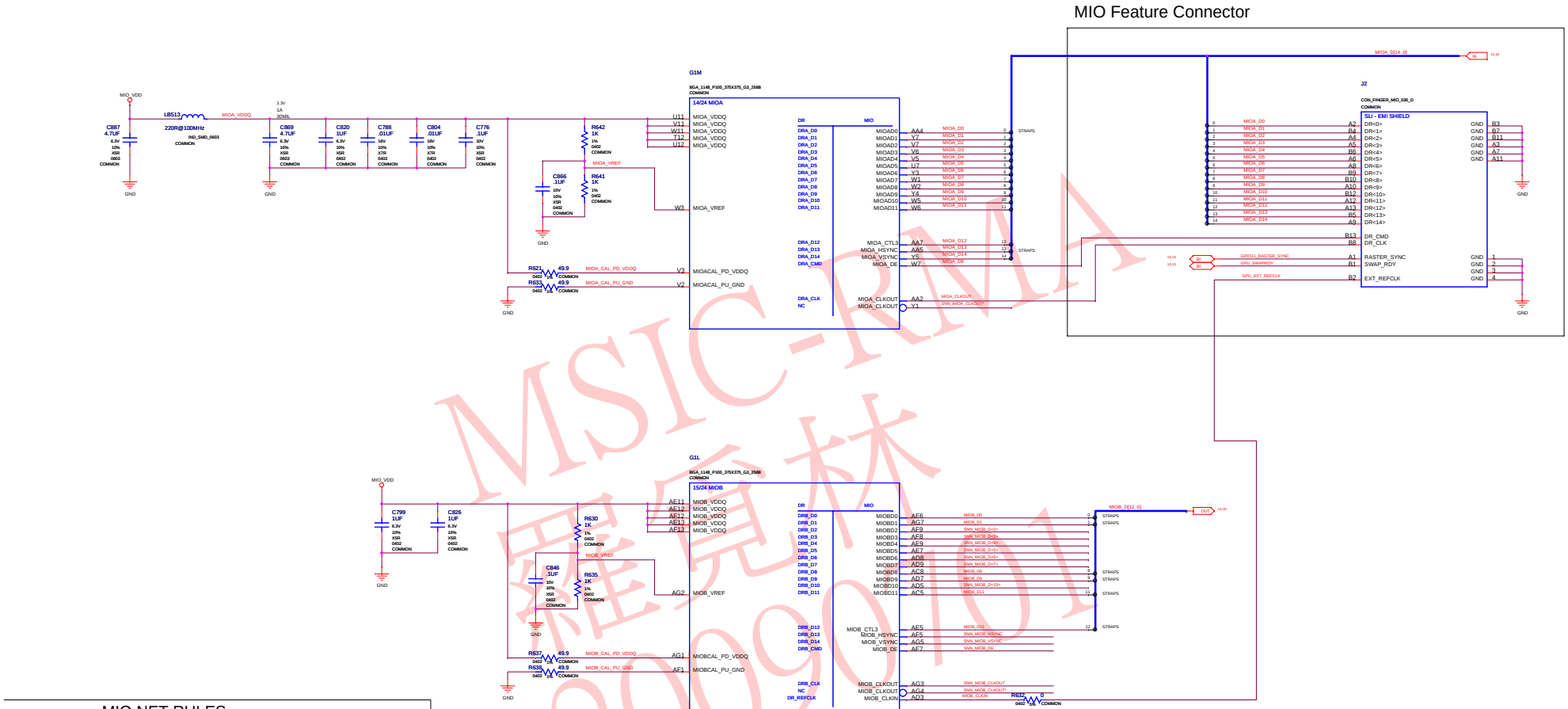
Page14: Multi-use IO(MIO) Interface



MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
MIOA_DI14..0	1	50OHM	
MIOA_CLKOUT	1	50OHM	
MIOA_DE	1	50OHM	
MIOB_DI12..0	1	50OHM	
MIOB_CLKIN	1	50OHM	
GPU_EXT_REFCLK	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	1.65V		12MIL
MIOACAL_PD_VDDQ			12MIL
MIOACAL_PU_GND			12MIL
MIOB_VREF	1.65V		12MIL
MIOBCAL_PD_VDDQ			12MIL
MIOBCAL_PU_GND			12MIL

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ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Multi-use IO(MIO) Interface

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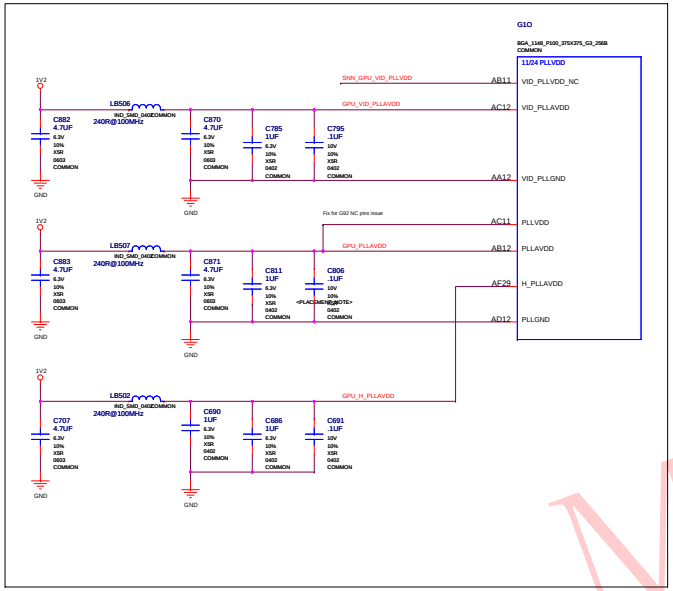
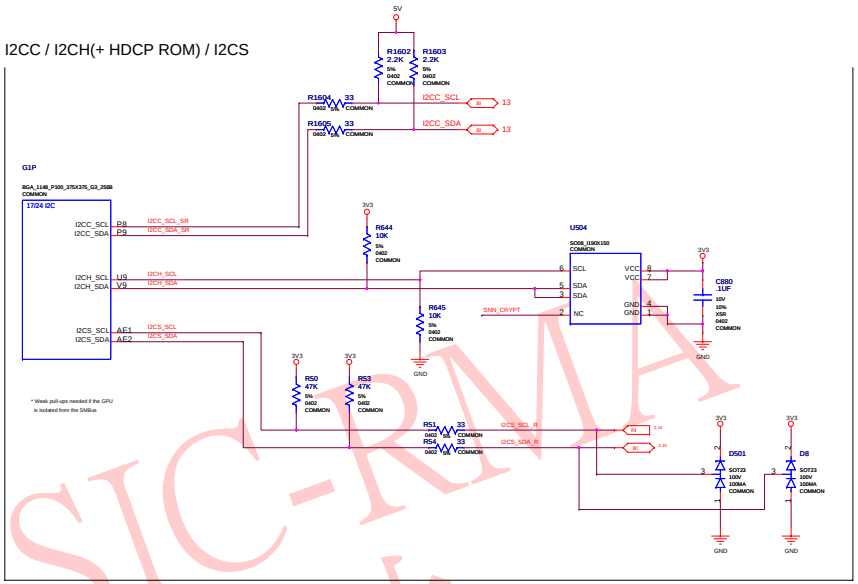
Page15: MISC: GPIO, I2C, BIOS, PLL, and XTAL

PLLVDD/VID_PLLVDD



I2CC / I2CH(+ HDCP ROM) / I2CS

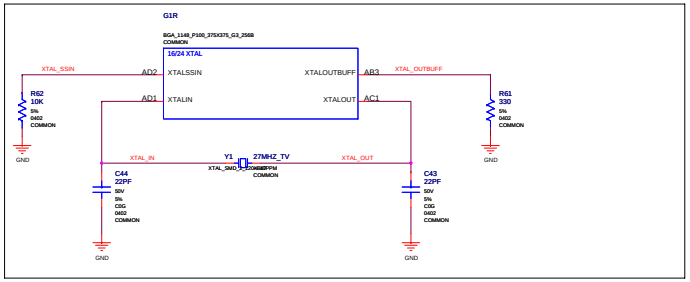


MISC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
I2CH_SCL	3	50OHM	
I2CH_SDA	3	50OHM	
I2CS_SCL	3	50OHM	
I2CS_SDA	3	50OHM	
I2CS_SCL_R	3	50OHM	
I2CS_SDA_R	3	50OHM	
ROM_CS*	3	50OHM	
ROM_SI	3	50OHM	
ROM_SO	3	50OHM	
ROM_SCLK	3	50OHM	
GPU_SWAPRDY	3	50OHM	
GPU_TESTMODE	3	50OHM	
GPIO0_DVI_A_HPD	3	50OHM	
GPIO1_DVI_C_HPD	3	50OHM	
GPIO4_FAN_PWM	3	50OHM	
GPIO5_VSEL0	3	50OHM	
GPIO6_VSEL1	3	50OHM	
GPIO7_FAN_TACH	3	50OHM	
GPIO8_THERM_OVERT*	3	50OHM	
GPIO11_RASTER_SYNC	3	50OHM	
XTAL_SSIN	1	50OHM	
XTAL_IN	1	50OHM	
XTAL_OUT	1	50OHM	
XTAL_OUTBUFF	1	50OHM	

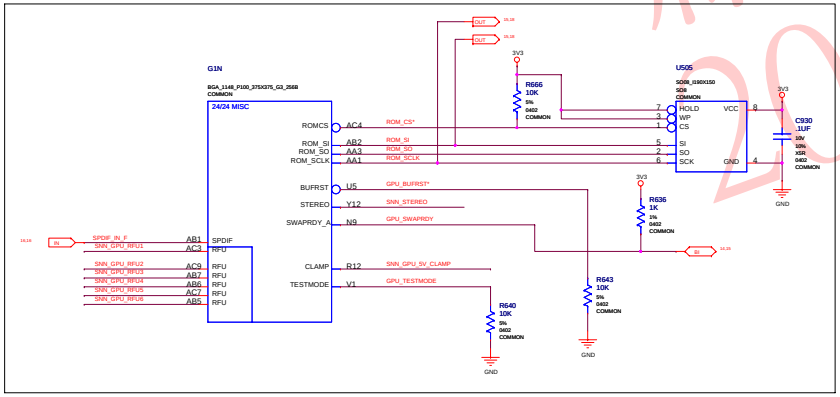
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
GPU_VID_PLLVDD	1.2V	0.05A	12MIL
GPU_VID_PLLAVDD	1.2V	0.05A	12MIL
GPU_PLLVDD	1.2V	0.05A	12MIL
GPU_PLLAVDD	1.2V	0.05A	12MIL
GPU_H_PLLAVDD	1.2V	0.05A	12MIL

XTAL

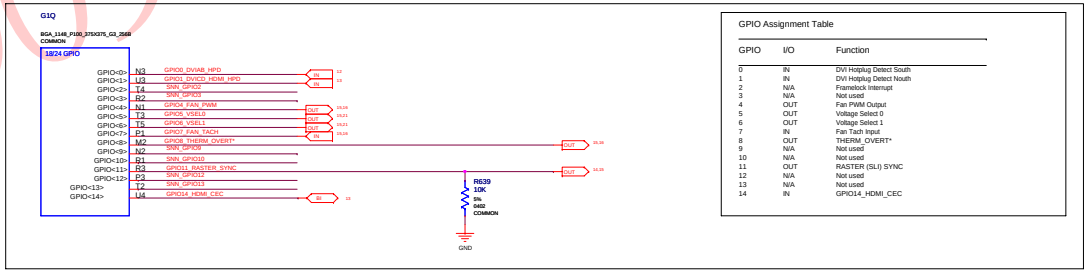


ROM / MISC

(BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)



GPIO



GPIO Assignment Table

GPIO	I/O	Function
0	IN	DVI Hotplug Detect South
1	IN	DVI Hotplug Detect North
2	N/A	Framelock Interrupt
3	N/A	Not used
4	OUT	Fan PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fan Tach Input
8	OUT	THERM_OVERT*
9	N/A	Not used
10	N/A	Not used
11	OUT	RASTER (SLI) SYNC
12	N/A	Not used
13	N/A	Not used
14	IN	GPIO14_HDMI_CEC

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ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO, I2C, BIOS, PLL, and XTAL

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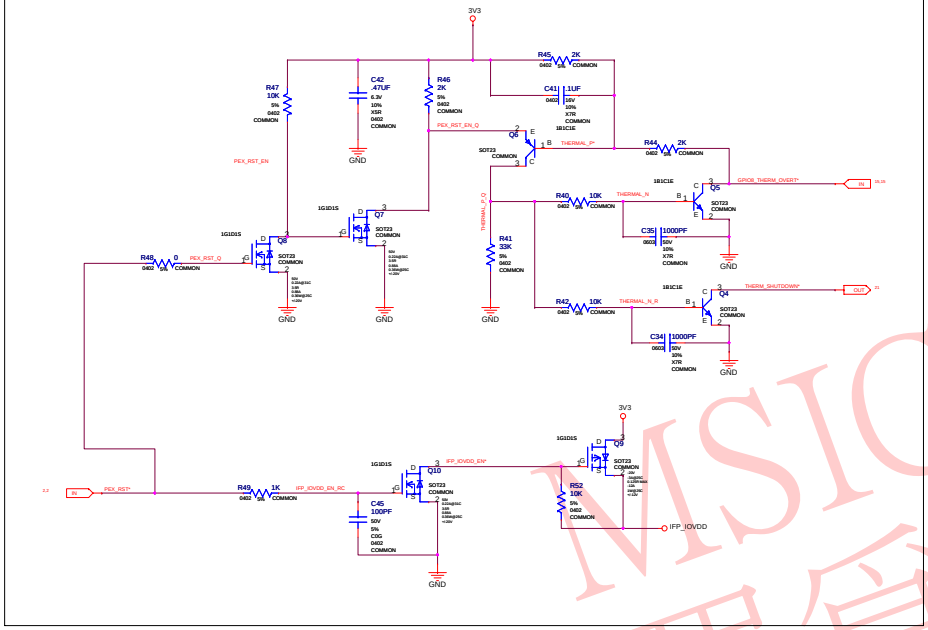
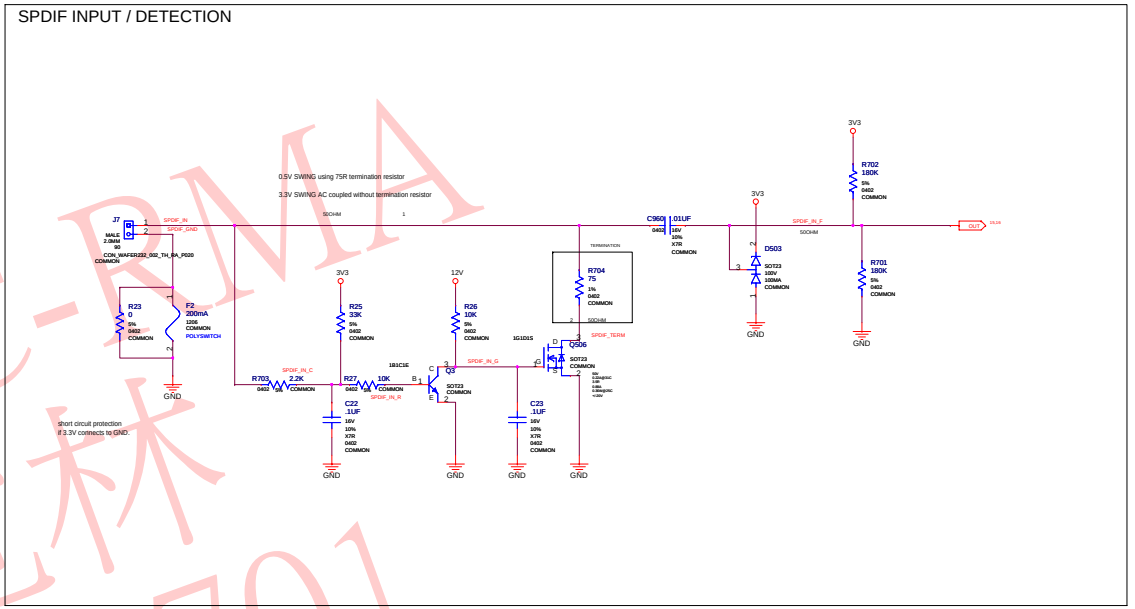
Page16: Thermal Control/Protection and SPDIF Input

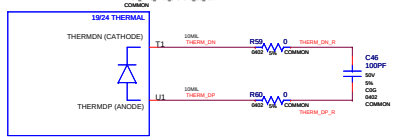
THERMAL PROTECTION/TMDS BACKDRIVE

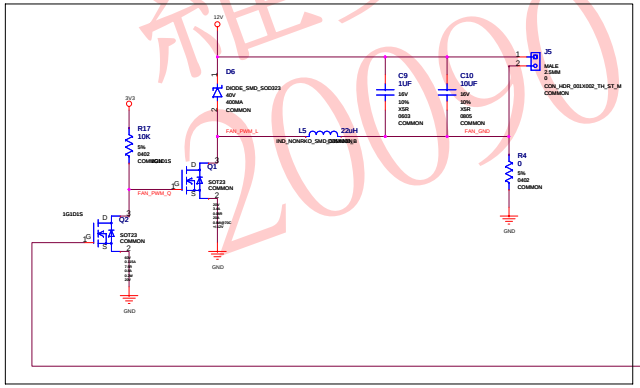


SPDIF INPUT / DETECTION

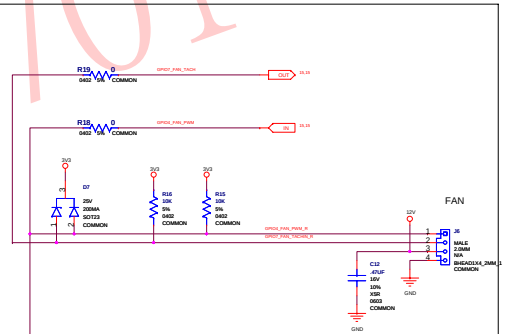


THERMAL DIODE





2-pin fan option



NET	IMPEDANCE	NV_CRITICAL_NET	MIN_LINE_WIDTH
SPDIF_IN_C	50OHM	1	
SPDIF_IN_R	50OHM	1	
SPDIF_IN_G	50OHM	1	
SPDIFIN_TERM	50OHM	1	
SPDIF_IN_F	50OHM	1	

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ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Control/Protection and SPDIF Input

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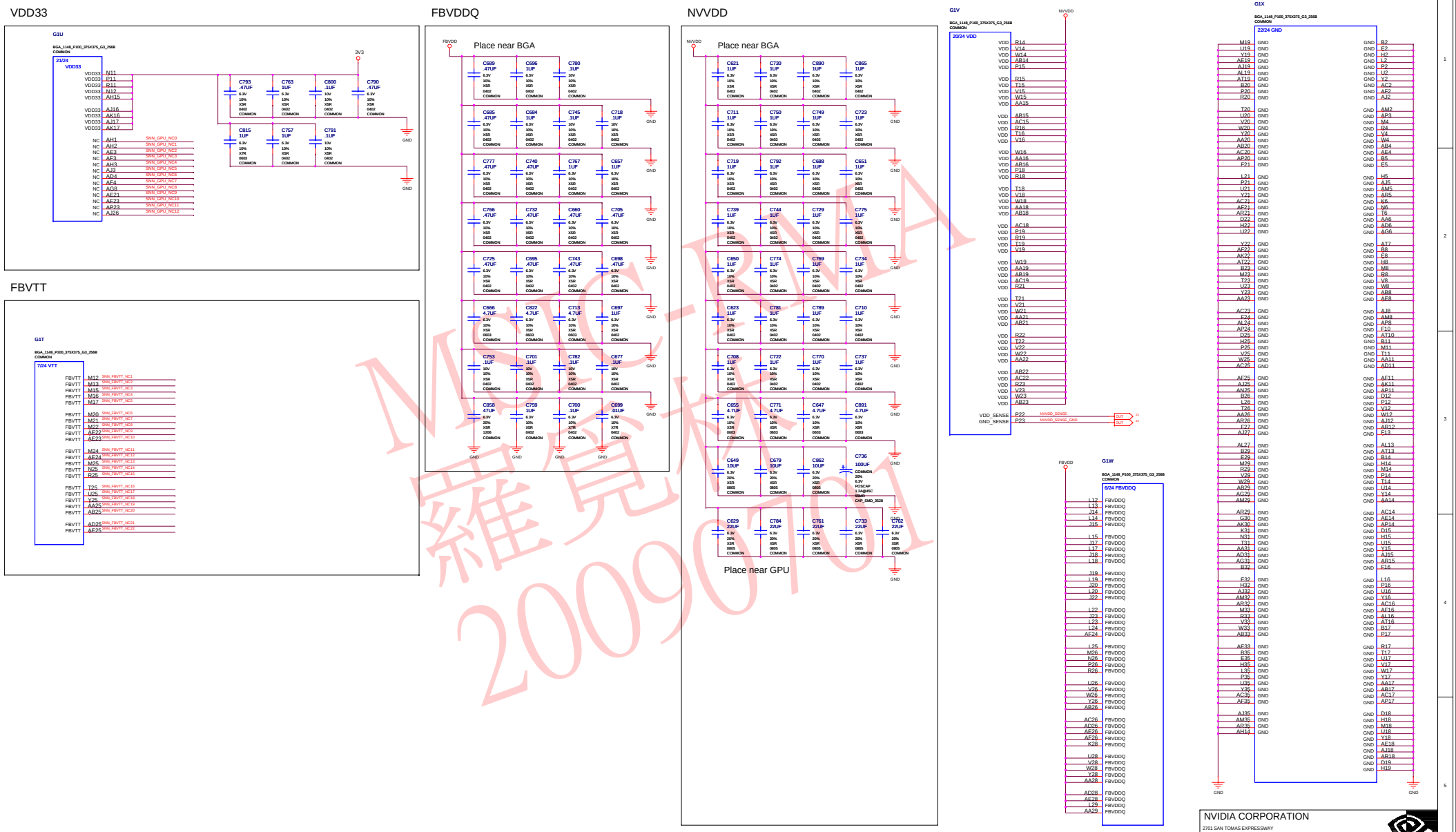
Page17: Power/GND and Decoupling

NVVVD and FBVVD decoupling need final data from SI



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ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power/GND and Decoupling

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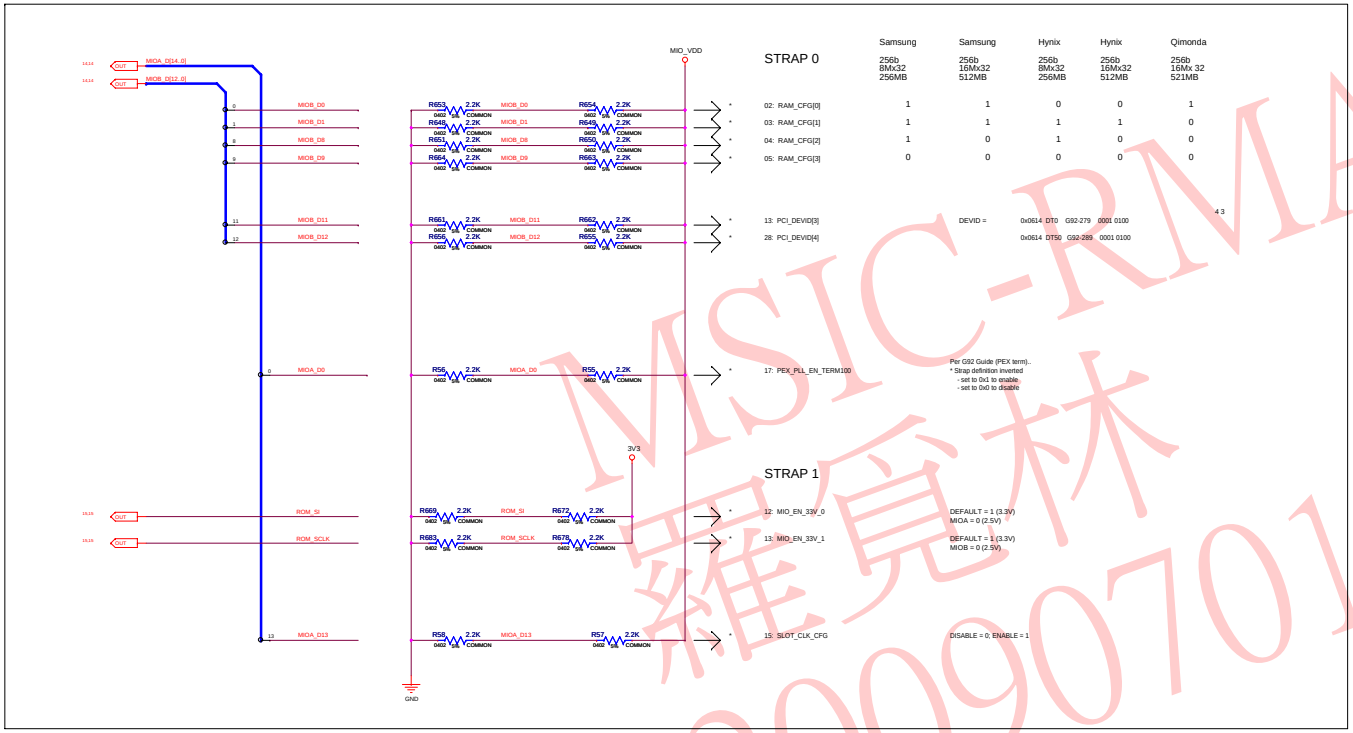
Page18: Configuration Straps and Mechanical

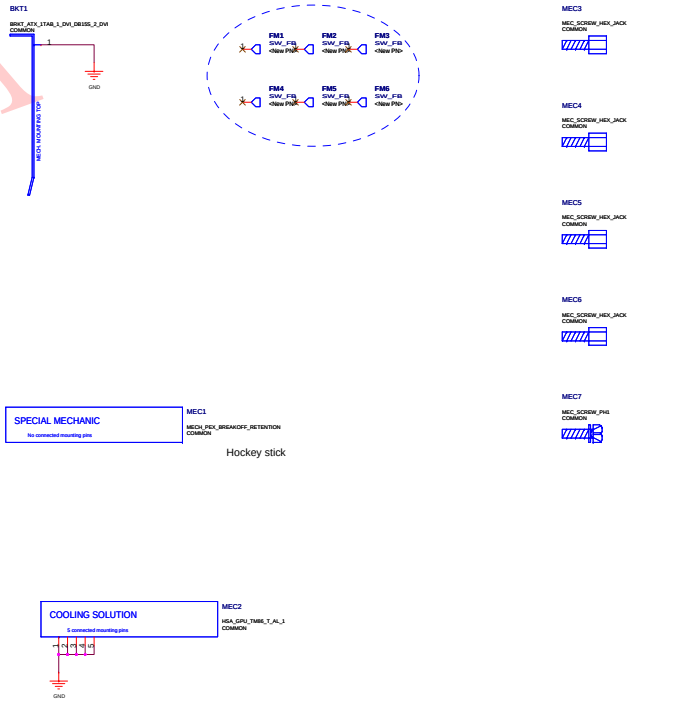
STRAPS



	Samsung	Samsung	Hynix	Hynix	Qimonda
	256b 8Mx32 256MB	256b 16Mx32 512MB	256b 8Mx32 256MB	256b 16Mx32 512MB	256b 16Mx 32 521MB
02: RAM_CFG[0]	1	1	0	0	1
03: RAM_CFG[1]	1	1	1	1	0
04: RAM_CFG[2]	1	0	1	0	0
05: RAM_CFG[3]	0	0	0	0	0

MECHANICAL

Mechanical parts need be updated when we have the final solution



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ASSEMBLY	
PAGE DETAIL	Configuration Straps and Mechanical

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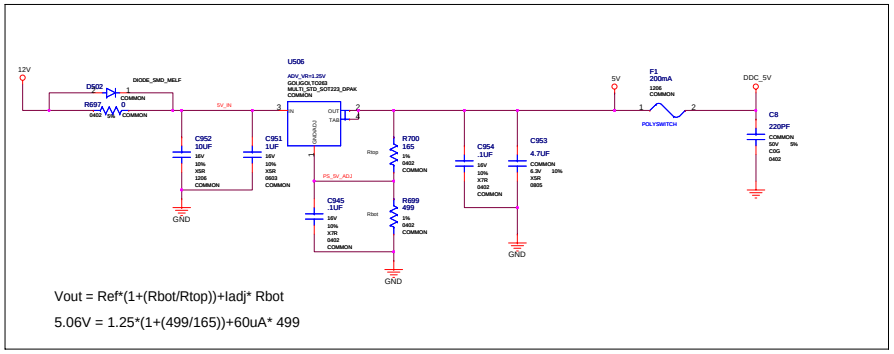
Page 19:Power Supply:IFP_PLLVDD,MIO_VDD,PEX_PLLVDD Option,DDV_5V

5V REGULATOR

5V DDC

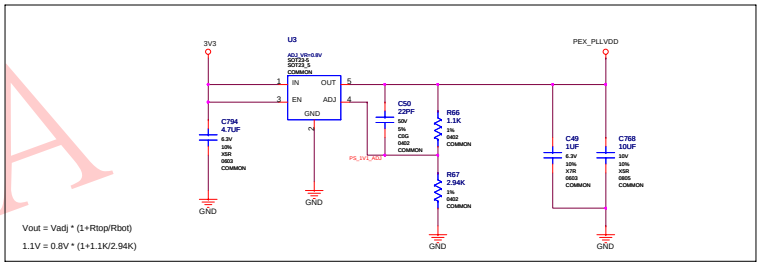


Vout = Ref*(1+(Rbot/Rtop))+Iadj* Rbot

5.06V = 1.25*(1+(499/165))+60uA* 499

PEX_PLLVDD Optional

(Stuff option)

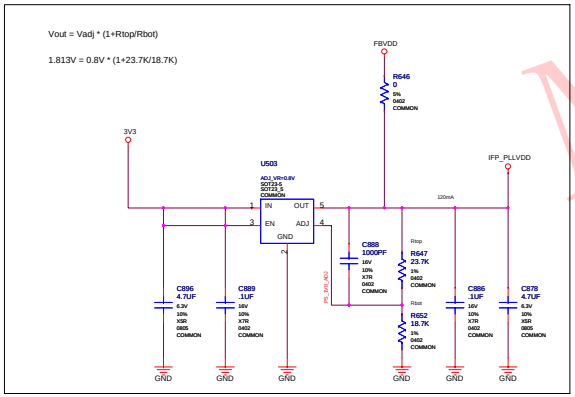


Vout = Vadj * (1+Rtop/Rbot)

1.1V = 0.8V * (1+1.1K/2.94K)

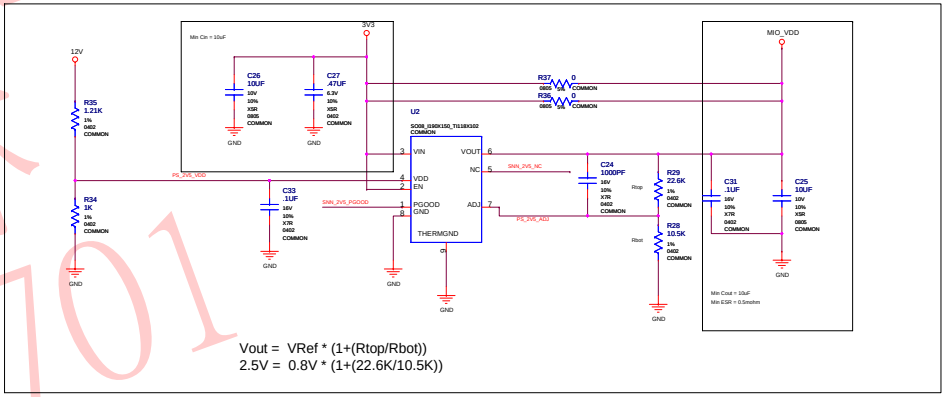
IFP PLL Supply 1.8V

(Stuff option)



MIO_VDD

(Stuff option)



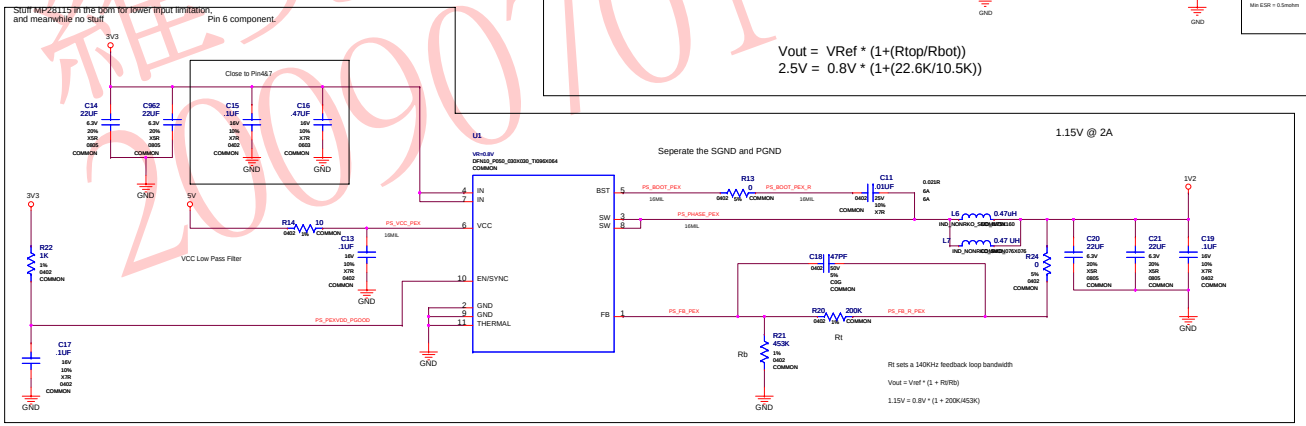
Vout = VRef * (1+(Rtop/Rbot))

2.5V = 0.8V * (1+(22.6K/10.5K))

1V2

Stuff MP28115 in the bom for lower input limitation, and meanwhile no stuff

Pin 6 component.



Seperate the SGND and PGND

1.15V @ 2A

VCC Low Pass Filter

Rt sets a 140KHz feedback loop bandwidth

Vout = Vref * (1 + Rt/Rb)

1.15V = 0.8V * (1 + 200K/453K)

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	0.1A	12MIL	5V
5V	0.15A	12MIL	5V
PEX_PLLVDD	0.12A	12MIL	1.1V
IFP_PLLVDD	0.12A	12MIL	1.8V
MIO_VDD	0.6A	12MIL	3.3V

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ASSEMBLY	
PAGE DETAIL	Power Supply:IFP_PLLVDD,MIO_VDD,PEX_PLLVDD Option,DDV_5V

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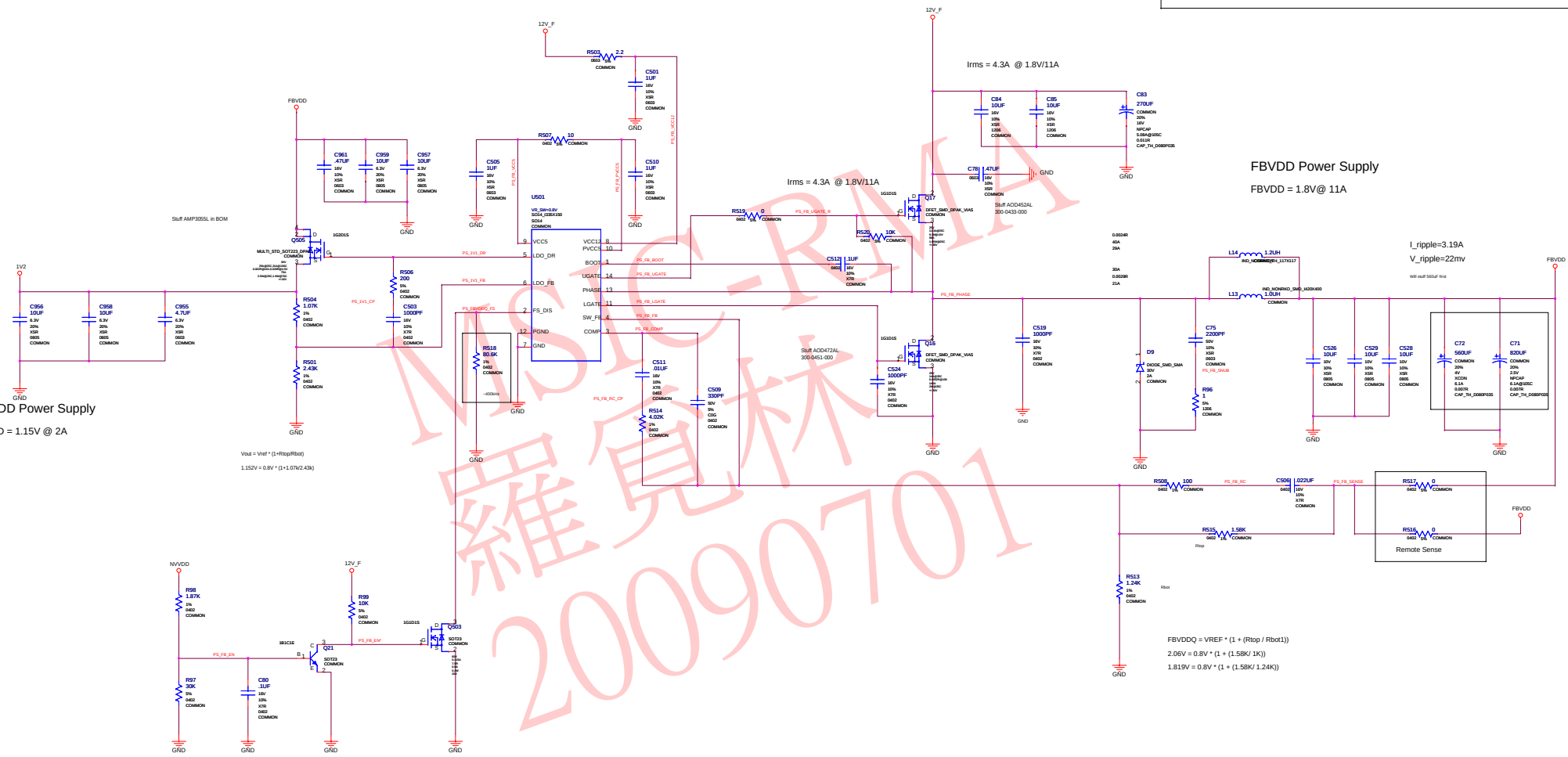
Page20:POWER SUPPLY: FBVDD,PEX_VDD

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
FBVDD	11A	20MIL	1.8V
1V2	2A	16MIL	1.15V



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ASSEMBLY	
PAGE DETAIL	POWER SUPPLY: FBVDD,PEX_VDD

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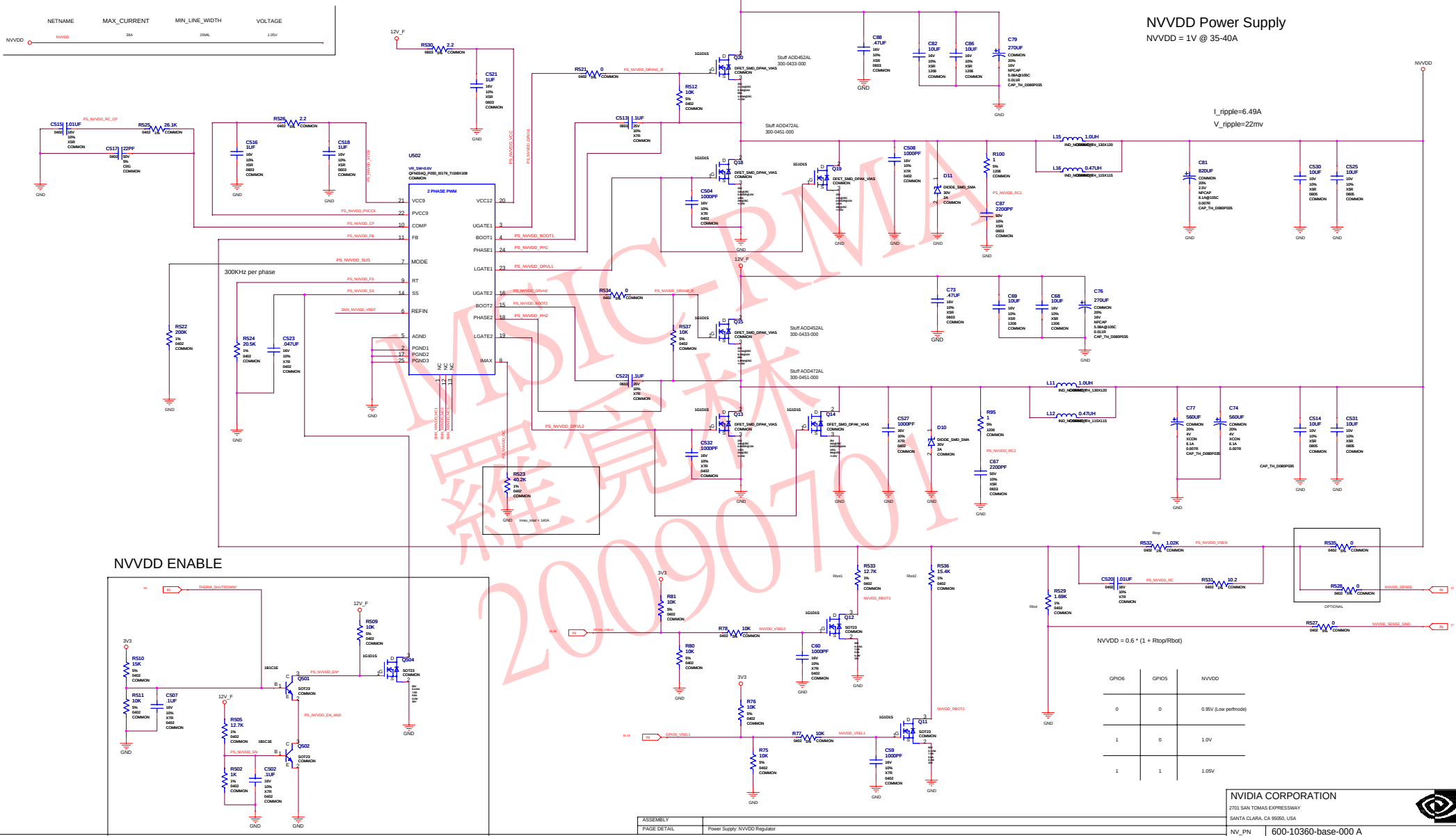
Page21:POWER SUPPLY: NVVDD



GPIO6	GPIO5	NVVDD
0	0	0.95V (Low perfmode)
1	0	1.0V
1	1	1.05V

ASSEMBLY	
PAGE DETAIL	Power Supply: NVVDD Regulator

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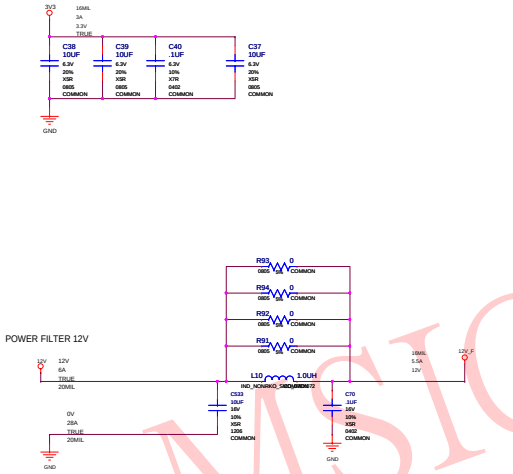
Page22: Power Supply: Filter of 12V,3V3



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ASSEMBLY	
PAGE DETAIL	Power Supply: Filter of 3V3, 12V

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