

256/512MB 128-BIT GDDR2  
LVDS, DVI-A, DVI-B, TV-OUT, VGA, HDMI  
SLI, HDCP, MXM V2.0 TTP SUPPORT


Page 1: Cover Page  
Page 2: PCI EXPRESS Interface  
Page 3: Frame Buffer GPU Interface  
Page 4: Frame Buffer Partition A Memories  
Page 5: Frame Buffer Partition C Memories  
Page 6: Memory Decoupling Caps  
Page 7: DACs, Clock-Generation  
Page 8: LVDS, TMDS GPU Interface  
Page 9: MXM Connector, IO-Section  
Page 10: GPIOs, JTAG, Thermal Sensor  
Page 11: Spread Spectrum, VBIOS and HDCP ROM  
Page 12: MIOA(SLI), MIOB  
Page 13: NVDDQ Power Supply  
Page 14: FBVDDQ, PEX1V2 and DAC\_Vref Power Supply  
Page 15: STRAPS, TTP, MOUNTINGHOLE

#	VARIANT	N/P/N	ASSEMBLY
0	BASE	860-9555-999-000	SAGE-LEVEL GENERIC SCHEMATIC ONLY - COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
1	SKXXXX	860-9555-999-000	S&W-400-KHNSK-280MR-18MR-GDGRS-18MR-RFPCA-LGDS + DVI_ADN_8 + TV_ZUT + VGA_WHM-IGL-HOCP.
2	SKXXXX	860-9555-999-000	S&W-400-KHNSK-280MR-18MR-GDGRS-22MR-RFPCA-LGDS + DVI_ADN_8 + TV_ZUT + VGA_WHM-IGL-HOCP.
3	SKXXXX	860-9555-999-000	S&W-70-TXMSK-280MR-18MR-GDGRS-22MR-RFPCA-LGDS + DVI_ADN_8 + TV_ZUT + VGA_WHM-IGL-HOCP.
4	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
5	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
6	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
7	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
8	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
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12	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
13	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
14	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
15	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>

- 1) Change MEC1\_JEDEC\_TYPE from MCH\_MXM2\_HOLES to MECH\_MXM2\_HOLES\_103NP\_4VIAS
- 2) Add pull low resistor to MIOA\_D[0] for straps
- 3) Add pull up resistor to MIOA\_D[6] for straps

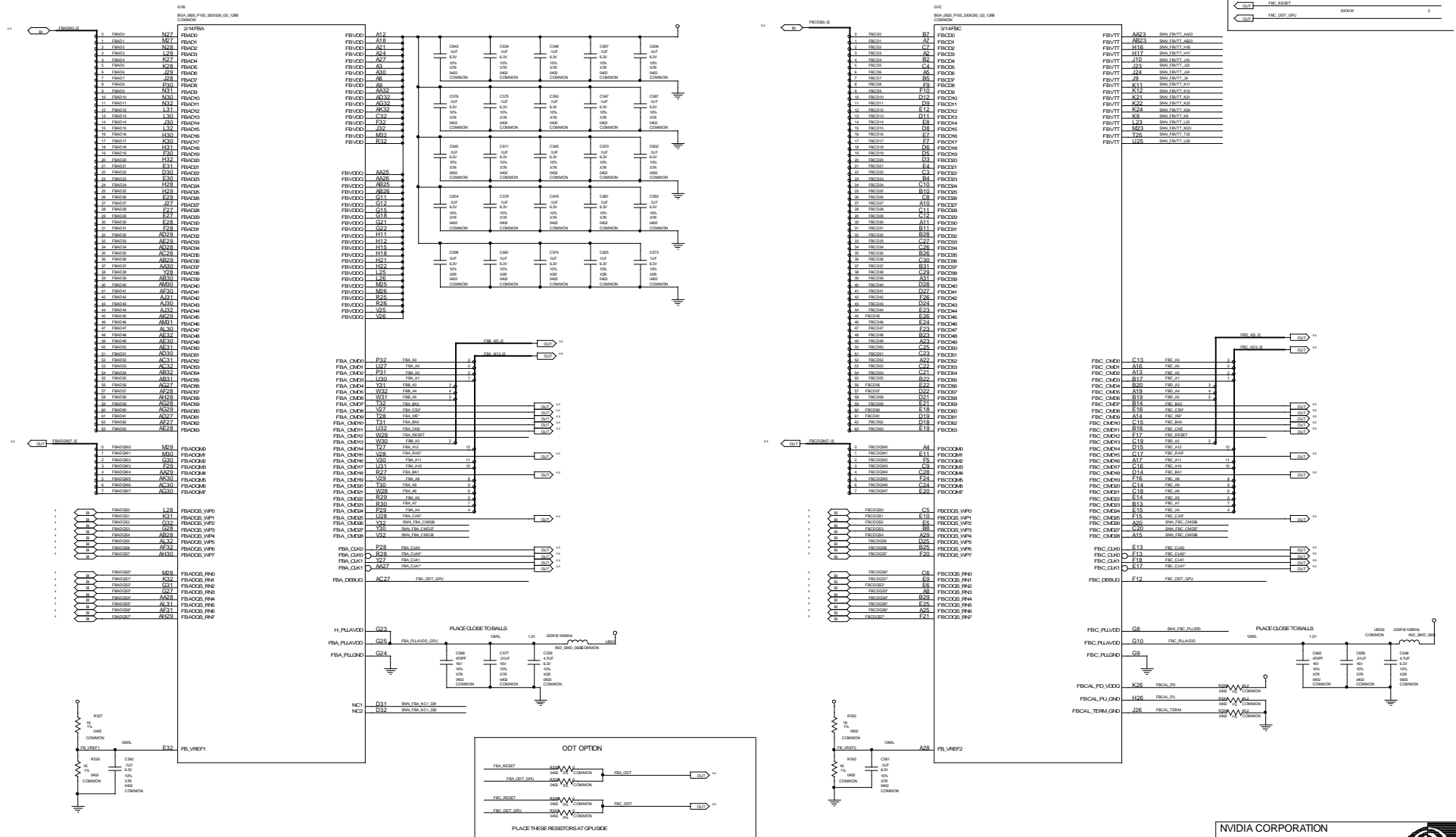
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FIN
PAGE DETAIL	Cover Page

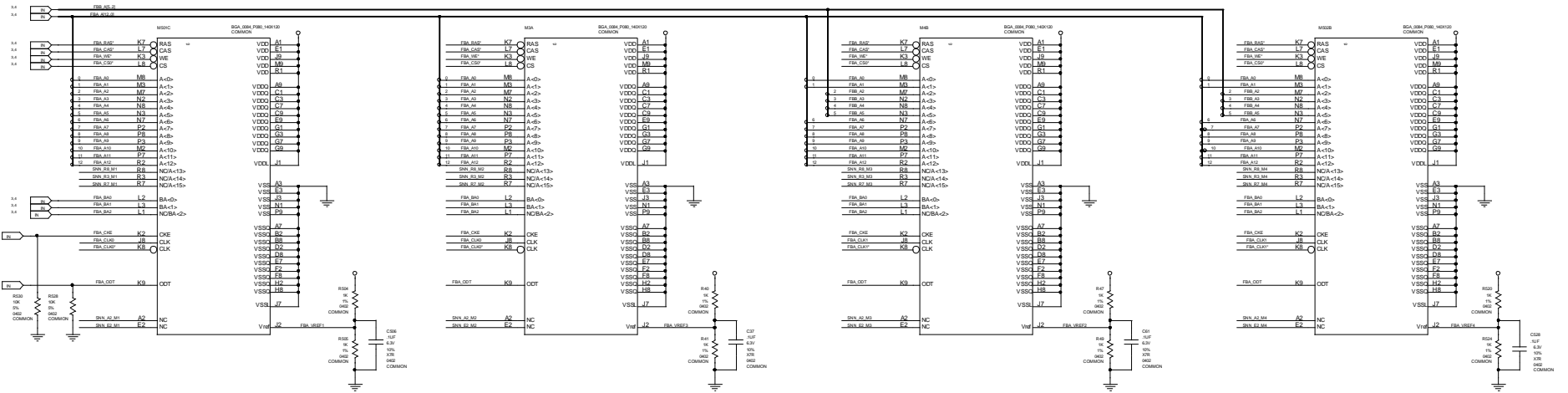
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# PAGE 3) GPU MEMORY INTERFACE





CLOCK TERMINATIONS



NET	MAN LINE WIDTH	VOLTAGE
FBA_VDDQ1	100um	1.8V
FBA_VDDQ2	100um	1.8V
FBA_VDDQ3	100um	1.8V
FBA_VDDQ4	100um	1.8V
FBA_VDDQ5	100um	1.8V
FBA_VDDQ6	100um	1.8V
FBA_VDDQ7	100um	1.8V
FBA_VDDQ8	100um	1.8V
FBA_VDDQ9	100um	1.8V
FBA_VDDQ10	100um	1.8V
FBA_VDDQ11	100um	1.8V
FBA_VDDQ12	100um	1.8V
FBA_VDDQ13	100um	1.8V
FBA_VDDQ14	100um	1.8V
FBA_VDDQ15	100um	1.8V
FBA_VDDQ16	100um	1.8V
FBA_VDDQ17	100um	1.8V
FBA_VDDQ18	100um	1.8V
FBA_VDDQ19	100um	1.8V
FBA_VDDQ20	100um	1.8V
FBA_VDDQ21	100um	1.8V
FBA_VDDQ22	100um	1.8V
FBA_VDDQ23	100um	1.8V
FBA_VDDQ24	100um	1.8V
FBA_VDDQ25	100um	1.8V
FBA_VDDQ26	100um	1.8V
FBA_VDDQ27	100um	1.8V
FBA_VDDQ28	100um	1.8V
FBA_VDDQ29	100um	1.8V
FBA_VDDQ30	100um	1.8V
FBA_VDDQ31	100um	1.8V
FBA_VDDQ32	100um	1.8V
FBA_VDDQ33	100um	1.8V
FBA_VDDQ34	100um	1.8V
FBA_VDDQ35	100um	1.8V
FBA_VDDQ36	100um	1.8V
FBA_VDDQ37	100um	1.8V
FBA_VDDQ38	100um	1.8V
FBA_VDDQ39	100um	1.8V
FBA_VDDQ40	100um	1.8V
FBA_VDDQ41	100um	1.8V
FBA_VDDQ42	100um	1.8V
FBA_VDDQ43	100um	1.8V
FBA_VDDQ44	100um	1.8V
FBA_VDDQ45	100um	1.8V
FBA_VDDQ46	100um	1.8V
FBA_VDDQ47	100um	1.8V
FBA_VDDQ48	100um	1.8V
FBA_VDDQ49	100um	1.8V
FBA_VDDQ50	100um	1.8V
FBA_VDDQ51	100um	1.8V
FBA_VDDQ52	100um	1.8V
FBA_VDDQ53	100um	1.8V
FBA_VDDQ54	100um	1.8V
FBA_VDDQ55	100um	1.8V
FBA_VDDQ56	100um	1.8V
FBA_VDDQ57	100um	1.8V
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FBA_VDDQ61	100um	1.8V
FBA_VDDQ62	100um	1.8V
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FBA_VDDQ64	100um	1.8V
FBA_VDDQ65	100um	1.8V
FBA_VDDQ66	100um	1.8V
FBA_VDDQ67	100um	1.8V
FBA_VDDQ68	100um	1.8V
FBA_VDDQ69	100um	1.8V
FBA_VDDQ70	100um	1.8V
FBA_VDDQ71	100um	1.8V
FBA_VDDQ72	100um	1.8V
FBA_VDDQ73	100um	1.8V
FBA_VDDQ74	100um	1.8V
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FBA_VDDQ81	100um	1.8V
FBA_VDDQ82	100um	1.8V
FBA_VDDQ83	100um	1.8V
FBA_VDDQ84	100um	1.8V
FBA_VDDQ85	100um	1.8V
FBA_VDDQ86	100um	1.8V
FBA_VDDQ87	100um	1.8V
FBA_VDDQ88	100um	1.8V
FBA_VDDQ89	100um	1.8V
FBA_VDDQ90	100um	1.8V
FBA_VDDQ91	100um	1.8V
FBA_VDDQ92	100um	1.8V
FBA_VDDQ93	100um	1.8V
FBA_VDDQ94	100um	1.8V
FBA_VDDQ95	100um	1.8V
FBA_VDDQ96	100um	1.8V
FBA_VDDQ97	100um	1.8V
FBA_VDDQ98	100um	1.8V
FBA_VDDQ99	100um	1.8V
FBA_VDDQ100	100um	1.8V

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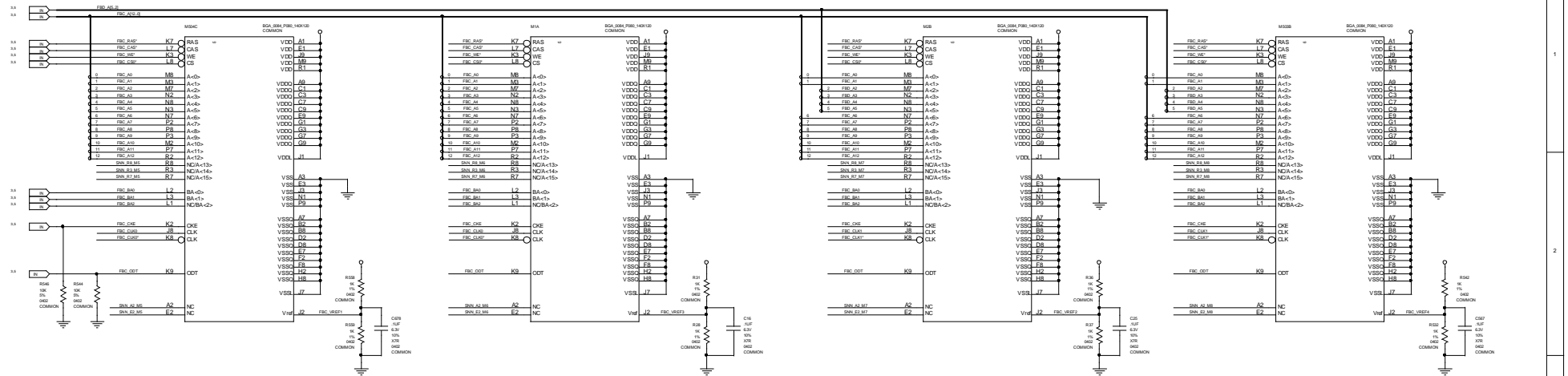
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ASSEMBLY  
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BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON AND/ OR DIFF. ASSEMBLY NOTES AND BOM NOT FINAL.  
Frame Buffer Partition A Memory

# PAGE 5) MEMORY PARTITION C



## CLOCK TERMINATIONS



NET	DIFFER	CIRCUIT	IMPEDANCE
FRC_0001	FRC_0001	1	100Ω
FRC_0002	FRC_0002	1	100Ω
FRC_0003	FRC_0003	1	100Ω
FRC_0004	FRC_0004	1	100Ω
FRC_0005	FRC_0005	1	100Ω
FRC_0006	FRC_0006	1	100Ω
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FRC_0040	FRC_0040	1	100Ω
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FRC_0058	FRC_0058	1	100Ω
FRC_0059	FRC_0059	1	100Ω
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FRC_0065	FRC_0065	1	100Ω
FRC_0066	FRC_0066	1	100Ω
FRC_0067	FRC_0067	1	100Ω
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FRC_0096	FRC_0096	1	100Ω
FRC_0097	FRC_0097	1	100Ω
FRC_0098	FRC_0098	1	100Ω
FRC_0099	FRC_0099	1	100Ω
FRC_0100	FRC_0100	1	100Ω

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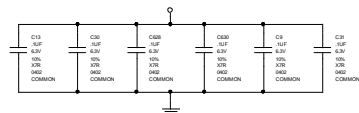
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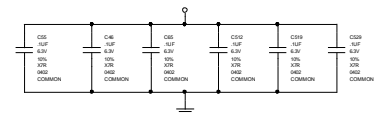
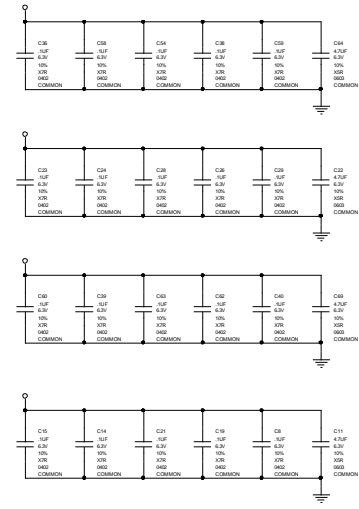
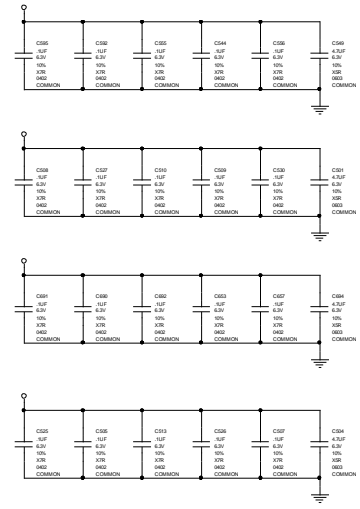
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DECOUPLING CAPS FOR MEMOYS (PARTION A AND PARTION C)



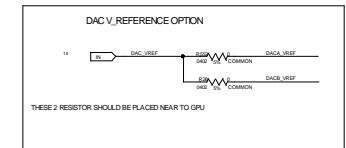
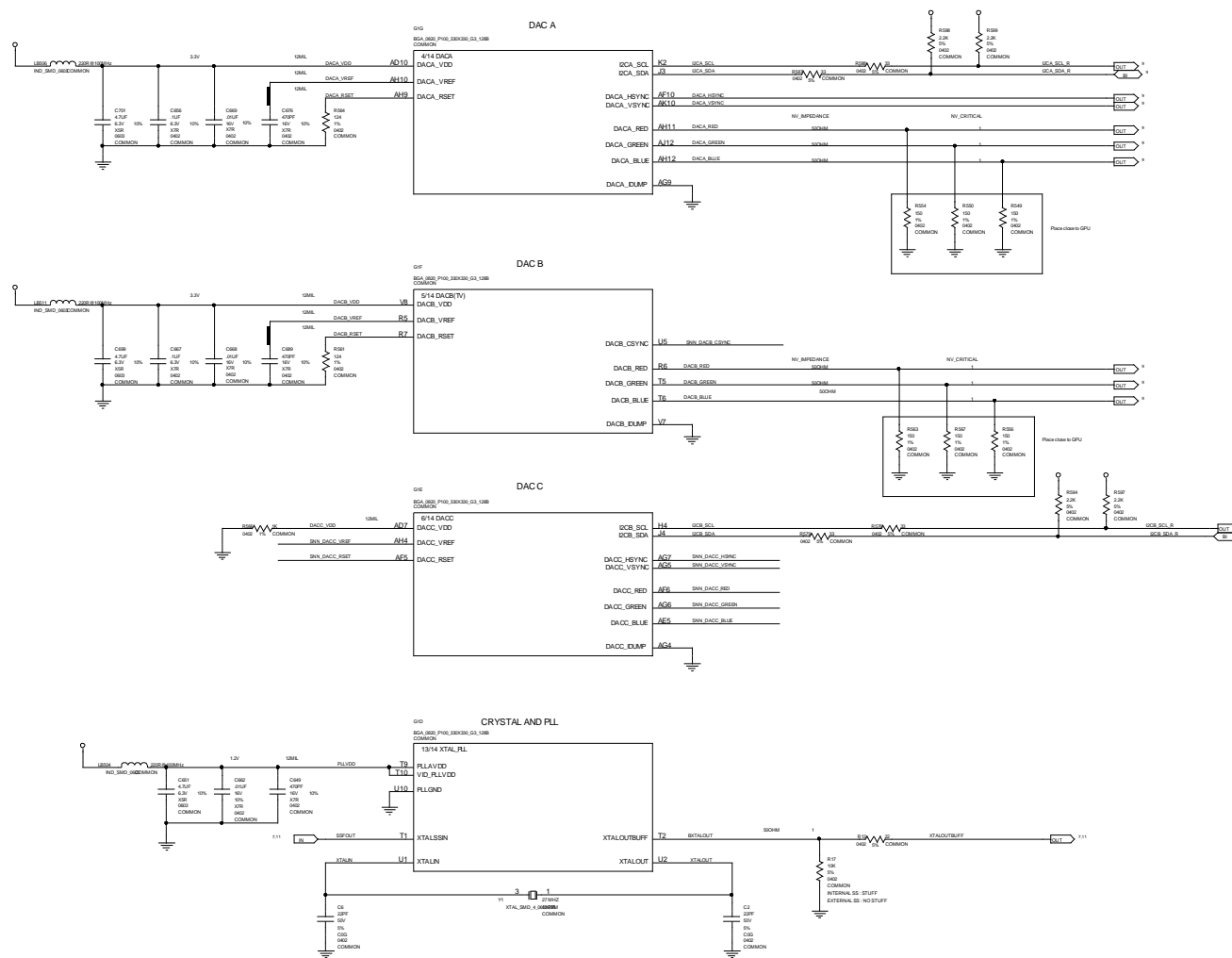
NVDD TRANSITION CAP NEAR BY PARTION A



NVDD TRANSITION CAP NEAR BY PARTION C

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PAGE DETAIL		Memory Decoupling Caps	
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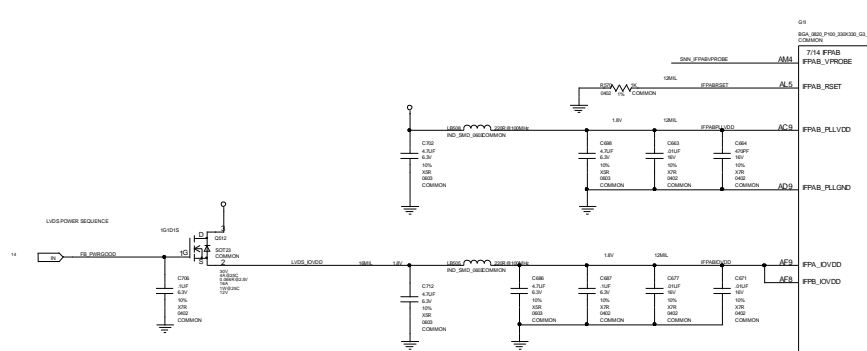
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712	XTALOUTBUFF	NOISE	1
713	XTALOUT	NOISE	1

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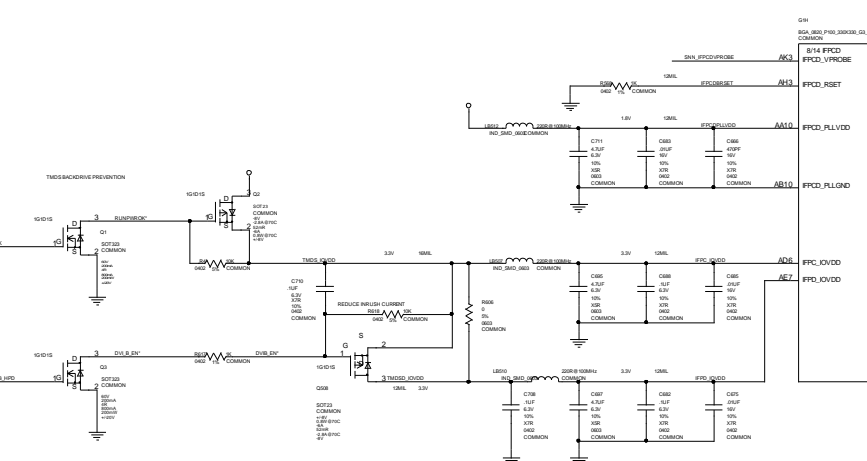
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LVDS

NET NAME	OFFPAR	LV_CRITICAL_NET	LV_IMPEDANCE
FFR_TX0_A10	FFR_TX0_A10	FFR_TX0_A10	100nF
FFR_TX0_A11	FFR_TX0_A11	FFR_TX0_A11	100nF
FFR_TX0_A12	FFR_TX0_A12	FFR_TX0_A12	100nF
FFR_TX0_A13	FFR_TX0_A13	FFR_TX0_A13	100nF
FFR_TX0_A14	FFR_TX0_A14	FFR_TX0_A14	100nF
FFR_TX0_A15	FFR_TX0_A15	FFR_TX0_A15	100nF
FFR_TX0_A16	FFR_TX0_A16	FFR_TX0_A16	100nF
FFR_TX0_A17	FFR_TX0_A17	FFR_TX0_A17	100nF
FFR_TX0_A18	FFR_TX0_A18	FFR_TX0_A18	100nF
FFR_TX0_A19	FFR_TX0_A19	FFR_TX0_A19	100nF
FFR_TX0_A20	FFR_TX0_A20	FFR_TX0_A20	100nF
FFR_TX0_A21	FFR_TX0_A21	FFR_TX0_A21	100nF
FFR_TX0_A22	FFR_TX0_A22	FFR_TX0_A22	100nF
FFR_TX0_A23	FFR_TX0_A23	FFR_TX0_A23	100nF
FFR_TX0_A24	FFR_TX0_A24	FFR_TX0_A24	100nF
FFR_TX0_A25	FFR_TX0_A25	FFR_TX0_A25	100nF
FFR_TX0_A26	FFR_TX0_A26	FFR_TX0_A26	100nF
FFR_TX0_A27	FFR_TX0_A27	FFR_TX0_A27	100nF
FFR_TX0_A28	FFR_TX0_A28	FFR_TX0_A28	100nF
FFR_TX0_A29	FFR_TX0_A29	FFR_TX0_A29	100nF
FFR_TX0_A30	FFR_TX0_A30	FFR_TX0_A30	100nF
FFR_TX0_A31	FFR_TX0_A31	FFR_TX0_A31	100nF
FFR_TX0_A32	FFR_TX0_A32	FFR_TX0_A32	100nF
FFR_TX0_A33	FFR_TX0_A33	FFR_TX0_A33	100nF
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FFR_TX0_A35	FFR_TX0_A35	FFR_TX0_A35	100nF
FFR_TX0_A36	FFR_TX0_A36	FFR_TX0_A36	100nF
FFR_TX0_A37	FFR_TX0_A37	FFR_TX0_A37	100nF
FFR_TX0_A38	FFR_TX0_A38	FFR_TX0_A38	100nF
FFR_TX0_A39	FFR_TX0_A39	FFR_TX0_A39	100nF
FFR_TX0_A40	FFR_TX0_A40	FFR_TX0_A40	100nF
FFR_TX0_A41	FFR_TX0_A41	FFR_TX0_A41	100nF
FFR_TX0_A42	FFR_TX0_A42	FFR_TX0_A42	100nF
FFR_TX0_A43	FFR_TX0_A43	FFR_TX0_A43	100nF
FFR_TX0_A44	FFR_TX0_A44	FFR_TX0_A44	100nF
FFR_TX0_A45	FFR_TX0_A45	FFR_TX0_A45	100nF
FFR_TX0_A46	FFR_TX0_A46	FFR_TX0_A46	100nF
FFR_TX0_A47	FFR_TX0_A47	FFR_TX0_A47	100nF
FFR_TX0_A48	FFR_TX0_A48	FFR_TX0_A48	100nF
FFR_TX0_A49	FFR_TX0_A49	FFR_TX0_A49	100nF
FFR_TX0_A50	FFR_TX0_A50	FFR_TX0_A50	100nF
FFR_TX0_A51	FFR_TX0_A51	FFR_TX0_A51	100nF
FFR_TX0_A52	FFR_TX0_A52	FFR_TX0_A52	100nF
FFR_TX0_A53	FFR_TX0_A53	FFR_TX0_A53	100nF
FFR_TX0_A54	FFR_TX0_A54	FFR_TX0_A54	100nF
FFR_TX0_A55	FFR_TX0_A55	FFR_TX0_A55	100nF
FFR_TX0_A56	FFR_TX0_A56	FFR_TX0_A56	100nF
FFR_TX0_A57	FFR_TX0_A57	FFR_TX0_A57	100nF
FFR_TX0_A58	FFR_TX0_A58	FFR_TX0_A58	100nF
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FFR_TX0_A99	FFR_TX0_A99	FFR_TX0_A99	100nF
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TMDS

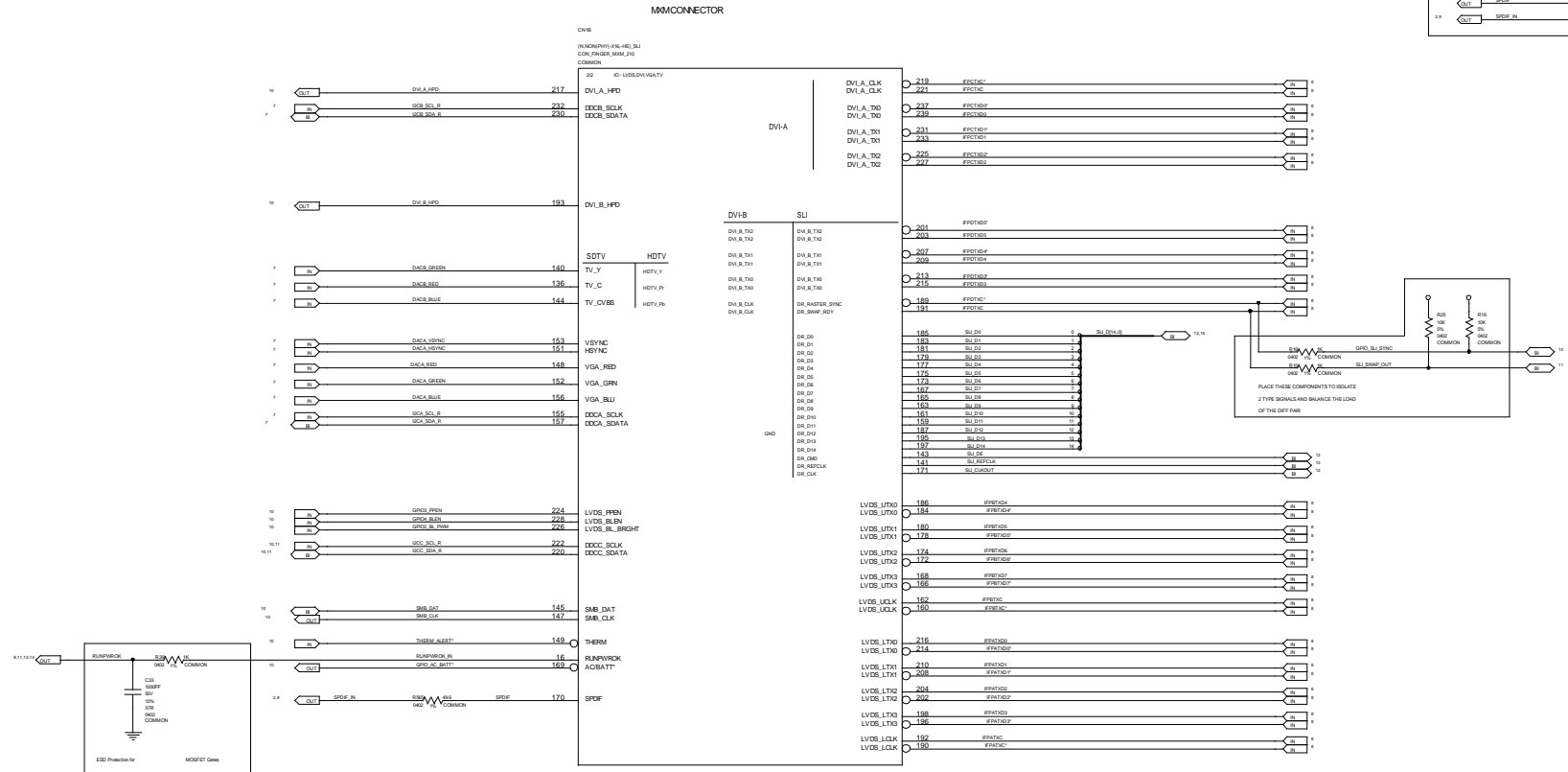
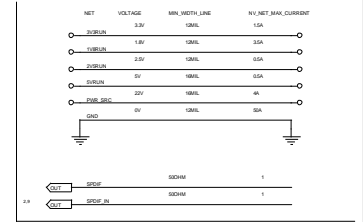
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FFC_TX0_A17	FFC_TX0_A17	FFC_TX0_A17	100nF
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FFC_TX0_A26	FFC_TX0_A26	FFC_TX0_A26	100nF
FFC_TX0_A27	FFC_TX0_A27	FFC_TX0_A27	100nF
FFC_TX0_A28	FFC_TX0_A28	FFC_TX0_A28	100nF
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FRONT DETAIL	LVDS, TMDS GPU interfaces

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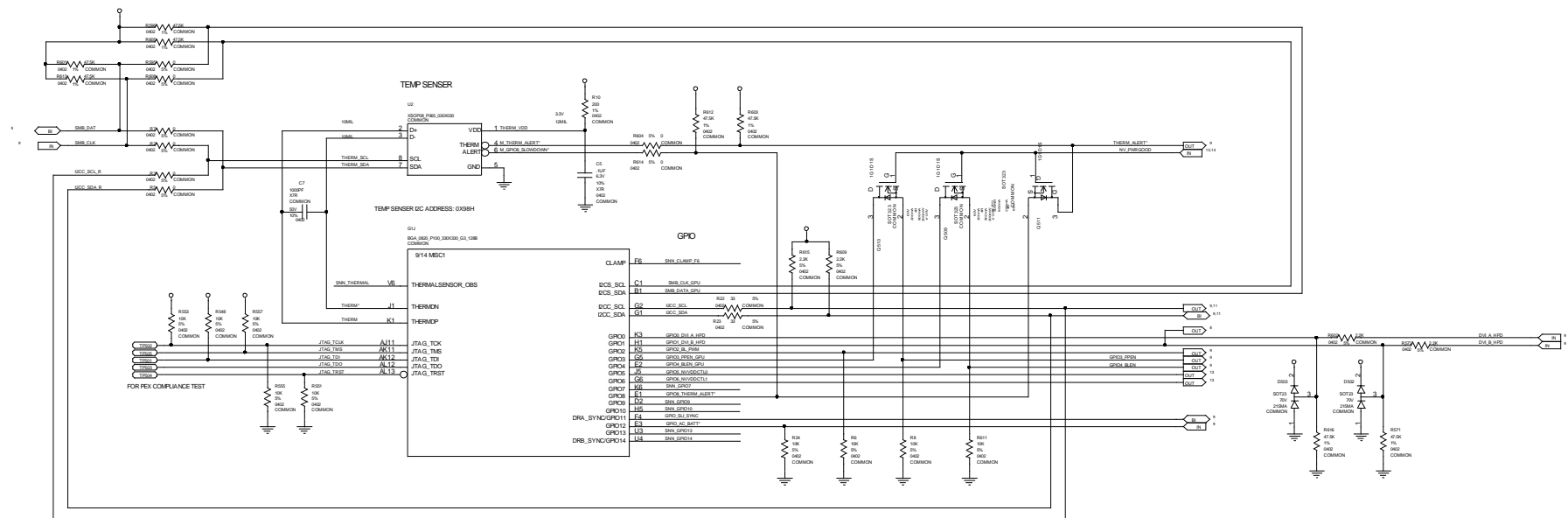
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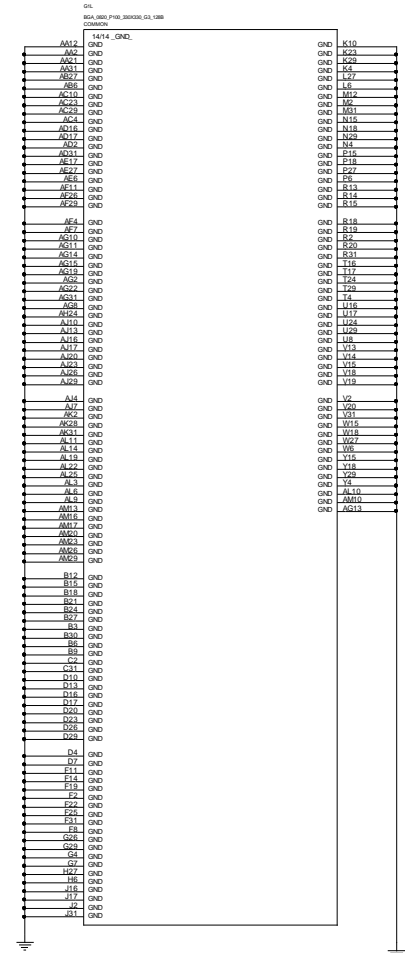
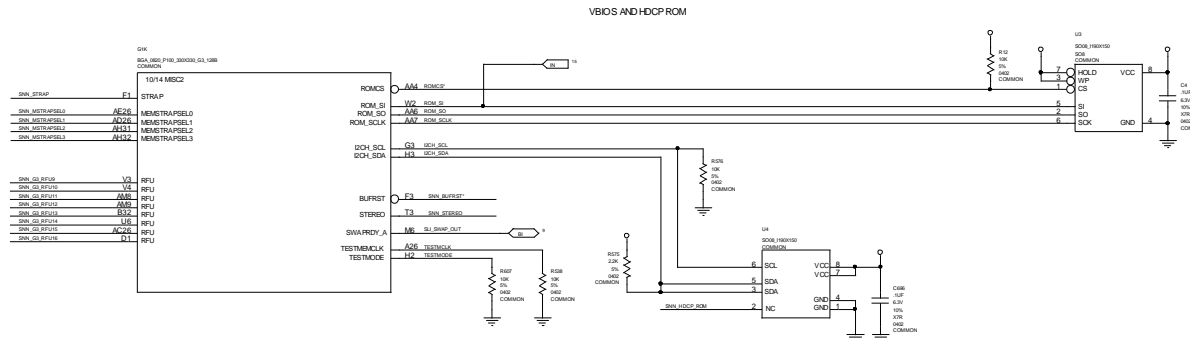
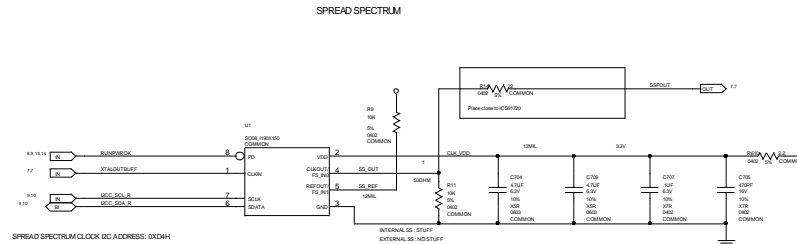


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PAGE DETAIL	GPIOs, JTAG, Thermal Sensor

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PAGE DETAIL  
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Spread Spectrum, VBIOS and HDCP ROM

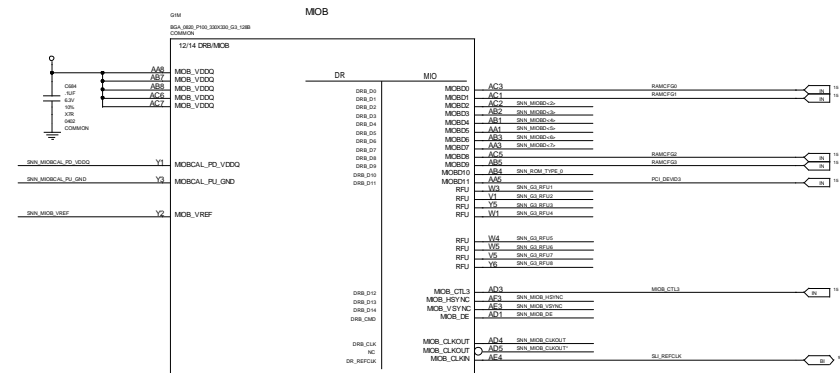
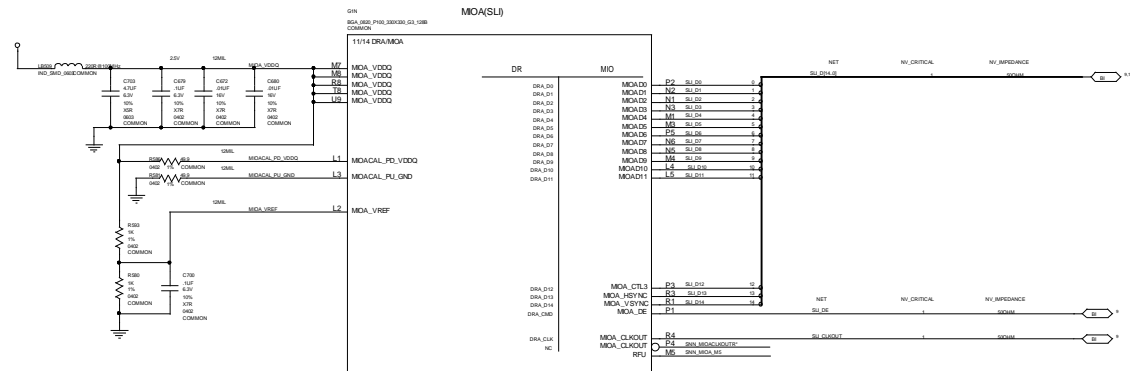
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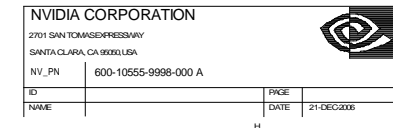


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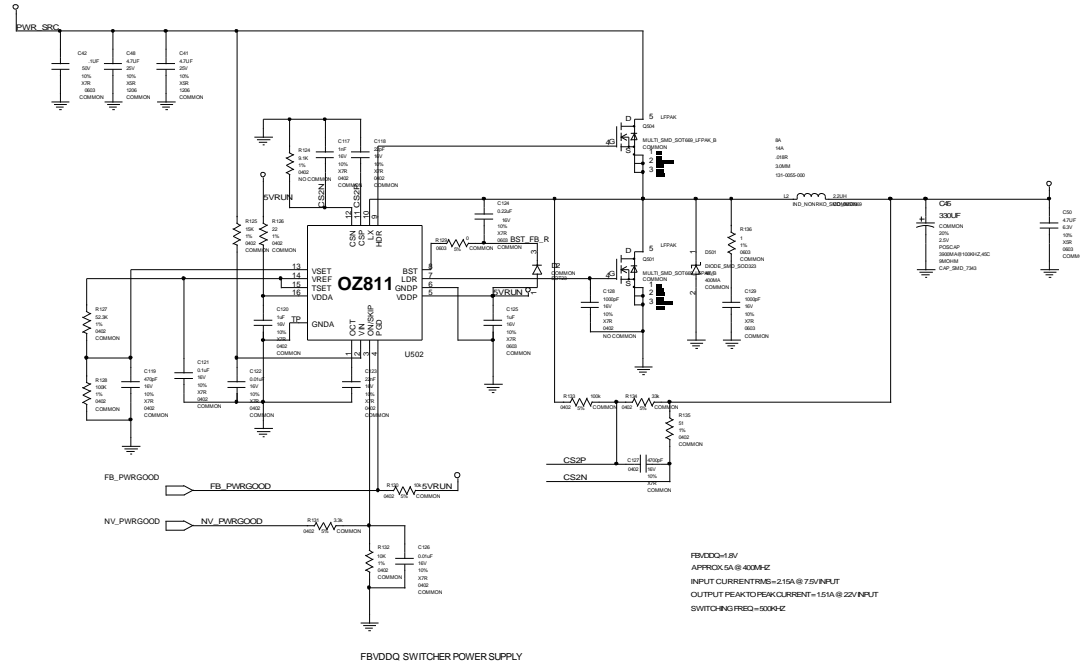
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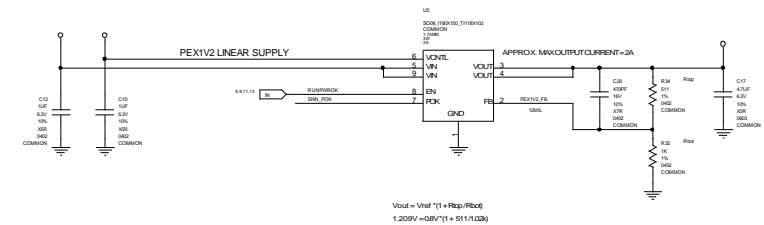
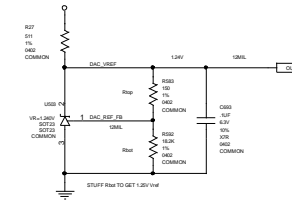
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NET	VOLTAGE	MIN. WIDTH, LINE	MIN. NET MAX. CURRENT
PEX1V2	1.2V	10MIL	2A
FBVDDQ	1.8V	10MIL	1A



DAC V. REFERENCE SUPPLY



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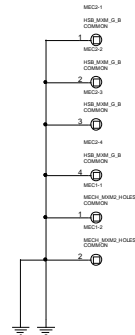
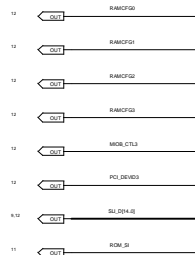
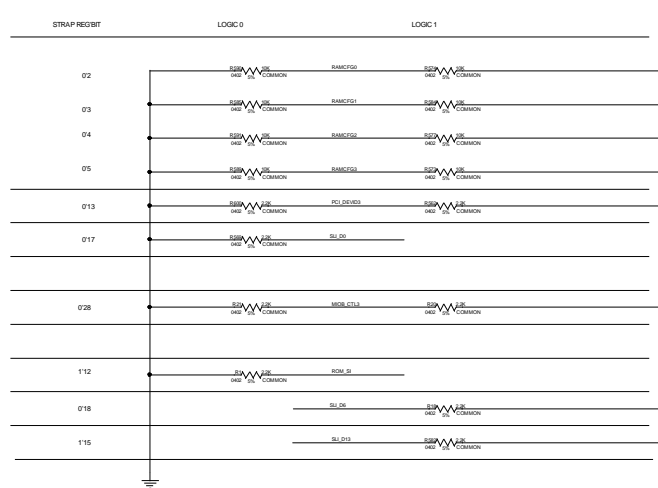
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DATE

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21 DEC 2008





RAM_CFG_0	<p>RAM_CFG[3]</p> <p>MS_0000: 16Mx16 DDR2 128Mx SRAM, EUDA.</p> <p>MS_0001: 16Mx16 DDR2 128Mx SRAM, SAMSUNG, MORON.</p> <p>MS_0010: 16Mx16 DDR2 128Mx SRAM, INFINEON.</p> <p>MS_0011: 16Mx16 DDR2 128Mx SRAM, HYNIX.</p> <p>MS_0100: 32Mx16 DDR2 128Mx SRAM, EUDA.</p> <p>MS_0101: 32Mx16 DDR2 128Mx SRAM, SAMSUNG, MORON.</p> <p>MS_0110: 32Mx16 DDR2 128Mx SRAM, INFINEON.</p> <p>MS_0111: 32Mx16 DDR2 128Mx SRAM, HYNIX.</p>
PCI_DEVID_3	<p>MS_0_DEVICE ID = 0x0407: G8M400.</p> <p>MS_1_DEVICE ID = 0x0408: G8M470.</p> <p>MS_1_DEVICE ID = 0x042B: G8M470.</p>
PEX_PU_EN_TERM100	
PCI_DEVID_EXT	
MIOA_EN_3.3V	
3GIO_PADCFG_LUT_ADR[0]	
SLOT_CLOCK_CONFIGURATION	

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PAGE DETAIL	STRAPS, TTP, MOUNTING HOLE

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