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Page	Description
	2010/11/30 1. P.21 ADD dual VBIOS 2. P.29 ADD 6262 3. P.30 remove NVVDD PWM 3. P31~P33 add V222-2.1 NVVDD 4. P.35 add thermal IC 5. add page number
	2010/12/01 1.change U6006 Vcc 2. ADD MEC8 3. page.32~33 remove NVDD mlcc 4. remove page.34 MEC1.5 5. remove MEC8 6. change L18 L19 to OL4-7670001 7. add thermal IC in PAGE.35
	2010/12/02 1. remove LB2 LB3 in PAGE.26 2. remove MEC1.3 3. remove M11 M12 PAGE.5 4. L17 to OL4-7670001 5. remove page 31.R898 R942 R253 R251 6. C97 C94 C137 C145 C104 C118 to 0805 7.ADD C655 8. remove PAGE13. FBA MLCC
	12/06 1.remove R517 page25.
	12/07 1.Add C705 C689 C583 C584 C1063

REV	VARIANT	N/PPN	ASSEMBLY
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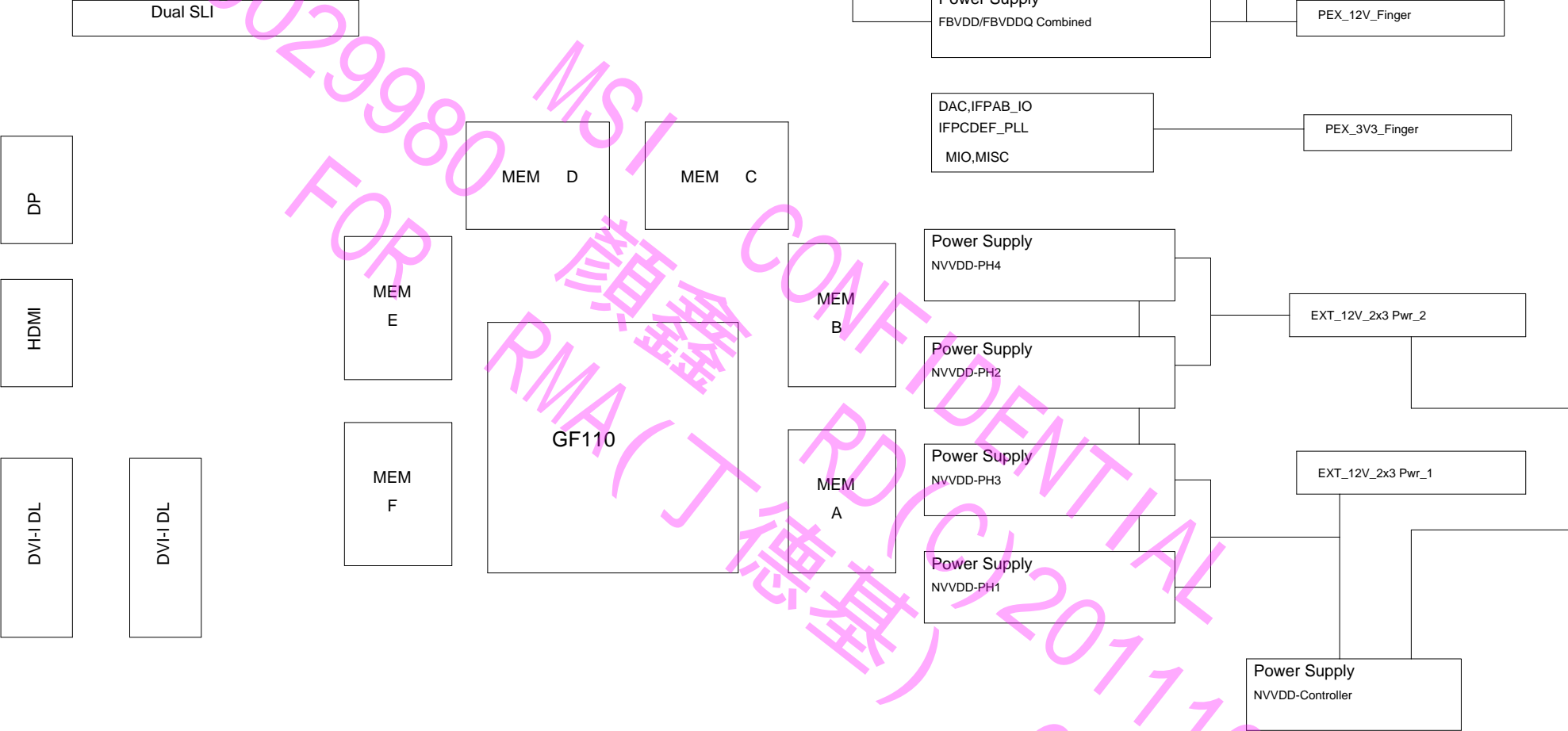
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Block Diagram

Power Sequence

5V - Always On
3V3 - Always On
12V_F - Always On
12V_PEX6_EXT1 - Always On
12V_PEX6_EXT2 - Always On
NVVDD -Input_Pex_Power_Rail_Enable
+ Thermal_Shutdown
-NVVDD_PGOOD
-Following FBVDDQ

FBVDD/FBVDDQ
PEX_VDD



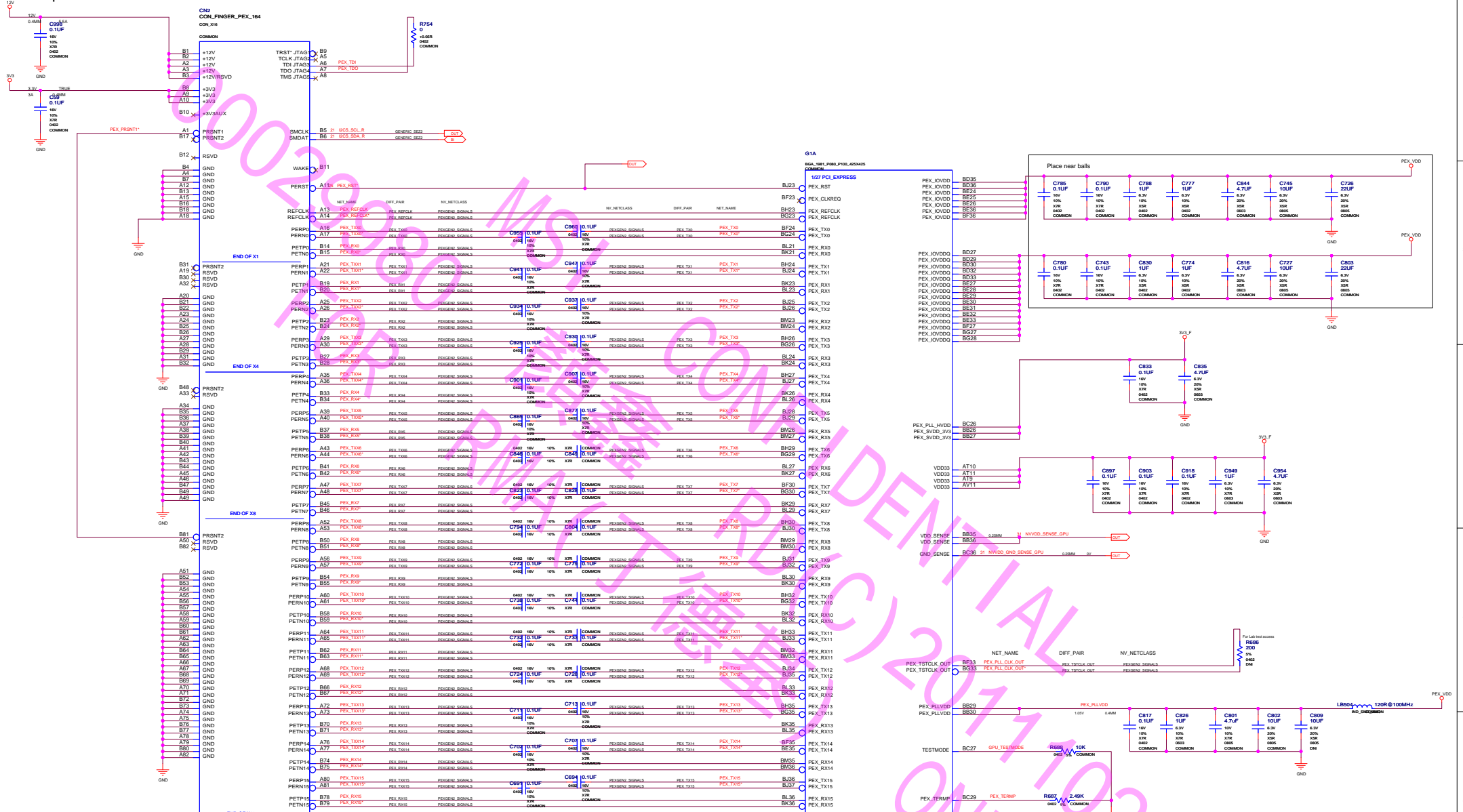
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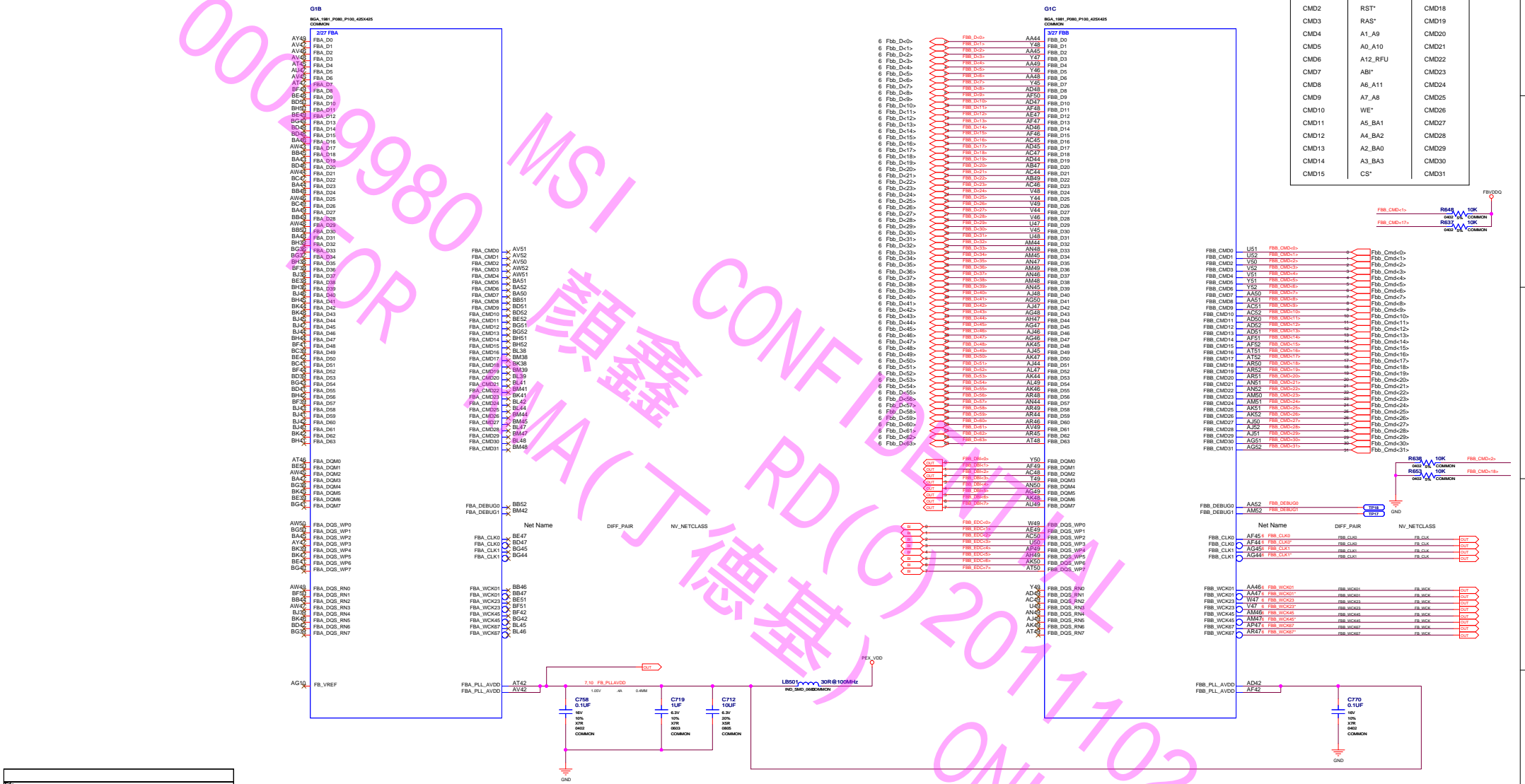
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PCI Express 2.0

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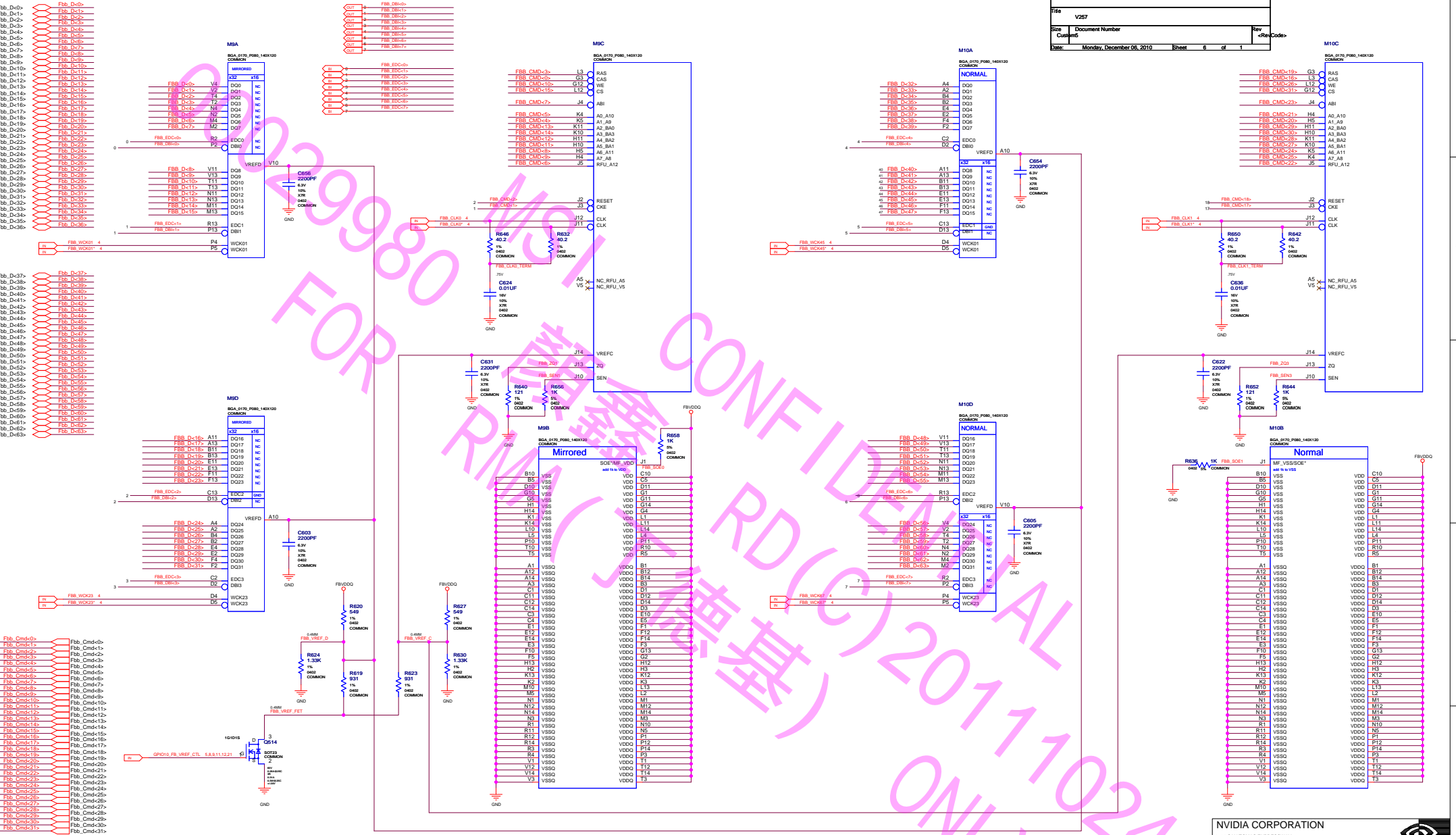
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GPU Framebuffer: Partition C/D


GDDR5 CMD Mapping		
0..31	CMD	32..63
CMD0	CAS*	CMD16
CMD1	CKE*	CMD17
CMD2	RST*	CMD18
CMD3	RAS*	CMD19
CMD4	A1, A9	CMD20
CMD5	A0, A10	CMD21
CMD6	A12, RFU	CMD22
CMD7	AB1*	CMD23
CMD8	A6, A11	CMD24
CMD9	A7, A8	CMD25
CMD10	WE*	CMD26
CMD11	A5, BA1	CMD27
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CMD13	A2, BA0	CMD29
CMD14	A3, BA3	CMD30
CMD15	CS*	CMD31



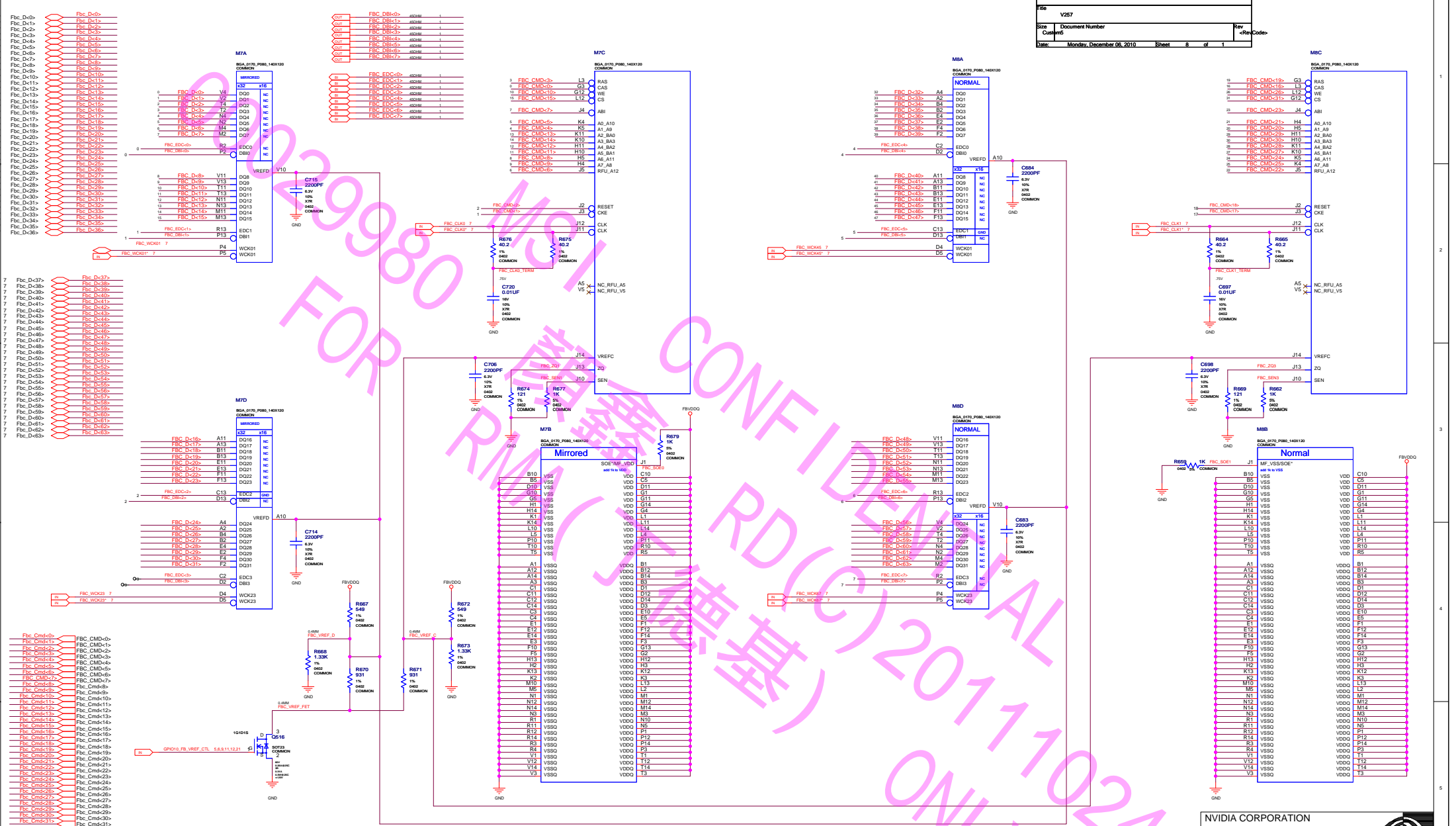
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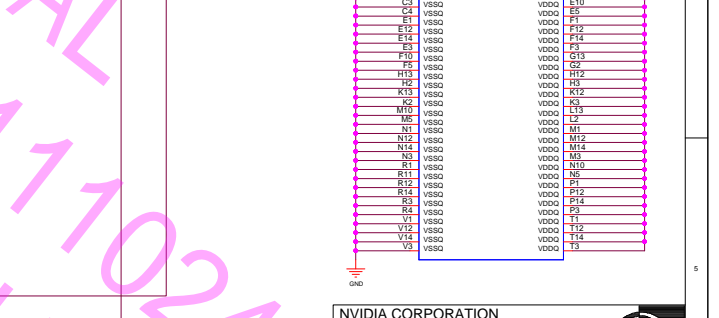
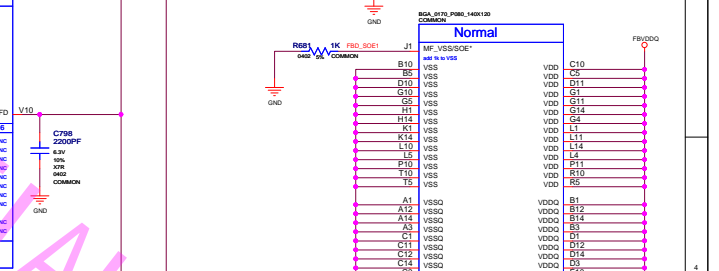
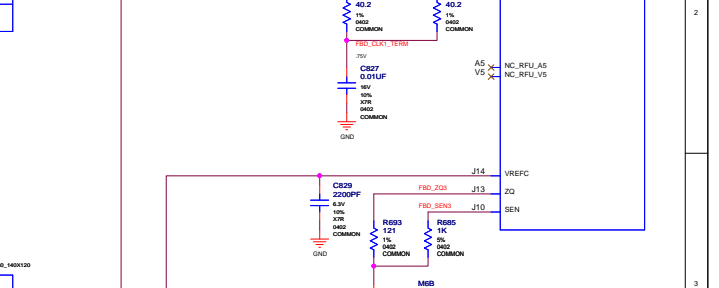
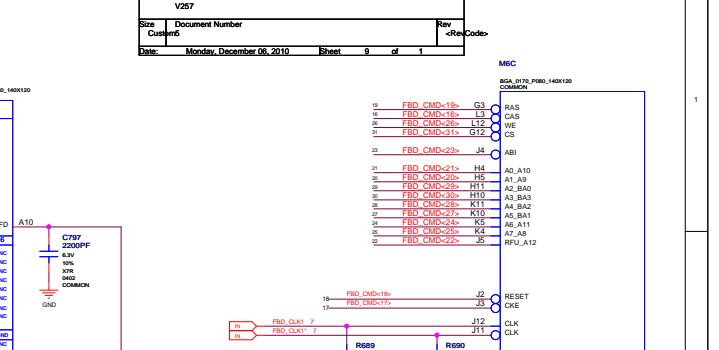
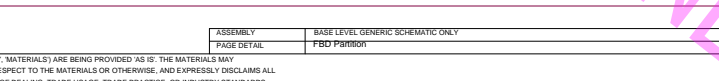
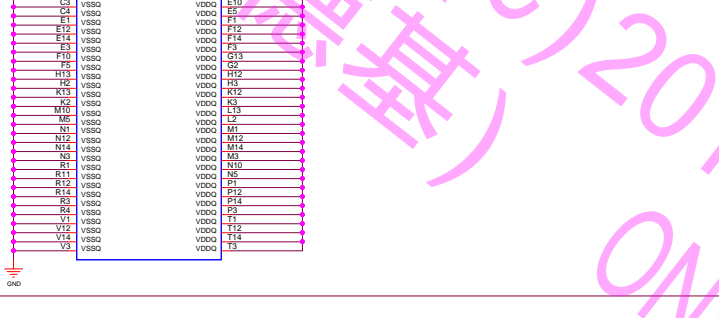
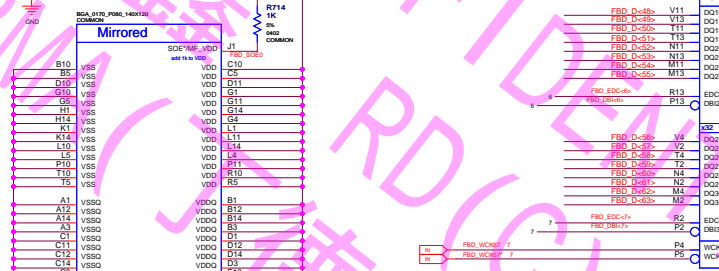
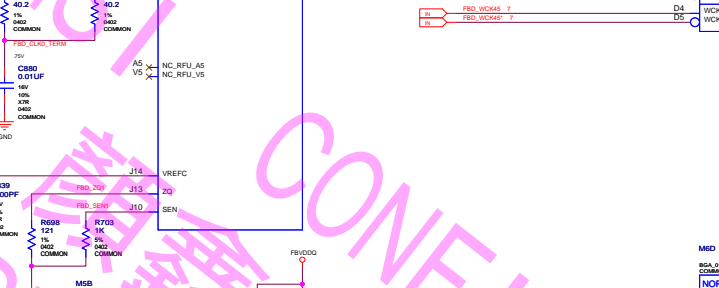
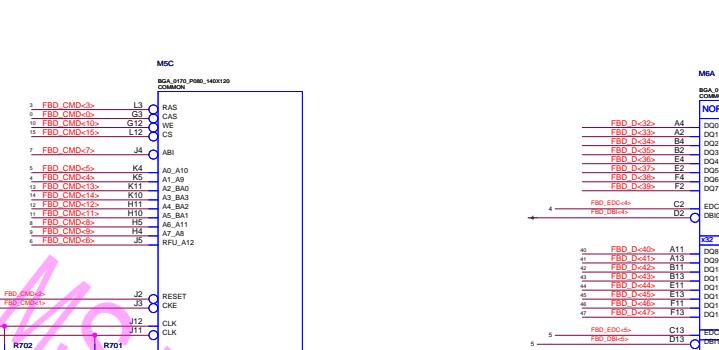
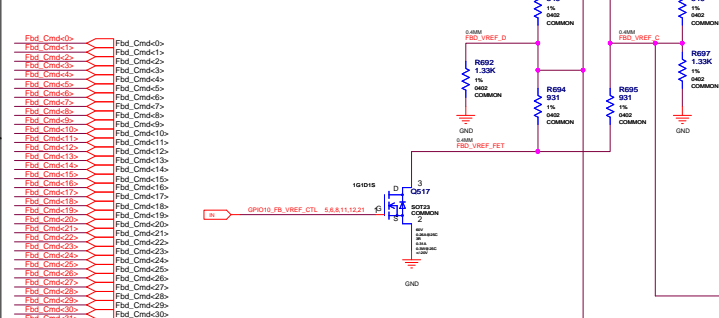
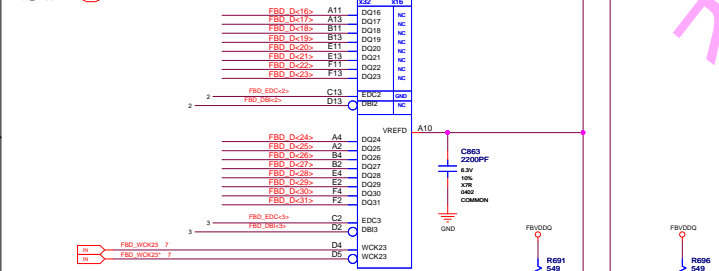
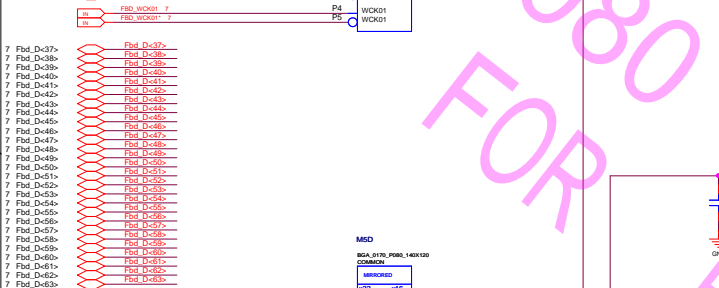
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PAGE DETAIL	GPU Framebuffer: Partition C/D

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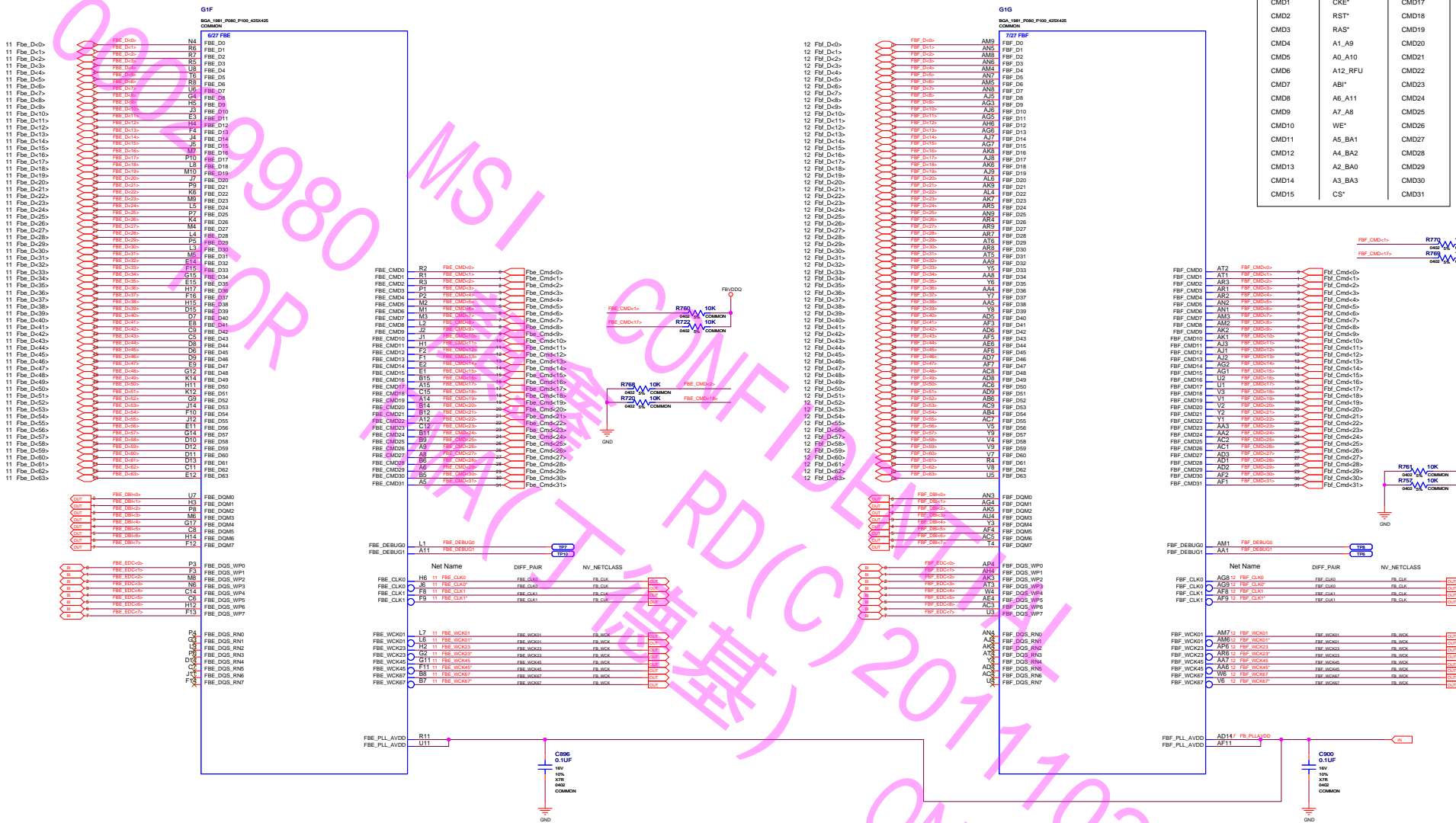
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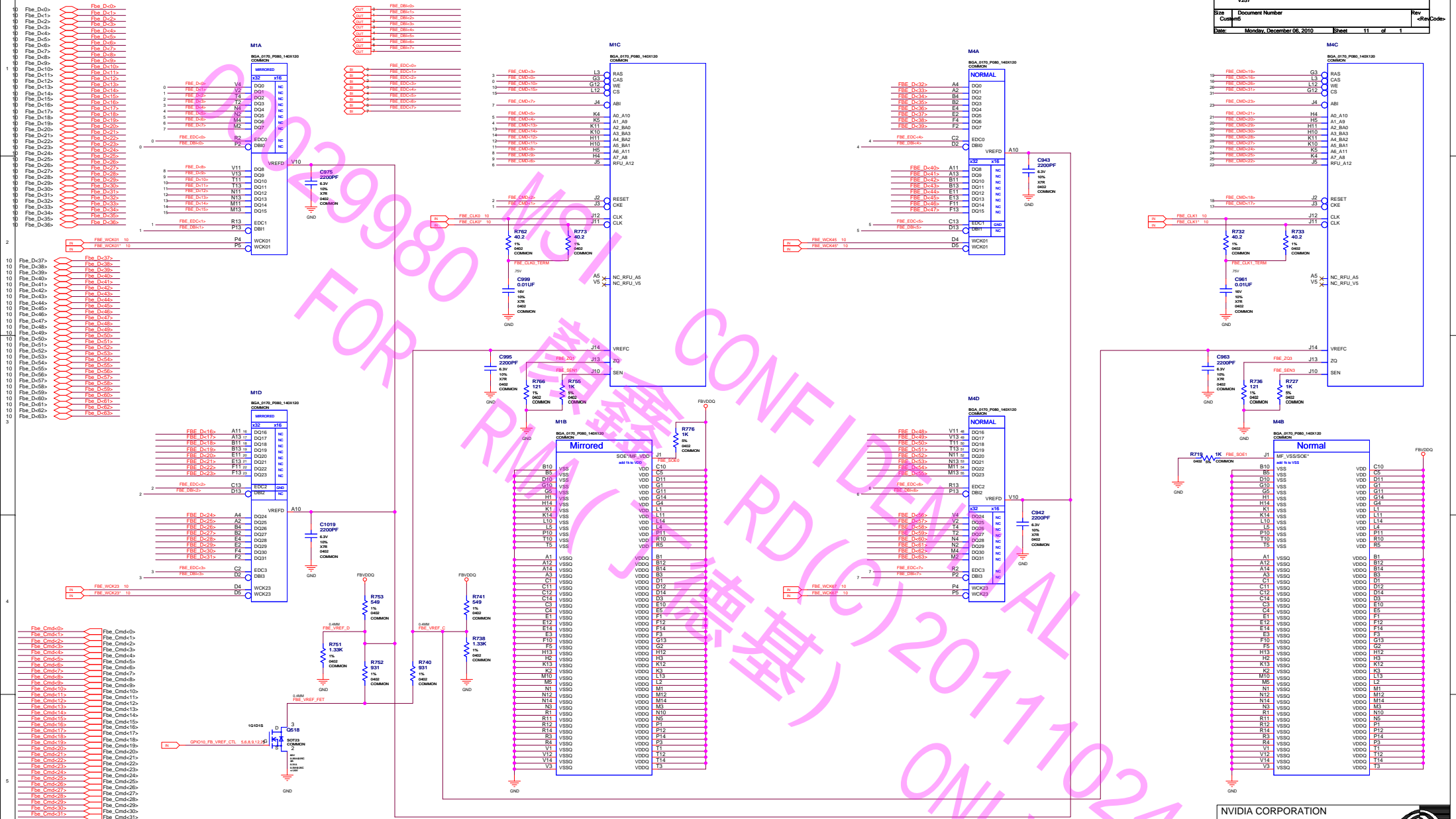
GPU Framebuffer: Partition E/F

GDDR5 CMD Mapping		
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CMD9	A7, A8	CMD25
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CMD12	A4, BA2	CMD28
CMD13	A2, BA0	CMD29
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CMD15	CS*	CMD31



MEMORY: FBE Partition

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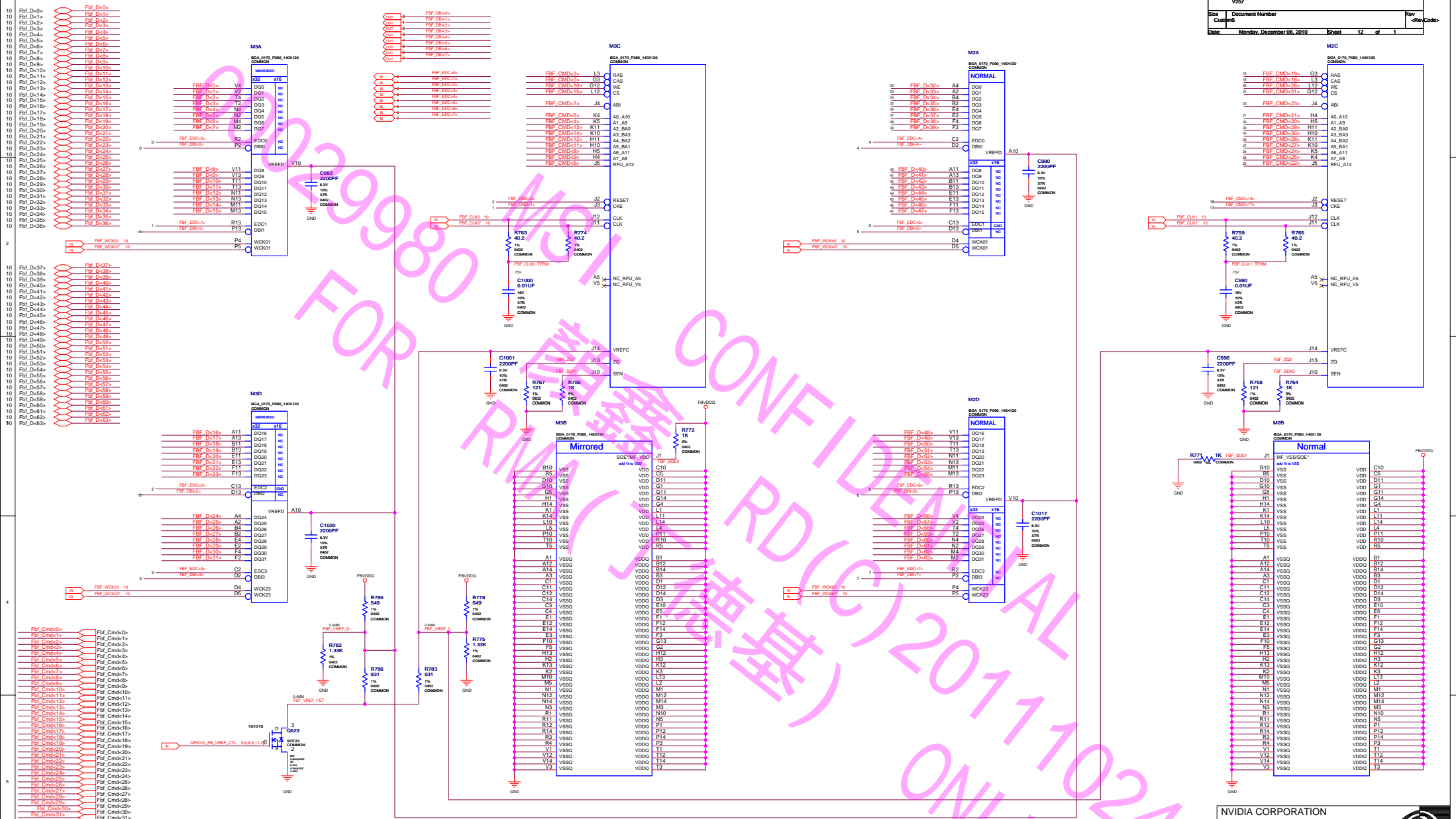
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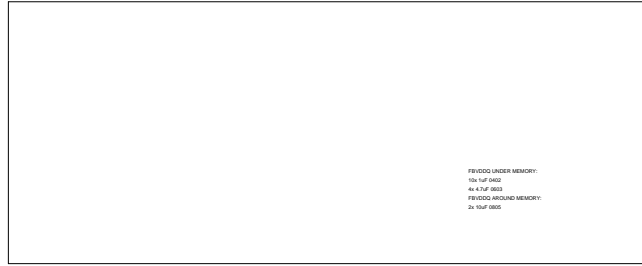
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GDDR5 Memory Decoupling

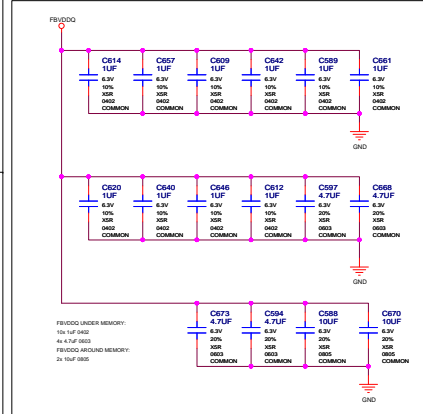
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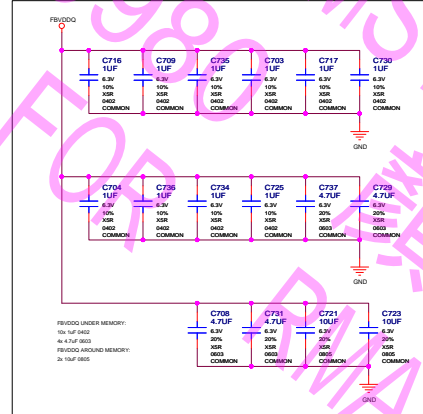
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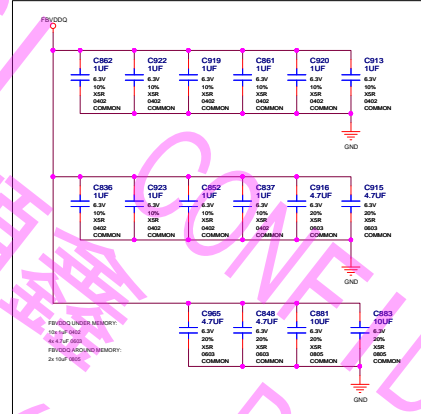
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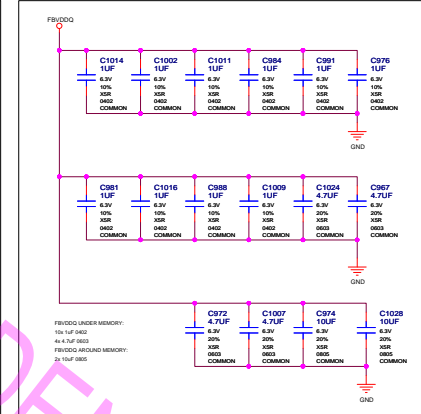
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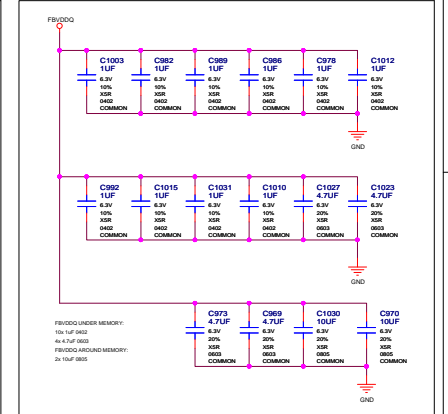
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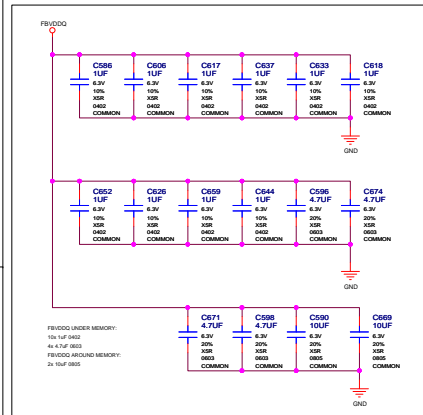
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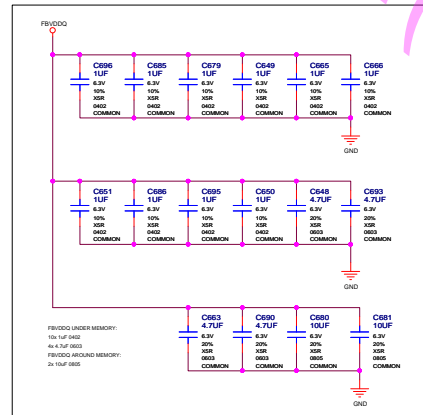
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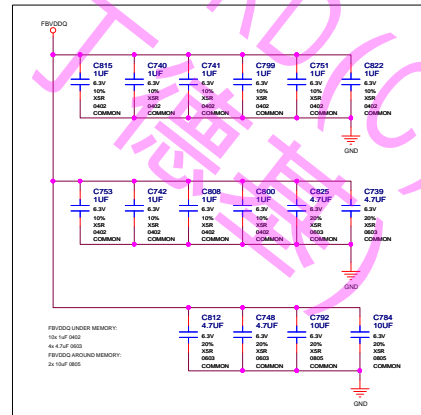
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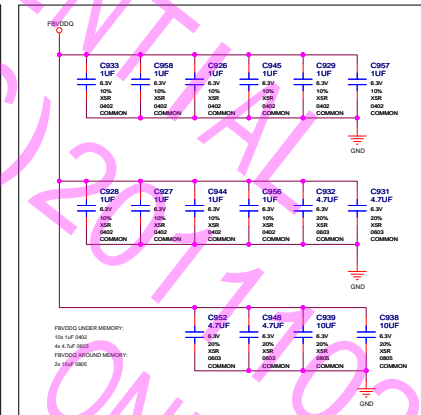
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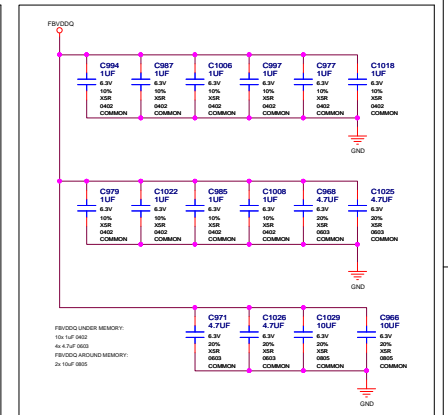
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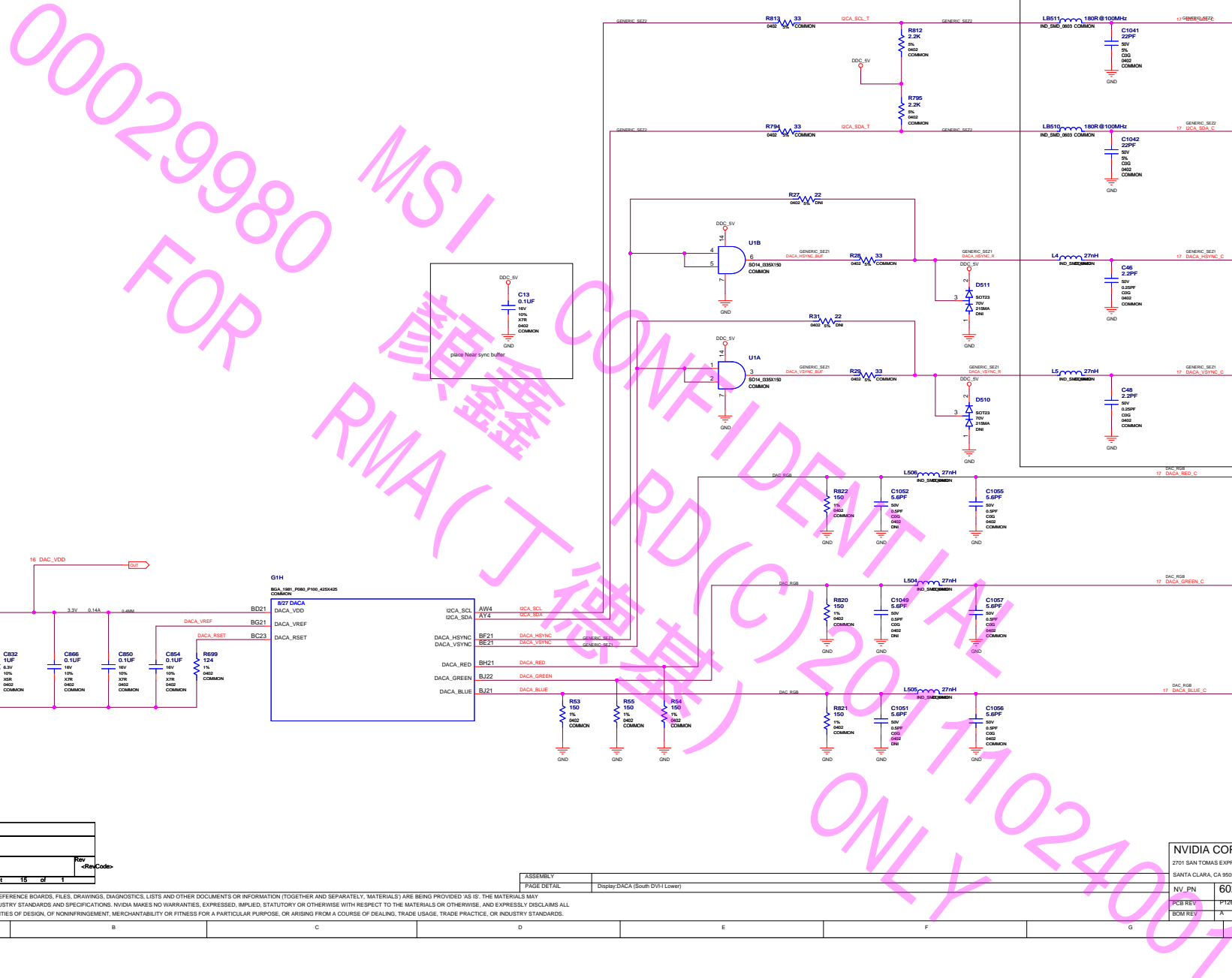


FBVDDQ under GPU
0.1uF 0402 X7R x8
0.47uF 0402 X5R x8
1uF 0402 X5R x8
FBVDDQ around GPU
4.7uF 0603 X5R x8
10uF 0805 X5R x6
22uF 0805 X5R x6

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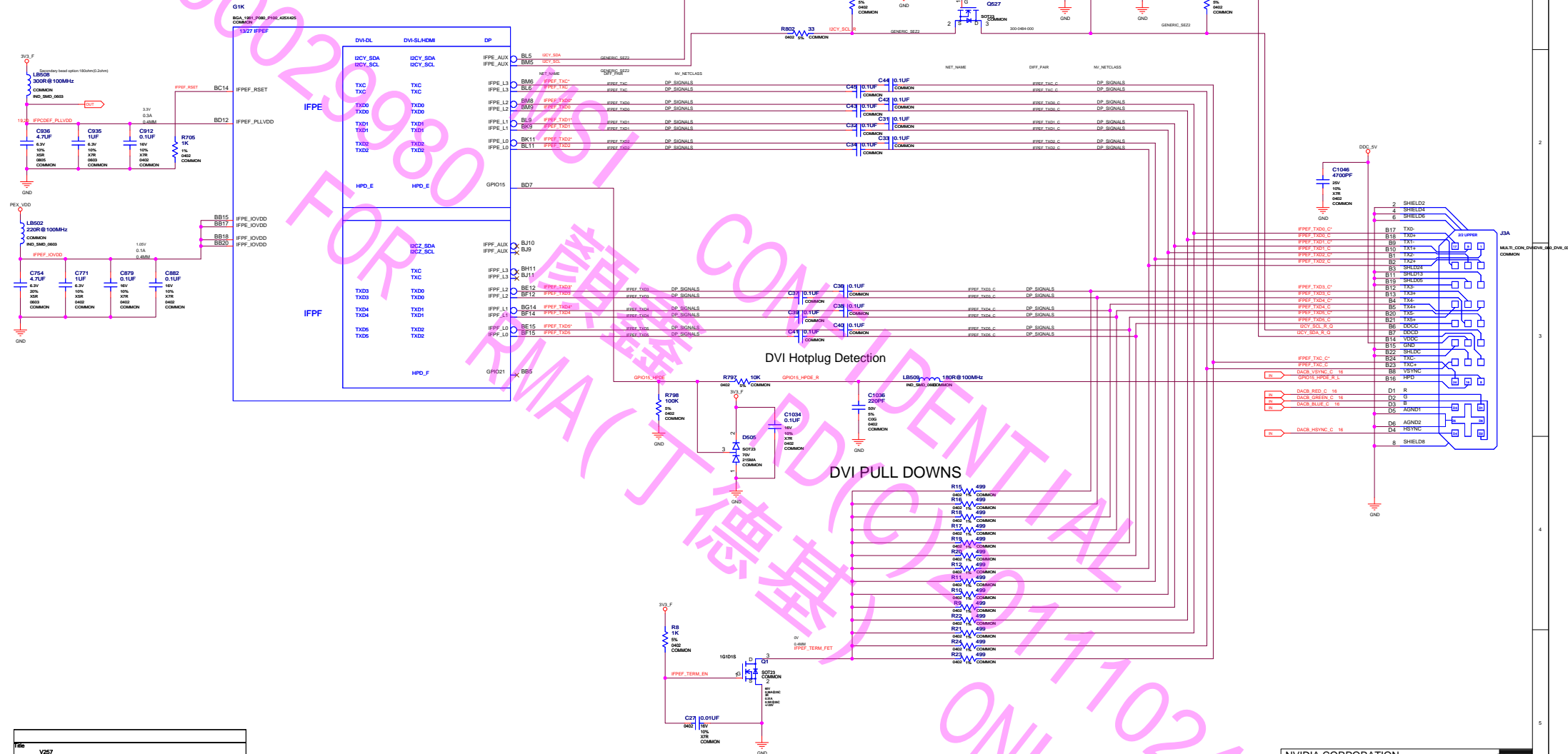
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ASSEMBLY	
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IFP E/F Interface (South DVI-I Upper)



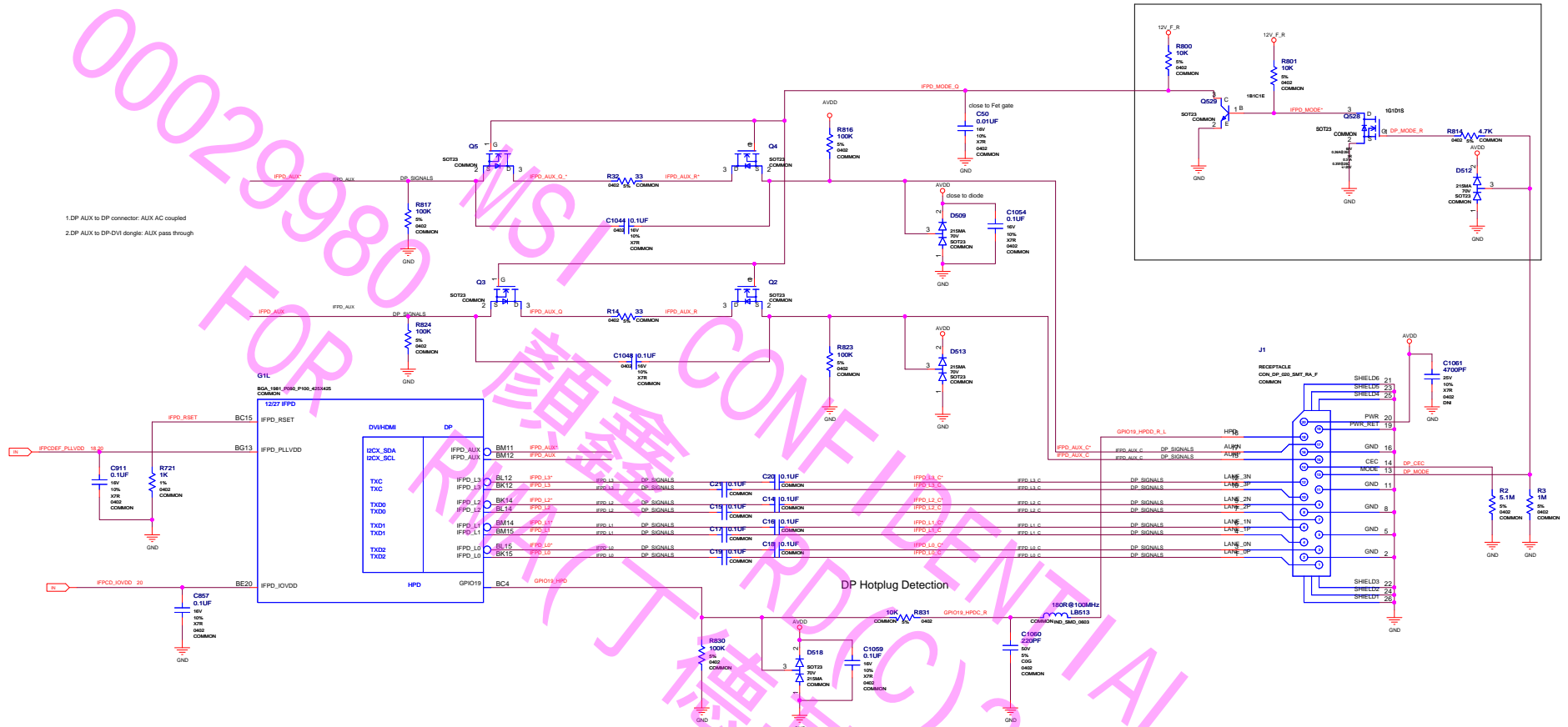
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- 1.DP AUX to DP connector: AUX AC coupled
2.DP AUX to DP-DVI dongle: AUX pass through



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IFPC Interface (Mid HDMI)

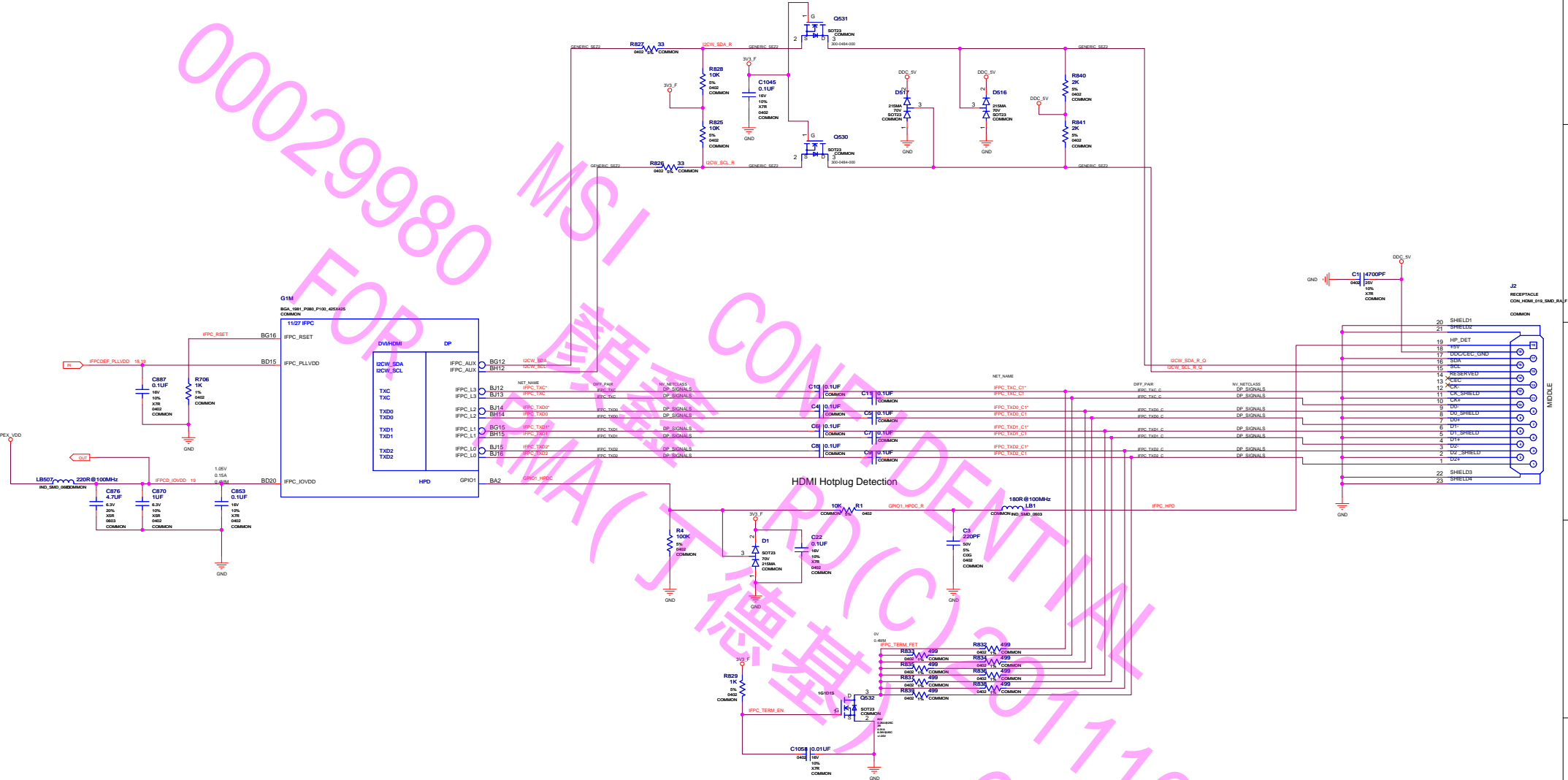
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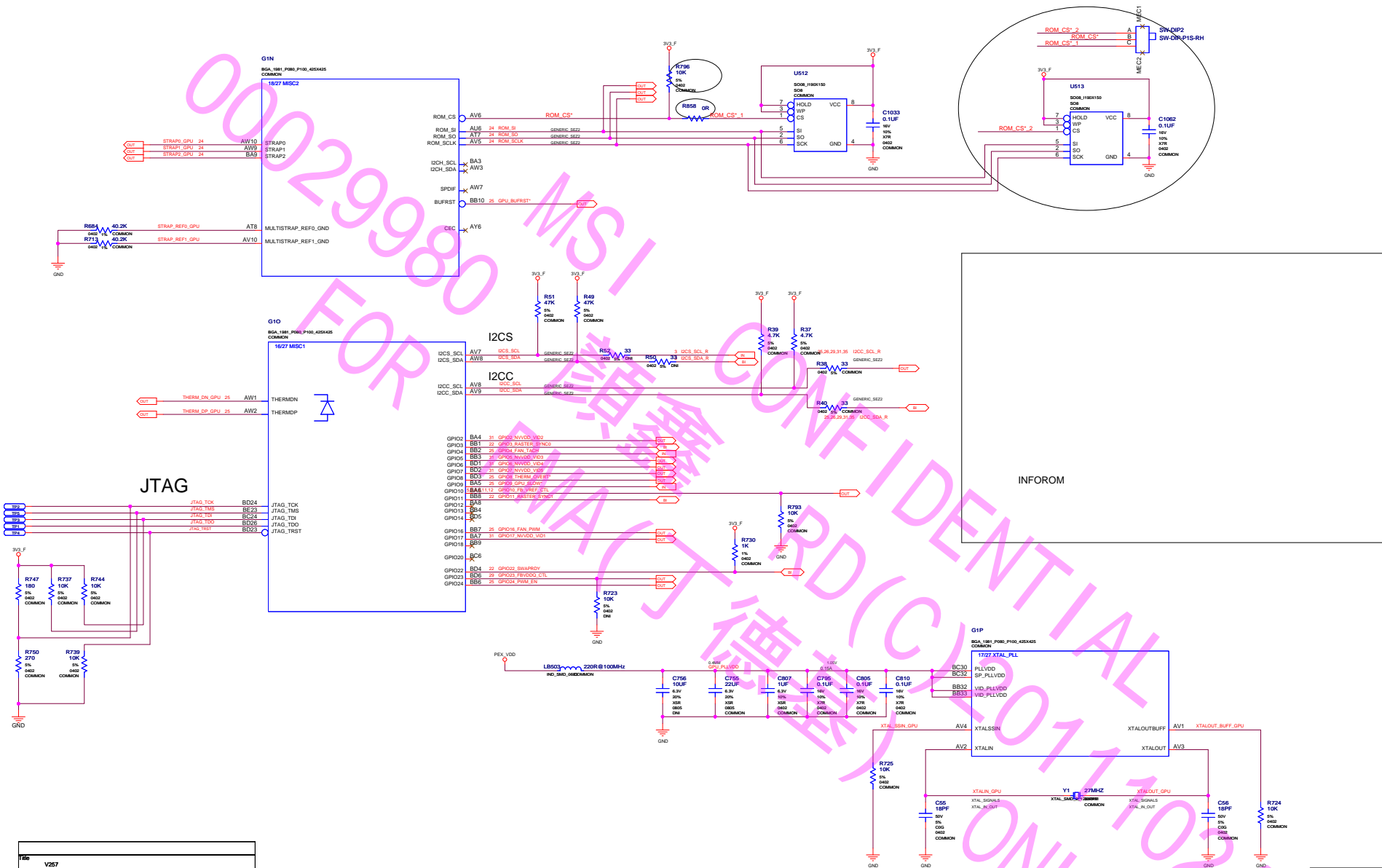
ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
IFPC Interface (Mid HDMI)

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MISC: GPIO, I2C, ROM, and XTAL



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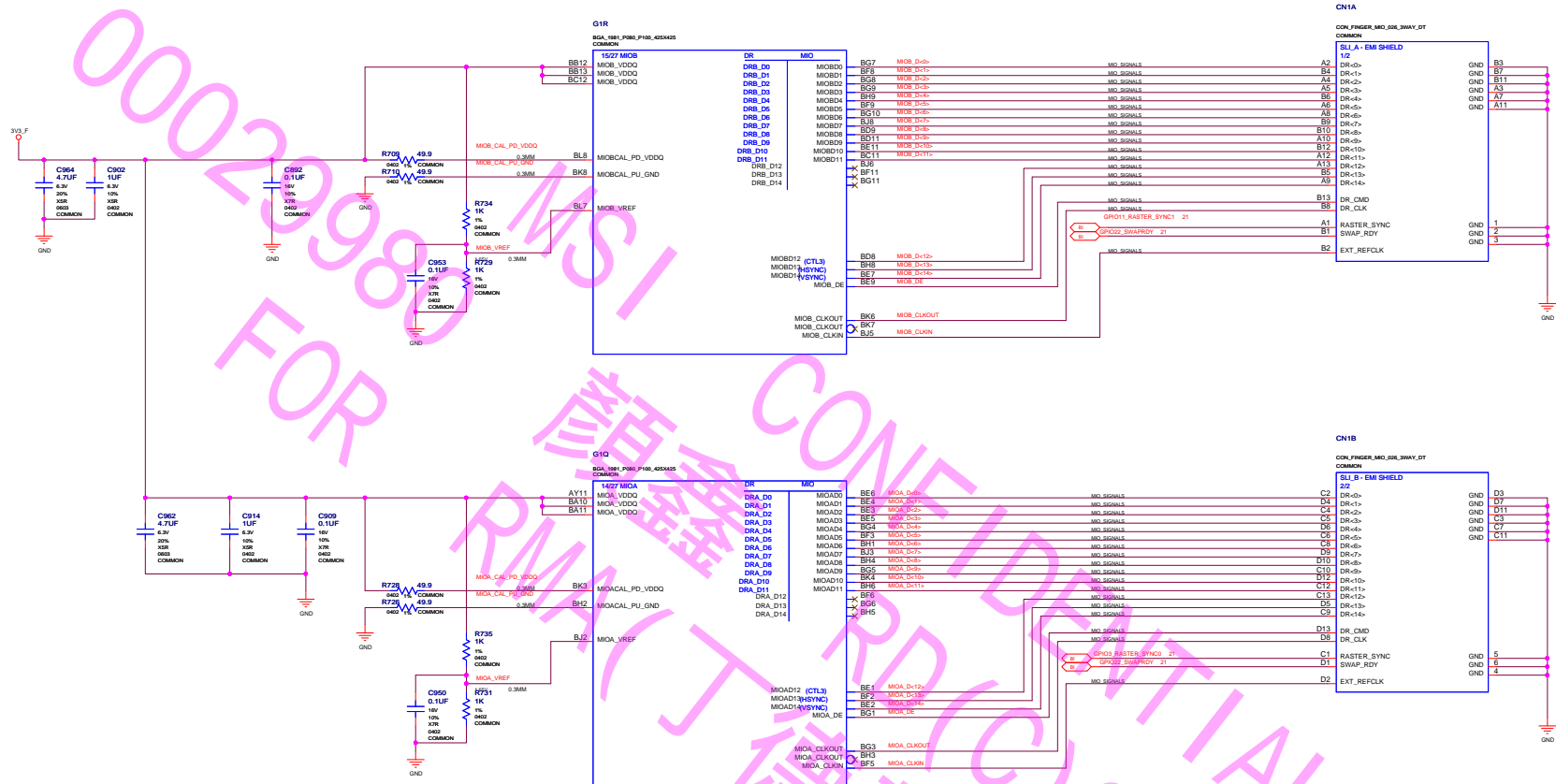
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PAGE DETAIL	MISC: GPIO, I2C, ROM, and XTAL

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Multi-use IO(MIO) Interface



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	Multi-use IO(MIO) Interface

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GPU POWER CONNECTIONS




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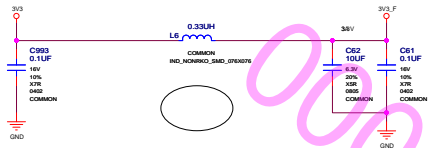
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

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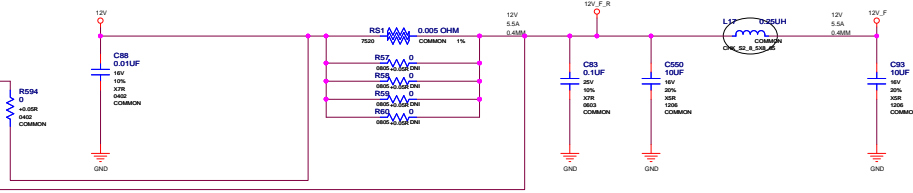


Power Supply: PEX PS INPUT, DETECTION LOGIC

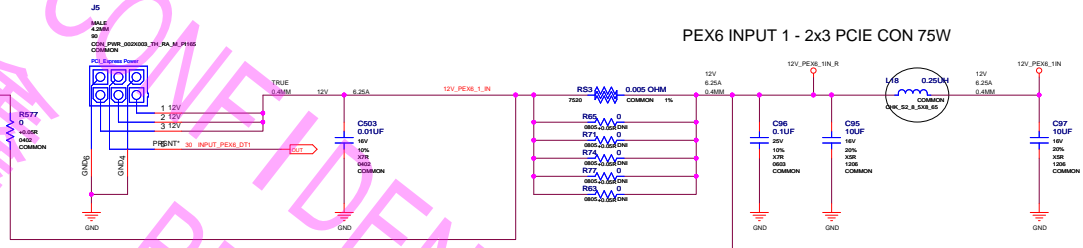
PEX_3V3 INPUT - 10W



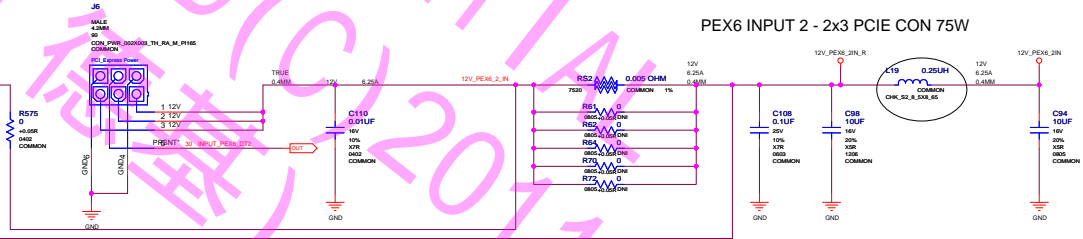
PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX6 INPUT 2 - 2x3 PCIE CON 75W



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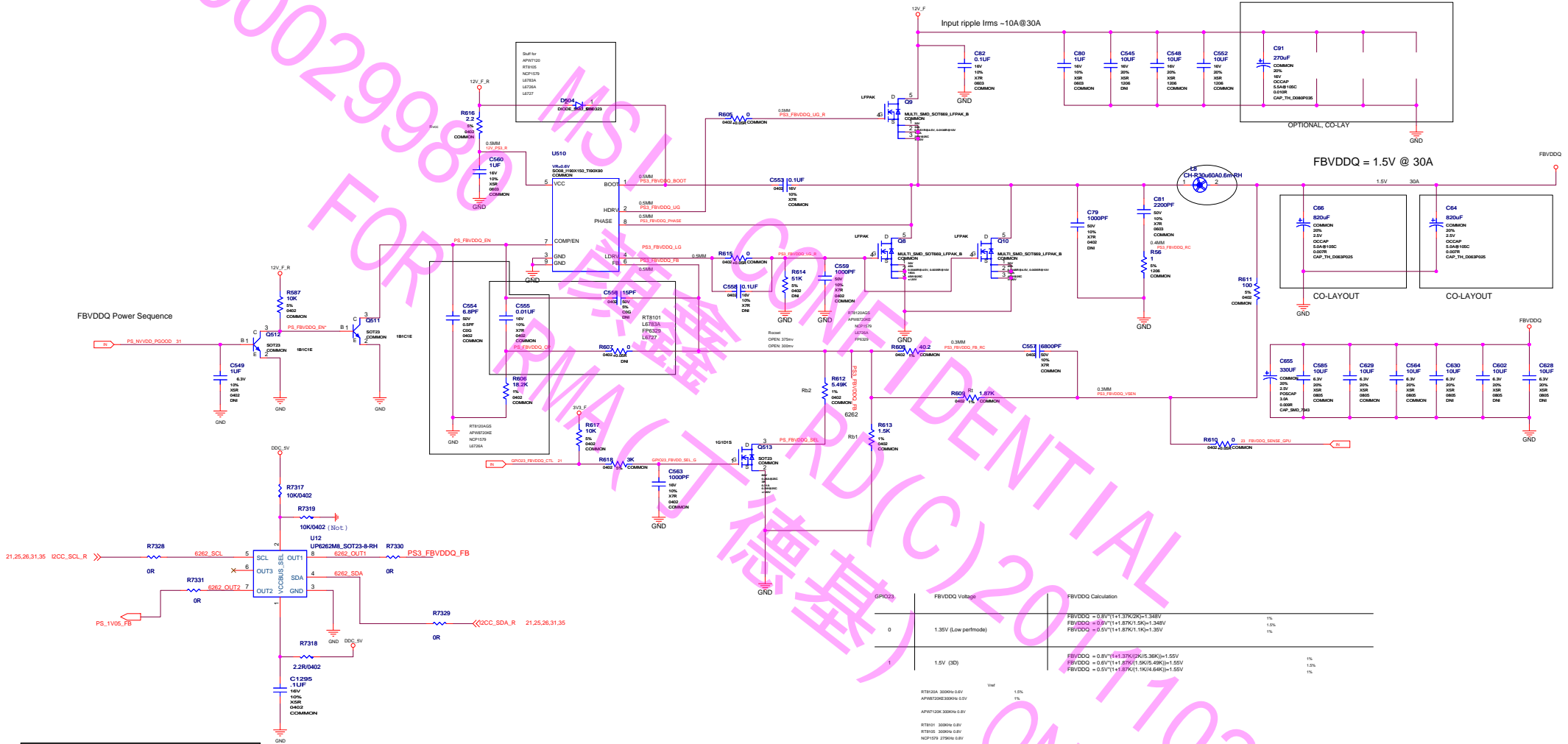
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Power Supply: FBVDDQ



FBVDDQ Voltage		FBVDDQ Calculation	
0	1.35V (Low perfmode)	FBVDDQ = 0.8V*(1+3.7K/2K)=1.348V	1%
		FBVDDQ = 0.8V*(1+1.87K/1.0K)=1.348V	1%
		FBVDDQ = 0.5V*(1+1.87K/1.1K)=1.35V	1%
1	1.5V (3D)	FBVDDQ = 0.8V*(1+3.7K/2K/0.39K)=1.55V	1%
		FBVDDQ = 0.8V*(1+1.87K/1.5K/0.49K)=1.55V	1.5%
		FBVDDQ = 0.5V*(1+1.87K/1.1K/0.64K)=1.55V	1%

RT8101A 300mA@0.5V	1.5%
AP7101A 300mA@0.5V	1%
AP7101A 300mA@0.5V	1%
RT8101A 300mA@0.5V	1.5%
RT8101A 300mA@0.5V	1.5%
RT8101A 300mA@0.5V	1.5%

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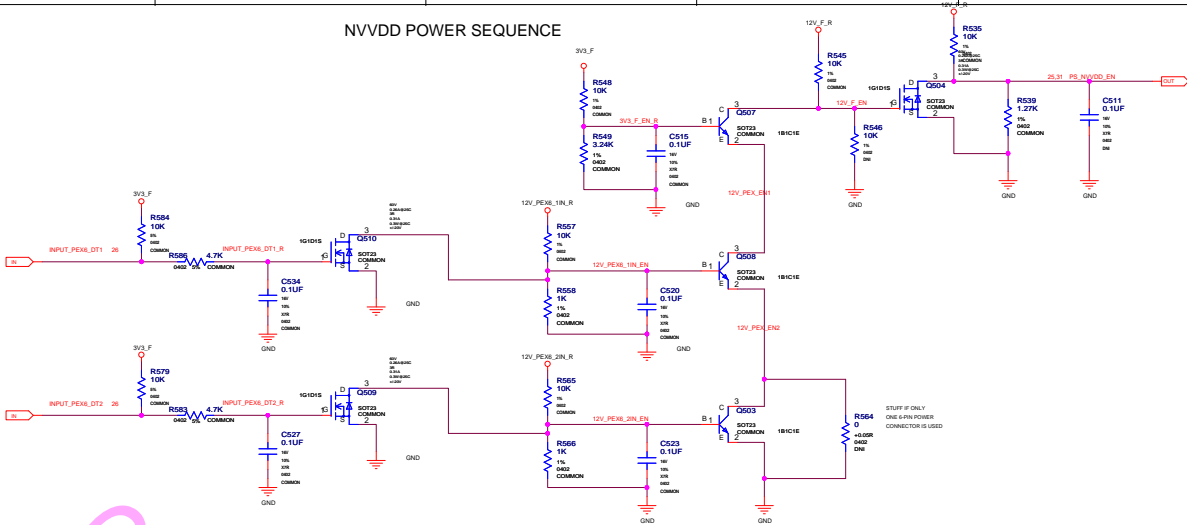
ASSEMBLY	Power Supply FBVDDQ
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Power Supply: NVVDD Controller

NVVDD POWER SEQUENCE



VID Table

GPIO7 VID_5	GPIO6 VID_4	GPIO5 VID_3	GPIO2 VID_2	GPIO17 VID_1	VRM11.0 VID Setting
0	0	0	0	1	1.20000V
0	0	0	1	0	1.18750V
0	0	0	1	1	1.17500V
0	0	1	0	0	1.16250V
0	0	1	0	1	1.15000V
0	0	1	1	0	1.13750V
0	0	1	1	1	1.12500V
0	1	0	0	0	1.11250V
0	1	0	0	1	1.10000V
0	1	0	1	0	1.08750V
0	1	0	1	1	1.07500V
0	1	1	0	0	1.06250V
0	1	1	0	1	1.05000V
0	1	1	1	0	1.03750V
0	1	1	1	1	1.02500V
1	0	0	0	0	1.01250V
1	0	0	0	1	1.00000V
1	0	0	1	0	0.98750V
1	0	0	1	1	0.97500V
1	0	1	0	0	0.96250V
1	0	1	0	1	0.95000V
1	0	1	1	0	0.93750V
1	0	1	1	1	0.92500V
1	1	0	0	0	0.91250V
1	1	0	0	1	0.90000V
1	1	0	1	0	0.88750V
1	1	0	1	1	0.87500V
1	1	1	0	0	0.86250V
1	1	1	0	1	0.85000V
1	1	1	1	0	0.83750V
1	1	1	1	1	0.82500V

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	Power Supply NVVDD Controller

RLIM1=5.62K,RLIM2 = 28.7K to set SW FREQ=300KHz,DCP=400A

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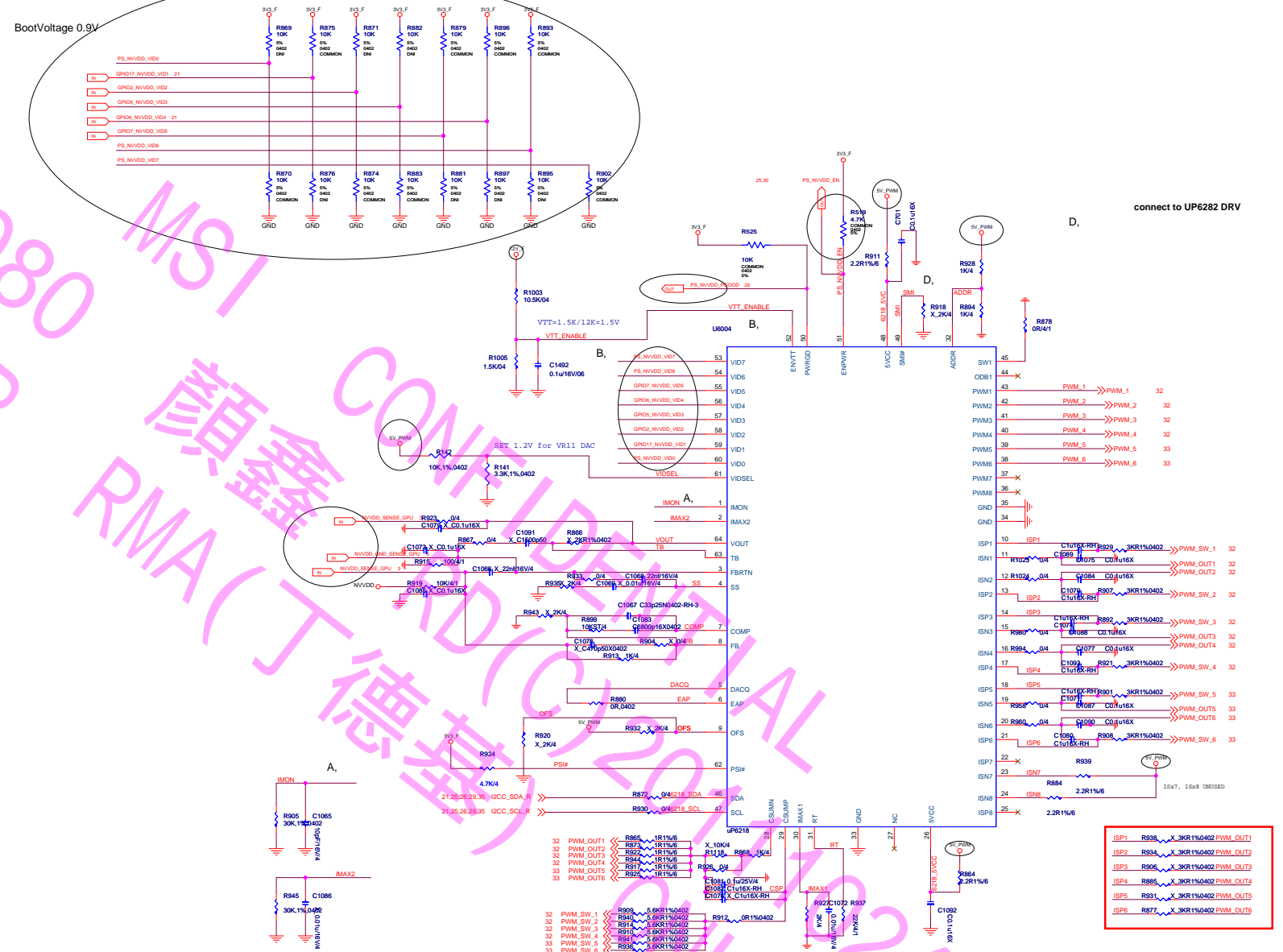
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Power Supply: NVVDD Regulator

VID Table	
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2	0
3	0
4	0
5	0
6	0
7	0
8	0
9	0
10	0
11	0
12	0
13	0
14	0
15	0
16	0
17	0
18	0
19	0
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171	0
172	0
173	0
174	0
175	0
176	0
177	0
178	0
179	0
180	0
181</	

GPI07 VID_5	GPI06 VID_4	GPI05 VID_3	GPI02 VID_2	GPI017 VID_1	VOUT
0	0	0	0	0	1.21250V
0	0	0	0	1	1.20000V
0	0	0	1	0	1.18750V
0	0	0	1	1	1.17500V
0	0	1	0	0	1.16250V
0	0	1	0	1	1.15000V
0	0	1	1	0	1.13750V
0	0	1	1	1	1.12500V
0	1	0	0	0	1.11250V
0	1	0	0	1	1.10000V
0	1	0	1	0	1.08750V
0	1	0	1	1	1.07500V
0	1	1	0	0	1.06250V
0	1	1	0	1	1.05000V
0	1	1	1	0	1.03750V
0	1	1	1	1	1.02500V
1	0	0	0	0	1.01250V
1	0	0	0	1	1.00000V
1	0	0	1	0	0.98750V
1	0	0	1	1	0.97500V
1	0	1	0	0	0.96250V
1	0	1	0	1	0.95000V
1	0	1	1	0	0.93750V
1	0	1	1	1	0.92500V
1	1	0	0	0	0.91250V
1	1	0	0	1	0.90000V
1	1	0	1	0	0.88750V
1	1	0	1	1	0.87500V
1	1	1	0	0	0.86250V
1	1	1	0	1	0.85000V
1	1	1	1	0	0.83750V
1	1	1	1	1	0.82500V

BootVoltage 0.9V



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PAGE DETAIL	Power Supply: NVVDD Regulator

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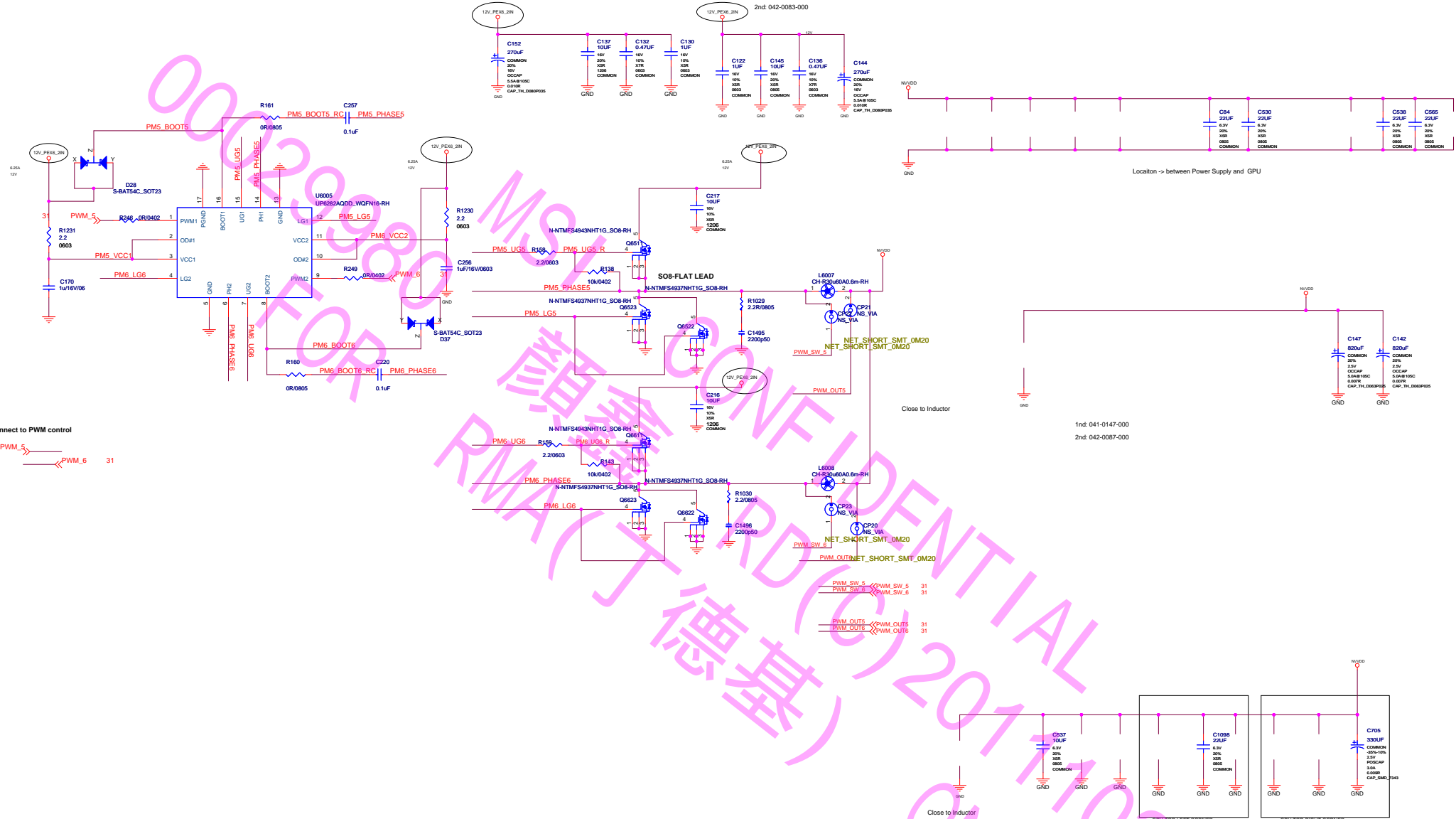
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Power Supply: NVVDD PHASE 5, 6



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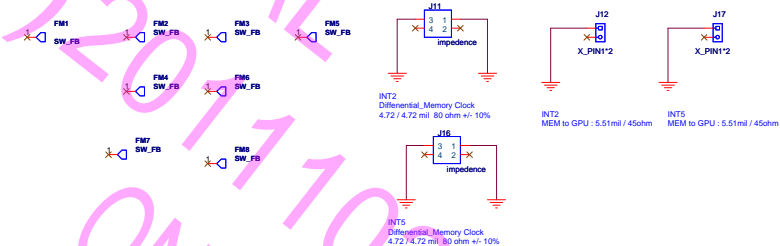
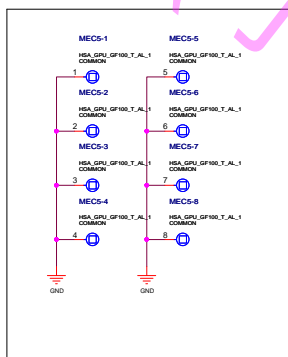
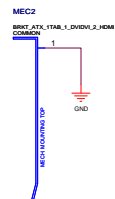
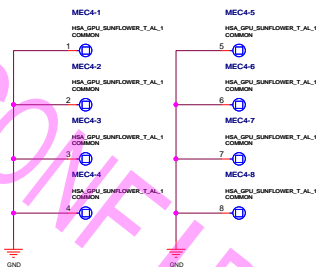
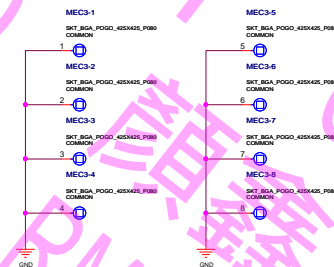
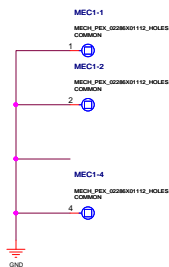
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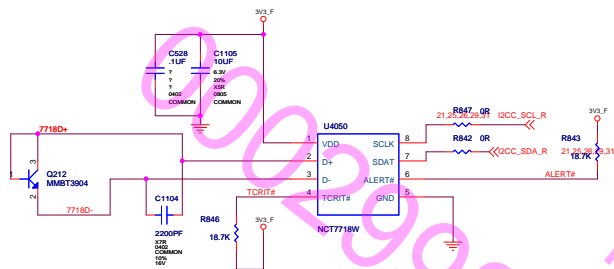


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