

PG410 A01

GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D +DVI-D + HDMI+ DP

TABLE OF CONTENTS


Page	Description	Page	Description
1	Table of Contents	26	PS: 1V8_PLL, 1V8_AON
2	Block Biagram	27	PS: 5V, PEX_VDD
3	PCI Express	28	PS: NV3V3, NV12V
4	GPU FB_AB	29	PS: FBVDD
5	MEMORY: FBA[31:0]	30	PS: NVVDD Controller
6	MEMORY: FBA[63:32]	31	PS: NVVDD Phase 1,2 & 3
7	MEMORY: FBB[31:0]	32	PS: NVVDD Rail Balance Login & Dynamic Phase
8	MEMORY: FBB[63:32]	33	PS: Input, Filtering, and Monitoring
9	MEM FB_AB PWR	34	PS: 12V Power Steering,PSI Control & LED
10	GPU FB_CD	35	PS: Shut Down and Sequencing
11	MEMORY: FBC[31:0]	36	PS: GC6 MISC
12	MEMORY: FBC[63:32]	37	MECH
13	MEMORY: FBD[31:0]		
14	MEMORY: FBD[63:32]		
15	MEM FB_CD PWR		
16	GPU PWR & GND		
17	GPU Decoupling		
18	IFPAB DVI-D-DL		
19	IFPE DP		
20	IFPF DP		
21	IFPC HDMI/DP		
22	IFPD DP		
23	MIOA/B Interface and Frame Lock		
24	MISC1: Fan, Thermal, JTAG, GPIO,STEREO		
25	MISC2: ROM, XTAL,STRAPS		

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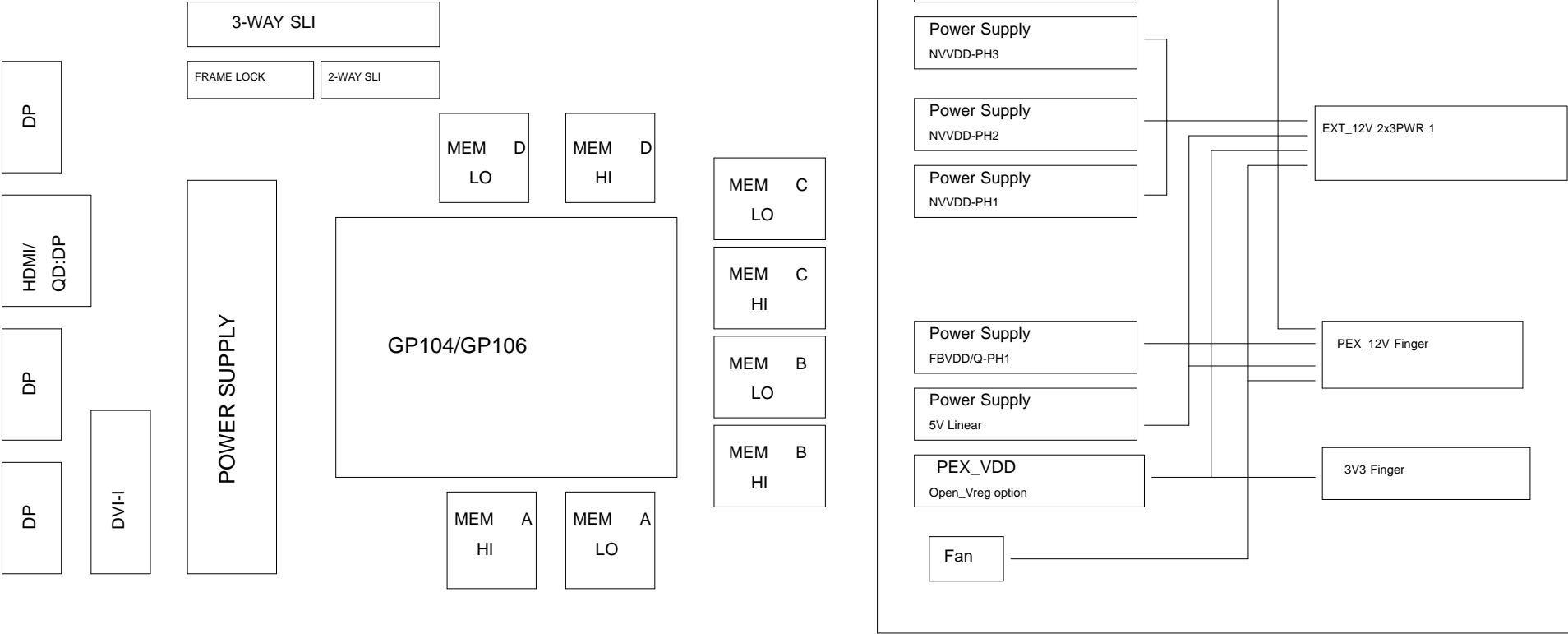
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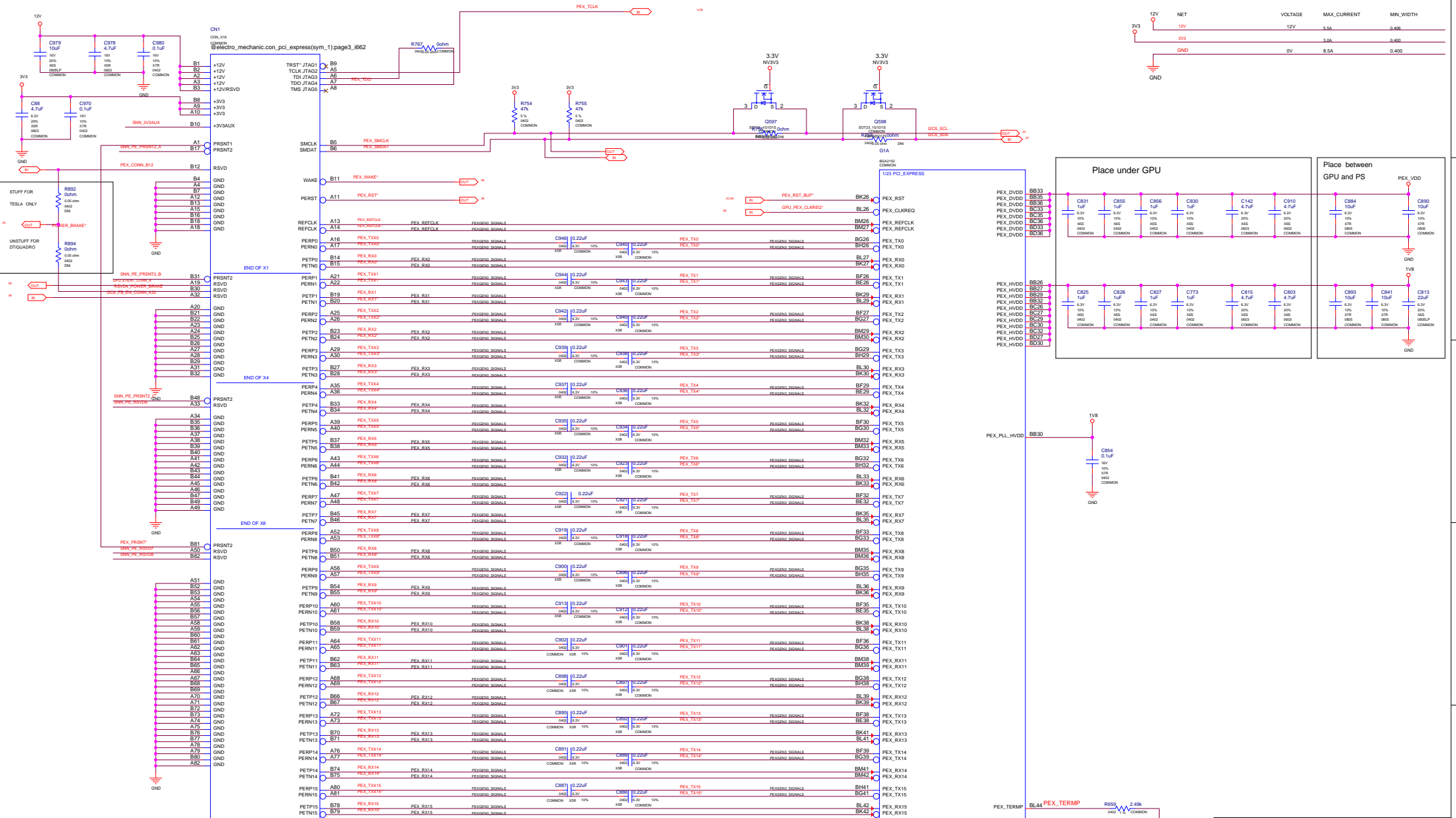
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PCB REV	PG410-A01	PAGE	1 OF 37
BCM REV	A	DATE	dd-mon-year



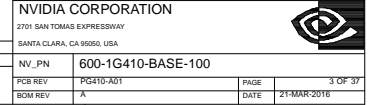
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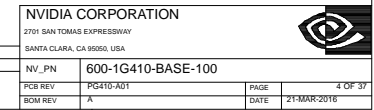
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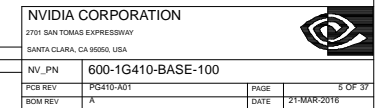
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NV_PN	600-1G410-BASE-100		
PCB REV	PG410-A01	PAGE	2 OF 37
BCM REV	A	DATE	21-MAR-2016

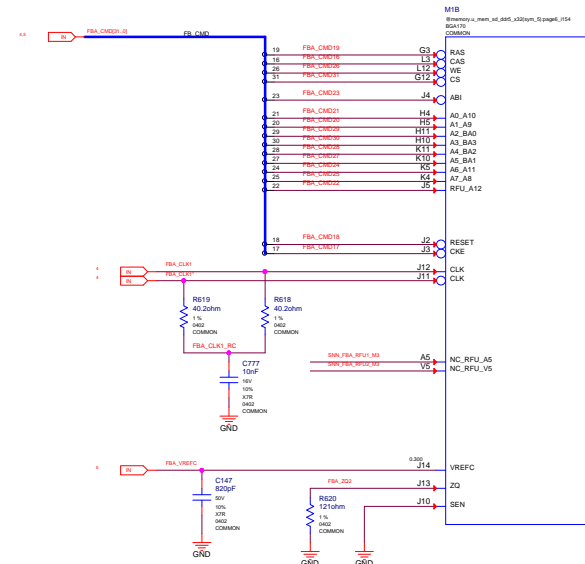


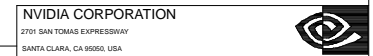
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NV_PN		600-1G410-BASE-100	
PCB REV		PG410-A01	
BOB REV		A	
PAGE		3 OF 37	
DATE		21-MAR-2016	



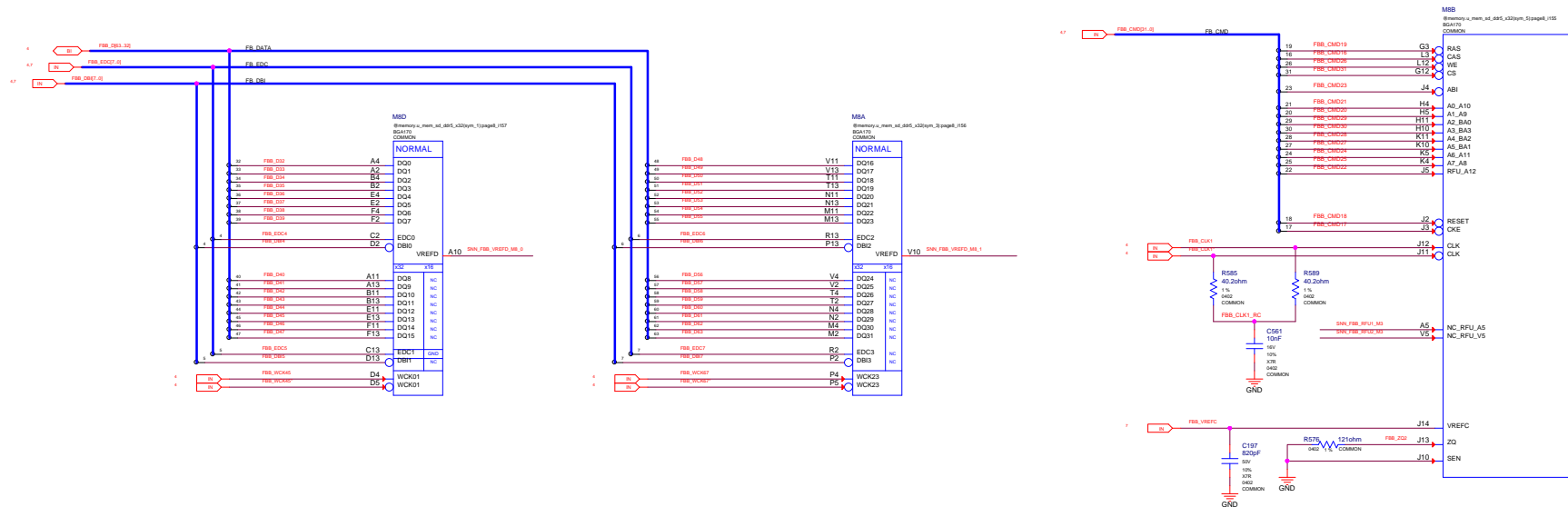








NV_PN	600-1G410-BASE-100		
PCB REV	PG410-A01	PAGE	7 OF 37
BOM REV	A	DATE	21-MAR-2016



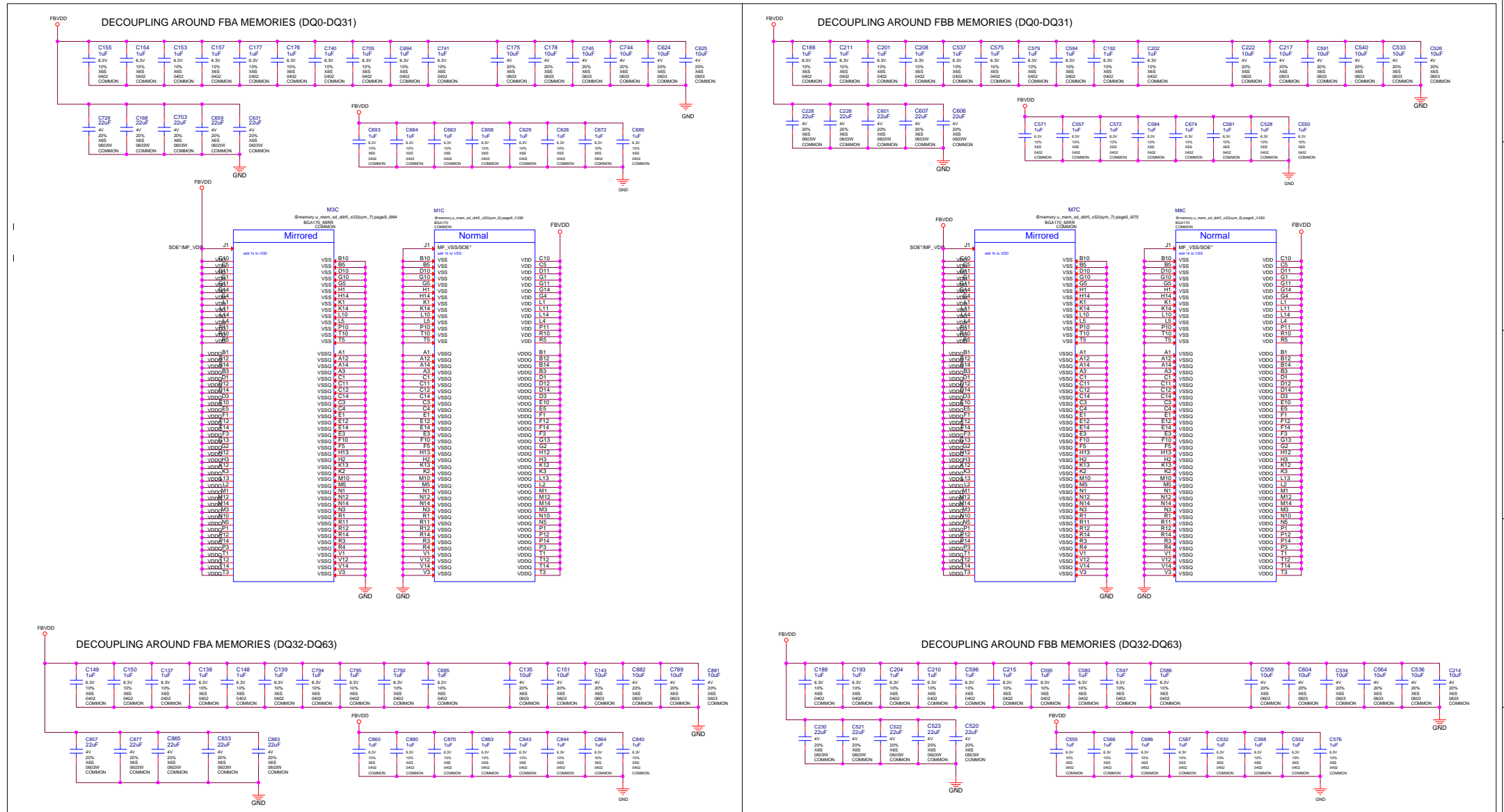
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PCB REV	PG410-A01	PAGE	8 OF 37
BCM REV	A	DATE	21-MAR-2016



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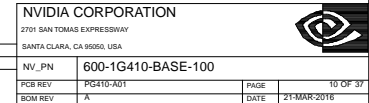
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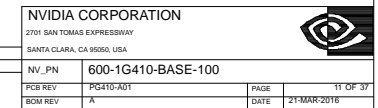
PCB REV PG410-A01

BOM REV A

PAGE 9 OF 37

DATE 21-MAR-2016






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NV_PN		600-1G410-BASE-100	
PCB REV	PG410-A01	PAGE	13 OF 37
BOM REV	A	DATE	21-MAR-2016


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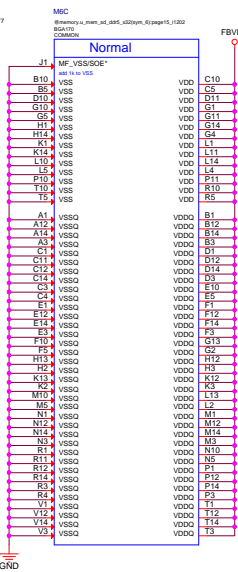
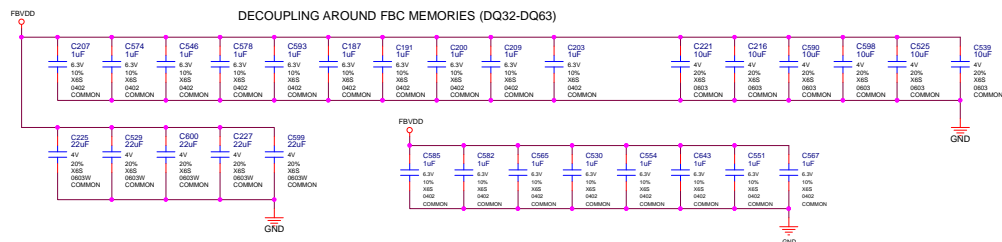
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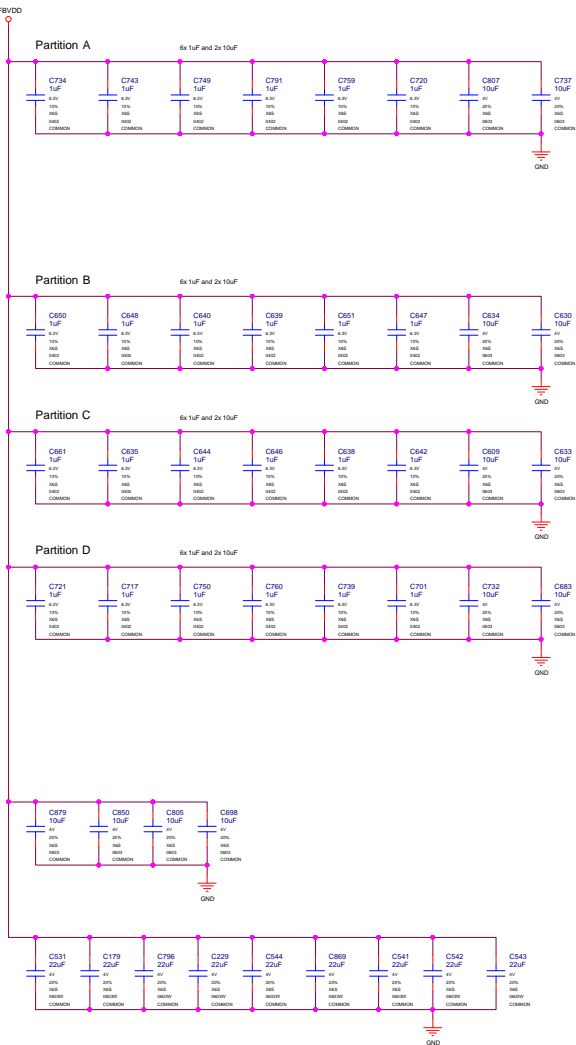


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PCB REV	PG410-A01	PAGE	14 OF 37
BOM REV	A	DATE	21-MAR-2016

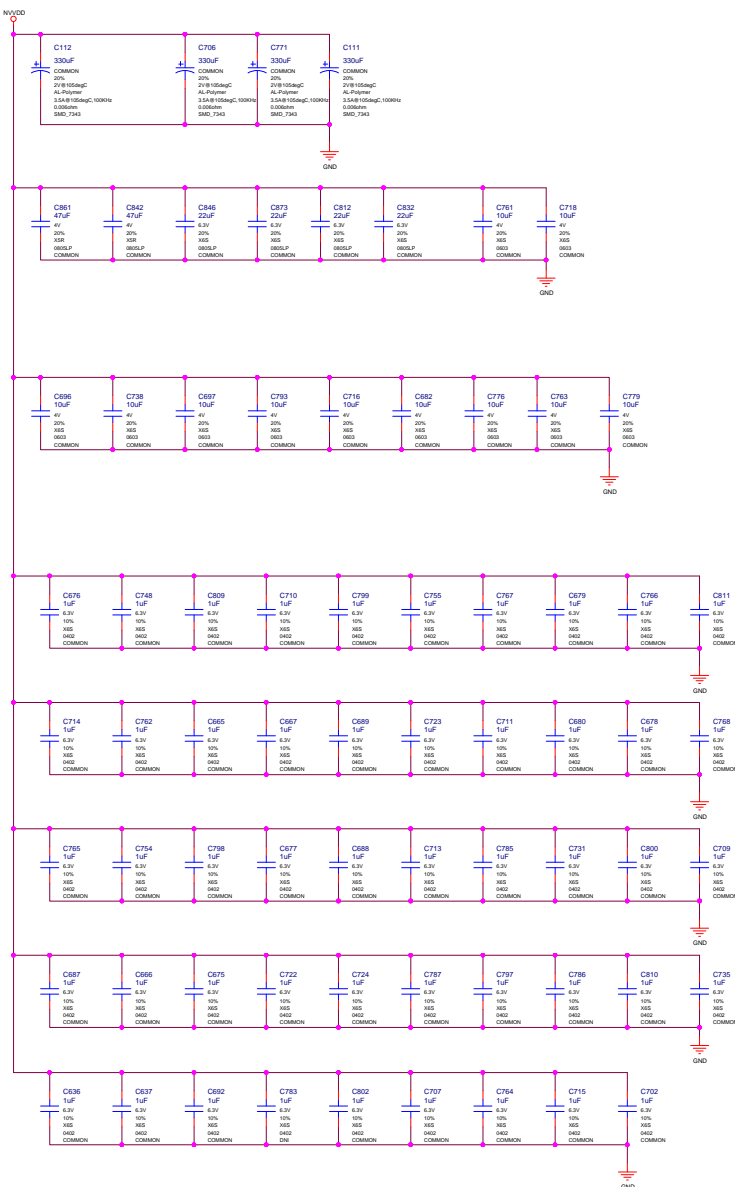


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PCB REV	PG410-A01	PAGE	15 OF 37
BOM REV	A	DATE	21-MAR-2016

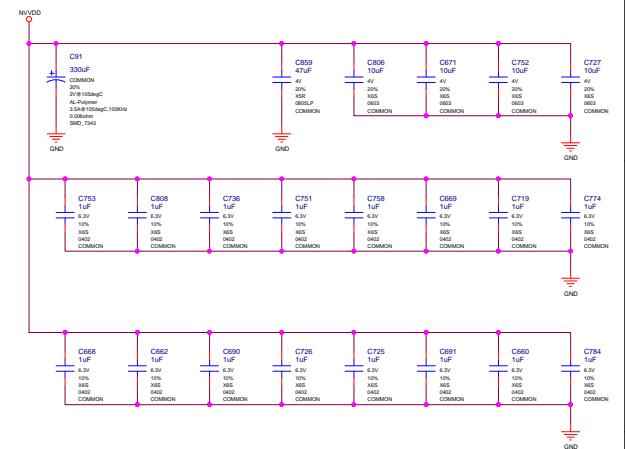
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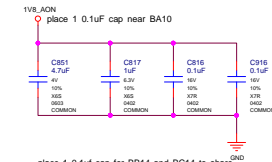
NVVDD



NVVDD

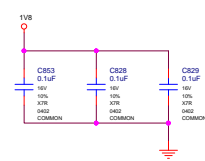


1V8_AON



place 1 0.1uF cap for BB14 and BC14 to share

1V8_MAIN



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	GPU Decoupling

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PCB REV PG410-A01

BCM REV A

PAGE 17 OF 37

DATE 21-MAR-2016



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NV_PN	600-1G410-BASE-100		
PCB REV	PG410-A01	PAGE	18 OF 37
BOM REV	A	DATE	21-MAR-2016


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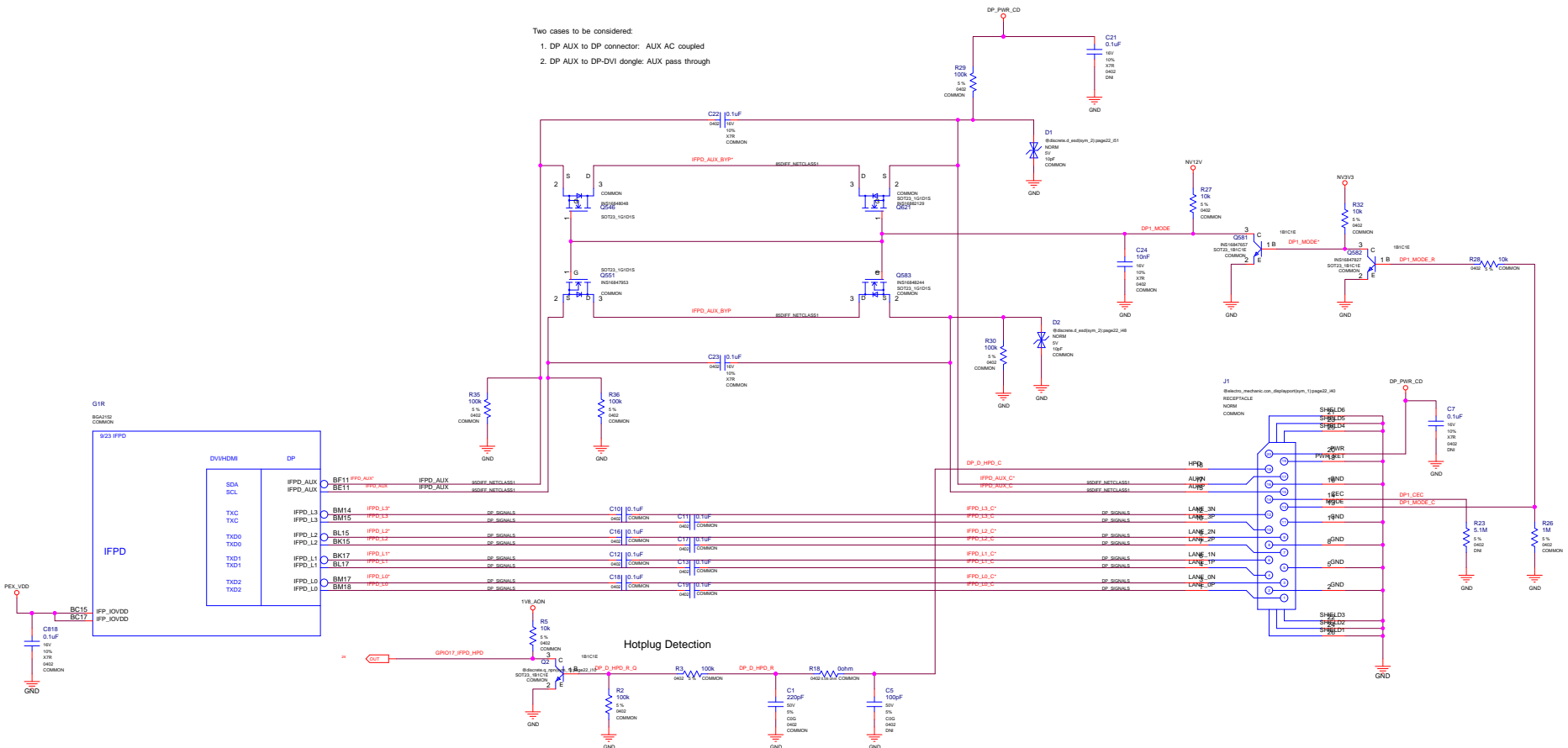
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NV_PN	600-1G410-BASE-100		
PCB REV	PG410-A01	PAGE	20 OF 37
BOM REV	A	DATE	21-MAR-2016



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PG410-A01

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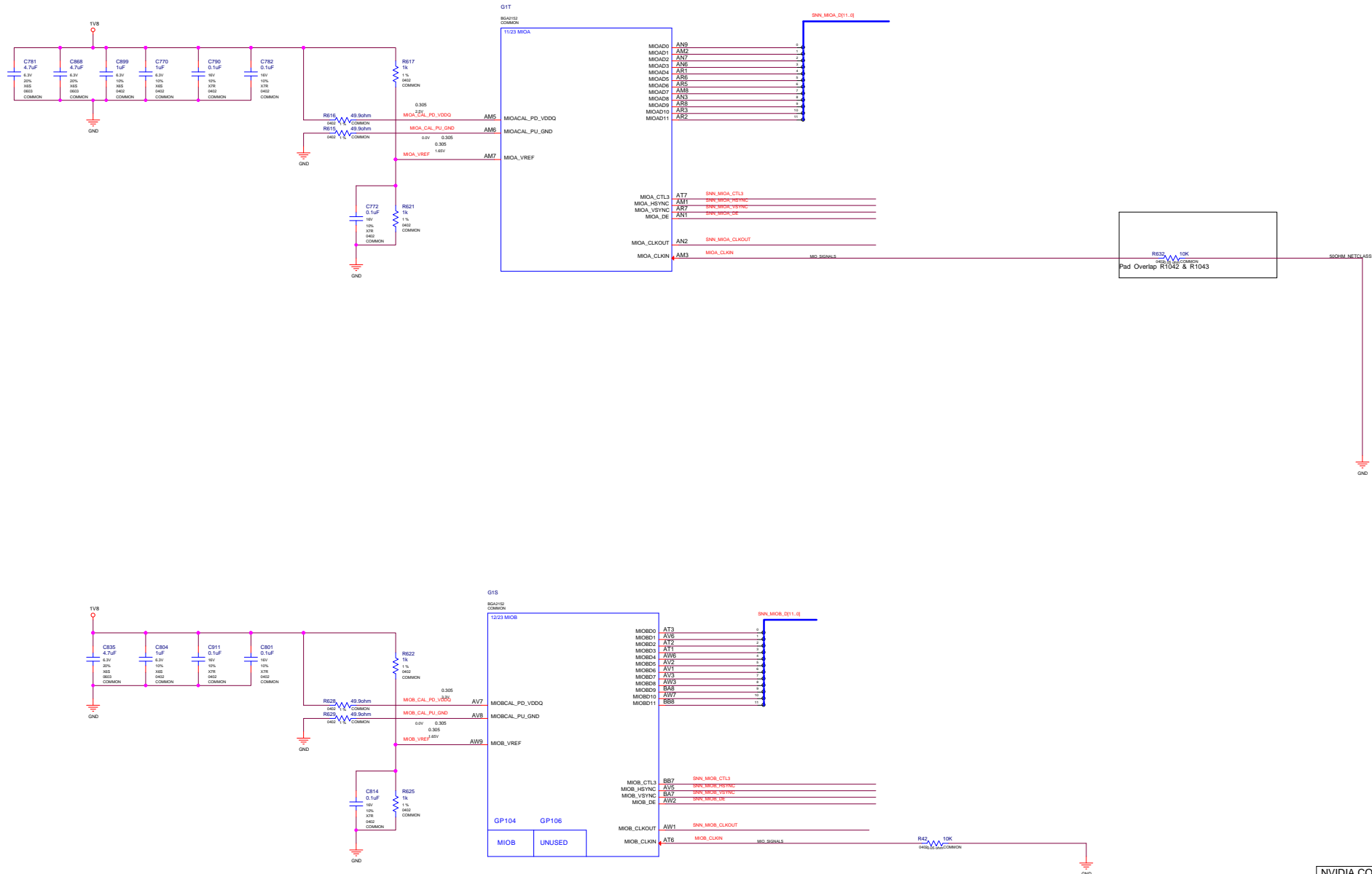
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PAGE

22 OF 37

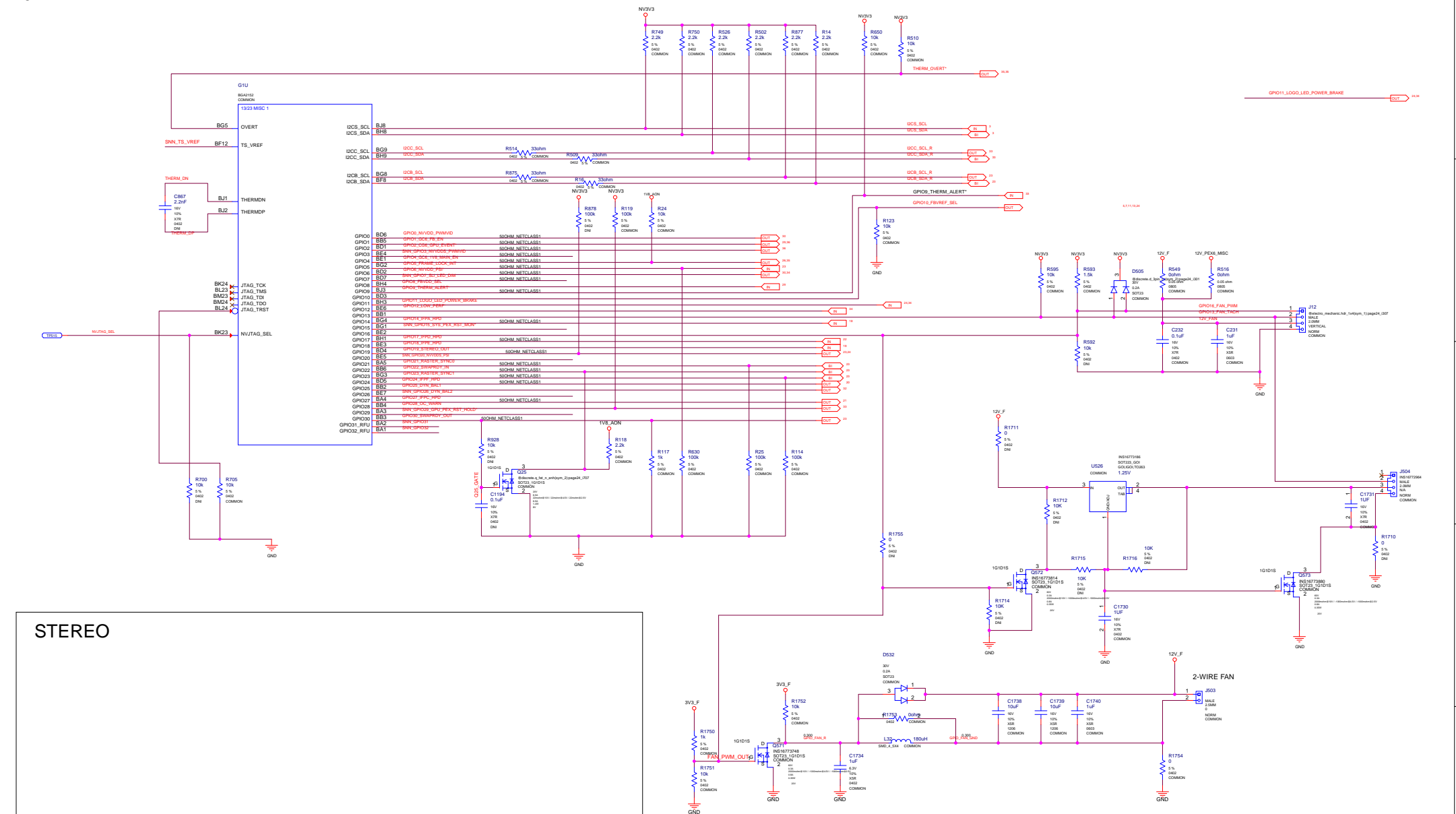
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NV_PN	600-1G410-BASE-100		
PCB REV	PG410-A01	PAGE	23 OF 37
BCM REV	A	DATE	21-MAR-2016



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	0	0	0
L	H	M	1	0	1	1
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

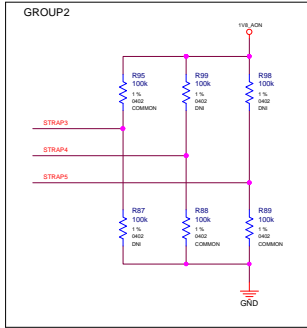
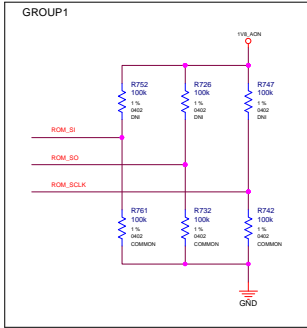
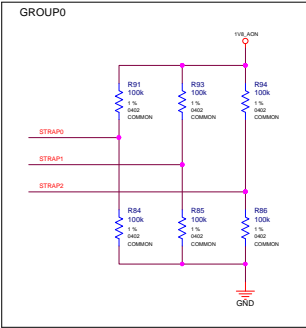
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

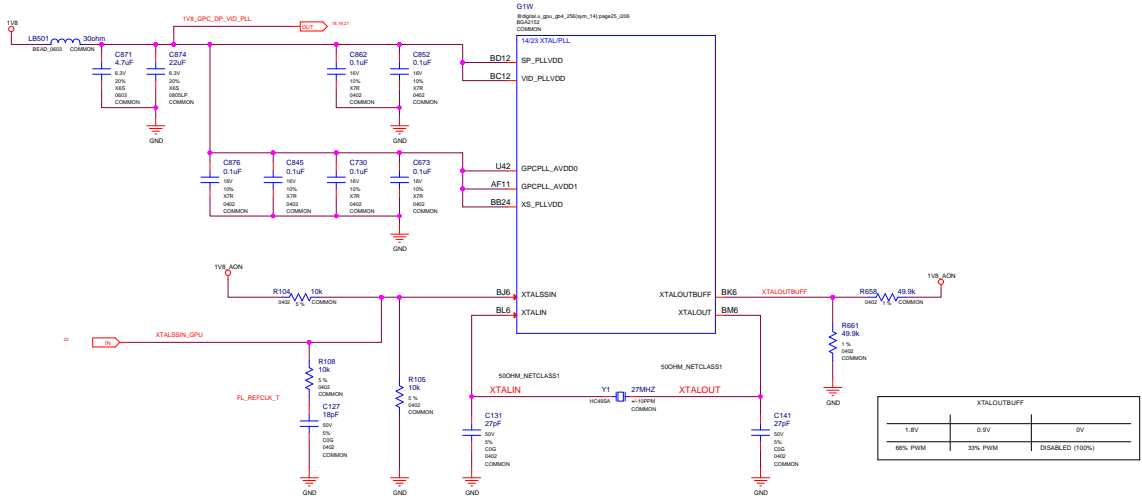
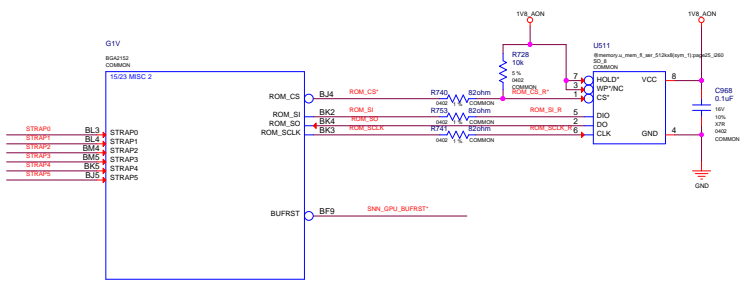
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL,STRAPS



CFG(3:0)	Config	Width	Vendor
0000	256Mx32 256-bit		Samsung
0001	256Mx32 256-bit		Micron
0010	256Mx32 256-bit		Hynix
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		



XTALOUTBUFF		
1.8V	0.9V	0V
80% PWM	33% PWM	DISABLED (100%)

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NV_PN	600-1G410-BASE-100
PCB REV	PG410-A01
BCM REV	A
PAGE	25 OF 37
DATE	21-MAR-2016

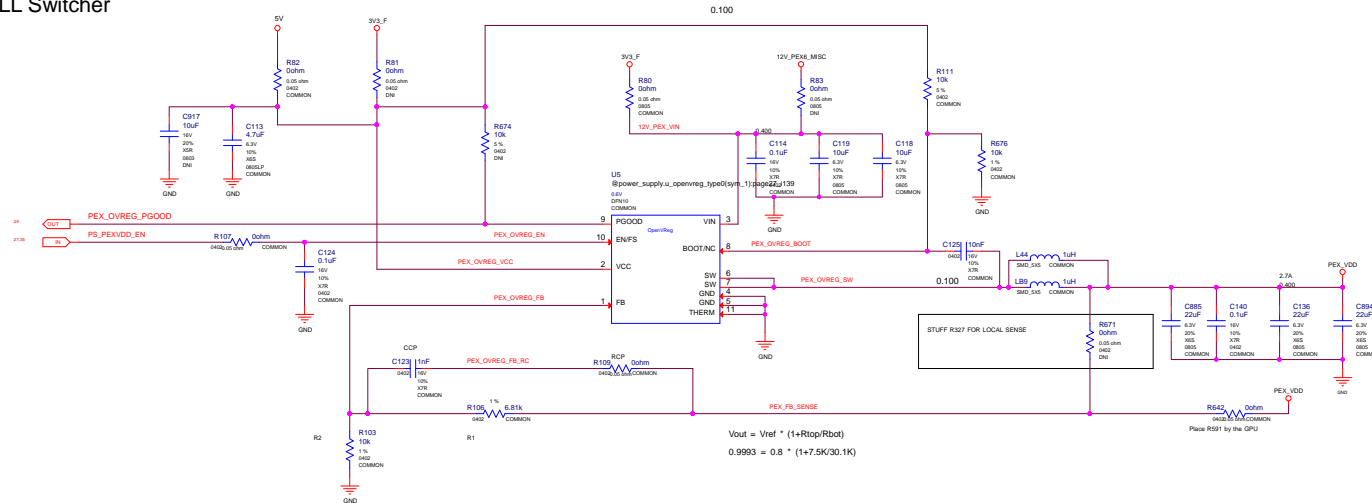
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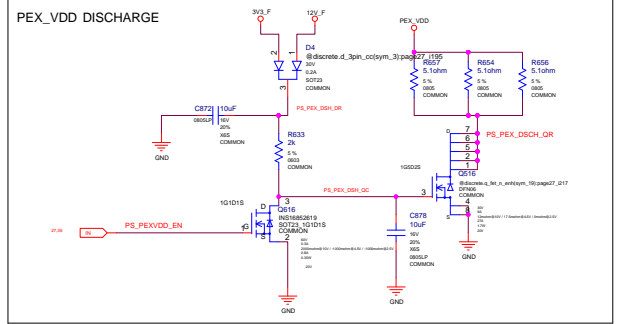
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NV_PN	600-1G410-BASE-100		
PCB REV	PG410-A01	PAGE	26 OF 37
BOM REV	A	DATE	21-MAR-2016

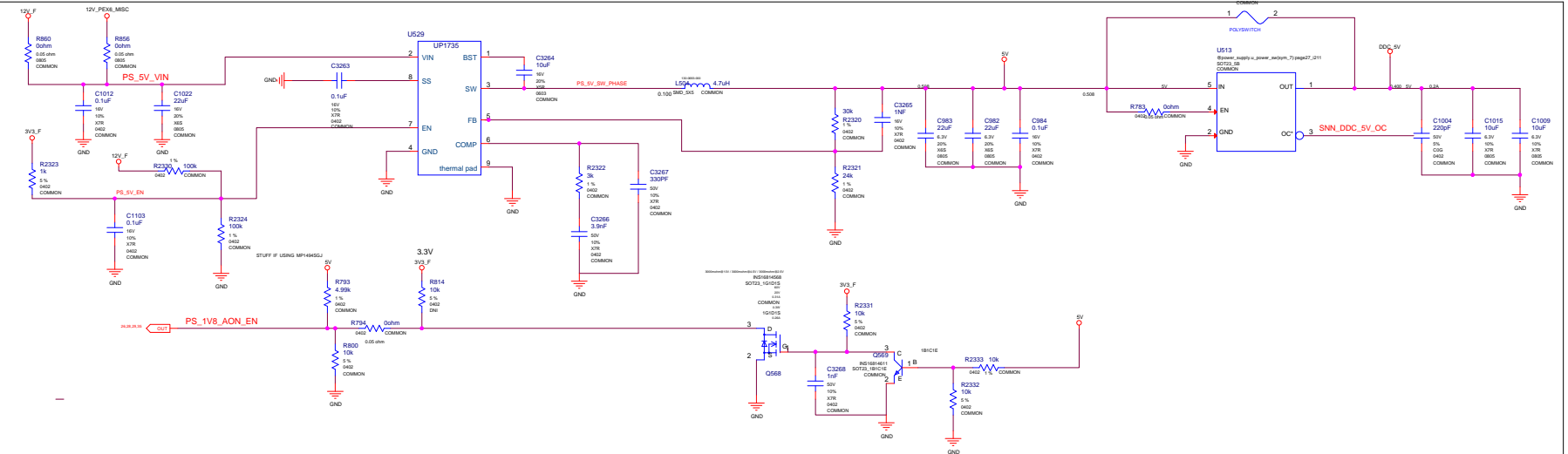
PEX PLL Switcher



PEX_VDD DISCHARGE



5V Switcher



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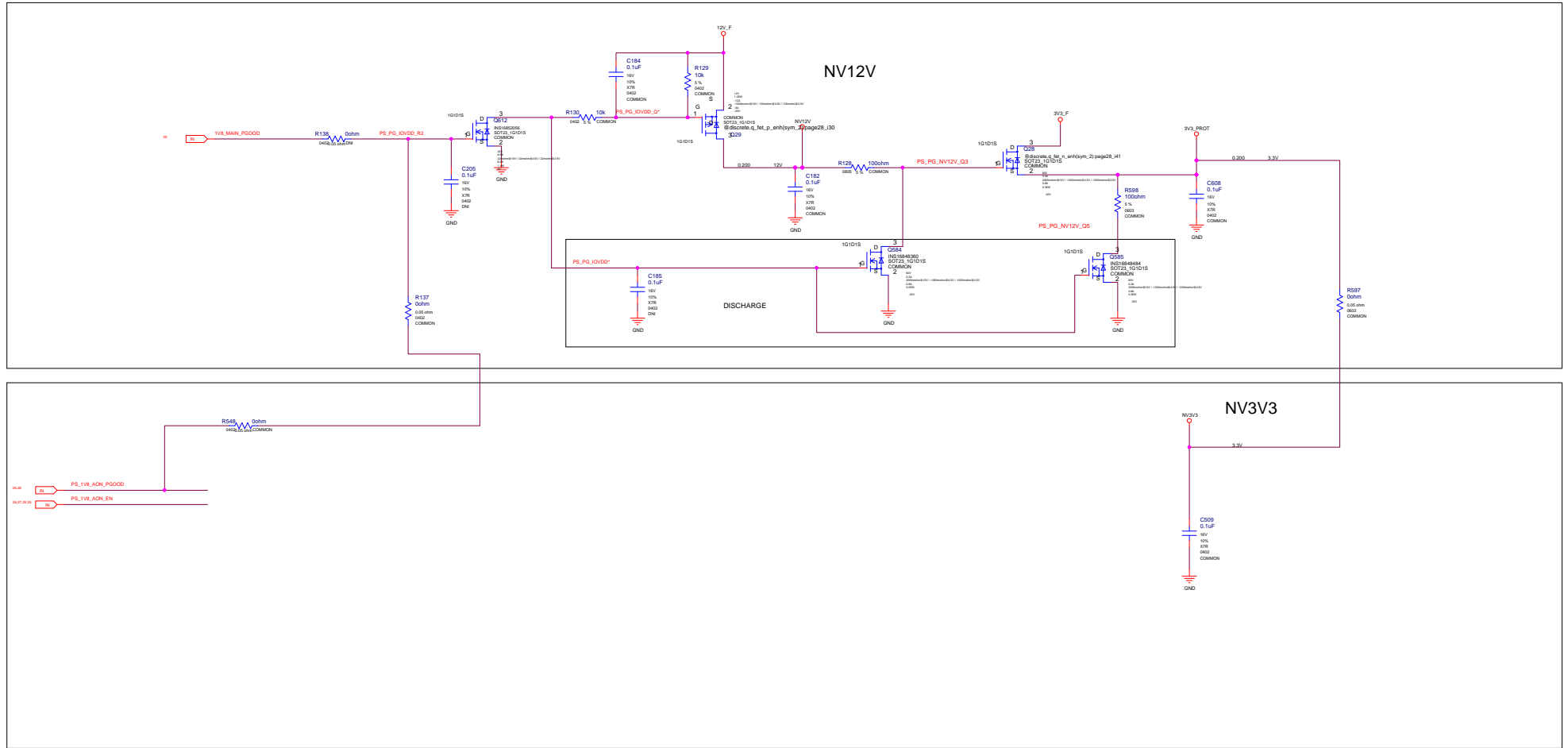


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PCB REV	PG410-A01	PAGE	27 OF 37
BCM REV	A	DATE	21-MAR-2016


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ASSEMBLY	ASSEMBLY DESCRIPTION
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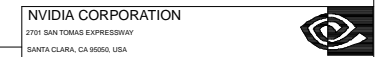


ASSEMBLY	«ASSEMBLY_DESCRIPTION
PAGE DETAIL	PS: NV3V3, NV12V

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NV_PN		600-1G410-BASE-100		
PCB REV	PG410-A01	PAGE	28 OF 37	
BOM REV	A	DATE	21-MAR-2016	





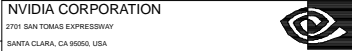
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PAGE DETAIL		PS: INVDD Phase 1.2 & 3		600-1G410-BASE-100	
MAY		DISCLAIMS ALL		PCB REV PG410-001	
Y STANDARDS.				PAGE 31 OF 37	
		BOM REV A		DATE 21-MAR-2016	

Page32: PS: NVVDD RAIL BALANCE LOGIC & DYNAMIC RAIL

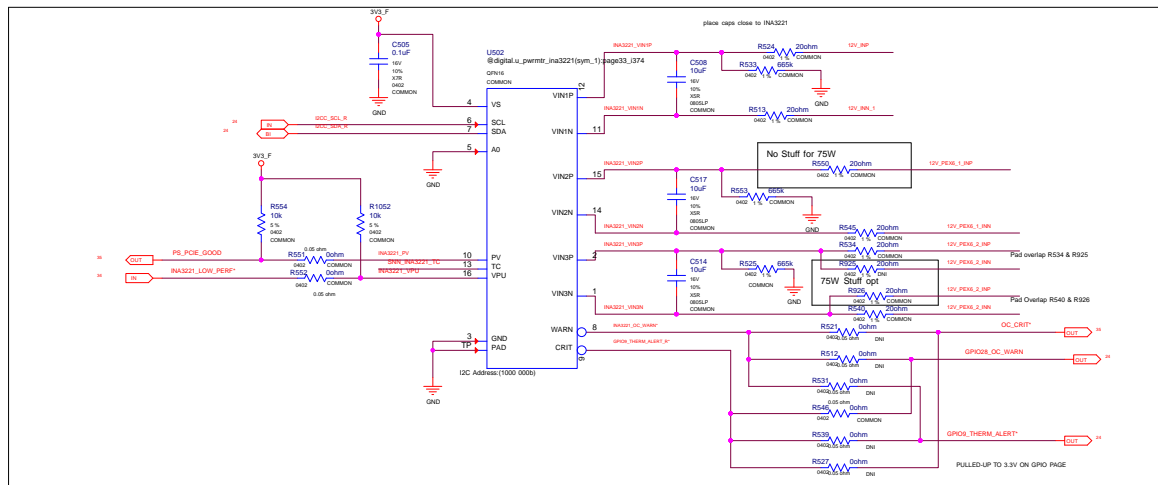


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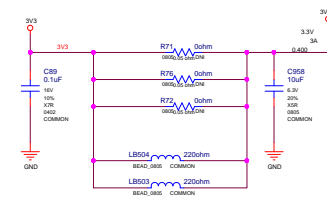
ASSEMBLY	<ASSEMBLY DESCRIPTION>		
PAGE DETAIL	PS NVVDD Rail Balance Logic & Dynamic Phase		
NV_PN	600-1G410-BASE-100		
PCB REV	PG410-A01	PAGE	32 OF 37
BOM REV	A	DATE	21-MAR-2016



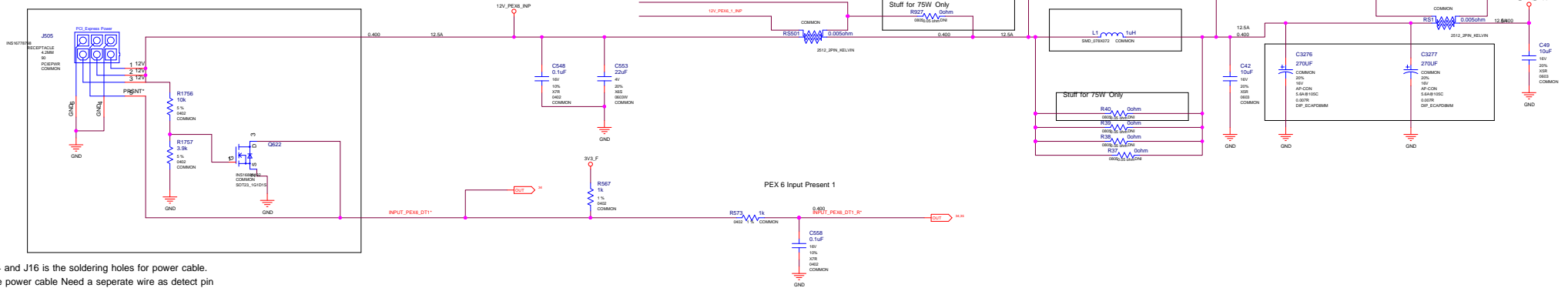
Page33: PS: Inputs, Filtering, and Monitoring



PEX 3V3 INPUT - 10W

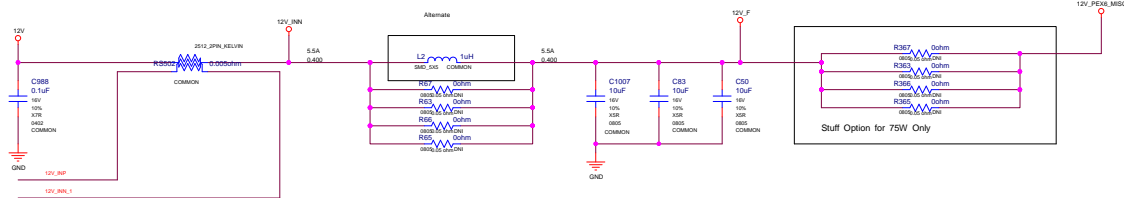



PEX6 INPUT 1 - 2x3 PCIE CON 75W



J14 and J16 is the soldering holes for power cable.
The power cable Need a seperate wire as detect pin
This detect wire need be soldered on J15

PEX_12V INPUT - 66W

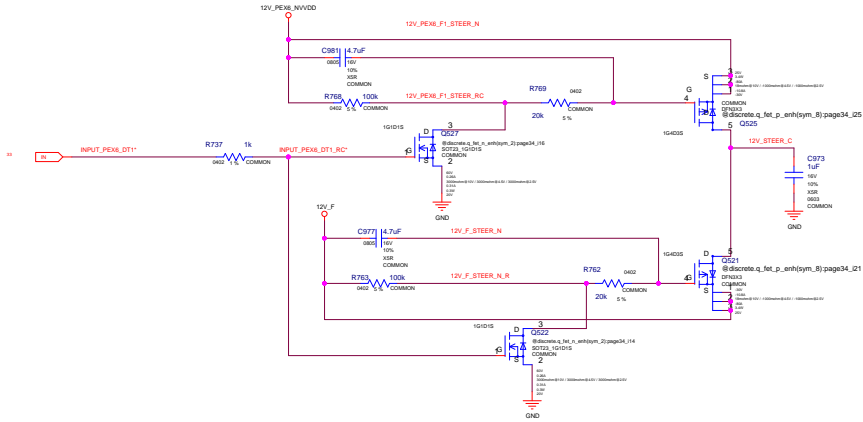


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PCB REV	PG40-A01	PAGE	33 OF 37	
BOM REV	A	DATE	21-MAR-2016	

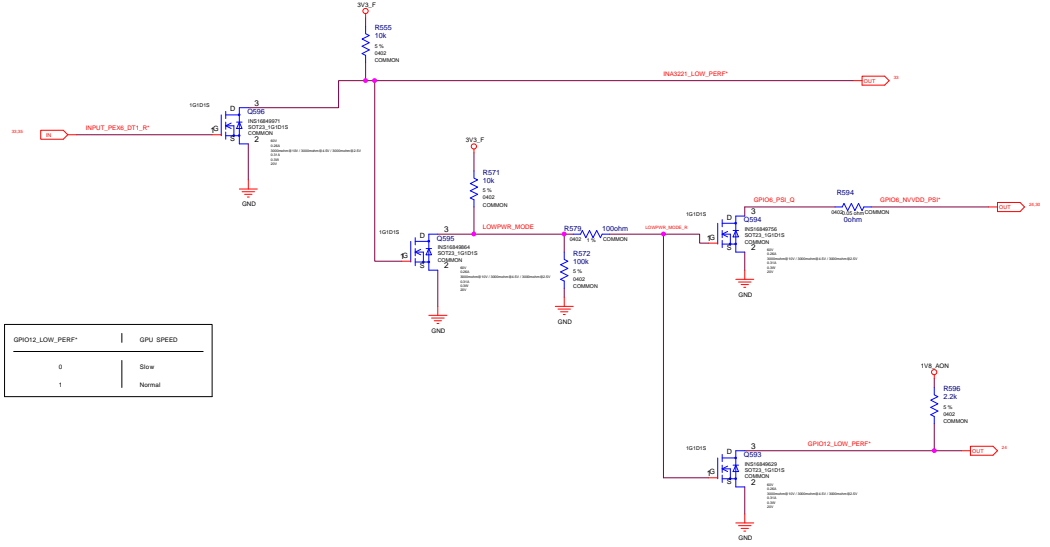
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12V CURRENT STEERING (UNDER POWER BOOT):

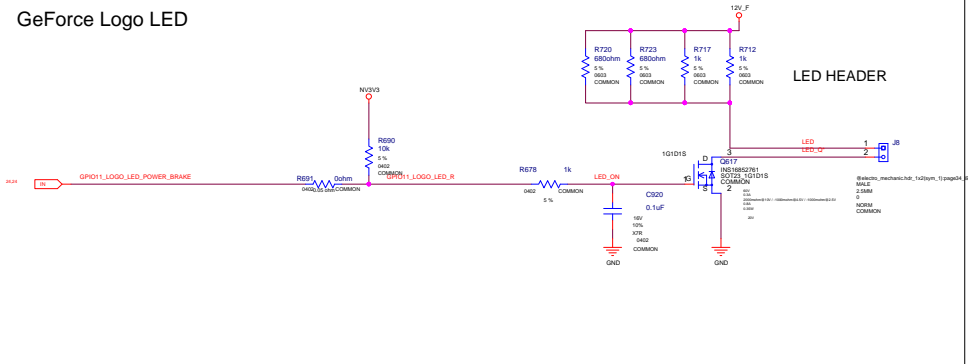
GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

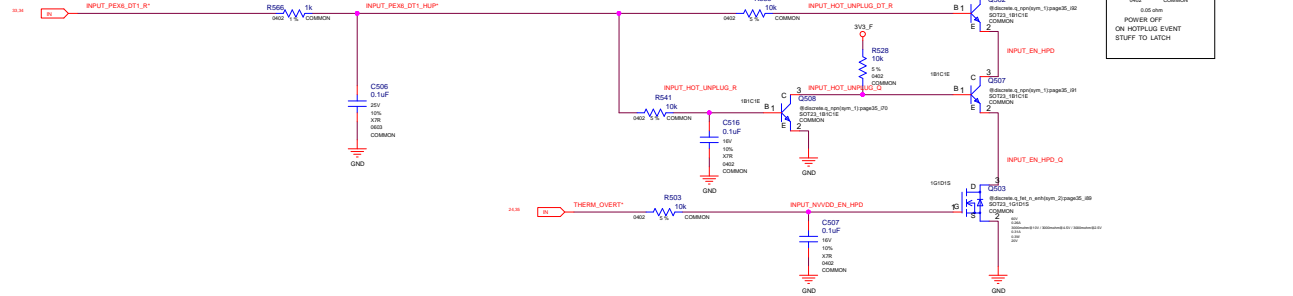


PEX Input - Power Level/PSI* Control

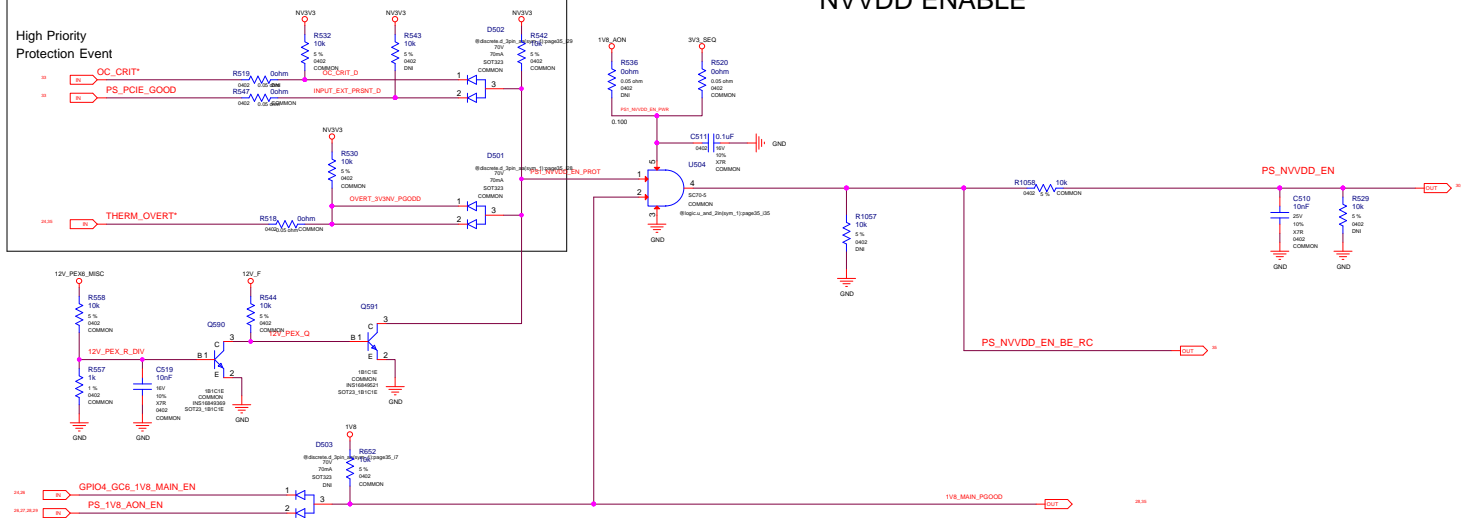


GeForce Logo LED





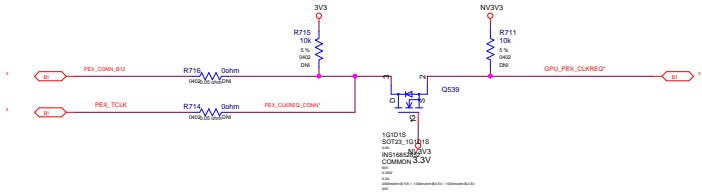
High Priority
Protection Event



PCB REV	PG410-A01	PAGE	35 OF 37
BOM REV	A	DATE	21-MAR-2016

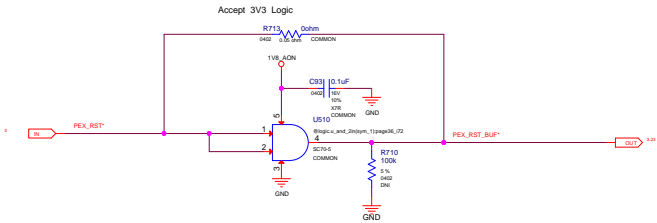
[illegible]

PEX_CLKREQ*



GPU_EVENT*

PEX_RST# LOGIC



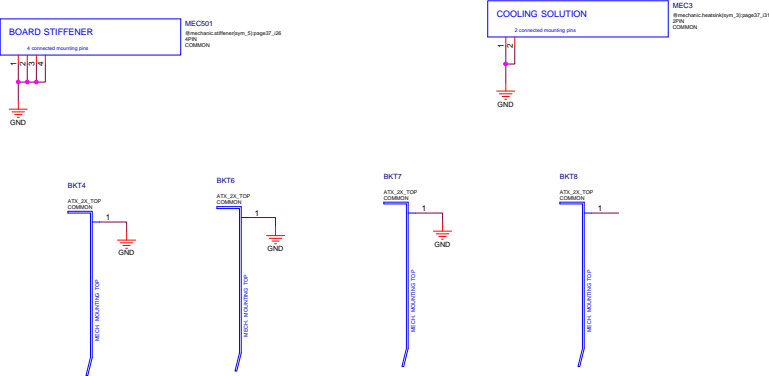
GC6 FB ENABLE

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PCB REV	PG410-A01	PAGE	38 OF 37
BCM REV	A	DATE	21-MAR-2016

Brackets: MOUNTING HOLES FOR HS DS: MOUNTING HOLES FOR HS SS:

GPU Stiffener:



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PCB REV	PG410-A01	PAGE	37 OF 37
BCM REV	A	DATE	21-MAR-2016