

PG186-A00

256b GDDR6 x16

DP + DP + DP + HDMI/DP

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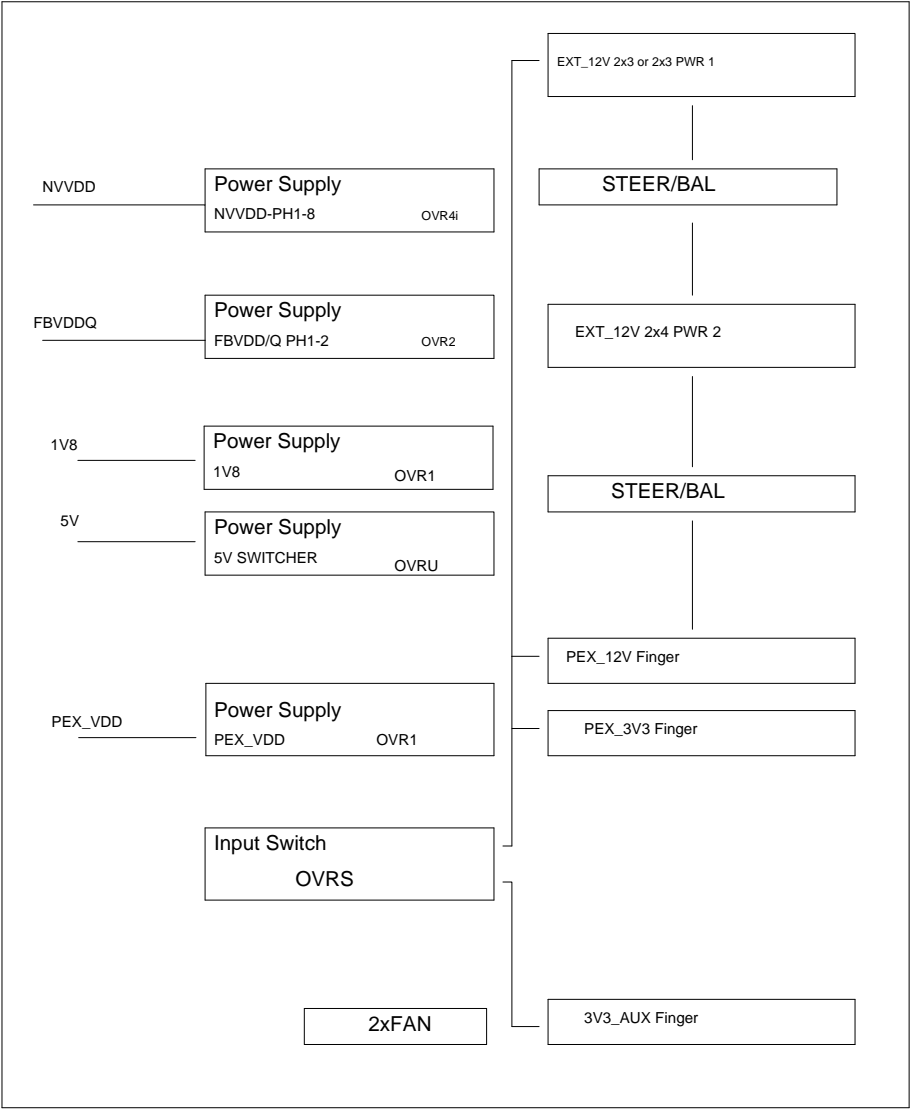
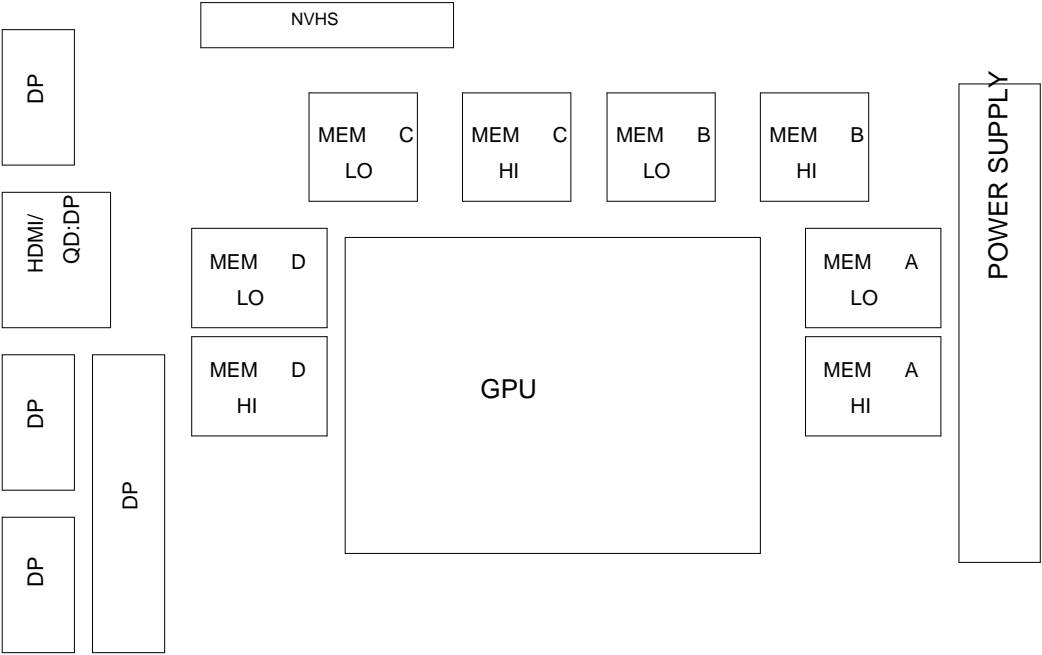
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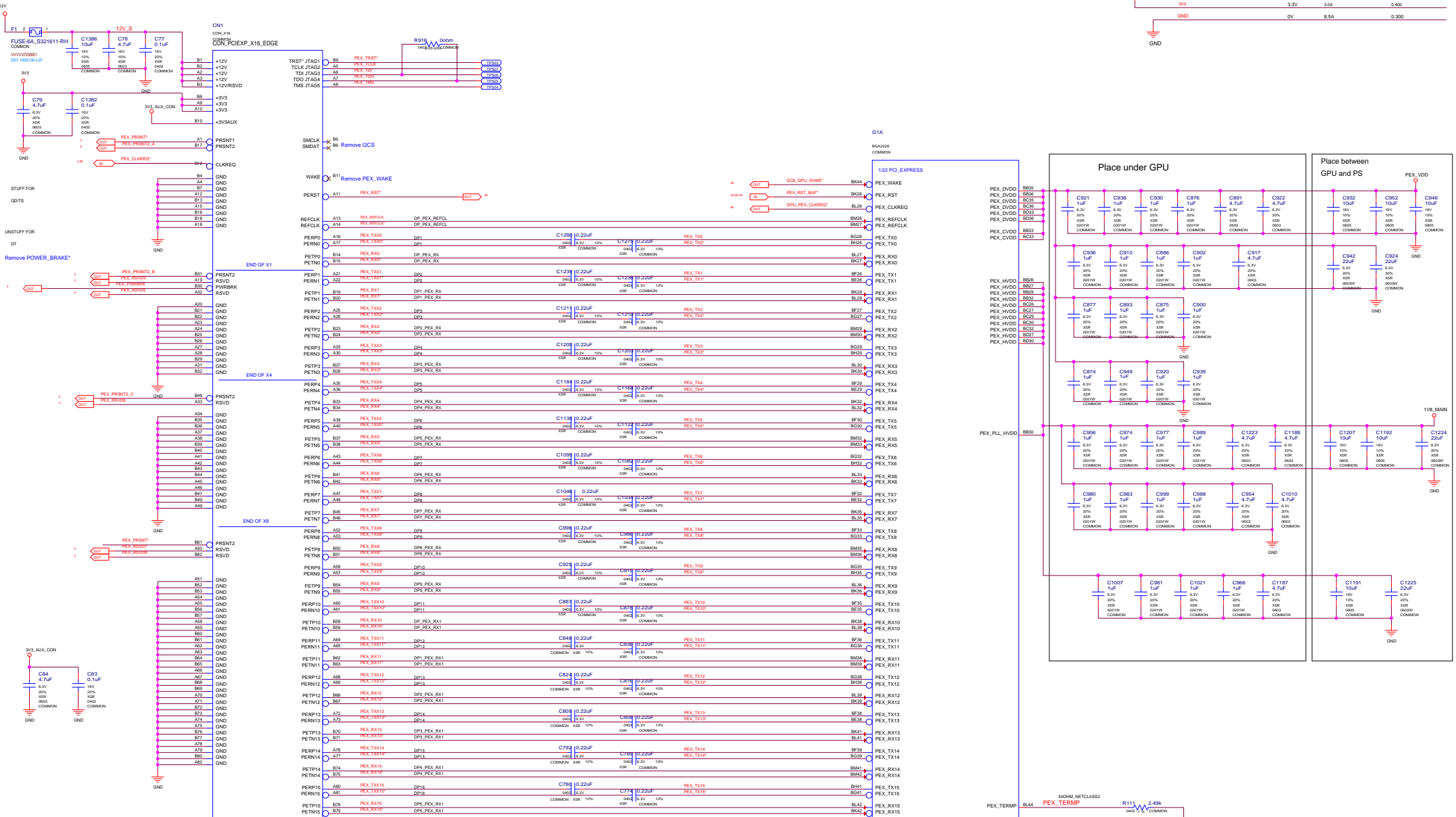
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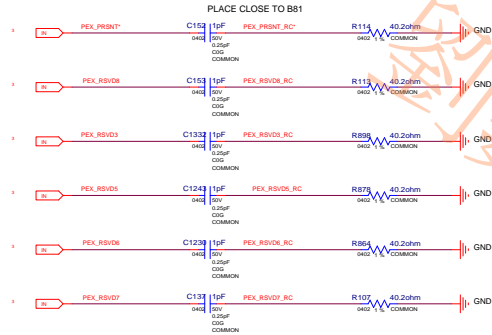
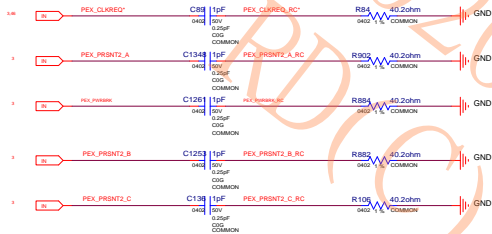
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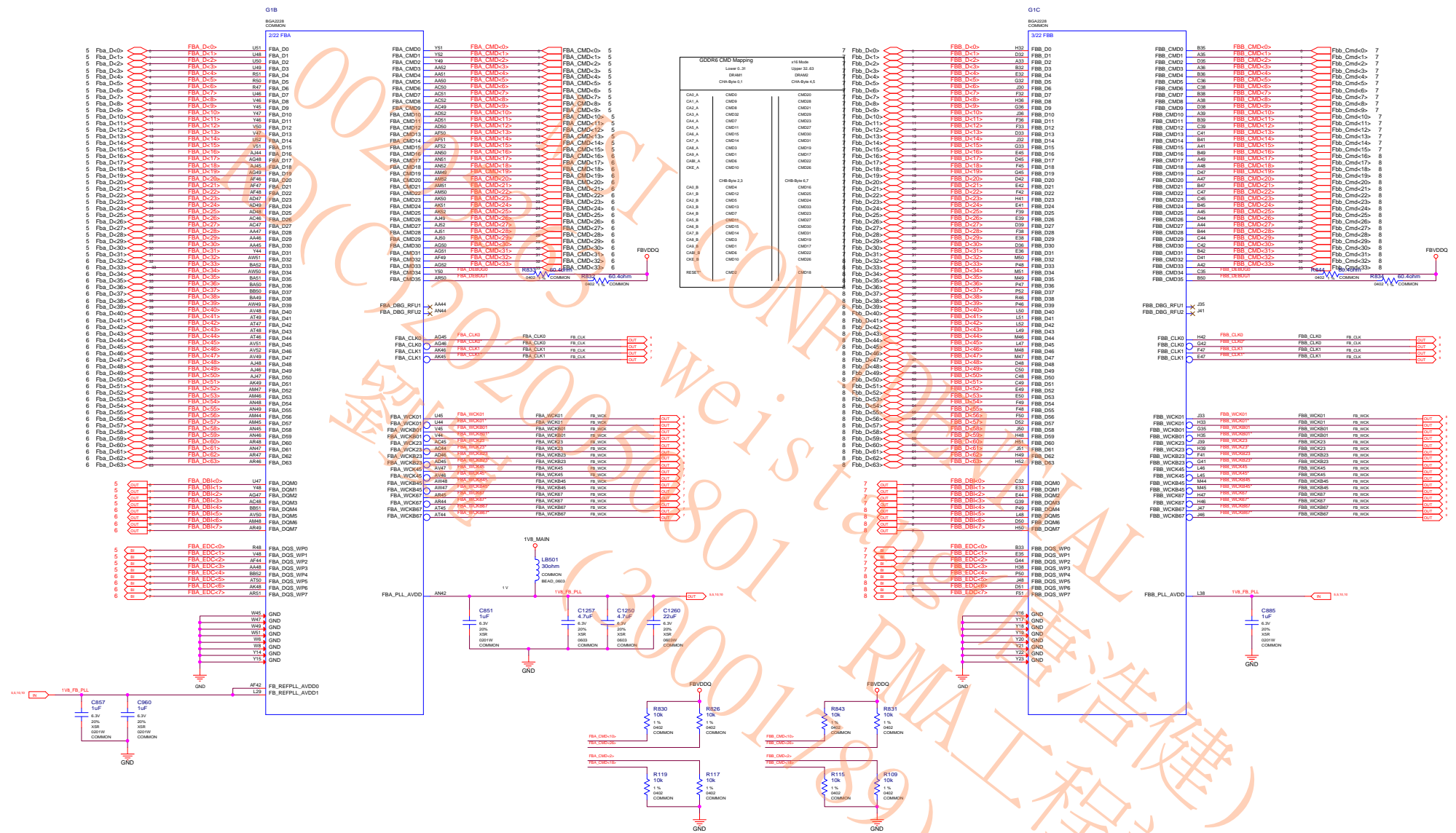
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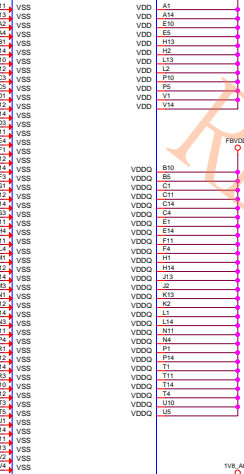
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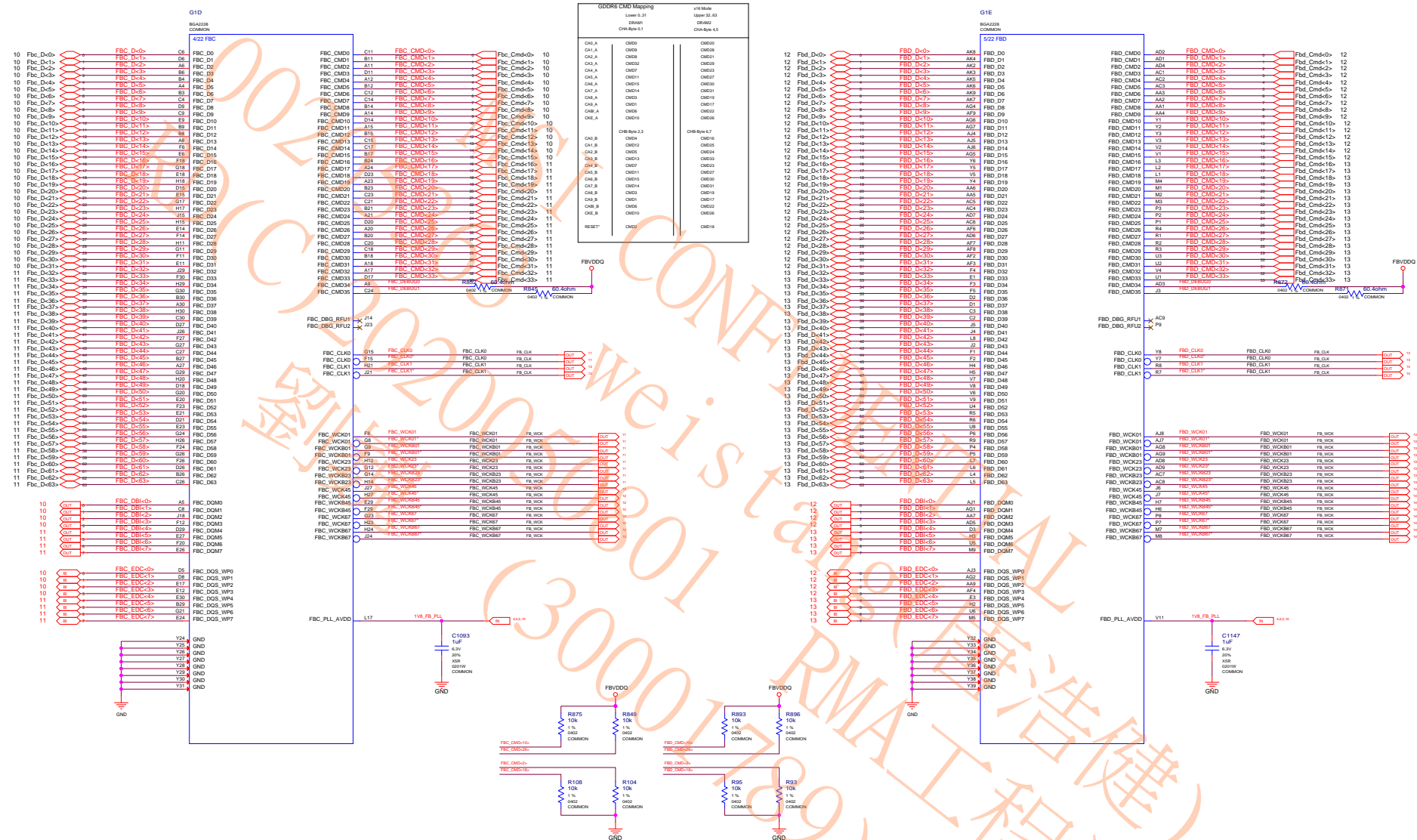


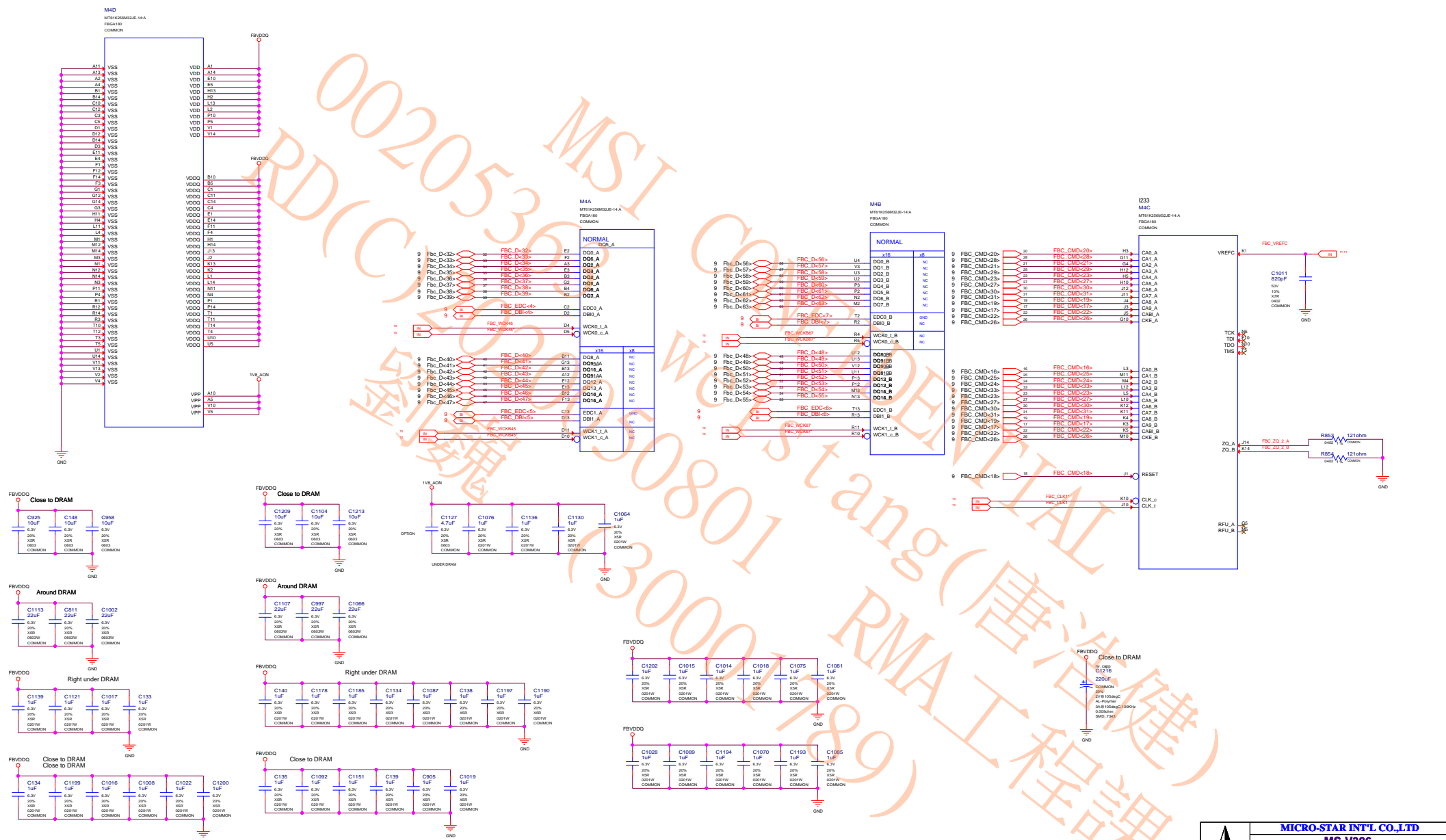


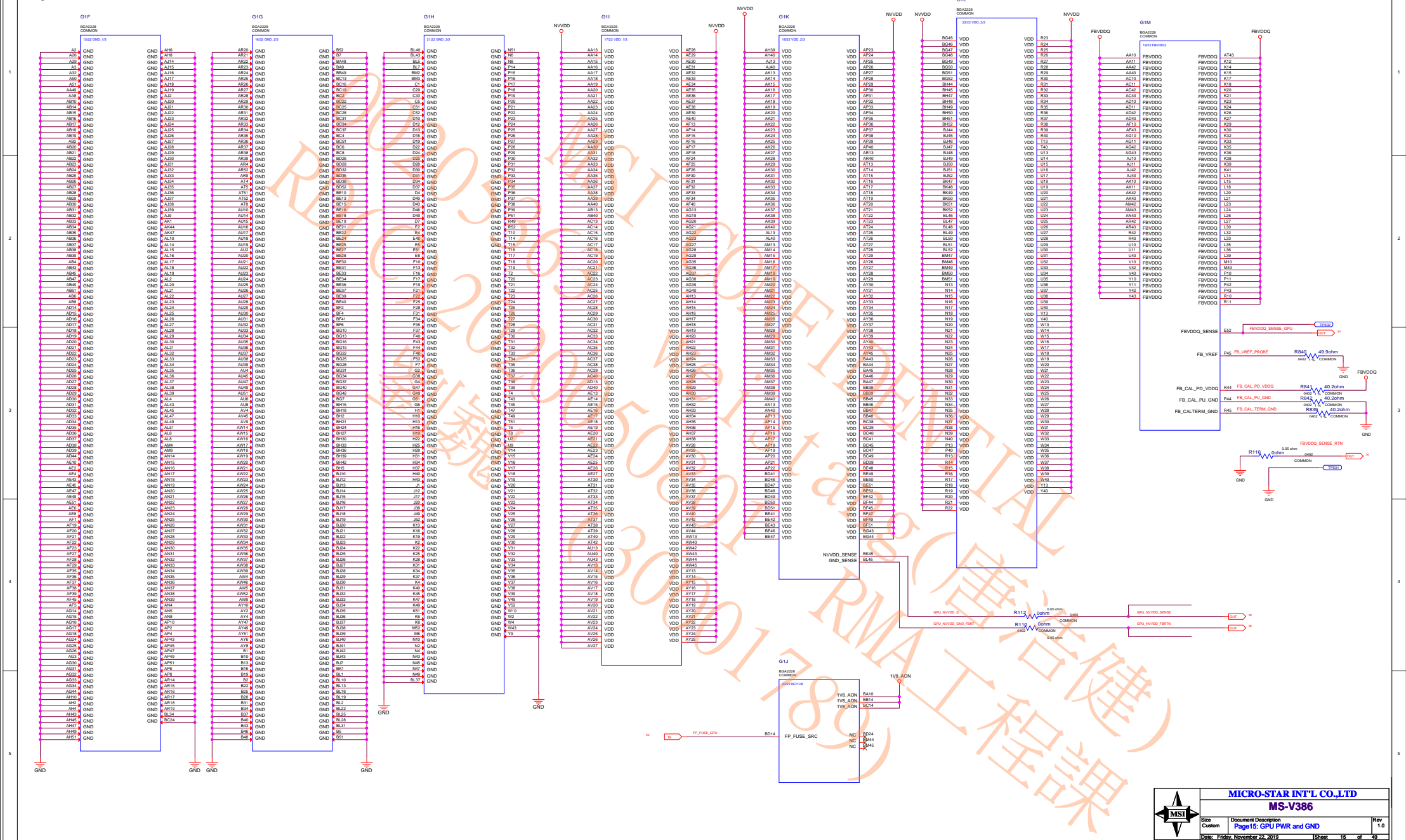


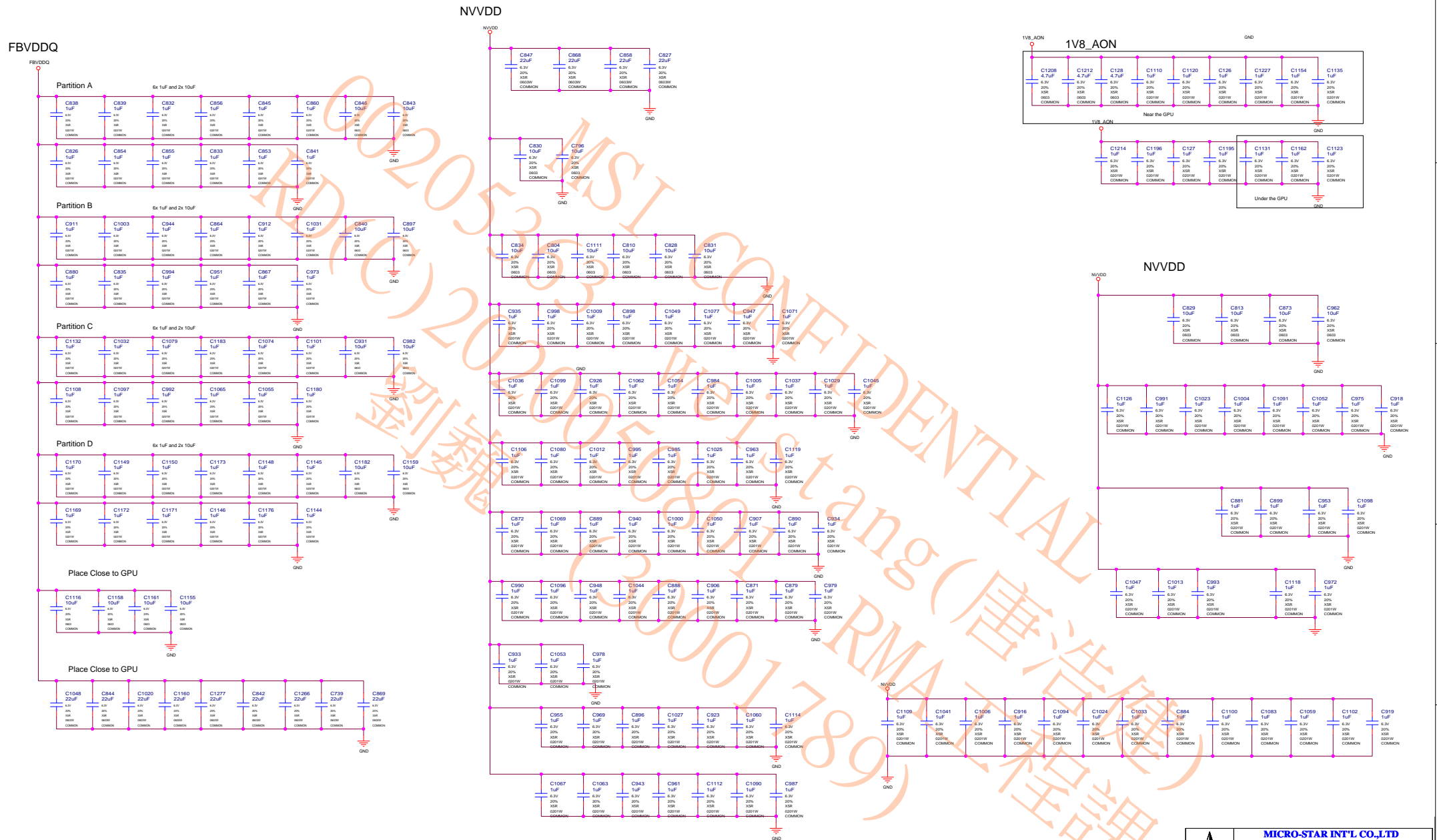


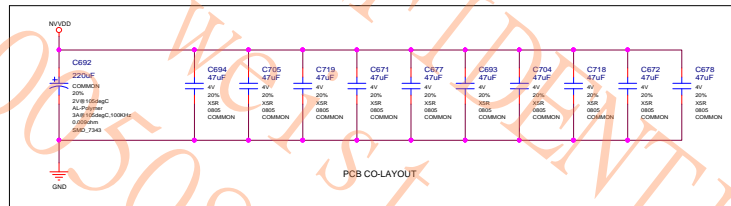
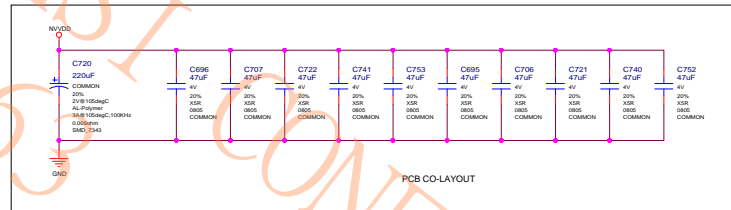
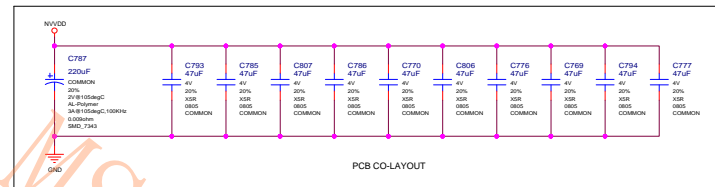
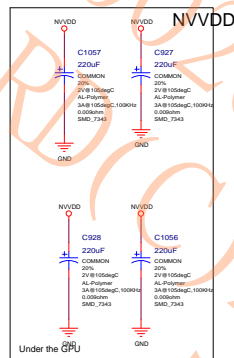
MTD
MT6128000000-14-A
FPGA100
COMMON

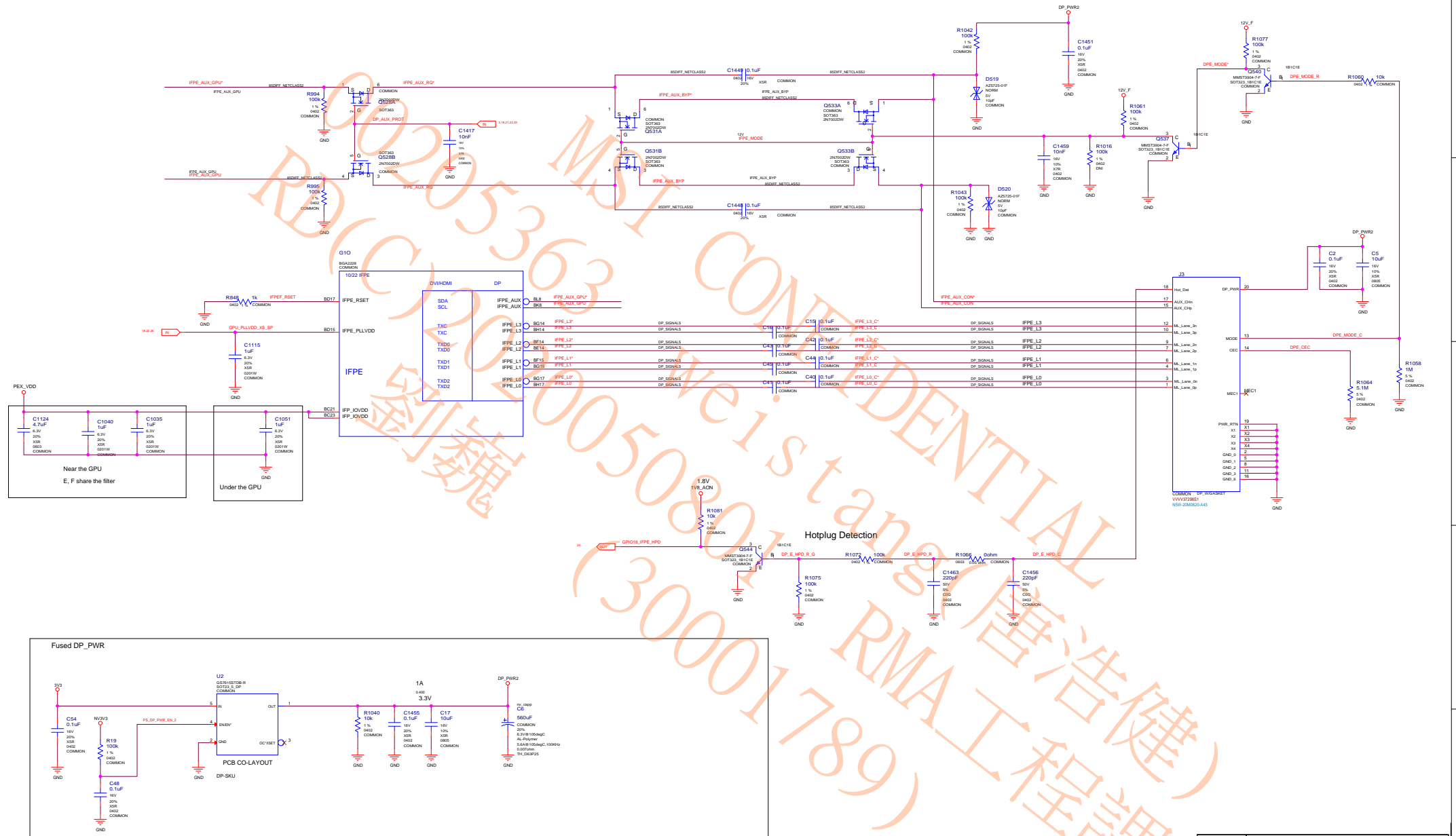


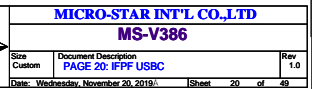
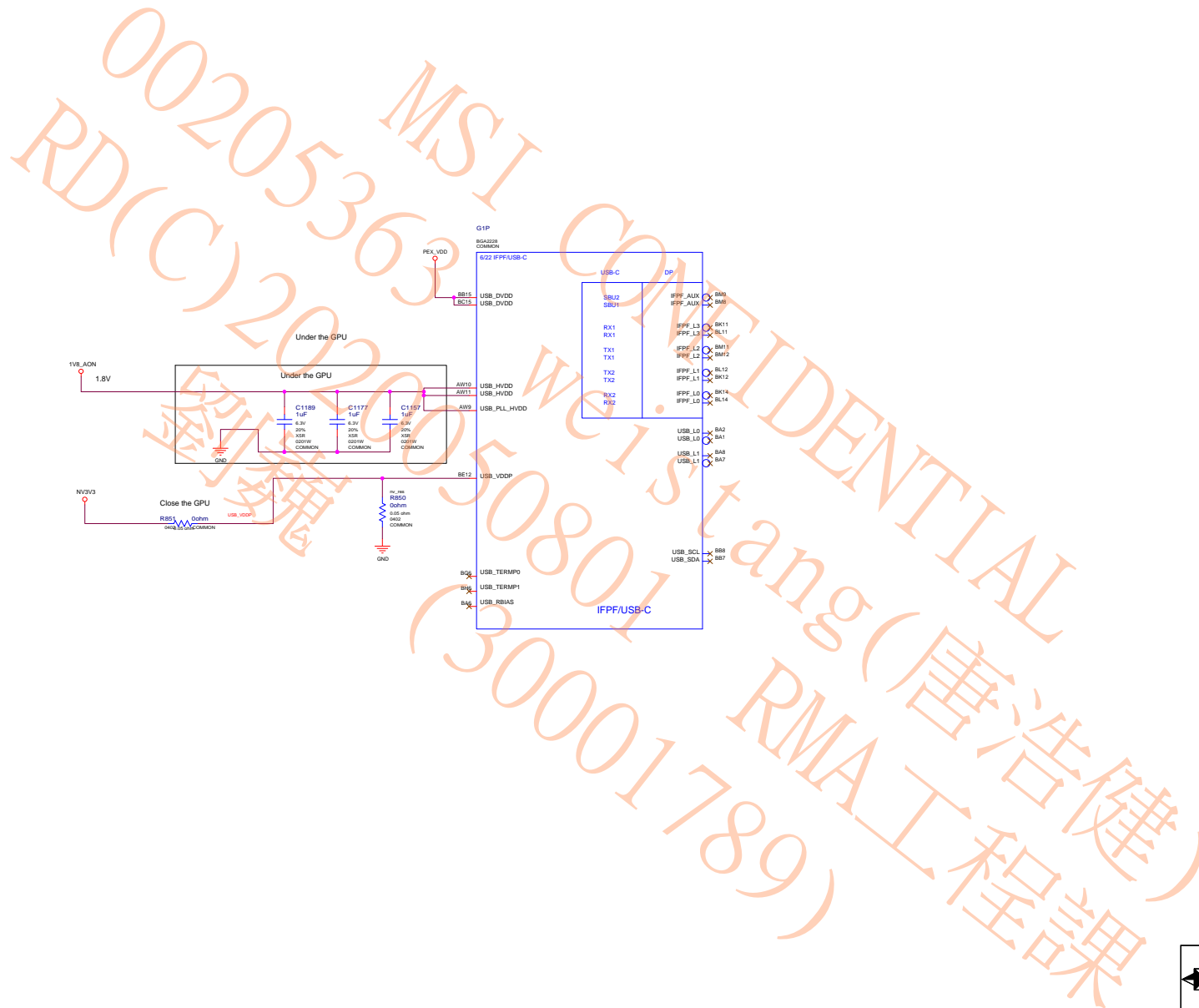


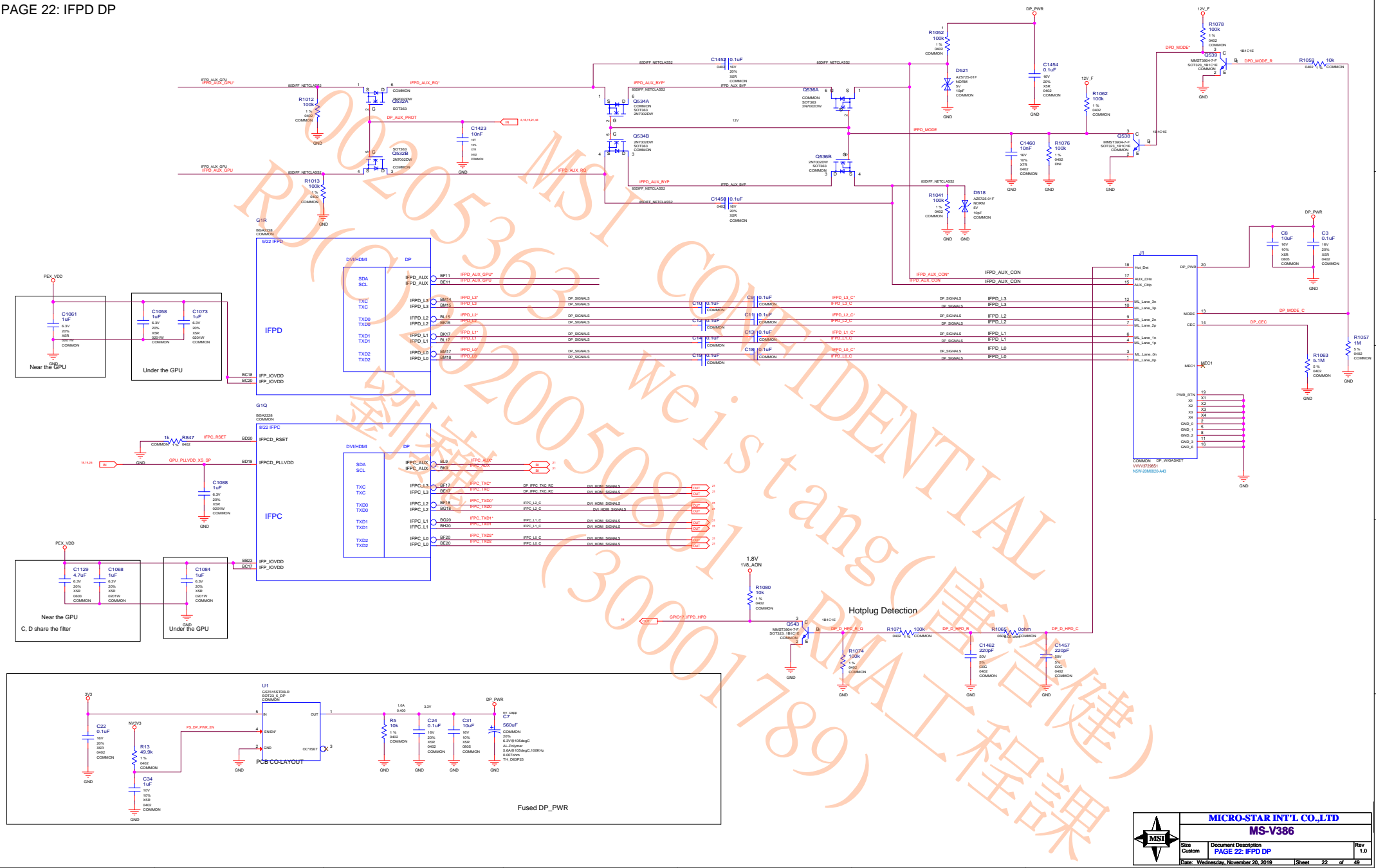




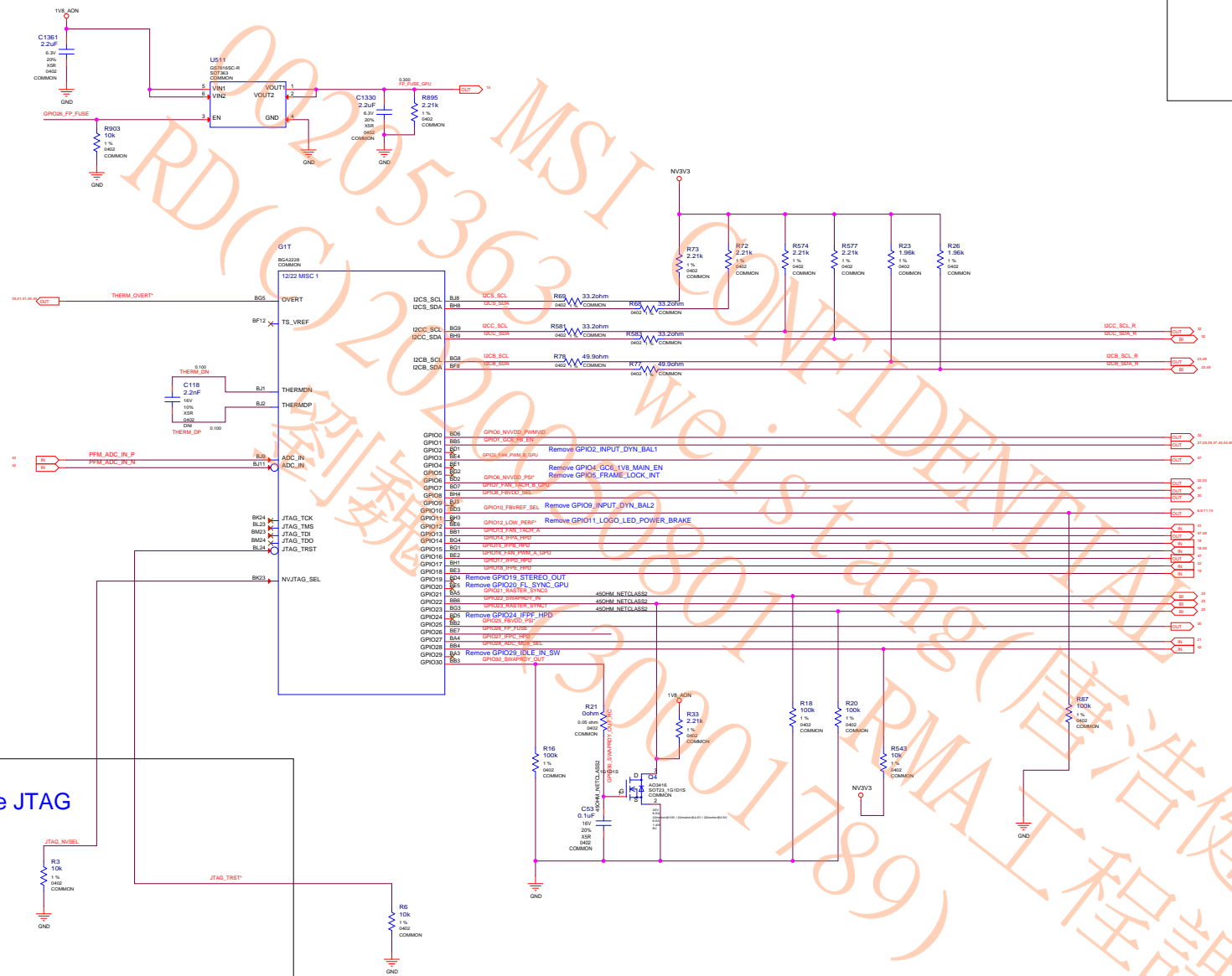








Remove POWER_BRAKE*



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

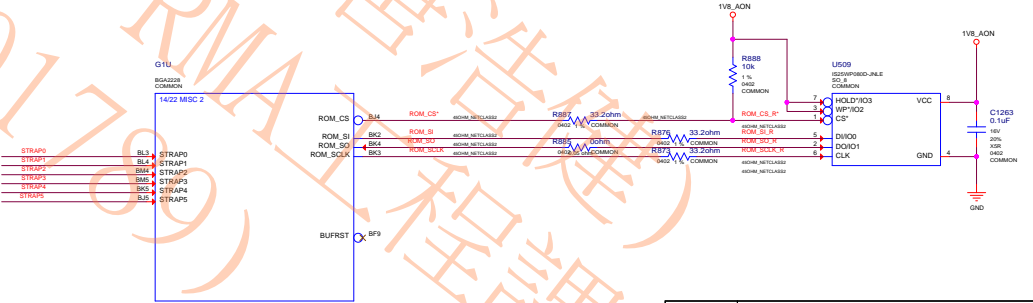
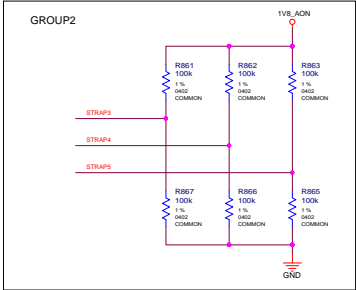
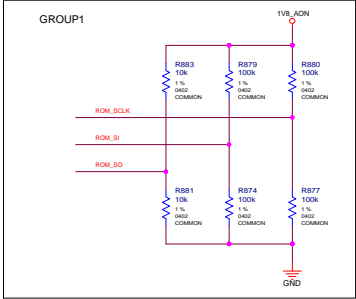
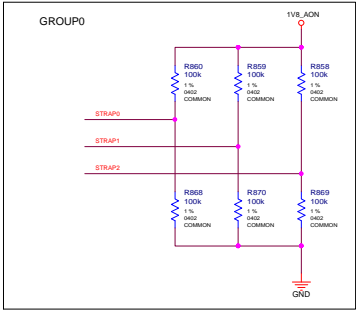
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

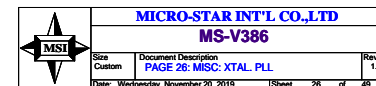
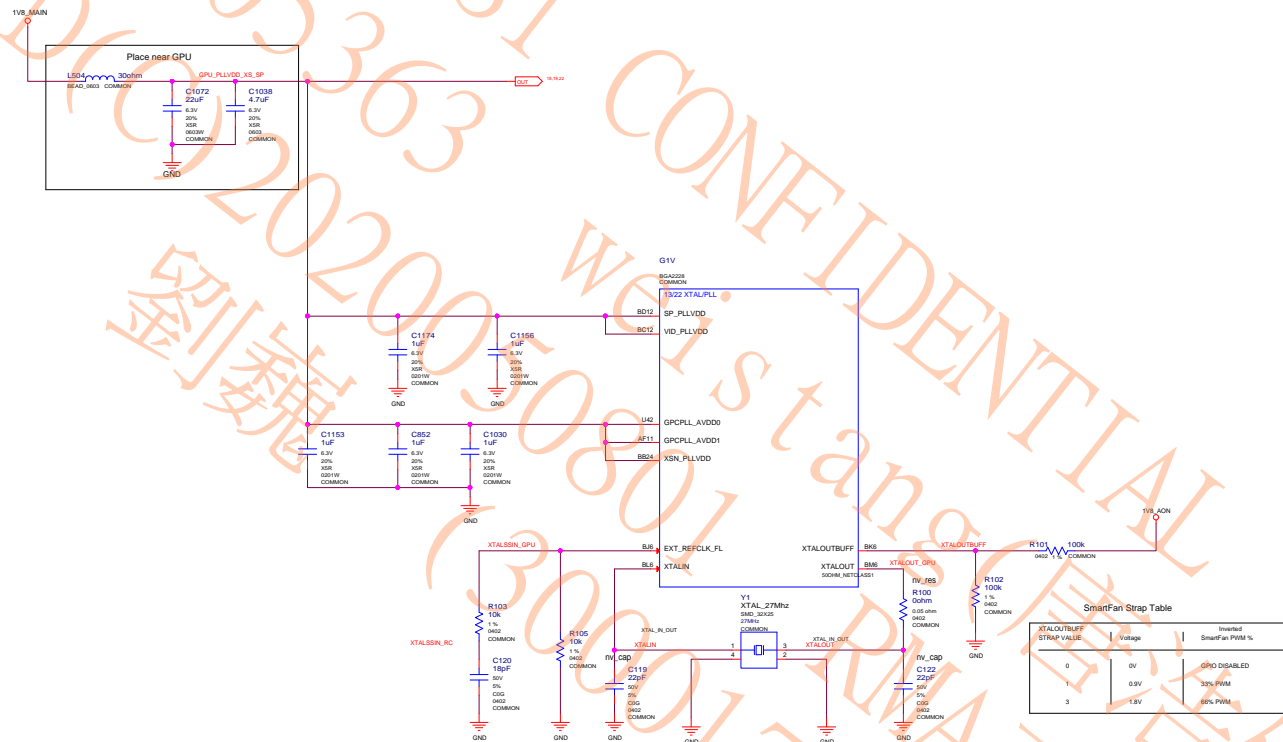
DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	1:SMB_ALT_ADDR ENABLE
M	H	L	1	1	1	0	0:SMB_ALT_ADDR DISABLE
M	L	H	1	1	0	1	1:DEVID_SEL REBRAND
M	L	L	1	1	0	0	0:DEVID_SEL ORIGINAL
L	H	M	1	0	1	1	1:PCIE_CFG LOW POWER
L	M	H	1	0	1	0	0:PCIE_CFG HIGH POWER
L	M	L	1	0	0	1	1:VGA_DEVICE ENABLE
L	L	M	1	0	0	0	0:VGA_DEVICE DISABLE
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	

Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung



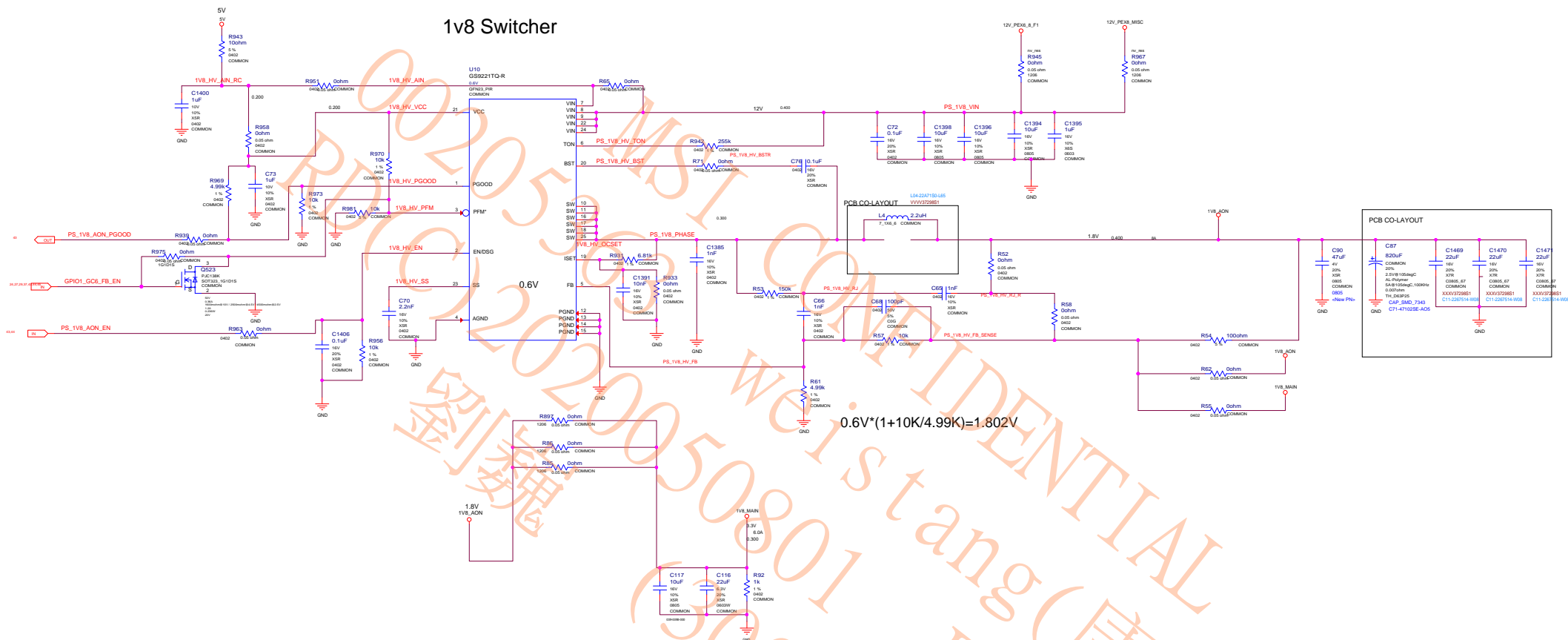




$$0.8V \cdot (1 + 40.2K/7.68K) = 4.9875V$$



1v8 Switcher

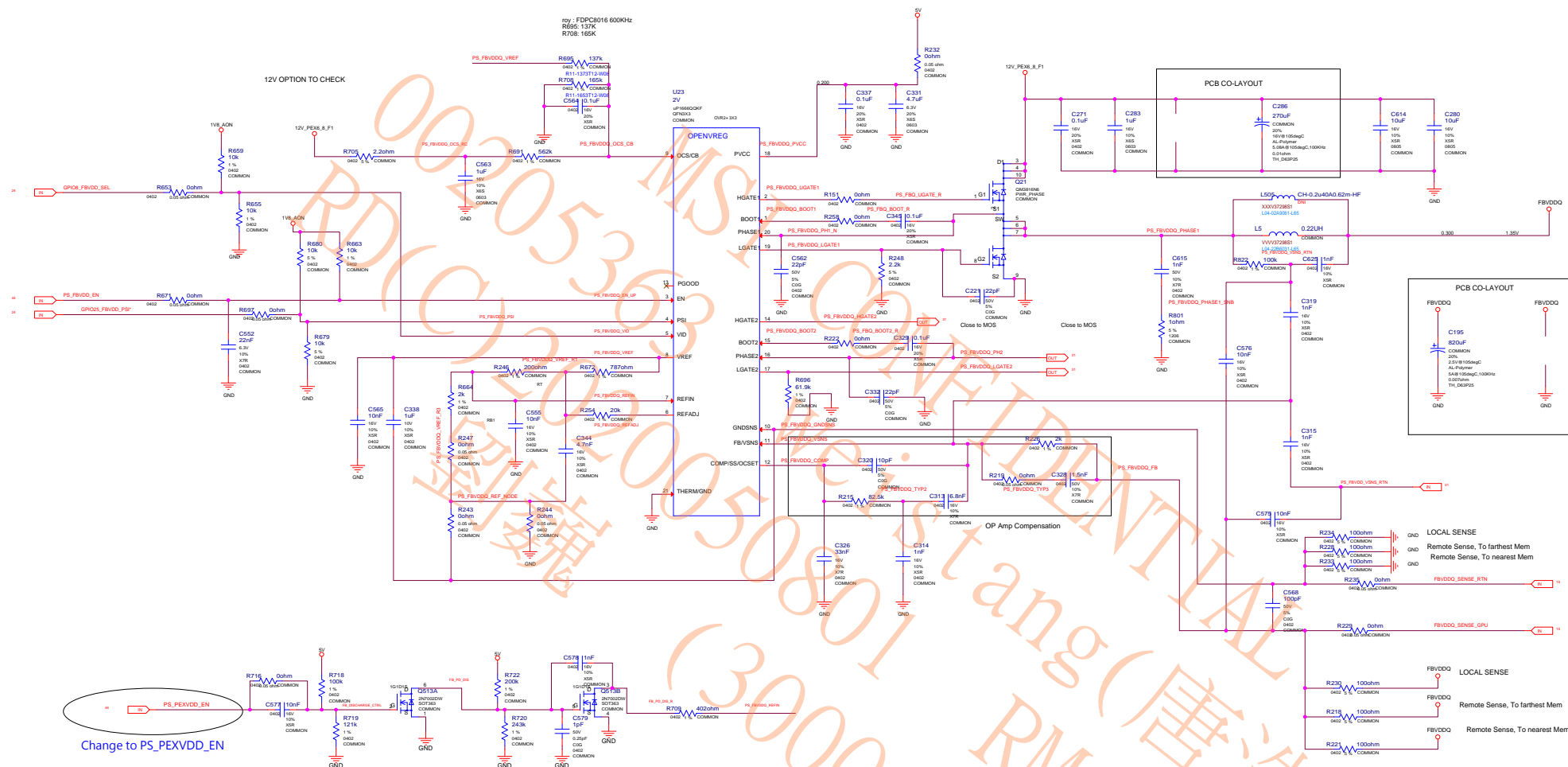


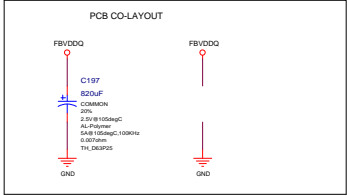
Remove PS_1V8_MAIN_EN

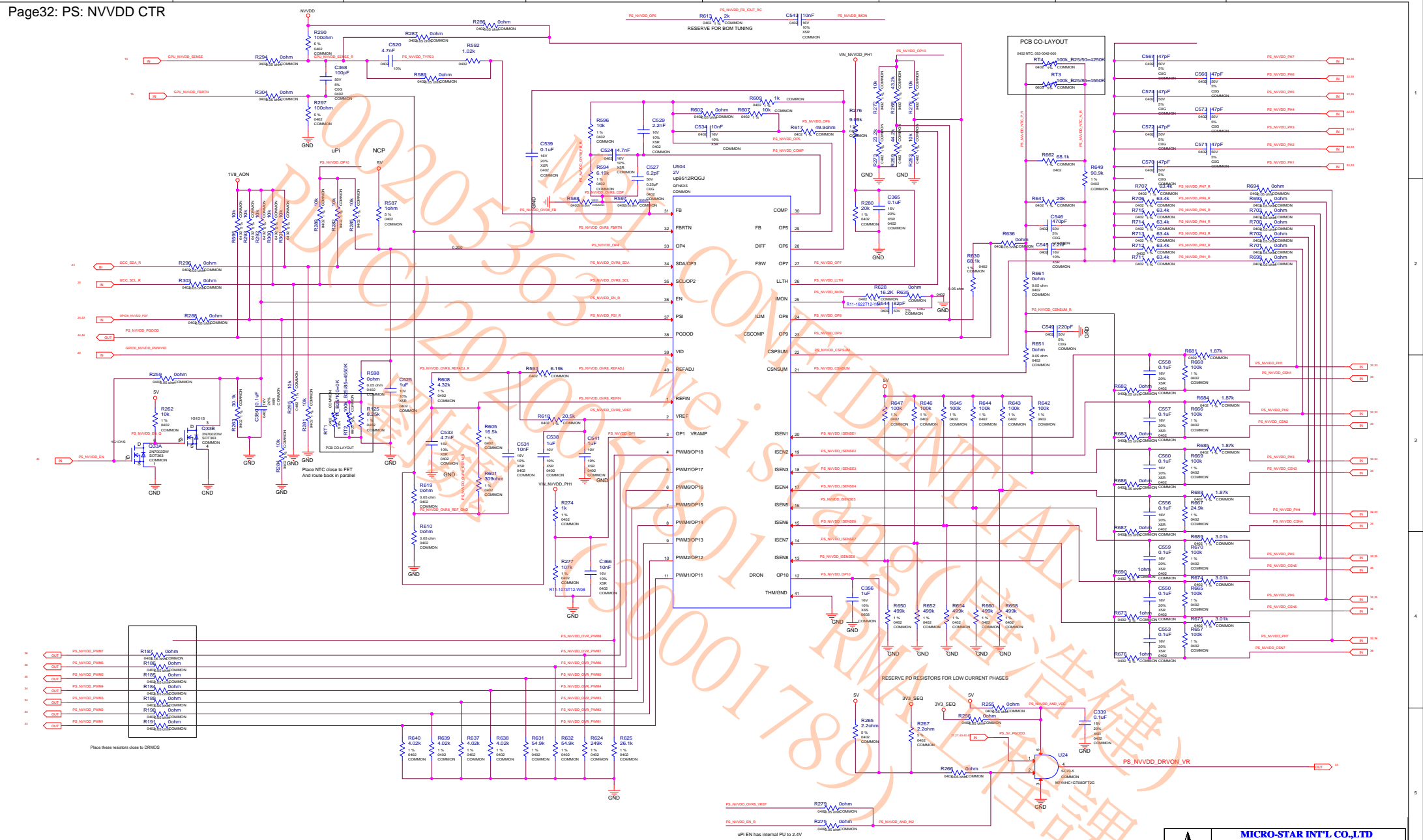
PEX Switcher

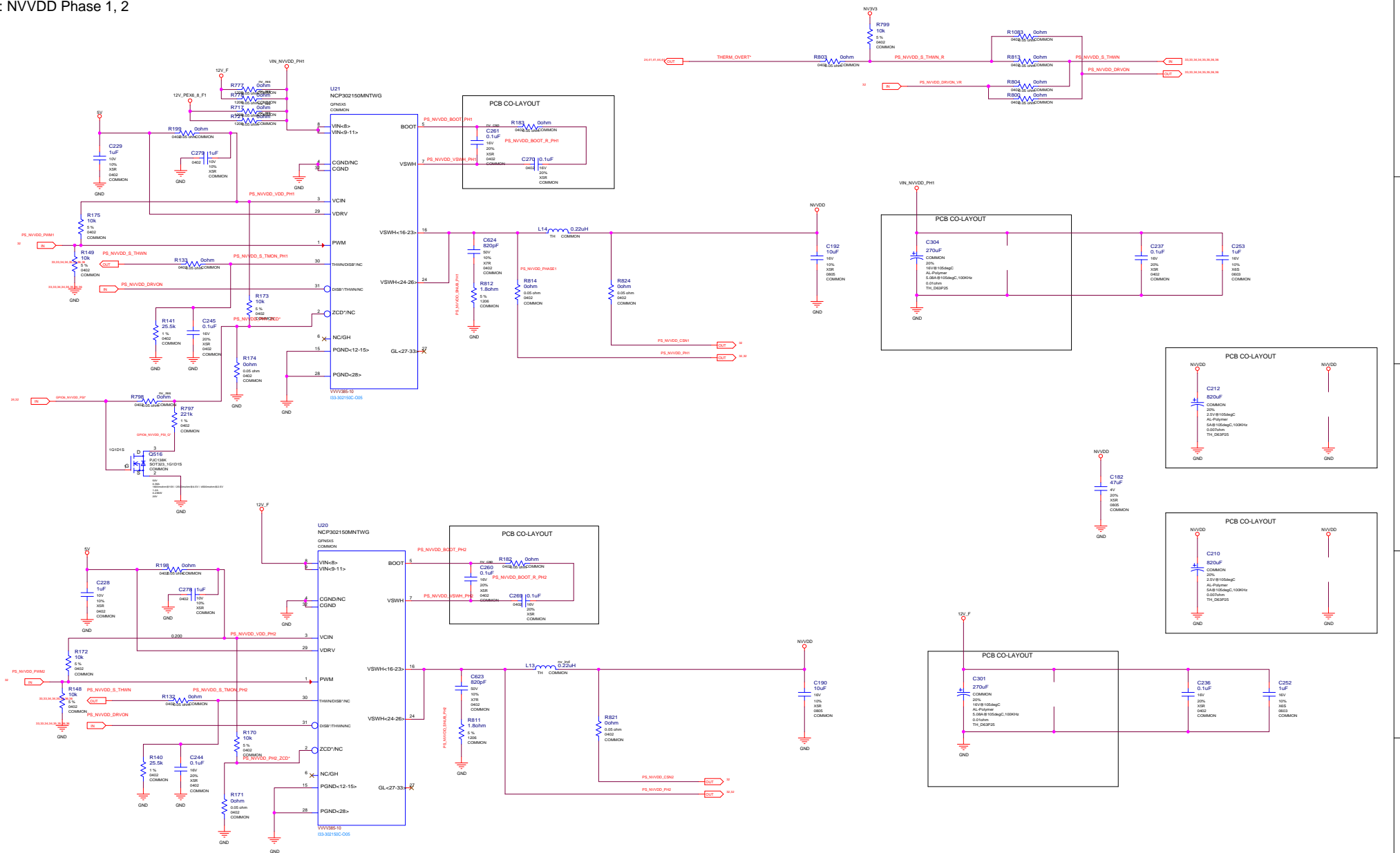
EN: $3.3V \cdot (10K/27.4K) = 1.2V$
ENABLE DISCHARGE OF PEX_VDD

$$0.6V \cdot (1 + 10K/14.7K) = 1.008V$$





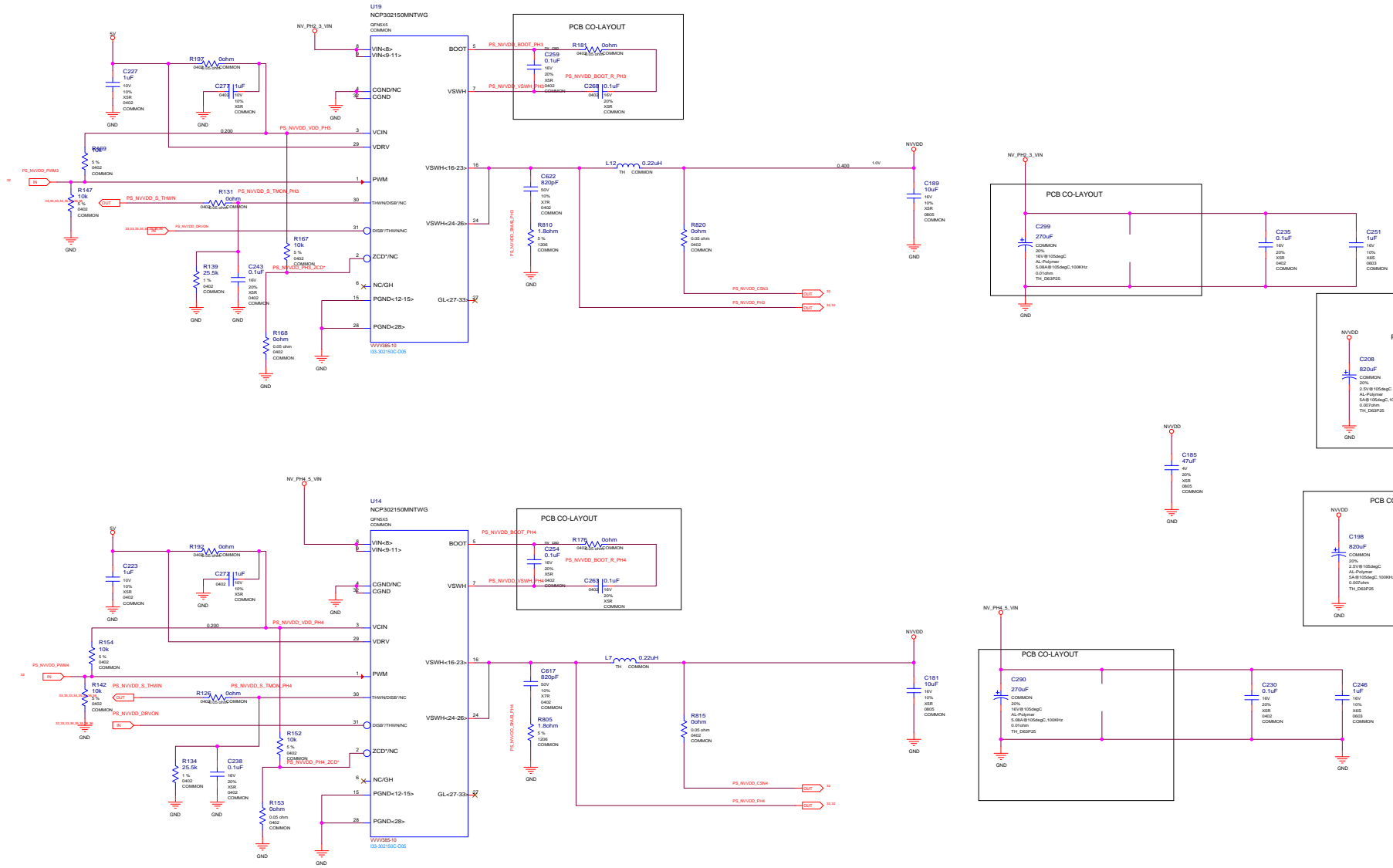


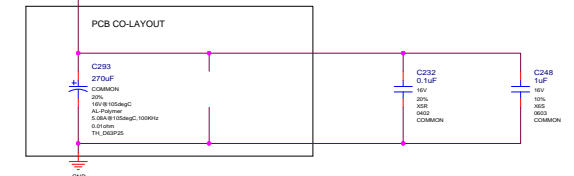
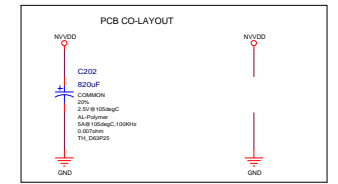


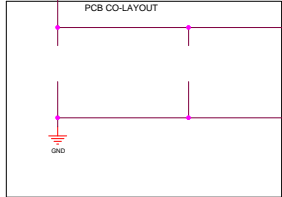
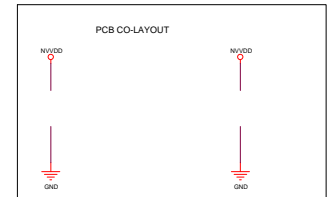
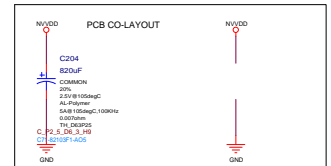
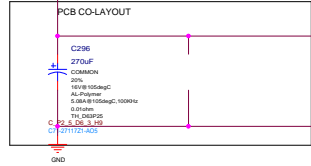
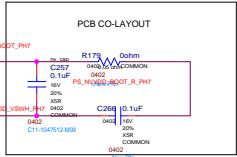
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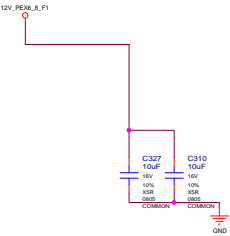
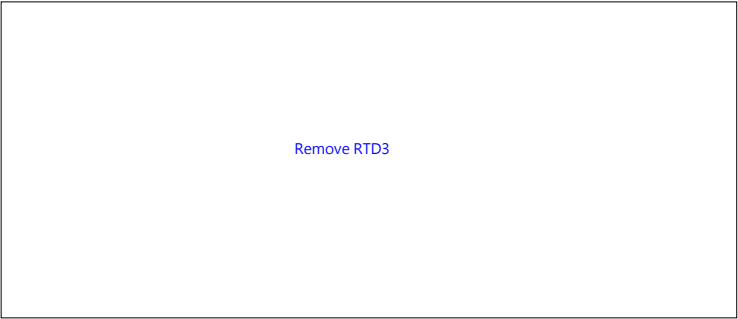


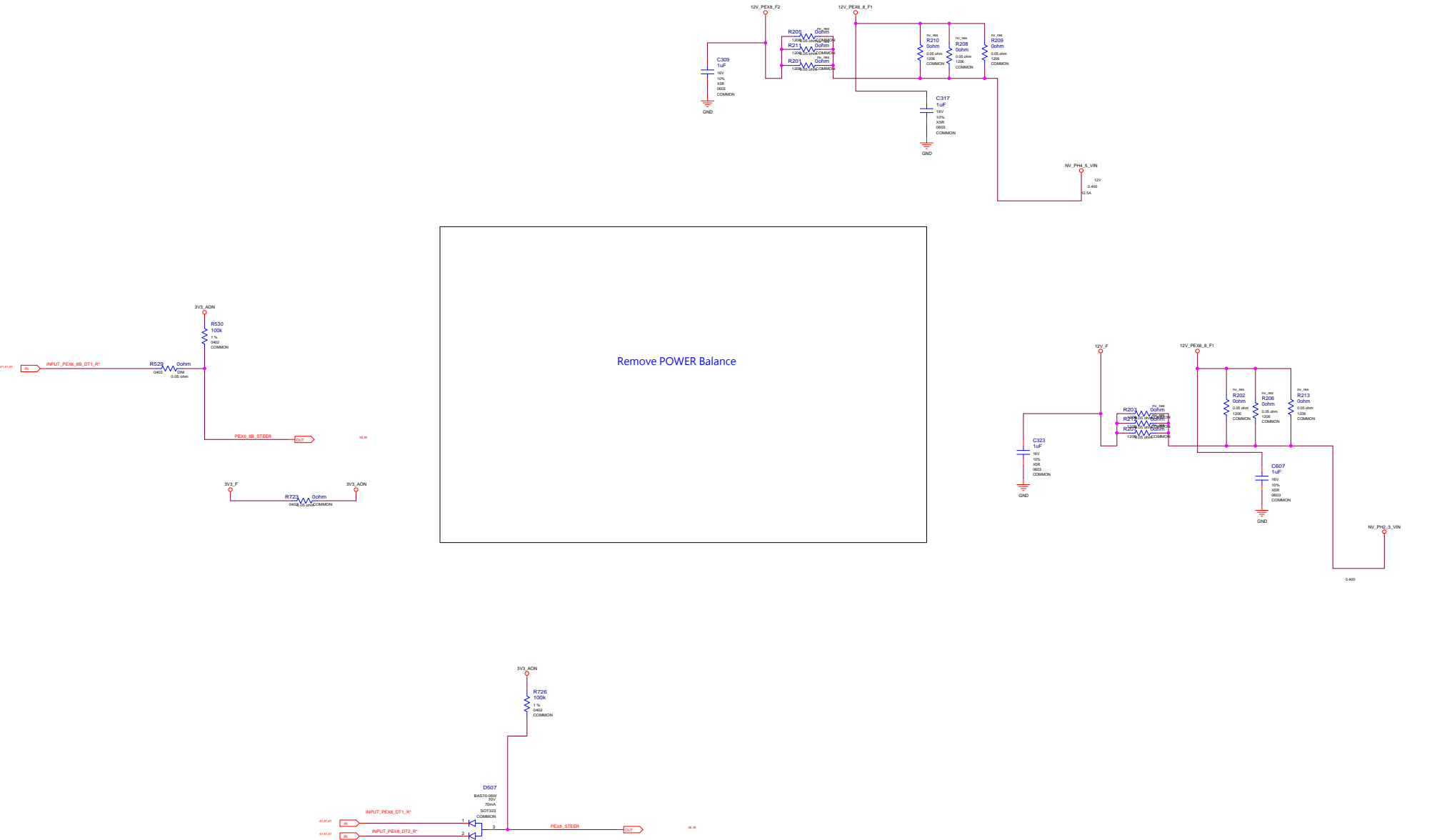




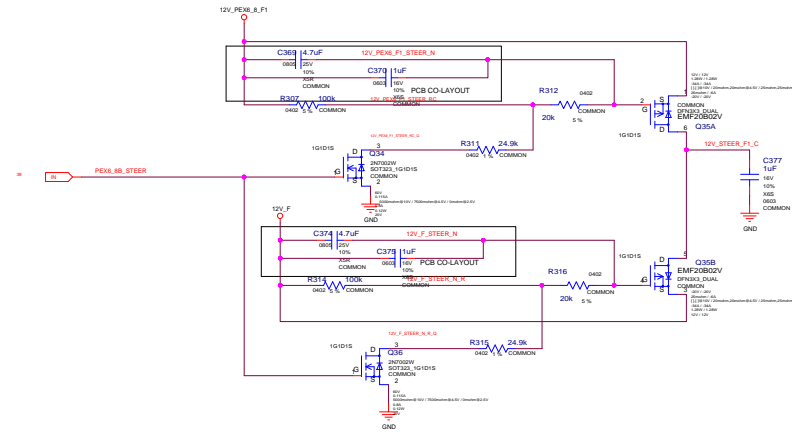
Remove Phase 8

AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

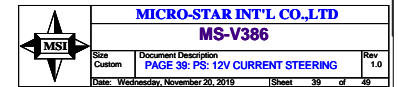
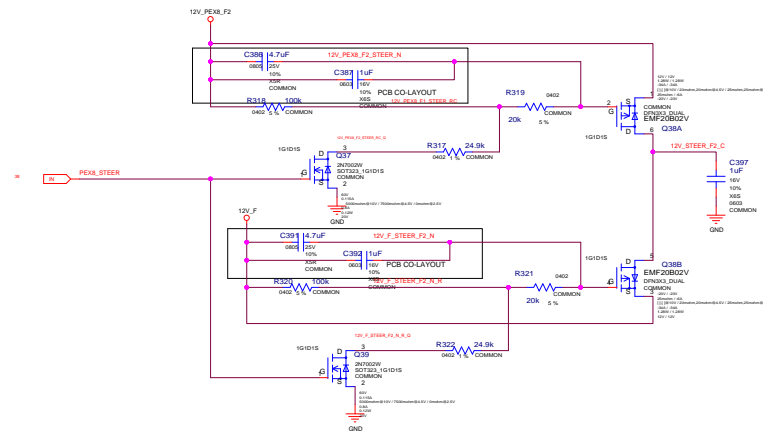


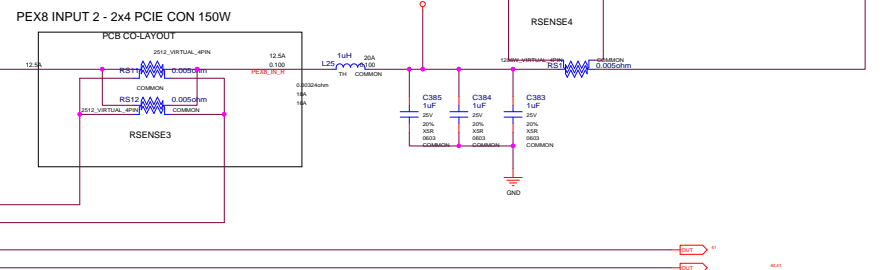
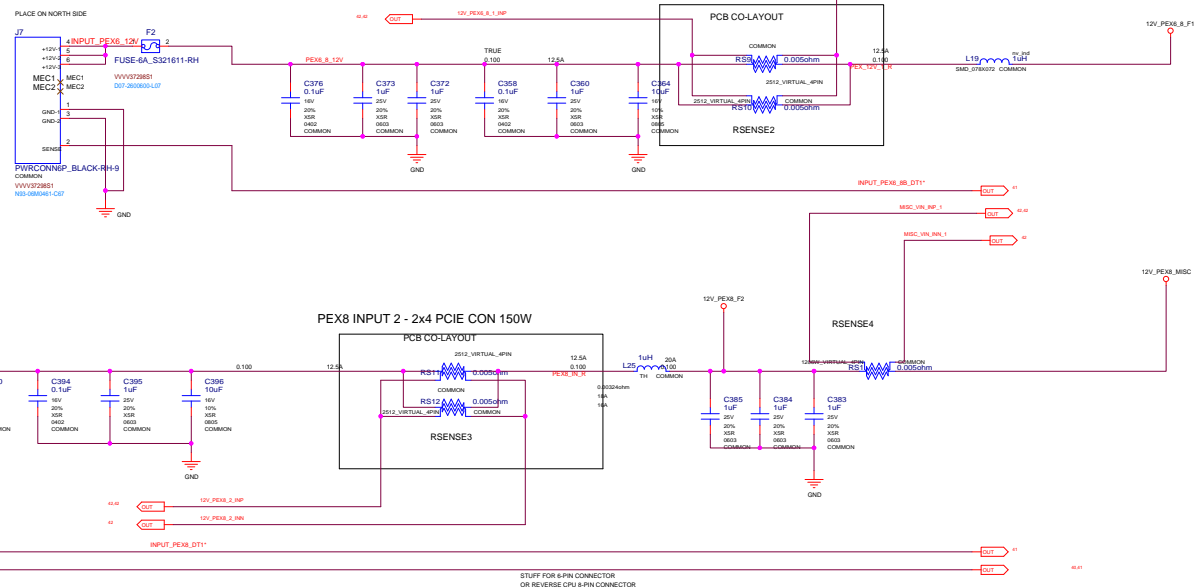
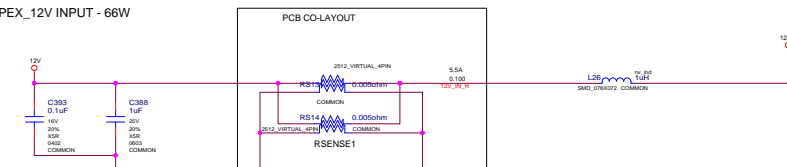
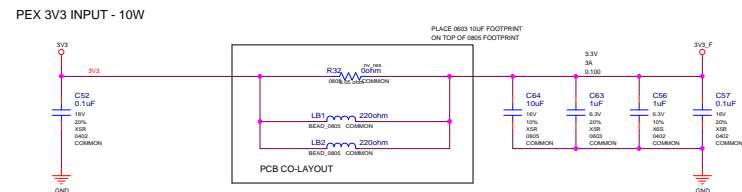


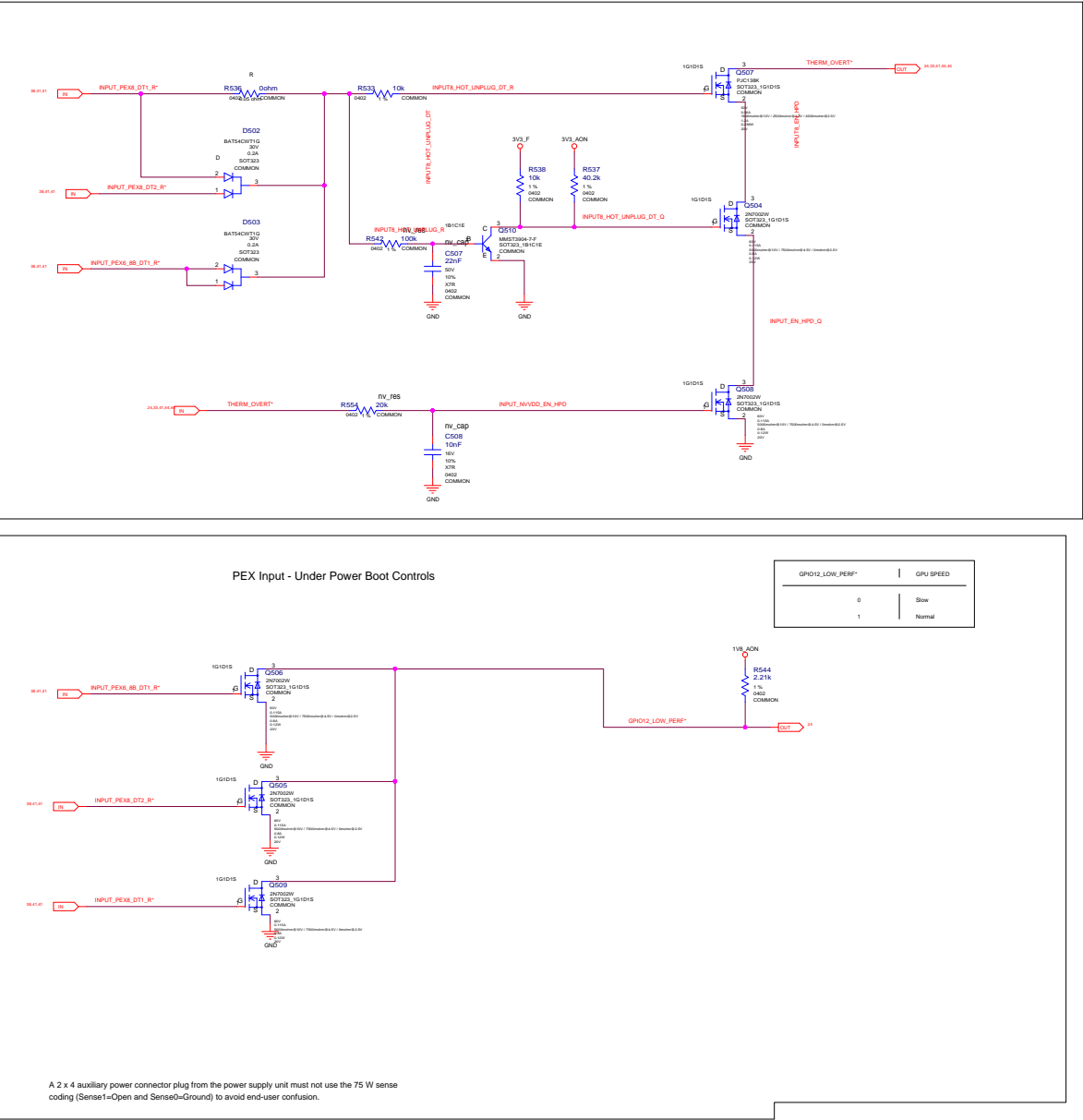
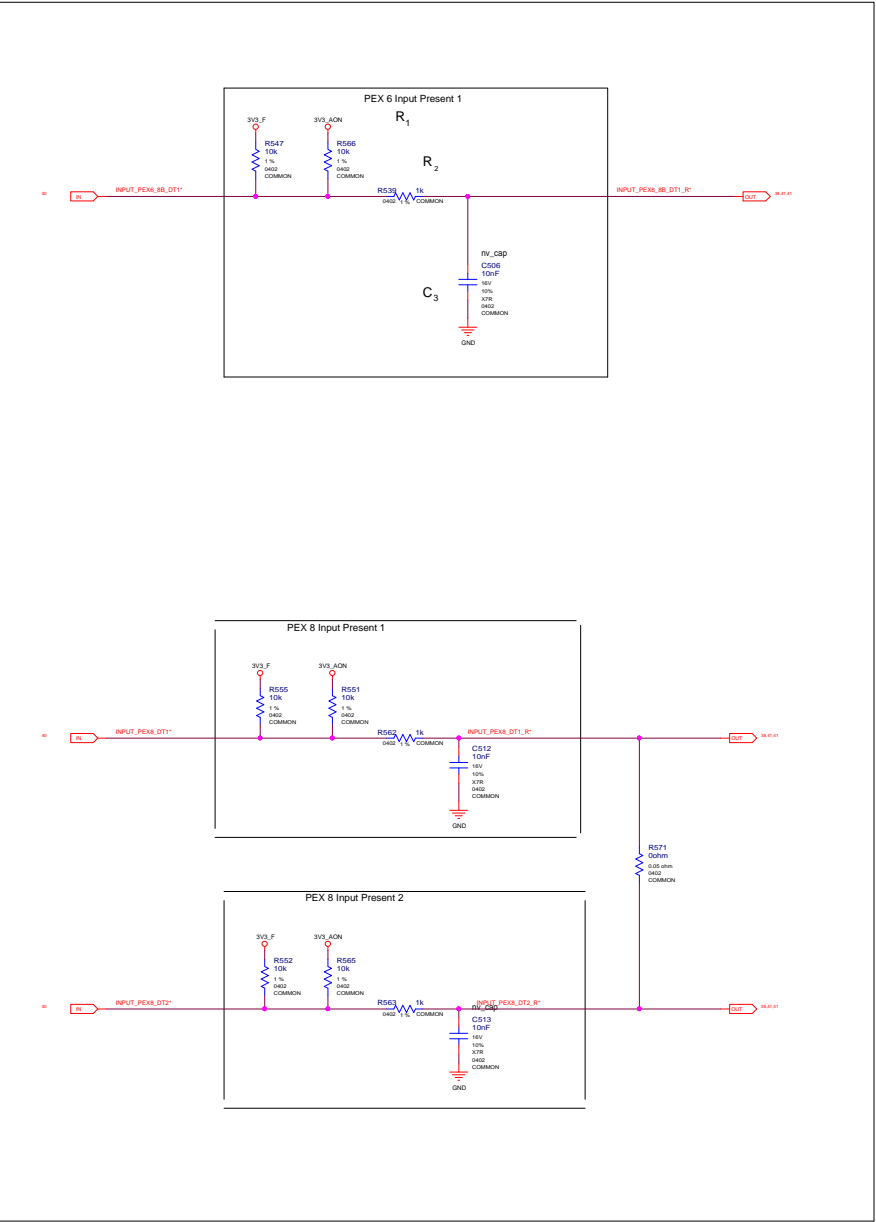
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

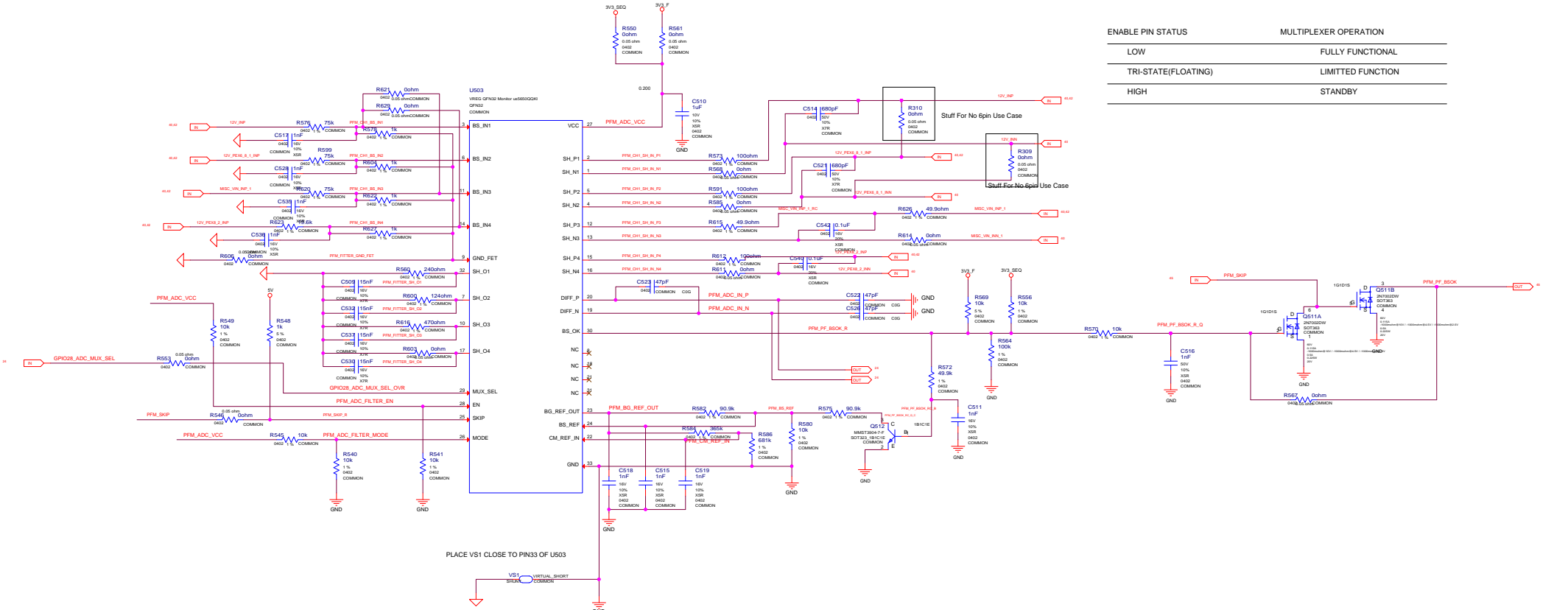


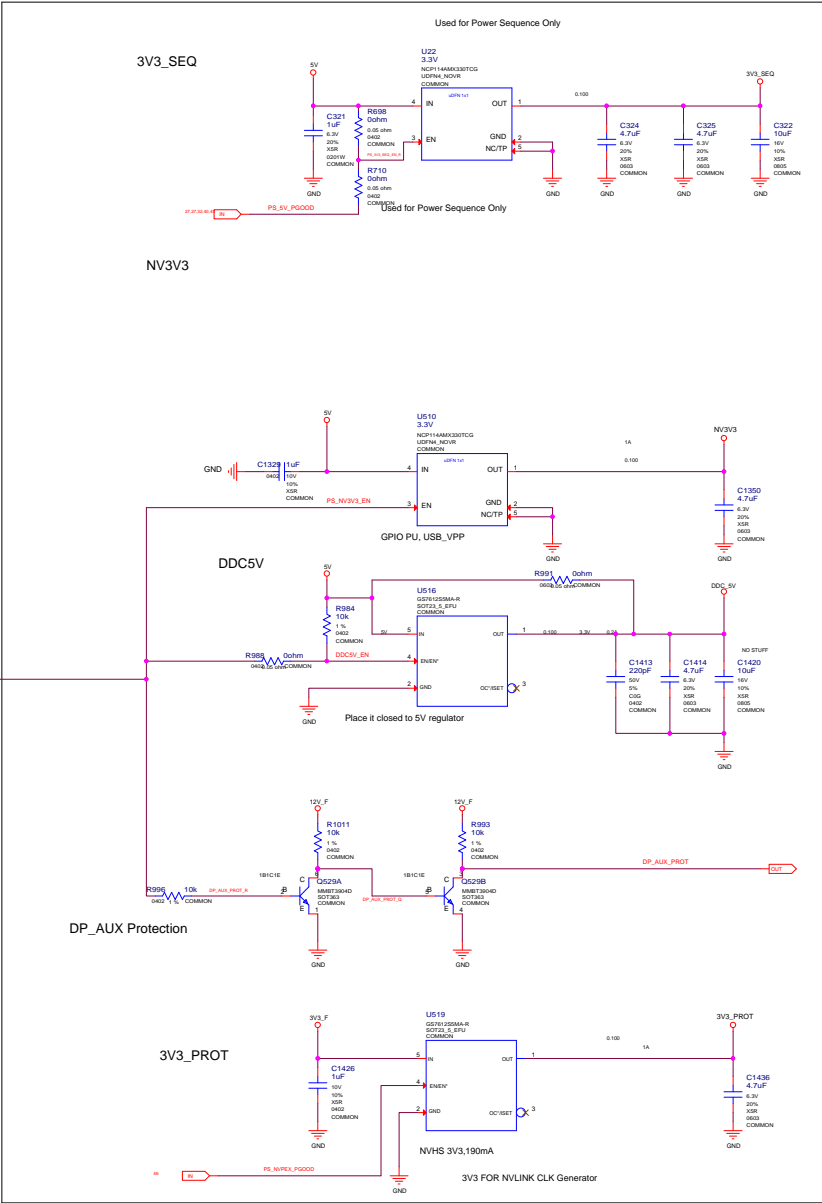
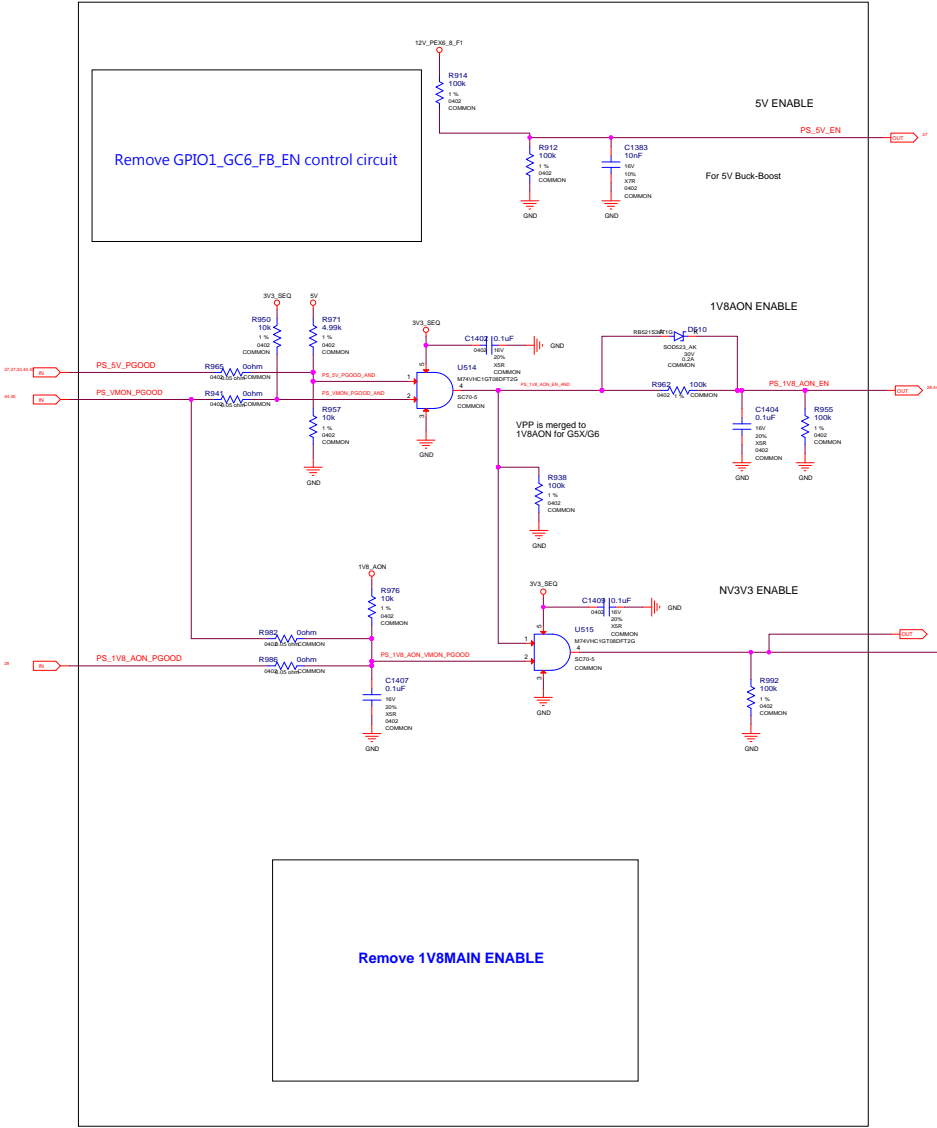
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

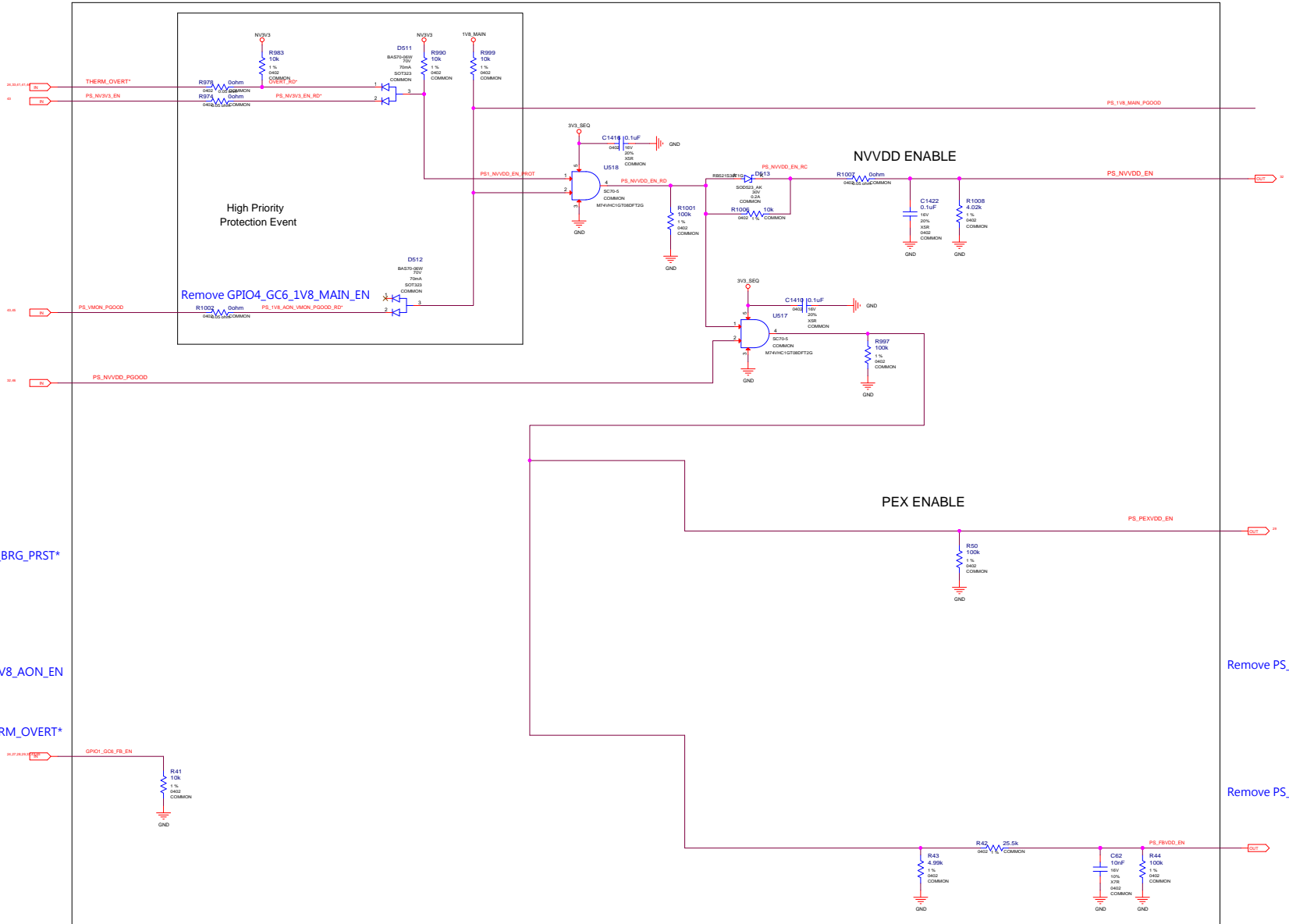


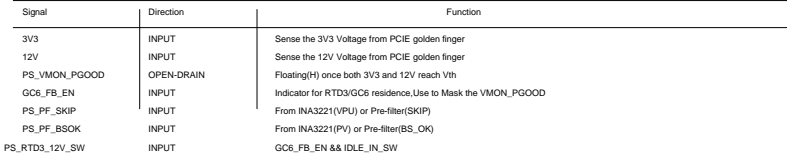





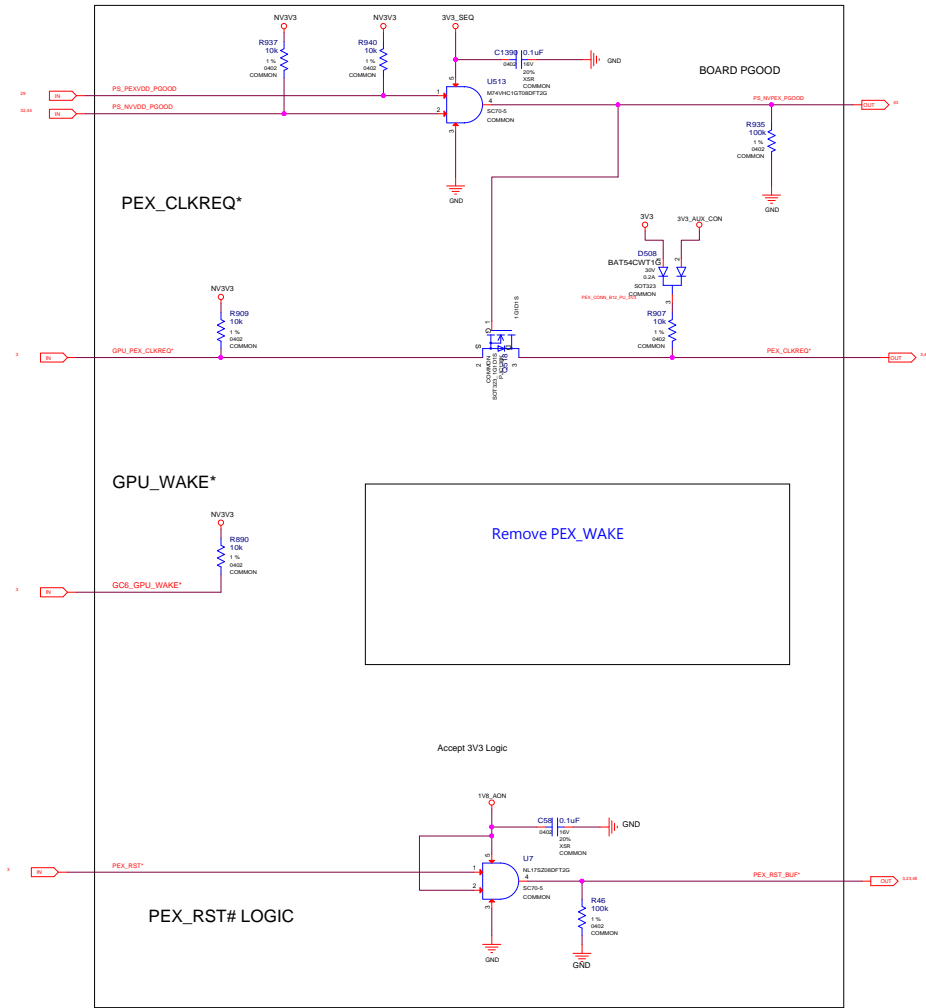




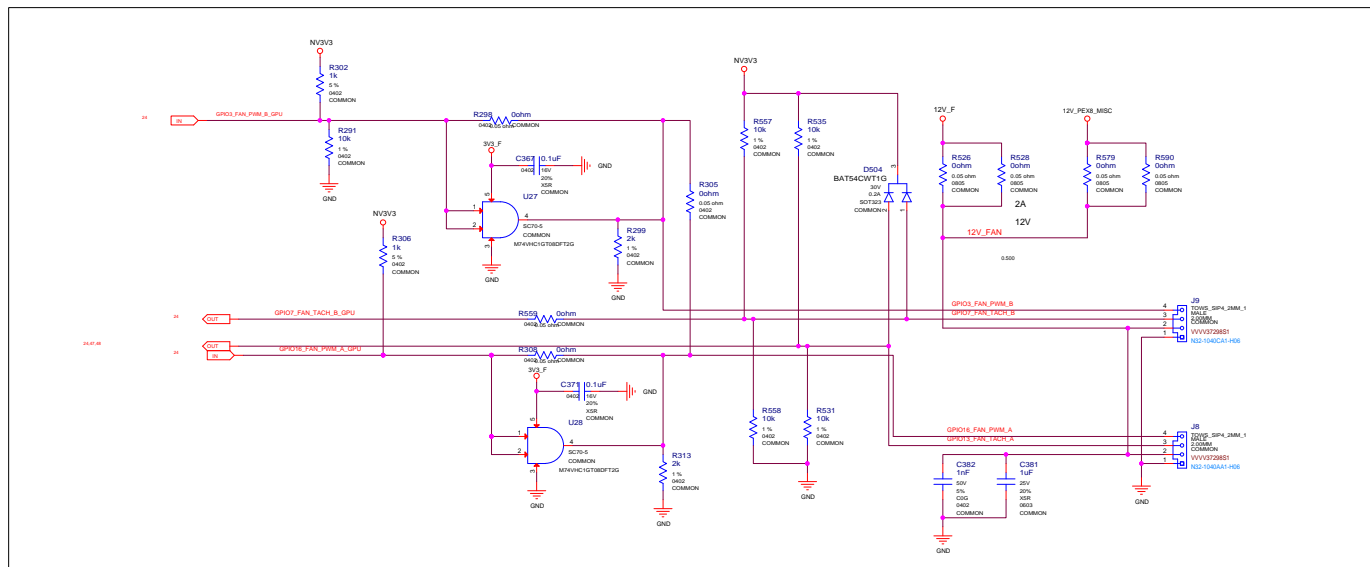




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Remvoe LED



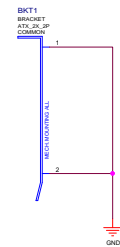
Remove LED BOOST



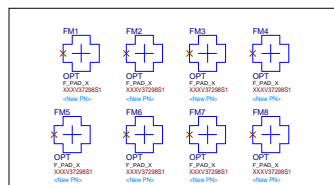
Remove LED2



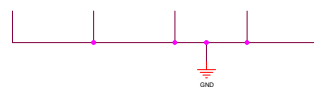
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HDMI_FEE
HDMI
\$\$\$\$\$
HDMI_FEE
COMMON
VVV386-10
Y01-RHDMI23-000



BOARD STIFFENER No connected mounting pins	MEC501 NCPIN COMMON
--	---------------------------



BGA SOCKET ASSY
12 connected mounting pins

MEC3
12PIN
COMMON

1 2 3 4 5 6 7 8 9 10 11 12

GND

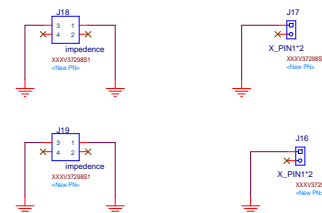


Figure 1: Schematic diagram of a 10-bus power system. The diagram shows a vertical busbar on the left connected to ground at the bottom. Ten buses are labeled MEC2-1 through MEC2-8. MEC2-1, MEC2-2, MEC2-3, and MEC2-4 are on the left busbar. MEC2-5, MEC2-6, MEC2-7, and MEC2-8 are on the right. Each bus has a circuit breaker symbol. Lines connect MEC2-1 to MEC2-5, MEC2-2 to MEC2-6, MEC2-3 to MEC2-7, and MEC2-4 to MEC2-8. Each line is labeled 'XB COMMON'.

