# P621-A02: G98-GB1-64, MXM-I, 256/128MB GDDR2 (32M/16Mx16),

# LVDS, HDMI, TV_OUT, VGA, HD Audio, DP option

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| SKU | VARIANT | NVPN | ASSEMBLY |
|---|---|---|---|
| 8 | Base | 600-10621-0000-200 | BASE LEVEL GENERIC SCHEMATIC ONLY |
| 1 | SKU0001 | 600-10621-0001-200 | NB9M-GS G98M ?/400MHz, 256MB(64bit) GDDR2 32Mx16 84FBGA, LVDS + HDMI + SD/HD(TV_OUT) + VGA |
| 2 | SKU0002 | 600-10621-0002-200 | Cancelled 128MB version |
| 3 | SKU0003 | 600-10621-0003-200 | NB9M-GE G98M ?/400MHz, 256MB(64bit) GDDR2 32Mx16 84FBGA, LVDS + HDMI + SD/HD(TV_OUT) + VGA |
| 4 | SKU9998 | 600-10621-9998-200 | All components |
| 5 | SKU0500 | 600-50621-0500-200 | G98-920 (G98-GLM) WORKSTATION SKU, DUAL TMDS, 256MB 32X16 DDR2 |
| 6 | <UNDEFINED> | <UNDEFINED> | <UNDEFINED> |
| 7 | <UNDEFINED> | <UNDEFINED> | <UNDEFINED> |
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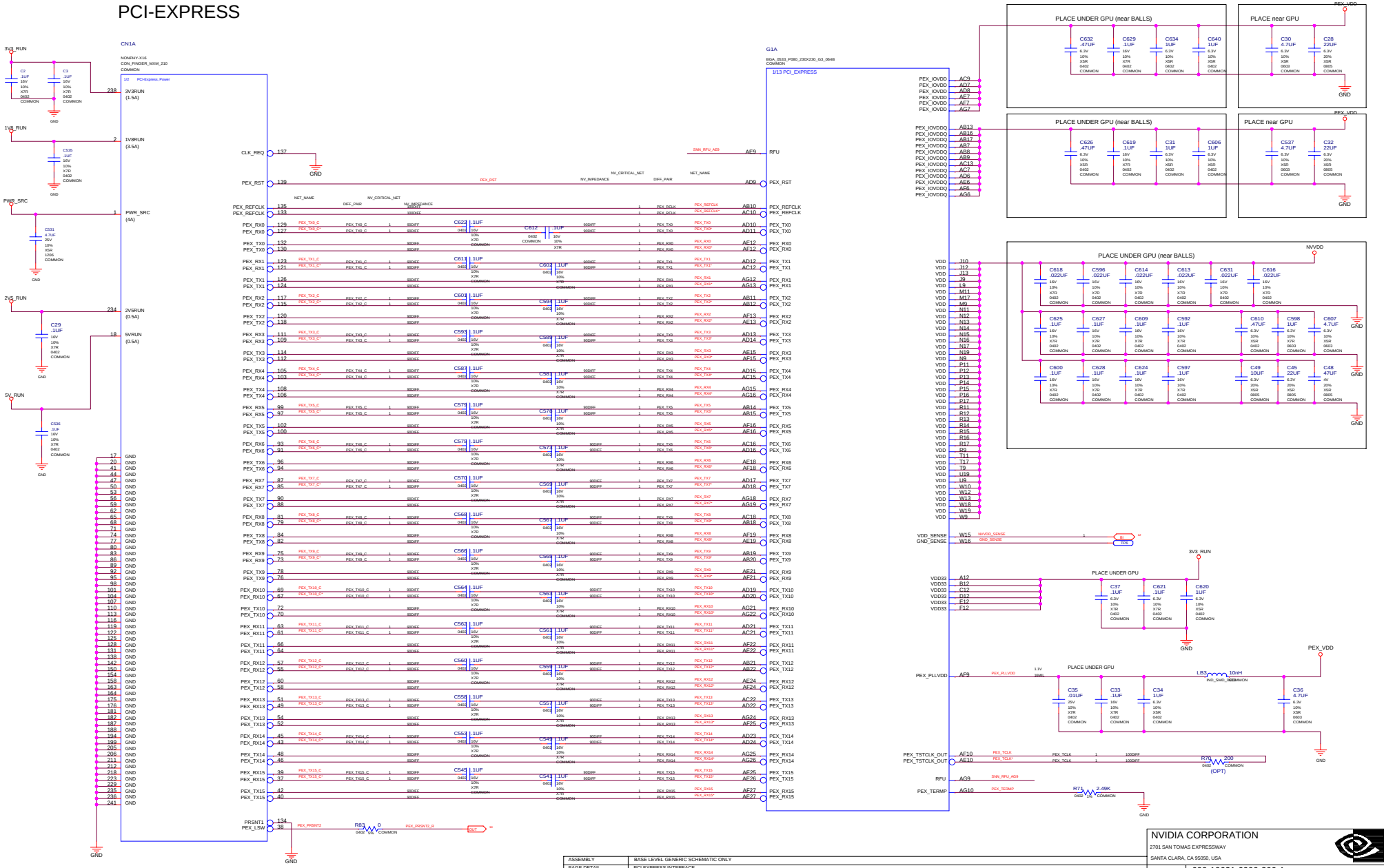
# PCI-EXPRESS

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| PAGE DETAIL | PCI EXPRESS INTERFACE |


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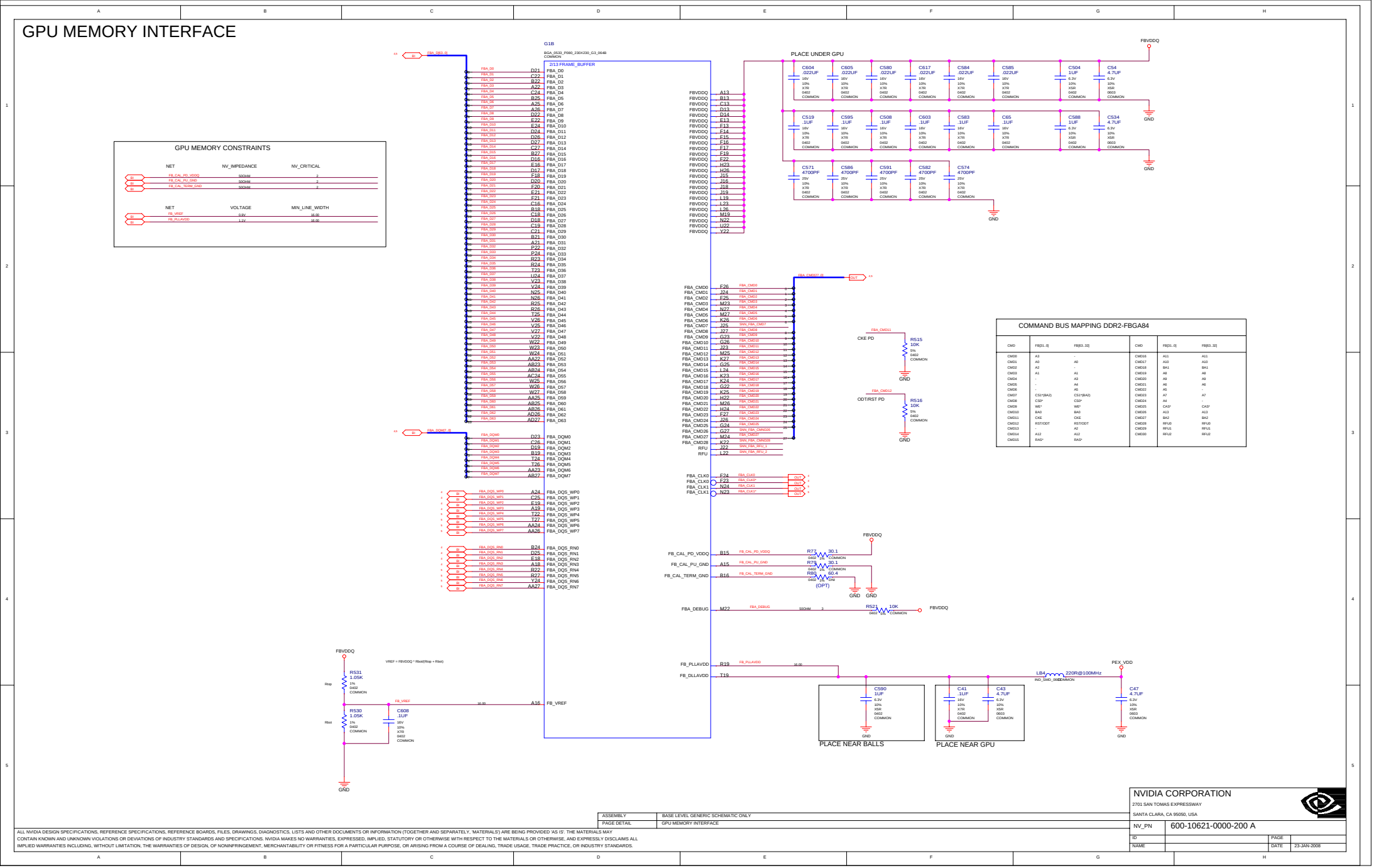
# GPU MEMORY INTERFACE

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|---|---|
| PAGE DETAIL | GPU MEMORY INTERFACE |


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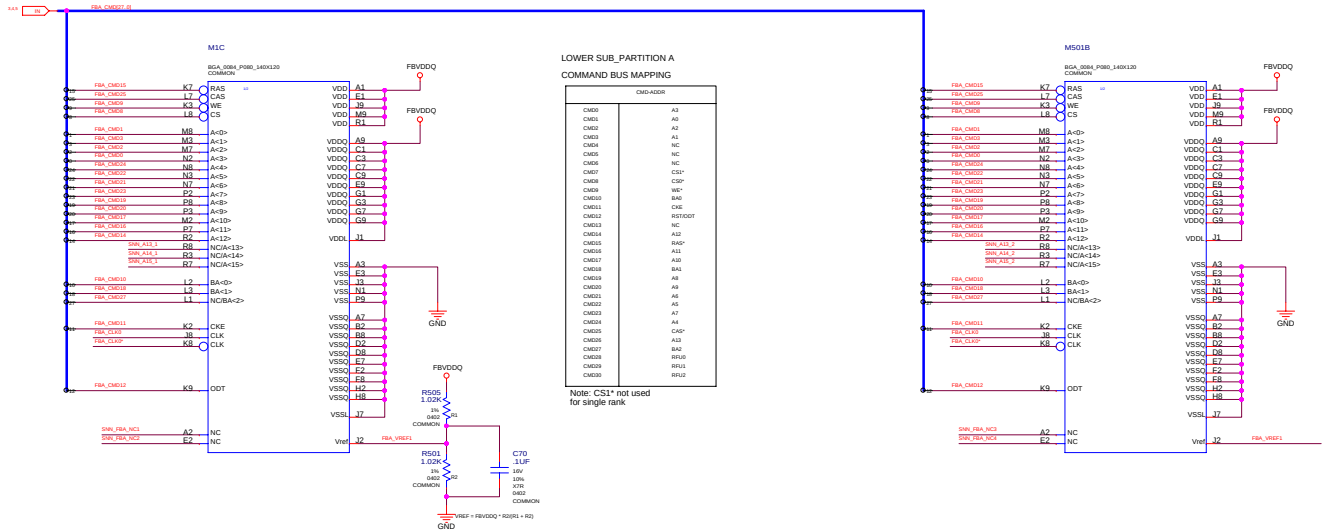
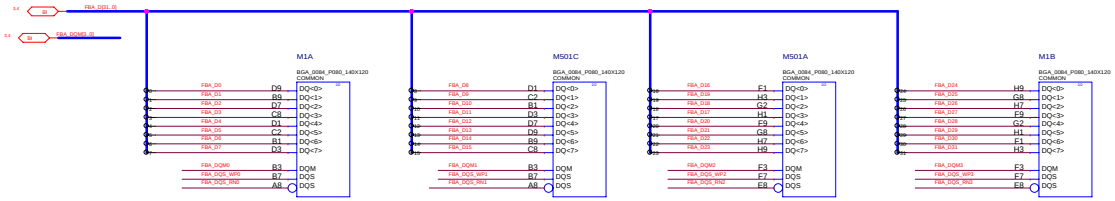
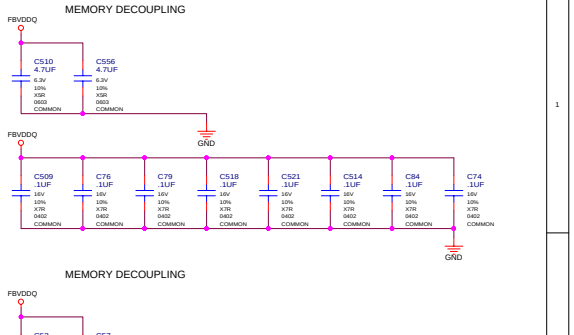
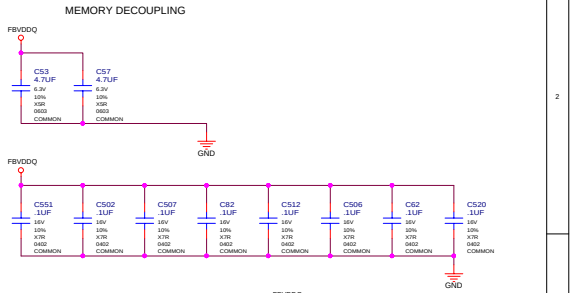
# MEMORY LOWER SUB-PARTITION INTERFACE D<31..0>

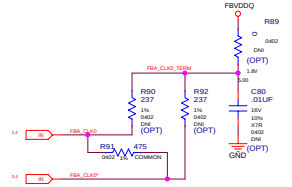



Place vias for both DQS, longest, and shortest bit of each byte just outside the memory packaged body.

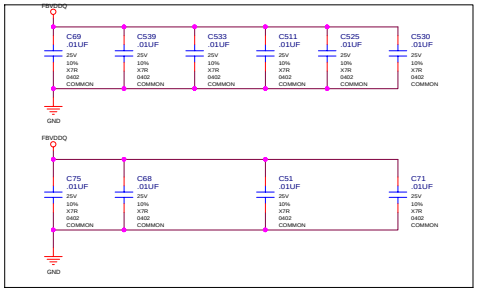


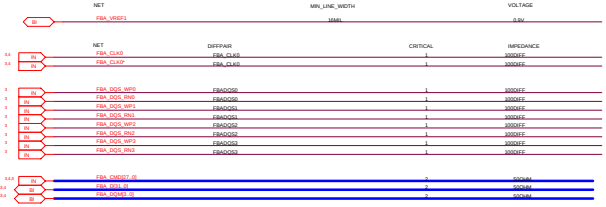




PLACE close to memorires so as to
Minimize the stub length!!
Single resistor termination to be placed on
same pads as 2 resistor termination

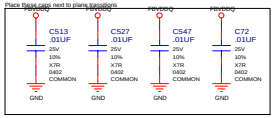
X-cap for CMD BUS




## MEMORY CONSTRAINTS




Place flying caps next to plane transitions

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| PAGE DETAIL | MEMORY LOWER SUB-PARTITION INTERFACE |

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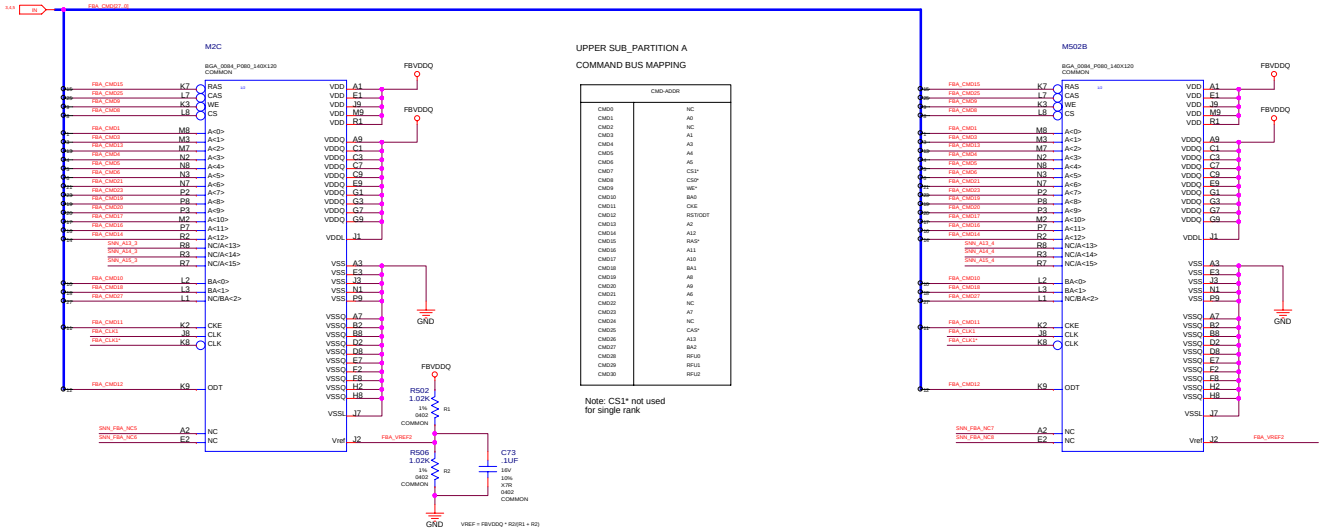
# MEMORY UPPER SUB-PARTITION INTERFACE D<63..32>

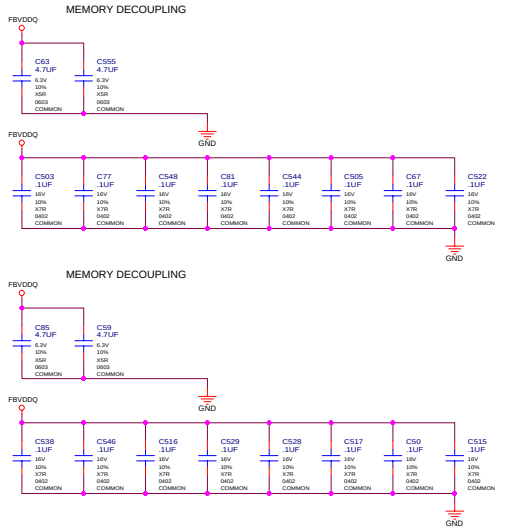


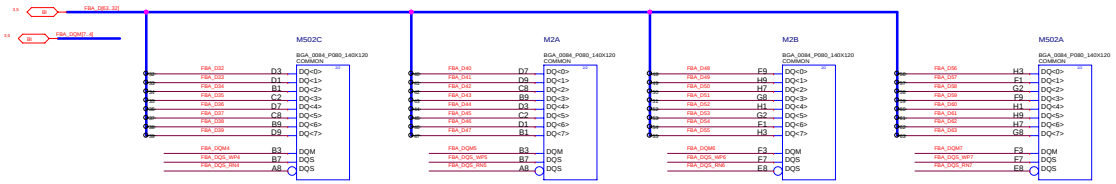

UPPER SUB_PARTITION A

COMMAND BUS MAPPING

| CMD-ADDR | |
|---|---|
| CMD0 | NC |
| CMD1 | A0 |
| CMD2 | NC |
| CMD3 | A1 |
| CMD4 | A3 |
| CMD5 | A4 |
| CMD6 | A5 |
| CMD7 | CS1* |
| CMD8 | CS0* |
| CMD9 | WE* |
| CMD10 | BA0 |
| CMD11 | CKE |
| CMD12 | RST/ODT |
| CMD13 | A2 |
| CMD14 | A12 |
| CMD15 | RAS* |
| CMD16 | A11 |
| CMD17 | A10 |
| CMD18 | BA1 |
| CMD19 | A6 |
| CMD20 | A9 |
| CMD21 | A6 |
| CMD22 | NC |
| CMD23 | A7 |
| CMD24 | NC |
| CMD25 | CAS* |
| CMD26 | A13 |
| CMD27 | BA2 |
| CMD28 | RFU0 |
| CMD29 | RFU1 |
| CMD30 | RFU2 |

Note: CS1* not used
for single rank




Place vias for both DQS, longest, and shortest
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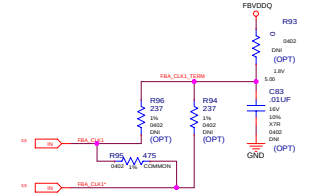


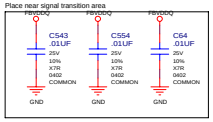

PLACE close to memorires so as to
Minimize the stub length!!
Single resistor termination to be placed on
same pads as 2 resistor termination

## MEMORY CONSTRAINTS

| NET | MIN_LINE_WIDTH | VOLTAGE |
|---|---|---|
| FBA_VREF2 | HMIL | 0.9V |

| NET | DIFFPAIR | CRITICAL | IMPEDANCE |
|---|---|---|---|
| FBA_CLK1 | FBA_CLK1 | 1 | 100DIFF |
| FBA_CLK1* | FBA_CLK1 | 1 | 100DIFF |
| FBA_DQS_WP4 | FBADQS4 | 1 | 100DIFF |
| FBA_DQS_RN4 | FBADQS4 | 1 | 100DIFF |
| FBA_DQS_WP5 | FBADQS5 | 1 | 100DIFF |
| FBA_DQS_RN5 | FBADQS5 | 1 | 100DIFF |
| FBA_DQS_WP6 | FBADQS6 | 1 | 100DIFF |
| FBA_DQS_RN6 | FBADQS6 | 1 | 100DIFF |
| FBA_DQS_WP7 | FBADQS7 | 1 | 100DIFF |
| FBA_DQS_RN7 | FBADQS7 | 1 | 100DIFF |
| FBA_CMD27..0 | | 2 | 50OHM |
| FBA_DB3..32 | | 2 | 50OHM |
| FBA_DQM7..4 | | 2 | 50OHM |

Place near signal transition area

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| PAGE DETAIL | MEMORY UPPER SUB-PARTITION INTERFACE |

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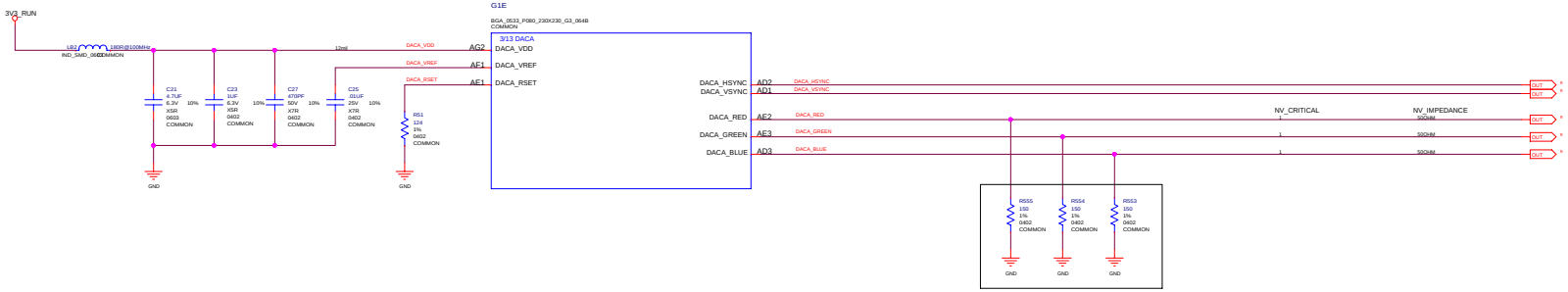
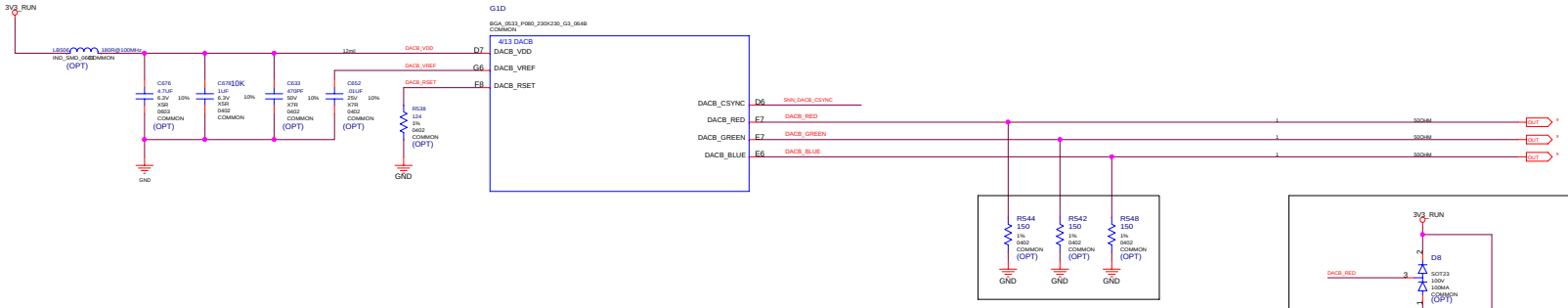
# DAC_A



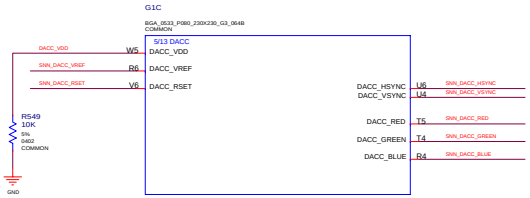

Place close to GPU

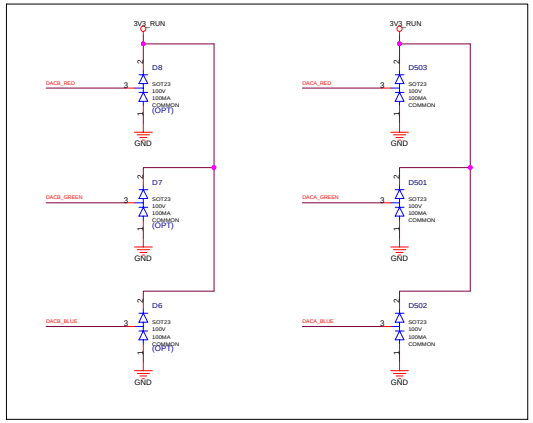
# DAC_B




Place close to GPU

# DAC_C




TV DAC ESD PROTECTION

| | |
|---|---|
| ASSEMBLY | |
| PAGE DETAIL | DAC A/B |

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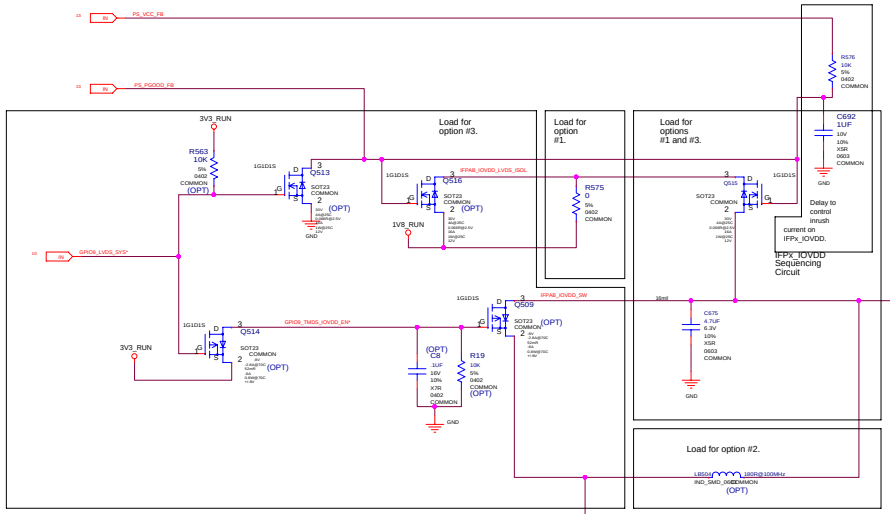
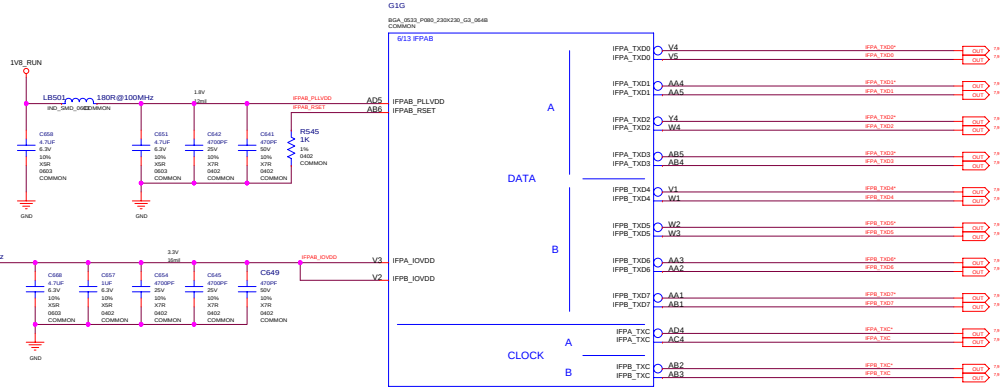
Loading options for IFPAB outputs

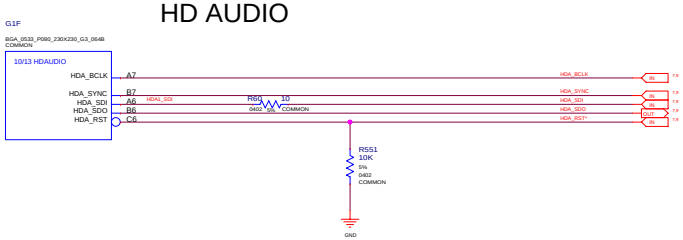
Option #1) IFPAB outputs to LVDS only.
Option #2) IFPAB outputs to DVI-C only.
Option #3) Controlled with GPIO9, IFPAB dynamically outputs to LVDS or DVI-C.




## LVDS/TMDS(link A&B)




## HD AUDIO




## (LVDS & HD AUDIO CONSTRAINTS)

| NET NAME | DIFFPAIR | NV_CRITICAL_NET | NV_IMPEDANCE |
|---|---|---|---|
| IFPA_TXD0* | IFPATXD0 | 1 | 100DIFF |
| IFPA_TXD0 | IFPATXD0 | 1 | 100DIFF |
| IFPA_TXD1* | IFPATXD1 | 1 | 100DIFF |
| IFPA_TXD1 | IFPATXD1 | 1 | 100DIFF |
| IFPA_TXD2* | IFPATXD2 | 1 | 100DIFF |
| IFPA_TXD2 | IFPATXD2 | 1 | 100DIFF |
| IFPA_TXD3* | IFPATXD3 | 1 | 100DIFF |
| IFPA_TXD3 | IFPATXD3 | 1 | 100DIFF |
| IFPB_TXD4* | IFPBTXD4 | 1 | 100DIFF |
| IFPB_TXD4 | IFPBTXD4 | 1 | 100DIFF |
| IFPB_TXD5* | IFPBTXD5 | 1 | 100DIFF |
| IFPB_TXD5 | IFPBTXD5 | 1 | 100DIFF |
| IFPB_TXD6* | IFPBTXD6 | 1 | 100DIFF |
| IFPB_TXD6 | IFPBTXD6 | 1 | 100DIFF |
| IFPB_TXD7* | IFPBTXD7 | 1 | 100DIFF |
| IFPB_TXD7 | IFPBTXD7 | 1 | 100DIFF |
| IFPA_TXC* | IFPATXC | 1 | 100DIFF |
| IFPA_TXC | IFPATXC | 1 | 100DIFF |
| IFPB_TXC* | IFPBTXC | 1 | 100DIFF |
| IFPB_TXC | IFPBTXC | 1 | 100DIFF |

| NET NAME | NV_CRITICAL_NET | NV_IMPEDANCE |
|---|---|---|
| HDA1_BCLK | 2 | 50OHM |
| HDA1_SYNC | 2 | 50OHM |
| HDA1_SDI | 2 | 50OHM |
| HDA1_SDO | 2 | 50OHM |
| HDA1_RST* | 2 | 50OHM |
| HDA_BCLK | 2 | 50OHM |
| HDA_SYNC | 2 | 50OHM |
| HDA_SDI | 2 | 50OHM |
| HDA_SDO | 2 | 50OHM |
| HDA_RST* | 2 | 50OHM |

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| PAGE DETAIL | LVDS(LINK A/B), HD AUDIO |

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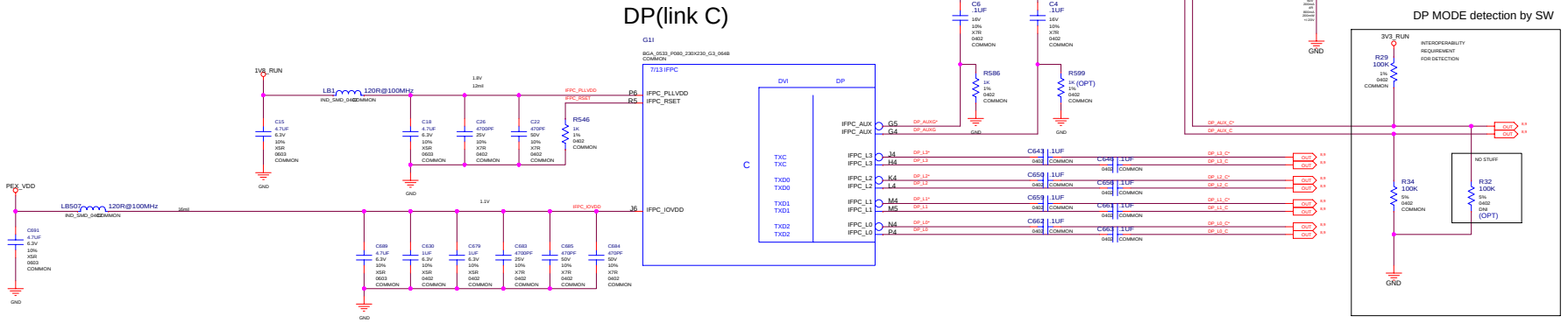


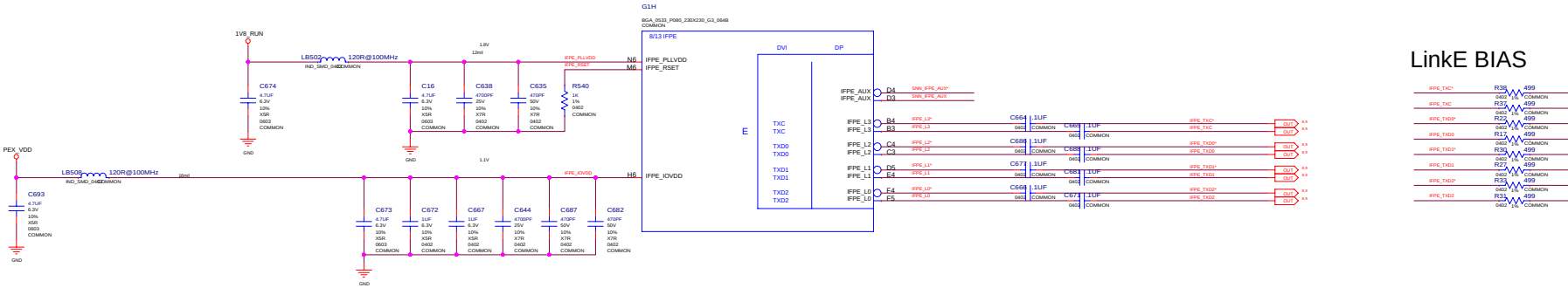


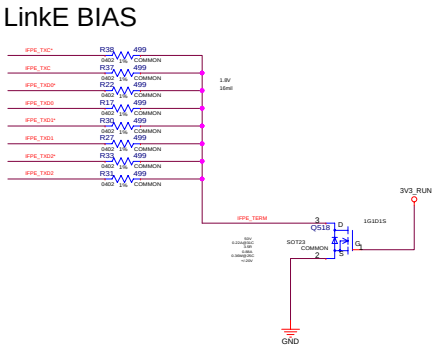


## (HDMI / DP CONSTRAINTS)

| NET NAME | DIFFPAIR | NV_CRITICAL_NET | NV_IMPEDANCE |
|---|---|---|---|
| IFPE_L3* | IFPE_L3 | 1 | 100DIFF |
| IFPE_L3 | IFPE_L3 | 1 | 100DIFF |
| IFPE_L2* | IFPE_L2 | 1 | 100DIFF |
| IFPE_L2 | IFPE_L2 | 1 | 100DIFF |
| IFPE_L1* | IFPE_L1 | 1 | 100DIFF |
| IFPE_L1 | IFPE_L1 | 1 | 100DIFF |
| IFPE_L0* | IFPE_L0 | 1 | 100DIFF |
| IFPE_L0 | IFPE_L0 | 1 | 100DIFF |
| IFPE_TXC* | IFPETXC | 1 | 100DIFF |
| IFPE_TXC | IFPETXC | 1 | 100DIFF |
| IFPE_TXD0* | IFPETXD0 | 1 | 100DIFF |
| IFPE_TXD0 | IFPETXD0 | 1 | 100DIFF |
| IFPE_TXD1* | IFPETXD1 | 1 | 100DIFF |
| IFPE_TXD1 | IFPETXD1 | 1 | 100DIFF |
| IFPE_TXD2* | IFPETXD2 | 1 | 100DIFF |
| IFPE_TXD2 | IFPETXD2 | 1 | 100DIFF |

| NET NAME | DIFFPAIR | NV_CRITICAL_NET | NV_IMPEDANCE |
|---|---|---|---|
| DP_AUXG* | DP_AUX | 1 | 100DIFF |
| DP_AUXG | DP_AUX | 1 | 100DIFF |
| DP_AUXG_R* | DP_AUX1 | 1 | 100DIFF |
| DP_AUXG_R | DP_AUX1 | 1 | 100DIFF |
| DP_L3* | DP_L3 | 1 | 100DIFF |
| DP_L3 | DP_L3 | 1 | 100DIFF |
| DP_L2* | DP_L2 | 1 | 100DIFF |
| DP_L2 | DP_L3 | 1 | 100DIFF |
| DP_L1* | DP_L1 | 1 | 100DIFF |
| DP_L1 | DP_L1 | 1 | 100DIFF |
| DP_L0* | DP_L0 | 1 | 100DIFF |
| DP_L0 | DP_L0 | 1 | 100DIFF |

| NET NAME | DIFFPAIR | NV_CRITICAL_NET | NV_IMPEDANCE |
|---|---|---|---|
| DP_AUX_C* | DP_AUX3 | 1 | 100DIFF |
| DP_AUX_C | DP_AUX3 | 1 | 100DIFF |
| DP_AUXT* | DP_AUX2 | 1 | 100DIFF |
| DP_AUXT | DP_AUX2 | 1 | 100DIFF |
| DP_L3_C* | DP1.3C | 1 | 100DIFF |
| DP_L3_C | DP1.3C | 1 | 100DIFF |
| DP_L2_C* | DP1.2C | 1 | 100DIFF |
| DP_L2_C | DP1.2C | 1 | 100DIFF |
| DP_L1_C* | DP1.1C | 1 | 100DIFF |
| DP_L1_C | DP1.1C | 1 | 100DIFF |
| DP_L0_C* | DP1.0C | 1 | 100DIFF |
| DP_L0_C | DP1.0C | 1 | 100DIFF |

| | |
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| PAGE DETAIL | HDMI, DP |

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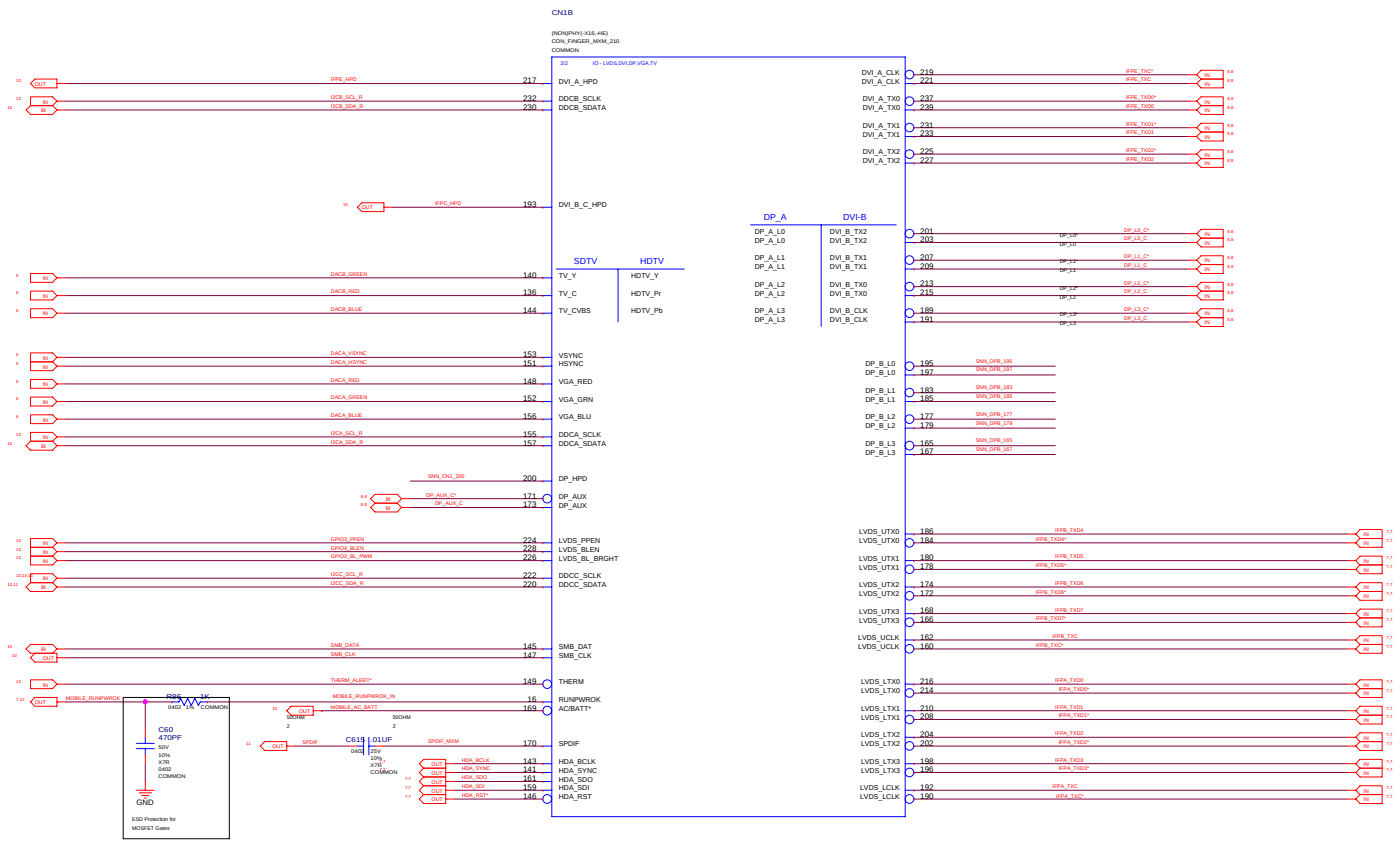
| NAME | |
| PAGE | |
| DATE | 23-JAN-2008 |

# MXM CONNECTOR

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| PAGE DETAIL | MXM CONNECTOR |

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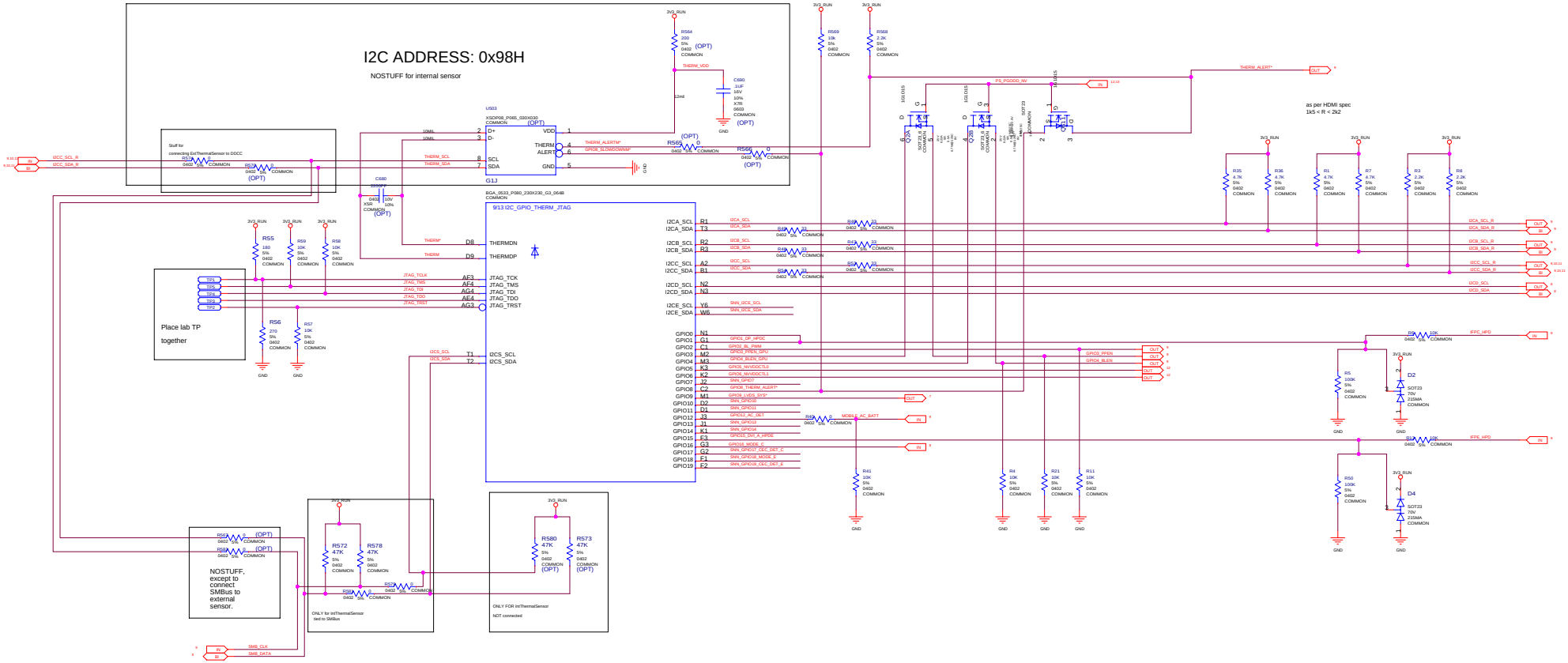
| NAME | | DATE | 23-JAN-2008 |

# GPIO, TEMP SENSOR, JTAG

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| PAGE DETAIL | GPIO, JTAG, TEMP SENSOR |

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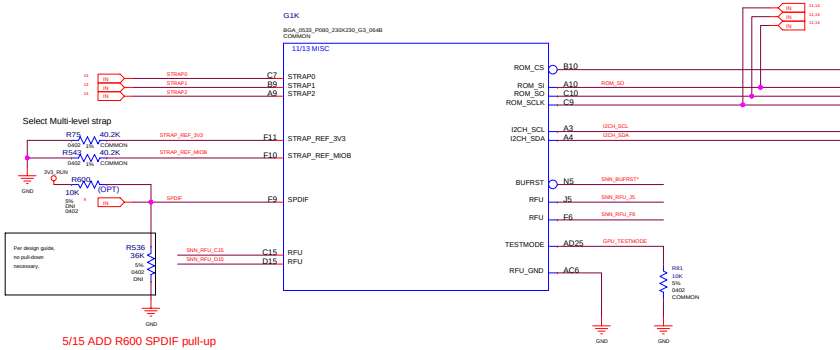
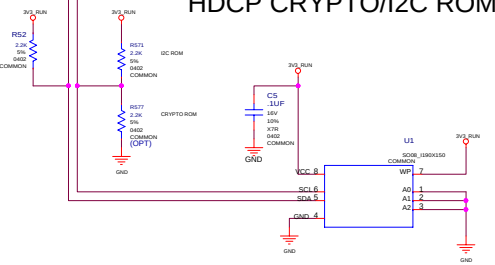
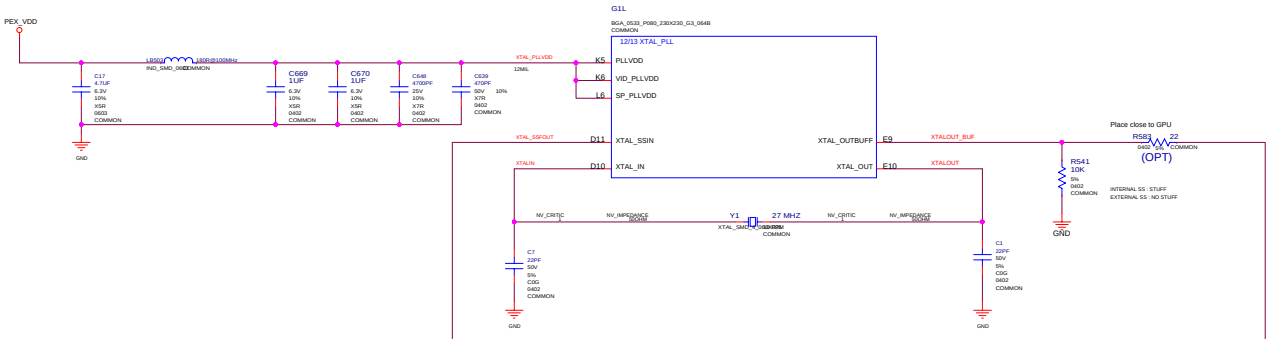
# VBIOS ROM



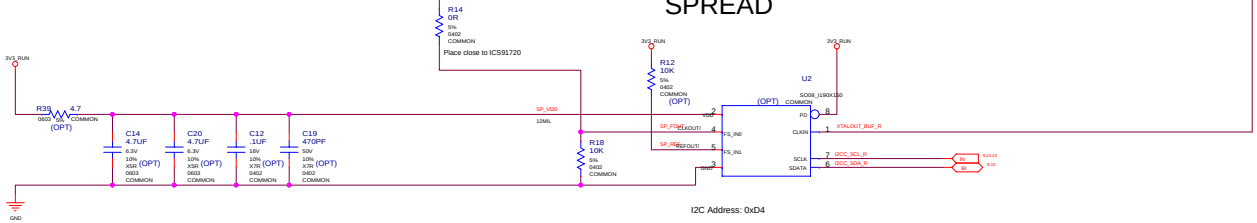

# HDCP CRYPTO/I2C ROM

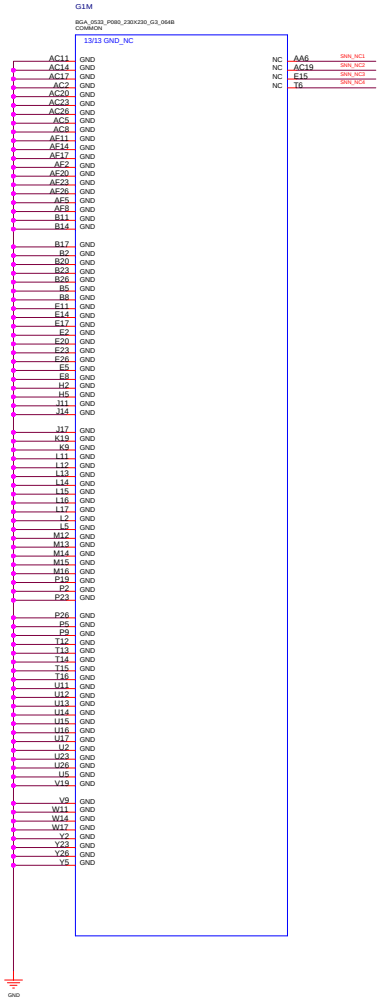



# XTAL




# SPREAD

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| PAGE DETAIL | VBIOS & HDCP ROM, XTAL, SPREAD SPECTRUM, SPDIF |

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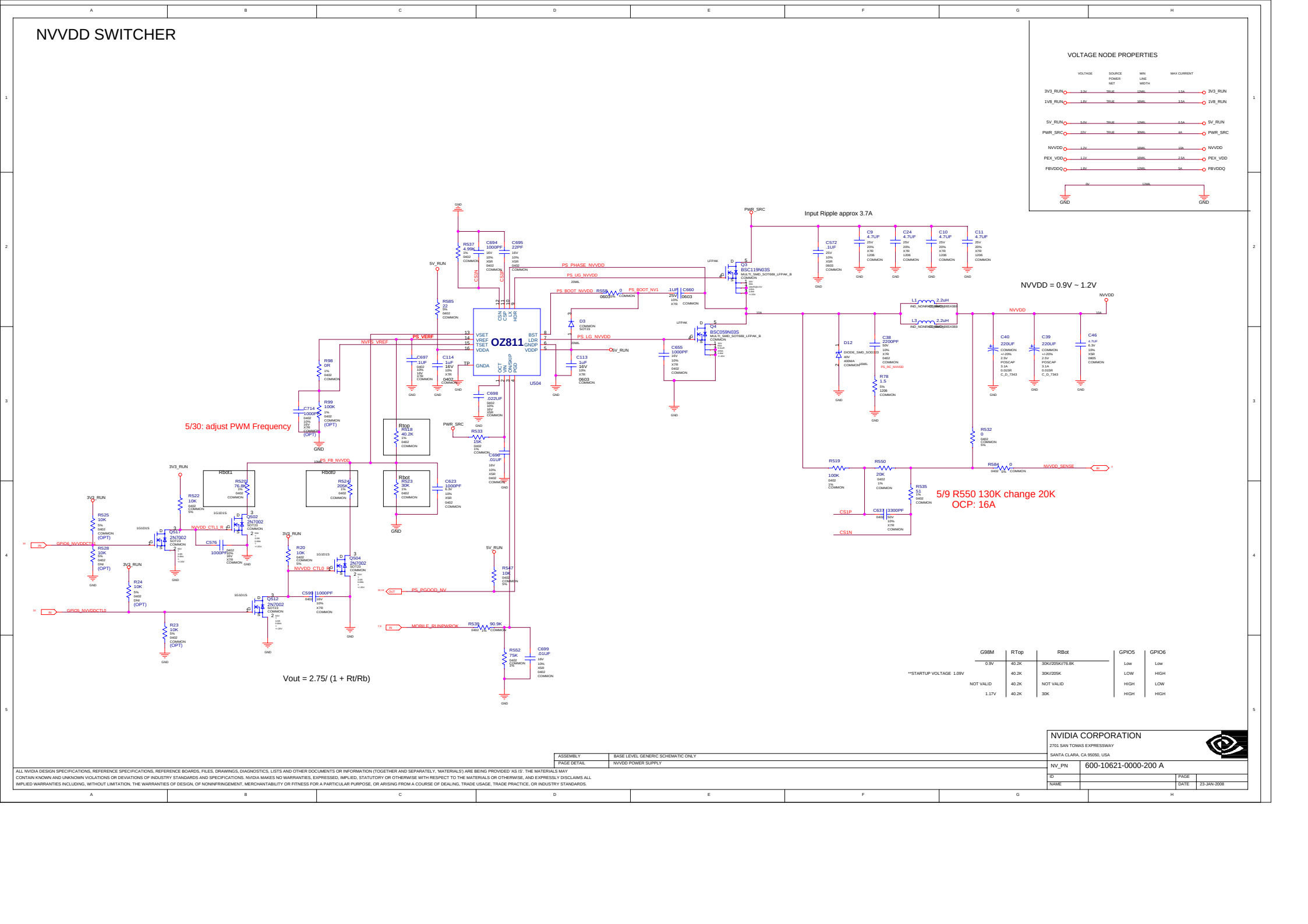
# NVVDD SWITCHER




| G98M | RTop | RBot | GPIO5 | GPIO6 |
|---|---|---|---|---|
| 0.9V | 40.2K | 30K//205K//76.8K | Low | Low |
| | 40.2K | 30K//205K | LOW | HIGH |
| NOT VALID | 40.2K | NOT VALID | HIGH | LOW |
| 1.17V | 40.2K | 30K | HIGH | HIGH |

| | |
|---|---|
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| PAGE DETAIL | NVVDD POWER SUPPLY |

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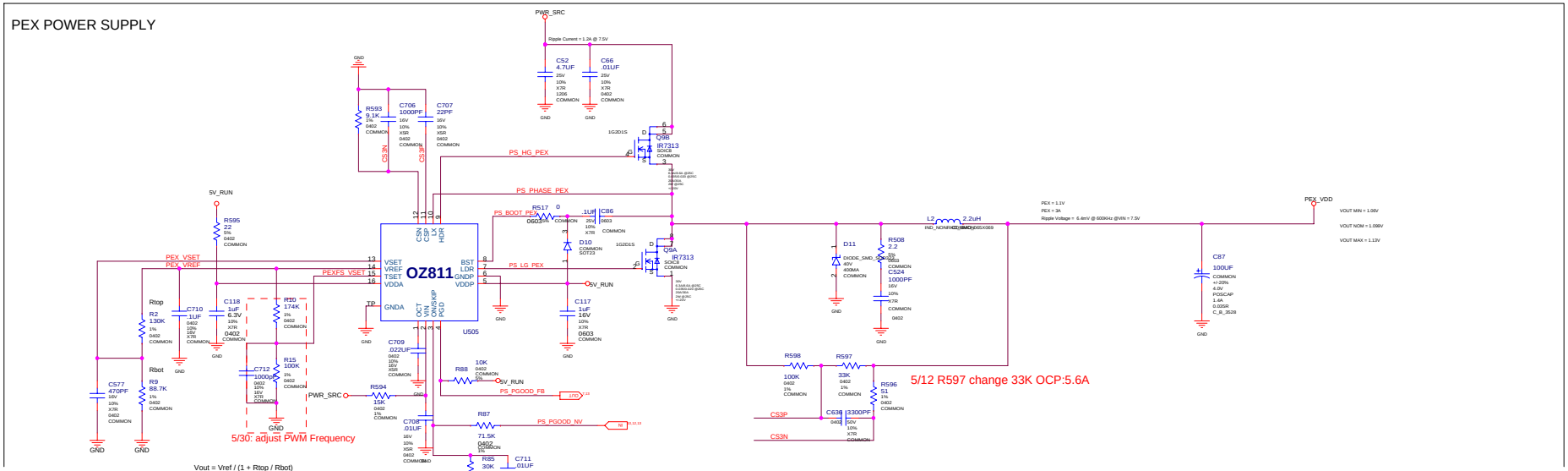
# FBVDDQ & PEX Power Supplies

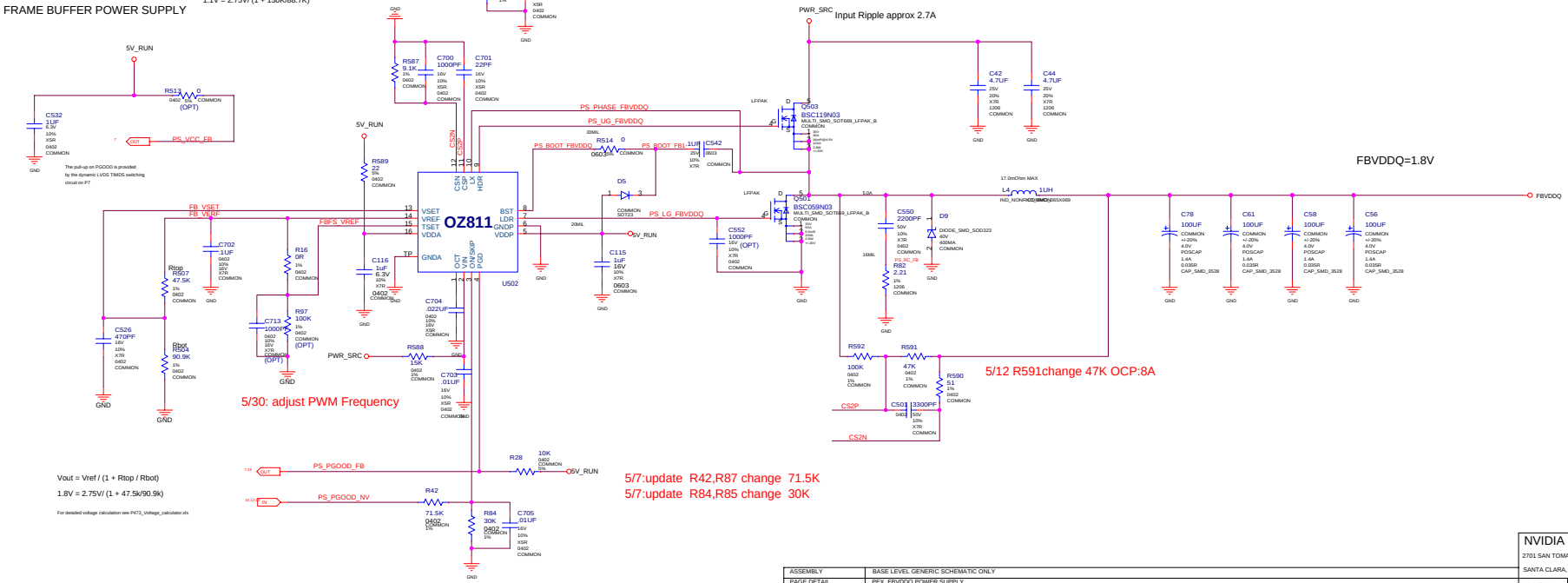
## PEX POWER SUPPLY




Vout = Vref / (1 + Rtop / Rbot)

1.1V = 2.75V/ (1 + 130K/88.7K)

## FRAME BUFFER POWER SUPPLY




Vout = Vref / (1 + Rtop / Rbot)

1.8V = 2.75V/ (1 + 47.5k/90.9k)

| | |
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| PAGE DETAIL | PEX, FBVDDQ POWER SUPPLY |

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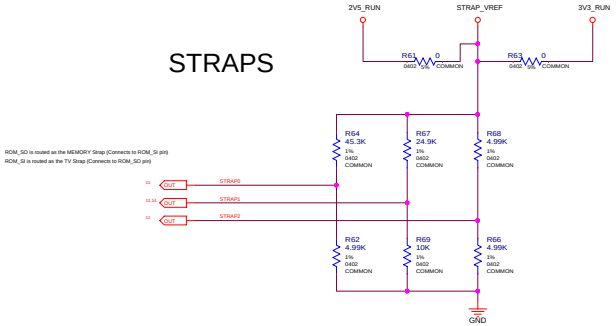
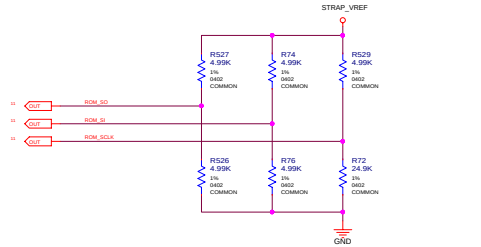
# STRAPS



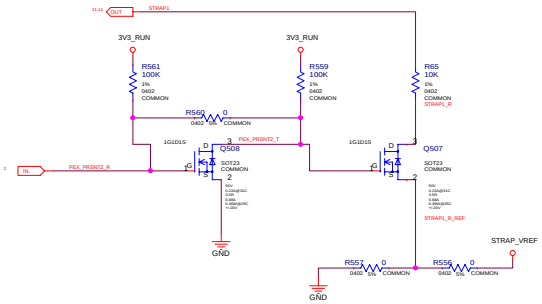




| | | | |
|---|---|---|---|
| STRAP0 | USER_BIT0 | 0xF: 45K PU (unused) | |
| | USER_BIT1 | | |
| | USER_BIT2 | | |
| | USER_BIT3 | | |
| STRAP1 | 3GIO_PADCFG_LUT_ADR0 | | |
| | 3GIO_PADCFG_LUT_ADR1 | 0x0: Desktop default (normal swing) - 5k PD | |
| | 3GIO_PADCFG_LUT_ADR2 | 0x1: Mobile default (low swing) - 10k PD | |
| | 3GIO_PADCFG_LUT_ADR3 | acc. to //hw/tesla_g98b/manuals/dev_ext_devices.ref | |
| STRAP2 | PCI_DEVID_0 | all 4 bits set by HW strapping | |
| | PCI_DEVID_1 | 0x06E8: 5K PU (NB9M-GE) | |
| | PCI_DEVID_2 | 0x06E9: 10K PU (NB9M-GS) | |
| | PCI_DEVID_3 | | |
| ROM_SO | TV_MODE_BIT0 | 0x0: NTSC-M | |
| | TV_MODE_BIT1 | | 5K PU |
| | TV_MODE_BIT2 | | |
| | XCLK_277 | 1: | |

| | | 128 MB (4pcs. 16Mx16) | | 256 MB (4pcs. 32Mx16) | |
|---|---|---|---|---|---|
| ROM_SI | RAM_CFG_0 | RAM_CFG[3:0] | Definitions | RAM_CFG[3:0] | Definitions |
| | RAM_CFG_1 | 0000 | Elpida | 0100 | 25k PD Elpida |
| | RAM_CFG_2 | 0001 | Samsung | 0101 | 30k PD Samsung |
| | RAM_CFG_3 | 0010 | Qimonda | 0110 | 35k PD Qimonda |
| | | 0011 | Hynix | 0111 | 45k PD Hynix |
| | | 0100 | Nanya | | |

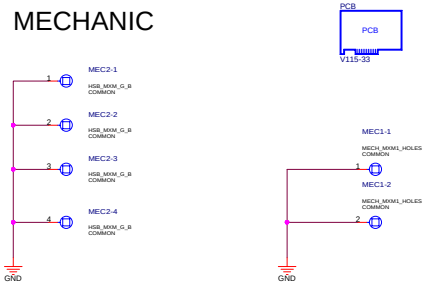
| | | | |
|---|---|---|---|
| ROM_SCLK | PCI_DEVID_EXT | 0: | |
| | SUB_VENDOR | 1: SUB_VENDOR BIOS | 25K PD |
| | SLOT_CLK_CONFIG | 0: | |
| | PEX_PLL_EN_TERM100 | 0: TERM100 DISABLED | |

# PEX SWING LEVEL




| | | |
|---|---|---|
| PEX_PRSNT2_R | R_STRAP1 | 3_GIO_PADCFG_LUT<3..0> |
| GND | 10k | 0x1 MOBILE_DEFAULT |
| FLOAT | 5k (10k ll 10k) | 0x0 DESKTOP_DEFAULT |

# MECHANIC

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Title: Basenet Report
Design: p621
Date: Dec 11 12:08:17 2007

Base nets and synonyms for
p621_lib.P621(@p621_lib.p621(sch_1))
Base Signal Location([Zone][dir])

DACA_BLUE 6.1G> 6.4G 9.3A<
DACA_GREEN 6.1G> 6.4G 9.3A<
DACA_HSYNC 6.1G> 9.3A<
DACA_RED 6.1G> 6.3G 9.3A<
DACA_RSET 6.1C
DACA_VDD 6.1C
DACA_VREF 6.1C
DACA_VSYNC 6.1G> 9.3A<
DACB_BLUE 6.3G> 6.4F 9.3A<
DACB_GREEN 6.3G> 6.4F 9.2A<
DACB_RED 6.3F 6.3G> 9.3A<
DACB_RSET 6.2C
DACB_VDD 6.2C
DACB_VREF 6.2C
DACC_VDD 6.4C
DP_AUXG 8.2E 8.5D<>
DP_AUXG* 8.2E 8.5D<>
DP_AUXG_R 8.1E 8.5D<>
DP_AUXG_R* 8.1E 8.5D<>
DP_AUXT 8.1E 8.5F<>
DP_AUXT* 8.1E 8.5F<>
DP_AUX_C 8.2G> 8.5F<> 9.3C<>
DP_AUX_C* 8.2G> 8.5F<> 9.3C<>
DP_L0 8.2E 8.5D<>
DP_L0* 8.2E 8.5D<>
DP_L0_C 8.2F> 8.5F<> 9.2F<
DP_L0_C* 8.2F> 8.5F<> 9.2F<
DP_L1 8.2E 8.5D<>
DP_L1* 8.2E 8.5D<>
DP_L1_C 8.2F> 8.5F<> 9.2F<
DP_L1_C* 8.2F> 8.5F<> 9.2F<
DP_L2 8.2E 8.5D<>
DP_L2* 8.2E 8.5D<>
DP_L2_C 8.2F> 8.5F<> 9.3F<
DP_L2_C* 8.2F> 8.5F<> 9.2F<
DP_L3 8.2E 8.5D<>
DP_L3* 8.2E 8.5D<>
DP_L3_C 8.2F> 8.5F<> 9.3F<
DP_L3_C* 8.2F> 8.5F<> 9.3F<
FBA_CLK0 3.3E> 4.2A 4.2E 4.3G< 4.5A<
FBA_CLK0* 3.3E> 4.2A 4.2E 4.3G< 4.5A<
FBA_CLK0_TERM 4.3G
FBA_CLK1 3.3E> 5.2A 5.2E 5.4G< 5.5A<
FBA_CLK1* 3.3E> 5.2A 5.2E 5.4G< 5.5A<
FBA_CLK1_TERM 5.3G
FBA_CMD<0> 3.2E 4.1A 4.1E
FBA_CMD<27..0> 3.2F> 4.1A< 4.5A< 5.1A< 5.5A<
FBA_CMD<1> 3.2E 4.1A 4.1E 5.1A 5.1E
FBA_CMD<2> 3.2E 4.1A 4.1E
FBA_CMD<3> 3.2E 4.1A 4.1E 5.1A 5.1E
FBA_CMD<4> 3.2E 5.1A 5.1E
FBA_CMD<5> 3.2E 5.1A 5.1E
FBA_CMD<6> 3.2E 5.1A 5.1E
FBA_CMD<8> 3.2E 4.1A 4.1E 5.1A 5.1E
FBA_CMD<9> 3.2E 4.1A 4.1E 5.1A 5.1E
FBA_CMD<10> 3.2E 4.2A 4.2E 5.2A 5.2E
FBA_CMD<11> 3.2E 3.2F 4.2A 4.2E 5.2A 5.2E
FBA_CMD<12> 3.3E 3.3F 4.2A 4.2E 5.2A 5.2E
FBA_CMD<13> 3.3E 5.1A 5.1E
FBA_CMD<14> 3.3E 4.2A 4.2E 5.2A 5.2E
FBA_CMD<15> 3.3E 4.1A 4.1E 5.1A 5.1E
FBA_CMD<16> 3.3E 4.2A 4.2E 5.2A 5.2E
FBA_CMD<17> 3.3E 4.2A 4.2E 5.2A 5.2E
FBA_CMD<18> 3.3E 4.2A 4.2E 5.2A 5.2E
FBA_CMD<19> 3.3E 4.2A 4.2E 5.2A 5.2E
FBA_CMD<20> 3.3E 4.2A 4.2E 5.2A 5.2E
FBA_CMD<21> 3.3E 4.1A 4.1E 5.2A 5.2E
FBA_CMD<22> 3.3E 4.1A 4.1E
FBA_CMD<23> 3.3E 4.2A 4.2E 5.2A 5.2E
FBA_CMD<24> 3.3E 4.1A 4.1E
FBA_CMD<25> 3.3E 4.1A 4.1E 5.1A 5.1E
FBA_CMD<27> 3.3E 4.2A 4.2E 5.2A 5.2E
FBA_D<0> 3.1C 4.3B
FBA_D<31..0> 4.3A<> 4.5A<> 3.1C<>
FBA_D<63..0> 3.1C<> 5.3A<> 5.5A<>
FBA_D<1> 3.1C 4.3B
FBA_D<2> 3.1C 4.3B
FBA_D<3> 3.1C 4.3B
FBA_D<4> 3.1C 4.3B
FBA_D<5> 3.1C 4.3B
FBA_D<6> 3.1C 4.3B
FBA_D<7> 3.1C 4.3B
FBA_D<8> 3.1C 4.3C
FBA_D<9> 3.1C 4.3C
FBA_D<10> 3.1C 4.3C
FBA_D<11> 3.1C 4.3C
FBA_D<12> 3.1C 4.3C
FBA_D<13> 3.1C 4.3C
FBA_D<14> 3.1C 4.3C
FBA_D<15> 3.1C 4.3C
FBA_D<16> 3.1C 4.3D
FBA_D<17> 3.1C 4.3D
FBA_D<18> 3.1C 4.3D
FBA_D<19> 3.1C 4.3D
FBA_D<20> 3.1C 4.3D
FBA_D<21> 3.2C 4.3D
FBA_D<22> 3.2C 4.3D
FBA_D<23> 3.2C 4.3D
FBA_D<24> 3.2C 4.3D
FBA_D<25> 3.2C 4.3D
FBA_D<26> 3.2C 4.3D
FBA_D<27> 3.2C 4.3D
FBA_D<28> 3.2C 4.3D
FBA_D<29> 3.2C 4.3D
FBA_D<30> 3.2C 4.3D
FBA_D<31> 3.2C 4.3D
FBA_D<32> 3.2C 5.3B
FBA_D<63..32> 3.1C<> 5.3A<> 5.5A<>
FBA_D<33> 3.2C 5.3B
FBA_D<34> 3.2C 5.3B
FBA_D<35> 3.2C 5.3B
FBA_D<36> 3.2C 5.3B
FBA_D<37> 3.2C 5.3B
FBA_D<38> 3.2C 5.3B
FBA_D<39> 3.2C 5.3B
FBA_D<40> 3.2C 5.3C
FBA_D<41> 3.2C 5.3C
FBA_D<42> 3.2C 5.3C
FBA_D<43> 3.2C 5.3C
FBA_D<44> 3.2C 5.3C
FBA_D<45> 3.2C 5.3C
FBA_D<46> 3.2C 5.3C
FBA_D<47> 3.2C 5.3C
FBA_D<48> 3.2C 5.3D
FBA_D<49> 3.2C 5.3D
FBA_D<50> 3.2C 5.3D
FBA_D<51> 3.2C 5.3D
FBA_D<52> 3.3C 5.3D
FBA_D<53> 3.3C 5.3D
FBA_D<54> 3.3C 5.3D
FBA_D<55> 3.3C 5.3D
FBA_D<56> 3.3C 5.3E
FBA_D<57> 3.3C 5.3E
FBA_D<58> 3.3C 5.3E
FBA_D<59> 3.3C 5.3E
FBA_D<60> 3.3C 5.3E
FBA_D<61> 3.3C 5.3E
FBA_D<62> 3.3C 5.3E
FBA_D<63> 3.3C 5.3E
FBA_DEBUG 3.4E
FBA_DQM<0> 3.3C 4.4B
FBA_DQM<3..0> 4.3A<> 4.5A<> 3.3C<>
FBA_DQM<7..0> 3.3C<> 5.3A<> 5.5A<>
FBA_DQM<1> 3.3C 4.4C
FBA_DQM<2> 3.3C 4.4D
FBA_DQM<3> 3.3C 4.4D
FBA_DQM<4> 3.3C 5.4B
FBA_DQM<7..4> 3.3C<> 5.3A<> 5.5A<>
FBA_DQM<5> 3.3C 5.4C
FBA_DQM<6> 3.3C 5.4D
FBA_DQM<7> 3.3C 5.4E
FBA_DQS_RN0 3.4C<> 4.4B 4.5A<
FBA_DQS_RN1 3.4C<> 4.4C 4.5A<
FBA_DQS_RN2 3.4C<> 4.4D 4.5A<
FBA_DQS_RN3 3.4C<> 4.4D 4.5A<
FBA_DQS_RN4 3.4C<> 5.4B 5.5A<
FBA_DQS_RN5 3.4C<> 5.4C 5.5A<
FBA_DQS_RN6 3.4C<> 5.4D 5.5A<
FBA_DQS_RN7 3.4C<> 5.4E 5.5A<
FBA_DQS_WP0 3.3C<> 4.4B 4.5A<
FBA_DQS_WP1 3.3C<> 4.4C 4.5A<
FBA_DQS_WP2 3.3C<> 4.4D 4.5A<
FBA_DQS_WP3 3.3C<> 4.4D 4.5A<
FBA_DQS_WP4 3.4C<> 5.4B 5.5A<
FBA_DQS_WP5 3.4C<> 5.4C 5.5A<
FBA_DQS_WP6 3.4C<> 5.4D 5.5A<
FBA_DQS_WP7 3.4C<> 5.4E 5.5A<
FBA_VREF1 4.2C 4.2F 4.4A<>
FBA_VREF2 5.2B 5.2F 5.4A<>
FB_CAL_PD_VDDQ 3.1A<> 3.4E
FB_CAL_PU_GND 3.2A<> 3.4E
FB_CAL_TERM_GND 3.2A<> 3.4E
FB_PLLAVDD 3.2A<> 3.4E
FB_VREF 3.2A<> 3.5C
GND_SENSE 2.4F
GPIO1_DP_HPDC 10.3D
GPIO2_BL_PWM 9.4A< 10.3F>
GPIO3_PPEN 9.3A< 10.3F>
GPIO3_PPEN_GPU 10.3D
GPIO4_BLEN 9.3A< 10.3F>
GPIO4_BLEN_GPU 10.3D
GPIO5_NVVDDCTL0 10.3F> 12.4A<
GPIO6_NVVDDCTL1 10.3F> 12.4A<
GPIO8_SLOWDOWNM* 10.2D
GPIO8_THERM_ALERT* 10.3D
GPIO9_LVDS_SYS* 7.2A< 10.3E>
GPIO9_TMDS_IOVDD_E 7.2B
N*
GPIO12_AC_DET 10.3D
GPIO15_DVI_A_HPDE 10.3D
GPIO16_MODE_C 8.1G< 10.3E<
GPIO16_MODE_C* 8.1F
GPU_TESTMODE 11.2C
HDA1_BCLK 7.5D<>
HDA1_RST* 7.5D<>
HDA1_SDI 7.4F 7.5D<>
HDA1_SDO 7.5D<>
HDA1_SYNC 7.5D<>
HDA_BCLK 7.4H< 7.5D<> 9.4C>
HDA_RST* 7.4H< 7.5D<> 9.4C>
HDA_SDI 7.4H< 7.5D<> 9.4C>
HDA_SDO 7.4H> 7.5D<> 9.4C>
HDA_SYNC 7.4H< 7.5D<> 9.4C>
I2CA_SCL 10.2D
I2CA_SCL_R 9.3A< 10.2H>
I2CA_SDA 10.2D
I2CA_SDA_R 9.3A<> 10.2H<>
I2CB_SCL 10.2D
I2CB_SCL_R 9.2A< 10.3H>
I2CB_SDA 10.3D
I2CB_SDA_R 9.2A<> 10.3H<>
I2CC_SCL 10.3D
I2CC_SCL_R 9.4A< 10.2A< 10.3H> 11.5E<
I2CC_SDA 10.3D
I2CC_SDA_R 9.4A<> 10.2A<> 10.3H<> 11.5E<>
I2CD_SCL 8.1G<> 10.3H>
I2CD_SDA 8.1G<> 10.3H>
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I2CH_SDA 11.2C
I2CS_SCL 10.3C
I2CS_SDA 10.3C
IFPAB_IOVDD 7.2F
IFPAB_IOVDD_3V3 7.3B
IFPAB_IOVDD_EN* 7.3B
IFPAB_IOVDD_LVDS_I 7.2B
SOL
IFPAB_IOVDD_SW 7.2C
IFPAB_PLLVDD 7.1F
IFPAB_RSET 7.1F
IFPA_TXC 7.2H> 7.5B<> 9.4F<
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IFPE_L3 8.3E 8.5B<>
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IFPE_RSET 8.3C
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JTAG_TCLK 10.3C
JTAG_TDI 10.3C
JTAG_TDO 10.3C
JTAG_TMS 10.3C
JTAG_TRST 10.3C
MOBILE_AC_BATT 9.4B> 10.3E<
MOBILE_RUNPWROK 7.3A< 9.4A> 12.2A<
MOBILE_RUNPWROK_IN 9.4B
NVVDD 12.2F
NVVDD_CTL0 12.4C
NVVDD_CTL0_R 12.4C
NVVDD_CTL1 12.4C
NVVDD_CTL1_R 12.4C
NVVDD_SENSE 2.4G<> 12.3E<>
PEX_PLLVDD 2.4F
PEX_PRSNT2 2.5C
PEX_PRSNT2_R 2.5D> 14.4A<
PEX_PRSNT2_T 14.4B
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PEX_REFCLK* 2.2E
PEX_RST 2.2D
PEX_RX0 2.2E
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PEX_TCLK* 2.5F
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PEX_TX0_C* 2.2C
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PEX_TX1_C* 2.2C
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PEX_TX7_C* 2.3C
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PEX_TX8_C 2.3C
PEX_TX8_C* 2.3C
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PEX_TX11_C 2.4C
PEX_TX11_C* 2.4C
PEX_TX12 2.4E
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PEX_TX13_C 2.4C
PEX_TX13_C* 2.4C
PEX_TX14 2.5E
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PEX_TX14_C 2.5C
PEX_TX14_C* 2.5C
PEX_TX15 2.5E
PEX_TX15* 2.5E
PEX_TX15_C 2.5C
PEX_TX15_C* 2.5C
PS_BOOT_FB1 13.3C
PS_BOOT_FBVDDQ 13.3C
PS_BOOT_NV1 12.2C
PS_BOOT_NVVDD 12.2C
PS_BOOT_PEX 13.2C
PS_CP_FB1 13.5B
PS_CP_FB2 13.4B
PS_CP_FB3 13.4E
PS_CP_NVVDD1 12.3B
PS_CP_NVVDD2 12.3B
PS_CP_NVVDD3 12.3D
PS_DR_FBFCCM 13.4B
PS_DR_NVFCCM 12.2B
PS_FB_FB 13.4C
PS_FB_NVVDD 12.4D
PS_FB_PEX 13.3C
PS_FS_FB 13.4B
PS_FS_NVVDD 12.3B
PS_ISEN_FBVDDQ 13.4C
PS_ISEN_NVVDD 12.2C
PS_LG_FBVDDQ 13.4C
PS_LG_NVVDD 12.2C
PS_LG_PEX 13.2C
PS_PGOOD_FB 7.1A< 13.2A> 13.4A>
PS_PGOOD_NV 10.2F< 12.2A> 13.2A< 13.4A<
PS_PHASE_FBVDDQ 13.4C
PS_PHASE_NVVDD 12.2C
PS_PHASE_PEX 13.2C
PS_RC_FB 13.4D
PS_RC_NVVDD 12.3E
PS_RC_PEX 13.2E
PS_UG_FBVDDQ 13.3C
PS_UG_NVVDD 12.2C
PS_VCC_FB 7.1A< 13.4A>
PS_VCC_NVVDD 12.2B
ROM_CS* 11.1C 11.1D
ROM_SCLK 11.1D< 11.1D< 14.3A>
ROM_SI 11.1D< 11.1D< 14.3A>
ROM_SO 11.1D< 11.1D< 14.3A>
SMB_CLK 9.4A> 10.4B<
SMB_DATA 9.4A<> 10.4B<>
SNN_A13_1 4.2B
SNN_A13_2 4.2E
SNN_A13_3 5.2A
SNN_A13_4 5.2E
SNN_A14_1 4.2B
SNN_A14_2 4.2E
SNN_A14_3 5.2A
SNN_A14_4 5.2E
SNN_A15_1 4.2B
SNN_A15_2 4.2E
SNN_A15_3 5.2A
SNN_A15_4 5.2E
SNN_BUFRST* 11.2C
SNN_CN1_200 9.3C
SNN_DACB_CSYNC 6.3D
SNN_DACC_BLUE 6.4D
SNN_DACC_GREEN 6.4D
SNN_DACC_HSYNC 6.4D
SNN_DACC_RED 6.4D
SNN_DACC_RSET 6.4C
SNN_DACC_VREF 6.4C
SNN_DACC_VSYNC 6.4D
SNN_DPB_165 9.3E
SNN_DPB_167 9.3E
SNN_DPB_177 9.3E
SNN_DPB_179 9.3E
SNN_DPB_183 9.3E
SNN_DPB_185 9.3E
SNN_DPB_195 9.3E
SNN_DPB_197 9.3E
SNN_FBA_CMD7 3.2E
SNN_FBA_CMND26 3.3E
SNN_FBA_CMND28 3.3E
SNN_FBA_NC1 4.2A
SNN_FBA_NC2 4.2A
SNN_FBA_NC3 4.2E
SNN_FBA_NC4 4.2E
SNN_FBA_NC5 5.2A
SNN_FBA_NC6 5.2A
SNN_FBA_NC7 5.2E
SNN_FBA_NC8 5.2E
SNN_FBA_RFU_1 3.3E
SNN_FBA_RFU_2 3.3E
SNN_GPIO7 10.3D
SNN_GPIO10 10.3D
SNN_GPIO11 10.3D
SNN_GPIO13 10.3D
SNN_GPIO14 10.3D
SNN_GPIO17_CEC_DET 10.3D_C
SNN_GPIO18_MODE_E 10.4D
SNN_GPIO19_CEC_DET 10.4D_E
SNN_I2CE_SCL 10.3D
SNN_I2CE_SDA 10.3D
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SNN_IFPE_AUX* 8.3E
SNN_NC1 11.1H
SNN_NC2 11.1H
SNN_NC3 11.1H
SNN_NC4 11.1H
SNN_PEX_NC 13.2B
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SNN_RFU_AG9 2.5F
SNN_RFU_C15 11.2A
SNN_RFU_D15 11.2A
SNN_RFU_F6 11.2C
SNN_RFU_J5 11.2C
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SPDIF_MXM 9.4C
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SP_REF 11.5D
SP_VDD 11.5C
STRAP0 11.1A< 14.1A>
STRAP1 11.1A< 14.1A> 14.4A>
STRAP1_R 14.4C
STRAP1_R_REF 14.4C
STRAP2 11.1A< 14.2A>
STRAP_REF_3V3 11.2A
STRAP_REF_MIOB 11.2A
THERM 10.3C
THERM* 10.2C
THERM_ALERT* 9.4A< 10.2G>
THERM_ALERTM* 10.2D
THERM_SCL 10.2C
THERM_SDA 10.2C
THERM_VDD 10.2D
XTALIN 11.4C
XTALOUT 11.4E
XTALOUT_BUF 11.4E
XTALOUT_BUF_R 11.5D
XTAL_PLLVDD 11.3C
XTAL_SSFOUT 11.4C

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