NV28M-P138, DAC, TMDS, LVDS, TVout, 32/64MB 4MX32 BGA DDR, AGP4X, Dell

X00

1. Schematics taken from E153-A00.

X17

1. Use RUNPWRGD for all PS enabling.

A01:

1. Corrected serial ROM hookup.

A02:

- X42 Corrected I2C2 hookup at U9 (CH7009).
- 2. Changed R254 to 1.5K 1%. This raises NVVDD to 1.25V.

NVVDD to 1.25V.
3. Connect GPIO1 to 90C387 PD, and disconnect SUS_STAT- from motherboard.
4. Change Q2 to FDS6982.

Change R287 to 2.67K and R254 to 1.1K when NVVDDSW stuff option is employed, with R254 = 1.5K when no NVVDDSW is used (NOSW stuff option).

6. Removed TP606 to allow better guard trace on thermal sensor D+ and D- lines.

Connected CH_GPIO0 to NSM_DUAL to select single or dual link panels.

A03:

X00

- 1. Add r989, r990, r991, r992 to pull up I2C
- 2. Change c82 and c84 into small package to fit into new mechanical requirement.
- 3. Change r44 from pull-up to pull-up to ground.
- 4. Chang c60 and c61 to 47pF fot TVout issue.

1. Change r287 to 4.02k; r254 to 1.21k.

A04:

X00

1. Change Mem vendor strapping option

X01

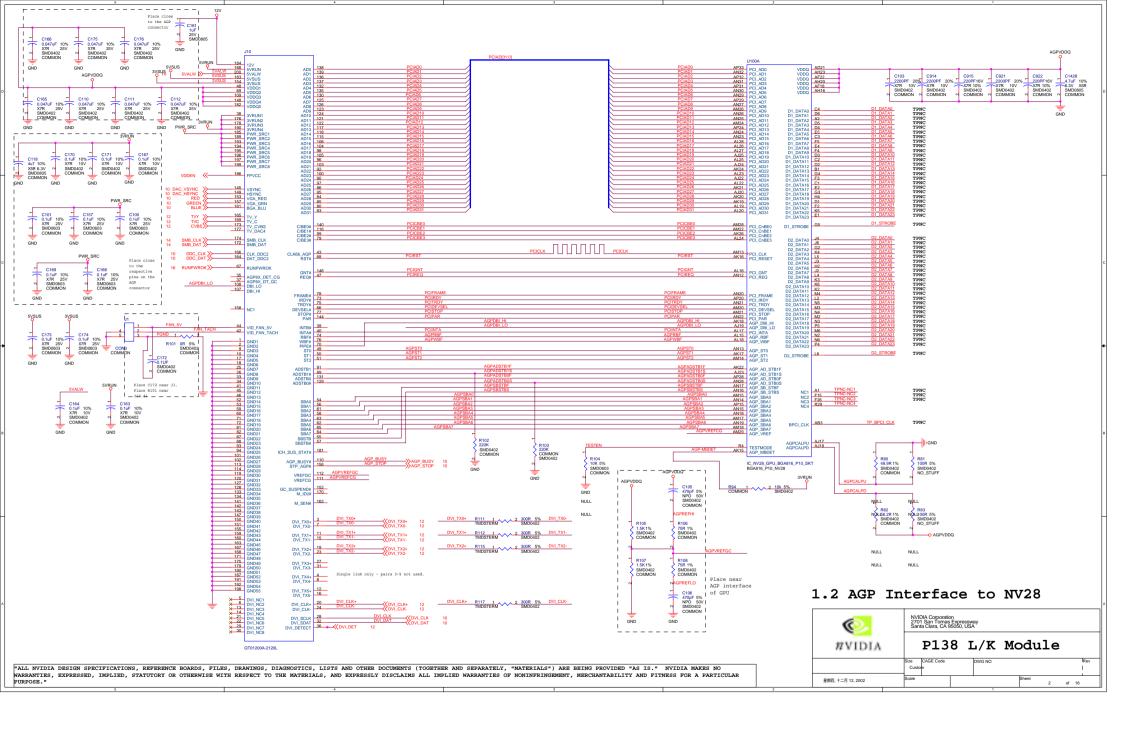
- 1. In P.13, rework to prevent LCDVCC backdrive. Connect L12.2 directly to C32.1 instead of 3.3NSM.
- 2. In P.14, rework to prevent LCDVCC glich. Use resistive load $\,$ n-fet as an inverter driven by 3VRUN instead of 5VRUN.
- 3. Change CH7009 to CH7009B and connect U9.9 (HPDET) to J10.36 (DVI DET)

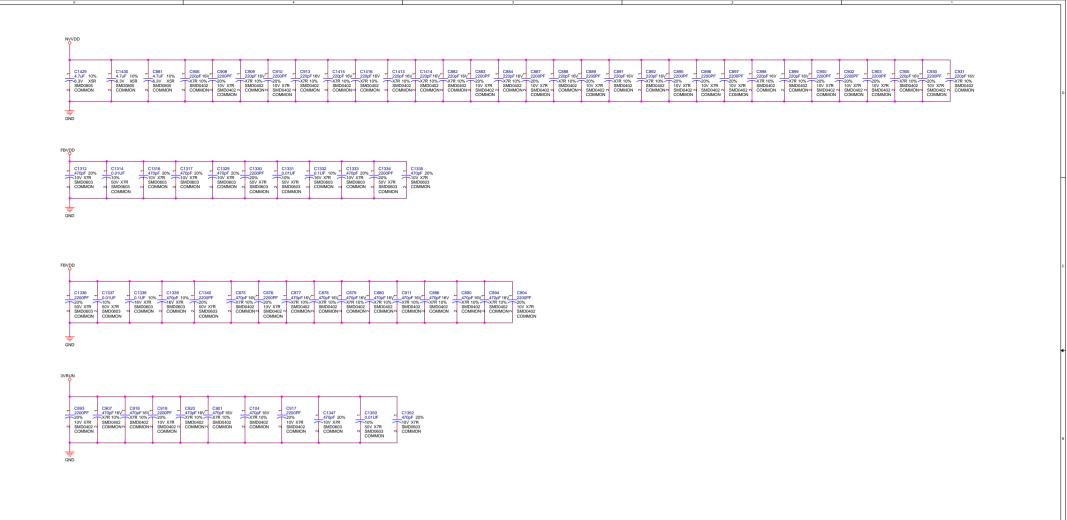
1.1 TOP PAGE

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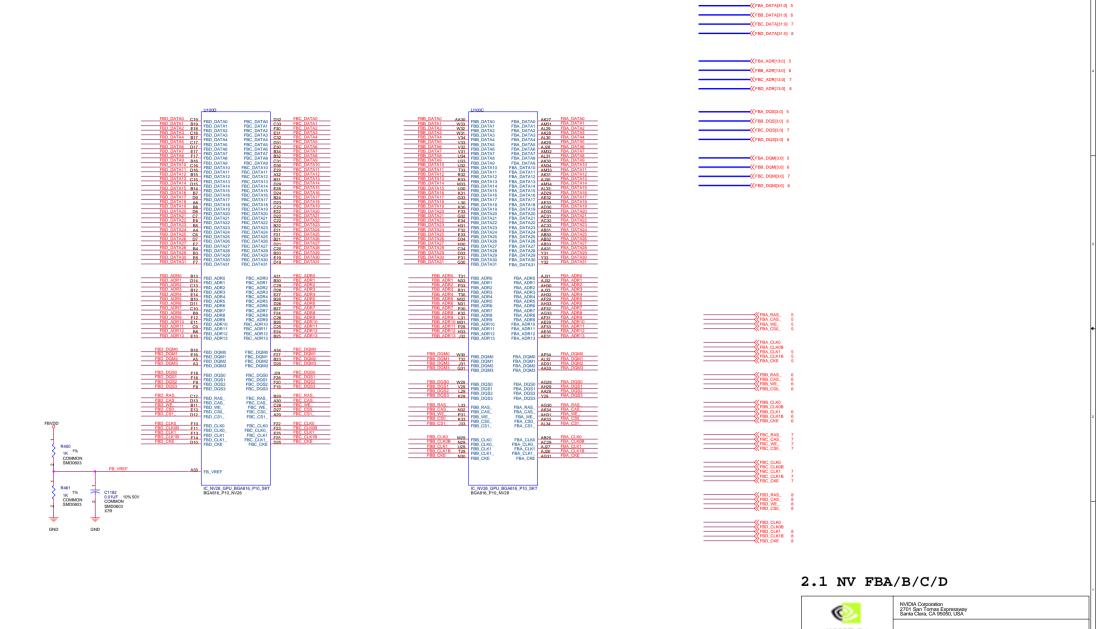


2.0 NV DECOUPLING

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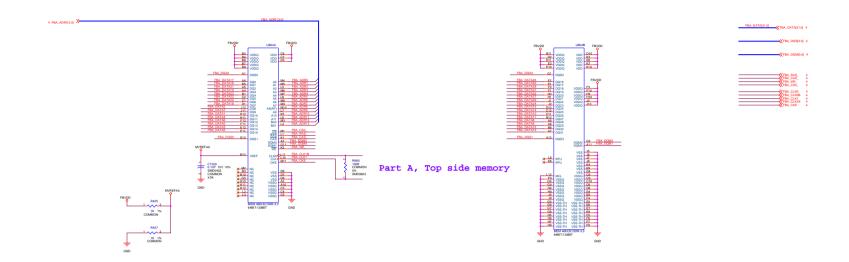
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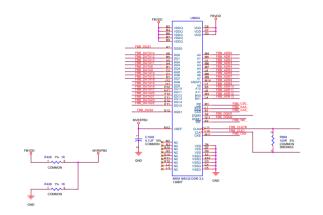
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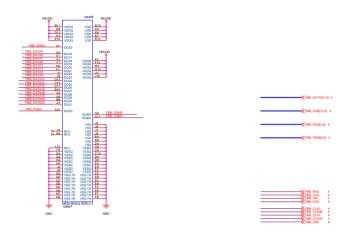


2.2 FBA DDR 4MX32 SDRAM

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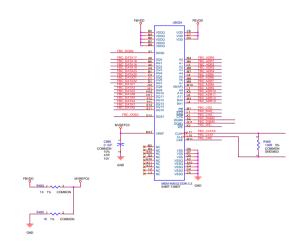


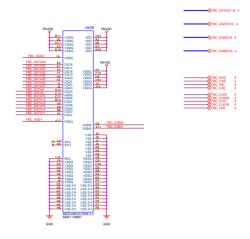


2.3 FBB DDR 4MX32 SDRAM

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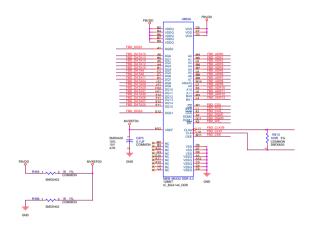


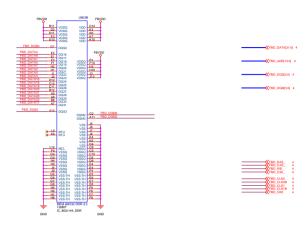


2.4 FBC DDR 4MX32 SDRAM

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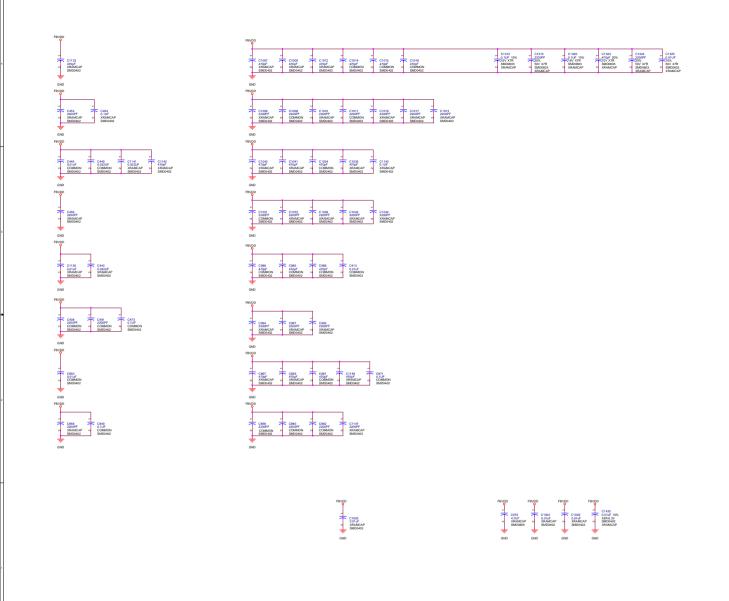




2.5 FBD DDR 4MX32 SDRAM

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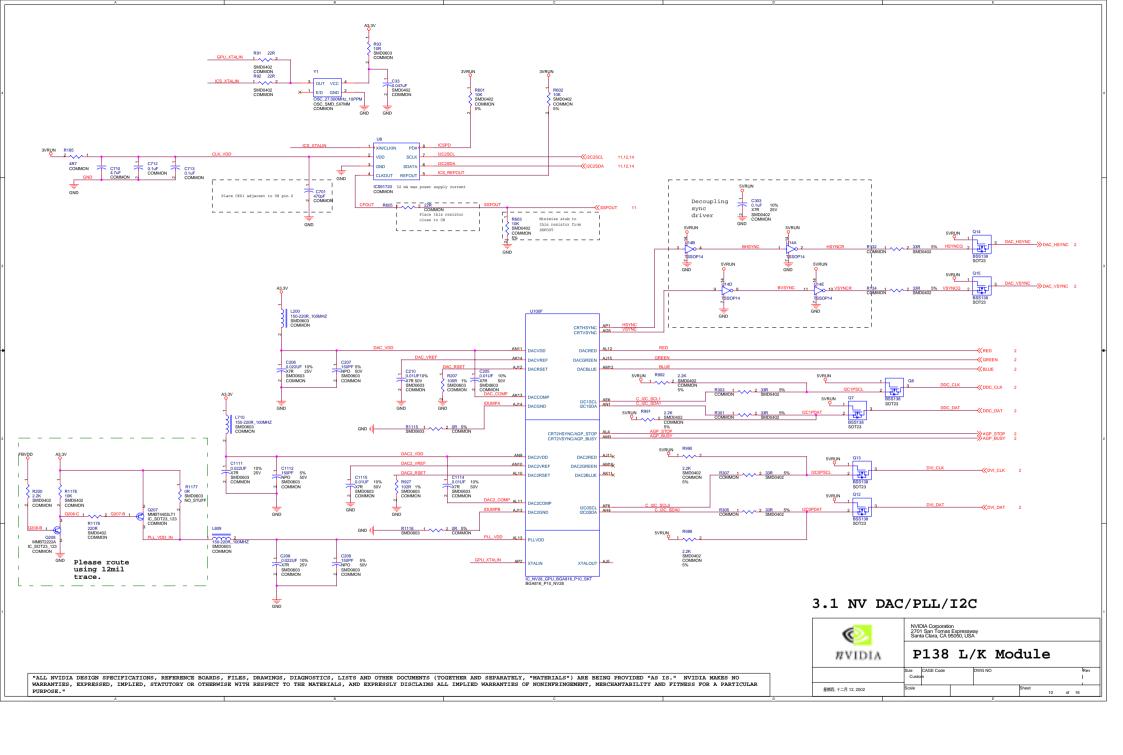
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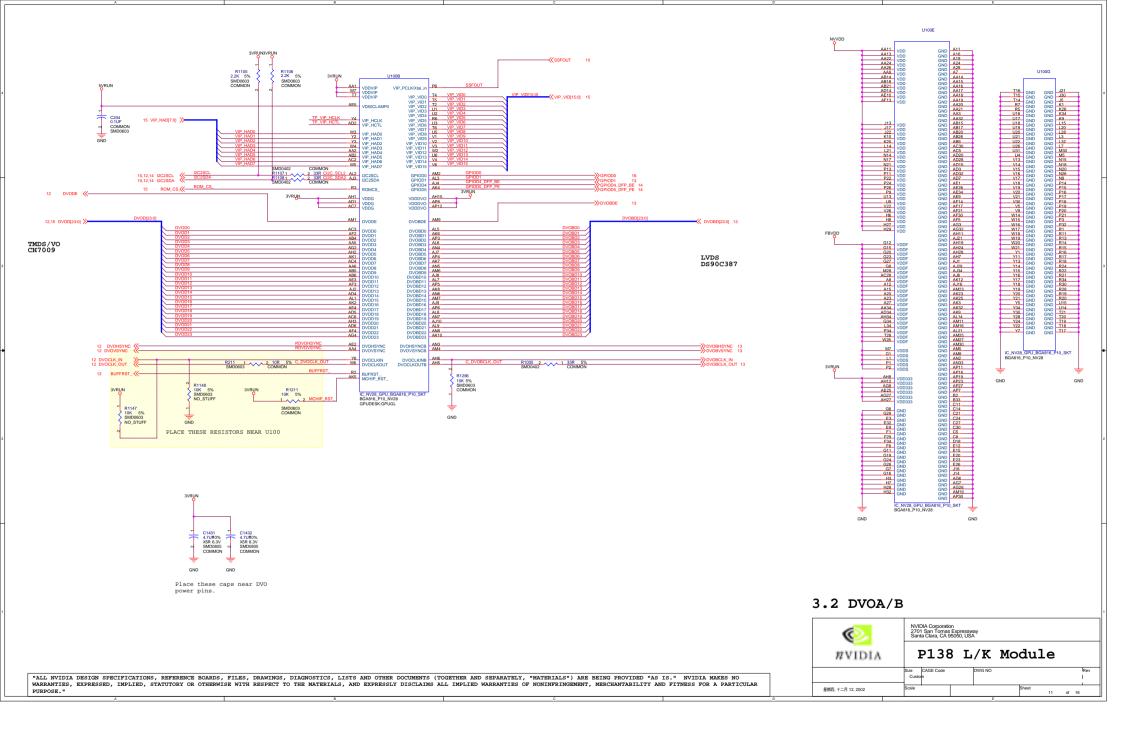


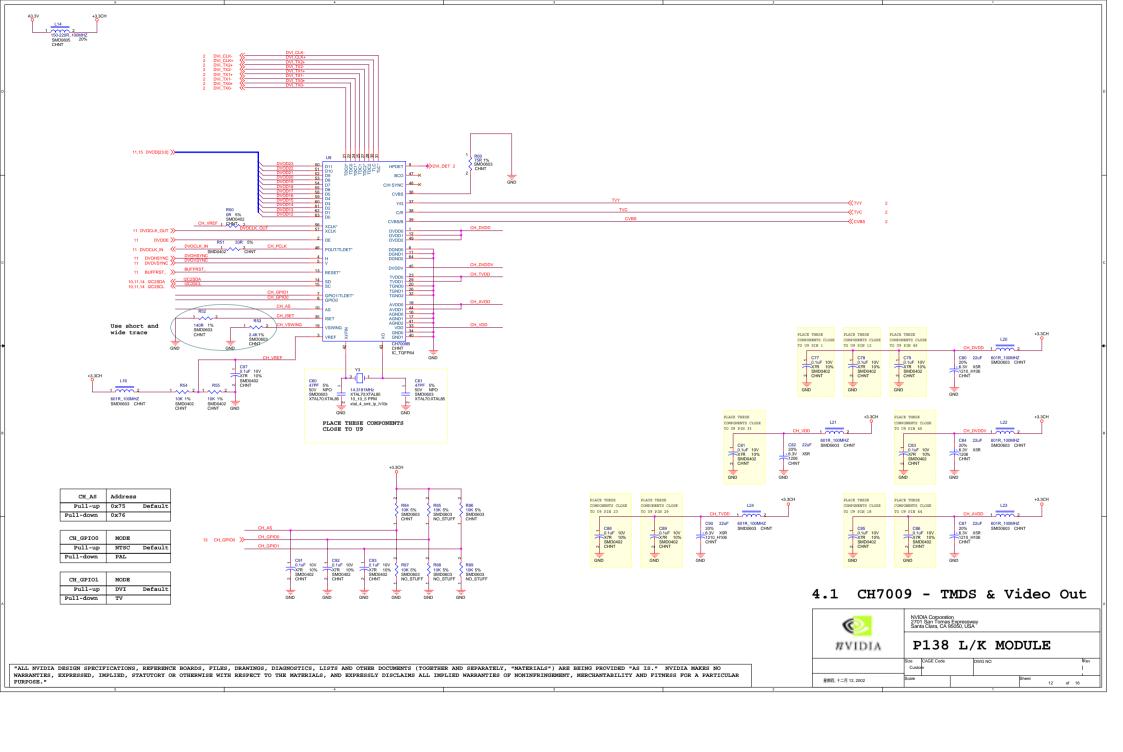
2.6 BGA MEMORY DECOUPLING

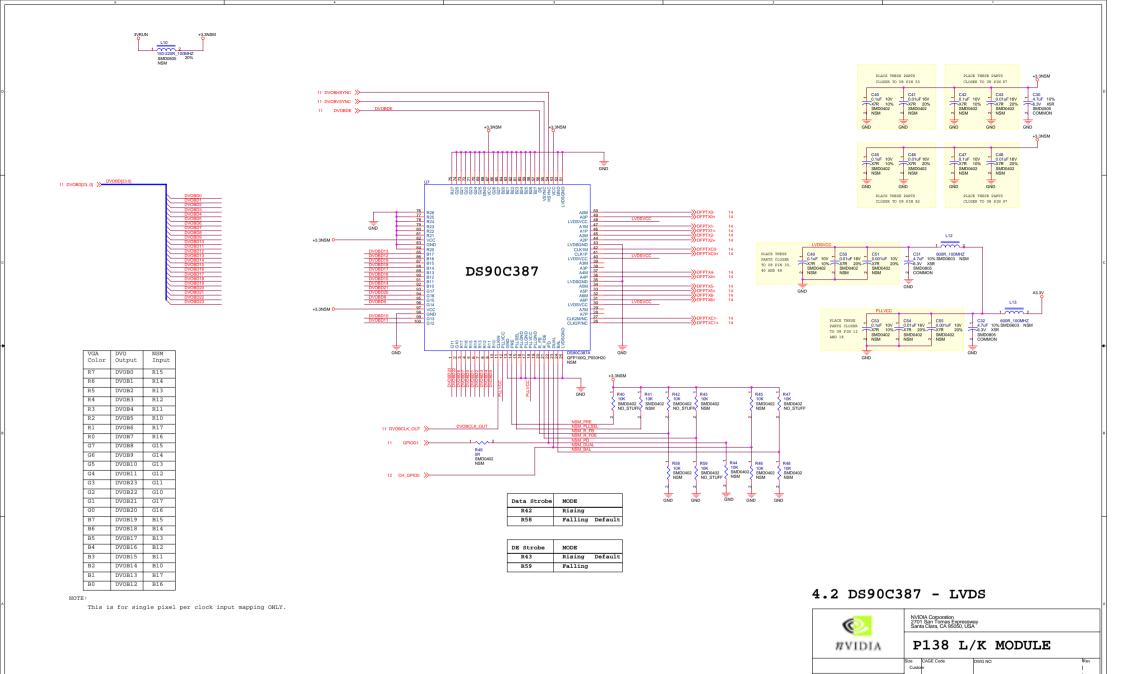
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