

DOCUMENT NUMBER: 105-CXXX00-00A

TITLE

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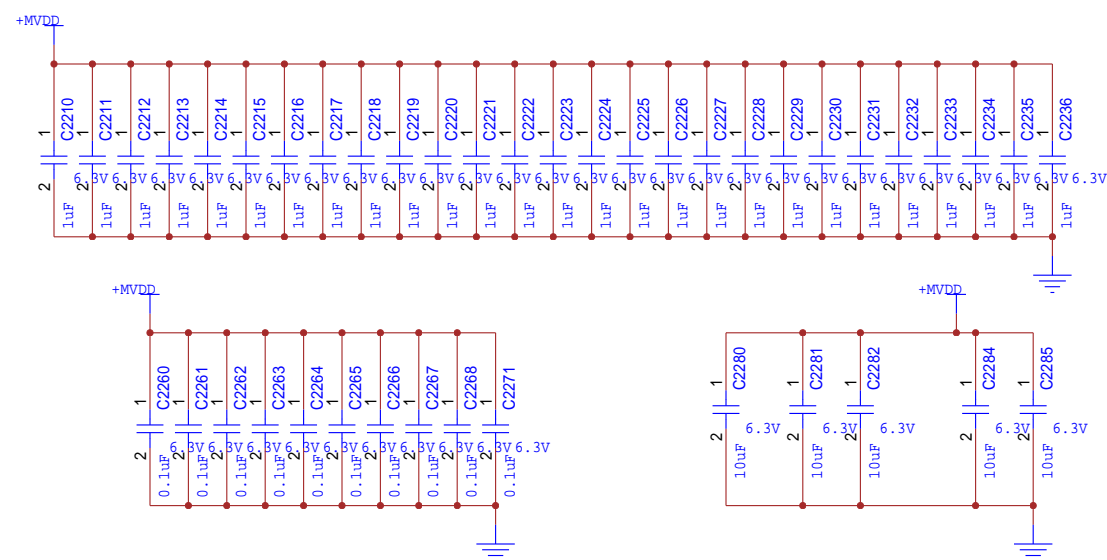
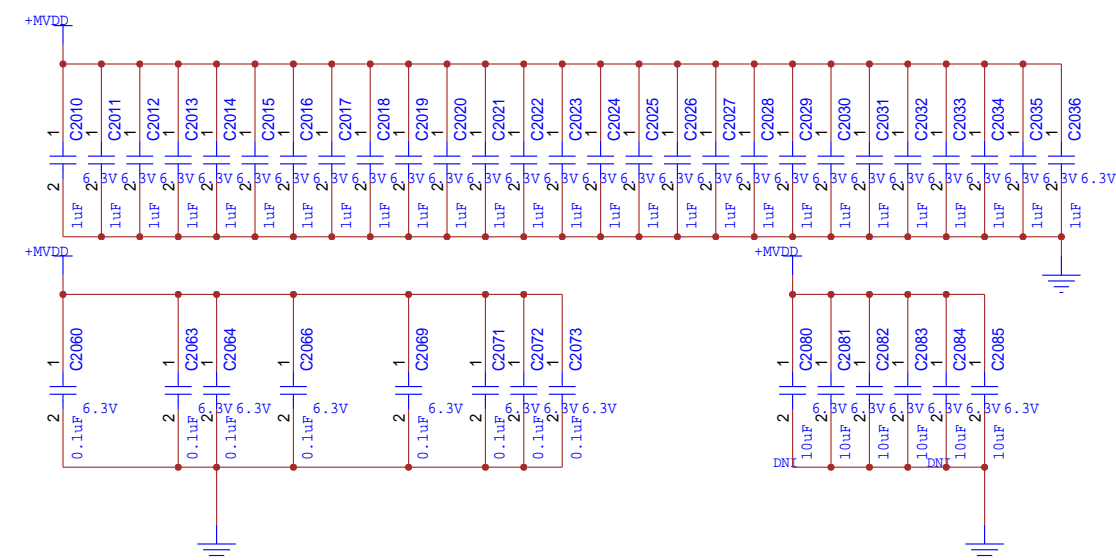
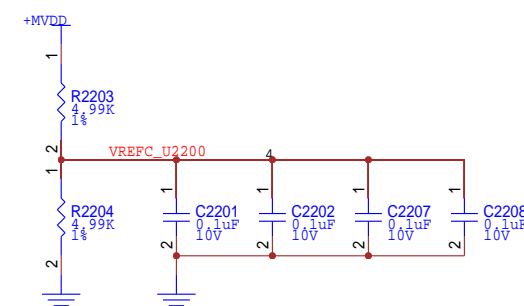
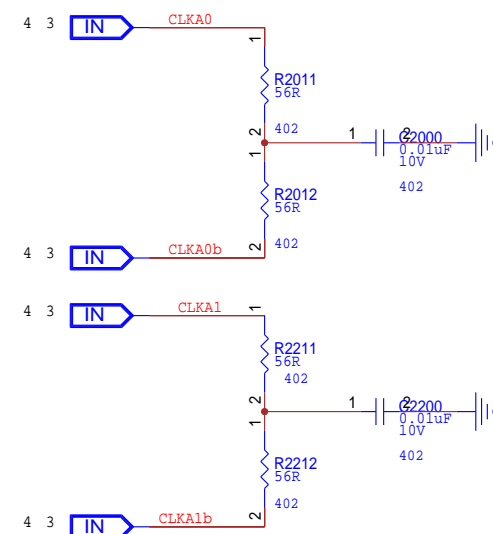
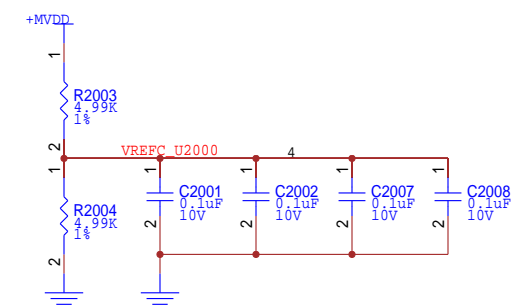
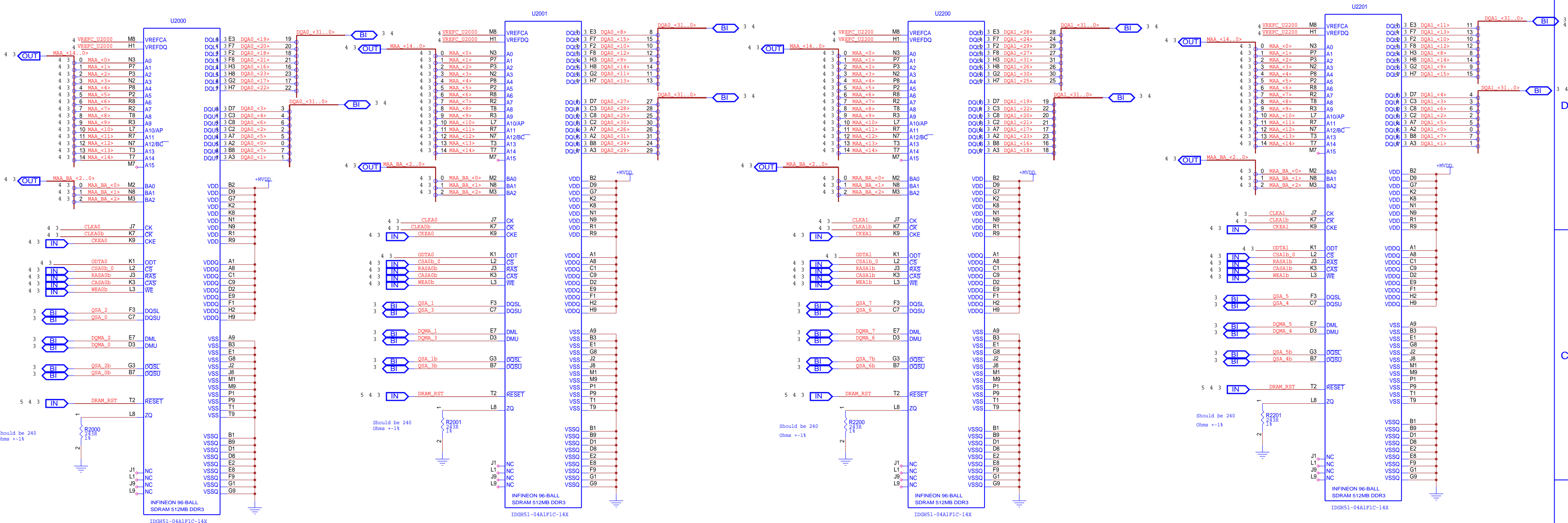
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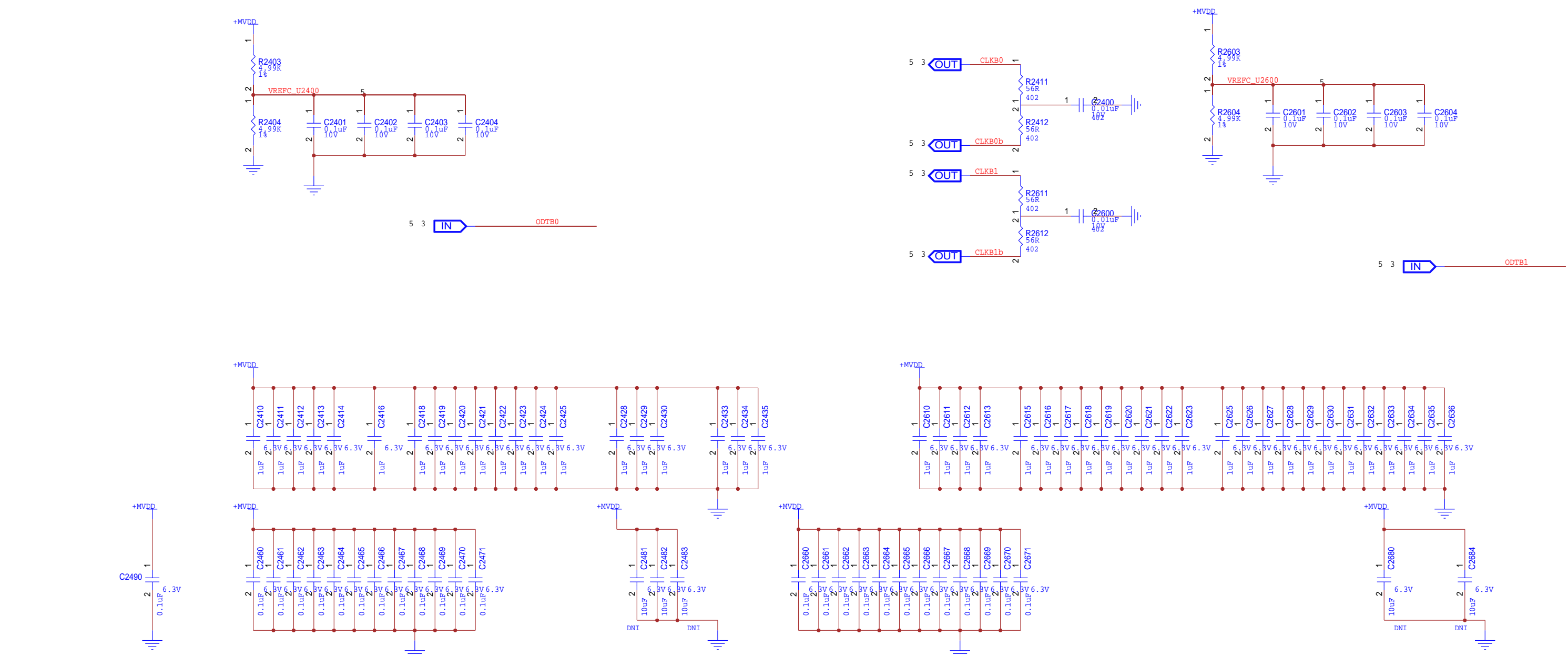
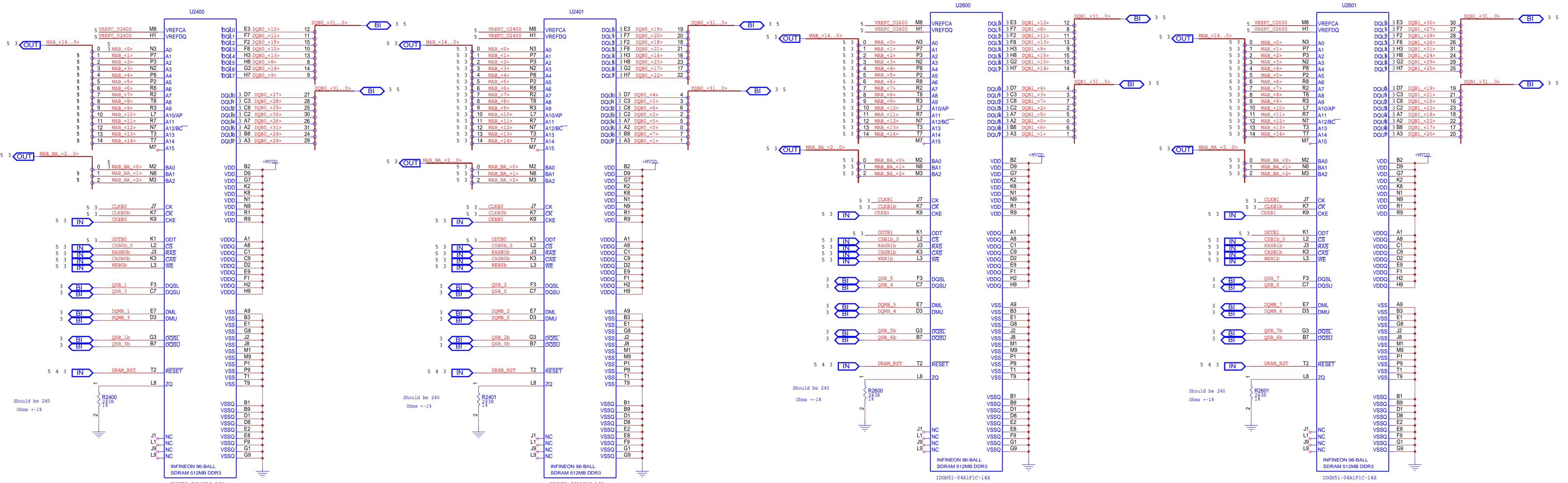
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(4) DDR3 Memory Channel A



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DATE: Thu Oct 30 10:11:22 2014	REV: 1.0		
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DOCUMENT NUMBER: 105-CXXX00-00A		TITLE	
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(5) DDR3 Memory Channel B

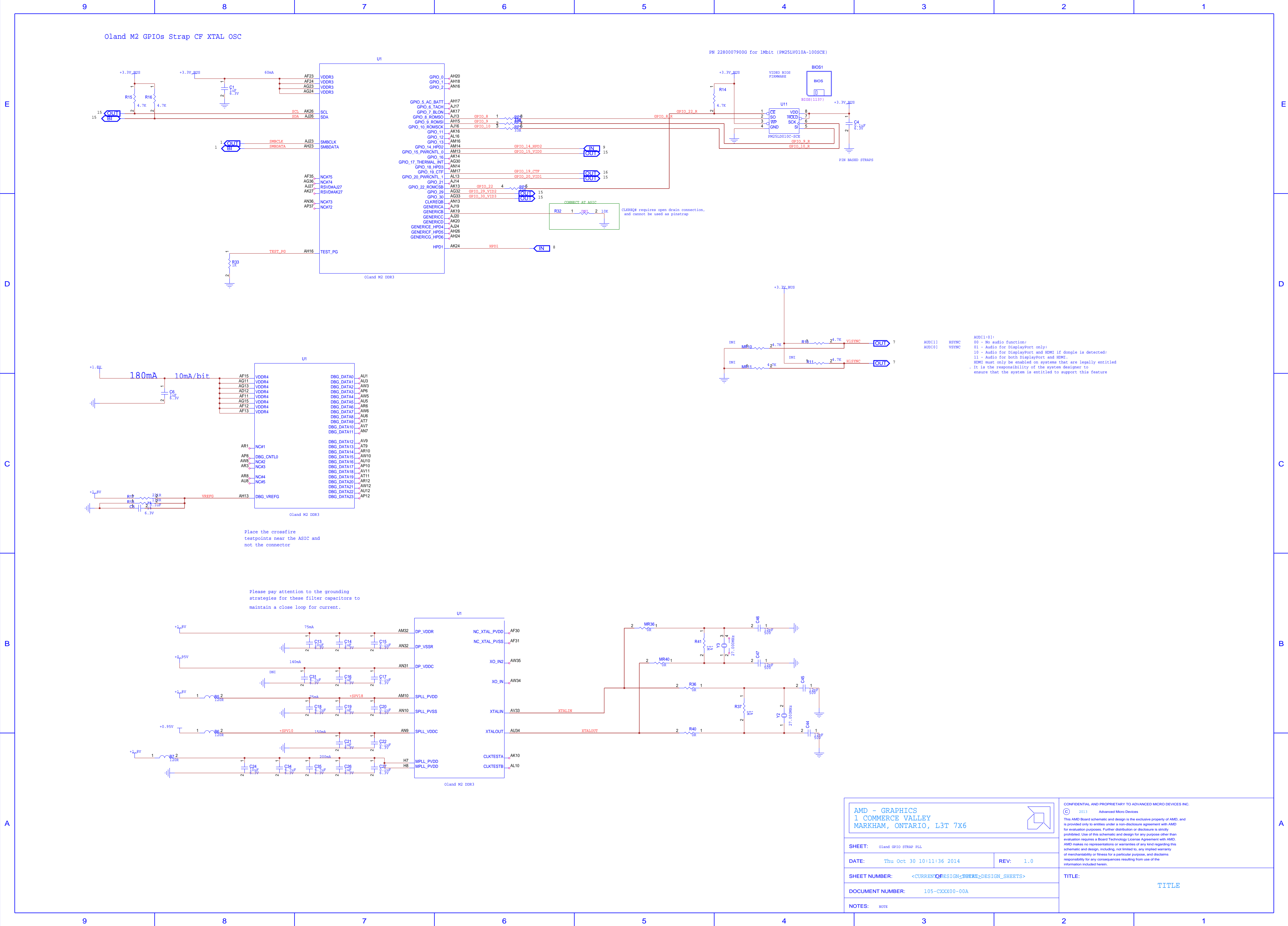



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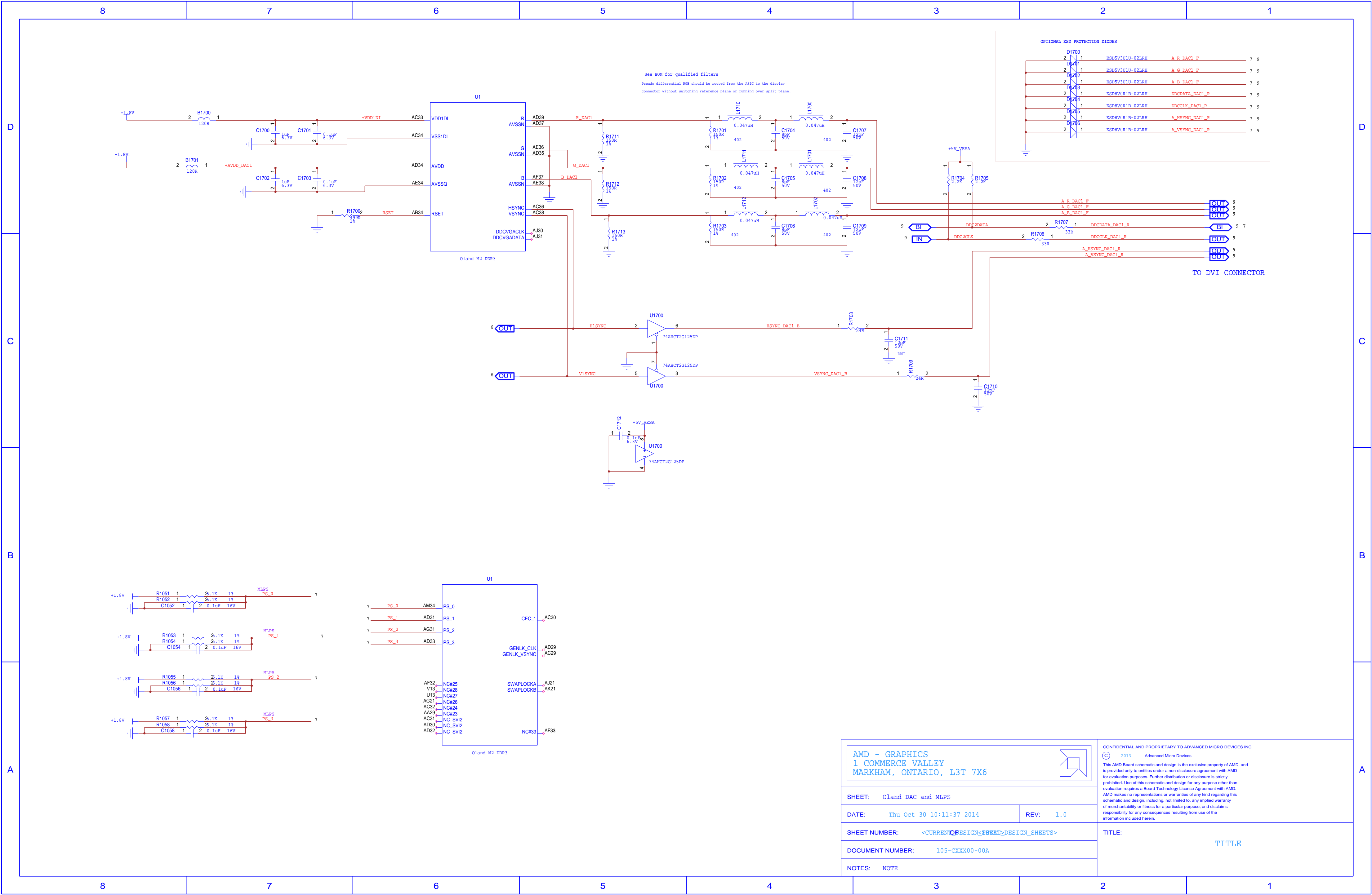
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SHEET: DDR3 CHB
DATE: Thu Oct 30 10:11:29 2014
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REV: 1.0
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SHEET: Oland DAC and MLPS

DATE: Thu Oct 30 10:11:37 2014

SHEET NUMBER: <CURRENTDESIGN>DESIGN_SHEETS>

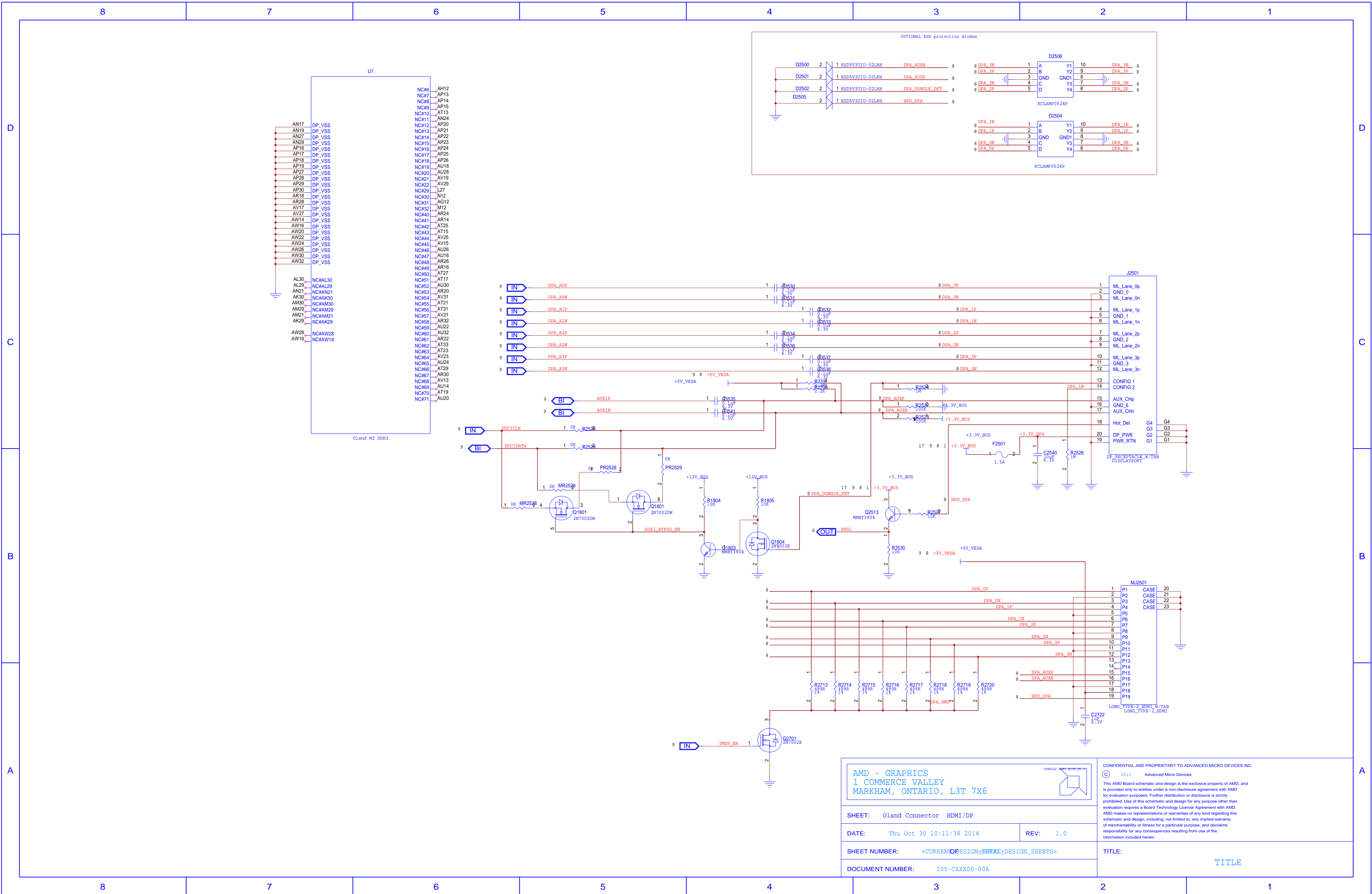
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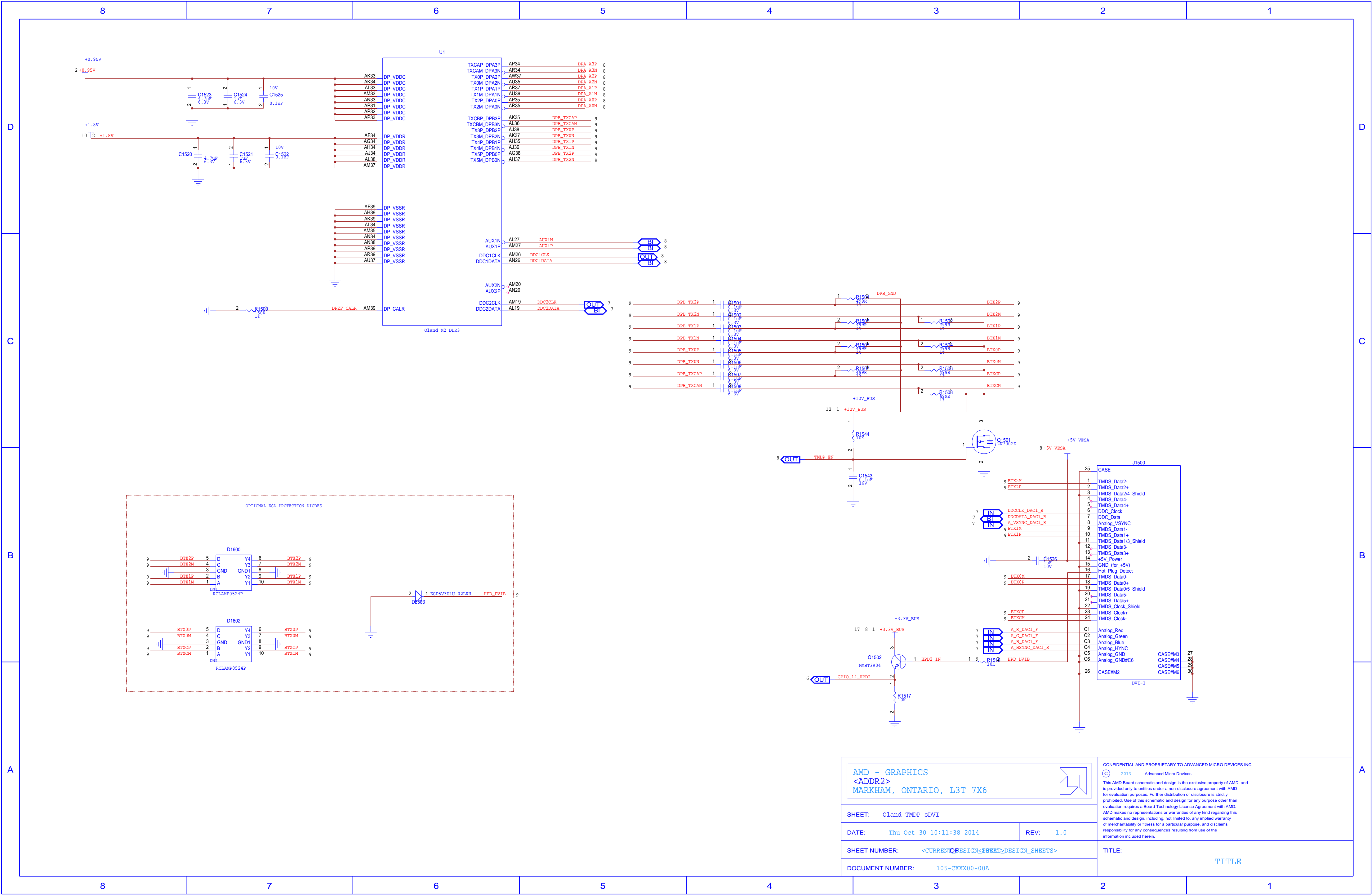
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AMD - GRAPHICS
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MARKHAM, ONTARIO, L3T 7X6

SHEET: Oland TMDP sDVI

DATE: Thu Oct 30 10:11:38 2014

REV: 1.0

SHEET NUMBER: <CURRENTDESIGN><SHEET><DESIGN_SHEETS>

DOCUMENT NUMBER: 105-CXXX00-00A

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TITLE

Oland M2 Power & GND

The schematic diagram illustrates the power and ground distribution for the Oland M2. It features several power planes: +VDDC, +MVDD, +1.8V, +0.95V, and FB_VDDC. The diagram includes numerous decoupling capacitors (C1 through C140) and microcontroller components (MC103, MC131, MC176, MC177, MC178, MC191, MC192, MC300, MC301, MC302). It also shows various signal and power pins for the Oland M2 DDR3 and Oland M2 DDR3 components. The diagram is organized into a grid with columns labeled 1 through 8 and rows labeled A through D.

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SHEET: Oland Power&GND

DATE: Thu Oct 30 10:11:39 2014 REV: 1.0

SHEET NUMBER: <CURRENTDESIGN<SHEET>>DESIGN_SHEETS>

DOCUMENT NUMBER: 105-CXXX00-00A

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TITLE:	TITLE
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D

C

B

A

D

C

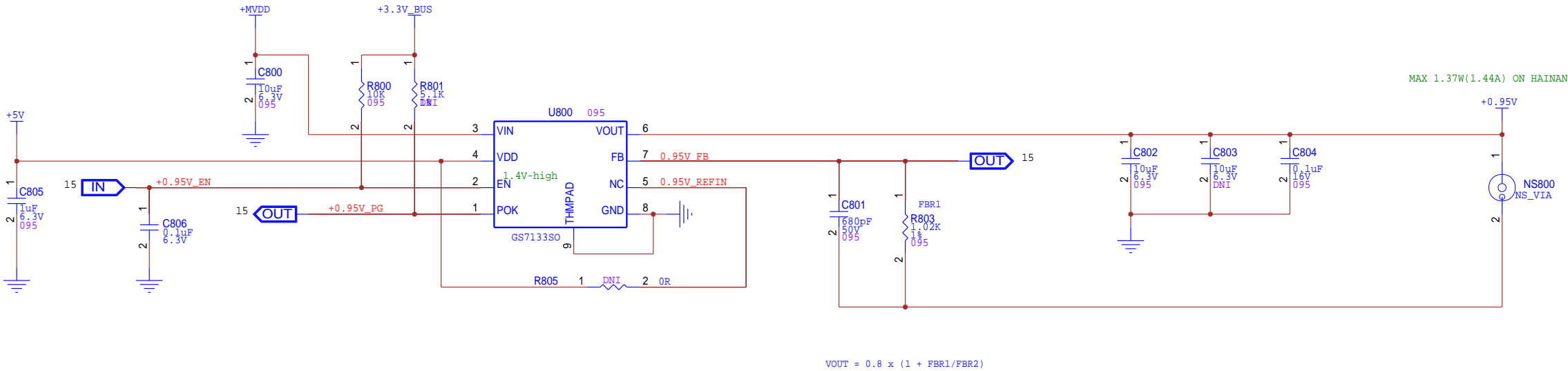
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A

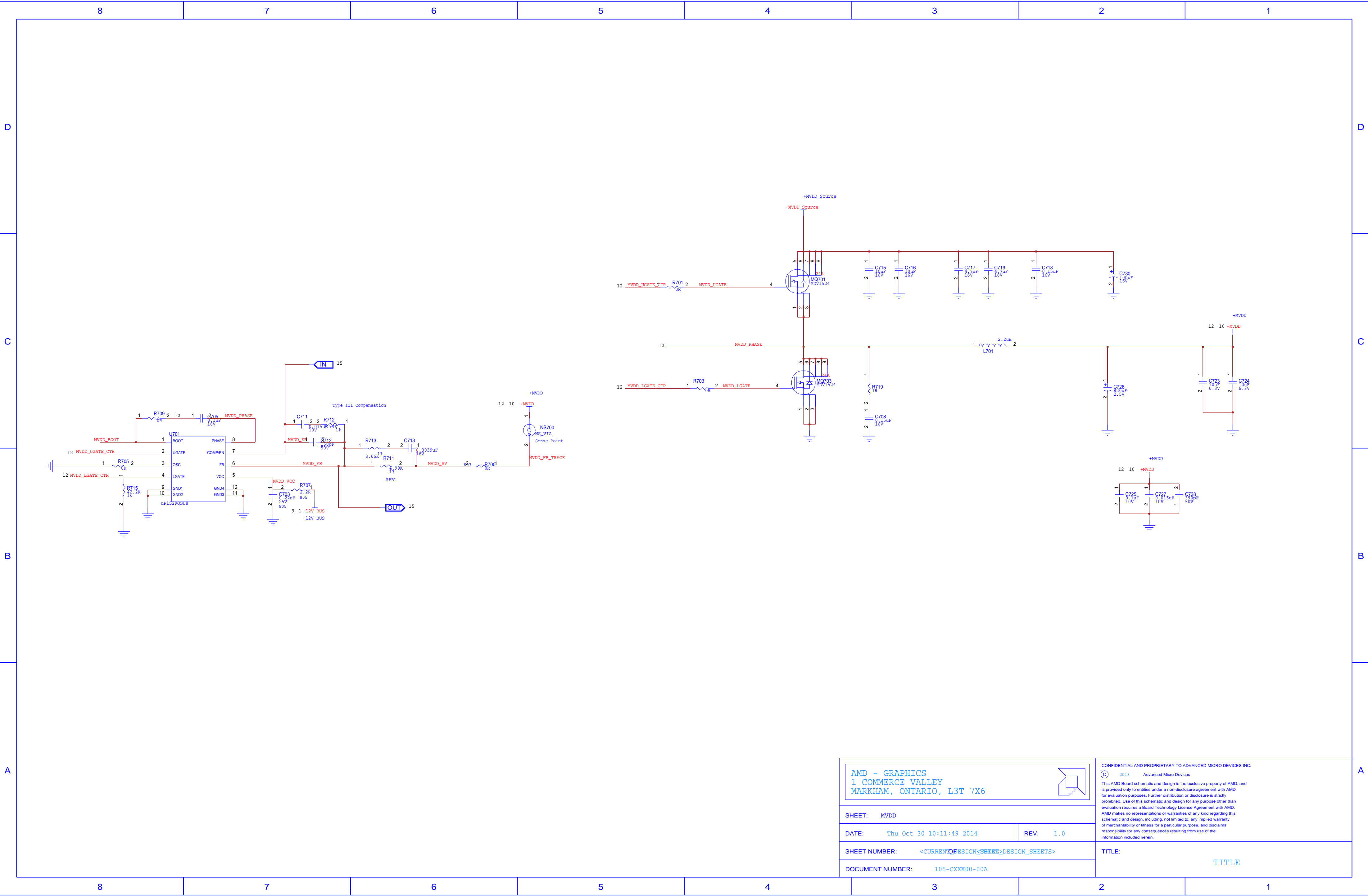
Linear Regulators

LDO #1: Vin = +1.5V +/-2% Vout = +0.95V +/- 2% Iout = 1.44A (TBV) RMS MAX

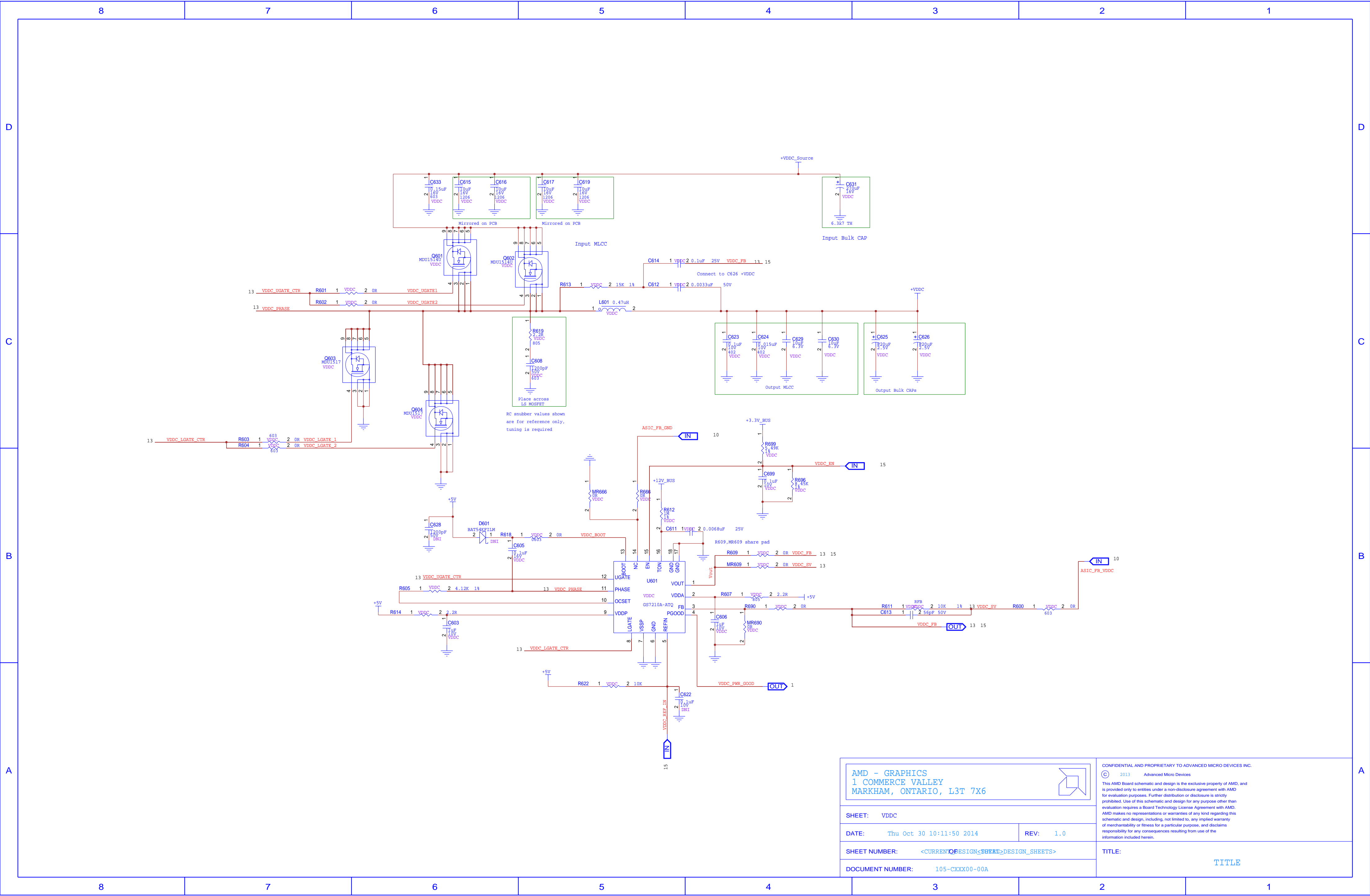
PCB: 50 to 70mm sq. copper area for cooling



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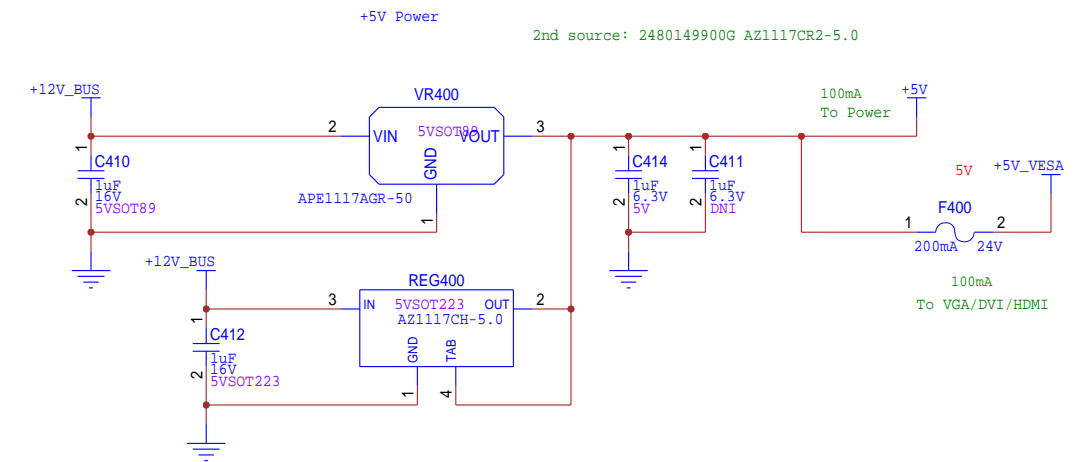
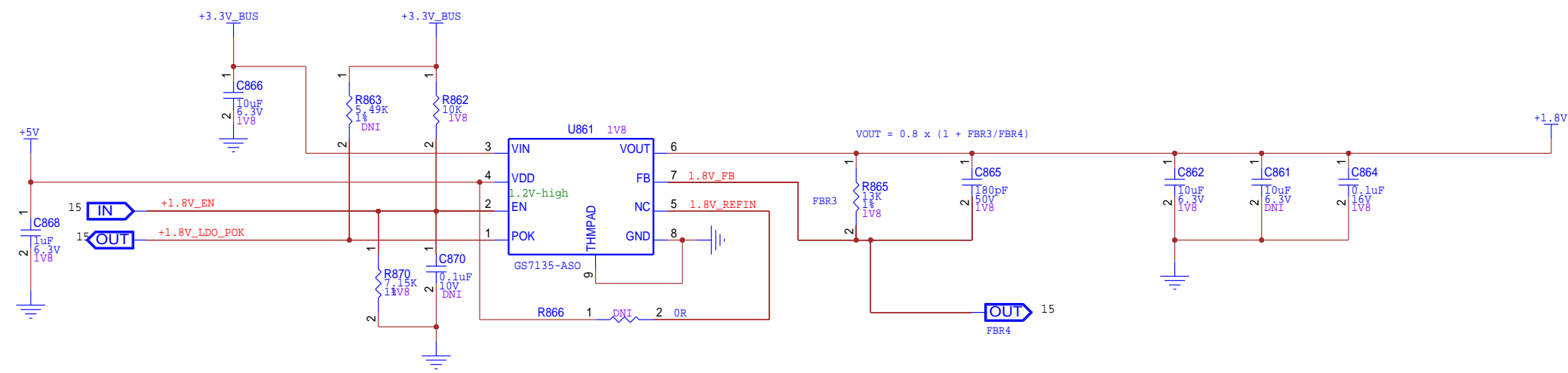
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DOCUMENT NUMBER: 105-CXXX00-00A			

LDO #2: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TbV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



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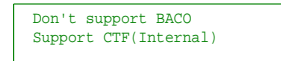
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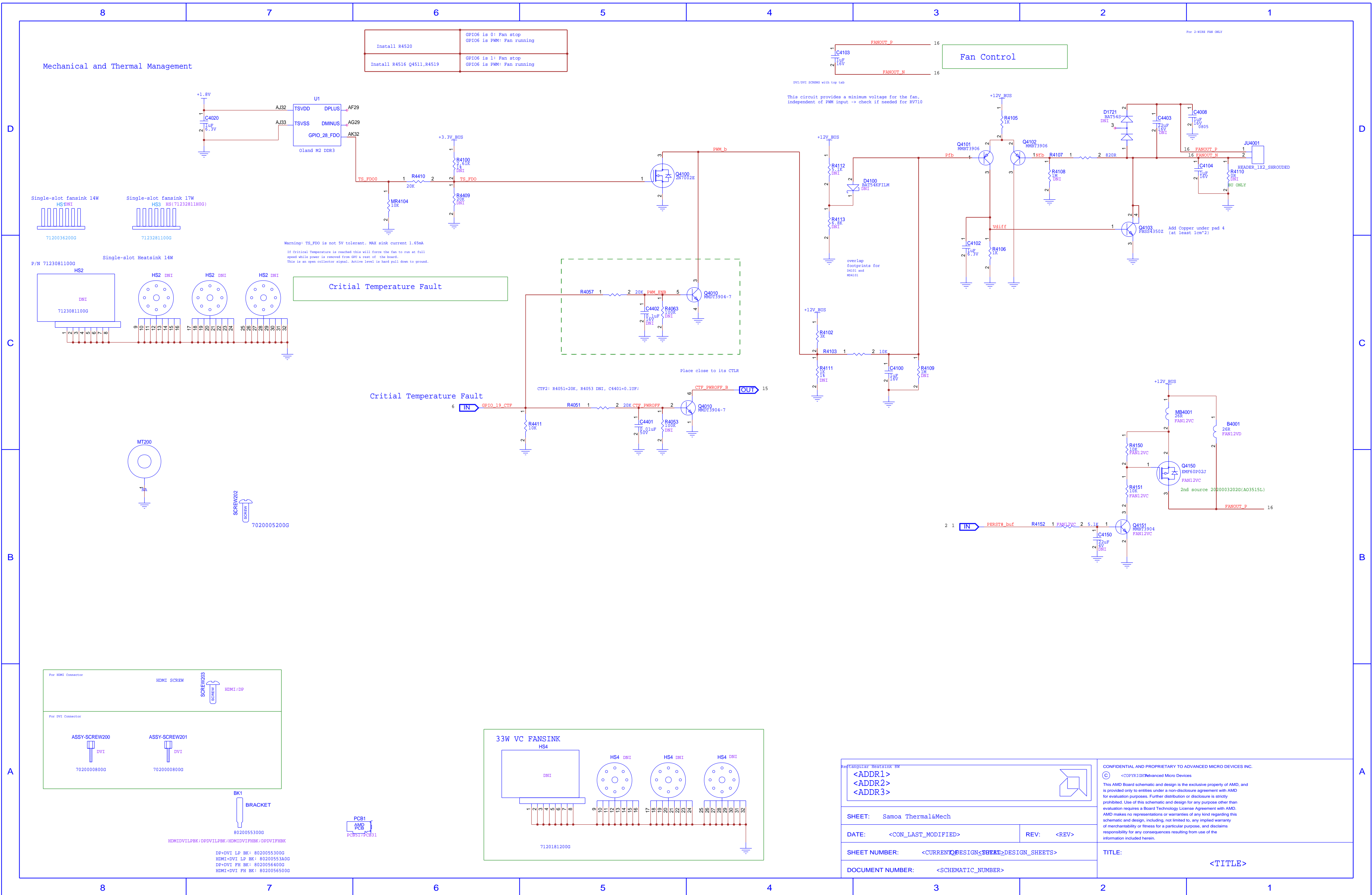
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DOCUMENT NUMBER: 105-CXXX00-00A

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B

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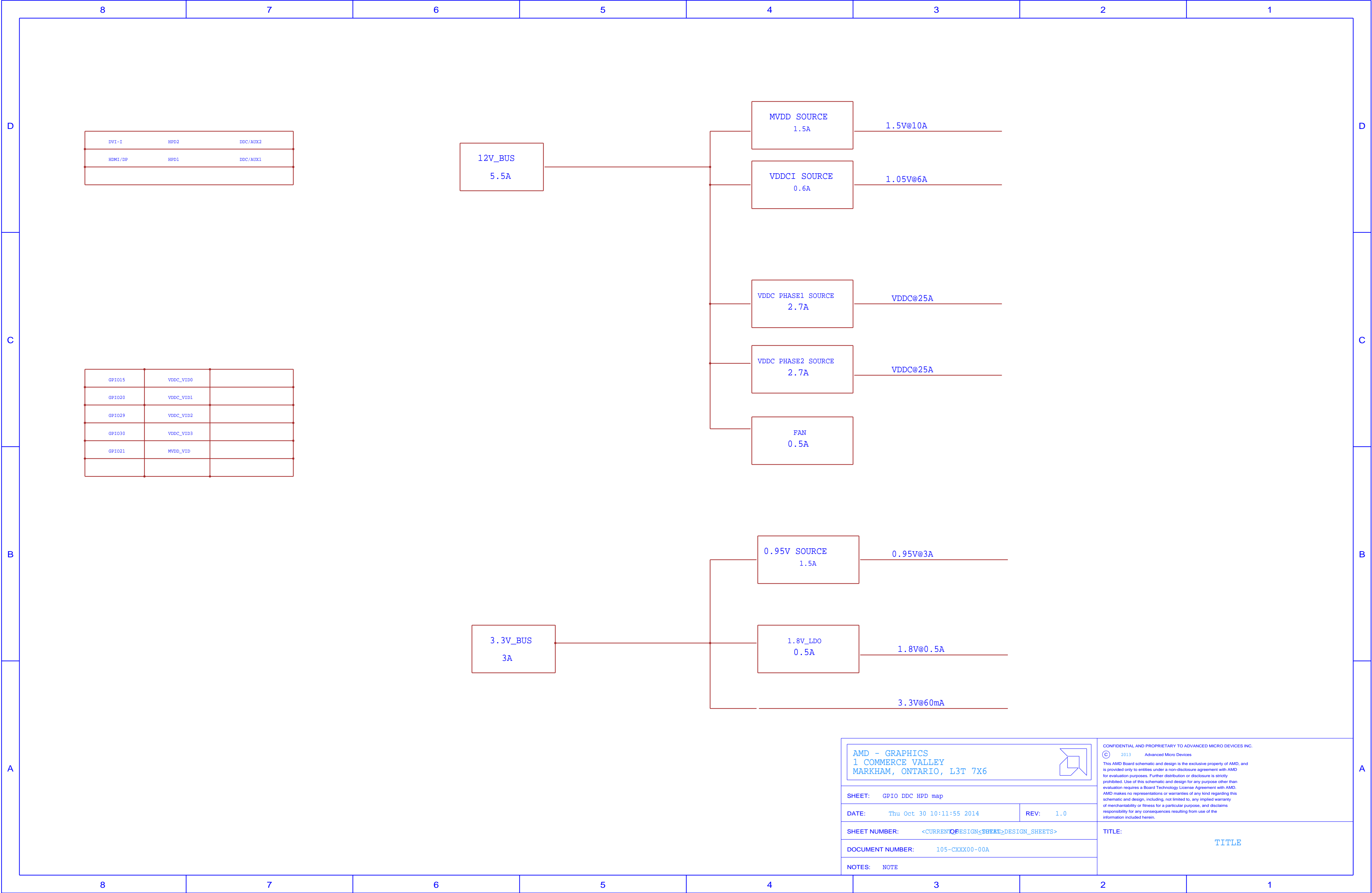
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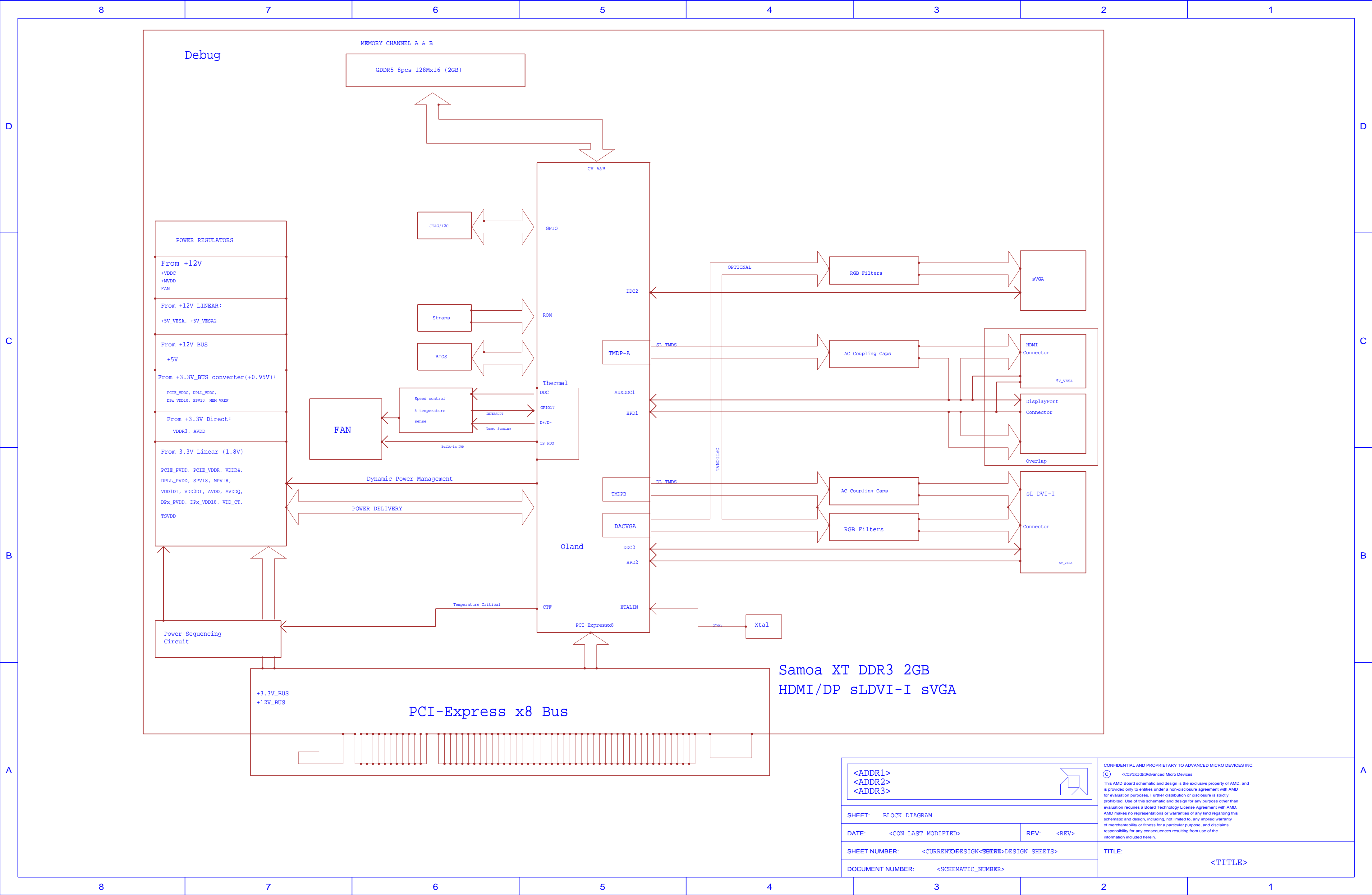
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DOCUMENT NUMBER: 105-CXXX00-00A





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D				TITLE Samoa XT DDR3 4GB SL_DVI-I+HDMI/DP			SCHEMATIC NO. 105-C872XX-00C			DATE													
				REVISION HISTORY			NOTE: <small>THIS SCHEMATIC REPRESENTS THE PCB, IT DOES NOT REPRESENT ANY SPECIFIC BOM. FOR STUFFING OPTIONS (COMPONENT VALUES, DUT) PLEASE CONSULT THE PRODUCT SPECIFIC BOM. PLEASE CONTACT AMD REPRESENTATIVE TO OBTAIN LATEST BOM CLOSEST TO THE APPLICATION DESIRED.</small>			REV P01													
	SCH REV	PCB REV	DATE	REVISION DESCRIPTION																			
	00	00B	2014/07/17	Initial Samoa XT DDR3 schematic based on C718																			
C																							
B																							
A																							
8			7			6			5			4			3			2			1		

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