

C116-B, NV31/NV34, 2M/4M/8M/DDR, 64MB, VIDEO OUT, VGA

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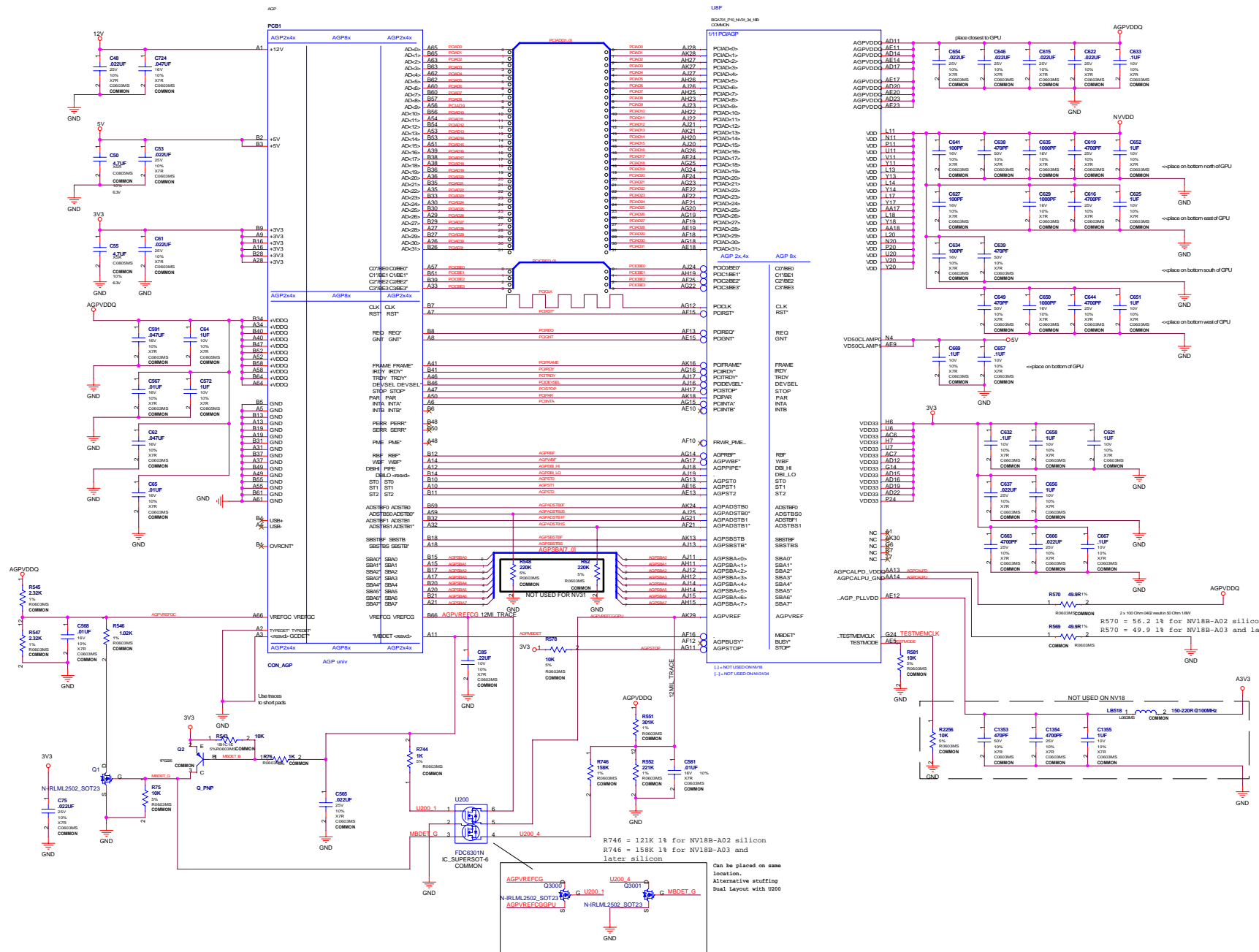
HISTORY:

0B

A. Change R534 from 2.43K_1% to 2.55K_1% (R11-2551T13-Y01), R533 change from 1.05K_1% to 1.18K_1% (R11-1181T13-Y01) to get FBVDDQ=2.528V.
B. Add R591 (2.2 ohm_0603_5%) and C409 (2200p_0603) to reduce VRM noise on L1 pin1.
200. SHORT ALL MEMORY DAMPING RESISTOR AND CHANGE COLOR TO RED.
210. ADD FBAA12 TO SUPPORT 16M*16 MEMORY


1 change all 0402 footprint to 0603.
2. Page 2
a. remove C62, C590, C574, C566, C615, C628, C642, C631, C626, C648, C647, C645, C624, R609, R625
b. add 2 MOSFET for U200 daul-lay
3. Page 3
remove C603, C609, C618, C611, C612, C610, C604, C592, R768, R770, R772, R774
4. Page 4, 5
a. remove C1112, C238, C241, C1115, C250, C1113, C1114, C228, C230, C1120, C1119, C247, C245, C244, C1121, C232, C1122
b. remove C1100, C247, C277, C1101, C1102, C286, C264, C1104, C1106, C280, C281, C299, C1107, C1108, C269, C270
c. remove memory data all damping(15ohm).
d. Move bypass capacitors(C1161, C1162, C1163, C1164) of memory clock to close GPU(PAGE3).
5. Page 6
remove U13(BIOS(ALTERNATIVE)), TEMP Sensor
6. Page 7
change Y3 package to DIP
7. Page 8
remove R695, R694, R693, R7, R1, C788, C797, C819, C806, C787, C796, C805, C818, C786, C795, C817, C804, L510, L509, L508
8. Page 10
a. remove S_OUT1, AV_OUT1, C789, C809, C790, C810, C791, C812, L519, L520, L521
b. add 9pin-mini-din
9. Page 11
a. remove ISL6529
b. add mosfet and OP(LM358) for NVVDD, FBVDD, FBVDDQ
c. change C41, C39 to DIP package
0728
change data[48:63] sequence
ddr suport 16*16M
0728
SUPOUT NV18B

NV18 AGP SECTION AND AGP CONNECTOR

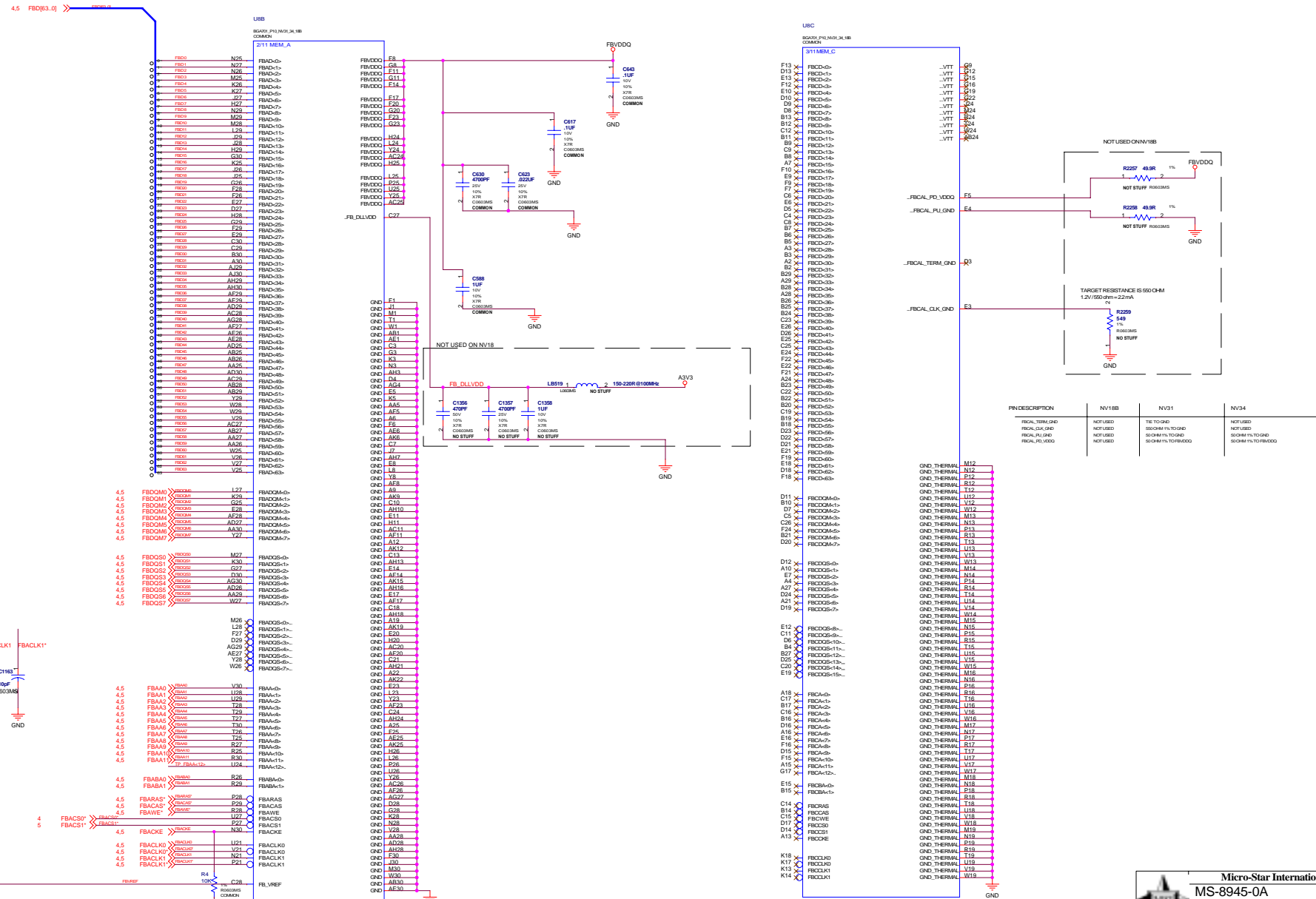


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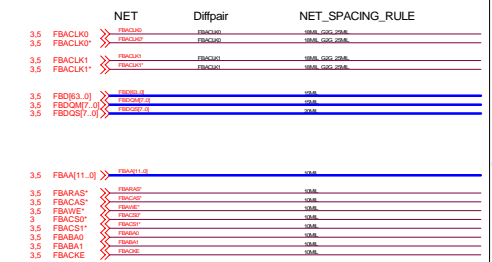
	Micro-Star International Co., LTD.			
	MS-8945-0A			
	Size	Document Number		Rev
	Custom	AGP INTERFACE		A00
Date:	Wurzburg, February 04, 2004 1 Sheet 2 of 11			

NV18 FRAMEBUFFER INTERFACE AND DECOUPLING



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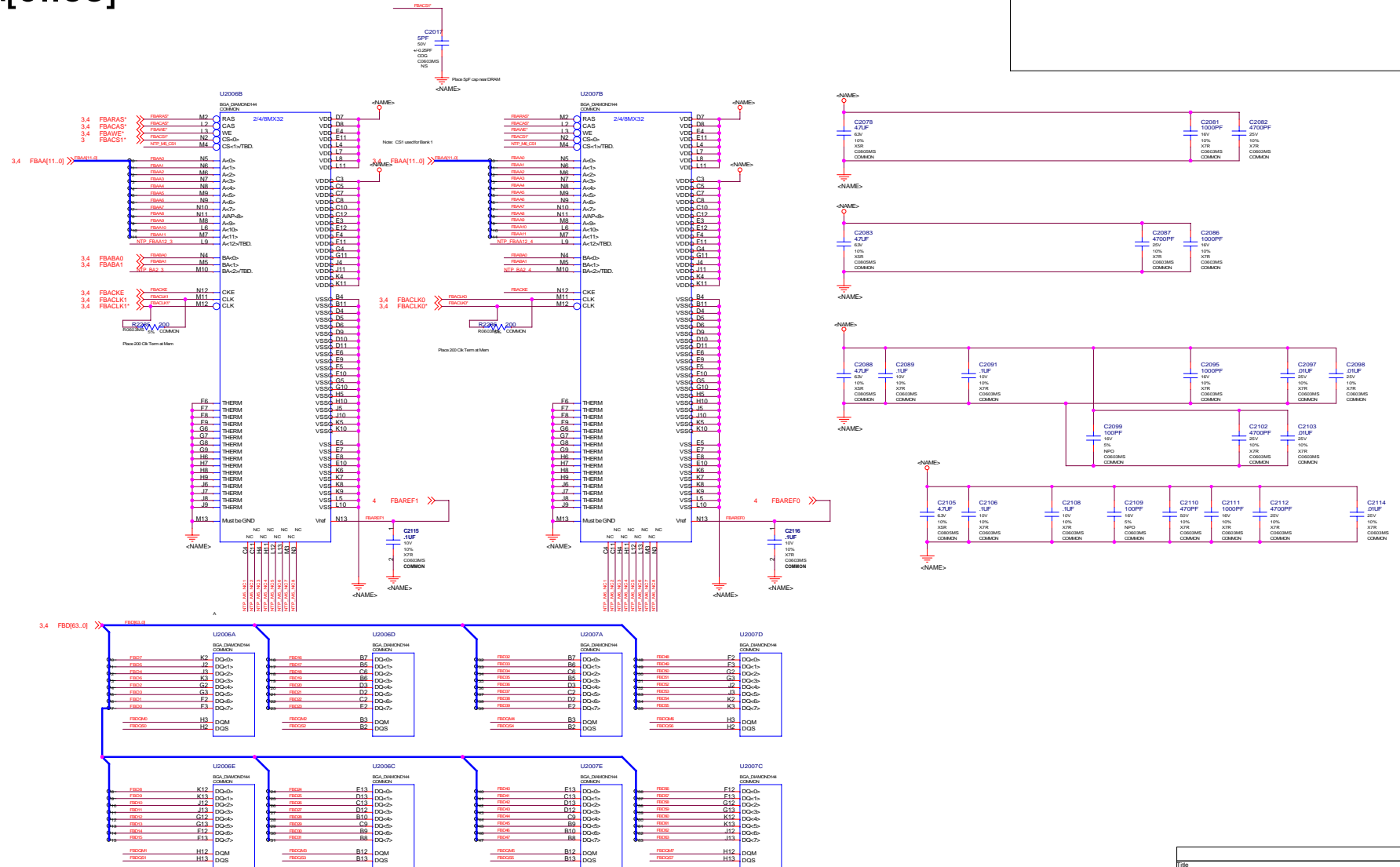
Bank 0: FBA[0..63]



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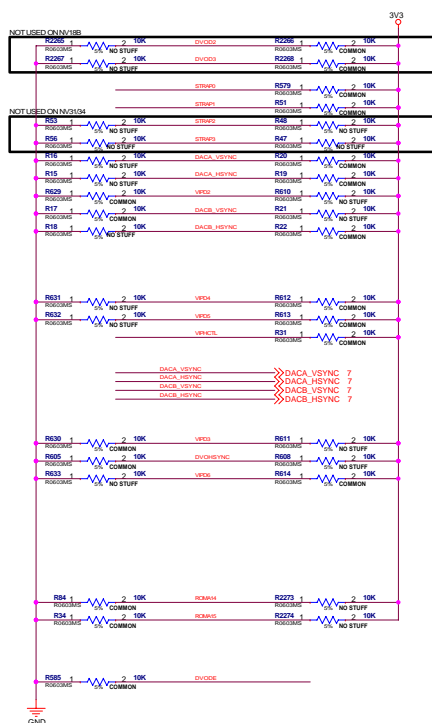
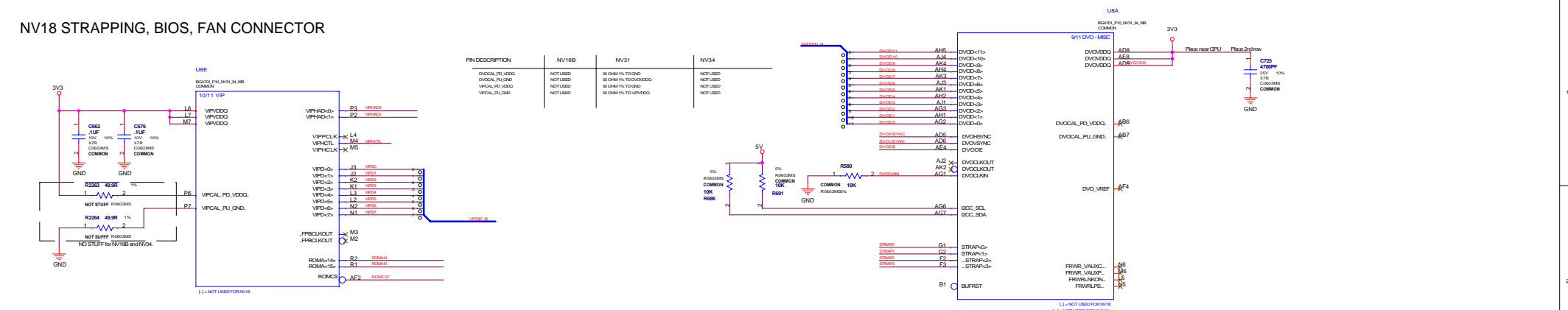
Partition A:Bottom Side Memory

Bank 0: FBA[0..63]



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Size	Document Number	Rev	
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Date:	Monday, January 05, 2004	Sheet	5 of 11

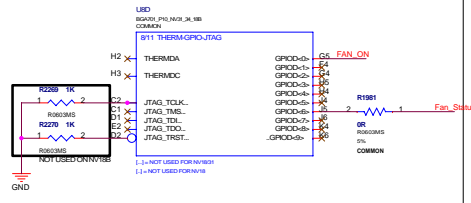
NV18 STRAPPING, BIOS, FAN CONNECTOR



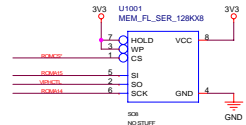
STRAPPING OPTIONS

Bit	Signal	VALUE_ID	VALUES
30	PCI_A0_30WHP	PCI_A0	000000000
31	SUB_VENDOR	SUB_VENDOR	00000000
32	RAM_CFG_0	RAM_CFG[0]	00000000000000000000000000000000
33	RAM_CFG_1		00000000000000000000000000000000
34	RAM_CFG_2		00000000000000000000000000000000
35	RAM_CFG_3		00000000000000000000000000000000
36	CRYSTAL_0	CRYSTAL[0]	00000000000000000000000000000000
37	TX_ADDR_0	TX_ADDR[0]	00000000000000000000000000000000
38	TX_ADDR_1		00000000000000000000000000000000
39	AGP_PIC16	AGP_PIC16	00000000000000000000000000000000
40	AGP_IDA	AGP_IDA	00000000000000000000000000000000
41	AGP_IDA2W0		00000000000000000000000000000000
42	PCI_DEVID_0	PCI_DEVID[0]	00000000000000000000000000000000
43	PCI_DEVID_1		00000000000000000000000000000000
44	SYS_TYPE	SYS_TYPE[0]	00000000000000000000000000000000
45	FP_FID0		00000000000000000000000000000000
46	USER_0		00000000000000000000000000000000
47	USER_1		00000000000000000000000000000000
48	USER_2		00000000000000000000000000000000
49	USER_3		00000000000000000000000000000000
50	PCI_DEVID_2		00000000000000000000000000000000
51	PCI_DEVID_3		00000000000000000000000000000000
52	CRYSTAL_1		00000000000000000000000000000000
53	FR_0		00000000000000000000000000000000
54	FR_1		00000000000000000000000000000000
55	SR		00000000000000000000000000000000
56	SR_GSM		00000000000000000000000000000000
57	SR_AGP		00000000000000000000000000000000
58	SR_ID		00000000000000000000000000000000
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60	ROM_TYPE_1		00000000000000000000000000000000
61	GSM_ID_0	ISMS[0]	00000000000000000000000000000000

NV18 GPIO

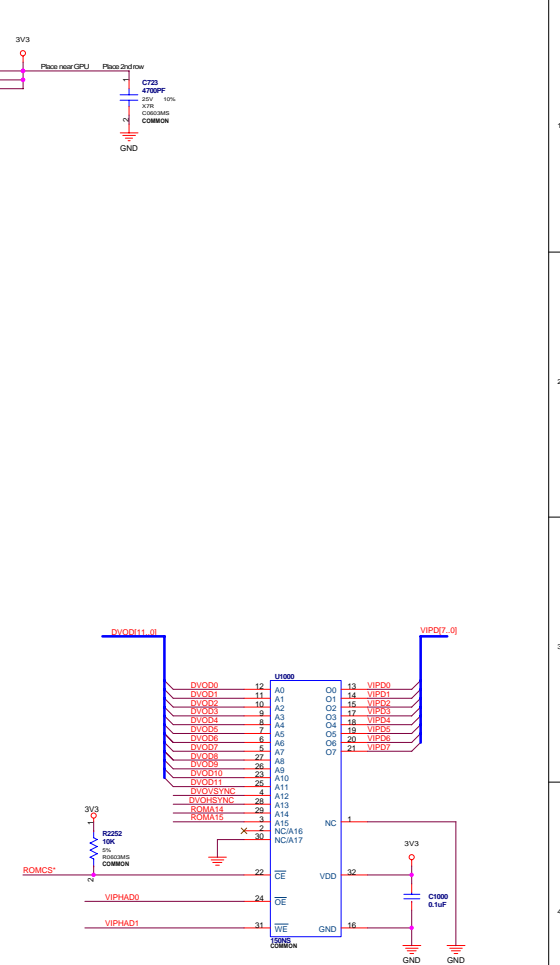
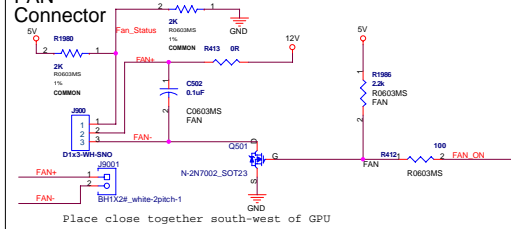


EEPROM

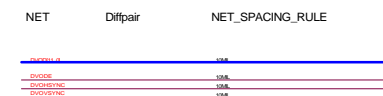


U1000 AND U1001 IS DUALAY.

FAN



VOLTAGE



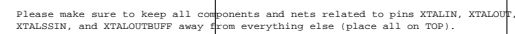
Micro-Star International Co., LTD.

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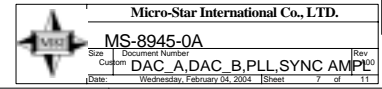
Size		Document Number	Rev
Custom		NV34 STRAPPING BIOS	A00
Date:	Wednesday, February 04, 2004	Sheet	6 of 11

PLEASE DUALLAY THE PULL-UP
RESISTER AND PULL-DOWN RESISTER.

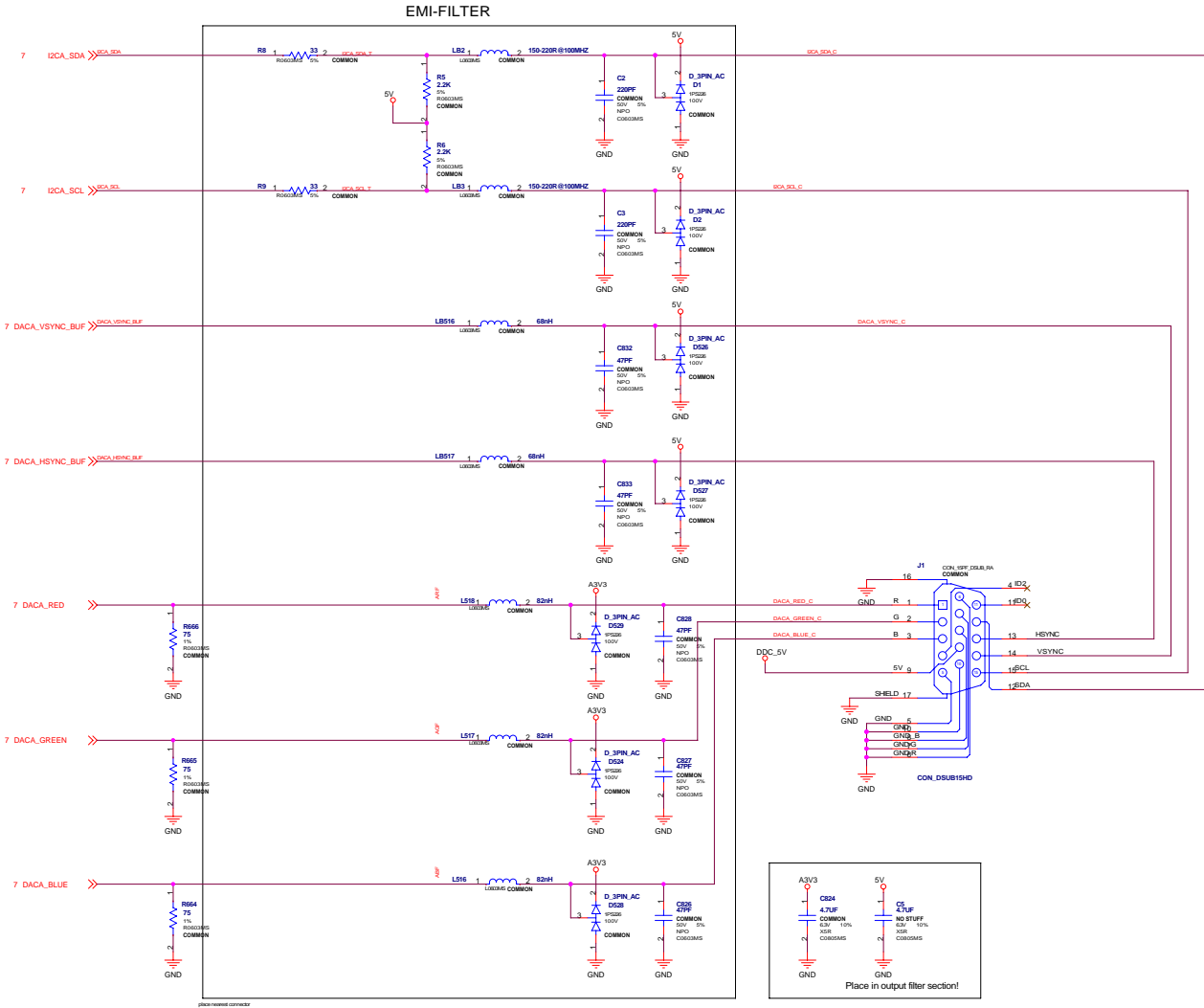
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8	DACA_RED	DACA_RED	37.5 OHM	200k, 200, 200k
8	DACA_GREEN	DACA_GREEN	37.5 OHM	200k, 200, 200k
8	DACA_BLUE	DACA_BLUE	37.5 OHM	200k, 200, 200k
9	DACB_RED	DACB_RED	37.5 OHM	200k, 200, 200k
9	DACB_GREEN	DACB_GREEN	37.5 OHM	200k, 200, 200k
9	DACB_BLUE	DACB_BLUE	37.5 OHM	200k, 200, 200k

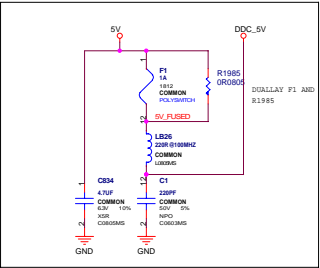


DACB output



NET	IMPEDANCE	NET_SPACING_RULE
REF	37.5 OHM	20M_100_20M
REF	37.5 OHM	20M_100_20M
REF	37.5 OHM	20M_100_20M
DACA_RED_C	10MIL TRACE	20M_100_20M
DACA_GREEN_C	10MIL TRACE	20M_100_20M
DACA_BLUE_C	10MIL TRACE	20M_100_20M

DDC 5V



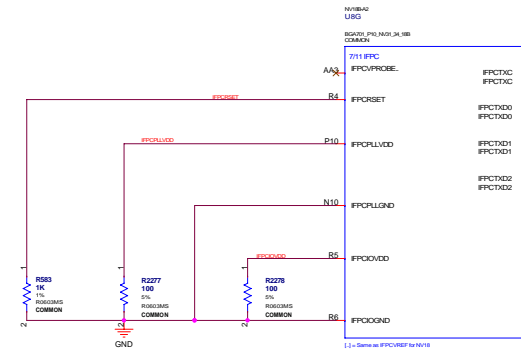
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[illegible]

The schematic diagram illustrates the DACB circuit, which is divided into two channels: DACB_BLUE and DACB_RED. Each channel is powered by a 3.3V supply (A3V3) and ground (GND).


DACB_BLUE Channel:

- Input Stage:** The input signal (DACB_BLUE) is connected to a 75 Ω resistor (R624) and a 1% resistor (R625). The output of this stage is connected to a 2.22pF capacitor (C1368) and a 1.8uF capacitor (C1369).
- Output Stage:** The output of the input stage is connected to a 3.3V supply (A3V3) and ground (GND). The output of this stage is connected to a 3.3V supply (A3V3) and ground (GND).

DACB_RED Channel:

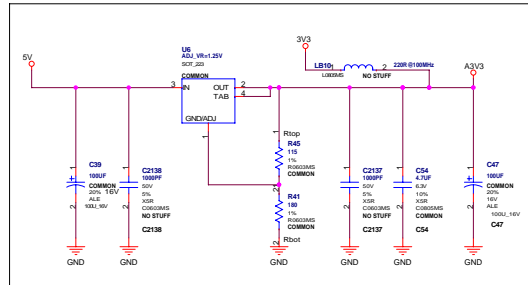
- Input Stage:** The input signal (DACB_RED) is connected to a 75 Ω resistor (R626) and a 1% resistor (R627). The output of this stage is connected to a 2.22pF capacitor (C1368) and a 1.8uF capacitor (C1369).
- Output Stage:** The output of the input stage is connected to a 3.3V supply (A3V3) and ground (GND). The output of this stage is connected to a 3.3V supply (A3V3) and ground (GND).

The circuit is powered by a 3.3V supply (A3V3) and ground (GND). The output of the DACB circuit is connected to a 3.3V supply (A3V3) and ground (GND).

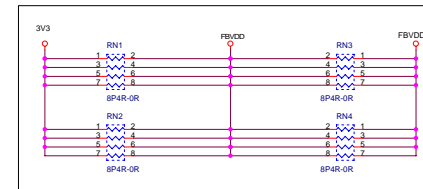
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POWER SUPPLY

ANALOG 3V3

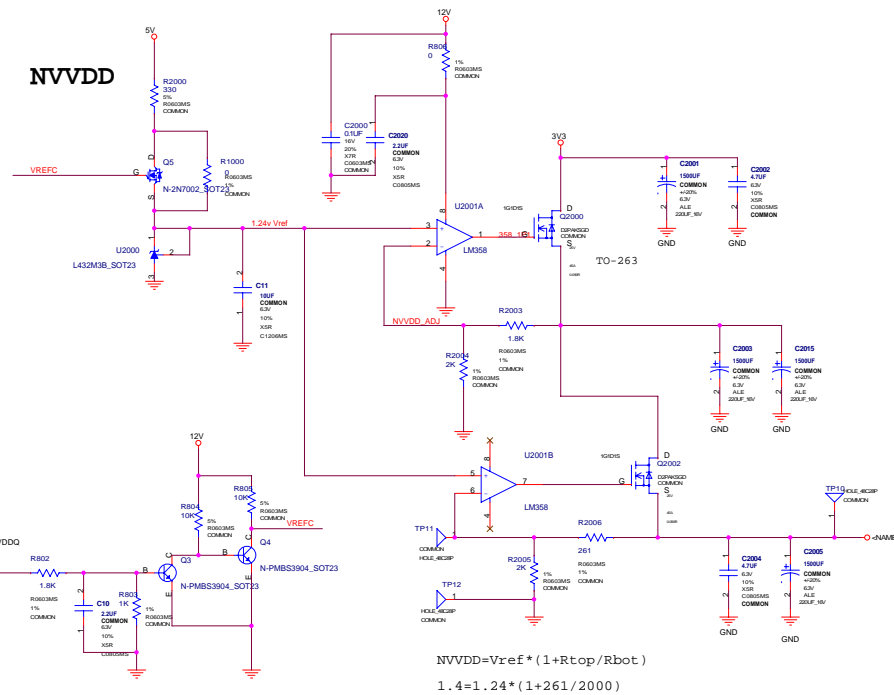


FBVDD 3.3V NO STUFF



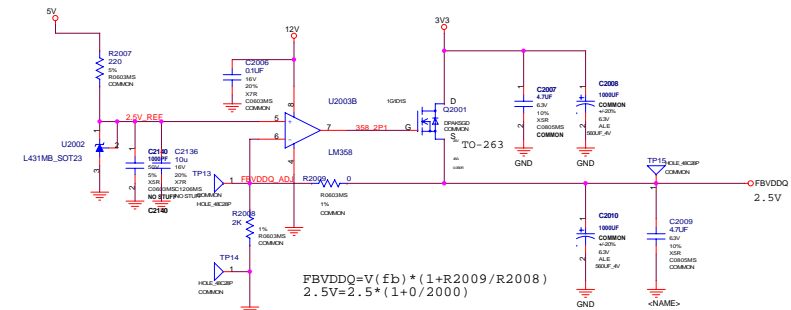
For SAMSUNG DDR FBVDD=FBVDDQ=2..8
HYNIX DDR FBVDD=2.5V on 200MHz

NVVDD



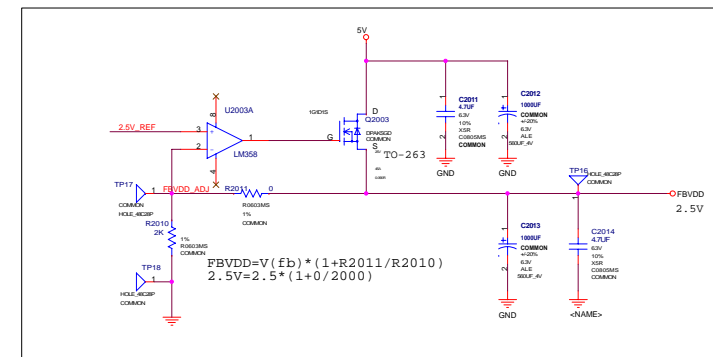
$$1.4 = 1.24 * (1 + 261 / 2000)$$

FBVDDQ



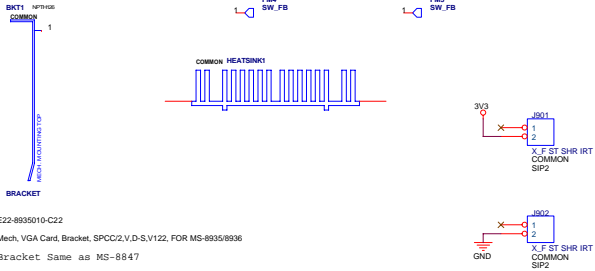
$$\begin{aligned} \text{FBVDDQ} &= V(\text{fb}) * (1 + R_{2009}/R_{2008}) \\ 2.5\text{V} &= 2.5 * (1 + 0/2000) \end{aligned}$$

FBVDD

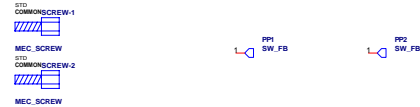


```
COMMON
FBVDD=V(fb)*(1+R2011/R2010)
2.5V=2.5*(1+0/2000)
```


MECHANICS



NET	NET_PHYSICAL_TYPE	VOLTAGE
3V3	3V3	3.3V
5V	5V	5V



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