P413: G86, DDR2 MEMORY 32MX16/16Mx16

REV HISTORY

96/05/28 Add SPDIF citcuit

V147 0A base on V074 12 changed

1.page 4&5 BA<2> change to FBA_CMD27
2.page 7 header change to D_sub
3.page 9 add to dual link
4.page 18&19 add 2nd bank
5.page 20 co-lay FBVDDQ use PWM circuit

ecu	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10413-xxxx-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10413-0000-000	P413: G86-200, 64 BIT DDR2 16Mx16 MEMORY, VGA+DVI+HDout
2	SKU0001	600-10413-0001-000	P413: G86-200, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+HDout
3	SKU0050	600-10413-0050-000	P413: G78-300, 64 BIT DDR2 16Mx16 MEMORY, VGA+DVI+HDout
4	SKU0051	600-10413-0051-000	P413: G78-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+HDout
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P413 Overview

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
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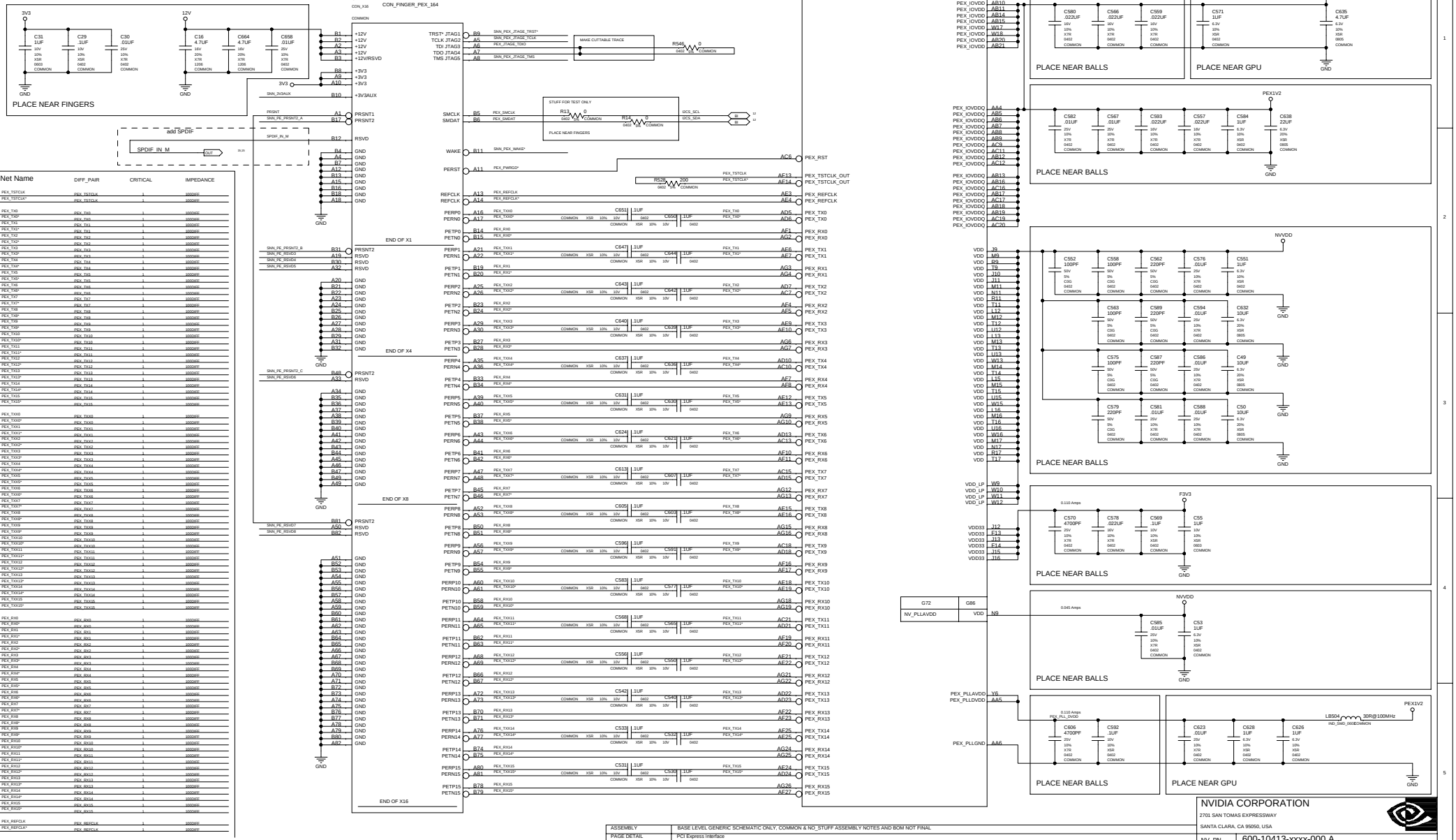
PCI Express Interface



Net Name

Net Name	DIFF_PAIR	CRITICAL	IMPEDANCE
PEX_TSTCLK	PEX_TSTCLK	1	100OHM
PEX_TSTCLK*	PEX_TSTCLK	1	100OHM
PEX_TX0	PEX_TX0	1	100OHM
PEX_TX0*	PEX_TX0	1	100OHM
PEX_TX1	PEX_TX1	1	100OHM
PEX_TX1*	PEX_TX1	1	100OHM
PEX_TX2	PEX_TX2	1	100OHM
PEX_TX2*	PEX_TX2	1	100OHM
PEX_TX3	PEX_TX3	1	100OHM
PEX_TX3*	PEX_TX3	1	100OHM
PEX_TX4	PEX_TX4	1	100OHM
PEX_TX4*	PEX_TX4	1	100OHM
PEX_TX5	PEX_TX5	1	100OHM
PEX_TX5*	PEX_TX5	1	100OHM
PEX_TX6	PEX_TX6	1	100OHM
PEX_TX6*	PEX_TX6	1	100OHM
PEX_TX7	PEX_TX7	1	100OHM
PEX_TX7*	PEX_TX7	1	100OHM
PEX_TX8	PEX_TX8	1	100OHM
PEX_TX8*	PEX_TX8	1	100OHM
PEX_TX9	PEX_TX9	1	100OHM
PEX_TX9*	PEX_TX9	1	100OHM
PEX_TX10	PEX_TX10	1	100OHM
PEX_TX10*	PEX_TX10	1	100OHM
PEX_TX11	PEX_TX11	1	100OHM
PEX_TX11*	PEX_TX11	1	100OHM
PEX_TX12	PEX_TX12	1	100OHM
PEX_TX12*	PEX_TX12	1	100OHM
PEX_TX13	PEX_TX13	1	100OHM
PEX_TX13*	PEX_TX13	1	100OHM
PEX_TX14	PEX_TX14	1	100OHM
PEX_TX14*	PEX_TX14	1	100OHM
PEX_TX15	PEX_TX15	1	100OHM
PEX_TX15*	PEX_TX15	1	100OHM
PEX_RX0	PEX_RX0	1	100OHM
PEX_RX0*	PEX_RX0	1	100OHM
PEX_RX1	PEX_RX1	1	100OHM
PEX_RX1*	PEX_RX1	1	100OHM
PEX_RX2	PEX_RX2	1	100OHM
PEX_RX2*	PEX_RX2	1	100OHM
PEX_RX3	PEX_RX3	1	100OHM
PEX_RX3*	PEX_RX3	1	100OHM
PEX_RX4	PEX_RX4	1	100OHM
PEX_RX4*	PEX_RX4	1	100OHM
PEX_RX5	PEX_RX5	1	100OHM
PEX_RX5*	PEX_RX5	1	100OHM
PEX_RX6	PEX_RX6	1	100OHM
PEX_RX6*	PEX_RX6	1	100OHM
PEX_RX7	PEX_RX7	1	100OHM
PEX_RX7*	PEX_RX7	1	100OHM
PEX_RX8	PEX_RX8	1	100OHM
PEX_RX8*	PEX_RX8	1	100OHM
PEX_RX9	PEX_RX9	1	100OHM
PEX_RX9*	PEX_RX9	1	100OHM
PEX_RX10	PEX_RX10	1	100OHM
PEX_RX10*	PEX_RX10	1	100OHM
PEX_RX11	PEX_RX11	1	100OHM
PEX_RX11*	PEX_RX11	1	100OHM
PEX_RX12	PEX_RX12	1	100OHM
PEX_RX12*	PEX_RX12	1	100OHM
PEX_RX13	PEX_RX13	1	100OHM
PEX_RX13*	PEX_RX13	1	100OHM
PEX_RX14	PEX_RX14	1	100OHM
PEX_RX14*	PEX_RX14	1	100OHM
PEX_RX15	PEX_RX15	1	100OHM
PEX_RX15*	PEX_RX15	1	100OHM
PEX_REFCLK	PEX_REFCLK	1	100OHM
PEX_REFCLK*	PEX_REFCLK	1	100OHM

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express Interface

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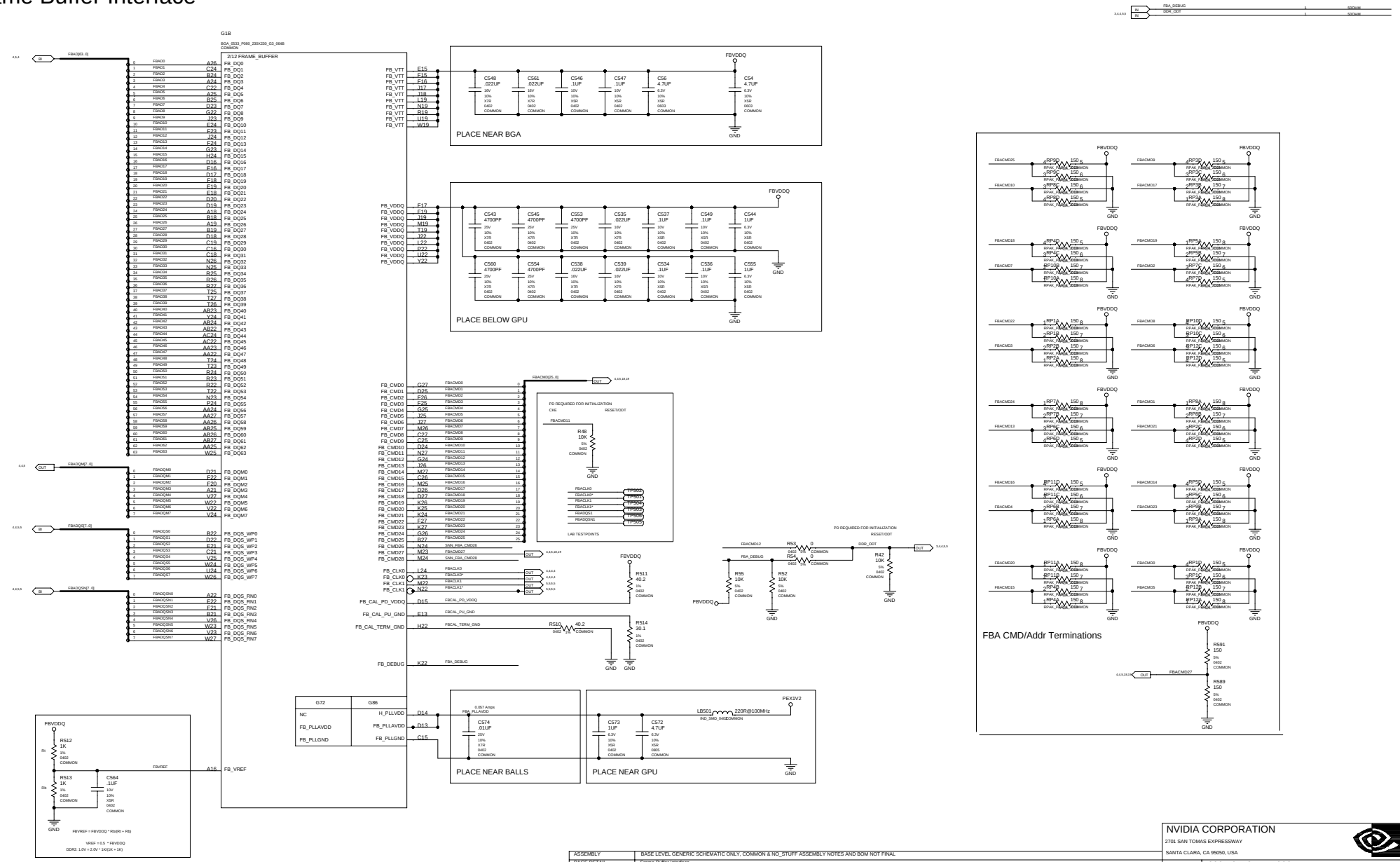
Frame Buffer Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Frame Buffer Interface

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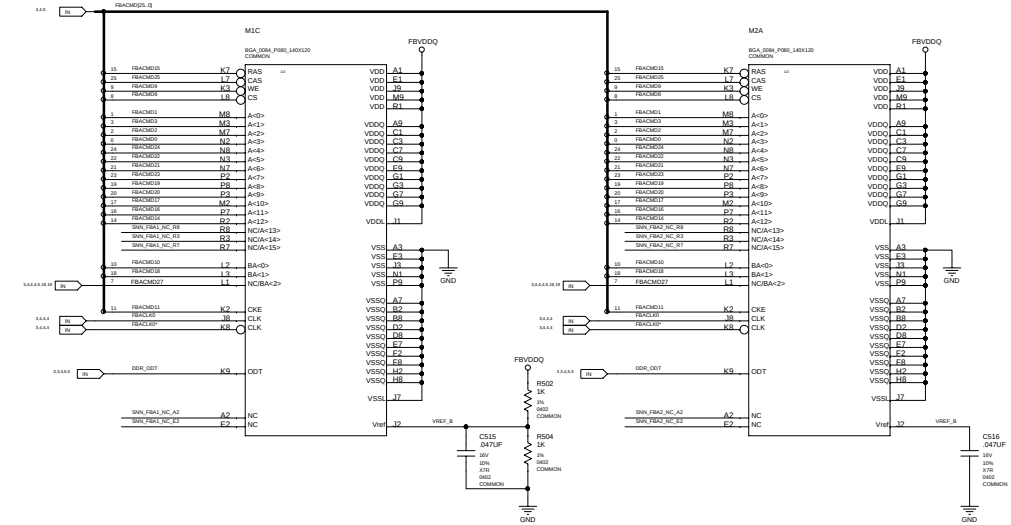
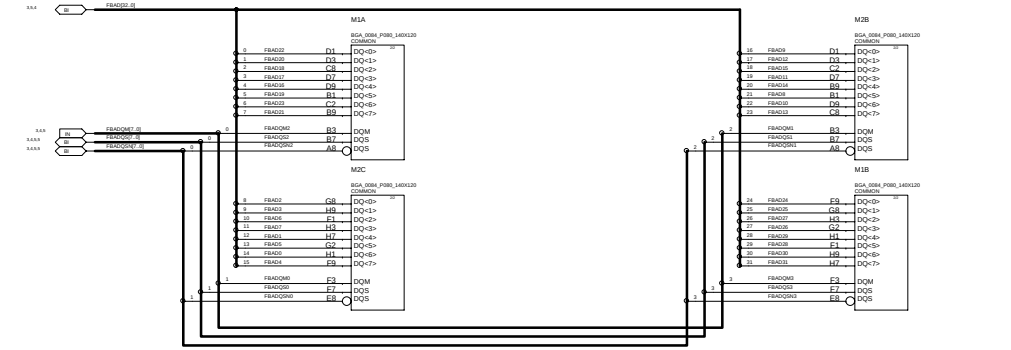
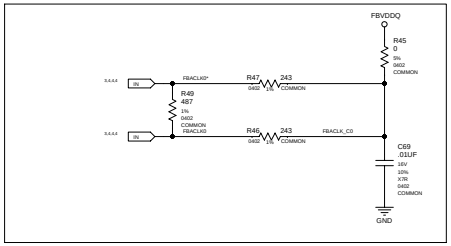
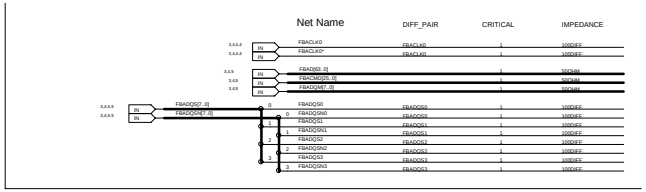
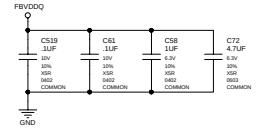
Memory 1st Bank 0..31

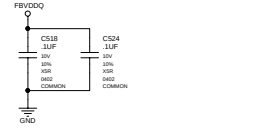


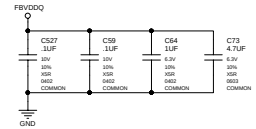


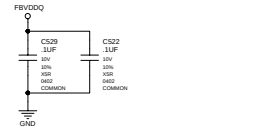




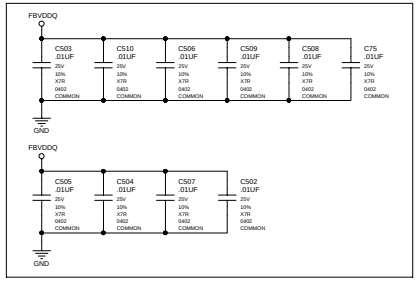




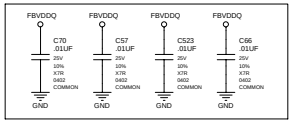




X-cap for CMD



Place these caps next to plane transitions



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Memory 1st Bank 0..31

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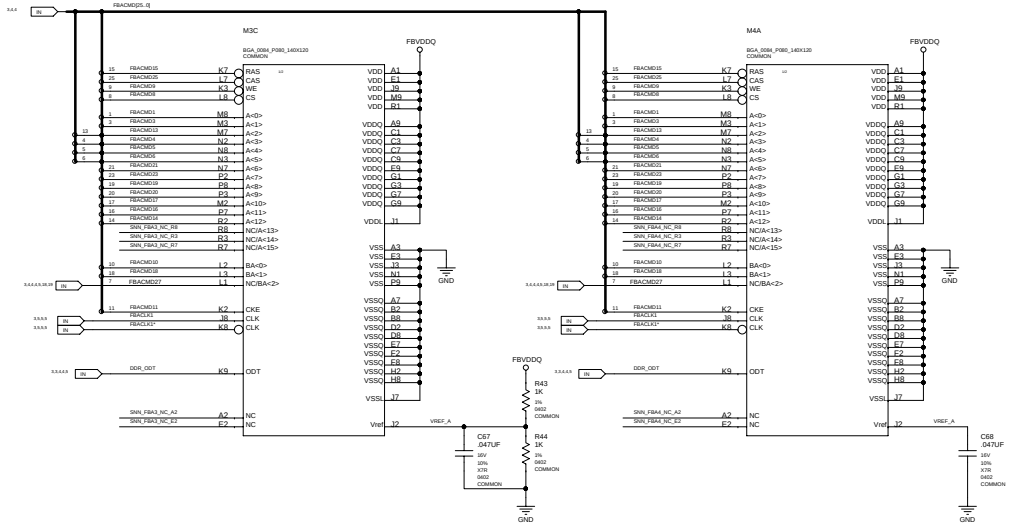
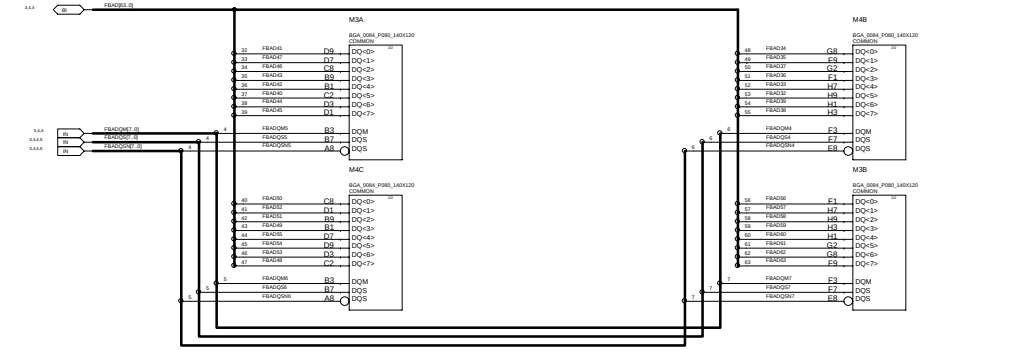
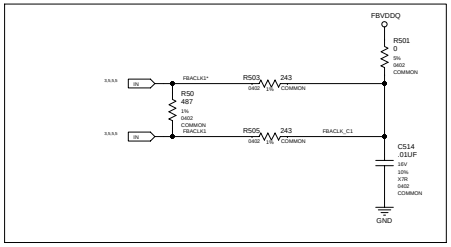
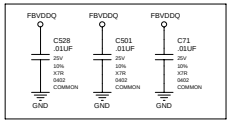
Memory 1st Bank 32..63

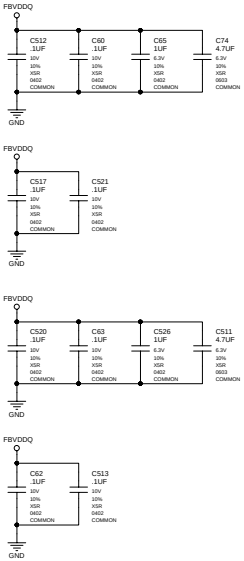




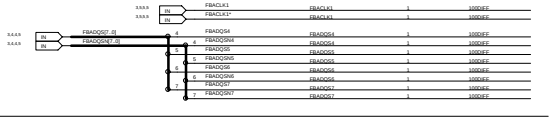


Place near signal transition area





Net Name | DIFF_PAIR | CRITICAL | IMPEDANCE



FBACLK1	FBACLK1	1	100DIFF
FBACLK1*	FBACLK1	1	100DIFF
FBADQS4	FBADQS4	1	100DIFF
FBADQSN4	FBADQS4	1	100DIFF
FBADQS5	FBADQS5	1	100DIFF
FBADQSN5	FBADQS5	1	100DIFF
FBADQS6	FBADQS6	1	100DIFF
FBADQSN6	FBADQS6	1	100DIFF
FBADQS7	FBADQS7	1	100DIFF
FBADQSN7	FBADQS7	1	100DIFF

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Memory 1st Bank 32..63

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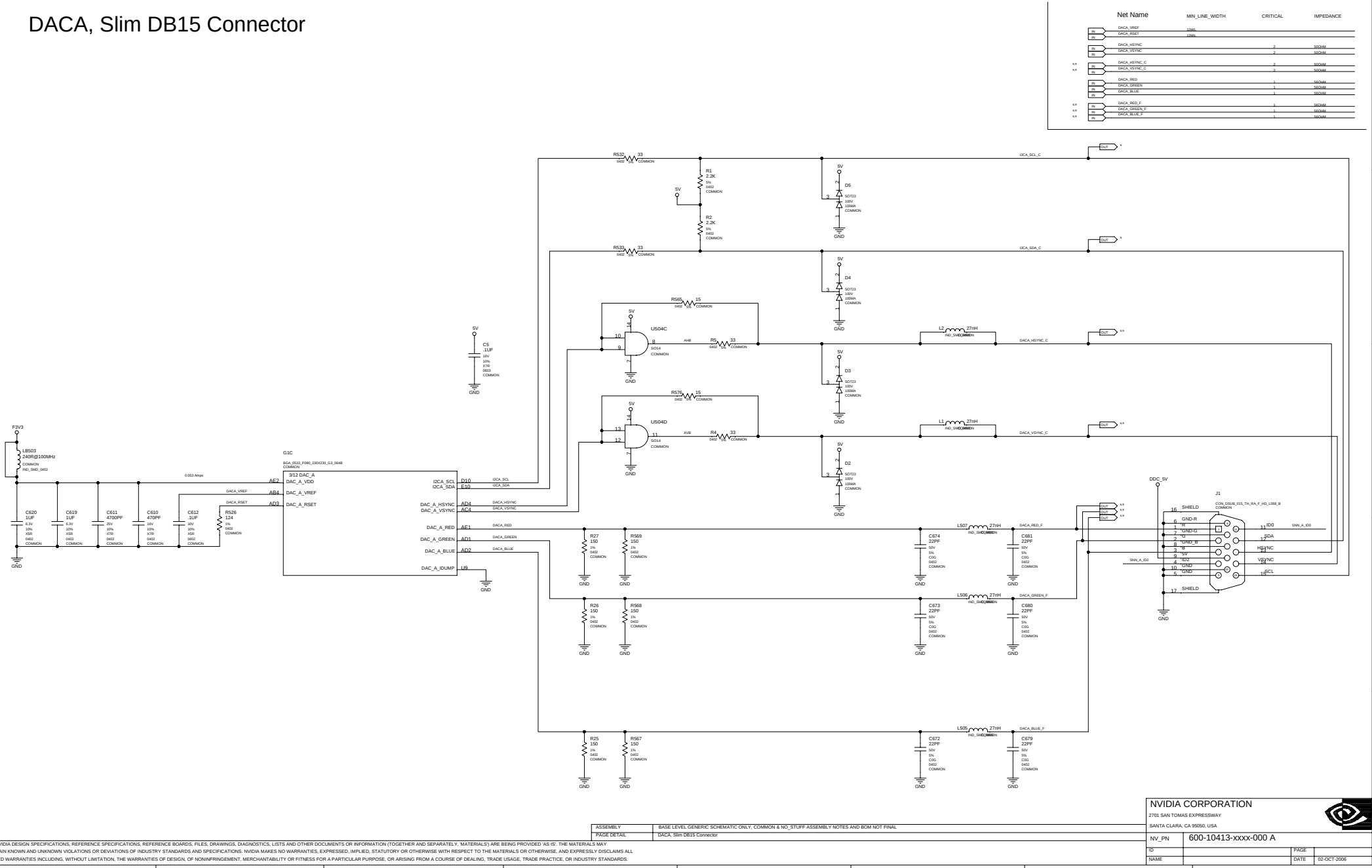
DACA, Slim DB15 Connector



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA_Slim DB15 Connector

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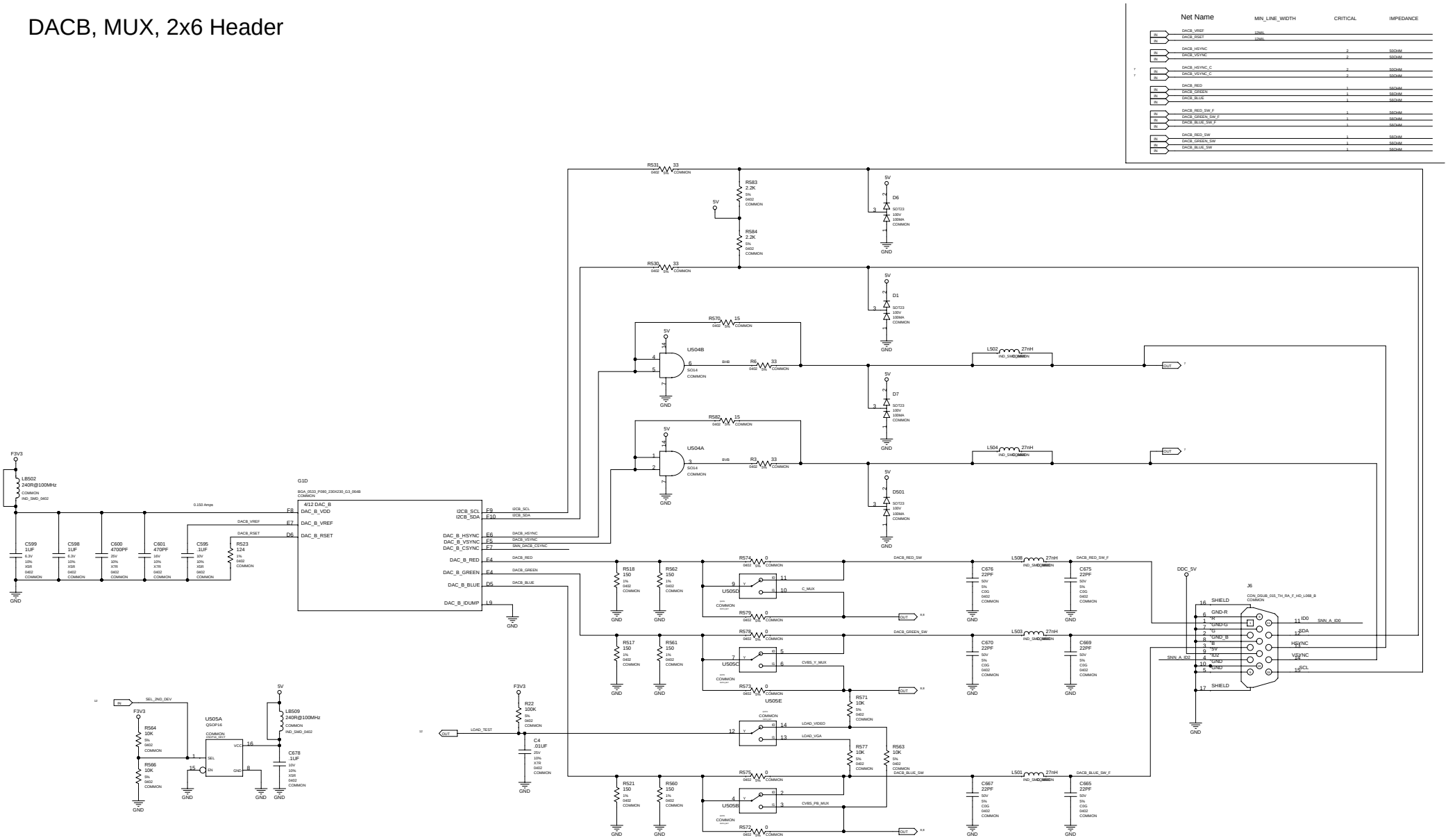
DACB, MUX, 2x6 Header



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB, MUX, 2x6 Header

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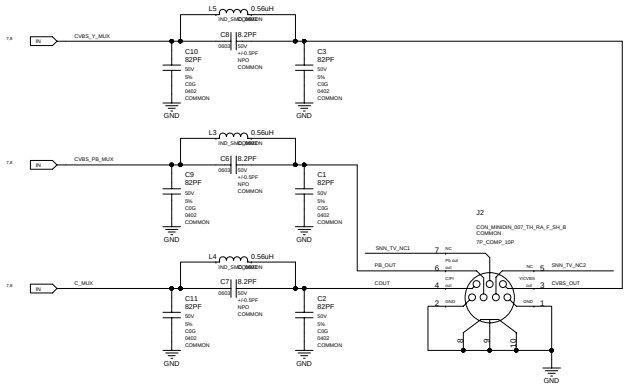
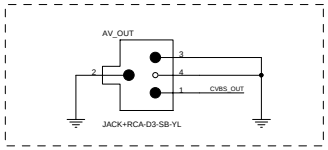
MiniDIN Connector

Net Name	CRITICAL	IMPEDANCE
C_MUX	1	50OHM
CVBS_Y_MUX	1	50OHM
CVBS_PB_MUX	1	50OHM
COUT	1	50OHM
CVBS_OUT	1	50OHM
PB_OUT	1	50OHM





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MiniDIN Connector

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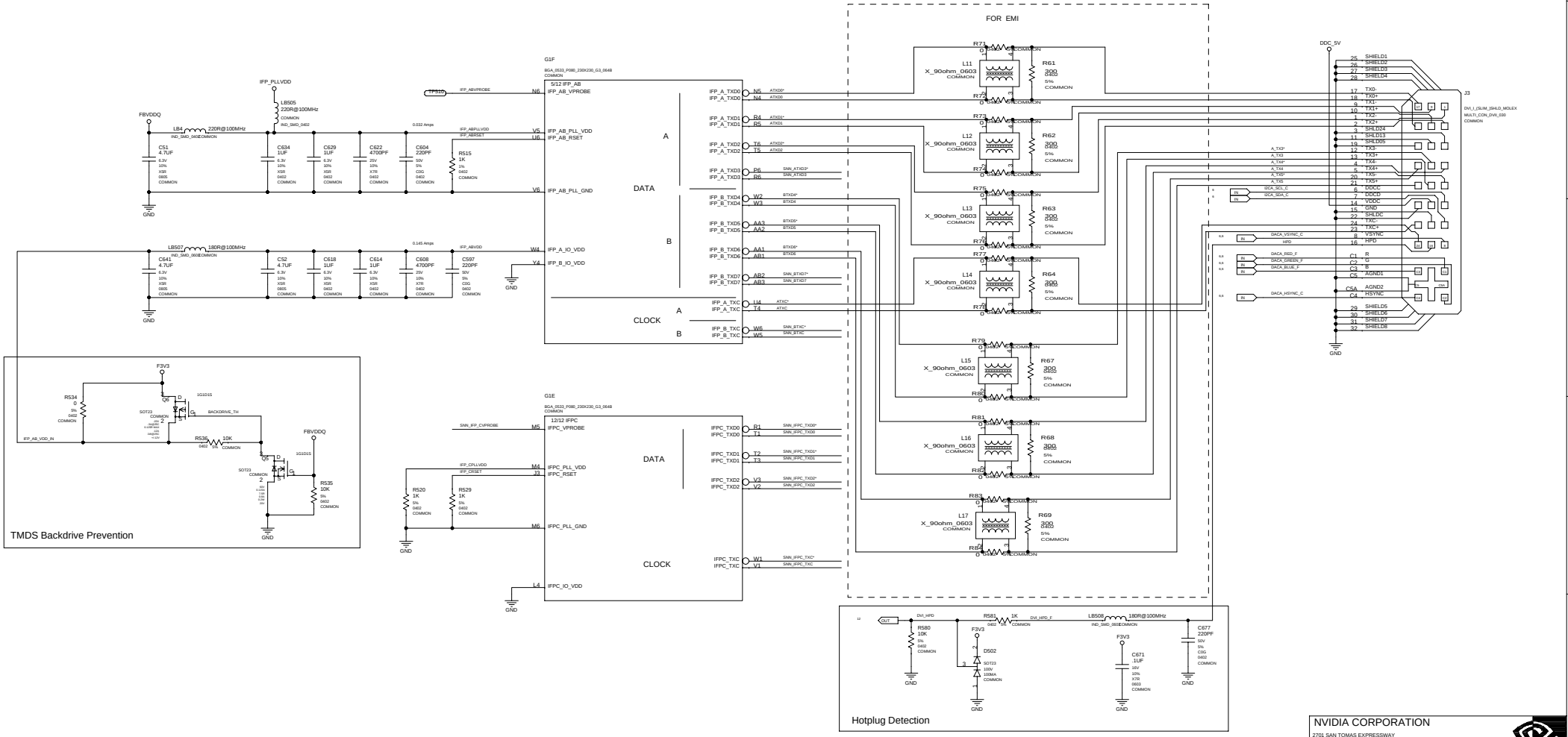
TMDS Interface

Net Name	DIFF_PAIR	CRITICAL	IMPEDANCE
ATXC	ATXC	1	100DIFF
ATXC*	ATXC	1	100DIFF
ATXD0	ATXD0	1	100DIFF
ATXD0*	ATXD0	1	100DIFF
ATXD1	ATXD1	1	100DIFF
ATXD1*	ATXD1	1	100DIFF
ATXD2	ATXD2	1	100DIFF
ATXD2*	ATXD2	1	100DIFF

Net Name	MIN_LINE_WIDTH	VOLTAGE
IFP_ABPLLVDD	16MIL	3.3V
IFP_ABVDD	16MIL	3.3V
IFP_ABVDD_IN	16MIL	3.3V



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS Interface

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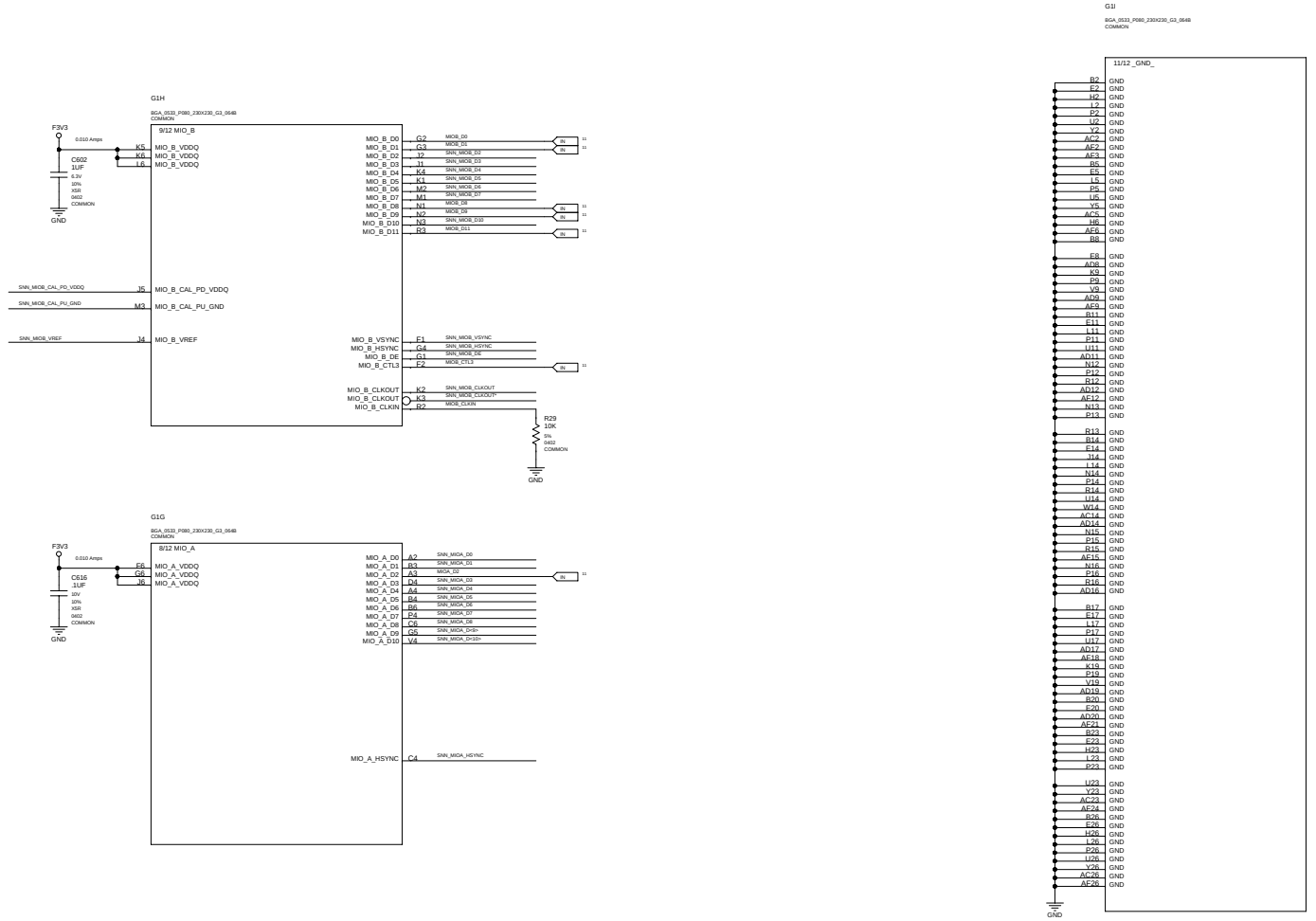
MIOA, MIOB Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA, MIOB Interface

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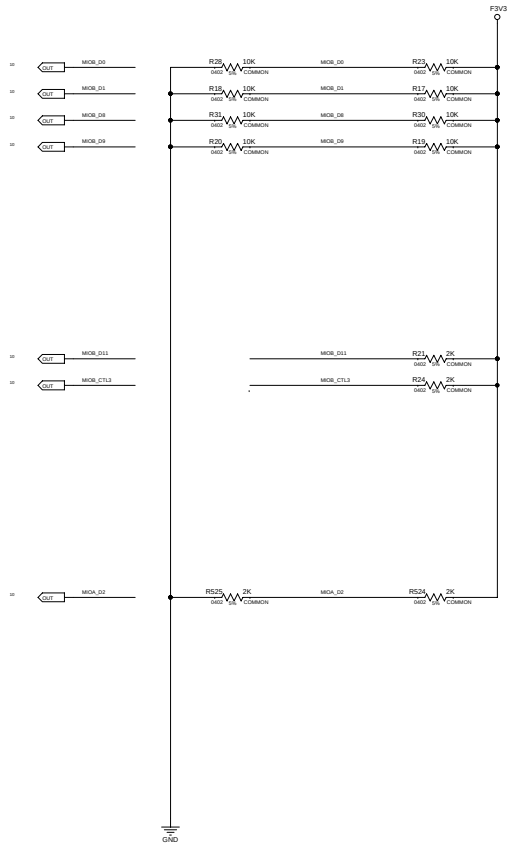
Straps, Mechanical Parts



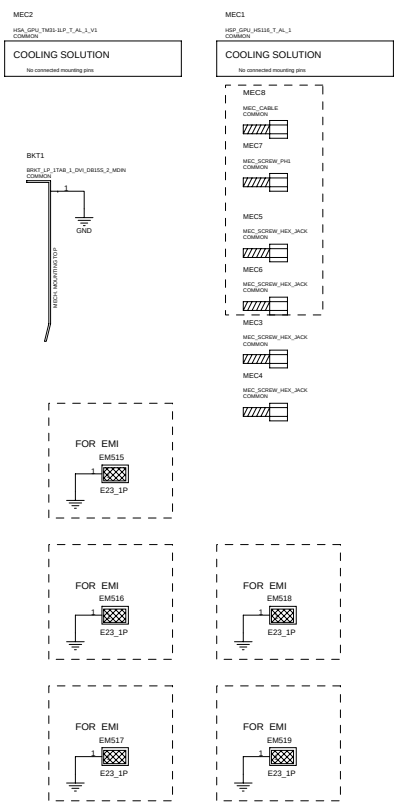
G86 Straps

Bit	Signal	Values			
01:	SUB_VENDOR	0 NO_BIOS 1 BIOS			
02:	RAM_CFG_0	0000	16Mx16 DDR2 64bit Elpida	1000	RFU
		0001	16Mx16 DDR2 64bit Samsung, Micron	1001	RFU
		0010	16Mx16 DDR2 64bit Infineon	1010	RFU
03:	RAM_CFG_1	0011	16Mx16 DDR2 64bit Hynix	1011	RFU
		0100	32Mx16 DDR2 64bit Elpida	1100	RFU
		0101	32Mx16 DDR2 64bit Samsung	1101	RFU
04:	RAM_CFG_2	0110	32Mx16 DDR2 64bit Infineon	1110	RFU
		0111	32Mx16 DDR2 64bit Hynix	1111	RFU
05:	RAM_CFG_3				
06:	CRYSTAL	0 27000K 1 14318K			
07:	TV_MODE_0	000 NTSC_M 001 NTSC_J 010 PAL_M 011 PAL_N 100 PAL_CN 101 PAL_BDGHI 110 RESERVED0 111 RESERVED1			
08:	TV_MODE_1				
09:	TV_MODE_2				
10:	PCI_DEVID_0	0010 (G86-200-A1: 0X0422) 0001 (G78-300-A1: 0X04C1)			
11:	PCI_DEVID_1				
12:	PCI_DEVID_2				
13:	PCI_DEVID_3				
	PCI_DEVID_4	G96 Strap			
17:	PEX_PLL_EN_TERM100	0 EN 1 DIS			
18:	3GIO_PADCFG_LUT_ADR_0	0000 DSKTOP_DEFAULT		1000 DSKTOP_HTHRS	
		0001 MOBILE_DEFAULT		1001 MOBILE_HTHRS_NAMP	
		0010 MOBILE_NTHRS_LLAMP		1010 MOBILE_HTHRS_LLAMP	
19:	3GIO_PADCFG_LUT_ADR_1	0011 MOBILE_NTHRS_LAMP		1011 MOBILE_HTHRS_LAMP	
		0100 MOBILE_NTHRS_HAMP		1100 MOBILE_HTHRS_HAMP	
		0101 MOBILE_NTHRS_HHAMP		1101 MOBILE_HTHRS_HHAMP	
20:	3GIO_PADCFG_LUT_ADR_2	0110 MOBILE_NTHRS_HHHAMP		1110 MOBILE_HTHRS_HHHAMP	
		0111 MOBILE_NTHRS_HHHHAMP		1111 MOBILE_HTHRS_HHHHAMP	
21:	3GIO_PADCFG_LUT_ADR_3				
22:	ROMTYPE_0	00 PARALLEL 01 SERIAL_AT25F 10 SERIAL_SST45VF			
23:	ROMTYPE_1	11 RESERVED			
24:	USER_0	0000 DEFAULT			
25:	USER_1				
26:	USER_2				
27:	USER_3				
12:	MIO_EN_33V_0	0 DISABLED 1 ENABLED			
13:	MIO_EN_33V_1	0 DISABLED 1 ENABLED			
15:	SLOT_CLK_CFG	0 DISABLED 1 ENABLED			
16:	PCI_IOBAR	0 DISABLED 1 ENABLED			
23:	BAR2_SIZE	0 32MB 1 16MB			

Pin Name
MIOAD1
MIOBD0
MIOBD1
MIOBD8
MIOBD9
MIOBD2
MIOAD7
MIOAD10
MIOBD6
MIOBD4
MIOBD5
MIOBD3
MIOBD11
MIOBCTL3
MIOAD0
MIOAD6
MIOAD8
MIOAD9
MIOB_HSYNC
MIOBD10
MIOB_VSYNC
MIOAD2
MIOAD3
MIOAD4
MIOAD5
ROM_SI
ROM_SCLK
MIOA_HSYNC
MIOBD7
MIOB_DE

G78 Straps

Bit	Signal	Values			
01:	SUB_VENDOR	0 NO_BIOS 1 BIOS			
02:	RAM_CFG_0	0000	16Mx16 DDR2 64bit Elpida	1000	16Mx16 DDR2 32bit Elpida
		0001	16Mx16 DDR2 64bit Samsung, Micron	1001	16Mx16 DDR2 32bit Samsung, Micron
		0010	16Mx16 DDR2 64bit Infineon	1010	16Mx16 DDR2 32bit Infineon
03:	RAM_CFG_1	0011	16Mx16 DDR2 64bit Hynix	1011	16Mx16 DDR2 32bit Hynix
		0100	32Mx16 DDR2 64bit Elpida	1100	32Mx16 DDR2 32bit Elpida
		0101	32Mx16 DDR2 64bit Samsung	1101	32Mx16 DDR2 32bit Samsung
04:	RAM_CFG_2	0110	32Mx16 DDR2 64bit Infineon	1110	32Mx16 DDR2 32bit Infineon
		0111	32Mx16 DDR2 64bit Hynix	1111	32Mx16 DDR2 32bit Hynix
05:	RAM_CFG_3				
06:	CRYSTAL	0 27000K OR 13500K 1 14318K OR UNKWN			
07:	TV_MODE_0	00 SECAM 01 NTSC 10 PAL 11 CRT			
08:	TV_MODE_1				
22:	CRYSTAL_1	0 13500K OR 14318K 1 27000K OR UNKWN			
12:	PCI_DEVID_0	TBD (G78: 0X????)			
13:	PCI_DEVID_1				
20:	PCI_DEVID_2				
21:	PCI_DEVID_3				
	PCI_DEVID_4				
11:	PEX_PLL_EN_TERM100	0 EN 1 DIS			
12:	3GIO_PADCFG_LUT_ADR_0	000 DEFAULT 001 MOBILE 010 MOBILE_LPWR			
13:	3GIO_PADCFG_LUT_ADR_1	011 MOBILE_LOWEST_PWR 100 MOBILE_LTHR 101 MOBILE_HTHR			
14:	3GIO_PADCFG_LUT_ADR_2	110 MOBILE_LTHR_LPWR 111 MOBILE_HTHR_LPWR			
16:	SLOT_CLK_CFG	0 PULLDN 1 INIT			
29:	ROMTYPE_0	00 PARALLEL 01 SERIAL_AT25F 10 SERIAL_SST45VF			
30:	ROMTYPE_1	11 LPC			
16:	USER_0	0000 DEFAULT			
17:	USER_1				
18:	USER_2				
19:	USER_3				
25:	BR	0 ENABLED 1 DISABLED			
15:	MOBILE_GPIO	0 PULLDN 1 FLOAT			



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Straps, Mechanical Parts

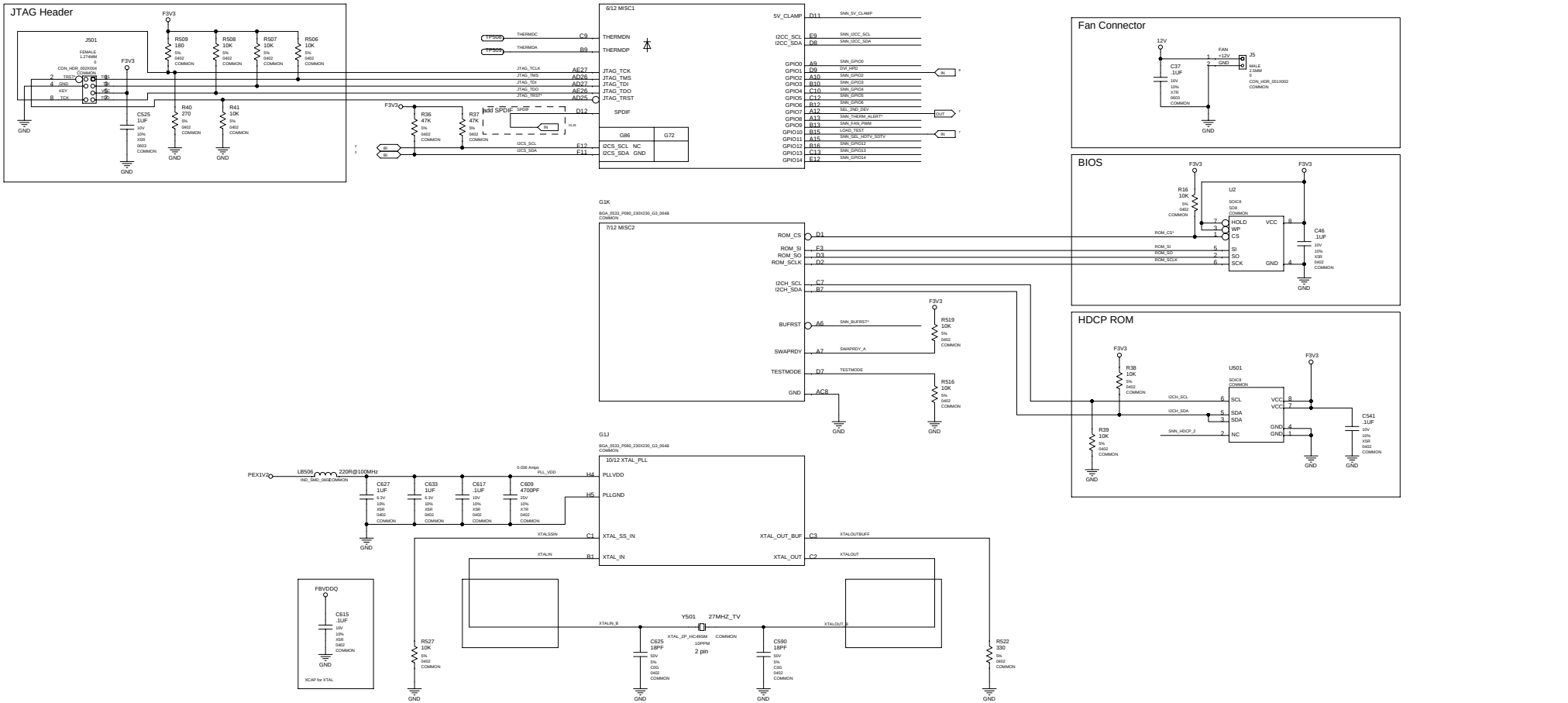
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10413-xxxx-000 A		
ID		PAGE	
NAME		DATE	02-OCT-2006

XTAL, GPIO, BIOS, FAN, JTAG, HDCP

Net Name	CRITICAL	IMPEDANCE
XTALIN	1	50OHM
XTALOUT	1	50OHM
XTALIN_T	1	50OHM
XTALOUT_T	1	50OHM
XTALIN_B	1	50OHM
XTALOUT_B	1	50OHM

Net Name	MIN_LINE_WIDTH	VOLTAGE
PLL_VDD	12MIL	1.2V



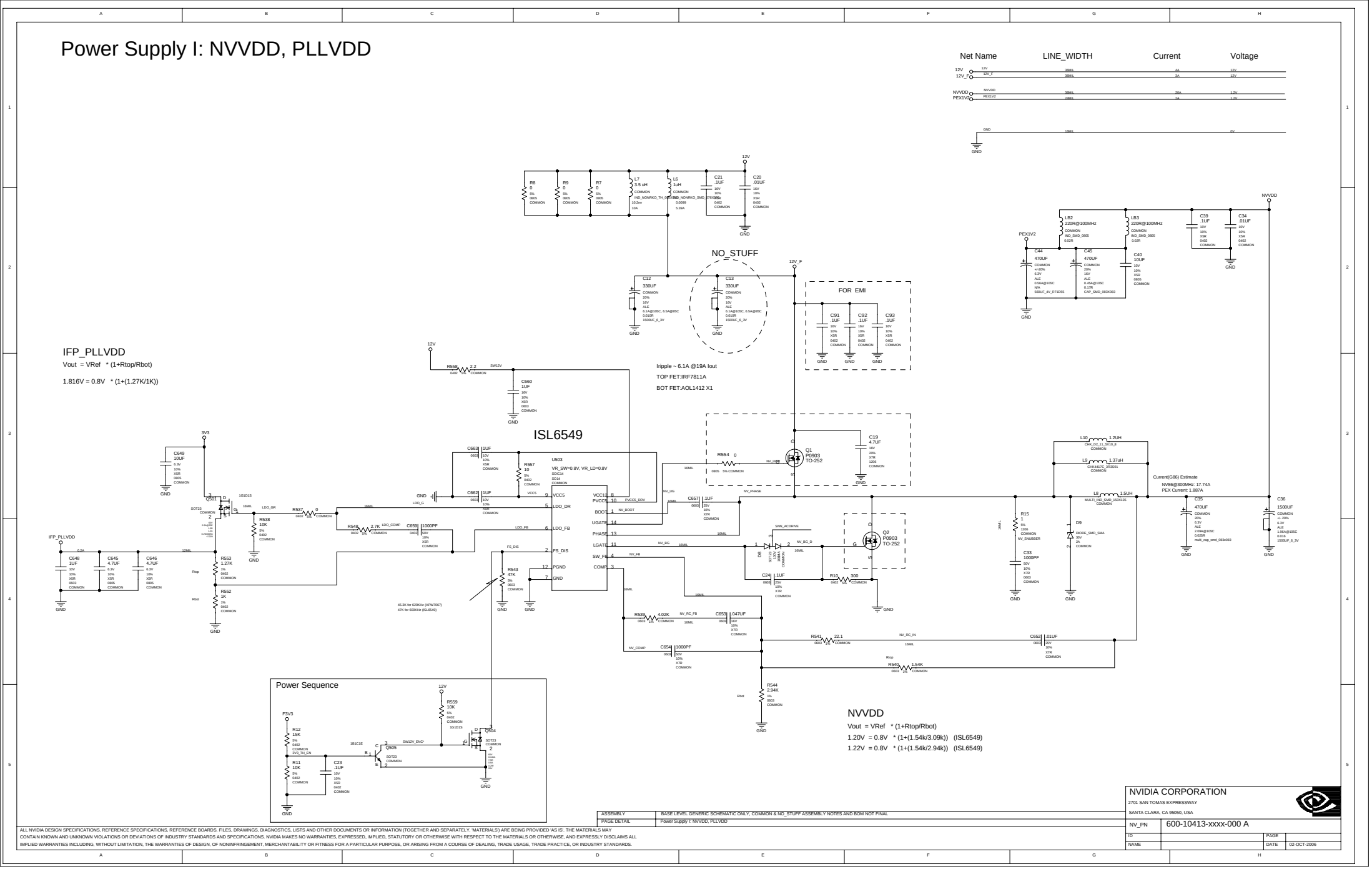
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, GPIO, BIOS, FAN, JTAG, HDCP

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10413-xxxx-000 A		
ID		PAGE	
NAME		DATE	02-OCT-2006

Power Supply I: NVVDD, PLLVDD

Net Name	LINE_WIDTH	Current	Voltage
12V	20MIL	4A	12V
12V_F	20MIL	3A	12V
NVVDD	30MIL	20A	1.2V
PEX1V2	24MIL	2A	1.2V
GND	16MIL		0V



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply I: NVVDD, PLLVDD

NVIDIA CORPORATION
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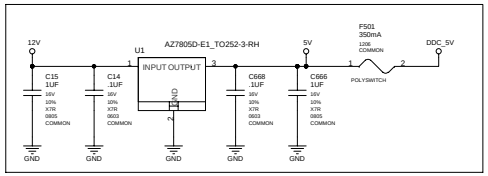
NV_PN	600-10413-xxxx-000 A		
ID		PAGE	
NAME		DATE	02-OCT-2006

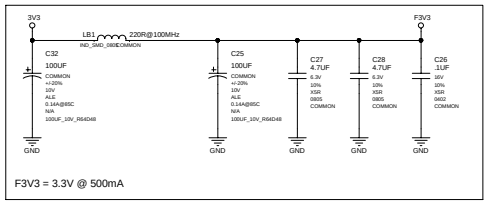
Power Supply II: 5V, DDC5V, F3V3, FBVDDQ

Net Name	MIN_LINE_WIDTH	CURRENT	VOLTAGE
5V DDC_5V	5V DDC_5V	12MIL 12MIL	0.25A 0.2A	5V 5V
F3V3 3V3	F3V3 3V3	12MIL 36MIL	1A 3A	3.3V 3.3V
FBVDDQ	FBVDDQ	36MIL	2A	2.0V

5V, DDC5V



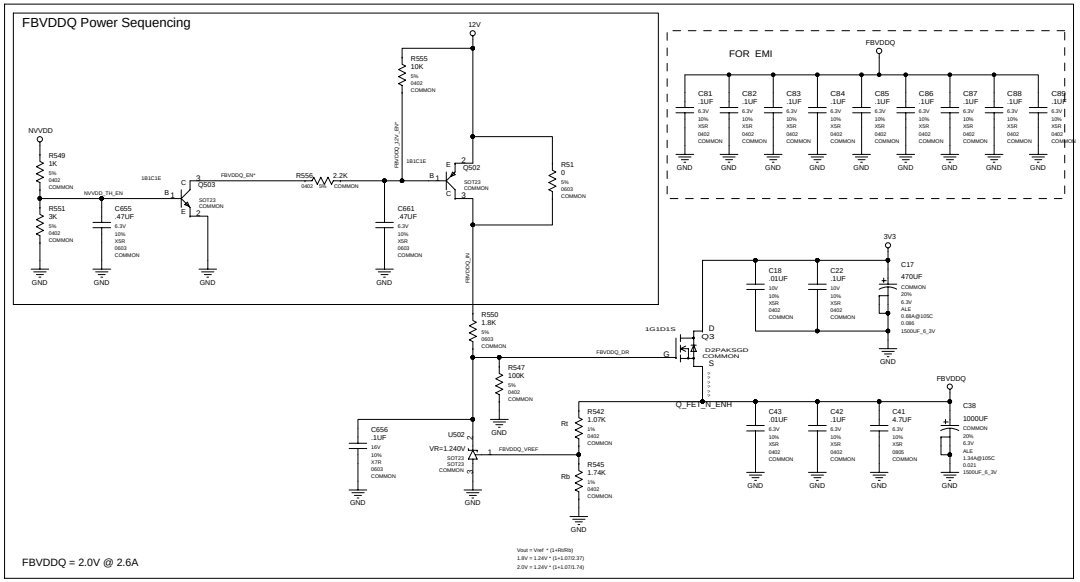
F3V3



F3V3 = 3.3V @ 500mA

FBVDDQ

FBVDDQ Power Sequencing



FBVDDQ = 2.0V @ 2.6A

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply II: F3V3, 5V, DDC5V, FBVDDQ

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10413-xxxx-000 A		
ID		PAGE	
NAME		DATE	02-OCT-2006

Title: Basenet Report
Design: p413
Date: Sep 29 14:42:41 2006

Base nets and synonyms for
p413_lib.P413(@p413_lib.p413(sch_1))
Base Signal Location([Zone][dir])

3V3 14.1G
3V3_TH_EN 13.5B
5V 14.1G
12V 13.1F
12V_F 13.1F
AHB 6.2E
ATXC 9.1G< 9.3E 9.3G
ATXC* 9.1G< 9.3E 9.3G
ATXD0 9.1G< 9.2E 9.2G
ATXD0* 9.1G< 9.2E 9.2G
ATXD1 9.1G< 9.2E 9.2G
ATXD1* 9.1G< 9.2E 9.2G
ATXD2 9.1G< 9.2E 9.2G
ATXD2* 9.1G< 9.2E 9.2G
AVB 6.3E
BACKDRIVE_TH 9.4B
BHB 7.2E
BVB 7.3E
COUT 8.1G< 8.3E
CVBS_OUT 8.1G< 8.3E
CVBS_PB_MUX 7.5F> 8.1G< 8.3C<
CVBS_Y_MUX 7.4F> 8.1G< 8.2C<
C_MUX 7.4F> 8.1G< 8.3C<
DACA_BLUE 6.1G< 6.4C
DACA_BLUE_F 6.4G> 6.1G< 9.3G<
DACA_GREEN 6.1G< 6.4C
DACA_GREEN_F 6.3G> 6.1G< 9.3G<
DACA_HSYNC 6.1G< 6.3C
DACA_HSYNC_C 6.2G> 6.1G< 9.3G<
DACA_RED 6.1G< 6.4C
DACA_RED_F 6.3G> 6.1G< 9.3G<
DACA_RSET 6.1G< 6.3B
DACA_VREF 6.1G< 6.3B
DACA_VSYNC 6.1G< 6.3C
DACA_VSYNC_C 6.3G> 6.1G< 9.3G<
DACB_BLUE 7.1G< 7.4C
DACB_BLUE_SW 7.1G< 7.5E
DACB_BLUE_SW_F 7.1G< 7.5F
DACB_GREEN 7.1G< 7.4C
DACB_GREEN_SW 7.1G< 7.4E
DACB_GREEN_SW_F 7.1G< 7.4F
DACB_HSYNC 7.1G< 7.3C
DACB_HSYNC_C 7.3G> 7.1G<
DACB_RED 7.1G< 7.4C
DACB_RED_SW 7.1G< 7.4E
DACB_RED_SW_F 7.1G< 7.4F
DACB_RSET 7.1G< 7.3B
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DDC_5V 14.1G
DDR_ODT 3.4F> 3.1G< 4.2A< 4.2C< 5.2A< 5.2C<
DVI_HPD 9.3E> 12.2F<
DVI_HPD_F 9.3F
F3V3 14.1G
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FBADQSN<7> 3.4B 5.1G 5.4D
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FBA_PLLAVDD 3.5C
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FBCAL_PU_GND 3.4C
FBCAL_TERM_GND 3.4C
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FBVDDQ_DR 14.3F
FBVDDQ_EN* 14.3E
FBVDDQ_IN 14.3F
FBVDDQ_VREF 14.4F
FBVREF 3.5B
FS_DIS 13.4C
HPD 9.3G
I2CA_SCL 6.3C
I2CA_SCL_C 6.1G> 9.2G<
I2CA_SDA 6.3C
I2CA_SDA_C 6.2G> 9.3G<
I2CB_SCL 7.3C
I2CB_SCL_C 7.1F
I2CB_SDA 7.3C
I2CB_SDA_C 7.2F
I2CH_SCL 12.3E 12.3G
I2CH_SDA 12.3E 12.4G
I2CS_SCL 2.1E<> 12.2C<>
I2CS_SDA 2.1E<> 12.2C<>
IFP_ABPLLVDD 9.1G< 9.2C
IFP_ABRSET 9.2C
IFP_ABVDD 9.1G< 9.3C
IFP_ABVDD_IN 9.1G<
IFP_ABVPROBE 9.2C
IFP_AB_VDD_IN 9.4A
IFP_CPLLVDD 9.4C
IFP_CRSET 9.4C
JTAG_TCLK 12.2C
JTAG_TDI 12.2C
JTAG_TDO 12.2C
JTAG_TMS 12.2C
JTAG_TRST* 12.2C
LDO_COMP 13.4C
LDO_FB 13.4C
LDO_G 13.3C
LDO_GR 13.3B
LOAD_TEST 7.5C> 12.2F<
LOAD_VGA 7.5E
LOAD_VIDEO 7.4E
MIOA_D2 11.4A> 10.3D< 11.4B
MIOB_CLKIN 10.3C
MIOB_CTL3 11.3A> 10.2D< 11.3B
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MIOB_D1 11.2A> 10.2D< 11.2B
MIOB_D8 11.2A> 10.2D< 11.2B
MIOB_D9 11.2A> 10.2D< 11.2B
MIOB_D11 11.3A> 10.2D< 11.3B
NVVDD 13.1F
NVVDD_TH_EN 14.3D
NV_BG 13.4D
NV_BG_D 13.4E
NV_BOOT 13.3D
NV_COMP 13.4D
NV_FB 13.4D
NV_PHASE 13.3E
NV_RC_FB 13.4D
NV_RC_IN 13.4F
NV_SNUBBER 13.4G
NV_UG 13.3E
NV_UGR 13.3E
PB_OUT 8.1G< 8.3E
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PEX_JTAGE_TDIO 2.1C
PEX_PLL_DVDD 2.5F
PEX_PWRGD* 2.2C

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PEX_RX3 2.3C 2.4A<
PEX_RX3* 2.3C 2.4A<
PEX_RX4 2.3C 2.4A<
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PEX_RX10* 2.4C 2.5A<
PEX_RX11 2.4C 2.5A<
PEX_RX11* 2.4C 2.5A<
PEX_RX12 2.4C 2.5A<
PEX_RX12* 2.4C 2.5A<
PEX_RX13 2.5A< 2.5C
PEX_RX13* 2.5A< 2.5C
PEX_RX14 2.5A< 2.5C
PEX_RX14* 2.5A< 2.5C
PEX_RX15 2.5A< 2.5C
PEX_RX15* 2.5A< 2.5C
PEX_SMCLK 2.1C
PEX_SMDAT 2.1C
PEX_TSTCLK 2.2A< 2.2E
PEX_TSTCLK* 2.2A< 2.2E
PEX_TX0 2.2A< 2.2E
PEX_TX0* 2.2A< 2.2E
PEX_TX1 2.2A< 2.2E
PEX_TX1* 2.2A< 2.2E
PEX_TX2 2.2A< 2.2E
PEX_TX2* 2.2A< 2.2E
PEX_TX3 2.2A< 2.3E
PEX_TX3* 2.2A< 2.3E
PEX_TX4 2.2A< 2.3E
PEX_TX4* 2.2A< 2.3E
PEX_TX5 2.2A< 2.3E
PEX_TX5* 2.2A< 2.3E
PEX_TX6 2.2A< 2.3E
PEX_TX6* 2.2A< 2.3E
PEX_TX7 2.2A< 2.3E
PEX_TX7* 2.2A< 2.3E
PEX_TX8 2.3A< 2.4E
PEX_TX8* 2.3A< 2.4E
PEX_TX9 2.3A< 2.4E
PEX_TX9* 2.3A< 2.4E
PEX_TX10 2.3A< 2.4E
PEX_TX10* 2.3A< 2.4E
PEX_TX11 2.3A< 2.4E
PEX_TX11* 2.3A< 2.4E
PEX_TX12 2.3A< 2.4E
PEX_TX12* 2.3A< 2.4E
PEX_TX13 2.3A< 2.5E
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PEX_TX14 2.3A< 2.5E
PEX_TX14* 2.3A< 2.5E
PEX_TX15 2.3A< 2.5E
PEX_TX15* 2.3A< 2.5E
PEX_TX0 2.2C 2.3A<
PEX_TX0* 2.2C 2.3A<
PEX_TX1 2.2C 2.3A<
PEX_TX1* 2.2C 2.3A<
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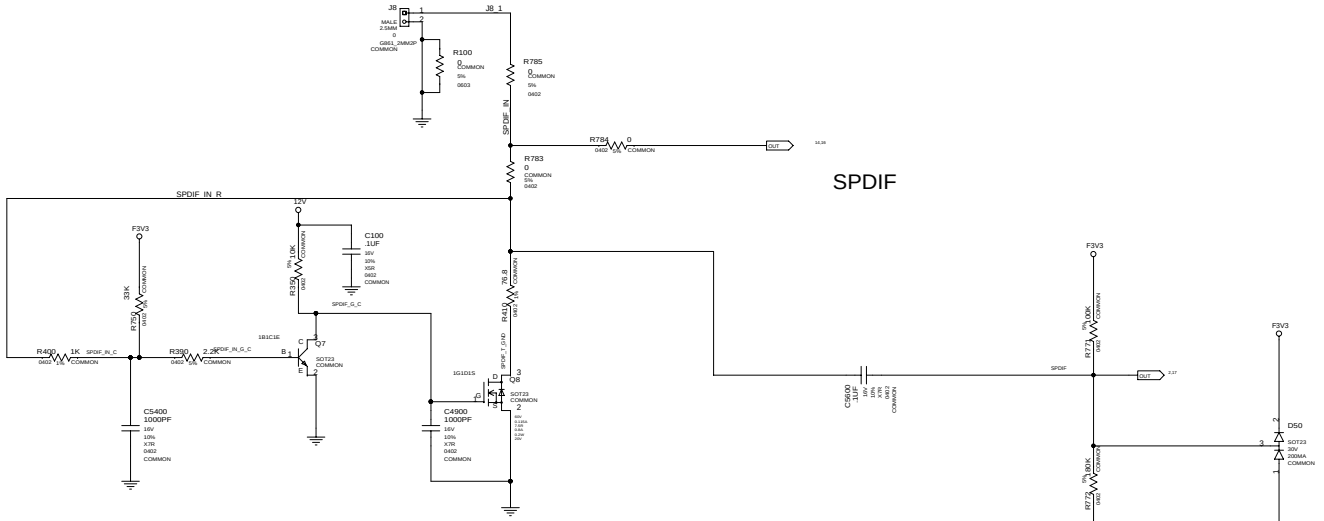

SPDIF

place close to GPU

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF

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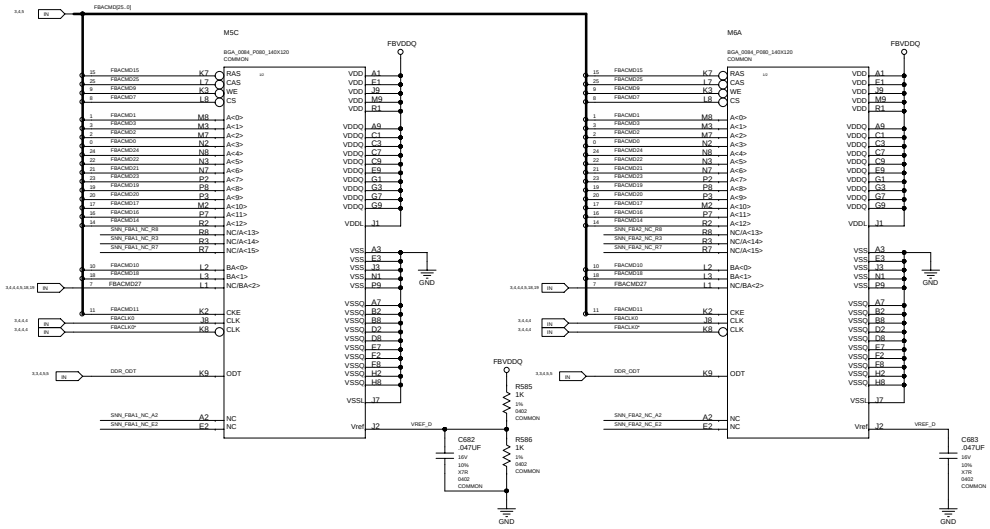
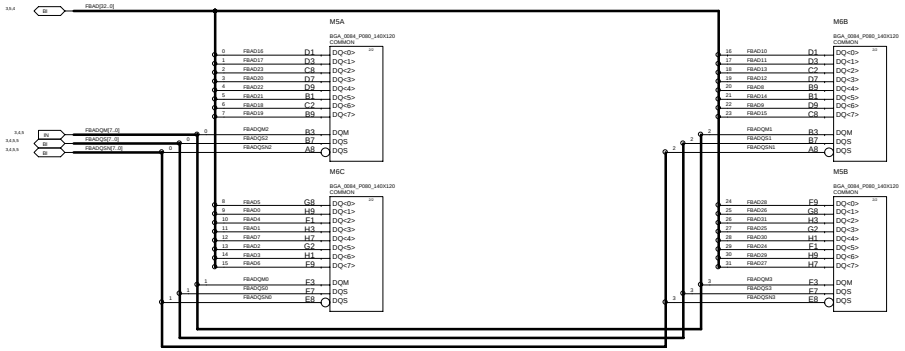
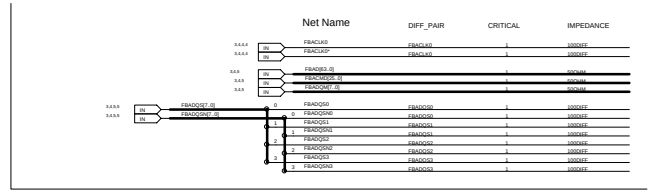
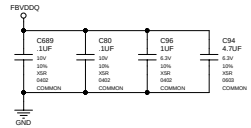
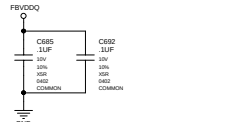
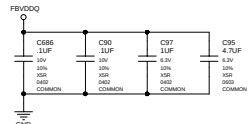


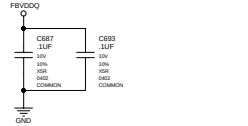




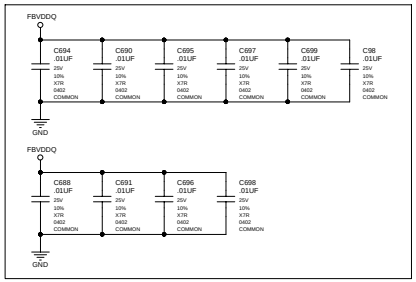




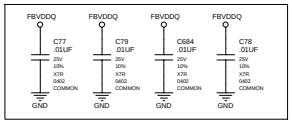




X-cap for CMD



Place these caps next to plane transitions



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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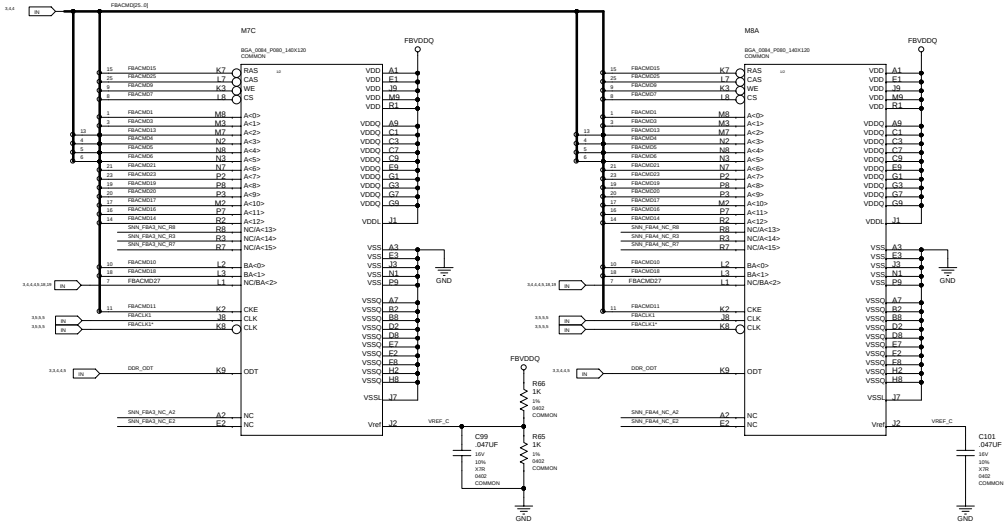
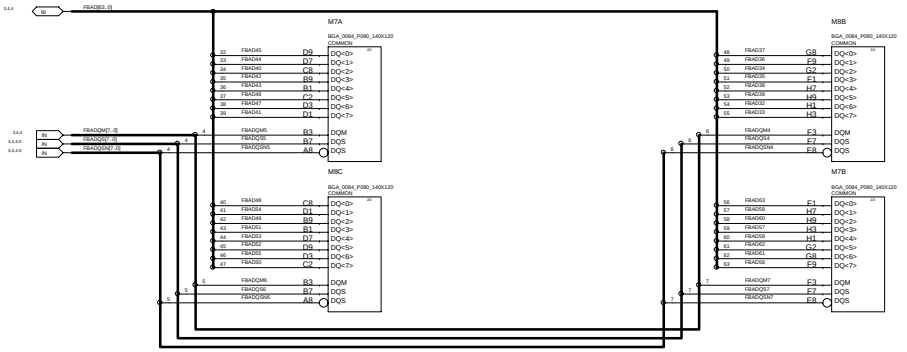
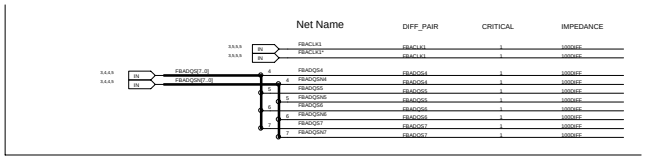
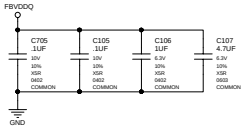
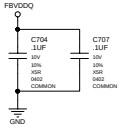
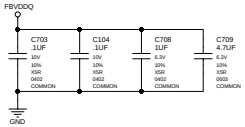


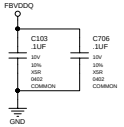




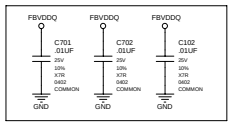








Place near signal transition area



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co-layout co-layout

PowerSupplyIII: FBVDDQ

APW7065 I32-0706502-A30
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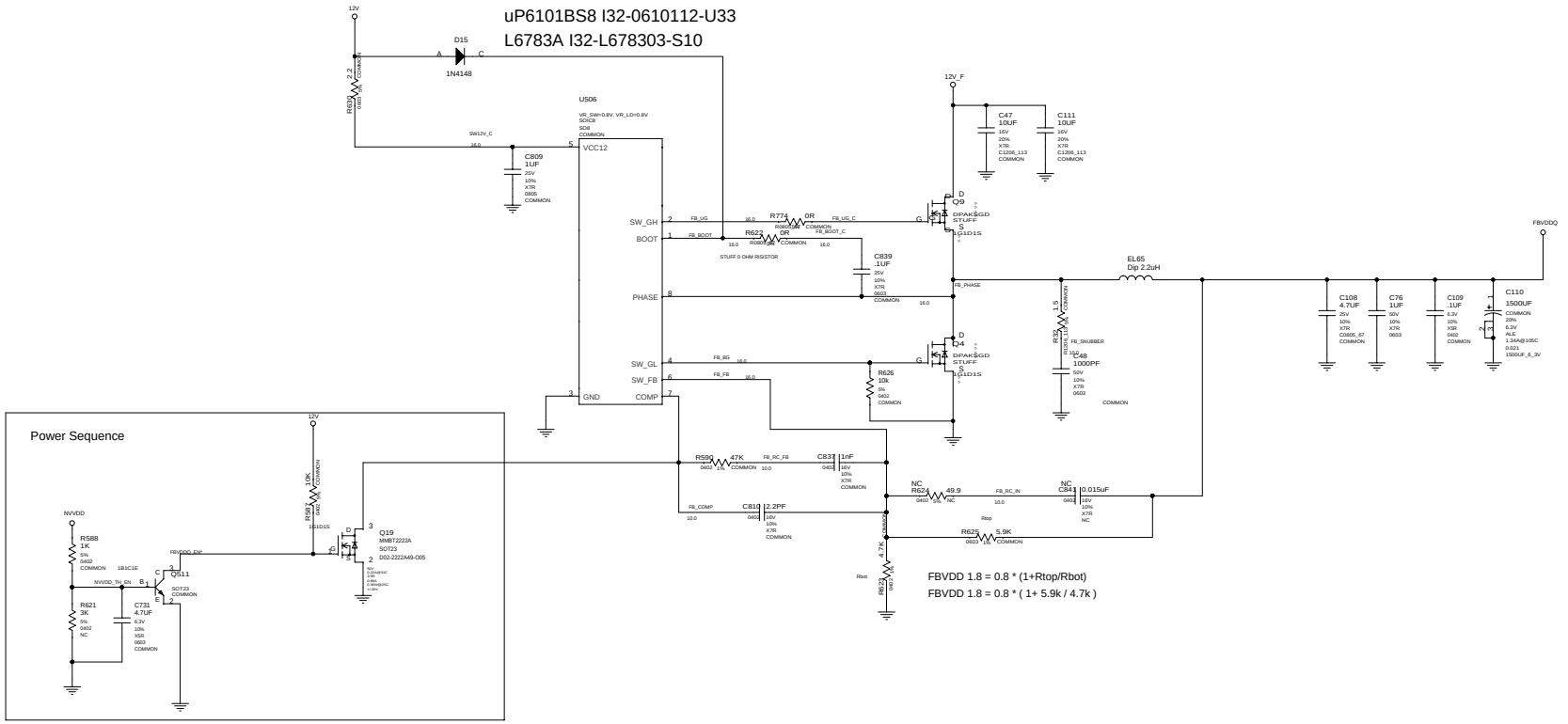

FBVDD 1.8 = 0.8 * (1+Rtop/Rbot)
FBVDD 1.8 = 0.8 * (1+ 5.9k / 4.7k)

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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