

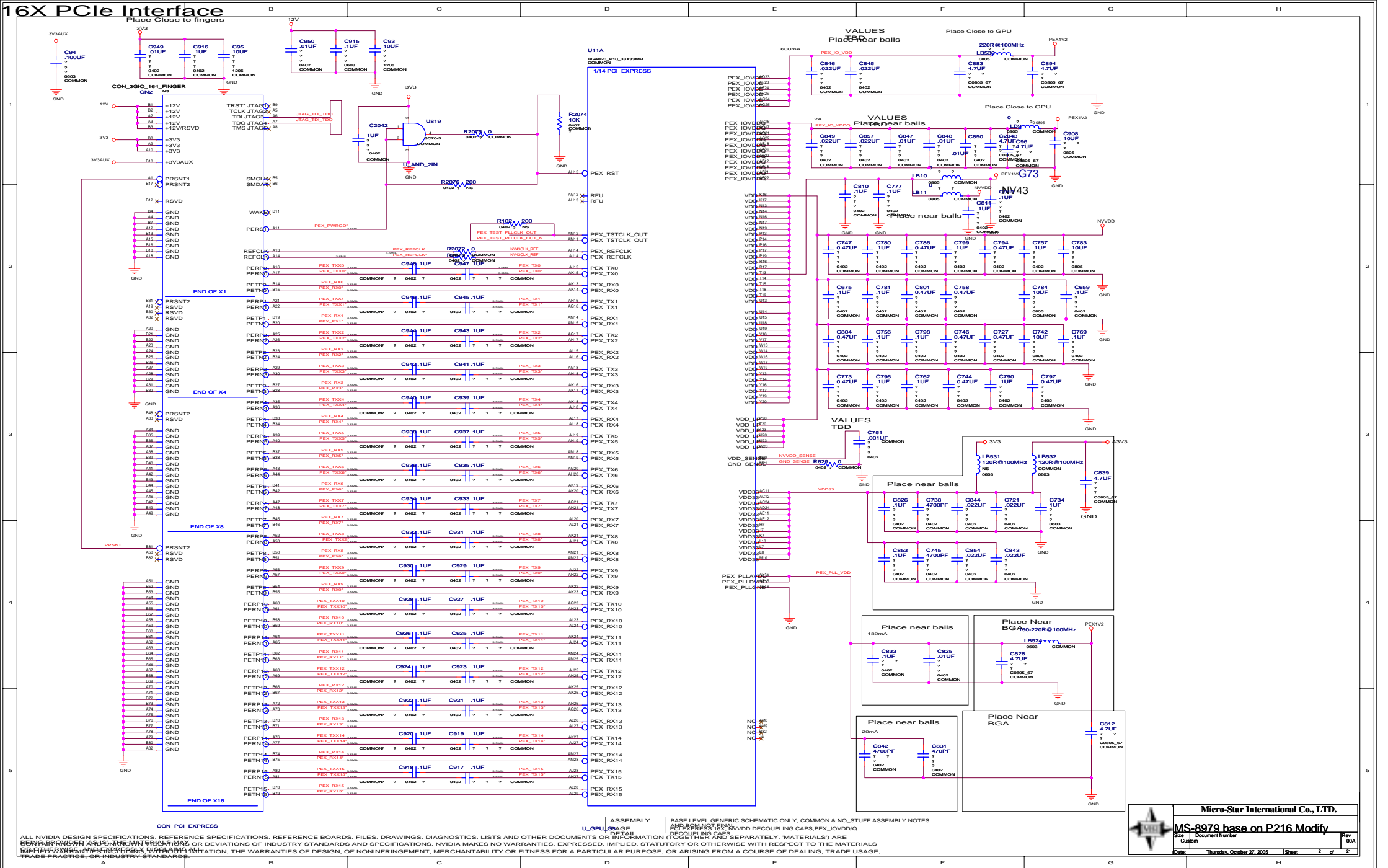
V053-0A DESIGN BASE ON V035 DESIGN

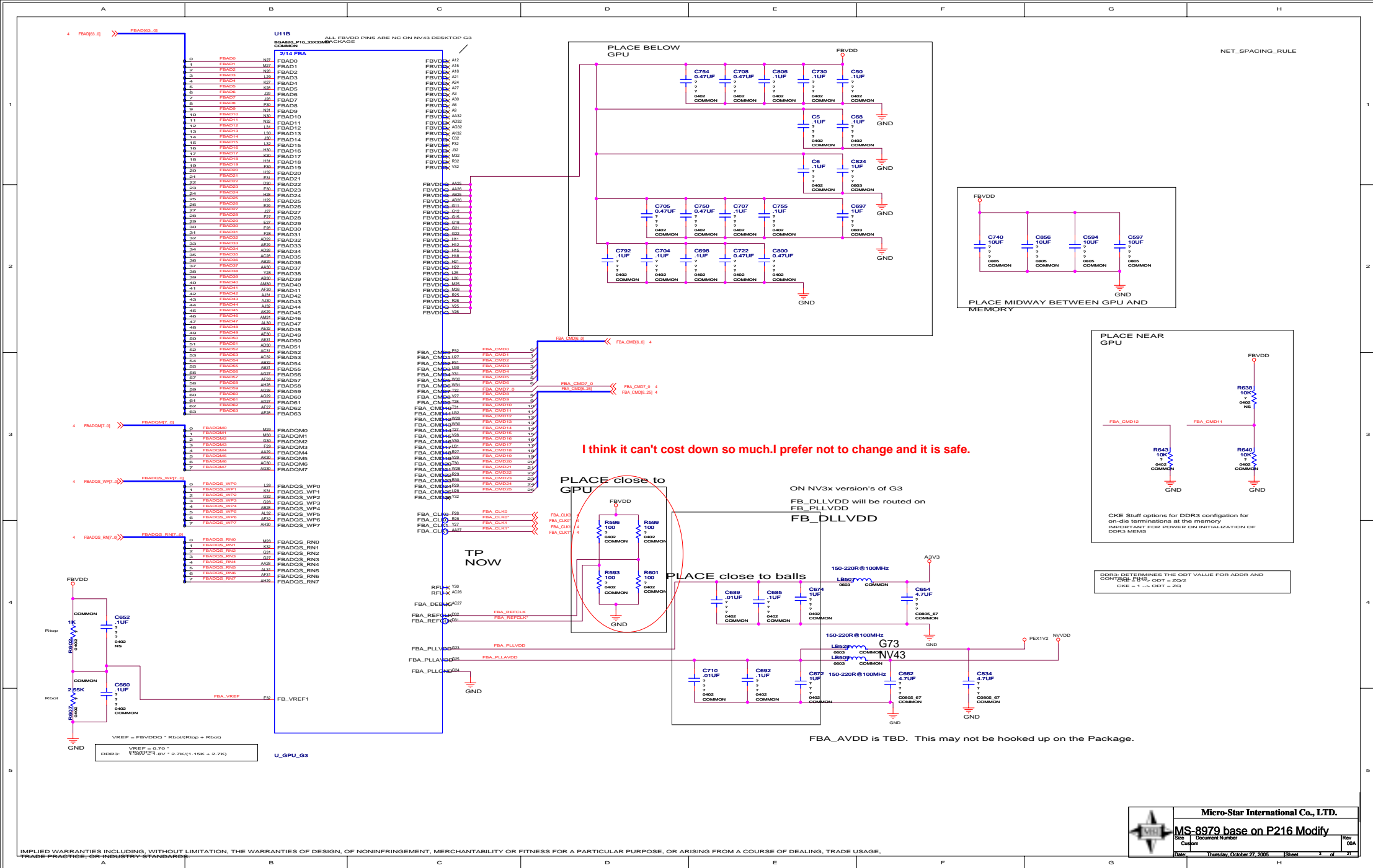
PAGE SUMMARY:

PAGE SUMMARY:

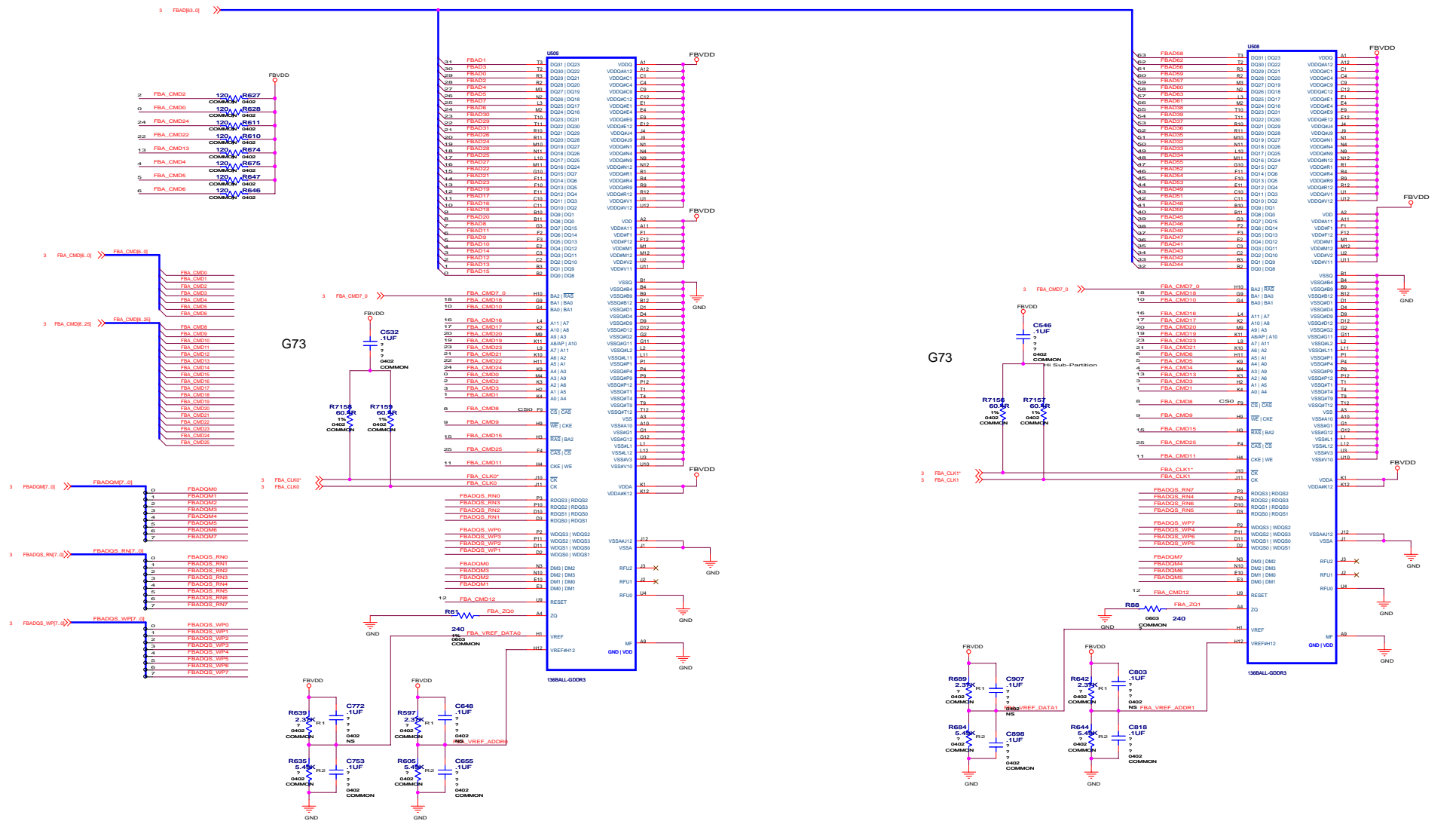
- PAGE03
- PAGE04
- PAGE06
- PAGE07

16X PCIe Interface



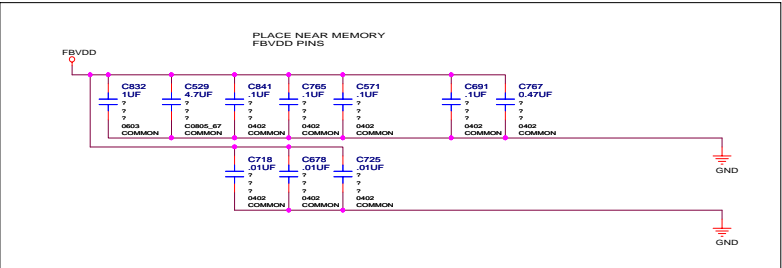


5 FrameBuffer: Partition A 8Mx32 BGA144 DDR3

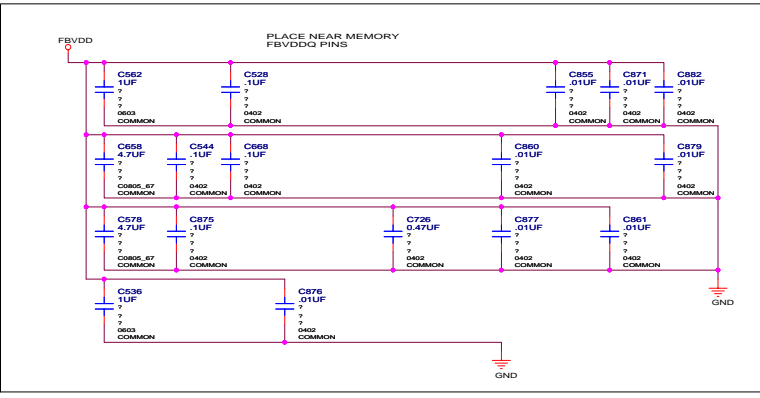
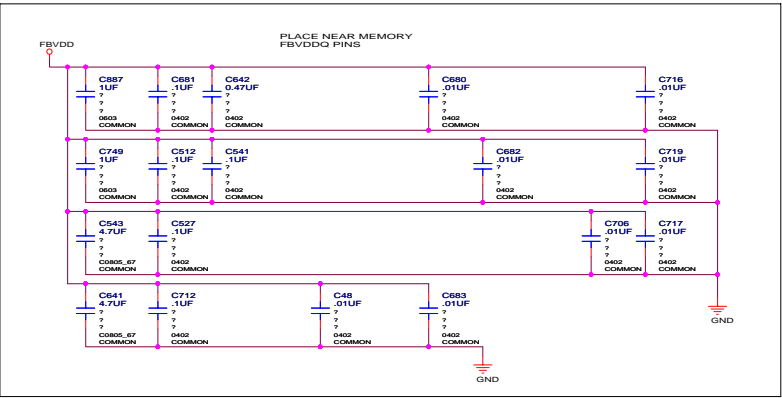
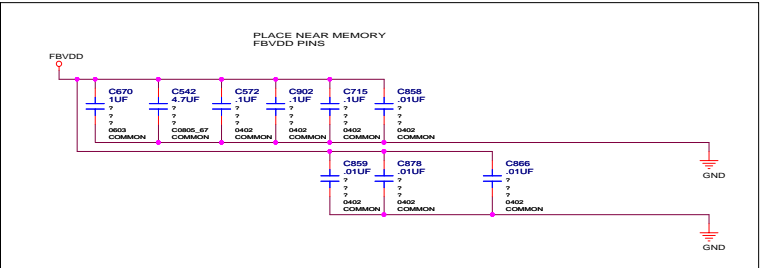


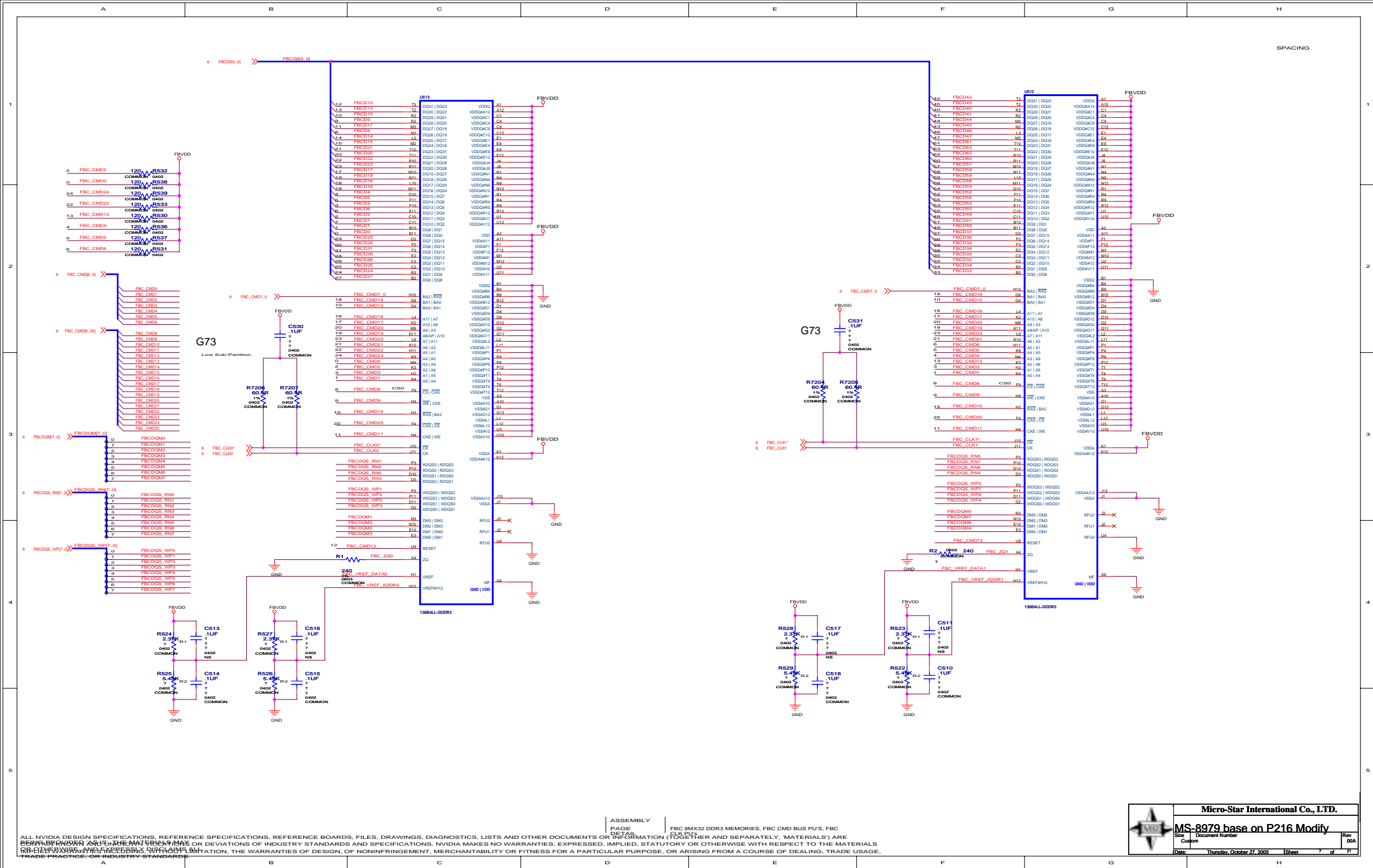
FRAME BUFFER: PARTITION A
DECOUPLING

Decoupling for FBA 0..31



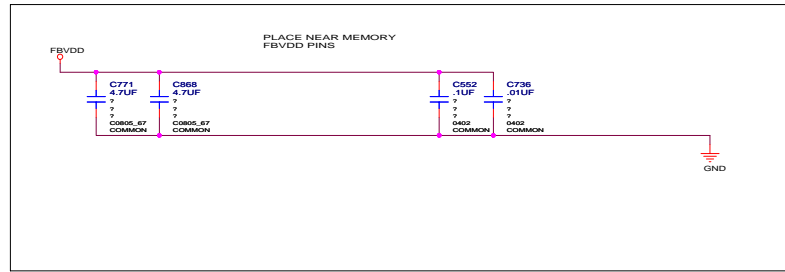
Decoupling for FBA 32..63



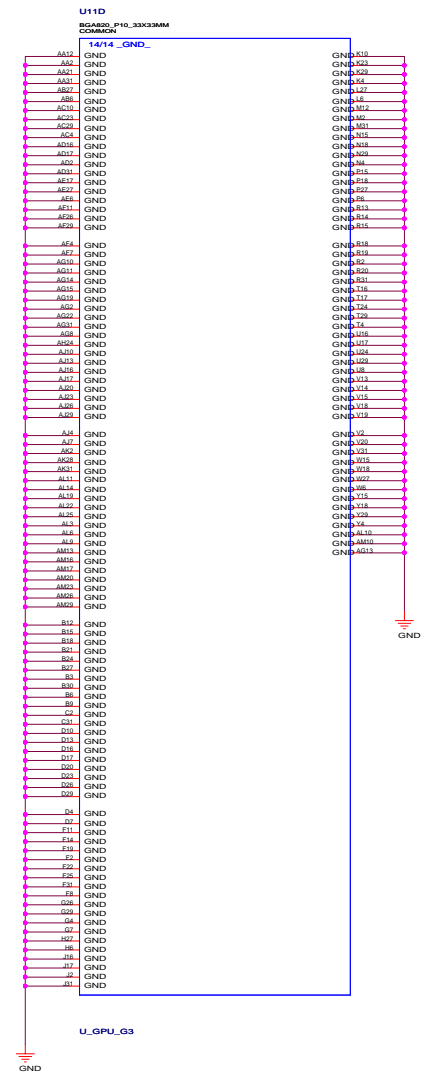
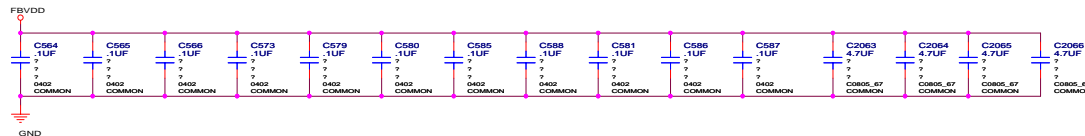
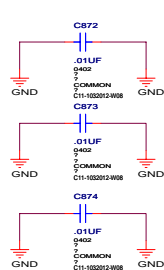
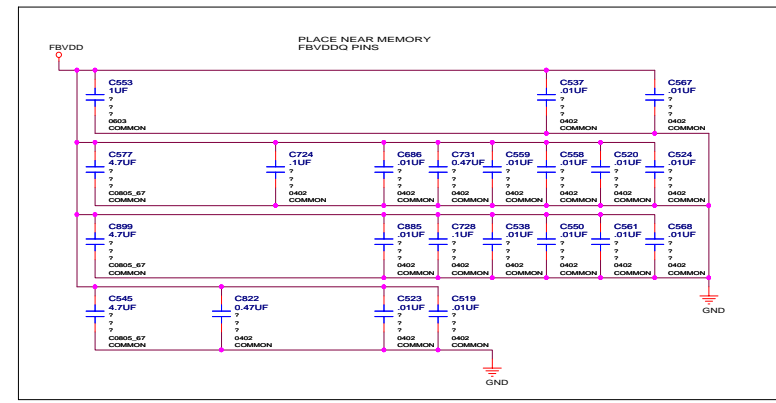
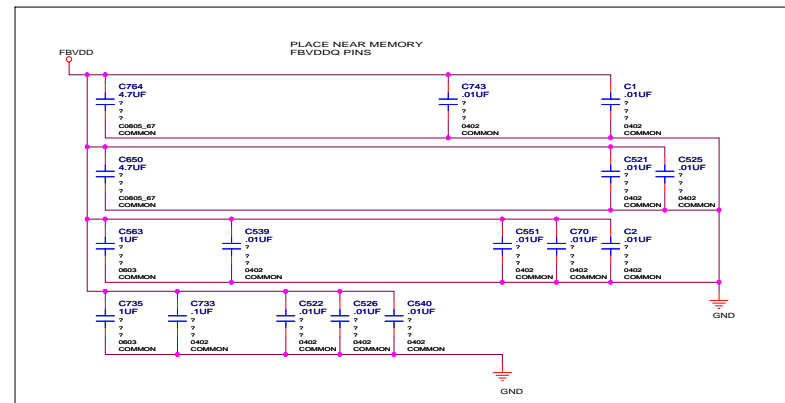
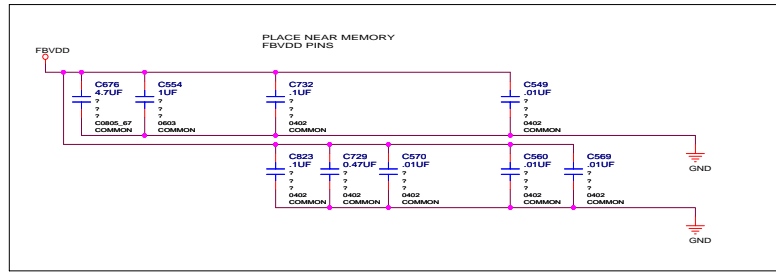


FRAMEBUFFER: PARTITION C DECOUPLING

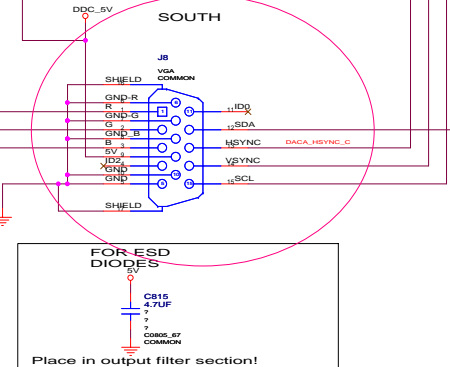
Decoupling for FBC 0..31




Decoupling for FBC 32..63



DACA
RGB-FILTER

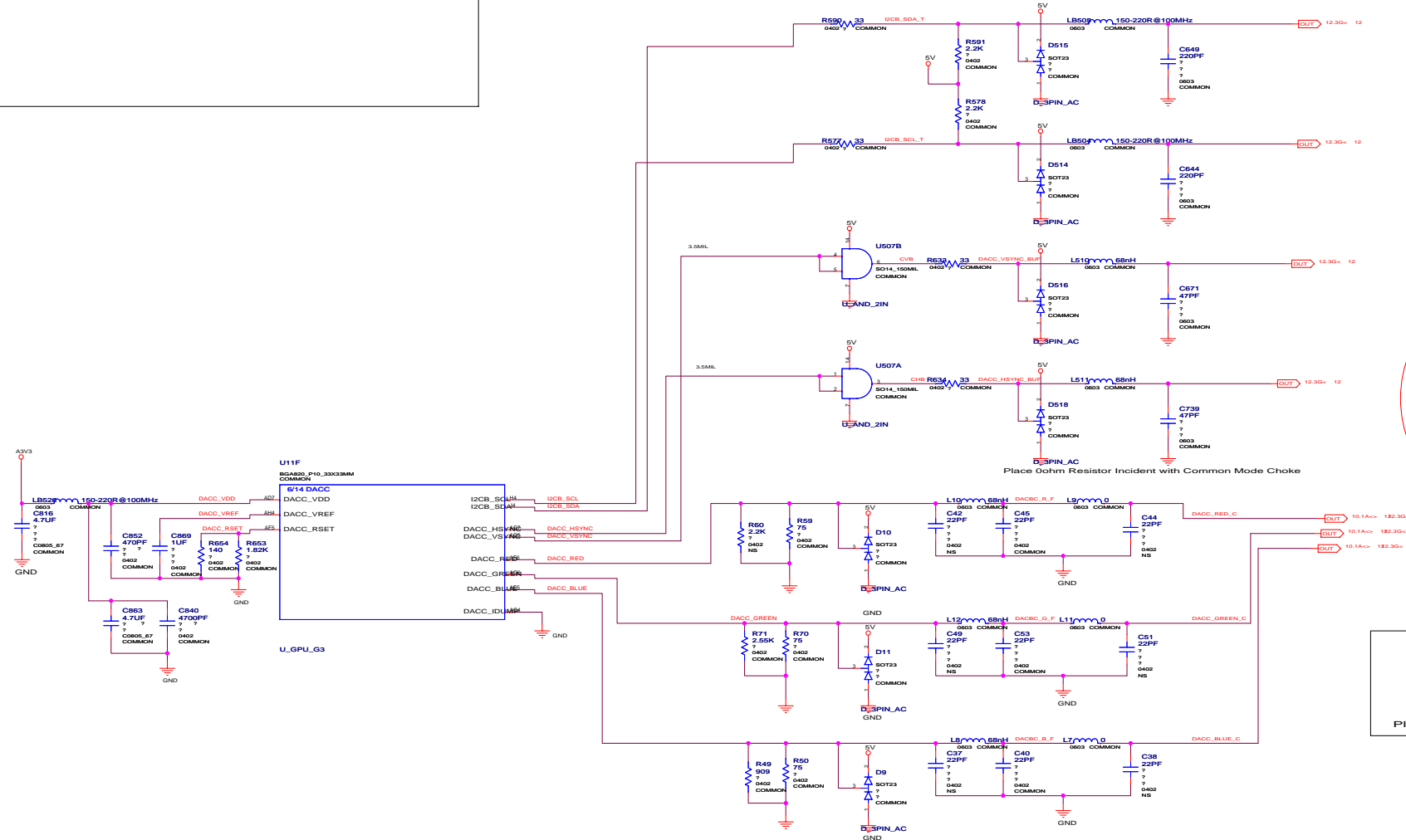


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Secondary Display
(DACC), To DVI-I

DACC
RGB-FILTER



FOR ES
DIODES



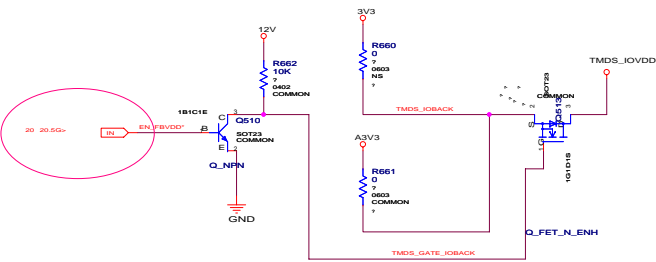
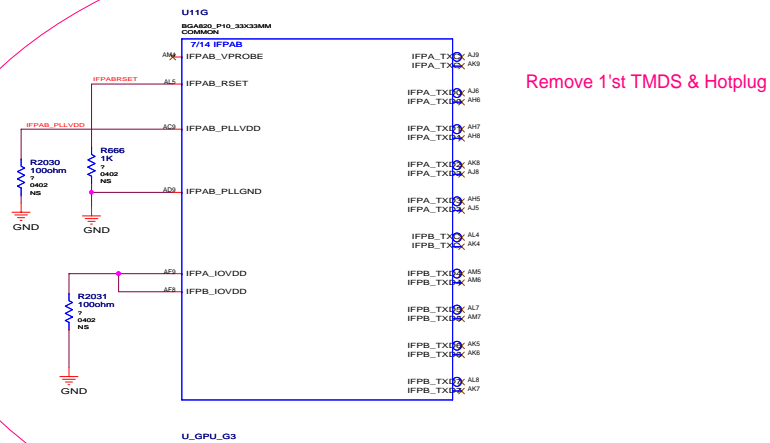
Place in output filter section!

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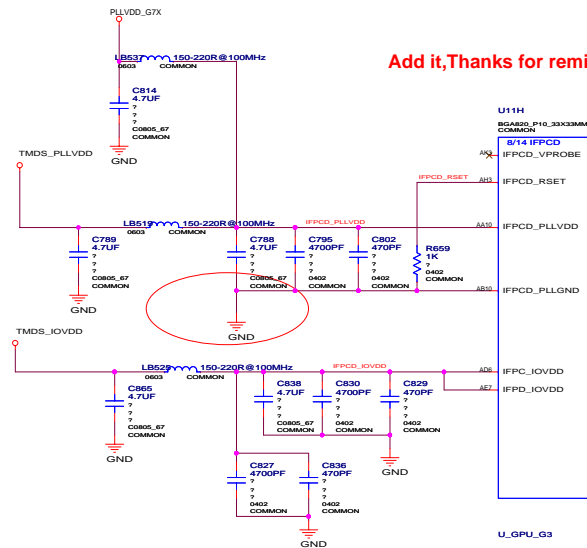
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INTERNAL TMD S .. LINK A & B

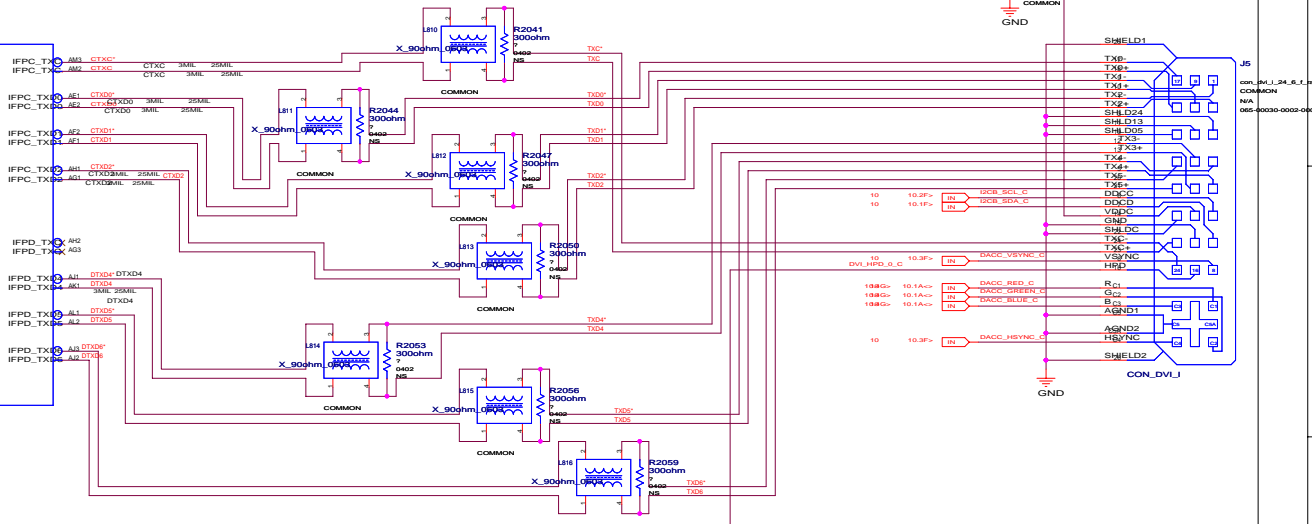
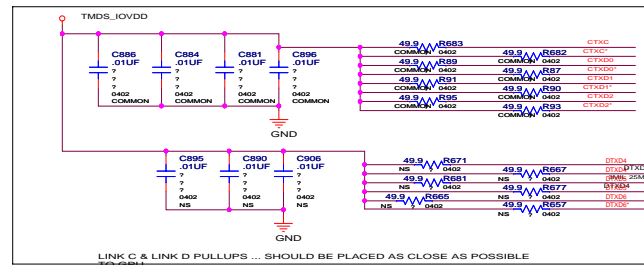


Net name change from 5v_ENBL* to EN_FBVD*

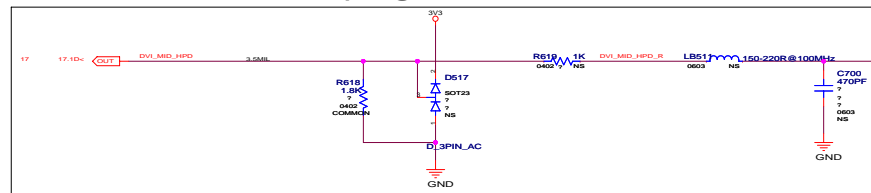
INTERNAL TMDS .. LINK C & D



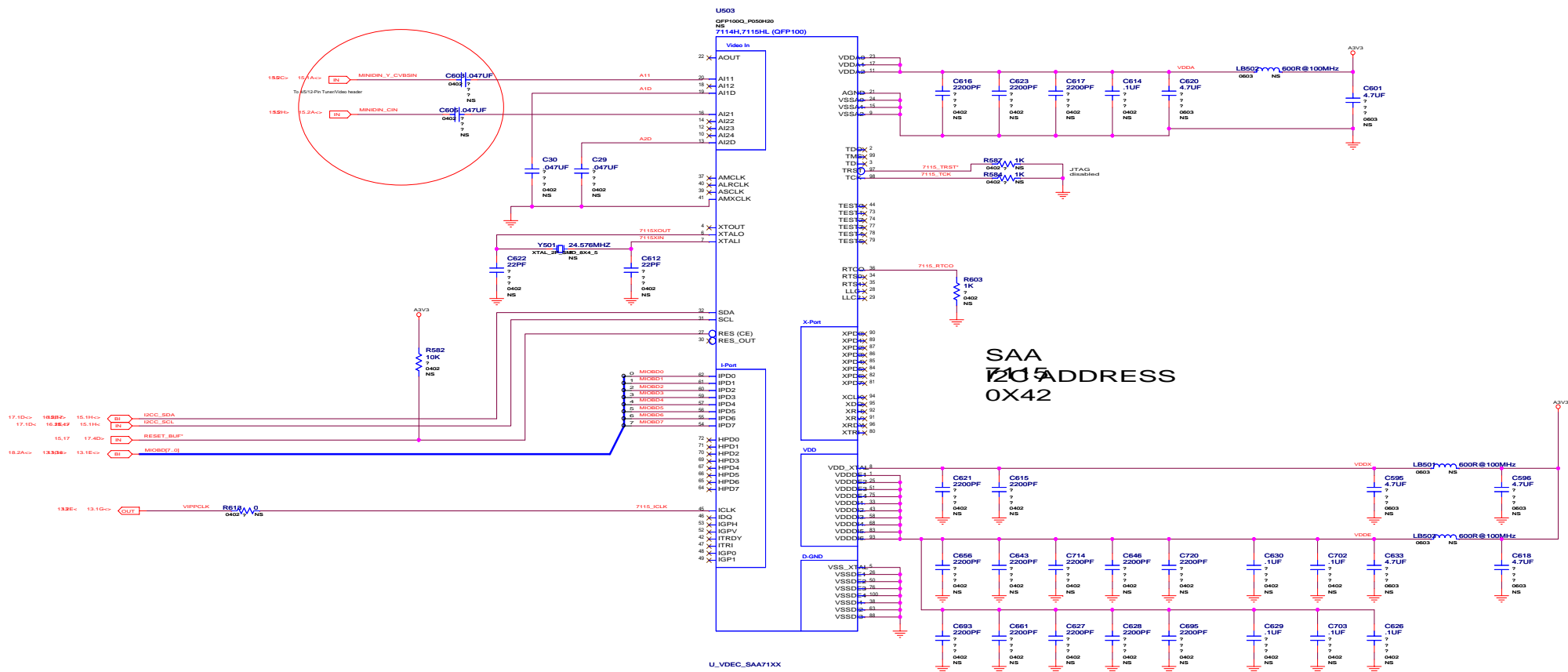
Add it,Thanks for remind it.



Hotplug Detection



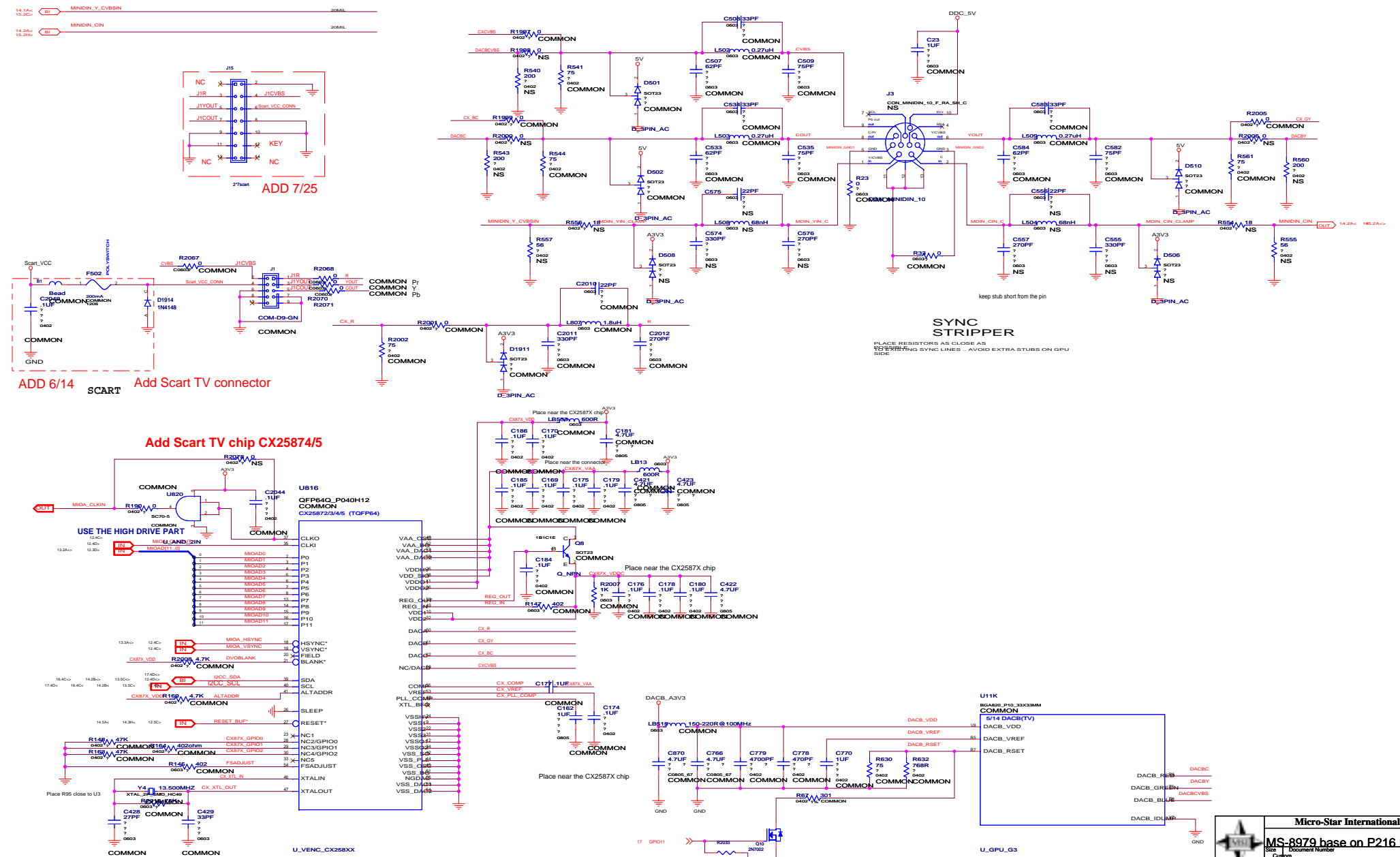
PHILIPS VIDEO CAPTURE

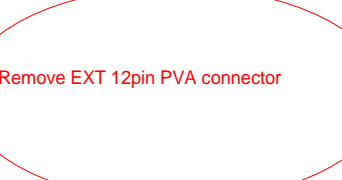


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DACB .. MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES



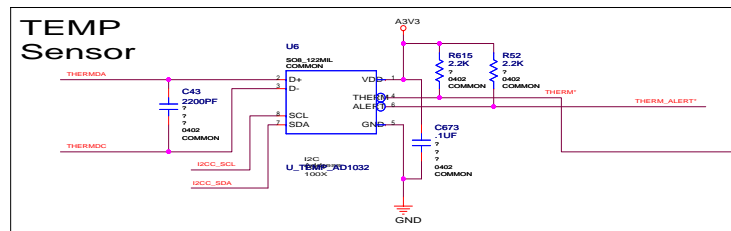
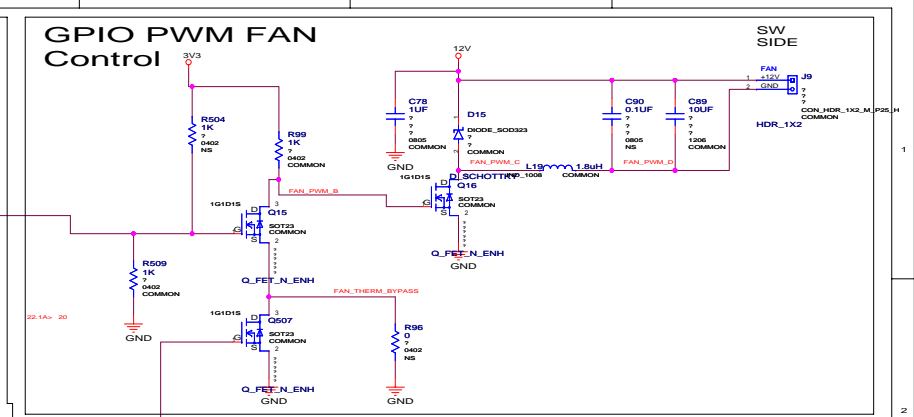
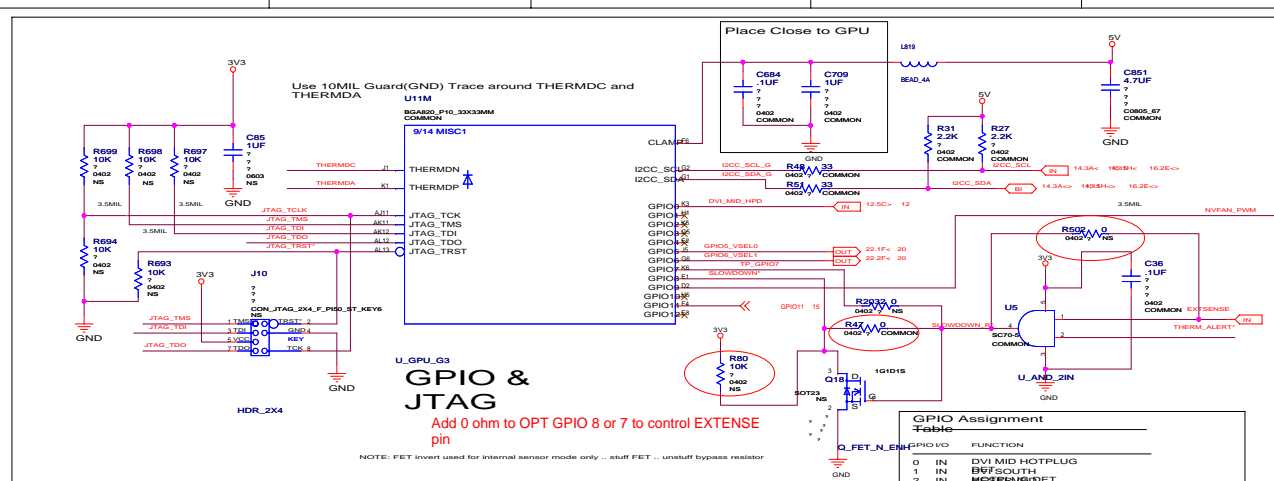
A large red oval graphic that frames the text "Remove EXT 12pin PVA connector".

Remove EXT 12pin PVA connector

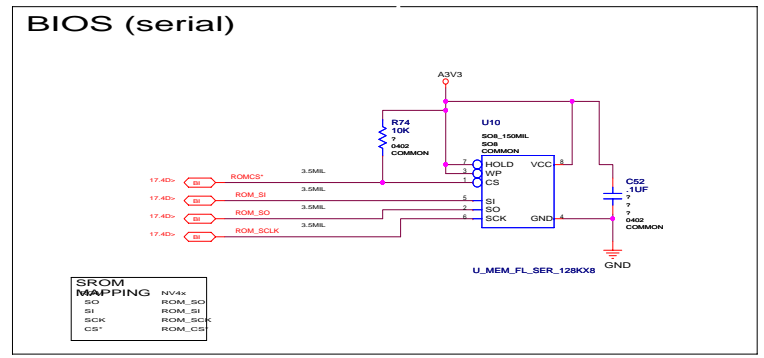
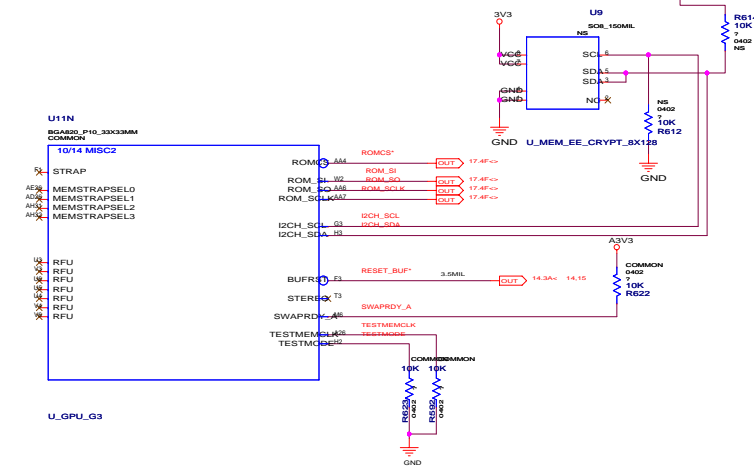


DEL EXT 4-PIN CONNECTOR

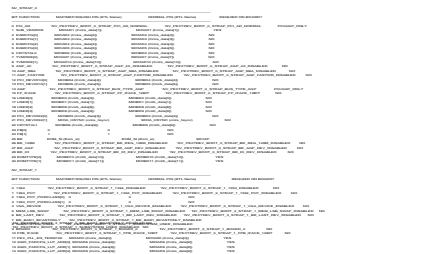




AUDIO and VIDEO signals are reserved for future GPU's. NV4x will not have support for these signals



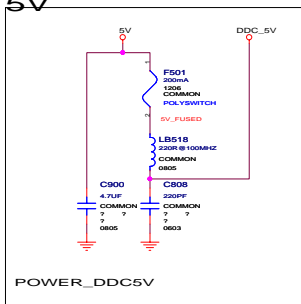
Assembly:
BIOS



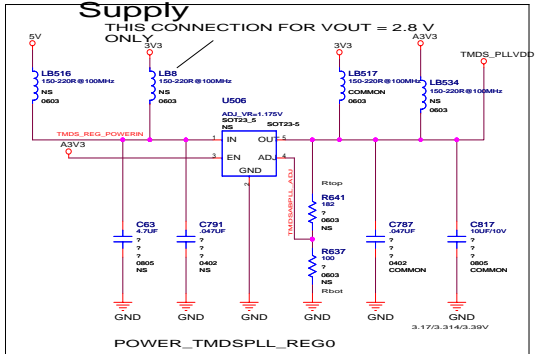
REG: NV_PEXTDEV_BOOT_0		VALUES
Bit Signal	VALUE_ID	
PCL_AD_SWAP	PCL_AD_SWAP	0 REVERSED
01: RAM_VENDOR	SUB_VENDOR	00000000 BIOS
02: RAM_CFG_0	RAM_CFG[3:0]	0000 1000
03: RAM_CFG_1	RAM_CFG[3:0]	0010 1001
04: RAM_CFG_2	RAM_CFG[3:0]	0010 1010
05: RAM_CFG_3	RAM_CFG[3:0]	0010 1011
06: CRYSTAL_0	CRYSTAL[1:0]	0010 2000 MHz 01 14.1818 MHz 10 27.000 MHz 11
07: TV_MODE_1	TV_MODE[1:0]	0000 1000
08: TV_MODE_0	TV_MODE[1:0]	0000 1001
09: AGP_Enable	AGP_30_8h	0 DISABLED 1 ENABLED
10: AGP_SBA	AGP_SBA[0]	0 SBA disabled 1 SBA enabled
11: AGP_FASTWR	AGP_FASTWR[0]	0 disabled 1 enabled
12: PCL_DEVID_0	PCL_DEVID[3:0]	0000 to 1400 - 1111 0x014F 0000 (default De 140)
13: PCL_DEVID_1	PCL_DEVID_1	
20: PCL_DEVID_2	PCL_DEVID_2	
21: PCL_DEVID_3	PCL_DEVID_3	
14: BUS_TYPE	BUS_TYPE[0]	0 PCI 1 USB
15: FP_IFACE	FP_IFACE[0]	0 FPM 1 SDRAM
23: FB_0	FB[1:0]	00 FPM 01 SDRAM 10 VESA 11 VESA
24: FB_1	FB[1:0]	00 FPM 01 SDRAM 10 VESA 11 VESA
25: BR	BR[0]	0 PARALLEL 1 SERIAL
26: BR_128M	BR	0 BR bit is ignored 1 BR bit is disabled
27: BR_AGP	BR	
28: BR_IO	BR	
30: ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Serial AT25F Signal_SST45F
30: ROM_TYPE_1	ROM_TYPE_1	00 Parallel 01 Serial AT25F Signal_SST45F
31: USER_0	STRAP_USER[3:0]	0000 (default)
31: USER_1	STRAP_USER[3:0]	0000 (default)
31: USER_2	STRAP_USER[3:0]	0000 (default)
31: USER_3	STRAP_USER[3:0]	0000 (default)

REG:	NV_STRAP_1	
Bit Signal	VALUE_ID	VALUES
11:		0 (default -- internal term on)
PIX_PLLEN_TERM100		
12:		
3GIO_PADCFG_LUT_ADR[0]		
13:		
3GIO_PADCFG_LUT_ADR[1]		
14:		
3GIO_PADCFG_LUT_ADR[2]		

Power Supply ...



TMDS AB/CD PLL



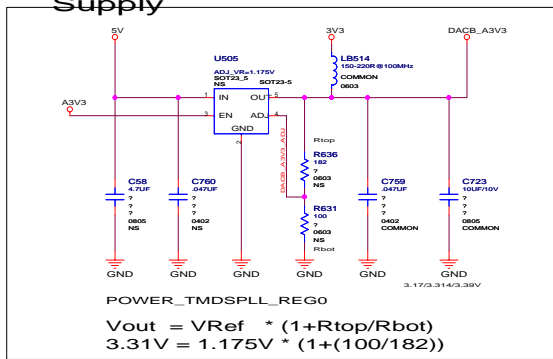
$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

$$3.31V = 1.175V * (1 + (100/182))$$

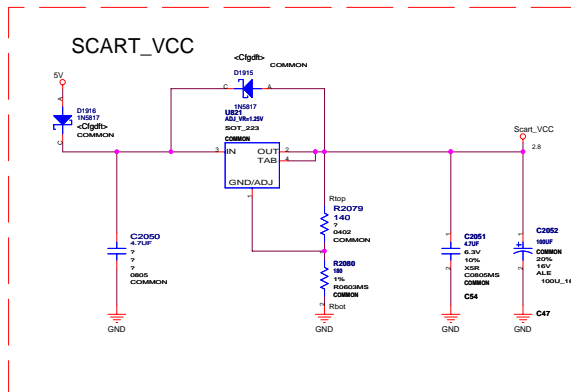
MIOA_VDDQ

Delete MIOA_2V5 PWR

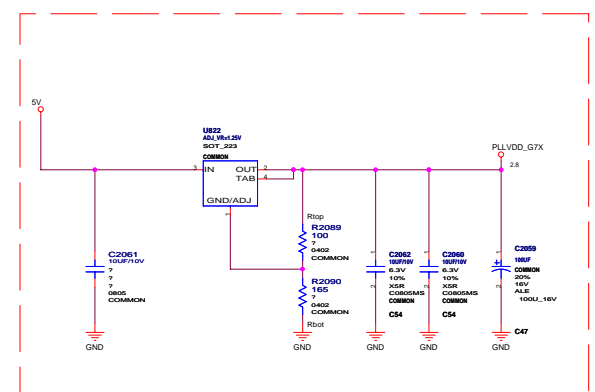
~~DACB
Supply~~



SCART_VCC



ADD 6/14



ADD 11/7 Rbot
 $V_{out} = V_{Ref} * (1 + R_{bot}/R_{top})$
 $3.31V = 1.25V * (1 + (165/100))$



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ISL6549 for Nvidia NV4x Graphic card power ckt

