

# P2002

2GB GDDR5, 256b, 64Mx32

Stacked DVI-I/DVI-D + HDMI + DP

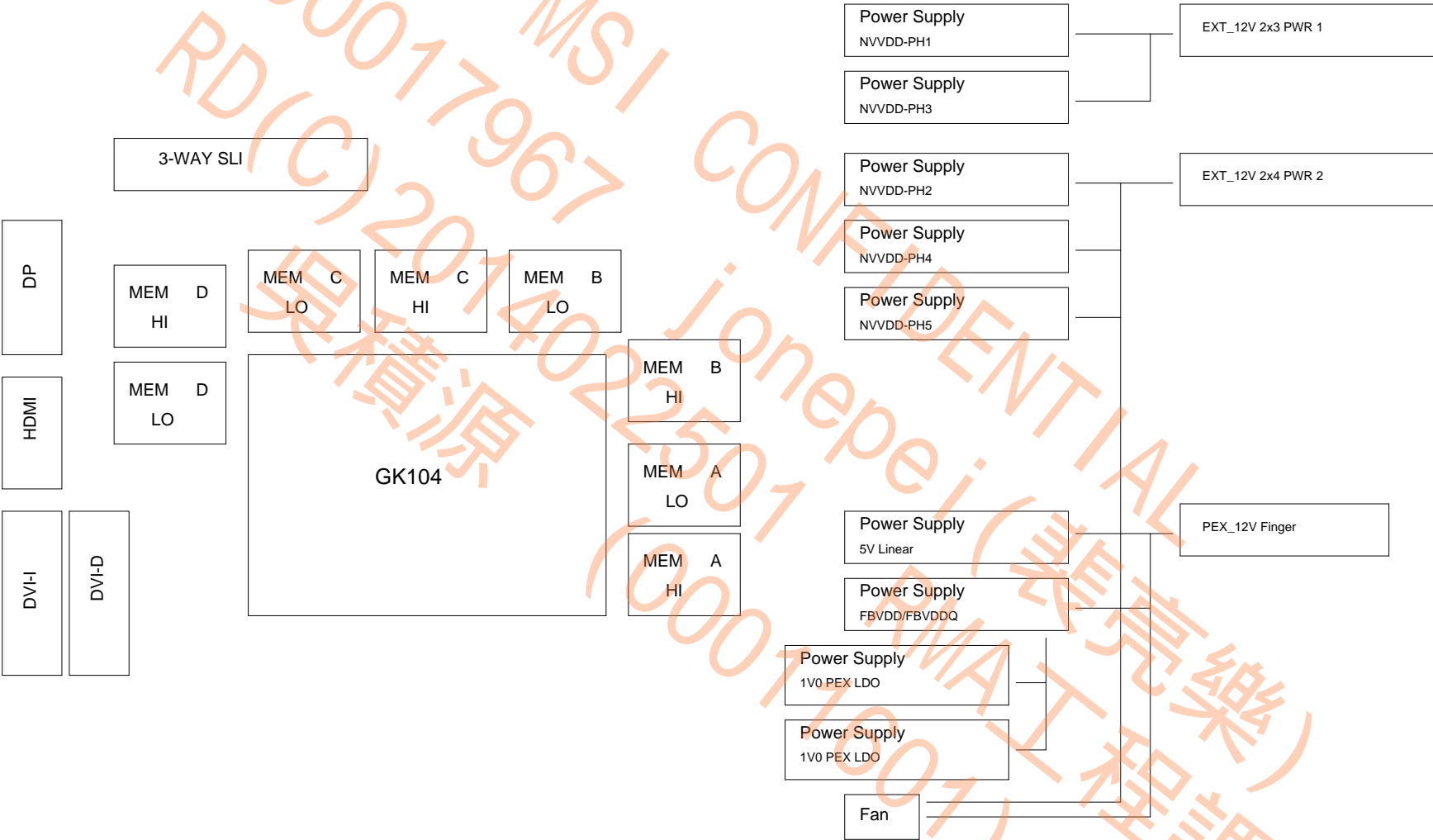
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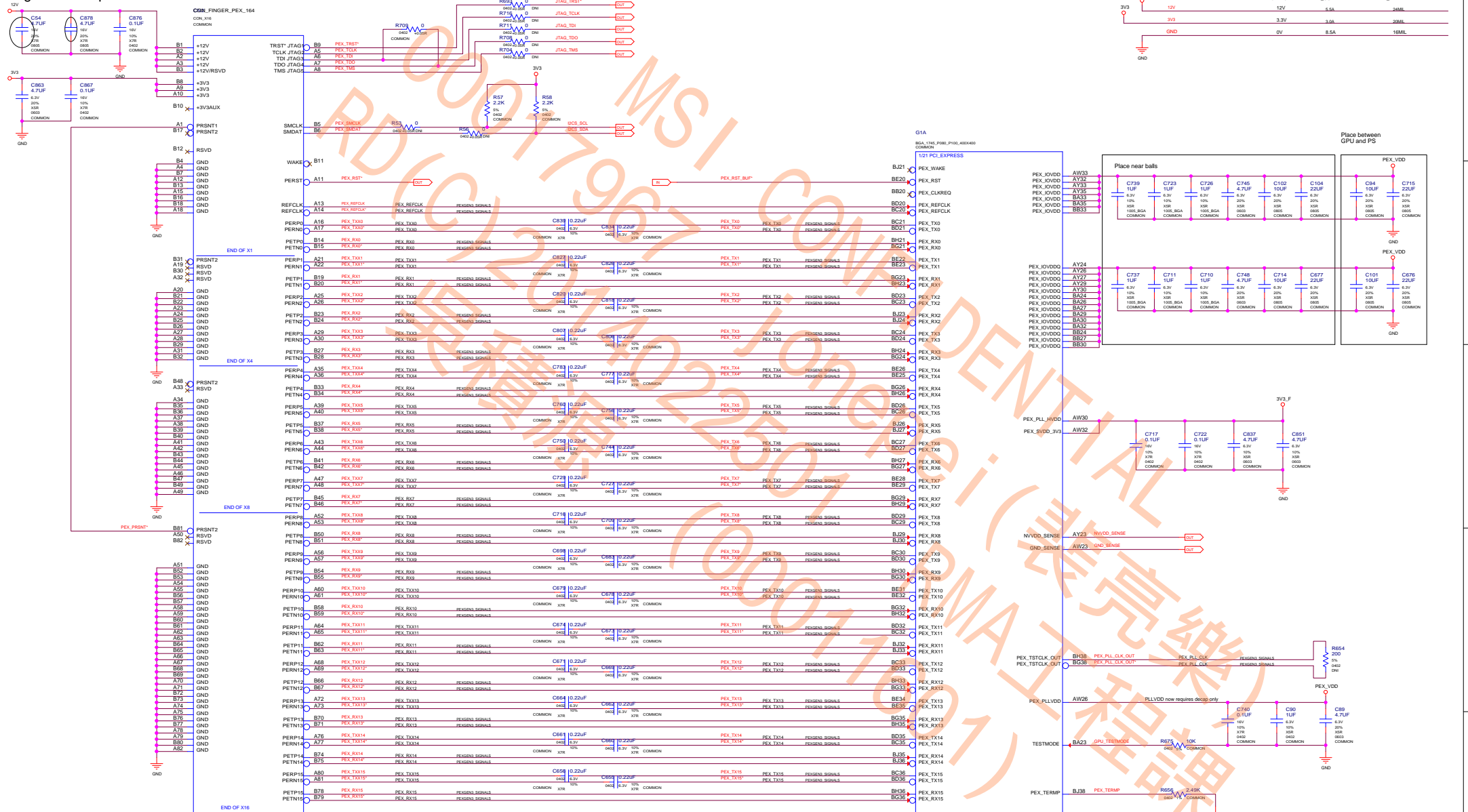
Base V282-I-0  
P117/P118 add dvi-i circuit  
P223 add I2C IB  
P225 CHANGE NVVDD POK & MEM OUTPUT CHOKER  
P226/P227 CHANGE NVVDD POWER CIRCUIT  
P30 CHANGE INPUT CHOKER / 6 pin 8 pin connect coil

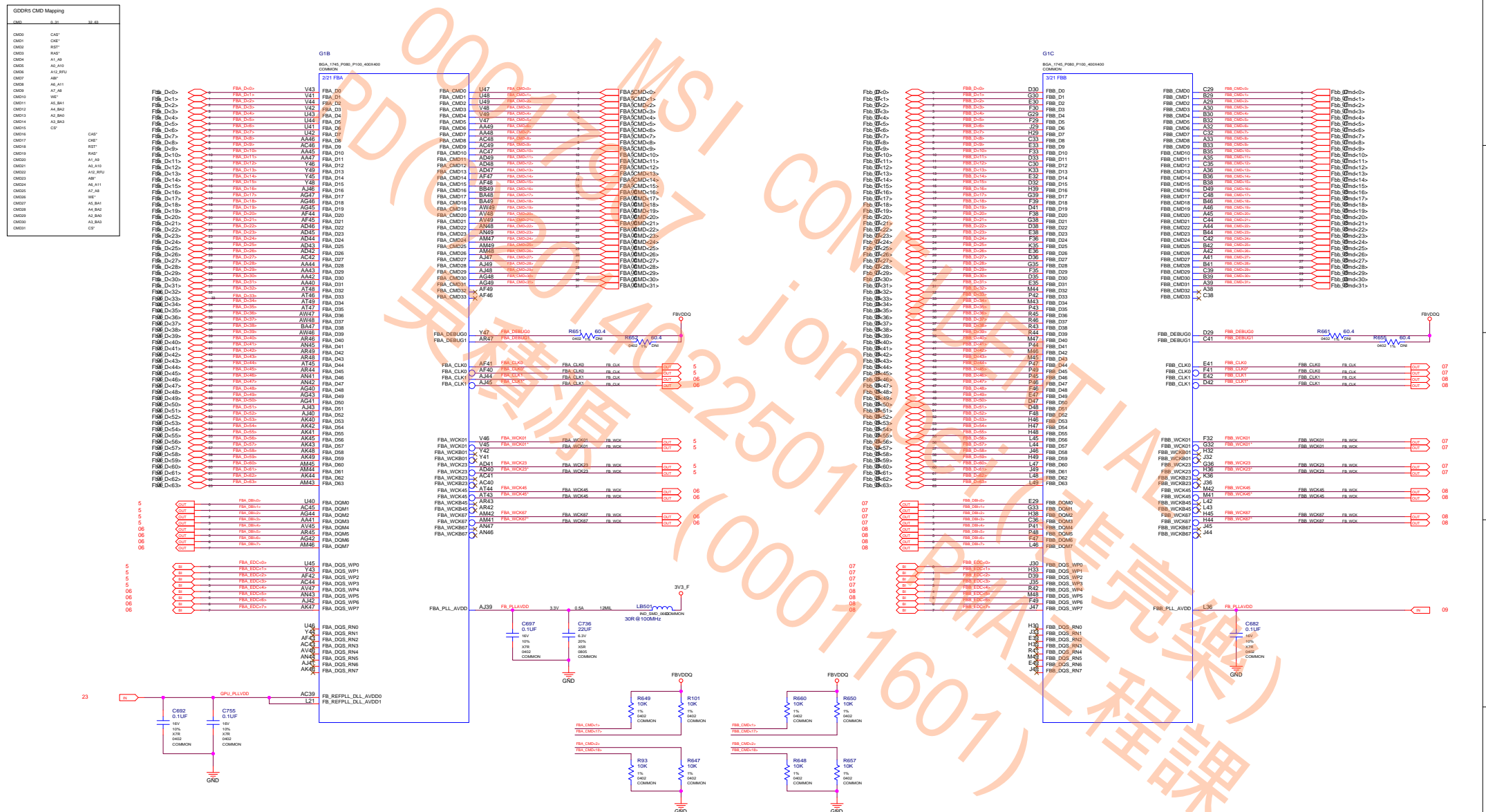
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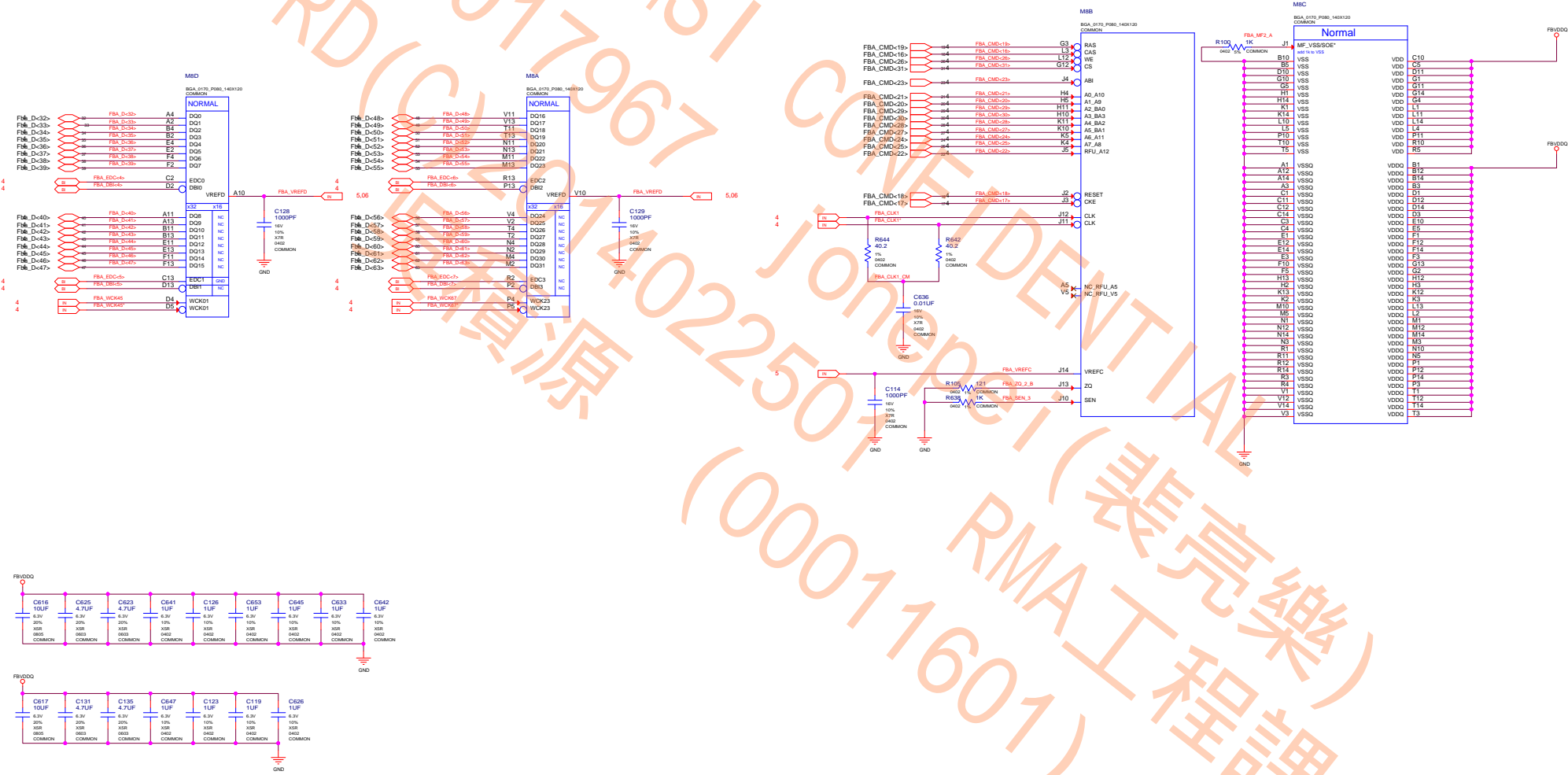
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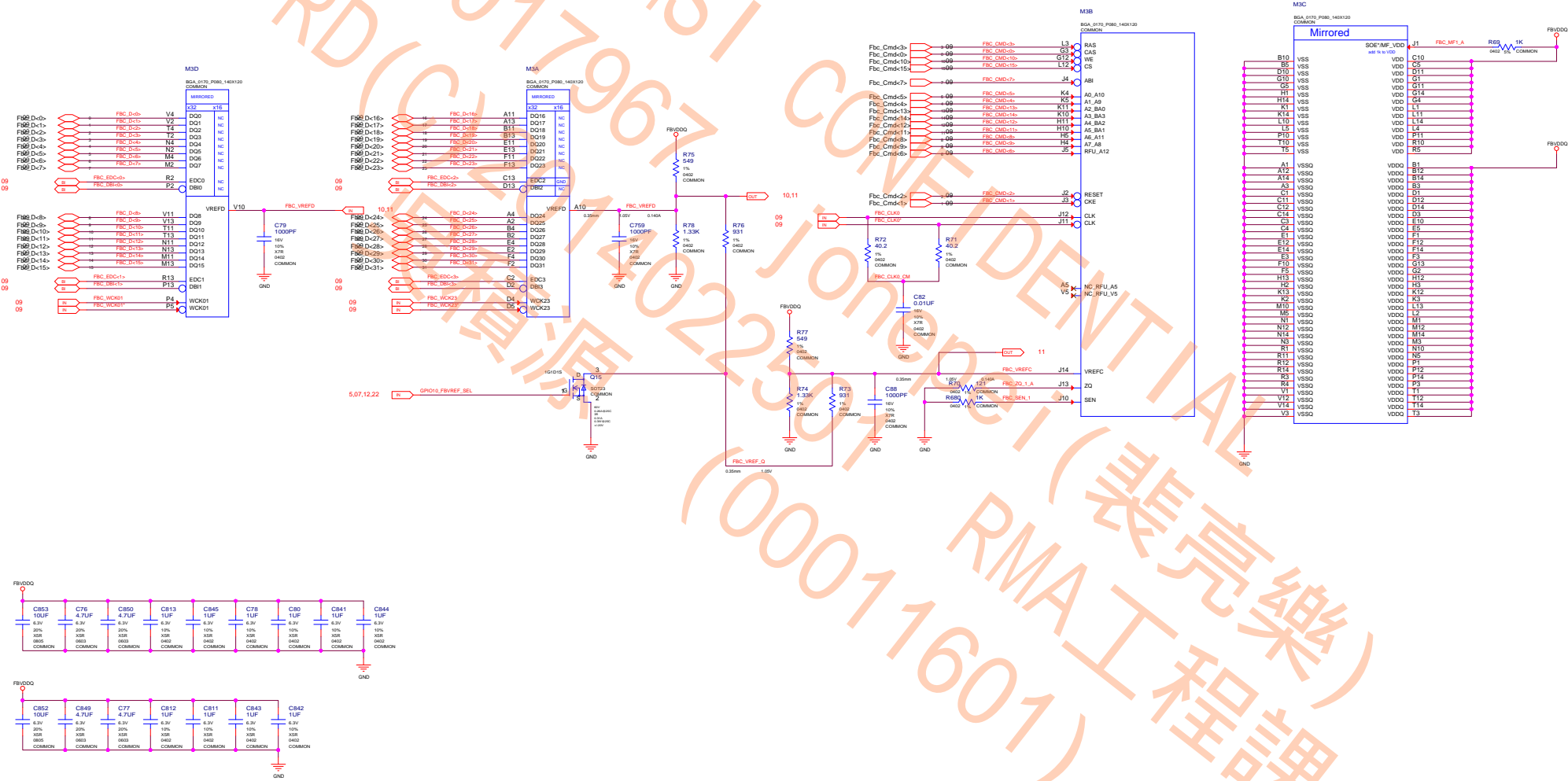


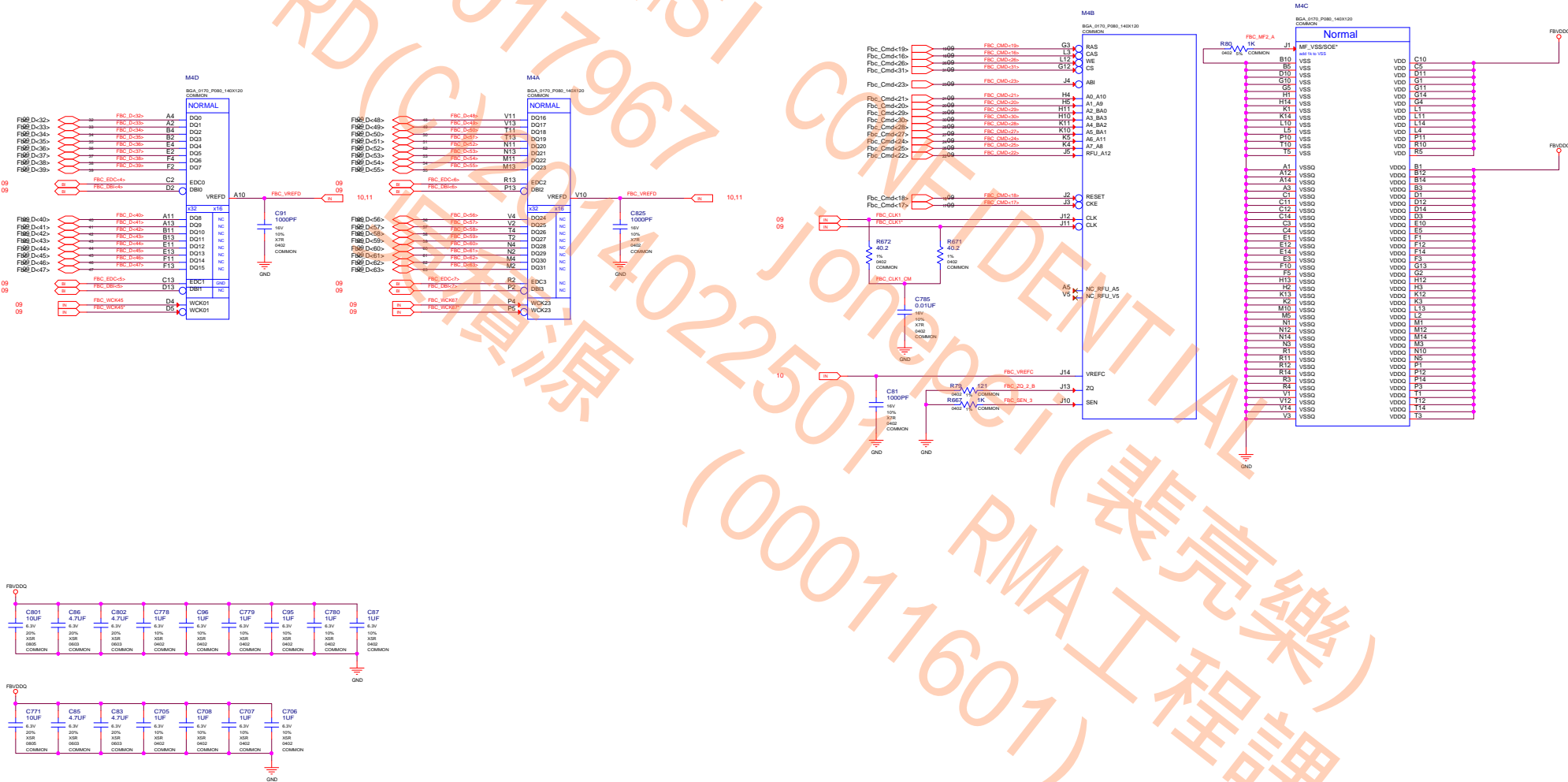








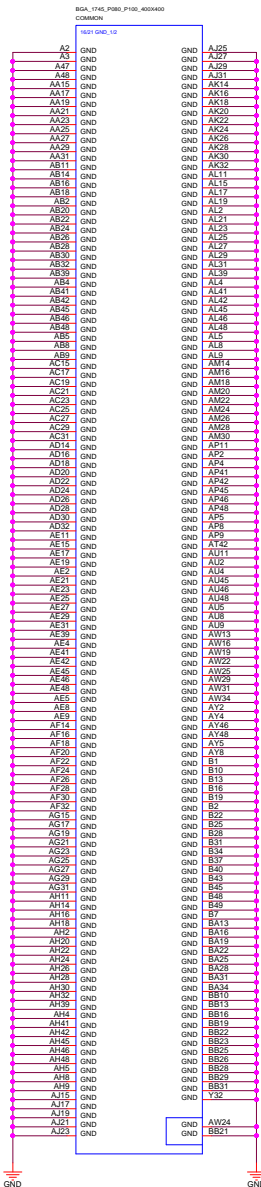




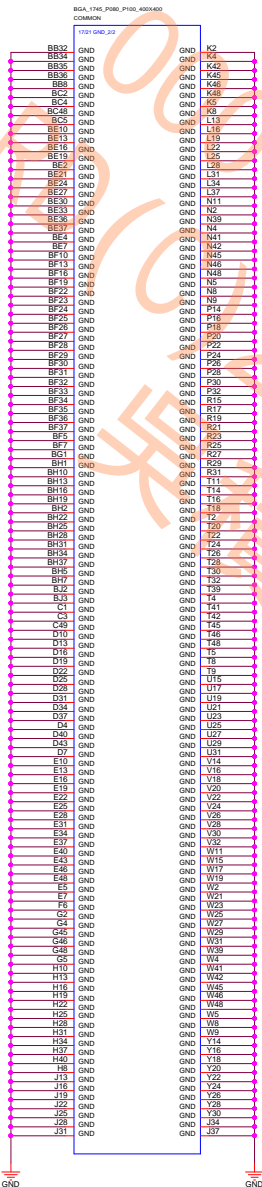




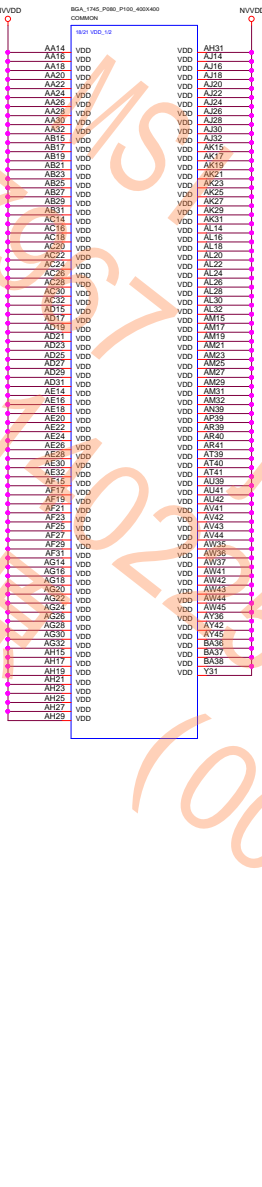
G1F



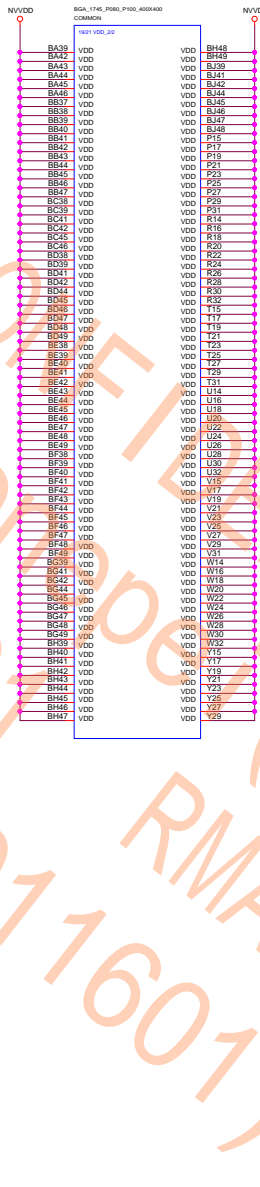
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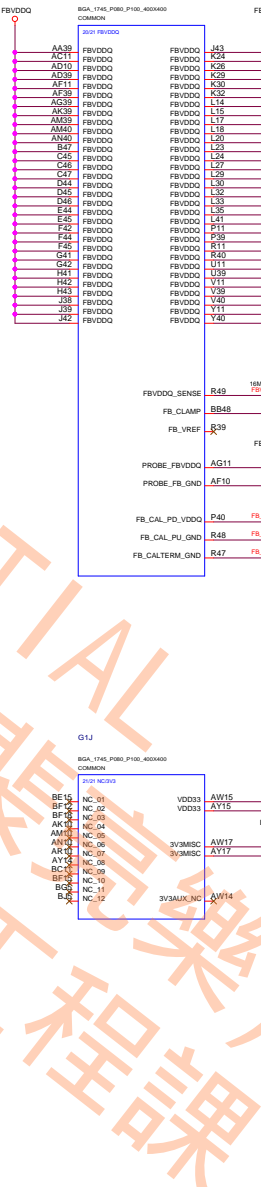
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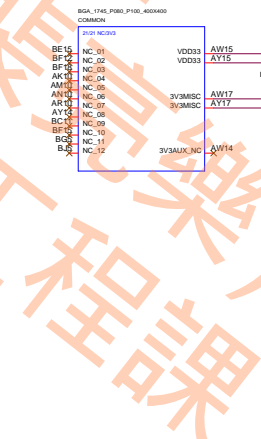
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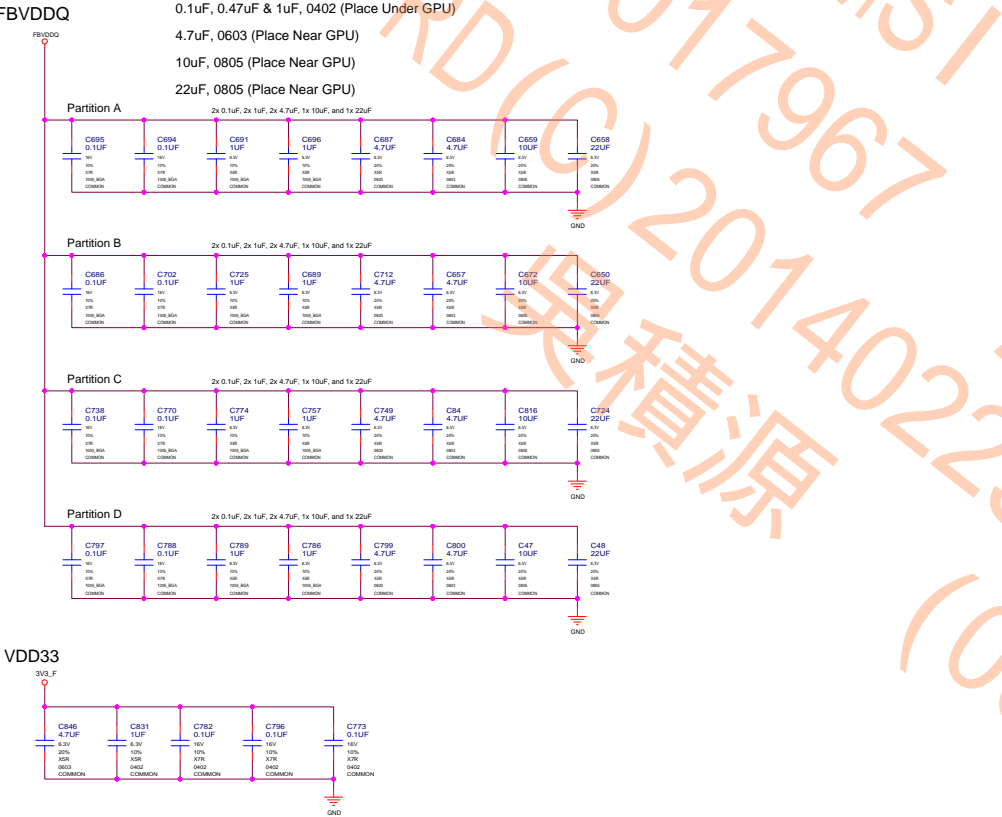
G1K



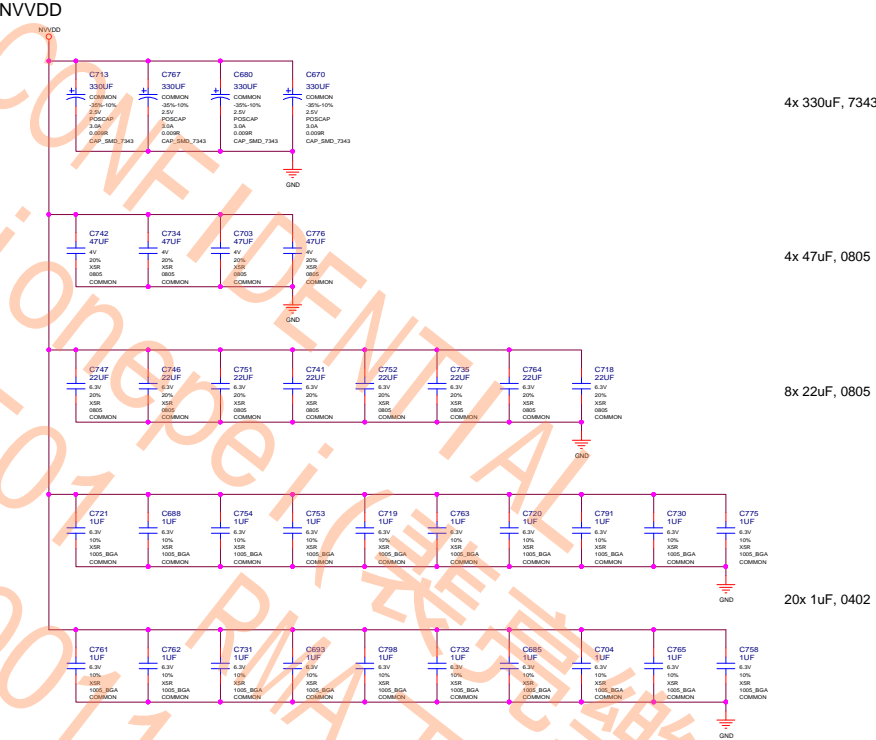
G1J



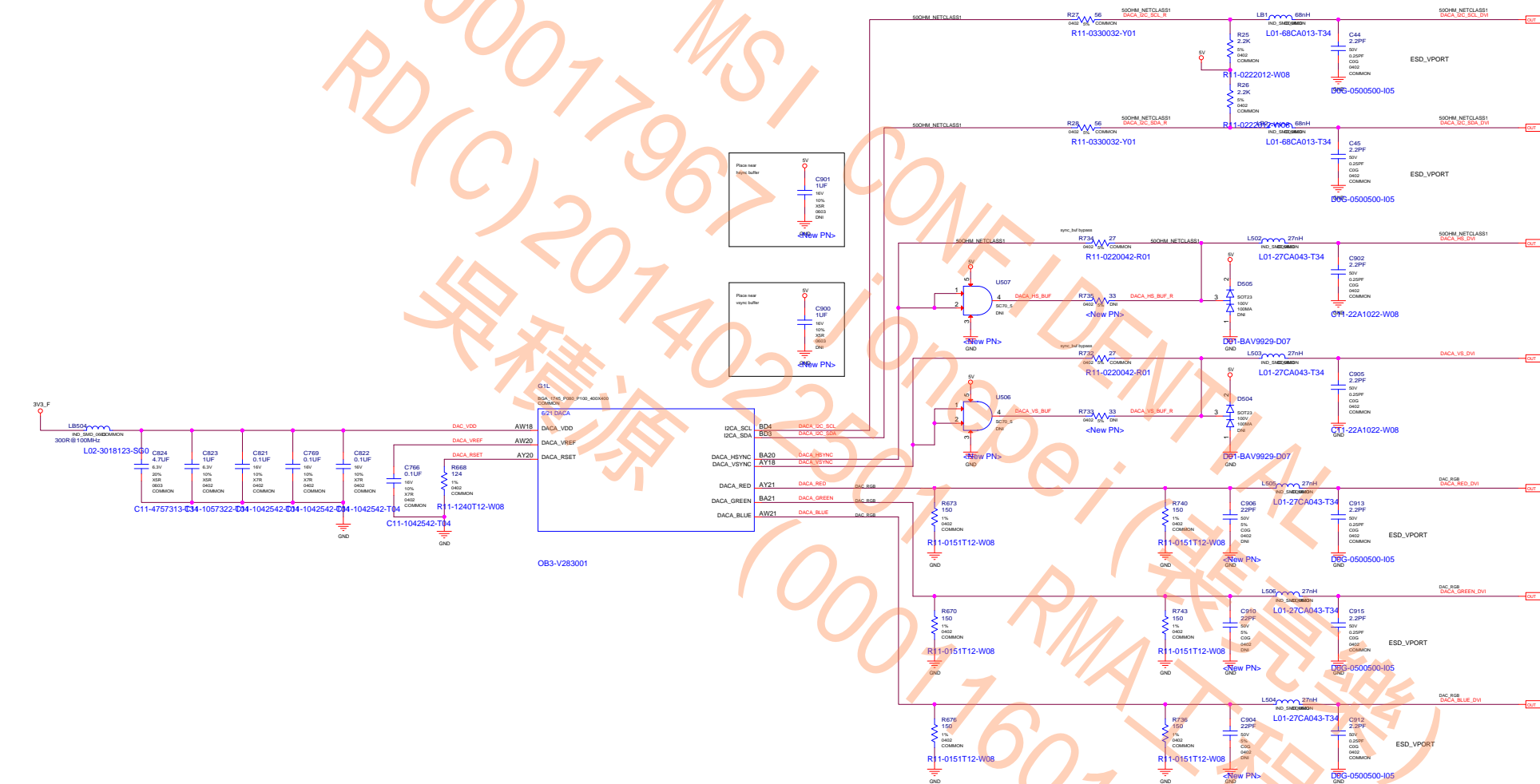
Based on GB2-X GDDR5 FBVDDQ Decap Guideline



NVVDD Decoupling caps. Place under GPU.





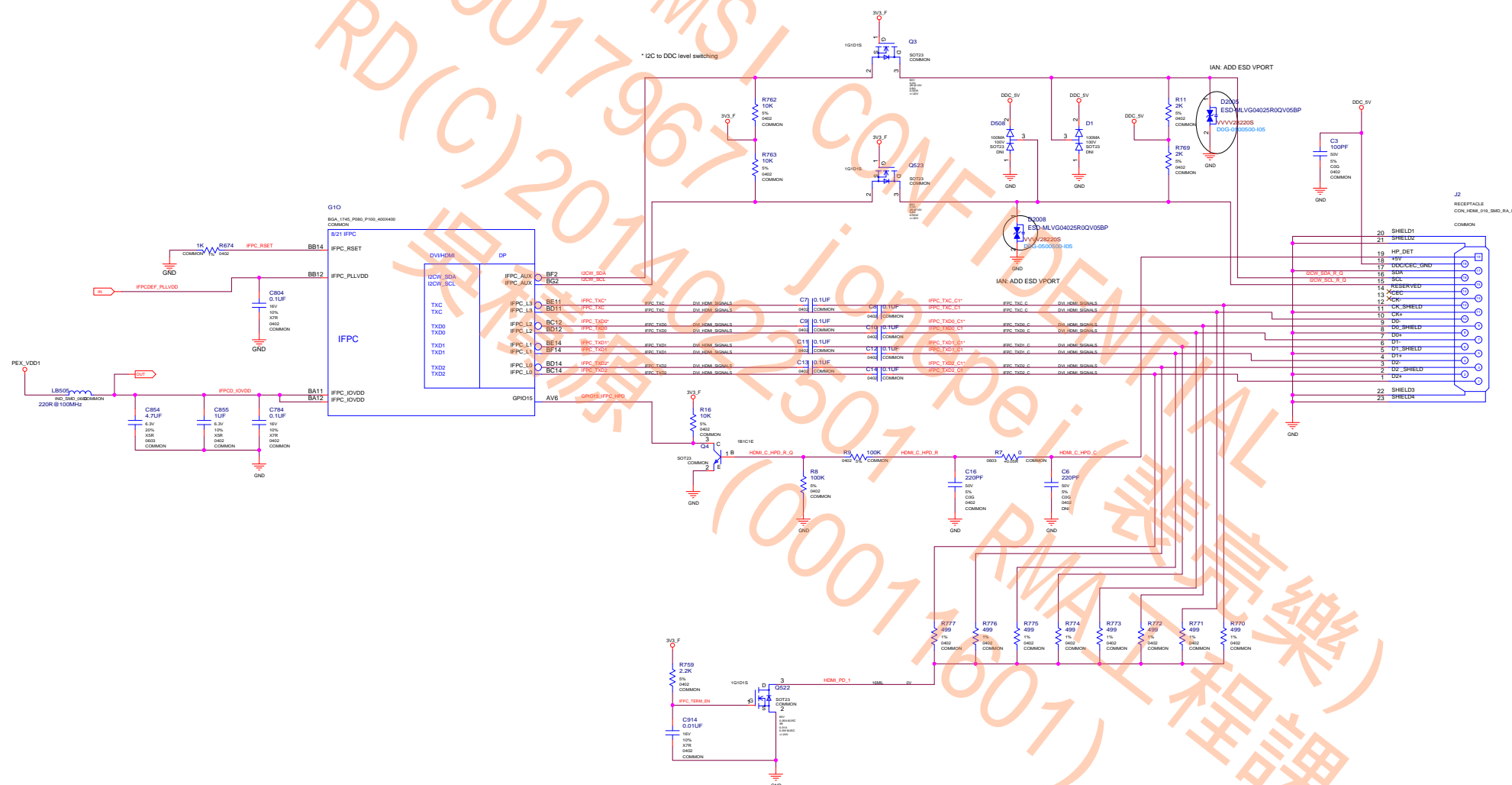


NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DAC_VDD	3.3V	0.25A	16MIL



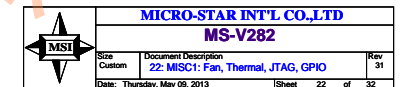












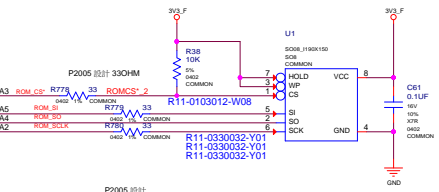
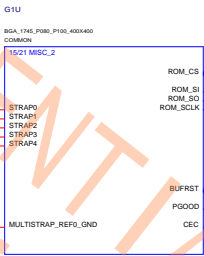
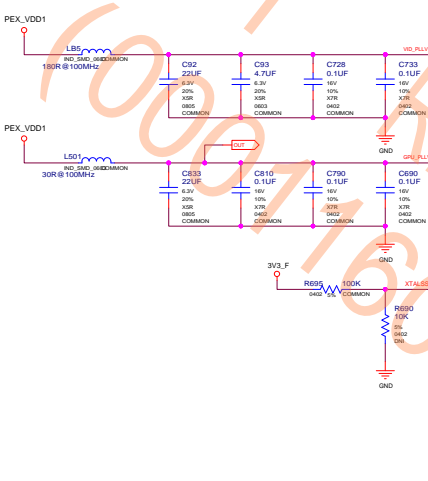
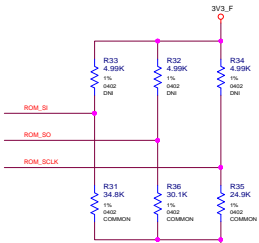
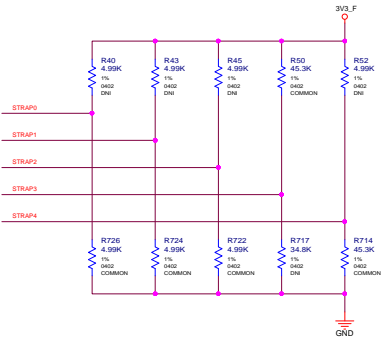


STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0000 - (0x1180)*	5K PD -400 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		
ROM_SI	RAMCFG[0]*	0*	
	RAMCFG[1]*	1*	35K PD*
	RAMCFG[2]*	1*	
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	10k PU*
	FB[0]_APERTURE_SIZE*	0*	For 256MB*
	FB[1]_APERTURE_SIZE*	1*	For 256MB*
ROM_SCLK	PEX_PLL_EN_TERM100*	0*	DISABLED*
	PCI_DEVID_EXT[5]*	0*	For 0x1180*
	SUB_VENDOR*	1*	Dedicated BIOS*
	PCI_DEVID_EXT[4]*	0*	For 0x1180*

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	32Mx32 256-bit Elpida		
0010	32Mx32 256-bit Hynix		
0011	32Mx32 256-bit Samsung		
0100	Reserved		
0101	64Mx32 192-bit Elpida		
0110	64Mx32 256-bit Hynix		
0111	64Mx32 256-bit Samsung		
1000	Reserved		
1001	32Mx32 192-bit Elpida		
1010	32Mx32 192-bit Hynix		
1011	32Mx32 192-bit Samsung		
1100	Reserved		
1101	64Mx32 192-bit Elpida		
1110	64Mx32 192-bit Hynix		
1111	64Mx32 192-bit Samsung		

	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2K 1% TO GND



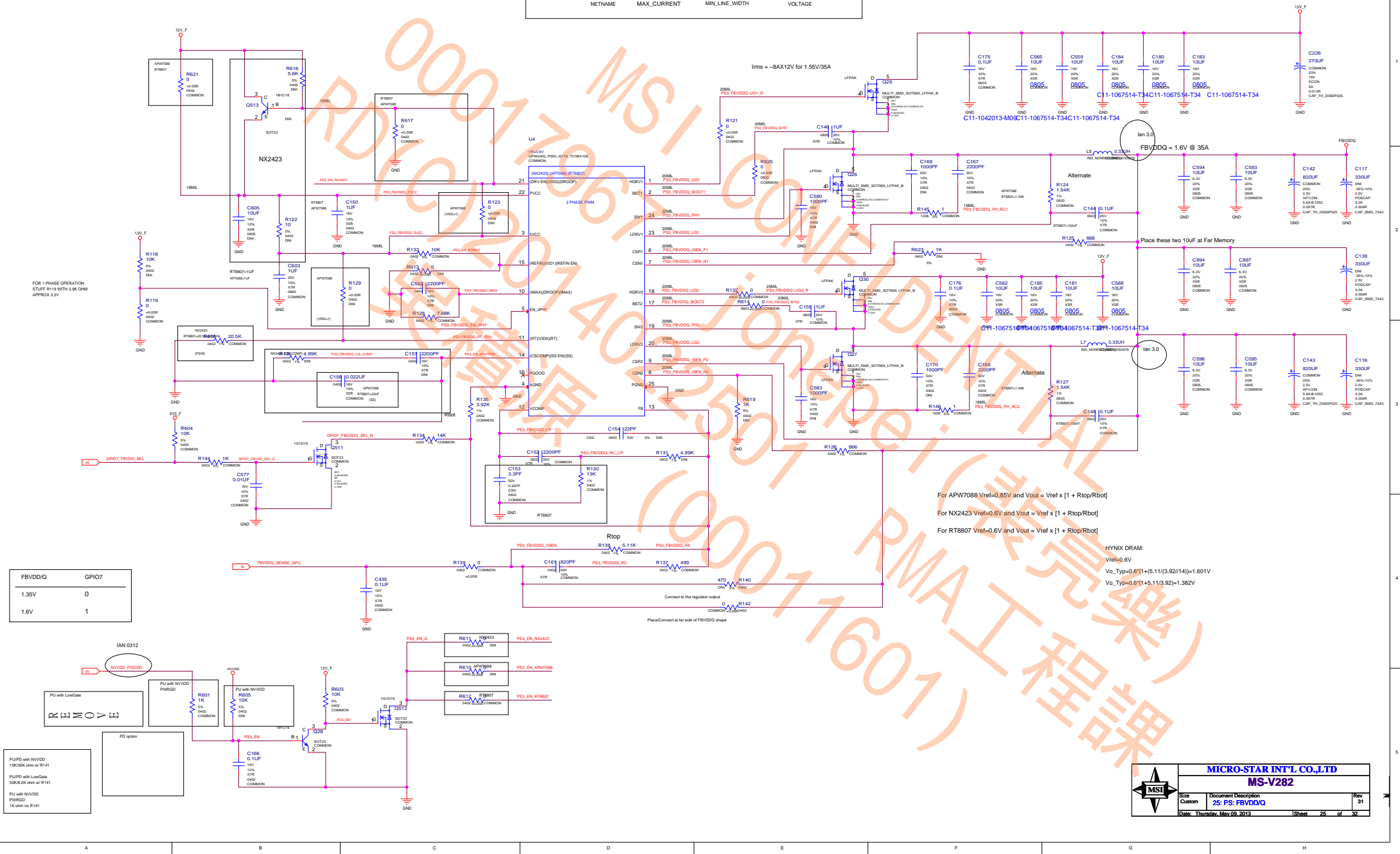
XTALIN	XTALOUT	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

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VID Table					
GPI07	GPI06	GPI05	GPI02	GPI017	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

\*VTC resistor is a placeholder

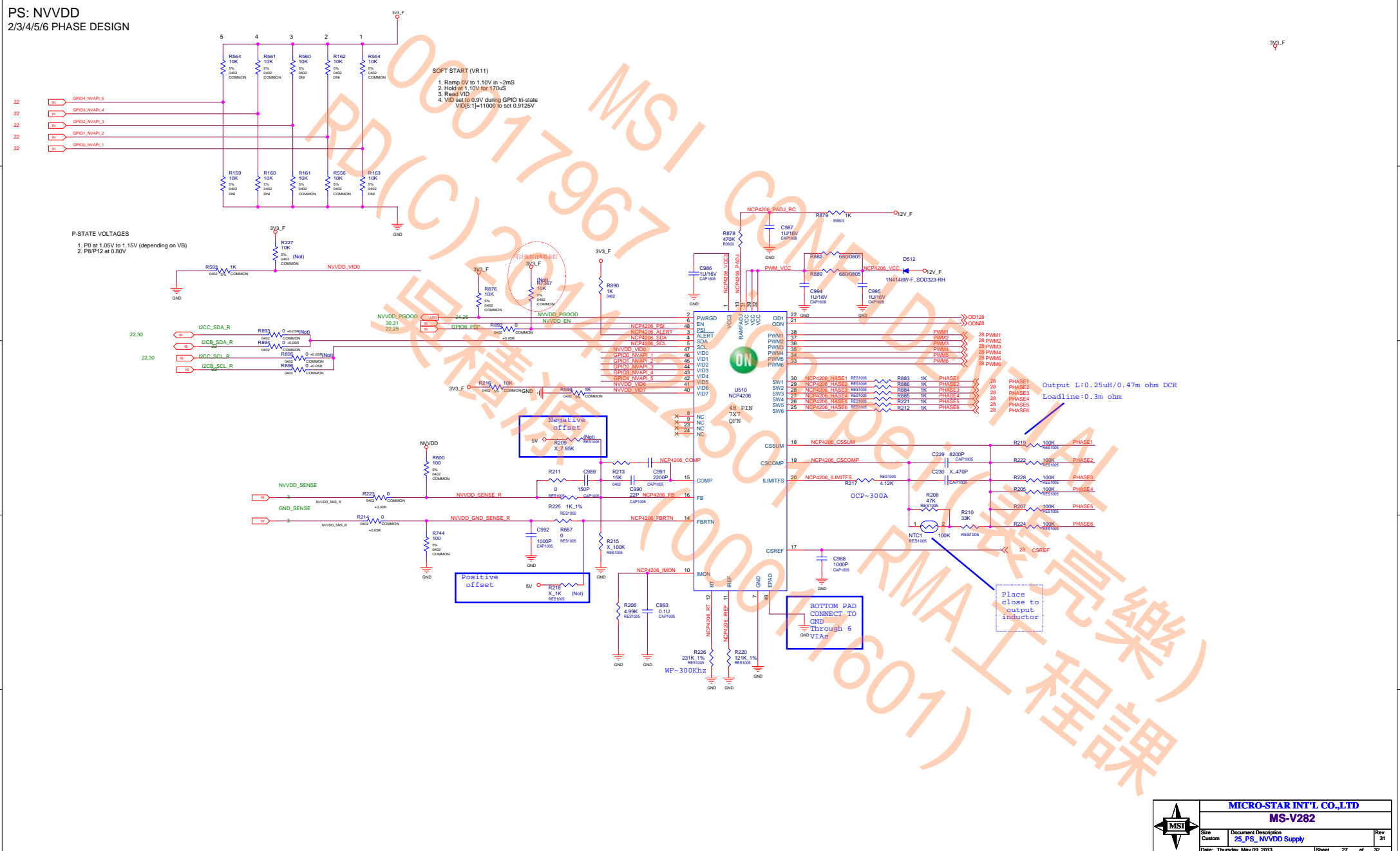
PSI intended for lower power states  
switching from 6 phases down to 1 or 2 phases  
PSI DRVON enabled for either 3 or 4 phases

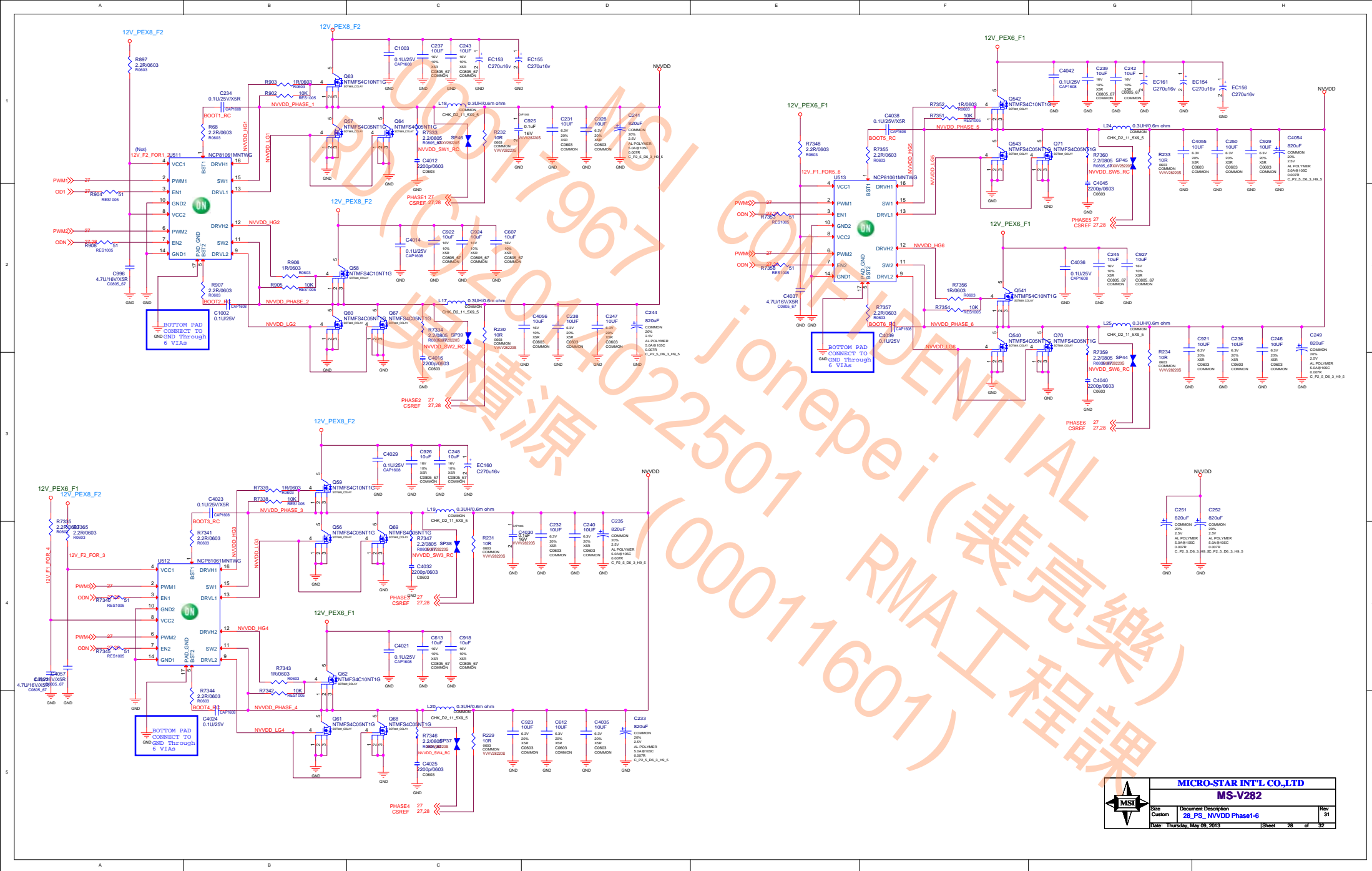
REMOVE V282-1.0 NVVDD PWM

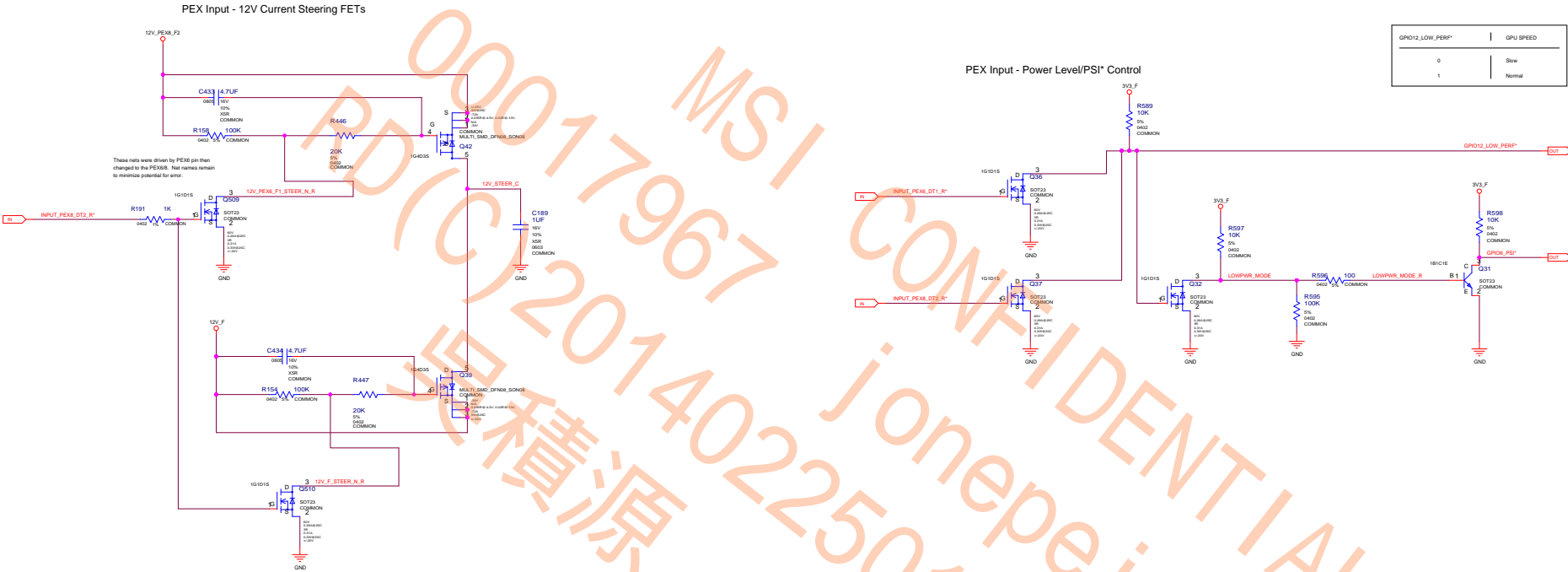


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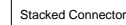
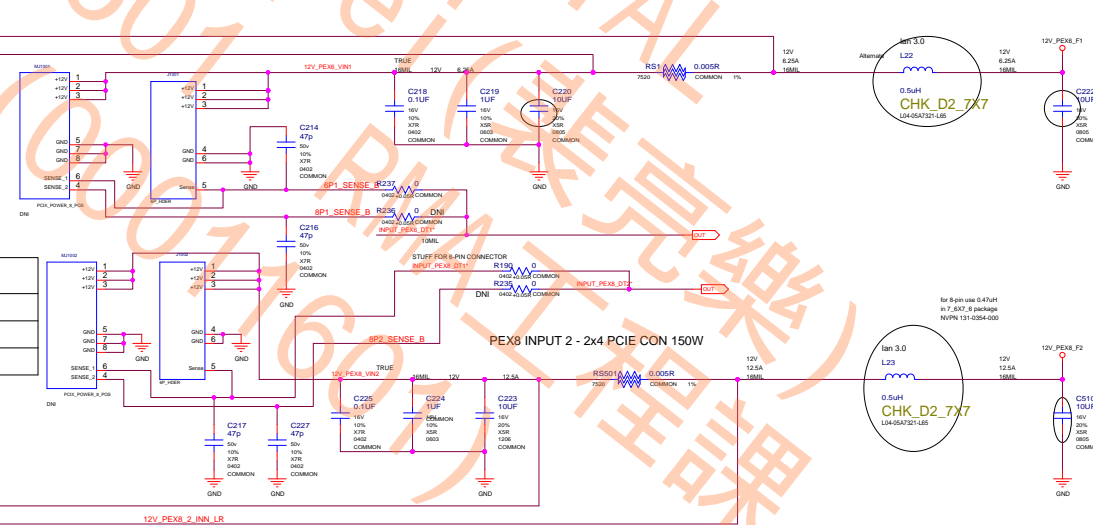
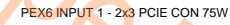
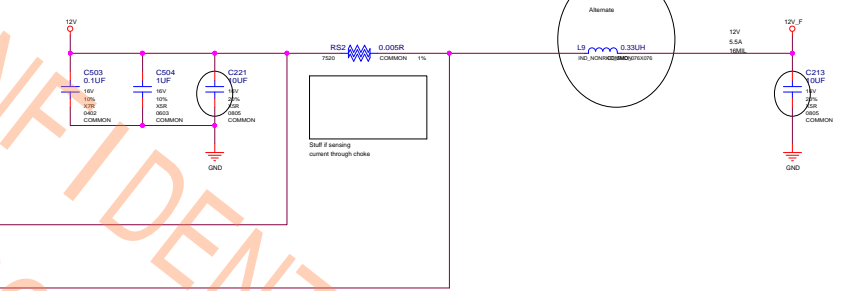
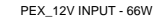
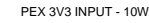
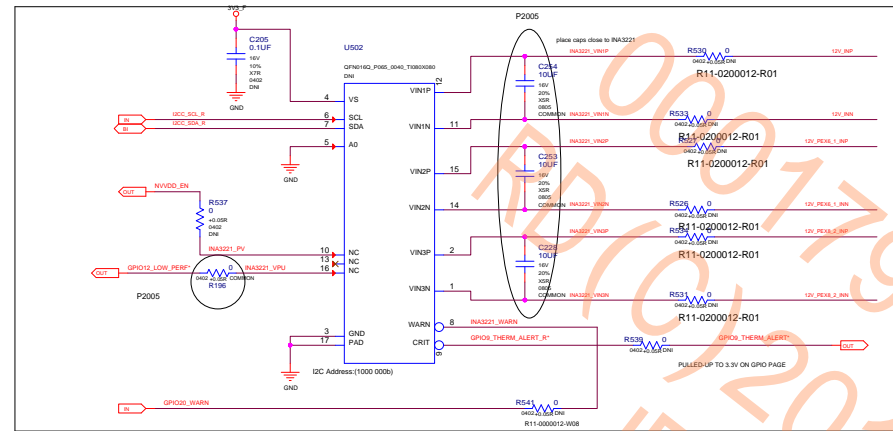
PS: NVVDD  
2/3/4/5/6 PHASE DESIGN





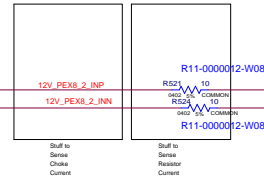






J6
6-pin PEX/8-pin PEX
6-pin PEX/6-pin PEX


See BOM to determin which connector is stuffed

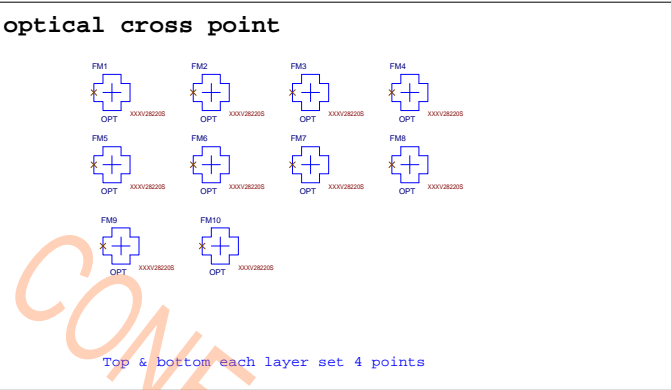


IFP\_IOVDD (backdrive prevention)

## CURRENT STEERING

## POWER CONNECTOR HOT-UNPLUG DETECT

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Brackets:



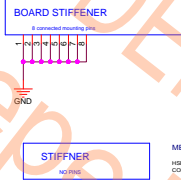
Bracket Screw



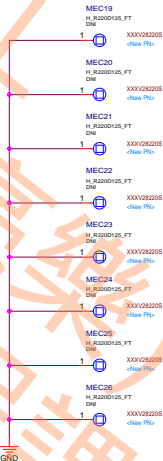
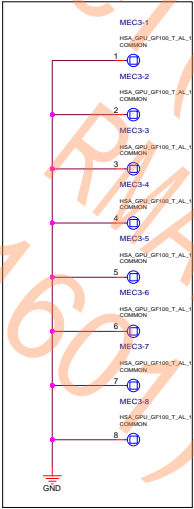
Hockey Stick



GPU Stiffner



Mechanical Holes Symbol



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