Title

RH RV620 256MB DDR2 VO+DMS59 6L LP

Schematic No. 105-B629xx-00B

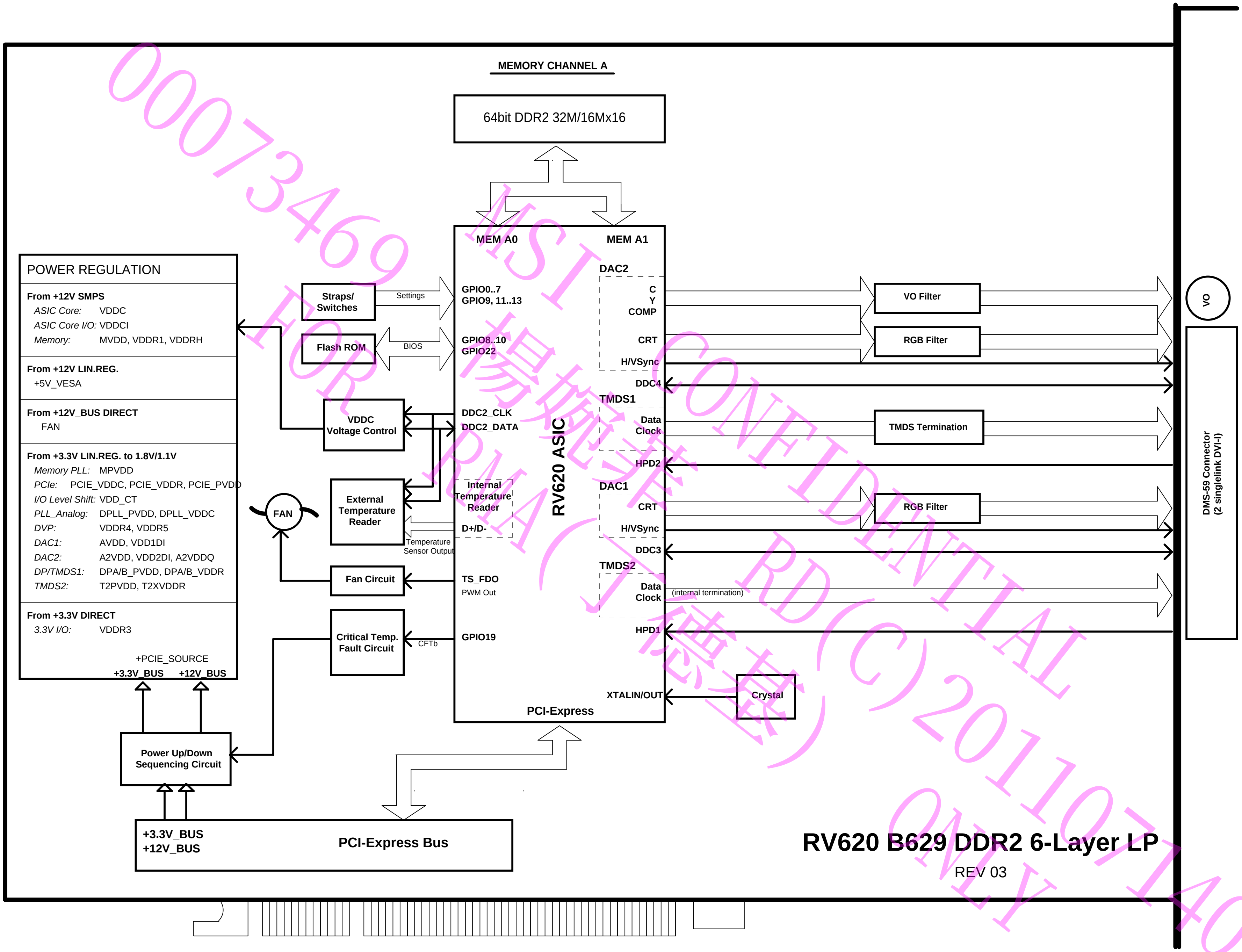
Date: Friday, April 25, 2008

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 03

Sch Rev	PCB Rev	Date	**TYPHOON** REVISION DESCRIPTION
01	00A	2008.02.04	START NEW TYPHOON SCHEMATIC. DERIVED FROM B530 REV06 (-00A) SCHEMATIC. CHANGED DISPLAY OUTPUT TO VO + DMS59.
02	00A	2008.02.04	REMOVED B100. CHANGED C2026 TO 0603 SIZE. REDUCED # OF STITCHING CAPS. CHANGED TO DDC3 & DDC4 FOR DISPLAY EDIDs, AND TO DDC2 FOR I2C DEBUG COMPONENTS.
03	00A	2008.02.05	REMOVED SUPPORT FOR 64Mx16 MEMORY CONFIGURATION FOR EASE OF LAYOUT.
04	00A	2008.02.12	ADDED CTF TEST CIRCUIT.
05	00A	2008.02.12	ADDED R1280 IN THE CTF TEST CIRCUIT.
06	00A	2008.02.14	REMOVED SHUNT RESISTORS R110 - R113 ON TMDP Tx LINES BECAUSE THEY ARE NOT REQUIRED.
07	00A	2008.02.20	ADD NOTE "DNI" FOR LVTM SHUNT RESISTORS (R100 - R102, R106)
08	00A	2008.02.21	CORRECT DDC4 DATA/CLOCK OFF-PAGE CONNECTORS (p.4)
09	00B	2008.03.17	CORRECT MVDDC_FB NET (p.9); UPDATE BLOCK DIAGRAM (p.20)
010	00B	2008.03.19	REMOVE FOOTPRINT FOR OSCILLATOR CIRCUIT (Y81, B80, C80, C81, R81, R82, R83, MR83) TO IMPROVE LAYOUT OF THE CRYSTAL (p.3); UPDATE BLOCK DIAGRAM (p.20)
011	00B	2008.03.24	ADD FOOTPRINT FOR AN ADDITIONAL CAPACITOR C64 (0402 SIZE) ON THE +DPLL_VDDC RAIL (p.3)

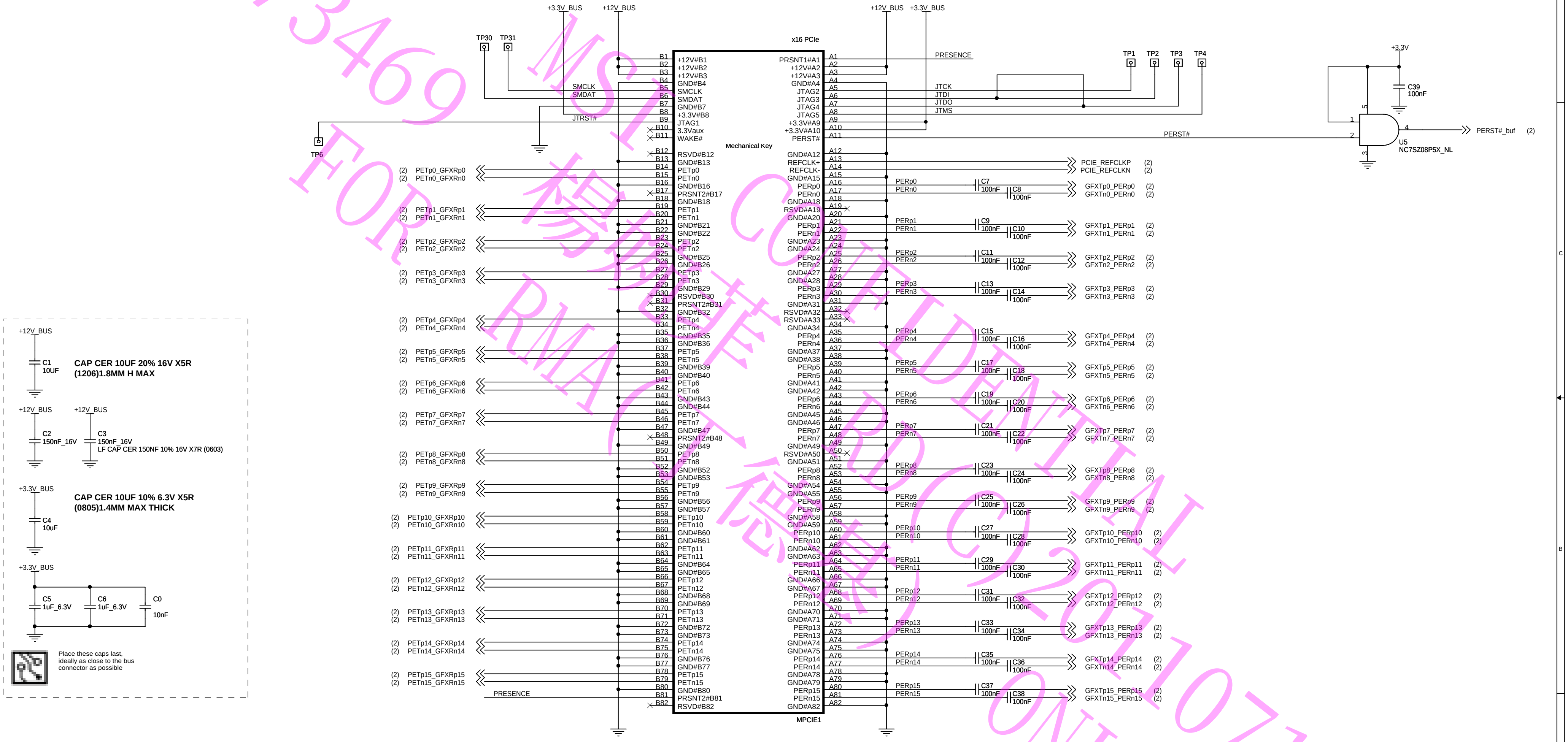


MEMORY CHANNEL A
64bit DDR2 32M/16Mx16
MEM A0
MEM A1
POWER REGULATION
From +12V SMPS
ASIC Core: VDDC
ASIC Core I/O: VDDCI
Memory: MVDD, VDDR1, VDDRH
From +12V LIN.REG.
+5V_VESA
From +12V_BUS DIRECT
FAN
From +3.3V LIN.REG. to 1.8V/1.1V
Memory PLL: MPVDD
PCIe: PCIE_VDDC, PCIE_VDDR, PCIE_PVDD
I/O Level Shift: VDD_CT
PLL_Analog: DPLL_PVDD, DPLL_VDDC
DVP: VDDR4, VDDR5
DAC1: AVDD, VDD1DI
DAC2: A2VDD, VDD2DI, A2VDDQ
DP/TMDS1: DPA/B_PVDD, DPA/B_VDDR
TMDS2: T2PVDD, T2XVDDR
From +3.3V DIRECT
3.3V I/O: VDDR3
+PCIE_SOURCE
+3.3V_BUS
+12V_BUS
Straps/ Switches
Settings
Flash ROM
BIOS
VDDC Voltage Control
External Temperature Reader
Temperature Sensor Output
FAN
Fan Circuit
Critical Temp. Fault Circuit
CFTb
GPIO0..7
GPIO9, 11..13
GPIO8..10
GPIO22
DDC2_CLK
DDC2_DATA
Internal Temperature Reader
D+/D-
TS_FDO
PWM Out
GPIO19
RV620 ASIC
PCI-Express
DAC2
C
Y
COMP
CRT
H/VSync
DDC4
TMDS1
Data
Clock
HPD2
DAC1
CRT
H/VSync
DDC3
TMDS2
Data
Clock
(internal termination)
HPD1
XTALIN/OUT
Crystal
VO Filter
RGB Filter
TMDS Termination
RGB Filter
VO
DMS-59 Connector
(2 singlelink DVI-I)
Power Up/Down Sequencing Circuit
+3.3V_BUS
+12V_BUS
PCI-Express Bus
RV620 B629 DDR2 6-Layer LP
REV 03

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, April 25, 2008	Rev 03
Sheet 20 of 20	
Title RH RV620 - BLOCK DIAGRAM	Doc No. 105-B629xx-00B

PCI-EXPRESS EDGE CONNECTOR



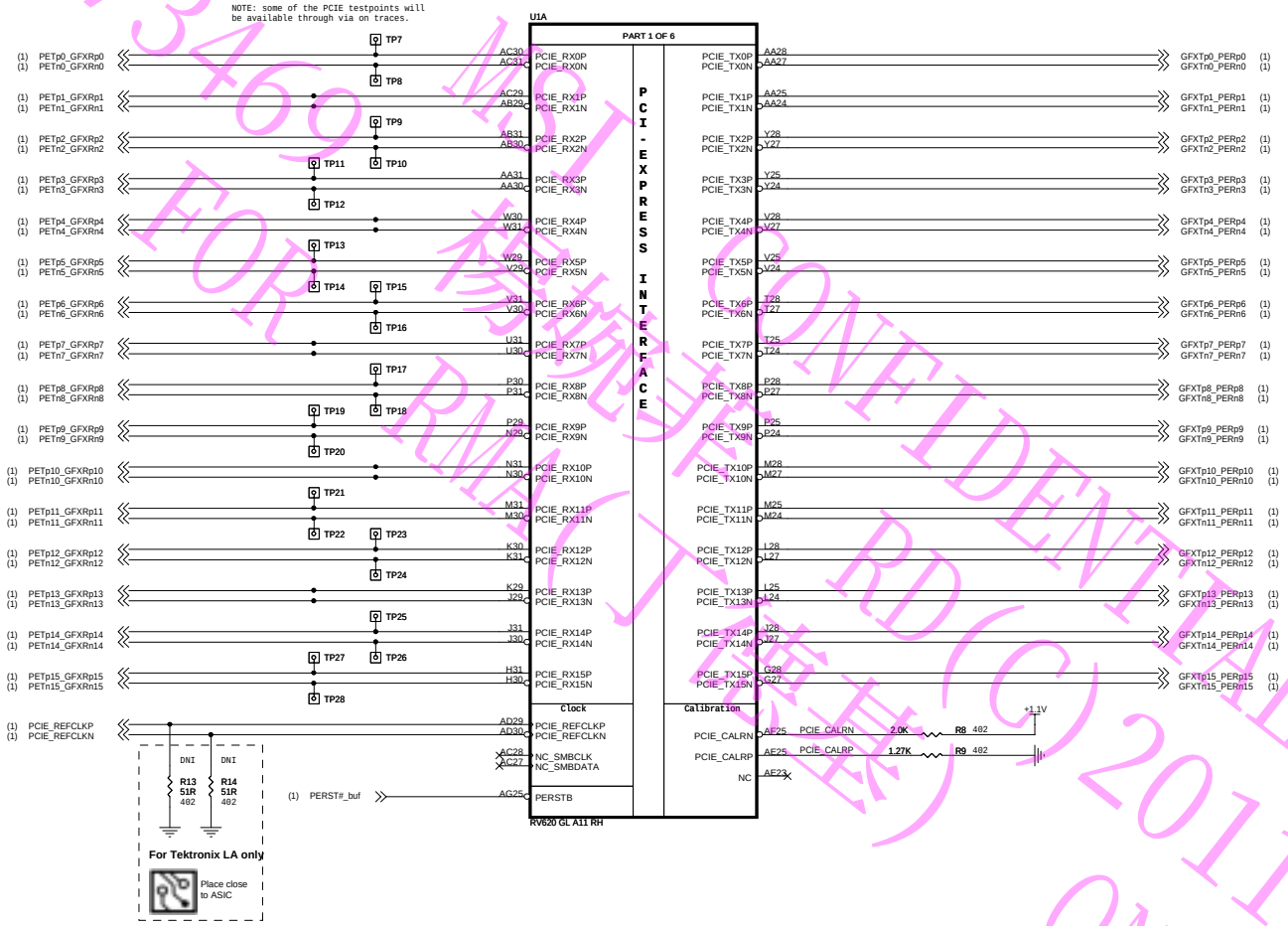
+3.3V_BUS
+12V_BUS
TP30
TP31
TP6
SMCLK
SMDAT
JTRST#
x16 PCIe
Mechanical Key
MPCIE1
PRESENCE
JTCK
JTDI
JTDO
JTMS
TP1
TP2
TP3
TP4
PERST#
+3.3V
C39
100nF
U5
NC7SZ08P5X_NL
PERST#_buf
PCIE_REFCLKP
PCIE_REFCLKN
+12V#B1
+12V#B2
+12V#B3
GND#B4
SMCLK
SMDAT
GND#B7
+3.3V#B8
JTAG1
3.3Vaux
WAKE#
RSVD#B12
PRSNT1#A1
+12V#A2
+12V#A3
GND#A4
JTAG2
JTAG3
JTAG4
JTAG5
+3.3V#A9
+3.3V#A10
PERST#
REFCLK+
REFCLK-
PETp0_GFXRp0
PETn0_GFXRn0
GFXTp0_PERp0
GFXTn0_PERn0
PETp15_GFXRp15
PETn15_GFXRn15
GFXTp15_PERp15
GFXTn15_PERn15
100nF
+12V_BUS
C1
10UF
CAP CER 10UF 20% 16V X5R
(1206)1.8MM H MAX
C2
150nF_16V
C3
150nF_16V
LF CAP CER 150NF 10% 16V X7R (0603)
+3.3V_BUS
C4
10uF
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK
C5
1uF_6.3V
C6
1uF_6.3V
C0
10nF
Place these caps last,
ideally as close to the bus
connector as possible

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, April 25, 2008	Rev 03
Sheet 1 of 20	
Title RH RV620 - PCI-E Edge Connector	Doc No. 105-B629xx-00B



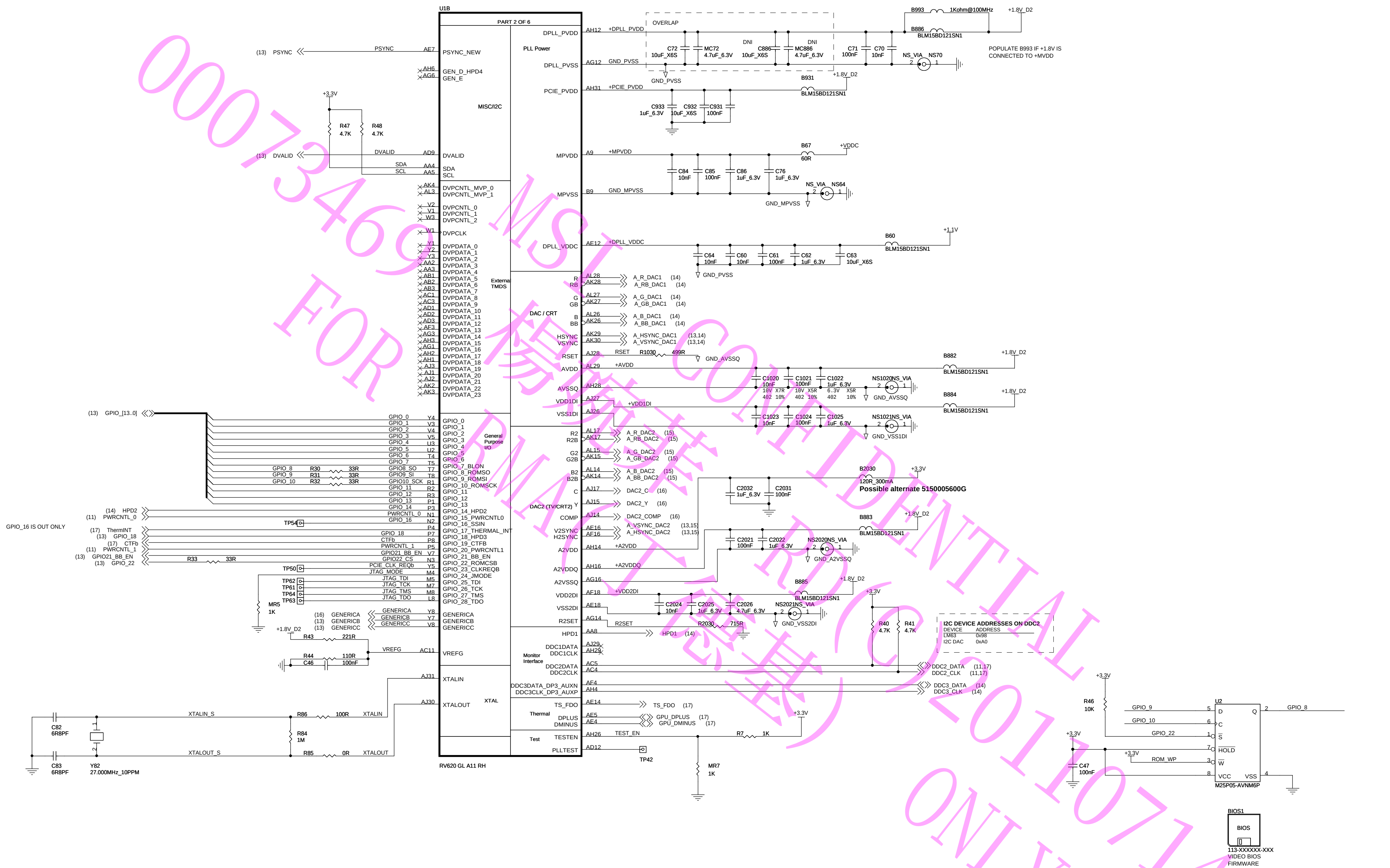
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, April 25, 2008 Rev 03

Sheet 2 of 20

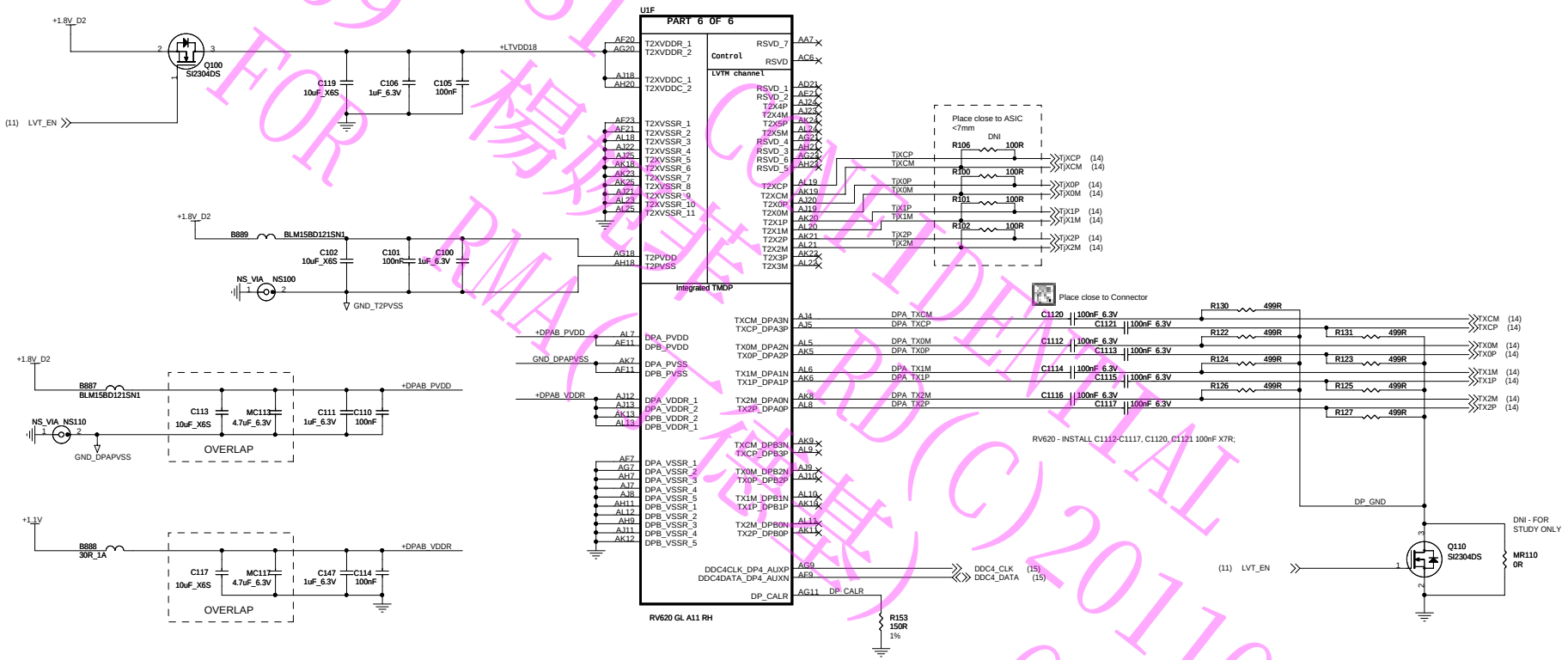
Title RH RV610 - ASIC PCIE Interface

Doc No. 105-B629xx-00B


U1B
PART 2 OF 6
PLL Power
MISC/I2C
External TMDS
DAC / CRT
General Purpose I/O
DAC2 (TV/CRT2)
Monitor Interface
XTAL
Thermal
Test
RV620 GL A11 RH
PSYNC_NEW
GEN_D_HPD4
GEN_E
DVALID
SDA
SCL
DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DPLL_PVDD
DPLL_PVSS
PCIE_PVDD
MPVDD
MPVSS
DPLL_VDDC
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1DI
VSS1DI
COMP
V2SYNC
H2SYNC
A2VDD
A2VDDQ
A2VSSQ
VDD2DI
VSS2DI
R2SET
HPD1
DDC1DATA
DDC1CLK
DDC2DATA
DDC2CLK
DDC3DATA_DP3_AUXN
DDC3CLK_DP3_AUXP
TS_FDO
DPLUS
DMINUS
TESTEN
PLLTEST
VREFG
XTALIN
XTALOUT
GENERICA
GENERICB
GENERICC
OVERLAP
DNI
POPULATE B993 IF +1.8V IS CONNECTED TO +MVDD
Possible alternate 5150005600G
I2C DEVICE ADDRESSES ON DDC2
DEVICE ADDRESS
LM63 0x98
I2C DAC 0xA0
GPIO_16 IS OUT ONLY
Y82
27.000MHz_10PPM
U2
M25P05-AVMN6P
BIOS1
BIOS
113-XXXXXX-XXX
VIDEO BIOS
FIRMWARE

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Friday, April 25, 2008
Rev	03
Sheet	3 of 20
Title	RH RV620 - ASIC Main
Doc No.	105-B629xx-00B



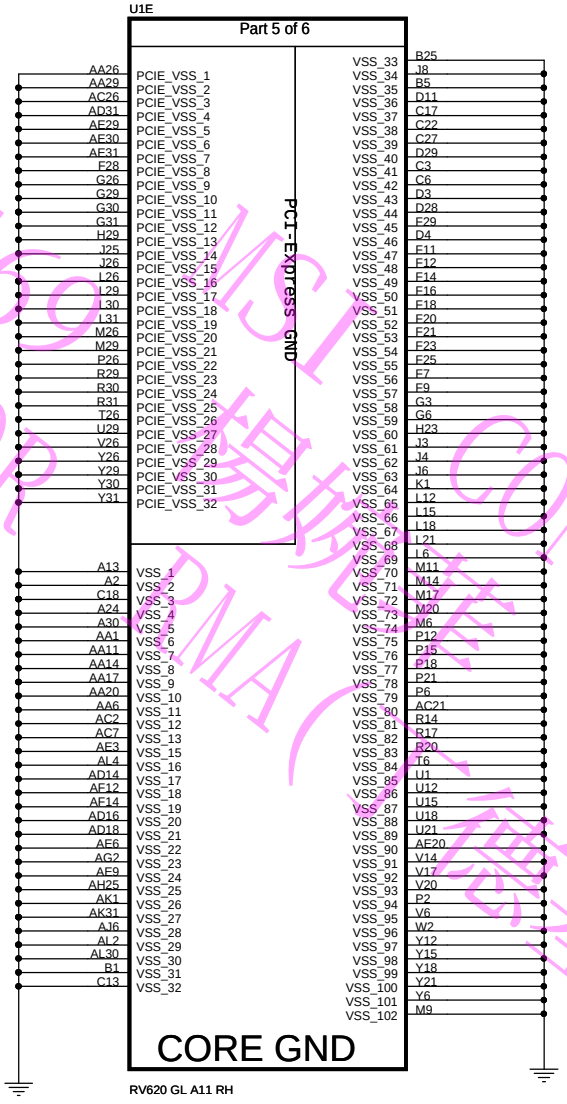
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, April 25, 2008 Rev 03

Sheet 4 of 20

Title: RH RV620 - ASIC TMDP/LVTM Interface

Doc No. 105-B629xx-00B



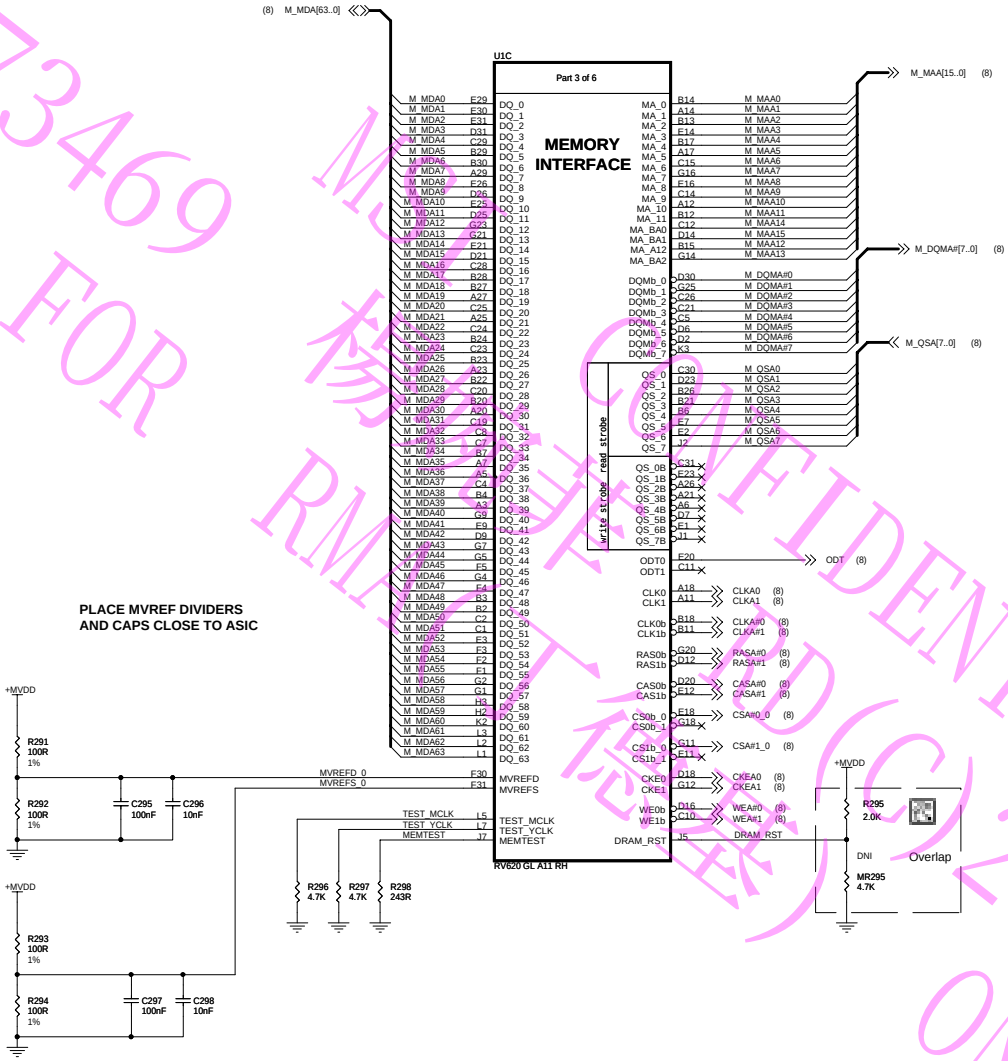
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, April 25, 2008 Rev 03

Sheet 5 of 20

Title RH RV620 - ASIC Ground

Doc No. 105-B629xx-00B



DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

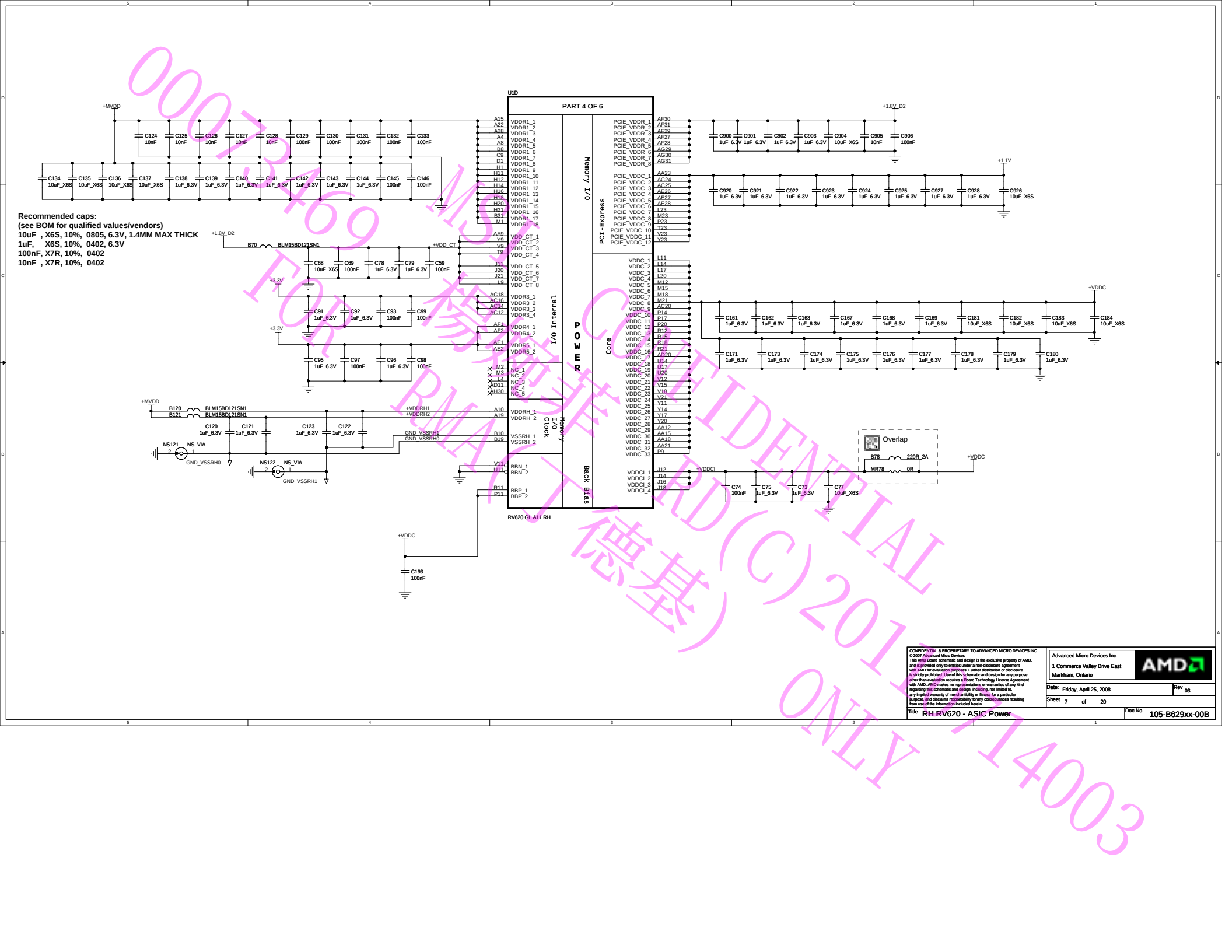
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, April 25, 2008 Rev 03

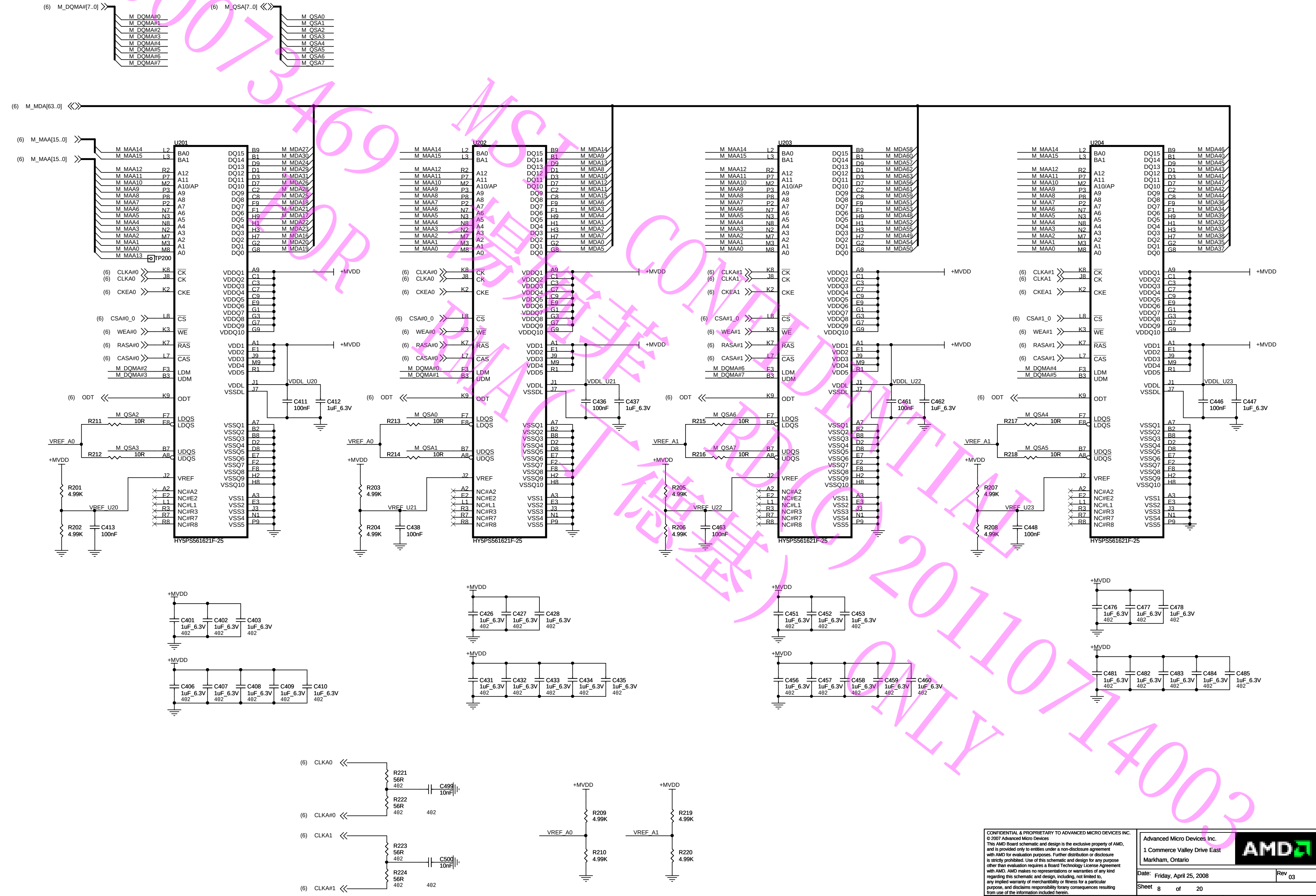
Sheet 6 of 20

Title RH RV620 - ASIC Memory Interface

Doc No. 105-B629xx-00B



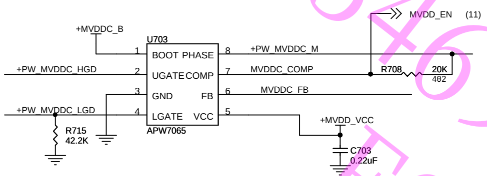
CHANNEL A: RANK 0 256MB DDR2

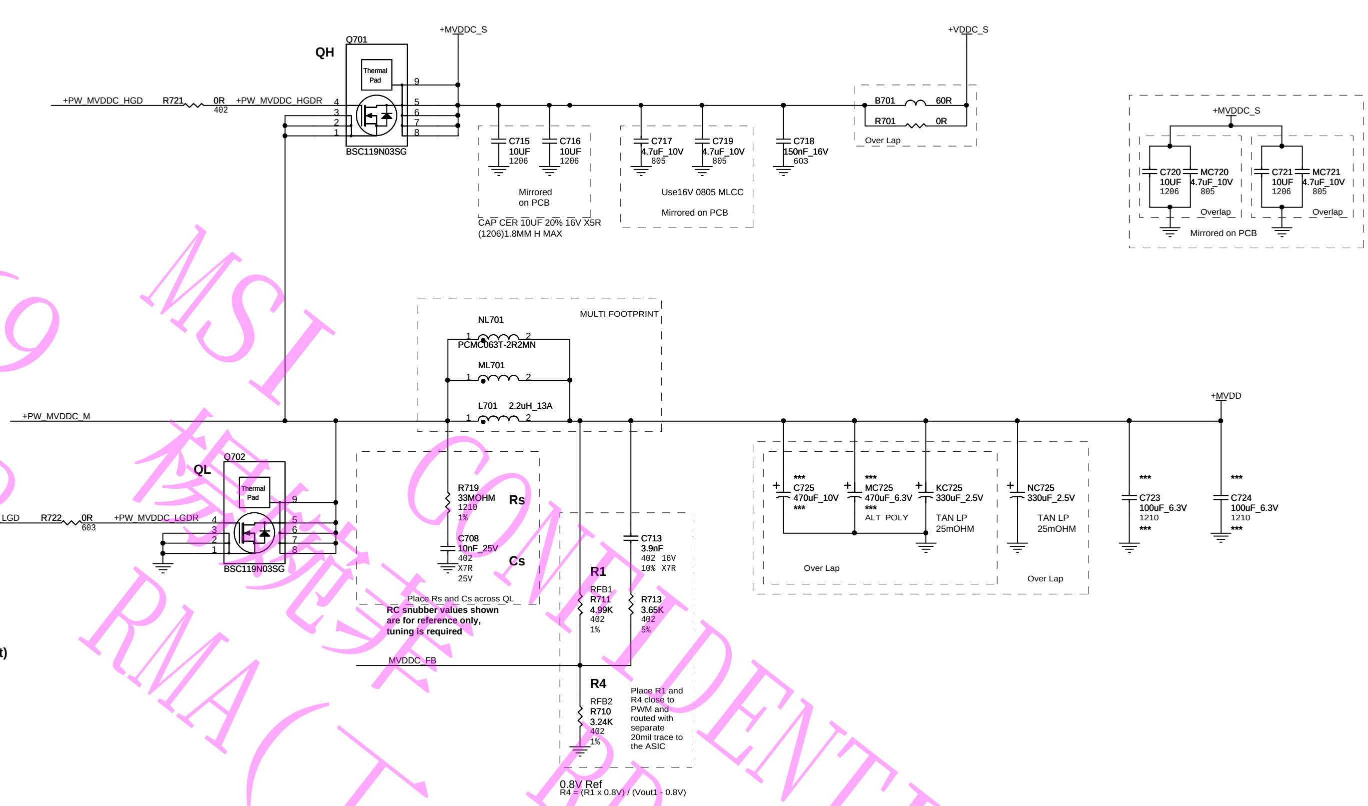


Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

AMD

Date: Friday, April 25, 2008 | Rev 03
Sheet 8 of 20
Title: RH RV620 - DDR2 256MB 64-bit CH. A
Doc No. 105-B629xx-00B

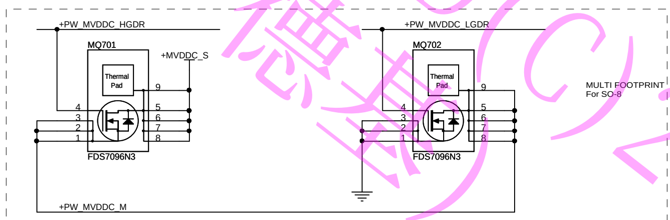



QH
Q701
BSC119N03SG
+MVDDC_S
+PW_MVDDC_HGD
R721 0R 402
+PW_MVDDC_HGDR
C715 10UF 1206
C716 10UF 1206
Mirrored on PCB
CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX
C717 4.7uF_10V 805
C719 4.7uF_10V 805
Use16V 0805 MLCC
Mirrored on PCB
C718 150nF_16V 603
+VDDC_S
B701 60R
R701 0R
Over Lap
+MVDDC_S
C720 10UF 1206
MC720 4.7uF_10V 805
C721 10UF 1206
MC721 4.7uF_10V 805
Overlap
Mirrored on PCB
MULTI FOOTPRINT
NL701 PCMC063T-2R2MN
ML701
L701 2.2uH_13A
+PW_MVDDC_M
+MVDD
QL
Q702
BSC119N03SG
+PW_MVDDC_LGD
R722 0R 603
+PW_MVDDC_LGDR
R719 33MOHM 1210 1% Rs
C708 10nF_25V 402 X7R 25V Cs
Place Rs and Cs across QL
RC snubber values shown are for reference only, tuning is required
MVDDC_FB
C713 3.9nF 402 16V 10% X7R
R1 RFB1 R711 4.99K 402 1%
R713 3.65K 402 5%
R4 RFB2 R710 3.24K 402 1%
Place R1 and R4 close to PWM and routed with separate 20mil trace to the ASIC
0.8V Ref
R4 = (R1 x 0.8V) / (Vout1 - 0.8V)
C725 470uF_10V
MC725 470uF_6.3V ALT POLY
KC725 330uF_2.5V TAN LP 25mOHM
NC725 330uF_2.5V TAN LP 25mOHM
Over Lap
C723 100uF_6.3V 1210
C724 100uF_6.3V 1210

List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

- ANPEC APW7120/APW7065 (12V)
- CAT CAT7583 (12V)
- INTERSIL ISL6545
- NEXSEM NX2114/2307
- RICHTEK RT9214/RT8101
- OnSemi ON1582
- uPI UP6101 (No Ext_Vref in)
- uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)



SMPS02- Regulator for MVDD

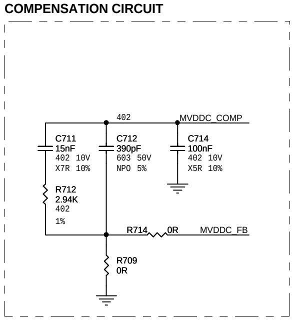
Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	1.82V (1.78V~1.86V)	10K p/n 3160100200G	7.87K p/n 3160787100G
	2.03V (1.99V~2.08V)	10K p/n 3160100200G	6.49K p/n 3160649100G

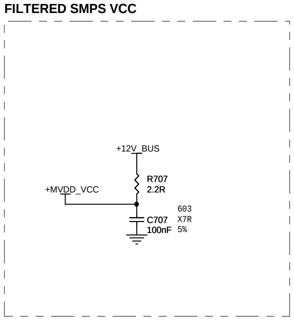
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

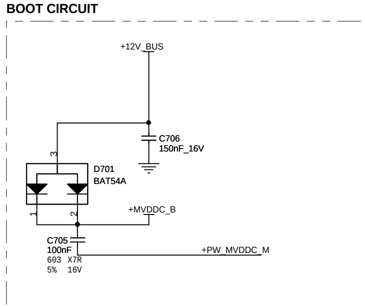
COMPENSATION CIRCUIT



FILTERED SMPS VCC



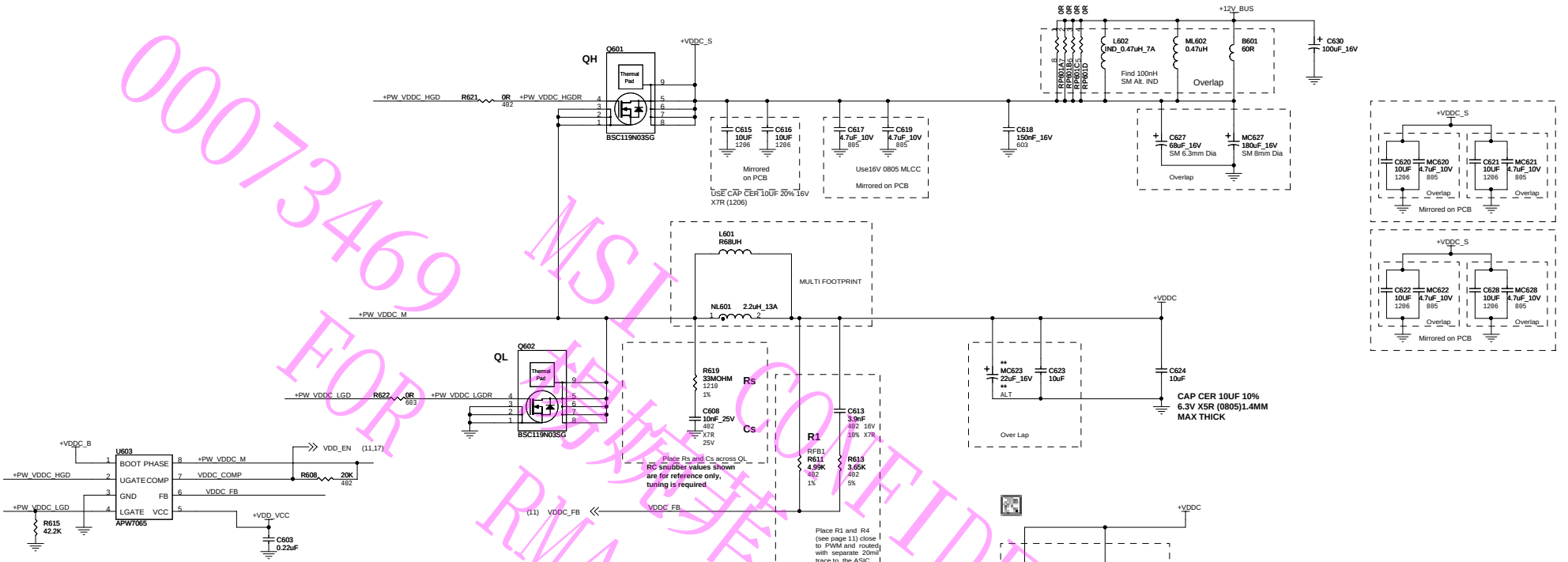
BOOT CIRCUIT



Layout guideline for Nexsem NX2114/2307

1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario
Date: Friday, April 25, 2008 Rev 03
Sheet 9 of 20
Title RH RV620 - MVDD SMPS Doc No. 105-B629xx-00B



List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7120/APW7065 (12V)
CAT CAT7583 (12V)
INTERSIL ISL6545
NEXSEM NX2114/2307
RICHTEK RT9214/RT8101
OnSemi ON1582
uPI UP6101 (No Ext_Vref in)

Layout guideline for Nexsem NX2114/2307

1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

SMPS02- Regulator for VDDC

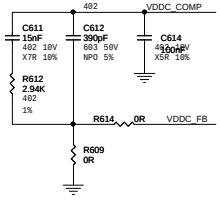
Vout = 0.9V ~ 1.2V

Part	Vout	RFB1	RFB2 (Page 11)
0.8V Ref	1.20V (1.18V~1.22V)	10K p/n 3160100200G	20K p/n 3160200200G
	1.12V (1.10V~1.14V)	10K p/n 3160100200G	24.9K p/n 3160249200G

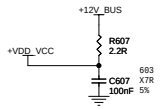
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

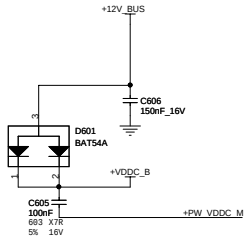
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT

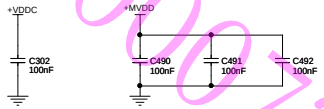


Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, April 25, 2008 Rev 03
Sheet 10 of 20
Title RH RV620 - VDDC SMPS
Doc No. 105-B629xx-00B

Stitching Capacitors

THESE ARE STITCHING CAPACITORS. PLACEMENT IS LAYOUT DEPENDANT.

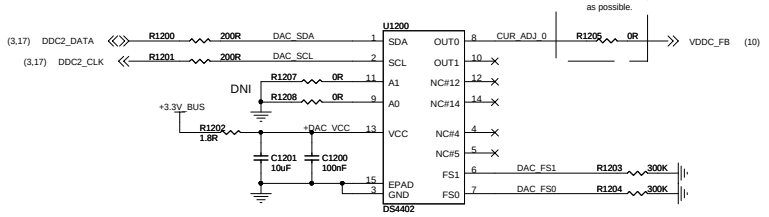


Place C490-492 near layer transitions (top/bottom).
THIS IS LAYOUT DEPENDENT.

I2C control of VDDC

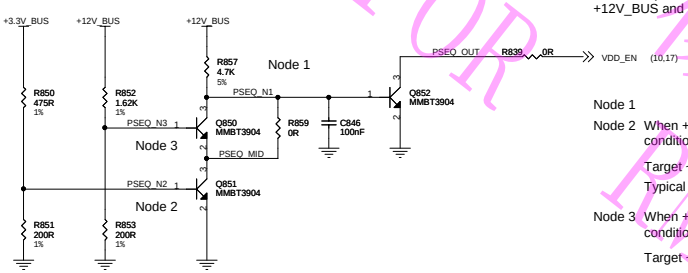
CIRCUITRY SHOULD BE PLACED CLOSE TO VDDC SMPS (U601) IN ORDER TO REDUCE STUB LENGTHS ON FB LINE.

Should be placed as close to VDDC SPMS as possible.



Power up/down Sequencing

Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.



Node 1

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

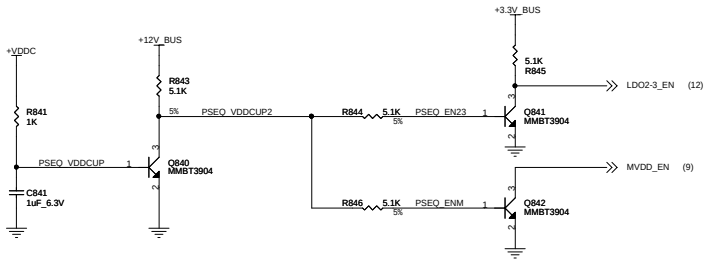
Typical trigger when +3.3V ramps above 2.2V (650mV)

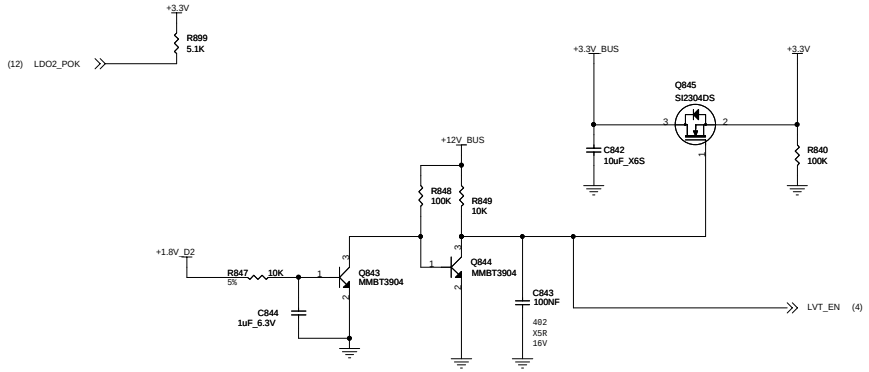
Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

When +12V_BUS ramps above min Vbe, SMPS_EN will be held low



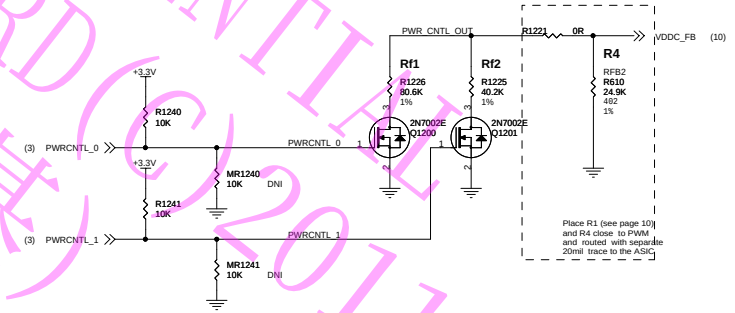


Power Play

VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1=80.6k, Rf2=40.6k, RFB2=80.6k	Rf1= Rf2=	
0	0	0.9		
0	1	1.0		
1	0	1.1		
1	1	1.2		

PLEASE SEE POWER PLAY TABLE AND BIOS FOR FULL IMPLEMENTATION DETAILS;

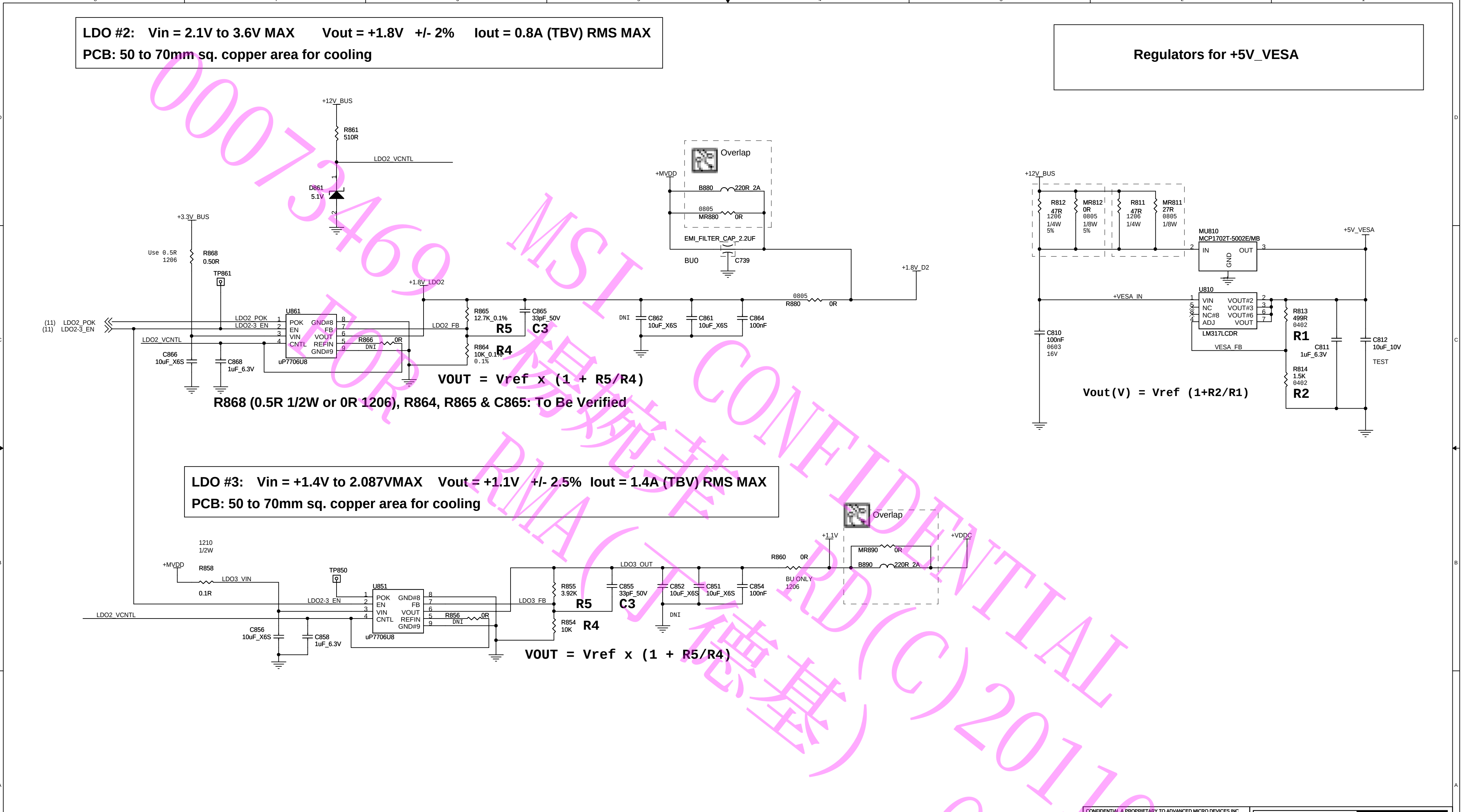


Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, April 25, 2008 Rev 03

Sheet 11 of 20

Title RH RV620 - VOLTAGE CONTROL, POWER SEQUENCING Doc No: 105-B629xx-00B


LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling
Regulators for +5V_VESA
+12V_BUS
R861 510R
LDO2_VCNTL
D861 5.1V
+3.3V_BUS
Use 0.5R 1206
R868 0.50R
TP861
Overlap
+MVDD
B880 220R_2A
MR880 0R
EMI_FILTER_CAP_2.2UF
BUO
C739
+1.8V_D2
+1.8V_LDO2
R880 0R
LDO2_POK
LDO2-3_EN
U861
POK EN VIN CNTL GND#8 FB VOUT REFIN GND#9
uP7706U8
R866 0R DNI
LDO2_FB
R865 12.7K_0.1%
C865 33pF_50V
R5
C3
R864 10K_0.1%
R4
C862 10uF_X6S
C861 10uF_X6S
C864 100nF
DNI
C866 10uF_X6S
C868 1uF_6.3V
VOUT = Vref x (1 + R5/R4)
R868 (0.5R 1/2W or 0R 1206), R864, R865 & C865: To Be Verified
R812 47R 1206 1/4W 5%
MR812 0R 0805 1/8W 5%
R811 47R 1206 1/4W
MR811 27R 0805 1/8W
MU810 MCP1702T-5002E/MB
IN OUT GND
+5V_VESA
+VESA_IN
U810
VIN NC NC#8 ADJ VOUT#2 VOUT#3 VOUT#6 VOUT
LM317LCDR
VESA_FB
R813 499R 0402
R1
C811 1uF_6.3V
C812 10uF_10V
TEST
R814 1.5K 0402
R2
C810 100nF 0603 16V
Vout(V) = Vref (1+R2/R1)
LDO #3: Vin = +1.4V to 2.087VMAX Vout = +1.1V +/- 2.5% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling
1210 1/2W
R858 0.1R
LDO3_VIN
TP850
U851
uP7706U8
LDO3_OUT
LDO3_FB
R856 0R DNI
R855 3.92K
C855 33pF_50V
R5
C3
R854 10K
R4
C852 10uF_X6S
C851 10uF_X6S
C854 100nF
DNI
C856 10uF_X6S
C858 1uF_6.3V
VOUT = Vref x (1 + R5/R4)
+1.1V
R860 0R
BU ONLY 1206
+VDDC
MR890 0R
B890 220R_2A

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

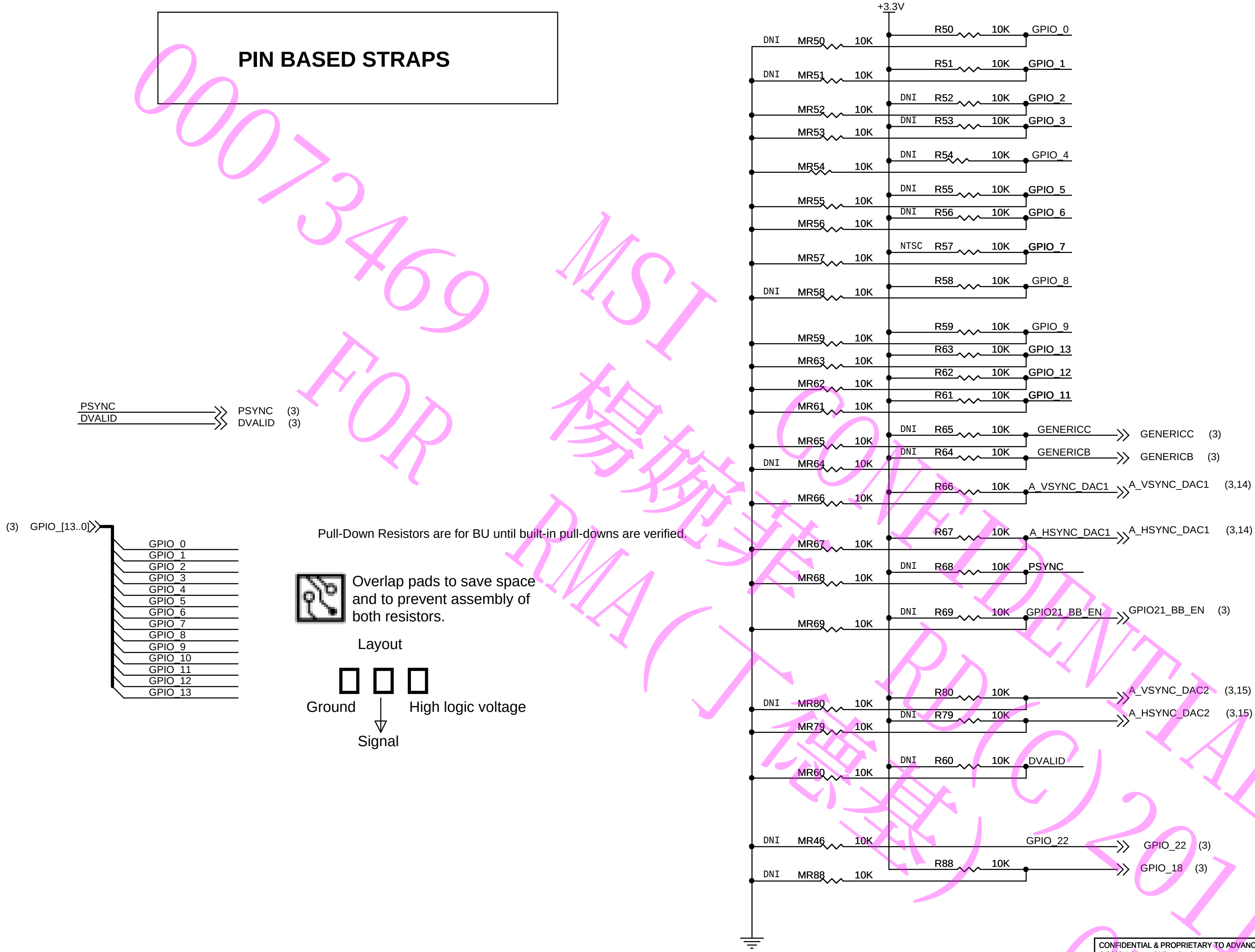
Date: Friday, April 25, 2008 | Rev 03

Sheet 12 of 20

Title: RH RV620 - LINEAR REGULATORS

Doc No. 105-B629xx-00B

PIN BASED STRAPS


+3.3V
R50 10K GPIO_0
R51 10K GPIO_1
DNI R52 10K GPIO_2
DNI R53 10K GPIO_3
DNI R54 10K GPIO_4
DNI R55 10K GPIO_5
DNI R56 10K GPIO_6
NTSC R57 10K GPIO_7
R58 10K GPIO_8
R59 10K GPIO_9
R63 10K GPIO_13
R62 10K GPIO_12
R61 10K GPIO_11
DNI R65 10K GENERICC
DNI R64 10K GENERICB
R66 10K A_VSYNC_DAC1
R67 10K A_HSYNC_DAC1
DNI R68 10K PSYNC
DNI R69 10K GPIO21_BB_EN
R80 10K
DNI R79 10K
DNI R60 10K DVALID
R88 10K
DNI MR50 10K
DNI MR51 10K
MR52 10K
MR53 10K
MR54 10K
MR55 10K
MR56 10K
MR57 10K
DNI MR58 10K
MR59 10K
MR63 10K
MR62 10K
MR61 10K
MR65 10K
DNI MR64 10K
MR66 10K
MR67 10K
MR68 10K
MR69 10K
DNI MR80 10K
MR79 10K
MR60 10K
DNI MR46 10K GPIO_22
DNI MR88 10K
GENERICC (3)
GENERICB (3)
A_VSYNC_DAC1 (3,14)
A_HSYNC_DAC1 (3,14)
GPIO21_BB_EN (3)
A_VSYNC_DAC2 (3,15)
A_HSYNC_DAC2 (3,15)
GPIO_22 (3)
GPIO_18 (3)
PSYNC
DVALID
PSYNC (3)
DVALID (3)
(3) GPIO_[13..0]
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
Pull-Down Resistors are for BU until built-in pull-downs are verified.
Overlap pads to save space and to prevent assembly of both resistors.
Layout
Ground
High logic voltage
Signal

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - ATI Internal Use Only - Reserved (Default: 00)

GPIO(4) - DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(7) - TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

GPIO(8) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0] IF
BIOS_ROM_EN=1 [default] (GPIO_22)
Atmel - AT25F512A (512 kbit) 0010
AT25F1024A (1 Mbit) 0011
ST Microelectronics - M25P05A (512 kbit) 0100
M25P10A (1 Mbit) 0101
M25P20 (2 Mbit) 0101
Chingis (formerly PMC) -
Pm25LV512 (512 kbit) 0100
Pm25LV010 (1 Mbit) 0101

If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.
(Config 3 = don't care).

x000	128MB
x001	256MB
x010	64MB
x011	32MB
x100	512MB
x101	1GB
x110	2GB
x111	4GB

GENERICC, GENERICB - ATI Internal Use Only - Reserved (Default: 0)

VSYNC - VIP_DEVICE_STRAP_EN
0: Driver would ignore the value sampled on VHAD_0 during reset
1: Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no).

HSYNC - ATI Internal Use Only - Reserved (Default 0)

PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO_21 - ATI Internal Use Only - Reserved (Default: 0)

VSYNC - DDR2 VENDOR SELECT ATI Board Feature I
(see GPIO_18)

HSYNC2 - ATI Internal Use Only - Reserved (Default: 0)

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

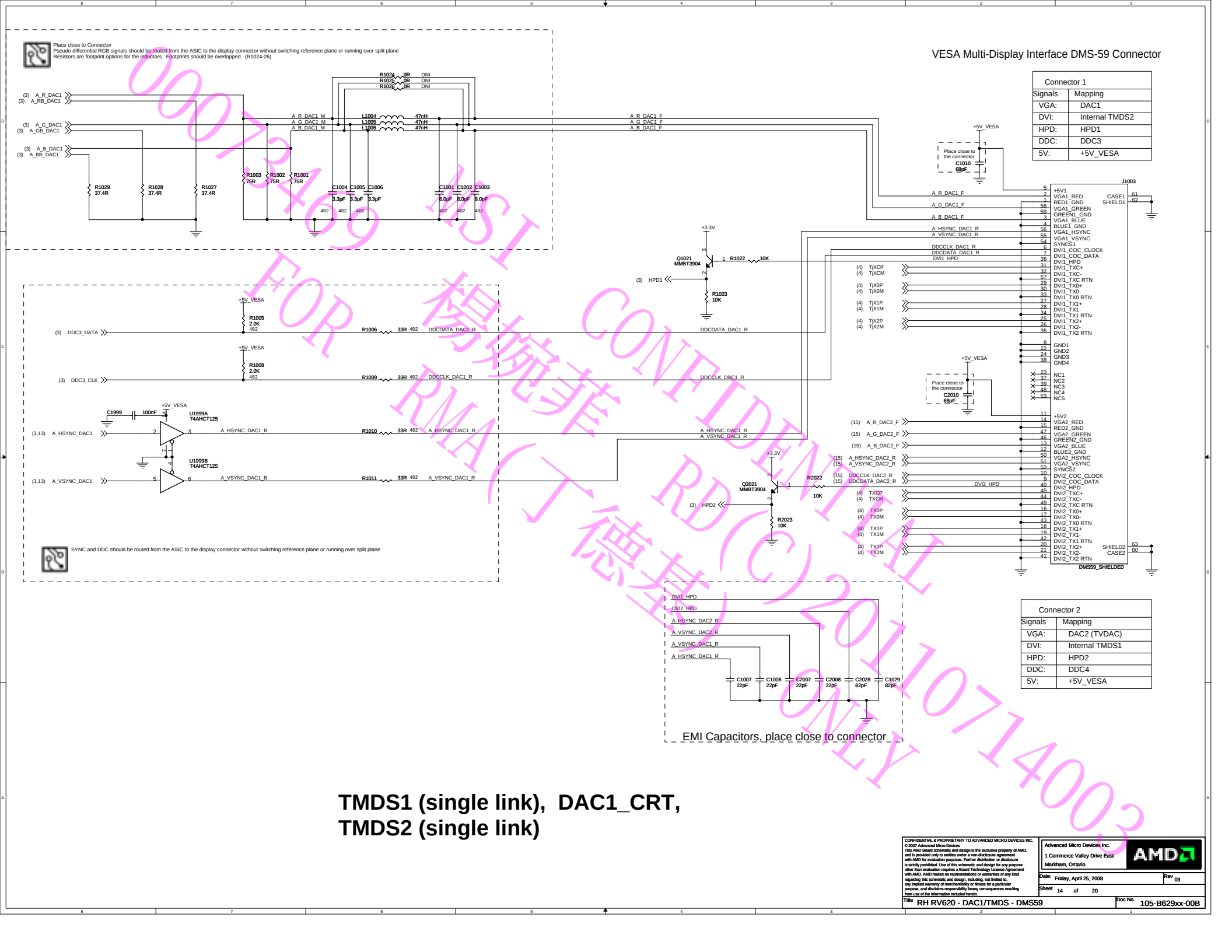
GPIO_22_ROMCSb - Enable external BIOS ROM device (Default 1)

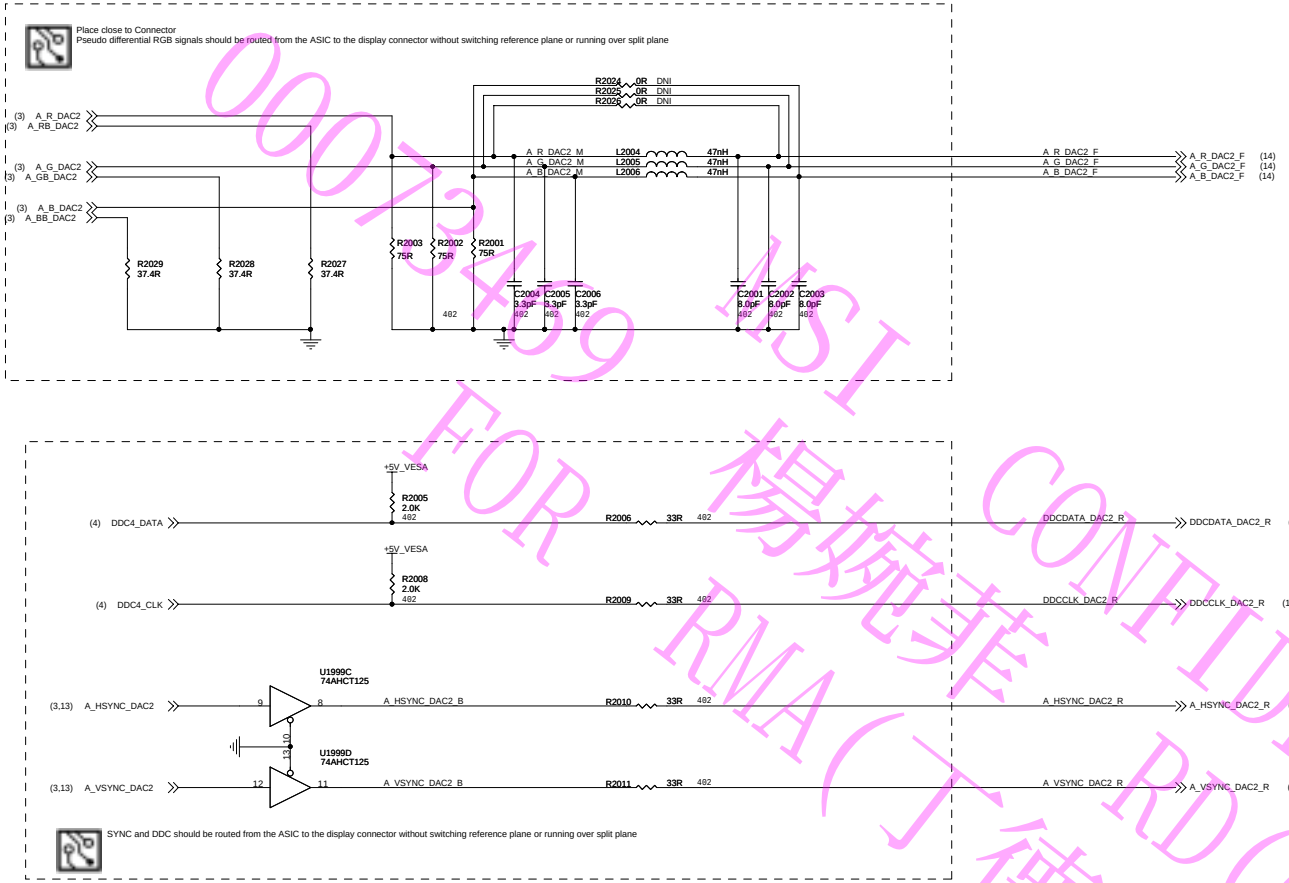
GPIO_18 - DDR2 MEM VENDOR [V2SYNC:GPIO_18] ATI Board Feature I

QUIMONDA	[0:0]
HYNIX	[0:1]
SAMSUNG	[1:0]

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, April 25, 2008 Rev 03
Sheet 13 of 20
Title RH RV620 - STRAPS AND CROSSFIRE Doc No. 105-B629xx-00B

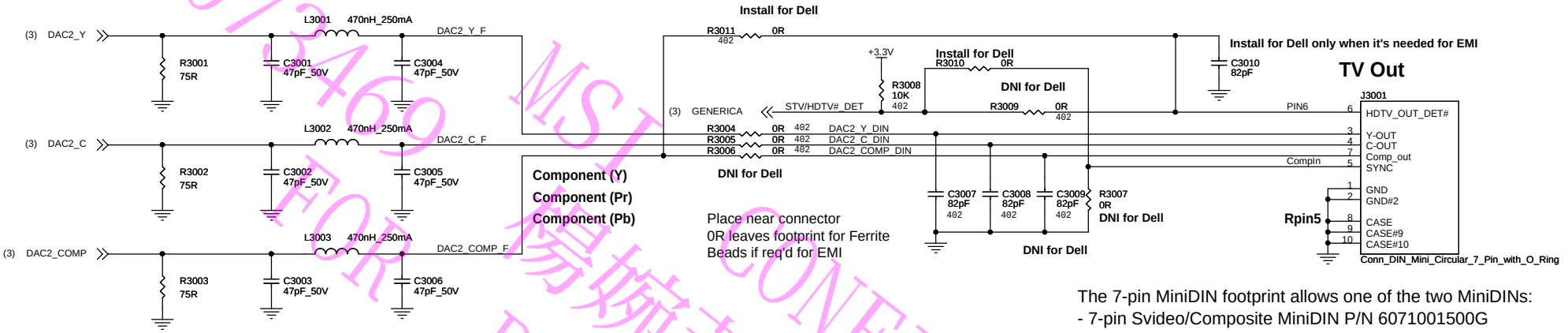




DAC2_CRT

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

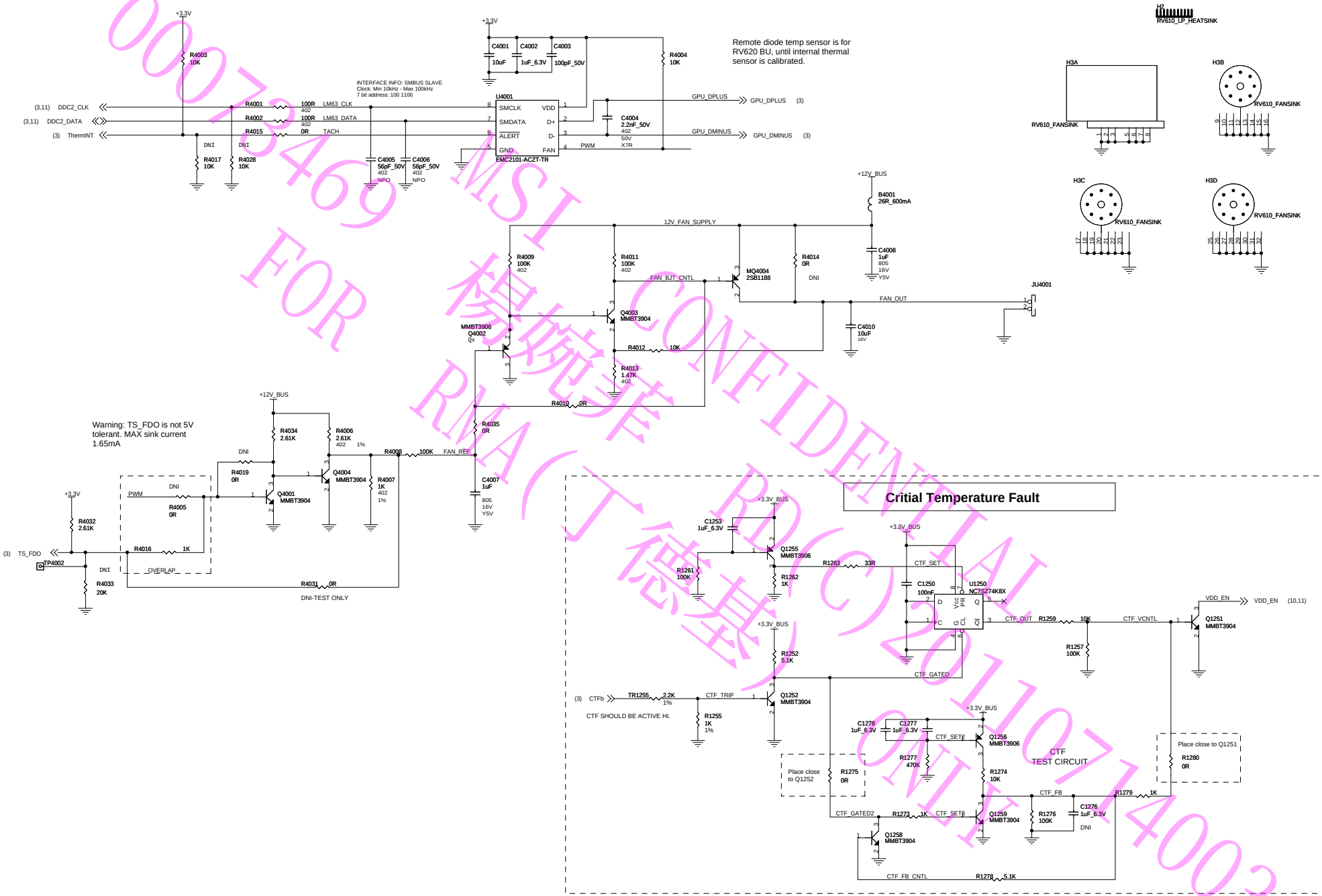
Date:	Friday, April 25, 2008
Rev	03
Sheet	15 of 20
Title	RH RV620 - DAC2
Doc No.	105-B629xx-00B



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, April 25, 2008	Rev 03
Sheet 16 of 20	
Title RH RV620 - TVO, DAC1	Doc No. 105-B629xx-00B



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Friday, April 25, 2008
Rev	03
Sheet	17 of 20
Title	RH RV620 - THERMAL MANAGEMENT
Doc No.	105-B629xx-00B

DVI/VGA SCREWS

ASSY-SCREW2

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW5

SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

ASSY-SCREW4

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW3

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW1

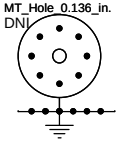
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY1

BRACKET

LP, TOP TAB, DIN, Dual DVI

MT1
MT_Hole_0.136_in.
DNI



SK1

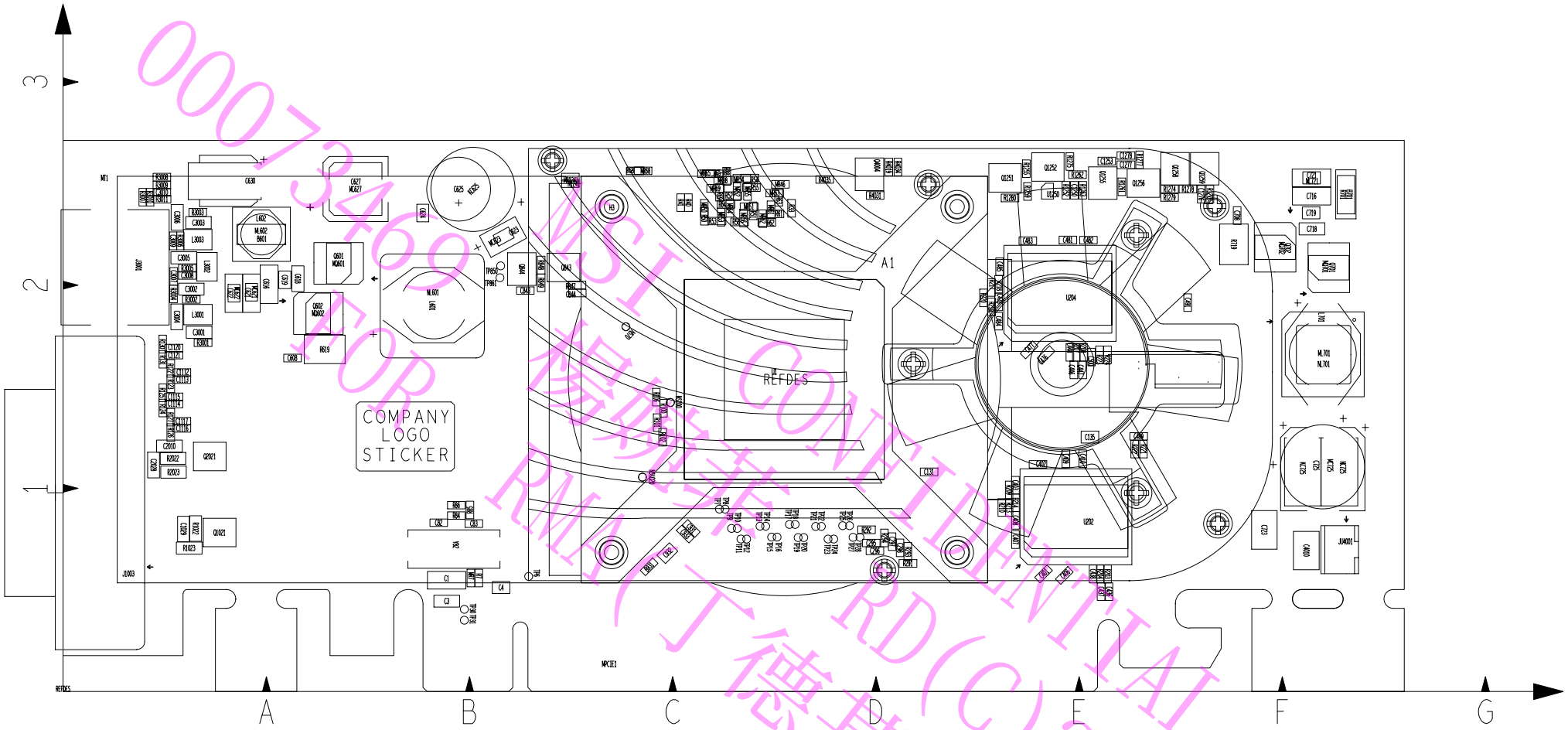
BGA_Socket_RV620

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, April 25, 2008 | Rev 03

Sheet 18 of 20

Title RH RV620 - MECHANICAL | Doc No. 105-B629xx-00B



AMD
ADVANCED MICRO DEVICES
PCBCAD GROUP

RH RV620 256MB DDR2 V0+DMS59 6L LP
PN 109-B62931-00B
MARCH 26, 2008
DESIGNER DORINA/SVETA/RAMESH

ASSEMBLY TOP
SHEET 1 OF 2

RESTRICTION NOTICE

RH RV620 256MB DDR2 V0+DMS59 6L LP
PN 109-B62931-00B
MARCH 26, 2008
DESIGNER DORINA\SVETA\RAMESH

AMD
ADVANCED MICRO DEVICES
PCBCAD GROUP