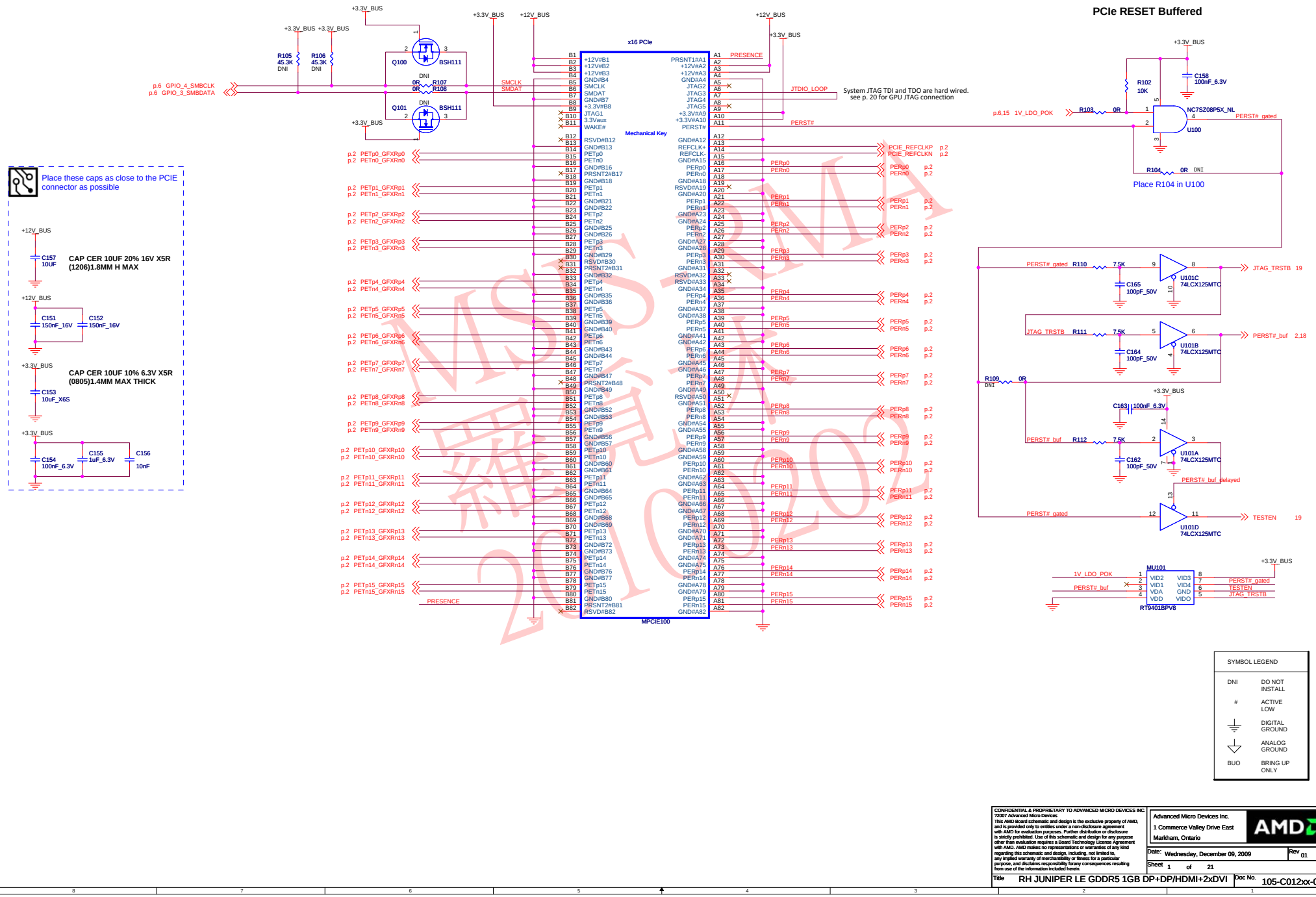
PCI-EXPRESS EDGE CONNECTOR

CORVETTE

1.Add PCIe Reset Buffered Circuit U101,MU101



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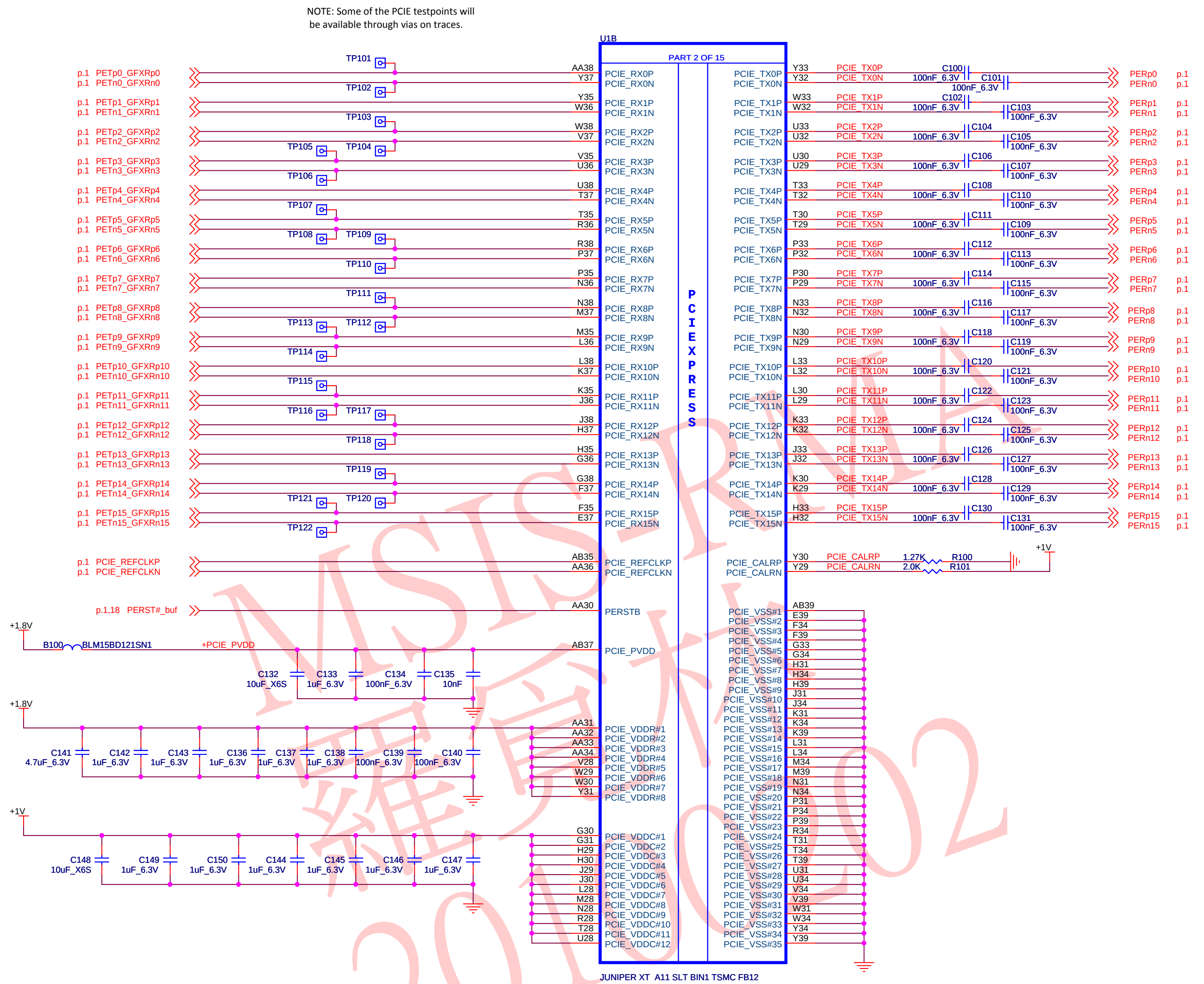
(2) JUNIPER PCIe Interface



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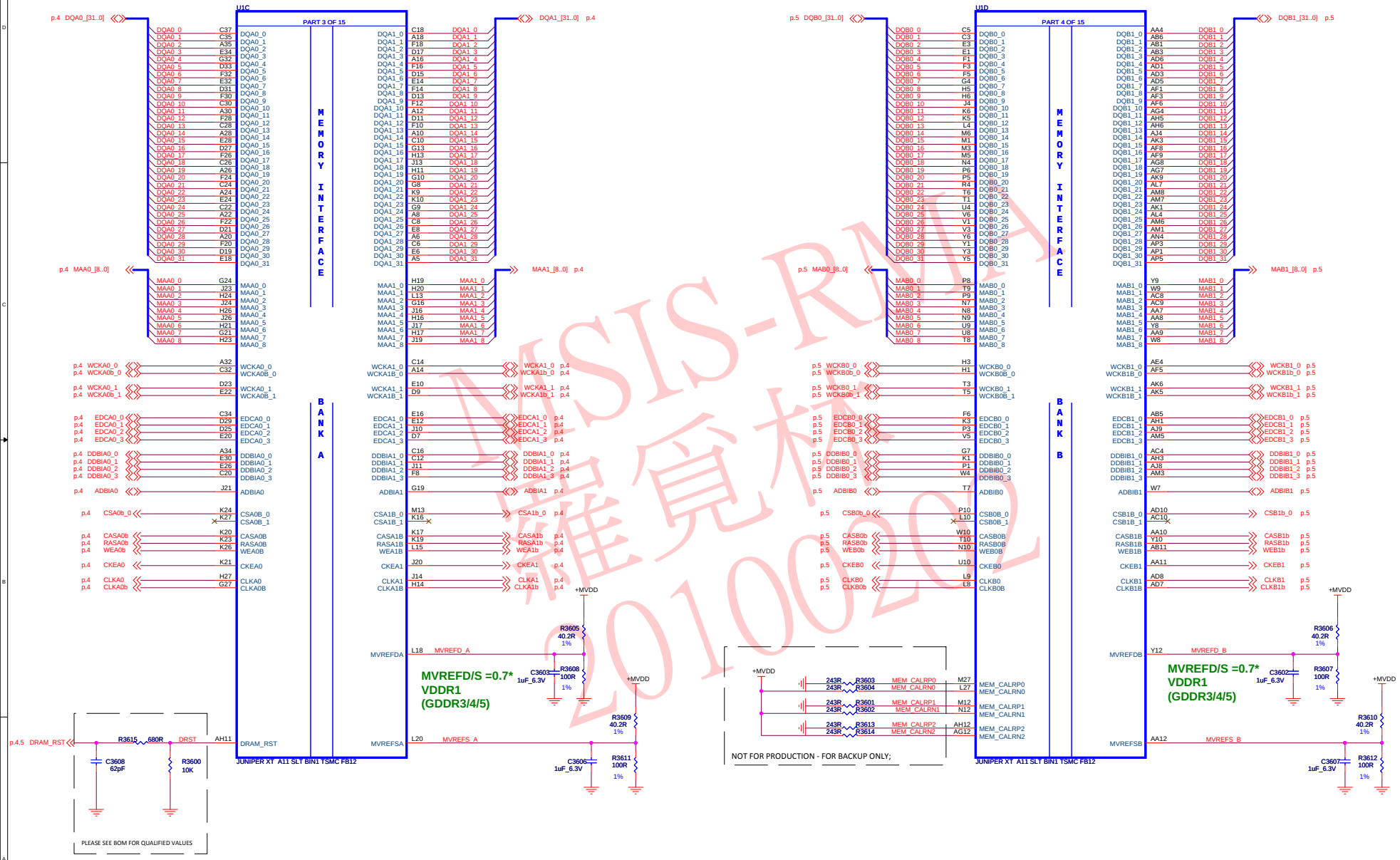
(3) JUNIPER MEM Interface Ch A&B



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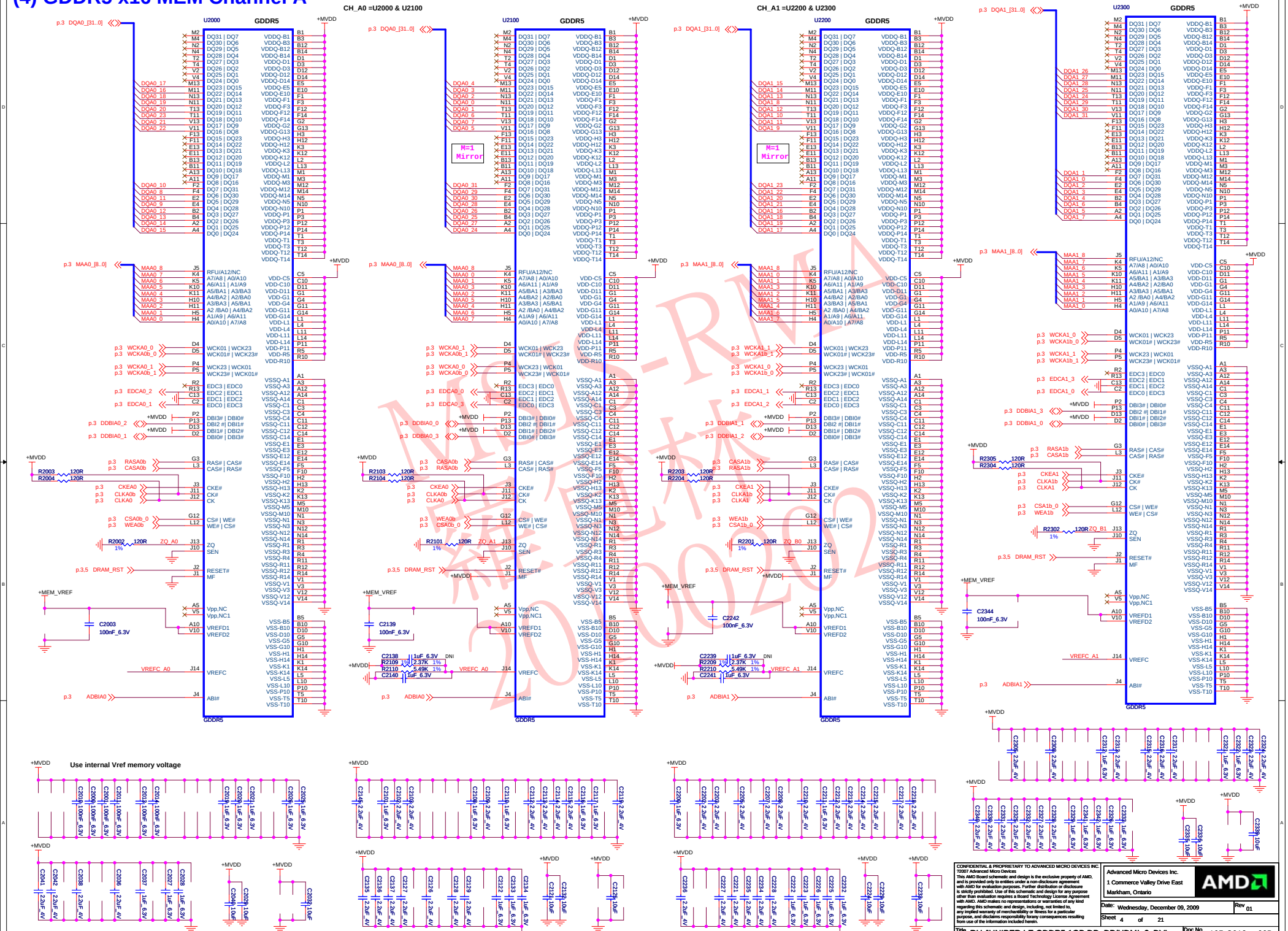
(4) GDDR5 x16 MEM Channel A



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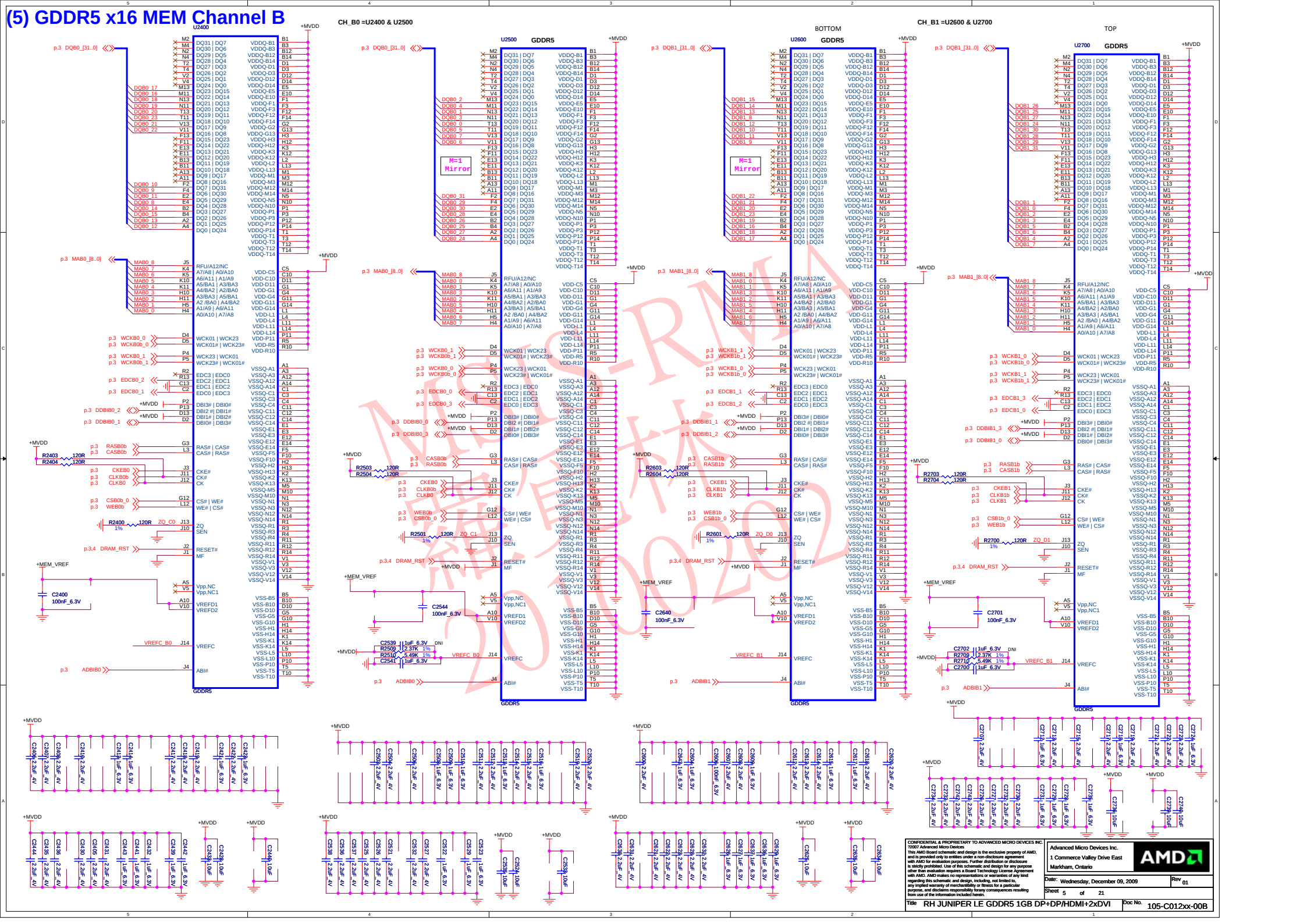
(5) GDDR5 x16 MEM Channel B



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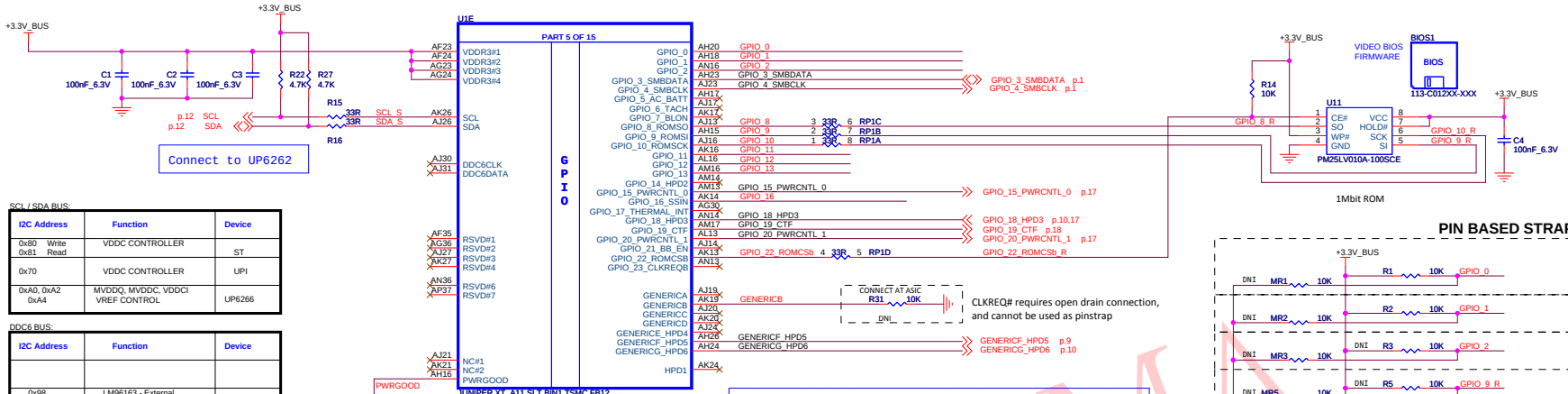
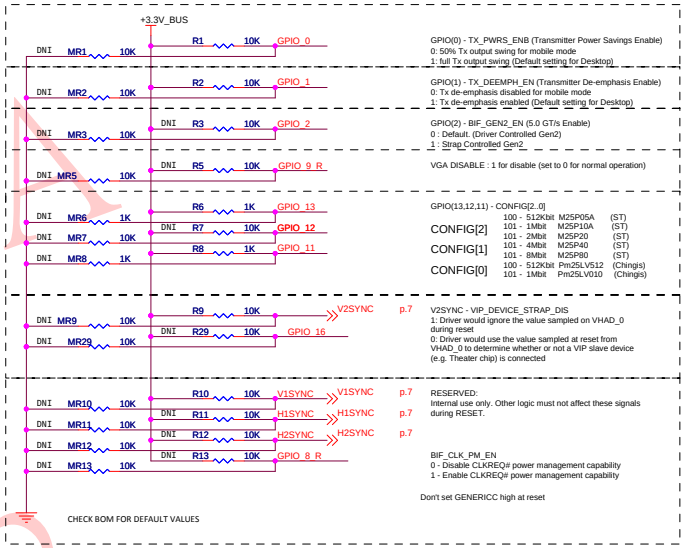
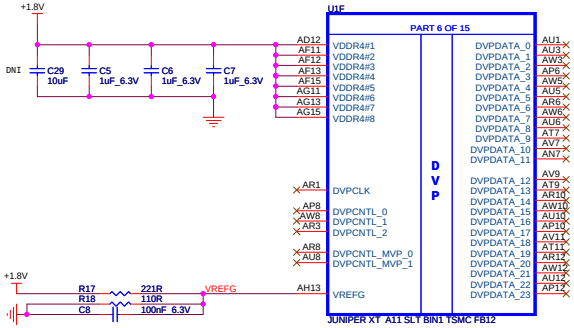
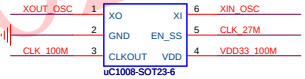
(06) JUNIPER GPIOs Strap CF XTAL OSC

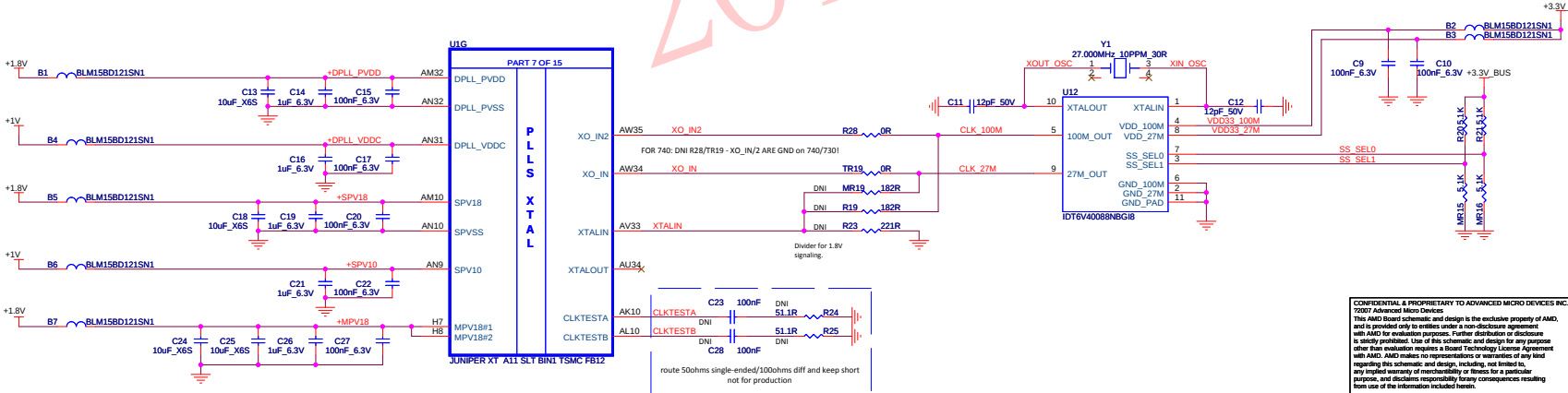


PIN BASED STRAPS









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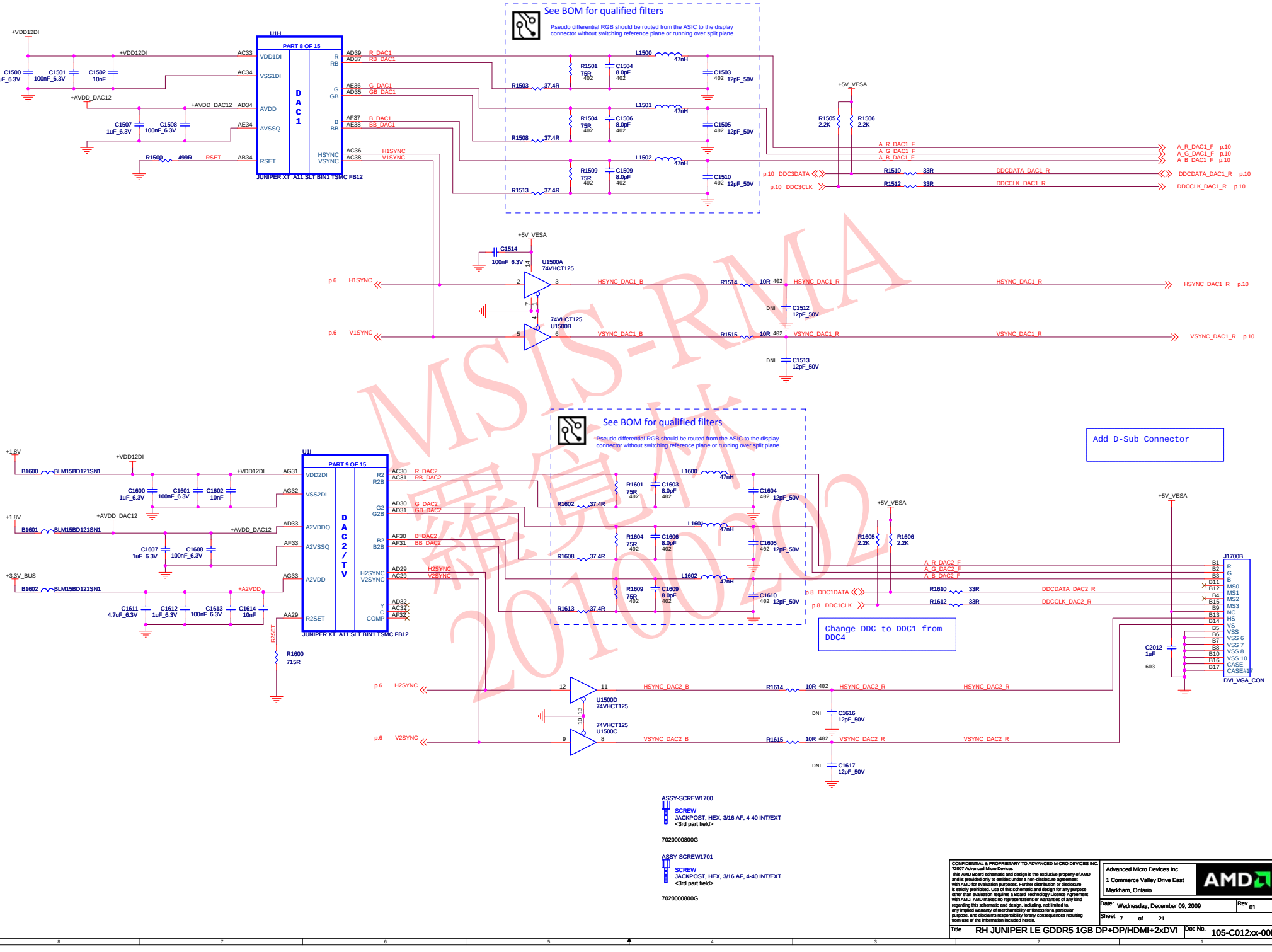
(07) JUNIPER DAC1 and DAC2



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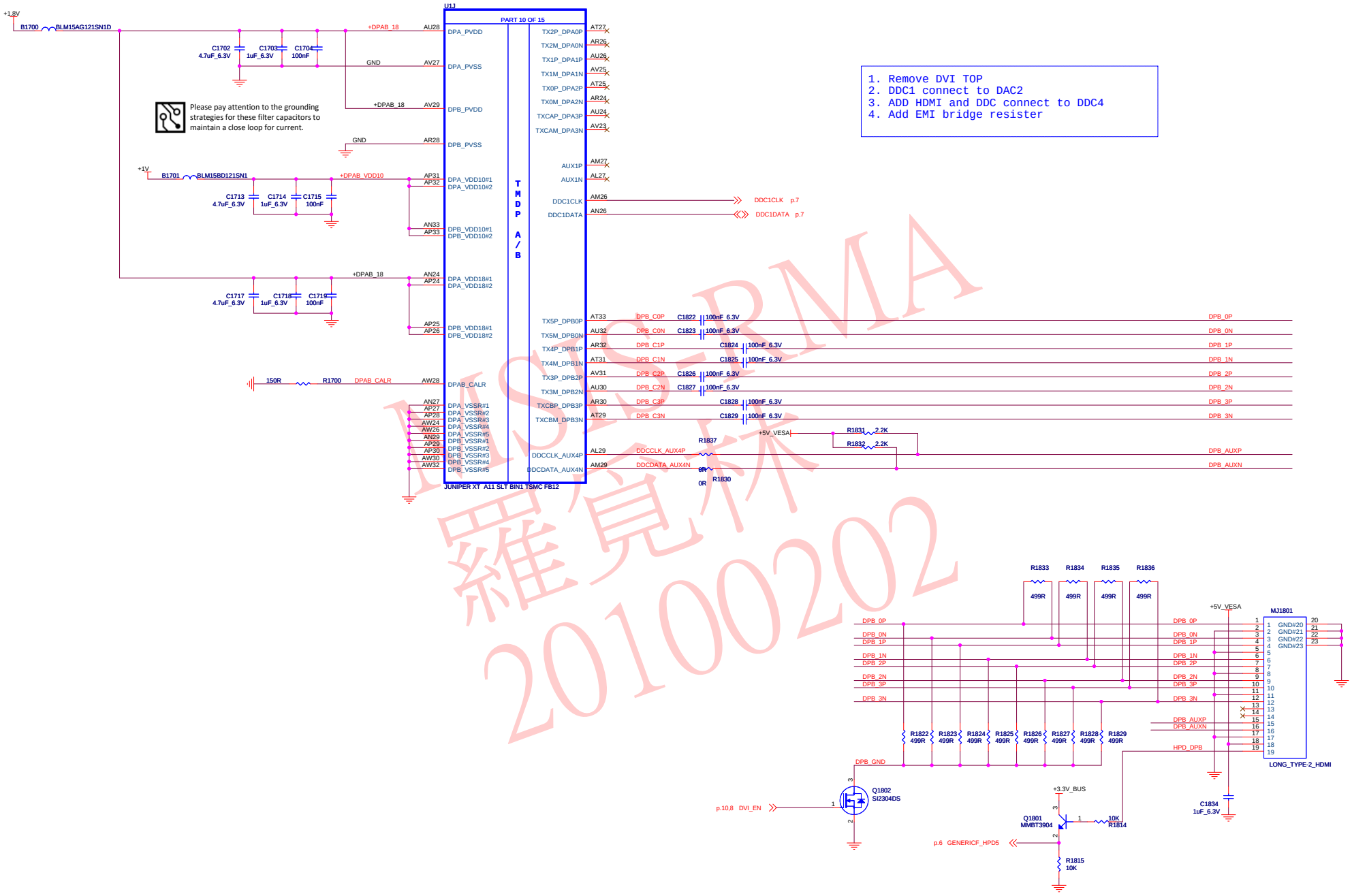
(08) JUNIPER TMDP A&B dDVI-I TOP



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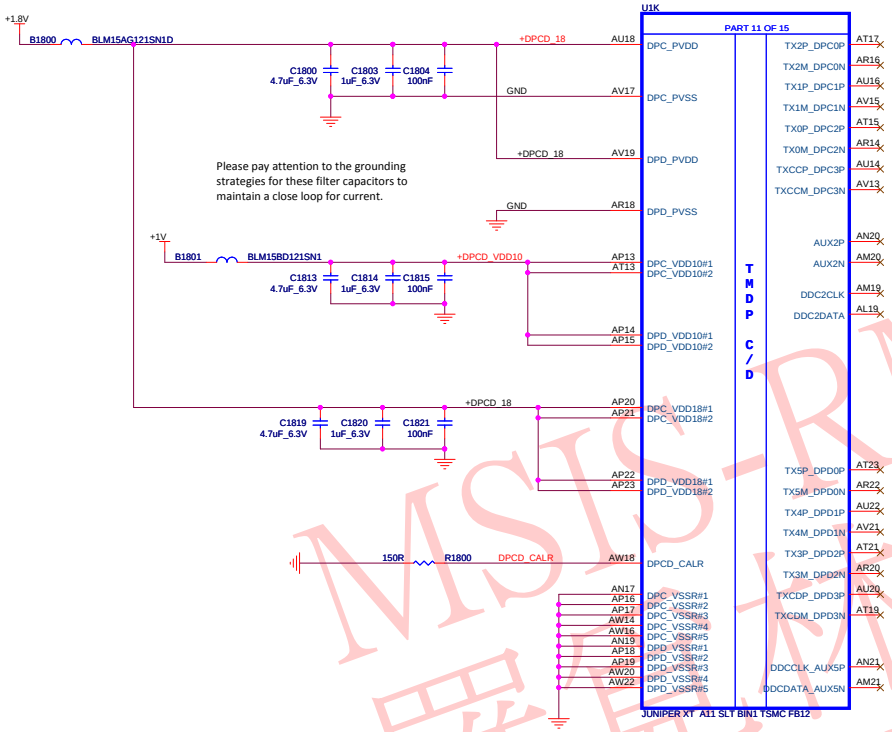
(09) JUNIPER Display Port C & Display Port/HDMI D



1.Removed DP,HDMI Circuit

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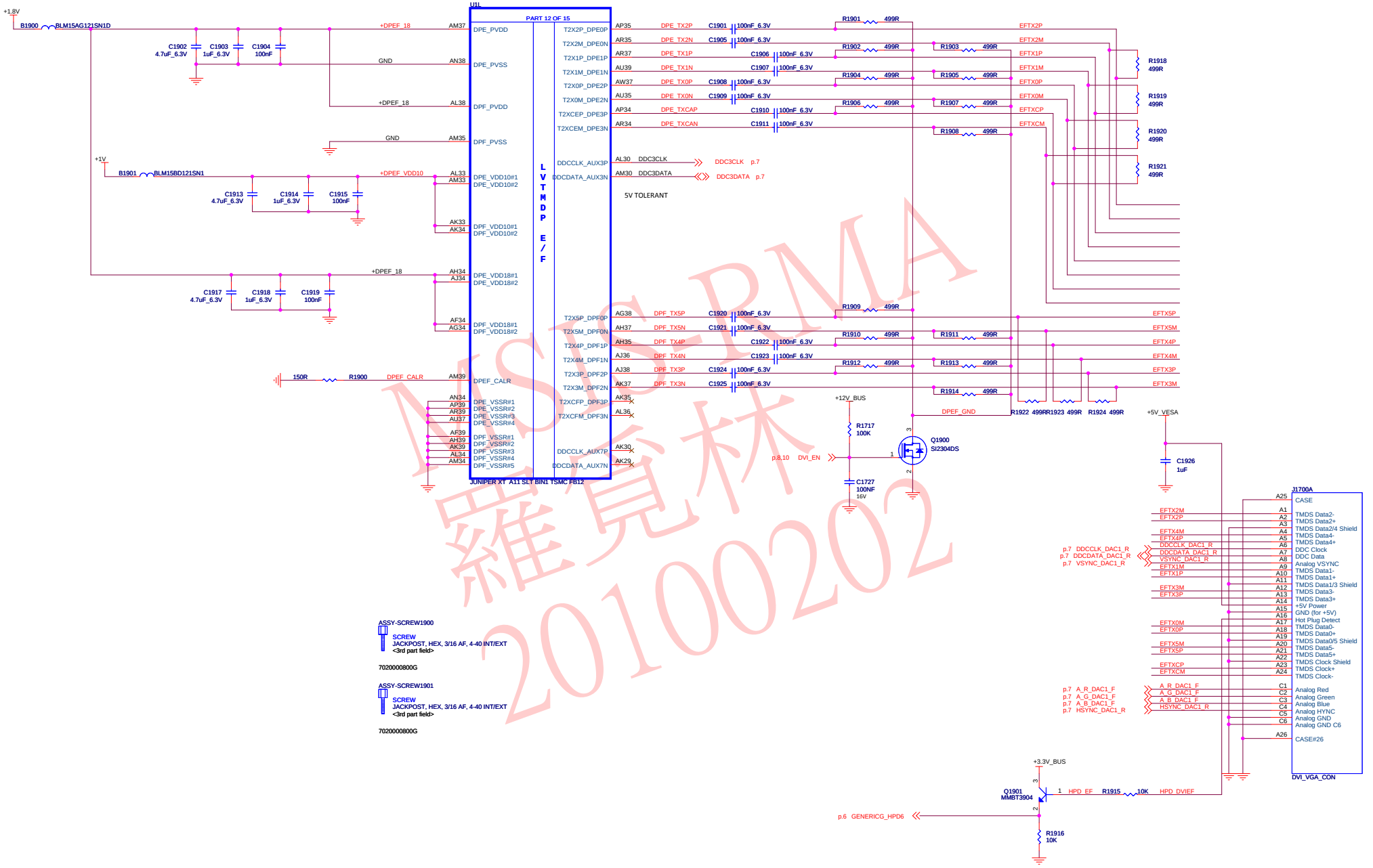
(10) JUNIPER LVTMDP E&F dDVI-I BOTTOM



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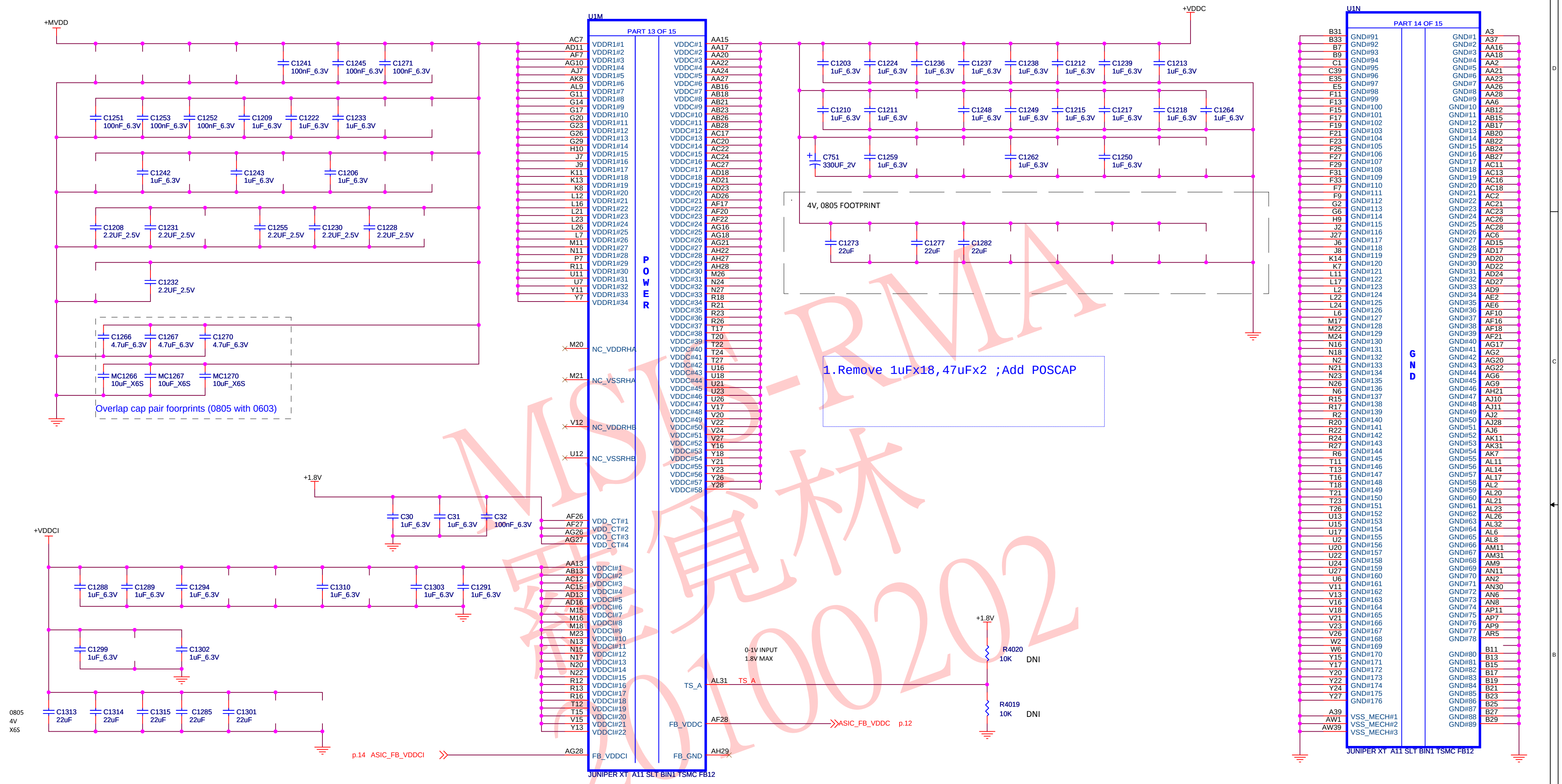
(11) JUNIPER Power & GND



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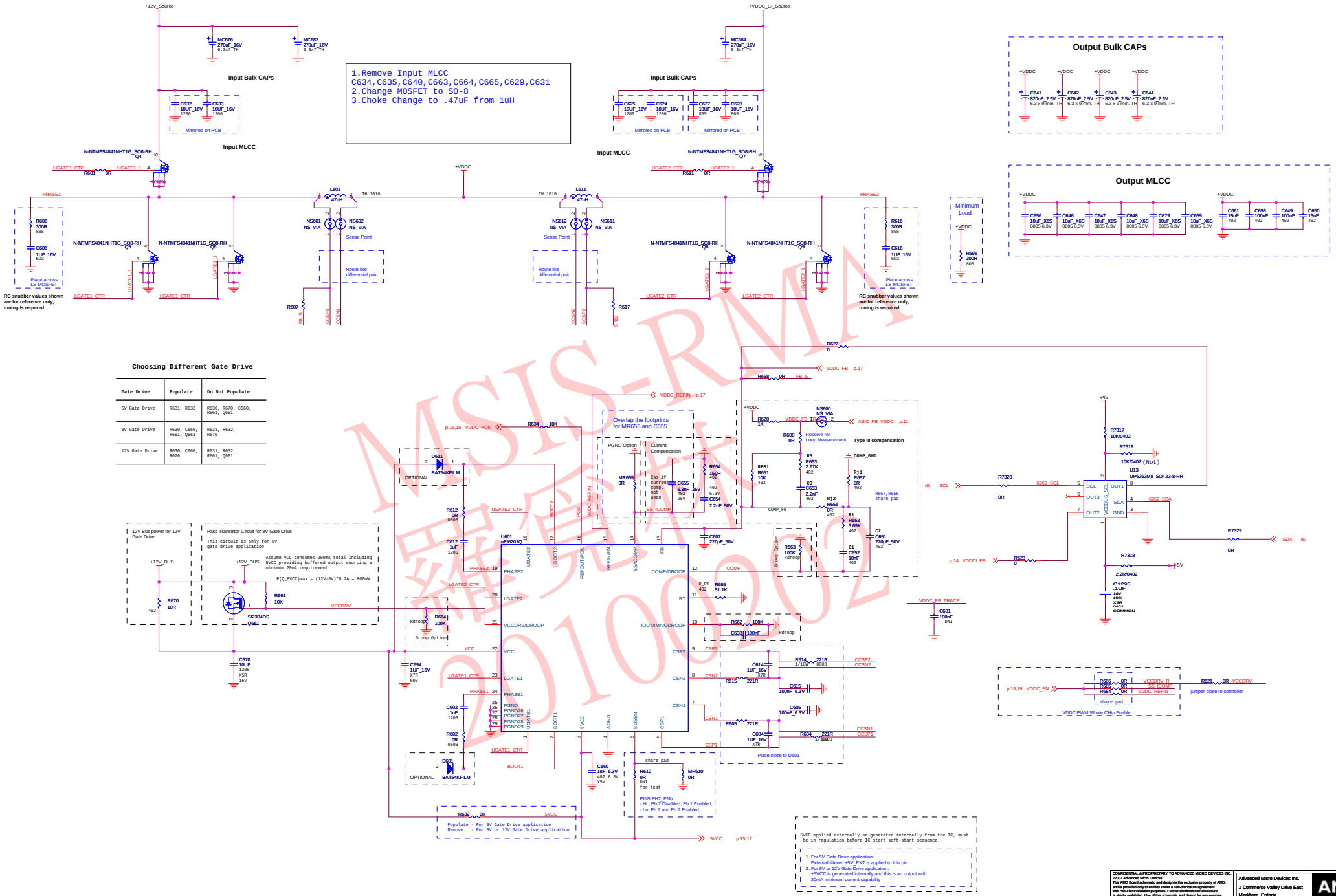

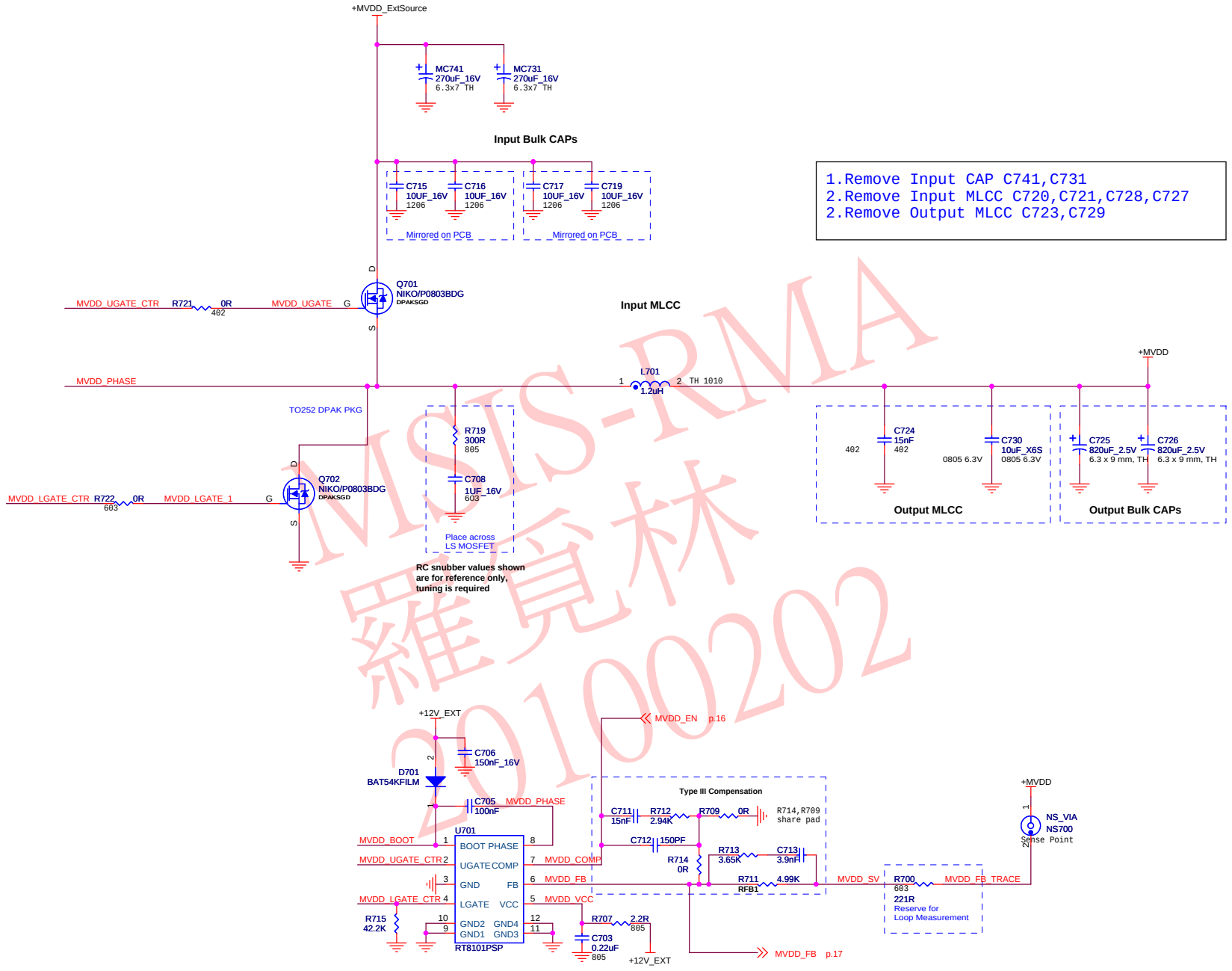

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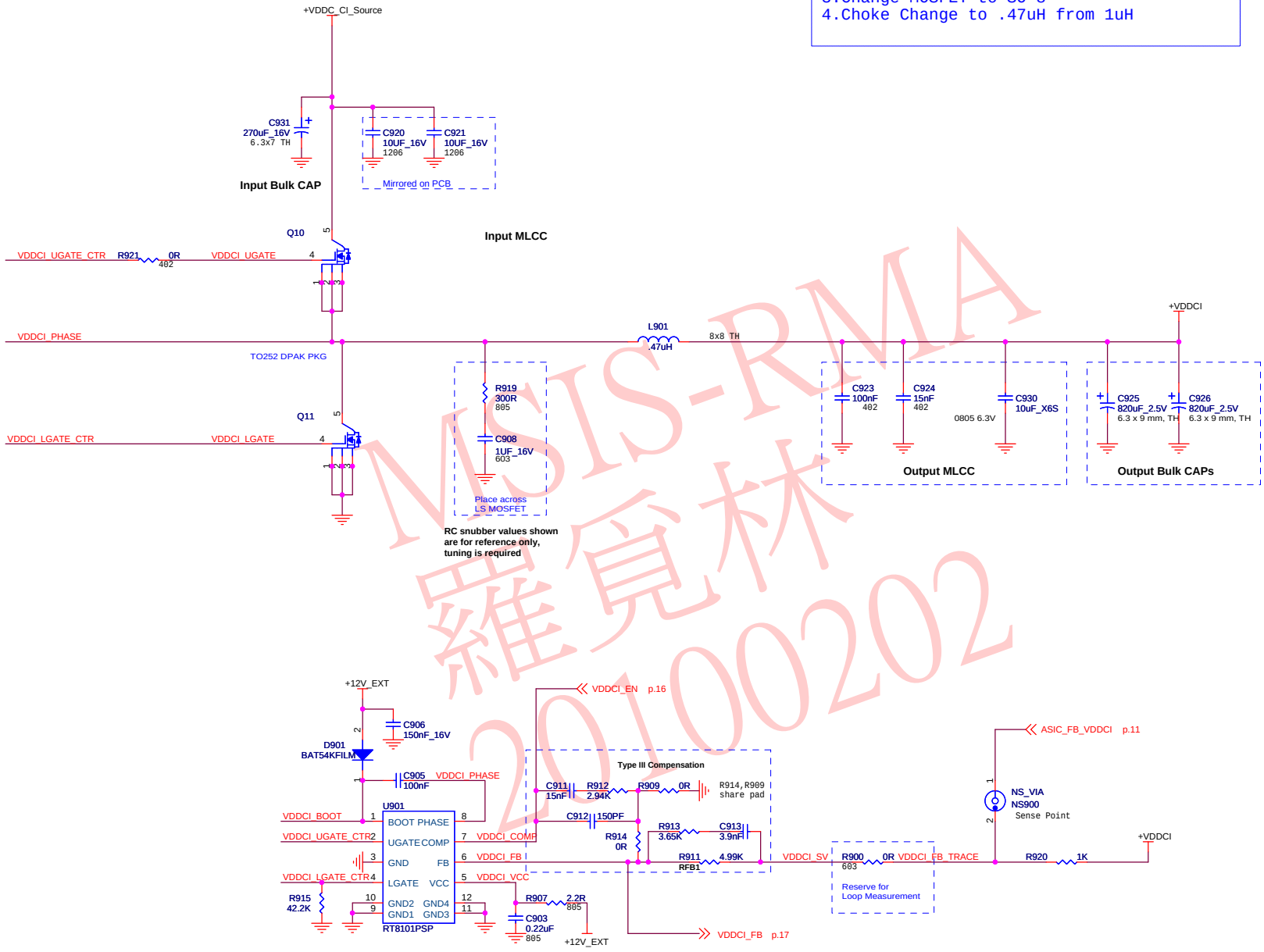
1.Remove Input MLCC C915,C916,C917,C919
2.Remove Output MLCC C923,C929
3.Change MOSFET to SO-8
4.Choke Change to .47uH from 1uH



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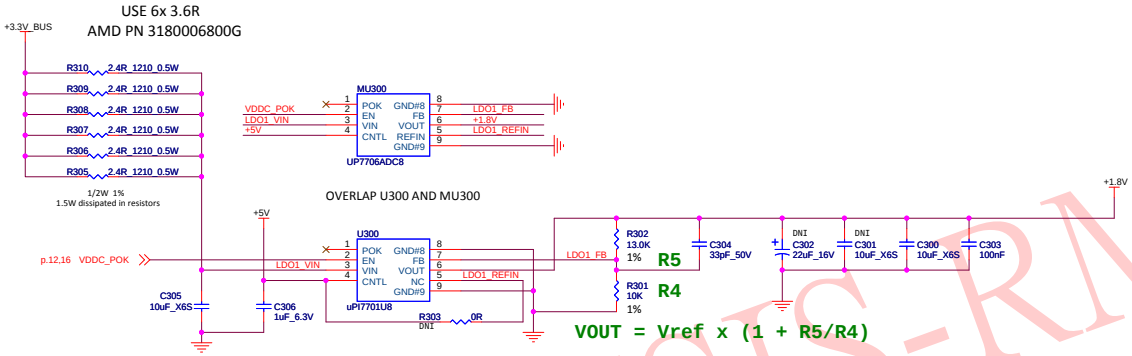
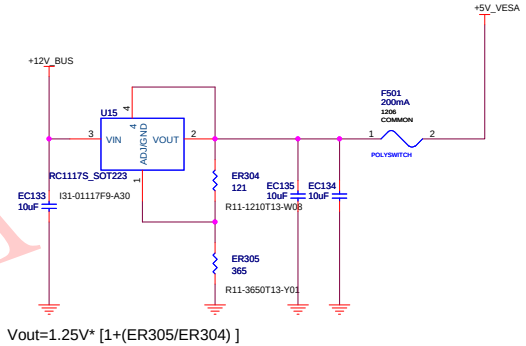
(15) Linear Regulators

Regulators for +5V, +5V_VESA and +5V_HDMI

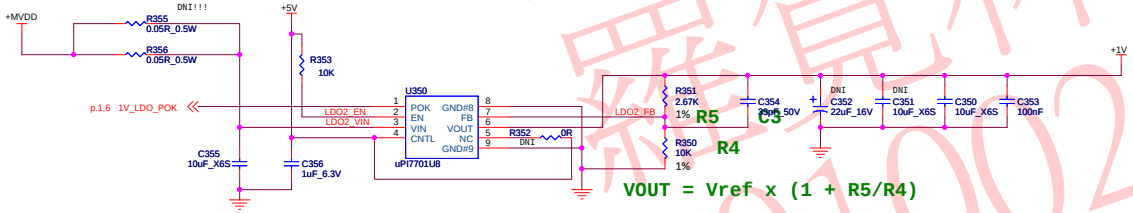
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling





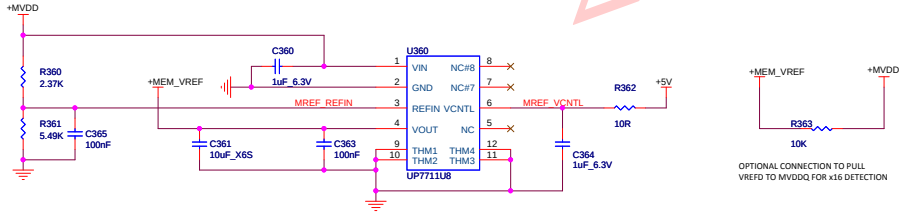
1.Change +5V REGULATOR to A1117

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



1.Removed BACKUP OPTION FOR +5V REGULATOR

Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ



There must be one 100nF at each VREF pin
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices

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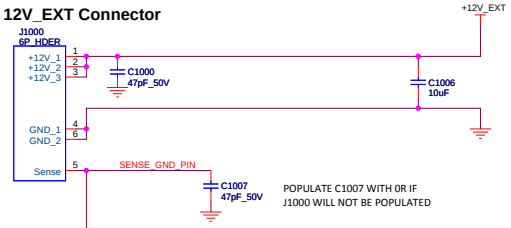
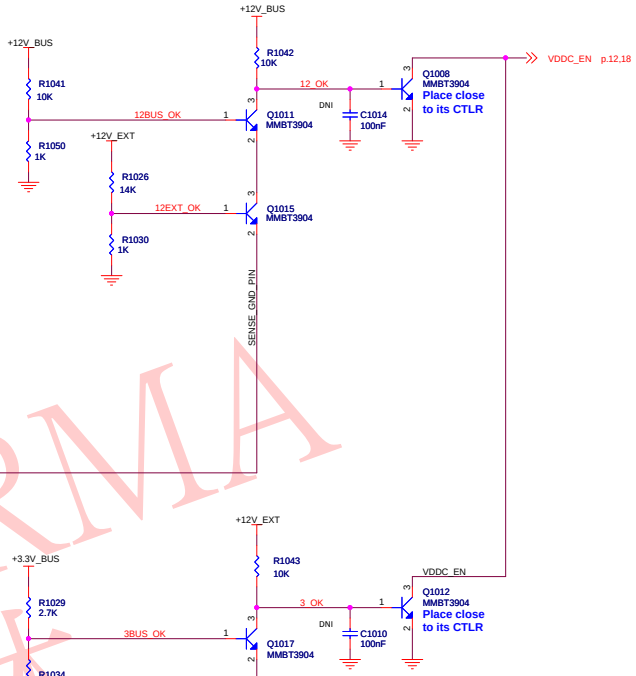
(16) Power Management - Power Gating and External Power Detect

12V_EXT Connector



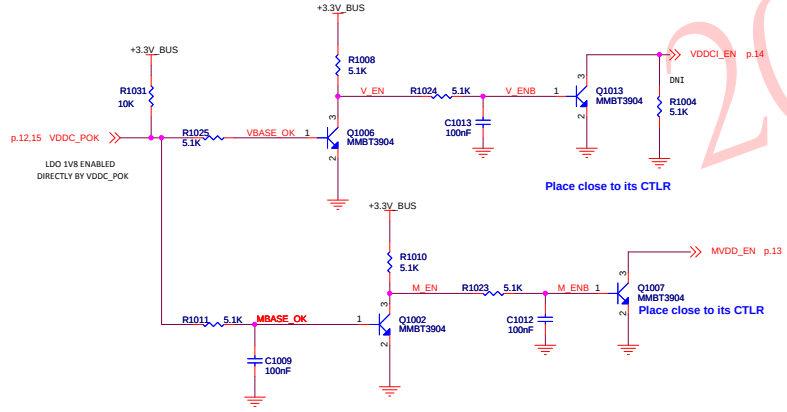
1.Remove option LED

12V_BUS, 12V_EXT & 3V3_BUS POWER SEQUENCING



POWER SEQUENCING CIRCUIT

FOR MVDD & VDDCI
(ENABLES CANNOT BE SHARED SINCE IT IS ALSO THE COMPENSATION PIN OF THE SMPS REGULATOR)



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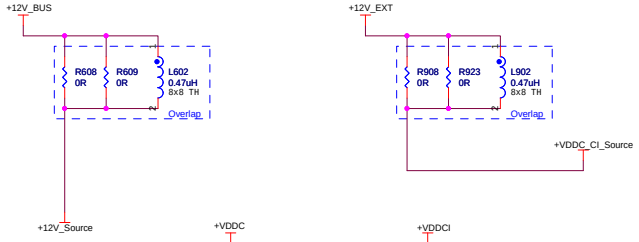
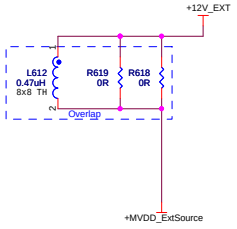
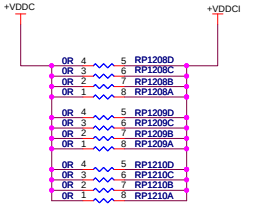
(18) Power Management 2

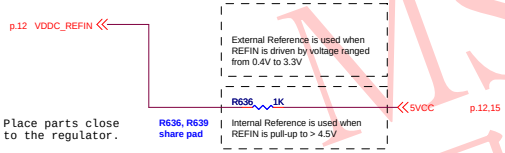






1.Removed I2C VOLTAGE REFERENCE FOR VDDC
2.Change input choke to .33uH from .47uH

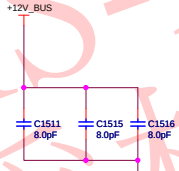
VDDC Reference Voltage Selection



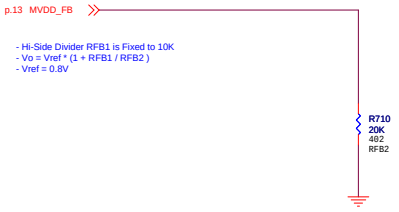
VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

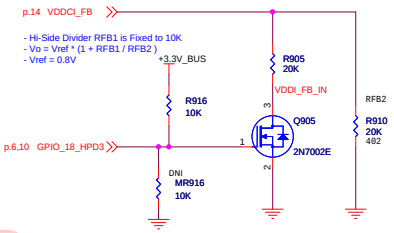
EMI Bypass Cap



MVDD Low Side Divider

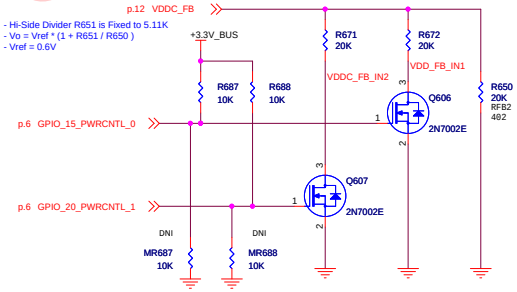


VDDCI Low Side Divider



VDDC Low Side Divider

R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V.
Then this will set VDDC to a fixed value.



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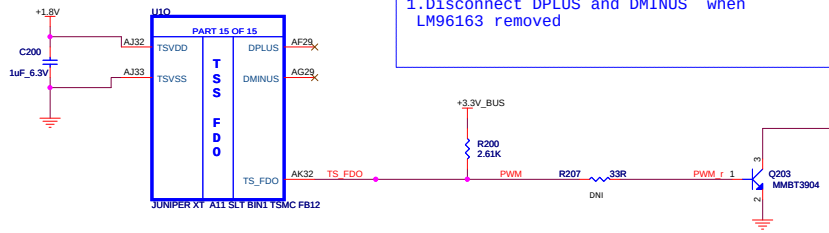
(19) Mechanical and Thermal Management

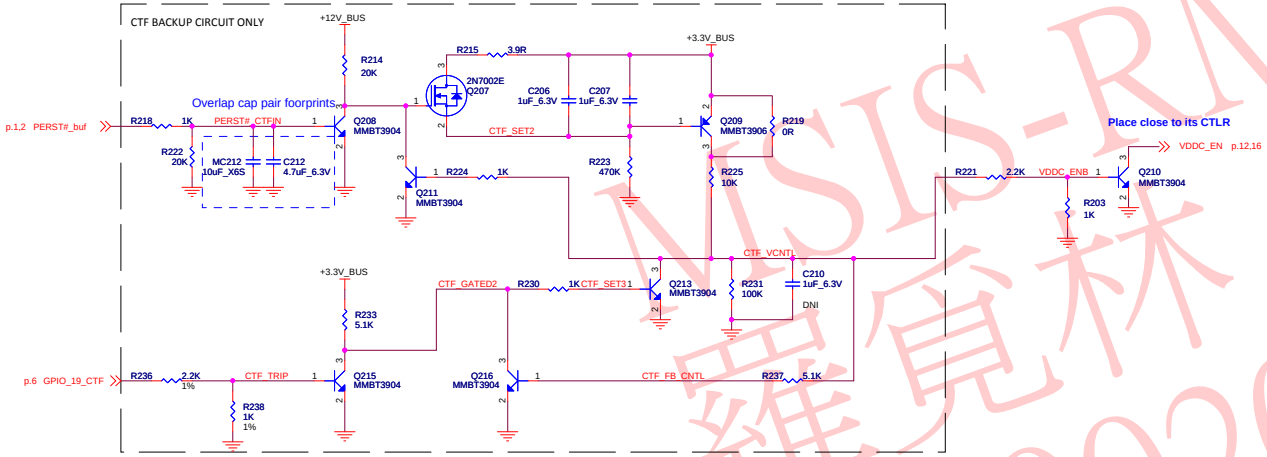
1.Disconnect DPLUS and DMINUS when LM96163 removed



Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board.
This is an open collector signal. Active level is hard pull down to ground.

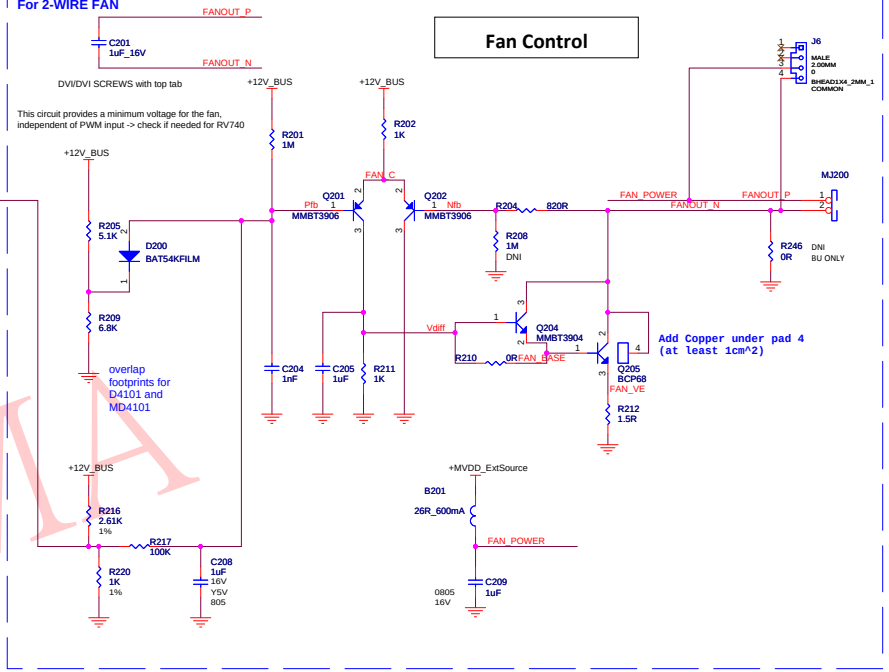
Critial Temperature Fault

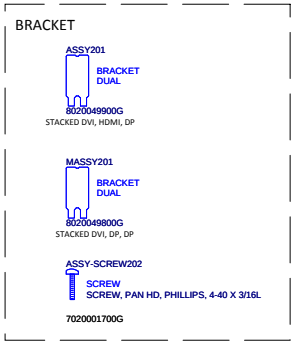


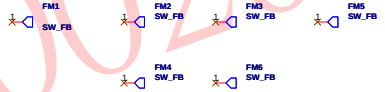
1.Remove CTF_VCNTRL
2.Remove TCRIT and GPIO_17_ThermINT when LM96163 removed

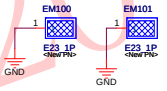
Fan Control

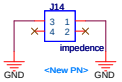
For 2-WIRE FAN



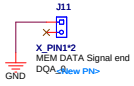




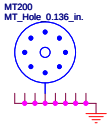




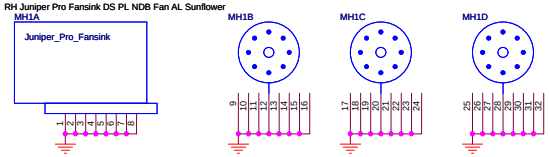
MEM :trace width=6mil,air gap=11mil / 80ohm



MEM to GPU : 5.1mil / 45ohm



RH Juniper Pro Fansink DS PL NDB Fan AL Sunflower



1.Remove VDDC Thermal Protection

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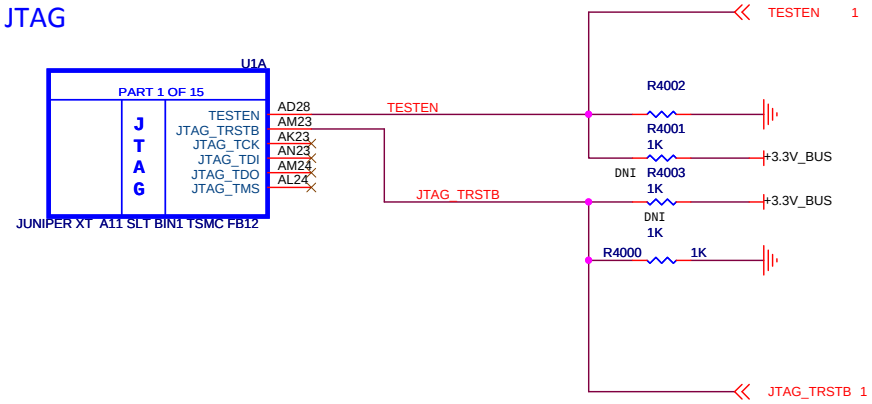
(19) Debug Circuits



1.Remove LED RED "ON" shows Fault circuit
2.Remove JTAG and re-connect to PCIe RESET Buffered
3.Remove SWITCH CONNECTIONS TO PINSTRAPS
4.Remove LM96163

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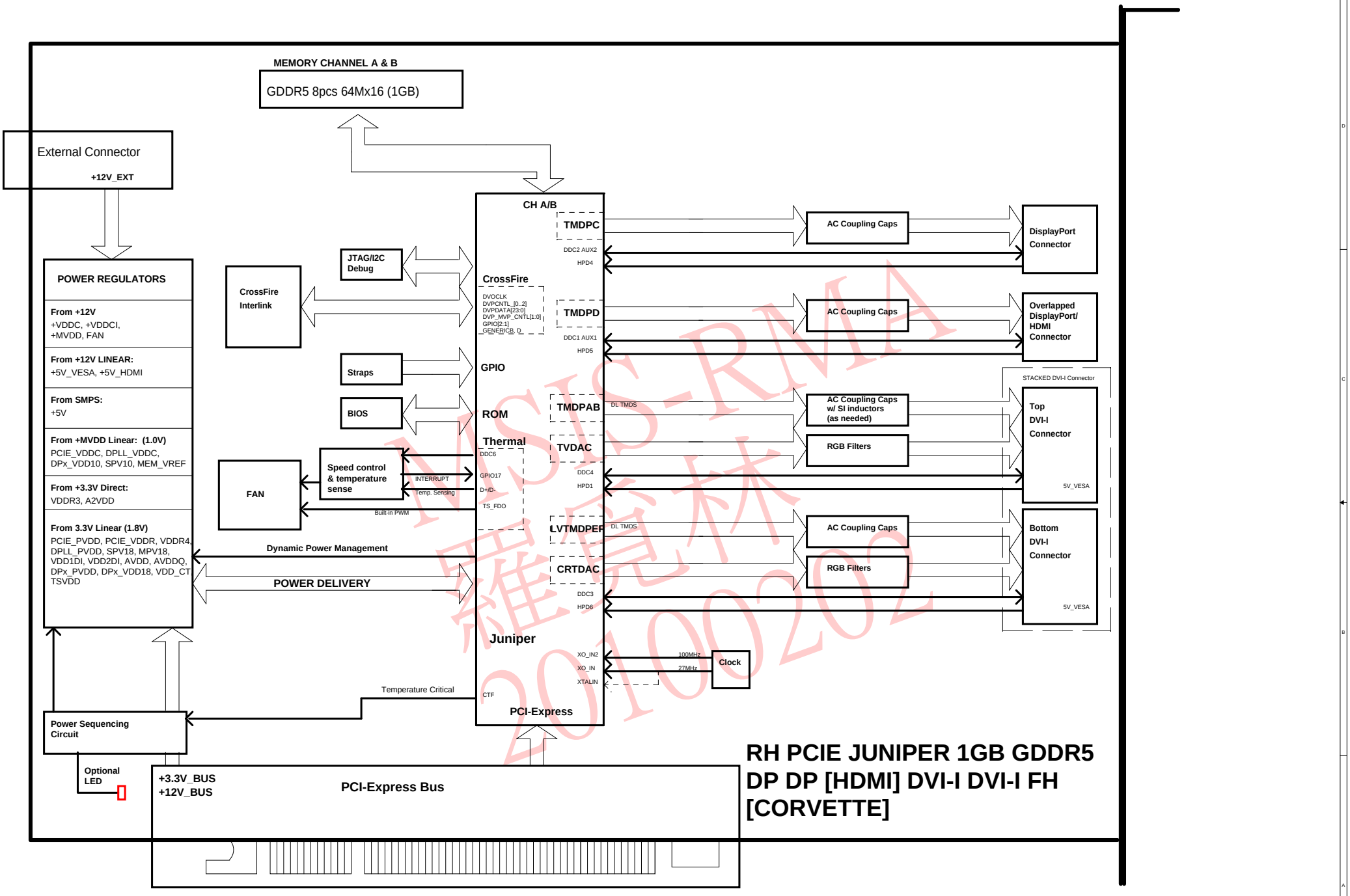

RH PCIE JUNIPER 1GB GDDR5 DP DP [HDMI] DVI-I DVI-I FH [CORVETTE]

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Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

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Title	Schematic No.	Date:
RH JUNIPER LE GDDR5 1GB DP+DP/HDMI+2xDVI	105-C012xx-00B	Wednesday, December 09, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 01

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/03/23	JUNIPER LE GDDR5 1GB - BASED ON C010 REV43;
01	00B	2009/07/13	p. 16 - ADD R1010-1, Q1002: MVDD WAS NOT DELAYED ENOUGH WRT VDDCI, ADD EXTRA TRANSISTOR CONNECTION TO CHANGE DELAY; p. 18 - REMOVE R247, R245, CHANGE NET NAME FROM CTF_BYPASS TO CTF_VCNTRL, CHANGE SW4003 CONNECTION TO PRODUCTION-READY CONFIG; p. 6 - ADD 2ND OSCILLATOR CLOCK SOLUTION TO MITIGATE ANY POSSIBLE CONCERNS SHARING GENERICA WITH XO_IN2, AND ALSO TO ALLOW FOR DIFFERENT SPREAD-SPECTRUM SETTINGS FOR DISPLAY AND MEMC TO MITIGATE ANY POSSIBLE EMI PROBLEMS; p.15 - REMOVE R300, R357: 0R WERE THERE FOR BU AND PRE-PRODUCTION DEVELOPMENT, REMOVE FOR PRODUCTION; p. 17 - ADD R687-8, MR687-8, R916, MR916: ADD OPTION OF PU/PD, SO DEFAULT VDDC/VDDCI ON POWER-UP CAN BE CONTROLLED IN BOM; P.8/10 - UPDATE TO DVI FOOTPRINT THAT ALLOWS FOR SINGLE-DVI OVERLAP; p. 15 - ADD R363 - OPTIONAL CONNECTION TO PULL VREFD TO MVDDQ FOR x16 DETECTION BY MEM DEVICES (CERTAIN MEM DEVICES HAVE A BUG THAT CANNOT DETECT x16/x32 WITHOUT PU/PD ON VREFD); p. 17 - ADD R1072-3, R1075-6: THESE ARE FOOTPRINTS TO BE USE FOR FERRITE BEADS IF EMI IS FAILING;

2009/09/16

p.4 1.Change to 32Mx32bit ,remove U2100,U2200
p.5 1.Change to 32Mx32bit ,remove U2500,U2600
p.6 1.Remove crossfire
2.Disconnect DDC6,GPIO 6,17 when M96163 removed

p.9 1.Remove Port D Display port
p.15 1.Change regulator for +5V
p.16 1.Remove option LED

p.17 1.Remove I2C VOLTAGE REFERENCE FOR VDDC

p.18 1.Remove CTF_VCNTRL
2.Remove TCRIT and GPIO_17_ThermINT when LM96163 removed
p.19 1.Remove LED RED "ON" shows Fault circuit
2.Remove JTAG
3.Remove SWITCH CONNECTIONS TO PINSTRAPS
4.Remove LM96163

2009/09/17

p.4 1.Add VREFD circuit
p.5 1.Add VREFD circuir
p.6 1.Remove 1.8V_LDO_POK,1V_LDO_POK to Powergood
2.SCL,SDA connect to UP6262
p.7,8,9,10 1.Remove ESD PROTECTION DIODES
p.8,9,10 1.Add EMI bridge
p.11 1.Remove 1uFx18,47uFx2 ;Add POSCAP
p.12 1.Add UP6262
p.13 Remove Q703 L-Side MOSFET
p.15 1.Remove MVREF LDO
p.18 1.Remove VDDC Thermal Protection

2009/09/18

p.2 1. Add PCIe RESET Buffered Circuit U101,MU101
p.6 1. Add CLOCK GENERATOR UC1008 colayout with U12

2009/09/29

p.6 1.Disconnect HPD1 when DVI TOP removed
2.Disconnect GENERICE_HPD4 when Displayport removed
3.Disconnect GENERICA when Displayport removed
p.7 1. Add D-Sub connector, DDC change to DDC1 from DDC4
p.8 1. Remove DVI TOP
2. DDC1 connect to DAC2
3. ADD HDMI and DDC connect to DDC4
p.9 1. Removed Displayport
2. Removed HDMI
p.6 1.Removed U2,Y2 reference clock circuit