P654 - GT200/NVIO2

P654, GT200-100, 896MB/1792MB - GDDR3 BGA136 16M/32Mx32

DVI-I + DVI-I/DP + HD/SD/TVout, SPDIF, Dual SLI

Table of Contents

sku	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10654-BASE-A03	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10654-0000-000	DT, GT200-100, 550/1350/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I + HDTV
2	SKU0001	600-10654-0001-000	DT, GT200-100, 550/1350/1000, 896MB - 16Mx32 GDDR3, DVI-I + DP + HDTV
3	SKU0051	600-10654-0051-300	DT, GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
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MS-V180 -0A
- PAGE 21:VGS SLIM
- PAGE-22 remove DACB HDTV Circuit
- PAGE 24:DVI change HDMI
- PAGE 25:DP modify DSDA/DSCL circuit
- PAGE 28:ADD I2C0_SCL/SDA and GPIO 3 circuit,remove GPIO 12
- PAGE 29:remove R112,R113 and GPIO8_FAN_TACH link to U21
- PAGE 33:remove R671,R572
- PAGE 35:remove RT8805CQVA change UPI6205 and UPI6262 circuit
- PAGE 36:remove NCP5388MNR2G change UPI6208 circuit
- PAGE 37/38 :remove NCP3418B change UPI6281 circuit
- PAGE 39 :Add WL83L786G circuit

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Title Page

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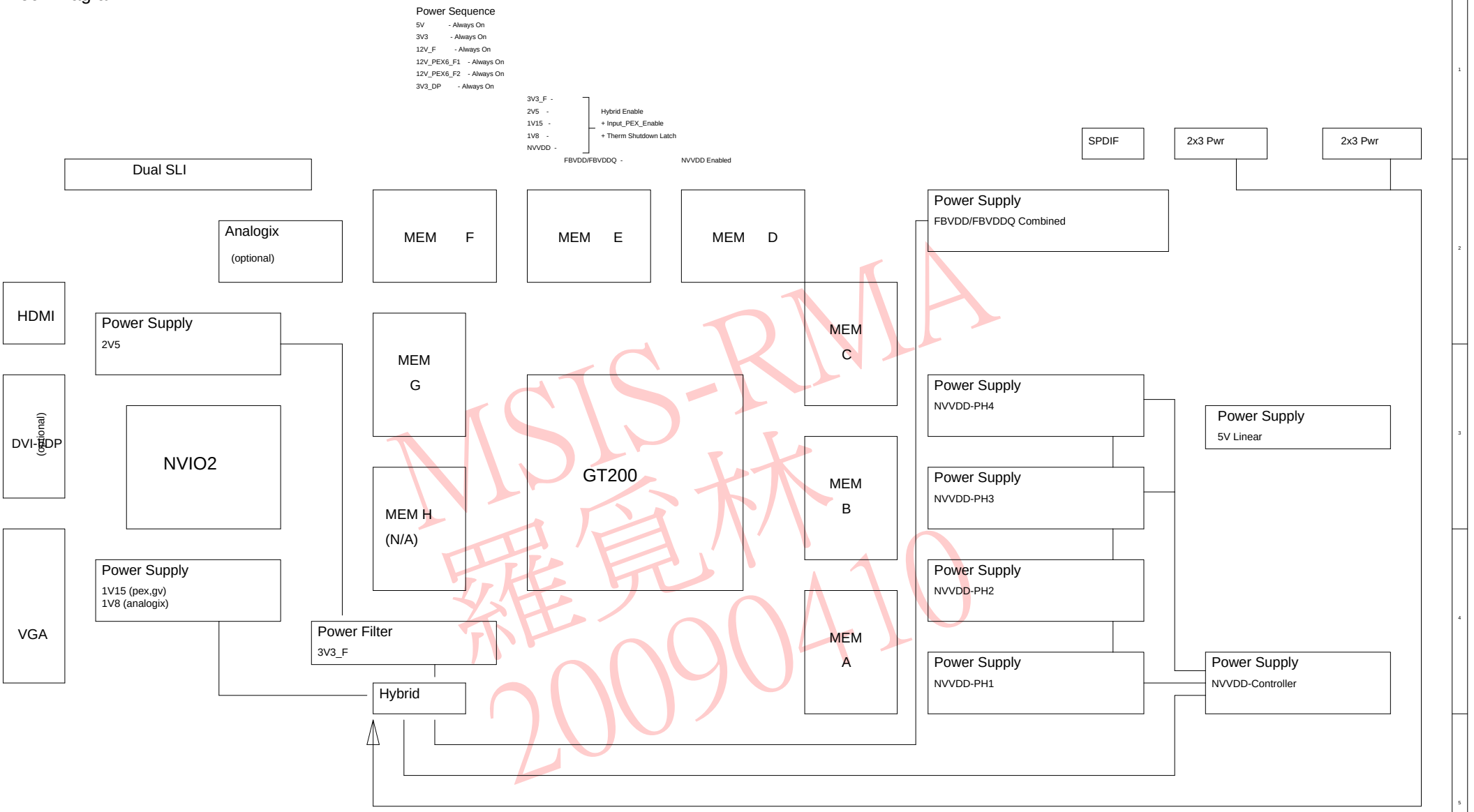
Block Diagram



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PAGE DETAIL	Block Diagram

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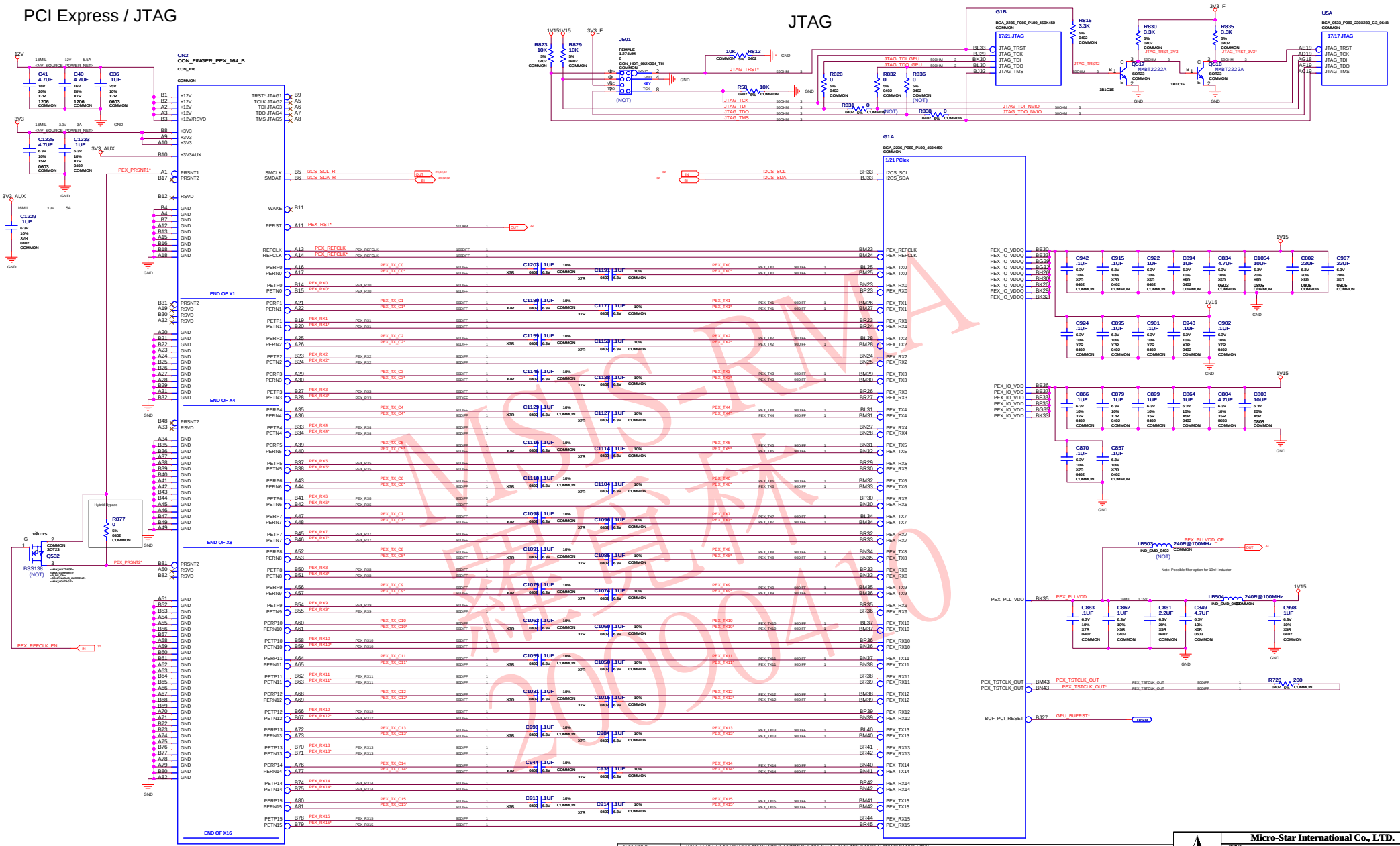
PCI Express / JTAG



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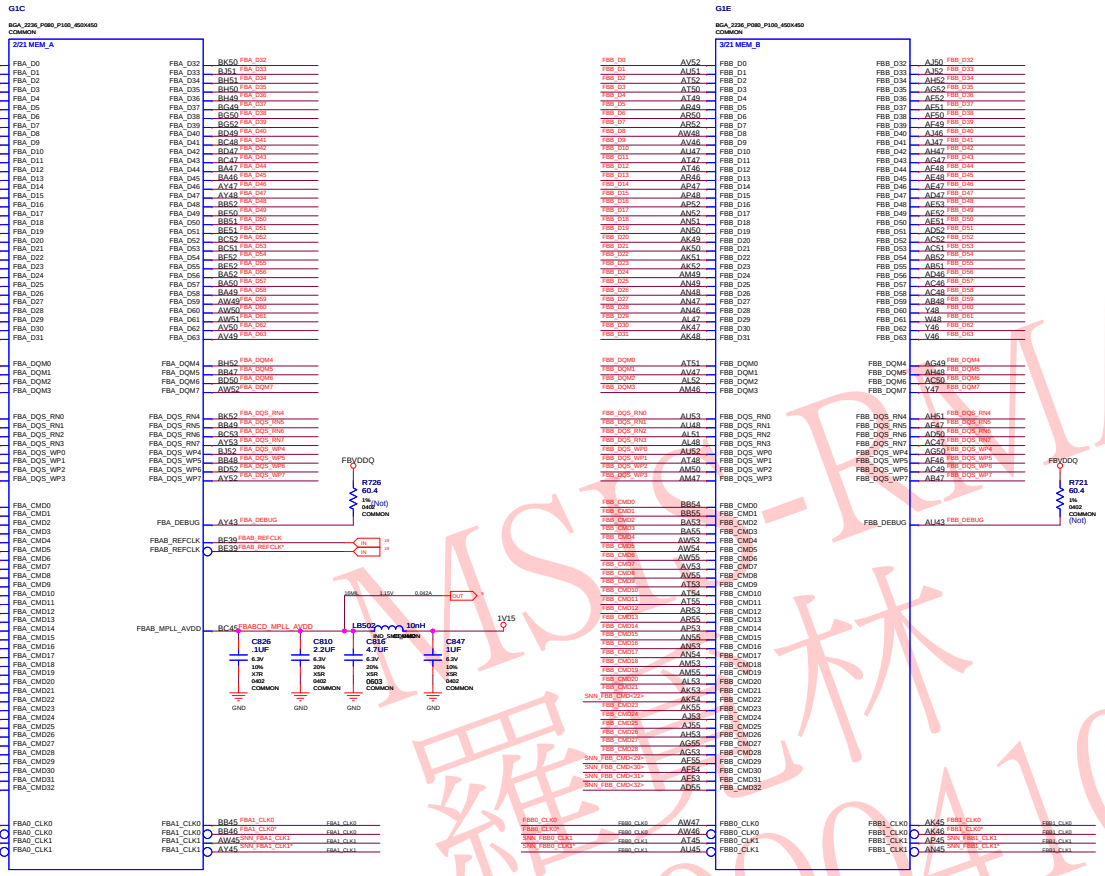
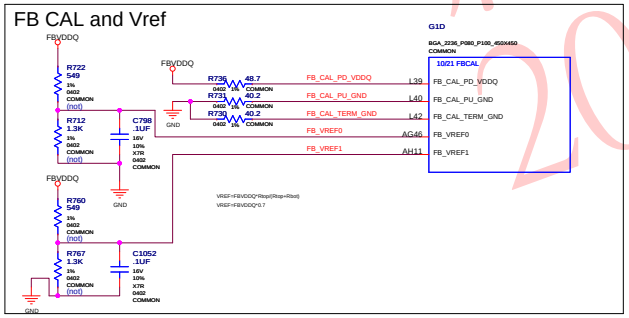
Framebuffer A,B: GPU Section + Calibration





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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Framebuffer A,B: GPU Section + Calibration

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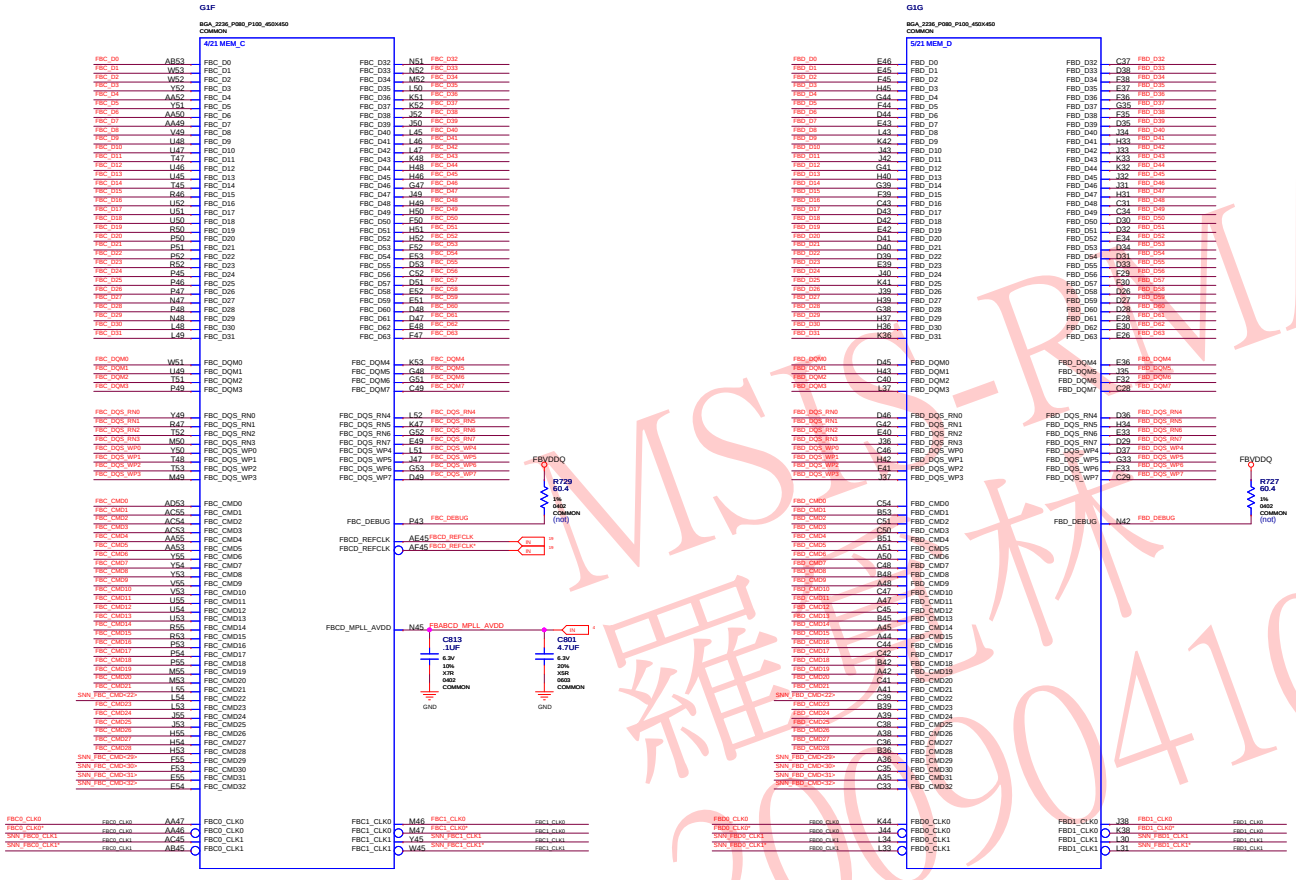
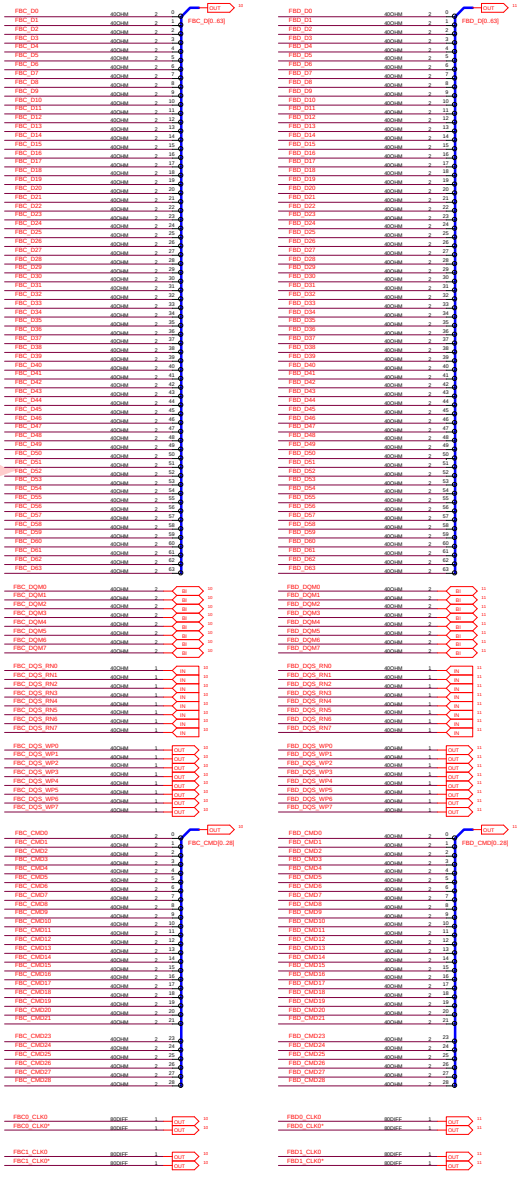
Framebuffer C,D: GPU Section





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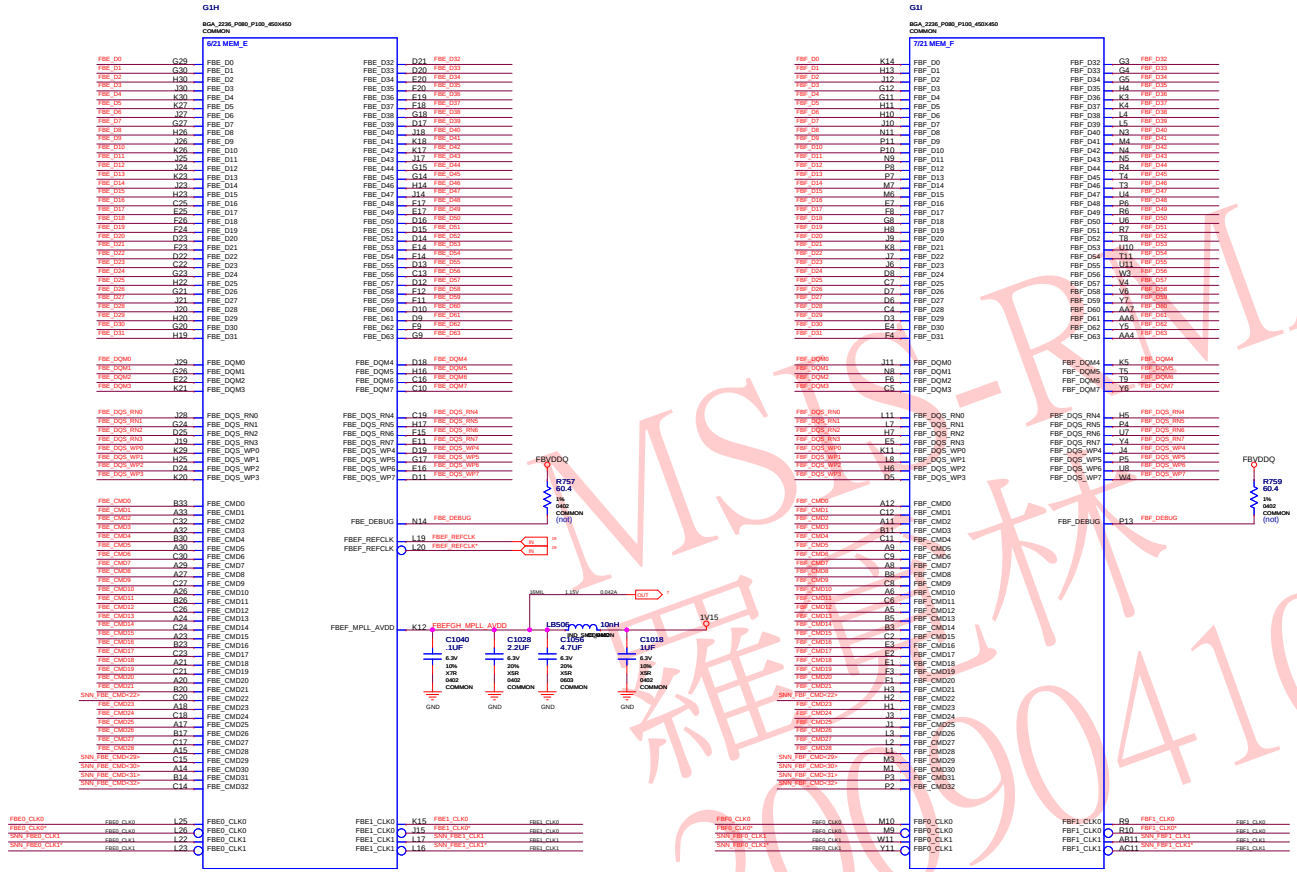
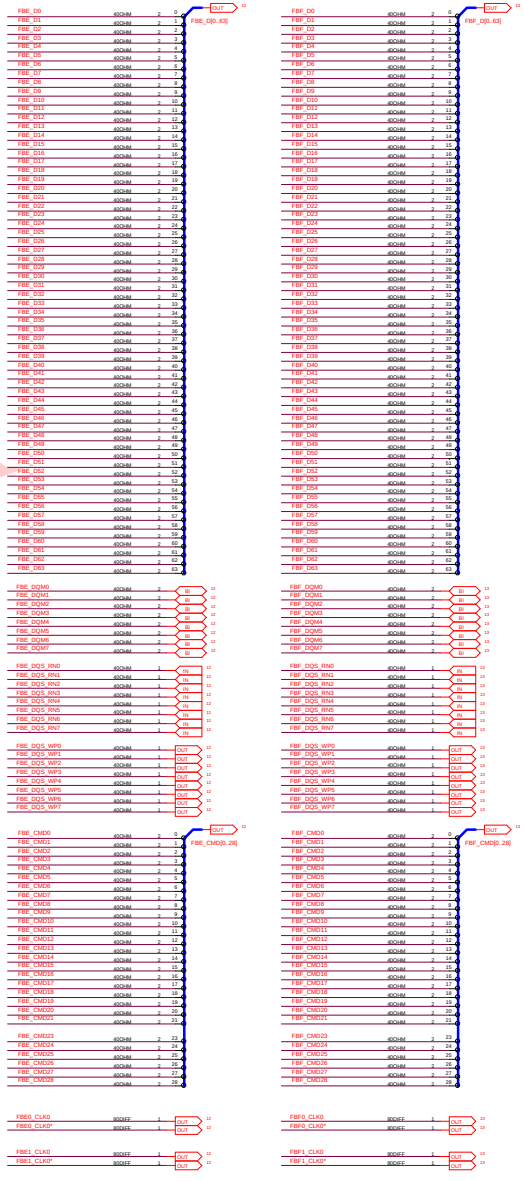
Framebuffer E,F: GPU Section





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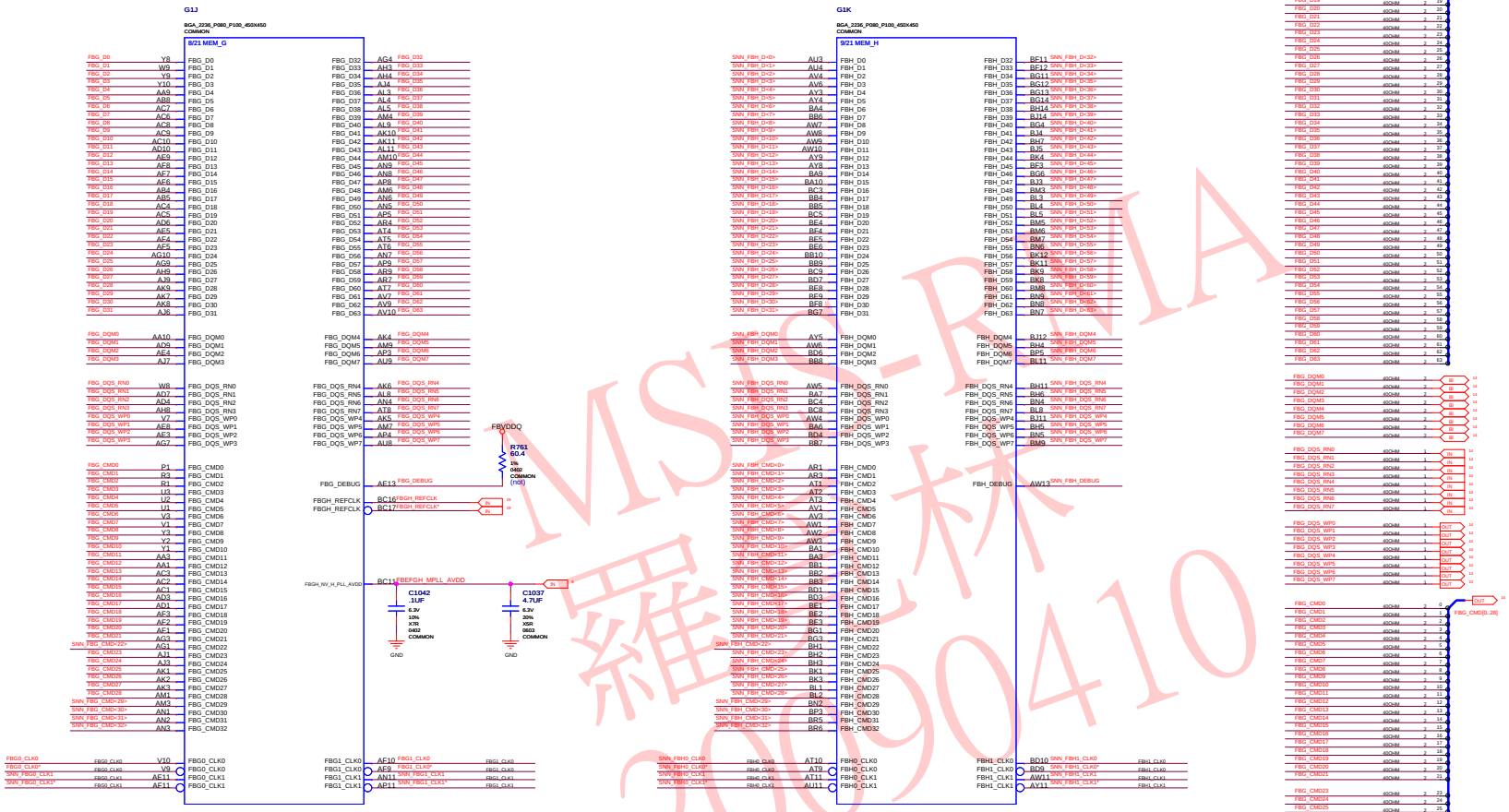

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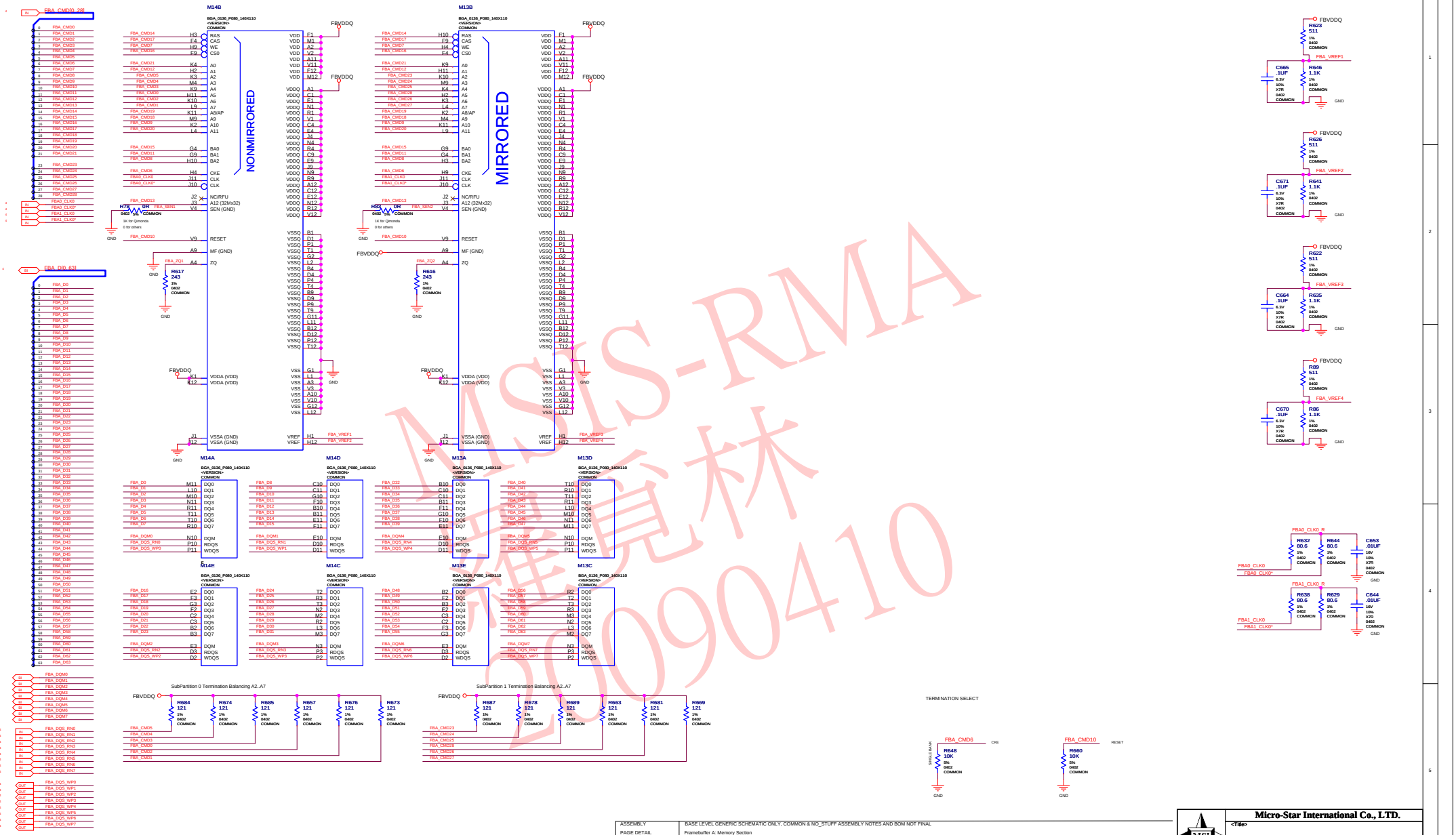
Framebuffer A: Memory Section



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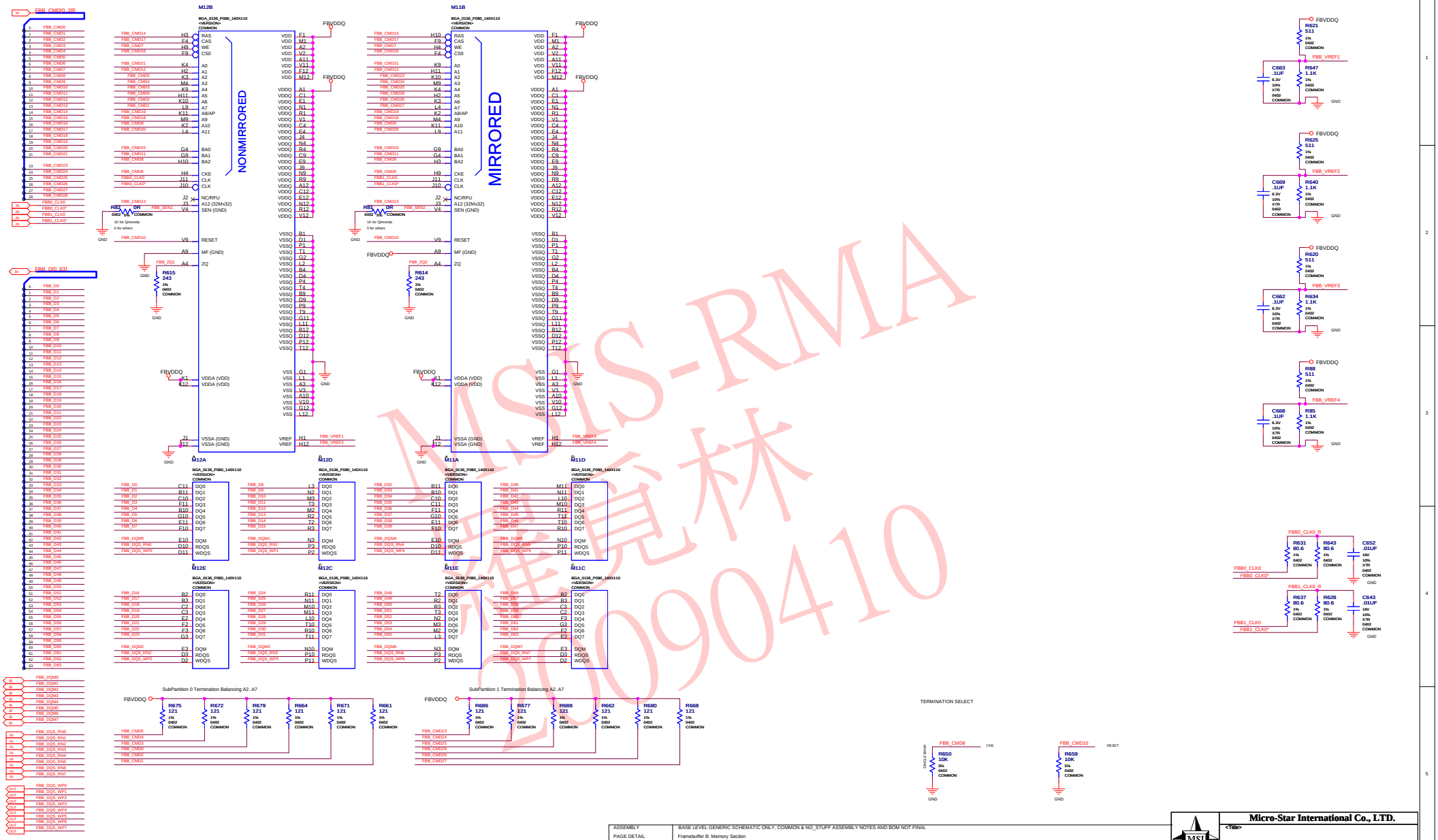

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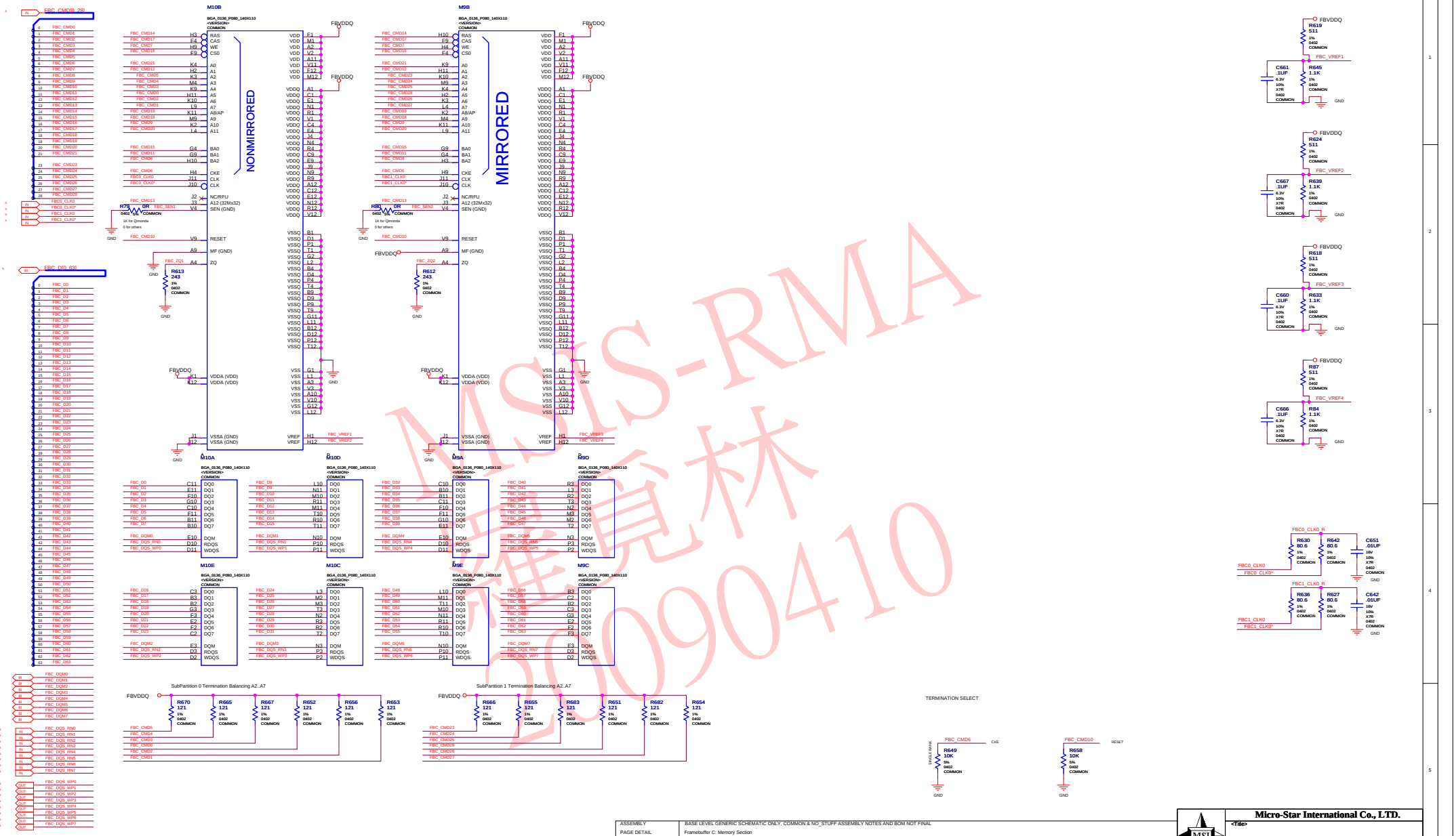

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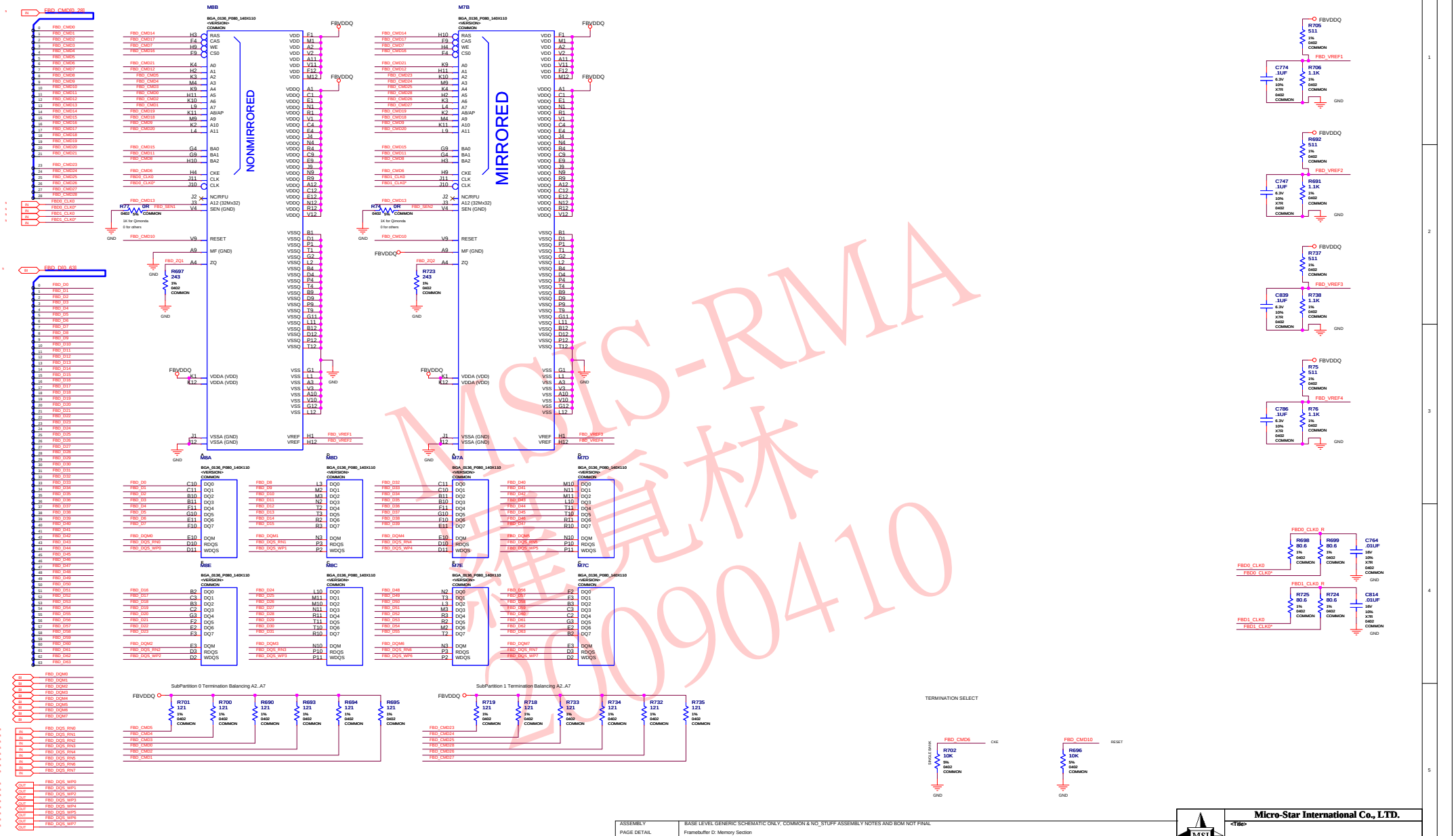

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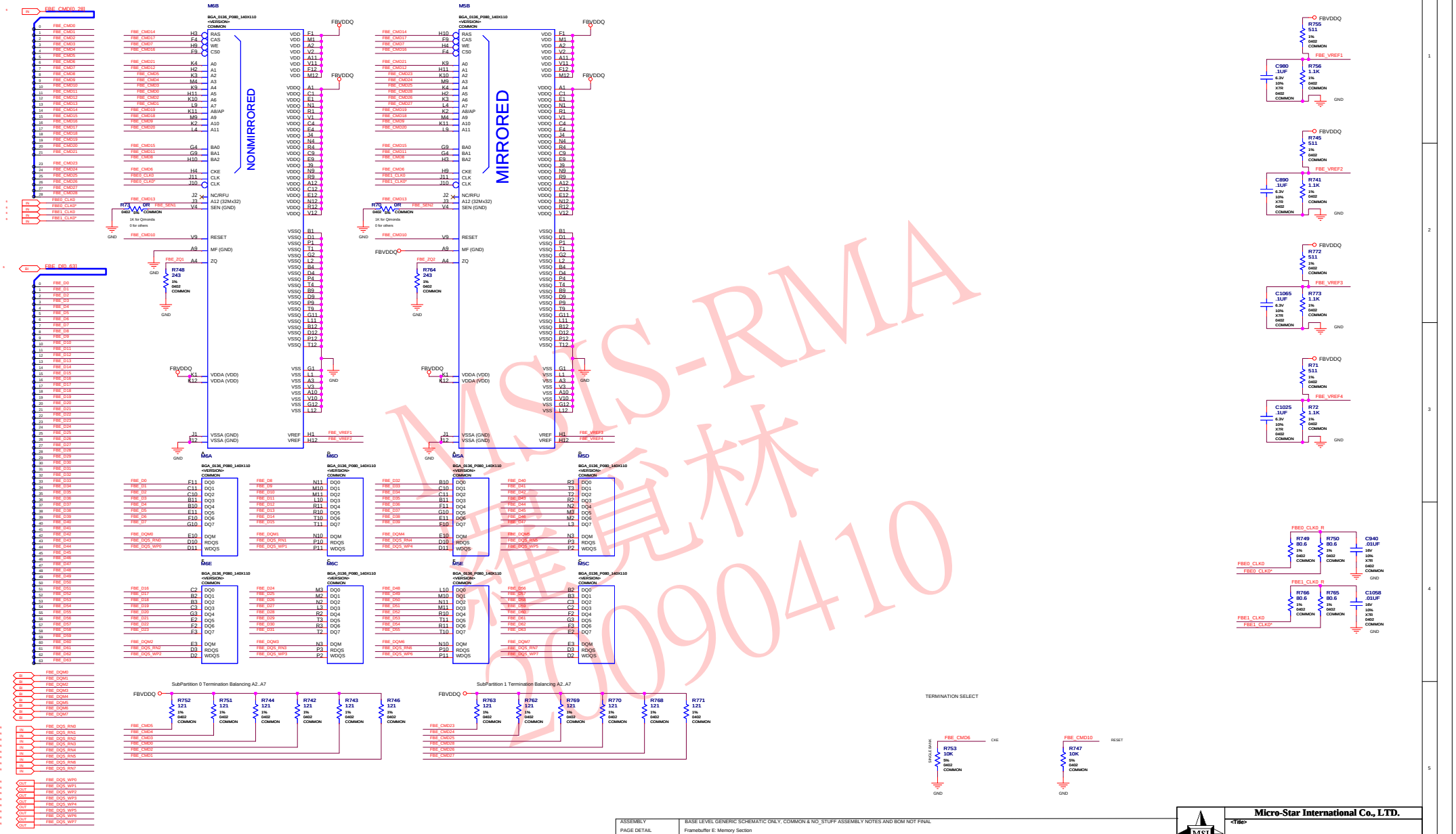

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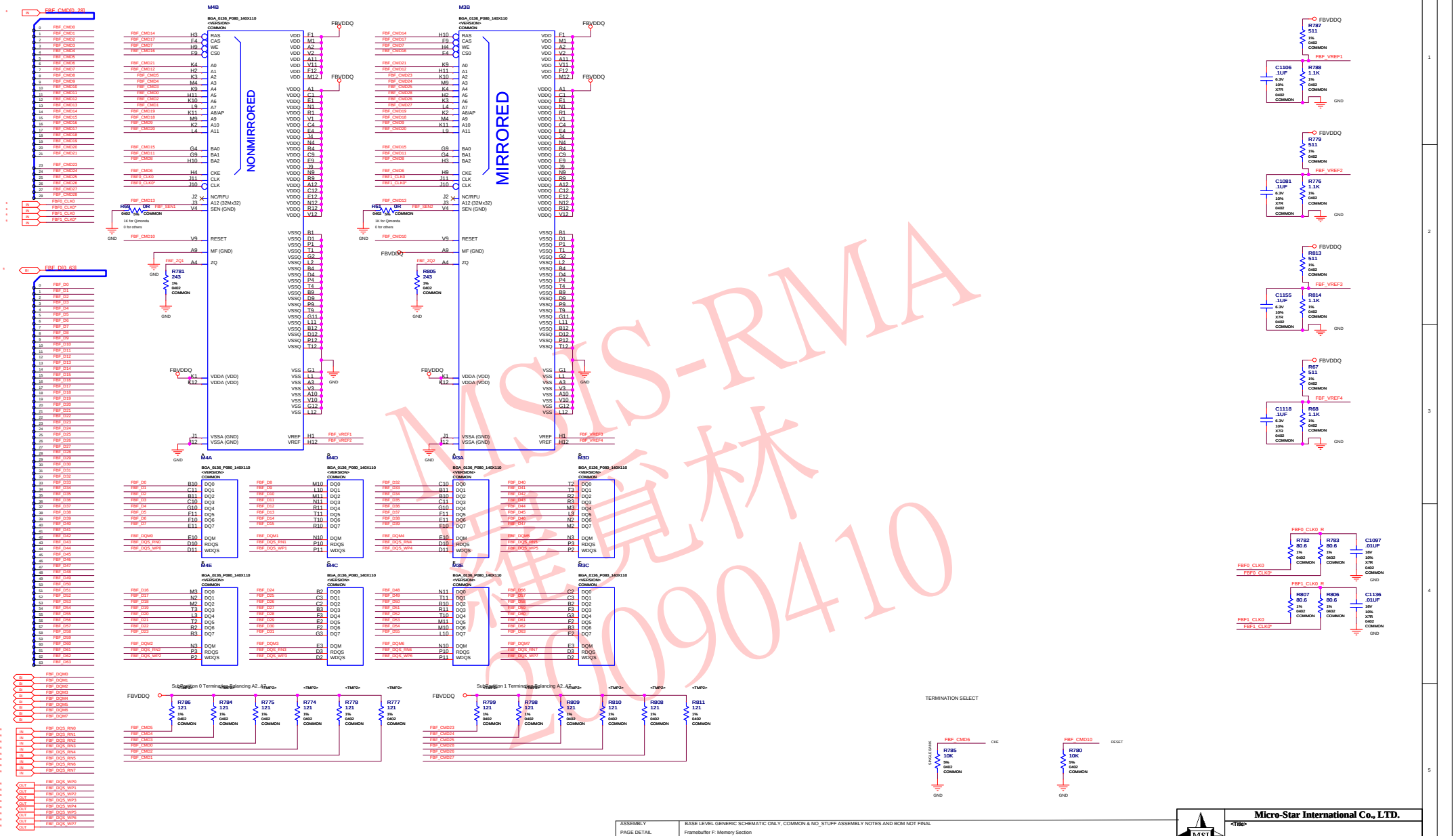

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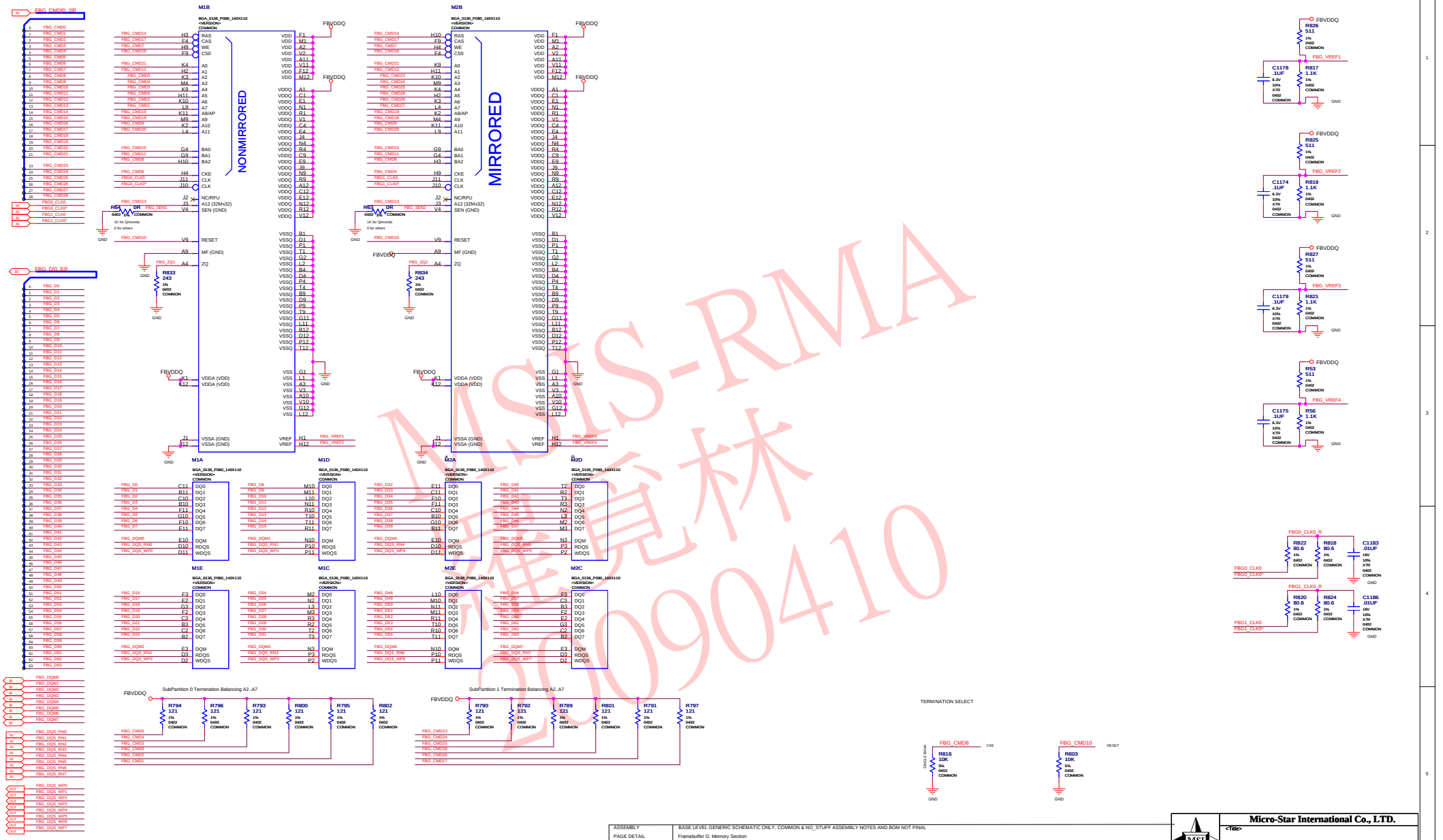

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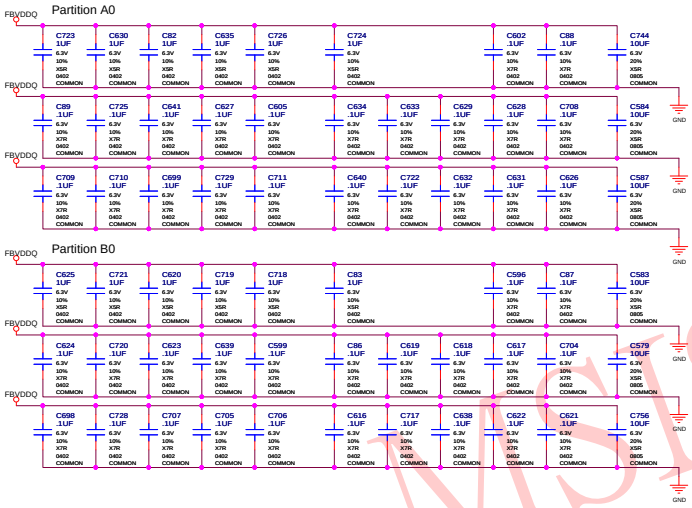
Decoupling: Memory Section A-D

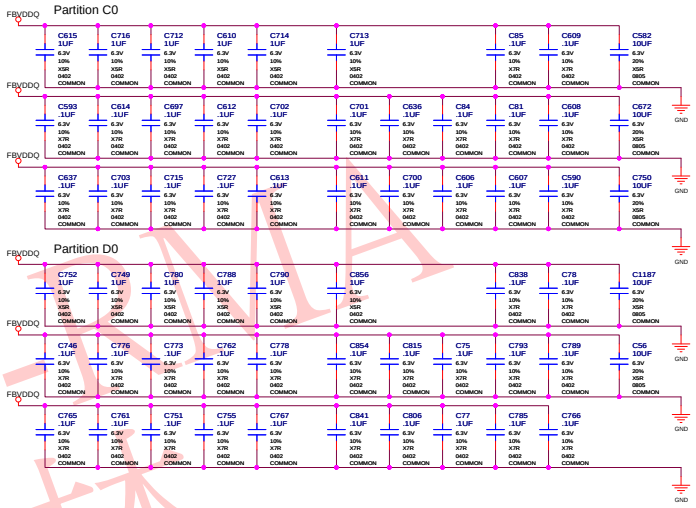
Banks A-D FBVDD/Q

Combined Distributed Capacitance

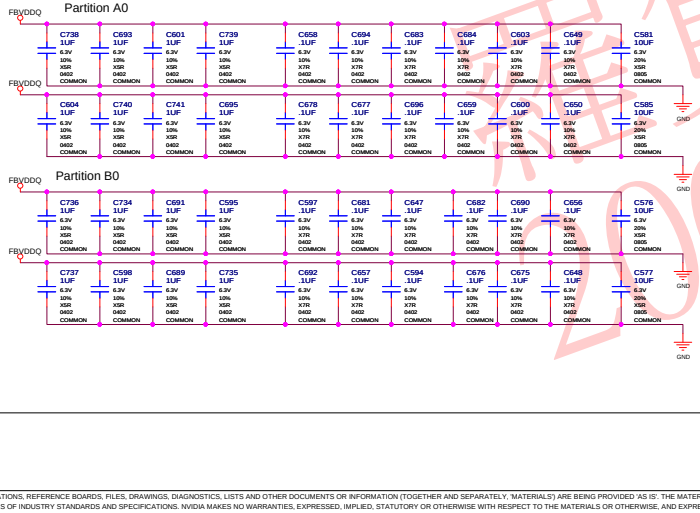
280 uF

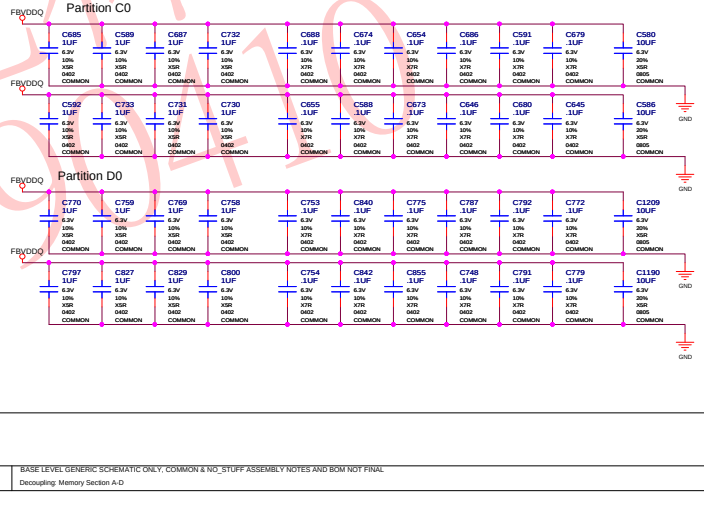
Decoupling for FBVDDQ





Decoupling for FBVDDQ





MSI 微星 2009年2月10

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Decoupling: Memory Section A-D

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<Title>		
Size: Custom	Document Number: <Doc>	Rev: <FevCode>
Date: Wednesday, February 11, 2009	Sheet 16 of 41	

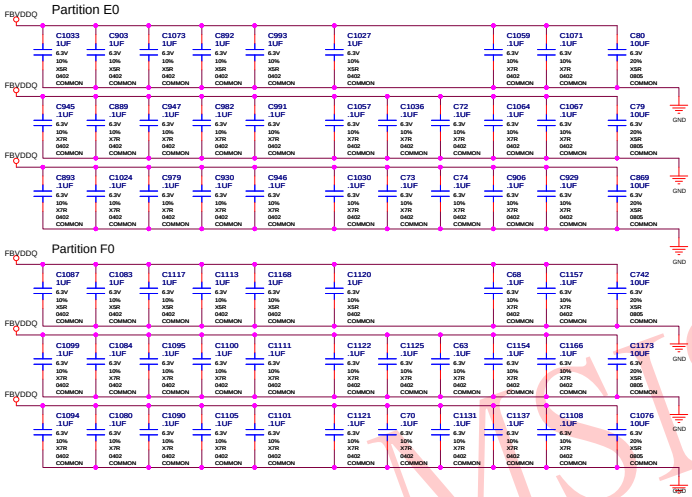
Decoupling: Memory Section E-G

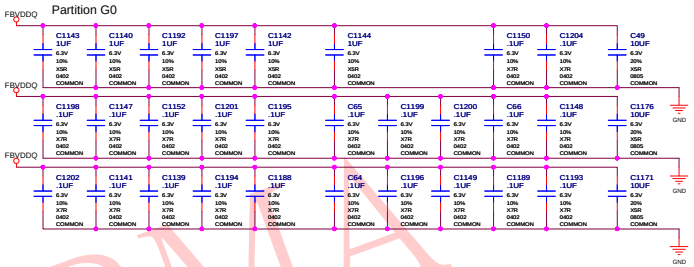
Banks E-G FBVDD/Q

Combined Distributed Capacitance

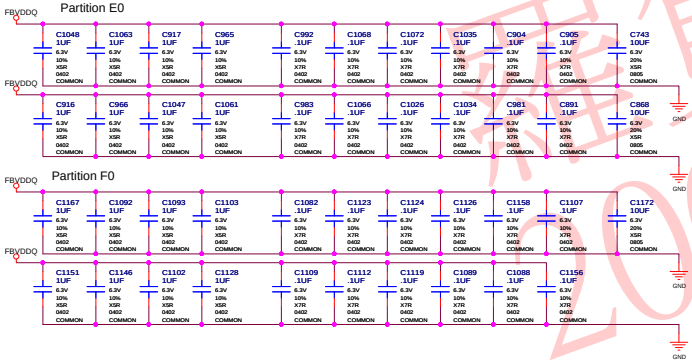
210 uF

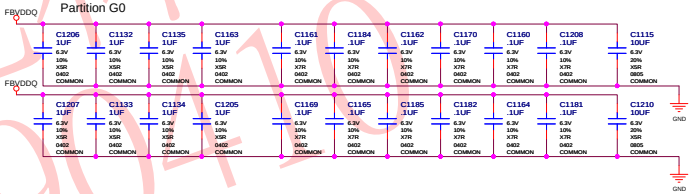
Decoupling for FBVDDQ





Decoupling for FBVDDQ





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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Decoupling: Memory Section E-G

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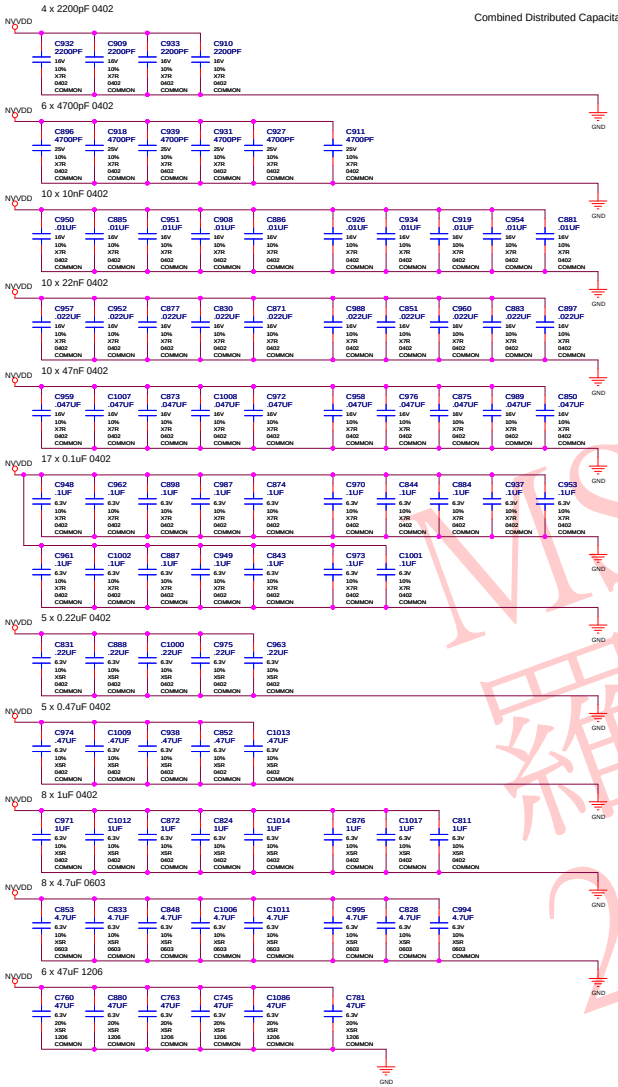
Decoupling: GPU (NVVDD, FBVDDQ)

Decoupling for NVVDD (under GPU)

GPU - NVVDD

Combined Distributed Capacitance

494 uF

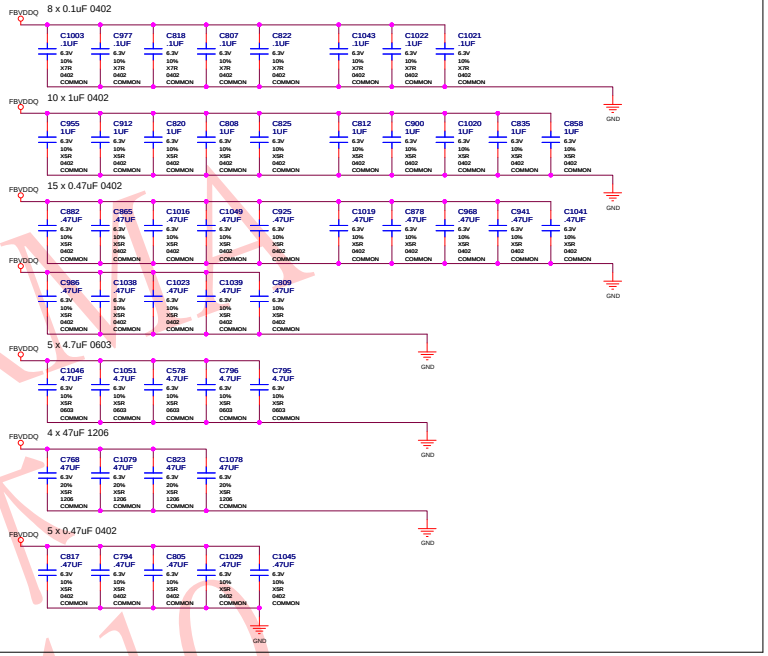


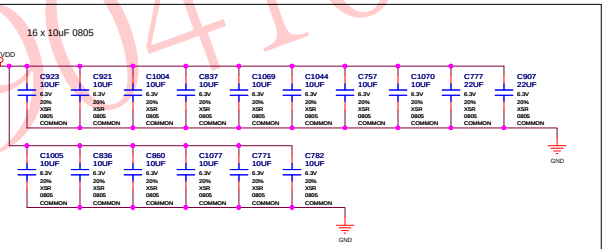
Decoupling for FBVDDQ (under GPU)

GPU - FBVDD/Q

Combined Distributed Capacitance

230 uF





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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Decoupling: GPU (NVVDD, FBVDDQ)

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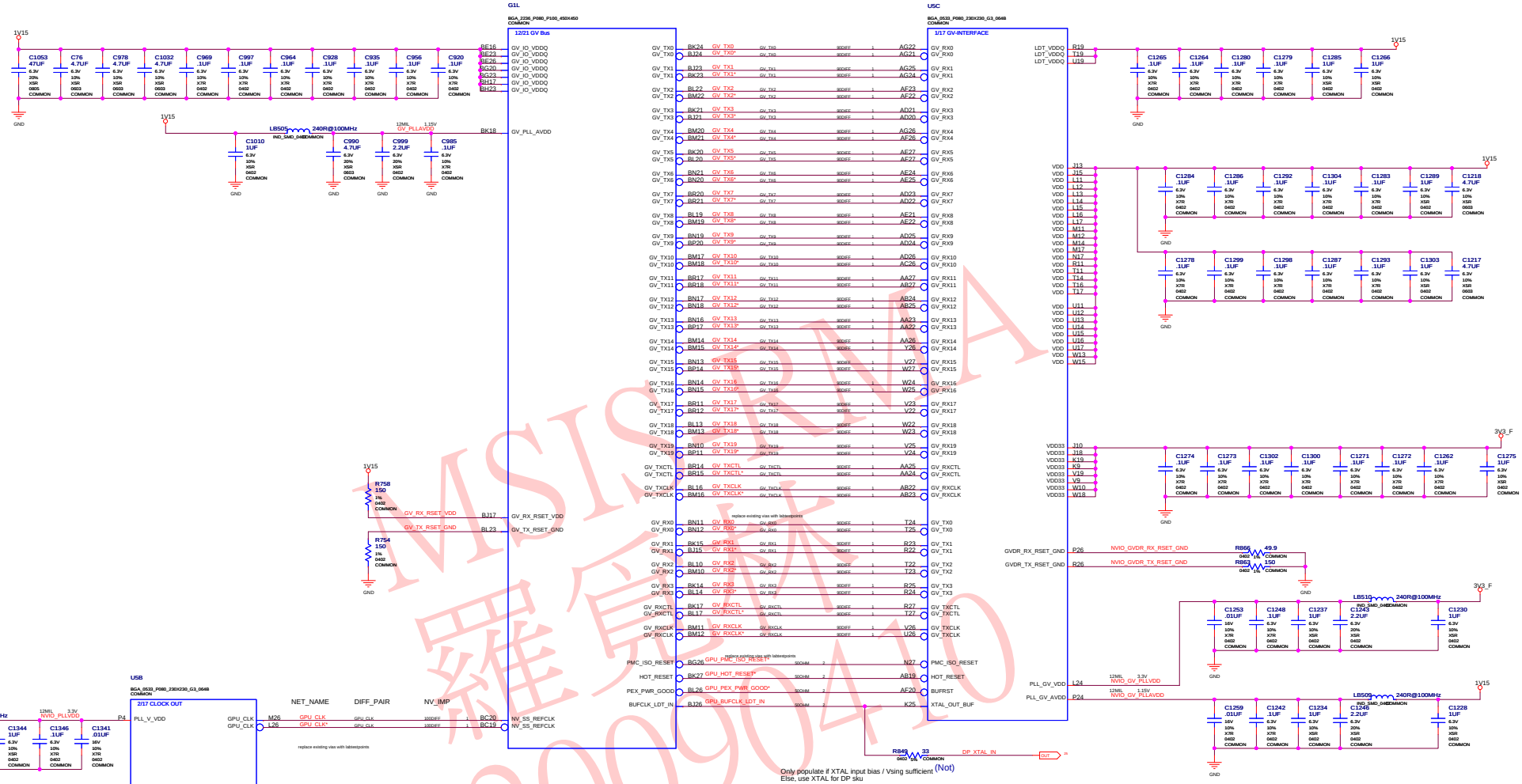
GPU-NVIO Interconnect: GV Bus / PLL



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	GPU-NVIO Interconnect: GV Bus / PLL

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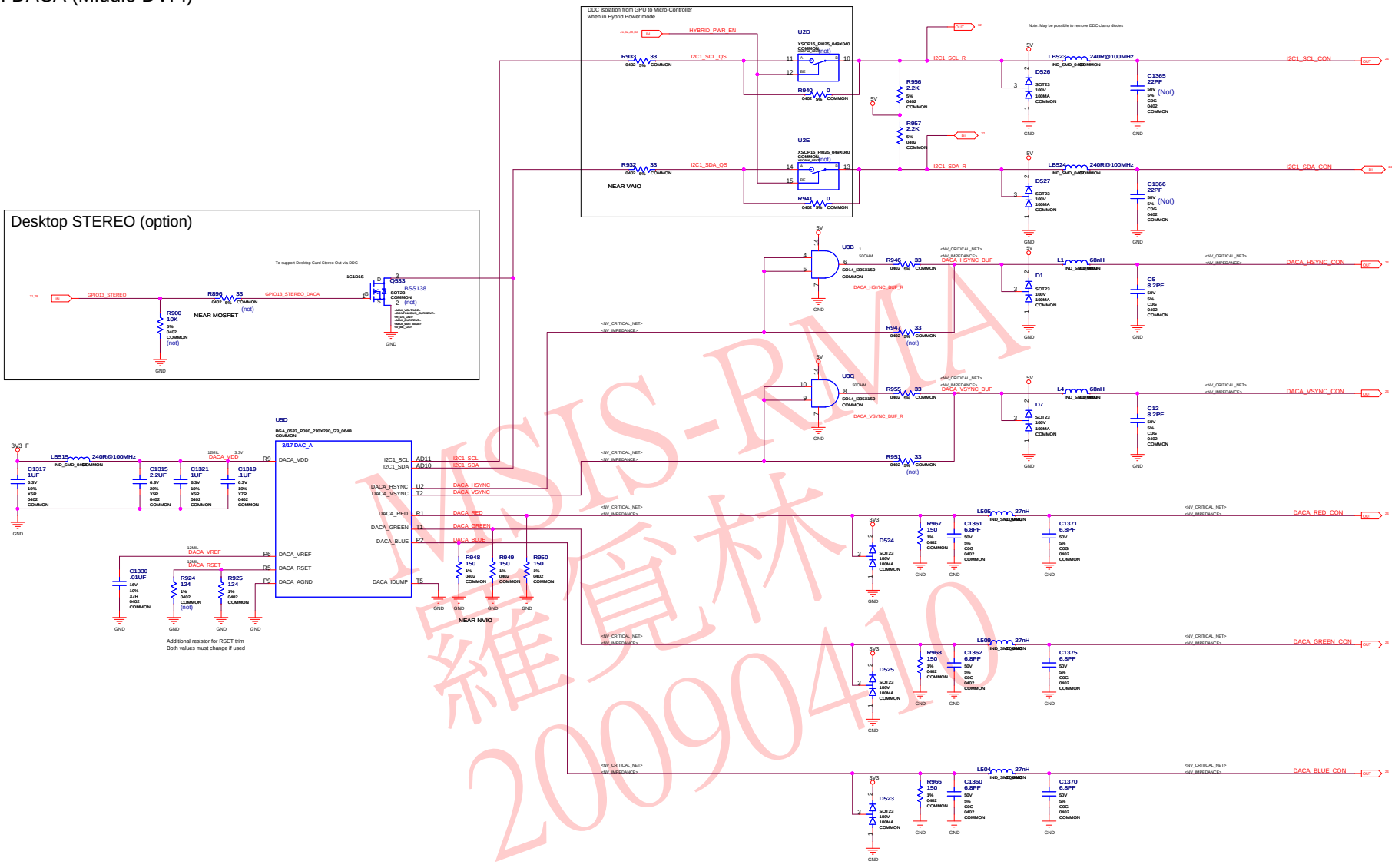
Date: Wednesday, February 11, 2009 Sheet 19 of 41

Display: DACA (Middle DVI-I)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: DACA (Middle DVI-I)

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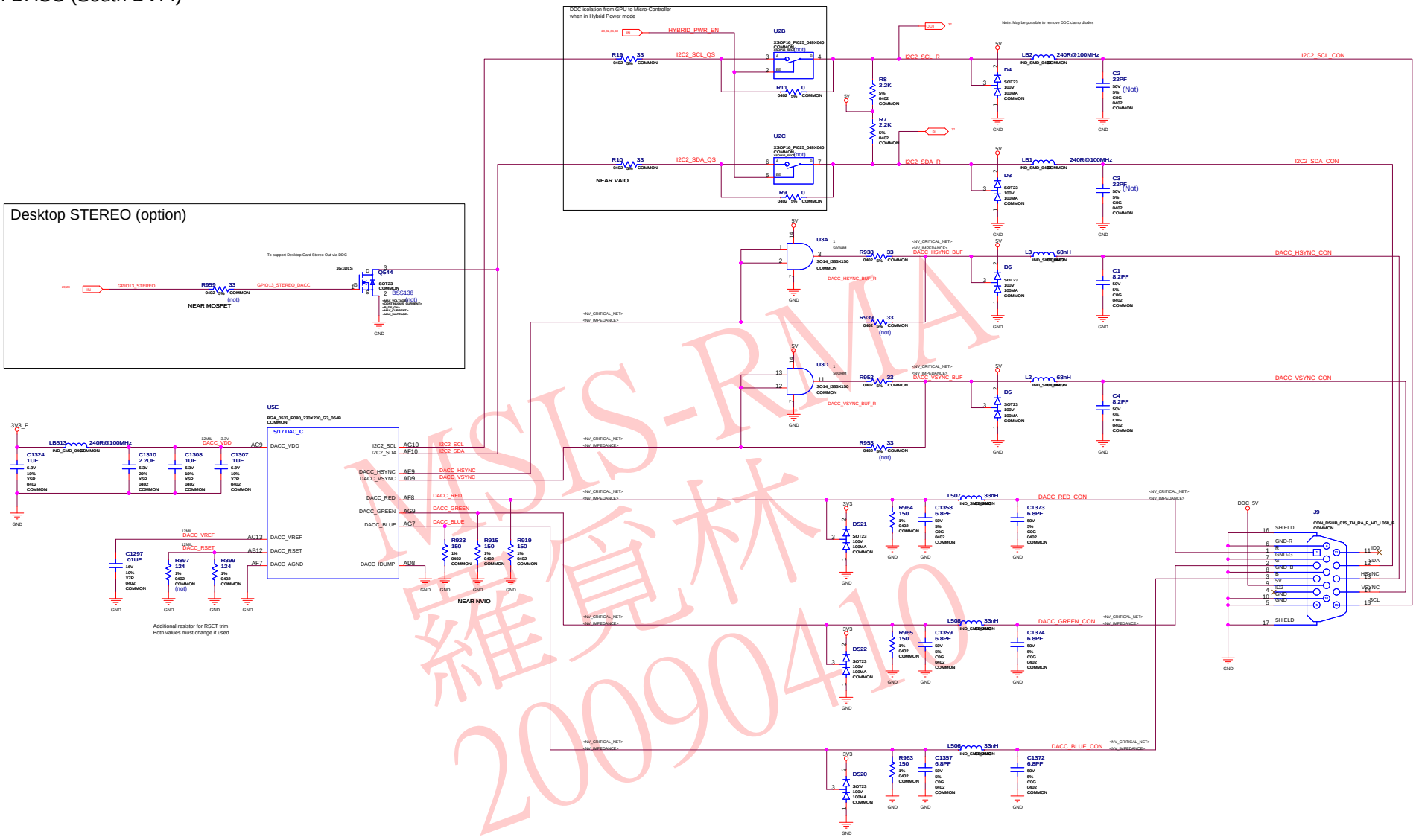
Date: Wednesday, February 11, 2009 Sheet 20 of 41

Display: DACC (South DVI-I)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: DACC (South DVI-I)

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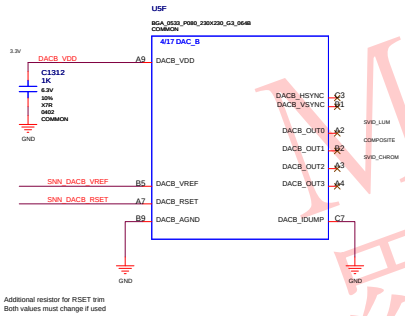
Date: Wednesday, February 11, 2009 | Sheet 21 of 41

Display: DACB (North MiniDIN) SD/HDTV out

11/21 remove TV



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: DACB (North MiniDIN) SD/HDTV out

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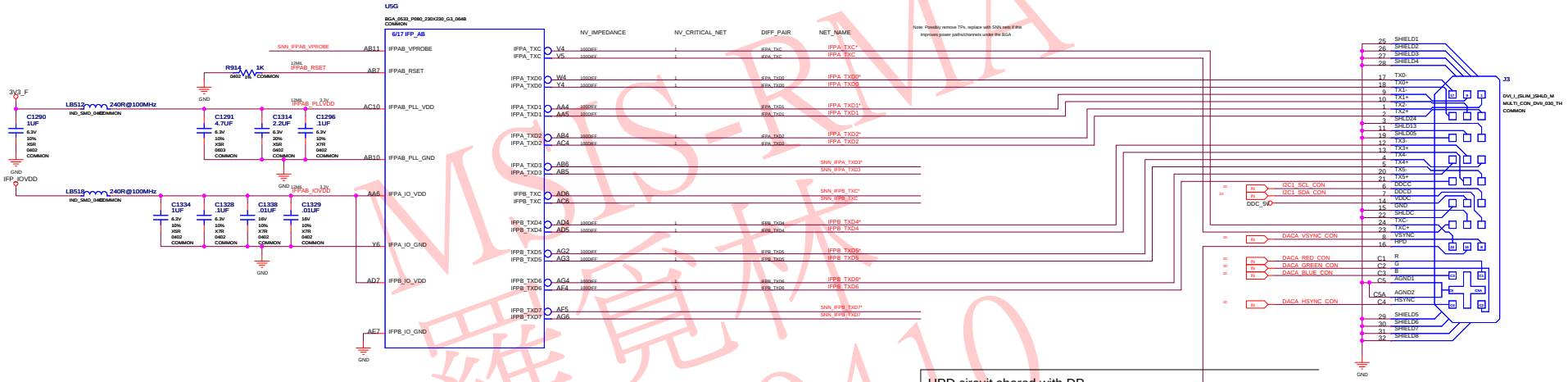
Date: Wednesday, February 11, 2009 Sheet 22 of 41

Display: IFPAB for South DVI-I (with DACC)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: IFPAB for south DVI-I (with DACC)

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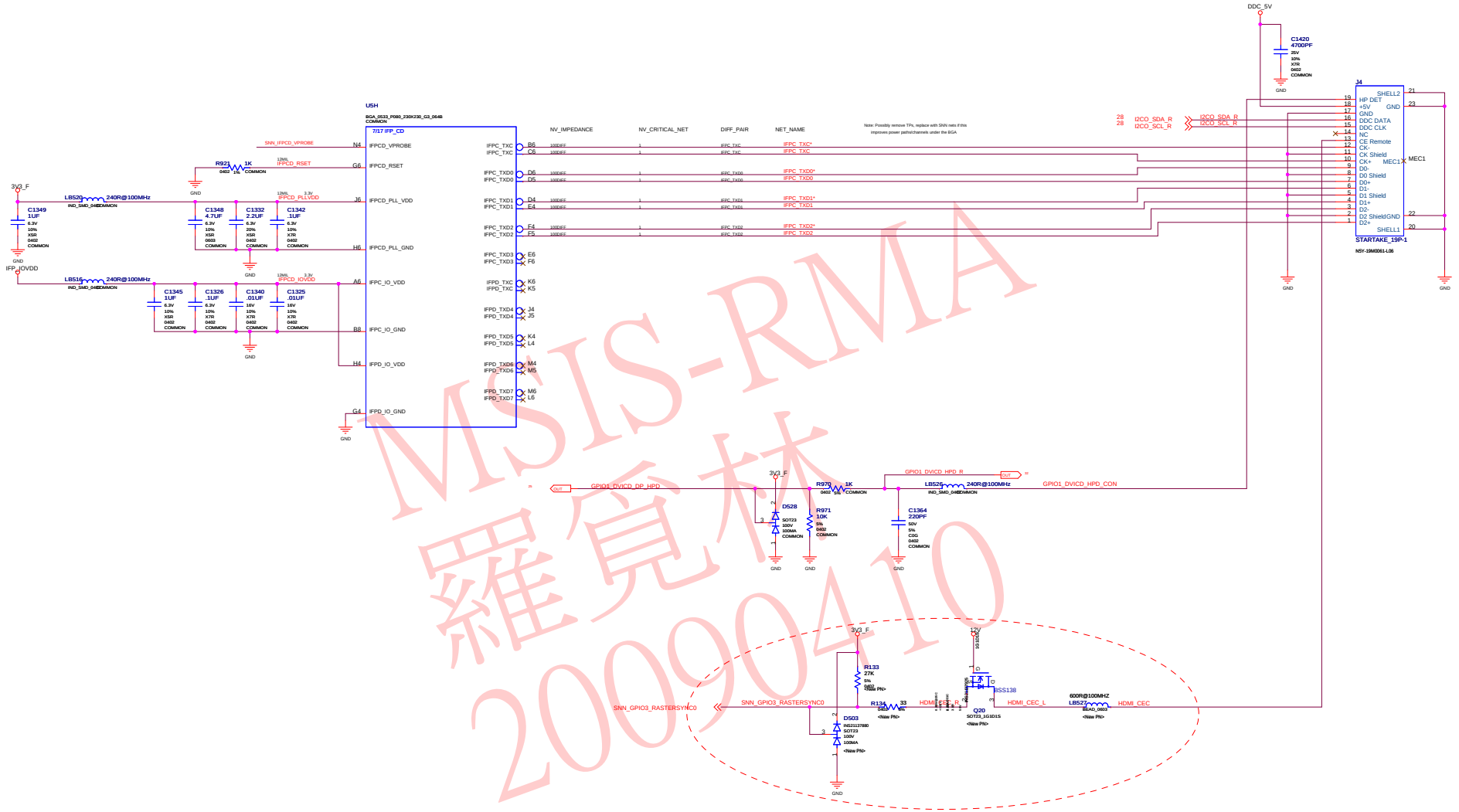
Size: Custom	Document Number: <Doc>		Rev: <FevCode>
Date: Wednesday, February 11, 2009	Sheet 23 of 41		

Display: IFPCD for middle DVI-I (with DACA)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: IFPCD for middle DVI-I (with DACA)

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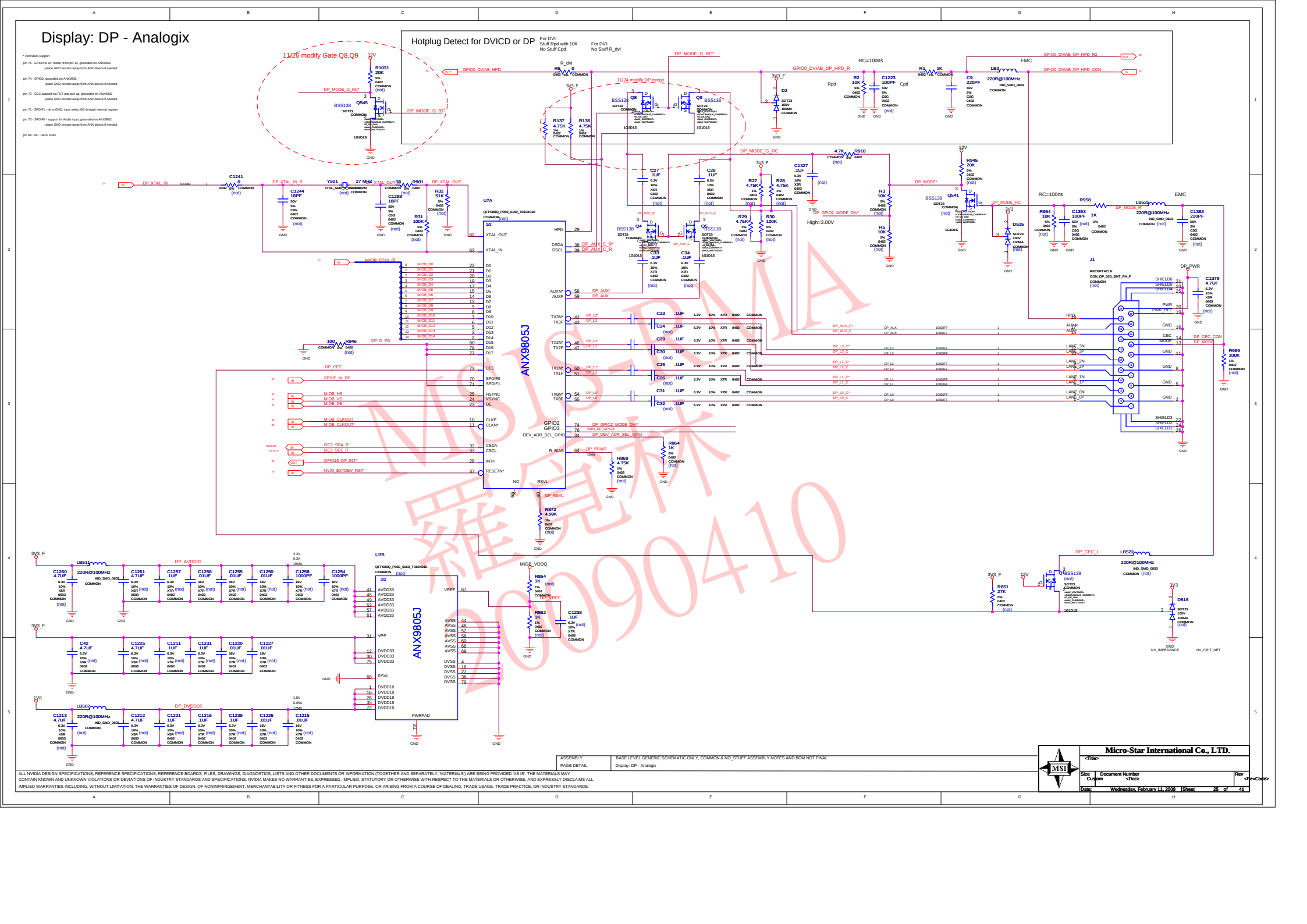
Date: Wednesday, February 11, 2009 Sheet 24 of 41

Display: DP - Analogix



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: DP - Analogix

Size: Custom	Document Number: <Doc>	Rev: <FevCode>
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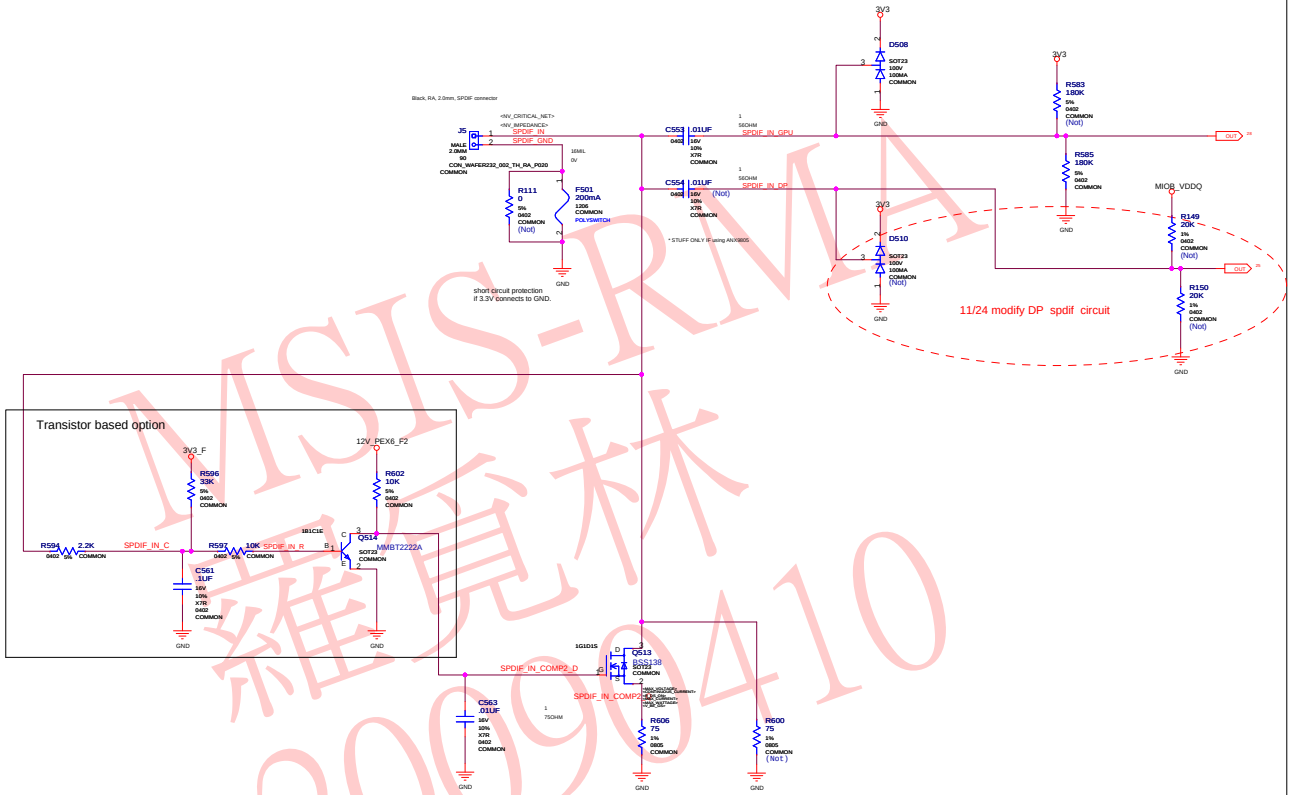
Connectors: SPDIF

SPDIF INPUT / Level Detection



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Connectors: SPDIF

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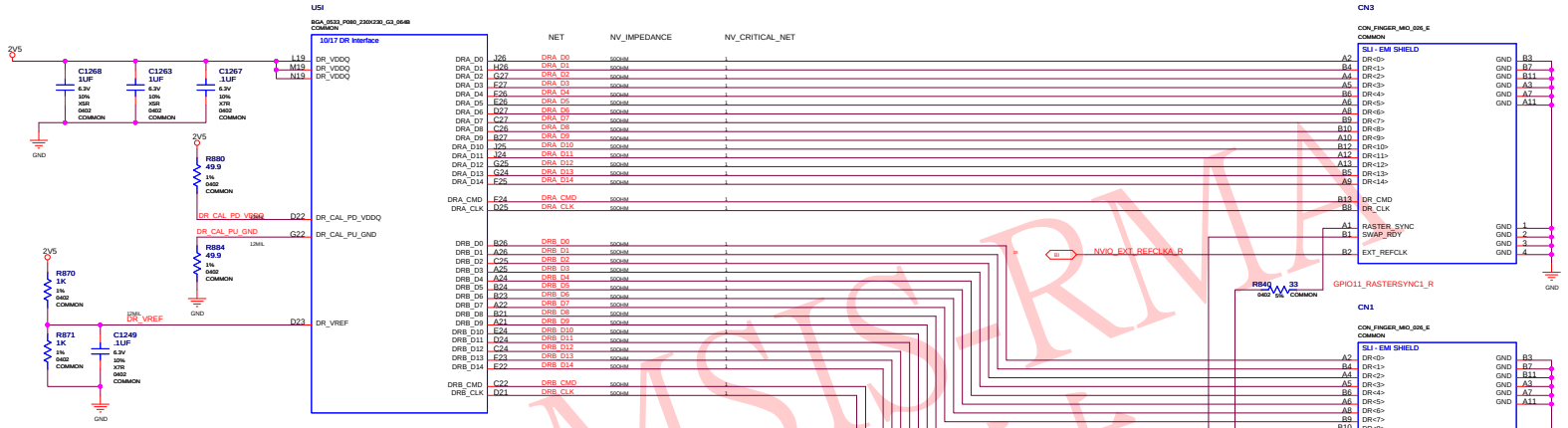
Size: Custom	Document Number: <Doc>	Rev: <FevCode>	
Date: Wednesday, February 11, 2009	Sheet: 26 of 41		

Connectors: DR Interface (Dual SLI)



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ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: Connectors: DR Interface (Dual SLI)

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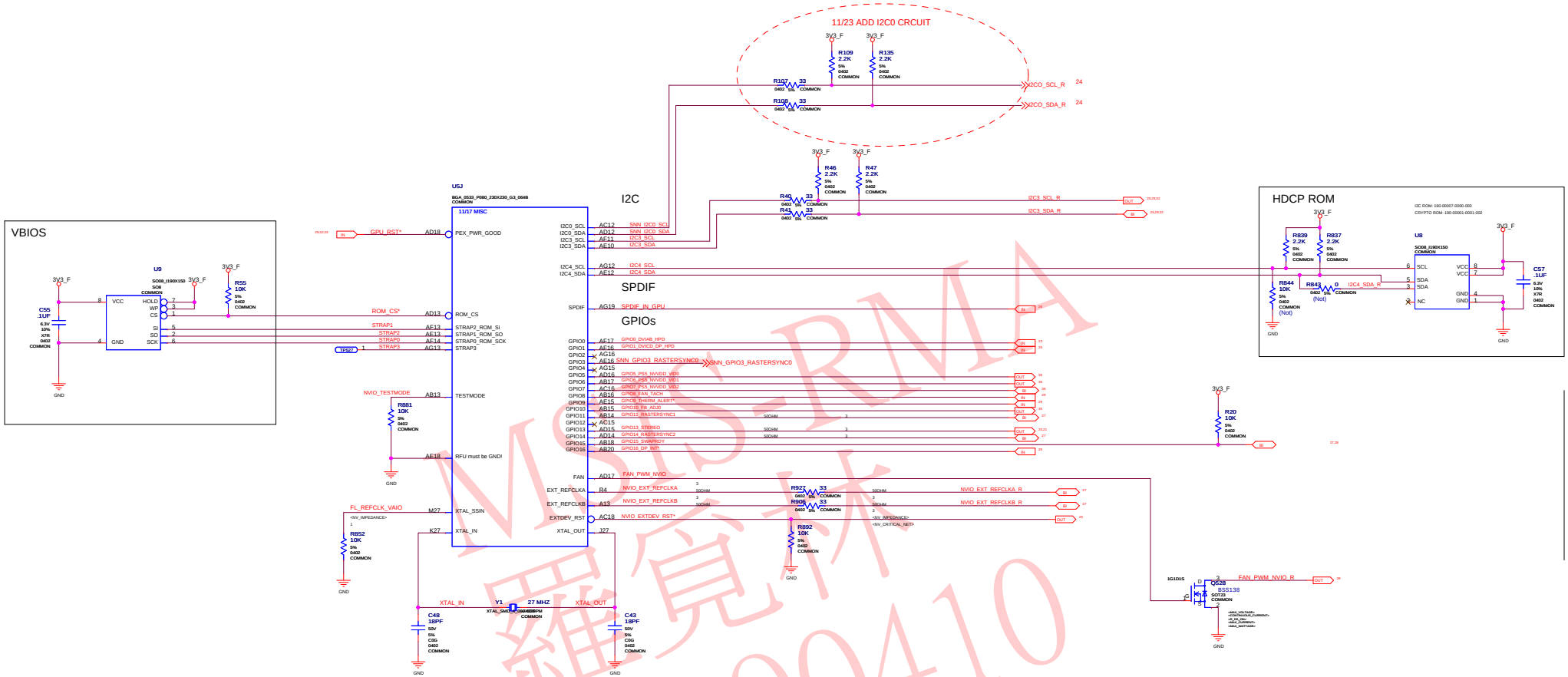
MISC: GPIO / XTAL / VBIOS / HDCP / I2C



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO / XTAL / VBIOS / HDCP / I2C

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<Title>

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MISC: FAN / THERM

TSENSE_OVERT Level Shifter (1.15V to 3.3V)

TSENSE_OVERT is the THERMAL ALERT pin for the internal Temp Sensor

1V15 · 3V3_F · R848 10K · R847 10K · R845 10K · Q519 MMBT2222A · Q520 MMBT2222A · TSENSE_OVERT_R · TSENSE_OVERT* · THERM_SHDN*

Internal GPU Thermal Sensor

Default Thermal Controller

FBVDDQ · TSENSE_AVDD is source by a filter FBVDDQ · LB501 10nH · C799 4.7UF · C821 4.7UF · CB19 1UF · C832 1UF · C845 1UF · 1K

G1M — BGA_2236_P080_P100_4501X450 COMMON — 13/21 THERMAL

AK34 TSENSE_AVDD · AJ33 TSENSE_VREF · AK29 TS_OBS · BR9 THERM_DP -> D+ · BR8 THERM_DN -> D- · BE20 TSENSE_1V5_SEL · BE19 TSENSE_OVERT

TP504 · C867 .1UF · TSENSE_VREF · TP505 · TS_OBS · TSENSE_OVERT

ROUTE DIFFERENTIALLY GUARD GND AROUND IF POSSIBLE

tsense_1v5_sel =0: TS_AVDD = 1.7v ~ 2.1v (default) (wired to gnd)
tsense_1v5_sel =1: TS_AVDD = 1.45v ~ 1.7v (wired to NVVDD)

LM99/MAX6649

(Alternate Thermal Controller)

U509 XSOP08_P065_030X030 COMMON (Not) · R804 200 · C1130 1UF · C71 2200PF · R66 2.2K · R45 2.2K · THERM_DP · THERM_DN · GPIO9_THERM_ALERT*

Note: POR internal thermal control external controls will be DNI

ADT7473

(Secondary thermal controller choice)

U11 XSOP16_P625_040X040 COMMON · C67 .1UF · C69 .1UF · I2C_SCL_THERM · I2C_SDA_THERM · FAN_TACH · THERM_PWM_ADDR_EN* · R65 10K

I2C3_SCL_R · I2C3_SDA_R · R860 0 · R859 0

I2CS_SCL_R · I2CS_SDA_R · R861 0 (Not) · R35 0 (Not)

Option to connect I2CS (SMBus) to Thermal Chip
This is desired for Tesla

FAN Connector

3V3 · R115 10K · Q21 BSS138 · Q23 BSS138 · FAN_CUTOFF_RC_O · C531 1UF · GPU_RST* · 1G1D1S

FAN Connector

D13 BAT54C · R117 10K · R116 10K · R1032 0 · R118 10K (Not) · C1382 1000PF (Not) · C168 1000PF (Not) · C1383 1000PF · J7 MALE 2.00MM N/A 8HEADER4_2MM_1 COMMON

12V_PEX6_F1 · 12/8 add remove R113

FAN_PWM · FAN_TACH_R

GPU Driven Fan and Tach

FAN_PWM_NVIO_R · GPIO8_FAN_TACH · R862 100 · R63 100 · FAN_TACH_R

12/8 add fan 轉速,H/W monitor

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: FAN / THERM

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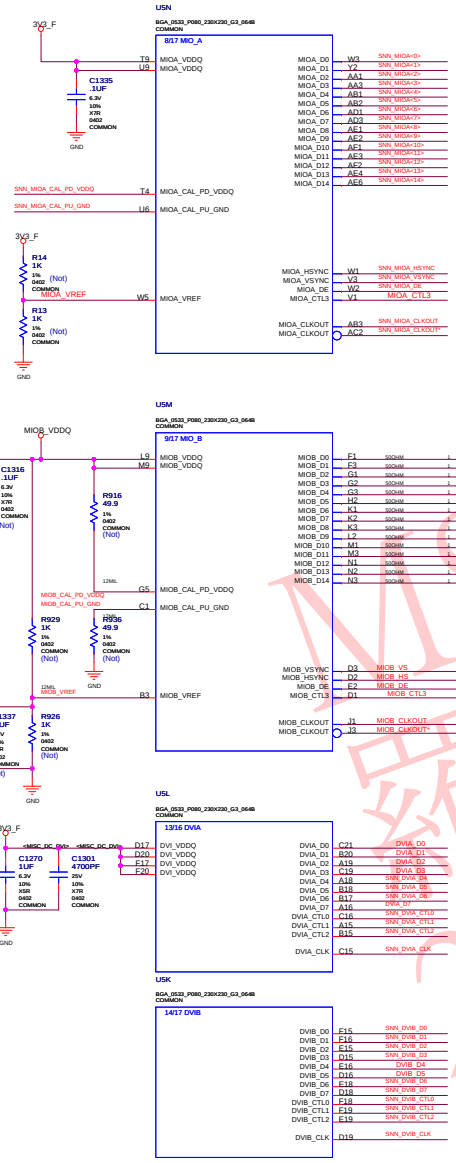
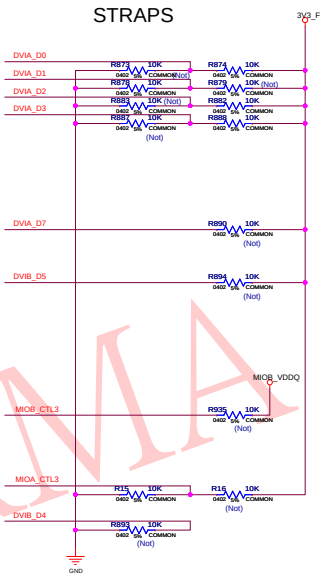
Date: Wednesday, February 11, 2009	Sheet 29 of 41	

MISC: MIO / DVI / STRAPS





STRAP BITS BOOT0 = 0x101000

NR_:_USAGE_____COMMENT_____

00 : GV_WIDTH DEFAULT=0x0 (WIDE)

01 : SUB_VENDOR DEFAULT=0x1 (FROM BIOS)

02 : RAM_CFG[0]

03 : RAM_CFG[1]

04 : RAM_CFG[2]

05 : RAM_CFG[3]

06 : CRYSTAL DEFAULT=0x0 (27MHz)

07 : TV_MODE[0] DEFAULT=0x1 (NTSC_J)
08 : TV_MODE[1]
09 : TV_MODE[2]

10 : PCI_DEVID[0] SET BY BIOS
11 : PCI_DEVID[1]
12 : PCI_DEVID[2]
13 : PCI_DEVID[3] DEFAULT=0x0

14 : FB_SIZE[0] DEFAULT=0x2 (256MB ??)
15 : FB_SIZE[1]
16 : FB_SIZE[2]

17 : PEX_PLL_EN_TERM100 DEFAULT=0x0 (ENABLED)

18 : 3GIO_PAD_CFG_LUT_ADR[0] DEFAULT=0x3 (DESKTOP_DEFAULT)
19 : 3GIO_PAD_CFG_LUT_ADR[1]
20 : 3GIO_PAD_CFG_LUT_ADR[2]
21 : 3GIO_PAD_CFG_LUT_ADR[3]

22 : ROMTYPE[0] DEFAULT=0x1 (AT25S)
23 : ROMTYPE[1]

24 : USER[0] SET BY BIOS
25 : USER[1]
26 : USER[2]
27 : USER[3]

28 : PCI_DEVID_EXT DEFAULT=0x0

STRAP BITS BOOT3 = 0x10100C

NR_:_USAGE_____COMMENT_____

06 : XCLK_555 DEFAULT=0x0

16 : PCI_IOBAR DEFAULT=0x1
0=DISABLE, 1=ENABLE

CFG_Config Width	Vendor
0000 Reserved	
0001 16Mx32 512-bit Qimonda	
0010 16Mx32 512-bit Hynix*	
0011 16Mx32 512-bit Samsung*	
0100 Reserved	
0101 32Mx32 512-bit Qimonda	
0110 32Mx32 512-bit Hynix	
0111 32Mx32 512-bit Samsung	
1000 Reserved	
1001 16Mx32 448-bit Qimonda	
1010 16Mx32 448-bit Hynix	
1011 16Mx32 448-bit Samsung	
1100 Reserved	
1101 32Mx32 448-bit Qimonda	
1110 32Mx32 448-bit Hynix	
1111 32Mx32 448-bit Samsung	

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PAGE DETAIL	MISC: MIO / DVI / STRAPS

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Date: Wednesday, February 11, 2009 Sheet 30 of 41

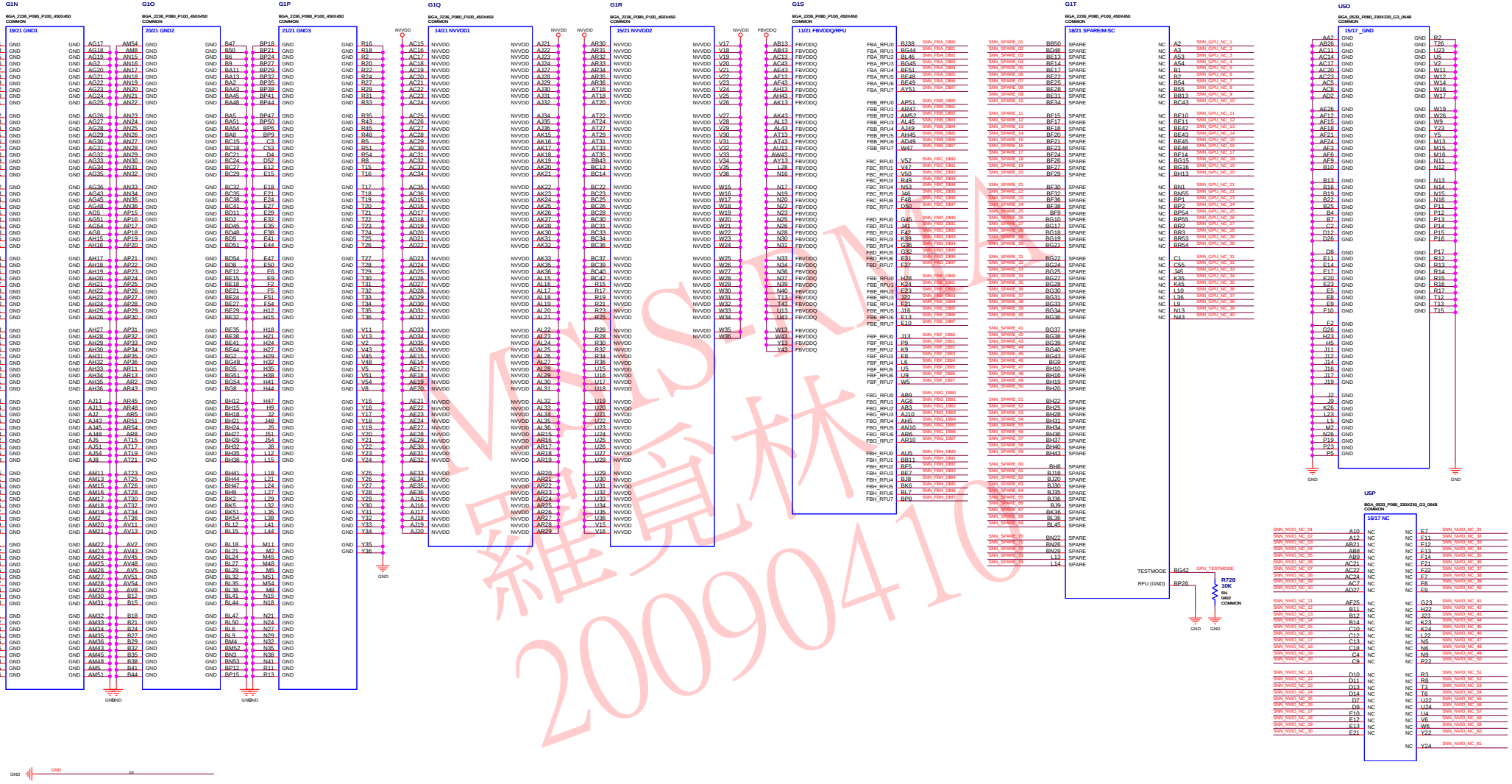
Power and GND (GPU and NVIOx)

GPU SECTION GND

GPU SECTION POWER

GPU SECTION MISC

NVIOx SECTION GND



ASSEMBLY
PAGE DETAIL
BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Power and GND (GPU and NVIOx)

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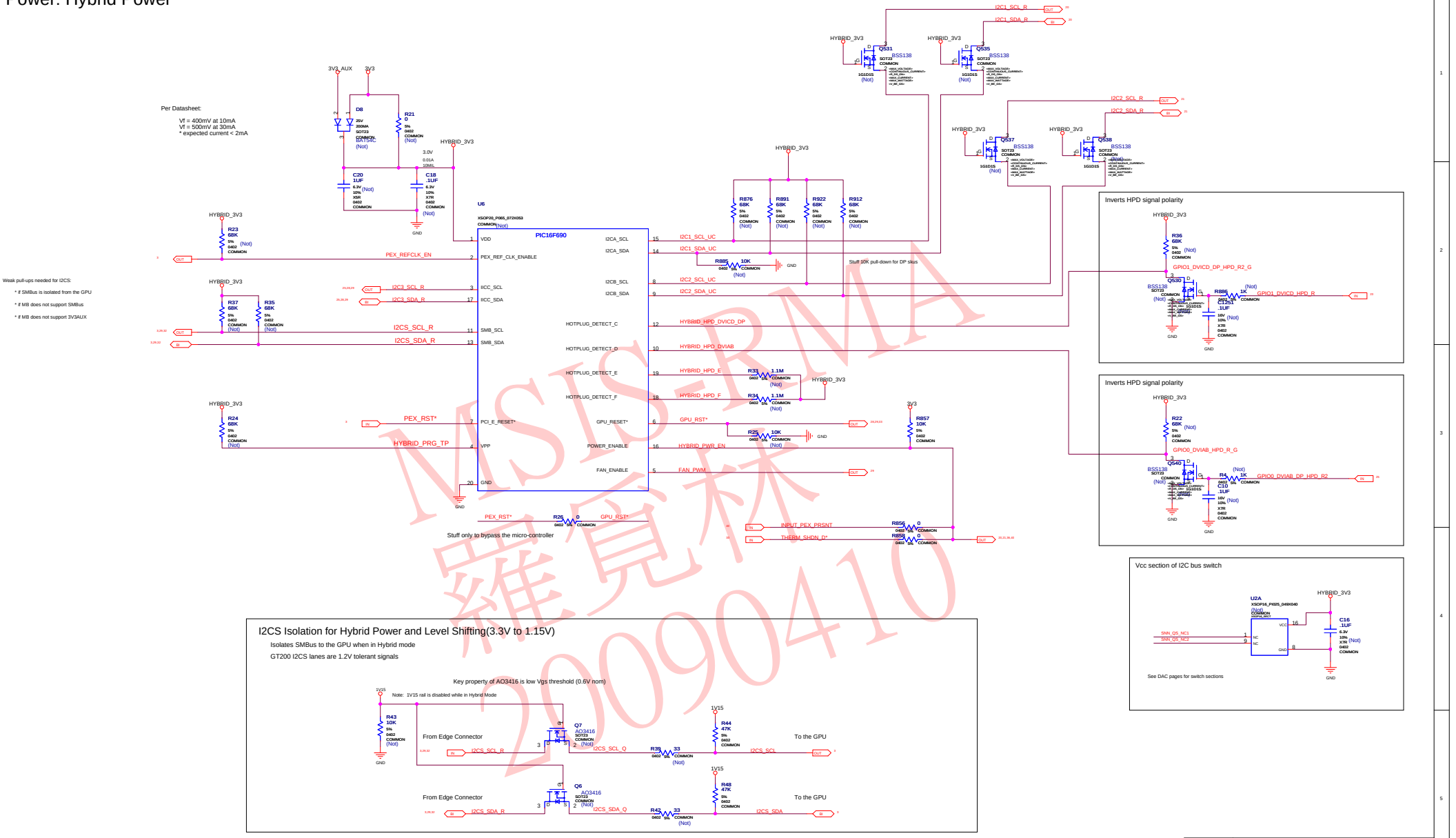
Power: Hybrid Power



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power: Hybrid Power

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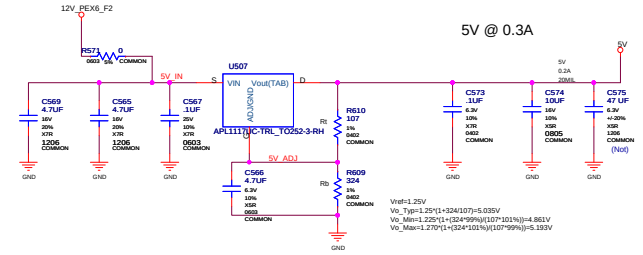
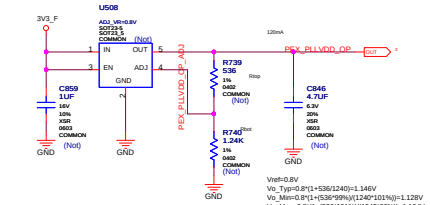
Power Supply: 5V LDO / 3V3_DP / THERM SHUTDOWN LATCH / IFP_IOVDD /PEX_PLVDD

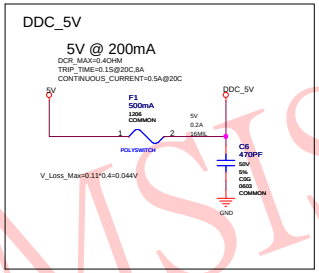
5V Linear



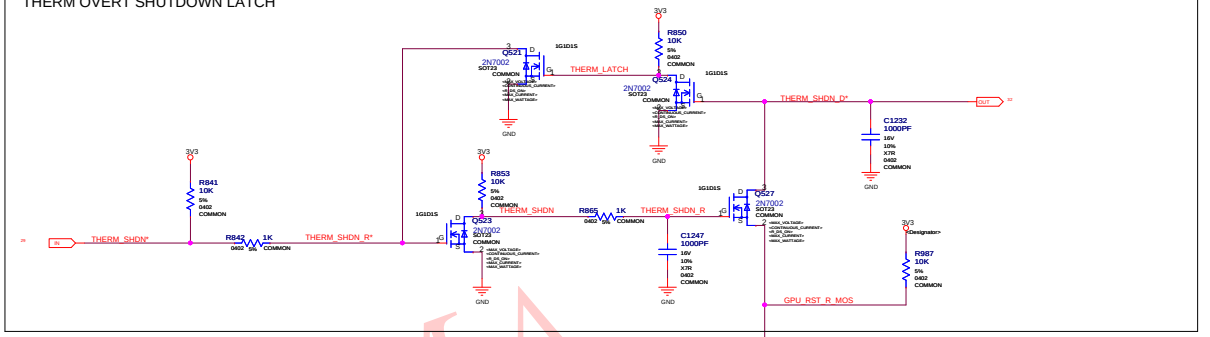
PEX PLLVDD optional Supply



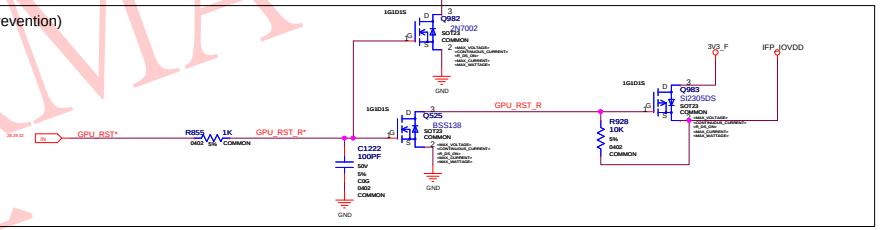
DDC_5V



THERM OVERT SHUTDOWN LATCH

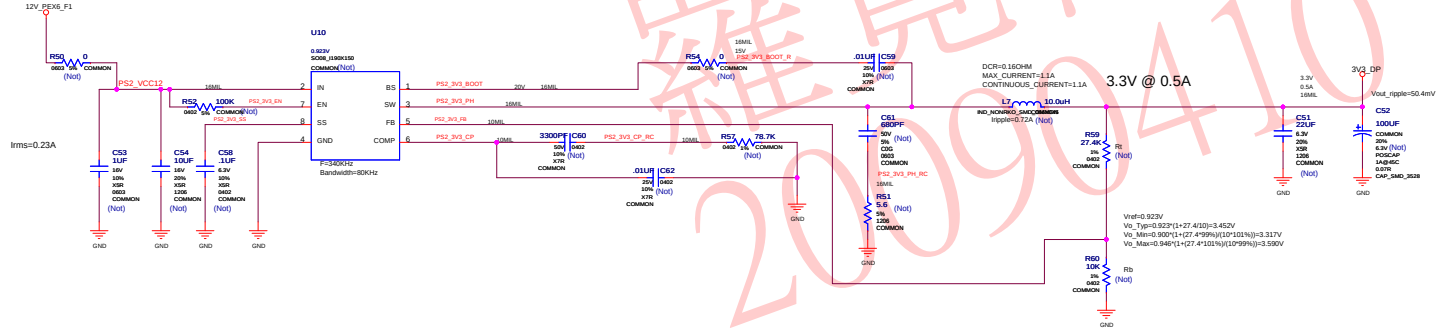


IFP_IOVDD (backdrive prevention)



3V3_DP SWITCHER

(Only required for DisplayPort SKU)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 5V + 5V Alt / SHDN LATCH / IFP_IOVDD

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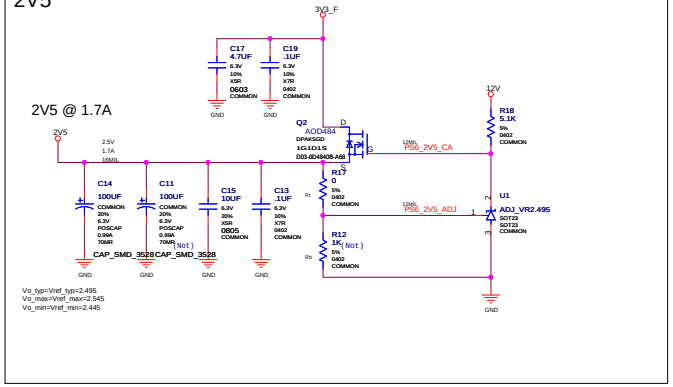
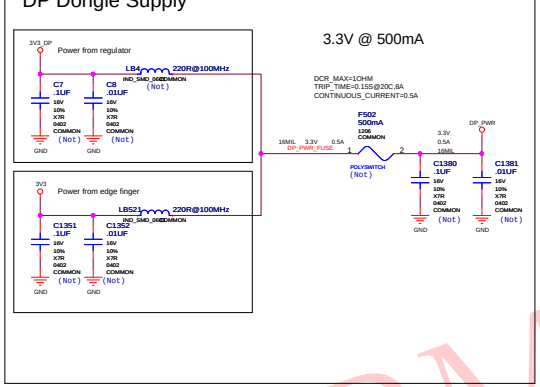
Size: Custom	Document Number: <Doc>	Rev: <FevCode>
Date: Wednesday, February 11, 2009	Sheet 33 of 41	

Power Supply: 2V5, DP_PWR, 8V5 1V15 (PEX_VDD, GV_VDD)

2V5



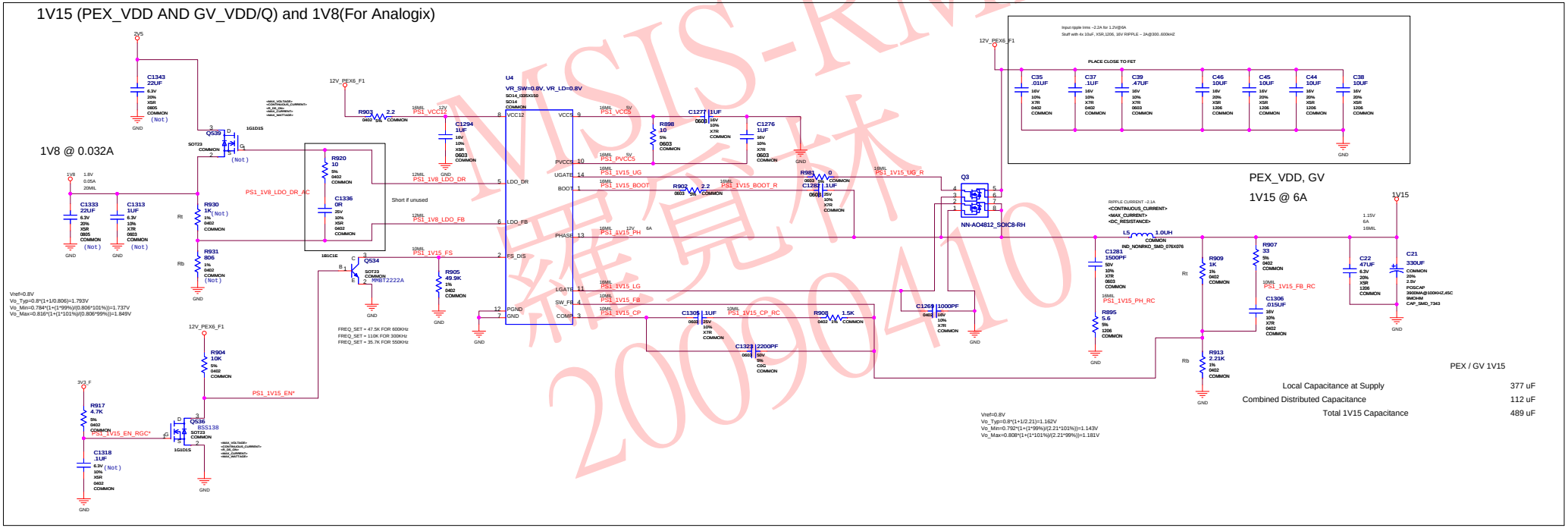
DP Dongle Supply



8V5

11/21:remove 8V5 circuit

1V15 (PEX_VDD AND GV_VDD/Q) and 1V8(For Analogix)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 2V5, DP_PWR, 1V15 (PEX_VDD, GV_VDD)

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Size: Custom	Document Number: <Doc>
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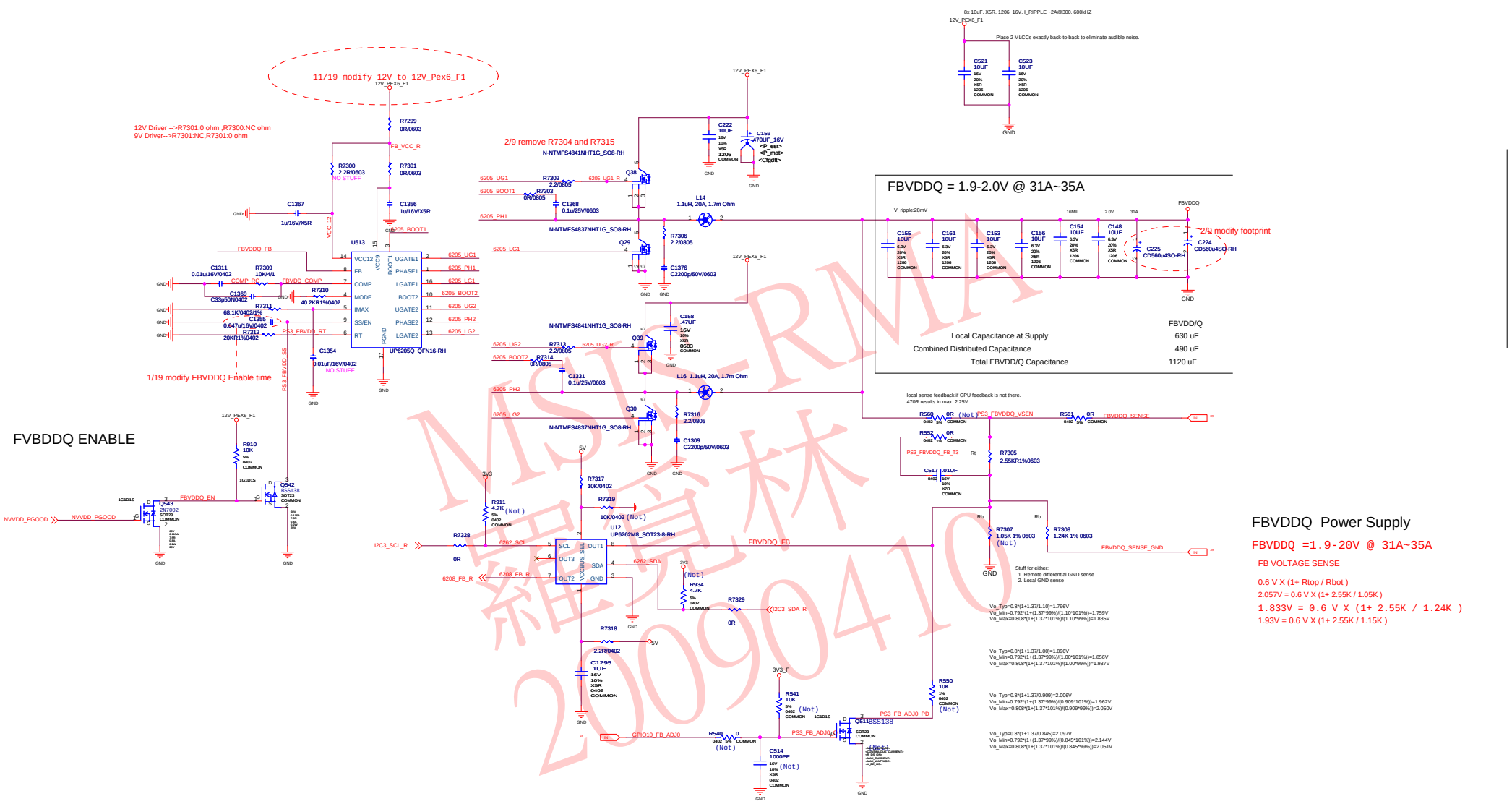
Power Supply: Combined FBVDD/Q



	FBVDD/Q
Local Capacitance at Supply	630 uF
Combined Distributed Capacitance	490 uF
Total FBVDD/Q Capacitance	1120 uF

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ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Power Supply: Combined FBVDD/Q

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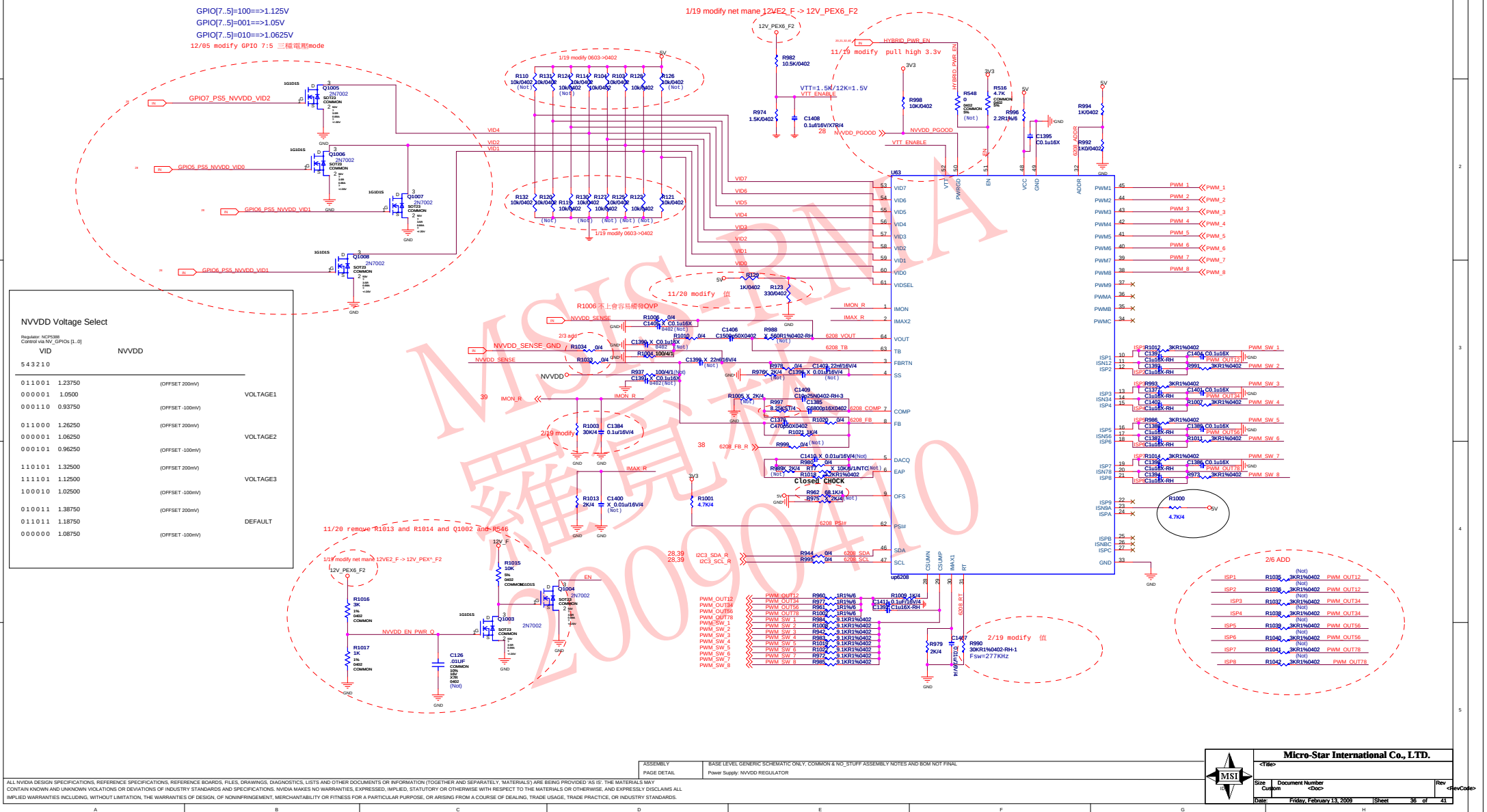
Size: Custom | Document Number: <Doc> | Rev: <FevCode>
Date: Wednesday, February 11, 2009 | Sheet 35 of 41

Power Supply: NVVDD Regulator



NVVDD Voltage Select

Regulator: NCP5388
Control via NV_GPIOs [1..0]

VID 543210	NVVDD	
011001	1.23750	(OFFSET 200mV)
000001	1.0500	VOLTAGE1
000110	0.93750	(OFFSET -100mV)
011000	1.26250	(OFFSET 200mV)
000001	1.06250	VOLTAGE2
000101	0.96250	(OFFSET -100mV)
110101	1.32500	(OFFSET 200mV)
111101	1.12500	VOLTAGE3
100010	1.02500	(OFFSET -100mV)
010011	1.38750	(OFFSET 200mV)
011011	1.18750	DEFAULT
000000	1.08750	(OFFSET -100mV)

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD REGULATOR

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<Title>

Size	Document Number	Rev
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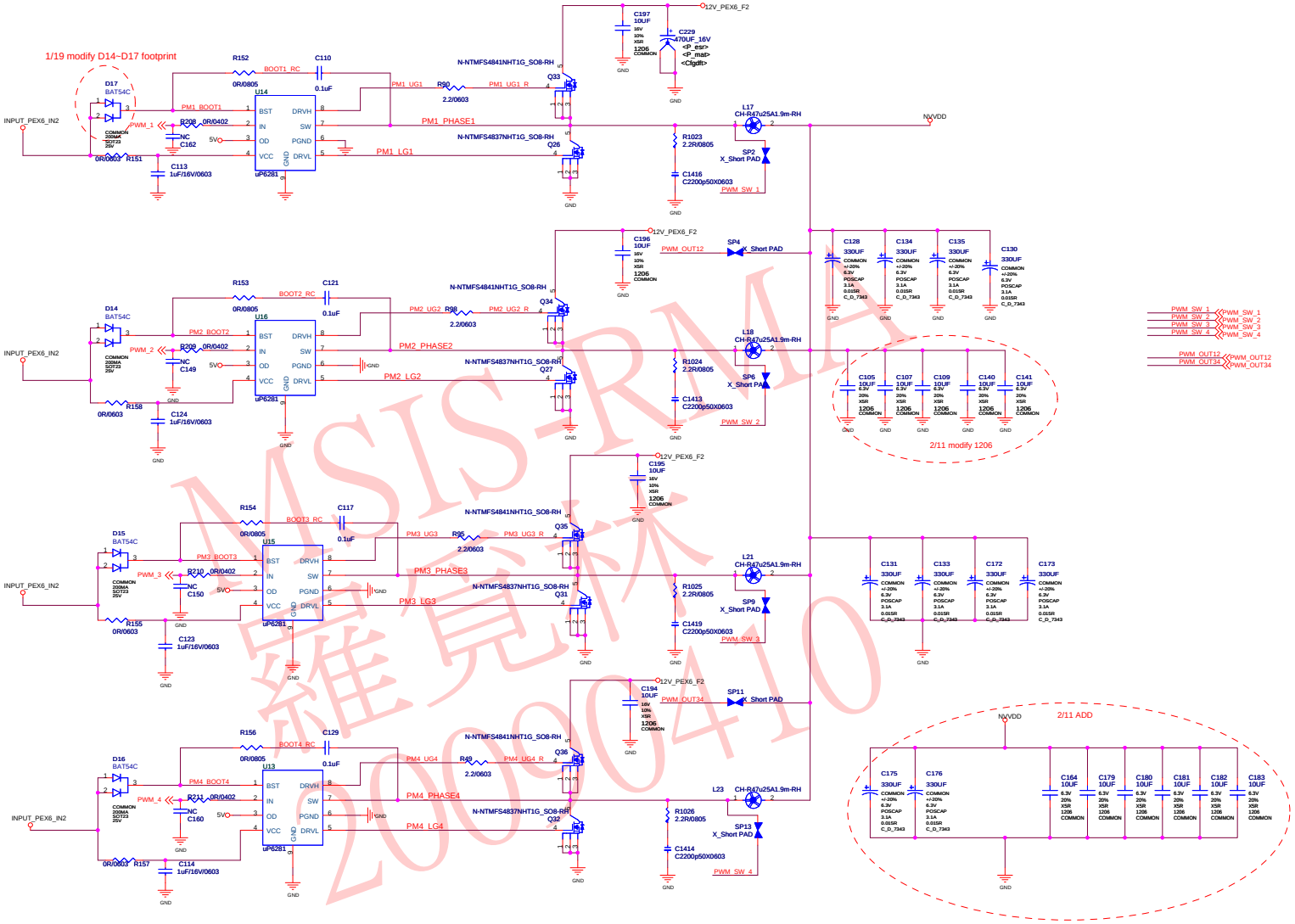
Date: Friday, February 13, 2009 Sheet 36 of 41

Power Supply: NVVDD Phase 1,2 powered from external PEX 6PIN



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 1-2 of 4

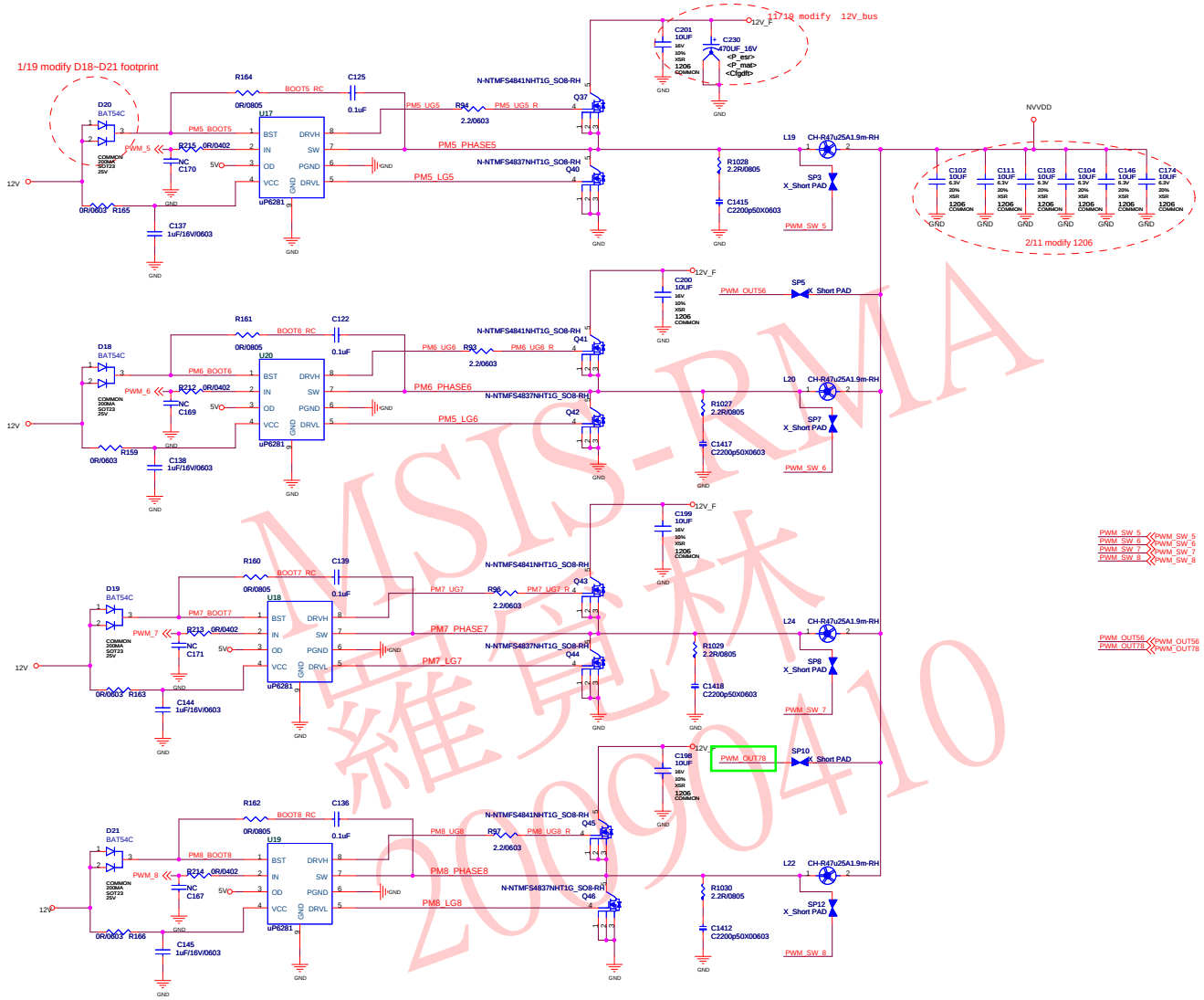
Micro-Star International Co., LTD.

<Title>

Size	Document Number	Rev
Custom	<Doc>	<FevCode>

Date: Wednesday, February 11, 2009 Sheet 37 of 41

Power Supply: NVVDD Phase 5~8 powered from internal PEX edge connector



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 3-4 of 4

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Power Supply: NVVDD power control

I2C Slave Address select circuit

Address 0X5EH

Address 0X5CH

Power Wattage Monitor

割斷software控制電壓

GPIO改為GPIN

GPIO 要用software 設為GPIO OUT,避免耗損電流

12/8 add Reconnoiter fan rotational speed to reconnoiter

NVVDD & FBVDDQ SENSE/MSUR

NVVDD CURRENT

NVVDD Voltage
1.18V

FBVVDQ Voltage
2V

POWER CONTROL 1 CIRCUITRY

RESISTORS AND CAPS ARE ALL PLACEHOLDERS
BASED ON VALUES DETERMINED BY JLOO 11/29/07

CTL1 ASSERTS HIGH WHEN THERE IS A JUMP IN CURRENT DRAW

POWER CONTROL 0 CIRCUITRY

RESISTORS AND CAPS ARE ALL PLACEHOLDERS
BASED ON VALUES DETERMINED BY JLOO 11/29/07

CTL0 ASSERTS HIGH WHEN THERE IS A JUMP IN CURRENT DRAW

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	NVVDD & FBVDDQ SENSE/MSUR

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Rev: <RevCode>	
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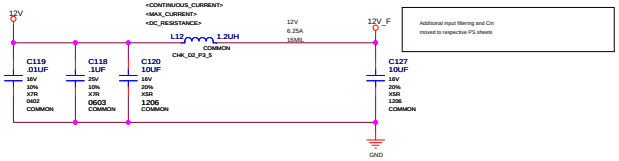
Power: Input Rail Filter and Detection Logic

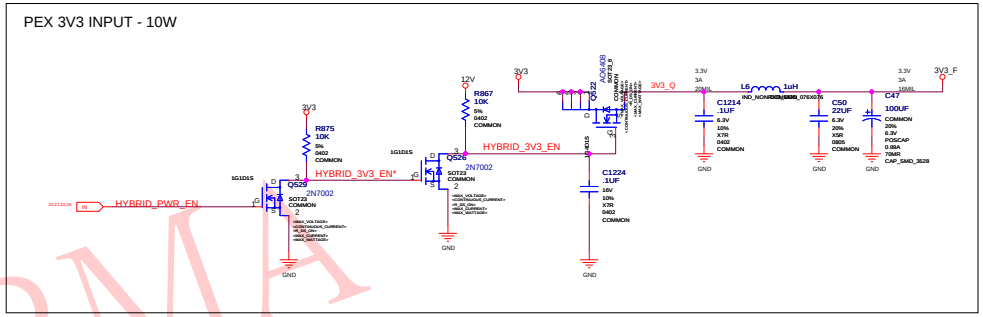
Connector Power State Table

3x3 Connector	2x3 Connector		Power	STATE
Connected	Connected		225W	Full Perf
Connected	Not Connected		150W	Board Off
Not Connected	Connected		150W	Board Off
Not Connected	Not Connected		75W	Board Off

PEX_12V INPUT - 66W

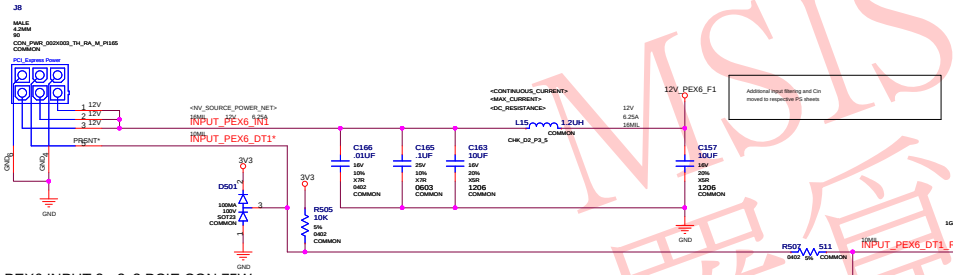


PEX 3V3 INPUT - 10W



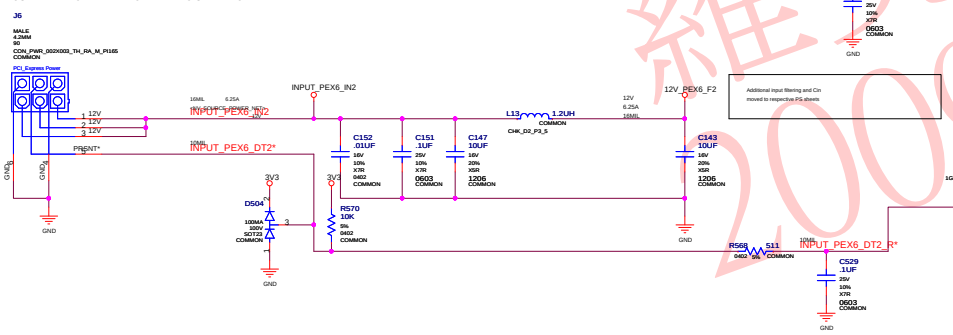
PEX6 INPUT 1 - 2x3 PCIE CON 75W

MUST BE ATTACHED AND POWERED TO START BOARD

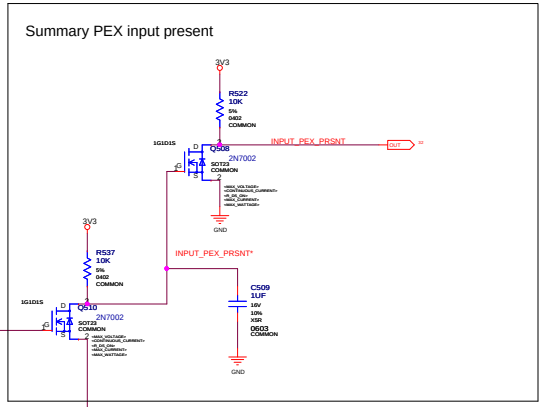


PEX6 INPUT 2 - 2x3 PCIE CON 75W

MUST BE ATTACHED AND POWERED TO START BOARD



Summary PEX input present



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Thermal/Mechanical/ID

Bracket and Assembly

GPU Socket

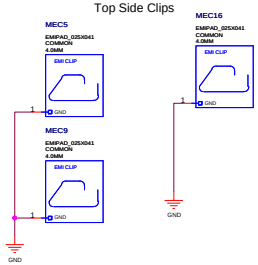
GPU Stiffener

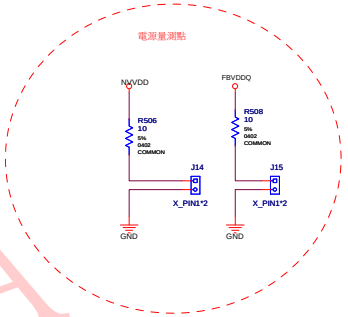
NVIOx Socket

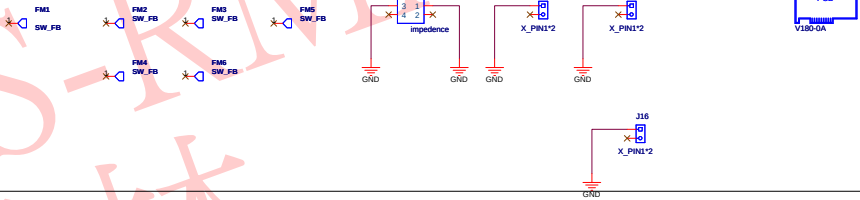
Hockey Stick Retention Mechanism

EMI Gnd Clips

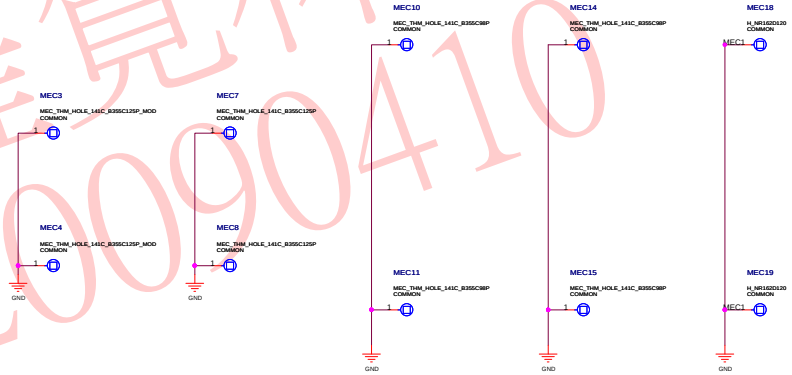
Top Side Clips







THERMAL/MECHANICAL HOLES



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