GND_TPVSS GND_A2VSSN GND_AVSSN GND_A2VSSQ GND_AVSSQ GND_MPVSS GND_PVSS GND_R2SET GND_RSET

The following grounds should be routed back to their respective regulators and then tied directly to the ground plane with one via: GND_PVSS, GND_MPVSS, GND_TPVSS, and GND_A2VSSN. The other ground pins (GND_AVSSN, GND_A2VSSQ, GND_RSET, GND_R2SET) should be tied to the ground plane directly through one via as close to the pins as possible without connecting to anything else. If space is an issue it is possible to use one via for two adjacent pins.

+VDDQ_BUS

Use 47uF Tant. 16V 20% D size (P/N 4230047600), 800mR Max. ESR and Max. ripple 430mA @ 100kHz or 100uF, Alum. 6.3V 20% 6.3mm dia (P/N 4261010700), 440mR Max. ESR and Max. ripple 230mA @ 100kHz or 47uF, Alum. 6.3V 20% 5mm dia (P/N 4262047600), 760mR Max. ESR and Max. ripple 150mA @ 100kHz

+5V_BUS +3.3V_BUS

+12V_BUS

C10 place at the AGP connector
C10 X_10uF 20V 4239010600 DNI

C2 47uF 10V 4261010700 Biggest footprint

C5 X_47uF 6.3V >=6.3V DNI

C8 X_47uF 6.3V >=6.3V DNI

AGP_SBA[7..0] (2)
AGP_ST[2..0] (2)
AGP_C/BE#[3..0] (2)
AGP_AD[31..0] (2)

MAGP1

	A1	12V	OVRCNT#	B1	
AGP_TYPEDET#	A2	TYPEDET#	5.0V	B2	
AGP_GC_8X_DET#	A3	GC_DET#/RESEVED	5.0V	B3	
	A4	USB-	USB+	B4	
	A5	GND	GND	B5	
	A6	INTA#	INTB#	B6	
	A7	RST#	CLK	B7	
	A8	GNT#	REQ#	B8	
	A9	VCC3.3	VCC3.3	B9	
AGP_ST1	A10	ST1	ST0	B10	AGP_ST0
	A11	MB_DET#/RESERVED	ST2	B11	AGP_ST2
	A12	DBI_HI/PIPE#	RBF#	B12	
	A13	GND	GND	B13	
	A14	WBF#	DBI_LO/RESERVED	B14	
AGP_SBA1	A15	SBA1	SBA0	B15	AGP_SBA0
	A16	VCC3.3	VCC3.3	B16	
AGP_SBA3	A17	SBA3	SBA2	B17	AGP_SBA2
	A18	SB_STB#	SB_STB	B18	
	A19	GND	GND	B19	
AGP_SBA5	A20	SBA5	SBA4	B20	AGP_SBA4
AGP_SBA7	A21	SBA7	SBA6	B21	AGP_SBA6
	A22	KEY	KEY	B22	
	A23	KEY	KEY	B23	
	A24	KEY	KEY	B24	
	A25	KEY	KEY	B25	
AGP_AD30	A26	AD30	AD31	B26	AGP_AD31
AGP_AD28	A27	AD28	AD29	B27	AGP_AD29
	A28	VCC3.3	VCC3.3	B28	
AGP_AD26	A29	AD26	AD27	B29	AGP_AD27
AGP_AD24	A30	AD24	AD25	B30	AGP_AD25
	A31	GND	GND	B31	
AGP_C/BE#3	A32	AD_STB1#	AD_STB1	B32	
	A33	C/BE3#	AD23	B33	AGP_AD23
AGP_AD22	A34	VDDQ	VDDQ	B34	
AGP_AD20	A35	AD22	AD21	B35	AGP_AD21
	A36	AD20	AD19	B36	AGP_AD19
	A37	GND	GND	B37	
AGP_AD18	A38	AD18	AD17	B38	AGP_AD17
AGP_AD16	A39	AD16	C/BE2#	B39	AGP_C/BE#2
	A40	VDDQ	VDDQ	B40	
	A41	FRAME#	IRDY#	B41	
	A42	KEY	KEY	B42	
	A43	KEY	KEY	B43	
	A44	KEY	KEY	B44	
	A45	KEY	KEY	B45	
	A46	TRDY#	DEVSEL#	B46	
	A47	STOP#	VDDQ	B47	
	A48	PME#	PERR#	B48	
	A49	GND	GND	B49	
	A50	PAR	SERR#	B50	
AGP_AD15	A51	AD15	C/BE1#	B51	AGP_C/BE#1
	A52	VDDQ	VDDQ	B52	
AGP_AD13	A53	AD13	AD14	B53	AGP_AD14
AGP_AD11	A54	AD11	AD12	B54	AGP_AD12
	A55	GND	GND	B55	
AGP_AD9	A56	AD9	AD10	B56	AGP_AD10
AGP_C/BE#0	A57	C/BE0#	AD8	B57	AGP_AD8
	A58	VDDQ	VDDQ	B58	
	A59	AD_STB0#	AD_STB0	B59	
AGP_AD6	A60	AD6	AD7	B60	AGP_AD7
	A61	GND	GND	B61	
AGP_AD4	A62	AD4	AD5	B62	AGP_AD5
AGP_AD2	A63	AD2	AD3	B63	AGP_AD3
	A64	VDDQ	VDDQ	B64	
	A65	AD0	AD1	B65	AGP_AD1
AGP_AD0	A66	VREFGC	VREFCG	B66	AGP_AGPREF

UNIVERSAL AGP BUS

(2) AGP_INTR#
(2) AGP_GNT#
(2) AGP_WBF#
(2) AGP_SB_STB#
(2) AGP_MB_8X_DET#
(2) AGP_DBI_HI

R83 0R

AGP_SB_STB (2)

R86 0R

AGP_RBF# (2)
AGP_DBI_LO (2)

+5V_BUS

C11 100nF X7R

R3 100R

AGP_RESET#

(2,14) AGP_RESET#

R4 180R

U6A SN74ACT86D

COMMON

(2) AGP_AD_STB1#

AGP_AD_STB1 (2)

(2) AGP_FRAME#

AGP_IRDY# (2)

(2) AGP_TRDY#
(2) AGP_STOP#

AGP_DEVSEL# (2)

(2) AGP_PAR

(2) AGP_AD_STB0#

AGP_AD_STB0 (2)

AGP_TYPEDET#

R19 0R

For retail, 1K ohm pull-down causes AMD system detects AGP2X only

+12V, TYPEDET# short protection for OEM (1KR)

AGP_GC_8X_DET#

R81 0R

AGP_VREFGC

+3.3V_BUS

R90 47K

U6D SN74ACT86D

AGP_MB_8X_DET#

TEST

R91 1K

+VDDQ_BUS

2N7002E Q10

R92 147R

R_AGP8X must be 1% resistor to provide 350mV +/- 5% on Vref

R_AGP8X

R93 332R

R94 100R

C19 10nF

UNIVERSAL VREFGC CIRCUIT (2X, 4X, 8X)

+VDDQ_BUS

R88 169R

Q9 2N7002E

TEST

R89 71.5R

AGP_AGPTEST

AGP_AGPTEST (2)

AGP_AGPREF
AGP_VREFGC

R84 X_0R
R85 X_0R

Keep stubs short

R_AGP8X must be 1% resistor to provide 350mV +/- 5% on Vref

R_AGP8X

+VDDQ_BUS

2N7002E Q11

TEST

R95 147R

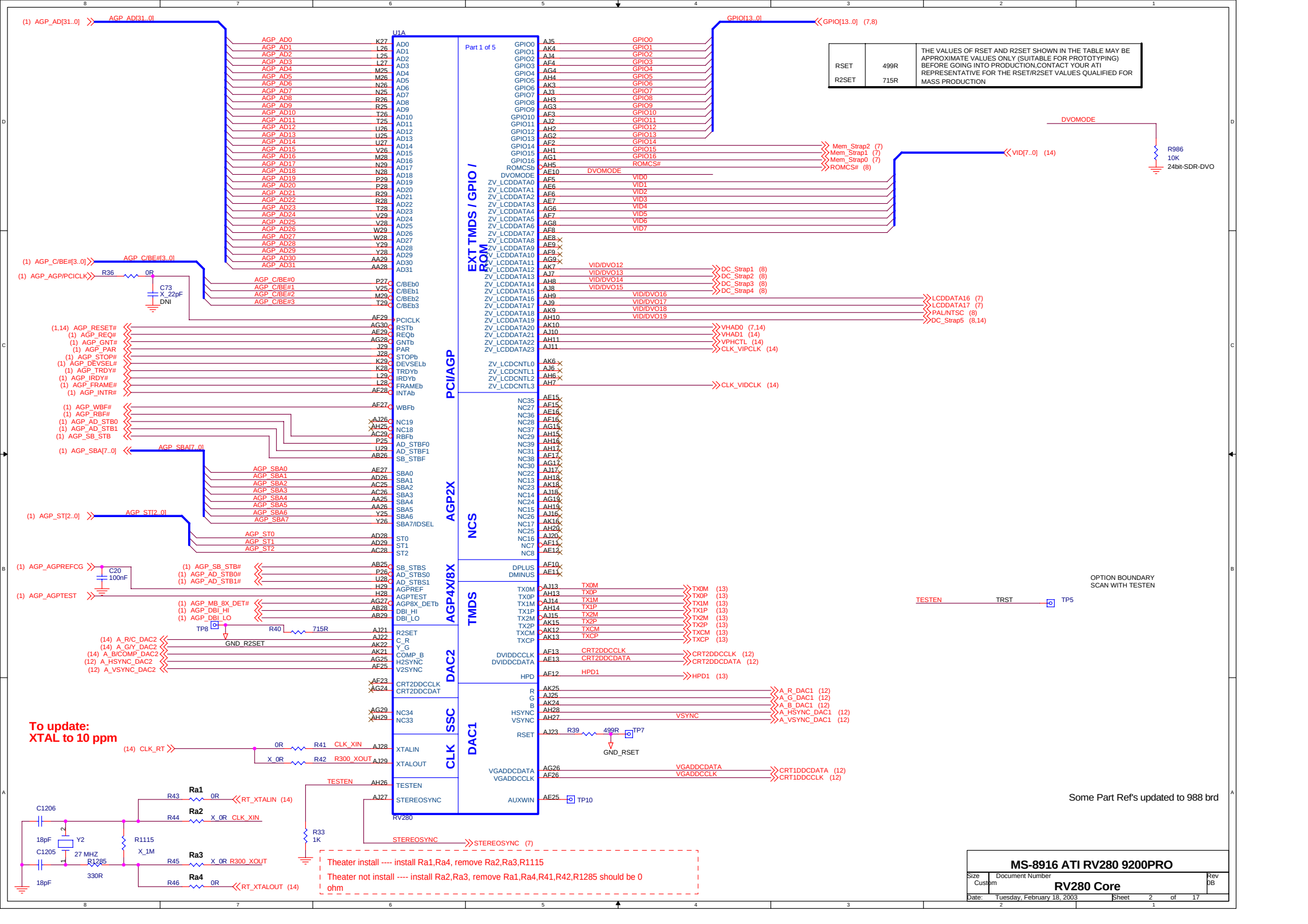
R96 332R

R97 100R

C21 10nF

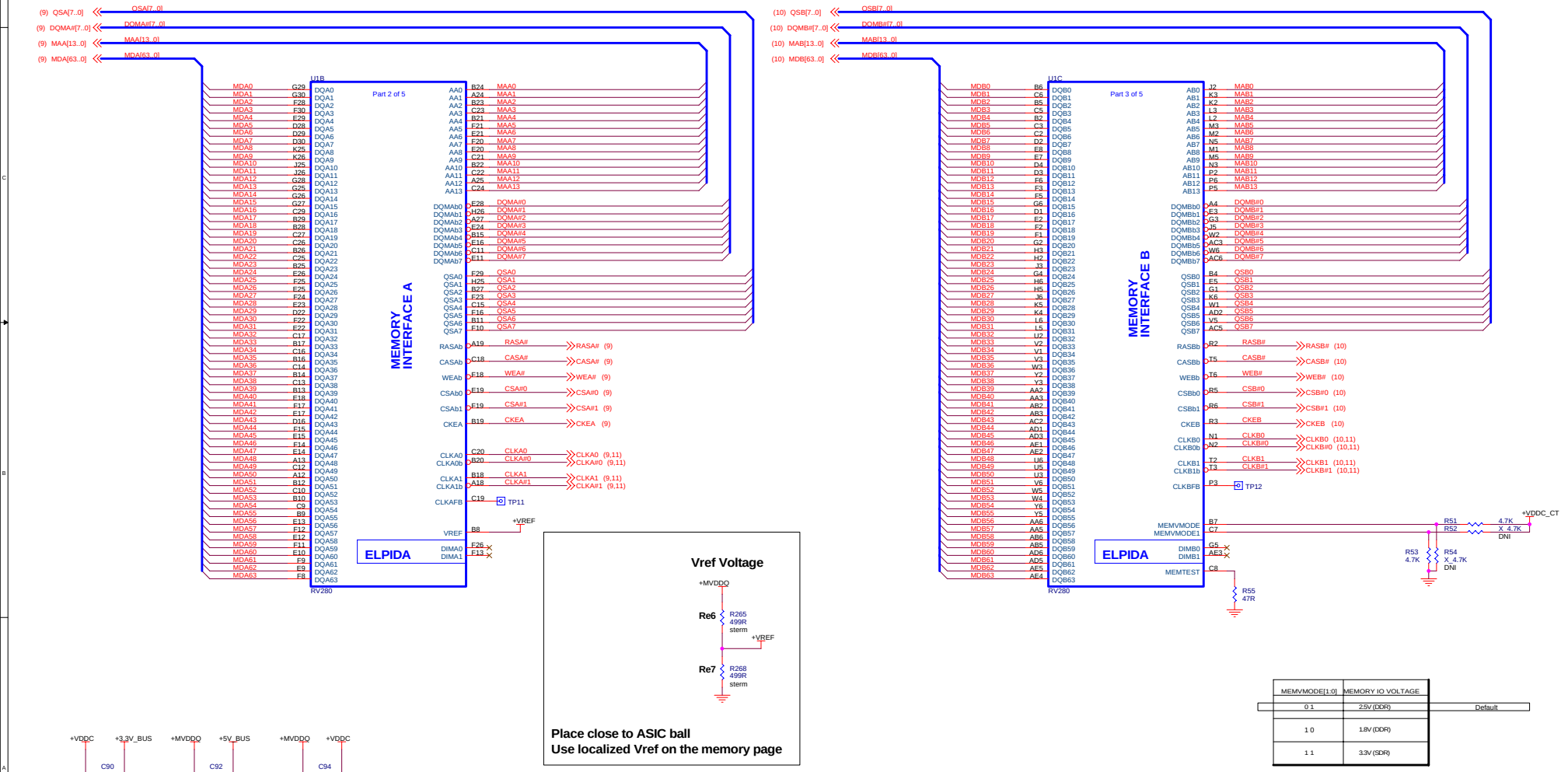
AGP_AGPREFCG (2)

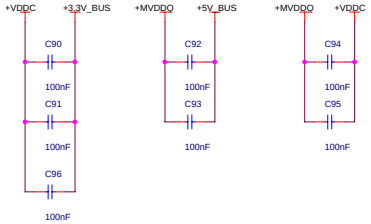
MS-8916 ATI RV280 9200PRO		
Size: Custom	Document Number: AGP Bus 8X	Rev: 0B
Date: Tuesday, February 18, 2003	Sheet 1 of 17	


U1A
Part 1 of 5
PCI/AGP
AGP2X
AGP4X/8X
NCS
TMDS
DAC2
SSC
CLK
DAC1
EXT TMDS / GPIO / ROM
RV280
RSET 499R
R2SET 715R
THE VALUES OF RSET AND R2SET SHOWN IN THE TABLE MAY BE APPROXIMATE VALUES ONLY (SUITABLE FOR PROTOTYPING) BEFORE GOING INTO PRODUCTION,CONTACT YOUR ATI REPRESENTATIVE FOR THE RSET/R2SET VALUES QUALIFIED FOR MASS PRODUCTION
To update:
XTAL to 10 ppm
Theater install ---- install Ra1,Ra4, remove Ra2,Ra3,R1115
Theater not install ---- install Ra2,Ra3, remove Ra1,Ra4,R41,R42,R1285 should be 0 ohm
OPTION BOUNDARY SCAN WITH TESTEN
Some Part Ref's updated to 988 brd
MS-8916 ATI RV280 9200PRO
RV280 Core
Size Custom
Document Number
Rev 0B
Date: Tuesday, February 18, 2003
Sheet 2 of 17

MEMORY CHANNEL A

MEMORY CHANNEL B



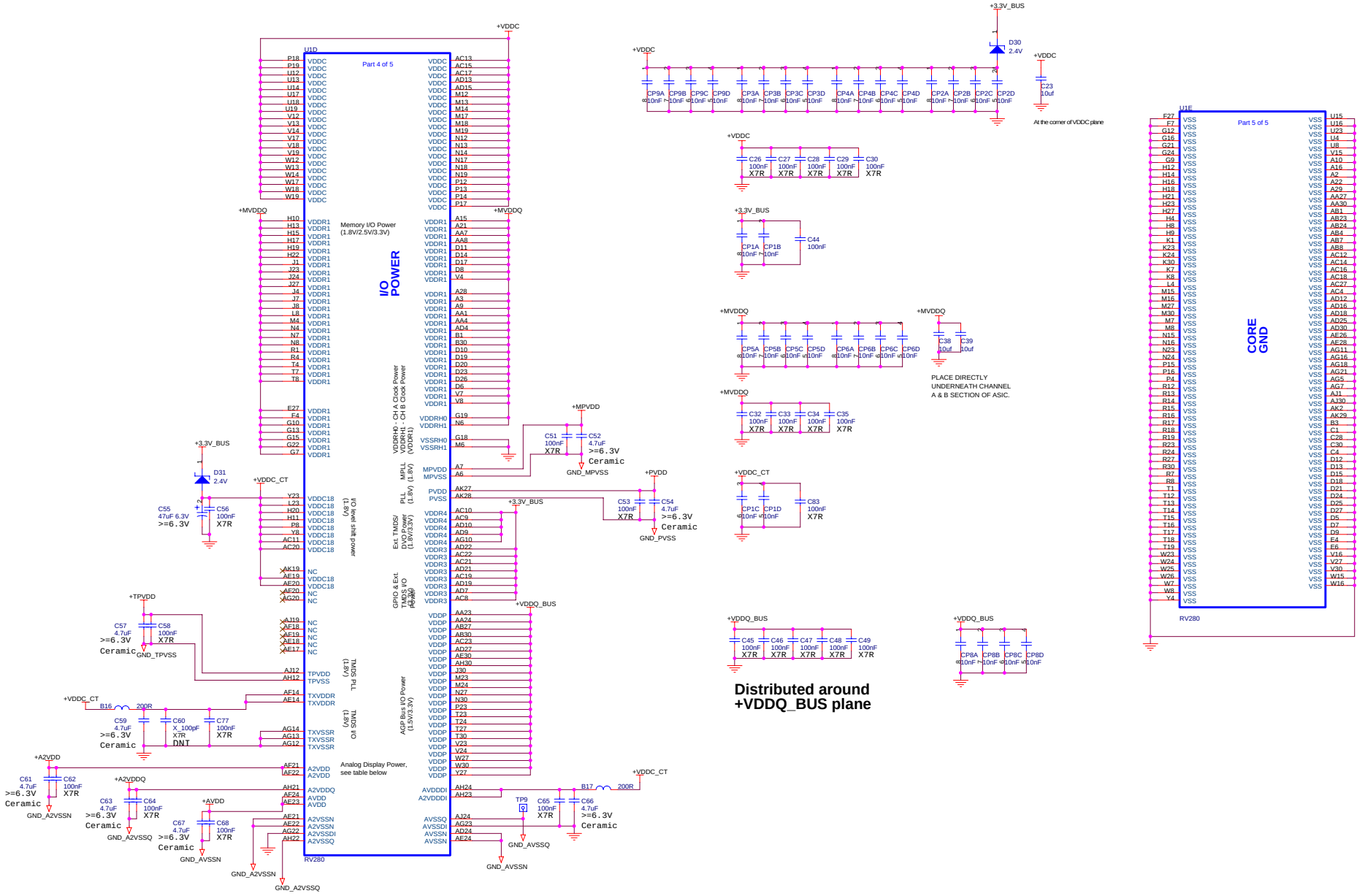


MEMVMODE[1-0]	MEMORY IO VOLTAGE	
0 1	2.5V (DDR)	Default
1 0	1.8V (DDR)	
1 1	3.3V (SDR)	

MS-8916 ATI RV280 9200PRO

Size: Custom | Document Number: **RV280 Mem Interface** | Rev: 0B

Date: Tuesday, February 18, 2003 | Sheet 3 of 17



Pin Names	+AVDD	Matching Ground	+A2VDD	Matching Ground	+A2VDDQ	Matching Ground	+AVDDDI +AZVDDDI	Matching Ground
Voltage	1.8V		2.5V		1.8V		1.8V	
Usage	DAC1 VDD (80mA)	AVSSN (Noisy)	DAC2 VDD (120mA)	A2VSSN (Noisy)	DAC2 Band Gap Ref.	A2VSSQ (Quiet)	Digital Power for DAC1 and DAC2	AVSSDI A2VSSDI (Digital)
	DAC1 Band Gap Ref.	AVSSQ (Quiet)						
Board power and ground option(s)	AVDD sourced from VDDC_CT thru bead at least 15 mil trace and not longer than 1.5 inch. AVSSN and AVSSQ with single via to GND close to the pin.		(1) A2VDD regulated source and A2VSSN return path routed with at least 15 mil trace and not longer than 1.5 inch. AVSSN with single via to GND at the regulator. (2) Sourced from VDD thru bead instead of the regulator		Source from AVDD thru bead. A2VSSQ with sigle via to GND close to the pin.		Source from VDDC_CT thru bead	

MS-8916 ATI RV280 9200PRO			
Size: Custom	Document Number: RV280 Power		Rev: 0B
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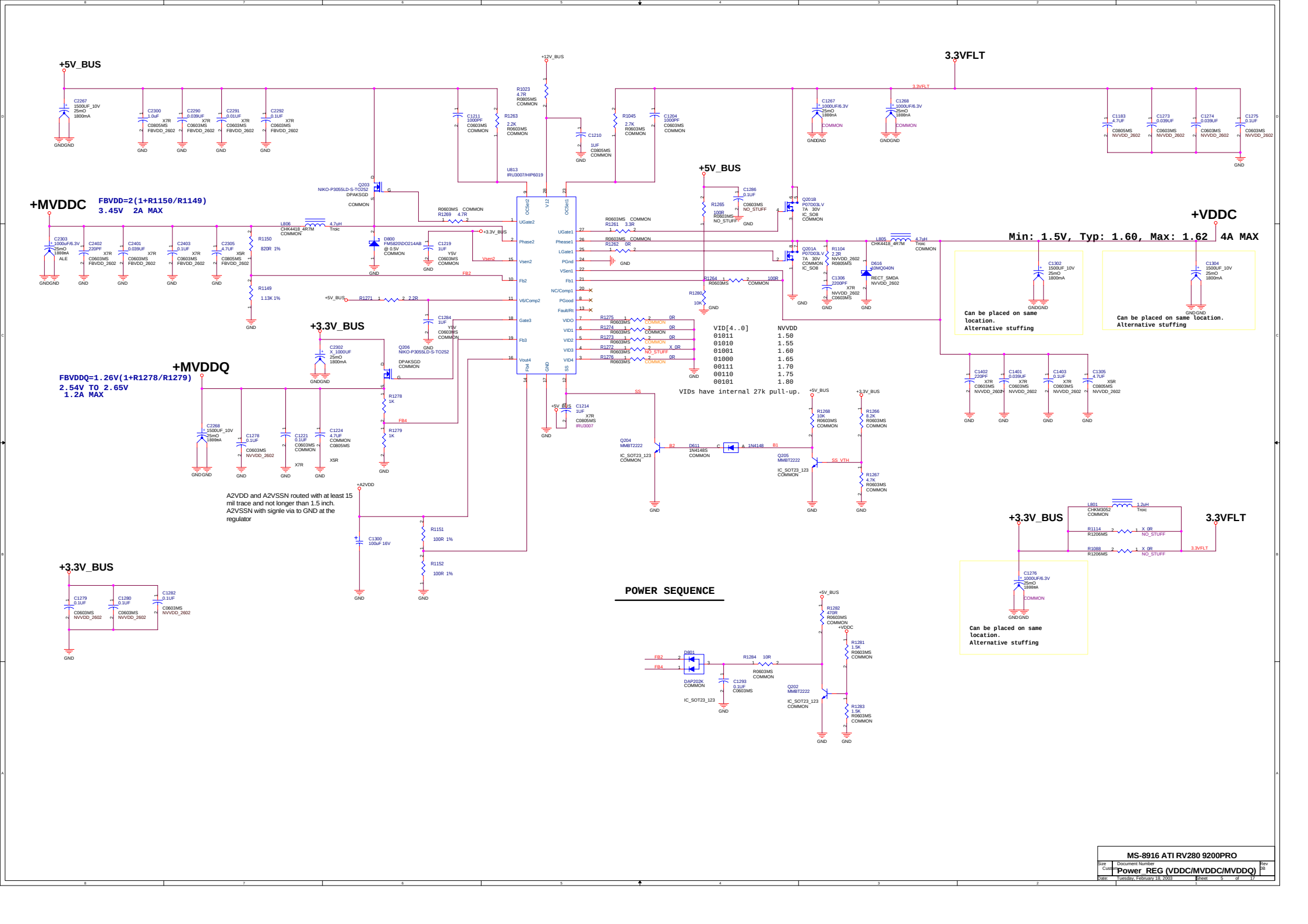
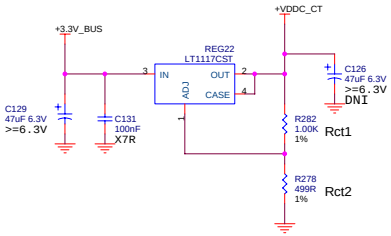

+5V_BUS
+12V_BUS
3.3VFLT
+MVDDC
FBVDD=2(1+R1150/R1149)
3.45V 2A MAX
+MVDDQ
FBVDDQ=1.26V(1+R1278/R1279)
2.54V TO 2.65V
1.2A MAX
+3.3V_BUS
+VDDC
Min: 1.5V, Typ: 1.60, Max: 1.62 4A MAX
VID[4..0] NVVDD
01011 1.50
01010 1.55
01001 1.60
01000 1.65
00111 1.70
00110 1.75
00101 1.80
VIDs have internal 27k pull-up.
A2VDD and A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch. A2VSSN with signle via to GND at the regulator
POWER SEQUENCE
Can be placed on same location. Alternative stuffing
MS-8916 ATI RV280 9200PRO
Power_REG (VDDC/MVDDC/MVDDQ)
Tuesday, February 18, 2003

Regulator for VDDC_CT (Core Transform) and AVDD/A2VDDQ/AVDDDI/A2VDDDI TXVDDR, LVDDRx, MPVDD

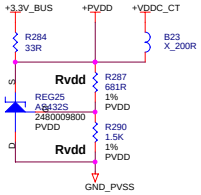
Vin = 3.3V AGP
Vout = 1.8V
Iout = 350mA + 100mA + 50mA = 500mA MAX
Iout = 600mA MAX (with PVDD/TPVDD)

	Rct1			Rct2		
1.8V	1K	3240100100	603	422R	3240422000	603
1.9V				499R	3240499000	603



Regulator for PVDD (Core PLLs) and optional TPVDD (TMDS PLLs)

Vin = 3.3V AGP
Vout = +1.8V
Iout = 25mA MAX (PVDD only)
Iout = 30mA MAX (PVDD + TPVDD)



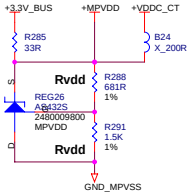
The value of resistor were chosen to reduce failure rate caused by possible defective regulators, i.e., 33R are used instead of 47R or 51R for more start up current. (3.465V - 1.8V) / 33R = 50.5mA

805 package resistor are required for sufficient power rating (0.1W rating). (3.465V - 1.8V) * 50.5mA = 0.085W; therefore, smaller resistor value would require 1206 package

Regulator for MPVDD (Memory PLLs)

Vin = 3.3V AGP
Vout = +1.8V
Iout = 10mA MAX

(Optional)



Regulator For TPVDD (TMDS PLLs)

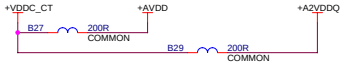
Vin = +3.3V AGP
Vout = 1.8V
Iout = 15mA MAX

TPVDD might not be needed if PVDD can provide stable 1.8V

(Optional)

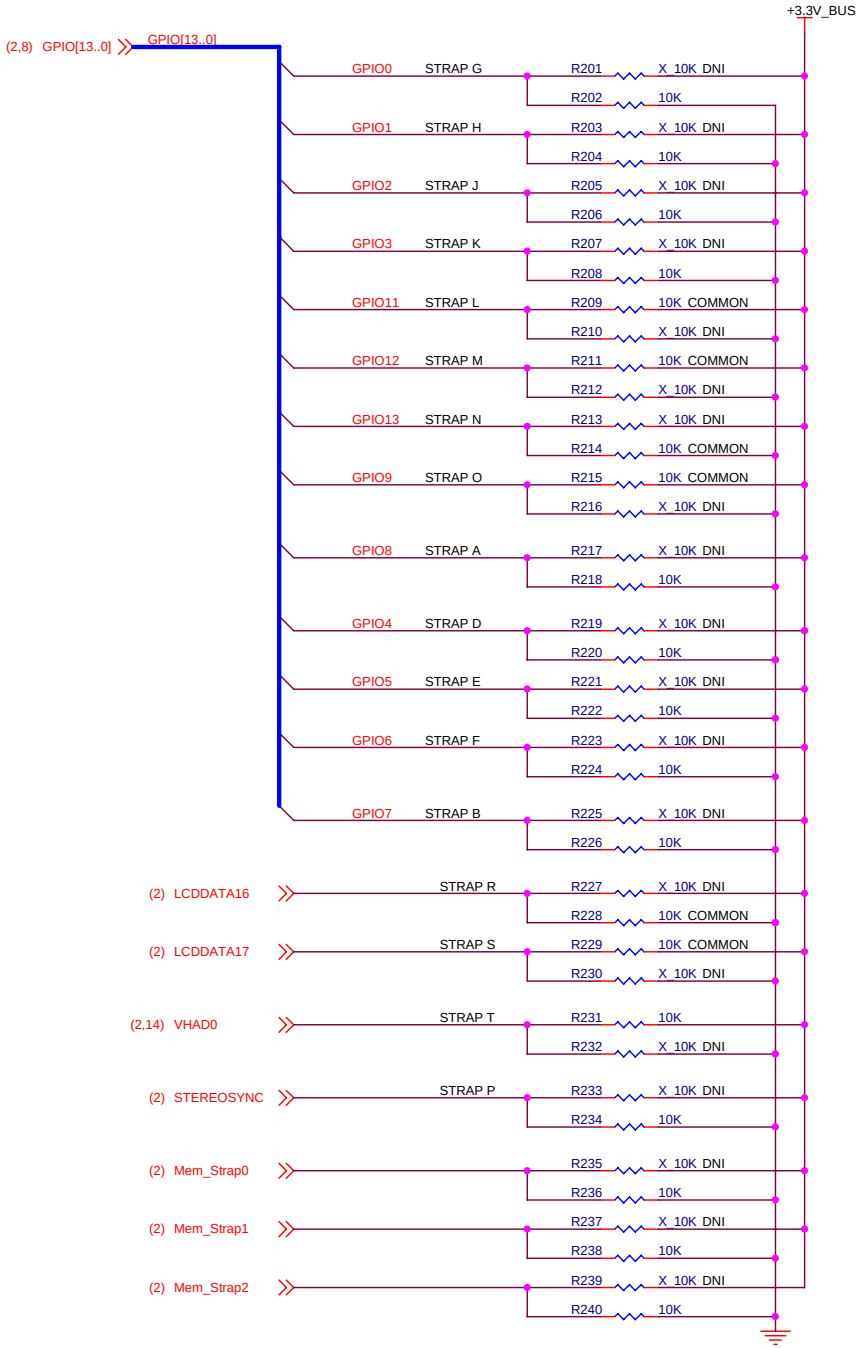
TPVDD = TPVDD + LPVDD + TXVDDR

AVDD/A2VDDQ (1st DAC & 2nd DAC Band Gap)



Some Part Ref's updated to 988 brd

MS-8916 ATI RV280 9200PRO		
Size: Custom	Document Number: Power_REG(VDDC_CT/etc)	Rev: 0B
Date: Tuesday, February 18, 2003	Sheet 6 of 17	



OPTION STRAPS

STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1100
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap. If AGP8X_DETb = 0: (both GC or MB 8x capable) 000 - AGP8x,0.8v signalling,PLL clk, IDSEL=AD16 001 - AGP8x,0.8v signalling,PLL clk, IDSEL=AD17 010 - AGP4x,0.8v signalling,PLL clk, IDSEL=AD16 011 - AGP4x,0.8v signalling,PLL clk, IDSEL=AD17	000 (internal pull-down)
VGA_DISABLE	GPIO(7)	**0 - VGA controller capabillity enabled.** 1 - The device will not be recognized as the systemis VGA controller.	0
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select 00 - single function device. 01 - two function device. No AGP in either function **10 - two function device. AGP only in function 0** 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	10
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. **0 - Slave VIP host port devices present** 1 - No slave VIP host port devices reporting presence during reset	0

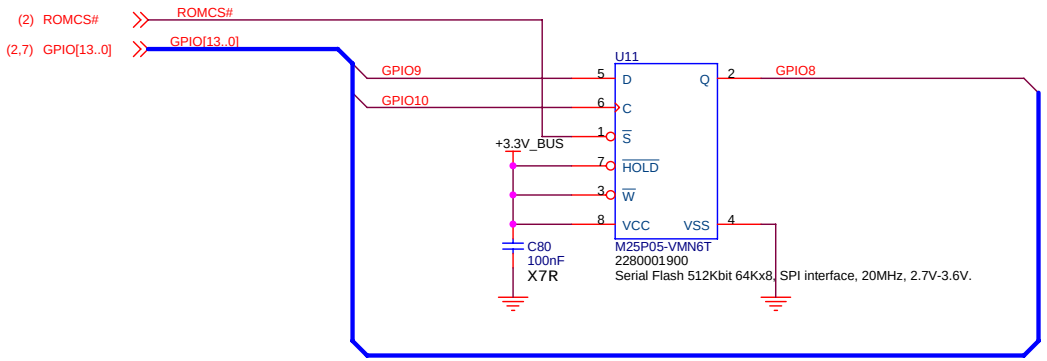
STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MS-8916 ATI RV280 9200PRO

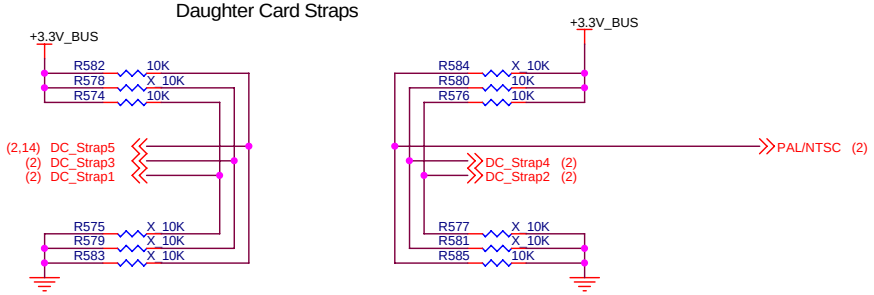
Size	Document Number	Rev
B	**Option Straps**	0B

Date: Tuesday, February 18, 2003 Sheet 7 of 17

SERIAL EEPROM BIOS



Daughter Card Straps



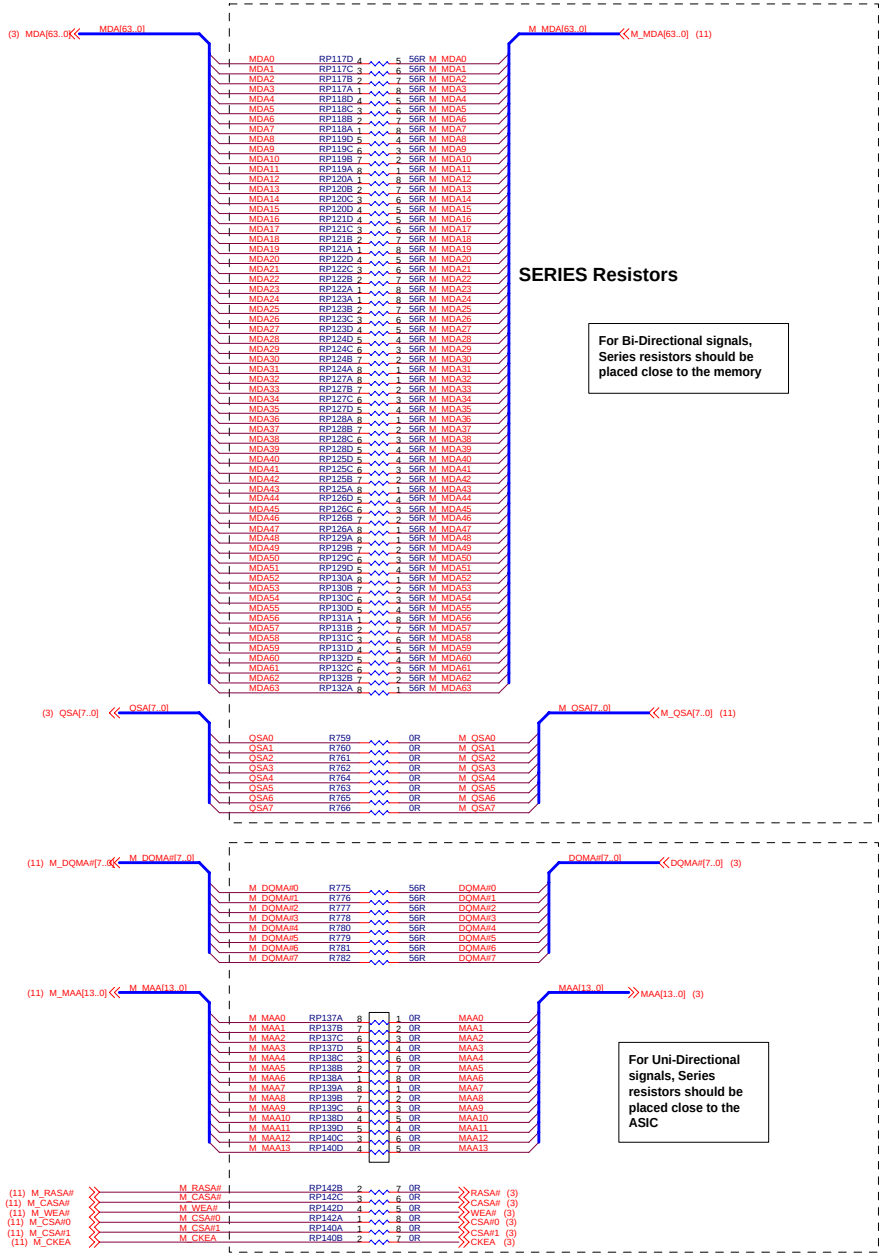
STRAPS	PIN	DESCRIPTION
DC_STRAP1	LCDDATA12	Internal TMDS 0 - Disabled 1 - Enabled
DC_STRAP2	LCDDATA13	Video Capture Enable 0 - Disabled 1 - Enabled
DC_STRAP4 DC_STRAP5	LCDDATA15 LCDDATA19 0 0 0 1 1 0 1 1	DAC2 Configuration DAC2 Off DAC2 On as CRT DAC2 On as TVOUT DAC2 On as TVOUT and CRT
PAL/NTSC	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)

MS-8916 ATI RV280 9200PRO

Size	Document Number	Rev
B	**Serial BIOS & HW Straps**	0B

Date: Tuesday, February 18, 2003 Sheet 8 of 17

TERMINATION FOR MEMORY CHANNEL A



SERIES Resistors

For Bi-Directional signals, Series resistors should be placed close to the memory

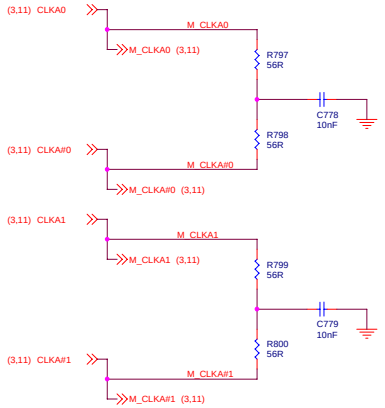
Proper Termination of QSA?

For Uni-Directional signals, Series resistors should be placed close to the ASIC

CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



MS-8916 ATI RV280 9200PRO		
Size: Custom	Document Number: Serial Termination CH A	Rev: 0B
Date: Tuesday, February 18, 2003	Sheet 9 of 17	

TERMINATION FOR MEMORY CHANNEL B

(3) MDB[63..0] → MDB[63..0]

MDB0	RP167A	8	1	56R	M_MDB0
MDB1	RP167B	7	2	56R	M_MDB1
MDB2	RP167C	6	3	56R	M_MDB2
MDB3	RP167D	5	4	56R	M_MDB3
MDB4	RP168A	8	1	56R	M_MDB4
MDB5	RP168B	7	2	56R	M_MDB5
MDB6	RP168C	6	3	56R	M_MDB6
MDB7	RP168D	5	4	56R	M_MDB7
MDB8	RP169D	5	4	56R	M_MDB8
MDB9	RP169C	6	3	56R	M_MDB9
MDB10	RP169B	7	2	56R	M_MDB10
MDB11	RP169A	8	1	56R	M_MDB11
MDB12	RP170A	1	8	56R	M_MDB12
MDB13	RP170B	2	7	56R	M_MDB13
MDB14	RP170C	3	6	56R	M_MDB14
MDB15	RP170D	4	5	56R	M_MDB15
MDB16	RP171A	8	1	56R	M_MDB16
MDB17	RP171B	7	2	56R	M_MDB17
MDB18	RP171C	6	3	56R	M_MDB18
MDB19	RP171D	5	4	56R	M_MDB19
MDB20	RP172A	8	1	56R	M_MDB20
MDB21	RP172B	7	2	56R	M_MDB21
MDB22	RP172C	6	3	56R	M_MDB22
MDB23	RP172D	5	4	56R	M_MDB23
MDB24	RP173A	1	8	56R	M_MDB24
MDB25	RP173B	2	7	56R	M_MDB25
MDB26	RP173C	3	6	56R	M_MDB26
MDB27	RP173D	4	5	56R	M_MDB27
MDB28	RP174D	5	4	56R	M_MDB28
MDB29	RP174C	6	3	56R	M_MDB29
MDB30	RP174B	7	2	56R	M_MDB30
MDB31	RP174A	8	1	56R	M_MDB31
MDB32	RP175D	4	5	56R	M_MDB32
MDB33	RP175C	3	6	56R	M_MDB33
MDB34	RP175B	2	7	56R	M_MDB34
MDB35	RP175A	1	8	56R	M_MDB35
MDB36	RP176D	4	5	56R	M_MDB36
MDB37	RP176C	3	6	56R	M_MDB37
MDB38	RP176B	2	7	56R	M_MDB38
MDB39	RP176A	1	8	56R	M_MDB39
MDB40	RP177A	8	1	56R	M_MDB40
MDB41	RP177B	7	2	56R	M_MDB41
MDB42	RP177C	6	3	56R	M_MDB42
MDB43	RP177D	5	4	56R	M_MDB43
MDB44	RP178D	4	5	56R	M_MDB44
MDB45	RP178C	3	6	56R	M_MDB45
MDB46	RP178B	2	7	56R	M_MDB46
MDB47	RP178A	1	8	56R	M_MDB47
MDB48	RP179D	5	4	56R	M_MDB48
MDB49	RP179C	6	3	56R	M_MDB49
MDB50	RP179B	7	2	56R	M_MDB50
MDB51	RP179A	8	1	56R	M_MDB51
MDB52	RP180D	5	4	56R	M_MDB52
MDB53	RP180C	6	3	56R	M_MDB53
MDB54	RP180B	7	2	56R	M_MDB54
MDB55	RP180A	8	1	56R	M_MDB55
MDB56	RP181D	5	4	56R	M_MDB56
MDB57	RP181C	6	3	56R	M_MDB57
MDB58	RP181B	7	2	56R	M_MDB58
MDB59	RP181A	8	1	56R	M_MDB59
MDB60	RP182A	1	8	56R	M_MDB60
MDB61	RP182B	2	7	56R	M_MDB61
MDB62	RP182C	3	6	56R	M_MDB62
MDB63	RP182D	4	5	56R	M_MDB63

M_MDB[63..0] → M_MDB[63..0] (11)

SERIES Resistors

For Bi-Directional signals, Series resistors should be placed close to the memory

(3) QSB[7..0] → QSB[7..0]

QSB0	R859	0R	M_QSB0	
QSB1	R860	0R	M_QSB1	
QSB2	R861	0R	M_QSB2	
QSB3	R862	0R	M_QSB3	
QSB4	R863	0R	M_QSB4	
QSB5	R864	0R	M_QSB5	
QSB6	R865	0R	M_QSB6	
QSB7	R866	0R	M_QSB7	

M_QSB[7..0] → M_QSB[7..0] (11)

Proper Termination of QSB?

(11) M_DQMB#[7..0] → M_DQMB#[7..0]

M_DQMB#0	R875	56R	DQMB#0
M_DQMB#1	R876	56R	DQMB#1
M_DQMB#2	R877	56R	DQMB#2
M_DQMB#3	R878	56R	DQMB#3
M_DQMB#4	R879	56R	DQMB#4
M_DQMB#5	R880	56R	DQMB#5
M_DQMB#6	R881	56R	DQMB#6
M_DQMB#7	R882	56R	DQMB#7

DQMB#[7..0] → DQMB#[7..0] (3)

(11) M_MAB[13..0] → M_MAB[13..0]

M_MAB0	RP187D	4	5	0R	MAB0
M_MAB1	RP187C	3	6	0R	MAB1
M_MAB2	RP187B	2	7	0R	MAB2
M_MAB3	RP187A	1	8	0R	MAB3
M_MAB4	RP188B	7	2	0R	MAB4
M_MAB5	RP188C	6	3	0R	MAB5
M_MAB6	RP188D	5	4	0R	MAB6
M_MAB7	RP189D	5	4	0R	MAB7
M_MAB8	RP189C	6	3	0R	MAB8
M_MAB9	RP189B	7	2	0R	MAB9
M_MAB10	RP188A	8	1	0R	MAB10
M_MAB11	RP189A	8	1	0R	MAB11
M_MAB12	RP190C	3	6	0R	MAB12
M_MAB13	RP190D	4	5	0R	MAB13

MAB[13..0] → MAB[13..0] (3)

For Uni-Directional signals, Series resistors should be placed close to the ASIC

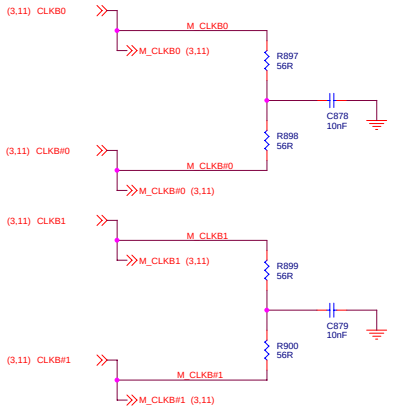
(11) M_RASB#	M_RASB#	RP192C	6	3	0R
(11) M_CASB#	M_CASB#	RP192B	7	2	0R
(11) M_WEB#	M_WEB#	RP192A	8	1	0R
(11) M_CSB#0	M_CSB#0	RP192D	5	4	0R
(11) M_CSB#1	M_CSB#1	RP190A	1	8	0R
(11) M_CKEB	M_CKEB	RP190B	2	7	0R

RASB# (3), CASB# (3), WEB# (3), CSB#0 (3), CSB#1 (3), CKEB (3)

CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

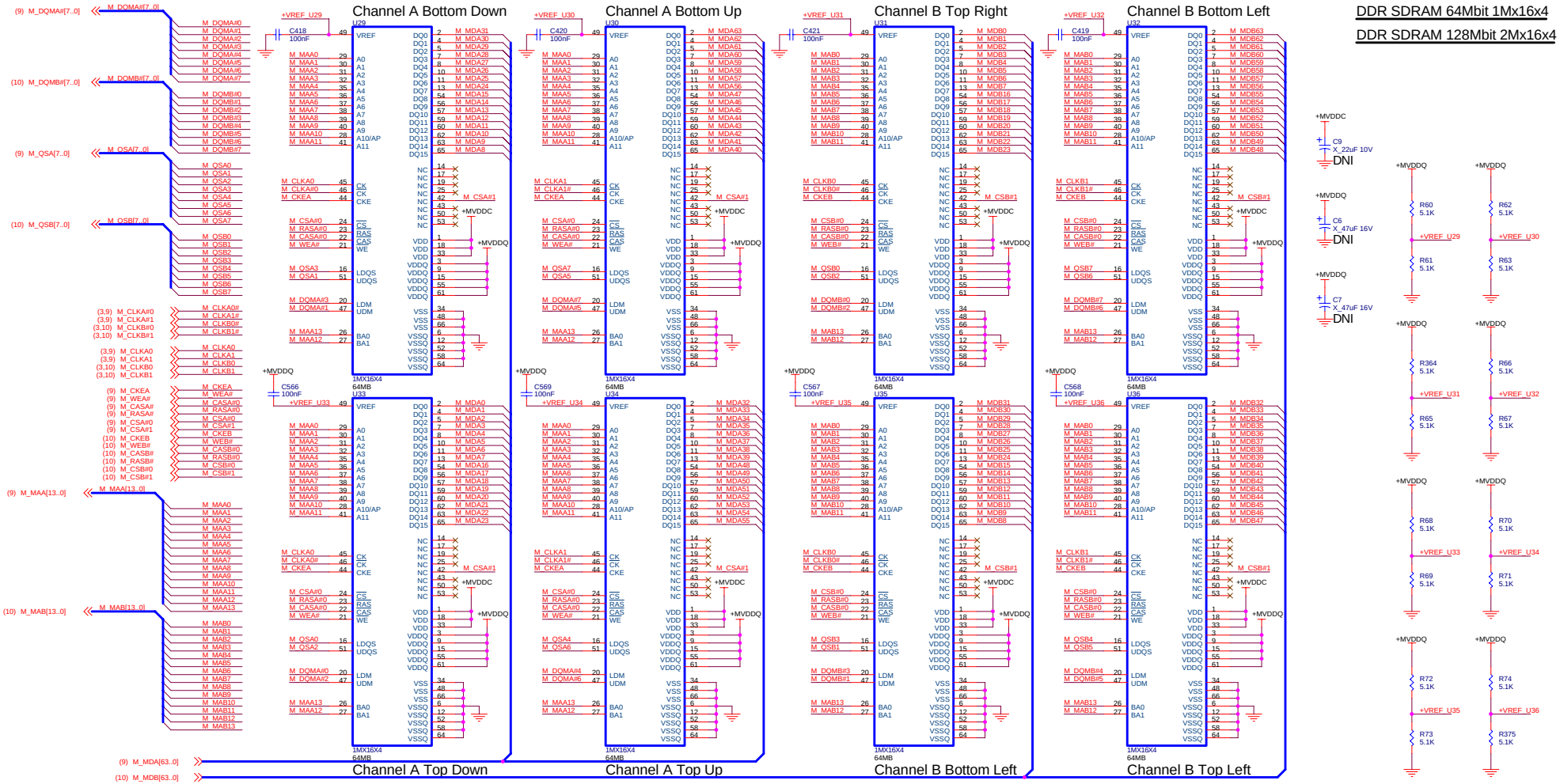
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



MS-8916 ATI RV280 9200PRO

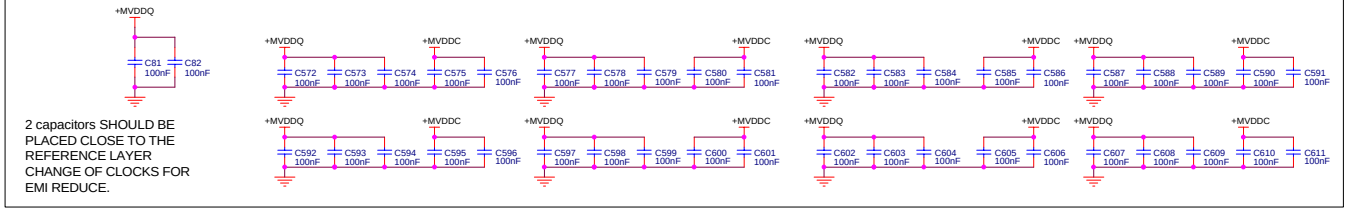
Size	Document Number	Rev
C	Serial Termination CH B	0B

Date: Tuesday, February 18, 2003 Sheet 10 of 17



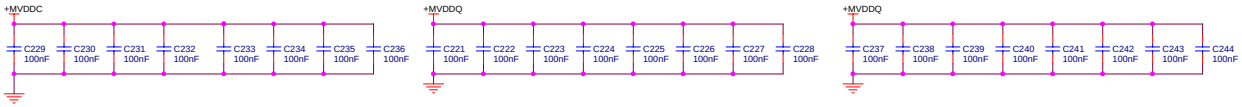
Note: These indications of the location of the memory for the solder side (bottom) are looking thru from the component side.

Put 1 1uF cap per power pin of memory



2 capacitors SHOULD BE PLACED CLOSE TO THE REFERENCE LAYER CHANGE OF CLOCKS FOR EMI REDUCE.

Place as many as possible.



Part number for 8Mx16: 2354274204 (Samsung)

DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

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Size C	Document Number TSOP 4/8x16 DDR	Rev 0B
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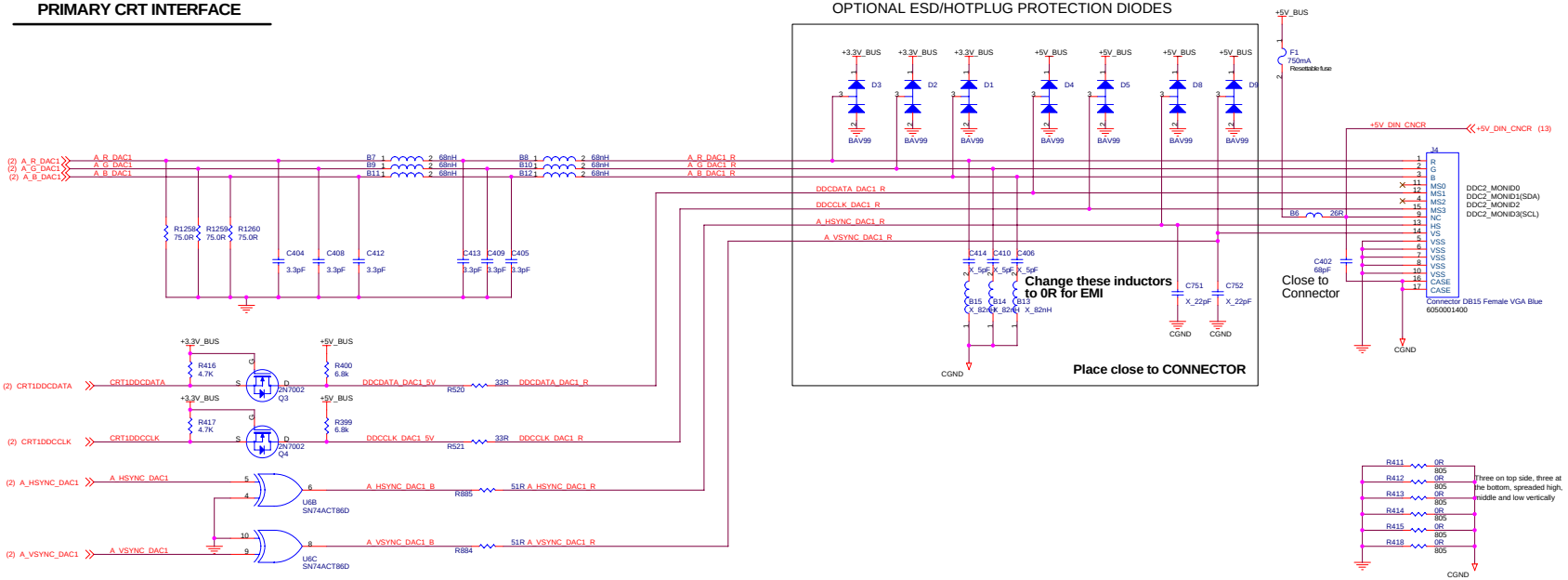
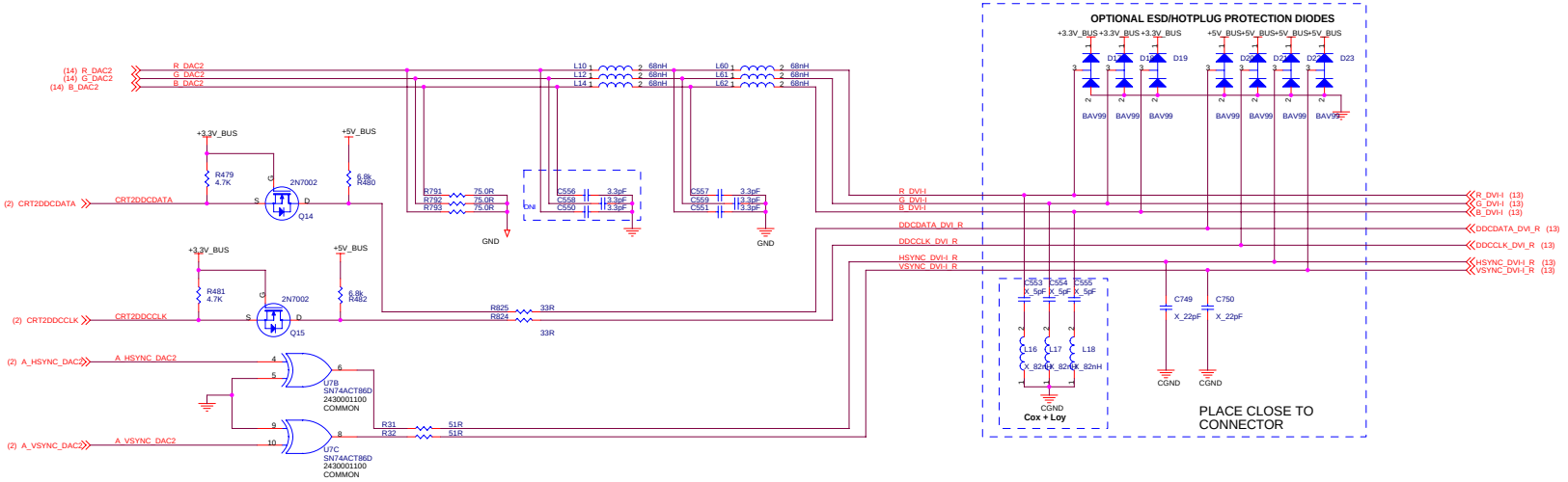
PRIMARY CRT INTERFACE



SECONDARY CRT INTERFACE



MS-8916 ATI RV280 9200PRO	
Size: Custom	Document Number: DAC RGB Filters
Rev: 1B	
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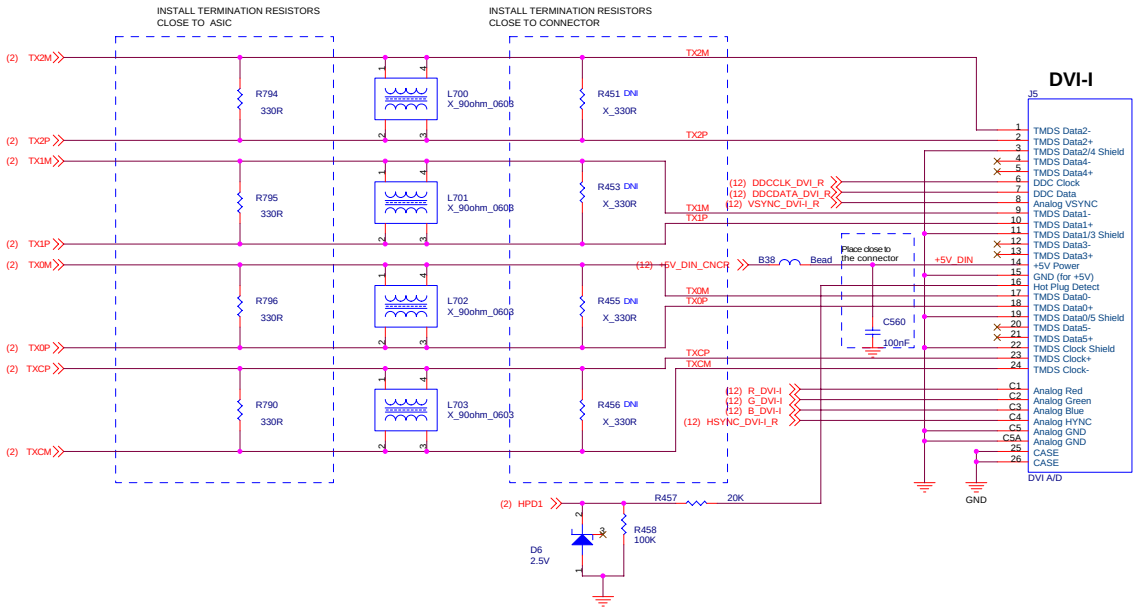
PRIMARY DVI-I CONNECTOR (DVI-I)



MS-8916 ATI RV280 9200PRO		
Size: Custom	Document Number: DVI-I Display	Rev: 0A
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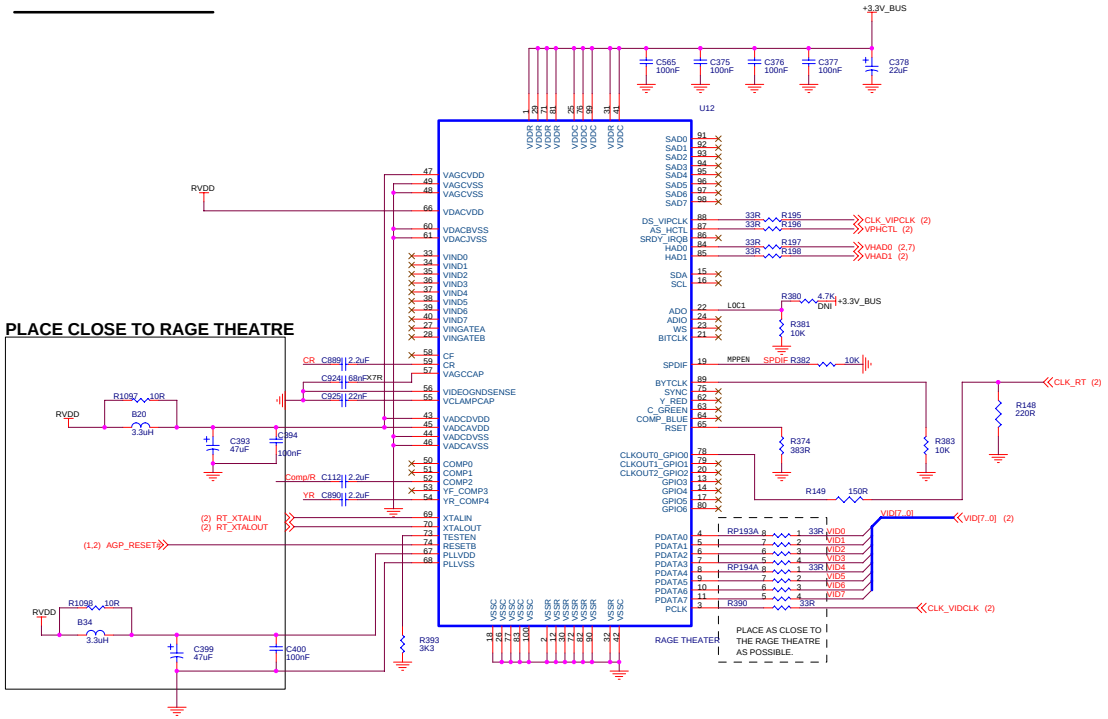
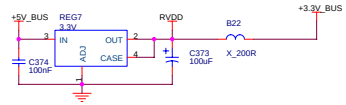
THEATER & TV-OUT

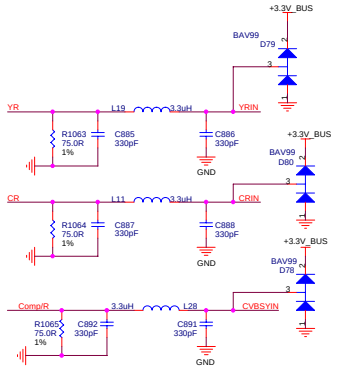
PLACE CLOSE TO RAGE THEATRE



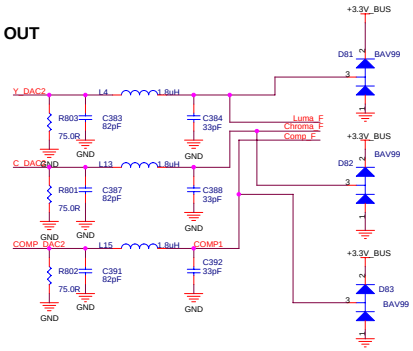
Regulator for RVDD



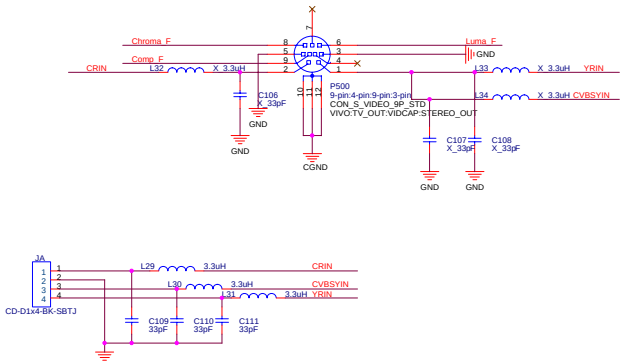
VIDEO IN



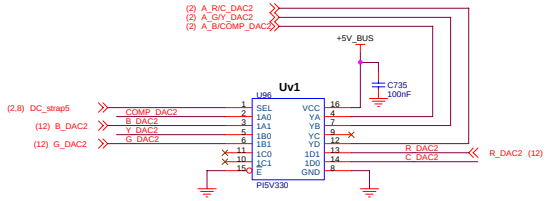
TV OUT



VIVO CONNECTOR



DEMUX



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Custom	Theater & TV-OUT	0B
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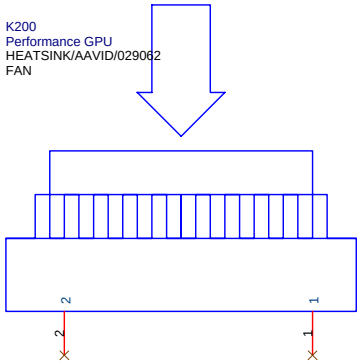
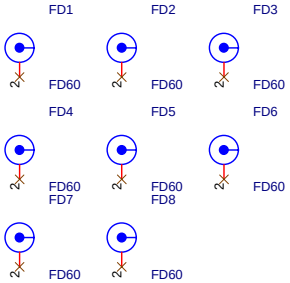
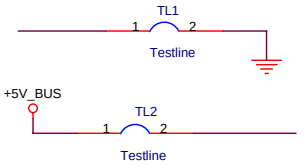
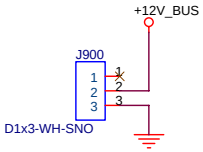
Heatsink









ASSY1
SCREW
JACKSCREW
{3rd part field}
7020000800

ASSY2
SCREW
JACKSCREW
{3rd part field}
7020000800

ASSY4
SCREW
JACKSCREW
{3rd part field}
7020000800

ASSY5
SCREW
JACKSCREW
{3rd part field}
7020000800

MS-8916 ATI RV280 9200PRO		
Size B	Document Number **Heatsink & Mechanicals**	Rev 0A
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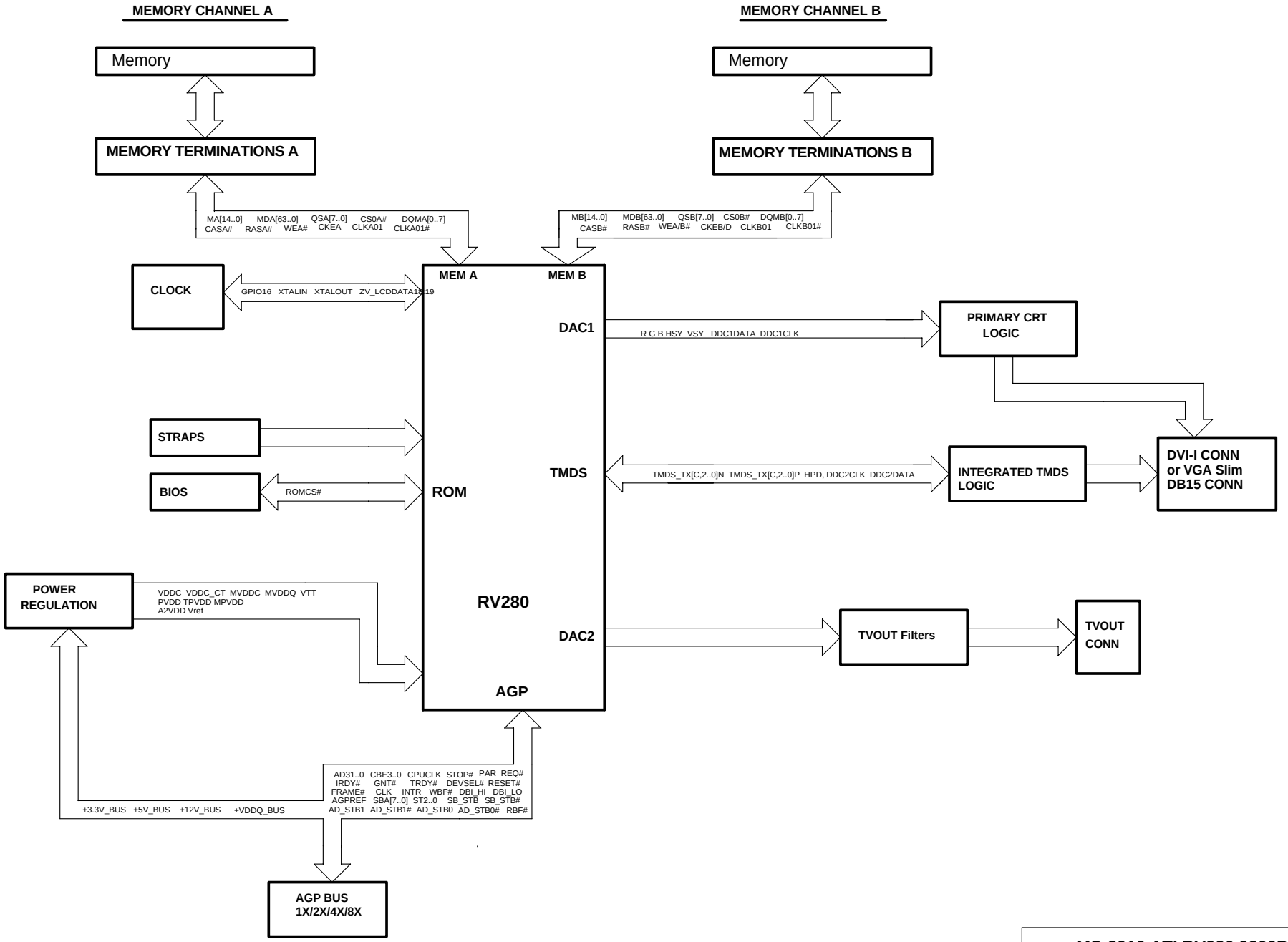

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Size	Document Number	Rev
B	Block Diagram	0B

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{Variant Name}

Title	Schematic No.	Date:
RV280 AGP8x 32/64/128MB 4/8x16 DDR	Rev Hishory	**Monday, February 17, 2003**

REVISION HISTORY

Rev 0B

Sch Rev	Date	REVISION DESCRIPTION
0	09/21/02	PRELIMINARY based on RV250 REFERENCE REF109 Schematic and RV250 BGA 958 Schematic
0.1	09/23/02	PRELIMINARY based on the RV280 REFERENCE REF 105-REF112-00A
	09/24/02	Copied from 09/24/02 version 0 of 105-ref112-00a RV280 Reference Design - pg1 Add AGP8X cold boot pull-ups - pg9,10 Move DQM Memory Termination Resistor close to ASIC
	09/25/02	Ready for design review. open issues listed below.
	09/25/02	John Digweed updated the ASIC to 215R78ANA11H
	9/27/02	MVDD circuit changed to linear, based on 988 brd.
	10/01/02	QSMA4/5 corrected. - (pg 1) Rearrange XOR gates, eliminate single AND gate - (pg 1) Rename AGP_AD_STB1# to AGP_AGPREF (cold boot fix) - (pg 6) Remove A2VDD option from +MVDDQ - (pg 7) Add resistor to disable microswitch
	10/03/02	Branch from filename 105-A06200-00A netlisted_1002, renamed part refs to match 105-988000-00A
	10/04/02	- (pg 1) Add TXVSSR ground symbol connected to digital GND - (pg 1) Change VDDQ_BUS cap to 47uF tant - (pg 1) Remove VREFGC fixed resistor/capacitor circuit, change R91 to 1K - (pg 1) Change value of C76 capacitor (AGP_AGPREF) - (pg 4) Replace 1uF cap on TXVDDR to 100pF and 100nF X7R caps - (pg 4) Replace 10uF cap on A2VDD to 22uF electrolitic or 10uF tantalum cap - (pg 4) Add 10nF capacitor arrray on +VDDQ_BUS - (pg 5) Update VDDC Alt1 regulator circuits - (pg 14) Change 0R for chassis and digital ground to 805 resistors - (pg 1) Removed AGP 8x Cool Boot Fix - (pg 1) Removed Q8, R87 for AGP_REFCG
	10/07/02	- (pg 1) C2, C5, C8 changed to 100 uF Alu Elec for cost savings. (p/n 4260110700) - (pg 11) C281-286 changed to 22uF Alu Elec for cost savings. (p/n 4260022600) Layout Begins EASY BOM created
	10/08/02	- (pg.6) MPVDD regulator removed. Derived from VDD_CT through B24. (moved to pg.4) - (pg.11) Reduced decoupling capacitors C221..C280 to C221..236 and changed value to 100 nF. (Layout cannot fit all) - (pg.4) Updated caps (add/remove) according to layout efforts on A058
	10/08/02	- (pg.4) Added C83 to +VDDC_CT
	10/09/02	- (pg.9/10) Rearranged Resistor Packs to facilitate layout
	10/10/02	- (pg.1) U4 added to replace U6D gate. Facilitates layout. - (pg. 6) MPVDD regulator added back. Should be DNI - (pg.9/10) Rpacks changed from 22R to 56R - (pg.12) Slim VGA changed to regular. DVI-i circuit removed.
	10/11/02	- (pg.10) RPacks 167 to 174 flipped L-R (pin 1-8, 2-7, 3-6, 4-5) - (pg.11) Bytes swapped on Channel B data bus and M_QSB, M_DQMB. M_MDB[0:7] <=> M_MDB_[8:15], M_MDB[16:23] <=> M_MDB[24:31] - (pg.1) Fixed short between 5VBus and AGP_MB_8X_DET#
	10/15/02	- (pg.9,10) RPacks 126, 188, 189 pins moved for layout. - (pg. 13) J8 RCA connector added for footprint, to overlap with Svideo
	10/16/02	- (pg.11) added C237-C244 on MVDDQ
	10/18/02	- (pg.1) added R84, R85 to comply with AGP 3.0 Spec Rev 1.0, AGPVref provision - (pg.11) added C6, C7, C9 on MVDDQ and MVDDC
1	11/15/02	- (pg. 1) Remove AGP series resistors - (pg. 1) Add AGPVREFCG circuit isolated from AGPVREFGC - Change all 1.0uF Y5V caps to 100nF X7R caps - Remove R34, C74, C75 - Change C20 footprint to 805 - Change C2, C5, C8, C52, C54, C55, C57, C59, C61, C63, C66, C67, C126, C130, C1035 footprint - Layout: Move R265 and R268 close to the ASIC ball