P2132-A01

NVG GK208 DDR3 64BIT
DVI-I/DVI-D + HDMI + VGA

VerA1: add ESD

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
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NV_PN	600-12132-BASE-QS1		
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A

PCI EXPRESS

12V_PEX
C61 10UF 16V 10% X5R 1206 COMMON
C62 0.1UF 16V 10% X7R 0402 COMMON
GND
3V3_PEX
C76 4.7UF 6.3V 20% X5R 0603 COMMON
GND
CLOSE TO CONNECTOR
NO STUFF DEFAULT

12V_PEX TRUE 5.5A 0.66M 12V
3V3_PEX TRUE 3A 0.46M 3.3V

CN1
CON_FINGER_PEX_124
CON_X16
DN

B1 +12V
B2 +12V
A2 +12V
A3 +12V
B3 +12V/RSVD
B8 +3V3
A9 +3V3
A10 +3V3
SNN_3V3AUX_AUX B10 +3V3AUX
PEX_PRSNT* A1 PRSNT1
B81 PRSNT2

B4 A4 B7 A12 B13 A15 B16 B18 A18 GND
A20 B22 A24 B26 A28 B29 A31 B32 GND
END OF X1
END OF X4
A34 B36 A38 B40 A42 B44 A46 B47 B49 A49 GND
END OF X8
A51 B53 A54 B56 A58 B60 A62 B64 A66 B68 A70 B72 A74 B76 A78 B80 A82 GND
END OF X16

SMCLK B5 PEX_SMCLK
SMDAT B6 PEX_SMDAT
R110 0 0402 +0.05R COMMON
R103 0 0402 +0.05R COMMON
I2CS_SCL
I2CS_SDA
OUT IN 10

0.1uF for PEX Gen2 default

PERST A11 PEX_RST*

REFCLK	A13	PEX_REFCLK	NET_NAME	DIFF_PAIR	NV_NETCLASS					NV_NETCLASS	DIFF_PAIR	NET_NAME	
REFCLK	A14		PEX_REFCLK	PEXGEN3_SIGNALS									
PERP0	A16		PEX_TX0	PEXGEN3_SIGNALS	0402 16V C134 0.1UF 10% X7R 0402 COMMON					PEXGEN3_SIGNALS	PEX_TX0	PEX_TX0	PEX_TX0
PERN0	A17									PEXGEN3_SIGNALS	PEX_TX0	PEX_TX0*	PEX_TX0
PETP0	B14		PEX_RX0	PEXGEN3_SIGNALS									PEX_RX0
PETN0	B15	PEX_RX0*	PEX_RX0	PEXGEN3_SIGNALS									PEX_RX0
PERP1	A21				0402 16V C139 0.1UF 10% X7R 0402 COMMON					PEXGEN3_SIGNALS	PEX_TX1	PEX_TX1	PEX_TX1
PERN1	A22		PEX_TX01							PEXGEN3_SIGNALS	PEX_TX1	PEX_TX1*	PEX_TX1
PETP1	B19		PEX_RX1	PEXGEN3_SIGNALS									PEX_RX1
PETN1	B20		PEX_RX1	PEXGEN3_SIGNALS									PEX_RX1
PERP2	A25				0402 16V C147 0.1UF 10% X7R 0402 COMMON					PEXGEN3_SIGNALS	PEX_TX2	PEX_TX2	PEX_TX2
PERN2	A26		PEX_TX02							PEXGEN3_SIGNALS	PEX_TX2	PEX_TX2*	PEX_TX2
PETP2	B23		PEX_RX2	PEXGEN3_SIGNALS									PEX_RX2
PETN2	B24		PEX_RX2	PEXGEN3_SIGNALS									PEX_RX2
PERP3	A29				0402 16V C150 0.1UF 10% X7R 0402 COMMON					PEXGEN3_SIGNALS	PEX_TX3	PEX_TX3	PEX_TX3
PERN3	A30									PEXGEN3_SIGNALS	PEX_TX3	PEX_TX3*	PEX_TX3
PETP3	B27		PEX_RX3	PEXGEN3_SIGNALS									PEX_RX3
PETN3	B28		PEX_RX3	PEXGEN3_SIGNALS									PEX_RX3
PERP4	A35				0402 16V C162 0.1UF 10% X7R 0402 COMMON					PEXGEN3_SIGNALS	PEX_TX4	PEX_TX4	PEX_TX4
PERN4	A36									PEXGEN3_SIGNALS	PEX_TX4	PEX_TX4*	PEX_TX4
PETP4	B33		PEX_RX4	PEXGEN3_SIGNALS									PEX_RX4
PETN4	B34		PEX_RX4	PEXGEN3_SIGNALS									PEX_RX4
PERP5	A39				0402 16V C167 0.1UF 10% X7R 0402 COMMON					PEXGEN3_SIGNALS	PEX_TX5	PEX_TX5	PEX_TX5
PERN5	A40									PEXGEN3_SIGNALS	PEX_TX5	PEX_TX5*	PEX_TX5
PETP5	B37		PEX_RX5	PEXGEN3_SIGNALS									PEX_RX5
PETN5	B38		PEX_RX5	PEXGEN3_SIGNALS									PEX_RX5
PERP6	A43				0402 16V C169 0.1UF 10% X7R 0402 COMMON					PEXGEN3_SIGNALS	PEX_TX6	PEX_TX6	PEX_TX6
PERN6	A44									PEXGEN3_SIGNALS	PEX_TX6	PEX_TX6*	PEX_TX6
PETP6	B41		PEX_RX6	PEXGEN3_SIGNALS									PEX_RX6
PETN6	B42		PEX_RX6	PEXGEN3_SIGNALS									PEX_RX6
PERP7	A47				0402 16V C175 0.1UF 10% X7R 0402 COMMON					PEXGEN3_SIGNALS	PEX_TX7	PEX_TX7	PEX_TX7
PERN7	A48									PEXGEN3_SIGNALS	PEX_TX7	PEX_TX7*	PEX_TX7
PETP7	B45		PEX_RX7	PEXGEN3_SIGNALS									PEX_RX7
PETN7	B46		PEX_RX7	PEXGEN3_SIGNALS									PEX_RX7
PERP8	A52											SNN_PEX_TX8	PEX_TX8
PERN8	A53											SNN_PEX_TX8*	PEX_TX8
PETP8	B50											SNN_PEX_RX8	PEX_RX8
PETN8	B51											SNN_PEX_RX8*	PEX_RX8
PERP9	A56											SNN_PEX_TX9	PEX_TX9
PERN9	A57											SNN_PEX_TX9*	PEX_TX9
PETP9	B54											SNN_PEX_RX9	PEX_RX9
PETN9	B55											SNN_PEX_RX9*	PEX_RX9
PERP10	A60											SNN_PEX_TX10	PEX_TX10
PERN10	A61											SNN_PEX_TX10*	PEX_TX10
PETP10	B58											SNN_PEX_RX10	PEX_RX10
PETN10	B59											SNN_PEX_RX10*	PEX_RX10
PERP11	A64											SNN_PEX_TX11	PEX_TX11
PERN11	A65											SNN_PEX_TX11*	PEX_TX11
PETP11	B62											SNN_PEX_RX11	PEX_RX11
PETN11	B63											SNN_PEX_RX11*	PEX_RX11
PERP12	A68											SNN_PEX_TX12	PEX_TX12
PERN12	A69											SNN_PEX_TX12*	PEX_TX12
PETP12	B66											SNN_PEX_RX12	PEX_RX12
PETN12	B67											SNN_PEX_RX12*	PEX_RX12
PERP13	A72											SNN_PEX_TX13	PEX_TX13
PERN13	A73											SNN_PEX_TX13*	PEX_TX13
PETP13	B70											SNN_PEX_RX13	PEX_RX13
PETN13	B71											SNN_PEX_RX13*	PEX_RX13
PERP14	A76											SNN_PEX_TX14	PEX_TX14
PERN14	A77											SNN_PEX_TX14*	PEX_TX14
PETP14	B74											SNN_PEX_RX14	PEX_RX14
PETN14	B75											SNN_PEX_RX14*	PEX_RX14
PERP15	A80											SNN_PEX_TX15	PEX_TX15
PERN15	A81											SNN_PEX_TX15*	PEX_TX15
PETP15	B78											SNN_PEX_RX15	PEX_RX15
PETN15	B79											SNN_PEX_RX15*	PEX_RX15

G1A
BGA_0595_P080_P084_P085_P090_P100_230X230
COMMON
1/14 PCI_EXPRESS

	GK208/GF117/GF119
PEX_WAKE	NC

SNN_PEX_WAKE_R* AB6 PEX_WAKE
AC7 PEX_RST
SNN_PEX_CLKREQ* AC6 PEX_CLKREQ
AE8 PEX_REFCLK
AD8 PEX_REFCLK*
AC9 PEX_TX0
AB9 PEX_TX0*
AG6 PEX_RX0
AG7 PEX_RX0*
AB10 PEX_TX1
AC10 PEX_TX1*
AF7 PEX_RX1
AE7 PEX_RX1*
AD11 PEX_TX2
AC11 PEX_TX2*
AE9 PEX_RX2
AF9 PEX_RX2*
AC12 PEX_TX3
AB12 PEX_TX3*
AG9 PEX_RX3
AG10 PEX_RX3*
AB13 PEX_TX4
AC13 PEX_TX4*
AF10 PEX_RX4
AE10 PEX_RX4*
AD14 PEX_TX5
AC14 PEX_TX5*
AE12 PEX_RX5
AF12 PEX_RX5*
AC15 PEX_TX6
AB15 PEX_TX6*
AG12 PEX_RX6
AG13 PEX_RX6*
AB16 PEX_TX7
AC16 PEX_TX7*
AF13 PEX_RX7
AF13 PEX_RX7*

SNN_PEX_TX8 / SNN_PEX_TX8*	AD17 / AC17	PEX_TX8 / PEX_TX8*
SNN_PEX_RX8 / SNN_PEX_RX8*	AE15 / AF15	PEX_RX8 / PEX_RX8*
SNN_PEX_TX9 / SNN_PEX_TX9*	AC18 / AB18	PEX_TX9 / PEX_TX9*
SNN_PEX_RX9 / SNN_PEX_RX9*	AG15 / AG16	PEX_RX9 / PEX_RX9*
SNN_PEX_TX10 / SNN_PEX_TX10*	AB19 / AC19	PEX_TX10 / PEX_TX10*
SNN_PEX_RX10 / SNN_PEX_RX10*	AF16 / AE16	PEX_RX10 / PEX_RX10*
SNN_PEX_TX11 / SNN_PEX_TX11*	AD20 / AC20	PEX_TX11 / PEX_TX11*
SNN_PEX_RX11 / SNN_PEX_RX11*	AE18 / AF18	PEX_RX11 / PEX_RX11*
SNN_PEX_TX12 / SNN_PEX_TX12*	AC21 / AB21	PEX_TX12 / PEX_TX12*
SNN_PEX_RX12 / SNN_PEX_RX12*	AG18 / AG19	PEX_RX12 / PEX_RX12*
SNN_PEX_TX13 / SNN_PEX_TX13*	AD23 / AE23	PEX_TX13 / PEX_TX13*
SNN_PEX_RX13 / SNN_PEX_RX13*	AF19 / AE19	PEX_RX13 / PEX_RX13*
SNN_PEX_TX14 / SNN_PEX_TX14*	AF24 / AE24	PEX_TX14 / PEX_TX14*
SNN_PEX_RX14 / SNN_PEX_RX14*	AE21 / AF21	PEX_RX14 / PEX_RX14*
SNN_PEX_TX15 / SNN_PEX_TX15*	AG24 / AG25	PEX_TX15 / PEX_TX15*
SNN_PEX_RX15 / SNN_PEX_RX15*	AG21 / AG22	PEX_RX15 / PEX_RX15*

GF119	GF117
	GK208

PEX_IOVDD AA22 AB23 AC24 AD25 AE26 AE27
PEX_IOVDDQ AA10 AA12 AA13 AA16 AA18 AA19 AA20 AA21 AB22 AC23 AD24 AE25 AF26 AF27
1530mA GK208
C171 1UF 6.3V 10% X5R 0402 COMMON
C170 1UF 6.3V 10% X5R 0402 COMMON
C131 4.7UF 6.3V 20% X5R 0603 COMMON
C128 10UF 6.3V 20% X5R 0805 COMMON
C132 1UF 6.3V 10% X5R 0402 COMMON
C165 1UF 6.3V 10% X5R 0402 COMMON
C164 4.7UF 6.3V 20% X5R 0603 COMMON
C173 10UF 6.3V 20% X5R 0805 COMMON
PLACE CLOSE TO GPU
PEX_VDD
C163 22UF 6.3V 20% X5R 0805 COMMON
C172 22UF 6.3V 20% X5R 0805 COMMON
C129 22UF 6.3V 20% X5R 0805 COMMON
C130 22UF 6.3V 20% X5R 0805 COMMON
OPTION
GND

PEX_PLL_HVDD AA8 AA9
PEX_SVDD_3V3 AB8
3V3_PLL
0.189 Amps GK208

VDD_SENSE F2 NVVDD_SENSE OUT 14
GND_SENSE F1 SNN_GND_SENSE

PEX_TSTCLK_OUT AF22 SNN_PEX_TSTCLK_OUT
PEX_TSTCLK_OUT AE22 SNN_PEX_TSTCLK_OUT*
PEX_PLLVDD 1.05V 0.130 Amps GK208
PEX_PLLVDD AA14 AA15
R147 0 0603 +0.05R COMMON
C161 0.1UF 16V 10% X7R 0402 COMMON
C159 1UF 6.3V 10% X5R 0402 COMMON
C157 4.7UF 6.3V 20% X5R 0603 COMMON
C158 10UF 6.3V 20% X5R 0805 COMMON
PLACE CLOSE TO GPU

TESTMODE AD9 GPU_TESTMODE
R139 10K 0402 5% COMMON
PEX_TERMP AF25 PEX_TERMP
R152 2.49K 0402 1% COMMON
GND

GPU FRAME BUFFER: PARTITION A

G1B

BGA_0595_P080_P084_P085_P090_P100_230X230
COMMON

2/14 FBA

NC	FB_CLAMP
GF119	GF117/GK208

F3 FB_CLAMP — R130 10K 5% 0402 COMMON — GND

NV_NETCLASS FB_DATA

FBA_D[63..0] (III)

FBA_D0	E18	FBA_D0
FBA_D1	F18	FBA_D1
FBA_D2	E16	FBA_D2
FBA_D3	F17	FBA_D3
FBA_D4	D20	FBA_D4
FBA_D5	D21	FBA_D5
FBA_D6	F20	FBA_D6
FBA_D7	E21	FBA_D7
FBA_D8	E15	FBA_D8
FBA_D9	D15	FBA_D9
FBA_D10	F15	FBA_D10
FBA_D11	F13	FBA_D11
FBA_D12	C13	FBA_D12
FBA_D13	B13	FBA_D13
FBA_D14	E13	FBA_D14
FBA_D15	D13	FBA_D15
FBA_D16	B15	FBA_D16
FBA_D17	C16	FBA_D17
FBA_D18	A13	FBA_D18
FBA_D19	A15	FBA_D19
FBA_D20	B18	FBA_D20
FBA_D21	A18	FBA_D21
FBA_D22	A19	FBA_D22
FBA_D23	C19	FBA_D23
FBA_D24	B24	FBA_D24
FBA_D25	C23	FBA_D25
FBA_D26	A25	FBA_D26
FBA_D27	A24	FBA_D27
FBA_D28	A21	FBA_D28
FBA_D29	B21	FBA_D29
FBA_D30	C20	FBA_D30
FBA_D31	C21	FBA_D31
FBA_D32	R22	FBA_D32
FBA_D33	R24	FBA_D33
FBA_D34	T22	FBA_D34
FBA_D35	R23	FBA_D35
FBA_D36	N25	FBA_D36
FBA_D37	N26	FBA_D37
FBA_D38	N23	FBA_D38
FBA_D39	N24	FBA_D39
FBA_D40	V23	FBA_D40
FBA_D41	V22	FBA_D41
FBA_D42	T23	FBA_D42
FBA_D43	U22	FBA_D43
FBA_D44	Y24	FBA_D44
FBA_D45	AA24	FBA_D45
FBA_D46	Y22	FBA_D46
FBA_D47	AA23	FBA_D47
FBA_D48	AD27	FBA_D48
FBA_D49	AB25	FBA_D49
FBA_D50	AD26	FBA_D50
FBA_D51	AC25	FBA_D51
FBA_D52	AA27	FBA_D52
FBA_D53	AA26	FBA_D53
FBA_D54	W26	FBA_D54
FBA_D55	Y25	FBA_D55
FBA_D56	R26	FBA_D56
FBA_D57	T25	FBA_D57
FBA_D58	N27	FBA_D58
FBA_D59	R27	FBA_D59
FBA_D60	V26	FBA_D60
FBA_D61	V27	FBA_D61
FBA_D62	W27	FBA_D62
FBA_D63	W25	FBA_D63

NV_NETCLASS FB_DQM

FBA_DQM[7..0] (OUT)

FBA_DQM0	D19	FBA_DQM0
FBA_DQM1	D14	FBA_DQM1
FBA_DQM2	C17	FBA_DQM2
FBA_DQM3	C22	FBA_DQM3
FBA_DQM4	P24	FBA_DQM4
FBA_DQM5	W24	FBA_DQM5
FBA_DQM6	AA25	FBA_DQM6
FBA_DQM7	U25	FBA_DQM7

NV_NETCLASS FB_DQS

FBA_DQS_WP[7..0] (III)

NET_NAME	DIFF_PAIR		
FBA_DQS_WP0	FBA_DQS0	E19	FBA_DQS_WP0
FBA_DQS_WP1	FBA_DQS1	C15	FBA_DQS_WP1
FBA_DQS_WP2	FBA_DQS2	B16	FBA_DQS_WP2
FBA_DQS_WP3	FBA_DQS3	B22	FBA_DQS_WP3
FBA_DQS_WP4	FBA_DQS4	R25	FBA_DQS_WP4
FBA_DQS_WP5	FBA_DQS5	W23	FBA_DQS_WP5
FBA_DQS_WP6	FBA_DQS6	AB26	FBA_DQS_WP6
FBA_DQS_WP7	FBA_DQS7	T26	FBA_DQS_WP7

NV_NETCLASS FB_DQS

FBA_DQS_RN[7..0] (III)

FBA_DQS_RN0	FBA_DQS0	F19	FBA_DQS_RN0
FBA_DQS_RN1	FBA_DQS1	C14	FBA_DQS_RN1
FBA_DQS_RN2	FBA_DQS2	A16	FBA_DQS_RN2
FBA_DQS_RN3	FBA_DQS3	A22	FBA_DQS_RN3
FBA_DQS_RN4	FBA_DQS4	P25	FBA_DQS_RN4
FBA_DQS_RN5	FBA_DQS5	W22	FBA_DQS_RN5
FBA_DQS_RN6	FBA_DQS6	AB27	FBA_DQS_RN6
FBA_DQS_RN7	FBA_DQS7	T27	FBA_DQS_RN7

SNN_FB_VREF — D23 — FB_VREF_PROBE

NV_NETCLASS FB_CMD

FBA_CMD[30..0] (OUT)

FBA_CMD0	C27	FBA_CMD0
FBA_CMD1	C26	SNN_FBA_CMD1
FBA_CMD2	E24	FBA_CMD2
FBA_CMD3	F24	FBA_CMD3
FBA_CMD4	D27	FBA_CMD4
FBA_CMD5	D26	FBA_CMD5
FBA_CMD6	F25	FBA_CMD6
FBA_CMD7	F26	FBA_CMD7
FBA_CMD8	F23	FBA_CMD8
FBA_CMD9	G22	FBA_CMD9
FBA_CMD10	G23	FBA_CMD10
FBA_CMD11	G24	FBA_CMD11
FBA_CMD12	F27	FBA_CMD12
FBA_CMD13	G25	FBA_CMD13
FBA_CMD14	G27	FBA_CMD14
FBA_CMD15	G26	FBA_CMD15
FBA_CMD16	M24	FBA_CMD16
FBA_CMD17	M23	SNN_FBA_CMD17
FBA_CMD18	K24	FBA_CMD18
FBA_CMD19	K23	FBA_CMD19
FBA_CMD20	M27	FBA_CMD20
FBA_CMD21	M26	FBA_CMD21
FBA_CMD22	M25	FBA_CMD22
FBA_CMD23	K26	FBA_CMD23
FBA_CMD24	K22	FBA_CMD24
FBA_CMD25	J23	FBA_CMD25
FBA_CMD26	J25	FBA_CMD26
FBA_CMD27	J24	FBA_CMD27
FBA_CMD28	K27	FBA_CMD28
FBA_CMD29	K25	FBA_CMD29
FBA_CMD30	J27	FBA_CMD30
FBA_CMD31	J26	SNN_FBA_CMD31

FBA_DEBUG0 — F22 — SNN_FBA_DEBUG0
FBA_DEBUG1 — J22 — SNN_FBA_DEBUG1

NET_NAME		DIFF_PAIR		NV_NETCLASS		
FBA_CLK0	D24	FBA_CLK0	FBA_CLK0*	FB_CLK	OUT	3,4,4
FBA_CLK0	D25	FBA_CLK0*	FBA_CLK0	FB_CLK	OUT	3,4,4
FBA_CLK1	N22	FBA_CLK1	FBA_CLK1*	FB_CLK	OUT	3,4,4
FBA_CLK1	M22	FBA_CLK1*	FBA_CLK1	FB_CLK	OUT	3,4,4

FBA_WCK01	D18	SNN_FBA_WCK01
FBA_WCK01	C18	SNN_FBA_WCK01*
FBA_WCK23	D17	SNN_FBA_WCK23
FBA_WCK23	D16	SNN_FBA_WCK23*
FBA_WCK45	T24	SNN_FBA_WCK45
FBA_WCK45	U24	SNN_FBA_WCK45*
FBA_WCK67	V24	SNN_FBA_WCK67
FBA_WCK67	V25	SNN_FBA_WCK67*

FB_PLLAVDD — F16 — 1V_PLL
FB_PLLAVDD — P22

FB_PLLAVDD	FB_DLLAVDD
GF117	GF119/GK208

FB_DLLAVDD — H22

PD REQUIRED FOR INITIALIZATION

FBA_CMD0	LOWER CHANNEL ODT	R160 10K 5% 0402 COMMON	GND
FBA_CMD3	LOWER CHANNEL CKE	R157 10K 5% 0402 COMMON	GND
FBA_CMD16	UPPER CHANNEL ODT	R161 10K 5% 0402 COMMON	GND
FBA_CMD19	UPPER CHANNEL CKE	R158 10K 5% 0402 COMMON	GND
FBA_CMD20	RST	R163 10K 5% 0402 COMMON	GND

CLK Termination

3,4,4	IN	FBA_CLK0	R155 80.6 1% 0402 COMMON
3,4,4	IN	FBA_CLK0*	
3,4,4	IN	FBA_CLK1	R156 80.6 1% 0402 COMMON
3,4,4	IN	FBA_CLK1*	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU FRAME BUFFER: PARTITION A

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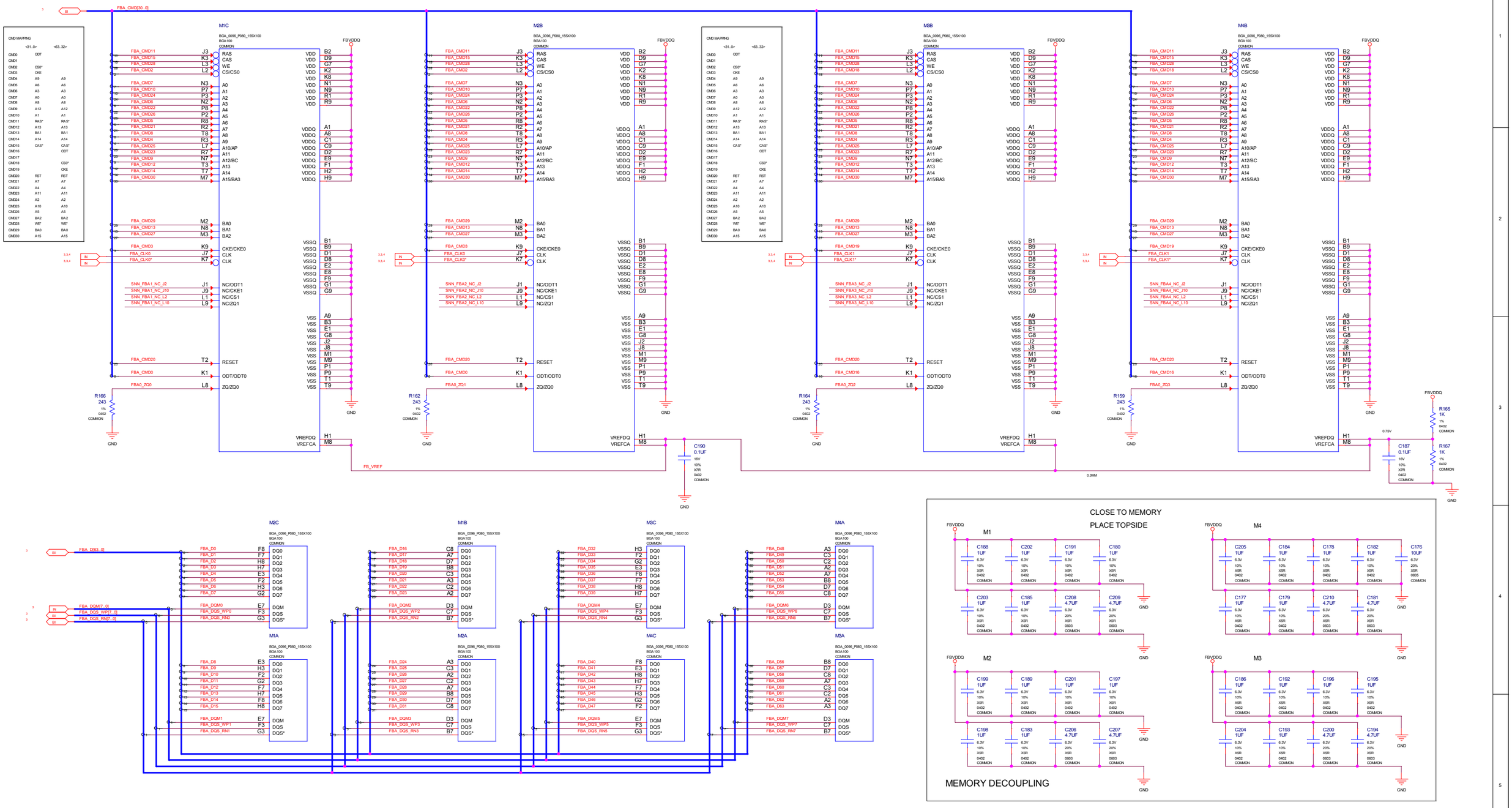
DDR3 Memories



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DDR3 Memories

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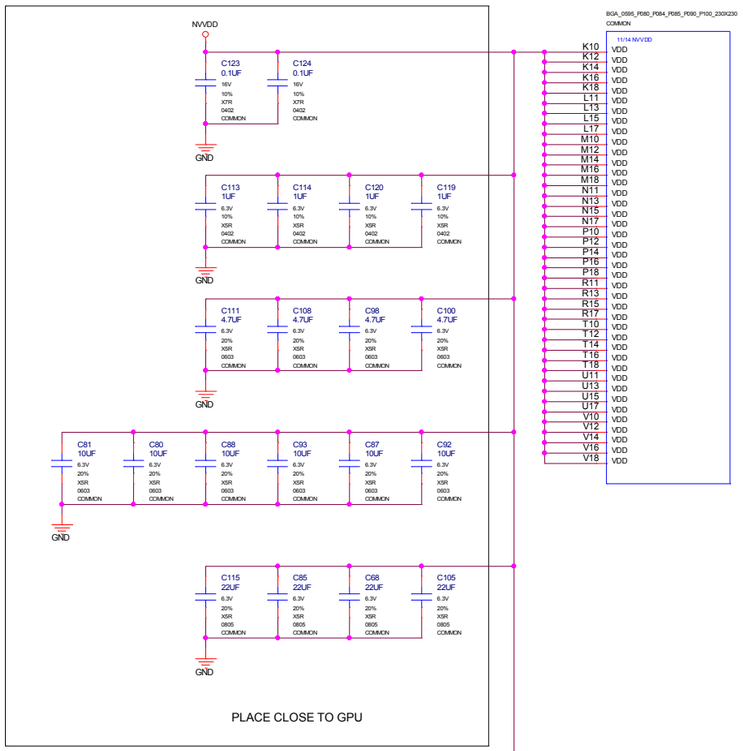
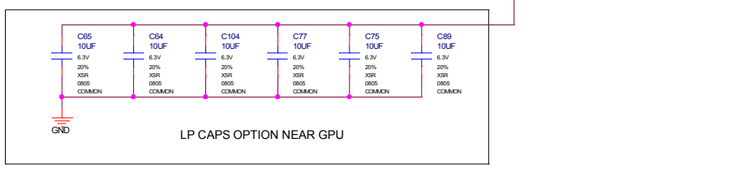
DECOUPLING FOR CORE POWER_TOP



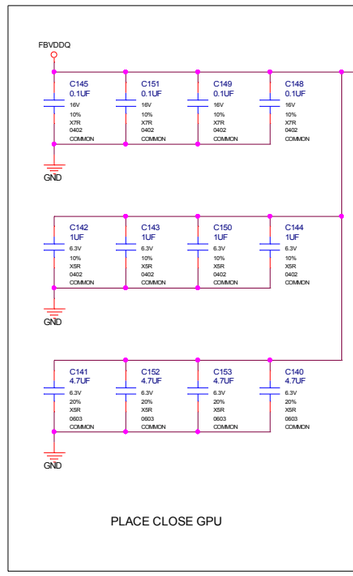


G1C

BGA_0595_PD80_PD84_PD85_PD90_P100_230X230
COMMON

11/14 NVVDD

K10	VDD
K12	VDD
K14	VDD
K16	VDD
K18	VDD
L11	VDD
L13	VDD
L15	VDD
L17	VDD
M10	VDD
M12	VDD
M14	VDD
M16	VDD
M18	VDD
N11	VDD
N13	VDD
N15	VDD
N17	VDD
P10	VDD
P12	VDD
P14	VDD
P16	VDD
P18	VDD
R11	VDD
R13	VDD
R15	VDD
R17	VDD
T10	VDD
T12	VDD
T14	VDD
T16	VDD
T18	VDD
U11	VDD
U13	VDD
U15	VDD
U17	VDD
V10	VDD
V12	VDD
V14	VDD
V16	VDD
V18	VDD



G1E

BGA_0595_PD80_PD84_PD85_PD90_P100_230X230
COMMON

12/14 FBVDDQ

B26	FBVDDQ
C25	FBVDDQ
E23	FBVDDQ
E26	FBVDDQ
F14	FBVDDQ
F21	FBVDDQ
G13	FBVDDQ
G14	FBVDDQ
G15	FBVDDQ
G16	FBVDDQ
G18	FBVDDQ
G19	FBVDDQ
G20	FBVDDQ
G21	FBVDDQ
H24	FBVDDQ
H26	FBVDDQ
J21	FBVDDQ
K21	FBVDDQ
L22	FBVDDQ
L24	FBVDDQ
L26	FBVDDQ
M21	FBVDDQ
N21	FBVDDQ
R21	FBVDDQ
T21	FBVDDQ
V21	FBVDDQ
W21	FBVDDQ

FBVDDQ

FB_CAL_PD_VDDQ	D22	FB_CAL_PD_VDDQ	R143 40.2 0402 1%	COMMON
FB_CAL_PU_GND	C24	FB_CAL_PU_GND	R154 40.2 0402 1%	COMMON
FB_CALTERM_GND	B25	FB_CAL_TERM_GND	R153 40.2 0402 1%	COMMON

Adjustable depending on GPU

GND

G1F

BGA_0595_PD80_PD84_PD85_PD90_P100_230X230
COMMON

13/14 GND

A2	GND	GND	M13
AB17	GND	GND	M15
AB20	GND	GND	M17
AB24	GND	GND	N10
AC2	GND	GND	N12
AC22	GND	GND	N14
AC26	GND	GND	N16
AC5	GND	GND	N18
AC8	GND	GND	P11
AD12	GND	GND	P13
AD13	GND	GND	P15
AD26	GND	GND	P17
AD15	GND	GND	P2
AD16	GND	GND	P23
AD18	GND	GND	P26
AD19	GND	GND	P5
AD21	GND	GND	R10
AD22	GND	GND	R12
AE11	GND	GND	R14
AE14	GND	GND	R16
AE17	GND	GND	R18
AE20	GND	GND	T11
AB11	GND	GND	T13
AF1	GND	GND	T15
AF11	GND	GND	T17
AF14	GND	GND	U10
AF17	GND	GND	U12
AF20	GND	GND	U14
AF23	GND	GND	U16
AF5	GND	GND	U18
AF8	GND	GND	U2
AG2	GND	GND	U23
AG26	GND	GND	U26
AB14	GND	GND	U5
B1	GND	GND	V11
B11	GND	GND	V13
B14	GND	GND	V15
B17	GND	GND	V17
B20	GND	GND	Y2
B23	GND	GND	Y23
B27	GND	GND	Y26
B5	GND	GND	Y5
B8	GND		
E11	GND		
E14	GND		
E17	GND		
E2	GND		
E20	GND		
E22	GND		
E25	GND		
E5	GND		
E8	GND		
H2	GND		
H23	GND		
H25	GND		
H5	GND		
K11	GND		
K13	GND		
K15	GND		
K17	GND		
L10	GND		
L12	GND		
L14	GND		
L16	GND		
L18	GND		
L2	GND		
L23	GND		
L25	GND		
L5	GND	GND	AA7
M11	GND	GND	AB7

GND GND

G1D

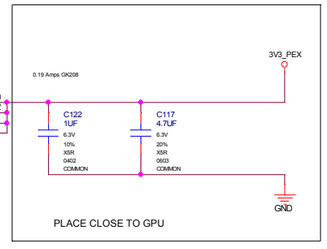
BGA_0595_PD80_PD84_PD85_PD90_P100_230X230
COMMON

14/14 XVDD/VDD33

SNN_NC_AD10	AD10	NC	VDD33 G10
SNN_NC_AD7	AD7	NC	VDD33 G12
SNN_NC_B19	B19	NC	VDD33 G8
			VDD33 G9
SNN_NC_F11	F11	3V3AUX_NC	
3V3_PLL	V5	FERMI_RSVD1_NC	
	V6	FERMI_RSVD2_NC	

CONFIGURABLE
POWER CHANNELS
* nc on substrate

3V3_PEX	
G1	XPWR_G1
G2	XPWR_G2
G3	XPWR_G3
G4	XPWR_G4
G5	XPWR_G5
G6	XPWR_G6
G7	XPWR_G7
3V3_PLL	
V1	XPWR_V1
V2	XPWR_V2
W1	XPWR_W1
W2	XPWR_W2
W3	XPWR_W3
W4	XPWR_W4



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DECOUPLING FOR CORE POWER_TOP

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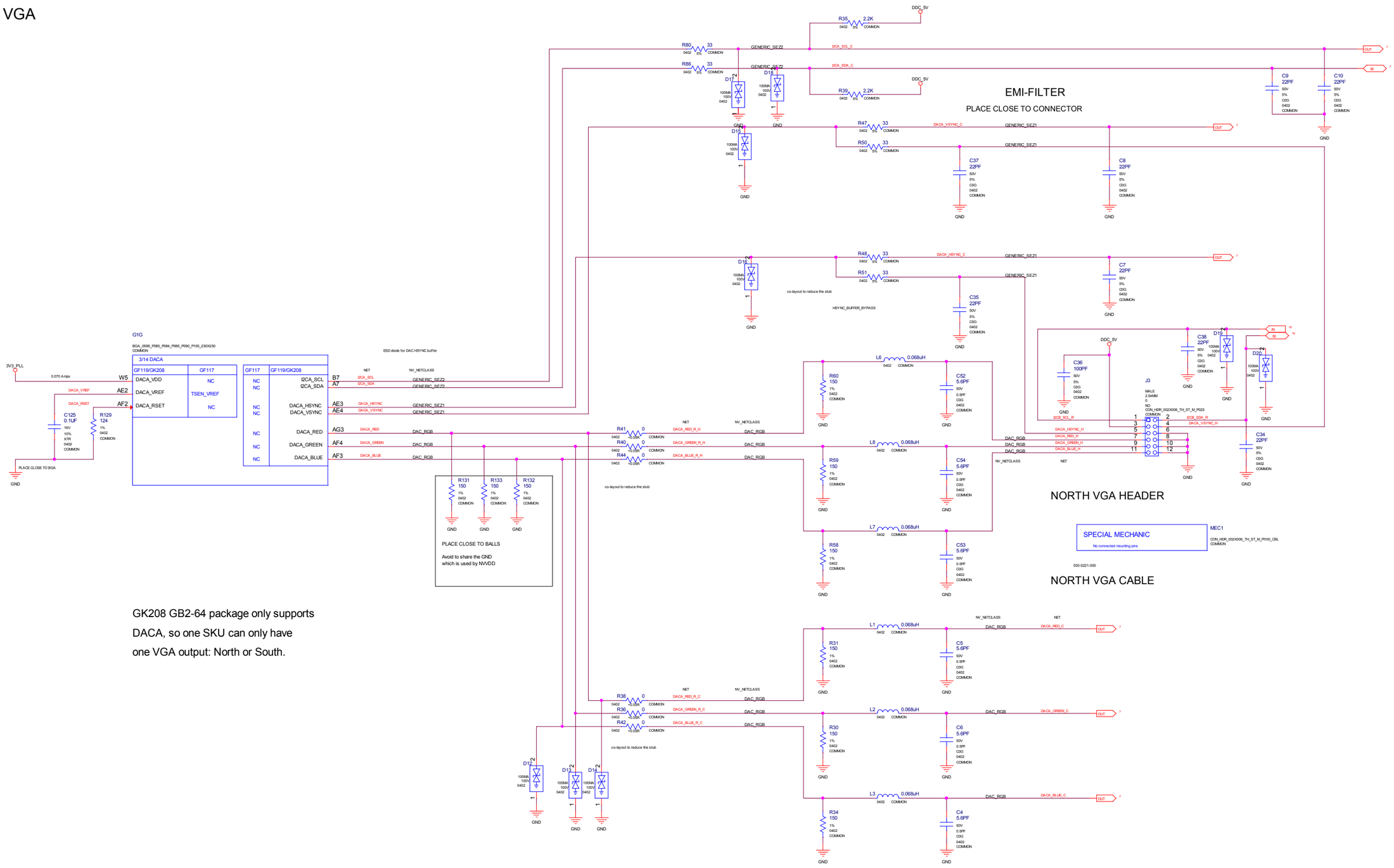
Page11: DACA VGA

GK208 GB2-64 package only supports DACA, so one SKU can only have one VGA output: North or South.



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DACA VGA

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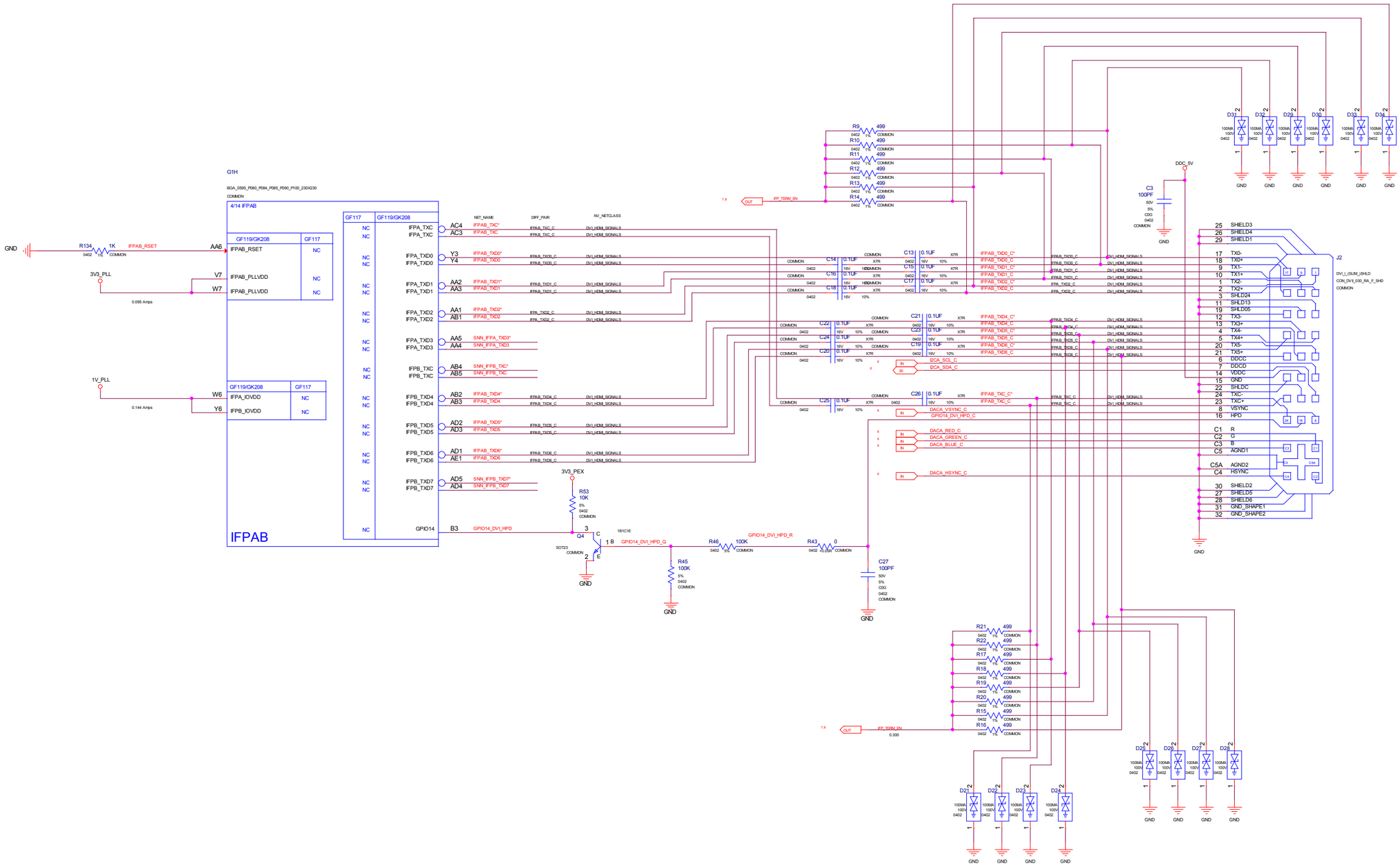
IFPAB TMDS



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPAB TMDS

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IFPC HDMI

PLACE UNDER GPU

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPC HDMI

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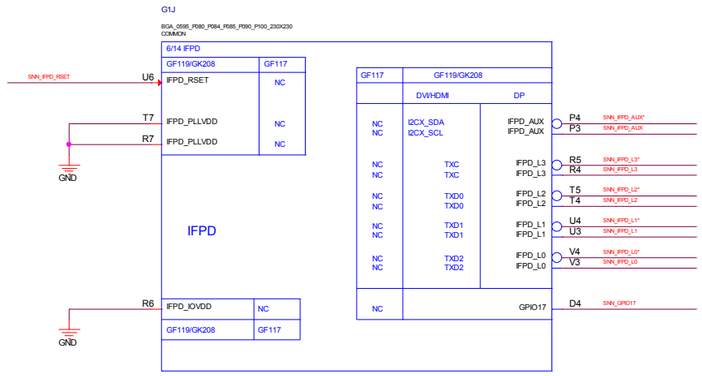
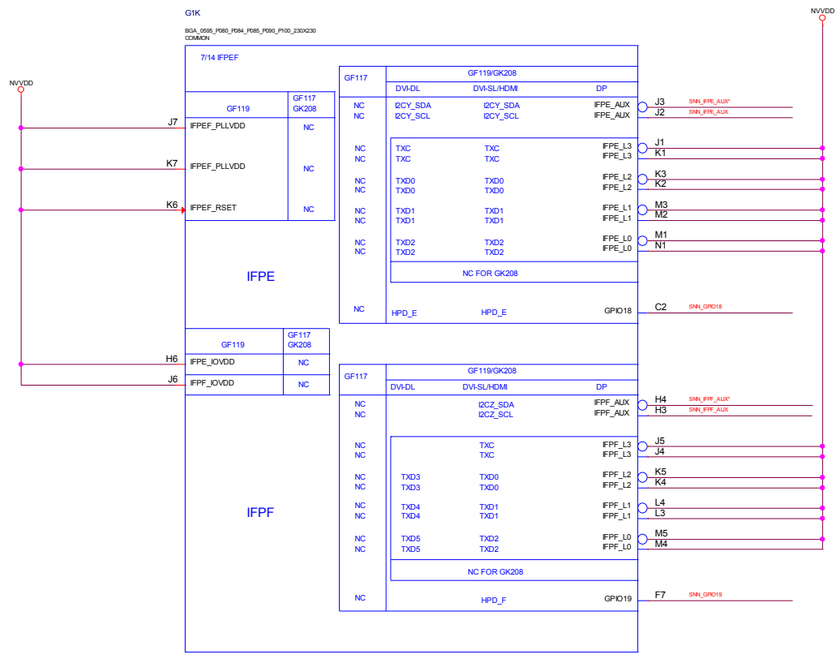
UNSED IFPD, IFPE & IFPF





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	UNSED IFPD, IFPE & IFPF

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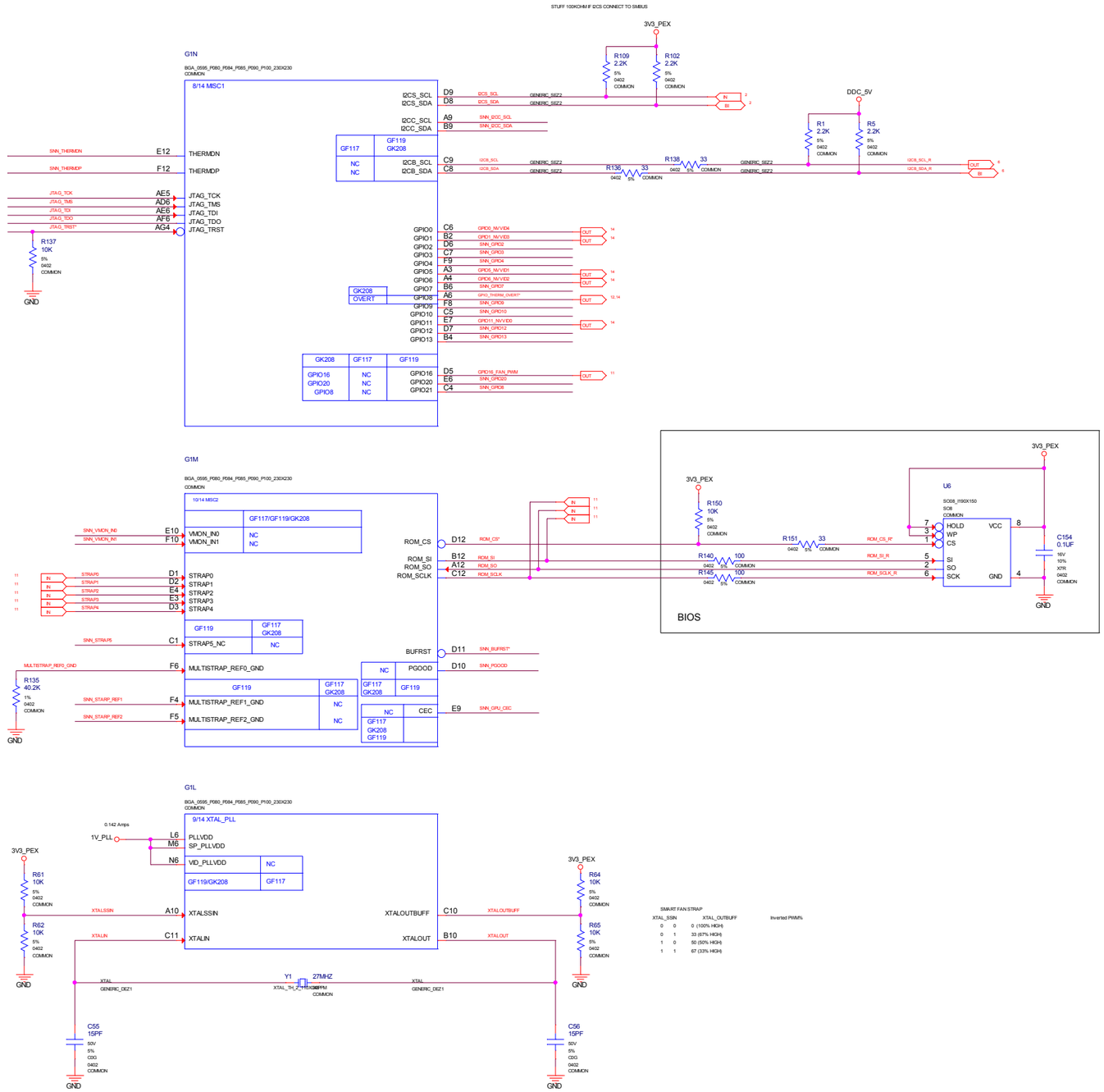
MISC INTERFACES

JTAG



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PAGE DETAIL	MISC INTERFACES

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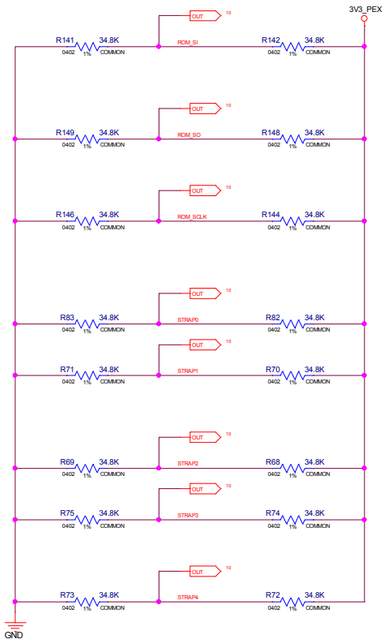
Page13: PCI-E Reset, STRAPS & FAN

Multilevel Straps

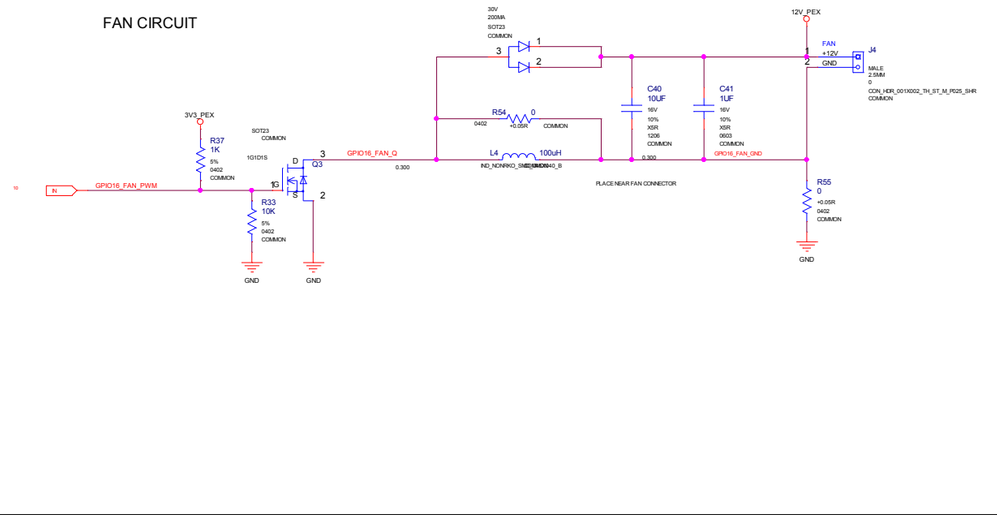
0000	5.1K to GND	1000	5.1K to VCC
0001	10K to GND	1001	10K to VCC
0010	15K to GND	1010	15K to VCC
0011	20K to GND	1011	20K to VCC
0100	24.9K to GND	1100	24.9K to VCC
0101	30.1K to GND	1101	30.1K to VCC
0110	34.8K to GND	1110	34.8K to VCC
0111	45.3K to GND	1111	45.3K to VCC

GK208 Straps



Bit	Signal	Values				
03:	RAMCFG[3]	0000	Reserved			ROM_SI
		0001	256Mx16 DDR3 X16 64bit Micron			
02:	RAMCFG[2]	0010	256Mx16 DDR3 X16 64bit Hynix			
		0011	256Mx16 DDR3 X16 64bit Samsung			
01:	RAMCFG[1]					
		0101	128Mx16 DDR3 X16 64bit Micron			
00:	RAMCFG[0]	0110	128Mx16 DDR3 X16 64bit Hynix			
		0111	128Mx16 DDR3 X16 64bit Samsung			
03:	FB[1]	01	128MB			ROM_SO
		10	256MB			
02:	FB[0]					
01:	SMB_ALT_ADDR	0	DISABLED	1	ENABLED	
00:	VGA_DEVICE	0	DISABLED	1	ENABLED	
03:	PCI_DEVID_EXT	SKU0	0	SKU1	TBD	ROM_SCLK
02:	SUB_VENDOR	0	NO_BIOS	1	BIOS	
01:	PCI_DEVID_EXT_BITS	SKU0	0	SKU1	TBD	
00:	PEX_PLL_EN_TERM100	0	DISABLED	1	ENABLED	
03:	USER[3]	0000	INIT			Strap0
02:	USER[2]					
01:	USER[1]					
00:	USER[0]					
03:	3GIO_PADCFG_LUT_ADR[3]	0000	DISKTOP_DEFAULT	1000	DISKTOP_HTHRS	Strap1
		0001	MOBILE_DEFAULT	1001	MOBILE_HTHRS_NAMP	
02:	3GIO_PADCFG_LUT_ADR[2]	0010	MOBILE_NTHRS_LLAMP	1010	MOBILE_HTHRS_LLAMP	
		0011	MOBILE_NTHRS_LAMP	1011	MOBILE_HTHRS_LAMP	
01:	3GIO_PADCFG_LUT_ADR[1]	0100	MOBILE_NTHRS_HAMP	1100	MOBILE_HTHRS_HAMP	
		0101	MOBILE_NTHRS_HHAMP	1101	MOBILE_HTHRS_HHAMP	
00:	3GIO_PADCFG_LUT_ADR[0]	0110	MOBILE_NTHRS_HHHAMP	1110	MOBILE_HTHRS_HHHAMP	
		0111	MOBILE_NTHRS_HHHHAMP	1111	MOBILE_HTHRS_HHHHAMP	
03:	PCI_DEVID[3]	SKU0	0100			Strap2
02:	PCI_DEVID[2]					
01:	PCI_DEVID[1]					
00:	PCI_DEVID[0]					
03:	SOR3_EXPOSED	0	DISABLED	1	ENABLED	Strap3
02:	SOR2_EXPOSED	0	DISABLED	1	ENABLED	
01:	SOR1_EXPOSED	0	DISABLED	1	ENABLED	
00:	SOR0_EXPOSED	0	DISABLED	1	ENABLED	
02:	PCIE_SPEED_CHANGE_GEN3	0	DISABLED	1	ENABLED	Strap4
01:	PCIE_MAX_SPEED	0	GEN1	1	GEN3	
00:	DP_PLL_VDD_3V3	0	USE1V8	1	USE3V3	

FAN CIRCUIT



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PAGE DETAIL	STRAPS & FAN

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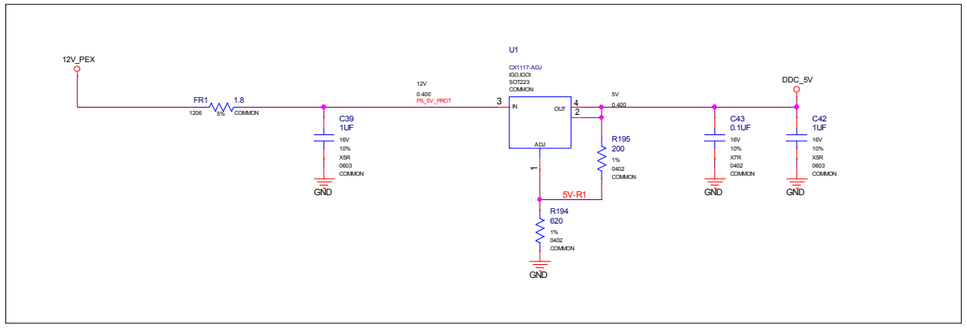
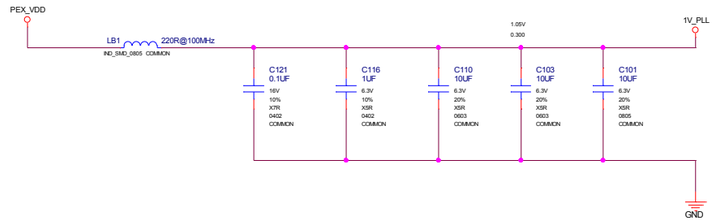
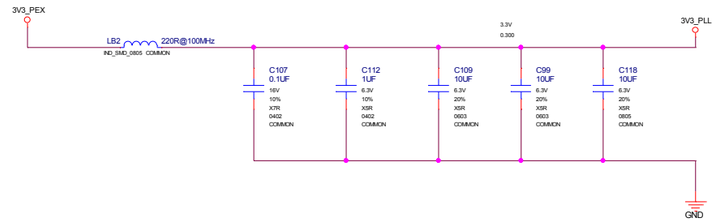
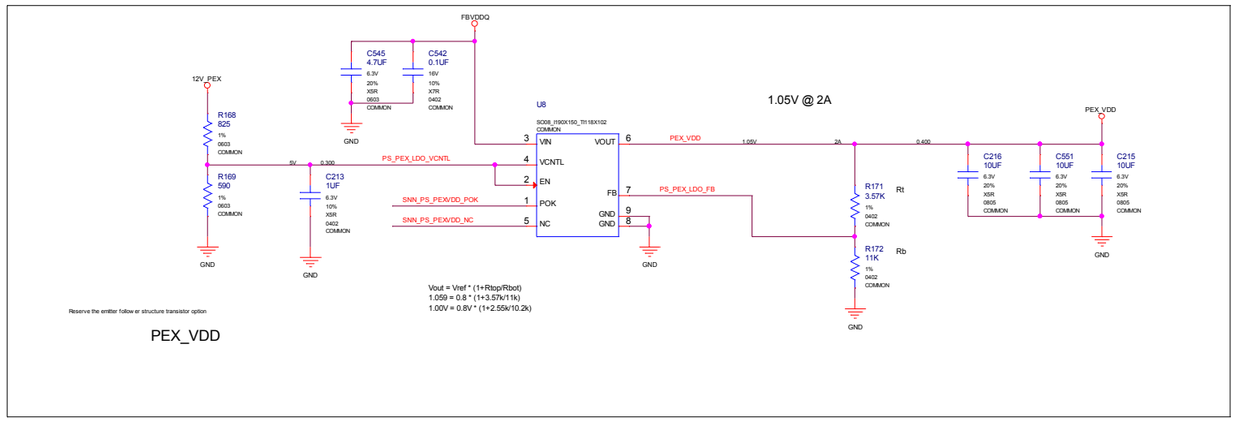
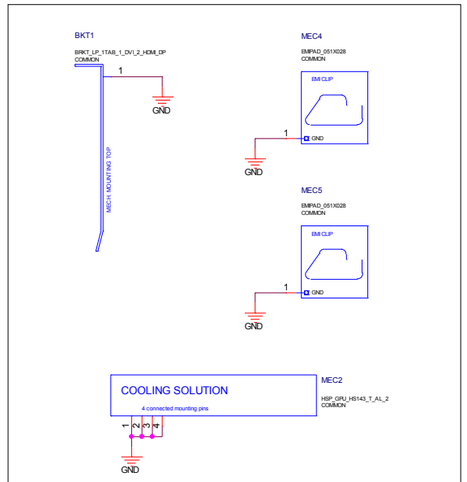
POWER SUPPLY I: PEXVDD, 5V

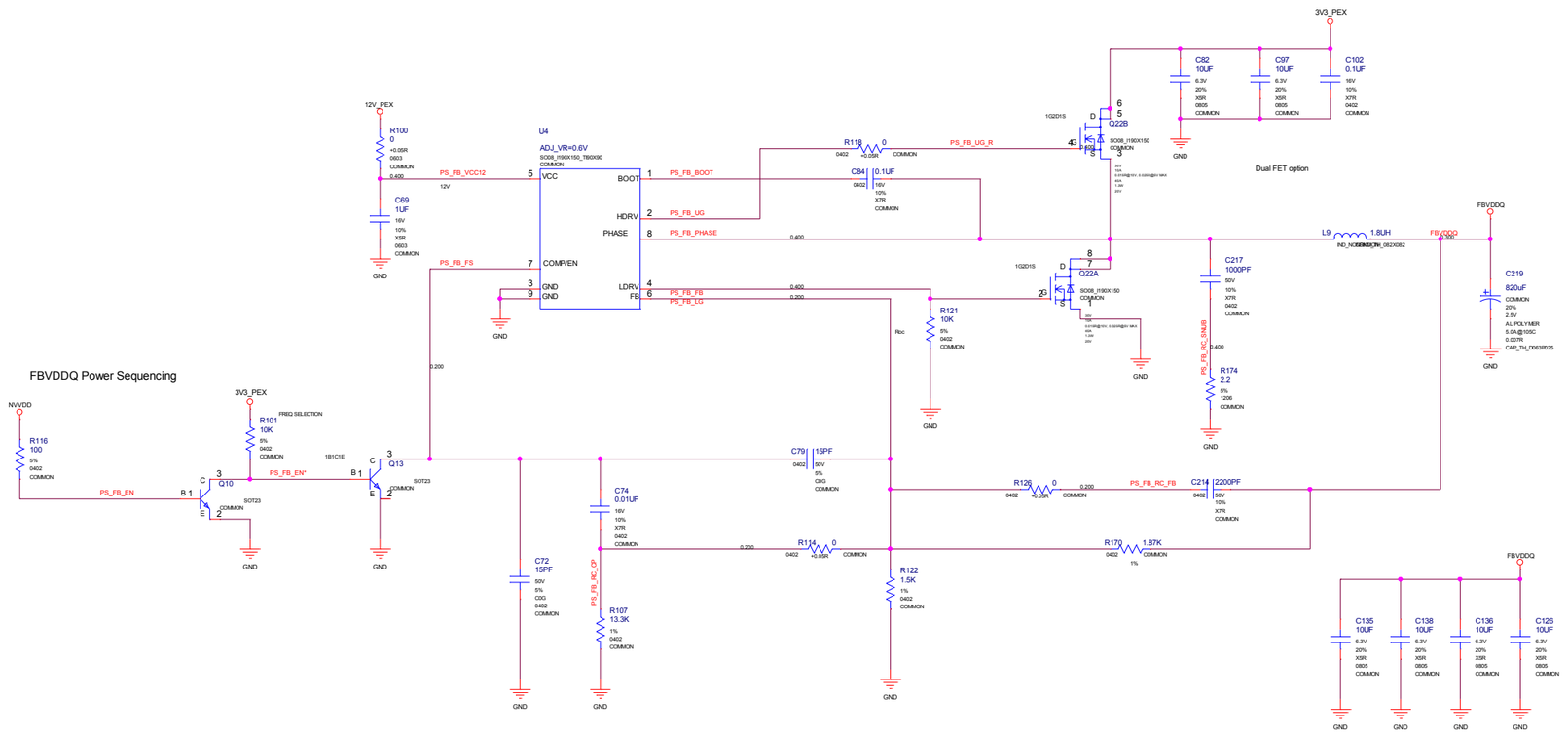




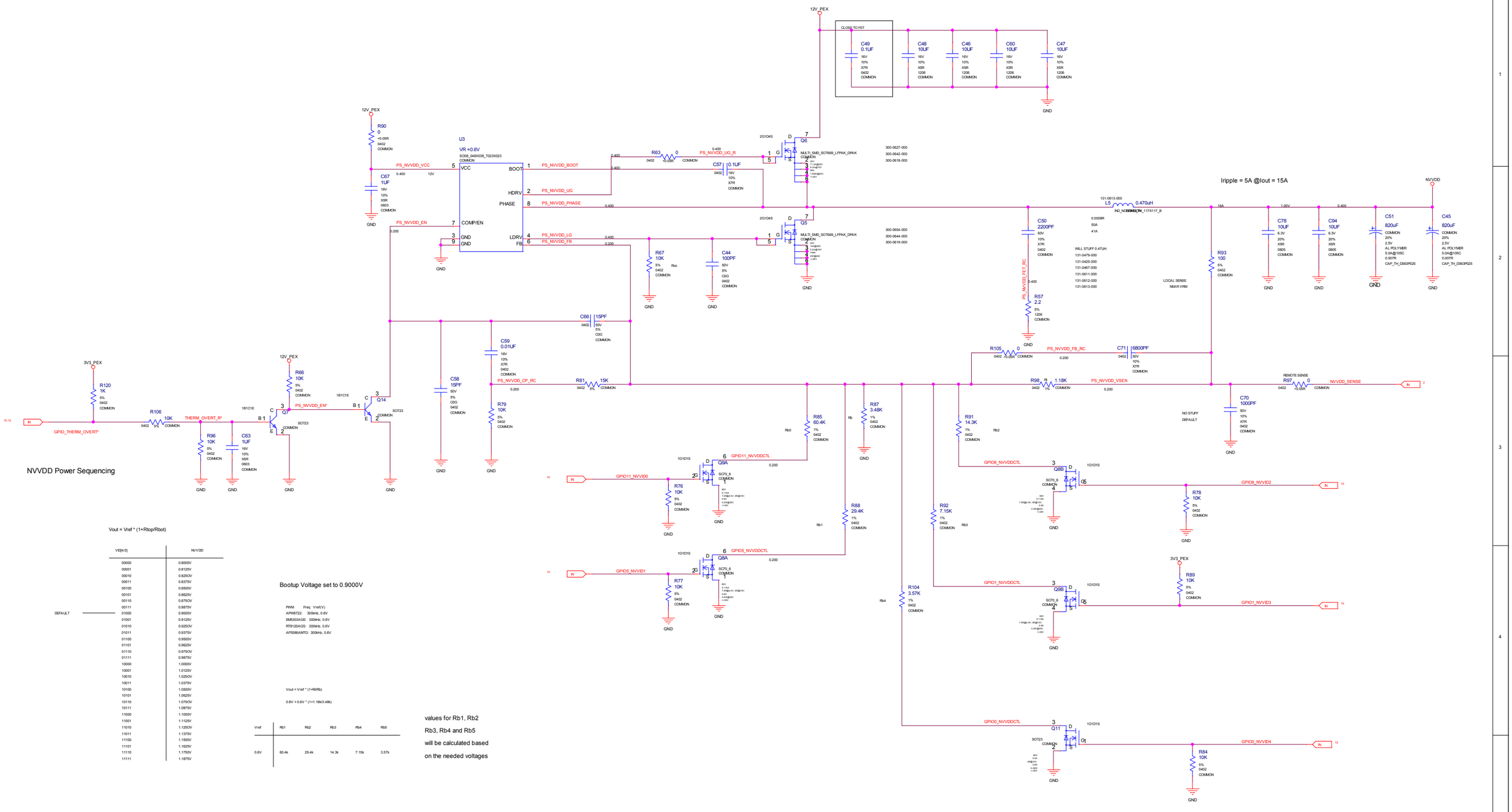







FBVDDQ Power Sequencing
NVVDD
R116
100
5%
0402
COMMON
PS_FB_EN
3V3_PEX
R101
10K
5%
0402
COMMON
FREQ SELECTION
Q10
SOT23
COMMON
PS_FB_EN*
1B1C1E
Q13
SOT23
COMMON
GND
12V_PEX
R100
0
+0.05R
0603
COMMON
0.400
PS_FB_VCC12
12V
C69
1UF
16V
10%
X5R
0603
COMMON
U4
ADJ_VR=0.6V
SOI08_I190X150_TB0X90
COMMON
VCC
BOOT
HDRV
PHASE
LDRV
FB
COMP/EN
GND
GND
PS_FB_BOOT
PS_FB_UG
PS_FB_PHASE
PS_FB_FB
PS_FB_LG
PS_FB_FS
0.200
0.400
R118
0
+0.05R
0402
COMMON
PS_FB_UG_R
C84
0.1UF
16V
10%
X7R
0402
COMMON
1G2D1S
Q22B
SO08_I190X150
COMMON
Q22A
SO08_I190X150
COMMON
Dual FET option
C82
10UF
6.3V
20%
X5R
0805
COMMON
C97
10UF
6.3V
20%
X5R
0805
COMMON
C102
0.1UF
16V
10%
X7R
0402
COMMON
3V3_PEX
L9
1.8UH
FBVDDQ
C219
820uF
COMMON
20%
2.5V
AL POLYMER
5.0A@105C
0.007R
CAP_TH_D063P025
C217
1000PF
50V
10%
X7R
0402
COMMON
PS_FB_RC_SNUB
R174
2.2
5%
1206
COMMON
R121
10K
5%
0402
COMMON
Rbc
C79
15PF
50V
5%
C0G
COMMON
C74
0.01UF
16V
10%
X7R
0402
COMMON
R126
0
+0.05R
0402
COMMON
0.200
PS_FB_RC_FB
C214
2200PF
50V
10%
X7R
COMMON
R114
0
+0.05R
0402
COMMON
R170
1.87K
1%
0402
COMMON
C72
15PF
50V
5%
C0G
0402
COMMON
PS_FB_RC_CP
R107
13.3K
1%
0402
COMMON
R122
1.5K
1%
0402
COMMON
C135
10UF
6.3V
20%
X5R
0805
COMMON
C138
10UF
6.3V
20%
X5R
0805
COMMON
C136
10UF
6.3V
20%
X5R
0805
COMMON
C126
10UF
6.3V
20%
X5R
0805
COMMON

POWER SUPPLY III: NVVDD



VID[4:0]	NVVDD
00000	0.8000V
00001	0.8125V
00010	0.8250V
00011	0.8375V
00100	0.8500V
00101	0.8625V
00110	0.8750V
00111	0.8875V
01000	0.9000V
01001	0.9125V
01010	0.9250V
01011	0.9375V
01100	0.9500V
01101	0.9625V
01110	0.9750V
01111	0.9875V
10000	1.0000V
10001	1.0125V
10010	1.0250V
10011	1.0375V
10100	1.0500V
10101	1.0625V
10110	1.0750V
10111	1.0875V
11000	1.1000V
11001	1.1125V
11010	1.1250V
11011	1.1375V
11100	1.1500V
11101	1.1625V
11110	1.1750V
11111	1.1875V

DEFAULT

Bootup Voltage set to 0.9000V

PWM	Freq	Vref(V)
APW8722:	300kHz,	0.6V
EMS303AGE:	300kHz,	0.6V
RT8122AGS:	300kHz,	0.6V
AP2586AMTG:	300kHz,	0.6V

Vout = Vref * (1+Rb/Rb)

0.6V = 0.6V * (1+1.18k/3.48k)

Vref	Rb1	Rb2	Rb3	Rb4	Rb5
0.6V	60.4k	29.4k	14.3k	7.15k	3.57k

values for Rb1, Rb2
Rb3, Rb4 and Rb5
will be calculated based
on the needed voltages

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	POWER SUPPLY III: NVVDD

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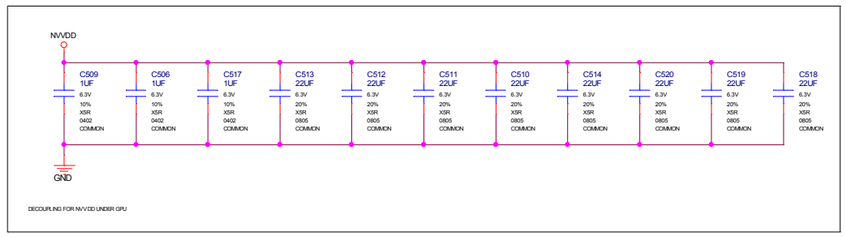
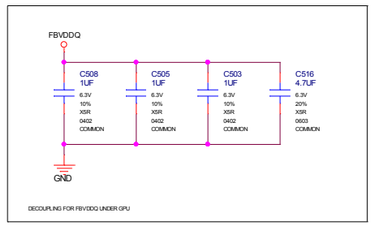
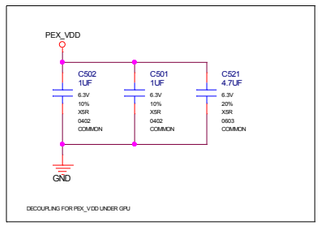
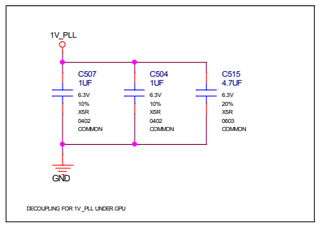
DECOUPLING FOR CORE POWER_BOTTOM









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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DECOUPLING FOR CORE POWER_BOTTOM

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