P561: G98, DDR2 MEMORY 32MX16/16Mx16/64MX16

V116-32

REV HISTORY

History 10

96/09/27	page 08	add AV_OUT
	page 13	change Q1, Q2 to TO252
	page 14	add FBVDDQ-LDO block, change U2 footprint
96/09/28	page 07	change J4 footprint
	page 12	add J7 (co-lay J6)
	page 13	add R572 for RT9259A, R570 footprint change to 0805, change L11, C11, C12, C31 footprint
	page 14	remove PWM block add D20, D21, C211, C212, C213, C214
96/10/01	page 14	add R210, R211
	page 09	add R75~R88, R63~R69, L15~L21 for DVI (EMI_solution)
96/10/02	page 12	add FAN Control Function
96/10/03	page 09	and netname (Between common Choke and DVI connector)
96/10/05	page 12	cnage Y501 (4 pin to 2 pin)

History 20

96/10/03	page 14	remove FBVDDQ-LDO block, add FBVDDQ-PWM function change L15 footprint as CHK4417C_3R3S01, change C35 footprint
96/10/05	page 12	cahnge Y501 (4pin to 2 pin)
96/10/09	page 11	add FM1~~ FM6 for Fiducial Point add U301~~U306 for EMI
	page 13	add C309 for EMI
	page 14	add C301~~C308, C310~~C312 for EMI
96/10/10	page 13	add L30
96/10/11	page 13	remove L10

- -

96/10/16 Page 10 : Add HDMI solution .

add J8 , Q11,Q12 , L31~L38 , D11~D14 , C110~C123 , C131~C138 , R201~R208 , R211~R219 , R331~R338 .

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10561-xxxx-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10561-0000-100	P561: G98-300, 64 BIT DDR2 16Mx16 MEMORY, VGA+DVI+HDout
2	SKU0001	600-10561-0001-100	P561: G98-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+HDout
3	SKU0997	600-10561-0997-100	P561: G98-300, 64 BIT DDR2 32MX16 MEMORY, VGA+DVI+HDOUT
4	SKU0997	600-10561-0997-200	P561: G98-300, 64 BIT DDR2 32MX16 MEMORY, VGA+DVI+HDOUT
5	SKU0001	600-10561-0001-200	P561: G98-300, 64 BIT DDR2 32MX16 MEMORY, VGA+DVI+HDOUT
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P561 Overview

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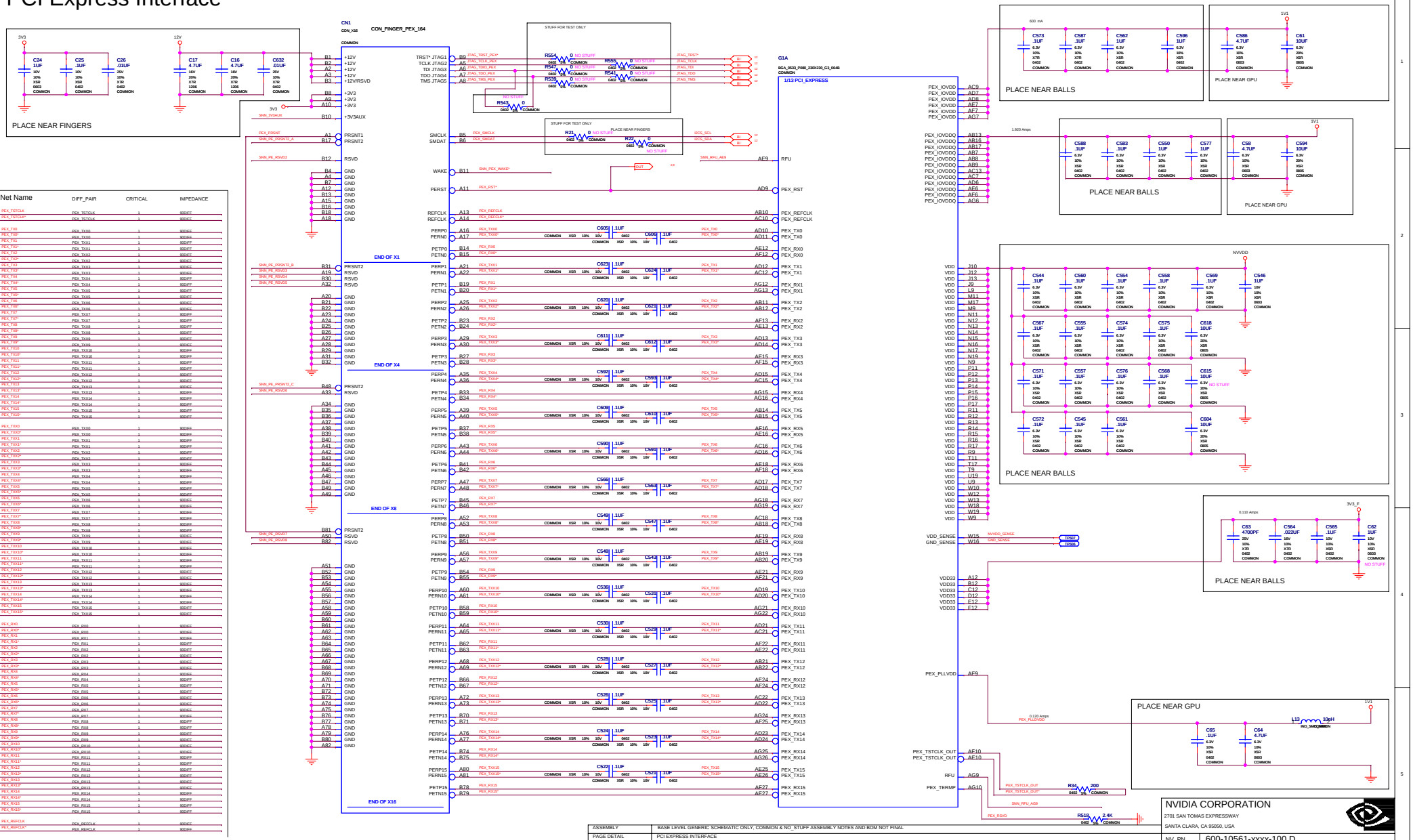
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
NAME		DATE	31-AUG-2007

PCI Express Interface



Net Name	DIFF_PAIR	CRITICAL	IMPEDANCE
PEX_TSTCLK	PEX_TSTCLK	1	90DIFF
PEX_TSTCLK*	PEX_TSTCLK*	1	90DIFF
PEX_TX0	PEX_TX0	1	90DIFF
PEX_TX0*	PEX_TX0*	1	90DIFF
PEX_TX1	PEX_TX1	1	90DIFF
PEX_TX1*	PEX_TX1*	1	90DIFF
PEX_TX2	PEX_TX2	1	90DIFF
PEX_TX2*	PEX_TX2*	1	90DIFF
PEX_TX3	PEX_TX3	1	90DIFF
PEX_TX3*	PEX_TX3*	1	90DIFF
PEX_TX4	PEX_TX4	1	90DIFF
PEX_TX4*	PEX_TX4*	1	90DIFF
PEX_TX5	PEX_TX5	1	90DIFF
PEX_TX5*	PEX_TX5*	1	90DIFF
PEX_TX6	PEX_TX6	1	90DIFF
PEX_TX6*	PEX_TX6*	1	90DIFF
PEX_TX7	PEX_TX7	1	90DIFF
PEX_TX7*	PEX_TX7*	1	90DIFF
PEX_TX8	PEX_TX8	1	90DIFF
PEX_TX8*	PEX_TX8*	1	90DIFF
PEX_TX9	PEX_TX9	1	90DIFF
PEX_TX9*	PEX_TX9*	1	90DIFF
PEX_TX10	PEX_TX10	1	90DIFF
PEX_TX10*	PEX_TX10*	1	90DIFF
PEX_TX11	PEX_TX11	1	90DIFF
PEX_TX11*	PEX_TX11*	1	90DIFF
PEX_TX12	PEX_TX12	1	90DIFF
PEX_TX12*	PEX_TX12*	1	90DIFF
PEX_TX13	PEX_TX13	1	90DIFF
PEX_TX13*	PEX_TX13*	1	90DIFF
PEX_TX14	PEX_TX14	1	90DIFF
PEX_TX14*	PEX_TX14*	1	90DIFF
PEX_TX15	PEX_TX15	1	90DIFF
PEX_TX15*	PEX_TX15*	1	90DIFF
PEX_RX0	PEX_RX0	1	90DIFF
PEX_RX0*	PEX_RX0	1	90DIFF
PEX_RX1	PEX_RX1	1	90DIFF
PEX_RX1*	PEX_RX1	1	90DIFF
PEX_RX2	PEX_RX2	1	90DIFF
PEX_RX2*	PEX_RX2	1	90DIFF
PEX_RX3	PEX_RX3	1	90DIFF
PEX_RX3*	PEX_RX3	1	90DIFF
PEX_RX4	PEX_RX4	1	90DIFF
PEX_RX4*	PEX_RX4	1	90DIFF
PEX_RX5	PEX_RX5	1	90DIFF
PEX_RX5*	PEX_RX5	1	90DIFF
PEX_RX6	PEX_RX6	1	90DIFF
PEX_RX6*	PEX_RX6	1	90DIFF
PEX_RX7	PEX_RX7	1	90DIFF
PEX_RX7*	PEX_RX7	1	90DIFF
PEX_RX8	PEX_RX8	1	90DIFF
PEX_RX8*	PEX_RX8	1	90DIFF
PEX_RX9	PEX_RX9	1	90DIFF
PEX_RX9*	PEX_RX9	1	90DIFF
PEX_RX10	PEX_RX10	1	90DIFF
PEX_RX10*	PEX_RX10	1	90DIFF
PEX_RX11	PEX_RX11	1	90DIFF
PEX_RX11*	PEX_RX11	1	90DIFF
PEX_RX12	PEX_RX12	1	90DIFF
PEX_RX12*	PEX_RX12	1	90DIFF
PEX_RX13	PEX_RX13	1	90DIFF
PEX_RX13*	PEX_RX13	1	90DIFF
PEX_RX14	PEX_RX14	1	90DIFF
PEX_RX14*	PEX_RX14	1	90DIFF
PEX_RX15	PEX_RX15	1	90DIFF
PEX_RX15*	PEX_RX15	1	90DIFF
PEX_REFCLK	PEX_REFCLK	1	90DIFF
PEX_REFCLK*	PEX_REFCLK	1	90DIFF

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE

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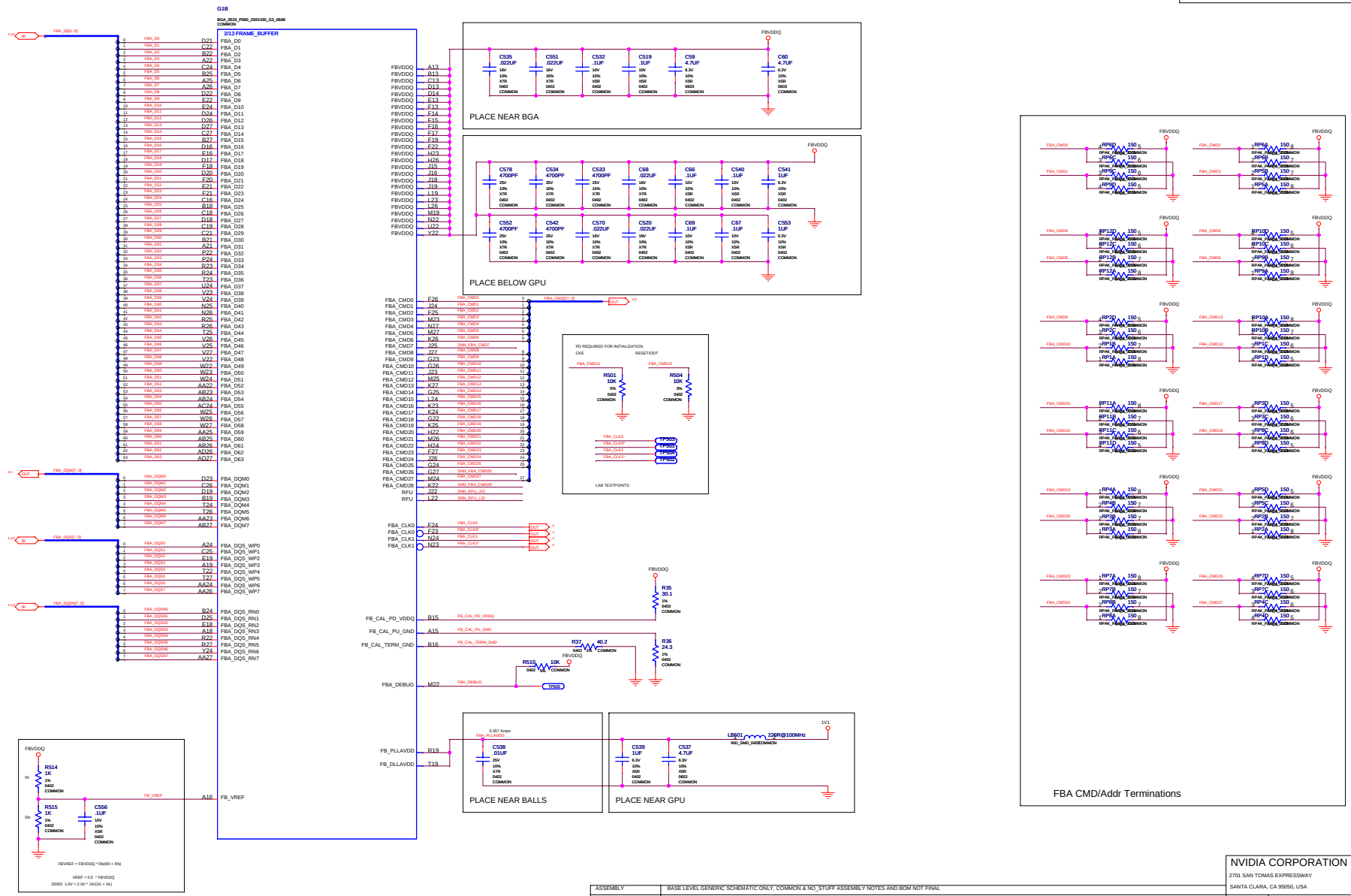
SANTA CLARA, CA 95050, USA

NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
NAME		DATE	31-AUG-2007

Frame Buffer Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Frame Buffer Interface

NVIDIA CORPORATION
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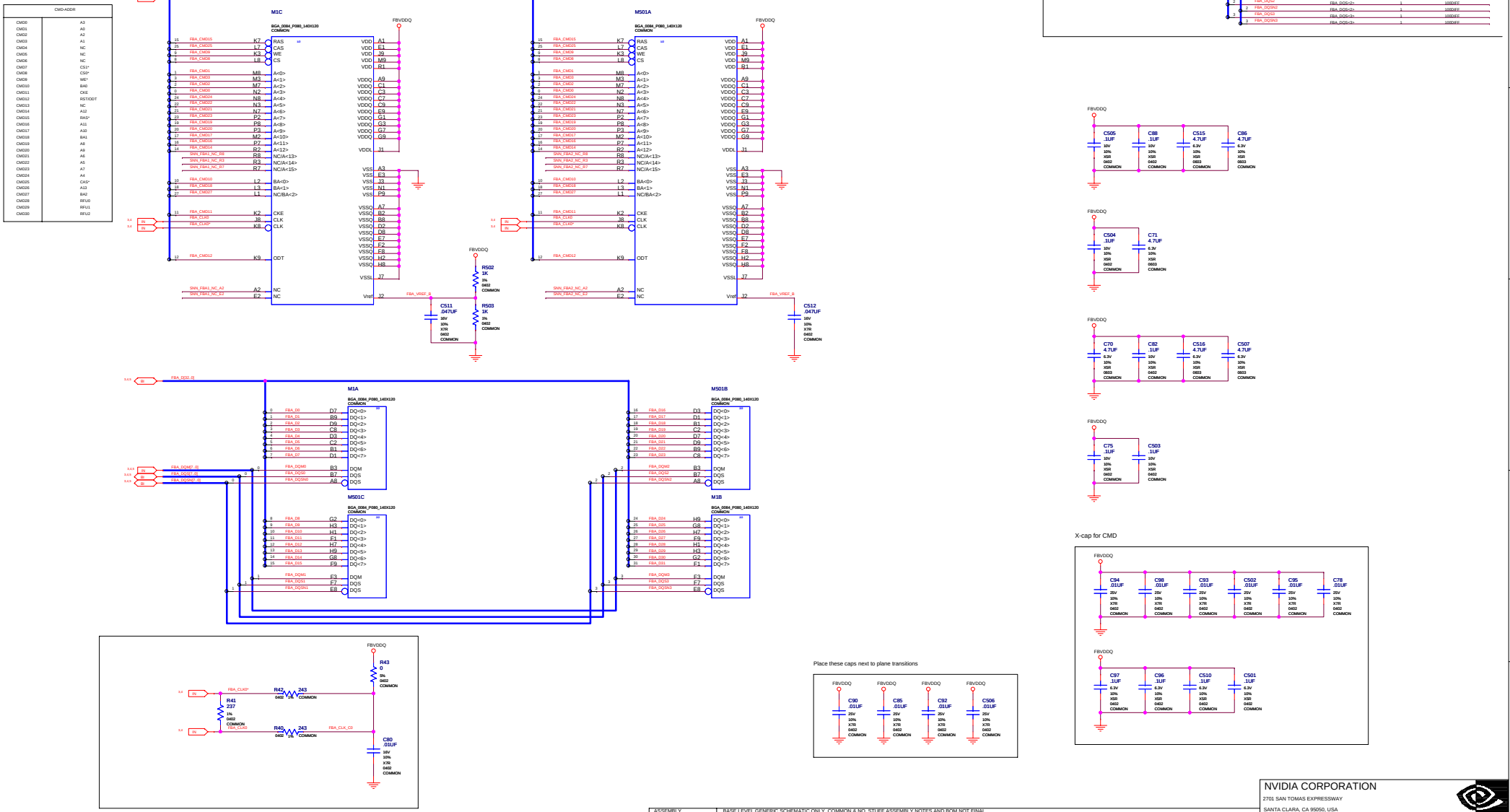
NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
NAME		DATE	31-AUG-2007

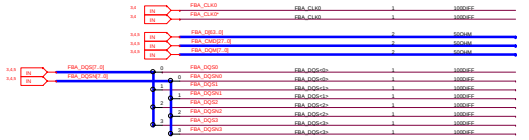
Memory 1st Bank 0..31



CMD-ADDR

CMD0	A3
CMD1	A0
CMD2	A2
CMD3	A1
CMD4	NC
CMD5	NC
CMD6	NC
CMD7	CS1*
CMD8	CS0*
CMD9	WE*
CMD10	BA0
CMD11	CKE
CMD12	RST/ODT
CMD13	NC
CMD14	A12
CMD15	RAS*
CMD16	A11
CMD17	A10
CMD18	BA1
CMD19	A8
CMD20	A9
CMD21	A6
CMD22	A5
CMD23	A7
CMD24	A4
CMD25	CAS*
CMD26	A13
CMD27	BA2
CMD28	RFU0
CMD29	RFU1
CMD30	RFU2

Net Name / DIFF_PAIR / CRITICAL / IMPEDANCE



FBVDDQ

C505 .1UF 10V 10% X5R 0402 COMMON
C88 .1UF 10V 10% X5R 0402 COMMON
C515 4.7UF 6.3V 10% X5R 0603 COMMON
C86 4.7UF 6.3V 10% X5R 0603 COMMON
C504 .1UF 10V 10% X5R 0402 COMMON
C71 4.7UF 6.3V 10% X5R 0603 COMMON
C70 4.7UF 6.3V 10% X5R 0603 COMMON
C82 .1UF 10V 10% X5R 0402 COMMON
C516 4.7UF 6.3V 10% X5R 0603 COMMON
C507 4.7UF 6.3V 10% X5R 0603 COMMON
C75 .1UF 10V 10% X5R 0402 COMMON
C503 .1UF 10V 10% X5R 0402 COMMON

X-cap for CMD

C94 .01UF 25V 10% X7R 0402 COMMON
C98 .01UF 25V 10% X7R 0402 COMMON
C93 .01UF 25V 10% X7R 0402 COMMON
C502 .01UF 25V 10% X7R 0402 COMMON
C95 .01UF 25V 10% X7R 0402 COMMON
C78 .01UF 25V 10% X7R 0402 COMMON
C97 .1UF 6.3V 10% X5R 0402 COMMON
C96 .1UF 6.3V 10% X5R 0402 COMMON
C510 .1UF 6.3V 10% X5R 0402 COMMON
C501 .1UF 6.3V 10% X5R 0402 COMMON

Place these caps next to plane transitions

C90 .01UF 25V 10% X7R 0402 COMMON
C85 .01UF 25V 10% X7R 0402 COMMON
C92 .01UF 25V 10% X7R 0402 COMMON
C506 .01UF 25V 10% X7R 0402 COMMON

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Memory 1st Bank 0..31

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NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
NAME		DATE	31-AUG-2007

Memory 1st Bank 32..63

CMD-ADDR	
CMD0	NC
CMD1	A5
CMD2	NC
CMD3	A1
CMD4	A3
CMD5	A4
CMD6	A5
CMD7	CS1*
CMD8	CS0*
CMD9	WE*
CMD10	BA0
CMD11	CKE
CMD12	RST/ODT
CMD13	A2
CMD14	A12
CMD15	RAS*
CMD16	A11
CMD17	A10
CMD18	BA1
CMD19	A8
CMD20	A9
CMD21	A6
CMD22	NC
CMD23	A7
CMD24	NC
CMD25	CAS*
CMD26	A13
CMD27	BA2
CMD28	RFU0
CMD29	RFU1
CMD30	RFU2

Net Name	DIFF_PAIR	CRITICAL	IMPEDANCE
FBA_CLK1	FBA_CLK1	1	100DIFF
FBA_CLK1*	FBA_CLK1	1	100DIFF
FBA_DQS7_0	FBA_DQS<4>	1	100DIFF
FBA_DQS7_1	FBA_DQS#4	1	100DIFF
FBA_DQ35	FBA_DQS<5>	1	100DIFF
FBA_DQS#5	FBA_DQS<5>	1	100DIFF
FBA_DQ36	FBA_DQS<6>	1	100DIFF
FBA_DQS#6	FBA_DQS<6>	1	100DIFF
FBA_DQ37	FBA_DQS<7>	1	100DIFF
FBA_DQS#7	FBA_DQS<7>	1	100DIFF

Place near signal transition area

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Memory 1st Bank 32..63

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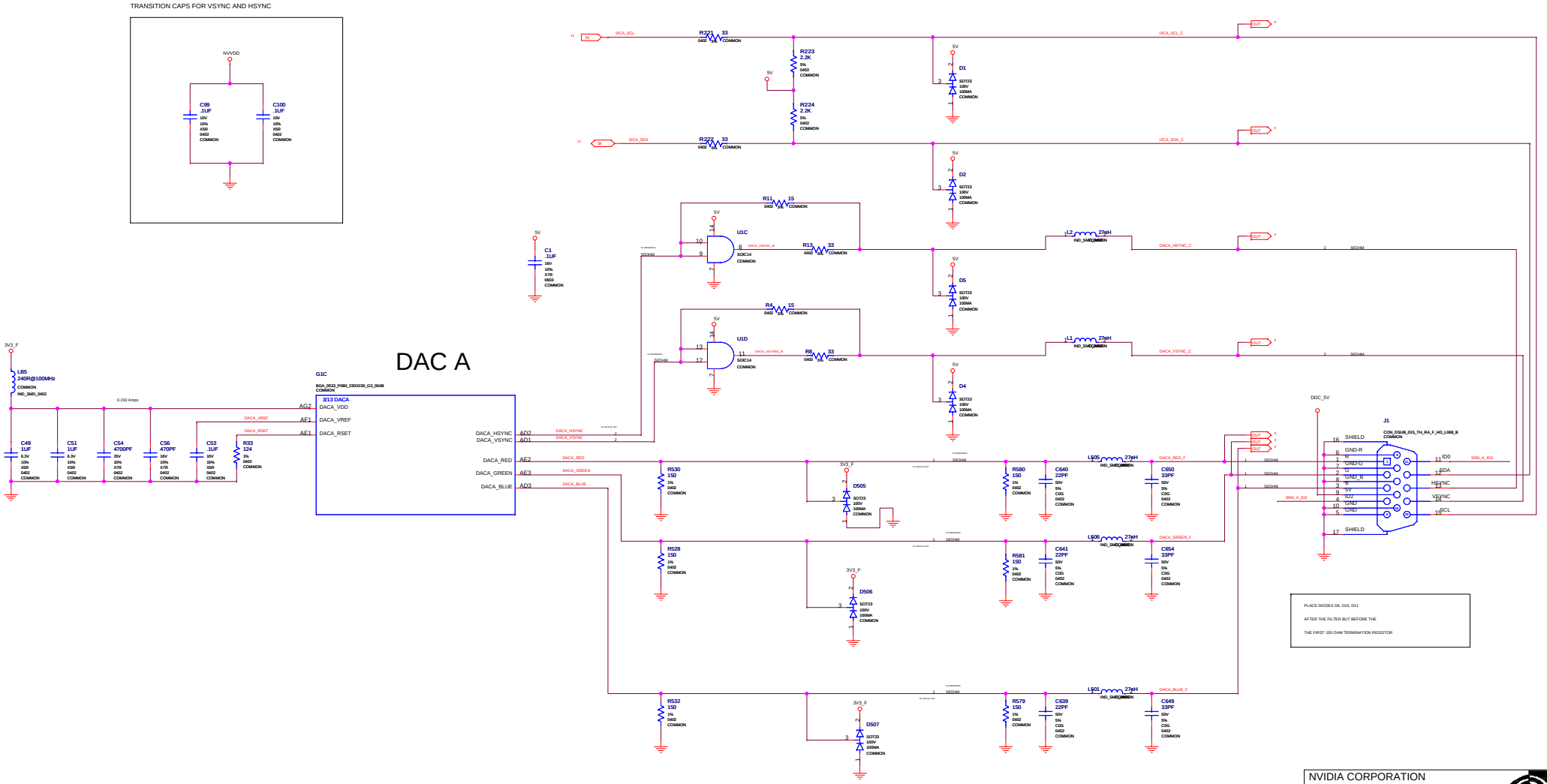
NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
NAME		DATE	31-AUG-2007

DACA, Slim DB15 Connector



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA, Slim DB15 Connector

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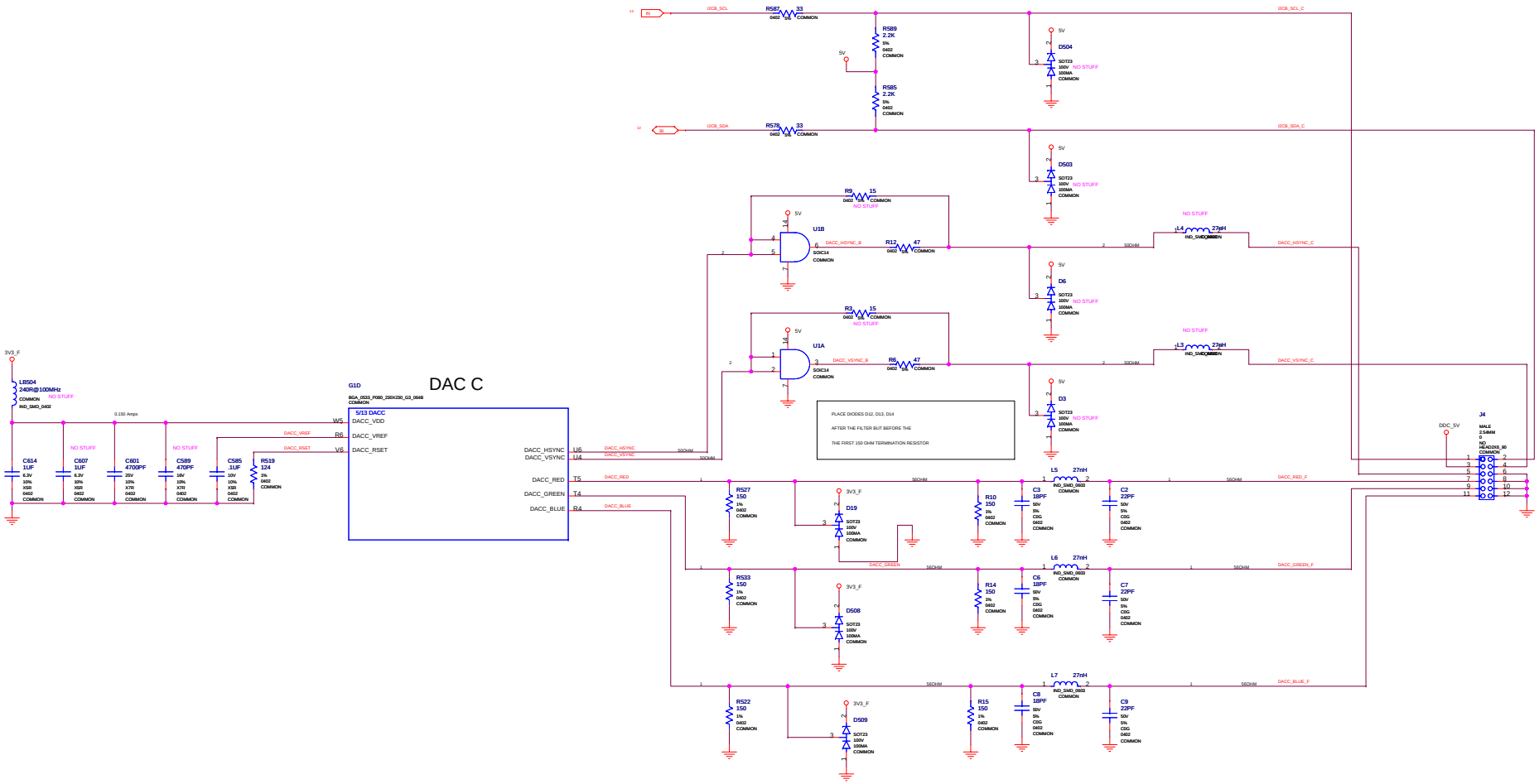
DAC C,2x6 Header



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC,2x6 Header

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NV_PN	600-10561-xxxx-100 D		
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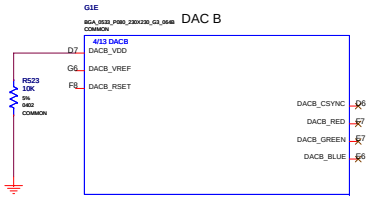
DAC B, 7 PIN MINI-DIN



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	VIDEO CONNECTORS: MiniDIN

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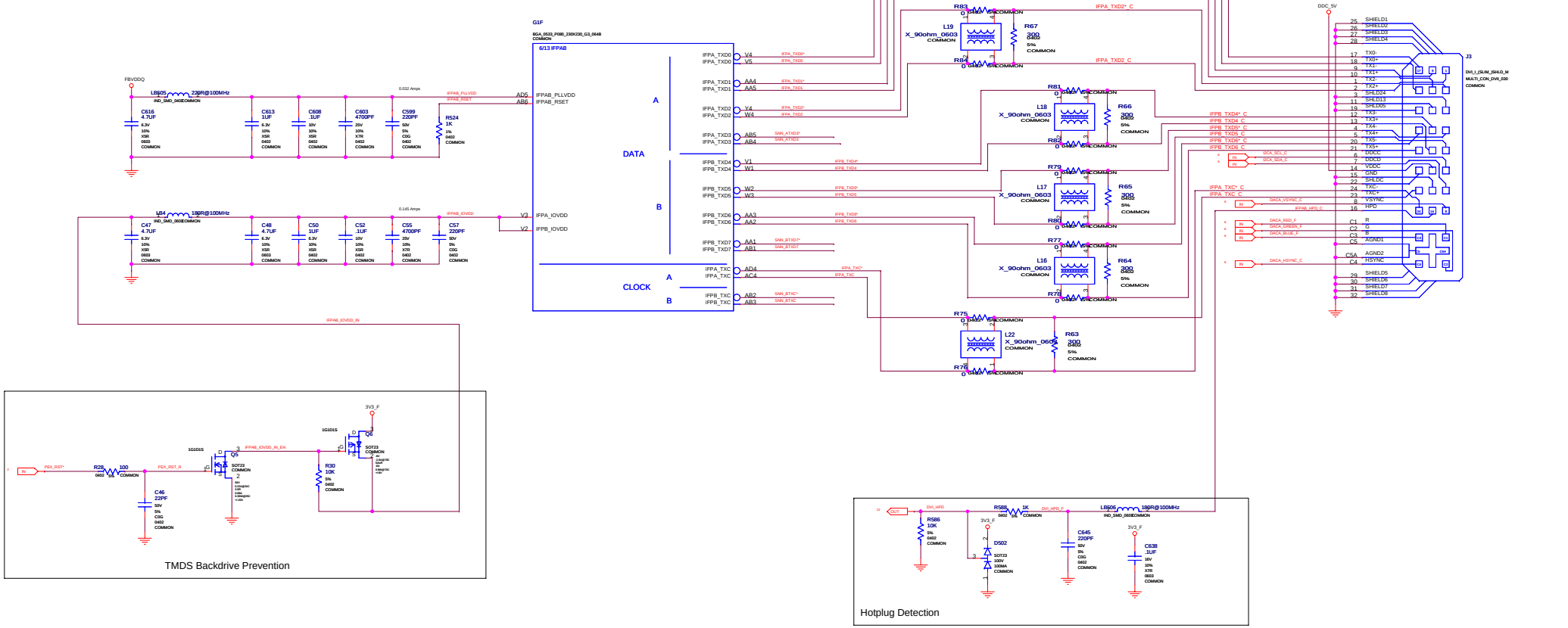
NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
NAME		DATE	31-AUG-2007

TMDS Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS Interface

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NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
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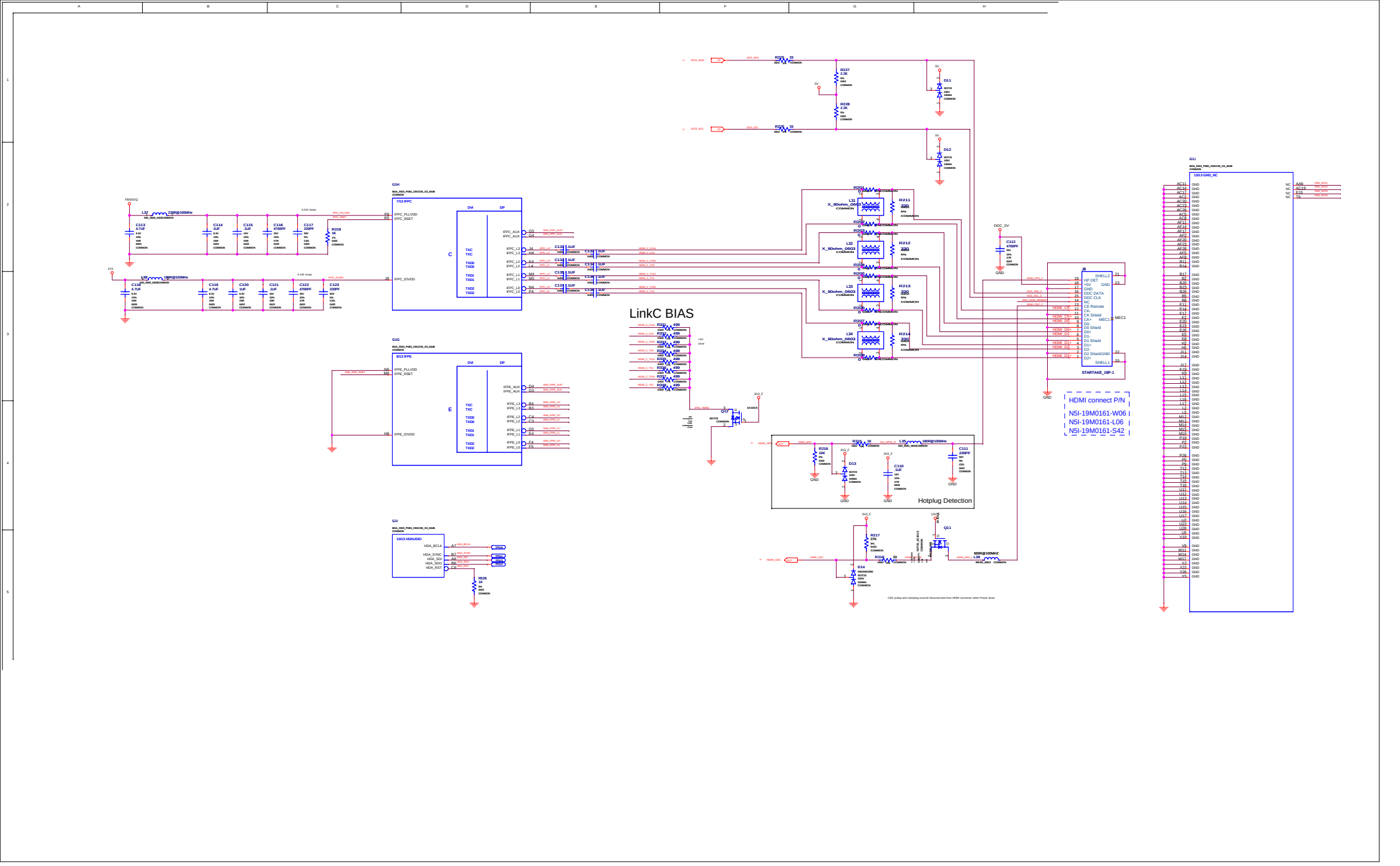
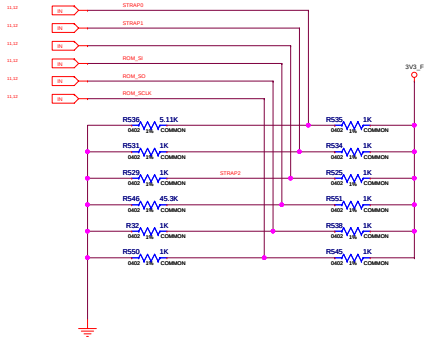

LinkC BIAS
HDMI connect P/N
N5I-19M0161-W06
N5I-19M0161-L06
N5I-19M0161-S42
Hotplug Detection
7/13 IFPC
8/13 IFPE
10/13 HDAUDIO
13/13 GND_NC
STARTAKE_19P-1
HP DET
+5V
DDC DATA
DDC CLK
CE Remote
CK Shield
CK+
D0 Shield
D0+
D1 Shield
D1+
D2 Shield
D2+
SHELL1
SHELL2
MEC1
MEC2

Straps, Mechanical Parts

MULTI LEVEL STRAPS



Each strap pin represents a 4 bit value

Pullup or Pulldown configures the MSB

Resistor Value determines the 3 LSBs

Resistor range is R*n

where n is 0-9 and R is 5K ohm.

Resistor Value	Multilevel	Tied to VCC	Tied to Ground
3 Kohms	Y	1000	0000
6 Kohms	Y	1001	0001
12 Kohms	Y	1010	0010
24 Kohms	Y	1011	0011
48 Kohms	Y	1100	0100
96 Kohms	Y	1101	0101
192 Kohms	Y	1110	0110
284 Kohms	Y	1111	0111
2 Kohms*	N	1xxx	0xxx

STRAPS

1. SUB VENDOR = 1 (ROM PRESENT
   = 0 (NO ROM PRESENT)

2. DEVICE ID FOR GB1-64 = 0x06E2
   a) PCI_DEV_ID = [3..0] LSB = 0010
   B) PCI_DEVID_EXT = [1] 47H BIT = 0

3. 3GIO_PADCFG_LUT_ADR[3..0] = 0000

4. TVMODE[2..0] = 001

5. RAMCFG[3..0] = 0000 16Mx16 DDR2 64 BIT ELPIDA
   = 0001 16Mx16 DDR2 64 BIT SAMSUNG, MICRON
   = 0010 16Mx16 DDR2 64 BIT INFINEON
   = 0011 16Mx16 DDR2 64 BIT HYNIX
   = 0100 32Mx16 DDR2 64 BIT ELPIDA
   = 0101 32Mx16 DDR2 64 BIT SAMSUNG
   = 0110 32Mx16 DDR2 64 BIT INFINEON
   = 0111 32Mx16 DDR2 64 BIT HYNIX

5. USER[3..0] = 0000

MULTI LEVEL MODE

STRAP_CAL_PU_GND0 (R512) = 40K
STRAP_CAL_PU_GND1 (R511) = 40K

SIGNAL	FUNCTION
STRAP[0]	USER[3..0]
STRAP[1]	3GIO_PADCFG_LUT_ADR[3..0]
STRAP[2]	PCI_DEVID[3..0]
ROM_SCLK	PCI_DEVID_EXT, SUB_VENDOR, SLOT_CLK_CFG, PEX_PLL_EN_TERM100
ROM_SI	RAMCFG[3..0]
ROM_SO	XCLK_277, TVMODE[2..0]

BRINGUP BINARY MODE

STRAP_CAL_PU_GND0 (R512) = NO STUFF
STRAP_CAL_PU_GND1 (R511) = NO STUFF

SIGNAL	FUNCTION
STRAP[0]	3G10_PADCFG_LUT_ADR[0]
STRAP[1]	3G10_PADCFG_LUT_ADR[1]
STRAP[2]	3G10_PADCFG_LUT_ADR[2]
ROM_SCLK	3G10_PADCFG_LUT_ADR[3]
ROM_SI	SUB VENDOR
ROM_SO	XCLK_277

PRODUCTION BINARY MODE

STRAP_CAL_PU_GND0 (R512) = NO STUFF
STRAP_CAL_PU_GND1 (R511) = 40K

SIGNAL	FUNCTION
STRAP[0]	RAMCFG[0]
STRAP[1]	RAMCFG[1]
STRAP[2]	RAMCFG[2]
ROM_SCLK	PCI_DEVID[2]
ROM_SI	PCI_DEVID_EXT
ROM_SO	XCLK_277

STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz (MULTI LEVEL) R511= 40K, R512=40K

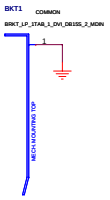
3V3_F	GND	PIN(SIGNAL)	FUNCTION
	5K	STRAP[0]	USER[3..0]
	5K	STRAP[1]	3GIO_PADCFG_LUT_ADR[3..0]
	25K	STRAP[2]	PCI_DEVID[3..0]
	25K	ROM_SCLK	PCI_DEVID_EXT, SUB_VENDOR, SLOT_CLK_CFG, PEX_PLL_EN_TERM100
25K	45K	ROM_SI	RAMCFG[3..0]
		ROM_SO	XCLK_277, TVMODE[2..0]

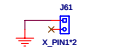
STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz (BRINGUP BINARY) R511= NO STUFF, R512=NO STUFF

3V3_F	GND	PIN(SIGNAL)	FUNCTION
	5K	STRAP[0]	3G10_PADCFG_LUT_ADR[0]
	5K	STRAP[1]	3G10_PADCFG_LUT_ADR[1]
	5K	STRAP[2]	3G10_PADCFG_LUT_ADR[2]
	5K	ROM_SCLK	3G10_PADCFG_LUT_ADR[3]
5K		ROM_SI	SUB VENDOR
5K		ROM_SO	XCLK_277

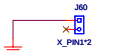
STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz (PRODUCTION BINARY) R511= 40K, R512= NO STUFF

3V3_F	GND	PIN(SIGNAL)	FUNCTION
5K		STRAP[0]	RAMCFG[0]
5K		STRAP[1]	RAMCFG[1]
5K		STRAP[2]	RAMCFG[2]
	5K	ROM_SCLK	PCI_DEVID[3]
	5K	ROM_SI	PCI_DEVID_EXT
5K		ROM_SO	XCLK_277

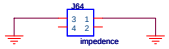




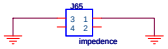
M502
FBA_D39
BOT
4.63mil / 50ohm
Reference GND



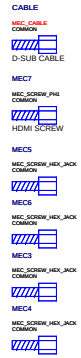
FBA_CMD17
BOT
3.6mil / 56ohm
Reference GND*

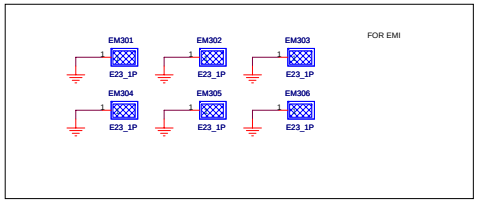


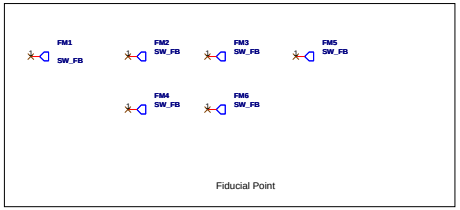
HDMI J8
HDMI_C_TX0/TX0#
BOT
3.5/5.7mil / 100ohm
Reference GND



DVI J3
IFPA_TXD1/TXD1*
BOT
3.5/5.7mil / 100ohm
Reference GND





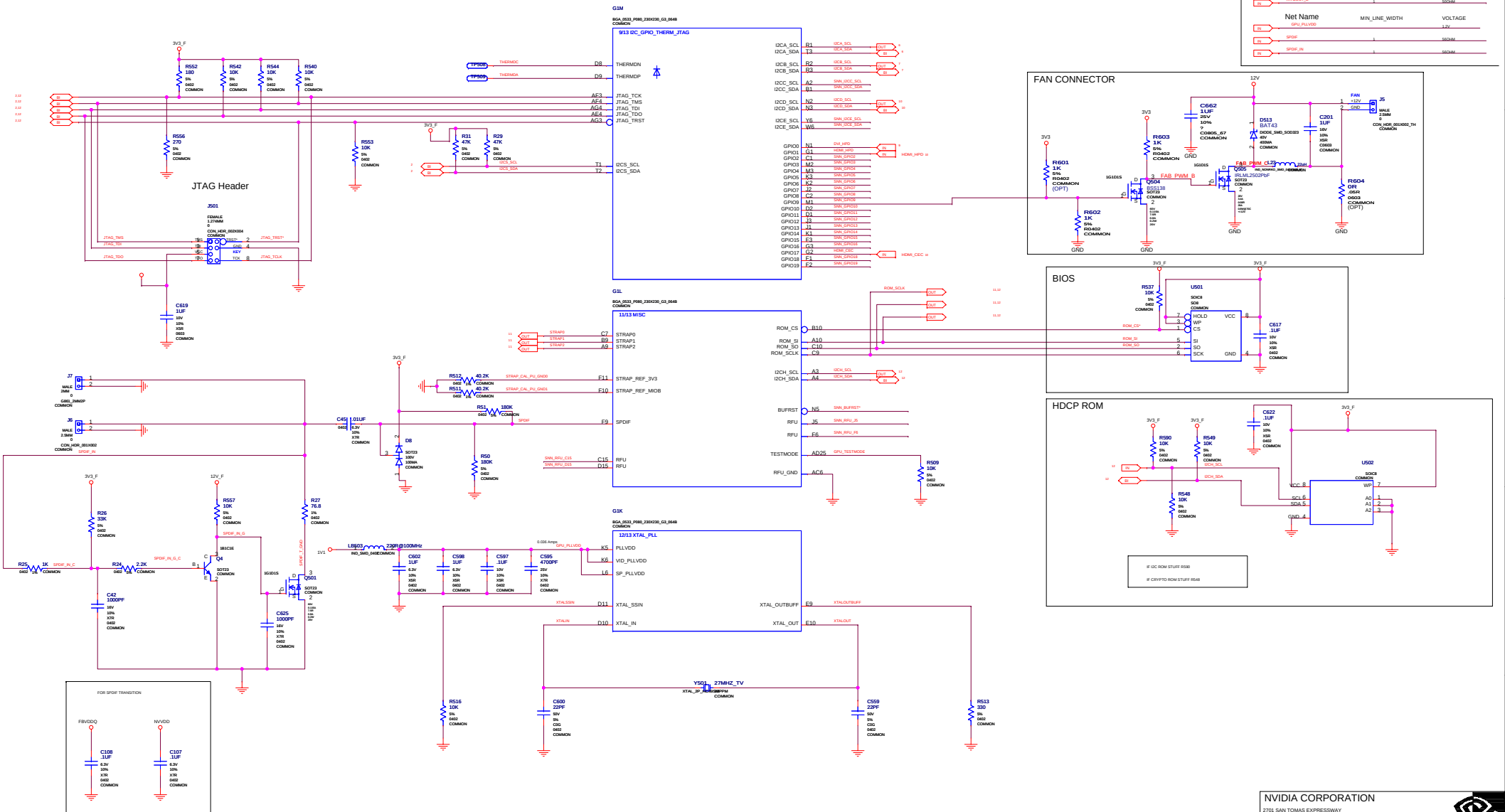


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Straps, Mechanical Parts

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
NAME		DATE	31-AUG-2007

XTAL, GPIO, BIOS, FAN, JTAG, HDCP, SPDIF



Net Name	CRITICAL	IMPEDANCE
XTALIN	1	50OHM
XTALOUT	1	50OHM
XTALIN_T	1	50OHM
XTALOUT_T	1	50OHM
XTALIN_B	1	50OHM
XTALOUT_B	1	50OHM

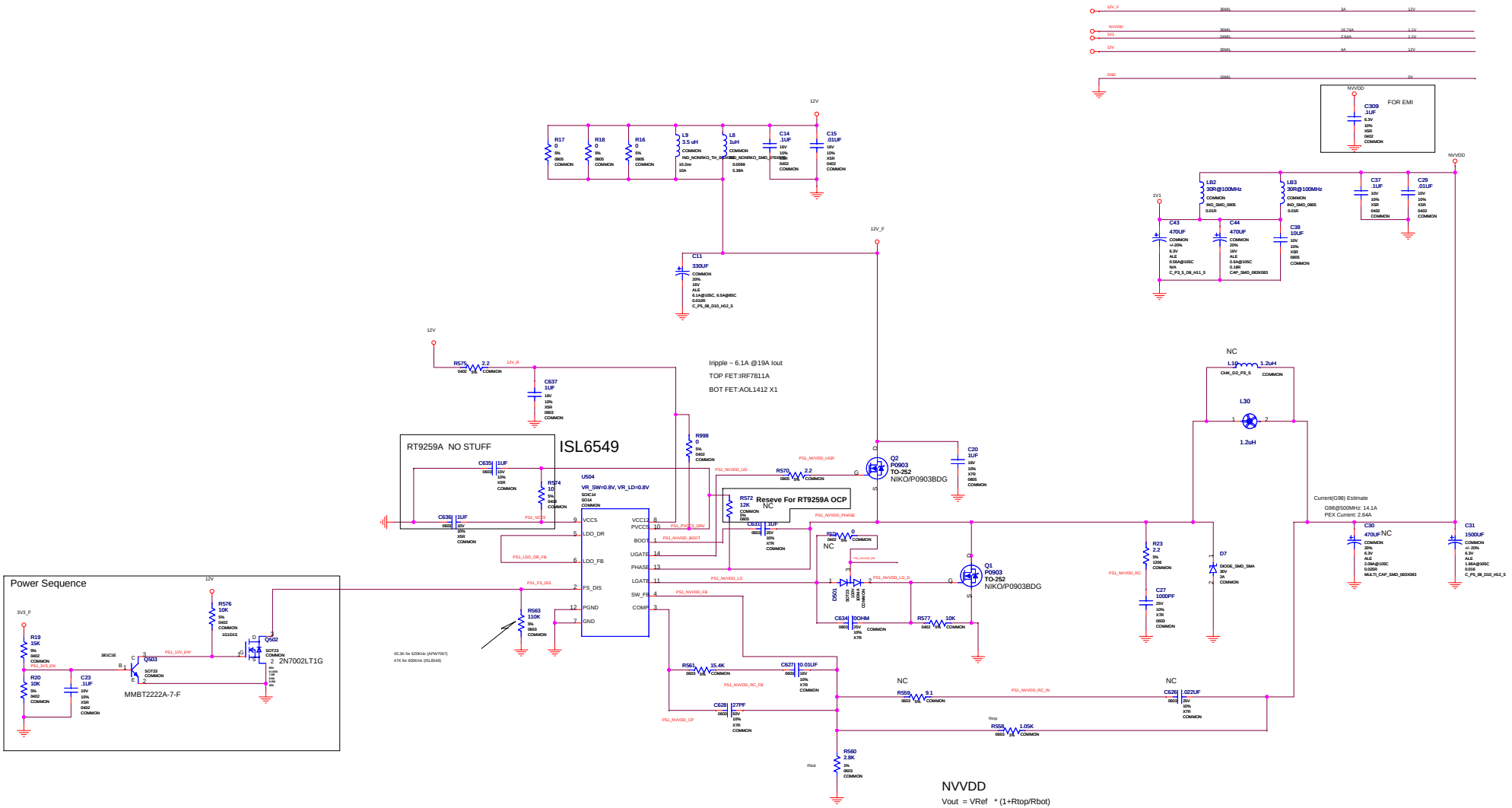
Net Name	MIN_LINE_WIDTH	VOLTAGE
GPU_PLLVDD	-	1.2V
SPDIF	1	5OHM
SPDIF_IN	1	5OHM

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, GPIO, BIOS, FAN, JTAG, HDCP, SPDIF

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
NAME		DATE	31-AUG-2007

Power Supply I: NVVDD, PLLVDD



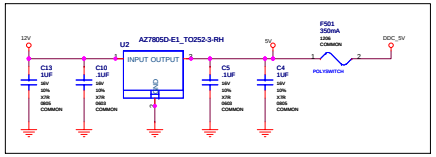
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply I: NVVDD, PLLVDD

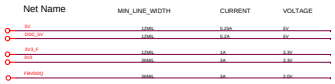
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
NAME		DATE	31-AUG-2007

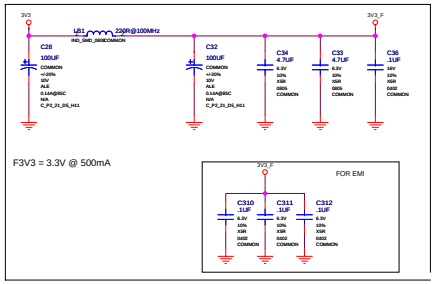
Power Supply II: 5V, DDC5V, F3V3, FBVDDQ

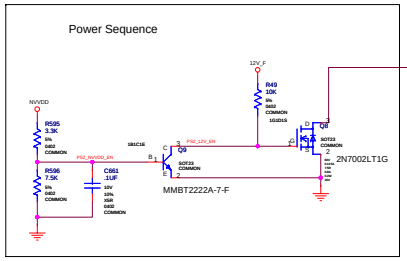
5V, DDC5V

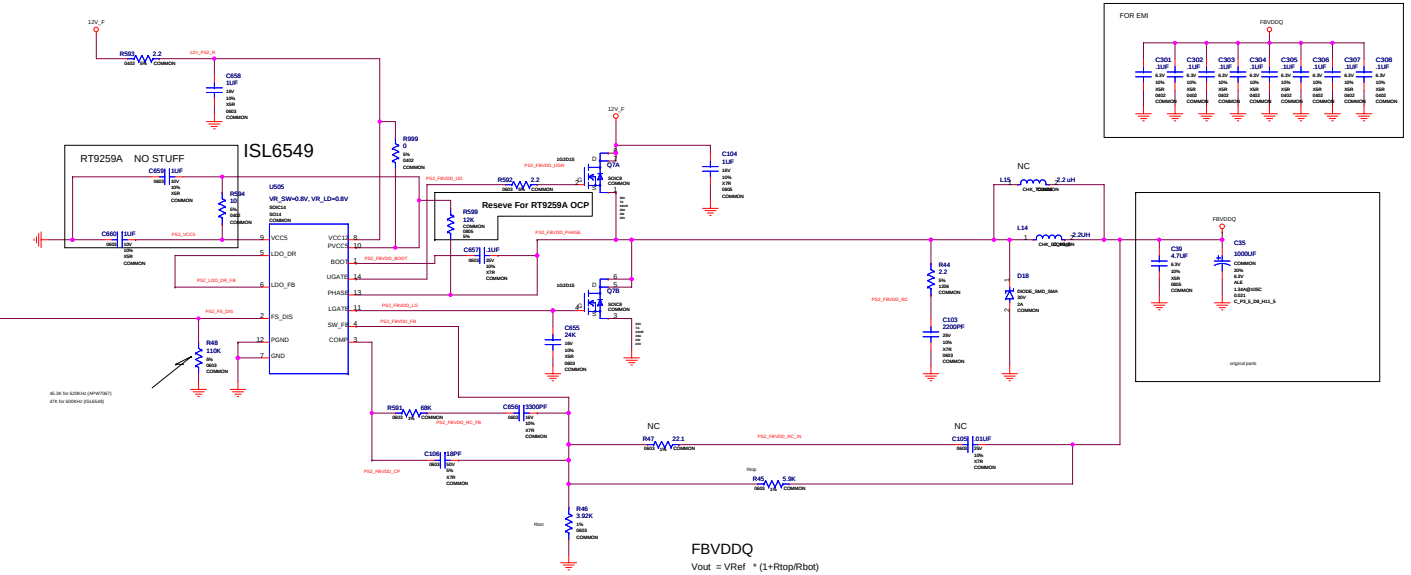




F3V3







FBVDDQ

Vout = VRef * (1+Rtop/Rbot)

1.800V = 0.8V * (1+(5.9K/4.7K)) (ISL6549)

2.000V = 0.8V * (1+(5.9k/3.92k)) (ISL6549)

2.156V = 0.8V * (1+(5.9k/3.4k)) (ISL6549)

Title: Basenet Report
Design: p561
Date: Aug 15 1:38:59 2007

Base nets and synonyms for
p561_lib.P561(@p561_lib.p561(sch_1))
Base Signal Location([Zone][dir])

1V1 13.1F
3V3 14.1G
3V3_F 14.1G
5V 14.1G
12V 13.1F
12V_F 13.1F
12V_PS2_R 14.2C
12V_R 13.3C
DACA_BLUE 6.4C
DACA_BLUE_F 6.4G> 9.3G<
DACA_GREEN 6.4C
DACA_GREEN_F 6.3G> 9.3G<
DACA_HSYNC 6.3C
DACA_HSYNC_B 6.2D
DACA_HSYNC_C 6.2G> 9.3G<
DACA_RED 6.4C
DACA_RED_F 6.3G> 9.3G<
DACA_RSET 6.3B
DACA_VREF 6.3B
DACA_VSYNC 6.3C
DACA_VSYNC_C 6.3G> 9.3G<
DACA_VSYNC_B 6.3D
DACB_BLUE 8.4D
DACB_COUT 8.4F
DACB_CVBS_OUT 8.3F 8.4G
DACB_GREEN 8.4D
DACB_PB_OUT 8.4F
DACB_RED 8.3D
DACB_RSET 8.3B
DACB_VREF 8.3B
DACC_BLUE 7.4C 7.4E
DACC_BLUE_F 7.4F
DACC_GREEN 7.4C 7.4E
DACC_GREEN_F 7.4F
DACC_HSYNC 7.3C
DACC_HSYNC_B 7.2D
DACC_HSYNC_C 7.2F
DACC_RED 7.4C 7.4E
DACC_RED_F 7.4F
DACC_RSET 7.3B
DACC_VREF 7.3B
DACC_VSYNC 7.3C
DACC_VSYNC_B 7.3D
DACC_VSYNC_C 7.3F
DDC_5V 14.1G
DVI_HPD 9.3E> 12.2E<
DVI_HPD_F 9.3F
FBA_CLK0 3.3D> 3.3D 4.1G<
4.2A< 4.2C< 4.5B<
FBA_CLK0* 3.3D 3.4D> 4.1G<
4.2A< 4.2C< 4.5B<
FBA_CLK1 3.3D 3.4D> 5.1G<
5.2A< 5.2C< 5.5B<
FBA_CLK1* 3.3D 3.4D> 5.1G<
5.2A< 5.2C< 5.5B<
FBA_CLK_C0 4.5B
FBA_CLK_C1 5.5B
FBA_CMD<0> 3.2C 3.2F 4.2B 4.2C
FBA_CMD<27..0> 3.2D> 4.1A< 4.1G<
5.1A<
FBA_CMD<1> 3.2C 3.2F 4.1B 4.1C
5.1B 5.1C
FBA_CMD<2> 3.2C 3.2G 4.1B 4.1C
FBA_CMD<3> 3.2C 3.2G 4.1B 4.1C
5.1B 5.1C
FBA_CMD<4> 3.2C 3.2F 5.2B 5.2C
FBA_CMD<5> 3.2C 3.2F 5.2B 5.2C
FBA_CMD<6> 3.2G 3.3C 5.2B 5.2C
FBA_CMD<8> 3.2G 3.3C 4.1B 4.1C
5.1B 5.1C
FBA_CMD<9> 3.2F 3.3C 4.1B 4.1C
5.1B 5.1C
FBA_CMD<10> 3.3C 3.3F 4.2B 4.2C
5.2B 5.2C
FBA_CMD<11> 3.3C 3.3D 4.2B 4.2C
5.2B 5.2C
FBA_CMD<12> 3.3C 3.3D 4.2B 4.2C
5.2B 5.2C
FBA_CMD<13> 3.2G 3.3C 5.1B 5.1C
FBA_CMD<14> 3.3C 3.3G 4.2B 4.2C
5.2B 5.2C
FBA_CMD<15> 3.3C 3.3F 4.1B 4.1C
5.1B 5.1C
FBA_CMD<16> 3.3C 3.3F 4.2B 4.2C
5.2B 5.2C
FBA_CMD<17> 3.3C 3.3G 4.2B 4.2C
5.2B 5.2C
FBA_CMD<18> 3.3C 3.3G 4.2B 4.2C
5.2B 5.2C
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5.2B 5.2C
FBA_CMD<20> 3.3C 3.3F 4.2B 4.2C
5.2B 5.2C
FBA_CMD<21> 3.3C 3.3G 4.2B 4.2C
5.2B 5.2C
FBA_CMD<22> 3.3C 3.3G 4.2B 4.2C
FBA_CMD<23> 3.3C 3.4F 4.2B 4.2C
5.2B 5.2C
FBA_CMD<24> 3.3C 3.4F 4.2B 4.2C
FBA_CMD<25> 3.3C 3.4G 4.1B 4.1C
5.1B 5.1C
FBA_CMD<27> 3.3C 3.4G 4.2B 4.2C
5.2B 5.2C
FBA_D<0> 3.1B 4.3B
FBA_D<32..0> 4.3A<>
3.1A<> 4.1G< 5.3A<>
FBA_D<63..0> 3.1A<> 4.1G< 5.3A<>
FBA_D<1> 3.1B 4.3B
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FBA_D<3> 3.1B 4.3B
FBA_D<4> 3.1B 4.3B
FBA_D<5> 3.1B 4.3B
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FBA_D<7> 3.1B 4.3B
FBA_D<8> 3.1B 4.4B
FBA_D<9> 3.1B 4.4B
FBA_D<10> 3.1B 4.4B
FBA_D<11> 3.1B 4.4B
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FBA_D<19> 3.2B 4.3D
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FBA_D<21> 3.2B 4.3D
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5.4A<
FBA_DQM<1> 3.3B 4.4B
FBA_DQM<2> 3.3B 4.3D
FBA_DQM<3> 3.3B 4.4D
FBA_DQM<4> 3.3B 5.3B
FBA_DQM<5> 3.3B 5.4B
FBA_DQM<6> 3.3B 5.3D
FBA_DQM<7> 3.3B 5.4D
FBA_DQS<0> 3.4B 4.1G 4.4B
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5.1G< 5.4A<
FBA_DQS<1> 3.4B 4.1G 4.4B
FBA_DQS<2> 3.4B 4.1G 4.4D
FBA_DQS<3> 3.4B 4.1G 4.4D
FBA_DQS<4> 3.4B 5.1G 5.4B
FBA_DQS<5> 3.4B 5.1G 5.4B
FBA_DQS<6> 3.4B 5.1G 5.4D
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FBA_DQSN<0> 3.4B 4.1G 4.4B
FBA_DQSN<7..0> 3.4A<> 4.1G< 4.4A<>
5.1G< 5.4A<
FBA_DQSN<1> 3.4B 4.1G 4.4B
FBA_DQSN<2> 3.4B 4.1G 4.4D
FBA_DQSN<3> 3.4B 4.1G 4.4D
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FBA_DQSN<6> 3.4B 5.1G 5.4D
FBA_DQSN<7> 3.4B 5.1G 5.4D
FBA_PLLAVDD 3.5C
FBA_VREF_A 5.3C 5.3E
FBA_VREF_B 4.3C 4.3E
FBVDDQ 14.1G
FB_CAL_PD_VDDQ 3.4C
FB_CAL_PU_GND 3.4C
FB_CAL_TERM_GND 3.4C
FB_VREF 3.5B
GND_SENSE 2.4F
GPU_PLLVDD 12.1G< 12.4C
GPU_TESTMODE 12.3E
HDA_BCLK 10.4C
HDA_RST 10.4C
HDA_SDI 10.4C
HDA_SDO 10.4C
HDA_SYNC 10.4C
I2CA_SCL 6.1D< 12.1E>
I2CA_SCL_C 6.1G> 9.2G<
I2CA_SDA 6.2D<> 12.1E<>
I2CA_SDA_C 6.2G> 9.3G<
I2CB_SCL 7.1D< 12.1E>
I2CB_SCL_C 7.1F
I2CB_SDA 7.2D<> 12.1E<>
I2CB_SDA_C 7.2F
I2CH_SCL 12.3E> 12.3F<
I2CH_SDA 12.3E<> 12.3F<>
I2CS_SCL 2.1E<> 12.2C<>
I2CS_SDA 2.1E<> 12.2C<>
IFPAB_HPD_C 9.3G
IFPAB_IOVDD 9.1G< 9.3C
IFPAB_IOVDD_IN 9.2G< 9.3B
IFPAB_IOVDD_IN_EN 9.4B
IFPAB_PLLVDD 9.1G< 9.2C
IFPAB_RSET 9.2C
IFPA_TXC 9.1G< 9.3E 9.3G
IFPA_TXC* 9.1G< 9.3E 9.3G
IFPA_TXD0 9.1G< 9.2E 9.2G
IFPA_TXD0* 9.1G< 9.2E 9.2G
IFPA_TXD1 9.1G< 9.2E 9.2G
IFPA_TXD1* 9.1G< 9.2E 9.2G
IFPA_TXD2 9.1G< 9.2E 9.2G
IFPA_TXD2* 9.1G< 9.2E 9.2G
IFPB_TXD4 9.1G< 9.2G 9.3E
IFPB_TXD4* 9.1G< 9.2E 9.2G
IFPB_TXD5 9.1G< 9.2G 9.3E
IFPB_TXD5* 9.1G< 9.2G 9.3E
IFPB_TXD6 9.1G< 9.2G 9.3E
IFPB_TXD6* 9.1G< 9.2G 9.3E
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12.1A<>
JTAG_TCLK_PEX 2.1C
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12.2A<>
JTAG_TDIO_PEX 2.1C
JTAG_TDO 2.1E<> 12.2A<>
12.2A<>
JTAG_TDO_PEX 2.1C
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12.1A<>
JTAG_TMS_PEX 2.1C
JTAG_TRST* 2.1E<> 12.2A<>
12.2A<>
JTAG_TRST_PEX* 2.1C
NVVDD 13.1F
NVVDD_SENSE 2.4F
PEX_PLLDVDD 2.5F
PEX_PRSNT 2.1B
PEX_REFCLK 2.2C 2.5A<
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PEX_RST* 2.2D> 2.2D> 9.4A<
PEX_RST_R 9.4A
PEX_RSVD 2.5F
PEX_RX0 2.2C 2.4A<
PEX_RX0* 2.2C 2.4A<
PEX_RX1 2.2C 2.4A<
PEX_RX1* 2.2C 2.4A<
PEX_RX2 2.2C 2.4A<
PEX_RX2* 2.2C 2.4A<
PEX_RX3 2.3C 2.4A<
PEX_RX3* 2.3C 2.4A<
PEX_RX4 2.3C 2.4A<
PEX_RX4* 2.3C 2.4A<
PEX_RX5 2.3C 2.5A<
PEX_RX5* 2.3C 2.5A<
PEX_RX6 2.3C 2.5A<
PEX_RX6* 2.3C 2.5A<
PEX_RX7 2.3C 2.5A<
PEX_RX7* 2.3C 2.5A<
PEX_RX8 2.4C 2.5A<
PEX_RX8* 2.4C 2.5A<
PEX_RX9 2.4C 2.5A<
PEX_RX9* 2.4C 2.5A<
PEX_RX10 2.4C 2.5A<
PEX_RX10* 2.4C 2.5A<
PEX_RX11 2.4C 2.5A<
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PS1_NVVDD_BOOT 13.3D
PS1_NVVDD_CP 13.4D
PS1_NVVDD_DR 13.4E
PS1_NVVDD_FB 13.4D
PS1_NVVDD_LG 13.4D
PS1_NVVDD_LG_D 13.4E
PS1_NVVDD_PHASE 13.3E
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PS1_NVVDD_RC_FB 13.4D
PS1_NVVDD_RC_IN 13.4F
PS1_NVVDD_UG 13.3D
PS1_NVVDD_UGR 13.3E
PS1_PVCC5_DRV 13.3D
PS1_VCC5 13.3C
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PS2_FBVDD_CP 14.4D
PS2_FBVDD_FB 14.3D
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SNN_BTXC* 9.3E
SNN_BTXD7 9.3E
SNN_BTXD7* 9.3E
SNN_BUFRST* 12.3E
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SNN_TV_NC2 8.4G
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SPDIF_T_GND 12.4B
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NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
NAME	<ENGINEER>	DATE	31-AUG-2007

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NV_PN	600-10561-xxxx-100 D		
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