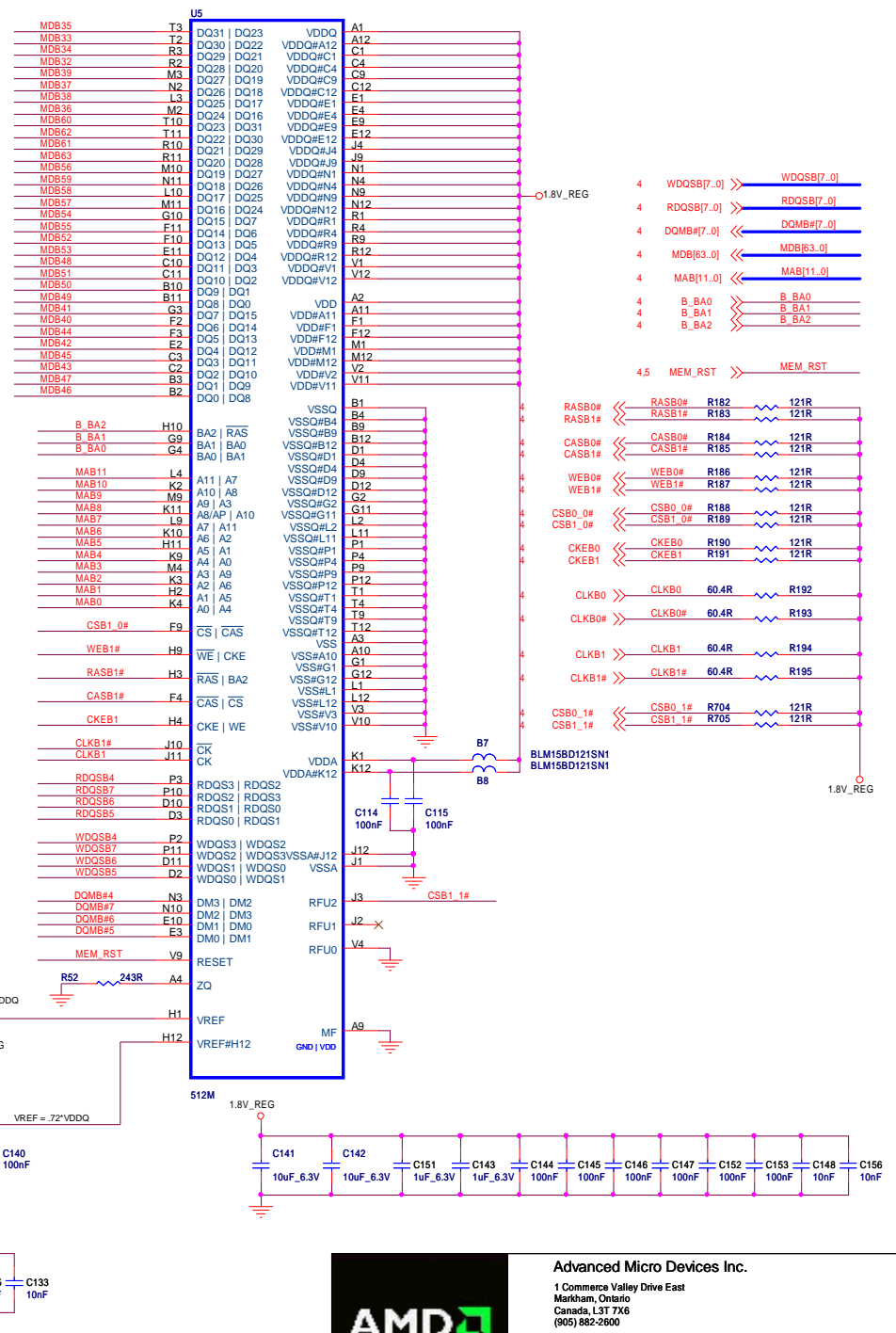
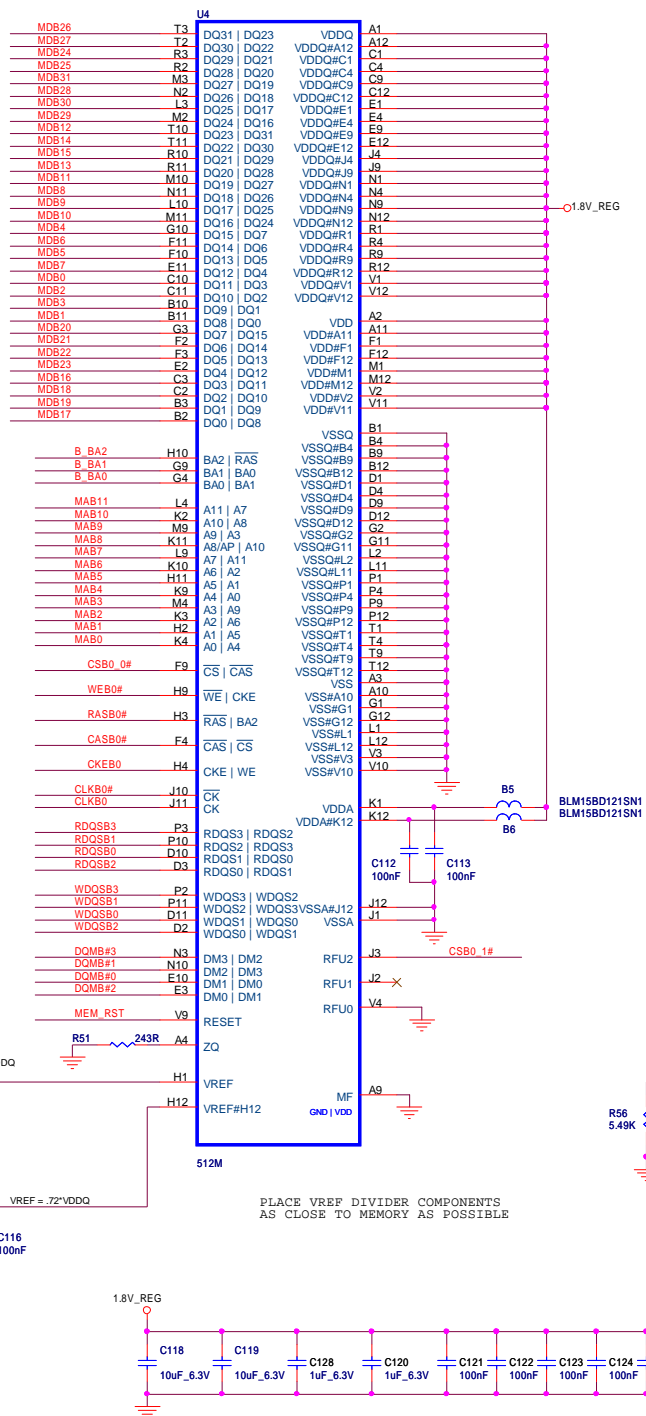




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PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE

G\_PWR\_SRC

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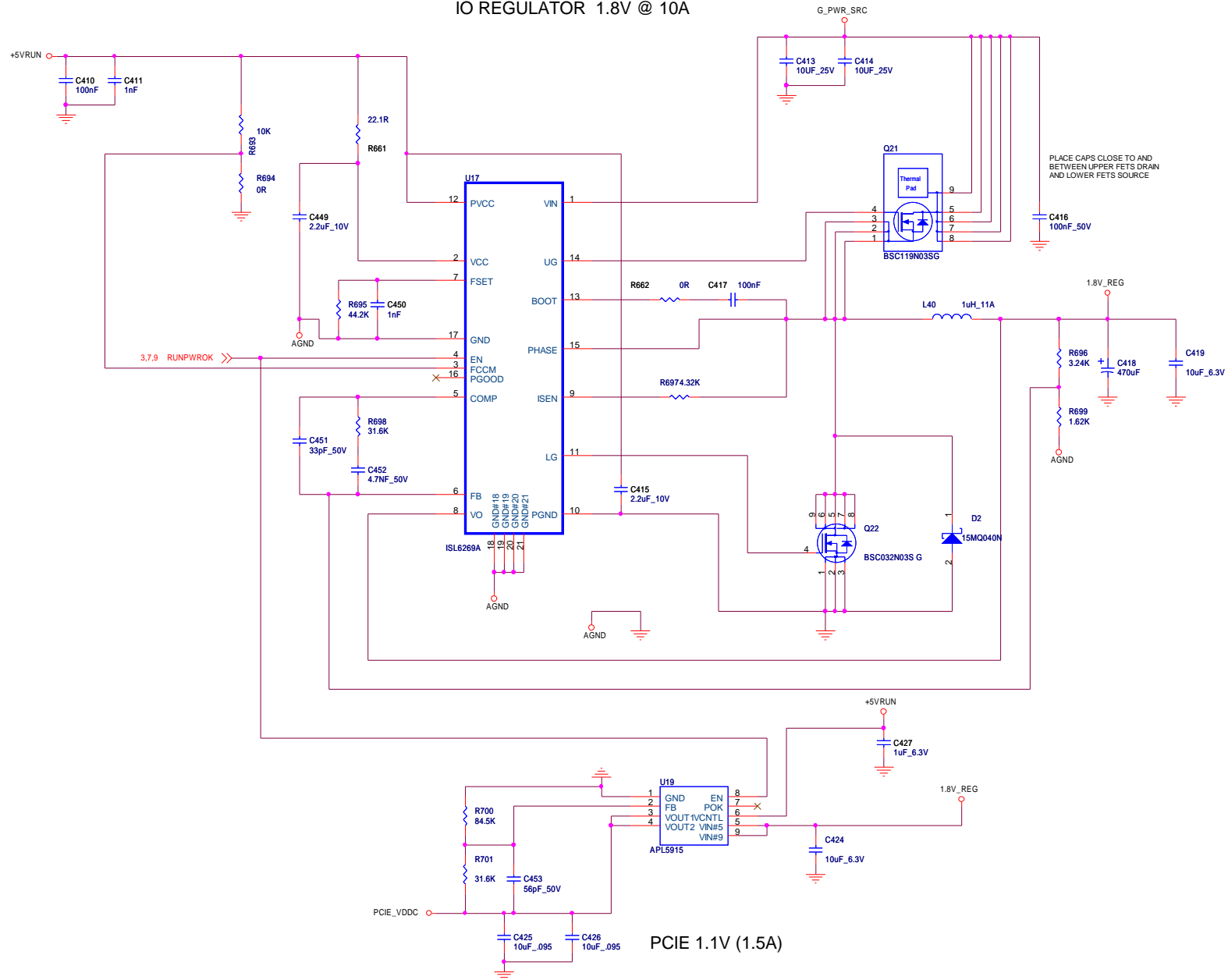
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# IO REGULATOR 1.8V @ 10A

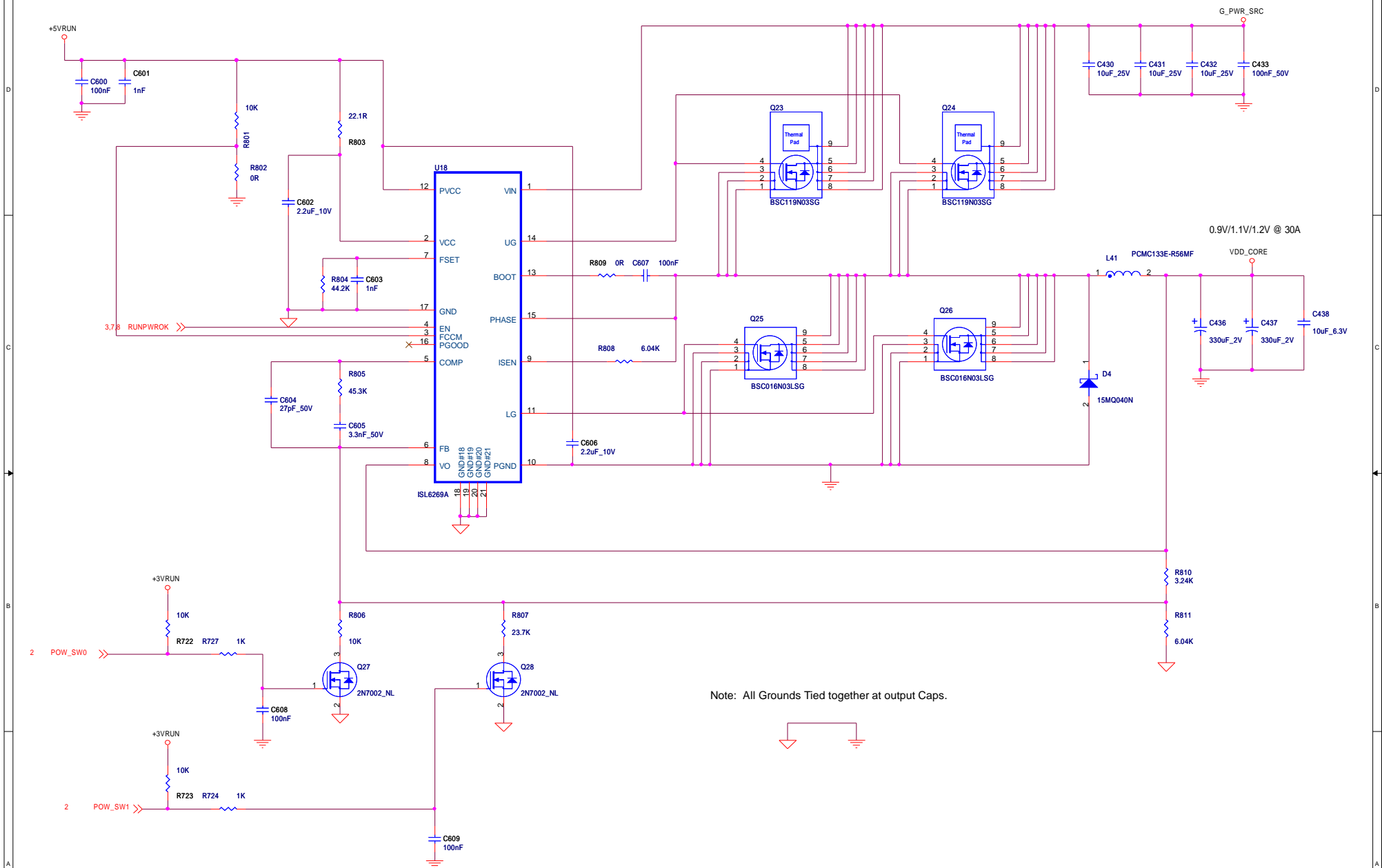


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# CORE PWM REGULATOR .9V - 1.2V @ 30A

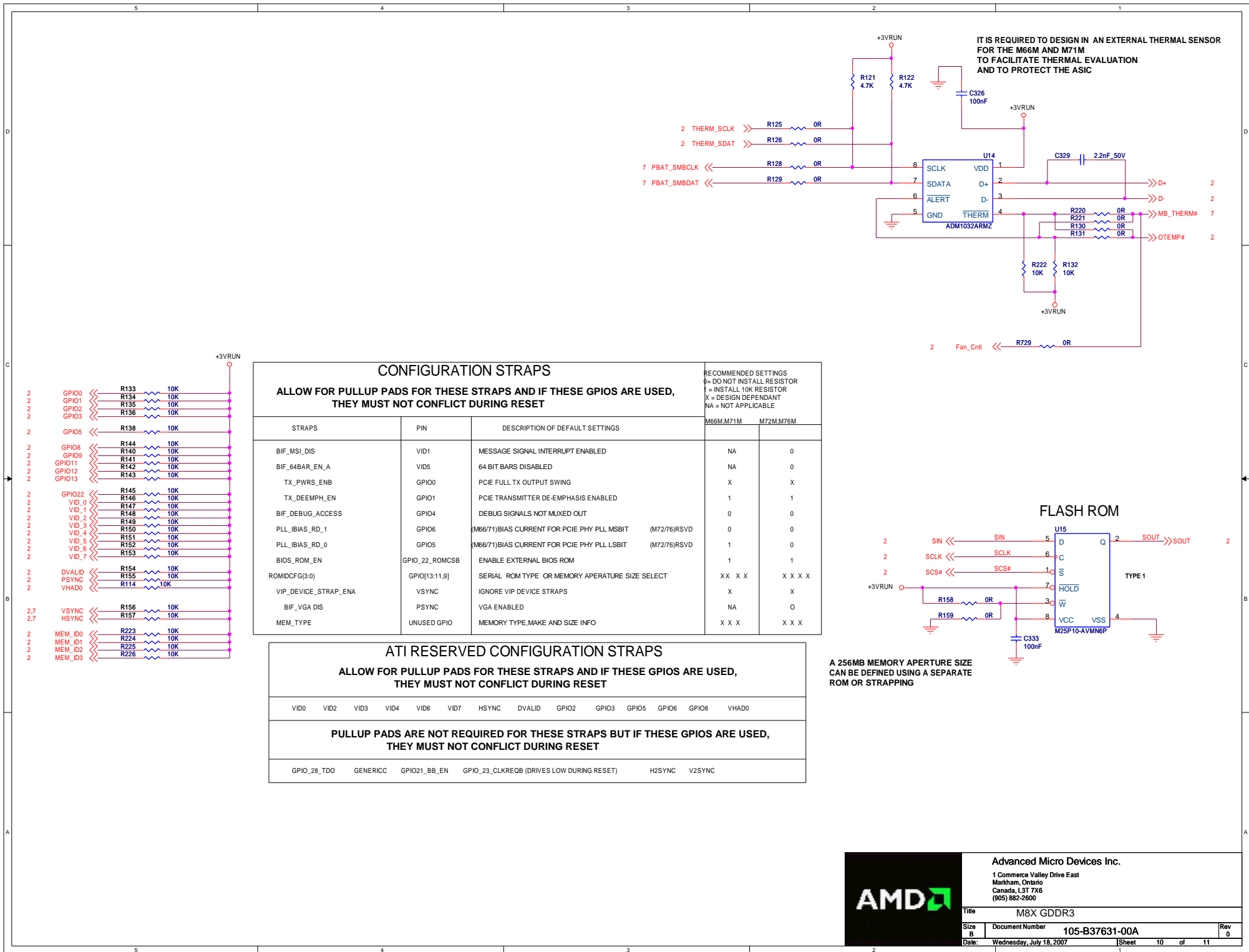



Note: All Grounds Tied together at output Caps.



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					Title M8X GDDR2										Schematic No. 105-B37631-00A					Date: Wednesday, July 18, 2007																			
					REVISION HISTORY										NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.										Rev 0														
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