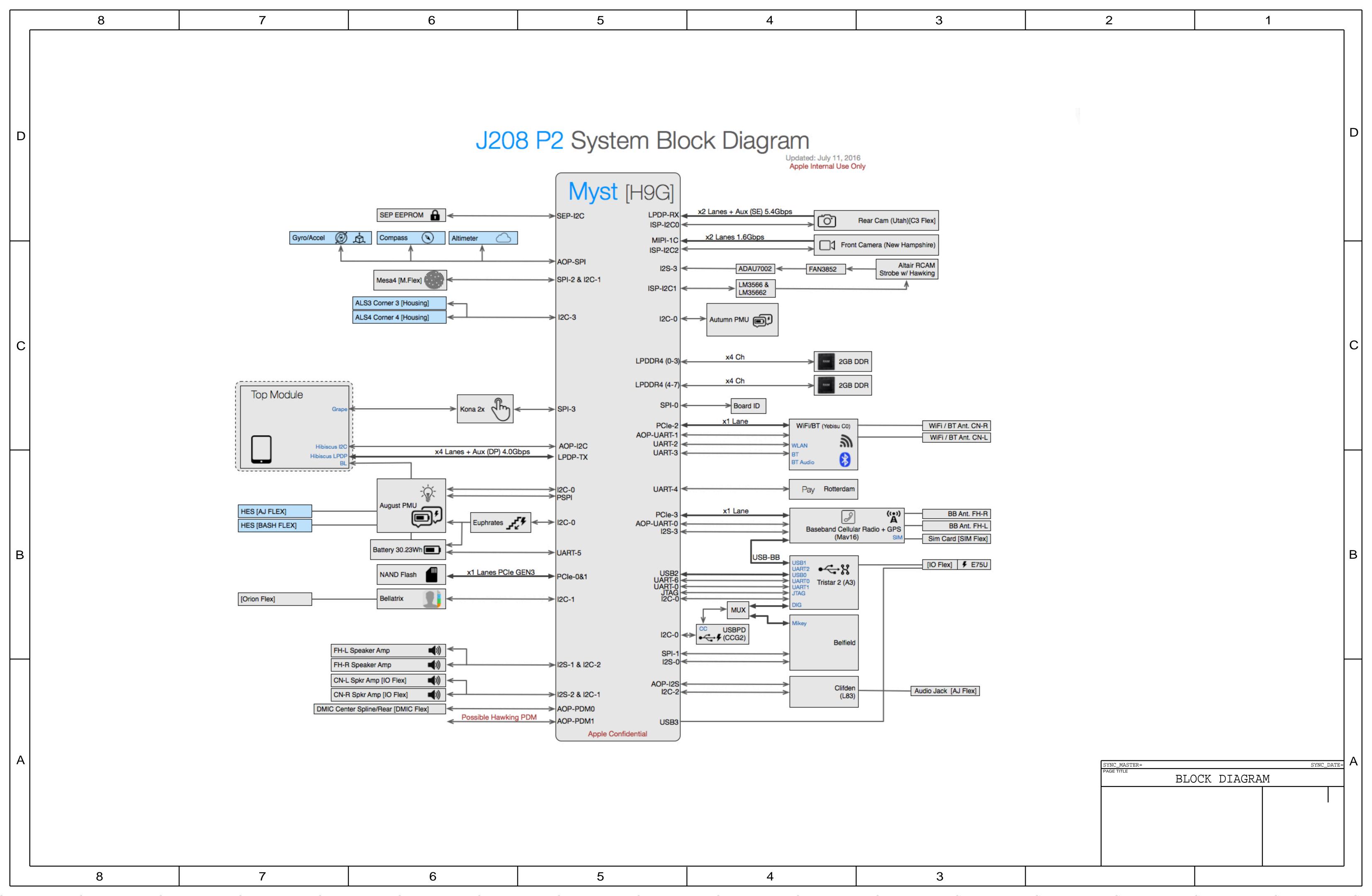
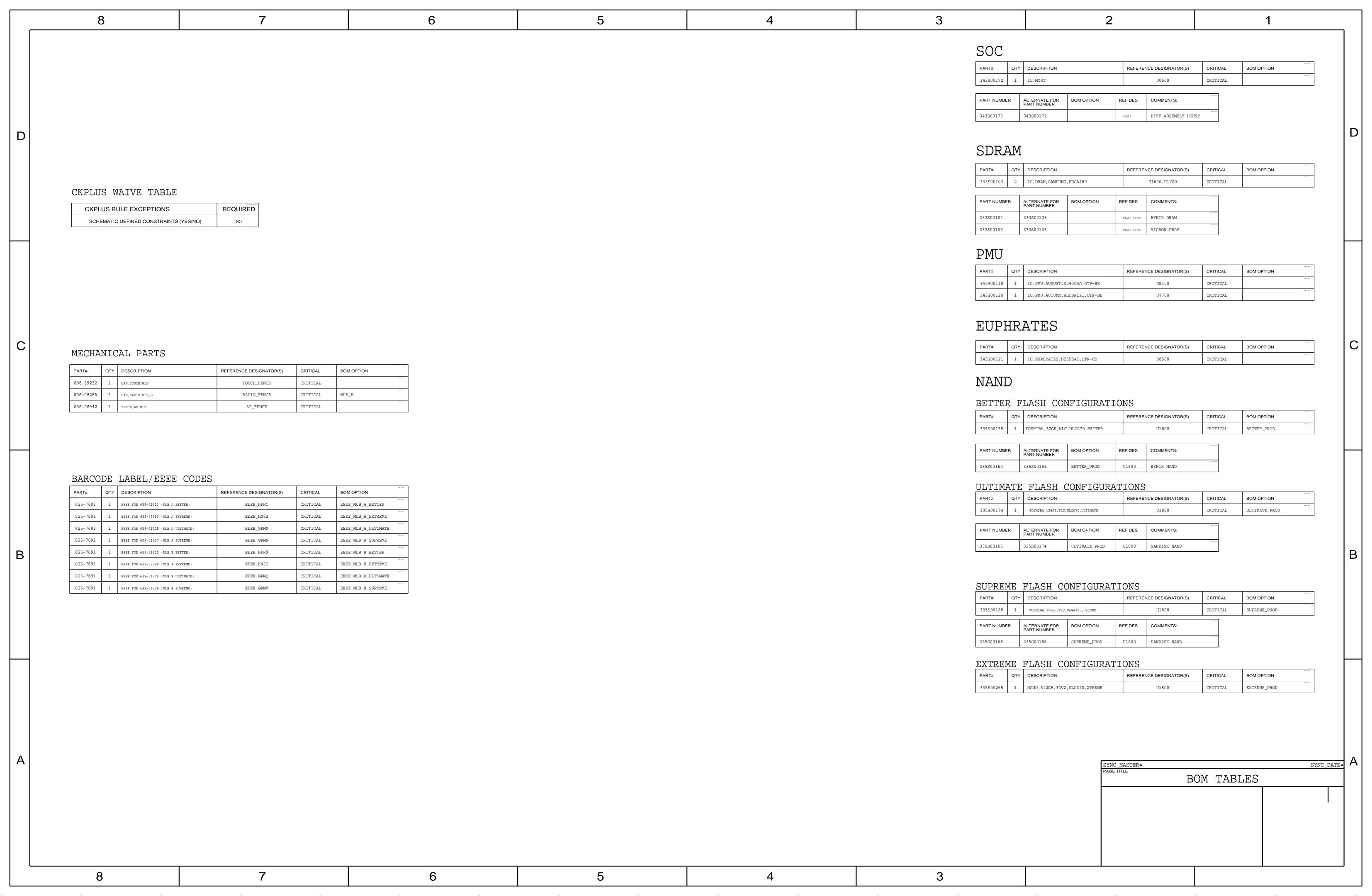
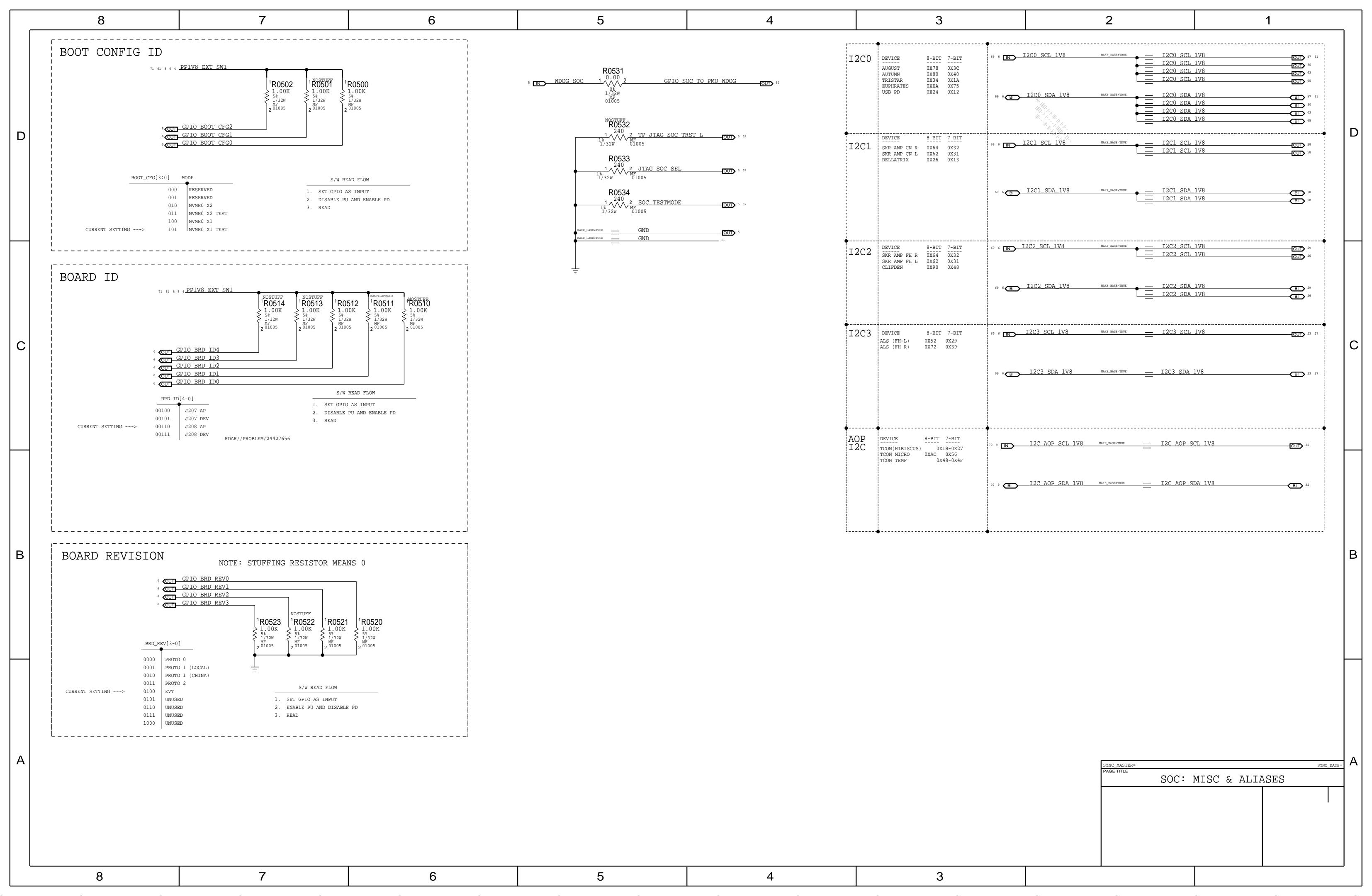
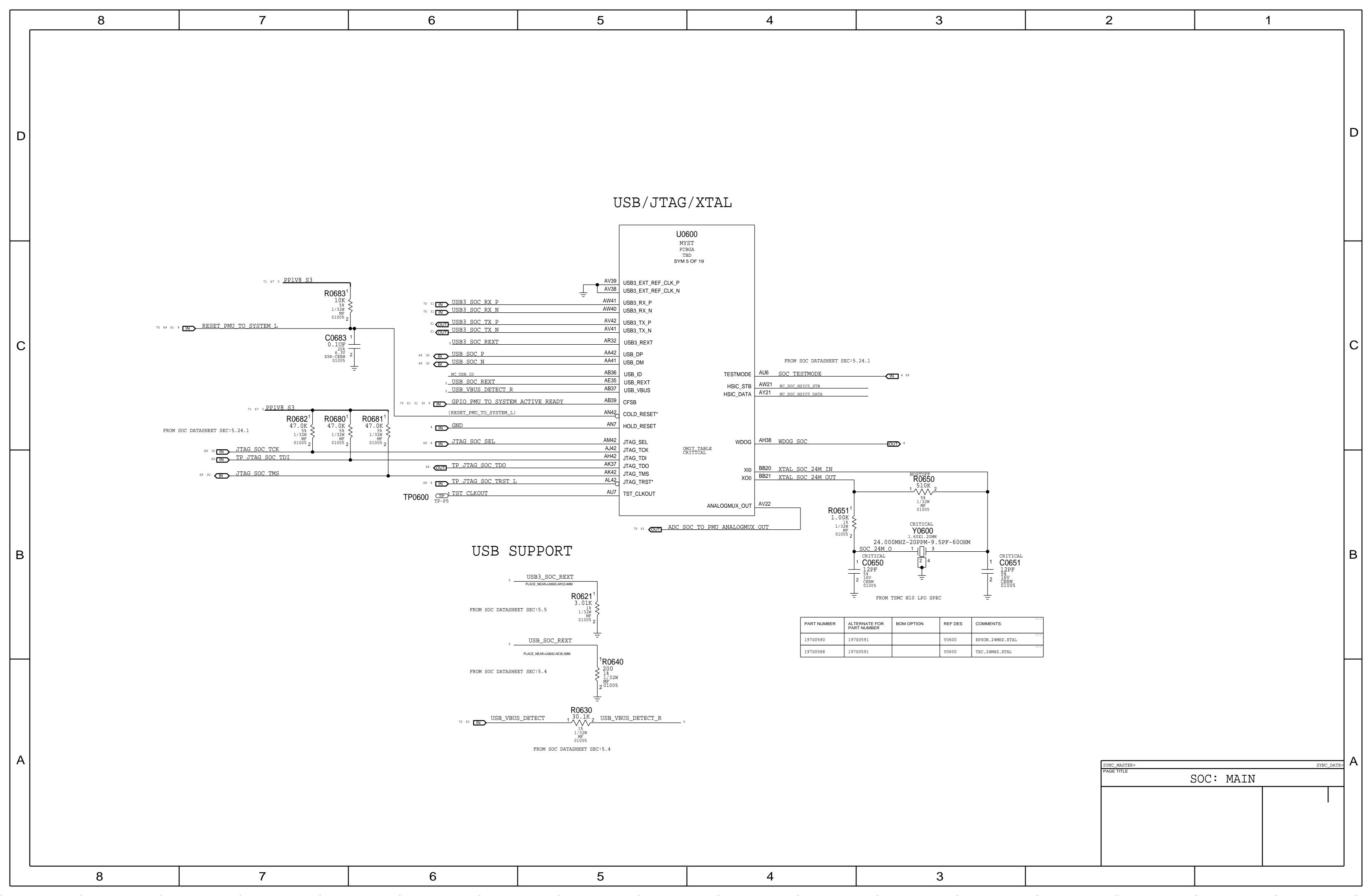
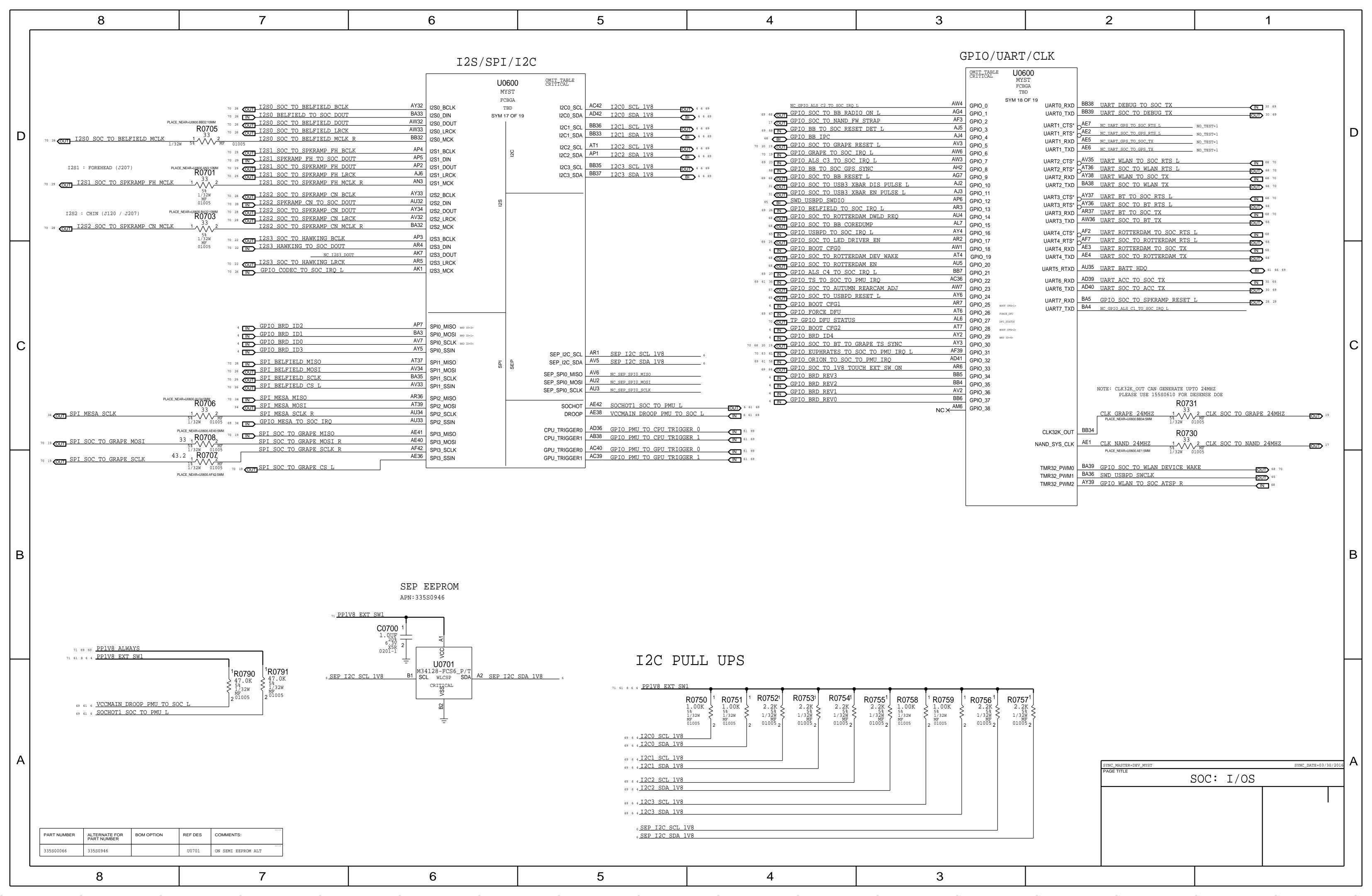
_	8 7	6	5		4	3		2	1		
	1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%. 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.		J208:	MT ₁ B-1	3			REV ECN	DESCRIPTION OF REVISION	CK APPD DATI	·F
	3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.	LAST MODIF	ICATION=Tue Oct					6 0007253455	ENGINEERING RELEASED	2016-10-05	
			207_MLB_B_ELBA								
			DEV_MYST SYN								
			RADIO_MLB SYN								
$ _{D} $			WIFI_MLB SYN	NC VER 0.29.0							
	PAGE CSA CONTENTS	SYNC	DATE	PAGE CS	SA CONTENTS	SYNC	DATE				
	1 1 TABLE OF CONTENTS			51 69		RADIO_MLB	10/03/2016				
	2 2 BLOCK DIAGRAM 3 4 BOM TABLES			$\frac{52}{53}$ 70		RADIO_MLB RADIO_MLB	10/03/2016				
	4 5 SOC: MISC & ALIASES		•	$\frac{53}{54}$ $\frac{74}{74}$		MLB_B_ELBA	11/20/2015				
	5 6 SOC: MAIN			55 77	· · ·	DEV_MYST	03/30/2016				
	6 7 SOC: I/OS 7 8 SOC: LPDP & MIPI	DEV_MYST	03/30/2016	56 78 57 79		DEV_MYST	03/30/2016				
	8 9 SOC: PCIE	DEV_MYST DEV_MYST	03/30/2016	58 80		DEV_MYST MLB_B_ELBA	03/30/2016				
	9 10 SOC: AOP	DEV_MYST	03/30/2016		POWER: AUGUST (1/4)	DEV_MYST	03/30/2016				
	10 11 SOC: DDR	DEV_MYST	03/30/2016	60 82		DEV_MYST	03/30/2016				
	11 12 SOC: POWER (IO) 12 13 SOC: POWER (CPU, GPU)	DEV_MYST DEV_MYST	03/30/2016	$\frac{61}{62}$ 83		DEV_MYST DEV_MYST	03/30/2016				
	13 14 SOC: POWER (SRAM, SOC)	DEV_MYST	03/30/2016	63 85		DEV_MYST	03/30/2016				
	14 15 SOC: GND	DEV_MYST	03/30/2016	64 86	POWER: EXTERNAL SWITCHES & LDOS	DEV_MYST	03/30/2016				
	15 16 DRAM: CHANNELS 0-3	DEV_MYST	03/30/2016	65 88		MLB_B_ELBA	03/30/2016				
c	16 17 DRAM: CHANNELS 4-7 17 18 NAND: NAND	DEV_MYST	03/30/2016	66 89 67 90		MLB_B_ELBA MLB_B_ELBA	03/30/2016				C
	18 21 SENSOR: CARBON, PHOS, MAGN	MLB_B_ELBA	03/30/2016	68 91							
	19 22 TOUCH: KONA MASTER	MLB_B_ELBA	03/30/2016	69 93		MLB_B_ELBA	03/30/2016				
	20 23 TOUCH: KONA SLAVE 21 24 TOUCH: GRAPE CONN	MLB_B_ELBA	03/30/2016		TEST: EE TP/PP POWER: ALIASES	MLB_B_ELBA	03/30/2016				
	22 26 HAWKING	MLB_B_ELBA MLB_B_ELBA	03/30/2016	71 121	FOWER. ALIASES						
	23 27 FLEX CONNS: CORNER 3	MLB_B_ELBA	02/24/2016								
	24 28 CAMERA: FRONT	MLB_B_ELBA	03/30/2016								
	25 29 CAMERA: STROBE 26 30 AUDIO: CLIFDEN, BELFIELD	MLB_B_ELBA MLB_B_ELBA	03/30/2016								
	27 31 FLEX CONNS: C4 & DMIC	MLB_B_ELBA	03/30/2016	-							
	28 32 AUDIO: SPEAKER AMPS (CN)	J120_MLB_B	04/03/2016								
	29 33 AUDIO: SPEAKER AMPS (FH) 30 35 IO: TRISTAR	J120_MLB_B	04/03/2016								
	31 37 IO: HOTBAR, SIM, XBAR	MLB_B_ELBA	03/30/2010								
	32 45 DISPLAY CONN	MLB_B_ELBA	03/30/2016								
	33 46 DISPLAY: EDP SUPPORT	MLB_B_ELBA	03/30/2016								
B	34 47 SENSOR: MESA 35 49 WIFI/BT: MODULE	MLB_B_ELBA WIFI_MLB_B	03/30/2016								B
	36 51 WIFI/BT: J208 FRONT END	WIFI_MLB_B	10/03/2016	_							
	37 55 [RADIO] PMU: CONTROL AND CLOCKS	RADIO_MLB	10/03/2016								
	38 56 [RADIO] PMU: SWITCHERS & LDOS	RADIO_MLB	10/03/2016								
	39 57 [RADIO] BASEBAND: POWER 40 58 [RADIO] BASEBAND: CONTROLS	RADIO_MLB RADIO_MLB	10/03/2016								
	41 59 [RADIO] BASEBAND GPIOS	RADIO_MLB	10/03/2016								
	42 60 [RADIO] XCVR: POWER	RADIO_MLB	10/03/2016								
	43 61 [RADIO] XCVR: TX PORTS 44 62 [RADIO] XCVR: RX PORTS	RADIO_MLB RADIO_MLB	10/03/2016								
	45 63 [RADIO] RX MATCHING	RADIO_MLB	10/03/2016								
	46 64 [RADIO] COUPLER & RIGHT COAX	RADIO_MLB	10/03/2016								
	47 65 [RADIO] DRX ASMS 48 66 [RADIO] DRX LNAS	RADIO_MLB	10/03/2016								
	48 00 [RADIO] DRX LNAS 49 67 [RADIO] PPXLR & UAT CO-AX	RADIO_MLB RADIO_MLB	10/03/2016								
	50 68 [RADIO] PMU: ET MODULATOR	RADIO_MLB	10/03/2016								
A								SYNC_MASTER=	TABLE OF CONTENTS	SYNC_DATE	E A
					SCH AND BOARD P/N			DRAWING TITLE	SCHEM, MLB-B, (NY), J208		7
					PART# QTY DESCRIPTION	REFERENCE DESIGNATOR(S) CRITICAL BOM OPTION	Mark Artis				4
					051-01016 1 SCHEM, MLB-B, NY, J208	SCH1 CRITICAL	VAR.4, (1900			1	
					820-00433 1 PCBF,MLB-B,NY,J208	PCB1 CRITICAL					
			_		A						
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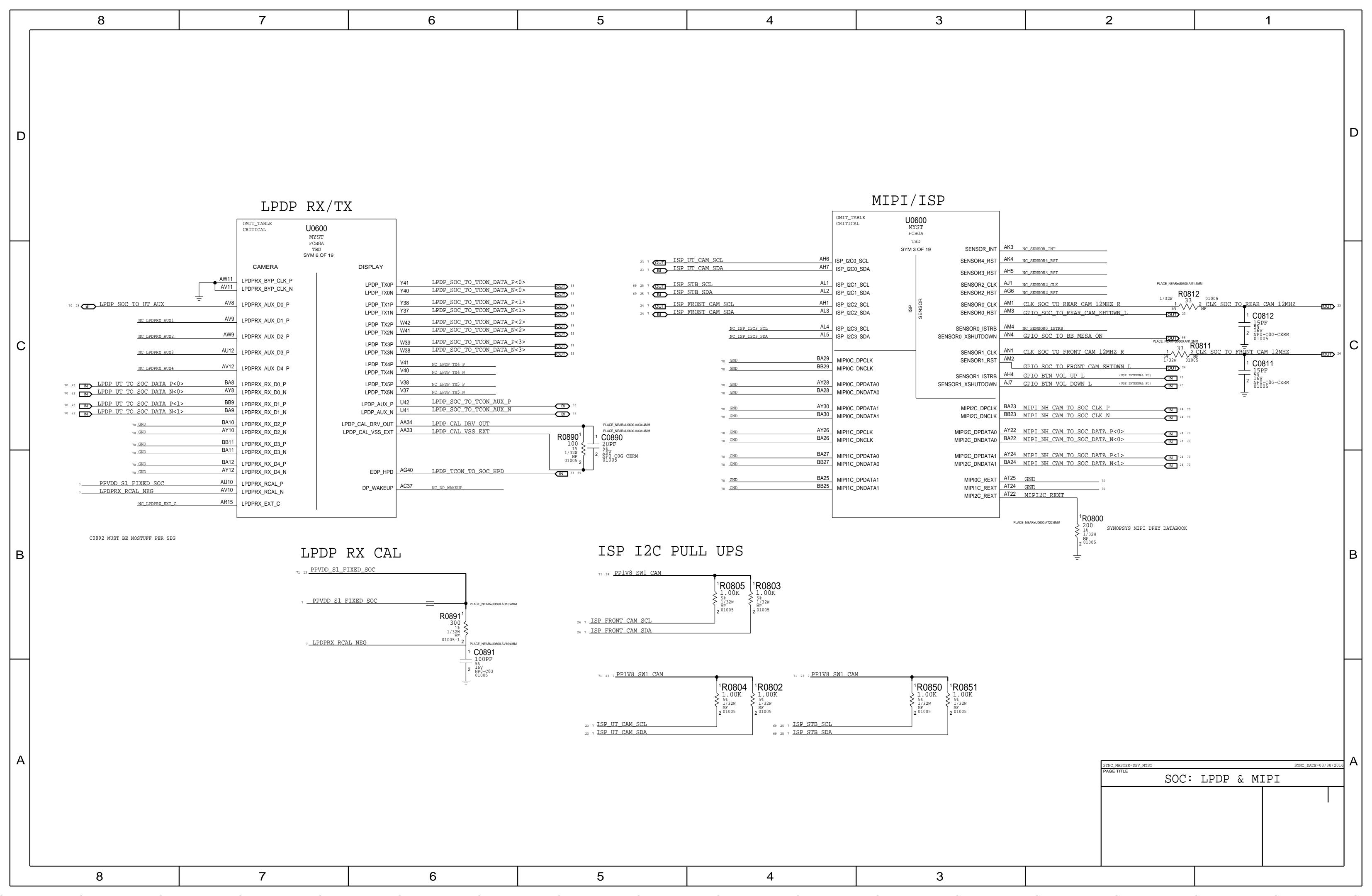


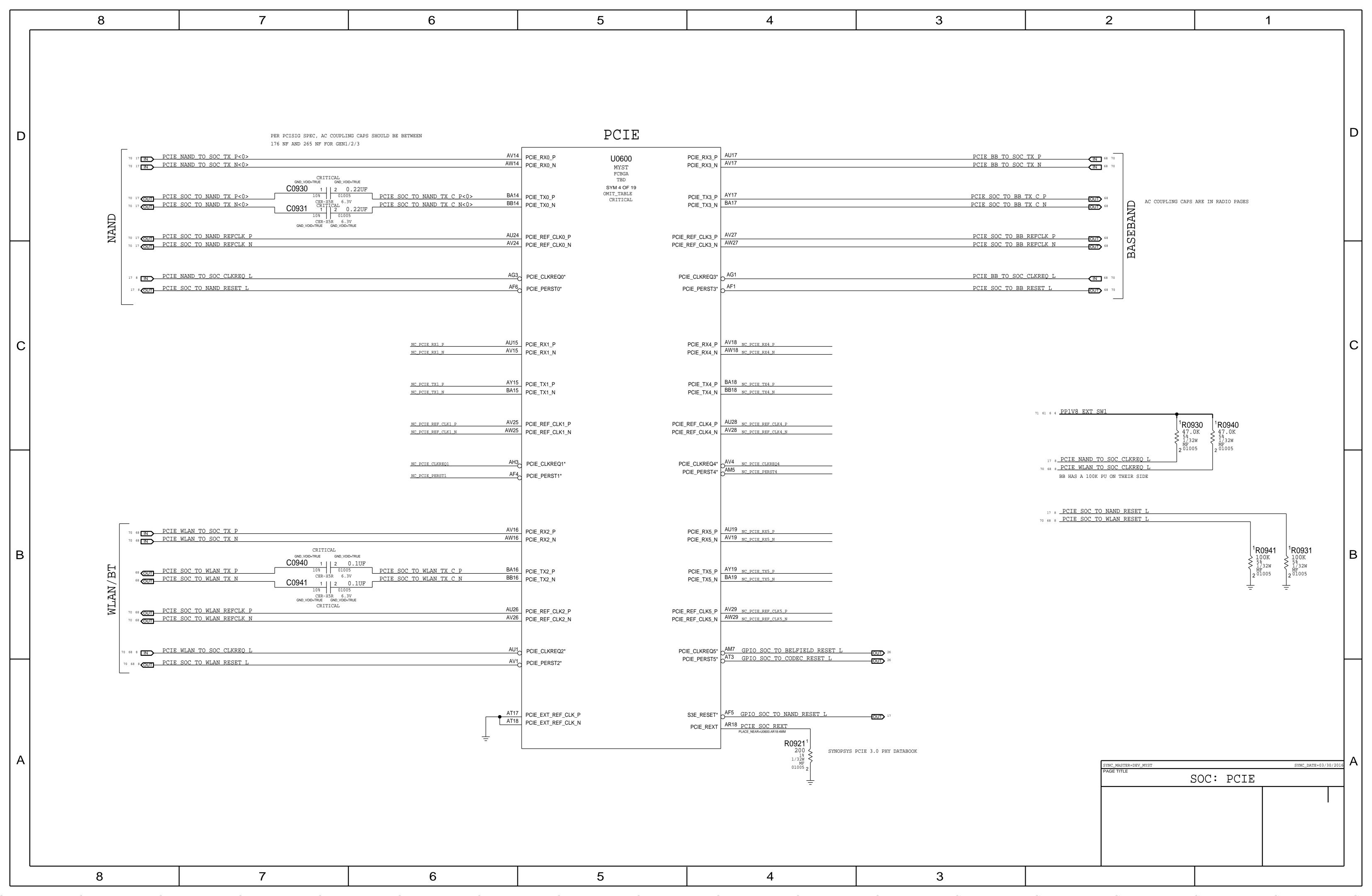


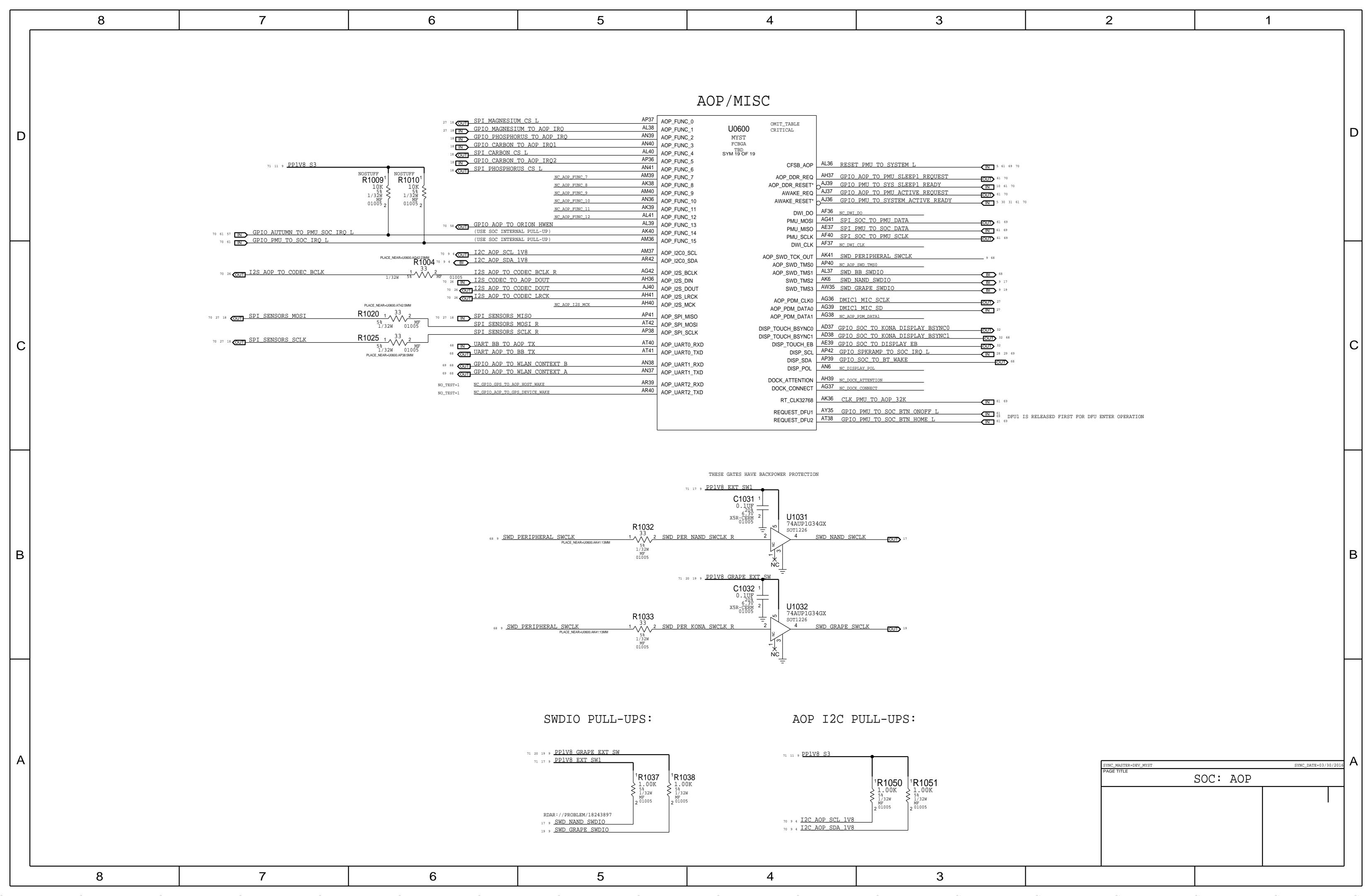


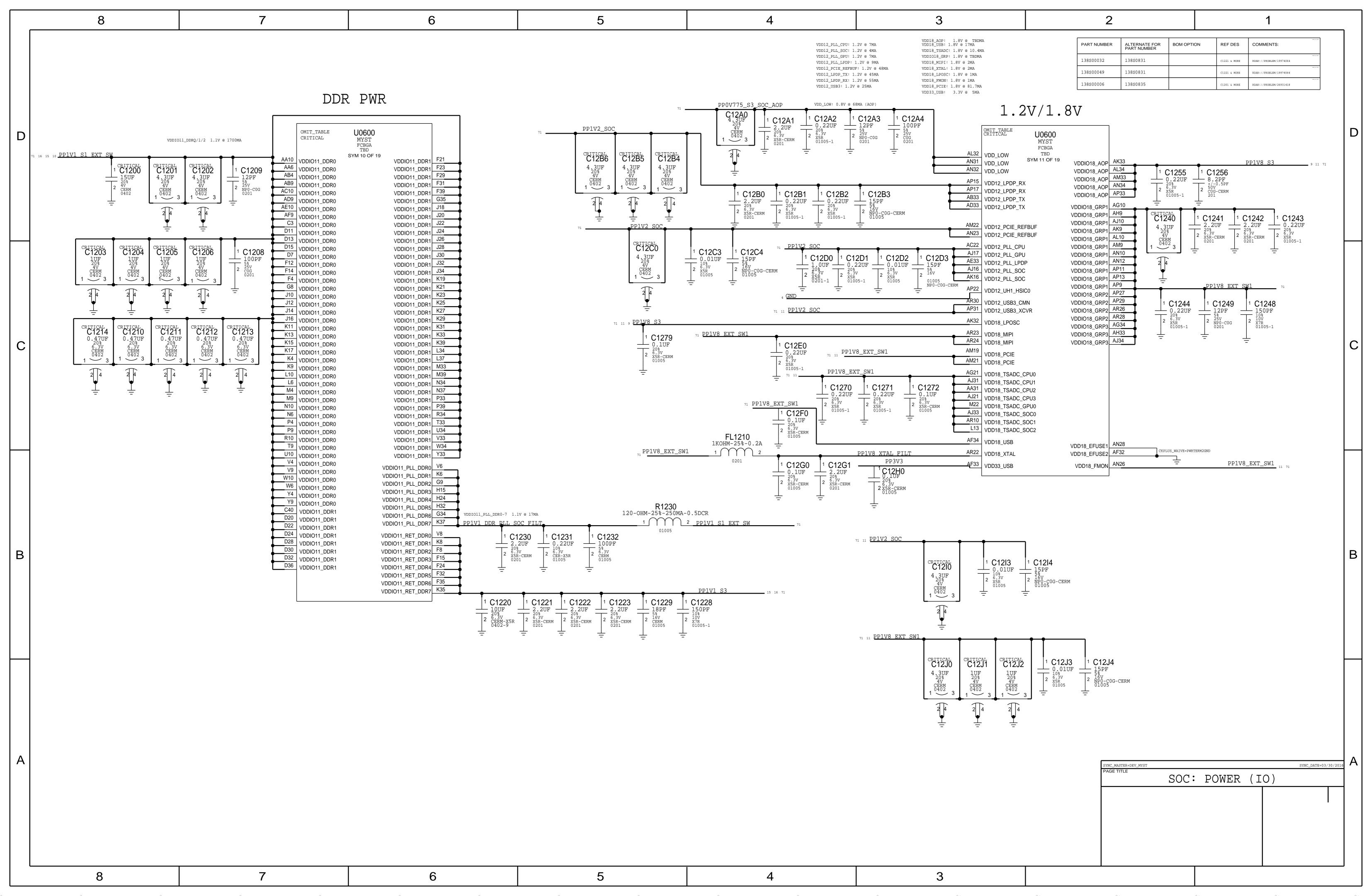


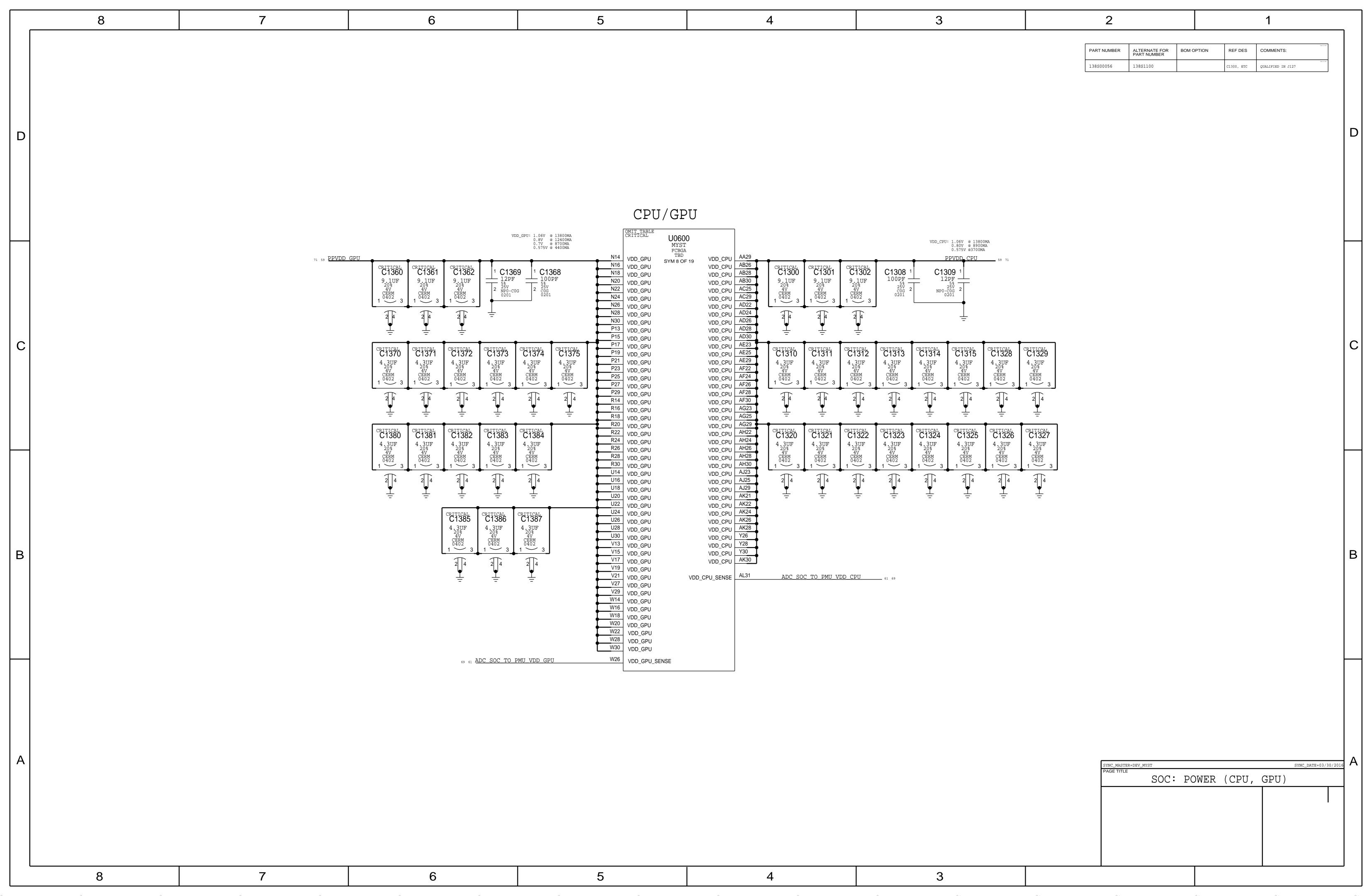


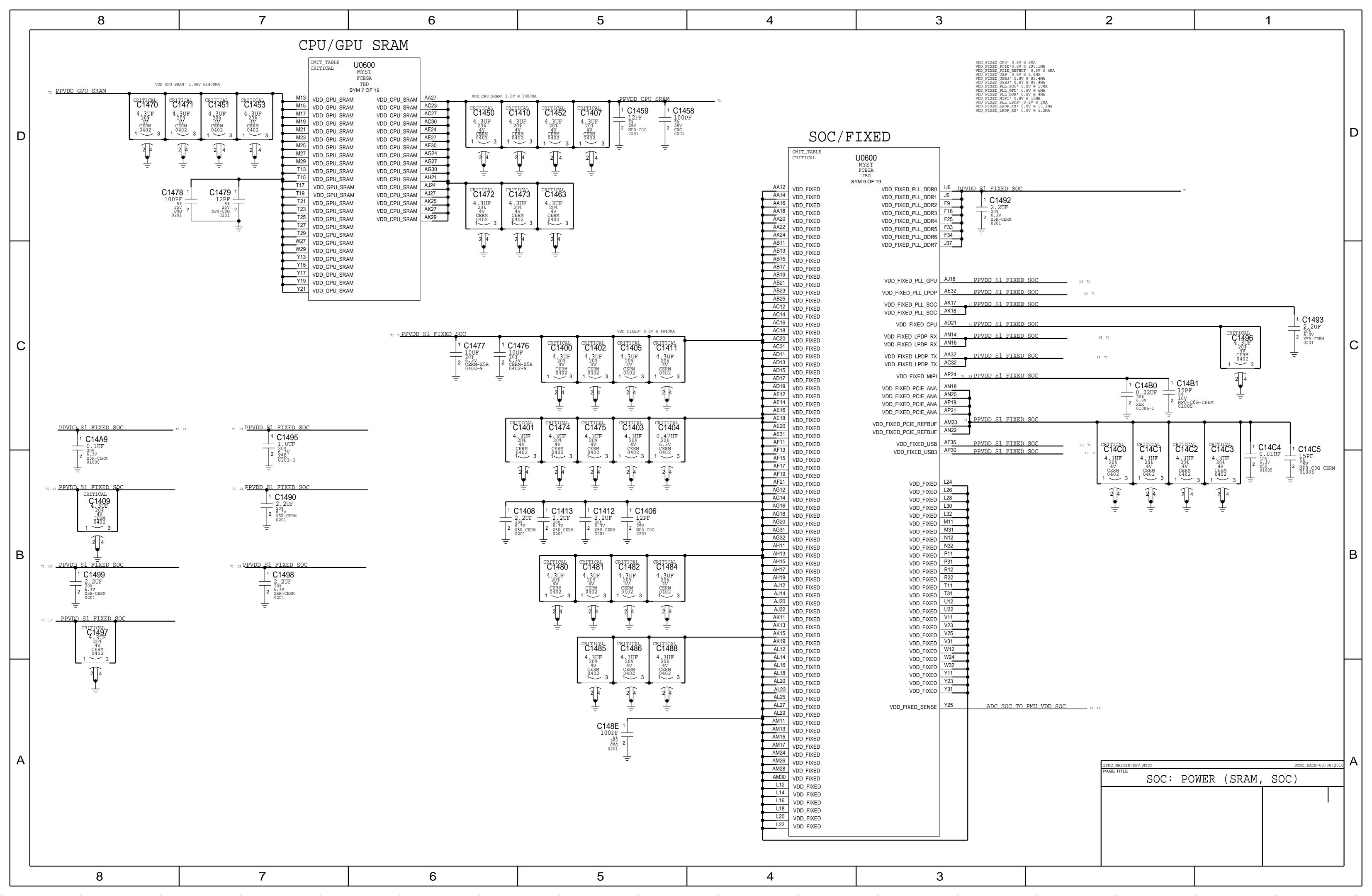


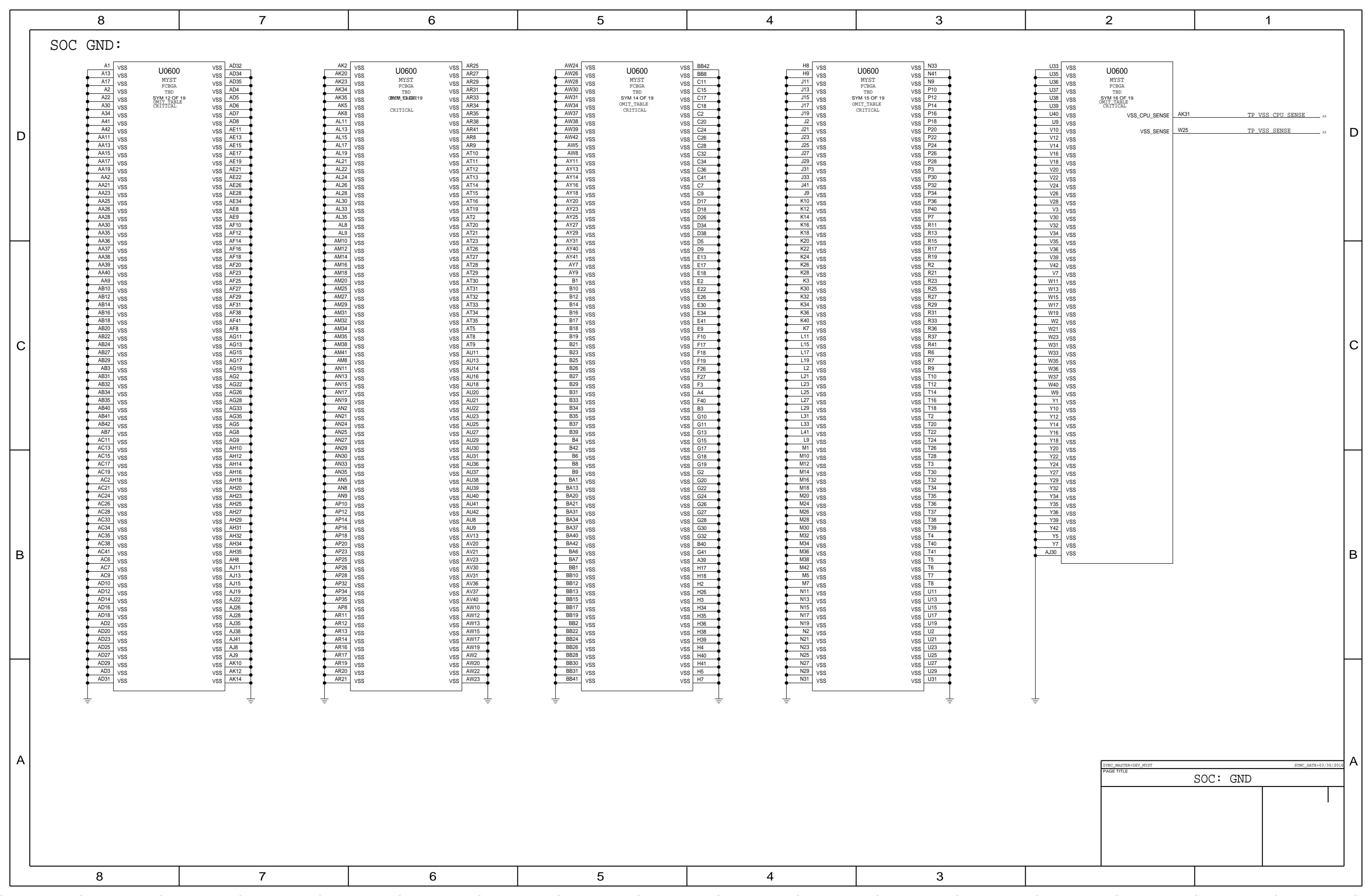


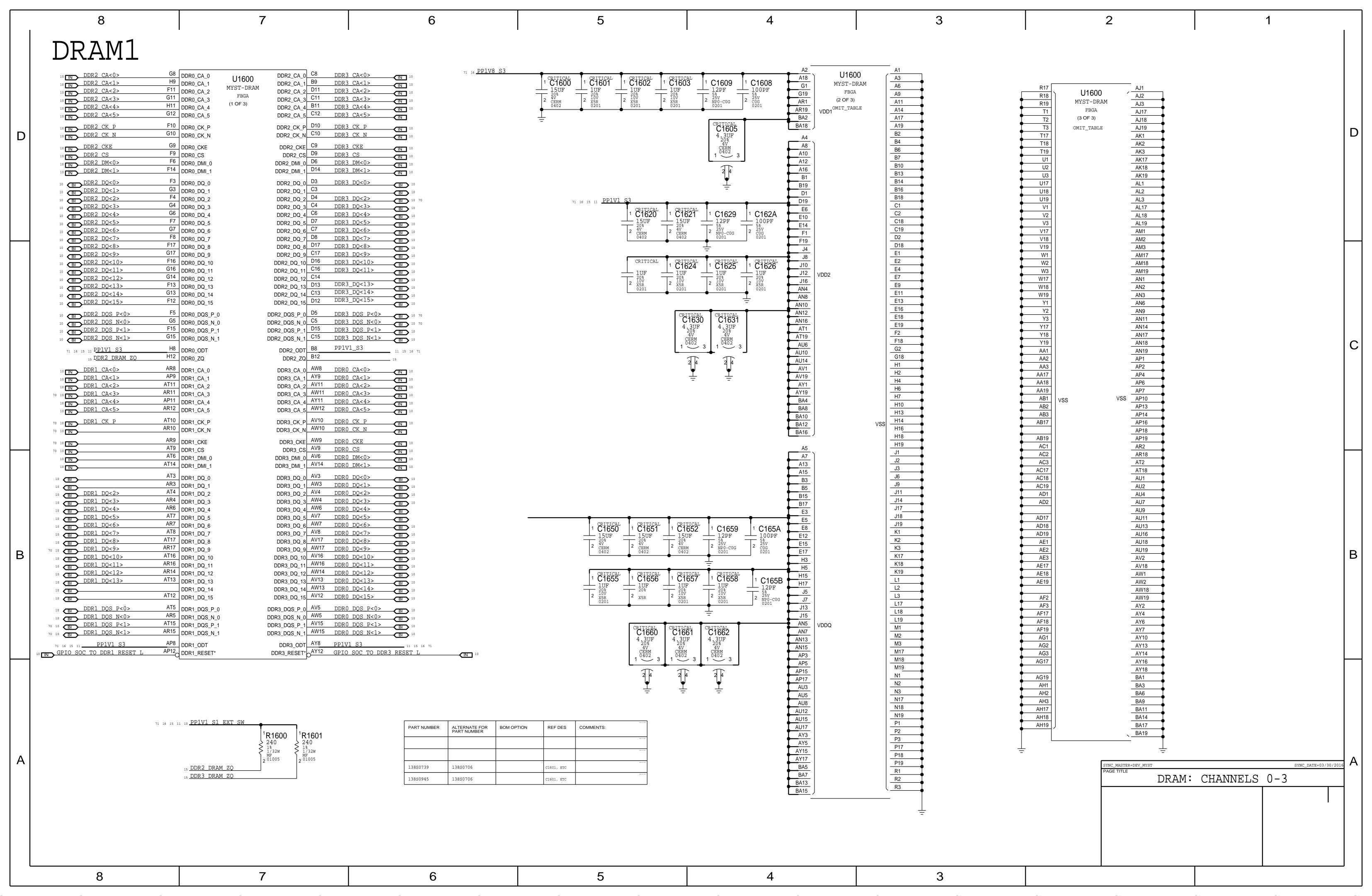


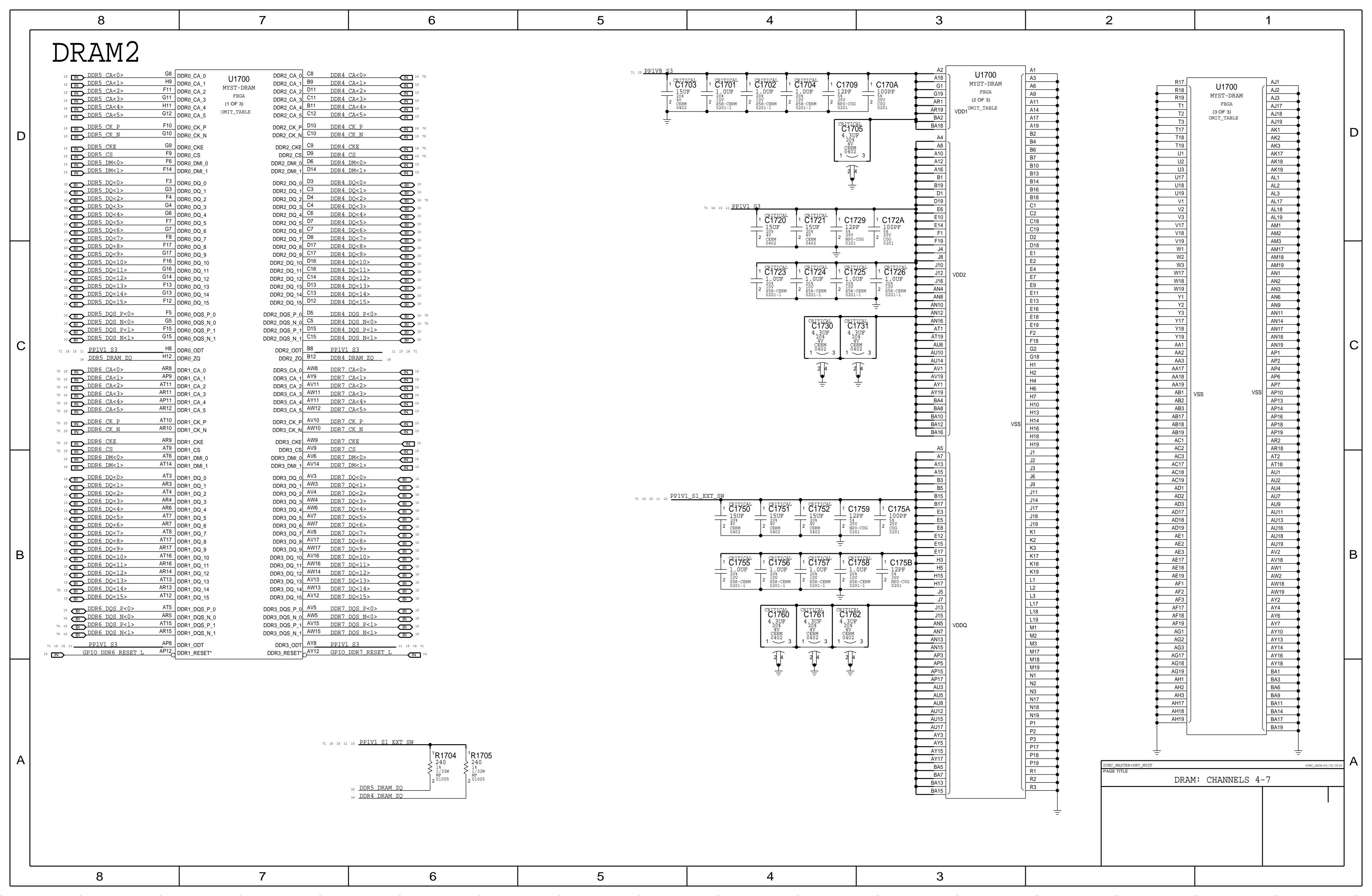


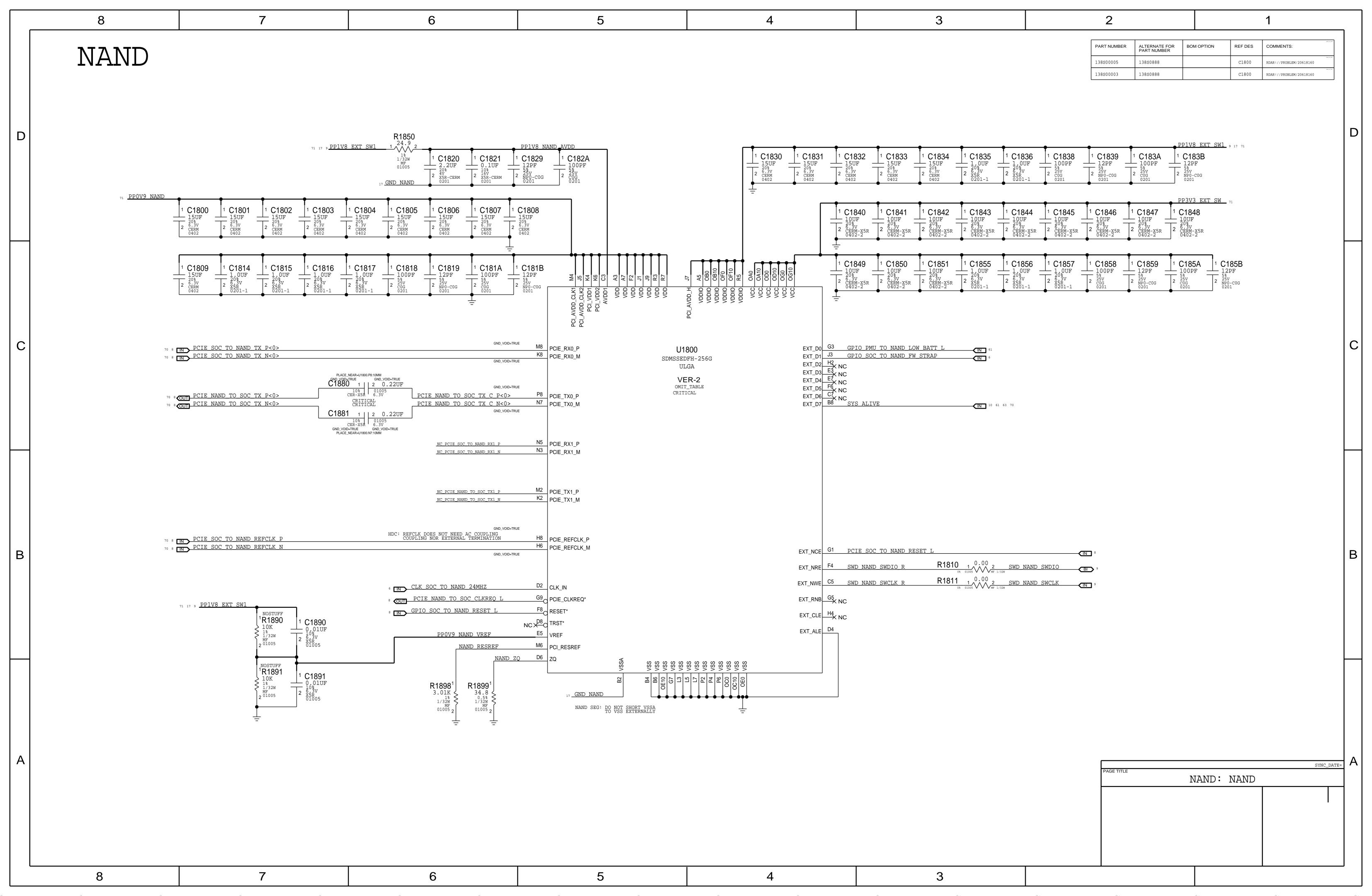


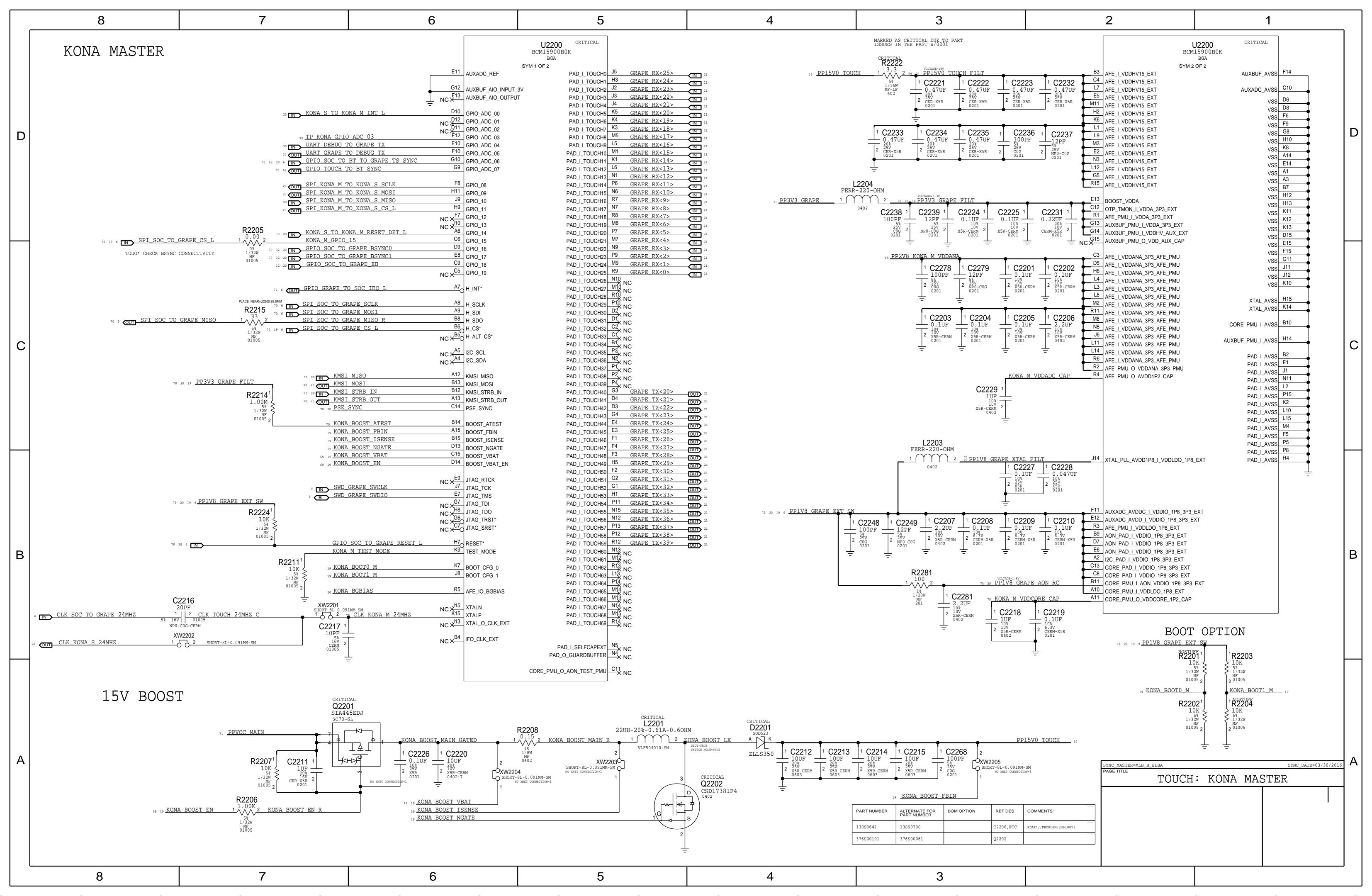


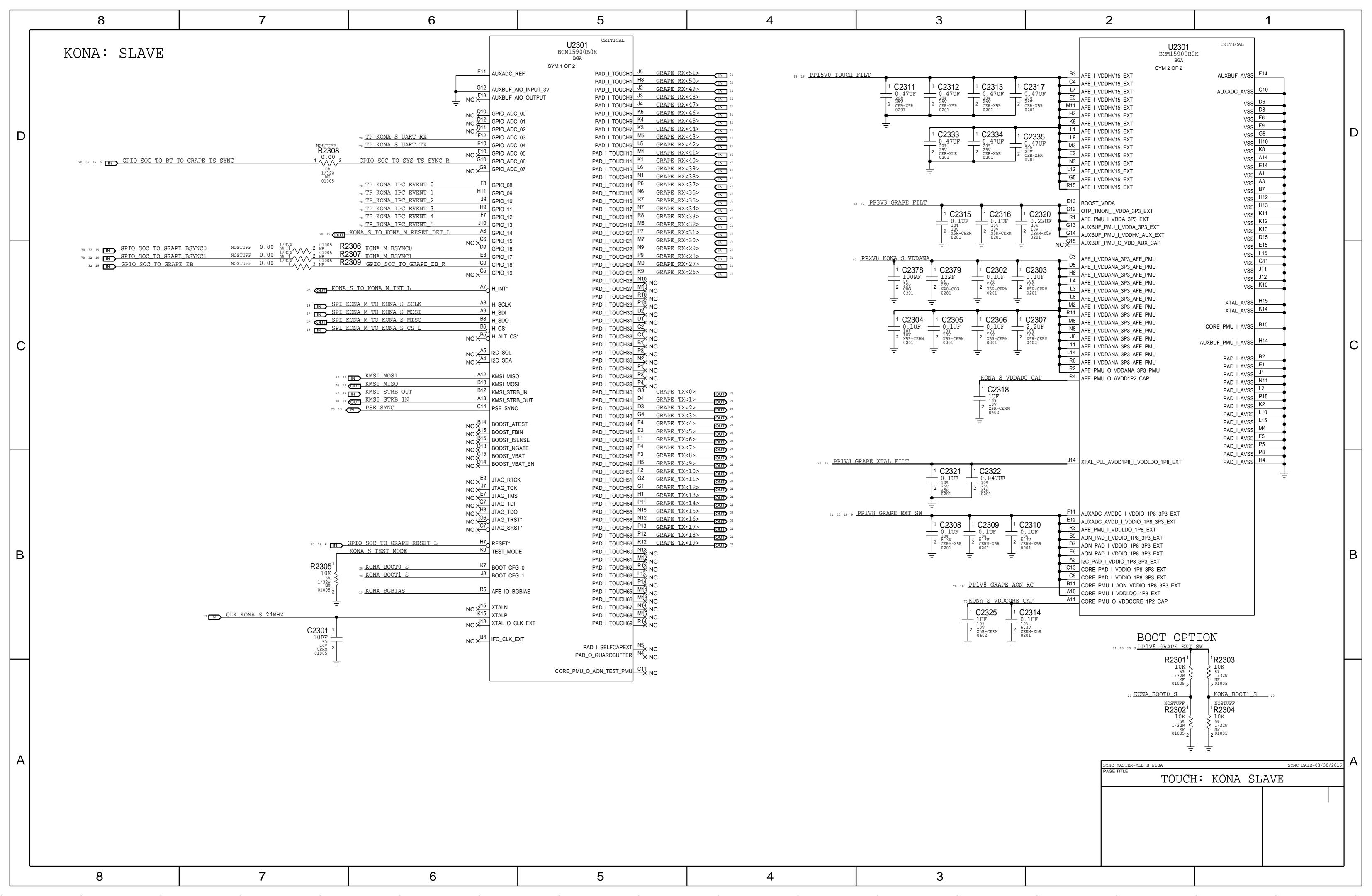


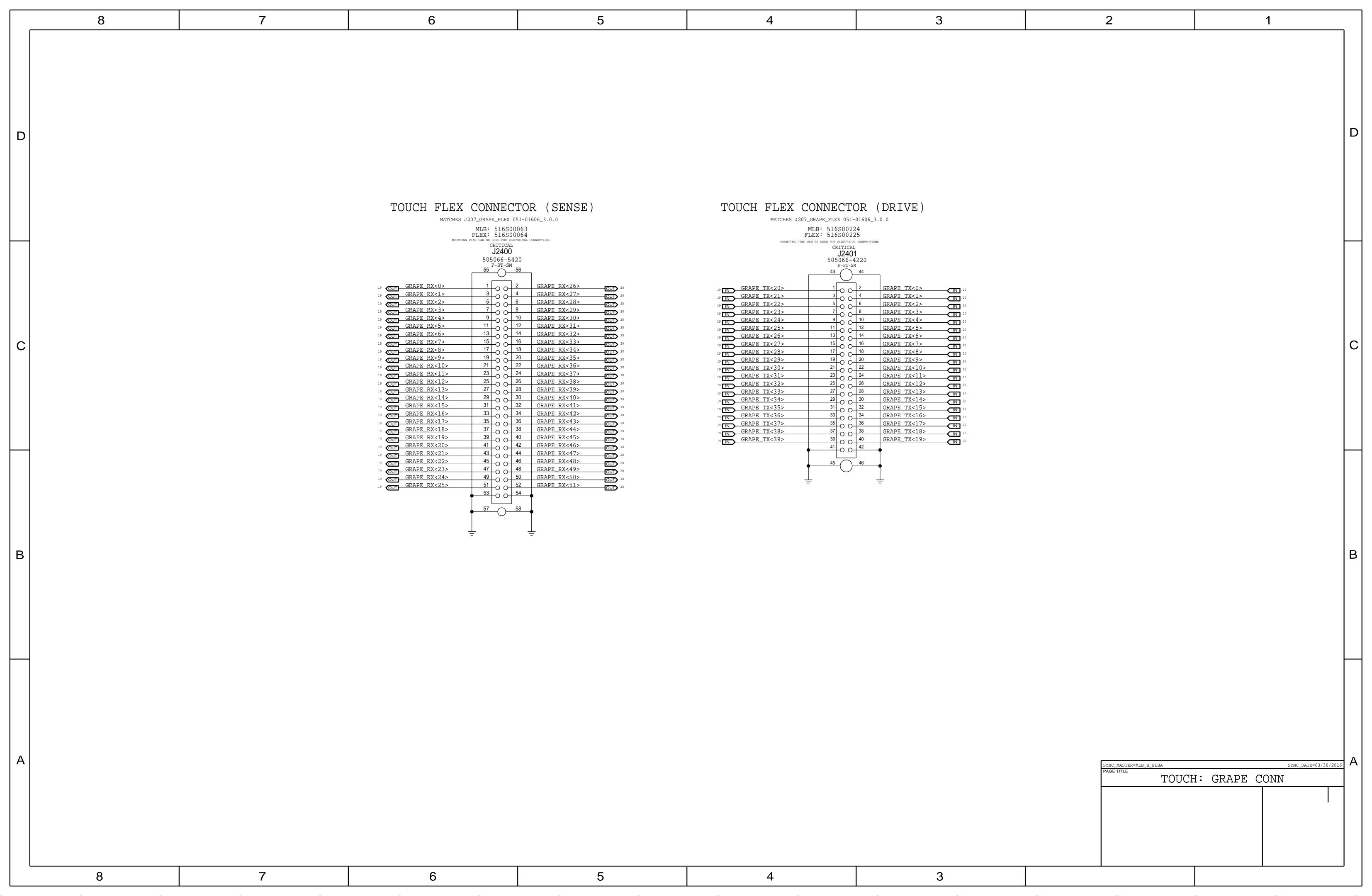


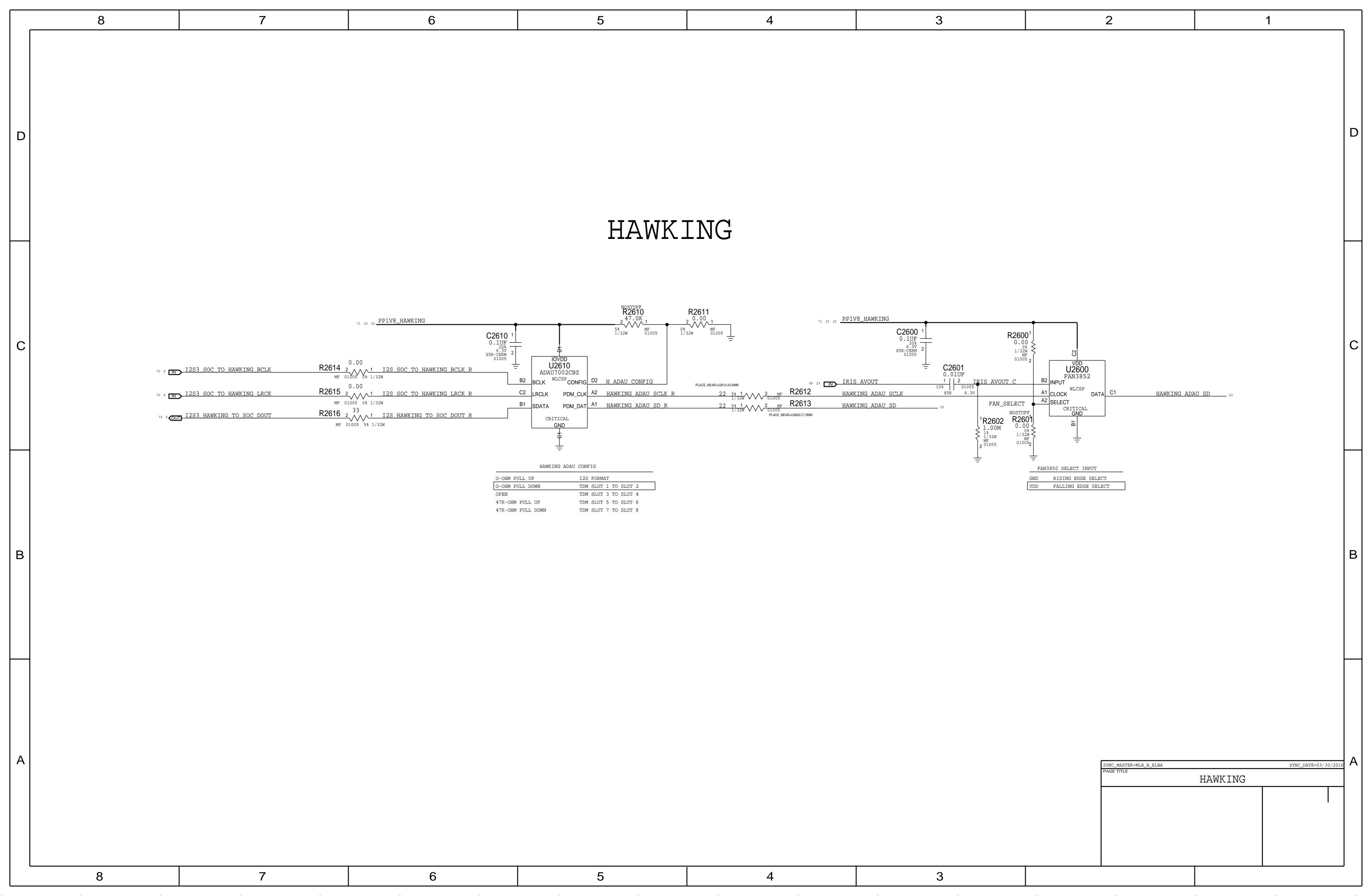


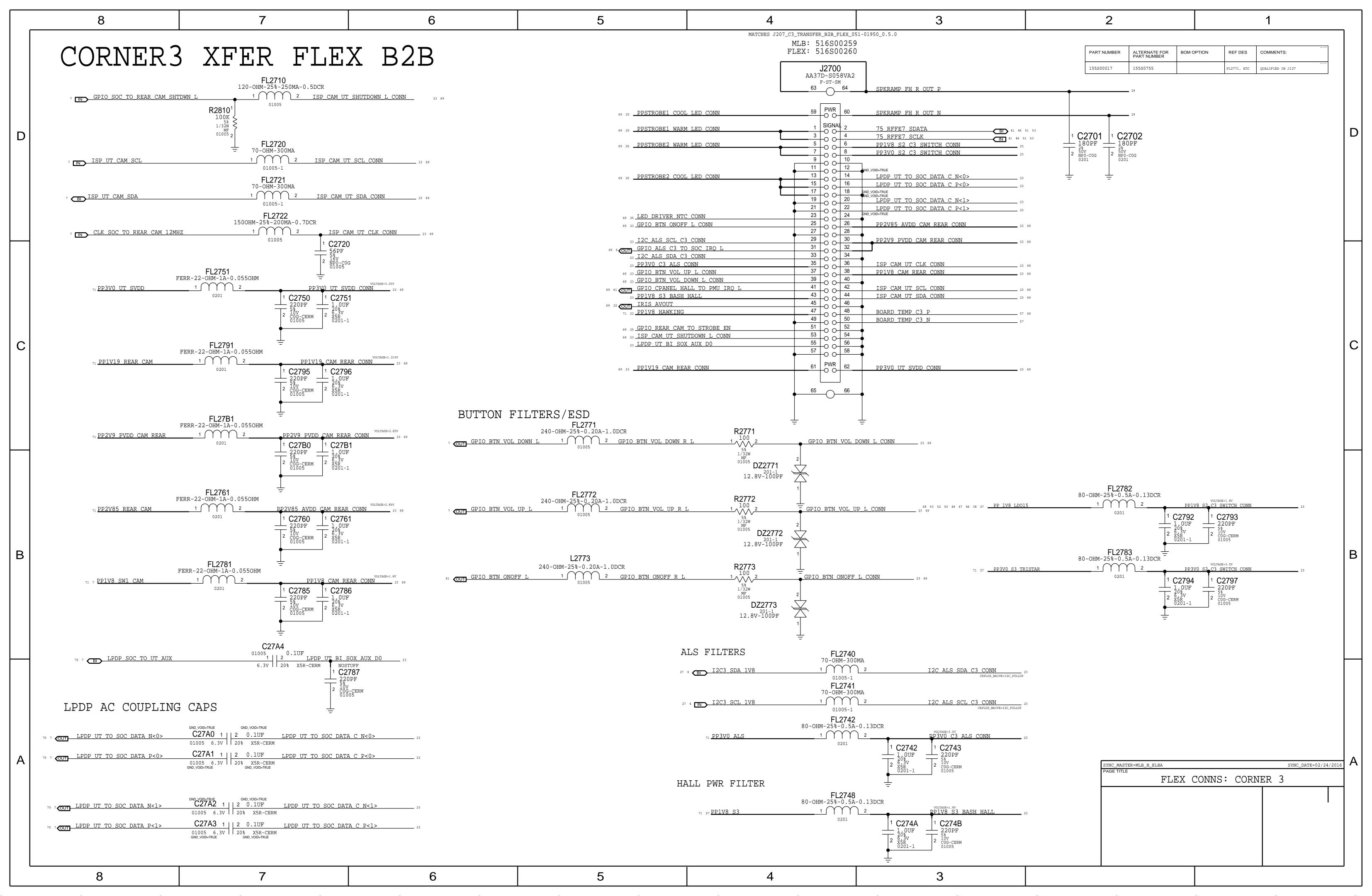


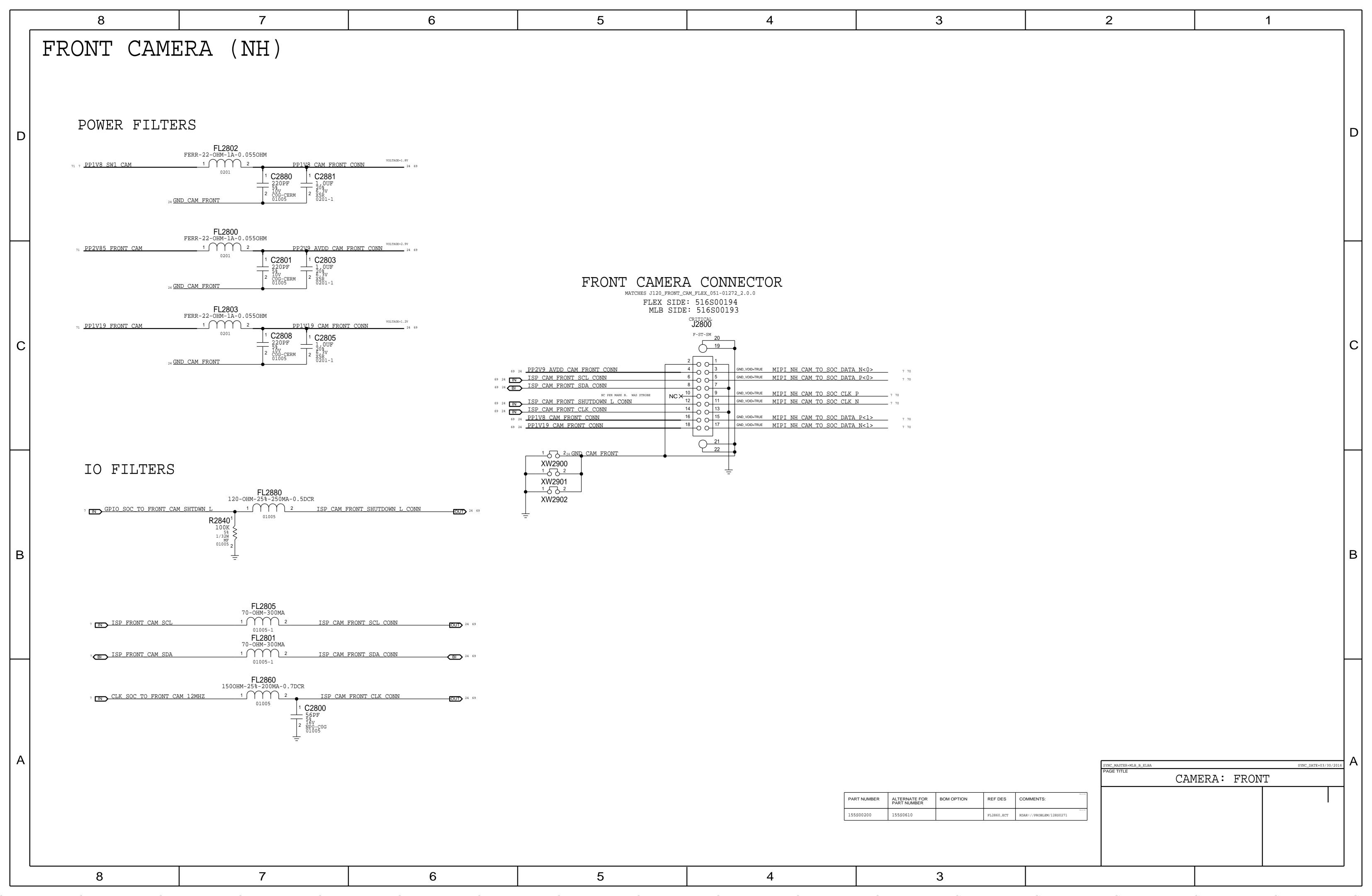


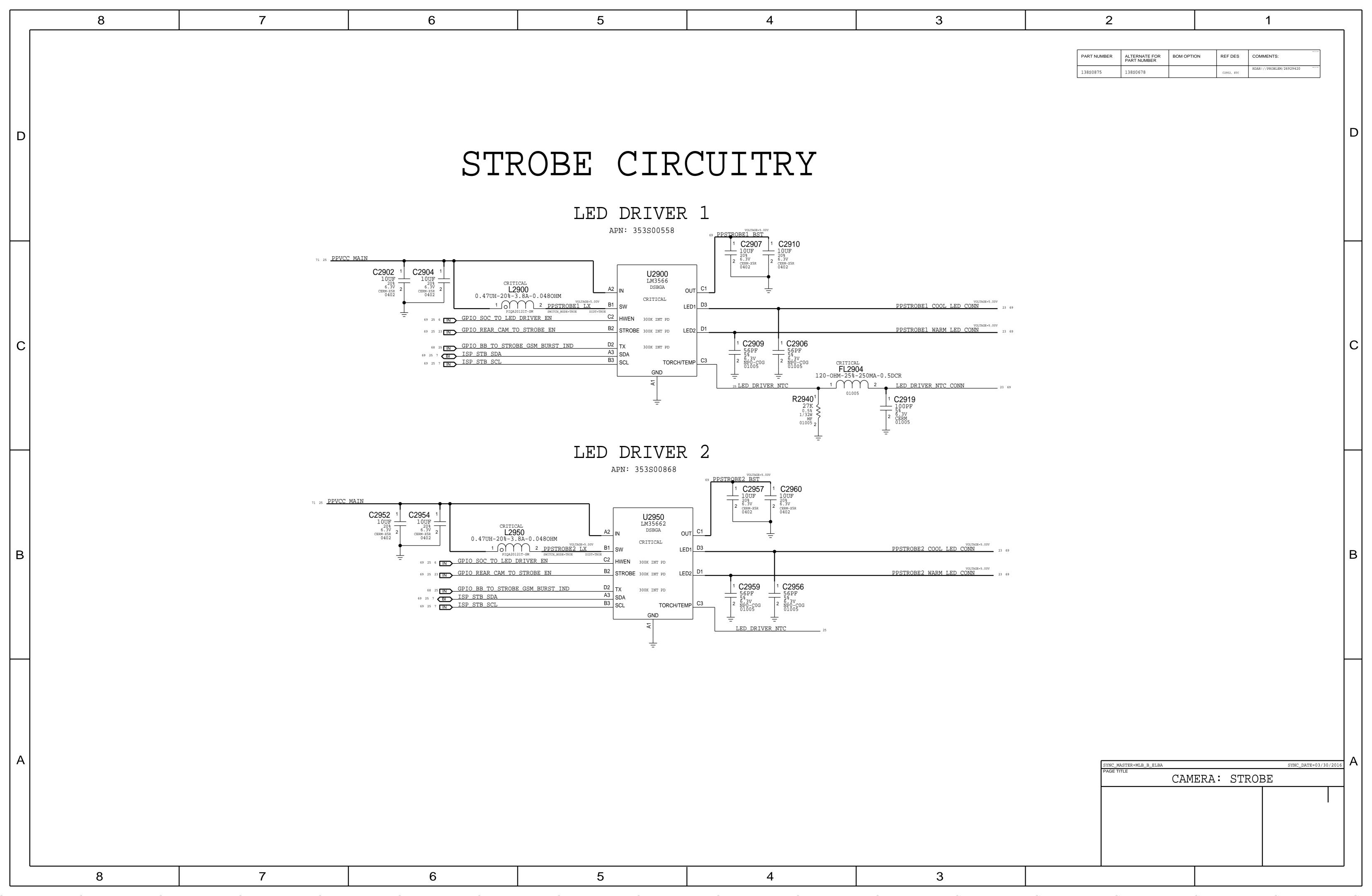


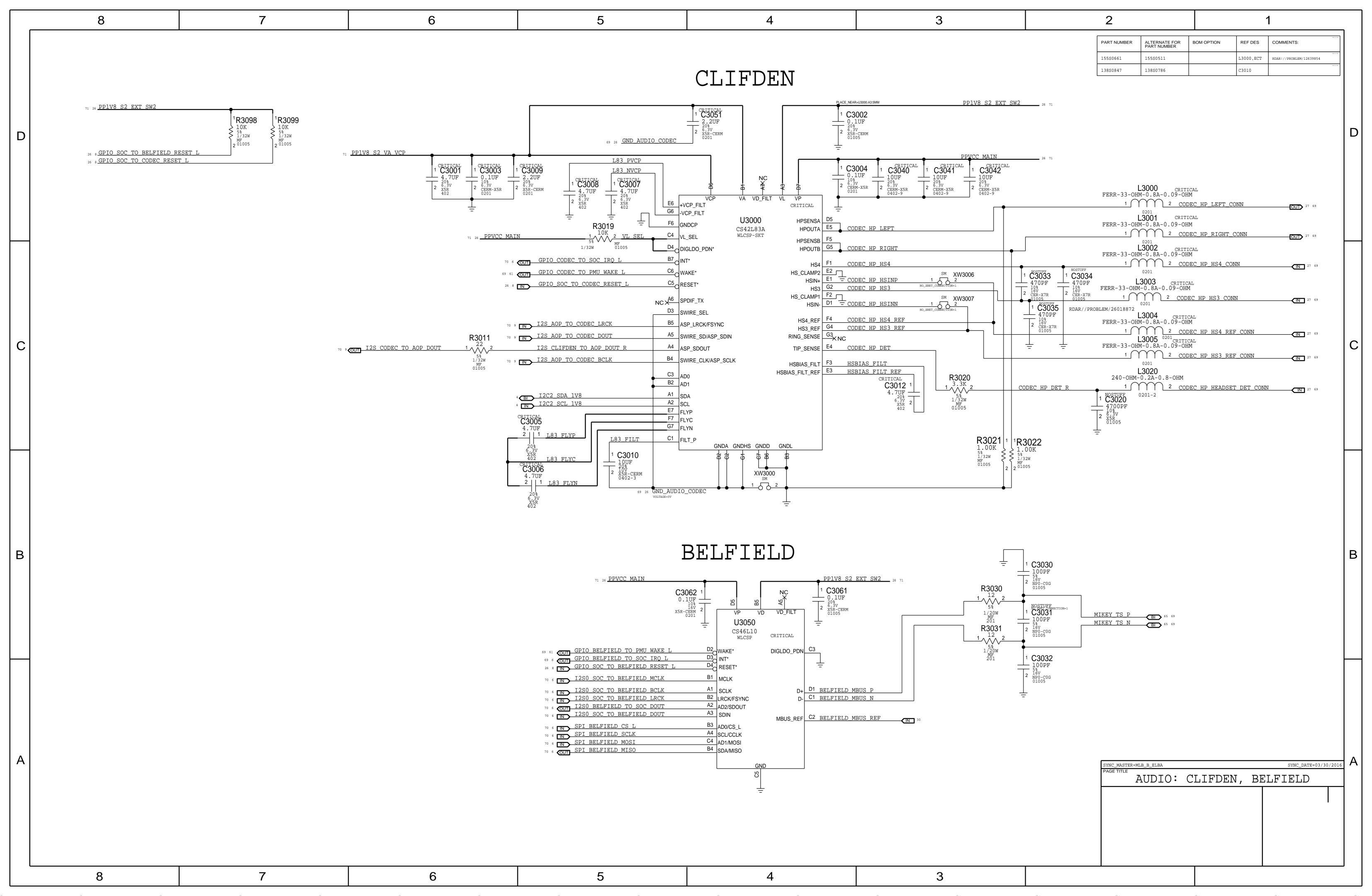


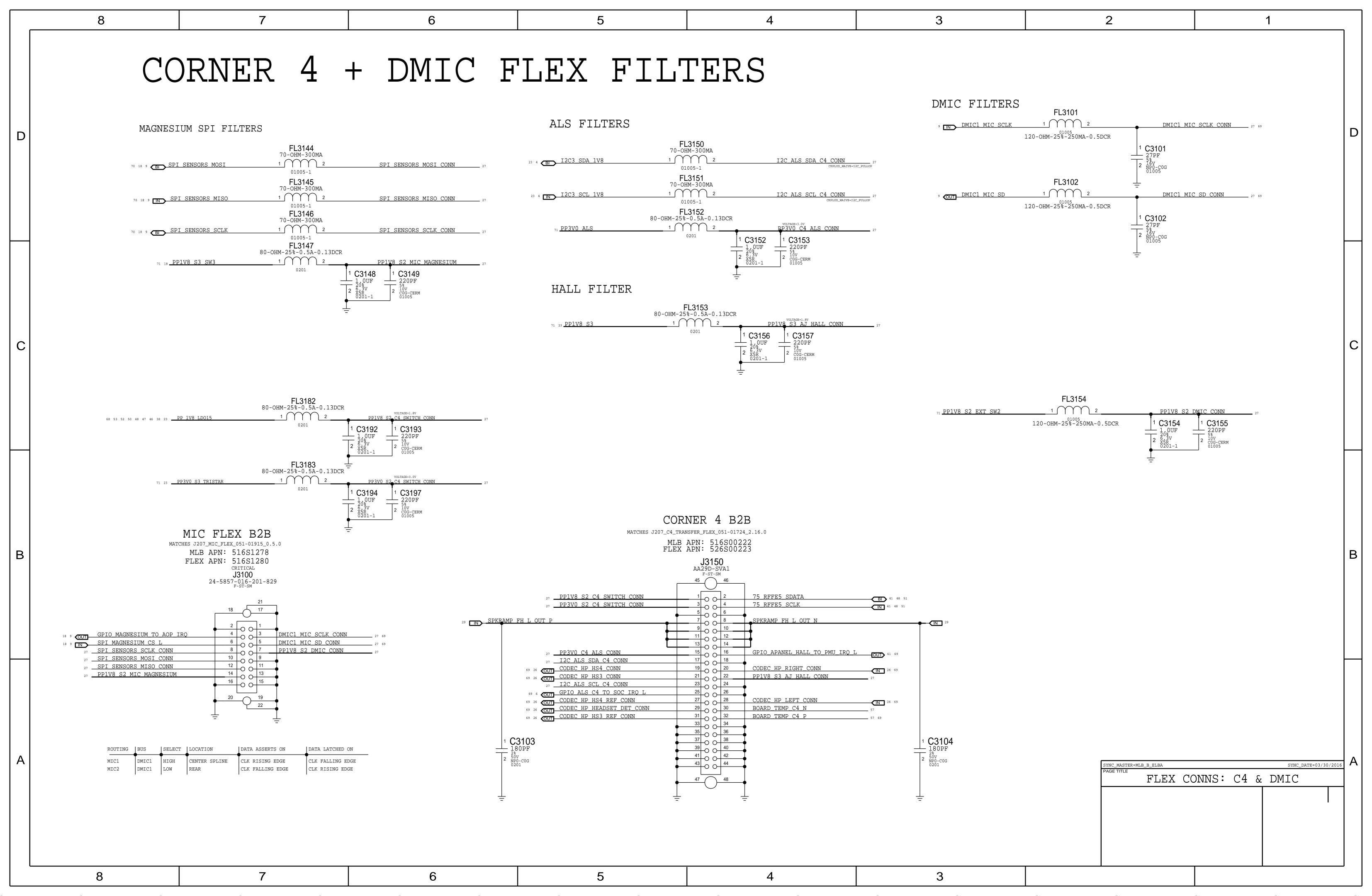


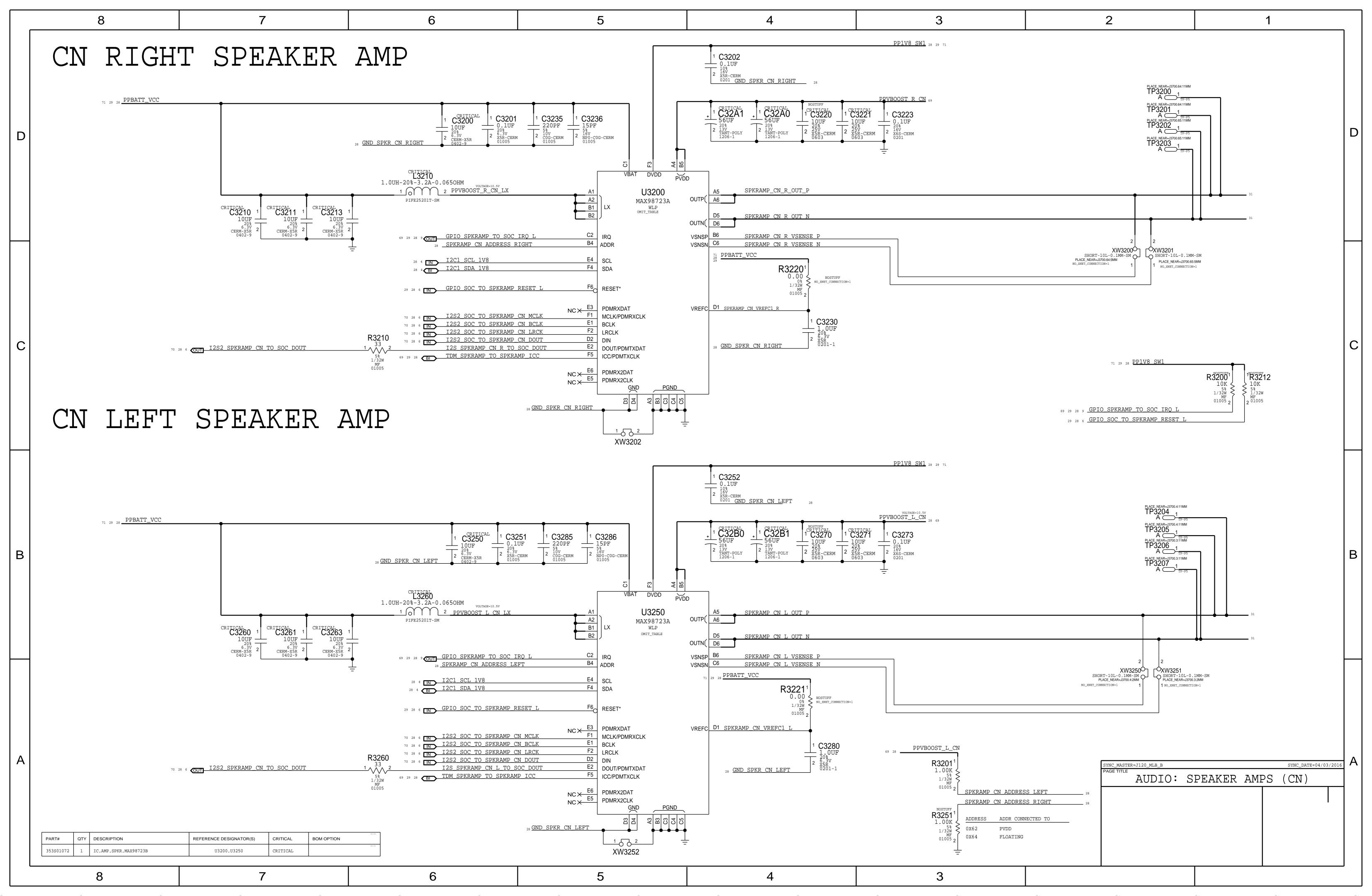


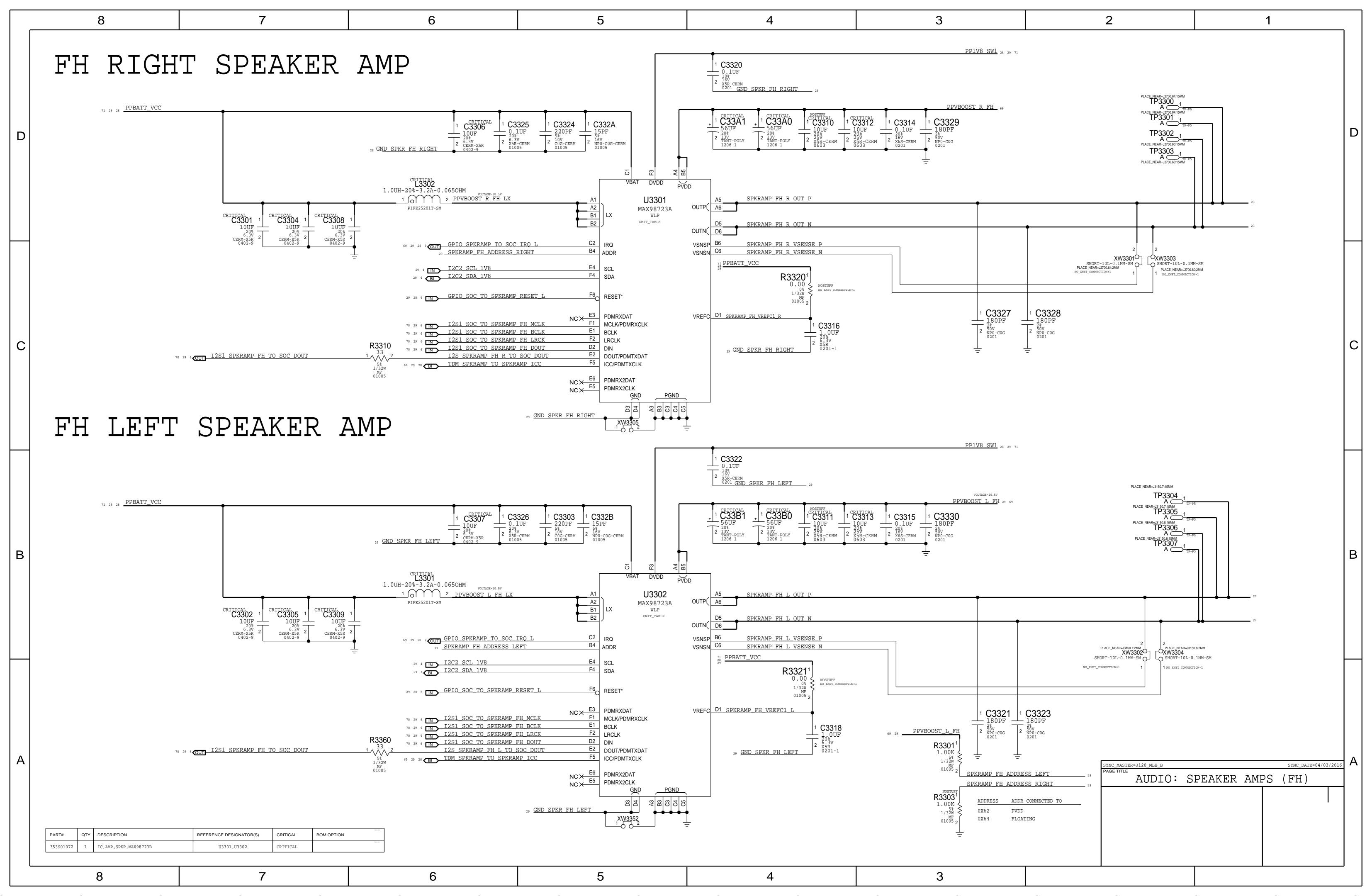


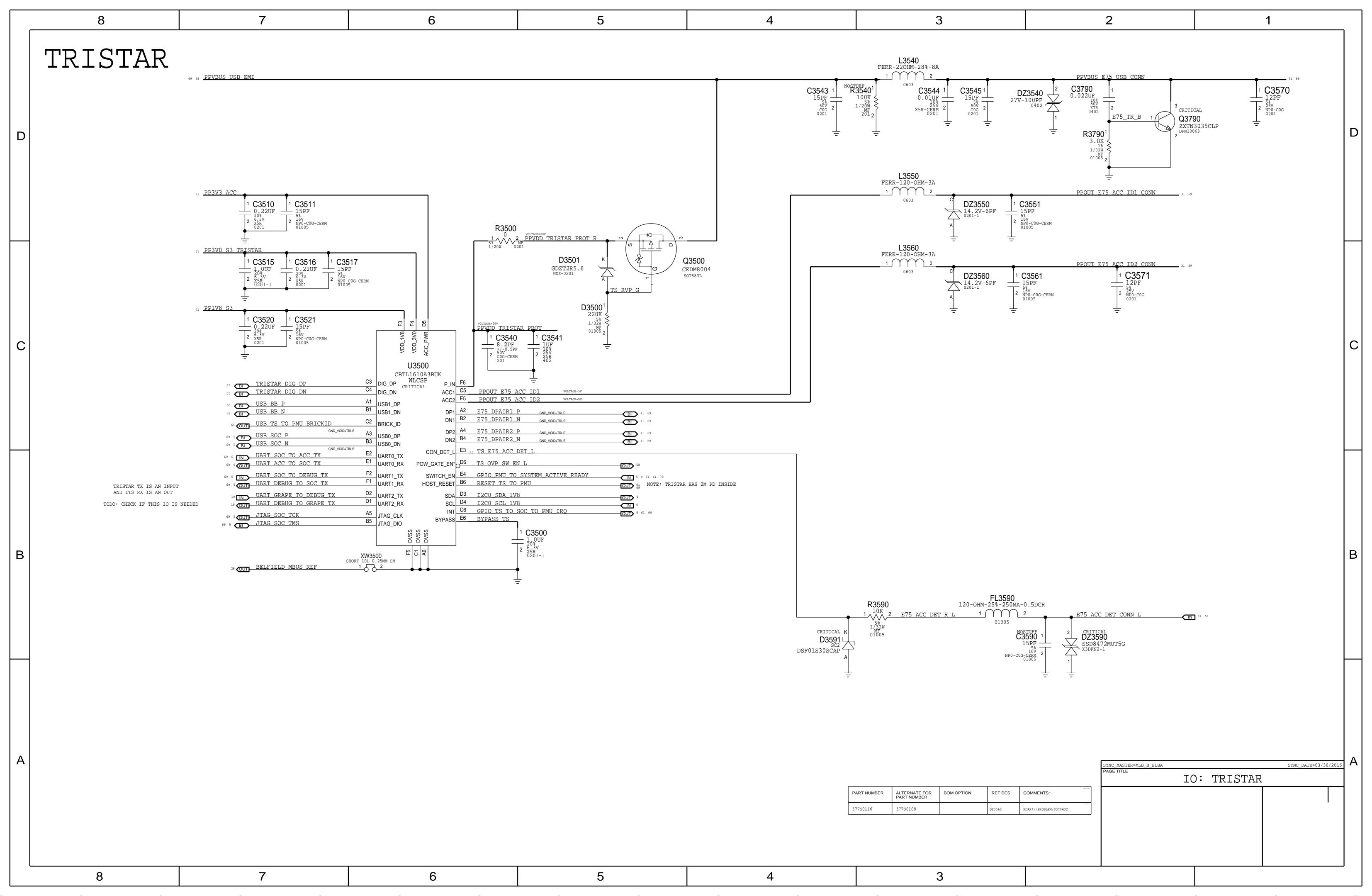


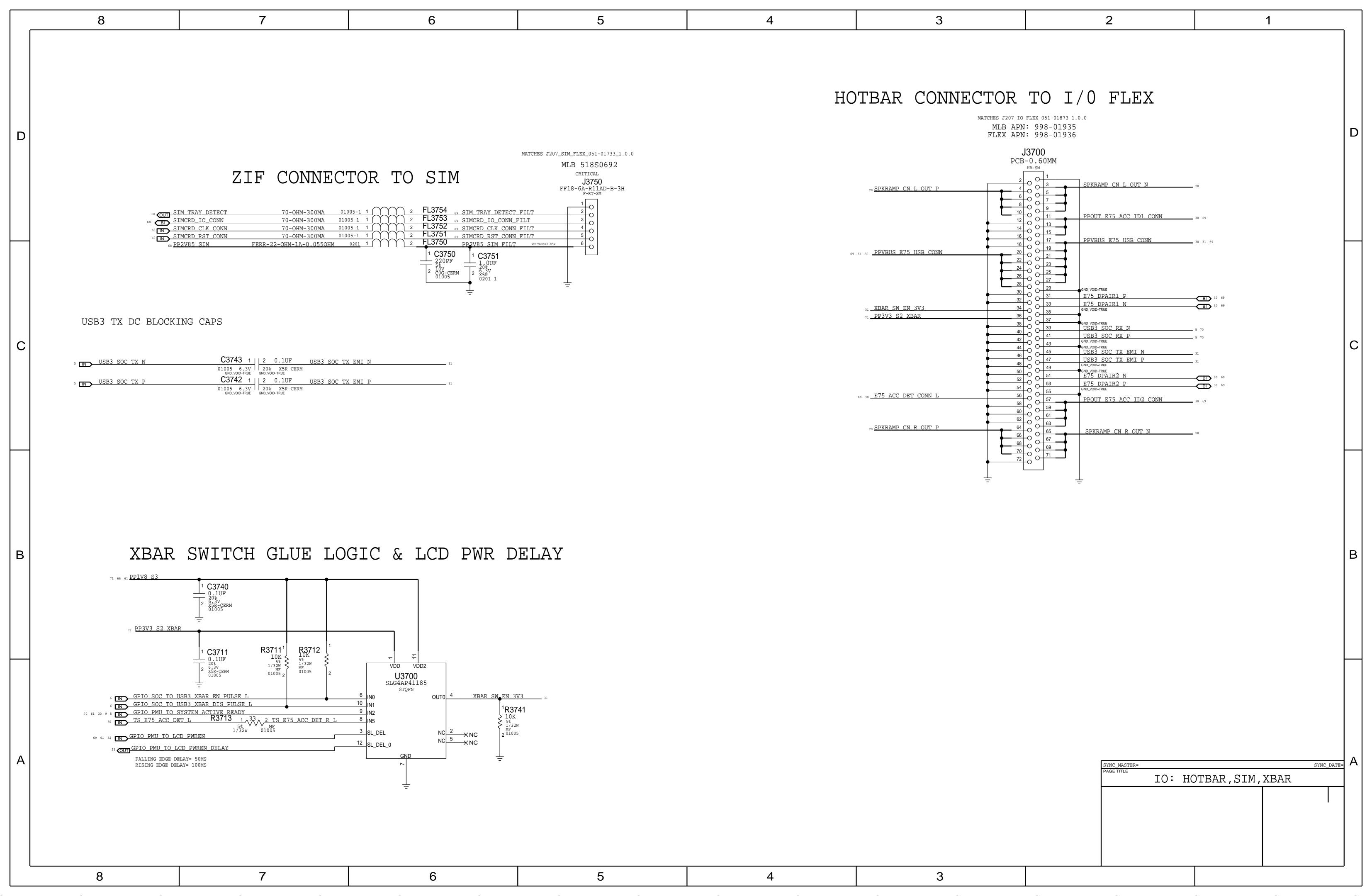


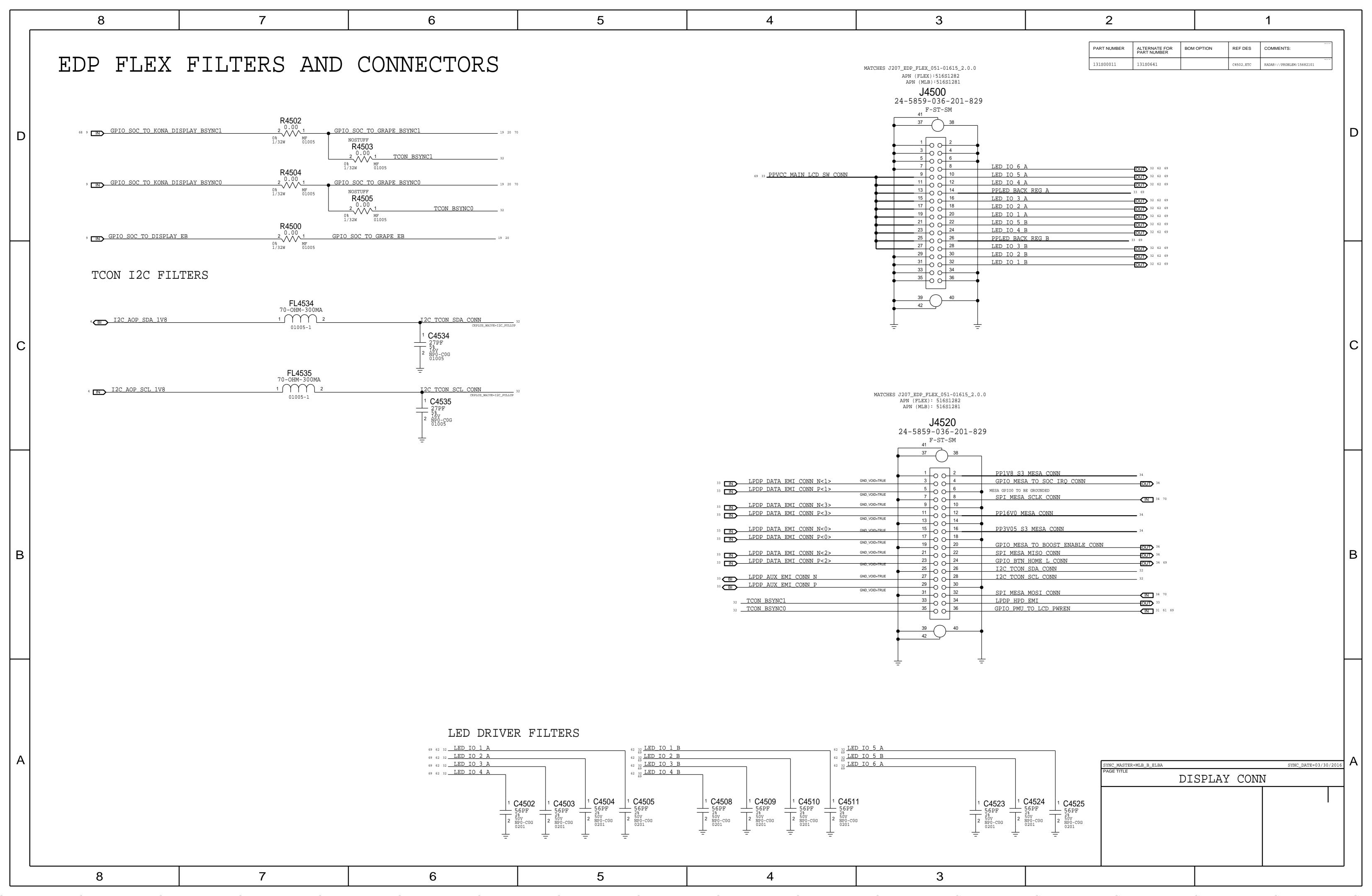


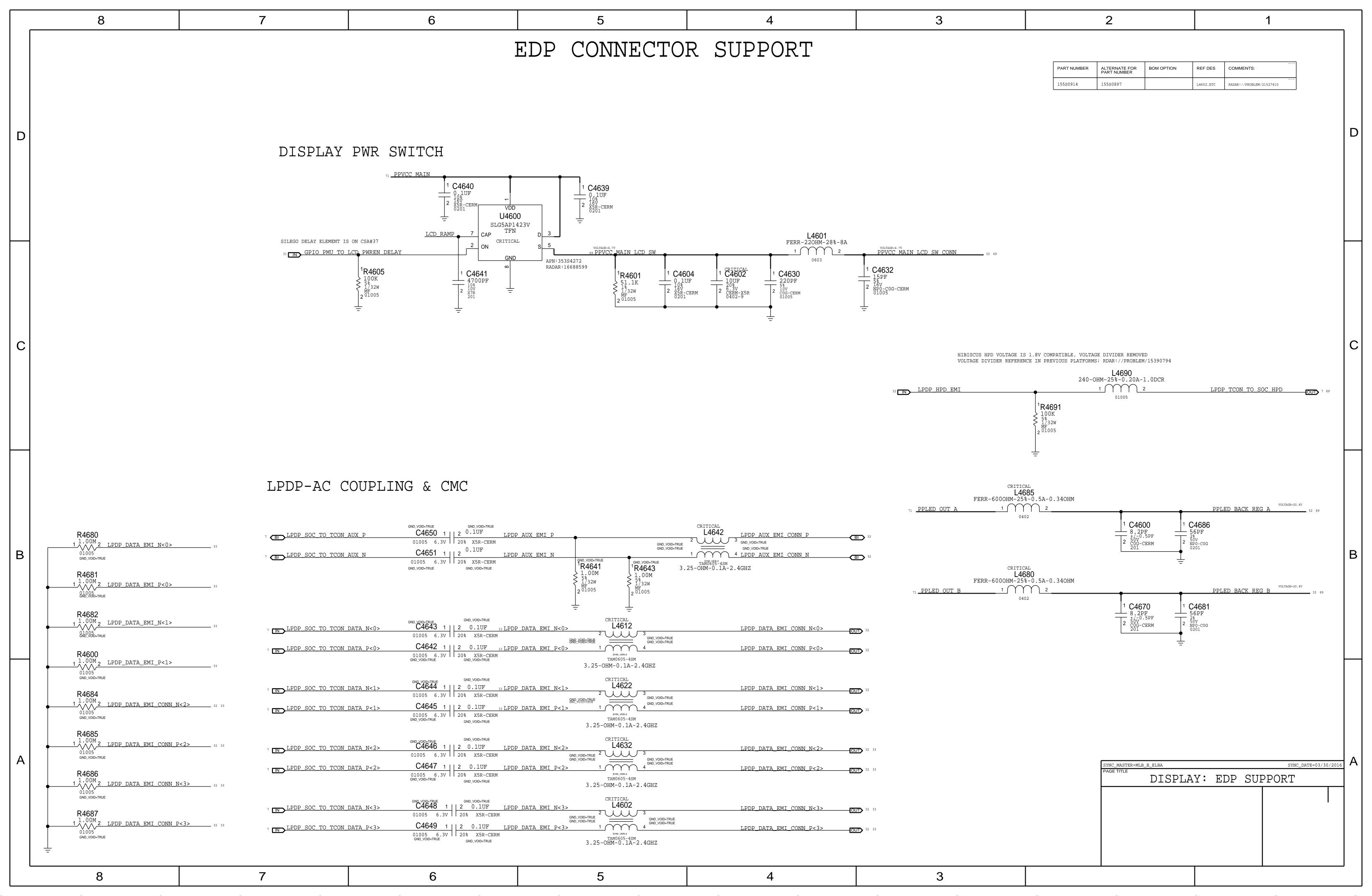


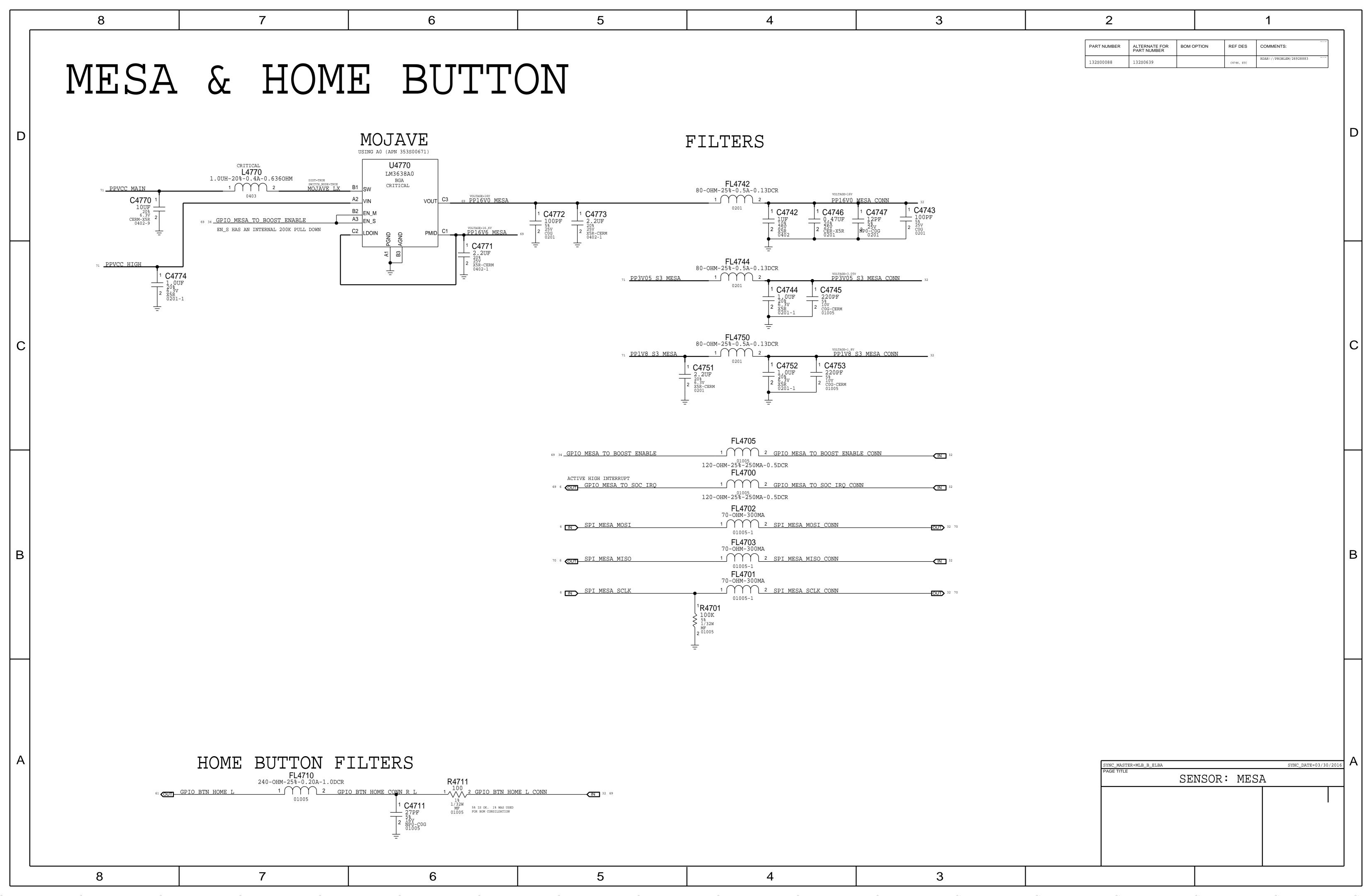


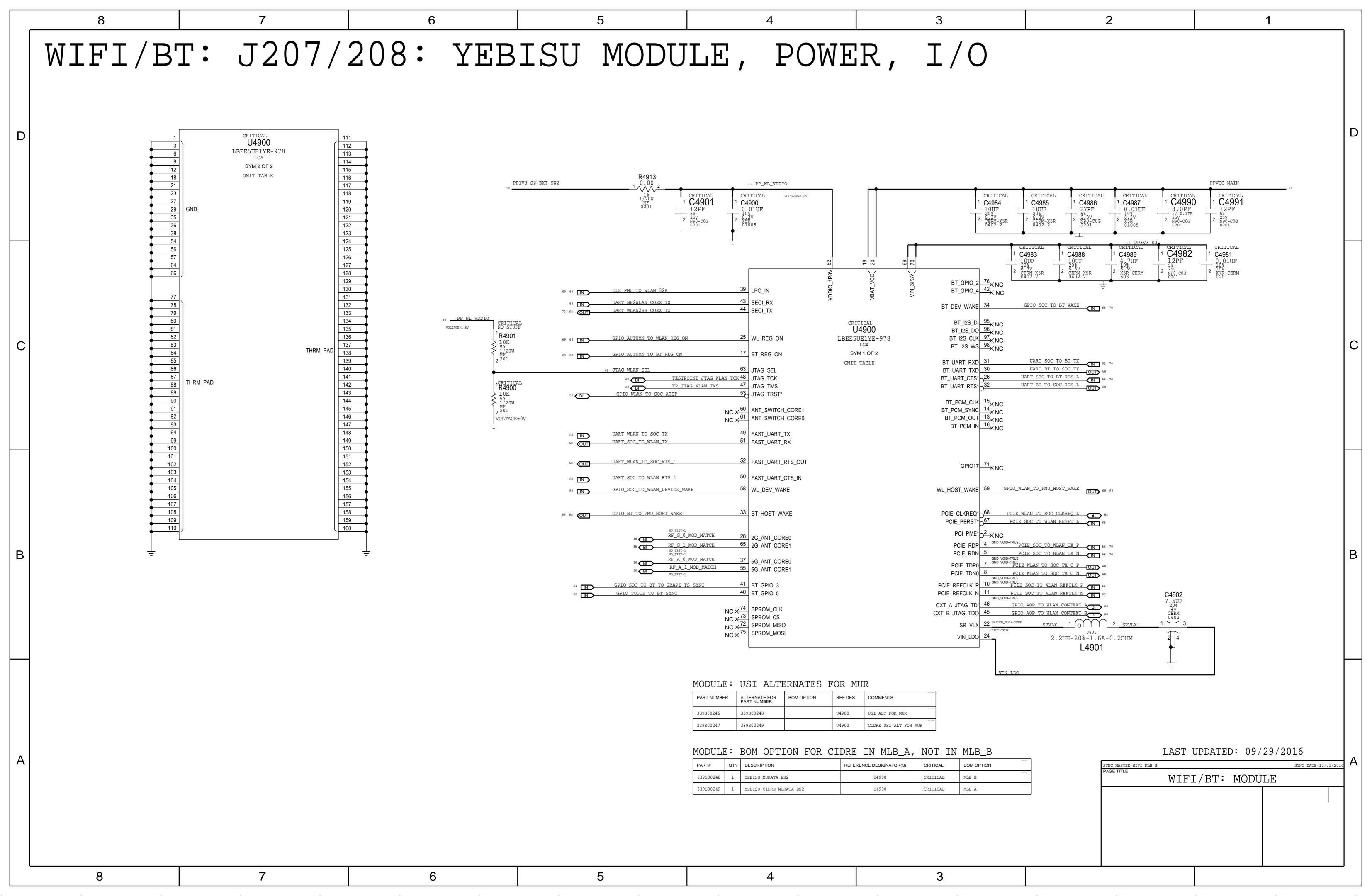


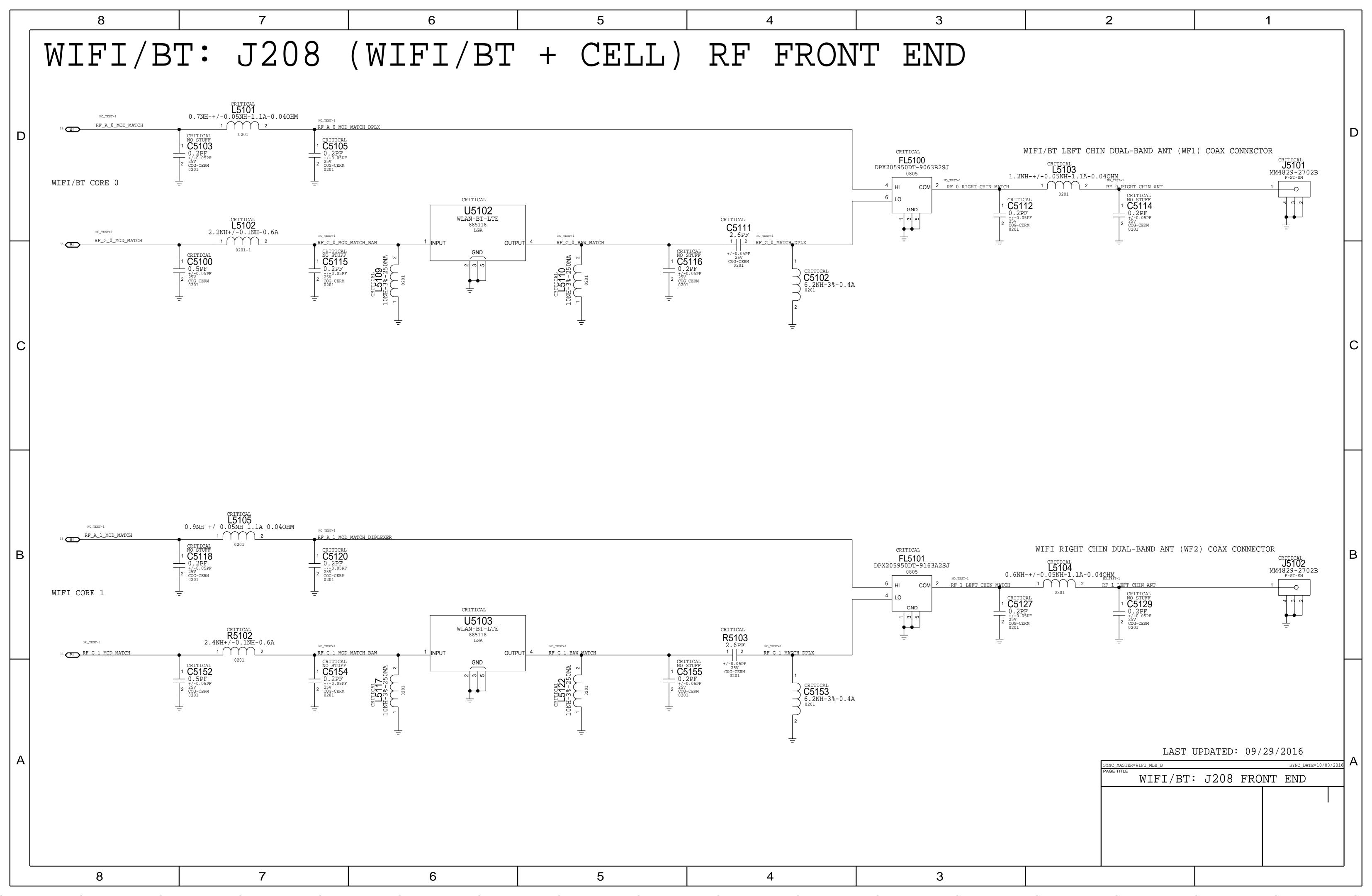


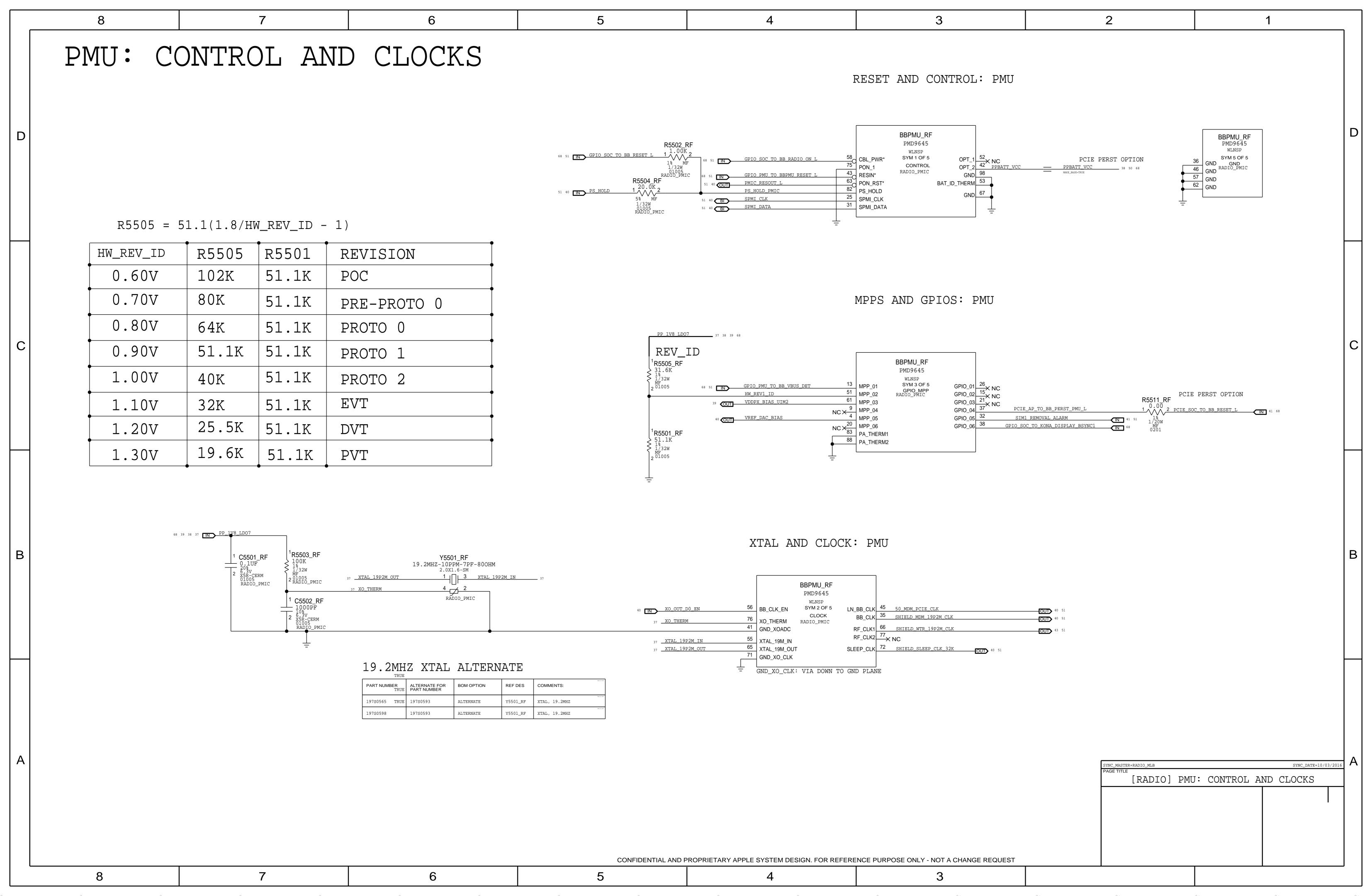


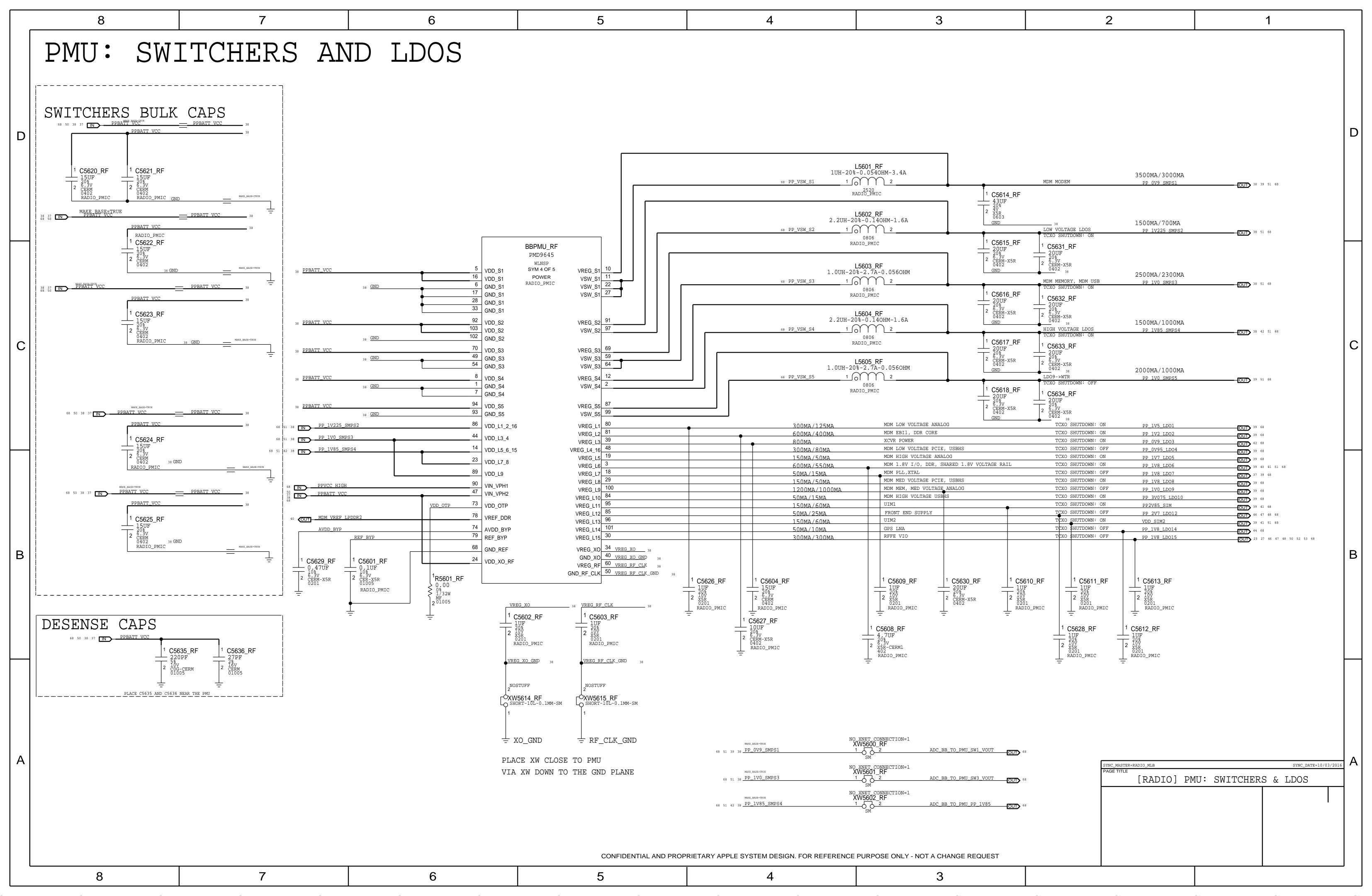


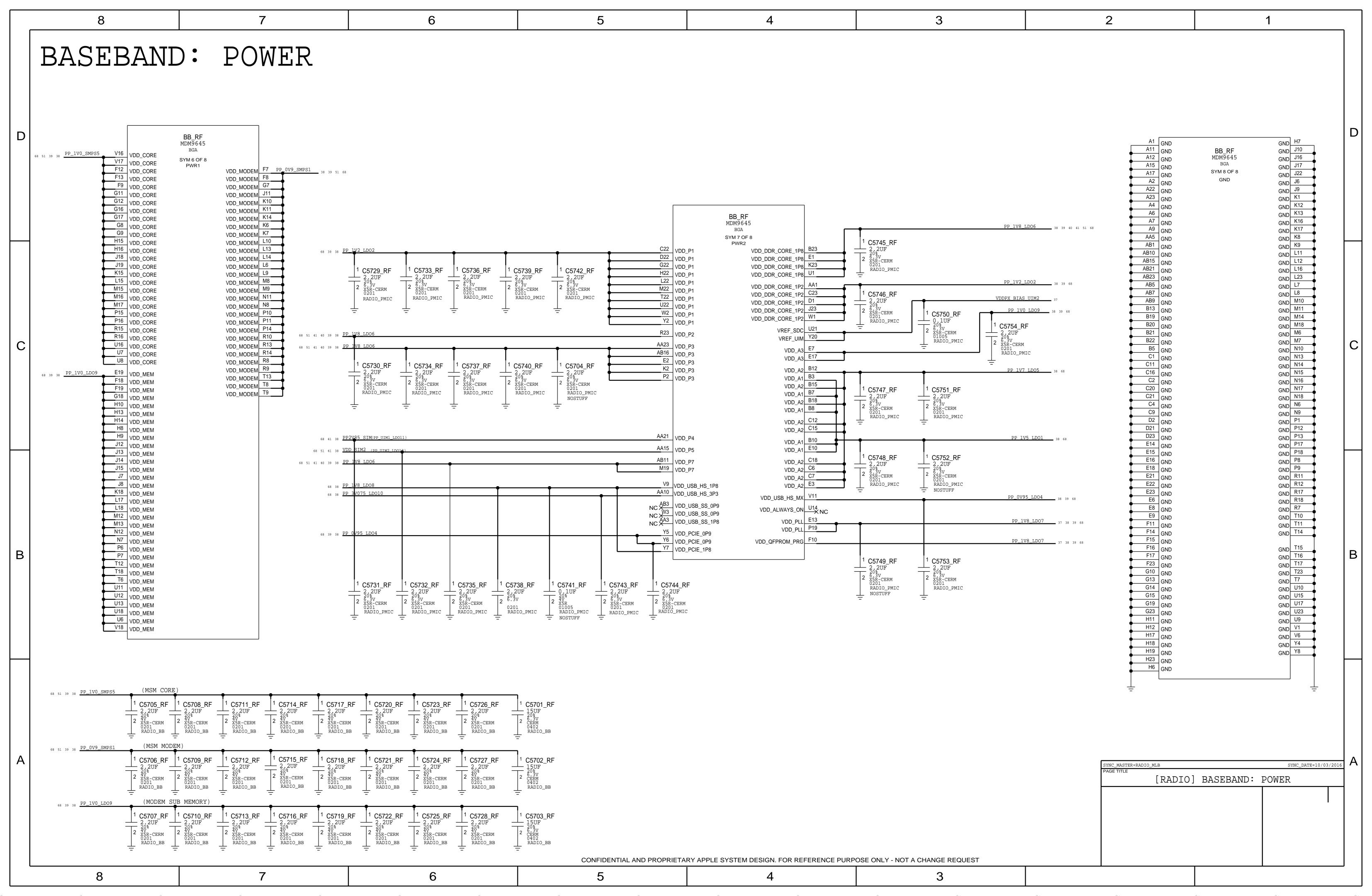


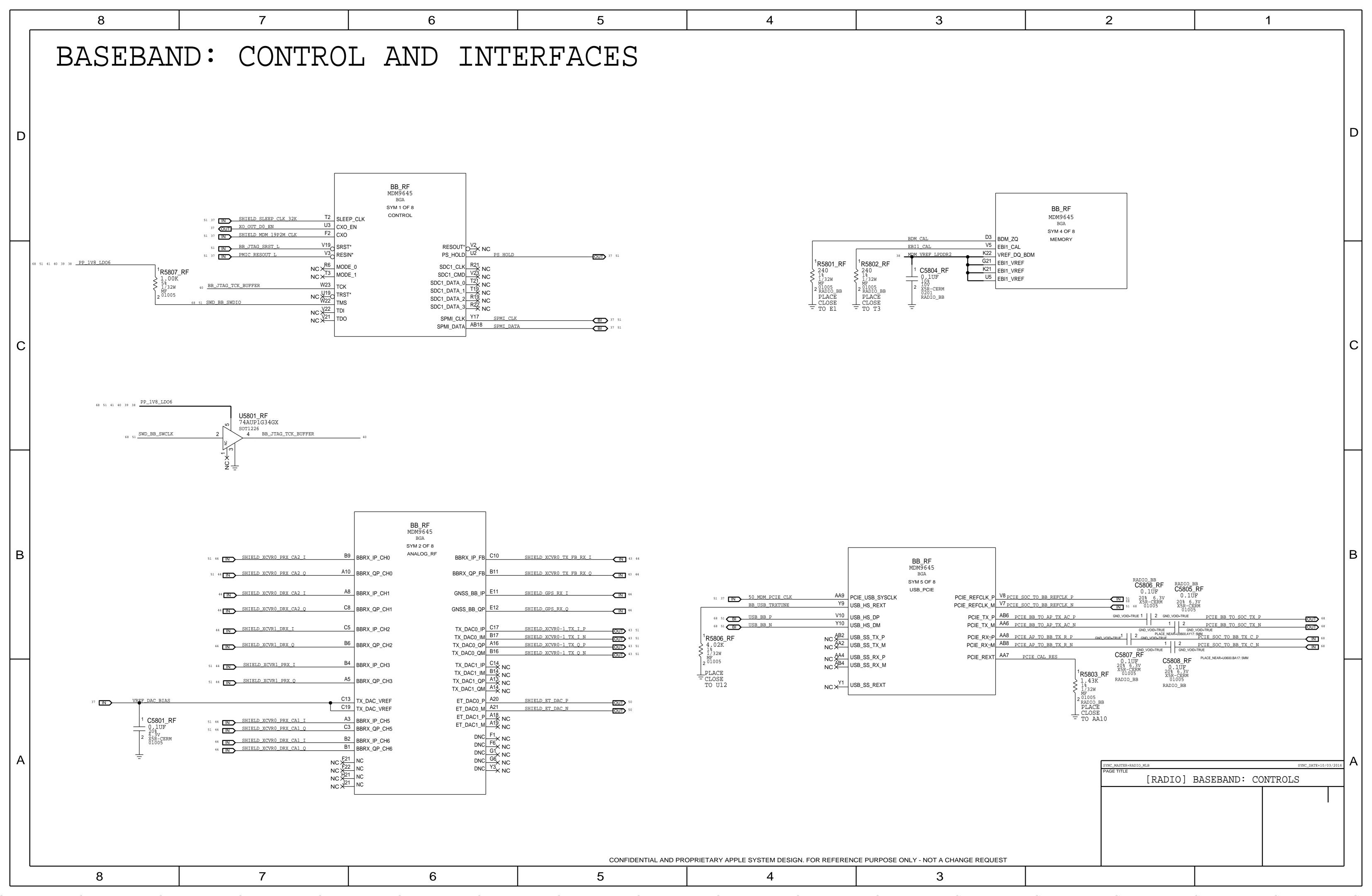


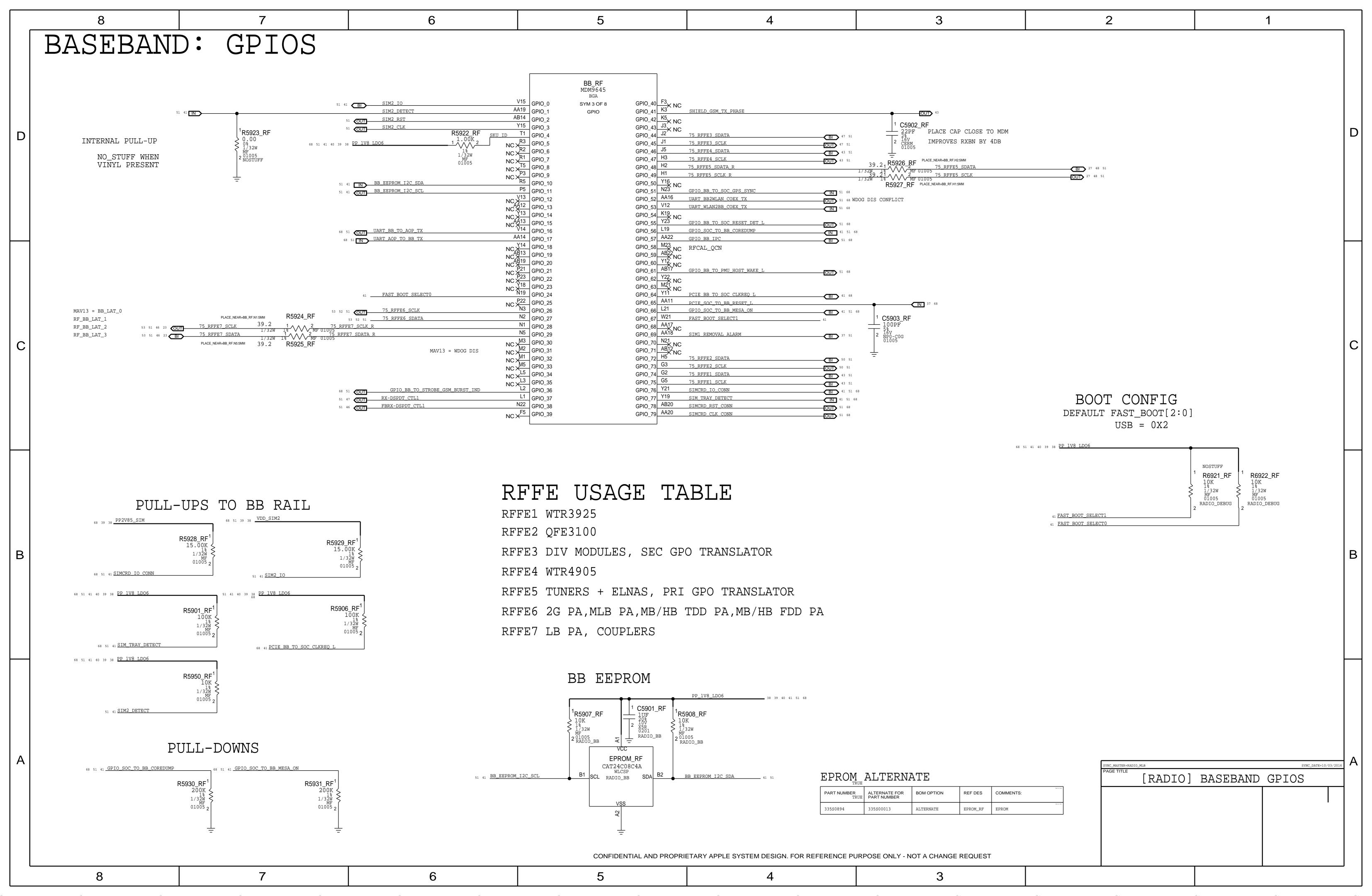


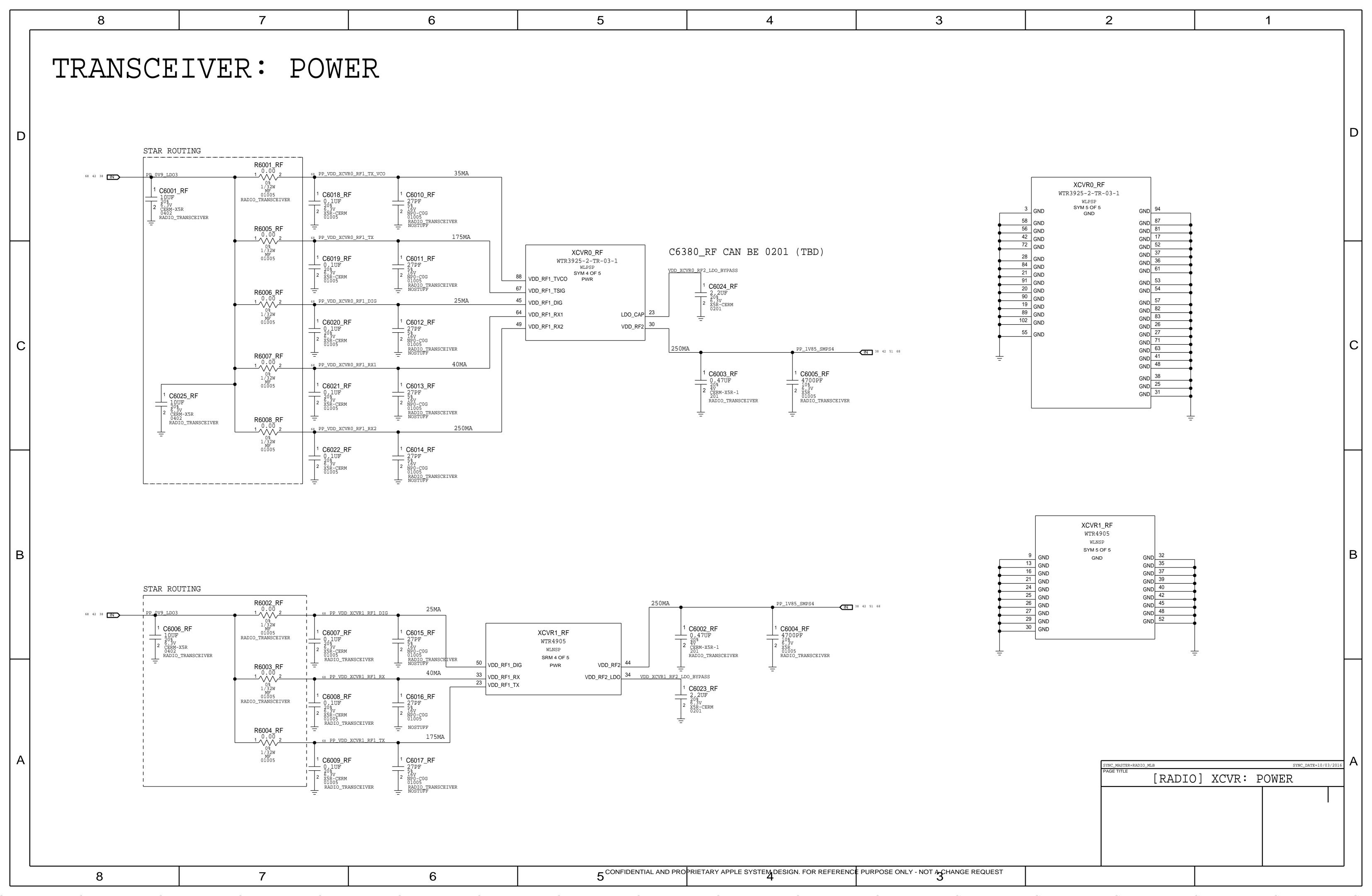


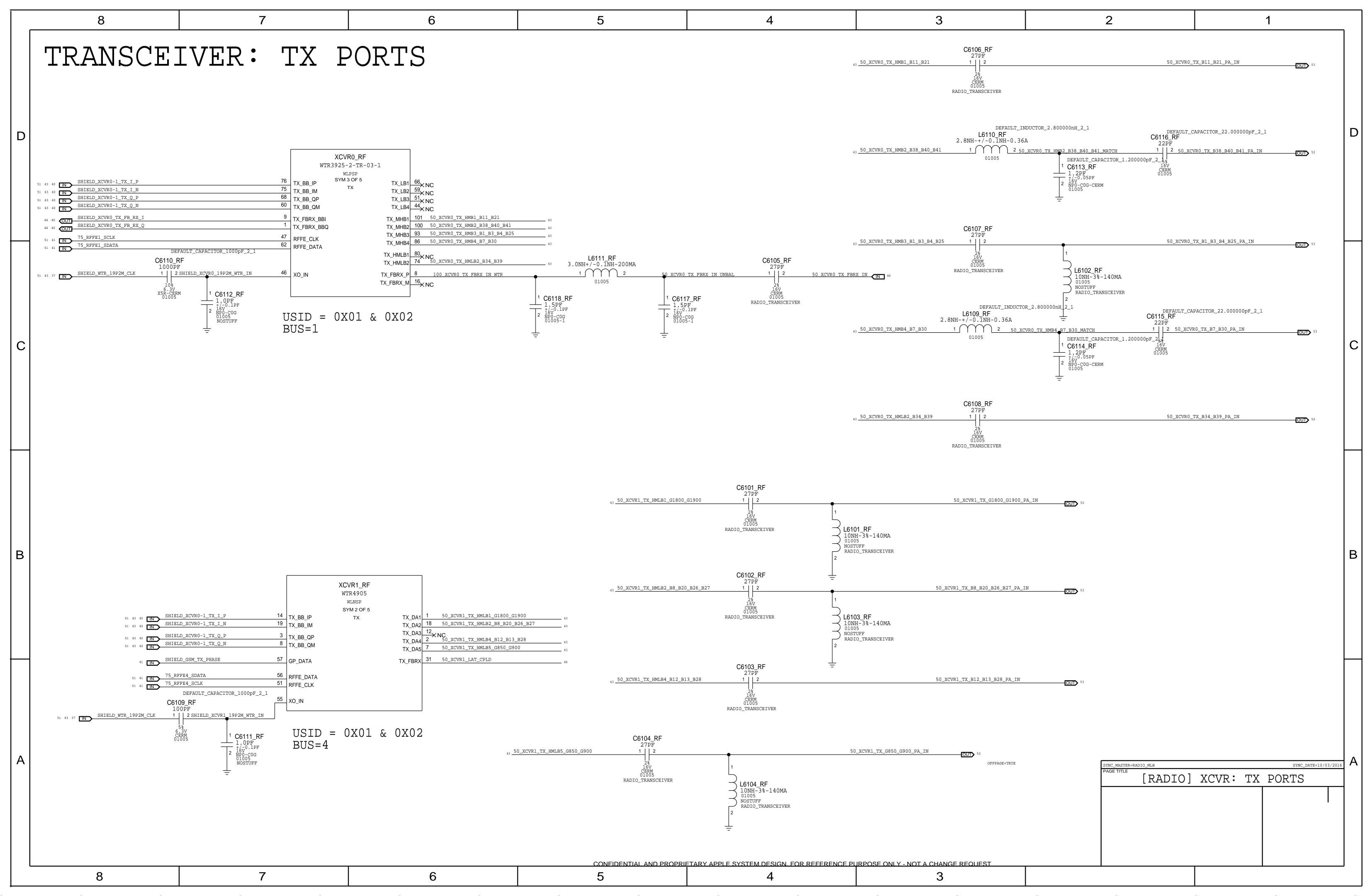


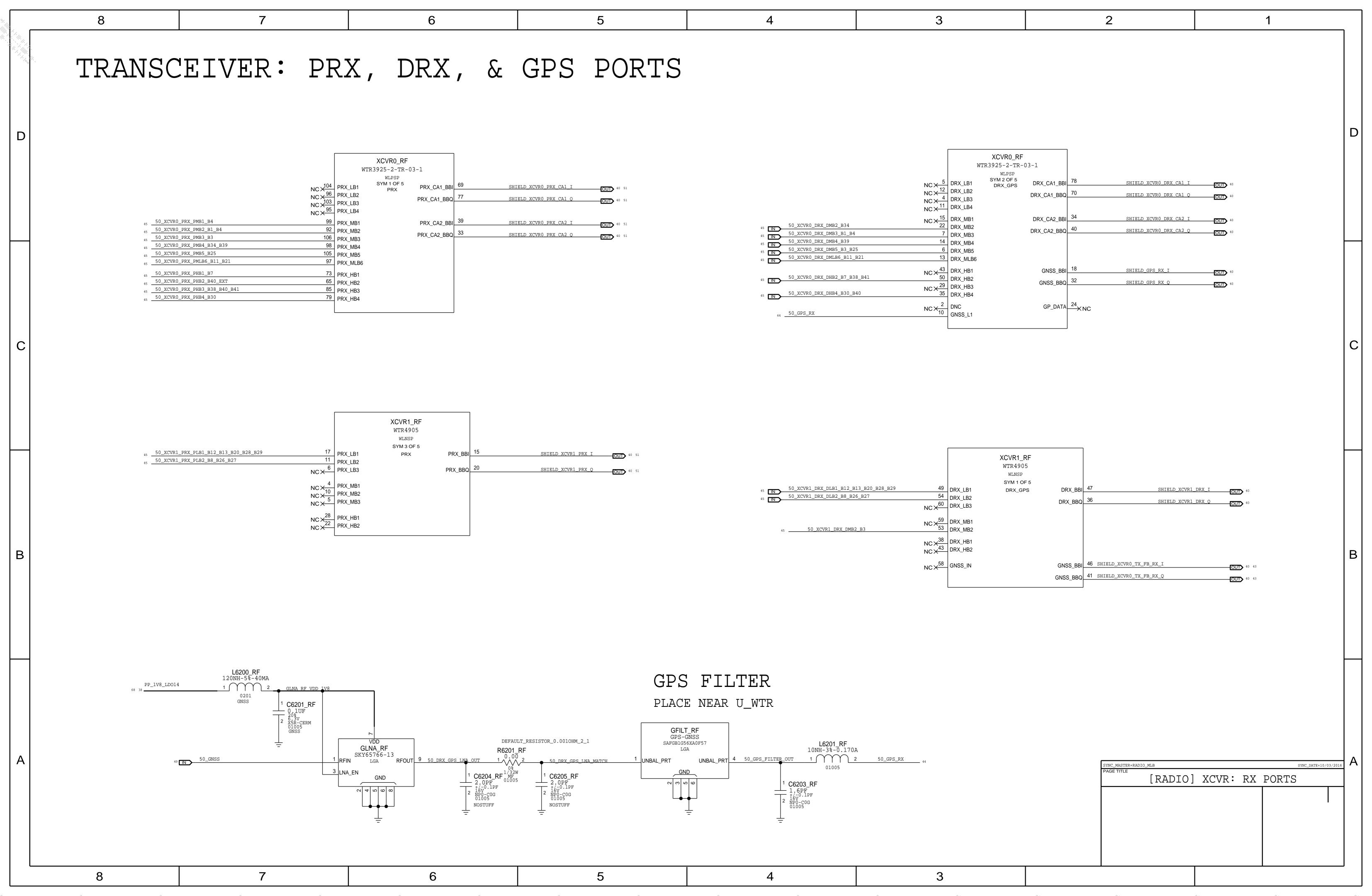


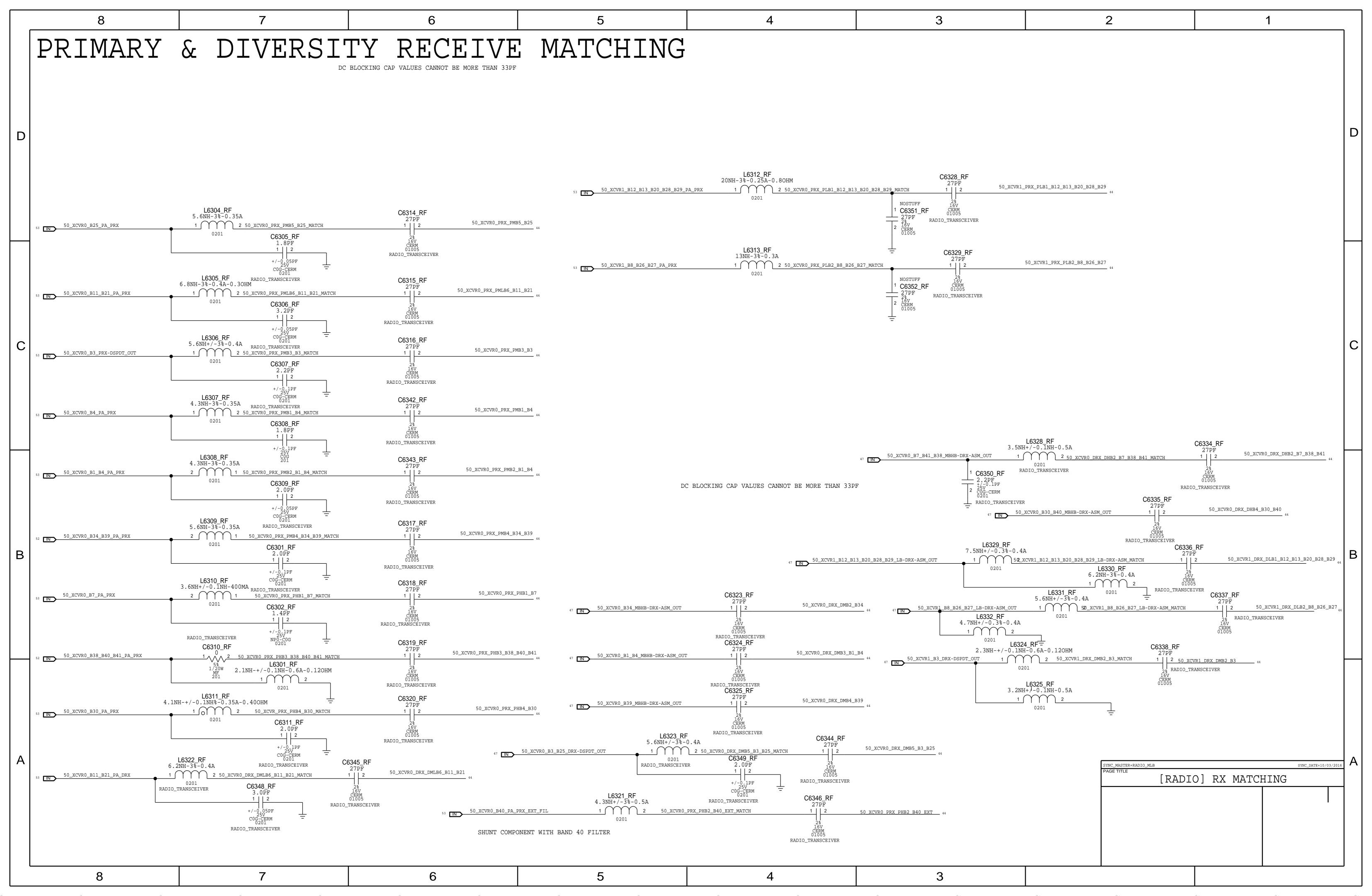


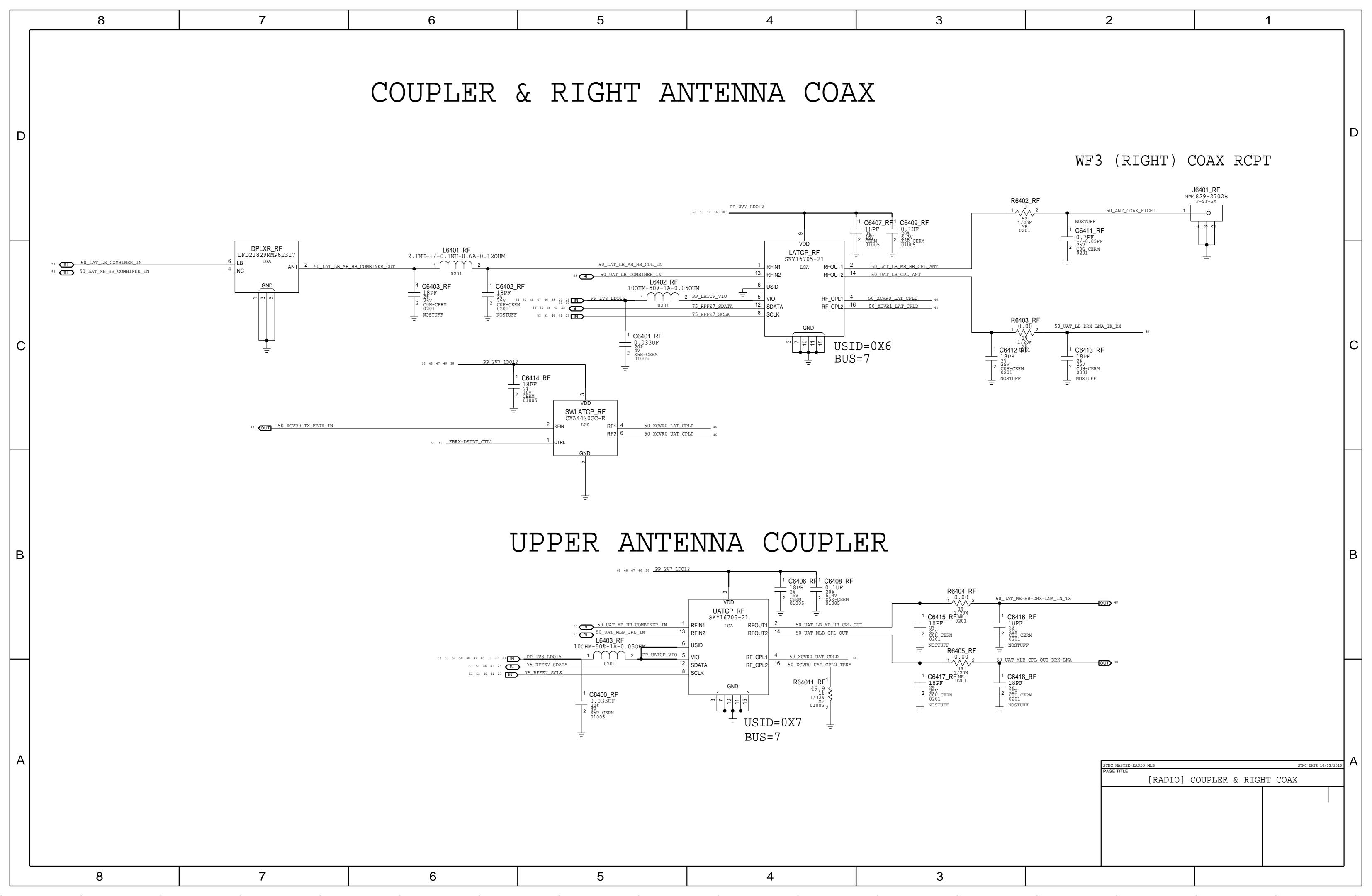


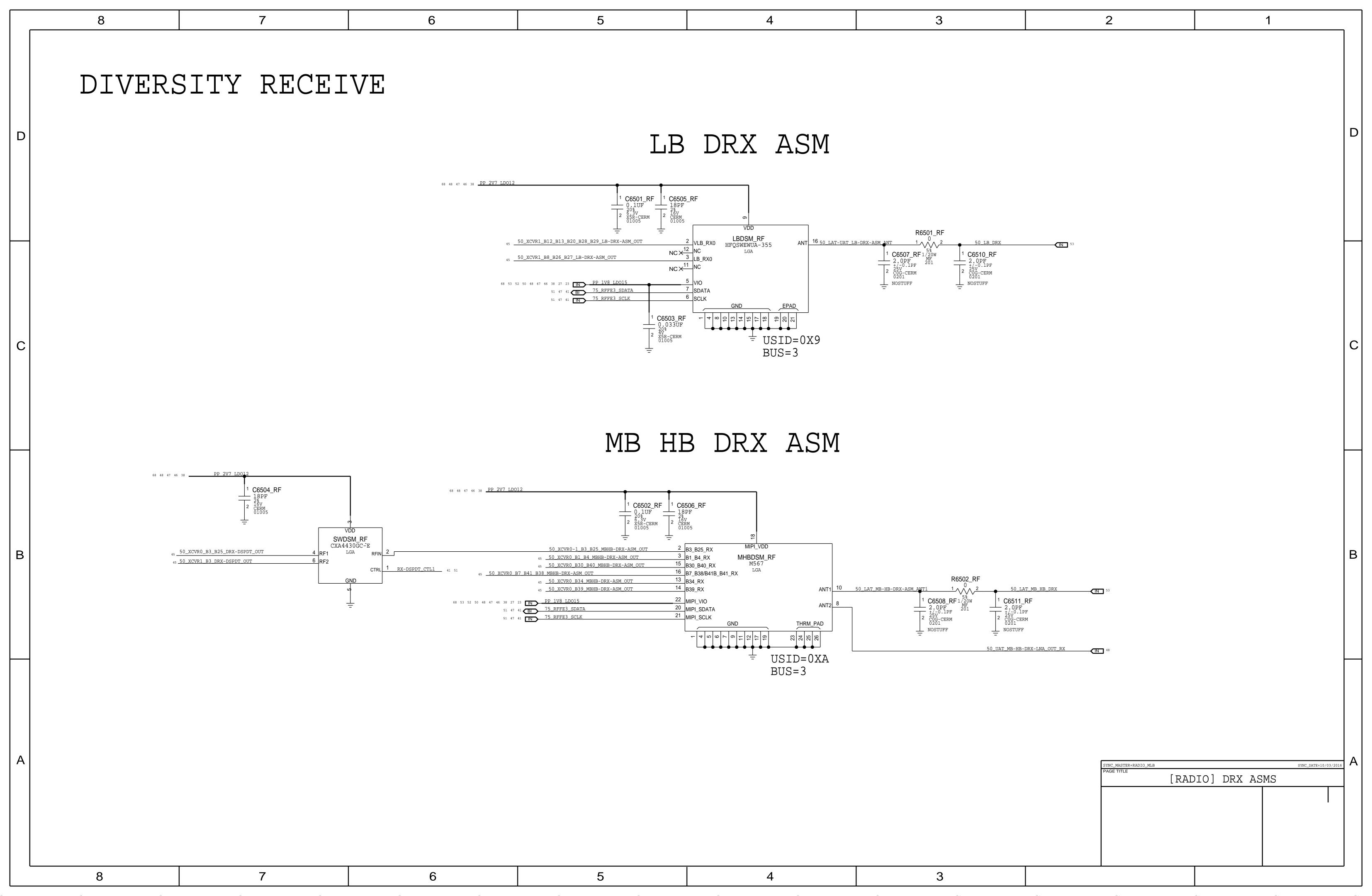


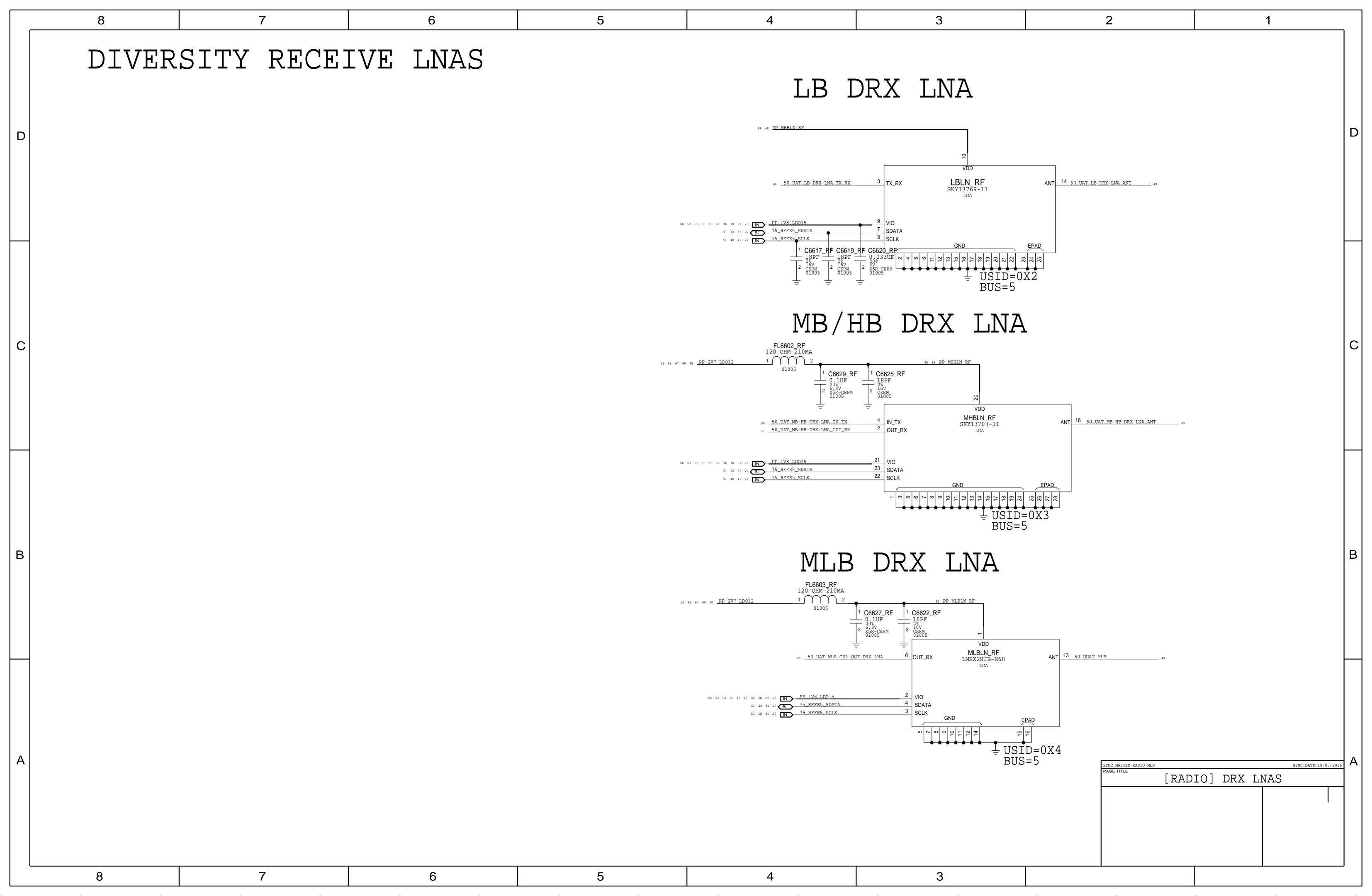


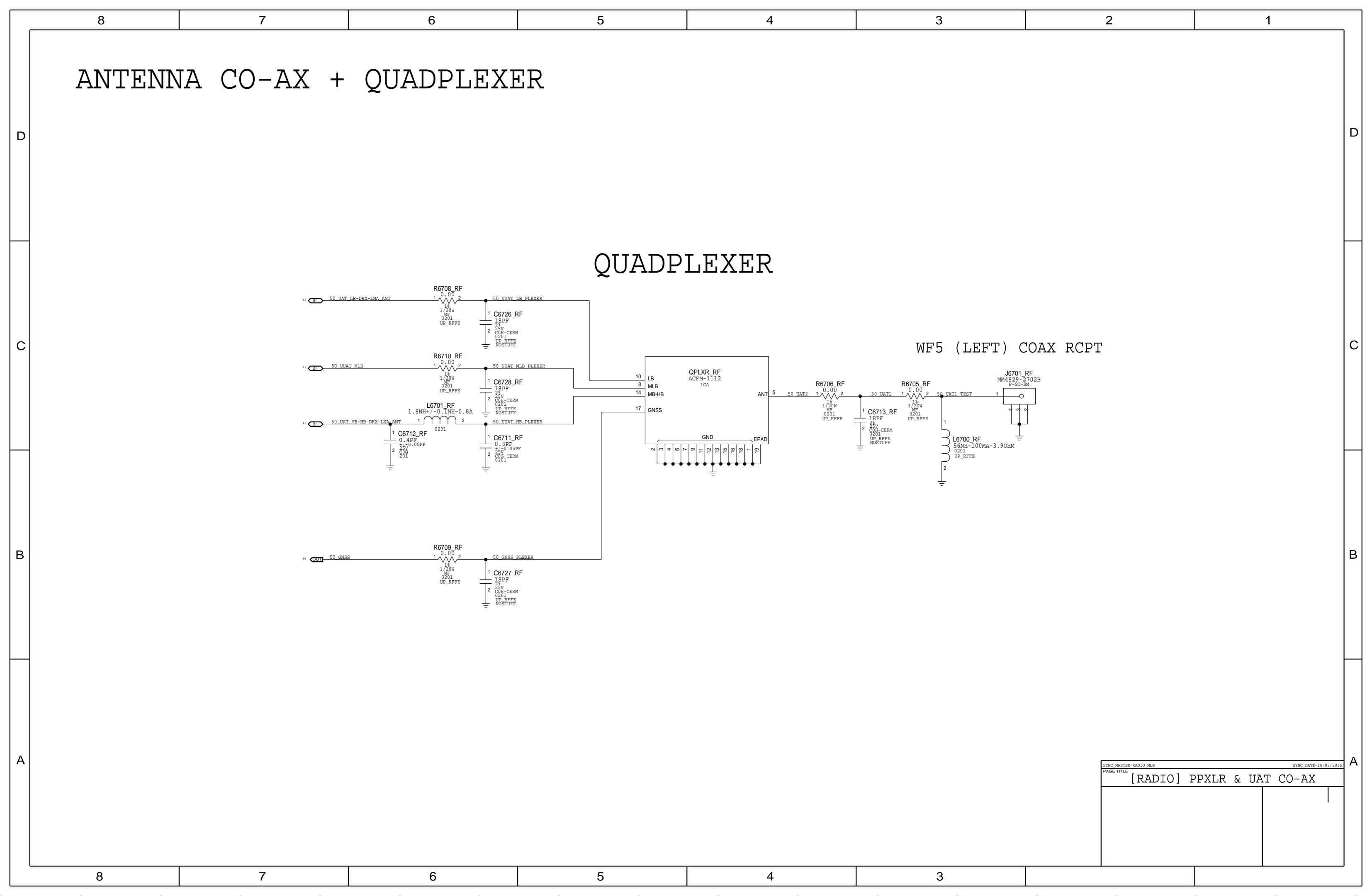


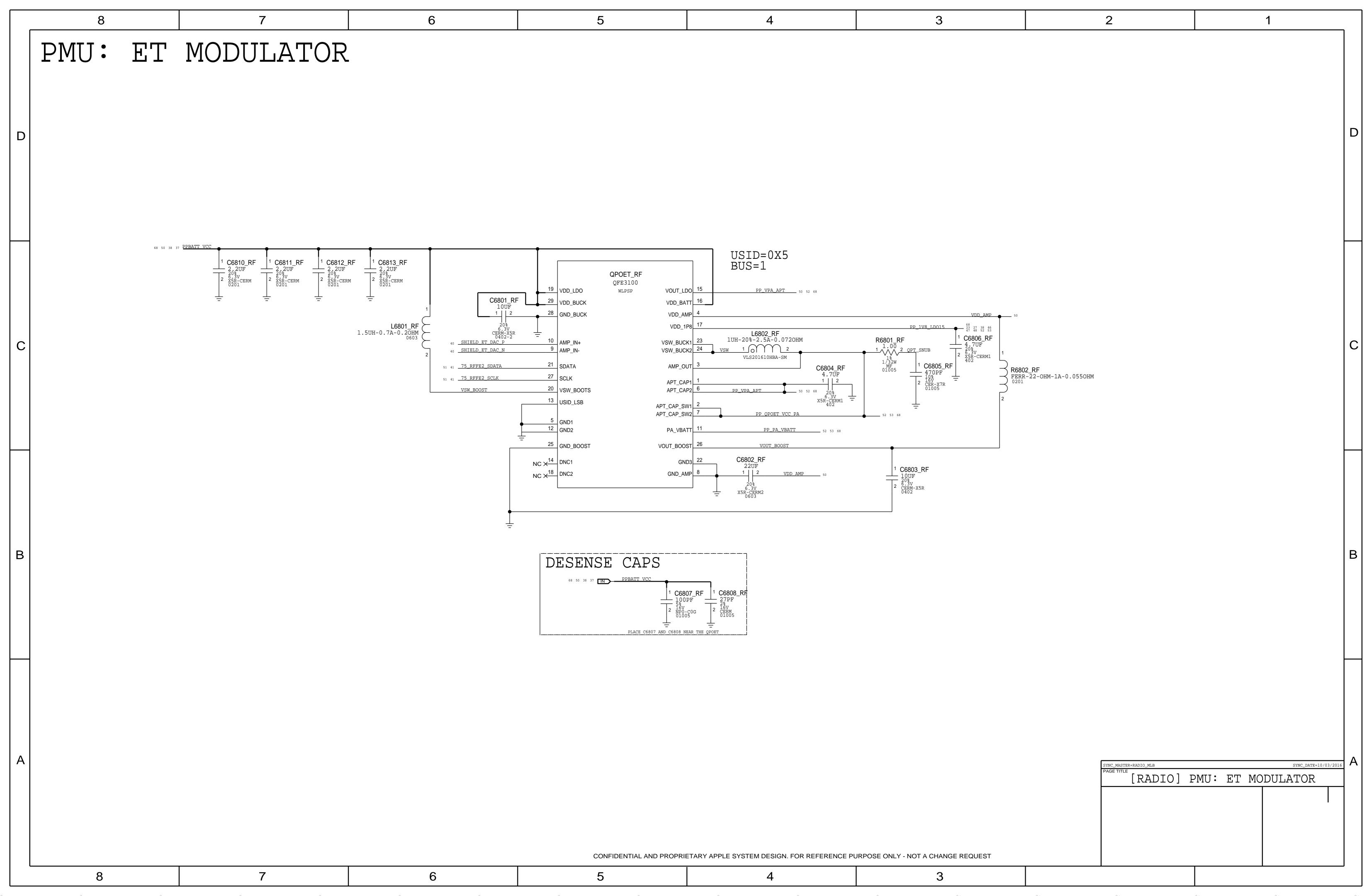


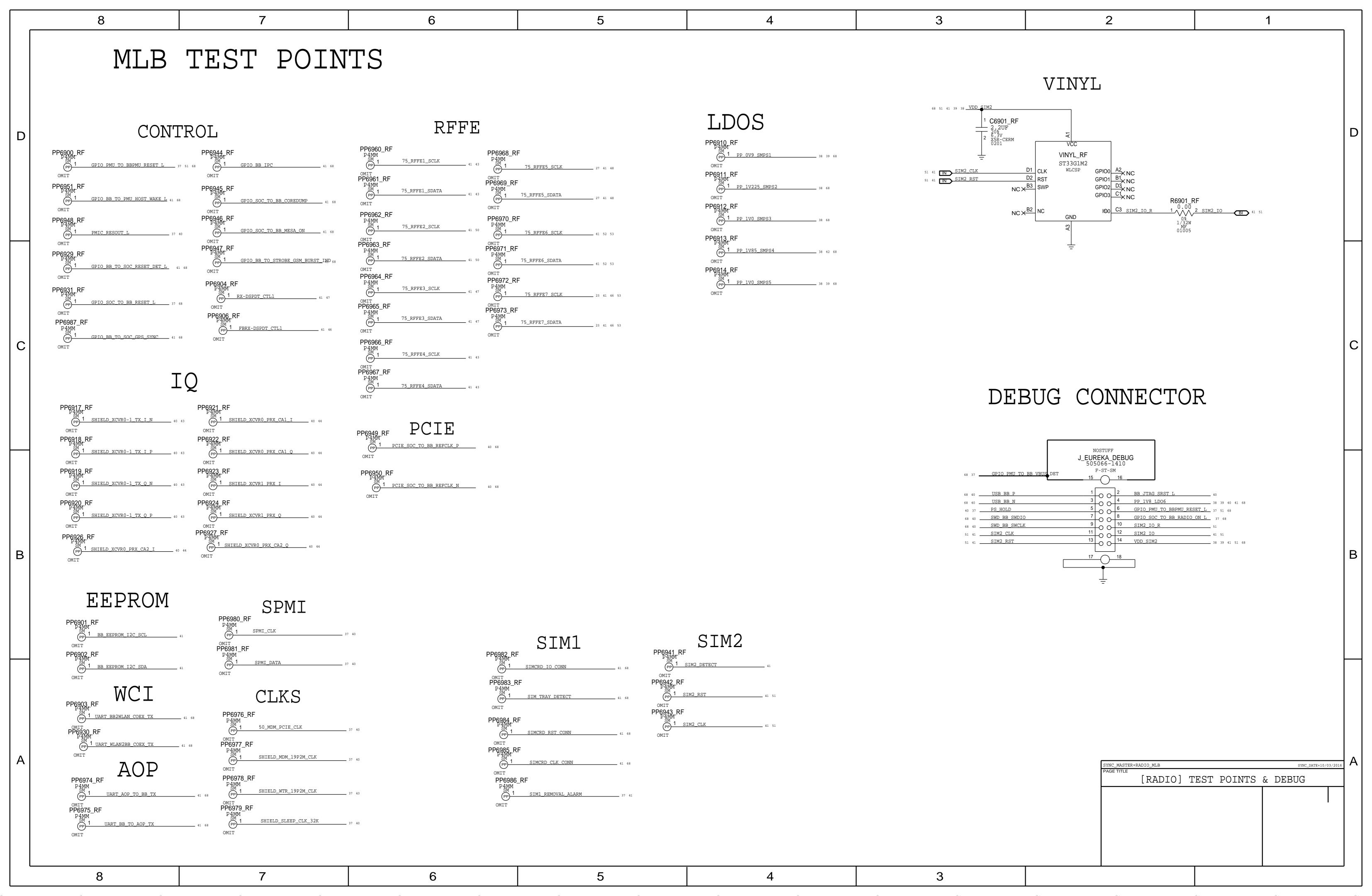


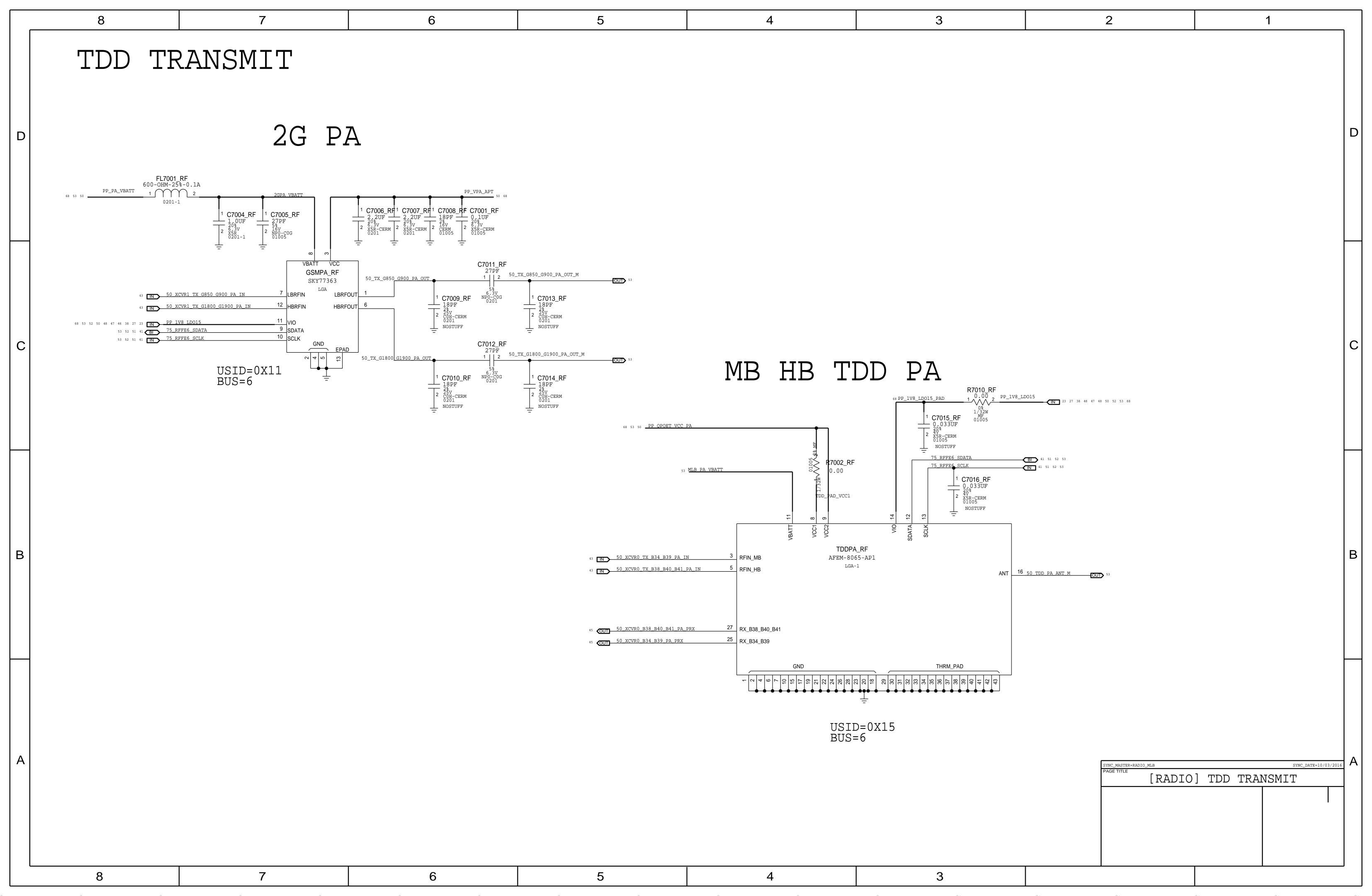


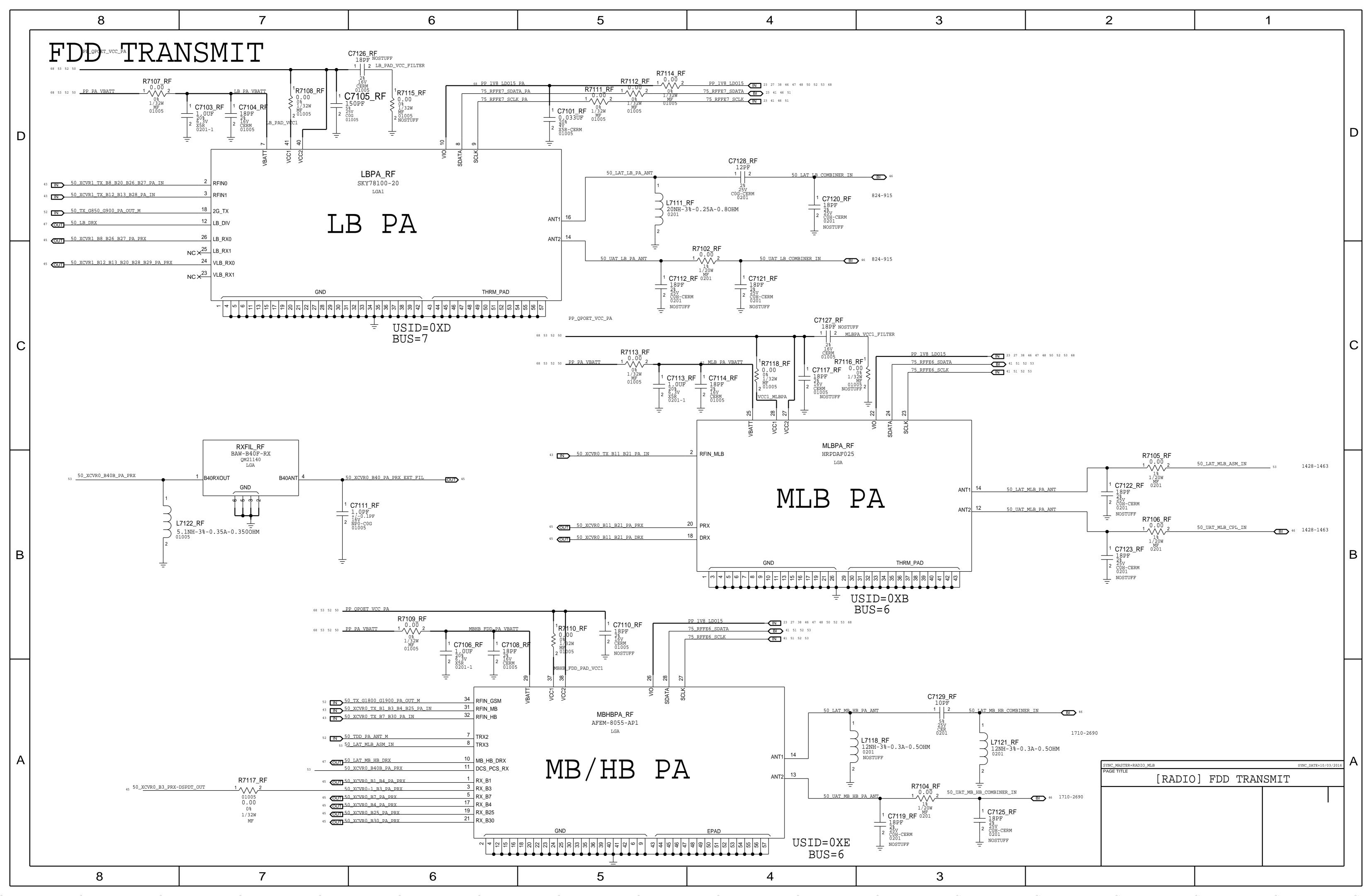


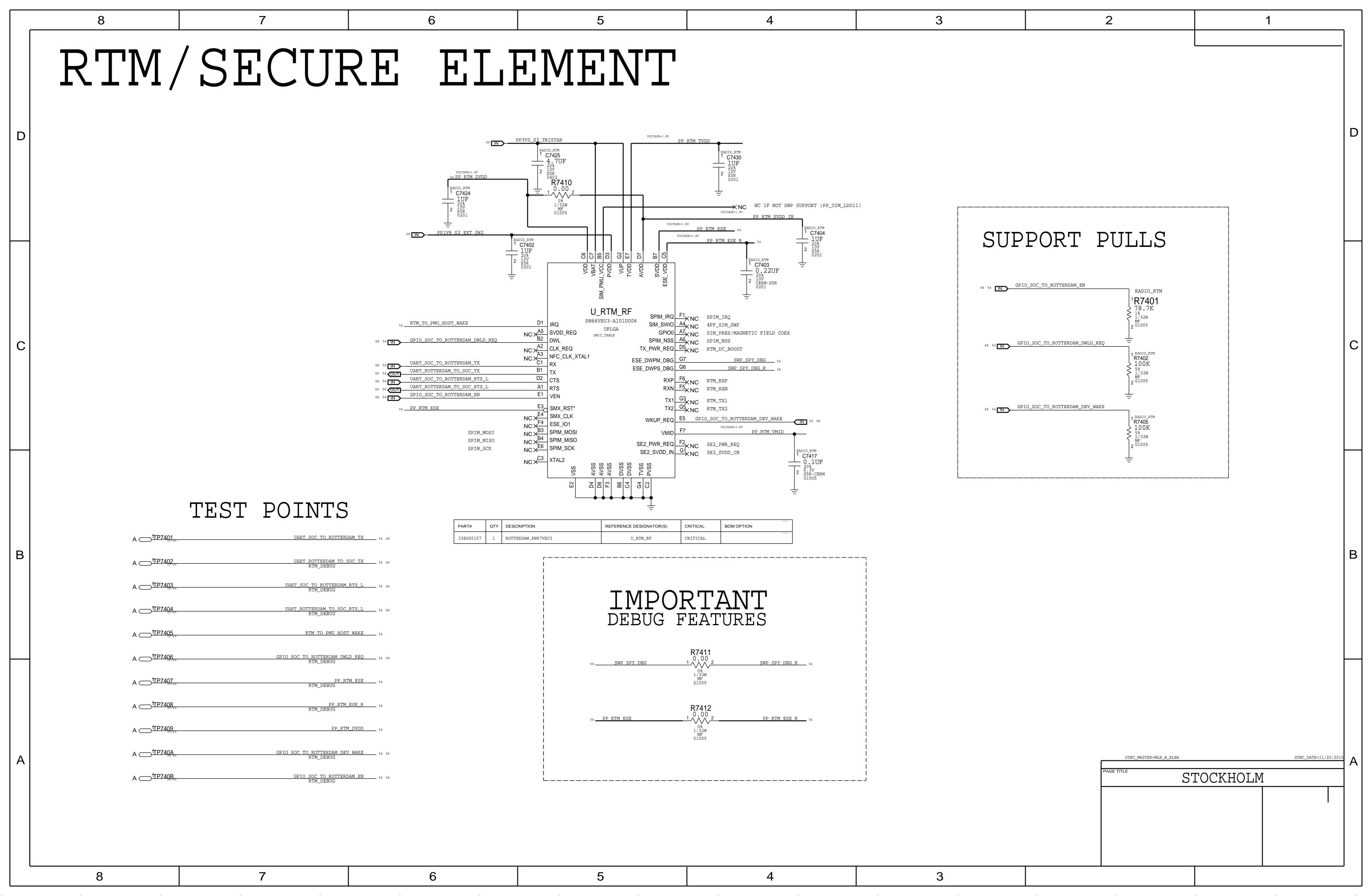


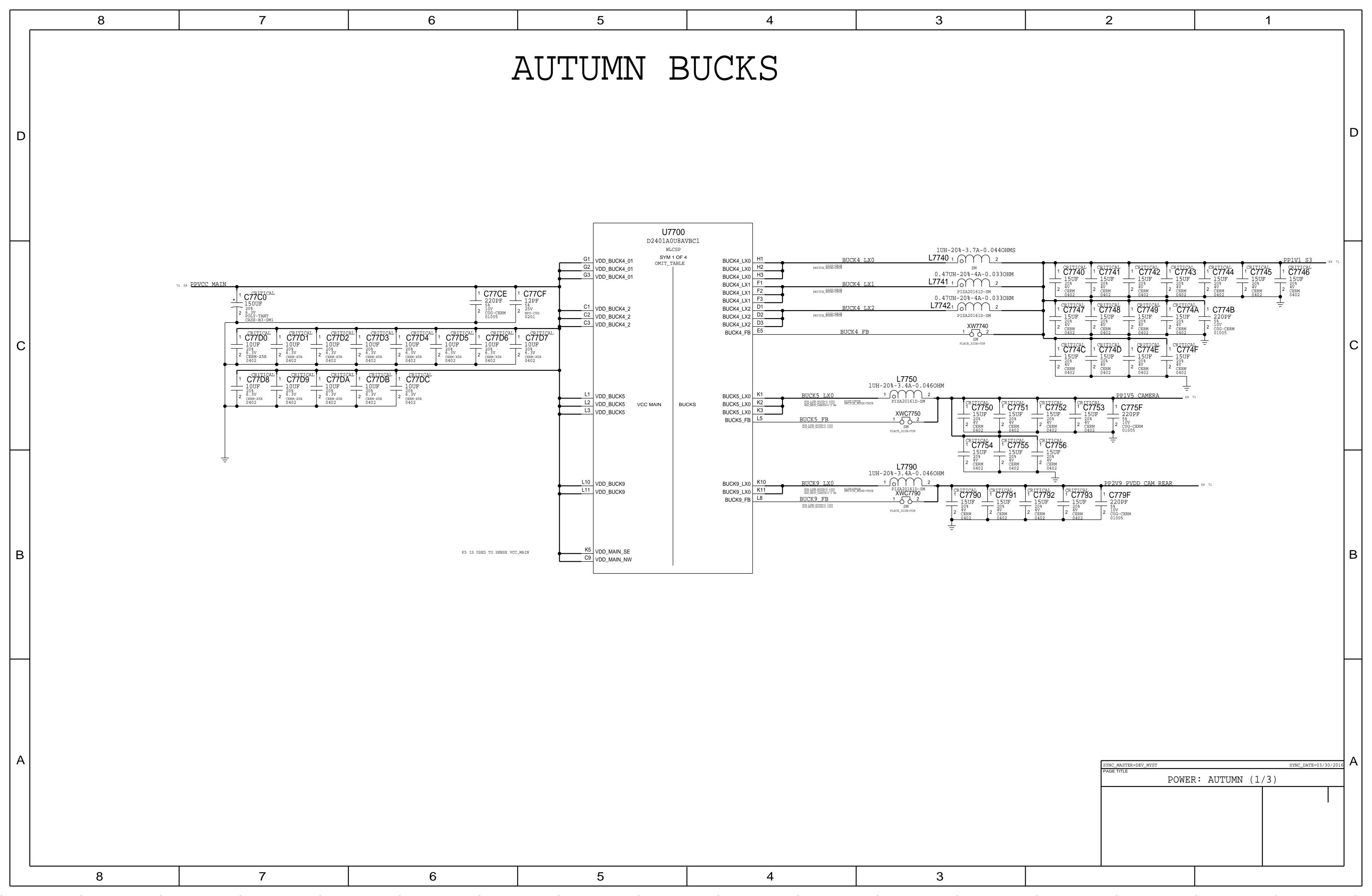


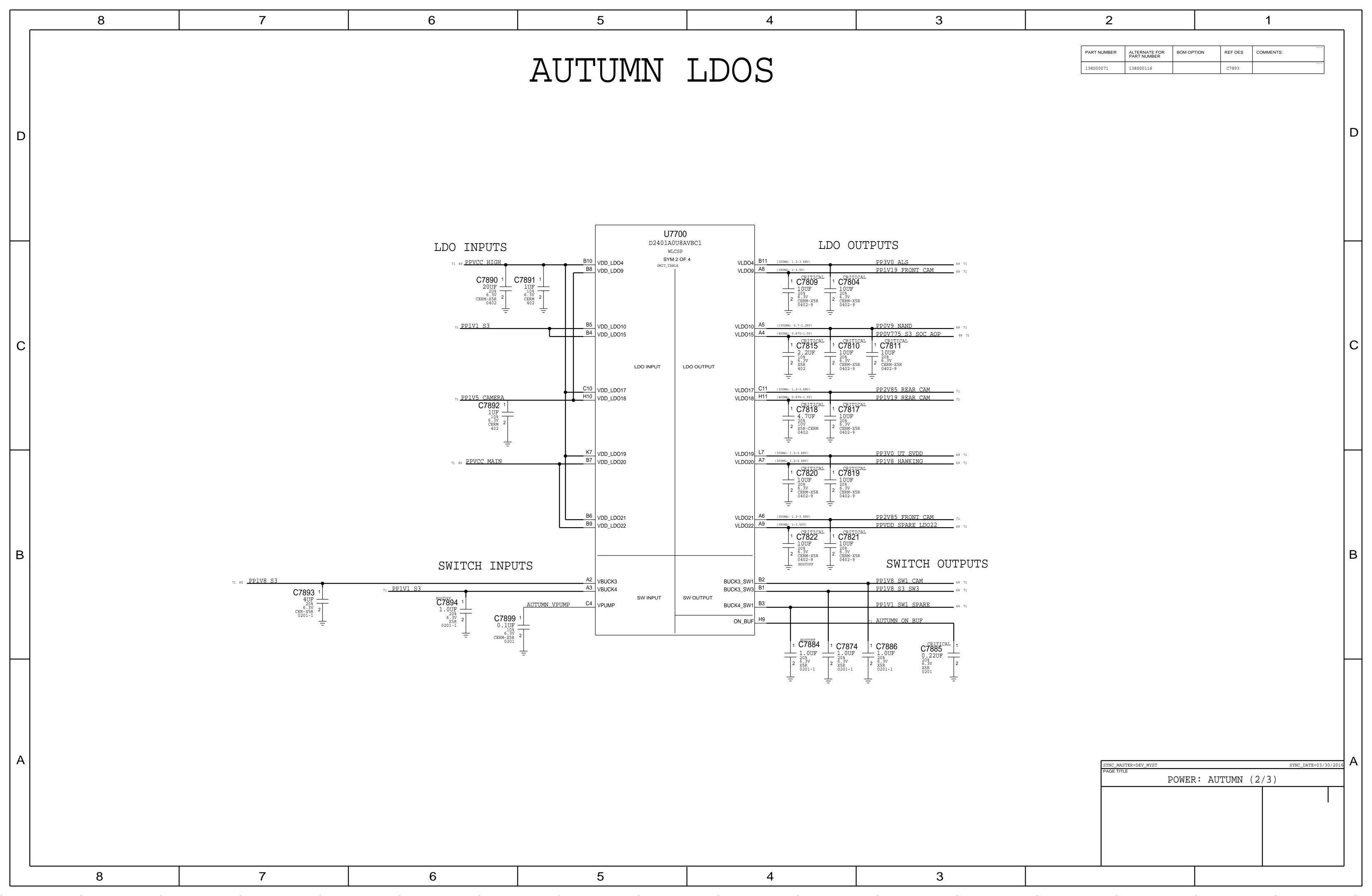


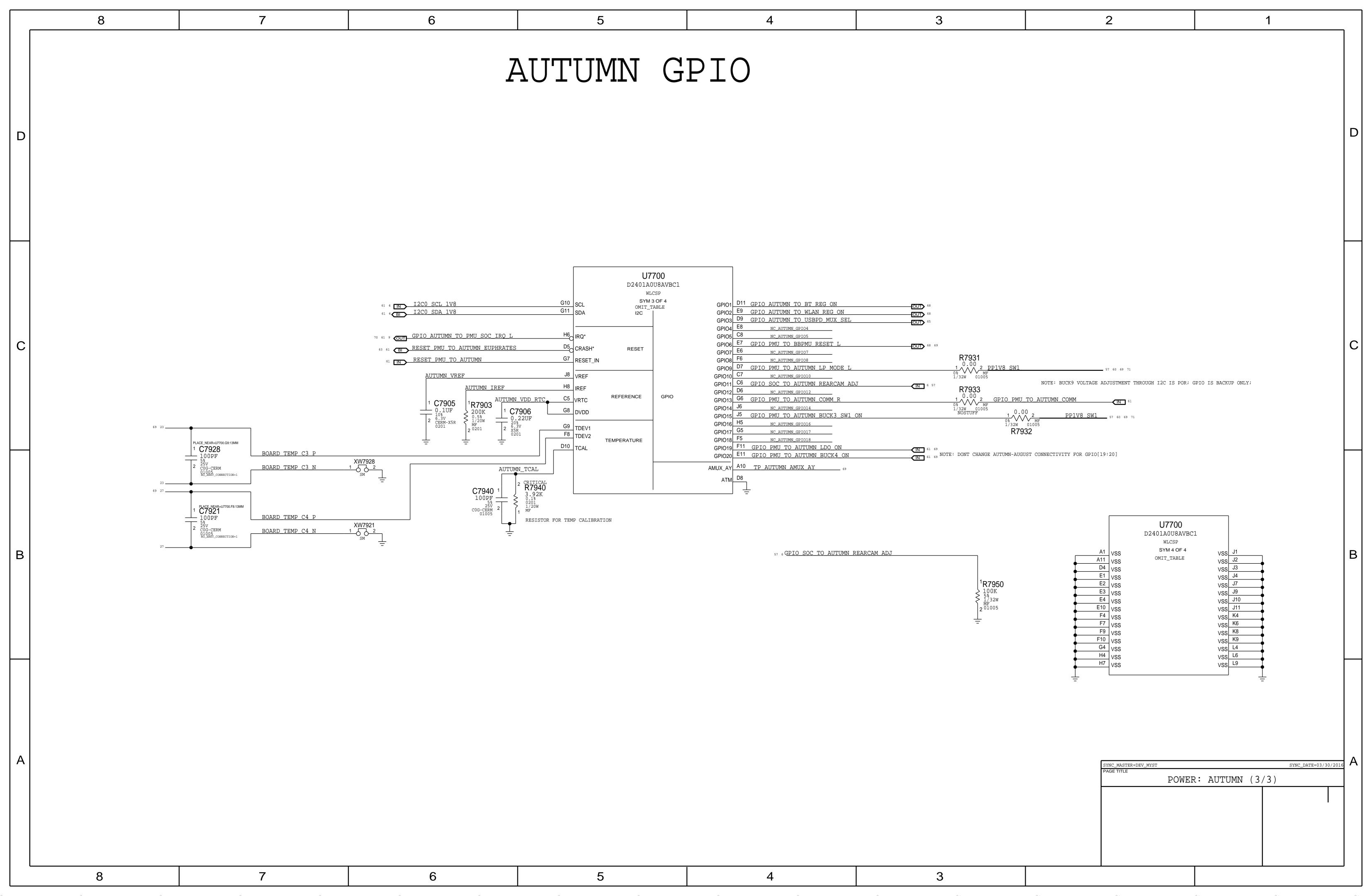


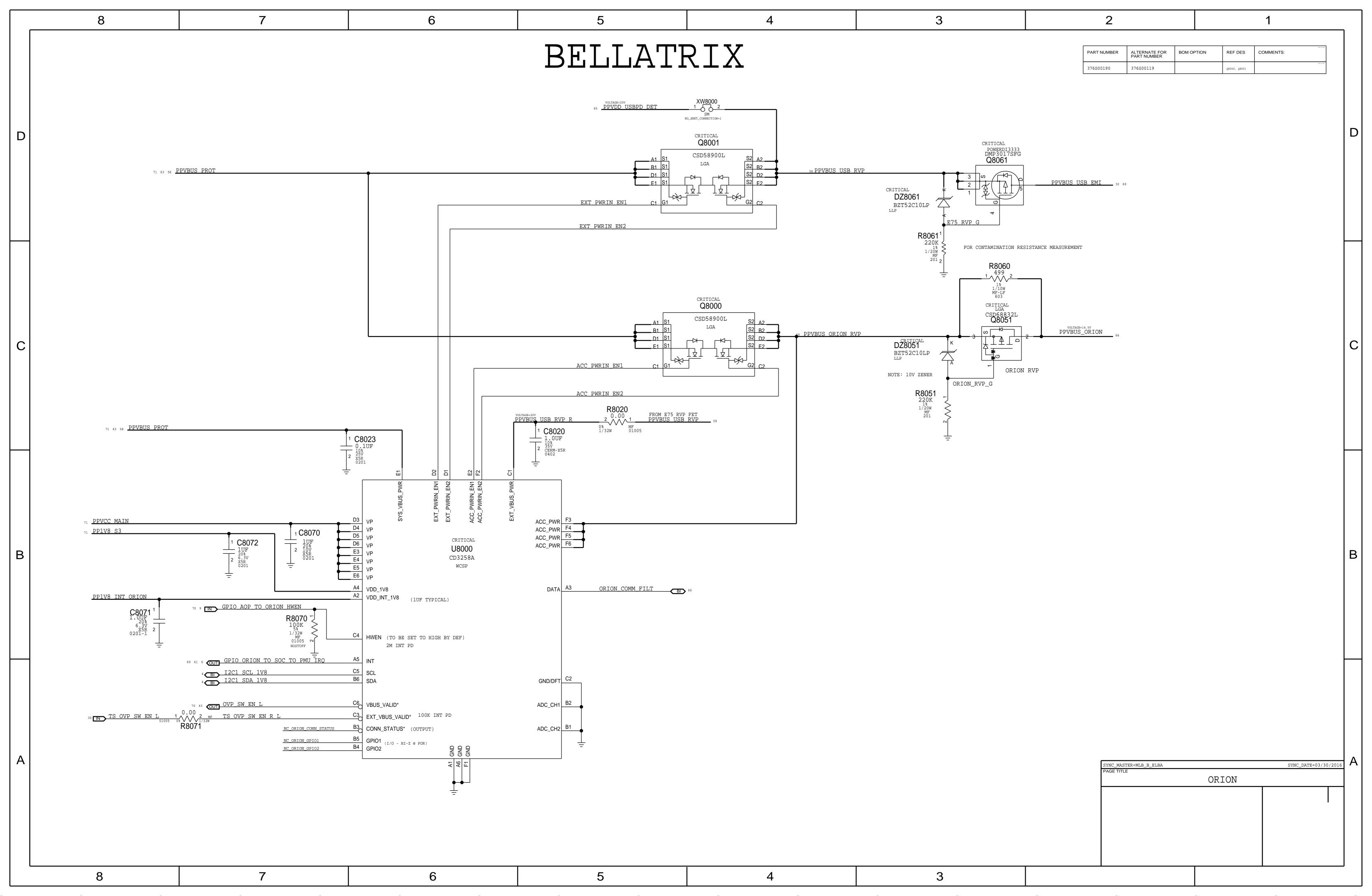


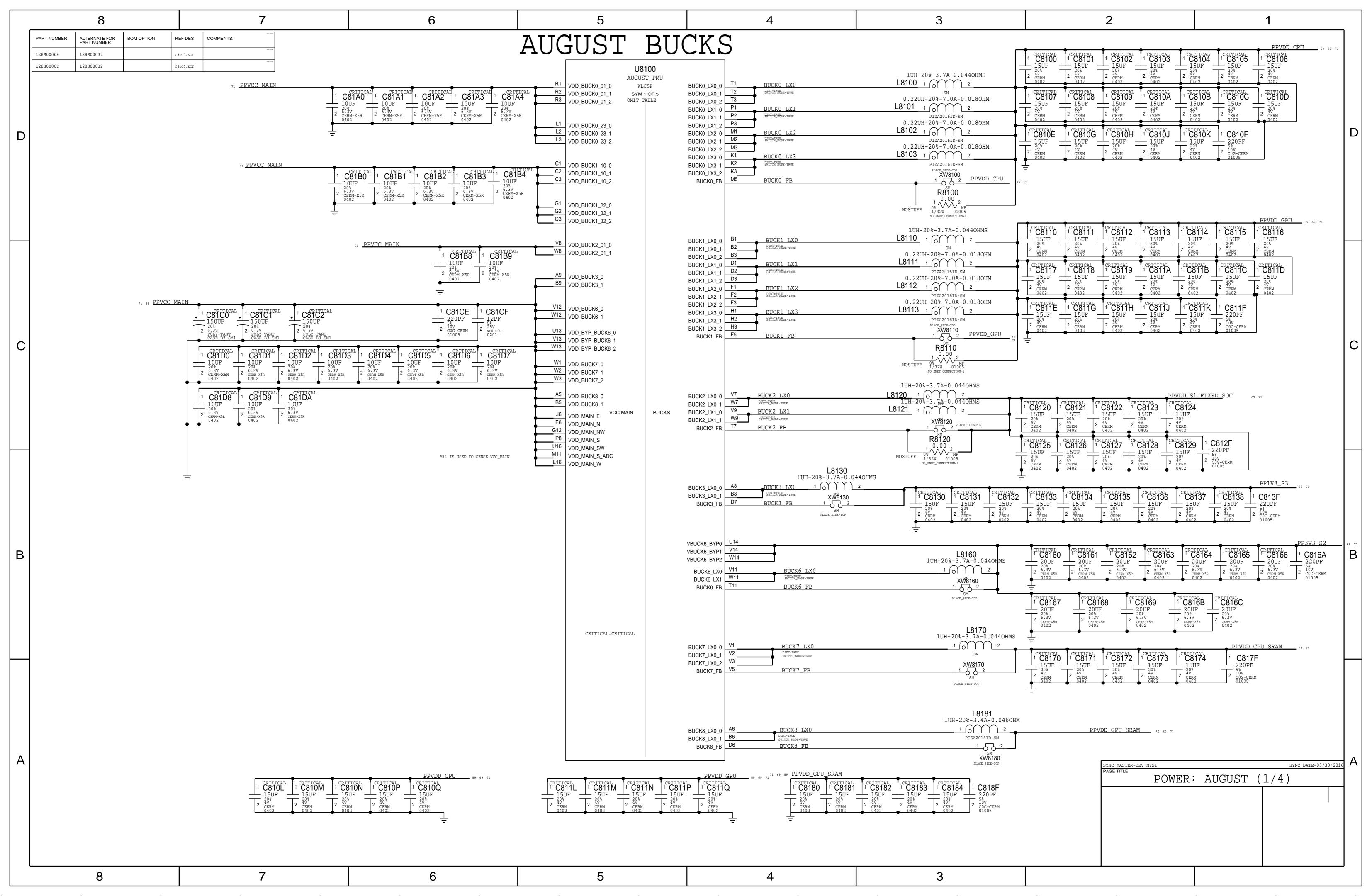


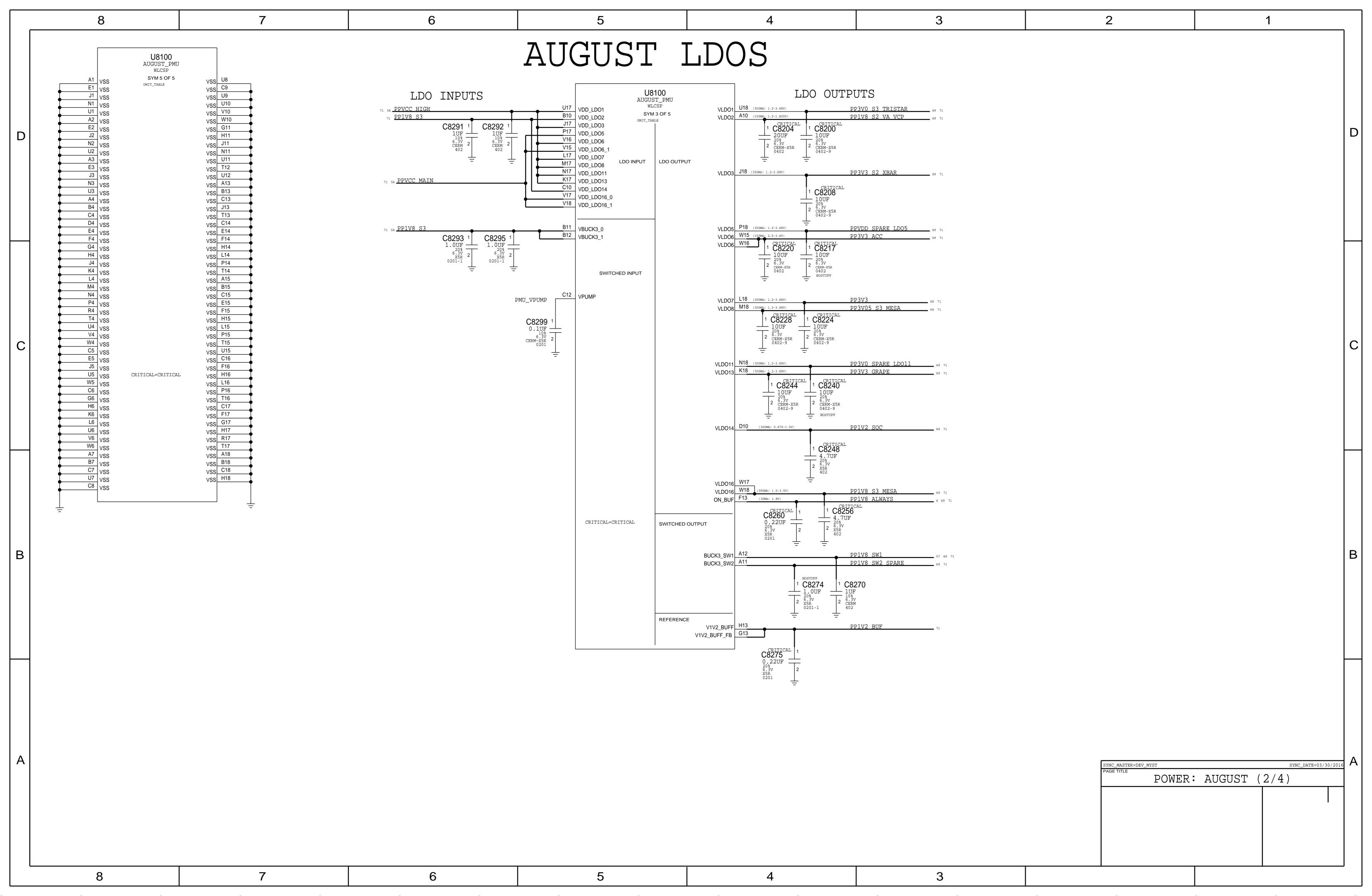


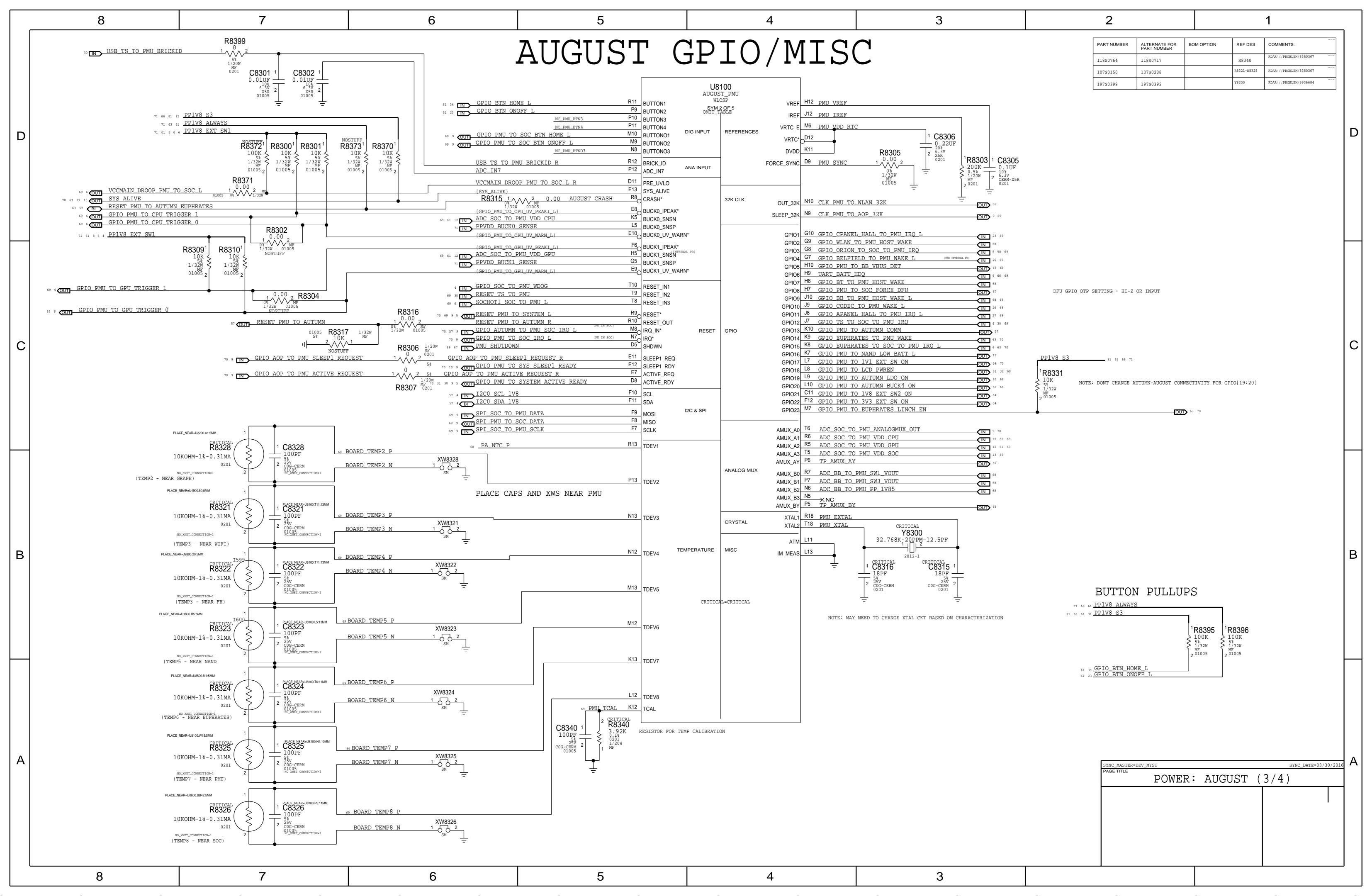


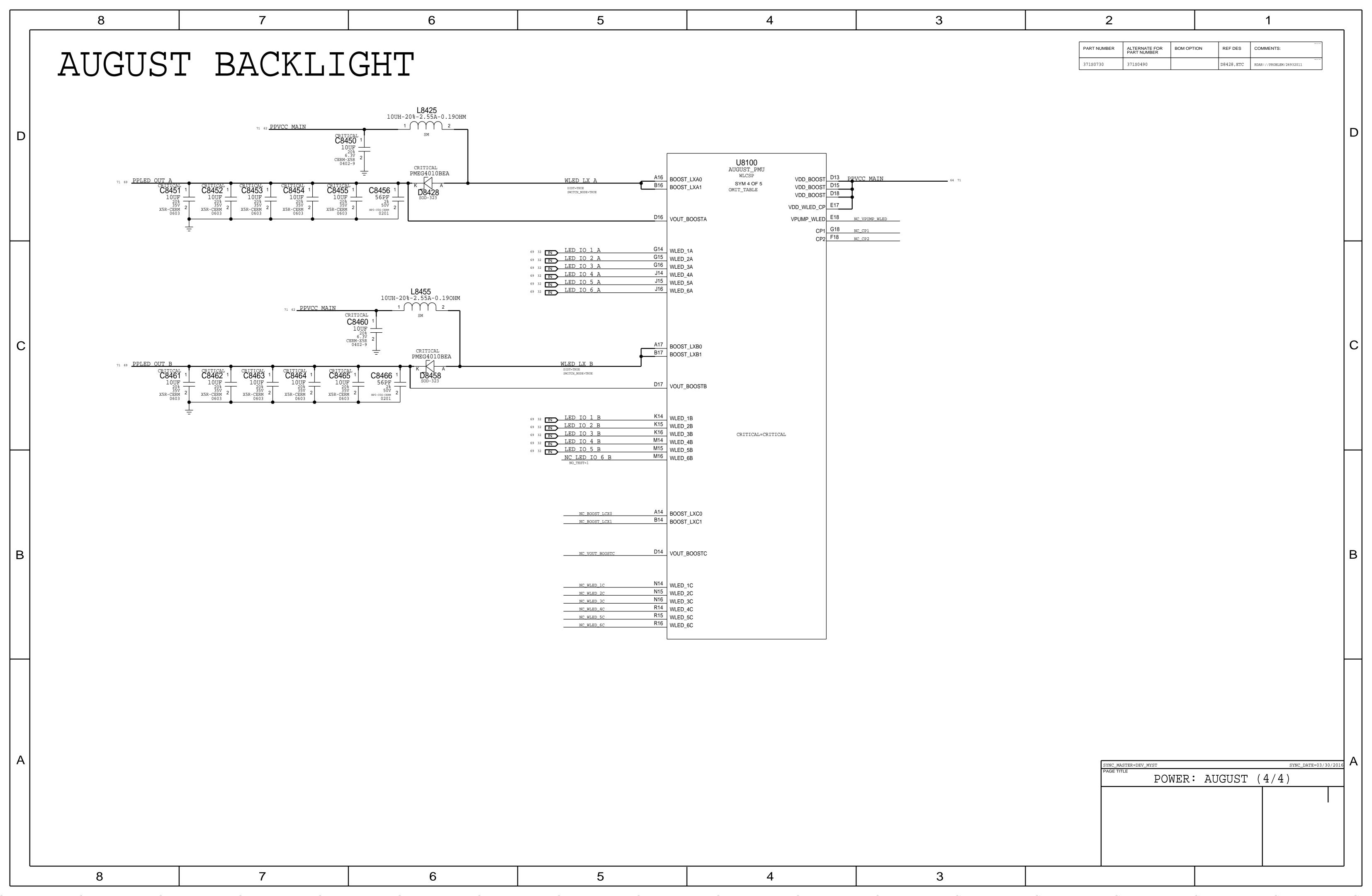


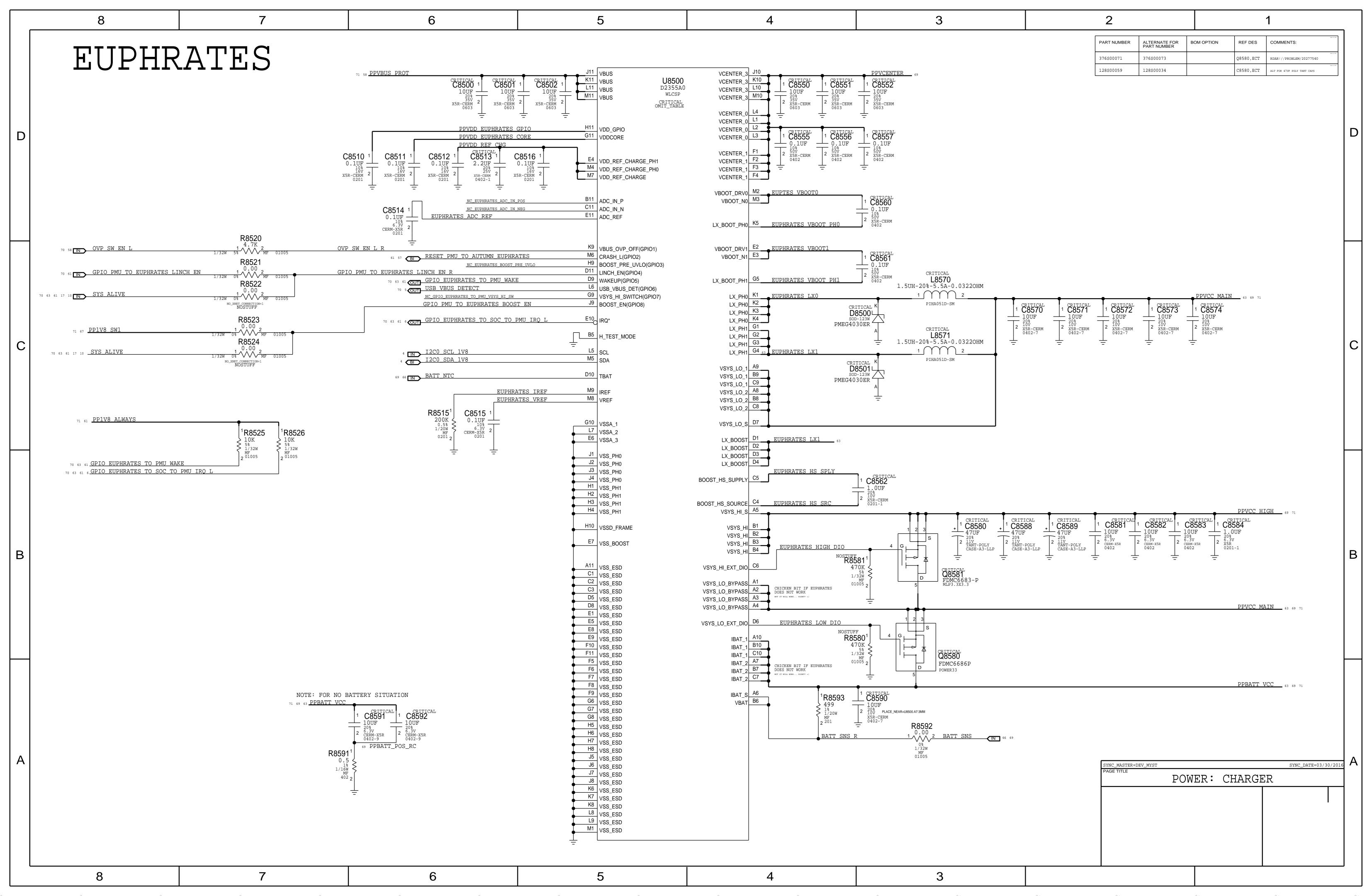


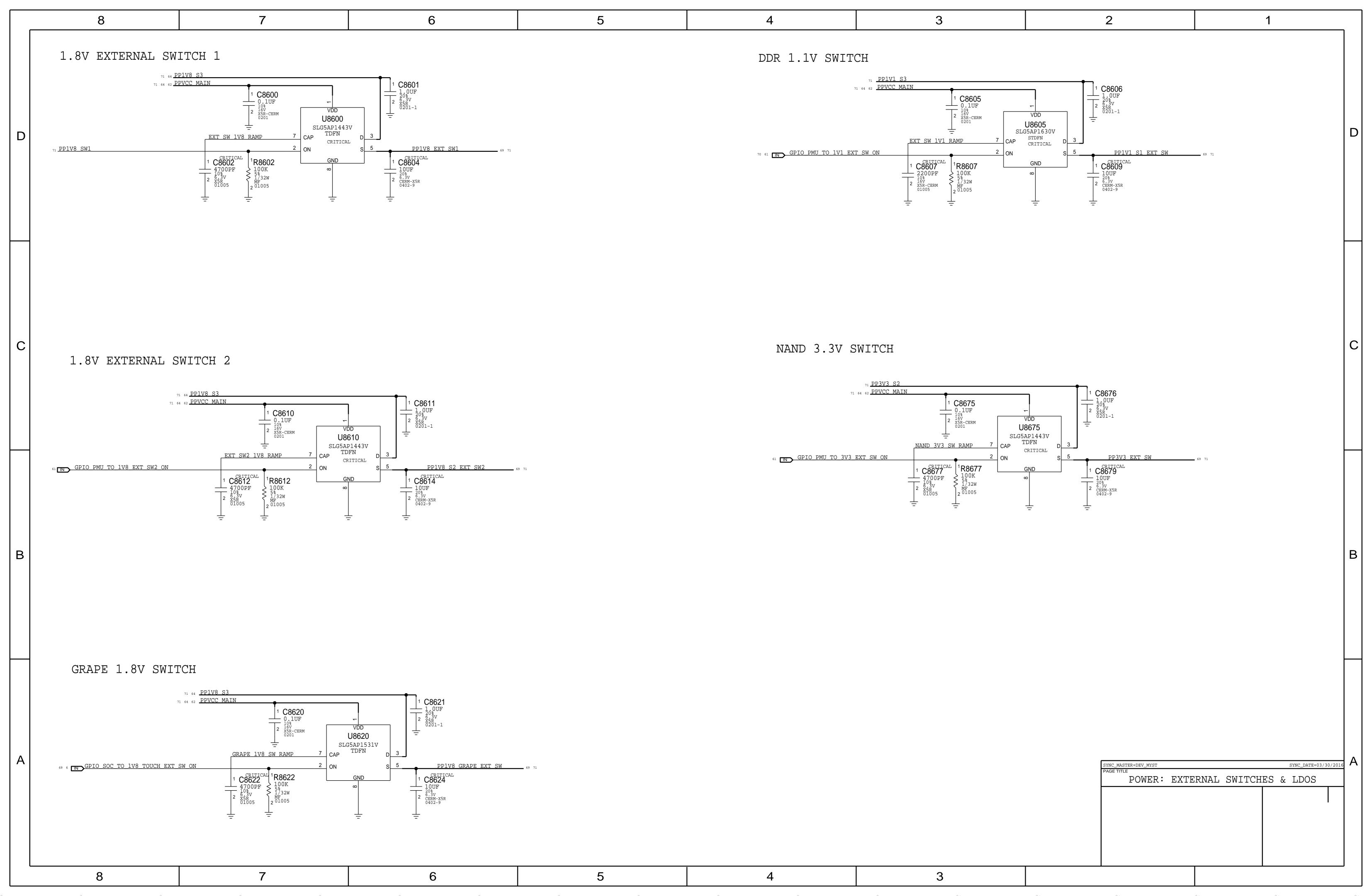


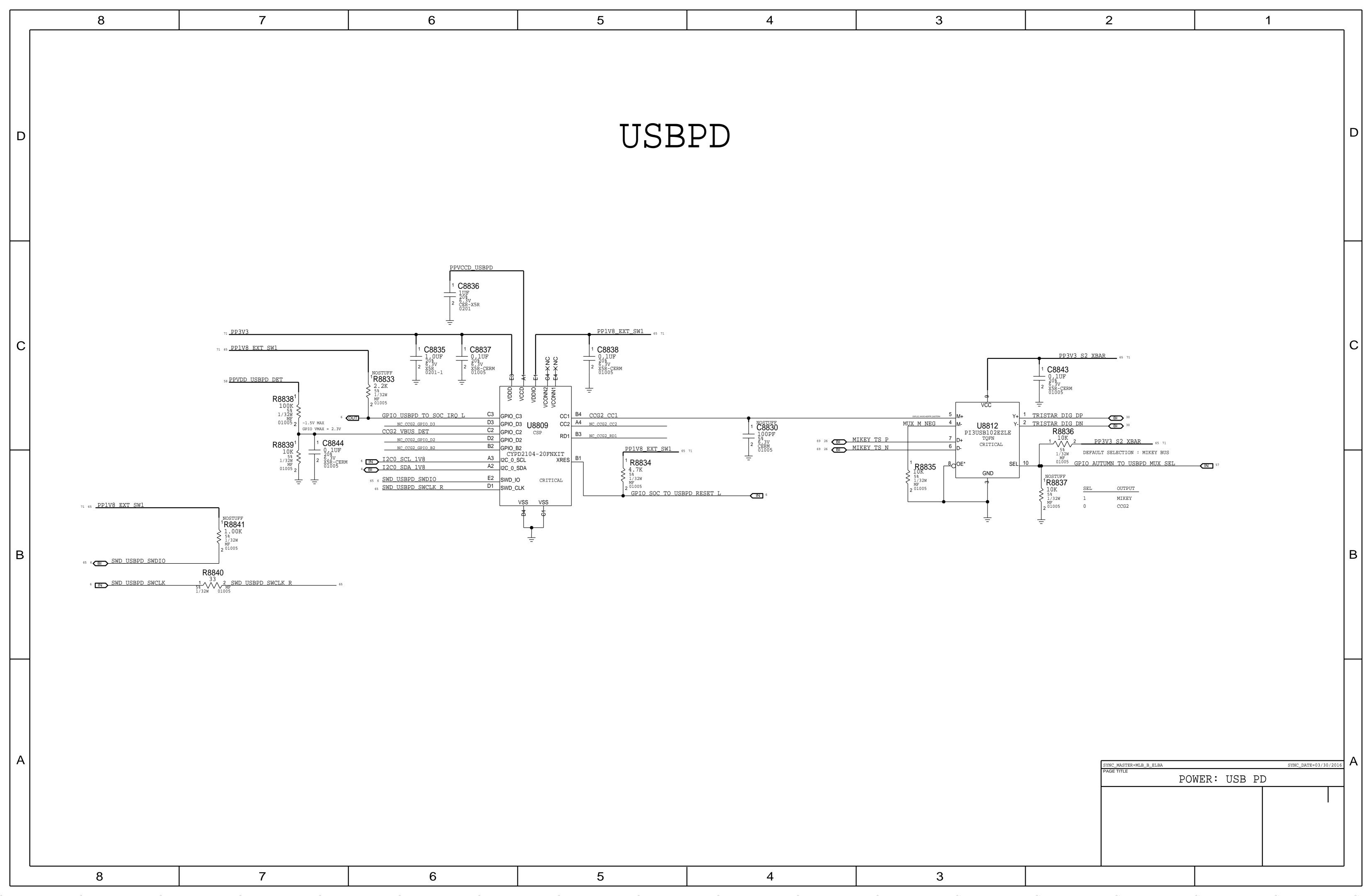


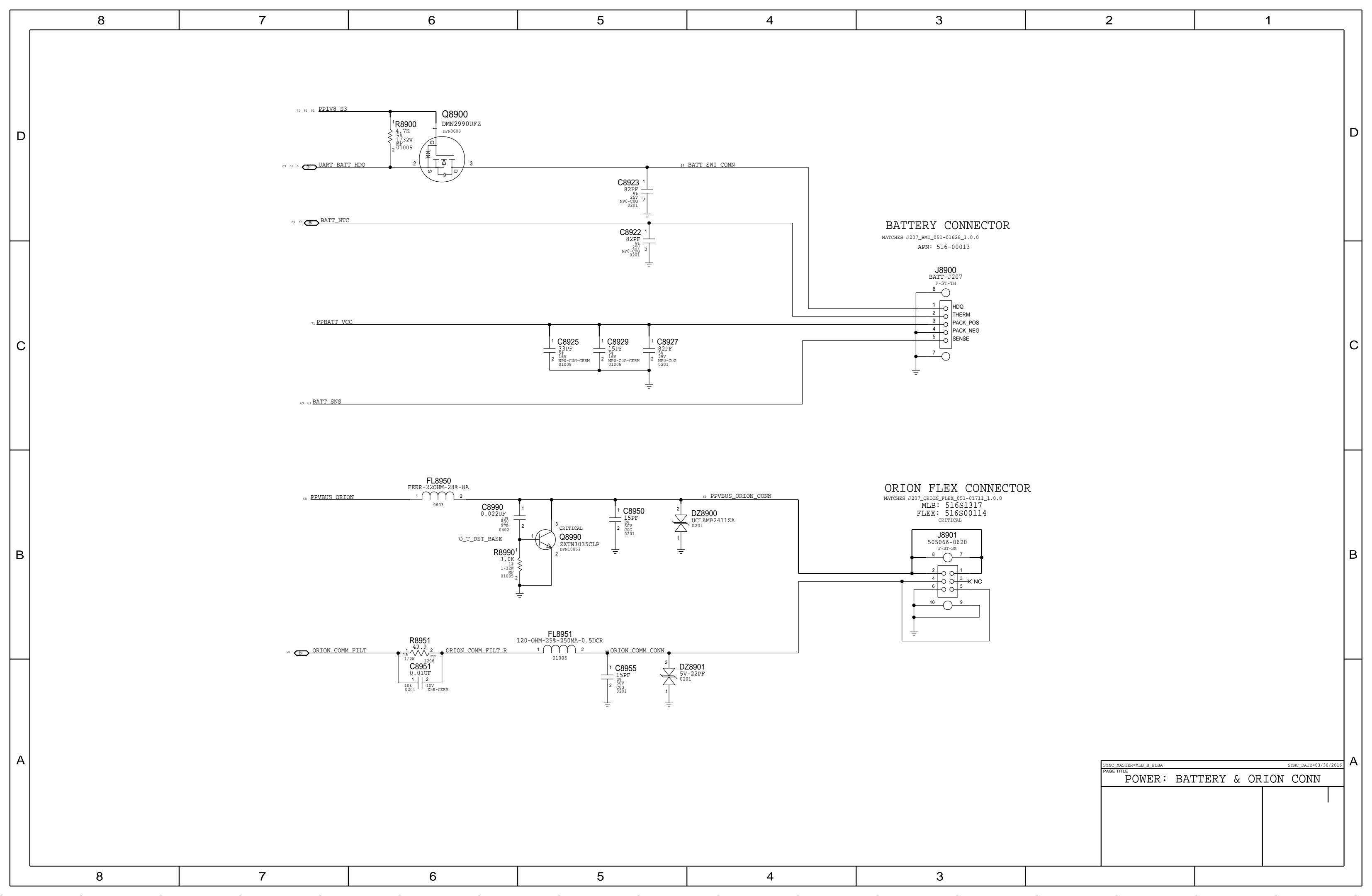


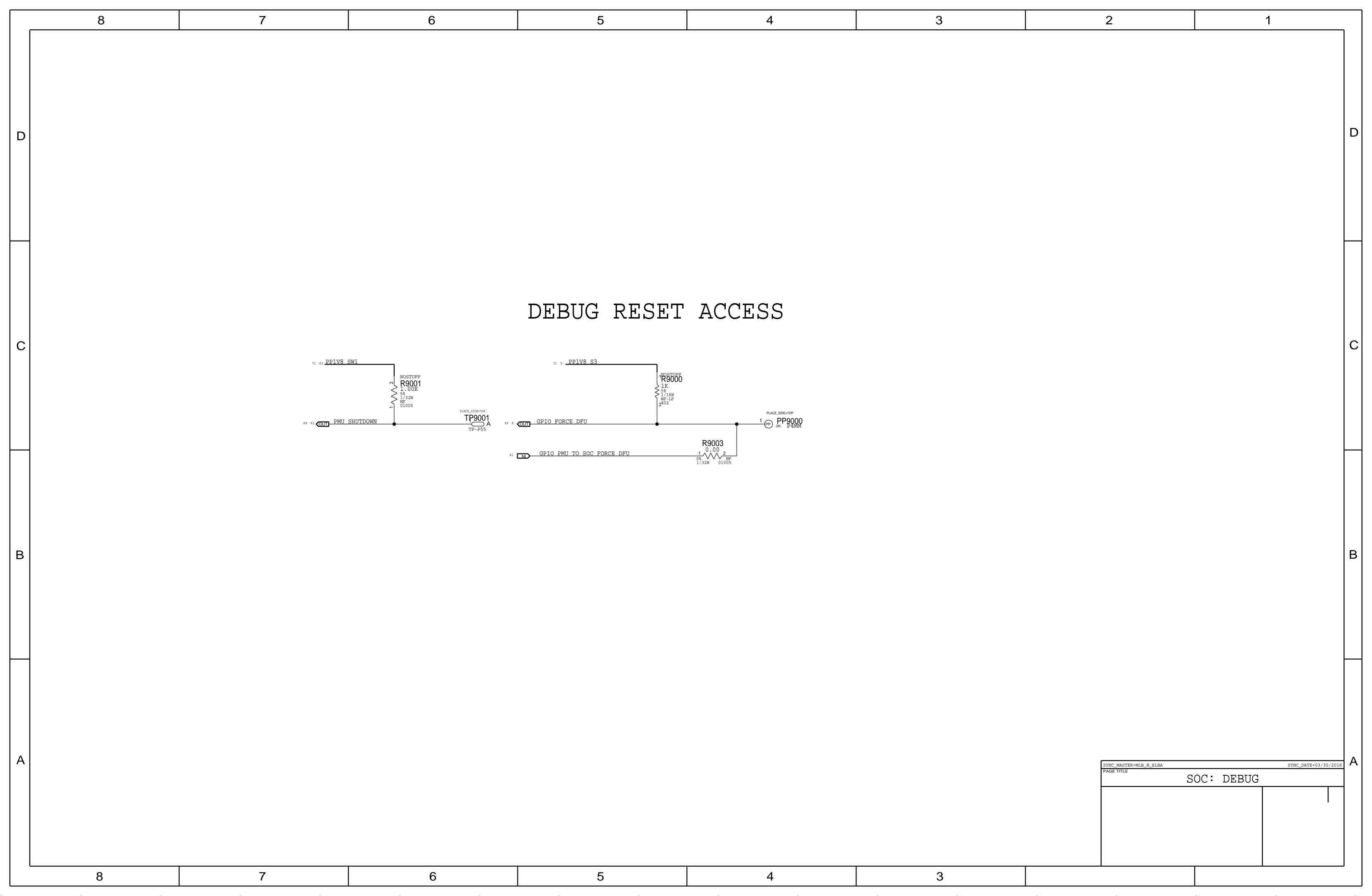


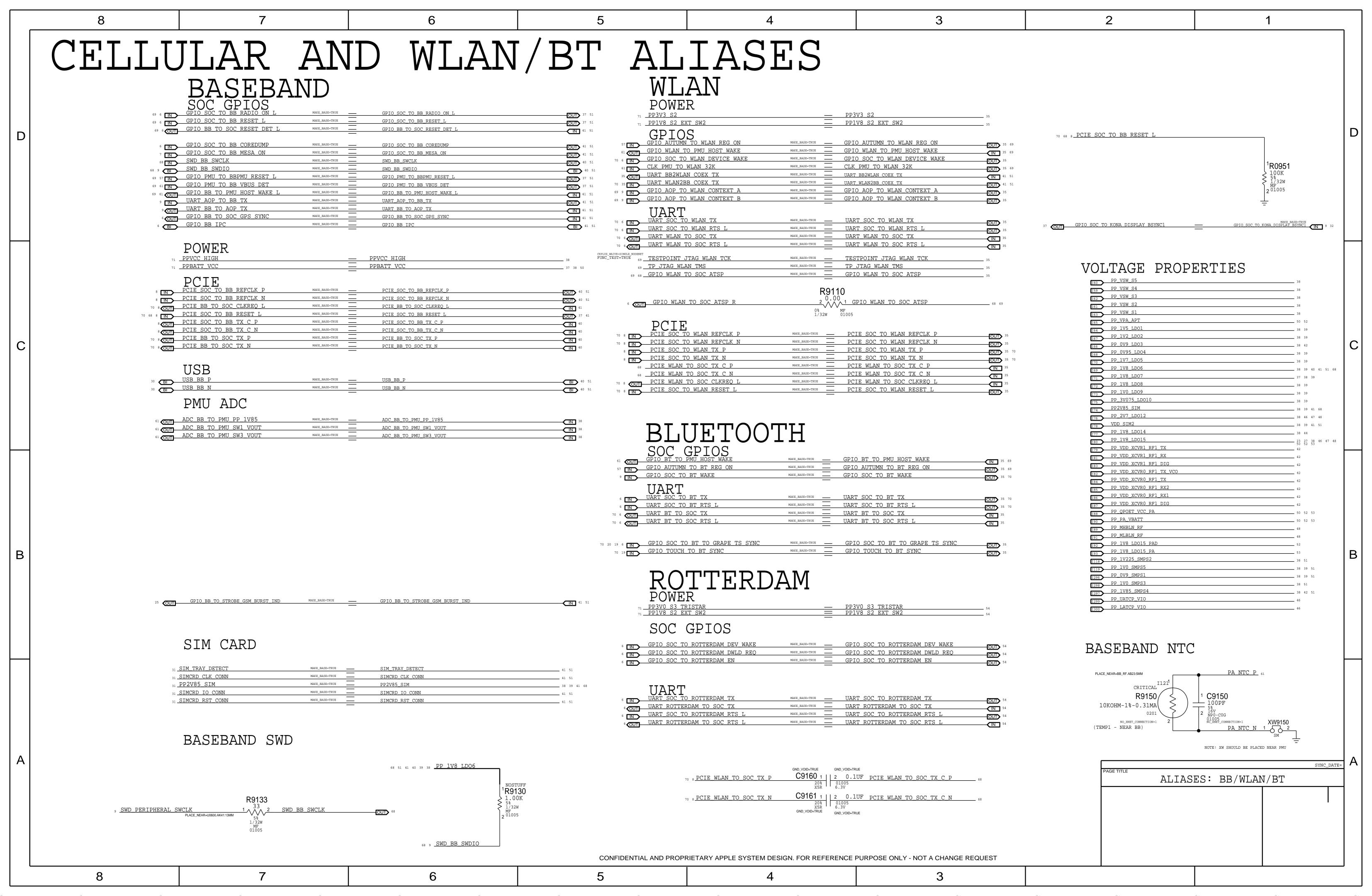


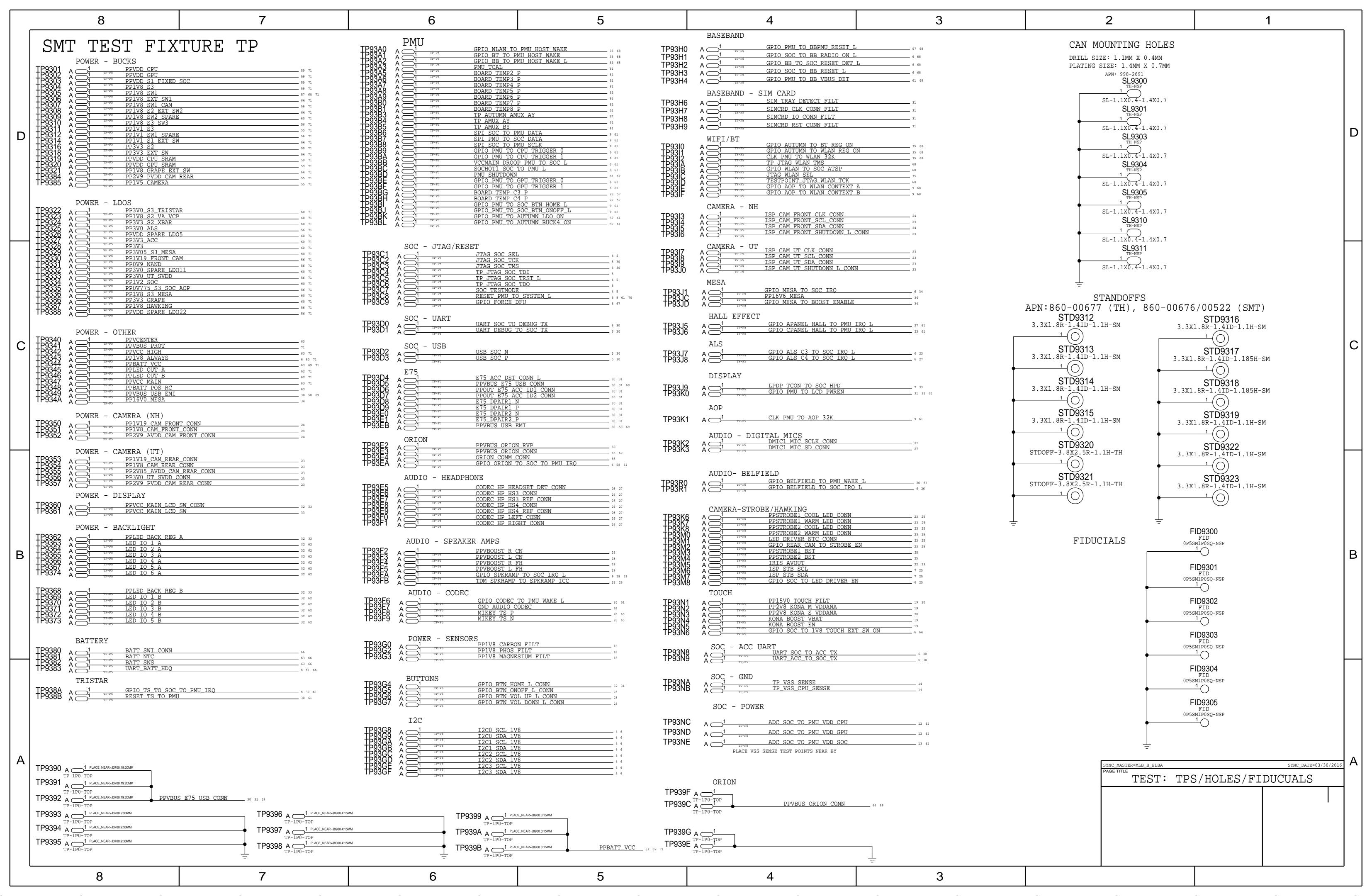


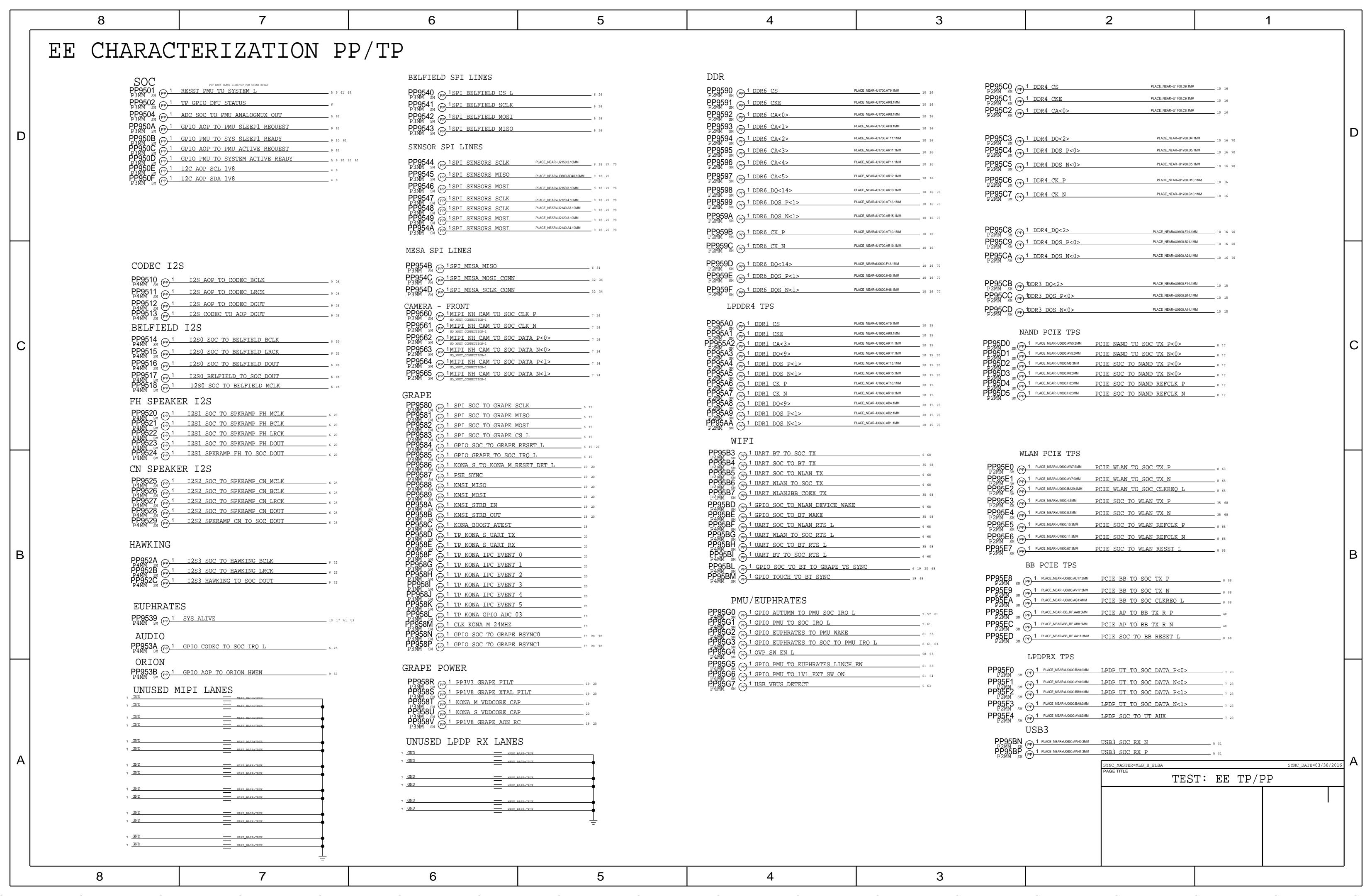












	8 7	6 5	4 3	2 1
POWER CONNECTIONS				
D	AUGUST_BUCKO (ACTIVE) PPVDD CPU MAKE_BASE=TRUE XWC190 2 PPVDD BUCKO SENSE SHORT-10L-0.1MM-SM AUGUST_BUCK1 (SW CONTROL) PPVDD GPU	AUTUMN_BUCK4 (SLEEP3) — PP1V1 S3 64 — PP1V1 S3 56	AUGUST_LD07 (ACTIVE) PP3V3 PP3V3 PP3V3 PP3V3 65 AUGUST_LD08 (SLEEP3)	CHARGER MAIN PPVCC MAIN — PPVCC MAIN
	AUGUST BUCK 2 (SLEEP 1) PPVDD S1 FIXED SOC PPVDD S1 FIXED SOC MAKE_BASE=TRUE XWC191 1	AUTUMN_BUCK4_SW1 (SPARE) 69 56 PP1V1 SW1 SPARE MAKE_BASE=TRUE T13 BUCK4 EXT SW (SLEEP1)	AUGUST_LDO8 (SLEEP3) = PP3V05 S3 MESA — PP3V05 S3 MESA — PP3V05 S3 MESA AUTUMN_LDO9 (ACTIVE) 69 56 PP1V19 FRONT CAM — PP1V19 FRONT CAM 24	PPVCC MAIN 33 PPVCC MAIN 62 PPVCC MAIN 34 PPVCC MAIN 58 PPVCC MAIN 25 PPVCC MAIN 62 PPVCC MAIN 62 PPVCC MAIN 19
	— PPVDD S1 FIXED SOC	BUCK4_EXT_SW (SLEEP1) 13	AUTUMN_LDO10 (ACTIVE) 69 56 PP0V9 NAND PP0V9 NAND AUGUST_LDO11 (SLEEP2) 69 60 PP3V0 SPARE LDO11 MAKE_BASE=TRUE T136	CHARGER HIGH 69 63 PPVCC HIGH MAKE_BASE=TRUE — PPVCC HIGH 56 60
C	## PPVDD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC ## PPVD S1 FIXED SOC	AUGUST_BUCK6 (SLEEP2)	AUGUST_LD013 (SW CONTROL) 69 60 PP3V3 GRAPE — PP3V3 GRAPE — PP3V3 GRAPE — 19 AUGUST_LD014 (ACTIVE)	### PPVCC HIGH 68 PPVCC HIGH 34 ### BATTERY Figure
	BUCK3_SW AUGUST_BUCK3_SW1 PP1V8 S3 AUGUST_BUCK3_SW1 (ACTIVE)		AUGUST_LDO14 (ACTIVE) — PP1V2 SOC 11	USB POWER INPUT 69 PPVBUS PROT — PPVBUS PROT — 58 63
	69 60 57 PP1V8 SW1 — PP1V8 SW1	AUGUST_BUCK7 (ACTIVE) 69 59 PPVDD CPU SRAM PPVDD CPU SRAM MAKE_BASE=TRUE	AUTUMN_LDO15 (SLEEP2) 69 56 PPOV775_S3_SOC_AOP PPOV775_S3_SOC_AOP 11	ON_BUF 69 60 6 PP1V8 ALWAYS — PP1V8 ALWAYS — 61 63 — — PP1V8 ALWAYS — PP1V8 ALWA
	AUGUST BUCK3_SW2 (SPARE) 69 60 PP1V8 SW2 SPARE T136	AUGUST_BUCK8 (SW CONTROL) PPVDD GPU SRAM — PPVDD GPU SRAM — PPVDD GPU SRAM 13	AUGUST_LD016 (SLEEP3) PP1V8_S3_MESA	BACKLIGHT BOOST 69 62 PPLED_OUT_A PPLED_OUT_A 33
	AUTUMN_BUCK3_SW1 (ACTIVE)	— 7 24 — 7 23 AUTUMN_BUCK9 (SW CONTROL) PP2V9 PVDD CAM REAR — PP2V9 PVDD CAM REAR 23 MAKE_BASE=TRUE	AUTUMN_LDO17 (SW CONTROL) 56 PP2V85 REAR CAM — PP2V85 REAR CAM — PP2V85 REAR CAM 23	69 62 PPLED OUT B — PPLED OUT B — 33 MAKE_BASE=TRUE — PPLED OUT B 33
В	AUTUMN BUCK3_SW3 (SLEEP2) — PP1V8_S3_SW3 — PP1V8_S3_SW3 — PP1V8_S3_SW3 — PP1V8_S3_SW3 — PP1V8_S3_SW3		AUTUMN_LDO18 (SW CONTROL) PP1V19 REAR CAM PP1V19 REAR CAM AUTUMN_LDO19 (SW CONTROL)	B
	BUCK3_EXT_SW1 (ACTIVE) PP1V8 EXT SW1 — PP1V8 EXT SW1		PP3V0 UT SVDD — PP3V0 UT SVDD	
	PP1V8 EXT SW1 PP1V8 EXT SW1 PP1V8 EXT SW1	AUGUST_LDO3 (SLEEP 2) 65 69 60 PP3V3 S2 XBAR — PP3V3 S2 XBAR	AUTUMN_LDO21 (SW CONTROL) PP2V85 FRONT CAM — PP2V85 FRONT CAM 24 ALITHIMAT T DO22 (CDADE)	
A	BUCK3_S2_EXT_SW2 (SLEEP2) PP1V8_S2_EXT_SW2 — PP1V8_S2_EXT_SW2 — PP1V8_S2_EXT_SW2 — PP1V8_S2_EXT_SW2 — PP1V8_S2_EXT_SW2 — PP1V8_S2_EXT_SW2 — PP1V8_S2_EXT_SW2		AUTUMN_LDO22 (SPARE) PPVDD_SPARE_LDO22 MAKE_BASE=TRUE AUTUMN_ON_BUF MAKE_BASE=TRUE AUGUST_V1V2_BUF	SYNC_MASTER= PAGE TITLE POWER: ALIASES
		AUGUST_LDO5 (SPARE) 69 60 PPVDD SPARE LDO5 MAKE_BASE=TRUE	AUGUST_V1V2_BUF O PP1V2 BUF MAKE_BASE=TRUE	
	EXTERNAL SWITCH (SW CONTROL) 69 64 PP1V8 GRAPE EXT SW PP1V8 GRAPE EXT SW MAKE_BASE=TRUE PP1V8 GRAPE EXT SW	AUGUST_LD06 (SW CONTROL) PP3V3 ACC PP3V3 ACC MAKE_BASE=TRUE		
	8 7	6 5	4 3	