

PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI


Tall DVI-I + DP + DP + DP/HDMI + DP

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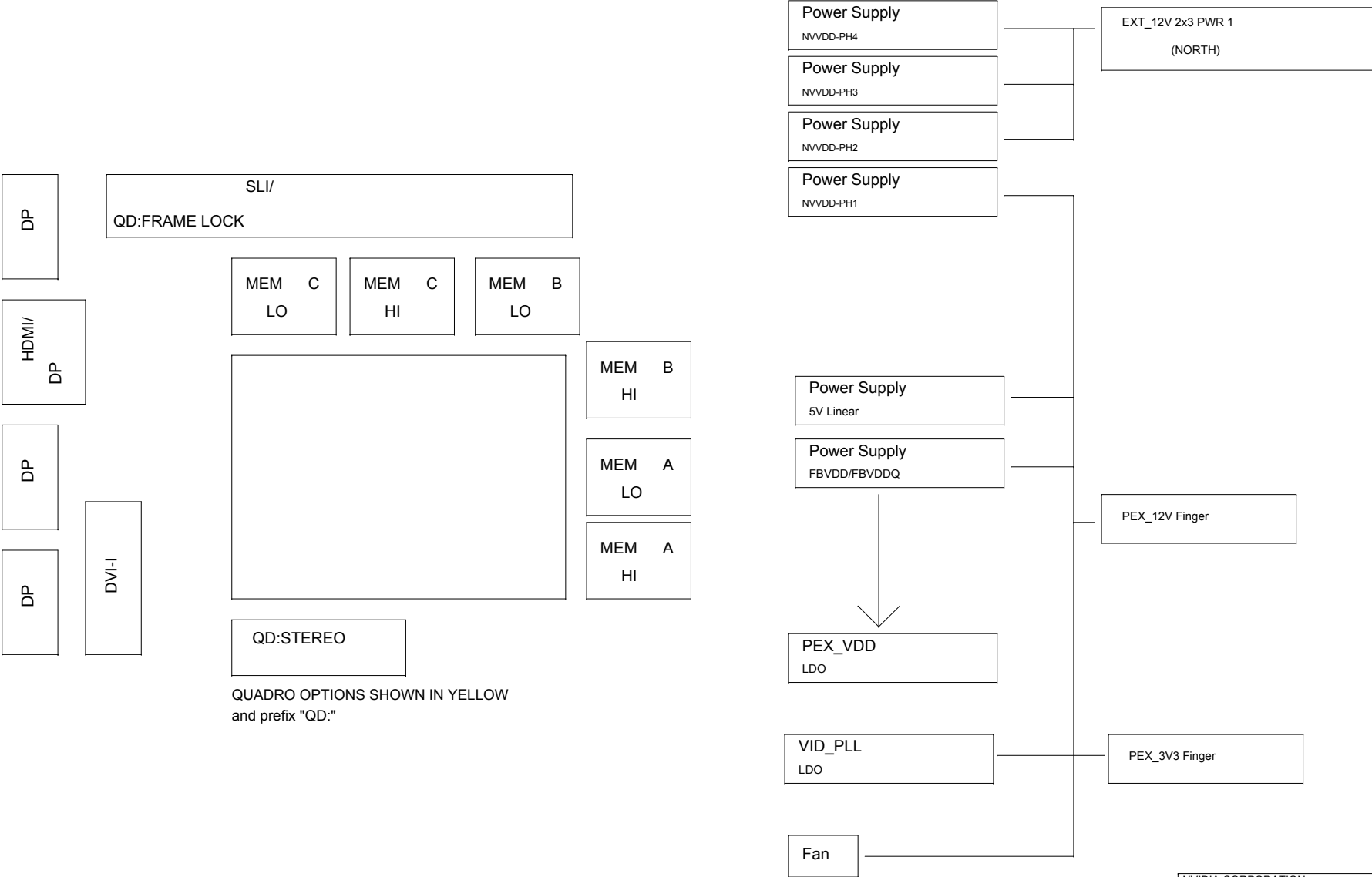
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Block Diagram

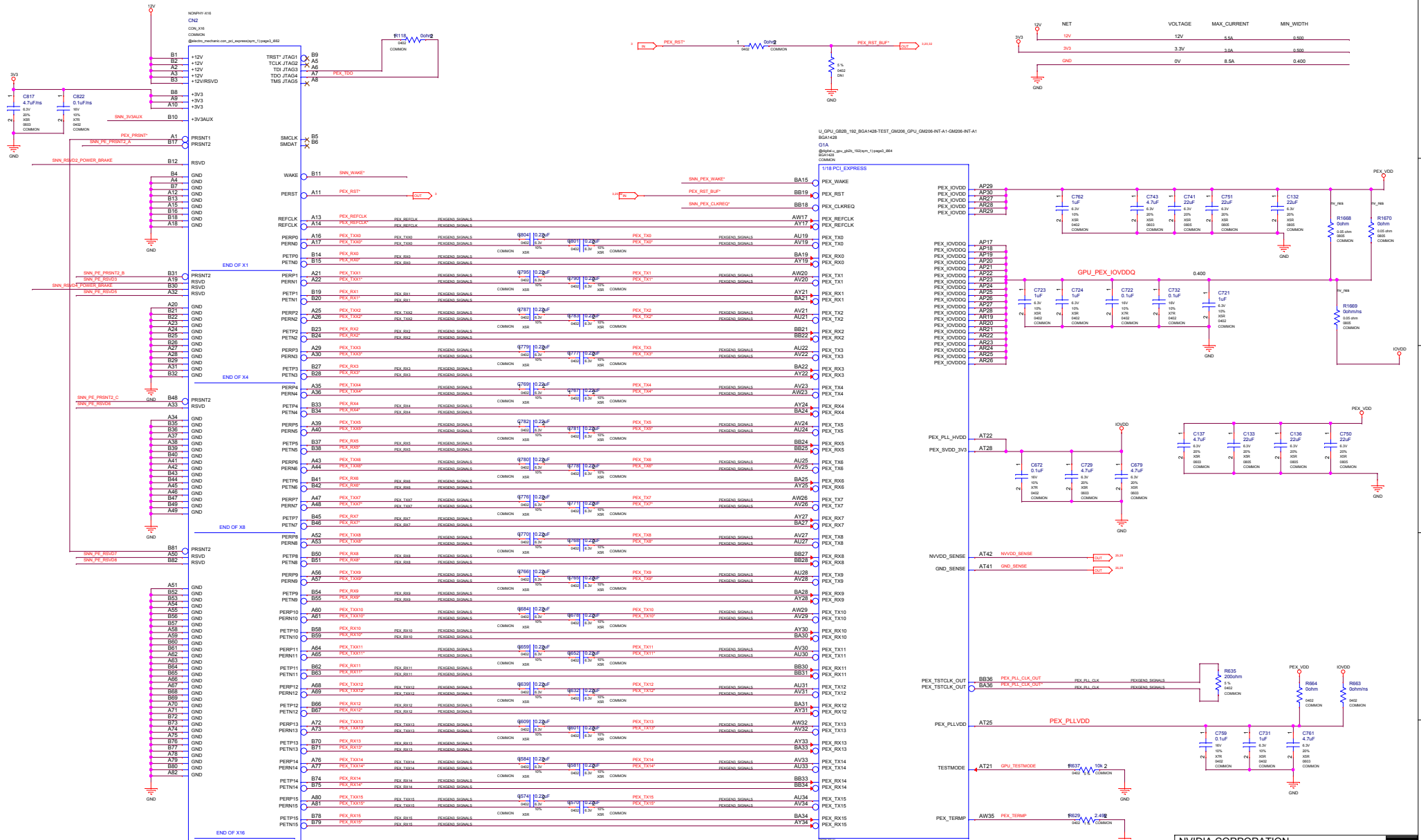


QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

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PCI Express

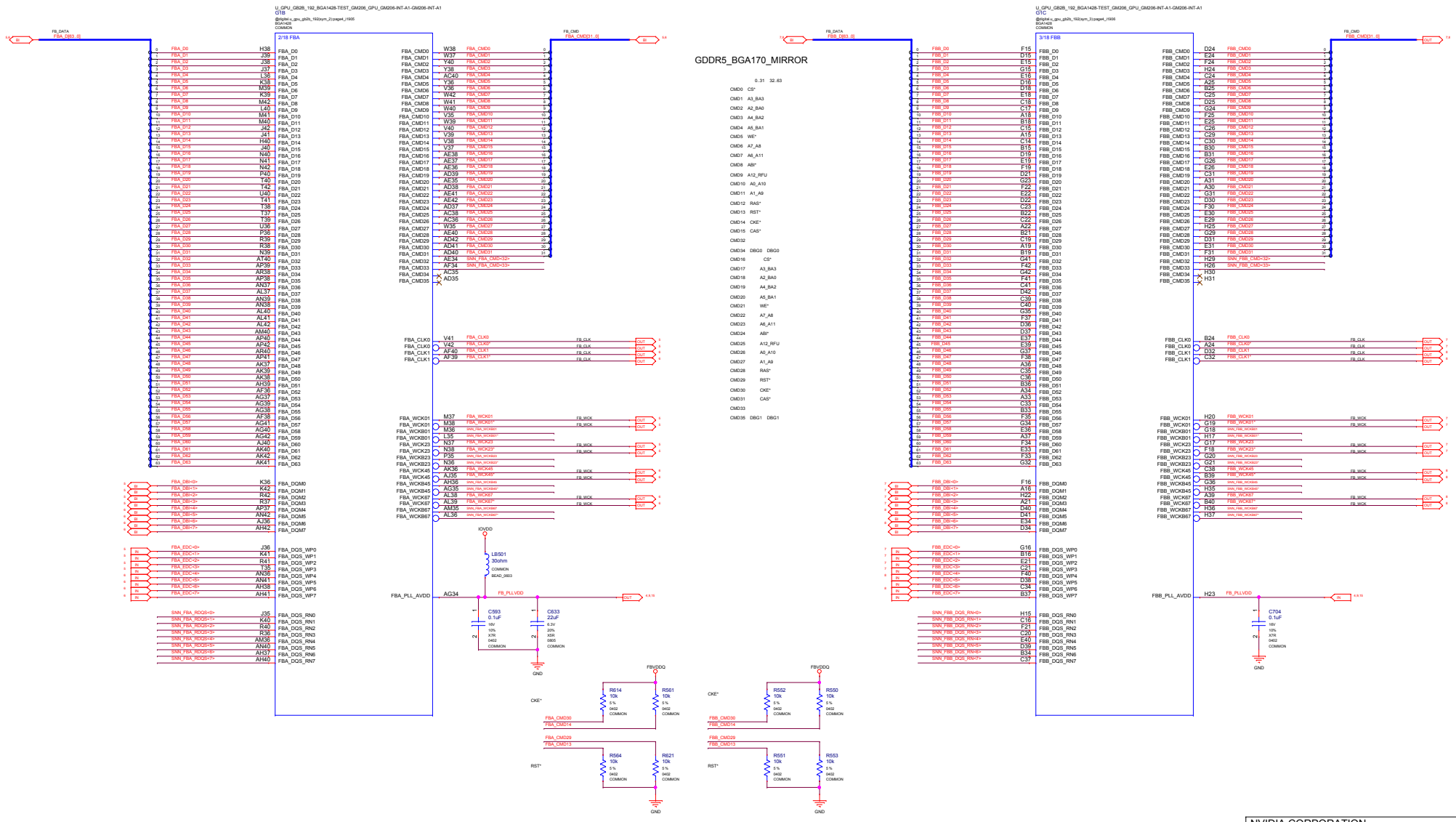


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MEMORY: GPU Partition A/B



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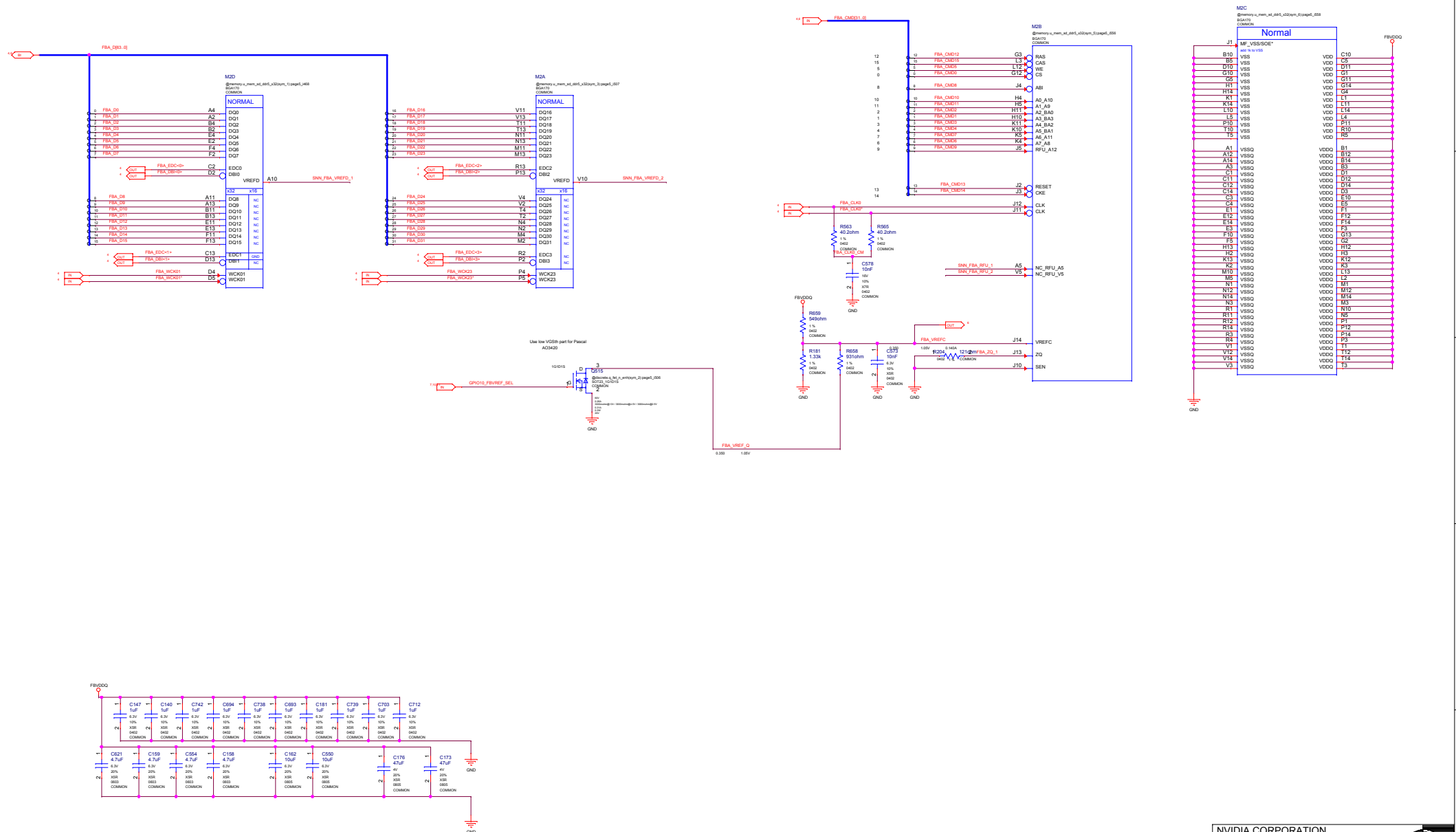
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A	B	C	D	E	F	G	H
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MEMORY: FBA Partition 31..0



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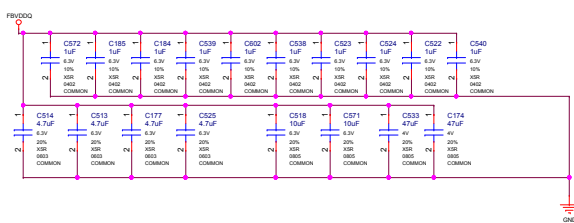
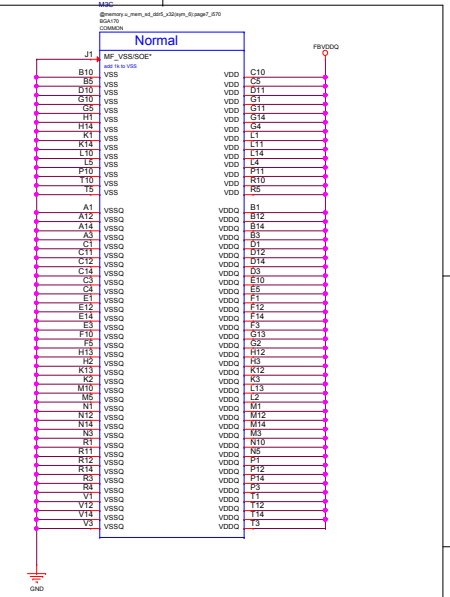
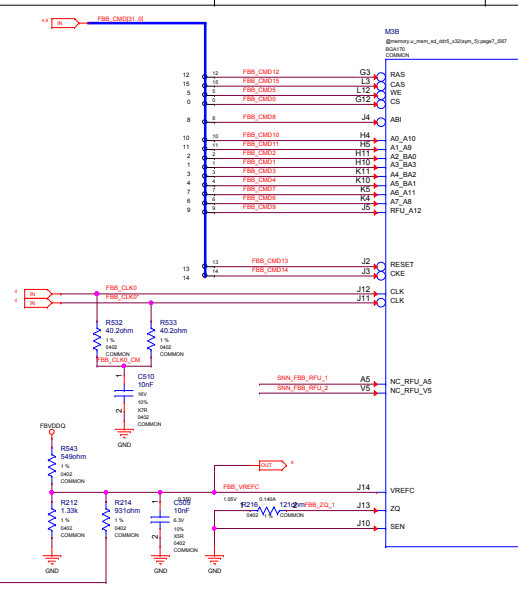
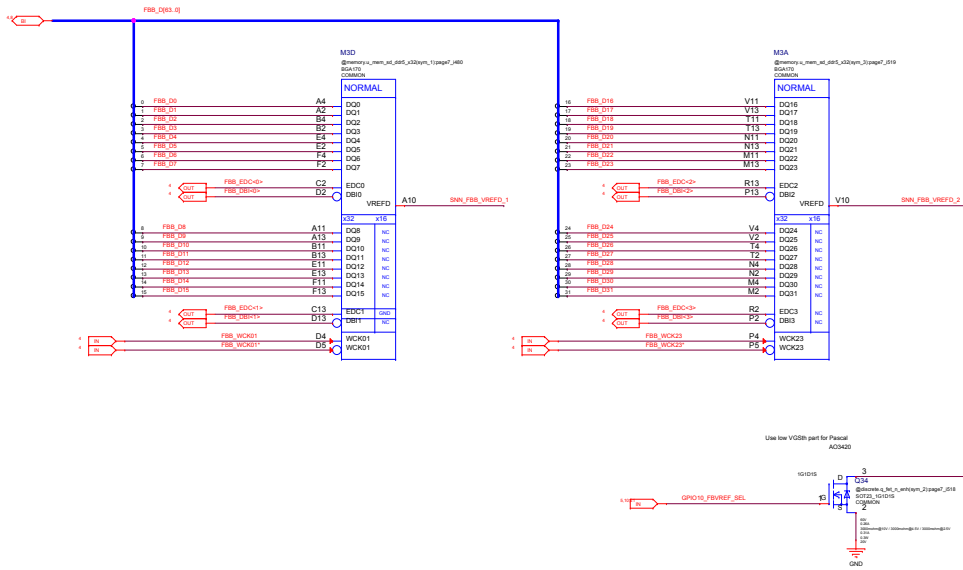
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MEMORY: FBB Partition 31..0



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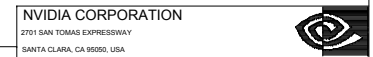
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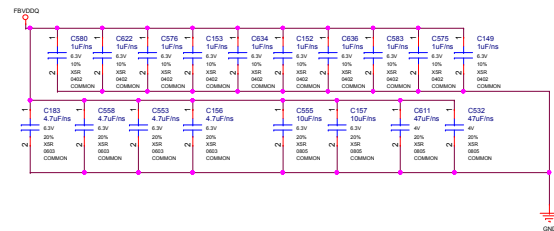
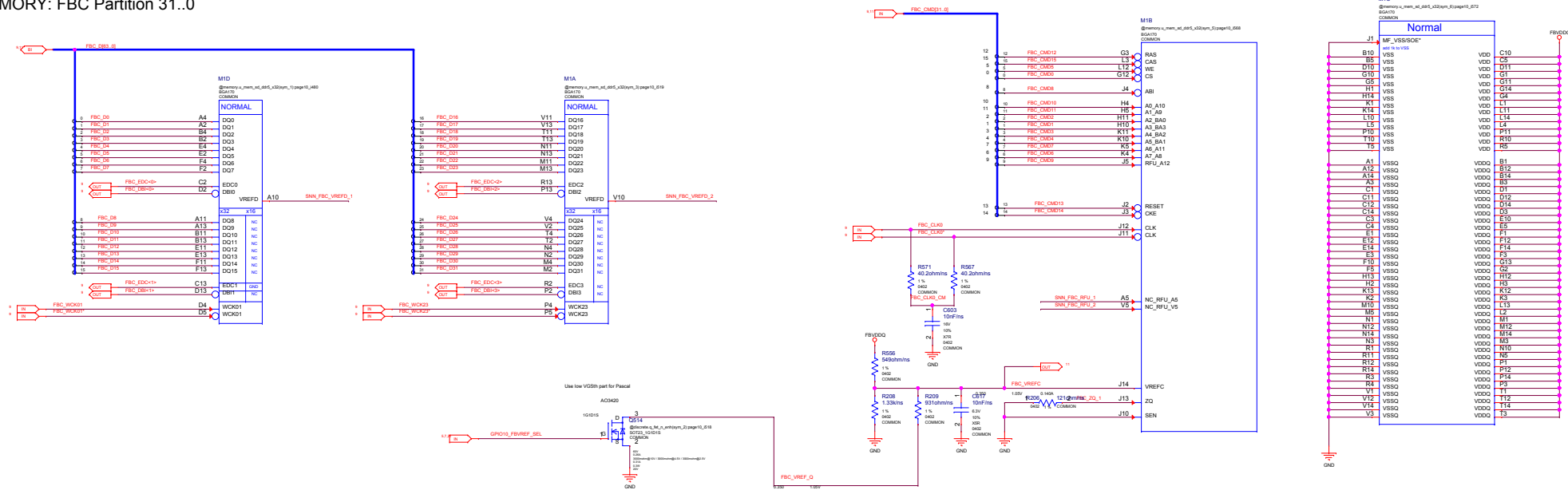
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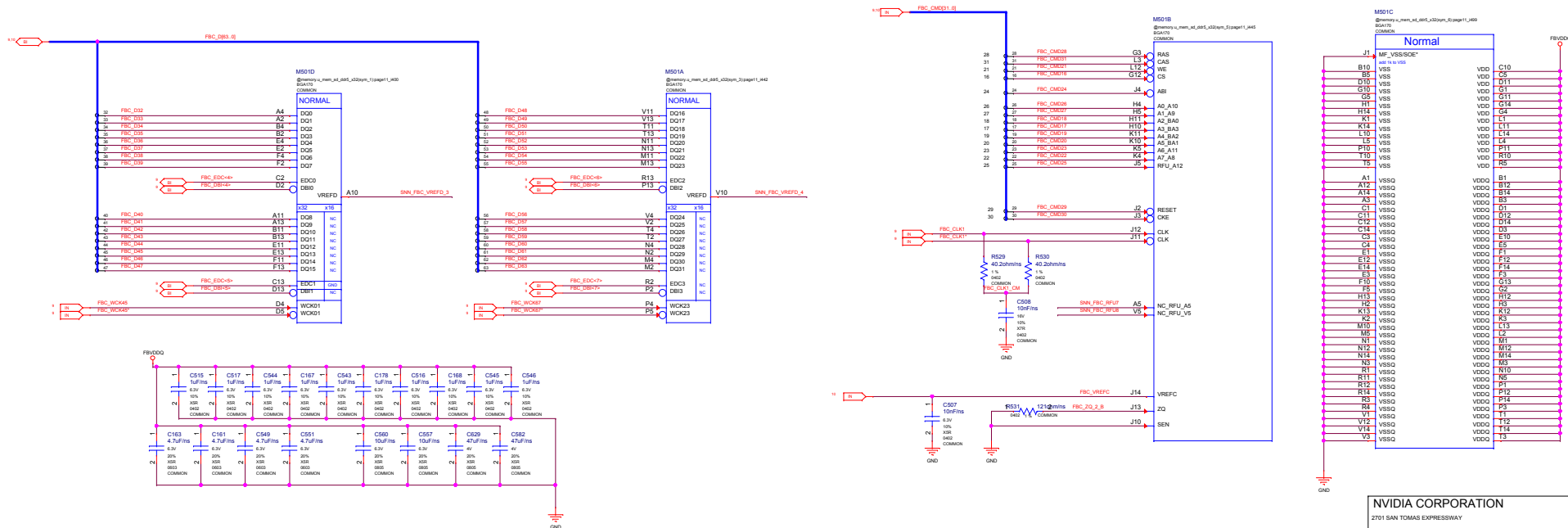
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GPU PWR and GND

U: GPU_GB2B_192_BGA1428-TEST_QM206_GPU_QM206-INT-A1-QM206-INT-A1

G11

BGA1428

COMMON



U: GPU_GB2B_192_BGA1428-TEST_QM206_GPU_QM206-INT-A1-QM206-INT-A1

G11

BGA1428

COMMON



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G11

BGA1428

COMMON

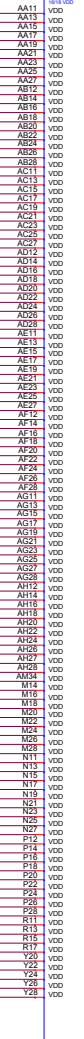


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BGA1428

COMMON

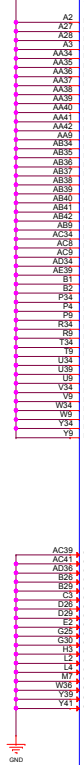


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G11

BGA1428

COMMON



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G11

BGA1428

COMMON

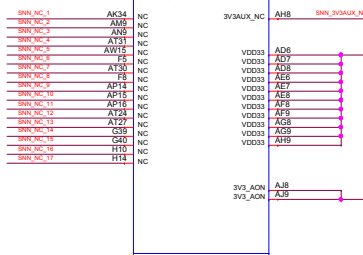


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G11

BGA1428

COMMON



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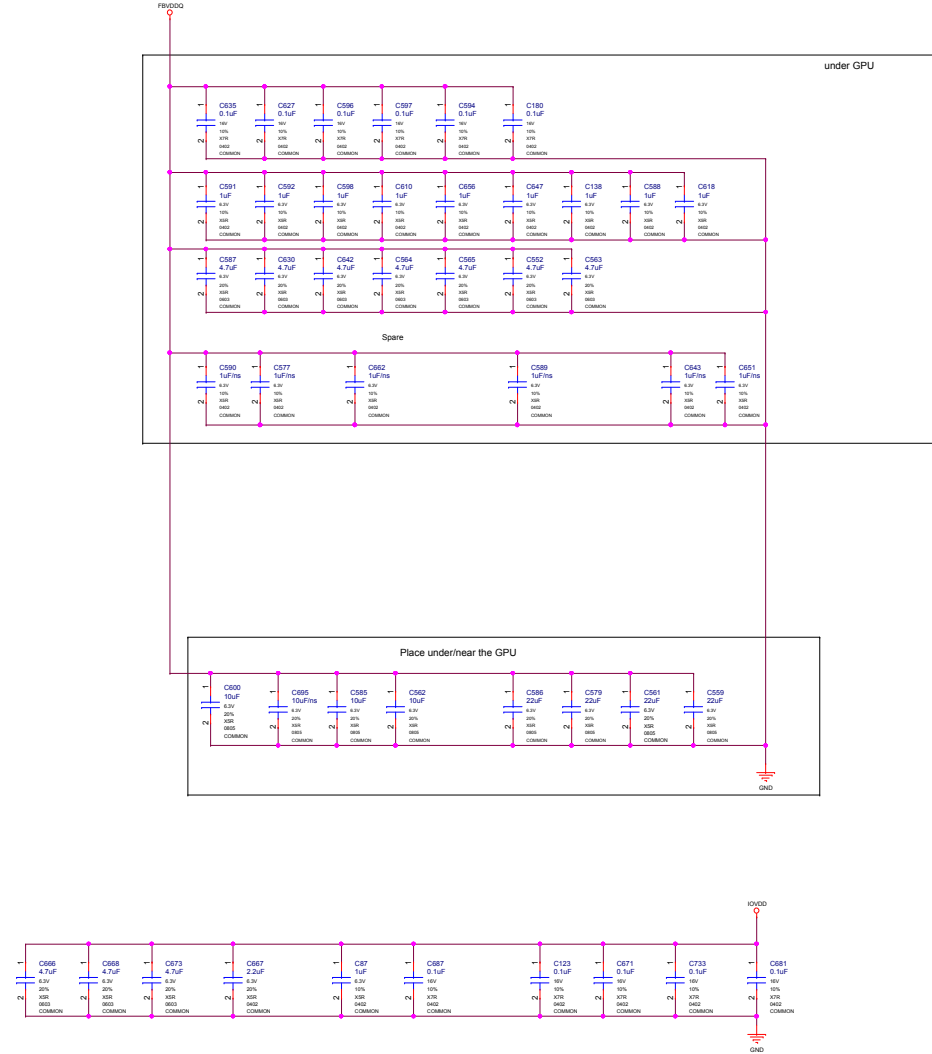
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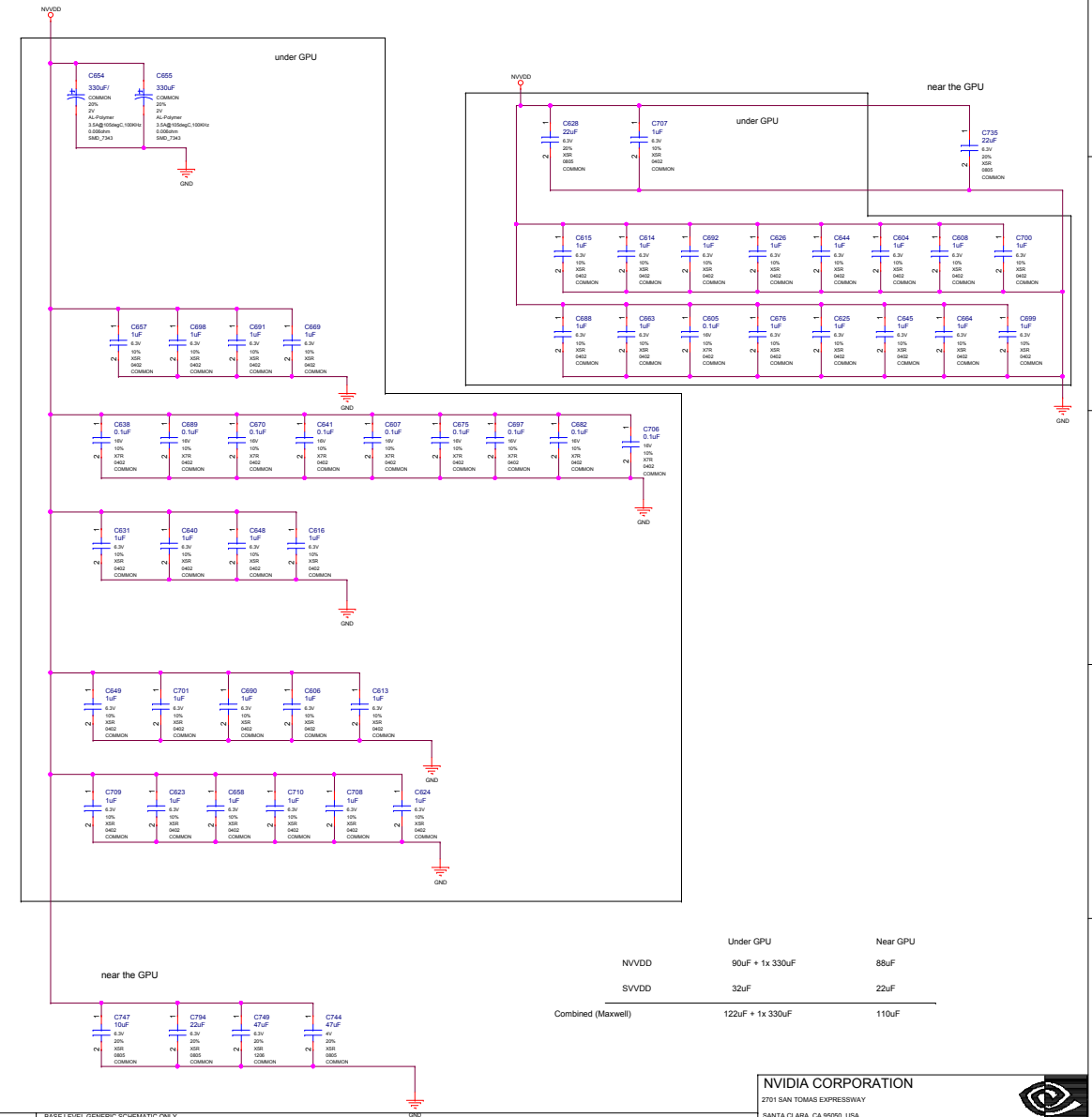
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GPU Decoupling

FBVDDQ



NVVDD



	Under GPU	Near GPU
NVDD	90uF + 1x 330uF	88uF
SVDD	32uF	22uF
Combined (Maxwell)	122uF + 1x 330uF	110uF

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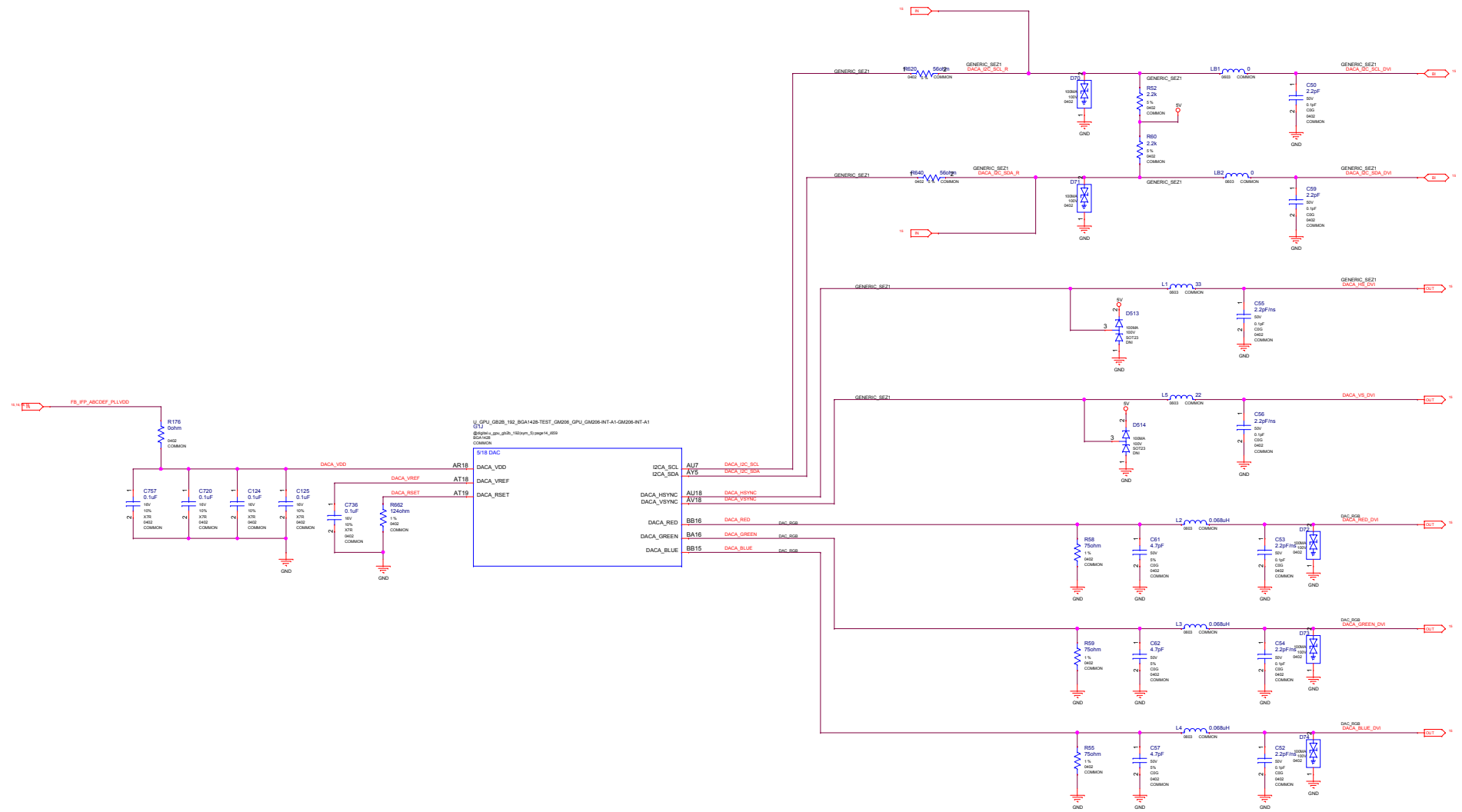


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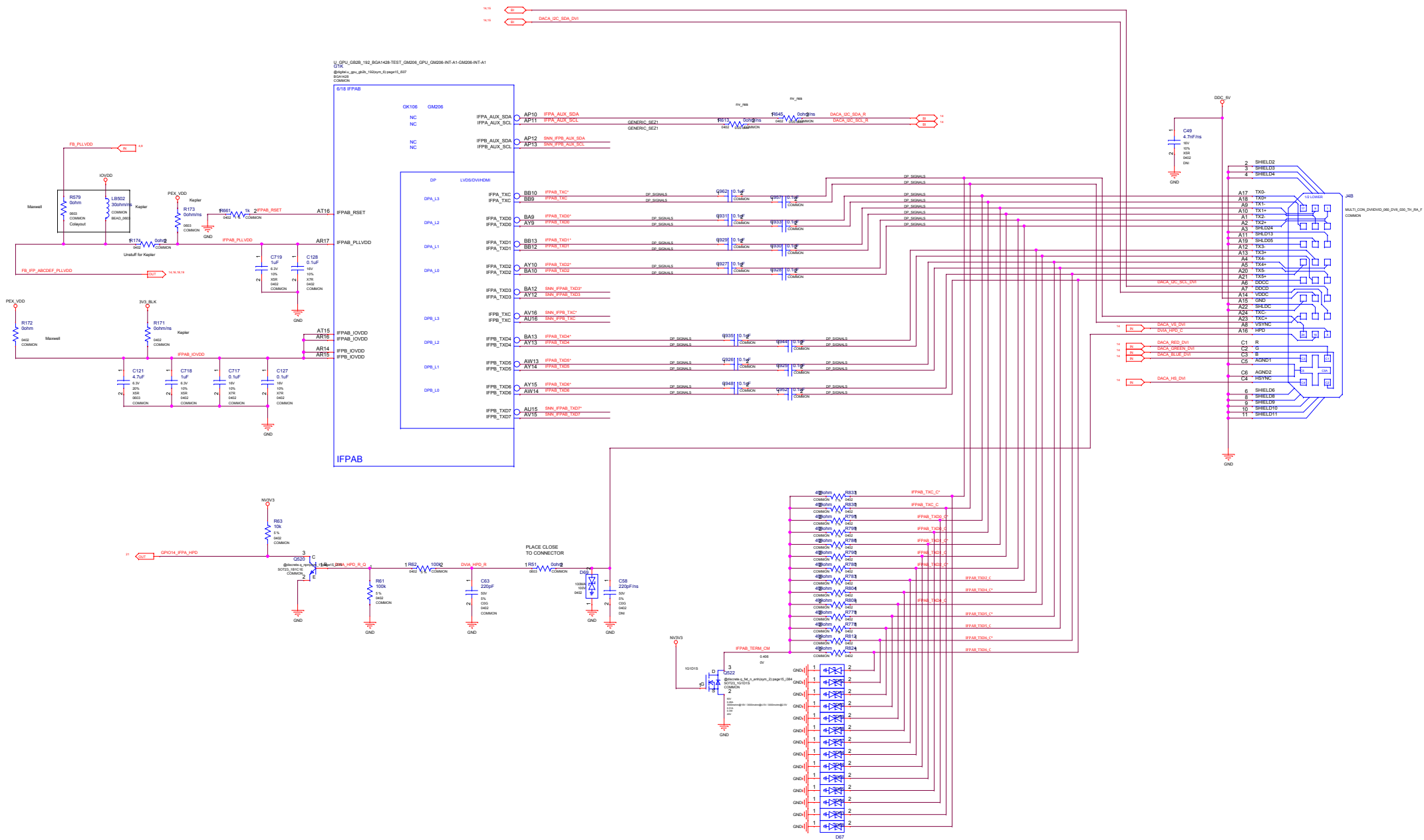
DACA Interface



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A

B

C

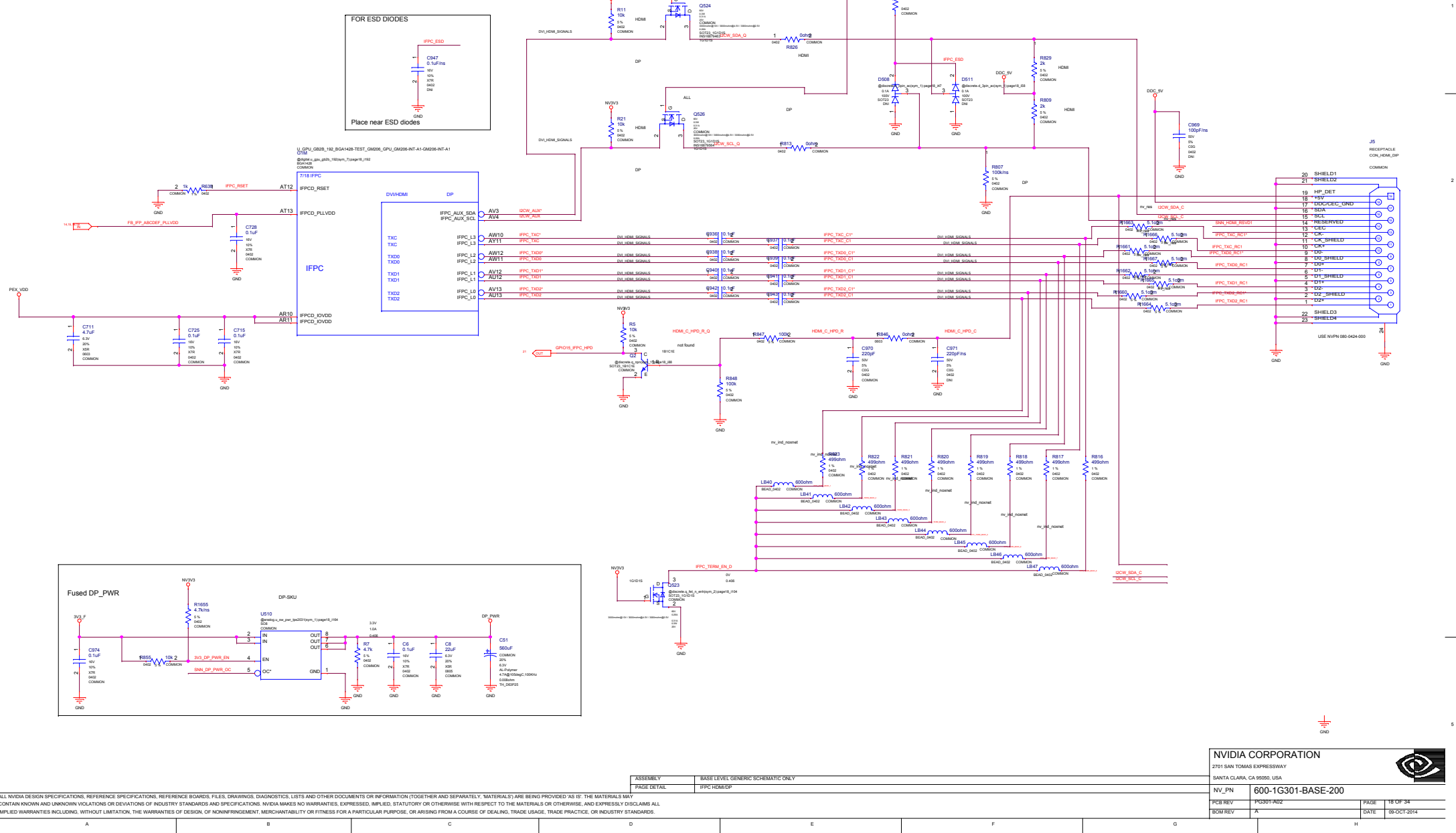
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E

F

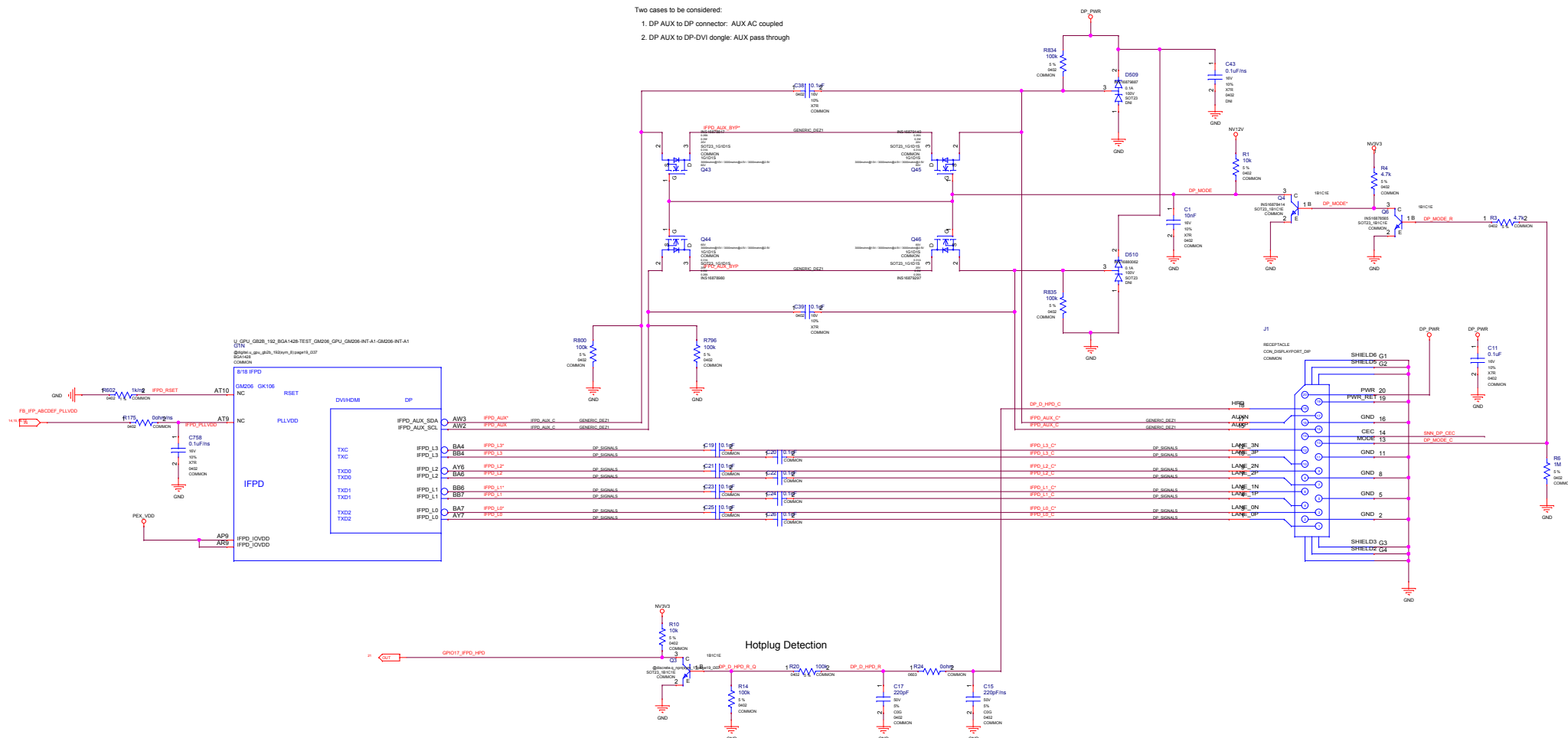
G

H



Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



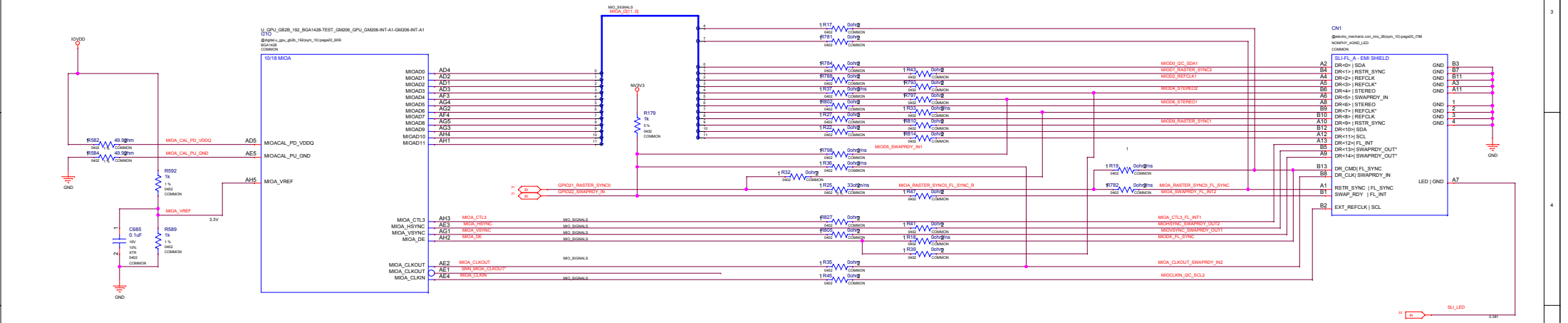
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MIOA/SLI Interface



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	3.3V	0.305	0.305
MIOA_CAL_PD_VDDQ	2.5V	0.305	0.305
MIOA_CAL_PD_GND	0.0V	0.305	0.305

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ASSEMBLY

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PAGE DETAIL

MIOA

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PCB REV

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08-OCT-2014

PCB REV

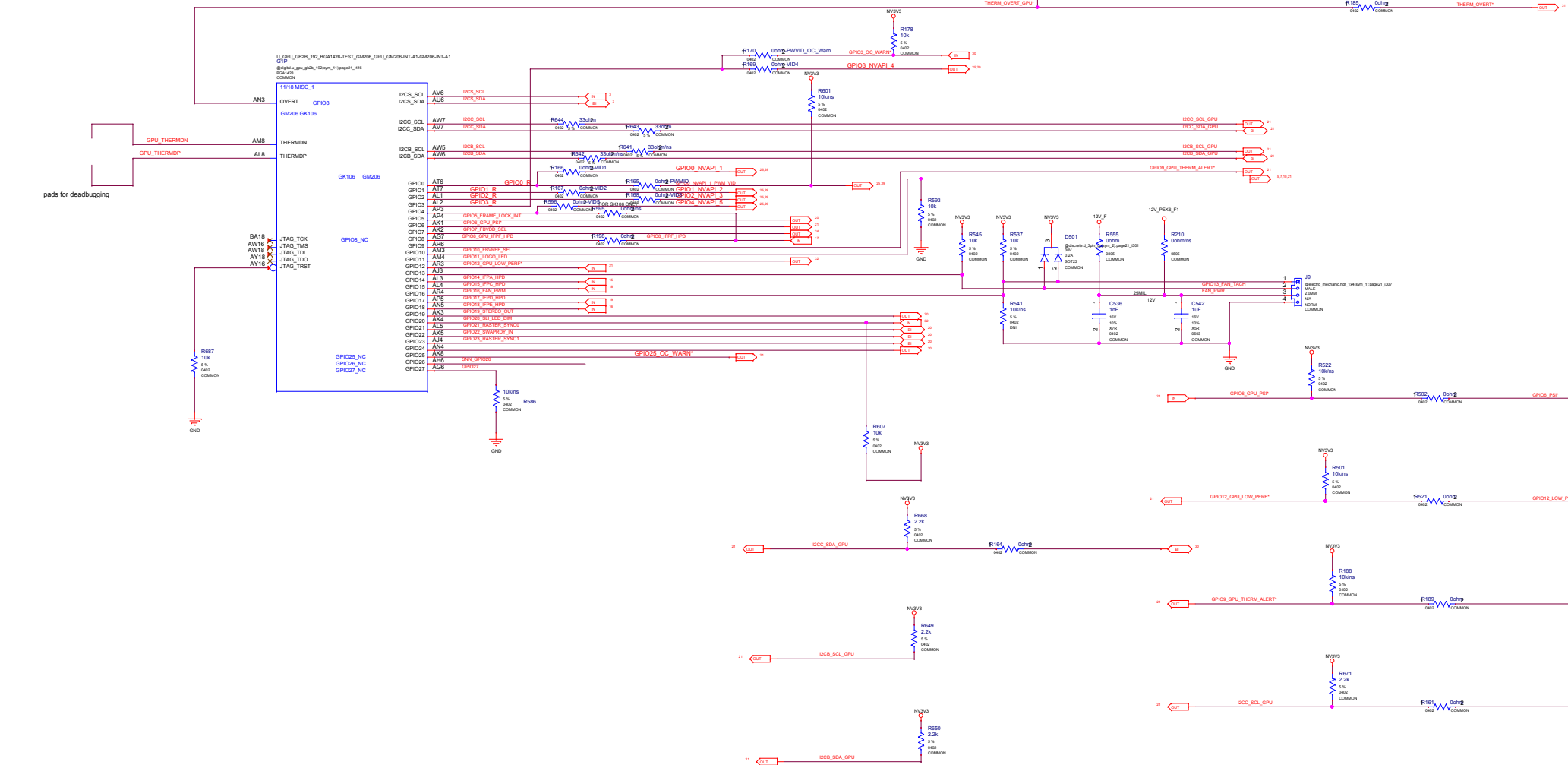
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08-OCT-2014




MISC1: Fan, Thermal, JTAG, GPIO



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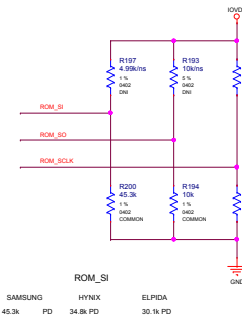
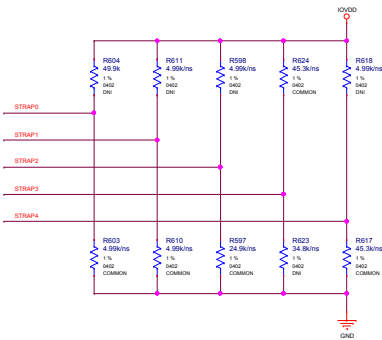
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MISC2: ROM, XTAL, Straps

	KEPLER	MAXWELL
STRAP0	USER_BIT [3:0]*	
STRAP1	3GIO_PADCFG_LUT_ADR*	
STRAP2	PCI_DEVID [3:0]*	
STRAP3	SOR_EXPOSED [3:0]*	
STRAP4	DP_PLL_VDD_33V*	
	PEX_MAX_SPEED*	
	PEX_SPD_CHANGE_GEN3*	
	*	
ROM_SI	RAMCFG[0]*	RAMCFG[0]*
	RAMCFG[1]*	RAMCFG[1]*
	RAMCFG[2]*	RAMCFG[2]*
	RAMCFG[3]*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	VGA_DEVICE*
	SMB_ALT_ADDR*	SMB_ALT_ADDR*
	FB[0]_APERTURE_SIZE*	PCIE_CFG*
	FB[1]_APERTURE_SIZE*	DEVID_SEL*
	PEX_PLL_EN_TERM100*	SOR0_EXPOSED*
ROM_SCLK	PCI_DEVID_EXT[5]*	SOR1_EXPOSED*
	SUB_VENDOR*	SOR2_EXPOSED*
	PCI_DEVID_EXT[4]*	SOR3_EXPOSED*

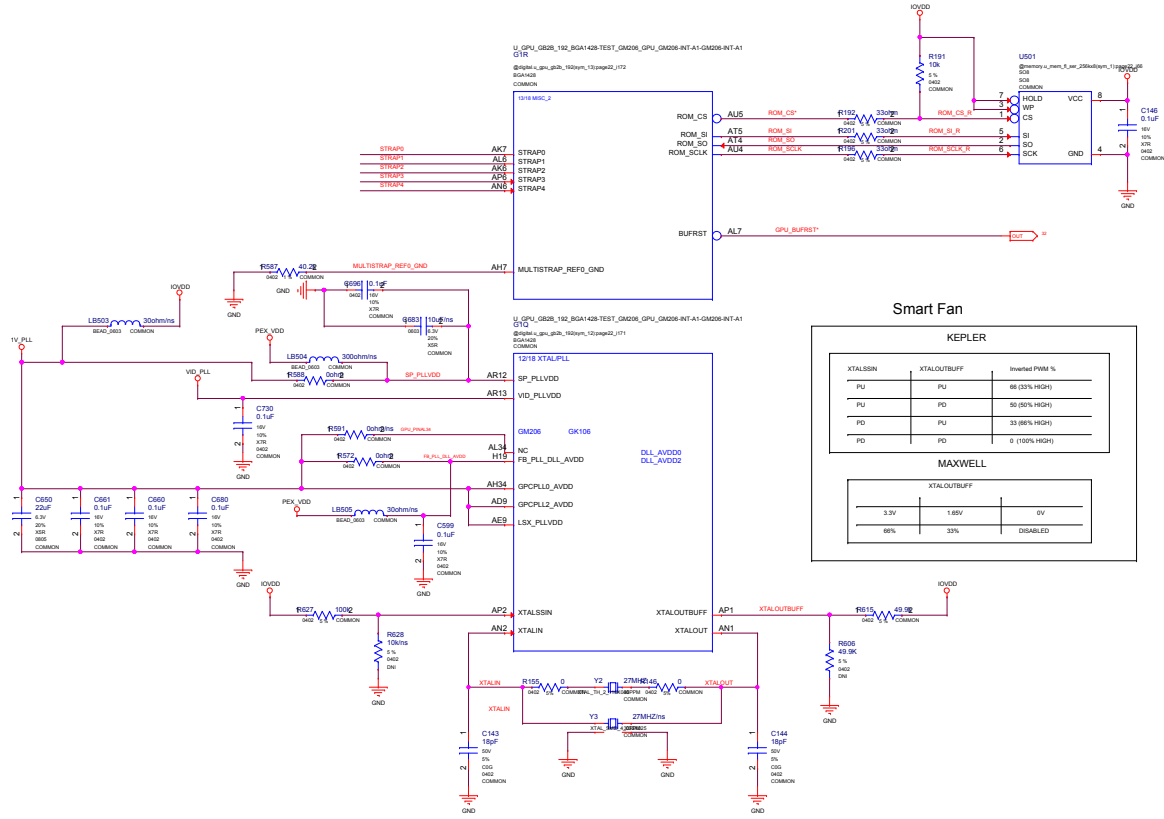
MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND

MAXWELL		
3.3V	1.65V	0V
GPU ISLAND ENABLED	GPU DEBUG MODE	GPU ISLAND DISABLED

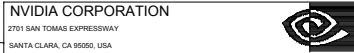


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC2: ROM, XTAL, Straps

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

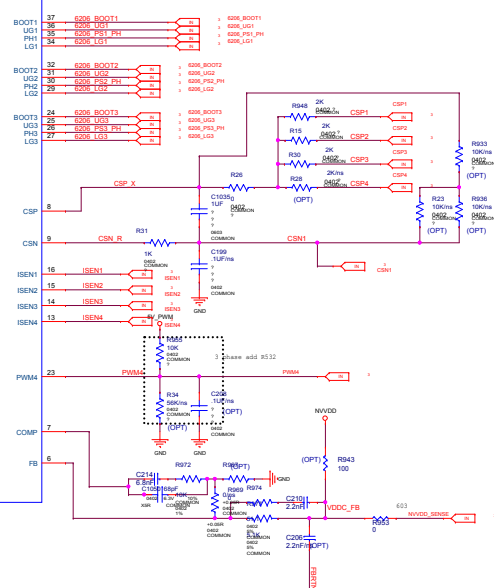
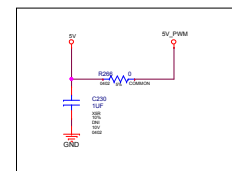
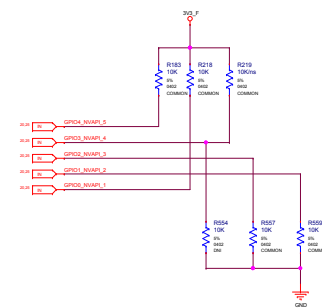


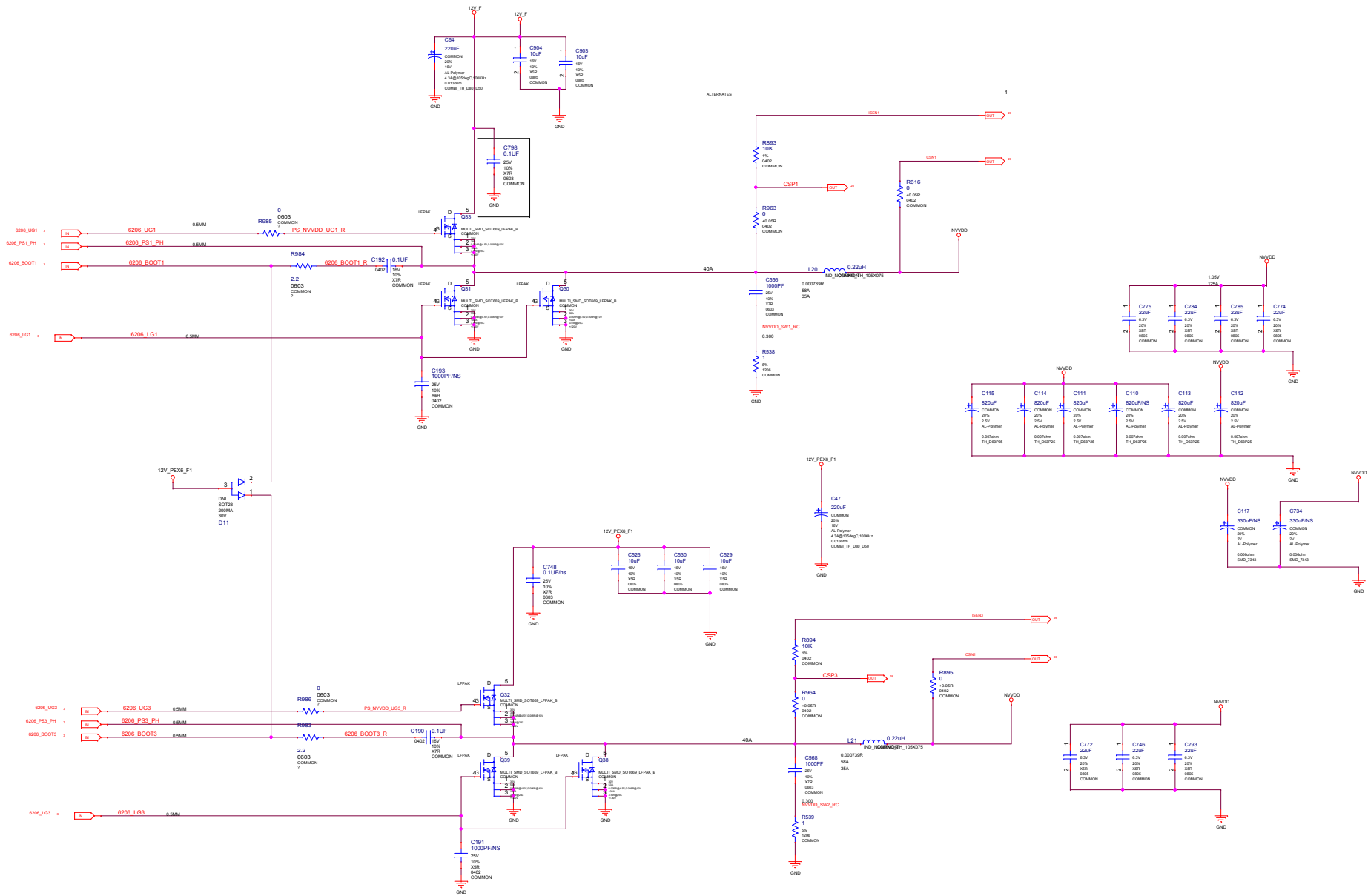
Smart Fan		
KEPLER		
XTALSSN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PD	PD	50 (25% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)
MAXWELL		
XTALOUTBUFF		
3.3V	1.65V	0V
66%	33%	DISABLED

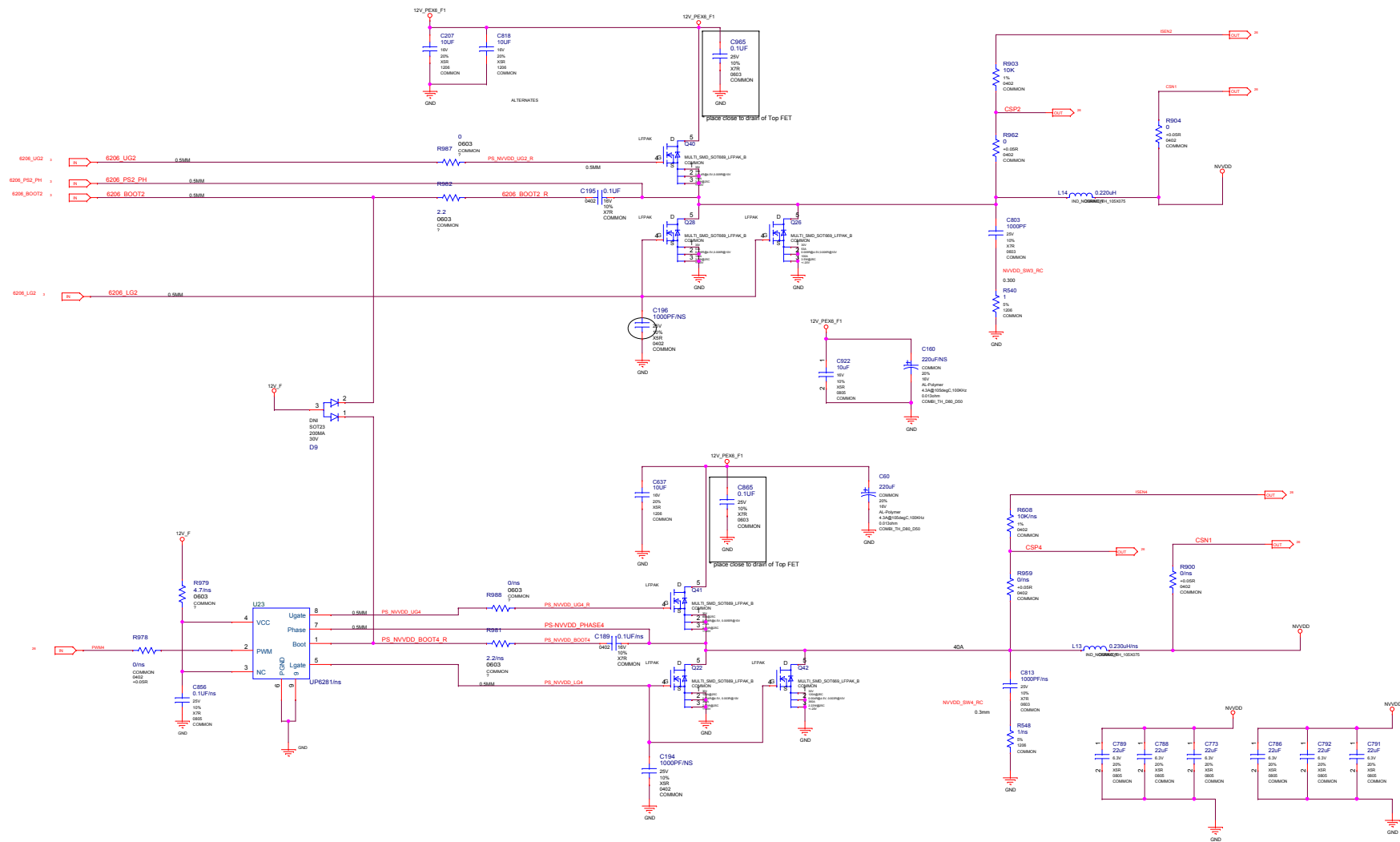


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DATE	06-OCT-2014

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[illegible]





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	(RESERVED)

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NV_PN	600-1G301-BASE-200		
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A number line from 0 to 10. A vertical line is drawn at 5, and a horizontal line is drawn at 5. The intersection is labeled 'H'.

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BOM REV	A	DATE	09-OCT-2014
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	H
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PS: NVVDD OVR2+1 POWER


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD OVR2+1 option

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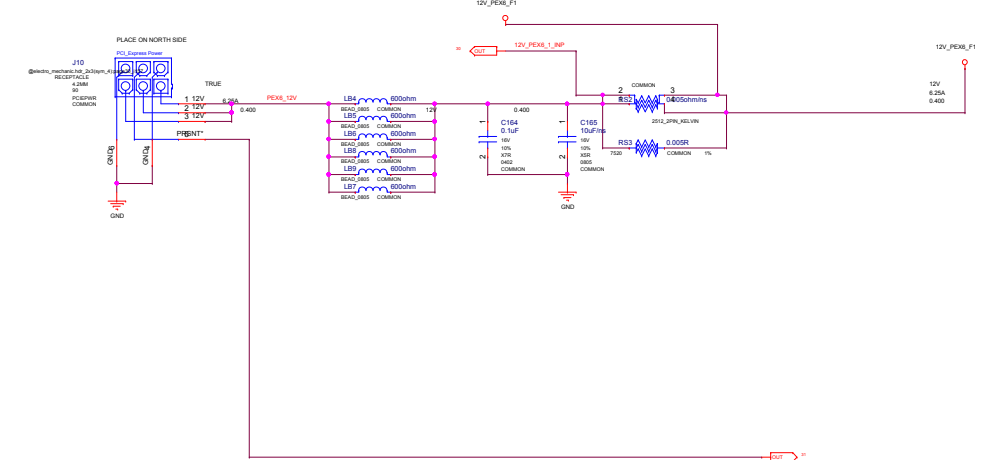
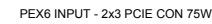
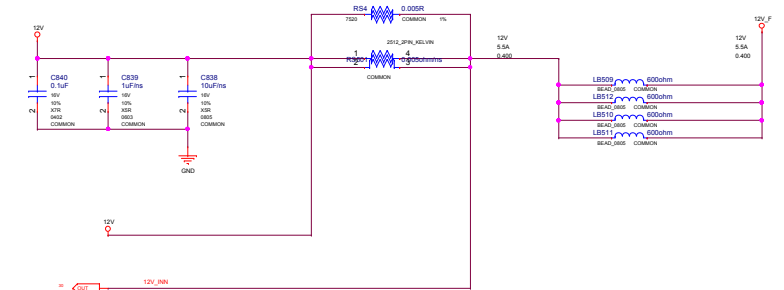
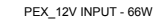
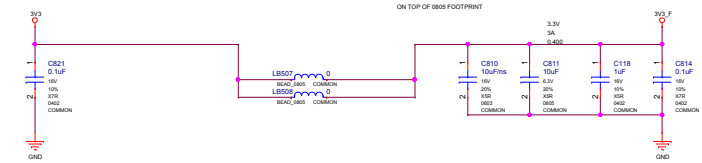
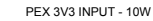
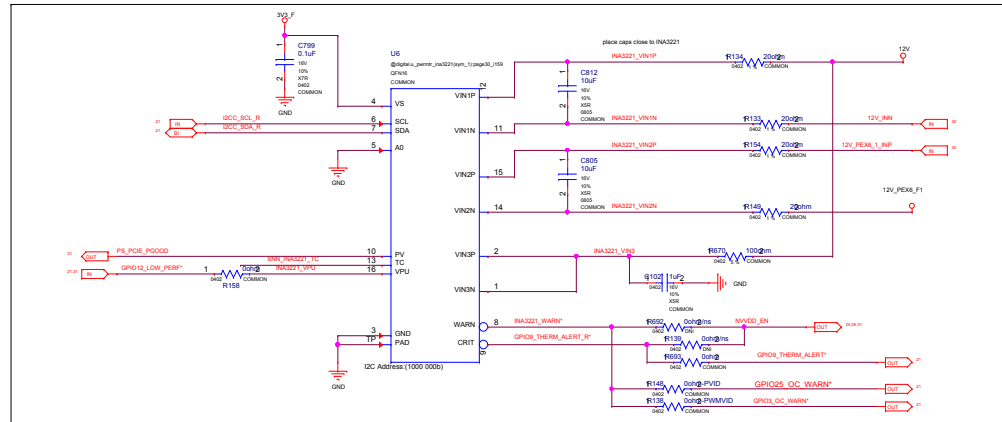
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PS: Inputs, Filtering, and Monitoring



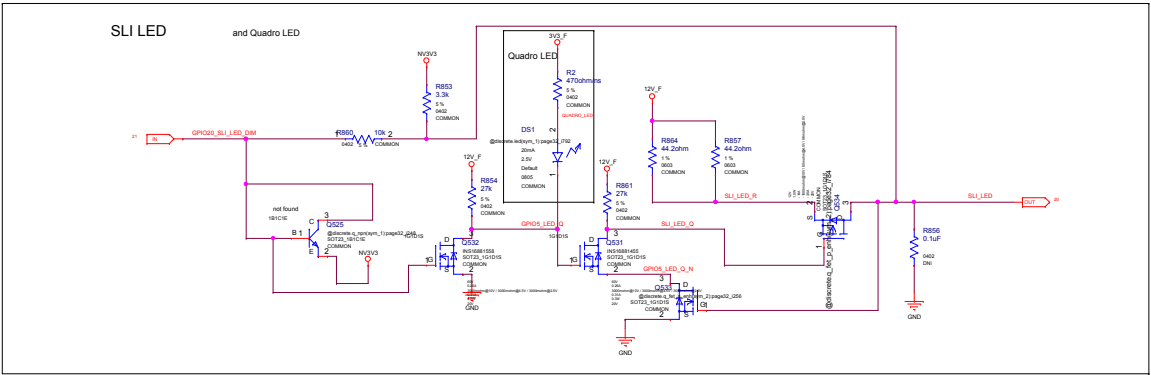
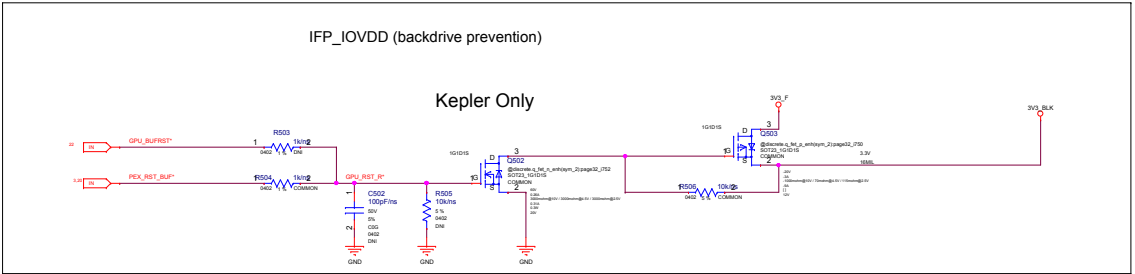
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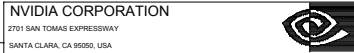
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LEDs

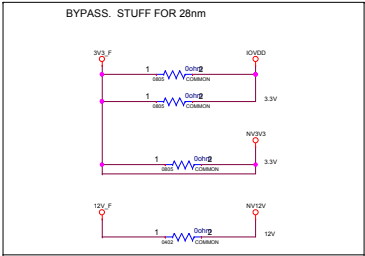


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PS: IOVDD, NV3V3, NV12V



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PAGE DETAIL	PS: IOVDD Regulator

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