

PG111-A01

GP108 64Bit sDDR4 X16

HDMI/DP + DL DVI-D /DP

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NV_PN

600-1G111-BASE-A01

PCB REV

PG111-A01

BOM REV


A

PAGE

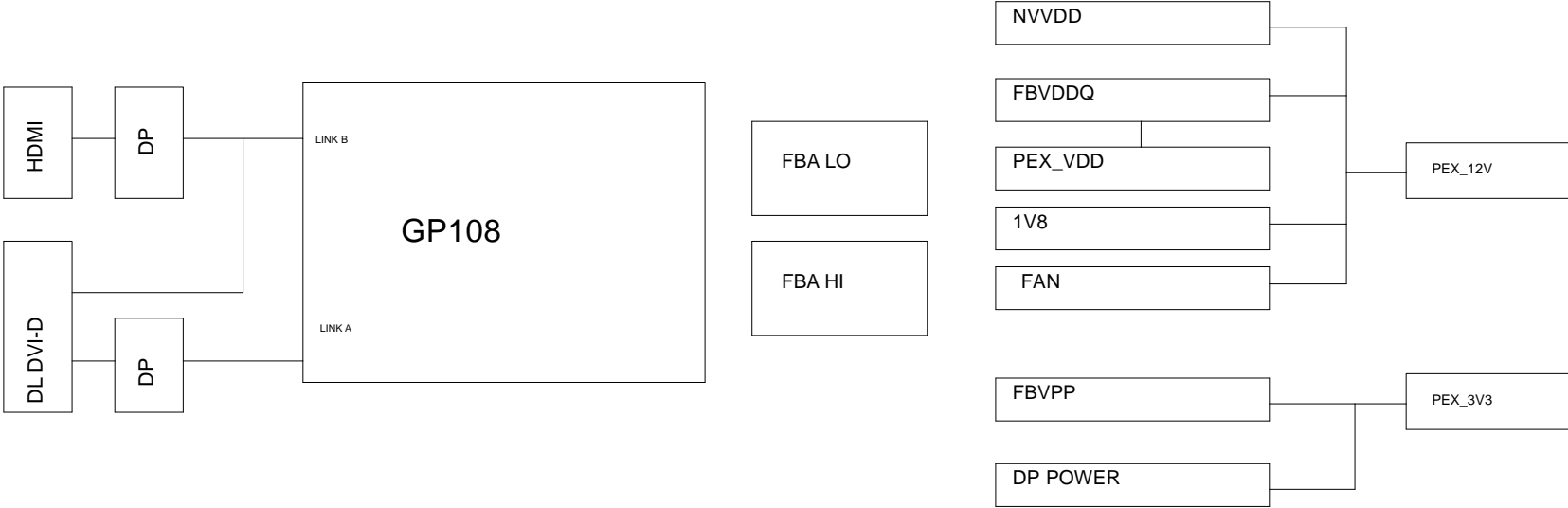
1 OF 21

DATE

16-FEB-2017



Block Diagram

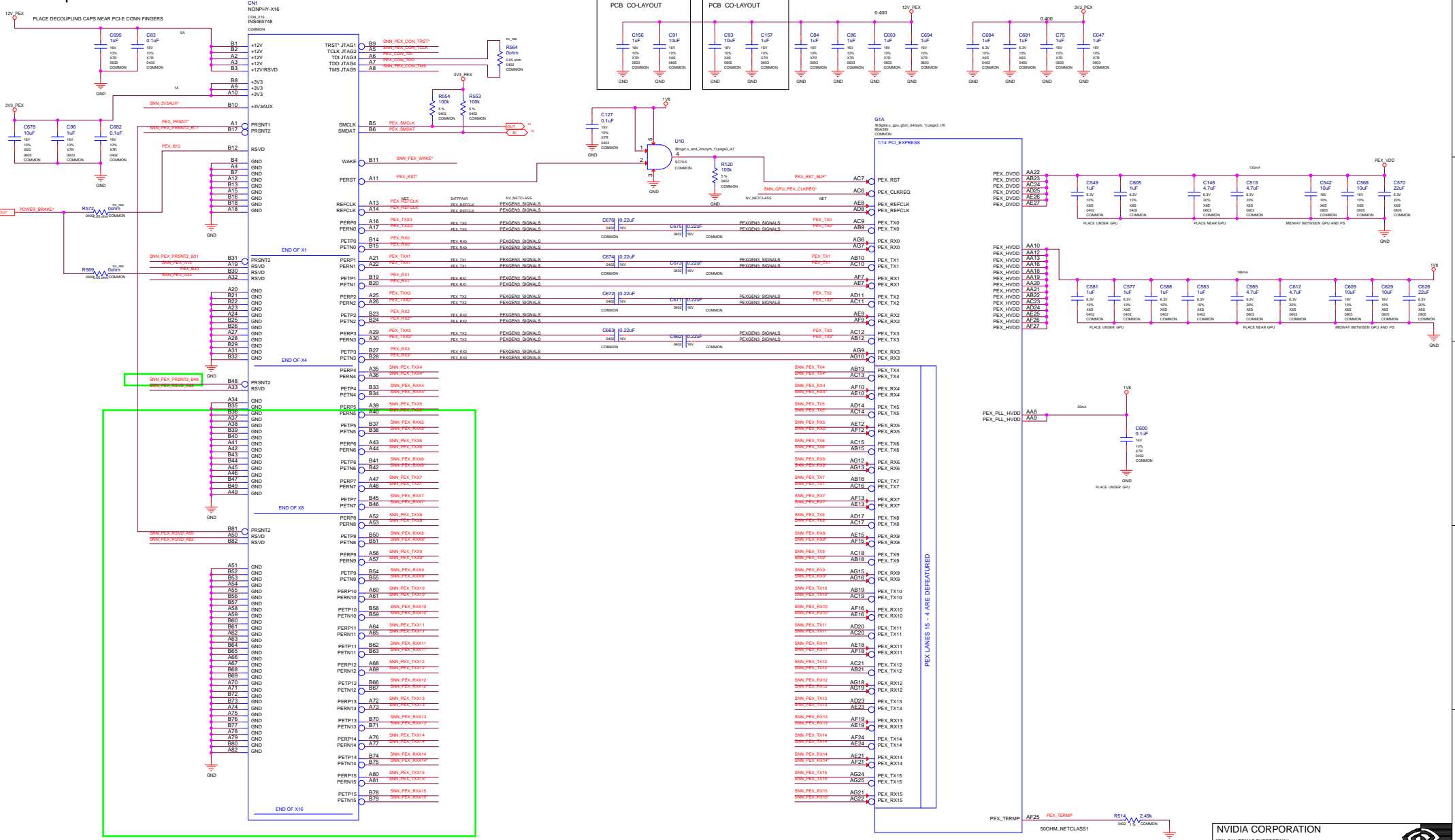


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PAGE DETAIL	Block Diagram

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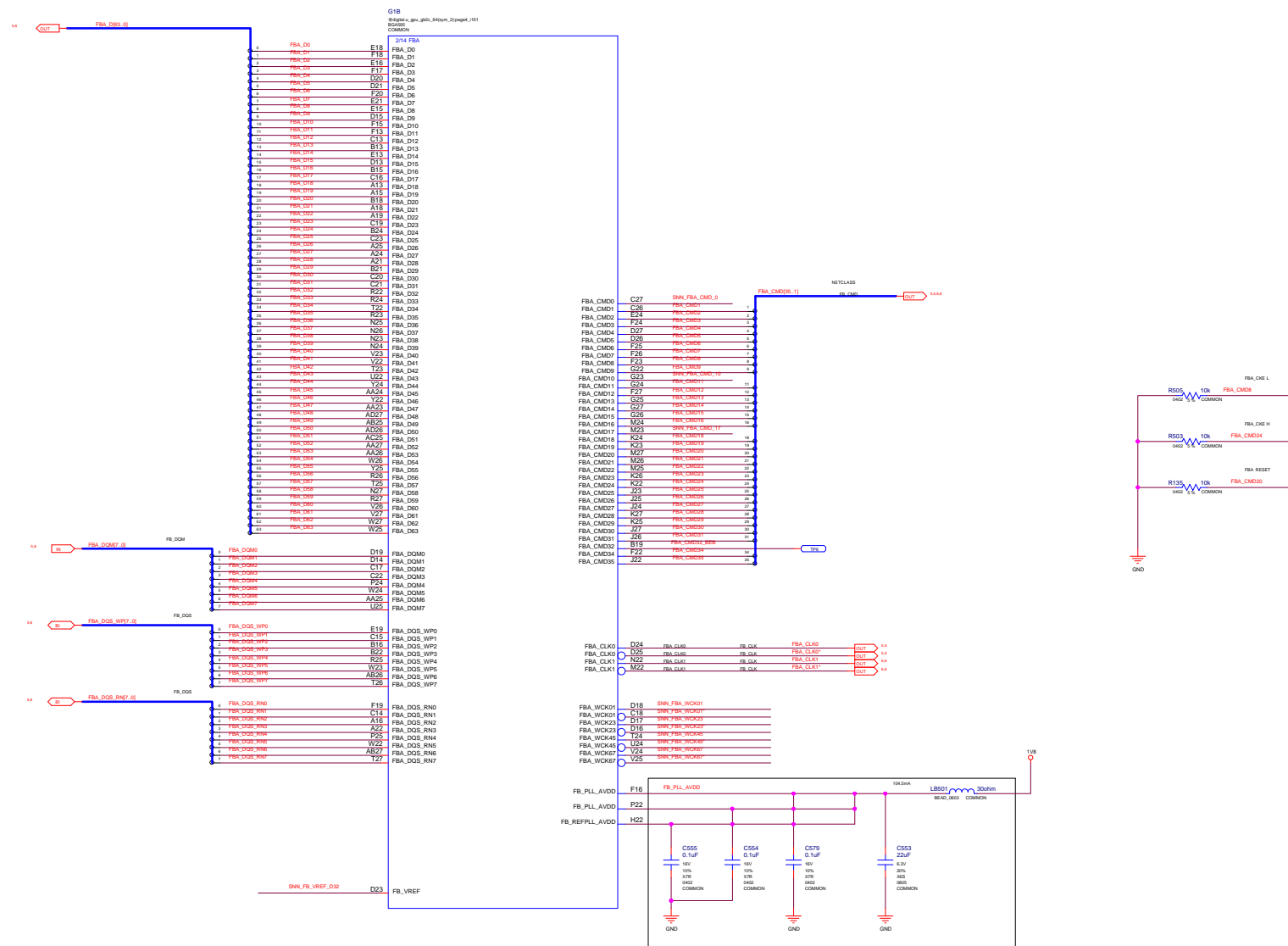
PCI Express



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REV		PCB REV	PG111-A01
ISOLATES ALL		DATE	10-FEB-2017
STANDARDS			

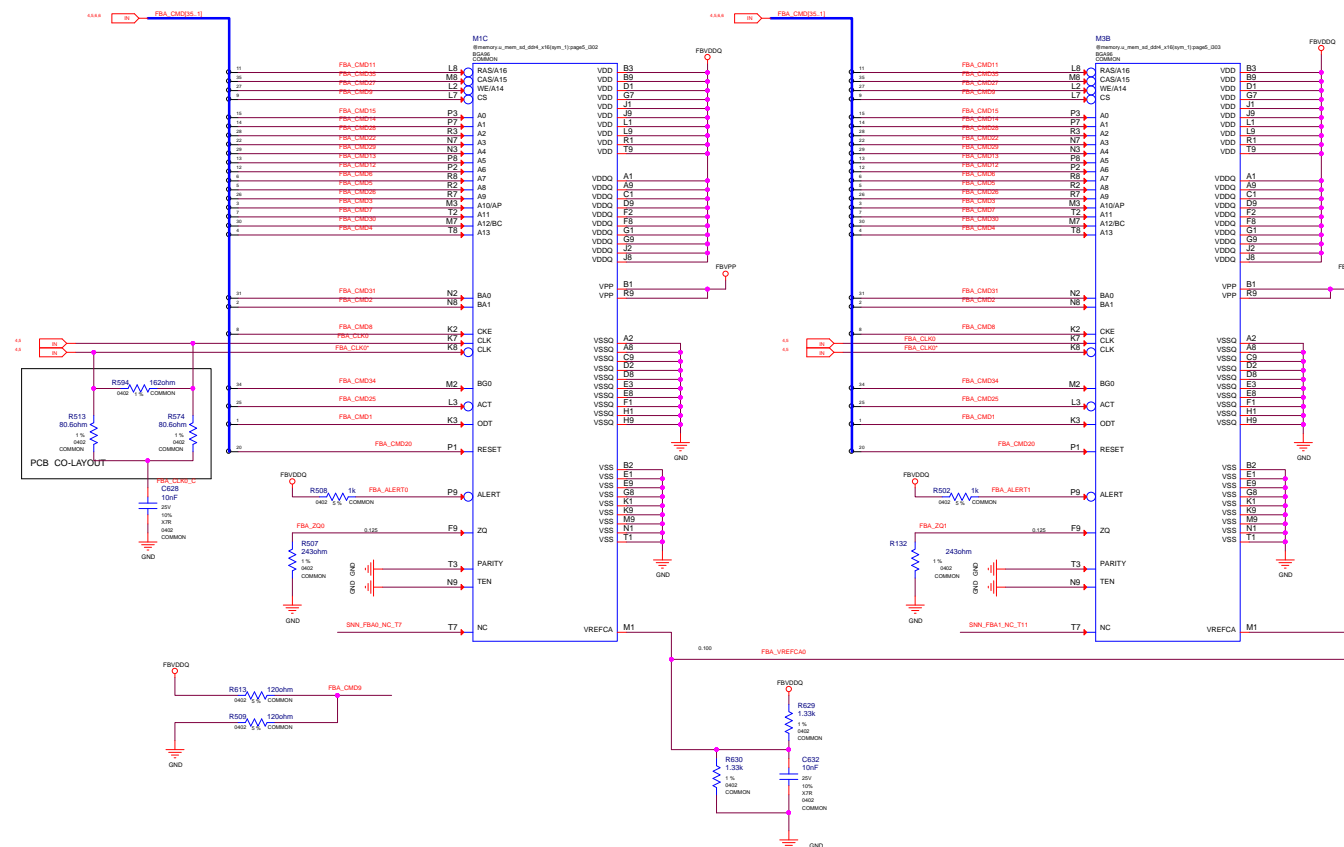
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GPU Frame Buffer

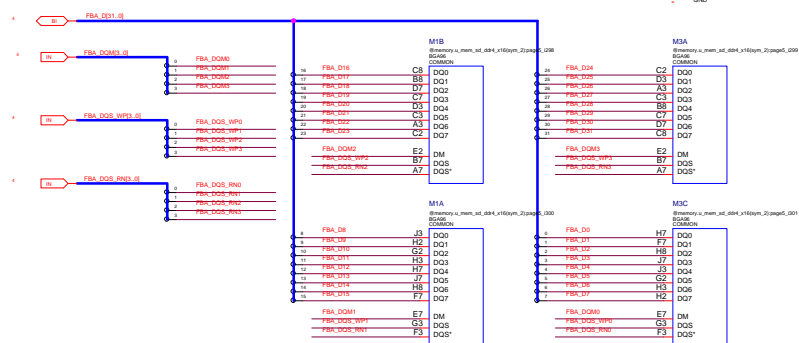
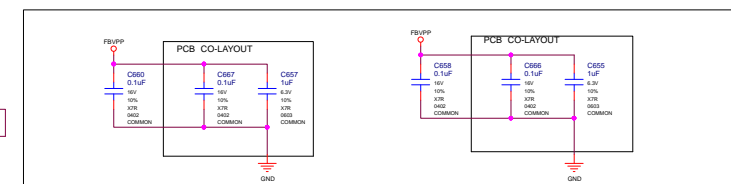
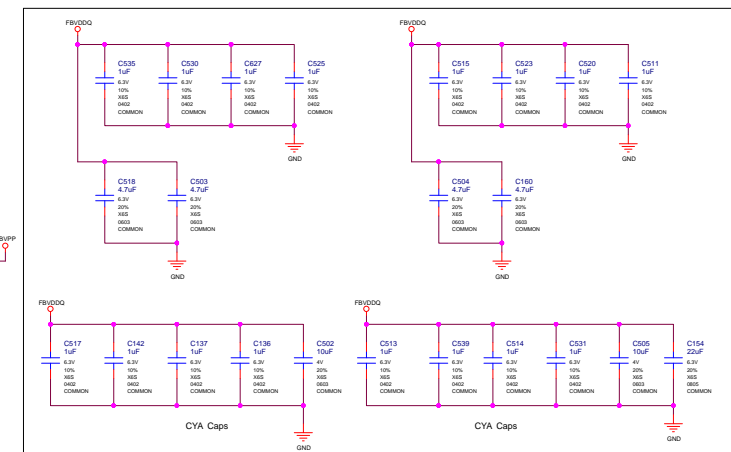


	LOWER	UPPER
	L31	S2-8
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MS02	MS1	MS1
MS03	MS14	MS14
MS04	MS1	MS1
MS05	MS1	MS1
MS06	MS1	MS1
MS07	MS1	MS1
MS08	MS1	MS1
MS09	MS1	MS1
MS10	MS1	MS1
MS11	MS1	MS1
MS12	MS1	MS1
MS13	MS1	MS1
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MS137	MS1	MS1
MS138	MS1	MS1
MS139	MS1	MS1
MS140	MS1	MS1
MS141	MS1	MS1
MS142	MS1	MS1
MS1		

FBA bits 31..00



Each memory
4x1uF 0402
2x4.7uF 0603



ASSEMBLY	«ASSEMBLY_DESCRIPTION
PAGE DETAIL	FBA bits 31..00

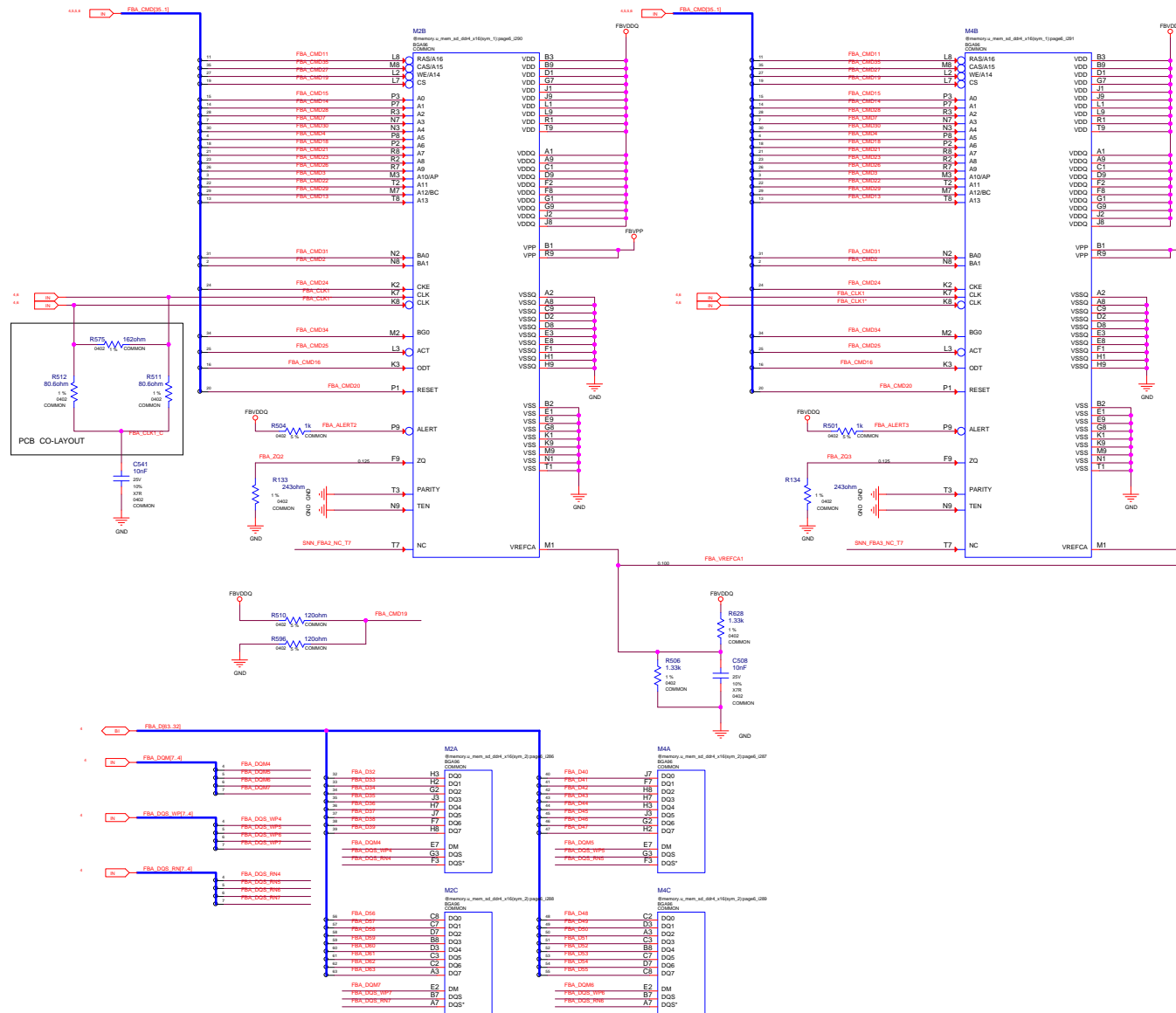
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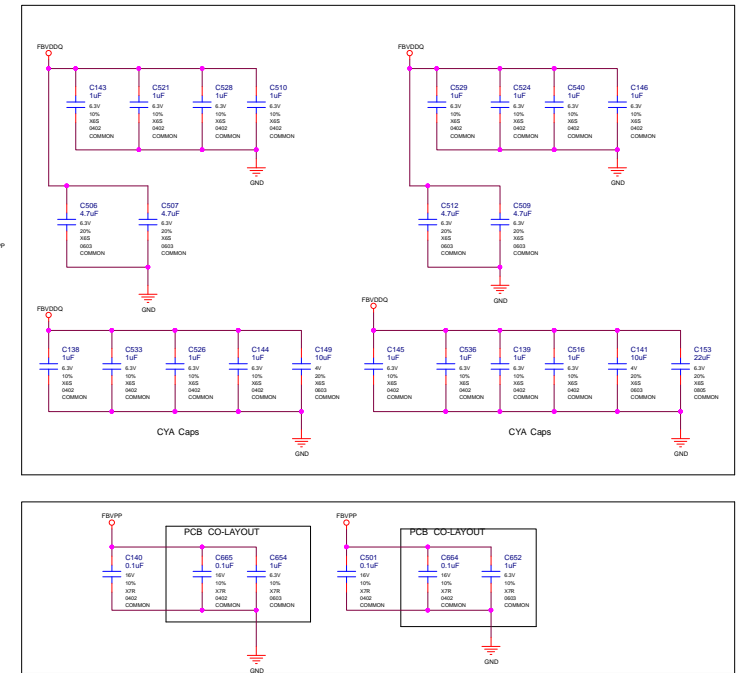


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FBA bits 63..32



Each memory
4x1uF 0402
2x4.7uF 0603



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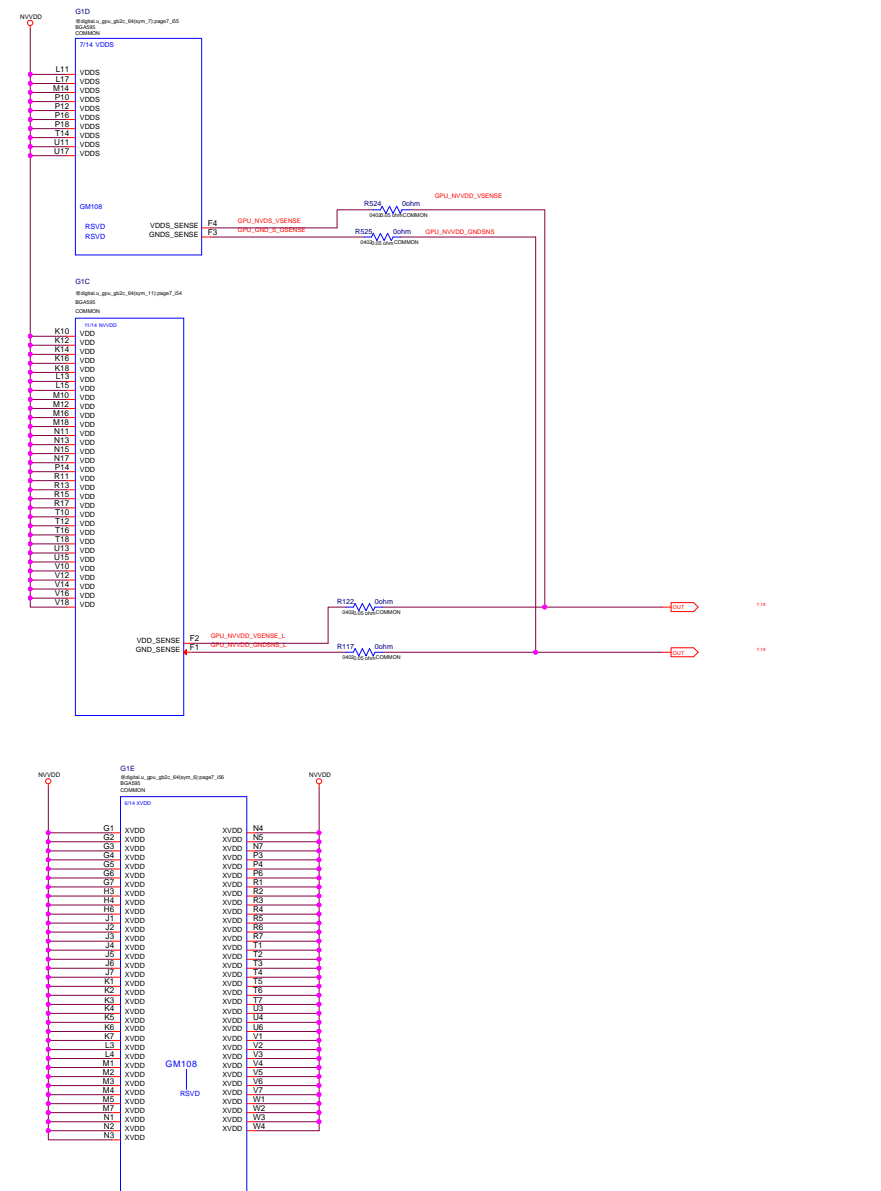
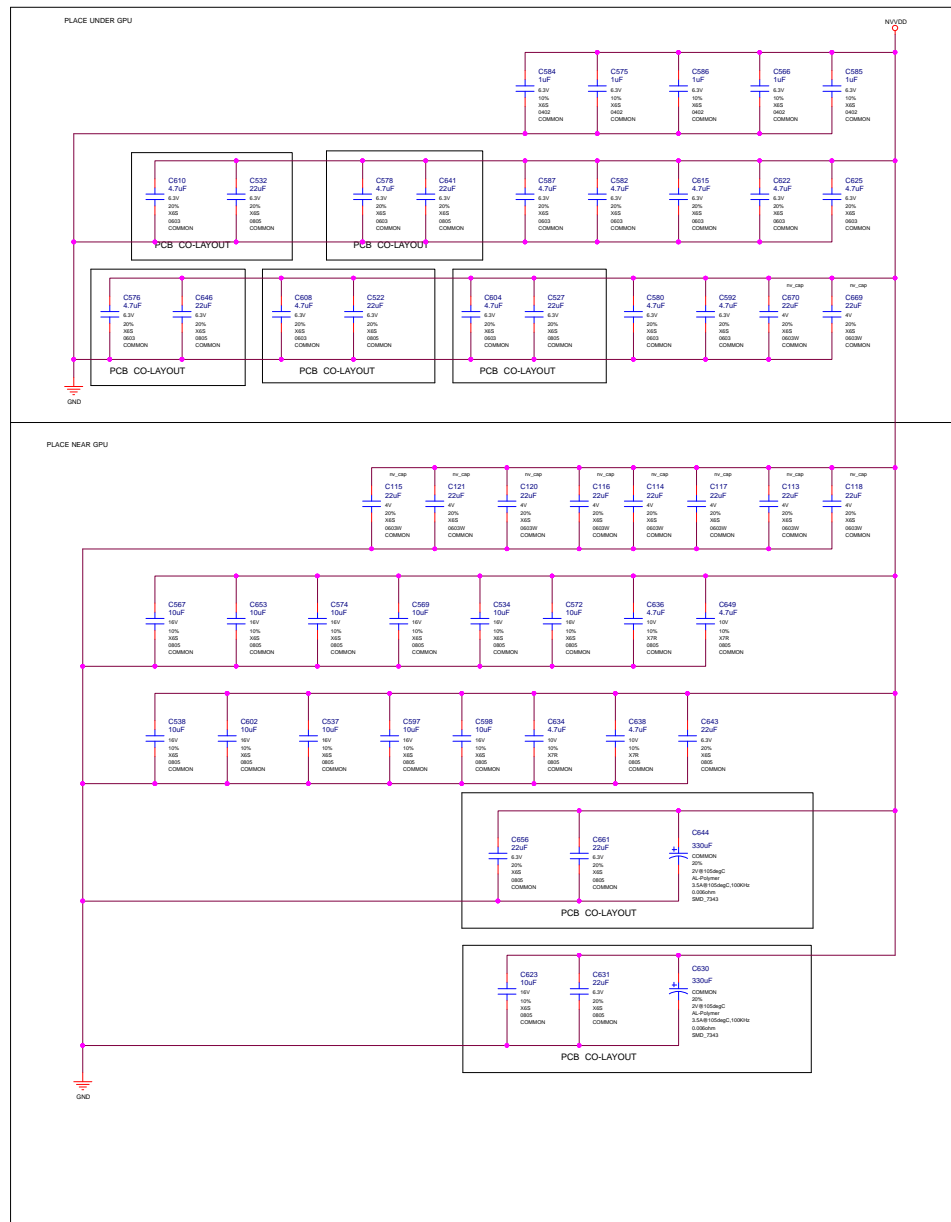


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PAGE DETAIL	FBA bits 63.32

NVDD Decoupling

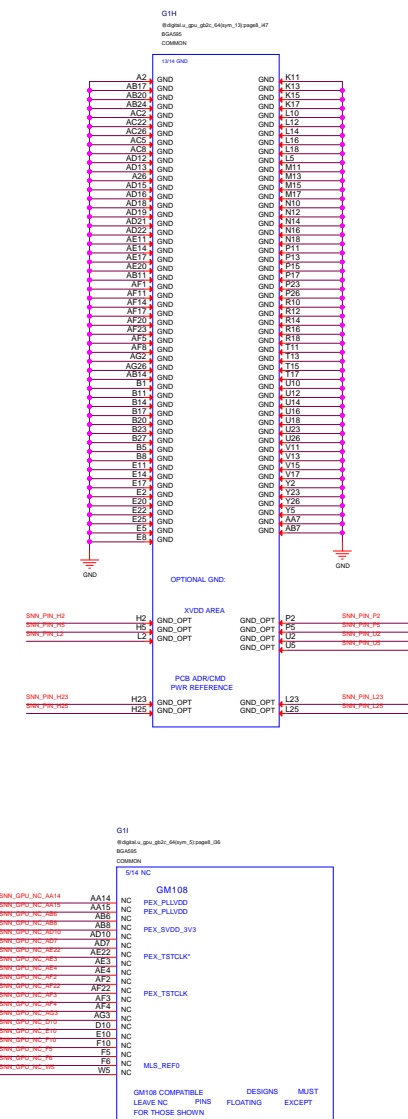
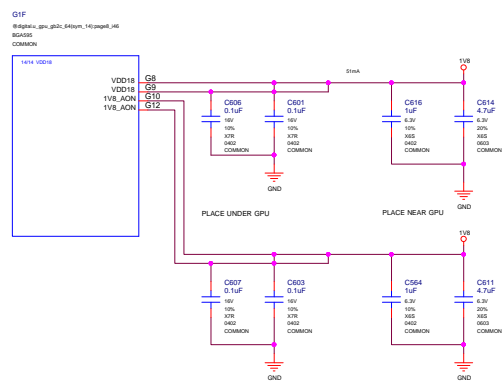
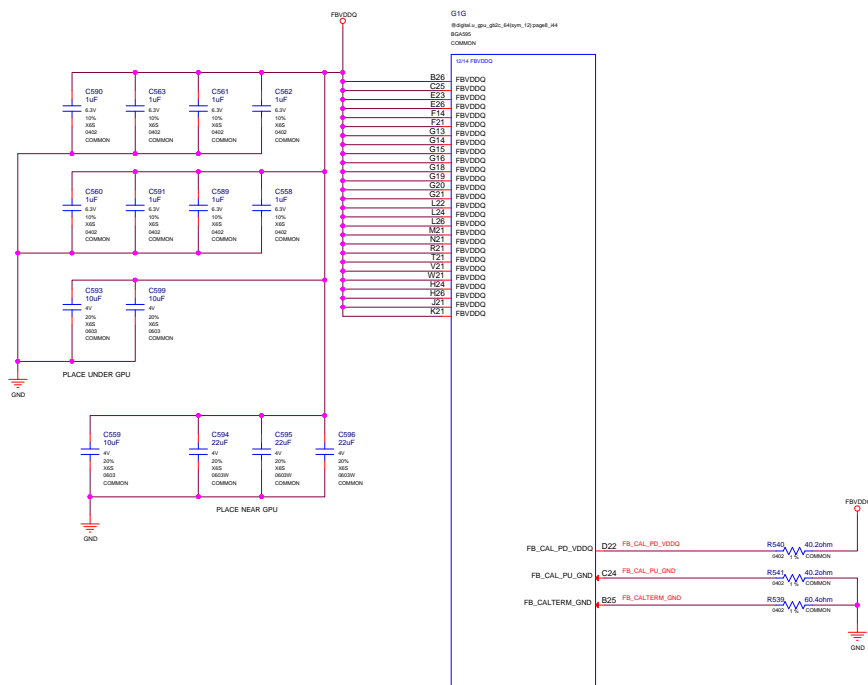


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FBVDDQ and 1V8 Decoupling



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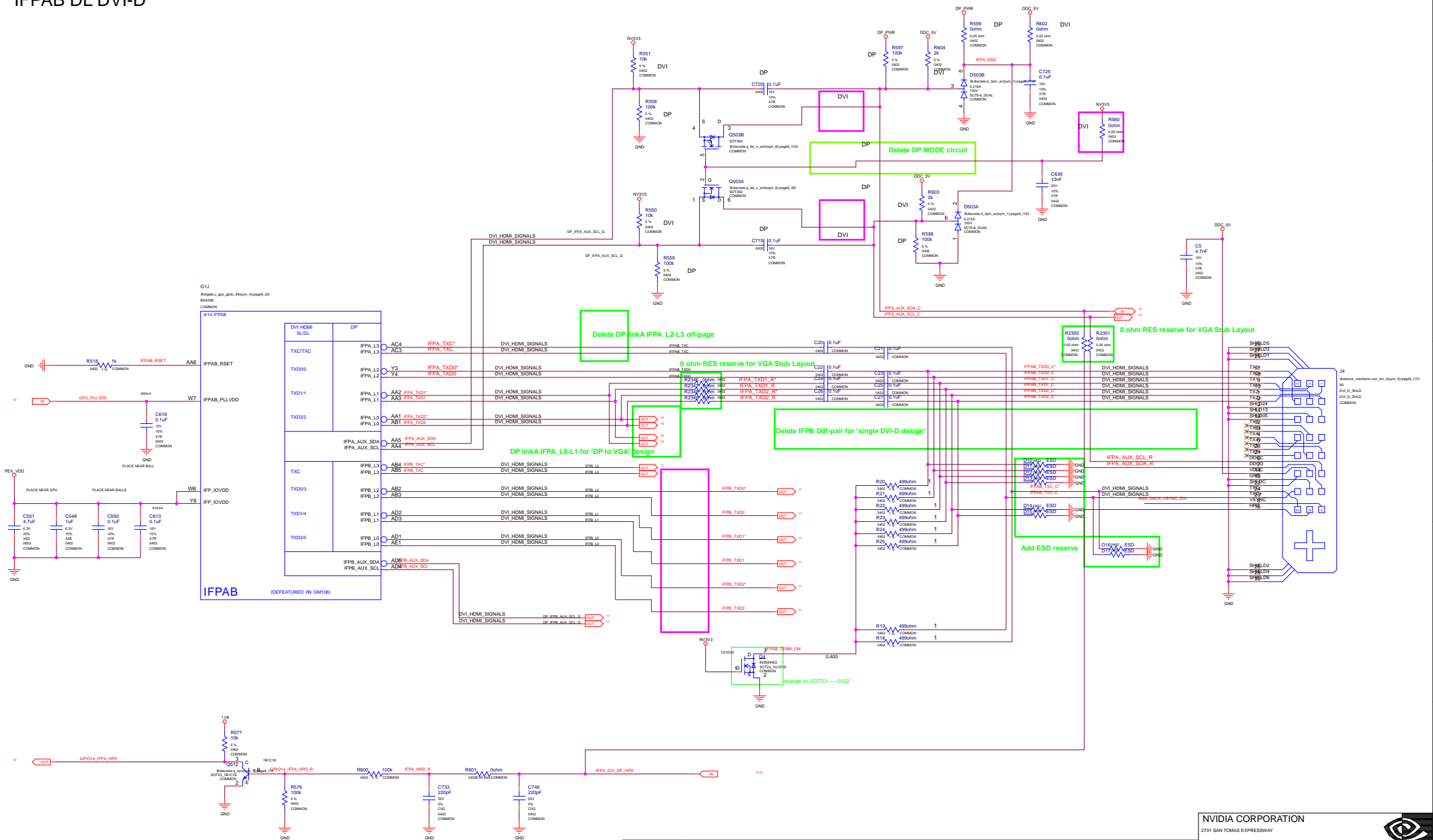
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IFPAB DL DVI-D



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IFPB HDMI/DP

8.11
8.11
8.11
8.11
8.11
8.11

10

Hotplug Detection

change to SOT23—0122

DP-SKU ONLY

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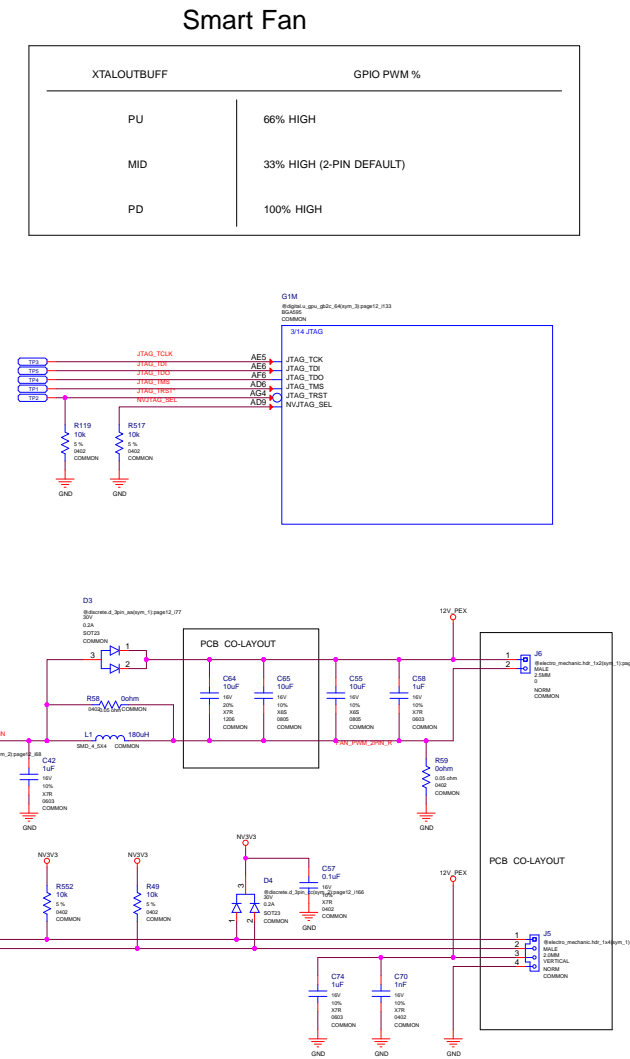
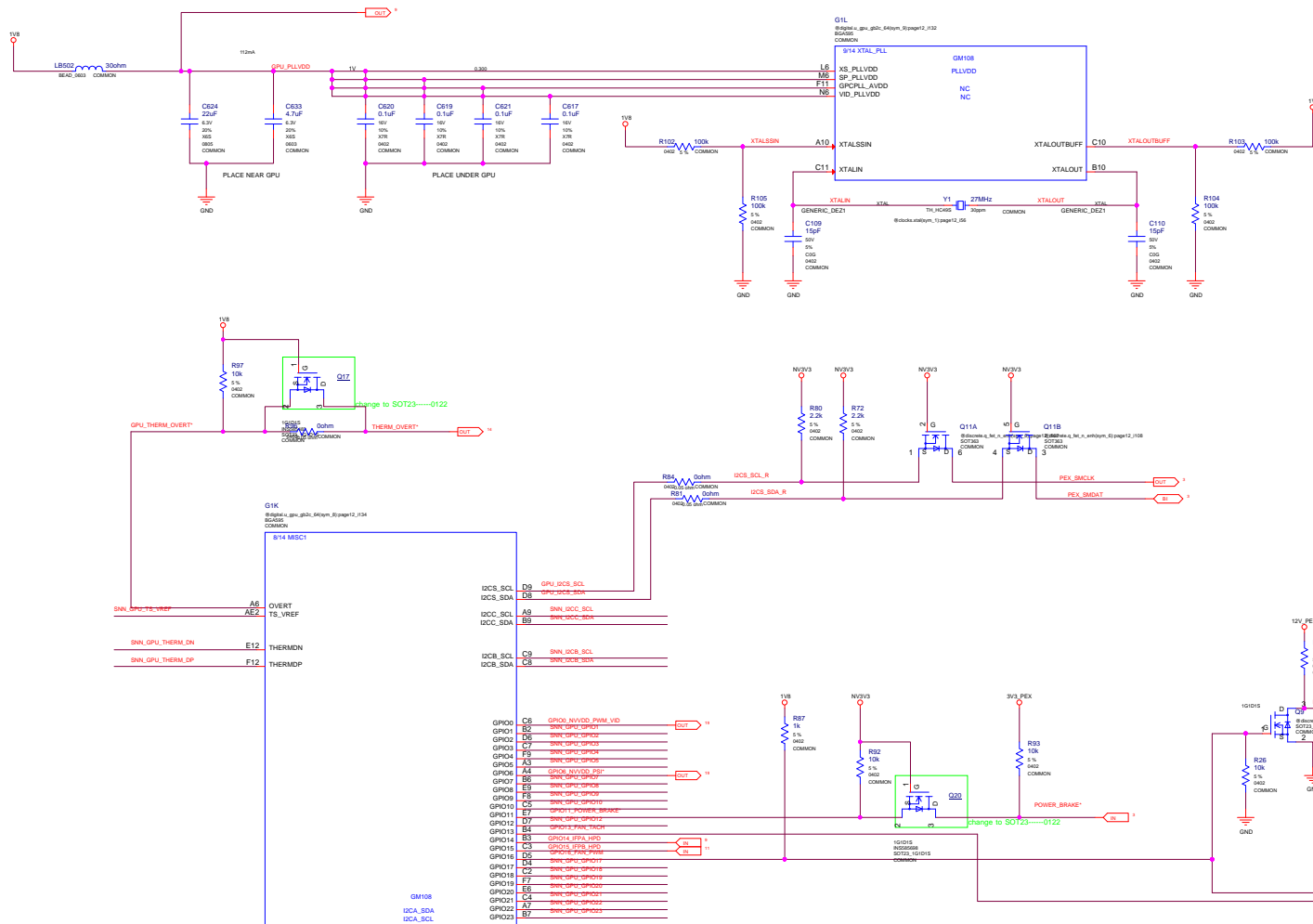
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ASSEMBLY ->ASSEMBLY_DESCRIPTION-
PAGE DETAIL IFPB DP/HDMI

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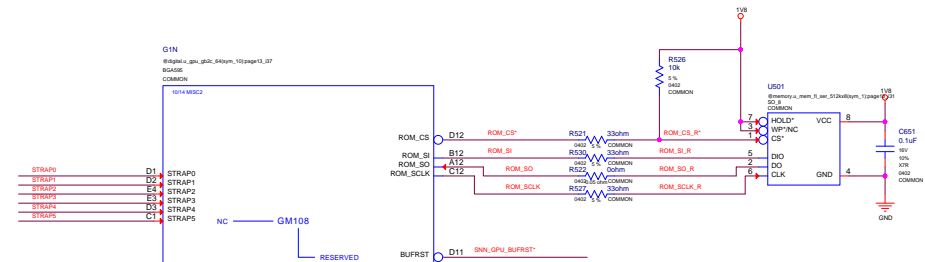
JTAG,GPIO&XTAL



ROM & STRAPS

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	SOR0/1 ENABLE
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	0000
L	L	H	0001
L	H	L	0010
L	H	H	0011
H	H	L	0110
H	H	H	0111
L	L	M	1000
L	M	L	1001

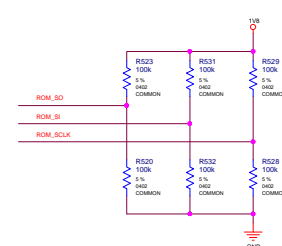
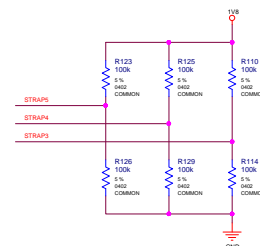
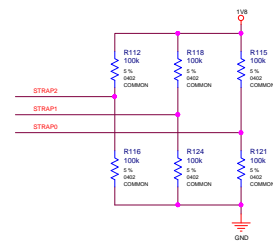
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```



ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	ROM & STRAPS

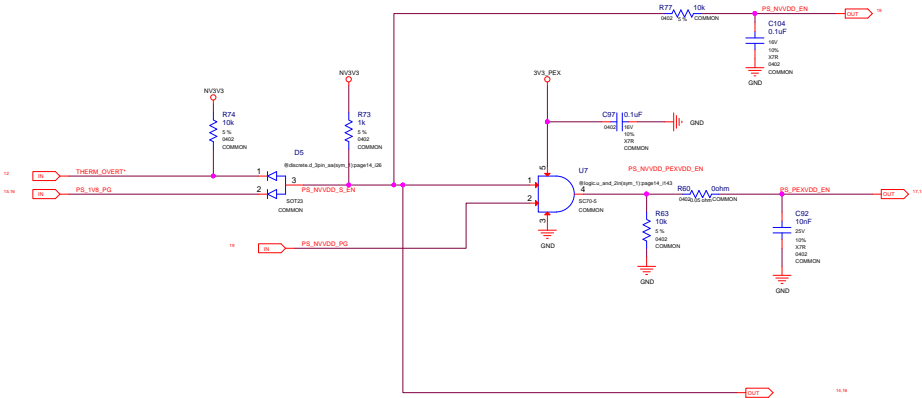
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Power Sequence




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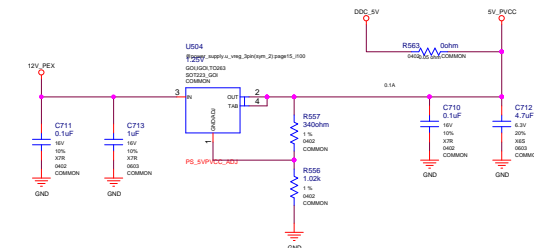
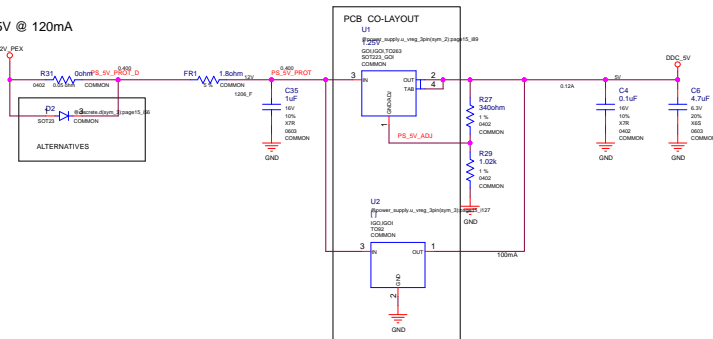
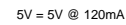
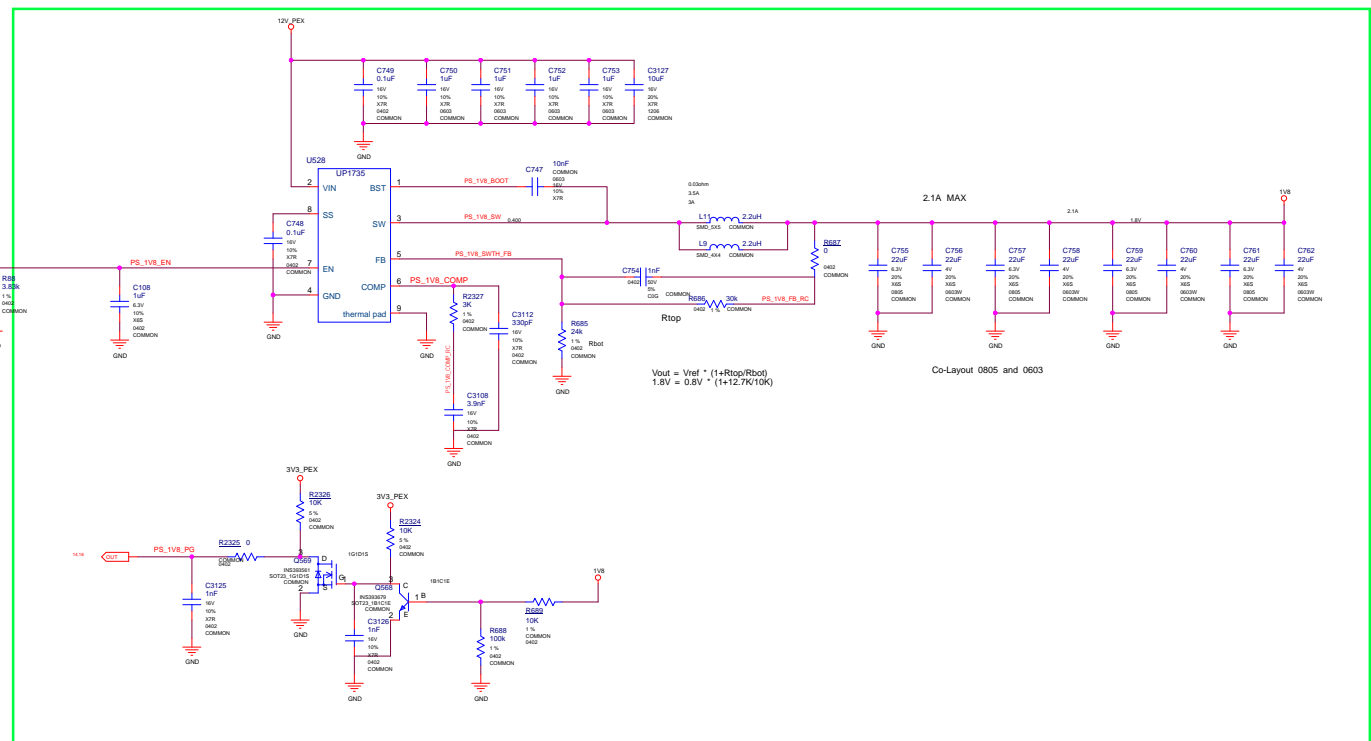
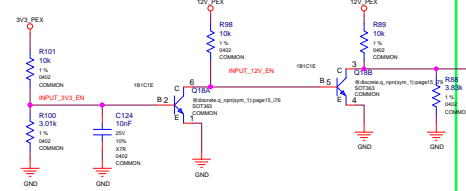
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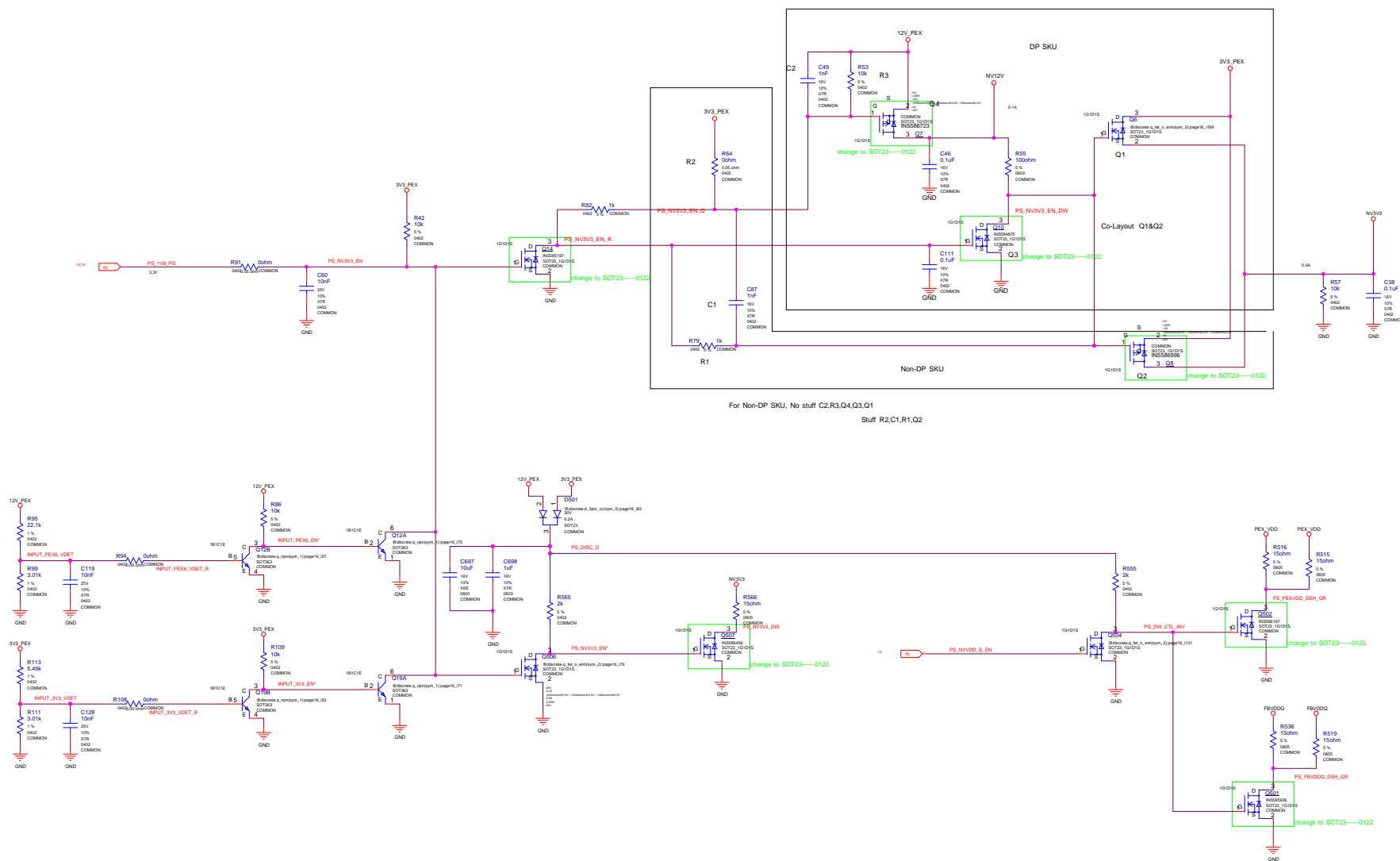


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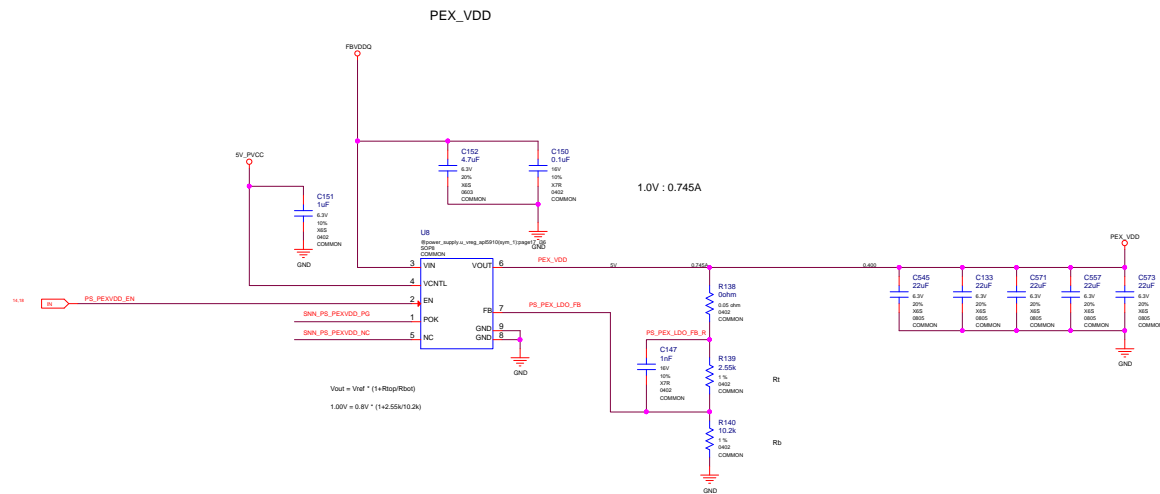
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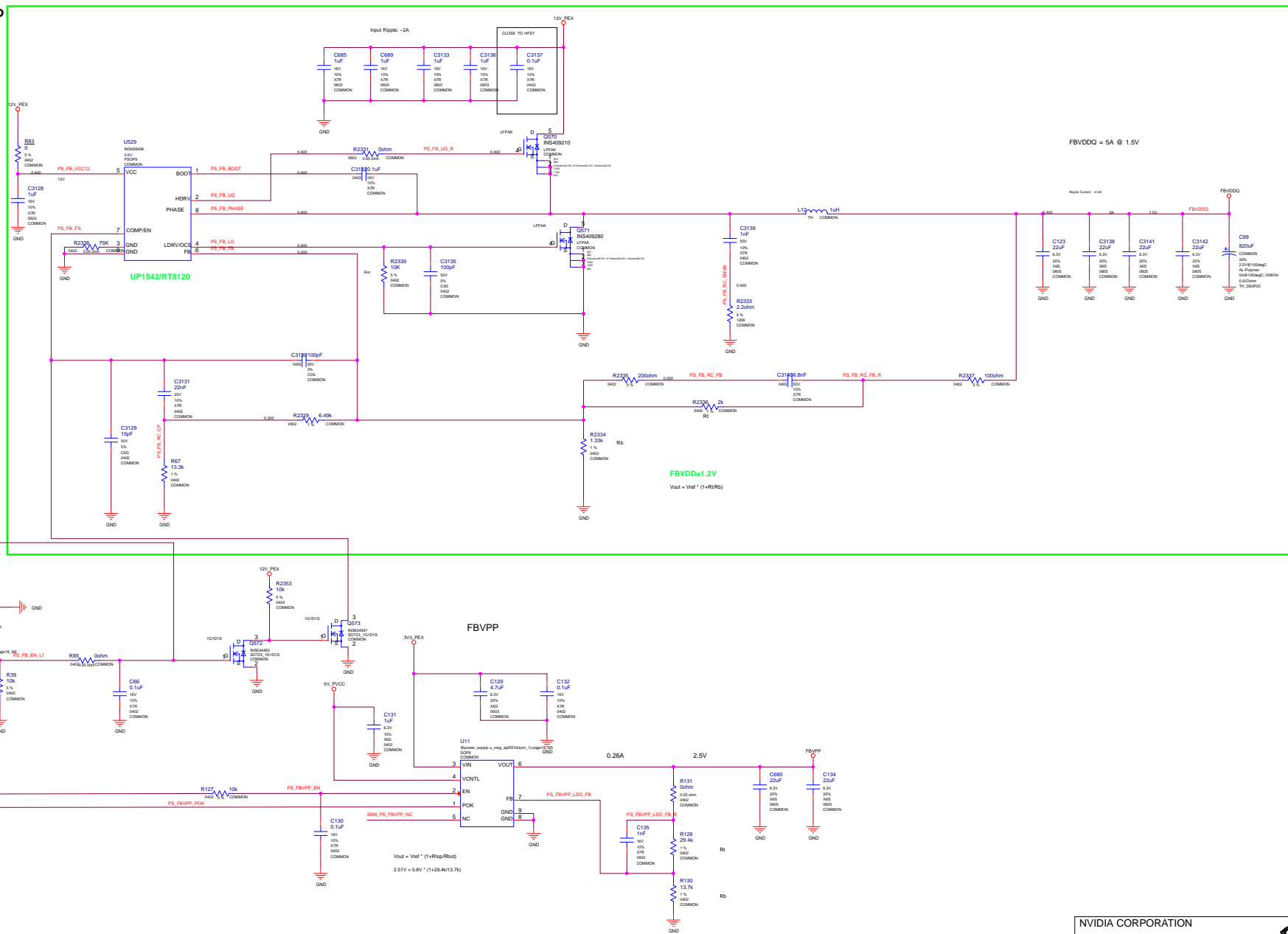
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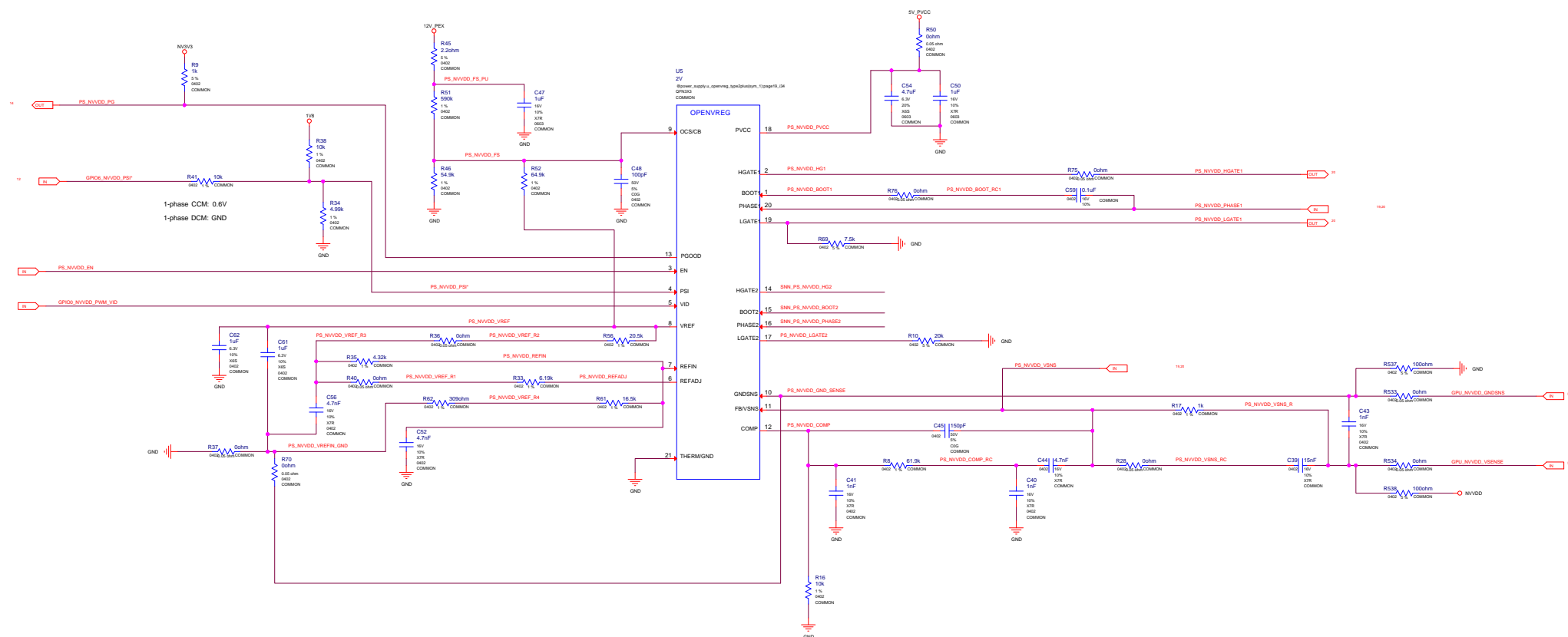


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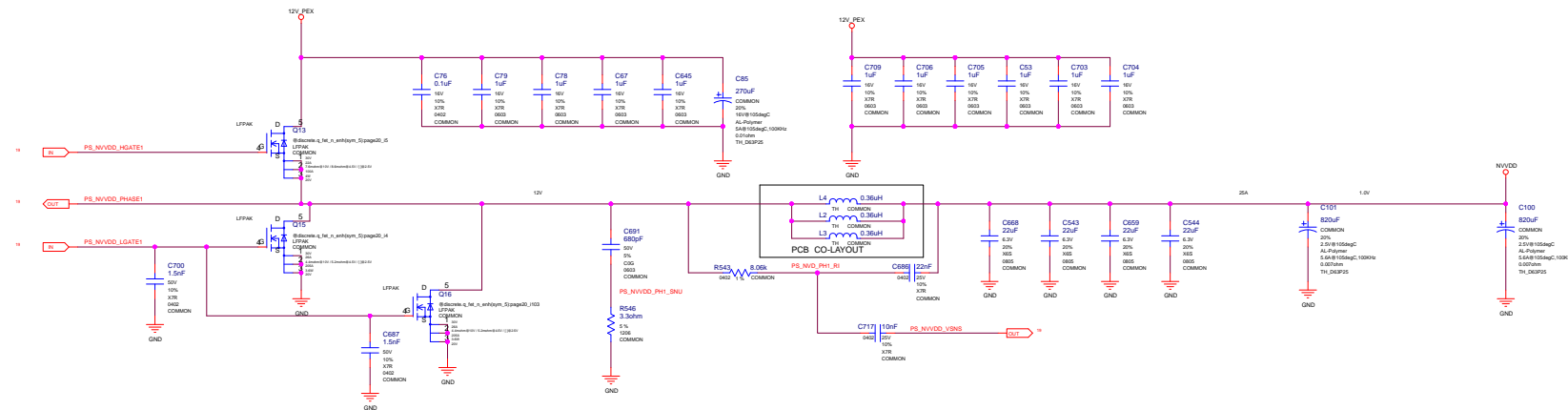
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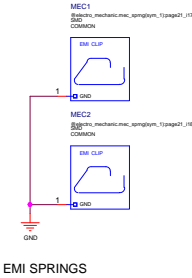
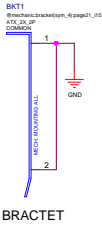
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Mechanical



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