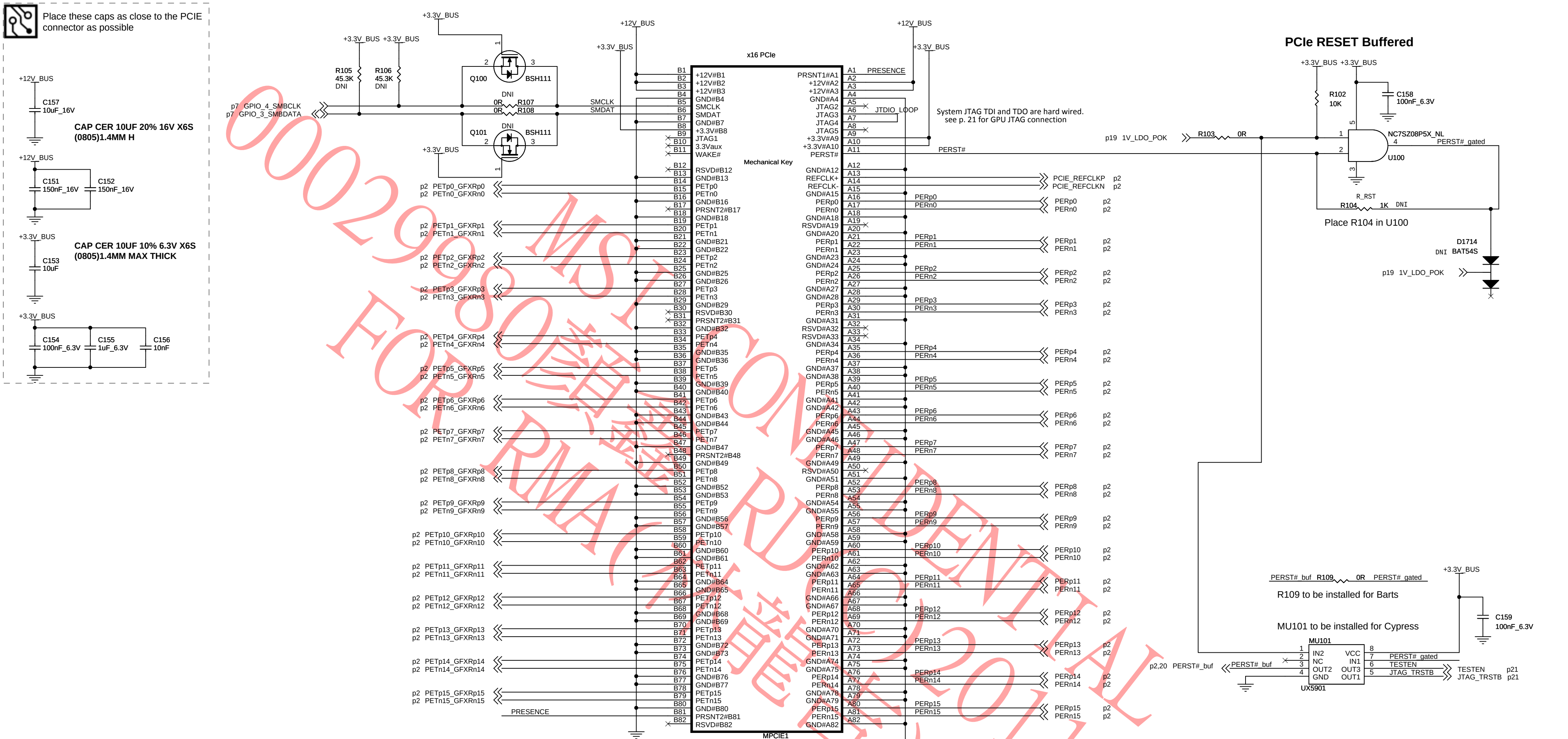
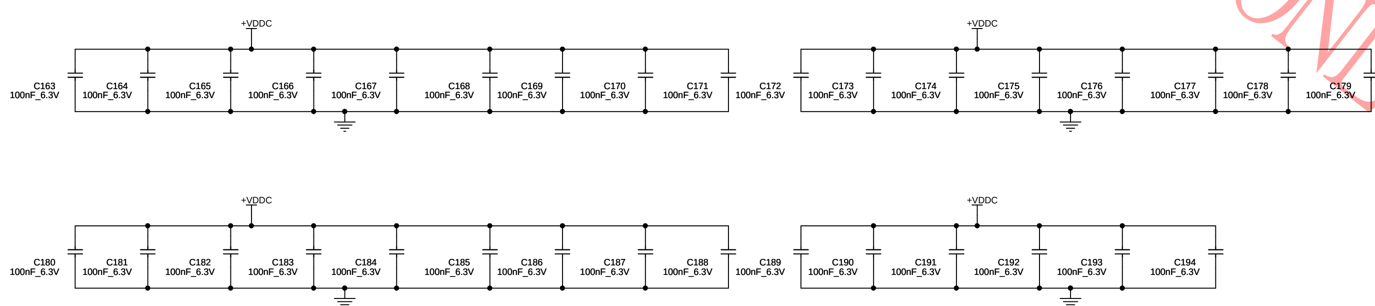
PCI-EXPRESS EDGE CONNECTOR



PCIe stitching caps: To be placed close to the PCIe diff pair routed on Layer 6 at the PCIe slot



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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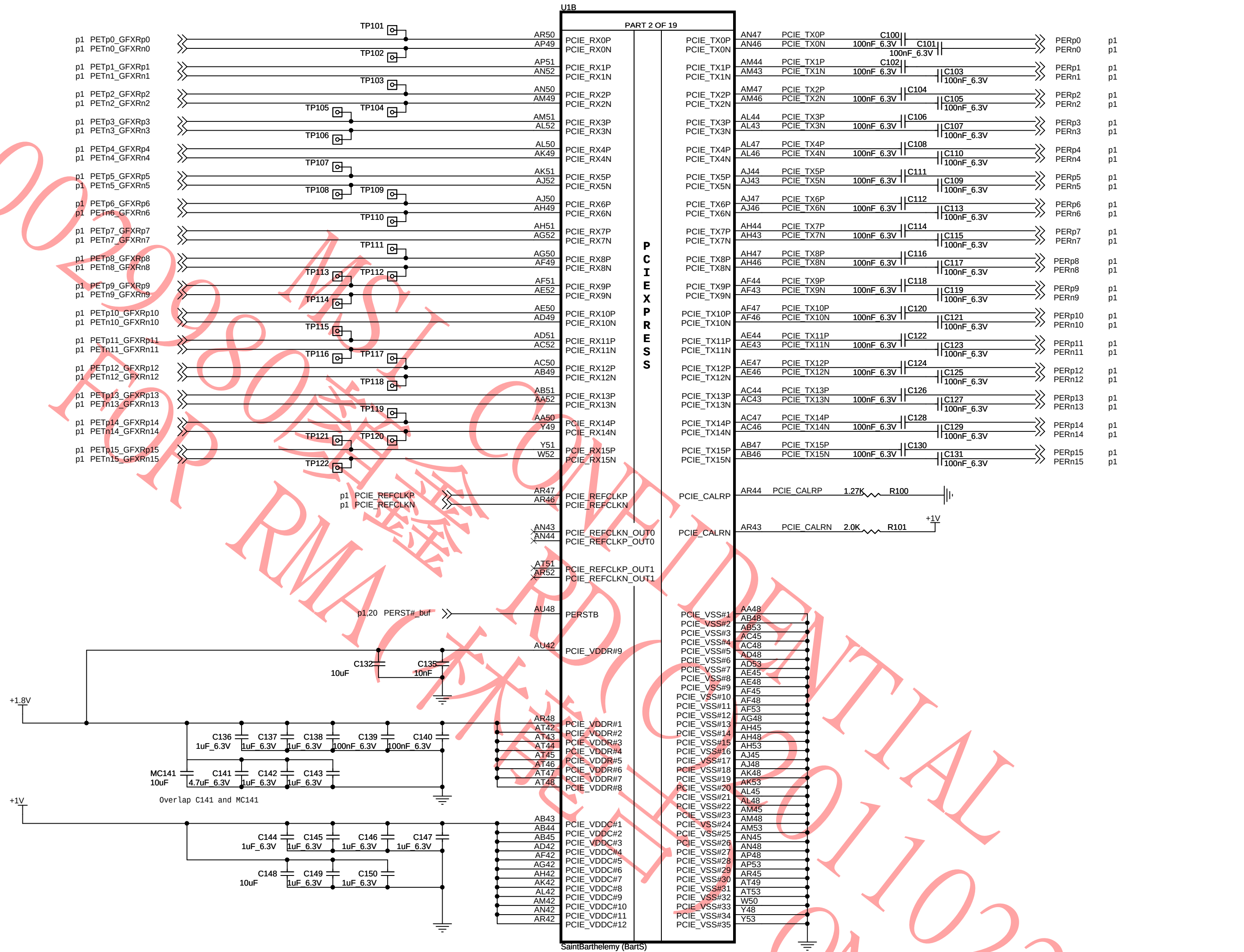
Title PCIE EDGE CONNECTOR
Doc No. 105-C220XX-00

(2) BARTS/CYPRESS PCIE Interface

NOTE: Some of the PCIE testpoints will
be available through vias on traces.



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Title ASIC PCIE Interface

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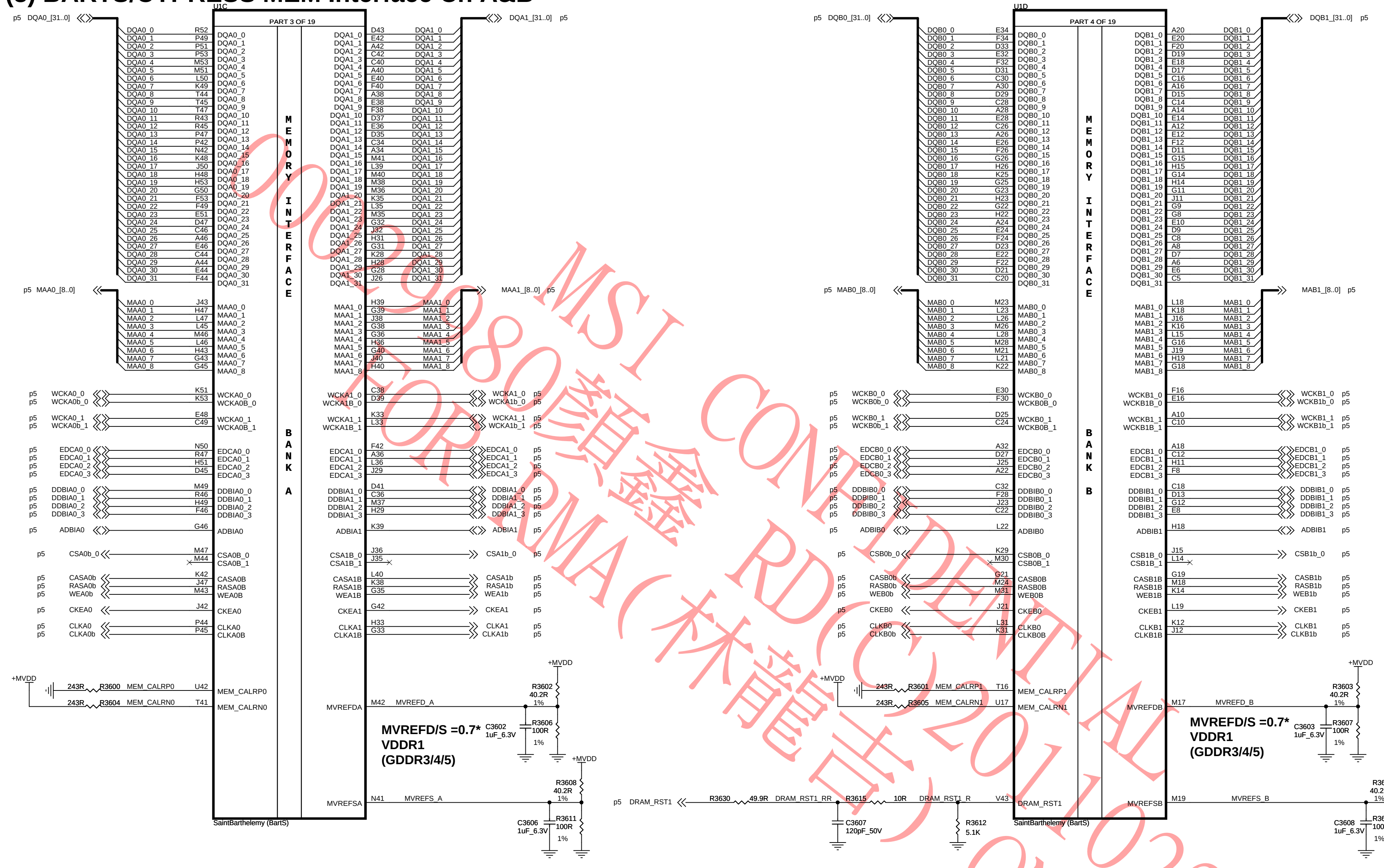
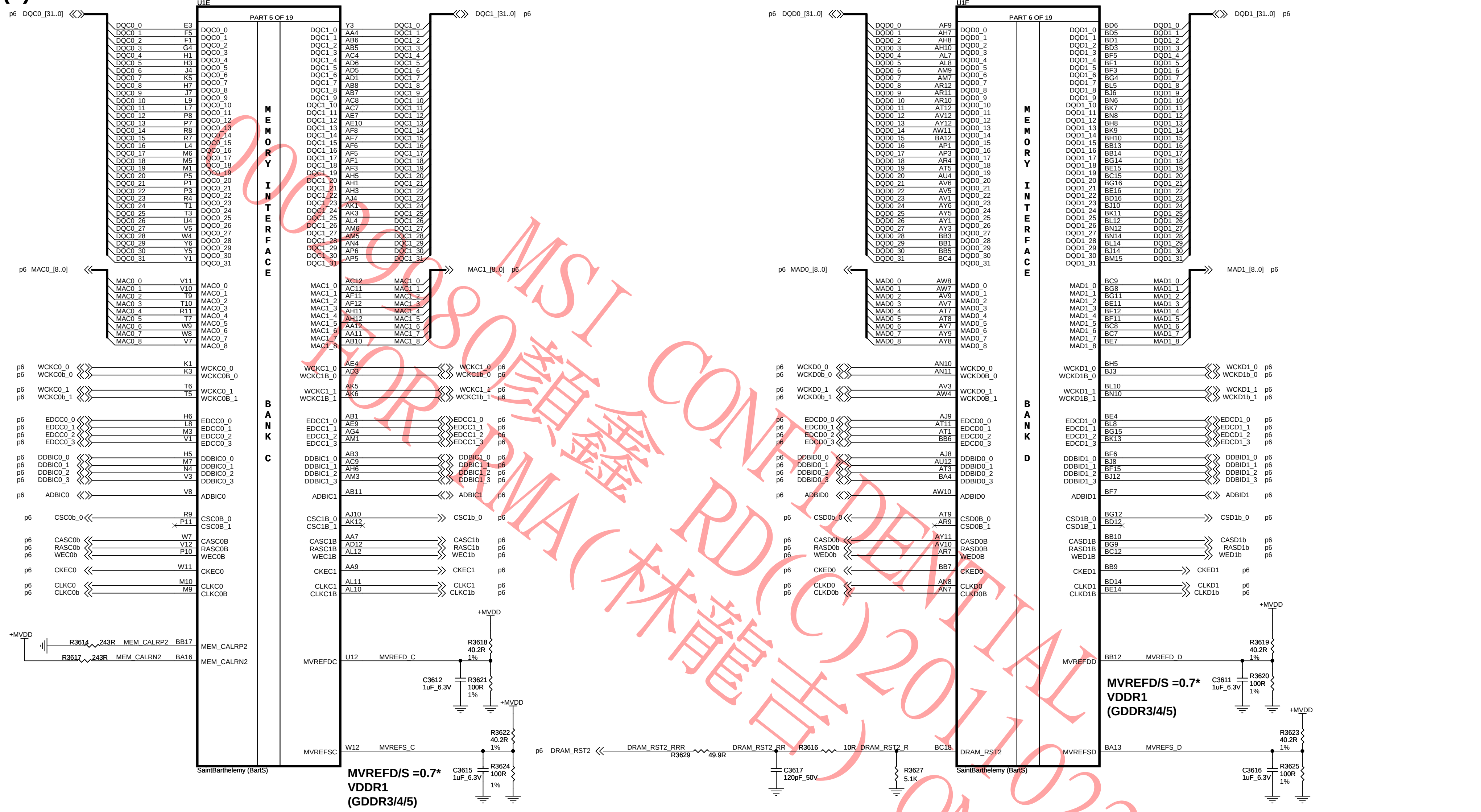
(3) BARTS/CYPRESS MEM Interface Ch A&B



(4) BARTS/CYPRESS MEM Interface Ch C&D



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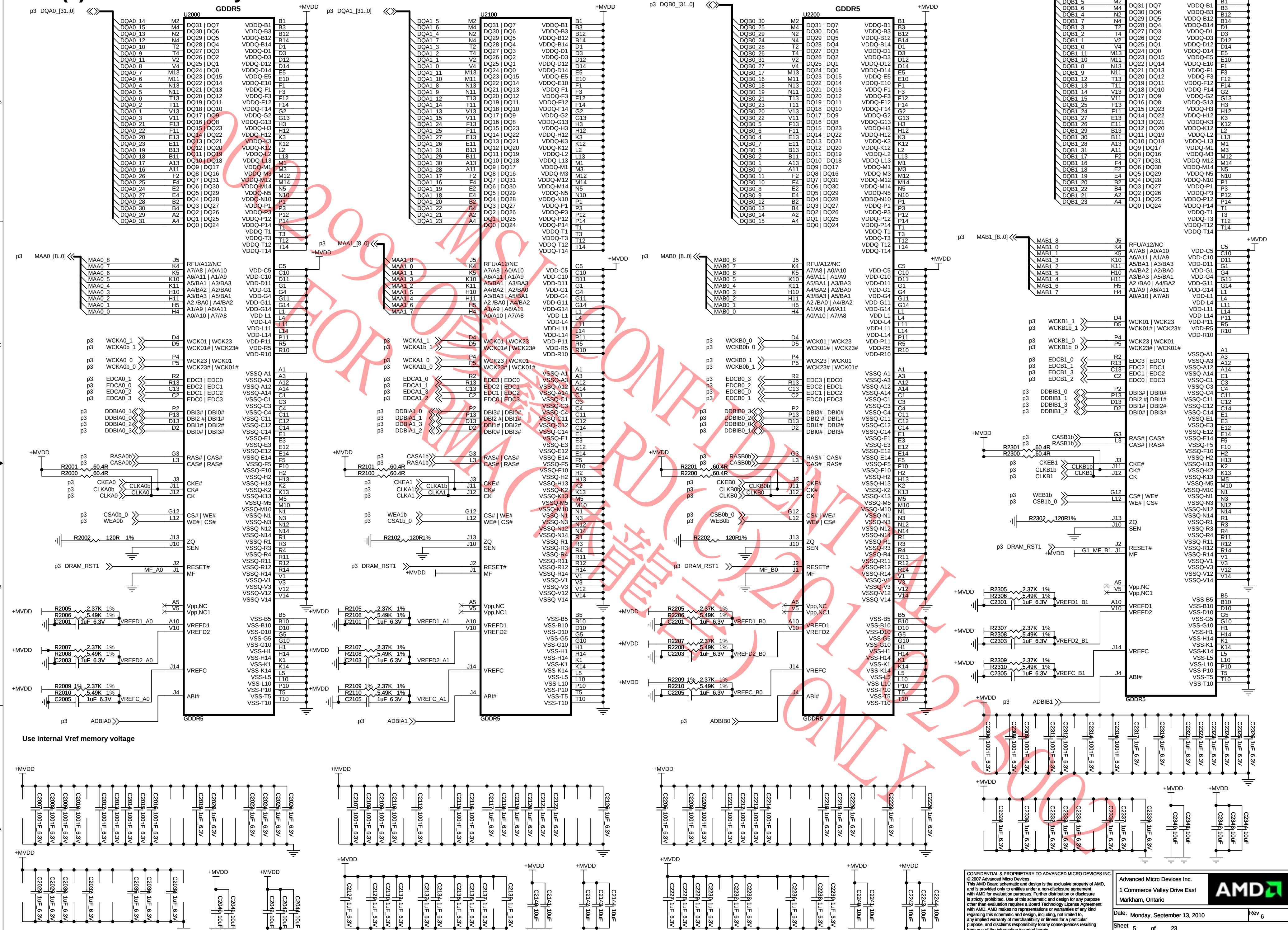
Title ASIC Memory Ch C & D	Doc No. 105-C220XX-00

(5) GDDR5 Memory Channel A&B



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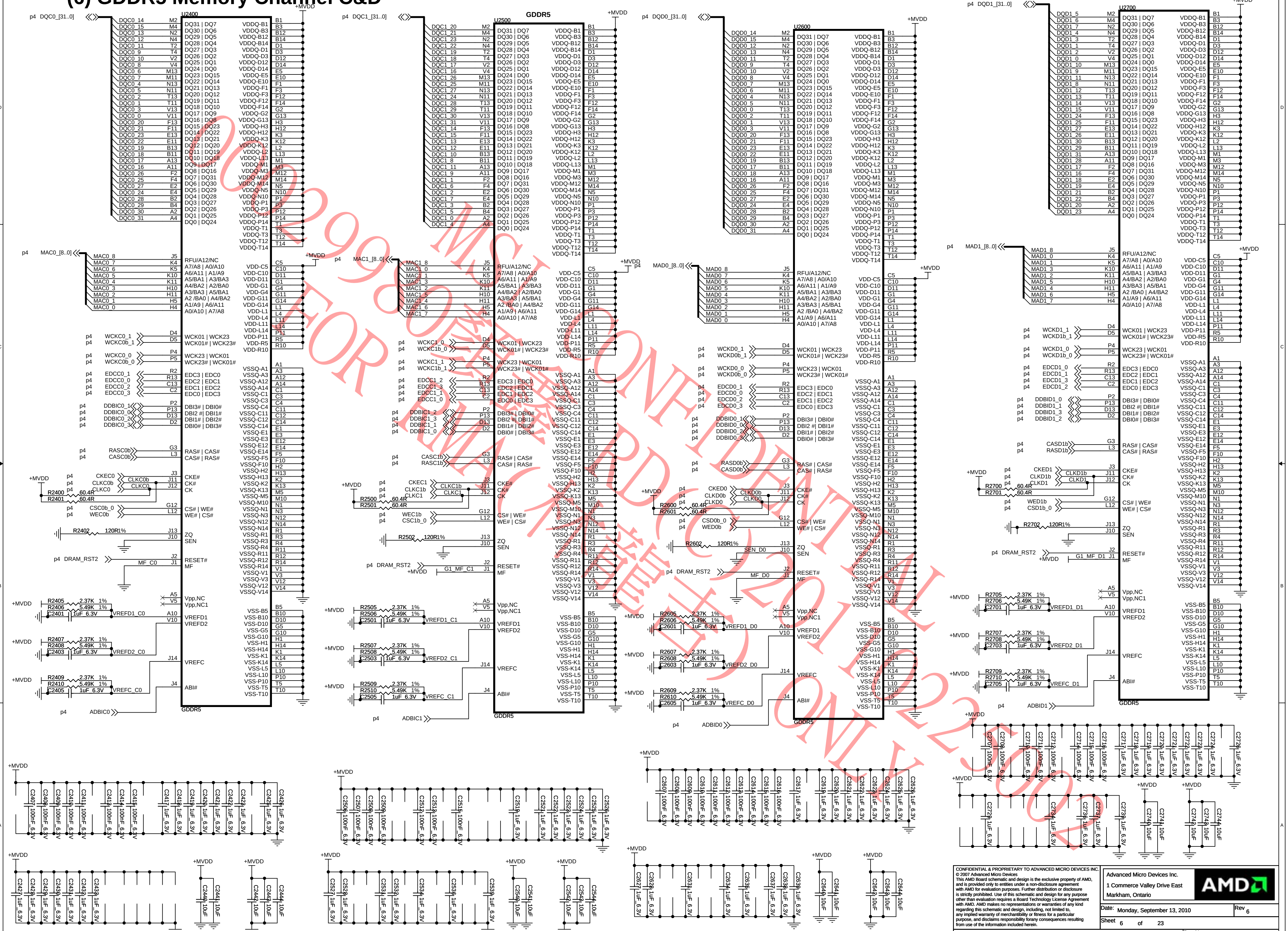
Title GDDR5 Ch A & B | Doc No. 105-C220XX-00

(6) GDDR5 Memory Channel C&D



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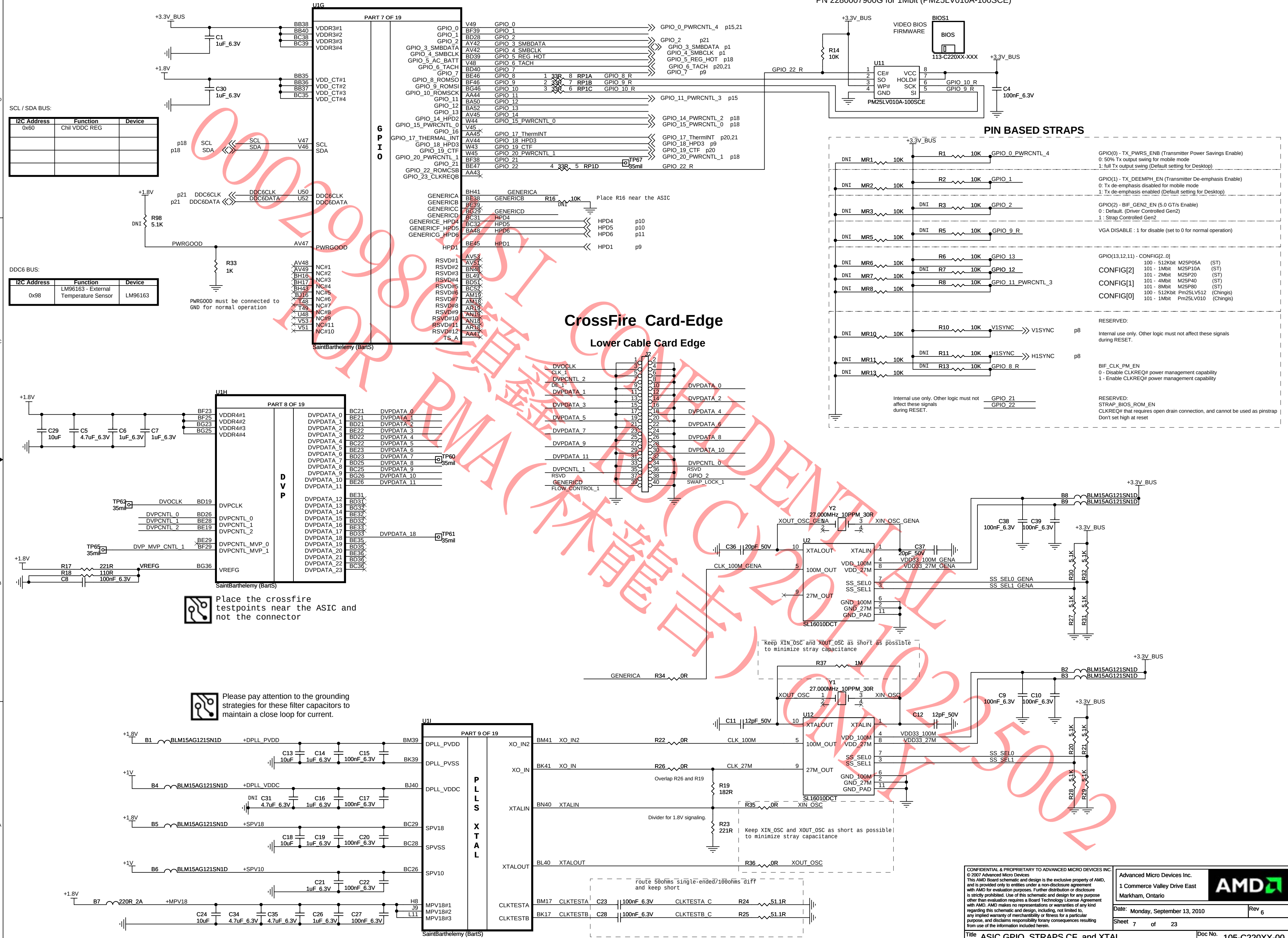
Title GDDR5 Ch C & D	Doc No. 105-C220XX-00

(07) BARTS/Cypress GPIOs Strap CF XTAL OSC



SCL / SDA BUS:

I2C Address	Function	Device
0x60	Chil VDDC REG	

DDC6 BUS:

I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

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Title: ASIC GPIO, STRAPS,CF, and XTAL
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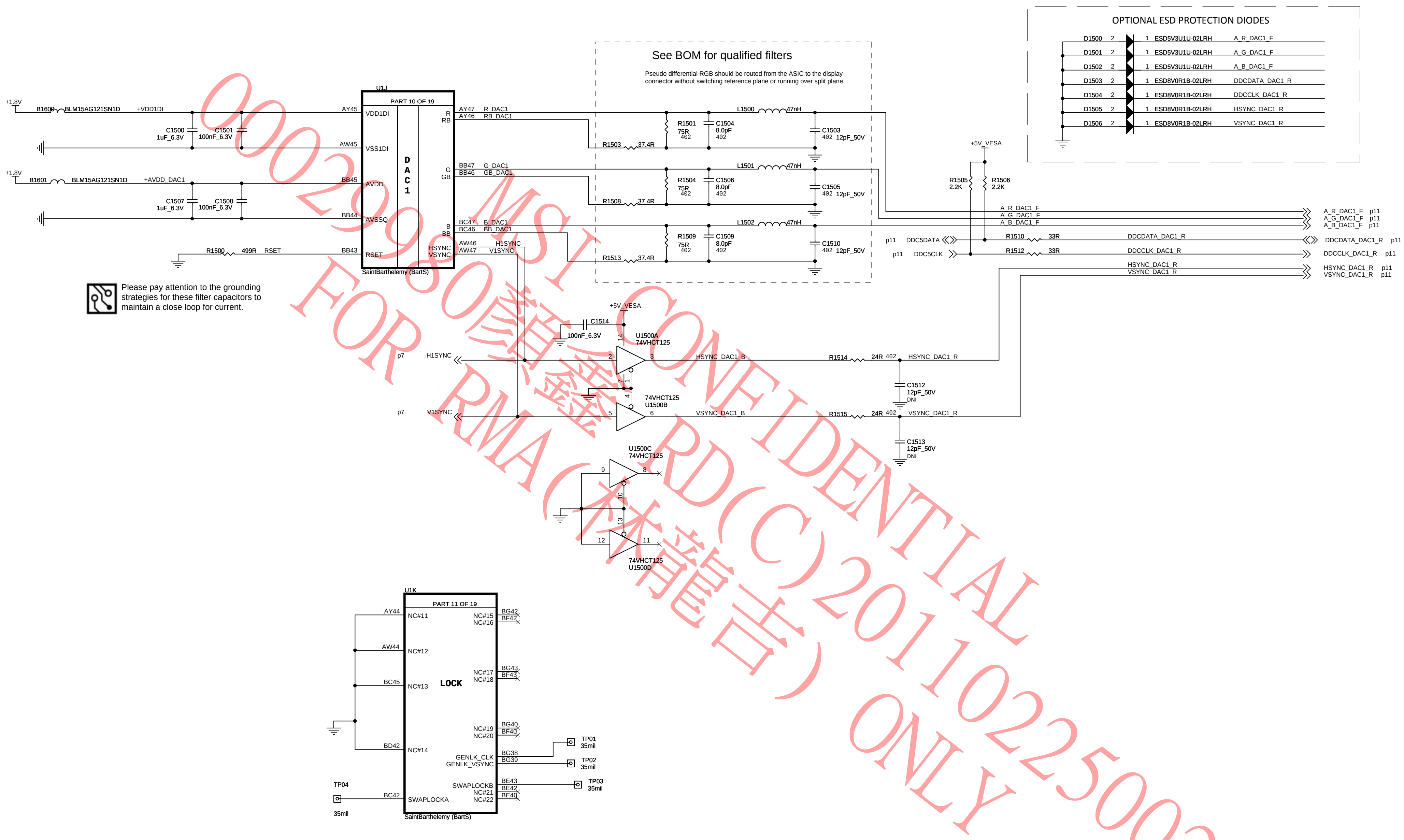
(08) BARTS/CYPRESS DAC1



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Title ASIC DAC1	Doc No. 105-C220XX-00

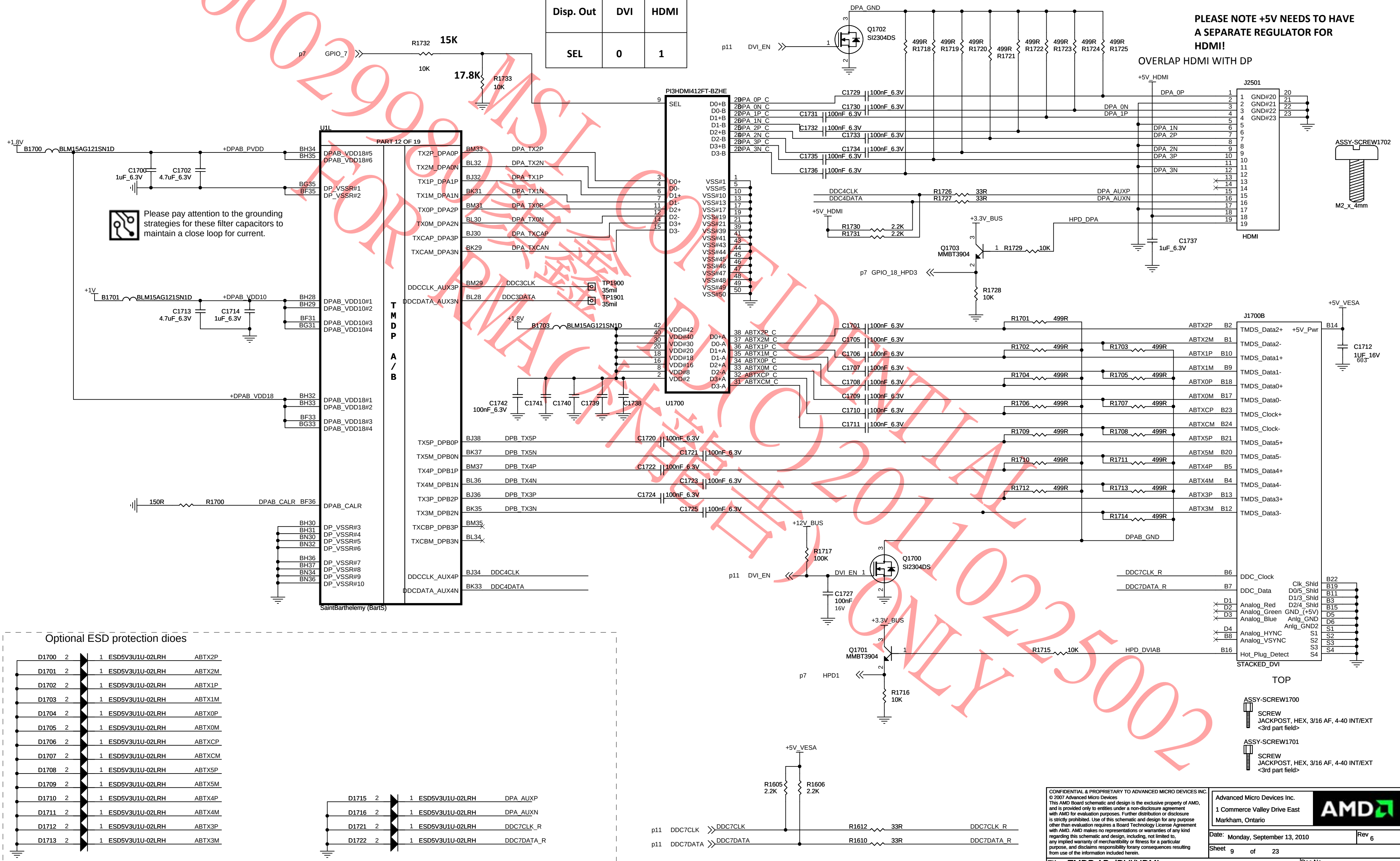
(09) BARTS/CYPRESS Top dDVI/HDMI

HDMI/DVI MUX:
0.1uF cap to be used, placed close to VDD power pins
Place 1x to top and 1x to bottom of the package
Use 5 ground vias for the ground pad: 1 via at each corner of the ground pad and 1 in the center of the ground pad
TDFN package to be used: 2600009800G
SEL is 1.8V only

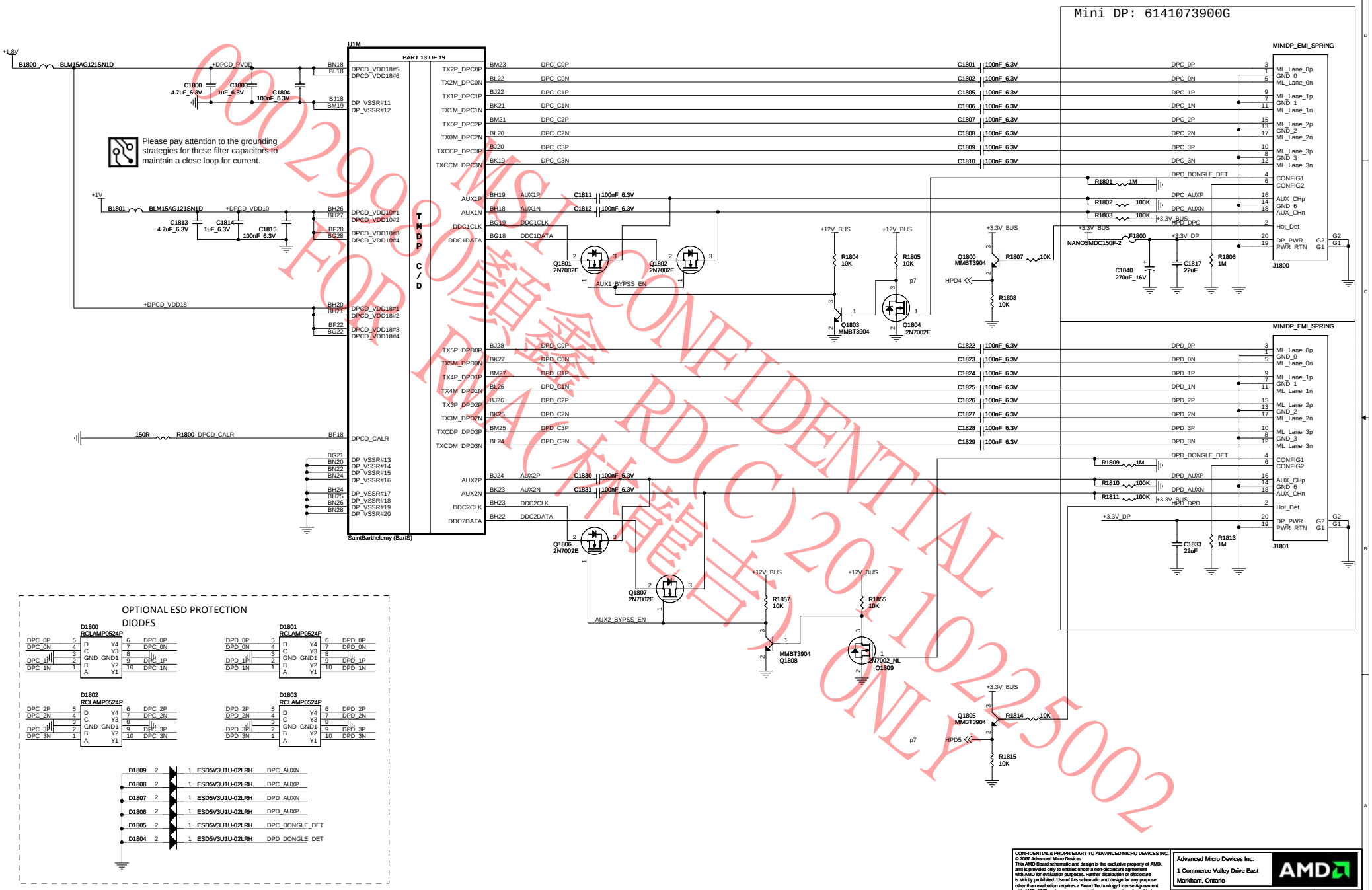
Disp. Out	DVI	HDMI
SEL	0	1

PLEASE NOTE +5V NEEDS TO HAVE A SEPARATE REGULATOR FOR HDMI!!

OVERLAP HDMI WITH DP



(10) BARTS/CYPRESS C&D mDP mDP



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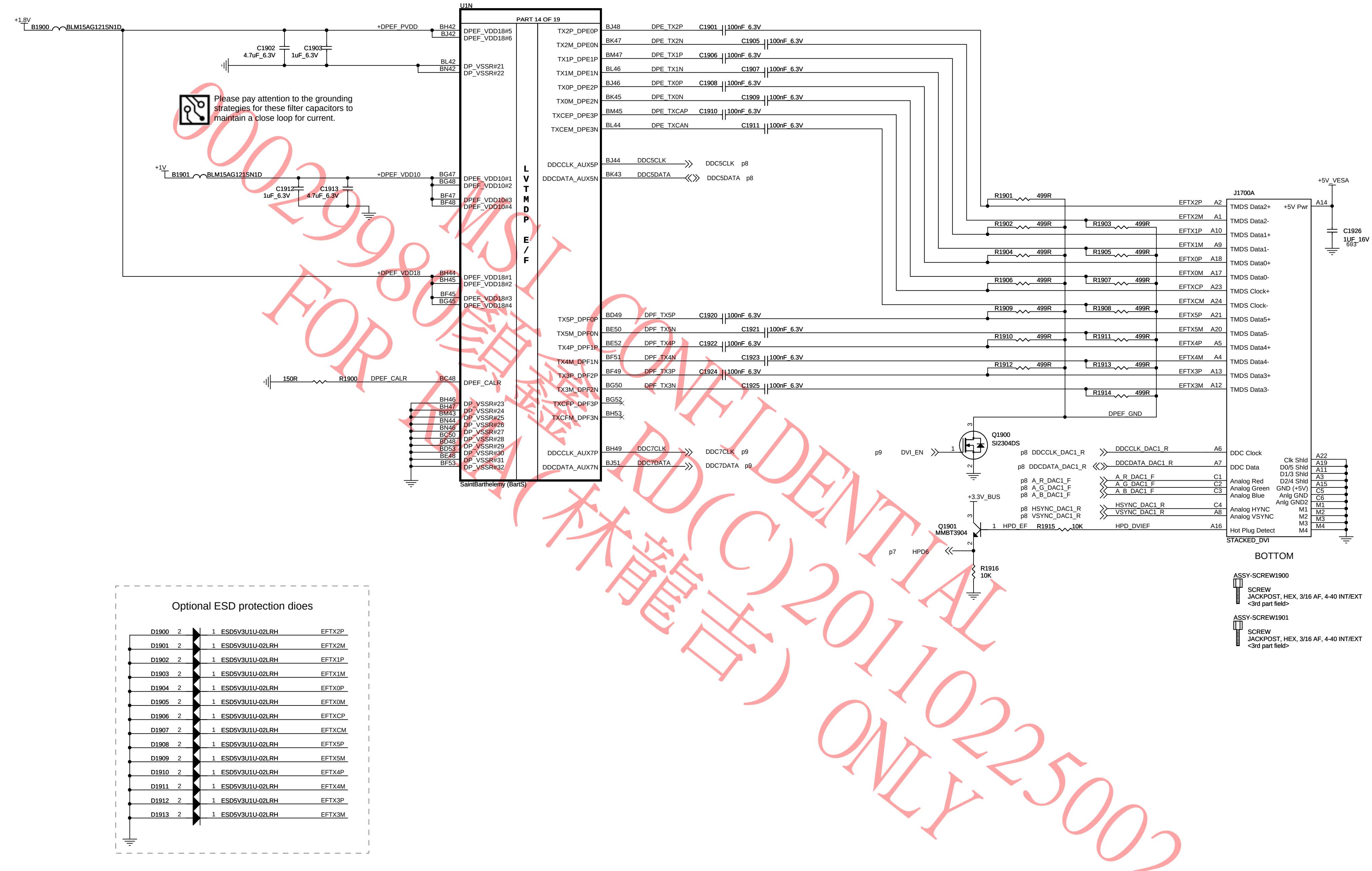
Title	TMDP CD mDP mDP
Doc No.	105-C220XX-00

(11) BARTS/CYPRESS E&F Bottom dDVI



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Title TMDS EF dDVI

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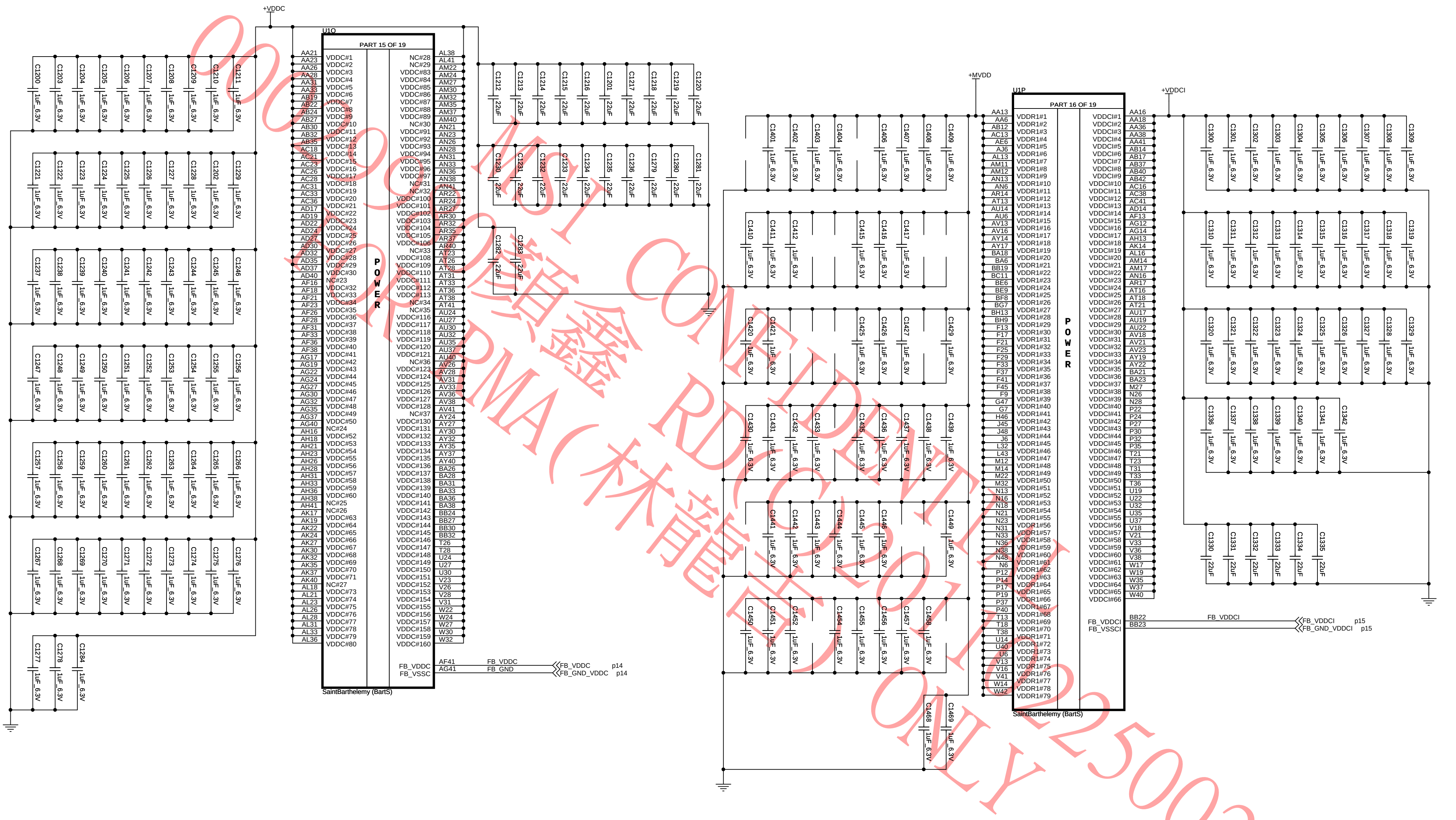
(12) BARTS/CYPRESS Power



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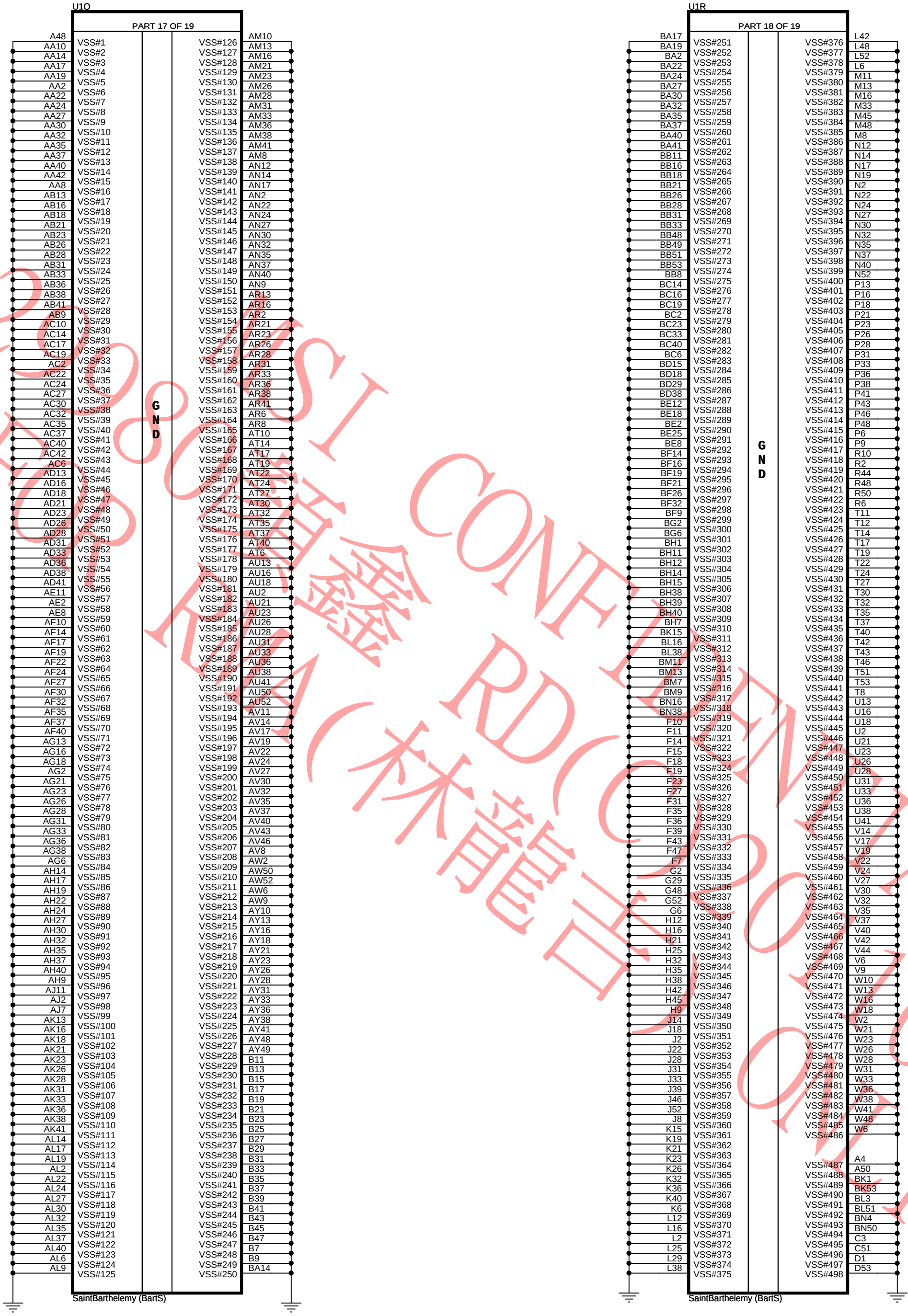
Title ASIC POWER | Doc No. 105-C220XX-00

(13) BARTS/CYPRESS GND



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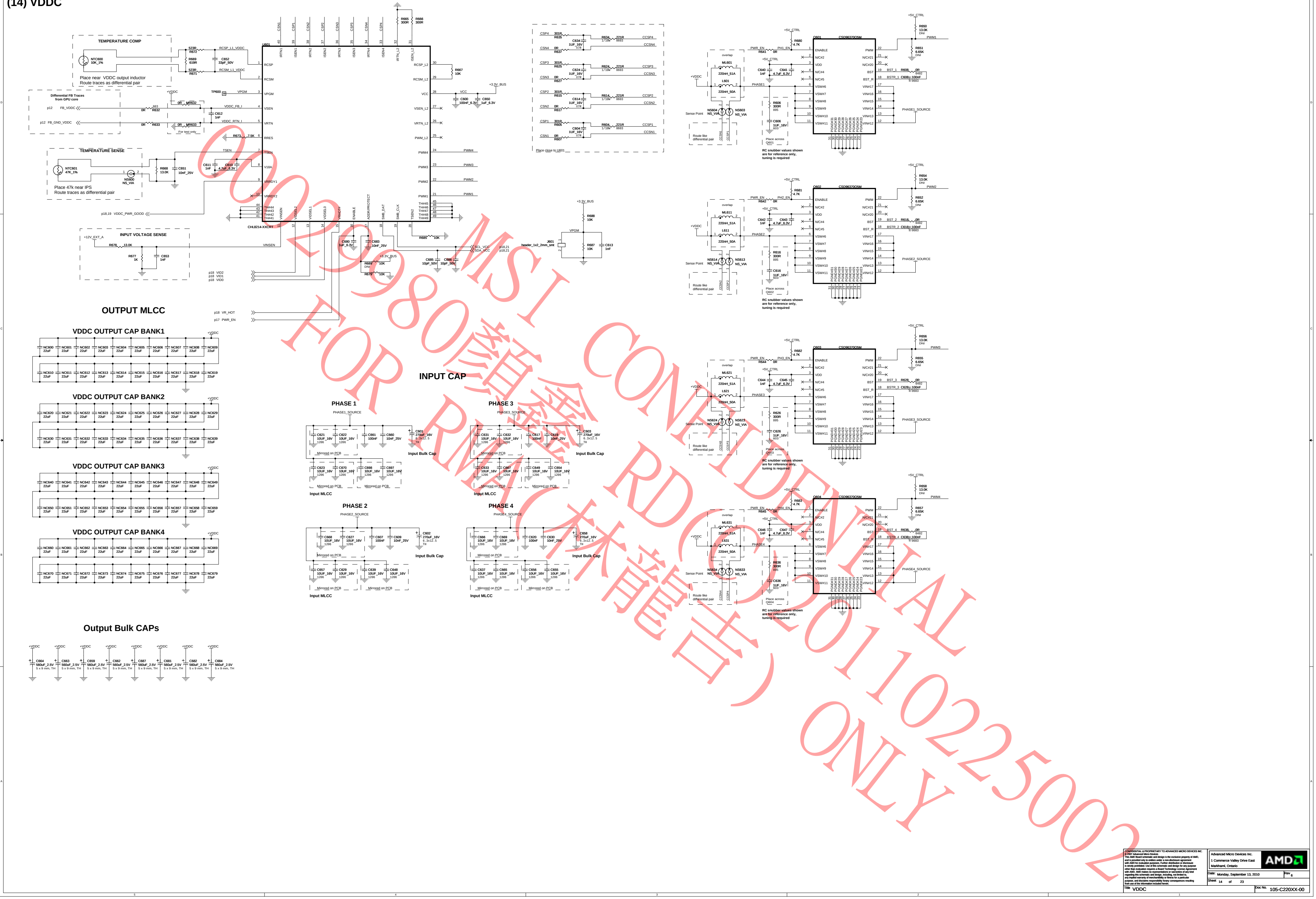
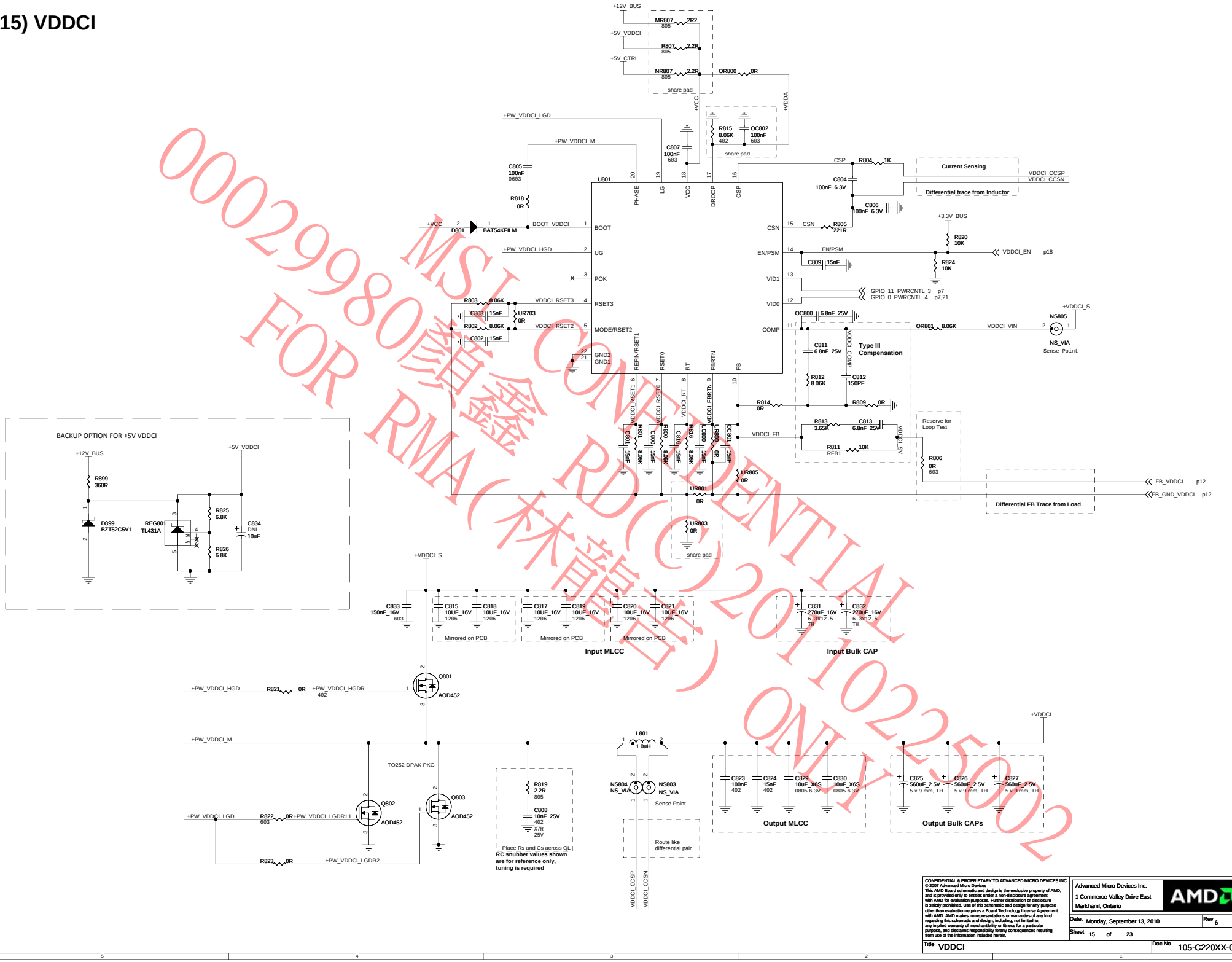
Title ASIC GND	Doc No. 105-C220XX-00

(14) VDDC



(15) VDDCI



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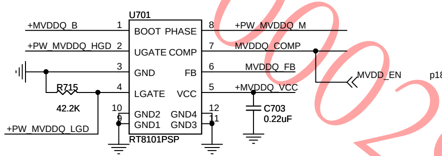
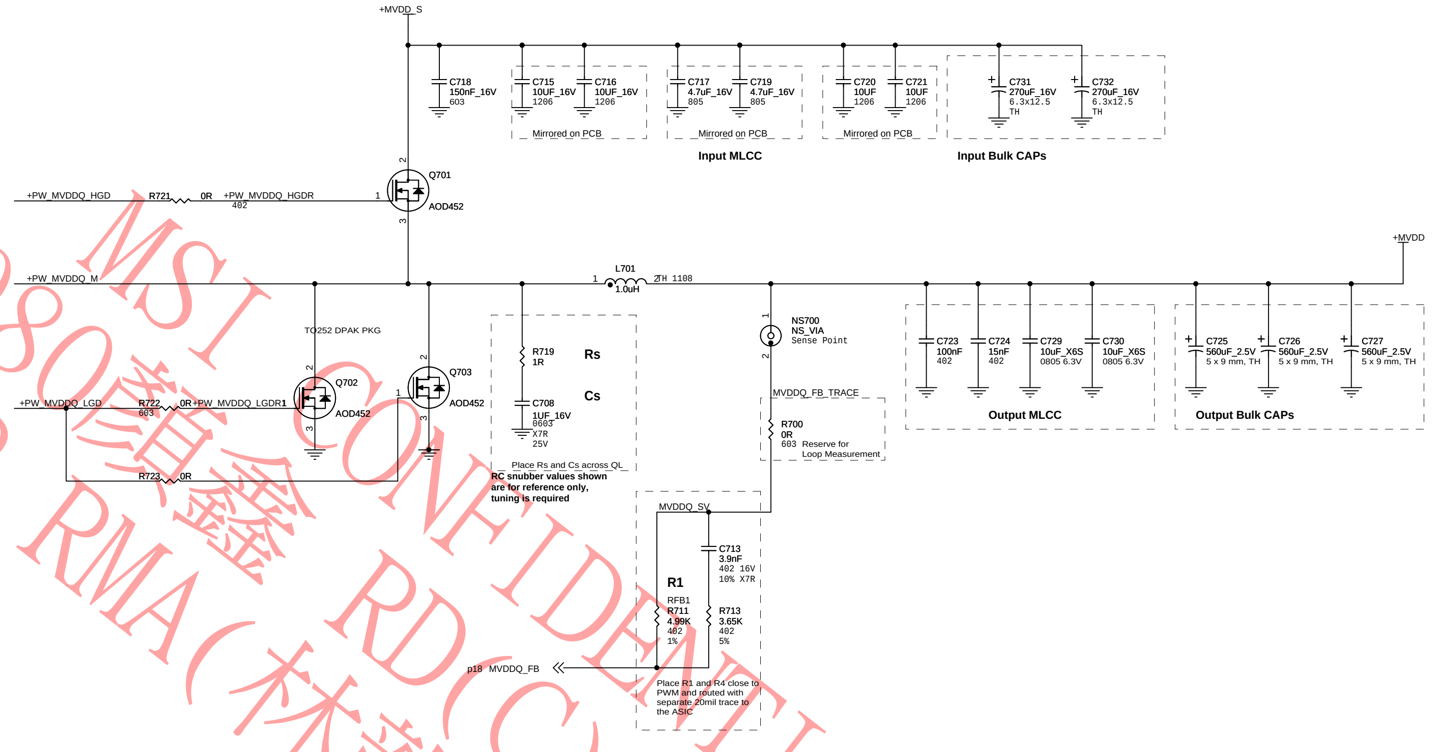
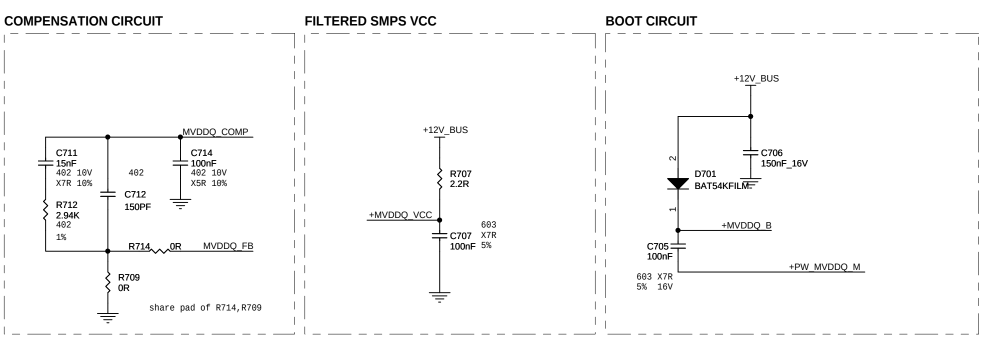
(16) MVDD





Layout guideline

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



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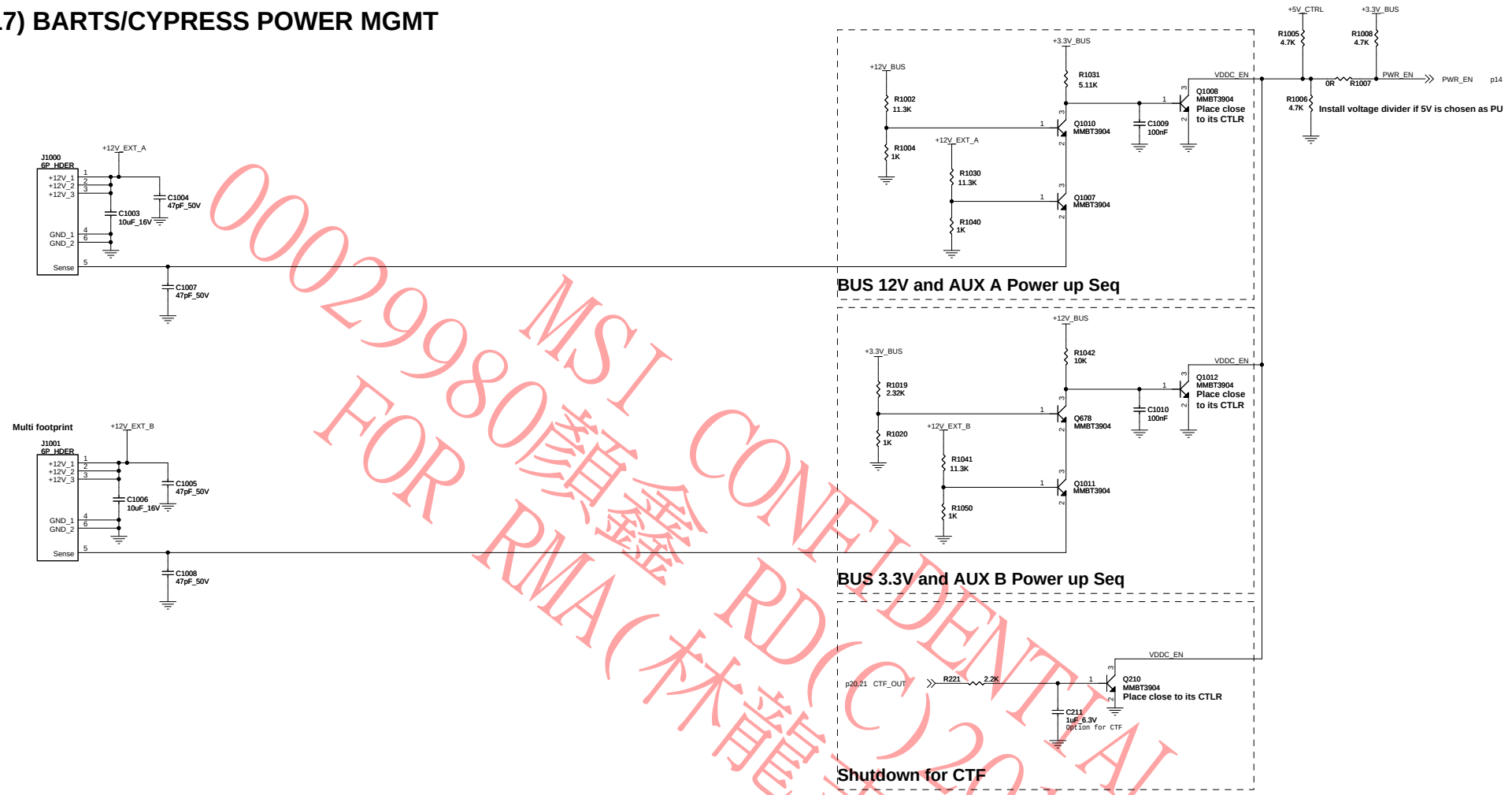
(17) BARTS/CYPRESS POWER MGMT



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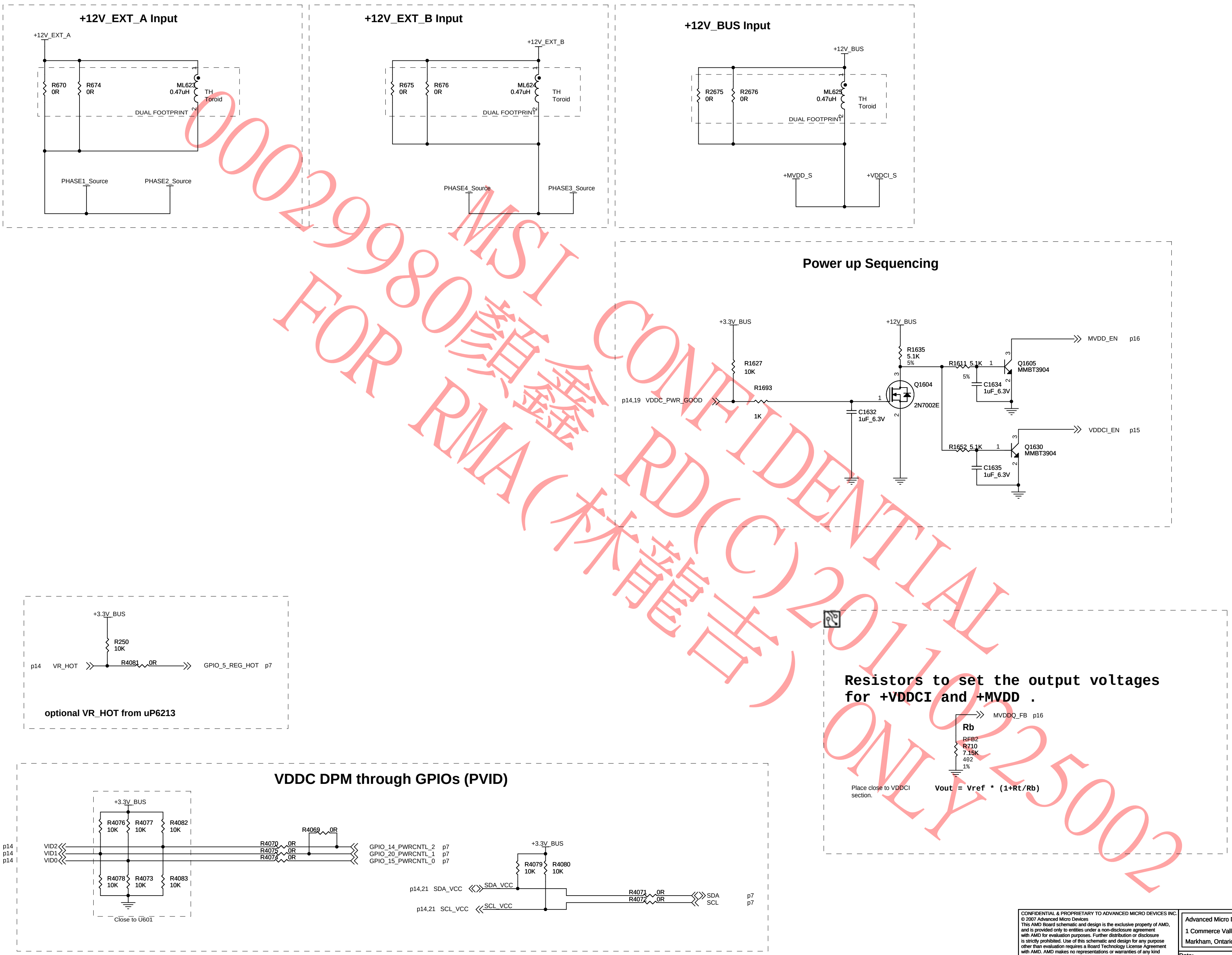
Title Power Management 1	Doc No. 105-C220XX-00

(18) BARTS/CYPRESS PWR MGMT 2



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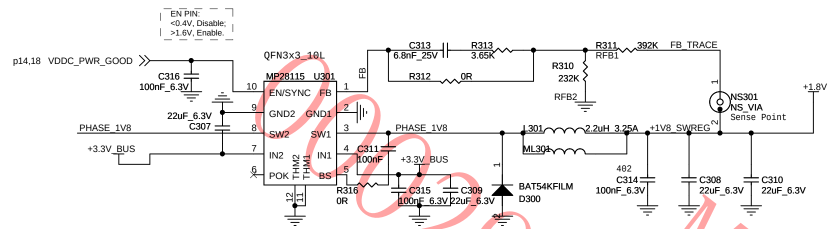
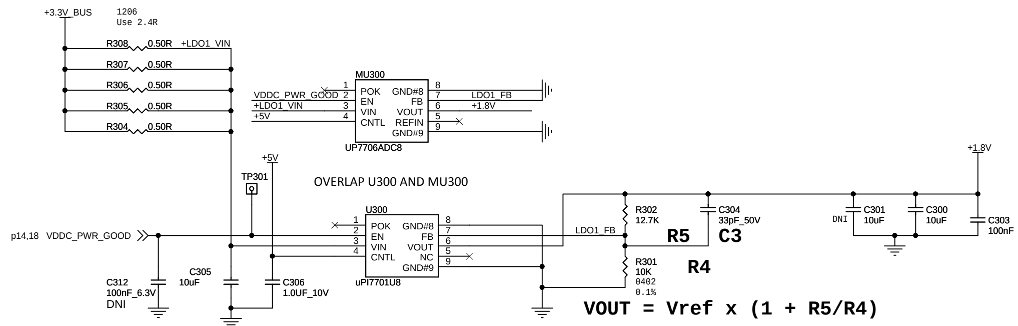
Title: Power Management 2 | Doc No. 105-C220XX-00

(18) BARTS/CYPRESS Small Rail Regulators

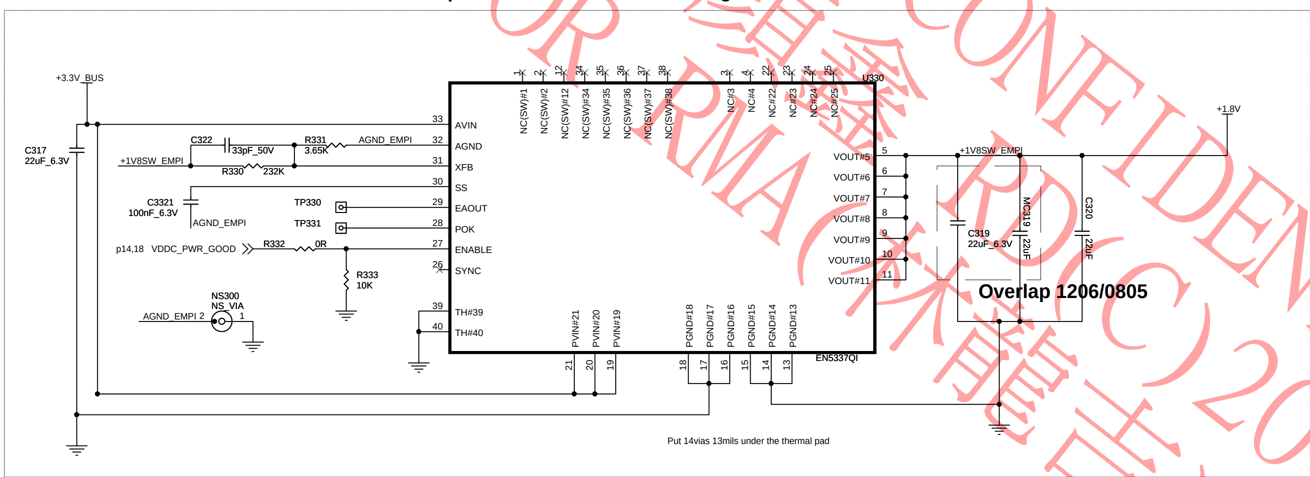
LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

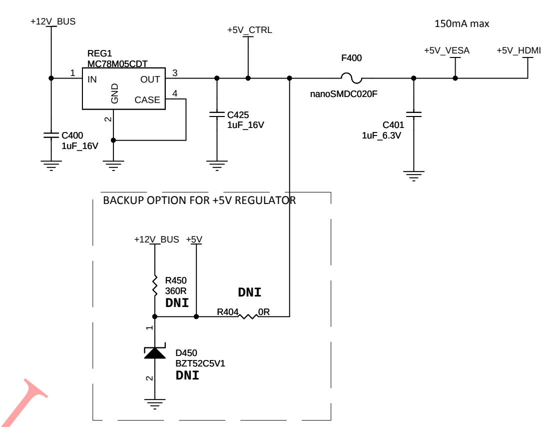




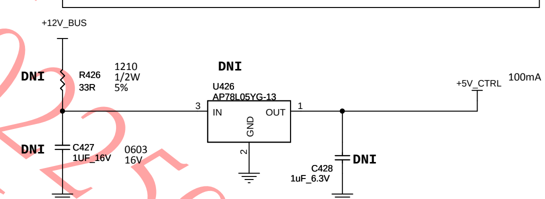
Regulators for +5V, +5V_VESA and +5V_HDMI
Iout max = 150mA (DVI+HDMI)

Other cheaper solution at 5MHz switching for 1.8V



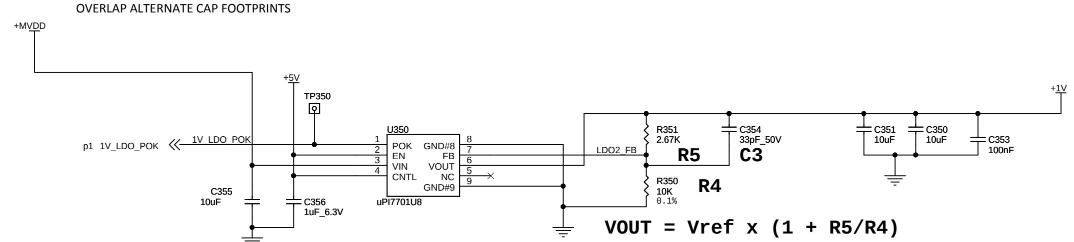


optional 5V power for VDDC regulator;



LDO #2: Vin = +1.35V to 1.8VMAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

OVERLAP ALTERNATE CAP FOOTPRINTS



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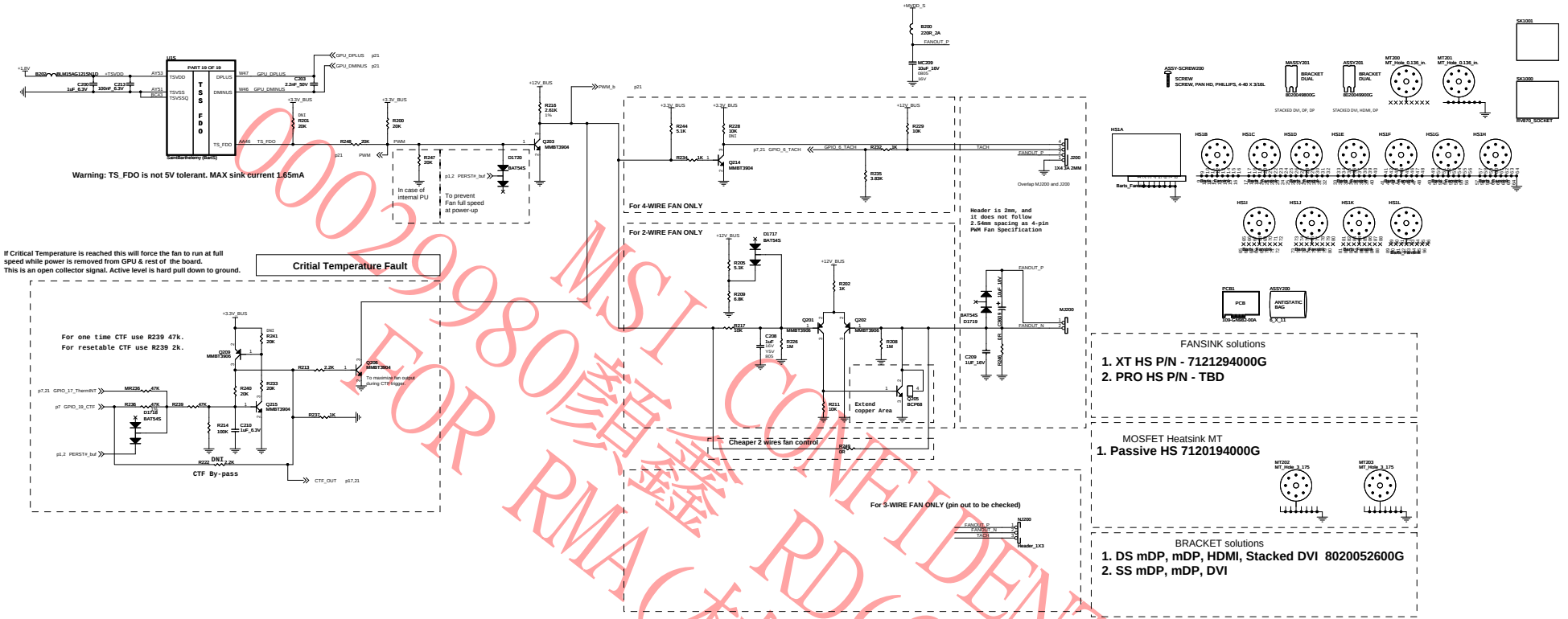
(20) BARTS/CYPRESS Mechanical and Thermal Management



FANSINK solutions

1. XT HS P/N - 7121294000G
2. PRO HS P/N - TBD

MOSFET Heatsink MT

1. Passive HS 7120194000G

BRACKET solutions

1. DS mDP, mDP, HDMI, Stacked DVI 8020052600G
2. SS mDP, mDP, DVI

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Title: Mechanical & Thermal Management

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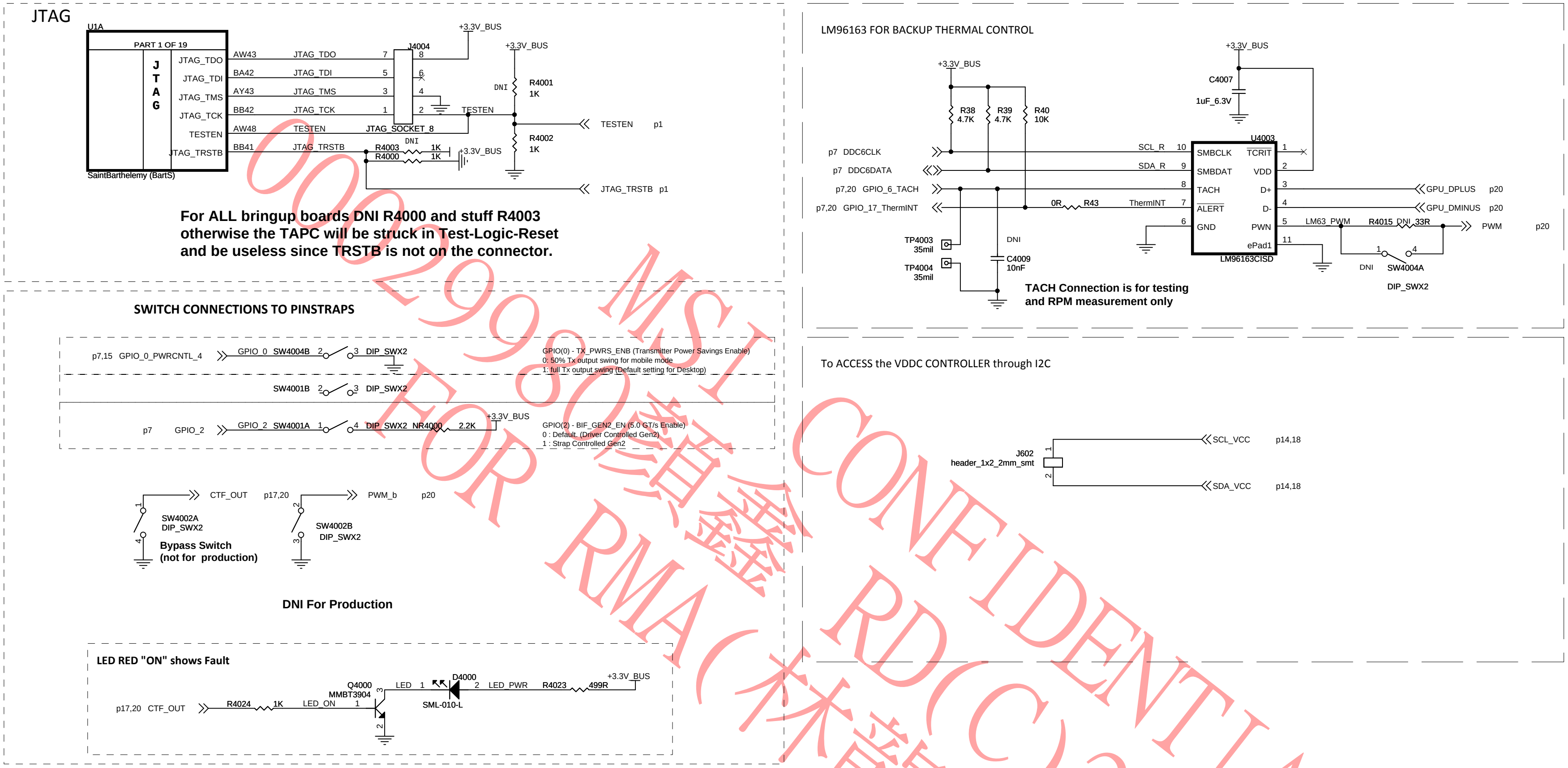
(21) BARTS/CYPRESS Debug Circuits



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Title	Debug Circuits
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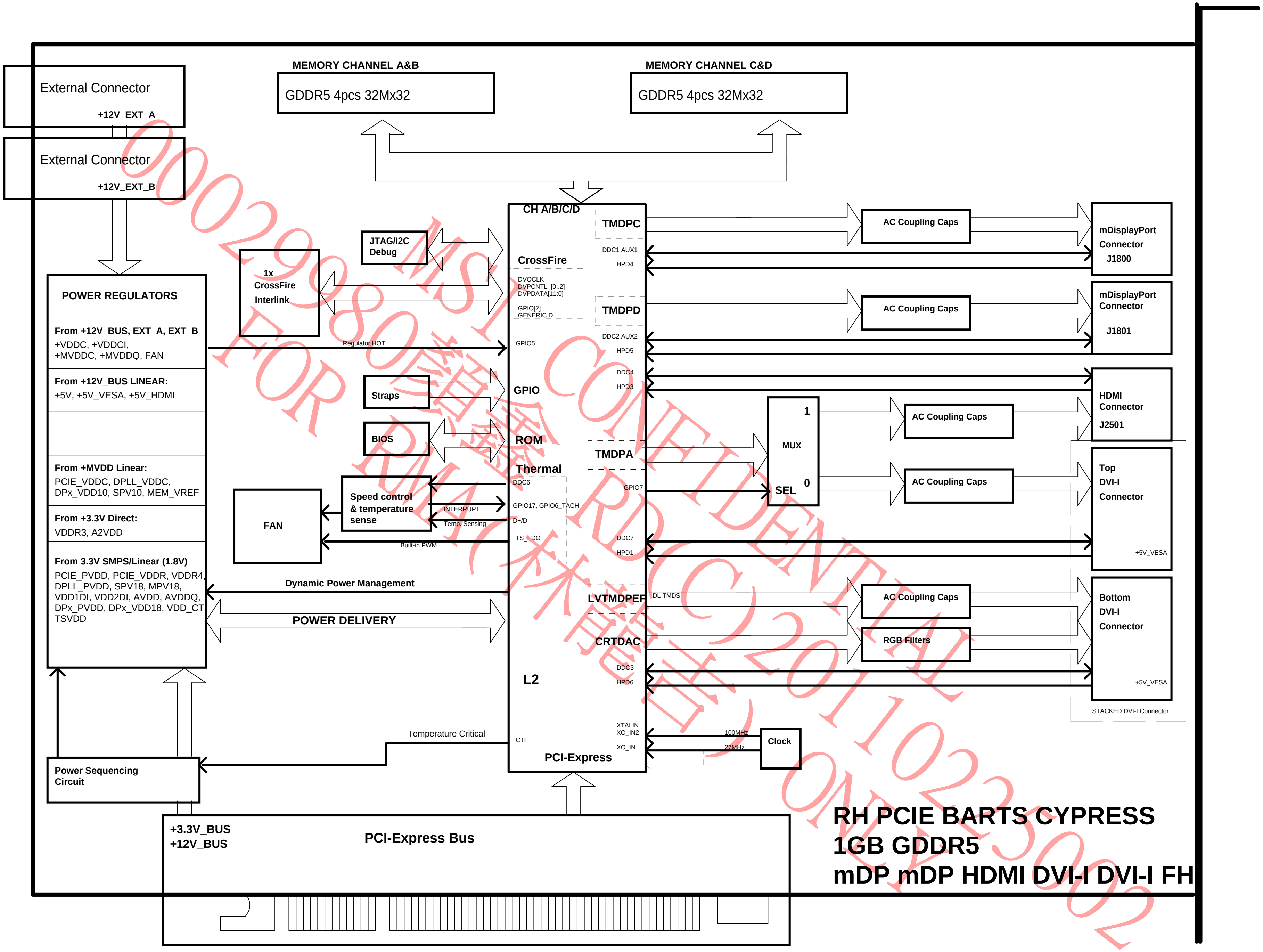

RH PCIE BARTS CYPRESS
1GB GDDR5
mDP mDP HDMI DVI-I DVI-I FH

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Title	Block Diagram	Doc No.	105-C220XX-00

Title	Schematic No.	Date:
RH BARTS CYPRESS GDDR5 mDP-mDP-HDMI-DVII-DVII	105-C220XX-00	Monday, September 13, 2010

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 6

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	10/04/2010	Initial release. Based on DB111
1	00B	09/08/2010	Page01: Added direct connection from Pull-Up for MU101 for Cypress Page14: update Q601,Q602,Q603,Q604 symbol Page17: add C211 Page20: add R201, R237, R241 Page50: update block diagram