P690: GT218, DDR3 MEMORY 64MX16/32MX16

Page 1: P690 Overview

Page 2: PCI Express Interface

Page 3: Frame Buffer Interface

Page 4: DDR3 Memories

Page 5: DAC A Slim VGA

Page 6: DAC B VGA Header

Page 7: TMDS Interface

Page 8: HDMI Connector

Page 9: IFPD, IFPE Interface, Fan, Mechanical

Page 10: XTAL, ROM, SPDIF, JTAG

Page 11: Thermal Protection, IFP_IOVDD, Straps

Page 12: Power Supply I: FBVDD/Q, PEX_VDD, 5V, 3V3_F

Page 13: Power Supply II: PLLVDD, NVVDD

V183 2.0 pcb change list

Page 2：Add EC1802 for 12V_PEX use , G1.E15 pin NC

Page 3：Add R72

Page 5：ESD diose move to close connector side

Page 7：Add EMI suggestion

Page 8：Add HDMI function

Page 8：G1.H6 pin connector to GND

Page 9：G1.P6 _D7 pin connector to GND

Page 10：Del JTAG、I2C SCH, U503 pin 3 connector to ROM_VCC

Page 12：Change FBVDDQ PWM sch , Add C99 for 3V3_PEX

Page 12：Change PEX_VDD、5V

Page 13：Change NVVDD PWM sch

Page 13：Del PEX_PLL sch

V183 3.0 pcb change list

Page 2 & 13：G1.W15 & G1.E15 connect to NVVDD_SENSE

Page 7：D504 chage to GPIO0_DVI_A_HPD

Page 8 & 9：HDMI function swap IFP_C & IFP_D Block

Page 8 & 9：HDMI function swap G1.H6 & G1.J6 external circuit

Page 9 ：G1.H6 GPU pin redefine to IFPE_IOVDD

Page 9 ：disconnect IFPD_* pin except G1.N6 & G1.H6 in G1F Block

Page 9：Swap J5 pin 1 & 4 , pin 2 & 3

Page 10：Del InfoROM sch、HDCP ROM sch

Page 10：Reserve I2CC & I2CH & I2CS pull high Resister

Page 10 & 13：Reserve GPIO5 & GPIO6 schematic

Page 13：Q10.G & Q17.G change to 3V3_F Pull High

Remove LB2、EC1802、C52、C60(chage to SMD one)、C1003、C1041、C1037、C1045、EC346、C1034、C1038、C1042、EC347、C1035、C1039、C1043、EC348、C1036、C1040、C1044、C1004、C1048、C1046、C1047

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10690-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10690-0000-000	GT218-300, 550/1375/800, 512MB/64bit, 64Mx16 DDR3, DVI-DL+DP+VGA, DT
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P690 Overview

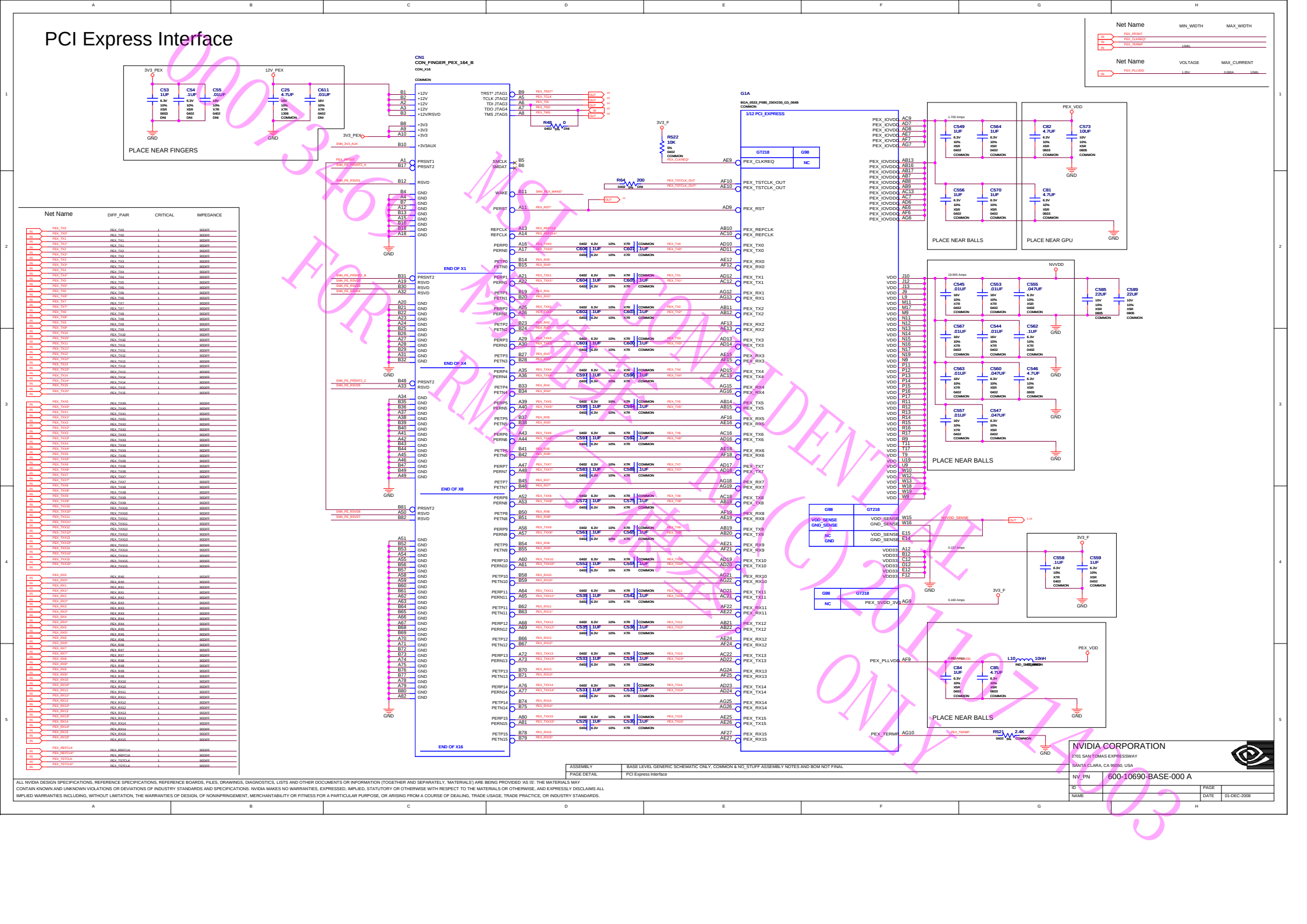
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

00073469 FOR 緯創 CONFIDENTIAL PD(C)20110714003 ONLY

PCI Express Interface



Net Name	DIFF_PAIR	CRITICAL	IMPEDANCE
PEX_TX0	PEX_TX0	1	90DIFF
PEX_TX0*	PEX_TX0	1	90DIFF
PEX_TX1	PEX_TX1	1	90DIFF
PEX_TX1*	PEX_TX1	1	90DIFF
PEX_TX2	PEX_TX2	1	90DIFF
PEX_TX2*	PEX_TX2	1	90DIFF
PEX_TX3	PEX_TX3	1	90DIFF
PEX_TX3*	PEX_TX3	1	90DIFF
PEX_TX4	PEX_TX4	1	90DIFF
PEX_TX4*	PEX_TX4	1	90DIFF
PEX_TX5	PEX_TX5	1	90DIFF
PEX_TX5*	PEX_TX5	1	90DIFF
PEX_TX6	PEX_TX6	1	90DIFF
PEX_TX6*	PEX_TX6	1	90DIFF
PEX_TX7	PEX_TX7	1	90DIFF
PEX_TX7*	PEX_TX7	1	90DIFF
PEX_TX8	PEX_TX8	1	90DIFF
PEX_TX8*	PEX_TX8	1	90DIFF
PEX_TX9	PEX_TX9	1	90DIFF
PEX_TX9*	PEX_TX9	1	90DIFF
PEX_TX10	PEX_TX10	1	90DIFF
PEX_TX10*	PEX_TX10	1	90DIFF
PEX_TX11	PEX_TX11	1	90DIFF
PEX_TX11*	PEX_TX11	1	90DIFF
PEX_TX12	PEX_TX12	1	90DIFF
PEX_TX12*	PEX_TX12	1	90DIFF
PEX_TX13	PEX_TX13	1	90DIFF
PEX_TX13*	PEX_TX13	1	90DIFF
PEX_TX14	PEX_TX14	1	90DIFF
PEX_TX14*	PEX_TX14	1	90DIFF
PEX_TX15	PEX_TX15	1	90DIFF
PEX_TX15*	PEX_TX15	1	90DIFF
PEX_TXX0	PEX_TXX0	1	90DIFF
PEX_TXX0*	PEX_TXX0	1	90DIFF
PEX_TXX1	PEX_TXX1	1	90DIFF
PEX_TXX1*	PEX_TXX1	1	90DIFF
PEX_TXX2	PEX_TXX2	1	90DIFF
PEX_TXX2*	PEX_TXX2	1	90DIFF
PEX_TXX3	PEX_TXX3	1	90DIFF
PEX_TXX3*	PEX_TXX3	1	90DIFF
PEX_TXX4	PEX_TXX4	1	90DIFF
PEX_TXX4*	PEX_TXX4	1	90DIFF
PEX_TXX5	PEX_TXX5	1	90DIFF
PEX_TXX5*	PEX_TXX5	1	90DIFF
PEX_TXX6	PEX_TXX6	1	90DIFF
PEX_TXX6*	PEX_TXX6	1	90DIFF
PEX_TXX7	PEX_TXX7	1	90DIFF
PEX_TXX7*	PEX_TXX7	1	90DIFF
PEX_TXX8	PEX_TXX8	1	90DIFF
PEX_TXX8*	PEX_TXX8	1	90DIFF
PEX_TXX9	PEX_TXX9	1	90DIFF
PEX_TXX9*	PEX_TXX9	1	90DIFF
PEX_TXX10	PEX_TXX10	1	90DIFF
PEX_TXX10*	PEX_TXX10	1	90DIFF
PEX_TXX11	PEX_TXX11	1	90DIFF
PEX_TXX11*	PEX_TXX11	1	90DIFF
PEX_TXX12	PEX_TXX12	1	90DIFF
PEX_TXX12*	PEX_TXX12	1	90DIFF
PEX_TXX13	PEX_TXX13	1	90DIFF
PEX_TXX13*	PEX_TXX13	1	90DIFF
PEX_TXX14	PEX_TXX14	1	90DIFF
PEX_TXX14*	PEX_TXX14	1	90DIFF
PEX_TXX15	PEX_TXX15	1	90DIFF
PEX_TXX15*	PEX_TXX15	1	90DIFF
PEX_RX0	PEX_RX0	1	90DIFF
PEX_RX0*	PEX_RX0	1	90DIFF
PEX_RX1	PEX_RX1	1	90DIFF
PEX_RX1*	PEX_RX1	1	90DIFF
PEX_RX2	PEX_RX2	1	90DIFF
PEX_RX2*	PEX_RX2	1	90DIFF
PEX_RX3	PEX_RX3	1	90DIFF
PEX_RX3*	PEX_RX3	1	90DIFF
PEX_RX4	PEX_RX4	1	90DIFF
PEX_RX4*	PEX_RX4	1	90DIFF
PEX_RX5	PEX_RX5	1	90DIFF
PEX_RX5*	PEX_RX5	1	90DIFF
PEX_RX6	PEX_RX6	1	90DIFF
PEX_RX6*	PEX_RX6	1	90DIFF
PEX_RX7	PEX_RX7	1	90DIFF
PEX_RX7*	PEX_RX7	1	90DIFF
PEX_RX8	PEX_RX8	1	90DIFF
PEX_RX8*	PEX_RX8	1	90DIFF
PEX_RX9	PEX_RX9	1	90DIFF
PEX_RX9*	PEX_RX9	1	90DIFF
PEX_RX10	PEX_RX10	1	90DIFF
PEX_RX10*	PEX_RX10	1	90DIFF
PEX_RX11	PEX_RX11	1	90DIFF
PEX_RX11*	PEX_RX11	1	90DIFF
PEX_RX12	PEX_RX12	1	90DIFF
PEX_RX12*	PEX_RX12	1	90DIFF
PEX_RX13	PEX_RX13	1	90DIFF
PEX_RX13*	PEX_RX13	1	90DIFF
PEX_RX14	PEX_RX14	1	90DIFF
PEX_RX14*	PEX_RX14	1	90DIFF
PEX_RX15	PEX_RX15	1	90DIFF
PEX_RX15*	PEX_RX15	1	90DIFF
PEX_REFCLK	PEX_REFCLK	1	90DIFF
PEX_REFCLK*	PEX_REFCLK	1	90DIFF
PEX_TSTCLK	PEX_TSTCLK	1	90DIFF
PEX_TSTCLK*	PEX_TSTCLK	1	90DIFF

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express Interface

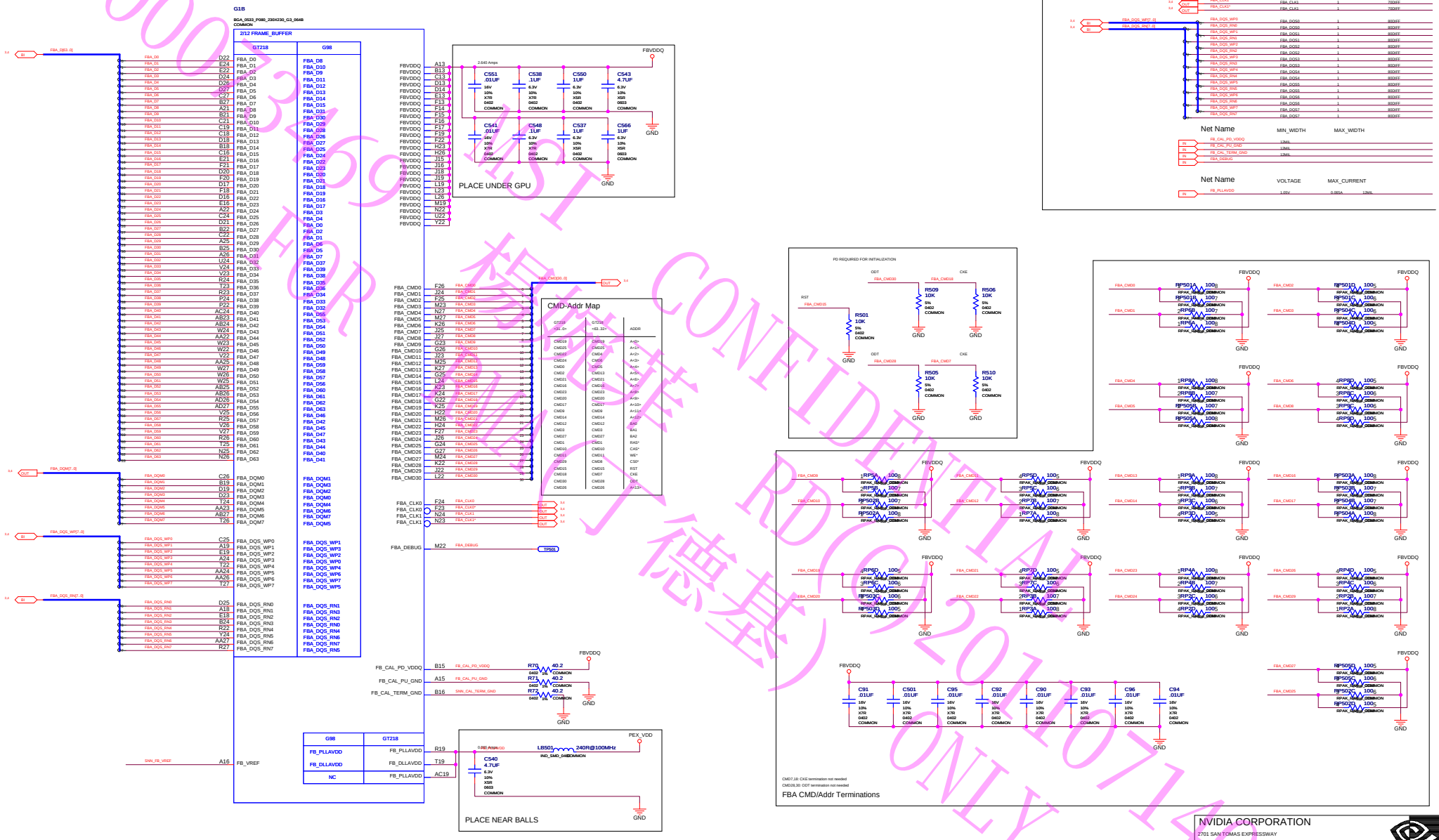
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

0013469 MSI COMPUTER CORP. CONFIDENTIAL FOR MSI INTERNAL USE ONLY RMA ONLY (C)2017 V03

Frame Buffer Interface



0003369 FOR
CONFIDENTIAL
RDC 2010071403
ONLY

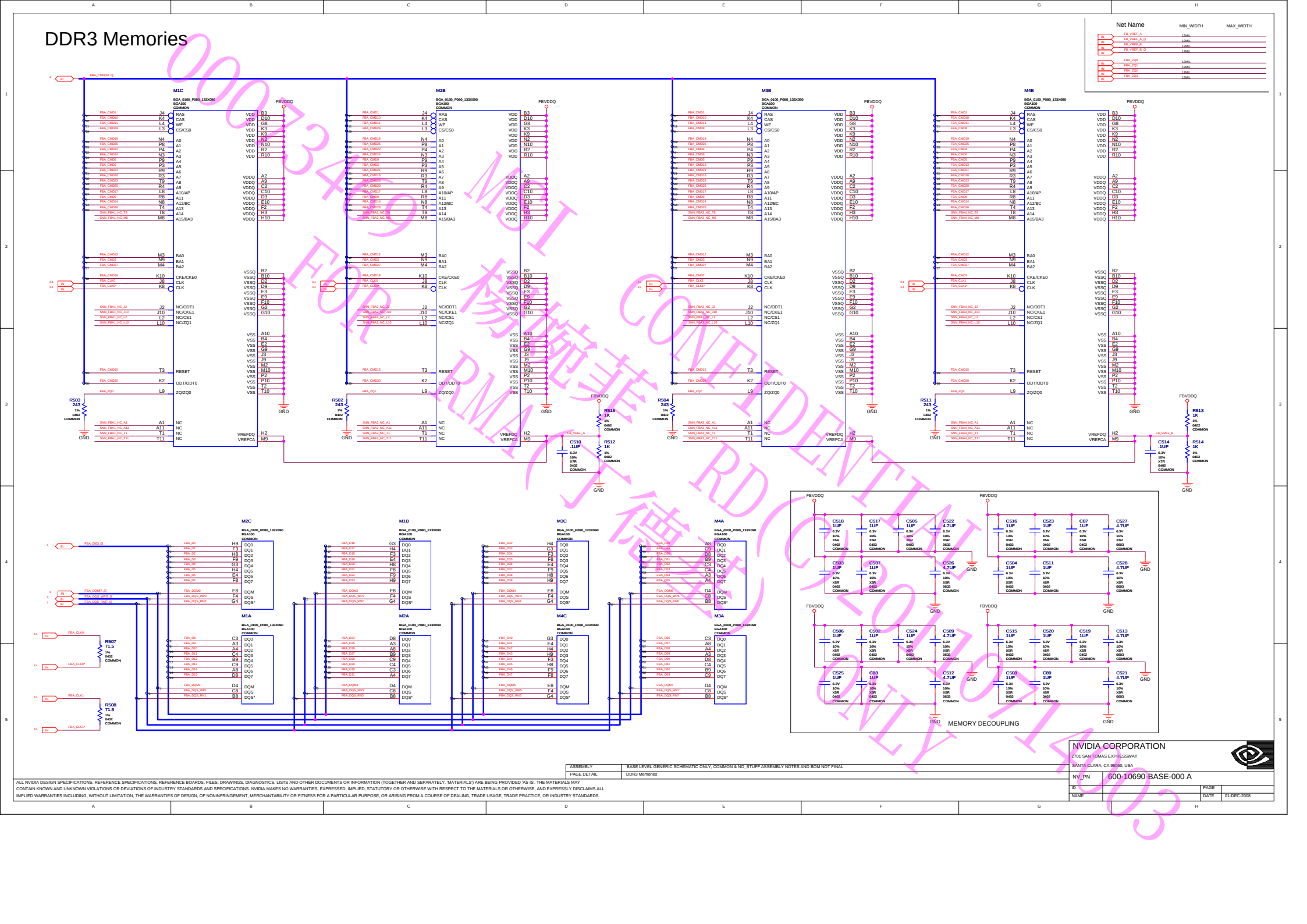
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Frame Buffer Interface

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

DDR3 Memories



Net Name	MIN_WIDTH	MAX_WIDTH
FB_VREF_A	12MIL	
FB_VREF_A_Q	12MIL	
FB_VREF_B	12MIL	
FB_VREF_B_Q	12MIL	
FBA_ZQ0	12MIL	
FBA_ZQ1	12MIL	
FBA_ZQ2	12MIL	
FBA_ZQ3	12MIL	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DDR3 Memories

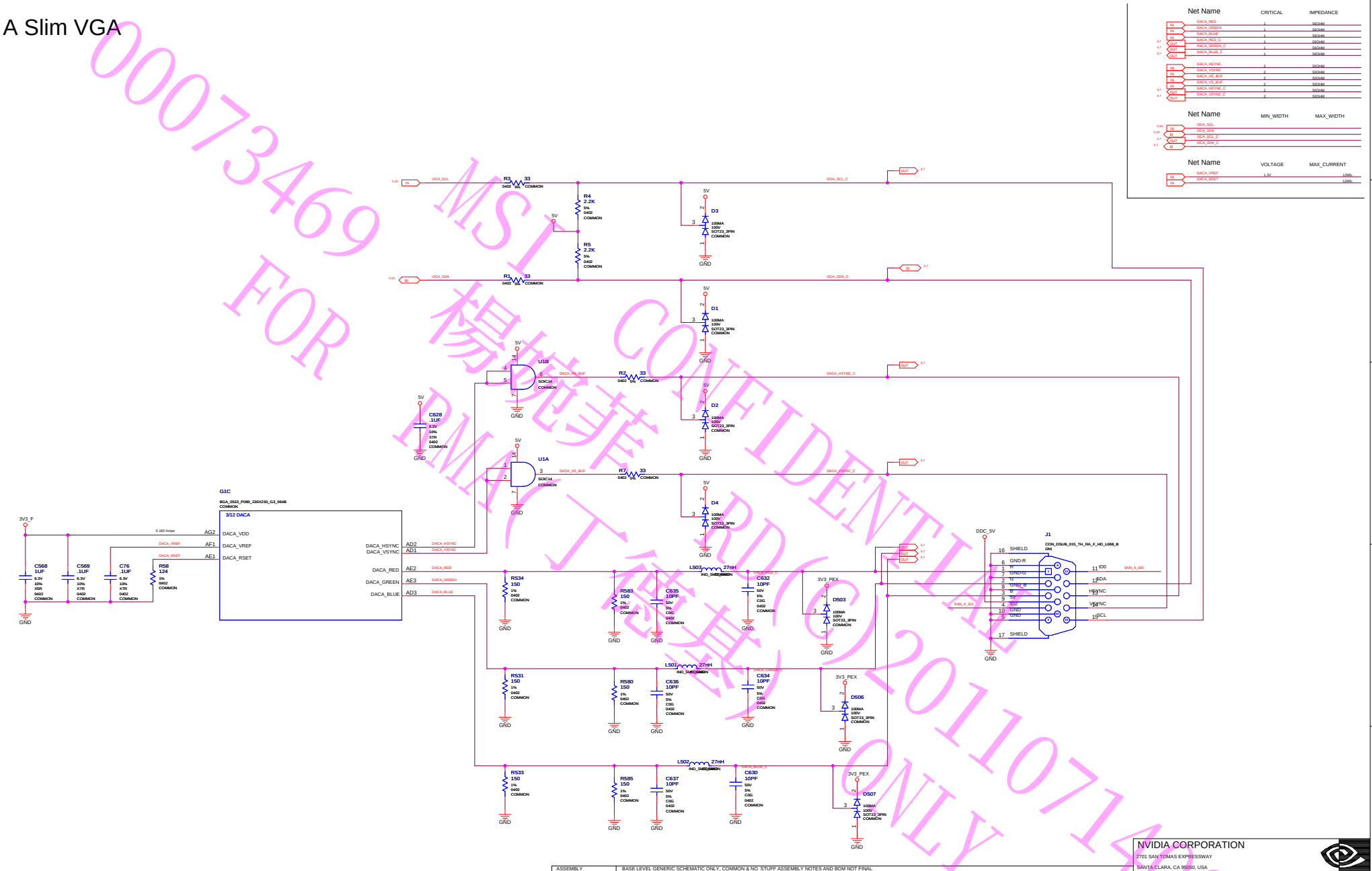
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A
ID	
NAME	
PAGE	
DATE	01-DEC-2008

0073409 NVIDIA CONFIDENTIAL FOR PMA 材质推广 RDC 2015/03/03 ONLY

DAC A Slim VGA



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DAC A Slim VGA

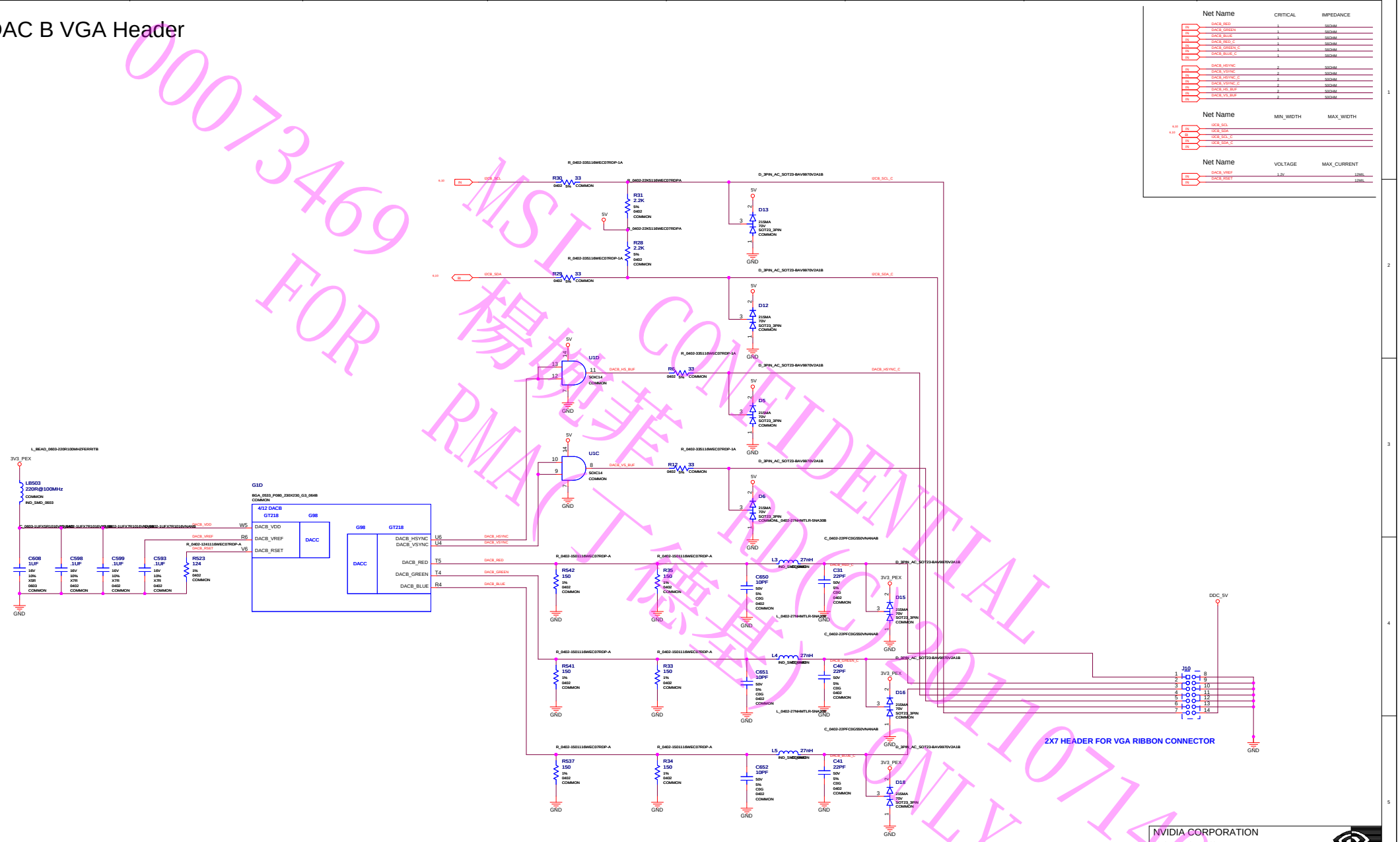
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

00073469 FOR RMA 杨艳霞 CONFIDENTIAL RD(C)20110714003 ONLY

DAC B VGA Header



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DAC B VGA Header

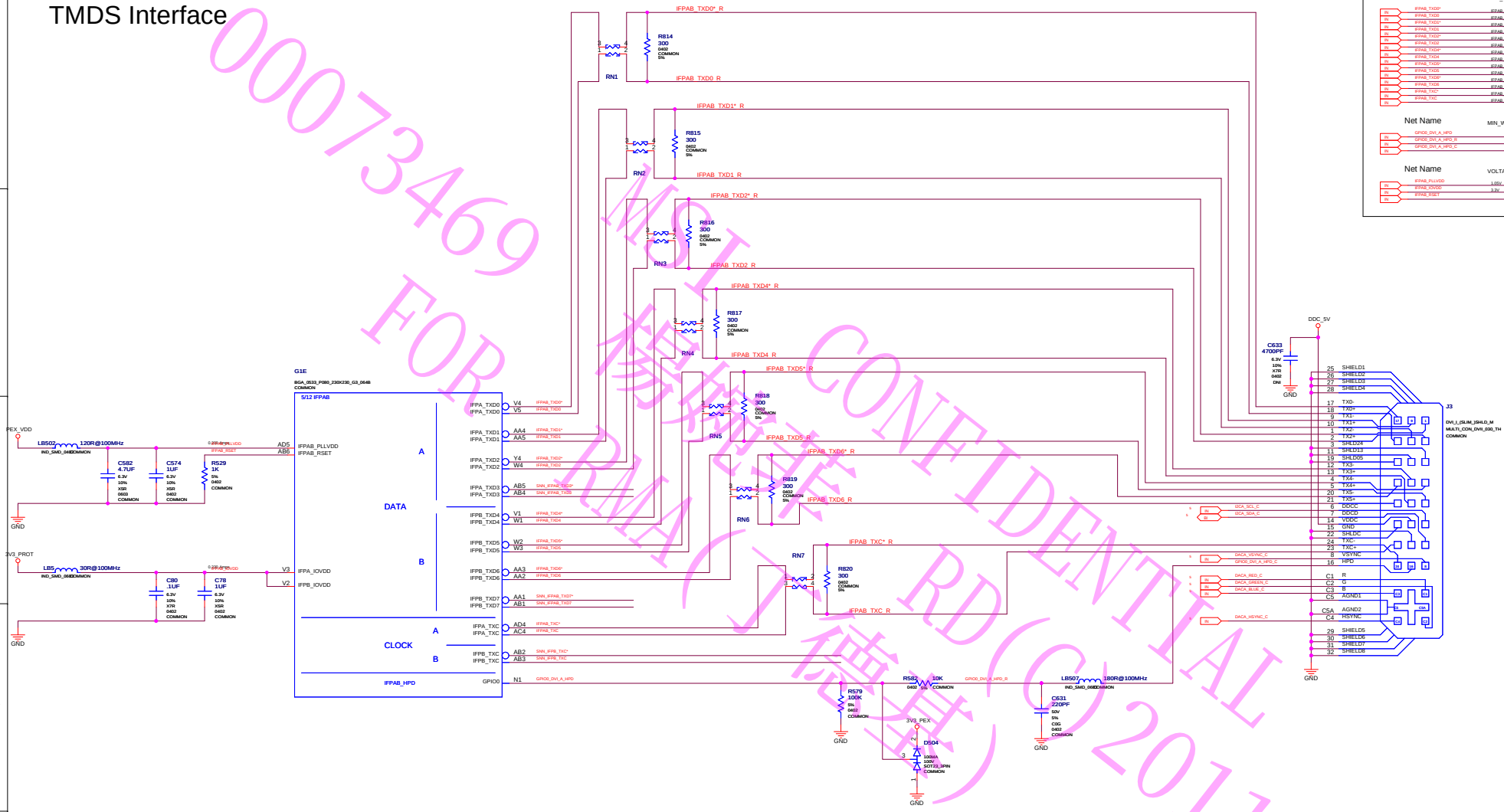
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

000734690 FOR RMA 杨凯雄 CONFIDENTIAL MSI (C) 2011 07 14 03 ONLY

TMDS Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS Interface

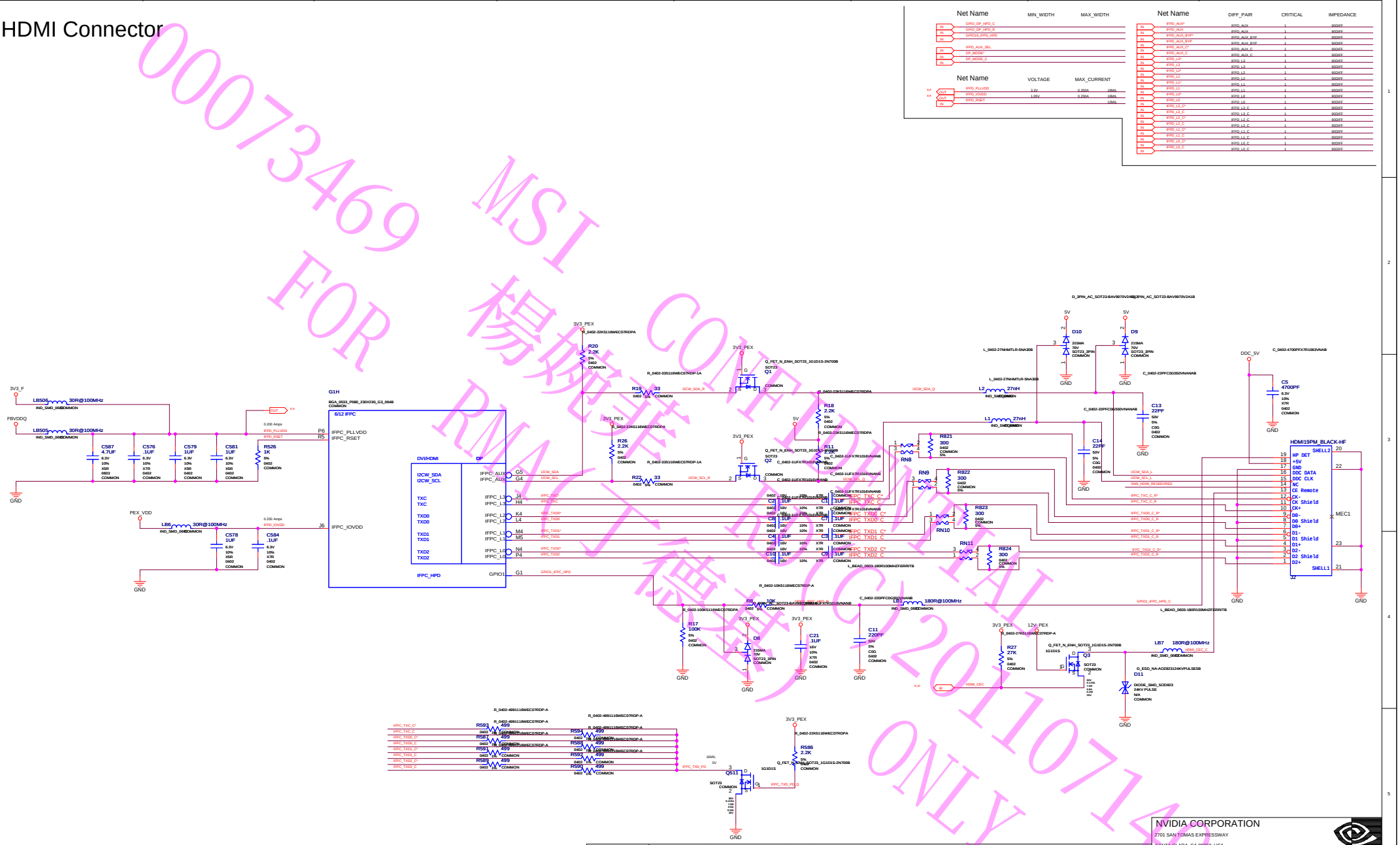
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A
ID	
NAME	
PAGE	
DATE	01-DEC-2008

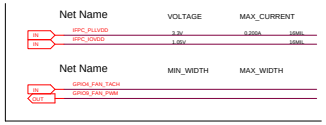
00073469 FOR RMA CONFIDENTIAL RD(C)20110714003 ONLY MSI 微星 (RMA 維修)

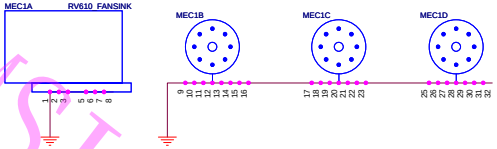
HDMI Connector

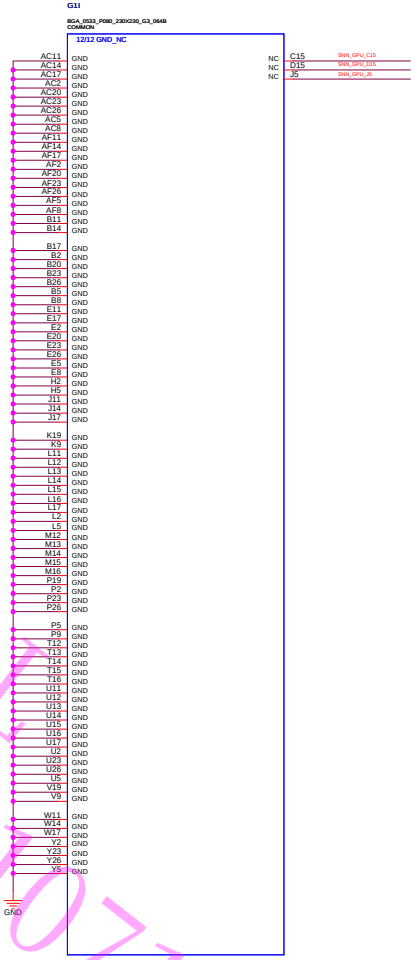


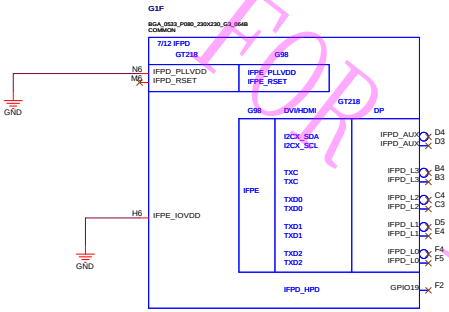
00073469 FOR MSI 楊梅廠 CONFIDENTIAL RMA 機密 ONLY 20110714 03

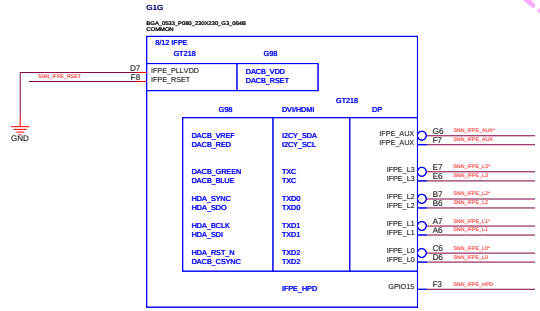
IFPD, IFPE Interface, Fan, Mechanical

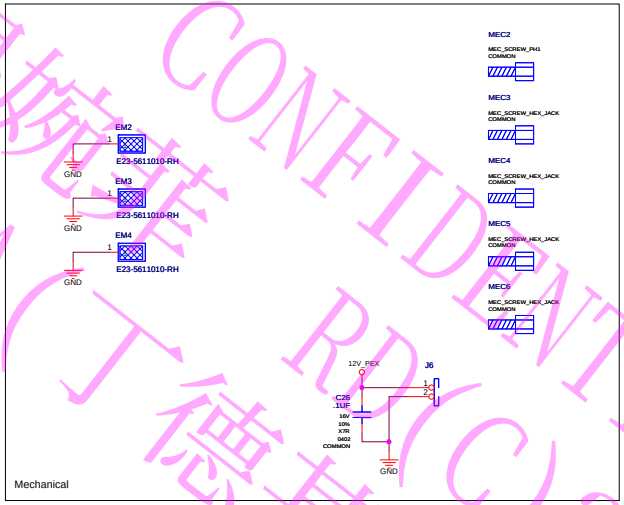


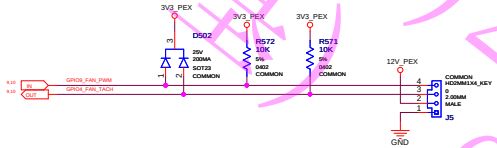












ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPC, IFPE Interface, Fan, Mechanical

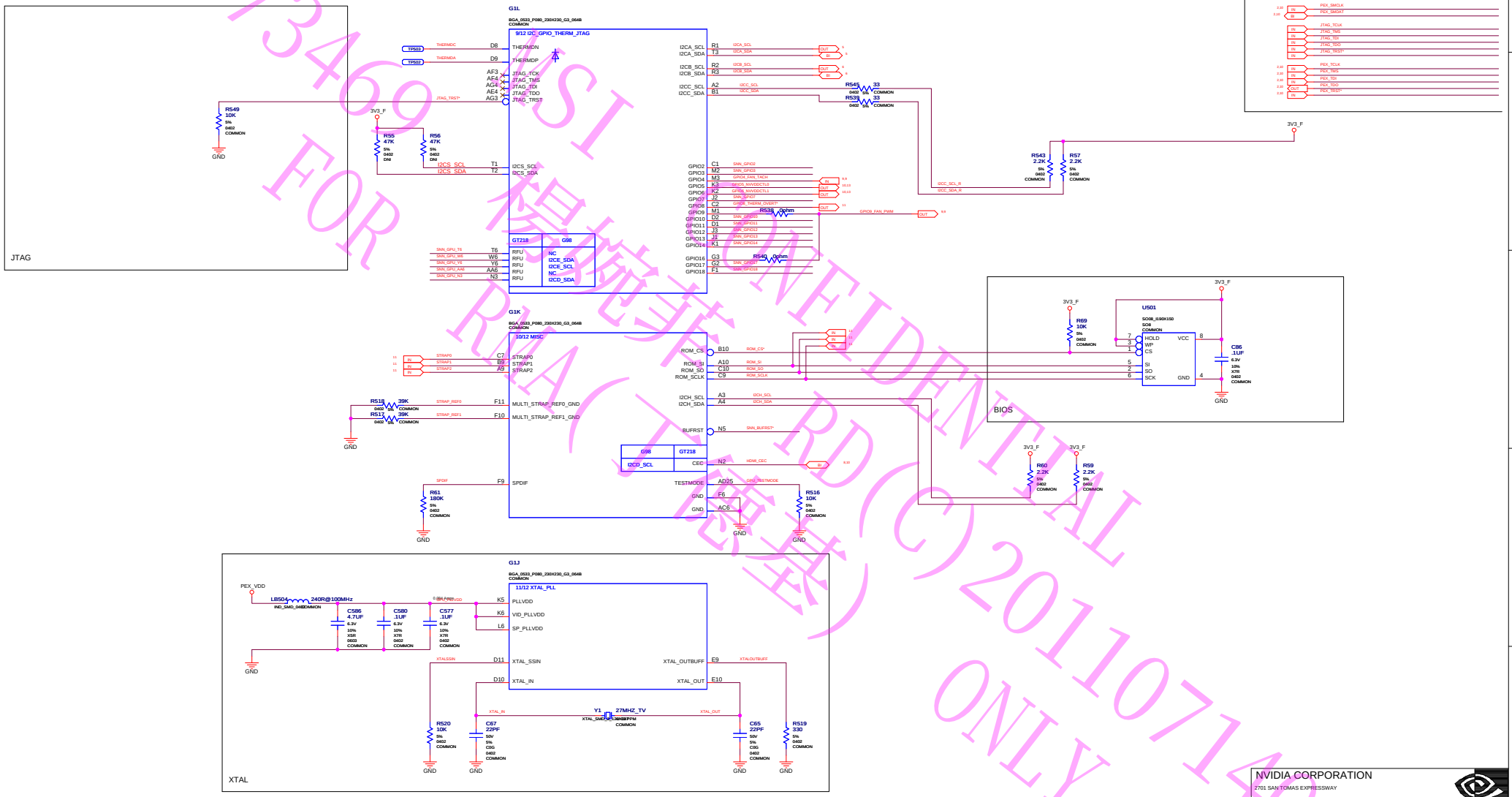
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

00073469
MSI
CONFIDENTIAL
RD(C)20110714003
FOR RMA(仅用于RMA)
ONLY

XTAL, ROM, SPDIF, JTAG



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, ROM, SPDIF, JTAG

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

0007346 NVIDIA CONFIDENTIAL FOR RMA (C)2011071403 ONLY

Thermal Protection, IFP_IOVDD, Straps

0007346 9 MSI 杨硕 CONFIDENTIAL FOR RMA (C)2011071403 RD ONLY

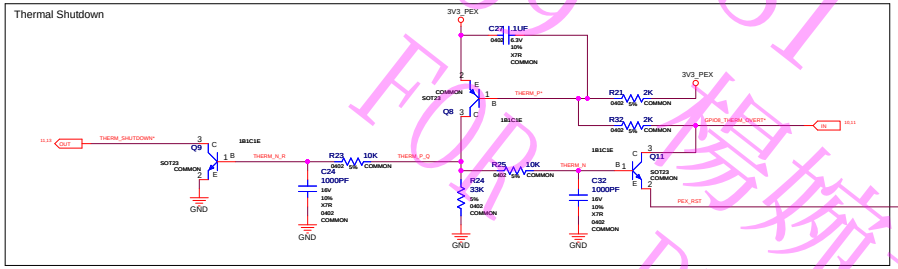
Net Name | MIN_WIDTH | MAX_WIDTH

PEX_RST
PEX_RST_B*
PEX_RST*
GPIO8_THERM_OVERT*
THERM_N_R
THERM_P_Q
THERM_P*
THERM_N
THERM_SHUTDOWN*
ROM_SI
ROM_SO
ROM_SCLK
STRAP2
STRAP1
STRAP0

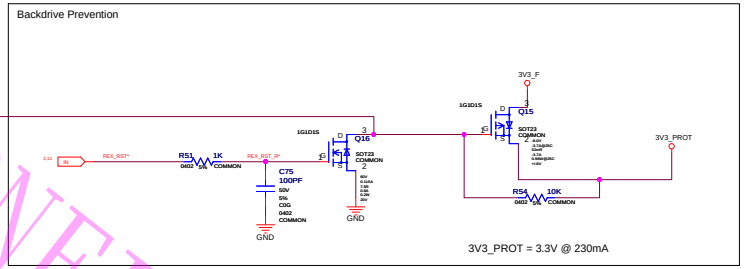
Net Name | VOLTAGE | MAX_CURRENT

3V3_PROT | 3V3_PROT | 3.3V | 0.23A | 16MIL

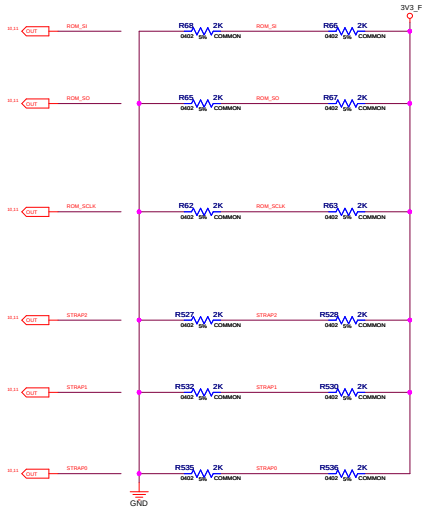
Thermal Shutdown



Backdrive Prevention



3V3_PROT = 3.3V @ 230mA



GT218 Straps MLS Mode

Bit	Signal	Values	
03:	RAMCFG[3]	0000	Elpida
		0001	Samsung, Micron
02:	RAMCFG[2]	0010	Qimonda
		0011	Hynix
01:	RAMCFG[1]	0100	Nanya
00:	RAMCFG[0]		
03:	XCLK_417	0	277 (Default)
02:	FB[0]	0	256M (Default)
01:	SMB_ALT_ADDR	0	0x8E
		1	0x0C
00:	VGA_DEVICE	0	Class code 302
		1	Class code 300
03:	PCI_DEVID_EXT	0	GT218-300-A1
02:	SUB_VENDOR	0	No BIOS
		1	BIOS
01:	SLOT_CLK_CFG	0	Disable
		1	Enable
00:	PEX_PLL_EN_TERM100	0	Disable
		1	Enable
03:	PCI_DEVID[3]	0000	GT218-300-A1
02:	PCI_DEVID[2]		
01:	PCI_DEVID[1]		
00:	PCI_DEVID[0]		
03:	3GIO_PADCFG_LUT_ADR[3]	0000	DSKTOP_DEFAULT
		0001	MOBILE_DEFAULT
02:	3GIO_PADCFG_LUT_ADR[2]	0010	MOBILE_NTHRS_LLAMP
		0011	MOBILE_NTHRS_LAMP
01:	3GIO_PADCFG_LUT_ADR[1]	0100	MOBILE_NTHRS_HAMP
00:	3GIO_PADCFG_LUT_ADR[0]	0101	MOBILE_NTHRS_HHAMP
		0110	MOBILE_NTHRS_HHHAMP
		0111	MOBILE_NTHRS_HHHHAMP
		1000	DSKTOP_HTHRS
		1001	MOBILE_HTHRS_NAMP
		1010	MOBILE_HTHRS_LLAMP
		1011	MOBILE_HTHRS_LAMP
		1100	MOBILE_HTHRS_HAMP
		1101	MOBILE_HTHRS_HHAMP
		1110	MOBILE_HTHRS_HHHAMP
		1111	MOBILE_HTHRS_HHHHAMP
03:	USER[3]	0000	Default
02:	USER[2]		
01:	USER[1]		
00:	USER[0]		

Multilevel Straps

5K to GND	0000
10K to GND	0001
15K to GND	0010
20K to GND	0011
25K to GND	0100
30K to GND	0101
35K to GND	0110
45K to GND	0111
5K to VCC	1000
10K to VCC	1001
15K to VCC	1010
20K to VCC	1011
25K to VCC	1100
30K to VCC	1101
35K to VCC	1110
45K to VCC	1111

GT218 Straps BU Mode

Bit	Signal	Values	
	PCI_DEVID_EXT	0	GT218-300-A1
	XCLK_417	0	277 (Default)
	3GIO_PADCFG_LUT_ADR[3]	0000	DSKTOP_DEFAULT
		0001	MOBILE_DEFAULT
	3GIO_PADCFG_LUT_ADR[2]	0010	MOBILE_NTHRS_LLAMP
		0011	MOBILE_NTHRS_LAMP
	3GIO_PADCFG_LUT_ADR[1]	0100	MOBILE_NTHRS_HAMP
		0101	MOBILE_NTHRS_HHAMP
	3GIO_PADCFG_LUT_ADR[0]	0110	MOBILE_NTHRS_HHHAMP
		0111	MOBILE_NTHRS_HHHHAMP
		1000	DSKTOP_HTHRS
		1001	MOBILE_HTHRS_NAMP
		1010	MOBILE_HTHRS_LLAMP
		1011	MOBILE_HTHRS_LAMP
		1100	MOBILE_HTHRS_HAMP
		1101	MOBILE_HTHRS_HHAMP
		1110	MOBILE_HTHRS_HHHAMP
		1111	MOBILE_HTHRS_HHHHAMP

GT218 Straps PM Mode

Bit	Signal	Values	
	PCI_DEVID_EXT	0	GT218-300-A1
	XCLK_417	0	277/277.OR 417/417
	PCI_DEVID[3]	0	GT218-300-A1
	RAMCFG[3]	0000	Elpida
		0001	Samsung, Micron
	RAMCFG[2]	0010	Qimonda
		0011	Hynix
	RAMCFG[1]	0100	Nanya
	RAMCFG[0]		

Mode	REF0/REF1
MLS	Stuff
BU	NO stuff
PM	Stuff one

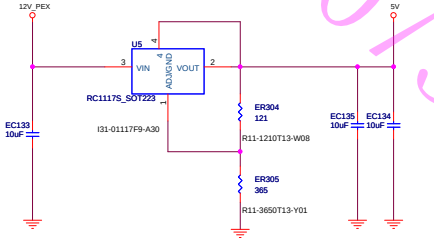
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Protection, IFP_IOVDD, Straps

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

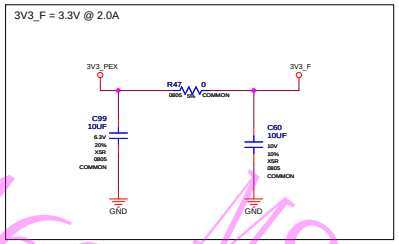
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

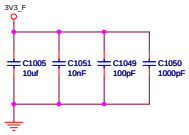
NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

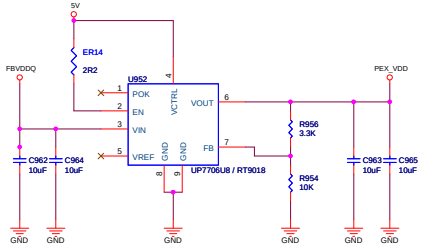
Power Supply I: FBVDD/Q, PEX_VDD, 5V, 3V3_F



Vout=1.25V* [1+(ER305/ER304)]

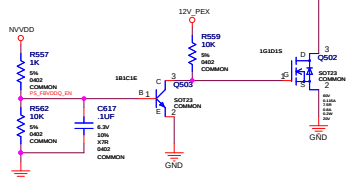




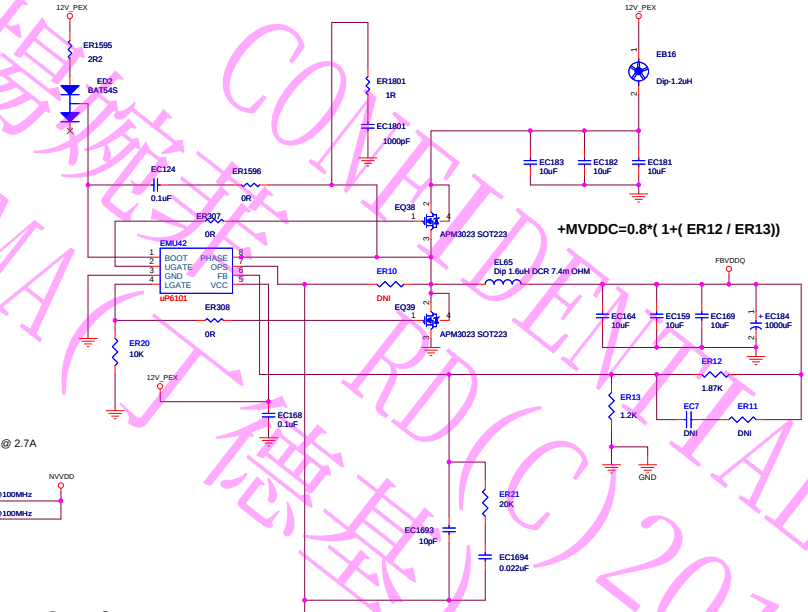


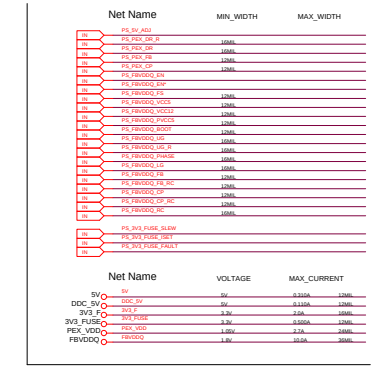
Vout=0.8V * (1+ R995 / R954)

PEX_VDD = 1.05V @ 2.7A



FBVDDQ Power Sequencing





00073469 MSI FOR RMA 楊梅維修 CONFIDENTIAL RD(C)20110714 ONLY 03

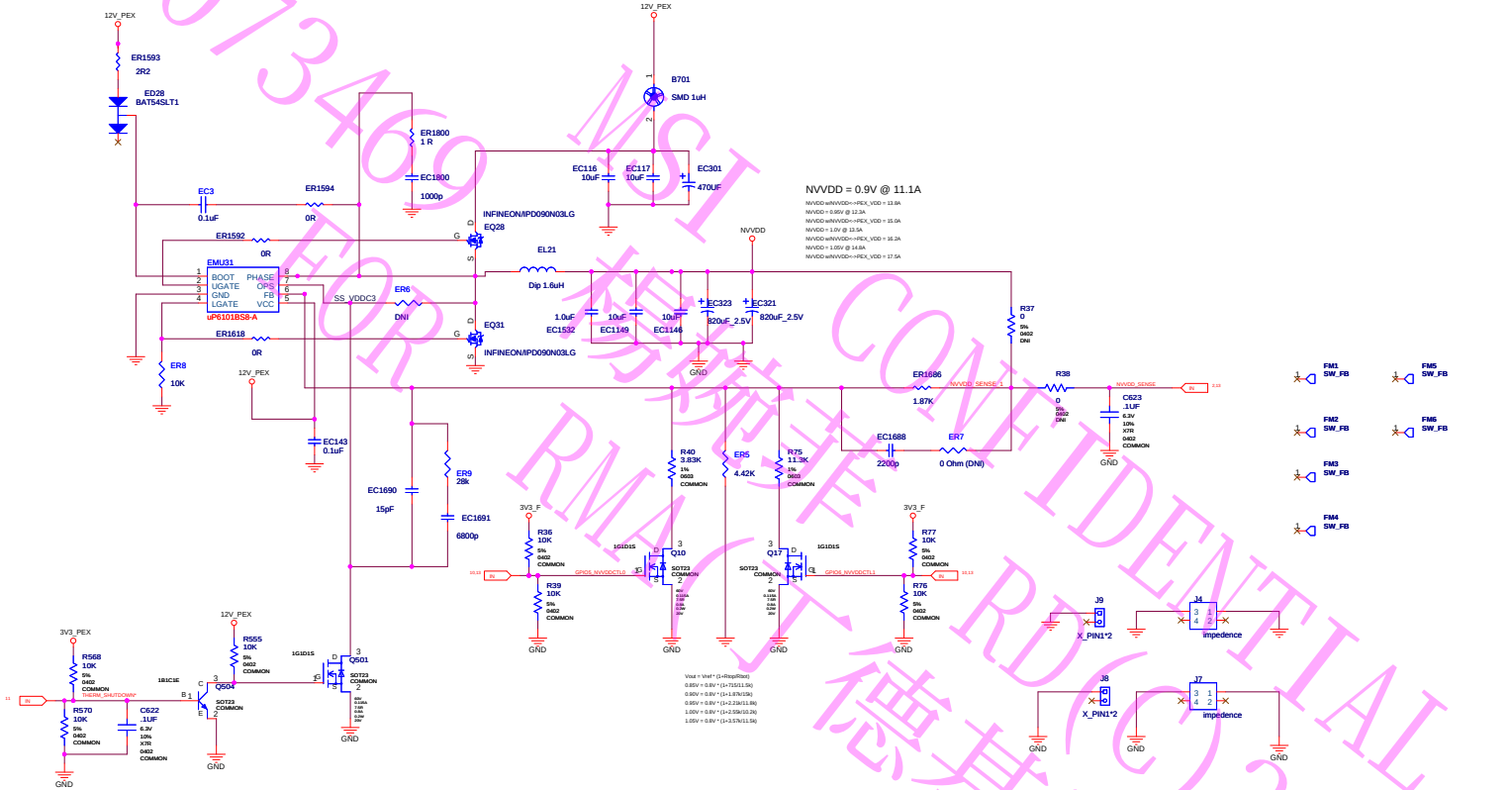
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply I: FBVDD/Q, PEX_VDD, 5V, 3V3_F

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

Power Supply II: PLLVDD, NVVDD



Net Name	MIN_WIDTH	MAX_WIDTH	CRITICAL
PS_NVVDD_ENP			
PS_NVVDD_FS	12MIL		
PS_NVVDD_VCC12	12MIL		
PS_NVVDD_VCC5	12MIL		
PS_NVVDD_PVCC5	12MIL		
PS_NVVDD_BOOT	12MIL		
PS_NVVDD_LDO			
PS_NVVDD_UG	16MIL		
PS_NVVDD_UG_R	16MIL		
PS_NVVDD_PHASE	16MIL		
PS_NVVDD_LG	16MIL		
PS_NVVDD_LG_D	16MIL		
PS_NVVDD_LG_R	16MIL		
PS_NVVDD_RC	16MIL		
PS_NVVDD_FB	12MIL		
PS_NVVDD_FB_RC	12MIL		
PS_NVVDD_CP	12MIL		
PS_NVVDD_CP_RC	12MIL		
NVVDD_SENSE			2
NVVDD_SENSE_R			2
GPIO8_NVVDDCTL			
PS_PEX_PLL_ADJ			

Net Name	VOLTAGE	MAX_CURRENT	POWER_NET
12V_PEX	12V	9.5A	36MIL TRUE
3V3_PEX	3.3V	3.0A	16MIL TRUE
NVVDD	1.1V	17.5A	36MIL

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply II: PLLVDD, NVVDD

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

0007346 9 MSI CONFIDENTIAL 仅供维修使用 RMA (C) 20110714 ONLY 德基

Title: Basenet Report
Design: design
Date: Dec 1 21:48:15 2008

Base nets and synonyms for
design_lib.DESIGN(@design_lib.design(sch
_1))
Base Signal Location([Zone][dir])

3V3_F 12.2H
3V3_FUSE 12.2H
3V3_PEX 13.2G
3V3_PROT 11.1H
5V 12.2H
12V_PEX 13.2G
DACA_BLUE 5.1G< 5.4C
DACA_BLUE_C 5.1G> 5.4F> 7.3F<
DACA_GREEN 5.1G< 5.4C
DACA_GREEN_C 5.1G> 5.4F> 7.3F<
DACA_HSYNC 5.1G< 5.4C
DACA_HSYNC_C 5.1G> 5.3F> 7.4F<
DACA_HS_BUF 5.1G< 5.3D
DACA_RED 5.1G< 5.4C
DACA_RED_C 5.1G> 5.4F> 7.3F<
DACA_RSET 5.2G< 5.4B
DACA_VREF 5.2G< 5.4B
DACA_VSYNC 5.1G< 5.4C
DACA_VSYNC_C 5.1G> 5.3F> 7.3F<
DACA_VS_BUF 5.1G< 5.3D
DACB_BLUE 6.1G< 6.4C
DACB_BLUE_C 6.1G< 6.5E
DACB_GREEN 6.1G< 6.4C
DACB_GREEN_C 6.1G< 6.4E
DACB_HSYNC 6.1G< 6.4C
DACB_HSYNC_C 6.1G< 6.3E
DACB_HS_BUF 6.1G< 6.3D
DACB_RED 6.1G< 6.4C
DACB_RED_C 6.1G< 6.4E
DACB_RSET 6.2G< 6.4B
DACB_VREF 6.2G< 6.4B
DACB_VSYNC 6.1G< 6.4C
DACB_VSYNC_C 6.1G< 6.3E
DACB_VS_BUF 6.1G< 6.3D
DDC_5V 12.2H
DP_MODE* 8.1F< 8.2F
DP_MODE_C 8.1F< 8.3G
FBA_CLK0 3.1G> 3.4D> 4.2A<
4.2B< 4.4A<
FBA_CLK0* 3.1G> 3.4D> 4.2A<
4.2B< 4.5A<
FBA_CLK1 3.1G> 3.4D> 4.2D<
4.2F< 4.5A<
FBA_CLK1* 3.1G> 3.4D> 4.2D<
4.2F< 4.5A<
FBA_CMD<0> 3.2C 3.2G 4.1A 4.1C
FBA_CMD<30..0> 3.1G> 3.2D> 4.1A<>
FBA_CMD<1> 3.2C 3.2G 4.1A 4.1C
4.1E 4.1F
FBA_CMD<2> 3.2C 3.2H 4.1A 4.1C
FBA_CMD<3> 3.2C 3.2H 4.2A 4.2C
4.2E 4.2F
FBA_CMD<4> 3.2C 3.3G 4.1E 4.1F
FBA_CMD<5> 3.3C 3.3G 4.1E 4.1F
FBA_CMD<6> 3.3C 3.3H 4.1E 4.1F
FBA_CMD<7> 3.3C 3.3F 4.2E 4.2F
FBA_CMD<8> 3.3C 3.3H 4.1E 4.1F
FBA_CMD<9> 3.3C 3.3E 4.2A 4.2C
4.2E 4.2F
FBA_CMD<10> 3.3C 3.3E 4.1A 4.1C
4.1E 4.1F
FBA_CMD<11> 3.3C 3.3F 4.1A 4.1C
4.1E 4.1F
FBA_CMD<12> 3.3C 3.3F 4.2A 4.2C
4.2E 4.2F
FBA_CMD<13> 3.3C 3.3G 4.1E 4.1F
FBA_CMD<14> 3.3C 3.3G 4.2A 4.2C
4.2E 4.2F
FBA_CMD<15> 3.2E 3.3C 4.3A 4.3C
4.3E 4.3F
FBA_CMD<16> 3.3C 3.3H 4.2A 4.2C
4.2E 4.2F
FBA_CMD<17> 3.3C 3.3H 4.2A 4.2C
4.2E 4.2F
FBA_CMD<18> 3.2F 3.3C 4.2A 4.2C
FBA_CMD<19> 3.3C 3.4E 4.1A 4.1C
4.1E 4.1F
FBA_CMD<20> 3.3C 3.4E 4.2A 4.2C
4.2E 4.2F
FBA_CMD<21> 3.3C 3.4F 4.2A 4.2C
4.2E 4.2F
FBA_CMD<22> 3.3C 3.4F 4.1A 4.1C
FBA_CMD<23> 3.3C 3.4G 4.2A 4.2C
4.2E 4.2F
FBA_CMD<24> 3.3C 3.4G 4.1A 4.1C
FBA_CMD<25> 3.3C 3.4H 4.1A 4.1C
4.1E 4.1F

FBA_CMD<26> 3.3C 3.4H 4.2A 4.2C
4.2E 4.2F
FBA_CMD<27> 3.3C 3.4H 4.2A 4.2C
4.2E 4.2F
FBA_CMD<28> 3.3C 3.3E 4.3E 4.3F
FBA_CMD<29> 3.3C 3.4H 4.1A 4.1C
FBA_CMD<30> 3.2E 3.3D 4.3A 4.3C
FBA_D<0> 3.1B 4.4B
FBA_D<0..1> 3.1A<> 3.1G<> 4.4A<>
FBA_D<1> 3.1B 4.4B
FBA_D<2> 3.1B 4.4A
FBA_D<3> 3.1B 4.4B
FBA_D<4> 3.1B 4.4B
FBA_D<5> 3.1B 4.4B
FBA_D<6> 3.1B 4.4B
FBA_D<7> 3.1B 4.4B
FBA_D<8> 3.1B 4.4B
FBA_D<9> 3.1B 4.5B
FBA_D<10> 3.1B 4.5B
FBA_D<11> 3.2B 4.5B
FBA_D<12> 3.2B 4.5B
FBA_D<13> 3.2B 4.5B
FBA_D<14> 3.2B 4.5B
FBA_D<15> 3.2B 4.5B
FBA_D<16> 3.2B 4.4C
FBA_D<17> 3.2B 4.4C
FBA_D<18> 3.2B 4.4C
FBA_D<19> 3.2B 4.4C
FBA_D<20> 3.2B 4.4C
FBA_D<21> 3.2B 4.4C
FBA_D<22> 3.2B 4.4C
FBA_D<23> 3.2B 4.4C
FBA_D<24> 3.2B 4.4C
FBA_D<25> 3.2B 4.5C
FBA_D<26> 3.2B 4.5C
FBA_D<27> 3.2B 4.5C
FBA_D<28> 3.2B 4.5C
FBA_D<29> 3.2B 4.5C
FBA_D<30> 3.2B 4.5C
FBA_D<31> 3.2B 4.5C
FBA_D<32> 3.2B 4.4D
FBA_D<33> 3.2B 4.4D
FBA_D<34> 3.2B 4.4D
FBA_D<35> 3.2B 4.4D
FBA_D<36> 3.2B 4.4D
FBA_D<37> 3.2B 4.4D
FBA_D<38> 3.2B 4.4D
FBA_D<39> 3.2B 4.4D
FBA_D<40> 3.2B 4.4D
FBA_D<41> 3.2B 4.5D
FBA_D<42> 3.2B 4.5D
FBA_D<43> 3.2B 4.5D
FBA_D<44> 3.2B 4.5D
FBA_D<45> 3.2B 4.5D
FBA_D<46> 3.2B 4.5D
FBA_D<47> 3.2B 4.5D
FBA_D<48> 3.2B 4.4E
FBA_D<49> 3.2B 4.4E
FBA_D<50> 3.2B 4.4E
FBA_D<51> 3.2B 4.4E
FBA_D<52> 3.2B 4.4E
FBA_D<53> 3.2B 4.4E
FBA_D<54> 3.2B 4.4E
FBA_D<55> 3.2B 4.4E
FBA_D<56> 3.2B 4.4E
FBA_D<57> 3.2B 4.5E
FBA_D<58> 3.2B 4.5E
FBA_D<59> 3.2B 4.5E
FBA_D<60> 3.2B 4.5E
FBA_D<61> 3.2B 4.5E
FBA_D<62> 3.2B 4.5E
FBA_D<63> 3.2B 4.5E
FBA_DEBUG 3.2G< 3.4C
FBA_DQM<0> 3.3B 4.4B
FBA_DQM<7..0> 3.1G> 3.3A> 4.4A<
FBA_DQM<1> 3.3B 4.5B
FBA_DQM<2> 3.3B 4.4C
FBA_DQM<3> 3.3B 4.5C
FBA_DQM<4> 3.3B 4.4D
FBA_DQM<5> 3.4B 4.5D
FBA_DQM<6> 3.4B 4.4E
FBA_DQM<7> 3.4B 4.5E
FBA_DQS_RN<0> 3.1G 3.4B 4.4B
FBA_DQS_RN<7..0> 3.1G<> 3.4A<> 4.4A<>
FBA_DQS_RN<1> 3.1G 3.4B 4.5B
FBA_DQS_RN<2> 3.1G 3.4B 4.4C
FBA_DQS_RN<3> 3.1G 3.4B 4.5C
FBA_DQS_RN<4> 3.1G 3.4B 4.4D
FBA_DQS_RN<5> 3.1G 3.4B 4.5D
FBA_DQS_RN<6> 3.1G 3.4B 4.4E
FBA_DQS_RN<7> 3.1G 3.4B 4.5E
FBA_DQS_WP<0> 3.1G 3.4B 4.4B
FBA_DQS_WP<7..0> 3.1G<> 3.4A<> 4.4A<>
FBA_DQS_WP<1> 3.1G 3.4B 4.5B
FBA_DQS_WP<2> 3.1G 3.4B 4.4C
FBA_DQS_WP<3> 3.1G 3.4B 4.5C

FBA_DQS_WP<4> 3.1G 3.4B 4.4D
FBA_DQS_WP<5> 3.1G 3.4B 4.5D
FBA_DQS_WP<6> 3.1G 3.4B 4.4E
FBA_DQS_WP<7> 3.1G 3.4B 4.5E
FBA_ZQ0 4.1G< 4.3A
FBA_ZQ1 4.1G< 4.3C
FBA_ZQ2 4.1G< 4.3E
FBA_ZQ3 4.1G< 4.3F
FBVDDQ 12.2H
FB_CAL_PD_VDDQ 3.2C< 3.4C
FB_CAL_PU_GND 3.2G< 3.4C
FB_CAL_TERM_GND 3.2G<
FB_PLLAVDD 3.2G< 3.5C
FB_VREF_A 4.1G< 4.3D
FB_VREF_A_Q 4.1G<
FB_VREF_B 4.1G< 4.3H
FB_VREF_B_Q 4.1G<
GPIO0_DVI_A_HPD 7.1G< 7.4D
GPIO0_DVI_A_HPD_C 7.1G< 7.3F
GPIO0_DVI_A_HPD_R 7.1G< 7.4E
GPIO4_FAN_TACH 9.1G< 9.4D> 10.2E<
GPIO5_NVDDCTL 10.2E> 13.1G< 13.5D<
GPIO5_NVDDCTL_R 13.4E
GPIO8_THERM_OVER_T* 10.2E> 11.1G< 11.2D<
GPIO9_FAN_PWM 9.1G> 9.4D< 10.2E>
GPIO10_IFPD_HPD 8.1F< 8.4D
GPIO_DP_HPD_C 8.1F< 8.4F
GPIO_DP_HPD_R 8.1F< 8.4E
GPU_PLLVDD 10.1F< 10.4C
GPU_TESTMODE 10.1G< 10.4E
I2CA_SCL 5.1G< 5.2C< 10.2E>
I2CA_SCL_C 5.1F> 5.1G> 7.3F<
I2CA_SDA 5.1G<> 5.2C<> 10.2E<>
I2CA_SDA_C 5.1G<> 5.2F<> 7.3F<>
I2CB_SCL 6.1G< 6.2C< 10.2E>
I2CB_SCL_C 6.1G< 6.2E
I2CB_SDA 6.1G<> 6.2C<> 10.2E<>
I2CB_SDA_C 6.1G< 6.2E
I2CC_SCL 10.1G< 10.2E
I2CC_SCL_R 10.1G< 10.2F
I2CC_SDA 10.1G< 10.2E
I2CC_SDA_R 10.1G< 10.2F
I2CH_SCL 10.1G< 10.3E
I2CH_SDA 10.1G< 10.3E
I2CS_SCL 10.1G< 10.2C
I2CS_SDA 10.1G< 10.2C
IFPAB_IOVDD 7.2G< 7.3C
IFPAB_PLLVDD 7.2G< 7.3C
IFPAB_RSET 7.2G< 7.3C
IFPAB_TXC 7.1G< 7.4D
IFPAB_TXC* 7.1G< 7.4D
IFPAB_TXD0 7.1G< 7.3D
IFPAB_TXD0* 7.1G< 7.3D
IFPAB_TXD1 7.1G< 7.3D
IFPAB_TXD1* 7.1G< 7.3D
IFPAB_TXD2 7.1G< 7.3D
IFPAB_TXD2* 7.1G< 7.3D
IFPAB_TXD4 7.1G< 7.3D
IFPAB_TXD4* 7.1G< 7.3D
IFPAB_TXD5 7.1G< 7.3D
IFPAB_TXD5* 7.1G< 7.3D
IFPAB_TXD6 7.1G< 7.3D
IFPAB_TXD6* 7.1G< 7.3D
IFPC_IOVDD 9.1G< 9.3B
IFPC_PLLVDD 9.1G< 9.2B
IFPD_AUX 8.1G< 8.4D
IFPD_AUX* 8.1G< 8.4D
IFPD_AUX_BYP 8.1G< 8.3D
IFPD_AUX_BYP* 8.1G< 8.2D
IFPD_AUX_C 8.1G< 8.4F
IFPD_AUX_C* 8.1G< 8.4F
IFPD_AUX_SEL 8.1F< 8.2D
IFPD_IOVDD 8.1F> 8.4C> 9.3A<
IFPD_L0 8.1G< 8.4D
IFPD_L0* 8.1G< 8.4D
IFPD_L0_C 8.1G< 8.4F
IFPD_L0_C* 8.1G< 8.4F
IFPD_L1 8.1G< 8.4D
IFPD_L1* 8.1G< 8.4D
IFPD_L1_C 8.1G< 8.4F
IFPD_L1_C* 8.1G< 8.4F
IFPD_L2 8.1G< 8.4D
IFPD_L2* 8.1G< 8.4D
IFPD_L2_C 8.1G< 8.4F
IFPD_L2_C* 8.1G< 8.4F
IFPD_L3 8.1G< 8.4D
IFPD_L3* 8.1G< 8.4D
IFPD_L3_C 8.1G< 8.4F
IFPD_L3_C* 8.1G< 8.4F
IFPD_PLLVDD 8.1F> 8.3C> 9.2A<
IFPD_RSET 8.1F< 8.4B
JTAG_TCLK 10.1G< 10.2C
JTAG_TDI 10.1G< 10.2C
JTAG_TDO 10.2C 10.2G<
JTAG_TMS 10.1G< 10.2C
JTAG_TRST* 10.2C 10.2G<

NVDDQ 13.2G
NVVDD_SENSE 2.4G> 13.1G< 13.4G<
NVVDD_SENSE_R 13.1G< 13.4F
PEX_CLKREQ* 2.1E 2.1G<
PEX_PLL 13.2G
PEX_PLLVDD 2.1G< 2.5F
PEX_PRSNT 2.1C 2.1G<
PEX_REFCLK 2.2D 2.5A<
PEX_REFCLK* 2.2D 2.5A<
PEX_RST 11.1G< 11.3C
PEX_RST* 2.2D> 11.1G< 11.2E<
PEX_RST_R* 11.1G< 11.2F
PEX_RX0 2.2D 2.4A<
PEX_RX0* 2.2D 2.4A<
PEX_RX1 2.2D 2.4A<
PEX_RX1* 2.2D 2.4A<
PEX_RX2 2.2D 2.4A<
PEX_RX2* 2.3D 2.4A<
PEX_RX3 2.3D 2.4A<
PEX_RX3* 2.3D 2.4A<
PEX_RX4 2.3D 2.4A<
PEX_RX4* 2.3D 2.4A<
PEX_RX5 2.3D 2.4A<
PEX_RX5* 2.3D 2.4A<
PEX_RX6 2.3D 2.5A<
PEX_RX6* 2.3D 2.5A<
PEX_RX7 2.3D 2.5A<
PEX_RX7* 2.4D 2.5A<
PEX_RX8 2.4D 2.5A<
PEX_RX8* 2.4D 2.5A<
PEX_RX9 2.4D 2.5A<
PEX_RX9* 2.4D 2.5A<
PEX_RX10 2.4D 2.5A<
PEX_RX10* 2.4D 2.5A<
PEX_RX11 2.4D 2.5A<
PEX_RX11* 2.4D 2.5A<
PEX_RX12 2.4D 2.5A<
PEX_RX12* 2.5A< 2.5D
PEX_RX13 2.5A< 2.5D
PEX_RX13* 2.5A< 2.5D
PEX_RX14 2.5A< 2.5D
PEX_RX14* 2.5A< 2.5D
PEX_RX15 2.5A< 2.5D
PEX_RX15* 2.5A< 2.5D
PEX_SMCLK 2.1D> 10.1G< 10.3B<
PEX_SMDAT 2.2D<> 10.1G<> 10.3B<>
PEX_TCLK 2.1D> 10.2A< 10.2C<
PEX_TDI 2.1D> 10.2A< 10.2G<
PEX_TDO 2.1D< 10.2A< 10.2G>
PEX_TERM* 2.1G< 9.5A
PEX_TMS 2.1D> 10.2A< 10.2G<
PEX_TRST* 2.1D> 10.2A< 10.2G<
PEX_TSTCLK 2.5A<
PEX_TSTCLK* 2.5A<
PEX_TSTCLK_OUT 2.2E
PEX_TSTCLK_OUT* 2.2E
PEX_TX0 2.2A< 2.2E
PEX_TX0* 2.2A< 2.2E
PEX_TX1 2.2A< 2.2E
PEX_TX1* 2.2A< 2.2E
PEX_TX2 2.2A< 2.2E
PEX_TX2* 2.2A< 2.2E
PEX_TX3 2.2A< 2.3E
PEX_TX3* 2.2A< 2.3E
PEX_TX4 2.2A< 2.3E
PEX_TX4* 2.2A< 2.3E
PEX_TX5 2.2A< 2.3E
PEX_TX5* 2.2A< 2.3E
PEX_TX6 2.2A< 2.3E
PEX_TX6* 2.2A< 2.3E
PEX_TX7 2.2A< 2.3E
PEX_TX7* 2.2A< 2.3E
PEX_TX8 2.2A< 2.4E
PEX_TX8* 2.2A< 2.4E
PEX_TX9 2.3A< 2.4E
PEX_TX9* 2.3A< 2.4E
PEX_TX10 2.3A< 2.4E
PEX_TX10* 2.3A< 2.4E
PEX_TX11 2.3A< 2.4E
PEX_TX11* 2.3A< 2.4E
PEX_TX12 2.3A< 2.4E
PEX_TX12* 2.3A< 2.4E
PEX_TX13 2.3A< 2.5E
PEX_TX13* 2.3A< 2.5E
PEX_TX14 2.3A< 2.5E
PEX_TX14* 2.3A< 2.5E
PEX_TX15 2.3A< 2.5E
PEX_TX15* 2.3A< 2.5E
PEX_TXI0 2.2D 2.3A<
PEX_TXI0* 2.2D 2.3A<
PEX_TXI1 2.2D 2.3A<
PEX_TXI1* 2.2D 2.3A<
PEX_TXI2 2.2D 2.3A<
PEX_TXI2* 2.2D 2.3A<
PEX_TXI3 2.3A< 2.3D

PEX_TXO3* 2.3A< 2.3D
PEX_TXO4 2.3A< 2.3D
PEX_TXO4* 2.3A< 2.3D
PEX_TXO5 2.3A< 2.3D
PEX_TXO5* 2.3A< 2.3D
PEX_TXO6 2.3A< 2.3D
PEX_TXO6* 2.3A< 2.3D
PEX_TXO7 2.3A< 2.3D
PEX_TXO7* 2.3D 2.4A<
PEX_TXO8 2.4A< 2.4D
PEX_TXO8* 2.4A< 2.4D
PEX_TXO9 2.4A< 2.4D
PEX_TXO9* 2.4A< 2.4D
PEX_TXO10 2.4A< 2.4D
PEX_TXO10* 2.4A< 2.4D
PEX_TXO11 2.4A< 2.4D
PEX_TXO11* 2.4A< 2.4D
PEX_TXO12 2.4A< 2.4D
PEX_TXO12* 2.4A< 2.4D
PEX_TXO13 2.4A< 2.5D
PEX_TXO13* 2.4A< 2.5D
PEX_TXO14 2.4A< 2.5D
PEX_TXO14* 2.4A< 2.5D
PEX_TXO15 2.4A< 2.5D
PEX_TXO15* 2.4A< 2.5D
PEX_VDD 12.2H
PS_3V3_FUSE_FAULT 12.1G< 12.3F
PS_3V3_FUSE_ISET 12.1G< 12.3F
PS_3V3_FUSE_SLEW 12.1G< 12.3F
PS_5V_ADJ 12.1G< 12.2B
PS_FBVDDQ_BOOT 12.1G< 12.3E
PS_FBVDDQ_CP 12.1G< 12.4E
PS_FBVDDQ_CP_RC 12.1G< 12.4E
PS_FBVDDQ_EN 12.1G< 12.5C
PS_FBVDDQ_FB 12.1G< 12.5C
PS_FBVDDQ_FB 12.1G< 12.4E
PS_FBVDDQ_FB_RC 12.1G< 12.4G
PS_FBVDDQ_FS 12.1G< 12.4D
PS_FBVDDQ_LG 12.1G< 12.4E
PS_FBVDDQ_PHASE 12.1G< 12.4E
PS_FBVDDQ_PVCCS 12.1G< 12.3E
PS_FBVDDQ_RC 12.1G< 12.4G
PS_FBVDDQ_UG 12.1G< 12.4E
PS_FBVDDQ_UG_R 12.1G< 12.3F
PS_FBVDDQ_VCC5 12.1G< 12.3D
PS_FBVDDQ_VCC12 12.1G< 12.3E
PS_NVDD_BOOT 13.1G< 13.3C
PS_NVDD_CP 13.1G< 13.3C
PS_NVDD_CP_RC 13.1G< 13.4D
PS_NVDD_EN 13.1G< 13.4B
PS_NVDD_FB 13.1G< 13.3C
PS_NVDD_FB_RC 13.1G< 13.4F
PS_NVDD_FS 13.1G< 13.3C
PS_NVDD_LDO 13.1G< 13.3C
PS_NVDD_LG 13.1G< 13.3C
PS_NVDD_LG_D 13.1G< 13.3D
PS_NVDD_LG_R 13.1G< 13.4E
PS_NVDD_PHASE 13.1G< 13.3C
PS_NVDD_PVCCS 13.1G< 13.3C
PS_NVDD_RC 13.1G< 13.4F
PS_NVDD_UG 13.1G< 13.3C
PS_NVDD_UG_R 13.1G< 13.3E
PS_NVDD_VCCS 13.1G< 13.3C
PS_NVDD_VCC12 13.1G< 13.3C
PS_PEX_CP 12.1G< 12.4C
PS_PEX_DR 12.1G< 12.3D
PS_PEX_DR_R 12.1G< 12.3E
PS_PEX_FB 12.1G< 12.4D
PS_PEX_PLL_ADJ 13.1E 13.2G<
ROM_CS* 10.1G< 10.3E
ROM_SCLK 10.3E< 11.1G> 11.4A<
11.4B
ROM_SI 10.3E< 11.1G> 11.3A>
11.3B
ROM_SO 10.3E< 11.1G> 11.3A>
11.3B
ROM_VCC 10.2F
SNN_3V3_AUX 2.1C
SNN_AOZ_7 12.2G
SNN_A_ID0 5.4G
SNN_A_ID2 5.4F
SNN_BUFRST* 10.3E
SNN_CAL_TERM_GND 3.4C
SNN_CEC 10.4E
SNN_DP_CEC 8.4G
SNN_FBA1_NC_A1 4.3A
SNN_FBA1_NC_A11 4.3A
SNN_FBA1_NC_J2 4.2A
SNN_FBA1_NC_J10 4.2A
SNN_FBA1_NC_L2 4.2A
SNN_FBA1_NC_L10 4.2A
SNN_FBA1_NC_M8 4.2A
SNN_FBA1_NC_T1 4.3A
SNN_FBA1_NC_T8 4.2A
SNN_FBA1_NC_T11 4.3A
SNN_FBA2_NC_A11 4.3C
SNN_FBA2_NC_J2 4.2C
SNN_FBA2_NC_J10 4.2C
SNN_FBA2_NC_L2 4.2C
SNN_FBA2_NC_L10 4.2C
SNN_FBA2_NC_M8 4.2C
SNN_FBA2_NC_T1 4.3C
SNN_FBA2_NC_T8 4.2C
SNN_FBA2_NC_T11 4.3C
SNN_FBA3_NC_A1 4.3E
SNN_FBA3_NC_A11 4.3E
SNN_FBA3_NC_J2 4.2E
SNN_FBA3_NC_J10 4.2E
SNN_FBA3_NC_L2 4.2E
SNN_FBA3_NC_L10 4.2E
SNN_FBA3_NC_M8 4.2E
SNN_FBA3_NC_T1 4.3E
SNN_FBA3_NC_T8 4.2E
SNN_FBA3_NC_T11 4.3E
SNN_FBA4_NC_A1 4.3F
SNN_FBA4_NC_A11 4.3F
SNN_FBA4_NC_J2 4.2F
SNN_FBA4_NC_J10 4.2F
SNN_FBA4_NC_L2 4.2F
SNN_FBA4_NC_L10 4.2F
SNN_FBA4_NC_M8 4.2F
SNN_FBA4_NC_T1 4.3F
SNN_FBA4_NC_T8 4.2F
SNN_FBA4_NC_T11 4.3F
SNN_FB_VREF 3.5B
SNN_GPIO2 10.2E
SNN_GPIO3 10.2E
SNN_GPIO6 10.2E
SNN_GPIO7 10.2E
SNN_GPIO10 10.2E
SNN_GPIO11 10.2E
SNN_GPIO12 10.2E
SNN_GPIO13 10.2E
SNN_GPIO14 10.2E
SNN_GPIO17 10.3E
SNN_GPIO18 10.3E
SNN_GPU_AA6 10.3C
SNN_GPU_C15 9.2H
SNN_GPU_D15 9.2H
SNN_GPU_J5 9.2H
SNN_GPU_N3 10.3C
SNN_GPU_T6 10.3C
SNN_GPU_W6 10.3C
SNN_GPU_Y6 10.3C
SNN_HDCP_2 10.4G
SNN_IFPAB_TXD3 7.3D
SNN_IFPAB_TXD3* 7.3D
SNN_IFPAB_TXD7 7.4D
SNN_IFPAB_TXD7* 7.3D
SNN_IFPB_TXC 7.4D
SNN_IFPB_TXC* 7.4D
SNN_IFPC_AUX 9.3C
SNN_IFPC_AUX* 9.2C
SNN_IFPC_HPD 9.3C
SNN_IFPC_L0 9.3C
SNN_IFPC_L0* 9.3C
SNN_IFPC_L1 9.3C
SNN_IFPC_L1* 9.3C
SNN_IFPC_L2 9.3C
SNN_IFPC_L2* 9.3C
SNN_IFPC_L3 9.3C
SNN_IFPC_L3* 9.3C
SNN_IFPE_RSET 9.2B
SNN_IFPE_AUX 9.4C
SNN_IFPE_AUX* 9.4C
SNN_IFPE_HPD 9.4C
SNN_IFPE_L0 9.4C
SNN_IFPE_L0* 9.4C
SNN_IFPE_L1 9.4C
SNN_IFPE_L1* 9.4C
SNN_IFPE_L2 9.4C
SNN_IFPE_L2* 9.4C
SNN_IFPE_L3 9.4C
SNN_IFPE_L3* 9.4C
SNN_IFPE_RSET 9.3B
SNN_PEX_WAKE* 2.2D
SNN_PE_PRSNT2_A 2.1C
SNN_PE_PRSNT2_B 2.2C
SNN_PE_PRSNT2_C 2.3C
SNN_PE_RSVD1 2.2C
SNN_PE_RSVD2 2.2C
SNN_PE_RSVD3 2.2C
SNN_PE_RSVD4 2.2C
SNN_PE_RSVD5 2.3C
SNN_PE_RSVD6 2.4C
SNN_PE_RSVD7 2.4C
SPDIF 10.1G< 10.4C
STRAP0 10.3C< 11.1G> 11.5A<
11.5B
STRAP1 10.3C< 11.1G> 11.4A>
11.4B

STRAP2 10.3C< 11.1G> 11.4A>
11.4B
STRAP_REF0 10.1G< 10.3C
STRAP_REF1 10.1G< 10.3C
THERMDA 10.1G< 10.2C
THERMDC 10.1C 10.1G<
THERM_N 11.1G< 11.2C
THERM_N_R 11.1G< 11.2B
THERM_P* 11.1G< 11.2C
THERM_P_Q 11.1G< 11.2B
THERM_SHUTDOWN* 11.1G> 11.2A> 13.4A<
XTALOUTBUFF 10.1F< 10.5E
XTALSSIN 10.1F< 10.5C
XTAL_IN 10.1F< 10.5C
XTAL_OUT 10.1F< 10.5D

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	<edit here to insert page detail>

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME	<ENGINEER>	DATE	01-DEC-2008

MSI 杨长征 CONFIDENTIAL FOR RMA 仅供RMA(C)2014 ONLY 07340 10714 03

Title: Cref Part
Report:
Design: design
Date: Dec 1
21:48:15 2008

BKT1 [9.3E]
C1 [8.4E]
C2 [8.4E]
C3 [8.4E]
C4 [8.4E]
C5 [5.5B]
C6 [5.5C]
C7 [8.5E]
C8 [12.2B]
C9 [8.4E]
C10 [8.4E]
C11 [8.4E]
C12 [8.4E]
C13 [8.5E]
C14 [6.4F]
C15 [12.3C]
C16 [12.4A]
C17 [8.4F]
C18 [12.3B]
C19 [12.3B]
C20 [12.4A]
C21 [12.2A]
C22 [12.4A]
C23 [12.4B]
C24 [11.3B]
C25 [2.1B]
C26 [9.4E]
C27 [11.2C]
C28 [13.2G]
C29 [8.2D]
C30 [8.3D]
C31 [6.4E]
C32 [11.3C]
C33 [13.4F]
C34 [13.2G]
C35 [13.3C]
C36 [12.3E]
C37 [13.2D]
C38 [6.4E]
C39 [13.2E]
C40 [12.3D]
C41 [12.4F]
C42 [13.3F]
C43 [12.3E]
C44 [13.2F]
C45 [13.2F]
C46 [6.5E]
C47 [13.2G]
C48 [13.2F]
C49 [13.2G]
C50 [13.4F]
C51 [12.4G]
C52 [12.2D]
C53 [2.1A]
C54 [2.1B]
C55 [2.1B]
C56 [12.3G]
C57 [13.4E]
C58 [10.3B]
C59 [13.4G]
C60 [12.2D]
C61 [12.4H]
C62 [12.4H]
C63 [12.4H]
C64 [12.4H]
C65 [10.5E]
C66 [13.3G]
C67 [10.5C]
C68 [13.1F]
C69 [13.1F]
C70 [5.3B]
C71 [13.1E]
C72 [5.2B]
C73 [5.2B]
C74 [5.3B]
C75 [11.3F]
C76 [5.4B]
C77 [8.4A]
C78 [7.3C]
C79 [8.4A]
C80 [7.3B]
C81 [2.2G]
C82 [2.1G]
C83 [10.4G]
C84 [2.5F]
C85 [2.5G]
C86 [10.3G]
C87 [4.4G]
C88 [4.5F]

C89 [4.5G]
C90 [3.5F]
C91 [3.5E]
C92 [3.5F]
C93 [3.5G]
C94 [3.5G]
C95 [3.5F]
C96 [3.5G]
C501 [3.5F]
C502 [4.5F]
C503 [4.4F]
C504 [4.4G]
C505 [4.4F]
C506 [4.5F]
C507 [4.4F]
C508 [4.5G]
C509 [4.5F]
C510 [4.3D]
C511 [8.4E]
C512 [4.5F]
C513 [4.5G]
C514 [4.3H]
C515 [4.5G]
C516 [4.4G]
C517 [4.4F]
C518 [4.4F]
C519 [4.5G]
C520 [4.5G]
C521 [4.5G]
C522 [4.4F]
C523 [4.4G]
C524 [4.5F]
C525 [4.5F]
C526 [4.4F]
C527 [4.4G]
C528 [4.4G]
C529 [2.5G]
C530 [2.5G]
C531 [2.5G]
C532 [2.5G]
C533 [2.5G]
C534 [2.5G]
C535 [2.4G]
C536 [2.4G]
C537 [3.2G]
C538 [3.1G]
C539 [2.4G]
C540 [3.5C]
C541 [3.2C]
C542 [2.4G]
C543 [3.1G]
C544 [2.3G]
C545 [2.2F]
C546 [2.3G]
C547 [2.3G]
C548 [3.2G]
C549 [2.1F]
C550 [3.1G]
C551 [3.1C]
C552 [2.4G]
C553 [2.2G]
C554 [2.4G]
C555 [2.2G]
C556 [2.2F]
C557 [2.3F]
C558 [2.4G]
C559 [2.4G]
C560 [2.3G]
C561 [2.4G]
C562 [2.3G]
C563 [2.3F]
C564 [2.1G]
C565 [2.4G]
C566 [3.2G]
C567 [2.3F]
C568 [5.4A]
C569 [5.4A]
C570 [2.2G]
C571 [6.4B]
C572 [2.4G]
C573 [2.1G]
C574 [7.3B]
C575 [2.4G]
C576 [8.4B]
C577 [10.4C]
C578 [8.4B]
C579 [8.4B]
C580 [10.4C]
C581 [8.4B]
C582 [7.3B]
C583 [2.3G]
C584 [8.4B]
C585 [8.2C]
C586 [10.4C]
C587 [8.4A]
C588 [2.3G]

C589 [8.3C]
C590 [10.3F]
C591 [2.3G]
C592 [2.3G]
C593 [10.2B]
C594 [2.3G]
C595 [2.3G]
C596 [2.3G]
C597 [2.3G]
C598 [8.2C]
C599 [8.3G]
C600 [2.3G]
C601 [2.3G]
C602 [2.2G]
C603 [2.2G]
C604 [2.2G]
C605 [2.2G]
C606 [2.2G]
C607 [2.2G]
C608 [13.3E]
C609 [12.4E]
C610 [6.5C]
C611 [2.1B]
C612 [13.4E]
C613 [13.4D]
C614 [13.3D]
C615 [12.4C]
C616 [12.5F]
C617 [12.5C]
C618 [12.5E]
C619 [12.5G]
C620 [6.5C]
C621 [12.3E]
C622 [13.4B]
C623 [8.3F]
C624 [12.3E]
C625 [12.3F]
C626 [12.3G]
C627 [12.3G]
C628 [5.3C]
C629 [6.5B]
C630 [5.5E]
C631 [7.4E]
C632 [5.4E]
C633 [7.2G]
C634 [5.4E]
CN1 [2.3C]
D1 [5.2E]
D2 [5.3E]
D3 [5.2E]
D4 [5.3E]
D5 [8.3E]
D6 [6.3E]
D7 [8.3G]
D8 [6.2E]
D9 [8.2F]
D10 [8.3F]
D11 [8.2E]
D12 [6.4E]
D13 [6.4E]
D14 [6.5E]
D15 [10.3B]
D16 [10.3B]
D17 [10.2G]
D501 [13.3D]
D502 [9.4E]
D503 [5.4E]
D504 [7.4E]
D505 [8.5E]
D506 [5.4E]
D507 [5.5E]
F501 [12.2G]
F502 [12.2B]
G1 [2.3F]
G1 [3.3C]
G1 [5.4C]
G1 [8.4C]
G1 [7.3D]
G1 [8.4C]
G1 [9.4C 9.3G 9.3C]
G1 [10.4D 10.2D 10.3D]
J1 [5.4G]
J2 [8.4G]
J3 [7.3G]
J4 [6.4G]
J5 [9.4F]
J6 [9.4E]
JS01 [10.2A]
L1 [6.4E]
L2 [6.4E]
L3 [6.5E]
L4 [12.4G]
L5 [12.3G]
L6 [13.3F]

L7 [13.3F]
L8 [13.3F]
L9 [13.4F]
L10 [2.5G]
L11 [2.5G]
L501 [5.4E]
L502 [5.5E]
L503 [5.4E]
LB1 [8.4F]
LB2 [12.2D]
LB3 [12.3A]
LB4 [12.3A]
LB5 [7.3B]
LB6 [8.4B]
LB501 [3.5D]
LB502 [7.3B]
LB503 [10.4B]
LB504 [10.4B]
LB505 [8.4A]
LB506 [8.3A]
LB507 [7.4F]
M1 [4.2B 4.4C 4.5B]
M2 [4.4B 4.5C 4.2C]
M3 [4.5E 4.2F 4.4D]
M4 [4.4E 4.2G 4.5D]
MEC1 [9.3D]
MEC2 [9.2F]
MEC3 [9.3F]
MEC4 [9.3F]
MEC5 [9.3F]
MEC6 [9.3F]
Q1 [8.3G]
Q2 [12.3B]
Q3 [8.3F]
Q4 [8.2E]
Q5 [8.3E]
Q6 [8.2D]
Q7 [8.3D]
Q8 [11.2C]
Q9 [11.2B]
Q10 [13.5E]
Q11 [11.2C]
Q12 [12.4F 12.3F]
Q13 [13.3E]
Q14 [13.3E]
Q15 [11.2G]
Q16 [11.2F]
Q501 [13.4B]
Q502 [12.5D]
Q503 [12.5C]
Q504 [13.4B]
R1 [5.2D]
R2 [5.3D]
R3 [5.2D]
R4 [5.2D]
R5 [5.2D]
R6 [5.2D]
R7 [5.3D]
R8 [5.3D]
R9 [8.2E]
R10 [8.3E]
R11 [8.3G]
R12 [6.2D]
R13 [6.2D]
R14 [8.2E]
R15 [8.3E]
R16 [8.2G]
R17 [8.2F]
R18 [12.2B]
R19 [12.2B]
R20 [6.2D]
R21 [11.2C]
R22 [6.2D]
R23 [11.2B]
R24 [11.3C]
R25 [11.2C]
R26 [8.3D]
R27 [8.3D]
R28 [13.5D]
R29 [13.4F]
R30 [6.4E]
R31 [13.4F]
R32 [11.2C]
R33 [13.4F]
R34 [13.4E]
R35 [13.4D]
R36 [13.3C]
R37 [13.4G]
R38 [12.3D]
R39 [12.4B]
R40 [13.2C]
R41 [6.4E]

R42 [12.3D]
R43 [6.5E]
R44 [13.3F]
R45 [12.4G]
R46 [13.4G]
R47 [12.2D]
R48 [2.1D]
R49 [13.2F]
R50 [13.1F]
R51 [11.2F]
R52 [10.3B]
R53 [10.3B]
R54 [11.3G]
R55 [10.2C]
R56 [10.2C]
R57 [10.2F]
R58 [5.4B]
R59 [10.4F]
R60 [10.4F]
R61 [10.4C]
R62 [11.4B]
R63 [11.4B]
R64 [2.2D]
R65 [11.3B]
R66 [11.3B]
R67 [11.3B]
R68 [11.3B]
R69 [10.3F]
R70 [3.4D]
R71 [3.4D]
R501 [3.3E]
R502 [4.3C]
R503 [4.3A]
R504 [4.3E]
R505 [3.3F]
R506 [3.2F]
R507 [4.5A]
R508 [4.5A]
R509 [3.2F]
R510 [3.3F]
R511 [4.3F]
R512 [4.3D]
R513 [4.3H]
R514 [4.3H]
R515 [4.3D]
R516 [10.4E]
R517 [10.3C]
R518 [10.3C]
R519 [10.5E]
R520 [10.5C]
R521 [2.5G]
R522 [2.1E]
R523 [9.2A]
R524 [6.4B]
R525 [9.3A]
R526 [8.4B]
R527 [11.4B]
R528 [11.4B]
R529 [7.3C]
R530 [11.4B]
R531 [5.4D]
R532 [11.4B]
R533 [5.5D]
R534 [5.4D]
R535 [11.5B]
R536 [11.5B]
R537 [6.4D]
R538 [10.2B]
R539 [10.2E]
R540 [6.4D]
R541 [6.5D]
R542 [10.2B]
R543 [10.2F]
R544 [10.2B]
R545 [10.2E]
R546 [10.2B]
R547 [10.2B]
R548 [10.2B]
R549 [10.2B]
R550 [13.3D]
R551 [13.3D]
R552 [13.4D]
R553 [12.3E]
R554 [13.3C]
R555 [13.4B]
R556 [12.4B]
R557 [12.5C]
R558 [13.4E]
R559 [12.5C]
R560 [12.4C]
R561 [12.4D]
R562 [12.5C]
R563 [12.5F]
R564 [12.3C]
R565 [12.5G]
R566 [12.5G]

R567 [12.5G]
R568 [13.4A]
R569 [12.3F]
R570 [13.4A]
R571 [9.4E]
R572 [9.4E]
R573 [12.3F]
R574 [8.4E]
R575 [12.4C]
R576 [8.4E]
R577 [8.3G]
R578 [8.3D]
R579 [7.4E]
R580 [5.4E]
R581 [6.2D]
R582 [7.4E]
R583 [5.4E]
R584 [6.3D]
R585 [5.5E]
RP1 [10.2B 10.2B 10.2B 10.2B]
RP2 [3.4H 3.4G 3.4H 3.4G]
RP3 [3.4F 3.4G 3.4G 3.4F]
RP4 [3.4H 3.4H 3.4G 3.4G]
RP5 [3.3F 3.3F 3.3F 3.3F]
RP6 [3.4F 3.3G 3.3G 3.4F]
RP7 [3.4F 3.4F 3.4F 3.4F]
RP8 [3.3G 3.3H 3.3G 3.3H]
RP9 [3.3G 3.3H 3.3G 3.3H]
RP501 [3.2G 3.2G 3.2H 3.2H]
RP502 [3.5H 3.5H 3.4F 3.4F]
RP503 [3.3H 3.4F 3.3H 3.4F]
RP504 [3.4H 3.3H 3.3H 3.4H]
RP505 [3.3G 3.4H 3.4H 3.3G]
TP501 [3.4D]
TP502 [10.2C]
TP503 [10.2C]
U1 [5.3D 5.3D]
U1 [6.3D 6.3D]
U2 [12.2B]
U3 [13.1E]
U501 [10.3G]
U502 [10.4G]
U503 [10.2G]
U504 [12.4D]
U505 [13.3C]
U506 [12.3G]
Y1 [10.5D]

0001246903 FOR
MSL 精简非 RMA 丁德基
CONFIDENTIAL
RD(C)20110714003
ONLY

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	<edit here to insert page detail>

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME	<ENGINEER>	DATE	01-DEC-2008