PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI

Tall DVI-I + DP + DP + DP/HDMI + DP

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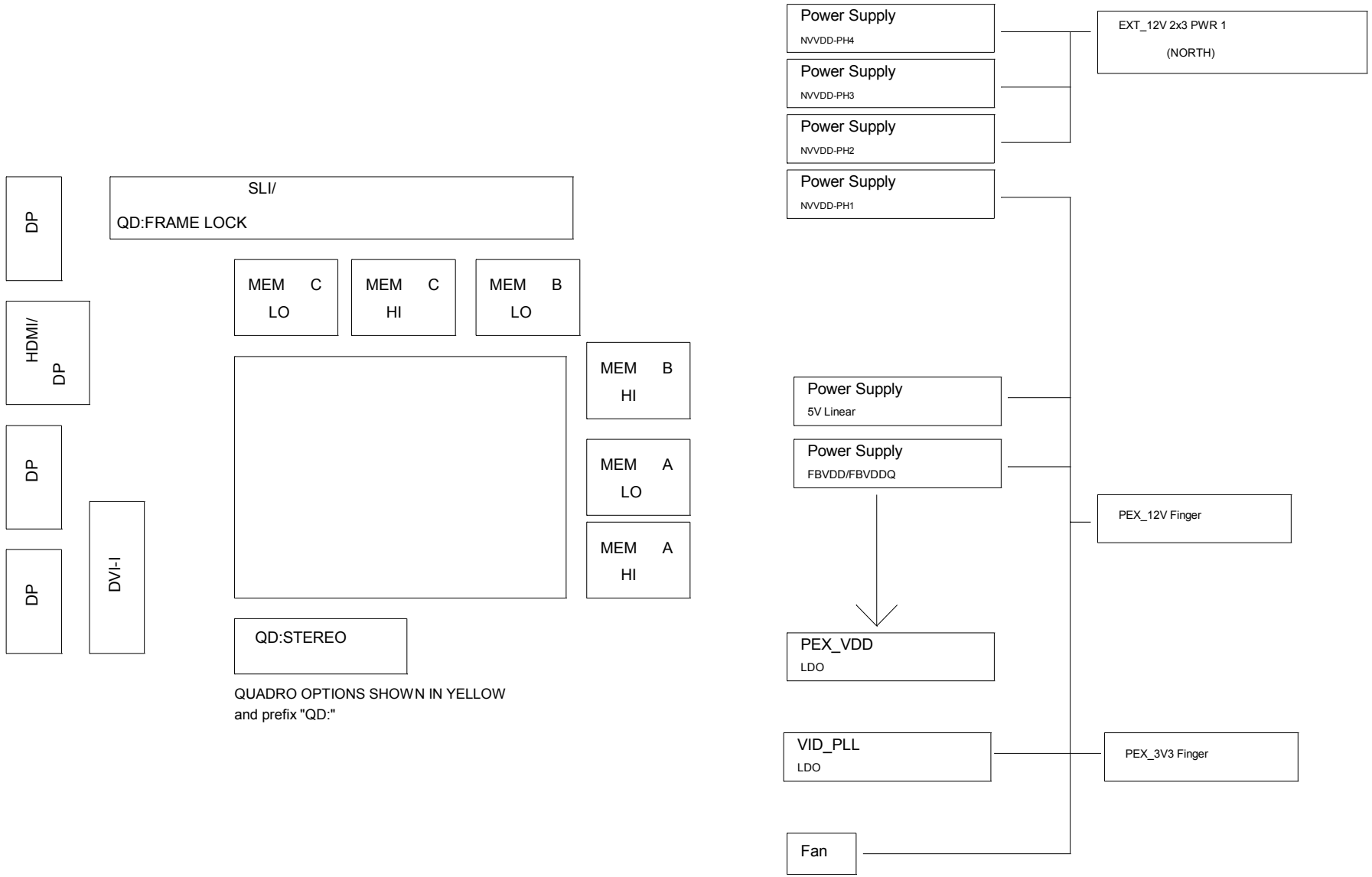
Block Diagram



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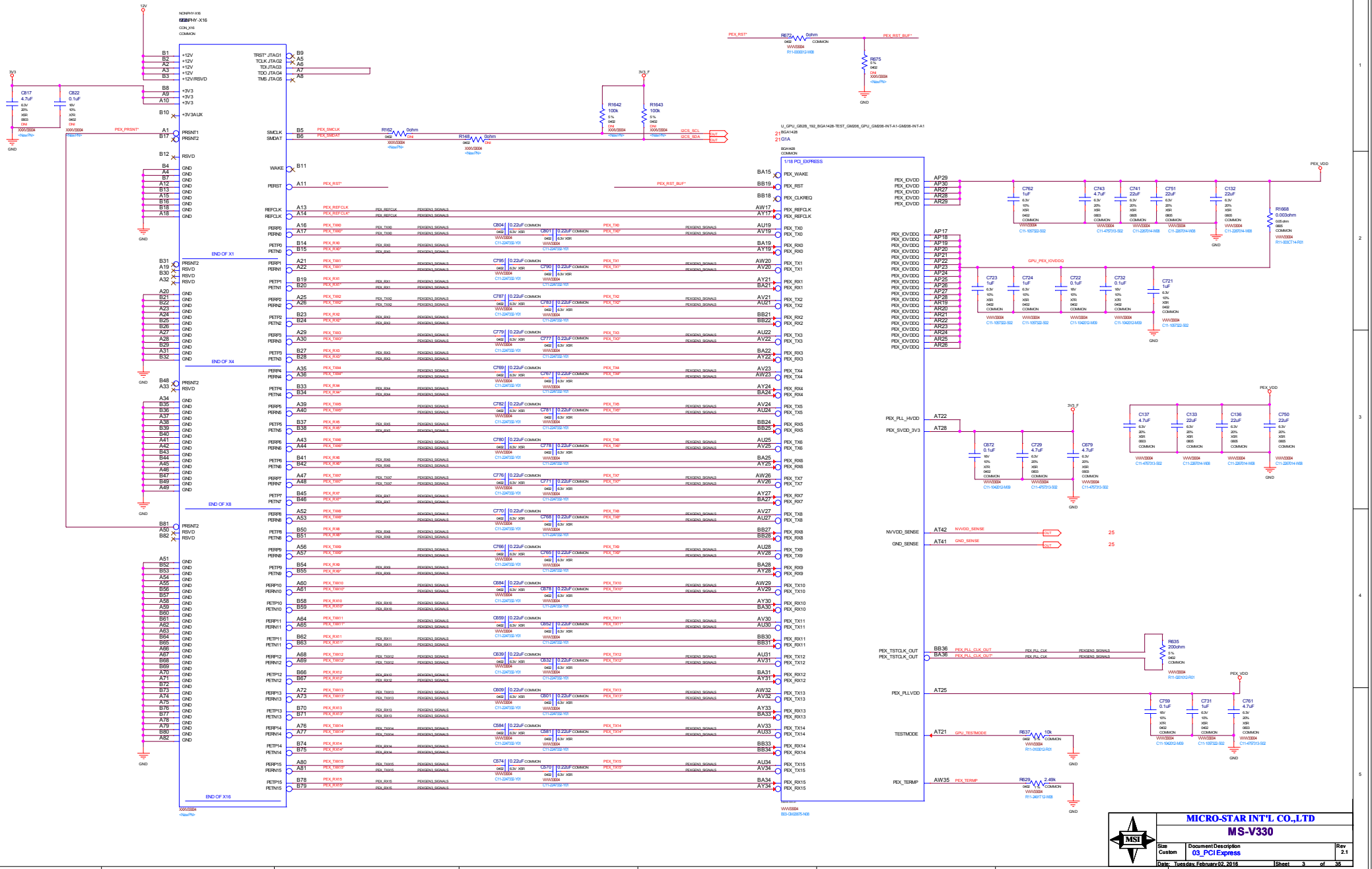
PCI Express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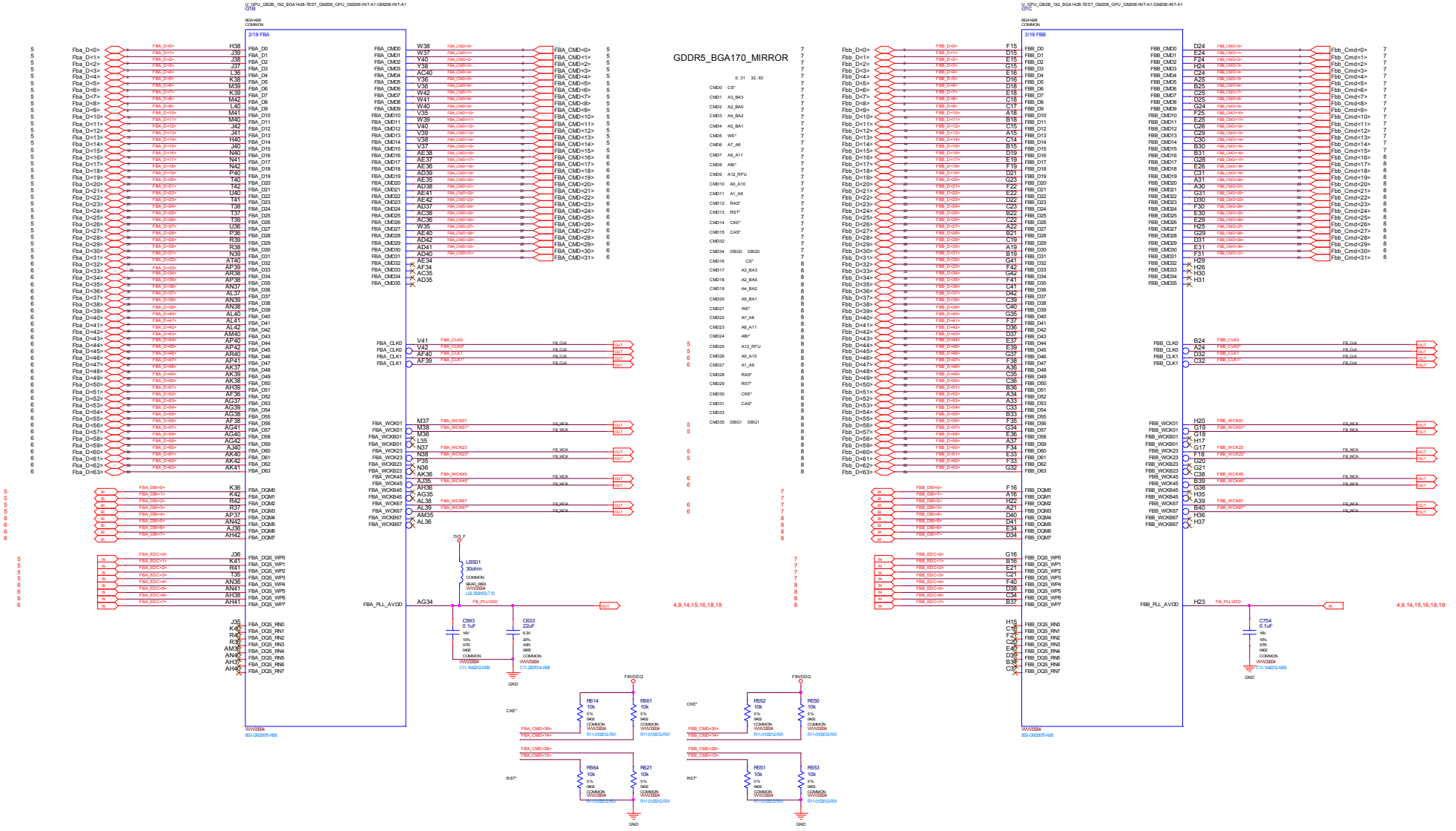
MEMORY: GPU Partition A/B



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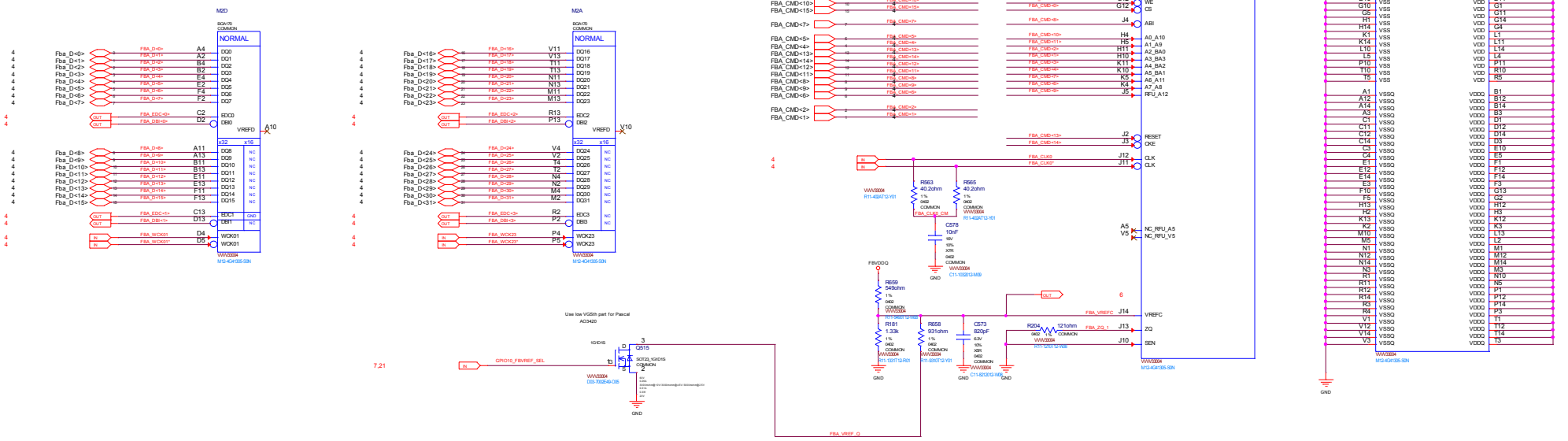
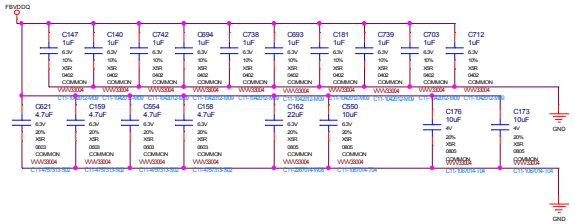
MEMORY: FBA Partition 31..0





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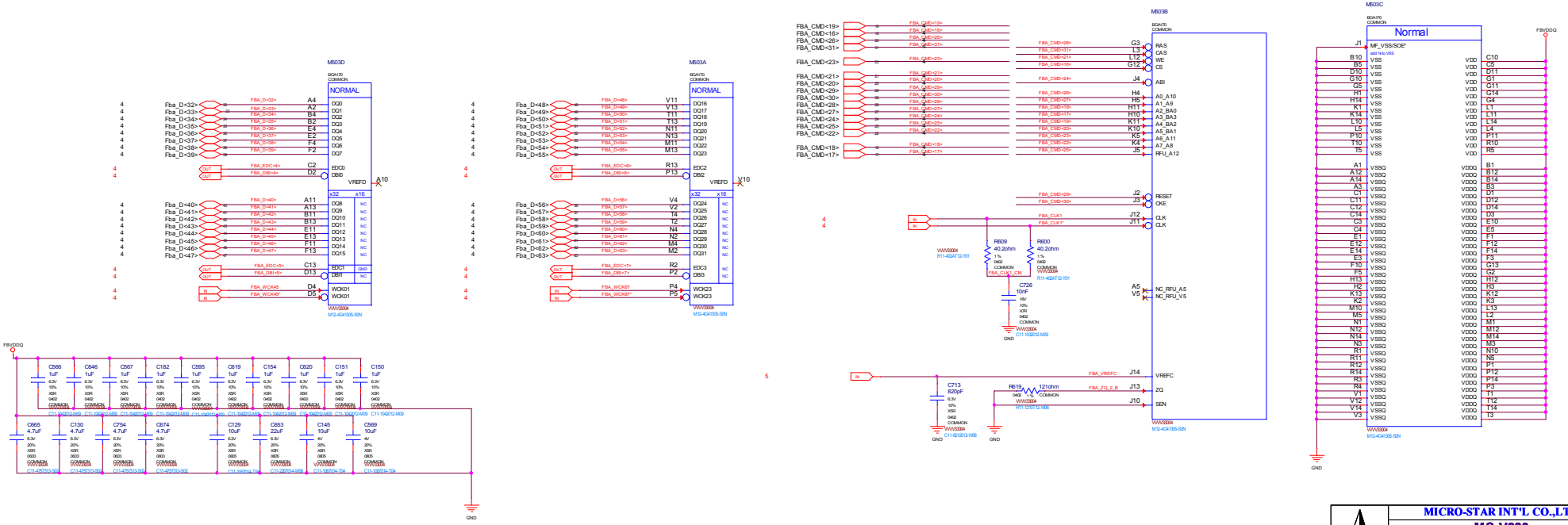
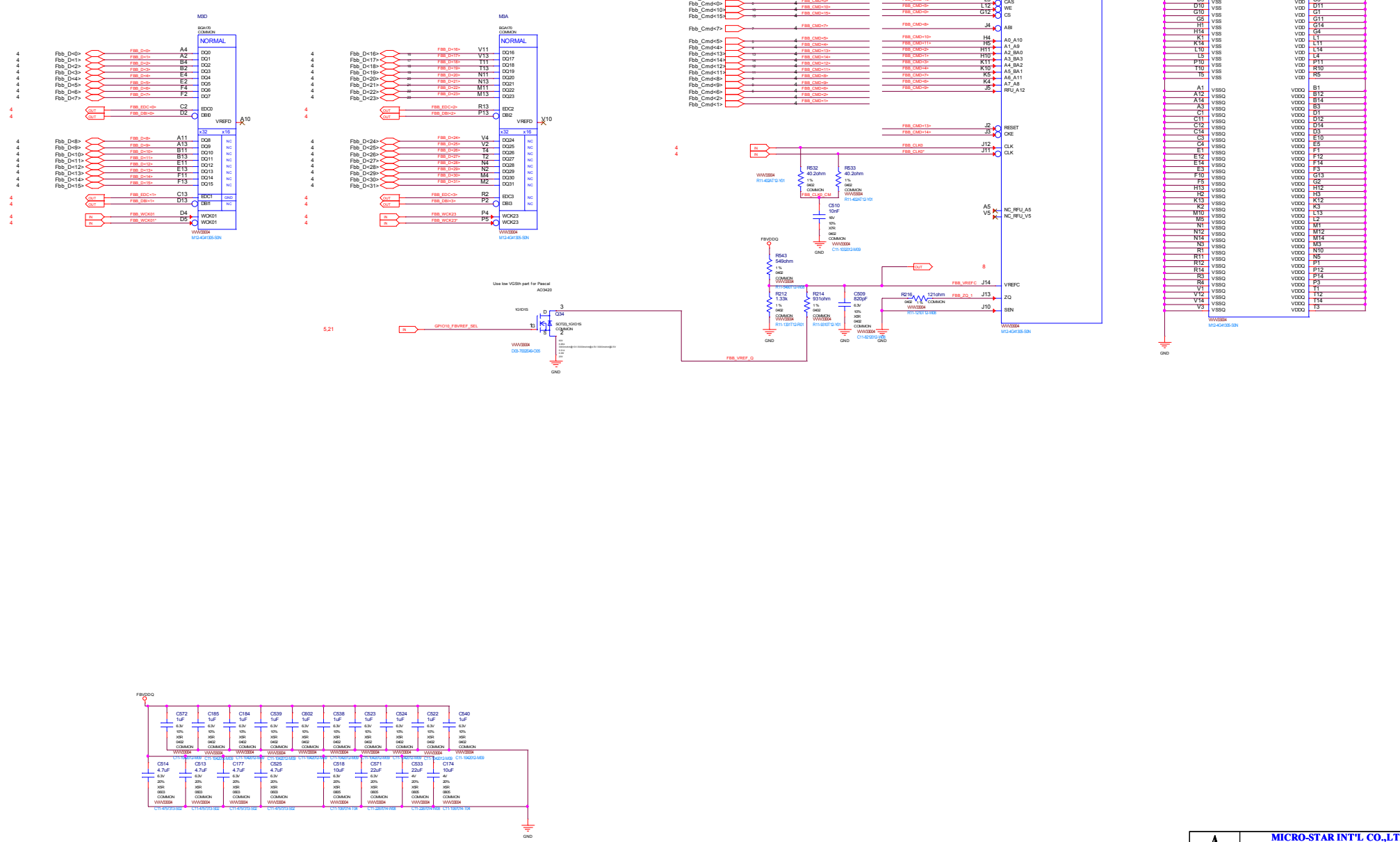
MEMORY: FBA Partition 63..32



MEMORY: FBB Partition 31..0



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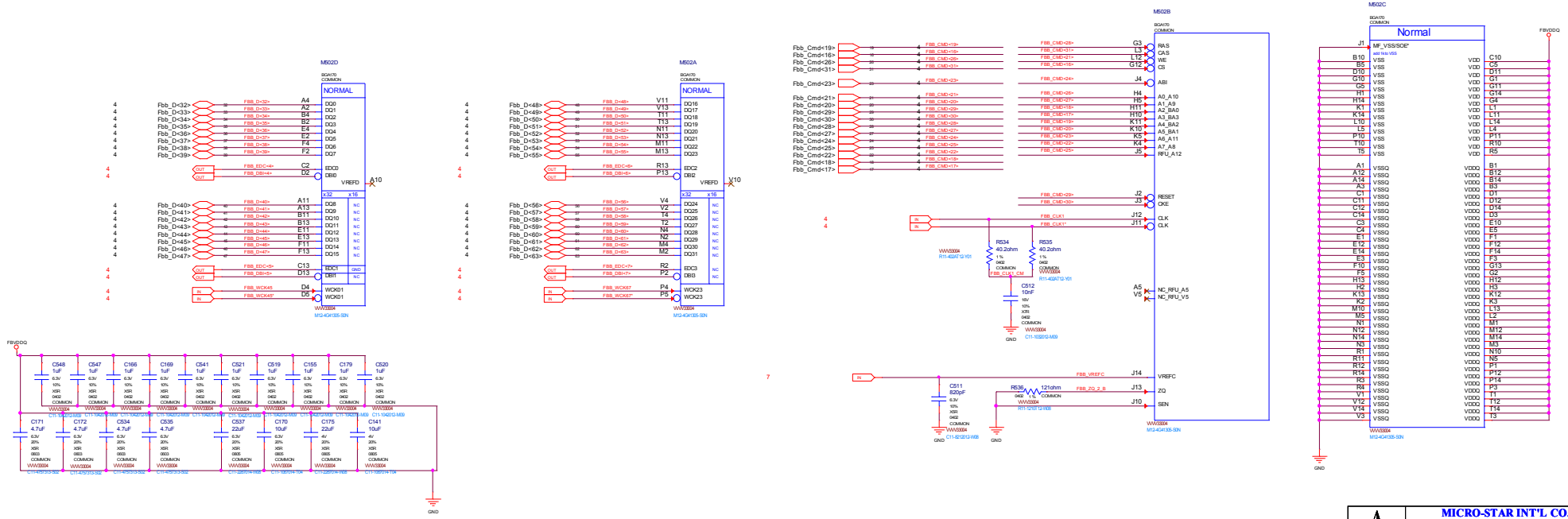
MEMORY: FBB Partition 63..32



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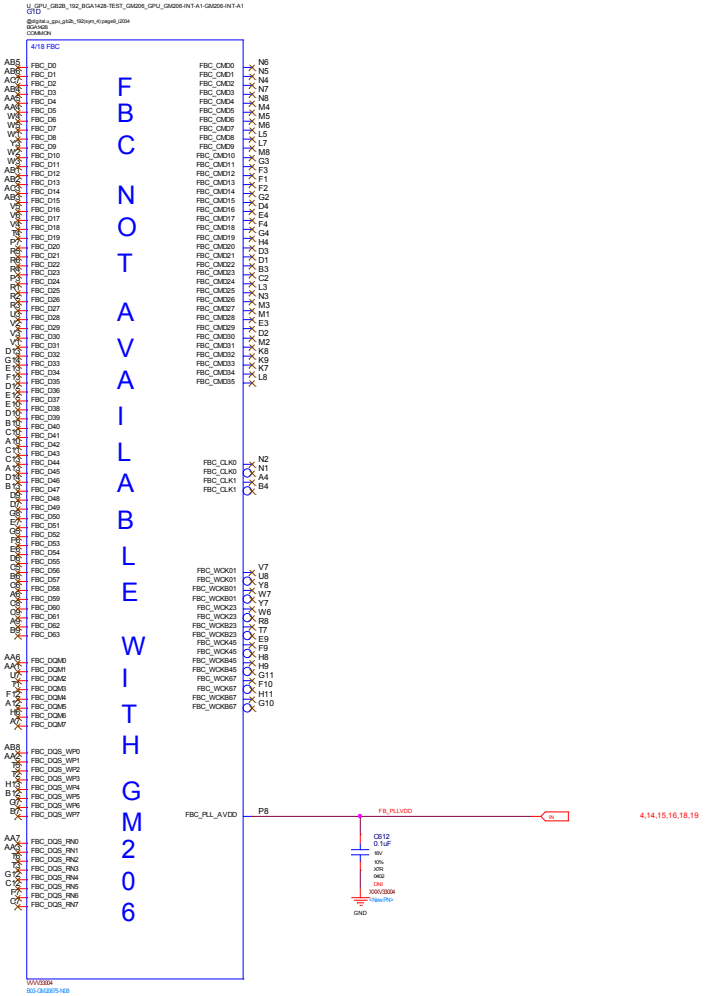
MEMORY: GPU Partition C/D



GDDR5_BGA170_MIRROR

	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD32		
CMD34	DBG0	DBG0
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*
CMD33		
CMD35	DBG1	DBG1

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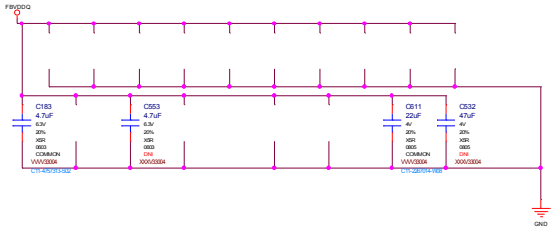
MEMORY: FBC Partition 31..0



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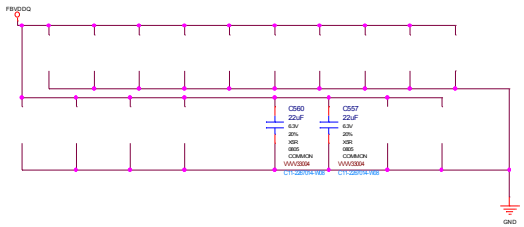
MEMORY: FBC Partition 63..32



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Size	Document Description	Rev
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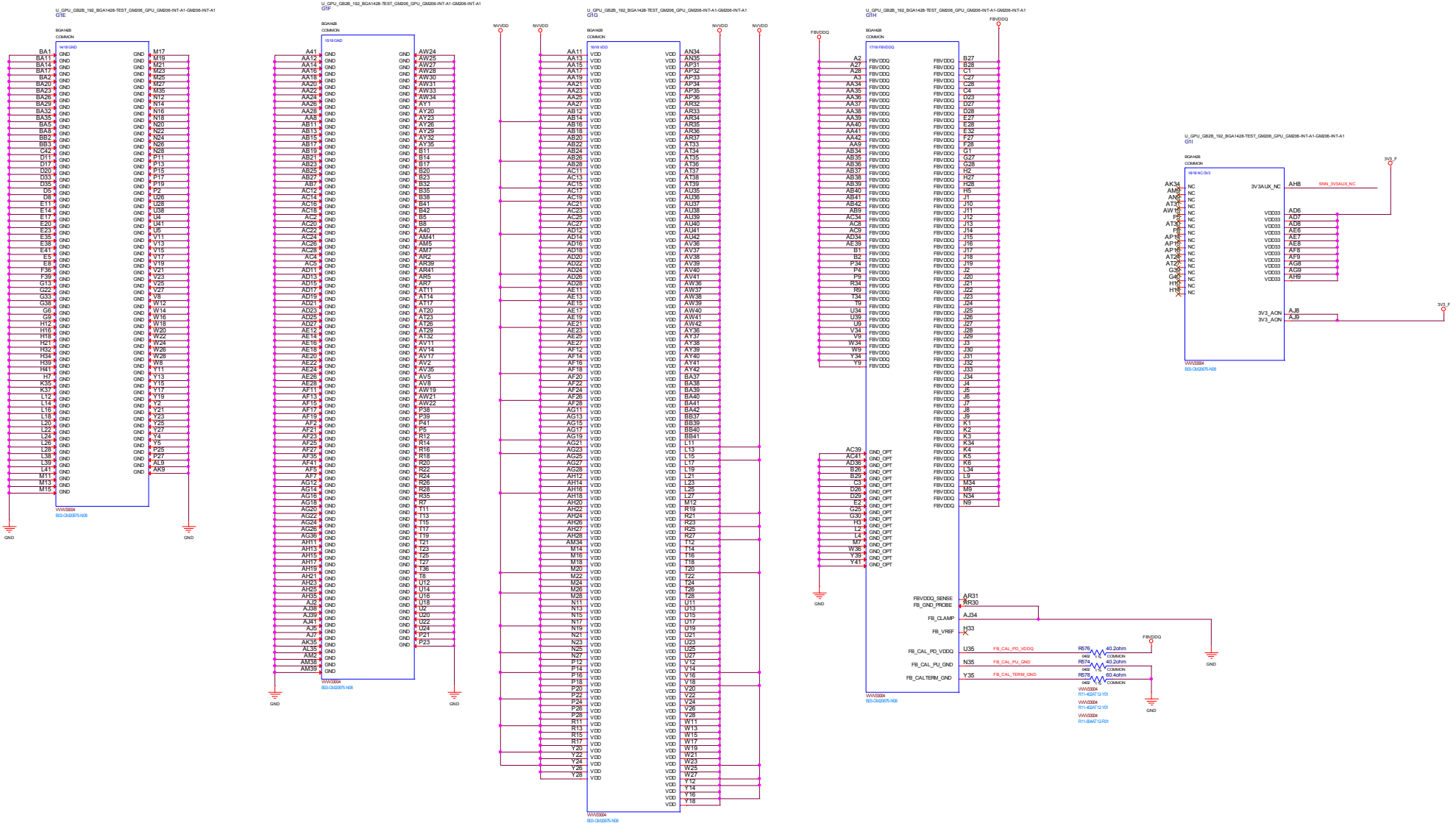
GPU PWR and GND



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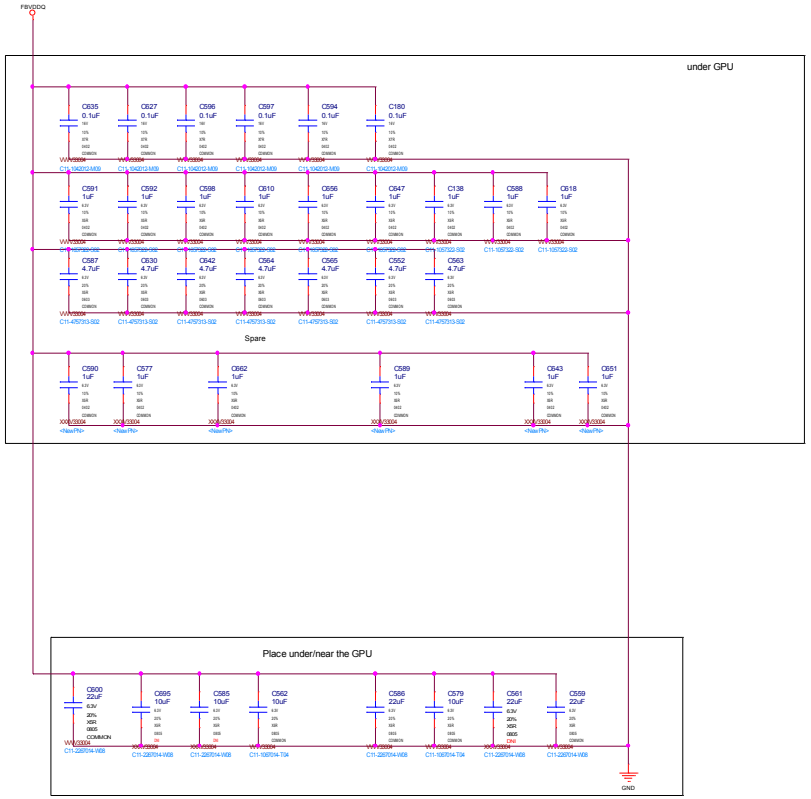
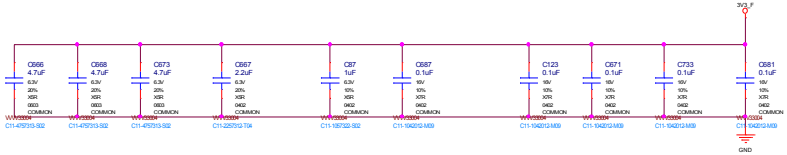
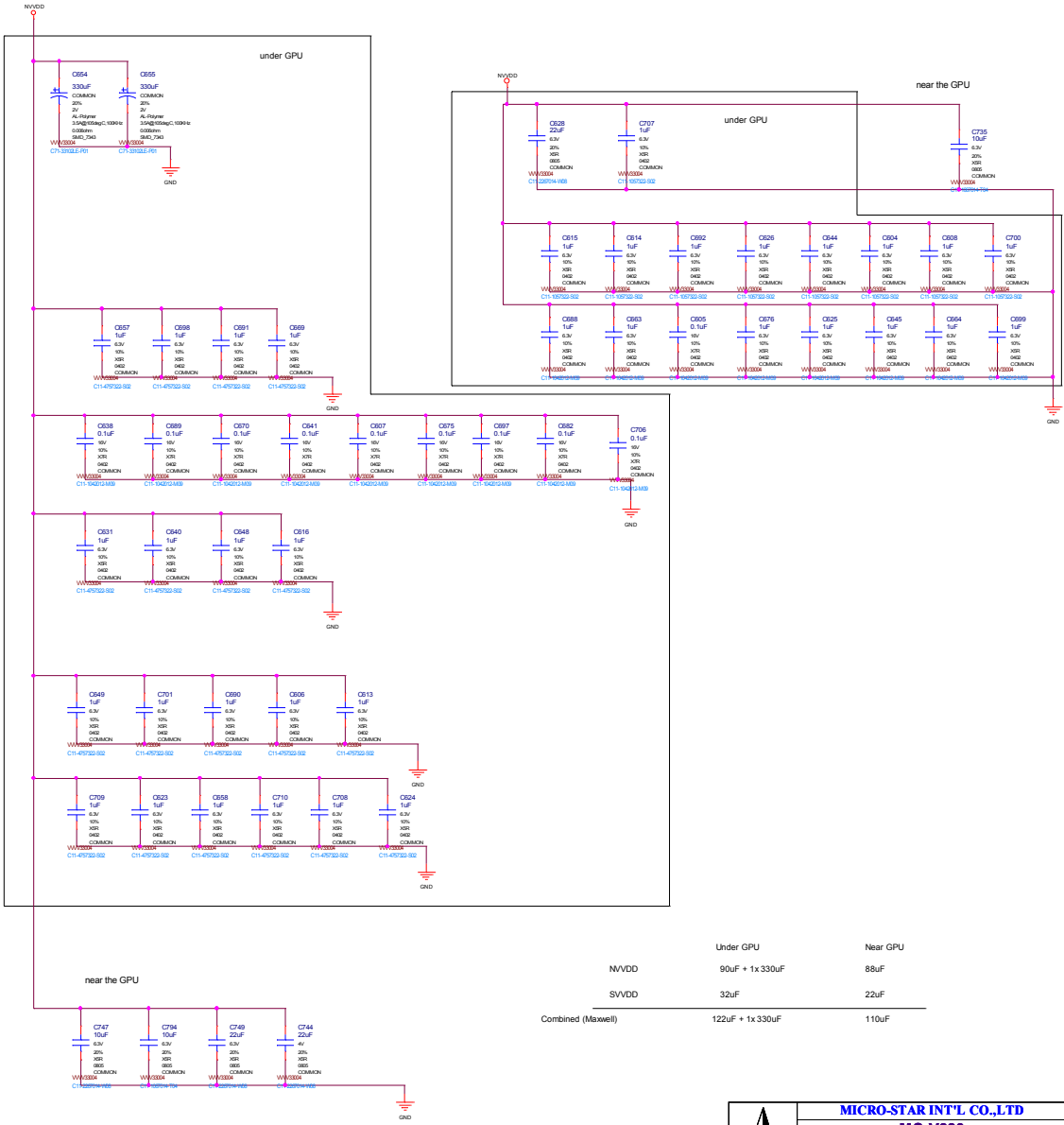
GPU Decoupling

FBVDDQ





NVVDD



	Under GPU	Near GPU
NVVDD	90uF + 1x 330uF	88uF
SVVDD	32uF	22uF
Combined (Maxwell)	122uF + 1x 330uF	110uF

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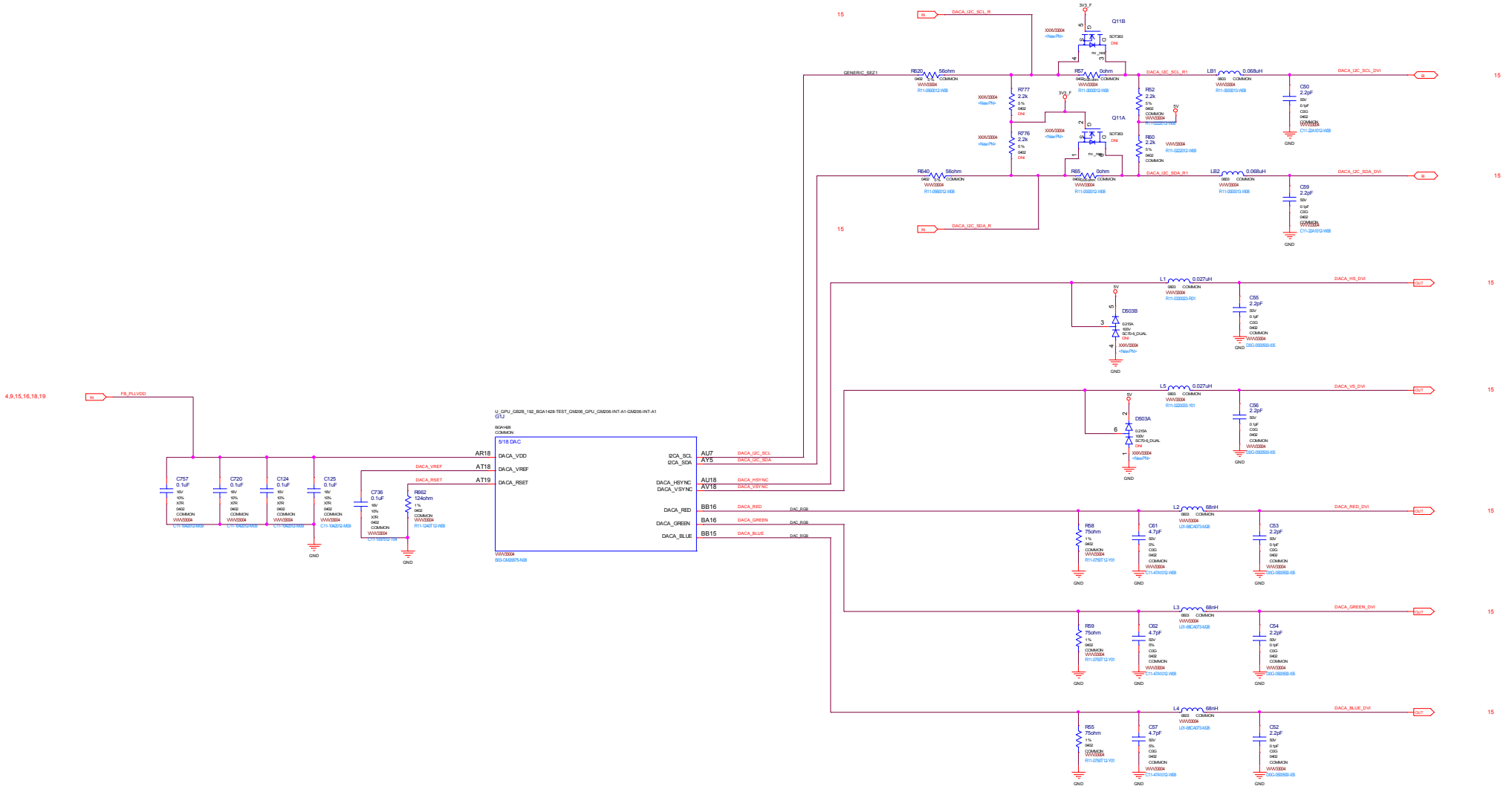
DACA Interface



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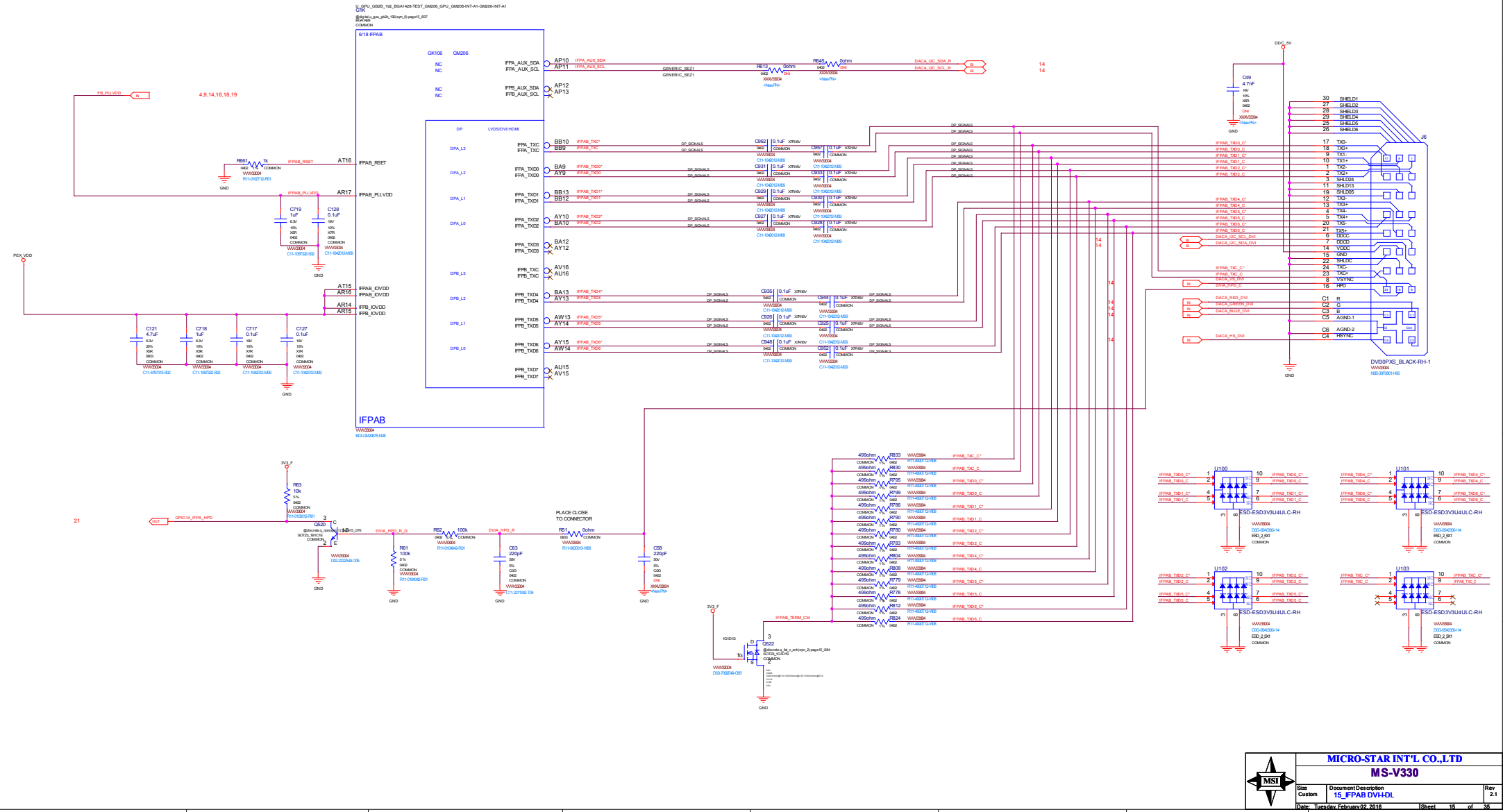
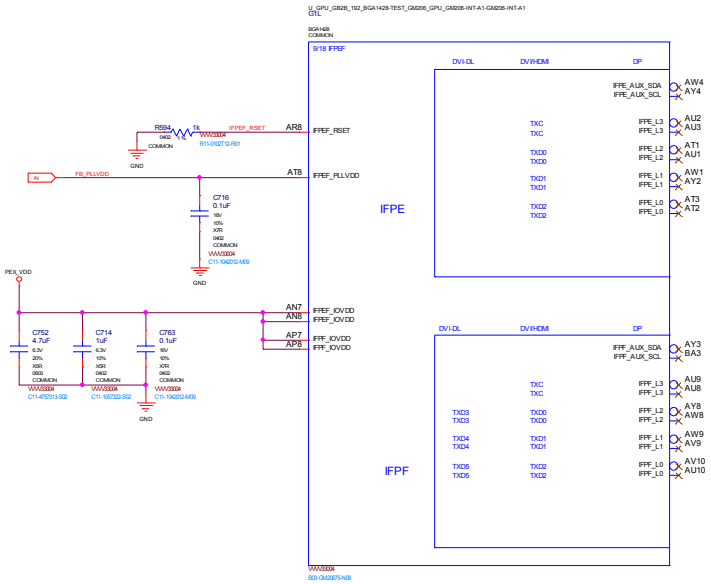
IFPAB DVI-I-DL



Page18: IFPEF with IFPE DP



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IFPF DP

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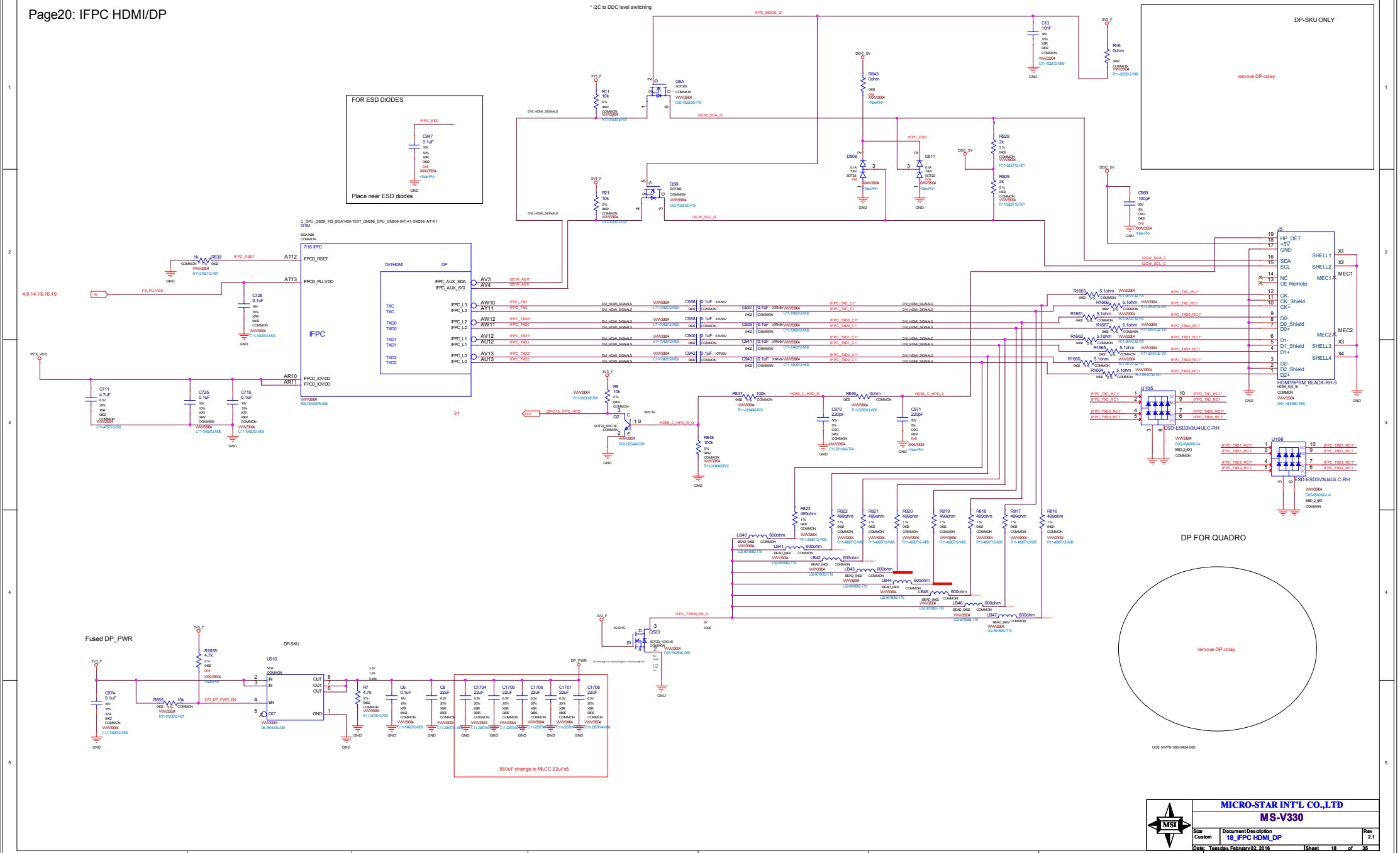
Page20: IFPC HDMI/DP



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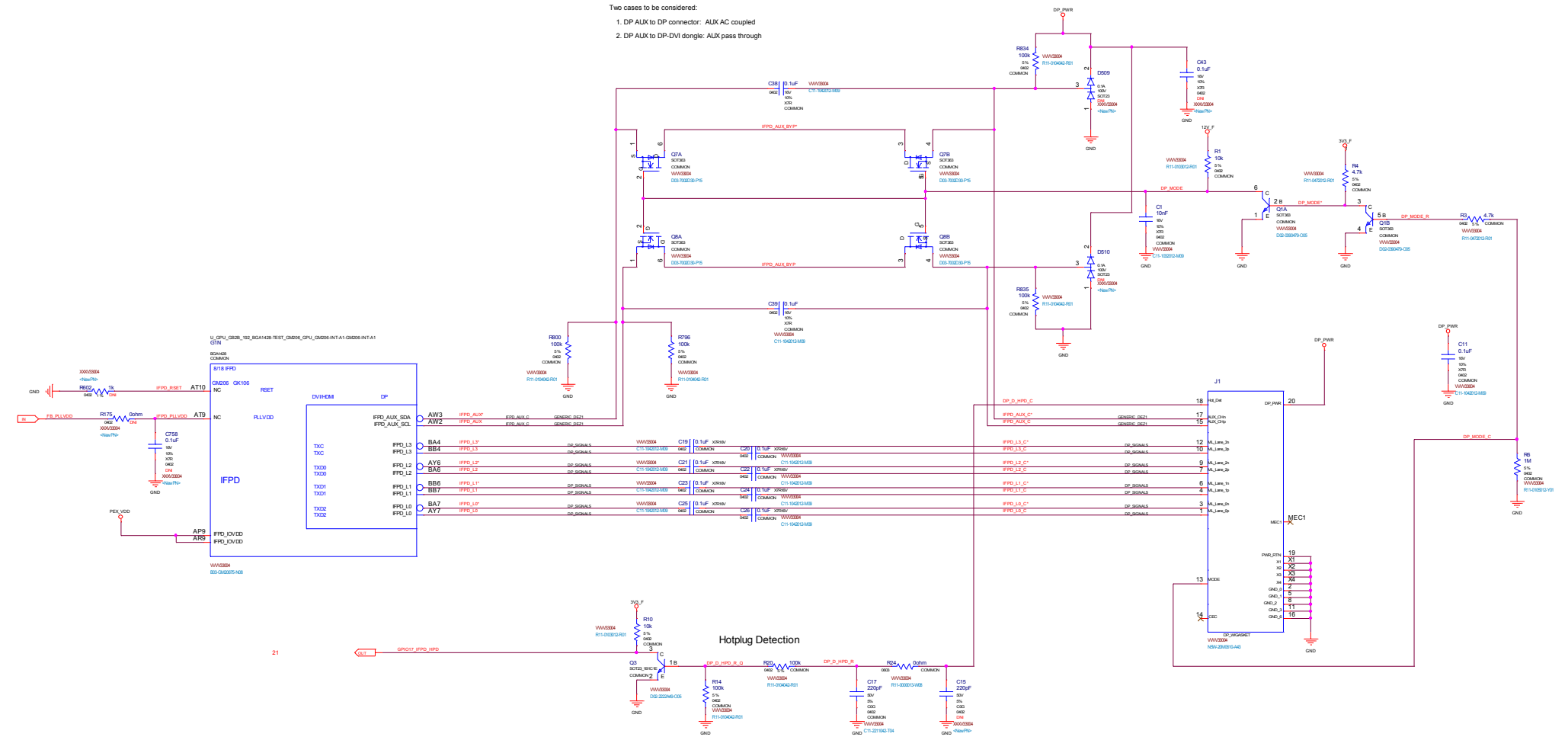
IFPD DP



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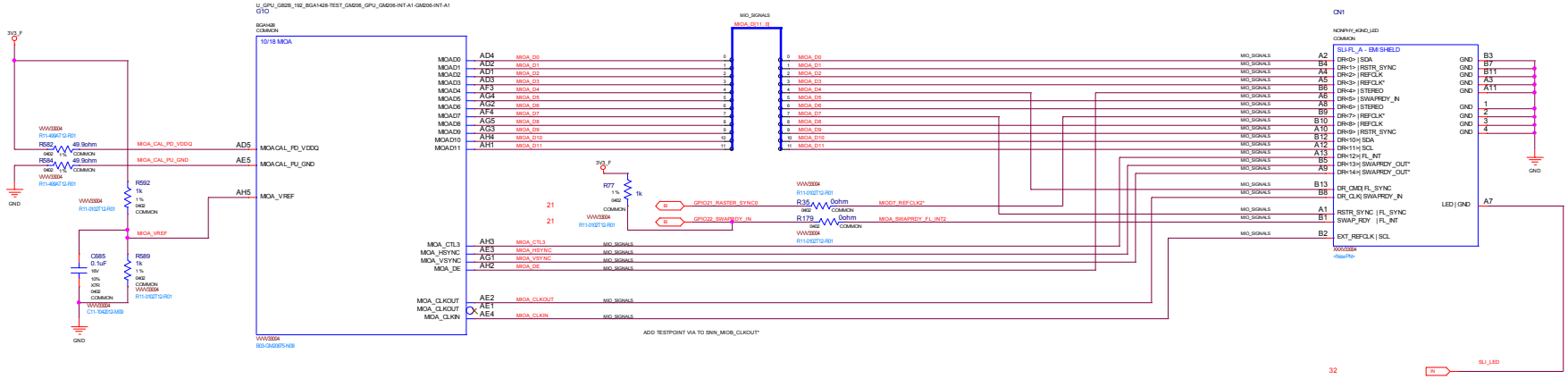
MIOA/SLI Interface



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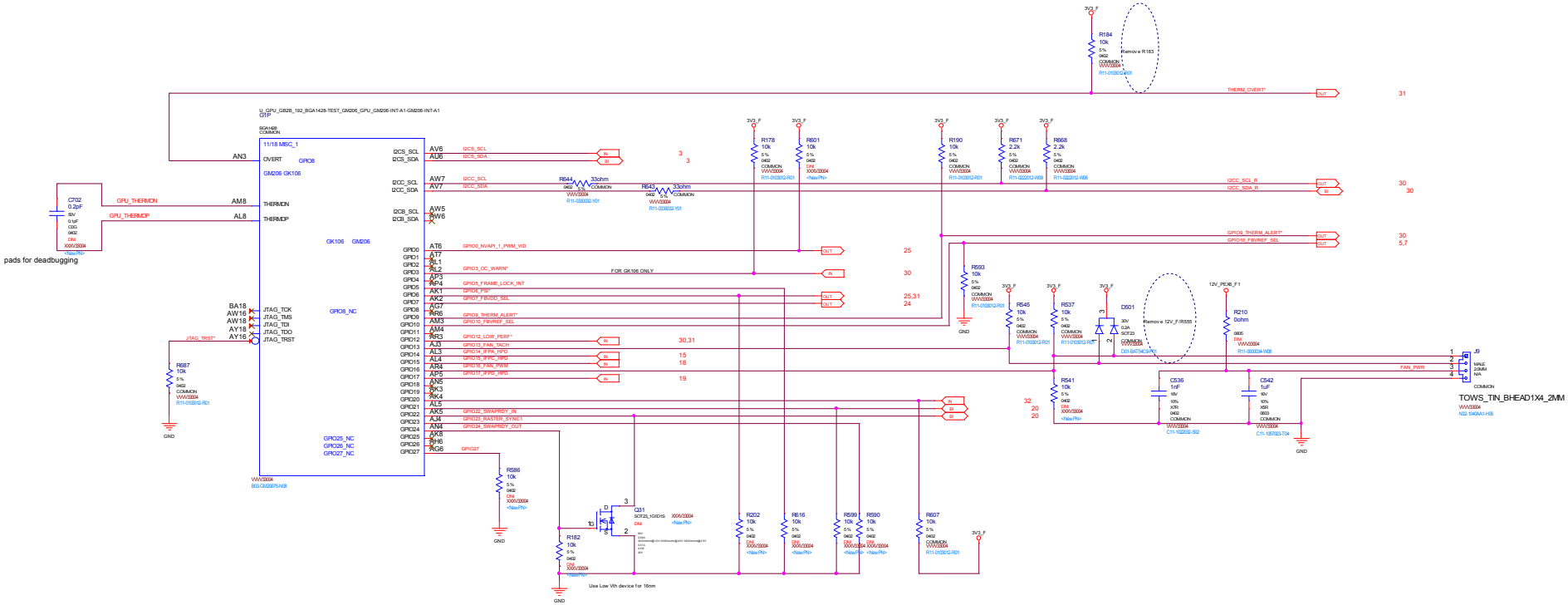
MISC1: Fan, Thermal, JTAG, GPIO



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MISC2: ROM, XTAL, Straps

	KEPLER	MAXWELL
STRAP0	USER_BIT [3:0]*	
STRAP1	3GIO_PADCFG_LUT_ADR*	
STRAP2	PCI_DEVID [3:0]*	
STRAP3	SOR_EXPOSED [3:0]*	
STRAP4	DP_PLL_VDD_33V*	
	PEX_MAX_SPEED*	
	PEX_SPD_CHANGE_GEN3*	
	*	
ROM_SI	RAMCFG[0]*	RAMCFG[0]*
	RAMCFG[1]*	RAMCFG[1]*
	RAMCFG[2]*	RAMCFG[2]*
	RAMCFG[3]*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	VGA_DEVICE*
	SMB_ALT_ADDR*	SMB_ALT_ADDR*
	FB[0]_APERTURE_SIZE*	PCIE_CFG*
	FB[1]_APERTURE_SIZE*	DEVID_SEL*
ROM_SCLK	PEX_PLL_EN_TERM100*	SOR0_EXPOSED*
	PCI_DEVID_EXT[5]*	SOR1_EXPOSED*
	SUB_VENDOR*	SOR2_EXPOSED*
	PCI_DEVID_EXT[4]*	SOR3_EXPOSED*

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

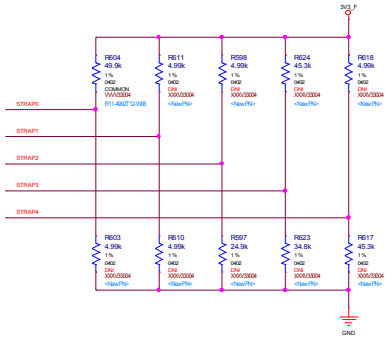
MULTI_STRAP_REF0_GND

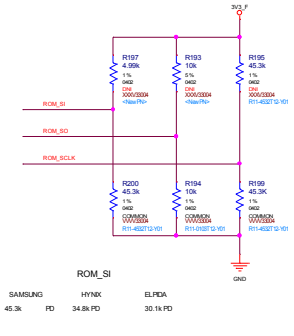
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND

MAXWELL

STRAP0

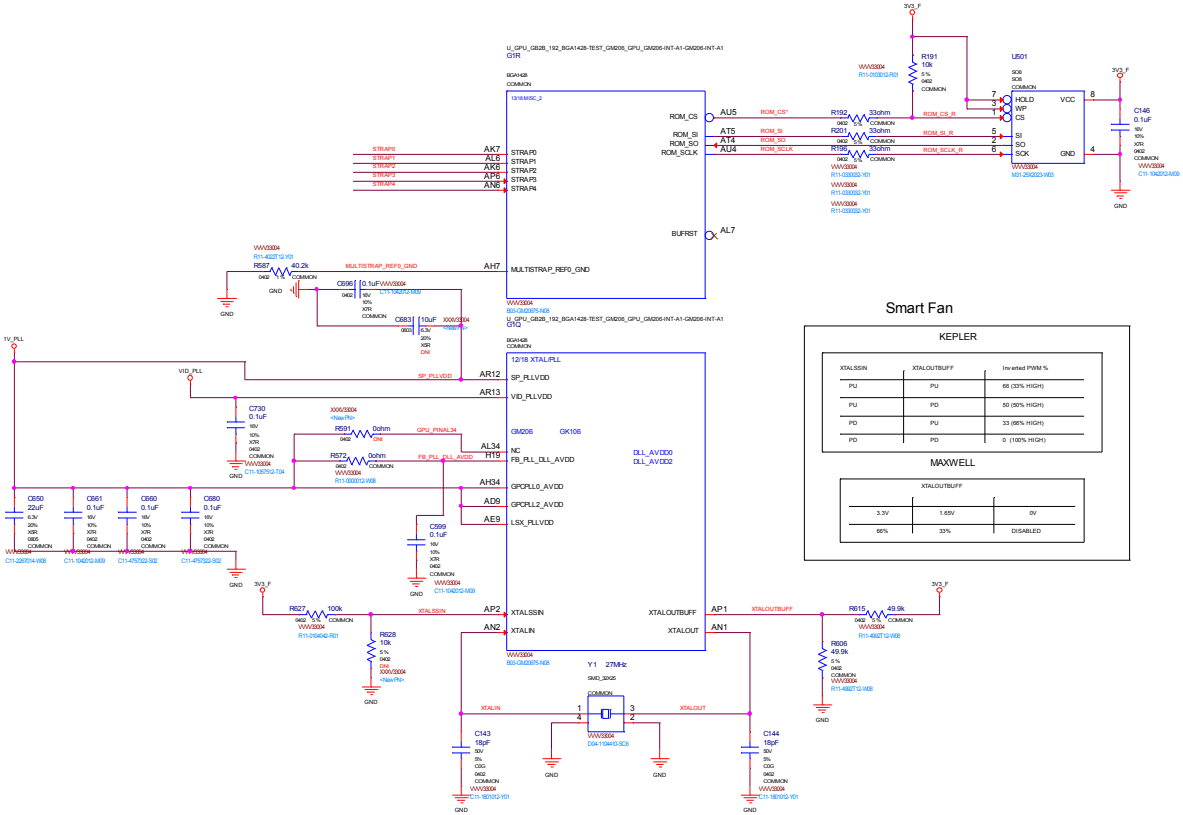
3.3V	1.65V	0V
GC6+ ISLAND ENABLED	GC6+ DEBUG MODE	GC6+ ISLAND DISABLED





ROM_SI

SAMSUNG	HYNIX	ELPIDA
45.3k PD	34.8k PD	30.1k PD



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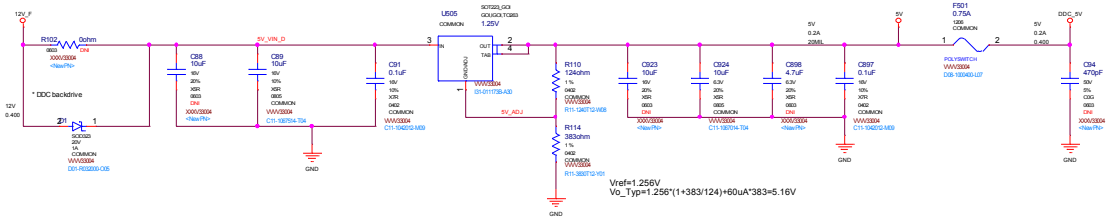
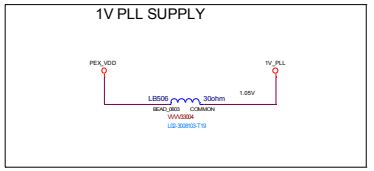
PS: 5V, PEX_VDD

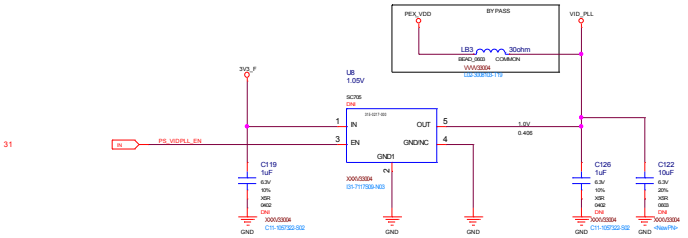
5V / DDC SUPPLY



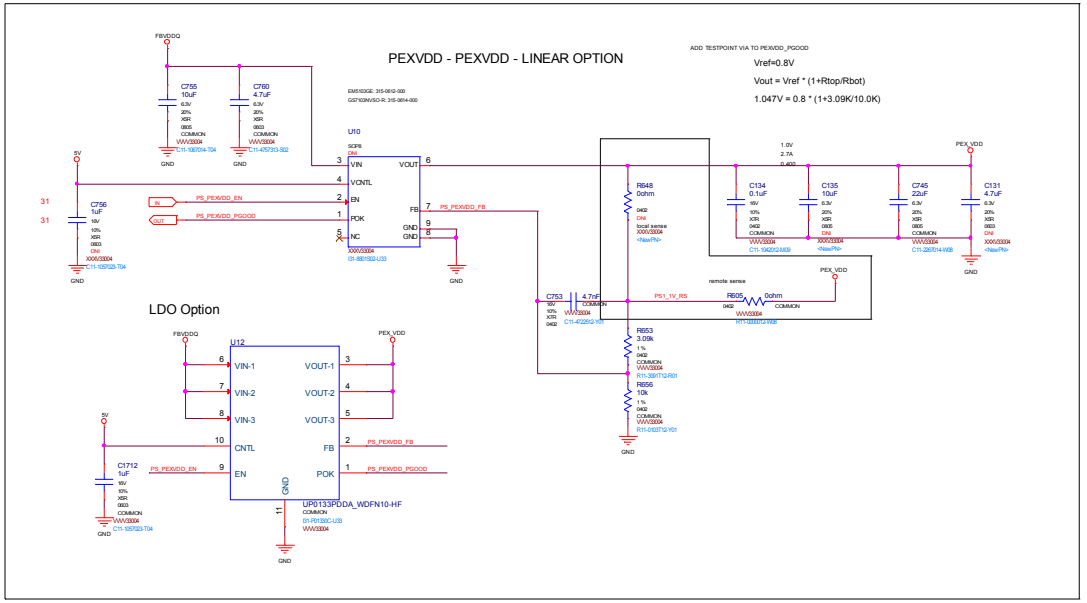
1V PLL SUPPLY



VID PLL SUPPLY



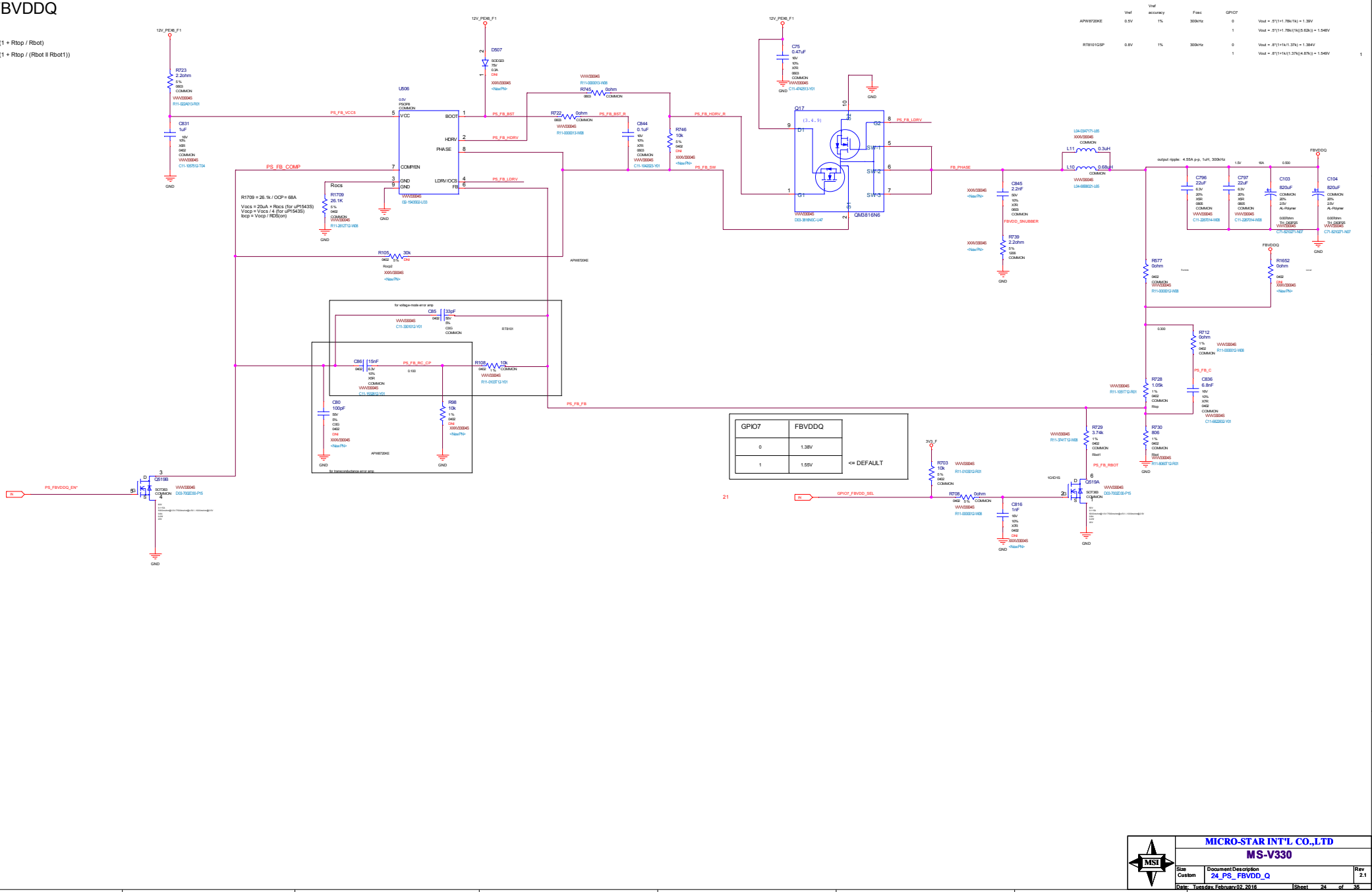
PEXVDD - PEXVDD - LINEAR OPTION



PS: FBVDDQ

Vout = Vref * (1 + Rtop / Rbot)

Vout = Vref * (1 + Rtop / (Rbot || Rbot1))



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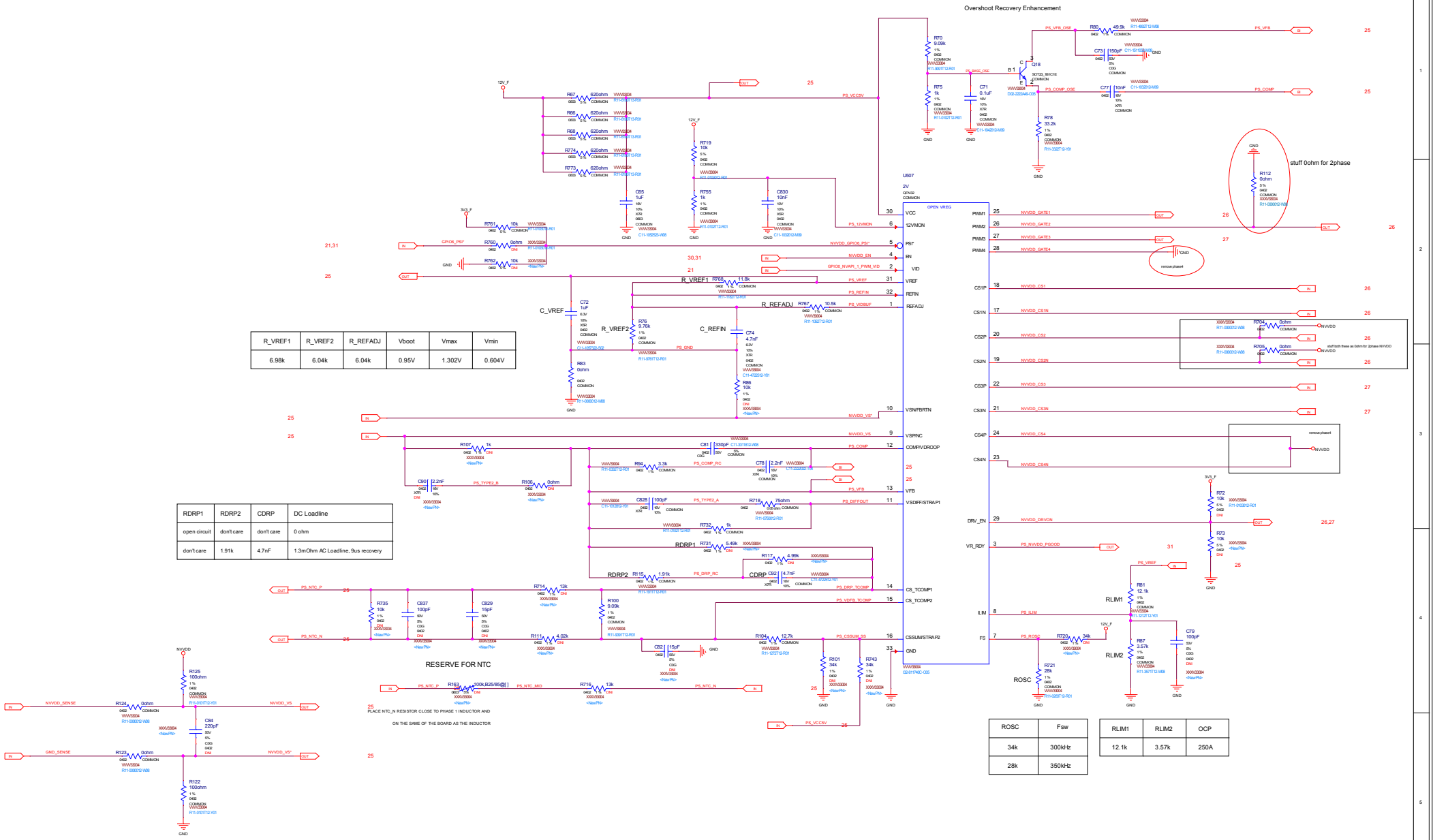
PS: NVVDD Controller



R_VREF1	R_VREF2	R_REFADJ	Vboot	Vmax	Vmin
6.98k	6.04k	6.04k	0.95V	1.302V	0.604V

RDRP1	RDRP2	CDRP	DC Loadline
open circuit	don't care	don't care	0 ohm
don't care	1.91k	4.7nF	1.3mOhm AC Loadline, 9us recovery

ROSC	Fsw
34k	300kHz
28k	350kHz

RLIM1	RLIM2	OCP
12.1k	3.57k	250A

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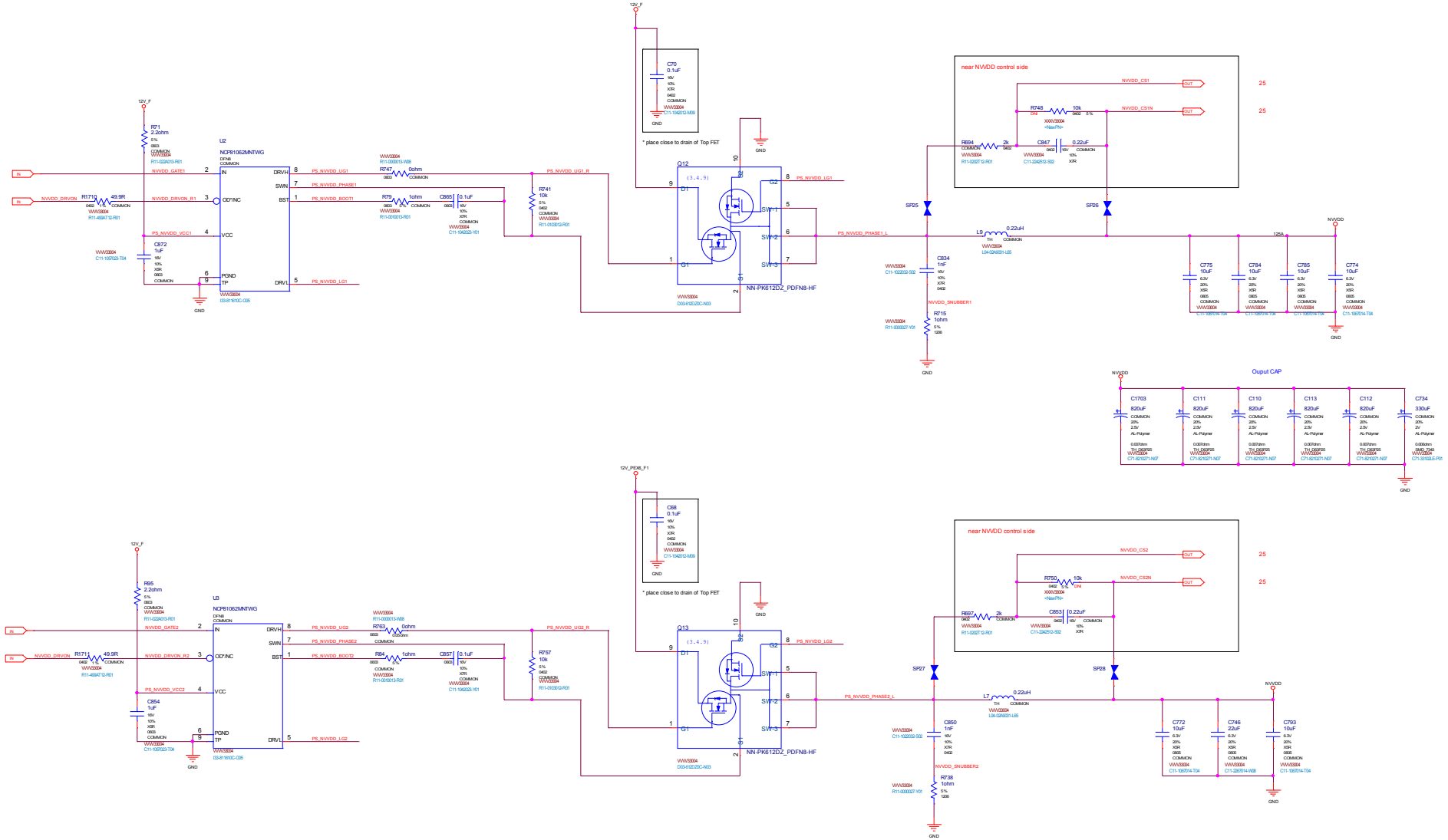
PS: NVVDD Phase 1,2



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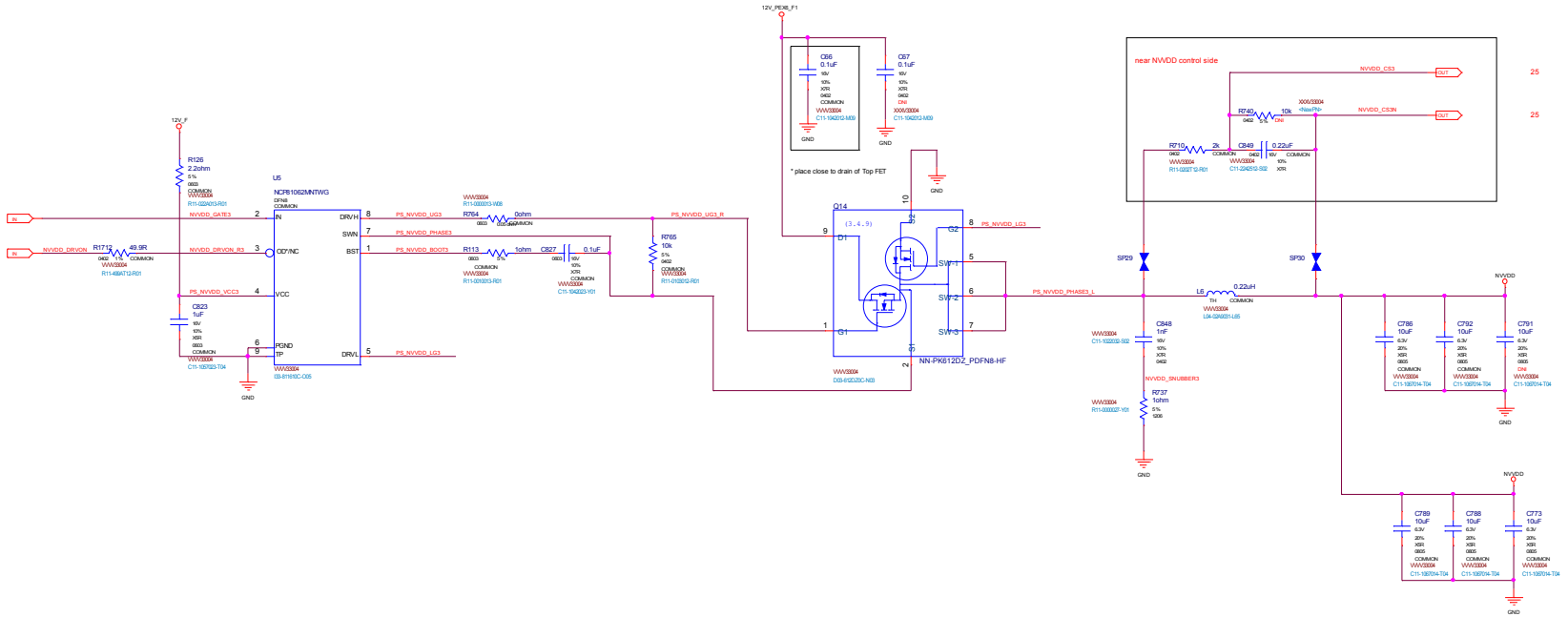
PS: NVVDD Phase 3,4



remove phase4

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[RESERVED]

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PS: NVVDD OVR2+1 POWER

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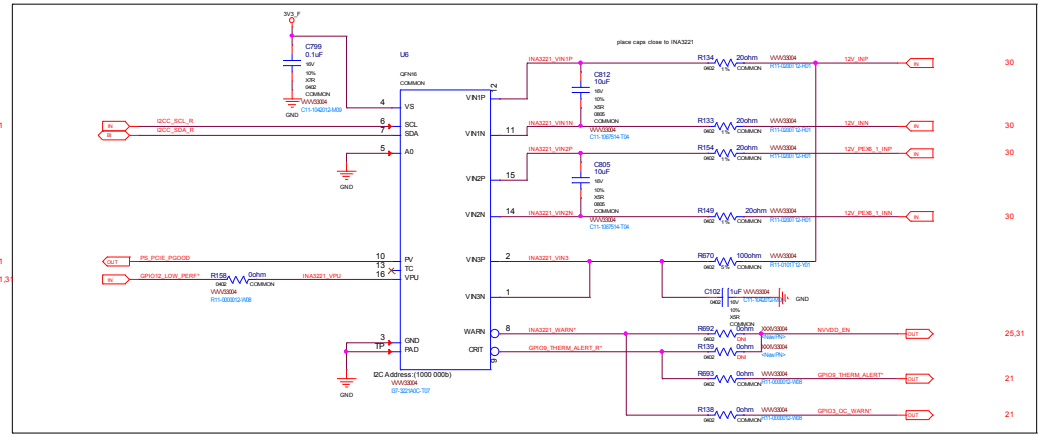
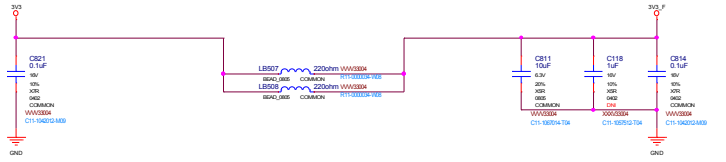
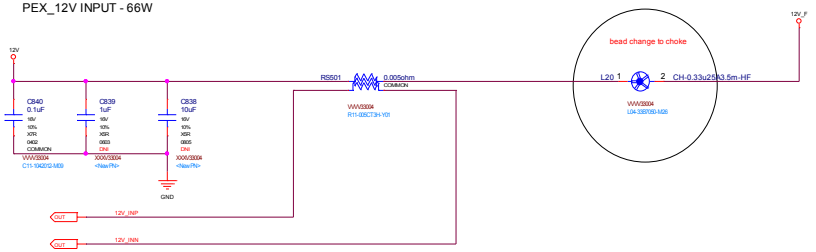
PS: Inputs, Filtering, Monitoring and 12V Current Steering



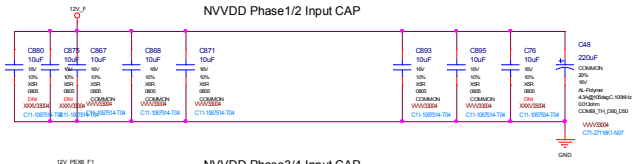
PEX 3V3 INPUT - 10W



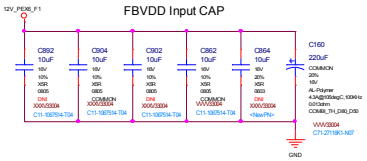
PEX_12V INPUT - 66W



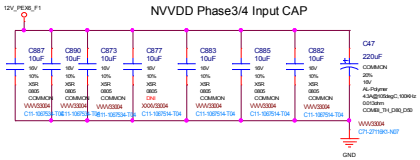
NVVDD Phase1/2 Input CAP



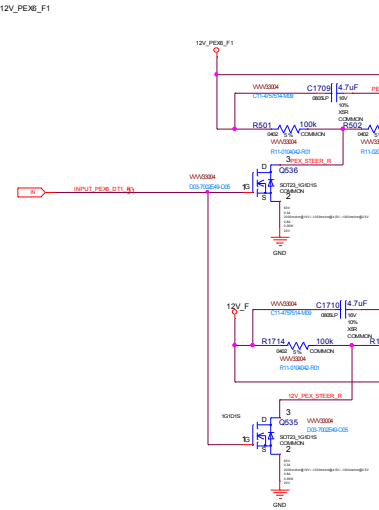
FBVDD Input CAP



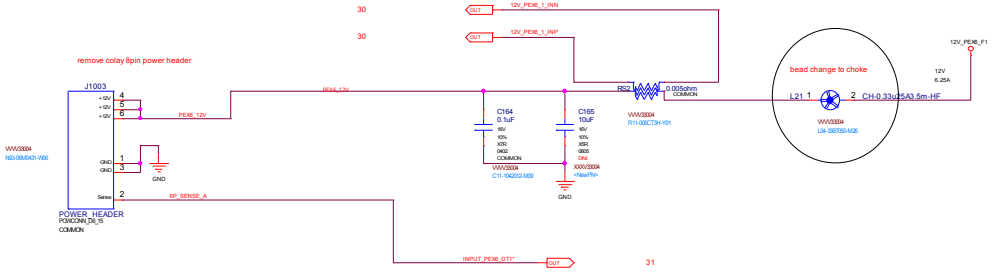
NVVDD Phase3/4 Input CAP



PEX Input - 12V Current Steering FETs



PEX6 INPUT - 2x3 PCIE CON 75W



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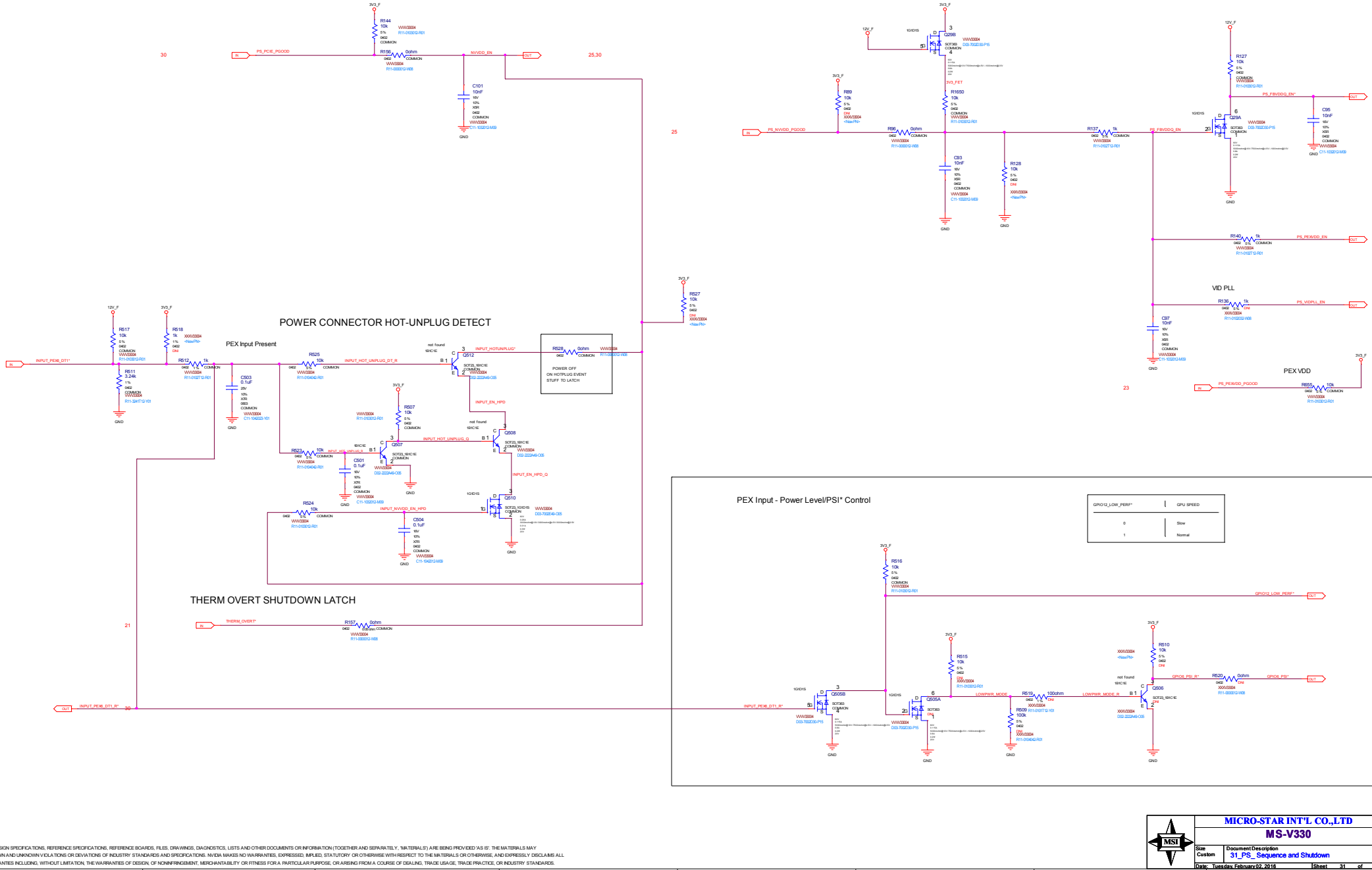
PS: Sequence and Shutdown



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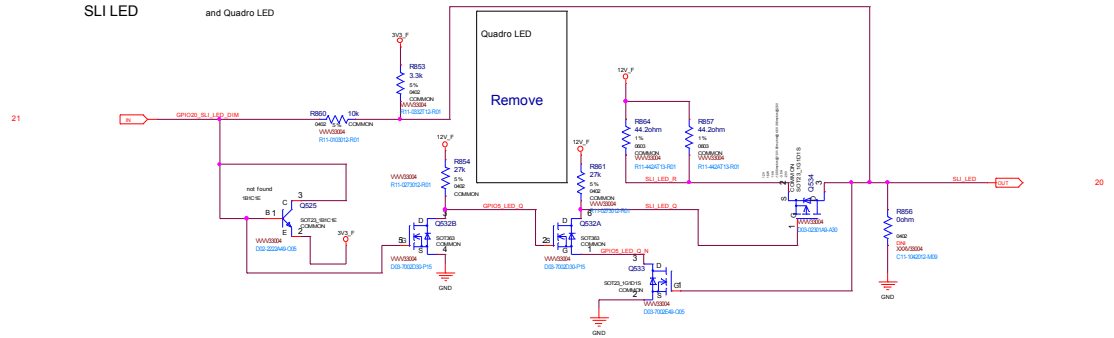
LEDs

IFP_IOVDD (backdrive prevention)

Kepler Only

Remove

SLI LED and Quadro LED



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PS: IOVDD, NV3V3, NV12V

OVR0 1.8V REGULATOR. STUFF FOR 16nm

Remove

Special Note:
1. Place [C_OUT] close to [L_OUT]
2. Use local FB sense (refer to design guide for details)
3. Place PLL/IO filter ferrite bead to the same position as FB local sense point

BYPASS. STUFF FOR 28nm

Remove

Gated rails required for 16nm

Remove

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Size	Document Description	Rev
Custom	33_PS_ IOVDD Regulator	2.1

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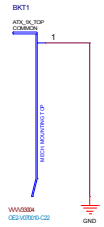
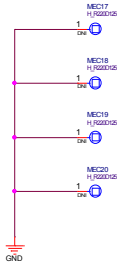
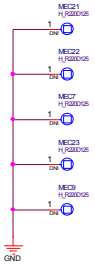
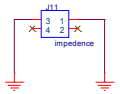
Mechanical: Bracket/Thermal Solution

Brackets:

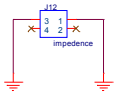




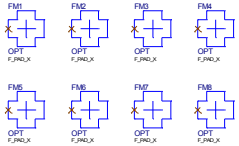




L1_D_0.12/0.101 80ohm



L4_D_0.1/0.12 90ohm



L1_S_0.126 47ohm

L4_S_0.102 52ohm

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Note:

2015/11/23	
page: 20	Remove_SLI net
page:21	ADD GPIO11_LOGO_LED NET / Remove_SLI net
page:24	預留 FBVDDQ convertor : NB685
page:25	移除第四相線路,預留關閉二相線路
page:27	移除第四相線路
page:32	新增Logo LED線路/移除SLI LED線路

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