NV11, 1/2/4MX32 DDR, RGB, INTERNAL DVI-I, TV, AGP.

PCI DEVICE ID 0X0=0X112 FOR NV11.

STRAPS: AGP4X, SIDEBAND DIS, FAST WRITE ENA, ADP BIOS, NORMAL PCIAD, 14.318MHZ
STRAP_RAM_TYPE [5:2]=1011-1MX32 DDR SDRAM

HISTORY REV. :

1) Based on P39-A00

2) Schematic changes; role rev to B00
   -remove BT device
   -strap resistor changes
   -add/remove resistors and caps
   -remove high dropout reg (u514)
  - R502 changed from 20K to 10K

3) C00:
   - Swapped LVDS signals back to "Rev A connections".

   - Hi Freq. cap arrays Decoupled to GND:
   1) SMB_CLK
   2) SMB_DAT
   3) PID2_I2C_CLK (aka I2CSCL)
   4) PID3_I2C_DAT (aka I2CSDA)
   5) PID3_I2CDAT (aka PID3)
   6) PID2_I2CCLK (aka PID2)
   7) PID1
   8) PID0

   - Added 10K, NO STUFF, from AGP_BUSY# to +3.3VSUS.

   - Connected C279 to +5VSUS.

4) D00:
   A) Power U513 from +3.3vsus instead of +3.3vrun.
   B) Changed R68 to 10K. Change R69 to 9.09K (to decrease static current draw in +2.5v regulator circuit)
   C) (layout change) Moved MVREF divider & caps (R172, R175, C424, C426) next to the RAMs
   D) Added 0-Ohm STUFF OPTION resistors for memory core FBVDD to go from either +3.3VSUS or +2.5V.
   E) Moved C836, C837, C247, C248, C270 to FBVDD
   F) Removed R166 & R126 (DFPCLK is unused)
   G) Moved pin 1 of R501 from +5vsus to +5vrun
   H) (layout change) Split 5vsus bus into +5vrun and +5vsus
   I) Added a NOSTUFF zero ohm resistor from DFP3.3V to +3.3VRUN (adds option to remove dfp regulator
   J) Added a .022uF cap in parallel with R550 (Increase power sequencing delay)
   K) Changed C57 to 330uF, d-size case
   L) Changed C828 is 330uF, d-size case
   M) (layout change) Moved IMI530 part (designator u1) to fix shorting problem
   N) (layout change) Connected J1 connector shield to ground
   O) (layout change) Connected mounting holes to ground. Don't plate inside of hole to allow for pimnut
   Q) Route VDDEN (GPIO3) to pin 166 on connector J10 (FPVCC)
   P) Added 2 Standoffs (1 metal, 1 plastic) and thermal pad per Dell's request.
   R) Connected pin 24 of J10 (ZV_PCLK) to pin B4 (VIPPCLK) on U29 (NV11)
   S) Created +5VRUN net, connect to pin 168 on J10 (+5VRUN)
   T) R155 = 357ohm, R150 is no-stuff
   U) Removed R152. Connected CHTVPIO_1 to CHTVPIO_0.
   V) Adjusted PCB form factor
   W) Changed R548 from 400K 5% to standard 390K 5%
   X) Changed R550 from 600K 5% to standard 620K 5%
   Y) Configured memory to 2Mx32-1001b (R524=NO STUFF, R523= STUFF
   Z) Changed R154, R156 to 10K.

5) E00:
   - Implemented ECO change list "P41_D00_ECOs-X02.doc" in
   current working directory:
   \\nvcorp\applied\designs\working\nv11\XXX-P0041-0000-E00
   - Sync'd up netlist with Layout.
   - Connect the S0 input of the IMISM530 to 3.3VRUN instead of CLK_VDD

6) E02:
   - Added 1000pf cap (C535) in parallel to R535 for EMI supression.
   - Changed mem termination from +3.3VRUN to +3.3VSUS. Affects R183-R186, C416

6a) E02-X01: Change C279 to no stuff per Dell request.

7) E03: Added SMD0603 foot print to the backside of board, C536 to DVI, DFP page.

{Item}\t{Quantity}\t{Reference}\t{USR DFINE}\t{PN}\t{Assembly}\t{Value}
{Assembly}{Source Package} {Value}{PN}{AVL1}{AVL2}{AVL3}{AVL4}{AVL5}

602-P0041-0000-E03

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NV11,AGP,1/2/4MX32M-DDR, TV, MFF Board

Size	CAGE Code	DWG NO	Rev
C			

Wednesday, February 21, 2001

Scale

Sheet 1 of 9

In all cases each capacitor should be low ESR/ESL and placed as close as possible to the respective rail connector pin(s).

Note: R11 18.2K = 1.5V
R11 36.5K = 1.9V

NVXX HOST INTERFACE

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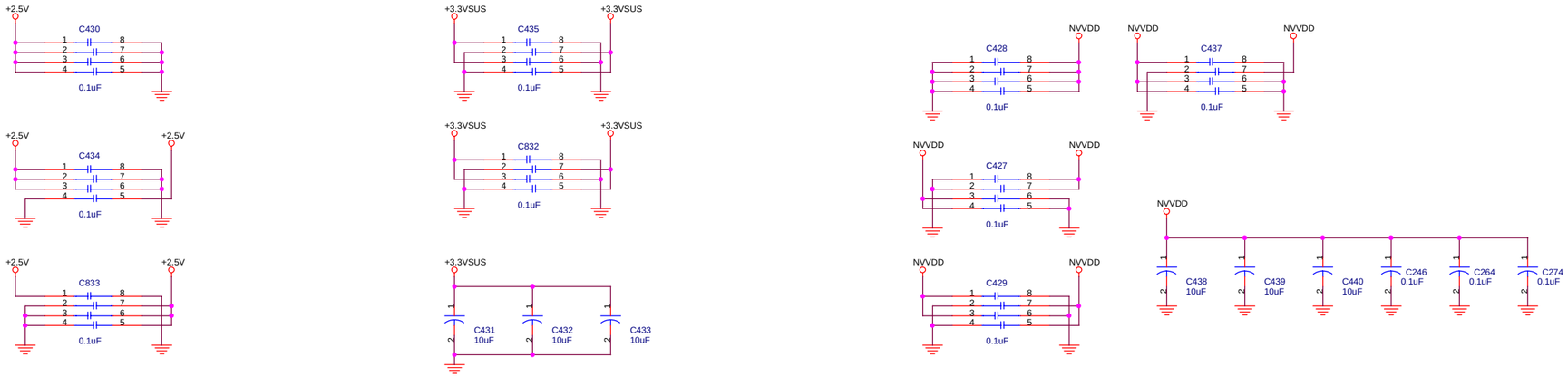
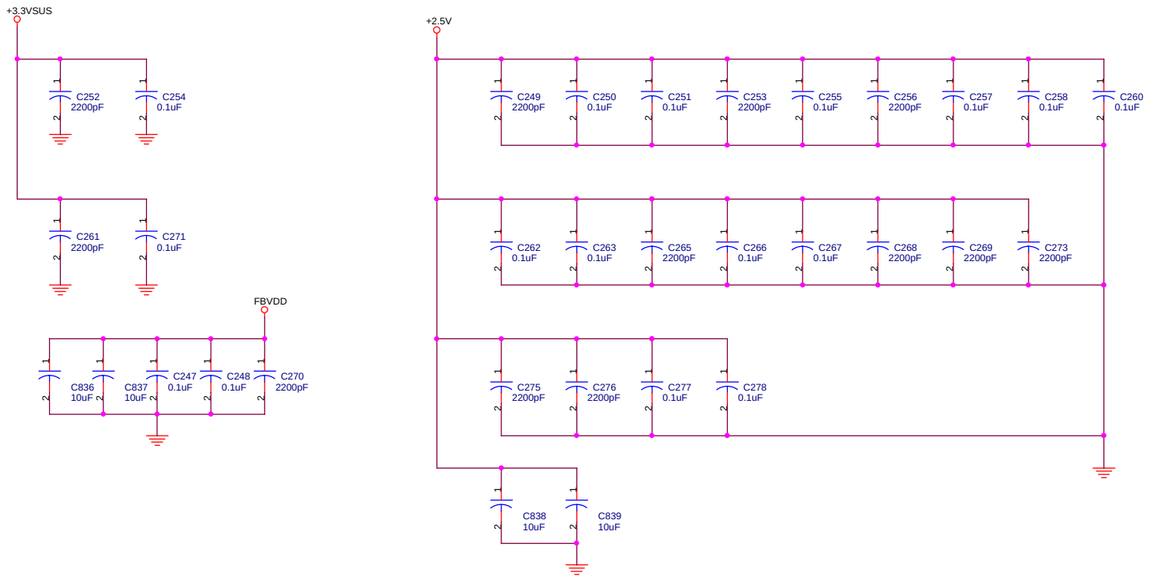
	Size: C	CAGE Code	DWG NO / Rev
Wednesday, February 21, 2001	Scale		Sheet: 2 of 9

NV11 DECOUPLING



FB (MEMORY) DECOUPLING



FB/NVXX DECOUPLING

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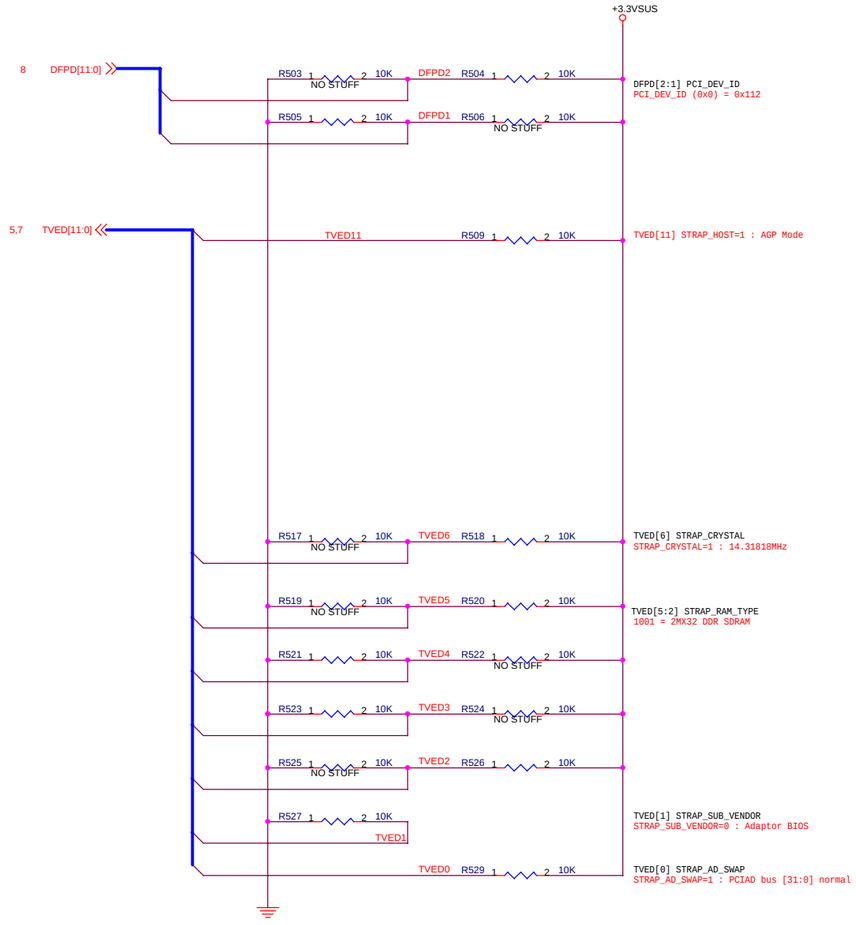
Wednesday, February 21, 2001	Size: C; CAGE Code; DWG NO; Rev Scale Sheet: 3 of 9



NVXX HOST STRAPS

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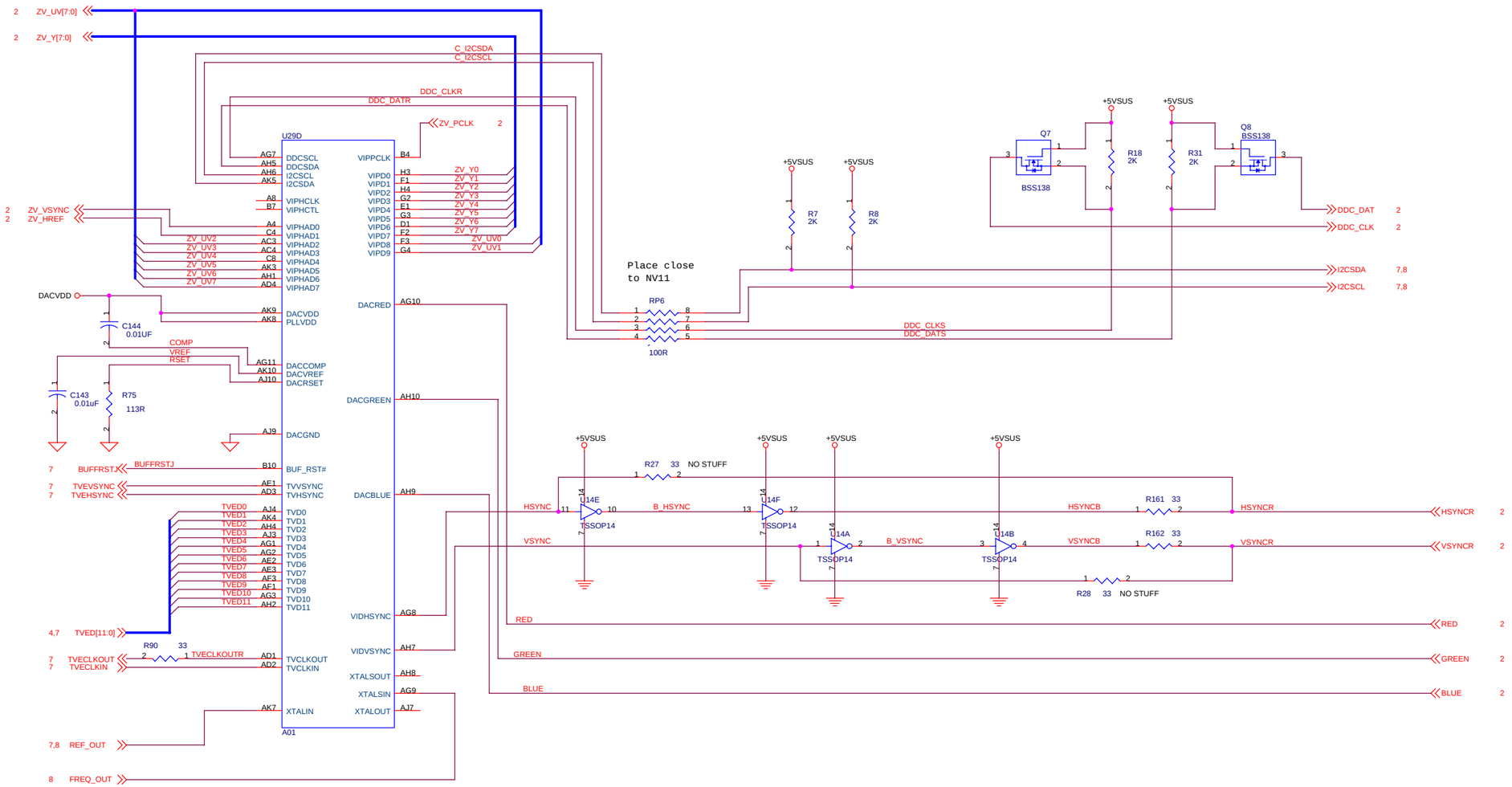
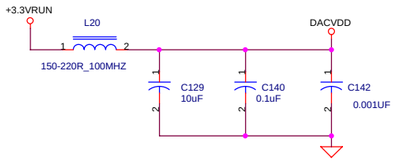
Size	CAGE Code	DWG NO	Rev
C			

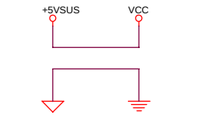
Wednesday, February 21, 2001

Scale

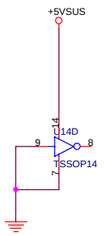
Sheet 4 of 9







Single point connection to DAC
output reference GND



DAC and MEDIA PORT

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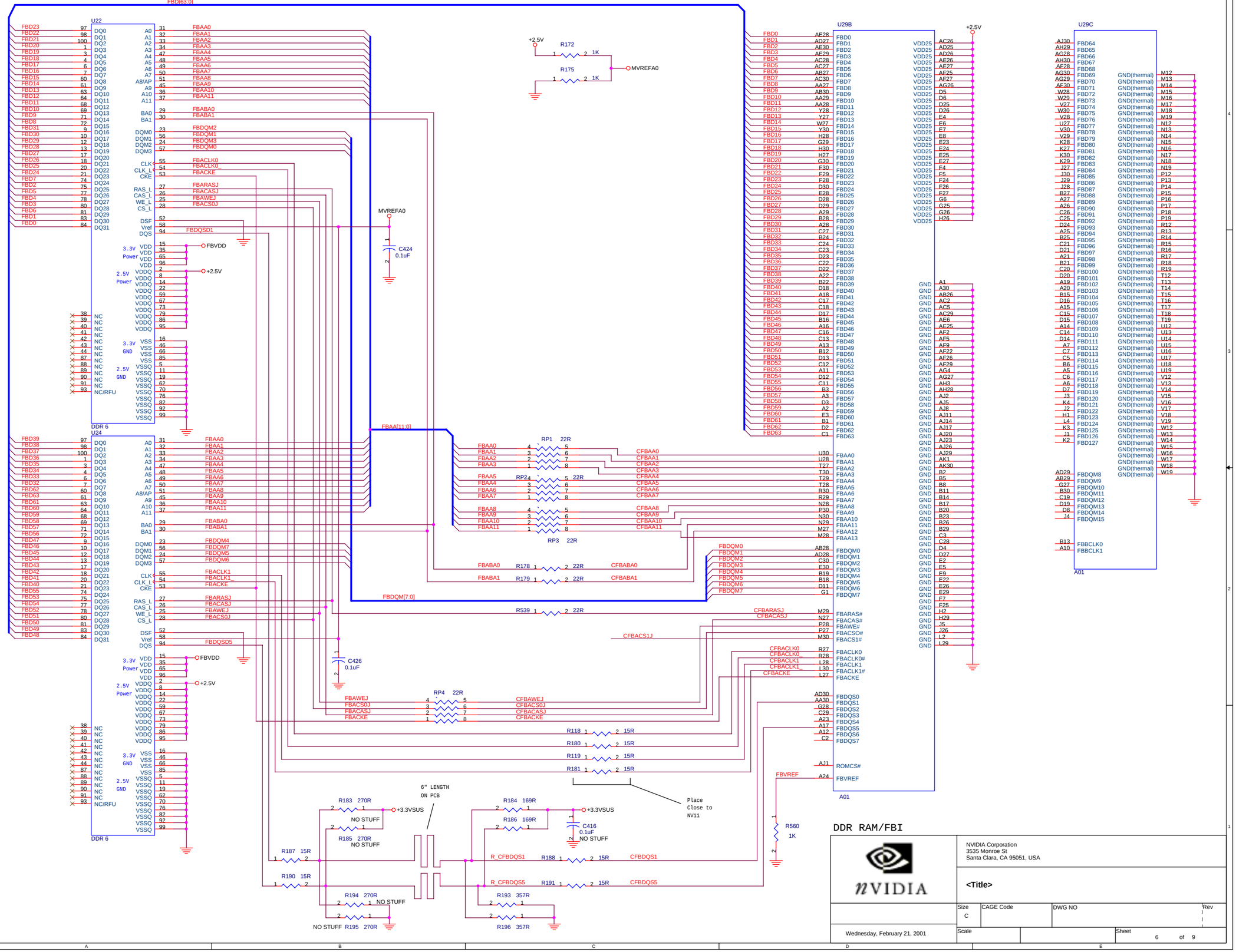
Size	CAGE Code	DWG NO	Rev
C			

Wednesday, February 21, 2001

Scale

Sheet 5 of 9


FBD[63:0]
U22
DDR 6
U24
DDR 6
FBAA[11:0]
FBDQM[7:0]
MVREFA0
R172 1K
R175 1K
+2.5V
C424 0.1uF
C426 0.1uF
FBVDD
RP1 22R
RP2 22R
RP3 22R
RP4 22R
R178 22R
R179 22R
R539 22R
R118 15R
R180 15R
R119 15R
R181 15R
R183 270R
R184 169R
R185 270R
R186 169R
R187 15R
R188 15R
R190 15R
R191 15R
R193 357R
R194 270R
R195 270R
R196 357R
R560 1K
C416 0.1uF
NO STUFF
+3.3VSUS
6" LENGTH ON PCB
Place Close to NV11
R_CFBDQS1
R_CFBDQS5
CFBDQS1
CFBDQS5
U29B
U29C
A01
FBVREF
ROMCS#
DDR RAM/FBI
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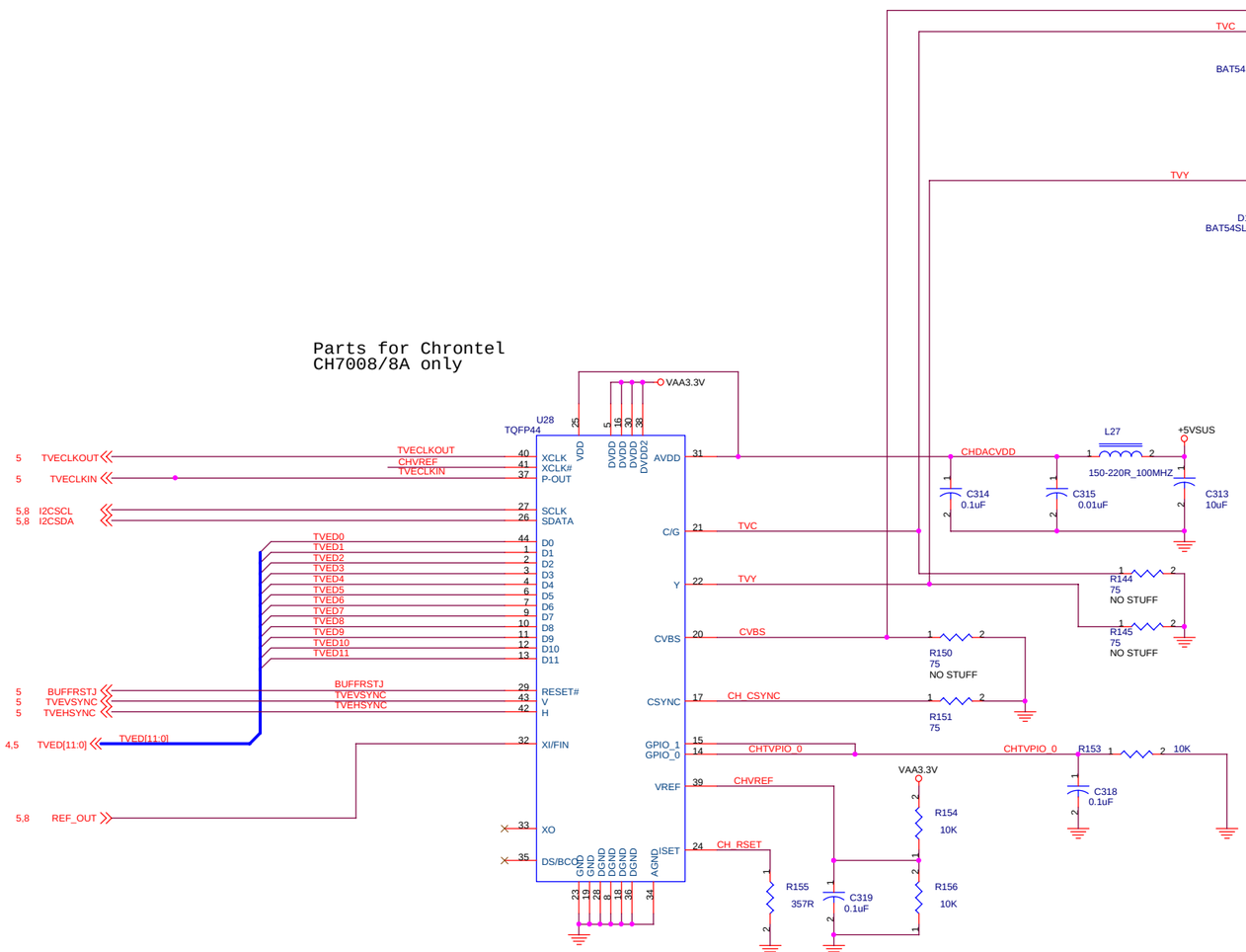
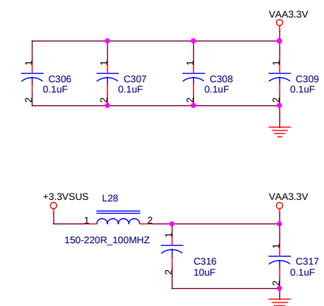
Size C
CAGE Code
DWG NO
Rev
Wednesday, February 21, 2001
Sheet 6 of 9

Parts for Chrontel
CH7008/8A only





Chrontel TV ENCODER

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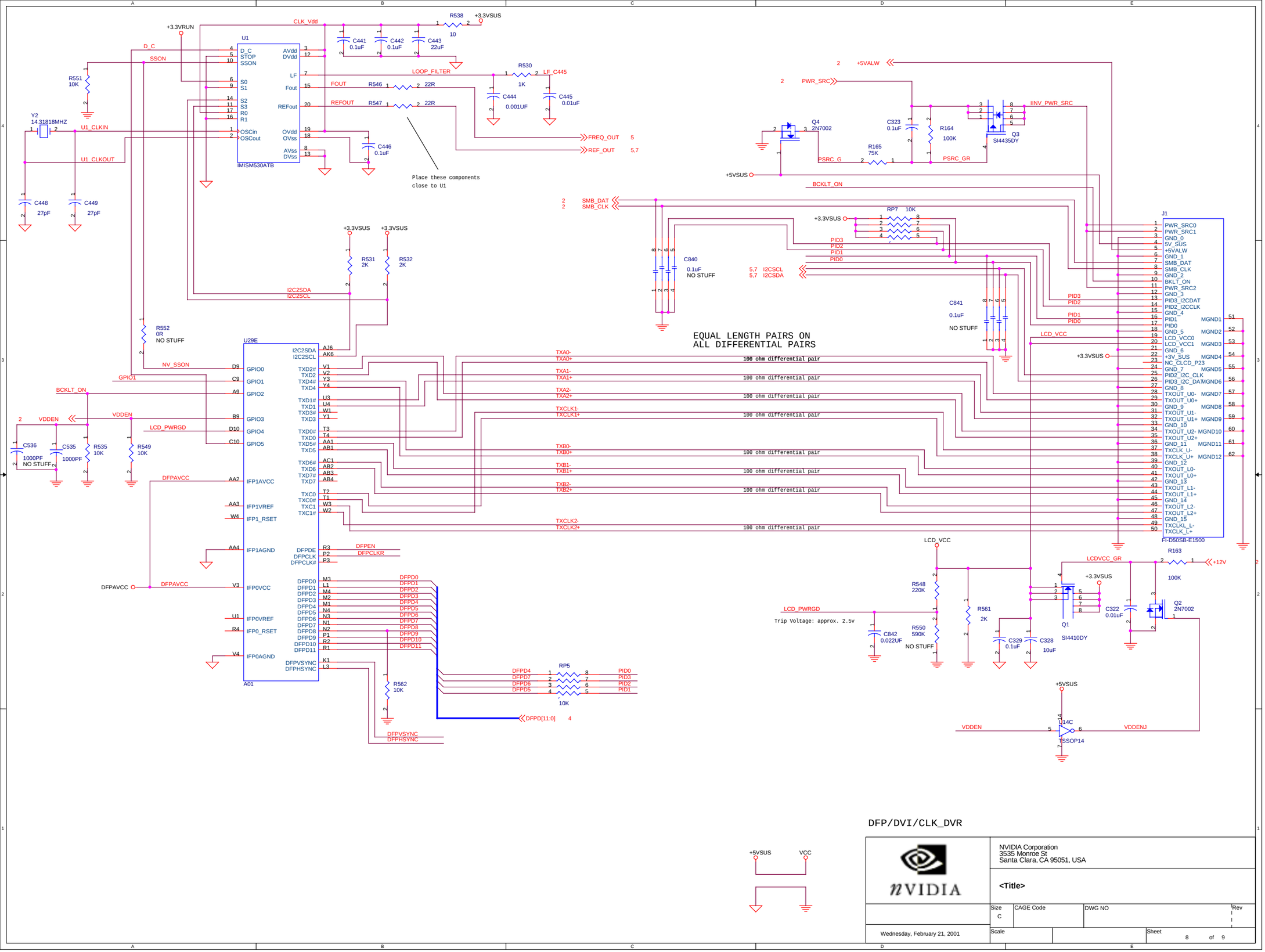
	Size: C	CAGE Code	DWG NO / Rev
Wednesday, February 21, 2001	Scale		Sheet: 7 of 9


U1
IMISM530ATB
Y2
14.31818MHZ
U1_CLKIN
U1_CLKOUT
C448
27pF
C449
27pF
Place these components
close to U1
FREQ_OUT
REF_OUT
EQUAL LENGTH PAIRS ON
ALL DIFFERENTIAL PAIRS
U29E
A01
J1
FI-D50SB-E1500
Q4
2N7002
Q3
SI4435DY
Q1
SI4410DY
Q2
2N7002
U14C
TSSOP14
RP5
RP7
DFP/DVI/CLK_DVR
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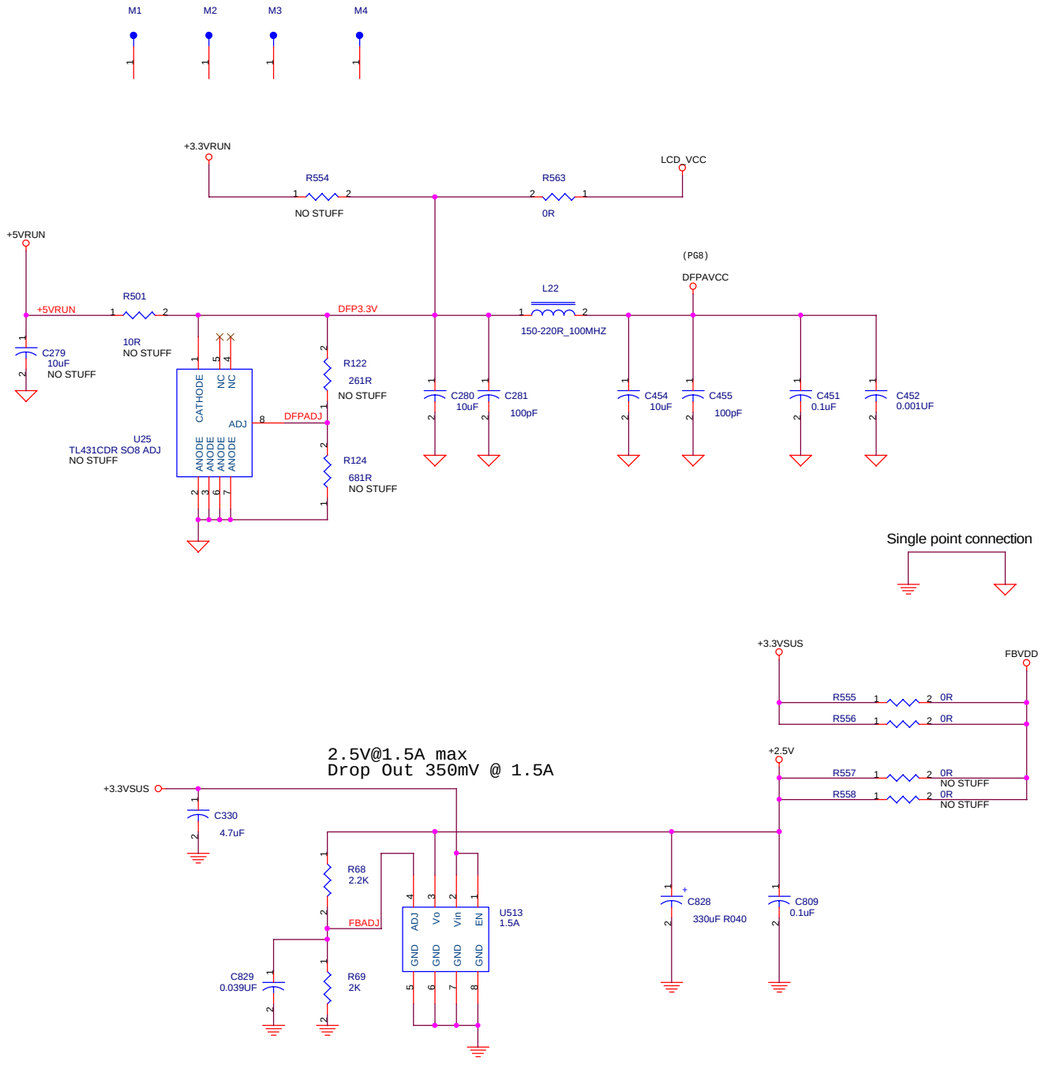
<Title>
Wednesday, February 21, 2001
Sheet 8 of 9



DC-DC CONTVR

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	Size: C | CAGE Code | DWG NO | Rev
Wednesday, February 21, 2001	Scale | Sheet: 9 of 9