

P561: G98, DDR2 MEMORY 32MX16/16Mx16/64MX16

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REV HISTORY


History 10		
96/09/27	page 08	add AV_OUT
	page 13	change Q1, Q2 to TO252
	page 14	add FBVDDQ-linear block, change U2 footprint
96/09/28	page 07	change J4 footprint
	page 12	add J7 (co-lay J6)
	page 13	add R572 for RT9259A, R570 footprint change to 0805, change L11, C11, C12, C31 footprint
	page 14	remove PWM block
		add D20, D21, C211, C212, C213, C214
96/10/01	page 14	add R210, R211
	page 09	add R75~R88, R63~R69, L15~L21 for DVI (EMI_solution)
96/10/02	page 12	add FAN Control Function
96/10/03	page 09	and netname (Between common Choke and DVI connector)
96/10/05	page 12	cnage Y501 (4 pin to 2 pin)
96/10/12	page 12	add L30, remove L10
96/10/12	baseon	PCB:2.0 CIRCUIT DSN CAHNGE to PCB :1.0
	ONLY CHANGE	page 13 remove PWM solution, ADD linear solutin
		remove C301~~C308 (EMI solution for FBVDDQ)
96/10/17	page 11	add CABLE and PCB
96/10/18	page 14	add C301~~C308 (EMI solution for FBVDDQ)
History 20		
96/10/03	page 14	remove FBVDDQ-LINNEAR block, add FBVDDQ-PWM function
		change L15 footprint as CHK4417C_3R3S01, change C35 footprint
96/10/05	page 12	cahngue Y501 (4pin to 2 pin)
96/10/09	page 11	add FM1~~ FM6 for Fiducial Point
		add U301~~U306 for EMI
	page 13	add C309 for EMI
	page 14	add C301~~C308, C310~~C312 for EMI
96/10/10	page 13	add L30
96/10/11	page 13	remove L10
96/10/17	page 11	add cable

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10561-xxxx-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10561-0000-100	P561: G98-300, 64 BIT DDR2 180A/16 MEMORY, VGA-DVI+HDMI
2	SKU0001	600-10561-0001-100	P561: G98-300, 64 BIT DDR2 320A/16 MEMORY, VGA-DVI+HDMI
3	SKU0007	600-10561-0007-100	P561: G98-300, 64 BIT DDR2 320X16 MEMORY, VGA-DVI+HDMI
4	SKU0007	600-10561-0007-200	P561: G98-300, 64 BIT DDR2 320X16 MEMORY, VGA-DVI+HDMI
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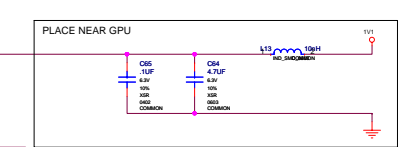
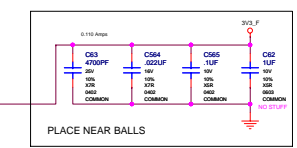
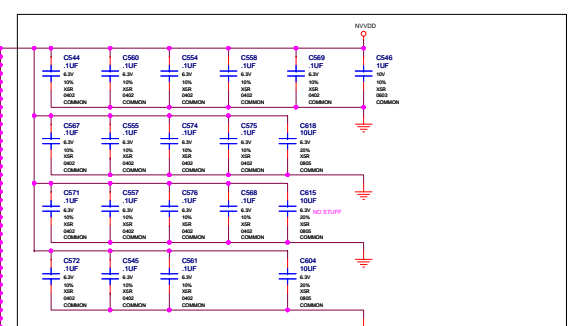
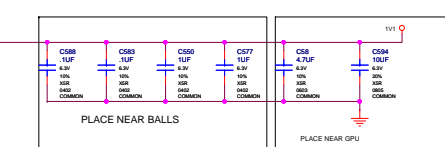
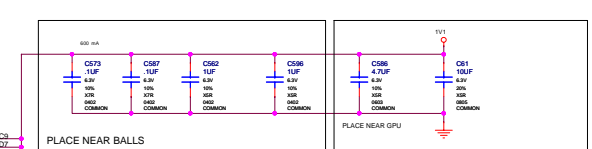
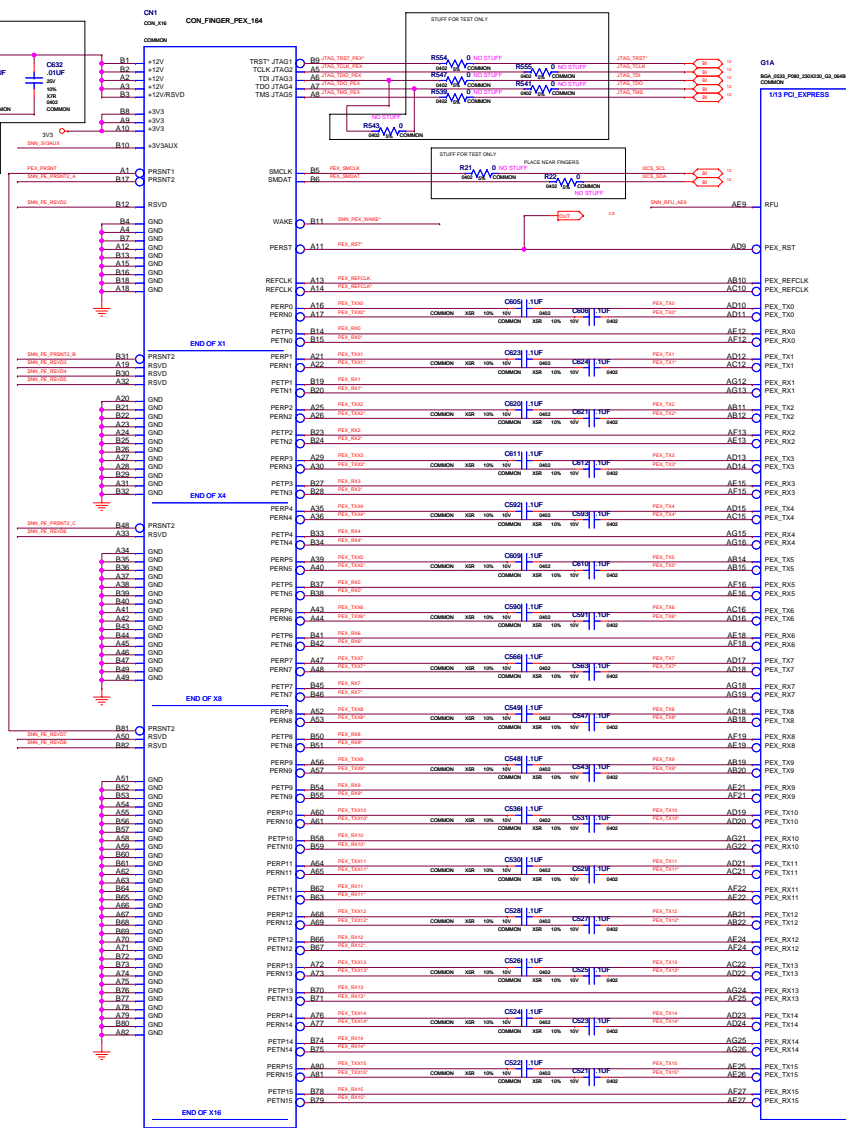
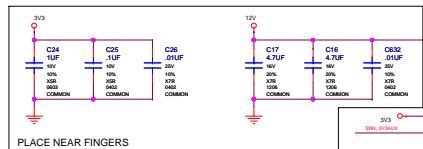
2701 SANTOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA




NV_PN	600-10561-xxxx-100 D		
REV		PAGE	
NAME		DATE	31-AUG-2007

PCI Express Interface



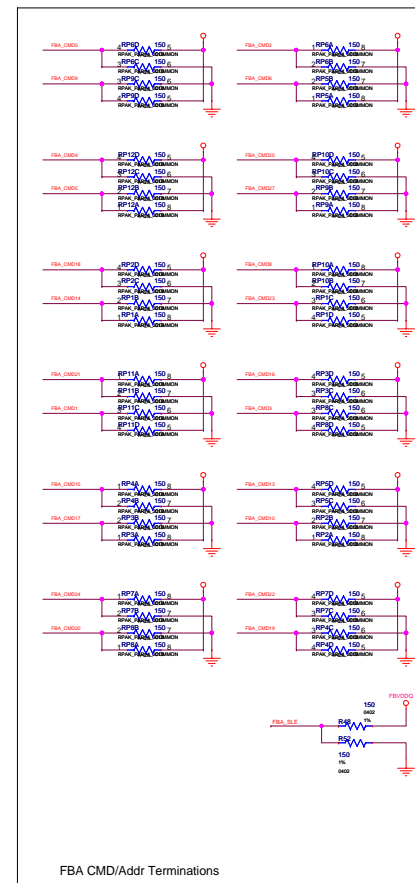
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
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ID		PAGE	
NAME		DATE	31-JUL-2007

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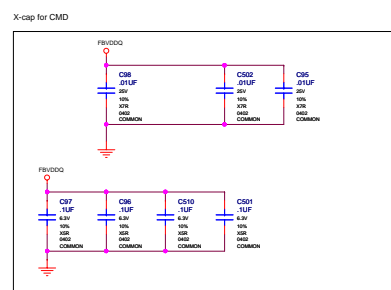
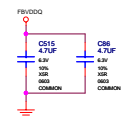
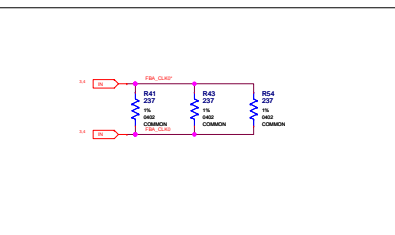
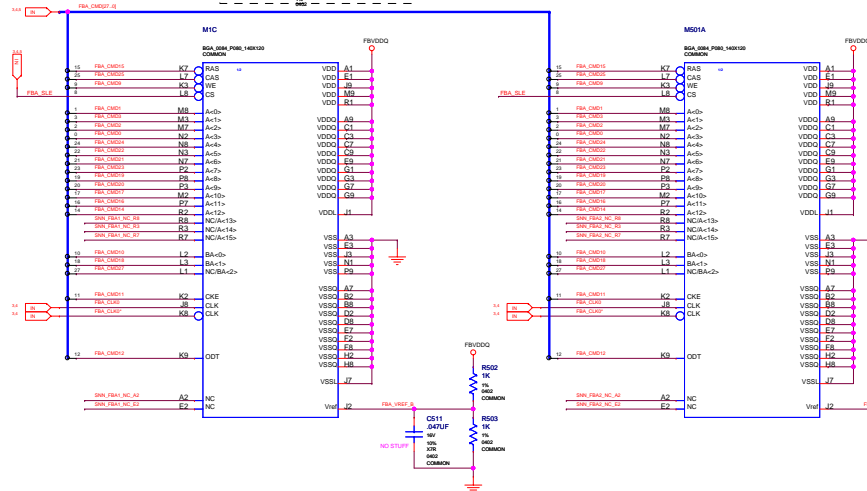
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINA
PAGE DETAIL	Frame Buffer Interface



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NV_PN	600-10561-xxxx-100 D
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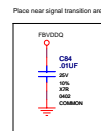
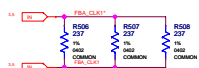
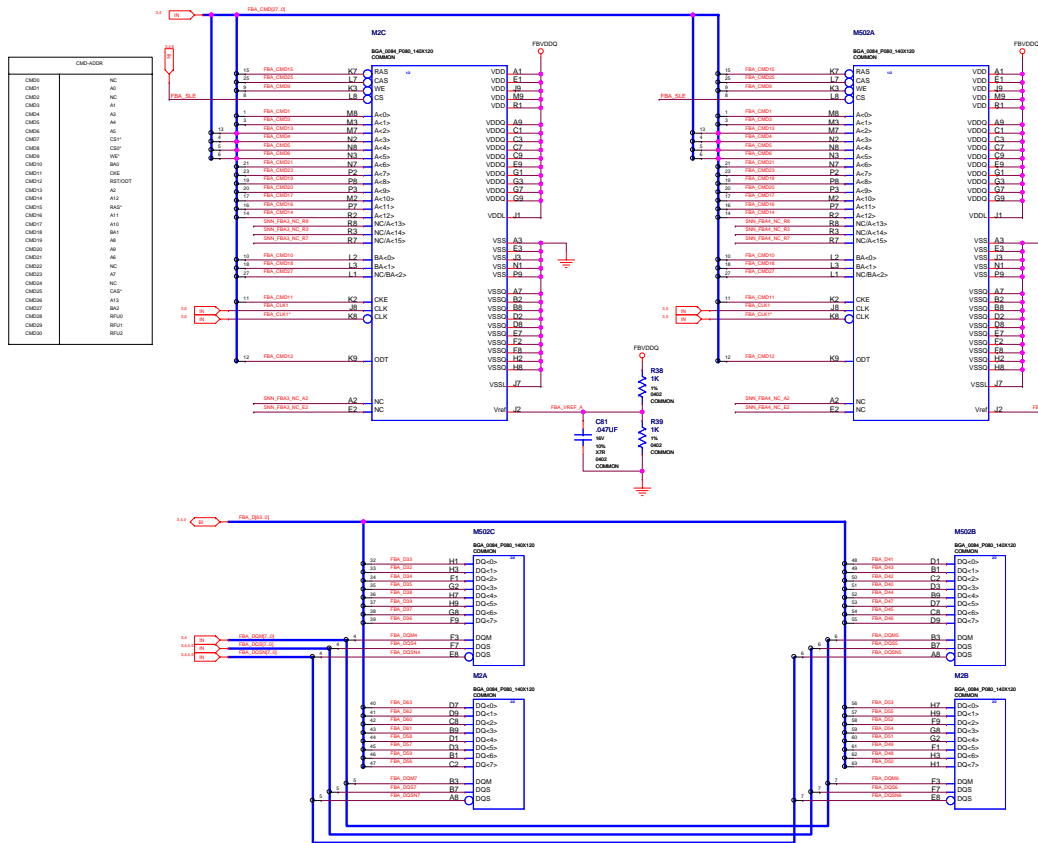
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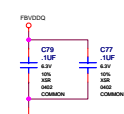
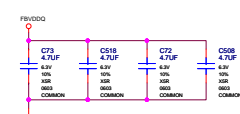
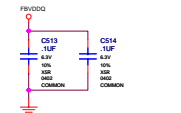
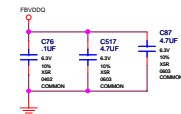
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Memory 2nd Bank 32..63



Net Name		DIFF_PAIR	CRITICAL	IMPEDANCE	
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NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

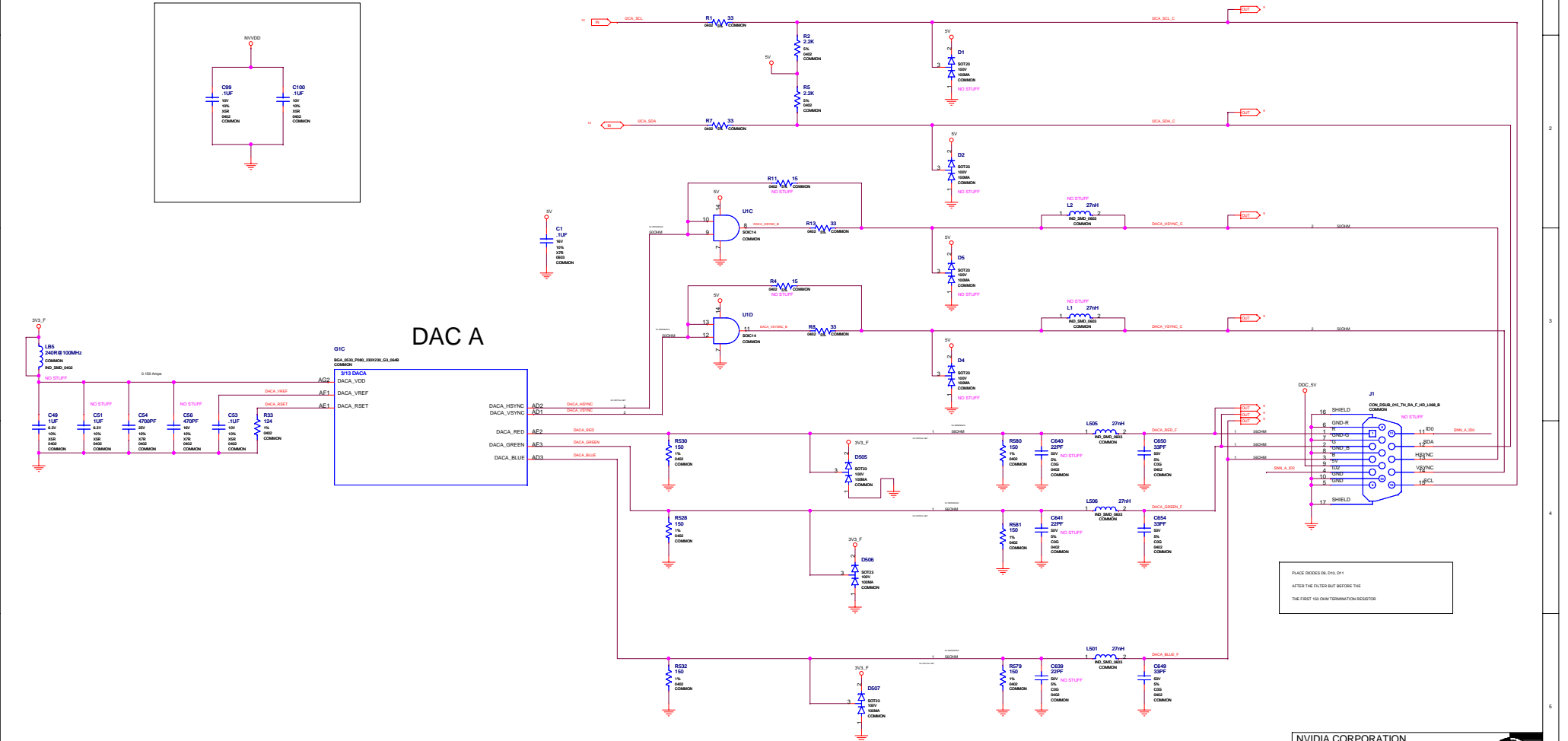
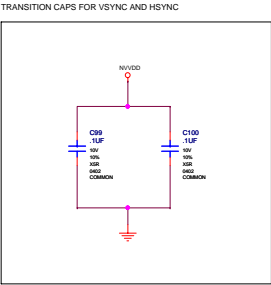


NV_PN	600-10561-xxxx-100 D
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ID		PAGE	
NAME		DATE	31-AUG-2007

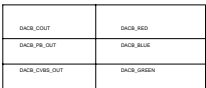
			H		
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DACA, Slim DB15 Connector



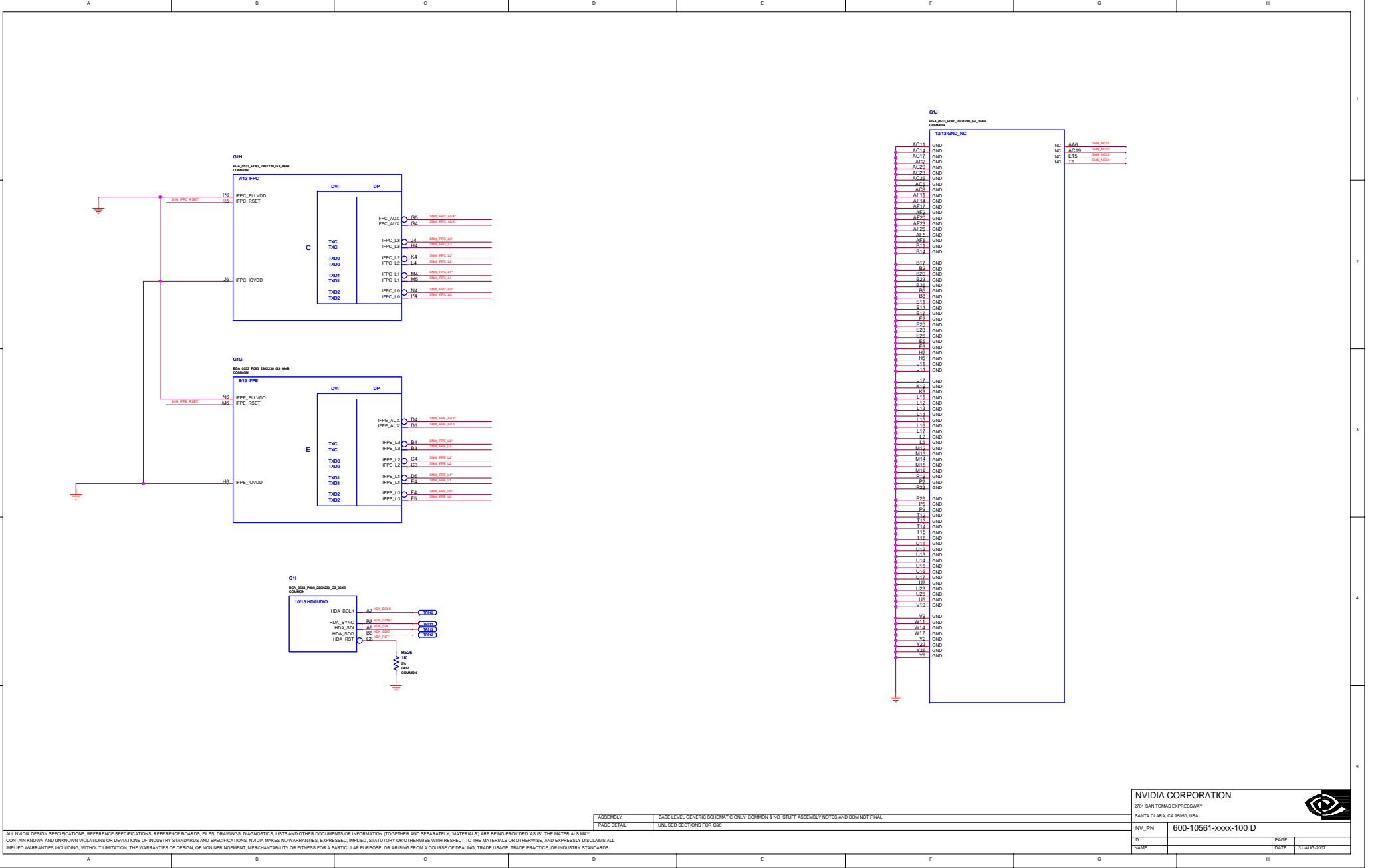
PLACE DIODES D4, D5, D6, D7
AFTER THE FILTER BUT BEFORE THE
THE FIRST 150 OHM TERMINATION RESISTOR

A	B	C	D	E	F	G
---	---	---	---	---	---	---

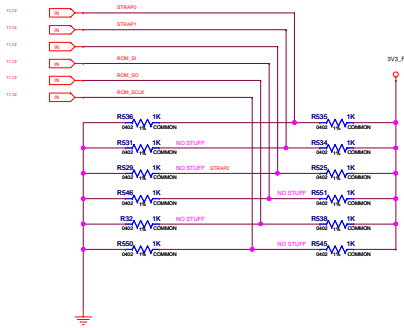


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NV_PN	600-10561-xxxx-100 D		
ID		PAGE	
NAME		DATE	31-AUG-2007

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Straps, Mechanical Parts



Each strap pin represents a 4 bit value.
Pullup or Pulldown configures the MSB.
Resistor Value determines the 3 LSBs.
Resistor range is $R \times n$
where n is 0-9 and R is 5K ohm.

Resistor Value	Multilevel	Tied to VCC	Tied to Ground
3 Kohms	Y	1000	0000
6 Kohms	Y	1001	0001
12 Kohms	Y	1010	0010
24 Kohms	Y	1011	0011
48 Kohms	Y	1100	0100
96 Kohms	Y	1101	0101
192 Kohms	Y	1110	0110
284 Kohms	Y	1111	0111
2 Kohms ^a	N	xxxx	xxxx

STRAPS

- ```

1. SUB VENDOR = 1 (ROM PRESENT)
 = 0 (NO ROM PRESENT)

2. DEVICE ID FOR GR464 = 0x0622
 A) PCI_DEV_ID_ID = 0x1558 = 0x010
 B) PCI_DEV_VENDOR_ID = 0x1404 = 0x010

3. XGID_PADCFG_LUT_ADDR_0 = 0x000

4. TUNING_CFG_ID = 0x01

5. RAMCFG_CFG_ID = 0x0000 DOR2 64 BIT ELPHDA
 = 0x01 10MAH4 DOR2 64 BIT DSAUSING, WIDCON
 = 0x01 10MAH4 DOR2 64 BIT INFTR
 = 0x02 10MAH4 DOR2 64 BIT ELPHDA
 = 0x03 10MAH4 DOR2 64 BIT DSAUSING
 = 0x11 10MAH4 DOR2 64 BIT INFTR

6. USER_CFG_ID = 0x000

```

| MULTI-LEVEL MODE |                                                              |
|------------------|--------------------------------------------------------------|
| SIGNAL           | FUNCTION                                                     |
| STRAP[0]         | USER[0]                                                      |
| STRAP[1]         | ASIC_FACTORY_LUT_ADR[0]                                      |
| STRAP[2]         | PCI_DEVICE[0]                                                |
| ROM_SCUR         | PCI_DEVICE_EXT_SLAVE_VENDOR_SLOT_CLK_CFG_PEX_PL1_EN_TERRAIN0 |
| ROM_SI           | RAMCFG[0]                                                    |
| ROM_SO           | XCLK_377_TMRDQ[0]                                            |

| BRINGUP BINARY MODE |  | STRAP_CAL_PU_GND0 (R012) = NO STUFF<br>STRAP_CAL_PU_GND1 (R011) = NO STUFF |
|---------------------|--|----------------------------------------------------------------------------|
| IGNAL               |  | FUNCTION                                                                   |
| STRAP00             |  | IGH1_PADCFG_LUT_ADDR0[0]                                                   |
| STRAP01             |  | IGH1_PADCFG_LUT_ADDR0[1]                                                   |
| STRAP02             |  | IGH1_PADCFG_LUT_ADDR0[2]                                                   |
| ROM_SCUR            |  | IGH1_PADCFG_LUT_ADDR0[3]                                                   |
| ROM_SI              |  | SUB_VENDOR                                                                 |
| ROM_SO              |  | XCUR_277                                                                   |

| PRODUCTION/BINARY MODE |  | STRAP_CAL_PU_GND8 (R012) = NO STUFF<br>STRAP_CAL_PU_GND1 (R011) = 40K |  |
|------------------------|--|-----------------------------------------------------------------------|--|
| SIGNAL                 |  | FUNCTION                                                              |  |
| STRAP[S]               |  | RAMC[Q]                                                               |  |
| STRAP1[                |  | RAMC[Q]                                                               |  |
| STRAP2[                |  | RAMC[Q]                                                               |  |
| ROM_SCUR               |  | PO_DEV[Q]                                                             |  |
| ROM_SI                 |  | PO_DEV[Q_EXT                                                          |  |
| ROM_S0                 |  | K0X_377                                                               |  |

STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz ( MULTI LEVEL) R511= 40K, R512=40K

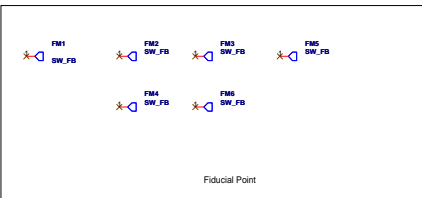
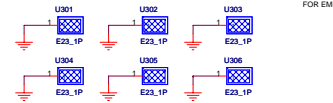
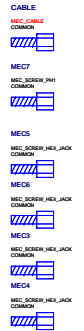
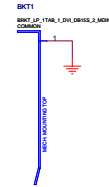
| ENV | QID | FUNCTION | FUNCTION                                       |
|-----|-----|----------|------------------------------------------------|
| 20K | 0K  | STRANSI  | USREQ_0                                        |
|     | 1K  | STRANSI  | SIOE_PDRGQ_LUT_AREQ_0                          |
|     | 25K | STRANSI  | PO_25KREQ_0                                    |
|     | 30K | ROM_ICM  | PO_30K_SLT_SUB_VENDOR_SULT_CMT_CPC_ROM_TERMINI |
|     | 40K | ROM_ICM  | RAMCFG_0                                       |
|     |     | ROM_ICM  | ICM_T7T10REQ_0                                 |

STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz (BRINGUP BINARY) R511= NO STUFF, R512=NO STUFF

| SOL# | QID | PHYSICALS | FUNCTION              |
|------|-----|-----------|-----------------------|
| SK   | SK  | STRAW1    | SOH_PRODCT1_LUT_ADRQ1 |
|      | SK  | STRAW2    | SOH_PRODCT2_LUT_ADRQ2 |
|      | SK  | STRAW3    | SOH_PRODCT3_LUT_ADRQ3 |
|      | SK  | ROM_SEL   | SOH_PRODCT4_LUT_ADRQ4 |
|      | SK  | ROM_CS    | ROM_VMOND             |
|      | SK  | ROM_SO    | XDL_ZPT               |

STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz ( PRODUCTION BINARY) R511= 40K, R512= NO STUFF

| ENV | QID | PIN(SIGNAL) | FUNCTION      |
|-----|-----|-------------|---------------|
| SA  |     | ETAP[0]     | ANALOG[0]     |
| SA  |     | ETAP[1]     | ANALOG[1]     |
| SA  |     | ETAP[2]     | ANALOG[2]     |
| SA  | SA  | ROM_ADDR    | PC0_DIV[0:17] |
| SA  | SA  | ROM_ID      | ROM_ID[7]     |



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|      |  |      |             |
|------|--|------|-------------|
| ID   |  | PAGE |             |
| NAME |  | DATE | 31-AUG-2007 |

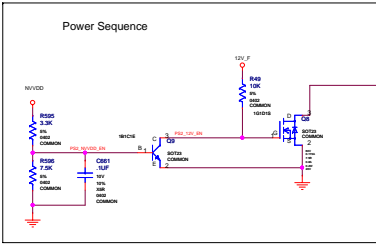
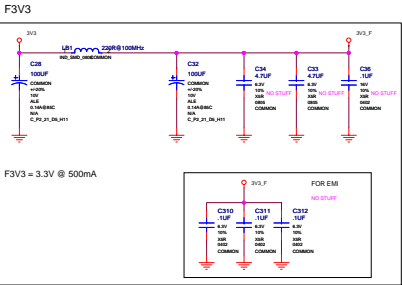
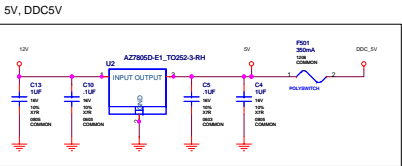
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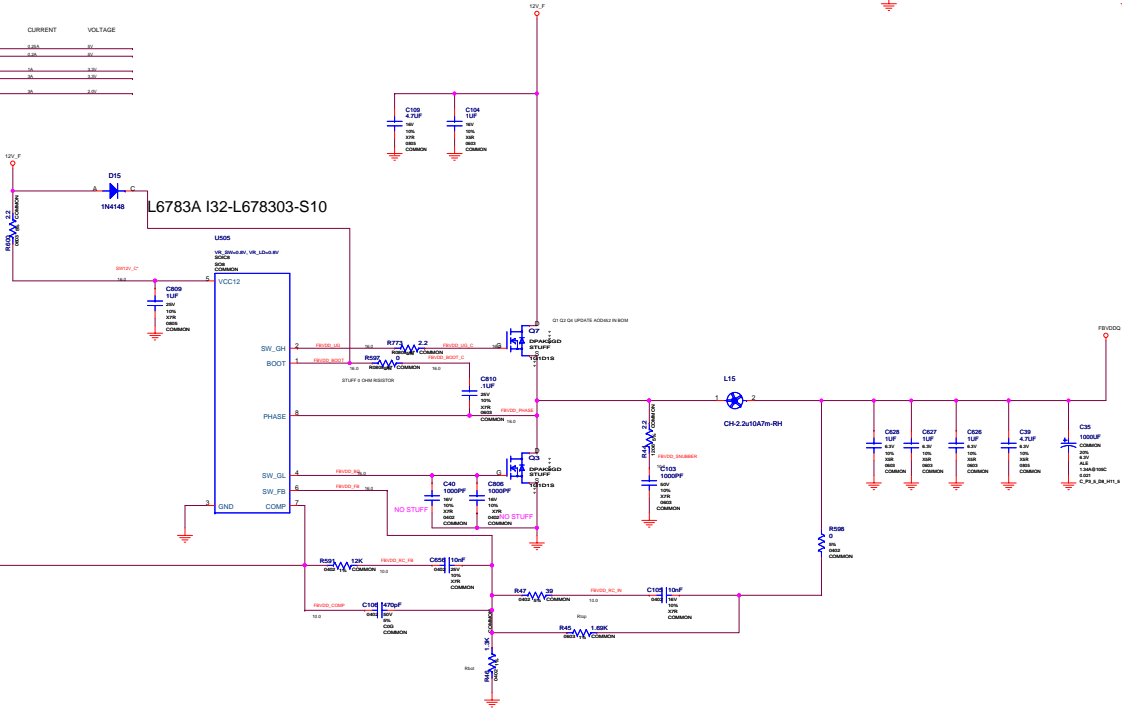
|             |                                                                                       |
|-------------|---------------------------------------------------------------------------------------|
| ASSEMBLY    | BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL |
| PAGE DETAIL | Straps, Mechanical Parts                                                              |



Power Supply II: 5V, DDC5V, F3V3, FBVDDQ



| Net Name | MIN_LENGTH | CURRENT | VOLTAGE |
|----------|------------|---------|---------|
| 5V       | 200        | 1.00    | 5V      |
| 5V_1     | 200        | 1.00    | 5V      |
| 5V_2     | 200        | 1.00    | 5V      |
| 5V_3     | 200        | 1.00    | 5V      |
| 5V_4     | 200        | 1.00    | 5V      |
| 5V_5     | 200        | 1.00    | 5V      |
| 5V_6     | 200        | 1.00    | 5V      |
| 5V_7     | 200        | 1.00    | 5V      |
| 5V_8     | 200        | 1.00    | 5V      |
| 5V_9     | 200        | 1.00    | 5V      |
| 5V_10    | 200        | 1.00    | 5V      |
| 5V_11    | 200        | 1.00    | 5V      |
| 5V_12    | 200        | 1.00    | 5V      |
| 5V_13    | 200        | 1.00    | 5V      |
| 5V_14    | 200        | 1.00    | 5V      |
| 5V_15    | 200        | 1.00    | 5V      |
| 5V_16    | 200        | 1.00    | 5V      |
| 5V_17    | 200        | 1.00    | 5V      |
| 5V_18    | 200        | 1.00    | 5V      |
| 5V_19    | 200        | 1.00    | 5V      |
| 5V_20    | 200        | 1.00    | 5V      |
| 5V_21    | 200        | 1.00    | 5V      |
| 5V_22    | 200        | 1.00    | 5V      |
| 5V_23    | 200        | 1.00    | 5V      |
| 5V_24    | 200        | 1.00    | 5V      |
| 5V_25    | 200        | 1.00    | 5V      |
| 5V_26    | 200        | 1.00    | 5V      |
| 5V_27    | 200        | 1.00    | 5V      |
| 5V_28    | 200        | 1.00    | 5V      |
| 5V_29    | 200        | 1.00    | 5V      |
| 5V_30    | 200        | 1.00    | 5V      |
| 5V_31    | 200        | 1.00    | 5V      |
| 5V_32    | 200        | 1.00    | 5V      |
| 5V_33    | 200        | 1.00    | 5V      |
| 5V_34    | 200        | 1.00    | 5V      |
| 5V_35    | 200        | 1.00    | 5V      |
| 5V_36    | 200        | 1.00    | 5V      |
| 5V_37    | 200        | 1.00    | 5V      |
| 5V_38    | 200        | 1.00    | 5V      |
| 5V_39    | 200        | 1.00    | 5V      |
| 5V_40    | 200        | 1.00    | 5V      |
| 5V_41    | 200        | 1.00    | 5V      |
| 5V_42    | 200        | 1.00    | 5V      |
| 5V_43    | 200        | 1.00    | 5V      |
| 5V_44    | 200        | 1.00    | 5V      |
| 5V_45    | 200        | 1.00    | 5V      |
| 5V_46    | 200        | 1.00    | 5V      |
| 5V_47    | 200        | 1.00    | 5V      |
| 5V_48    | 200        | 1.00    | 5V      |
| 5V_49    | 200        | 1.00    | 5V      |
| 5V_50    | 200        | 1.00    | 5V      |
| 5V_51    | 200        | 1.00    | 5V      |
| 5V_52    | 200        | 1.00    | 5V      |
| 5V_53    | 200        | 1.00    | 5V      |
| 5V_54    | 200        | 1.00    | 5V      |
| 5V_55    | 200        | 1.00    | 5V      |
| 5V_56    | 200        | 1.00    | 5V      |
| 5V_57    | 200        | 1.00    | 5V      |
| 5V_58    | 200        | 1.00    | 5V      |
| 5V_59    | 200        | 1.00    | 5V      |
| 5V_60    | 200        | 1.00    | 5V      |
| 5V_61    | 200        | 1.00    | 5V      |
| 5V_62    | 200        | 1.00    | 5V      |
| 5V_63    | 200        | 1.00    | 5V      |
| 5V_64    | 200        | 1.00    | 5V      |
| 5V_65    | 200        | 1.00    | 5V      |
| 5V_66    | 200        | 1.00    | 5V      |
| 5V_67    | 200        | 1.00    | 5V      |
| 5V_68    | 200        | 1.00    | 5V      |
| 5V_69    | 200        | 1.00    | 5V      |
| 5V_70    | 200        | 1.00    | 5V      |
| 5V_71    | 200        | 1.00    | 5V      |
| 5V_72    | 200        | 1.00    | 5V      |
| 5V_73    | 200        | 1.00    | 5V      |
| 5V_74    | 200        | 1.00    | 5V      |
| 5V_75    | 200        | 1.00    | 5V      |
| 5V_76    | 200        | 1.00    | 5V      |
| 5V_77    | 200        | 1.00    | 5V      |
| 5V_78    | 200        | 1.00    | 5V      |
| 5V_79    | 200        | 1.00    | 5V      |
| 5V_80    | 200        | 1.00    | 5V      |
| 5V_81    | 200        | 1.00    | 5V      |
| 5V_82    | 200        | 1.00    | 5V      |
| 5V_83    | 200        | 1.00    | 5V      |
| 5V_84    | 200        | 1.00    | 5V      |
| 5V_85    | 200        | 1.00    | 5V      |
| 5V_86    | 200        | 1.00    | 5V      |
| 5V_87    | 200        | 1.00    | 5V      |
| 5V_88    | 200        | 1.00    | 5V      |
| 5V_89    | 200        | 1.00    | 5V      |
| 5V_90    | 200        | 1.00    | 5V      |
| 5V_91    | 200        | 1.00    | 5V      |
| 5V_92    | 200        | 1.00    | 5V      |
| 5V_93    | 200        | 1.00    | 5V      |
| 5V_94    | 200        | 1.00    | 5V      |
| 5V_95    | 200        | 1.00    | 5V      |
| 5V_96    | 200        | 1.00    | 5V      |
| 5V_97    | 200        | 1.00    | 5V      |
| 5V_98    | 200        | 1.00    | 5V      |
| 5V_99    | 200        | 1.00    | 5V      |
| 5V_100   | 200        | 1.00    | 5V      |



FBVDDQ

$$V_{out} = V_{Ref} \cdot (1 + R_{top}/R_{bot})$$

1.800V = 0.8V \* (1 + (5.9k/4.7k)) (ISL6549)

2.000V = 0.8V \* (1 + (5.9k/3.92k)) (ISL6549)

2.156V = 0.8V \* (1 + (5.9k/3.4k)) (ISL6549)



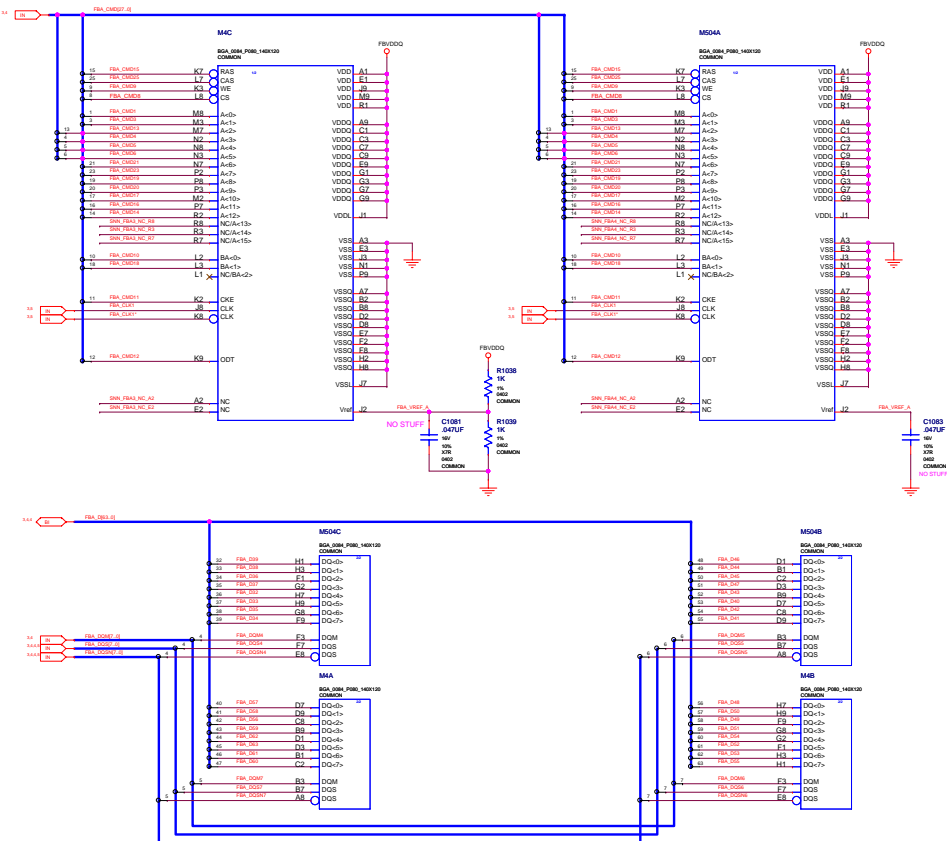




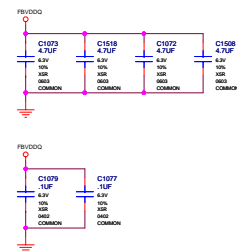
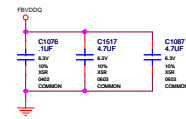


## Memory 1st Bank 32..63

| CMD-ACOR |    |         |
|----------|----|---------|
| CMD00    |    | NC      |
| CMD01    | AI | AI      |
| CMD02    |    | NC      |
| CMD03    | AI | AI      |
| CMD04    | AI | A3      |
| CMD05    |    | AI      |
| CMD06    | AI | AI      |
| CMD07    |    | CS1*    |
| CMD08    |    | CS0*    |
| CMD09    |    | W0*     |
| CMD10    |    | BA3     |
| CMD11    |    | OK      |
| CMD12    |    | WSTF00T |
| CMD13    |    |         |
| CMD14    | AI | AI      |
| CMD15    |    | BA0*    |
| CMD16    |    | A11     |
| CMD17    |    | A10     |
| CMD18    |    | BA1*    |
| CMD19    |    | AI      |
| CMD20    |    | AI      |
| CMD21    |    | AI      |
| CMD22    |    | NC      |
| CMD23    | AI | AI      |
| CMD24    |    | NC      |
| CMD25    |    | CAS*    |
| CMD26    |    | A13     |
| CMD27    |    | BA2     |
| CMD28    |    | RFU0    |
| CMD29    |    | RFU1    |
| CMD30    |    | RFU2    |



|  | Net Name | DIFF_PAIR | CRITICAL | IMPEDANCE |
|--|----------|-----------|----------|-----------|
|  | FBI_DQ04 | FBI_DQ05  | 1        | 1000FT    |
|  | FBI_DQ06 | FBI_DQ07  | 1        | 1000FT    |
|  | FBI_DQ08 | FBI_DQ09  | 1        | 1000FT    |
|  | FBI_DQ10 | FBI_DQ11  | 1        | 1000FT    |
|  | FBI_DQ12 | FBI_DQ13  | 1        | 1000FT    |
|  | FBI_DQ14 | FBI_DQ15  | 1        | 1000FT    |
|  | FBI_DQ16 | FBI_DQ17  | 1        | 1000FT    |
|  | FBI_DQ18 | FBI_DQ19  | 1        | 1000FT    |
|  | FBI_DQ20 | FBI_DQ21  | 1        | 1000FT    |
|  | FBI_DQ22 | FBI_DQ23  | 1        | 1000FT    |



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|----|--|
| ID |  |
|----|--|

|      |  |      |             |
|------|--|------|-------------|
| NAME |  | DATE | 31-AUG-2007 |
|------|--|------|-------------|

A number line from 0 to 10. A vertical line is drawn at 4, and a horizontal line is drawn at 6. The intersection is labeled 'H'.

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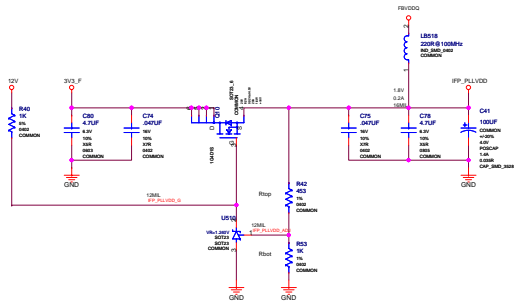
|          |                                                                                       |
|----------|---------------------------------------------------------------------------------------|
| ASSEMBLY | BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL |
|----------|---------------------------------------------------------------------------------------|

|             |                       |
|-------------|-----------------------|
| PAGE DETAIL | Memory 1st Bank 32.63 |
|-------------|-----------------------|

## Power Supply II: FBVDDQ

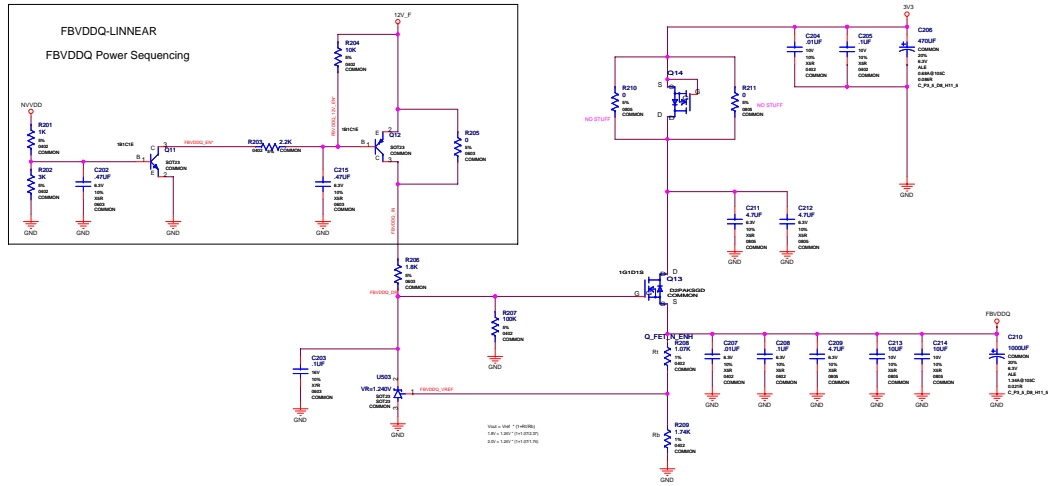
### IFP\_PLLVDD Power Supply

IFP\_PLLVDD = 1.8V @ 200mA



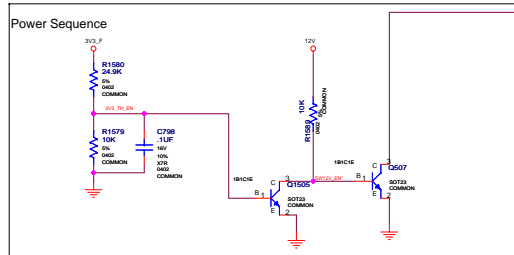
$$\text{IFP\_PLLVD} = \text{VREF} * (1 + (\text{Rtop} / \text{Rbot}))$$

$$1.801\text{V} = 1.24\text{V} * (1 + (453/1000))$$

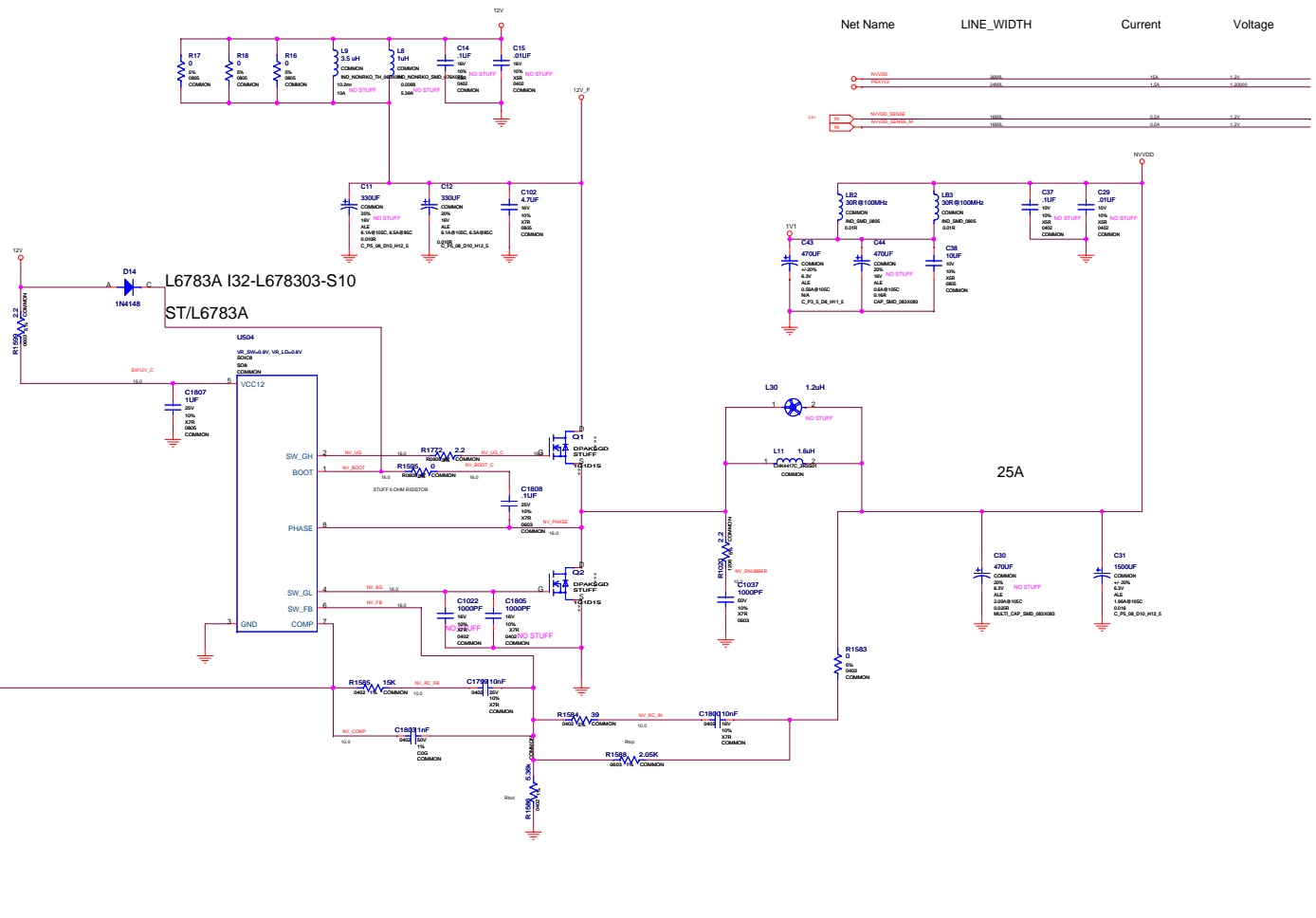


FBVDDQ = 2.0V @ 2.6A

# PowerSupplyII: NVVDD



QUADRA EXPRESS, IN-BOM



NVVDD  
 $V_{out} = V_{Ref} \cdot (1 + R_{top}/R_{bot})$   
 $1.1V = 0.8V \cdot (1 + (1.54k/4.02k)) \quad (ISL6549)$   
 $1.2V = 0.8V \cdot (1 + (1.54k/3.09k)) \quad (ISL6549)$   
 $1.2V = 0.8V \cdot (1 + (10k/20k)) \quad (APW7065)$

|                            |                      |
|----------------------------|----------------------|
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| 2701 SAN TOMAS EXPRESSWAY  |                      |
| SANTA CLARA, CA 95050, USA |                      |
| NV_PN                      | 600-10403-0000-200 A |
| ID                         |                      |
| NAME                       |                      |
| PAGE                       |                      |
| DATE                       | 12 JAN 2007          |

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