V078-0A BASE ON V079-0A modify

P501-A01 DESIGN -- G73, 256 MB DDR2, VGA, DVI-I, HDTV

PAGE SUMMARY:

REV HISTORY

Base on P501_A01 modify

7/25-0A

1.PAGE:12 Removed TMDS C/D connecter

2.PAGE:10 Add DACC Fly cable DSub

9/26-0A

1.PAGE:10,16 revised DACA hotplug circuit

10/19-10

1.NA

SKU	VARIANT	NVPN	ASSEMBLY
8	0000	600-10501-0000-100	G73 400/350MHz 256MB 128bit DDR2 16MX16 DVI-I+VGA+HDTVOUT
1	0001	600-10501-0001-100	G73-V 375/350MHZ 256MB 128bit DDR2 16MX16 DVI-I+VGA+HDTVOUT
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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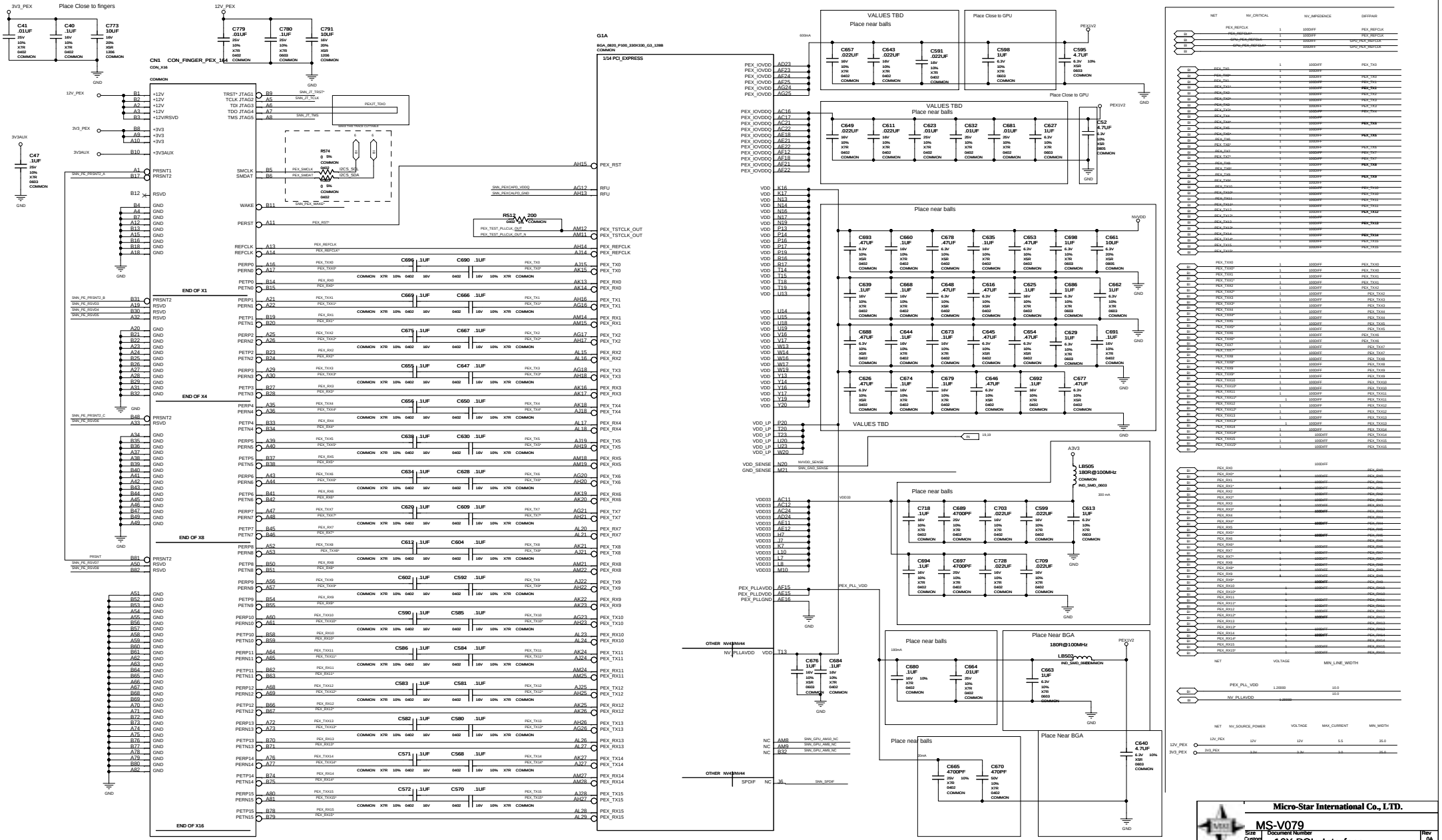
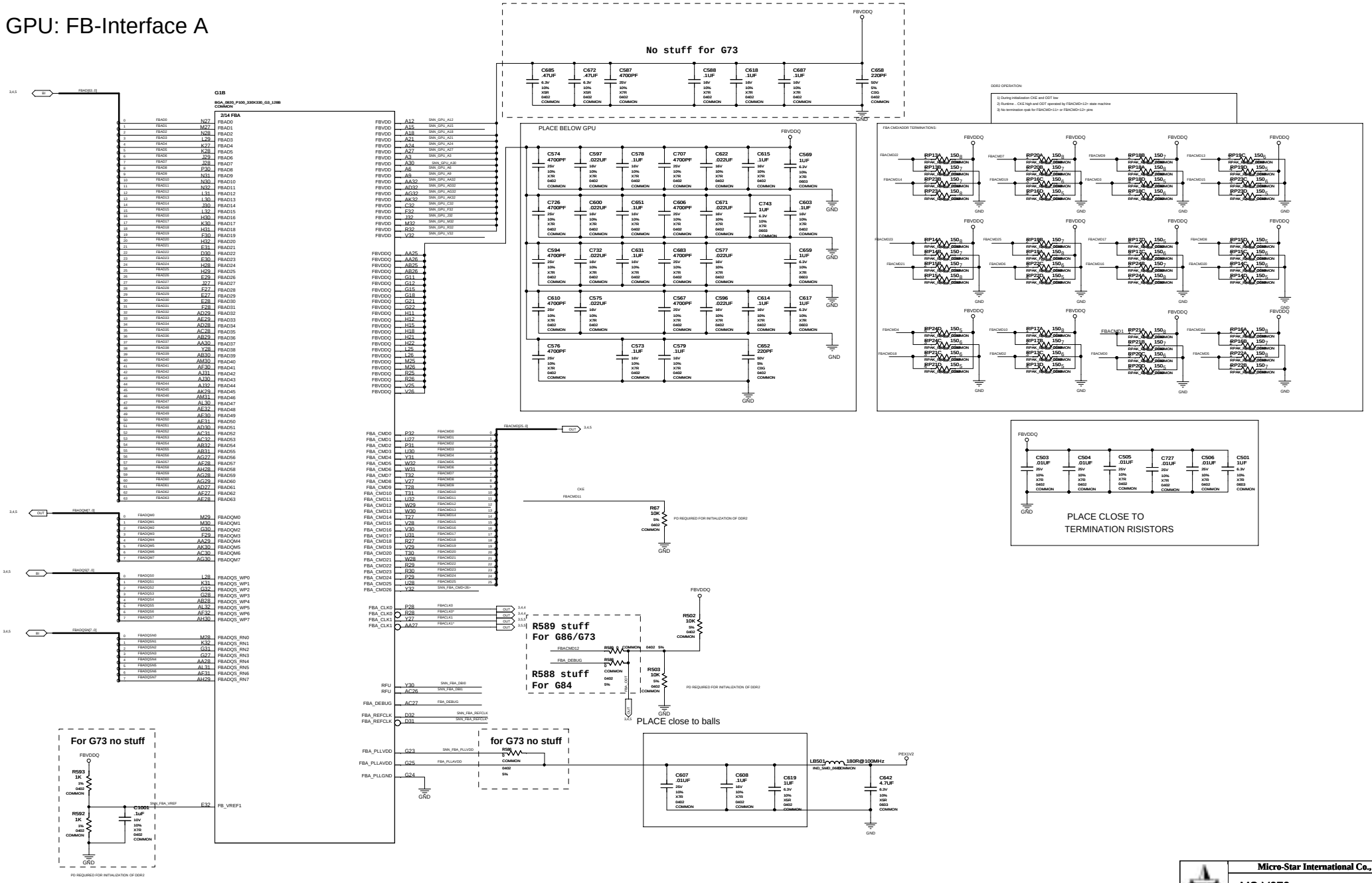
16X PCIe Interface



GPU: FB-Interface A



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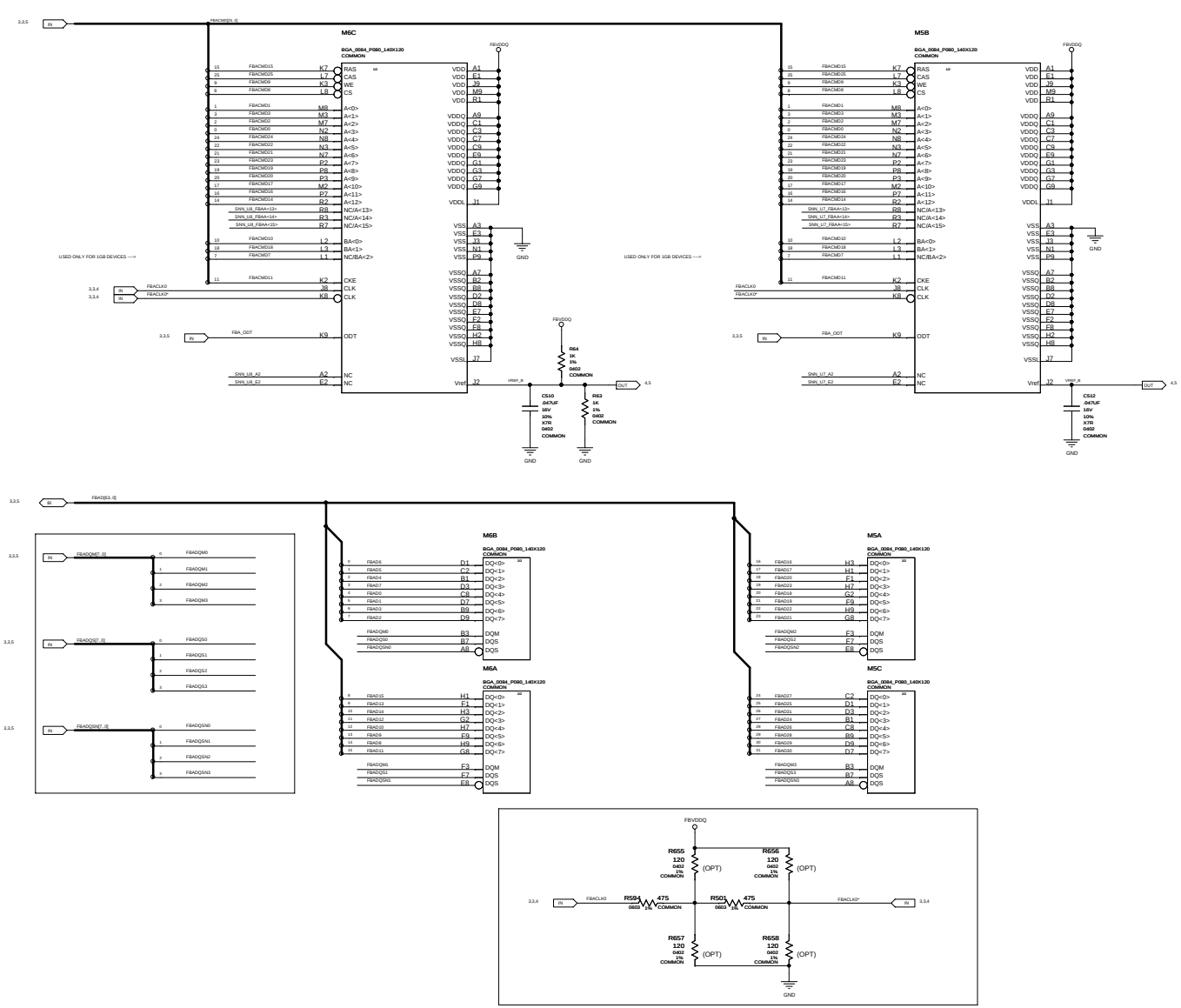
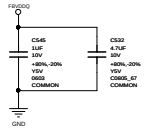
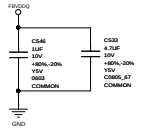
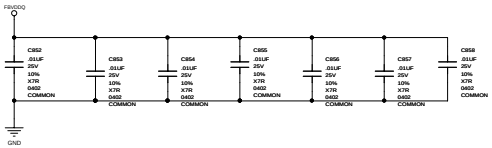
FBA MEMORY 1st bank 0..31

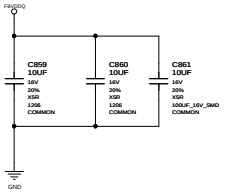
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY











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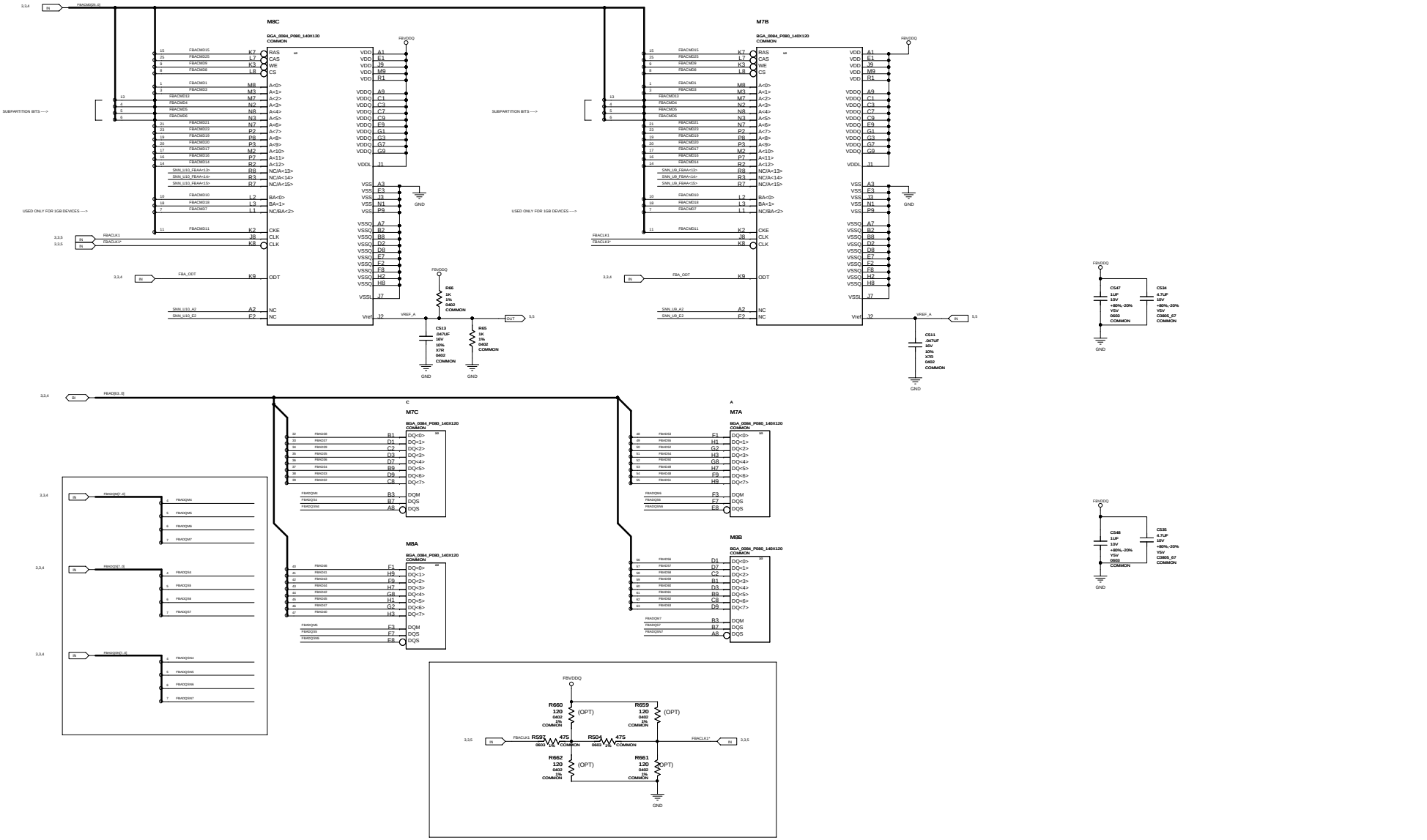
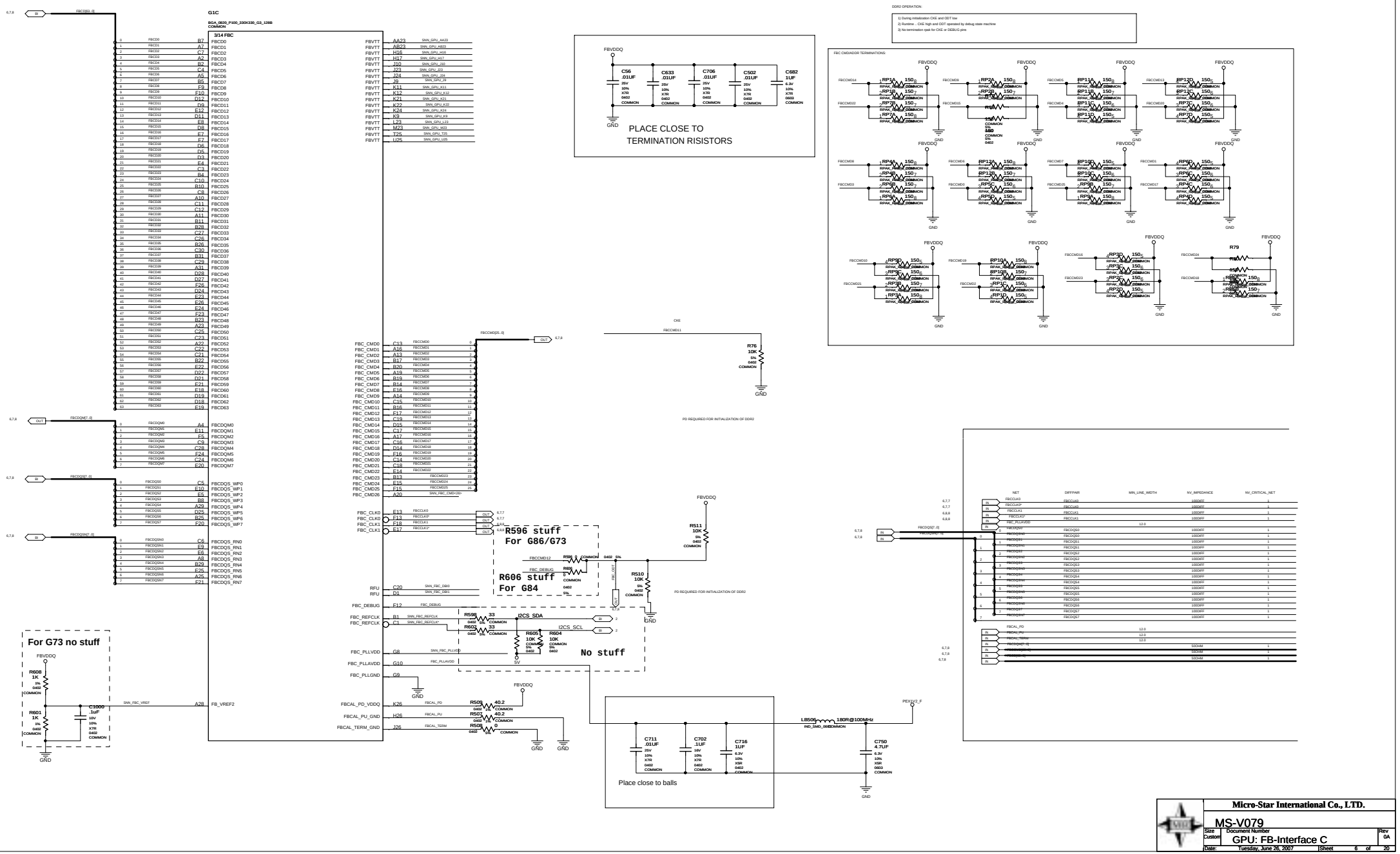
FBA MEMORY 1st bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

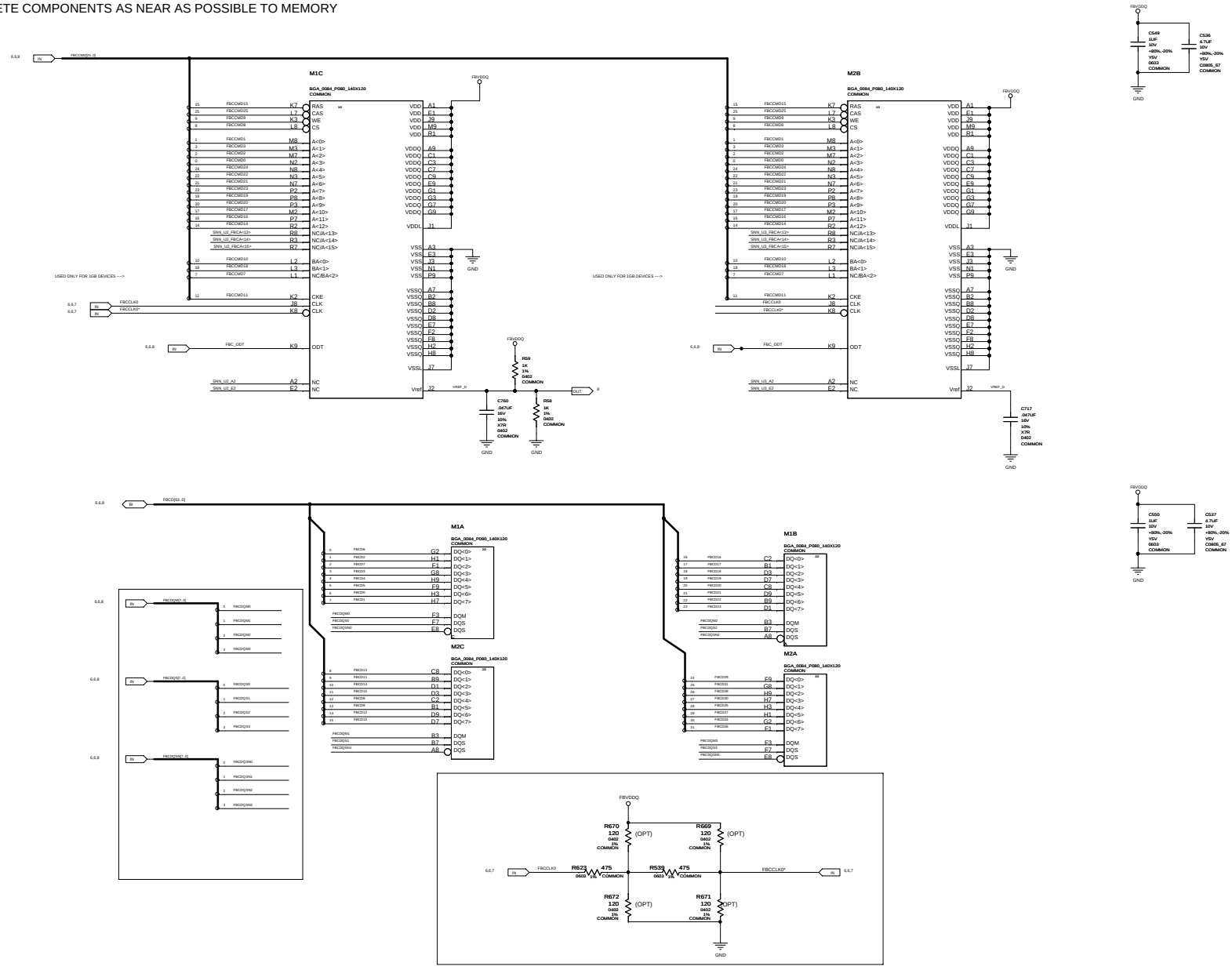


GPU: FB-Interface C



FBC MEMORY 2nd bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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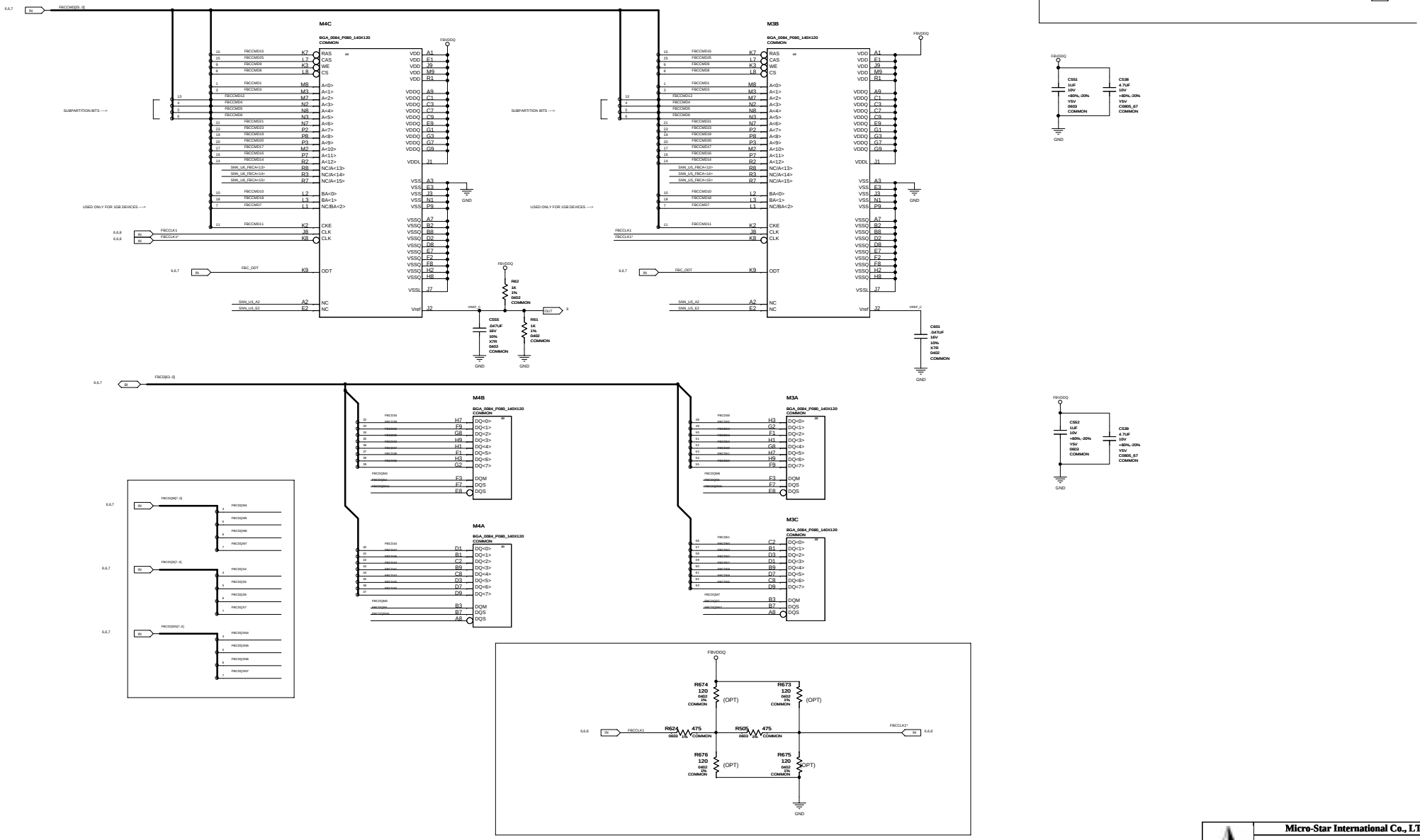
FBC MEMORY 2nd bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



NAME MIN_LINE_WIDTH

VREF_C 12.0 VREF_D 12.0

C551 1UF 10V +80%,-20% Y5V 0603 COMMON

C538 4.7UF 10V +80%,-20% Y5V C0805_67 COMMON

C552 1UF 10V +80%,-20% Y5V 0603 COMMON

C538 4.7UF 10V +80%,-20% Y5V C0805_67 COMMON

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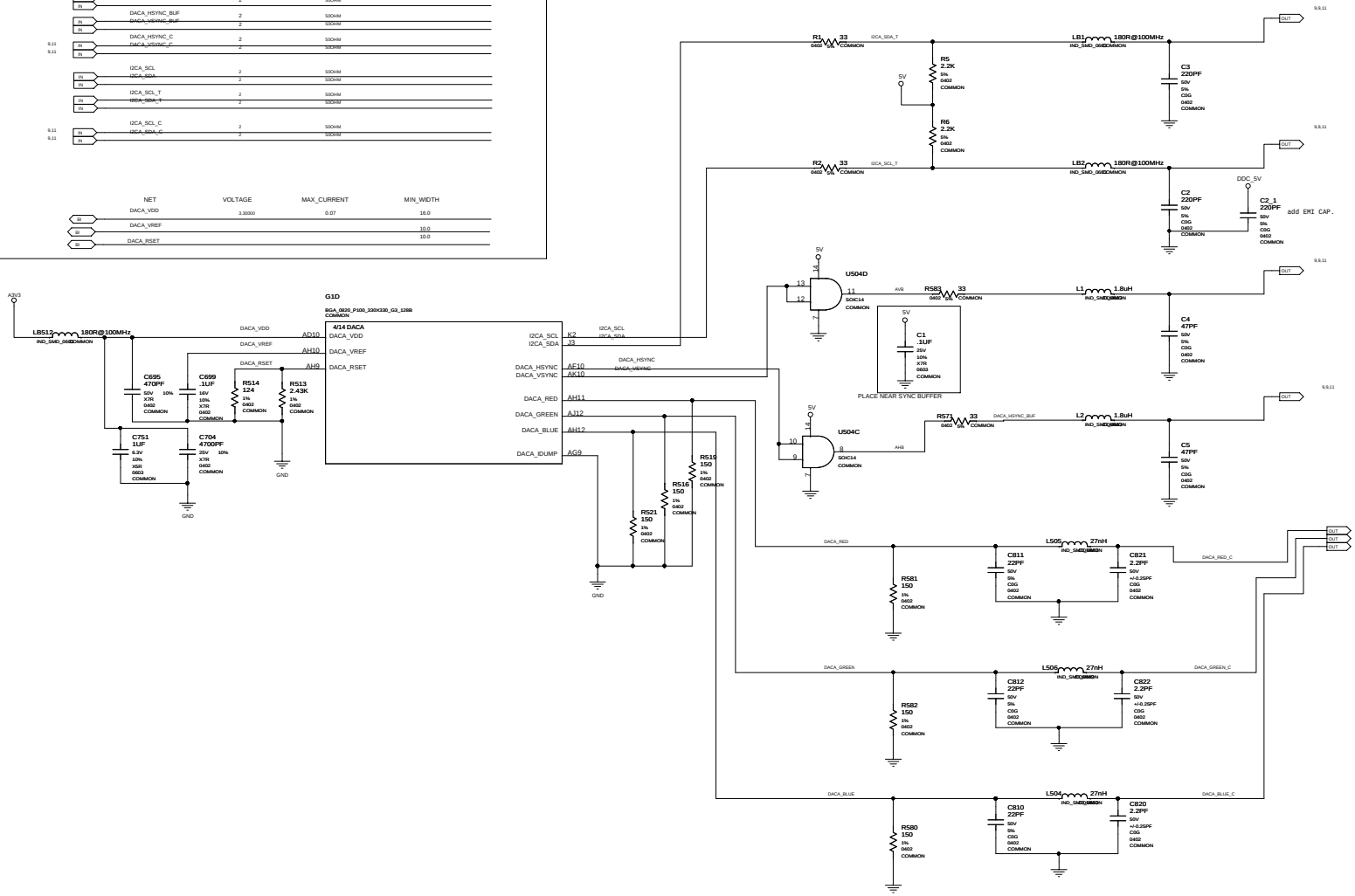
Primary Display (DACA), Slim DB15

DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACA_RED	1	50OHM	
DACA_GREEN	1	50OHM	
DACA_BLUE	1	50OHM	
DACA_RED_C	1	50OHM	
DACA_GREEN_C	1	50OHM	
DACA_BLUE_C	1	50OHM	
DACA_HSYNC	2	50OHM	
DACA_VSYNC	2	50OHM	
AVB	2	50OHM	
DACA_HSYNC_BUF	2	50OHM	
DACA_VSYNC_BUF	2	50OHM	
DACA_HSYNC_C	2	50OHM	
DACA_VSYNC_C	2	50OHM	
I2CA_SCL	2	50OHM	
I2CA_SDA	2	50OHM	
I2CA_SCL_T	2	50OHM	
I2CA_SDA_T	2	50OHM	
I2CA_SCL_C	2	50OHM	
I2CA_SDA_C	2	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACA_VDD	3.30000	0.07	16.0
DACA_VREF			10.0
DACA_RSET			10.0

DACA RGB-FILTER



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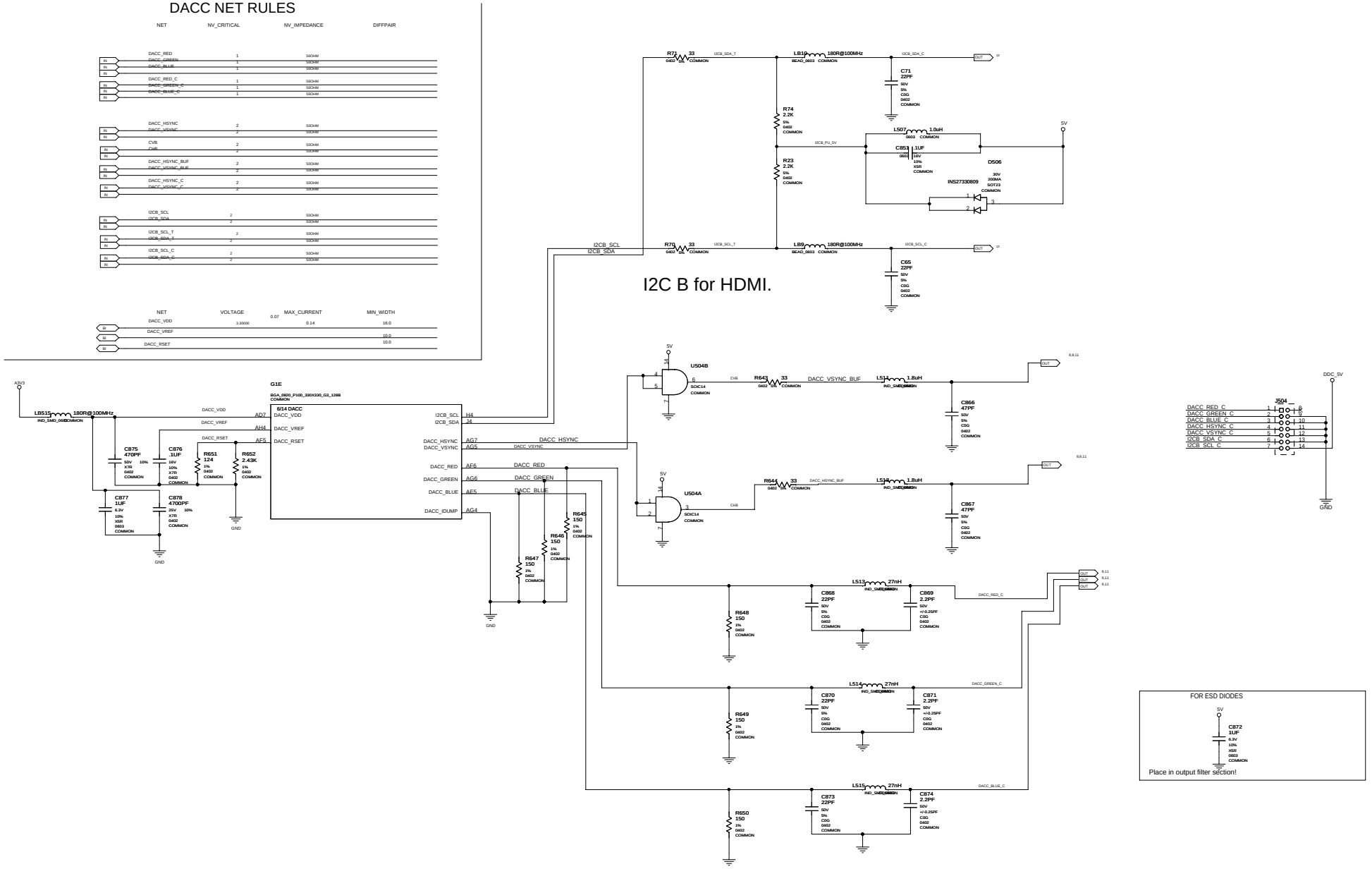
Secondary Display (DACC), DB15



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MS-V079	
Size: Custom	Document Number: Secondary Display (DACC), DB15
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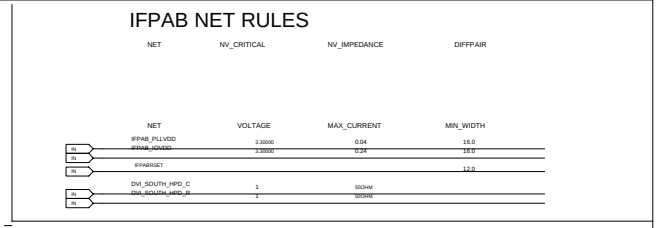
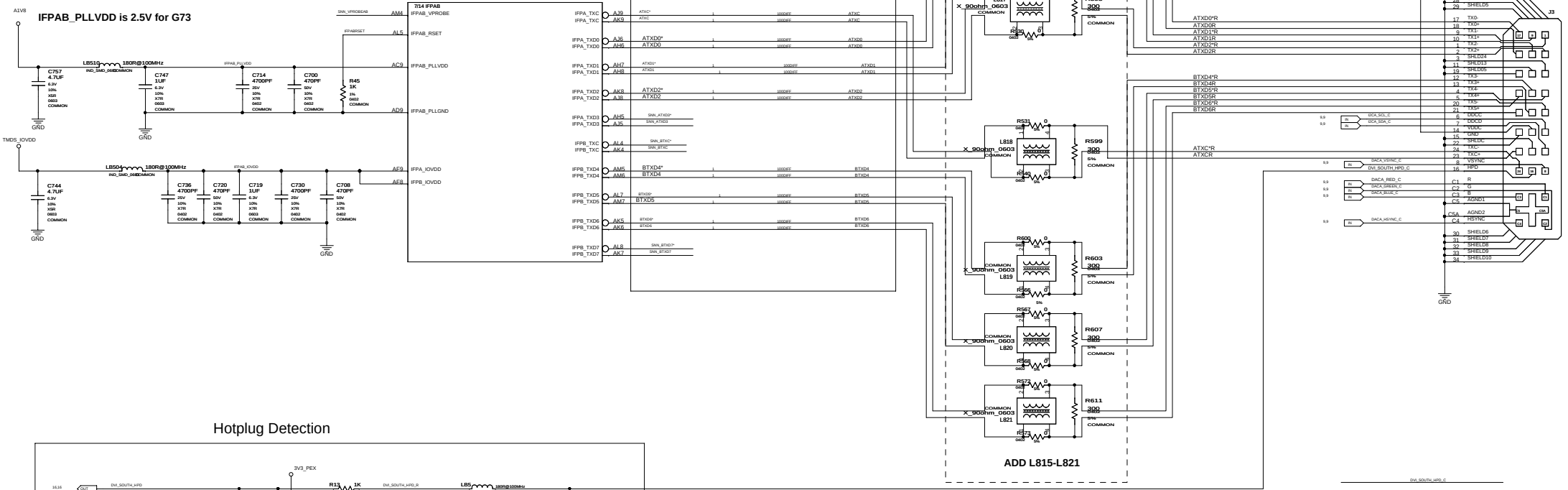
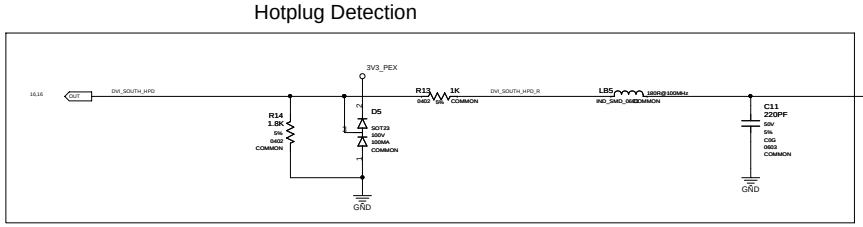
INTERNAL TMDS .. LINK A & B







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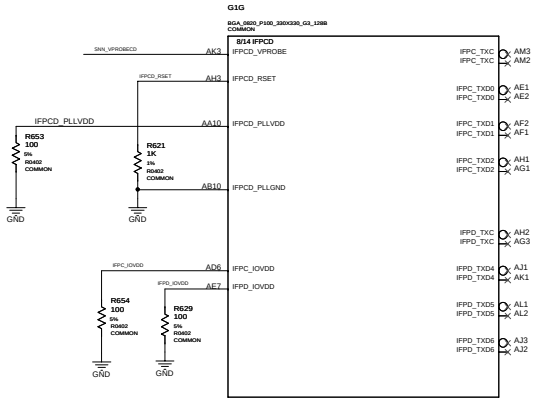
INTERNAL TMDS .. LINK C

IFPAB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPCD_RSET	1	50OHM	
DVI_MID_HPD_C	1	50OHM	
DVI_MID_HPD_R	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPCD_PLLVDD	3.30000	0.04	16.0
IFPC_IOVDD	2.20000	0.12	16.0
IFPD_IOVDD	2.20000	0.12	16.0



CEC pullup and clamping must be disconnected from HDMI connector when Power down

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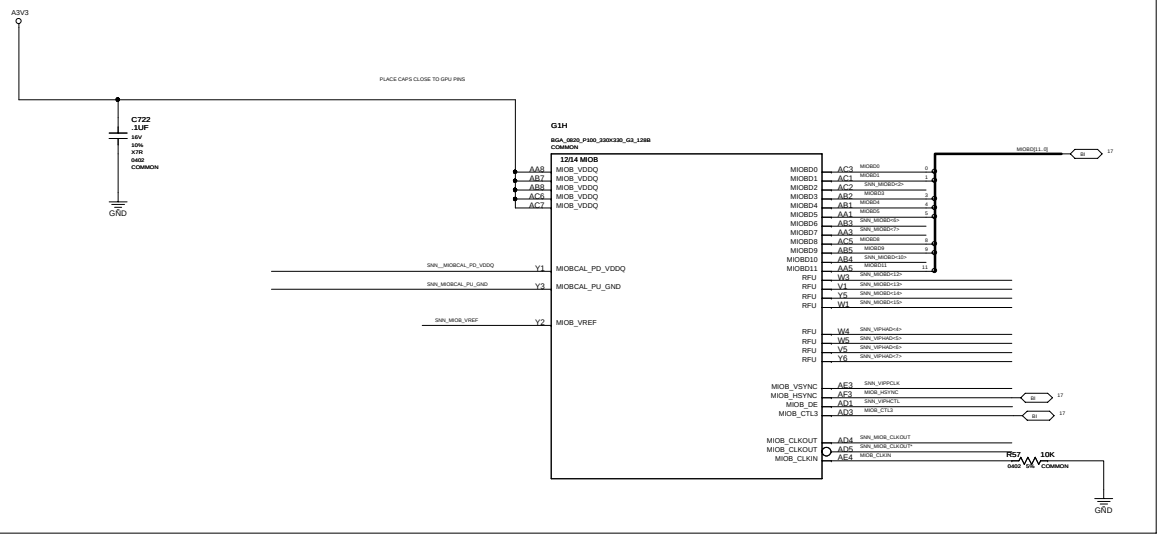
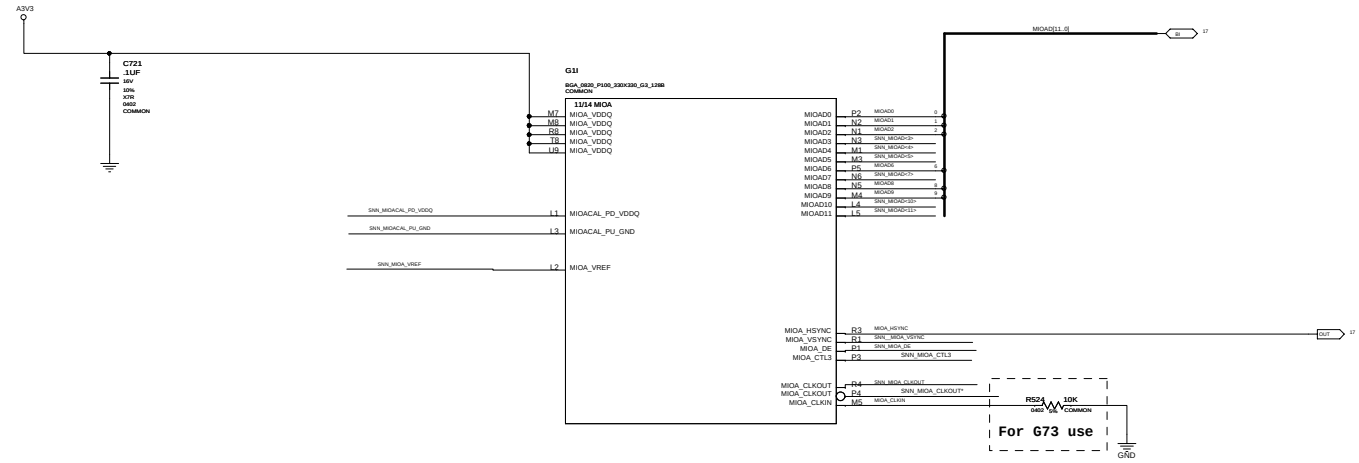
G3 VIP/MIOB/MIOA

G3 VIP/MIOB



G3 MIOA



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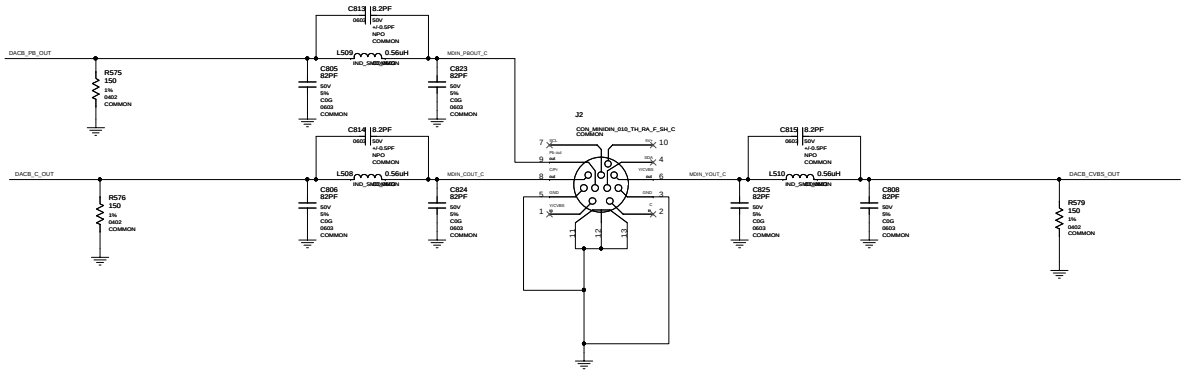
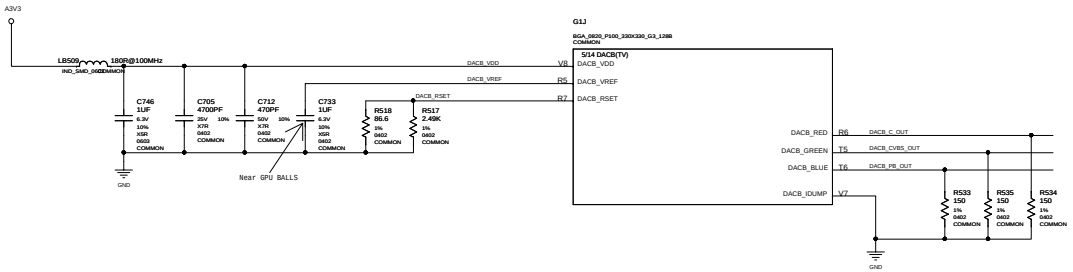
DACB .. MiniDIN VIDEO OUT CONNECTOR

DACB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACB_C_OUT	1	56OHM	
MDIN_COUT_C	1	56OHM	
DACB_CVBS_OUT	1	56OHM	
MDIN_YOUT_C	1	56OHM	
DACB_PB_OUT	1	56OHM	
MDIN_PBOUT_C	1	56OHM	
MDIN_SCL_C	2	50OHM	
MDIN_SDA_C	2	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACB_VDD	3.30000	0.07	16.0
DACB_VREF			16.0
DACB_RSET			16.0





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Size: Custom	Document Number: DACB .. MiniDIN VIDEO OUT	Rev: 0A
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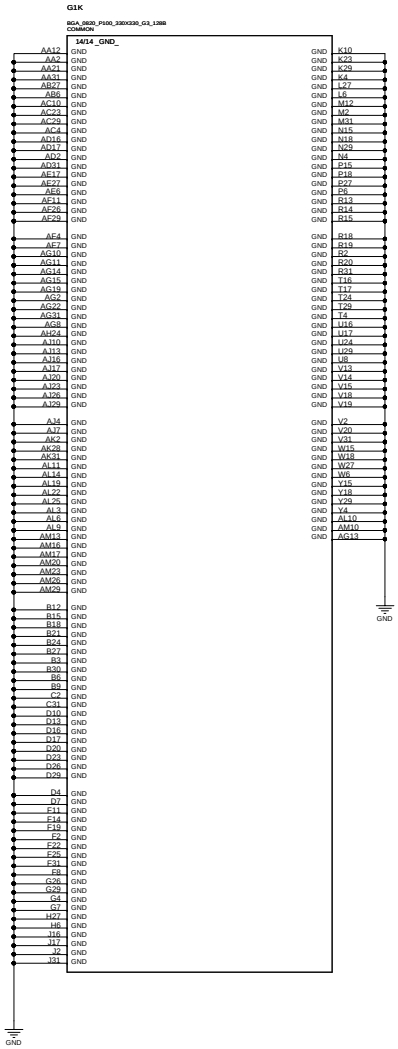
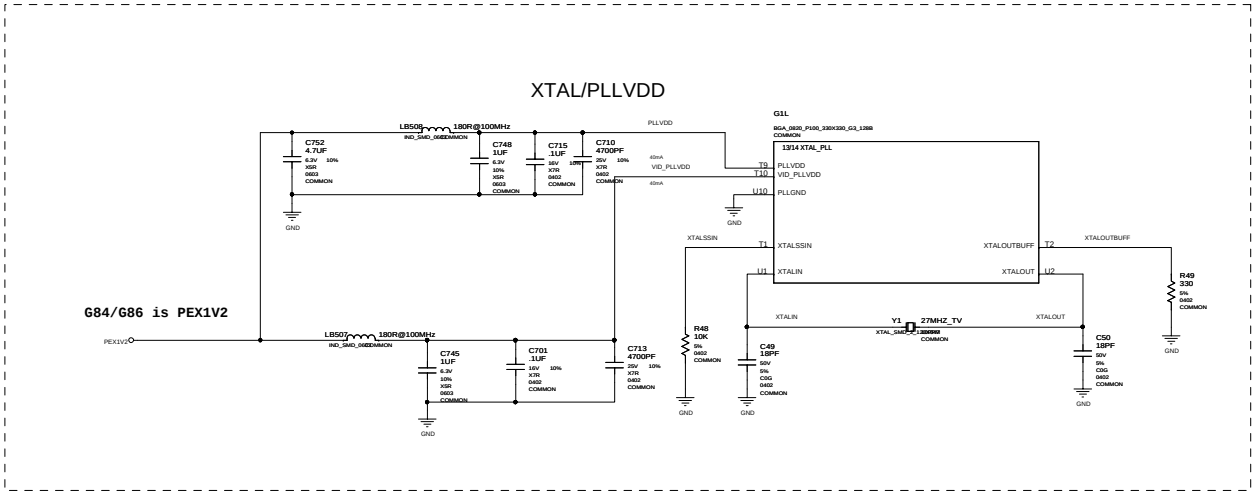
GND/XTAL/PLLVDD





NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
XTALIN	1	50OHM	
XTALOUT	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
PLL_VDD	2.5V	0.3	12MIL
VID_PLLVDD	2.5V	0.3	12.0

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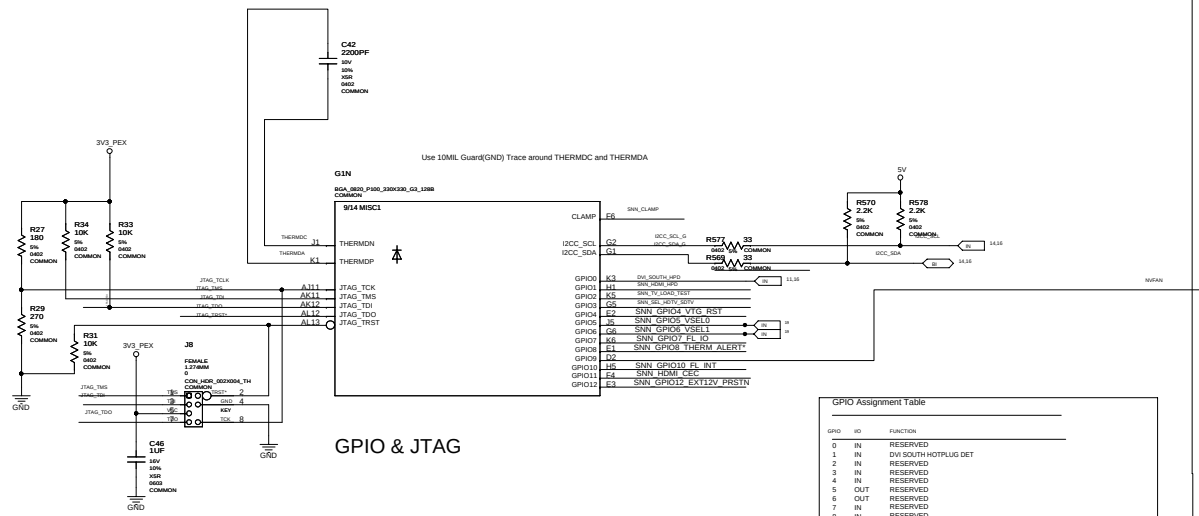
GPIO / JTAG / HDCP / BIOS / SPDIF

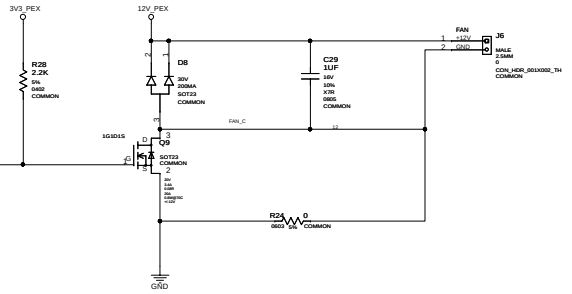


GPIO & JTAG

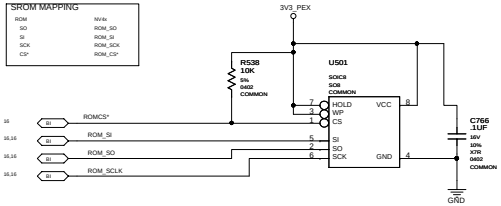
GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	RESERVED
1	IN	DVI SOUTH HOTPLUG DET
2	IN	RESERVED
3	IN	RESERVED
4	IN	RESERVED
5	OUT	RESERVED
6	OUT	RESERVED
7	IN	RESERVED
8	IN	RESERVED
9	OUT	FAN Control(ON/OFF)
10	OUT	RESERVED
11	IN	RESERVED
12	IN	RESERVED

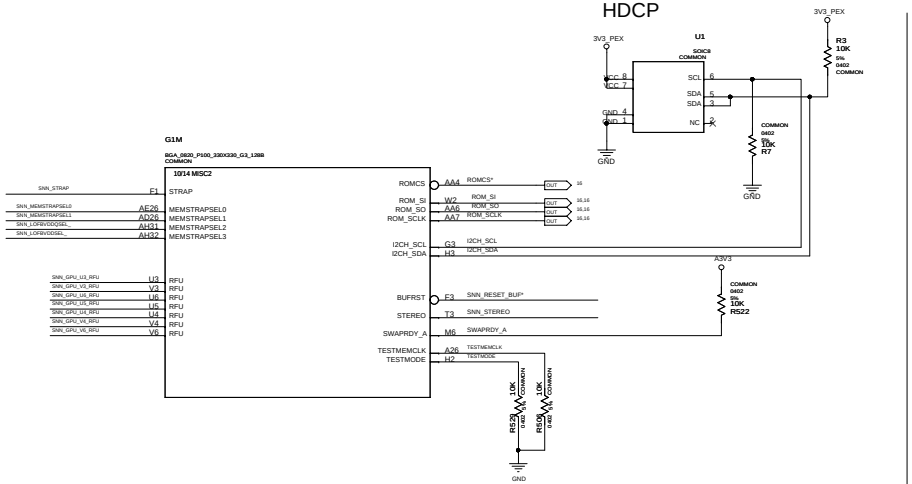
GPIO ON/OFF FAN Control



BIOS (serial)



HDCP



MISC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
I2CC_SCL	2	50OHM	
I2CC_SDA	2	50OHM	
I2CC_SCL_G	2	50OHM	
I2CC_SDA_G	2	50OHM	
I2CH_SCL	2	50OHM	
I2CH_SDA	2	50OHM	
ROM_CS*	2	50OHM	
ROM_SI	2	50OHM	
ROM_SO	2	50OHM	
ROM_SCLK	2	50OHM	
DVI_SOUTH_HPD	2	50OHM	
SPDIF	1	50OHM	
SPDIF_IN	1	50OHM	

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GPIO / JTAG / HDCP / BIOS / SPDIF

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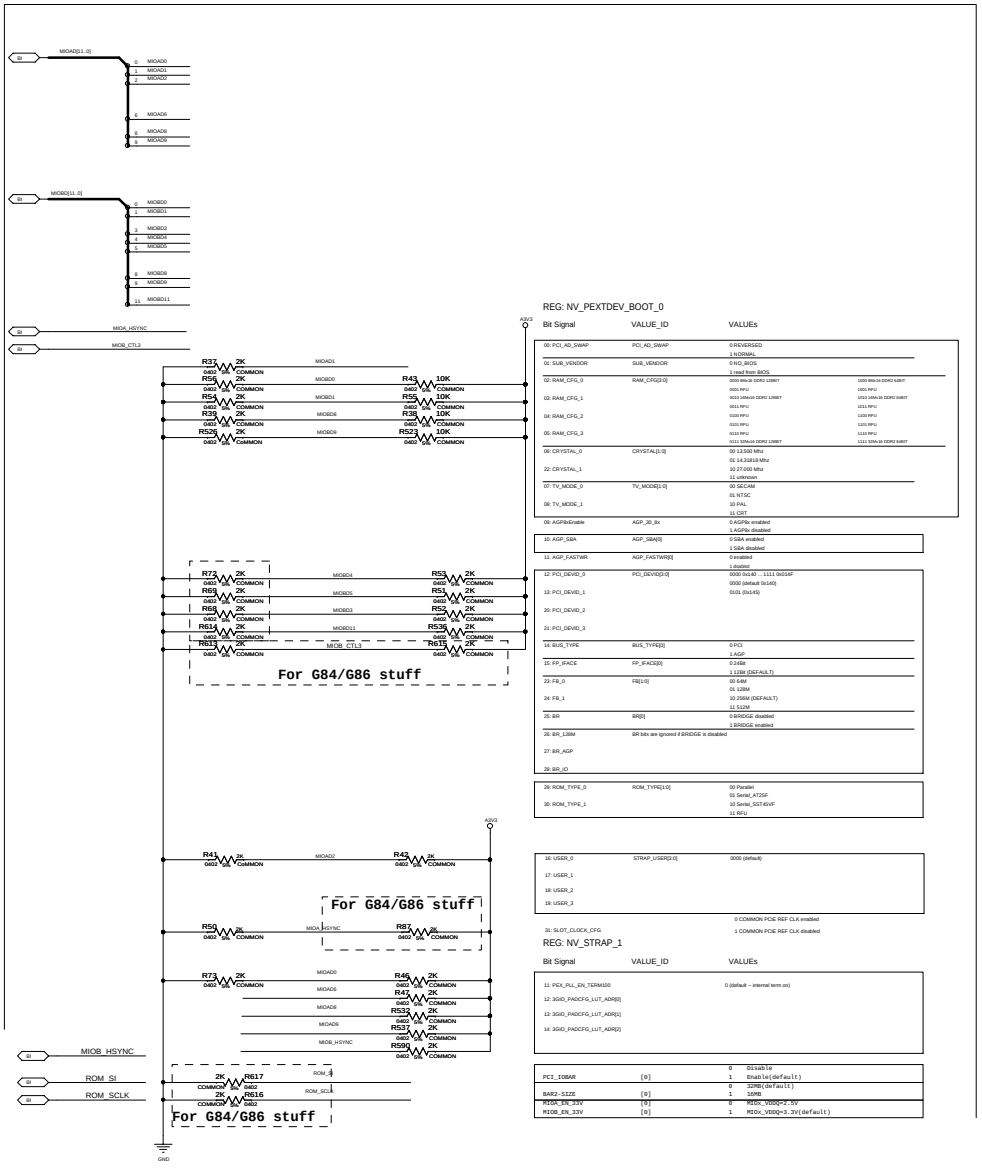
STRAPS, Mechanical Parts

Straps

Assembly: BIOS



REG: NV_PEXTDEV_BOOT_0

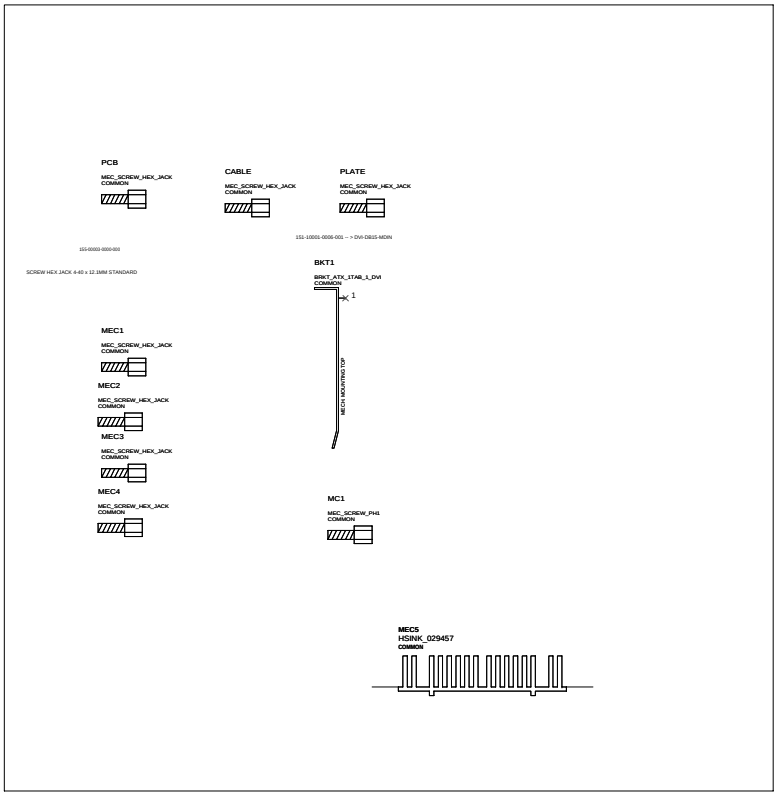
Bit	Signal	VALUE_ID	VALUEs
00: PCI_AD_SWAP		PCI_AD_SWAP	0 REVERSED 1 NORMAL
01: SUB_VENDOR		SUB_VENDOR	0 NO_BIOS 1 Read from BIOS
02: RAM_CFG_0		RAM_CFG[3:0]	0000 64bit DDR2 128BIT 0001 RFU 0010 128bit DDR2 128BIT 0011 RFU 0100 RFU 0101 RFU 0110 RFU 0111 32bit DDR2 128BIT 1000 256bit DDR2 64BIT 1001 RFU 1010 256bit DDR2 64BIT 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 32bit DDR2 64BIT
03: RAM_CFG_1			
04: RAM_CFG_2			
05: RAM_CFG_3			
06: CRYSTAL_0		CRYSTAL[1:0]	00 13.500 Mhz 01 14.31818 Mhz 10 27.000 Mhz 11 unknown
22: CRYSTAL_1			
07: TV_MODE_0		TV_MODE[1:0]	00 SECAM 01 NTSC 10 PAL 11 CRT
08: TV_MODE_1			
09: AGPBkEnable		AGP_30_8x	0 AGPBk enabled 1 AGPBk disabled
10: AGP_SBA		AGP_SBA[0]	0 SBA enabled 1 SBA disabled
11: AGP_FASTWR		AGP_FASTWR[0]	0 enabled 1 disabled
12: PCI_DEVID_0		PCI_DEVID[3:0]	0000 0x140 ... 1111 0x014F 0000 (default 0x140)
13: PCI_DEVID_1			0101 (0x145)
20: PCI_DEVID_2			
21: PCI_DEVID_3			
14: BUS_TYPE		BUS_TYPE[0]	0 PCI 1 AGP
15: FP_IFACE		FP_IFACE[0]	0 24bit 1 12bit (DEFAULT)
23: FB_0		FB[1:0]	00 64M 01 128M
24: FB_1			10 256M (DEFAULT) 11 512M
25: BR		BR[0]	0 BRIDGE disabled 1 BRIDGE enabled
26: BR_128M		BR bits are ignored if BRIDGE is disabled	
27: BR_AGP			
28: BR_IO			
29: ROM_TYPE_0		ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F 10 Serial_SST45VF 11 RFU
30: ROM_TYPE_1			
16: USER_0		STRAP_USER[3:0]	0000 (default)
17: USER_1			
18: USER_2			
19: USER_3			
31: SLOT_CLOCK_CFG			0 COMMON PCIE REF CLK enabled 1 COMMON PCIE REF CLK disabled

REG: NV_STRAP_1

Bit	Signal	VALUE_ID	VALUEs
11: PEX_PLL_EN_TERM100			0 (default – internal term on)
12: 3GIO_PADCFG_LUT_ADR[0]			
13: 3GIO_PADCFG_LUT_ADR[1]			
14: 3GIO_PADCFG_LUT_ADR[2]			

		0	Disable
PCI_IOBAR	[0]	1	Enable(default)
		0	32MB(default)
BAR2-SIZE	[0]	1	16MB
MIOA_EN_33V	[0]	0	MIOx_VDDQ=2.5V
MIOB_EN_33V	[0]	1	MIOx_VDDQ=3.3V(default)

Mechanical parts



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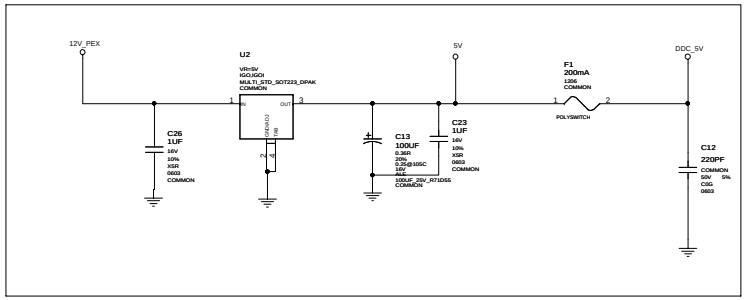
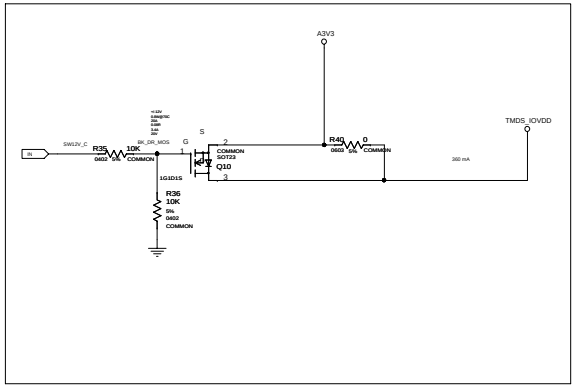
Power Supply:TMDS_IOVDD/A3V3/5V/DAC_REF

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	0.1	12.0	5.00000
A2V5	0.96	25.0	2.50000
TMDS_IOVDD	0.24	20.0	3.30000
A3V3	0.4	20.0	3.30000
GND		25.0	0.000000

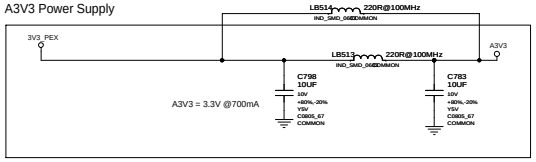
DDC 5V



TMDS IO SUPPLY WITH BACKDRIVE PROTECTION



A3V3 Power Supply

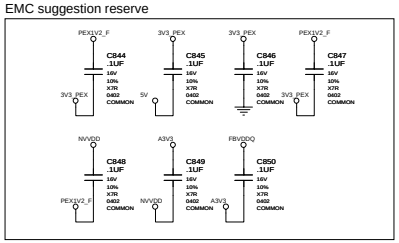


FM1 FM4

FM2 FM5

FM3 FM6

EMC suggestion reserve



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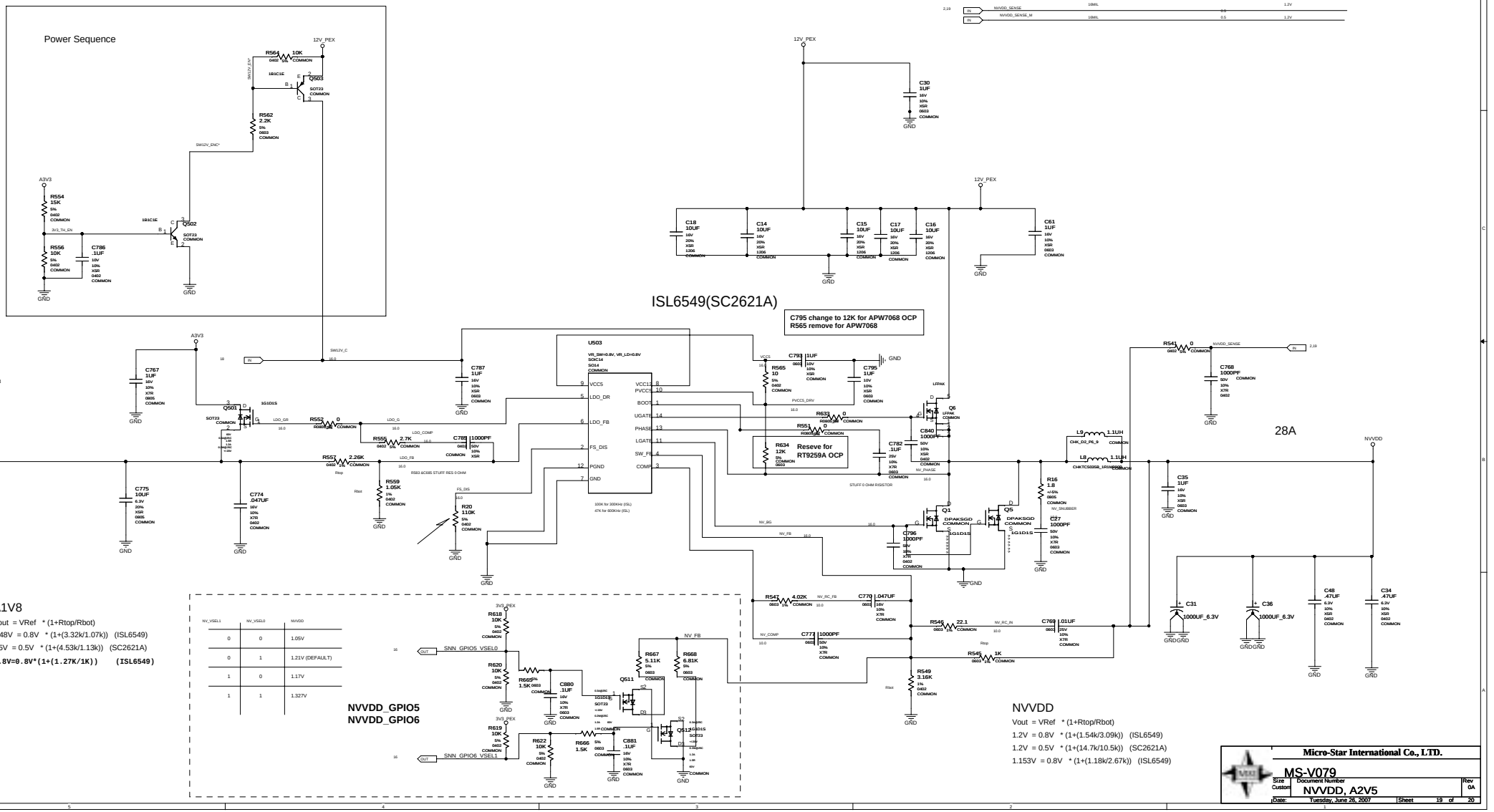
PowerSupplyI: NVVDD, A2V5

Net Name	LINE_WIDTH	Current	Voltage
12V_F	20MIL	3	12V
NVVDD	20MIL	15	1.2V
PEX1V2	24MIL	1.5	1.20000
NVVDD_SENSE	10MIL	0.5	1.2V
NVVDD_SENSE_M	10MIL	0.5	1.2V



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MS-V079		
Size: Custom	Document Number: NVVDD, A2V5	Rev: 0A
Date: Tuesday, June 26, 2007	Sheet 19 of 20	

PowerSupplyIII: FBVDDQ,PEX1V2