

PG110-A00

GP108 64Bit GDDR5 X32

HDMI/DP + DVI-D/DP

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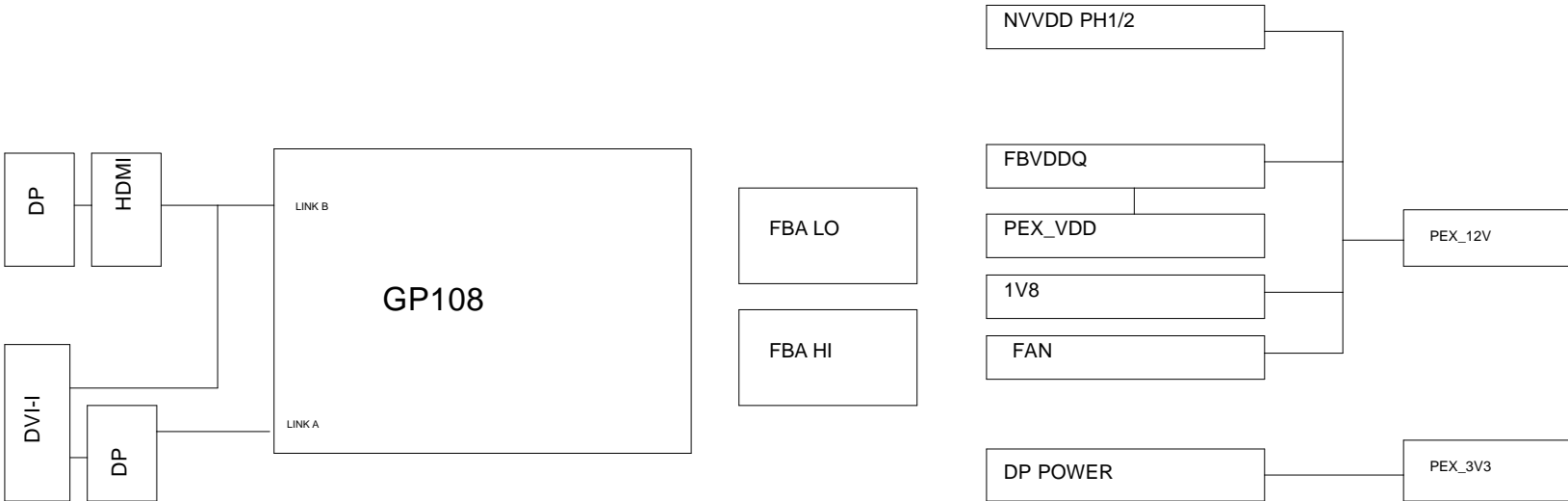
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Block Diagram

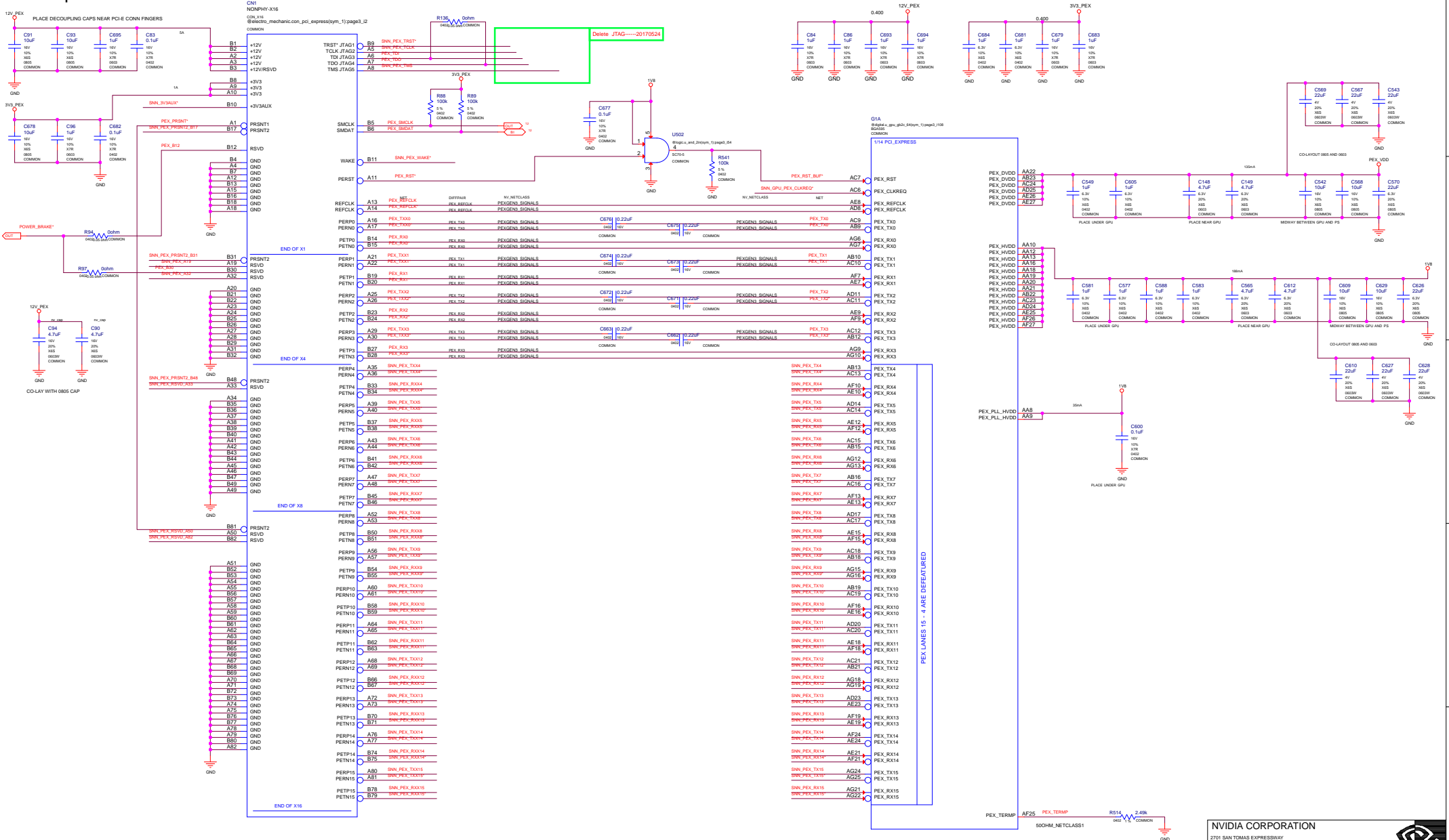



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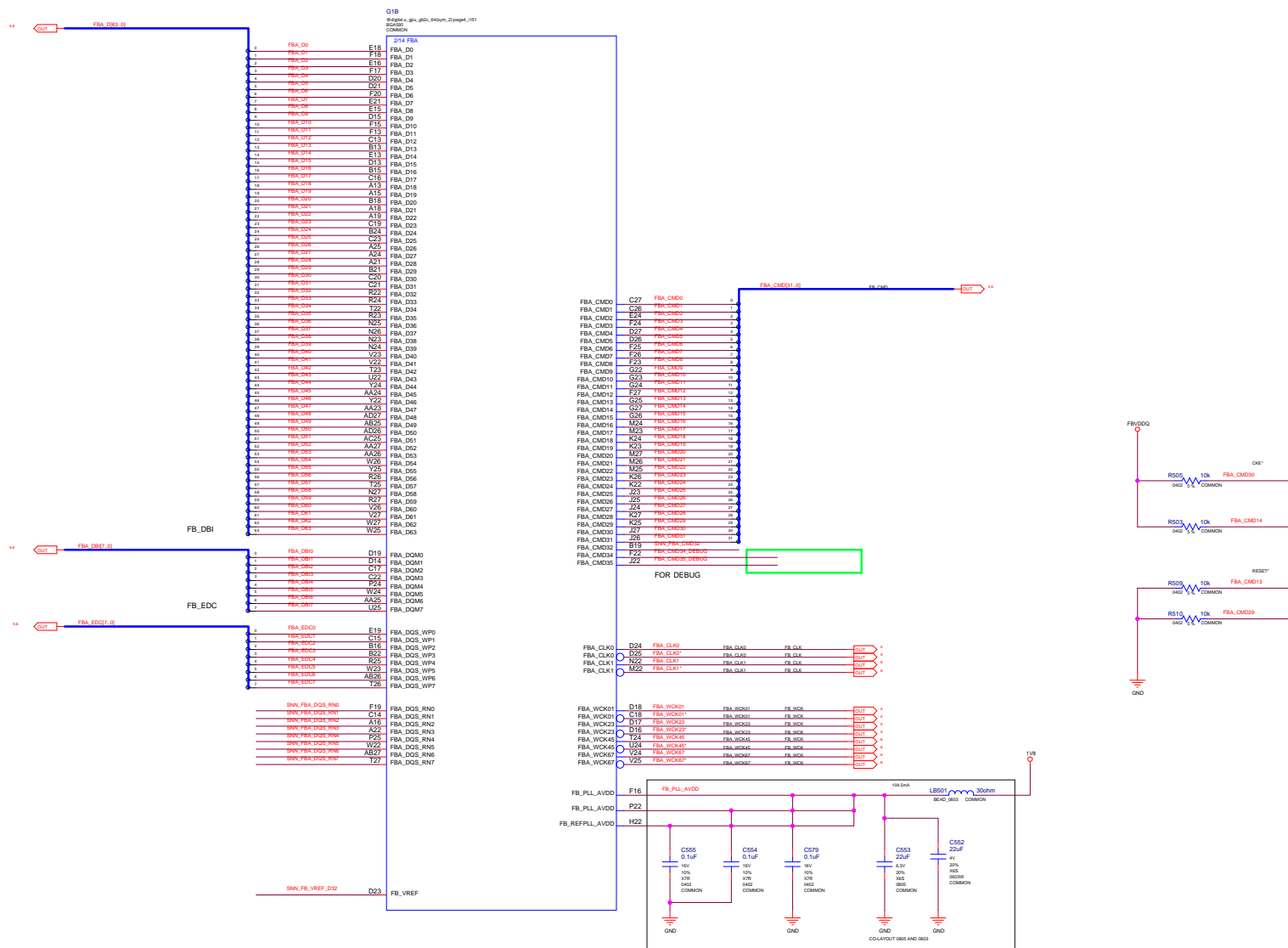
PCI Express



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## GPU Frame Buffer



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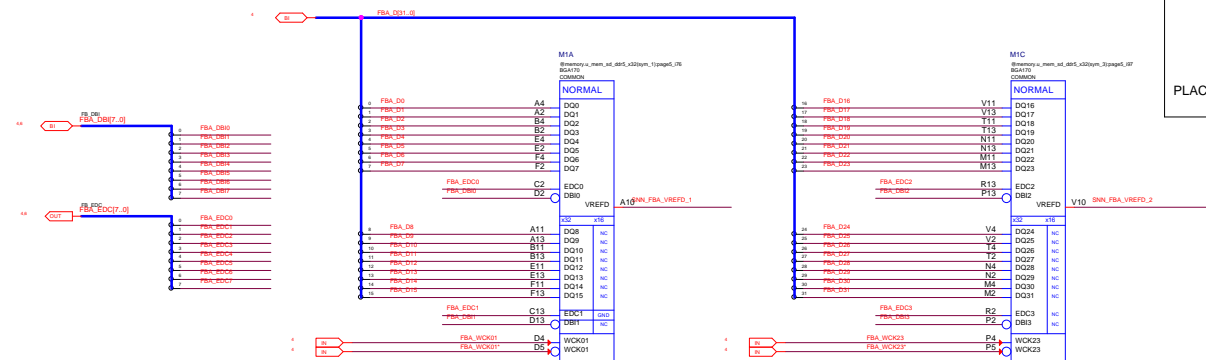
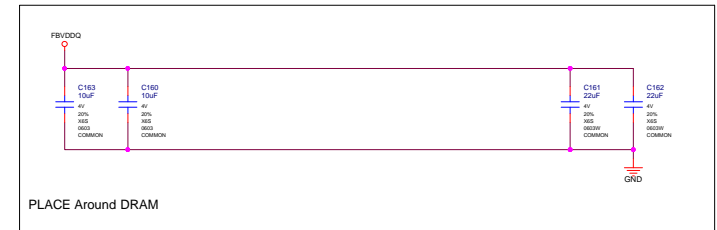
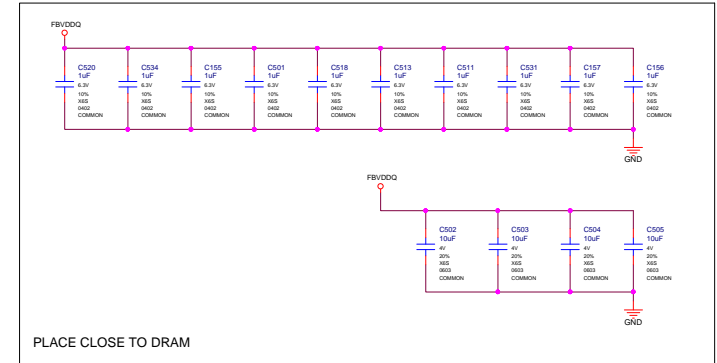
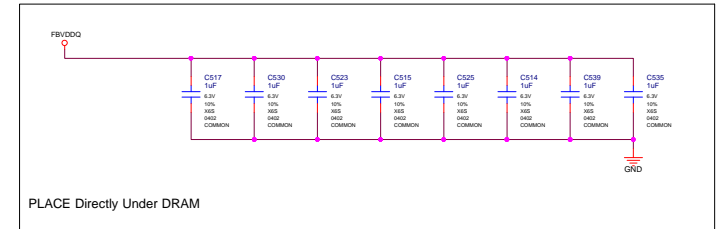
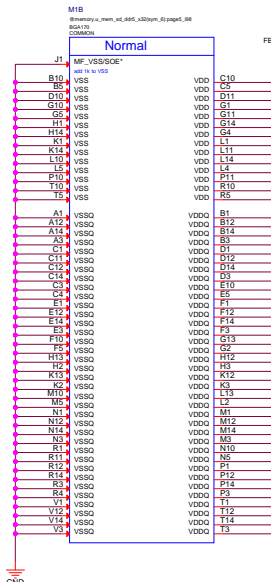
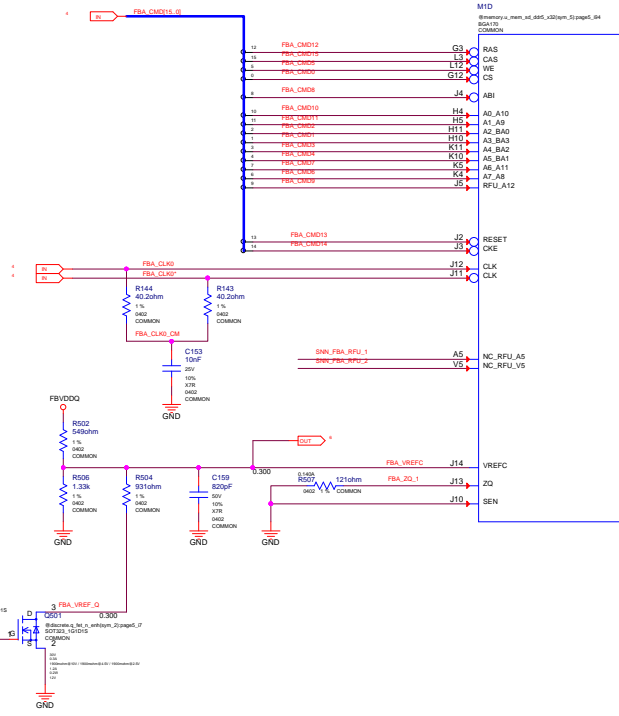
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MAY		PCB REV	PC110-A00
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STANDARDS		PCB REV	A

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## FBA bits 31..00

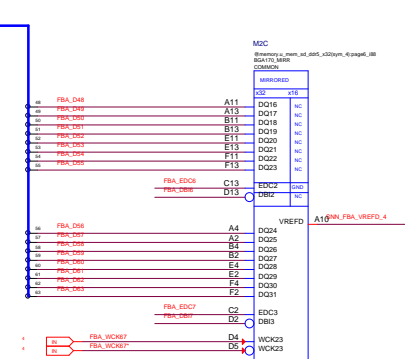
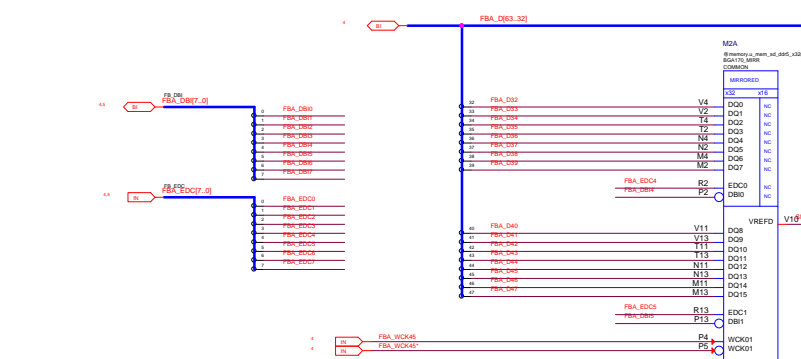
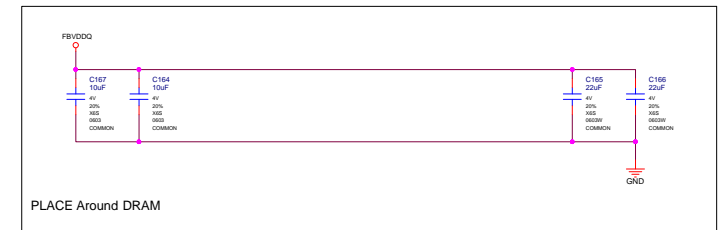
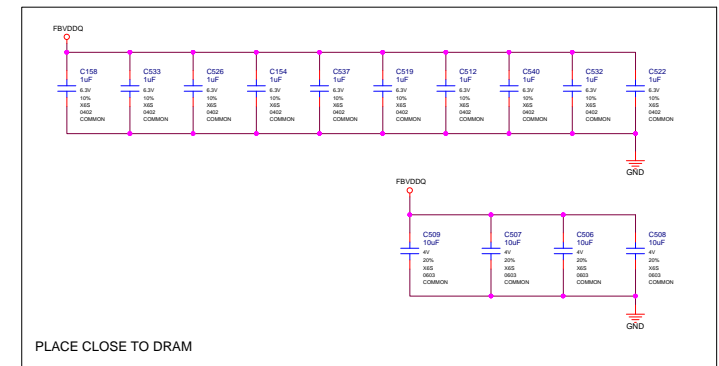
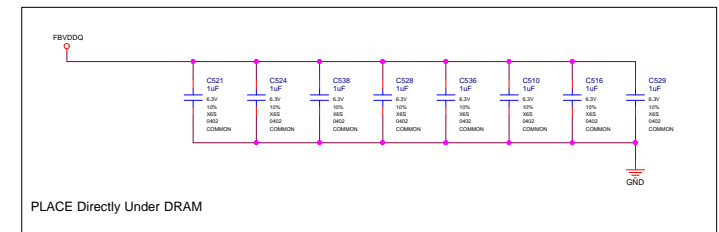
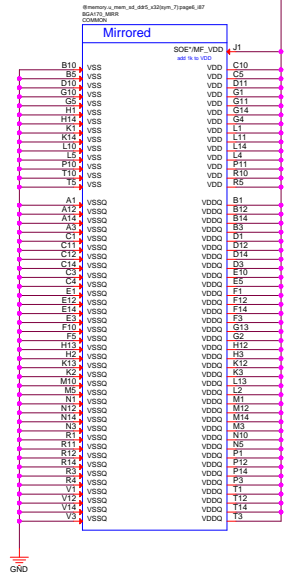
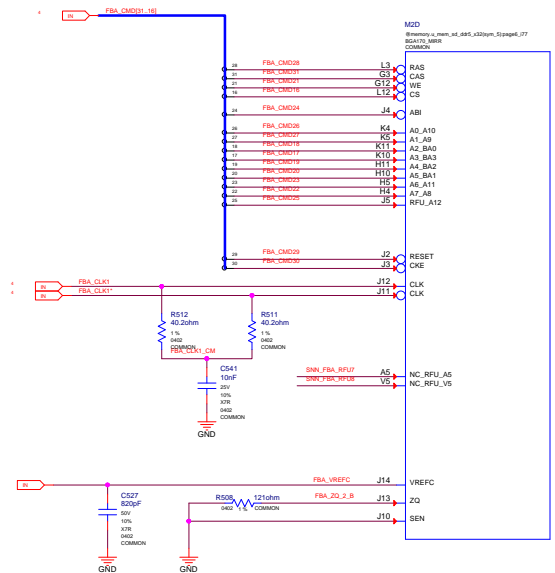
CMD	0.31	32.63
CMD0	CS <sup>1</sup>	
CMD1	A3_BA0	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A6_BA1	
CMD5	WEC	
CMD6	A7_A8	
CMD7	AB <sup>1</sup>	
CMD8	AB <sup>1</sup>	
CMD9	A12_RFU	
CMD10	AL_A11	
CMD11	A1_A9	
CMD12	BA0 <sup>1</sup>	
CMD13	RS1	
CMD14	CS <sup>1</sup>	
CMD15	CS <sup>1</sup>	
CMD16		CS <sup>1</sup>
CMD17		A3_BA0
CMD18		A4_BA2
CMD19		AB <sup>1</sup>
CMD20		WEC <sup>1</sup>
CMD21		AB <sup>1</sup>
CMD22		AB <sup>1</sup>
CMD23		AL_A11
CMD24		A7_A8
CMD25		A12_RFU
CMD26		AO_A10
CMD27		A1_A9
CMD28		RS <sup>1</sup>
CMD29		RS <sup>1</sup>
CMD30		CS <sup>1</sup>
CMD31		CS <sup>1</sup>



# FBA bits 63..32

QDDR5\_BGA170\_MMR

CMD	0..31	32..63
CMD0	C5*	
CMD1	A3,BA3	
CMD2	A2,BA2	
CMD3	A4,BA2	
CMD4	A5,BA1	
CMD5	WE*	
CMD6	A7,A8	
CMD7	A6,A11	
CMD8	AB*	
CMD9	A12,RFU	
CMD10	A0,A10	
CMD11	A1,A9	
CMD12	BA2*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		C5*
CMD17		A3,BA3
CMD18		A2,BA2
CMD19		A4,BA2
CMD20		A5,BA1
CMD21		WE*
CMD22		A7,A8
CMD23		A6,A11
CMD24		AB*
CMD25		A12,RFU
CMD26		A0,A10
CMD27		A1,A9
CMD28		BA2*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



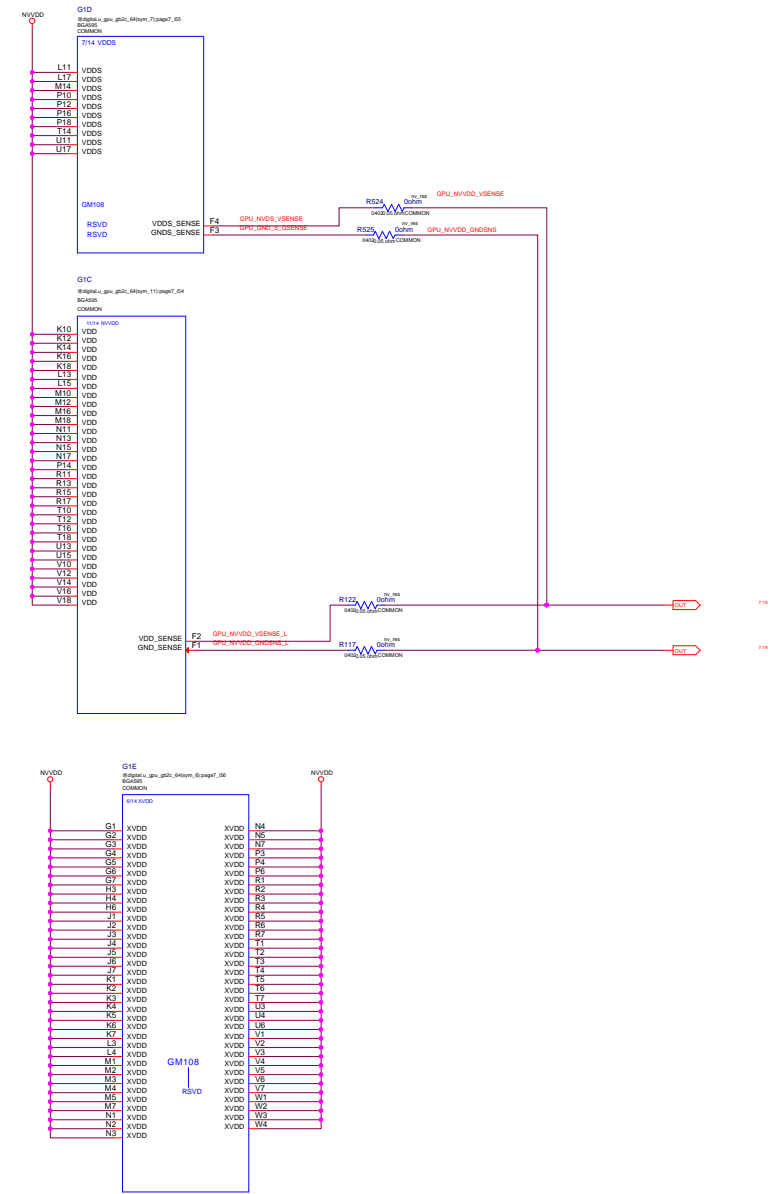
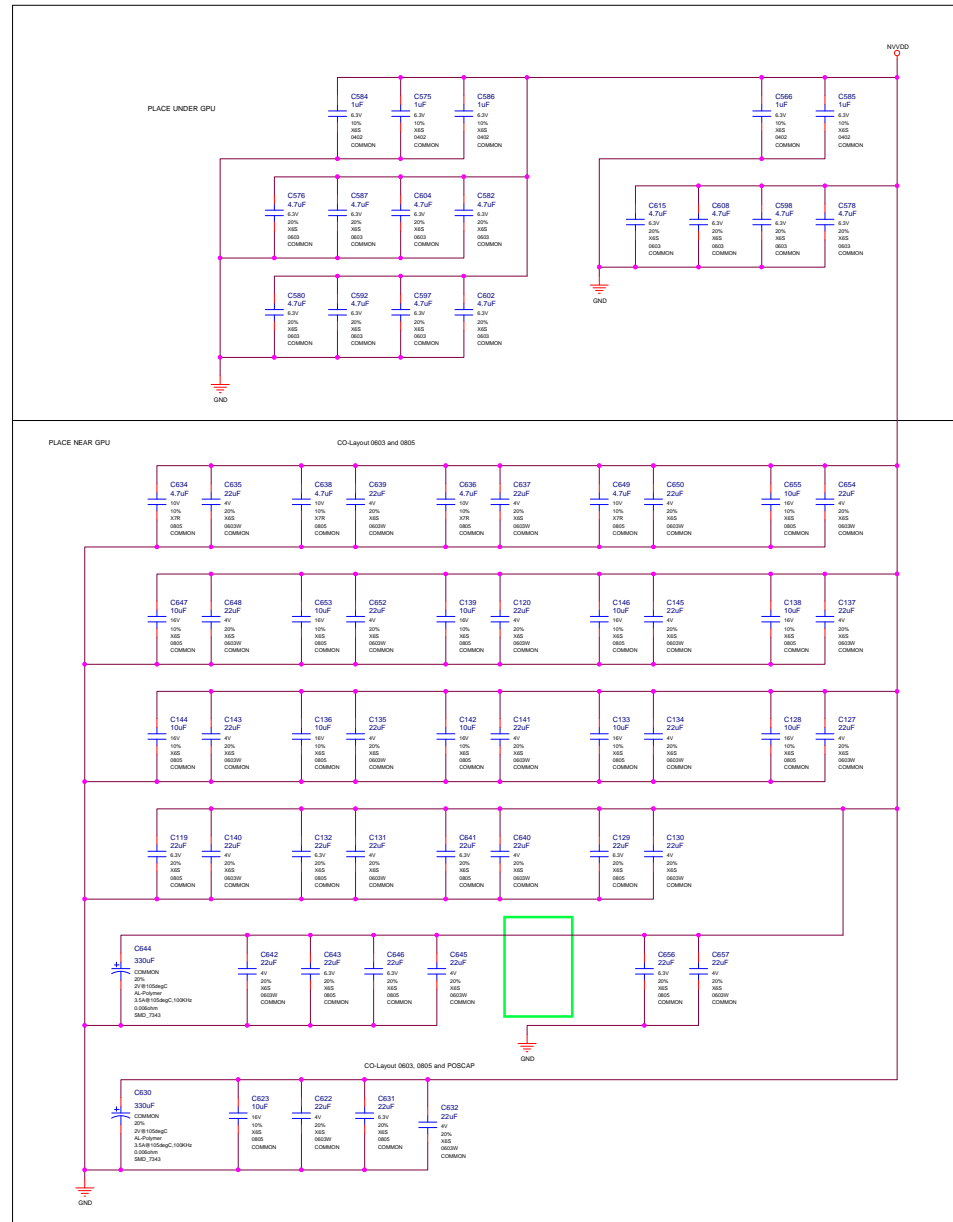
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## NVVVD Decoupling



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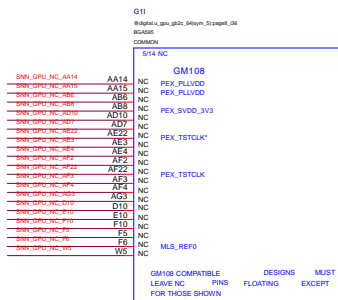
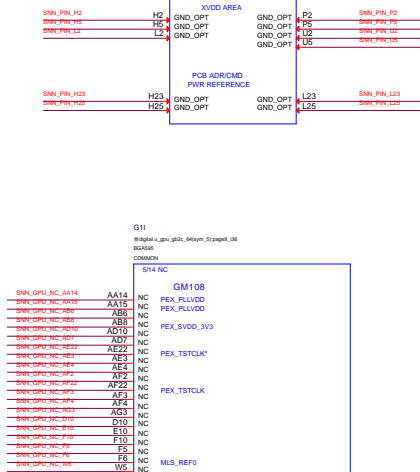
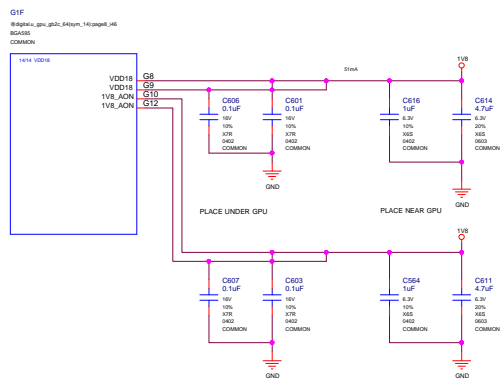
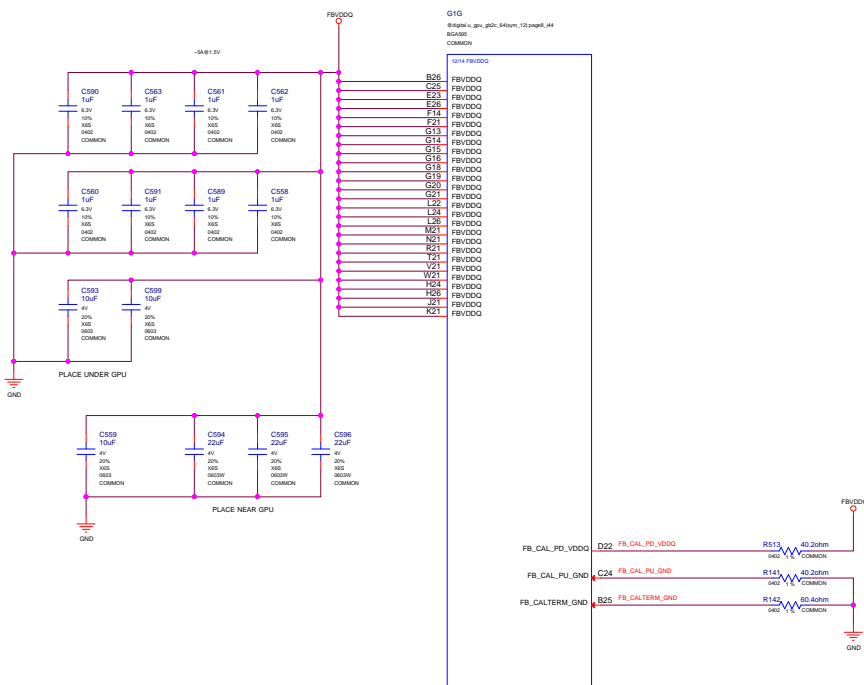
NV_PN	600-1G110-BASE-A00
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Figure 1 is a horizontal timeline. A vertical line divides the timeline into two sections. The left section is labeled 'H' and the right section is labeled 'H'.

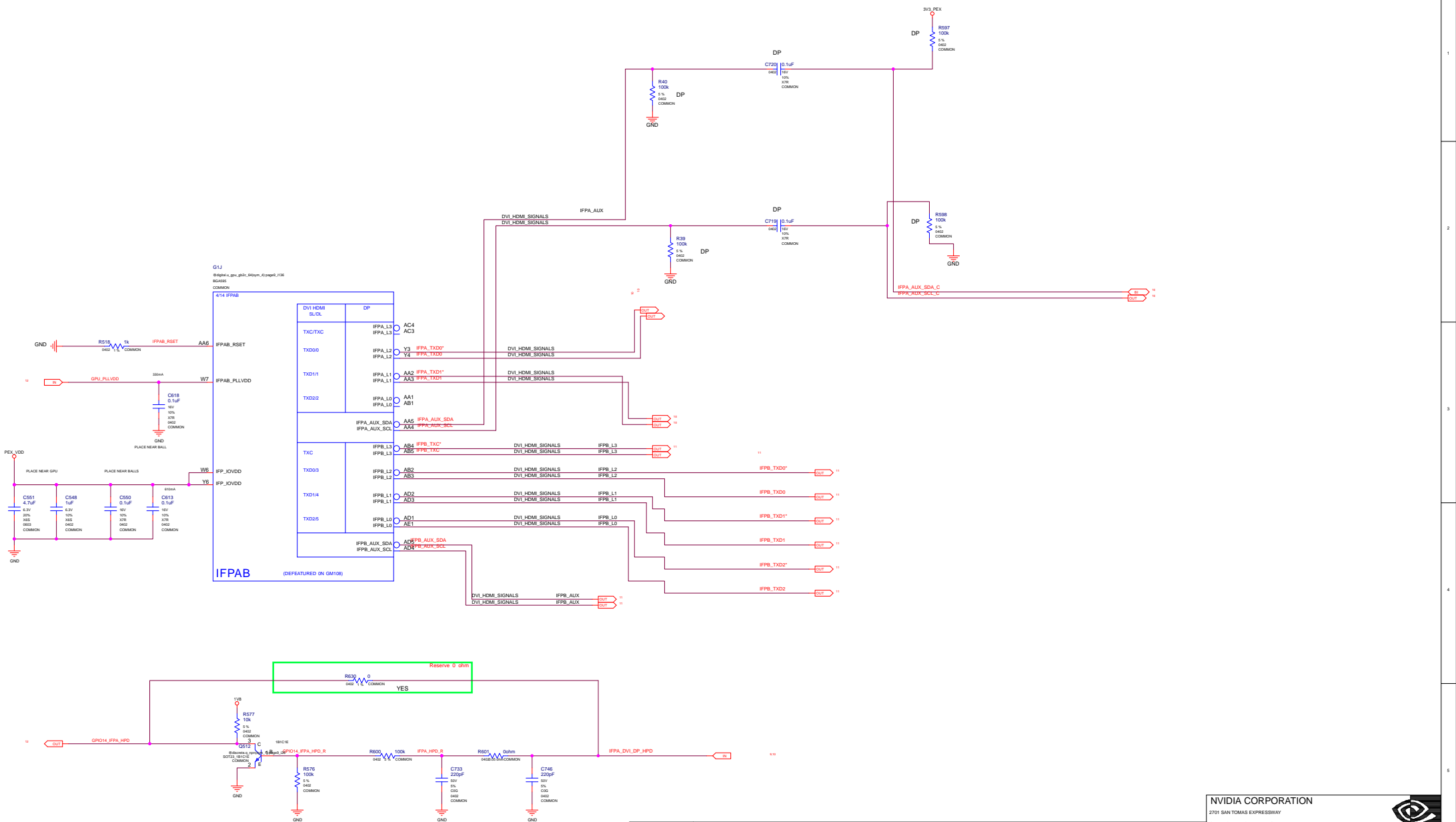
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# FBVDDQ and 1V8 Decoupling





## IFPAB DL DVI-D



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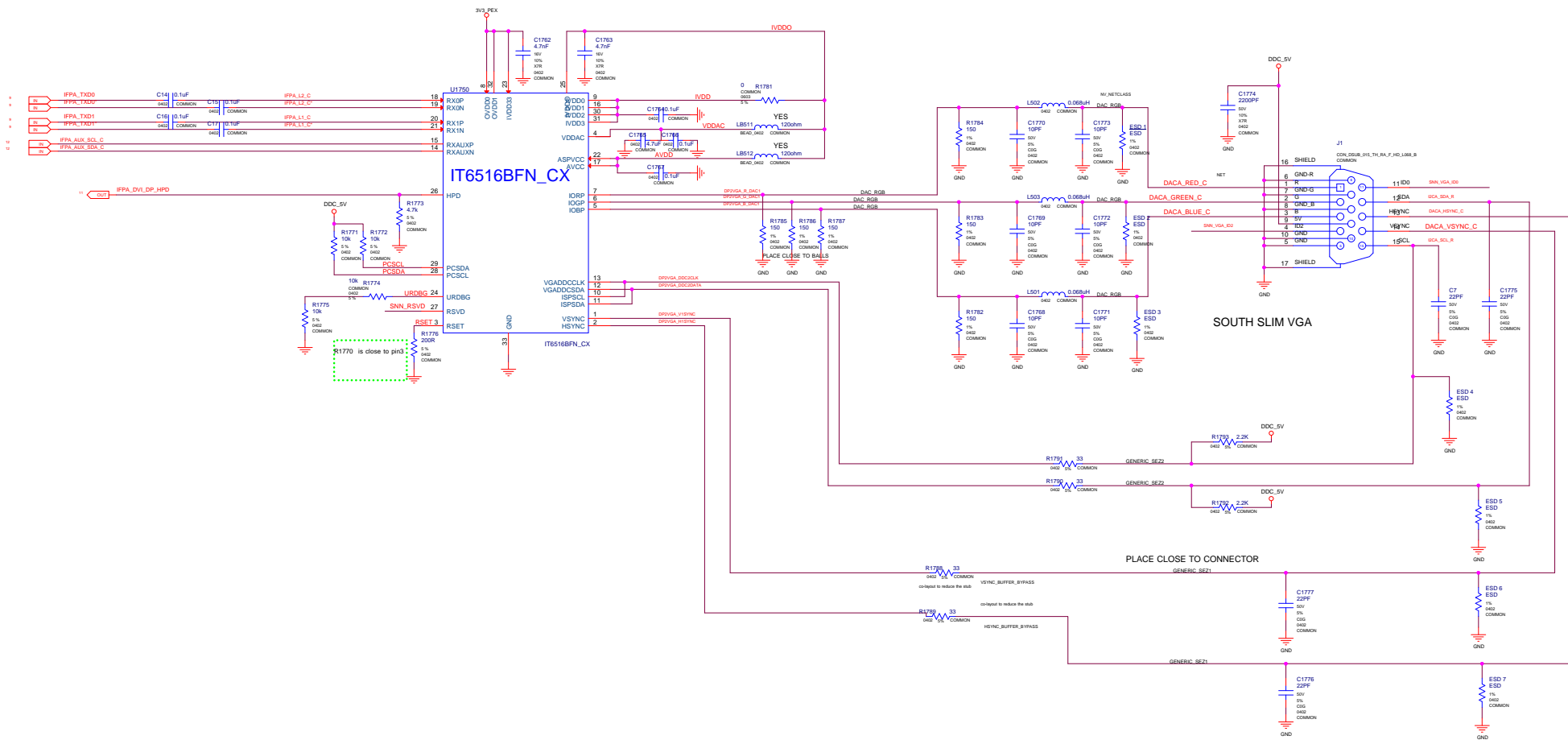


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PAGE DETAIL	IFPAB DL-DVI

## IFPA DP



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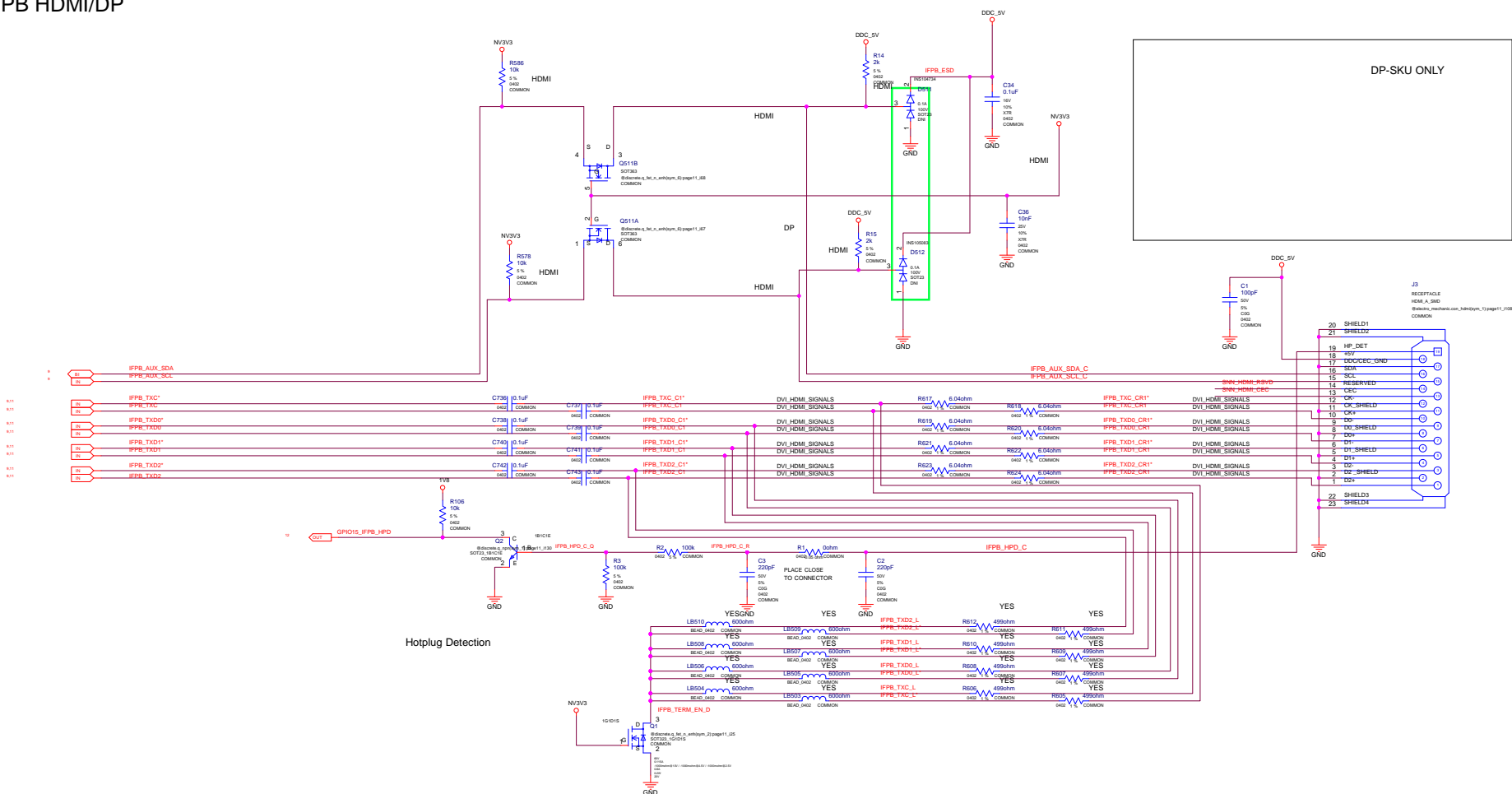
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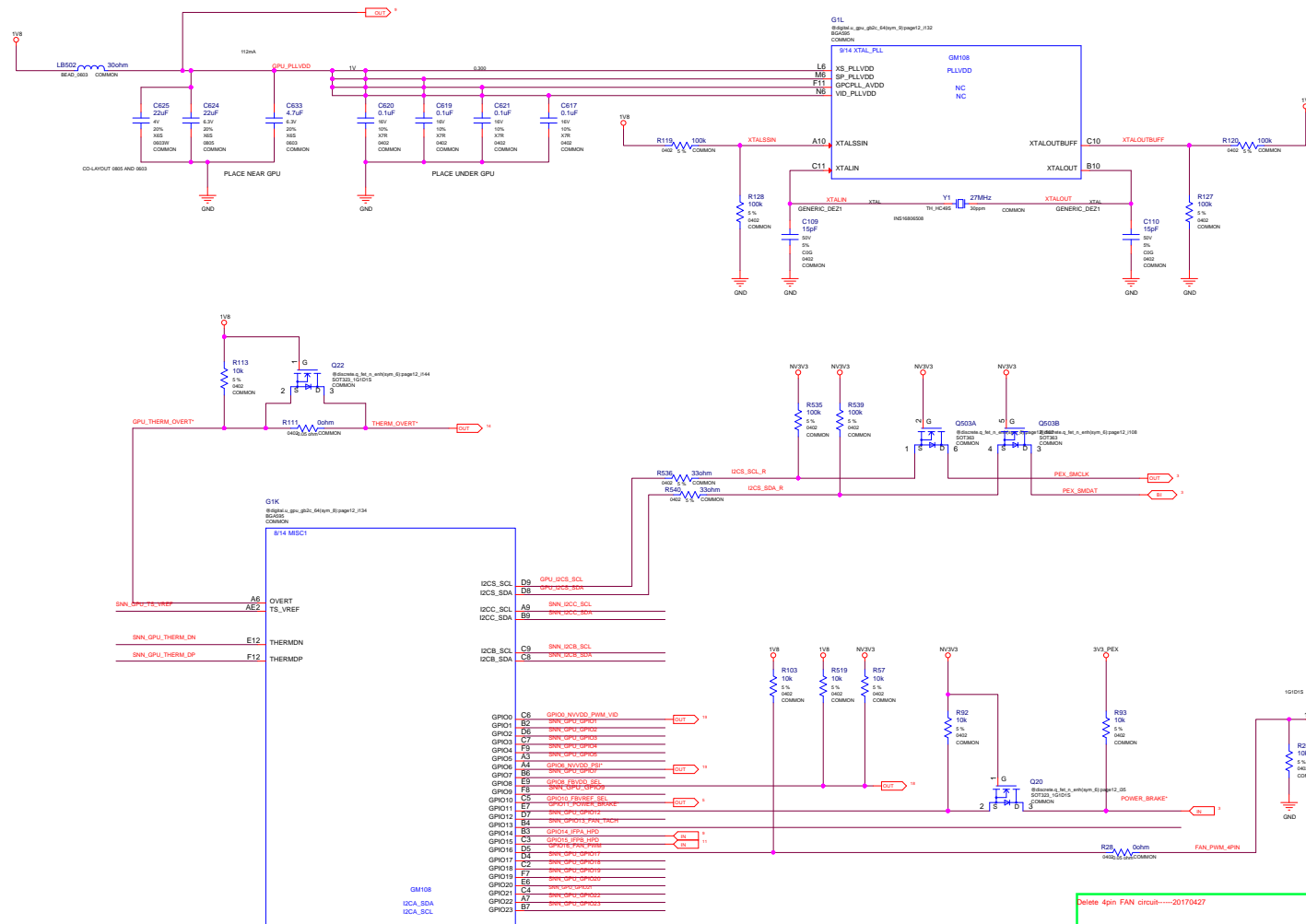
# IFPB HDMI/DP



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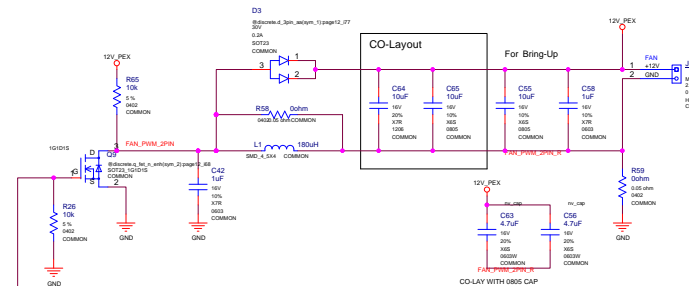
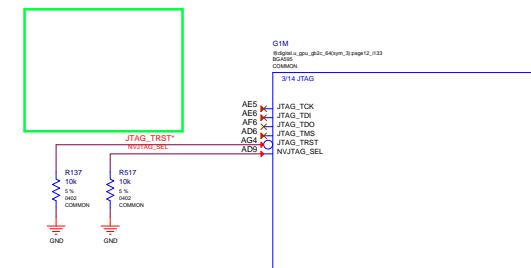
ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	IFPB DP/HDMI

## JTAG,GPIO&XTAL




## Smart Fan

XTALOUTBUFF	GPIO PWM %
PU	66% HIGH
MID	33% HIGH (2-PIN DEFAULT)
PD	100% HIGH



Delete 4pin FAN circuit-----20170423

ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	JTAG,GPIO&XTAL

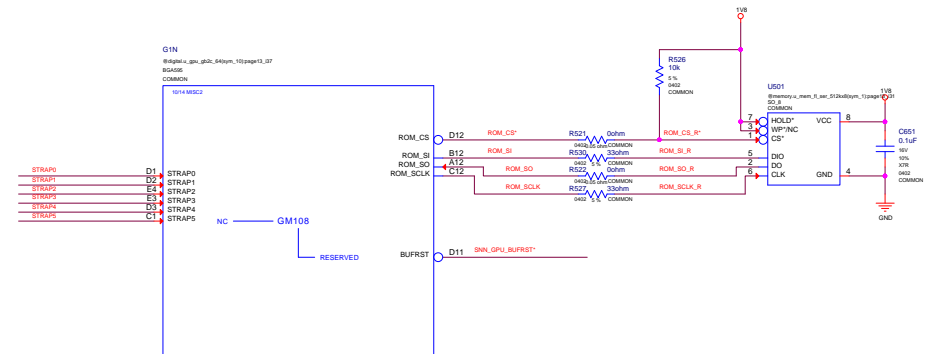
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<b>PCB REV</b>		<b>PG110-A00</b>	<b>PAGE</b>	<b>12 OF</b>
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## ROM & STRAPS

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	SOR0/1 ENABLE
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	DEFAULT
L	L	H	0001	
L	H	L	0010	
L	H	H	0011	
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	

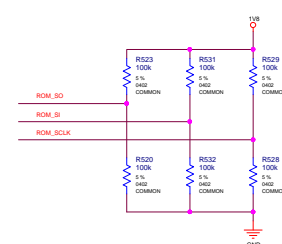
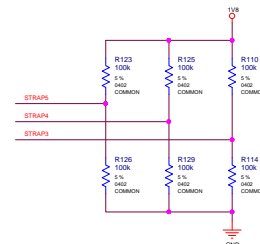
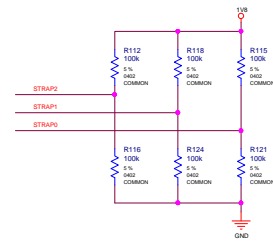
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M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```



ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	ROM & STRAPS

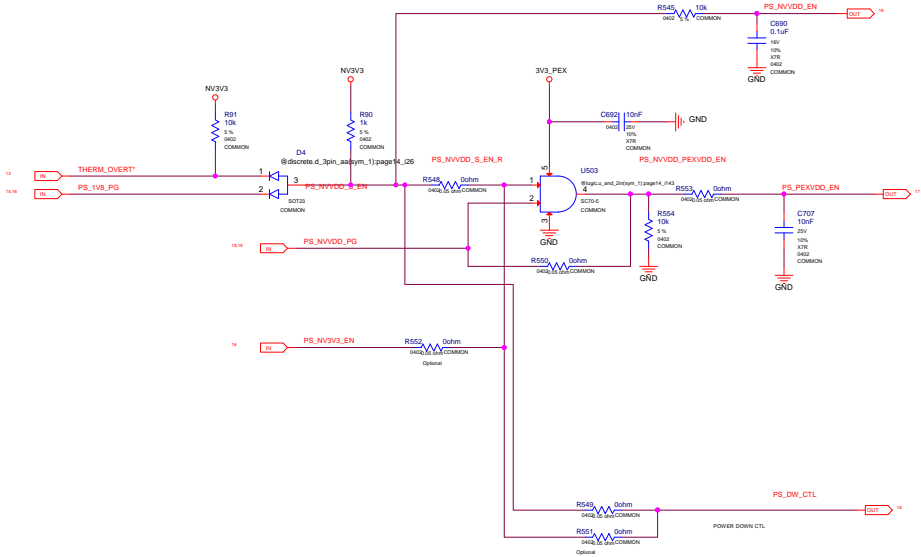
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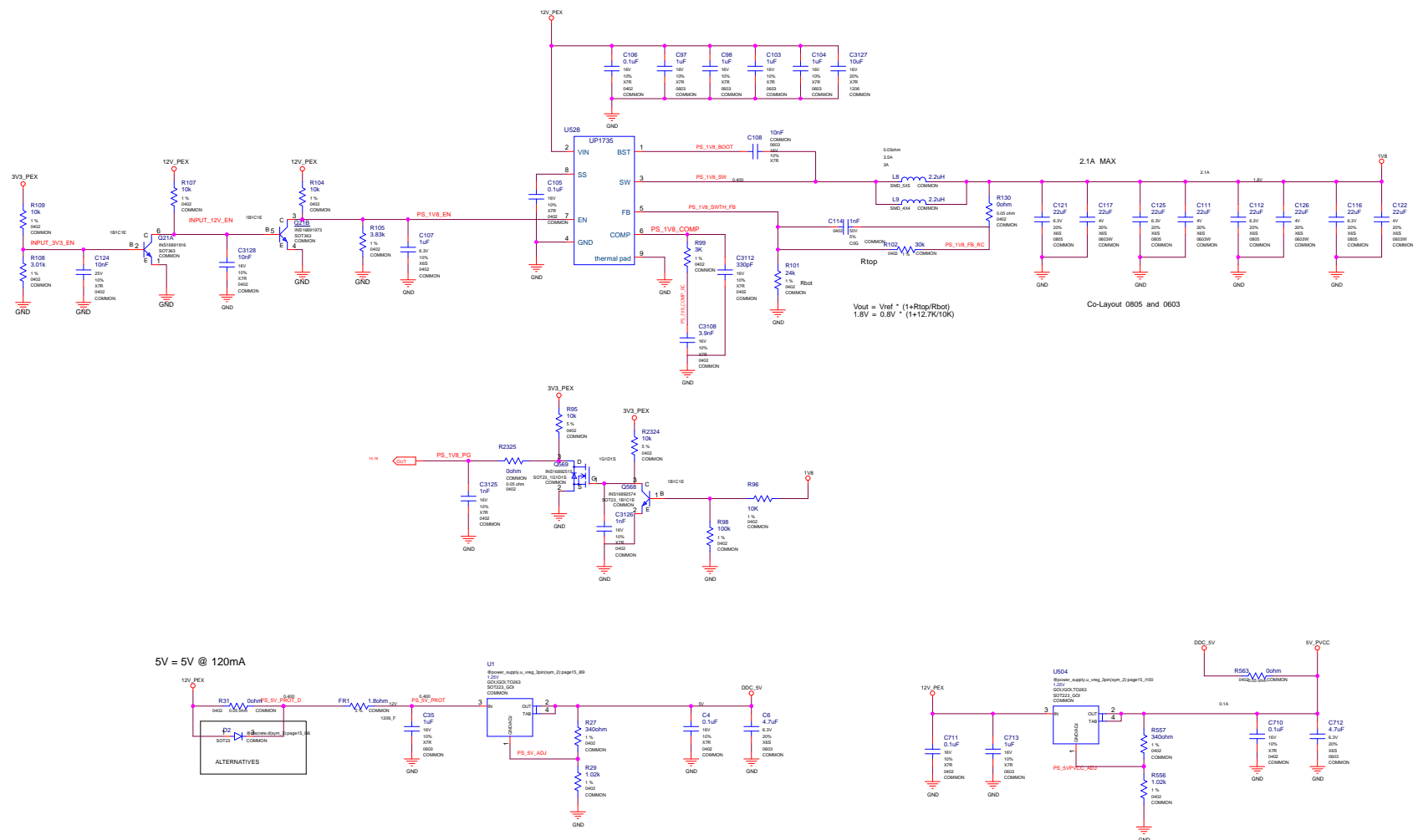
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PAGE DETAIL	POWER:1V8 & 5V

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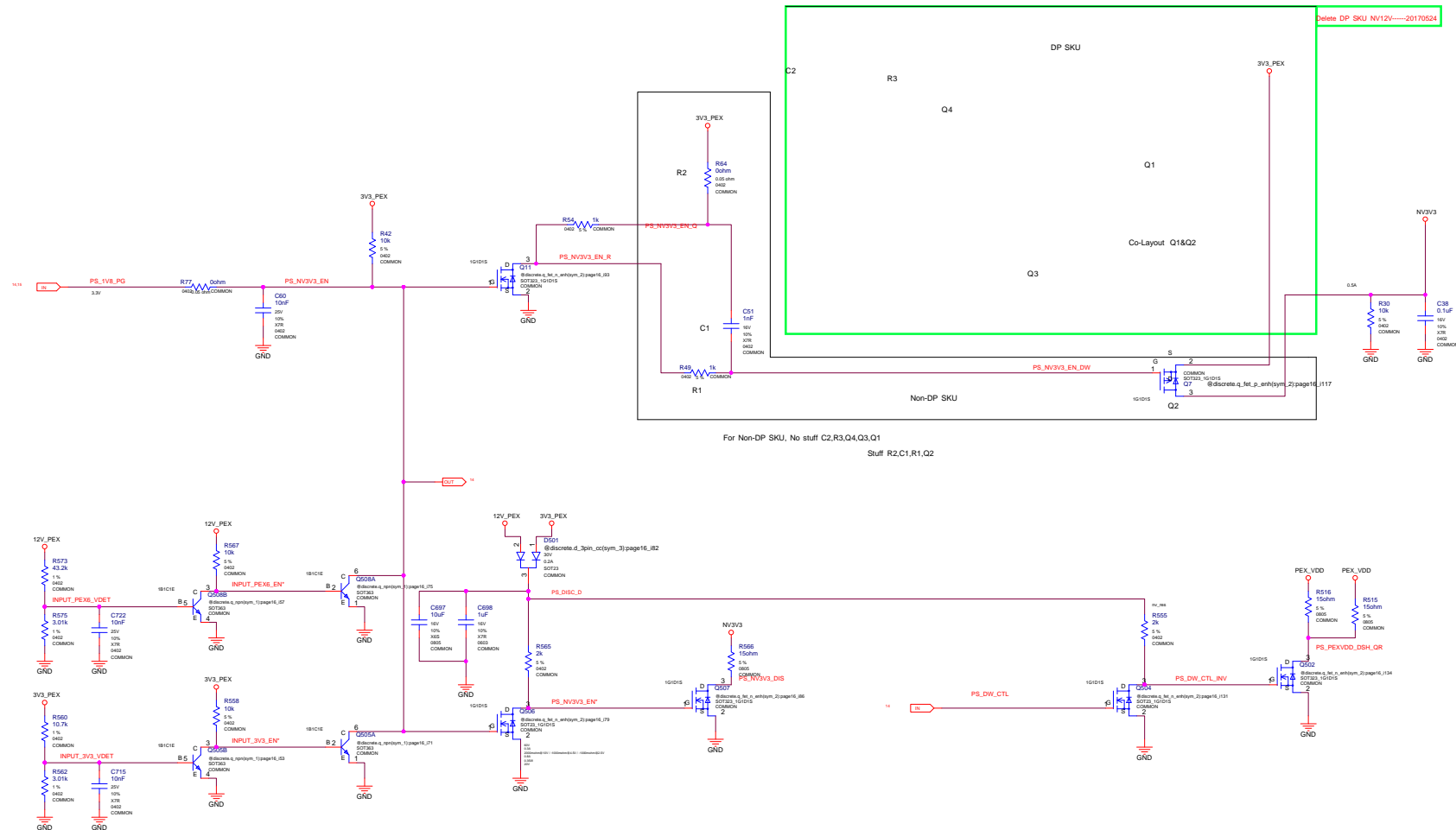
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# POWER: NV3V3, NV12V



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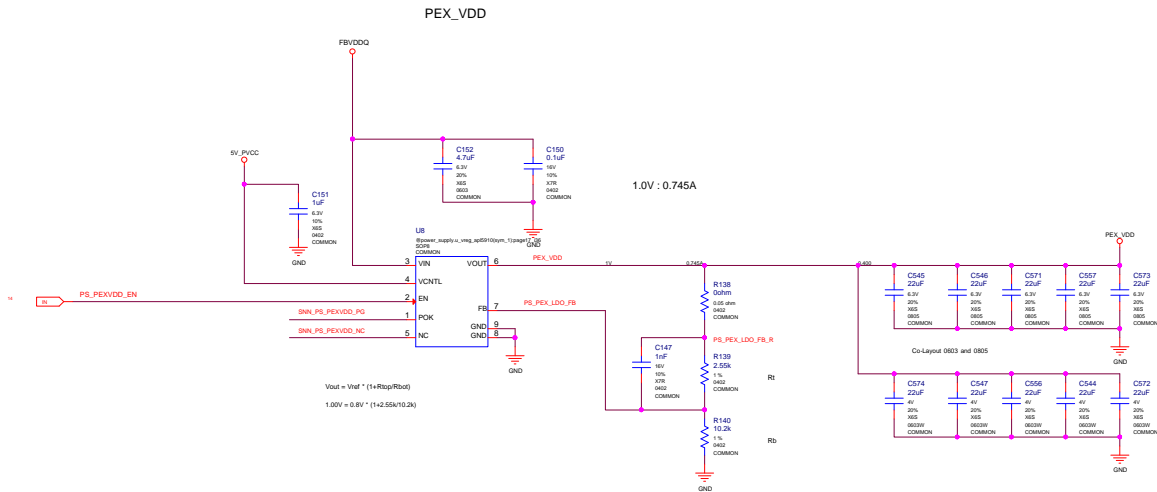
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PCB REV	PG110-A00
BCM REV	A
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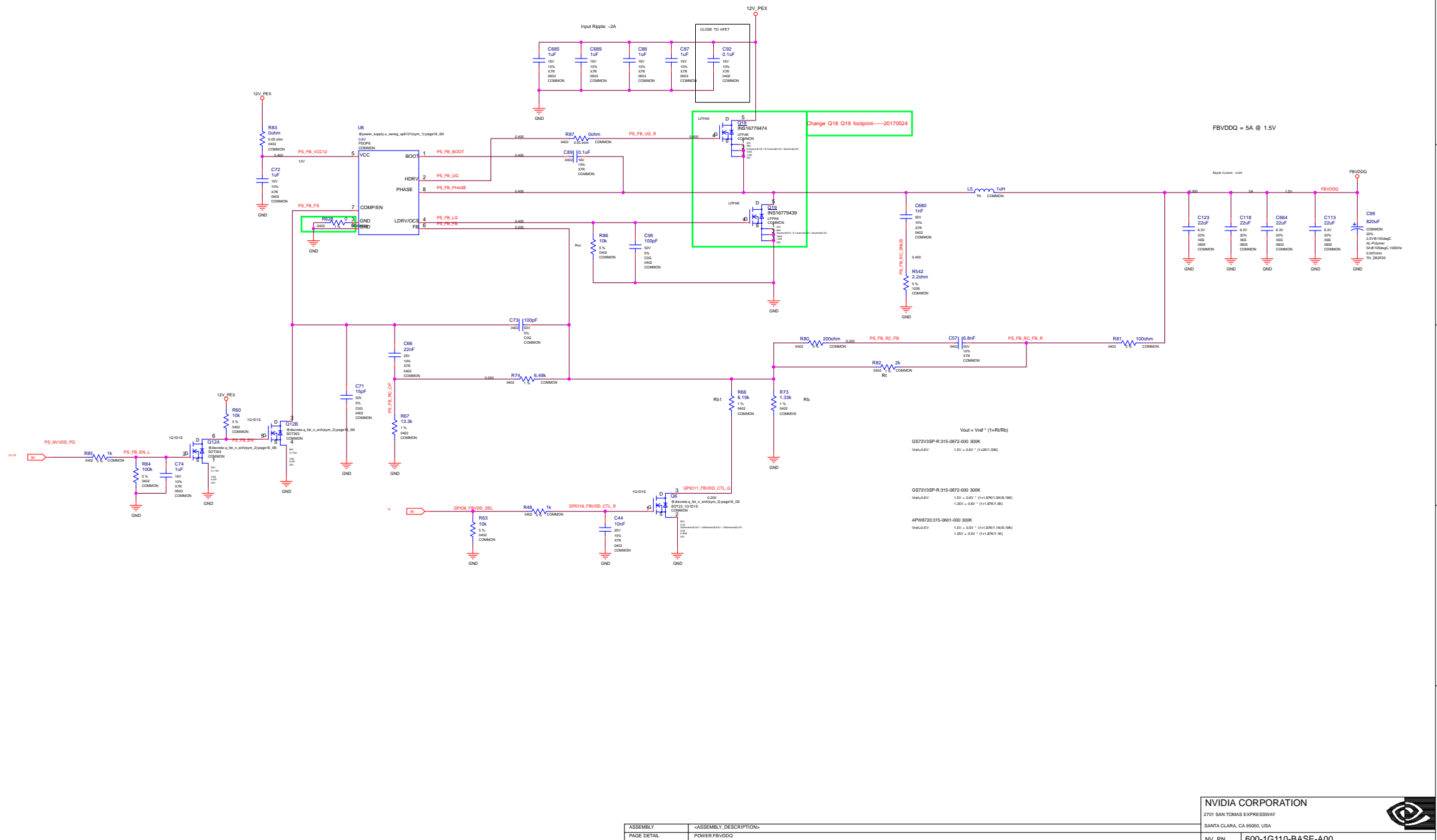


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## POWER:FBVDDQ



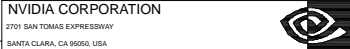
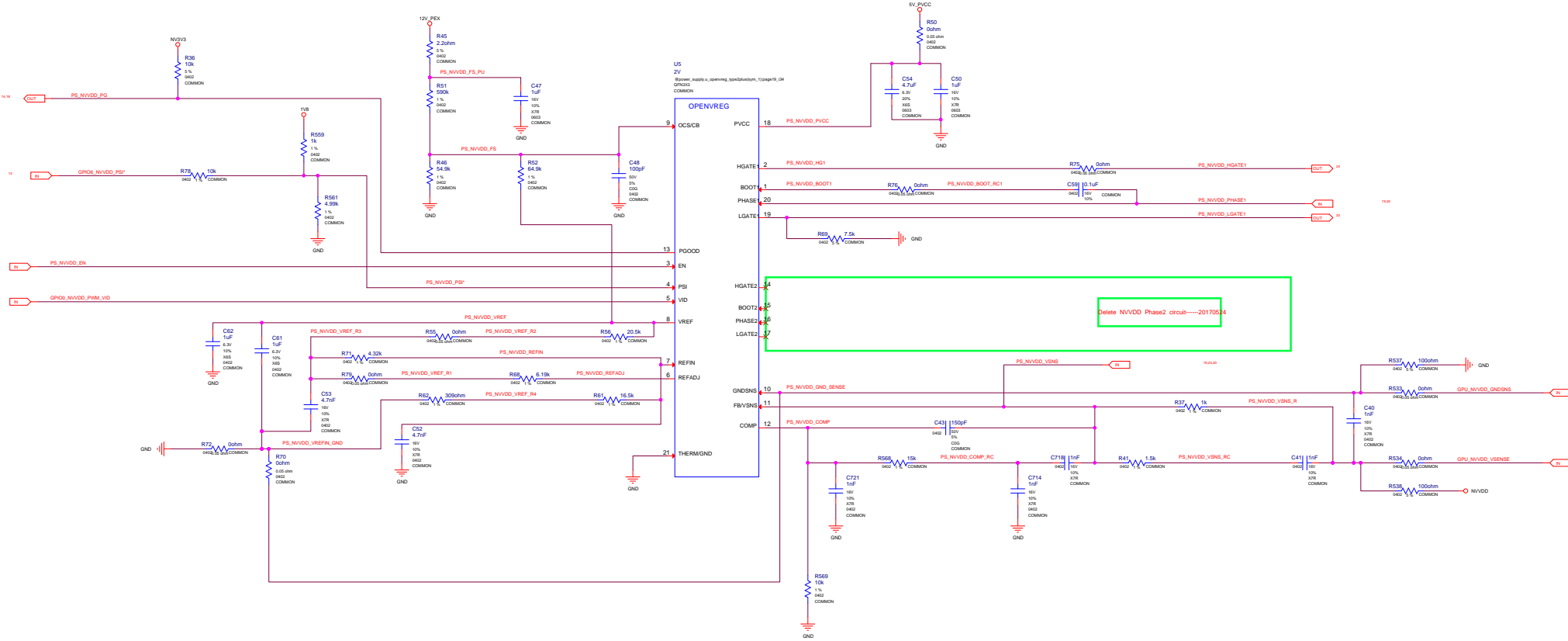
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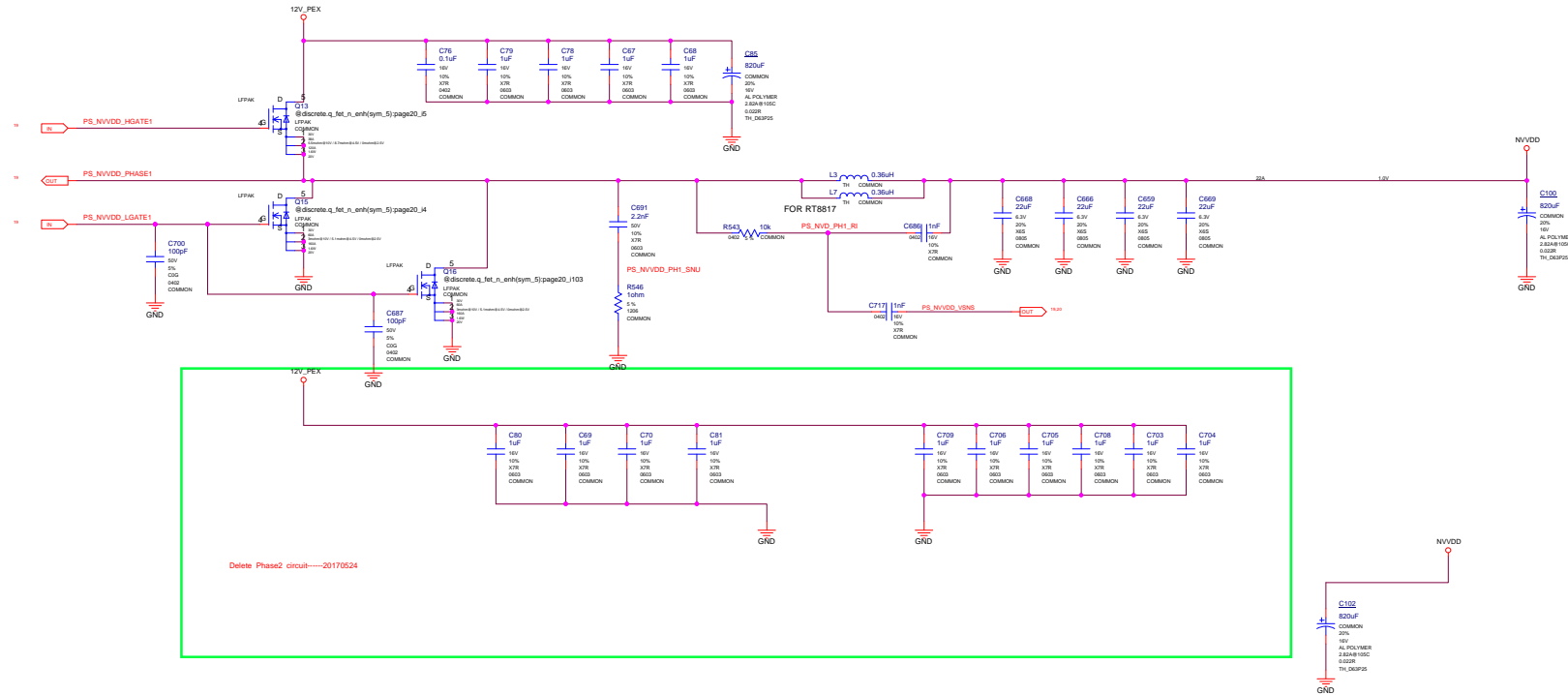
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## Mechanical



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