

NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF, AGP4X
PCI DEVICE ID 0X0=0X200 FOR NV20.

NVVD SET TO: 1.67V FOR -H CHIP
FBVDD SET TO: 3.47V
FBVDDQ SET TO: 2.59V

HISTORY REVISION:

X00: Based on P50-A06
- See change list in 149- file.
- Set FBVDDQ=2.59V


P50-A07-X01:
- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

P50-A08:
X04: - Delay PLL_VDD to come up after NVVD.
X05: - Added 1UF accross R257.
X06: - Removed X04-5 above, added a switcher generated PLL delay option.
- SSEN cap for 2nd SW changed to 1UF.
- A05 Si, NVVD=1.52V

P50-A09:
X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.
X03: - Added option to pull up power good to 12V

ECO1235: - Changed R841 PU to 10K (from 4.7K)

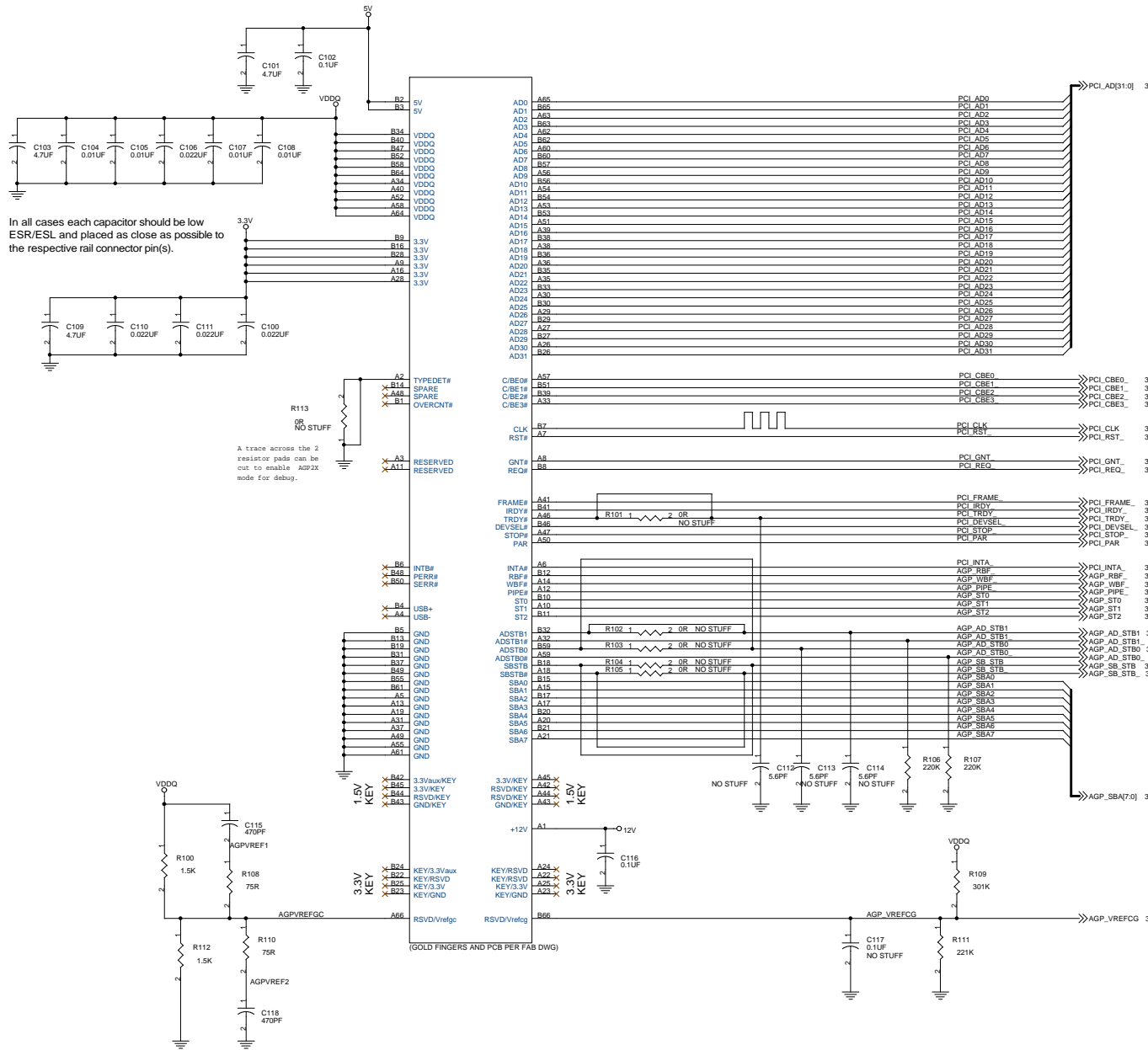
ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction.
Replaced C303,306,309 with 75ohm and no stuffed R208-210.



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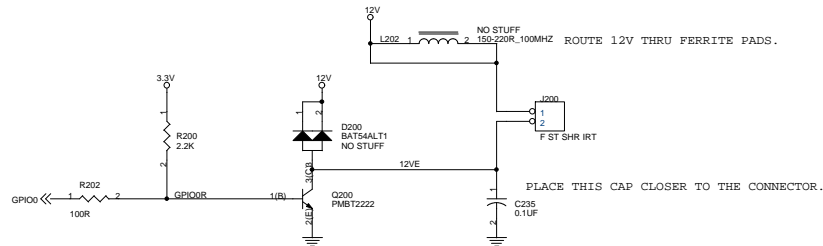
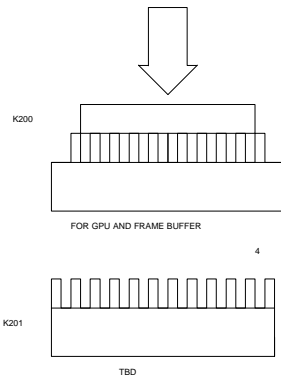
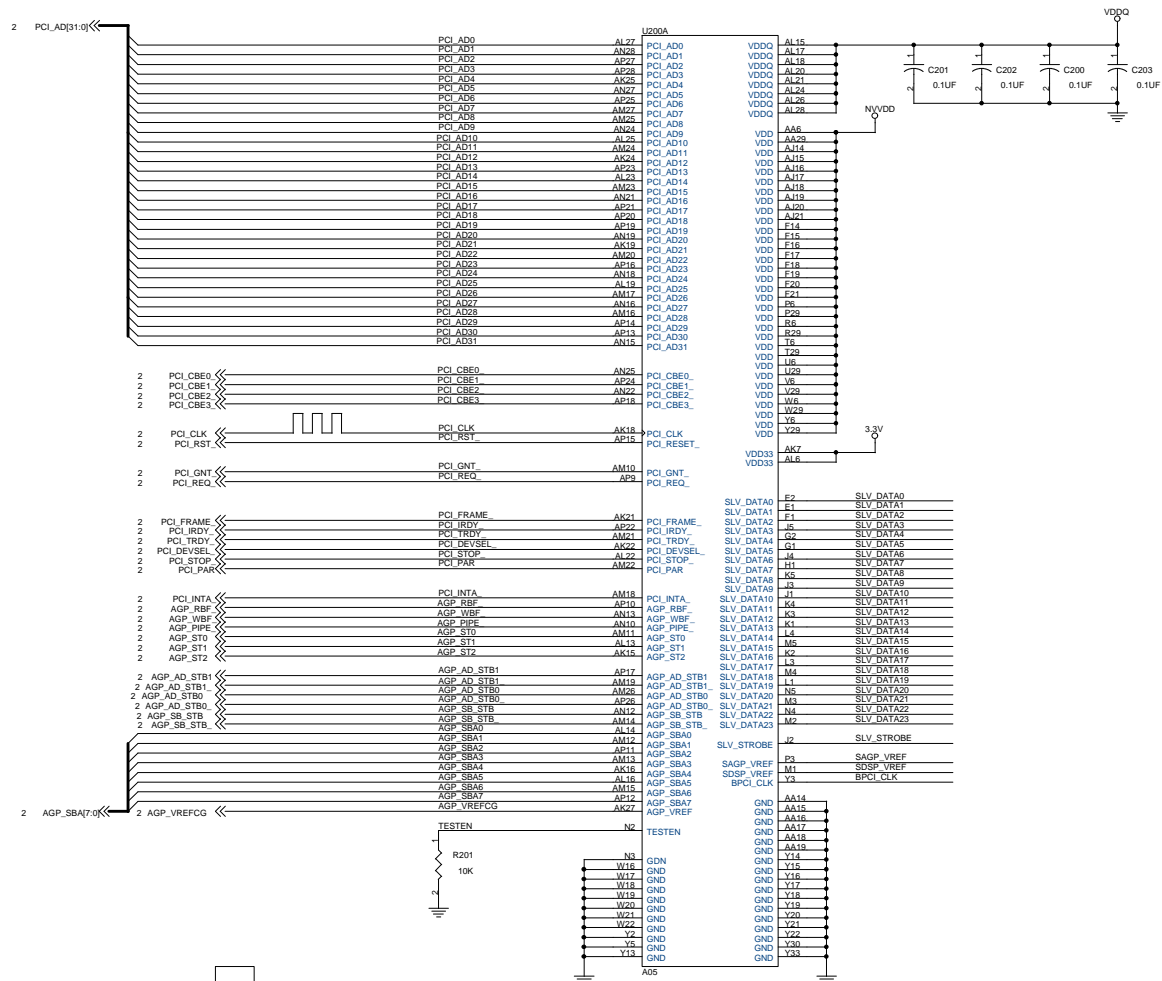
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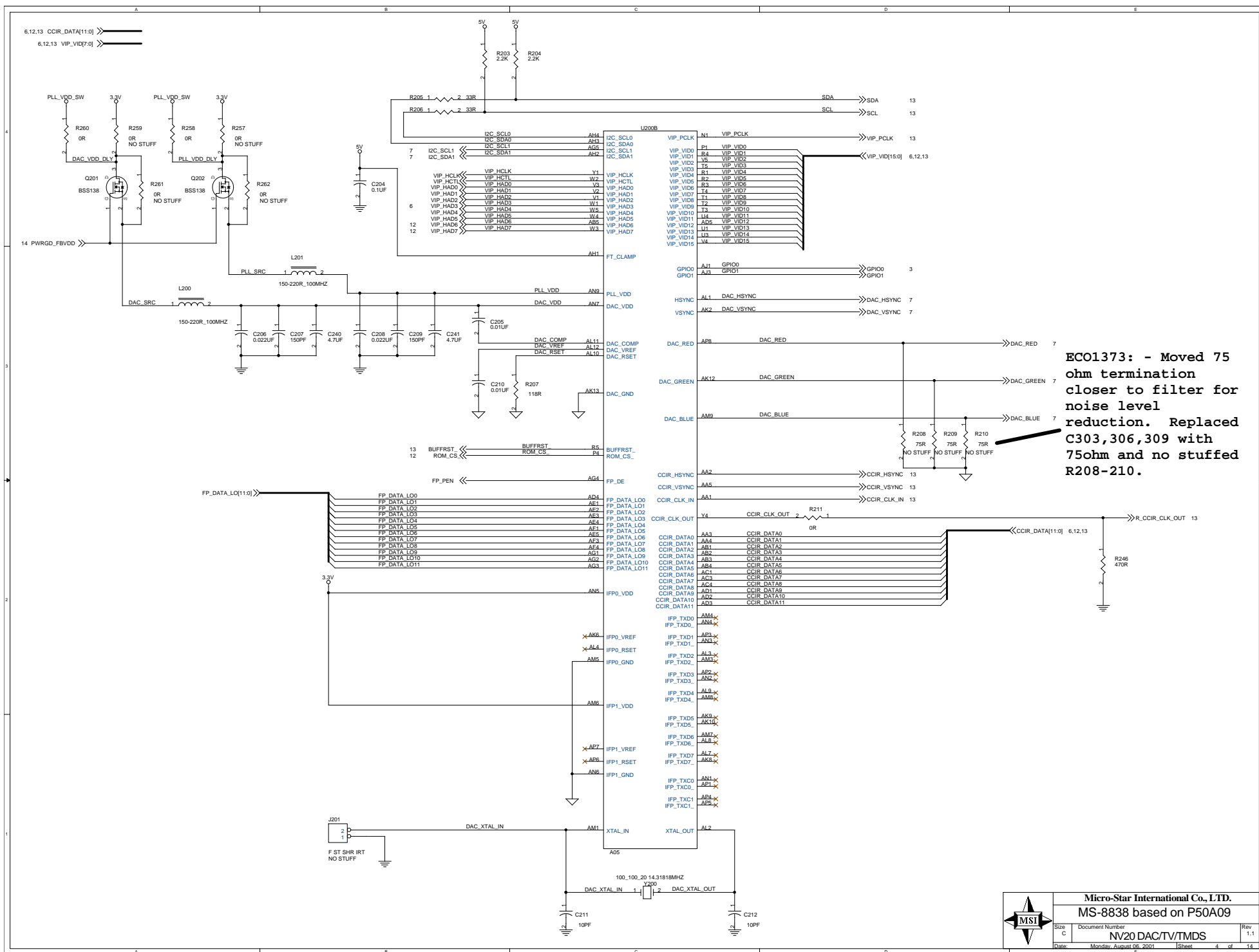
Size	Document Number	Rev
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Date	Monday, August 06, 2001	
Sheet	1 of 14	

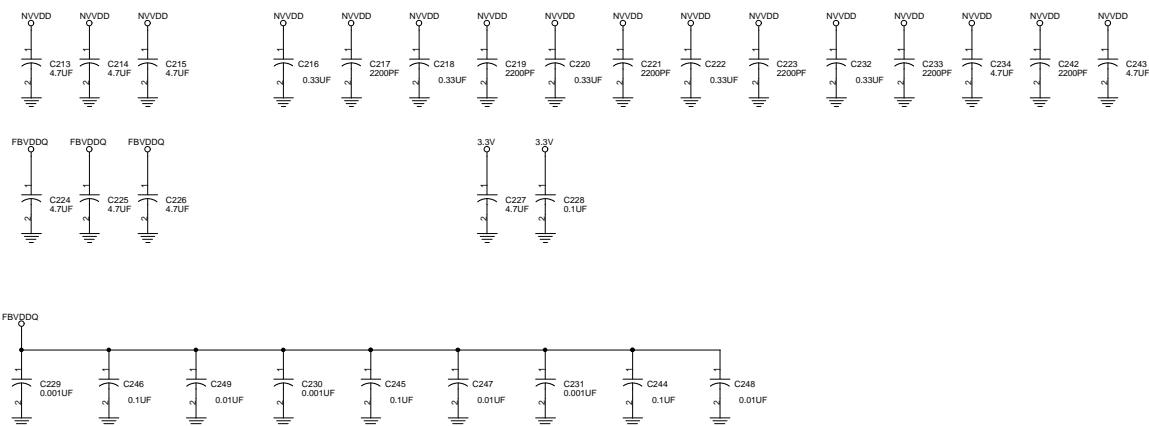


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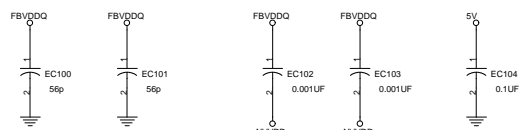
Size	Document Number	Rev
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Date	Monday, August 06, 2001	Sheet 2 of 14





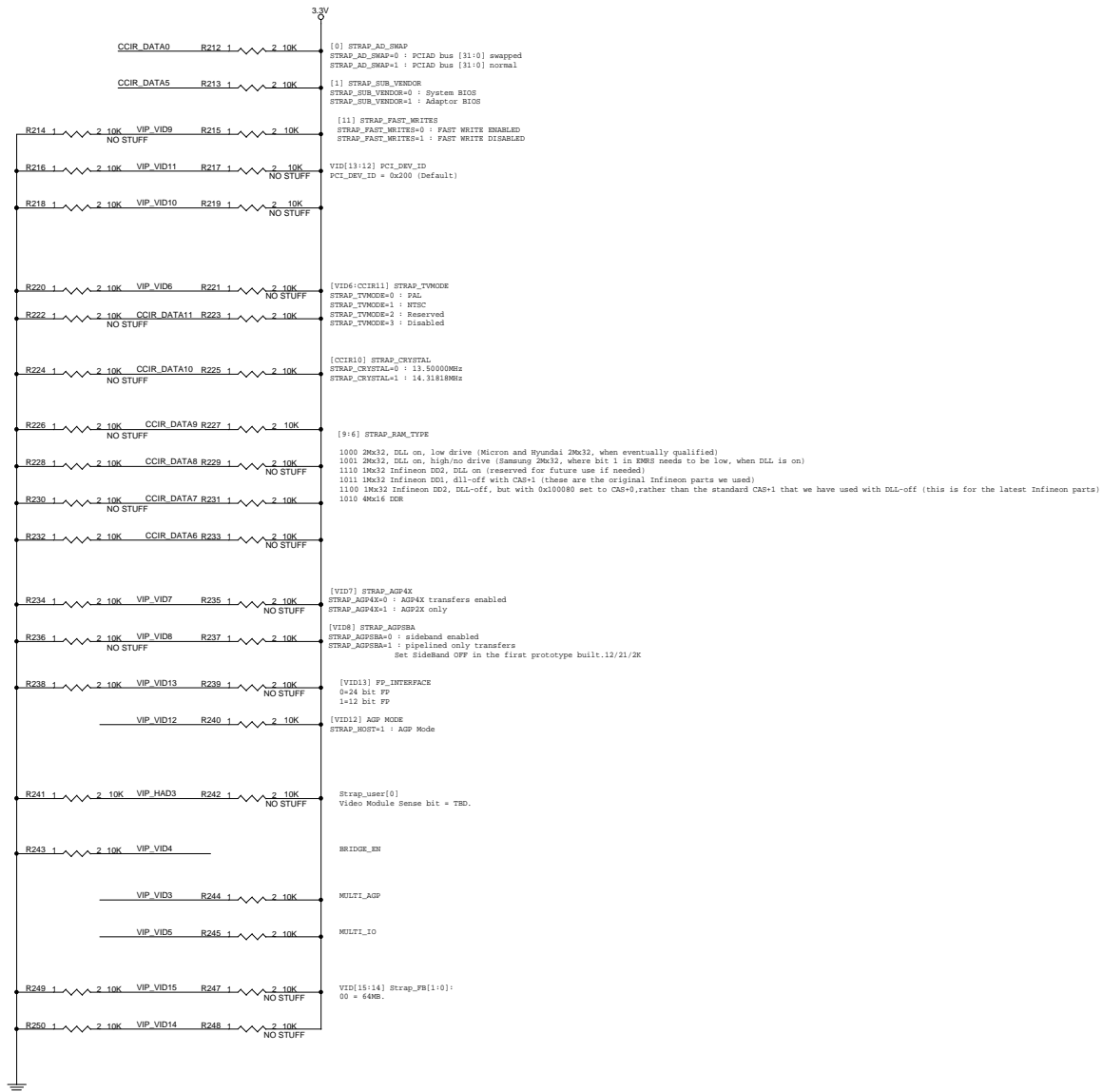


For EMI Solution



4,12,13 CCIR_DATA[11:0] >>
4,12,13 VIP_VID[15:0] >>
4 FP_DATA_LQ[11:0] >>

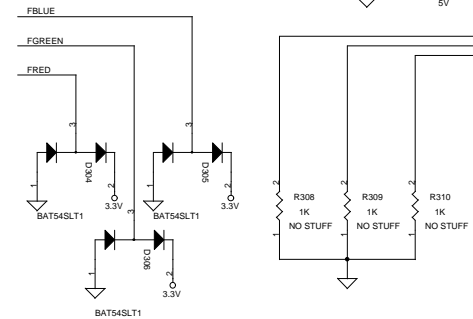
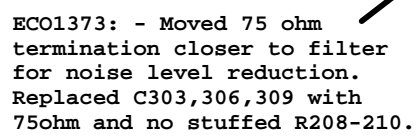
4 VIP_HAD[0] >>
4 VIP_HAD[1] >>
4 VIP_HAD[2] >>
4 VIP_HAD[3] >>
4 VIP_HAD[4] >>
4 VIP_HAD[5] >>
4,12 VIP_HAD[6] >>
4,12 VIP_HAD[7] >>



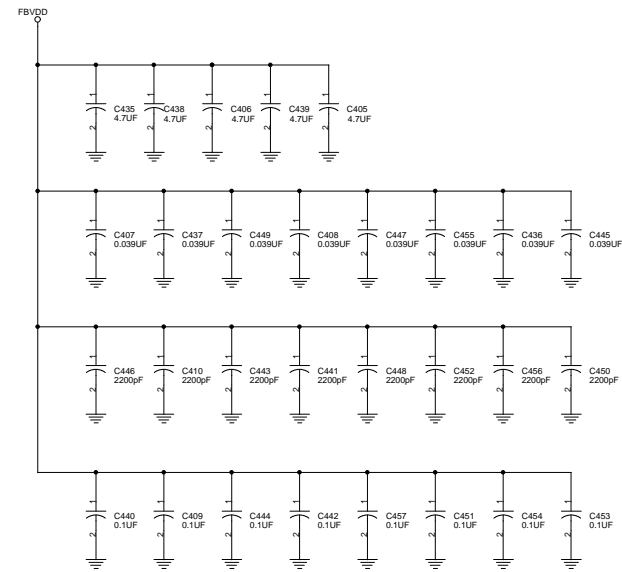
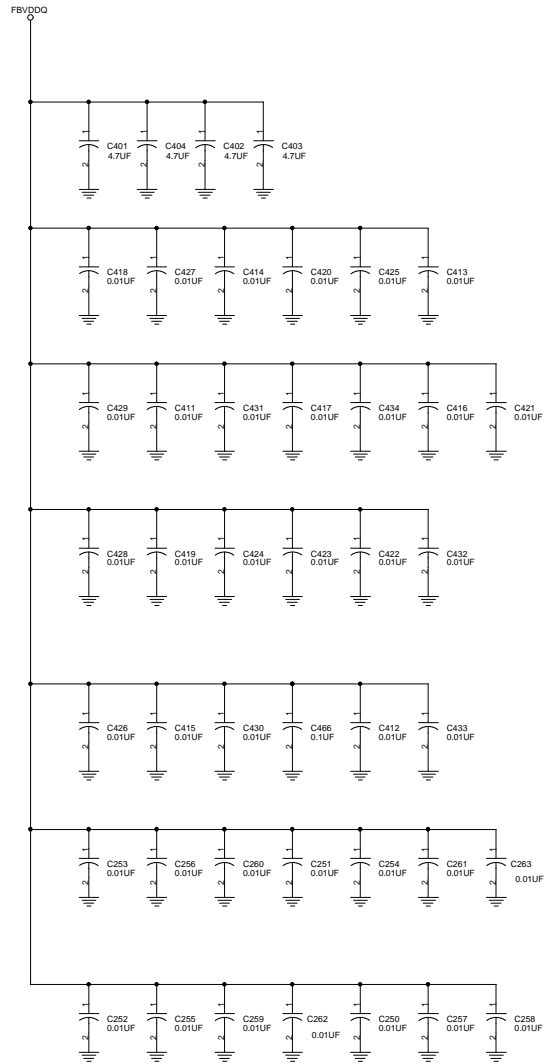
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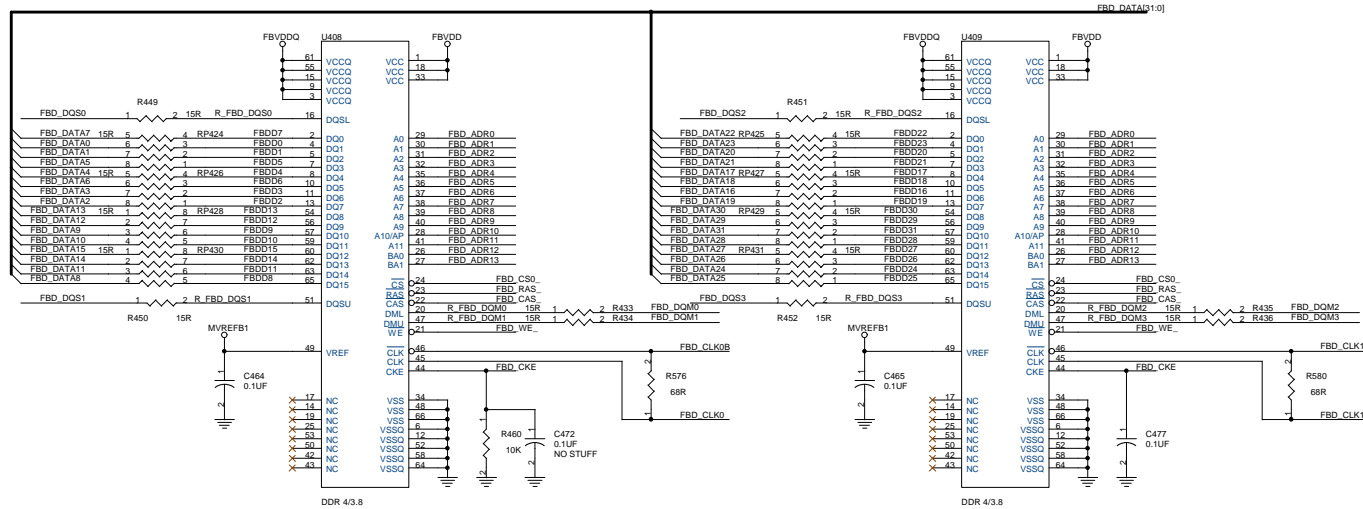
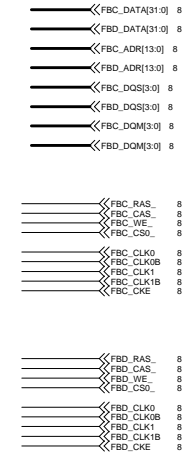
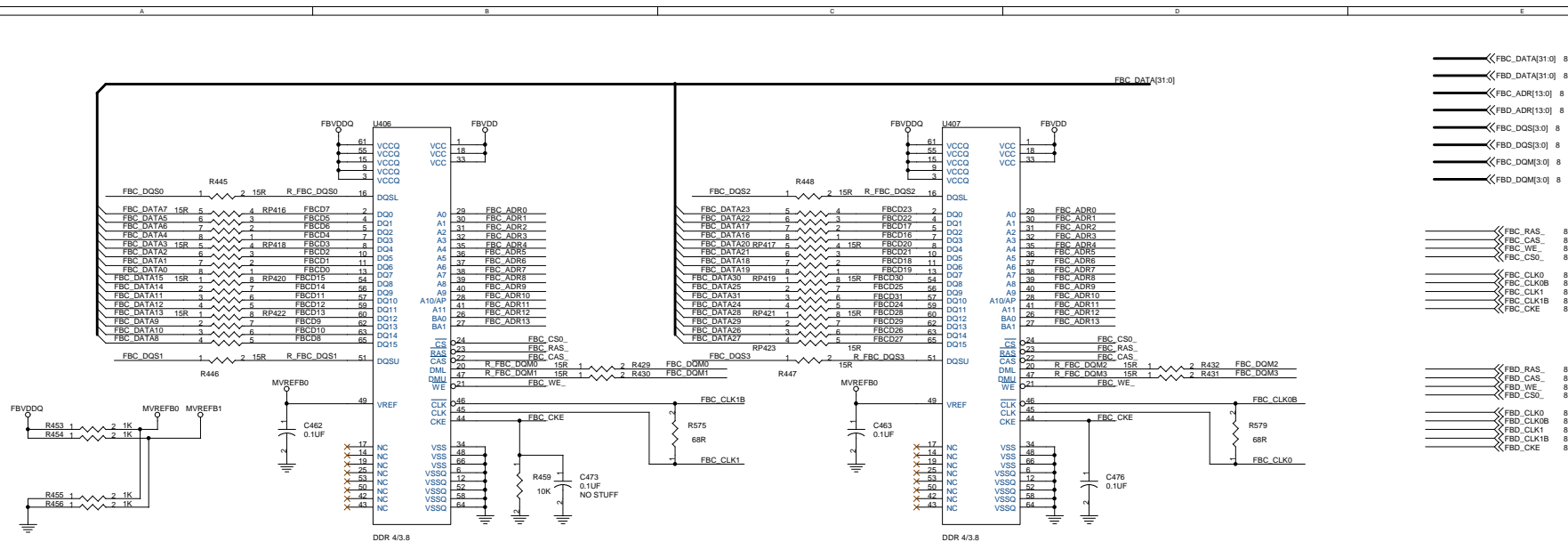
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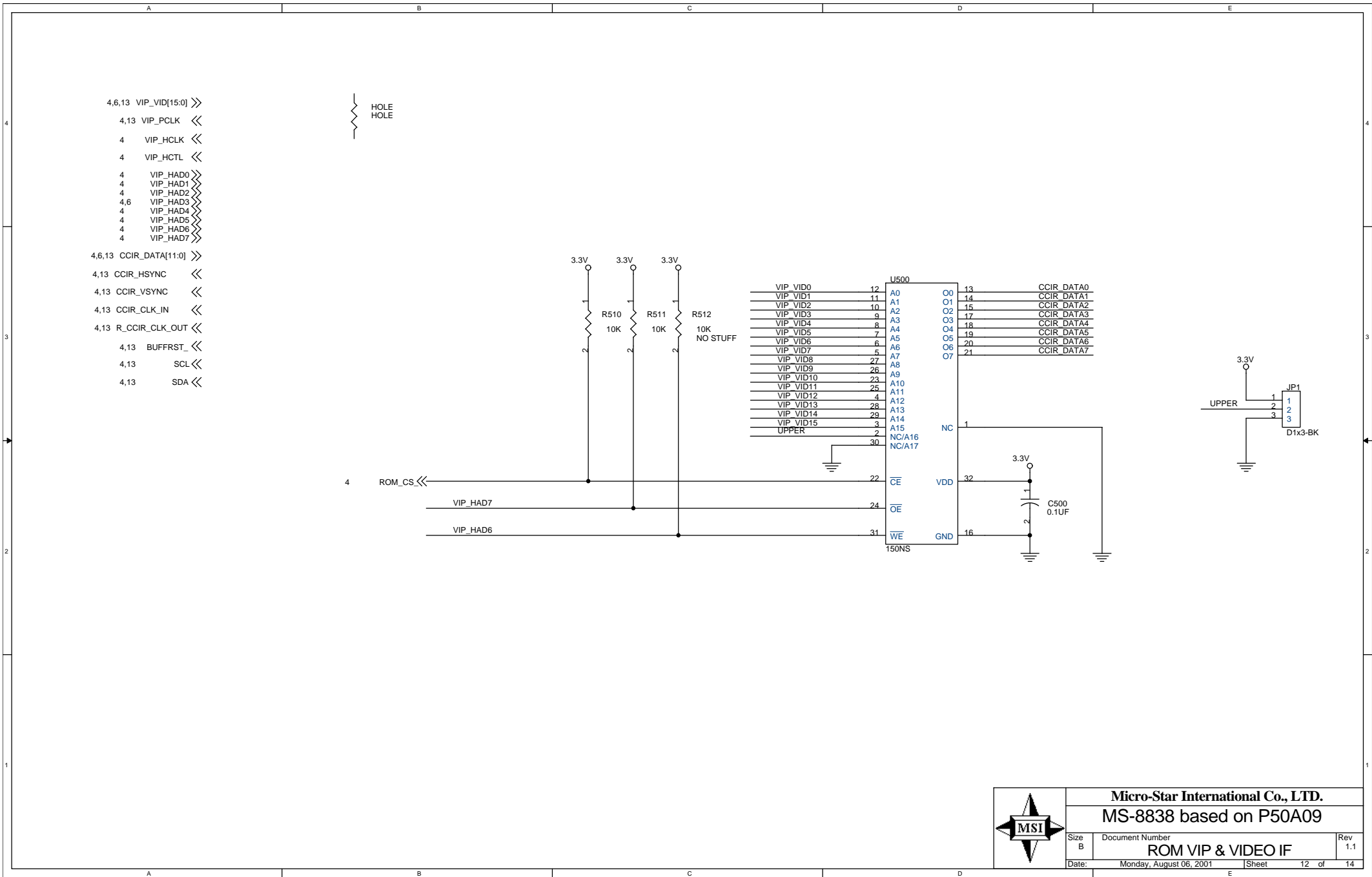
Size	Document Number	Rev
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Date	Monday, August 06, 2001	Sheet 6 of 14







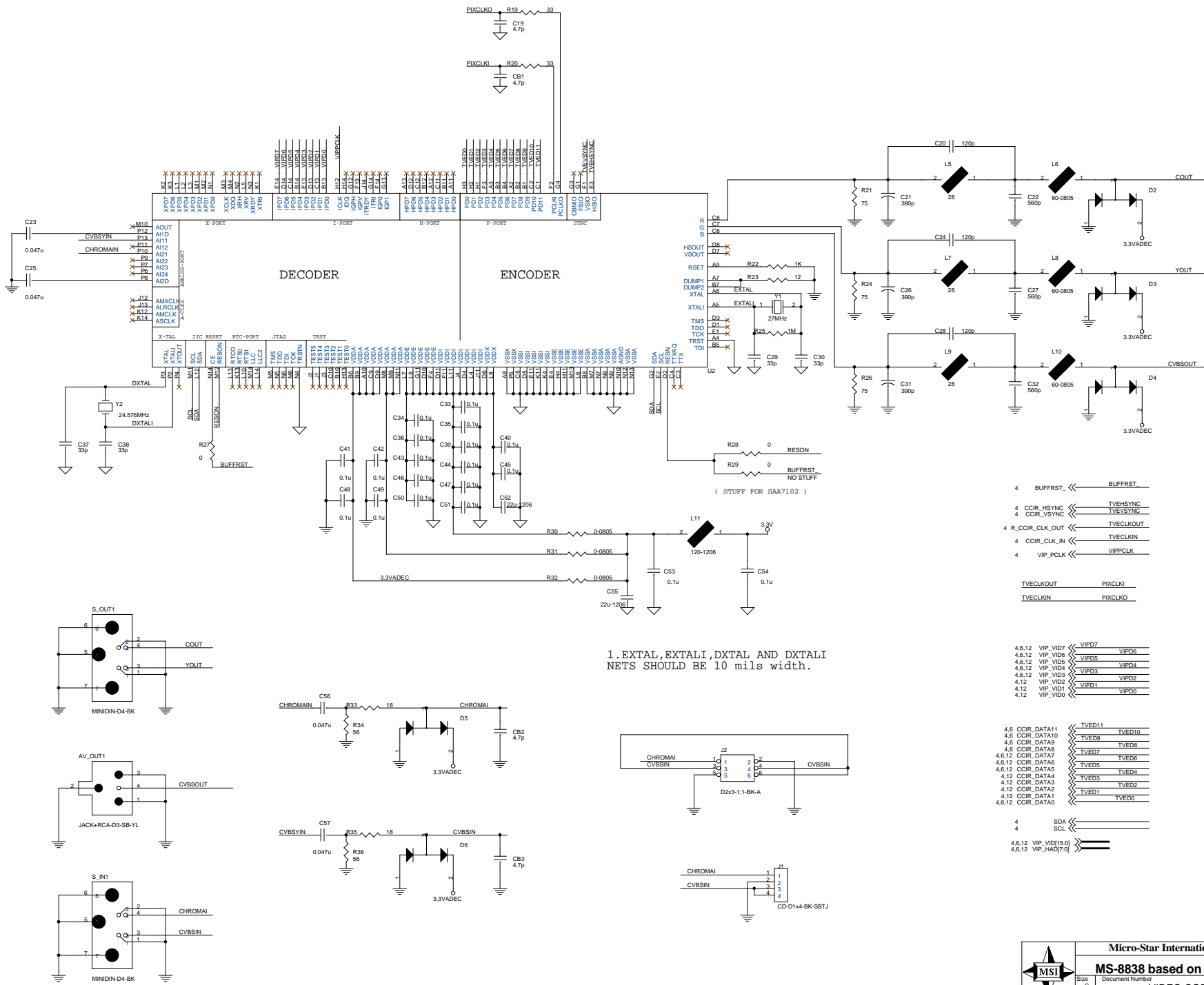




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MS-8838 based on P50A09

Size B	Document Number ROM VIP & VIDEO IF	Rev 1.1
Date: Monday, August 06, 2001	Sheet 12 of 14	



- 4.12 VIP_VID7 << VIPD7
4.6.12 VIP_VID6 << VIPD6
4.6.12 VIP_VID5 << VIPD5
4.6.12 VIP_VID4 << VIPD4
4.6.12 VIP_VID3 << VIPD3
4.12 VIP_VID2 << VIPD2
4.12 VIP_VID1 << VIPD1
4.12 VIP_VID0 << VIPD0
- 4.6 CCIR_DATA11 << TVED11
4.6 CCIR_DATA10 << TVED10
4.6 CCIR_DATA9 << TVED9
4.6 CCIR_DATA8 << TVED8
4.6.12 CCIR_DATA7 << TVED7
4.6.12 CCIR_DATA6 << TVED6
4.6.12 CCIR_DATA5 << TVED5
4.12 CCIR_DATA4 << TVED4
4.12 CCIR_DATA3 << TVED3
4.12 CCIR_DATA2 << TVED2
4.12 CCIR_DATA1 << TVED1
4.6.12 CCIR_DATA0 << TVED0
- 4 SDA << SDA
4 SCL << SCL
- 4.6.12 VIP_VID15[0] << VIPD15[0]
4.6.12 VIP_HAD[7:0] << VIPD7[0]

