

P1065-B00


GF116 MXM V3.0 Type B, LVDS, Quad DP, DVI, VGA, SLI
GB1-192, 3072MB/1536MB GDDR5 x16

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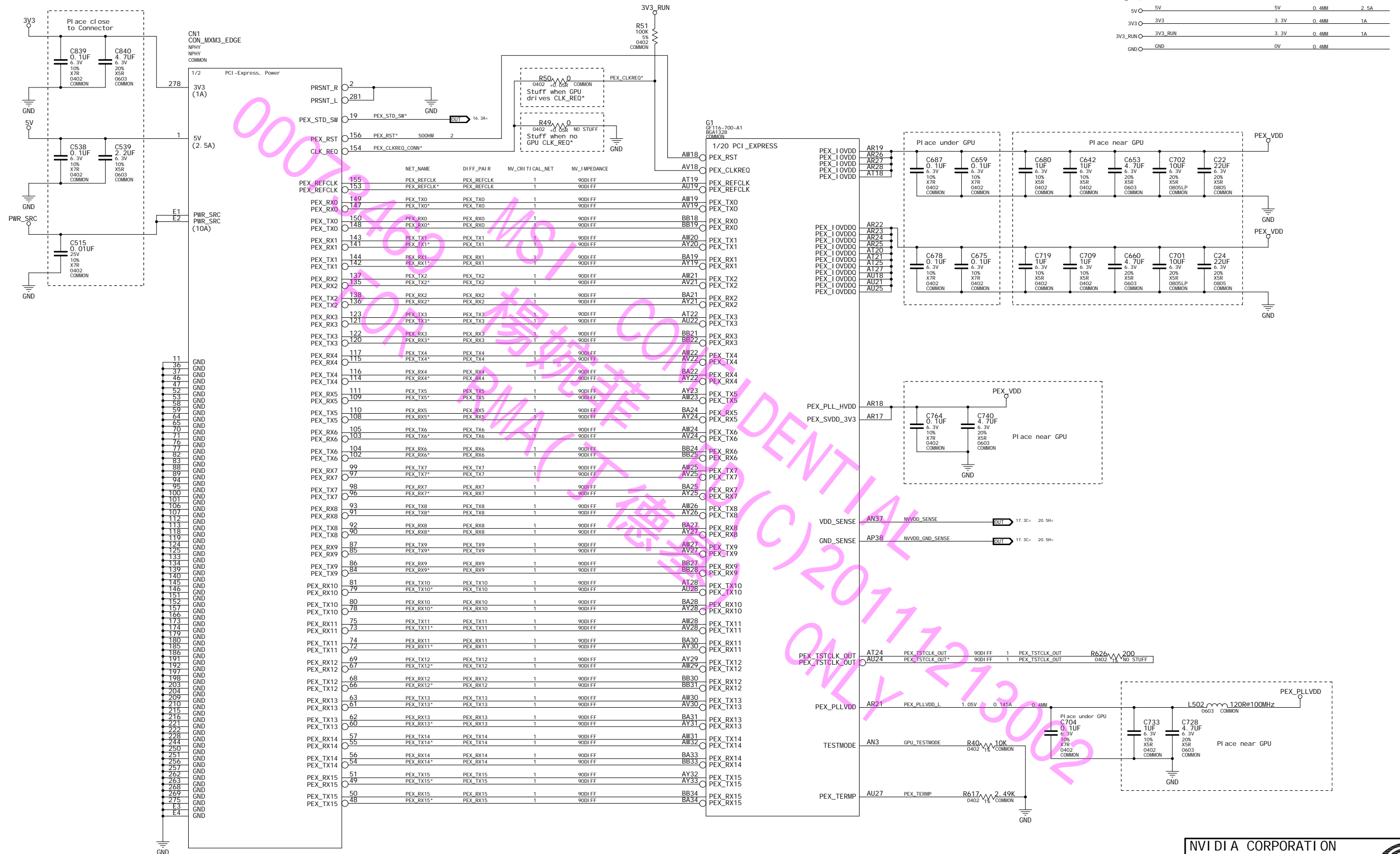
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2. PCI Express Interface

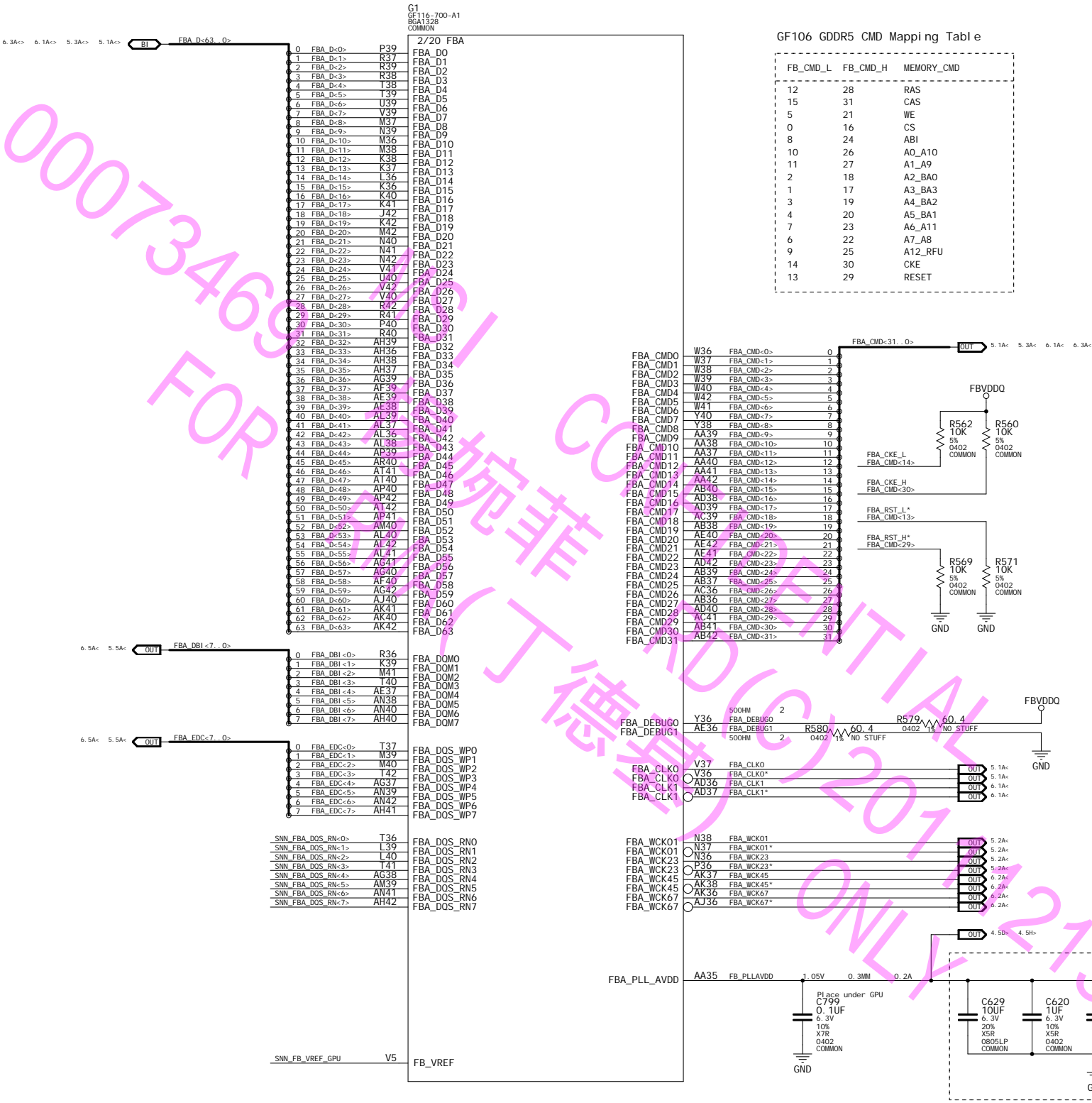


ASSEMBLY	P1065-B00 SKU13
PAGE DETAIL	PCI Express Interface

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3. Frame Buffer Interface A



GF106 GDDR5 CMD Mapping Table

FB_CMD_L	FB_CMD_H	MEMORY_CMD
12	28	RAS
15	31	CAS
5	21	WE
0	16	CS
8	24	AB1
10	26	A0_A10
11	27	A1_A9
2	18	A2_BA0
1	17	A3_BA3
3	19	A4_BA2
4	20	A5_BA1
7	23	A6_A11
6	22	A7_AB
9	25	A12_RFU
14	30	CKE
13	29	RESET

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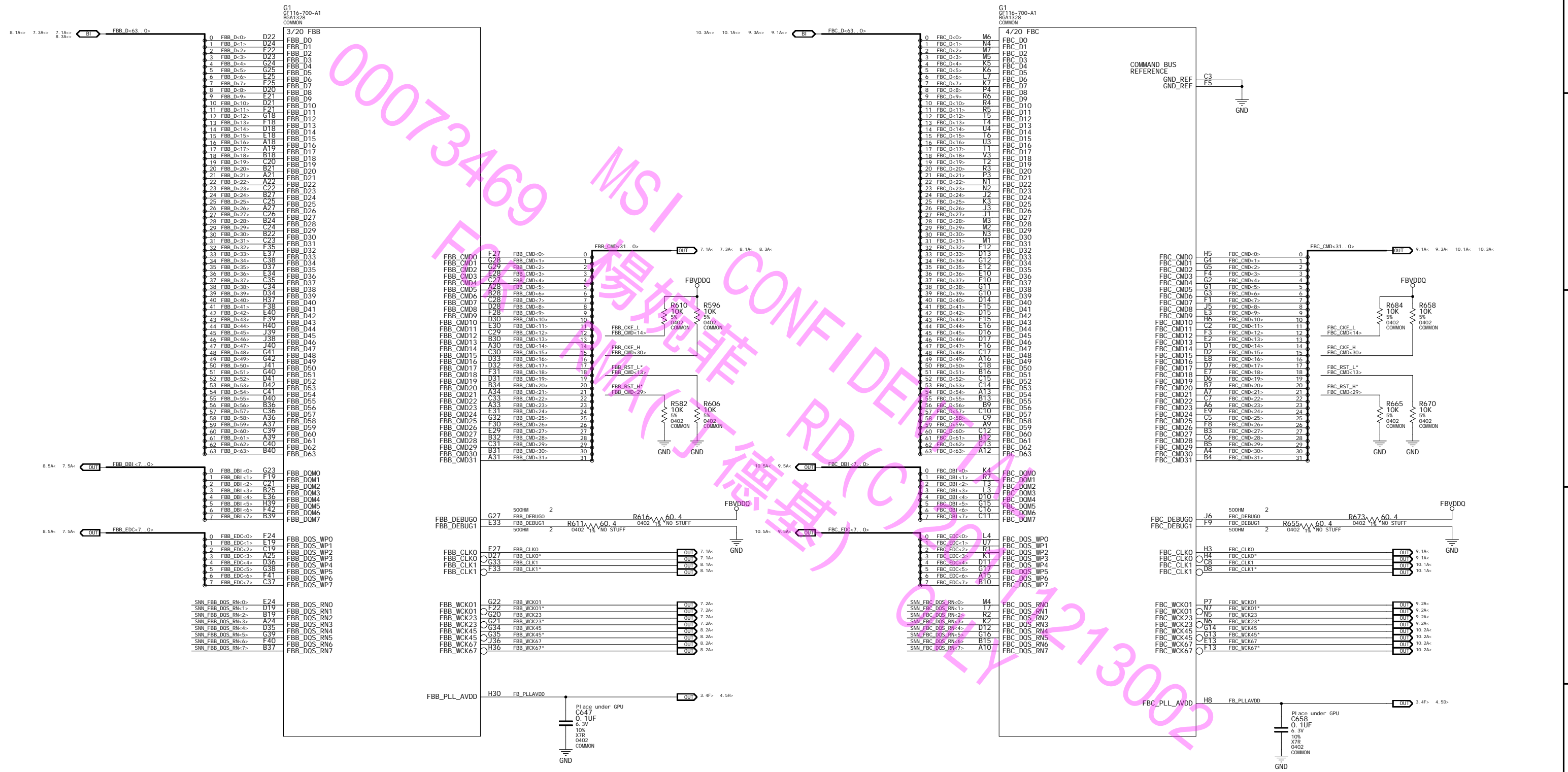
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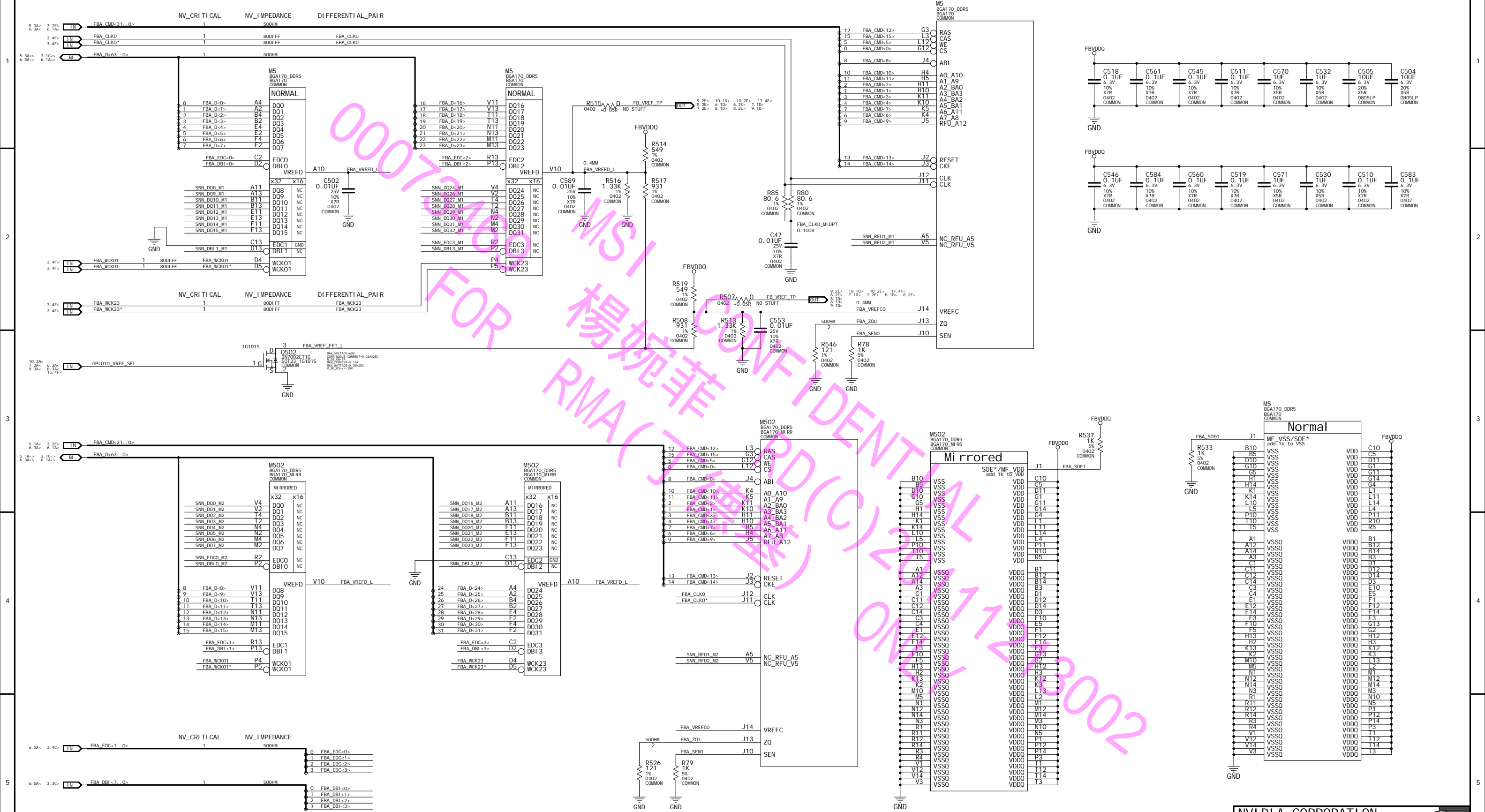
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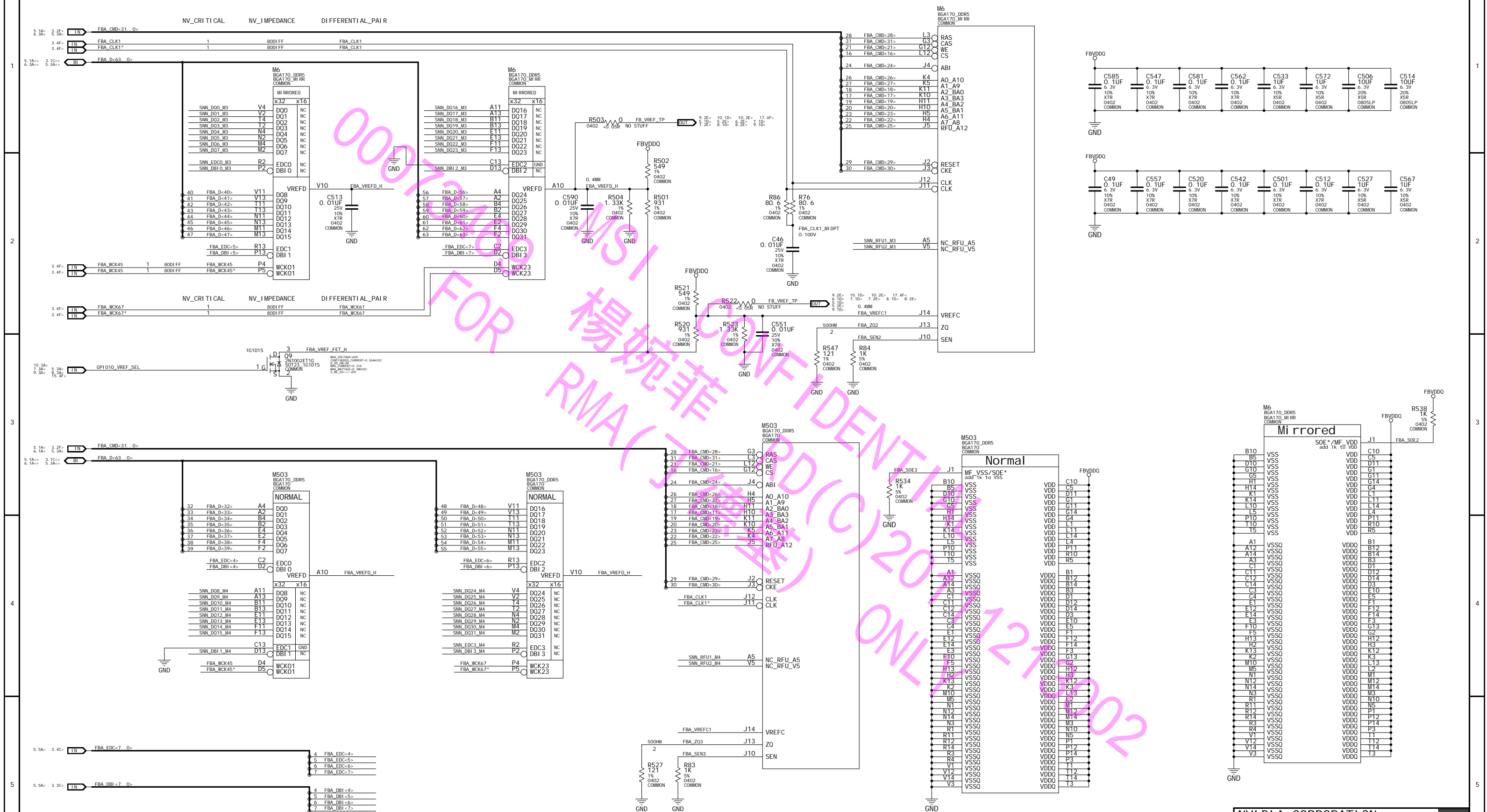
4. Frame Buffer Interface B and C



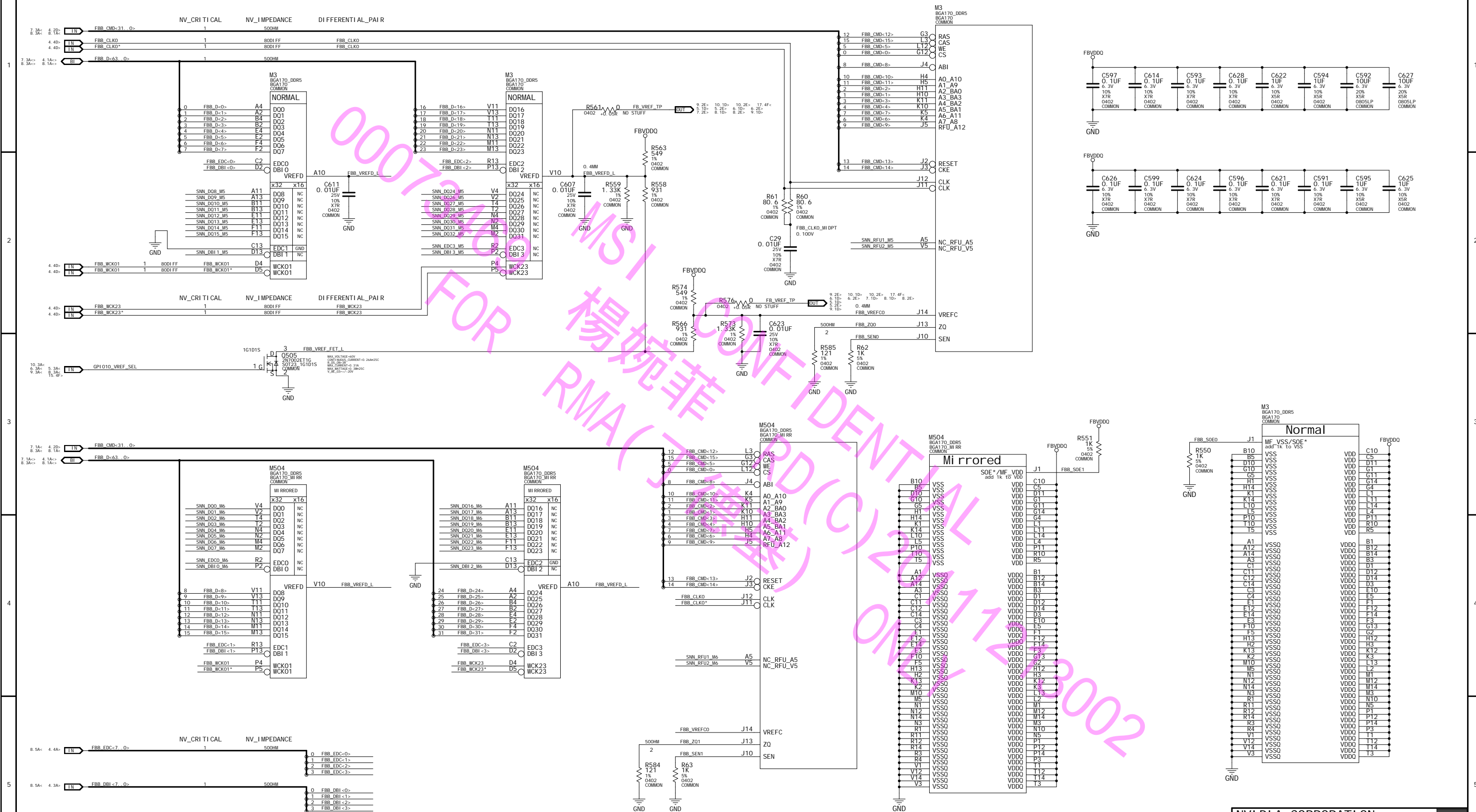
5. Frame Buffer Partition A - Lower Half



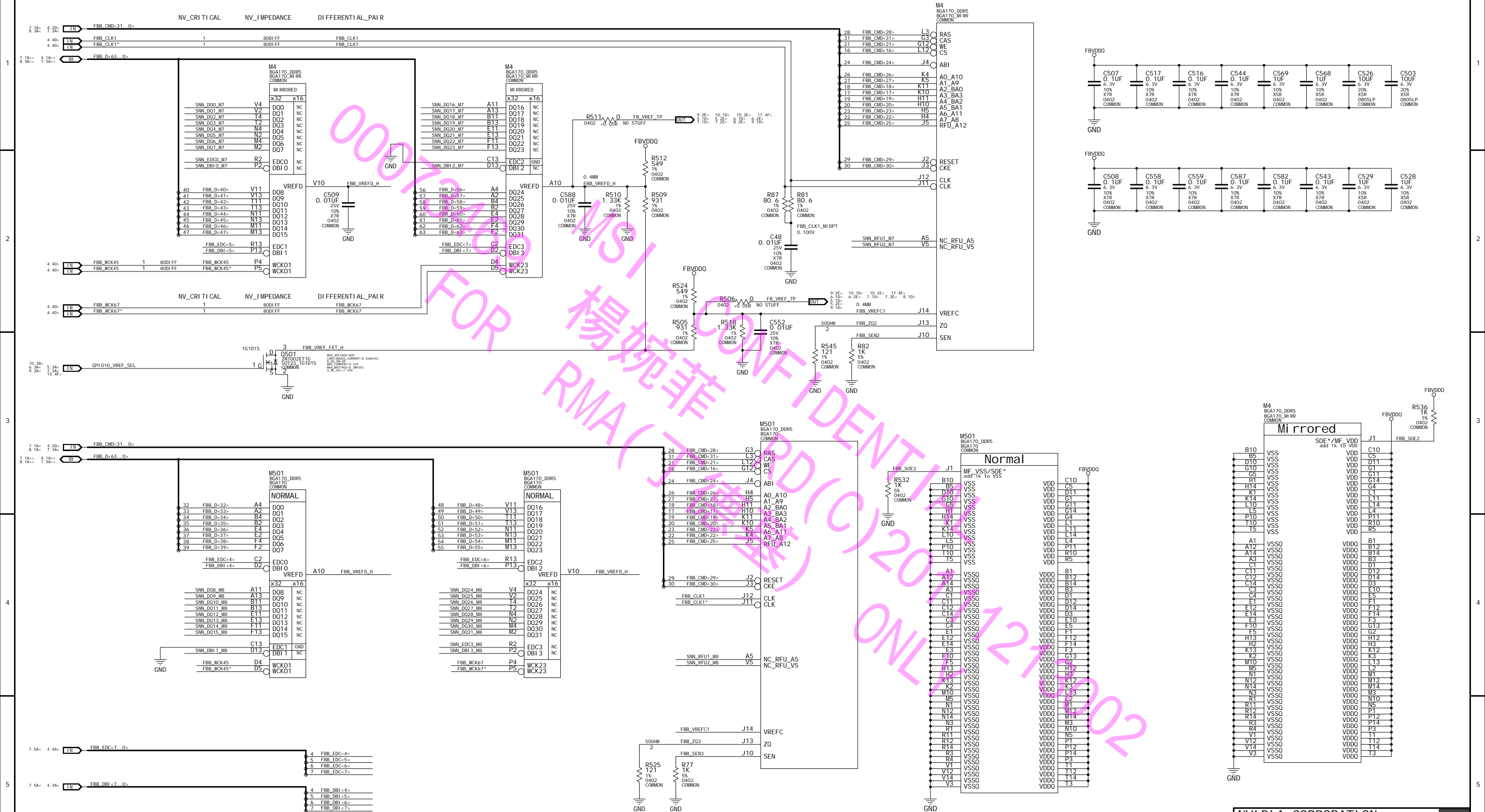
6. Frame Buffer Partition A - Upper Half



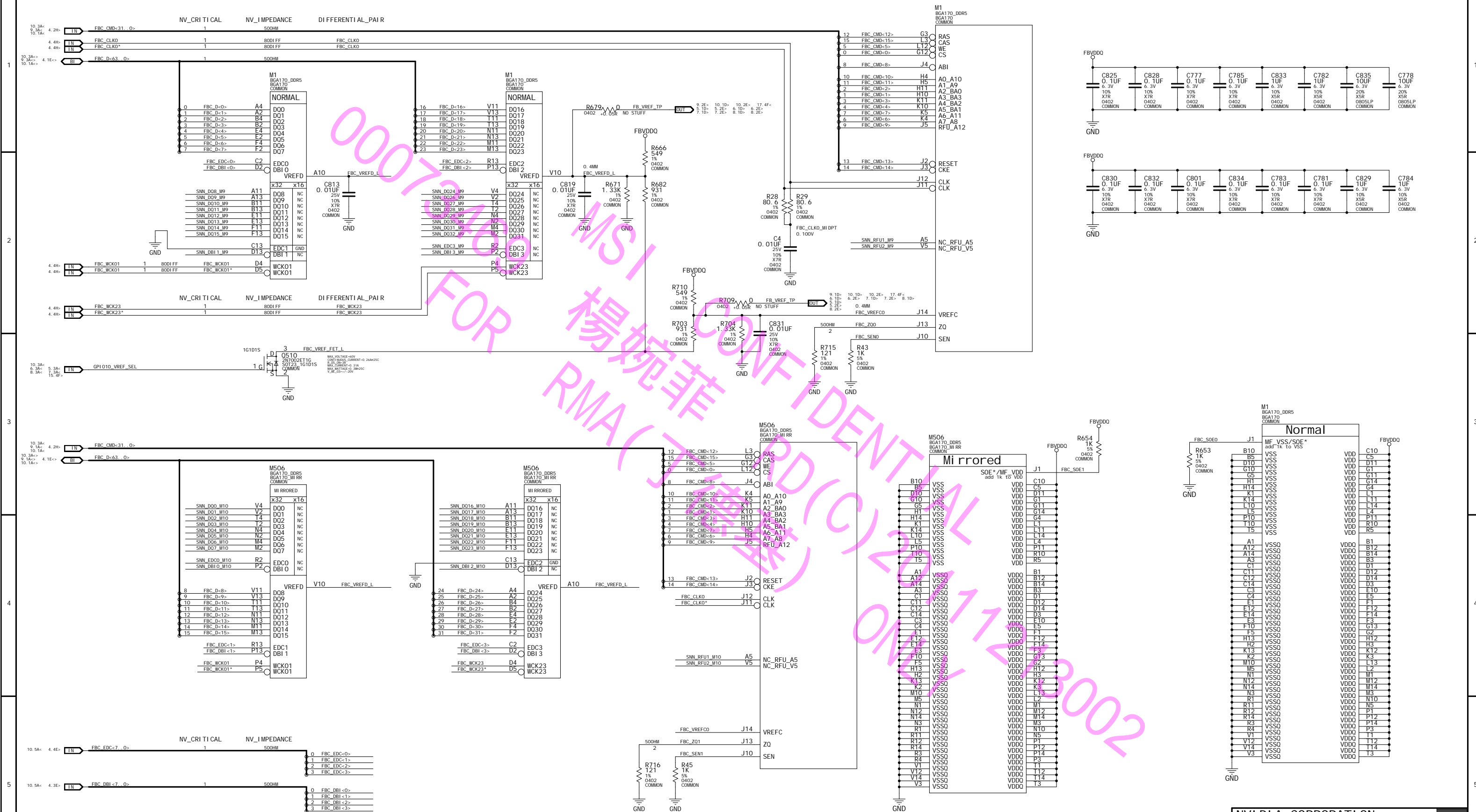
7. Frame Buffer Partition B - Lower Half



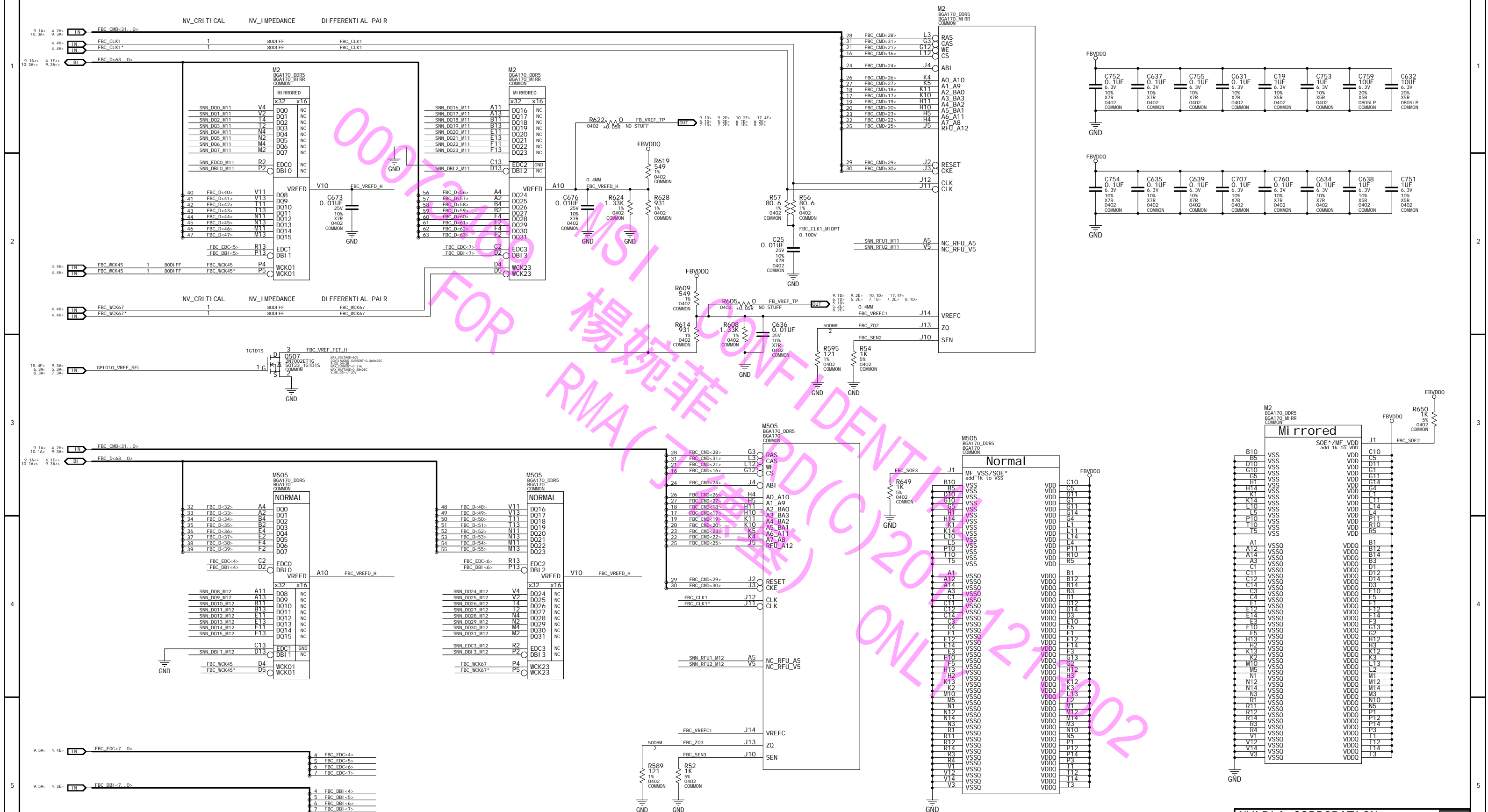
8. Frame Buffer Partition B - Upper Half



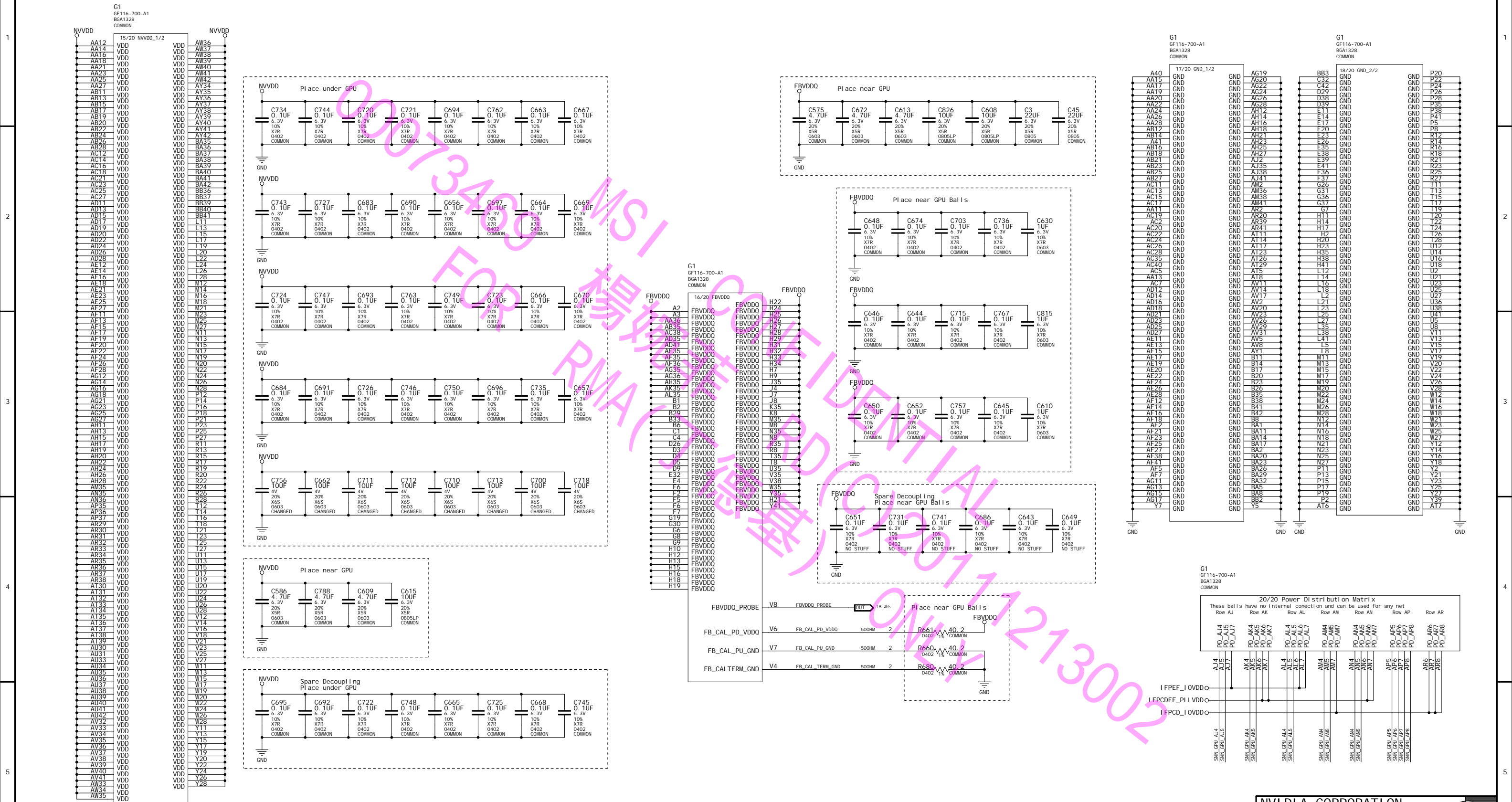
9. Frame Buffer Partition C - Lower Half



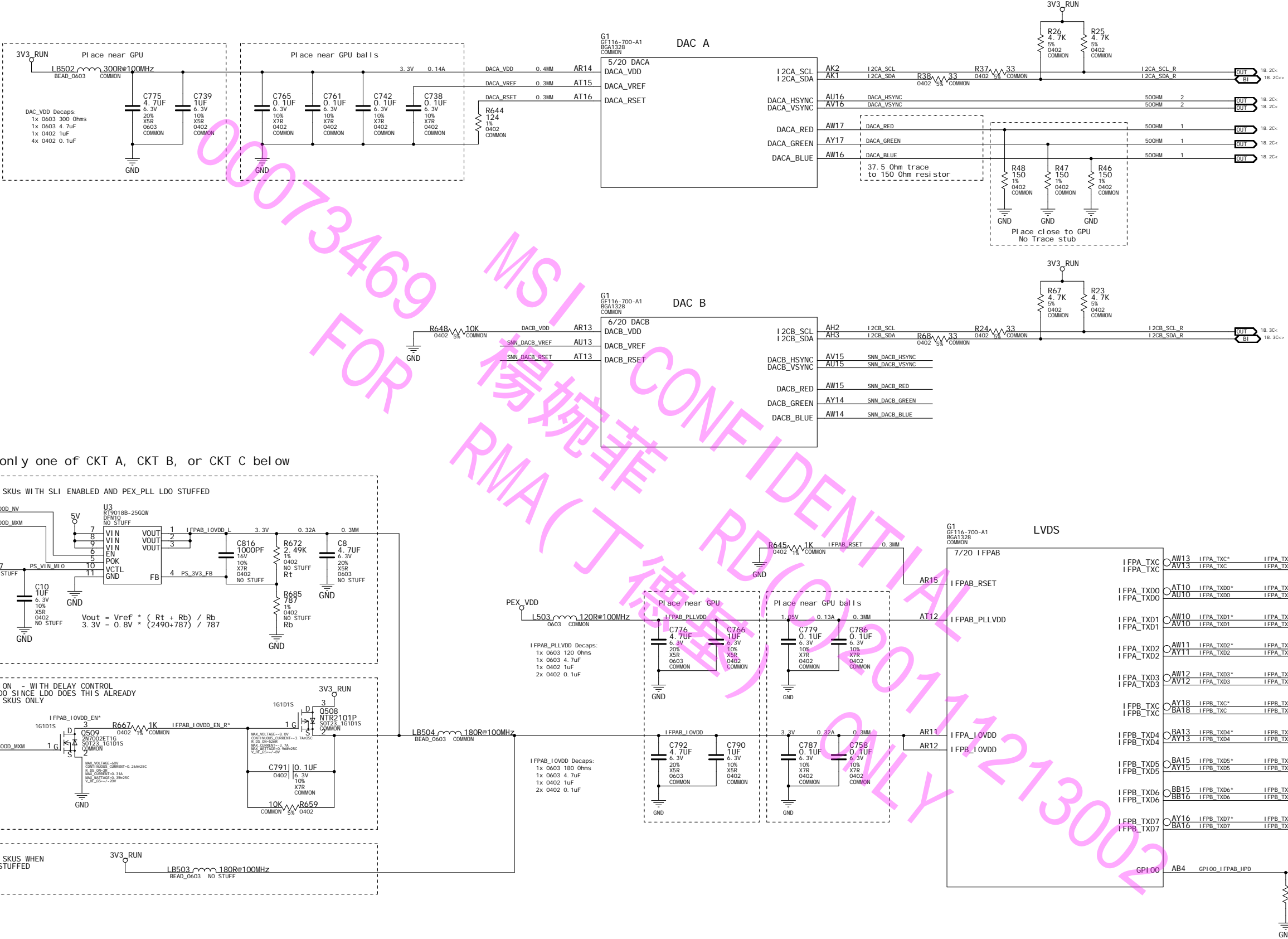
10. Frame Buffer Partition C - Upper Half



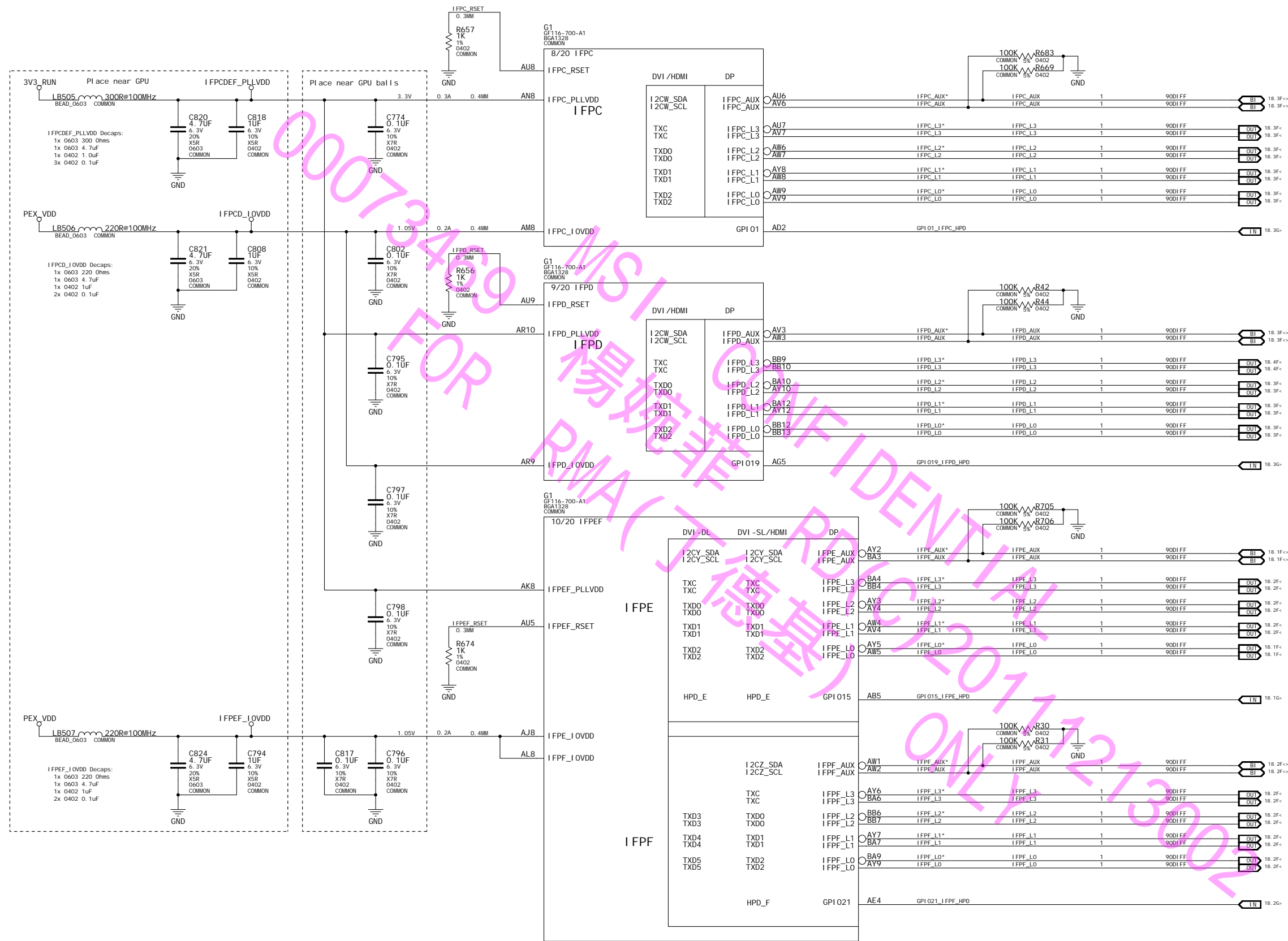
11: NVVDD and FBVDDQ Decoupling

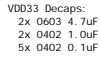


12. DAC_A, DAC_B, LVDS

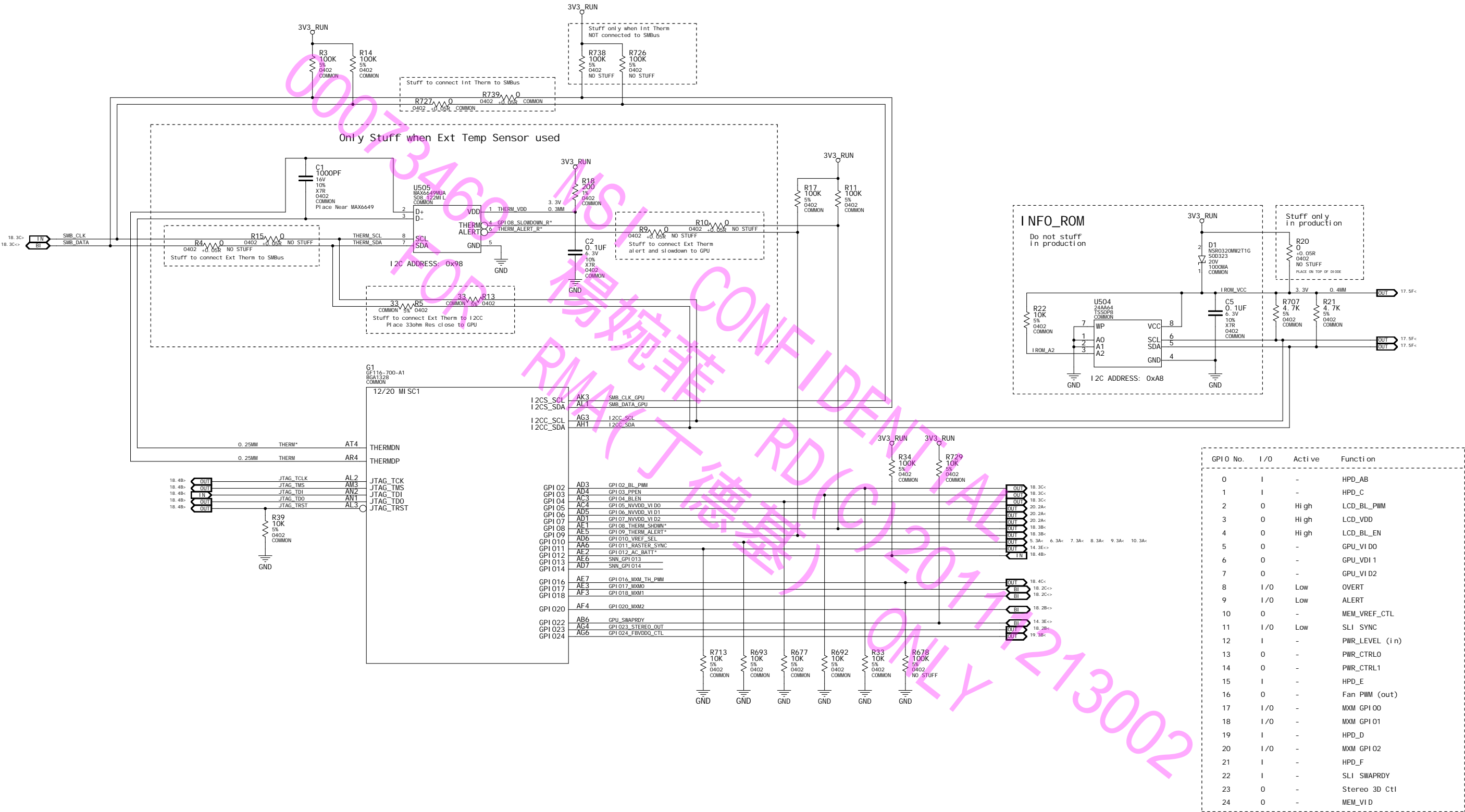


13. DP Links C, D, E, F



[illegible]

15. GPIO, JTAG, INFO_ROM, Thermal Sensor



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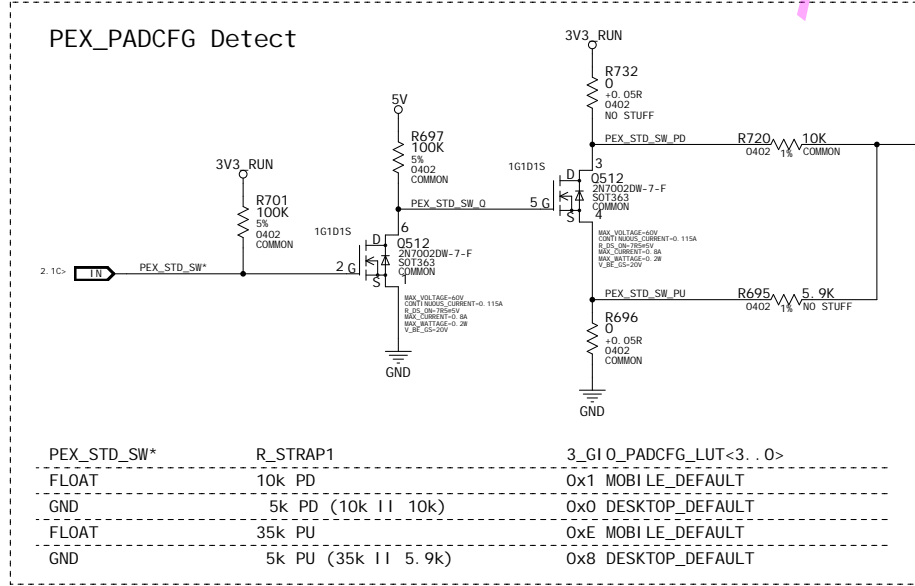
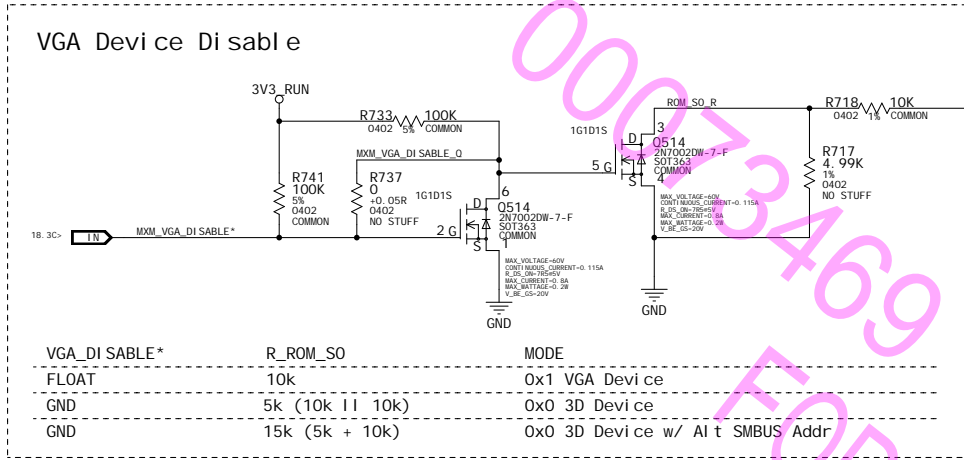
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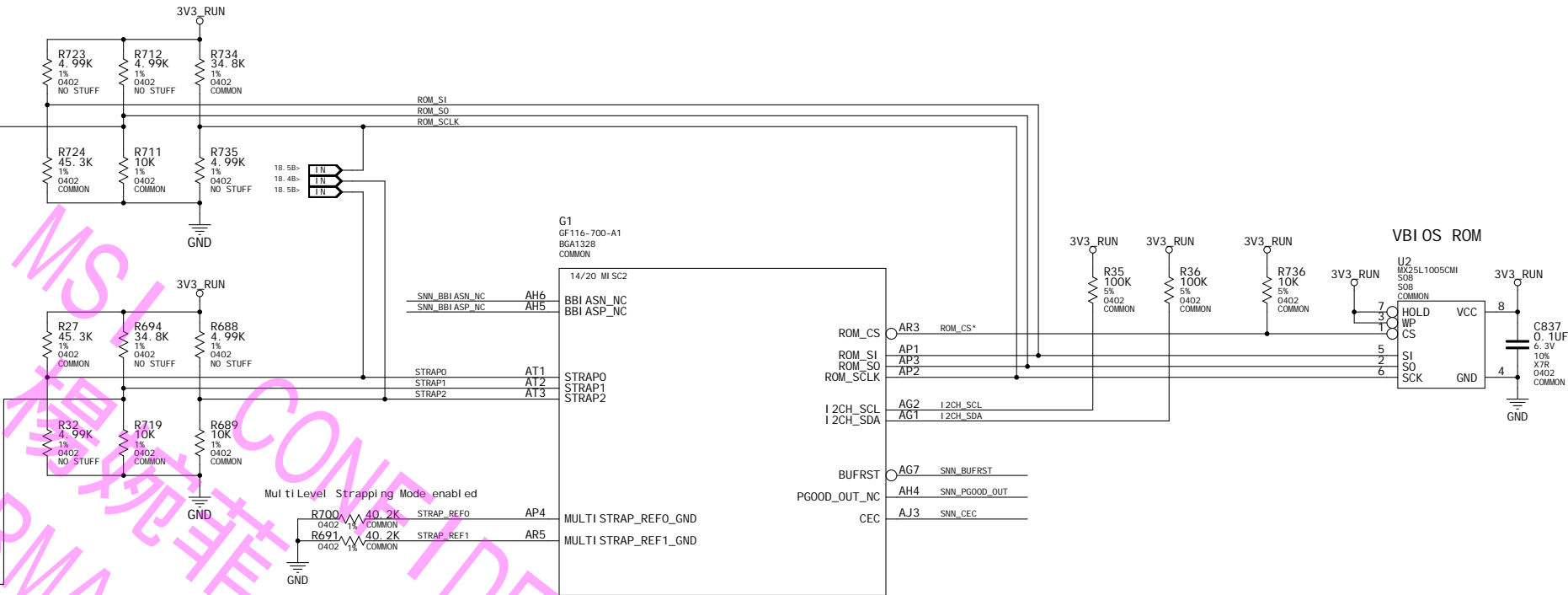
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16. Straps, VGA Di sabl e, PADCFG, VBI OS

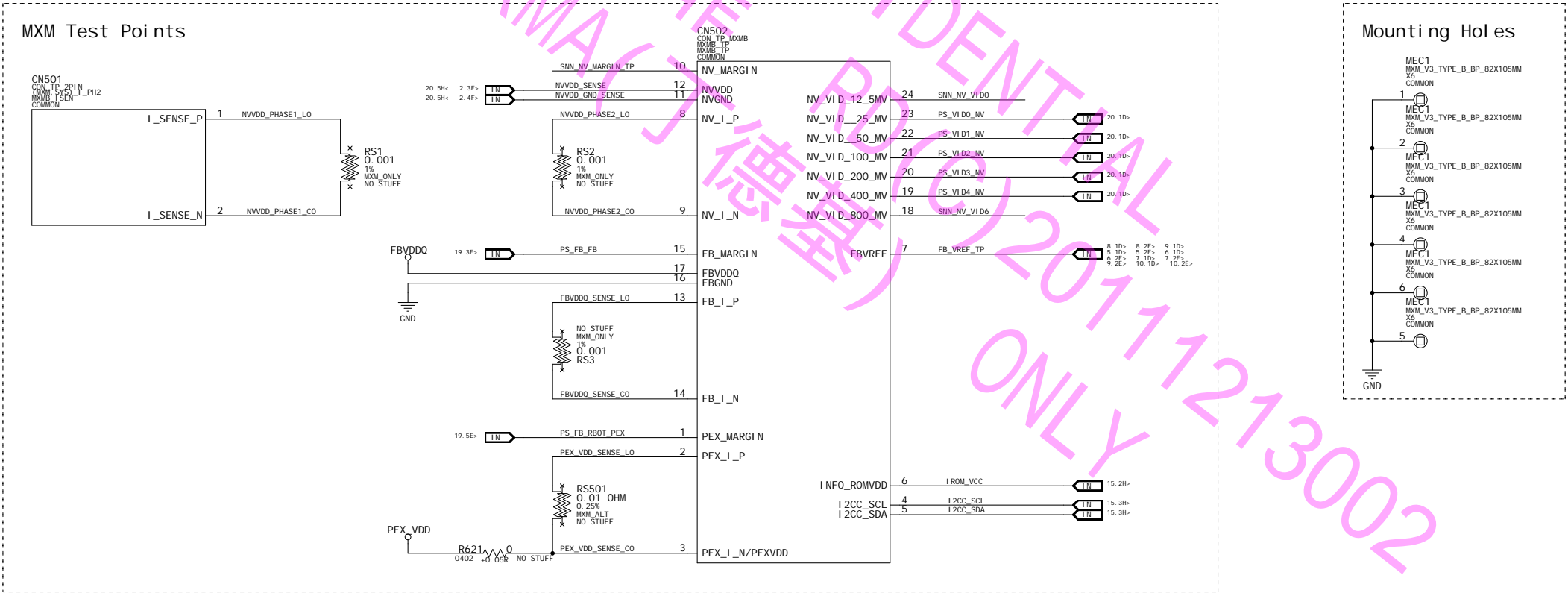
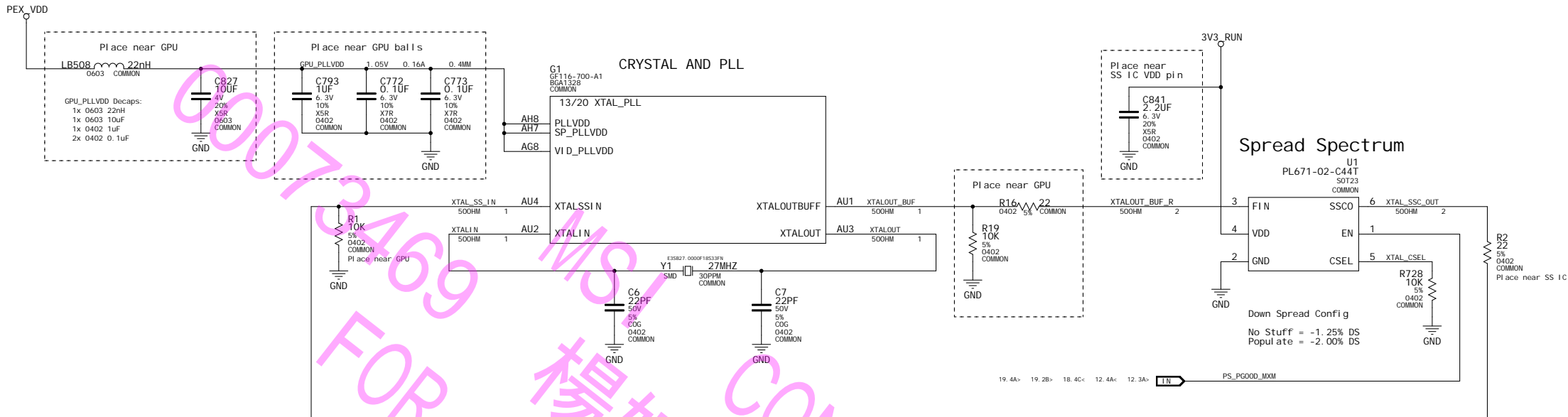


	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111

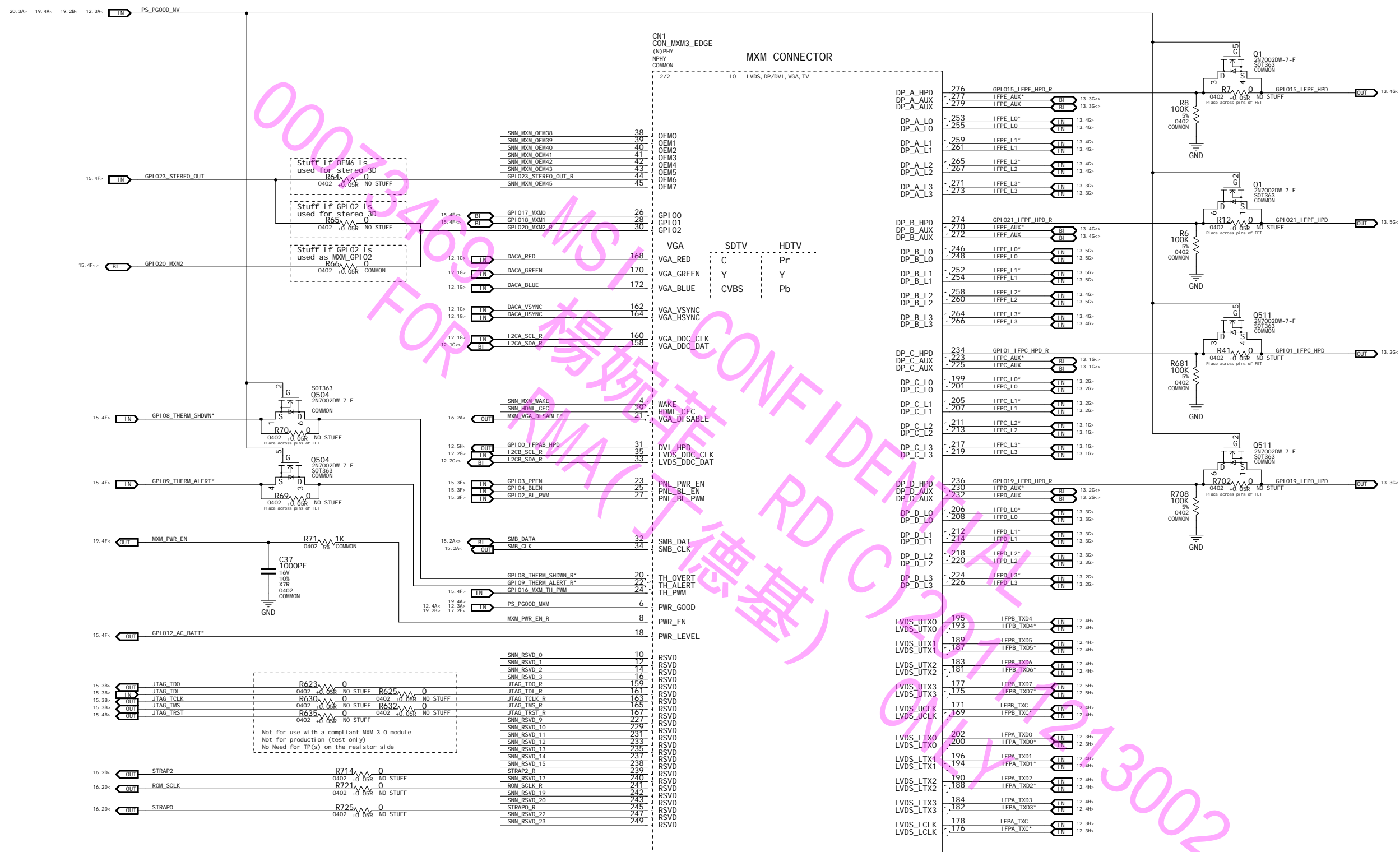


ROM_S0	VGA_DEVI CE	1: VGA DEVI CE
	SMB_ALT_ADDR	0: 0x9E(POR)
	FB_O_BAR SI ZE	0: 256MB(POR)
	XCLK_417	0: 277MHz(POR)
ROM_SI	RAM_CFG[3: 0]	0x4: 128Mx16 192-bi t Hyni x 0x5: 128Mx16 192-bi t Samsu ng 0x6: 64Mx16 192-bi t Hyni x 0x7: 64Mx16 192-bi t Samsu ng
ROM_SCLK	PEX_PLL_EN_TERM100	0: DI SABLED (POR)
	SLOT_CLK_CONF IG	1: GPU and MCH COMMON REFCLK
	SUB_VENDOR	1: VBI OS ROM I S PRESENT
	PCI_DEVI D_EXT	1: PCDEVI D[4]
STRAP0	USER_BI T[3: 0]	0xF: EDI D used
STRAP1	3GI O_PADCFG_LUT_ADR[3: 0]	0x1: Mobi le (l ow swi ng) 0x0: Deskt op (hi gh swi ng)
STRAP2	PCI_DEVI D[3: 0]	0x1: SKU1, SKU2, SKU12-15 0x2: SKU3 TBD: SKU501, SKU502

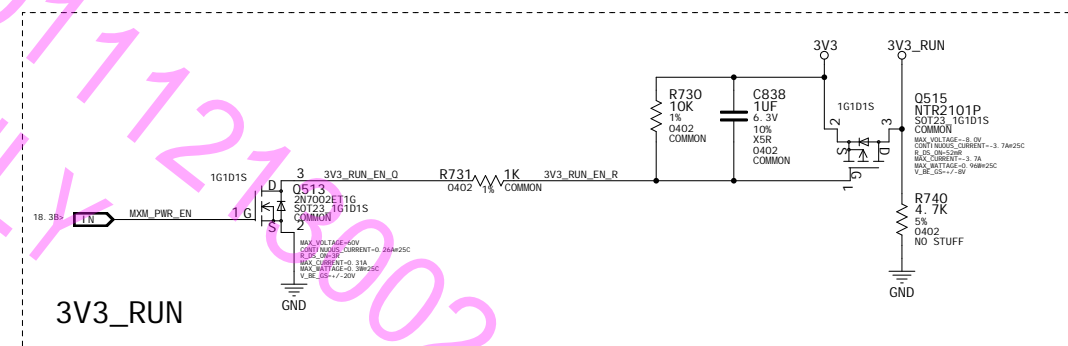
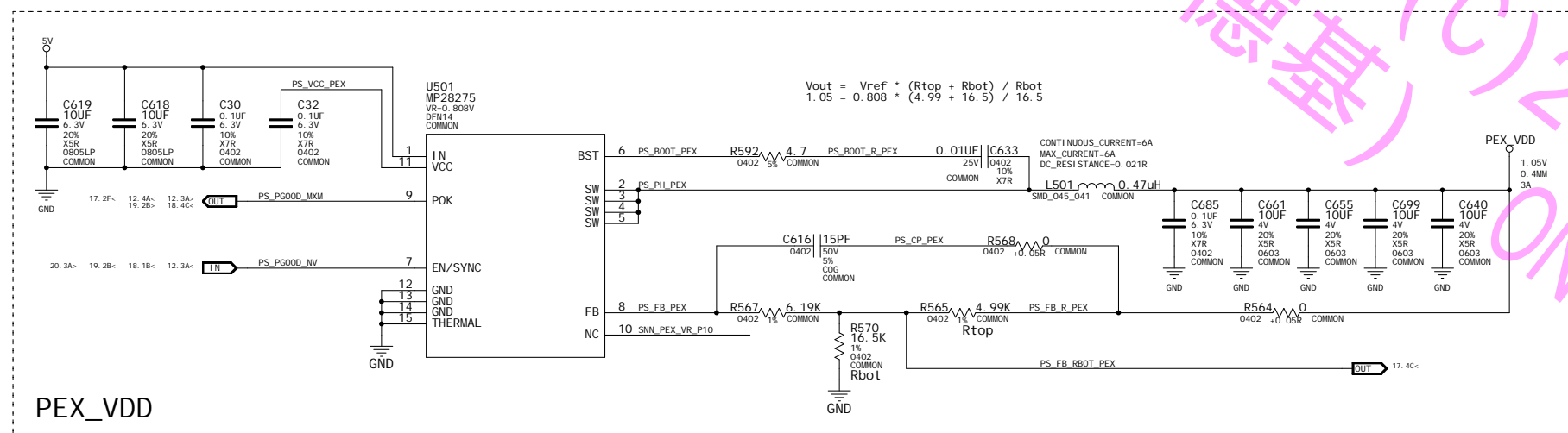
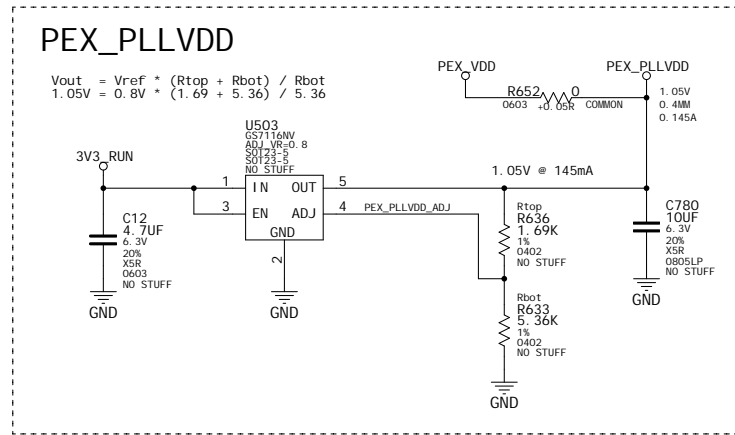
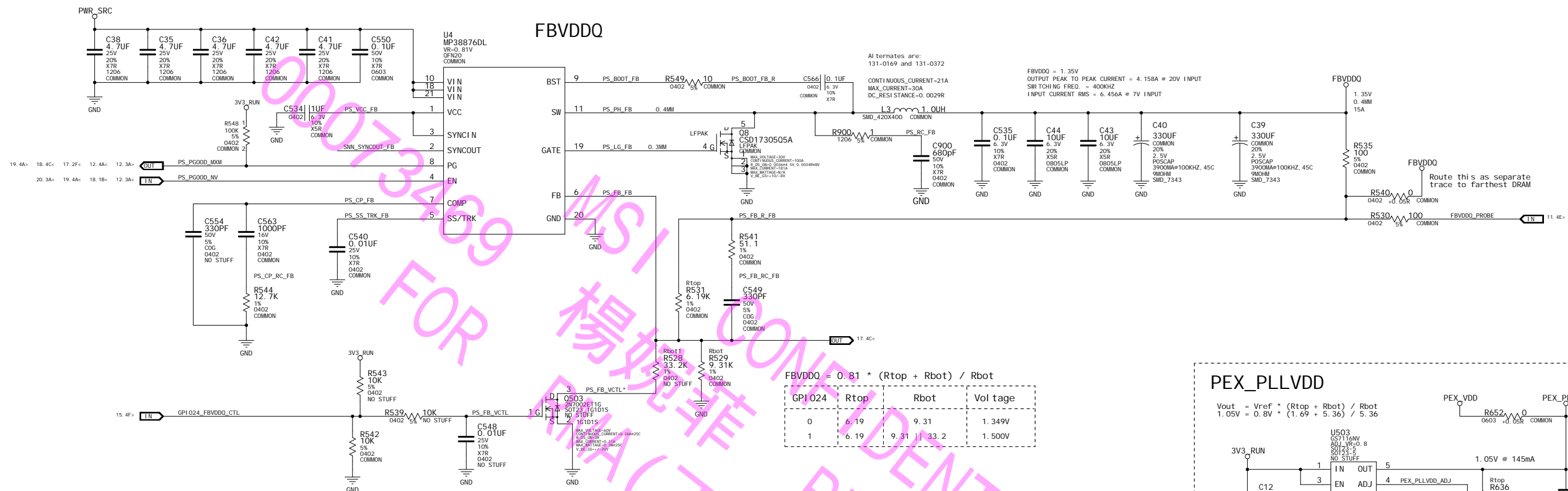
17. PLL, Crystal , Spread, MXM Test Points, Mounting Holes



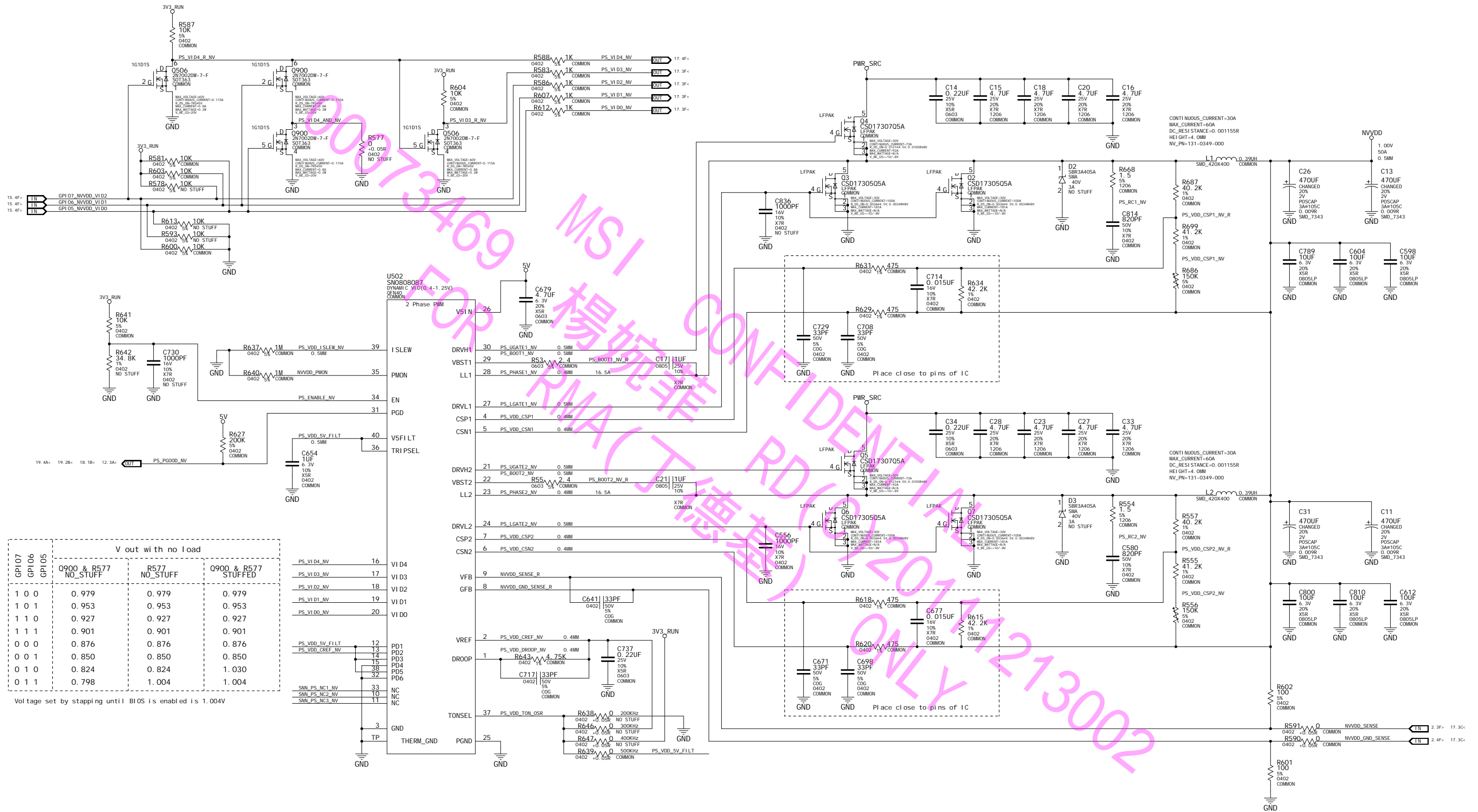
18. MXM Connector



19. FBVDDQ, PEX_PLLVDD, PEX_VDD, 3V3_RUN




20. NVVDD POWER SUPPLY



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