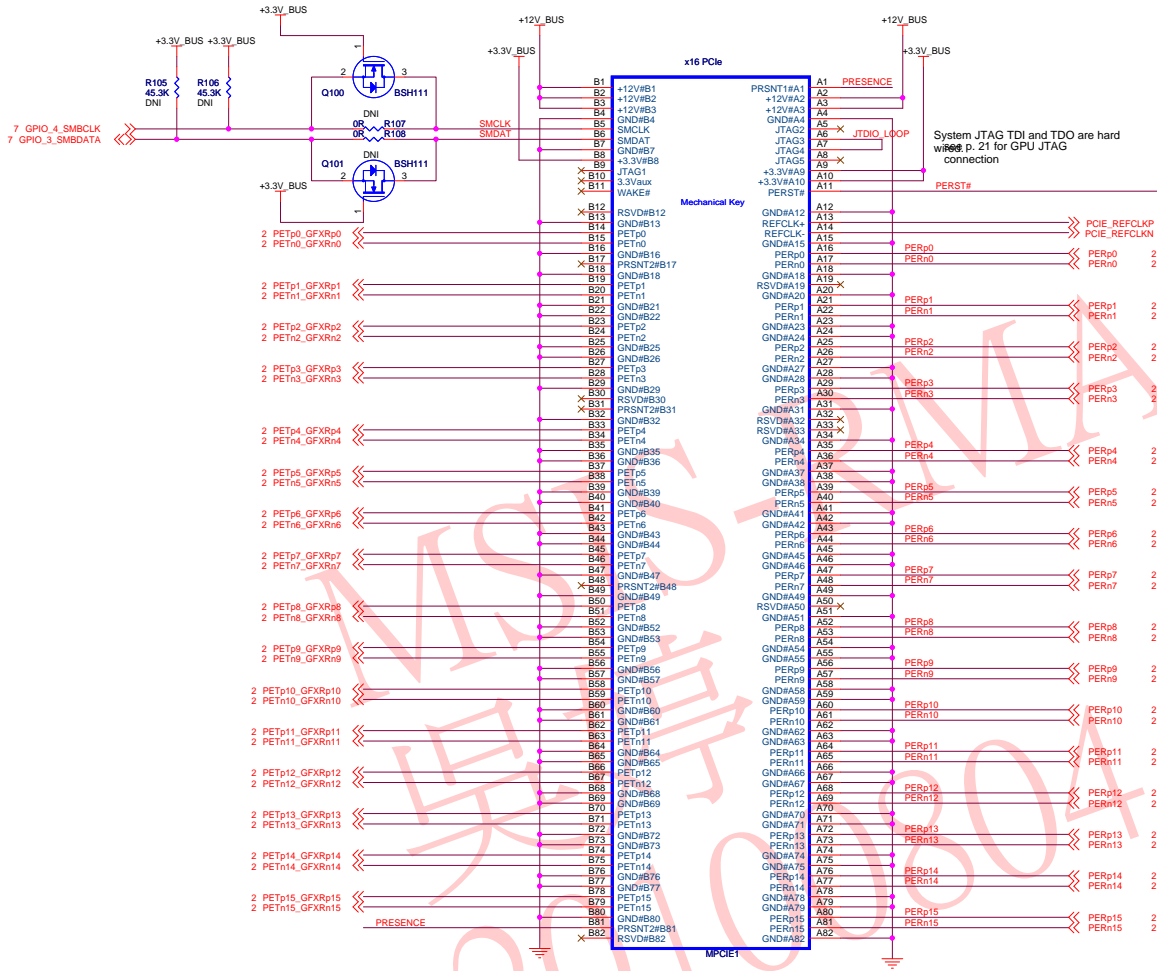
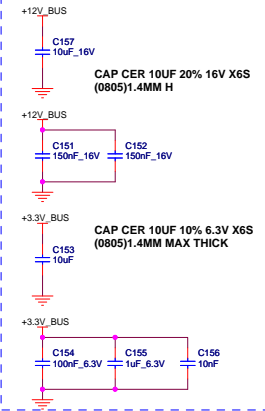


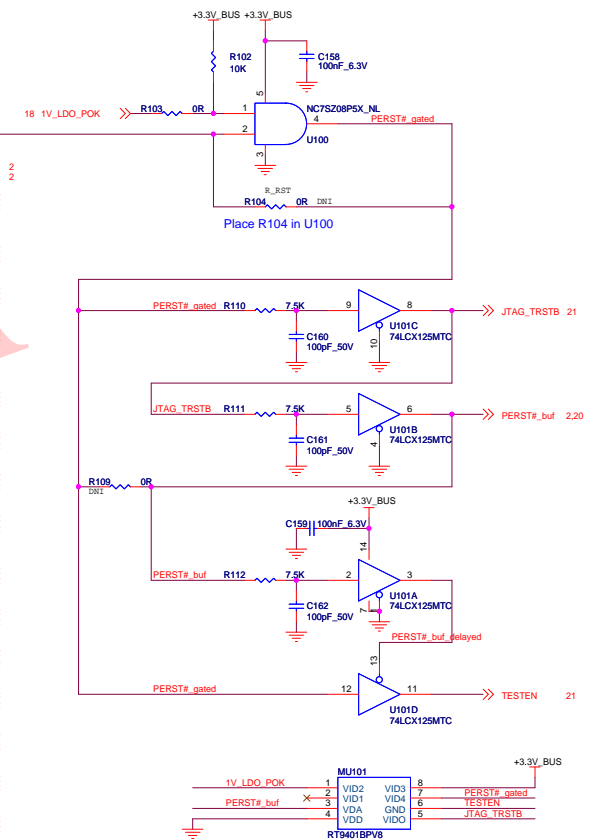
PCI-EXPRESS EDGE CONNECTOR



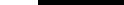
Place these caps as close to the PCIe connector as possible



PCIe RESET Buffered

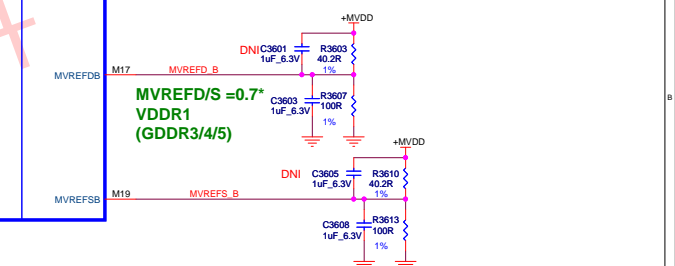
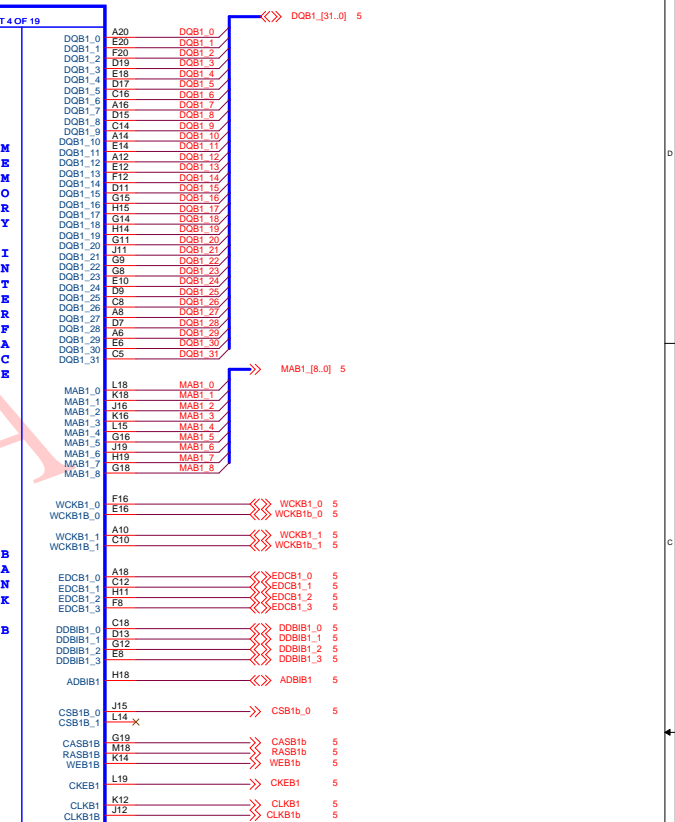
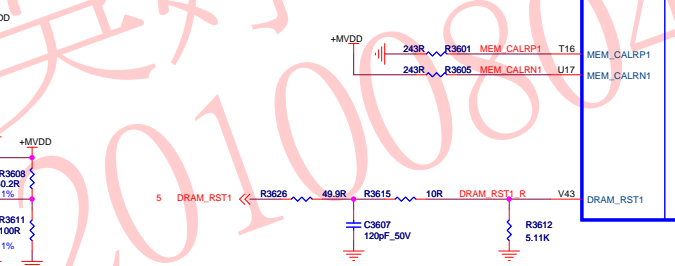
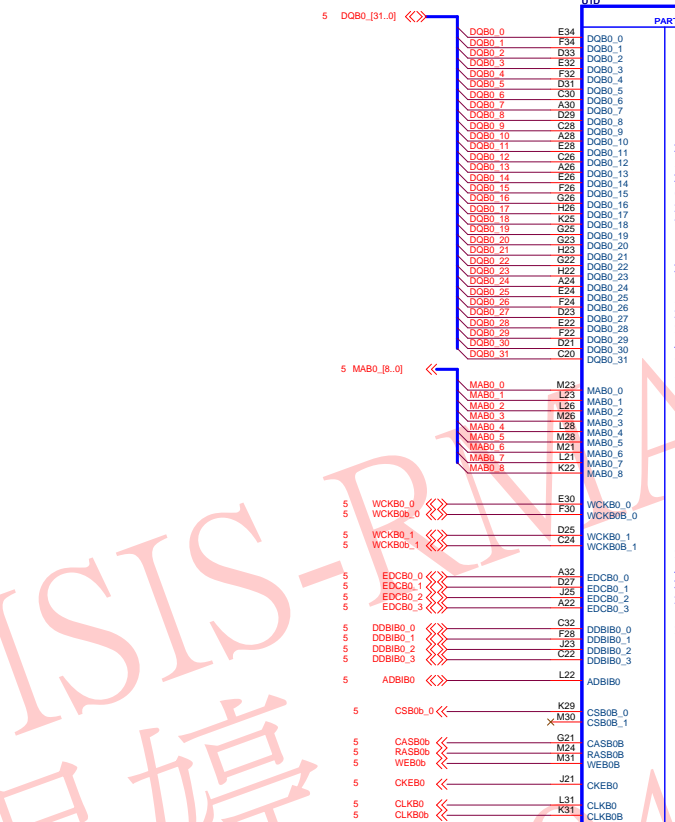
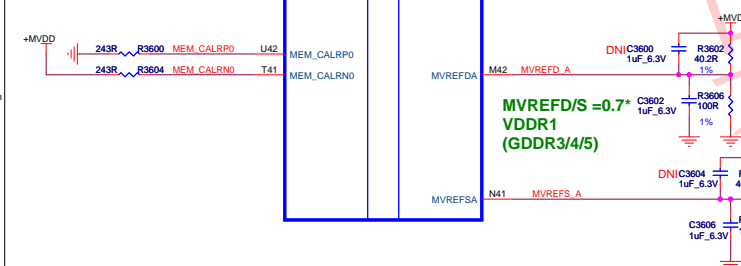
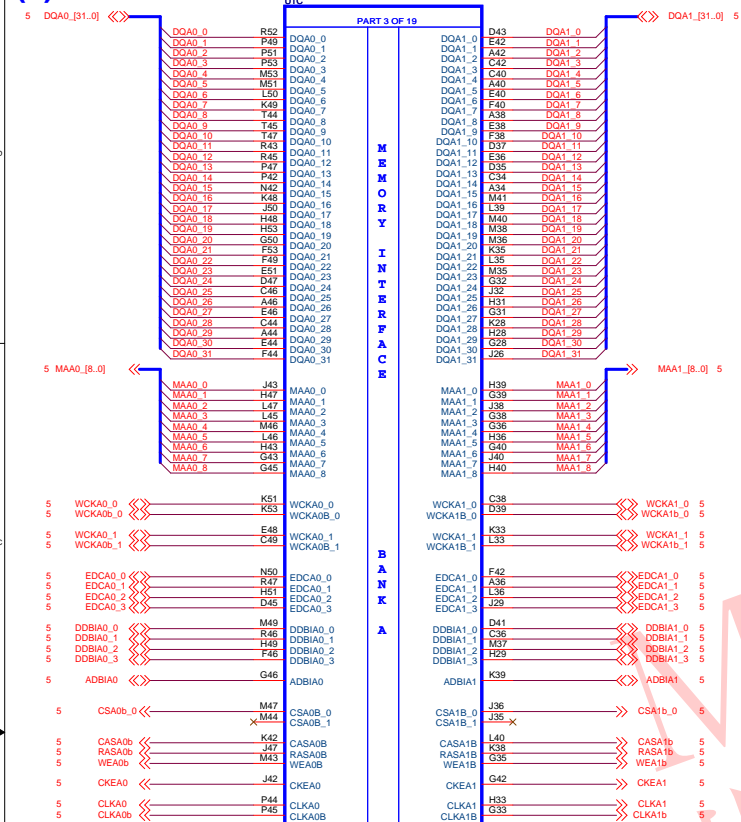


SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
	BRING UP ONLY

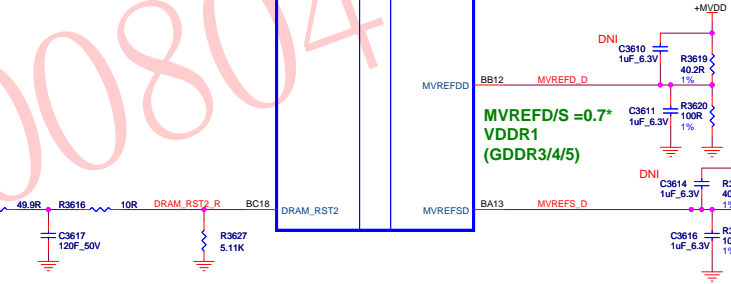
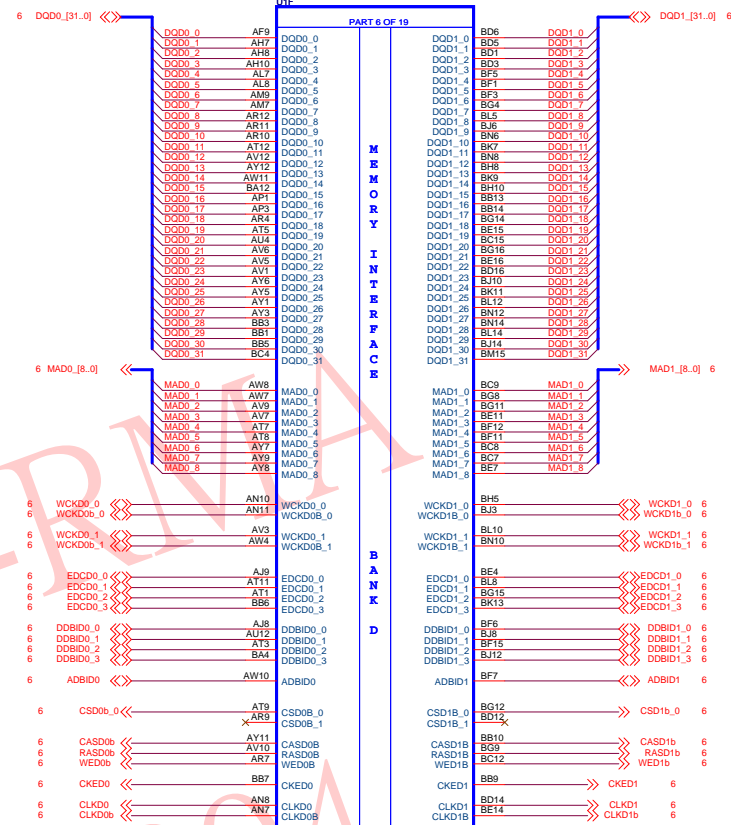
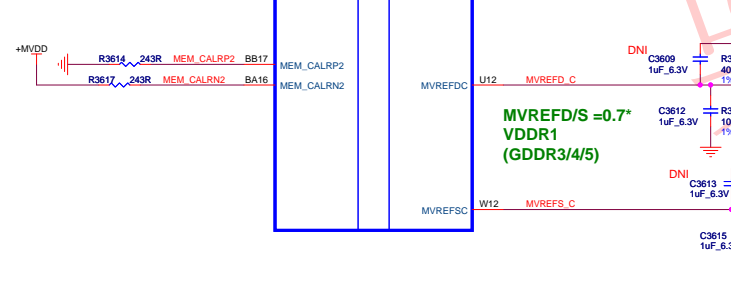
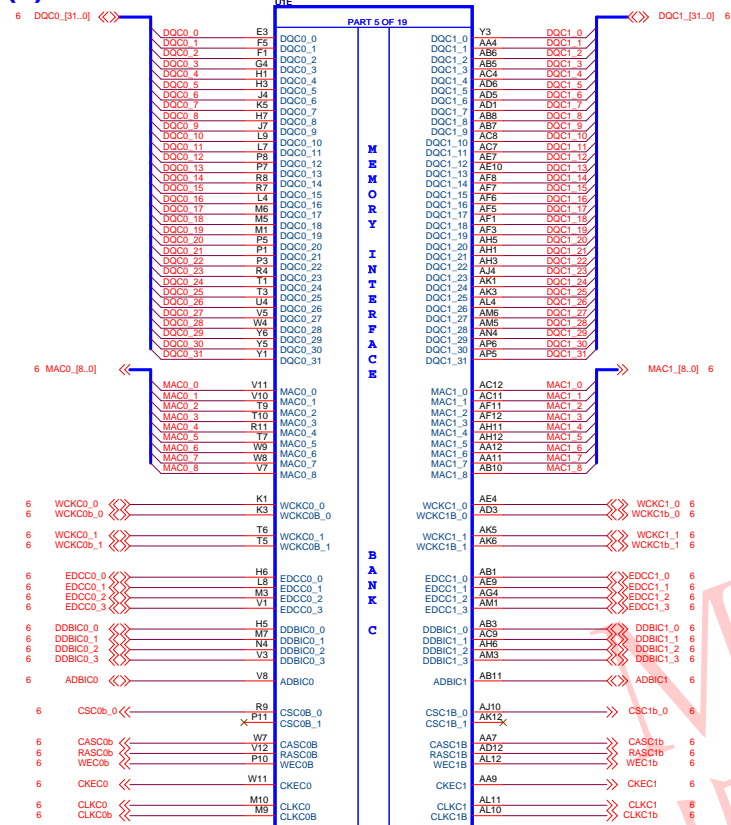
				<p>CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC. TM907 Advanced Micro Devices</p> <p>This AMD Board Schematic and design is the exclusive property of AMD, and is provided only to assist under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.</p> <p>Title ASIC PCIE Interface</p>				<p>Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario</p> 			
				<p>Date: Tuesday, December 15, 2009 Rev: 2</p>							
				<p>Sheet 2 of 23</p>							
				<p>Doc No. 105-C008XX-00C</p>							



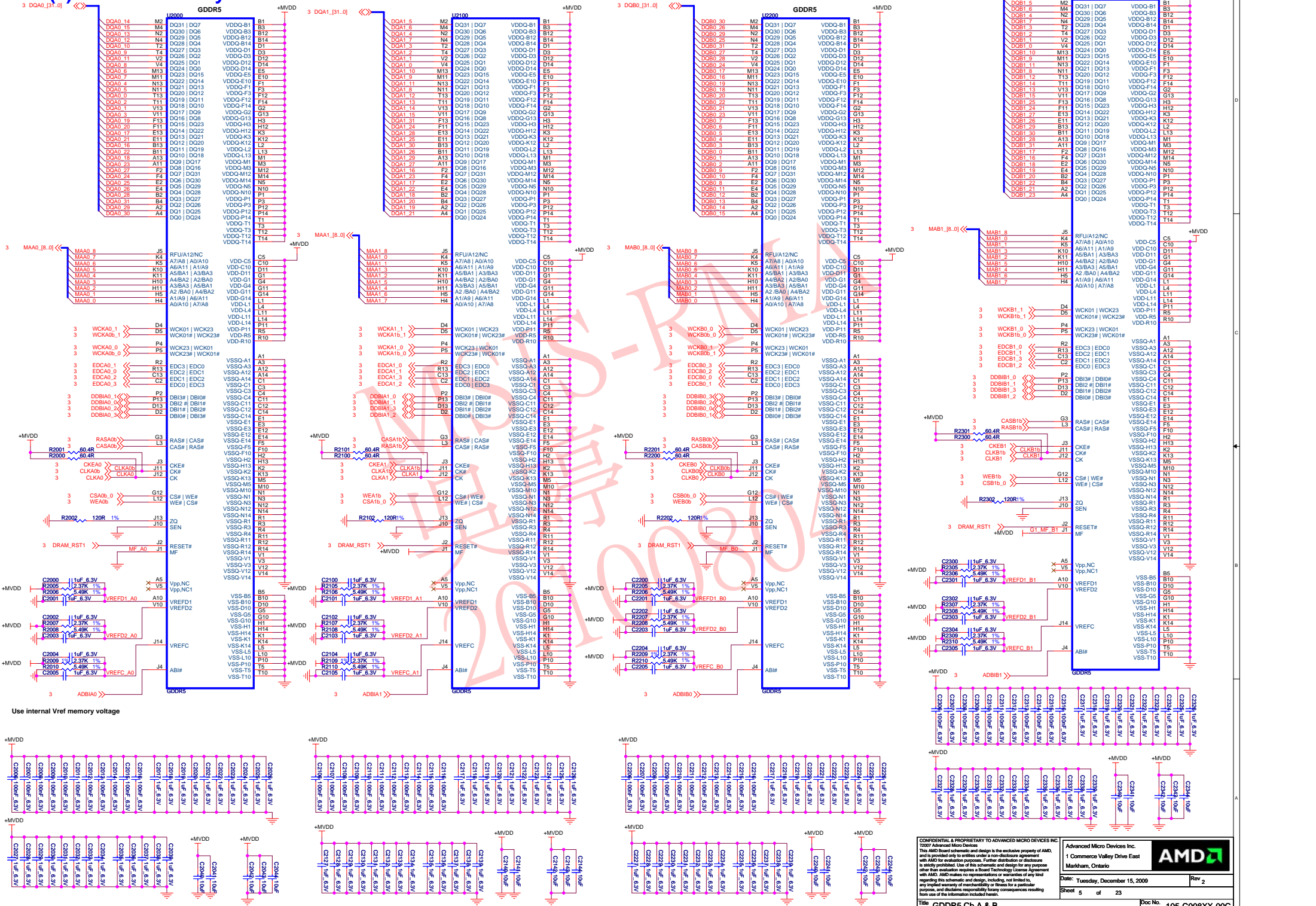
(3) CYPRESS MEM Interface Ch A&B



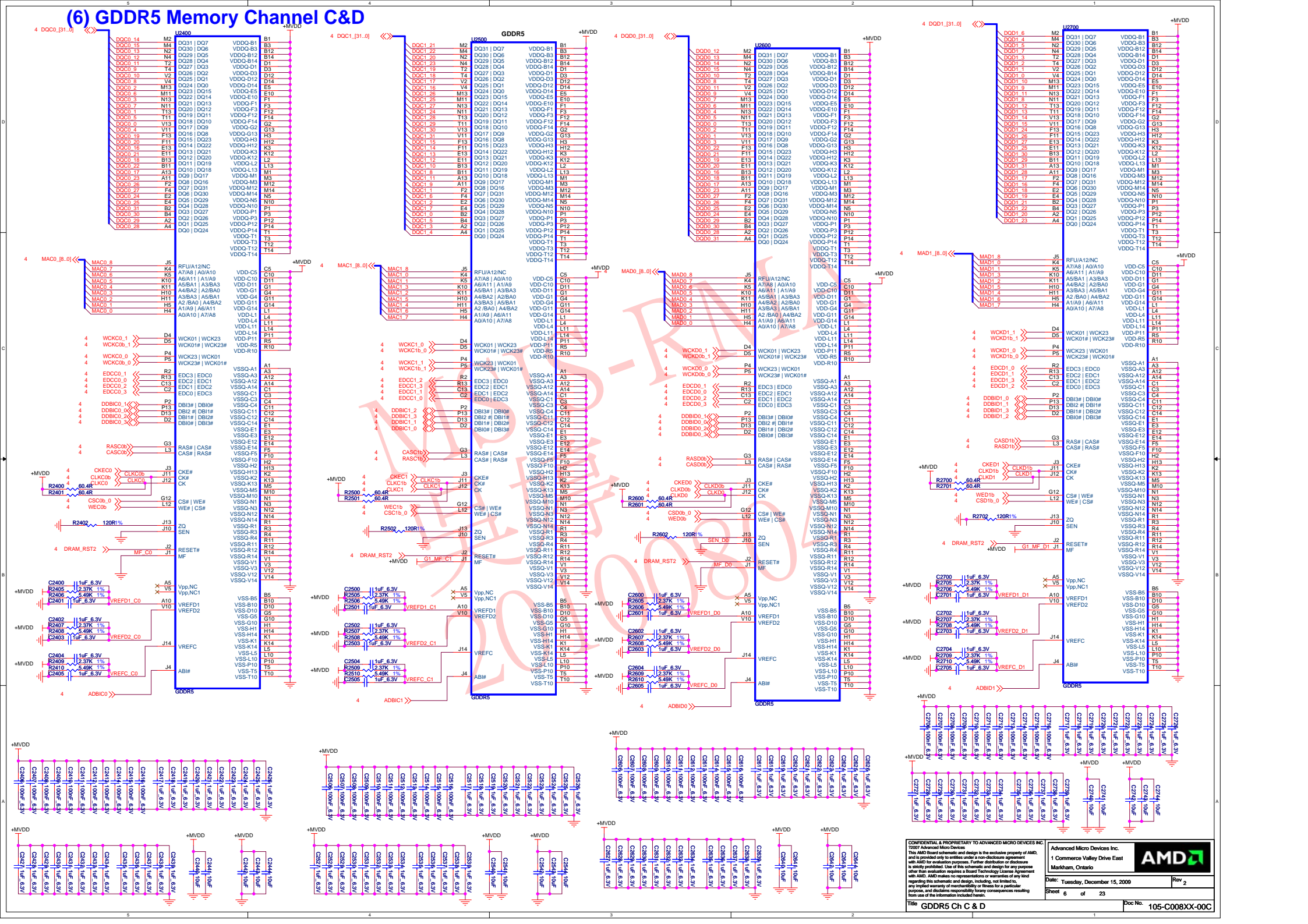
(4) CYPRESS MEM Interface Ch C&D



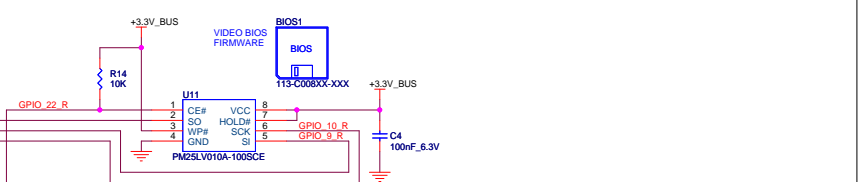
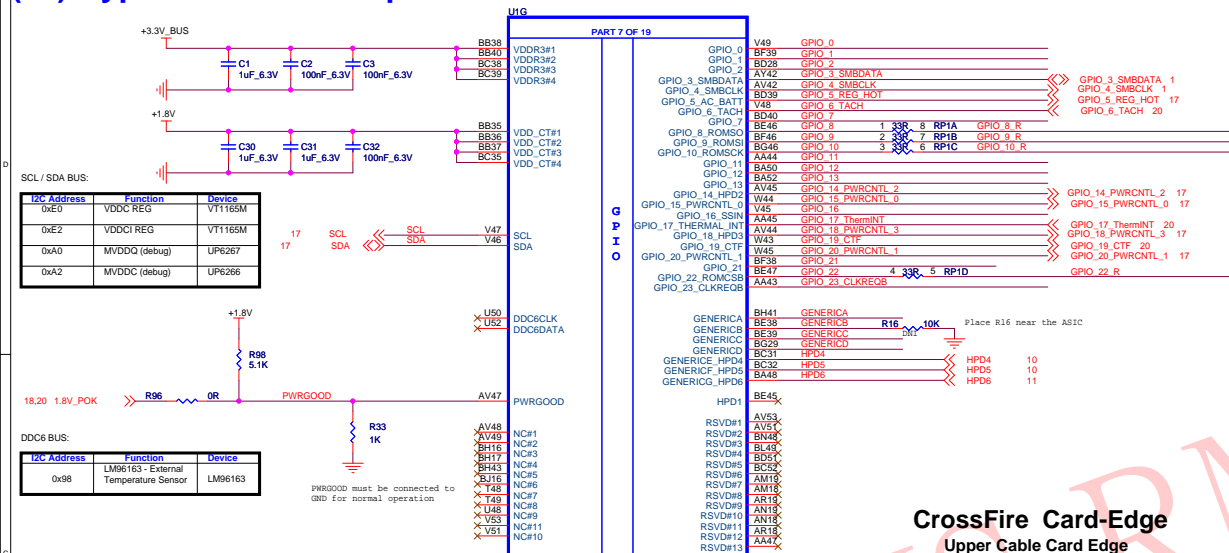
(5) GDDR5 Memory Channel A&B



(6) GDDR5 Memory Channel C&D



(07) Cypress GPIOs Strap CF XTAL OSC

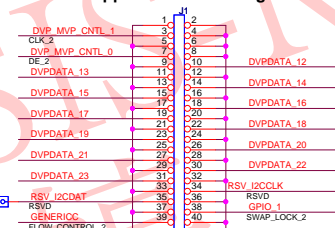


PIN BASED STRAPS

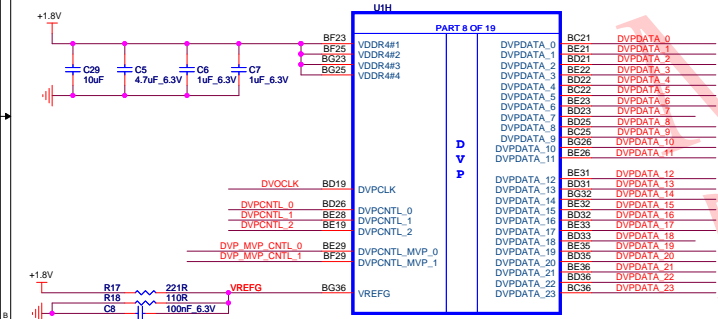
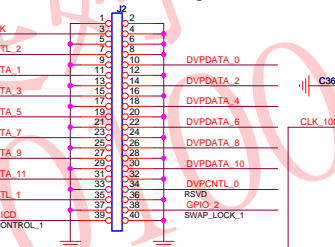



CrossFire Card-Edge


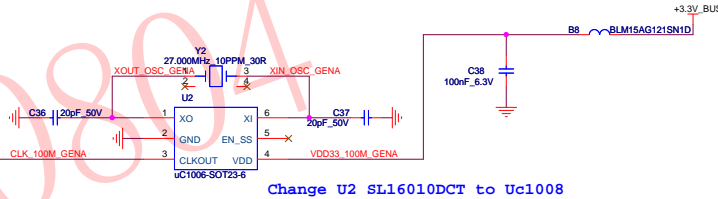
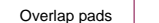
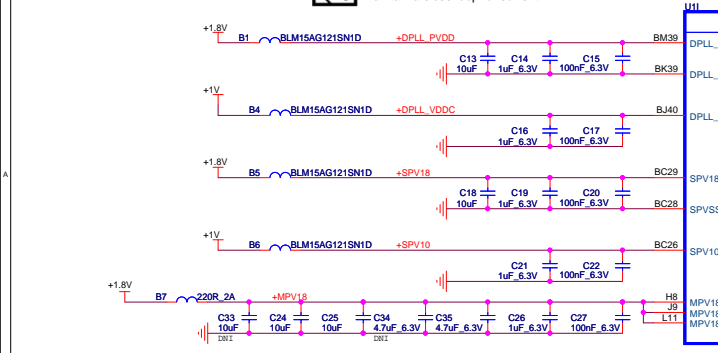
Upper Cable Card Edge



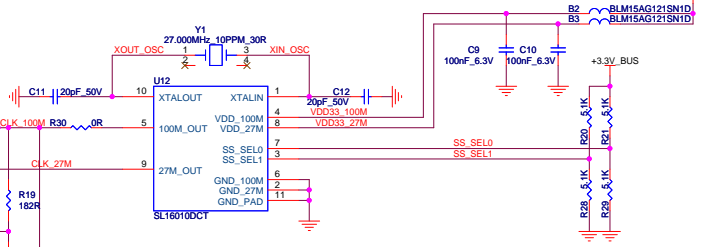
Lower Cable Card Edge



 Place the crossfire testpoints near the ASIC and not the connector

 Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

Change U2 SL16010DCT to Uc1008



Co-lay Uc1008 with U12 SL16010DCT

CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.
©2007 Advanced Micro Devices

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

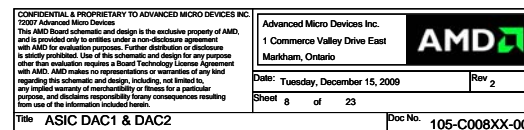
The AMD logo, featuring the letters "AMD" in a bold, sans-serif font, followed by a green square icon containing a white stylized "A" shape.

Date: Tuesday, December 15, 2009	Rev 2
Sheet 7 of 23	

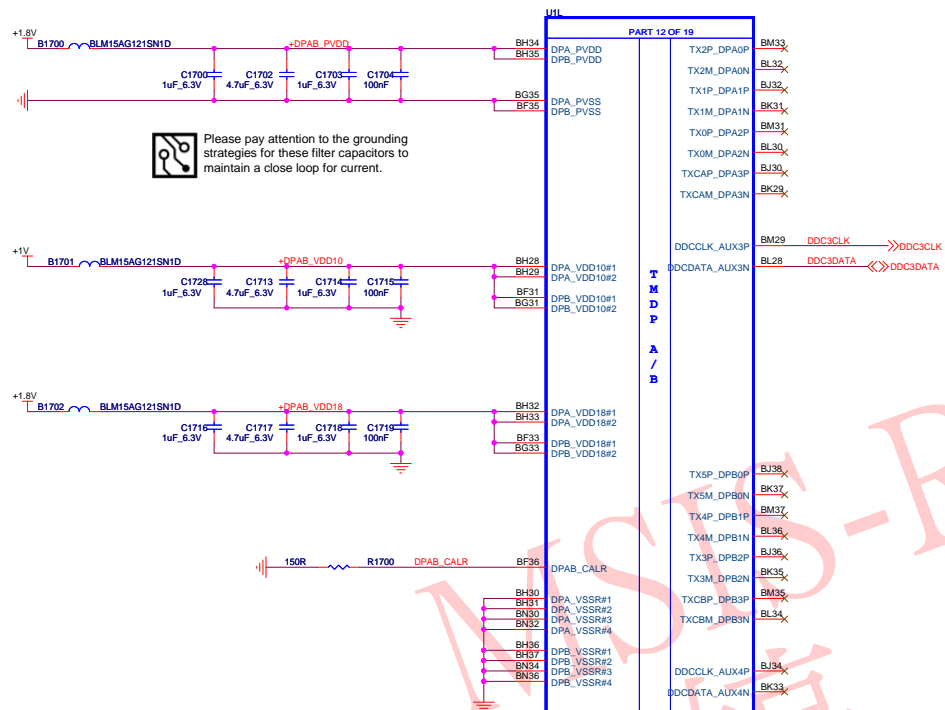
Title ASIC GPIO, STRAPS, CF, and XTAL

Doc No.	105-C008XX-00C
---------	----------------

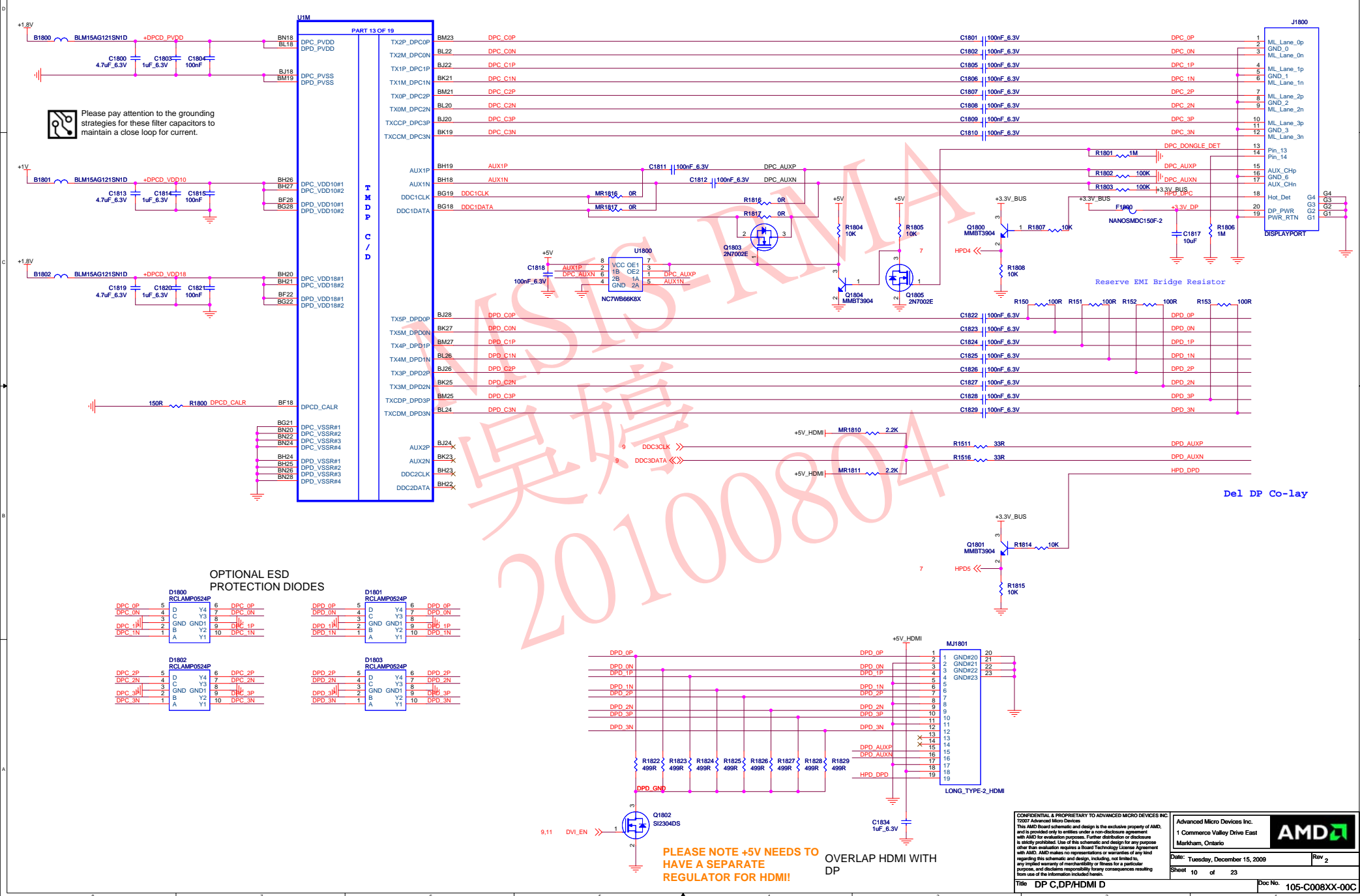
Del Optional ECD protection DIODES



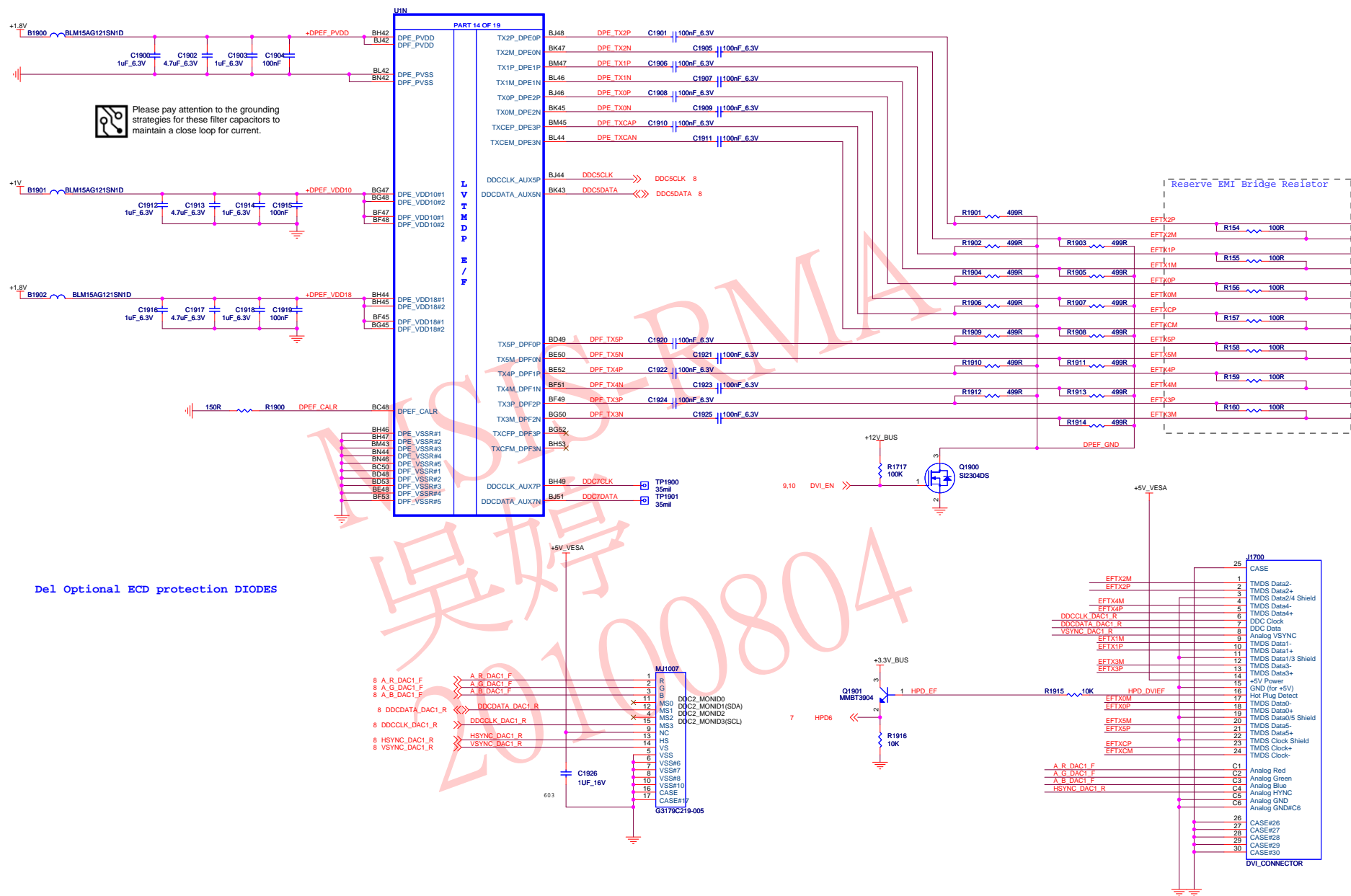
(09) CYPRESS TMD5 A&B



(10) CYPRESS Display Port/HDMI C&D

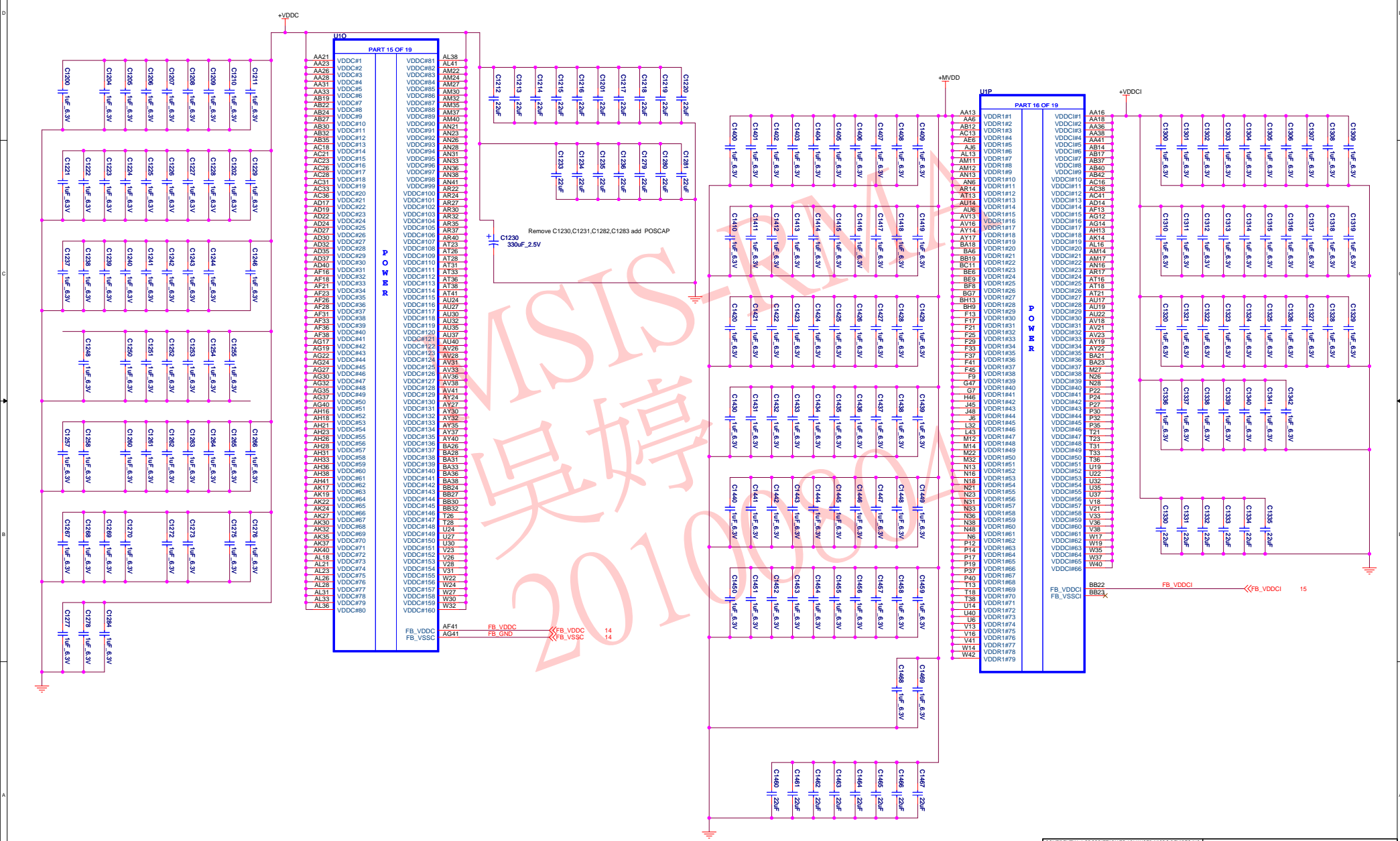


(11) CYPRESS LVTMDP E&F



Del Dual DVI Connector Change to Single DVI

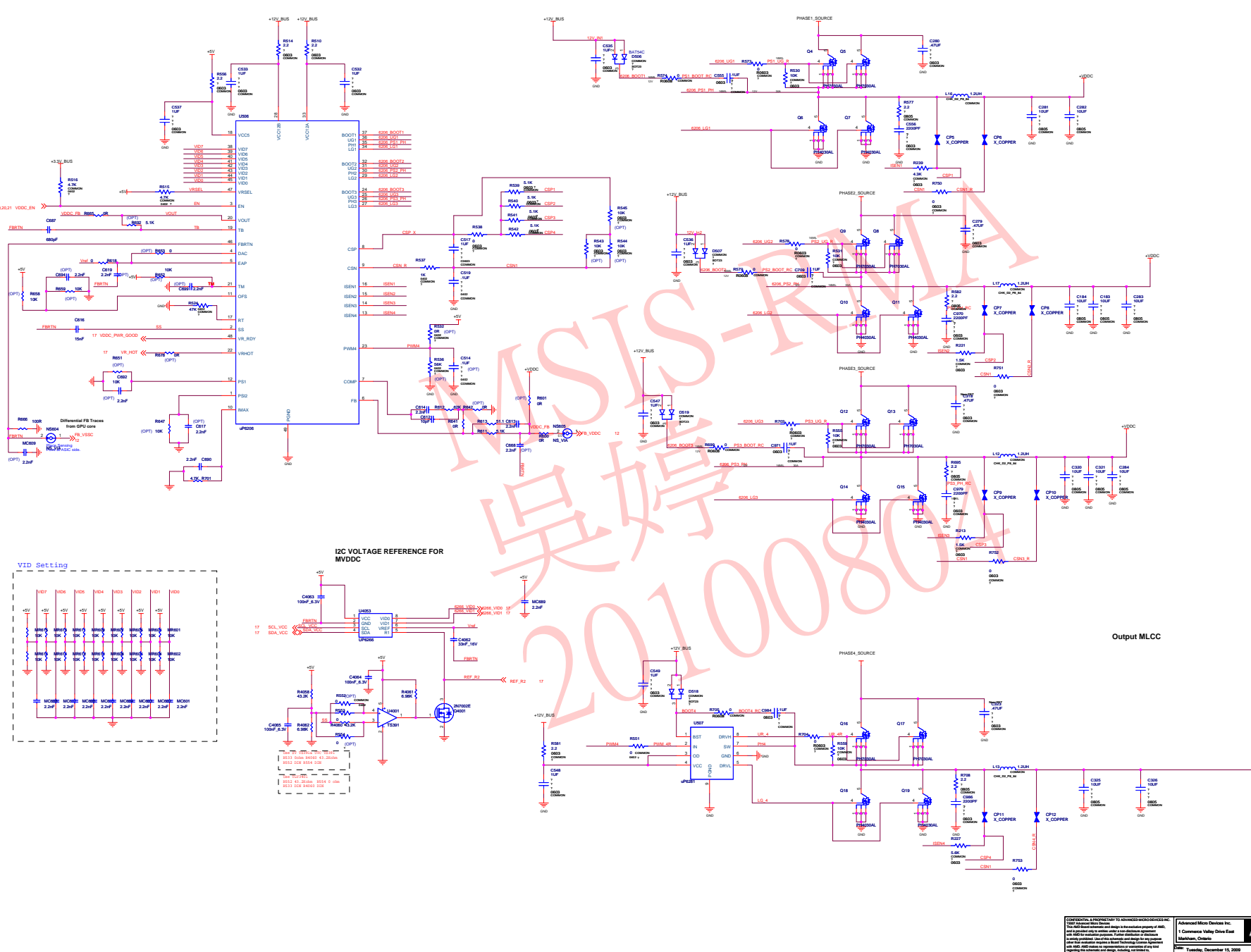
(12) CYPRESS Power



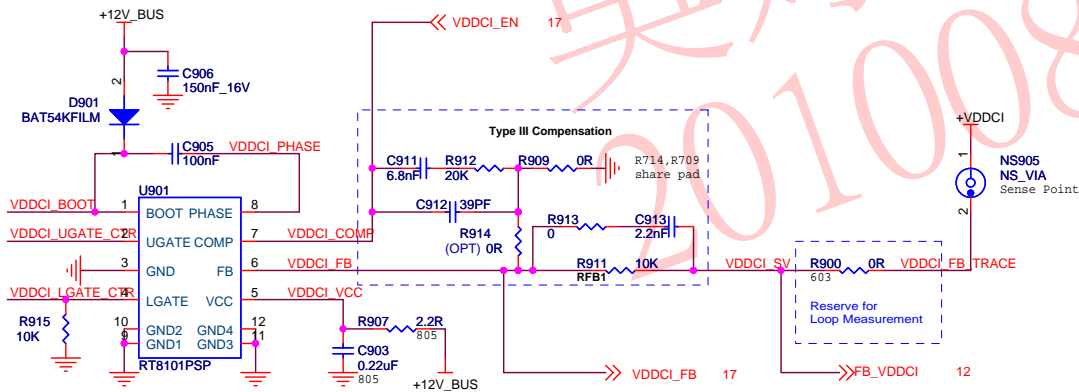
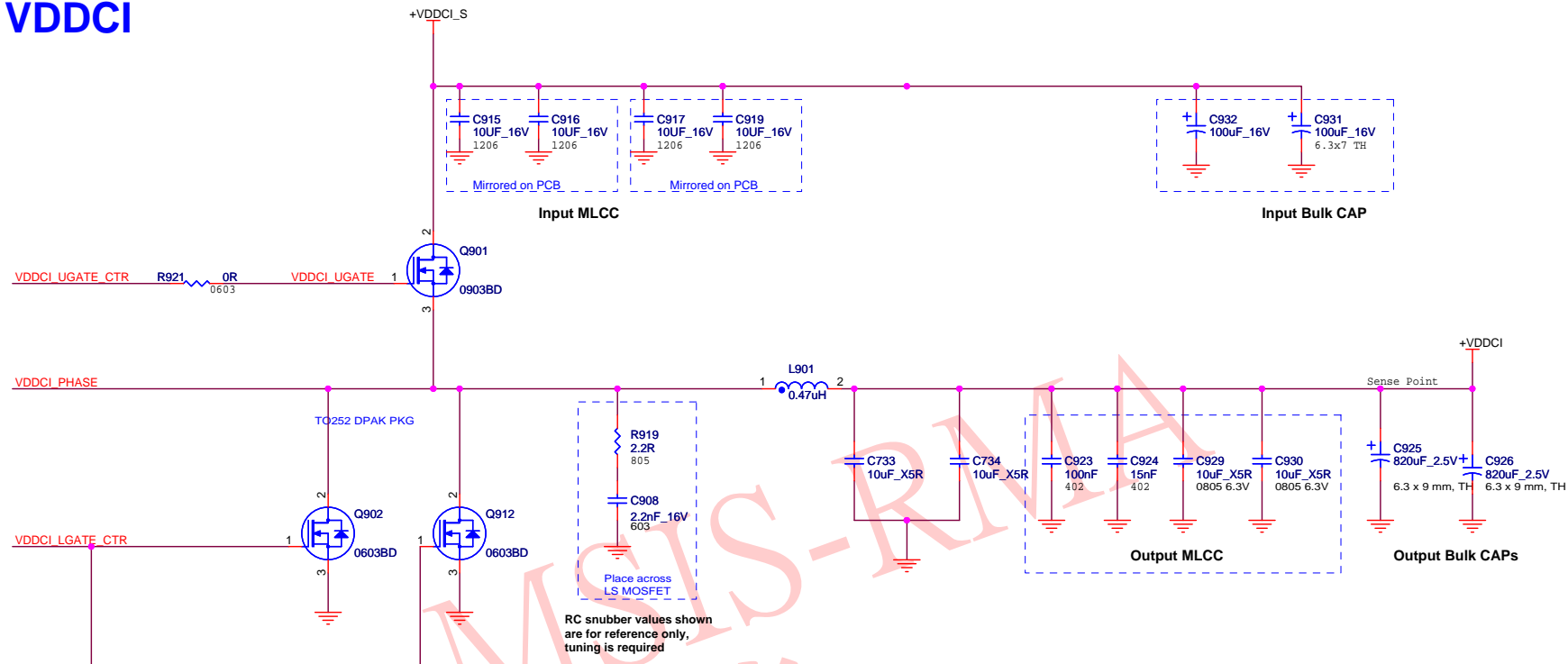
(13) CYPRESS GND

UIC			UIR		
PART 17 OF 19			PART 18 OF 19		
A46	VSS#1	VSS#126	BA17	VSS#251	VSS#376
AA10	VSS#2	VSS#127	BA20	VSS#252	VSS#377
AA14	VSS#3	VSS#128	BA21	VSS#253	VSS#378
AA17	VSS#4	VSS#129	BA22	VSS#254	VSS#379
AA20	VSS#5	VSS#130	BA23	VSS#255	VSS#380
AA22	VSS#6	VSS#131	BA24	VSS#256	VSS#381
AA24	VSS#7	VSS#132	BA25	VSS#257	VSS#382
AA27	VSS#8	VSS#133	BA26	VSS#258	VSS#383
AA30	VSS#9	VSS#134	BA27	VSS#259	VSS#384
AA32	VSS#10	VSS#135	BA28	VSS#260	VSS#385
AA35	VSS#11	VSS#136	BA29	VSS#261	VSS#386
AA37	VSS#12	VSS#137	BA30	VSS#262	VSS#387
AA40	VSS#13	VSS#138	BA31	VSS#263	VSS#388
AA42	VSS#14	VSS#139	BA32	VSS#264	VSS#389
AA45	VSS#15	VSS#140	BA33	VSS#265	VSS#390
AB13	VSS#16	VSS#141	BA34	VSS#266	VSS#391
AB16	VSS#17	VSS#142	BA35	VSS#267	VSS#392
AB18	VSS#18	VSS#143	BA36	VSS#268	VSS#393
AB21	VSS#19	VSS#144	BA37	VSS#269	VSS#394
AB23	VSS#20	VSS#145	BA38	VSS#270	VSS#395
AB26	VSS#21	VSS#146	BA39	VSS#271	VSS#396
AB28	VSS#22	VSS#147	BA40	VSS#272	VSS#397
AB31	VSS#23	VSS#148	BA41	VSS#273	VSS#398
AB33	VSS#24	VSS#149	BA42	VSS#274	VSS#399
AB36	VSS#25	VSS#150	BA43	VSS#275	VSS#400
AB38	VSS#26	VSS#151	BA44	VSS#276	VSS#401
AB41	VSS#27	VSS#152	BA45	VSS#277	VSS#402
AB43	VSS#28	VSS#153	BA46	VSS#278	VSS#403
AC10	VSS#29	VSS#154	BA47	VSS#279	VSS#404
AC14	VSS#30	VSS#155	BA48	VSS#280	VSS#405
AC17	VSS#31	VSS#156	BA49	VSS#281	VSS#406
AC19	VSS#32	VSS#157	BA50	VSS#282	VSS#407
AC2	VSS#33	VSS#158	BA51	VSS#283	VSS#408
AC22	VSS#34	VSS#159	BA52	VSS#284	VSS#409
AC24	VSS#35	VSS#160	BA53	VSS#285	VSS#410
AC27	VSS#36	VSS#161	BA54	VSS#286	VSS#411
AC30	VSS#37	VSS#162	BA55	VSS#287	VSS#412
AC32	VSS#38	VSS#163	BA56	VSS#288	VSS#413
AC35	VSS#39	VSS#164	BA57	VSS#289	VSS#414
AC37	VSS#40	VSS#165	BA58	VSS#290	VSS#415
AC40	VSS#41	VSS#166	BA59	VSS#291	VSS#416
AC42	VSS#42	VSS#167	BA60	VSS#292	VSS#417
AC6	VSS#43	VSS#168	BA61	VSS#293	VSS#418
AD13	VSS#44	VSS#169	BA62	VSS#294	VSS#419
AD16	VSS#45	VSS#170	BA63	VSS#295	VSS#420
AD18	VSS#46	VSS#171	BA64	VSS#296	VSS#421
AD21	VSS#47	VSS#172	BA65	VSS#297	VSS#422
AD23	VSS#48	VSS#173	BA66	VSS#298	VSS#423
AD26	VSS#49	VSS#174	BA67	VSS#299	VSS#424
AD28	VSS#50	VSS#175	BA68	VSS#300	VSS#425
AD31	VSS#51	VSS#176	BA69	VSS#301	VSS#426
AD33	VSS#52	VSS#177	BA70	VSS#302	VSS#427
AD36	VSS#53	VSS#178	BA71	VSS#303	VSS#428
AD38	VSS#54	VSS#179	BA72	VSS#304	VSS#429
AD41	VSS#55	VSS#180	BA73	VSS#305	VSS#430
AD43	VSS#56	VSS#181	BA74	VSS#306	VSS#431
AE2	VSS#57	VSS#182	BA75	VSS#307	VSS#432
AE5	VSS#58	VSS#183	BA76	VSS#308	VSS#433
AF10	VSS#59	VSS#184	BA77	VSS#309	VSS#434
AF14	VSS#60	VSS#185	BA78	VSS#310	VSS#435
AF17	VSS#61	VSS#186	BA79	VSS#311	VSS#436
AF19	VSS#62	VSS#187	BA80	VSS#312	VSS#437
AF22	VSS#63	VSS#188	BA81	VSS#313	VSS#438
AF24	VSS#64	VSS#189	BA82	VSS#314	VSS#439
AF27	VSS#65	VSS#190	BA83	VSS#315	VSS#440
AF30	VSS#66	VSS#191	BA84	VSS#316	VSS#441
AF32	VSS#67	VSS#192	BA85	VSS#317	VSS#442
AF35	VSS#68	VSS#193	BA86	VSS#318	VSS#443
AF37	VSS#69	VSS#194	BA87	VSS#319	VSS#444
AF40	VSS#70	VSS#195	BA88	VSS#320	VSS#445
AG13	VSS#71	VSS#196	BA89	VSS#321	VSS#446
AG16	VSS#72	VSS#197	BA90	VSS#322	VSS#447
AG18	VSS#73	VSS#198	BA91	VSS#323	VSS#448
AG2	VSS#74	VSS#199	BA92	VSS#324	VSS#449
AG21	VSS#75	VSS#200	BA93	VSS#325	VSS#450
AG23	VSS#76	VSS#201	BA94	VSS#326	VSS#451
AG26	VSS#77	VSS#202	BA95	VSS#327	VSS#452
AG28	VSS#78	VSS#203	BA96	VSS#328	VSS#453
AG31	VSS#79	VSS#204	BA97	VSS#329	VSS#454
AG33	VSS#80	VSS#205	BA98	VSS#330	VSS#455
AG36	VSS#81	VSS#206	BA99	VSS#331	VSS#456
AG38	VSS#82	VSS#207	BA100	VSS#332	VSS#457
AG6	VSS#83	VSS#208	BA101	VSS#333	VSS#458
AH10	VSS#84	VSS#209	BA102	VSS#334	VSS#459
AH17	VSS#85	VSS#210	BA103	VSS#335	VSS#460
AH19	VSS#86	VSS#211	BA104	VSS#336	VSS#461
AH22	VSS#87	VSS#212	BA105	VSS#337	VSS#462
AH24	VSS#88	VSS#213	BA106	VSS#338	VSS#463
AH27	VSS#89	VSS#214	BA107	VSS#339	VSS#464
AH30	VSS#90	VSS#215	BA108	VSS#340	VSS#465
AH32	VSS#91	VSS#216	BA109	VSS#341	VSS#466
AH35	VSS#92	VSS#217	BA110	VSS#342	VSS#467
AH37	VSS#93	VSS#218	BA111	VSS#343	VSS#468
AH40	VSS#94	VSS#219	BA112	VSS#344	VSS#469
AH43	VSS#95	VSS#220	BA113	VSS#345	VSS#470
AH45	VSS#96	VSS#221	BA114	VSS#346	VSS#471
AJ2	VSS#97	VSS#222	BA115	VSS#347	VSS#472
AJ7	VSS#98	VSS#223	BA116	VSS#348	VSS#473
AK13	VSS#99	VSS#224	BA117	VSS#349	VSS#474
AK16	VSS#100	VSS#225	BA118	VSS#350	VSS#475
AK18	VSS#101	VSS#226	BA119	VSS#351	VSS#476
AK21	VSS#102	VSS#227	BA120	VSS#352	VSS#477
AK23	VSS#103	VSS#228	BA121	VSS#353	VSS#478
AK26	VSS#104	VSS#229	BA122	VSS#354	VSS#479
AK31	VSS#105	VSS#230	BA123	VSS#355	VSS#480
AK33	VSS#106	VSS#231	BA124	VSS#356	VSS#481
AK36	VSS#107	VSS#232	BA125	VSS#357	VSS#482
AK38	VSS#108	VSS#233	BA126	VSS#358	VSS#483
AK40	VSS#109	VSS#234	BA127	VSS#359	VSS#484
AL1	VSS#110	VSS#235	BA128	VSS#360	VSS#485
AL14	VSS#111	VSS#236	BA129	VSS#361	VSS#486
AL17	VSS#112	VSS#237	BA130	VSS#362	VSS#487
AL19	VSS#113	VSS#238	BA131	VSS#363	VSS#488
AL2	VSS#114	VSS#239	BA132	VSS#364	VSS#489
AL22	VSS#115	VSS#240	BA133	VSS#365	VSS#490
AL24	VSS#116	VSS#241	BA134	VSS#366	VSS#491
AL27	VSS#117	VSS#242	BA135	VSS#367	VSS#492
AL30	VSS#118	VSS#243	BA136	VSS#368	VSS#493
AL32	VSS#119	VSS#244	BA137	VSS#369	VSS#494
AL35	VSS#120	VSS#245	BA138	VSS#370	VSS#495
AL37	VSS#121	VSS#246	BA139	VSS#371	VSS#496
AL40	VSS#122	VSS#247	BA140	VSS#372	VSS#497
AL6	VSS#123	VSS#248	BA141	VSS#373	VSS#498
AL9	VSS#124	VSS#249	BA142	VSS#374	VSS#499
AL9	VSS#125	VSS#250	BA143	VSS#375	VSS#500

(14) VDDC



(15) VDDCI



CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.
©2007 Advanced Micro Devices
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

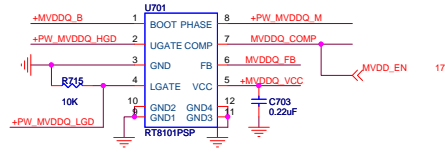


Date: Tuesday, December 15, 2009
Rev 2
Sheet 15 of 23

Title VDDCI Doc No. 105-C008XX-00C

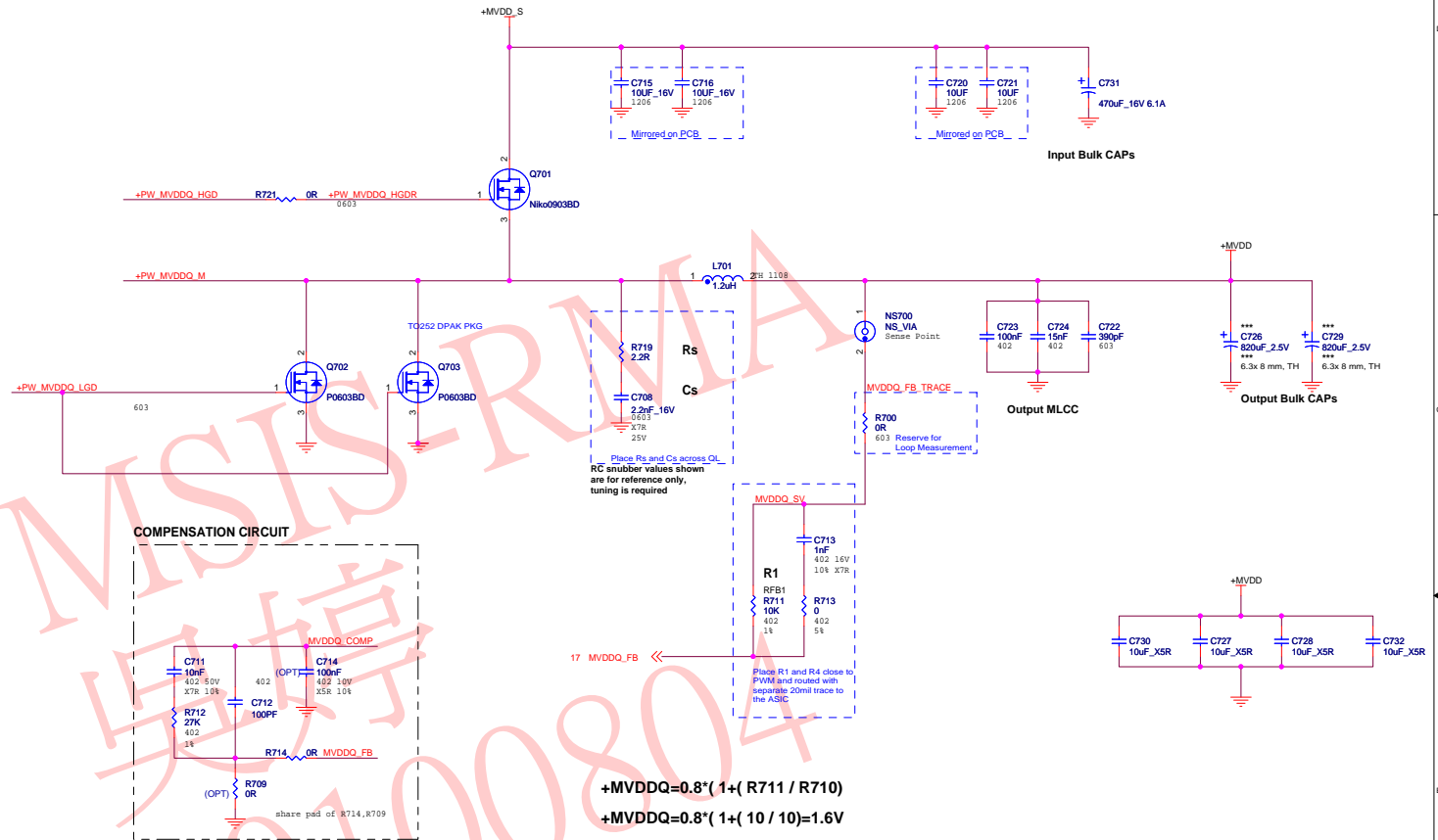


(16) MVDDQ

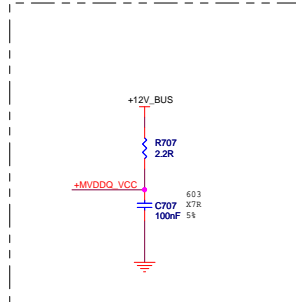


Layout guideline

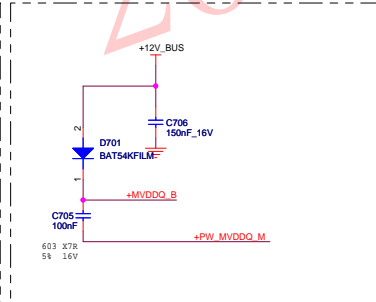
- 1-Position the controller (U703) such that LGate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces (PW_MVDDQ_LGD and PW_MVDDQ_HGD) as short and as wide as possible to reduce the trace inductance.
- 2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows:
Vcc bypass cap is C703, and Boost cap is C705.
- 3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and C712.



FILTERED SMPS VCC



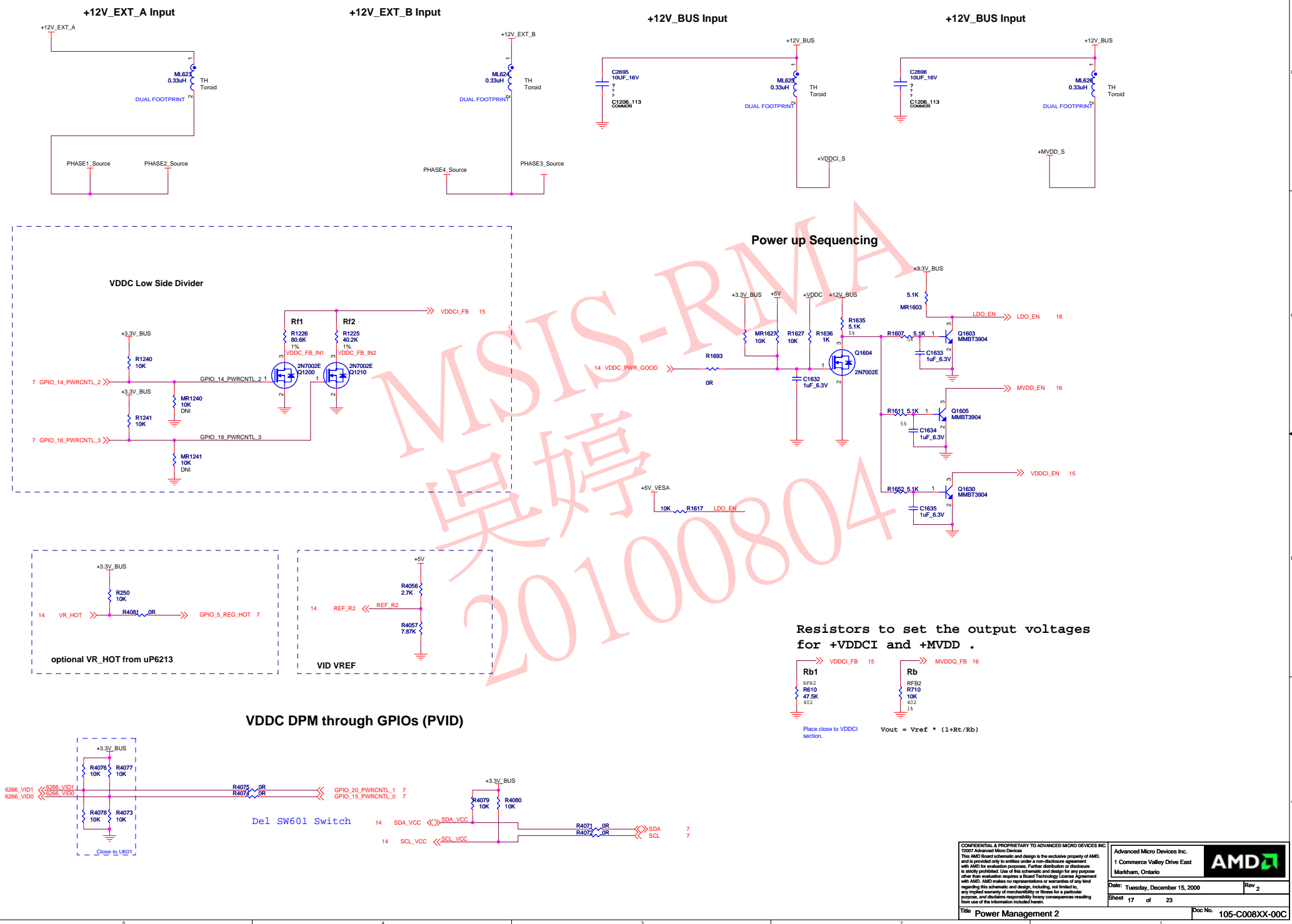
BOOT CIRCUIT



CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.
7207 Advanced Micro Devices
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

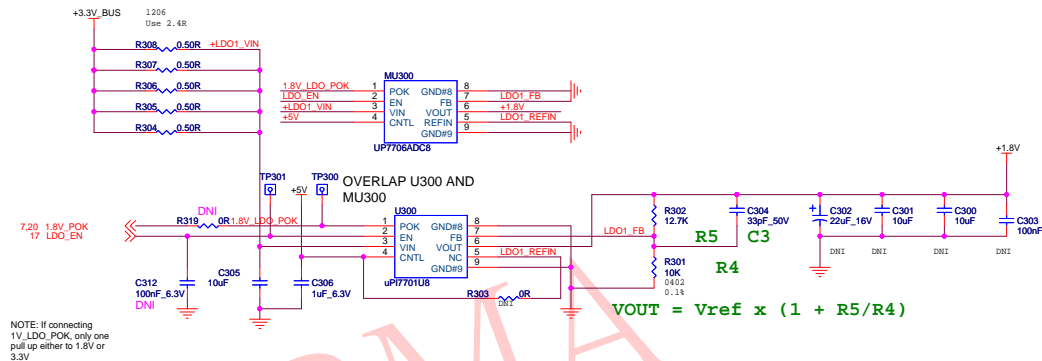
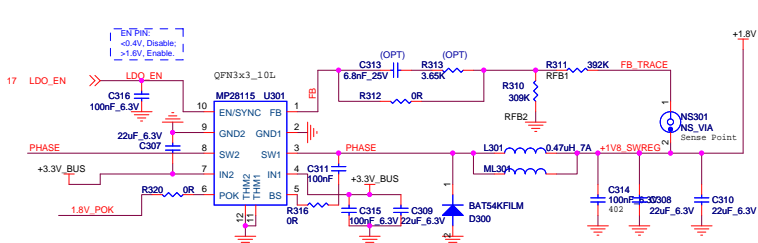
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario
Date: Tuesday, December 15, 2009
Sheet 16 of 23
Rev 2
Doc No. 105-C008XX-00C

(17) CYPRESS VDDCI POWER PLAY



(18) CYPRESS Small Rail Regulators

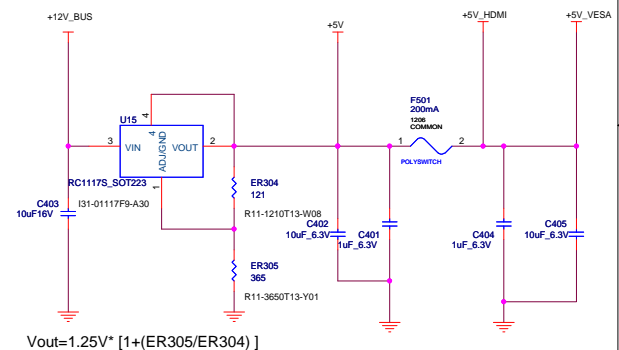
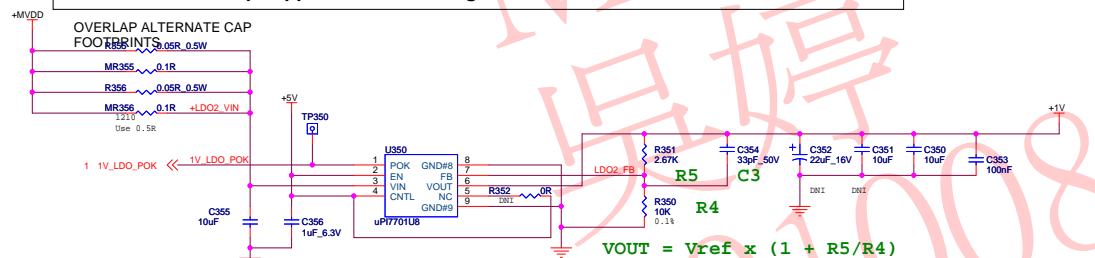
LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



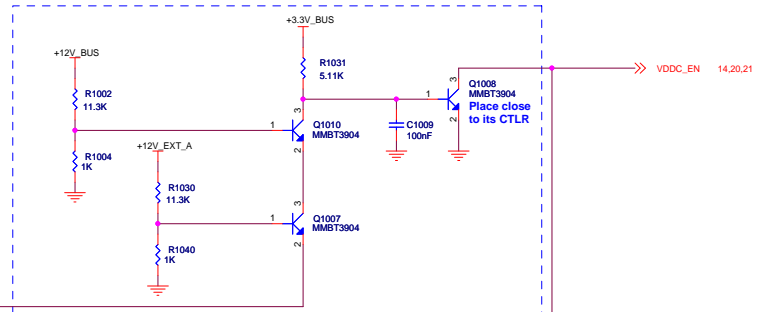
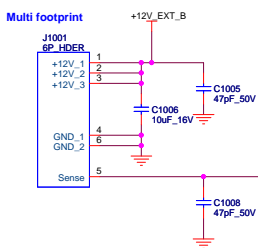
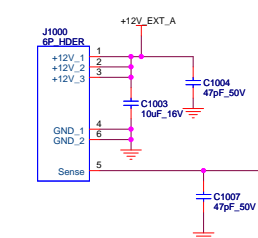
NOTE: If connecting 1V_LDO_POK, only one pull up either to 1.8V or 3.3V

optional 5V power for VDDC regulator;

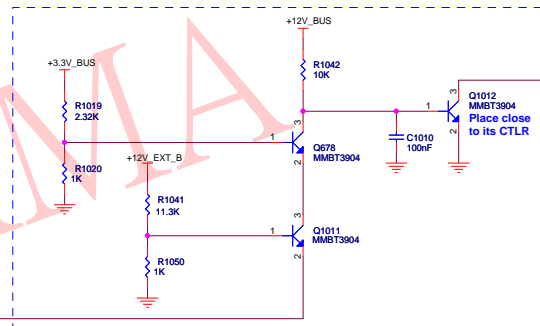
LDO #2: Vin = +1.35V to 1.8VMAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



(19) CYPRESS POWER MGMNT



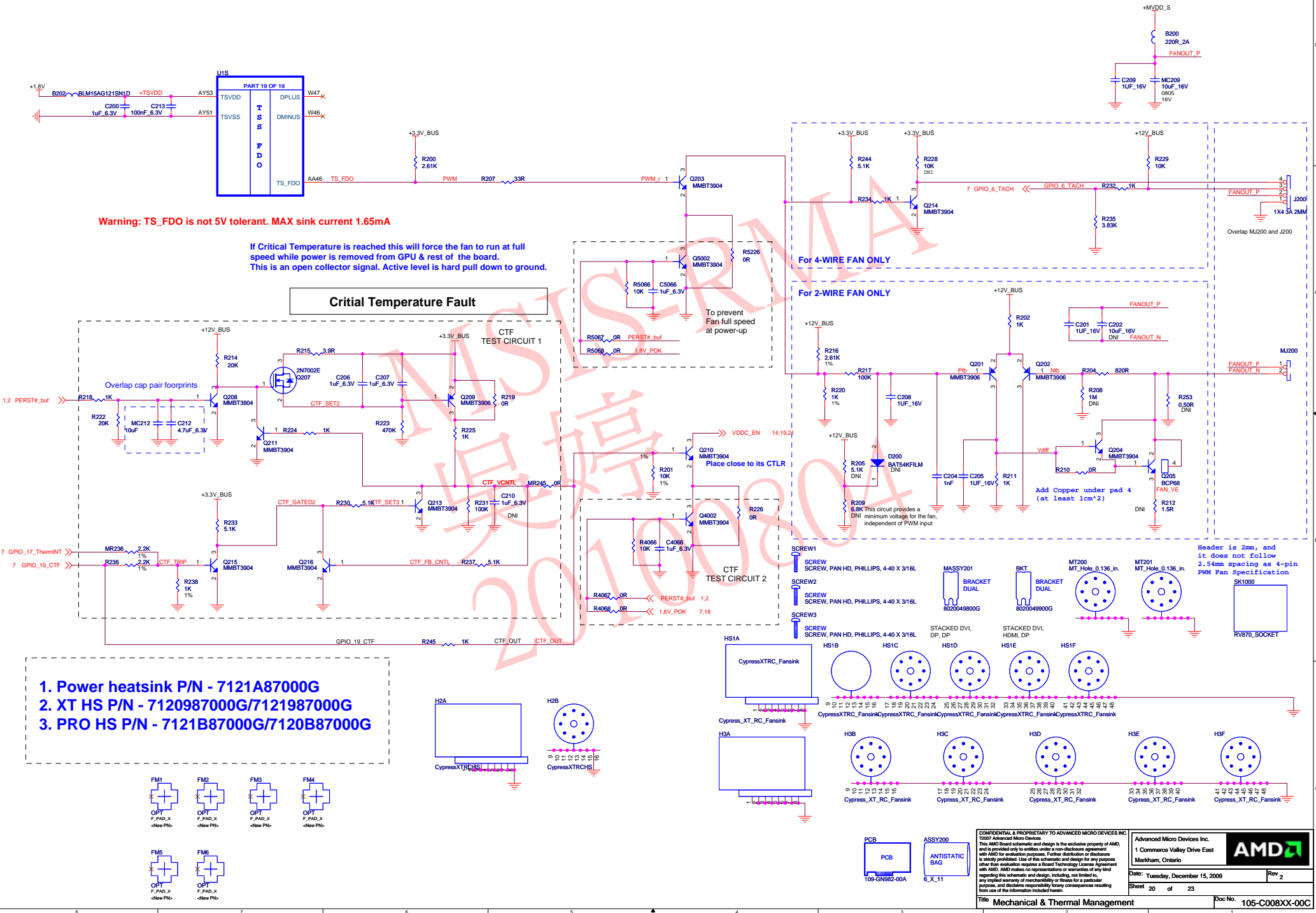
BUS 12V and AUX A Power up Seq



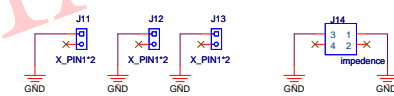
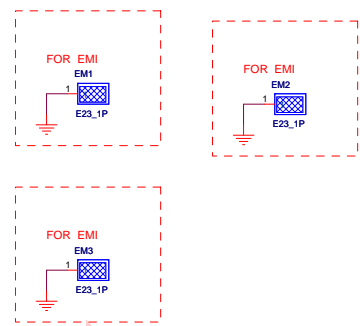
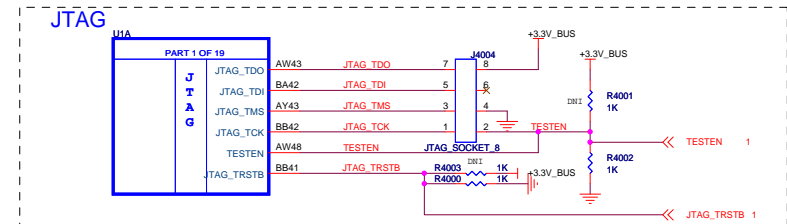
BUS 3.3V and AUX B Power up Seq

MSIS-RMA
吳婷
20100804

(20) CYPRESS Mechanical and Thermal Management

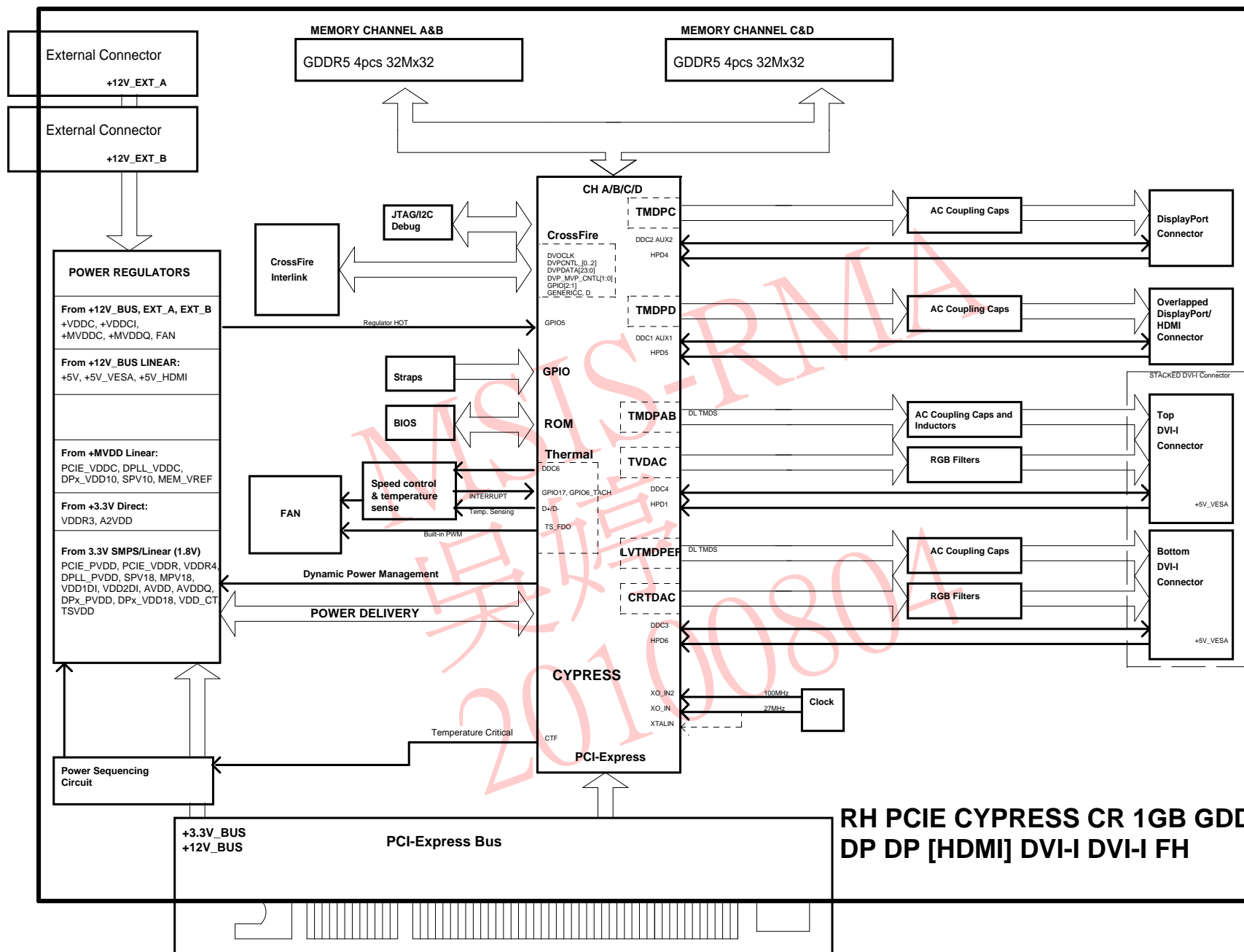


(21) CYPRESS Debug Circuits



Del PTC protect circuit.

MSIS-RMA
吳婷
20100804



**RH PCIE CYPRESS CR 1GB GDDR5
DP DP [HDMI] DVI-I DVI-I FH**



Title			Schematic No.	Date:
RH CYPRESS GDDR5 DP-HDMI-DVII-DVII			105-C008XX-00C	Tuesday, December 15, 2009
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.	
			Rev	2
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION	
0	00A	09/08/11		
1	00B	09/08/26		
2	00C	09/09/24	Initial release. Based on CYpress XT C001 00 PCB	
V209-0A		09/10/12	Based on CYpress XT C008 0C PCB 1. Page 7 Change U2 SL16010DCT to Uc1006 and Co-lay Uc1008 with U12 SL16010DCT 2. Page 8 Del DAC2 RGB 3. Page 9 Disable TMDP AB and disable DDC_AUX3,DDC_AUX4 4. Page 10 Del DP co-lay with HDMI 5. Page 11 Del Dual DVI Connector Change to Single DVI and Co-lay Slim D-Sub 6. Page 12 Remove C1230,C1231,C1282,C1283 add POSCAP 7. Page 14 Change VDDC PWM to Upi6206 8. Page 18 Change +5V circuit. 9. Page 21 Del PTC protect circuit. 10. Page3,4 changing the DRAM reset circuit 11. Page10 chang HDMI DDC to DDC3 12. Page 14 co-lay U4001 with TLV3401	
		09/11/2		

MSIS-RMA
吳婷
20100804