

PG180A02

256b GDDR6x16

TALL DP + DP + DP + HDMI DP + USB

TABLE OF CONTENTS

Page Description

Page Description

Page Description

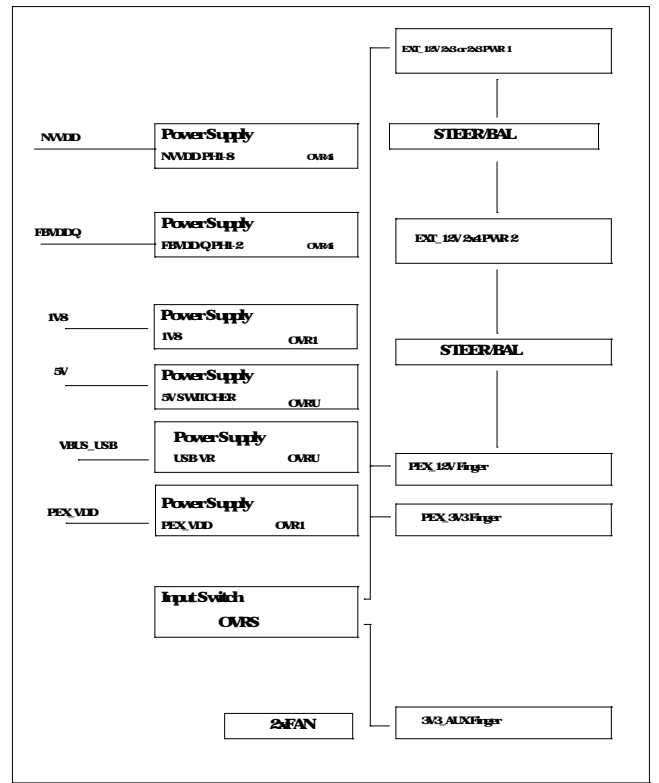
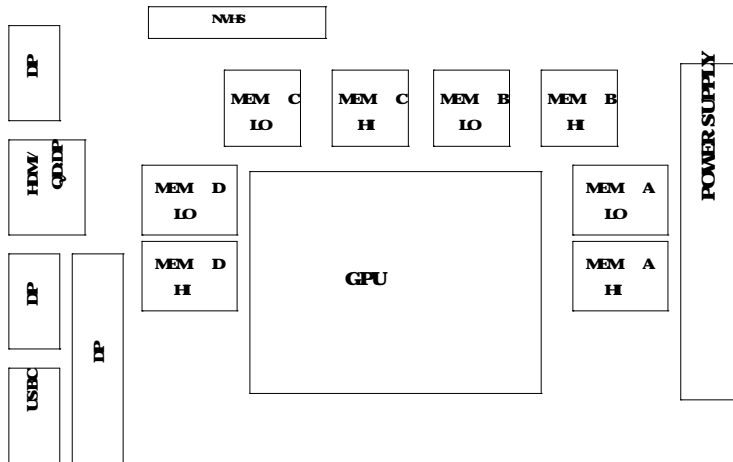
1 Table of Contents
2 Block Diagram
3 PCI Express
4 PCI Termination
5 MEMORY: GPU Partition A/B
6 MEMORY: FBA Partition 3L0
7 MEMORY: FBA Partition 3L32
8 MEMORY: FBA Partition 3L0
9 MEMORY: FBA Partition 3L32
10 MEMORY: GPU Partition C/D
11 MEMORY: FBC Partition 3L0
12 MEMORY: FBC Partition 3L32
13 MEMORY: FBD Partition 3L0
14 MEMORY: FBD Partition 3L32
15 GPU PAR and GND
16 GPU Decoupling
17 GPU DECOUPLING
18 EPAB TALL DP
19 EPB DP
20 EPF USB C
21 EPF HDMI 2.0 DP
22 EPD DP
23 N/A S INTERFACE
24 MISC: FAN THERMAL, JTAG, GPIO, STEREO
25 MISC: ROM STRAPS
26 MISC: XTAL, PLL
27 MISC: USB PPC
28 PS: USB VR
29 PS: 5V, 5V BACKUP
30 PS: PEX/DD I/VS
31 PS: FB/MD CONTROLLER
32 PS: FB/MD CONTROLLER OVR3
33 PS: FB/MD PHASE 1, 2
34 PS: N/A/MD CONTROLLER OVR3
35 PS: N/A/MD Phase 1, 2
36 PS: N/A/MD Phase 3, 4
37 PS: N/A/MD Phase 5, 6
38 PS: N/A/MD Phase 7, 8
39 PS: INPUT SWITCH R/D3
40 PS: INPUT SWITCH R/D3 USB

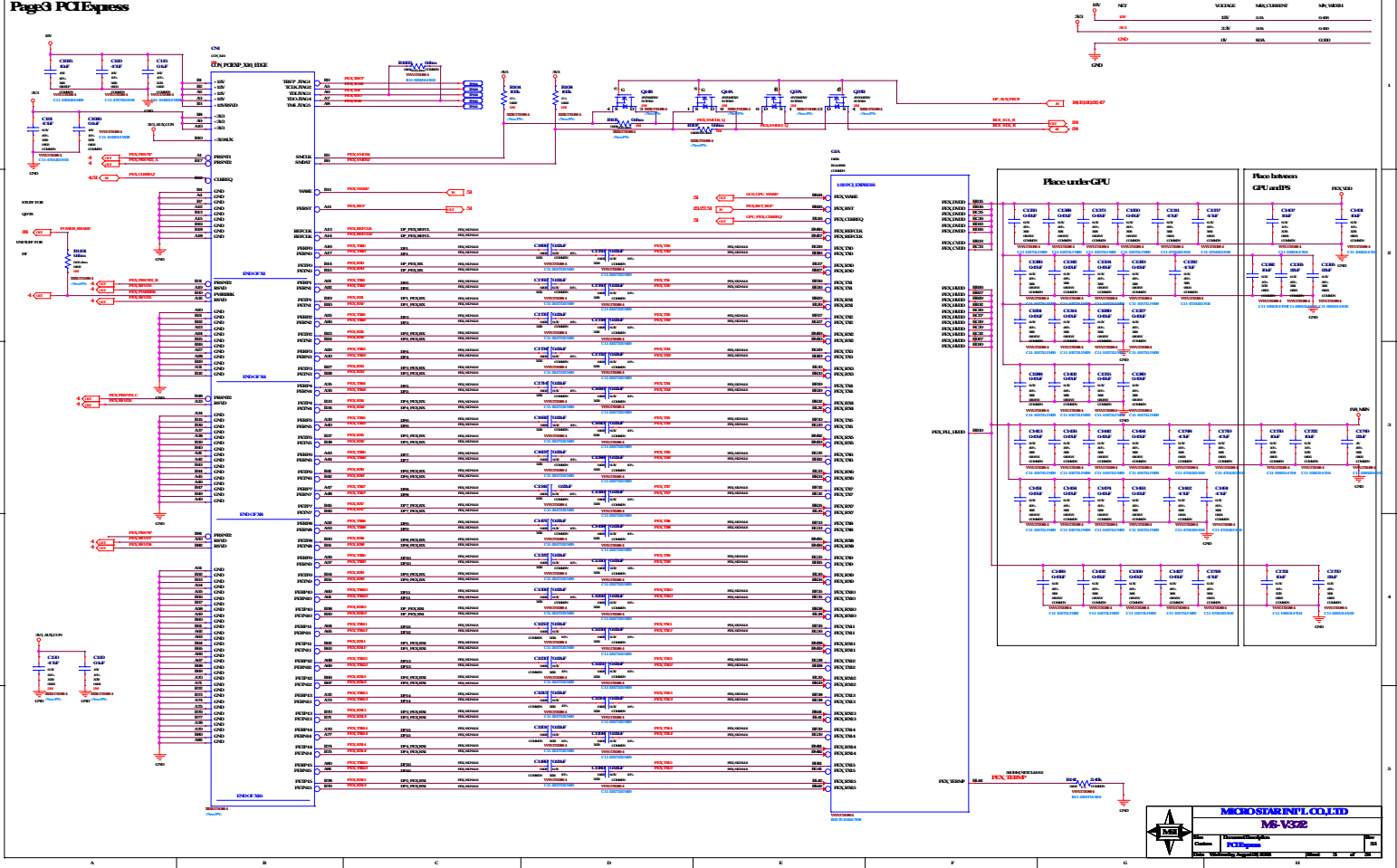
41 PS: INPUT SWITCH RAIL BALANCE
42 PS: 12V CURRENT STEERING
43 PS: VR THERMAL PROTECTION
44 PS: INPUTS, FILTERING AND MONITORING
45 PS: CURRENT STEERING, HOT UNPLUG DETECT
46 PS: PRE FILTER
47 SEQUENCE: 5V, I/VS, N/A/3, 3/ENABLE
48 SEQUENCE: NV, PEX, FB/ENABLE
49 SEQUENCE: PCIE VOLTAGE MONITOR
50 SEQUENCE: DISCHARGE
51 SEQUENCE: MISC
52 LED & FAN HEADERS
53 LED 2
54 Mechanical Bracket/Thermal Solution

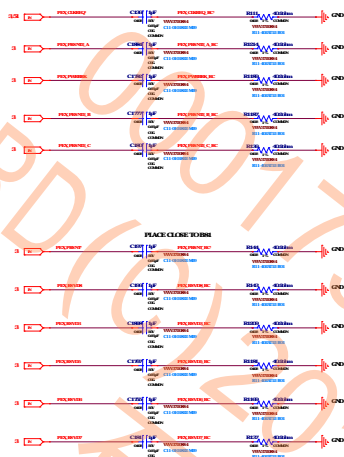
V32230 Change List
18 Change J46 footprint
19 Change J36 footprint
20 Remove DP coil put
21 Remove JTAG & unused GPIO
32 Remove OVB, PS, FB/MD CONTROLLER OVR3
34 N/A/MD CONTROLLER change to MP2888A
35 DRMC5 change to IQ phases
36 DRMC5 change to IQ phases
37 Add N/A/MD Output CAP
41 Remove INPUT SWITCH RAIL Balance
44 JS change to Spin
Add Fuse F1-F3
Change 12V input chicle footprint
45 Add Hot Unplug Detect for JS
52 Add Remove LED & Fan Via 12V qpin
53 Add MCU IIS256 for RGB LED

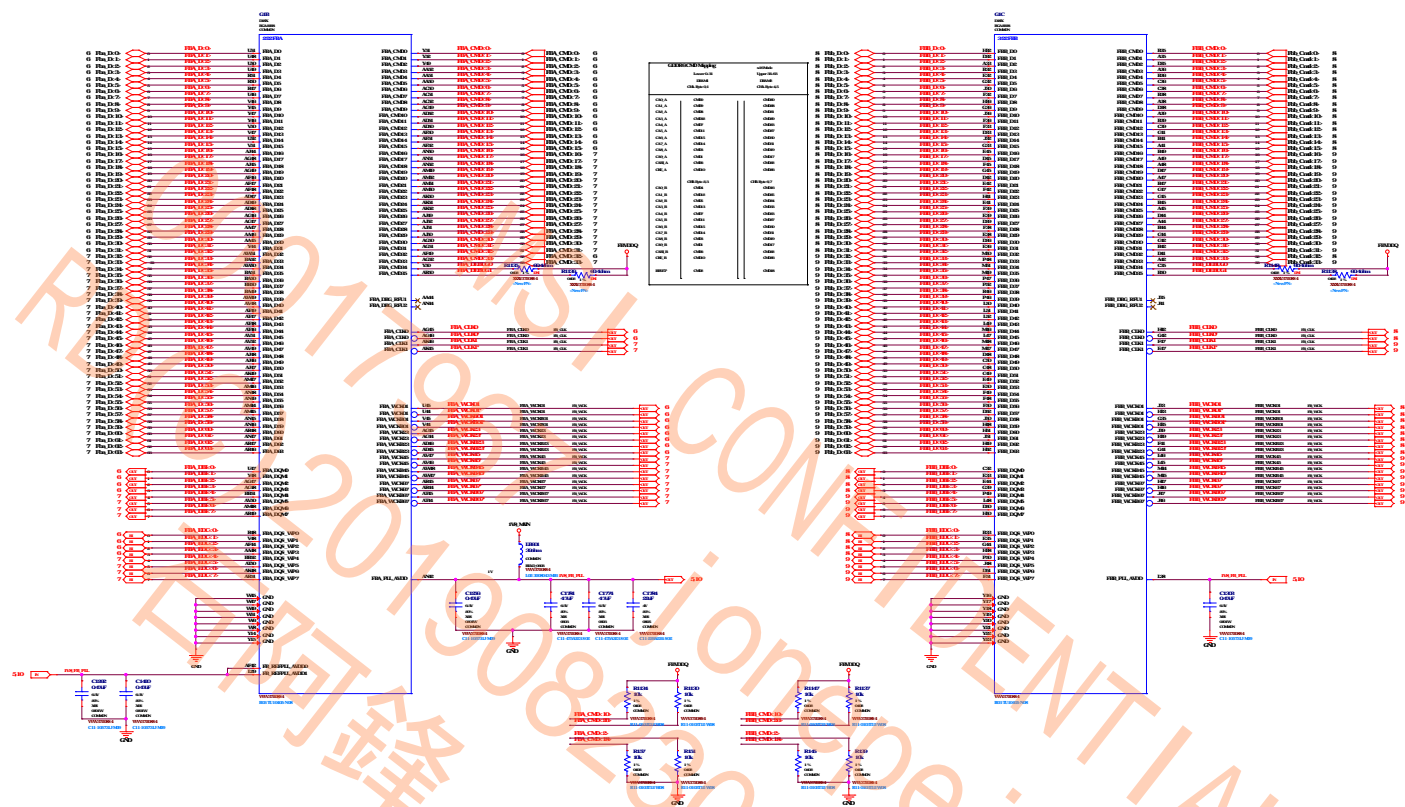
V32231 Change List
Base on V32230 No changed

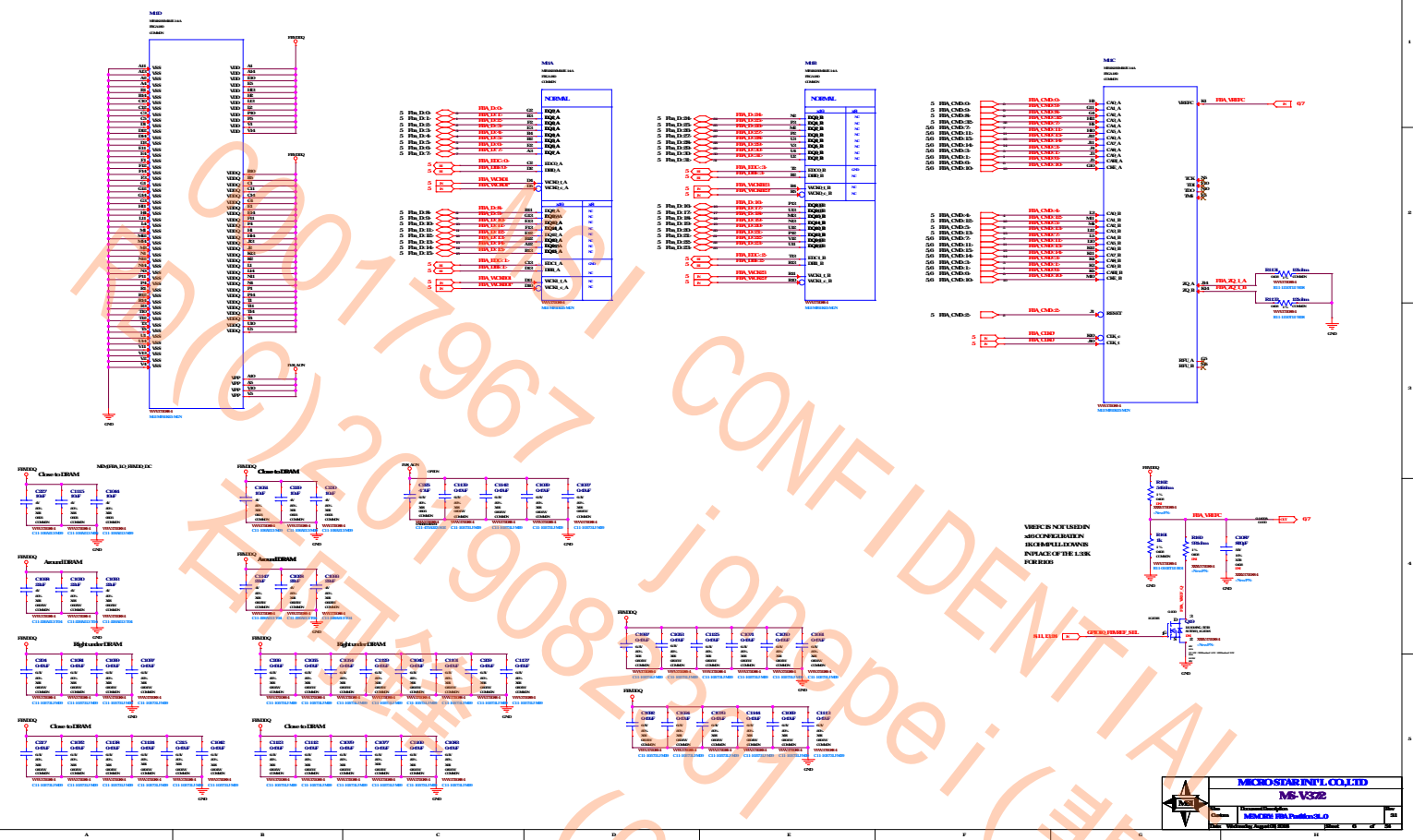


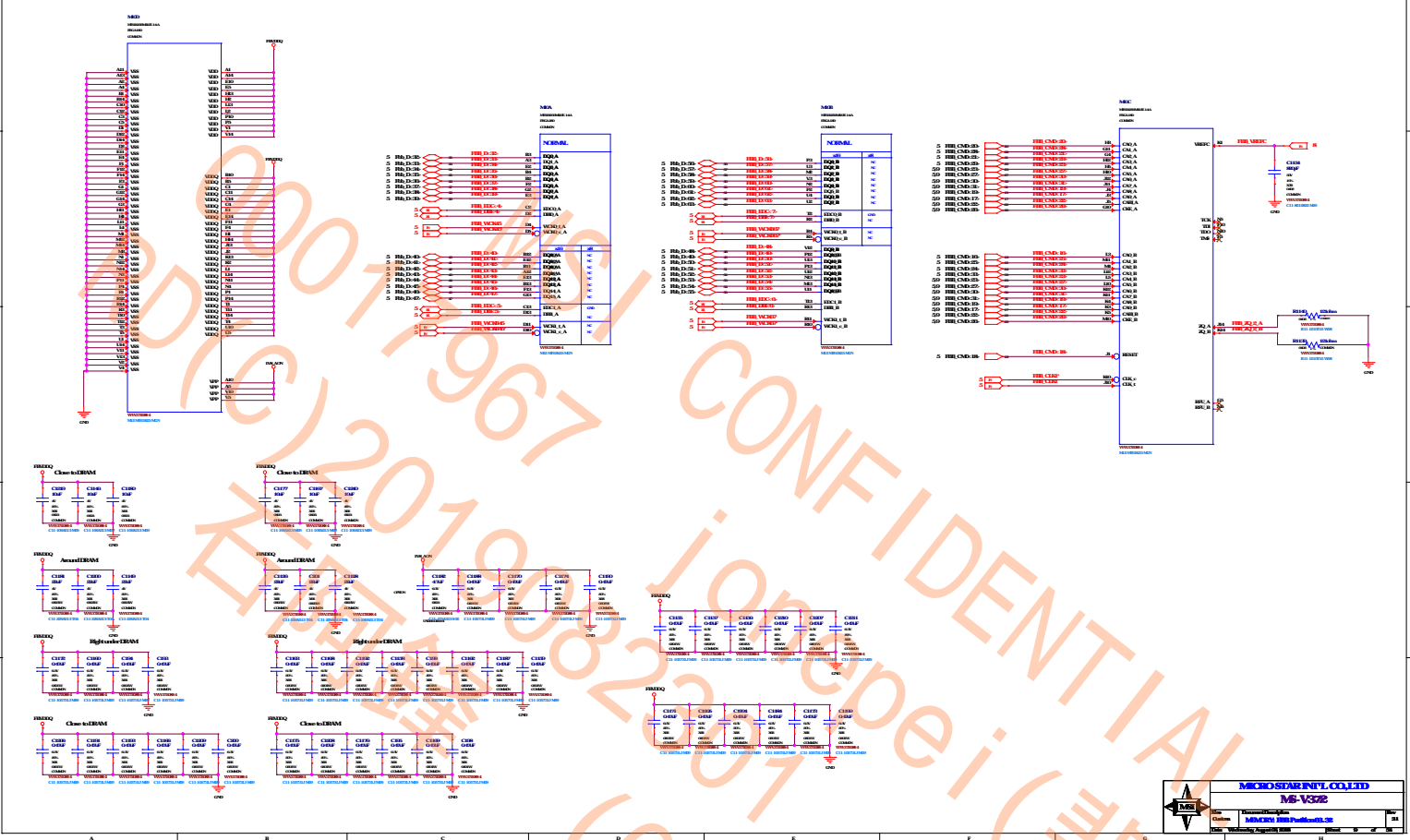


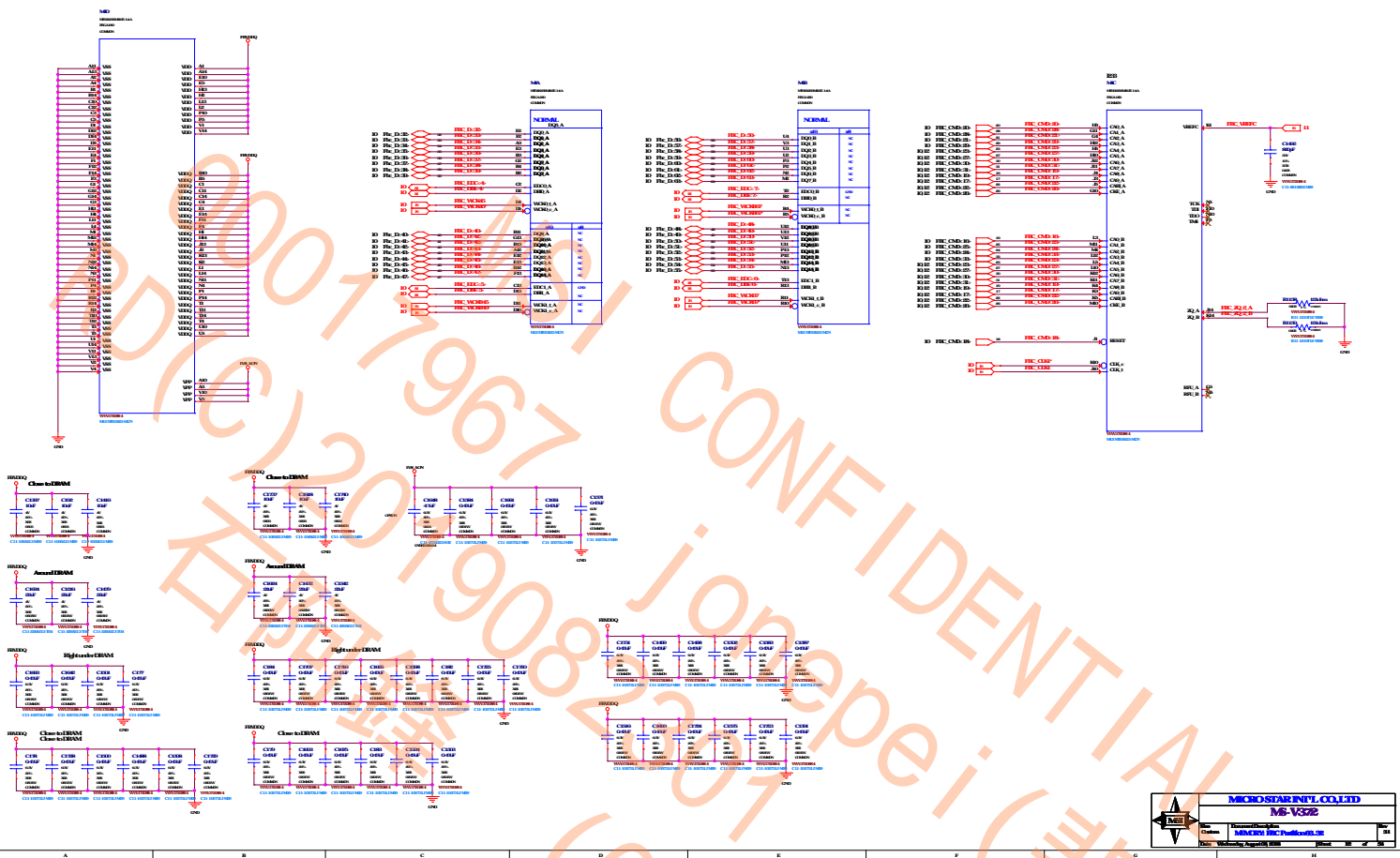


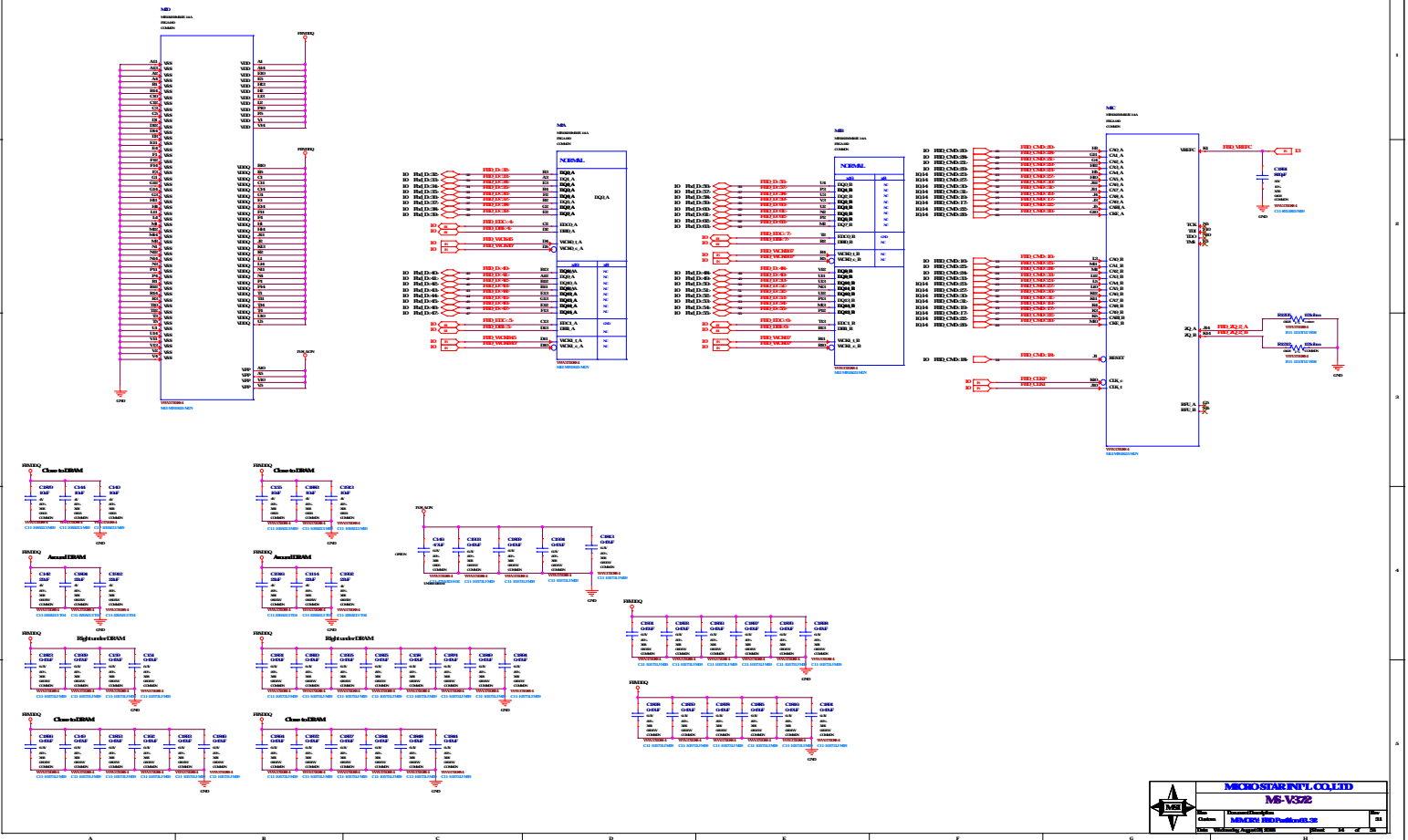


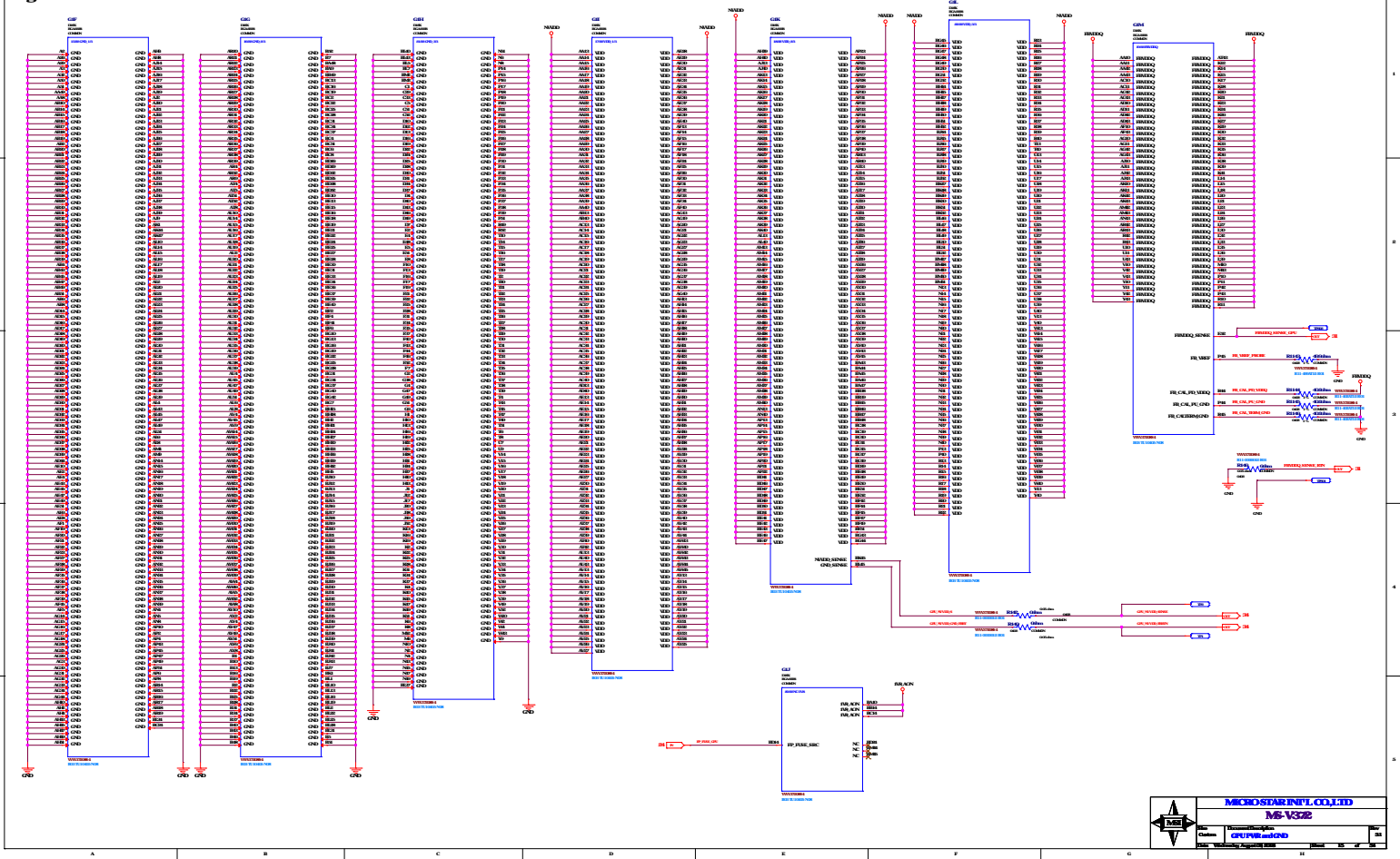


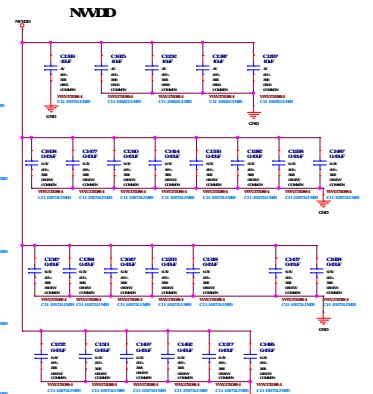
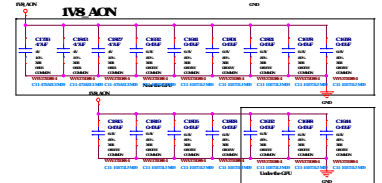
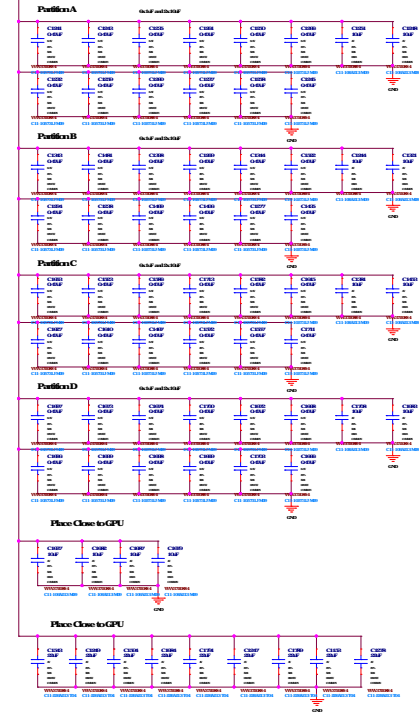




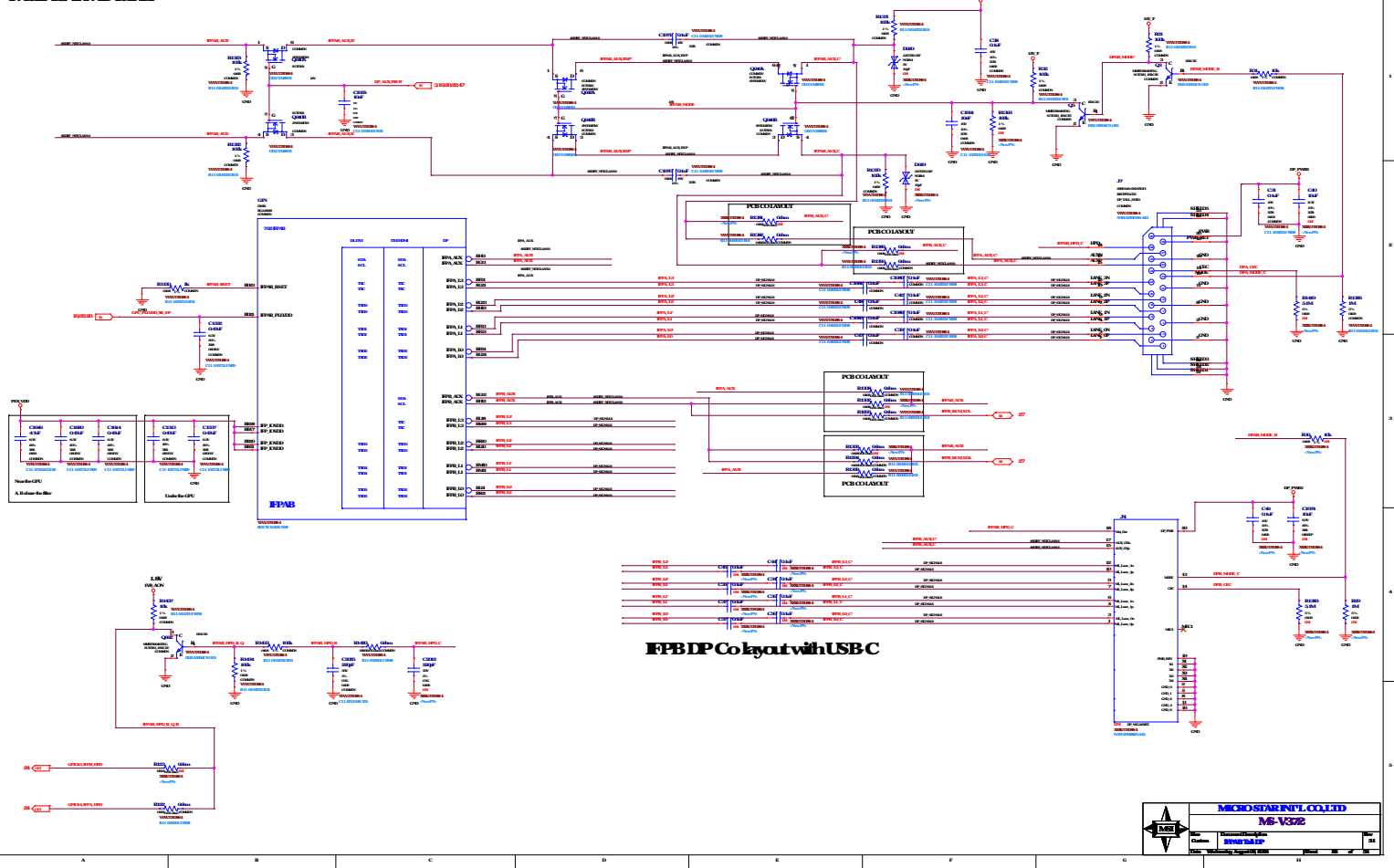


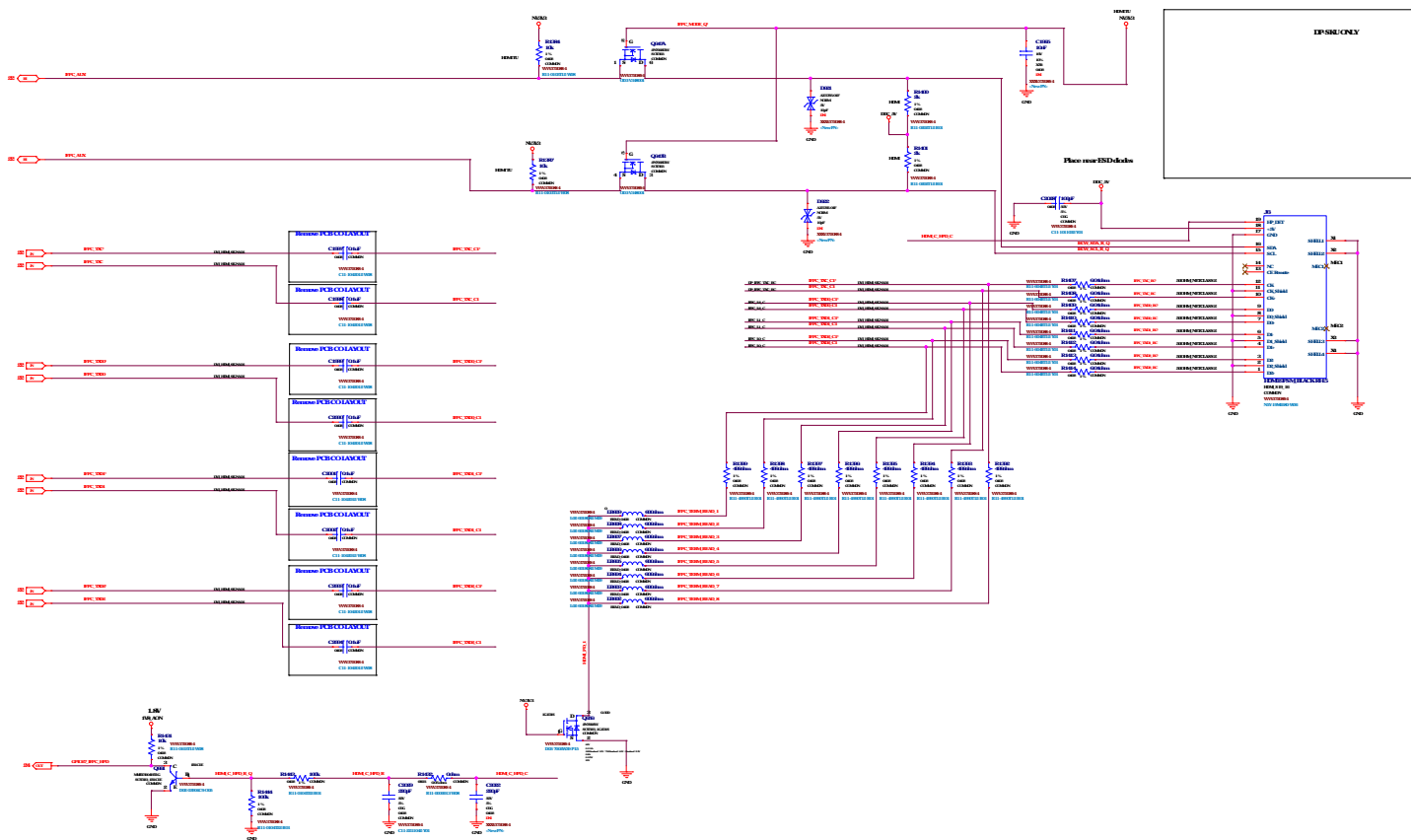


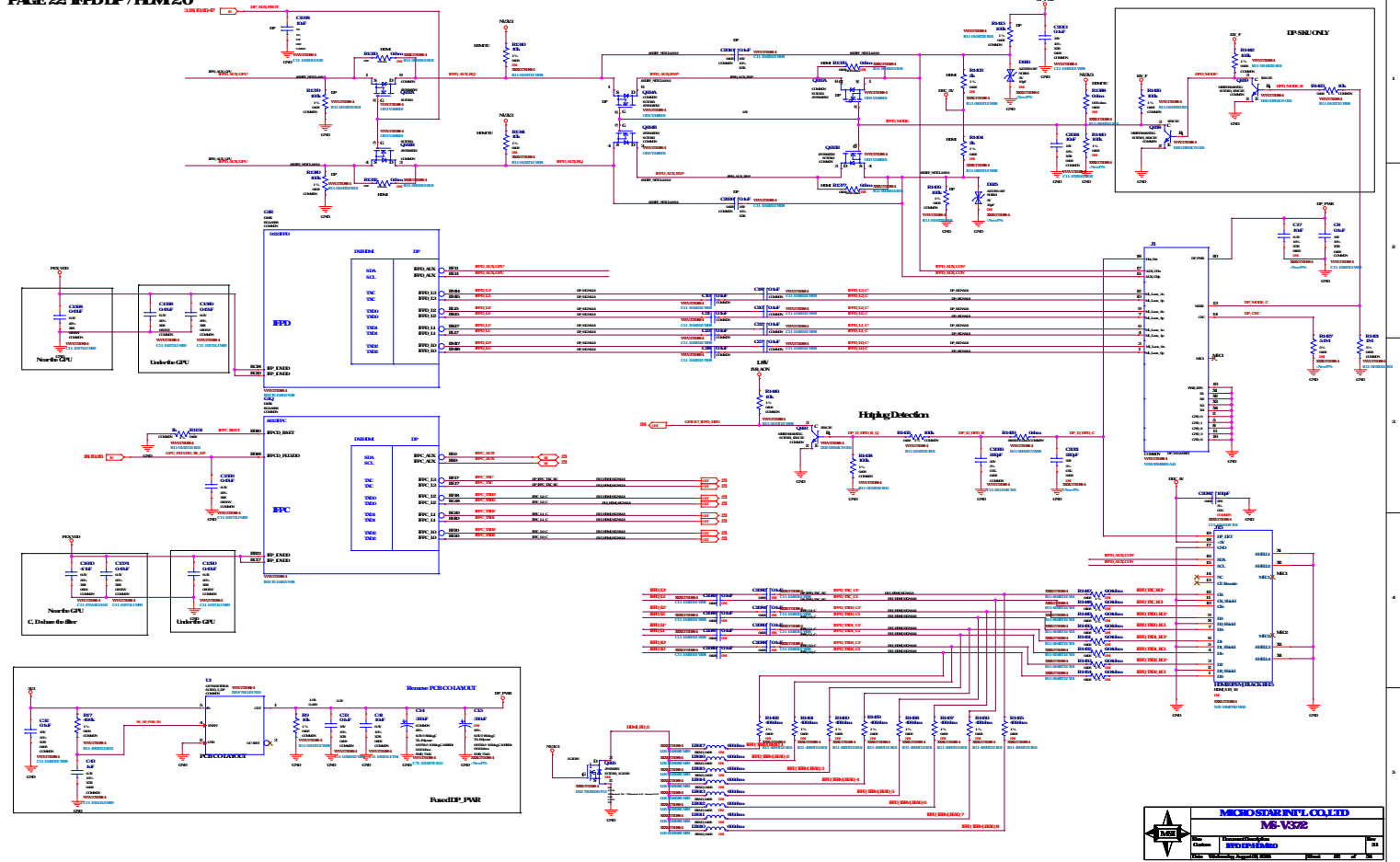


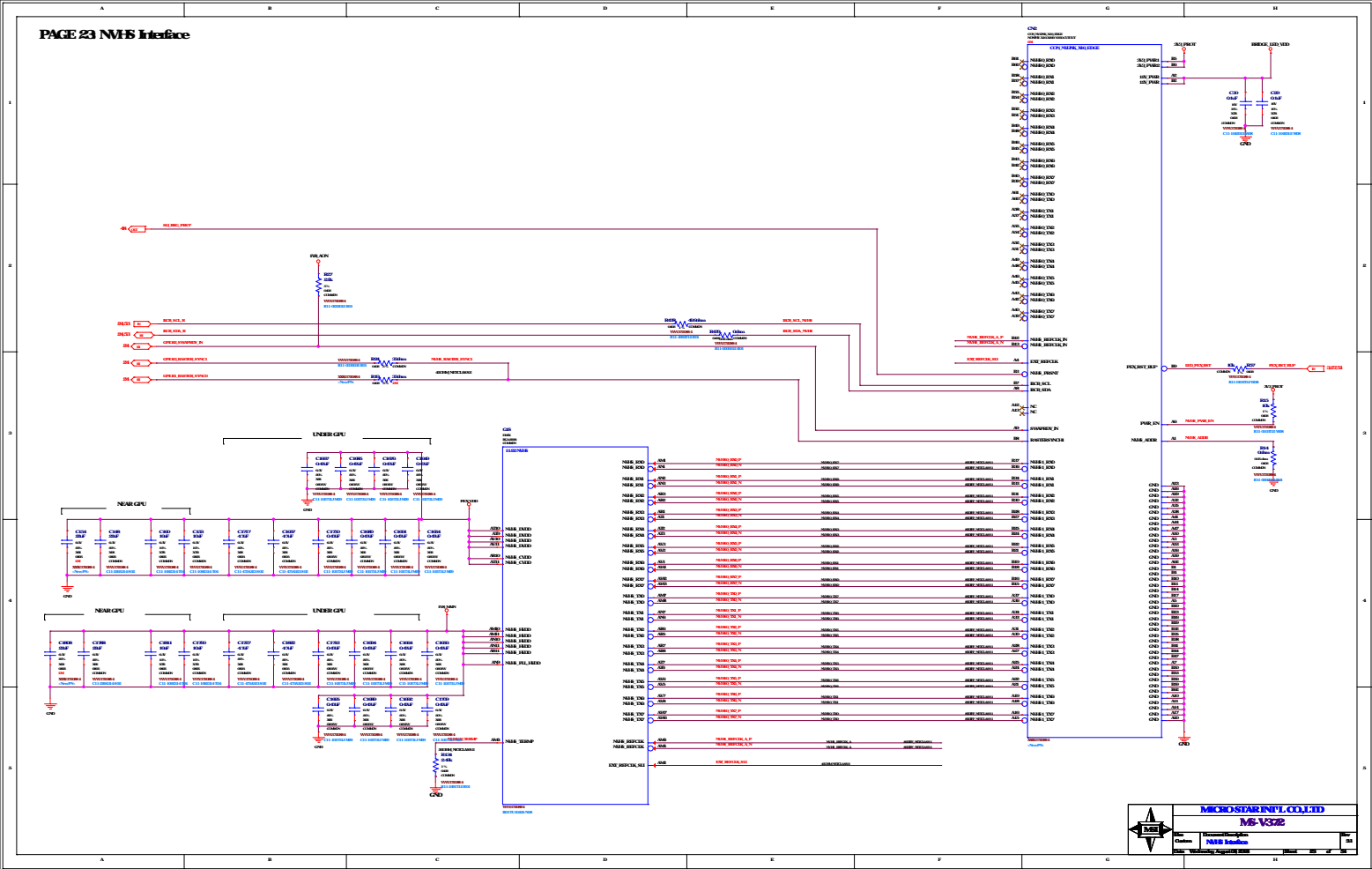
NVDD











H-High :Tied to L8V
M-Midk:Tied to O9V
L-Low :Tied to OV

— **DEFAULT**

DEFAULT

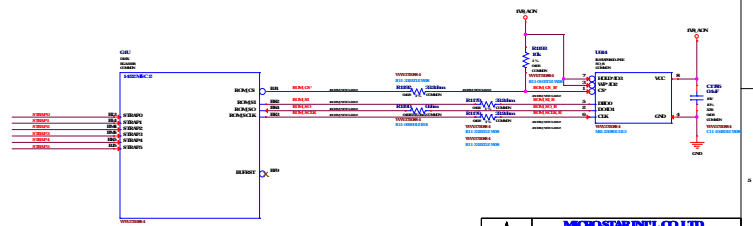
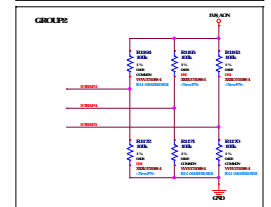
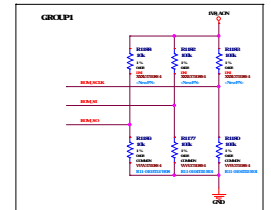
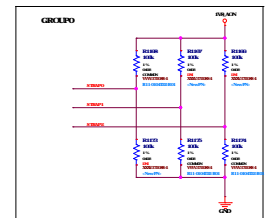
RAMEQ[4]	DENSITY	WIDTH	VENDOR
0000	8G5	2204k	Samsung
0001	8G5	2204k	Micron
0000	8G5	2204k	Hjds
0010	10G5	2204k	Samsung
0011	10G5	2204k	Samsung

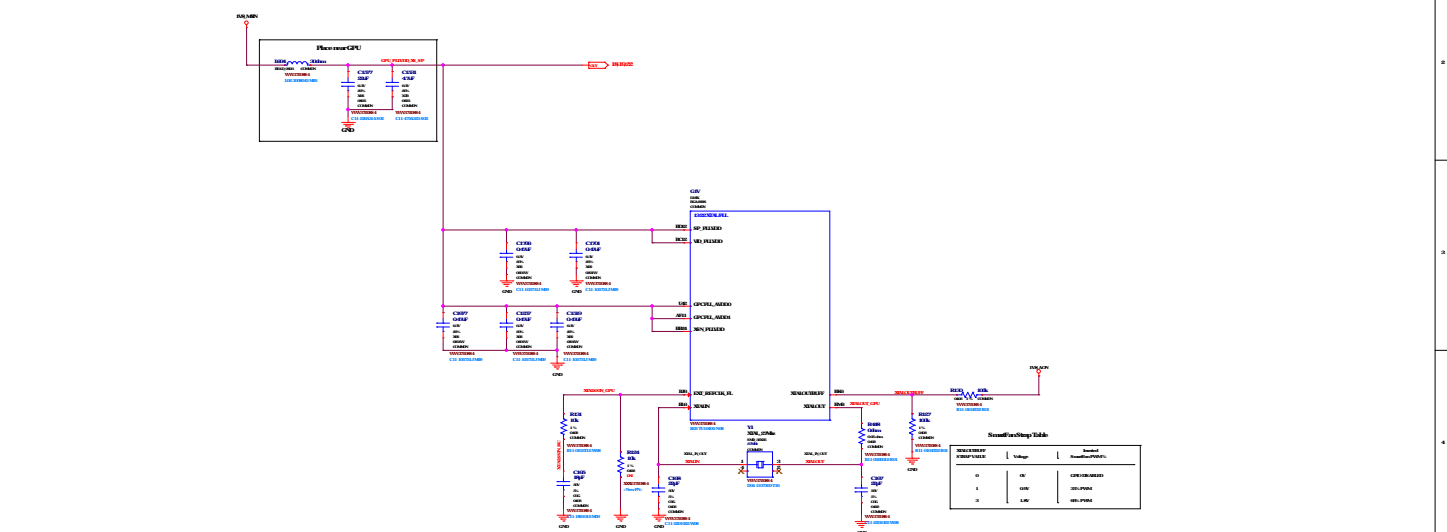
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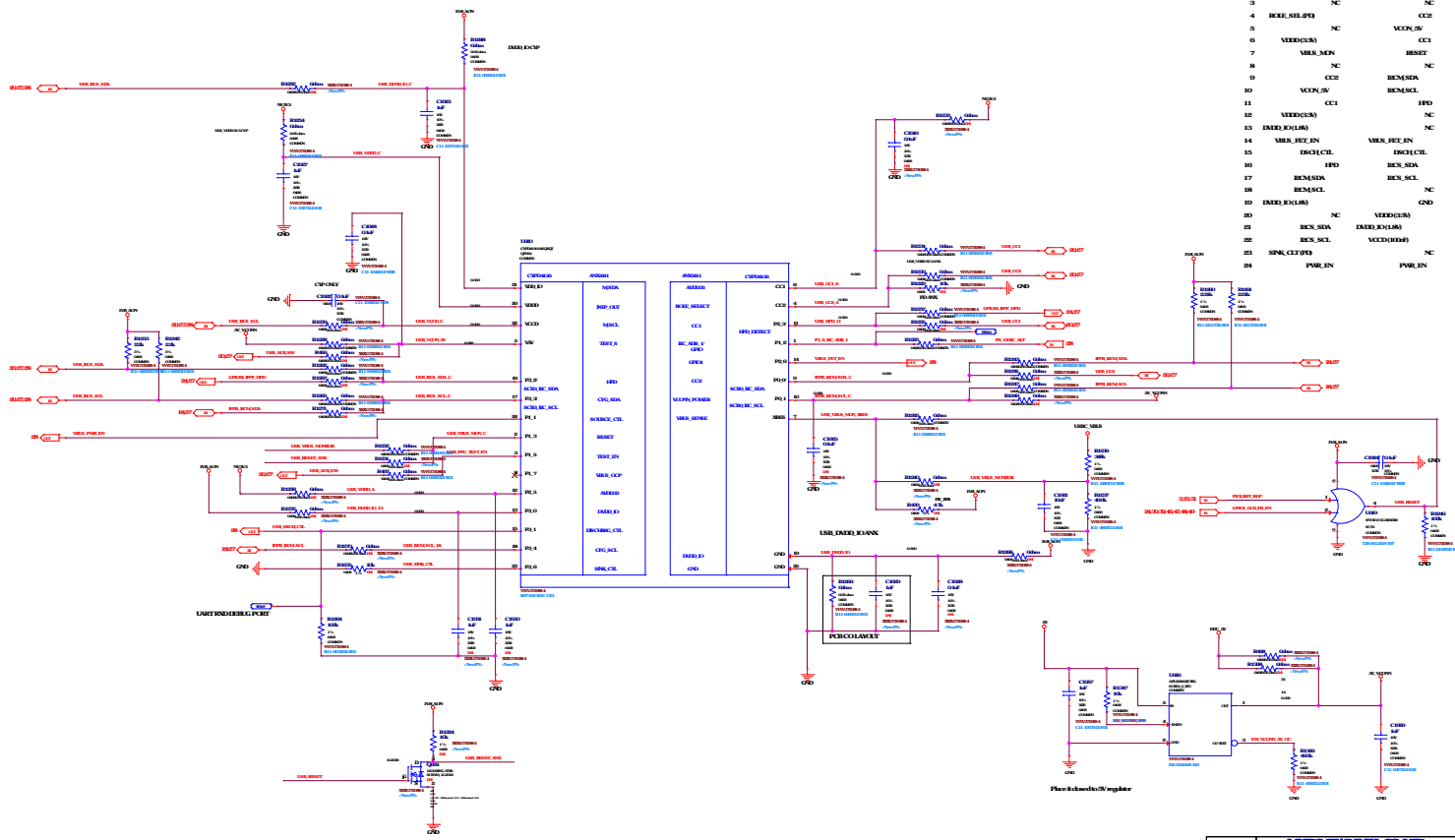
+-----+
+|SMI_AIT_AIDR_ENABLE|
+|SMI_AIT_AIDR_DISABLE|
+|EVID_SEL_REBRAND|
+|EVID_SEL_ORIGINAL|
+|PCIE_CFG_LOWPOWER|
+|PCIE_CFG_HIGHPOWER|
+|VGA_DEVICE_ENABLE|
+|VGA_DEVICE_DISABLE|
+-----+

```

Definition

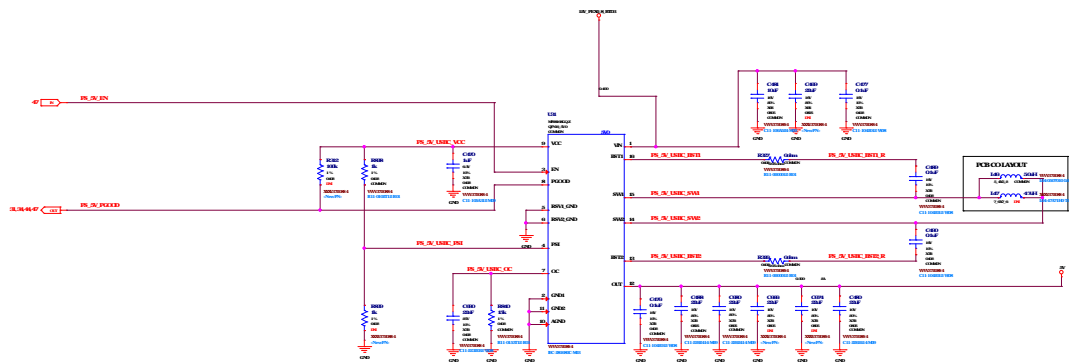




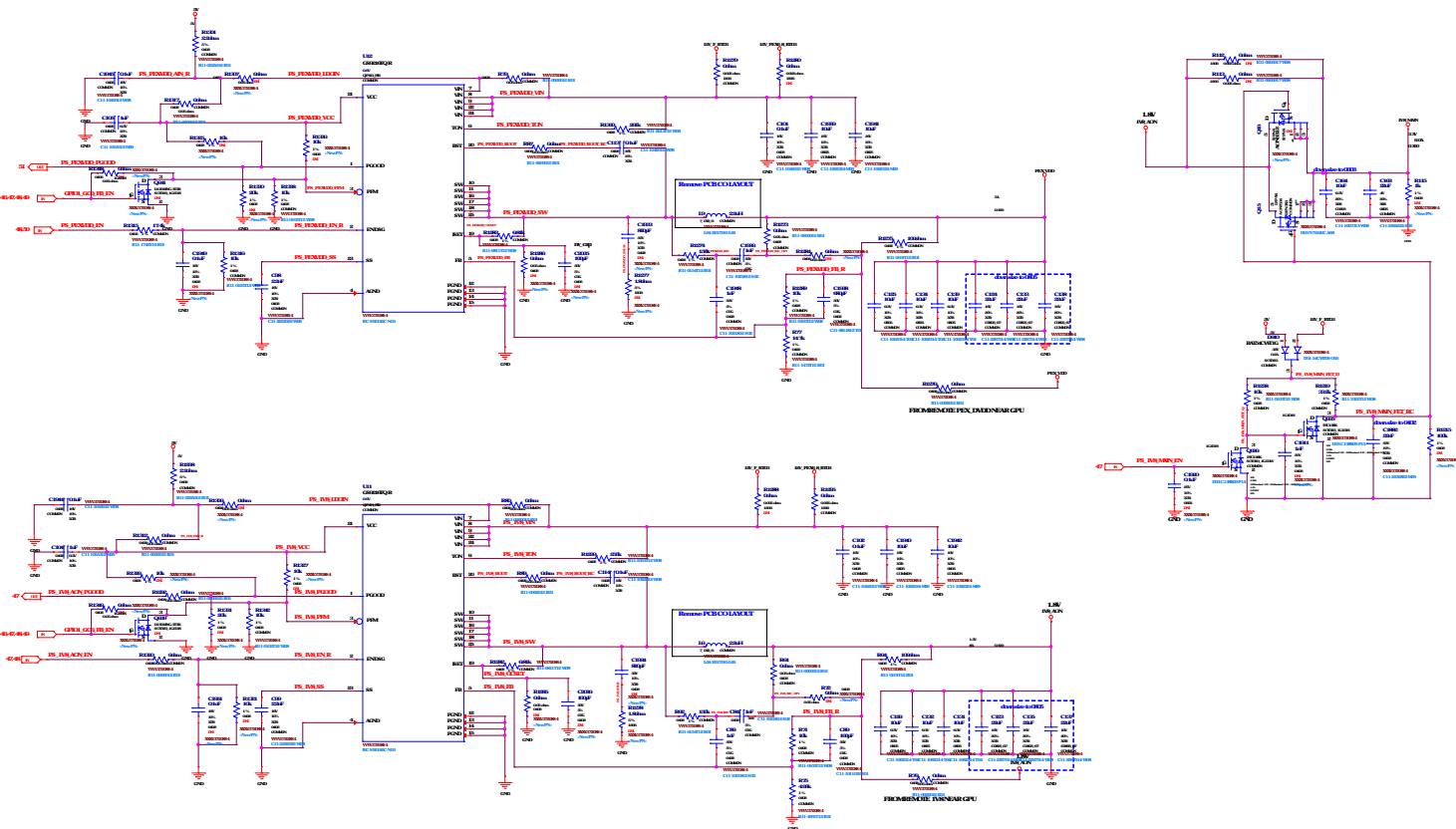


PN	ANK	CNP
1	TP	TP
2	RESET	VRM_AEN
3	NC	NC
4	RESET	CCS
5	NC	VCCIN/5V
6	VRM_AEN	CC1
7	VRM_AEN	RESET
8	NC	NC
9	CCS	VRM_AEN
10	VCCIN/5V	VRM_AEN
11	CC1	VRM_AEN
12	VRM_AEN	NC
13	VRM_AEN	NC
14	VRM_AEN	VRM_AEN
15	VRM_AEN	VRM_AEN
16	VRM_AEN	VRM_AEN
17	VRM_AEN	VRM_AEN
18	VRM_AEN	VRM_AEN
19	VRM_AEN	VRM_AEN
20	VRM_AEN	VRM_AEN
21	VRM_AEN	VRM_AEN
22	VRM_AEN	VRM_AEN
23	VRM_AEN	VRM_AEN
24	VRM_AEN	VRM_AEN



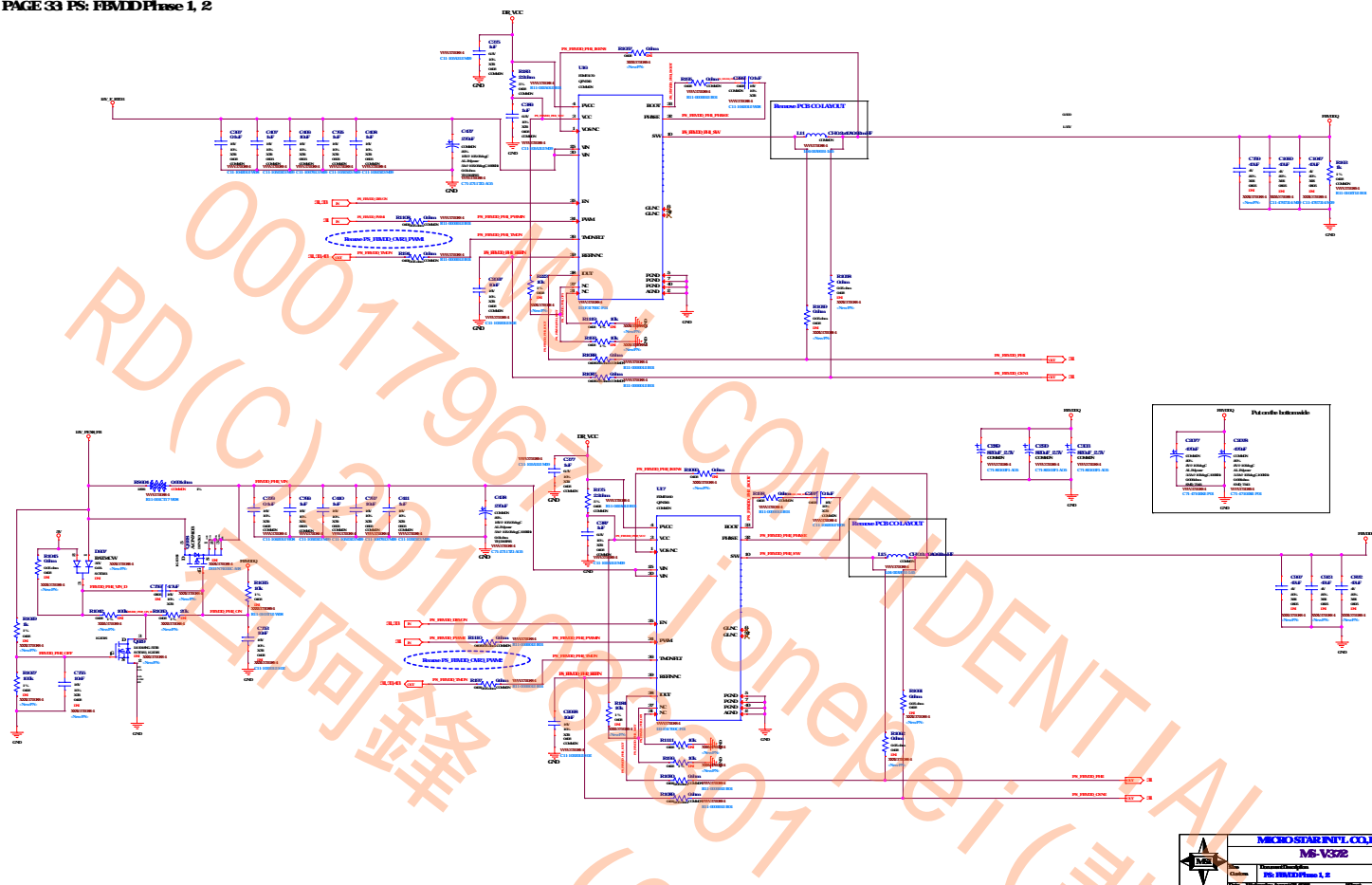


Remove U32 (R1738GJ8)

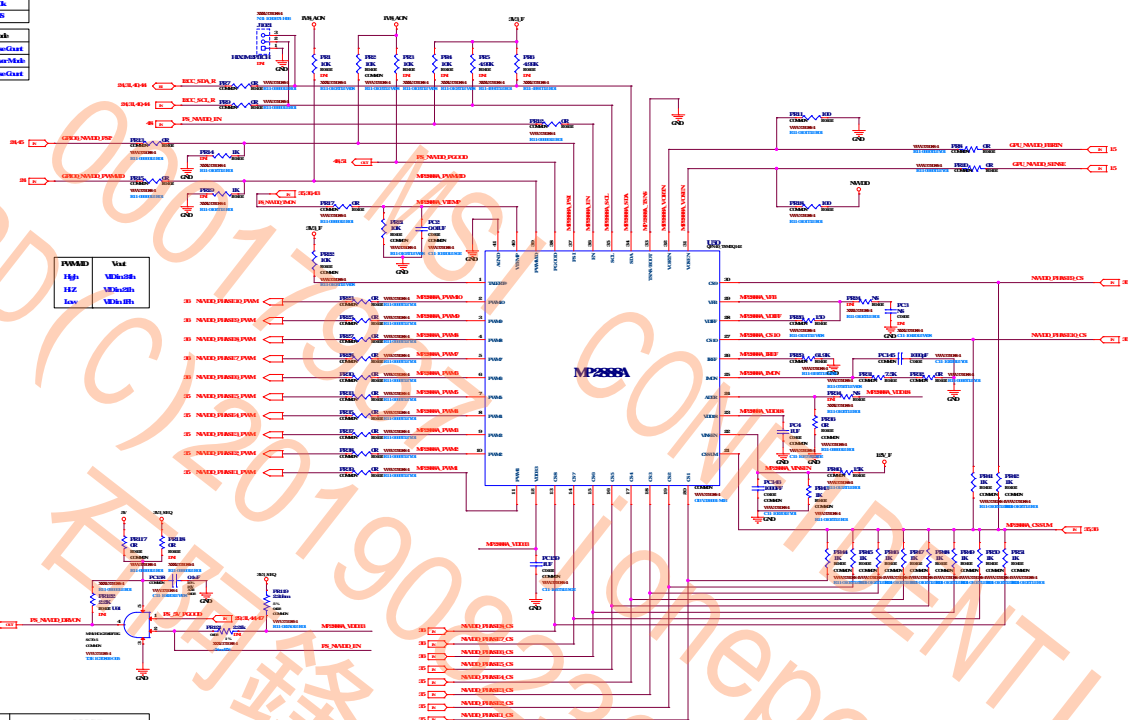


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RD(C)2019082301 RMA工程師
石阿鋒 (00068760)





INType	RS
INValue	RS
INValue	RS
INType	Mode
INType	HighFlowGnd
INType	AutoFlowMode
INType	Low
INType	LowFlowGnd

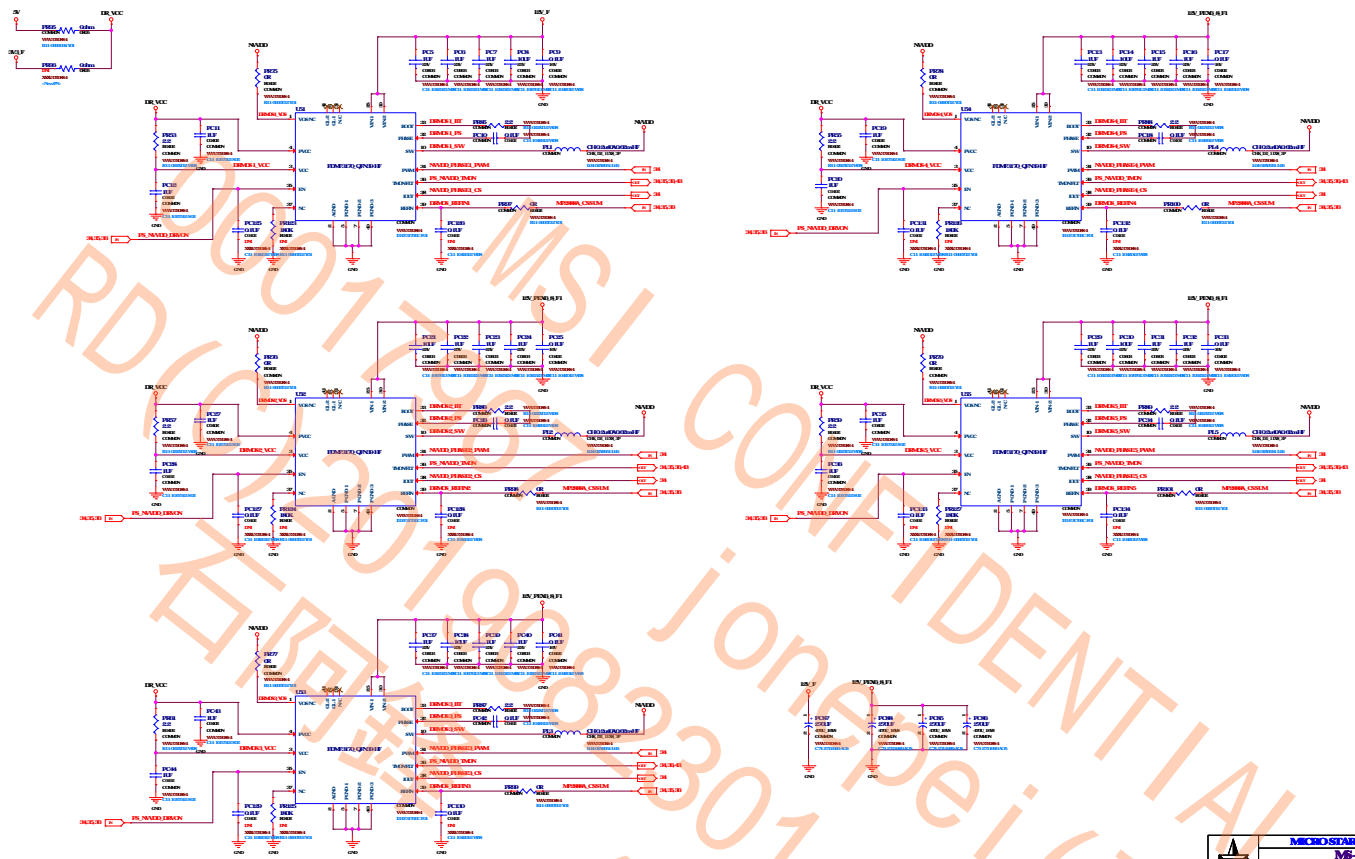


PARAM	Unit
High	MHz
Low	MHz

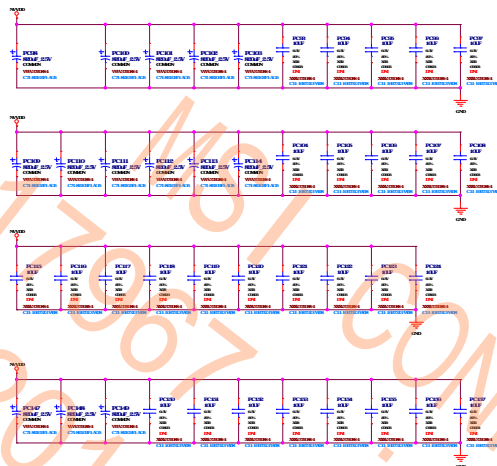
TEC	-NMID
InVinc	30A
Modt	06V
Loadline	0uohm

Power	Setting	Power	Power
Address	Power	Min	Max
200	0.000	0.000	0.000
201	0.000	0.000	0.000
202	0.000	0.000	0.000
203	0.000	0.000	0.000
204	0.000	0.000	0.000
205	0.000	0.000	0.000
206	0.000	0.000	0.000
207	0.000	0.000	0.000
208	0.000	0.000	0.000
209	0.000	0.000	0.000
210	0.000	0.000	0.000
211	0.000	0.000	0.000
212	0.000	0.000	0.000
213	0.000	0.000	0.000
214	0.000	0.000	0.000
215	0.000	0.000	0.000
216	0.000	0.000	0.000
217	0.000	0.000	0.000
218	0.000	0.000	0.000
219	0.000	0.000	0.000
220	0.000	0.000	0.000
221	0.000	0.000	0.000
222	0.000	0.000	0.000
223	0.000	0.000	0.000
224	0.000	0.000	0.000
225	0.000	0.000	0.000
226	0.000	0.000	0.000
227	0.000	0.000	0.000
228	0.000	0.000	0.000
229	0.000	0.000	0.000
230	0.000	0.000	0.000
231	0.000	0.000	0.000
232	0.000	0.000	0.000
233	0.000	0.000	0.000
234	0.000	0.000	0.000
235	0.000	0.000	0.000
236	0.000	0.000	0.000
237	0.000	0.000	0.000
238	0.000	0.000	0.000
239	0.000	0.000	0.000
240	0.000	0.000	0.000
241	0.000	0.000	0.000
242	0.000	0.000	0.000
243	0.000	0.000	0.000
244	0.000	0.000	0.000
245	0.000	0.000	0.000
246	0.000	0.000	0.000
247	0.000	0.000	0.000
248	0.000	0.000	0.000
249	0.000	0.000	0.000
250	0.000	0.000	0.000





NVDD Output CAP



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RD(C)2019082301 RMA工程課
石阿鋒 (00068760)

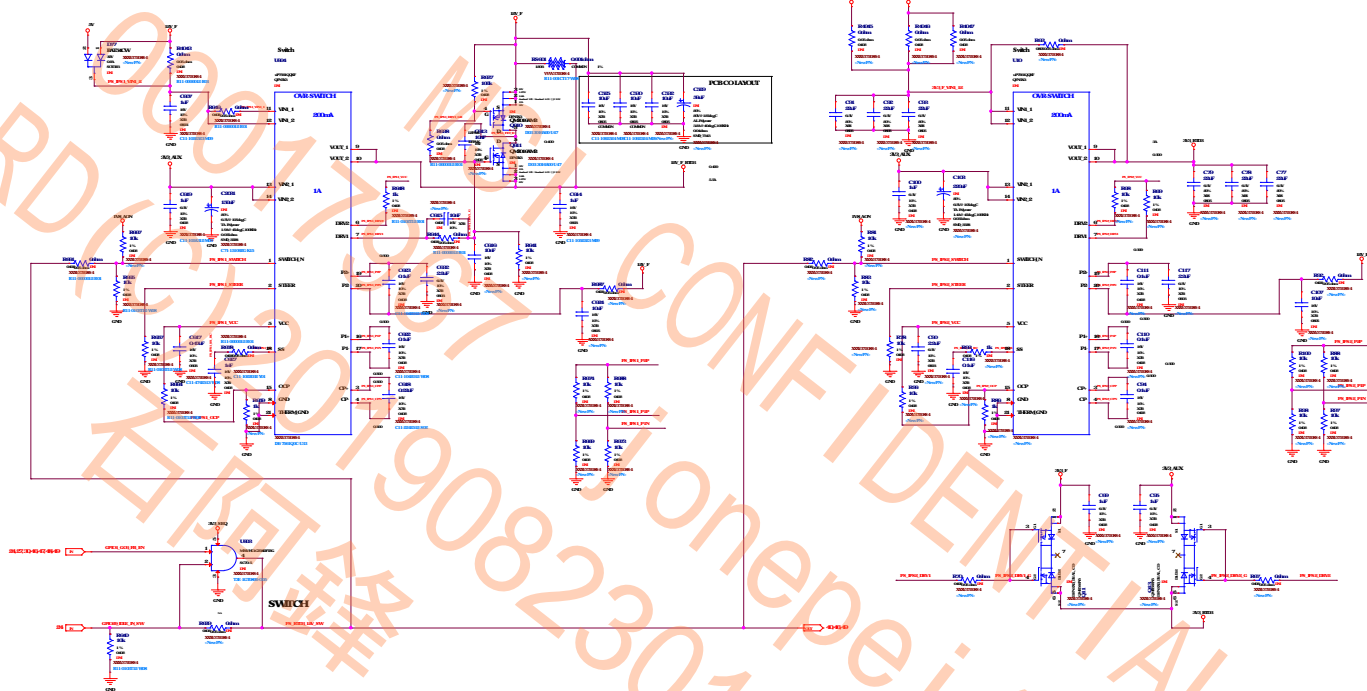


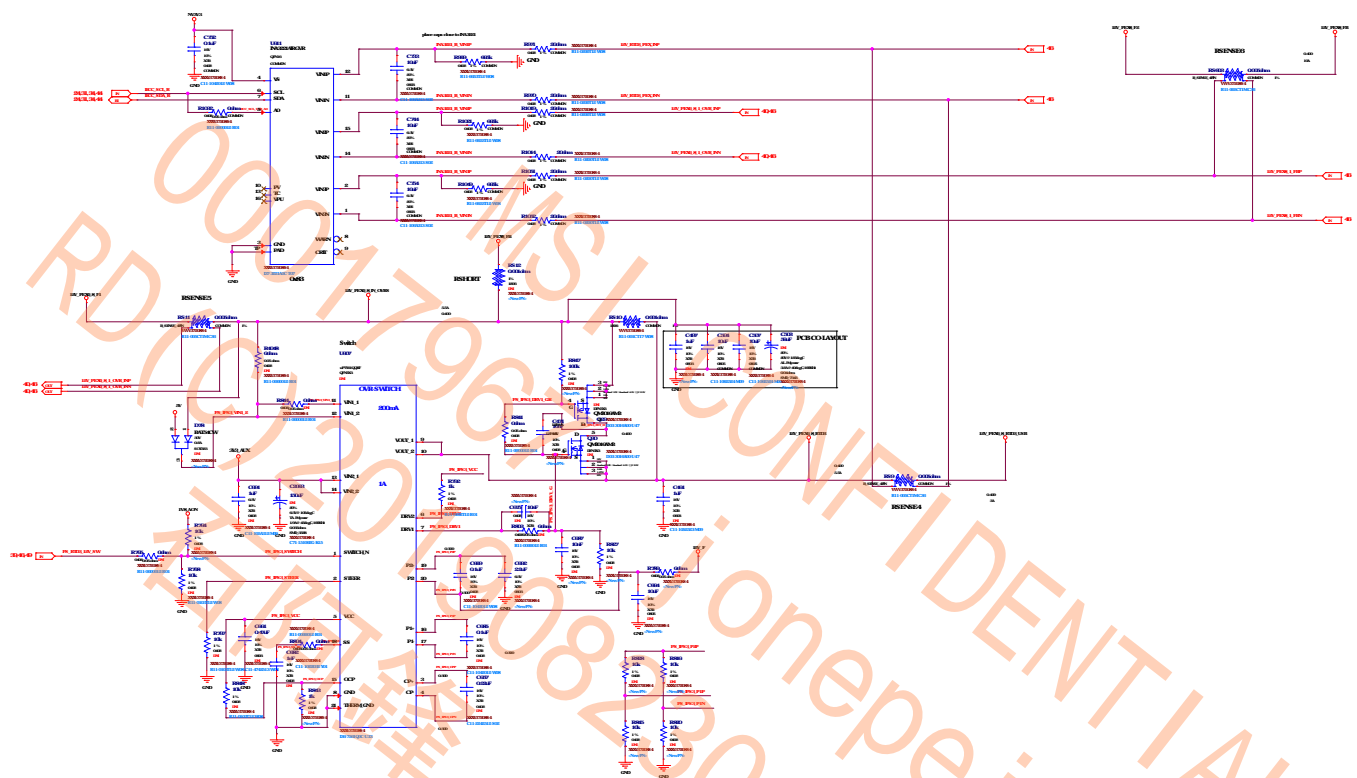
AND GATE LOGIC FOR P BOARD

GPEN	GPEN0	SWITCH	VCUT
0	0	0	IN_F
0	1	0	IN_F
1	0	0	IN_F
1	1	1	IN_A

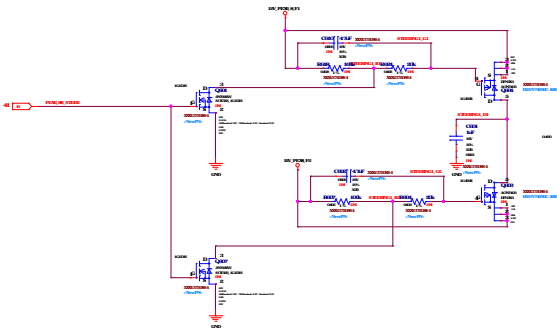
AND GATE LOGIC FOR P BOARD

GPEN	GPEN0	SWITCH	VCUT
0	0	0	IN0
0	1	0	IN0
1	0	0	IN0
1	1	1	IN0A

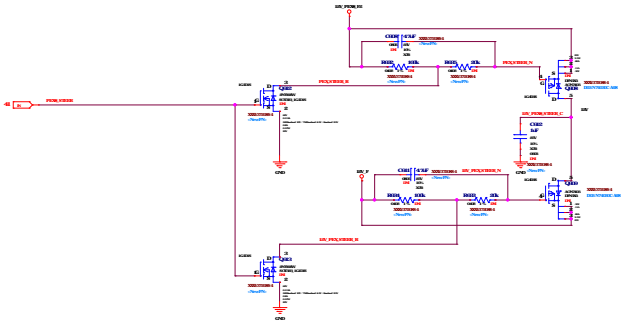


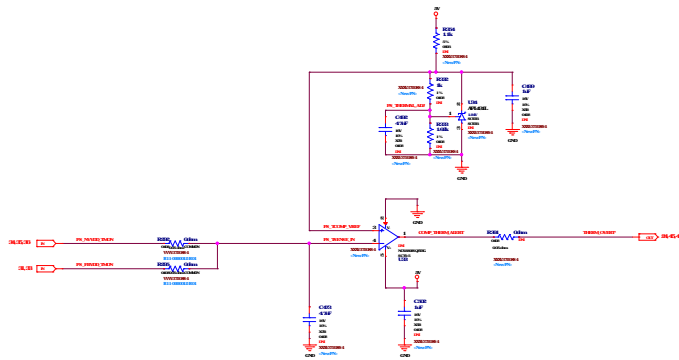


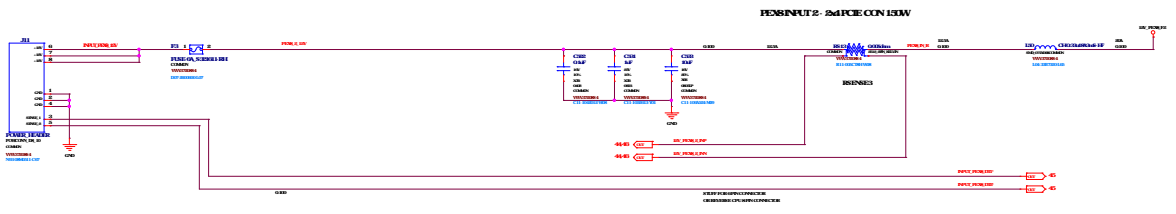
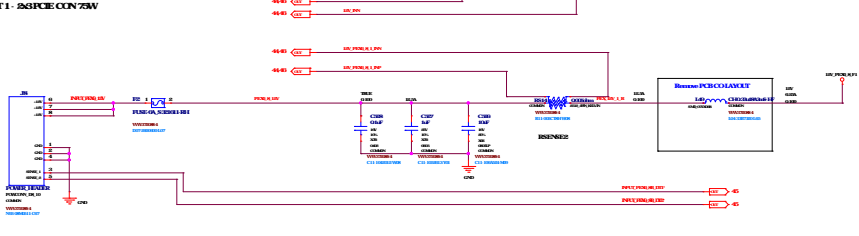
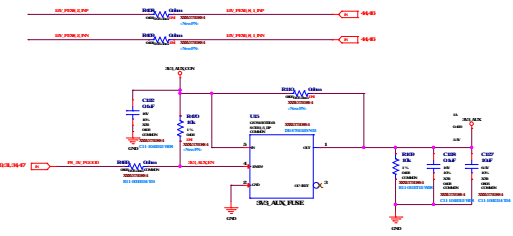
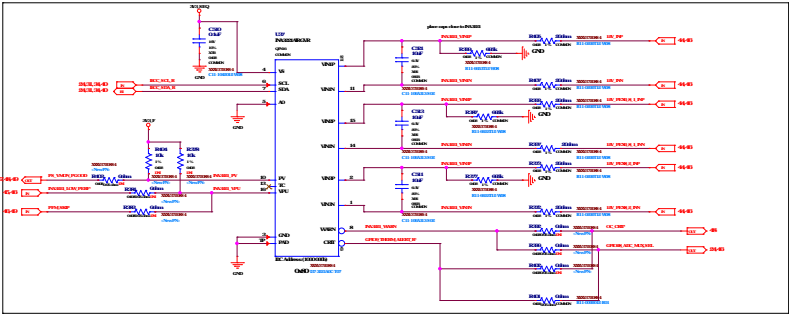
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEXEDGE TO PEX88PIN INPUT AREA

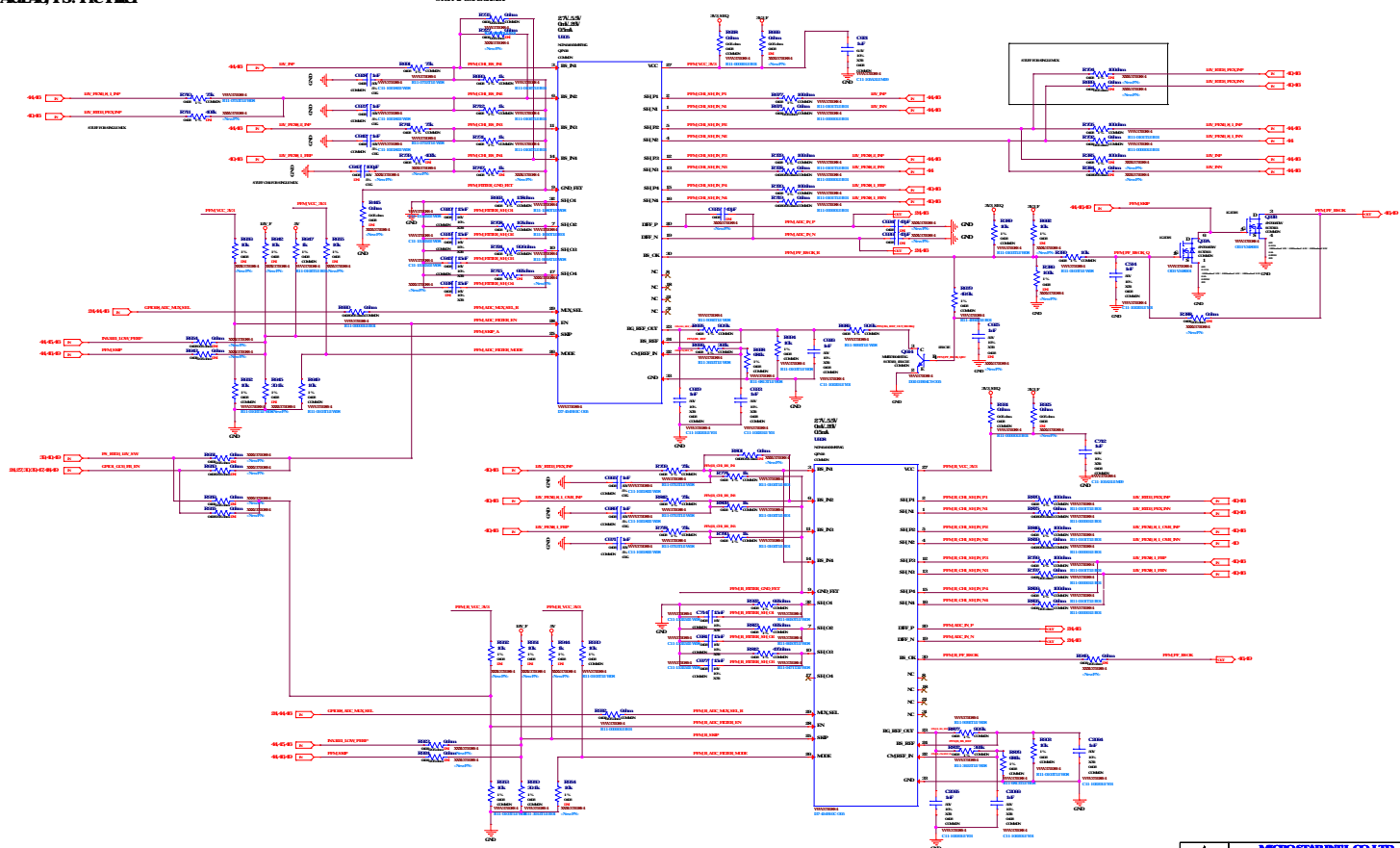


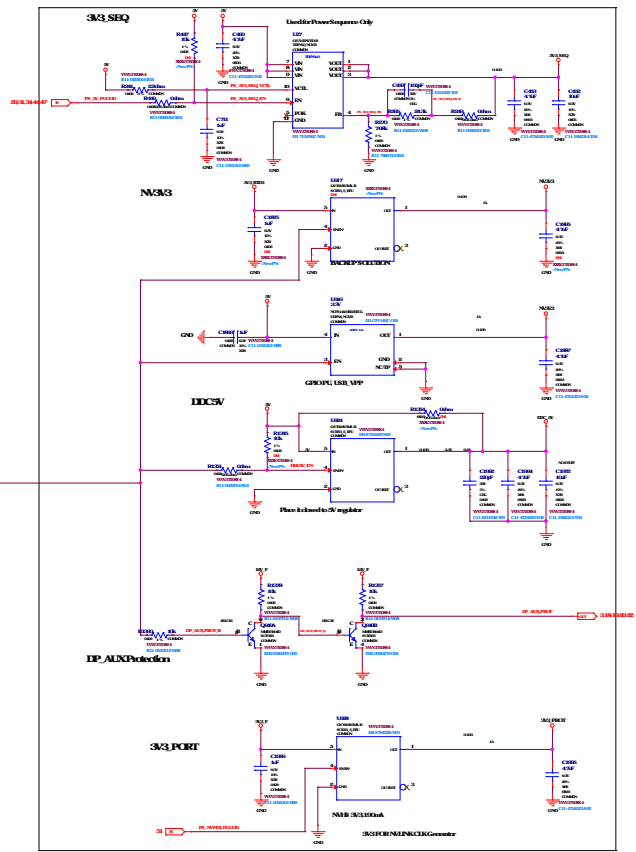
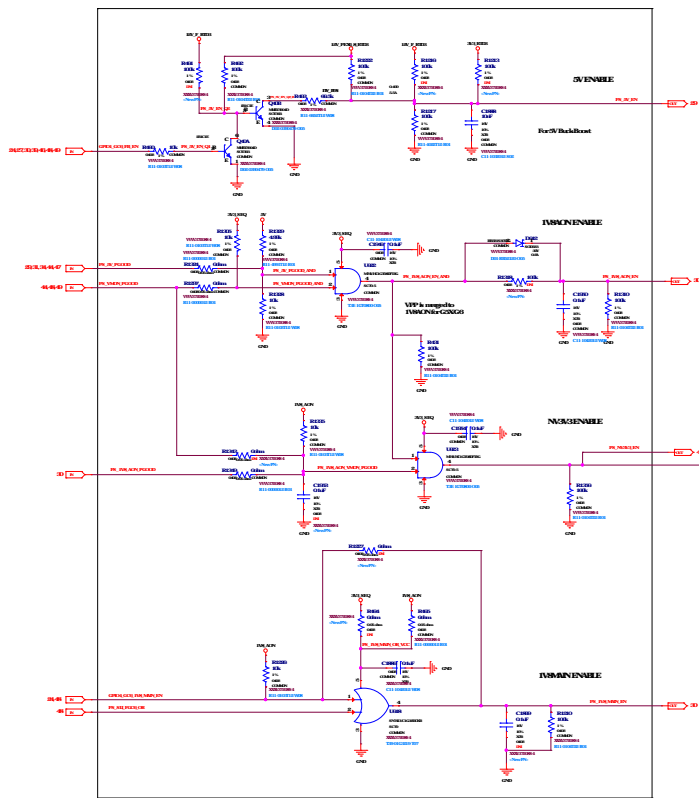
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEXEDGE TO PEX88PIN INPUT AREA

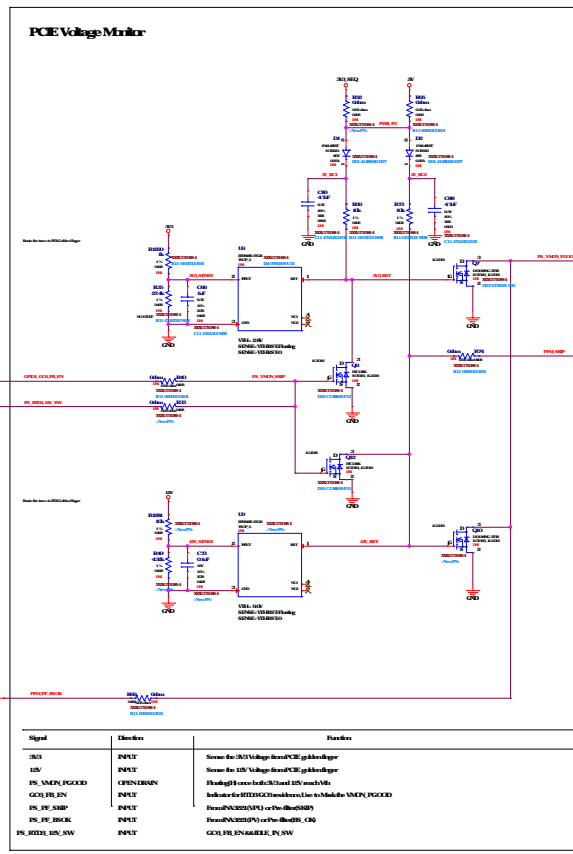








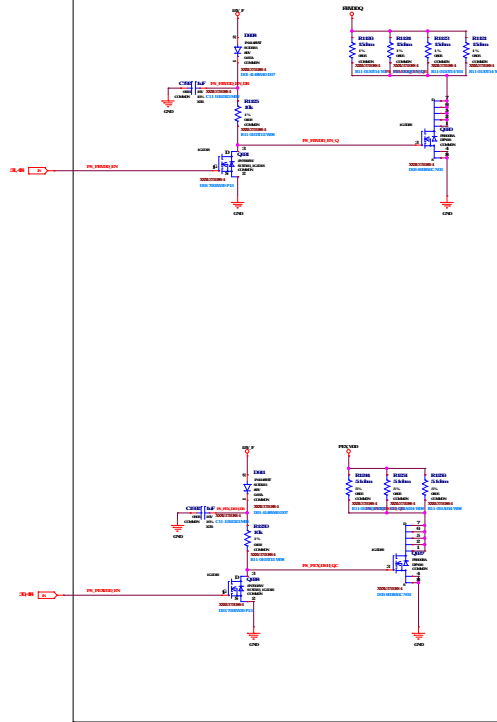


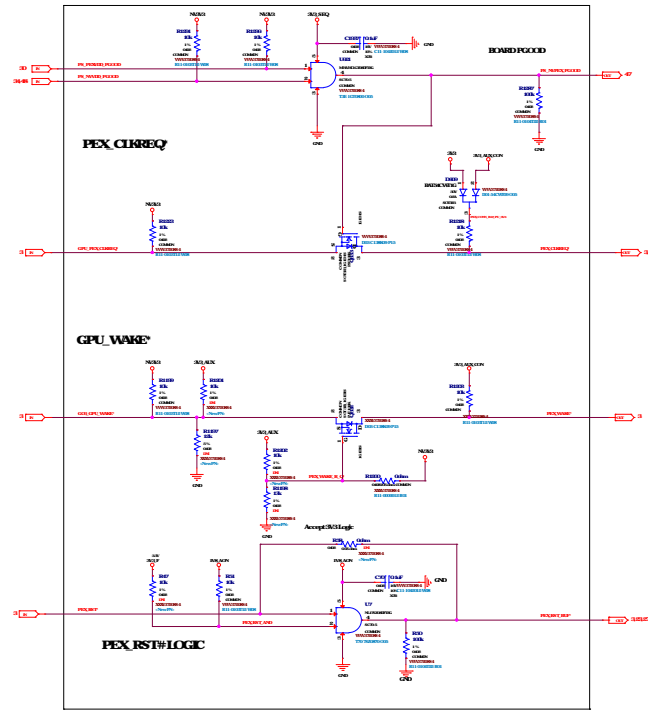


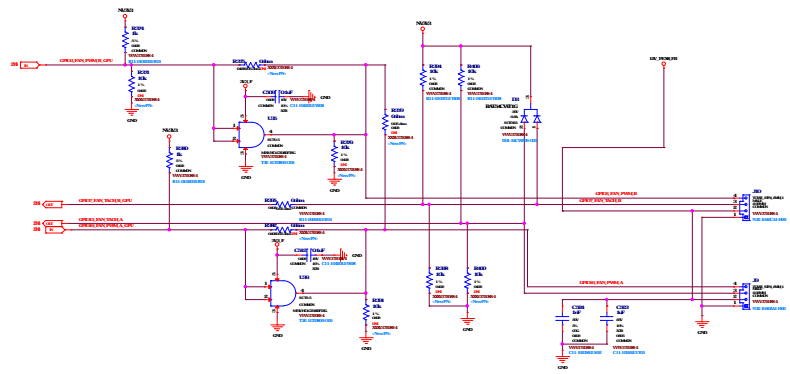
BOM Configuration

COMPNO	POWER/SENSE	POWER/SENSE	POWER/SENSE
Use Po Filter	Po Filter NOTIFY ULS NOTIFY QMS NOTIFY DIS	Po Filter NOTIFY ULS NOTIFY QMS NOTIFY DIS	Po Filter
Use POCES	Voltage_Monitor NOTIFY ULS NOTIFY QMS	POCES NOTIFY ULS NOTIFY QMS	POCES
NO POCES	Voltage_Monitor	Voltage_Monitor	NA

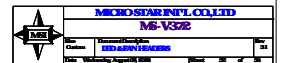
Power Supply
P3322-3/3/SEQ
Po_Filter(ADC_MUX/3/3/SEQ)
Dual Po Filter case
Only use the Primary Po Filter to sense 3/3/SEQ
and All Input ISSs

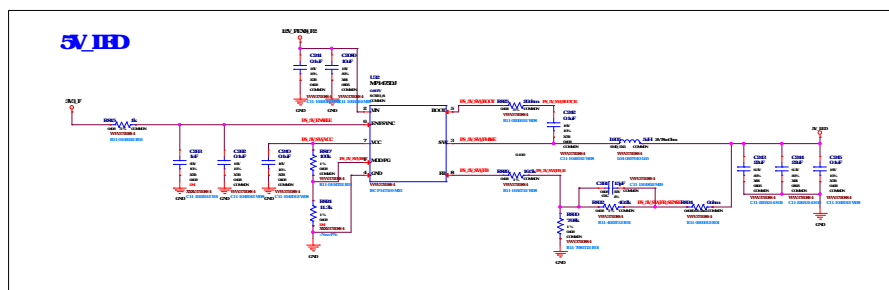
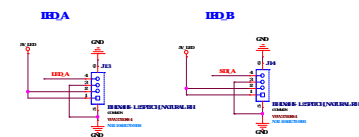
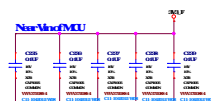
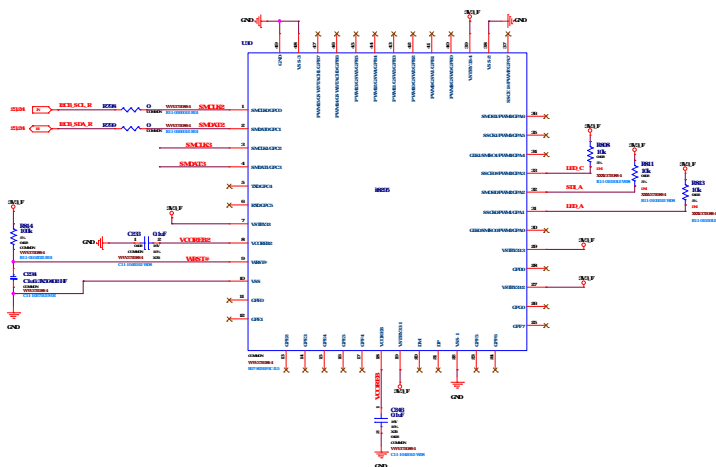




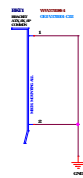


Remove LED BOOST

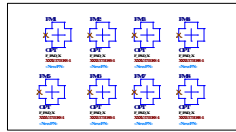
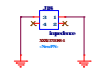




Bracket



Screw



CPU Mounting Hole



Mechanical Holes Symbol

