P407-A00: G84M/86M MXM V1.3
256/512MB 128-BIT GDDR2
LVDS, DVI-A, DVI-B, TV-OUT, VGA, HDMI
SLI, HDCP SUPPORT

Table of Contents

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10407-9998-300	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
1	SKU0001	600-10407-0001-300	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
2	SKU0002	600-10407-0002-300	G84M-600 450/400 512MB 128bit GDDR2 32Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
3	SKU0003	600-10407-0003-300	G84M-700 500/400 512MB 128bit GDDR2 32Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
4	SKU0003	600-10407-0004-300	G86M-770 500/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

P407_A03 change list:

1) P407_A03 is modified from P555_A00 to insure they are exactly same, except 2 mounting holes and 4 thermal hole

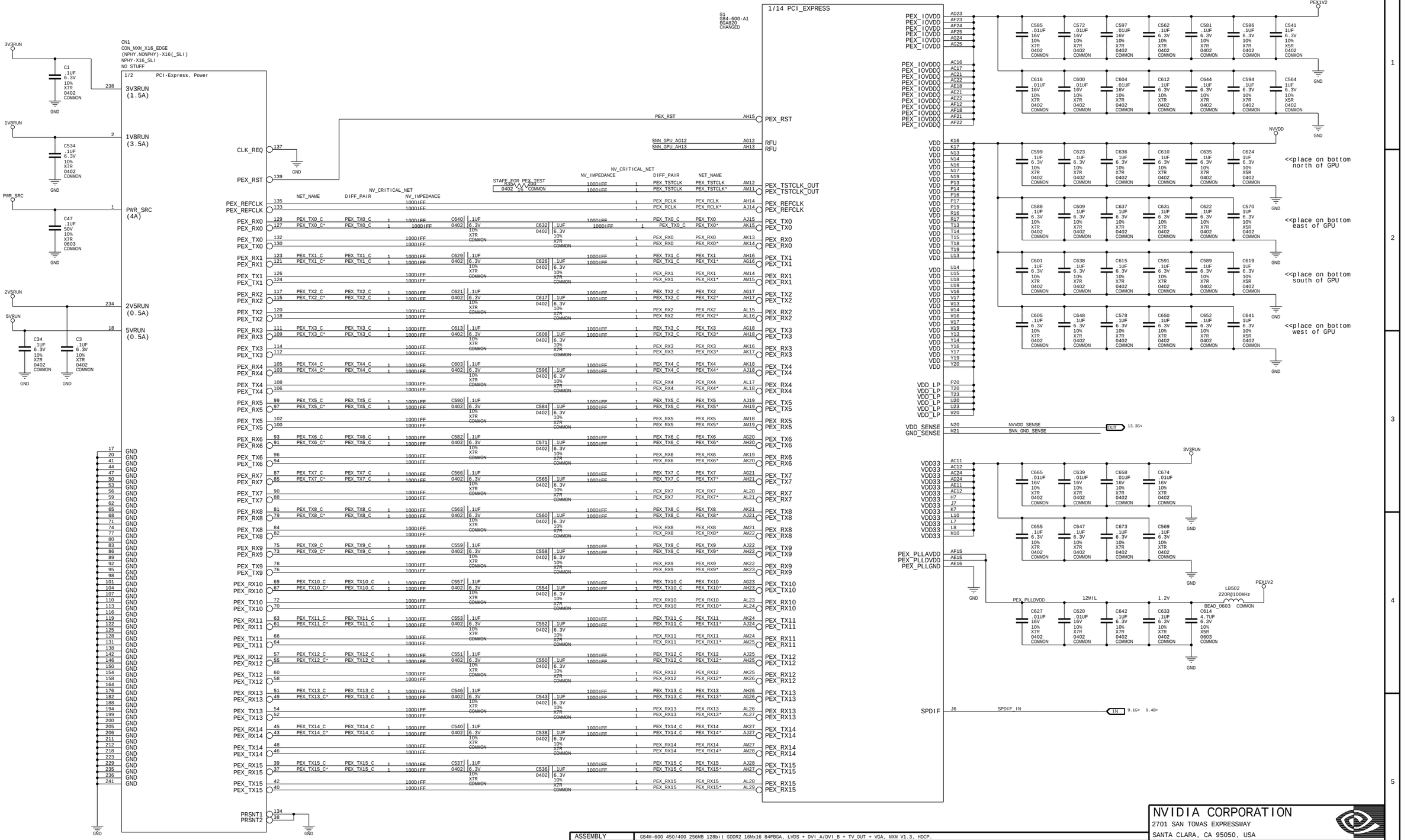
2) Change mounting holes and thermal holes from MXM V2.0 to MXM V1.3

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	Cover Page

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10407-0001-300 A		
ID	p407_a03	PAGE	1 OF 18
NAME	myan	DATE	21-DEC-2006

PAGE 2) MXM-II GOLDEN EDGE, PCI EXPRESS INTERFACE



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	PCI EXPRESS Interface

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10407-0001-300 A		
ID	p407_a03	PAGE	2 OF 18
NAME	myan	DATE	21-DEC-2006

PAGE 3) GPU MEMORY INTERFACE

NET	NV_IMPEDANCE	NV_CRITICAL_NET
FBA_RESET	50OHM	2
FBA_ODT_GPU	50OHM	2
FBC_RESET	50OHM	2
FBC_ODT_GPU	50OHM	2

G1
G84-600-A1
BGA820
CHANGED

2/14 FBA

0	FBAD<0>	N27	FBAD0
1	FBAD<1>	M27	FBAD1
2	FBAD<2>	N28	FBAD2
3	FBAD<3>	L29	FBAD3
4	FBAD<4>	K27	FBAD4
5	FBAD<5>	K28	FBAD5
6	FBAD<6>	J29	FBAD6
7	FBAD<7>	J28	FBAD7
8	FBAD<8>	P30	FBAD8
9	FBAD<9>	N31	FBAD9
10	FBAD<10>	N30	FBAD10
11	FBAD<11>	N32	FBAD11
12	FBAD<12>	L31	FBAD12
13	FBAD<13>	L30	FBAD13
14	FBAD<14>	J30	FBAD14
15	FBAD<15>	L32	FBAD15
16	FBAD<16>	H30	FBAD16
17	FBAD<17>	K30	FBAD17
18	FBAD<18>	H31	FBAD18
19	FBAD<19>	F30	FBAD19
20	FBAD<20>	H32	FBAD20
21	FBAD<21>	E31	FBAD21
22	FBAD<22>	D30	FBAD22
23	FBAD<23>	E30	FBAD23
24	FBAD<24>	H28	FBAD24
25	FBAD<25>	H29	FBAD25
26	FBAD<26>	E29	FBAD26
27	FBAD<27>	J27	FBAD27
28	FBAD<28>	F27	FBAD28
29	FBAD<29>	E27	FBAD29
30	FBAD<30>	E28	FBAD30
31	FBAD<31>	F28	FBAD31
32	FBAD<32>	AD29	FBAD32
33	FBAD<33>	AE29	FBAD33
34	FBAD<34>	AD28	FBAD34
35	FBAD<35>	AC28	FBAD35
36	FBAD<36>	AB29	FBAD36
37	FBAD<37>	AA30	FBAD37
38	FBAD<38>	Y28	FBAD38
39	FBAD<39>	AB30	FBAD39
40	FBAD<40>	AW30	FBAD40
41	FBAD<41>	AF30	FBAD41
42	FBAD<42>	AJ31	FBAD42
43	FBAD<43>	AJ30	FBAD43
44	FBAD<44>	AJ32	FBAD44
45	FBAD<45>	AK29	FBAD45
46	FBAD<46>	AM31	FBAD46
47	FBAD<47>	AL30	FBAD47
48	FBAD<48>	AE32	FBAD48
49	FBAD<49>	AE30	FBAD49
50	FBAD<50>	AE31	FBAD50
51	FBAD<51>	AD30	FBAD51
52	FBAD<52>	AC31	FBAD52
53	FBAD<53>	AC32	FBAD53
54	FBAD<54>	AB32	FBAD54
55	FBAD<55>	AB31	FBAD55
56	FBAD<56>	AG27	FBAD56
57	FBAD<57>	AF28	FBAD57
58	FBAD<58>	AH28	FBAD58
59	FBAD<59>	AG28	FBAD59
60	FBAD<60>	AG29	FBAD60
61	FBAD<61>	AD27	FBAD61
62	FBAD<62>	AF27	FBAD62
63	FBAD<63>	AE28	FBAD63

0	FBADQM<0>	M29	FBADQM0
1	FBADQM<1>	M30	FBADQM1
2	FBADQM<2>	G30	FBADQM2
3	FBADQM<3>	F29	FBADQM3
4	FBADQM<4>	AA29	FBADQM4
5	FBADQM<5>	AK30	FBADQM5
6	FBADQM<6>	AC30	FBADQM6
7	FBADQM<7>	AG30	FBADQM7

B1	FBADQS0	L28	FBADQS_WP0
B1	FBADQS1	K31	FBADQS_WP1
B1	FBADQS2	G32	FBADQS_WP2
B1	FBADQS3	G28	FBADQS_WP3
B1	FBADQS4	AB28	FBADQS_WP4
B1	FBADQS5	AL32	FBADQS_WP5
B1	FBADQS6	AF32	FBADQS_WP6
B1	FBADQS7	AH30	FBADQS_WP7

B1	FBADQS0*	M28	FBADQS_RN0
B1	FBADQS1*	K32	FBADQS_RN1
B1	FBADQS2*	G31	FBADQS_RN2
B1	FBADQS3*	G27	FBADQS_RN3
B1	FBADQS4*	AA28	FBADQS_RN4
B1	FBADQS5*	AL31	FBADQS_RN5
B1	FBADQS6*	AF31	FBADQS_RN6
B1	FBADQS7*	AH29	FBADQS_RN7

FBVDD	A12	
FBVDD	A18	
FBVDD	A21	
FBVDD	A24	
FBVDD	A27	
FBVDD	A3	
FBVDD	A30	
FBVDD	A6	
FBVDD	A9	
FBVDD	AA32	
FBVDD	AD32	
FBVDD	AG32	
FBVDD	AK32	
FBVDD	C32	
FBVDD	F32	
FBVDD	J32	
FBVDD	M32	
FBVDD	R32	
FBVDDQ	AA25	
FBVDDQ	AA26	
FBVDDQ	AB25	
FBVDDQ	AB26	
FBVDDQ	G11	
FBVDDQ	G15	
FBVDDQ	G18	
FBVDDQ	G21	
FBVDDQ	G22	
FBVDDQ	H11	
FBVDDQ	H12	
FBVDDQ	H15	
FBVDDQ	H18	
FBVDDQ	H21	
FBVDDQ	H22	
FBVDDQ	L25	
FBVDDQ	L26	
FBVDDQ	M25	
FBVDDQ	M26	
FBVDDQ	R25	
FBVDDQ	R26	
FBVDDQ	V25	
FBVDDQ	V26	

FBVDDQ

C643	C634	C548	C607	C606
.1UF	.1UF	.1UF	.1UF	.1UF
6.3V	6.3V	6.3V	6.3V	6.3V
10%	10%	10%	10%	10%
X7R	X7R	X7R	X7R	X7R
0402	0402	0402	0402	0402
COMMON	COMMON	COMMON	COMMON	COMMON

C576	C575	C593	C547	C587
.1UF	.1UF	.1UF	.1UF	.1UF
6.3V	6.3V	6.3V	6.3V	6.3V
10%	10%	10%	10%	10%
X7R	X7R	X7R	X7R	X7R
0402	0402	0402	0402	0402
COMMON	COMMON	COMMON	COMMON	COMMON

C645	C611	C545	C670	C602
.1UF	.1UF	.1UF	.1UF	.1UF
6.3V	6.3V	6.3V	6.3V	6.3V
10%	10%	10%	10%	10%
X7R	X7R	X7R	X7R	X7R
0402	0402	0402	0402	0402
COMMON	COMMON	COMMON	COMMON	COMMON

C654	C579	C618	C681	C583
.1UF	.1UF	.1UF	.1UF	.1UF
6.3V	6.3V	6.3V	6.3V	6.3V
10%	10%	10%	10%	10%
X7R	X7R	X7R	X7R	X7R
0402	0402	0402	0402	0402
COMMON	COMMON	COMMON	COMMON	COMMON

C598	C661	C574	C625	C573
1UF	1UF	1UF	1UF	1UF
6.3V	6.3V	6.3V	6.3V	6.3V
10%	10%	10%	10%	10%
X5R	X5R	X5R	X5R	X5R
0402	0402	0402	0402	0402
COMMON	COMMON	COMMON	COMMON	COMMON

GND

FBA_CMD0	P32	FBA_A<3>	3
FBA_CMD1	U27	FBA_A<0>	0
FBA_CMD2	P31	FBA_A<2>	2
FBA_CMD3	U30	FBA_A<1>	1
FBA_CMD4	Y31	FBB_A<3>	3
FBA_CMD5	W32	FBB_A<4>	4
FBA_CMD6	W31	FBB_A<5>	5
FBA_CMD7	T32	FBA_BA2	
FBA_CMD8	V27	FBA_CS0*	
FBA_CMD9	T28	FBA_WE*	
FBA_CMD10	T31	FBA_BA0	
FBA_CMD11	U32	FBA_CKE	
FBA_CMD12	W29	FBA_RESET	
FBA_CMD13	W30	FBB_A<2>	2
FBA_CMD14	T27	FBA_A<12>	12
FBA_CMD15	V28	FBA_RAS*	
FBA_CMD16	V30	FBA_A<11>	11
FBA_CMD17	U31	FBA_A<10>	10
FBA_CMD18	R27	FBA_BA1	
FBA_CMD19	V29	FBA_A<8>	8
FBA_CMD20	T30	FBA_A<9>	9
FBA_CMD21	W28	FBA_A<6>	6
FBA_CMD22	R29	FBA_A<5>	5
FBA_CMD23	R30	FBA_A<7>	7
FBA_CMD24	P29	FBA_A<4>	4
FBA_CMD25	U28	FBA_CAS*	
FBA_CMD26	Y32	SNN_FBA_CMD26	
FBA_CMD27	Y30	SNN_FBA_CMD27	
FBA_CMD28	V32	SNN_FBA_CMD28	

FBB_A<5..2> → FBB_A<3>, FBB_A<4>, FBB_A<5>, FBB_A<2>
FBA_A<12..0> → FBA_A<3>, FBA_A<0>, FBA_A<2>, FBA_A<1>, FBB_A<3>, FBB_A<4>, FBB_A<5>, FBB_A<2>, FBA_A<12>, FBA_RAS*, FBA_A<11>, FBA_A<10>, FBA_BA1, FBA_A<8>, FBA_A<9>, FBA_A<6>, FBA_A<5>, FBA_A<7>, FBA_A<4>, FBA_CAS*

FBA_CLK0	P28	FBA_CLK0	4.3A< 4.4F<
FBA_CLK0	R28	FBA_CLK0*	4.3A< 4.4F<
FBA_CLK1	Y27	FBA_CLK1	4.3C< 4.4F<
FBA_CLK1	AA27	FBA_CLK1*	4.3E< 4.4F<
FBA_DEBUG	AC27	FBA_ODT_GPU	

H_PLLAVDD	G23		
FBA_PLLAVDD	G25	FBA_PLLAVDD_GPU	
FBA_PLLGND	G24		

PLACE CLOSE TO BALLS
FBA_PLLAVDD_GPU — 12MIL — 1.2V — 220R@100MHz BEAD_0603 COMMON — LB501 — PEX1V2

C568	470PF	16V 10% X7R 0402 COMMON
C577	.01UF	16V 10% X7R 0402 COMMON
C539	4.7UF	6.3V 10% X5R 0603 COMMON

GND

NC1	D31	SNN_FBA_NC1_D31	
NC2	D32	SNN_FBA_NC1_D32	

FBVDDQ
R527 1K 1% 0402 NO STUFF
FB_VREF1 — 12MIL — E32 — FB_VREF1
R529 1K 1% 0402 NO STUFF
C542 .1UF 6.3V 10% X7R 0402 COMMON
GND

ODT OPTION

FBA_RESET	R535	0 0402 5% NO STUFF	FBA_ODT
FBA_ODT_GPU	R532	0 0402 5% COMMON	
FBC_RESET	R545	0 0402 5% NO STUFF	FBC_ODT
FBC_ODT_GPU	R547	0 0402 5% COMMON	

FBA_ODT → OUT 4.2A< 4.5F<
FBC_ODT → OUT 5.2A< 5.5F<

PLACE THESE RESISTORS AT GPU SIDE

G1
G84-600-A1
BGA820
CHANGED

3/14 FBC

0	FBCD<0>	B7	FBCD0
1	FBCD<1>	A7	FBCD1
2	FBCD<2>	C7	FBCD2
3	FBCD<3>	A2	FBCD3
4	FBCD<4>	B2	FBCD4
5	FBCD<5>	C4	FBCD5
6	FBCD<6>	A5	FBCD6
7	FBCD<7>	B5	FBCD7
8	FBCD<8>	F9	FBCD8
9	FBCD<9>	F10	FBCD9
10	FBCD<10>	D12	FBCD10
11	FBCD<11>	D9	FBCD11
12	FBCD<12>	E12	FBCD12
13	FBCD<13>	D11	FBCD13
14	FBCD<14>	E8	FBCD14
15	FBCD<15>	D8	FBCD15
16	FBCD<16>	E7	FBCD16
17	FBCD<17>	F7	FBCD17
18	FBCD<18>	D6	FBCD18
19	FBCD<19>	D5	FBCD19
20	FBCD<20>	D3	FBCD20
21	FBCD<21>	E4	FBCD21
22	FBCD<22>	C3	FBCD22
23	FBCD<23>	B4	FBCD23
24	FBCD<24>	C10	FBCD24
25	FBCD<25>	B10	FBCD25
26	FBCD<26>	C8	FBCD26
27	FBCD<27>	A10	FBCD27
28	FBCD<28>	C11	FBCD28
29	FBCD<29>	C12	FBCD29
30	FBCD<30>	A11	FBCD30
31	FBCD<31>	B11	FBCD31
32	FBCD<32>	B28	FBCD32
33	FBCD<33>	C27	FBCD33
34	FBCD<34>	C26	FBCD34
35	FBCD<35>	B26	FBCD35
36	FBCD<36>	C30	FBCD36
37	FBCD<37>	B31	FBCD37
38	FBCD<38>	C29	FBCD38
39	FBCD<39>	A31	FBCD39
40	FBCD<40>	D28	FBCD40
41	FBCD<41>	D27	FBCD41
42	FBCD<42>	F26	FBCD42
43	FBCD<43>	D24	FBCD43
44	FBCD<44>	E23	FBCD44
45	FBCD<45>	E26	FBCD45
46	FBCD<46>	E24	FBCD46
47	FBCD<47>	F23	FBCD47
48	FBCD<48>	B23	FBCD48
49	FBCD<49>	A23	FBCD49
50	FBCD<50>	C25	FBCD50
51	FBCD<51>	C23	FBCD51
52	FBCD<52>	A22	FBCD52
53	FBCD<53>	C22	FBCD53
54	FBCD<54>	C21	FBCD54
55	FBCD<55>	B22	FBCD55
56	FBCD<56>	E22	FBCD56
57	FBCD<57>	D22	FBCD57
58	FBCD<58>	D21	FBCD58
59	FBCD<59>	E21	FBCD59
60	FBCD<60>	E18	FBCD60
61	FBCD<61>	D19	FBCD61
62	FBCD<62>	D18	FBCD62
63	FBCD<63>	E19	FBCD63

0	FBCDQM<0>	A4	FBCDQM0
1	FBCDQM<1>	E11	FBCDQM1
2	FBCDQM<2>	F5	FBCDQM2
3	FBCDQM<3>	C9	FBCDQM3
4	FBCDQM<4>	C28	FBCDQM4
5	FBCDQM<5>	F24	FBCDQM5
6	FBCDQM<6>	C24	FBCDQM6
7	FBCDQM<7>	E20	FBCDQM7

B1	FBCDQS0	C5	FBCDQS_WP0
B1	FBCDQS1	E10	FBCDQS_WP1
B1	FBCDQS2	E5	FBCDQS_WP2
B1	FBCDQS3	B8	FBCDQS_WP3
B1	FBCDQS4	A29	FBCDQS_WP4
B1	FBCDQS5	D25	FBCDQS_WP5
B1	FBCDQS6	B25	FBCDQS_WP6
B1	FBCDQS7	F20	FBCDQS_WP7

B1	FBCDQS0*	C6	FBCDQS_RN0
B1	FBCDQS1*	E9	FBCDQS_RN1
B1	FBCDQS2*	E6	FBCDQS_RN2
B1	FBCDQS3*	A8	FBCDQS_RN3
B1	FBCDQS4*	B29	FBCDQS_RN4
B1	FBCDQS5*	E25	FBCDQS_RN5
B1	FBCDQS6*	A25	FBCDQS_RN6
B1	FBCDQS7*	F21	FBCDQS_RN7

FBVTT	AA23	SNN_FBVTT_AA23
FBVTT	AB23	SNN_FBVTT_AB23
FBVTT	H16	SNN_FBVTT_H16
FBVTT	H17	SNN_FBVTT_H17
FBVTT	J10	SNN_FBVTT_J10
FBVTT	J23	SNN_FBVTT_J23
FBVTT	J24	SNN_FBVTT_J24
FBVTT	J9	SNN_FBVTT_J9
FBVTT	K11	SNN_FBVTT_K11
FBVTT	K12	SNN_FBVTT_K12
FBVTT	K21	SNN_FBVTT_K21
FBVTT	K22	SNN_FBVTT_K22
FBVTT	K24	SNN_FBVTT_K24
FBVTT	K9	SNN_FBVTT_K9
FBVTT	L23	SNN_FBVTT_L23
FBVTT	M23	SNN_FBVTT_M23
FBVTT	T25	SNN_FBVTT_T25
FBVTT	U25	SNN_FBVTT_U25

FBC_CMD0	C13	FBC_A<3>	3
FBC_CMD1	A16	FBC_A<0>	0
FBC_CMD2	A13	FBC_A<2>	2
FBC_CMD3	B17	FBC_A<1>	1
FBC_CMD4	B20	FBD_A<3>	3
FBC_CMD5	A19	FBD_A<4>	4
FBC_CMD6	B19	FBD_A<5>	5
FBC_CMD7	B14	FBC_BA2	
FBC_CMD8	E16	FBC_CS0*	
FBC_CMD9	A14	FBC_WE*	
FBC_CMD10	C15	FBC_BA0	
FBC_CMD11	B16	FBC_CKE	
FBC_CMD12	F17	FBC_RESET	
FBC_CMD13	C19	FBD_A<2>	2
FBC_CMD14	D15	FBC_A<12>	12
FBC_CMD15	C17	FBC_RAS*	
FBC_CMD16	A17	FBC_A<11>	11
FBC_CMD17	C16	FBC_A<10>	10
FBC_CMD18	D14	FBC_BA1	
FBC_CMD19	F16	FBC_A<8>	8
FBC_CMD20	C14	FBC_A<9>	9
FBC_CMD21	C18	FBC_A<6>	6
FBC_CMD22	E14	FBC_A<5>	5
FBC_CMD23	B13	FBC_A<7>	7
FBC_CMD24	E15	FBC_A<4>	4
FBC_CMD25	F15	FBC_CAS*	
FBC_CMD26	A20	SNN_FBC_CMD26	
FBC_CMD27	C20	SNN_FBC_CMD27	
FBC_CMD28	A15	SNN_FBC_CMD28	

FBD_A<5..2> → FBD_A<3>, FBD_A<4>, FBD_A<5>, FBD_A<2>
FBC_A<12..0> → FBC_A<3>, FBC_A<0>, FBC_A<2>, FBC_A<1>, FBD_A<3>, FBD_A<4>, FBD_A<5>, FBD_A<2>, FBC_A<12>, FBC_RAS*, FBC_A<11>, FBC_A<10>, FBC_BA1, FBC_A<8>, FBC_A<9>, FBC_A<6>, FBC_A<5>, FBC_A<7>, FBC_A<4>, FBC_CAS*

FBC_CLK0	E13	FBC_CLK0	5.3A< 5.3F<
FBC_CLK0	F13	FBC_CLK0*	5.3B< 5.4F<
FBC_CLK1	F18	FBC_CLK1	5.3C< 5.4F<
FBC_CLK1	E17	FBC_CLK1*	5.3E< 5.4F<
FBC_DEBUG	F12	FBC_ODT_GPU	

FBC_PLLVDD	G8	SNN_FBC_PLLVDD	
FBC_PLLAVDD	G10	FBC_PLLAVDD	
FBC_PLLGND	G9		

PLACE CLOSE TO BALLS
FBC_PLLAVDD — 12MIL — 1.2V — LB503 COMMON — 220R@100MHz BEAD_0603 — PEX1V2

C660	470PF	16V 10% X7R 0402 COMMON
C659	.01UF	16V 10% X7R 0402 COMMON
C646	4.7UF	6.3V 10% X5R 0603 COMMON

GND

FBCAL_PD_VDDQ	K26	FBCAL_PD	R539 40.2 1% 0402 COMMON
FBCAL_PU_GND	H26	FBCAL_PU	R541 40.2 1% 0402 COMMON
FBCAL_TERM_GND	J26	FBCAL_TERM	R534 40.2 1% 0402 NO STUFF

FBVDDQ, GND

FBVDDQ
R533 1K 1% 0402 NO STUFF
FB_VREF2 — 12MIL — A28 — FB_VREF2
R543 1K 1% 0402 NO STUFF
C561 .1UF 6.3V 10% X7R 0402 COMMON
GND

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	Frame Buffer GPU Interface

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2701 SAN TOMAS EXPRESSWAY
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NV_PN	600-10407-0001-300 A		
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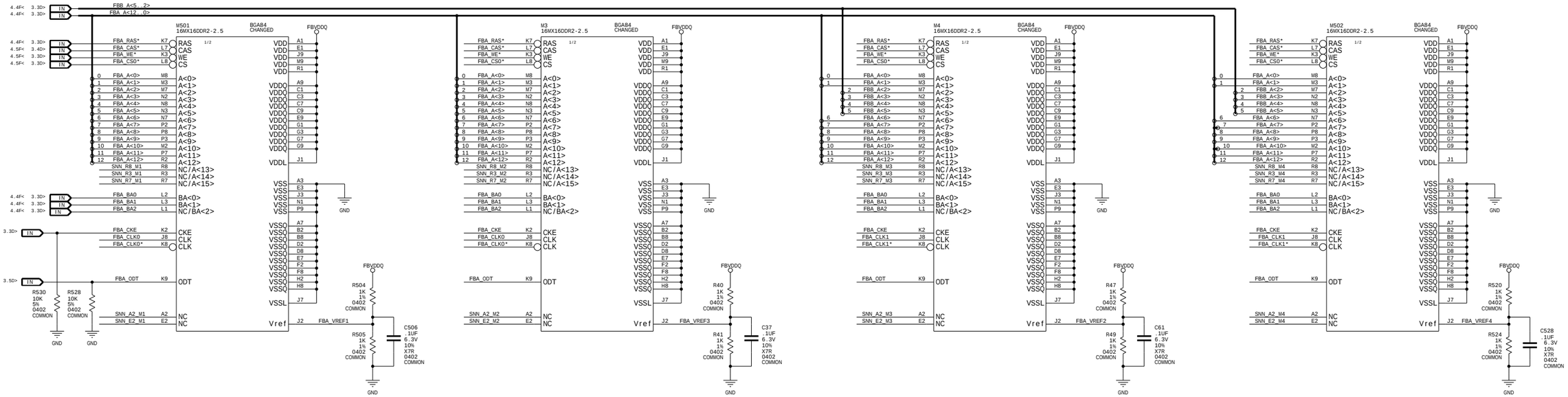
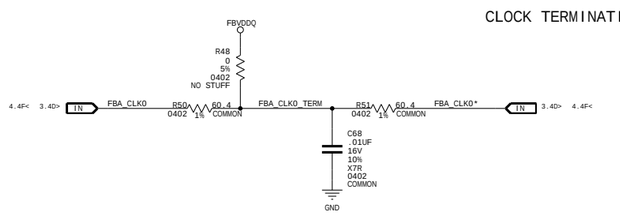
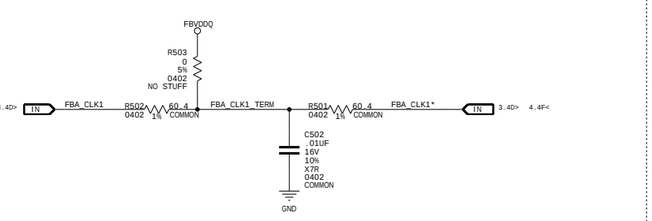
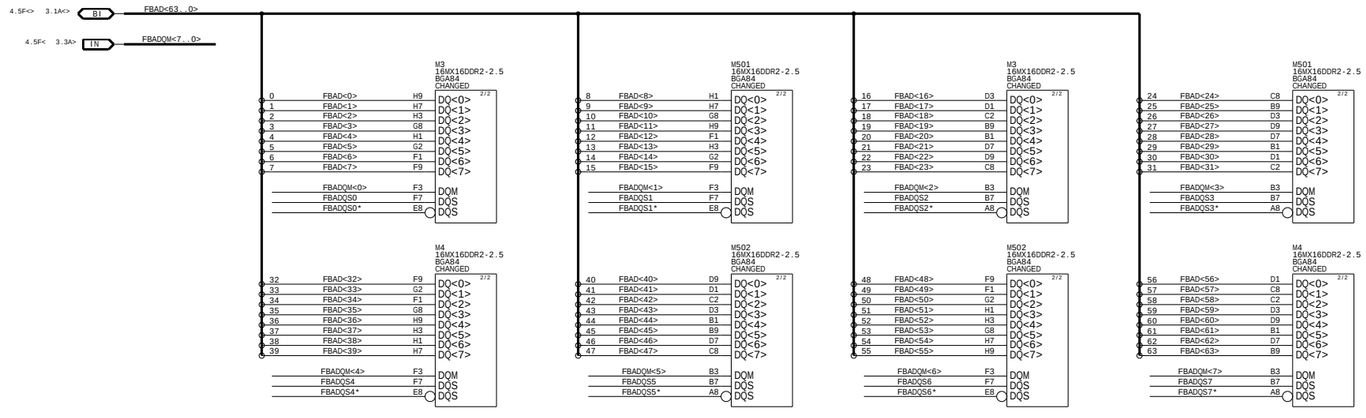
PAGE 4) MEMORY PARTITION A



CLOCK TERMINATIONS







NET	MIN_LINE_WIDTH	VOLTAGE
FBA_VREF1	16MIL	0.9V
FBA_VREF2	16MIL	0.9V
FBA_VREF3	16MIL	0.9V
FBA_VREF4	16MIL	0.9V

NET	DIFFPAIR	CRITICAL	IMPEDANCE
FBA_CLK0	FBA_CLK0	1	100DIFF
FBA_CLK0*	FBA_CLK0	1	100DIFF
FBA_CLK1	FBA_CLK1	1	100DIFF
FBA_CLK1*	FBA_CLK1	1	100DIFF
FBADQS0	FBADQS0	1	100DIFF
FBADQS0*	FBADQS0	1	100DIFF
FBADQS1	FBADQS1	1	100DIFF
FBADQS1*	FBADQS1	1	100DIFF
FBADQS2	FBADQS2	1	100DIFF
FBADQS2*	FBADQS2	1	100DIFF
FBADQS3	FBADQS3	1	100DIFF
FBADQS3*	FBADQS3	1	100DIFF
FBADQS4	FBADQS4	1	100DIFF
FBADQS4*	FBADQS4	1	100DIFF
FBADQS5	FBADQS5	1	100DIFF
FBADQS5*	FBADQS5	1	100DIFF
FBADQS6	FBADQS6	1	100DIFF
FBADQS6*	FBADQS6	1	100DIFF
FBADQS7	FBADQS7	1	100DIFF
FBADQS7*	FBADQS7	1	100DIFF
FBA_A<12..0>		2	56OHM
FBB_A<5..2>		2	56OHM
FBA_BA0		2	56OHM
FBA_BA1		2	56OHM
FBA_CKE		2	56OHM
FBA_BA2		2	56OHM
FBA_RAS*		2	56OHM
FBA_CAS*		2	56OHM
FBA_WE*		2	56OHM
FBA_CS0*		2	56OHM
FBA_CS1*		2	56OHM
FBAD<63..0>		2	50OHM
FBADQM<7..0>		2	50OHM
FBA_ODT		2	56OHM

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	Frame Buffer Partition A Memories

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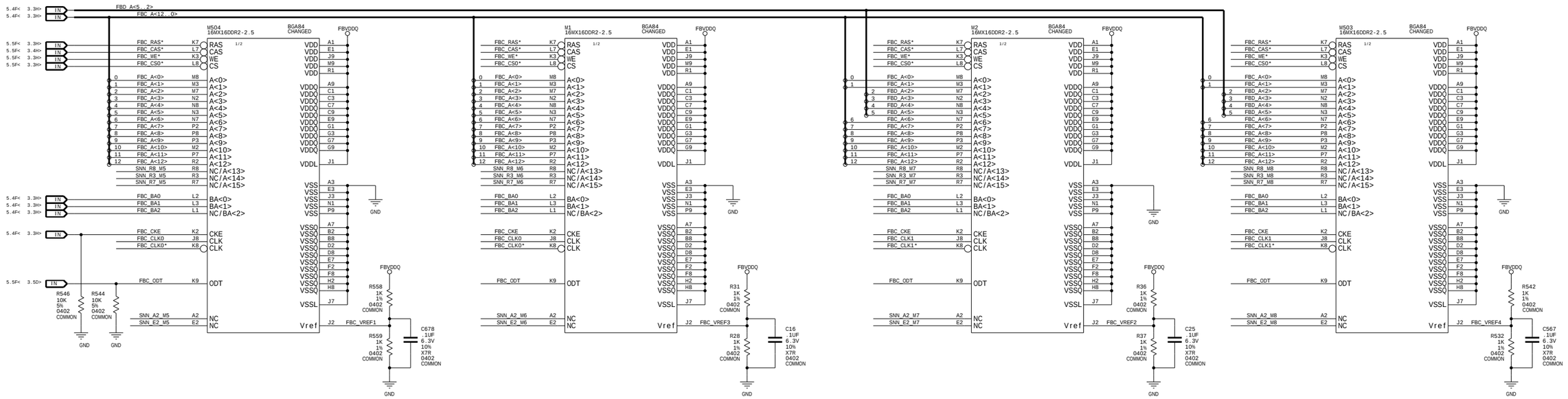
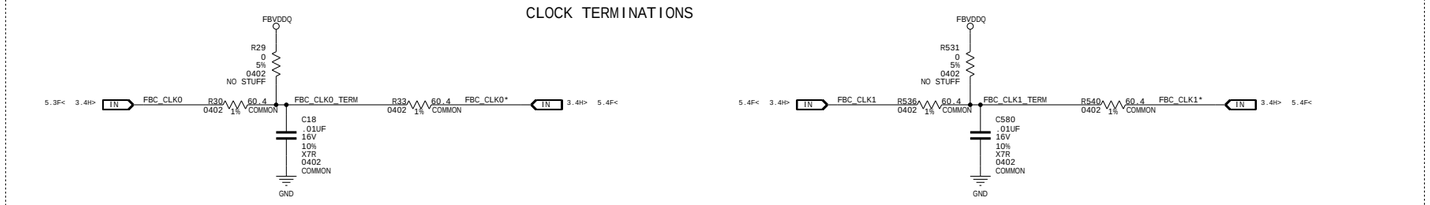
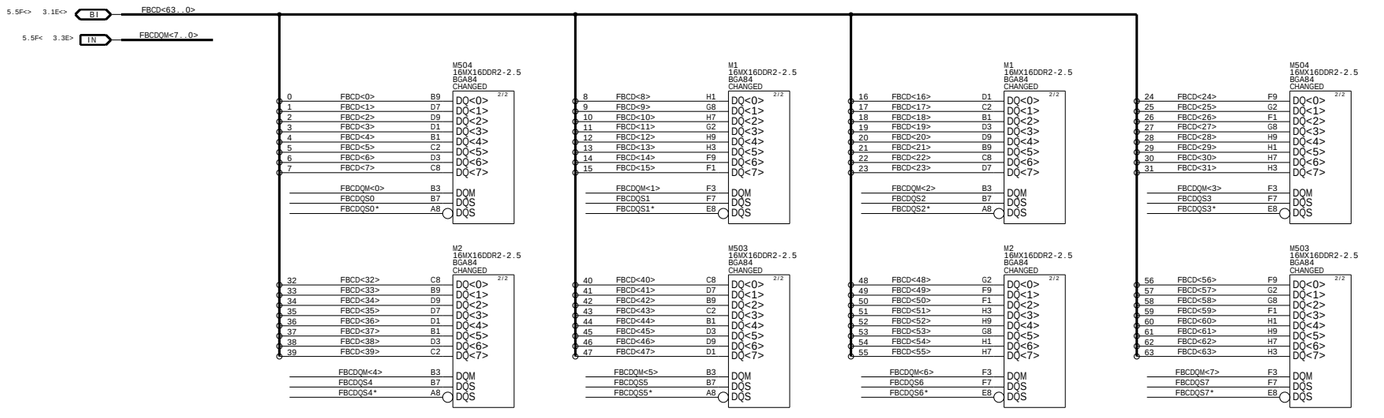
PAGE 5) MEMORY PARTITION C



CLOCK TERMINATIONS





NET	MIN_LINE_WIDTH	VOLTAGE
FBC_VREF1	16MIL	0.9V
FBC_VREF2	16MIL	0.9V
FBC_VREF3	16MIL	0.9V
FBC_VREF4	16MIL	0.9V

NET	DIFFPAIR	CRITICAL	IMPEDANCE
FBC_CLK0	FBC_CLK0	1	100DIFF
FBC_CLK0*	FBC_CLK0	1	100DIFF
FBC_CLK1	FBC_CLK1	1	100DIFF
FBC_CLK1*	FBC_CLK1	1	100DIFF
FBCDQS0	FBCDQS0	1	100DIFF
FBCDQS0*	FBCDQS0	1	100DIFF
FBCDQS1	FBCDQS1	1	100DIFF
FBCDQS1*	FBCDQS1	1	100DIFF
FBCDQS2	FBCDQS2	1	100DIFF
FBCDQS2*	FBCDQS2	1	100DIFF
FBCDQS3	FBCDQS3	1	100DIFF
FBCDQS3*	FBCDQS3	1	100DIFF
FBCDQS4	FBCDQS4	1	100DIFF
FBCDQS4*	FBCDQS4	1	100DIFF
FBCDQS5	FBCDQS5	1	100DIFF
FBCDQS5*	FBCDQS5	1	100DIFF
FBCDQS6	FBCDQS6	1	100DIFF
FBCDQS6*	FBCDQS6	1	100DIFF
FBCDQS7	FBCDQS7	1	100DIFF
FBCDQS7*	FBCDQS7	1	100DIFF

NET		CRITICAL	IMPEDANCE
FBC_A<12..0>		2	56OHM
FBD_A<5..2>		2	56OHM
FBC_BA0		2	56OHM
FBC_BA1		2	56OHM
FBC_CKE		2	56OHM
FBC_BA2		2	56OHM
FBC_RAS*		2	56OHM
FBC_CAS*		2	56OHM
FBC_WE*		2	56OHM
FBC_CS0*		2	56OHM
FBC_CS1*		2	56OHM
FBCD<63..0>		2	50OHM
FBCDQM<7..0>		2	50OHM
FBC_ODT		2	56OHM

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	Frame Buffer Partition C Memories

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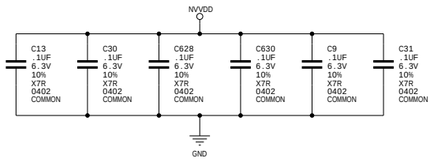
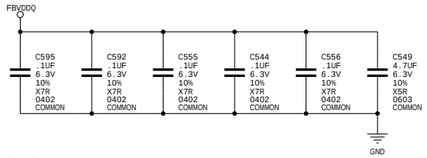
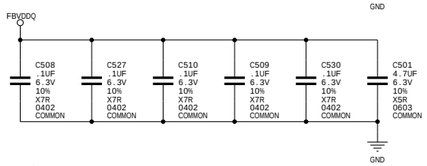
PAGE 6) MEMORY DECOUPLING CAPS

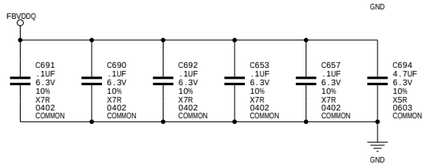
DECOUPLING CAPS FOR MEMORYS (PARTION A AND PARTION C)

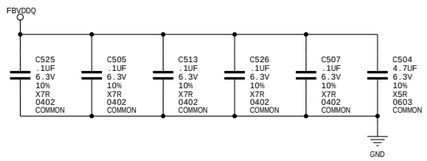


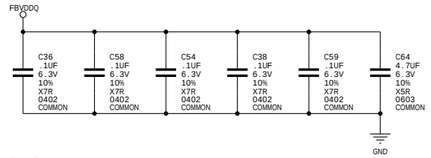
NVVDD TRANSITION CAP NEAR BY PARTION A

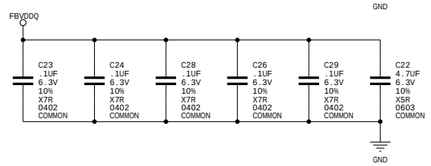


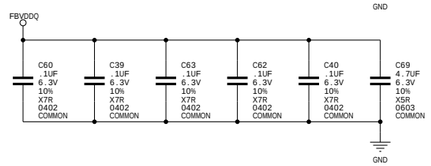


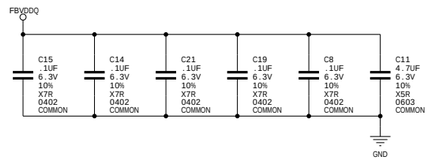


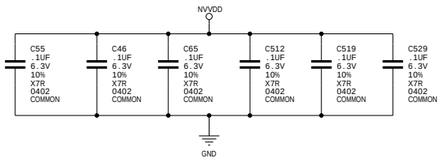












NVVDD TRANSITION CAP NEAR BY PARTION C

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	Memory Decoupling Caps

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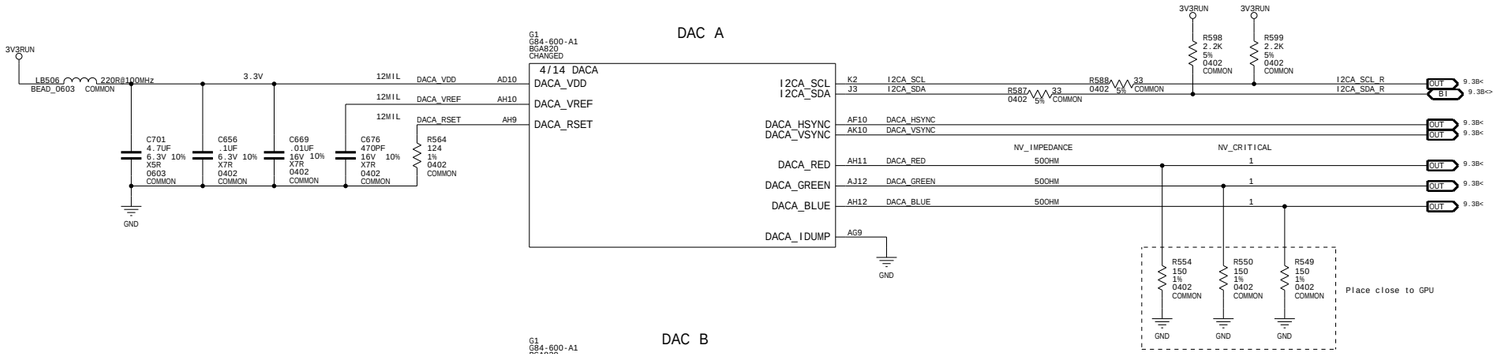
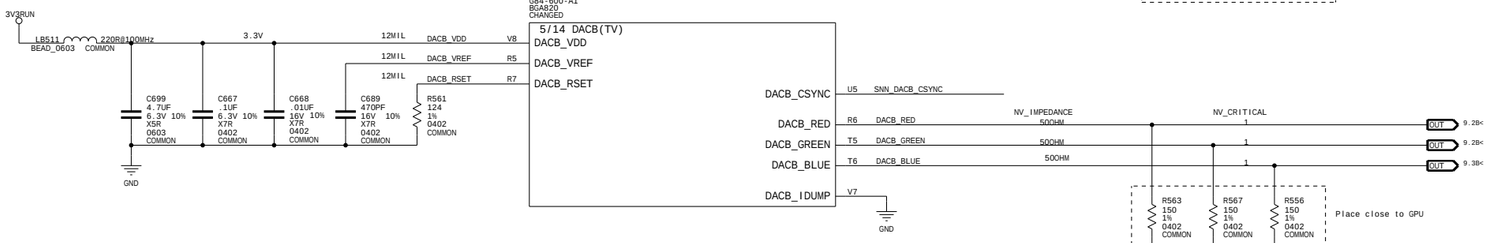
PAGE 7) DAC_A, DAC_B, DAC_C, PLL, CRYSTAL

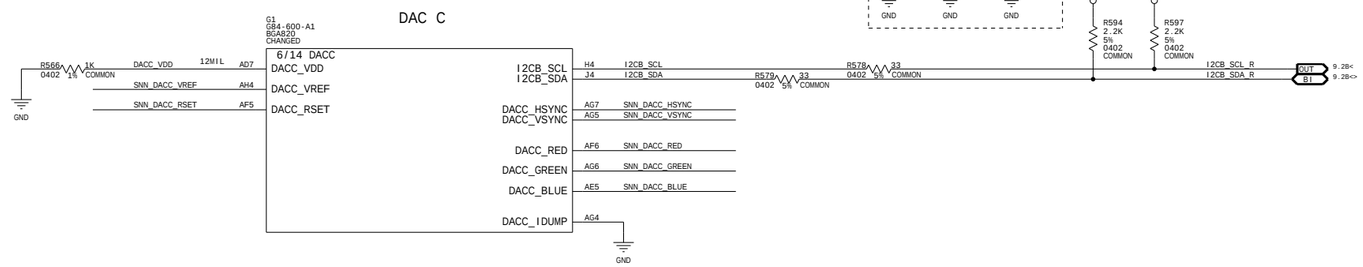
DAC A



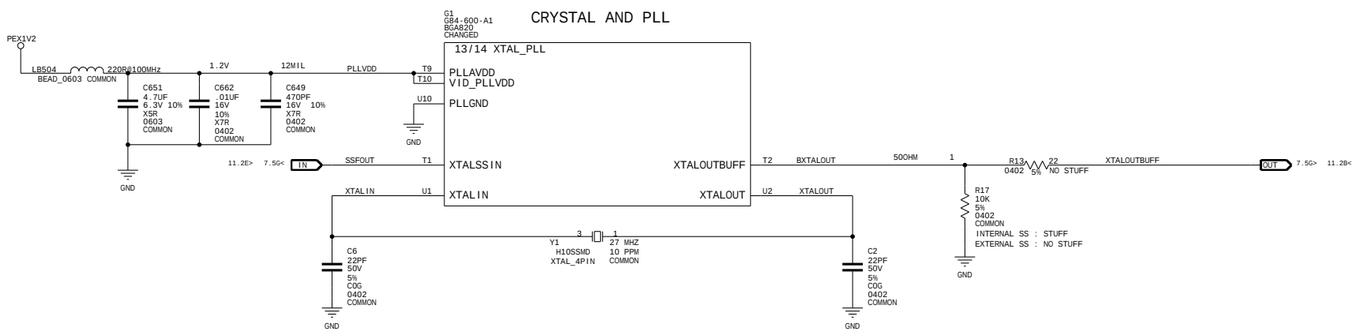
DAC B



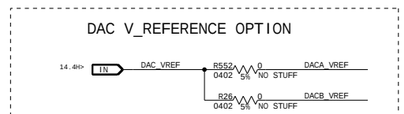
DAC C



CRYSTAL AND PLL



DAC V_REFERENCE OPTION



NV_NET_NAME	NV_IMPEDANCE	NV_CRITICAL_NET
OUT XTALOUT	500HM	1
IN XTALIN	500HM	1
11.2B< 7.4F> OUT XTALOUTBUFF	500HM	1
11.2E> 7.4C< IN SSFOUT	500HM	1

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	DACs, Clock-Generation

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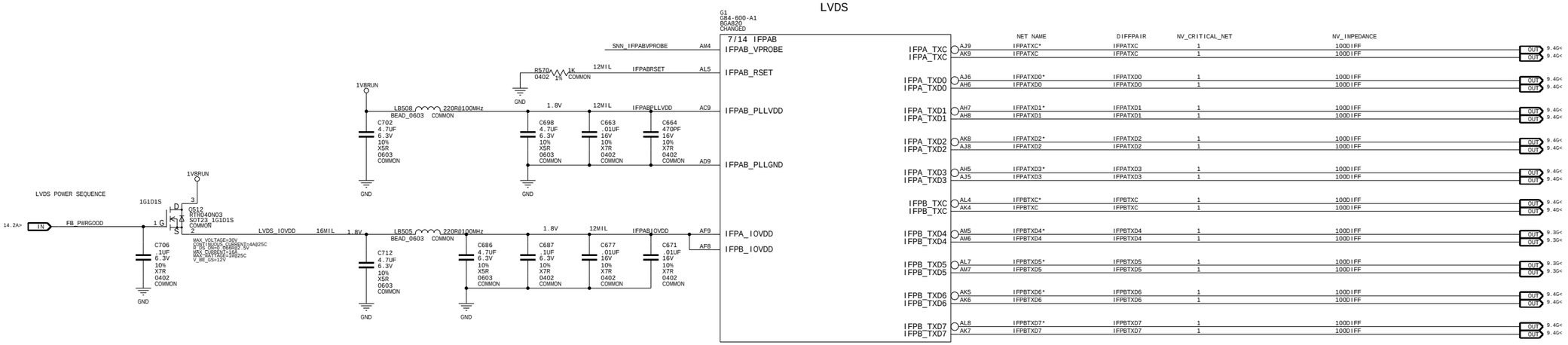
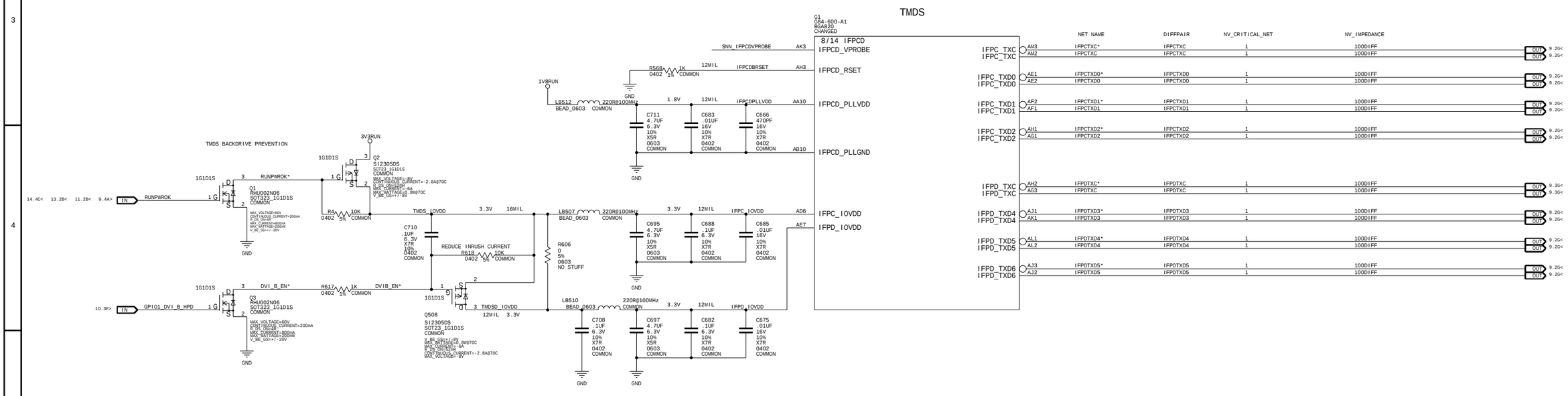
PAGE 8) LVDS(LINK A/B), TMDS(LINK C/D)

LVDS



TMDS



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	LVDS, TMDS GPU Interface

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PAGE 9) MXM CONNECTOR

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
3V3RUN	3.3V	12MIL	1.5A
1V8RUN	1.8V	12MIL	3.5A
2V5RUN	2.5V	12MIL	0.5A
5VRUN	5V	16MIL	0.5A
PWR_SRC	22V	16MIL	4A
GND	0V	12MIL	50A

OUT SPDIF 50OHM 1

2.5G< OUT SPDIF_IN 50OHM 1
9.4B>

MXM CONNECTOR

CN1
CON_MXM_X16_EDGE
(N,NON)PHY(-X16,-HE)_SLI
NPHY-X16_SLI
NO STUFF

2/2 IO - LVDS,DVI,VGA,TV

10.3H< OUT DVI_A_HPD 217 — DVI_A_HPD
7.3G> IN I2CB_SCL_R 232 — DDCB_SCLK
7.3G<> BI I2CB_SDA_R 230 — DDCB_SDATA

DVI-A: DVI_A_CLK / DVI_A_CLK; DVI_A_TX0 / DVI_A_TX0; DVI_A_TX1 / DVI_A_TX1; DVI_A_TX2 / DVI_A_TX2

10.3H< OUT DVI_B_HPD 193 — DVI_B_HPD

DVI-B: DVI_B_TX2 / DVI_B_TX2; DVI_B_TX1 / DVI_B_TX1; DVI_B_TX0 / DVI_B_TX0; DVI_B_CLK / DVI_B_CLK

SDTV / HDTV

7.2F> IN DACB_GREEN 140 — TV_Y / HDTV_Y
7.2F> IN DACB_RED 136 — TV_C / HDTV_Pr
7.3F> IN DACB_BLUE 144 — TV_CVBS / HDTV_Pb

SLI: DR_RASTER_SYNC / DR_SWAP_RDY; DR_D0 … DR_D14; DR_CMD; DR_REFCLK; DR_CLK

7.1F> IN DACA_VSYNC 153 — VSYNC
7.1F> IN DACA_HSYNC 151 — HSYNC
7.1F> IN DACA_RED 148 — VGA_RED
7.1F> IN DACA_GREEN 152 — VGA_GRN
7.2F> IN DACA_BLUE 156 — VGA_BLU
7.1F> IN I2CA_SCL_R 155 — DDCA_SCLK
7.1F<> BI I2CA_SDA_R 157 — DDCA_SDATA

GND

10.3F> IN GPIO3_PPEN 224 — LVDS_PPEN
10.3F> IN GPIO4_BLEN 228 — LVDS_BLEN
10.3F> IN GPIO2_BL_PWM 226 — LVDS_BL_BRGHT

11.2B< 10.3F> IN I2CC_SCL_R 222 — DDCC_SCLK
11.2B<> 10.3F<> BI I2CC_SDA_R 220 — DDCC_SDATA

10.2A<> BI SMB_DAT 145 — SMB_DAT
10.2A< OUT SMB_CLK 147 — SMB_CLK

10.2F> IN THERM_ALERT* 149 — THERM

14.4C< 13.2B< 11.2B< 8.4A< OUT RUNPWROK — R39 1K 0402 1% COMMON — RUNPWROK_IN 16 — RUNPWROK
10.3F< OUT GPIO_AC_BATT* 169 — AC/BATT*

C33 1000PF 50V 10% X7R 0402 COMMON

2.5G< 9.1G> OUT SPDIF_IN — R565 49.9 0402 1% COMMON — SPDIF 170 — SPDIF

GND

ESD Protection for MOSFET Gates

IFPCTXC* 219 — IN 8.3H>
IFPCTXC 221 — IN 8.3H>
IFPCTXD0* 237 — IN 8.3H>
IFPCTXD0 239 — IN 8.3H>
IFPCTXD1* 231 — IN 8.3H>
IFPCTXD1 233 — IN 8.3H>
IFPCTXD2* 225 — IN 8.4H>
IFPCTXD2 227 — IN 8.4H>

IFPDTXD5* 201 — IN 8.4H>
IFPDTXD5 203 — IN 8.4H>
IFPDTXD4* 207 — IN 8.4H>
IFPDTXD4 209 — IN 8.4H>
IFPDTXD3* 213 — IN 8.4H>
IFPDTXD3 215 — IN 8.4H>
IFPDTXC* 189 — IN 8.4H>
IFPDTXC 191 — IN 8.4H>

SLI_D<0> 185 — 0 — SLI_D<14..0> — BI 12.1F<> 15.4B>
SLI_D<1> 183 — 1
SLI_D<2> 181 — 2
SLI_D<3> 179 — 3
SLI_D<4> 177 — 4
SLI_D<5> 175 — 5
SLI_D<6> 173 — 6
SLI_D<7> 167 — 7
SLI_D<8> 165 — 8
SLI_D<9> 163 — 9
SLI_D<10> 161 — 10
SLI_D<11> 159 — 11
SLI_D<12> 187 — 12
SLI_D<13> 195 — 13
SLI_D<14> 197 — 14

SLI_DE 143 — BI 12.2F<>
SLI_REFCLK 141 — BI 12.4F<>
SLI_CLKOUT 171 — BI 12.2F<>

2V5RUN 2V5RUN
R25 10K 5% 0402 COMMON
R19 10K 5% 0402 COMMON
R16 1K 0402 1% COMMON — GPIO_SLI_SYNC — BI 10.3F<>
R15 1K 0402 1% COMMON — SLI_SWAP_OUT — BI 11.4C<>

PLACE THESE COMPONENTS TO ISOLATE
2 TYPE SIGNALS AND BALANCE THE LOAD
OF THE DIFF PAIR

LVDS_UTX0 / LVDS_UTX0: IFPBTXD4 186 / IFPBTXD4* 184 — IN 8.2H>
LVDS_UTX1 / LVDS_UTX1: IFPBTXD5 180 / IFPBTXD5* 178 — IN 8.2H>
LVDS_UTX2 / LVDS_UTX2: IFPBTXD6 174 / IFPBTXD6* 172 — IN 8.2H>
LVDS_UTX3 / LVDS_UTX3: IFPBTXD7 168 / IFPBTXD7* 166 — IN 8.2H>
LVDS_UCLK / LVDS_UCLK: IFPBTXC 162 / IFPBTXC* 160 — IN 8.2H>

LVDS_LTX0 / LVDS_LTX0: IFPATXD0 216 / IFPATXD0* 214 — IN 8.1H>
LVDS_LTX1 / LVDS_LTX1: IFPATXD1 210 / IFPATXD1* 208 — IN 8.1H>
LVDS_LTX2 / LVDS_LTX2: IFPATXD2 204 / IFPATXD2* 202 — IN 8.2H>
LVDS_LTX3 / LVDS_LTX3: IFPATXD3 198 / IFPATXD3* 196 — IN 8.2H>
LVDS_LCLK / LVDS_LCLK: IFPATXC 192 / IFPATXC* 190 — IN 8.1H>

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	MXM Connector, IO-Section

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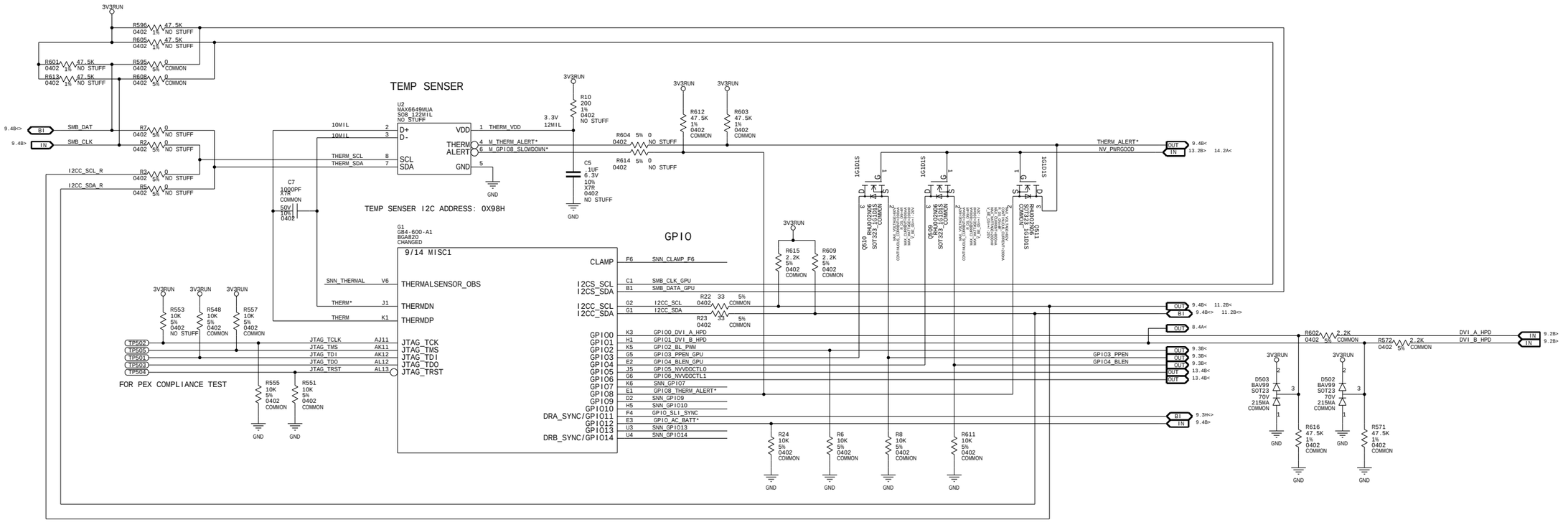
PAGE 10) GPIO, JTAG, TEMP SENSOR



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	GPIOs. JTAG, Thermal Senser

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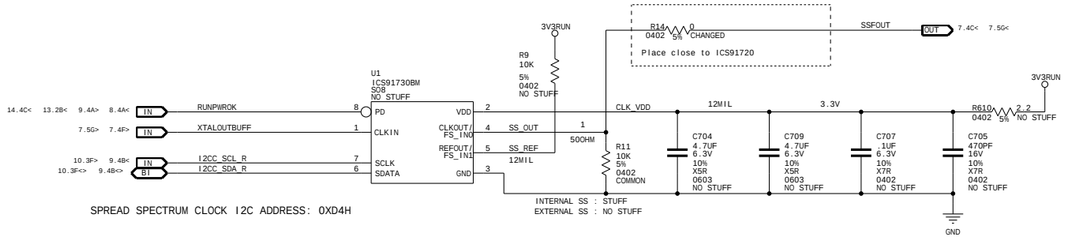
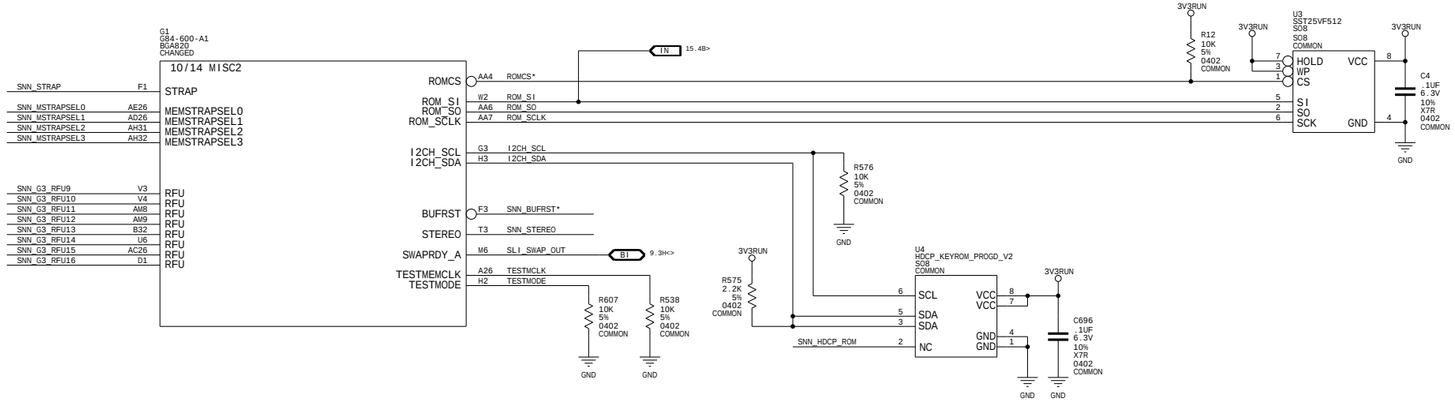
NAME	myan	DATE	21-DEC-2006

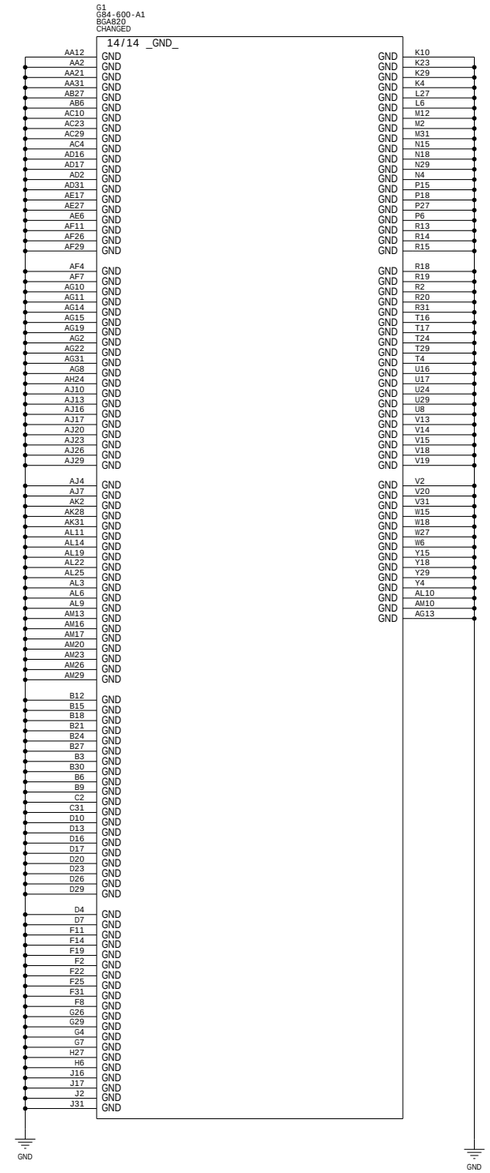
PAGE 11) SPREAD SPECTRUM, VBIOS, HDCP BIOS, GPU GND

SPREAD SPECTRUM



VBIOS AND HDCP ROM





ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	Spread Spectrum, VBIOS and HDCP ROM

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NV_PN	600-10407-0001-300 A		
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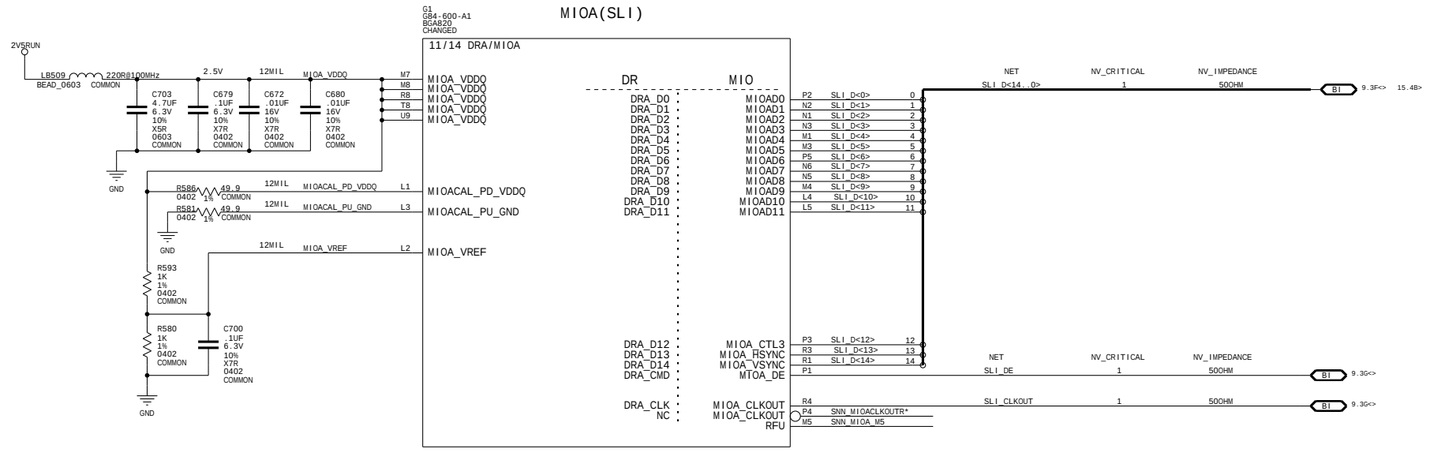
PAGE 12) MIOA(SLI), MIOB



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	MIOA(SLI), MIOB

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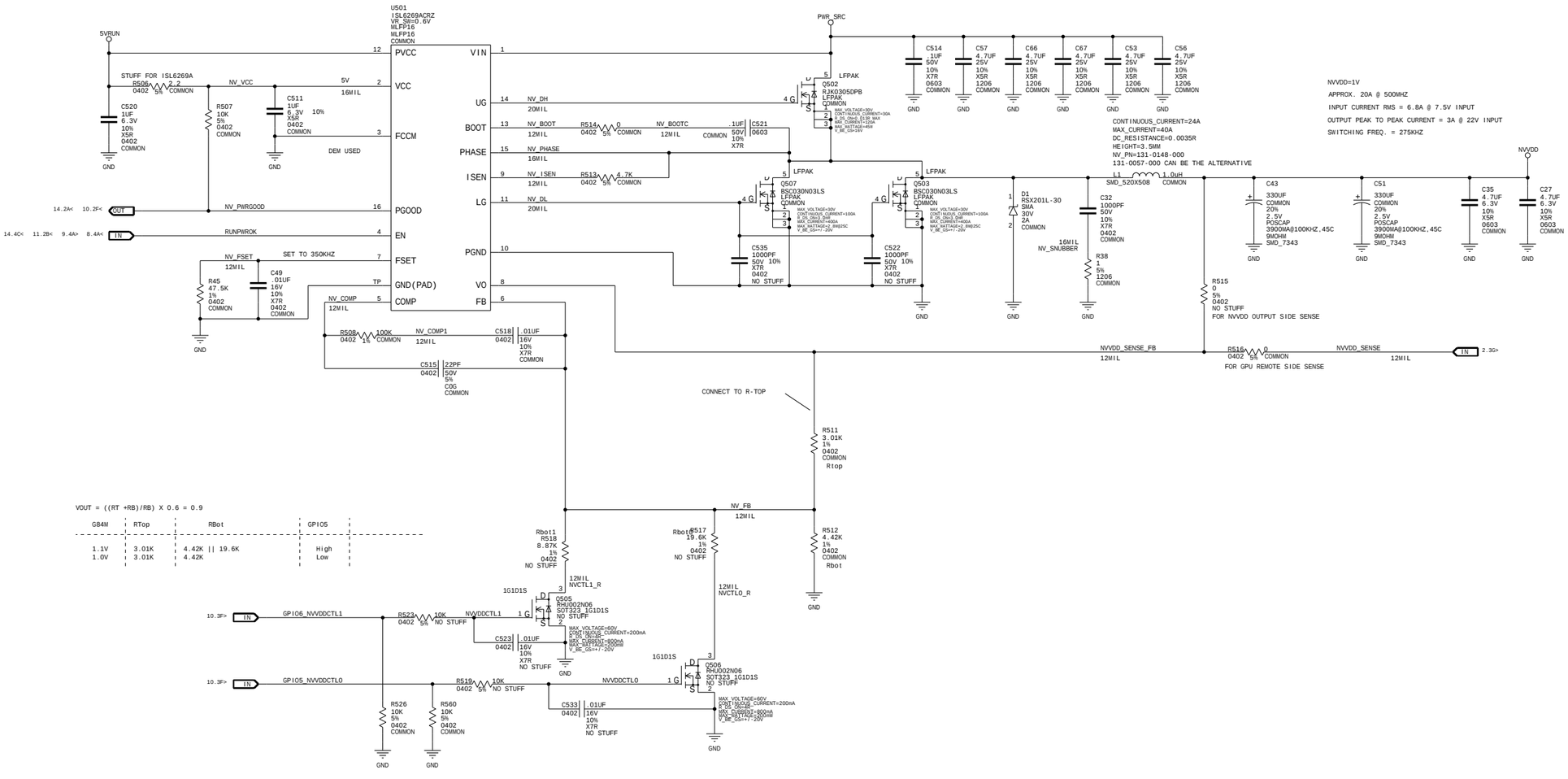
PAGE 13) NVVDD POWER SUPPLY

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
NVVDD — NVVDD	1V	12MIL	30A — NVVDD

NVVDD SWITCHER POWER SUPPLY



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	NVVDD Power Supply

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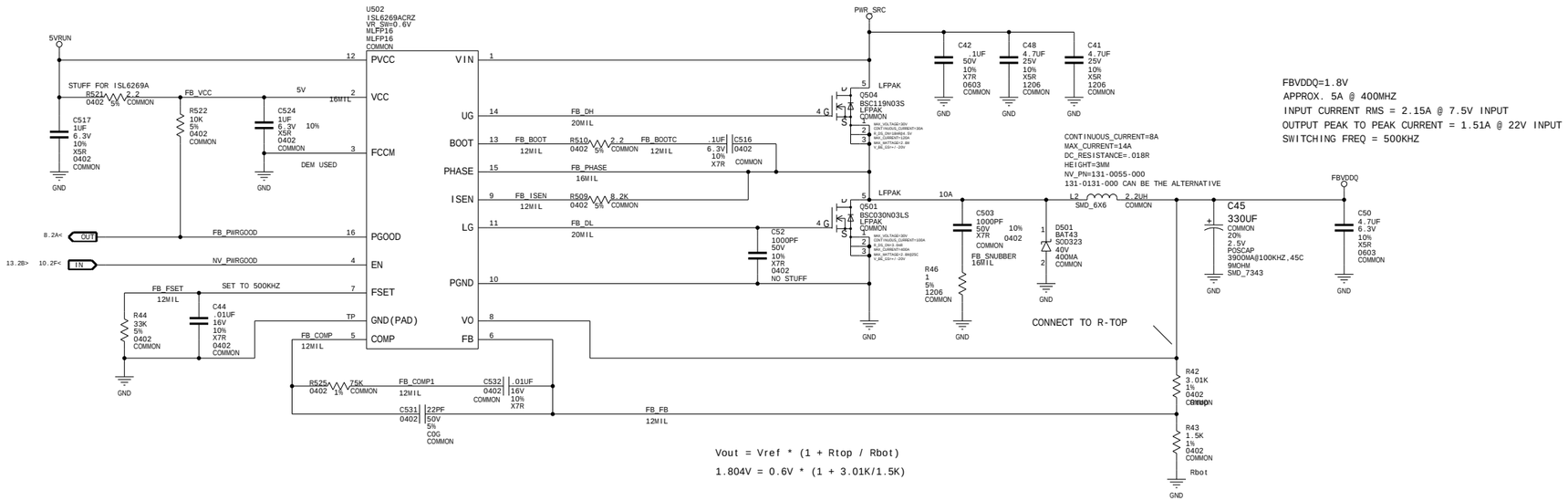
PAGE 14) FBVDDQ AND PEX1V2 POWER SUPPLY

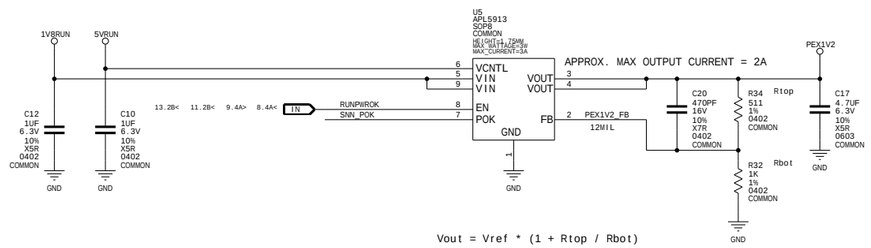
NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
PEX1V2 — PEX1V2	1.2V	12MIL	2A
FBVDDQ — FBVDDQ	1.8V	12MIL	10A

FBVDDQ SWITCHER POWER SUPPLY

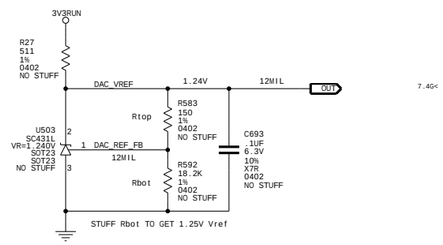


FBVDDQ=1.8V
APPROX. 5A @ 400MHZ
INPUT CURRENT RMS = 2.15A @ 7.5V INPUT
OUTPUT PEAK TO PEAK CURRENT = 1.51A @ 22V INPUT
SWITCHING FREQ = 500KHZ

PEX1V2 LINEAR SUPPLY



DAC V_REFERENCE SUPPLY



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	FBVDDQ, PEX1V2 and DAC_Vref Power Supply

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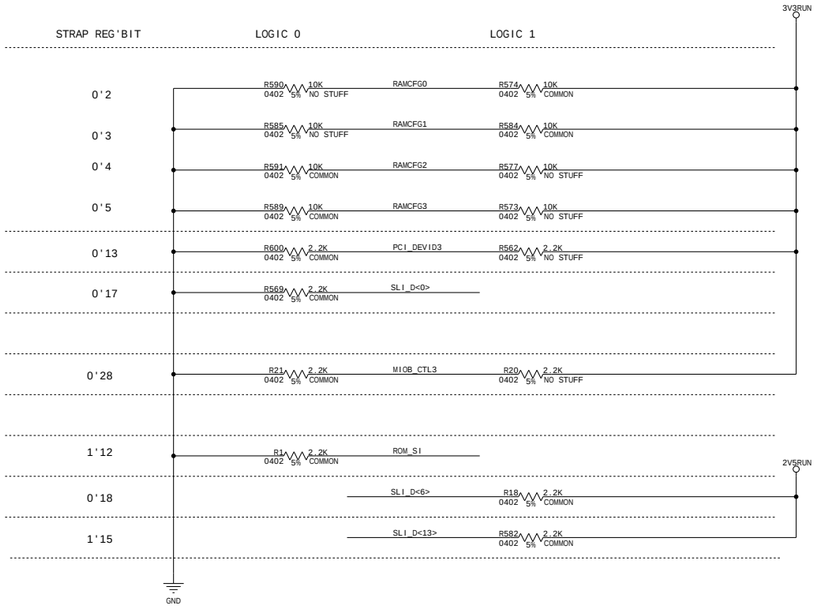
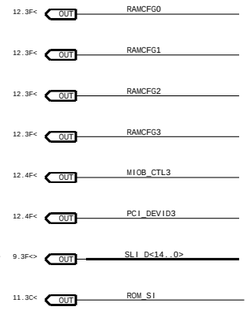
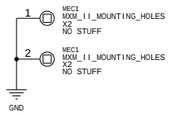
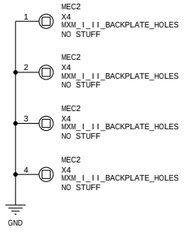
PAGE 15) STRAPS, MOUNTING HOLES



RAM_CFG_0	RAM_CFG[3:0] MS_0000: 16Mx16 DDR2 128bit SDRAM, ELPIDA. MS_0001: 16Mx16 DDR2 128bit SDRAM, SAMSUNG, MICRON. MS_0010: 16Mx16 DDR2 128bit SDRAM. INFINEON. MS_0011: 16Mx16 DDR2 128bit SDRAM, HYNIX. MS_0100: 32Mx16 DDR2 128bit SDRAM, ELPIDA. MS_0101: 32Mx16 DDR2 128bit SDRAM, SAMSUNG, MICRON. MS_0110: 32Mx16 DDR2 128bit SDRAM. INFINEON. MS_0111: 32Mx16 DDR2 128bit SDRAM, HYNIX.
RAM_CFG_1	
RAM_CFG_2	
RAM_CFG_3	
PCI_DEVID_3	MS_0: DEVICE ID = 0x0407, G84M-600. MS_1: DEVICE ID = 0x0408: G84M-700 MS_1: DEVICE ID = 0x0428: G86M-700
PEX_PLL_EN_TERM100	
PCI_DEVID_EXT	
MIOA_EN_3.3V	
3GIO_PADCFG_LUT_ADR[0]	
SLOT CLOCK CONFIGURATION	







ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
PAGE DETAIL	STRAPS, TTP, MOUNTING HOLE

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NV_PN	600-10407-0001-300 A		
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Title: Basenet Report
Design: p555_a00
Date: Nov 30 11:00:17 2006

Base nets and synonyms for p407_lib.P555_A00(@p407_lib.p555_a00(sch_1))

Base Signal	Location([Zone][dir])
1V8RUN	9.1G
2V5RUN	9.1G
3V3RUN	9.1G
5VRUN	9.1G
BXTALOUT	7.4D
CLK_VDD	11.2C
DACA_BLUE	7.2F> 9.3B<
DACA_GREEN	7.1F> 9.3B<
DACA_HSYNC	7.1F> 9.3B<
DACA_RED	7.1F> 9.3B<
DACA_RSET	7.1C
DACA_VDD	7.1C
DACA_VREF	7.1C 7.4H
DACA_VSYNC	7.1F> 9.3B<
DACB_BLUE	7.3F> 9.3B<
DACB_GREEN	7.2F> 9.2B<
DACB_RED	7.2F> 9.2B<
DACB_RSET	7.2C
DACB_VDD	7.2C
DACB_VREF	7.2C 7.4H
DACC_VDD	7.3C
DAC_REF_FB	14.4G
DAC_VREF	7.4G< 14.4H>
DVIB_EN*	8.4B
DVI_A_HPD	9.2B> 10.3H<
DVI_B_EN*	8.4B
DVI_B_HPD	9.2B> 10.3H<
FBAD<0>	3.1A 4.4B
FBAD<63..0>	3.1A<> 4.4A<> 4.5F<>
FBAD<1>	3.1A 4.4B
FBAD<2>	3.1A 4.4B
FBAD<3>	3.1A 4.4B
FBAD<4>	3.1A 4.4B
FBAD<5>	3.1A 4.4B
FBAD<6>	3.1A 4.4B
FBAD<7>	3.1A 4.4B
FBAD<8>	3.1A 4.4C
FBAD<9>	3.1A 4.4C
FBAD<10>	3.1A 4.4C
FBAD<11>	3.1A 4.4C
FBAD<12>	3.1A 4.4C
FBAD<13>	3.1A 4.4C
FBAD<14>	3.1A 4.4C
FBAD<15>	3.1A 4.4C
FBAD<16>	3.1A 4.4D
FBAD<17>	3.2A 4.4D
FBAD<18>	3.2A 4.4D
FBAD<19>	3.2A 4.4D
FBAD<20>	3.2A 4.4D
FBAD<21>	3.2A 4.4D
FBAD<22>	3.2A 4.4D
FBAD<23>	3.2A 4.4D
FBAD<24>	3.2A 4.4D
FBAD<25>	3.2A 4.4D
FBAD<26>	3.2A 4.4D
FBAD<27>	3.2A 4.4D
FBAD<28>	3.2A 4.4D
FBAD<29>	3.2A 4.4D
FBAD<30>	3.2A 4.4D
FBAD<31>	3.2A 4.4D
FBAD<32>	3.2A 4.5B
FBAD<33>	3.2A 4.5B
FBAD<34>	3.2A 4.5B
FBAD<35>	3.2A 4.5B
FBAD<36>	3.2A 4.5B
FBAD<37>	3.2A 4.5B
FBAD<38>	3.2A 4.5B
FBAD<39>	3.2A 4.5B
FBAD<40>	3.2A 4.5C
FBAD<41>	3.2A 4.5C
FBAD<42>	3.2A 4.5C
FBAD<43>	3.2A 4.5C
FBAD<44>	3.2A 4.5C
FBAD<45>	3.2A 4.5C
FBAD<46>	3.2A 4.5C
FBAD<47>	3.3A 4.5C
FBAD<48>	3.3A 4.5D
FBAD<49>	3.3A 4.5D
FBAD<50>	3.3A 4.5D
FBAD<51>	3.3A 4.5D
FBAD<52>	3.3A 4.5D
FBAD<53>	3.3A 4.5D
FBAD<54>	3.3A 4.5D
FBAD<55>	3.3A 4.5D
FBAD<56>	3.3A 4.5D
FBAD<57>	3.3A 4.5D
FBAD<58>	3.3A 4.5D

FBAD<59>	3.3A 4.5D
FBAD<60>	3.3A 4.5D
FBAD<61>	3.3A 4.5D
FBAD<62>	3.3A 4.5D
FBAD<63>	3.3A 4.5D
FBADQM<0>	3.3A 4.4B
FBADQM<7..0>	3.3A> 4.4A< 4.5F<
FBADQM<1>	3.3A 4.4C
FBADQM<2>	3.3A 4.4D
FBADQM<3>	3.3A 4.4D
FBADQM<4>	3.3A 4.5B
FBADQM<5>	3.3A 4.5C
FBADQM<6>	3.3A 4.5D
FBADQM<7>	3.3A 4.5D
FBADQS0	3.3A<> 4.4B 4.4F<>
FBADQS0*	3.4A<> 4.4B 4.4F<>
FBADQS1	3.4A<> 4.4C 4.4F<>
FBADQS1*	3.4A<> 4.4C 4.4F<>
FBADQS2	3.4A<> 4.4D 4.4F<>
FBADQS2*	3.4A<> 4.4D 4.4F<>
FBADQS3	3.4A<> 4.4D 4.4F<>
FBADQS3*	3.4A<> 4.4D 4.4F<>
FBADQS4	3.4A<> 4.4F<> 4.5B
FBADQS4*	3.4A<> 4.4F<> 4.5B
FBADQS5	3.4A<> 4.4F<> 4.5C
FBADQS5*	3.4A<> 4.4F<> 4.5C
FBADQS6	3.4A<> 4.4F<> 4.5D
FBADQS6*	3.4A<> 4.4F<> 4.5D
FBADQS7	3.4A<> 4.4F<> 4.5D
FBADQS7*	3.4A<> 4.4F<> 4.5D
FBA_A<0>	3.3C 4.1A 4.1C 4.1E 4.1G
FBA_A<12..0>	3.3D> 4.1A< 4.4F<
FBA_A<1>	3.3C 4.1A 4.1C 4.1E 4.1G
FBA_A<2>	3.3C 4.1A 4.1C
FBA_A<3>	3.3C 4.1A 4.1C
FBA_A<4>	3.3C 4.1A 4.1C
FBA_A<5>	3.3C 4.1A 4.1C
FBA_A<6>	3.3C 4.1A 4.1C 4.1E 4.1G
FBA_A<7>	3.3C 4.1A 4.1C 4.1E 4.1G
FBA_A<8>	3.3C 4.1A 4.1C 4.1E 4.1G
FBA_A<9>	3.3C 4.2A 4.2C 4.2E 4.2G
FBA_A<10>	3.3C 4.2A 4.2C 4.2E 4.2G
FBA_A<11>	3.3C 4.2A 4.2C 4.2E 4.2G
FBA_A<12>	3.3C 4.2A 4.2C 4.2E 4.2G
FBA_BA0	3.3D> 4.2A< 4.2C 4.2E 4.2G 4.4F<
FBA_BA1	3.3D> 4.2A< 4.2C 4.2E 4.2G 4.4F<
FBA_BA2	3.3D> 4.2A< 4.2C 4.2E 4.2G 4.4F<
FBA_CAS*	3.4D> 4.1A< 4.1C 4.1E 4.1G 4.5F<
FBA_CKE	3.3D> 4.2A< 4.2C 4.2E 4.2G 4.4F<
FBA_CLK0	3.4D> 4.2A 4.2C 4.3A< 4.4F<
FBA_CLK0*	3.4D> 4.2A 4.2C 4.3C< 4.4F<
FBA_CLK0_TERM	4.3B
FBA_CLK1	3.4D> 4.2E 4.2G 4.3C< 4.4F<
FBA_CLK1*	3.4D> 4.2E 4.2G 4.3E< 4.4F<
FBA_CLK1_TERM	4.3D
FBA_CS0*	3.3D> 4.1A< 4.1C 4.1E 4.1G 4.5F<
FBA_CS1*	4.5F<
FBA_ODT	3.5D> 4.2A< 4.2C 4.2E 4.2G 4.5F<
FBA_ODT_GPU	3.1G> 3.4C 3.5C
FBA_PLLAVDD_GPU	3.4C
FBA_RAS*	3.3D> 4.1A< 4.1C 4.1E 4.1G 4.4F<
FBA_RESET	3.1G> 3.3C 3.5C
FBA_VREF1	4.2B 4.3F<
FBA_VREF2	4.2F 4.3F<
FBA_VREF3	4.2D 4.3F<
FBA_VREF4	4.2H 4.3F<
FBA_WE*	3.3D> 4.1A< 4.1C 4.1E 4.1G 4.5F<
FBB_A<2>	3.3C 4.1E 4.1G
FBB_A<5..2>	3.3D> 4.1A< 4.4F<
FBB_A<3>	3.3C 4.1E 4.1G
FBB_A<4>	3.3C 4.1E 4.1G
FBB_A<5>	3.3C 4.1E 4.1G
FBCAL_PD	3.4G
FBCAL_PU	3.4G

FBCAL_TERM	3.5G
FBCD<0>	3.1E 5.4B
FBCD<63..0>	3.1E<> 5.4A<> 5.5F<>
FBCD<1>	3.1E 5.4B
FBCD<2>	3.1E 5.4B
FBCD<3>	3.1E 5.4B
FBCD<4>	3.1E 5.4B
FBCD<5>	3.1E 5.4B
FBCD<6>	3.1E 5.4B
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FBCD<8>	3.1E 5.4C
FBCD<9>	3.1E 5.4C
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FBCD<12>	3.1E 5.4C
FBCD<13>	3.1E 5.4C
FBCD<14>	3.1E 5.4C
FBCD<15>	3.1E 5.4C
FBCD<16>	3.1E 5.4D
FBCD<17>	3.2E 5.4D
FBCD<18>	3.2E 5.4D
FBCD<19>	3.2E 5.4D
FBCD<20>	3.2E 5.4D
FBCD<21>	3.2E 5.4D
FBCD<22>	3.2E 5.4D
FBCD<23>	3.2E 5.4D
FBCD<24>	3.2E 5.4D
FBCD<25>	3.2E 5.4D
FBCD<26>	3.2E 5.4D
FBCD<27>	3.2E 5.4D
FBCD<28>	3.2E 5.4D
FBCD<29>	3.2E 5.4D
FBCD<30>	3.2E 5.4D
FBCD<31>	3.2E 5.4D
FBCD<32>	3.2E 5.5B
FBCD<33>	3.2E 5.5B
FBCD<34>	3.2E 5.5B
FBCD<35>	3.2E 5.5B
FBCD<36>	3.2E 5.5B
FBCD<37>	3.2E 5.5B
FBCD<38>	3.2E 5.5B
FBCD<39>	3.2E 5.5B
FBCD<40>	3.2E 5.5C
FBCD<41>	3.2E 5.5C
FBCD<42>	3.2E 5.5C
FBCD<43>	3.2E 5.5C
FBCD<44>	3.2E 5.5C
FBCD<45>	3.2E 5.5C
FBCD<46>	3.2E 5.5C
FBCD<47>	3.3E 5.5C
FBCD<48>	3.3E 5.5D
FBCD<49>	3.3E 5.5D
FBCD<50>	3.3E 5.5D
FBCD<51>	3.3E 5.5D
FBCD<52>	3.3E 5.5D
FBCD<53>	3.3E 5.5D
FBCD<54>	3.3E 5.5D
FBCD<55>	3.3E 5.5D
FBCD<56>	3.3E 5.5D
FBCD<57>	3.3E 5.5D
FBCD<58>	3.3E 5.5D
FBCD<59>	3.3E 5.5D
FBCD<60>	3.3E 5.5D
FBCD<61>	3.3E 5.5D
FBCD<62>	3.3E 5.5D
FBCD<63>	3.3E 5.5D
FBCDQM<0>	3.3E 5.4B
FBCDQM<7..0>	3.3E> 5.4A< 5.5F<
FBCDQM<1>	3.3E 5.4C
FBCDQM<2>	3.3E 5.4D
FBCDQM<3>	3.3E 5.4D
FBCDQM<4>	3.3E 5.5B
FBCDQM<5>	3.3E 5.5C
FBCDQM<6>	3.3E 5.5D
FBCDQM<7>	3.3E 5.5D
FBCDQS0	3.3E<> 5.4B 5.4F<>
FBCDQS0*	3.4E<> 5.4B 5.4F<>
FBCDQS1	3.4E<> 5.4C 5.4F<>
FBCDQS1*	3.4E<> 5.4C 5.4F<>
FBCDQS2	3.4E<> 5.4D 5.4F<>
FBCDQS2*	3.4E<> 5.4D 5.4F<>
FBCDQS3	3.4E<> 5.4D 5.4F<>
FBCDQS3*	3.4E<> 5.4D 5.4F<>
FBCDQS4	3.4E<> 5.4F<> 5.5B
FBCDQS4*	3.4E<> 5.4F<> 5.5B
FBCDQS5	3.4E<> 5.4F<> 5.5C
FBCDQS5*	3.4E<> 5.4F<> 5.5C
FBCDQS6	3.4E<> 5.4F<> 5.5D
FBCDQS6*	3.4E<> 5.4F<> 5.5D
FBCDQS7	3.4E<> 5.4F<> 5.5D
FBCDQS7*	3.4E<> 5.4F<> 5.5D
FBC_A<0>	3.3G 5.1A 5.1C 5.1E 5.1G
FBC_A<12..0>	3.3H> 5.1A< 5.4F<
FBC_A<1>	3.3G 5.1A 5.1C 5.1E 5.1G

FBC_A<2>	3.3G 5.1A 5.1C
FBC_A<3>	3.3G 5.1A 5.1C
FBC_A<4>	3.3G 5.1A 5.1C
FBC_A<5>	3.3G 5.1A 5.1C
FBC_A<6>	3.3G 5.1A 5.1C 5.1E 5.1G
FBC_A<7>	3.3G 5.1A 5.1C 5.1E 5.1G
FBC_A<8>	3.3G 5.1A 5.1C 5.1E 5.1G
FBC_A<9>	3.3G 5.1A 5.1C 5.1E 5.1G
FBC_A<10>	3.3G 5.1A 5.1C 5.1E 5.1G
FBC_A<11>	3.3G 5.1A 5.1C 5.1E 5.1G
FBC_A<12>	3.3G 5.2A 5.2C 5.2E 5.2G
FBC_BA0	3.3H> 5.2A< 5.2C 5.2E 5.2G 5.4F<
FBC_BA1	3.3H> 5.2A< 5.2C 5.2E 5.2G 5.4F<
FBC_BA2	3.3H> 5.2A< 5.2C 5.2E 5.2G 5.4F<
FBC_CAS*	3.4H> 5.1A< 5.1C 5.1E 5.1G 5.5F<
FBC_CKE	3.3H> 5.2A< 5.2C 5.2E 5.2G 5.4F<
FBC_CLK0	3.4H> 5.2A 5.2C 5.3A< 5.3F<
FBC_CLK0*	3.4H> 5.2A 5.2C 5.3B< 5.4F<
FBC_CLK0_TERM	5.3B
FBC_CLK1	3.4H> 5.2E 5.2G 5.3C< 5.4F<
FBC_CLK1*	3.4H> 5.2E 5.2G 5.3E< 5.4F<
FBC_CLK1_TERM	5.3D
FBC_CS0*	3.3H> 5.1A< 5.1C 5.1E 5.1G 5.5F<
FBC_CS1*	5.5F<
FBC_ODT	3.5D> 5.2A< 5.2C 5.2E 5.2G 5.5F<
FBC_ODT_GPU	3.1G> 3.4G 3.5C
FBC_PLLAVDD	3.4G
FBC_RAS*	3.3H> 5.1A< 5.1C 5.1E 5.1G 5.5F<
FBC_RESET	3.1G> 3.3G 3.5C
FBC_VREF1	5.2B 5.3F<
FBC_VREF2	5.2F 5.3F<
FBC_VREF3	5.2D 5.3F<
FBC_VREF4	5.2H 5.3F<
FBC_WE*	3.3H> 5.1A< 5.1C 5.1E 5.1G 5.5F<
FBD_A<2>	3.3G 5.1E 5.1G
FBD_A<5..2>	3.3H> 5.1A< 5.4F<
FBD_A<3>	3.3G 5.1E 5.1G
FBD_A<4>	3.3G 5.1E 5.1G
FBD_A<5>	3.3G 5.1E 5.1G
FBVDDQ	14.1G
FB_BOOT	14.2C
FB_BOOTC	14.2D
FB_COMP	14.3B
FB_COMP1	14.3C
FB_DH	14.2C
FB_DL	14.2C
FB_FB	14.3D
FB_FSET	14.2B
FB_ISEN	14.2C
FB_PHASE	14.2C
FB_PWRGOOD	8.2A< 14.2A>
FB_SNUBBER	14.2E
FB_VCC	14.2B
FB_VREF1	3.5A
FB_VREF2	3.5E
GPIO0_DVI_A_HPD	10.3D
GPIO1_DVI_B_HPD	8.4A< 10.3F>
GPIO2_BL_PWM	9.3B< 10.3F>
GPIO3_PPEN	9.3B< 10.3F>
GPIO3_PPEN_GPU	10.3D
GPIO4_BLEN	9.3B< 10.3F>
GPIO4_BLEN_GPU	10.3D
GPIO5_NVVDDCTL0	10.3F> 13.4B<
GPIO6_NVVDDCTL1	10.3F> 13.4B<
GPIO8_THERM_ALERT*	10.3D
GPIO_AC_BATT*	9.4B> 10.3F<
GPIO_SLI_SYNC	9.3H<> 10.3F<>
I2CA_SCL	7.1D
I2CA_SCL_R	7.1F> 9.3B<
I2CA_SDA	7.1D
I2CA_SDA_R	7.1F<> 9.3B<>
I2CB_SCL	7.3D
I2CB_SCL_R	7.3G> 9.2B<
I2CB_SDA	7.3D
I2CB_SDA_R	7.3G<> 9.2B<>
I2CC_SCL	10.3D

I2CC_SCL_R	9.4B< 10.3F> 11.2B<
I2CC_SDA	10.3D
I2CC_SDA_R	9.4B<> 10.3F<> 11.2B<>
I2CH_SCL	11.4C
I2CH_SDA	11.4C
IFPABIOVDD	8.2D
IFPABPLLVDD	8.1D
IFPABRSET	8.1D
IFPATXC	8.1H> 9.4G<
IFPATXC*	8.1H> 9.4G<
IFPATXD0	8.1H> 9.4G<
IFPATXD0*	8.1H> 9.4G<
IFPATXD1	8.1H> 9.4G<
IFPATXD1*	8.1H> 9.4G<
IFPATXD2	8.2H> 9.4G<
IFPATXD2*	8.2H> 9.4G<
IFPATXD3	8.2H> 9.4G<
IFPATXD3*	8.2H> 9.4G<
IFPBTXC	8.2H> 9.4G<
IFPBTXC*	8.2H> 9.4G<
IFPBTXD4	8.2H> 9.3G<
IFPBTXD4*	8.2H> 9.3G<
IFPBTXD5	8.2H> 9.3G<
IFPBTXD5*	8.2H> 9.3G<
IFPBTXD6	8.2H> 9.4G<
IFPBTXD6*	8.2H> 9.4G<
IFPBTXD7	8.2H> 9.4G<
IFPBTXD7*	8.2H> 9.4G<
IFPCDBRSET	8.3D
IFPCDPLLVDD	8.3D
IFPCTXC	8.3H> 9.2G<
IFPCTXC*	8.3H> 9.2G<
IFPCTXD0	8.3H> 9.2G<
IFPCTXD0*	8.3H> 9.2G<
IFPCTXD1	8.3H> 9.2G<
IFPCTXD1*	8.3H> 9.2G<
IFPCTXD2	8.4H> 9.2G<
IFPCTXD2*	8.4H> 9.2G<
IFPC_IOVDD	8.4D
IFPDTXC	8.4H> 9.3G<
IFPDTXC*	8.4H> 9.3G<
IFPDTXD3	8.4H> 9.2G<
IFPDTXD3*	8.4H> 9.2G<
IFPDTXD4	8.4H> 9.2G<
IFPDTXD4*	8.4H> 9.2G<
IFPDTXD5	8.4H> 9.2G<
IFPDTXD5*	8.4H> 9.2G<
IFPD_IOVDD	8.4D
JTAG_TCLK	10.3B
JTAG_TDI	10.3B
JTAG_TDO	10.3B
JTAG_TMS	10.3B
JTAG_TRST	10.3B
LVDS_IOVDD	8.2B
MIOACAL_PD_VDDQ	12.2C
MIOACAL_PU_GND	12.2C
MIOA_VDDQ	12.1C
MIOA_VREF	12.2C
MIOB_CTL3	12.4F< 15.2C 15.4B>
M_GPIO8_SLOWDOWN*	10.2C
M_THERM_ALERT*	10.2C
NVCTL0_R	13.4D
NVCTL1_R	13.4D
NVVDD	13.1G
NVVDDCTL0	13.4D
NVVDDCTL1	13.4C
NVVDD_SENSE	2.3G> 13.3G<
NVVDD_SENSE_FB	13.3F
NV_BOOT	13.2C
NV_BOOTC	13.2D
NV_COMP	13.2C
NV_COMP1	13.3C
NV_DH	13.2C
NV_DL	13.2C
NV_FB	13.3D
NV_FSET	13.2B
NV_ISEN	13.2C
NV_PHASE	13.2C
NV_PWRGOOD	10.2F< 13.2B> 14.2A<
NV_SNUBBER	13.2F
NV_VCC	13.2B
PCI_DEVID3	12.4F< 15.2C 15.4B>
PEX1V2	14.1G
PEX1V2_FB	14.4D
PEX_PLLDVDD	2.4F
PEX_RCLK	2.2E
PEX_RCLK*	2.2E
PEX_RST	2.1D
PEX_RX0	2.2E
PEX_RX0*	2.2E
PEX_RX1	2.2E
PEX_RX1*	2.2E
PEX_RX2	2.2E
PEX_RX2*	2.2E
PEX_RX3	2.3E

PEX_RX3*	2.3E
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PEX_RX4*	2.3E
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PEX_RX5*	2.3E
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PEX_RX6*	2.3E
PEX_RX7	2.3E
PEX_RX7*	2.3E
PEX_RX8	2.4E
PEX_RX8*	2.4E
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PEX_RX9*	2.4E
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PEX_RX10*	2.4E
PEX_RX11	2.4E
PEX_RX11*	2.4E
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PEX_RX13*	2.5E
PEX_RX14	2.5E
PEX_RX14*	2.5E
PEX_RX15	2.5E
PEX_RX15*	2.5E
PEX_TSTCLK	2.2E
PEX_TSTCLK*	2.2E
PEX_TX0	2.2E
PEX_TX0*	2.2E
PEX_TX0_C	2.2B
PEX_TX0_C*	2.2B
PEX_TX1	2.2E
PEX_TX1*	2.2E
PEX_TX1_C	2.2B
PEX_TX1_C*	2.2B
PEX_TX2	2.2E
PEX_TX2*	2.2E
PEX_TX2_C	2.2B
PEX_TX2_C*	2.2B
PEX_TX3	2.3E
PEX_TX3*	2.3E
PEX_TX3_C	2.3B
PEX_TX3_C*	2.3B
PEX_TX4	2.3E
PEX_TX4*	2.3E
PEX_TX4_C	2.3B
PEX_TX4_C*	2.3B
PEX_TX5	2.3E
PEX_TX5*	2.3E
PEX_TX5_C	2.3B
PEX_TX5_C*	2.3B
PEX_TX6	2.3E
PEX_TX6*	2.3E
PEX_TX6_C	2.3B
PEX_TX6_C*	2.3B
PEX_TX7	2.3E
PEX_TX7*	2.3E
PEX_TX7_C	2.3B
PEX_TX7_C*	2.3B
PEX_TX8	2.4E
PEX_TX8*	2.4E
PEX_TX8_C	2.4B
PEX_TX8_C*	2.4B
PEX_TX9	2.4E
PEX_TX9*	2.4E
PEX_TX9_C	2.4B
PEX_TX9_C*	2.4B
PEX_TX10	2.4E
PEX_TX10*	2.4E
PEX_TX10_C	2.4B
PEX_TX10_C*	2.4B
PEX_TX11	2.4E
PEX_TX11*	2.4E
PEX_TX11_C	2.4B
PEX_TX11_C*	2.4B
PEX_TX12	2.4E
PEX_TX12*	2.4E
PEX_TX12_C	2.4B
PEX_TX12_C*	2.4B
PEX_TX13	2.5E
PEX_TX13*	2.5E
PEX_TX13_C	2.5B
PEX_TX13_C*	2.5B
PEX_TX14	2.5E
PEX_TX14*	2.5E
PEX_TX14_C	2.5B
PEX_TX14_C*	2.5B
PEX_TX15	2.5E
PEX_TX15*	2.5E
PEX_TX15_C	2.5B
PEX_TX15_C*	2.5B
PLLVDD	7.4C
PWR_SRC	9.1G
RAMCFG0	12.3F< 15.1C 15.3B>
RAMCFG1	12.3F< 15.2C 15.4B>
RAMCFG2	12.3F< 15.2C 15.4B>

RAMCFG3	12.3F< 15.2C 15.4B>
ROMCS*	11.3C
ROM_SCLK	11.3C
ROM_SI	11.3C< 15.3C 15.4B>
ROM_SO	11.3C
RUNPWROK	8.4A< 9.4A> 11.2B< 13.2B< 14.4C<
RUNPWROK*	8.4B
RUNPWROK_IN	9.4C
SLI_CLKOUT	9.3G<> 12.2F<>
SLI_D<0>	9.3E 12.1E
SLI_D<14..0>	9.3F<> 12.1F<> 15.4B>
SLI_D<1>	9.3E 12.1E
SLI_D<2>	9.3E 12.1E
SLI_D<3>	9.3E 12.1E
SLI_D<4>	9.3E 12.2E
SLI_D<5>	9.3E 12.2E
SLI_D<6>	9.3E 12.2E
SLI_D<7>	9.3E 12.2E
SLI_D<8>	9.3E 12.2E
SLI_D<9>	9.3E 12.2E
SLI_D<10>	9.3E 12.2E
SLI_D<11>	9.3E 12.2E
SLI_D<12>	9.3E 12.2E
SLI_D<13>	9.3E 12.2E 15.3C
SLI_D<14>	9.3E 12.2E
SLI_DE	9.3G<> 12.2F<>
SLI_REFCLK	9.3G<> 12.4F<>
SLI_SWAP_OUT	9.3H<> 11.4C<>
SMB_CLK	9.4B> 10.2A<
SMB_CLK_GPU	10.3D
SMB_DAT	9.4B<> 10.2A<>
SMB_DATA_GPU	10.3D
SNN_A2_M1	4.2A
SNN_A2_M2	4.2C
SNN_A2_M3	4.2E
SNN_A2_M4	4.2G
SNN_A2_M5	5.2A
SNN_A2_M6	5.2C
SNN_A2_M7	5.2E
SNN_A2_M8	5.2G
SNN_BUFRST*	11.4C
SNN_CLAMP_F6	10.3D
SNN_DACB_CSYNC	7.2D
SNN_DACC_BLUE	7.3D
SNN_DACC_GREEN	7.3D
SNN_DACC_HSYNC	7.3D
SNN_DACC_RED	7.3D
SNN_DACC_RSET	7.3C
SNN_DACC_VREF	7.3C
SNN_DACC_VSYNC	7.3D
SNN_E2_M1	4.2A
SNN_E2_M2	4.2C
SNN_E2_M3	4.2E
SNN_E2_M4	4.2G
SNN_E2_M5	5.2A
SNN_E2_M6	5.2C
SNN_E2_M7	5.2E
SNN_E2_M8	5.2G
SNN_FBA_CMD26	3.4C
SNN_FBA_CMD27	3.4C
SNN_FBA_CMD28	3.4C
SNN_FBA_NC1_D31	3.5C
SNN_FBA_NC1_D32	3.5C
SNN_FBC_CMD26	3.4G
SNN_FBC_CMD27	3.4G
SNN_FBC_CMD28	3.4G
SNN_FBC_PLLVDD	3.4G
SNN_FBVTT_AA23	3.1G
SNN_FBVTT_AB23	3.1G
SNN_FBVTT_H16	3.1G
SNN_FBVTT_H17	3.1G
SNN_FBVTT_J9	3.1G
SNN_FBVTT_J10	3.1G
SNN_FBVTT_J23	3.1G
SNN_FBVTT_J24	3.1G
SNN_FBVTT_K9	3.1G
SNN_FBVTT_K11	3.1G
SNN_FBVTT_K12	3.1G
SNN_FBVTT_K21	3.1G
SNN_FBVTT_K22	3.1G
SNN_FBVTT_K24	3.1G
SNN_FBVTT_L23	3.1G
SNN_FBVTT_M23	3.1G
SNN_FBVTT_T25	3.1G
SNN_FBVTT_U25	3.2G
SNN_G3_RFU1	12.4E
SNN_G3_RFU2	12.4E
SNN_G3_RFU3	12.4E
SNN_G3_RFU4	12.4E
SNN_G3_RFU5	12.4E
SNN_G3_RFU6	12.4E
SNN_G3_RFU7	12.4E
SNN_G3_RFU8	12.4E
SNN_G3_RFU9	11.4A
SNN_G3_RFU10	11.4A

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
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SNN_G3_RFU11	11.4A
SNN_G3_RFU12	11.4A
SNN_G3_RFU13	11.4A
SNN_G3_RFU14	11.4A
SNN_G3_RFU15	11.4A
SNN_G3_RFU16	11.4A
SNN_GND_SENSE	2.3F
SNN_GPIO7	10.3D
SNN_GPIO9	10.3D
SNN_GPIO10	10.3D
SNN_GPIO13	10.3D
SNN_GPIO14	10.3D
SNN_GPU_AG12	2.1D
SNN_GPU_AH13	2.2D
SNN_HDCP_ROM	11.4D
SNN_IFPABVPROBE	8.1D
SNN_IFPCDVPROBE	8.3D
SNN_MIOACLKOUTR*	12.2E
SNN_MIOA_M5	12.2E
SNN_MIOBCAL_PD_VDDQ	12.3C
SNN_MIOBCAL_PU_GND	12.3C
SNN_MIOBD<2>	12.3E
SNN_MIOBD<3>	12.3E
SNN_MIOBD<4>	12.3E
SNN_MIOBD<5>	12.3E
SNN_MIOBD<6>	12.3E
SNN_MIOBD<7>	12.3E
SNN_MIOB_CLKOUT	12.4E
SNN_MIOB_CLKOUT*	12.4E
SNN_MIOB_DE	12.4E
SNN_MIOB_HSYNC	12.4E
SNN_MIOB_VREF	12.4C
SNN_MIOB_VSYNC	12.4E
SNN_MSTRAPSEL0	11.3A
SNN_MSTRAPSEL1	11.3A
SNN_MSTRAPSEL2	11.3A
SNN_MSTRAPSEL3	11.3A
SNN_POK	14.4C
SNN_R3_M1	4.2A
SNN_R3_M2	4.2C
SNN_R3_M3	4.2E
SNN_R3_M4	4.2G
SNN_R3_M5	5.2A
SNN_R3_M6	5.2C
SNN_R3_M7	5.2E
SNN_R3_M8	5.2G
SNN_R7_M1	4.2A
SNN_R7_M2	4.2C
SNN_R7_M3	4.2E
SNN_R7_M4	4.2G
SNN_R7_M5	5.2A
SNN_R7_M6	5.2C
SNN_R7_M7	5.2E
SNN_R7_M8	5.2G
SNN_R8_M1	4.2A
SNN_R8_M2	4.2C
SNN_R8_M3	4.2E
SNN_R8_M4	4.2G
SNN_R8_M5	5.2A
SNN_R8_M6	5.2C
SNN_R8_M7	5.2E
SNN_R8_M8	5.2G
SNN_ROM_TYPE_0	12.3E
SNN_STEREO	11.4C
SNN_STRAP	11.3A
SNN_THERMAL	10.3B
SPDIF	9.1G> 9.4C
SPDIF_IN	2.5G< 9.1G> 9.4B>
SSFOUT	7.4C< 7.5G< 11.2E>
SS_OUT	11.2C
SS_REF	11.2C
TESTMCLK	11.4C
TESTMODE	11.4C
THERM	10.3B
THERM*	10.3B
THERM_ALERT*	9.4B< 10.2F>
THERM_SCL	10.2B
THERM_SDA	10.2B
THERM_VDD	10.2C
TMDSD_IOVDD	8.4C
TMDS_IOVDD	8.4B
XTALIN	7.4C 7.5G<
XTALOUT	7.4D 7.5G>
XTALOUTBUFF	7.4F> 7.5G> 11.2B<

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM V1.3, HDCP.
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C3 [2.3A]
C4 [11.3F]
C5 [10.2D]
C6 [7.5C]
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C12 [14.4C]
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C14 [6.4E]
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