NV15 DF, 1/2/4MX32 DDR, RGB, Ext. TMDS DVI-I, TV, AGP4X.

PCI DEVICE ID 0X0=0X151.

Design Notes:
X11-602-10023-0000-A00 SOURCE
Memory Options for 4MX32, 2MX32 AND ESMT 2MX32 DONE
3.3V VDD SUPPORT FOR ESMT 2MX32 DONE

Design Notes for A01:

X02: R897, R898 IDUMP RES Added. Decaps C436 -> C450 added for Memory

X03: Gnd split shunt res R899 added. R335->R338 & R380->R383 PKG changed to 0805.
R880->R883 PKG changed to 0603
X04: IDUMP RES R898 Removed

X07: R810 changed to 110R from 100R,
     D801, R829,R835,R831,R827- to be stuffed.
     PCB A01 done.
A01-X08: R810 changed to 115R from 110R. R811 changed to 100R from 102R
     Y201-Property and BOM updated for CH7007
     L201,L202,L205,L206,L209,L210 BOM Changed to 0603 but footprint is still 0805.

Design Notes for A02:
X01: Taken from AX1 Ver 008.DSN
     L201,L202,L205,L206,L209,L210 Foot print changed to 0603
     D801,R829,R835,R831,R827- No stuff.

X02: R900, R901 new comp added to U800.22 for Boot problem for 3.3V coming late.
     L201, L205, L209- Changed to 68nH from 82nH for FCC.
     C361, C323- No Stuff for FCC.
     D801 and R829,R835,R831,R827 STUFF

PCB-A02 done- 8/30/01, P-Release 8/31/01
X03: C805 Changed to 1UF from 4.7UF

Design Notes for A03:
X01: C805 Changed to 1UF from 4.7UF

X02:
C805 Changed to 0.1UF from 1.0UF
Q809,Q810,R902->R903 added.

PCB-A03 done- 9/10/01, P-Release AP3 9/10/01

X03: Support for HIP6019 along with U3007 is done
R829 Removed from SCH, instead R836 to be stuffed
ADDed C986-for HIP Soft Start
C984, C987, R907 for HIP Compnesation1 Ckt.
C985, C988, R908 for HIP Compnesation2 Ckt.
R906, C983 in the VTT feed back control path for HIP.
R805 Rewired and To be Stuffed for Unisem.

P23-SCH R.003
Last Updt:
9/11/01

NVIDIA Corporation
3535 Monroe St
Santa Clara, CA 95051, USA

602-10023-0000-A03

| Size B | CAGE Code | DWG NO | Rev 06 |

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{Item}\t{Quantity}\t{Reference}\t{Value}\t{Assembly}\t{MAIN}\t{NVPNMAIN}\t{NVPNBT}\t{NVPNCH}\t{NVPNTMDS}
{Assembly}{Source Package} {Value}{PN}{AVL1}{AVL2}{AVL3}{AVL4}{AVL5}

U100A

PCIAD[31:0]

Signal	Pin
PCIAD0	AE25
PCIAD1	AF25
PCIAD2	AD23
PCIAD3	AF24
PCIAD4	AC22
PCIAD5	AE23
PCIAD6	AC21
PCIAD7	AF23
PCIAD8	AE21
PCIAD9	AC20
PCIAD10	AF21
PCIAD11	AD20
PCIAD12	AF20
PCIAD13	AC19
PCIAD14	AE19
PCIAD15	AD19
PCIAD16	AC16
PCIAD17	AF16
PCIAD18	AD16
PCIAD19	AE15
PCIAD20	AC15
PCIAD21	AF15
PCIAD22	AD15
PCIAD23	AE13
PCIAD24	AB14
PCIAD25	AF13
PCIAD26	AD12
PCIAD27	AF12
PCIAD28	AC12
PCIAD29	AE11
PCIAD30	AD11
PCIAD31	AF11

VDDQ
C100 0.1UF C101 0.1UF
C102 0.1UF C103 0.1UF

VDDQ	AE24
VDDQ	AE20
VDDQ	AB18
VDDQ	AE16
VDDQ	AB15
VDDQ	AE12
VDDQ	AB12
VDDQ	AB9
VDDQ	AE8

GND	AF10
GND	AF14
GND	AF18
GND	AF22
GND	AB11
GND	AB16

PCICBE0	AD21	PCICBE0#
PCICBE1	AF19	PCICBE1#
PCICBE2	AF17	PCICBE2#
PCICBE3	AC14	PCICBE3#

| PCICLK | AC13 | PCICLK |
| PCIRST_ | AB13 | PCIRST# |

| PCIGNT_ | AC7 | PCIGNT# |
| PCIREQ_ | AF6 | PCIREQ# |

PCIFRAME_	AD17	PCIFRAME#
PCIIRDY_	AE17	PCIIRDY#
PCITRDY_	AC17	PCITRDY#
PCIDEVSEL_	AE18	PCIDEVSEL#
PCISTOP_	AD18	PCISTOP#
PCIPAR	AC18	PCIPAR

PCIINTA_	AD13	PCIINTA#
AGPRBF_	AE7	AGPRBF#
AGPWBF_	AB10	AGPWBF#
AGPPIPE_	AD8	AGPPIPE#
AGPST0	AD7	AGPST0
AGPST1	AB8	AGPST1
AGPST2	AE7	AGPST2

AGPADSTB1	AE14	AGPADSTB1
AGPADSTB1_	AD14	AGPADSTB1#
AGPADSTB0	AE22	AGPADSTB0
AGPADSTB0_	AD22	AGPADSTB0#
AGPSBSTB	AF9	AGPSBSTB
AGPSBSTB_	AD9	AGPSBSTB#
AGPSBA0	AF8	AGPSBA0
AGPSBA1	AC8	AGPSBA1
AGPSBA2	AE9	AGPSBA2
AGPSBA3	AC9	AGPSBA3
AGPSBA4	AD10	AGPSBA4
AGPSBA5	AC10	AGPSBA5
AGPSBA6	AE10	AGPSBA6
AGPSBA7	AC11	AGPSBA7
AGPVREFCG	AD24	AGPVREF

AGPSBA[7:0]

| TESTEN | AC3 | TESTEN |

R100 10K

FBVDDQ AGP3.3V NVVDD

VDD25	AB20
GND	AB7
VDD25	AA21
VDD25	AA20
VDD25	AA19
VDD25	AA18
VDD33	AA7
VDD33	AA6
GND	Y22
VDD33	Y21
VDD25	Y6
VDD	Y5
VDD25	W21
VDD	W8
VDD25	V21
VDD	V6
VDD25	J21
VD50CLAMP0	J6
VDD25	H21
VDD25	H6
VDD25	G22
VDD25	G21
VDD25	G6
VD50CLAMP0	G5
VDD25	F21
VDD25	F20
VDD25	F19
VDD25	F18
VDD25	F9
VDD25	F8
VDD25	F7
VDD25	F6
GND	E20

5V

Geforce2-TI, 256 Bit 3D GPU

K100

Fansink for GeForce2-GTS

5V
R101 2.2K
R102 100R
GPIO0R
Q100 PMBT2222

12V
D100 BAT54ALT1 NO STUFF

12V
J101
1
2
F ST SHR IRT

GPIO0Q
C980 0.1UF 16V

GPIO0

1a. NV15 HOST

Size C	CAGE Code	DWG NO	Rev

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Scale

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1b1. AGP I/O

5V

Location for 5V filter, if needed for EMC.

R150
0R

C104
4.7UF

C108
0.1UF

VDDQ

5VFLT

C109 4.7UF
C110 0.01UF
C111 0.01UF
C112 0.022UF
C113 0.01UF
C114 0.01UF

AGP3.3V

C115 4.7UF
C116 0.022UF
C117 0.022UF
C118 0.022UF

In all cases each capacitor should be low
ESR/ESL and placed as close as possible to
the respective rail connector pin(s).

Pin	Signal		Pin	Signal	Net
B2	5V		A65	AD0	PCIAD0
B3	5V		A65	AD1	PCIAD1
B34	VDDQ		A63	AD2	PCIAD2
B40	VDDQ		B63	AD3	PCIAD3
B47	VDDQ		A62	AD4	PCIAD4
B52	VDDQ		A60	AD5	PCIAD5
B58	VDDQ		B62	AD6	PCIAD6
B64	VDDQ		B60	AD7	PCIAD7
A34	VDDQ		B57	AD8	PCIAD8
A40	VDDQ		A56	AD9	PCIAD9
A52	VDDQ		B56	AD10	PCIAD10
A58	VDDQ		A54	AD11	PCIAD11
A64	VDDQ		B54	AD12	PCIAD12
B9	3.3V		A53	AD13	PCIAD13
B16	3.3V		B53	AD14	PCIAD14
B28	3.3V		A51	AD15	PCIAD15
A9	3.3V		A39	AD16	PCIAD16
A16	3.3V		B38	AD17	PCIAD17
A28	3.3V		A38	AD18	PCIAD18
			B36	AD19	PCIAD19
			A36	AD20	PCIAD20
			B35	AD21	PCIAD21
			A35	AD22	PCIAD22
			B33	AD23	PCIAD23
			A30	AD24	PCIAD24
			B30	AD25	PCIAD25
			A29	AD26	PCIAD26
			B29	AD27	PCIAD27
			A27	AD28	PCIAD28
			B27	AD29	PCIAD29
			A26	AD30	PCIAD30
			B26	AD31	PCIAD31

PCIAD[31:0] 2

TYPEDET_
A2 TYPEDET#
B14 SPARE
A48 SPARE
B1 OVERCNT#

R103 0R

A57 C/BE0 PCICBE0 PCICBE0 2
B51 C/BE1 PCICBE1 PCICBE1 2
B39 C/BE2 PCICBE2 PCICBE2 2
A33 C/BE3 PCICBE3 PCICBE3 2

B7 CLK PCICLK PCICLK 2
A7 RST# PCIRST_ PCIRST_ 2

A3 RESERVED
A11 RESERVED

A8 GNT# PCIGNT_ PCIGNT_ 2
B8 REQ# PCIREQ_ PCIREQ_ 2

A41 FRAME# PCIFRAME_ PCIFRAME_ 2
B41 IRDY#   PCIIRDY_   PCIIRDY_   2
A46 TRDY#   PCITRDY_   PCITRDY_   2
B46 DEVSEL# PCIDEVSEL_ PCIDEVSEL_ 2
A47 STOP#   PCISTOP_   PCISTOP_   2
A50 PAR   PCIPAR   PCIPAR   2

R104 1 2 0R NO STUFF

B6 INTB#
B48 PERR#
B50 SERR#

A6 INTA#   PCIINTA_ PCIINTA_ 2
B12 RBF#   AGPRBF_   AGPRBF_   2
A14 WBF#   AGPWBF_   AGPWBF_   2
A12 PIPE#   AGPPIPE_ AGPPIPE_ 2
B10 ST0   AGPST0   AGPST0   2
A10 ST1   AGPST1   AGPST1   2
B11 ST2   AGPST2   AGPST2   2

B4 USB+
A4 USB-

B32 ADSTB1   AGPADSTB1 AGPADSTB1 2
A32 ADSTB1# AGPADSTB1_ AGPADSTB1_ 2
B59 ADSTB0   AGPADSTB0 AGPADSTB0 2
A59 ADSTB0# AGPADSTB0_ AGPADSTB0_ 2
B18 SBSTB   AGPSBSTB   AGPSBSTB   2
A18 SBSTB#   AGPSBSTB_ AGPSBSTB_ 2
B15 SBA0   AGPSBA0
A15 SBA1   AGPSBA1
B17 SBA2   AGPSBA2
A17 SBA3   AGPSBA3
B20 SBA4   AGPSBA4
A20 SBA5   AGPSBA5
B21 SBA6   AGPSBA6
A21 SBA7   AGPSBA7

R105 1 2 0R NO STUFF
R106 1 2 0R NO STUFF
R107 1 2 0R NO STUFF
R108 1 2 0R NO STUFF

B5 GND
B13 GND
B19 GND
B31 GND
B49 GND
B55 GND
B61 GND
A5 GND
A13 GND
A19 GND
A31 GND
A37 GND
A49 GND
A55 GND
A61 GND

C119 5.6PF NO STUFF
C120 5.6PF NO STUFF
C121 5.6PF NO STUFF
R109 220K
R110 220K

AGPSBA[7:0] 2

B42 3.3Vaux/KEY
B45 3.3V/KEY
B44 RSVD/KEY
B43 GND/KEY

A45 3.3V/KEY
A42 RSVD/KEY
A44 RSVD/KEY
A43 GND/KEY

1.5V KEY
1.5V KEY

VDDQ

C122 470PF
R111 1.5K 1%

AGPVREF1

R113 75R 1%

AGPVREFGC
A66 RSVD/Vrefgc

R116 1.5K 1%
R114 75R 1%

AGPVREF2

C126 470PF

A1 +12V

C123 0.1UF 16V

B24 KEY/3.3Vaux
B22 KEY/RSVD
B25 KEY/3.3V
B23 KEY/GND

A24 KEY/RSVD
A22 KEY/RSVD
A25 KEY/3.3V
A23 KEY/GND

3.3V KEY
3.3V KEY

B66 RSVD/Vrefcg   AGPVREFCG   AGPVREFCG 2

VDDQ
R112 301K 1%

C125 0.1UF NO STUFF
R115 221K 1%

P23-A01 BARE PCB

NVVDD — C137 4.7UF
NVVDD — C127 4.7UF

NVVDD — C132 0.33UF
NVVDD — C929 2200PF
NVVDD — C133 0.33UF
NVVDD — C930 2200PF
NVVDD — C134 0.33UF
NVVDD — C931 2200PF
NVVDD — C135 0.33UF
FBVDDQ — C932 2200PF

FBVDDQ — C139 4.7UF
FBVDDQ — C136 4.7UF

AGP3.3V — C350 4.7UF
AGP3.3V — C433 0.1UF

FBVDDQ
C963 2200PF NO STUFF
C964 2200PF NO STUFF
C965 2200PF NO STUFF

FBVDDQ
C129 0.1UF
C130 0.1UF
C131 0.1UF
C142 0.1UF
C140 0.1UF
C141 0.1UF

1y. NV15 DECOUPLING

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nVIDIA

Size	CAGE Code	DWG NO	Rev
A			

Thursday, September 13, 2001

Scale

AGP3.3V

7,14,16,17 TVED[11:0]
7,14 VIPD[7:0]

TVED0   R117 1 ⟋⟍ 2 10K
[0] STRAP_AD_SWAP
STRAP_AD_SWAP=0 : PCIAD bus [31:0] swapped
STRAP_AD_SWAP=1 : PCIAD bus [31:0] normal

TVED1   R118 1 ⟋⟍ 2 10K
[1] STRAP_SUB_VENDOR
STRAP_SUB_VENDOR=0 : System BIOS
STRAP_SUB_VENDOR=1 : Adaptor BIOS

R125 1 ⟋⟍ 2 10K   VIPD7   R126 1 ⟋⟍ 2 10K
NO STUFF
[11] STRAP_FAST_WRITES
STRAP_FAST_WRITES=0 : FAST WRITE ENABLED
STRAP_FAST_WRITES=1 : FAST WRITE DISABLED

R119 1 ⟋⟍ 2 10K   VIPD6   R120 1 ⟋⟍ 2 10K
NO STUFF
[15] STRAP_DFP_WIDTH
STRAP_DFP_WIDTH=0 : 24-BIT
STRAP_DFP_WIDTH=1 : 12-BIT

R123 1 ⟋⟍ 2 10K   VIPD5   R124 1 ⟋⟍ 2 10K
NO STUFF

R121 1 ⟋⟍ 2 10K   VIPD4   R122 1 ⟋⟍ 2 10K
NO STUFF
[13:12] PCI_DEV_ID
PCI_DEV_ID = 0x151 (Default)

R533 1 ⟋⟍ 2 10K   TVED8   R534 1 ⟋⟍ 2 10K
NO STUFF

R531 1 ⟋⟍ 2 10K   TVED7   R532 1 ⟋⟍ 2 10K
NO STUFF
[8:7] STRAP_TVMODE
STRAP_TVMODE=0 : PAL
STRAP_TVMODE=1 : NTSC
STRAP_TVMODE=2 : Reserved
STRAP_TVMODE=3 : Disabled

R127 1 ⟋⟍ 2 10K   TVED6   R128 1 ⟋⟍ 2 10K
NO STUFF
[6] STRAP_CRYSTAL
STRAP_CRYSTAL=0 : 13.50000MHz
STRAP_CRYSTAL=1 : 14.31818MHz

R129 1 ⟋⟍ 2 10K   TVED5   R130 1 ⟋⟍ 2 10K
NO STUFF

4M=4MX32

2M=2MX32

2M also applicable
for 2ME
4M = K4D263238M-5
2M = HY5DU643222AQ-5
2ME= M13L64322A-5

R131 1 ⟋⟍ 2   TVED4   R132 1 ⟋⟍ 2
4M=NO STUFF:2M/2ME=10K   4M=10K:2ME/2M=NO STUFF

R133 1 ⟋⟍ 2   TVED3   R134 1 ⟋⟍ 2
4M=NO STUFF:2M/2ME=10K   4M=10K:2ME/2M=NO STUFF

R135 1 ⟋⟍ 2   TVED2   R136 1 ⟋⟍ 2
4M=NO STUFF:2M/2ME=10K   4M=10K:2ME/2M=NO STUFF

[5:2] STRAP_RAM_TYPE

1000 2Mx32, DLL on, low drive (Micron and Hyundai 2Mx32, when eventually qualified)
1001 2Mx32, DLL on, high/no drive (Samsung 2Mx32, where bit 1 in EMRS needs to be low, when DLL is on)
1110 1Mx32 Infineon DD2, DLL on (reserved for future use if needed)
1011 1Mx32 Infineon DD1, dll-off with CAS+1 (these are the original Infineon parts we used)
1100 1Mx32 Infineon DD2, DLL-off, but with 0x100080 set to CAS+0,rather than the standard CAS+1 that we have used with DLL-off (this is for the latest Infineon parts)
1010 4Mx16 DDR
1111 4Mx32 DDR

R137 1 ⟋⟍ 2 10K   TVED9   R138 1 ⟋⟍ 2 10K
NO STUFF
[9] STRAP_AGP4X
STRAP_AGP4X=0 : AGP4X transfers enabled
STRAP_AGP4X=1 : AGP2X only

R139 1 ⟋⟍ 2 10K   TVED10   R140 1 ⟋⟍ 2 10K
NO STUFF
[10] STRAP_AGPSBA
STRAP_AGPSBA=0 : sideband enabled
STRAP_AGPSBA=1 : pipelined only transfers

TVED11   R142 1 ⟋⟍ 2 10K
STRAP_HOST=1 : AGP Mode

1z. NV15 HOST STRAPS

2a. DAC I/O

Size	CAGE Code		DWG NO		Rev
C					2

| Scale | | | Sheet | 6 | of | 18 |

Thursday, September 13, 2001

2b. NV15 DAC/TV/TMDS

TVED[11:0] 5,14,16,17
VIPD[7:0] 5,14

R402 2.2K
R403 2.2K

R405 1 2 33R SDA SDA 15,17
R404 1 2 33R SCL SCL 15,17

U100B

Pin	Signal		Signal	Pin
AD2	VD50CLAMP0	VIPPCLK	D5	VIPPCLK → VIPPCLK
AB4	DDCSCL0	VIPD0	M5	VIPD0
AD3	DDCSDA0	VIPD1	M4	VIPD1
AE2	DDCSCL1	VIPD2	L5	VIPD2
AE1	DDCSDA1	VIPD3	L4	VIPD3
		VIPD4	K3	VIPD4
		VIPD5	K4	VIPD5
B3	VIPHCLK	VIPD6	J3	VIPD6
A3	VIPHCTL	VIPD7	J4	VIPD7
C3	VIPHAD0	VIPD8	K5	VIPD8
B2	VIPHAD1	VIPD9	J5	VIPD9
V3	VIPHAD2	VIPD10	H5	VIPD10
V2	VIPHAD3	VIPD11	H4	VIPD11
A2	VIPHAD4	VIPD12	G4	VIPD12
W5	VIPHAD5	VIPD13	F4	VIPD13
V5	VIPHAD6	VIPD14	E4	VIPD14
U5	VIPHAD7	VIPD15	D4	VIPD15

VIPD[15:0] 5,14

5V

CSCL
CSDA
CDDCSCL 6
CDDCSDA 6

VIPHCLK 14
VIPHCTL 14
VIPHAD0 14
VIPHAD1 14
VIPHAD2 14
VIPHAD3 14
VIPHAD4
VIPHAD5
VIPHAD6
VIPHAD7

C214 0.1UF

D7	BUFFRST#	BUFFRST_	→ BUFFRST_ 17
AF1	GPIO0	GPIO0	→ GPIO0 2
AC4	GPIO1	GPIO1	→ GPIO1 15
AE3	HSYNC	DACHSYNC	→ DACHSYNC 6,14
AF2	VSYNC	DACVSYNC	→ DACVSYNC 6

AGP3.3V
L211
1 2
150-220R_100MHZ
DACVDD

AC6 DACVDD

C215 0.1UF
C216 0.001UF
C217 0.01UF

AF4	RED	DACRED	→ DACRED 6
AE6	COMP	DACCOMP	
AD6	VREF	DACVREF	
AF5	RSET	DACRSET	
AE5	GREEN	DACGREEN	→ DACGREEN 6
AD5	DACGND	BLUE	AE4 DACBLUE → DACBLUE 6

R211 75R 1%
R213 75R 1%
R214 75R 1%

C218 0.01UF
R212 113R 1%

Place res as per guidelines------->
R899 1 2 NO STUFF

Place res as per guidelines------->

R897 1 2 0R IDUMP

AC5 PLLVDD
AF3 XTALIN XTALOUT AD4

V4	TVCLKIN	TVCLKOUT	V1 CTVECLKOUT → CTVECLKOUT 17
W1	TVVSYNC	TVD0(DPFD23)	AC1 TVED0
W3	TVHSYNC	TVD1(DFPD22)	AD1 TVED1
		TVD2(DFPD21)	AB3 TVED2
		TVD3(DFPD20)	AB2 TVED3
		TVD4(DFPD19)	Y4 TVED4
		TVD5(DFPD18)	AA3 TVED5
		TVD6(DFPD17)	W4 TVED6
		TVD7(DFPD16)	Y3 TVED7
		TVD8(DFPD15)	Y1 TVED8
		TVD9(DFPD14)	Y2 TVED9
		TVD10(DFPD13)	AA2 TVED10
		TVD11(DFPD12)	AA4 TVED11

17 TVECLKIN
17 TVEVSYNC
17 TVEHSYNC

R216 220K

TVED[11:0] 5,14,16,17

AB1	ROMCS#	ROMCS_	→ ROMCS_ 14
U3	DFPCLK	DFPCLK	→ DFPCLK 16
T4	DFPCLK#	DFPCLK_	→ DFPCLK_ 16
P4	DFPD0	DFPD0	→ DFPD[11:0] 16
P3	DFPD1	DFPD1	
R3	DFPD2	DFPD2	
P2	DFPD3	DFPD3	
R2	DFPD4	DFPD4	
R1	DFPD5	DFPD5	
T2	DFPD6	DFPD6	
T3	DFPD7	DFPD7	
T1	DFPD8	DFPD8	
R4	DFPD9	DFPD9	
U4	DFPD10	DFPD10	
U2	DFPD11	DFPD11	
U1	DFPEN		→ DFPEN 16
N4	DFPVSYNC	DFPVSYNC	→ DFPVSYNC 16
N5	DFPHSYNC	DFPHSYNC	→ DFPHSYNC 16
P5	DFPAVCC		
R5	DFPVREF	NC_DFPVREF	
T5	DFPAGND		

AGP3.3V

ULTRA A04 DF

100_100_20 14.31818MHZ
Y200
DACXTALIN 1 2 DACXTALOUT

C225 TBD NO STUFF
C223 10PF
C224 10PF

Use thick (non-impedance controlled) traces on XTALIN/OUT

nVIDIA

Size C CAGE Code DWG NO Rev 2
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U100D

U100C

Not required for testpoints since these are no internal connections

NVVDD   FBVDDQ

5V

C435
0.1UF

FBVDDQ   AGP3.3V

12   CFBBA[13:0]

12,13   FBDQM[15:8]

12   CFBDQS[15:8]
12   CFBBRAS_
12   CFBBCAS_
12   CFBBWE_
12   CFBBCS0_
12   CFBBCS1_
12   CFBBCLK0_
12   CFBBCLK0
12   CFBBCLK1_
12   CFBBCLK1
12   CFBBCKE

FBVREF

FBVDDQ

R300
1K

C981
0.1UF

C982
0.1UF

ULTRA A04 DF

10   CFBAA[13:0]

10,11   FBDQM[7:0]

10   CFBDQS[7:0]

10   CFBARAS_
10   CFBACAS_
10   CFBAWE_
10   CFBACS0_
10   CFBACS1_

10   CFBACLK0_
10   CFBACLK0
10   CFBACLK1_
10   CFBACLK1
10   CFBACKE

NVVDD

ULTRA A04 DF

3a. NV15 FBA/FBB

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3535 Monroe St
Santa Clara, CA 95051, USA

𝑛VIDIA

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3b. FB DECOUPLING

FBVDDQ C322 4.7UF NO STUFF
FBVDDQ C313 4.7UF NO STUFF

FBVDD C334 4.7UF NO STUFF
FBVDD C362 4.7UF NO STUFF
FBVDD

FBVDDQ C301 0.1UF
FBVDDQ C302 0.1UF
FBVDDQ C303 0.1UF
FBVDDQ C304 0.1UF
FBVDDQ C305 0.1UF
FBVDDQ C306 0.1UF
FBVDDQ C307 0.1UF
FBVDDQ C308 0.1UF
FBVDDQ C309 0.1UF
FBVDDQ C310 0.1UF
FBVDDQ C311 0.1UF
FBVDDQ C312 4.7UF

C438 0.1UF C436 0.1UF C314 0.1UF C315 2200PF C316 0.1UF C317 0.039UF

FBVDDQ C323 4.7UF FBVDDQ C324 2200PF FBVDDQ C325 2200PF C326 0.1UF FBVDDQ C327 0.039UF FBVDDQ C328 0.1UF FBVDDQ C329 0.1UF FBVDDQ C330 2200PF FBVDDQ C331 0.1UF FBVDDQ C332 2200PF FBVDDQ C333 0.1UF

NO STUFF AS PER FCC TEST

C318 0.1UF C320 0.1UF C321 0.039UF

C437 0.1UF C439 0.1UF C440 0.1UF C441 0.1UF C442 0.1UF C443 0.1UF C444 0.1UF C445 0.1UF C446 0.1UF C447 0.1UF C448 0.1UF C449 0.1UF C450 0.1UF

FBVDDQ

C335 0.1UF C336 0.1UF C337 0.1UF C338 0.1UF

C351 2200PF C352 2200PF C354 0.1UF

VTT

C375 4.7UF C376 0.1UF C377 0.1UF C378 2200PF C379 0.1UF C380 0.039UF C381 0.1UF

C361 4.7UF NO STUFF AS PER FCC TEST C363 4.7UF C364 0.1UF C365 0.1UF

C366 0.1UF C367 2200PF C368 0.1UF

C388 4.7UF C389 0.1UF C390 0.1UF C391 2200PF C392 0.1UF C393 0.039UF C394 0.1UF

C369 0.1UF C370 2200PF C371 0.1UF C372 0.039UF C373 2200PF C374 0.039UF

C401 4.7UF C402 0.1UF C403 0.1UF C404 2200PF C405 0.1UF C406 0.039UF C407 0.1UF

FBVDDQ

C382 0.1UF C383 0.1UF C384 0.1UF C385 0.1UF C386 0.1UF C387 0.1UF

VTT C339 4.7UF VTT C340 4.7UF VTT C341 4.7UF VTT C342 0.1UF C343 2200PF VTT C344 0.1UF C345 2200PF VTT C346 0.1UF C347 2200PF VTT C348 0.1UF

C395 0.1UF C396 0.1UF C397 0.1UF C398 0.1UF C399 0.1UF C400 0.1UF

VTT C355 0.1UF VTT C356 0.1UF VTT C357 0.1UF VTT C358 0.1UF VTT C359 0.1UF C360 0.1UF

3c1 FBA DDR 2MX32 SDRAM

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3c2. FBA DDR 2MX32 SDRAM TERM

VTT

RP304
5 4 FBD0
6 3 FBD1
7 2 FBD2
8 1 FBD3
75R

RP306
4 5 FBD7
3 6 FBD6
2 7 FBD5
1 8 FBD4
75R

RP309
8 1 FBD11
7 2 FBD10
6 3 FBD9
5 4 FBD8
75R

RP311
8 1 FBD15
7 2 FBD14
6 3 FBD13
5 4 FBD12
75R

VTT

RP305
4 5 FBD19
3 6 FBD18
2 7 FBD17
1 8 FBD16
75R

RP307
4 5 FBD22
3 6 FBD23
2 7 FBD20
1 8 FBD21
75R

RP308
8 1 FBD25
7 2 FBD26
6 3 FBD27
5 4 FBD24
75R

RP310
8 1 FBD28
7 2 FBD29
6 3 FBD30
5 4 FBD31
75R

VTT

R335 1 2 75R FBACLK0
NO STUFF

R880 1 2 68R

R336 1 2 75R FBACLK0
NO STUFF

R337 1 2 75R FBACLK1
NO STUFF

R881 1 2 68R

R338 1 2 75R FBACLK1
NO STUFF

FBD[127:0]   8,10,12,13
FBDQM[7:0]   8,10
FBACLK0   10
FBACLK0_   10
FBACLK1   10
FBACLK1_   10
FBACKE   10

C423 0.1UF   C421 0.1UF   C420 0.1UF

VTT

RP312
4 5 FBD32
3 6 FBD33
2 7 FBD39
1 8 FBD38
75R

RP314
4 5 FBD37
3 6 FBD36
2 7 FBD35
1 8 FBD34
75R

RP316
8 1 FBD51
7 2 FBD50
6 3 FBD49
5 4 FBD48
75R

RP318
8 1 FBD55
7 2 FBD54
6 3 FBD52
5 4 FBD53
75R

VTT

RP313
4 5 FBD41
3 6 FBD44
2 7 FBD42
1 8 FBD40
75R

RP315
4 5 FBD45
3 6 FBD47
2 7 FBD46
1 8 FBD43
75R

RP317
8 1 FBD59
7 2 FBD57
6 3 FBD58
5 4 FBD56
75R

RP319
8 1 FBD60
7 2 FBD61
6 3 FBD62
5 4 FBD63
75R

R339 1 2 75R FBDQM2
R340 1 2 75R FBDQM3
R341 1 2 75R FBDQM0
R342 1 2 75R FBDQM1
R343 1 2 75R FBDQM4
R344 1 2 75R FBDQM6
R345 1 2 75R FBDQM5
R346 1 2 75R FBDQM7

U305
4M = K4D263238M-5
2M = HY5DU643222AQ-5
2ME= M13L64322A-5
DDR-5
4M=NO STUFF:2M=2MX32:2ME=E2MX32

U306
DDR-5
4M=4MX32:2M=2MX32:2ME=E2MX32

U307
DDR-5
4M=NO STUFF:2M=2MX32:2ME=E2MX32

U308
DDR-5
4M=4MX32:2M=2MX32:2ME=E2MX32

FBD[127:0]   8,10,11,13
CFBBA[13:0]   8
CFBBRAS_   8
CFBBCAS_   8
CFBBWE_   8
CFBBCS0_   8
CFBBCS1_   8
CFBBCLK0   8
CFBBCLK0_   8
CFBBCLK1   8
CFBBCLK1_   8
CFBBCKE   8
CFBDQS[15:8] 8
CFBDQM[15:8] 8,13
FBBCLK0   13
FBBCLK0_   13
FBBCLK1   13
FBBCLK1_   13

3c4. FBB DDR 2MX32 SDRAM TERM

RP325 75R
4	5	FBD67
3	6	FBD68
2	7	FBD65
1	8	FBD64

RP327 75R
5	4	FBD75
6	3	FBD72
7	2	FBD73
8	1	FBD74

RP329 75R
1	8	FBD66
2	7	FBD70
3	6	FBD71
4	5	FBD69

RP331 75R
8	1	FBD77
7	2	FBD78
6	3	FBD79
5	4	FBD76

RP324 75R
4	5	FBD95
3	6	FBD91
2	7	FBD92
1	8	FBD94

RP326 75R
5	4	FBD84
6	3	FBD83
7	2	FBD85
8	1	FBD86

RP328 75R
8	1	FBD81
7	2	FBD82
6	3	FBD80
5	4	FBD87

RP330 75R
8	1	FBD88
2	7	FBD90
3	6	FBD89
4	5	FBD93

RP332 75R
5	4	FBD97
6	3	FBD96
7	2	FBD98
8	1	FBD100

RP334 75R
5	4	FBD108
6	3	FBD110
7	2	FBD109
8	1	FBD111

RP336 75R
8	1	FBD103
7	2	FBD101
6	3	FBD102
5	4	FBD99

RP338 75R
1	8	FBD104
2	7	FBD105
3	6	FBD107
4	5	FBD106

RP333 75R
4	5	FBD115
3	6	FBD114
2	7	FBD113
1	8	FBD112

RP335 75R
4	5	FBD119
3	6	FBD118
2	7	FBD117
1	8	FBD116

RP337 75R
8	1	FBD123
7	2	FBD122
6	3	FBD121
5	4	FBD120

RP339 75R
8	1	FBD126
2	7	FBD125
6	3	FBD127
5	4	FBD124

VTT

FBD[127:0]   8,10,11,12
FBDQM[15:8] 8,12
FBBCKE   12
FBBCLK0   12
FBBCLK0_   12
FBBCLK1   12
FBBCLK1_   12

R380 1 2 75R NO STUFF — FBBCLK0
R882 1 2 68R
R381 1 2 75R NO STUFF — FBBCLK0_
R382 1 2 75R NO STUFF — FBBCLK1
R883 1 2 68R
R383 1 2 75R NO STUFF — FBBCLK1_

C429 0.1UF   C430 0.1UF   C428 0.1UF   C431 0.1UF

R384 1 2 75R FBDQM11
R385 1 2 75R FBDQM10
R386 1 2 75R FBDQM9
R387 1 2 75R FBDQM8
R388 1 2 75R FBDQM14
R389 1 2 75R FBDQM15
R390 1 2 75R FBDQM12
R391 1 2 75R FBDQM13

5,7,16,17 TVED[11:0] TVEDI11:0I

VIPD[15:0] 5,7

U501

TVED0	12	A0	O0	13	VIPD0
TVED1	11	A1	O1	14	VIPD1
TVED2	10	A2	O2	15	VIPD2
TVED3	9	A3	O3	17	VIPD3
TVED4	8	A4	O4	18	VIPD4
TVED5	7	A5	O5	19	VIPD5
TVED6	6	A6	O6	20	VIPD6
TVED7	5	A7	O7	21	VIPD7
TVED8	27	A8			
TVED9	26	A9			
TVED10	23	A10			
TVED11	25	A11			

7	VIPHAD2	4 A12
7	VIPHAD3	28 A13
7	VIPHAD4	29 A14
6,7	DACHSYNC	3 A15

2 NC/A16
30 NC/A17

NC 1

AGP3.3V

7	ROMCS_ 22 CE VDD 32
7	VIPHAD0 24 OE
7	VIPHAD1 31 WE GND 16

C962
0.1UF

FLASH 64KX8 3.3V PLCC32

7   GPIO1

DFPHOTPLUG

R518
10K

R519
100K

D400
BAT54SLT1
NO STUFF

AGP3.3V

7,17   SDA   L505 1   2 150-220R_100MHZ   DVISDA   DVISDA   17
7,17   SCL   L506 1   2 150-220R_100MHZ   DVISCL   DVISCL   17

C520
220PF

C521
220PF

P400

16   DFPTX2+   DFPTX2+   R884   1   2 300R   2   TMDS DATA 2+   DDC Clk   6
16   DFPTX2-   DFPTX2-   NO STUFF   1   TMDS DATA 2-   DDC Data   7
HOT PLUG DETECT   16
5   TMDS DATA 4+   RED   C1   DVI_RED   8   RP500   1   MONRED   MONRED   6
4   TMDS DATA 4-   DVI_GREEN   7   2   MONGREEN   MONGREEN   6
16   DFPTX1+   DFPTX1+   R885   1   2 300R   10   TMDS DATA 1+   GREEN   C2   DVI_BLUE   6   3   MONBLUE   MONBLUE   6
16   DFPTX1-   DFPTX1-   NO STUFF   9   TMDS DATA 1-   BLUE   C3   5   4
0R
13   TMDS DATA 3+
12   TMDS DATA 3-   H SYNC   C4   MONHSYNC   6
16   DFPTX0+   DFPTX0+   R886   1   2 300R   18   TMDS DATA 0+   V SYNC   C8   MONVSYNC   6
16   DFPTX0-   DFPTX0-   NO STUFF   17   TMDS DATA 0-
21   TMDS DATA5+   A GND   C5A
20   TMDS DATA 5-   A GND   C5
16   DFPTXC0+   DFPTXC0+   R887   1   2 300R   23   TMDS CLK +   GND (ANALOG)   15
16   DFPTXC0-   DFPTXC0-   NO STUFF   24   TMDS Clk -
+5V POWER   14   DDCPOWER   6
26   MOUNTING
25   MOUNTING   TMDS CLK Shield   22
TMDS 2/4 Shield   3
TMDS DATA 1/3 Shield   11
TMDS DATA 0/5 Shield   19

F RA WHITE IRT

C522
0.1UF

M1002

SCREW HEX FOR DVI CONNECTOR

M1001

SCREW HEX FOR DVI CONNECTOR

5a. DVI-I I/O

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5a1. TV ENCODERS

MASTER TIMING

NTSC

SET BASE ADR TO 8A=1

Stuff for CX, No stuff for CH/BT

AGAINST PER CHRIS WOJSLAW

OR OR SHORT OK ?

Parts for Chrontel CH7008/8A only

U521

U522
CH7007 TQFP44

VAA3.3V   VAA3.3V   VAA3.3V   AGP3.3V   5V

4P 45-GND-SPRING
P401

BT=BT869:CX=CX25871

CX=10_10_18 13.50000MHz:BT=10_10_18 13.50000MHz:CH=10_10_18 14.31818MHZ

Y201 20PF LOAD CRYSTAL

600 OHM_100MHZ, 0.25 OHM DCR

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8a. NV15 POWER SUPPLY

Place L800 close to Q802

Place this caps close to L800
6 caps can be placed at the same location, stuffing alternative

Place this caps close to Q803
6 caps can be placed at the same location, stuffing alternative

L800 1uH 20%
IND_UNI_PAC1B Ferrite 4.4A

6 caps can be placed at the same location, stuffing alternative

NVVDD=2.05V

Place this caps close to L801
6 caps can be placed at the same location, stuffing alternative

Place L801, Q802 & D800 close together

VTT 1.25V@3.5A +/-125mV

Q803A IRF7311 Place this parts close together @Vgs=5.0V Rds(on) < 0.050 ohm

Q803B IRF7311

V0=1.25V

Place this caps close to L803
6 caps can be placed at the same location, stuffing alternative

U800 US3007

Q800 MTD3055V
Needs large copper for 2.5W power dissipation (>1sq inch)

Keep RC close to Q800 gate pin

ALL HIP PARTS NO STUFF

FBVDDQ OUT

Place this caps close to Q800
6 caps can be placed at the same location, stuffing alternative

Place this caps close to Q800
6 caps can be placed at the same location, stuffing alternative

SWR2 OUT (NVVDD)	R814	R815	R816
2.05V@4A +/-50mV	100R	No Stuff	4.02K
1.95V	100R	2.61K	No Stuff

R816=100/((2.05V/2)-1)
R815=130/(2-1.95v)

I=(3.3-0.5-2.05)/(10/4)=300mA Typ

2.05v

FBVDDQ OUT		R810	R811
2.5V	2.50V@1.5A +/-125mV	97.6R	100R
1.95V	1.95V for SDR	54.9R	100R
2.65V	2.50V@1.5A +/-125mV	110R	100R
2.705V		117R	102R
2.709V *		115R	100R
2.709V		110R	95.3R

R810=((LINEAR OUT/1.26)-1)*100(R811)

NVVDD PRE-CHARGE CKT

PZTA14 is another SOT-223 part.

FZT604/SOT-223 NO STUFF

ZENER 3.3V MMBZ5226BLT1/SOT23 NO STUFF

Resistor tolerances 5% unless specified

AGP3.3

4M=0R:2M=0R:2ME=NO STUFF

LINEAR=2.5V

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Size C	CAGE Code	DWG NO		Rev I

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