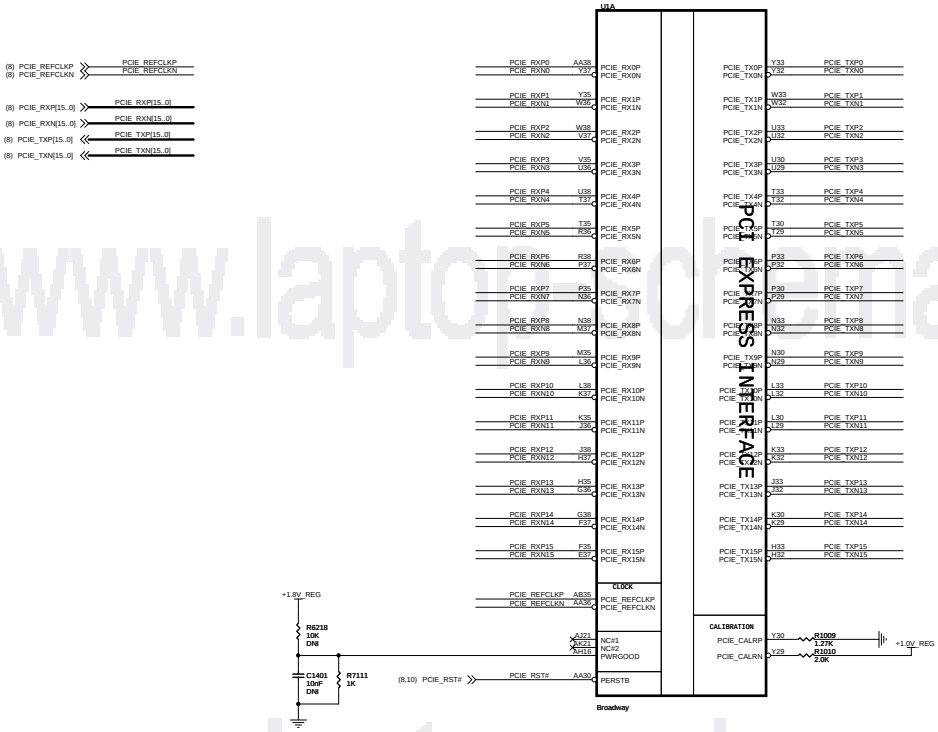

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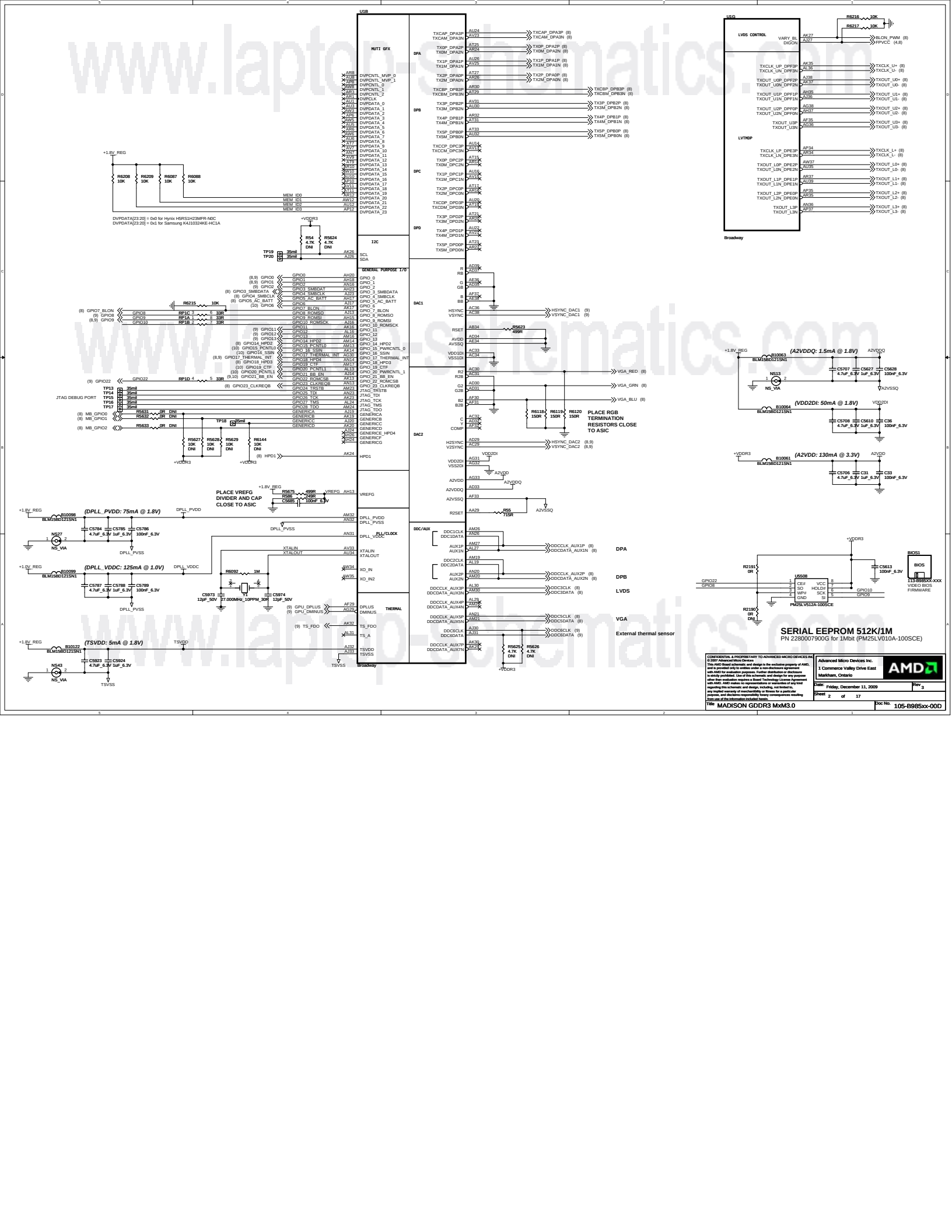
U1B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
DDC/AUX
PLL/CLOCK
THERMAL
VREFG
Broadway
U1G
LVDS CONTROL
LVTMDP
PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC
PLACE RGB TERMINATION RESISTORS CLOSE TO ASIC
(DPLL_PVDD: 75mA @ 1.8V)
(DPLL_VDDC: 125mA @ 1.0V)
(TSVDD: 5mA @ 1.8V)
(A2VDDQ: 1.5mA @ 1.8V)
(VDD2DI: 50mA @ 1.8V)
(A2VDD: 130mA @ 3.3V)
SERIAL EEPROM 512K/1M
PN 2280007900G for 1Mbit (PM25LV010A-100SCE)
MADISON GDDR3 MxM3.0
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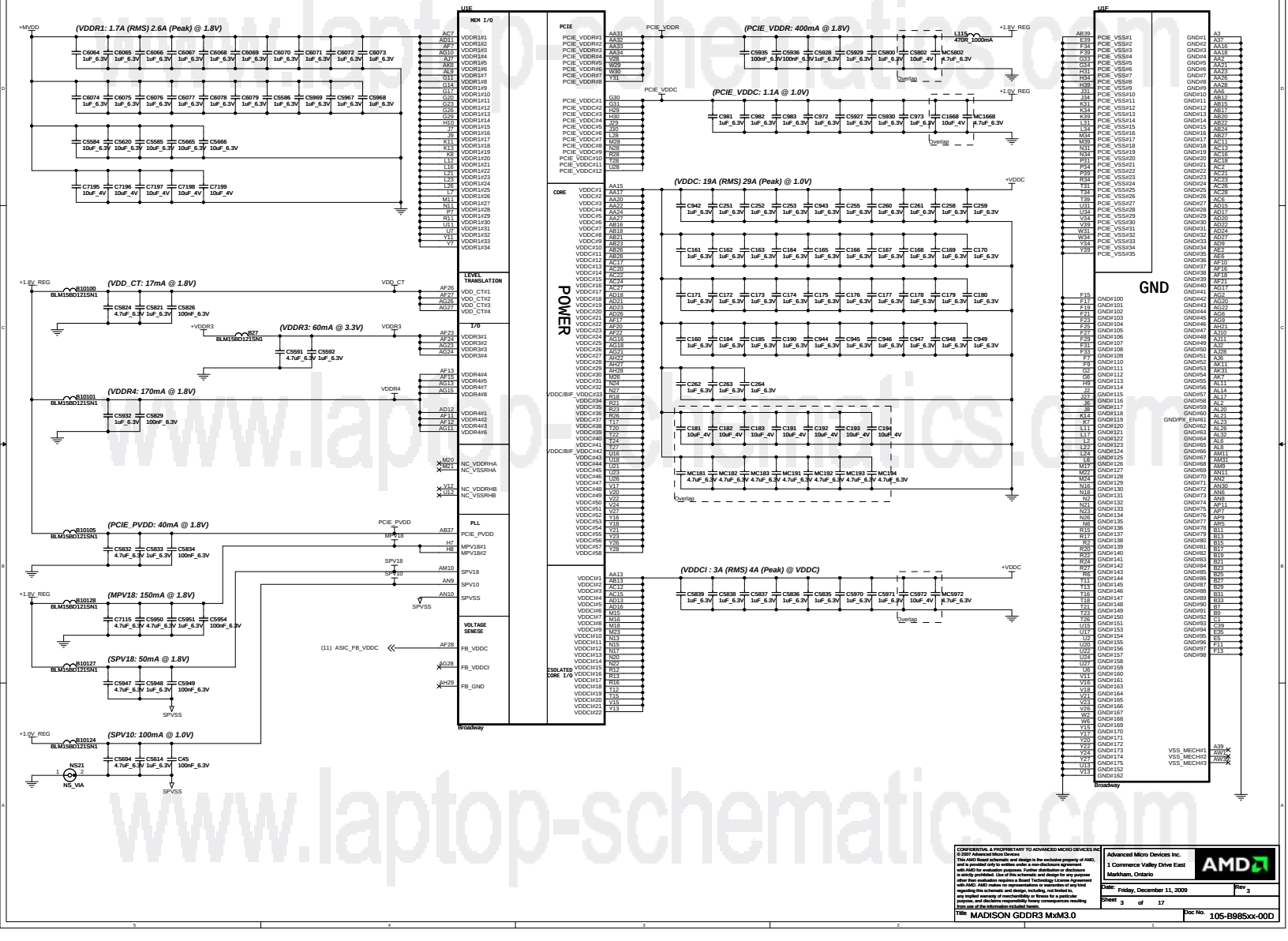

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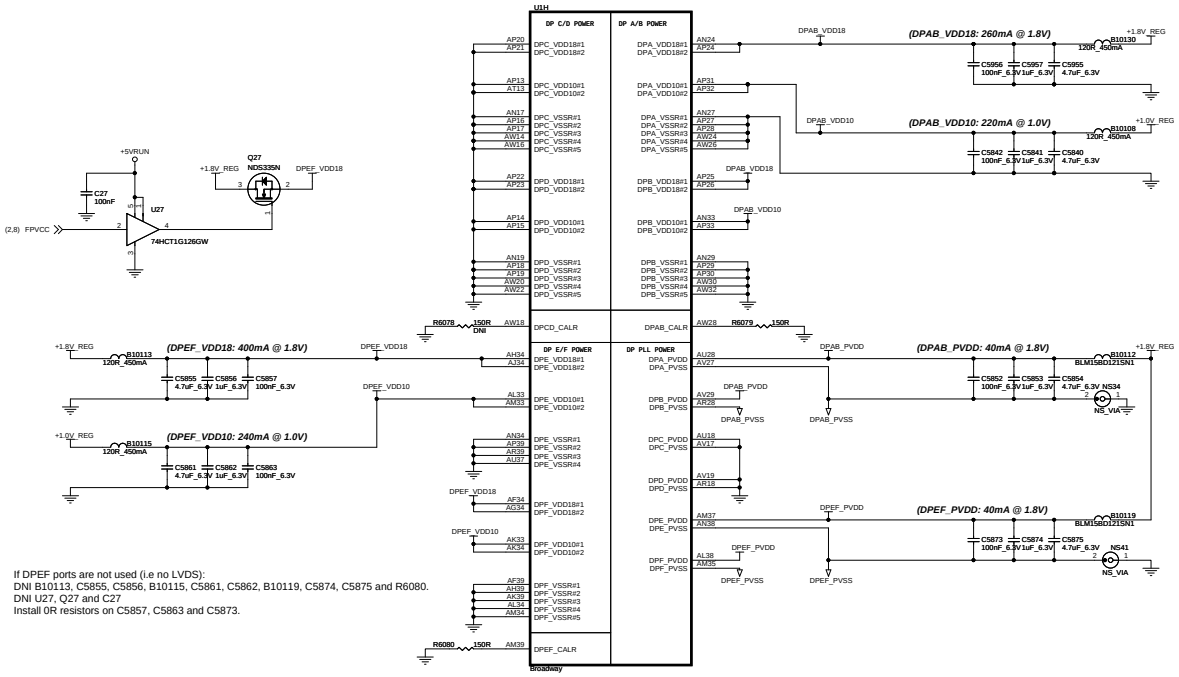

If DPEF ports are not used (i.e no LVDS):
DNI B10113, C5855, C5856, B10115, C5861, C5862, B10119, C5874, C5875 and R6080.
DNI U27, Q27 and C27
Install 0R resistors on C5857, C5863 and C5873.

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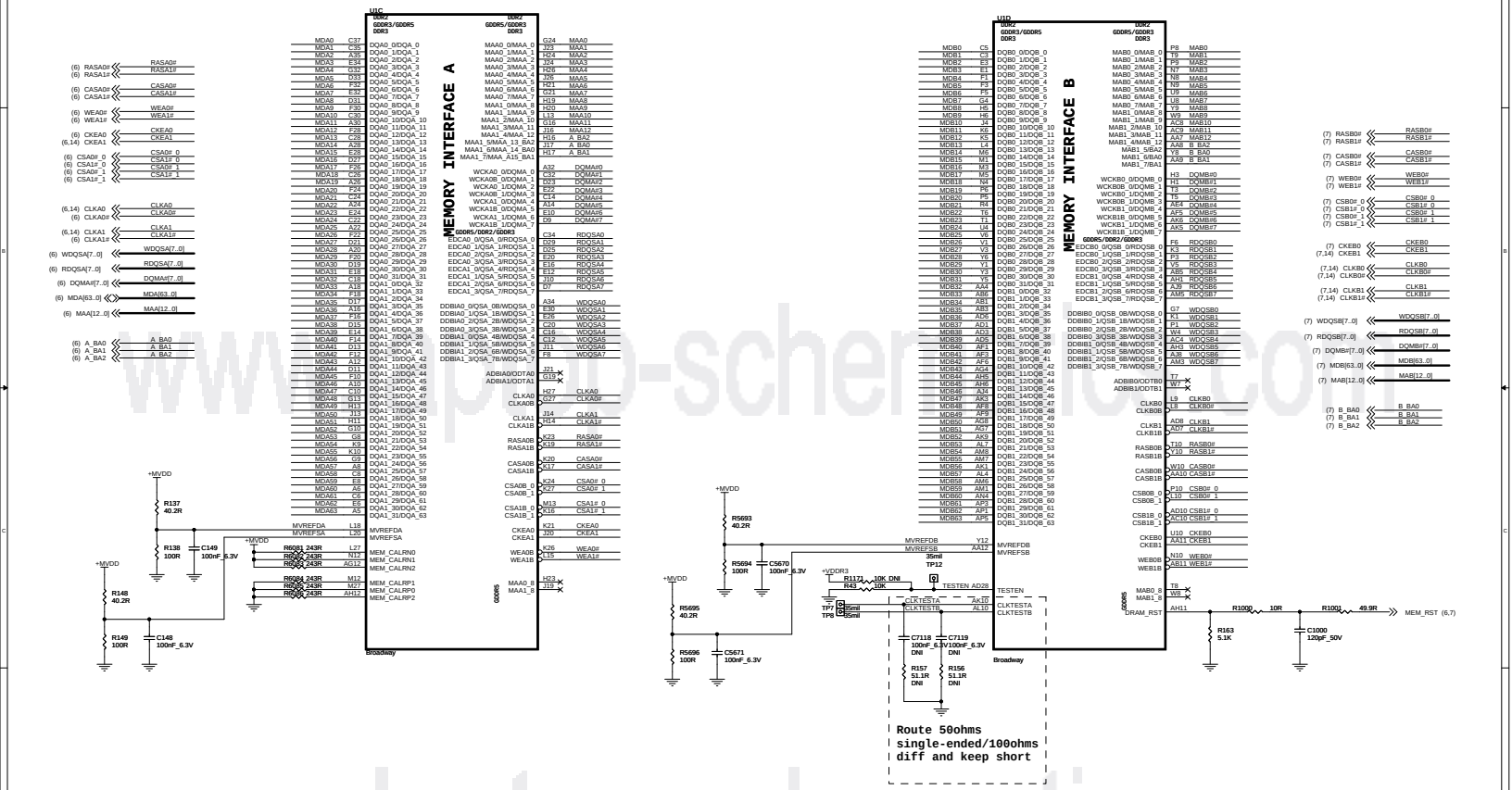

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GDDR3 32MX32 MEMORY

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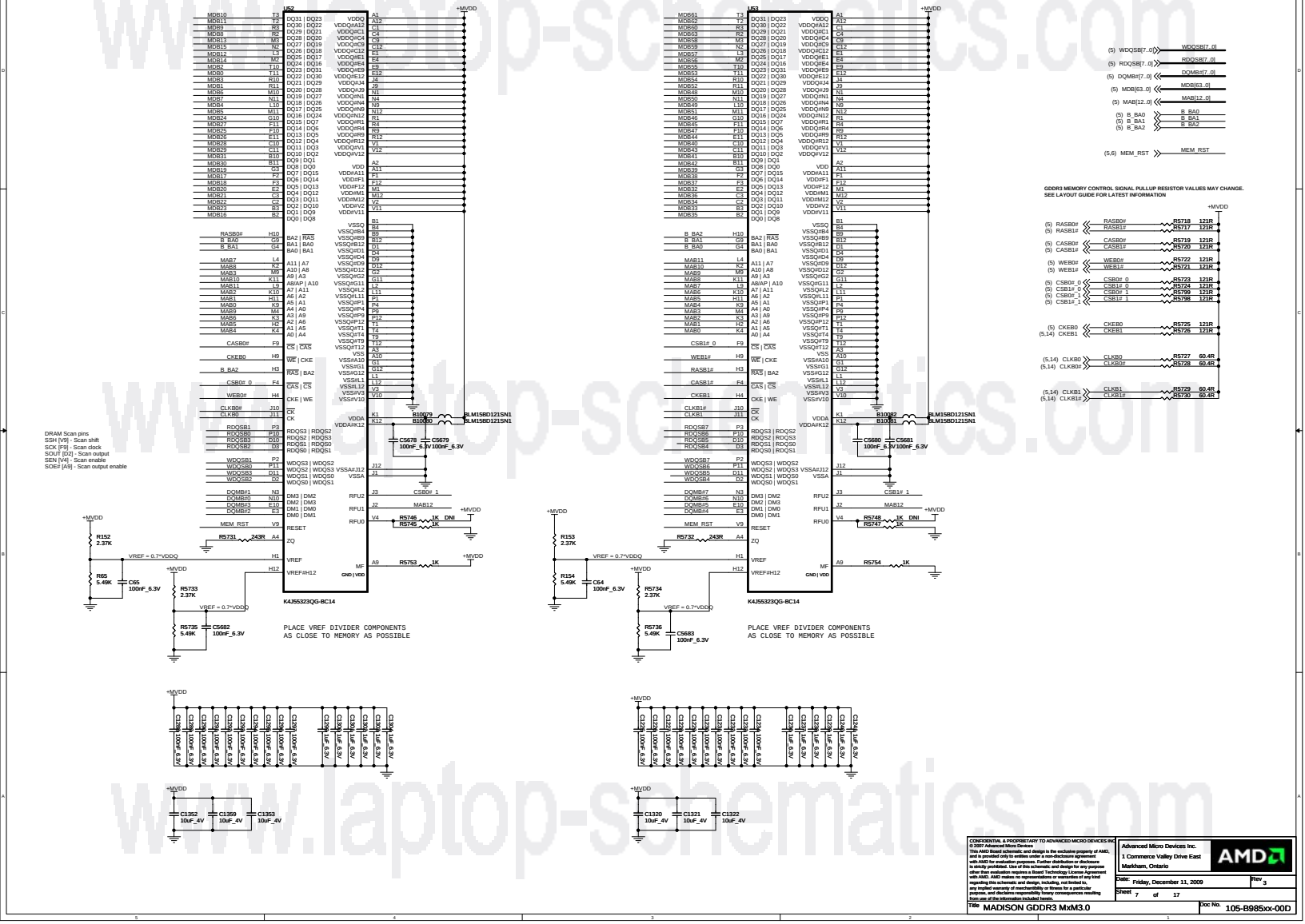
GDDR3 32MX32 MEMORY



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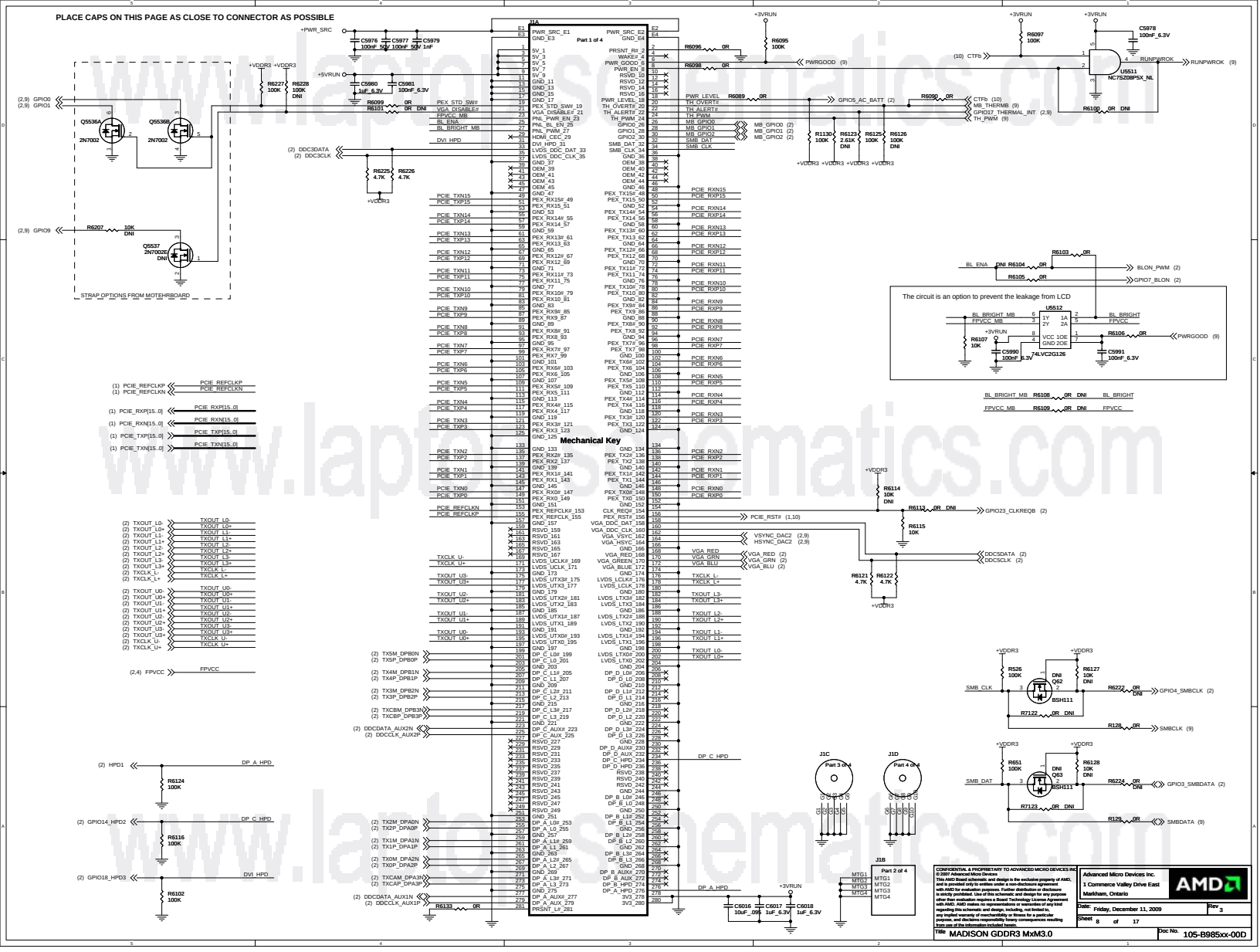

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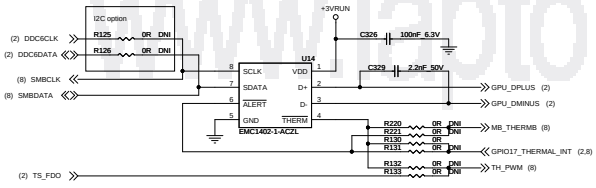
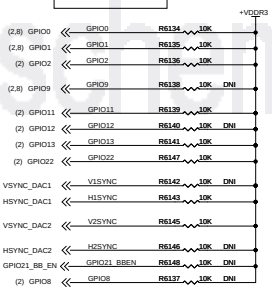
External Thermal Sensor



PIN STRAPS



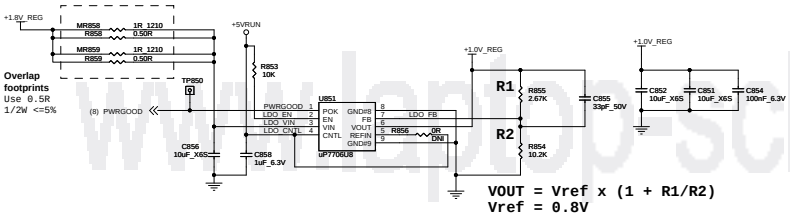
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing GPIO0 and GPIO1 pulls ups need to be stuffed with Q5536 if system board is controlling the PCIE swing.	1
TX_DEEMPH_EN	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE Gen2 Enable 0: Advertises the PCIE device as 2.5GT/s capable at power-on 1: Advertises the PCIE device as 5.0GT/s capable at power-on	1
BIF_VGA DIS	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU) GPIO9 pull up needs to be stuffed with Q5537 if system board is controlling the VGA capacity	0
ROMIDCFG[2:0]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select if GPIO22 = 0, defines memory aperture size if GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	101
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	1
AUD[1] AUD[0]	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	10
VIP_DEVICE_STRAP_DIS	V2SYNC	VIP Device Strap Enable 0: Slave VIP host port devices present 1: No slave VIP host port devices reporting presence	1
SMS_EN_HARD GPIO21_BBEN BIF_CLK_PM_EN	H2SYNC GPIO21_BBEN GPIO8	Reserved Reserved Reserved	0

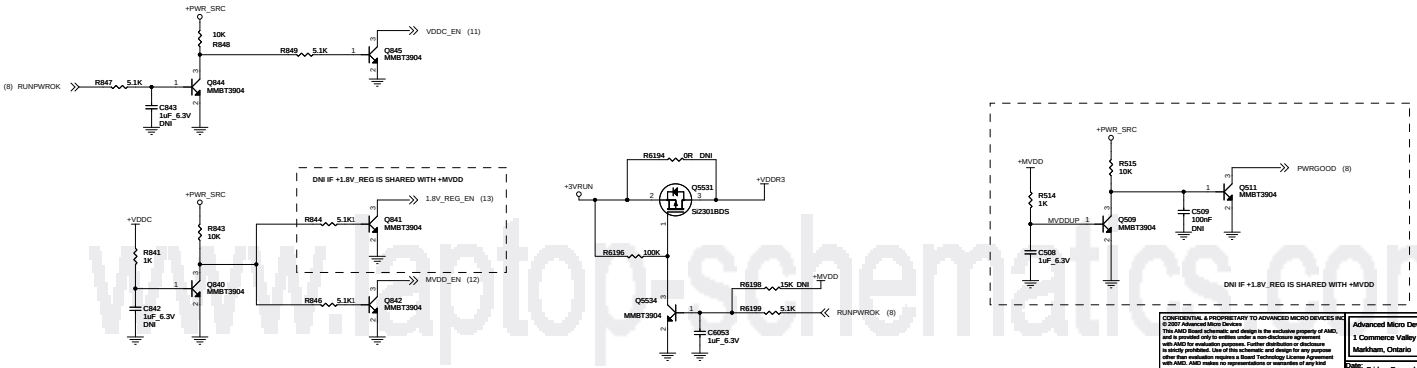
LDO Vin = +1.8V +/-5% Vout = +1.0V +/- 2% Iout = 1.7A RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



VOUT = Vref x (1 + R1/R2)
Vref = 0.8V

Power Up Sequence



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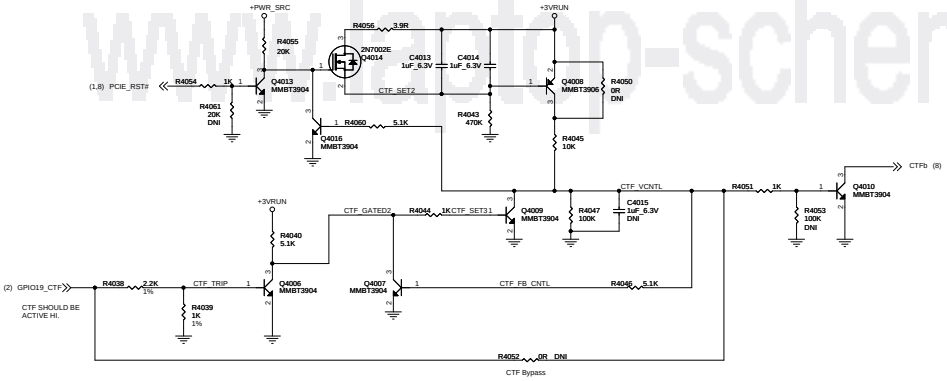
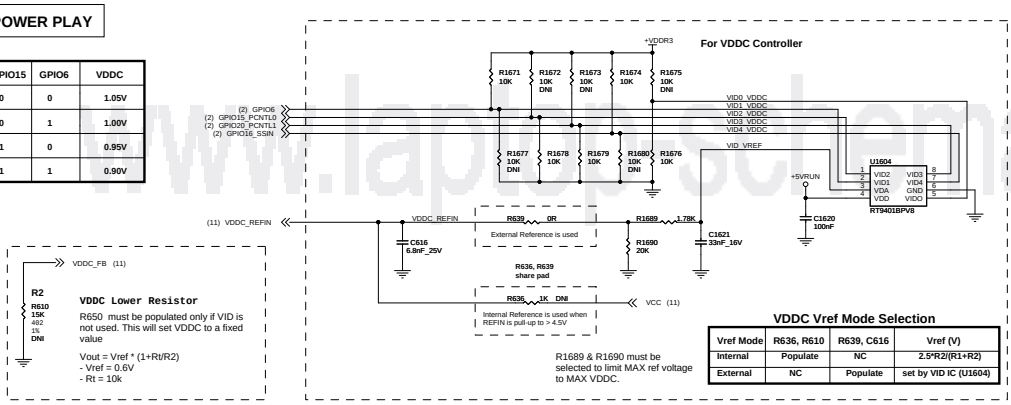
CRITICAL TEMPERATURE FAULT



POWER PLAY

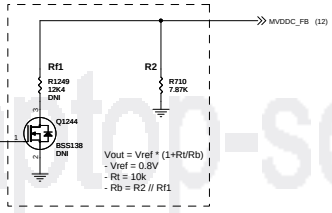
GPIO15	GPIO6	VDDC
0	0	1.05V
0	1	1.00V
1	0	0.95V
1	1	0.90V

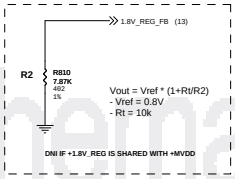


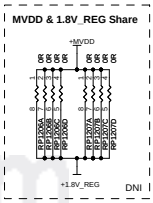
VDDC Vref Mode Selection

Vref Mode	R636, R610	R639, C616	Vref (V)
Internal	Populate	NC	2.5*R2/(R1+R2)
External	NC	Populate	set by VID IC (U1604)

GPIO21	MVDD
-	1.8V
-	-







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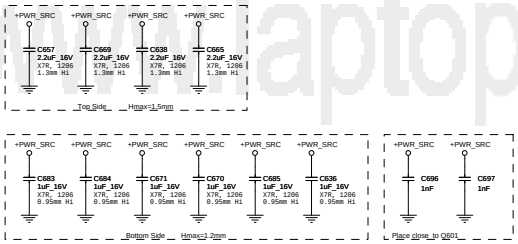
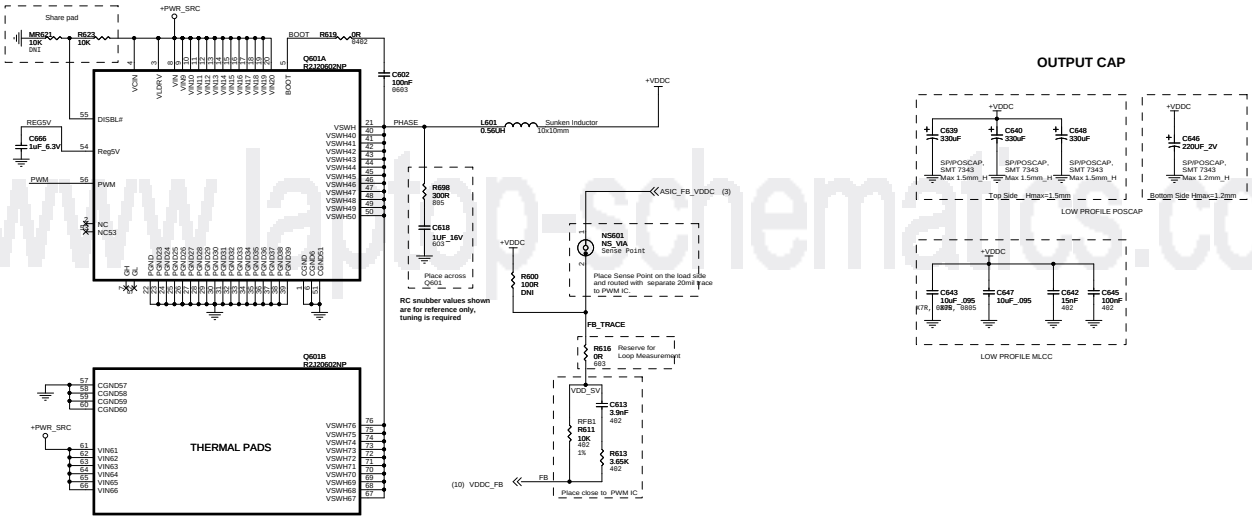
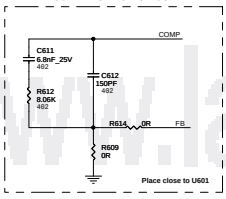
INPUT CAP



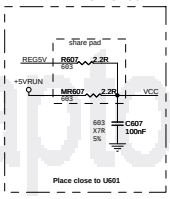


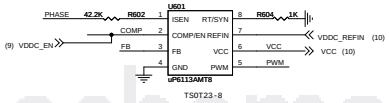
OUTPUT CAP

COMPENSATION CIRCUIT



FILTERED SMPS VCC





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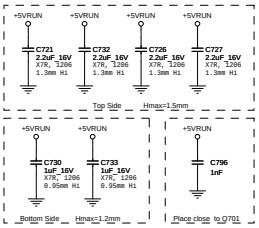
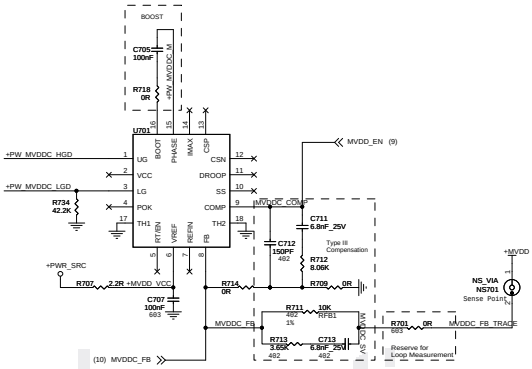
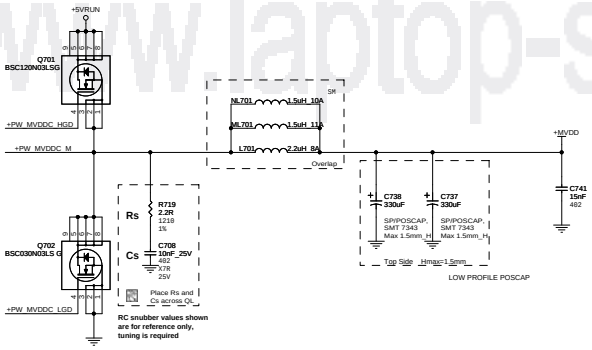
INPUT CAP







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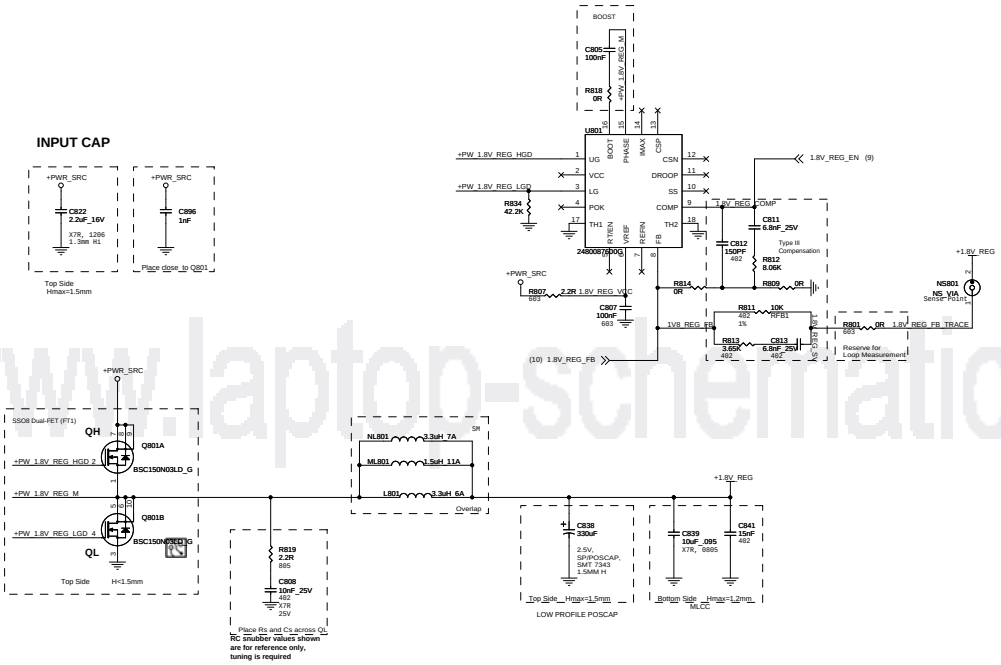

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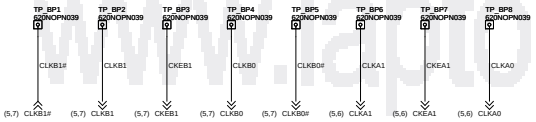

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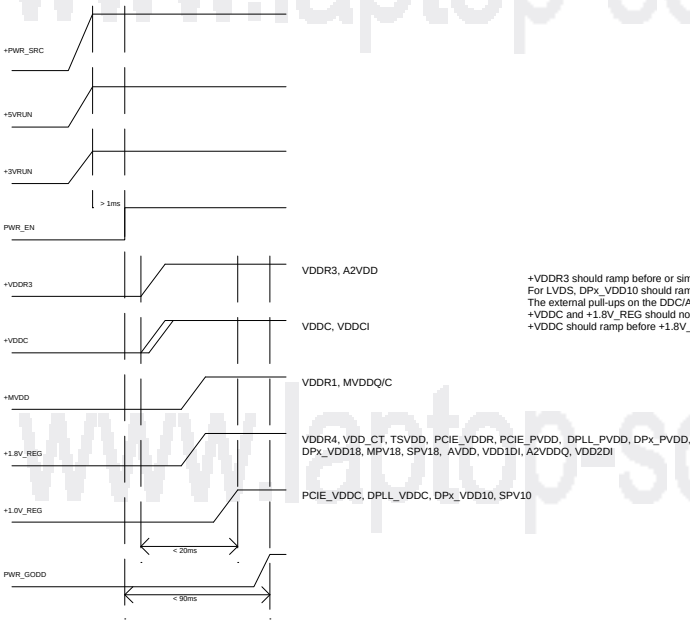
POWER UP SEQUENCE (not to scale)



+VDDR3 should ramp before or simultaneously with +VDDC.
For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and PCIe Reference clock should begin before DPx_VDD18.
The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both +VDDC and +1.8V_REG have ramped up.
+VDDC and +1.8V_REG should not ramp-up simultaneously.
+VDDC should ramp before +1.8V_REG and +1.0V_REG.

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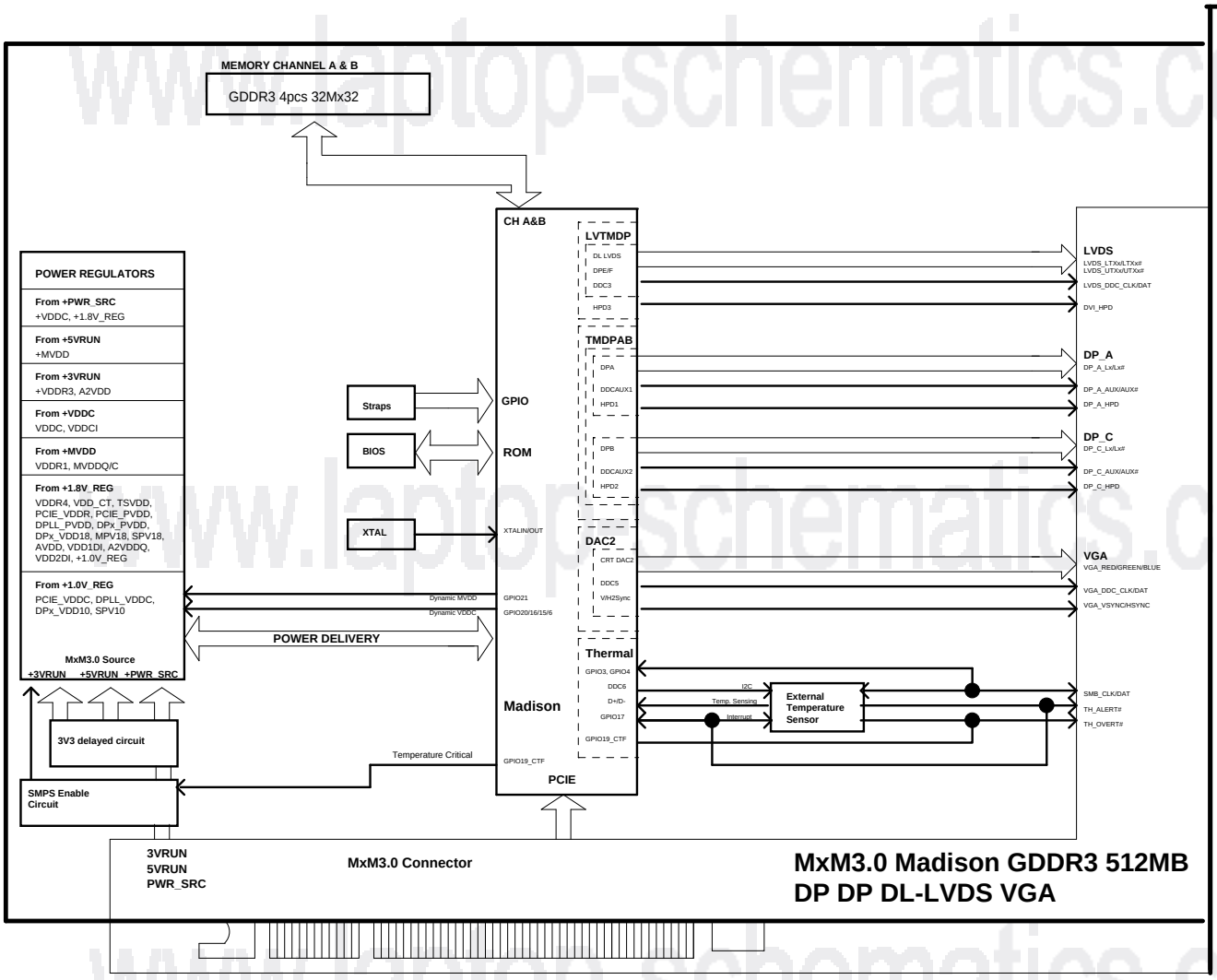

MxM3.0 Madison GDDR3 512MB
DP DP DL-LVDS VGA

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Title	Schematic No.	Date:
MADISON GDDR3 MxM3.0	105-B985xx-00D	Friday, December 11, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 3

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	09/06/02	Initial design for Madison GDDR3 MxM3.0 based on M96 B803
1	00B	09/08/27	Add U27, Q27, C27 - Gating circuit to delay DPEF_VDD18 Add R1677, R1678, R1679, R1680 - Pull downs for VID circuit Add R600 for debug Increase TP coverage
2	00C	09/10/30	Add C696, C697, C796, C896 (0402 input caps for power supplies) Add R1001 (DRAM_RST topology change) Change J1 symbol (inlcudes non-plated tooling holes) Move JTAG TPs out of the back plate area
3	00D	09/12/11	Pull back power planes