

NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X

PCI DEVICE ID 0X0=0X200 FOR NV20.

NVDD SET TO 1.60 FOR -VP CHIP

FBVDD SET TO: 3.47V

FBVDDQ SET TO: 2.59V

HISTORY REVISION:

X00: Based on P50-A06

- See change list in 149- file.
- Set FBVDDQ=2.59V

P50-A07-X01:

- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

P50-A08:

X04: - Delay PLL_VDD to come up after NVVDD.

X05: - Added 1UF accross R257.

X06: - Removed X04-5 above, added a switcher generated PLL delay option.

- SSENNA cap for 2nd SW changed to 1UF.
- A05 Si, NVVDD=1.52V

P50-A09:

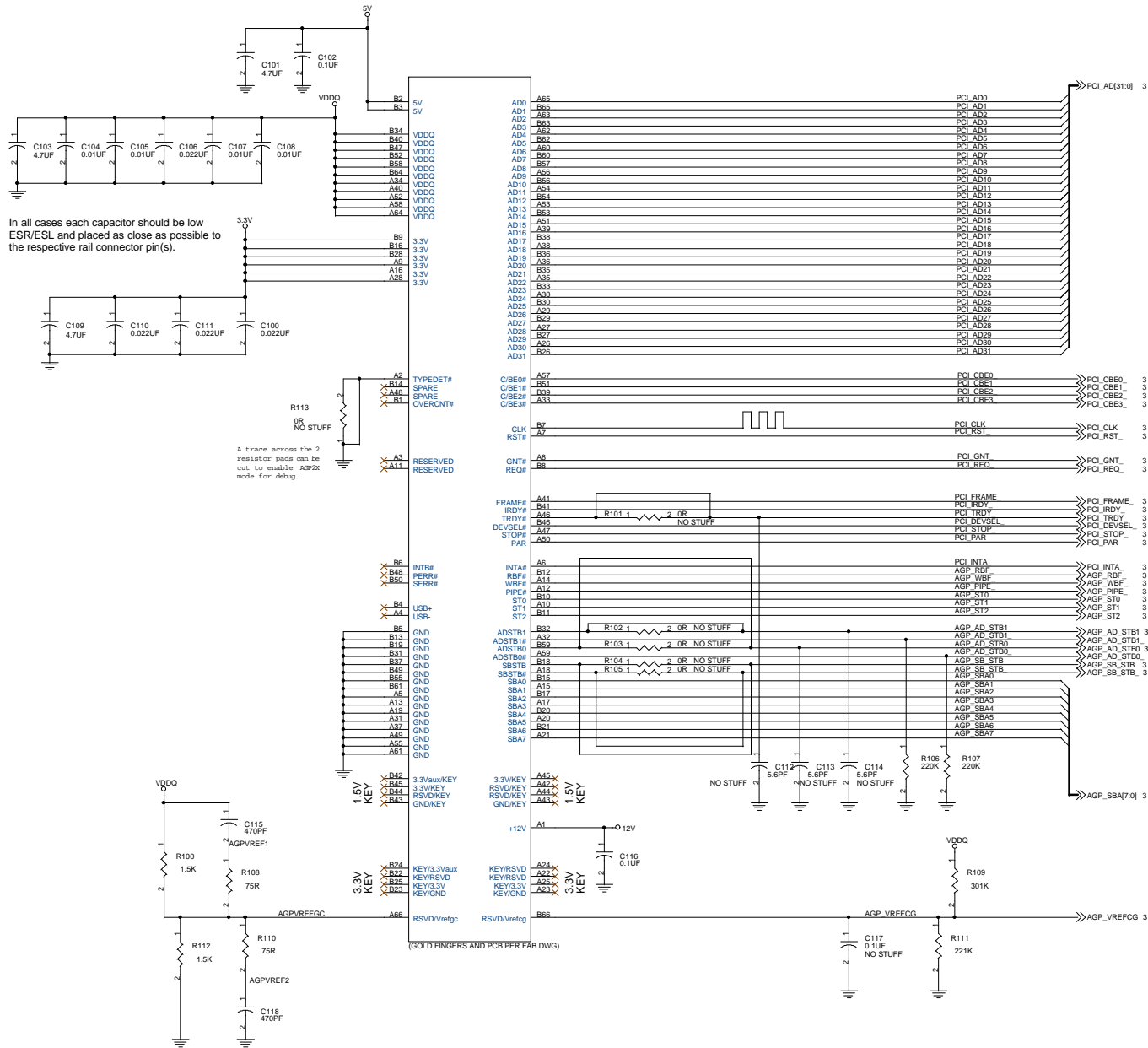
X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.

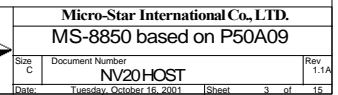
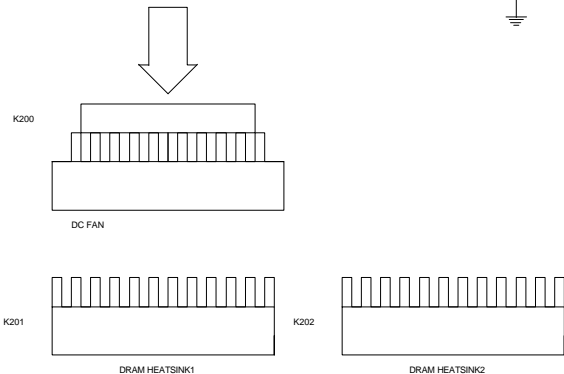
X03: - Added option to pull up power good to 12V

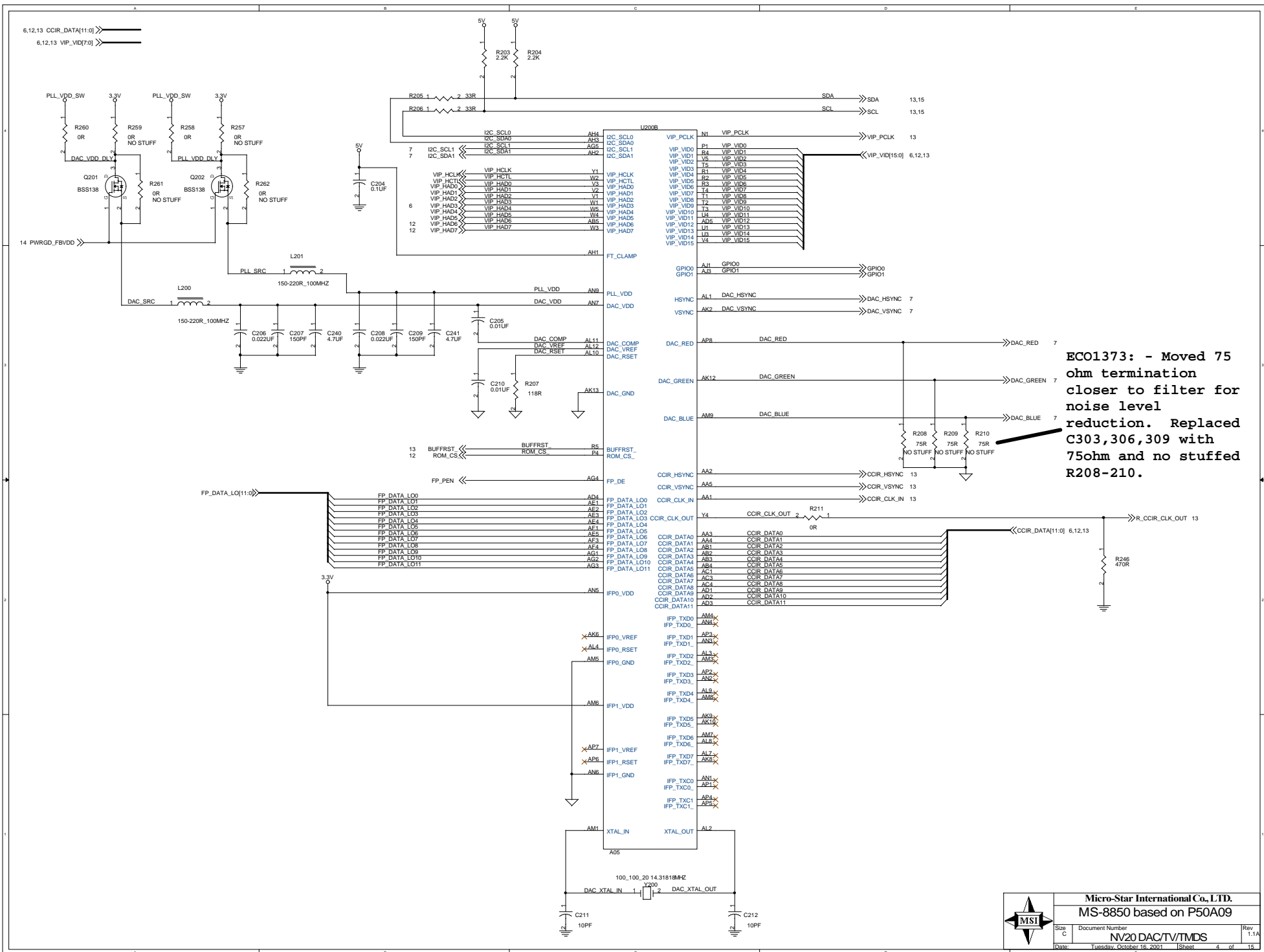
EC01235: - Changed R841 PU to 10K (from 4.7K)

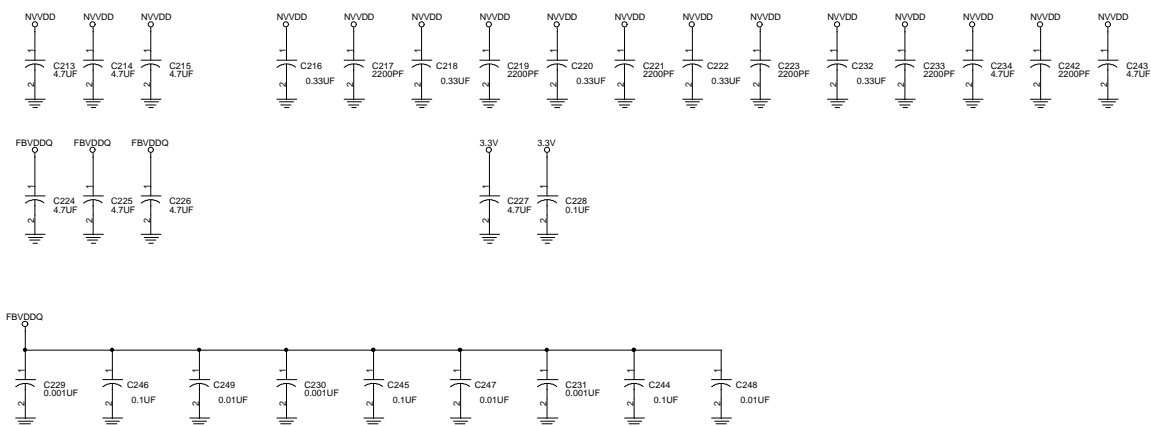
EC01373: - Moved 75 ohm termination closer to filter for noise level reduction. Replaced C303,306,309 with 75ohm and no stuffed R208-210.

- 1. GOLD FINGER
- 2. HOST
- 3. DAC/TV/TMDS
- 4. DECOUPING
- 5. STRAPS
- 6. CRT
- 7. FBA/FBB
- 8. DECOUPING
- 9. 2*32 DDR
- 10. 2*32 DDR
- 11. 1M FLASH ROM 3.3V
- 12. TV PH/7108
- 13. POWER
- 14. HARDWARE MONITOR

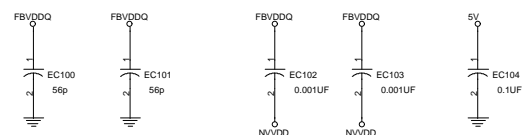








For EMI Solution



Micro-Star International Co., LTD.
MS-8850 based on P50A09

Size
C

Document Number
NV20 DECOUPLING

Rev
1.1A

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FBD_DATA0_R16	FBD_DATA0	FBC_DATA0	A34	FBC_DATA0
FBD_DATA1_A16	FBD_DATA1	FBC_DATA1	B33	FBC_DATA1
FBD_DATA2_E15	FBD_DATA2	FBC_DATA2	A33	FBC_DATA2
FBD_DATA3_C15	FBD_DATA3	FBC_DATA3	A32	FBC_DATA3
FBD_DATA4_D14	FBD_DATA4	FBC_DATA4	B31	FBC_DATA4
FBD_DATA5_C12	FBD_DATA5	FBC_DATA5	A32	FBC_DATA5
FBD_DATA6_D12	FBD_DATA6	FBC_DATA6	B30	FBC_DATA6
FBD_DATA7_A14	FBD_DATA7	FBC_DATA7	A29	FBC_DATA7
FBD_DATA8_C13	FBD_DATA8	FBC_DATA8	C29	FBC_DATA8
FBD_DATA9_B13	FBD_DATA9	FBC_DATA9	D28	FBC_DATA9
FBD_DATA10_A13	FBD_DATA10	FBC_DATA10	B28	FBC_DATA10
FBD_DATA11_A11	FBD_DATA11	FBC_DATA11	D27	FBC_DATA11
FBD_DATA12_A12	FBD_DATA12	FBC_DATA12	B27	FBC_DATA12
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FBD_DATA15_D11	FBD_DATA15	FBC_DATA15	D26	FBC_DATA15
FBD_DATA16_B11	FBD_DATA16	FBC_DATA16	A27	FBC_DATA16
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FBD_DATA28_G10	FBD_DATA28	FBC_DATA28	C17	FBC_DATA28
FBD_DATA29_G10	FBD_DATA29	FBC_DATA29	A17	FBC_DATA29
FBD_DATA30_H10	FBD_DATA30	FBC_DATA30	C16	FBC_DATA30
FBD_DATA31_H10	FBD_DATA31	FBC_DATA31	C16	FBC_DATA31

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FBD_ADR2_C10	FBD_ADR2	FBC_ADR2	A26	FBC_ADR2
FBD_ADR3_D10	FBD_ADR3	FBC_ADR3	D25	FBC_ADR3
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FBD_ADR5_B10	FBD_ADR5	FBC_ADR5	C23	FBC_ADR5
FBD_ADR6_C10	FBD_ADR6	FBC_ADR6	A23	FBC_ADR6
FBD_ADR7_D10	FBD_ADR7	FBC_ADR7	D22	FBC_ADR7
FBD_ADR8_G10	FBD_ADR8	FBC_ADR8	E24	FBC_ADR8
FBD_ADR9_B10	FBD_ADR9	FBC_ADR9	E21	FBC_ADR9
FBD_ADR10_A10	FBD_ADR10	FBC_ADR10	D21	FBC_ADR10
FBD_ADR11_B10	FBD_ADR11	FBC_ADR11	B18	FBC_ADR11
FBD_ADR12_C10	FBD_ADR12	FBC_ADR12	C21	FBC_ADR12
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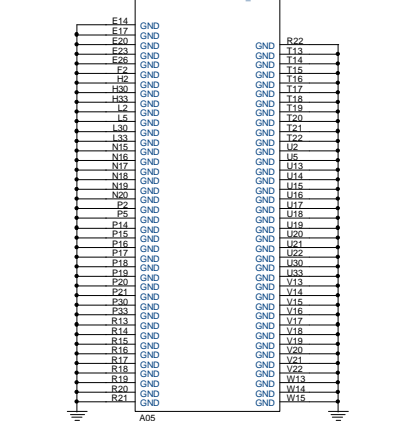
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FBD_DQM3_C15	FBD_DQM3	FBC_DQM3	B18	FBC_DQM3

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FBD_CKE_C8	FBD_CKE	FBC_CKE	A22	FBC_CKE

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FBD_CLK0B_A7	FBD_CLK0B	FBC_CLK0B	C22	FBC_CLK0B
FBD_CLK1_D9	FBD_CLK1	FBC_CLK1	A25	FBC_CLK1
FBD_CLK1B_C9	FBD_CLK1B	FBC_CLK1B	B25	FBC_CLK1B
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FBB_DATA2_W32	FBB_DATA2	FBA_DATA2	AM29	FBA_DATA2
FBB_DATA3_W32	FBB_DATA3	FBA_DATA3	AF30	FBA_DATA3
FBB_DATA4_W32	FBB_DATA4	FBA_DATA4	AF31	FBA_DATA4
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FBB_DATA14_W32	FBB_DATA14	FBA_DATA14	AM34	FBA_DATA14
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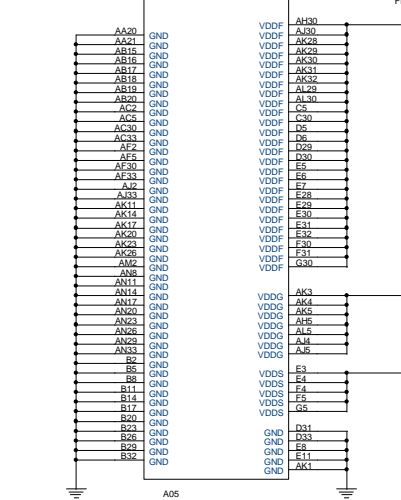
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FBB_ADR7_R31	FBB_ADR7	FBA_ADR7	AK33	FBA_ADR7
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FBB_DQM2_V31	FBB_DQM2	FBA_DQM2	AC31	FBA_DQM2
FBB_DQM3_V31	FBB_DQM3	FBA_DQM3	AS33	FBA_DQM3

FBB_DQS0_V32	FBB_DQS0	FBA_DQS0	AM30	FBA_DQS0
FBB_DQS1_V32	FBB_DQS1	FBA_DQS1	AL32	FBA_DQS1
FBB_DQS2_V32	FBB_DQS2	FBA_DQS2	AE30	FBA_DQS2
FBB_DQS3_V32	FBB_DQS3	FBA_DQS3	AA34	FBA_DQS3

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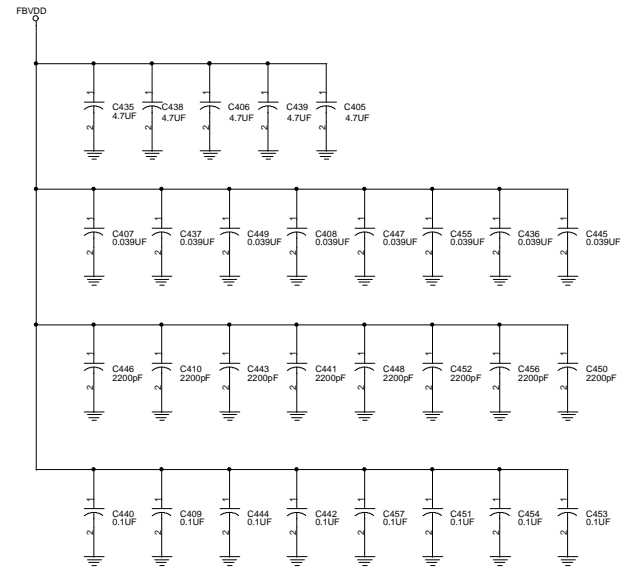
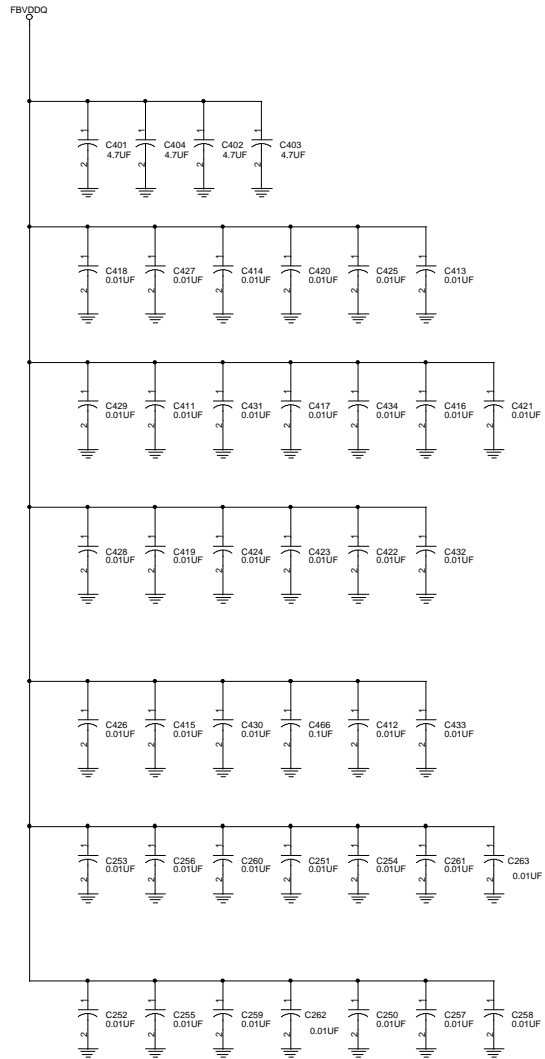
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FBB_CLK1B_K32	FBB_CLK1B	FBA_CLK1B	AH34	FBA_CLK1B
FBB_CKE_K31	FBB_CKE	FBA_CKE	AD31	FBA_CKE



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FBB_DATA31[31:0]	10
FBC_DATA31[31:0]	11
FBD_DATA31[31:0]	11
FBA_ADR[13:0]	10
FBB_ADR[13:0]	10
FBC_ADR[13:0]	11
FBD_ADR[13:0]	11
FBA_DQS[3:0]	10
FBB_DQS[3:0]	10
FBC_DQS[3:0]	11
FBD_DQS[3:0]	11
FBA_DOM[3:0]	10
FBB_DOM[3:0]	10
FBC_DOM[3:0]	11
FBD_DOM[3:0]	11
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FBA_CAS	10
FBA_WE	10
FBA_CS0	10
FBA_CLK0	10
FBA_CLK0B	10
FBA_CLK1	10
FBA_CLK1B	10
FBA_CKE	10
FBB_RAS	10
FBB_CAS	10
FBB_WE	10
FBB_CS0	10
FBB_CLK0	10
FBB_CLK0B	10
FBB_CLK1	10
FBB_CLK1B	10
FBB_CKE	10
FBC_RAS	11
FBC_CAS	11
FBC_WE	11
FBC_CS0	11
FBC_CLK0	11
FBC_CLK0B	11
FBC_CLK1	11
FBC_CLK1B	11
FBC_CKE	11
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FBD_CAS	11
FBD_WE	11
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FBD_CLK0	11
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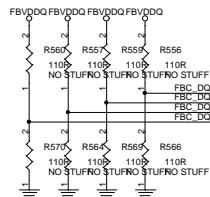
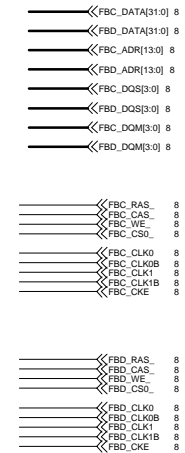


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Size C Document Number
FB DECOUPLING 4MX16 SDRAM

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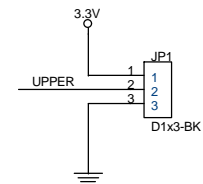
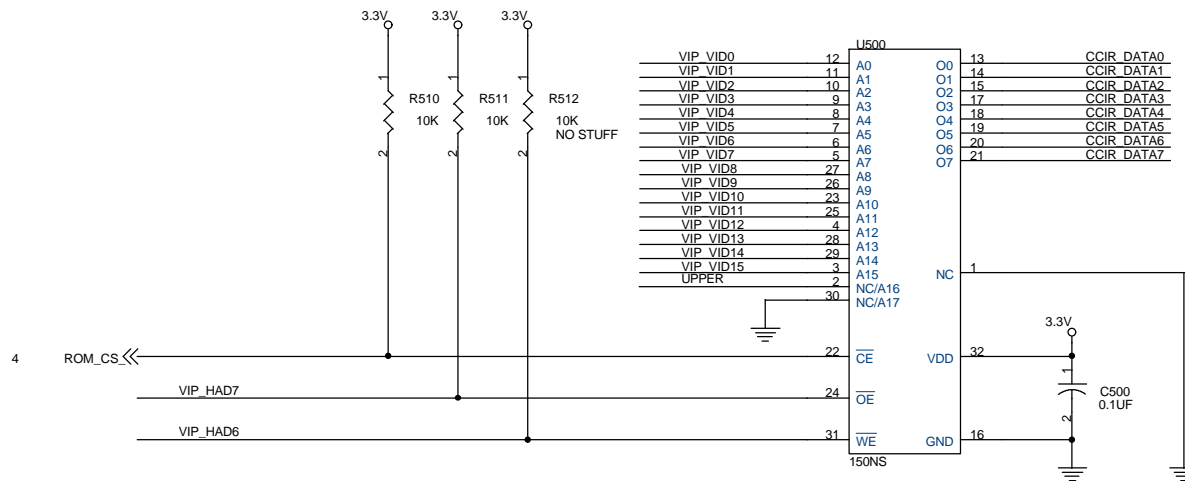
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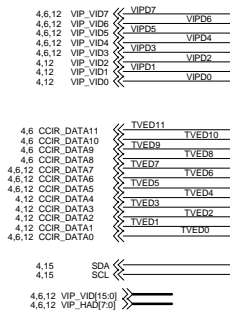
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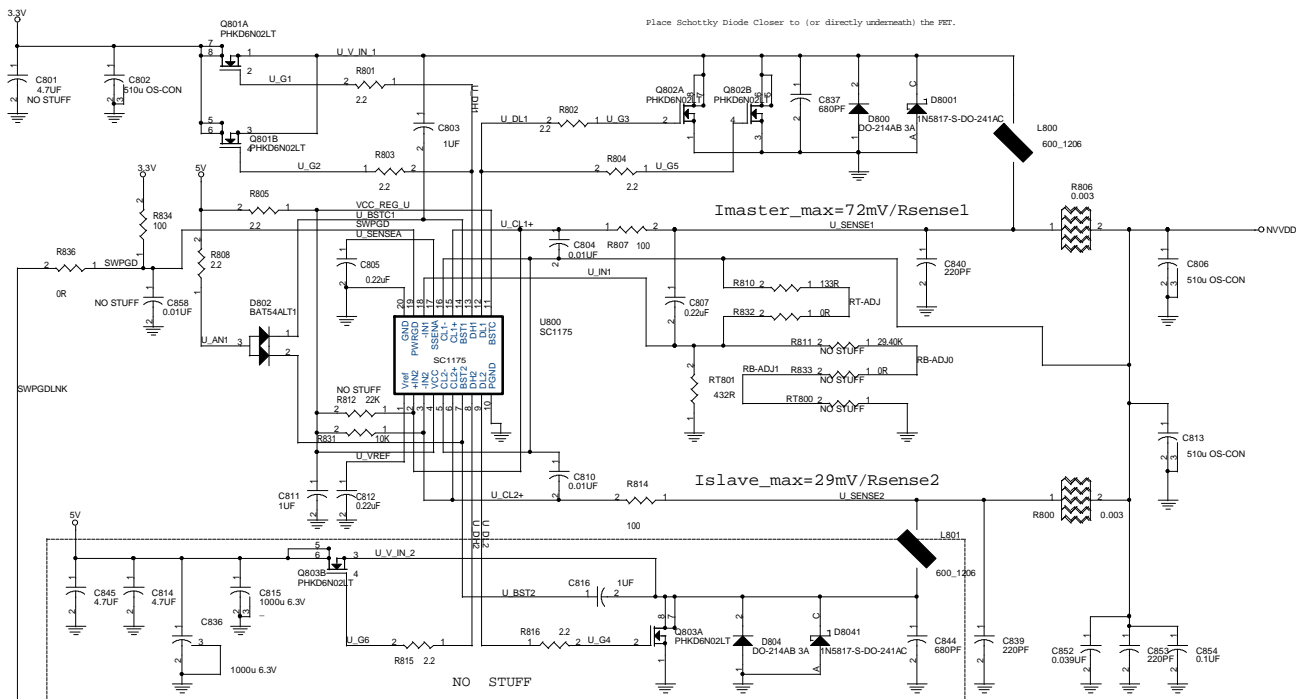
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4,13 VIP_PCLK <<
4 VIP_HCLK <<
4 VIP_HCTL <<
4 VIP_HAD0 >>
4 VIP_HAD1 >>
4 VIP_HAD2 >>
4,6 VIP_HAD3 >>
4 VIP_HAD4 >>
4 VIP_HAD5 >>
4 VIP_HAD6 >>
4 VIP_HAD7 >>
4,6,13 CCIR_DATA[11:0] >>
4,13 CCIR_HSYNC <<
4,13 CCIR_VSYNC <<
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4,13 R_CCIR_CLK_OUT <<
4,13 BUFRST_ <<
4,13,15 SCL <<
4,13,15 SDA <<

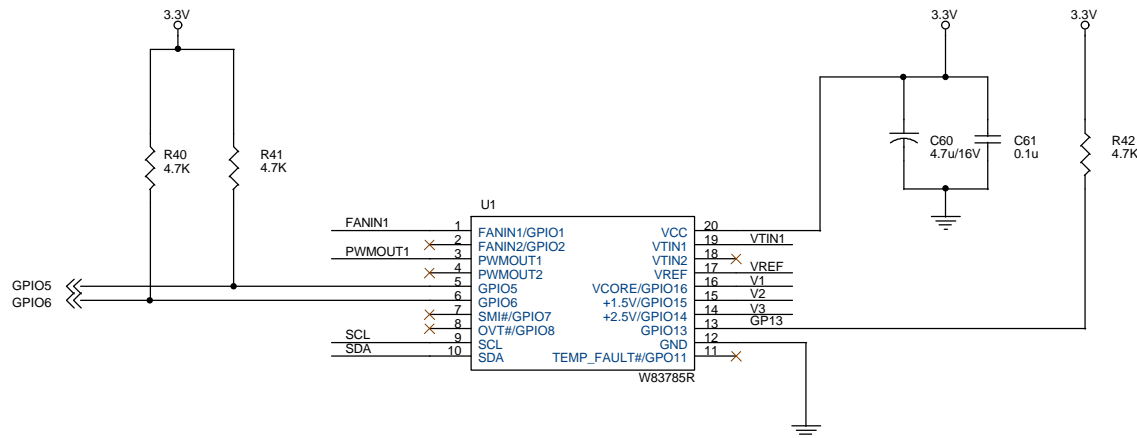
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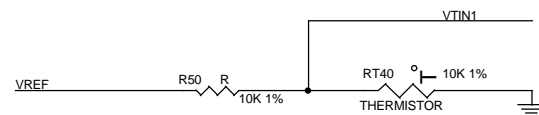
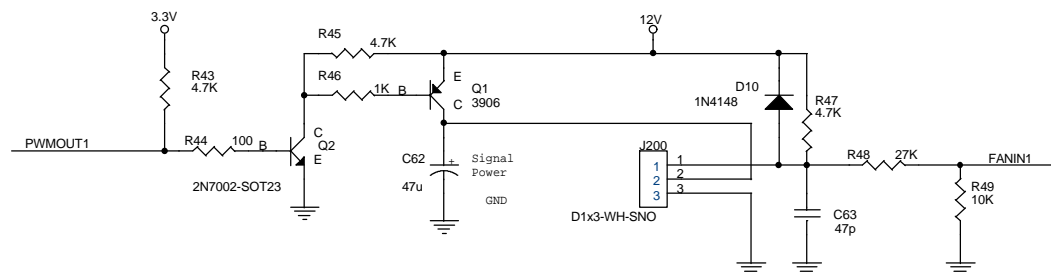
JP1(2-3)
JUMPER CAP -GREEN-(2-3)PIN





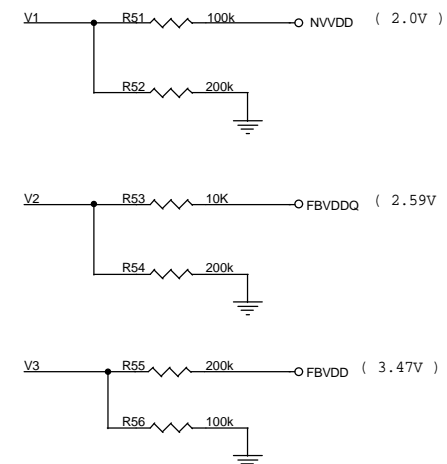


PWM1 Circuit for FAN1 speed Control
FOR 12V FAN



TEMPERATURE SENSING CIRCUIT

SDA << SDA 4,13
SCL << SCL 4,13



VOLTAGE SENSING CIRCUIT



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Size
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HARDWARE MONITOR

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