

P561: G98, DDR2 MEMORY 32MX16/16Mx16/64MX16

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Page 14: Power Supply II: F3V3, 5V, DDC5V, FBVDDQ

Page 15: Basenet Report

Page 16: Cref Part

REV HISTORY

History 10

96/09/27 page 08 add AV\_OUT

page 13 change Q1, Q2 to TO252

page 14 add FBVDDQ-linear block, change U2 footprint

96/09/28 page 07 change J4 footprint

page 12 add J7 (co-lay J6)

page 13 add R572 for RT9259A, R570 footprint change to 0805,

page 14 change L11, C11, C12, C31 footprint

remove PWM block

add D20, D21, C211, C212, C213, C214

96/10/01 page 14 add R210, R211

page 09 add R75~R88, R63~R69, L15~L21 for DVI (EMI\_solution)

96/10/02 page 12 add FAN Control Function

96/10/03 page 09 and netname (Between common Choke and DVI connector)

96/10/05 page 12 cnage Y501 (4 pin to 2 pin)

96/10/12 page 12 add L30, remove L10

96/10/12 baseon PCB:2.0 CIRCUIT DSN CAHNGE to PCB :1.0

ONLY CHANGE page 13 remove PWM solution, ADD linear solutin

remove C301~~C308 ( EMI solution for FBVDDQ)

96/10/17 page 11 add CABLE and PCB

96/10/18 page 14 add C301~~C308 ( EMI solution for FBVDDQ)

History 20

96/10/03 page 14 remove FBVDDQ-LINNEAR block, add FBVDDQ-PWM function

change L15 footprint as CHK4417C\_3R3S01, change C35 footprint

96/10/05 page 12 cahnge Y501 (4pin to 2 pin)

96/10/09 page 11 add FM1~~ FM6 for Fiducial Point

add U301~~U306 for EMI

page 13 add C309 for EMI

page 14 add C301~~C308, C310~~C312 for EMI

96/10/10 page 13 add L30

96/10/11 page 13 remove L10

96/10/17 page 11 add cable

History 21

96/11/06 page 13 add C11, C12 foot print C\_P3\_5\_D8\_H11\_5


page 14 change L15 footprint, increase PHASE's line width of FBVDDQ on top plane

96/11/07 page 13 add C211,C212,C213,C214

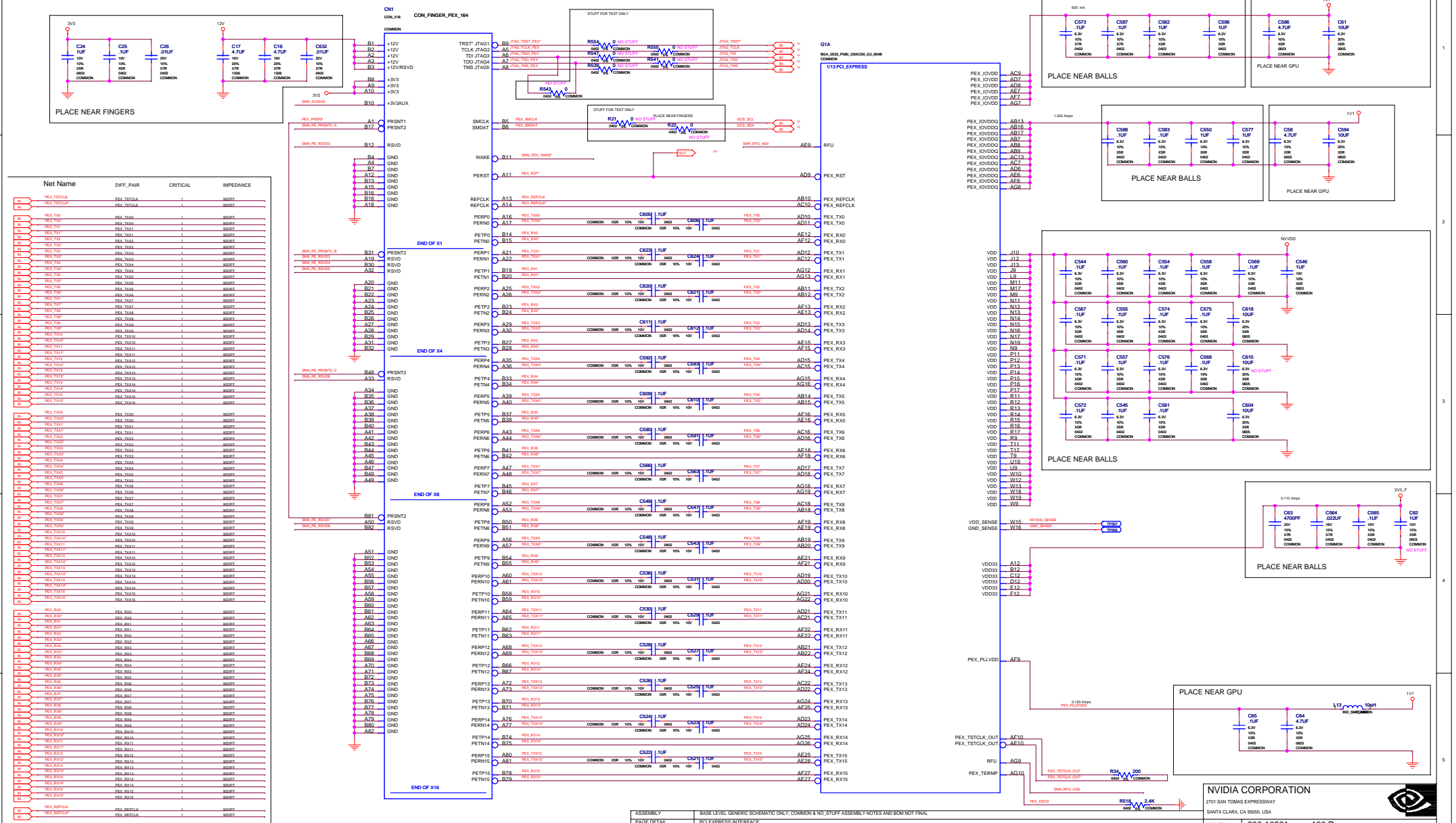
REV	VARIANT	NVPN	ASSEMBLY
0	BASE	600-10561-xxxx-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10561-0000-100	P561: G98-300, 64 BIT DDR2 16Mx16 MEMORY, VGA+DVI+Hdout
2	SKU0001	600-10561-0001-100	P561: G98-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+Hdout
3	SKU0987	600-10561-0987-100	P561: G98-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+HdOUT
4	SKU0997	600-10561-0997-200	P561: G98-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+HdOUT
5	SKU0001	600-10561-0001-200	P561: G98-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+HdOUT
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P561 Overview

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## PCI Express Interface



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PAGE DETAIL	PCI EXPRESS INTERFACE

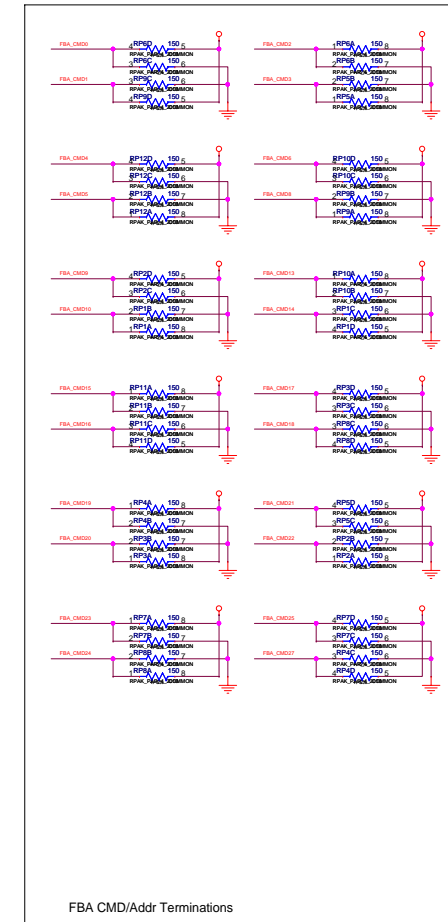
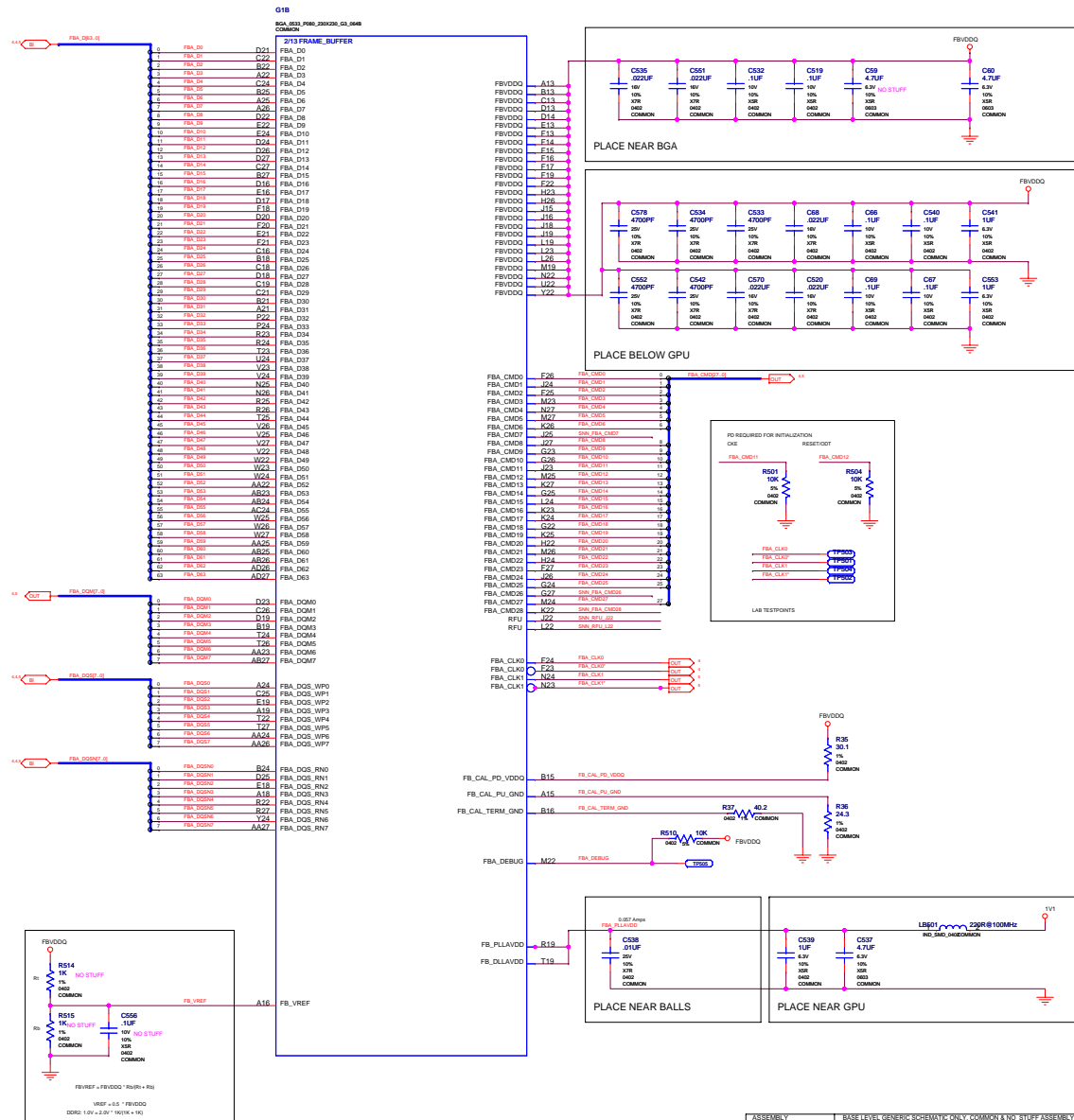
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## Frame Buffer Interface



### FBA CMD/Addr Terminations

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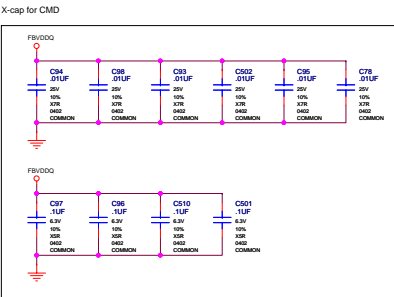
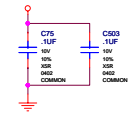
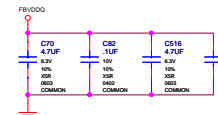
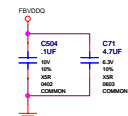
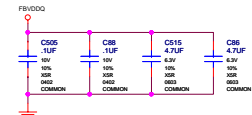
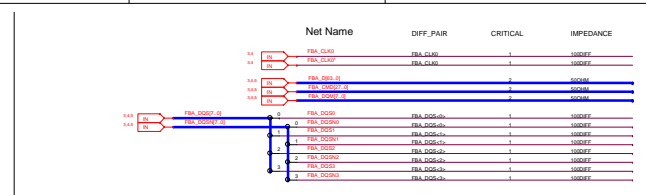
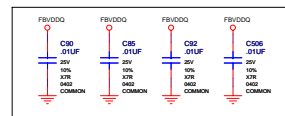
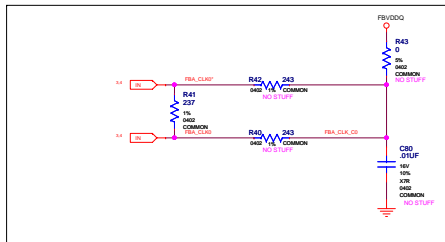
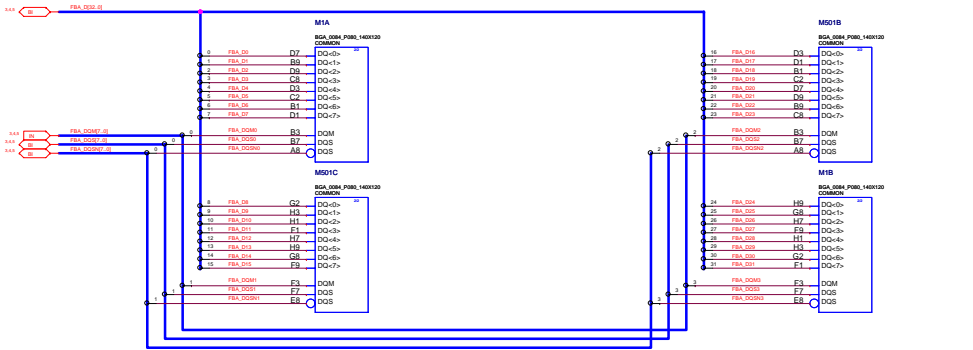
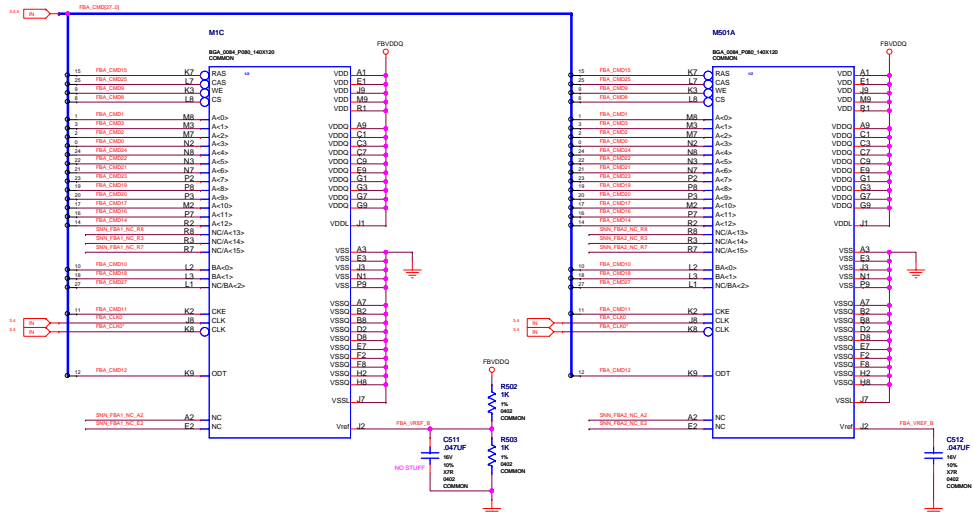
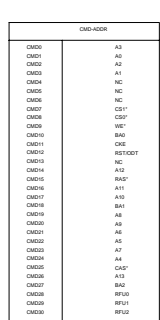
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PAGE DETAIL	Frame Buffer Interface

## Memory 1st Bank 0..31



### X-cap for CMD

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PAGE DETAIL	Memory 1st Bank 0.31

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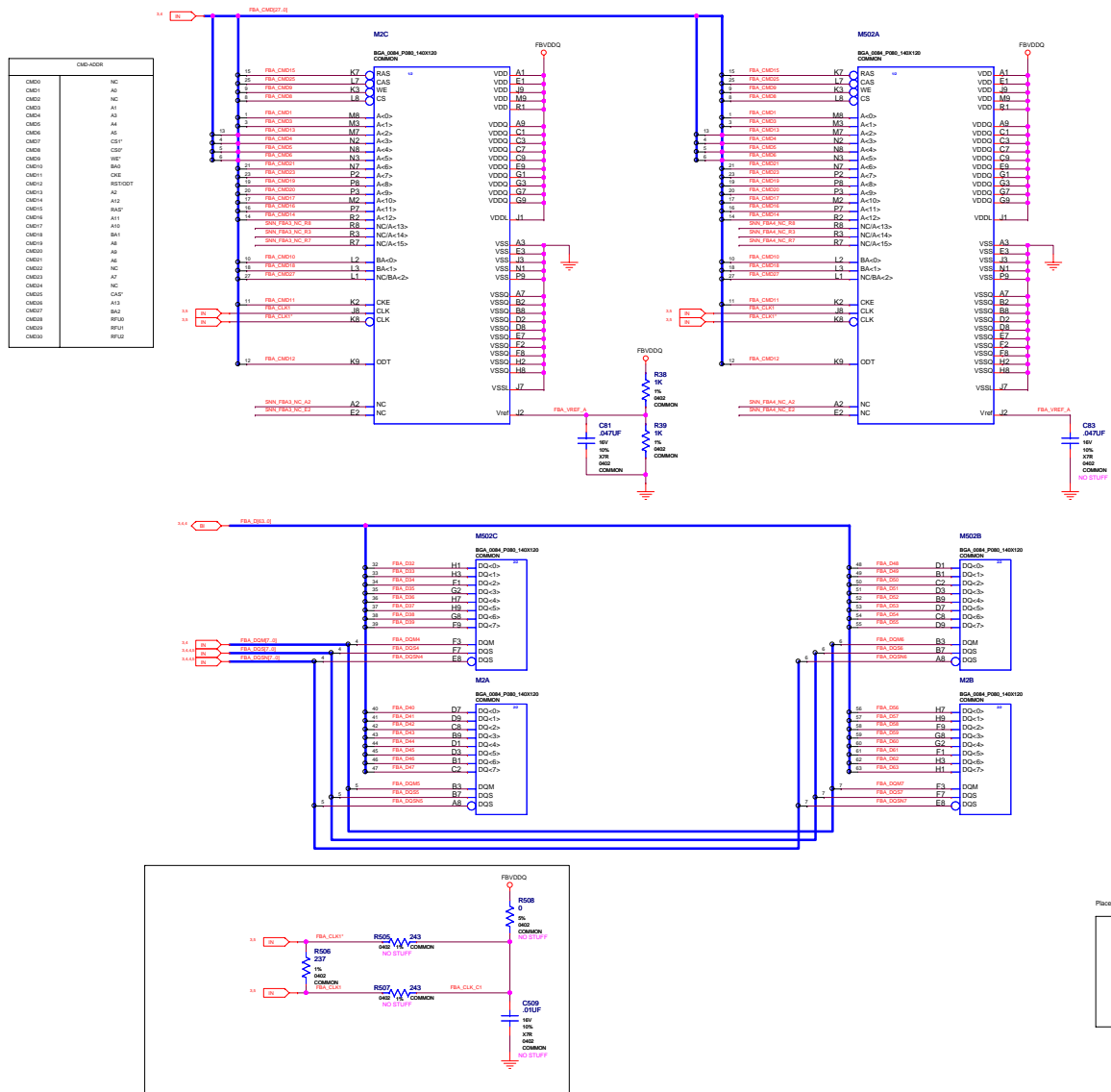
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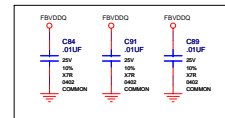
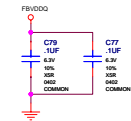
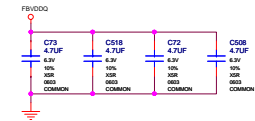
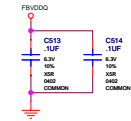
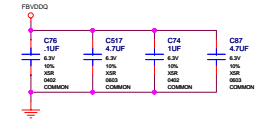
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NAME		DATE	31-AUG-2007



## Memory 1st Bank 32..63



		Net Name	DIFF_PAIR	CRITICAL	IMPEDANCE
		FBK_D041	FBK_D041_1	+	100ΩFF
		FBK_D042	FBK_D042_1	+	100ΩFF
		FBK_D043	FBK_D043_1	+	100ΩFF
144	144	FBK_D050_13	FBK_D050_1	+	100ΩFF
144	144	FBK_D050_14	FBK_D050_1	+	100ΩFF
		FBK_D051	FBK_D051_1	+	100ΩFF
		FBK_D052	FBK_D052_1	+	100ΩFF
		FBK_D053	FBK_D053_1	+	100ΩFF
		FBK_D054	FBK_D054_1	+	100ΩFF
		FBK_D055	FBK_D055_1	+	100ΩFF
		FBK_D056	FBK_D056_1	+	100ΩFF
		FBK_D057	FBK_D057_1	+	100ΩFF
		FBK_D058	FBK_D058_1	+	100ΩFF
		FBK_D059	FBK_D059_1	+	100ΩFF
		FBK_D060	FBK_D060_1	+	100ΩFF
		FBK_D061	FBK_D061_1	+	100ΩFF
		FBK_D062	FBK_D062_1	+	100ΩFF



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PAGE DETAIL	Memory 1st Bank 32.63

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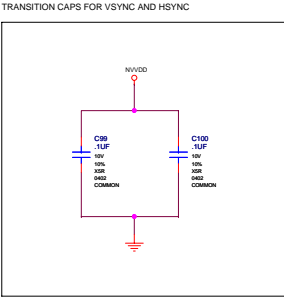
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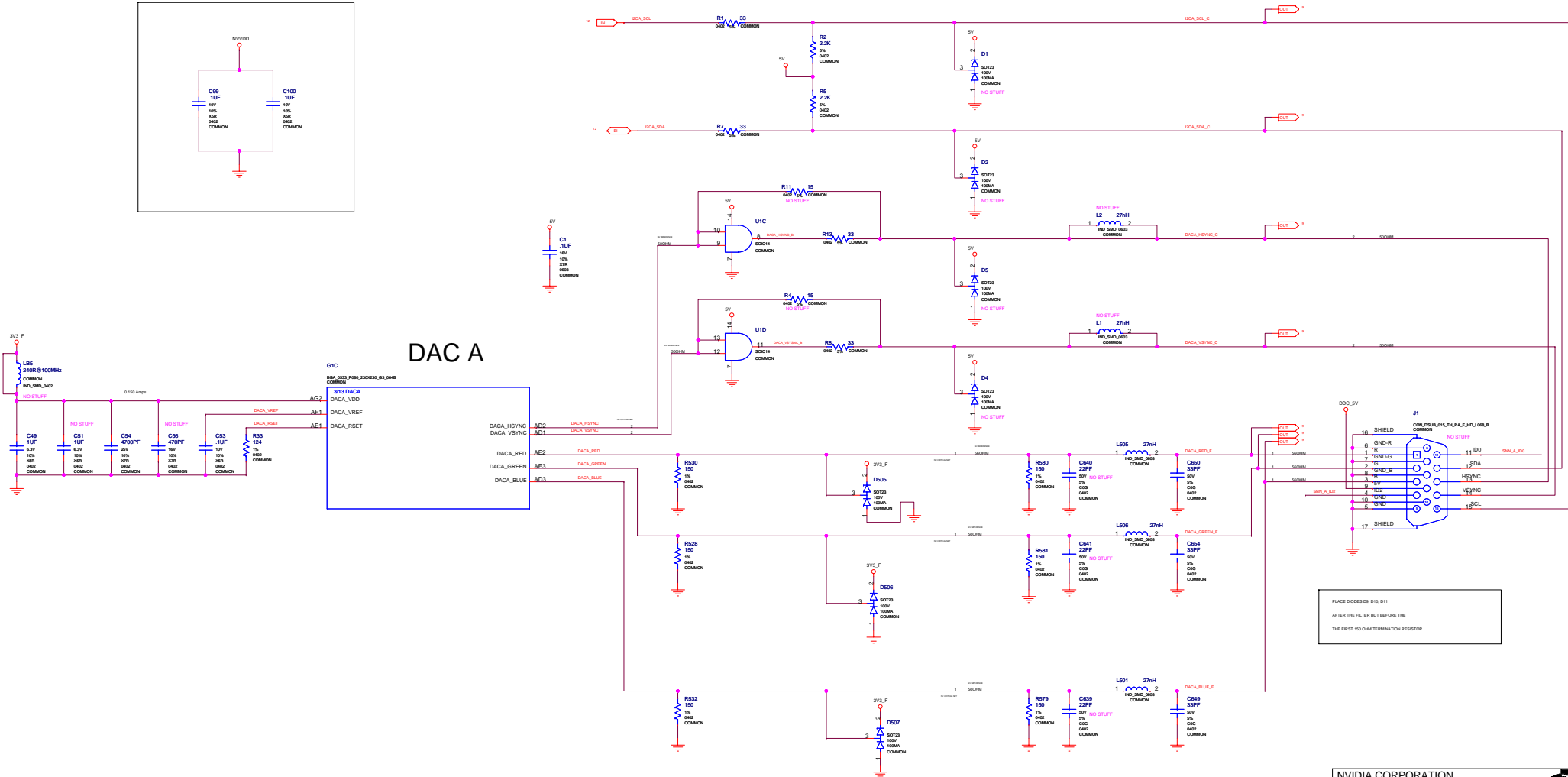
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DACA, Slim DB15 Connector



DAC A



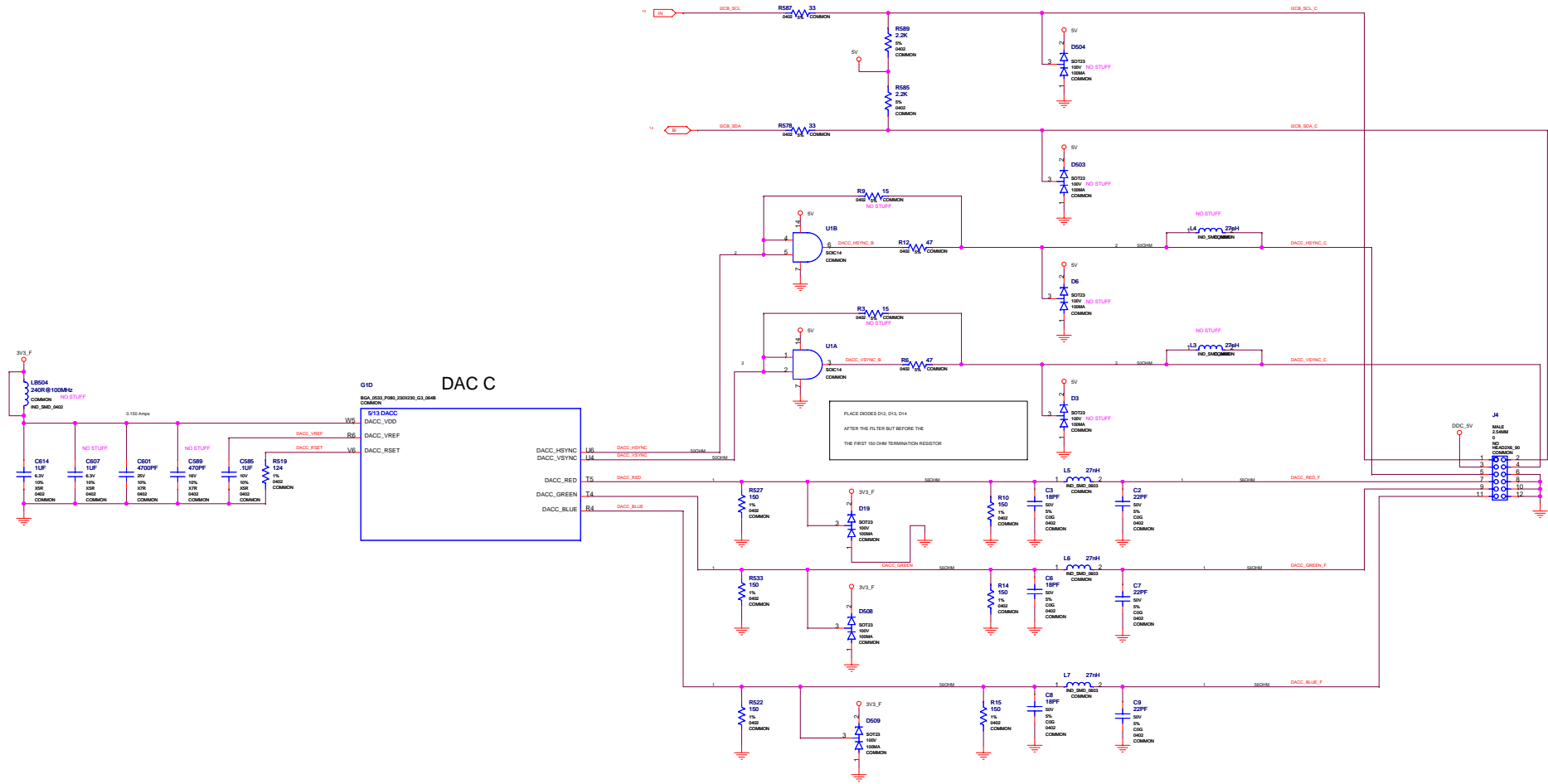
PLACE DIODES D6, D10, D11  
AFTER THE FILTER BUT BEFORE THE  
THE FIRST 150 OHM TERMINATION RESISTOR

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PAGE DETAIL	DACA, Slim DB15 Connector

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## DAC C,2x6 Header



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PAGE DETAIL	DACC.2x6 Header

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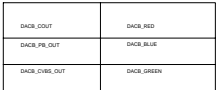


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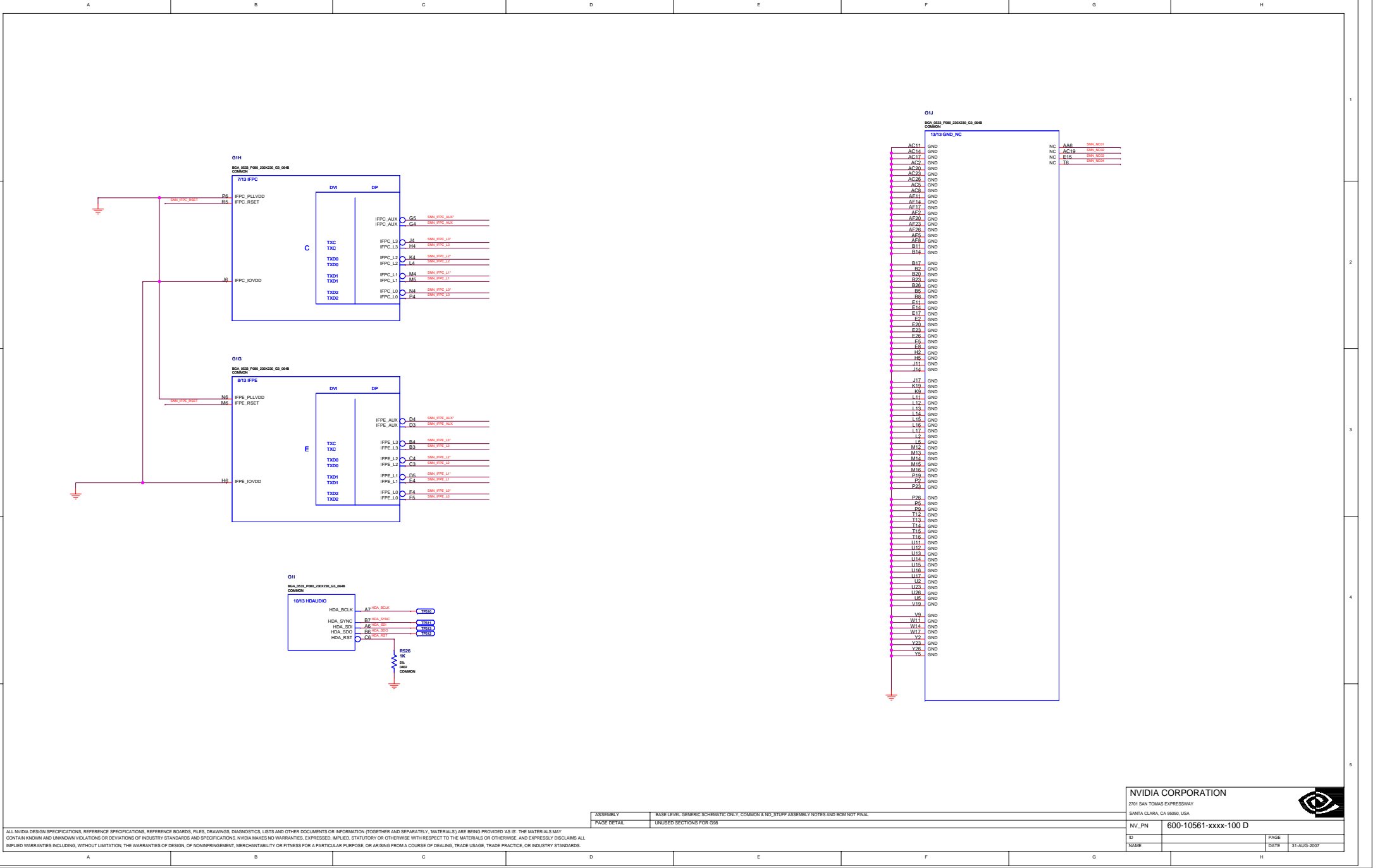


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	VIDEO CONNECTORS: MiniDIN

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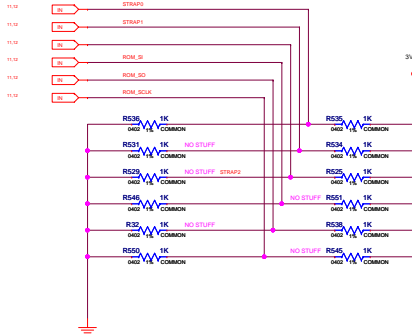




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## Straps, Mechanical Parts

## MULTI LEVEL STRAPS



Each strap pin represents a 4 bit value  
Pullup or Pulldown configures the MSB  
Resistor Value determines the 3 LSBs  
Resistor range is  $R \times n$   
where n is 0-9 and R is 5K ohm.

Resistor Value	Multilevel	Tied to VCC	Tied to Ground
3 Kohms	Y	0000	0000
6 Kohms	Y	0001	0001
12 Kohms	Y	0010	0010
24 Kohms	Y	0011	0011
48 Kohms	Y	1000	0100
96 Kohms	Y	1001	0101
192 Kohms	Y	1100	0110
284 Kohms	Y	1111	0111
2 Kohms*	N	xxxx	xxxx

## STRAPS

- ```

1. SUB VENDOR = 1 (ROM PRESENT)
   0 (NO ROM PRESENT)

2. DEVICE ID FOR GE1-64 = 0x6E2
   A) PCI_DEV_ID = 0x111C8 = 0x10
   B) PCI_DEV_ID = 0x111C8 = 0

3. XG0_PADOFF_LEN_ADDR_0 = 0x000

4. TUNED02_02 = 001

5. RAMCFG2_02 = 0000 10000 64 BIT ELPIA
   =0001 10000 64 BIT SAMVING, MACRON
   =0010 10000 64 BIT HYPERION
   =0011 10000 64 BIT HYPERION
   =0100 10000 64 BIT ELPIA
   =0101 10000 64 BIT SAMVING
   =0110 10000 64 BIT HYPERION
   =0111 10000 64 BIT HYPERION

6. USER02_02 = 0000

```

| MULTILEVEL MODE                                                    |                                                                   |
|--------------------------------------------------------------------|-------------------------------------------------------------------|
| STRAP_CAR_PUL_QMS0 (RS10) = 40K<br>STRAP_CAR_PUL_QMS1 (RS11) = 40K |                                                                   |
| SIGNAL                                                             | FUNCTION                                                          |
| STRAP[0]                                                           | USER[0]                                                           |
| STRAP[1]                                                           | SGO_PADOFG_LUT_ADR[0]                                             |
| STRAP[2]                                                           | SGO_DEV[0]                                                        |
| ROM_CAR                                                            | SLOT_DEV[0], EXT_SLAVE_VENDOR, SLOT_CAR_CQX, PEX_PUL_EN_TERMIN[0] |
| ROM_SI                                                             | RANKCFG[0]                                                        |
| ROM_SO                                                             | COLX[277], TWMODEP[0]                                             |

| BRINGUP BINARY MODE |                          | STRAP_CAL_PU1_GND0 (R512) = NO STUFF<br>STRAP_CAL_PU1_GND1 (R511) = NO STUFF |
|---------------------|--------------------------|------------------------------------------------------------------------------|
| SIGNAL              | FUNCTION                 |                                                                              |
| STRAP[0]            | SG10, PADCFG, IUT_ADR[0] |                                                                              |
| STRAP[1]            | SG10, PADCFG, IUT_ADR[1] |                                                                              |
| STRAP[2]            | SG10, PADCFG, IUT_ADR[2] |                                                                              |
| ROM, SOLK           | SG10, PADCFG, IUT_ADR[3] |                                                                              |
| ROM, SI             | SUB_VENDOR               |                                                                              |
| ROM, SO             | XCLK_27T                 |                                                                              |

| PRODUCTION BINARY MODE |              |
|------------------------|--------------|
| SIGNAL                 | FUNCTION     |
| STRAP[0]               | RAMCFG[0]    |
| STRAP[1]               | RAMCFG[1]    |
| STRAP[2]               | RAMCFG[2]    |
| ROM_SEL0               | PG2_SEL[0:0] |
| ROM_S1                 | PG2_SEL[0:1] |
| ROM_S0                 | PG2_SEL[0:2] |

## STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz ( MULTI LEVEL) R511= 40K, R512=40K

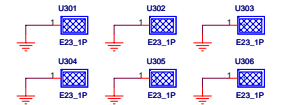
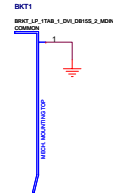
| 303_F | QMD     | FUNCTIONAL | FUNCTION                                           |
|-------|---------|------------|----------------------------------------------------|
| 25K   | 5K      | STRAP0     | USER0-0                                            |
|       | 5K      | STRAP1     | GPIO_FUNC0_L1UT_ADDR0-0                            |
|       | 25K     | STRAP2     | PCI_FUNC0-0                                        |
|       | ROM_32K | ROM_32K    | PCI_DEVICE_EXT_BUS_VENDOR_SLOT_CFG_PEX_P1_P3_TERM0 |
|       | 45K     | ROM_3D     | RANKCFG0-0                                         |
|       |         |            | CLKA_27_TMODE0-0                                   |

## STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz ( BRINGUP BINARY) R511= NO STUFF, R512=NO STUFF

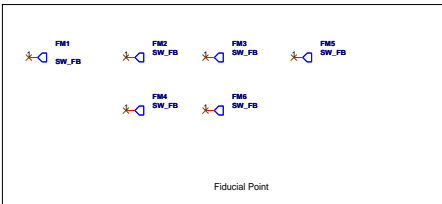
| 303_F | QMD | PARAM1 | FUNCTION            |
|-------|-----|--------|---------------------|
|       | SK  | STRAP1 | 3011_FADDS_LUT_ADR1 |
|       | SK  | STRAP1 | 3011_FADDS_LUT_ADR1 |
|       | SK  | STRAP2 | 3011_FADDS_LUT_ADR2 |
| SK    | SK  | ROM_SC | 3011_FADDS_LUT_ADR2 |
|       |     | ROM_SI | SUB_VENDOR          |
| SK    |     | ROM_SO | NCLA_277            |

## STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz ( PRODUCTION BINARY) R511= 40K, R512= NO STUFF

| 315_F | GND | (PINSIGNAL) | FUNCTION       |
|-------|-----|-------------|----------------|
| SK    |     | STRAP[3]    | RANCPQ[3]      |
| SK    |     | STRAP[1]    | RANCPQ[1]      |
| SK    |     | STRAP[2]    | RANCPQ[2]      |
| SK    | SK  | RGM_SCL     | PCI_DEVICE     |
| SK    | SK  | RGM_SS      | PCI_DEVICE_EXT |
| SK    |     | RGM_SD      | NCLA_277       |



FOR EMI



Fiducial Point

NVIDIA CORPORATION

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SANTA CLARA, CA 95050, USA



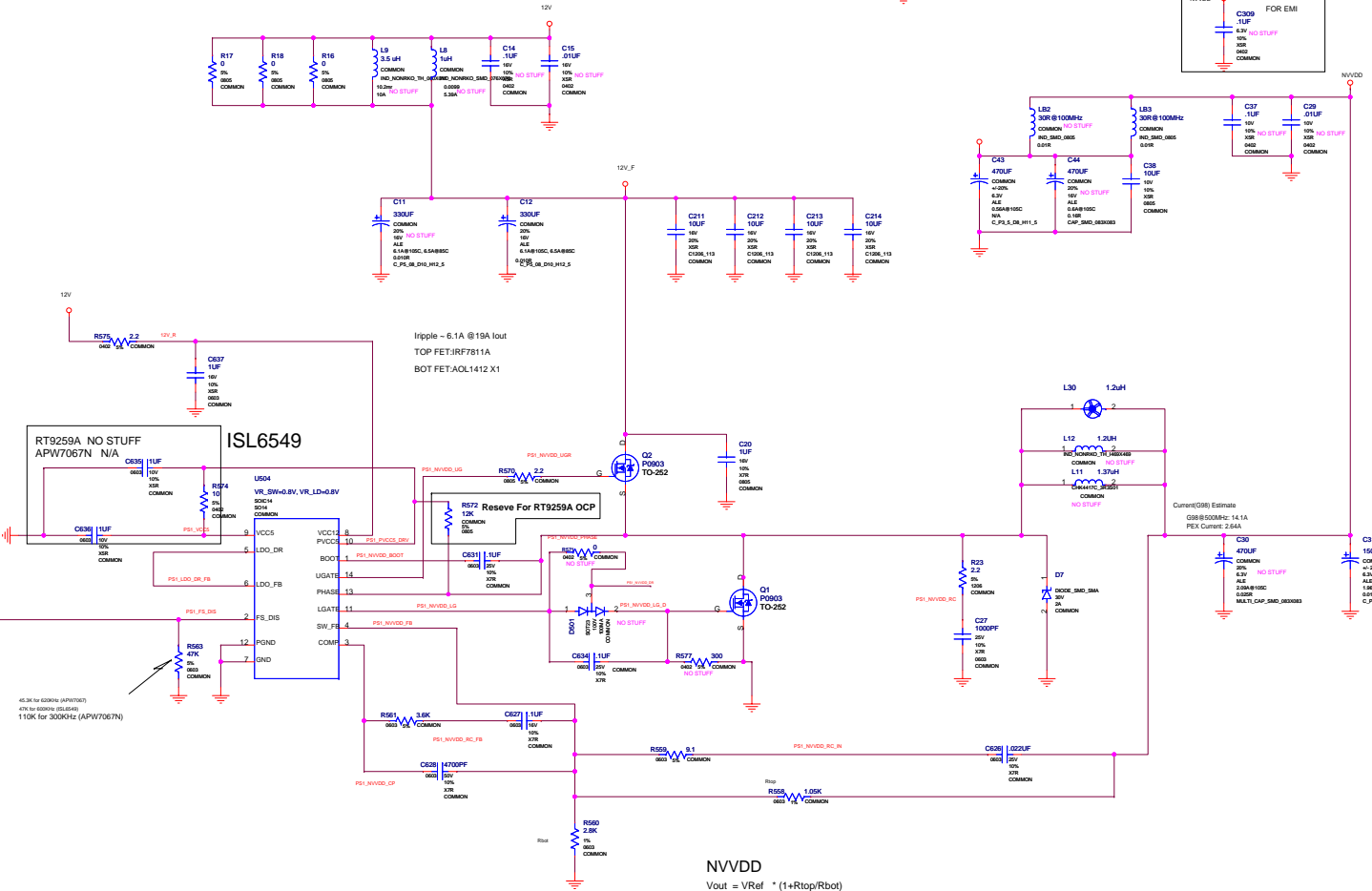
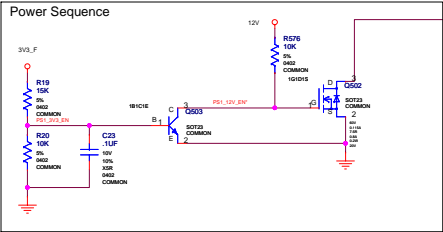
|       |                      |
|-------|----------------------|
| NV_PN | 600-10561-xxxx-100 D |
|-------|----------------------|

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|------|--|------|-------------|
| ID   |  | PAGE |             |
| NAME |  | DATE | 31-AUG-2007 |

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Power Supply I: NVVDD, PLLVDD



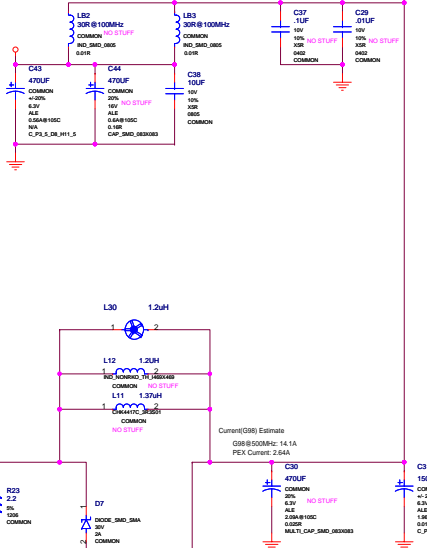
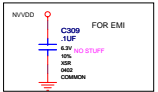
NVVDD

$V_{out} = V_{ref} \cdot \left(1 + \frac{R_{top}}{R_{bot}}\right)$

$1.1V = 0.8V \cdot \left(1 + \frac{1.05k\Omega}{2.8k\Omega}\right)$  (ISL6549)

$1.15V = 0.8V \cdot \left(1 + \frac{1.02k\Omega}{2.32k\Omega}\right)$  (ISL6549)

| Net Name | LINE_WIDTH | Current | Voltage |
|----------|------------|---------|---------|
| 12V_F    | 360MIL     | 3A      | 12V     |
| NVVDD    | 360MIL     | 16.74A  | 1.1V    |
| PLL      | 360MIL     | 2.64A   | 1.1V    |
| 12V      | 360MIL     | 6A      | 12V     |
| DND      | 360MIL     |         | 0V      |



|             |                                                                                       |
|-------------|---------------------------------------------------------------------------------------|
| ASSEMBLY    | BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL |
| PAGE DETAIL | Power Supply I: NVVDD, PLLVDD                                                         |

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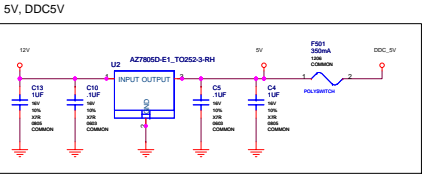
SANTA CLARA, CA 95050, USA

NV\_PN 600-10561-xxxx-100 D

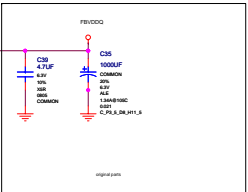
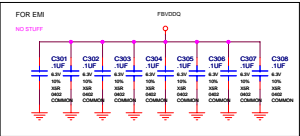
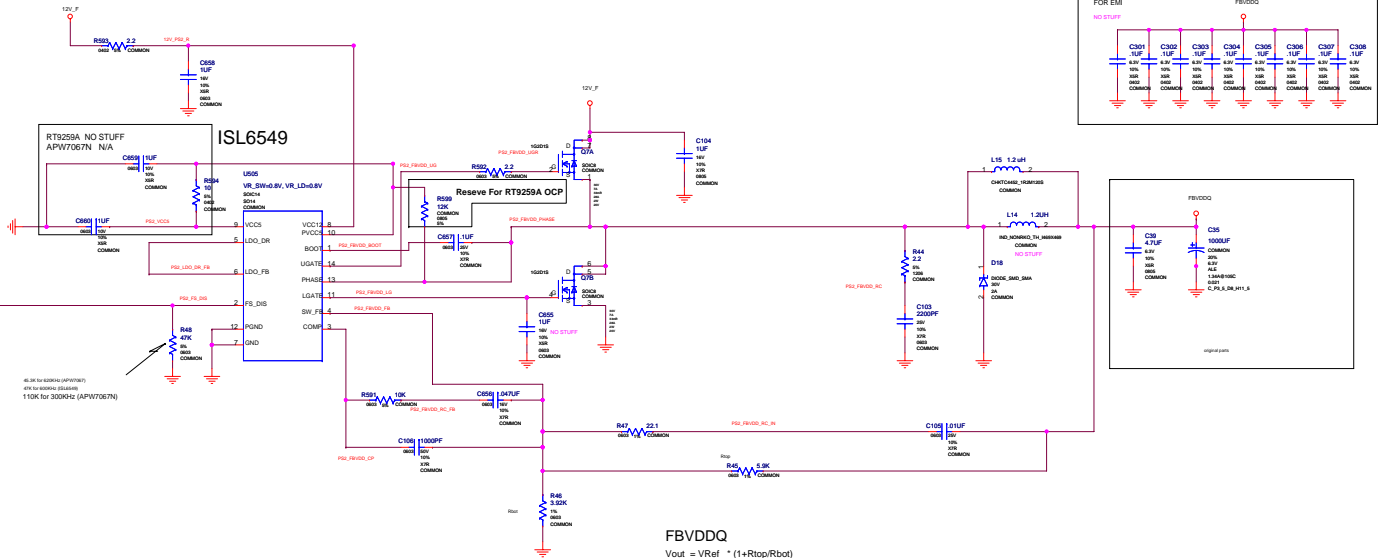
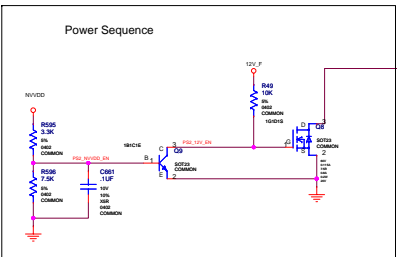
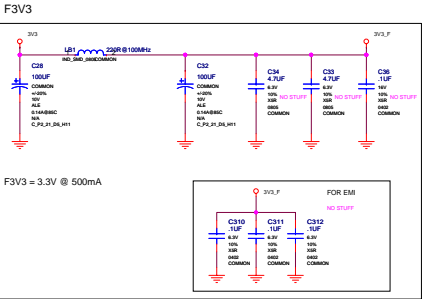
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| ID   | PAGE             |
| NAME | DATE 31-AUG-2007 |

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Power Supply II: 5V, DDC5V, F3V3, FBVDDQ



| Net Name | MIN_LINE_WIDTH | CURRENT | VOLTAGE |
|----------|----------------|---------|---------|
| 5V       | 1.2MM          | 0.2A    | 5V      |
| DDC5V    | 1.2MM          | 0.2A    | 5V      |
| F3V3     | 1.2MM          | 1A      | 3.3V    |
| FBVDDQ   | 1.2MM          | 1A      | 1.8V    |




FBVDDQ

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

1.800V = 0.8V \* (1 + (5.9K/4.7K)) (ISL6549)

2.000V = 0.8V \* (1 + (5.9K/3.92K)) (ISL6549)

2.156V = 0.8V \* (1 + (5.9K/3.4K)) (ISL6549)

|                                                                                      |  |                             |                                                                                       |             |
|--------------------------------------------------------------------------------------|--|-----------------------------|---------------------------------------------------------------------------------------|-------------|
| <b>NVIDIA CORPORATION</b><br>2701 SAN TOMAS EXPRESSWAY<br>SANTA CLARA, CA 95050, USA |  |                             |  |             |
| <b>NV_PN</b>                                                                         |  | <b>600-10561-xxxx-100 D</b> |                                                                                       |             |
| <b>ID</b>                                                                            |  | <b>PAGE</b>                 |                                                                                       |             |
| <b>NAME</b>                                                                          |  | <b>DATE</b>                 |                                                                                       | 31-AUG-2007 |

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<div>C278 [8.44]</div> <div>C279 [8.37]</div> <div>C280 [8.40]</div> <div>C281 [8.56]</div> <div>C282 [8.56]</div> <div>C283 [8.40]</div> </div> |  | <div> <div>D511 [8.50]</div> <div>D512 [8.40]</div> <div>D501 [14.18]</div> <div>G1 [2.37]</div> <div>G1 [3.30]</div> <div>G1 [8.40]</div> <div>G1 [7.40]</div> <div>G1 [8.30]</div> <div>G1 [10.40 10.38]</div> <div>D504 [2.24]</div> <div>G1 [12.40 12.20]</div> <div>D505 [12.30]</div> <div>J1 [8.46]</div> <div>D502 [13.40]</div> <div>J3 [8.39]</div> <div>J4 [7.30]</div> <div>J5 [12.20]</div> <div>D503 [13.24]</div> <div>D501 [12.28]</div> <div>L1 [8.37]</div> <div>D502 [12.20]</div> <div>D501 [12.20]</div> <div>L2 [8.37]</div> <div>D501 [12.20]</div> <div>L4 [7.37]</div> <div>D502 [8.28]</div> <div>L5 [7.47]</div> <div>D502 [12.20]</div> <div>D501 [12.20]</div> <div>D501 [12.20]</div> <div>D501 [12.20]</div> <div>D501 [12.20]</div> <div>D501 [12.20]</div> <div>D501 [12.20]</div> <div>D501 [12.20]</div> <div>D501 [12.20]</div> <div>D501 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