

## (1) PCI-E INTERFACE

D

D

C

C

B

B

A

A

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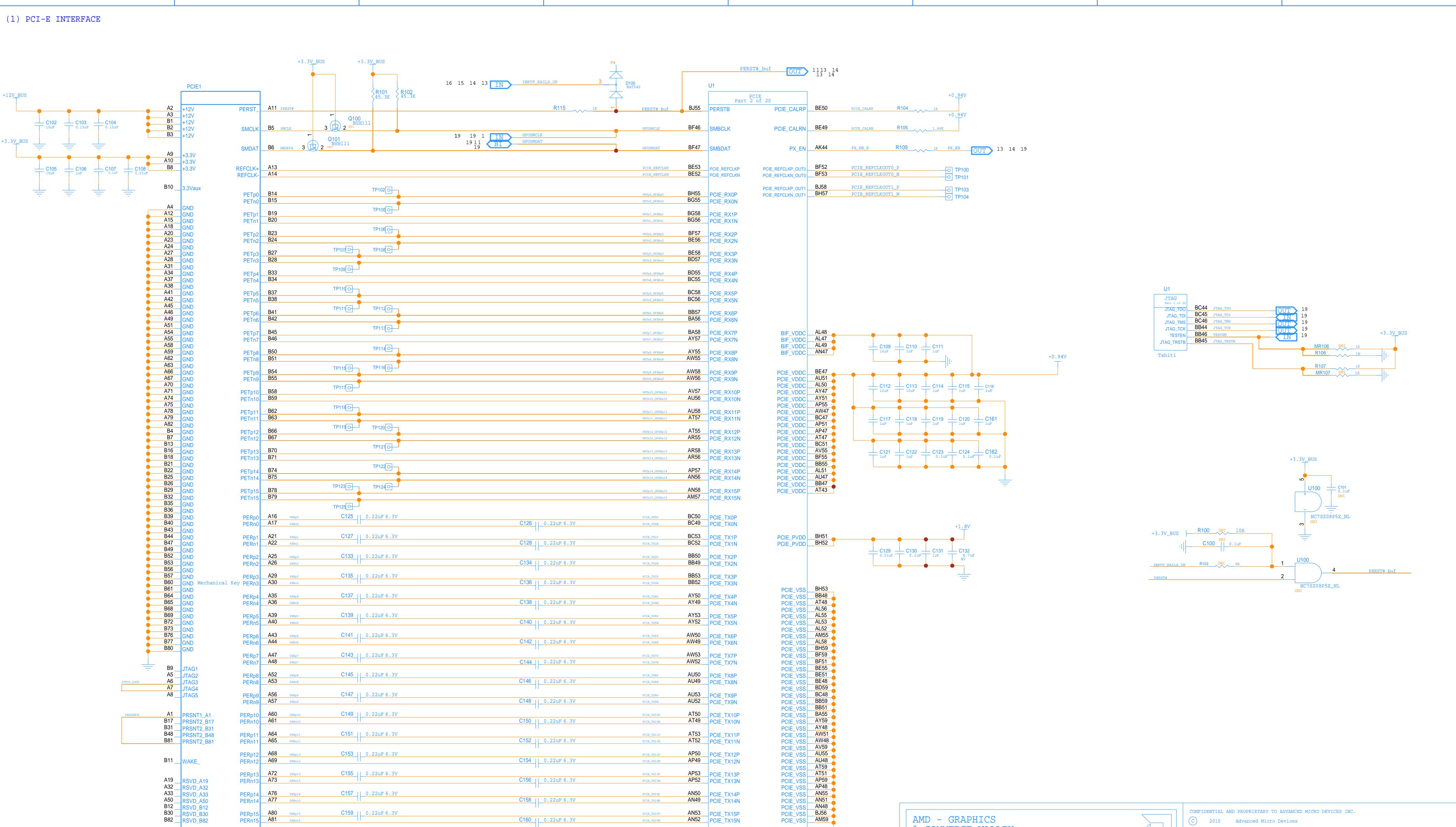
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SHEET: TAHITI\_PCIE

DATE: Wed Nov 02 15:28:37 2011 | REV: 1.0

SHEET NUMBER: 1 OF 21

DOCUMENT NUMBER: 105-C38600-00

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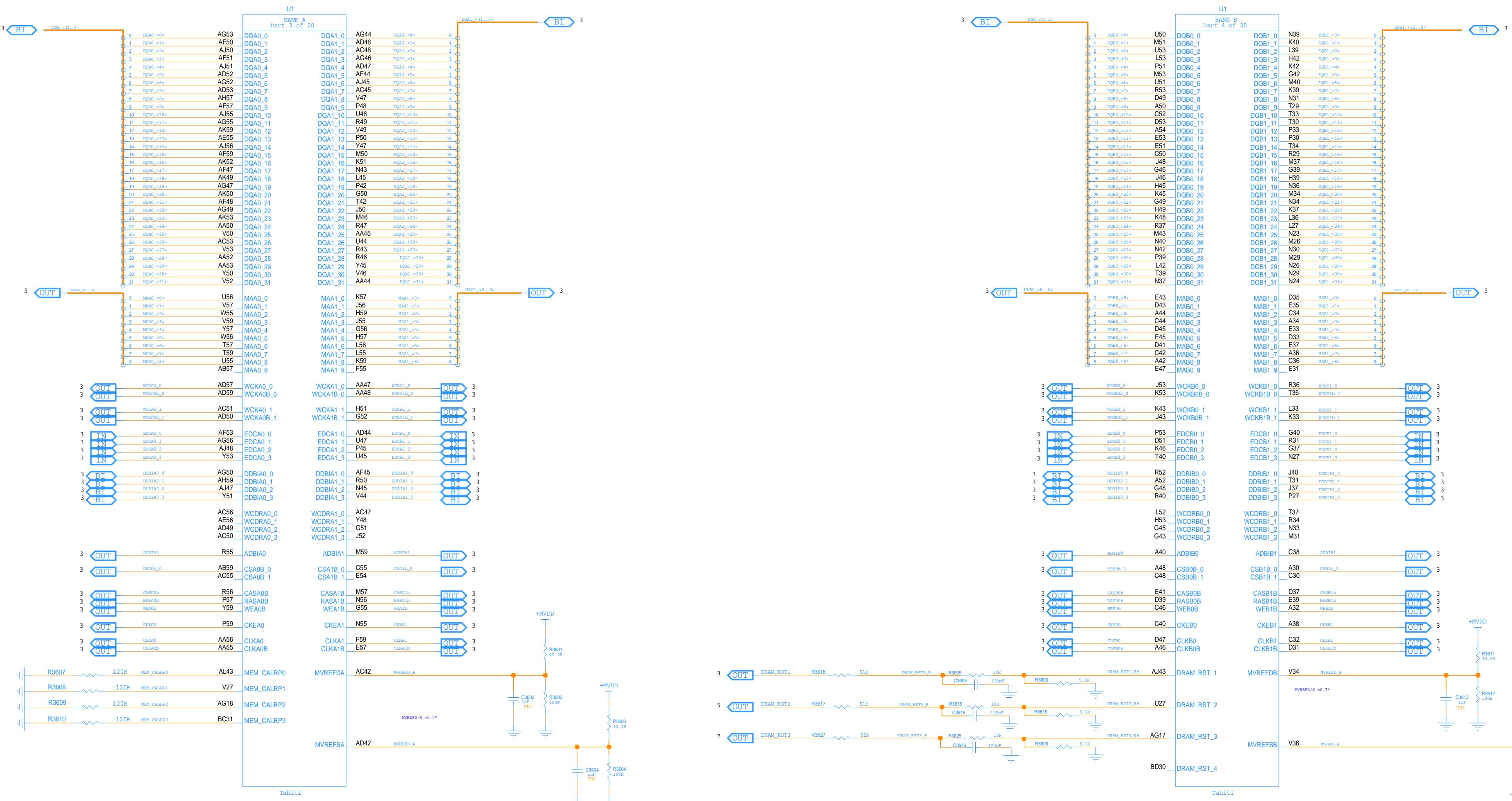
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## (2) TAHITI Memory Channel A&amp;B



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SHEET: TAHITI MEM AB

DATE: Wed Nov 02 15:28:40 2011

REV: 1.0

SHEET NUMBER: 2 OF 21

DOCUMENT NUMBER: 105-C38600-00

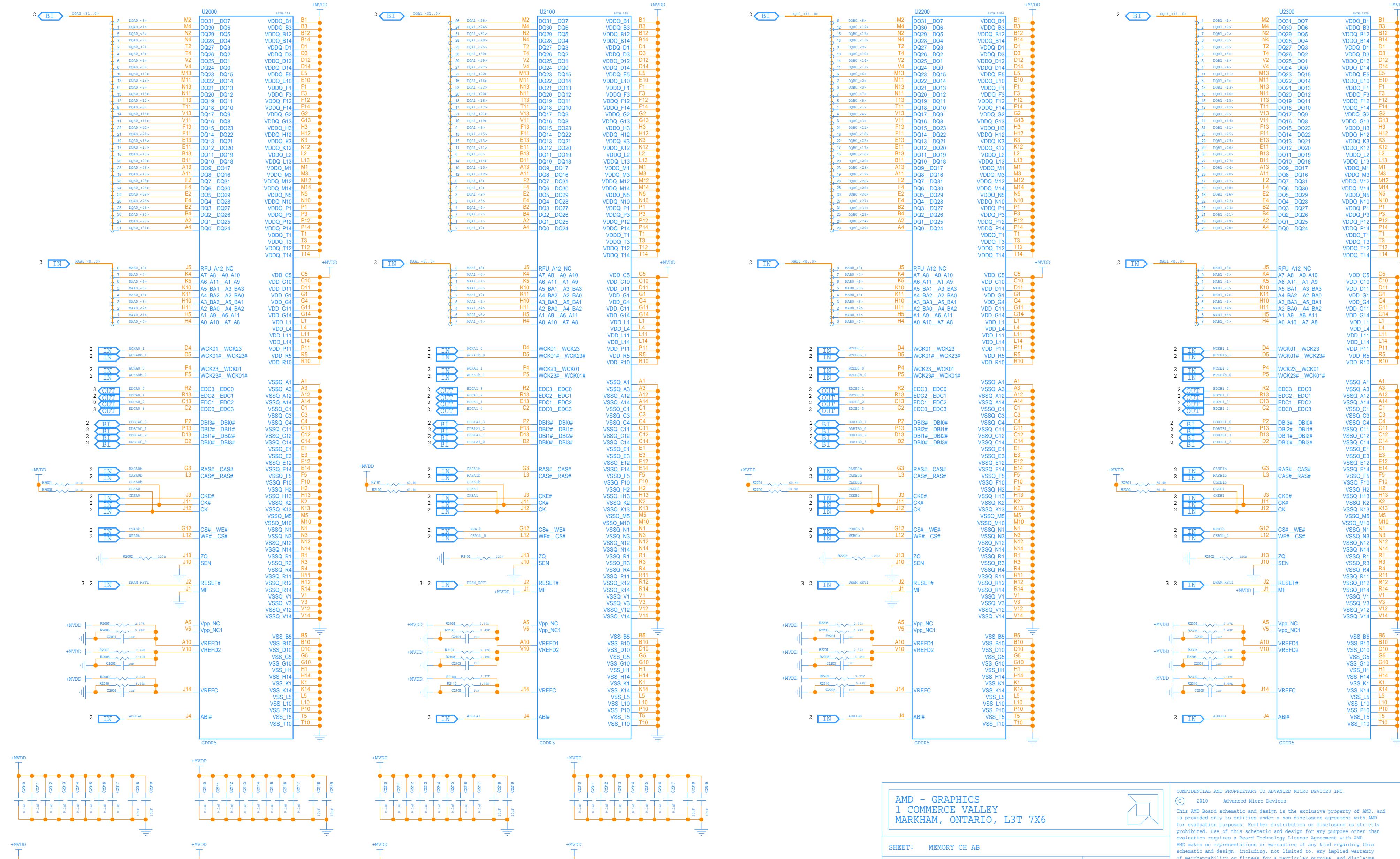
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## (3) GDDR5 Memory Channel A&amp;B



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SHEET: MEMORY CH AB

DATE: Wed Nov 02 15:28:39 2011 REV: 1.0

SHEET NUMBER: 3 OF 21

DOCUMENT NUMBER: 105-C38600-00

NOTES: NOTE

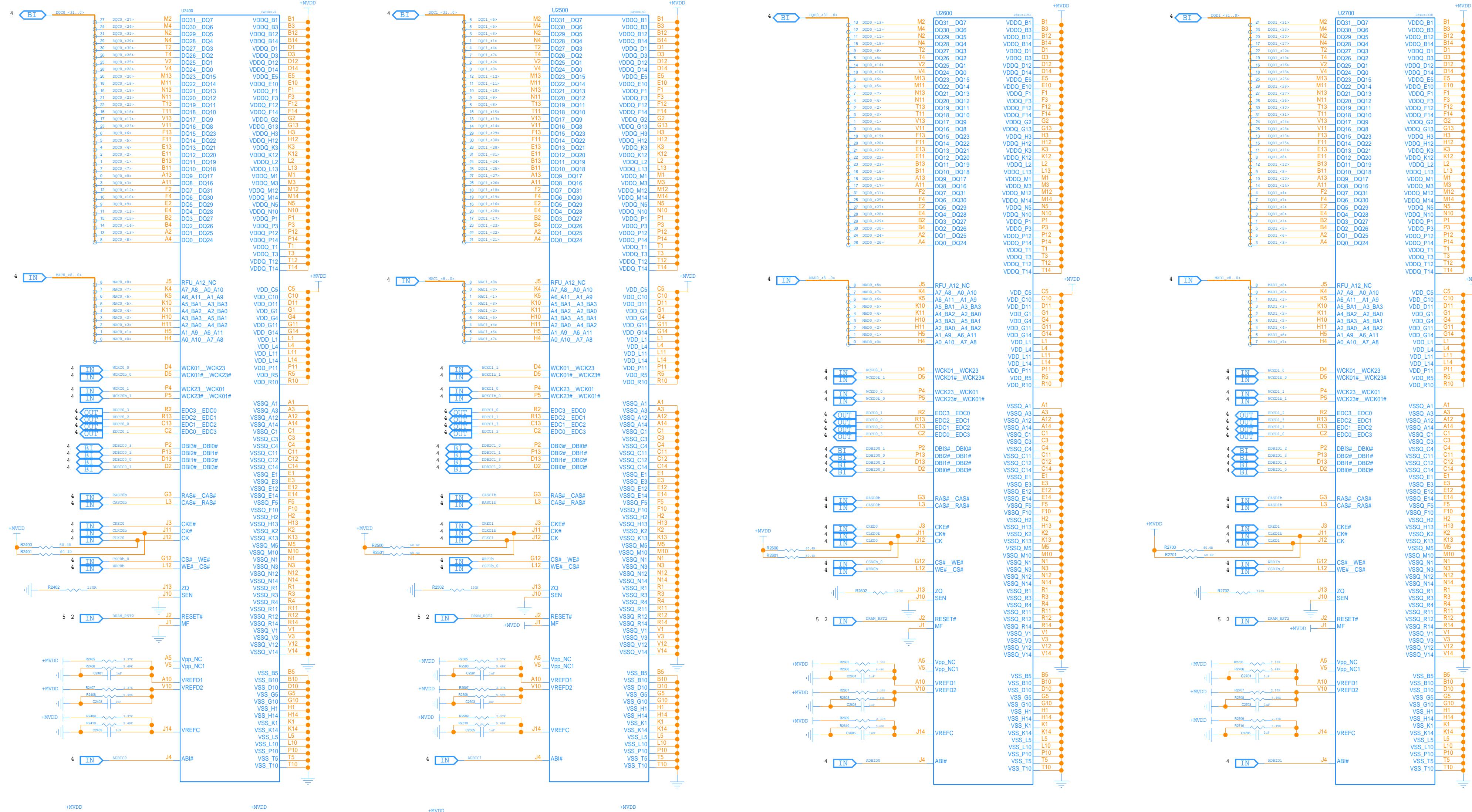
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## (5) GDDR5 Memory Channel C&amp;D



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SHEET: MEMORY CH CD

DATE: Thu Nov 03 14:06:56 2011 REV: 1.0

SHEET NUMBER: 5 OF 21

DOCUMENT NUMBER: 105-C38600-00

NOTES: NOTE

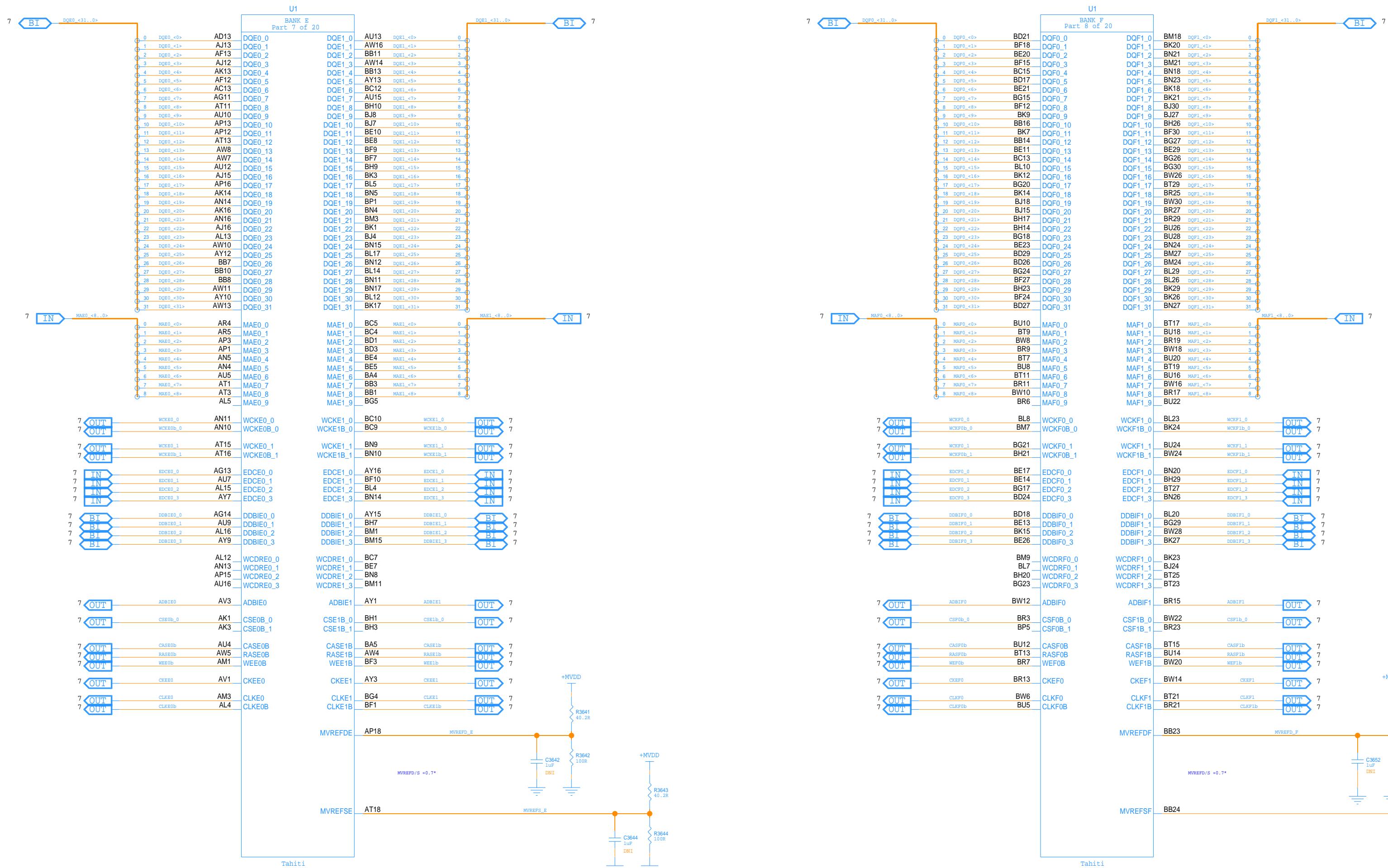
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## (6) TAHITI Memory Channel E&amp;F



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SHEET: TAHITI\_MEM\_EF

DATE: Wed Nov 02 15:28:40 2011 REV: 1.0

SHEET NUMBER: 6 OF 21

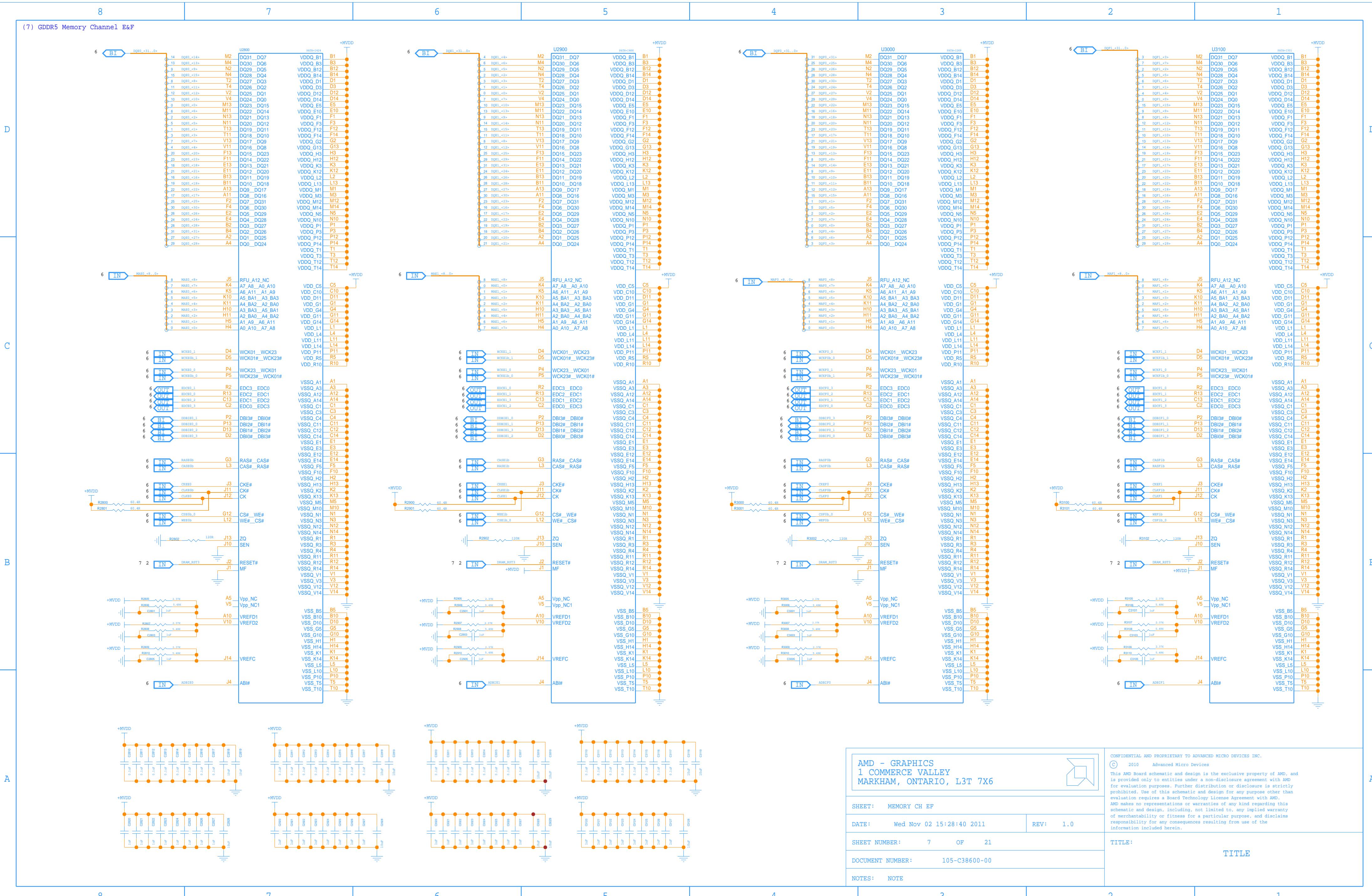
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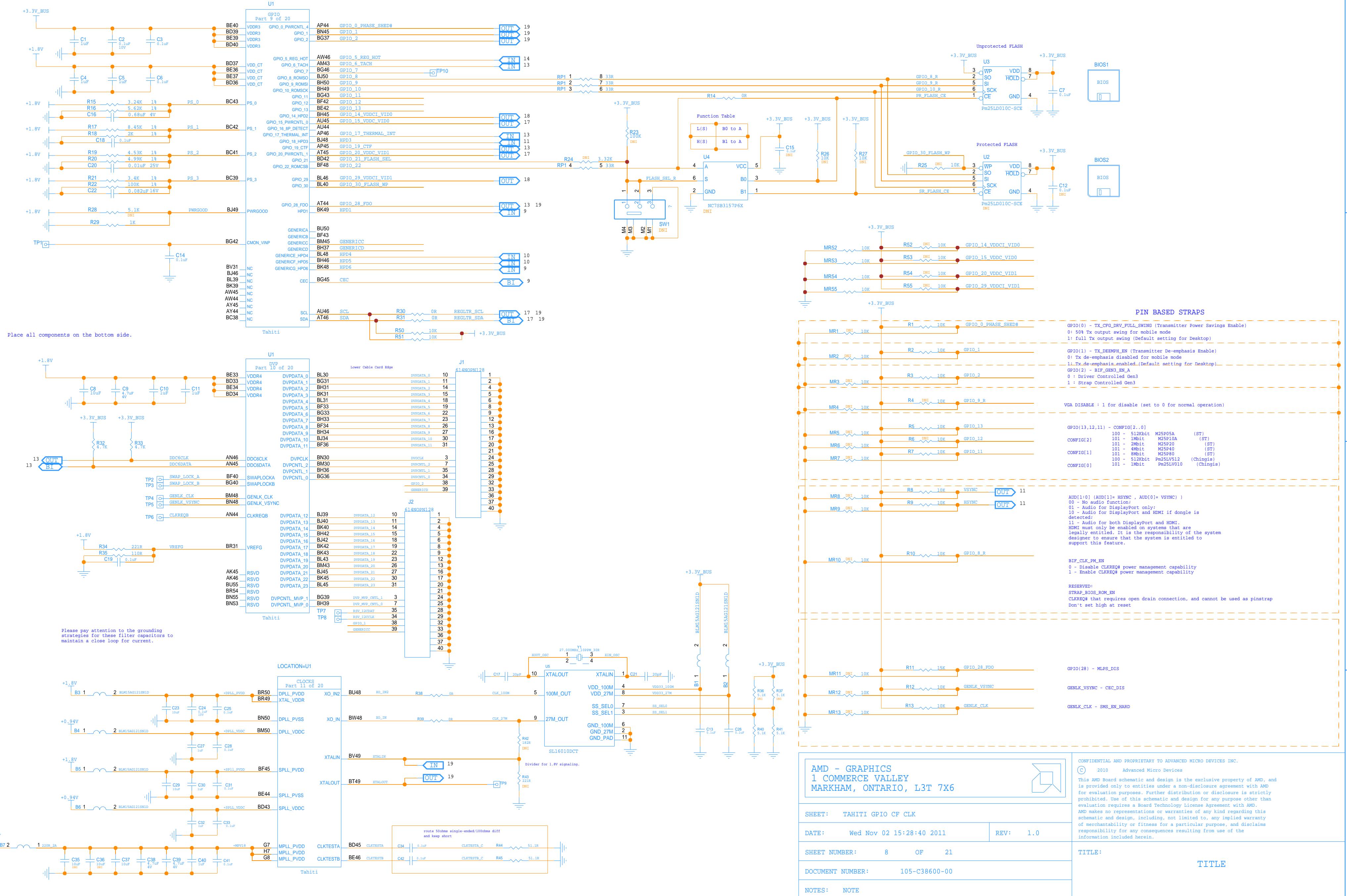
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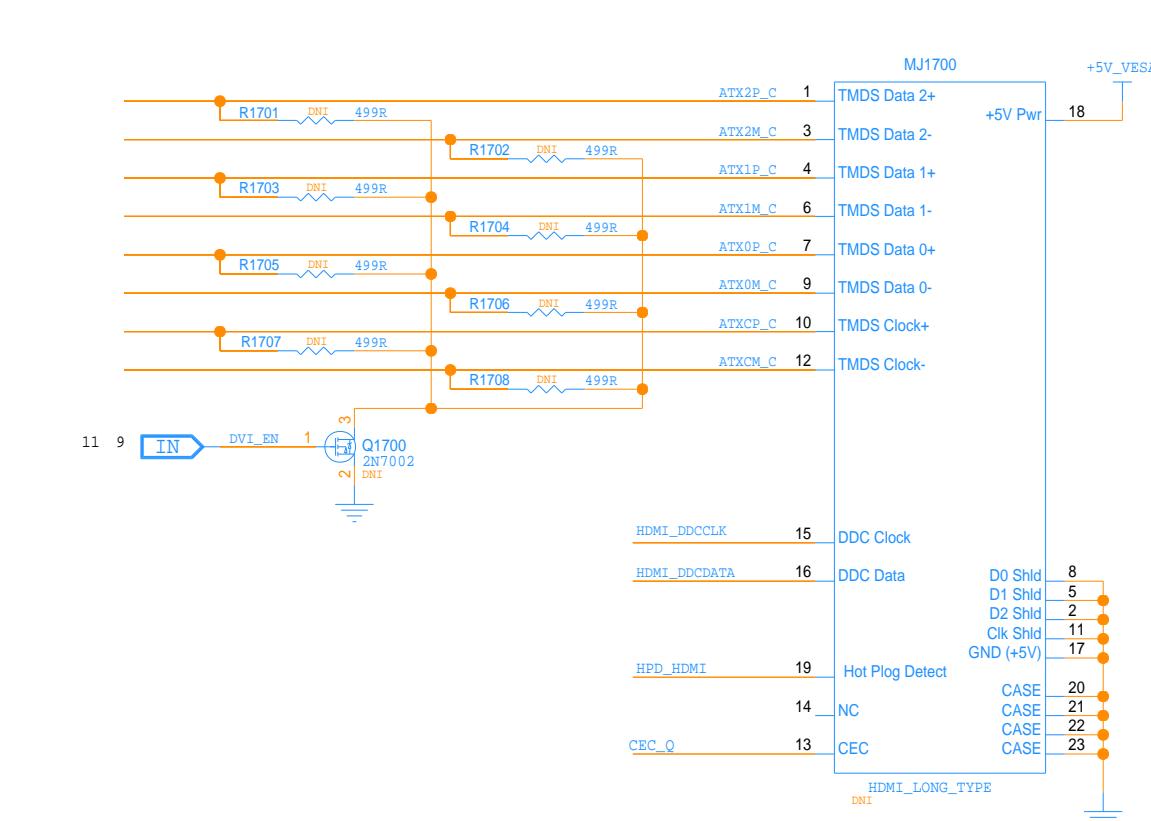
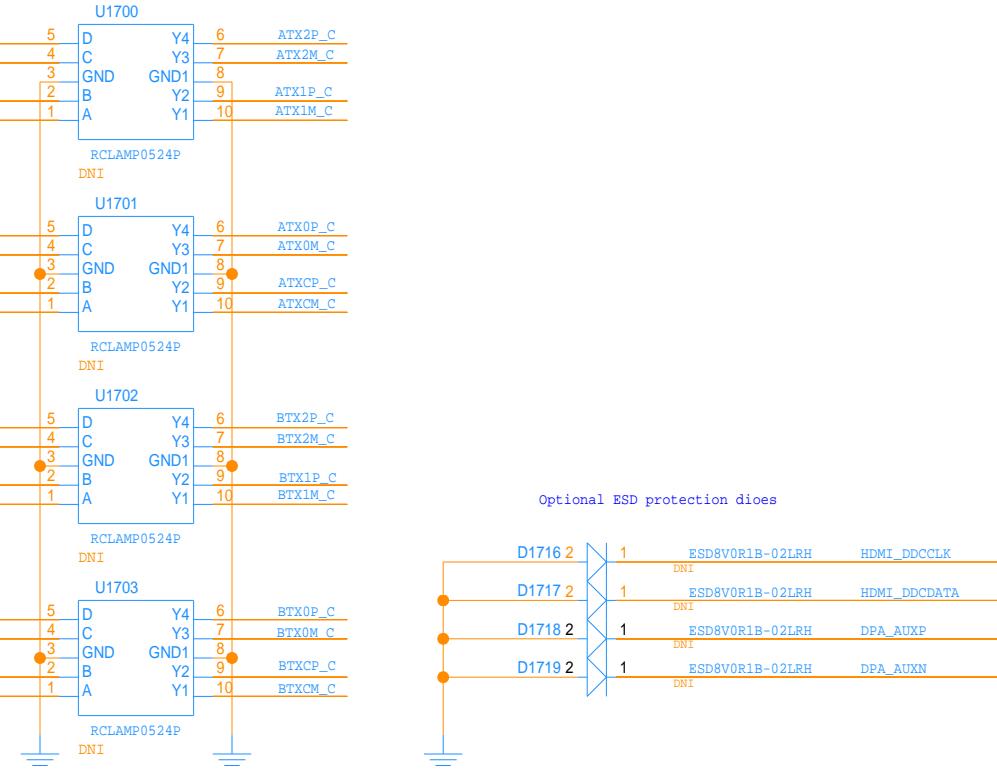
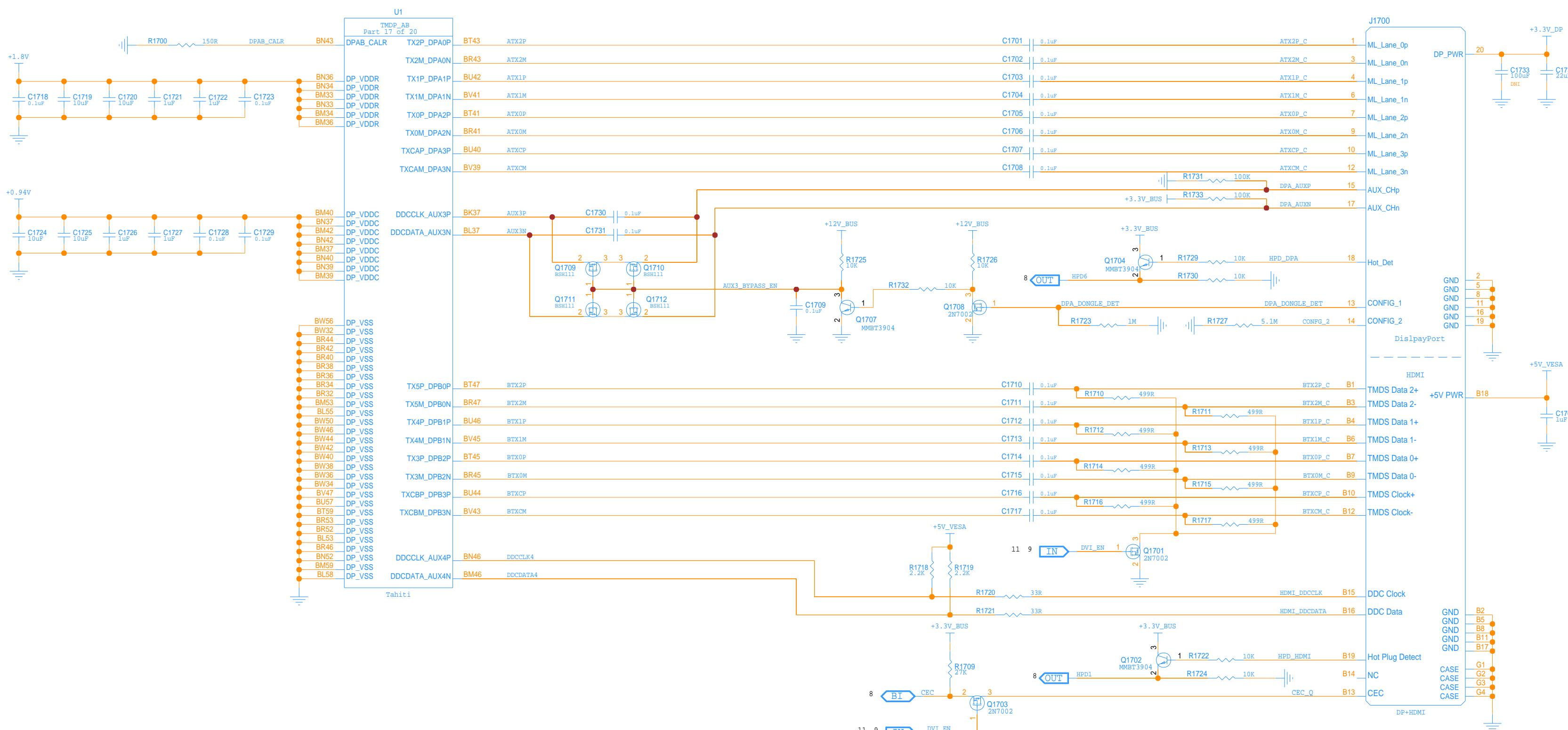
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## (8) TAHITI GPIO/CF/CLKS



## (9) TAHITI HDMI DVI AB



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SHEET: TAHITI HDMI DP AB

DATE: Wed Nov 02 15:28:39 2011 REV: 1.0

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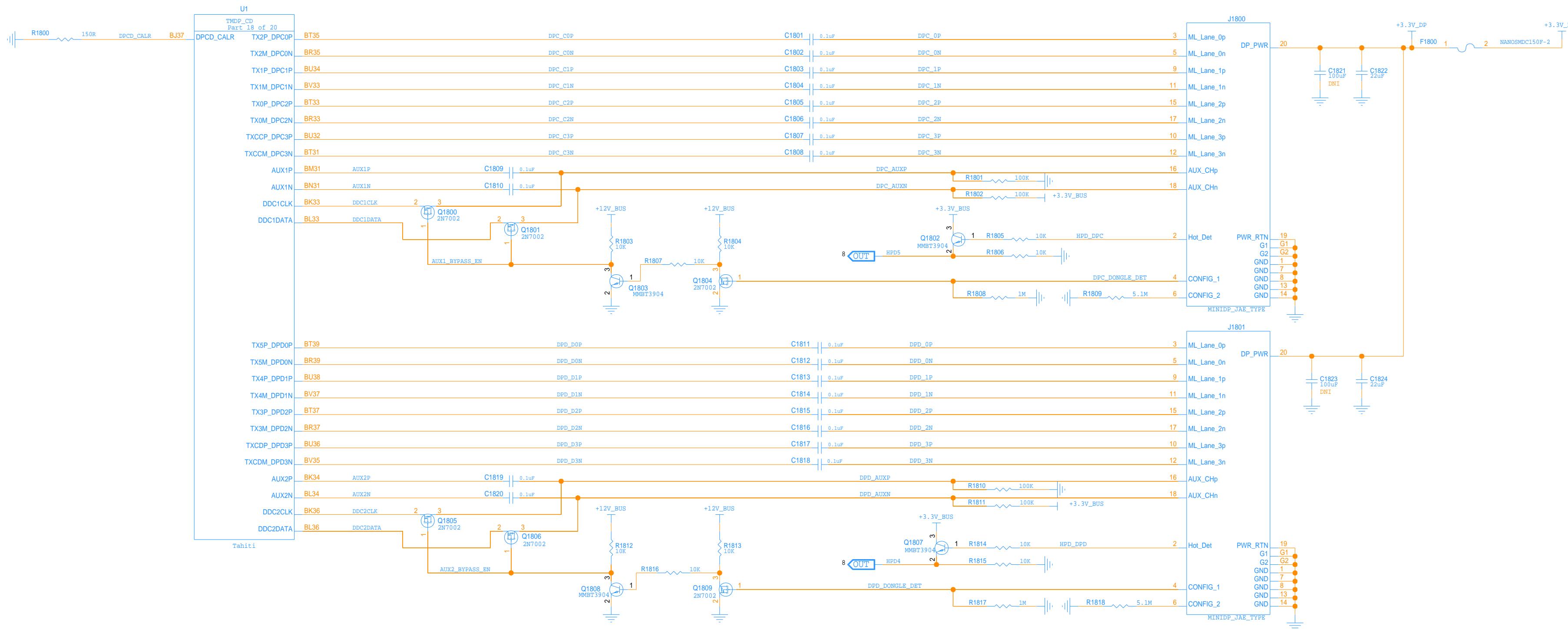
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NOTES: NOTE

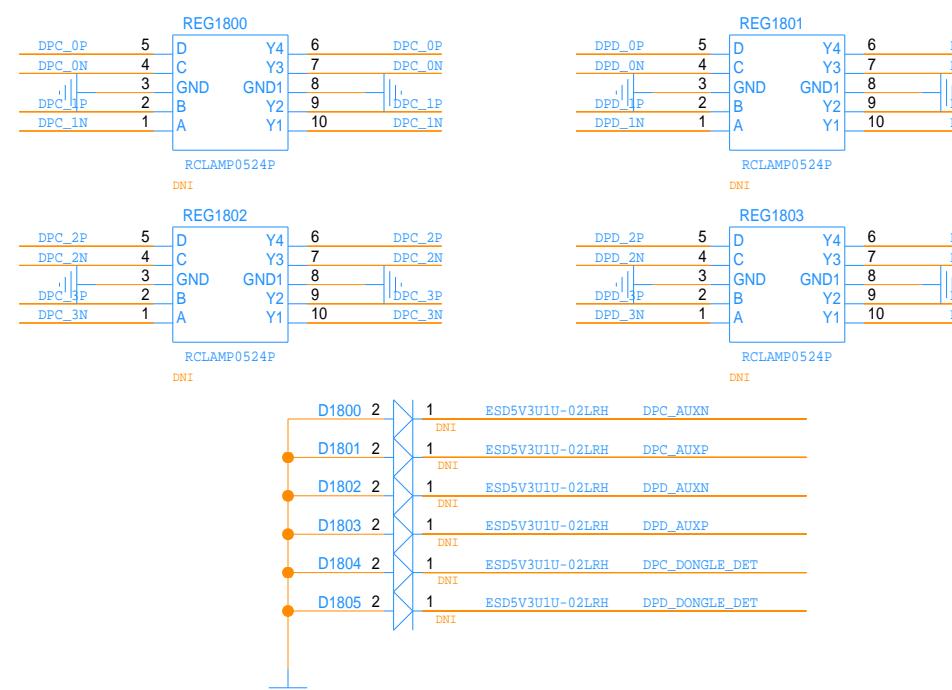
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(10) TAHITI mDP mDP CD



## OPTIONAL ESD PROTECTION DIODES



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SHEET: TAHITI mDP mDP CD

DATE: Wed Nov 02 15:28:39 2011 REV: 1.0

SHEET NUMBER: 10 OF 21

DOCUMENT NUMBER: 105-C38600-00

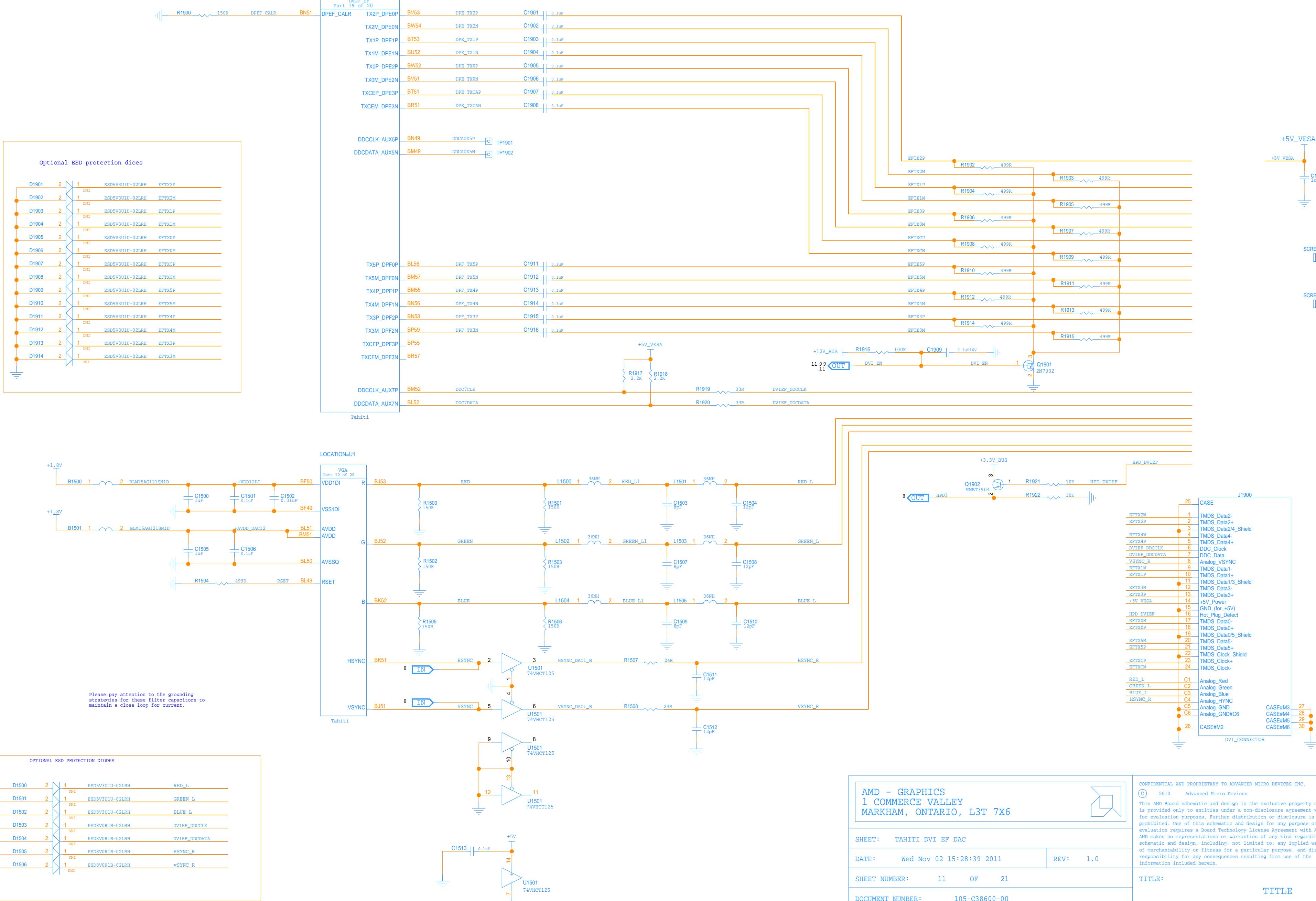
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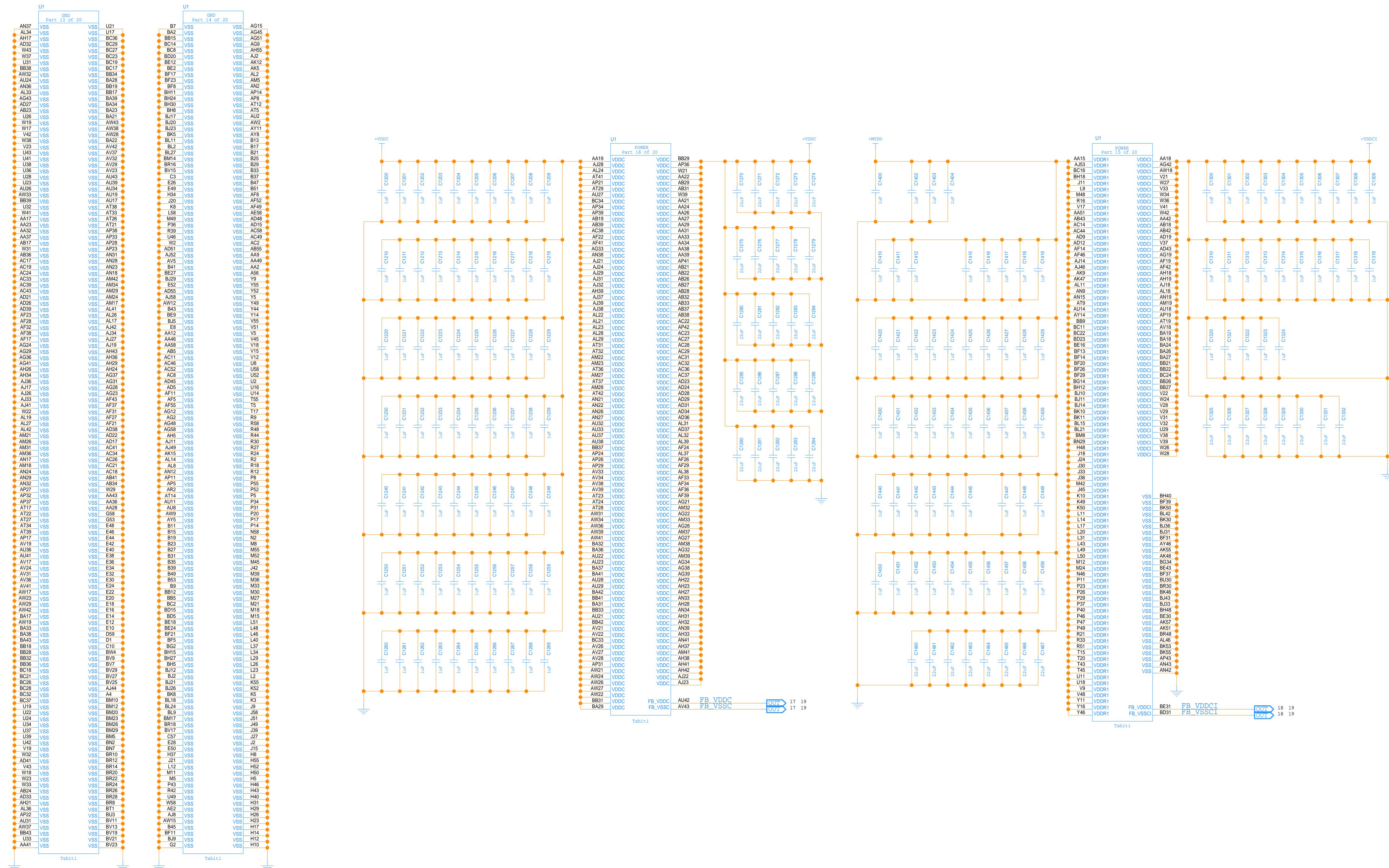
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## (11) TAHITI DVI EF DAC



(12) TAHITI POWER



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SHEET: TAHITI POWER

DATE: Wed Nov 02 15:28:41 2011 REV: 1.0

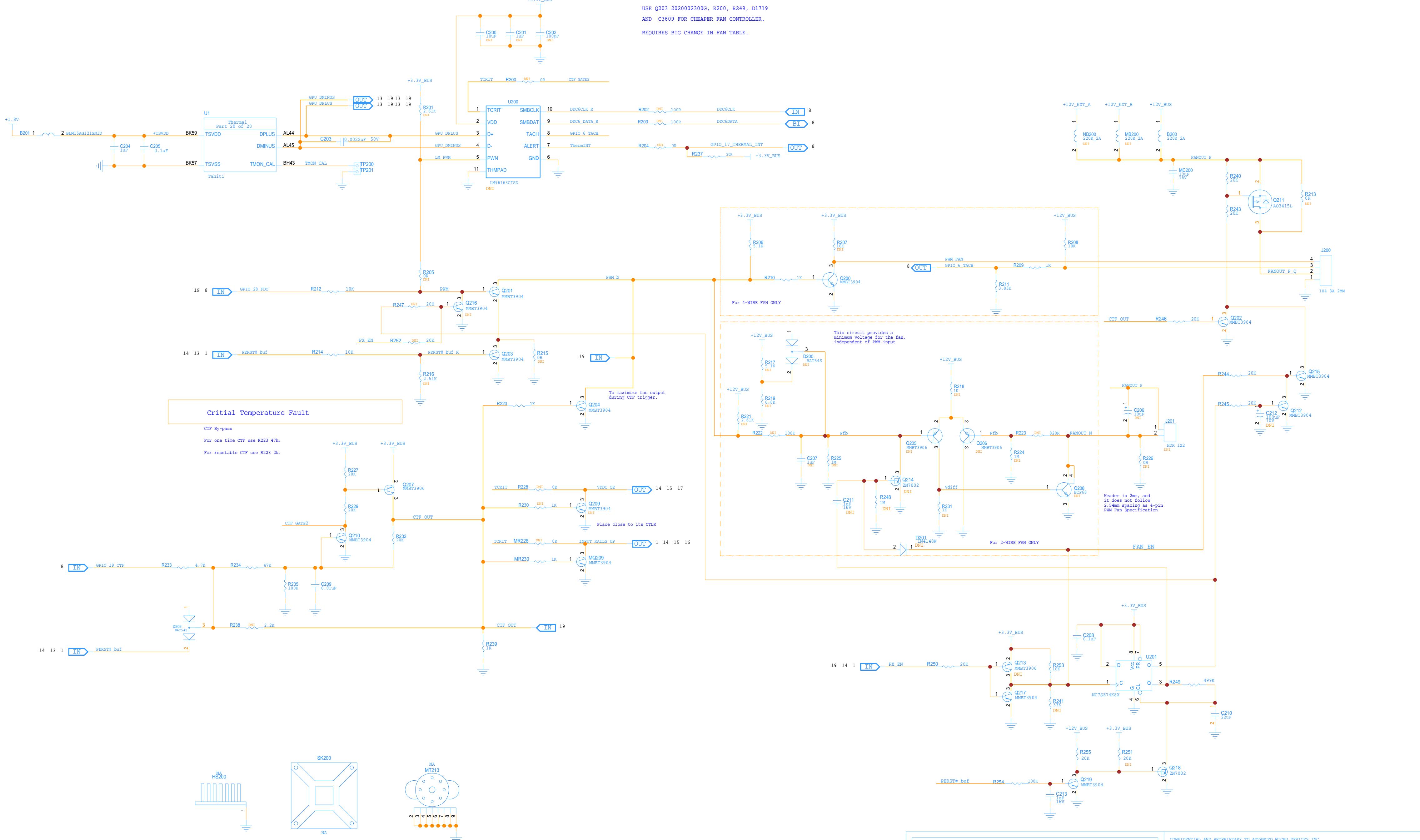
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(13) TAHITI THERMAL MECH



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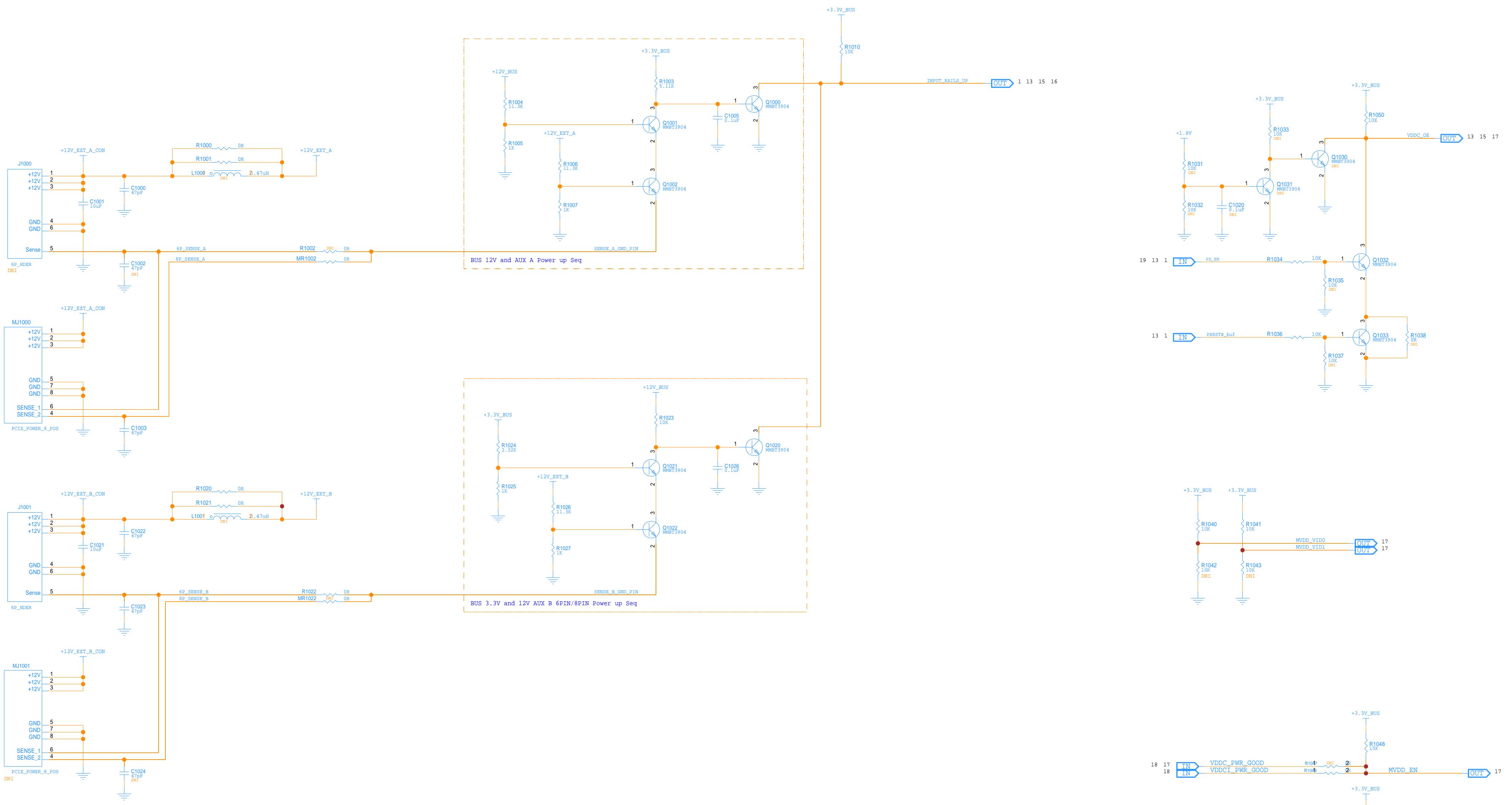
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SHEET NUMBER:

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## (14) POWER MGMT



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SHEET: POWER MNGMT

DATE: Wed Nov 02 15:28:38 2011 REV: 1.0

SHEET NUMBER: 14 OF 21

DOCUMENT NUMBER: 105-C38600-00

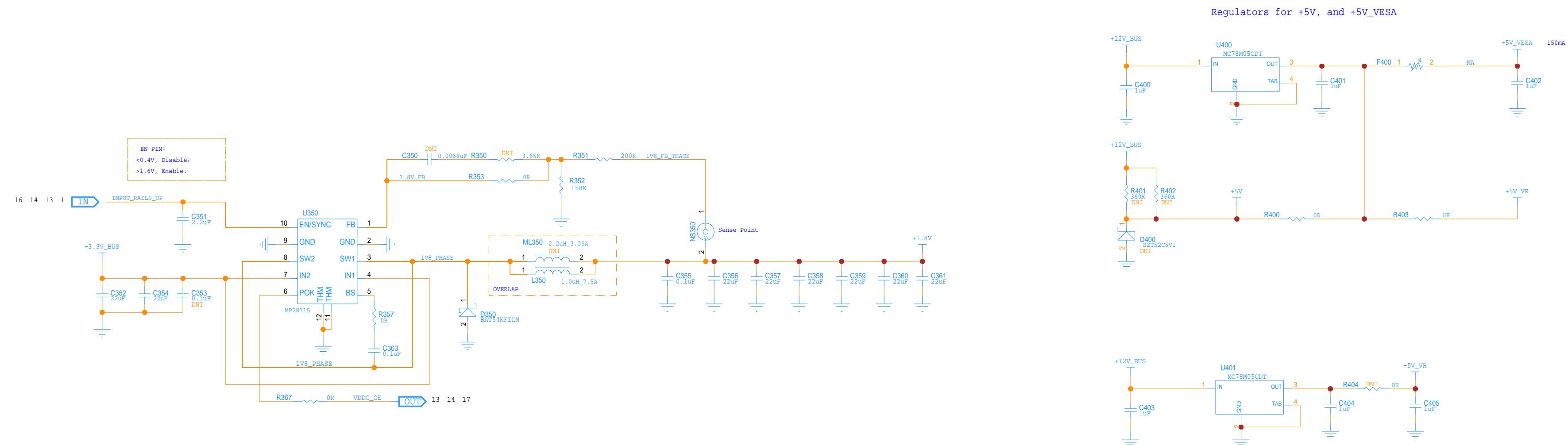
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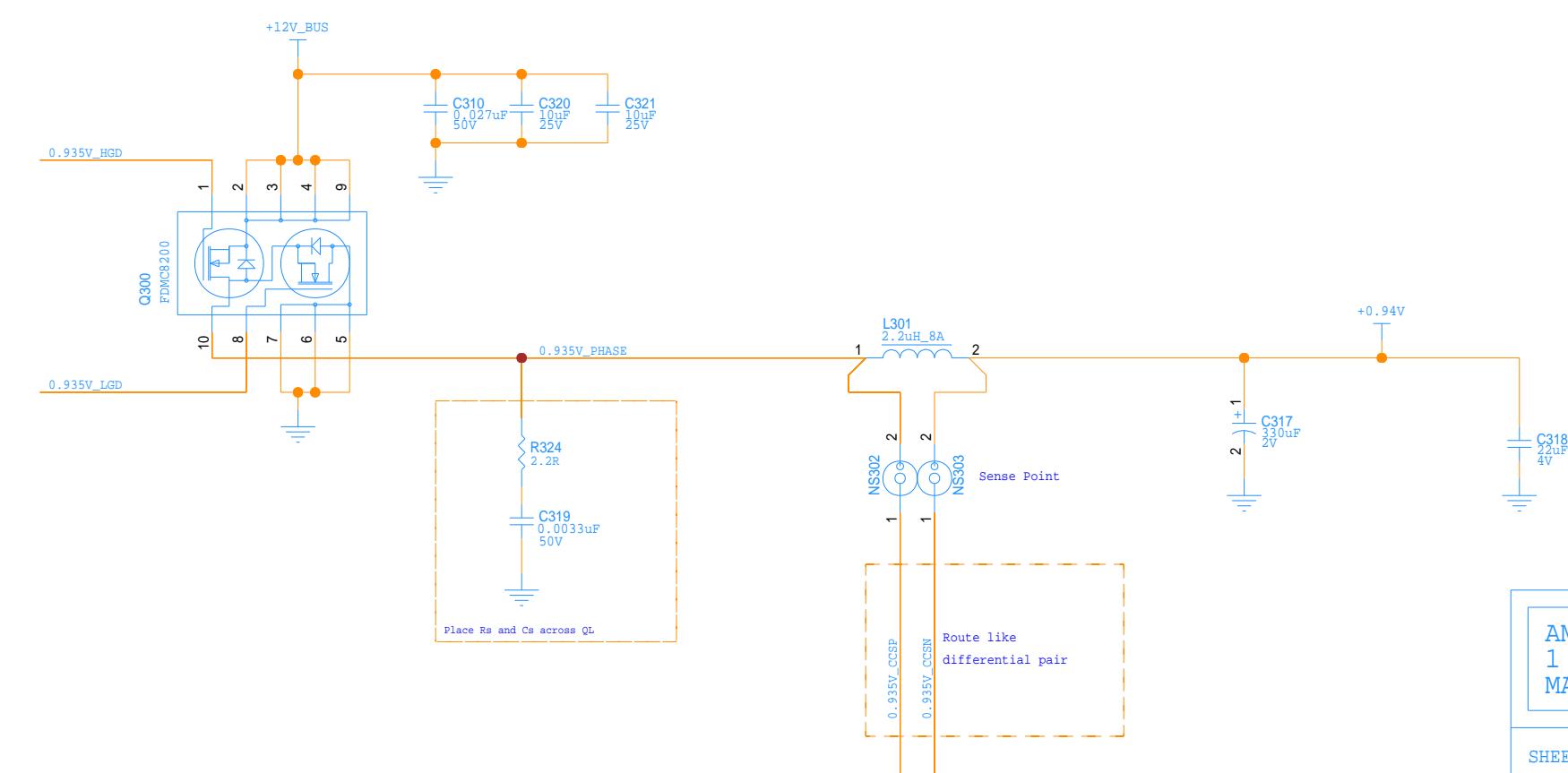
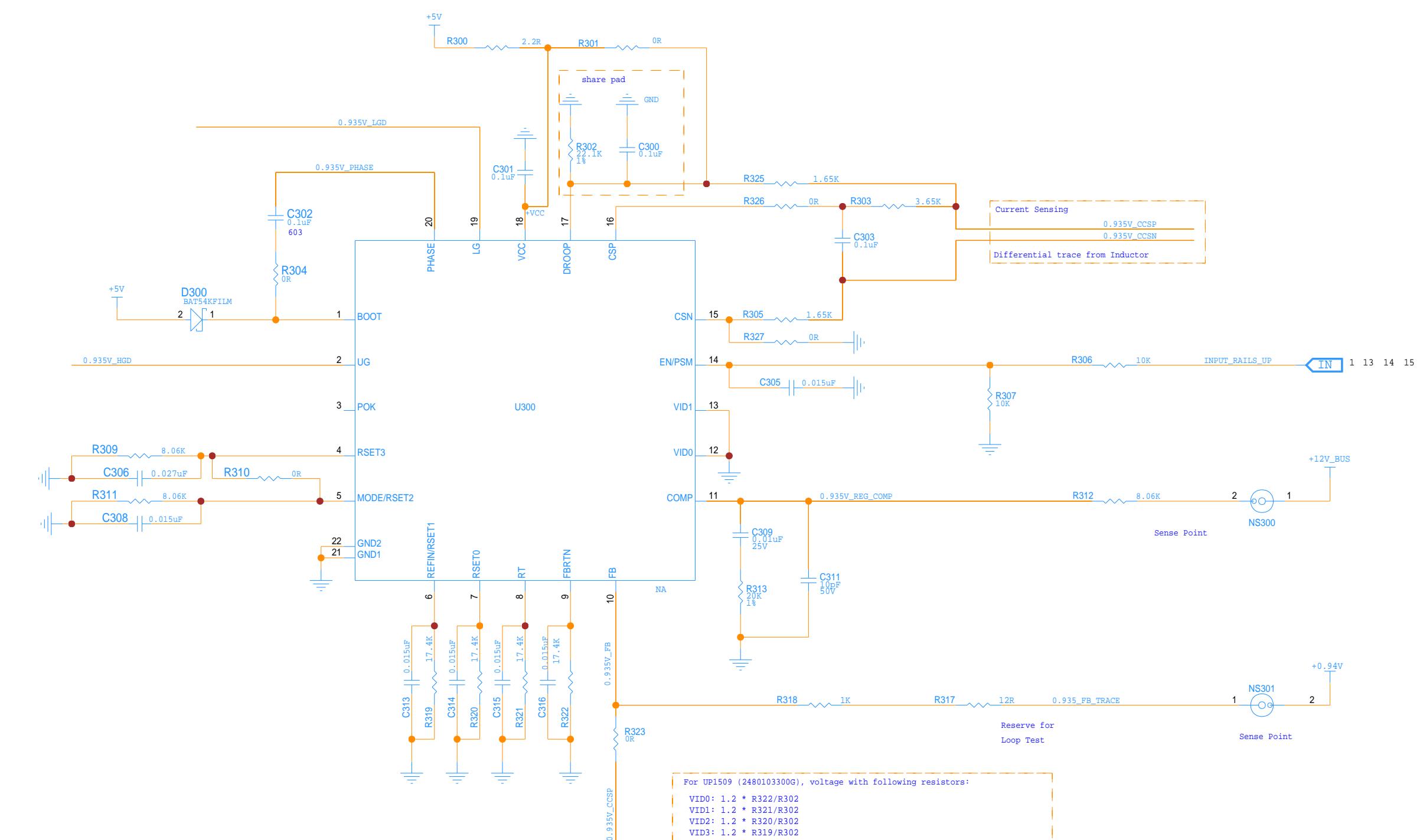
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## (15) BIF, 5V, 1.8V REG



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SHEET: BIF 1.8V 5V REG		TITLE: <b>TITLE</b>	
DATE: Wed Nov 02 15:28:38 2011		REV: 1.0	
SHEET NUMBER: 15 OF 21		TITLE: <b>TITLE</b>	
DOCUMENT NUMBER: 105-C38600-00			
NOTES: NOTE			

## (16) 0.94V REG



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SHEET: 0.94V REG

DATE: Wed Nov 02 15:28:38 2011

REV: 1.0

SHEET NUMBER: 16 OF 21

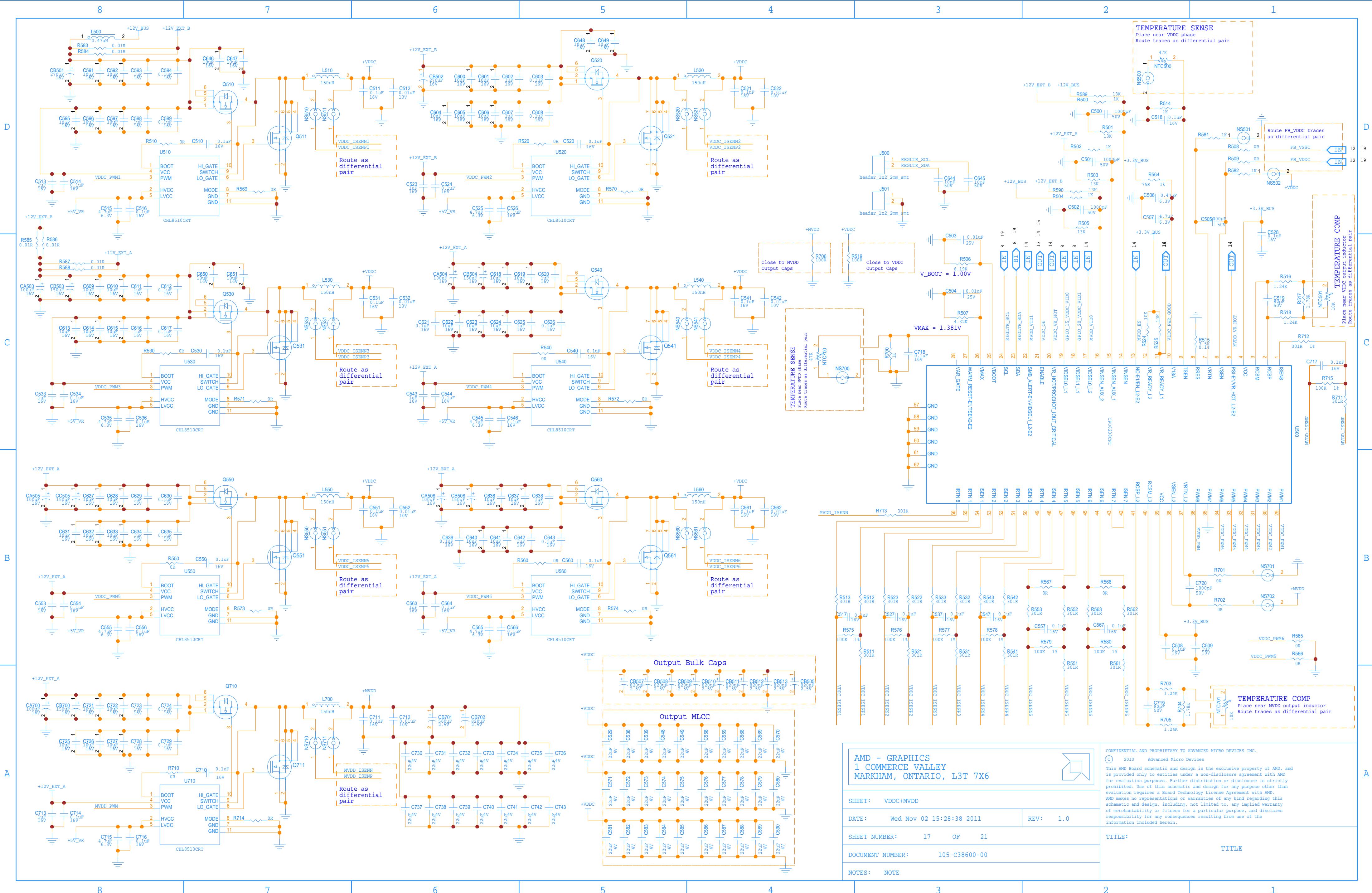
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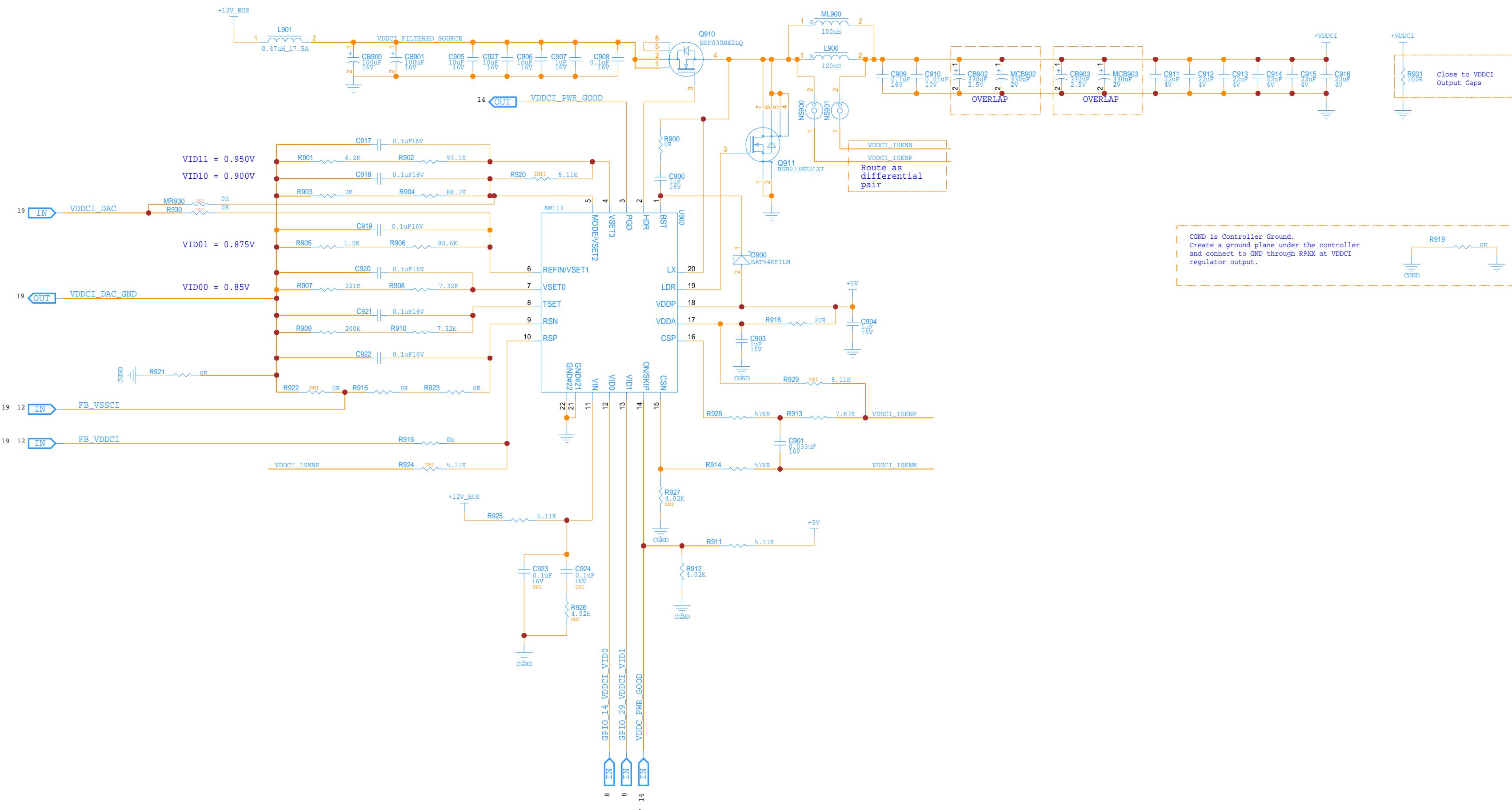
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SHEET: VDDCI

DATE: Wed Nov 02 15:28:38 2011

REV: 1.0

SHEET NUMBER: 18 OF 21

DOCUMENT NUMBER: 105-C3860-00

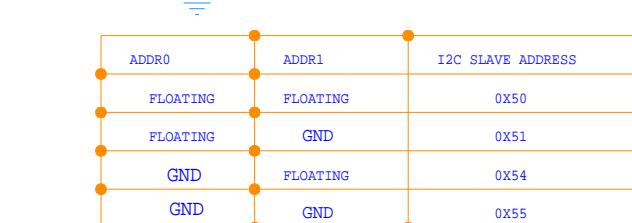
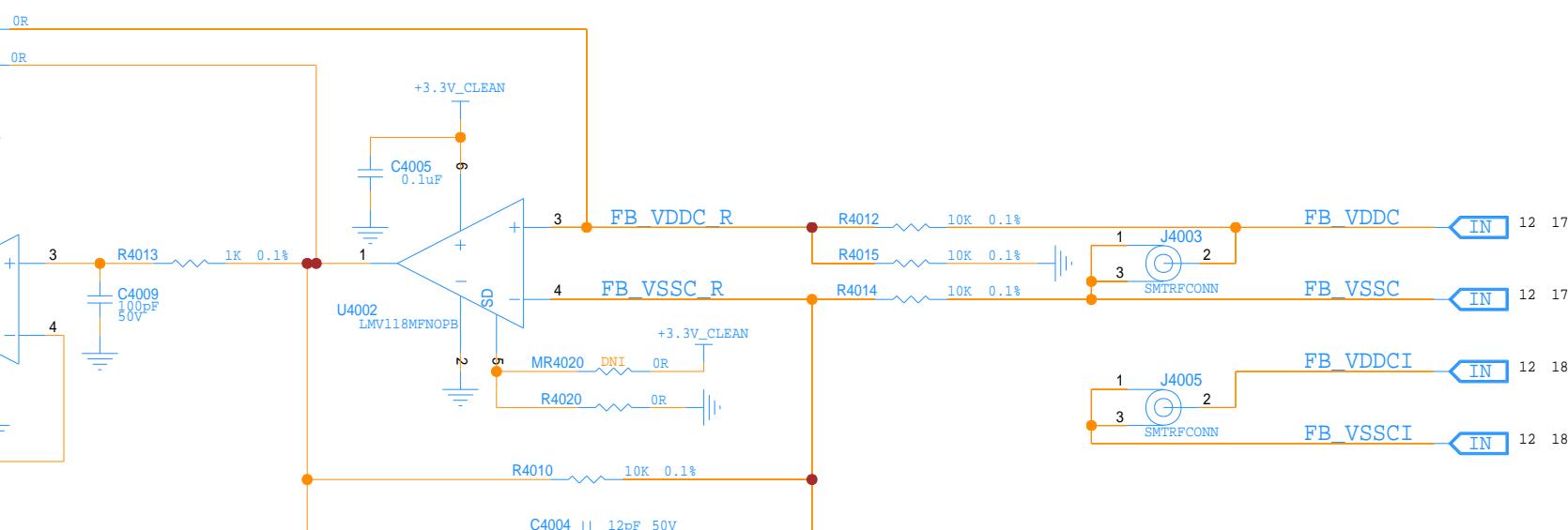
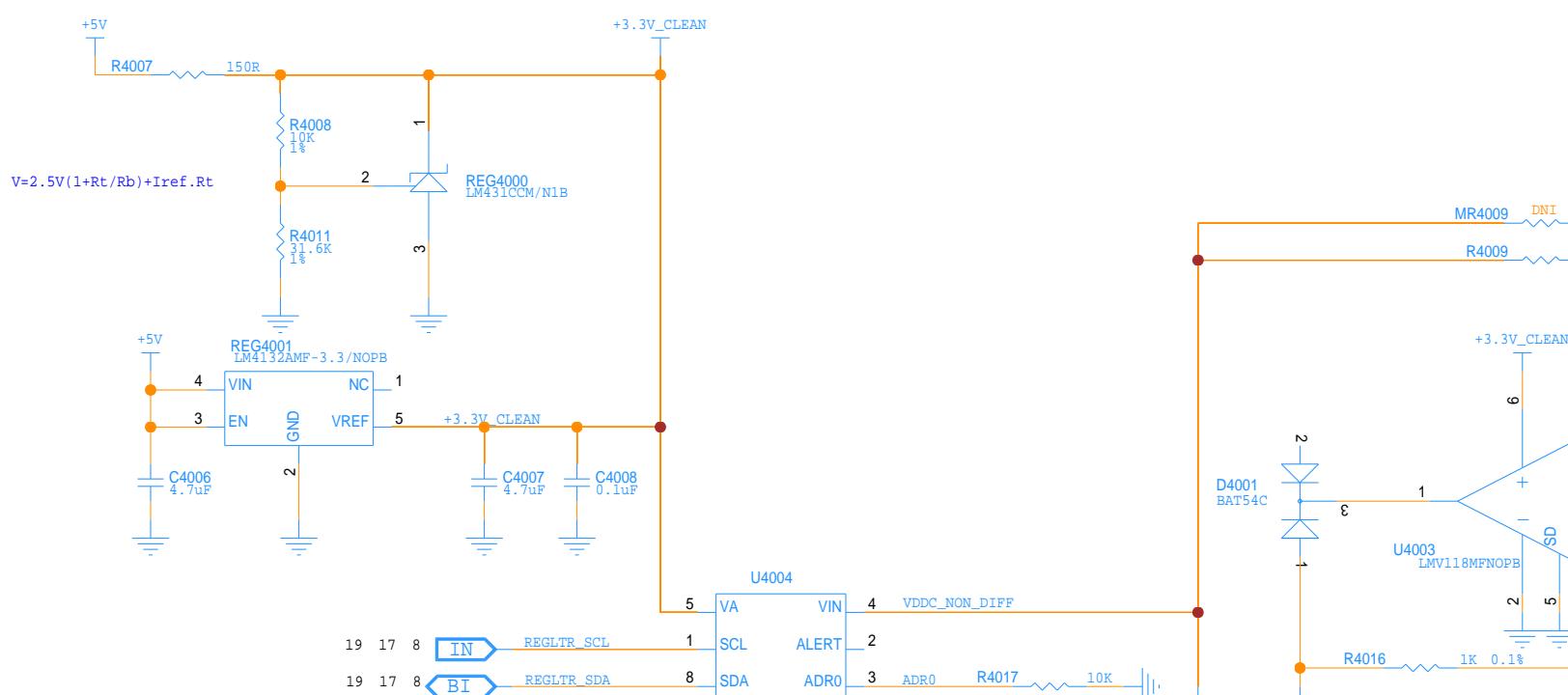
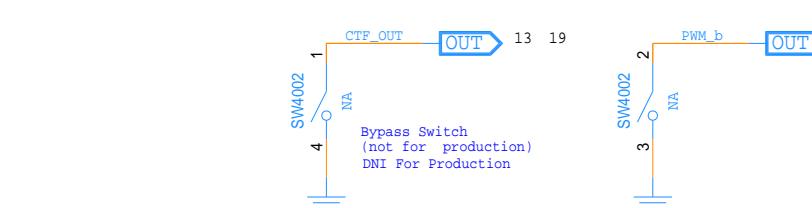
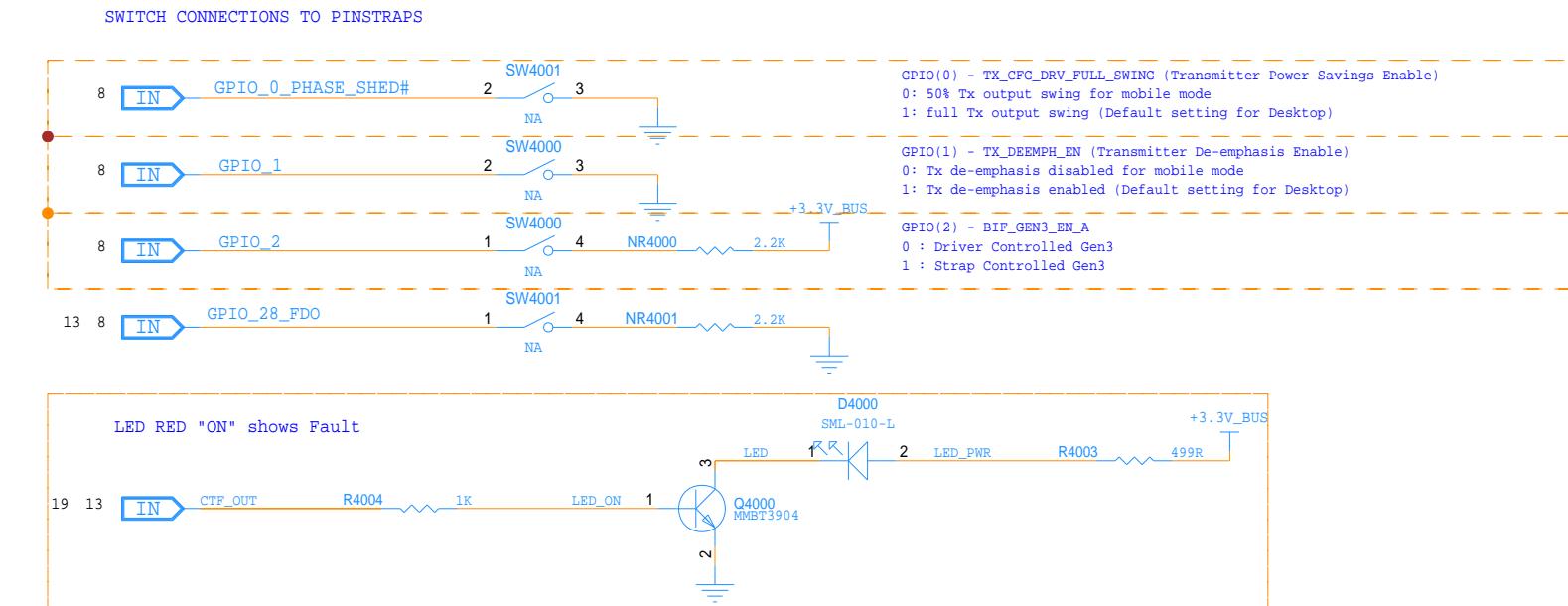
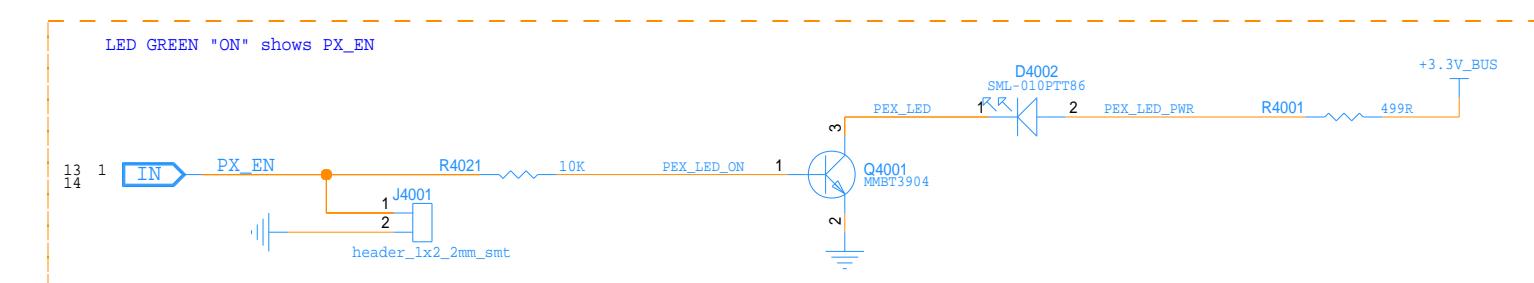
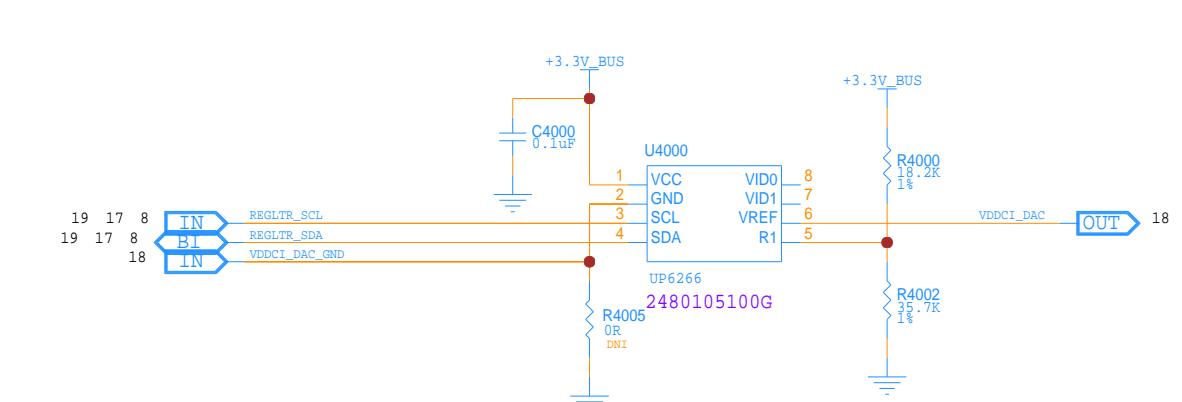
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## (21) DEBUG CIRCUITS



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SHEET: DEBUG CIRCUITS

DATE: Wed Nov 02 15:28:38 2011 REV: 1.0

SHEET NUMBER: 19 OF 21

DOCUMENT NUMBER: 105-C38600-00

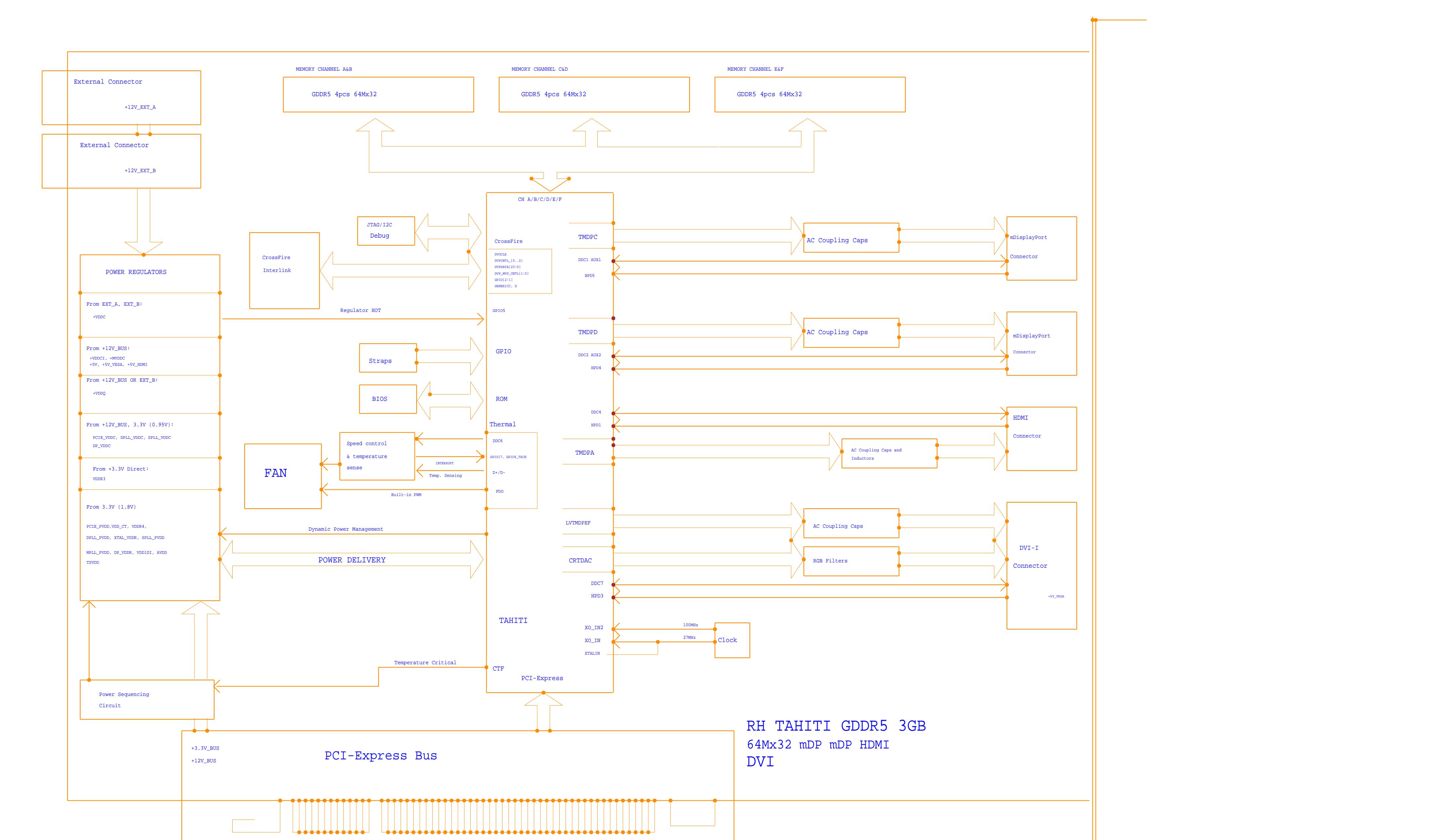
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SHEET: BLOCK DIAGRAM

DATE: Fri Oct 28 12:01:04 2011 REV: 1.0

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DOCUMENT NUMBER: 105-C38600-00

DATE: Thu Nov 03 14:05:25 2011

SHEET NUMBER: 21 OF 21

REV: 1.0

## REVISION HISTORY

ENGINEER:

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SCH Rev	PCB Rev	Date	REVISION DESCRIPTION	D
1	00B	11/08/01	Base on -00A : 1. Change the power deliver tree for support Pro ASIC 2. Change the VDDC input bulk caps due to height validation the specs	
2	00	11/11/01	Base on -00B : 1. Change the circuit for fan control in BACO mode	
A				A
B				B
C				C
D				D