P584-A01: MXM-I, G86M, 256/128MB, 64-bit 32M16 or 16M16(4 pcs) DDR2 LVDS, DVI _A, TV_OUT, VGA, HDMI /HDCP

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SKU	VARI ANT	NVPN	ASSEMBLY
В	BASE	600-10584-0000-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10584-0001-000	G86M ?/? 256MB(64bit) DDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA
2	SKU0002	600-10584-0002-000	G86M ?/? 128MB(64bit) DDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA
3	SKU0003	600-10584-0003-000	G86M ?/? 256MB(64bit) DDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA
4	SKU0004	600-10584-0004-000	G86M ?/? 128MB(64bit) DDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA
5	<undefi ned=""></undefi>	<undefi ned?<="" th=""><th><undefi ned?<="" th=""></undefi></th></undefi>	<undefi ned?<="" th=""></undefi>
6	<undefi ned=""></undefi>	<undefi ned=""></undefi>	<undefi ned=""></undefi>
7	<undefi ned=""></undefi>	<undefi ned=""></undefi>	<undefi ned=""></undefi>
8	<undefi ned=""></undefi>	<undefi ned=""></undefi>	<undefi ned=""></undefi>
9	<undefi ned=""></undefi>	<undefi ned=""></undefi>	<undefi ned=""></undefi>
10	<undefi ned=""></undefi>	<undefi ned=""></undefi>	<undefi ned=""></undefi>
11	<undefi ned=""></undefi>	<undefi ned=""></undefi>	<undefi ned=""></undefi>
12	<undefi ned=""></undefi>	<undefi ned=""></undefi>	<undefi ned=""></undefi>
13	<undefi ned=""></undefi>	<undefi ned=""></undefi>	<undefi ned=""></undefi>
14	<undefi ned=""></undefi>	<undefi ned=""></undefi>	<undefi ned=""></undefi>
15	<undefi ned=""></undefi>	<undefi ned=""></undefi>	<undefi ned=""></undefi>
			-

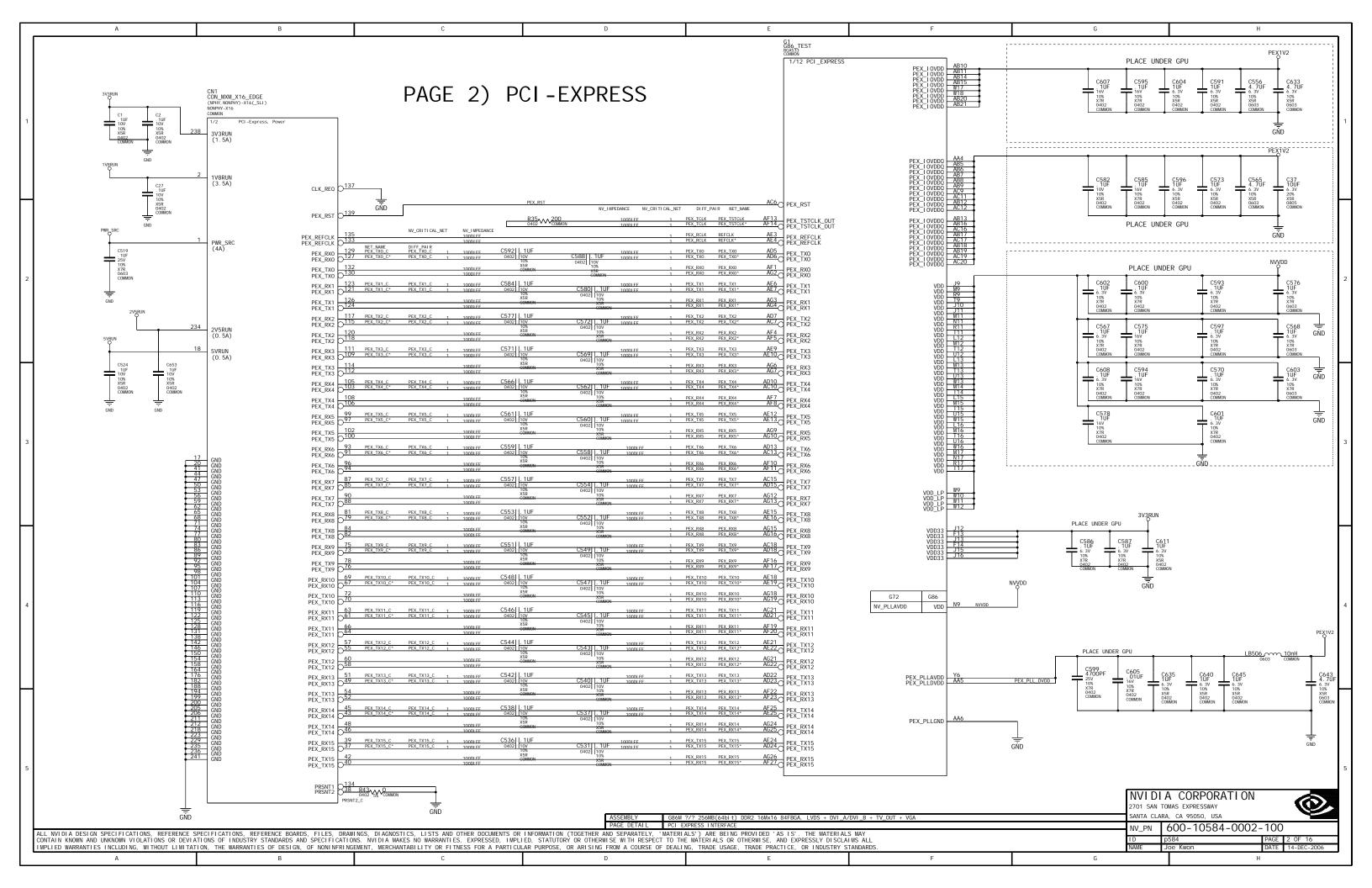
NVIDIA CORPORATION

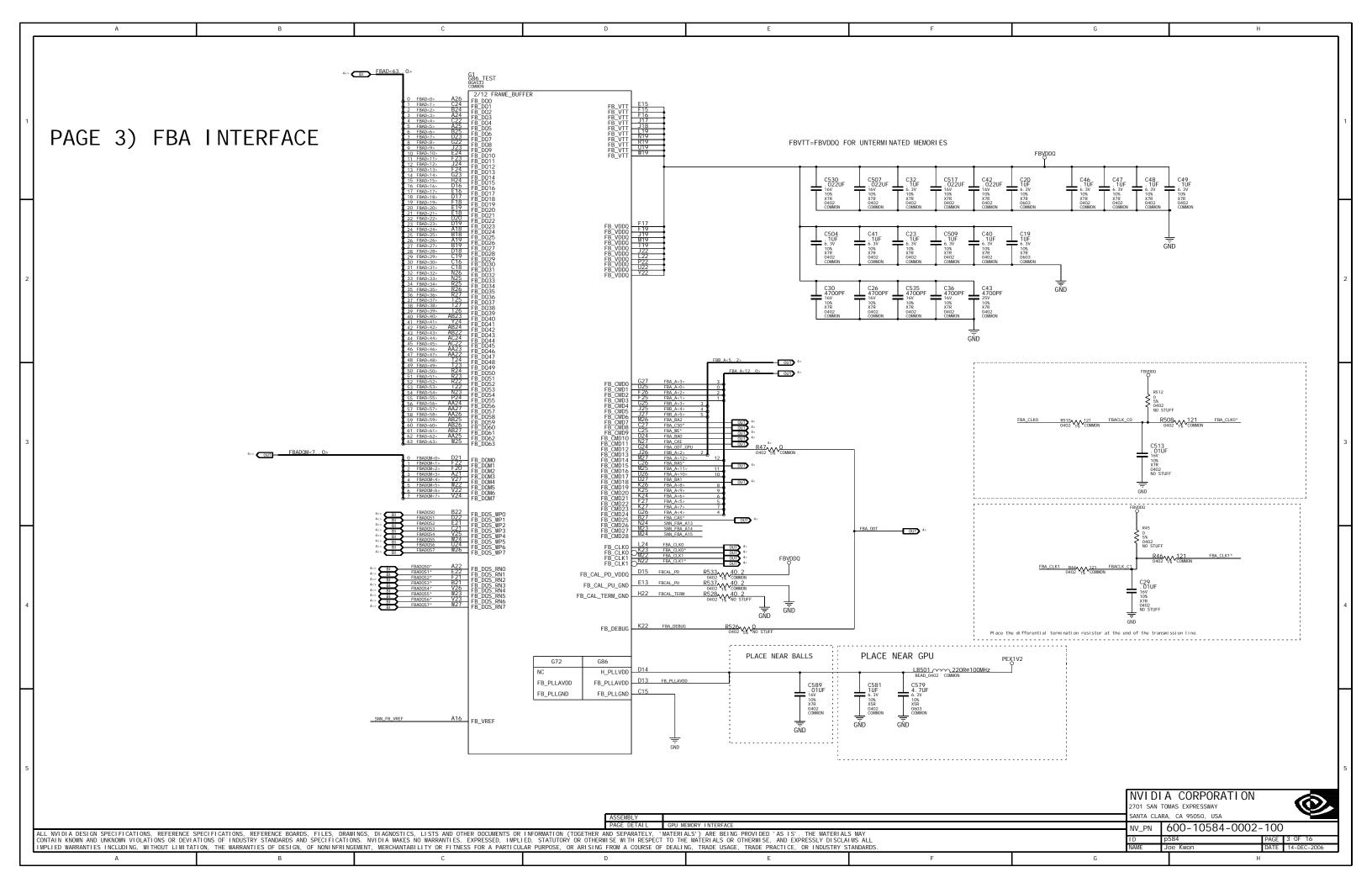
2701 SAN TOMAS EXPRESSWAY

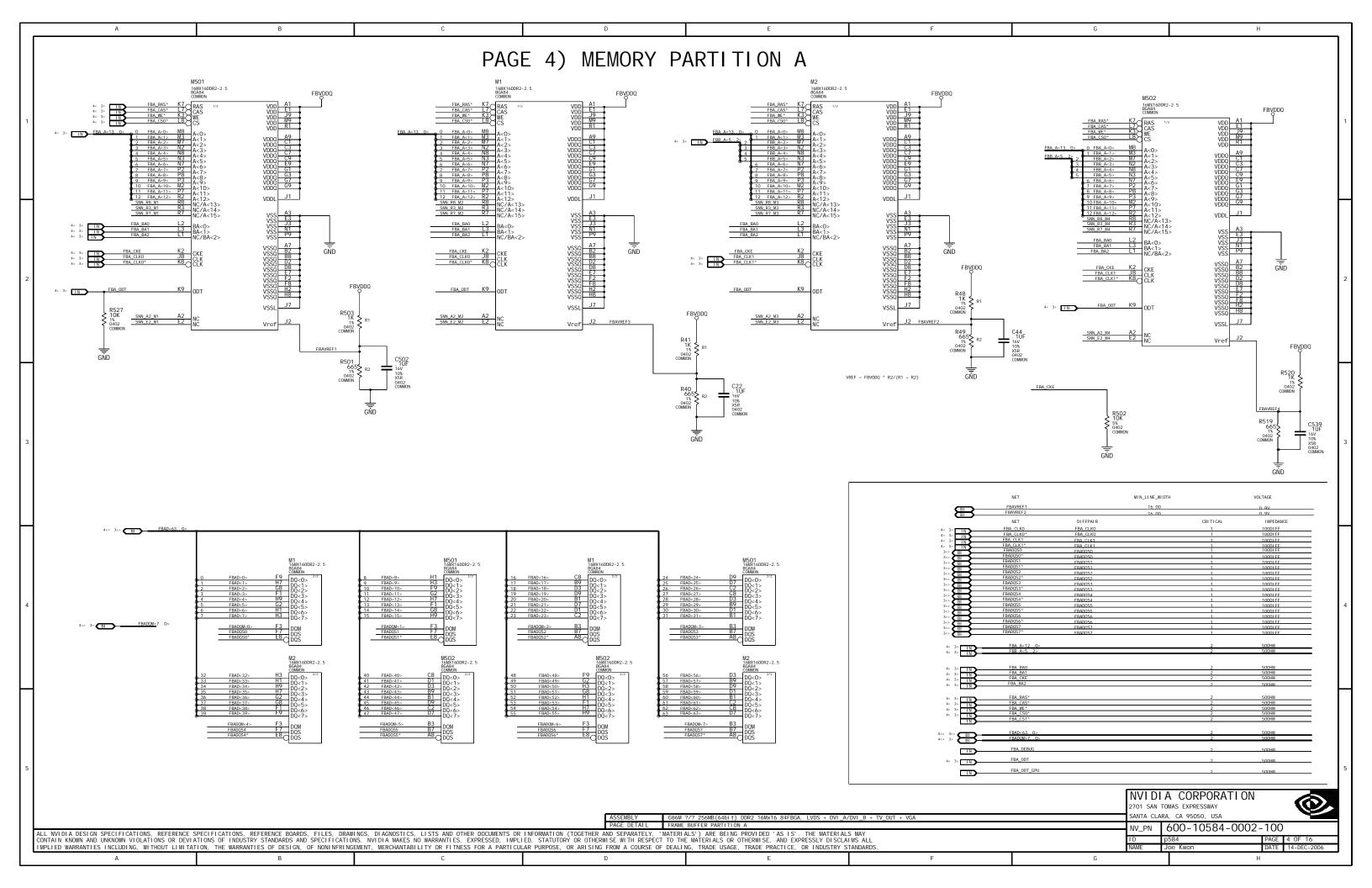
SANTA CLARA, CA 95050, USA

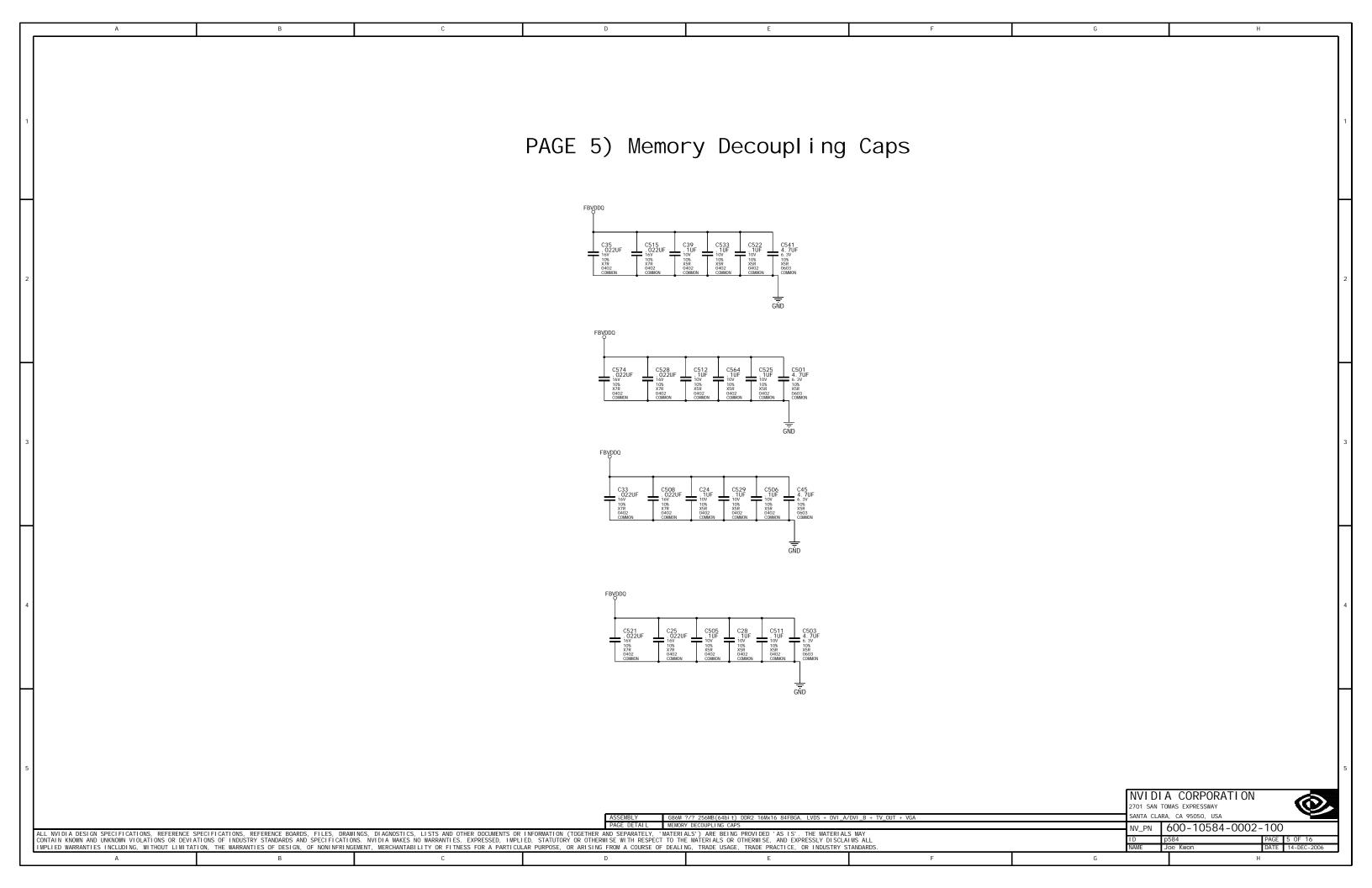
NV_PN 600-10584-0002-100

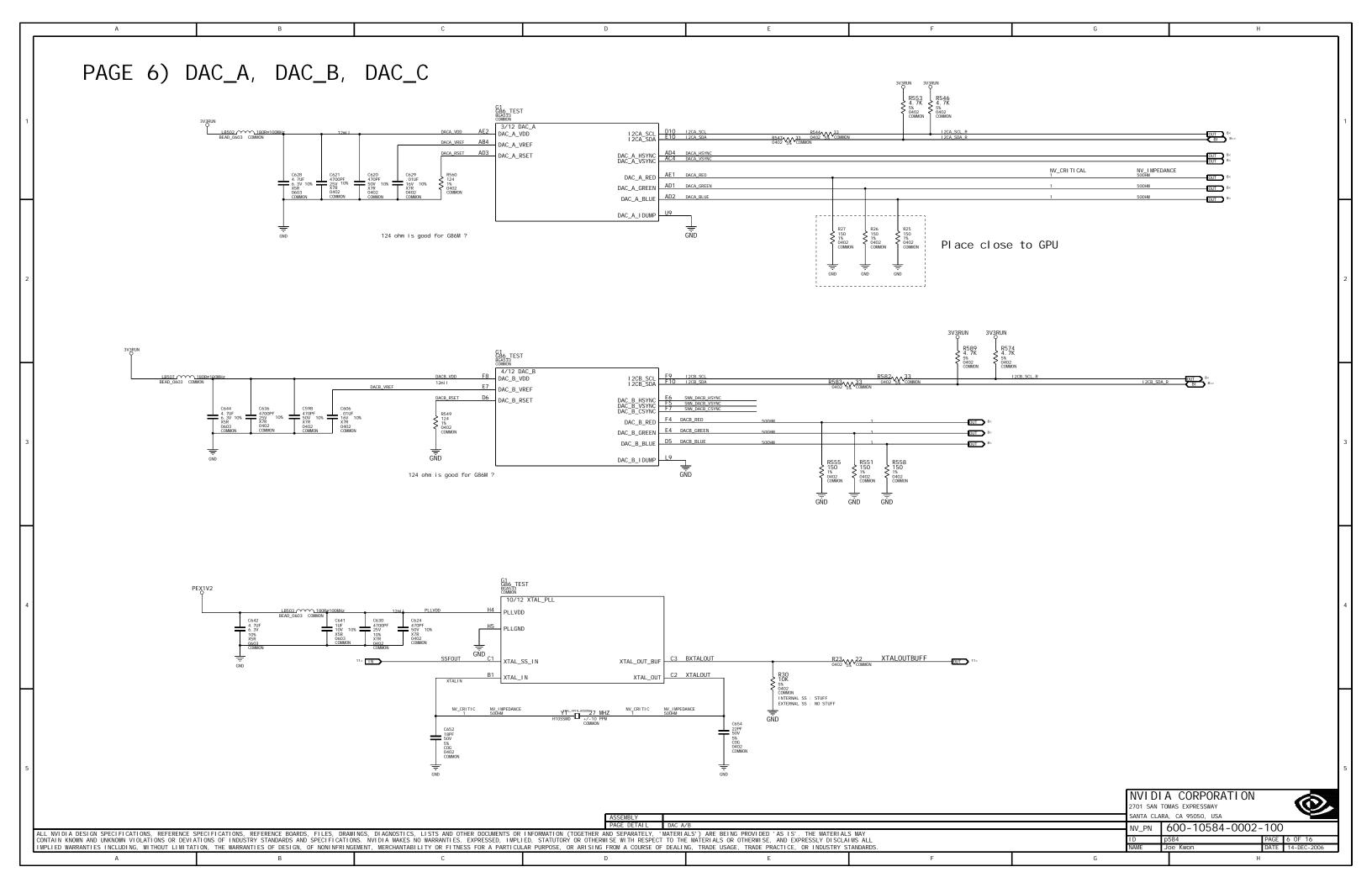
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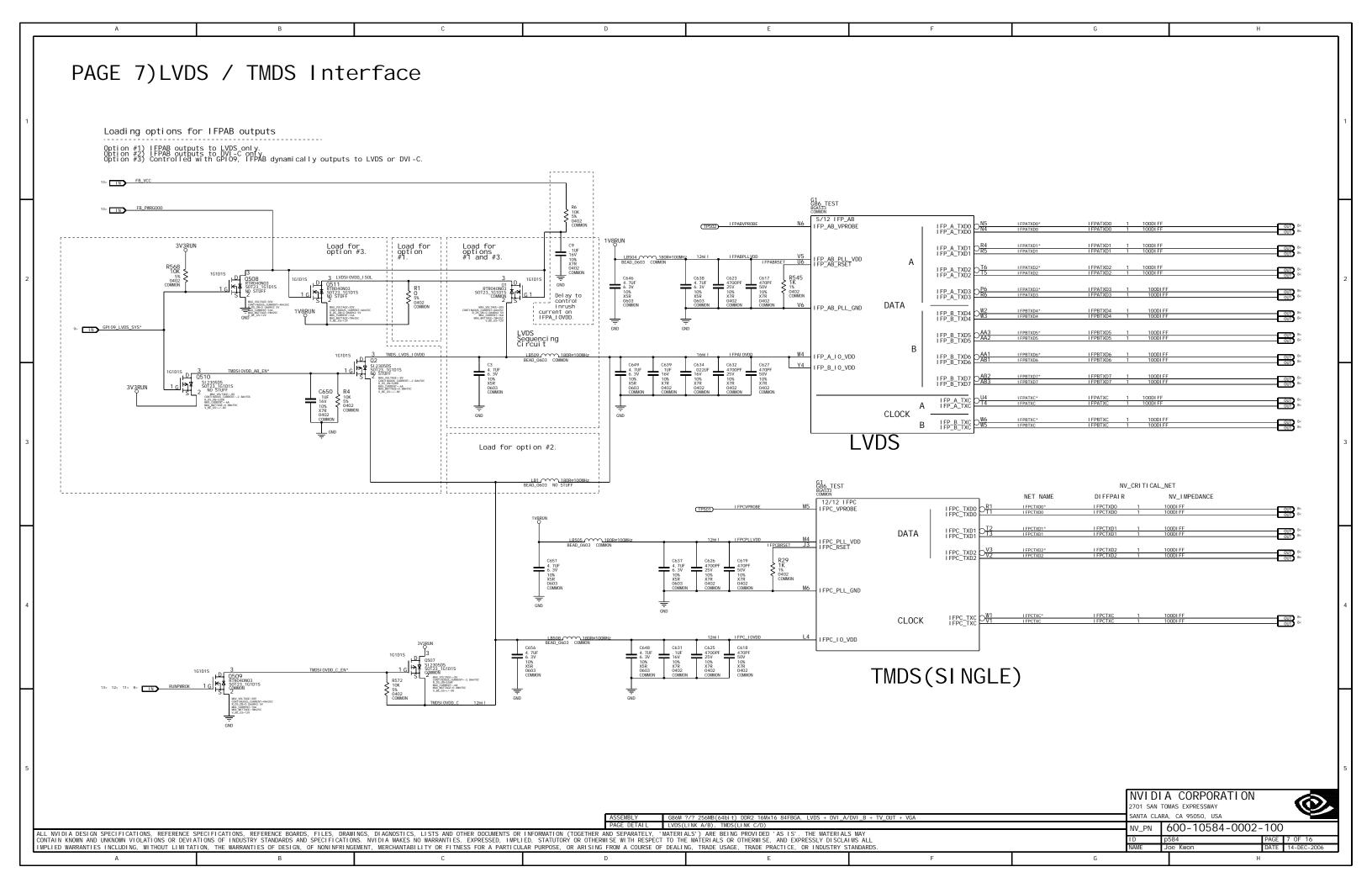


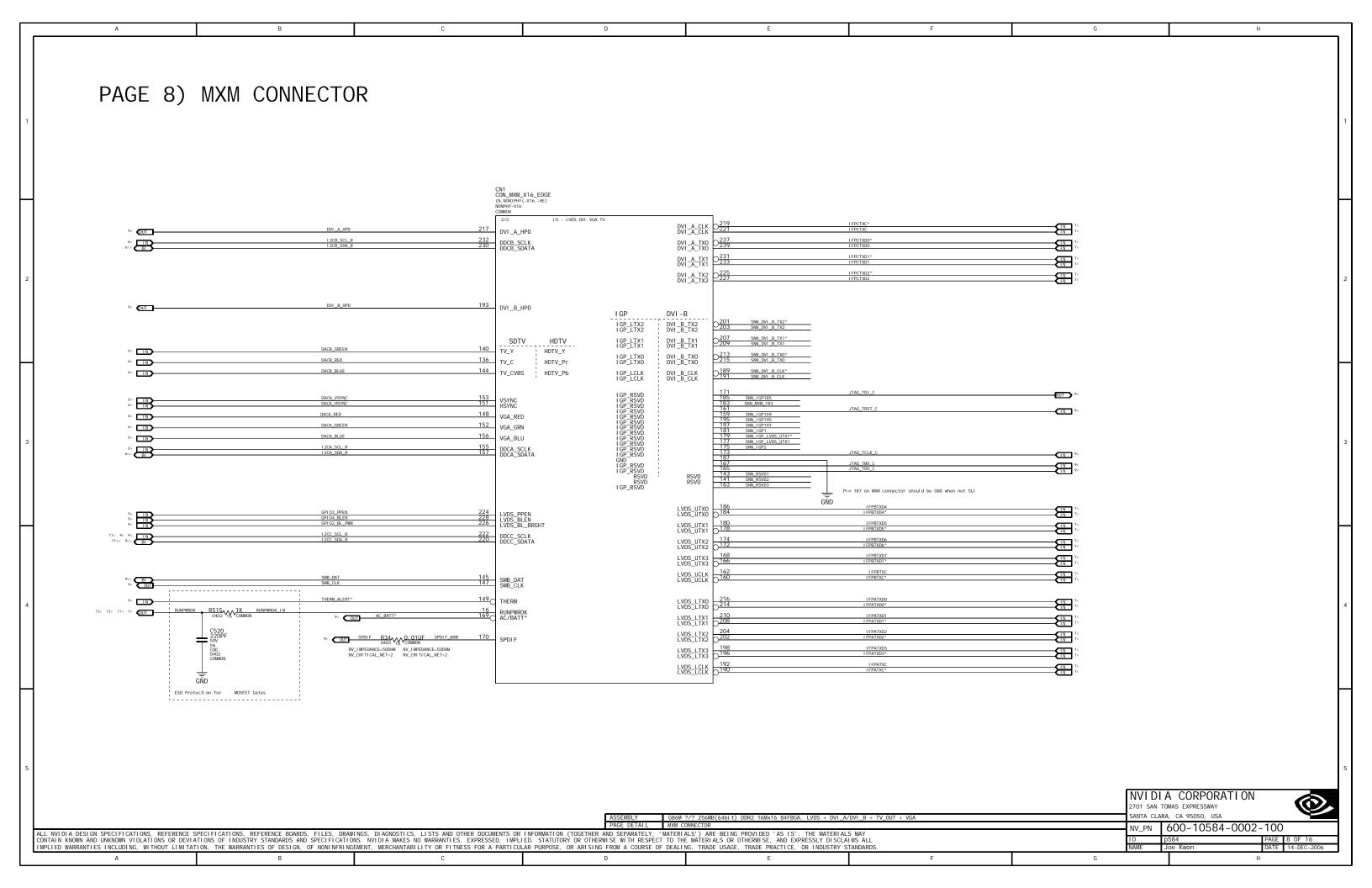


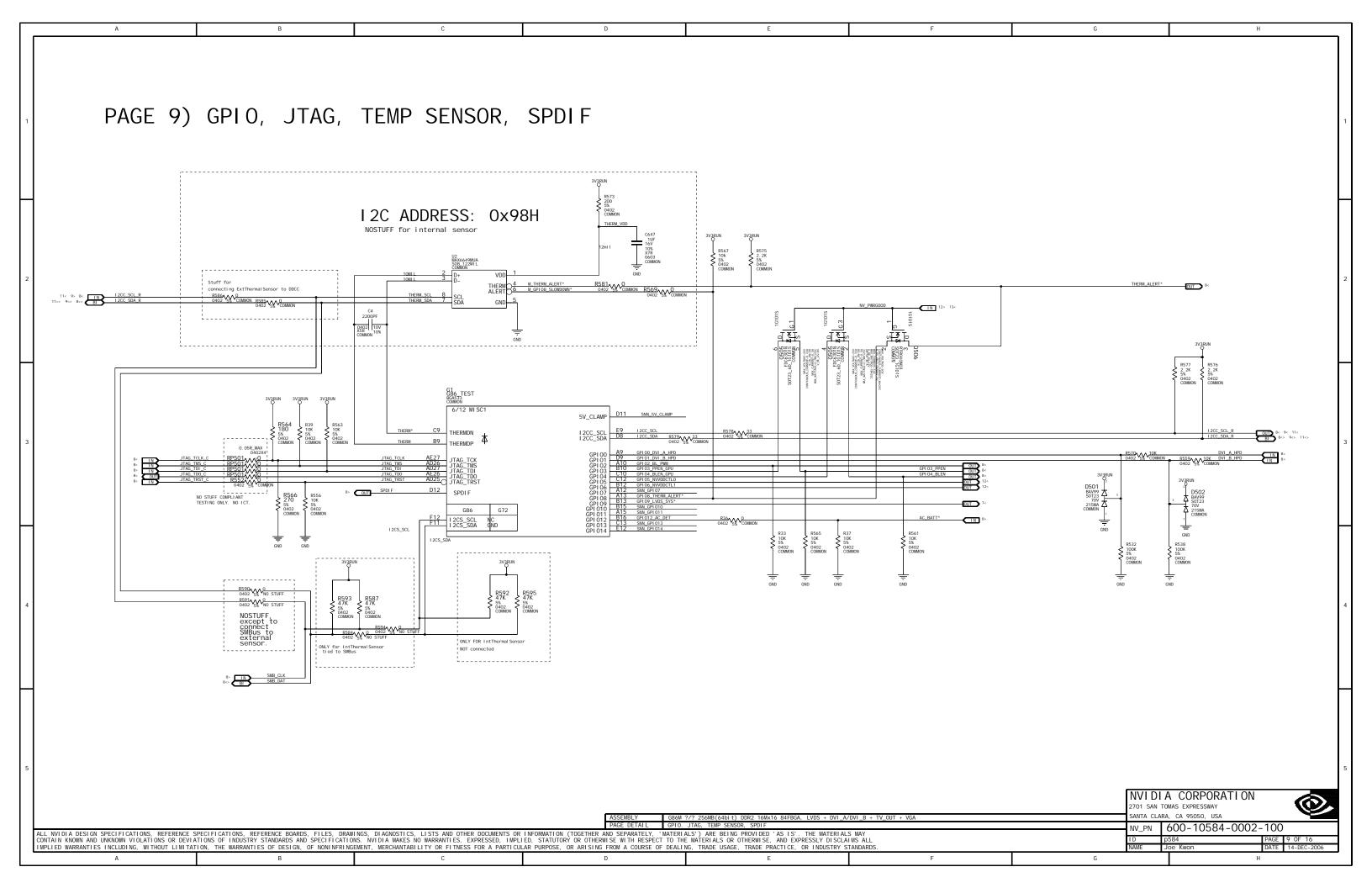


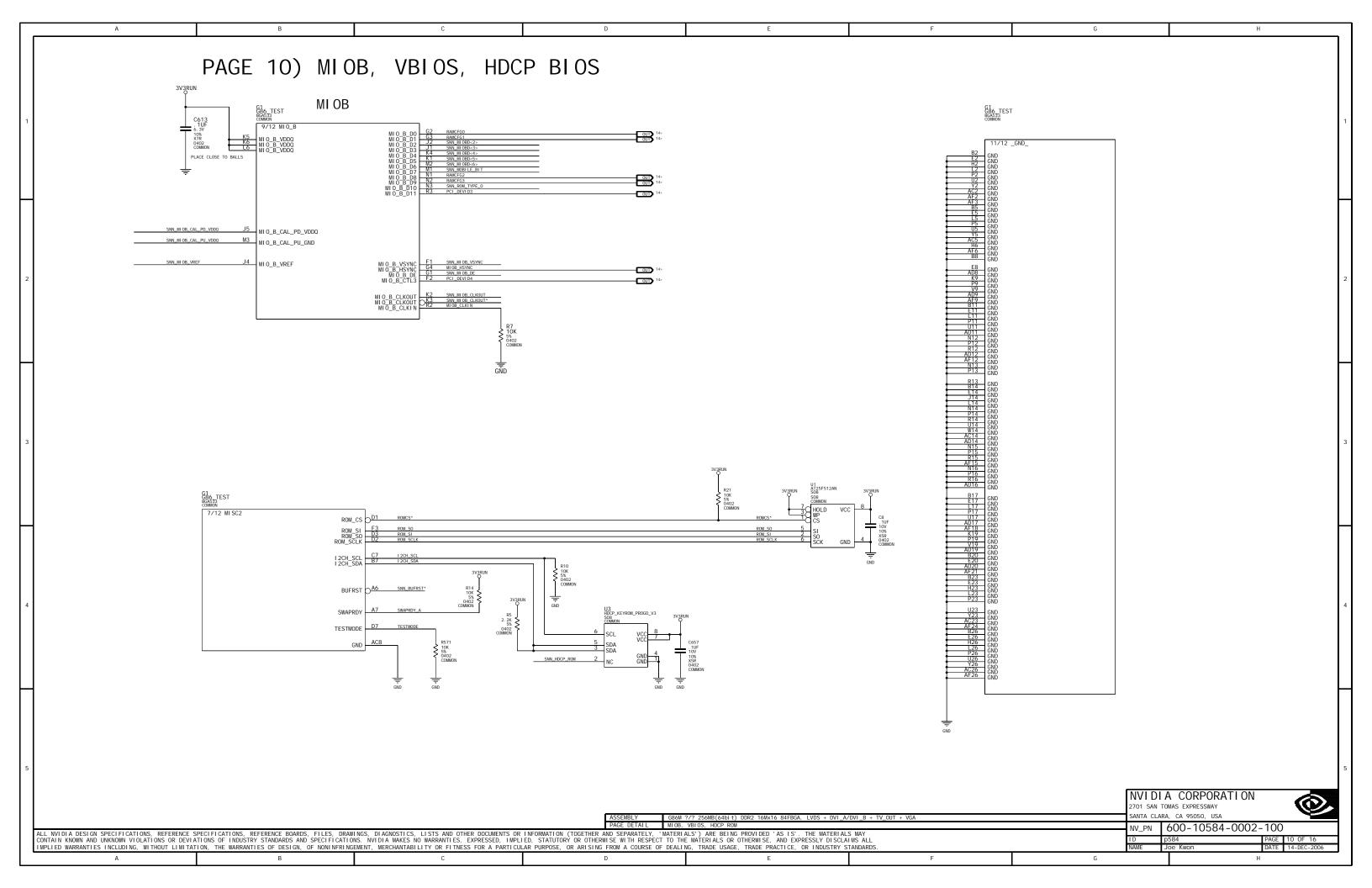


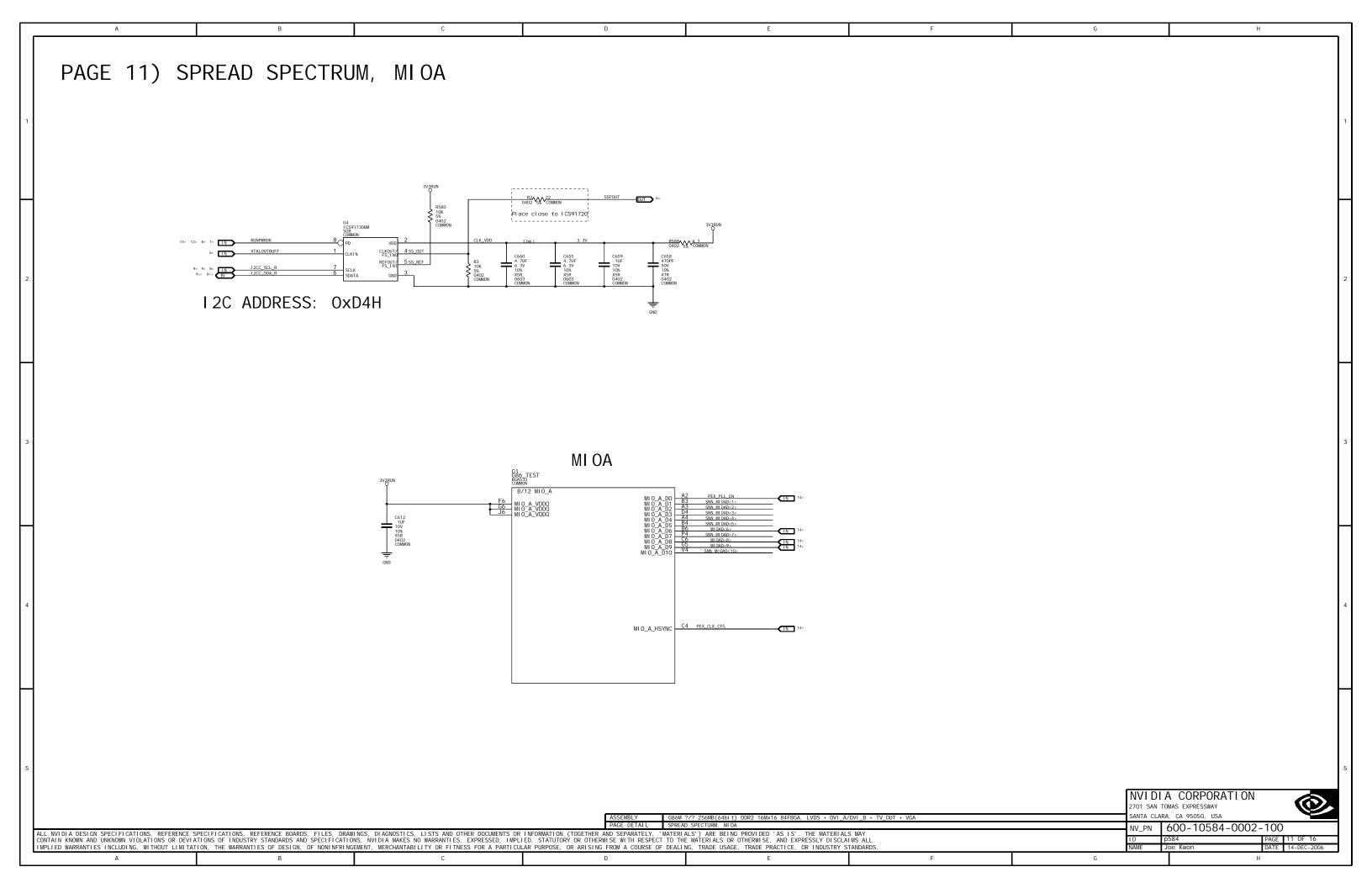


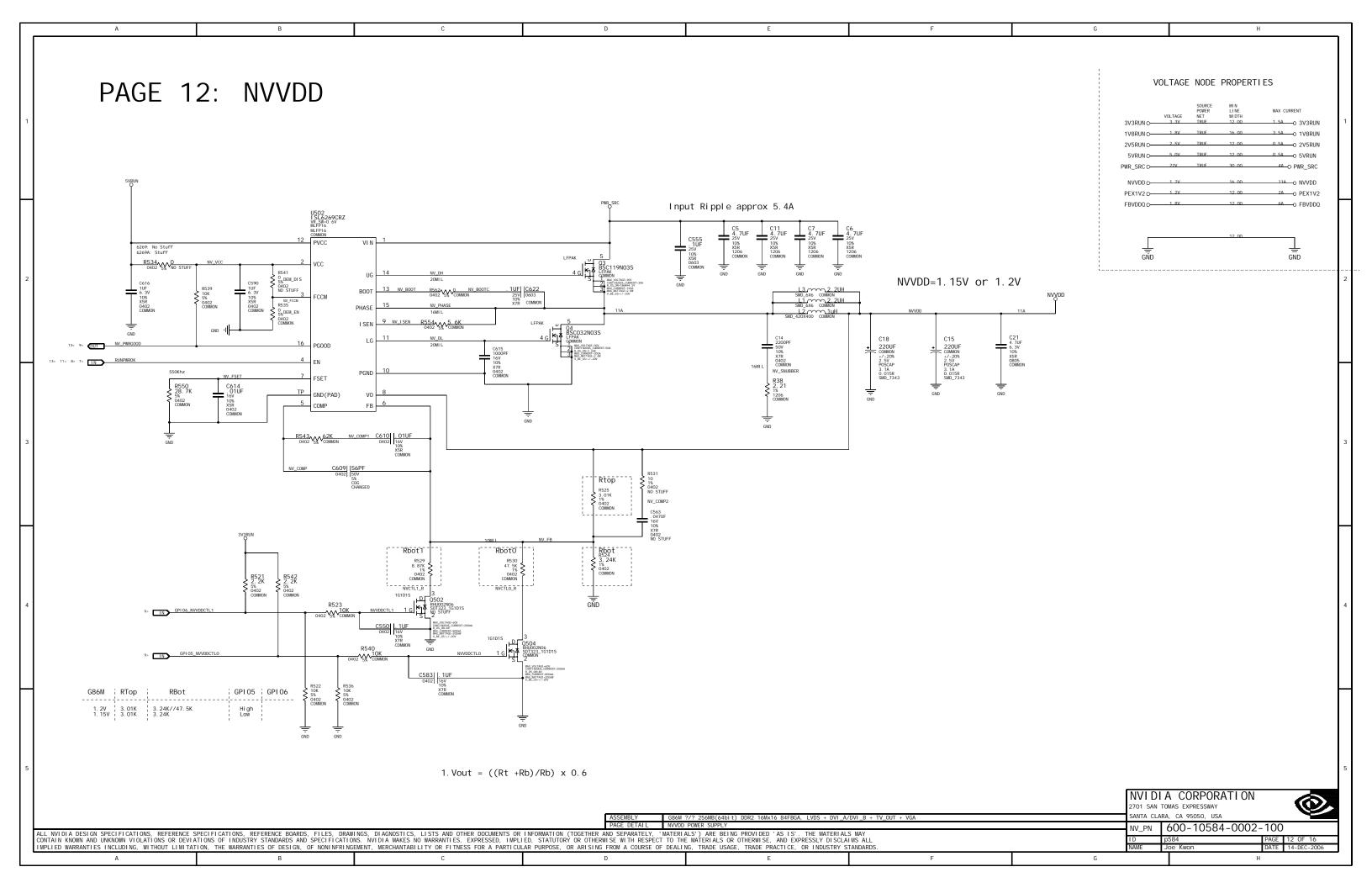


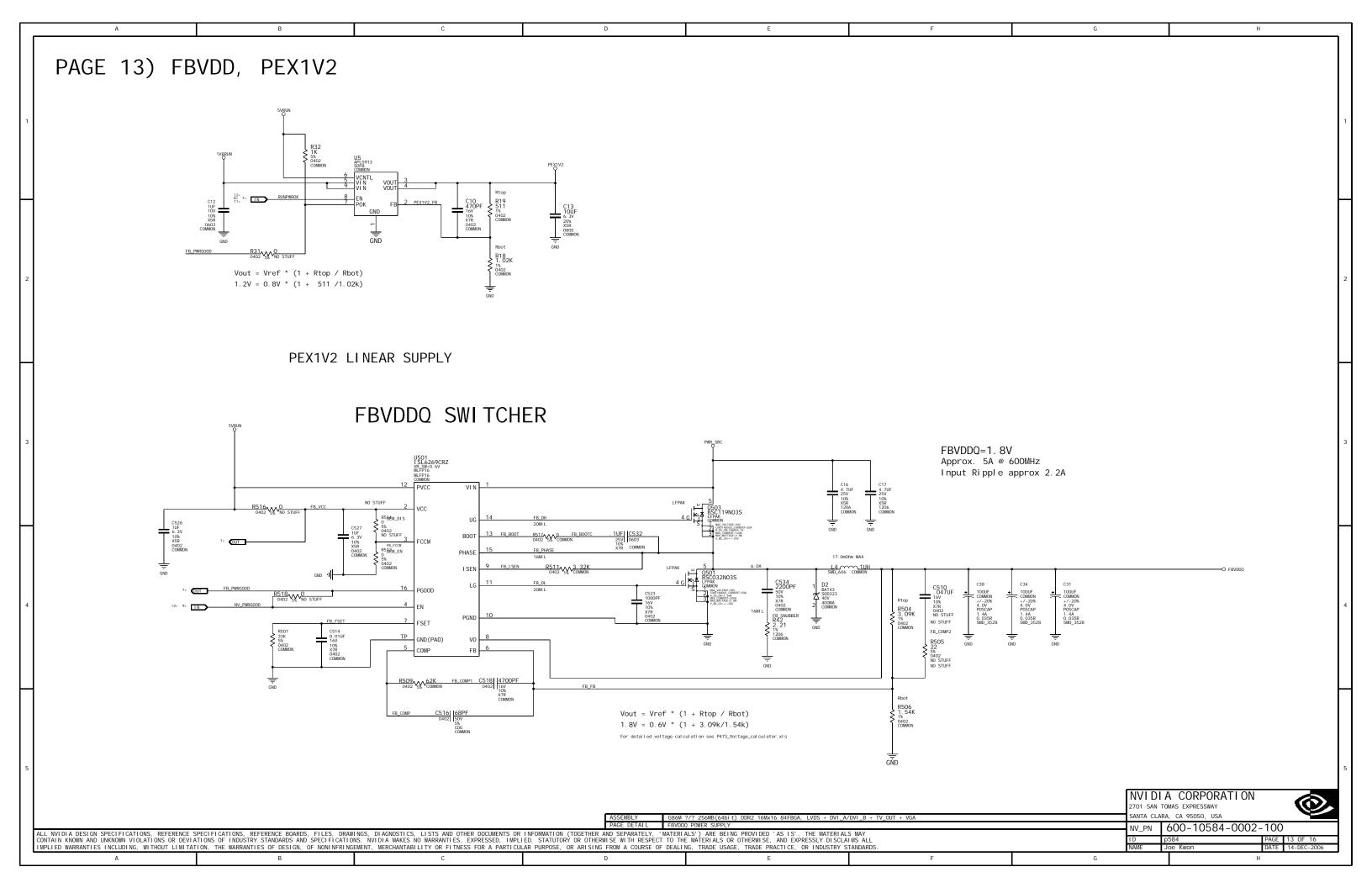


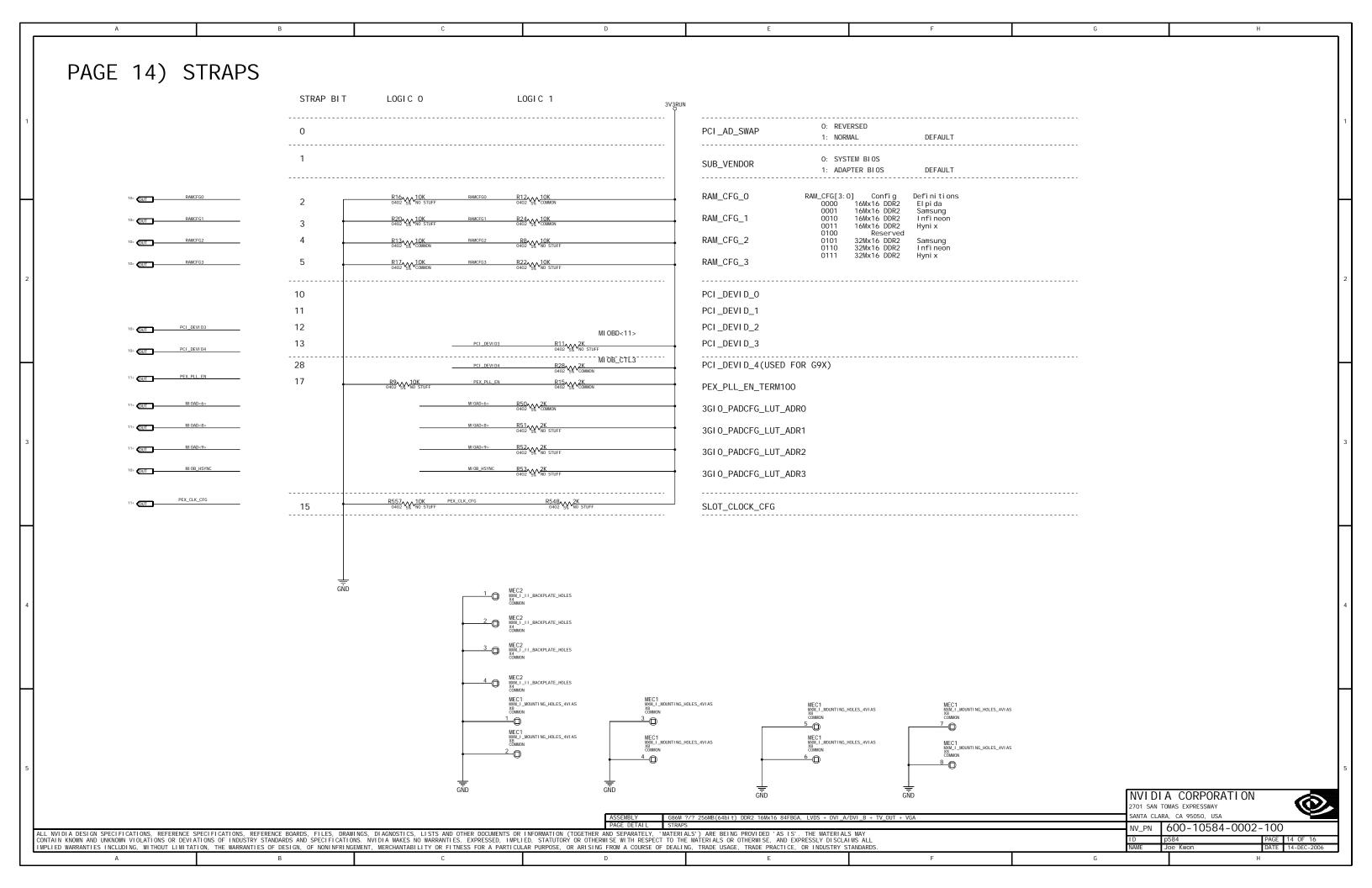












Α G Ti tle: Basenet Report FB_DL Desi qn: FBADOM<2: 3.3C 4.4D FB FB 13.4D NVVDDCTI O 12.4C PEX TX9 C 2.4C SNN MLOB CAL PU VD 10, 2A Dec 12 17: 33: 02 2006 13. 4C 12. 4C 2. 4C Date: FBADQM<3> FB_FCCM NVVDDCTL1 PEX_TX9_C* FBADOM<4> 3.3C 4.5B FB_FSET 13. 4B NV BOOT 12. 2C 12. 2C PFX TX10 2. 4E 2. 4E SNN MLOB CLKOUT FB_I SEN FBADQM<5> NV_BOOTO PEX_TX10 SNN_MI OB_CLKOUT* p419 lib. P419(@p419 lib. p419(sch 1)) FBADQM<6> 3.3C 4.5D FB PHASE 13. 4D NV COMP 12. 3B PEX TX10 C 2. 4C SNN MIOB DE 10. 2C 12. 3B PEX_TX10_C 2. 4C FBADQM<7> FB_PLLAVDD 3.4D NV_COMP1 SNN_MI OB_VREF 10. 2A Location([Zone][dir]) Base Si gnal FRADOSO 3.3C<> 4.4B 4.4F<> FB PWRGOOD 7. 2A< 13. 2A 13. 4A NV COMP2 12. 3D PFX TX11 2.4F SNN MLOB VSYNC 10. 2C 12. 2C 2. 4E FBADQS0* 3. 4C<> 4. 4B 4. 4F<> FB_SNUBBER NV_DH PEX_TX11* SNN_MOBI LE_BI T BXTALOUT 6. 4D FBADQS1 3. 3C<> 4. 4C 4. 4F<> FB VCC 7. 1A< 13. 4B> NV DL 12. 2C PEX TX11 C 2.4C SNN MXM 183 8. 3E 2. 4C CLK_VDD 11. 2C FBADQS1 GPI 00_DVI _A_HPD NV_FB 12. 4D PEX_TX11_C SNN_R3_M1 DACA BLUE 6. 2H> 8. 3A< FBADOS2 3. 4C<> 4. 4D 4. 4F<> GPI 01 DVI B HPD 9. 3D NV FCCM 12. 2B PFX TX12 2.4F SNN R3 M2 4. 2C GPI 02_BL_PWM DACA_GREEN 6. 1H> 8. 3A< FBADQS2 3. 4C<> 4. 4D 4. 4F<> NV_FSET 12. 3B PEX_TX12* SNN_R3_M3 DACA HSYNO 6. 1H> 8. 3A< FBADQS3 3. 4C<> 4. 4D 4. 4F<> GPI 03 PPEN 8. 3A< 9. 3F> NV ISEN 12. 2C PEX TX12 C 2.4C SNN R3 M4 4. 2G 6. 1H> 8. 3A< 3. 4C<> 4. 4D 4. 4F<> GPI 03_PPEN_GPU 2. 4C DACA_RED FBADQS3 9. 3D NV_PHASE 12. 2C PEX_TX12_C SNN_R7_M1 DACA RSET 6. 1C FBADQS4 3. 4C<> 4. 4F<> 4. 5B GPI 04 BLEN 8. 3A< 9. 3F> NV PWRGOOD 9. 2F< 12. 2A> 13. 4A< PEX TX13 2. 4E SNN R7 M2 4. 2C DACA_VDD GPI 04_BLEN_GPU NV_SNUBBER 12. 3E PEX_TX13* SNN_R7_M3 9.3F> 12.4A< DACA VRFF 6.1C FBADOS5 3. 4C<> 4. 4F<> 4. 5C GPLOS NVVDDCTLO NV VCC 12. 2B PEX TX13 C 2.4C SNN R7 M4 4. 2G GPI 06_NVVDDCTL1 PCI _DEVI D3 PEX_TX13_C DACA_VSYN SNN_R8_M1 DACB BLUE 6. 3F> 8. 3A< FBADQS6 3. 4C<> 4. 4F<> 4. 5D GPI 08 THERM ALERT* 9.3D PCI DEVID4 10. 2D> 14. 2A> 14. 3C PEX TX14 2. 5E SNN R8 M2 4. 2C DACB_GREEN FBADQS6* GPI 09_LVDS_SYS* PEX1V2_FB PEX_TX14* 2. 5E SNN_R8_M3 11. 4F< 14. 3A> 14. 3C DACB RED 6.3F> 8.3A< FBADOS7 3. 4C<> 4. 4F<> 4. 5D GPI 012 AC DET 9. 3D PEX CLK CEG PEX TX14 C 2.5C SNN R8 M4 4. 2G 3. 4C<> 4. 4F<> 4. 5D 2. 5C DACB_RSET FBADQS7* I 2CA_SCL PEX_PLL_DVDD PEX_TX14_C SNN_ROM_TYPE_0 10. 1C 11. 3E< 14. 3A> 14. 3C DACB VDD 6.3C FBAVREF1 4. 2B 4. 3F<> 12CA SCL R 6. 1H> 8. 3A< PEX PLL EN PEX TX15 2. 5E SNN RSVD1 8. 3E DACB_VREF FBAVREF2 4. 2F 4. 3F<> I 2CA_SDA PEX_RST PEX_TX15* 2. 5E SNN_RSVD2 DVI A HPD 8. 2A> 9. 3H< FBAVREF3 4. 2D I 2CA SDA R 6. 1H<> 8. 3A<> PEX RXO 2. 2E PEX TX15 C 2.5C SNN RSVD3 8. 3E PEX_RXO* PEX_TX15_C* DVI _B_HPD 8. 2A> 9. 3H< I 2CB_SCL FBACLK CO 3. 3G FBA_A<0> 3.3D 4.1A 4.1C 4.1F L2CB SCL R 6. 3H> 8. 2A< PFX RX1 2. 2E PLI VDD SPDLE MXM 8.4C FBACLK_C1 I 2CB_SDA PEX_RX1* PRSNT2_C FBAD<0> 3.1C 4.4B FBA A<12..0> 3. 3E> 4. 4F< 12CB SDA R 6. 3H<> 8. 2A<> PEX RX2 2. 2E RAMCFGO 10. 1D> 14. 1C 14. 2A: SS OUT 11. 2C 4. 1A< 4. 1C 4. 1E 4. 1G FBAD<63..0 PEX_RX2* 2. 2E 10. 1D> 14. 2A> 14. 2C RAMCFG1 SS_REF FBA A<13...0: 8. 4A< 9. 2A< 9. 3H FBAD<1> 3.1C 4.4B 4. 1A< 4. 1C 4. 1F 4. 1G I 2CC_SCL_R PFX RX3 2. 3F RAMCEG2 10. 1D> 14. 2A> 14. 20 SWAPRDY A 10.4C FBAD<2> FBA_A<1> 3. 3D 4. 1A 4. 1C 4. 1E PEX_RX3* RAMCFG3 10. 1D> 14. 2A> 14. 2C TESTMODE FBAD<3> 3.1C 4.4B 4.1G 12CC SDA 9. 3D PEX RX4 2. 3E REFCLK 2. 2E THERM 9.3C 3. 3D 4. 1A 4. 1C I 2CC_SDA_R PEX_RX4* REFCLK* 2. 2E FBAD<5> 3.1C 4.4B FBA_A<3> 3. 3D 4. 1A 4. 1C 11. 2B<> PEX_RX5 2. 3E ROMCS* 10. 3C 10. 3E THERM_ALERT* 8. 4A< 9. 2H FBA_A<4> 3. 3D 4. 1A 4. 1C I 2CH_SCL PEX_RX5* ROM_SCLK THERM_SCL FBAD<7> 3.1C 4.4B FBA A<5> 3.3D 4.1A 4.1C L2CH SDA 10.4C PFX RX6 2. 3E ROM SI 10.4C 10.4F THERM SDA 9. 20 FBA_A<6> I 2CS_SCL PEX_RX6* ROM_SO THERM_VDD FBAD<9> 3.1C 4.4C 12CS SDA 9.4C PEX RX7 2. 3E RUNPWROK 7. 5A< 8. 4A> 11. 2B TMDSI OVDD AB EN* 7. 3B FBA_A<7> 3. 3D 4. 1A 4. 1C 4. 1E I FPABPLLVDD PEX_RX7* TMDSI OVDD_C 12. 3A< 13. 2B< FBAD<11> 3.10.4.40 LEPARRSET 7. 2F PFX RX8 2.4F RUNPWROK I N 8. 4B TMDSLOVDD C FN* 7. 4B FBA_A<8> 3. 3D 4. 1A 4. 1C 4. 1E FBAD<12> 3.1C 4.4C I FPABVPROB 7. 2E PEX_RX8* SMB_CLK TMDS_LVDS_I OVDD FBAD<13> 3.1C 4.4C I FPAI OVDD 7. 2E PEX RX9 2. 4E SMB DAT 8. 4A<> 9. 4B<> XTALI N 6. 4C 3. 3D 4. 1A 4. 1C 4. 1E PEX_RX9* XTALOUT FBA_A<9> I FPATXO SNN_5V_CLAMF 9. 3D FBAD<15> 3.1C 4.4C I FPATXC* 7. 3H> 8. 4G< PEX_RX10 2. 4E SNN_A2_M1 4. 2A XTALOUTBUFF 6. 4F> 11. 2B< FBA_A<10> 3. 3D 4. 1A 4. 1C 4. 1E I FPATXDO 7. 2H> 8. 4G< PEX_RX10 SNN_A2_M2 FBAD<17> 3.1C 4.4D I FPATXDO 7. 2H> 8. 4G< PEX RX11 2. 4E SNN A2 M3 4. 2E FBA_A<11> 3. 3D 4. 1A 4. 1C 4. 1E I FPATXD1 PEX_RX11* SNN_A2_M4 4. 2G FBAD<18> FBAD<19> 3. 2C 4. 4D 4. 2G I FPATXD1 7. 2H> 8. 4G< PEX RX12 2. 4E SNN BUFRST* 10.4C FBA_A<12> 3. 3D 4. 1A 4. 1C 4. 1E I FPATXD2 PEX_RX12* SNN_DACB_CSYNC 6. 3D FBAD<21> 3. 2C 4. 4D LEPATXD2 7. 2H> 8. 4G+ PFX RX13 2. 5F SNN DACB HSYNC 6. 3D FBAD<22> FBA_BA0 3. 3E> 4. 2A< 4. 2C 4. 2E I FPATXD3 PEX_RX13* SNN_DACB_VSYNC FBAD<23> 3. 2C 4. 4D 4. 2G 4. 4F< I FPATXD3* 7. 2H> 8. 4G< PEX RX14 2. 5E SNN DVI B CLK 8. 3E SNN_DVI_B_CLK FBAD<24> 3. 2C 4. 4D FBA_BA1 PEX_RX14* 8. 3E FBAD<25> 3. 2C 4. 4D 4. 2G 4. 4F< I FPBTXC* 7. 3H> 8. 4G< PEX_RX15 2. 5E SNN_DVI_B_TXO 8. 2E FBA_BA2 3. 3E> 4. 2A< 4. 2C 4. 2E I FPBTXD4 PEX_RX15* SNN_DVI _B_TX0 FBAD<27> 3. 2C 4. 4D 4. 2G 4. 4F< I FPBTXD4 7. 2H> 8. 3G< PEX TSTCLK 2. 2E SNN DVI B TX1 8. 2E FBA_CAS* 3. 3E> 4. 1A< 4. 1C 4. 1E PEX_TSTCLK* 2. 2E SNN_DVI _B_TX1 FBAD<28 3.2C 4.4D I FPBTXD5 7. 2H> 8. 4G< 8. 2E FBAD<29> 3. 2C 4. 4D 4. 1G 4. 5F< I FPBTXD5 7. 2H> 8. 4G< PEX TXO 2. 2E SNN DVI B TX2 8. 2E FBA_CKE 3. 3E> 4. 2A< 4. 2C 4. 2E I FPBTXD6 PEX_TX0* SNN_DVI _B_TX2 8. 2E 3.2C 4.4D FBAD<31> 3. 2C. 4. 4D 4. 2G 4. 3G 4. 4F< LEPRTXD6* 7. 2H> 8. 4G+ PEX TXO C 2.20 SNN F2 M1 4. 2A FBAD<32> FBA_CLKO I FPBTXD7 PEX_TXO_C* SNN_E2_M2 FBAD<33> 3, 2C 4, 4B 4. 4F< I FPBTXD7 7. 3H> 8. 4G< PEX TX1 2. 2E SNN E2 M3 4. 2E 3. 3H 3. 4E> 4. 2A< 4. 2C PEX_TX1* FBAD<34 3. 2C 4. 4B FBA_CLKO* I FPCBRSET SNN_E2_M4 4. 2G FBAD<35> 3. 2C 4. 5B 4.4F< I FPCPLLVDD 7.4E PEX_TX1_C 2. 2C SNN_FBA_A13 3. 3D FBA_CLK1 3. 4E> 3. 4G 4. 2E< 4. 2G 3. 2C 4. 5B PEX_TX1_C* 2. 2C SNN_FBA_A14 FBAD<37> 3, 2C 4, 5B I FPCTXC* 7. 4H> 8. 2G< PEX TX2 2. 2E SNN FBA A15 3.4D 3. 4E> 3. 4H 4. 2E< 4. 2G I FPCTXDO PEX_TX2* SNN_FB_VREF FBA_CLK1* FBAD<39> 3.2C 4.5B 4.4F< I FPCTXDO* 7. 3H> 8. 2G< PEX_TX2_C 2.20 SNN_GPI 07 9. 3D 3. 3E> 4. 1A< 4. 1C 4. 1E FBAD<40: 3. 2C 4. 4C FBA_CSO* I FPCTXD1 PEX_TX2_C* 2. 2C SNN_GPI 010 9. 3D FBAD<41> 3, 20, 4, 40 4. 1G 4. 5F< LEPCTXD1 7. 4H> 8. 2G+ PEX TX3 2. 2F SNN GPI 011 9. 3D FBAD<42> FBA_CS1* I FPCTXD2 PEX_TX3* SNN_GPI 013 3. 4D 4. 5F< FBAD<43> 3. 2C 4. 5C FBA DEBUG I FPCTXD2* 7. 4H> 8. 2G< PEX TX3 C 2. 2C SNN GPI 014 9. 4D FBAD<44> FBA_ODT 3. 4F> 4. 2A< 4. 2C 4. 2E I FPCVPROBE PEX_TX3_C* SNN_HDCP_ROM FBAD<45> 3. 2C 4. 5C 4. 2G< 4. 5F< I FPC_I OVDD 7.4E PEX_TX4 2. 3E SNN_I GP1 8. 3E FBA_ODT_GPL PEX_TX4* SNN_I GP2 3. 3E> 4. 1A< 4. 1C 4. 1E 8. 3G< 9. 3A< FBAD<47> 3. 2C 4. 5C FBA RAS* JTAG TCLK C PEX TX4 C 2. 3C SNN I GP159 8. 3E JTAG_TDI PEX_TX4_C* SNN_I GP185 8. 3E FBA_WE* FBAD<49> 3.3C 4.4D 3. 3E> 4. 1A< 4. 1C 4. 1E JTAG_TDI_C 8.3G> 9.3A< PEX_TX5 2. 3E SNN_I GP195 8. 3E FBAD<50> JTAG_TD0 PEX_TX5* SNN_I GP197 3. 3D 4. 1F 4. 1G 8.3G< 9.3A> FBAD<51> 3.3C 4.5D FBB A<2> JTAG TDO C PEX TX5 C 2.30 SNN LGP LVDS UTX1 8.3F FBAD<52> FBB_A<5..2: PEX_TX5_C* SNN_I GP_LVDS_U FBAD<53> 3.3C 4.5D 4.4F< JTAG TMS C 8. 3G< 9. 3A< PEX TX6 2. 3E SNN MI OAD<1> 11. 38 FBAD<54> FBB_A<3> 3. 3D 4. 1E 4. 1G JTAG_TRST PEX_TX6* SNN_MI OAD<2> 8.3G< 9.3A< FBAD<55> 3.3C 4.5D FBB_A<4> 3. 3D 4. 1E 4. 1G JTAG_TRST_C PEX_TX6_C 2. 3C SNN_MI OAD<3> 11. 3E FBAD<56 FBB_A<5> 3. 3D 4. 1E 4. 1G LVDSI OVDD_I SOL PEX_TX6_C* 2. 3C SNN_MI OAD<4> 11. 4E< 14. 3A> 14. 3C FBAD<57> 3.3C 4.4D FBCAL PD 3. 4D MI OAD<6> PEX TX7 2. 3E SNN MI OAD<5> 11. 3E MI OAD<8> PEX_TX7* FBAD<58> FBCAL_PU SNN_MI OAD<7> FBAD<59> 3.3C 4.5D FBCAL_TERM 3.4D MI OAD<9> 11. 4E< 14. 3A> 14. 3C PEX_TX7_C 2.3C SNN_MI OAD<10> 11. 4E FB_B00T MI OB_CLKI N PEX_TX7_C* SNN_MI OBD<2> FBAD<61> 3.3C 4.5D FB BOOTC 13. 4D MI OB HSYNC 10. 2D> 14. 3A> 14. 30 PEX TX8 2. 3E SNN MI OBD<3> 10.1C FBAD<62> FB_COMP 13.5C M_GPI 08_SLOWDOWN* PEX_TX8* SNN_MI OBD<4> FBAD<63> 3.3C 4.5D FB_COMP1 13.4C M THERM ALERT* 9. 2D PEX TX8 C 2. 3C SNN MI OBD<5> 10.1C FBADQM<0 FB_COMP2 NVCTLO_R PEX_TX8_C* SNN_MI OBD<6> FBADQM<7..0> 3. 3B> 4. 4A<> 4. 5F<: FB_DH 13. 3D NVCTL1_R 12.4C PEX_TX9 2. 4E SNN_MI OB_CAL_PD_VD 10. 2A NVIDIA CORPORATION 701 SAN TOMAS EXPRESSWAY SANTA CLARA CA 95050 LISA 600-10584-0002-100 NV_PN ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. 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