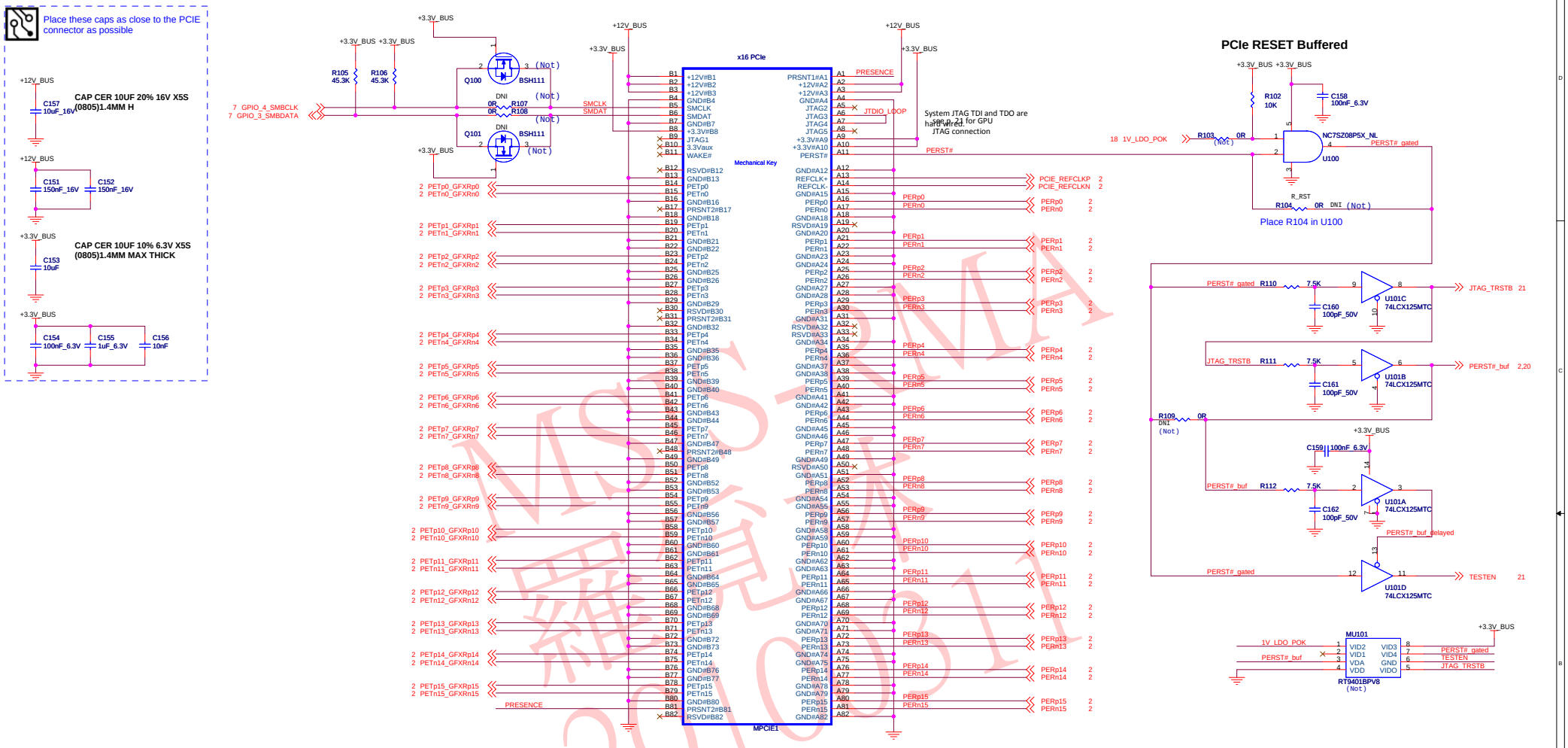
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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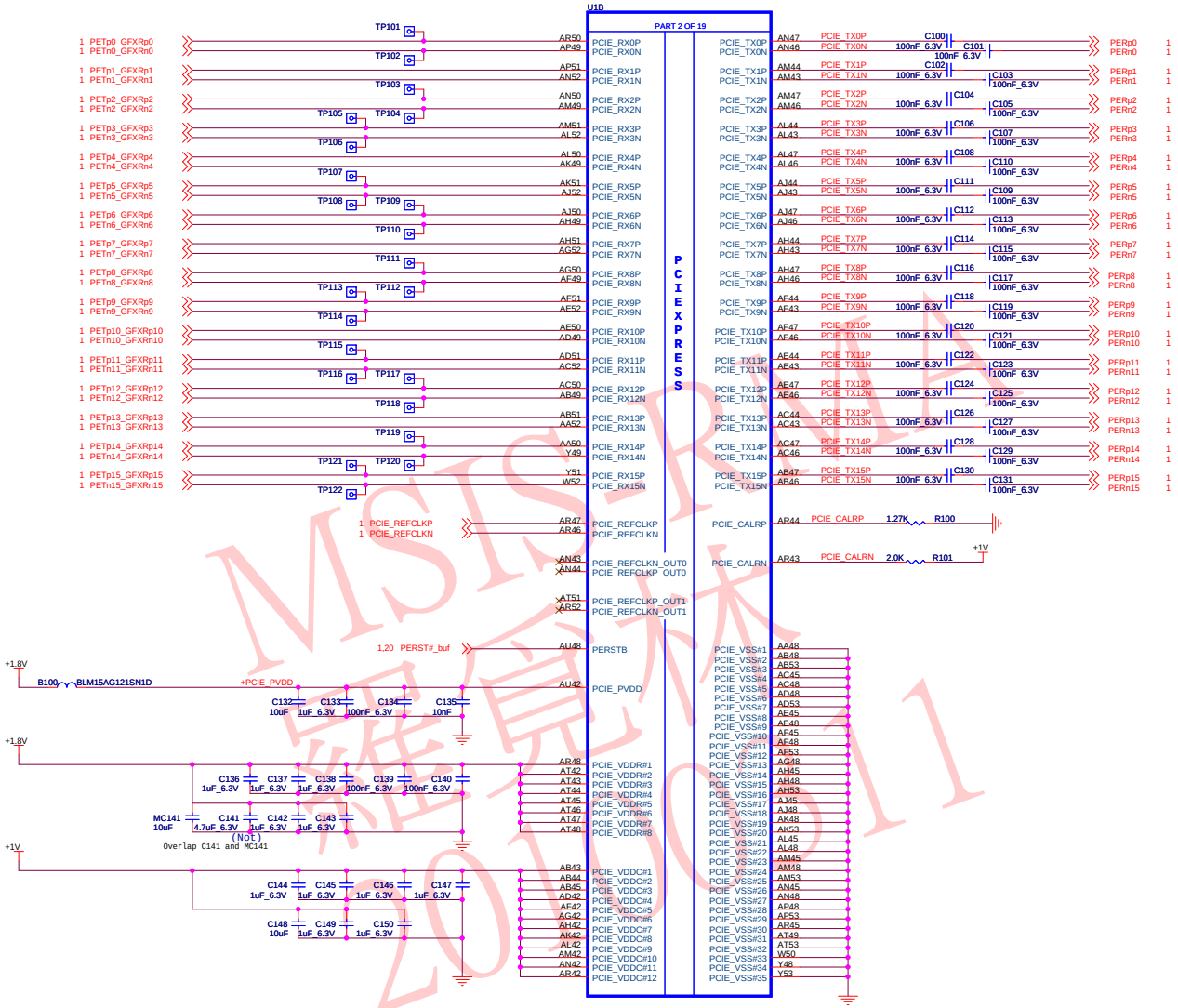
Title PCIE EDGE CONNECTOR Doc No. 105-C008XX-00B

(2) CYPRESS PCIE Interface

NOTE: Some of the PCIE testpoints will
be available through vias on traces.



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Title ASIC PCIE Interface

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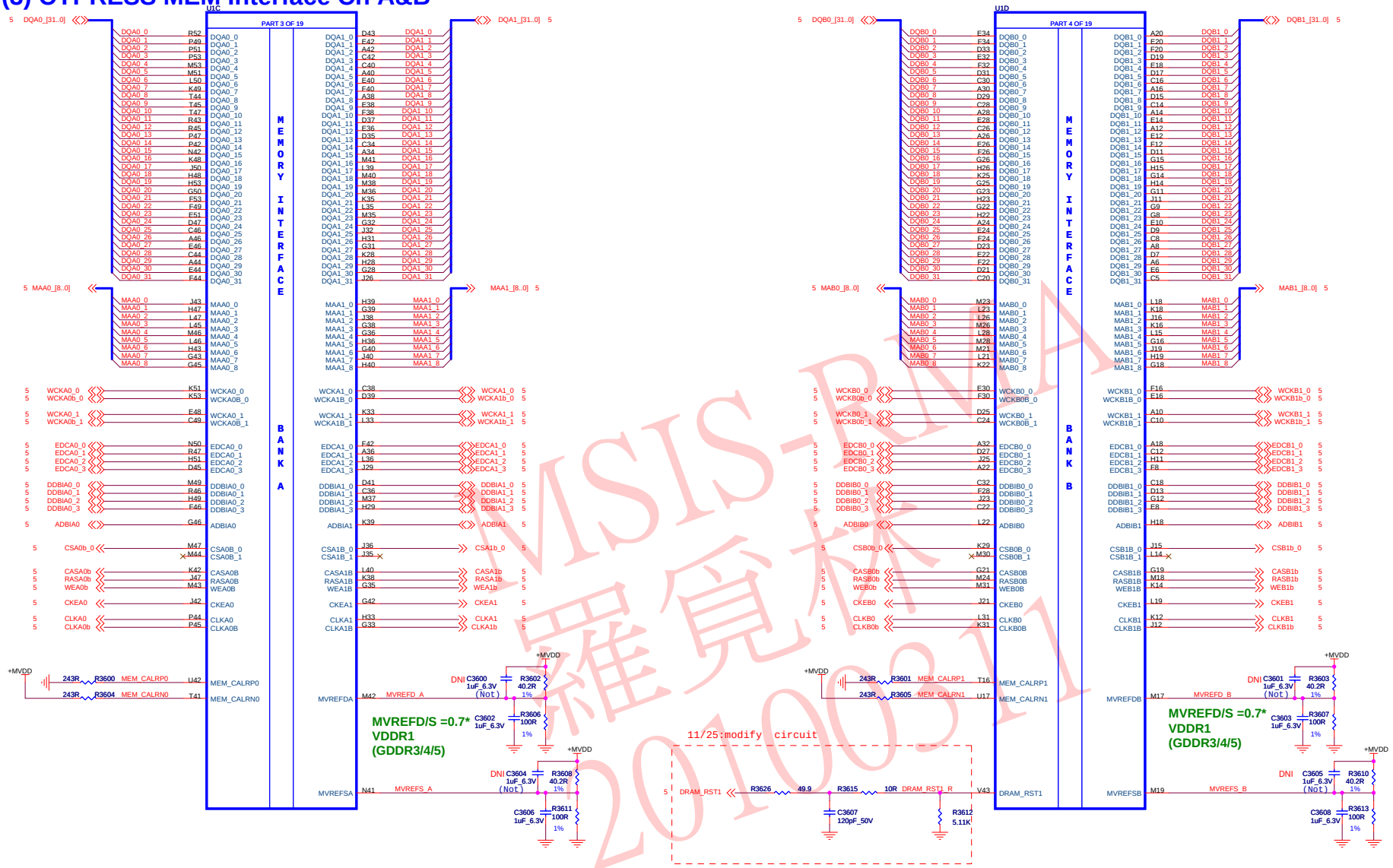
(3) CYPRESS MEM Interface Ch A&B



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Title ASIC Memory Ch A & B

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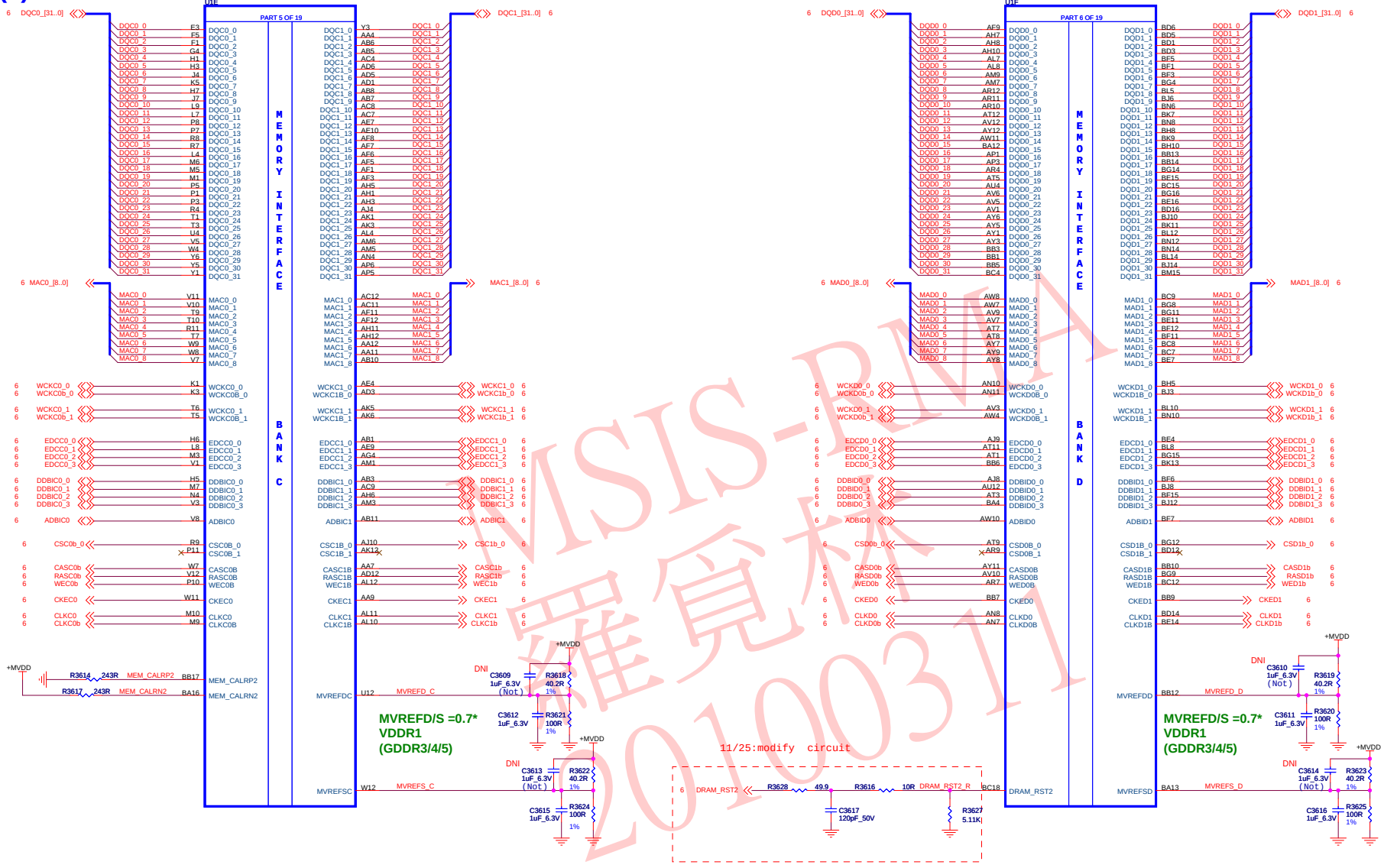
(4) CYPRESS MEM Interface Ch C&D



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Title ASIC Memory Ch C & D

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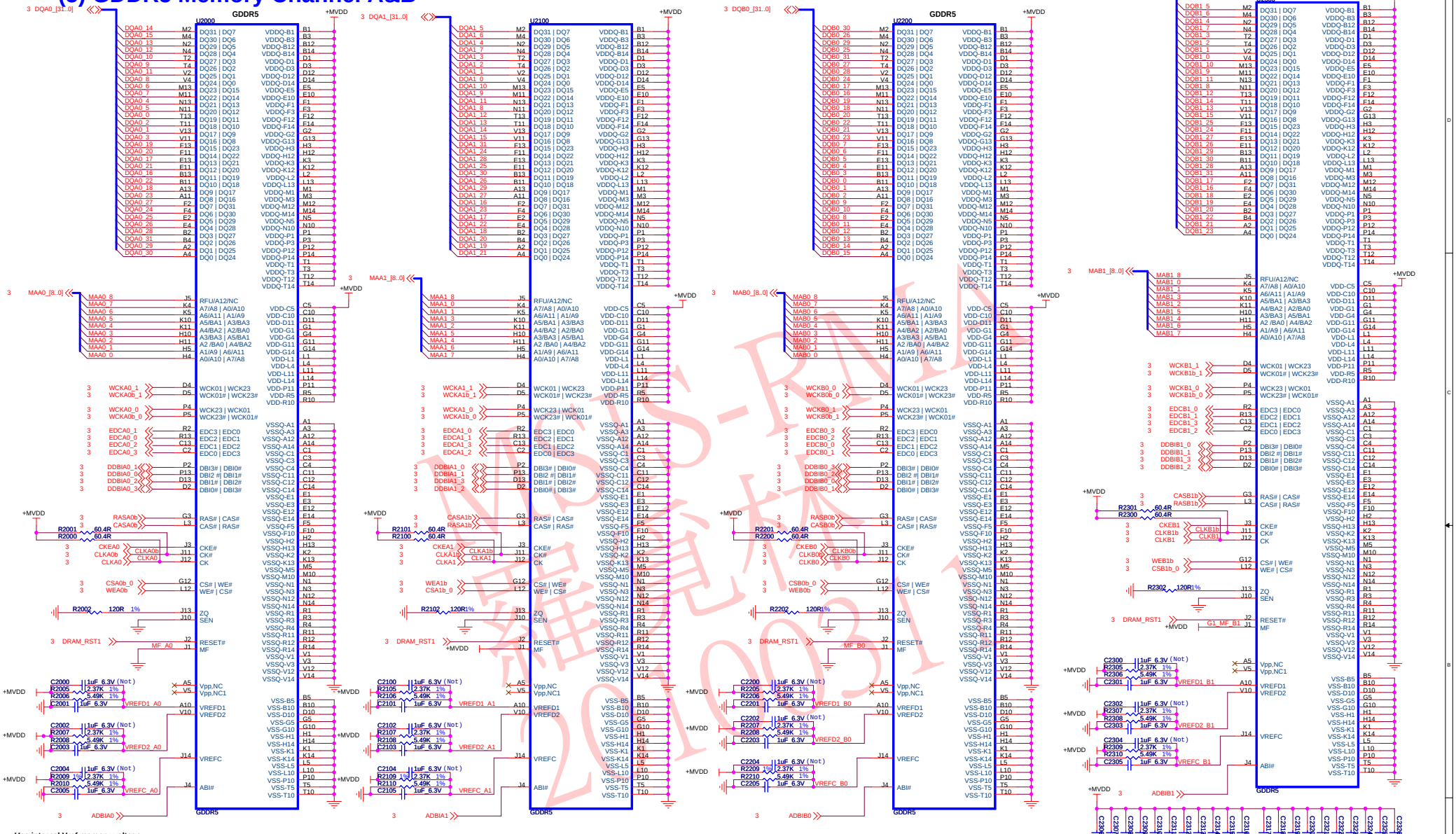
(5) GDDR5 Memory Channel A&B



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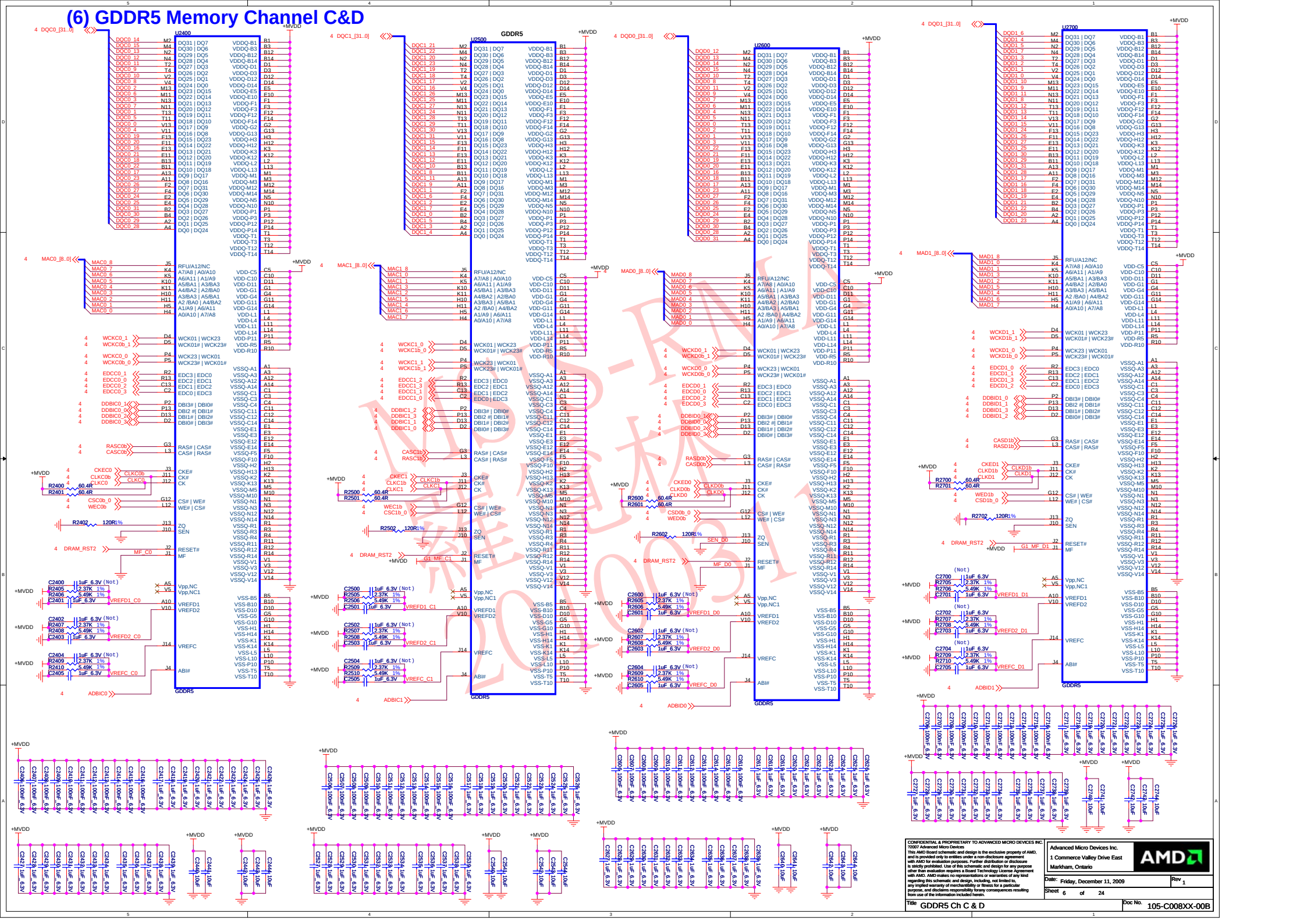
(6) GDDR5 Memory Channel C&D



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(07) Cypress GPIOs Strap CF XTAL OSC

PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

SCL / SDA BUS:

I2C Address	Function	Device
0xE0	VDDC REG	VT1165M
0xE2	VDDCI REG	VT1165M
0xA0	MVDDQ (debug)	UP6267
0xA2	MVDDC (debug)	UP6266

DDC6 BUS:

I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

PWRGOOD must be connected to GND for normal operation

CrossFire Card-Edge

Upper Cable Card Edge

Lower Cable Card Edge

Place the crossfire testpoints near the ASIC and not the connector

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

Overlap pads

11/23 add

Divider for 1.8V signaling.

route 50ohms single-ended/100ohms diff and keep short

10/15 add co-layout
12/5 remove R27 and C39

PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO(13,12,11) - CONFIG[2..0]

CONFIG[2]	100 - 512Kbit	M25P05A	(ST)
	101 - 1Mbit	M25P10A	(ST)
CONFIG[1]	101 - 2Mbit	M25P20	(ST)
	101 - 4Mbit	M25P40	(ST)
CONFIG[0]	101 - 8Mbit	M25P80	(ST)
	100 - 512Kbit	Pm25LV512	(Chingis)
	101 - 1Mbit	Pm25LV010	(Chingis)

VIP_DEVICE_STRAP_DIS
0:VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

RESERVED:
Internal use only. Other logic must not affect these signals during RESET.

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

TV OUT STANDARD 0 - PAL TVO 1 - NTSC TVO

RESERVED:
STRAP_BIOS_ROM_EN
CLKREQ# that requires open drain connection, and cannot be used as pinstrap
Don't set high at reset

Internal use only. Other logic must not affect these signals during RESET.

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Title ASIC GPIO, STRAPS,CF, and XTAL

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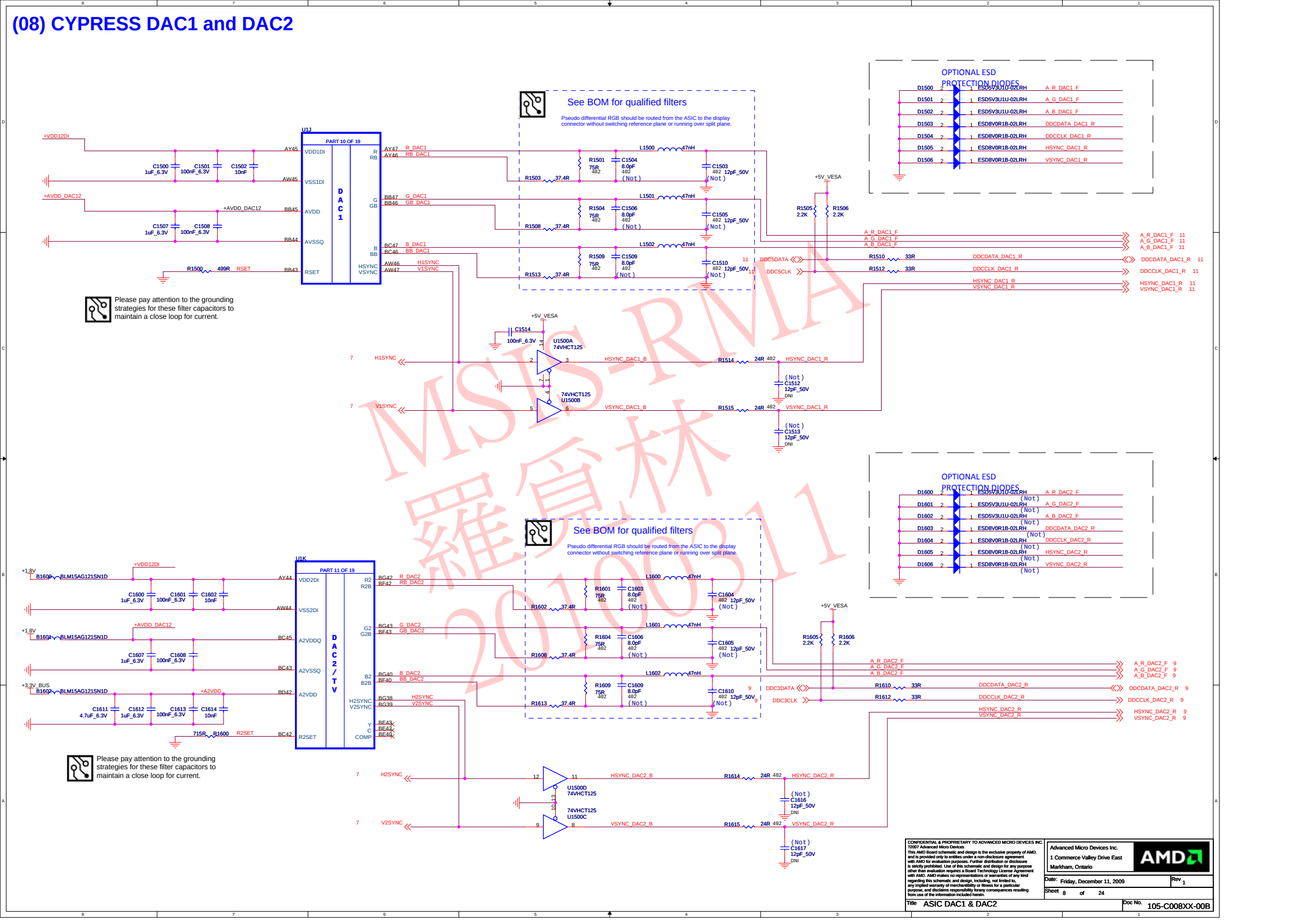
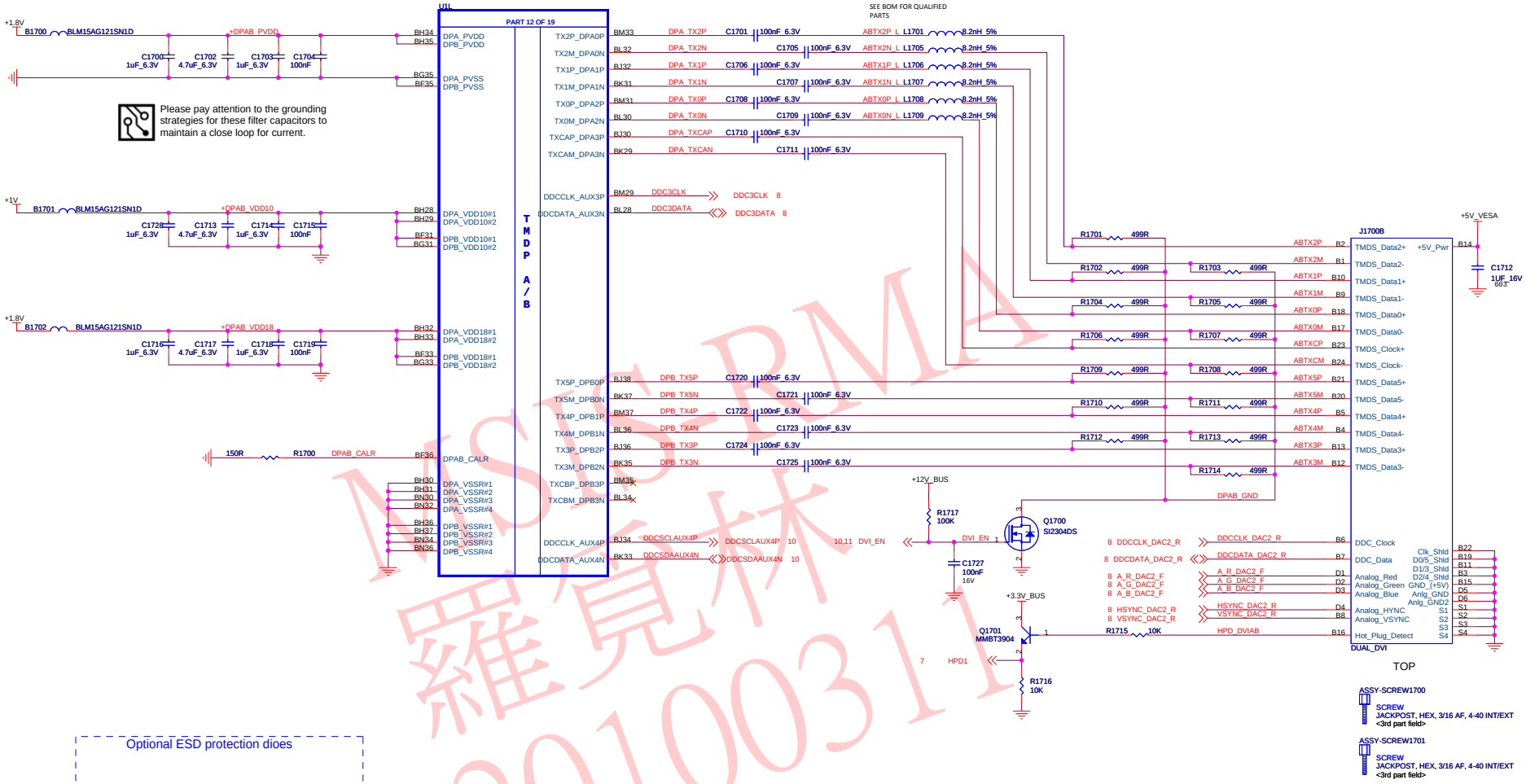
(08) CYPRESS DAC1 and DAC2



(09) CYPRESS TMDS A&B



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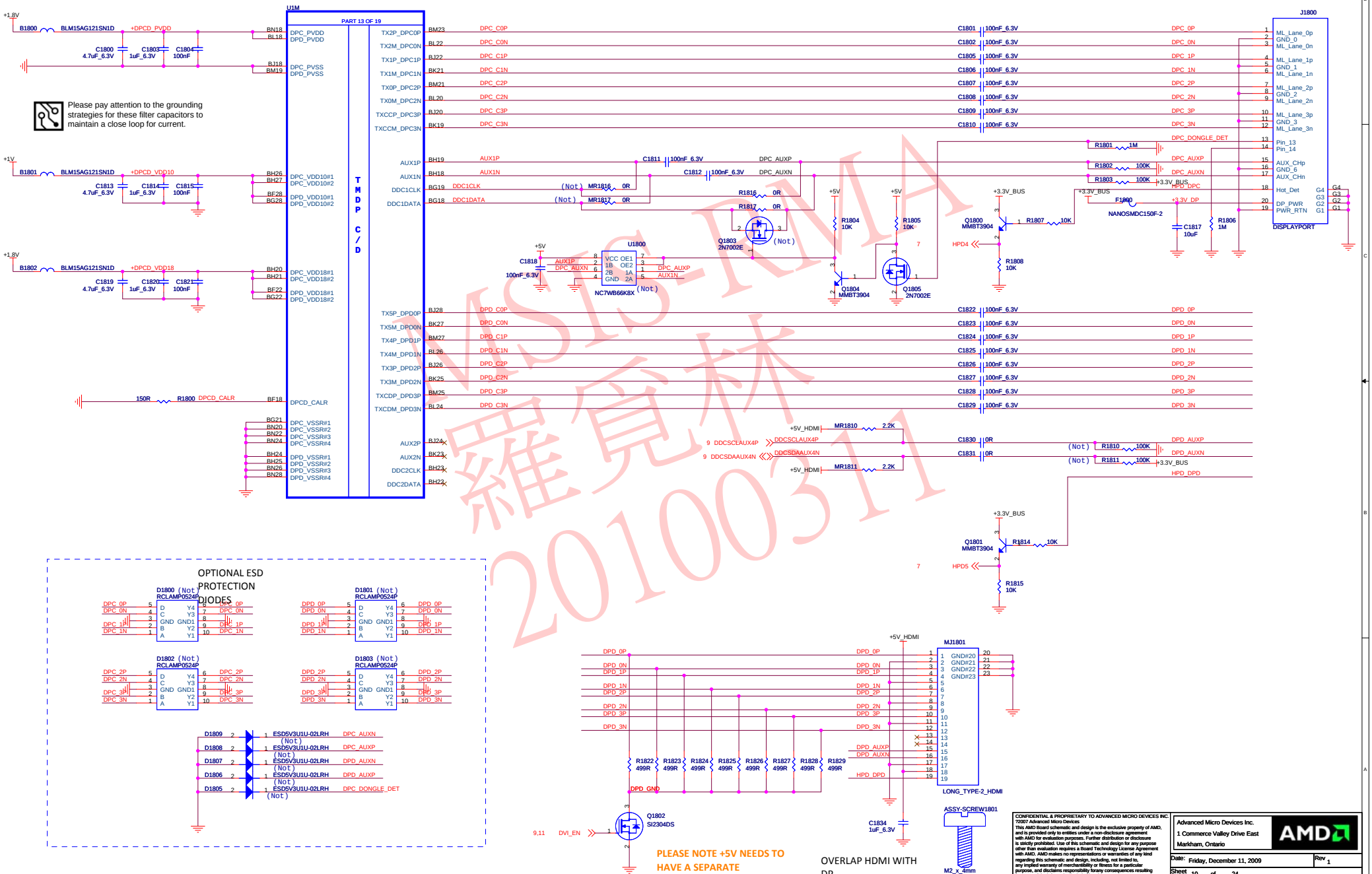
(10) CYPRESS Display Port/HDMI C&D



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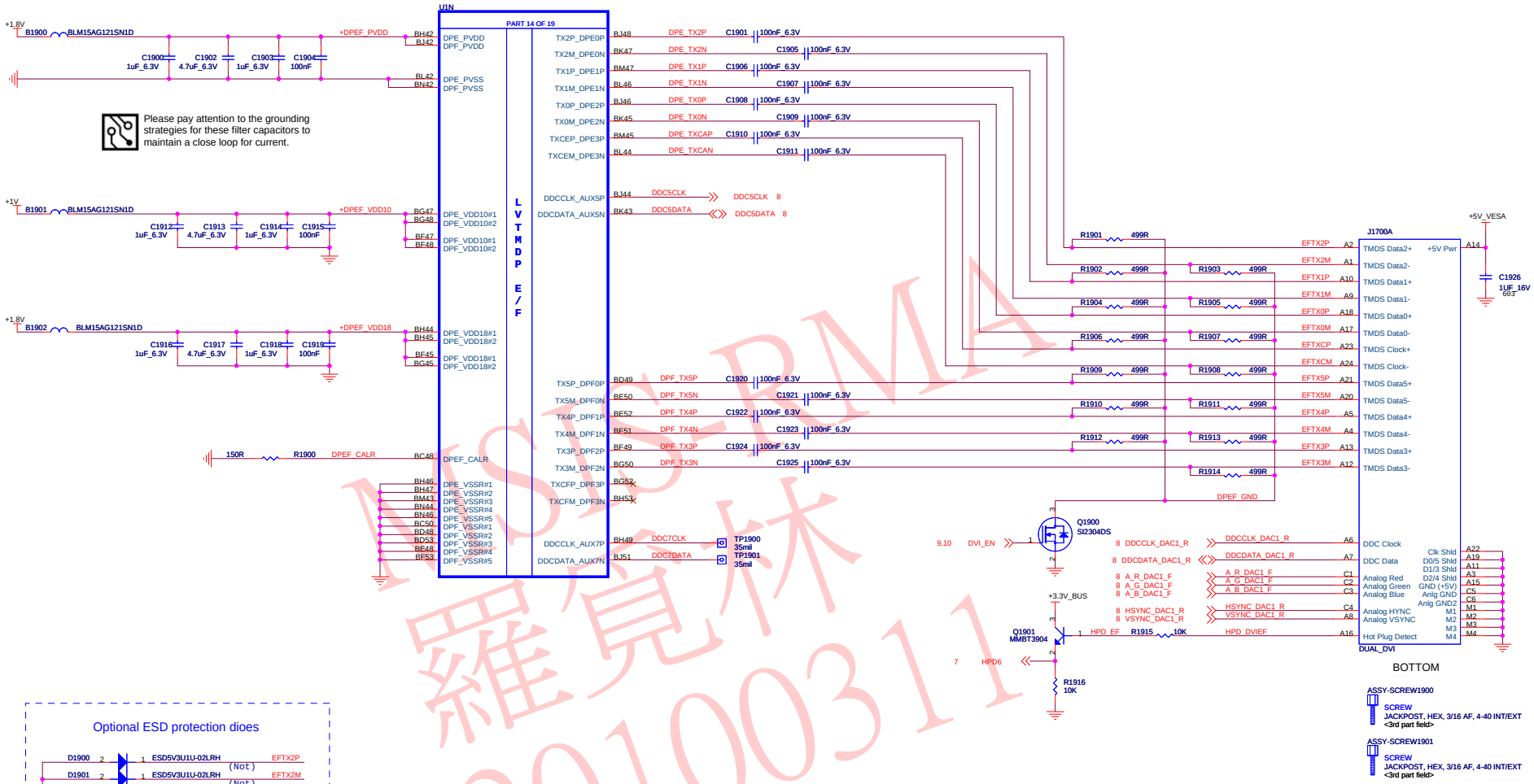
(11) CYPRESS LVTMDP E&F



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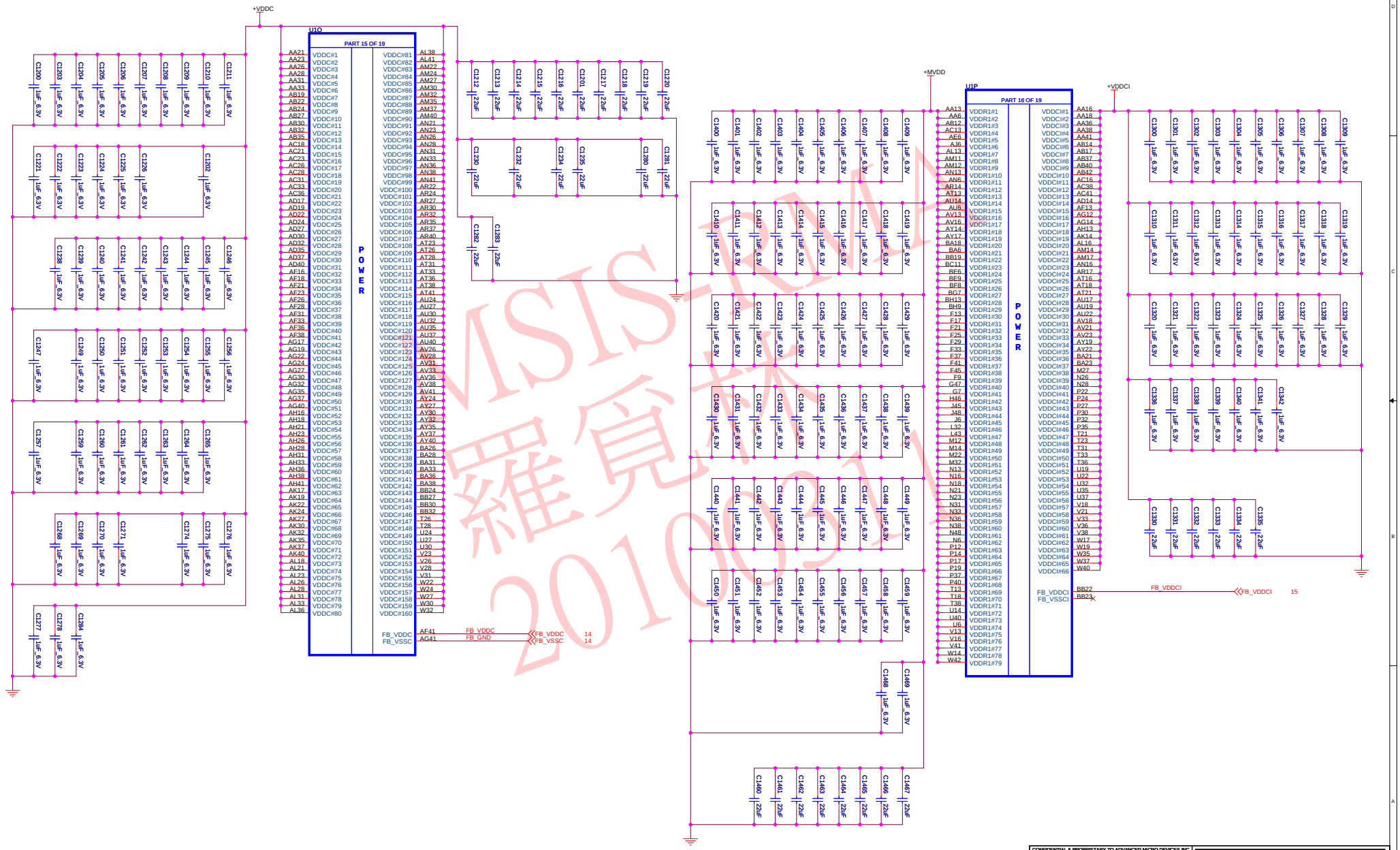
(12) CYPRESS Power



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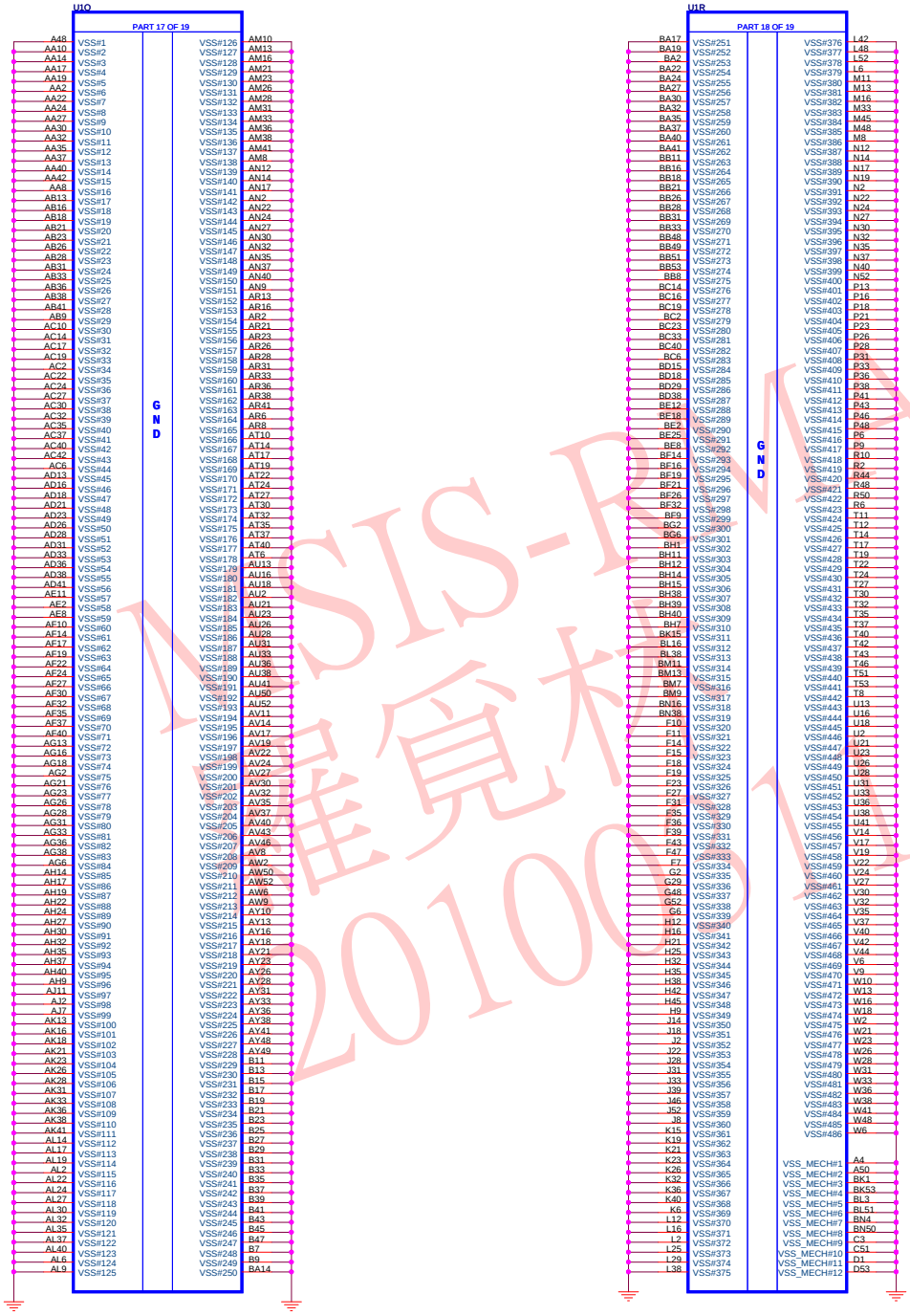
(13) CYPRESS GND



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Title ASIC GND

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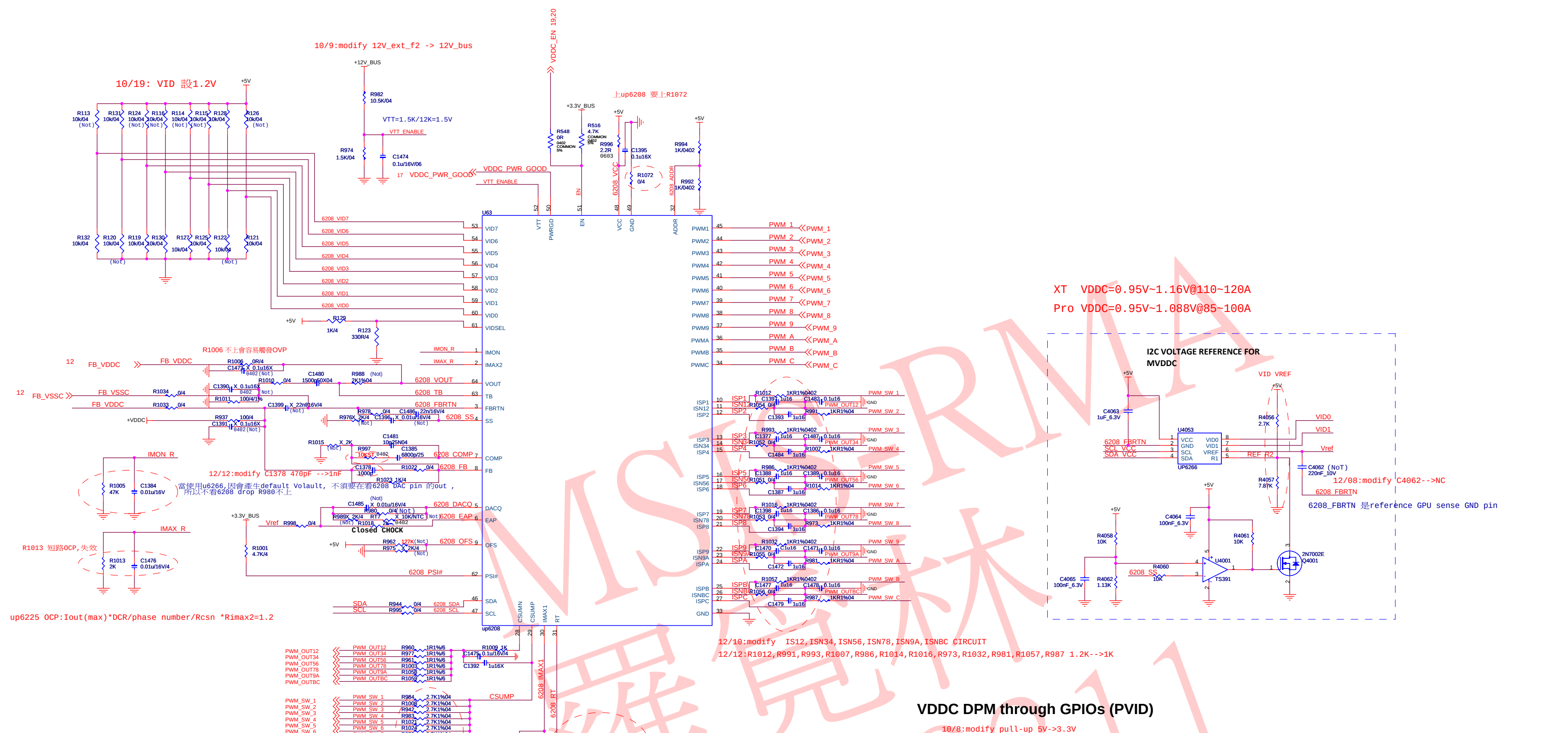
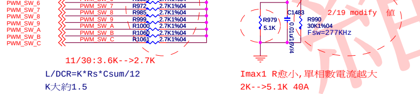
(14) VDDC

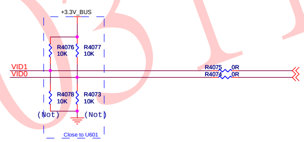
相數切換6208-->12phase 2,6,12
相數切換6208-->8phase 1,3,4
相數切換6225-->12phase 2,4,6,8,10,12(or 1,3,5,7,9,11)



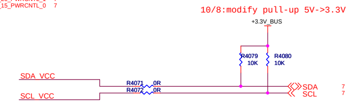


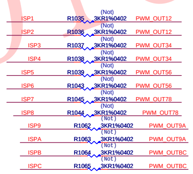
VDDC DPM through GPIOs (PVID)

10/8:modify pull-up 5V->3.3V



10/8:modify pull-up 5V->3.3V





11/20:modify

CYPRESS XT

State(SD)	VDDC	GPIO_15	GPIO_20
Boot-up	1.15V		
Low state	0.95V	1	1
Medium state	1.0625V	1	0
High state	1.125V	0	1
	1.175V	0	0

depends on leakage:1.125V for Hight leakage
1.175V for Low leakage

State(DD)	VDDC	GPIO_15	GPIO_20
Boot-up	1.15V		
Low state	0.95V		
Low/Medium state	1.0625V	1	0
High state	1.125V	0	1
	1.175V	0	0

depends on leakage:1.125V for Hight leakage
1.175V for Low leakage

CYPRESS Pro

State(DD)	VDDC	GPIO_15	GPIO_20
Boot-up	1.0V		
Low state	1.0V	0	0
Medium state	1.038V	0	1
High state	1.088V	1	0

State(SD)	VDDC	GPIO_15	GPIO_20
Boot-up	1.0V		
Low state	0.95V	1	1
Medium state	1.038V	0	1
High state	1.088V	1	0

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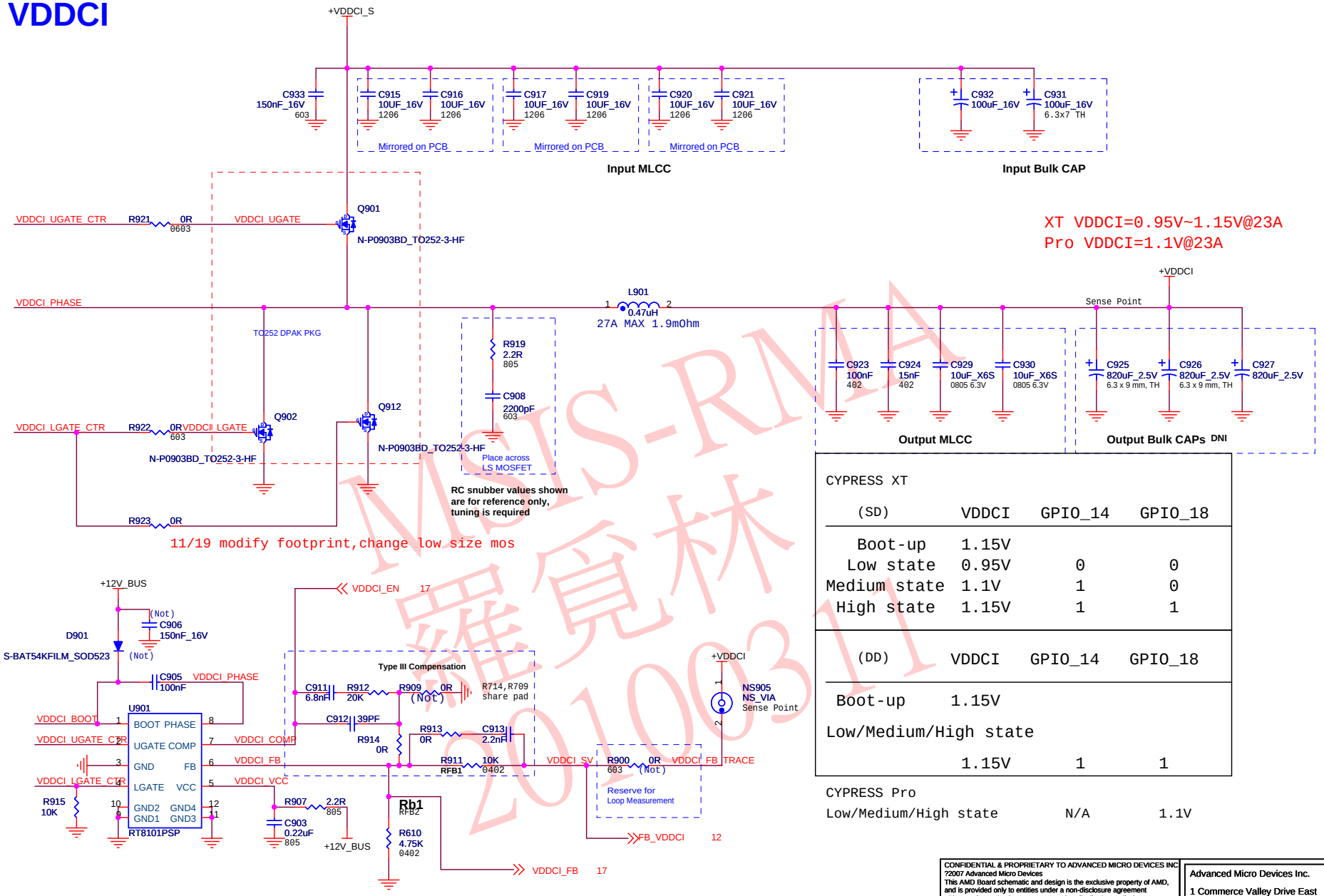
(15) VDDCI



CYPRESS XT (SD)	VDDCI	GPIO_14	GPIO_18
Boot-up	1.15V		
Low state	0.95V	0	0
Medium state	1.1V	1	0
High state	1.15V	1	1

(DD)	VDDCI	GPIO_14	GPIO_18
Boot-up	1.15V		
Low/Medium/High state	1.15V	1	1

CYPRESS Pro

Low/Medium/High state	N/A	1.1V	

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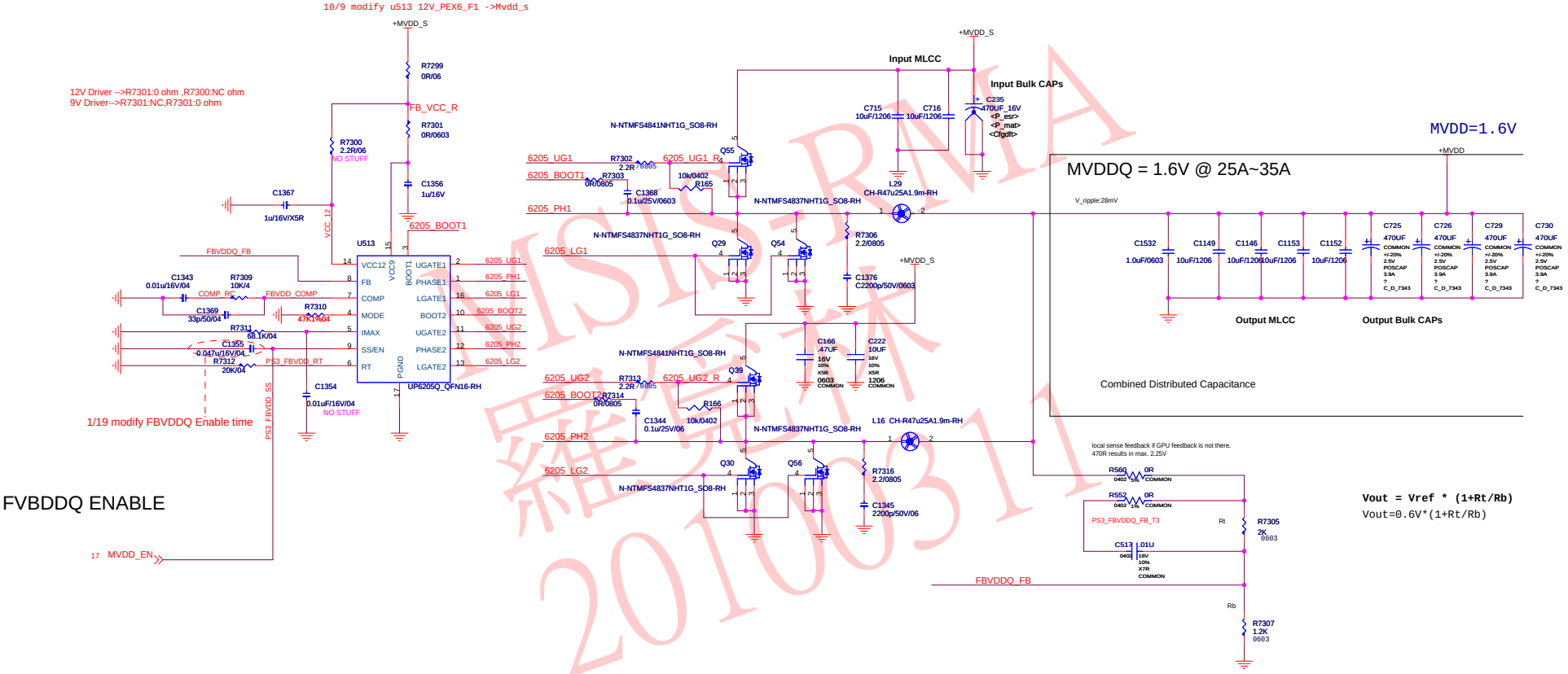
(16) MVDDQ



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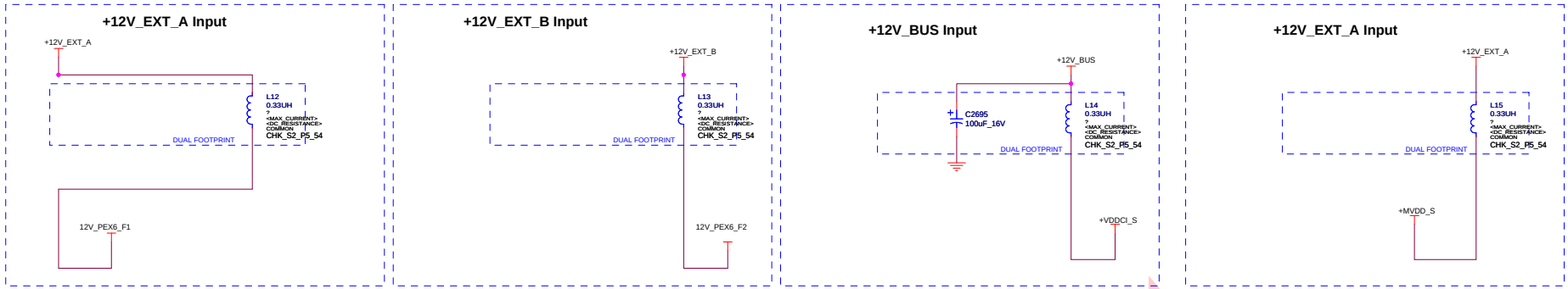
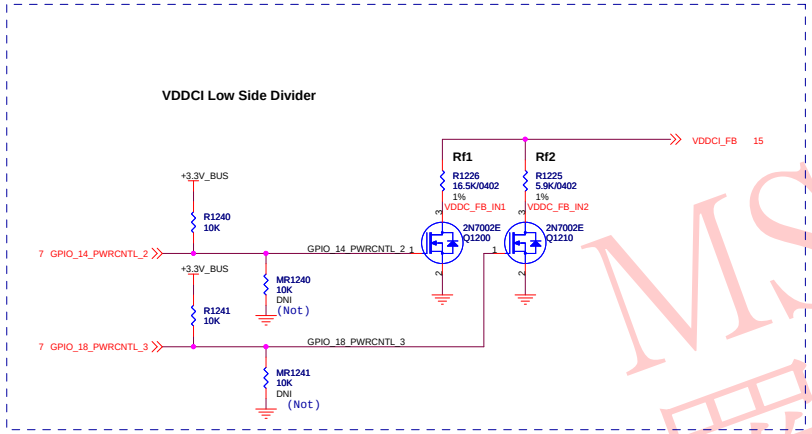
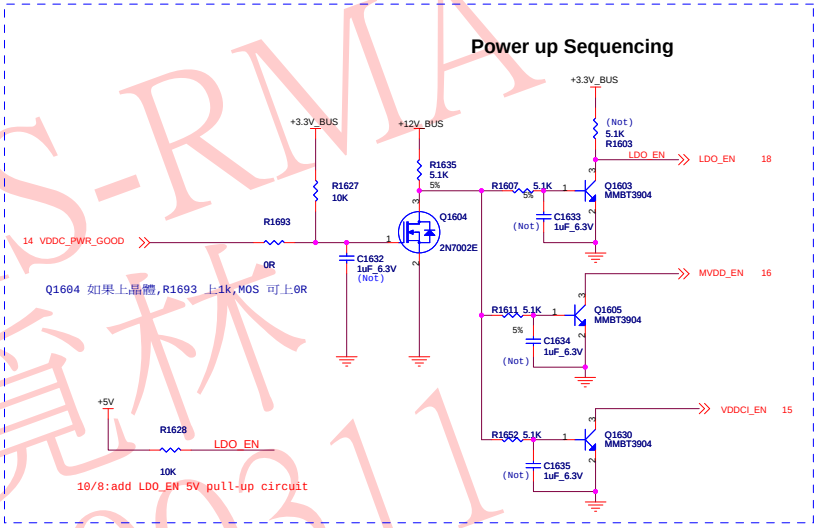
(17) CYPRESS VDDCI POWER PLAY







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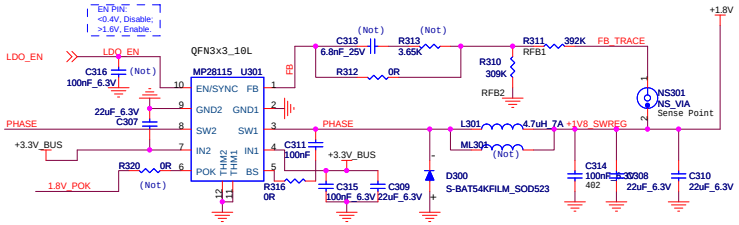
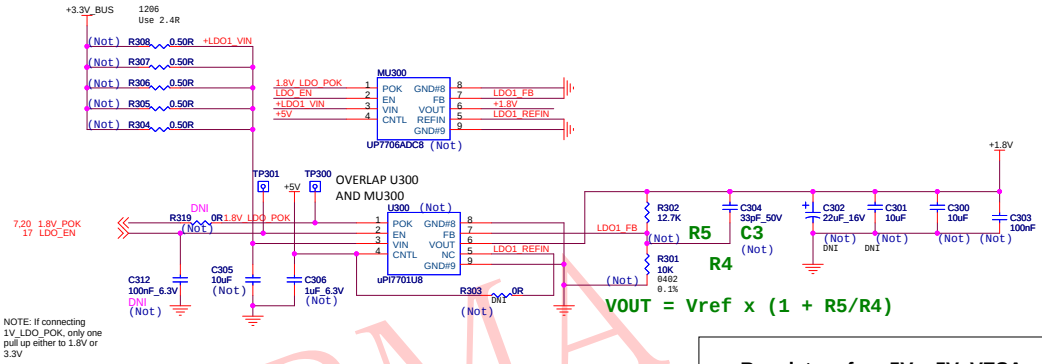
(18) CYPRESS Small Rail Regulators

LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

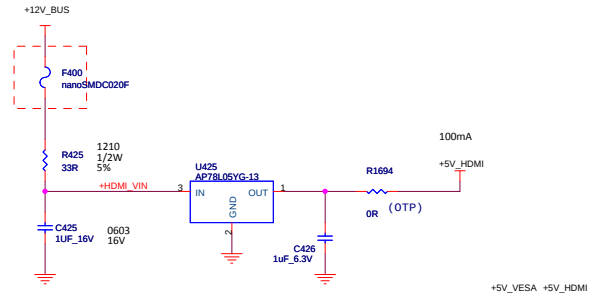


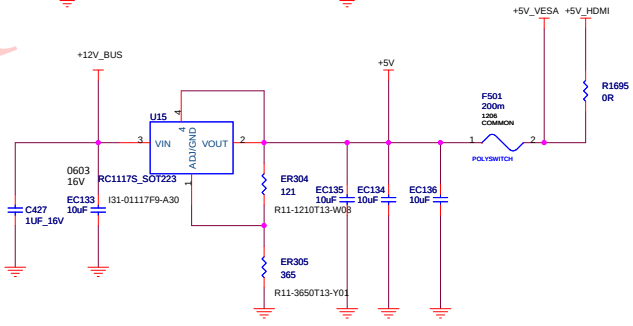


Regulators for +5V, +5V_VESA and +5V_HDMI

R450 << 15mA
R450+R451 << 30mA

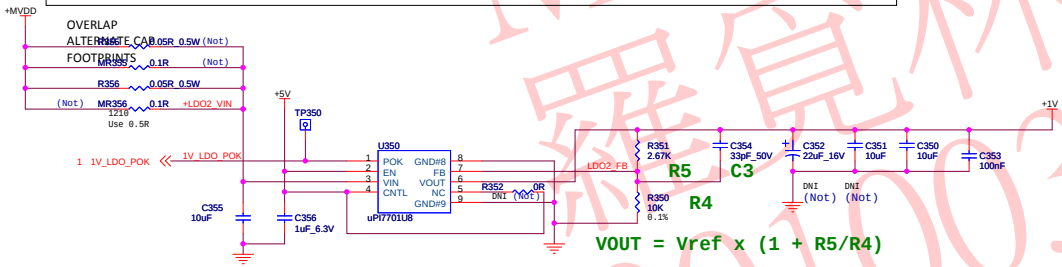
10/13 ADD 5V_hdmi circuit





Vout=1.25V* [1+(ER305/ER304)]

LDO #2: Vin = +1.35V to 1.8VMAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



optional 5V power for VDDC regulator;

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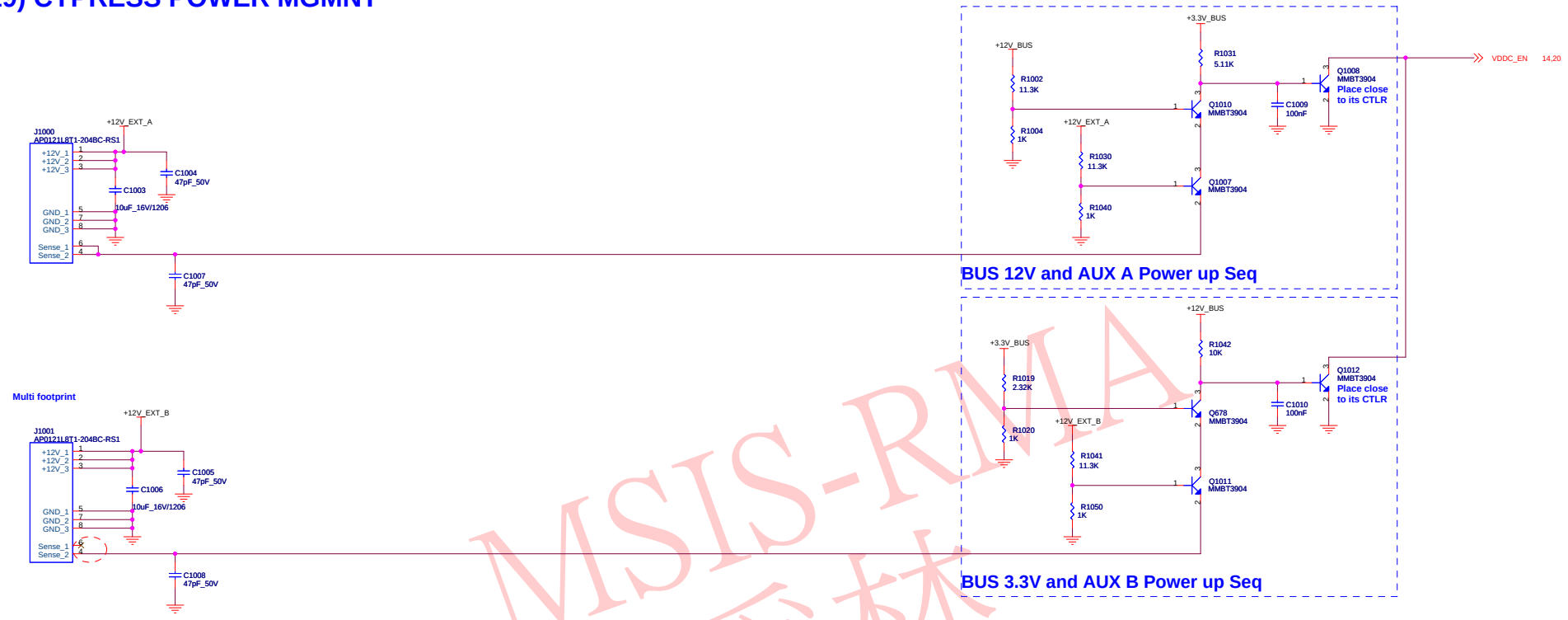
(19) CYPRESS POWER MGMNT



12/5 移除支援power compoent 6 pin

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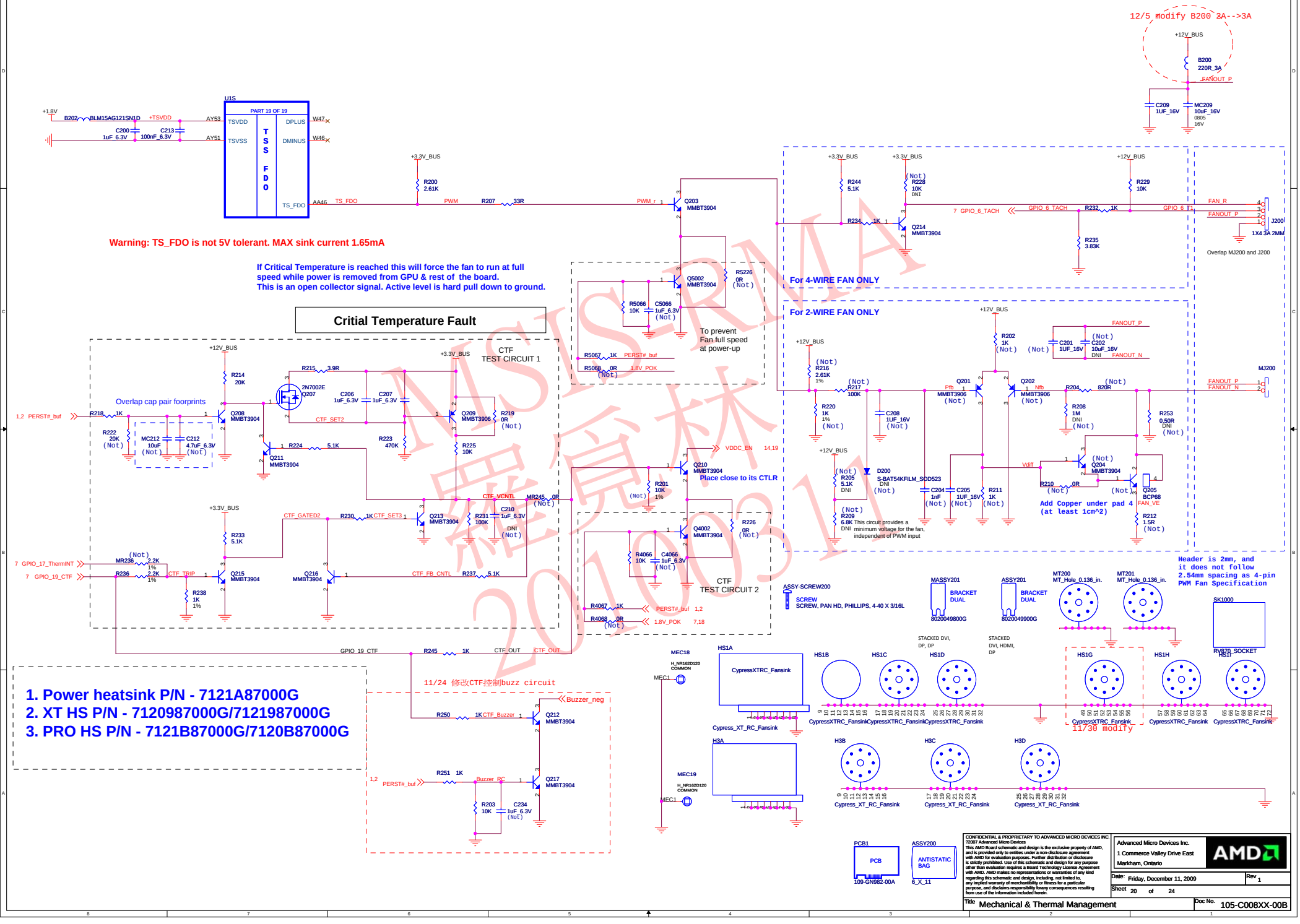
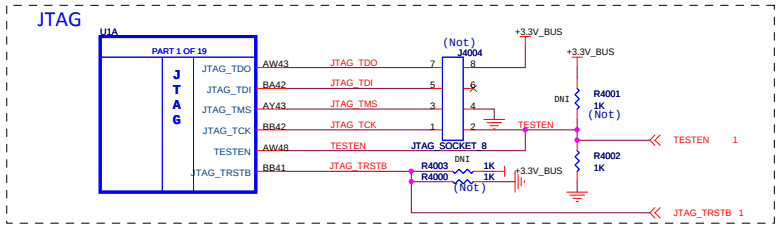
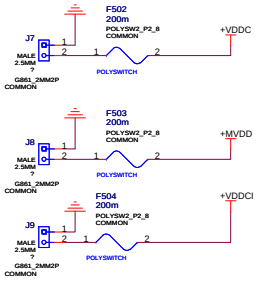
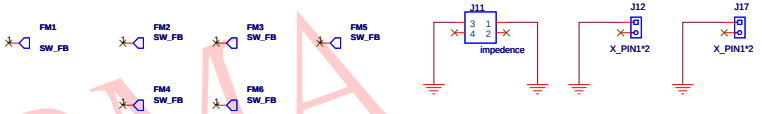
(20) CYPRESS Mechanical and Thermal Management

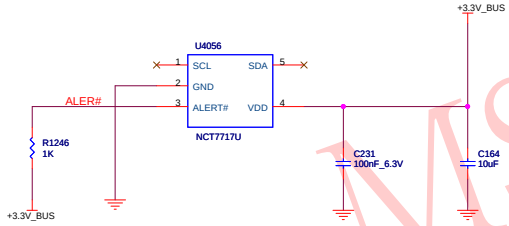


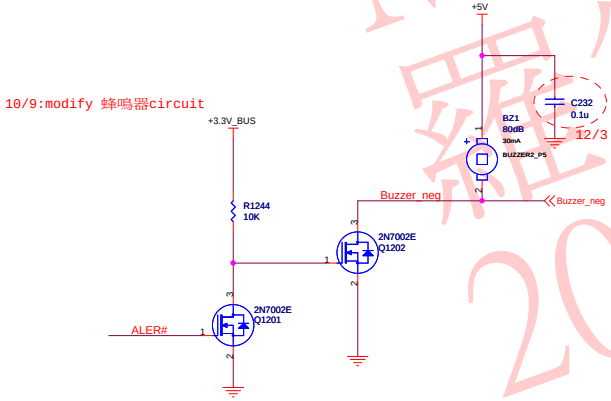
(21) CYPRESS Debug Circuits











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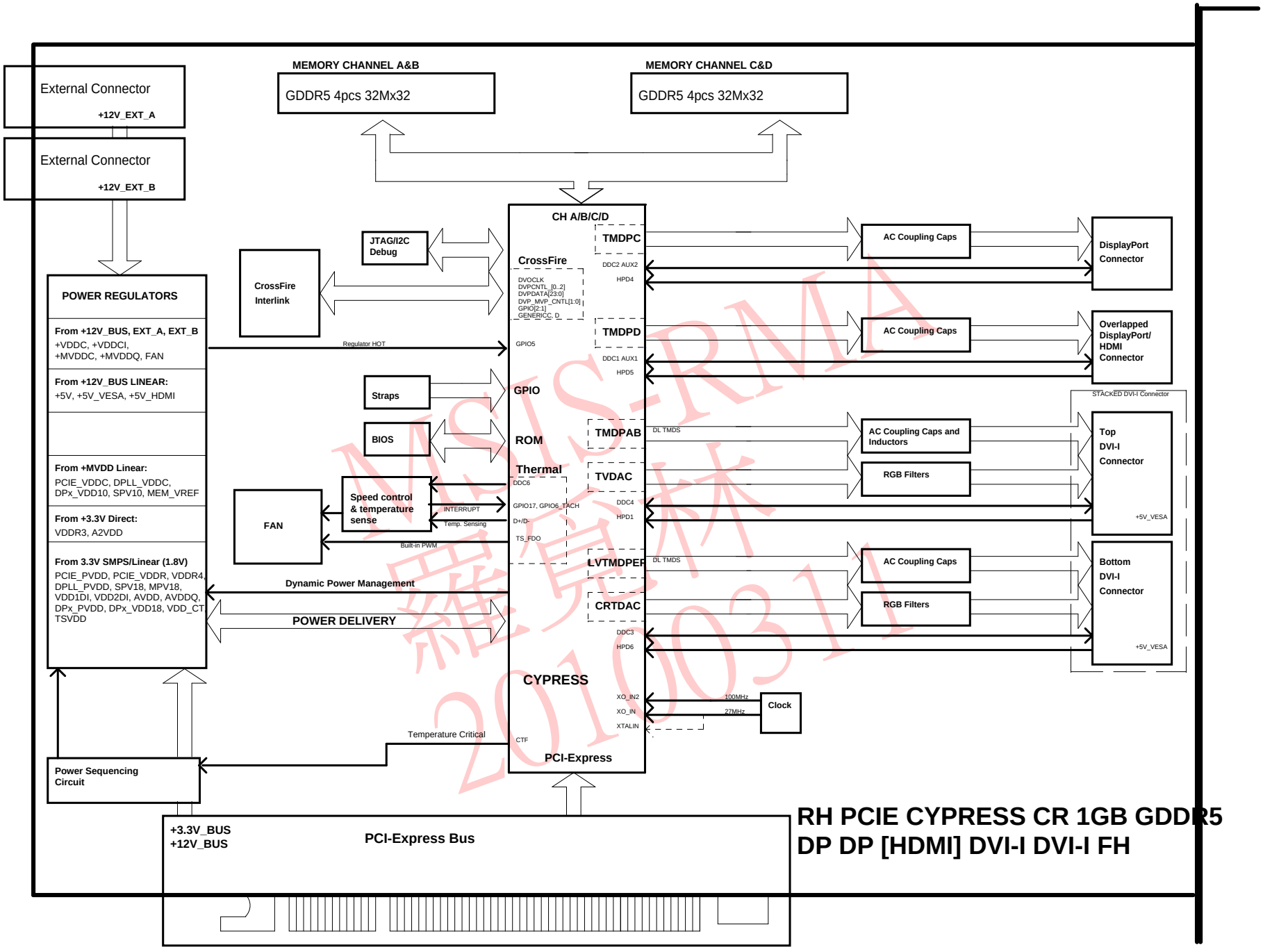

RH PCIE CYPRESS CR 1GB GDDR5
DP DP [HDMI] DVI-I DVI-I FH

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Markham, Ontario
Canada, L3T 7X6 (905) 882-2600

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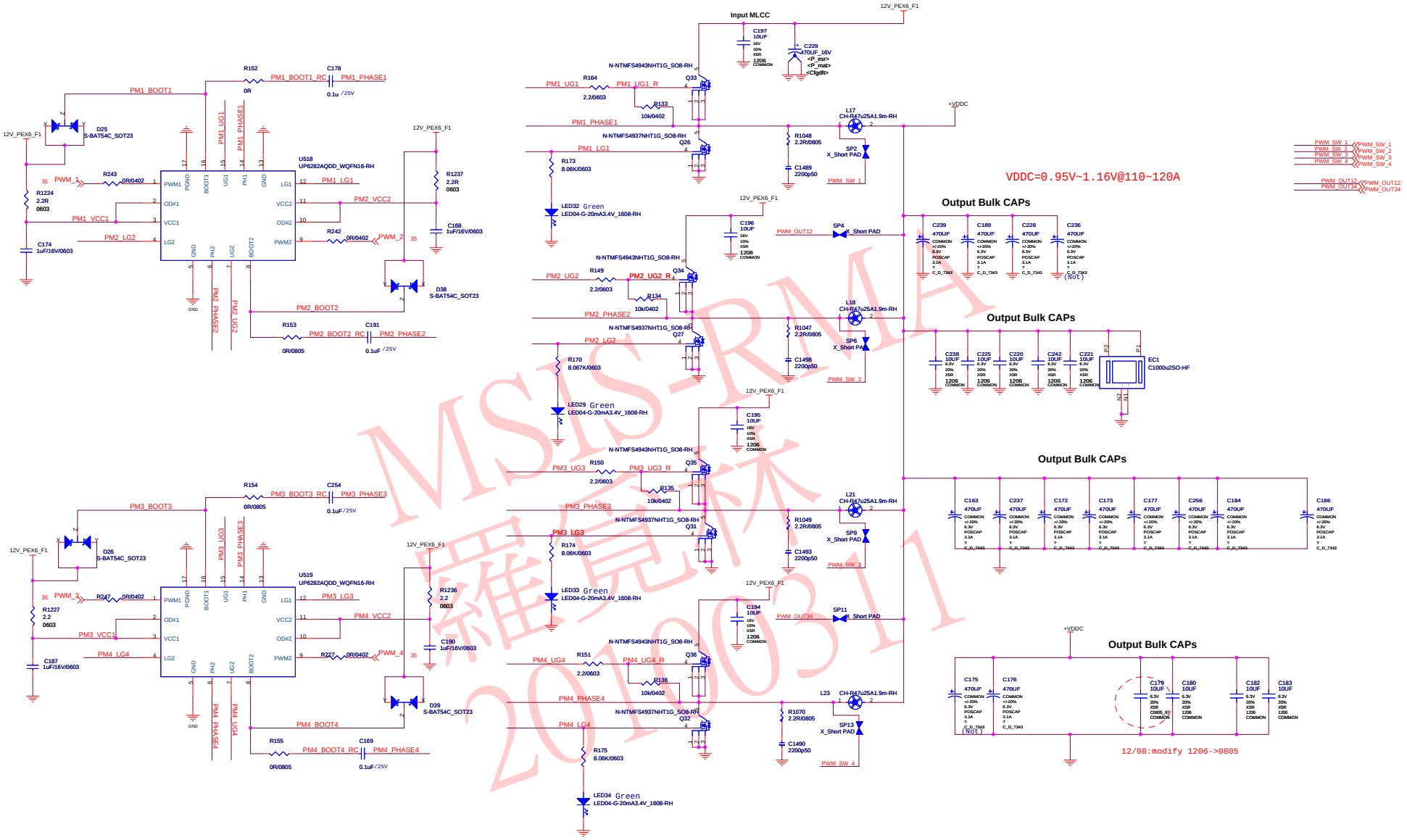
Title	Block Diagram
Doc No.	105-C008XX-00B

Power Supply: VDDC 1~4 Phase powered from external PEX 8PIN



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 1-2 of 4

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<Title>

Size: Custom | Document Number: <Doc> | Rev: <FevCode>

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Title	Schematic No.	Date:
RH CYPRESS GDDR5 DP-HDMI-DVII-DVII	105-C008XX-00B	Friday, December 11, 2009

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

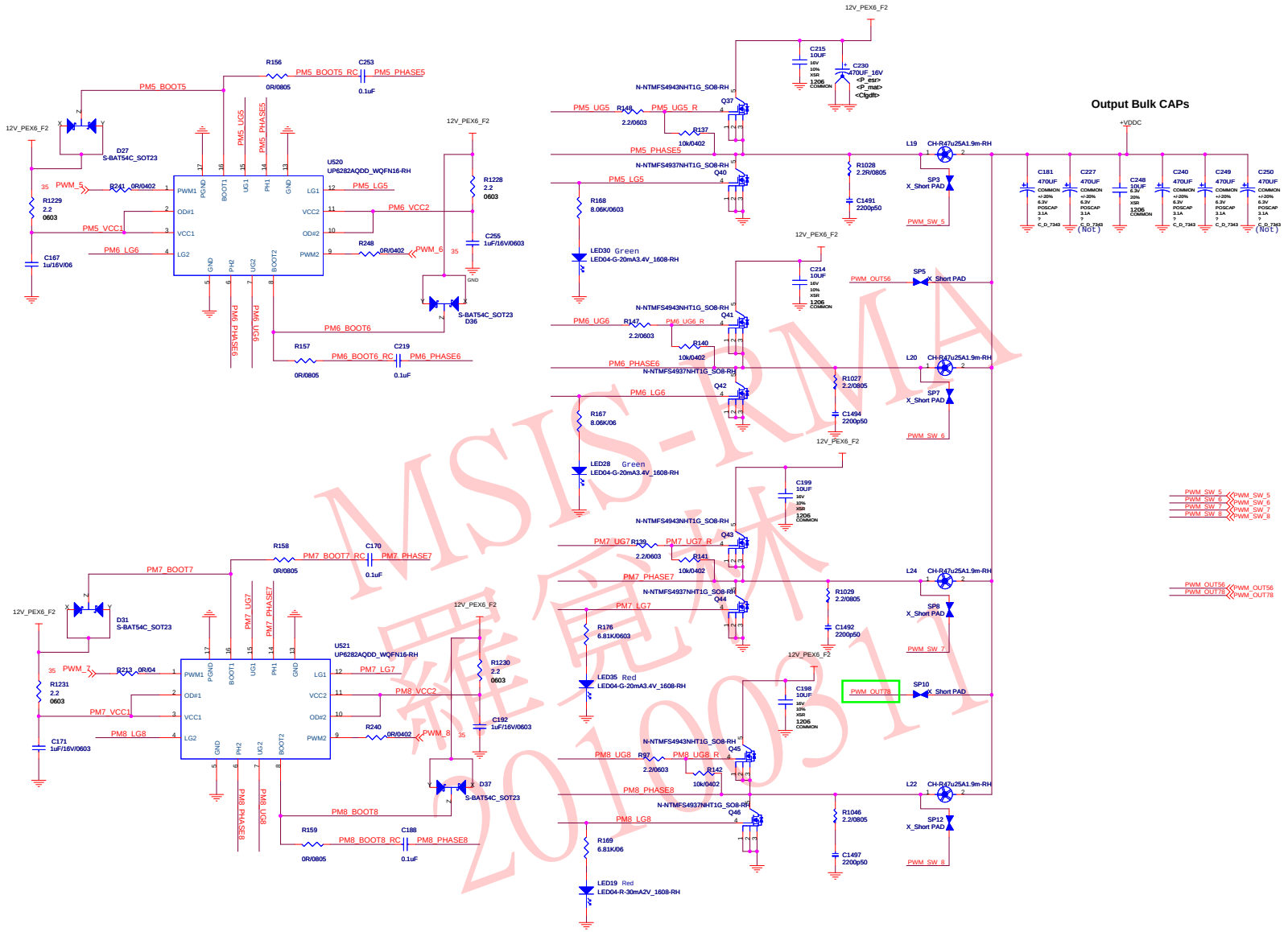
Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	09/08/11	Initial release. Based on CYpress XT C001 00 PCB
1	00B	09/08/26	1. To use the Phoenix shroud with the heatsink solution Move the power connectors beside each other 2. Added PCIe reset delay circuitry;

1.page7: co-layout CLK generator
2.page10 : remove co-layout DP component and circuit, HDMI SMD change DIP
3.page14 : remove up6213 PWM circuit , change Up6208 circuit
4.page15 : remove up6101 PWM circuit , change Up6205 circuit
5.page17 : change ML623, ML624,ML625,ML627 SMD,
12V_BUS Input 轉MVDD_S,改爲12V_EXT_A Input
6.page18 : change 5V circuit
7.page21 : add Voltage measure
8.page20 :add 1x4 Pin 風扇circuit
9.page21 : add thermal NCT7717u circuit

1.0
1.page3/4: modify DRAM_RST2 circuit
2.page7: add 27M 終端電阻

Power Supply: NVVDD Phase 5~8 powered from internal PEX edge connector



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 3-4 of 4

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<Title>

Size	Document Number	Rev
Custom	<Doc>	<FevCode>

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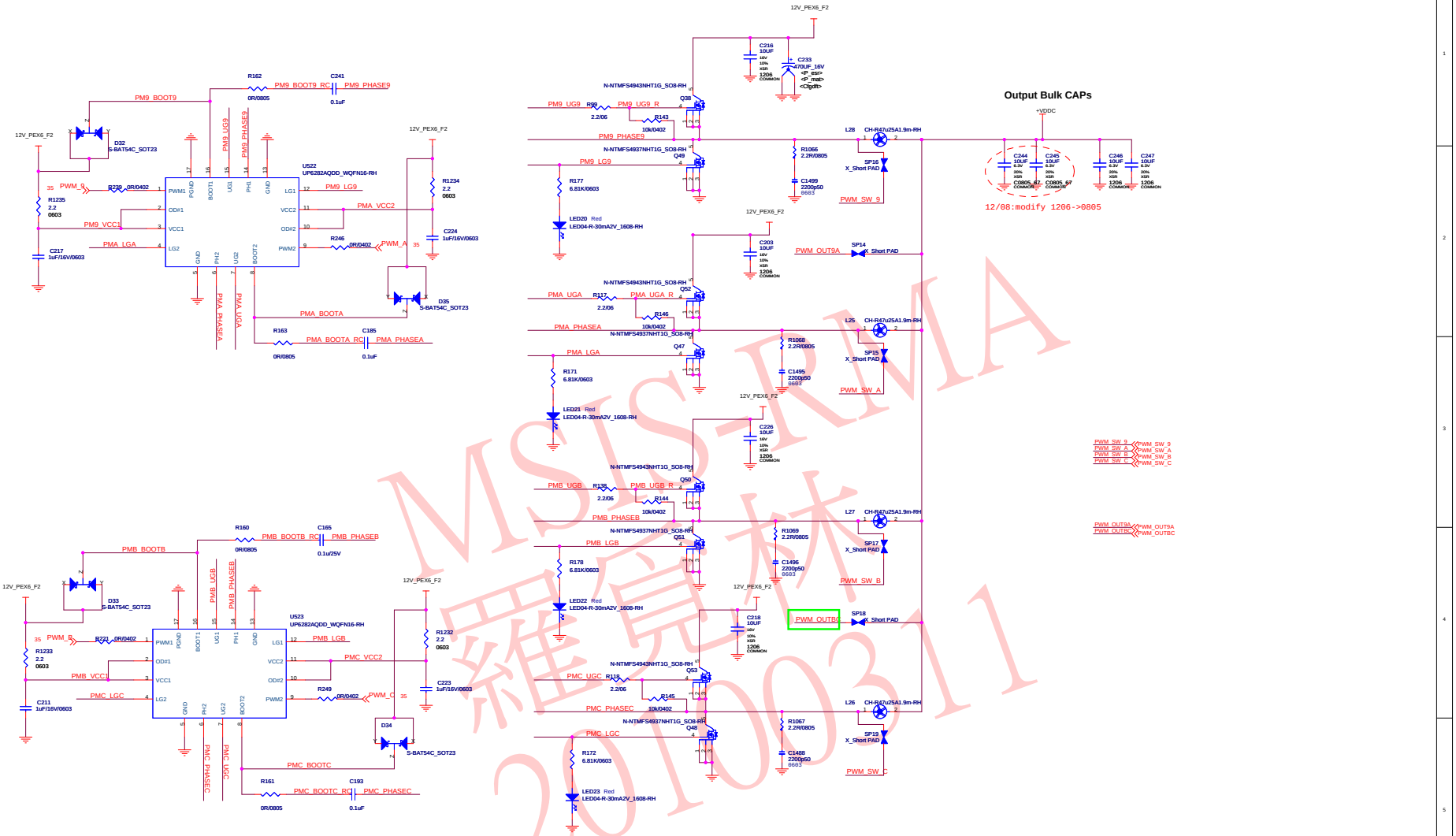
Power Supply: NVVDD Phase 9~12 powered from internal PEX edge connector



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 3-4 of 4

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<Title>

Size	Document Number	Rev
Custom	<Doc>	<RevCode>

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