
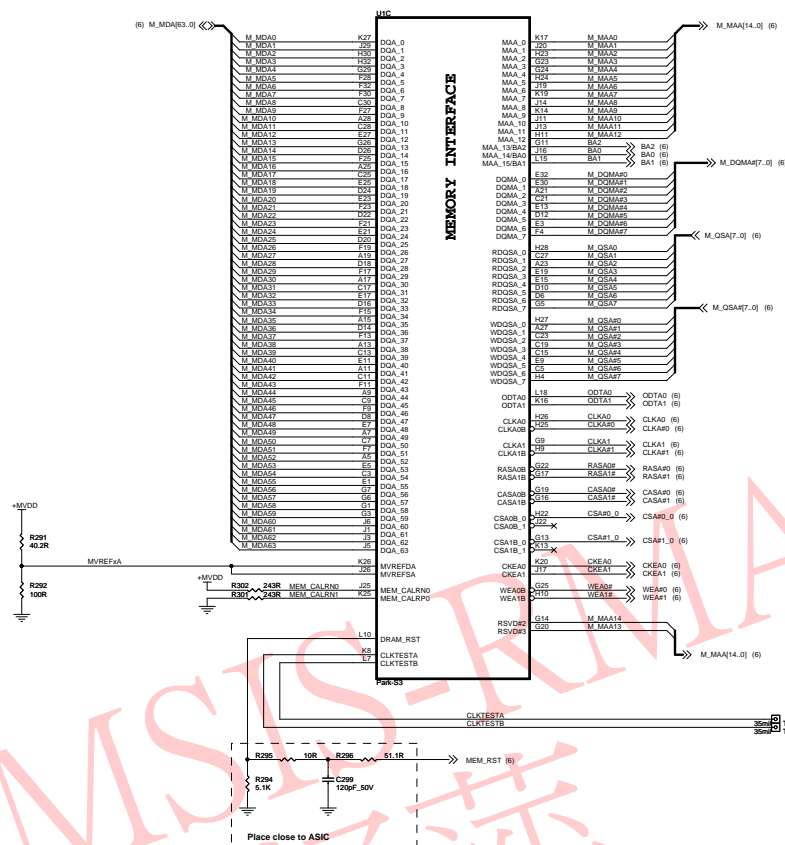
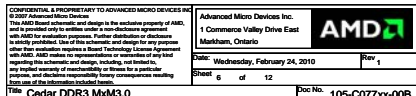
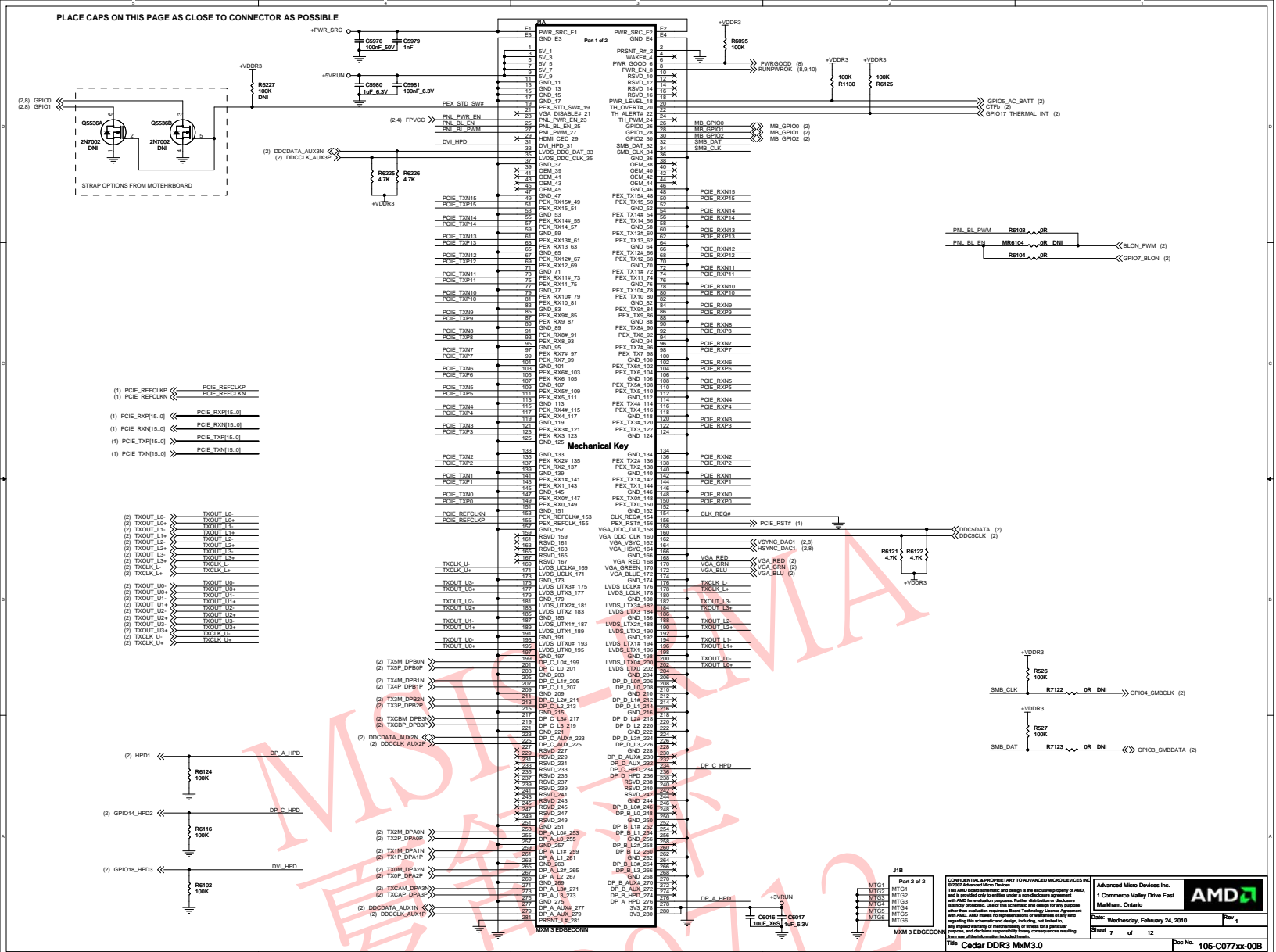


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<p>Date: _____</p>		<p>Wednesday, February 24, 2010</p>		<p>Rev 1</p>	
<p>Sheet _____</p>		<p>3 of 12</p>		<p>Doc No. 105-C077xxc-00B</p>	
<p>Title: Cedar DDR3 M3x0.3</p>					



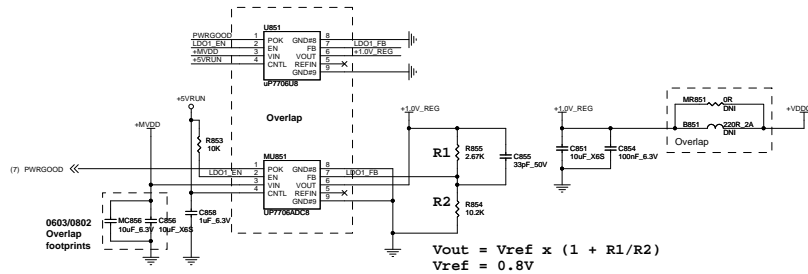
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Voltage Settings and Power Play

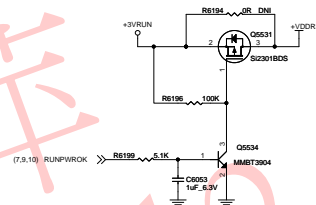
LDO1 Vin = +1.5V +/-2% Vout = +1.0V +/- 2% Iout = 1.5A RMS MAX (TBV)
PCB: 50 to 70mm sq. copper area for cooling



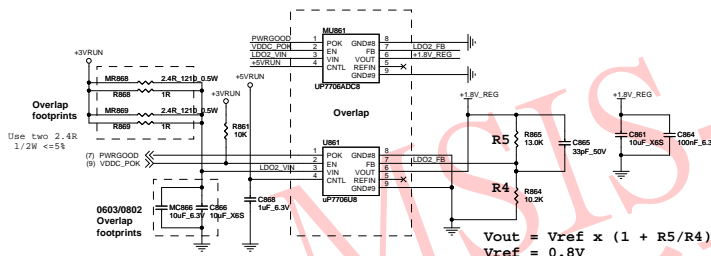
PIN STRAPS

- | GPIO | Pin | Function | IO Type | IO Mode | IO Direction |
|------------------|--------|----------|---------|---------|--------------|
| (2,7) GPIO0 | GPIO0 | R6134 | IOK | | |
| (2,7) GPIO1 | GPIO1 | R6135 | IOK | | |
| (2,7) GPIO2 | GPIO2 | R6136 | IOK | | |
| (2) GPIO9 | GPIO9 | R6138 | IOK | DNI | |
| (2) GPIO11 | GPIO11 | R6139 | IOK | DNI | |
| (2) GPIO12 | GPIO12 | R6140 | IOK | DNI | |
| (2) GPIO13 | GPIO13 | R6141 | IOK | | |
| (2) GPIO22 | GPIO22 | R6147 | IOK | | |
| (2,7) VSYNC_DAC1 | V1SYNC | R6142 | IOK | | |
| (2,7) HS2NC_DAC1 | H1SYNC | R6143 | IOK | | |
| (2) VSYNC_DAC2 | V2SYNC | R6145 | IOK | | |
| (2) HS2NC_DAC2 | H2SYNC | R6146 | IOK | DNI | |

VDDR3 GATING



LDO2 $V_{in} = +3.3V \pm 6\%$ $V_{out} = +1.8V \pm 2\%$ $I_{out} = 0.8A \text{ RMS MAX (TBV)}$
PCB: 50 to 70mm sq. copper area for cooling



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_EN	GPIO0	Power Saving Savings Enable 1. 50% TX output swing 2. Full TX output swing	1
TX_DEEMPH_EN	GPIO1	PCIe Transmitter De-emphasis Enable 1. Tx de-emphasis disabled 2. Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIe Gen2 Enable 1. Advertises the PCIe device as 5.0GT/s capable at power-on	1
BIF_VGA_DS	GPIO9	VGA Control 1. VGA controller capacity enabled 2. VGA controller capacity disabled 3. VGA controller capacity disabled for multi-GPU	0
ROMCFGCFG[0]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO2 = 1, defines ROM type 0 - 512Kbit, 48Mbita memory aperture size 1 - 1Mbit, 48Mbita ROM (S1) 2 - 1Mbit, 48Mbita ROM (S2) 3 - 1Mbit, 48Mbita ROM (S3) 4 - 1Mbit, 48Mbita ROM (S4) 5 - 1Mbit, 48Mbita ROM (S5) 6 - 512Kbit, 48Mbita ROM (S6) 7 - 1Mbit, 48Mbita ROM (S7) 8 - 512Kbit, 48Mbita ROM (S8) 9 - 1Mbit, 48Mbita ROM (S9) 10 - 512Kbit, 48Mbita ROM (S10) 11 - 1Mbit, 48Mbita ROM (S11) 12 - 512Kbit, 48Mbita ROM (S12) 13 - 1Mbit, 48Mbita ROM (S13) 14 - 512Kbit, 48Mbita ROM (S14) 15 - 1Mbit, 48Mbita ROM (S15)	XXX
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 1. Enabled	1
AUD[1] AUD[0]	H2SYNC H2VSYNC	0 - No audio function 1 - Audio to DP only 2 - Audio to HDMI (eDP or HDMI) display is detected 3 - Audio to both DP and HDMI eDP and HDMI may only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
VIP_DEVICE_STRAP_DS	V2SYNC	VIP Device Strap Disable 0. Slave VIP host port device present 1. No slave VIP host port devices reporting presence	1
SMS_EN_HARD	H2SYNC	Reserved	0

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Title Cedar DCR3 MxM3.0 Doc No. 105-C077X-00B

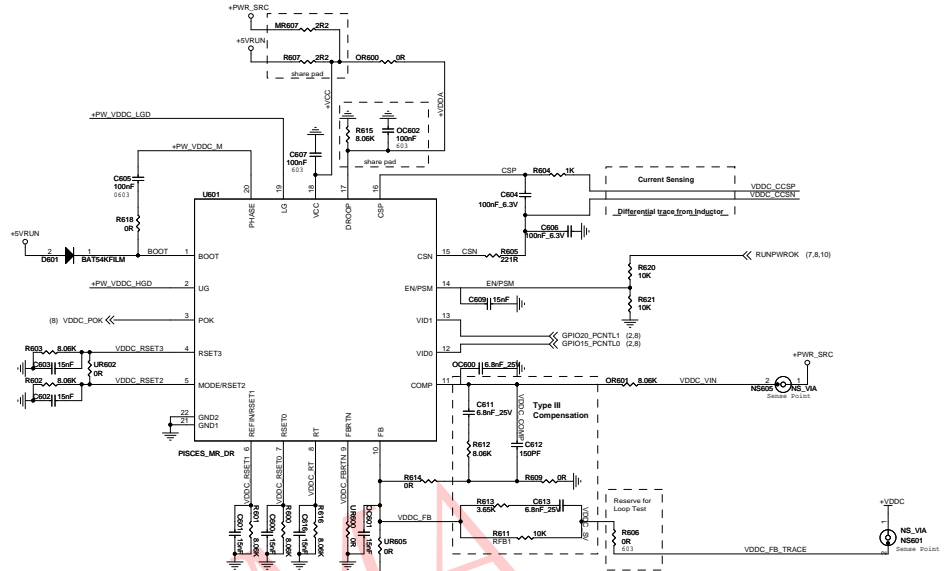


Figure 1: Schematic diagram of the power supply decoupling network. The diagram shows a three-stage decoupling network connected to a power supply rail. The first stage consists of capacitor C639 (330µF, SPIPOSCAP, SMT 7343, Max 1.5mm_H) connected to ground. The second stage consists of capacitor C640 (330µF, SPIPOSCAP, SMT 7343, Max 1.5mm_H) connected to ground. The third stage consists of capacitor C641 (220µF, 2V, SPIPOSCAP, SMT 7343, Max 1.2mm_H) connected to ground. The capacitors are connected in series between the power supply rail and ground. The diagram is labeled "Top Side Hmax=1.5mm" and "Bottom Side Hmax=1.2mm".

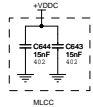


Figure 10 shows two circuit diagrams for capacitor placement. The left diagram, labeled 'Top Side', shows three capacitors: C721 (22uF, 1206, 1.3mm HI), C723 (22uF, 16V, 1206, 1.3mm HI), and C732 (22uF, 16V, 1206, 1.3mm HI). The right diagram, labeled 'Bottom Side', shows one capacitor: C725 (1uF, 16V, 1206, 0.95mm HI). Both diagrams indicate a maximum clearance of 1.5mm for the top side and 2mm for the bottom side.

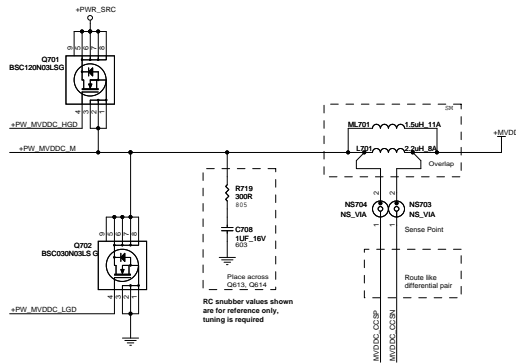
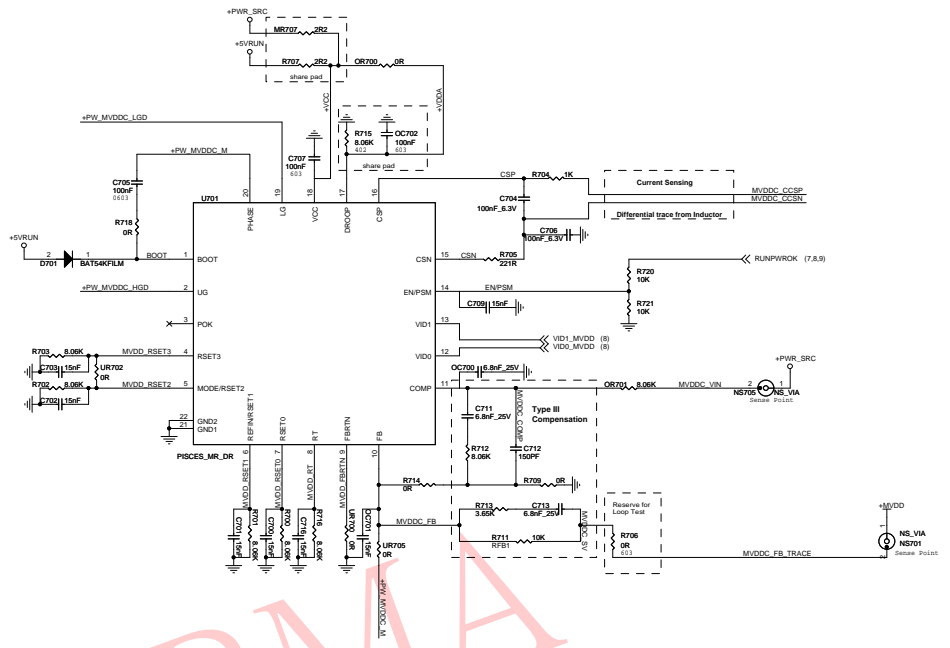

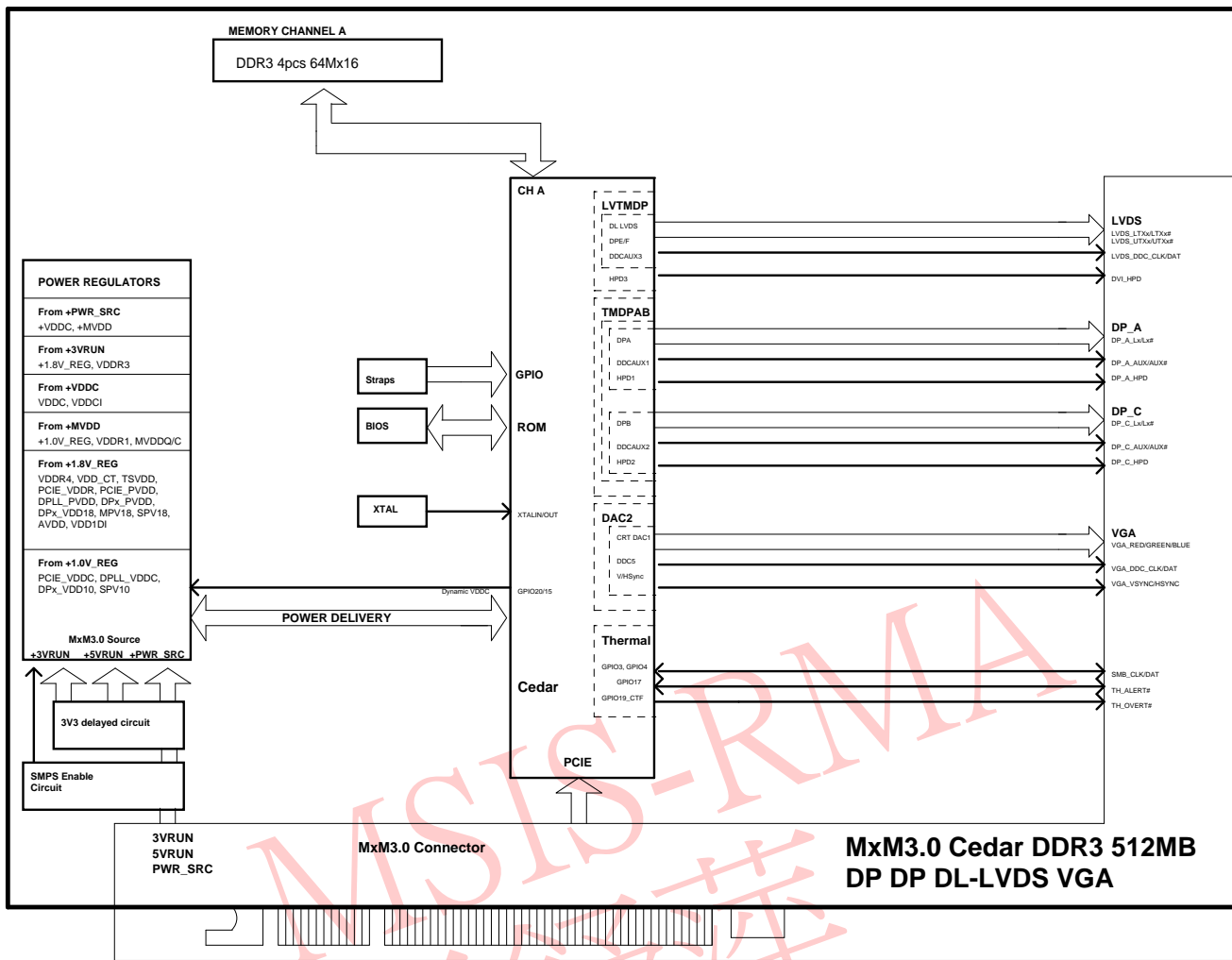


Figure 1 compares two capacitor types: a Low Profile POSCAP and an MLCC. The POSCAP (C737, 330uF) has a height of 1.5mm. The MLCC (C741, 15nF 402) is shown as a standard surface-mount capacitor. Both are connected to +MVDD and ground.



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Title: Cedar DDR3 Mbd3.0		Doc No: 105-C0779a-00B			





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NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

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