

P455-A01 DT SKU2

P455-A01, G71-A02, 256MB 8Mx32 GDDR3 (700Mhz),
DVI -I -DL, DVI -I -DL, HDTV-Out for Dell HMG

Table of Contents:

Page 1: Overview

Page 2: PCI Express 1.0

Page 3: MEMORY: GPU Partition A/B

Page 4: MEMORY: GPU Partition C/D

Page 5: FBA Partition

Page 6: FBB Partition

Page 7: FBC Partition

Page 8: FBD Partition

Page 9: FrameBuffer Net Properties

Page 10: DACA Interface

Page 11: DACC Interface

Page 12: IFP A/B and C/D Interface

Page 13: DACB and Stereo Interface

Page 14: Video Capture (Philips SAA7115)

Page 15: Multi-use IO(MIO) Interface

Page 16: GPIO, I2C, ROM, HDMI, and XTAL

Page 17: Strapping Configuration

Page 18: Power/GND and Decoupling

Page 19: Power Supply I: A2V5, DDC5V, SAA7115, TMDS Supplies

Page 20: Power Supply II: PEX Input Filters, External 12V Power, NVVDD VID Control

Page 21: Power Supply III: FBVDDQ and PEX1V2

Page 22: Power Supply IV: NVVDD

Page 23: Thermal Diode, Fan Control

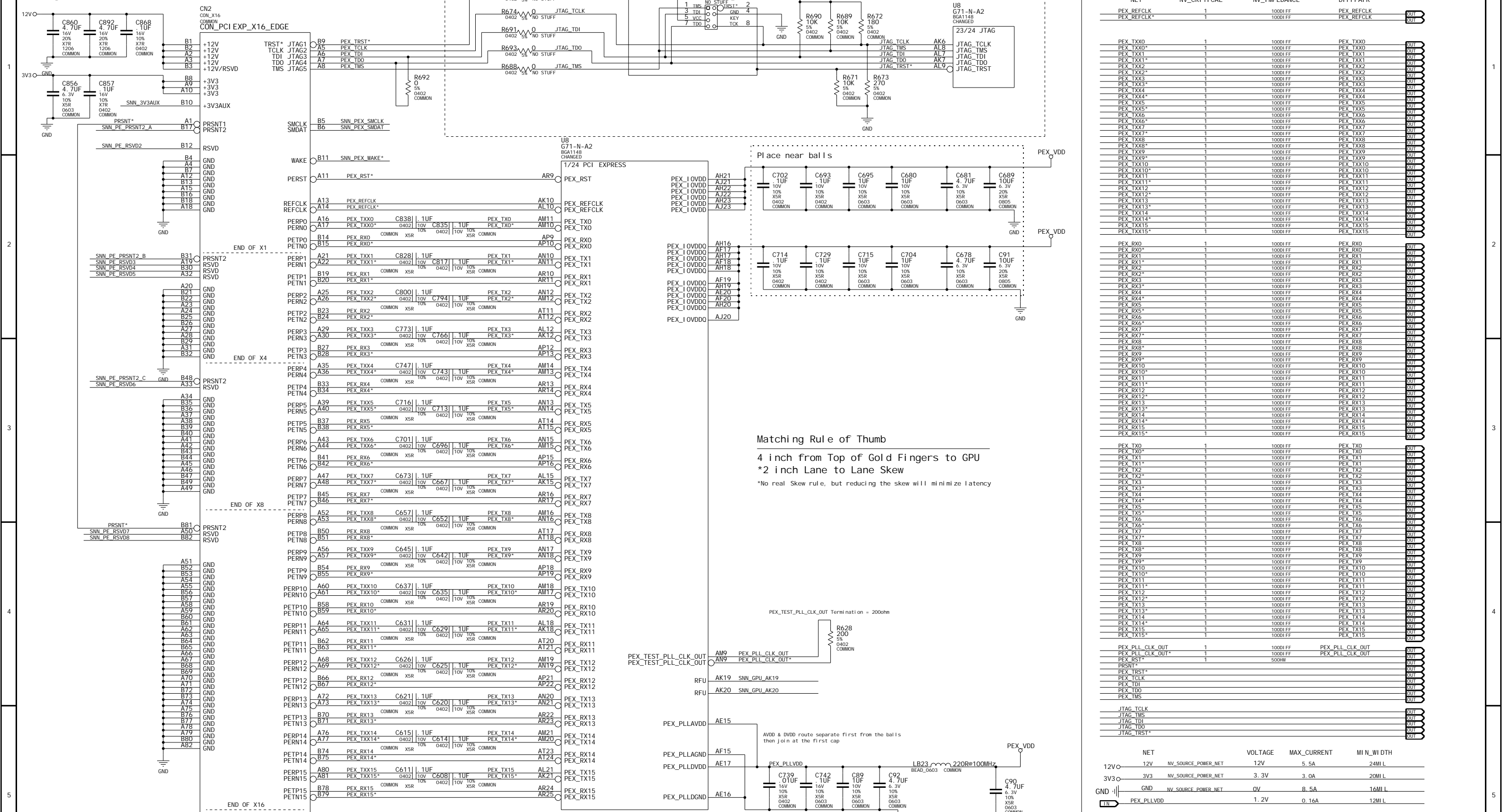
Page 24: Mechanical: Bracket/Thermal Solution

REVISION HISTORY:

X1 RevA: Initial Release

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10455-base-001	P455 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10455-0000-001	G71-GT - 256MB-8Mx32 GDDR3, DVI-I-DL + DVI-I-DL + HDTV, 450/700 MHz
2	SKU0002	600-10455-0002-001	G71-GS - 256MB-8Mx32 GDDR3, DVI-I-DL + DVI-I-DL + HDTV, 450/700 MHz for Dell HMG
3	SKU0500	600-50455-0500-001	G71GL-U - 256MB-8Mx32 GDDR3, DVI-I-DL + DVI-I-DL + STEREO, 450/700 MHz
4	SKU0501	600-50455-0501-001	G71GL-Std - 256MB 8Mx32 GDDR3, DVI-I-DL + DVI-I-DL + HDTV, 375/600 MHz
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

Page2: PCI Express 1.0



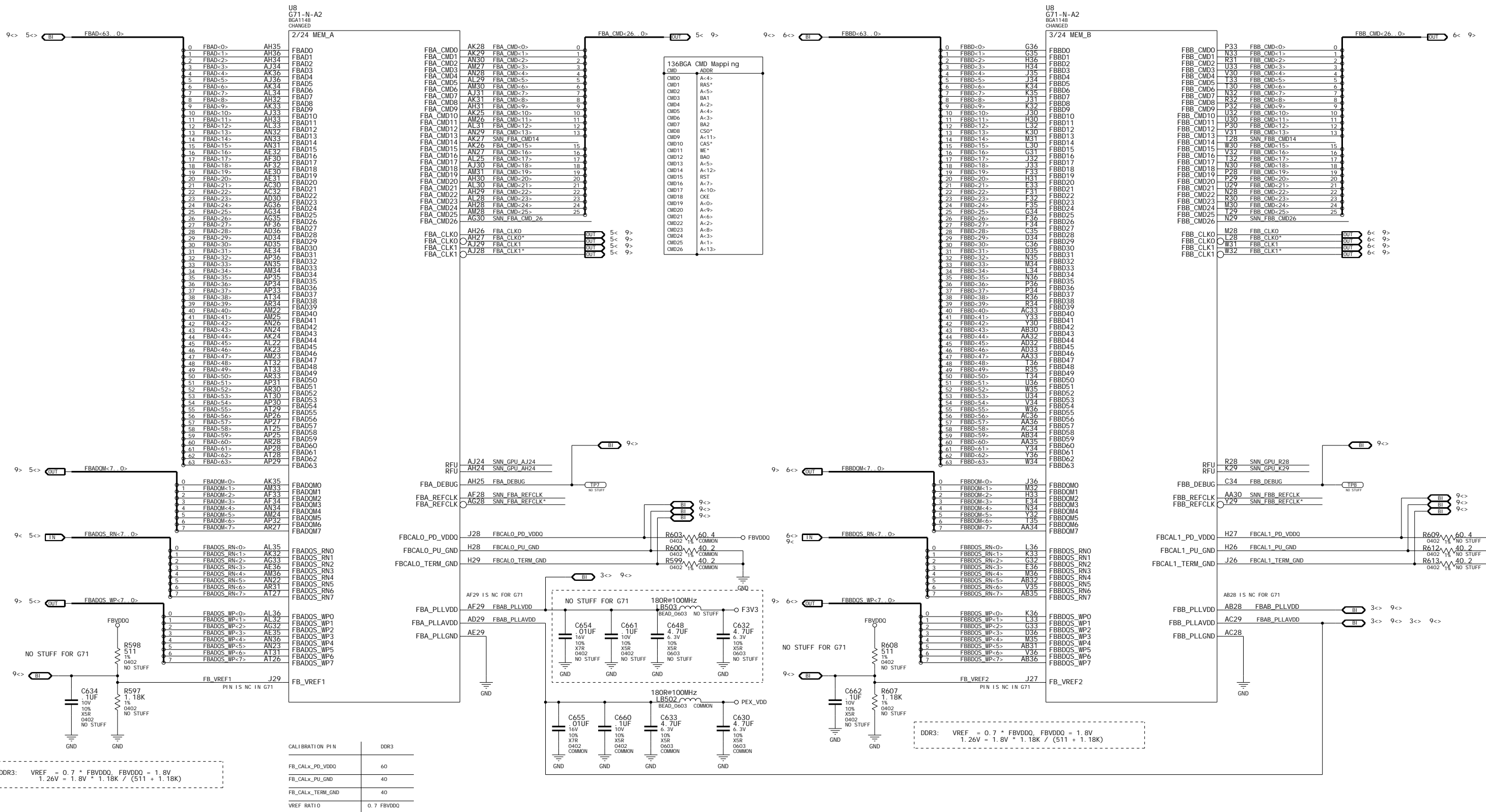
NET		NV_CRI TI CAL		NV_I MPEDANCE		DI FFPAI R	
PEX_REFCLK		1		1000I FF		PEX_REFCLK	
PEX_REFCLK*		1		1000I FF		PEX_REFCLK	OUT
PEX_TX00		1		1000I FF		PEX_TX00	OUT
PEX_TX00*		1		1000I FF		PEX_TX00	OUT
PEX_TXX1		1		1000I FF		PEX_TXX1	OUT
PEX_TXX1*		1		1000I FF		PEX_TXX1	OUT
PEX_TXX2		1		1000I FF		PEX_TXX2	OUT
PEX_TXX2*		1		1000I FF		PEX_TXX2	OUT
PEX_TXX3		1		1000I FF		PEX_TXX3	OUT
PEX_TXX3*		1		1000I FF		PEX_TXX3	OUT
PEX_TXX4		1		1000I FF		PEX_TXX4	OUT
PEX_TXX4*		1		1000I FF		PEX_TXX4	OUT
PEX_TXX5		1		1000I FF		PEX_TXX5	OUT
PEX_TXX5*		1		1000I FF		PEX_TXX5	OUT
PEX_TXX6		1		1000I FF		PEX_TXX6	OUT
PEX_TXX6*		1		1000I FF		PEX_TXX6	OUT
PEX_TXX7		1		1000I FF		PEX_TXX7	OUT
PEX_TXX7*		1		1000I FF		PEX_TXX7	OUT
PEX_TXX8		1		1000I FF		PEX_TXX8	OUT
PEX_TXX8*		1		1000I FF		PEX_TXX8	OUT
PEX_TXX9		1		1000I FF		PEX_TXX9	OUT
PEX_TXX9*		1		1000I FF		PEX_TXX9	OUT
PEX_TXX10		1		1000I FF		PEX_TXX10	OUT
PEX_TXX10*		1		1000I FF		PEX_TXX10	OUT
PEX_TXX11		1		1000I FF		PEX_TXX11	OUT
PEX_TXX11*		1		1000I FF		PEX_TXX11	OUT
PEX_TXX12		1		1000I FF		PEX_TXX12	OUT
PEX_TXX12*		1		1000I FF		PEX_TXX12	OUT
PEX_TXX13		1		1000I FF		PEX_TXX13	OUT
PEX_TXX13*		1		1000I FF		PEX_TXX13	OUT
PEX_TXX14		1		1000I FF		PEX_TXX14	OUT
PEX_TXX14*		1		1000I FF		PEX_TXX14	OUT
PEX_TXX15		1		1000I FF		PEX_TXX15	OUT
PEX_TXX15*		1		1000I FF		PEX_TXX15	OUT
PEX_RX0		1		1000I FF		PEX_RX0	OUT
PEX_RX0*		1		1000I FF		PEX_RX0	OUT
PEX_RX1		1		1000I FF		PEX_RX1	OUT
PEX_RX1*		1		1000I FF		PEX_RX1	OUT
PEX_RX2		1		1000I FF		PEX_RX2	OUT
PEX_RX2*		1		1000I FF		PEX_RX2	OUT
PEX_RX3		1		1000I FF		PEX_RX3	OUT
PEX_RX3*		1		1000I FF		PEX_RX3	OUT
PEX_RX4		1		1000I FF		PEX_RX4	OUT
PEX_RX4*		1		1000I FF		PEX_RX4	OUT
PEX_RX5		1		1000I FF		PEX_RX5	OUT
PEX_RX5*		1		1000I FF		PEX_RX5	OUT
PEX_RX6		1		1000I FF		PEX_RX6	OUT
PEX_RX6*		1		1000I FF		PEX_RX6	OUT
PEX_RX7		1		1000I FF		PEX_RX7	OUT
PEX_RX7*		1		1000I FF		PEX_RX7	OUT
PEX_RX8		1		1000I FF		PEX_RX8	OUT
PEX_RX8*		1		1000I FF		PEX_RX8	OUT
PEX_RX9		1		1000I FF		PEX_RX9	OUT
PEX_RX9*		1		1000I FF		PEX_RX9	OUT
PEX_RX10		1		1000I FF		PEX_RX10	OUT
PEX_RX10*		1		1000I FF		PEX_RX10	OUT
PEX_RX11		1		1000I FF		PEX_RX11	OUT
PEX_RX11*		1		1000I FF		PEX_RX11	OUT
PEX_RX12		1		1000I FF		PEX_RX12	OUT
PEX_RX12*		1		1000I FF		PEX_RX12	OUT
PEX_RX13		1		1000I FF		PEX_RX13	OUT
PEX_RX13*		1		1000I FF		PEX_RX13	OUT
PEX_RX14		1		1000I FF		PEX_RX14	OUT
PEX_RX14*		1		1000I FF		PEX_RX14	OUT
PEX_RX15		1		1000I FF		PEX_RX15	OUT
PEX_RX15*		1		1000I FF		PEX_RX15	OUT
PEX_TX0		1		1000I FF		PEX_TX0	OUT
PEX_TX0*		1		1000I FF		PEX_TX0	OUT
PEX_TX1		1		1000I FF		PEX_TX1	OUT
PEX_TX1*		1		1000I FF		PEX_TX1	OUT
PEX_TX2		1		1000I FF		PEX_TX2	OUT
PEX_TX2*		1		1000I FF		PEX_TX2	OUT
PEX_TX3		1		1000I FF		PEX_TX3	OUT
PEX_TX3*		1		1000I FF		PEX_TX3	OUT
PEX_TX4		1		1000I FF		PEX_TX4	OUT
PEX_TX4*		1		1000I FF		PEX_TX4	OUT
PEX_TX5		1		1000I FF		PEX_TX5	OUT
PEX_TX5*		1		1000I FF		PEX_TX5	OUT
PEX_TX6		1		1000I FF		PEX_TX6	OUT
PEX_TX6*		1		1000I FF		PEX_TX6	OUT
PEX_TX7		1		1000I FF		PEX_TX7	OUT
PEX_TX7*		1		1000I FF		PEX_TX7	OUT
PEX_TX8		1		1000I FF		PEX_TX8	OUT
PEX_TX8*		1		1000I FF		PEX_TX8	OUT
PEX_TX9		1		1000I FF		PEX_TX9	OUT
PEX_TX9*		1		1000I FF		PEX_TX9	OUT
PEX_TX10		1		1000I FF		PEX_TX10	OUT
PEX_TX10*		1		1000I FF		PEX_TX10	OUT
PEX_TX11		1		1000I FF		PEX_TX11	OUT
PEX_TX11*		1		1000I FF		PEX_TX11	OUT
PEX_TX12		1		1000I FF		PEX_TX12	OUT
PEX_TX12*		1		1000I FF		PEX_TX12	OUT
PEX_TX13		1		1000I FF		PEX_TX13	OUT
PEX_TX13*		1		1000I FF		PEX_TX13	OUT
PEX_TX14		1		1000I FF		PEX_TX14	OUT
PEX_TX14*		1		1000I FF		PEX_TX14	OUT
PEX_TX15		1		1000I FF		PEX_TX15	OUT
PEX_TX15*		1		1000I FF		PEX_TX15	OUT
PEX_PLL_CLK_OUT		1		1000I FF		PEX_PLL_CLK_OUT	OUT
PEX_PLL_CLK_OUT*		1		1000I FF		PEX_PLL_CLK_OUT	OUT
PEX_RST*		1		500mH			OUT
PRSWT*							OUT
PEX_TRST*							OUT
PEX_TCLK							OUT
PEX_TDI							OUT
PEX_TDO							OUT
PEX_TMS							OUT
JTAG_TCLK							OUT
JTAG_TMS							OUT
JTAG_TDI							OUT
JTAG_TDO							OUT
JTAG_TRST*							OUT
NET				VOLTAGE	MAX_CURRENT	MI N_WI DTH	
12V○	12V	NV_SOURCE_POWER_NET		12V	5. 5A	24MI L	
3V3○	3V3	NV_SOURCE_POWER_NET		3. 3V	3. 0A	20MI L	
GND	GND	NV_SOURCE_POWER_NET		0V	8. 5A	16MI L	
PEX_PLLVDD				1. 2V	0. 16A	12MI L	

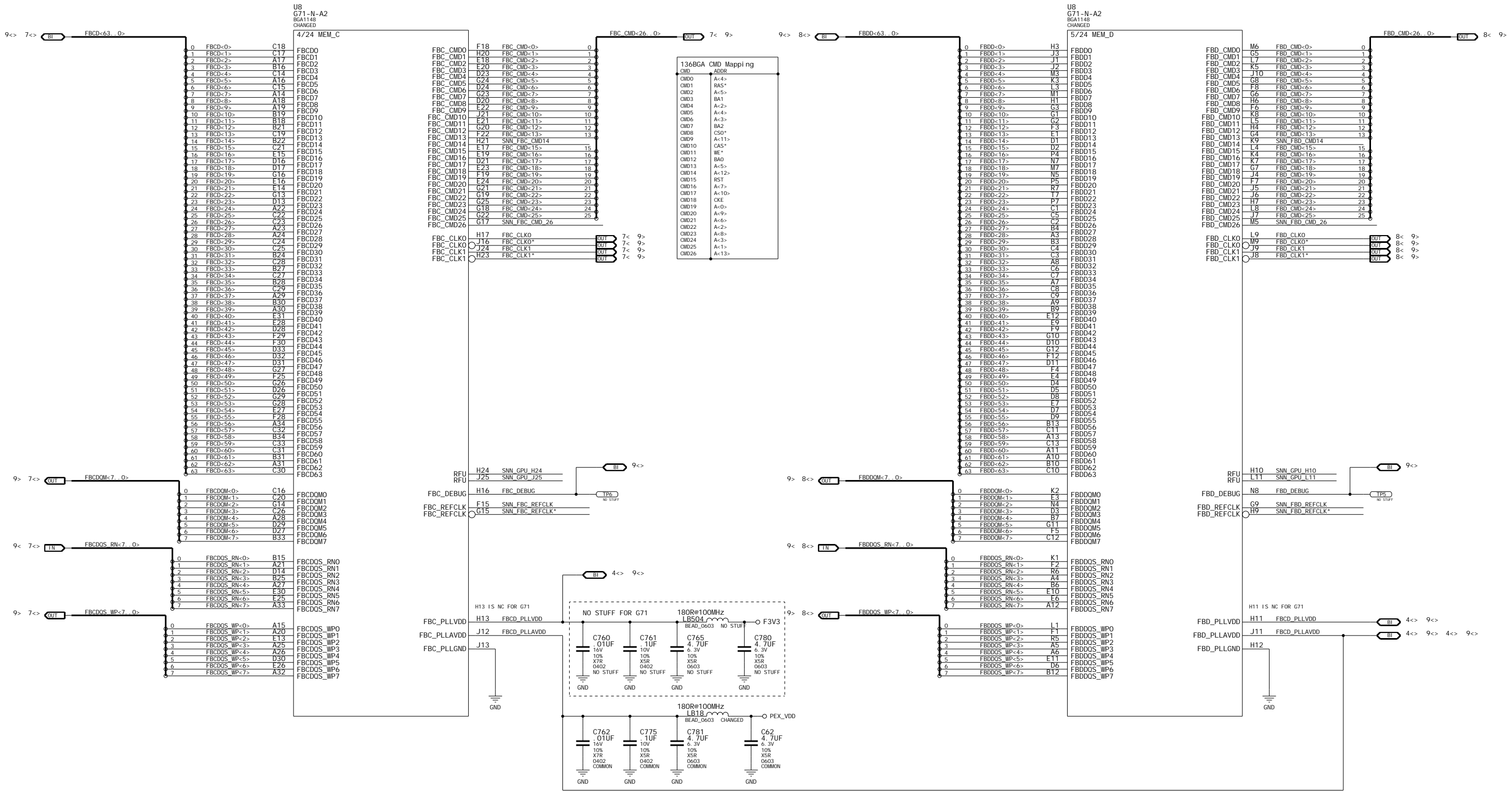
Matching Rule of Thumb

4 inch from Top of Gold Fingers to GPU
*2 inch Lane to Lane Skew

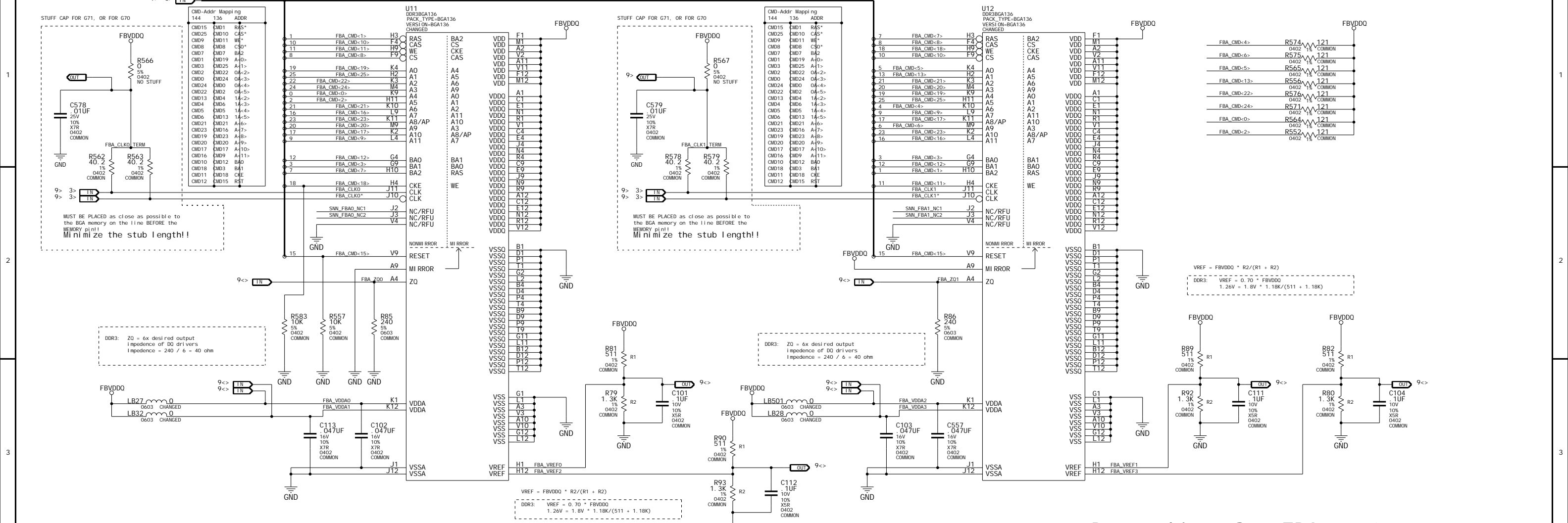
*No real Skew rule, but reducing the skew will minimize latency

ASSEMBLY	G71-GS - 256MB-8Mx32 GDDR3, DVI-I-DL + DVI-I-DL + HDTV, 450/700 MHz for Dell HMG4	SANTA CLARA, CA 95050, USA	
PAGE DETAIL	PCI Express 1.0	NV_PN	600-10455-0002-001
AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY		ID	design
WISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL		PAGE	2 OF 24
FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.		NAME	LFarasati
		DATE	9-FEB-2006

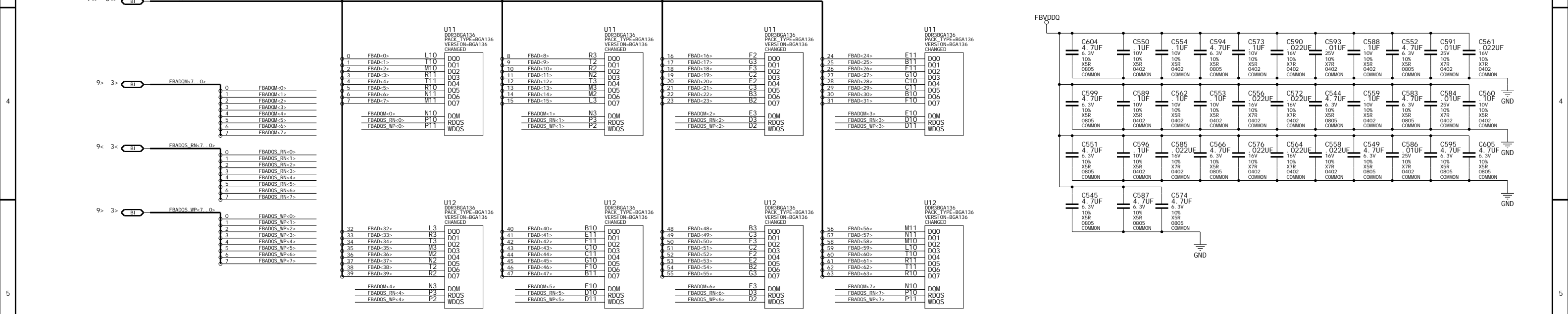




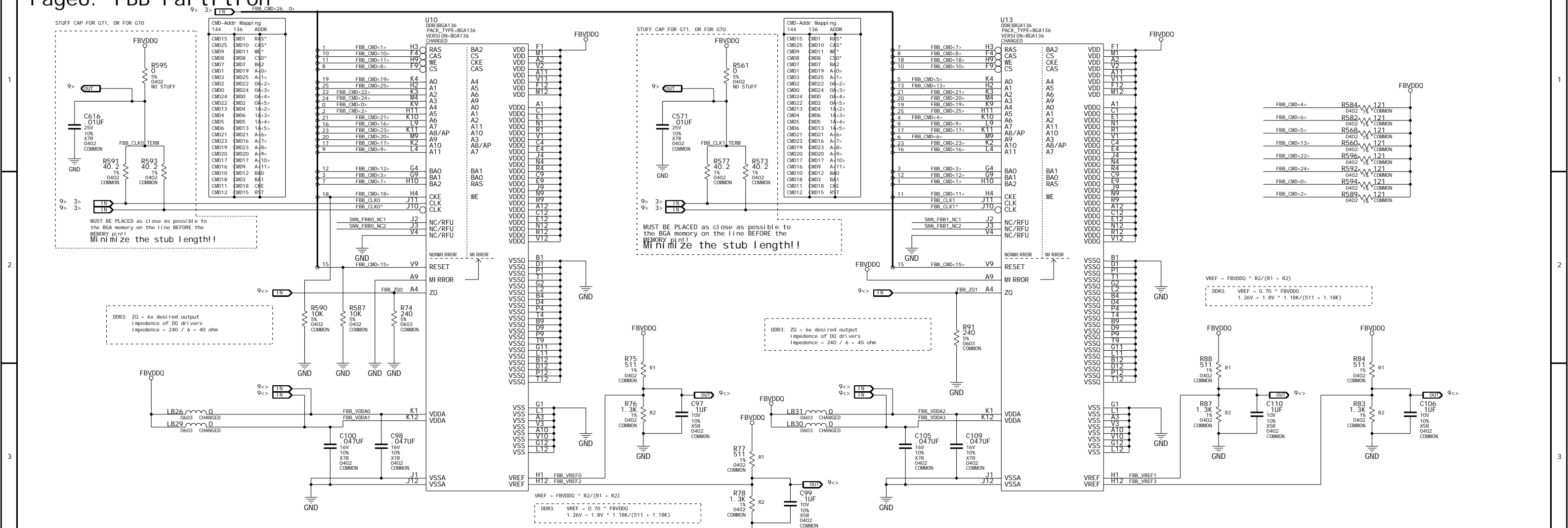
Page5: FBA Parti ti on



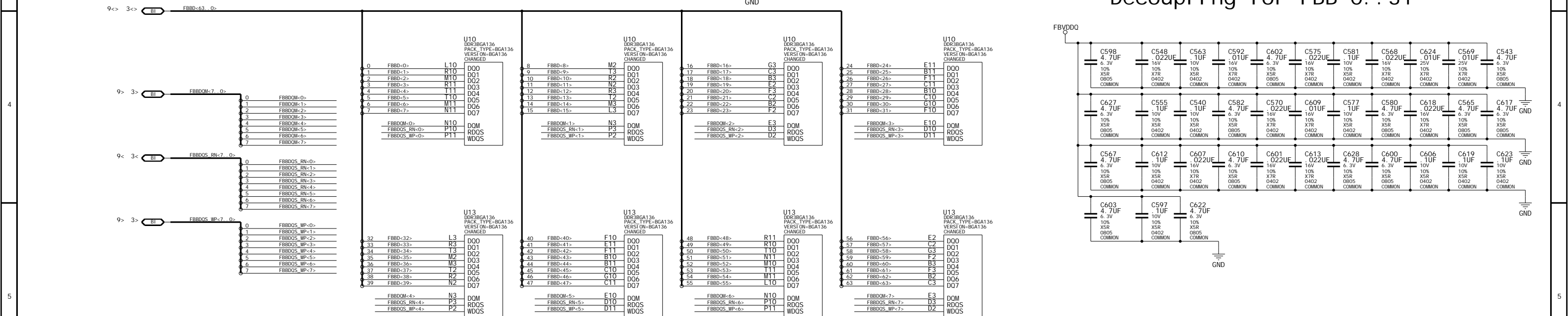
Decoupling for FBA 0..31



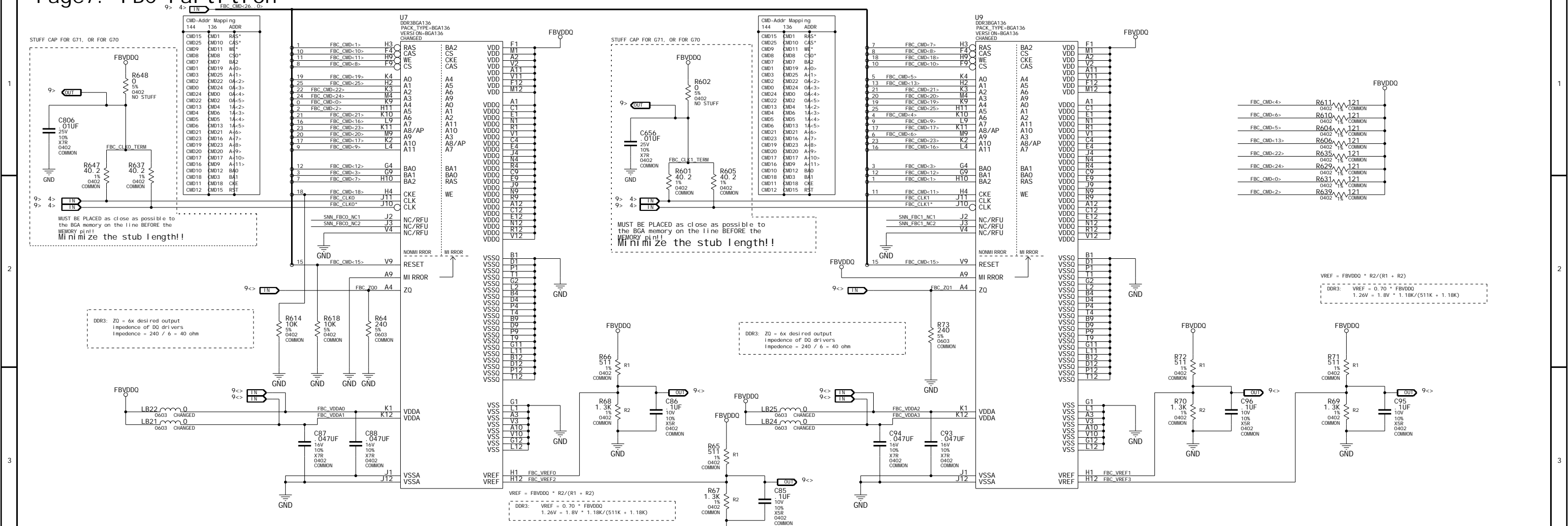
Page6: FBB Partition



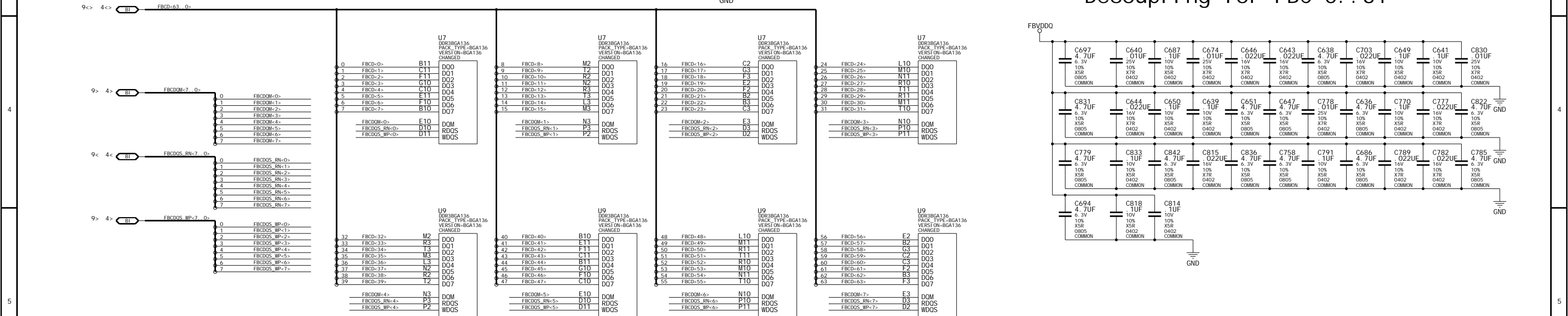
Decoupling for FBB 0..31



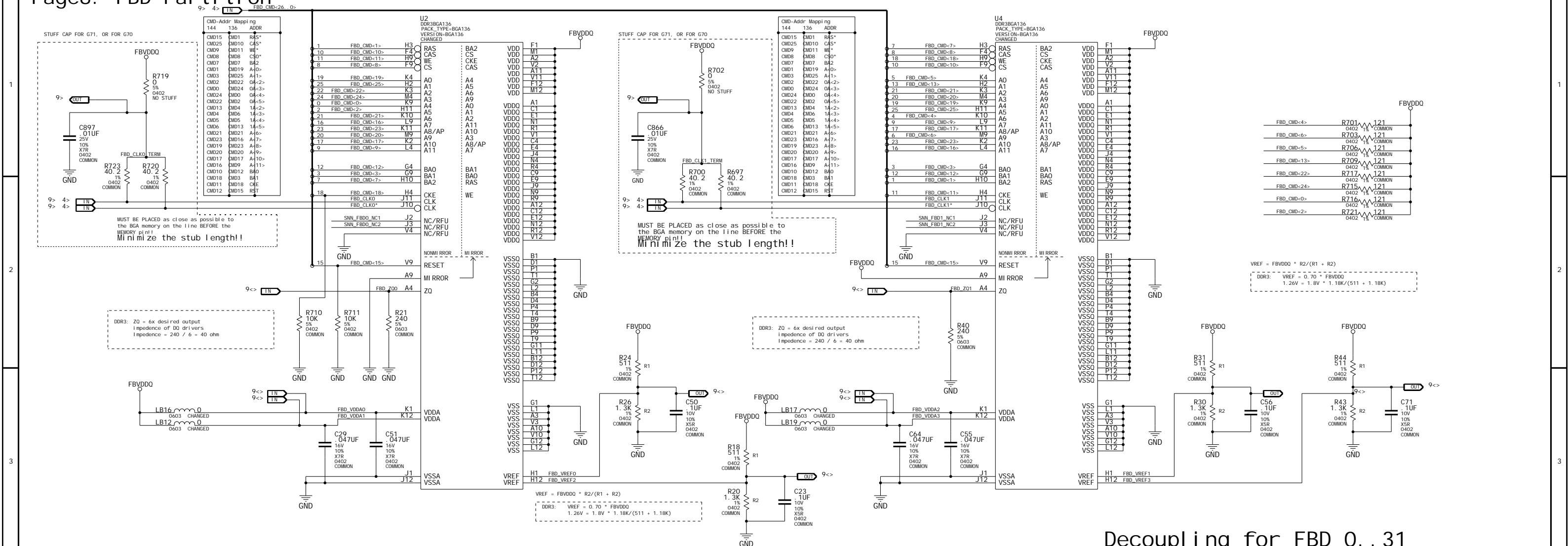
Page7: FBC Partition



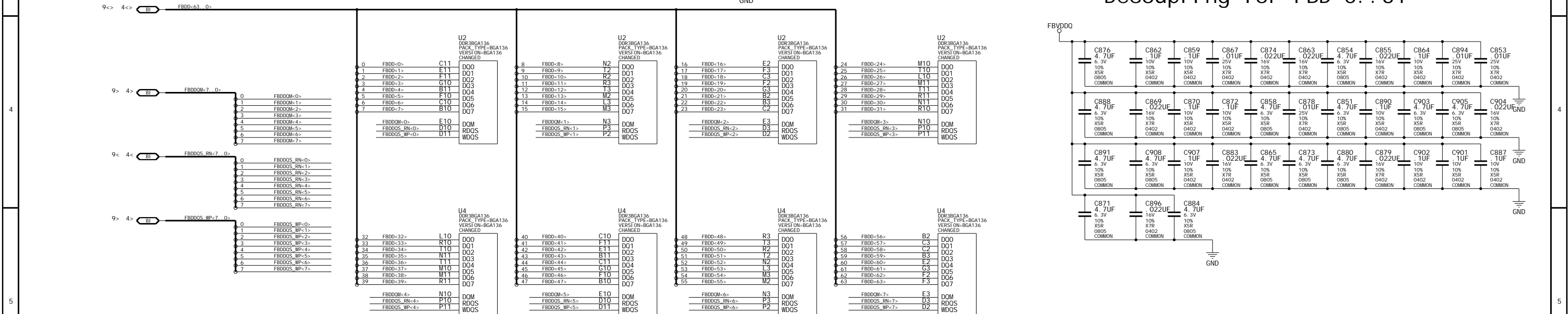
Decoupling for FBC 0..31



Page8: FBD Partit ion



Decoupling for FBD 0..31



NET RULES for FrameBuffer A/B

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
5<	3>	OUT FBA_CLK0	1	80DFF	FBA_CLK0
5<	3>	OUT FBA_CLK0*	1	80DFF	FBA_CLK0
5<	3>	OUT FBA_CLK0_TERM	1	400HM	
5<	3>	OUT FBA_CLK1	1	80DFF	FBA_CLK1
5<	3>	OUT FBA_CLK1*	1	80DFF	FBA_CLK1
5<	3>	OUT FBA_CLK1_TERM	1	400HM	

5<	3>	OUT FBA_CMD<26..0>	1	500HM	
5<>	3>	OUT FBDDQS_WP<7..0>	1	500HM	
5<>	3<	IN FBDDQS_RN<7..0>	1	500HM	
5<>	3<	OUT FBDDQM<7..0>	1	500HM	
5<>	3<>	BI FBDD<63..0>	1	500HM	

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
6<	3>	OUT FBB_CLK0	1	80DFF	FBB_CLK0
6<	3>	OUT FBB_CLK0*	1	80DFF	FBB_CLK0
6<	3>	OUT FBB_CLK0_TERM	1	400HM	
6<	3>	OUT FBB_CLK1	1	80DFF	FBB_CLK1
6<	3>	OUT FBB_CLK1*	1	80DFF	FBB_CLK1
6<	3>	OUT FBB_CLK1_TERM	1	400HM	

6<	3>	OUT FBB_CMD<26..0>	1	500HM	
6<>	3>	OUT FBDDQS_WP<7..0>	1	500HM	
6<>	3<	IN FBDDQS_RN<7..0>	1	500HM	
6<>	3<	OUT FBDDQM<7..0>	1	500HM	
6<>	3<>	BI FBDD<63..0>	1	500HM	

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
3<>	BI	FBAL0_PD_VDD0	1	500HM	
3<>	BI	FBAL0_PU_GND	1	500HM	
3<>	BI	FBAL0_TERM_GND	1	500HM	
3<>	BI	FBAL1_PD_VDD0	1	500HM	
3<>	BI	FBAL1_PU_GND	1	500HM	
3<>	BI	FBAL1_TERM_GND	1	500HM	
3<>	BI	FBA_DEBUG	1	500HM	
3<>	BI	FBB_DEBUG	1	500HM	

		NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
3<>	BI	FBAB_PLLVDD	3.3V	0.04A	12MIL
3<>	BI	FBAB_PLLAVDD	1.2V	0.12A	12MIL
5>	BI	FBA_VREF0	1.26V	0.02A	12MIL
5>	BI	FBA_VREF1	1.26V	0.02A	12MIL
5>	BI	FBA_VREF2	1.26V	0.02A	12MIL
5>	BI	FBA_VREF3	1.26V	0.02A	12MIL
5<	BI	FBA_Z00	1.26V	0.02A	12MIL
5<	BI	FBA_Z01	1.26V	0.02A	12MIL
5<	BI	FBA_VDDA0	1.8V	0.02A	12MIL
5<	BI	FBA_VDDA1	1.8V	0.02A	12MIL
5<	BI	FBA_VDDA2	1.8V	0.02A	12MIL
5<	BI	FBA_VDDA3	1.8V	0.02A	12MIL

6>	BI	FBB_VREF0	1.26V	0.02A	12MIL
6>	BI	FBB_VREF1	1.26V	0.02A	12MIL
6>	BI	FBB_VREF2	1.26V	0.02A	12MIL
6>	BI	FBB_VREF3	1.26V	0.02A	12MIL
6<	BI	FBB_Z00	1.26V	0.02A	12MIL
6<	BI	FBB_Z01	1.26V	0.02A	12MIL
6<	BI	FBB_VDDA0	1.8V	0.02A	12MIL
6<	BI	FBB_VDDA1	1.8V	0.02A	12MIL
6<	BI	FBB_VDDA2	1.8V	0.02A	12MIL
6<	BI	FBB_VDDA3	1.8V	0.02A	12MIL
3<>	BI	FB_VREF1	1.26V	0.02A	12MIL
3<>	BI	FB_VREF2	1.26V	0.02A	12MIL

NET RULES for FrameBuffer C/D

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
7<	4>	OUT FBC_CLK0	1	80DFF	FBC_CLK0
7<	4>	OUT FBC_CLK0*	1	80DFF	FBC_CLK0
7>	4>	OUT FBC_CLK0_TERM	1	400HM	
7<	4>	OUT FBC_CLK1	1	80DFF	FBC_CLK1
7<	4>	OUT FBC_CLK1*	1	80DFF	FBC_CLK1
7>	4>	OUT FBC_CLK1_TERM	1	400HM	

7<	4>	OUT FBC_CMD<26..0>	1	500HM	
7<>	4>	OUT FBDDQS_WP<7..0>	1	500HM	
7<>	4>	OUT FBDDQS_RN<7..0>	1	500HM	
7<>	4>	OUT FBDDQM<7..0>	1	500HM	
7<>	4<>	BI FBDD<63..0>	1	500HM	

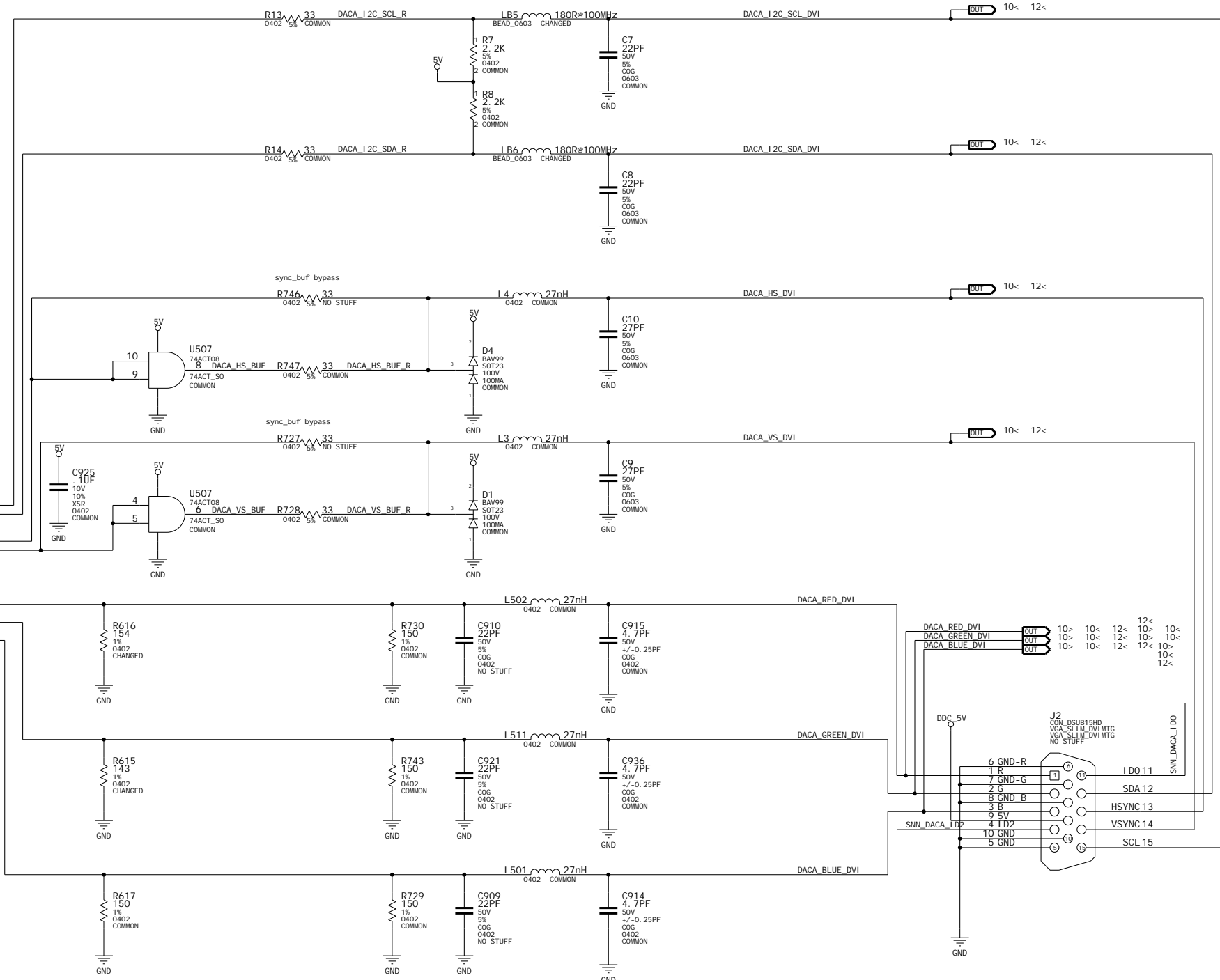
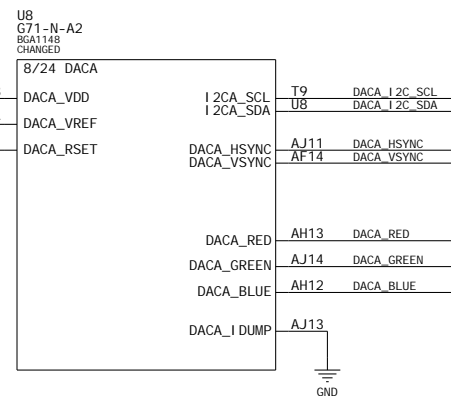
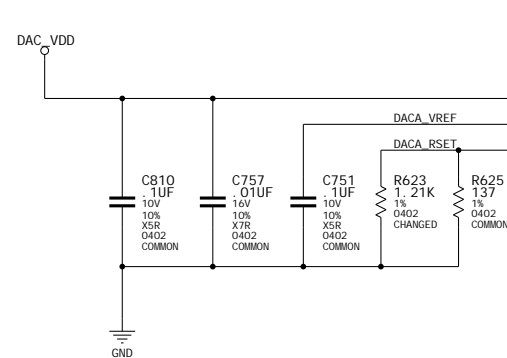
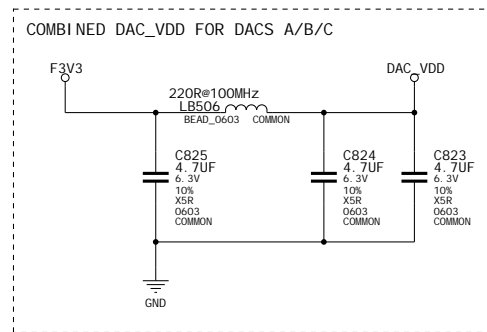
		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
8<	4>	OUT FBD_CLK0	1	80DFF	FBD_CLK0
8<	4>	OUT FBD_CLK0*	1	80DFF	FBD_CLK0
8>	4>	OUT FBD_CLK0_TERM	1	400HM	
8<	4>	OUT FBD_CLK1	1	80DFF	FBD_CLK1
8<	4>	OUT FBD_CLK1*	1	80DFF	FBD_CLK1
8>	4>	OUT FBD_CLK1_TERM	1	400HM	

8<	4>	OUT FBD_CMD<26..0>	1	500HM	
8<>	4>	OUT FBDDQS_WP<7..0>	1	500HM	
8<>	4>	OUT FBDDQS_RN<7..0>	1	500HM	
8<>	4>	OUT FBDDQM<7..0>	1	500HM	
8<>	4<>	BI FBDD<63..0>	1	500HM	
4<>	BI	FBC_DEBUG	1	500HM	
4<>	BI	FBD_DEBUG	1	500HM	

		NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
4<>	BI	FBDD_PLLVDD	3.3V	0.04A	12MIL
4<>	BI	FBDD_PLLAVDD	1.2V	0.12A	12MIL
7>	BI	FBC_VREF0	1.26V	0.02A	12MIL
7>	BI	FBC_VREF1	1.26V	0.02A	12MIL
7>	BI	FBC_VREF2	1.26V	0.02A	12MIL
7>	BI	FBC_VREF3	1.26V	0.02A	12MIL
7<	BI	FBC_Z00	1.26V	0.02A	12MIL
7<	BI	FBC_Z01	1.26V	0.02A	12MIL
7<	BI	FBC_VDDA0	1.8V	0.02A	12MIL
7<	BI	FBC_VDDA1	1.8V	0.02A	12MIL
7<	BI	FBC_VDDA2	1.8V	0.02A	12MIL
7<	BI	FBC_VDDA3	1.8V	0.02A	12MIL

9>	BI	FBD_VREF0	1.26V	0.02A	12MIL
9>	BI	FBD_VREF1	1.26V	0.02A	12MIL
8>	BI	FBD_VREF2	1.26V	0.02A	12MIL
8>	BI	FBD_VREF3	1.26V	0.02A	12MIL
8<	BI	FBD_Z00	1.26V	0.02A	12MIL
8<	BI	FBD_Z01	1.26V	0.02A	12MIL
8<	BI	FBD_VDDA0	1.8V	0.02A	12MIL
8<	BI	FBD_VDDA1	1.8V	0.02A	12MIL
8<	BI	FBD_VDDA2	1.8V	0.02A	12MIL
8<	BI	FBD_VDDA3	1.8V	0.02A	12MIL

Page10: DACA Interface



DACA NET RULES

		NET	NV_CRI T I CAL	NV_I MPEDANCE	ECSet
		DACA_RED	1	750HM	DAC_RGB_CSET
		DACA_GREEN	1	750HM	DAC_RGB_CSET
		DACA_BLUE	1	750HM	DAC_RGB_CSET
12<	10>	DACA_RED_DVI	1	750HM	DAC_RGB_CSET
12<	10>	DACA_GREEN_DVI	1	750HM	DAC_RGB_CSET
12<	10>	DACA_BLUE_DVI	1	750HM	DAC_RGB_CSET
		DACA_HSYNC	2	500HM	
		DACA_VSYNC	2	500HM	
		DACA_HS_BUF	2	500HM	
		DACA_VS_BUF	2	500HM	
		DACA_HS_BUF_R	2	500HM	
		DACA_VS_BUF_R	2	500HM	
12<	10>	DACA_HS_DVI	2	500HM	
12<	10>	DACA_VS_DVI	2	500HM	
		DACA_I2C_SCL			
		DACA_I2C_SDA			
		DACA_I2C_SCL_R			
		DACA_I2C_SDA_R			
12<	10>	DACA_I2C_SCL_DVI			
12<	10>	DACA_I2C_SDA_DVI			
		DACA_VREF			
		DACA_RSET			
		NET	VOLTAGE	MAX_CURRENT	MI N_WI DTH
DAC_VDDO		DAC_VDD	3.3V	0.25A	16MI L

ASSEMBLY	G71-GS - 256MB-8Mx32 GDDR3, DVI-I-L-DL + DVI-I-L-DL + HDTV, 450/700 MHz for Dell HMG
PAGE DETAIL	DACA Interface

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

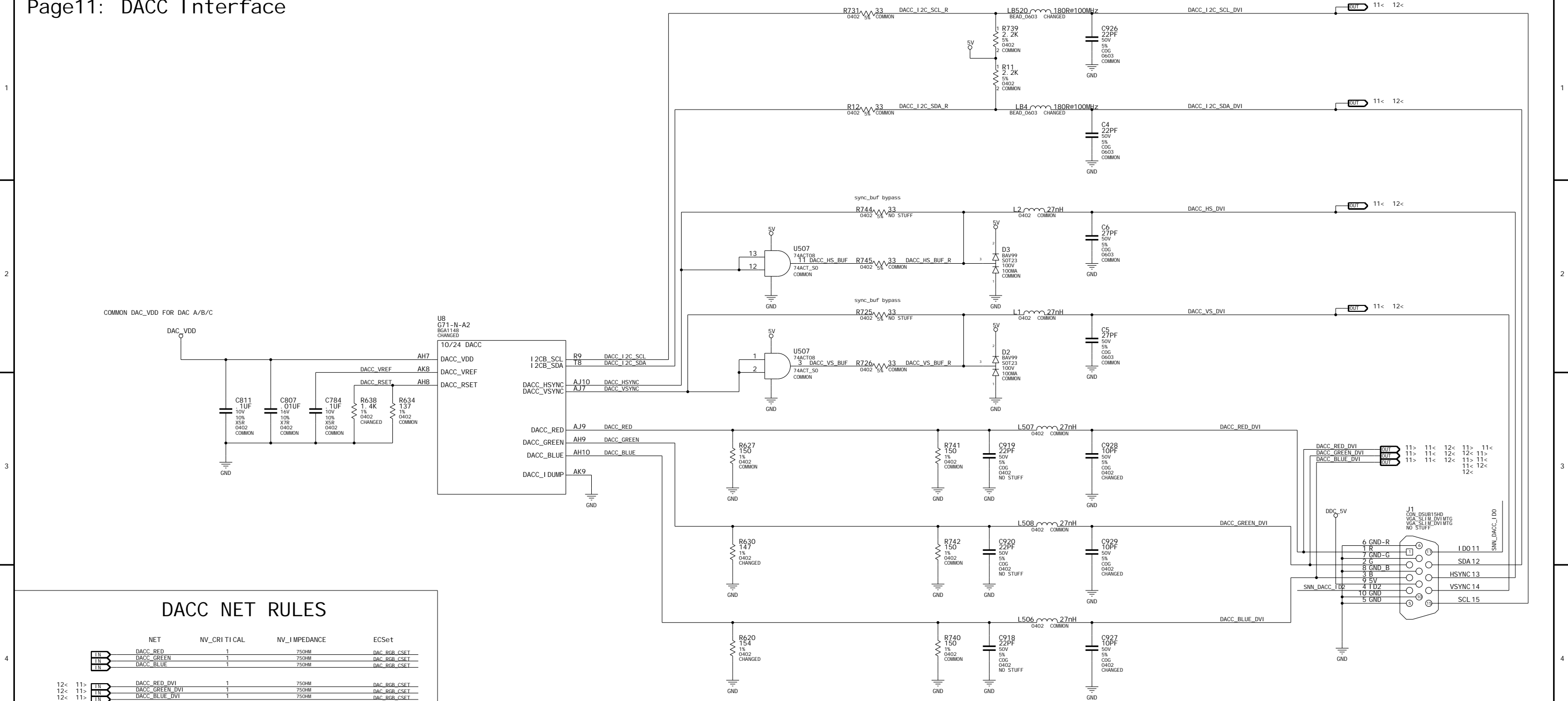
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



NV_PN	600-10455-0002-001
-------	--------------------

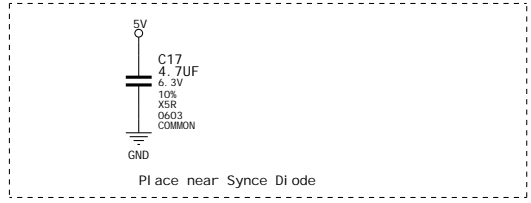
ID	deslgn	PAGE	10 OF 24
NAME	LFarasati	DATE	9-FEB-2006

Page11: DACC Interface



DACC NET RULES

NET	NV_CRTICAL	NV_IMPEDANCE	ECSet
DACC_RED	1	75OHM	DAC_RGB_CSET
DACC_GREEN	1	75OHM	DAC_RGB_CSET
DACC_BLUE	1	75OHM	DAC_RGB_CSET
DACC_RED_DVI	1	75OHM	DAC_RGB_CSET
DACC_GREEN_DVI	1	75OHM	DAC_RGB_CSET
DACC_BLUE_DVI	1	75OHM	DAC_RGB_CSET
DACC_HSYNC	2	50OHM	
DACC_VSYNC	2	50OHM	
DACC_HS_BUF	2	50OHM	
DACC_VS_BUF	2	50OHM	
DACC_HS_BUF_R	2	50OHM	
DACC_VS_BUF_R	2	50OHM	
DACC_HS_DVI	2	50OHM	
DACC_VS_DVI	2	50OHM	
DACC_I2C_SCL			
DACC_I2C_SDA			
DACC_I2C_SCL_R			
DACC_I2C_SDA_R			
DACC_I2C_SCL_DVI			
DACC_I2C_SDA_DVI			
DACC_VREF			
DACC_RSET			



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

ASSEMBLY

G71-GS - 256MB-8Mx32 GDDR3, DVI-I-DL + DVI-I-DL + HDTV, 450/700 MHz for Dell HMG

PAGE DETAIL

DACC Interface

NV_PN

600-10455-0002-001

ID

design

PAGE

11 OF 24

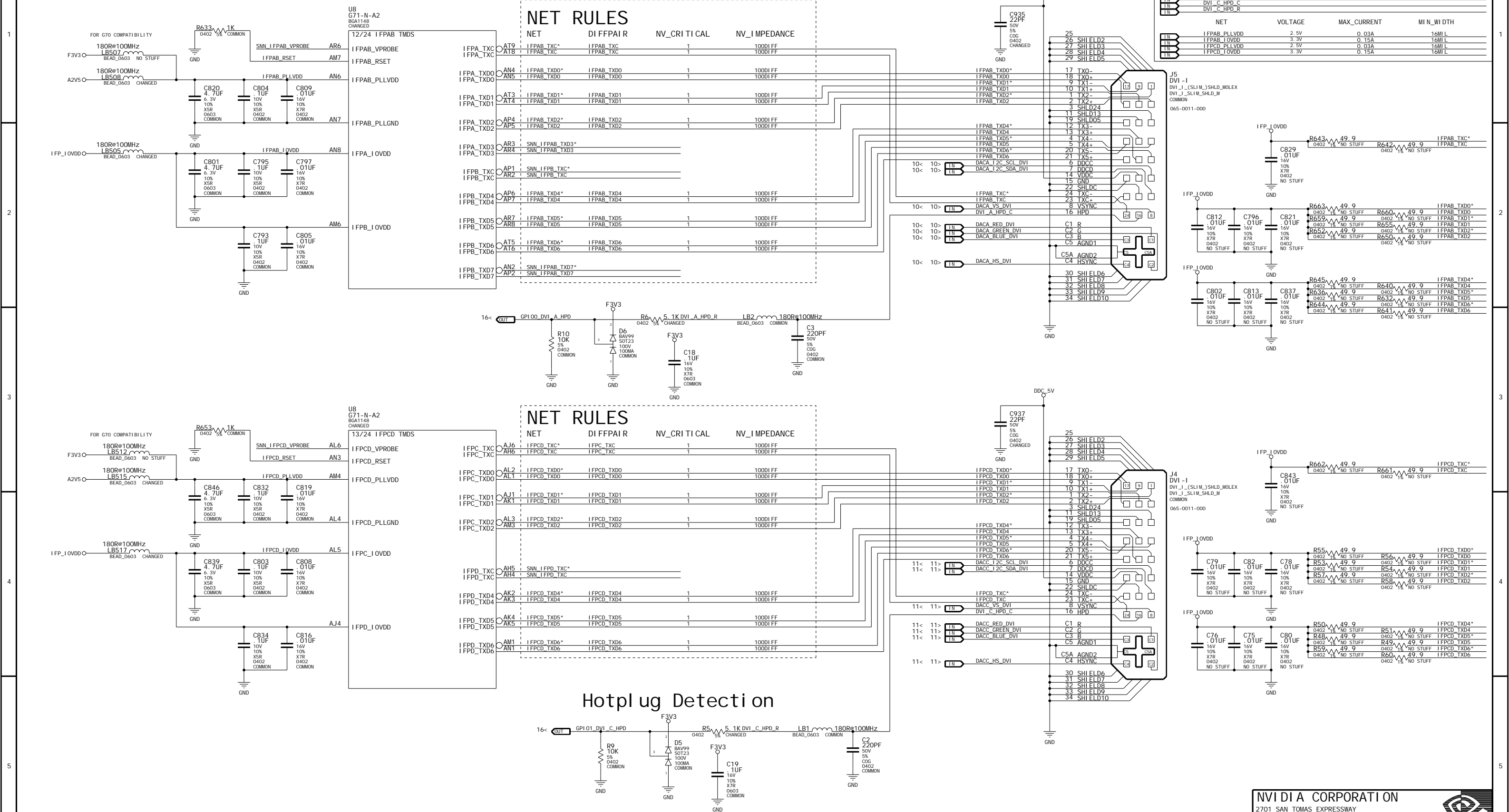
NAME

Lfarasati

DATE

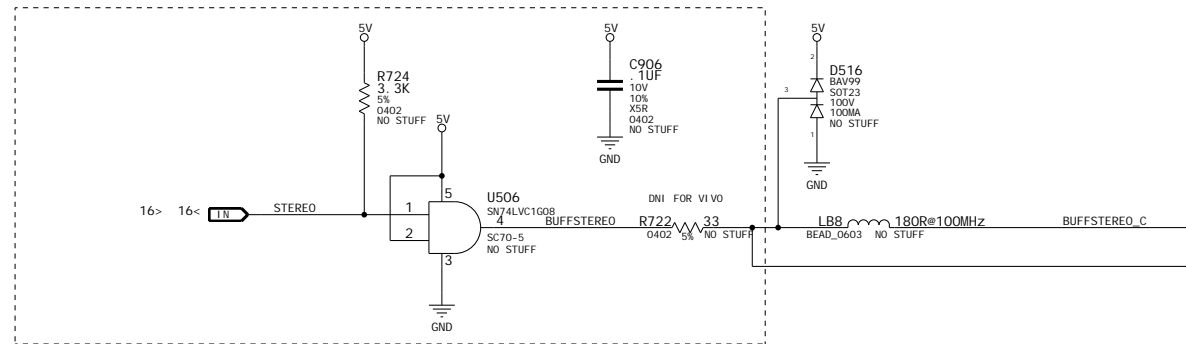
9-FEB-2006

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

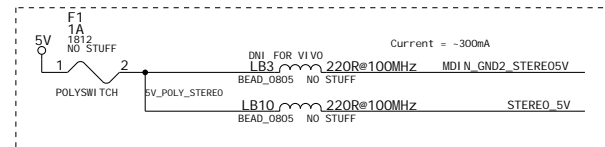


Page13: DACB and Stereo Interface

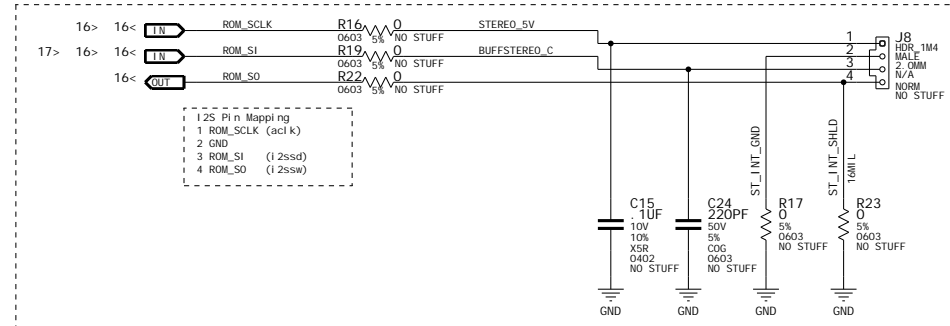
Stereo 3D



Stereo 5V



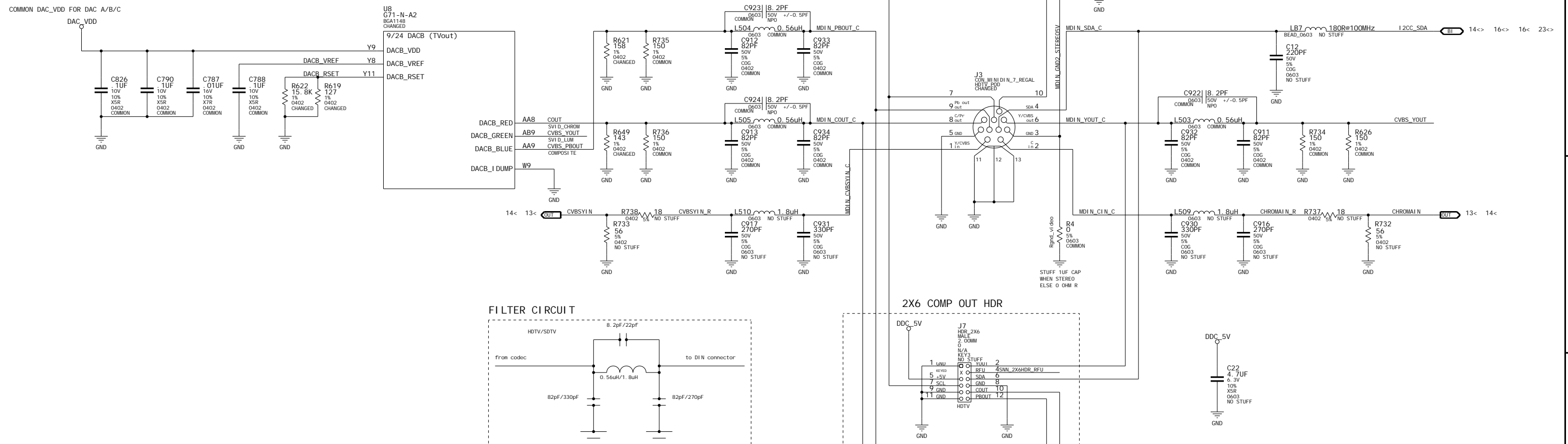
Internal Stereo Out/ I2S (Optional)



DACB & STEREO NET RULES

		NET	NV_CRI T I C A L	NV_I M P E D A N C E	ECSet
14<		IN_COUT	1	750HM	DACB_RGB_CSET
		MDI N_COUT_C	1	750HM	DACB_RGB_CSET
		CVBS_YOUT	1	750HM	DACB_RGB_CSET
		MDI N_YOUT_C	1	750HM	DACB_RGB_CSET
		CVBS_PBOUT	1	750HM	DACB_RGB_CSET
		MDI N_PBOUT_C	1	750HM	DACB_RGB_CSET
	13>	CVBSYIN	1	500HM	
		CVBSYIN_R	1	500HM	
		MDI N_CVBSYIN_C	1	500HM	
	14<	13>	CHROMA I N	1	500HM
CHROMA I N_R			1	500HM	
MDI N_C I N_C			1	500HM	
		I2CC_SCL_BUFFSTEREO_R			
	MDI N_SCL_C_STEREO				
	BUFFSTEREO				
	BUFFSTEREO_C				
	MDI N_SDA_C				

NET		VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	5V_POLY_STEREO	5.0V	0.03A	16MIL
IN	STEREO_5V	5.0V	0.03A	16MIL
IN	MDI_N_GND2_STEREO5V	0.0V		16MIL
IN	ST_INT_GND	0.0V		16MIL
IN	ST_INT_SHLD	0.0V		16MIL
IN	DACB_VREF			16MIL
IN	DACB_RSET			16MIL
IN	MDI_N_GND	0.0V		16MIL























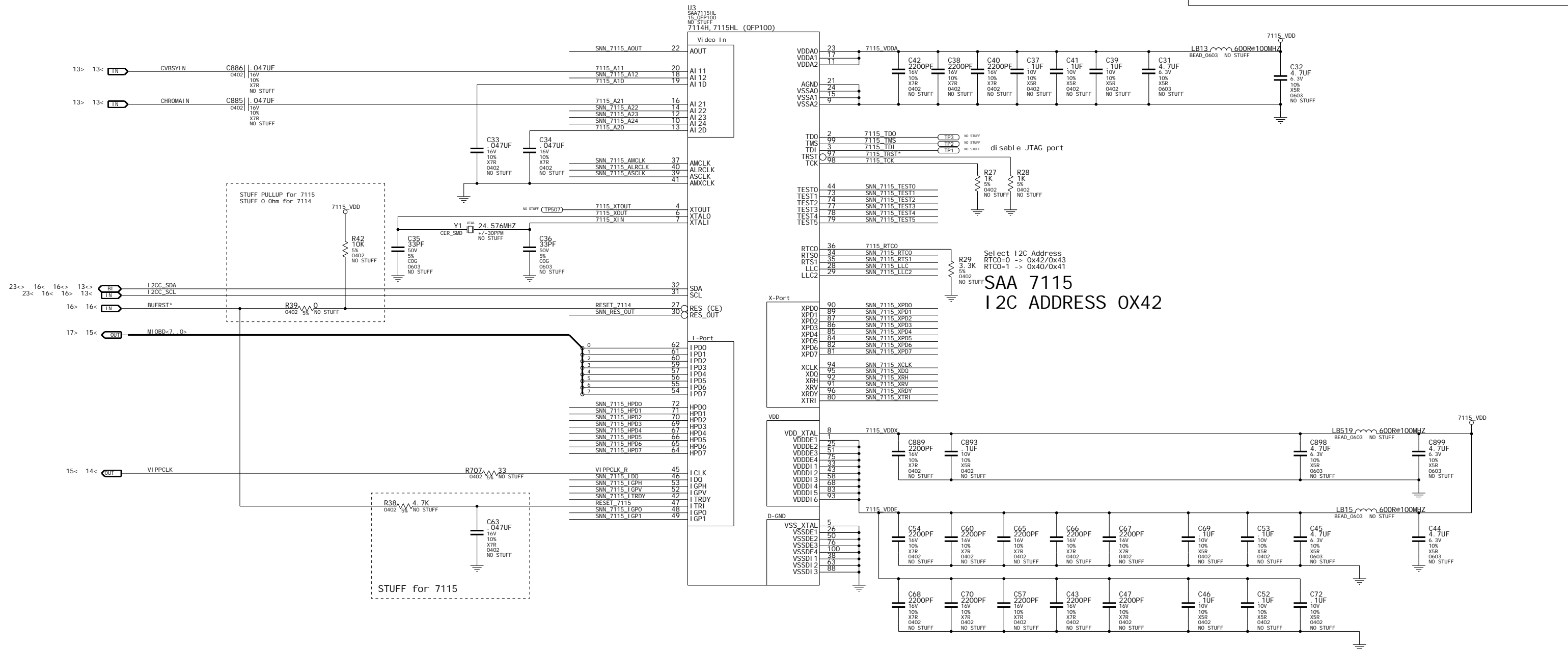
NVI DI A CORPORATION ON 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN 600-10455-0002-001				
ID	description		PAGE	13 OF 24
NAME	Lfarasati		DATE	9-FEB-2006

VIDEO CAPTURE

SAA7115 NET RULES

14>
15<

	NET	NV_CRI T1 CAL	NV_I IMPEDANCE	DI_FFPAI R
	V1PPCLK_R	1	500HM	
	V1PPCLK	1	500HM	
	7115_A11	2	500HM	
	7115_A1D	2	500HM	
	7115_A2D	2	500HM	
	7115_A2I	2	500HM	
	7115_XOUT	1	500HM	
	7115_XIN	1	500HM	
	RESET_7114	2	500HM	
	RESET_7115	2	500HM	
	7115_TRST*	2	500HM	
	7115_TCK	2	500HM	
	7115_RTCD	2	500HM	
	7115_TMS			
	7115_TDO			
	7115_TDI			
	7115_XTOUT			
	NET	VOLTAGE	MAX_CURRENT	MIN_WI_DTH
	7115_VDDA	3.3V	0.09A	16MI L
	7115_VDDE	3.3V	0.08A	16MI L
	7115_VDDX	3.3V	0.01A	16MI L



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

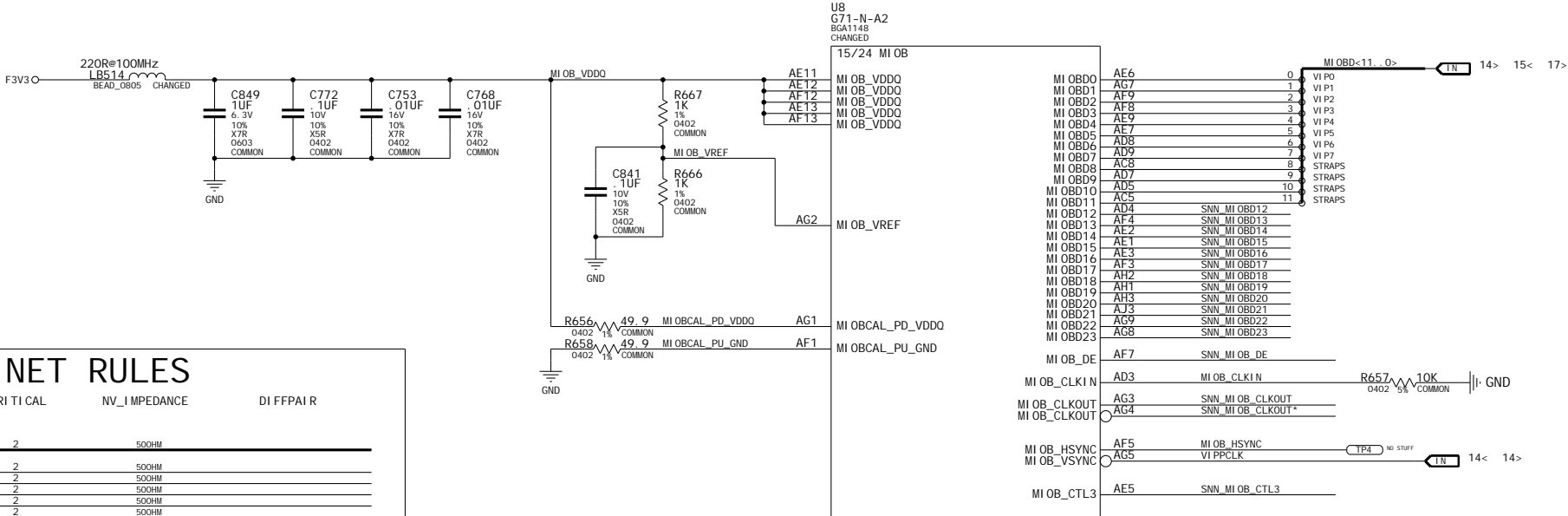
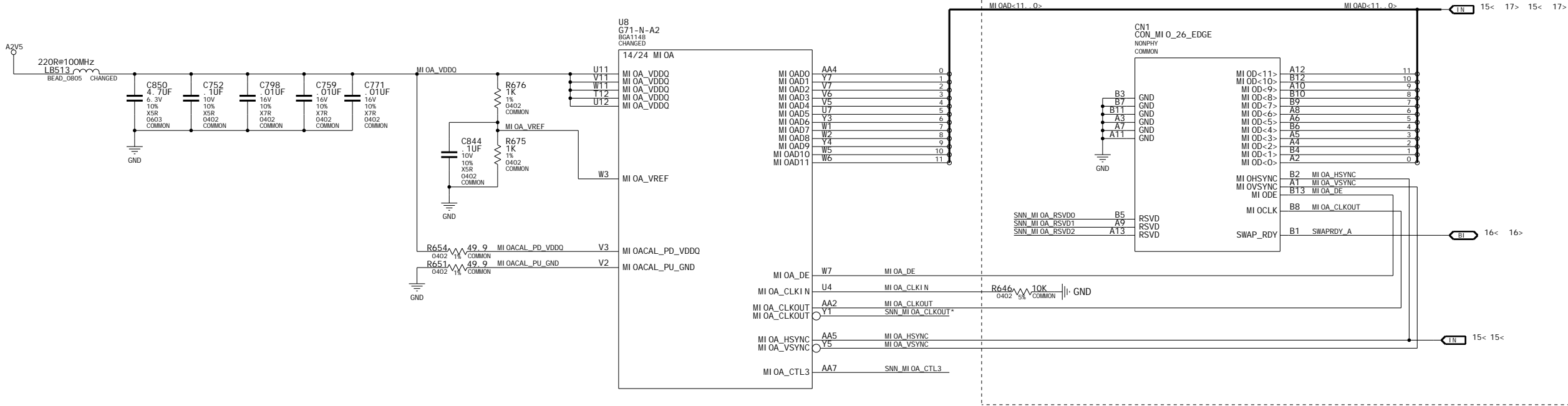
SANTA CLARA, CA 95050, USA

NV_PN	600-10455-0002-001
-------	--------------------

ID	design	PAGE	14 OF 24
NAME	LFarasati	DATE	9-FEB-2006

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

MI O Feature Connector



MI O NET RULES

NET	NV_CRI TICAL	NV_I MPEDANCE	DI FFPAI R
MI OAD<11... 0>	2	50OHM	
MI OA_CLKI N	2	50OHM	
MI OA_CLKOUT	2	50OHM	
MI OA_DE	2	50OHM	
MI OA_HSYNC	2	50OHM	
MI OA_VSYNC	2	50OHM	
MI OBD<11... 0>	2	50OHM	
MI OB_CLKI N	2	50OHM	
MI OB_HSYNC			
NET	VOLTAGE	MAX_CURRENT	MI N_WI DTH
MI OA_VDDQ	2.5V	0.80A	16MI L
MI OA_VREF	1.65V		12MI L
MI OACAL_PD_VDDQ	2.5V		12MI L
MI OACAL_PU_GND	0.0V		12MI L
MI OB_VDDQ	3.3V	0.03A	12MI L
MI OB_VREF	1.65V		12MI L
MI OBCAL_PD_VDDQ	3.3V		12MI L
MI OBCAL_PU_GND	0.0V		12MI L

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

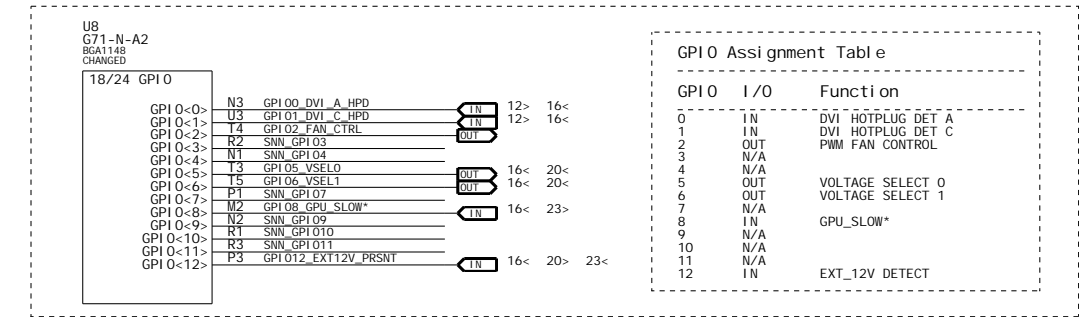
SANTA CLARA, CA 95050, USA



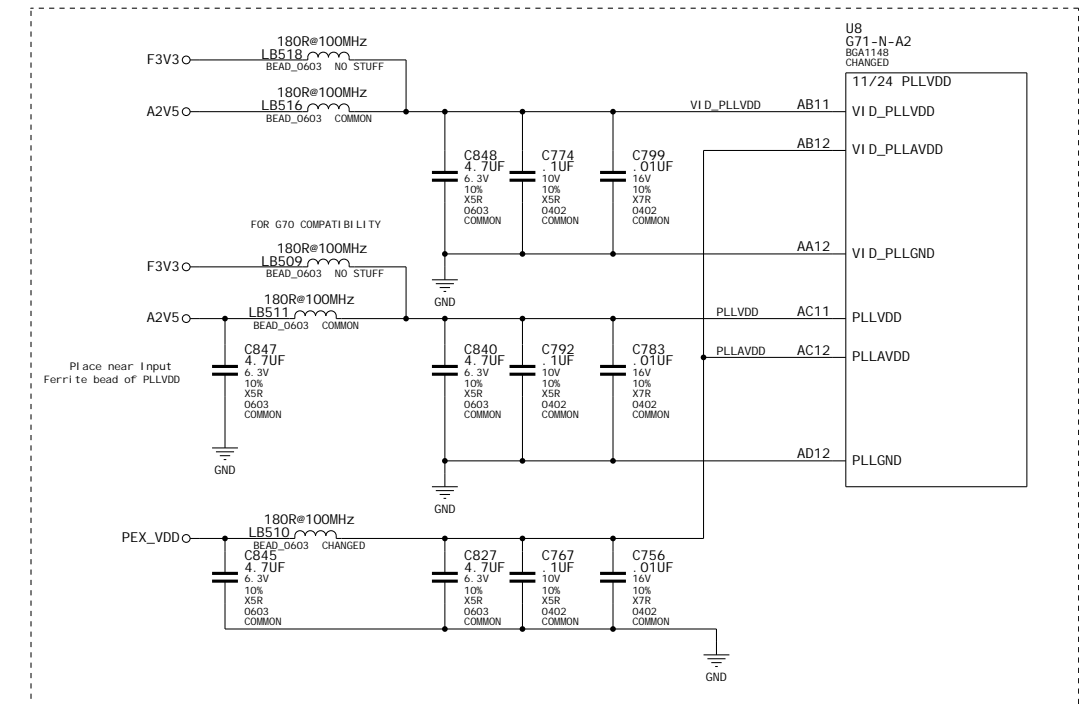
NV_PN 600-10455-0002-001

ID	desi gn	PAGE	15 OF 24
NAME	LFarasati	DATE	9-FEB-2006

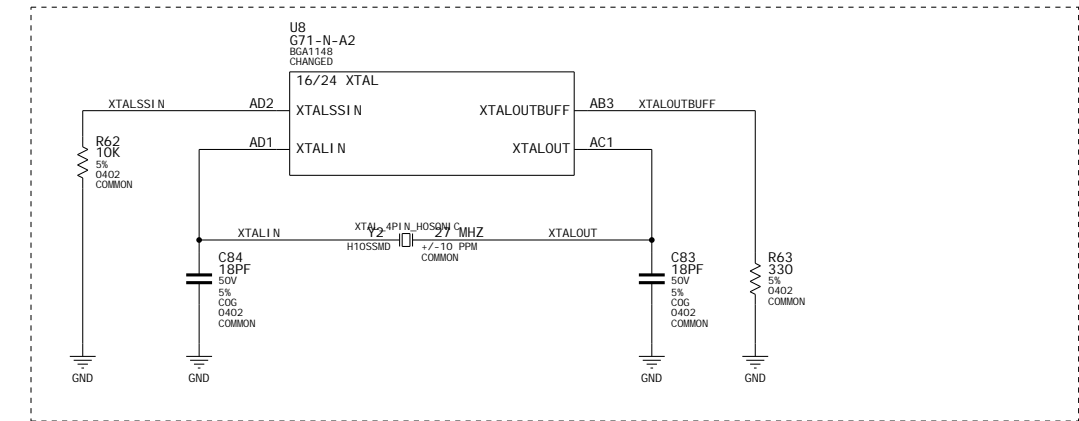
GPI 0



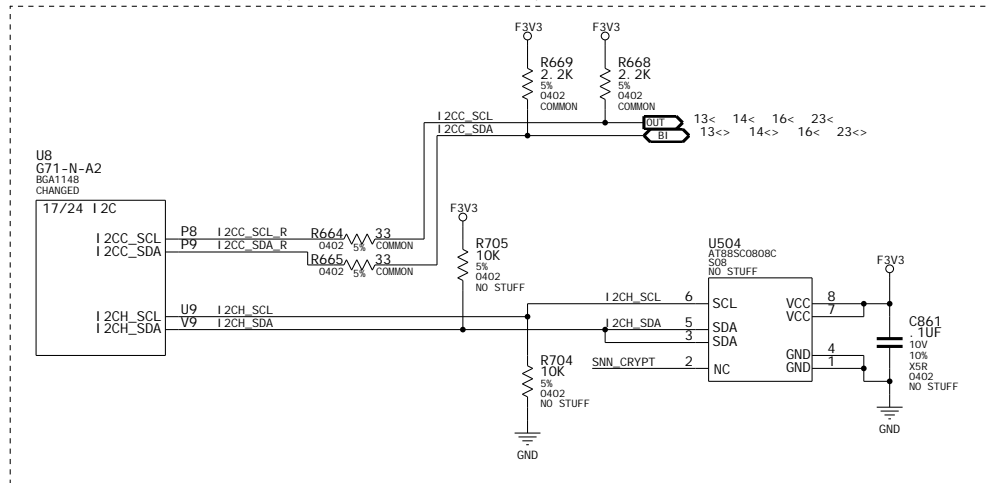
PLLVD D/V I D_P L L V D D



XTAL

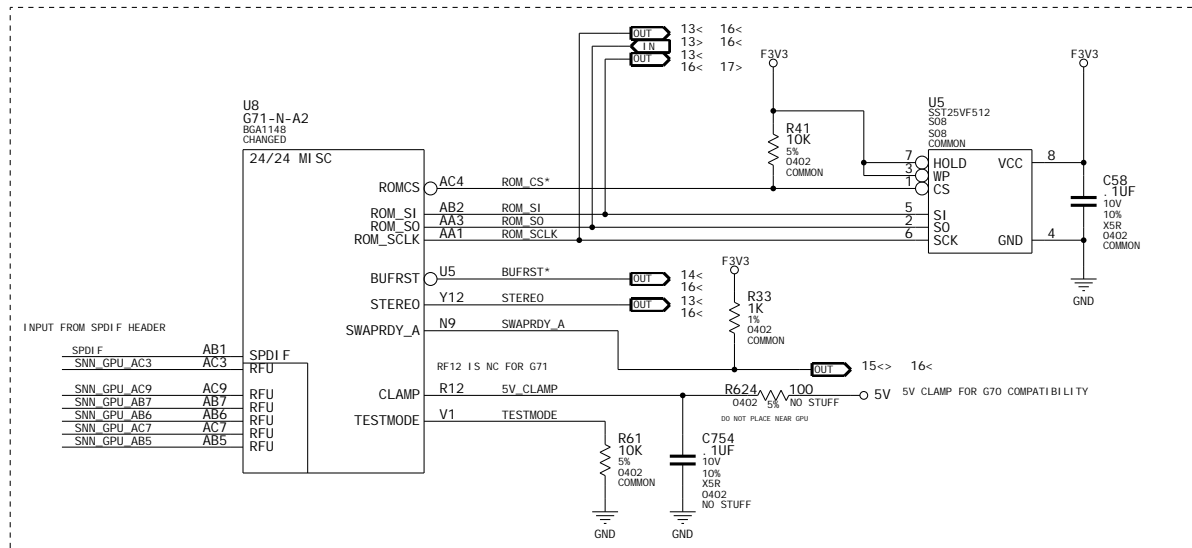


I 2CC / I 2CH(+ HDCP ROM)



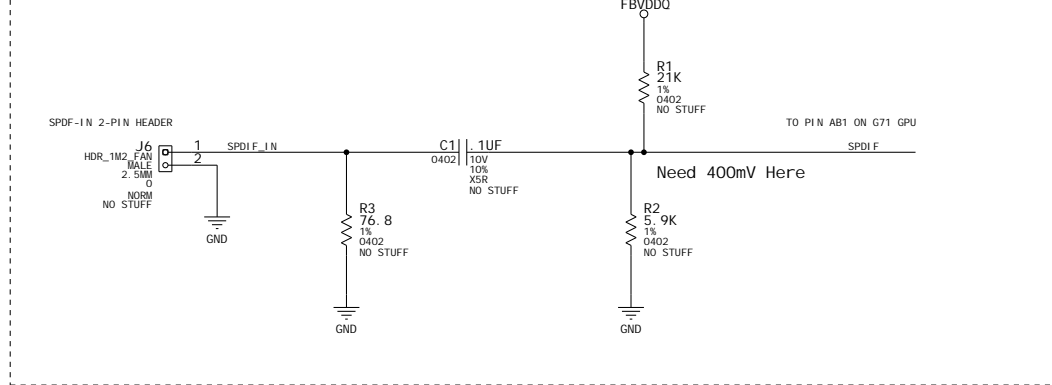
ROM / MISC

(BUFRST/STEREO/SWAPRDY/TESTMODE)



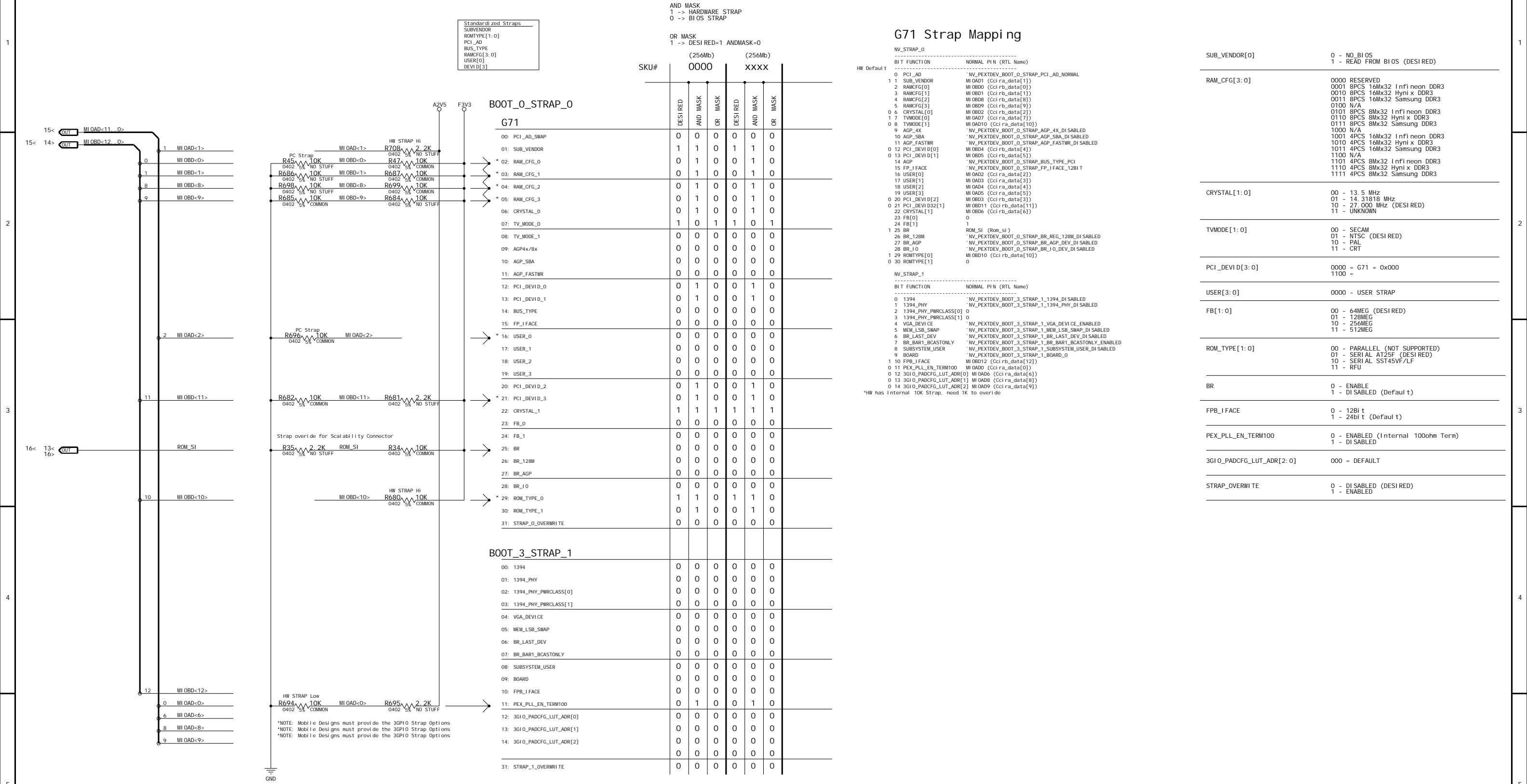
SPDIF INPUT FOR HDMI (OPTIONAL)

NO STUFF FOR G70



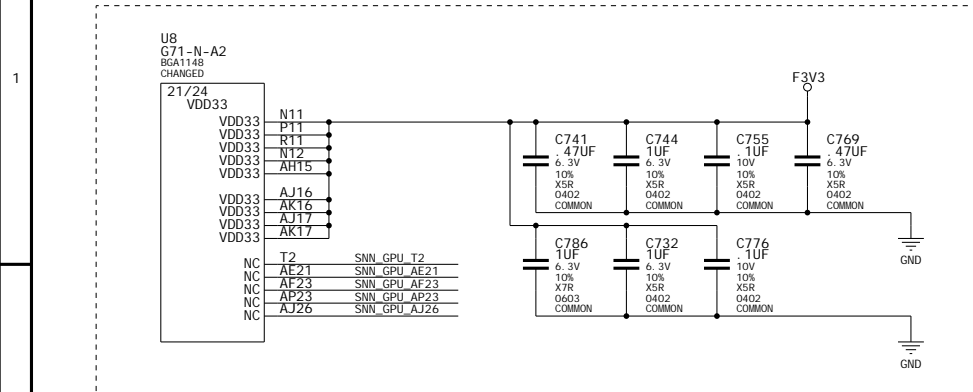
MISC NET RULES

	NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
23<	16>	12CC_SCL		
14<>	13<	12CC_SDA		
23<>	16<>	12CC_SCL_R		
		12CC_SDA_R		
		12CH_SCL		
		12CH_SDA		
		ROM_CS*		
16<	13<	ROM_SI		
16<	13>	ROM_SO		
16>	13<	ROM_SCLK		
		BUFRST*		
16>	14<	STEREO		
16>	13<	SWAPRDY_A		
16>	15<>	TESTMODE		
16<	12>	GPI00_DVI_A_HPD		
16<	12>	GPI01_DVI_C_HPD		
20<	16>	GPI05_VSELO		
20<	16>	GPI06_VSEL1		
23<	16>	GPI08_GPU_SLOW*		
23<	16>	GPI02_FAN_CTRL		
20>	16>	GPI012_EXT12V_PRSNT		
23<				
		XTALSSIN	1	500HM
		XTALIN	1	500HM
		XTALOUT	1	500HM
		XTALOUTBUFF		
		SPDIF_IN		
		SPDIF		
	NET	VOLTAGE	MAX_CURRENT	MI N_WI DTH
	VI D_PLLVDD	2.5V	0.03A	12MI L
	PLLVD	2.5V	0.03A	12MI L
	PLLVDD	1.2V		10MI L
	5V_CLAMP	5V		16MI L

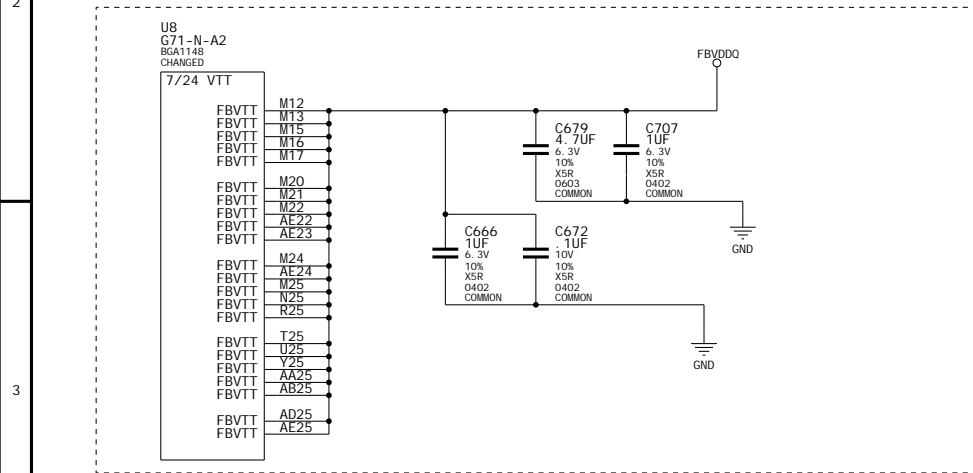


Page18: Power/GND and Decoupling

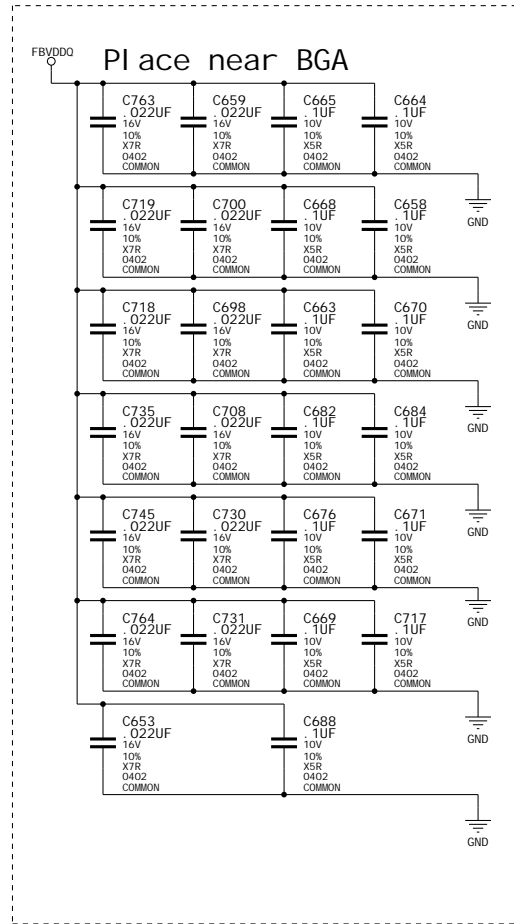
VDD33



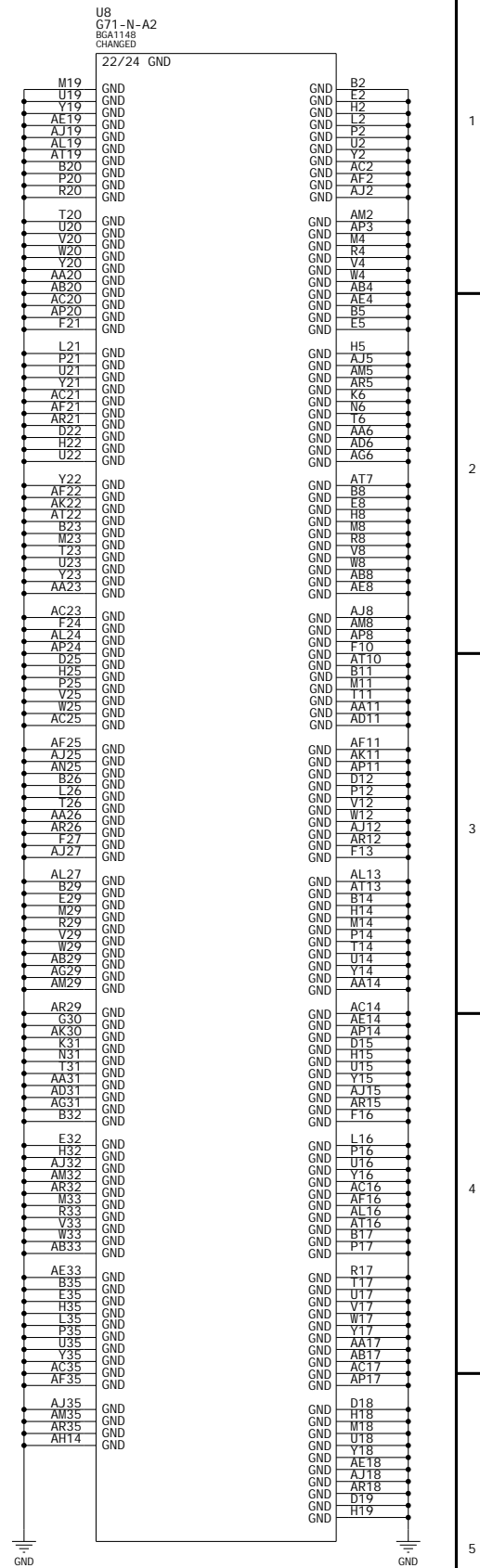
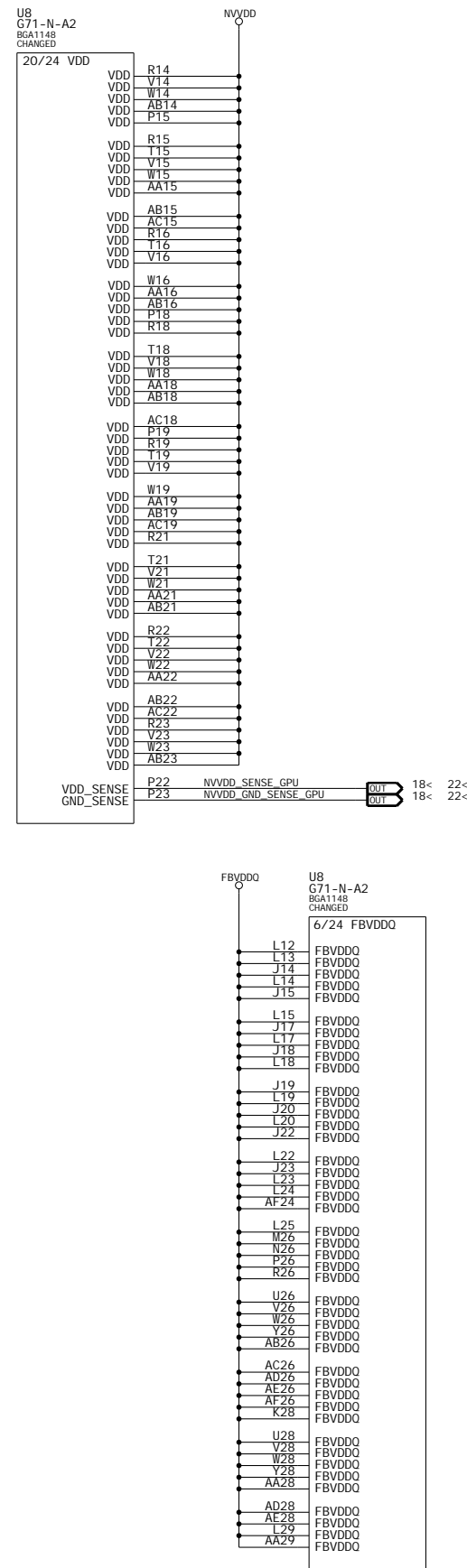
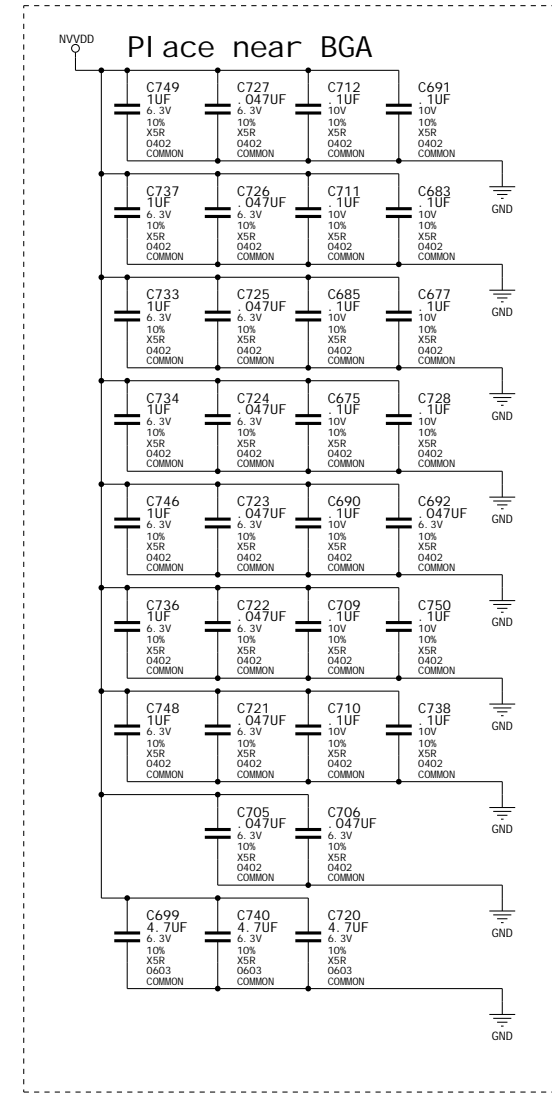
FBVTT




FBVDDQ




NVVDD



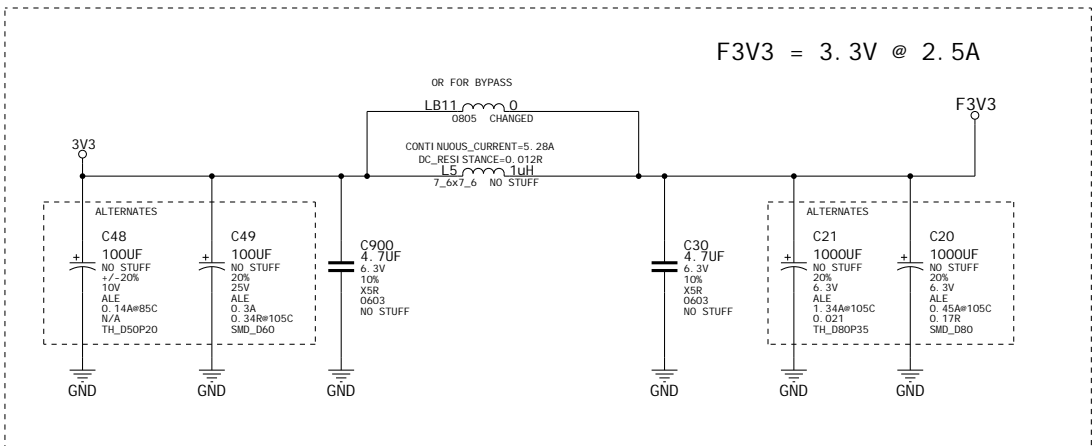
		NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
22<	18>		NVDD_SENSE_GPU		
22<	18>		NVDD_GND_SENSE_GPU		

ASSEMBLY	G71-GS - 256MB-8Mx32 GDDR3, DVI-I-DL + DVI-I-DL + HDTV, 450/700 MHz for Dell HMG
PAGE DETAIL	Power/GND and Decoupling

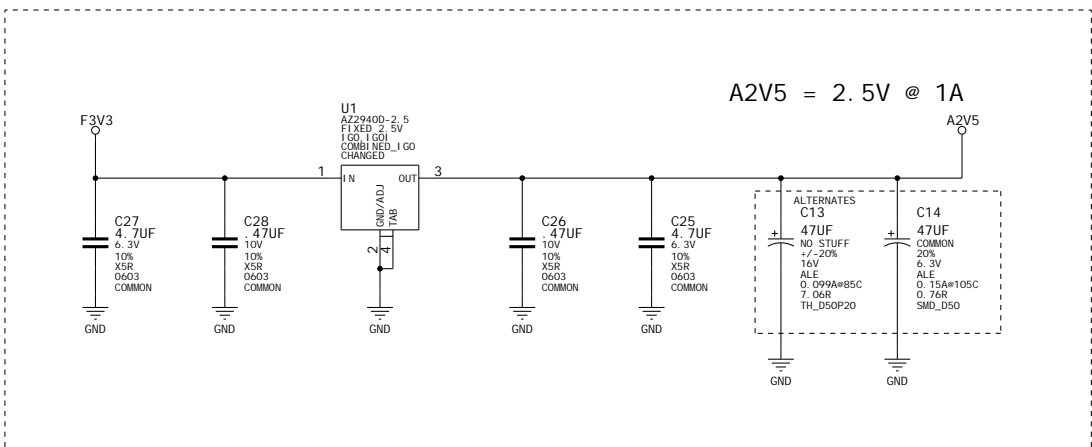
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVI DI A CORPORATI ON			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-10455-0002-001		
ID	design	PAGE	18 OF 24
NAME	LFarasati	DATE	9-FEB-2006

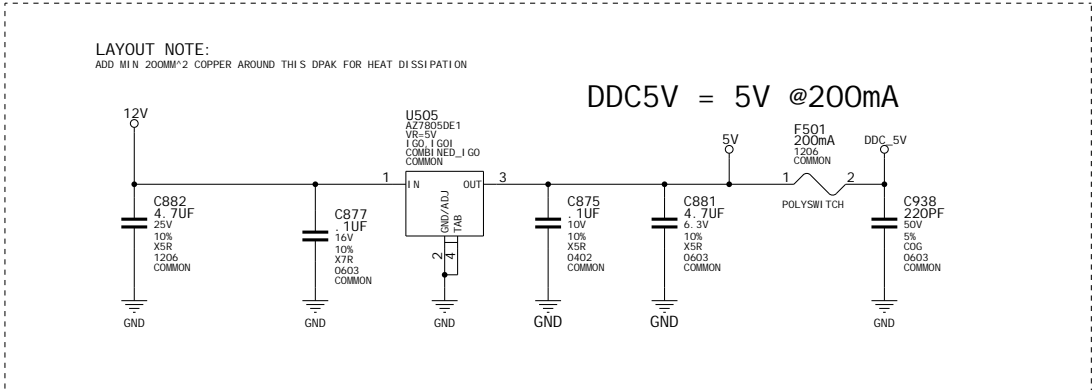
F3V3 Supply



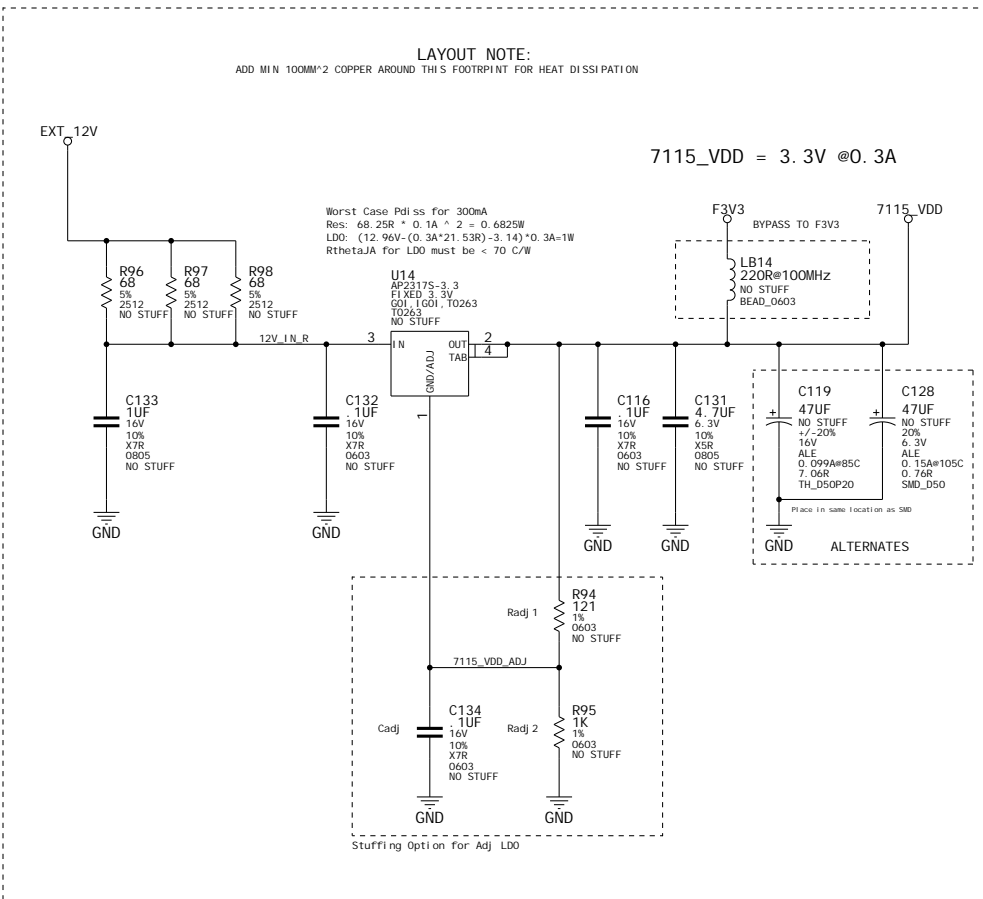
A2V5 Supply



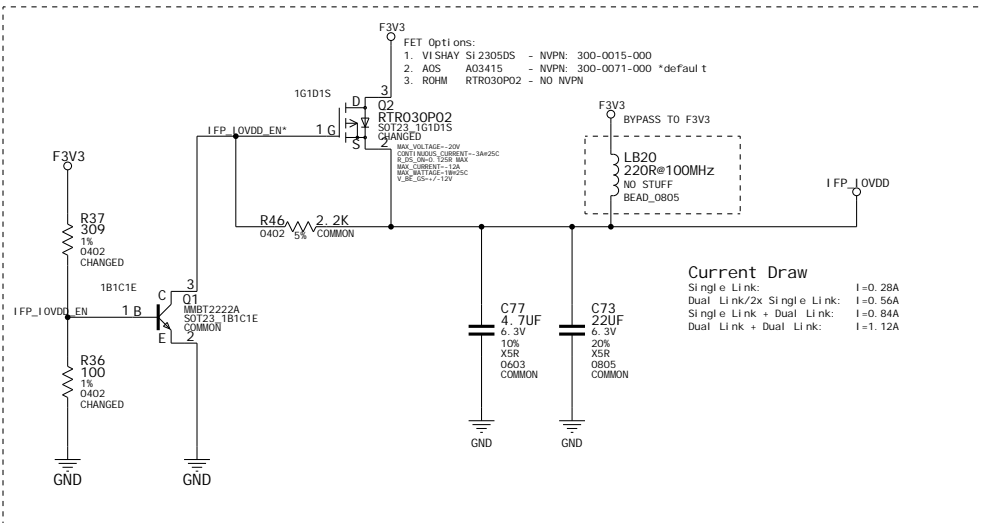
5V and DDC5V Supply



SAA7115_VDD Supply



TMDS IOVDD Backdrive Prevention



POWER NET RULES

F3V3 NET RULES	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
F3V3	F3V3	3.3V	2.5A	16MIL
7115_VDD	7115_VDD	3.3V	0.3A	12MIL
7115_VDD_ADJ	7115_VDD_ADJ			10MIL
12V_IN_R	12V_IN_R			12MIL

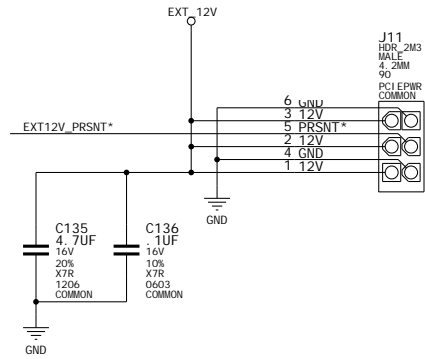
IFP_IOVDD NET RULES	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFP_IOVDD	IFP_IOVDD	3.3V	1.2A	16MIL
IFP_IOVDD_EN	IFP_IOVDD_EN			10MIL
IFP_IOVDD_EN*	IFP_IOVDD_EN*			10MIL

5V and DDC5V NET RULES	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
5V	5V	5.0V	0.1A	16MIL
DDC_5V	DDC_5V	5.0V	0.1A	16MIL

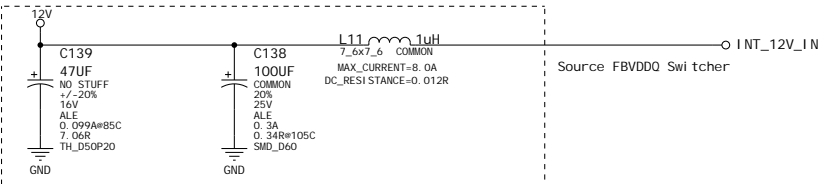
A2V5 NET RULES	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
A2V5	A2V5	2.5V	1.0A	16MIL



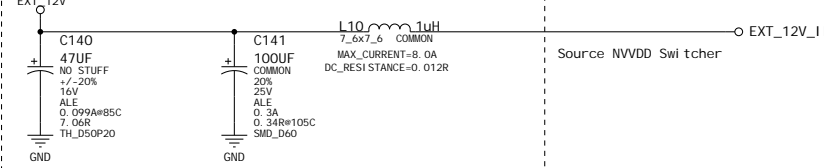
Internal & External 12V Input Filters



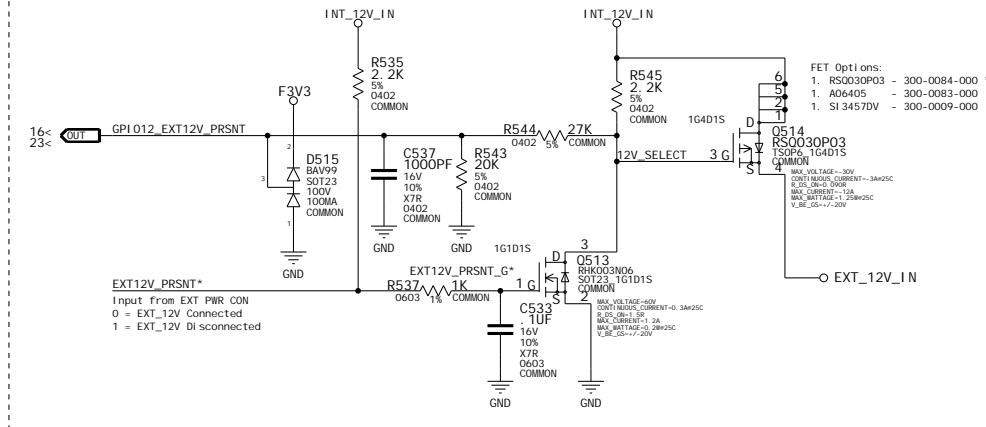
INPUT FILTER FOR INTERNAL 12V



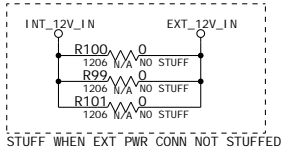
INPUT FILTER FOR EXTERNAL 12V



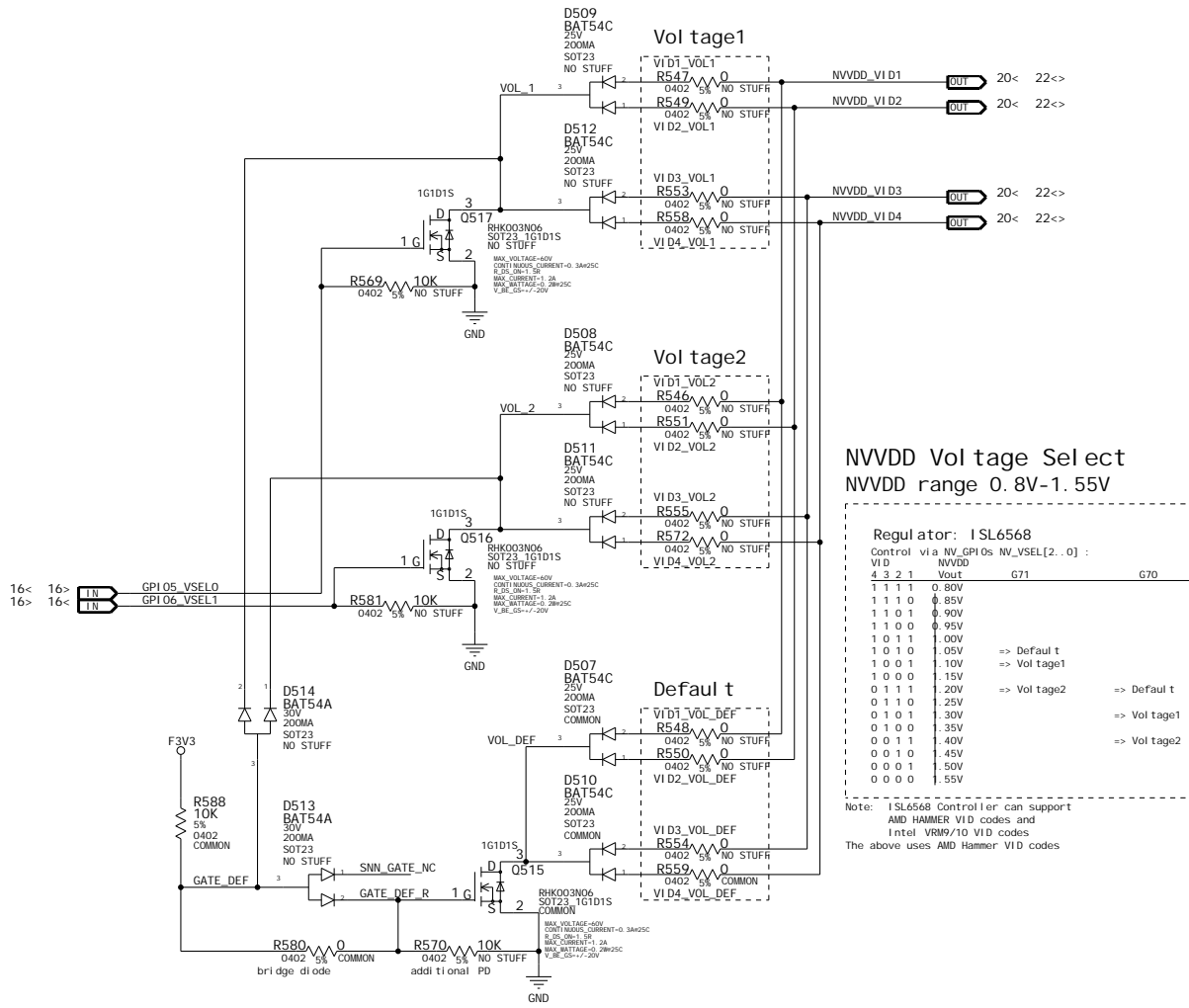
12V Input Selection for NVVDD



Bypass External Connector



NVVDD VI D CONTROL



NVDD Voltage Selection
NVDD range 0.8V-1.55V

```

Regulator: ISL6568
Control via NV_GPIOs NV_NVS[2..0]
VID      NVVID      Vout      G71      G70
4 3 2 1
1 1 1 1 0.80V
1 1 1 0 0.85V
1 1 0 1 0.90V
1 1 0 0 0.95V
1 0 1 1 1.00V
1 0 1 0 1.05V    => Default t
1 0 0 1 1.10V    => Vol tage1
1 0 0 0 1.15V
0 1 1 1 1.20V
0 1 1 0 1.25V    => Vol tage2
0 1 0 1 1.30V    => Vol tage1
0 1 0 0 1.35V
0 0 1 1 1.40V    => Vol tage2
0 0 1 0 1.45V
0 0 0 1 1.50V
0 0 0 0 1.55V

```

Note: ISL6568 Controller can support
AMD HAMMER VID codes and
Intel VRM9/10 VID codes
The above uses AMD Hammer VID codes

	NET	VOLTAGE	MAX_CURRENT	MIN_LENGTH_WARNING
EXT_12V_O	EXT_12V	12V	5.5A	50MIL
INT_12V_IN_O	INT_12V_IN	12V	8A	50MIL
EXT_12V_IN_O	EXT_12V_IN	12V	8A	50MIL

	NET	NV_CRI TI CAL	NV_I IMPEDANCE	DI FFPAIR R
22<>	20>	1IN	NVDD_VI D1	
22<>	20>	1IN	NVDD_VI D2	
22<>	20>	1IN	NVDD_VI D3	
22<>	20>	1IN	NVDD_VI D4	
		1IN	VOL_1	
		1IN	VI D1_VOL1	
		1IN	VI D2_VOL1	
		1IN	VI D3_VOL1	
		1IN	VI D4_VOL1	
		1IN	VOL_2	
		1IN	VI D1_VOL2	
		1IN	VI D2_VOL2	
		1IN	VI D3_VOL2	
		1IN	VI D4_VOL2	
		1IN	VOL_DEF	
		1IN	VI D1_VOL_DEF	
		1IN	VI D2_VOL_DEF	
		1IN	VI D3_VOL_DEF	
		1IN	VI D4_VOL_DEF	
		1IN	GATE_DEF	
		1IN	GATE_DEF_R	
		1IN	12V_SELECT	
		1IN	EXT12V_PRSNT*	
		1IN	EXT12V_PRSNT*_G*	

Default selection for NVVDD_VID[4..1]

ASSEMBLY	G71-GS - 256MB-8Mx32 GDDR3, DVI-I-DL + DVI-I-DL + HDTV, 450/700 MHz for Dell HMC
PAGE DETAIL	Power Supply II: PEX Input Filters, External 12V Power, NVDD VID Control

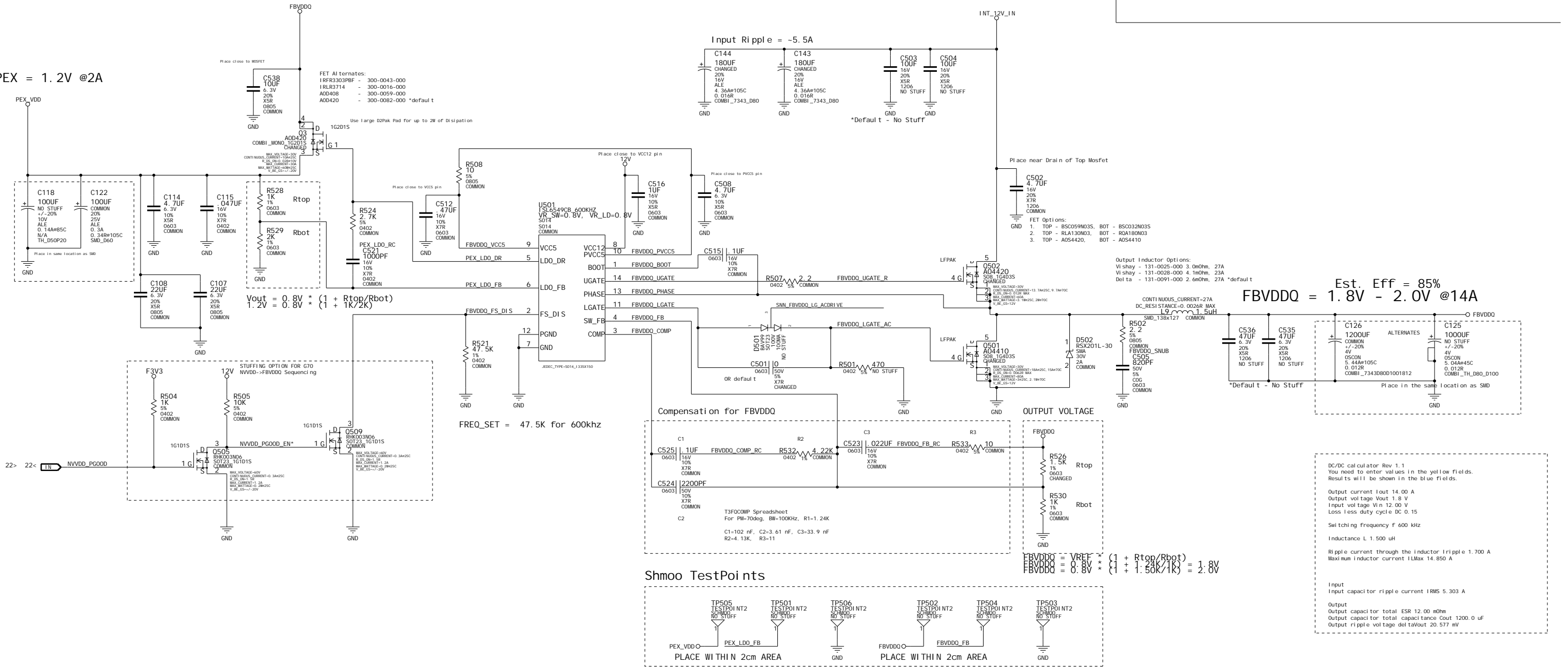
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARD.

Page21: Power Supply III: FBVDDQ & PEX_VDD

FBVDDQ and PEX_VDD NET RULES

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBVDDQ NET RULES	FBVDDQ	1.8V	14A	16MIL
	FBVDDQ_VCC5	5V		12MIL
	FBVDDQ_PVCC5	5V		12MIL
	FBVDDQ_FS_D1S			10MIL
	NVDDQ_PG00D_EN*			10MIL
	FBVDDQ_BOOT			12MIL
	FBVDDQ_UGATE			16MIL
	FBVDDQ_UGATE_R			16MIL
	FBVDDQ_LGATE			16MIL
	FBVDDQ_LGATE_AC			16MIL
	FBVDDQ_SNUB			12MIL
	FBVDDQ_PHASE	1.8V	14A	12MIL
	FBVDDQ_COMP			12MIL
	FBVDDQ_COMP_RC			12MIL
PEX_VDD NET RULES	PEX_VDD	1.2V	2A	16MIL
	PEX_LDO_DR			12MIL
	PEX_LDO_RC			12MIL
	PEX_LDO_FB			12MIL

PEX = 1.2V @2A



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA



NV_PN 600-10455-0002-001

ID	desgn	PAGE	21 OF 24
NAME	Lfarasati	DATE	9-FEB-2006

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

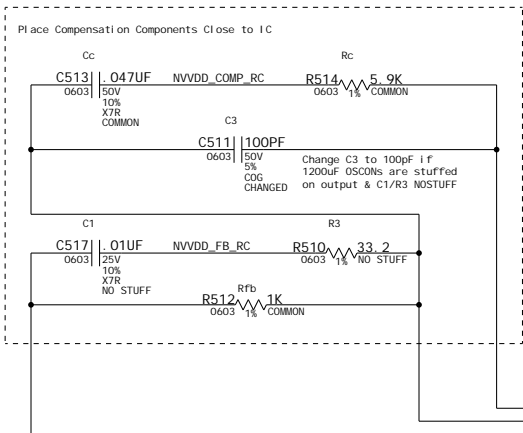
ASSEMBLY	G71-GS - 256MB-8Mx32 GDDR3, DV1-I-DL + DV1-I-DL + HDTV, 450/700 MHz for Del I HMG
PAGE DETAIL	Power Supply III: FBVDDQ and PEX1V2

NVVDD NET RULES

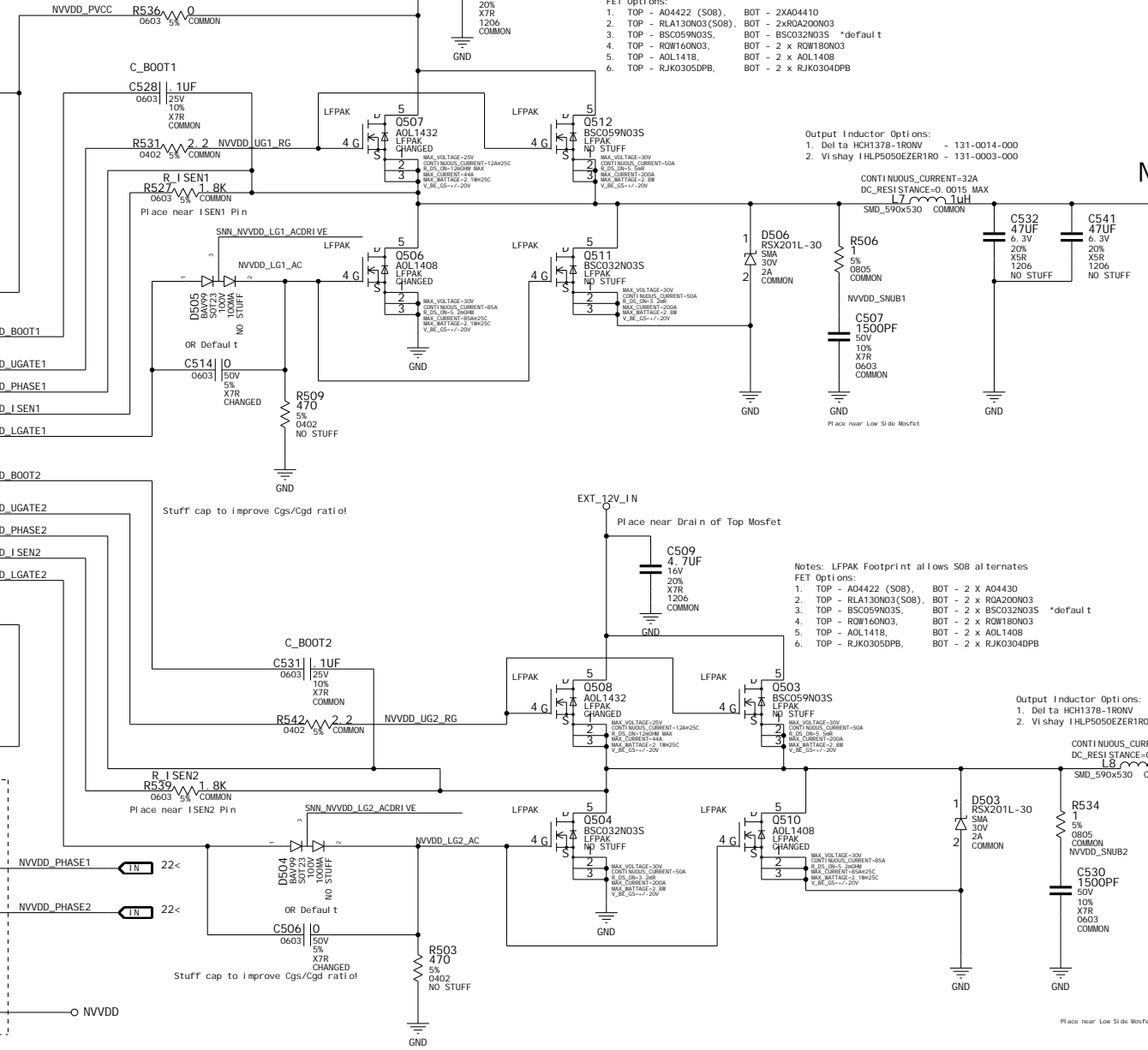
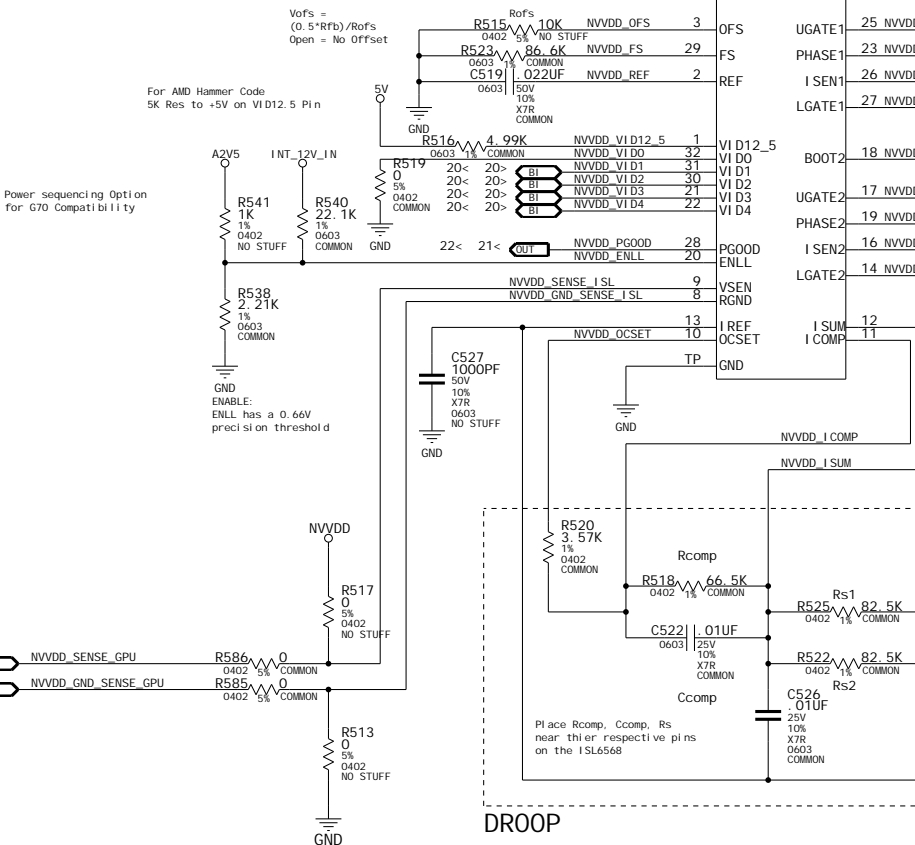
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
NVVDD	1.2V	50A	20MIL
NVVDD_PVCC	12V	0.003A	20MIL
NVVDD_VCC	5V	0.02A	20MIL
NVVDD_BOOT1			20MIL
NVVDD_UGATE1			20MIL
NVVDD_UG1_RG			20MIL
NVVDD_PHASE1	25A		20MIL
NVVDD_LGATE1			20MIL
NVVDD_BOOT2			20MIL
NVVDD_UGATE2			20MIL
NVVDD_UG2_RG	25A		20MIL
NVVDD_PHASE2			20MIL
NVVDD_LG2_AC			20MIL
NVVDD_ISEN1			20MIL
NVVDD_ISEN2			20MIL
NVVDD_SNUB1			12MIL
NVVDD_COMP			12MIL
NVVDD_FB			12MIL
NVVDD_COMP_RC			12MIL
NVVDD_FB_RC			12MIL
NVVDD_VDIFF			12MIL
NVVDD_I_SUM			12MIL
NVVDD_I_COMP			12MIL
NVVDD_OCSET			12MIL
NVVDD_REF			10MIL

NET	NV_CRTICAL	NV_IMPEDANCE	DIFFPAIR
NVVDD_VID0			
NVVDD_VID12_5			
NVVDD_PG00D			
NVVDD_ENLL			
NVVDD_OFS			
NVVDD_FS			
NVVDD_SENSE_I_SL			
NVVDD_GND_SENSE_I_SL			

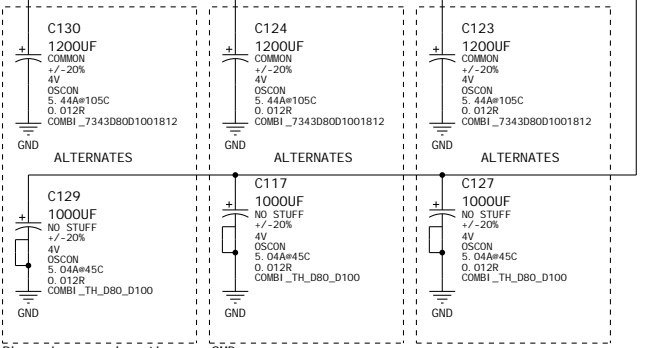
Compensation



Switching Freq = 300KHz/channel



NVVDD = 1.0V..1.2V (30..45A)



NVIDIA CORPORATION

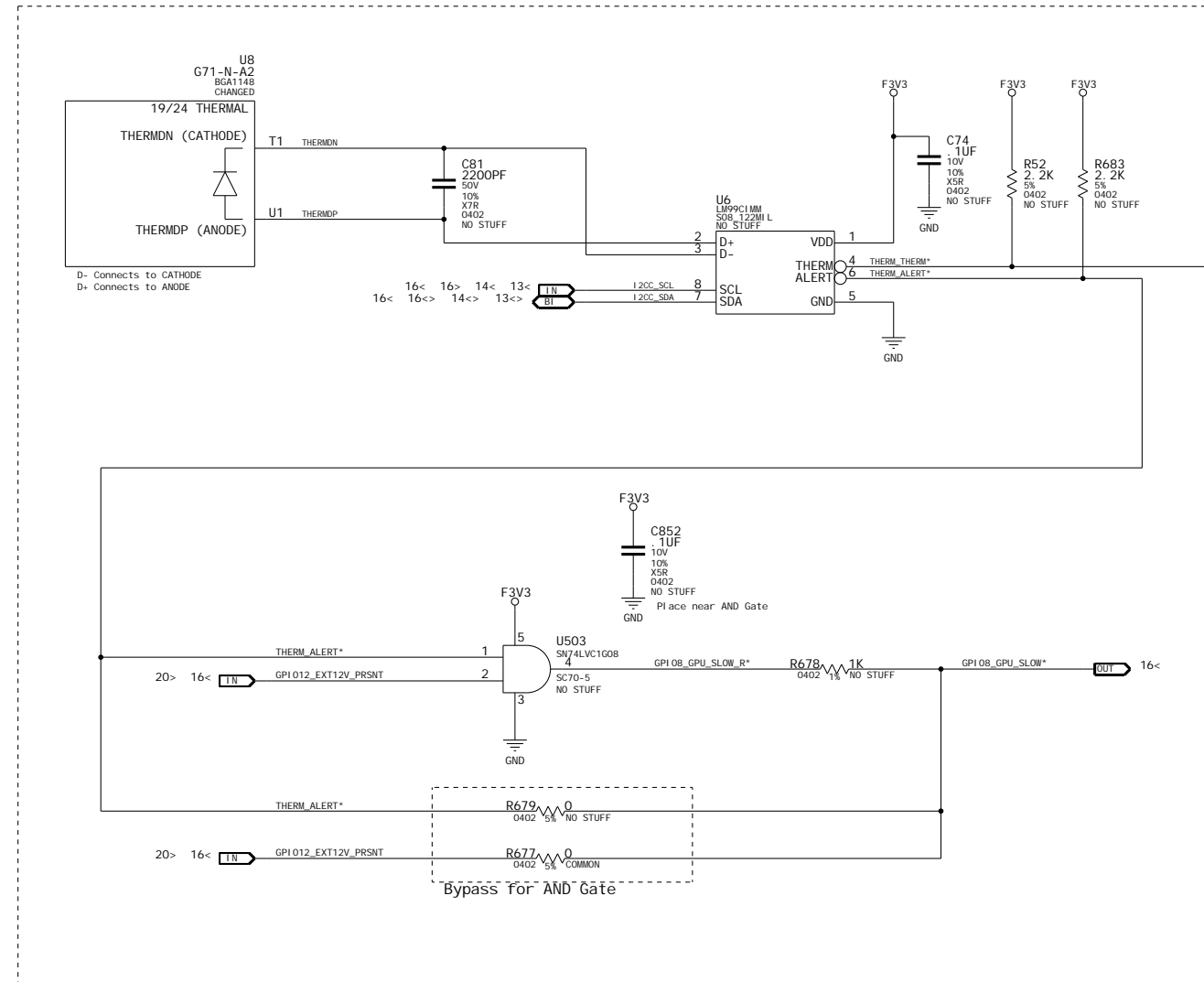
2701 SAN TOMAS EXPRESWAY
SANTA CLARA, CA 95050, USA



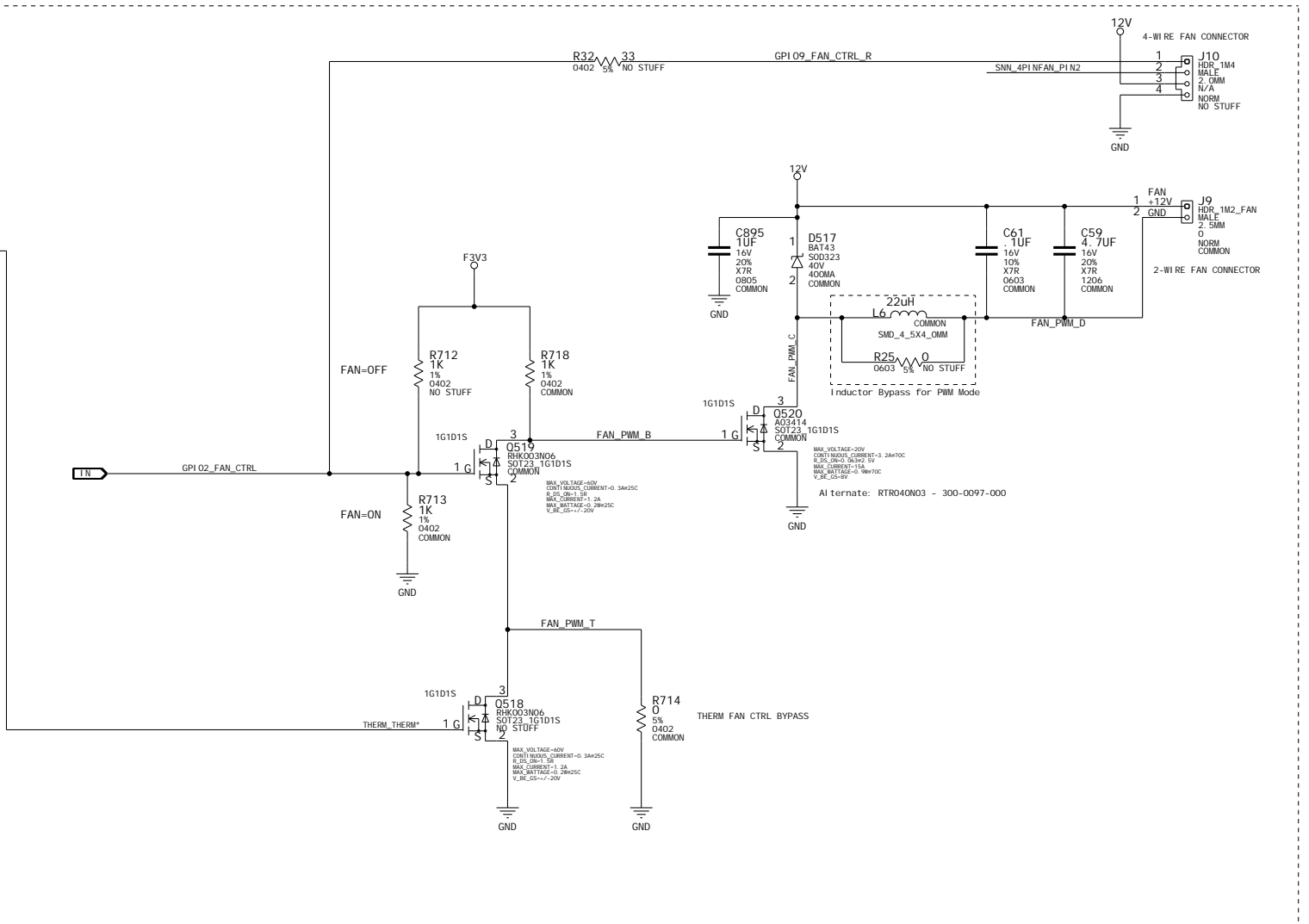
NV_PN	600-10455-0002-001		
ID	desi gn	PAGE	22 OF 24
NAME	LFarasati	DATE	9-FEB-2006

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

EXTERNAL THERMAL DIODE



FAN CONTROL



	NET	NV_CRI T I CAL	NV_I MPEDANCE	DI FFPAI R
	1N	FAN_PWM_B		
	1N	FAN_PWM_C		
	1N	FAN_PWM_D		
	1N	FAN_PWM_T		
23>	1N	THERM_THERM*		
	1N	THERM_ALERT*		
	1N	GPIOB_GPU_SLOW_R*		
	NET			MI N_WI DTH
	1N	THERMDN		10M L
	1N	THERMDP		10M L

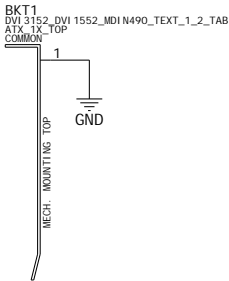
ASSEMBLY	G71-GS - 256MB-8Mx32 GDDR3, DVI-I-DL + DVI-I-DL + HDTV, 450/700 MHz for Dell HMG
PAGE DETAIL	Thermal Diode, Fan Control

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVI DI A CORPORATI ON 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN	600-10455-0002-001		
ID	desi gn	PAGE	23 OF 24
NAME	LFarasati	DATE	9-FEB-2006

Brackets:

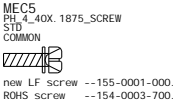
- 151-10001-0006-000 DVI , DVI , MDI N (text - 1-South, 2-North)
- 151-10001-0006-002 DVI , DB15, MDI N



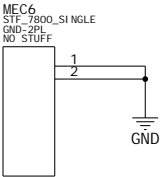
Connector Screws



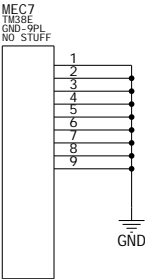
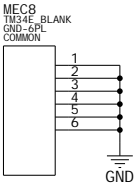
Bracket Screw



Stiffener for WS SKUs



Heatsink



BGA Socket

