

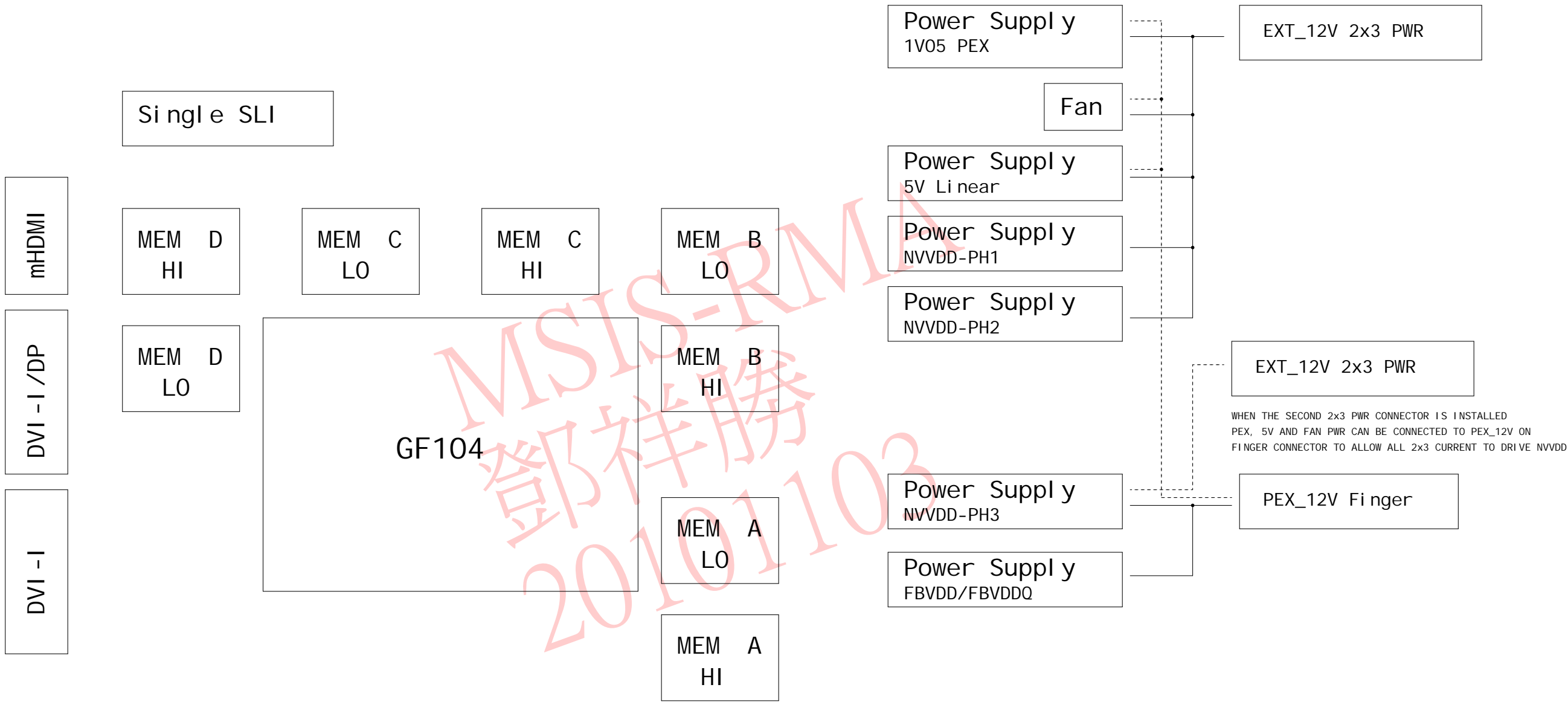
P1041-B01 GF104

GF104-300, 768MB/1536MB, GDDR5 192b 32M/64Mx32
DVI -I -DL, DVI -I -DL/DP, mHDMI

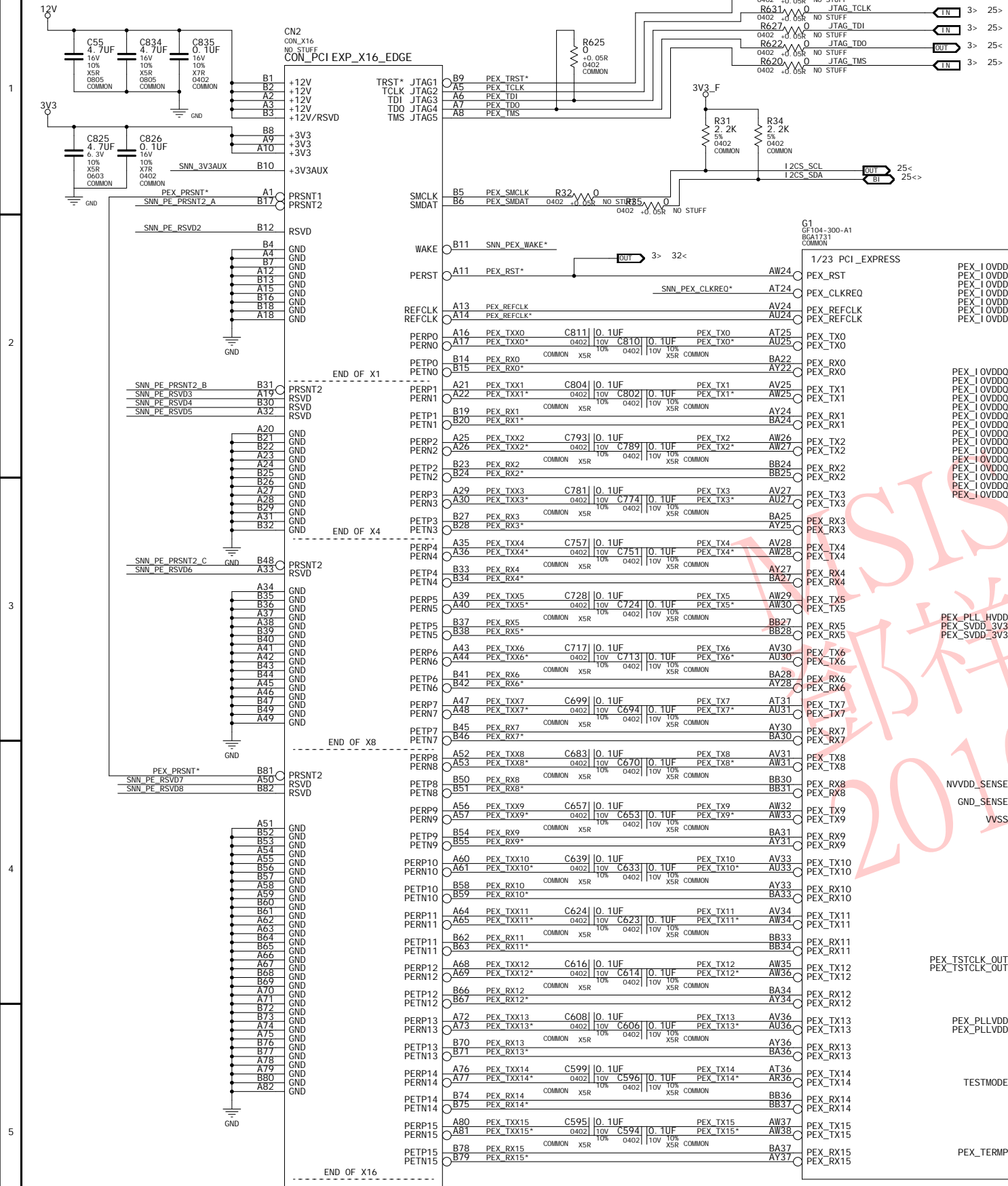
Table of Contents:

- Page 1: Title
- Page 2: Block Diagram
- Page 3: PCI Express
- Page 4: GPU Partition A/B
- Page 5: FBA Partition 31..0
- Page 6: FBA Partition 63..32
- Page 7: FBB Partition 31..0
- Page 8: FBB Partition 63..32
- Page 9: GPU Partition C/D
- Page 10: FBC Partition 31..0
- Page 11: FBC Partition 63..32
- Page 12: FBD Partition 31..0
- Page 13: FBD Partition 63..32
- Page 14: FB Net Properties
- Page 15: GPU PWR and GND
- Page 16: GPU Decoupling
- Page 17: Blank
- Page 18: DACA (South)
- Page 19: DACB (Mid)
- Page 20: IFPAB DVI-DL (South)
- Page 21: IFPEF DVI-DL (Mid)
- Page 22: IFPEF DP (Mid)
- Page 23: IFPC mHDMI (North)
- Page 24: Multi-use IO (MIO) Interface
- Page 25: Misc: Fan, Thermal, JTAG, GPIO
- Page 26: Misc: ROM, HDCP, XTAL, Straps
- Page 27: PS: 5V, PEX_VDD
- Page 28: PS: FBVDD/Q
- Page 29: PS: NVVDD Controller
- Page 30: PS: NVVDD Phase 1-2
- Page 31: PS: NVVDD Phase 3-4
- Page 32: PS: Inputs, Shutdown, IFP
- Page 33: Mechanical: Bracket/Thermal Solution
- Page 34: Blank

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11041-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-11041-0000-300	P1041 GF104-300 768MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
2	SKU0010	600-11041-0010-300	P1041 GF104-350 1024MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
3	QS1	600-11041-0010-QS1	P1041 GF104-350 1024MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>



Page3: PCI Express



PEX NET RULES

NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
PEX_REFCLK	1	90DI FF	PEX_REFCLK
PEX_REFCLK*	1	90DI FF	PEX_REFCLK
PEX_TX0	1	90DI FF	PEX_TX0
PEX_TX0*	1	90DI FF	PEX_TX0
PEX_TX1	1	90DI FF	PEX_TX1
PEX_TX1*	1	90DI FF	PEX_TX1
PEX_TX2	1	90DI FF	PEX_TX2
PEX_TX2*	1	90DI FF	PEX_TX2
PEX_TX3	1	90DI FF	PEX_TX3
PEX_TX3*	1	90DI FF	PEX_TX3
PEX_TX4	1	90DI FF	PEX_TX4
PEX_TX4*	1	90DI FF	PEX_TX4
PEX_TX5	1	90DI FF	PEX_TX5
PEX_TX5*	1	90DI FF	PEX_TX5
PEX_TX6	1	90DI FF	PEX_TX6
PEX_TX6*	1	90DI FF	PEX_TX6
PEX_TX7	1	90DI FF	PEX_TX7
PEX_TX7*	1	90DI FF	PEX_TX7
PEX_TX8	1	90DI FF	PEX_TX8
PEX_TX8*	1	90DI FF	PEX_TX8
PEX_TX9	1	90DI FF	PEX_TX9
PEX_TX9*	1	90DI FF	PEX_TX9
PEX_TX10	1	90DI FF	PEX_TX10
PEX_TX10*	1	90DI FF	PEX_TX10
PEX_TX11	1	90DI FF	PEX_TX11
PEX_TX11*	1	90DI FF	PEX_TX11
PEX_TX12	1	90DI FF	PEX_TX12
PEX_TX12*	1	90DI FF	PEX_TX12
PEX_TX13	1	90DI FF	PEX_TX13
PEX_TX13*	1	90DI FF	PEX_TX13
PEX_TX14	1	90DI FF	PEX_TX14
PEX_TX14*	1	90DI FF	PEX_TX14
PEX_TX15	1	90DI FF	PEX_TX15
PEX_TX15*	1	90DI FF	PEX_TX15
PEX_RX0	1	90DI FF	PEX_RX0
PEX_RX0*	1	90DI FF	PEX_RX0
PEX_RX1	1	90DI FF	PEX_RX1
PEX_RX1*	1	90DI FF	PEX_RX1
PEX_RX2	1	90DI FF	PEX_RX2
PEX_RX2*	1	90DI FF	PEX_RX2
PEX_RX3	1	90DI FF	PEX_RX3
PEX_RX3*	1	90DI FF	PEX_RX3
PEX_RX4	1	90DI FF	PEX_RX4
PEX_RX4*	1	90DI FF	PEX_RX4
PEX_RX5	1	90DI FF	PEX_RX5
PEX_RX5*	1	90DI FF	PEX_RX5
PEX_RX6	1	90DI FF	PEX_RX6
PEX_RX6*	1	90DI FF	PEX_RX6
PEX_RX7	1	90DI FF	PEX_RX7
PEX_RX7*	1	90DI FF	PEX_RX7
PEX_RX8	1	90DI FF	PEX_RX8
PEX_RX8*	1	90DI FF	PEX_RX8
PEX_RX9	1	90DI FF	PEX_RX9
PEX_RX9*	1	90DI FF	PEX_RX9
PEX_RX10	1	90DI FF	PEX_RX10
PEX_RX10*	1	90DI FF	PEX_RX10
PEX_RX11	1	90DI FF	PEX_RX11
PEX_RX11*	1	90DI FF	PEX_RX11
PEX_RX12	1	90DI FF	PEX_RX12
PEX_RX12*	1	90DI FF	PEX_RX12
PEX_RX13	1	90DI FF	PEX_RX13
PEX_RX13*	1	90DI FF	PEX_RX13
PEX_RX14	1	90DI FF	PEX_RX14
PEX_RX14*	1	90DI FF	PEX_RX14
PEX_RX15	1	90DI FF	PEX_RX15
PEX_RX15*	1	90DI FF	PEX_RX15
PEX_TX0	1	90DI FF	PEX_TX0
PEX_TX0*	1	90DI FF	PEX_TX0
PEX_TX1	1	90DI FF	PEX_TX1
PEX_TX1*	1	90DI FF	PEX_TX1
PEX_TX2	1	90DI FF	PEX_TX2
PEX_TX2*	1	90DI FF	PEX_TX2
PEX_TX3	1	90DI FF	PEX_TX3
PEX_TX3*	1	90DI FF	PEX_TX3
PEX_TX4	1	90DI FF	PEX_TX4
PEX_TX4*	1	90DI FF	PEX_TX4
PEX_TX5	1	90DI FF	PEX_TX5
PEX_TX5*	1	90DI FF	PEX_TX5
PEX_TX6	1	90DI FF	PEX_TX6
PEX_TX6*	1	90DI FF	PEX_TX6
PEX_TX7	1	90DI FF	PEX_TX7
PEX_TX7*	1	90DI FF	PEX_TX7
PEX_TX8	1	90DI FF	PEX_TX8
PEX_TX8*	1	90DI FF	PEX_TX8
PEX_TX9	1	90DI FF	PEX_TX9
PEX_TX9*	1	90DI FF	PEX_TX9
PEX_TX10	1	90DI FF	PEX_TX10
PEX_TX10*	1	90DI FF	PEX_TX10
PEX_TX11	1	90DI FF	PEX_TX11
PEX_TX11*	1	90DI FF	PEX_TX11
PEX_TX12	1	90DI FF	PEX_TX12
PEX_TX12*	1	90DI FF	PEX_TX12
PEX_TX13	1	90DI FF	PEX_TX13
PEX_TX13*	1	90DI FF	PEX_TX13
PEX_TX14	1	90DI FF	PEX_TX14
PEX_TX14*	1	90DI FF	PEX_TX14
PEX_TX15	1	90DI FF	PEX_TX15
PEX_TX15*	1	90DI FF	PEX_TX15
PEX_PLL_CLK_OUT	1	90DI FF	PEX_PLL_CLK_OUT
PEX_PLL_CLK_OUT*	1	90DI FF	PEX_PLL_CLK_OUT
PEX_RST*	1	50OHM	PEX_RST*
PEX_TRST*	1	50OHM	PEX_TRST*
PEX_TCLK	1	50OHM	PEX_TCLK
PEX_TDI	1	50OHM	PEX_TDI
PEX_TDO	1	50OHM	PEX_TDO
PEX_TMS	1	50OHM	PEX_TMS
JTAG_TCLK	1	50OHM	JTAG_TCLK
JTAG_TMS	1	50OHM	JTAG_TMS
JTAG_TDI	1	50OHM	JTAG_TDI
JTAG_TDO	1	50OHM	JTAG_TDO
JTAG_TRST*	1	50OHM	JTAG_TRST*
NET	VOLTAGE	MAX_CURRENT	MI_N_WI DTH
12V	12V	5.5A	24MI L
3V3	3V3	3.0A	20MI L
GND	GND	8.5A	16MI L
PEX_PLLVDD	1.05V	0.16A	12MI L

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV_PN

600-11041-0010-QS1

PCB REV

h1041-001

BOM REV

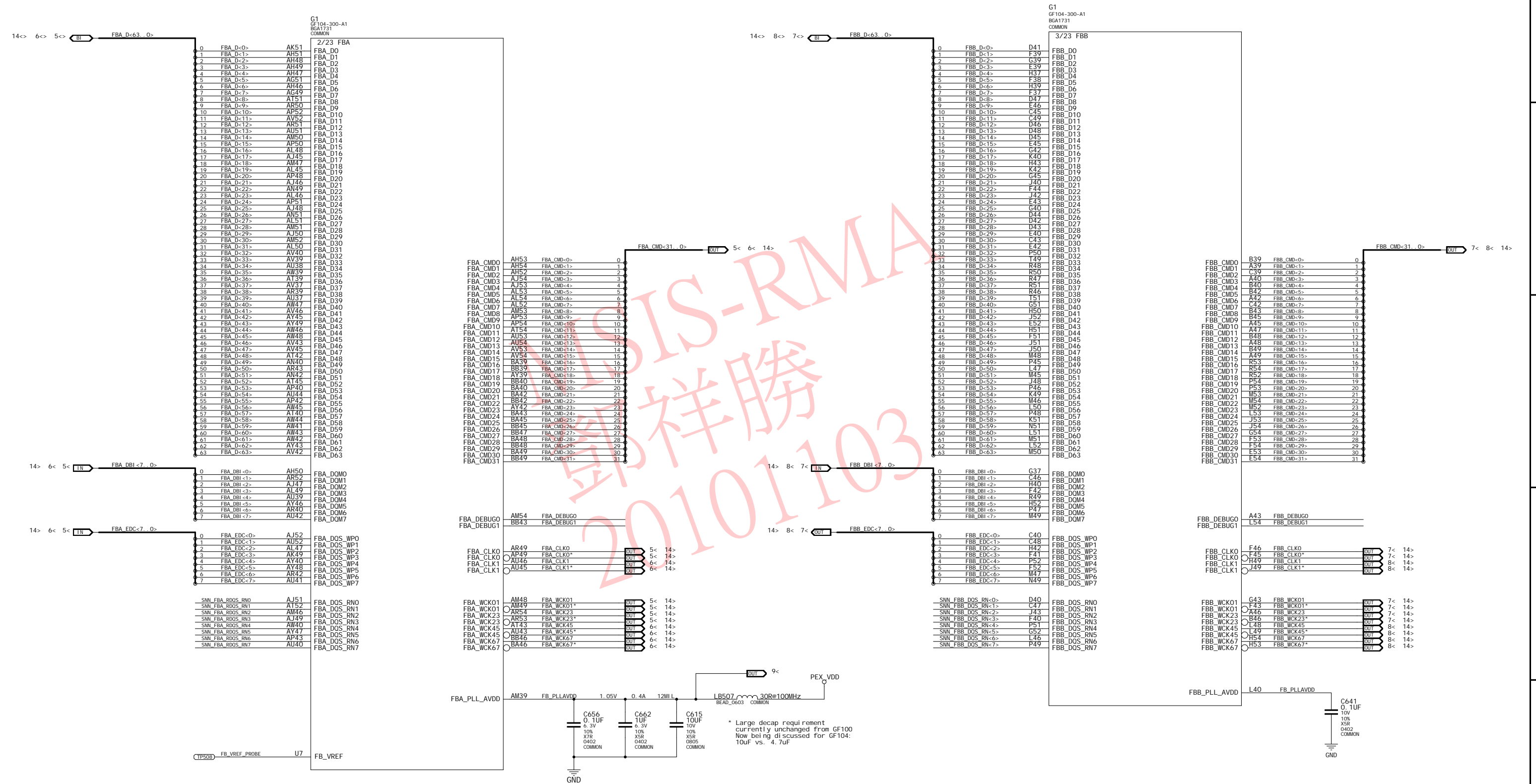
100a2

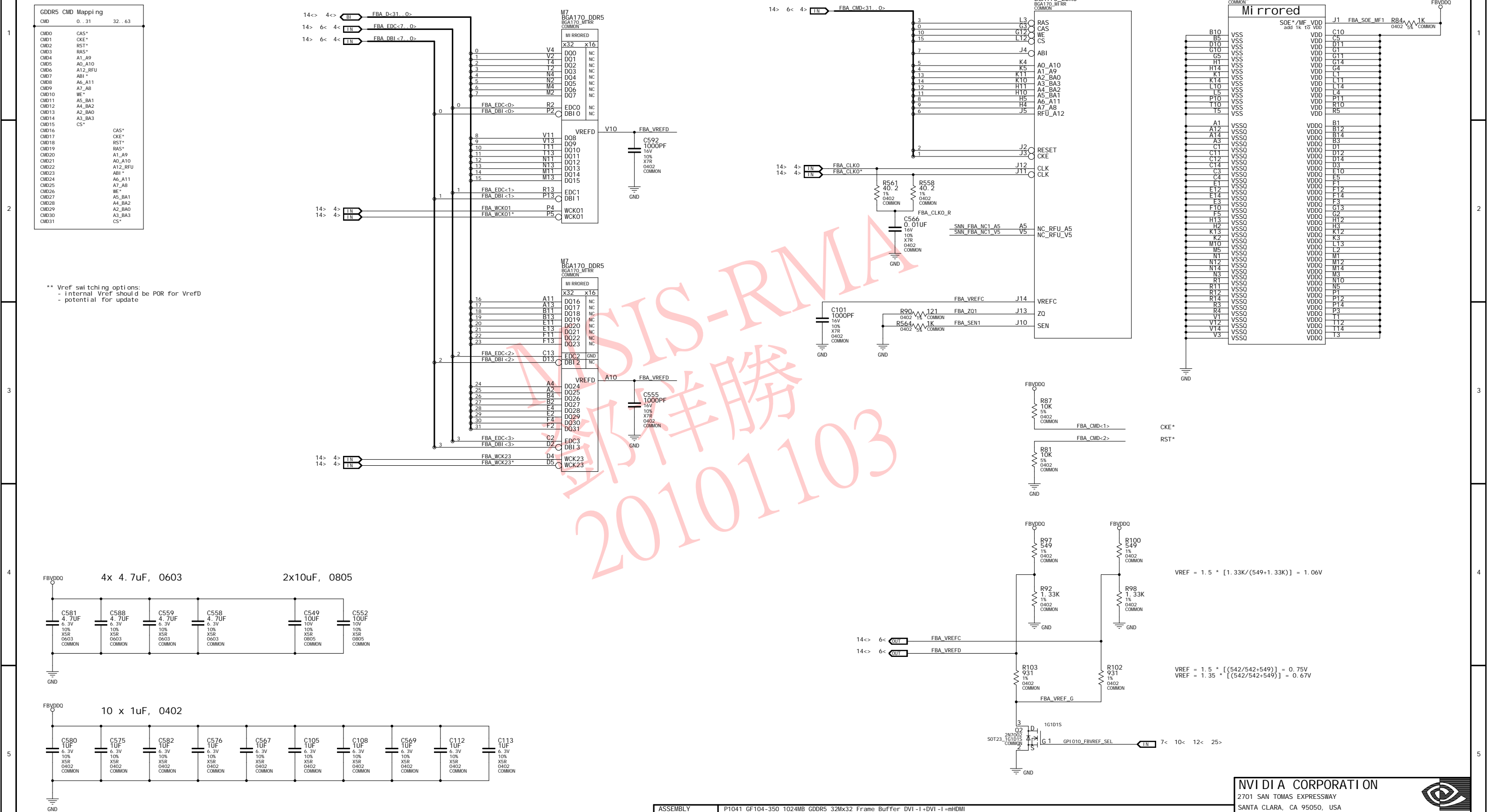
PAGE

3 OF 34

DATE

06-MAY-2010



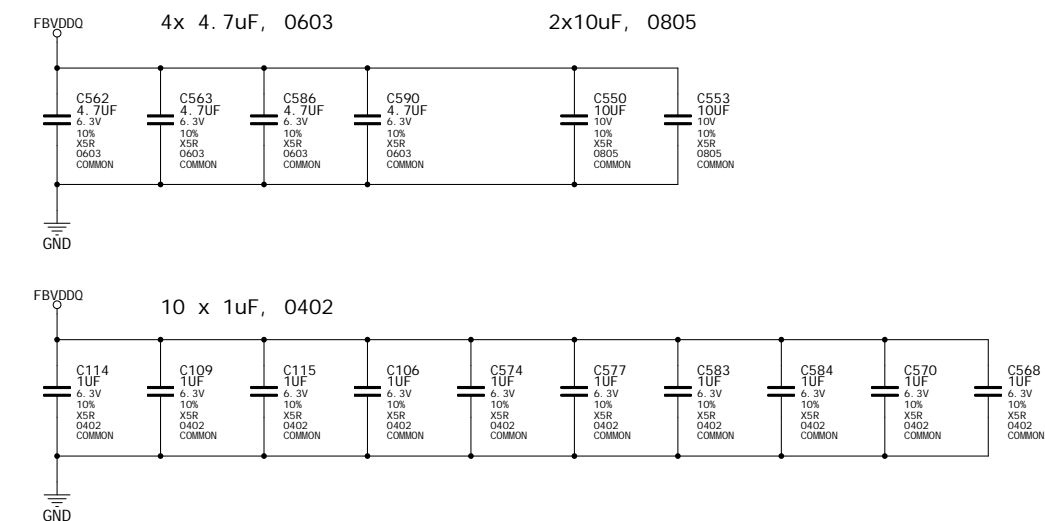
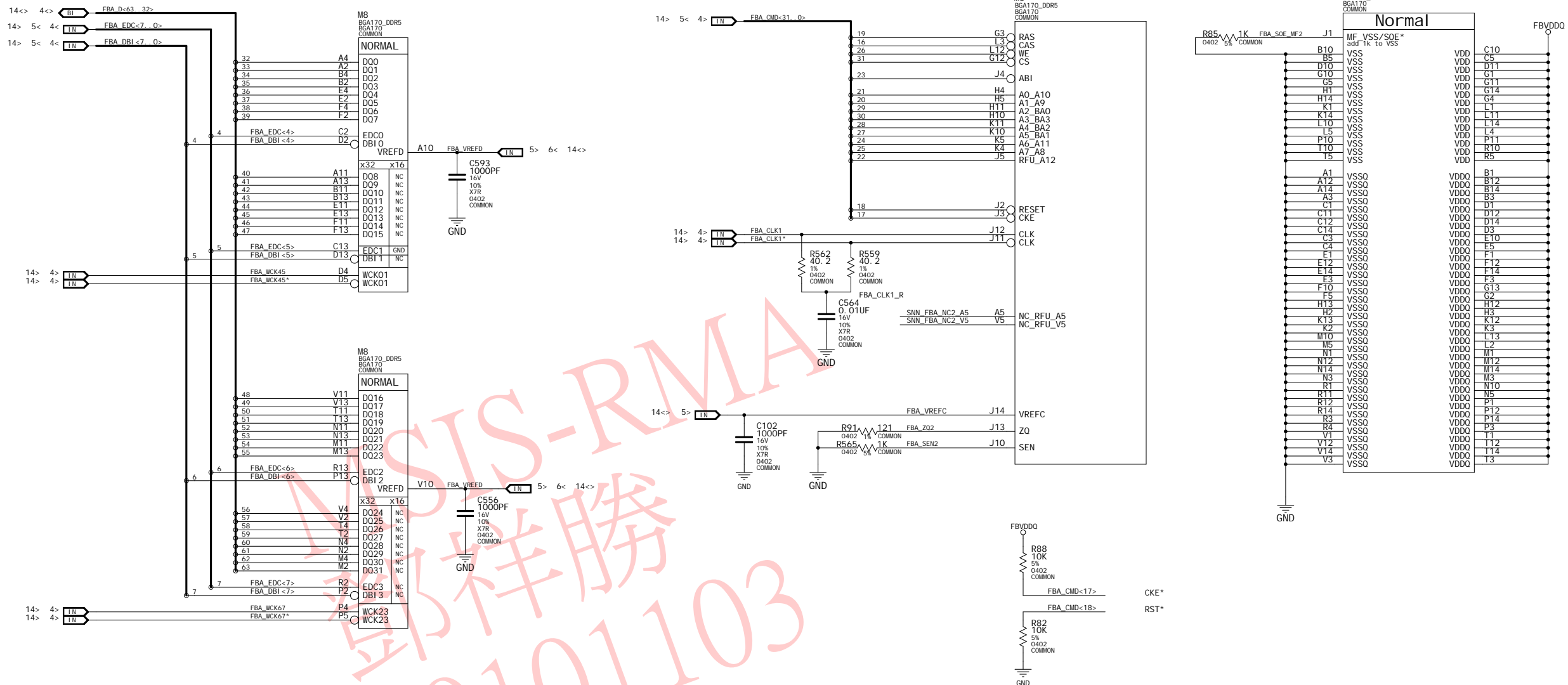


GDDR5 CMD Mapping		
CMD	0 ... 31	32 ... 63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	AB1 *	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_A6	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		AB1 *
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_A6
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

```

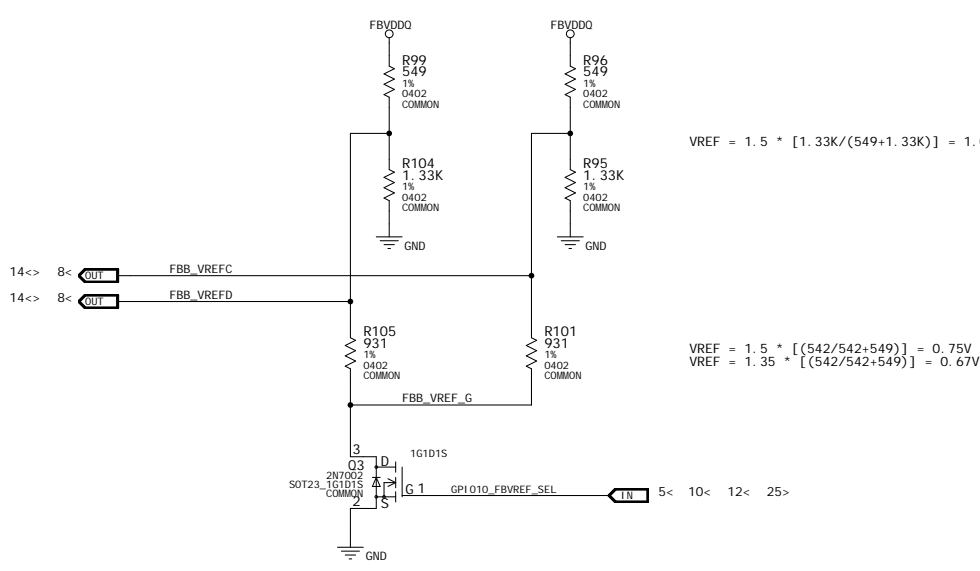
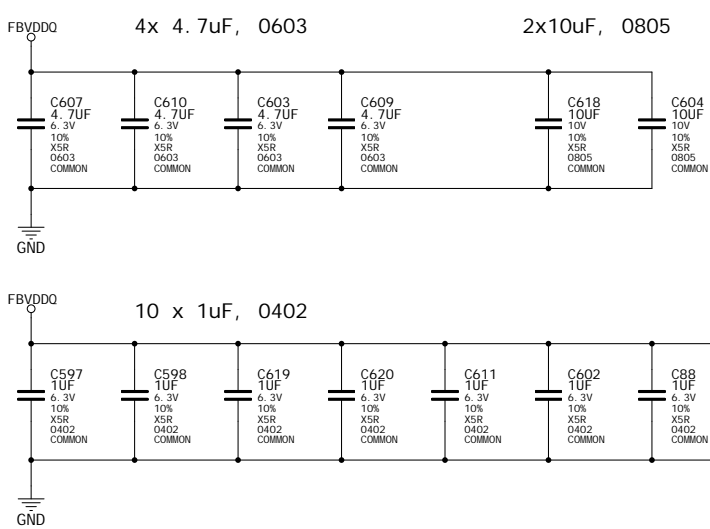
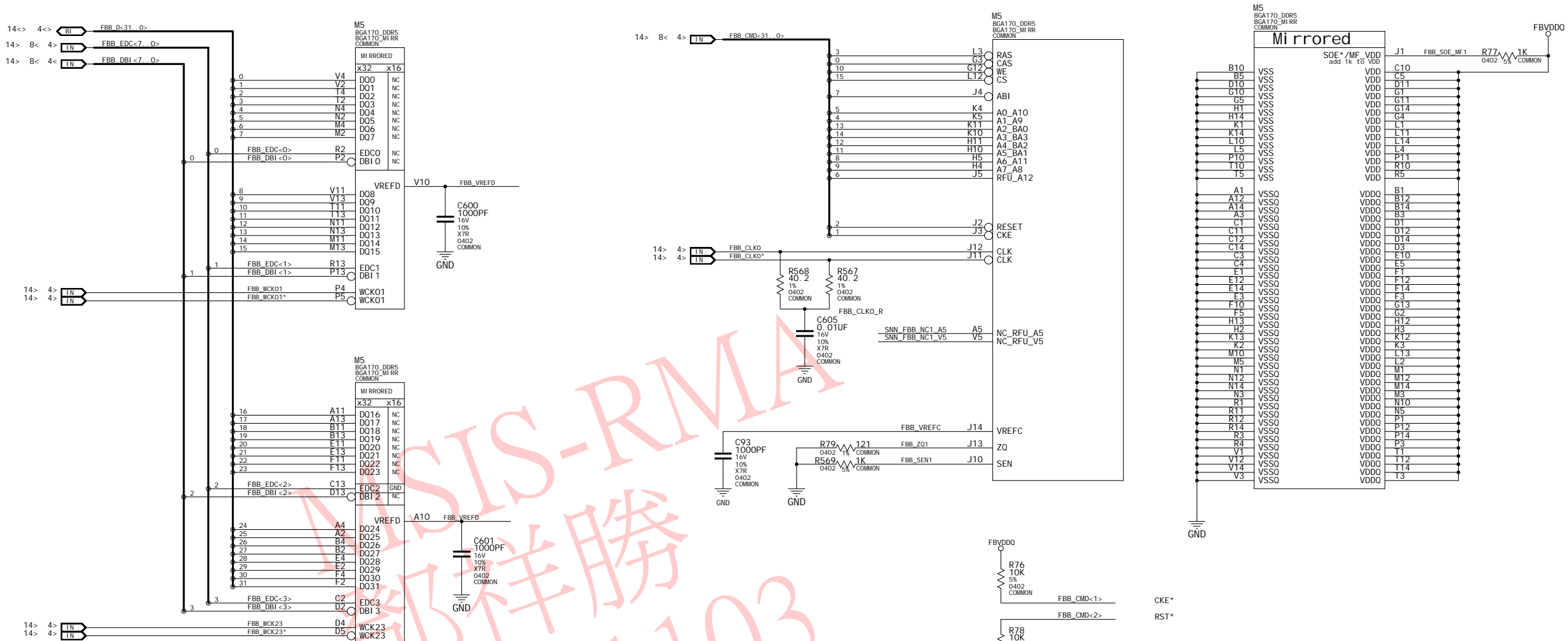
** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update

```



GDDR5 CMD Mapping			
CMD	0..31	32..63	
CMD0	CAS*		
CMD1	CKE*		
CMD2	RST*		
CMD3	RAS*		
CMD4	A1_A9		
CMD5	A0_A10		
CMD6	A12_RFU		
CMD7	AB1 *		
CMD8	A6_A11		
CMD9	A7_A8		
CMD10	WE*		
CMD11	A5_BA1		
CMD12	A4_BA2		
CMD13	A2_BA0		
CMD14	A3_BA3		
CMD15	CS*		
CMD16	CAS*		
CMD17	CKE*		
CMD18	RST*		
CMD19	RAS*		
CMD20	A1_A9		
CMD21	A0_A10		
CMD22	A12_RFU		
CMD23	AB1 *		
CMD24	A6_A11		
CMD25	A7_A8		
CMD26	WE*		
CMD27	A5_BA1		
CMD28	A4_BA2		
CMD29	A2_BA0		
CMD30	A3_BA3		
CMD31	CS*		

** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update



NV I D I A CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

ASSEMBLY

PAGE DETAIL

P1041 GF104-350 1024MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI

FBB Partition 31..0

NV_PN

PCB REV

BOM REV

600-11041-0010-QS1

P1041-B01

A

PAGE

DATE

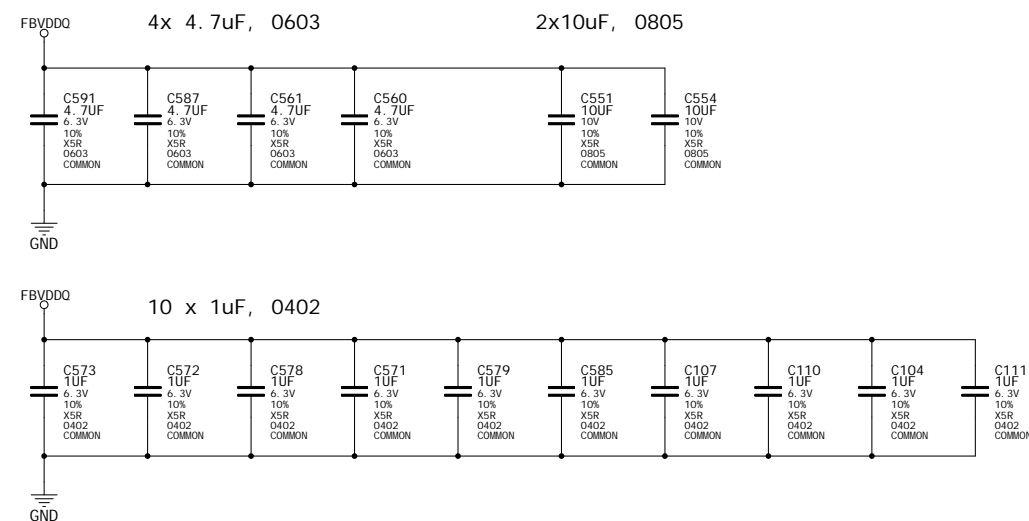
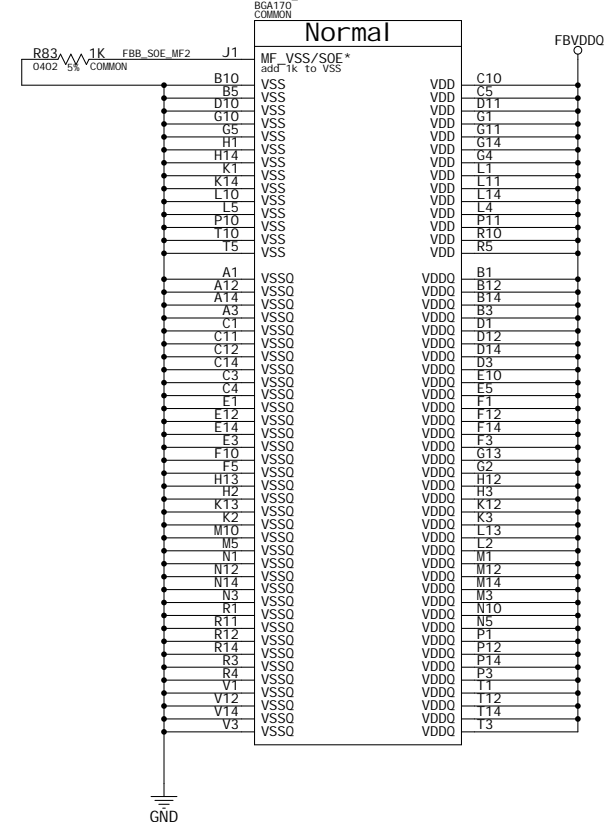
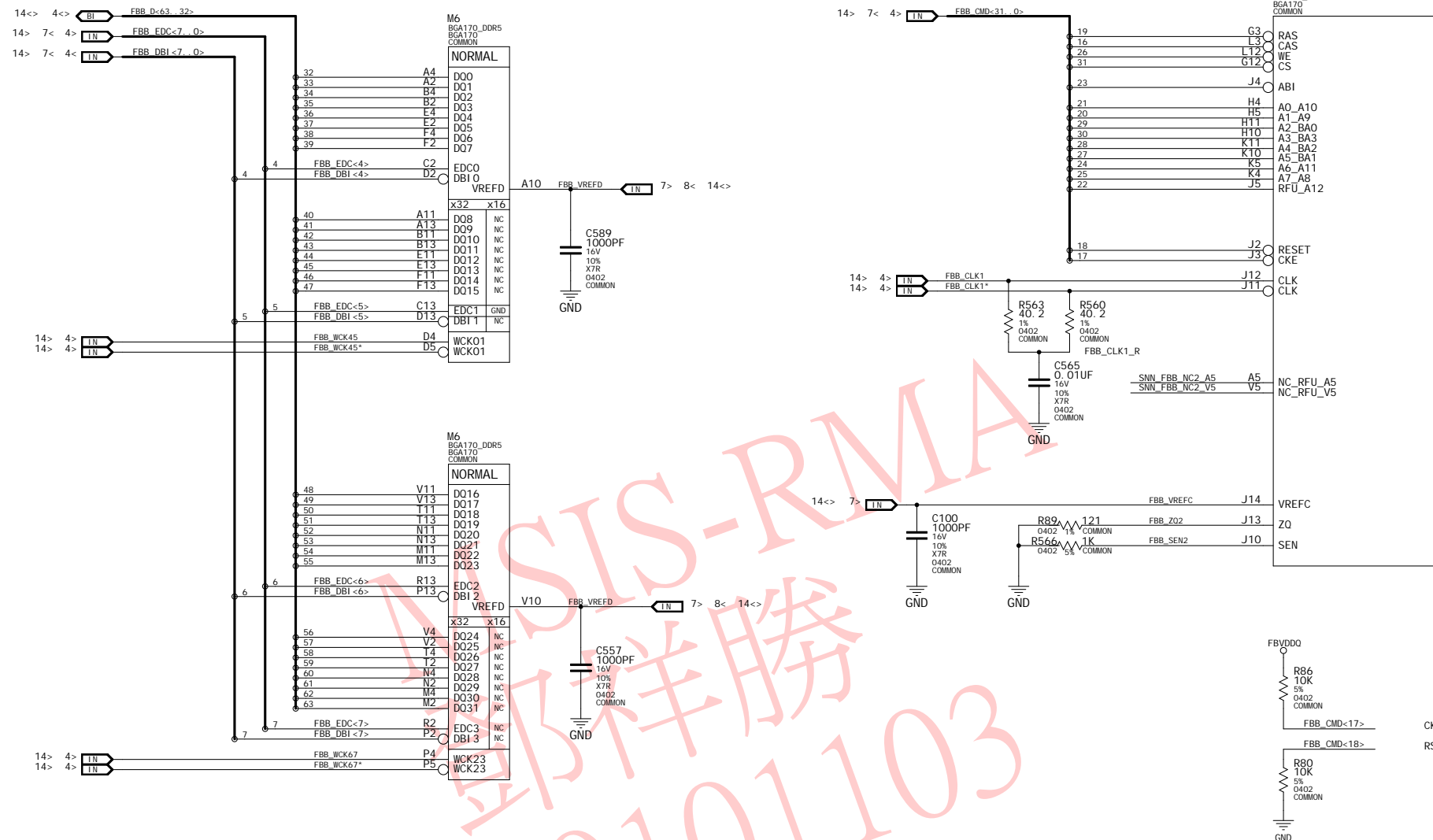
7 OF 34

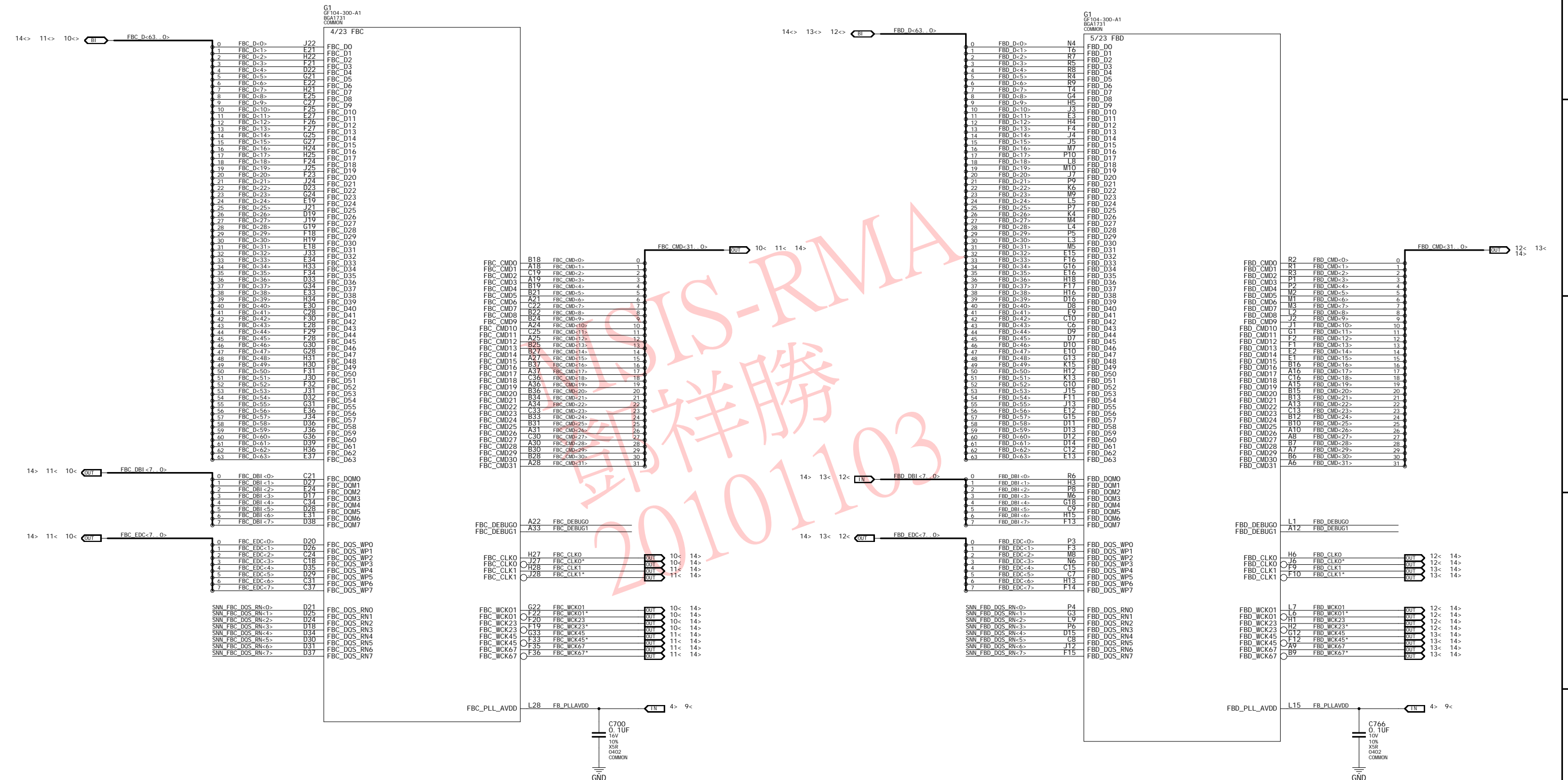
06-MAY-2010

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

GDDR5 CMD Mapping		
CMD	0...31	32...63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	AB1*	
CMD8	A5_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		AB1*
CMD24		A5_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

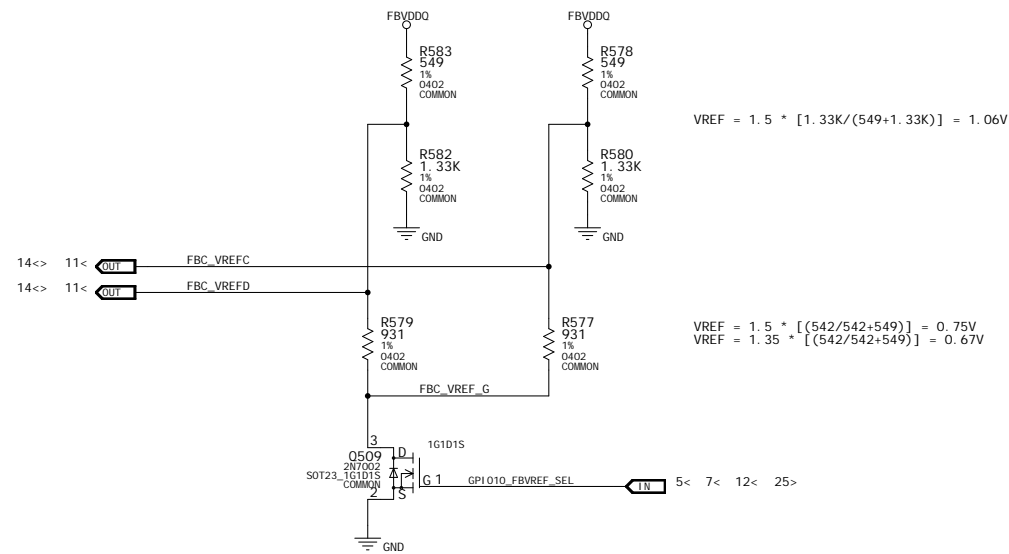
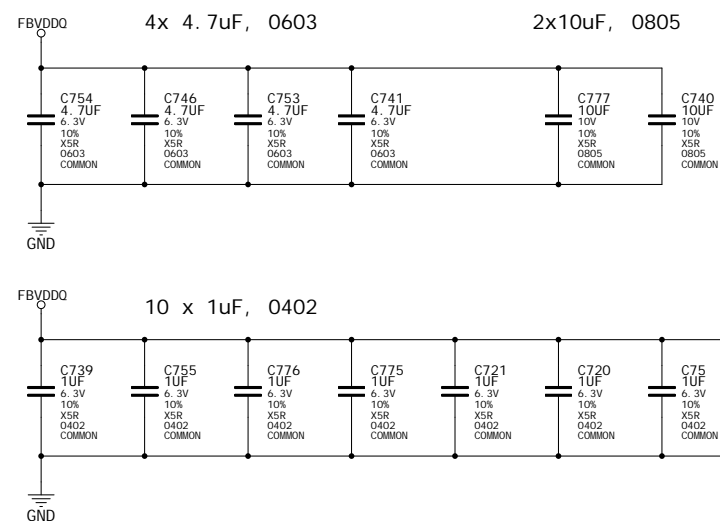
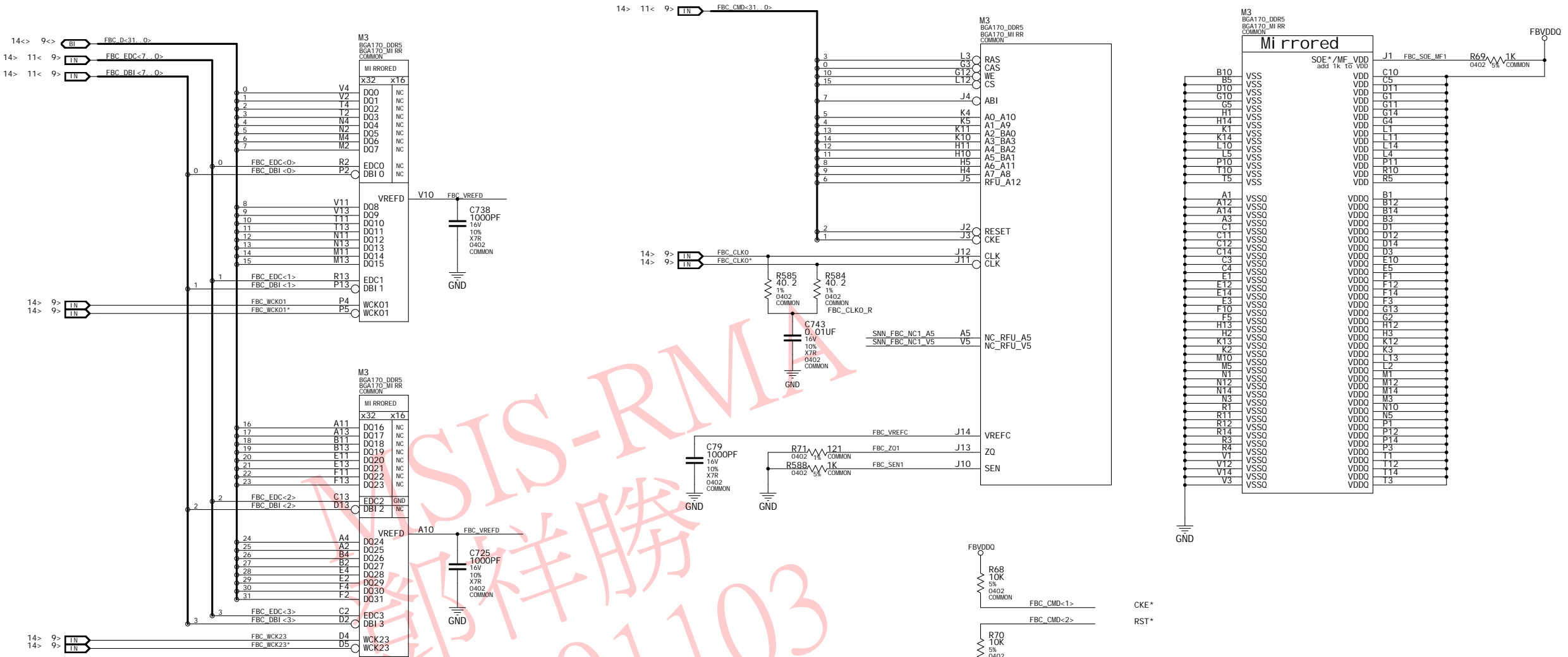
- ** Vref switching options:
 - internal Vref should be POR for VrefD
 - potential for update






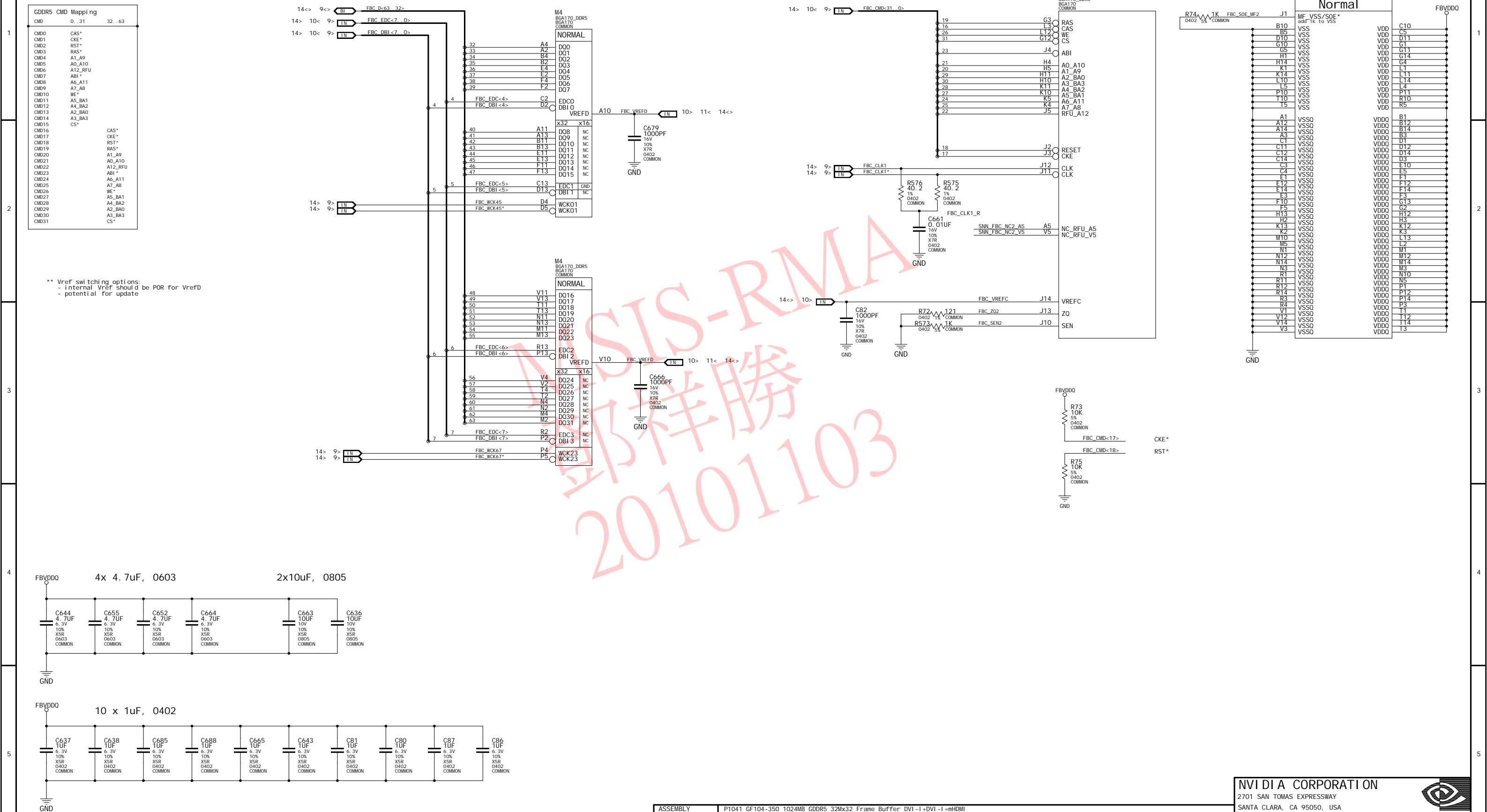
GDDR5 CMD Mapping		
CMD	0...31	32...63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_REFU	
CMD7	AB1*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_REFU
CMD23		AB1*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

```
** Vref swi tching options:
- internal Vref should be POR for VrefD
- potential for update
```



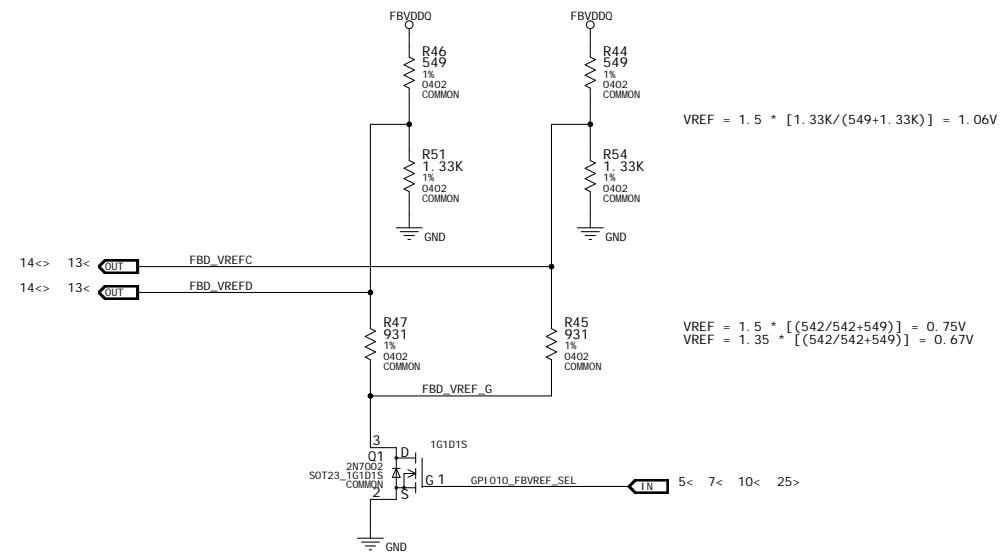
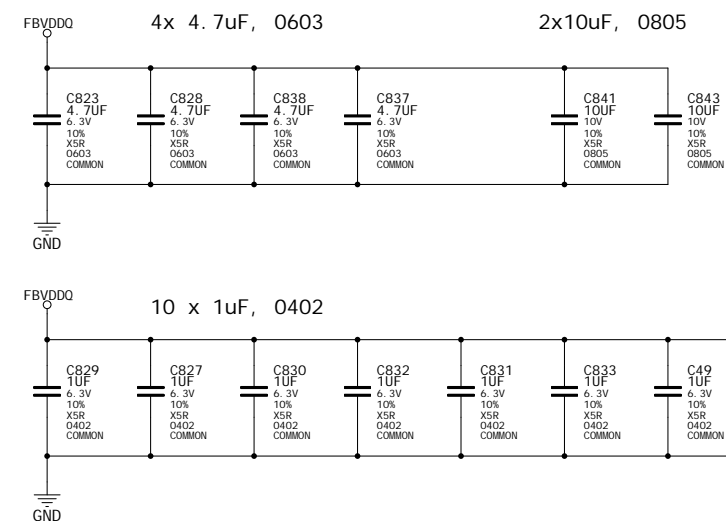
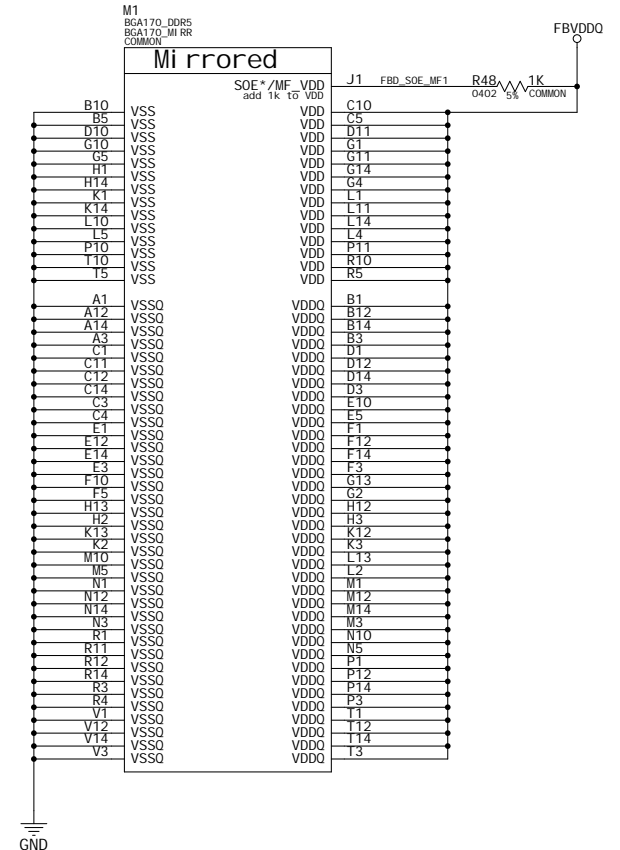
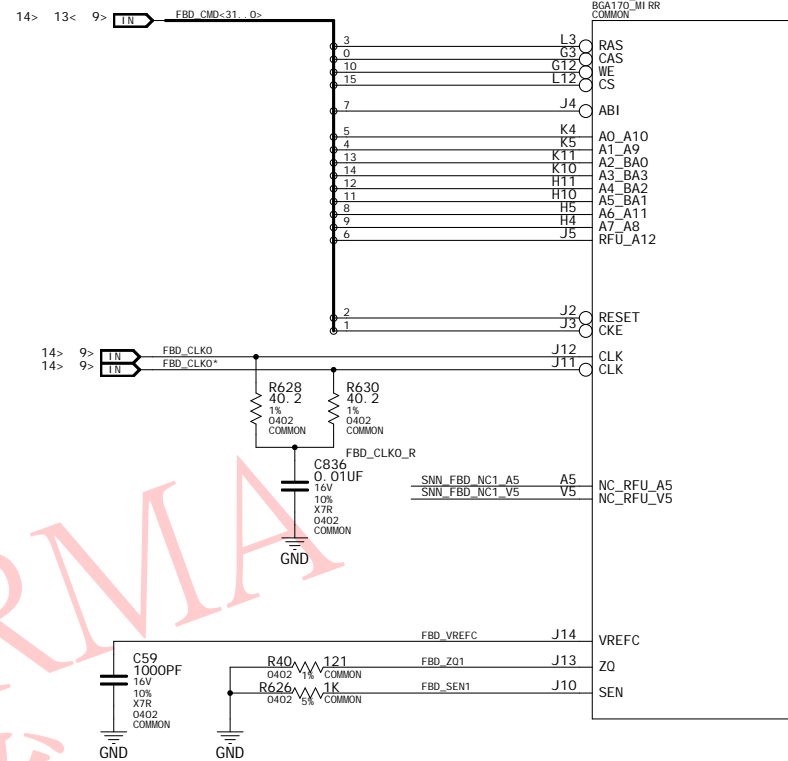
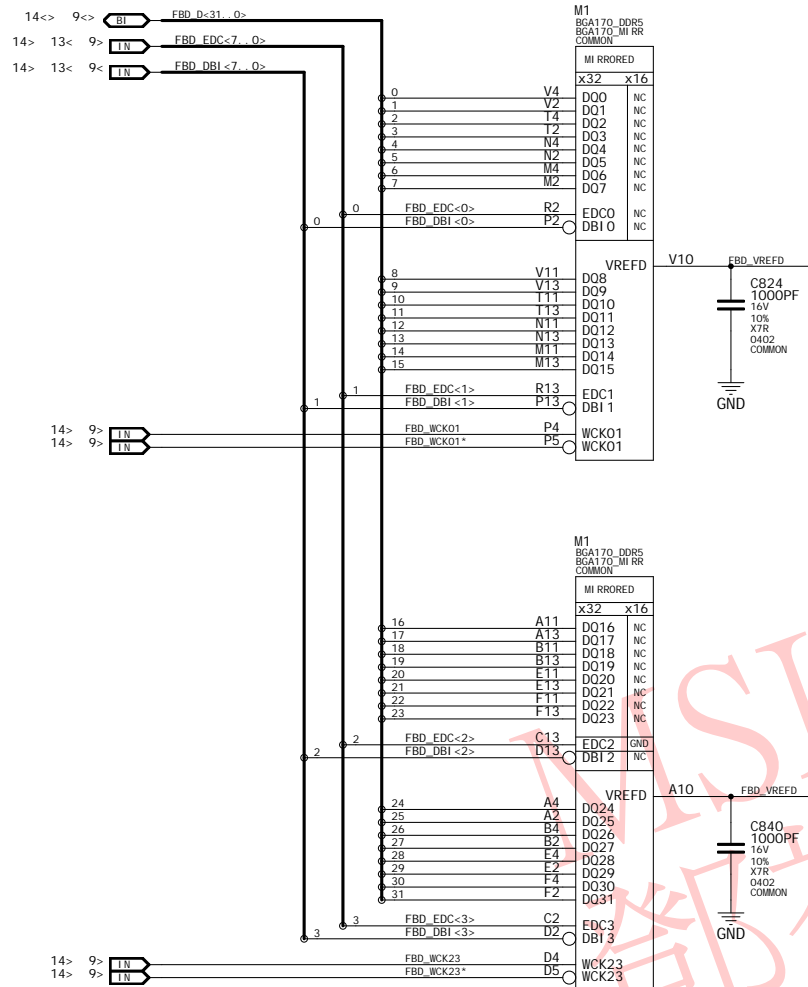
NVI DI A CORPORATI ON 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PLN		600-11041-0010-QS1		
PCB REV	P1041-B01	PAGE	10 OF 34	
BOM REV		DATE	06-MAY-2010	


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.



GDNR5	CMD	Mappi ng
CMD0	0.. 31	32.. 63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_ A9	
CMD5	A0_ A10	
CMD6	A12_ RFU	
CMD7	AB1*	
CMD8	A6_ A11	
CMD9	A7_ A8	
CMD10	WE*	
CMD11	A5_ BA1	
CMD12	A1_ BA2	
CMD13	A2_ BA0	
CMD14	A3_ BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_ A9
CMD21		A0_ A10
CMD22		A12_ RFU
CMD23		AB1*
CMD24		A6_ A11
CMD25		A7_ A8
CMD26		WE*
CMD27		A5_ BA1
CMD28		A4_ BA2
CMD29		A2_ BA0
CMD30		A3_ BA3
CMD31		CS*

```
** Vref swi tching options:
- internal Vref should be POR for VrefD
- potential for update
```

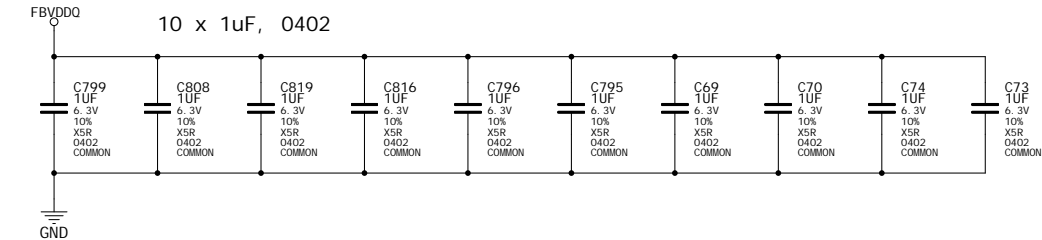
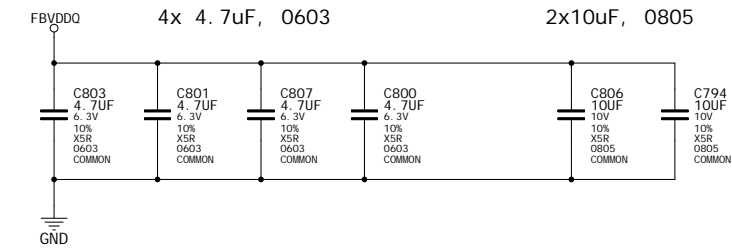
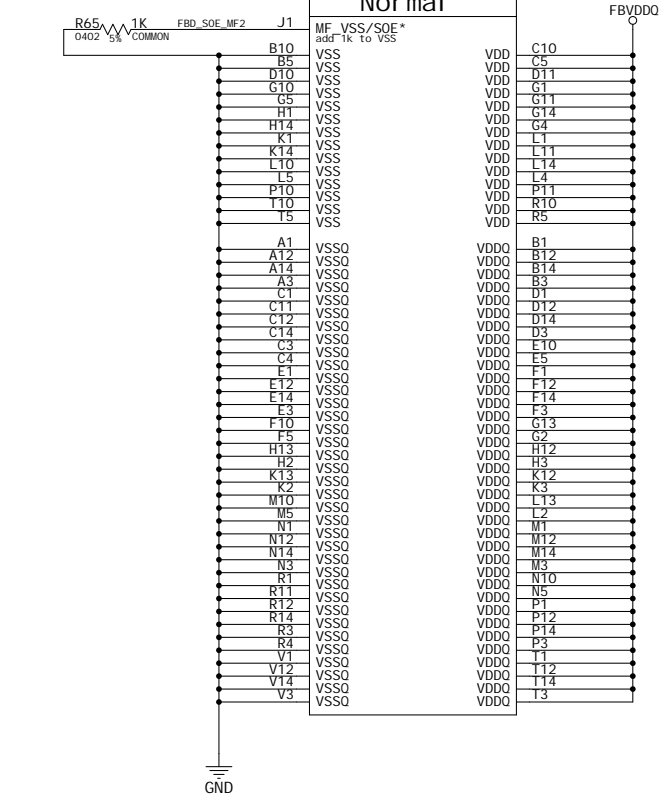
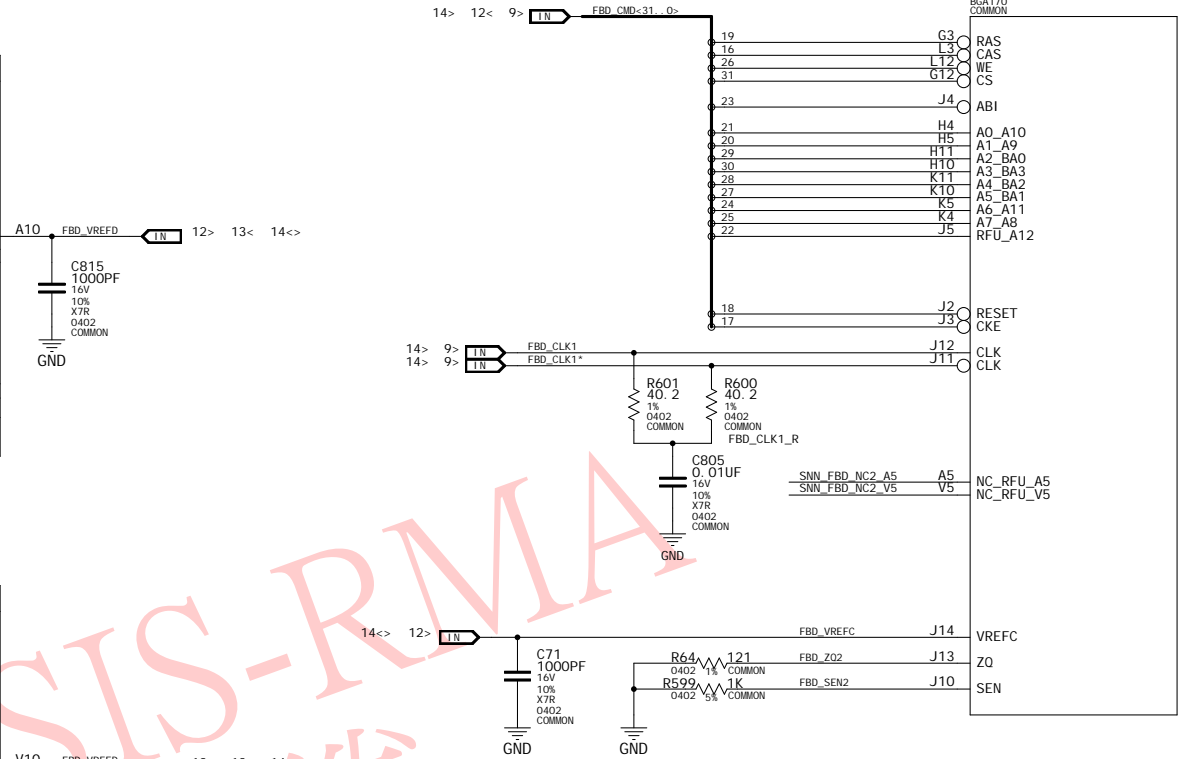
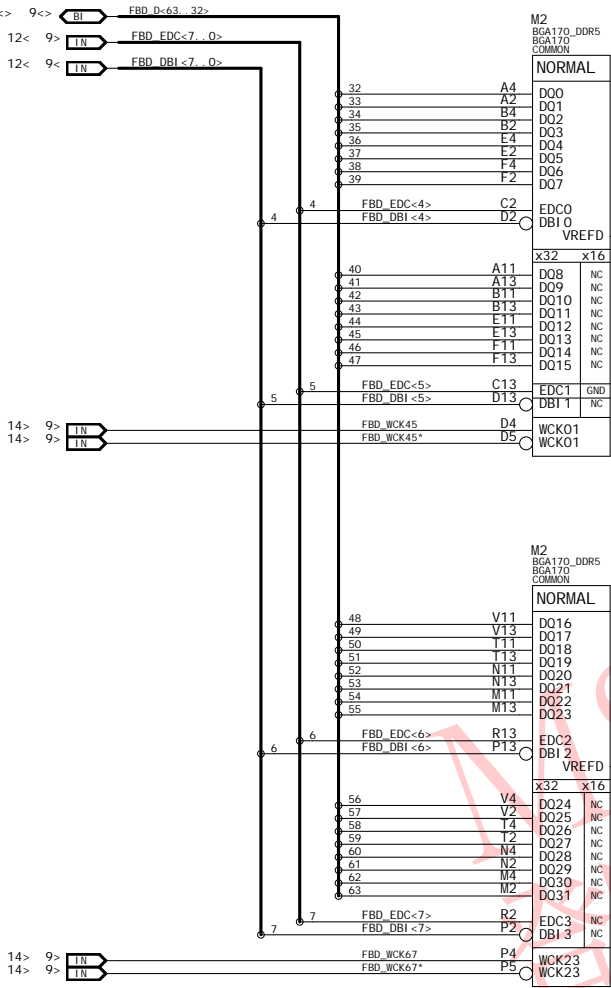


NVI DI A CORPORATI ON			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PLN	600-11041-0010-QS1		
PCB REV	P1041-B01	PAGE	12 OF 34
BOM REV		DATE	06-MAY-2010

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.





































GDDR5 CMD Mapping			
CMD	0. . 31	32. . 63	
CMD0	CAS*		
CMD1	CKE*		
CMD2	RST*		
CMD3	RAS*		
CMD4	A1_A9		
CMD5	A0_A10		
CMD6	A12_RFU		
CMD7	AB1 *		
CMD8	A6_A11		
CMD9	A7_A8		
CMD10	WE*		
CMD11	A5_BA1		
CMD12	A4_BA2		
CMD13	A2_BA0		
CMD14	A3_BA3		
CMD15	CS*		
CMD16	CAS*		
CMD17	CKE*		
CMD18	RST*		
CMD19	RAS*		
CMD20	A1_A9		
CMD21	A0_A10		
CMD22	A12_RFU		
CMD23	AB1 *		
CMD24	A6_A11		
CMD25	A7_A8		
CMD26	WE*		
CMD27	A5_BA1		
CMD28	A4_BA2		
CMD29	A2_BA0		
CMD30	A3_BA3		
CMD31	CS*		





































** Vref switching options:
- Internal Vref should be POR for VrefD
- potential for update



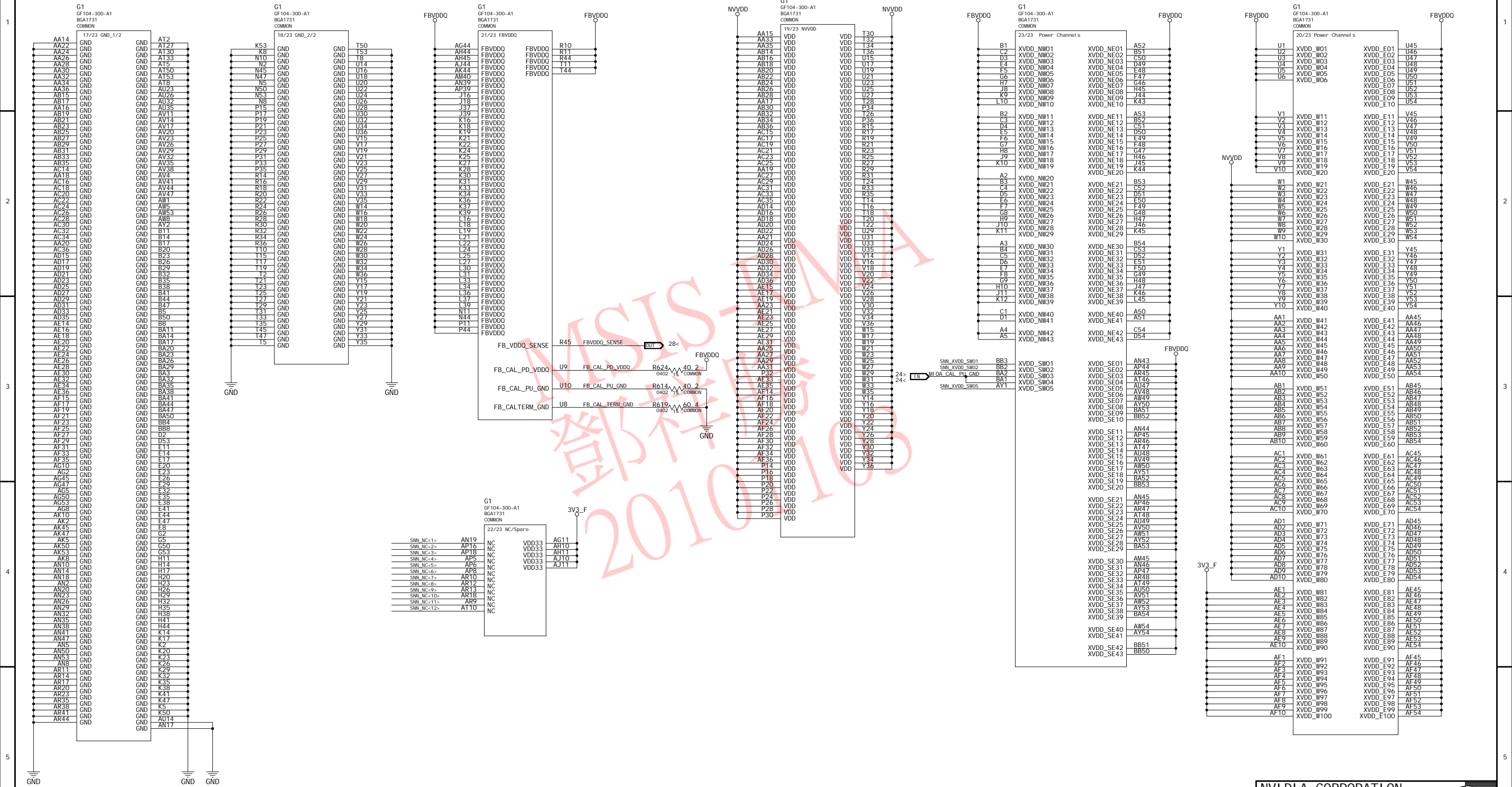
NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-11041-0010-QS1		
PCB REV	P1041-B01	PAGE	13 OF 34
BOM REV	A	DATE	06-MAY-2010

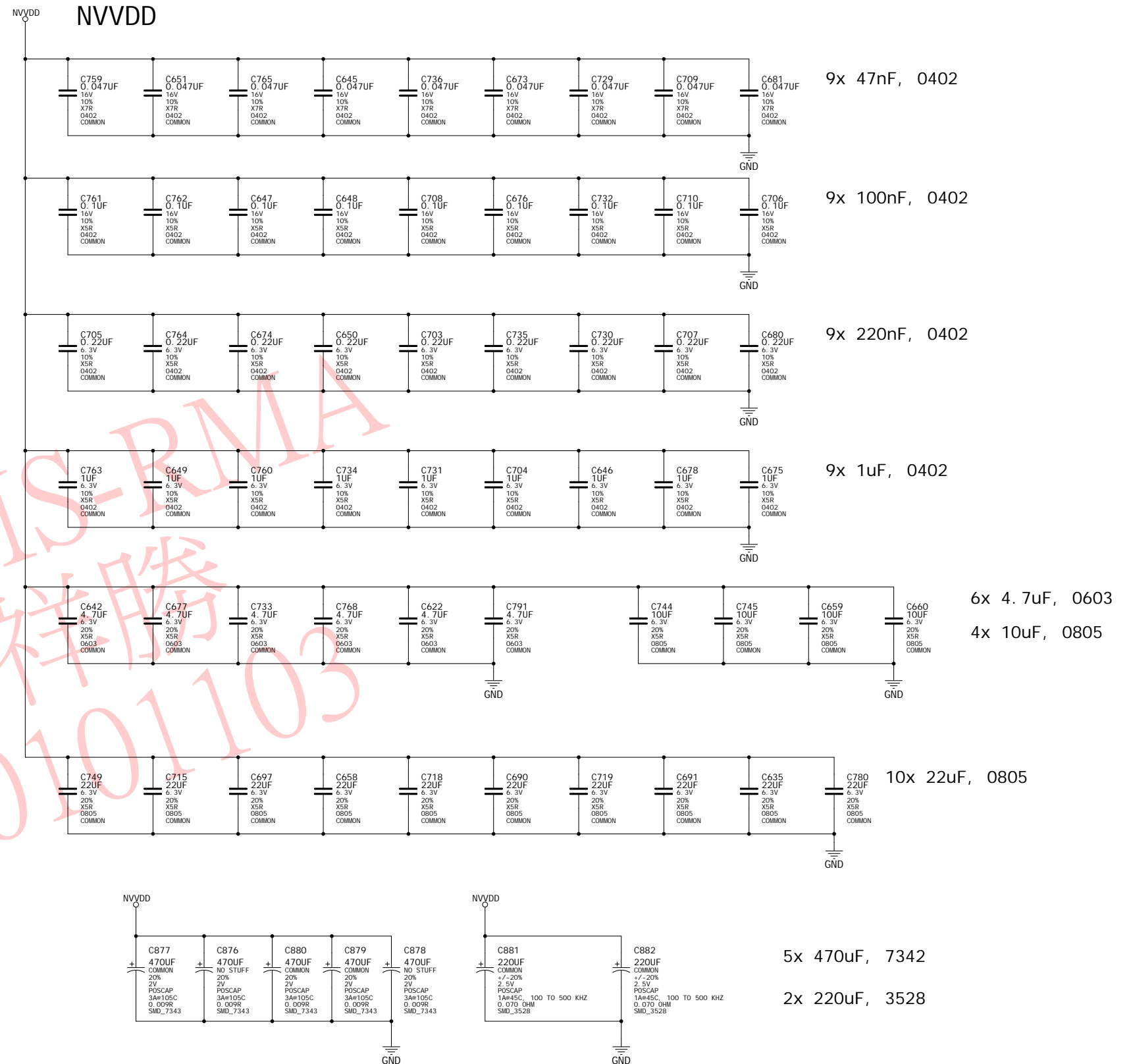
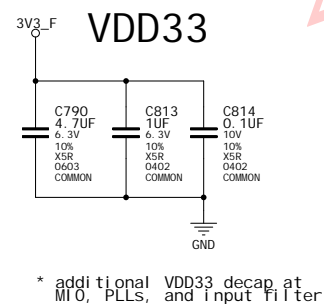
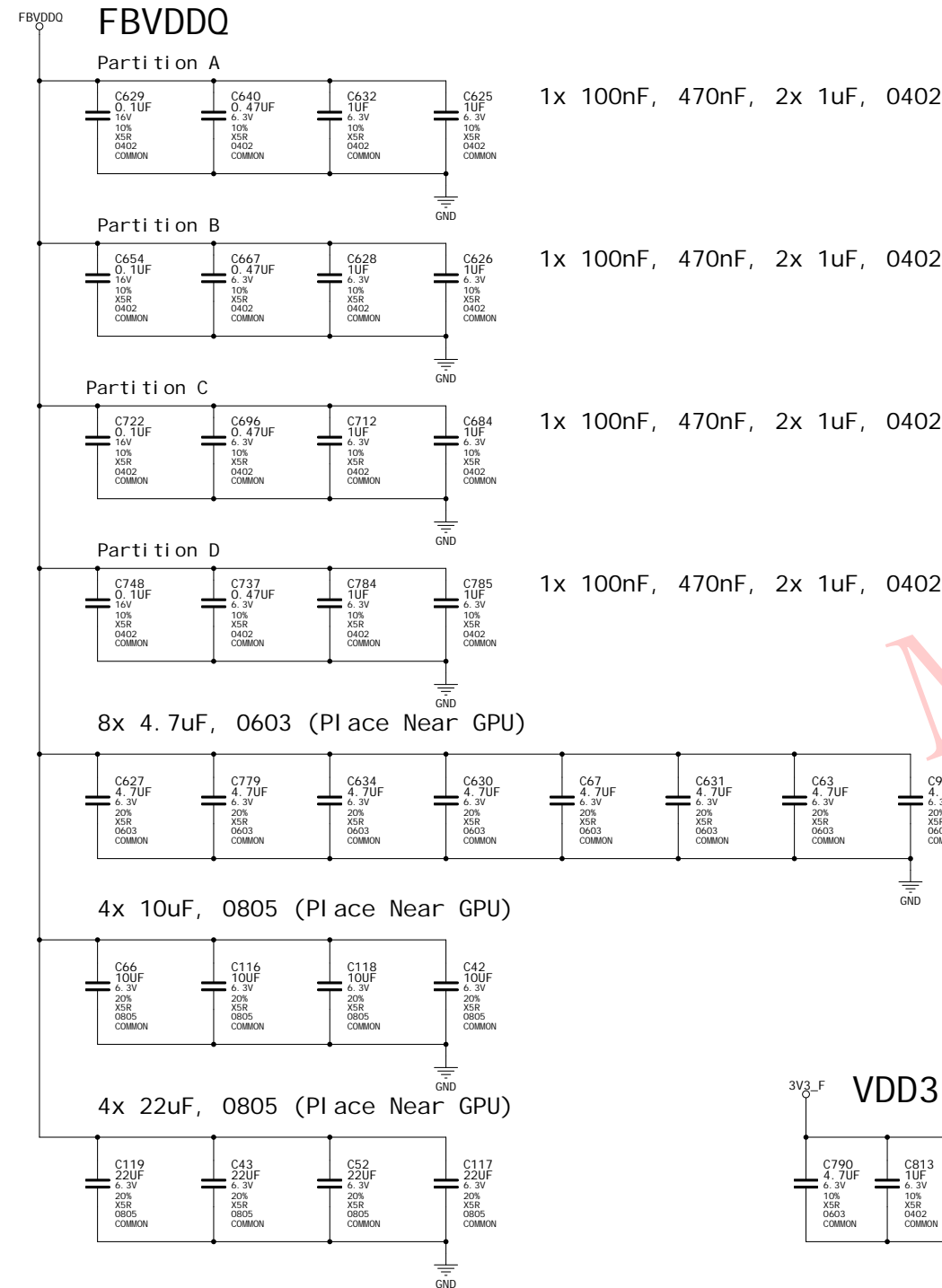
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NET RULES for FrameBuffer A/B				
NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
5< 4>		FBA_CLK0	1	FBA_CLK0
		FBA_CLK0*	80DI FF	FBA_CLK0
6< 4>		FBA_CLK1	1	FBA_CLK1
		FBA_CLK1*	80DI FF	FBA_CLK1
7< 4>		FBB_WCK01	1	FBB_WCK01
		FBB_WCK01*	80DI FF	FBB_WCK01
7< 4>		FBB_WCK23	1	FBB_WCK23
		FBB_WCK23*	80DI FF	FBB_WCK23
8< 4>		FBB_WCK45	1	FBB_WCK45
		FBB_WCK45*	80DI FF	FBB_WCK45
8< 4>		FBB_WCK67	1	FBB_WCK67
		FBB_WCK67*	80DI FF	FBB_WCK67
6< 5< 4>		FBA_CMD<31..0>	1	45OHM
		FBA_EDC<7..0>	1	45OHM
6< 5< 4<>		FBA_DBI<7..0>	1	45OHM
		FBA_D<63..0>	1	45OHM
NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
7< 4>		FBB_CLK0	1	FBB_CLK0
		FBB_CLK0*	80DI FF	FBB_CLK0
8< 4>		FBB_CLK1	1	FBB_CLK1
		FBB_CLK1*	80DI FF	FBB_CLK1
5< 4>		FBA_WCK01	1	FBA_WCK01
		FBA_WCK01*	80DI FF	FBA_WCK01
5< 4>		FBA_WCK23	1	FBA_WCK23
		FBA_WCK23*	80DI FF	FBA_WCK23
6< 4>		FBA_WCK45	1	FBA_WCK45
		FBA_WCK45*	80DI FF	FBA_WCK45
6< 4>		FBA_WCK67	1	FBA_WCK67
		FBA_WCK67*	80DI FF	FBA_WCK67
8< 7< 4>		FBB_CMD<31..0>	1	45OHM
		FBB_EDC<7..0>	1	45OHM
8< 7< 4<>		FBB_DBI<7..0>	1	45OHM
		FBB_D<63..0>	1	45OHM
NET		VOLTAGE	MAX_CURRENT	MI N_WI DTH
6< 5>		FBA_VREFD	1.00V	0.02A
6< 5>		FBA_VREFC	1.00V	0.02A
8< 7>		FBB_VREFD	1.00V	0.02A
8< 7>		FBB_VREFC	1.00V	0.02A

NET RULES for FrameBuffer C/D				
NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
10< 9>		FBC_CLK0	1	FBC_CLK0
		FBC_CLK0*	80DI FF	FBC_CLK0
11< 9>		FBC_CLK1	1	FBC_CLK1
		FBC_CLK1*	80DI FF	FBC_CLK1
10< 9>		FBC_WCK01	1	FBC_WCK01
		FBC_WCK01*	80DI FF	FBC_WCK01
10< 9>		FBC_WCK23	1	FBC_WCK23
		FBC_WCK23*	80DI FF	FBC_WCK23
11< 9>		FBC_WCK45	1	FBC_WCK45
		FBC_WCK45*	80DI FF	FBC_WCK45
11< 9>		FBC_WCK67	1	FBC_WCK67
		FBC_WCK67*	80DI FF	FBC_WCK67
11< 10< 9>		FBC_CMD<31..0>	1	45OHM
		FBC_EDC<7..0>	1	45OHM
11< 10< 9>		FBC_DBI<7..0>	1	45OHM
		FBC_D<63..0>	1	45OHM
NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
12< 9>		FBD_CLK0	1	FBD_CLK0
		FBD_CLK0*	80DI FF	FBD_CLK0
13< 9>		FBD_CLK1	1	FBD_CLK1
		FBD_CLK1*	80DI FF	FBD_CLK1
12< 9>		FBD_WCK01	1	FBD_WCK01
		FBD_WCK01*	80DI FF	FBD_WCK01
12< 9>		FBD_WCK23	1	FBD_WCK23
		FBD_WCK23*	80DI FF	FBD_WCK23
13< 9>		FBD_WCK45	1	FBD_WCK45
		FBD_WCK45*	80DI FF	FBD_WCK45
13< 9>		FBD_WCK67	1	FBD_WCK67
		FBD_WCK67*	80DI FF	FBD_WCK67
13< 12< 9>		FBD_CMD<31..0>	1	45OHM
		FBD_EDC<7..0>	1	45OHM
13< 12< 9>		FBD_DBI<7..0>	1	45OHM
		FBD_D<63..0>	1	45OHM
NET		VOLTAGE	MAX_CURRENT	MI N_WI DTH
11< 10>		FBC_VREFD	1.00V	0.02A
11< 10>		FBC_VREFC	1.00V	0.02A
13< 12>		FBD_VREFD	1.00V	0.02A
13< 12>		FBD_VREFC	1.00V	0.02A

** Power channels are configurable.
XVDD_* pins are not connected on the substrate.
Therefore, XVDD_* pins can be assigned as needed.





ASSEMBLY	P1041 GF104-350 1024MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDM
PAGE DETAIL	GPU Decoupling

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN 600-11041-0010-QS1			
PCB REV	PT041-B01	PAGE	16 OF 34
BOM REV		DATE	06-MAY-2010

MSIS-RMA
鄧祥勝
20101103

NV I D I A C O R P O R A T I O N

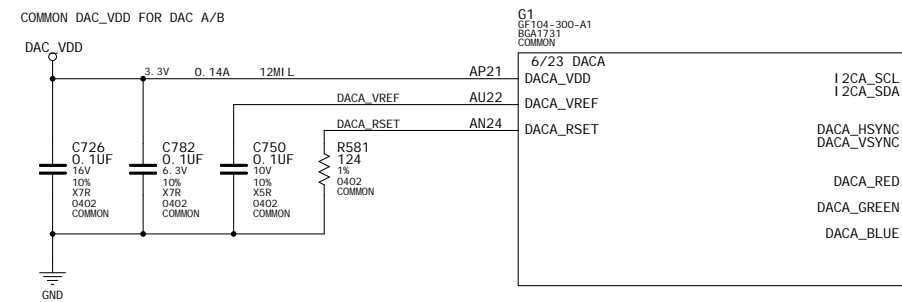
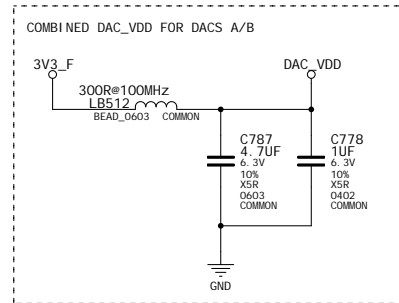
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



NV_PN 600-11041-0010-QS1

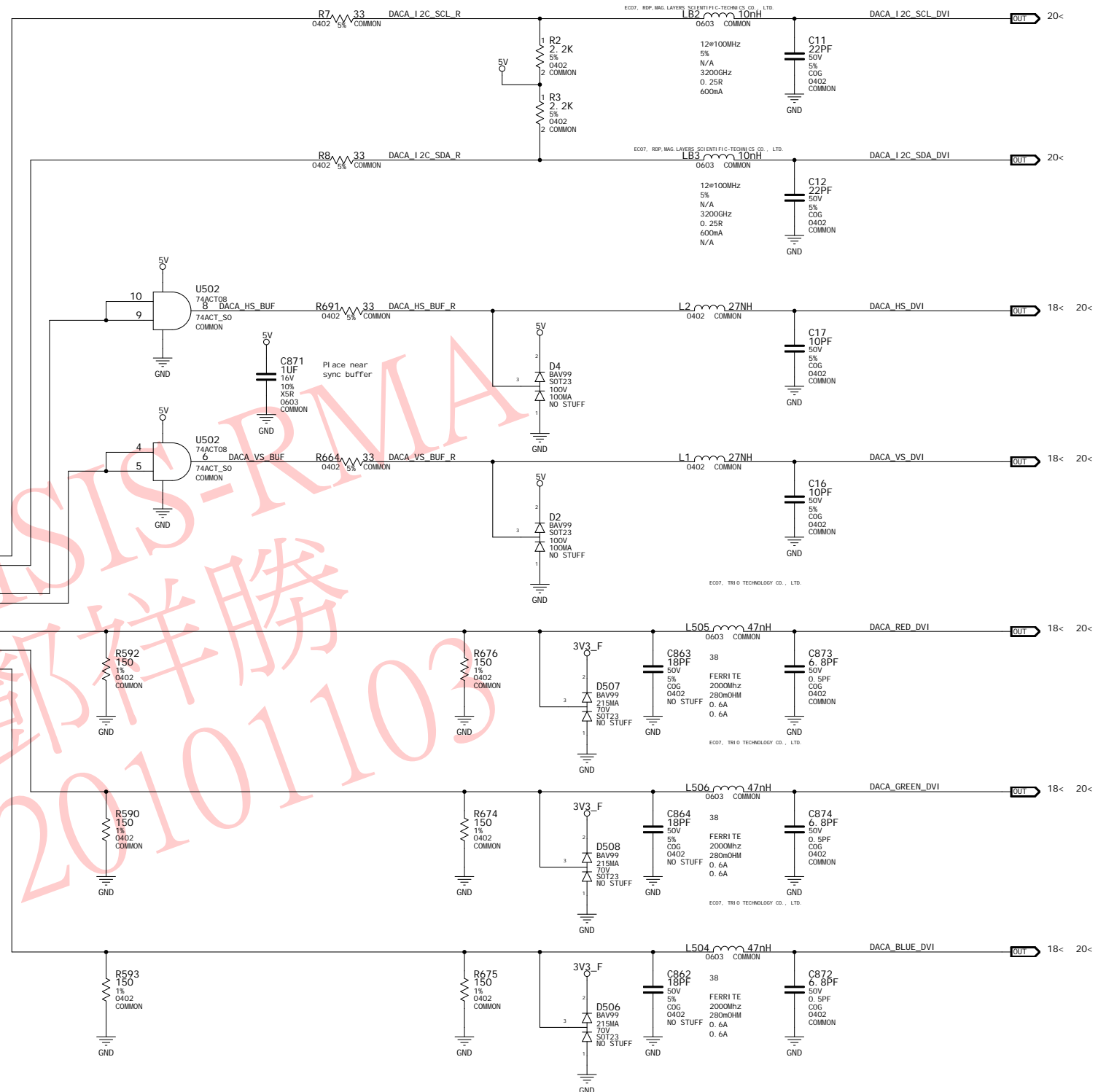
PCB REV	P1041-B01	PAGE	17 OF 34
BOM REV	A	DATE	06-MAY-2010

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.




DACA NET RULES

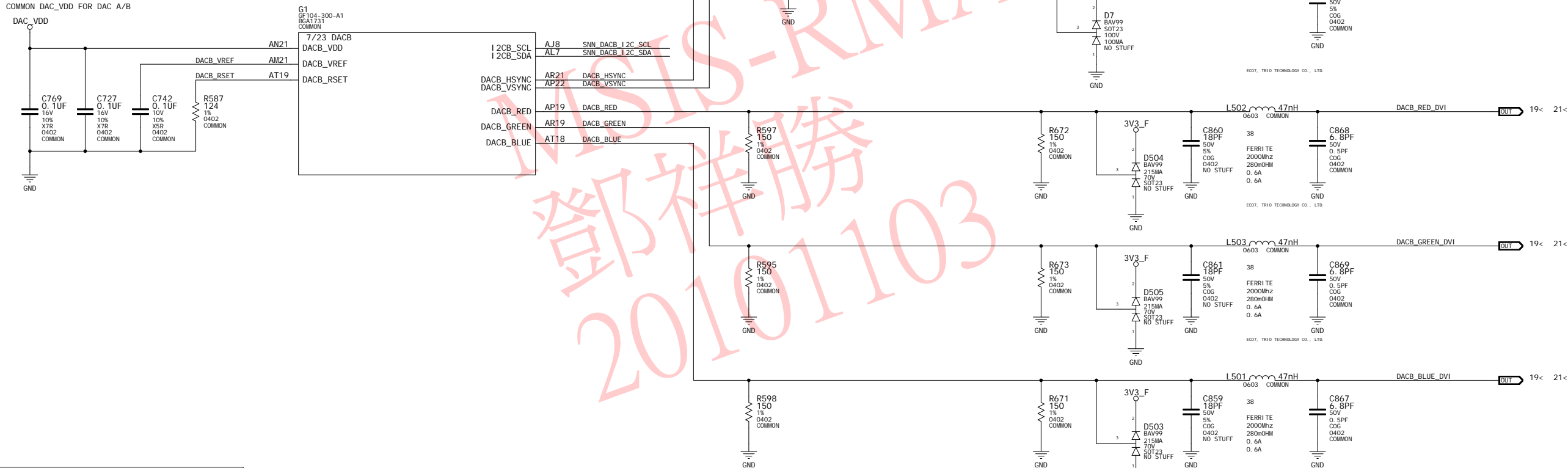
	NET	NV_CRI T1 CAL	NV_I IMPEDANCE
IN	DACA_RED	1	750HM
IN	DACA_GREEN	1	750HM
IN	DACA_BLUE	1	750HM
IN	DACA_RED_DVI	1	750HM
IN	DACA_GREEN_DVI	1	750HM
IN	DACA_BLUE_DVI	1	750HM
IN	DACA_HSYNC	2	500HM
IN	DACA_VSYNC	2	500HM
IN	DACA_HS_BUF	2	500HM
IN	DACA_VS_BUF	2	500HM
IN	DACA_HS_BUF_R	2	500HM
IN	DACA_VS_BUF_R	2	500HM
IN	DACA_HS_DVI	2	500HM
IN	DACA_VS_DVI	2	500HM
















ASSEMBLY	P1041 GF104-350 1024MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	DACA (South)

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVI DI A CORPORATI ON			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-11041-0010-QS1		
PCB REV	P1041-B01	PAGE	18 OF 34
BOM REV	A	DATE	06-MAY-2010



DACB NET RULES

		NET	NV_CRI T I C A L	NV_I M P E D A N C E
		 DACB_RED	1	750HM
		 DACB_GREEN	1	750HM
		 DACB_BLUE	1	750HM
21<	19>	 DACB_RED_DVI	1	750HM
21<	19>	 DACB_GREEN_DVI	1	750HM
21<	19>	 DACB_BLUE_DVI	1	750HM
		 DACB_HSYNC	2	500HM
		 DACB_VSYNC	2	500HM
		 DACB_HS_BUF	2	500HM
		 DACB_VS_BUF	2	500HM
		 DACB_HS_BUF_R	2	500HM
		 DACB_VS_BUF_R	2	500HM
21<	19>	 DACB_HS_DVI	2	500HM
21<	19>	DACB_VS_DVI	2	500HM

ASSEMBLY	P1041 GF104-350 1024MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	DACB (Mi d)

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVI DI A CORPORATI ON

2701 SAN TOMAS EXPRESSWAY

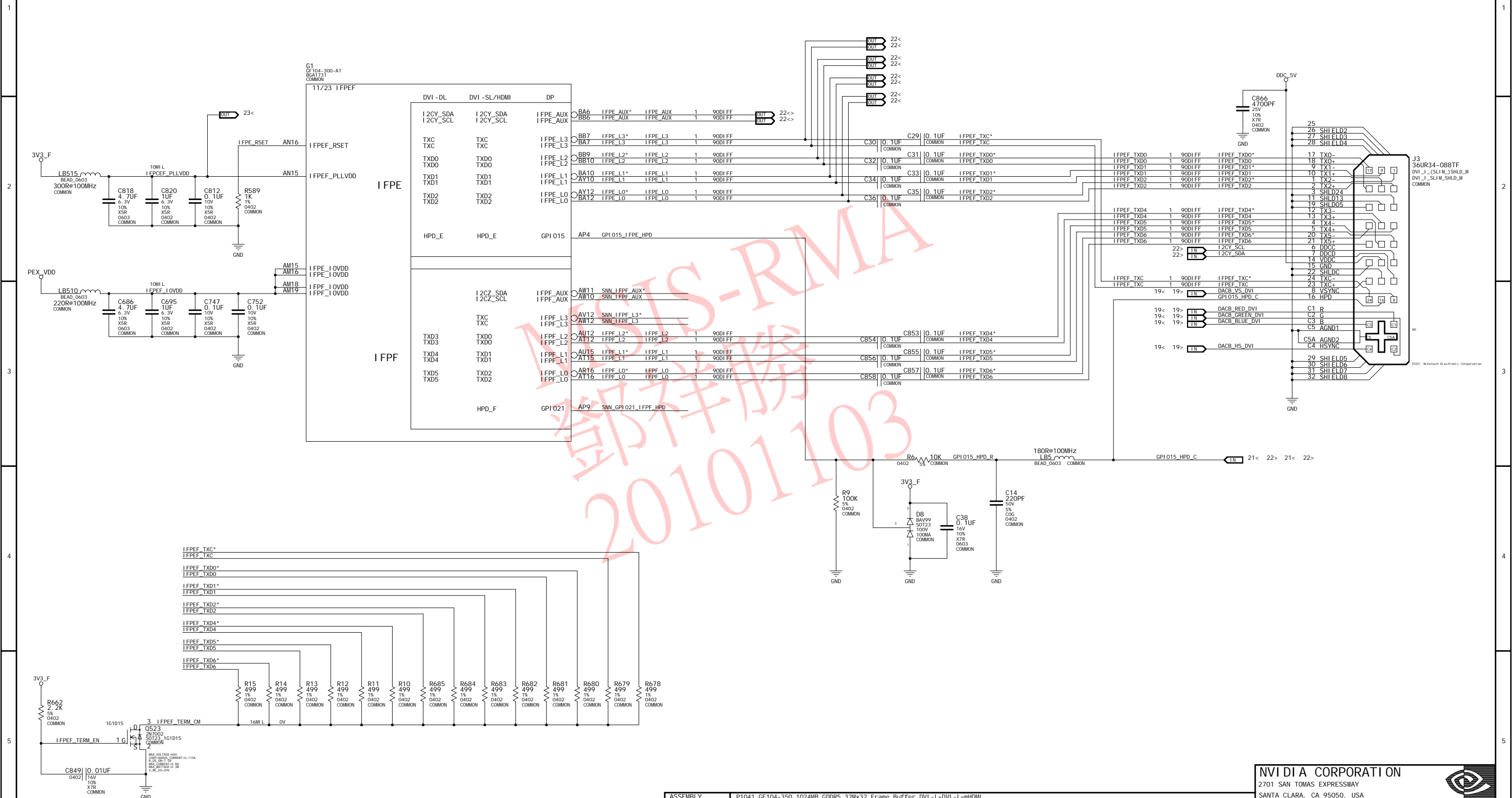
SANTA CLARA, CA 95050, US

NV_PN	600-11041-0010-QS1
-------	--------------------

PCB REV	P1041-B01	PAGE	19 OF 34
BOM REV	A	DATE	06-MAY-2010




ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.



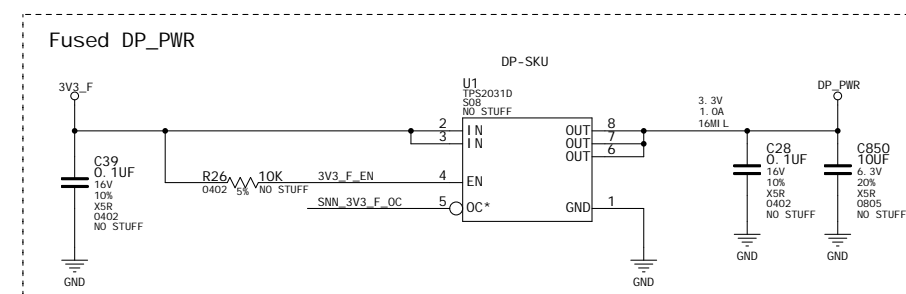
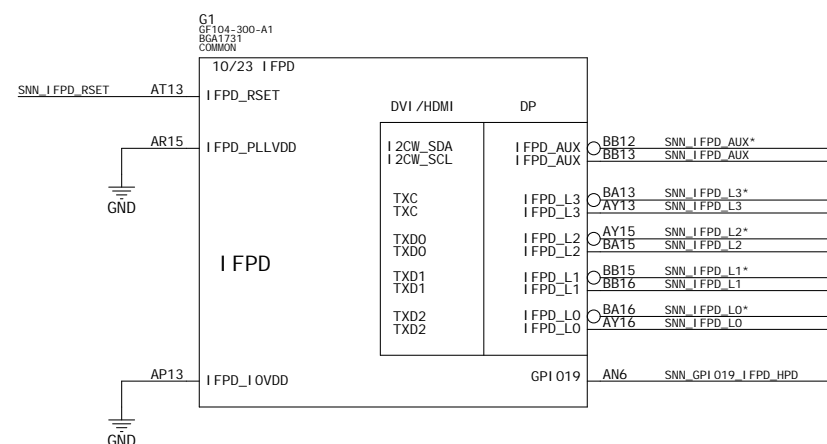
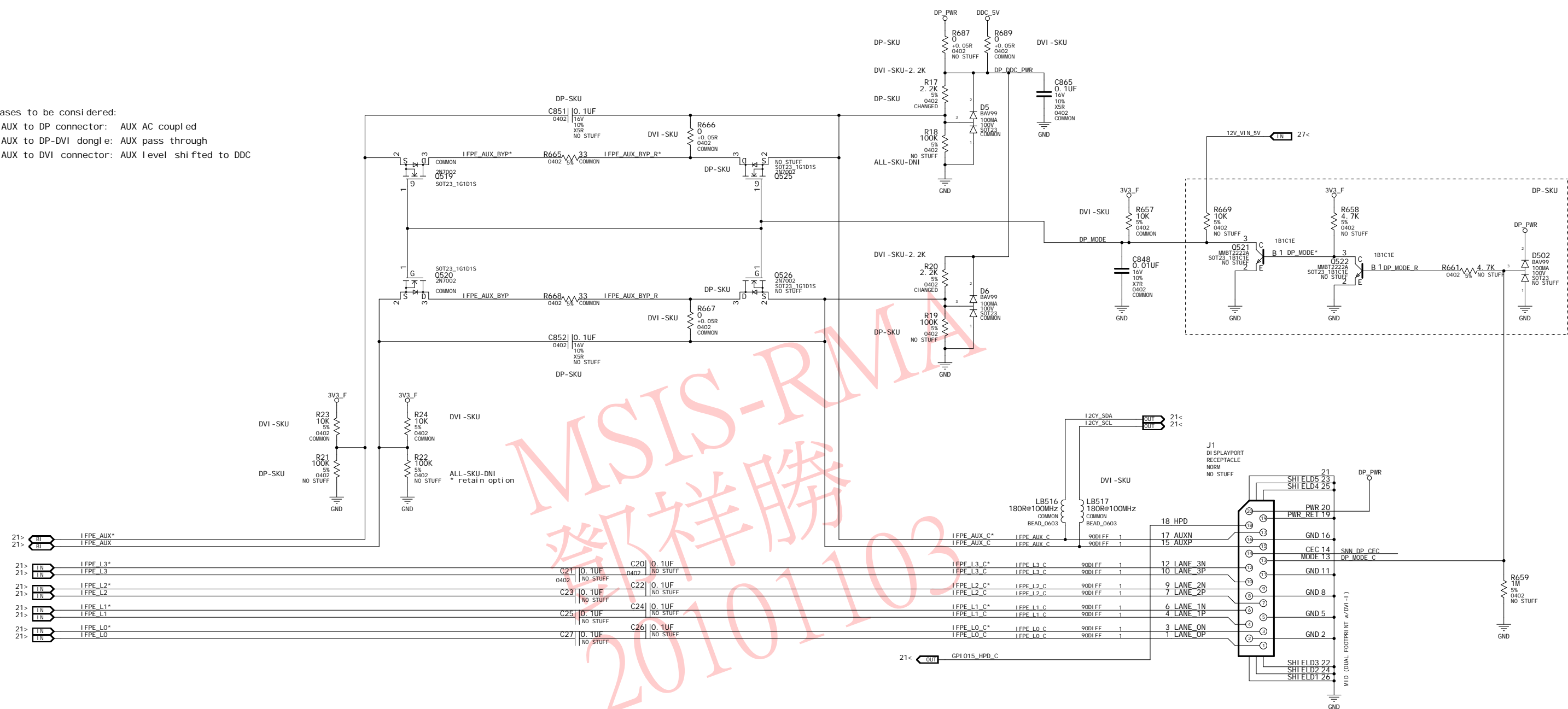
ASSEMBLY	P1041 GF104-350 1024MB GDDR5 32Mx32 Frame Buffer DVI -I +DVI -I =mHDMI
PAGE DETAIL	1 FPEF DVI -DL (Mi d)

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVI DI A CORPORATI ON 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN		600-11041-0010-QS1		
PCB REV		P1041-B01		PAGE 21 OF 34
BOM REV		DATE		06-MAY-2010

Three cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through
3. DP AUX to DVI connector: AUX level shifted to DDC



ASSEMBLY	P1041 GF104-350 1024MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDM
PAGE DETAIL	1 FPEF DP (Mid)

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

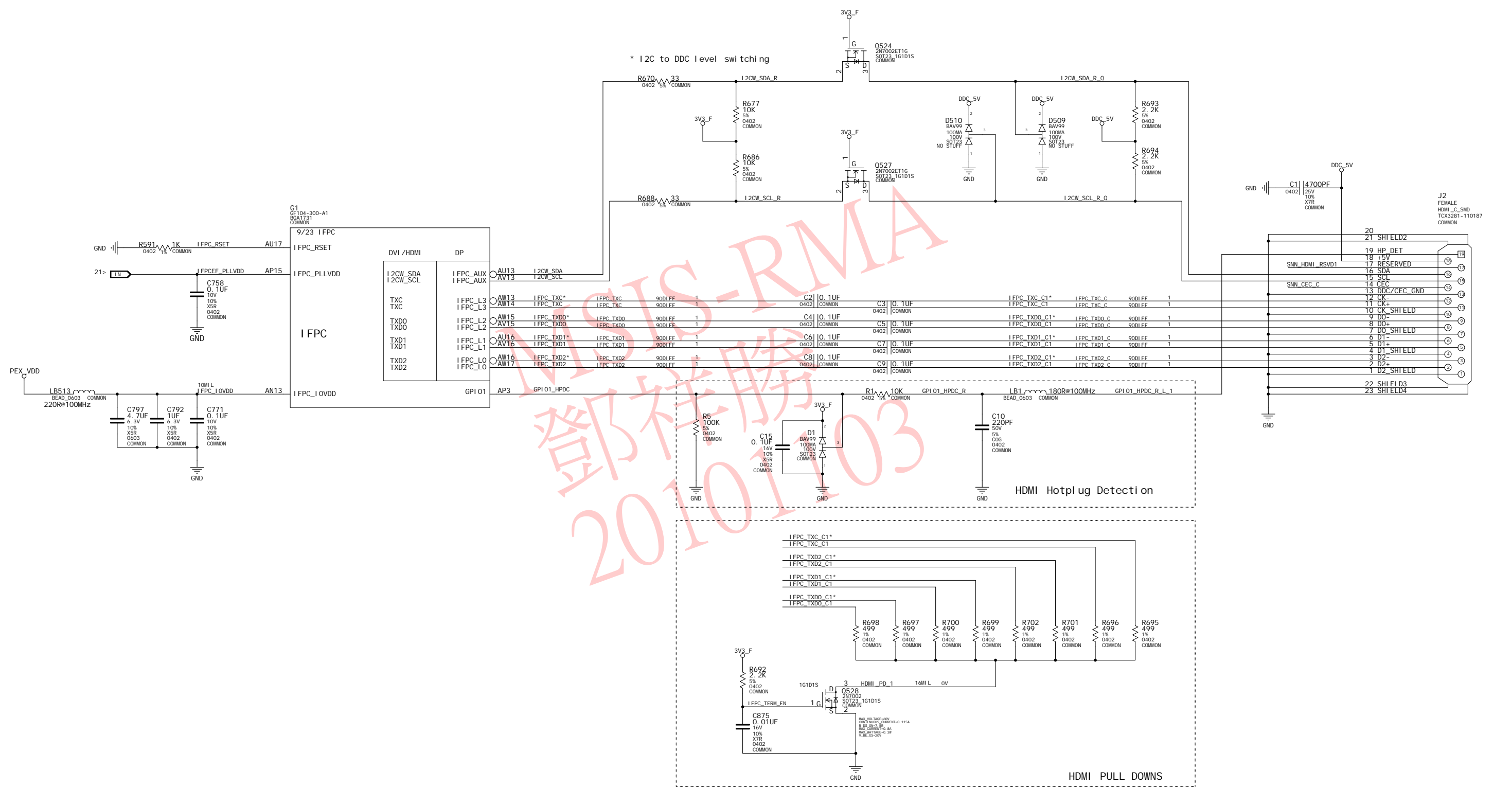
NVI DIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



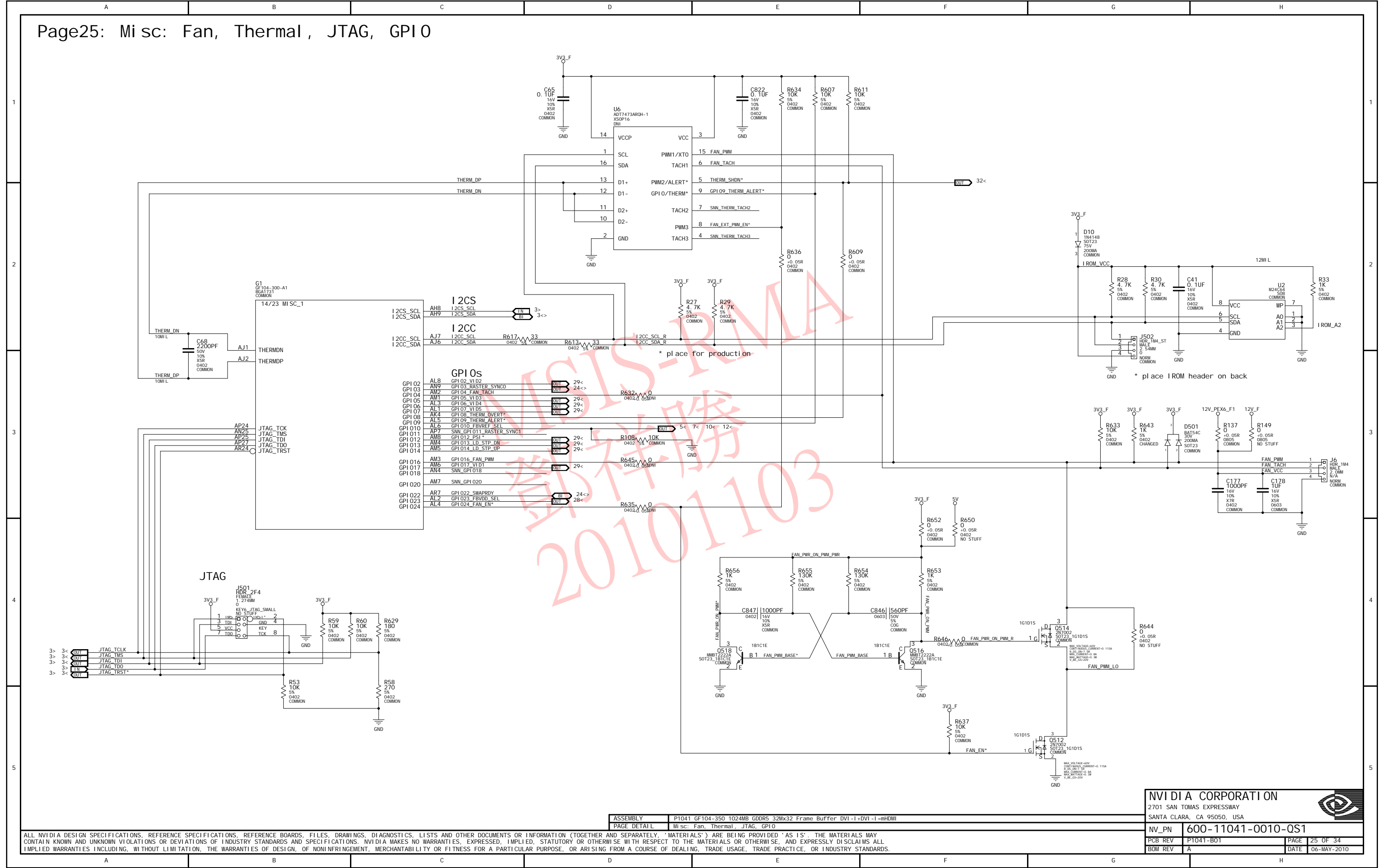
NV_PN	600-11041-0010-QS1
-------	--------------------

PCB REV	P1041-B01	PAGE	22 OF 34
BOM REV	A	DATE	06-MAY-2010



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-11041-0010-QS1		
PCB REV	P1041-B01	PAGE	23 OF 34
BOM REV	A	DATE	06-MAY-2010



ASSEMBLY	P1041 GF104-350 1024MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
PAGE DETAIL	Misc: Fan, Thermal, JTAG, GPIO

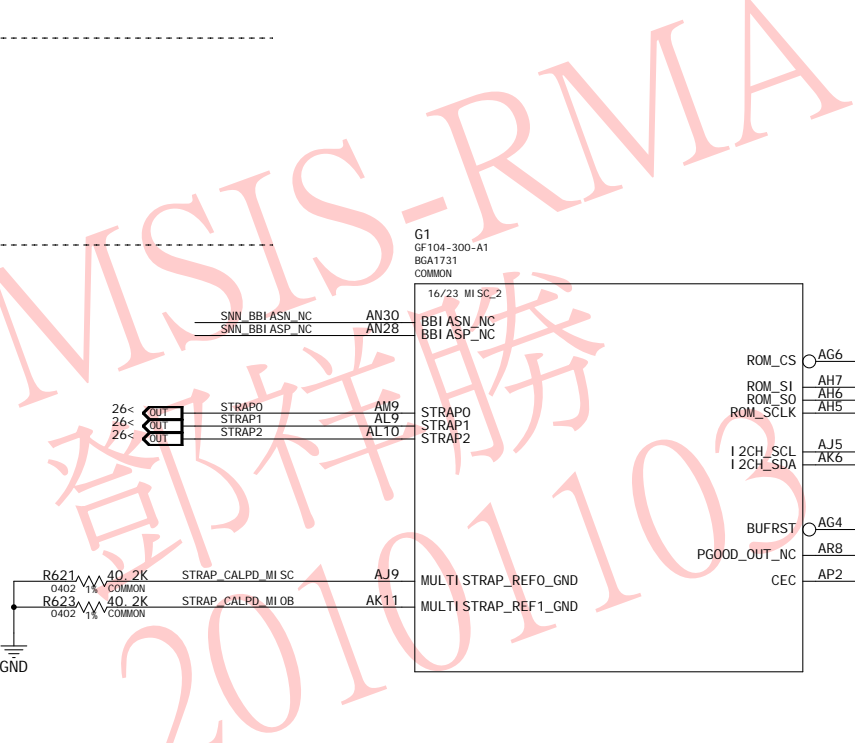
Page26: Mi sc: ROM, HDCP, XTAL, Straps

STRAPO	USER_BIT [3..0]	0000: => 5K PD
STRAP1	3GIO_PADCFG_LUT_ADR	0000 : =>5K PD 0000 Desktop
STRAP2	PCI_DEVID [3:0]	0010 For 0x0E22 : => 15K PD 0100 For 0x0E24 : => 25K PD
ROM_SI	RAMCFG[0]	32Mx32 256 bit Samsung for SKU 10 first memory 0011: PD 20K 32Mx32 256 bit Hynix for SKU 10 2'nd memory 0010: PD 15K
	RAMCFG[1]	
	RAMCFG[2]	32Mx32 192 bit Samsung for SKU 0 first memory 1011: PU 20K 32Mx32 192 bit Hynix for SKU 0 2'nd memory 1010: PU 15K
	RAMCFG[3]	
ROM_SO	VGA_DEVICE	1
	SMB_ALT_ADDR	0
	FB[0]_BAR_SIZE	0
ROM_SCLK	XCLK_417	0
	PEX_PLL_EN_TERM100	1 ENABLED
	SLOT_CLK_CFG	1 ENABLE
	SUB_VENDOR	1 Dedicated BIOS
	PCI_DEVID_EXT	0 0xC
		10k PD
		45K PD

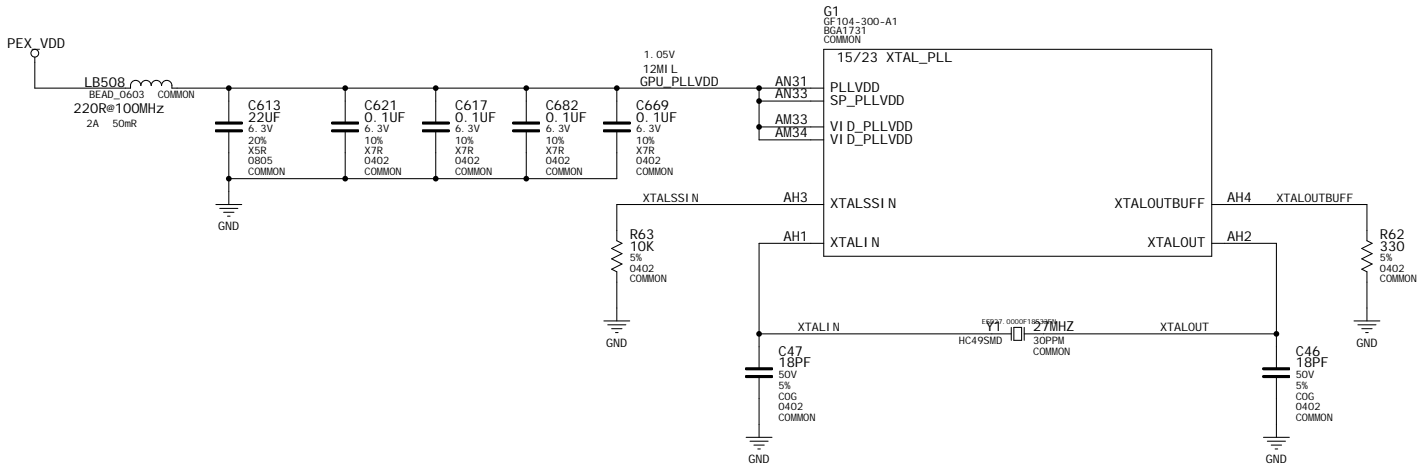
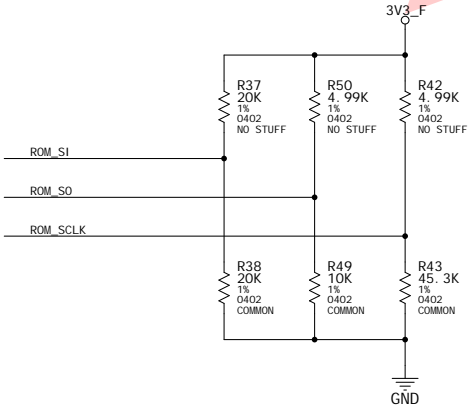
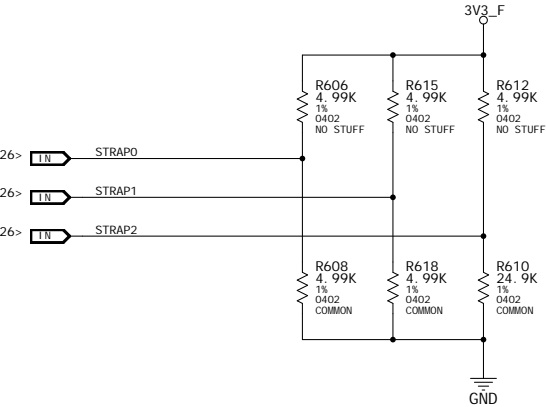
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit Qimonda	
0010	32Mx32 256-bit Hynix	
0011	32Mx32 256-bit Samsung	
0100	Reserved	
0101	64Mx32 256-bit Qimonda	
0110	64Mx32 256-bit Hynix	
0111	64Mx32 256-bit Samsung	
1000	Reserved	
1001	32Mx32 192-bit Qimonda	
1010	32Mx32 192-bit Hynix	
1011	32Mx32 192-bit Samsung	
1100	Reserved	
1101	64Mx32 192-bit Qimonda	
1110	64Mx32 192-bit Hynix	
1111	64Mx32 192-bit Samsung	

MISCSNET RULES			
NET	NV_CRI TICAL	NV_I MPEDANCE	
XTALSSIN	1	50OHM	
XTALIN	1	50OHM	
XTALOUT	1	50OHM	

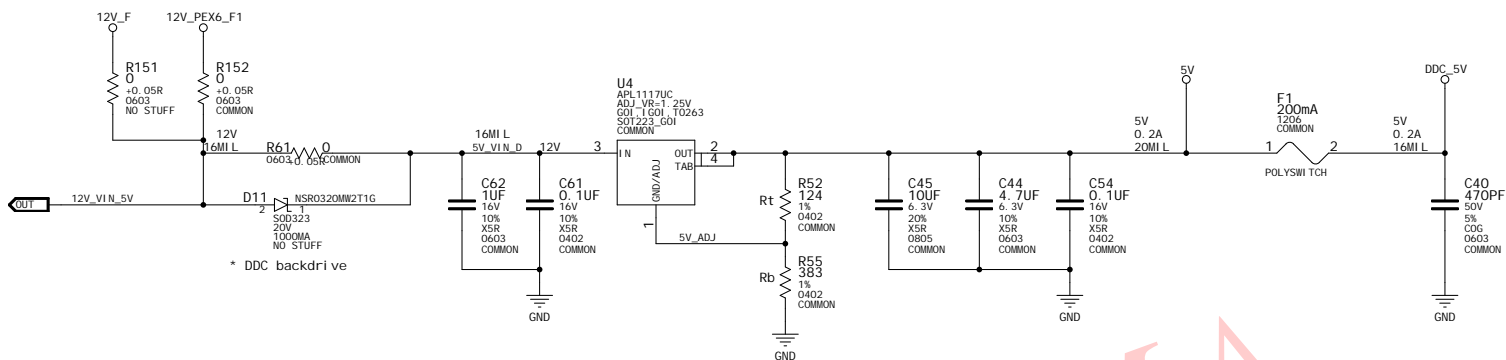


BINARY PRODUCTION	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY BRINGUP	NC	NC
MULTI-LEVEL	40.2k 1% TO GND	40.2k 1% TO GND



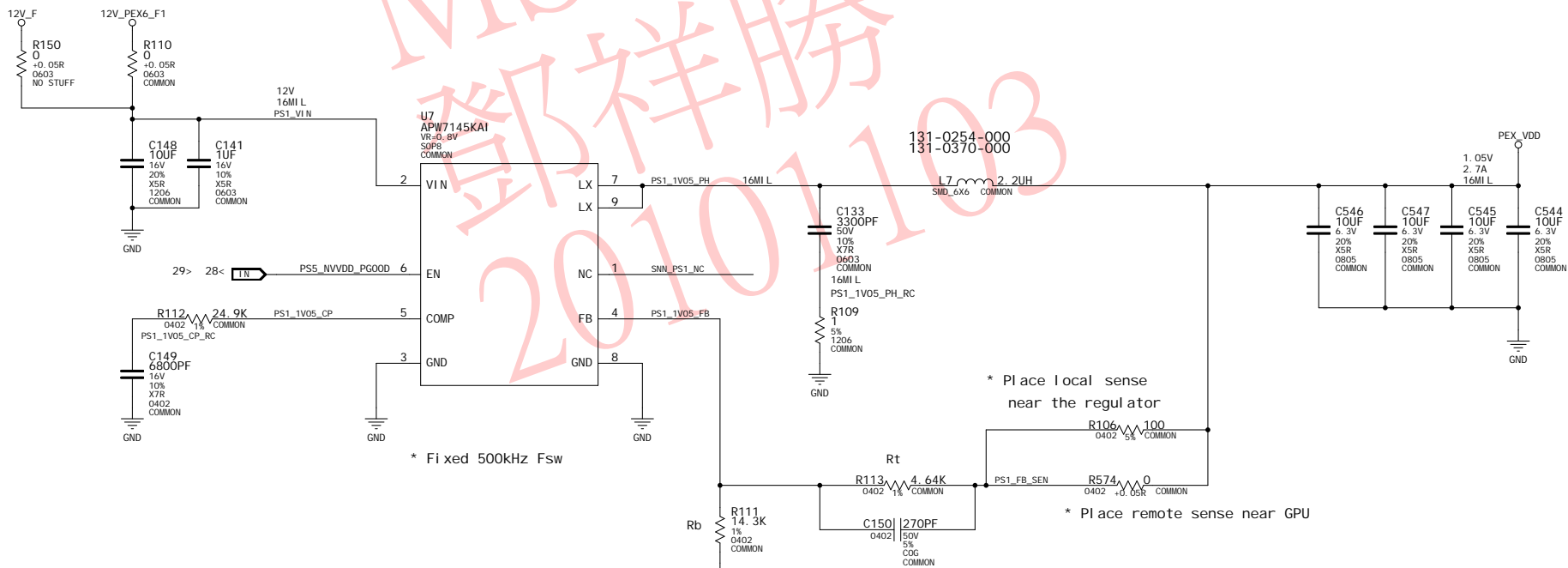
NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-11041-0010-QS1		
PCB REV	P1041-B01	PAGE	26 OF 34
BOM REV	A	DATE	06-MAY-2010

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

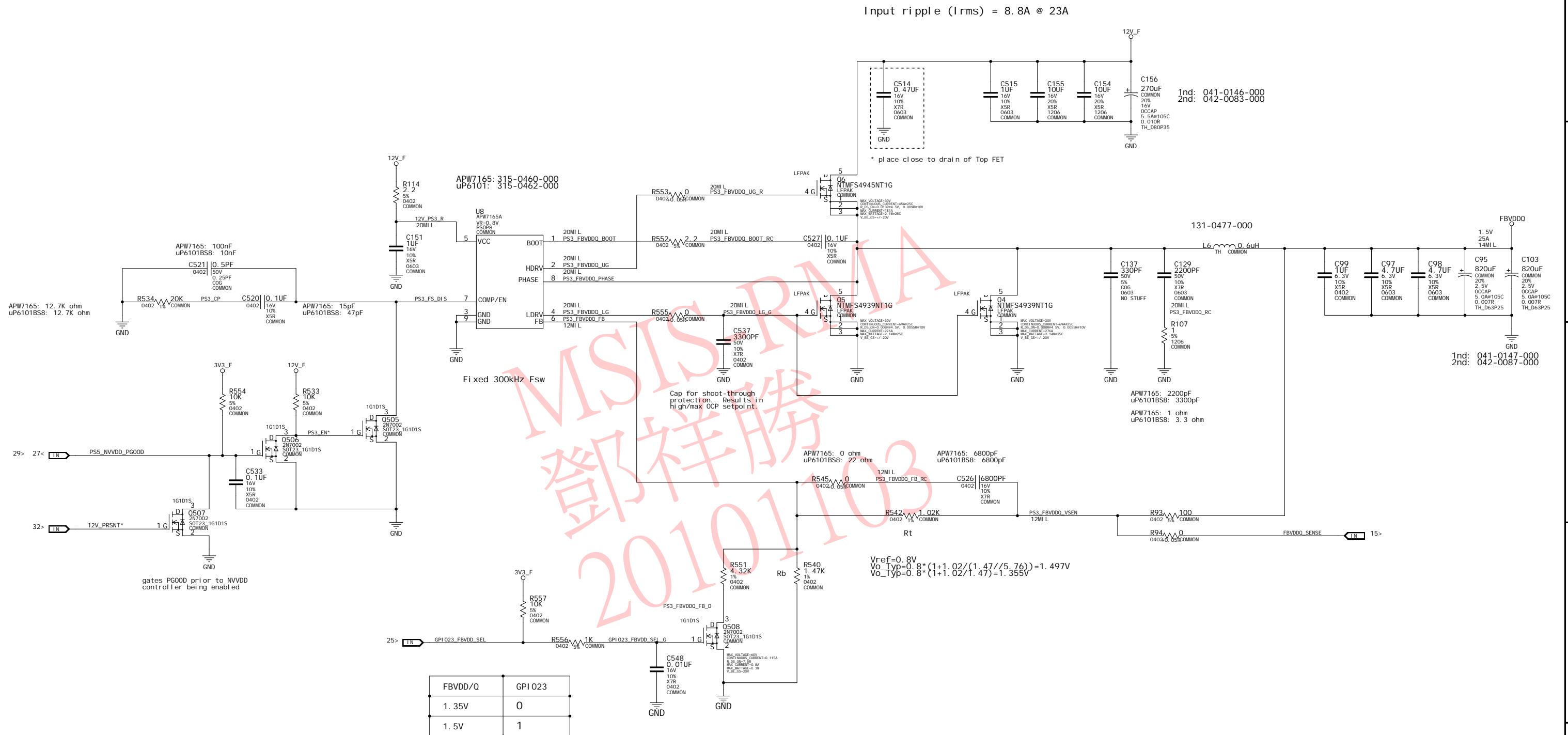


$$V_{ref}=1.256V$$
$$V_{o_typ}=1.256 \times (1 + \frac{383}{124}) + 60\mu A \times 383 = 5.16V$$

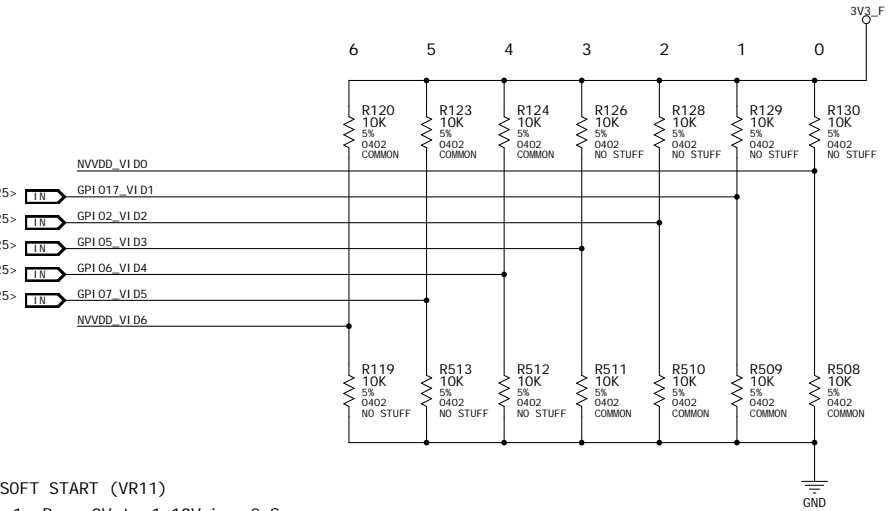
Input ripple (I rms) = -0.9A @ 2.7A



$$V_{ref}=0.8V$$
$$V_{o_typ}=0.8 \times (1 + \frac{R_t}{R_b}) = 1.0467V$$
$$V_{o_typ}=0.8 \times (1 + \frac{4.64K}{14.3K}) = 1.0596V$$

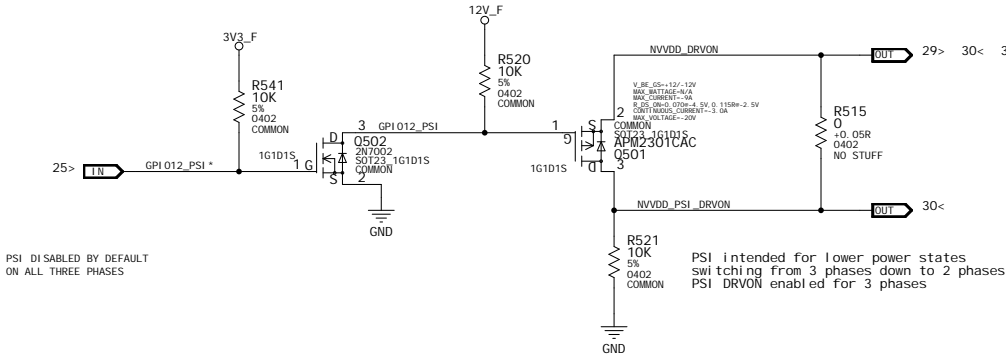


VID Table					
GPI 07	GPI 06	GPI 05	GPI 02	GPI 017	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V



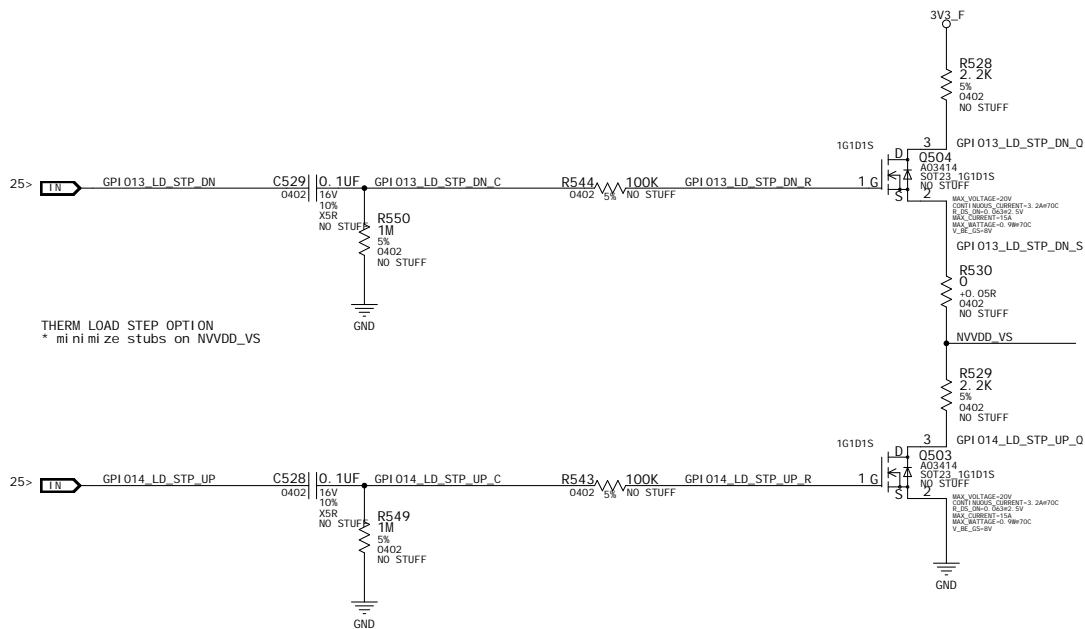
- SOFT START (VR11)
1. Ramp OV to 1.10V in ~2mS
 2. Hold at 1.10V for 170uS
 3. Read VID
 4. VID set to 0.9V during GPIO tri-state
VID[5:1]=11000 to set 0.9125V

- P-STATE VOLTAGES
1. P0 at 1.05V
 2. P8/P12 at 0.80V



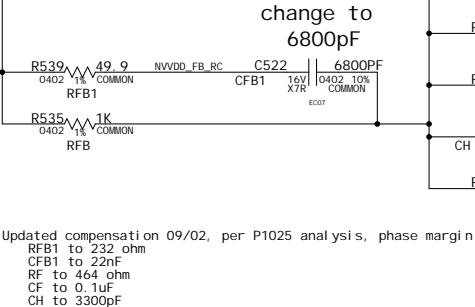
PSI DISABLED BY DEFAULT
ON ALL THREE PHASES

PSI intended for lower power states
Switching from 3 phases down to 2 phases
PSI DRVON enabled for 3 phases

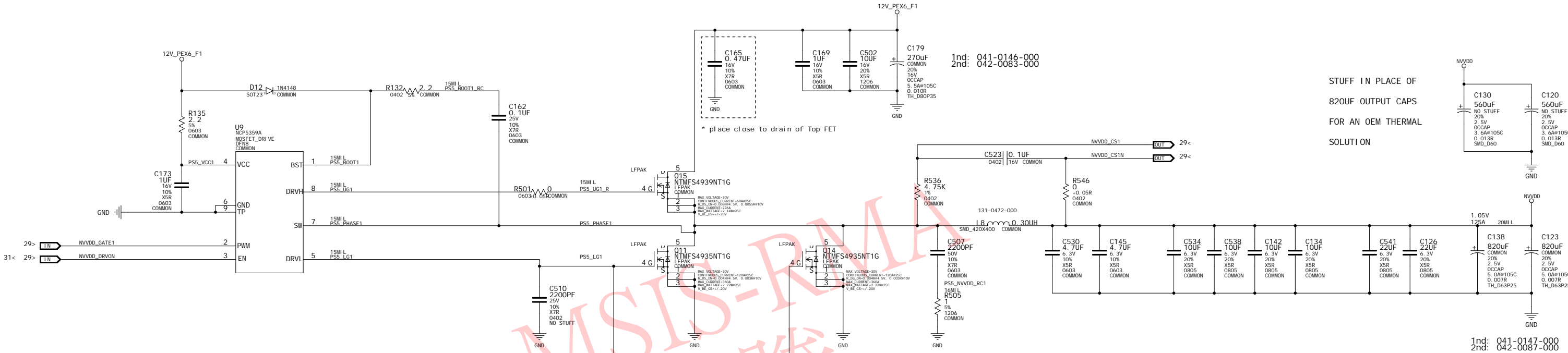


THERM LOAD STEP OPTION
* minimize stubs on NVVDD_VS

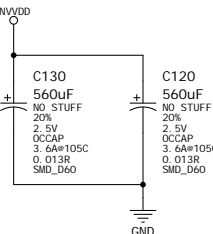
Vset offset option
* do not populate



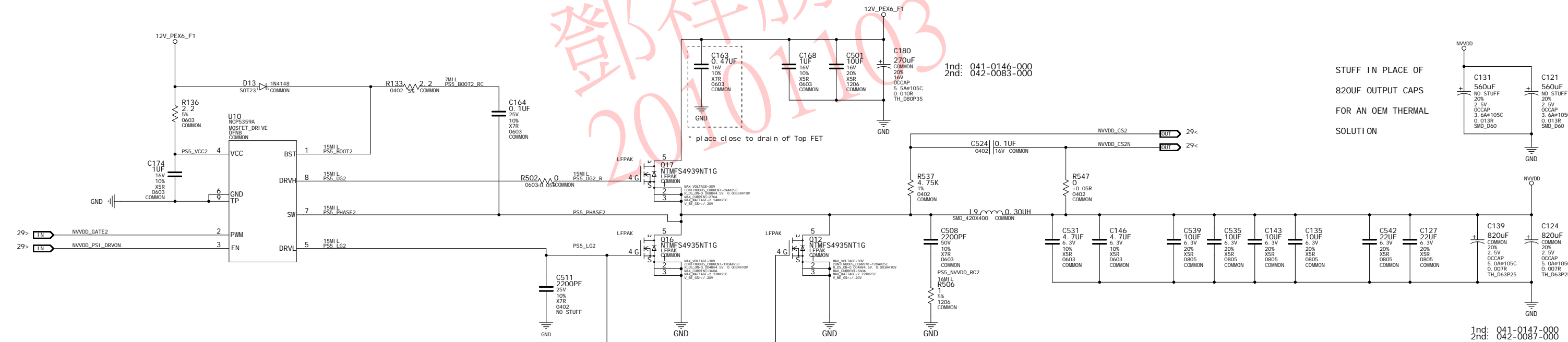
Input ripple (I_{rms})/phase = 10.175A @ 90A
I_{rms} shared across phase 1-2 input caps



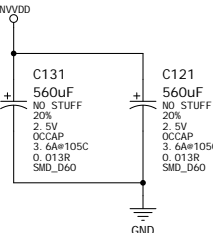
STUFF IN PLACE OF
820UF OUTPUT CAPS
FOR AN OEM THERMAL
SOLUTION



1nd: 041-0147-000
2nd: 042-0087-000



STUFF IN PLACE OF
820UF OUTPUT CAPS
FOR AN OEM THERMAL
SOLUTION

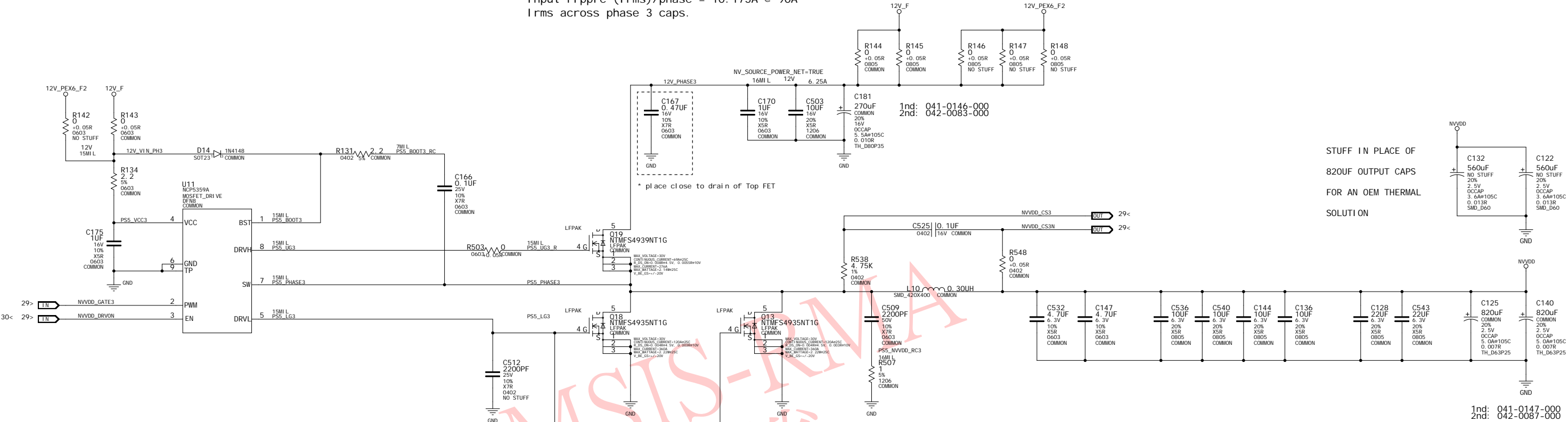


1nd: 041-0147-000
2nd: 042-0087-000

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-11041-0010-QS1		
PCB REV	P1041-B01	PAGE	30 OF 34
BOM REV	A	DATE	06-MAY-2010

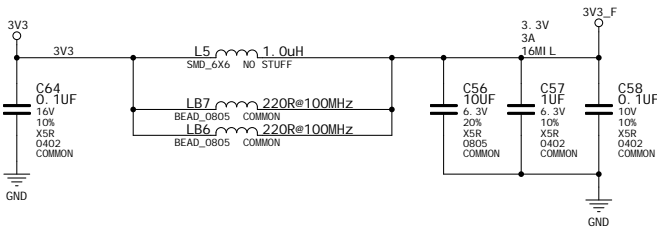
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

Input ripple (I_{rms})/phase = 10.175A @ 90A
I_{rms} across phase 3 caps.



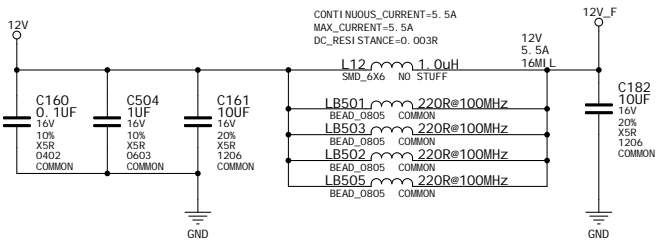
1

PEX 3V3 INPUT - 10W



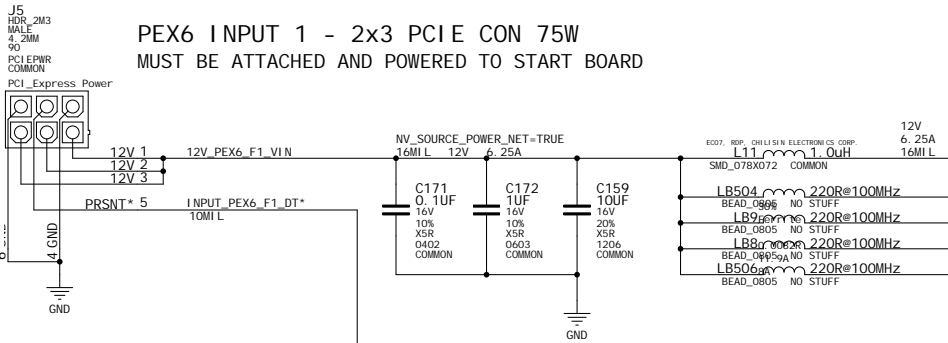
2

PEX_12V INPUT - 66W



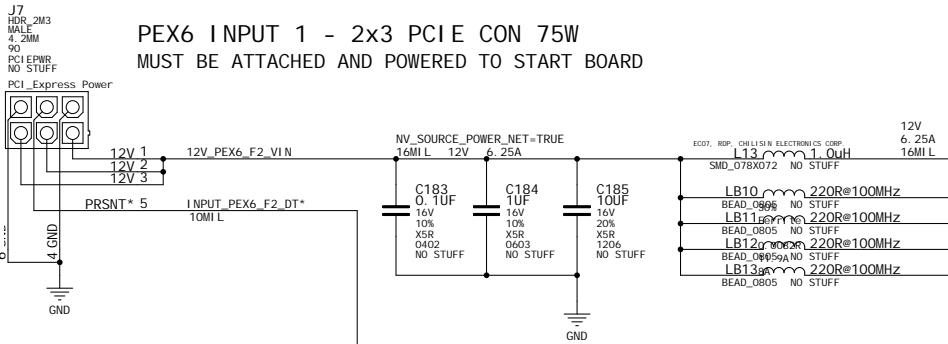
3

PEX6 INPUT 1 - 2x3 PCIe CON 75W
MUST BE ATTACHED AND POWERED TO START BOARD



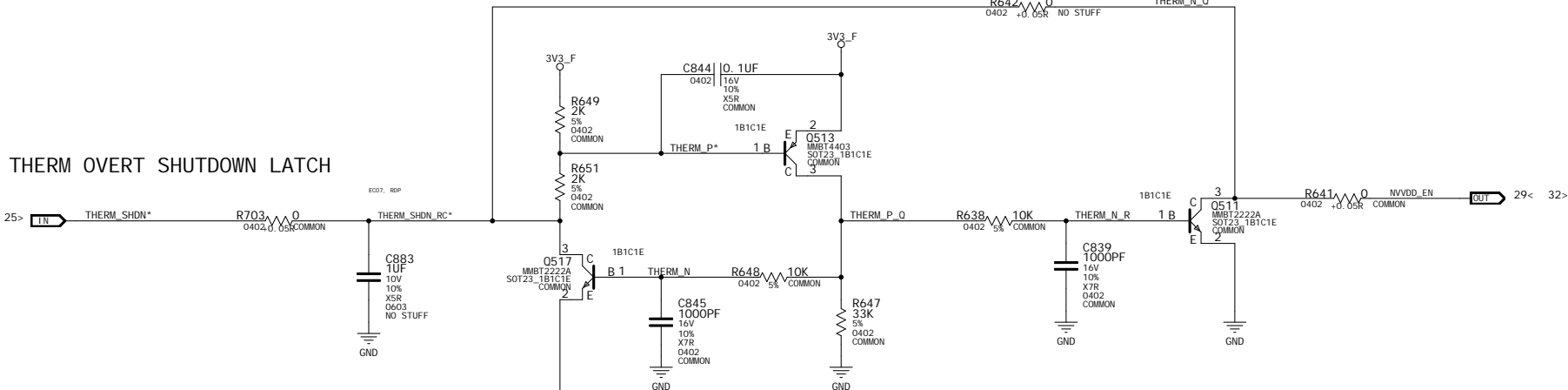
4

PEX6 INPUT 1 - 2x3 PCIe CON 75W
MUST BE ATTACHED AND POWERED TO START BOARD

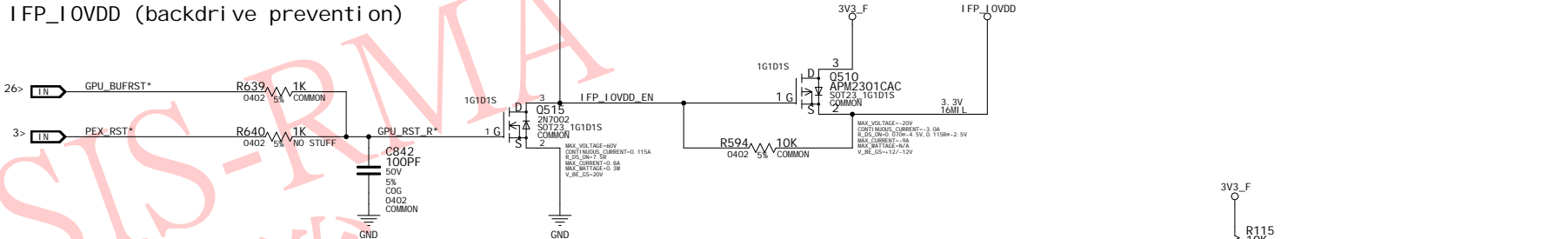


5

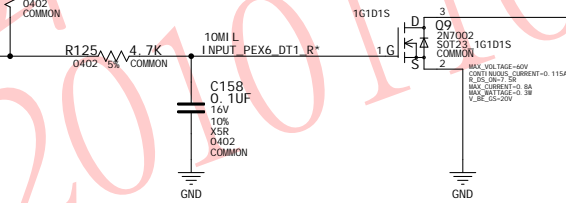
THERM OVERT SHUTDOWN LATCH



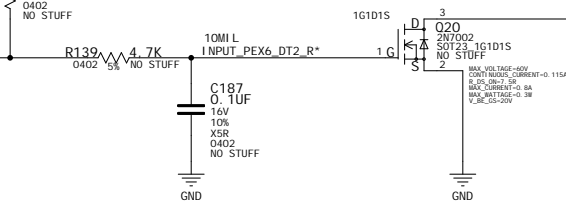
I FP_I0VDD (backdrive prevention)



PEX Input Present 1



PEX Input Present 1



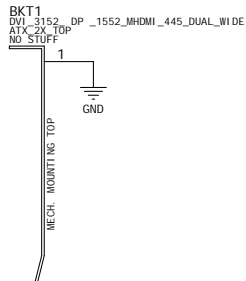
STUFF IF ONLY
ONE 6-PIN POWER
CONNECTOR IS USED

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-11041-0010-QS1		
PCB REV	P1041-B01	PAGE	32 OF 34
BOM REV	A	DATE	06-MAY-2010

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

Brackets:

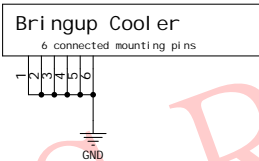
Bracket with DVI_DP_mHDMI : 151-10001-0355-071



Bracket Screw

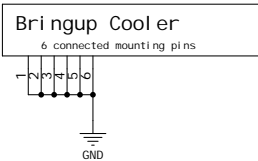


Cooler/GPU Sti ffener



MEC3
HSA GF104
6PIN
NO STUFF

P1041 MOUNTING HOLE LOCATIONS



MEC1
p1041_mech_hole
6PIN
NO STUFF

	A	B	C	D	E	F	G	H
1	Page34: Bl ank							
2								
3								
4								
5								

MSIS-RMA
鄧祥勝
20101103

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	P1041 GF104-350 1024MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
PAGE DETAIL	Blank

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-11041-0010-QS1		
PCB REV	P1041-B01	PAGE	34 OF 34
BOM REV	A	DATE	06-MAY-2010

