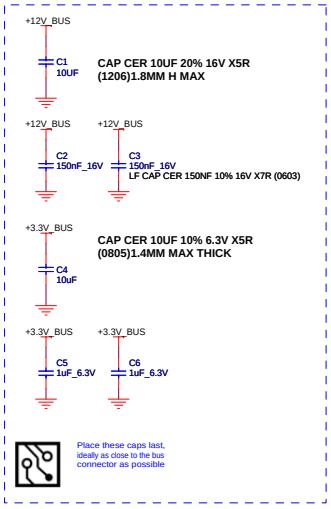
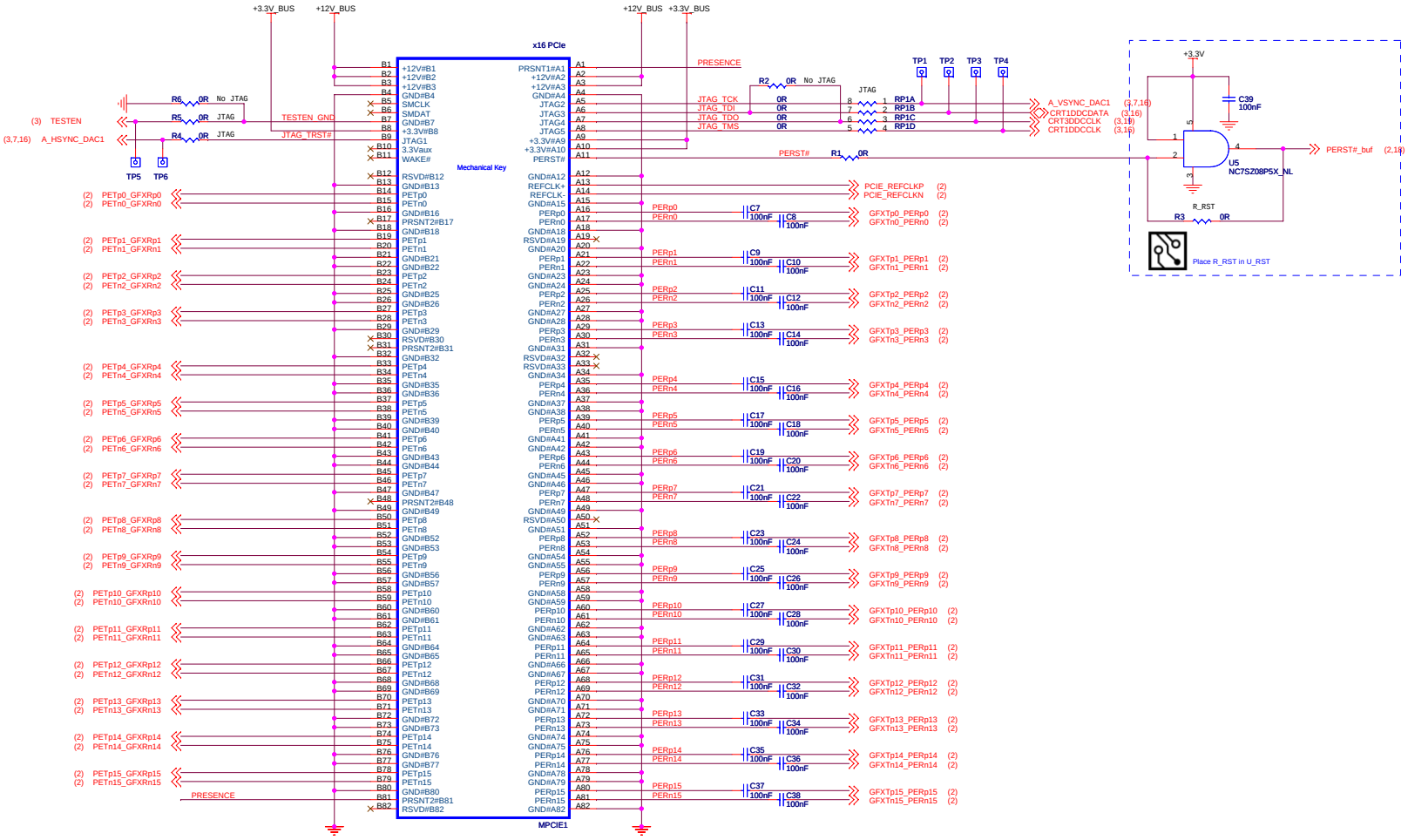
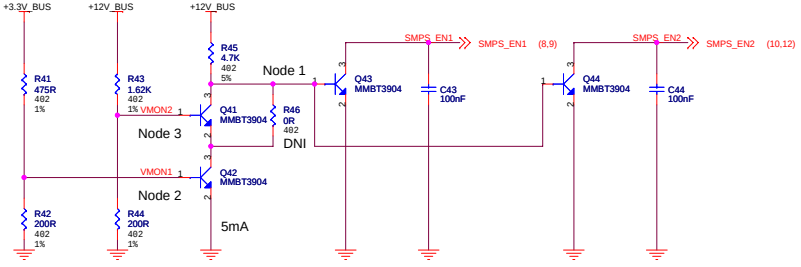
PCI-EXPRESS EDGE CONNECTOR







POWER SEQUENCING

Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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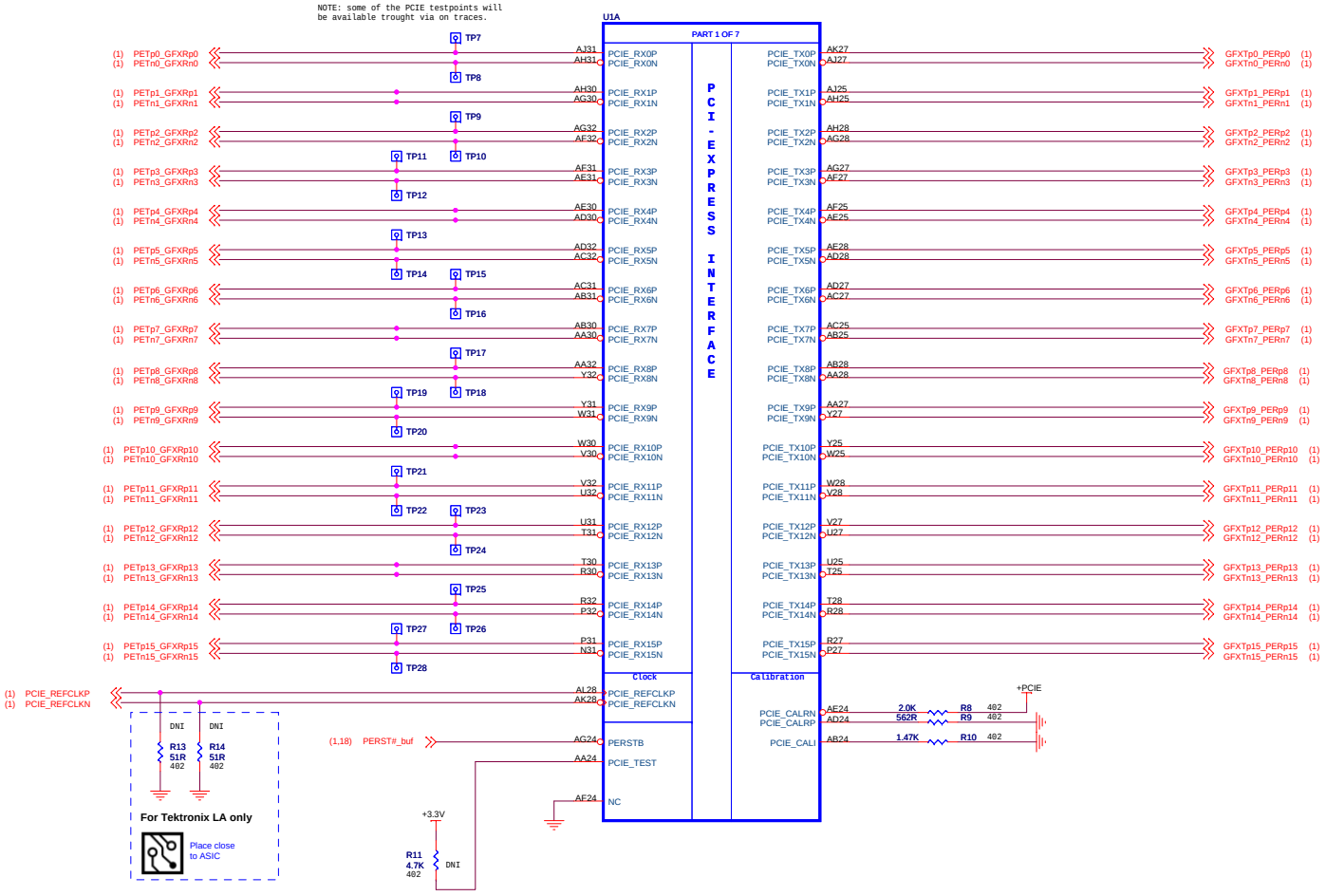

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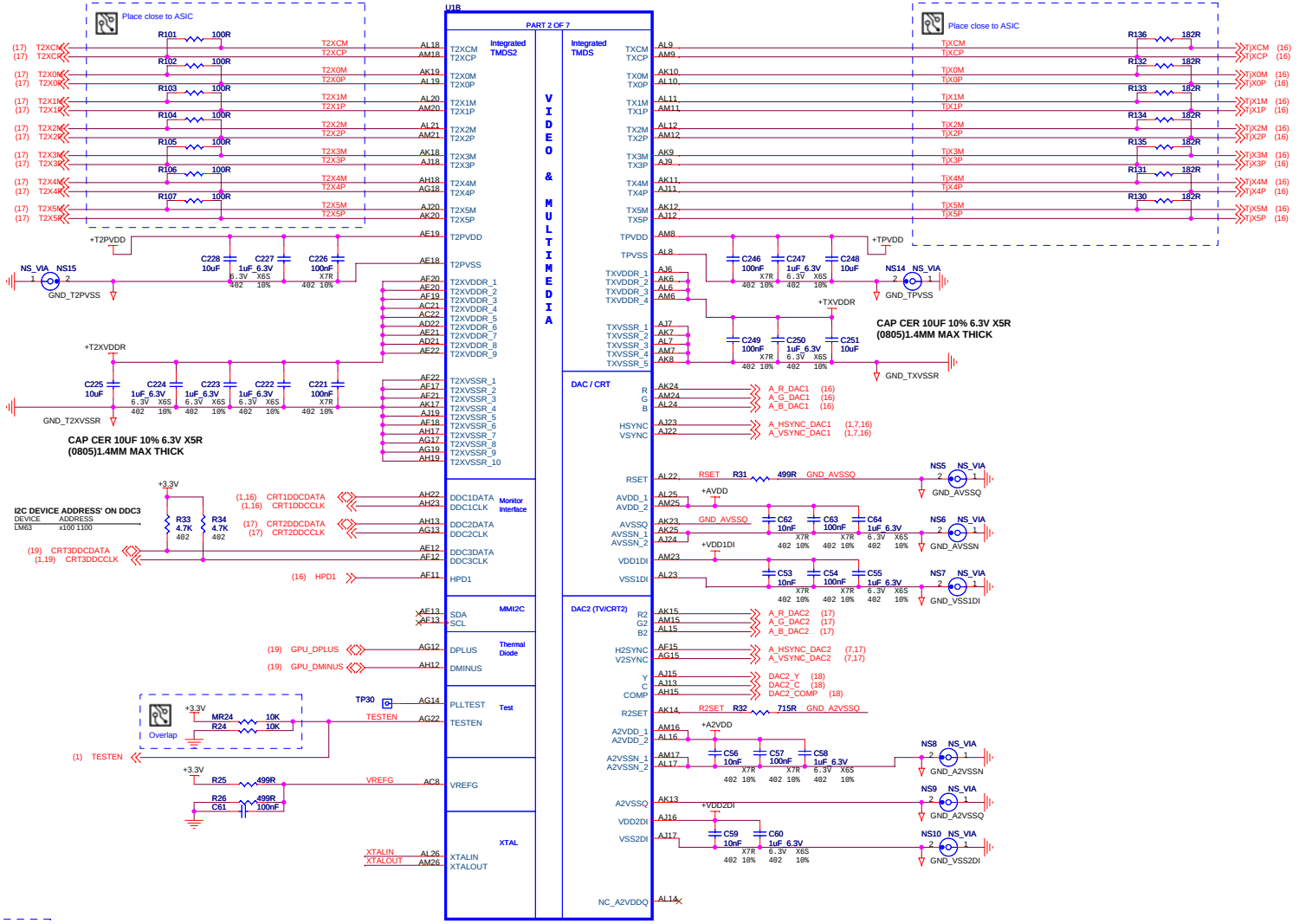
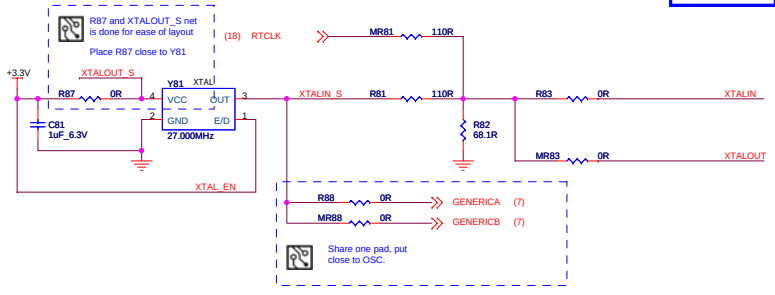
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X5R, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402





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Recommended caps:
(see BOM for qualified values/vendors)
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1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402

U1E

PART 5 OF 7

POWER

Memory I/O

PCI-Express

Core

Memory I/O Clock

DVO I/O

I/O Internal

Selected PLL's

+MVDD

C301 C302 C303 C304 C305 C306 C307 C308 C309 C310 1uF_6.3V

C311 C312 C313 C314 C315 C316 C317 C318 C319 C320 1uF_6.3V

C321 C322 C326 C327 C328 C329 C330 1uF_6.3V

C341 C342 C343 C344 C345 10uF

CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

VDDR1_1 J1 M1 R1 V1 AA1 A3 P9 J10 N9 P10 A9 Y10 P8 R9 Y9 J11 A21 M10 N10 Y8 J18 J19 K21 A12 H13 A15 J20 J13 K11 K19 A18 L23 K20 K24 L24 H19 A24 K13 J32 A30 C32 F32 L32

VDDR1_2 VDDR1_3 VDDR1_4 VDDR1_5 VDDR1_6 VDDR1_7 VDDR1_8 VDDR1_9 VDDR1_10 VDDR1_11 VDDR1_12 VDDR1_13 VDDR1_14 VDDR1_15 VDDR1_16 VDDR1_17 VDDR1_18 VDDR1_20 VDDR1_21 VDDR1_22 VDDR1_23 VDDR1_24 VDDR1_25 VDDR1_26 VDDR1_27 VDDR1_28 VDDR1_29 VDDR1_30 VDDR1_31 VDDR1_32 VDDR1_33 VDDR1_34 VDDR1_35 VDDR1_36 VDDR1_37 VDDR1_38 VDDR1_39 VDDR1_40 VDDR1_41 VDDR1_42 VDDR1_43 VDDR1_45 VDDR1_46

+MVDD

B54 BLM15BD121SN1
B55 BLM15BD121SN1

C231 C232 C233 C234 1uF_6.3V

NS16 NS_VIA
NS17 NS_VIA
GND_VSSRH0
GND_VSSRH1

VDDRH0 A27 VDDRH1 F1
VSSRH0 A28 VSSRH1 F1

+3.3V

C241 C242 C243 C244 1uF_6.3V
C245 10uF

CAP CER 10UF 10%
6.3V X5R (0805)1.4MM
MAX THICK

VDDR3_1 AB9 VDDR3_2 AB10 VDDR3_3 AA9 VDDR3_4 AC19 VDDR3_5 AD18 VDDR3_6 AC20 VDDR3_7 AD19 VDDR3_8 AD20

+VDDR_DVP

C236 C237 C238 C239 1uF_6.3V

VDDR4_1 AJ5 VDDR4_2 AM5 VDDR4_3 AL5 VDDR4_4 AK5

VDDR5_1 AE2 VDDR5_2 AE3 VDDR5_3 AE4 VDDR5_4 AE5

+PVDD

C69 10nF C70 100nF C71 1uF_6.3V

NS12 NS_VIA
GND_PVSS

PVDD AJ14
PVSS AH14

PCIE_PVDD_12_1 V23 PCIE_PVDD_12_2 N23 PCIE_PVDD_12_3 P23 PCIE_PVDD_12_4 U23

PCIE_PVSS W23

C201 C202 C203 C204 1uF_6.3V

NS18 NS_VIA
GND_PCIE_PVSS

PCIE_VDDR_12_1 N29 PCIE_VDDR_12_2 N28 PCIE_VDDR_12_3 N27 PCIE_VDDR_12_4 N26 PCIE_VDDR_12_5 N25 PCIE_VDDR_12_6 AL31 PCIE_VDDR_12_7 AM31 PCIE_VDDR_12_8 AM30 PCIE_VDDR_12_9 AL32 PCIE_VDDR_12_10 AL30 PCIE_VDDR_12_11 AM28 PCIE_VDDR_12_12 AL29 PCIE_VDDR_12_13 AM29 PCIE_VDDR_12_14 AM27

C191 C192 C193 C194 C195 C196 C197 C198 1uF_6.3V
C199 C200 10uF

CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

VDDC_1 AC11 VDDC_2 AC12 VDDC_3 P14 VDDC_4 U15 VDDC_5 W14 VDDC_6 W15 VDDC_7 R17 VDDC_8 R15 VDDC_9 V15 VDDC_10 V16 VDDC_11 T16 VDDC_12 U16 VDDC_13 T17 VDDC_14 U17 VDDC_15 V14 VDDC_16 R18 VDDC_17 T18 VDDC_18 V18 VDDC_19 P18 VDDC_20 P19 VDDC_21 R19 VDDC_22 W19 VDDC_23 AD11 VDDC_24 N13 VDDC_25 N14 VDDC_26 N19 VDDC_27 N20 VDDC_28 P13 VDDC_29 P20 VDDC_30 W13 VDDC_31 W20 VDDC_32 Y13 VDDC_33 Y14 VDDC_34 Y19 VDDC_35 Y20 VDDC_36 AC14 VDDC_37 M23 VDDC_38 V10 VDDC_39 K18

C161 C162 C163 C164 C165 C166 C167 C168 C169 C170 1uF_6.3V
C181 C182 C183 10uF

C171 C172 C173 C174 C175 C176 C177 C178 C179 C180 1uF_6.3V

C151 C152 1uF_6.3V

CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

VDDCI_1 W10 VDDCI_2 T14 VDDCI_3 W17 VDDCI_4 P16 VDDCI_5 T23 VDDCI_6 K14 VDDCI_7 U19 VDDCI_8

C211 C212 C216 1uF_6.3V
C213 10uF

VDD25_1 AC13 VDD25_2 AC16 VDD25_3 AC18 VDD25_4 L10 VDD25_5 K22 VDD25_6 AA10

C206 C207 C208 C209 1uF_6.3V
C210 10uF

MPVDD A6
MPVSS A5

C67 1uF_6.3V C66 100nF C65 10nF
C68 22uF_16V

NS_VIA NS11
GND_MPVSS

VDDPLL AC15

C214 C215 1uF_6.3V

B56 BLM15BD121SN1

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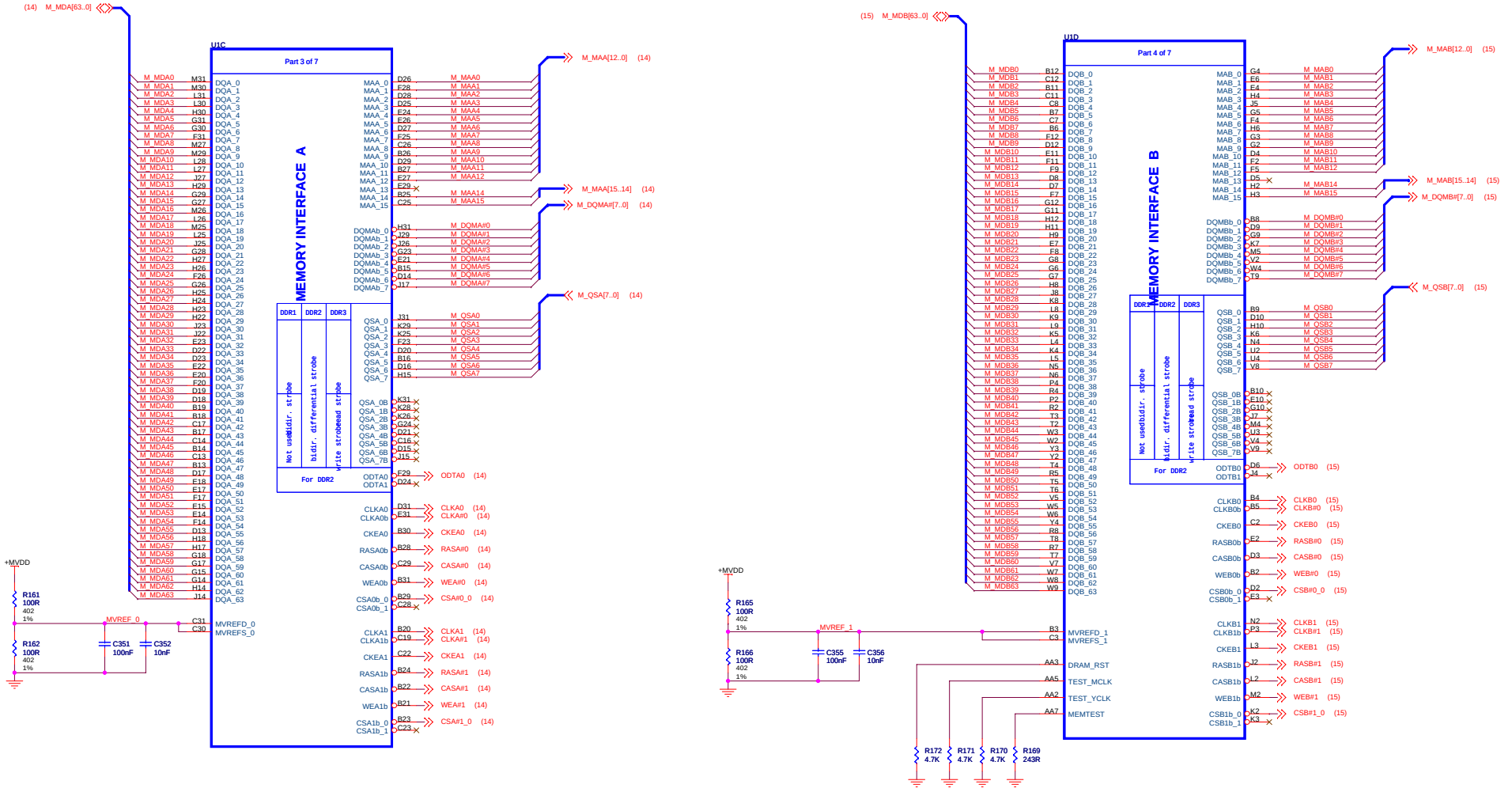

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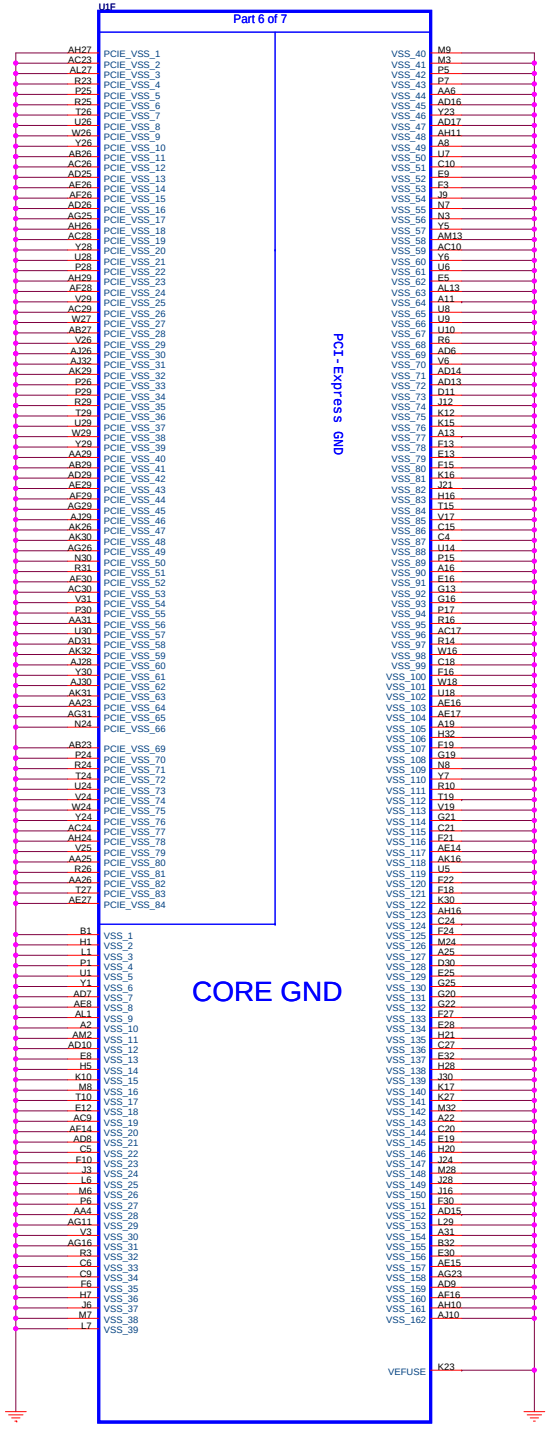

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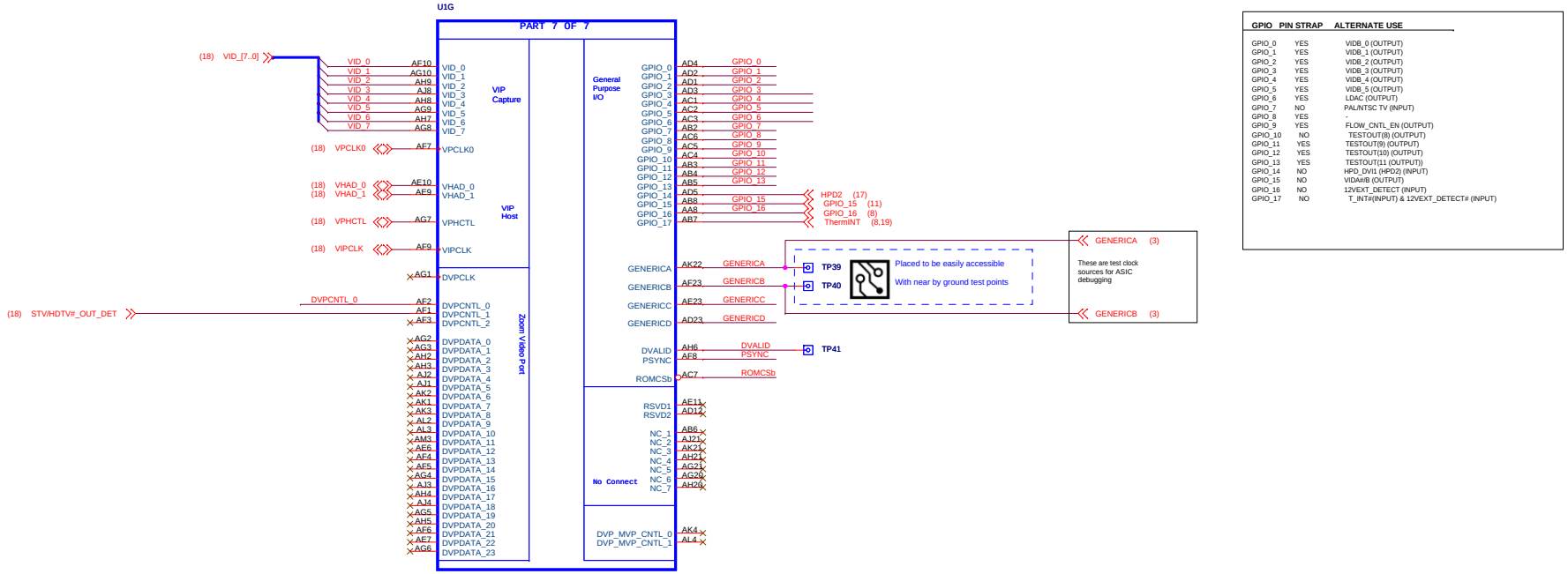


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDA#/B (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - Miscellaneous PCI-Express Modes
00: Halt impedance calibration before transmitter is enabled and enable receiver detection (Default setting for Desktop)
01: Allow impedance calibration to continue on in the background AFTER transmitter has been enabled and enable receive detection.
10: Bypass common-mode detection & receiver detection and halt impedance calibration before TX_EN.
11: Short-circuit internal loopback and halt impedance calibration before TX_EN and enable receiver detection.

GPIO(4) - DEBUG_ACCESS: 0 for normal operation, 1 for debug mode

GPIO(6:5) - PLL_IBIAS_RD (Reduced mirror bias setting for PHY PLL) ATI PCIE FEATURE III
Provide 4 different IBIAS settings - Set to 00 for R520

GPIO(8) - FORCE_COMPLIANCE: 0 for Normal operation, 1 for Force into Compliance Mode

GPIO(9,13:11) - ROMIDCFG[3..0]
1001 - 1M AT25F1024 ROM (Atmel)
1010 - 1M AT45DB011 ROM (Atmel)
1011 - 1M M25P10 ROM (ST)
1100 - 512K M25P05 ROM (ST) (ATI default)
1101 - 1M SST45LF010 ROM (SST), 1M W45B512 ROM (WinBond), 512K W45B012 ROM (WinBond)
1110 - 1M SST25VF010 ROM (SST), 512K SST25VF512 ROM (SST)
1111 - 1M NX25F011B ROM (NexFlash)

VSYNC - VIP_DEVICE
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - DWNGRD ATI Feature I
This straps allow a Workstation bonded part to be downgraded to a normal part on a board. This allow inventory management to better balance demand.
0 - Device remain a Workstation grade part
1 - Part is downgraded to a Normal part

ATI Feature II
H2SYNC, V2SYNC, GENERICC - Star Memory System repair mode
000 - Default

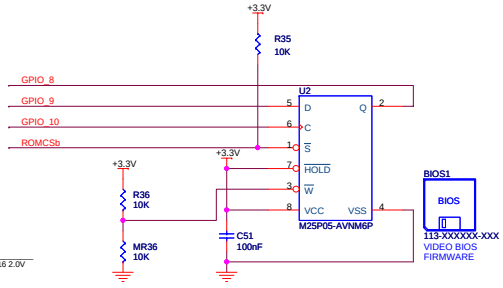
Memory Vendor Straps for DDR2 16Mx16 and 32Mx16: ----------> ATI Board Feature I

[31:24]@ MC_MISC_0	MEMTYPE[1:0] [DVPCNTL_0:GPIO_15]	Memory
20h	[0 : 0]	Common and Infineon 16Mx16 2.0V
21h	[0 : 1]	Samsung 16Mx16
22h	[1 : 0]	Infineon 16Mx16 1.8V
23h	[1 : 1]	Hynix 16Mx16
24h	[0 : 0]	Micron 16Mx16
25h	[0 : 1]	Elpida 16Mx16
26h	[1 : 0]	Reserved
27h	[1 : 1]	Reserved
28h	[0 : 0]	Common 32Mx16
29h	[0 : 1]	Samsung 32Mx16
2Ah	[1 : 0]	Infineon 32Mx16
2Bh	[1 : 1]	Hynix 32Mx16
2Ch	[0 : 0]	Micron 32Mx16
2Dh	[0 : 1]	Elpida 32Mx16
2Eh	[1 : 0]	Reserved
2Fh	[1 : 1]	Reserved

VGA DISABLE : 1 for disable (set to 0 for normal operation)

TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper position 2-3)
1 - NTSC TVO (Jumper position 1-2)

NOT USED.



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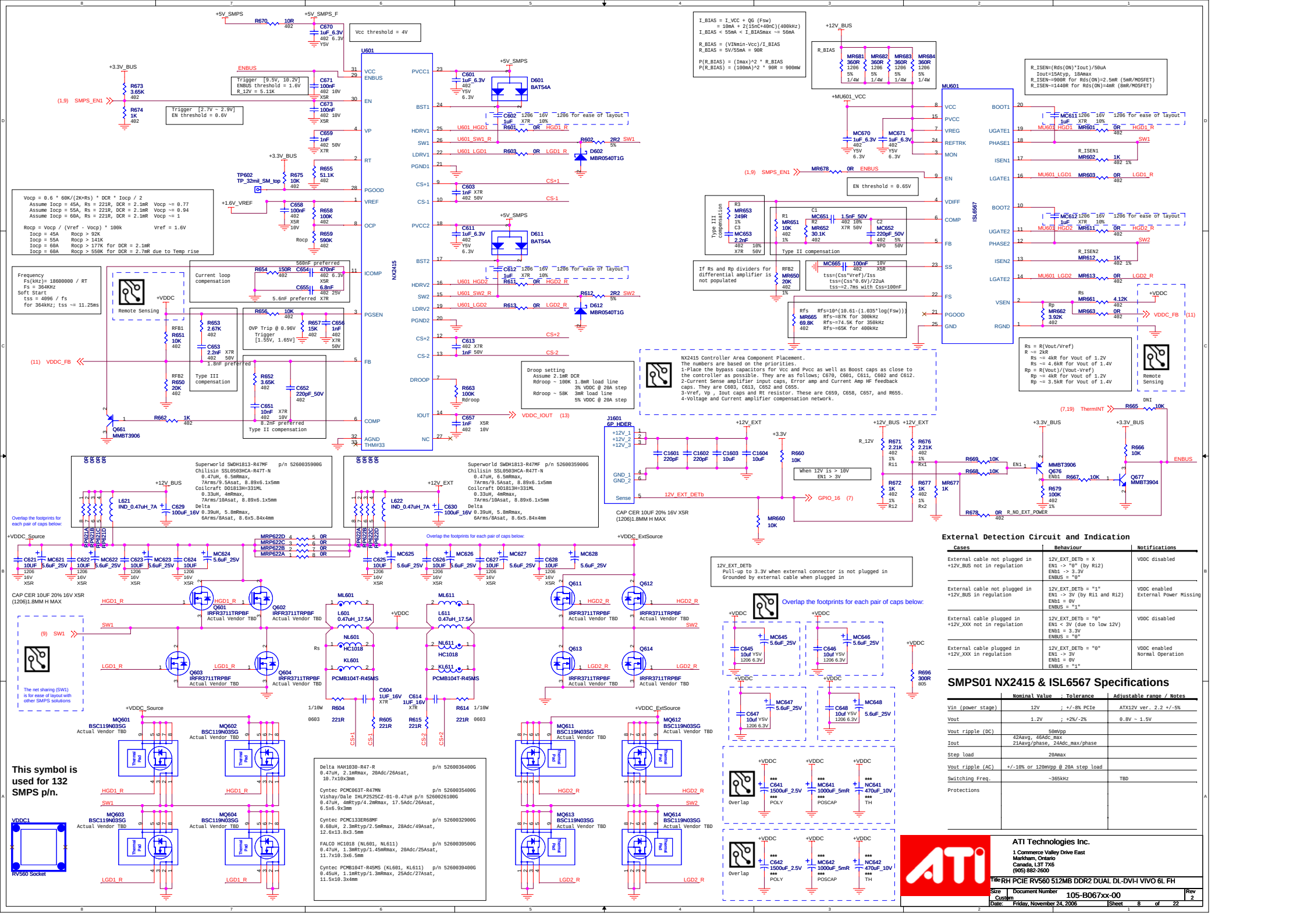

External Detection Circuit and Indication

Cases	Behaviour	Notifications
External cable not plugged in +12V_BUS not in regulation	12V_EXT_DETb = X EN1 -> "0" (by Ri2) ENb1 -> 3.3V ENBUS = "0"	VDDC disabled
External cable not plugged in +12V_BUS in regulation	12V_EXT_DETb = "1" EN1 -> 3V (by Ri1 and Ri2) ENb1 = 0V ENBUS = "1"	VDDC enabled External Power Missing
External cable plugged in +12V_XXX not in regulation	12V_EXT_DETb = "0" EN1 < 3V (due to low 12V) ENb1 = 3.3V ENBUS = "0"	VDDC disabled
External cable plugged in +12V_XXX in regulation	12V_EXT_DETb = "0" EN1 -> 3V ENb1 = 0V ENBUS = "1"	VDDC enabled Normal Operation

SMPS01 NX2415 & ISL6567 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	1.2V ; +2%/-2%	0.8V ~ 1.5V
Vout ripple (DC)	50mVpp	
Iout	42Aavg, 46Adc_max 21Aavg/phase, 24Adc_max/phase	
Step load	20Amax	
Vout ripple (AC)	+/-10% or 120mVpp @ 20A step load	
Switching Freq.	~365kHz	TBD
Protections		

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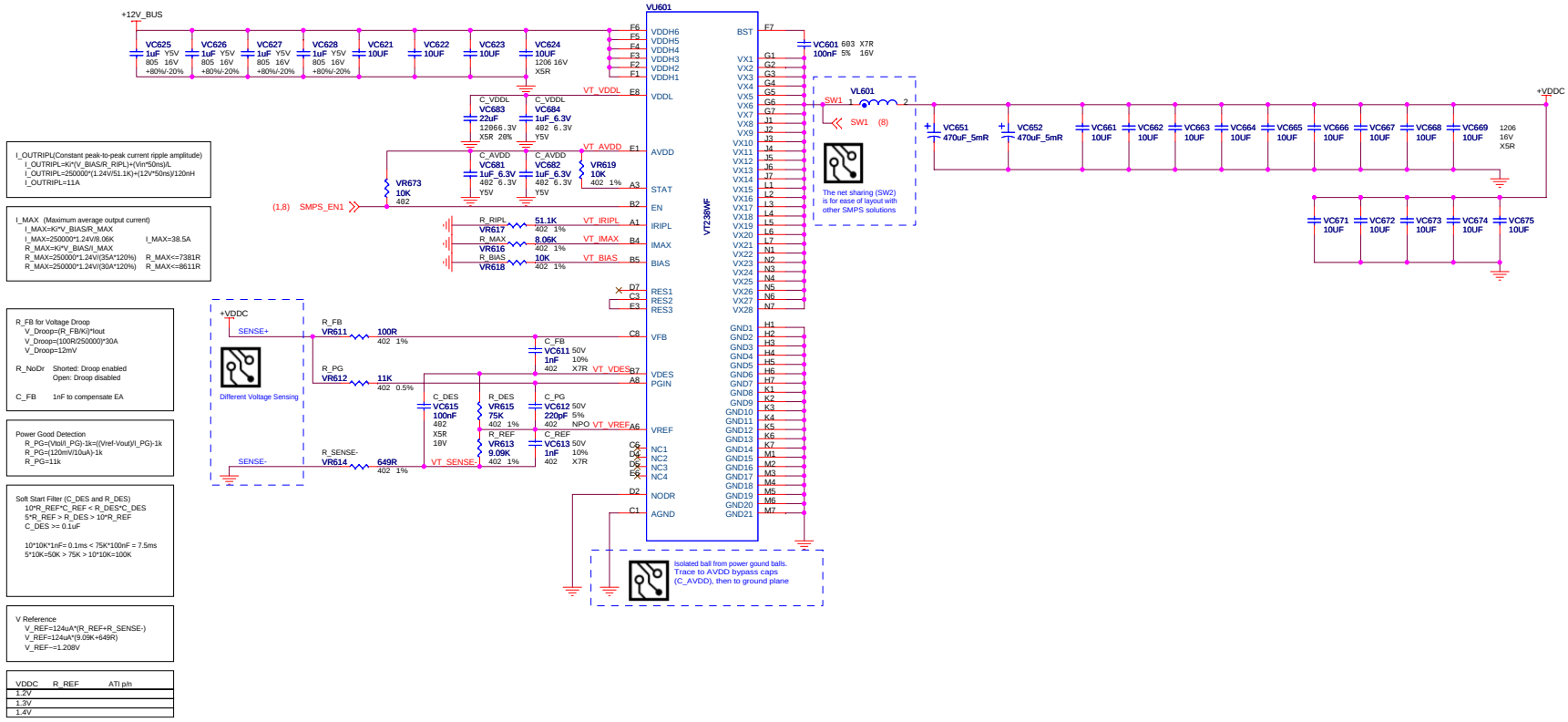

SMPS01 Volterra Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	1.2V ; +2%/-2%	0.8V ~ 1.5V
Vout ripple (DC)	50mVpp	
Iout	30Aavg, 35Adc_max	
Step load	20Amax	
Vout ripple (AC)	+/-10% or 120mVpp @ 20A step load	
Switching Freq.	1MHz	100ns on time minimum
Protections	UVLO [9.5V, 10.1V] OVLO [13.4V, 14.1V] OTP [120degCj 150degCj] OCP/SCP IMAX	

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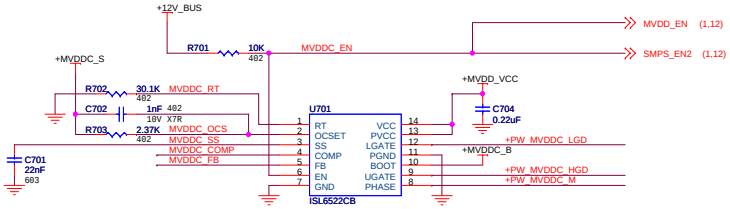
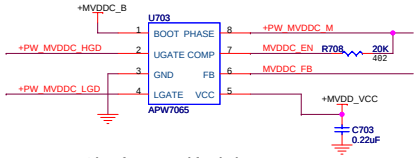


List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7074 (12V)
CAT CAT7522/CAT7523
INTERSIL ISL6522/ISL6535
RICHTEK RT9232/RT9232A/RT9232B



List of supported foodprint

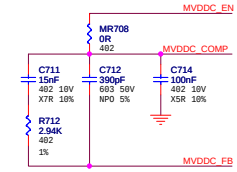
The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7120/APW7065 (12V)
CAT CAT7583 (12V)
INTERSIL ISL6545
NEXSEM NX2114/2307
RICHTEK RT9214/RT8101
OnSemi ON1582

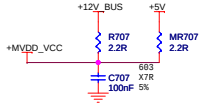
Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

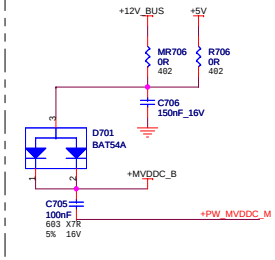
COMPENSATION CIRCUIT



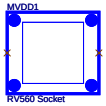
FILTERED SMPS VCC



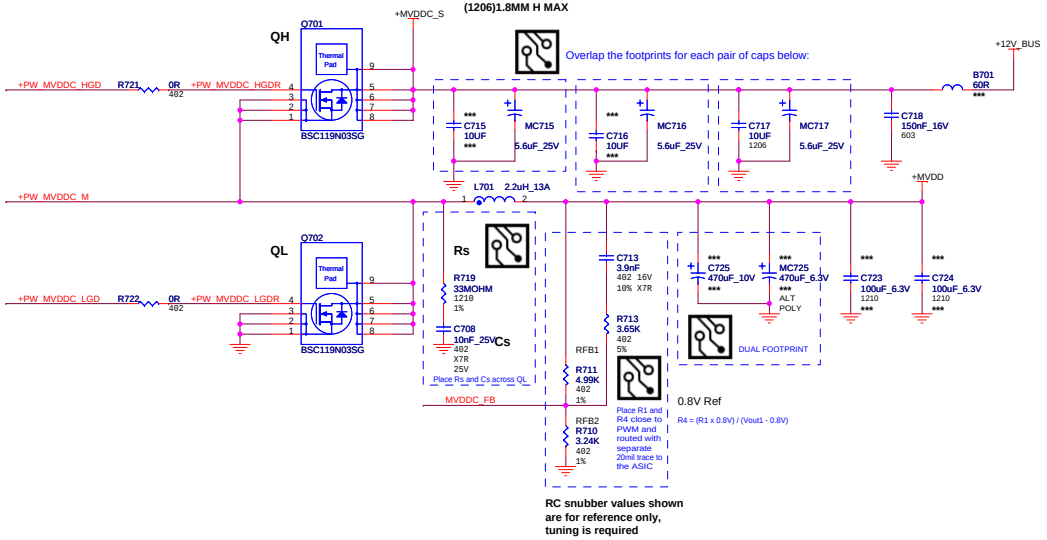
BOOT CIRCUIT



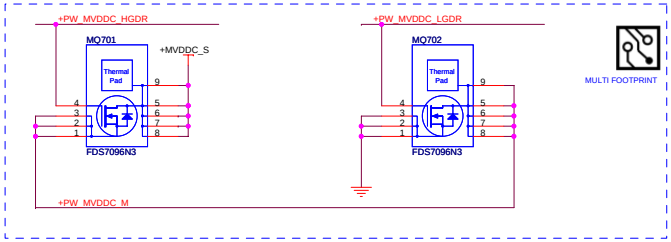
This symbol is used for 132 SMPS p/n.



CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX



RC snubber values shown are for reference only, tuning is required



SMPS02- Regulator for MVDD

Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G

SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

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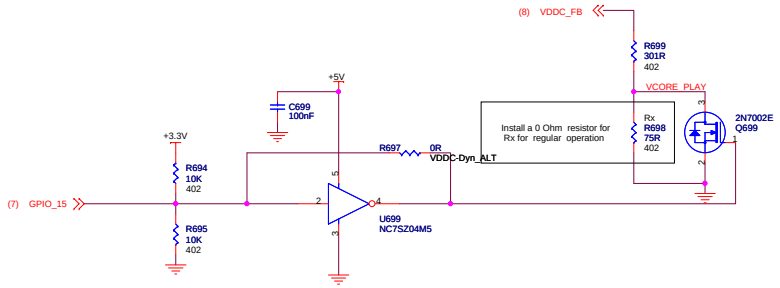
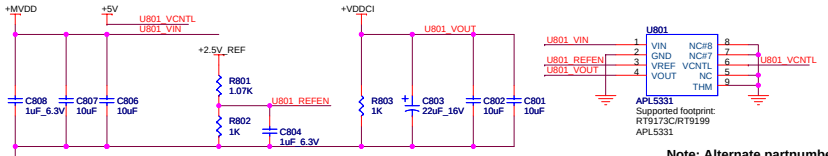
Option for Dynamic VDDC

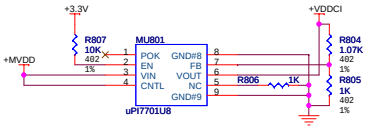


Optional Regulator for +VDDCI
Vout = 1.2V ~ 1.4V



CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

CAP CER 10UF 10%
6.3V X5R (0805)1.4MM
MAX THICK



Note: Alternate partnumbers are provided as possible choices only.
See BOM for qualified regulators/vendors. Not all combinations are tested.

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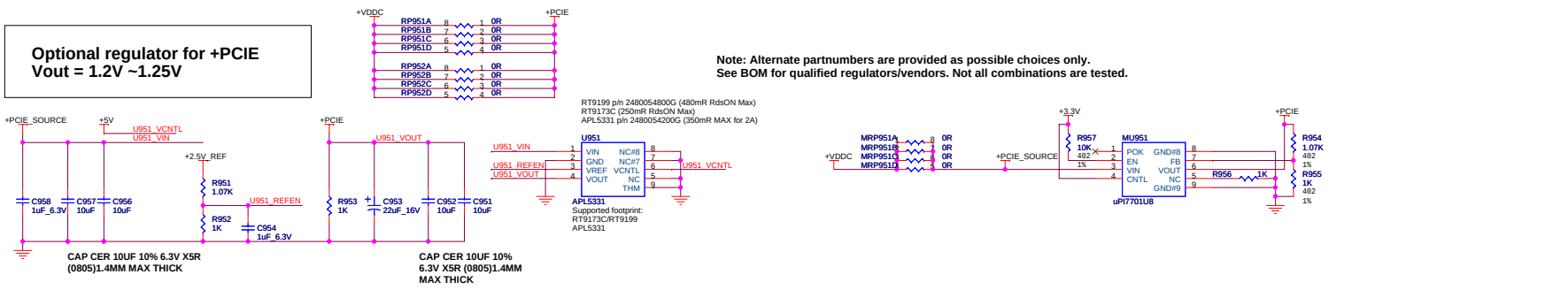
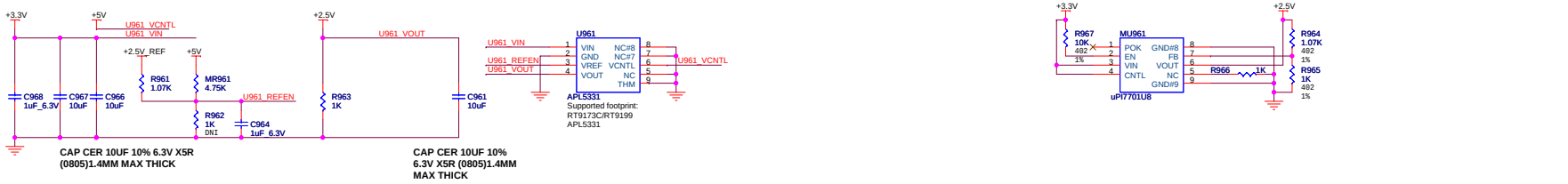
Optional regulator for +PCIE
Vout = 1.2V ~1.25V

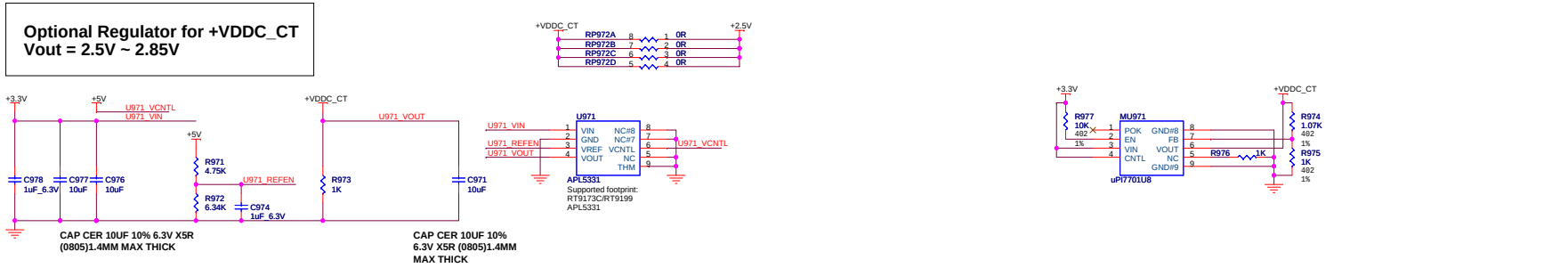
Note: Alternate partnumbers are provided as possible choices only.
See BOM for qualified regulators/vendors. Not all combinations are tested.

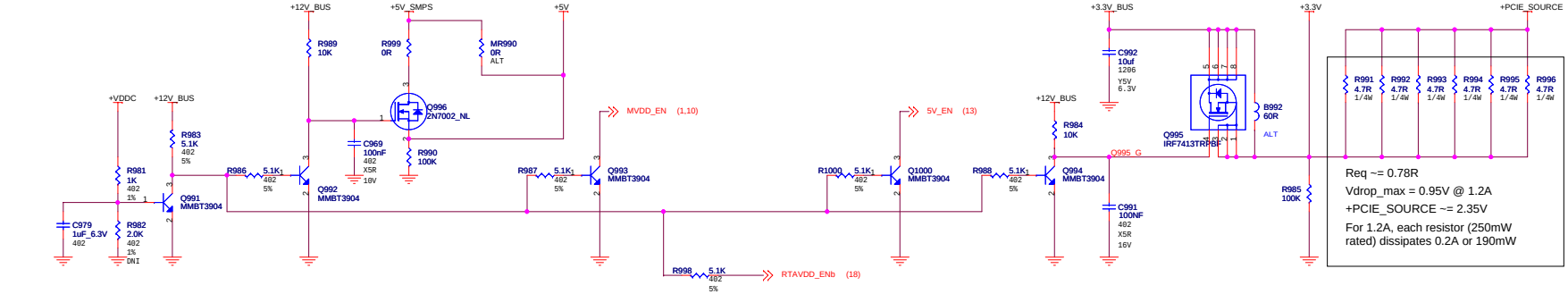


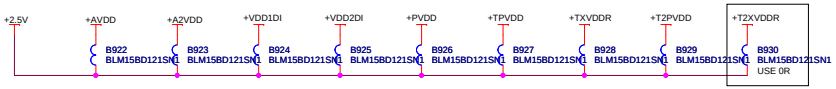
Optional regulator for +2.5V
Vout = 2.5V



Optional Regulator for +VDDC_CT
Vout = 2.5V ~ 2.85V







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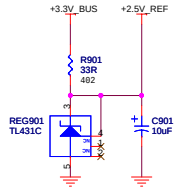
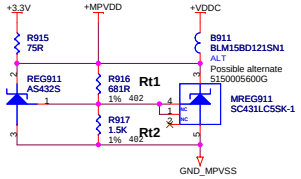
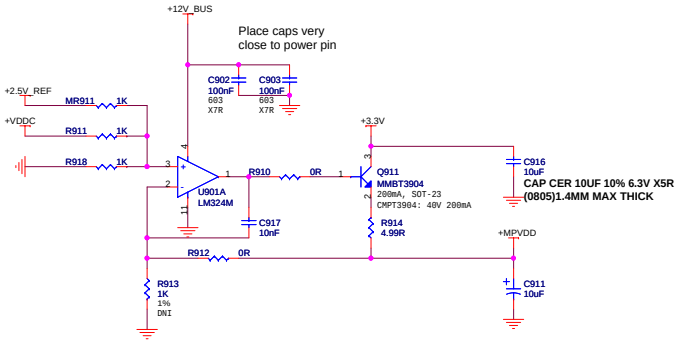
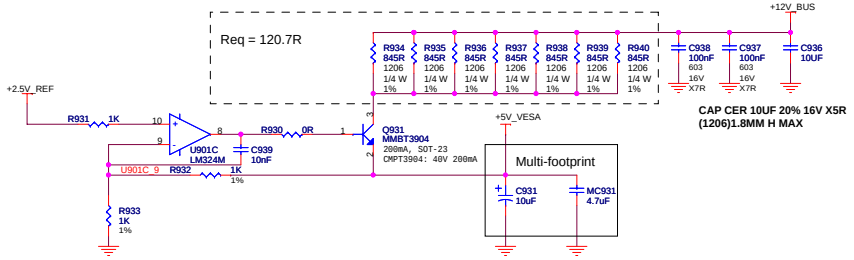


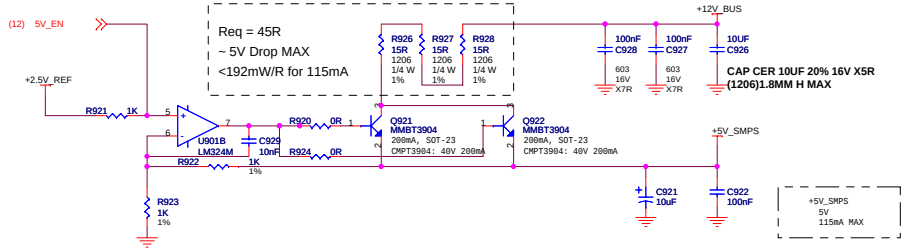
Alt regulator for +MPVDD
Vout = 1.2V (not tracking to VDDC)
Iout = 10mA MAX

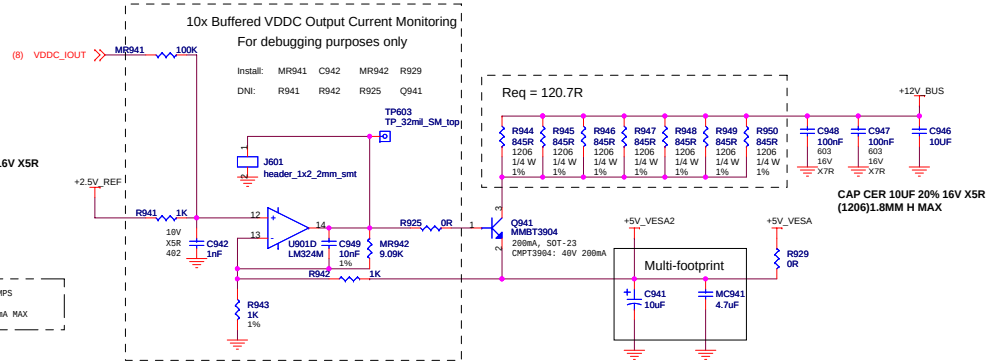


	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100









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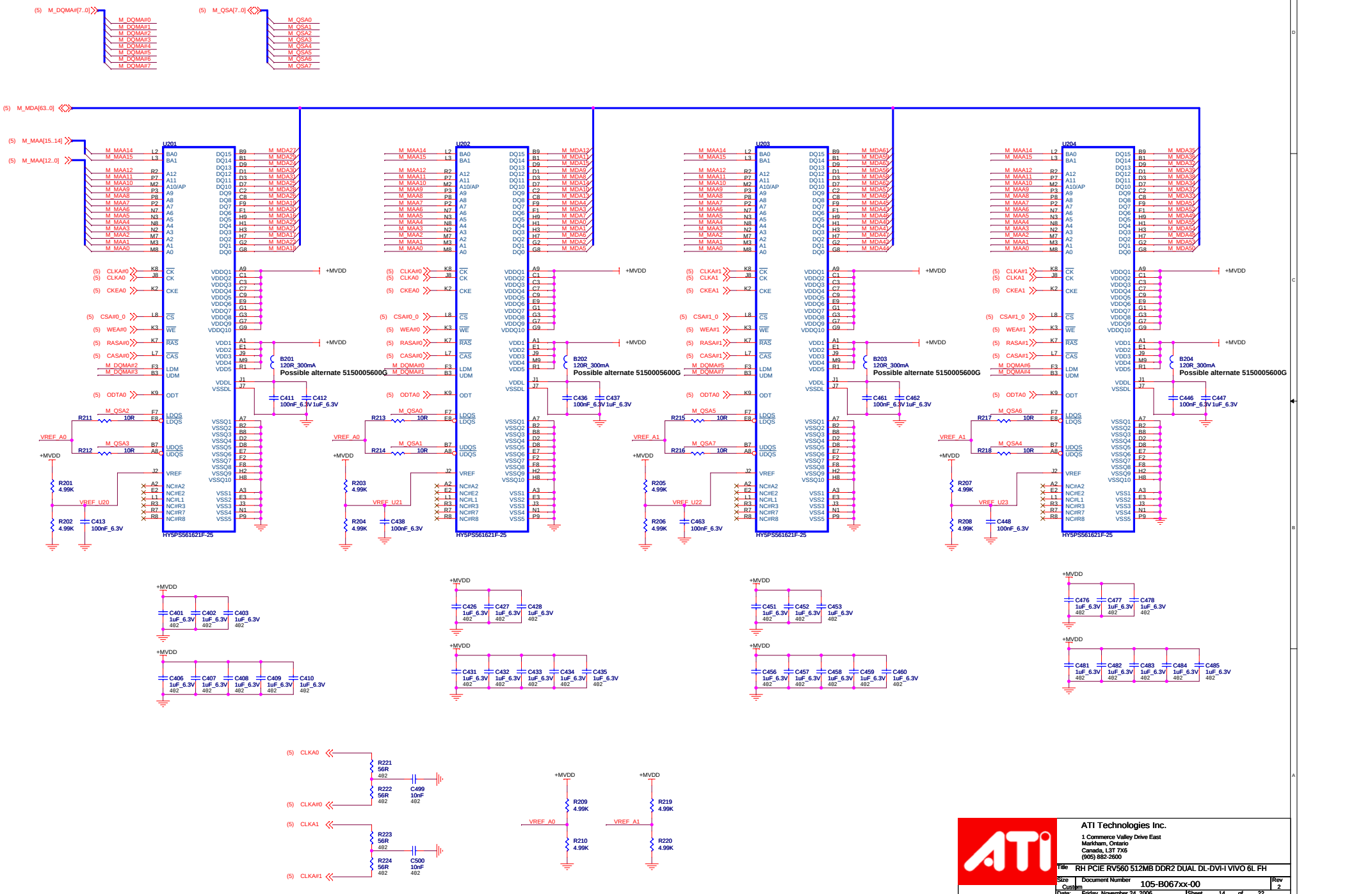
CHANNEL A: 128MB/256MB DDR2



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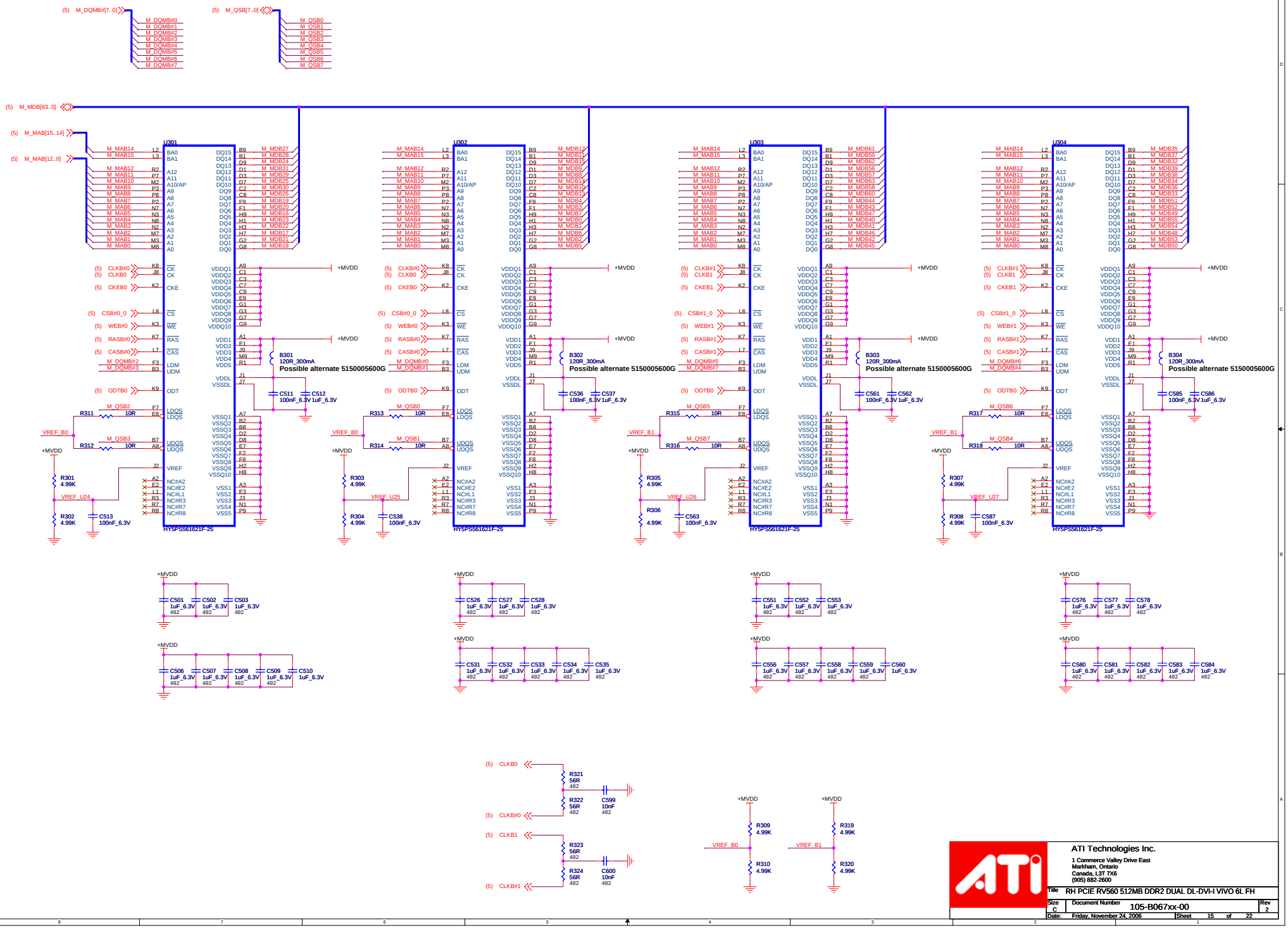
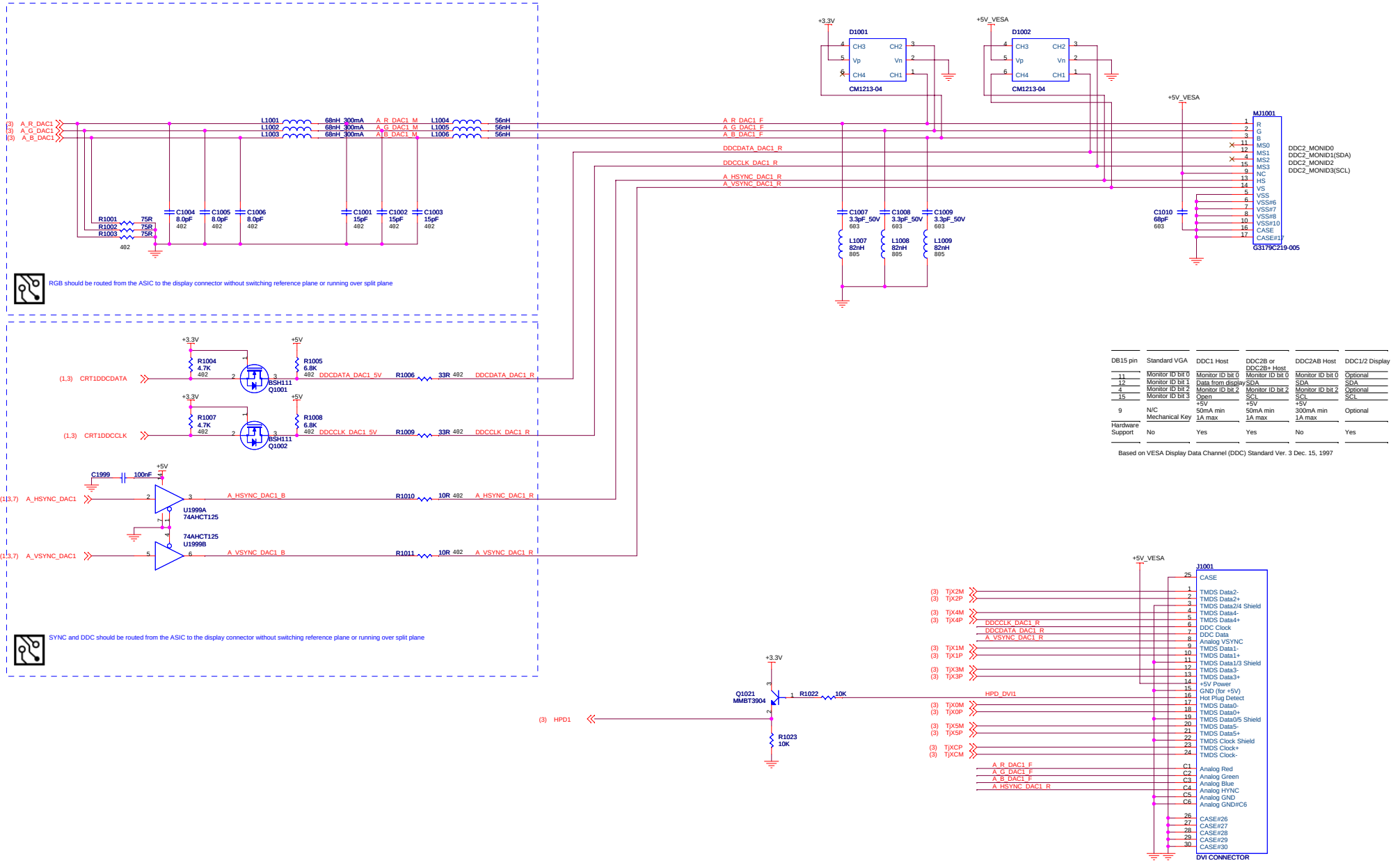
CHANNEL B: 128MB/256MB DDR2





DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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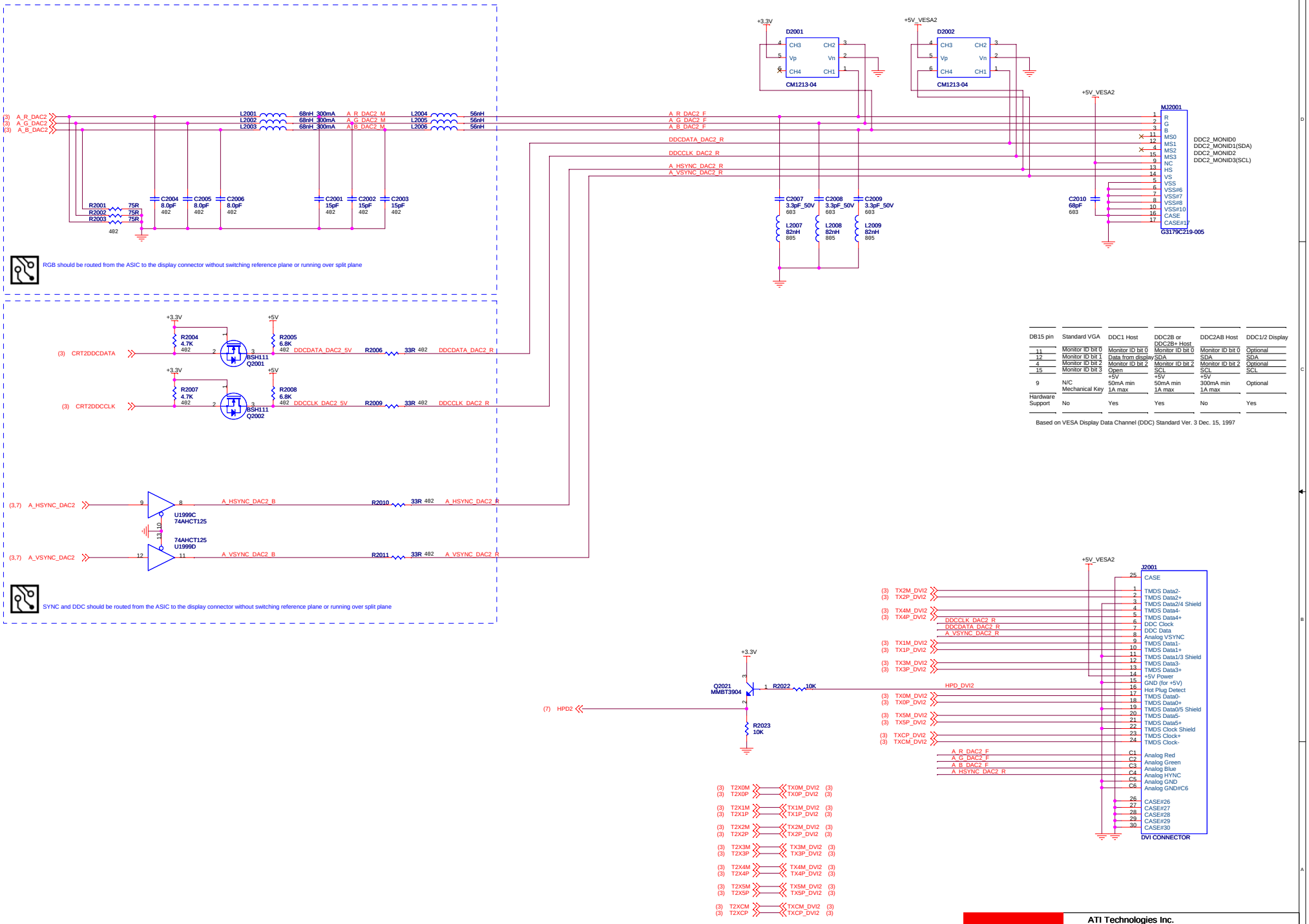

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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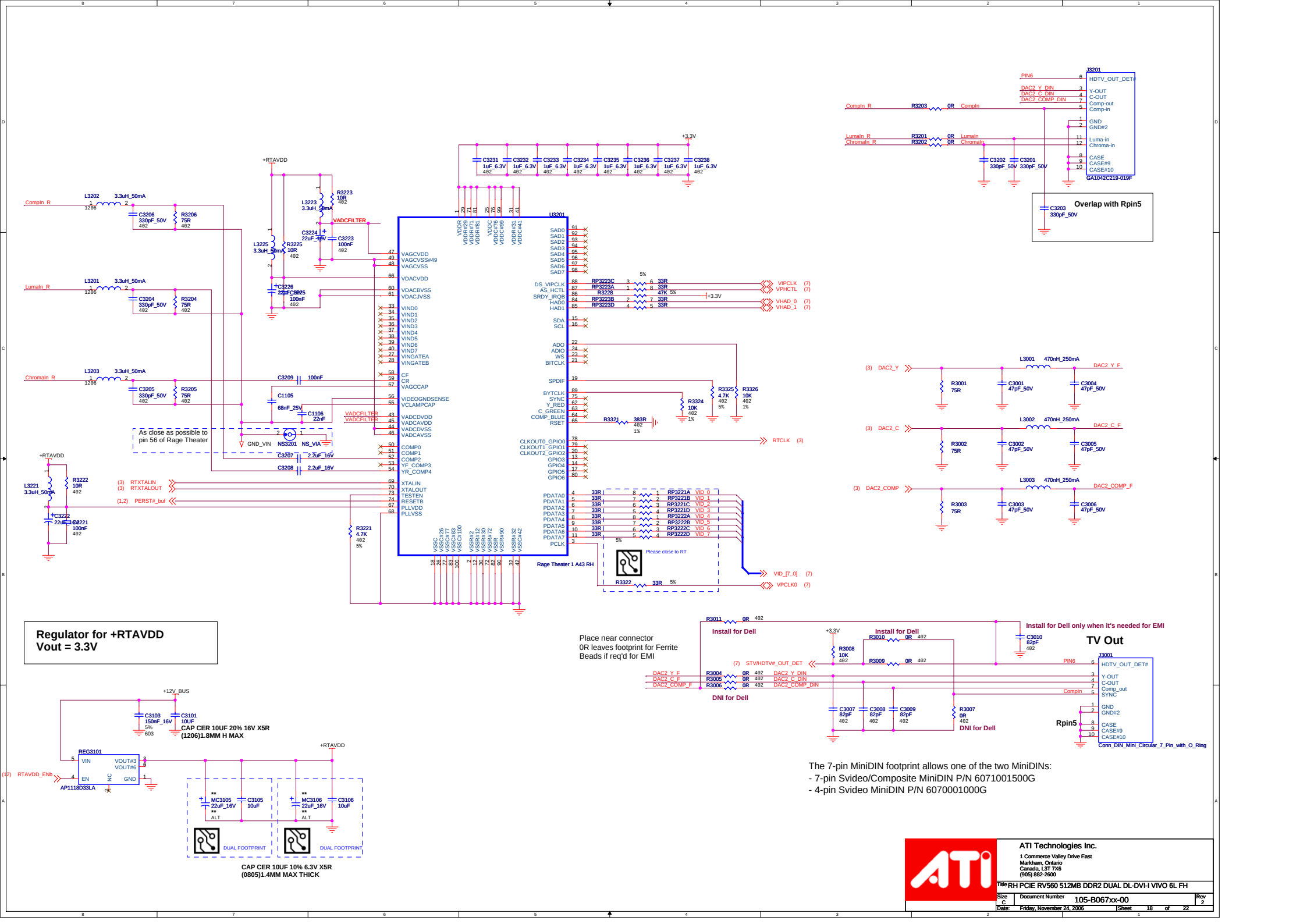
Regulator for +RTAVDD
Vout = 3.3V
Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI
TV Out
Overlap with Rpin5
Rage Theater 1 A43 RH
As close as possible to
pin 56 of Rage Theater
Please close to RT
Install for Dell
DNI for Dell
Install for Dell only when it's needed for EMI
CAP CER 10UF 20% 16V X5R
(1206)1.8MM H MAX
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK
The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G
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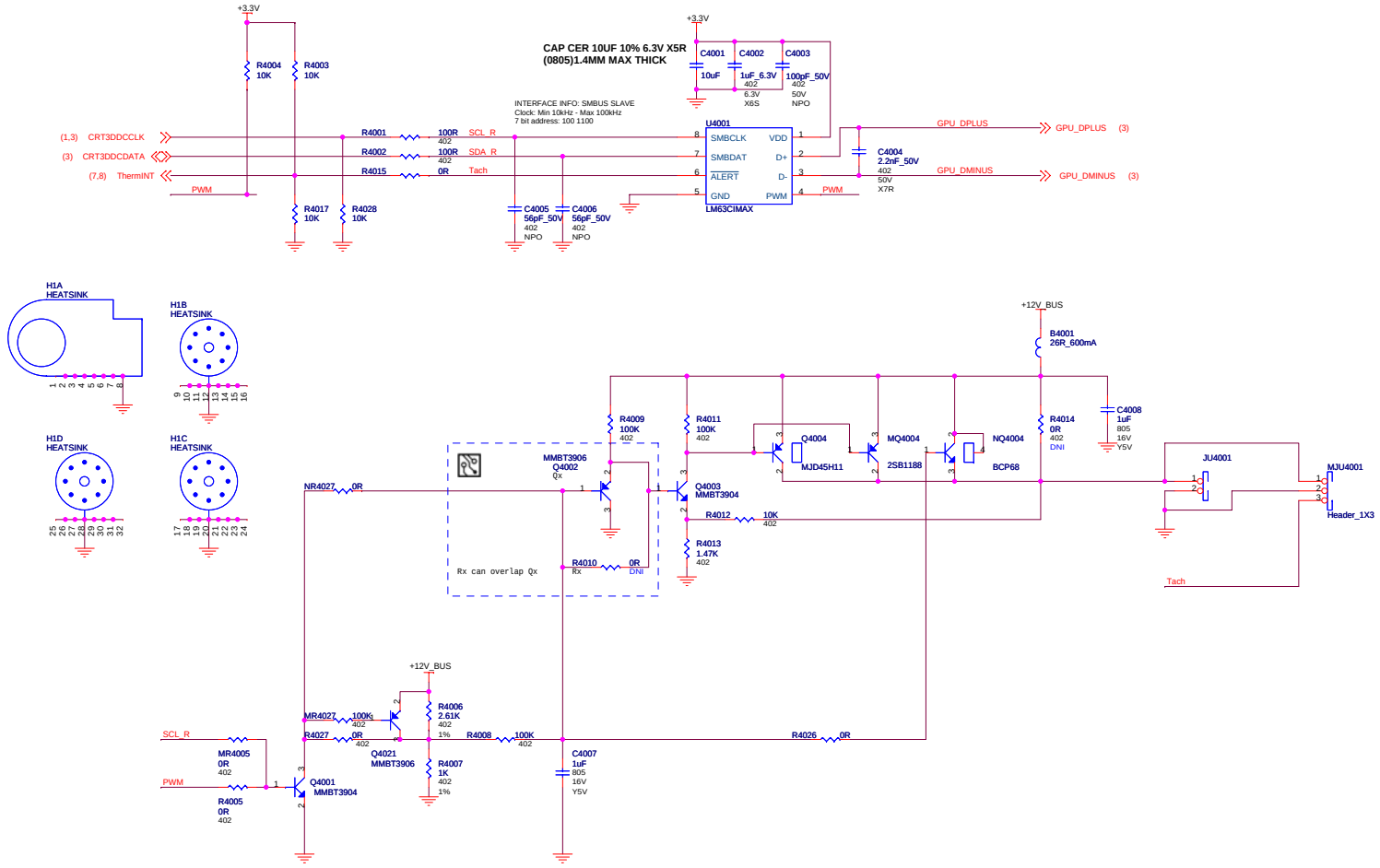

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DVI/DVI SCREWS with top tab

ASSY-SCREW1
SCREW
JACKSCREW
<3rd part field>
7020000800G

ASSY-SCREW2
SCREW
JACKSCREW
<3rd part field>
7020000800G

ASSY-SCREW5
SCREW
PAN_HEAD
7020001700G

ASSY-SCREW3
SCREW
JACKSCREW
<3rd part field>
7020000800G

ASSY-SCREW4
SCREW
JACKSCREW
<3rd part field>
7020000800G

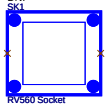
BKT1
BRACKET
8020042500G

ASSY1
ANTISTATIC
BAG
6_X_11

MT1
MT_Hole_0.136_in.

MT2
MT_Hole_0.136_in_6VIA

DNI
SK1



RV560 Socket

PCB1

109-B06731-00

<Variant Name>

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<variant_name>

Title	Schematic No.	Date:
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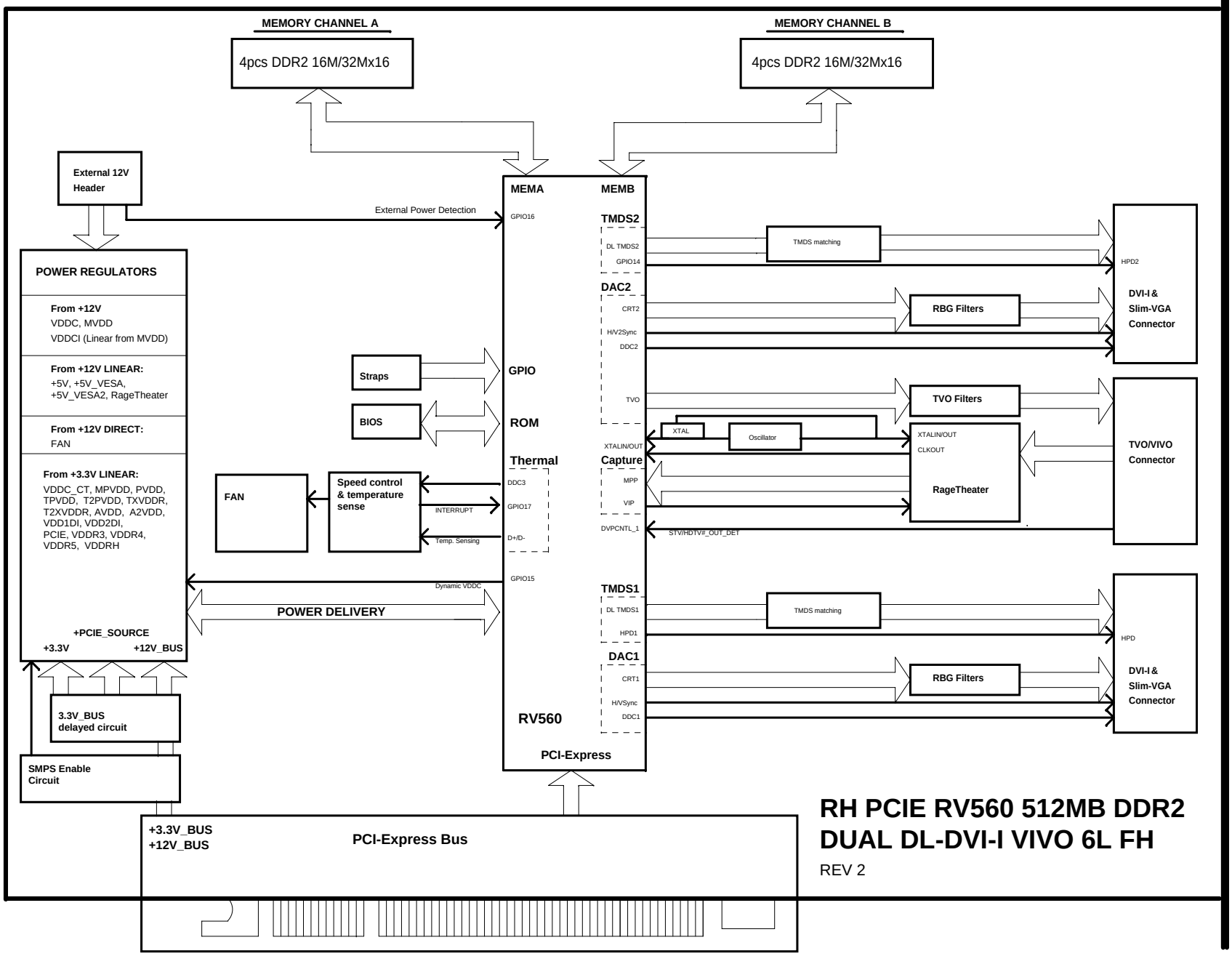
REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/07/25	Design based on 105/109-A880xx-00E Replacing GDDR3 memory config to DDR2 (pg 19) Removing +1.8V regulator - not required (pg 11) Removing linear regulator for +MVDD (not used) to facilitate PCB design
1	00B	06/08/11	Remove CrossFire support (pg 08) Renaming net label BUSEN to ENBUS
2	00	06/09/20	(pg 19) Updating H1 symbols (Layout) Addressing DFM issues (pg 08) Changing MQ601, MQ602, MQ603, MQ604, MQ611, MQ612, MQ613, MQ614 from p-tdson-8 to SO8_PowerPak (dual footprint) (pg 10) Changing Q701 and Q702 from p-tdson-8 to SO8_PowerPak (dual footprint)



RH PCIE RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH

REV 2

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