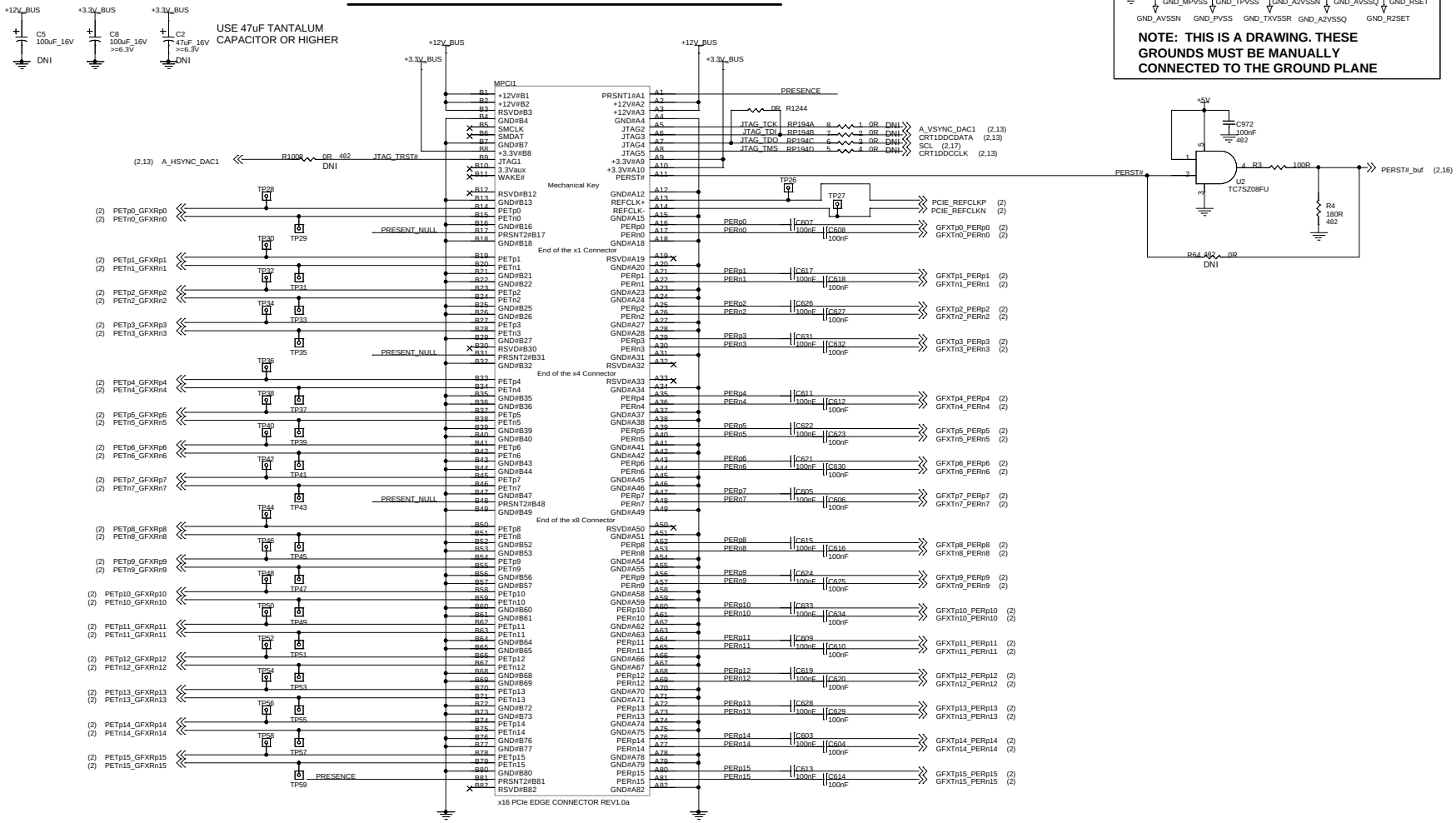
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI		
Size C	Document Number 105-A334xx-00B		Rev 1
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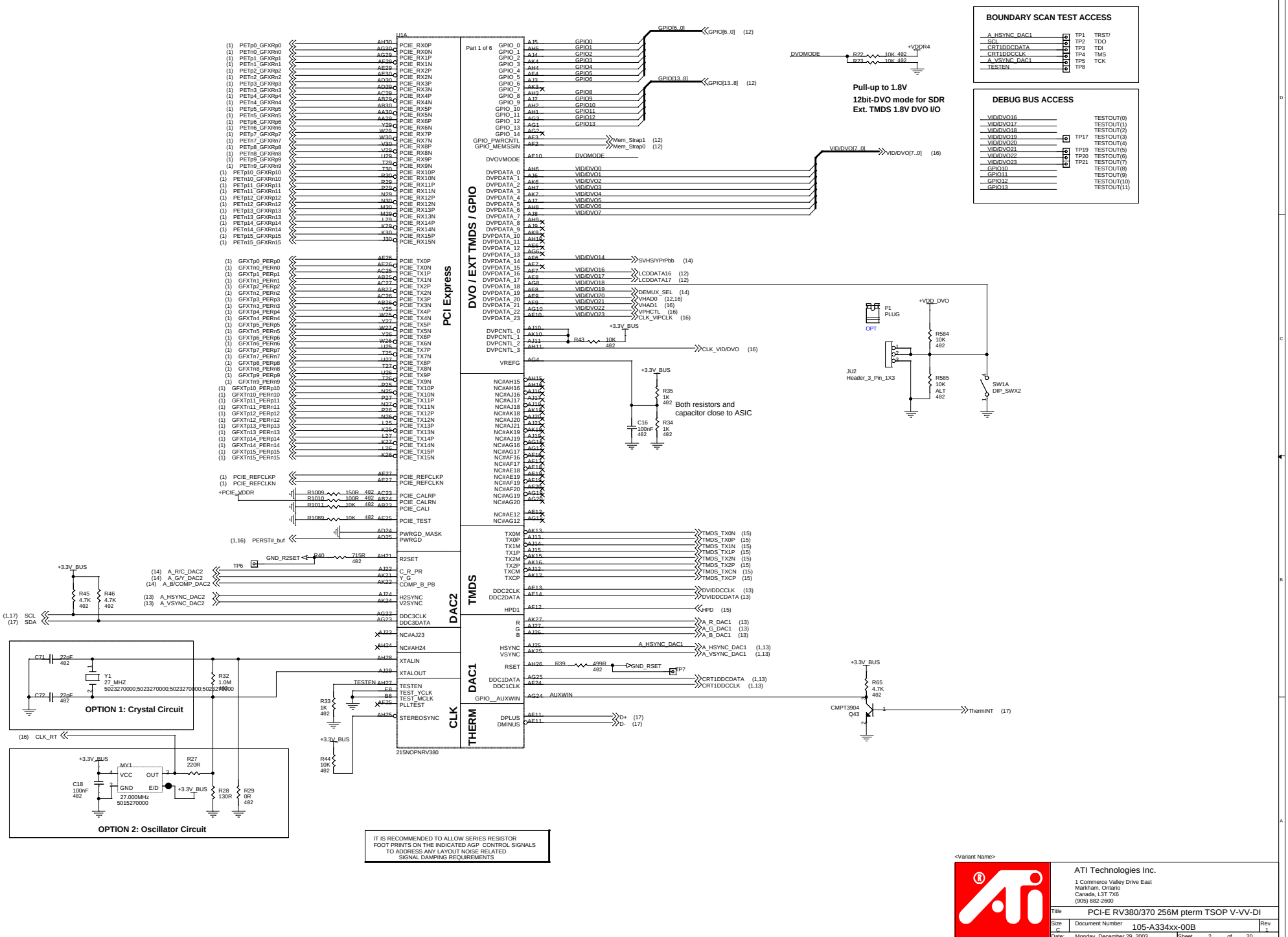
BOUNDARY SCAN TEST ACCESS
A_HSYNC_DAC1
SCL
CRT1DDCDATA
CRT1DDCCLK
A_VSYNC_DAC1
TESTEN
TP1 TRST/
TP2 TDO
TP3 TDI
TP4 TMS
TP5 TCK
TP8
DEBUG BUS ACCESS
VID/DVO16
VID/DVO17
VID/DVO18
VID/DVO19
VID/DVO20
VID/DVO21
VID/DVO22
VID/DVO23
GPIO10
GPIO11
GPIO12
GPIO13
TP17
TP19
TP20
TP21
TESTOUT(0)
TESTOUT(1)
TESTOUT(2)
TESTOUT(3)
TESTOUT(4)
TESTOUT(5)
TESTOUT(6)
TESTOUT(7)
TESTOUT(8)
TESTOUT(9)
TESTOUT(10)
TESTOUT(11)
U1A
Part 1 of 6
PCI Express
DVO / EXT TMDS / GPIO
DAC2
TMDS
DAC1
CLK
THERM
215NOPNRV380
Pull-up to 1.8V
12bit-DVO mode for SDR
Ext. TMDS 1.8V DVO I/O
Both resistors and
capacitor close to ASIC
OPTION 1: Crystal Circuit
OPTION 2: Oscillator Circuit
IT IS RECOMMENDED TO ALLOW SERIES RESISTOR
FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS
TO ADDRESS ANY LAYOUT NOISE RELATED
SIGNAL DAMPING REQUIREMENTS
<Variant Name>
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Title PCI-E RV380/370 256M pterm TSOP V-VV-DI
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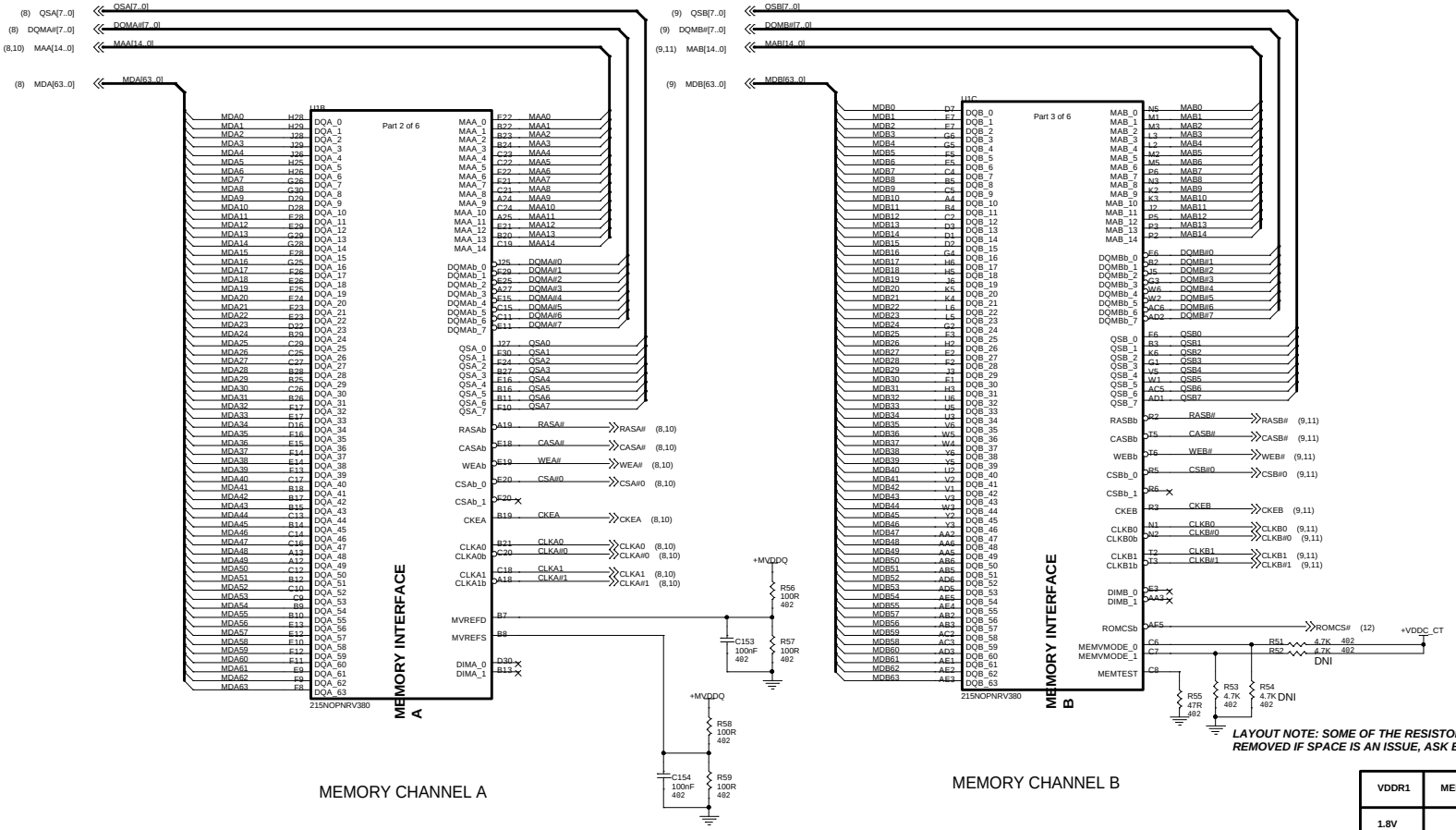

MEMORY CHANNEL A

MEMORY CHANNEL B

PLACE C351/152 VERY CLOSE TO ASIC

R56/57/58/59 CLOSE TO ASIC AS WELL

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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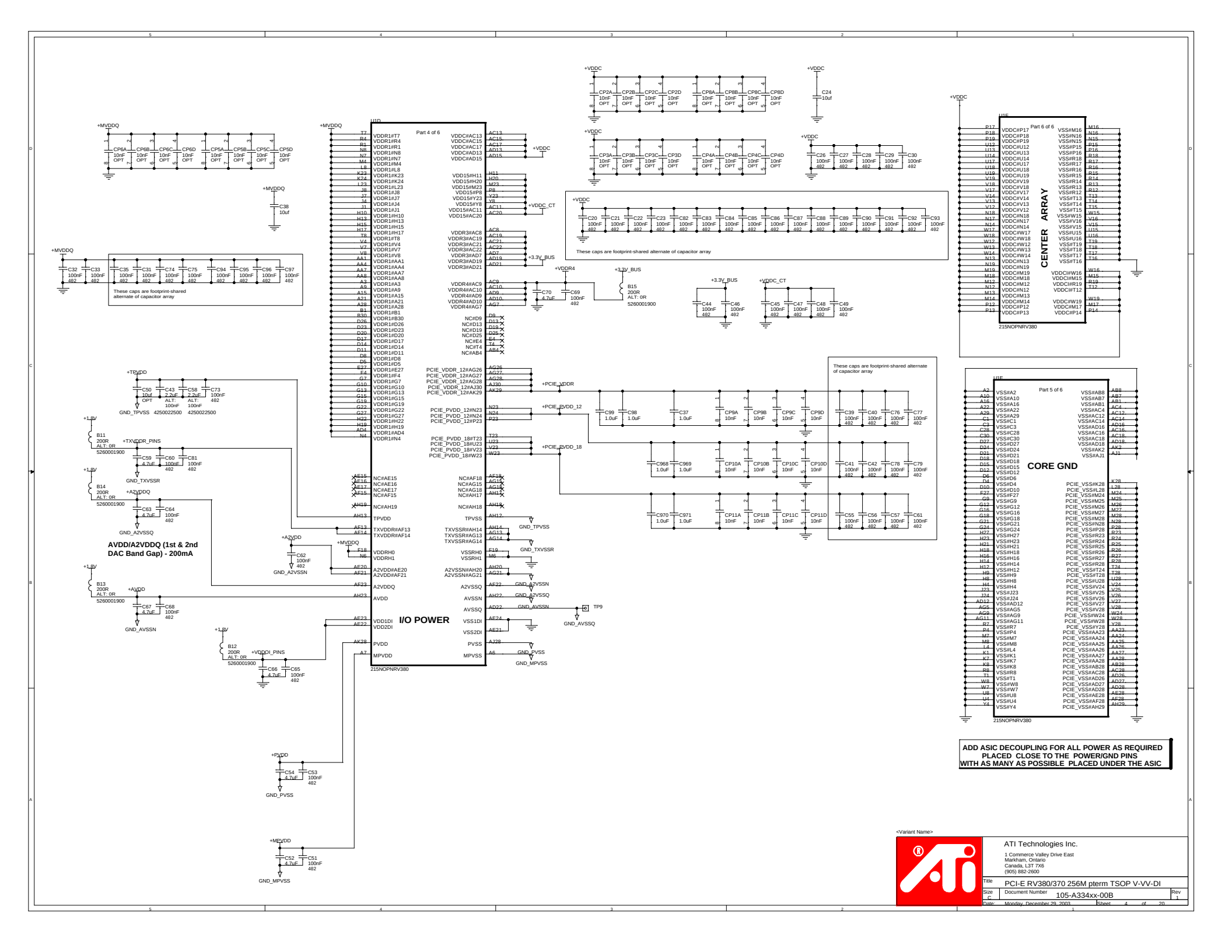
U1D
Part 4 of 6
215NOPNRV380
I/O POWER
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
These caps are footprint-shared alternate of capacitor array
These caps are footprint-shared alternate of capacitor array
U1E
Part 6 of 6
CENTER ARRAY
215NOPNRV380
U1E
Part 5 of 6
CORE GND
215NOPNRV380
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
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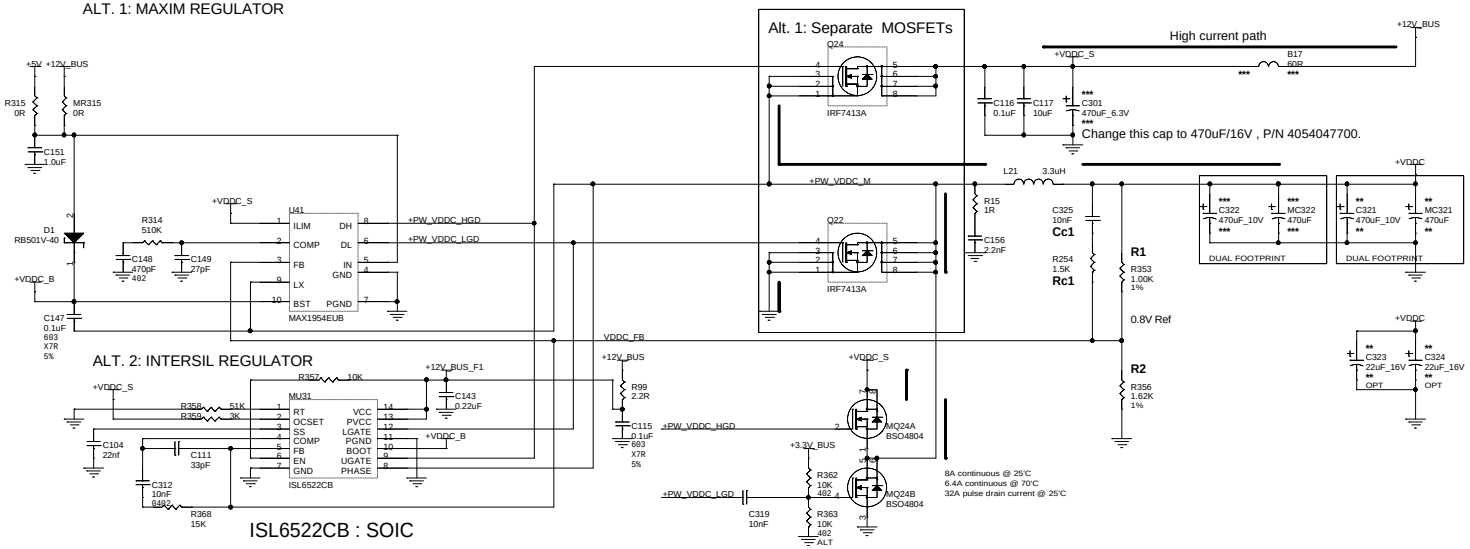
Regulator for VDDC (ASIC Core)

Vout = 1.2V ~ 1.3V

ALT. 1: MAXIM REGULATOR



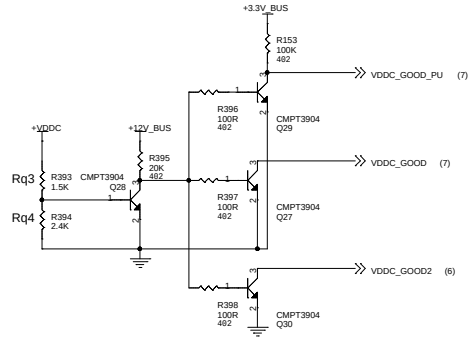
***	Indicate number of power via required for the connection

Part	NOTES
MAX1954	Do not install Cc1, Rc1
ISL6522	Install Cc1, Rc1

Part	Vout	R1	R2
MAX1954 ISL6522 0.8V Ref	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240110100
	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100

Circuit to hold PCI-E voltage low and wait for +VDDC for proper power sequence

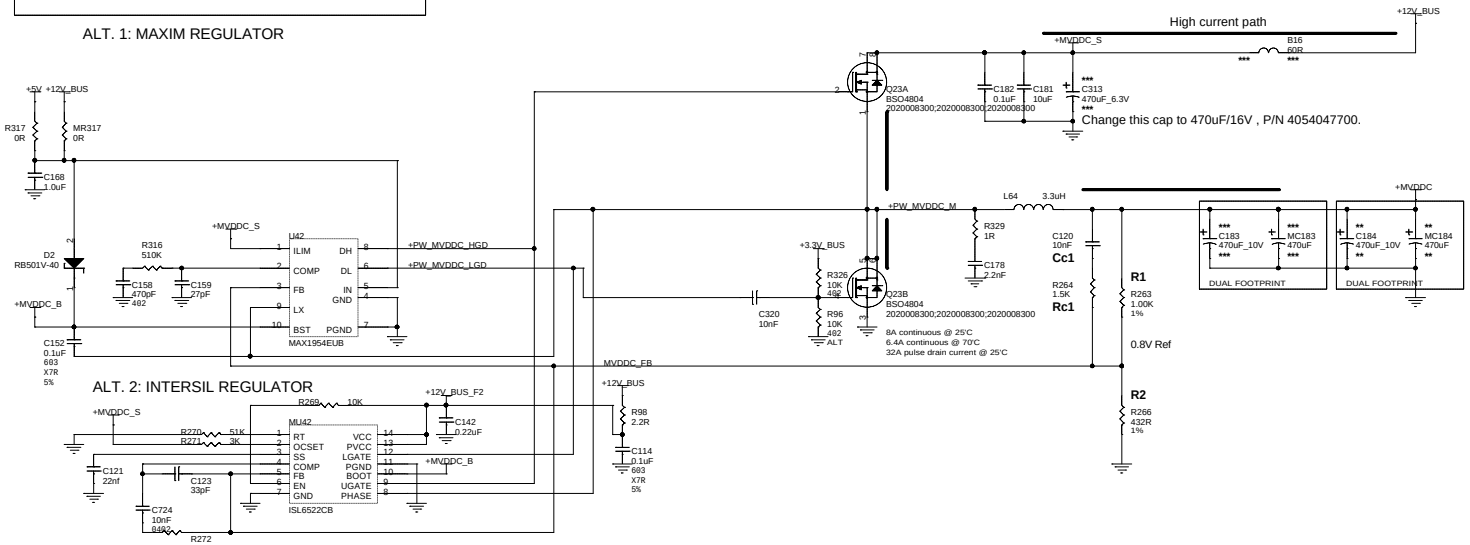
+VDDC	Rq3	Rq4
+1.3V	1.5K	2.4K



Regulator for MVDDC (Memory Core)

Vout = 2.5V ~ 3.3V

ALT. 1: MAXIM REGULATOR



<Variant Name>

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Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI		
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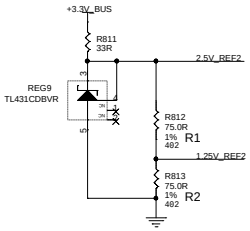
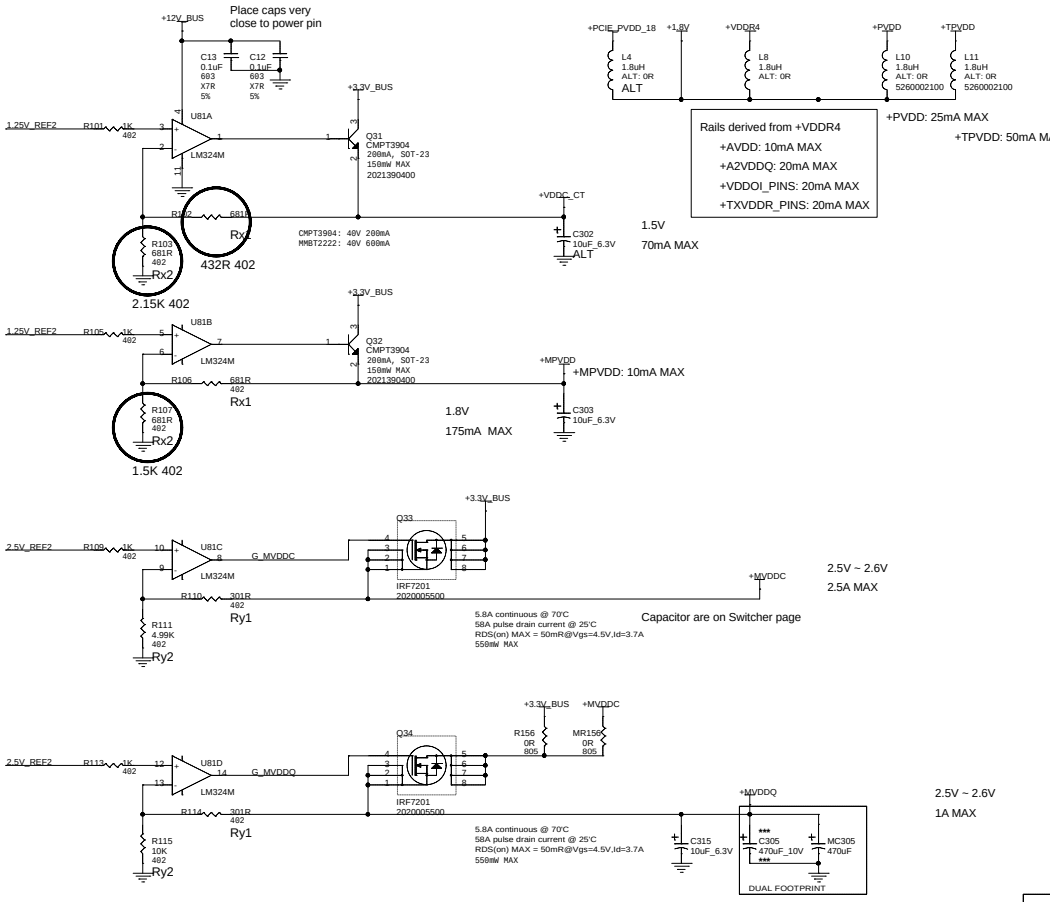


Voltage Req.	R1	R2
0.8V	150R P/N 3240150000	71.5R P/N 3240075R500
1.25V	75R P/N 3240075000 603 P/N 316075R000 402	75R P/N 3240075000 603 P/N 316075R000 402
1.5V	49.9R P/N 3240049900	75R P/N 3240075000 603 P/N 316075R000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

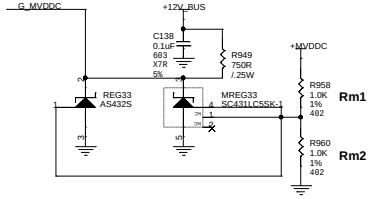
Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240015200

Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.5V	0R P/N 3230000000 603 P/N 3150000000 402	DNI



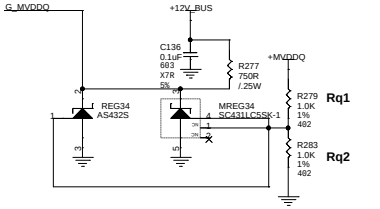
Alt. regulator for +MVDDC
Vout = 2.5V ~ 2.6V
Iout = 500mA MAX

Voltage Req.	Rm1	Rm2
3.34V [-0.04V/+0.04V]	4.32K	2.55K
3.45V [-0.04V/+0.04V]	4.32K	2.43K
2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100



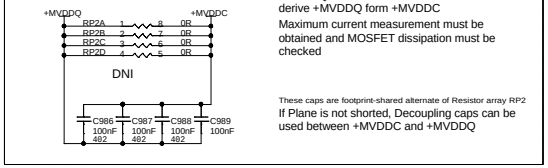
Alt regulator for +MVDDQ
Vout = 2.5V ~ 2.6V
Iout = 200mA MAX

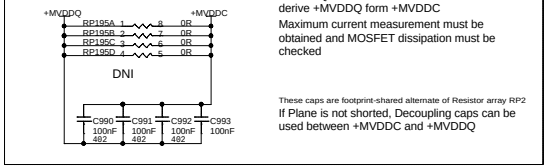
Voltage Req.	Rq1	Rq2
1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
2.5V	1K 3240100100	1K 3240100100
2.6V	4.75K 3240475100	4.32K 3240432100



Regulator for +VTT (Termination)
Vout = 1.25V ~ 1.3V with +2.5V +MVDDQ
Iout = 1000mA MAX

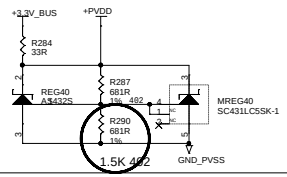
+MVDDQ = +2.5V	Rt1	Rt2
1.25V	1K 3240100100	1K 3240100100
1.3V	1.0K 3240100100 603 3160100100 402	1.02K 3240102100



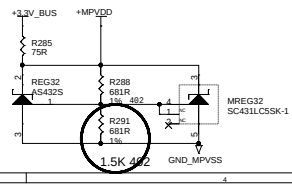


	Rt1	Rt2
1.52V +0.01V/-0.01V	432R 3240432000	2.15K
1.61V +0.01V/-0.01V	432R 3240432000	1.5K 3230015200
1.69V +0.01V/-0.01V	432R 3240432000	1.21K 3240121100
1.718V +0.01V/-0.01V	562R 3240562000	1.5K 3230015200
1.8175V +0.01V/-0.01V	681R 3240681000	1.5K 3230015200

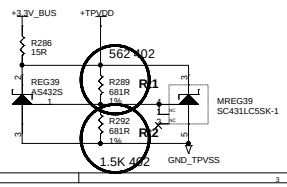
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



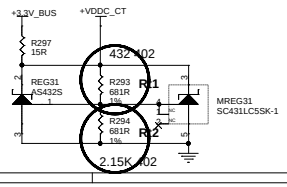
Alt regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX

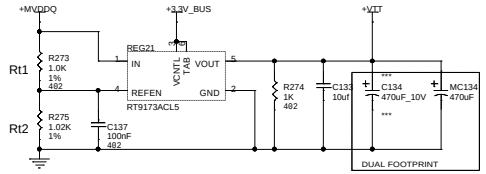


Alt. regulator for +TPVDD
Vout = 1.6V ~ 1.8V
Iout = 50mA MAX



Alt regulator for +VDDC_CT
Vout = 1.5V
Iout = 70mA MAX





<Variant Name>

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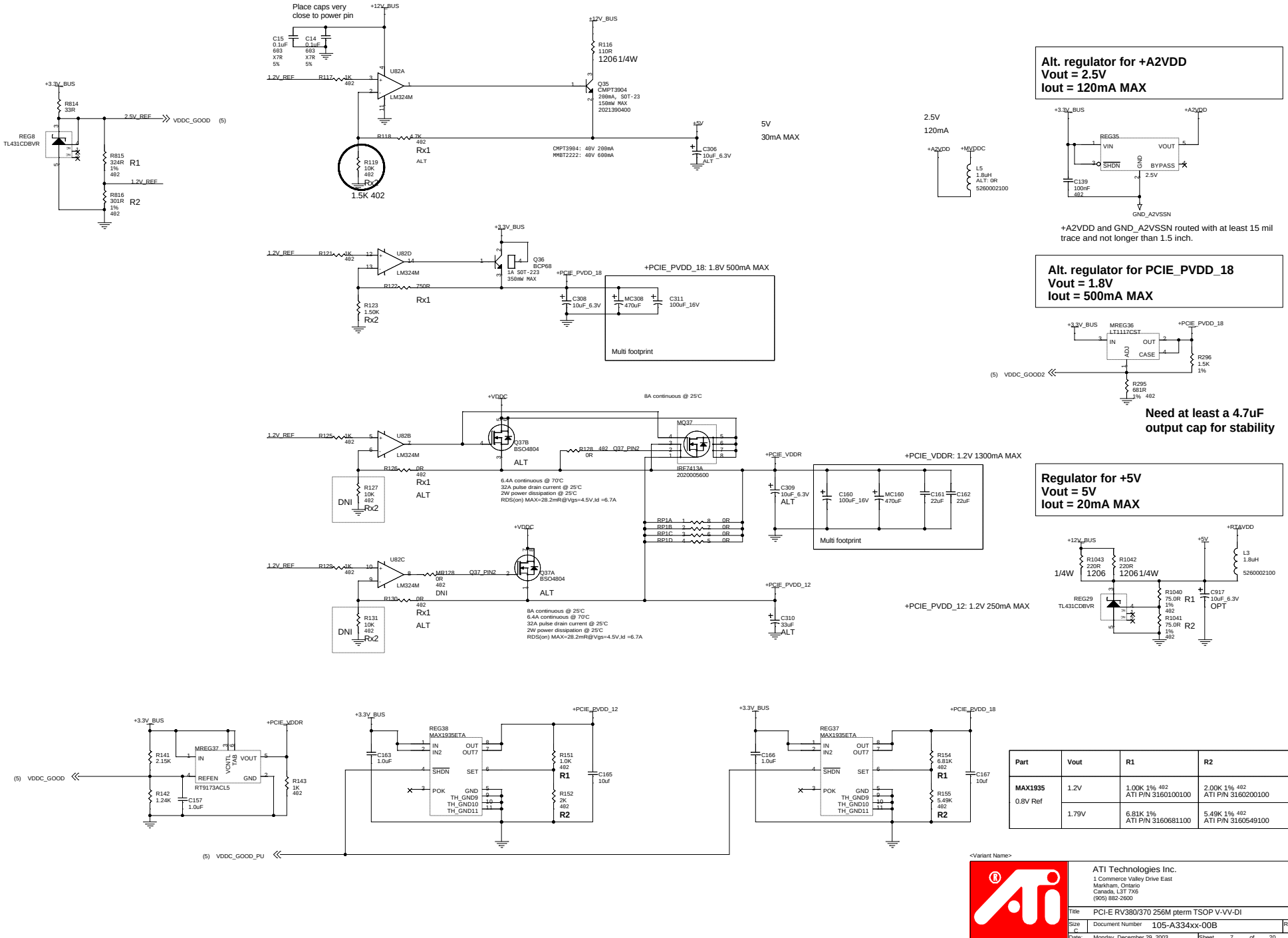

Part	Vout	R1	R2
MAX1935 0.8V Ref	1.2V	1.00K 1% 402 ATI P/N 3160100100	2.00K 1% 402 ATI P/N 3160200100
	1.79V	6.81K 1% ATI P/N 3160681100	5.49K 1% 402 ATI P/N 3160549100

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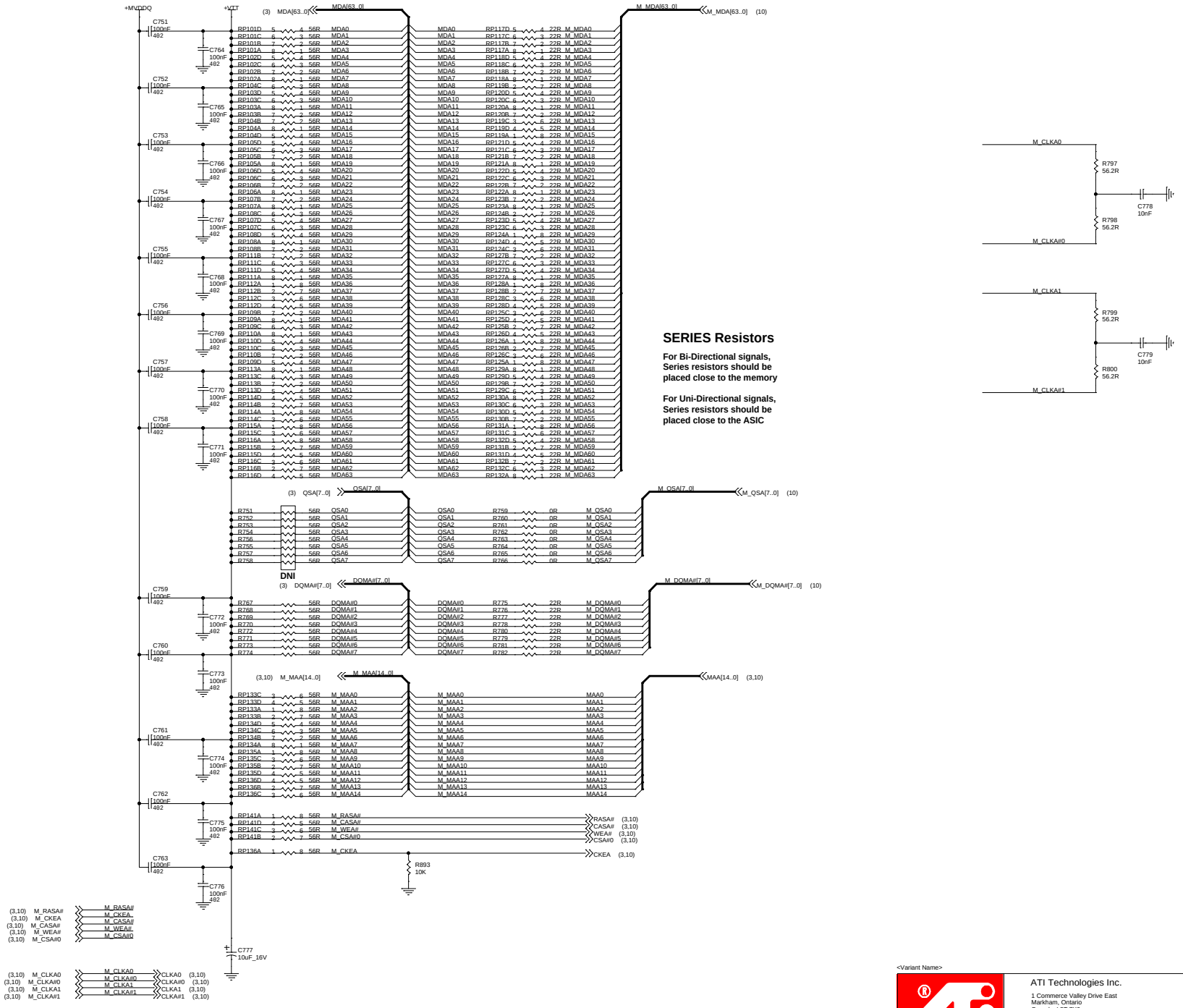

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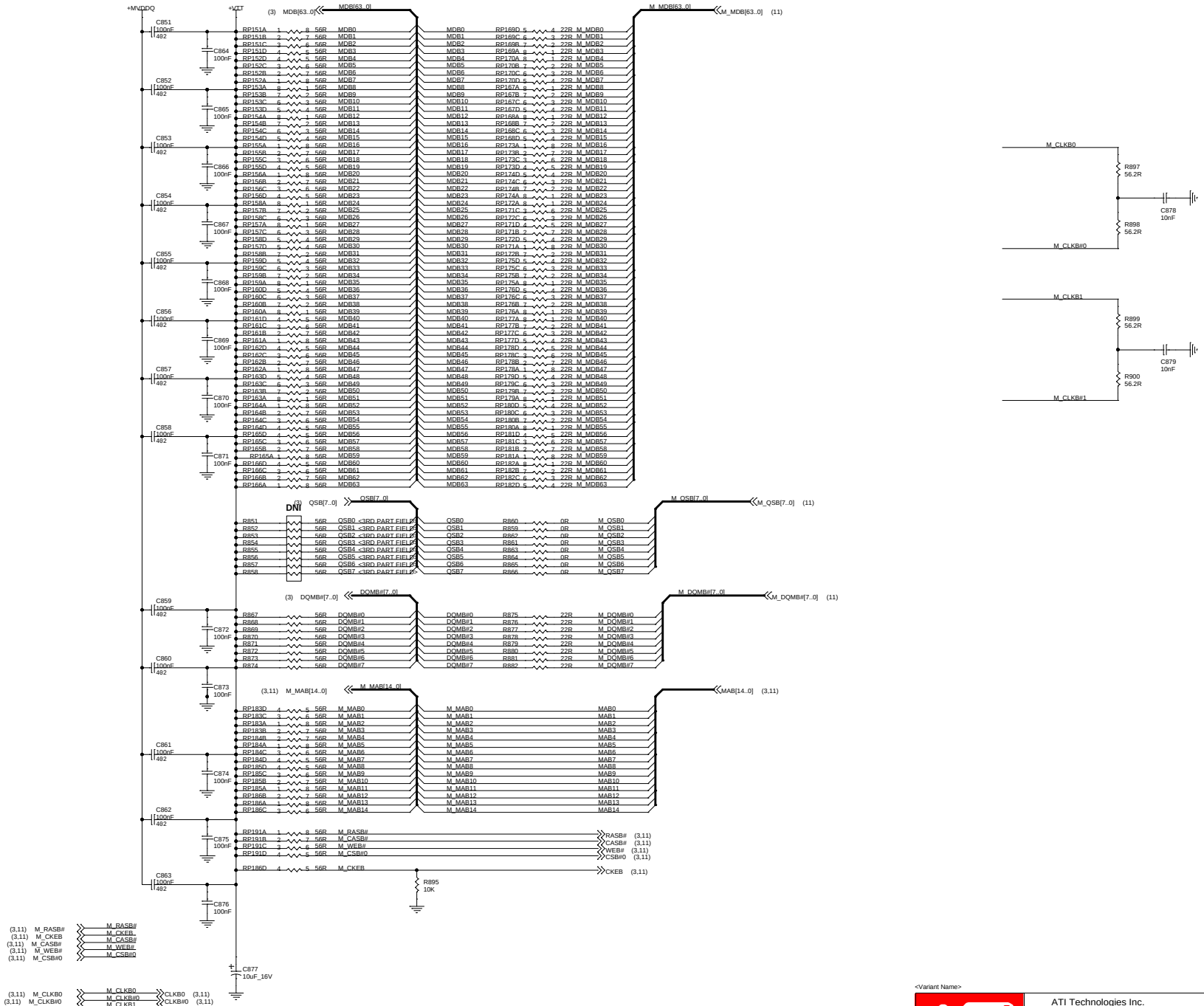

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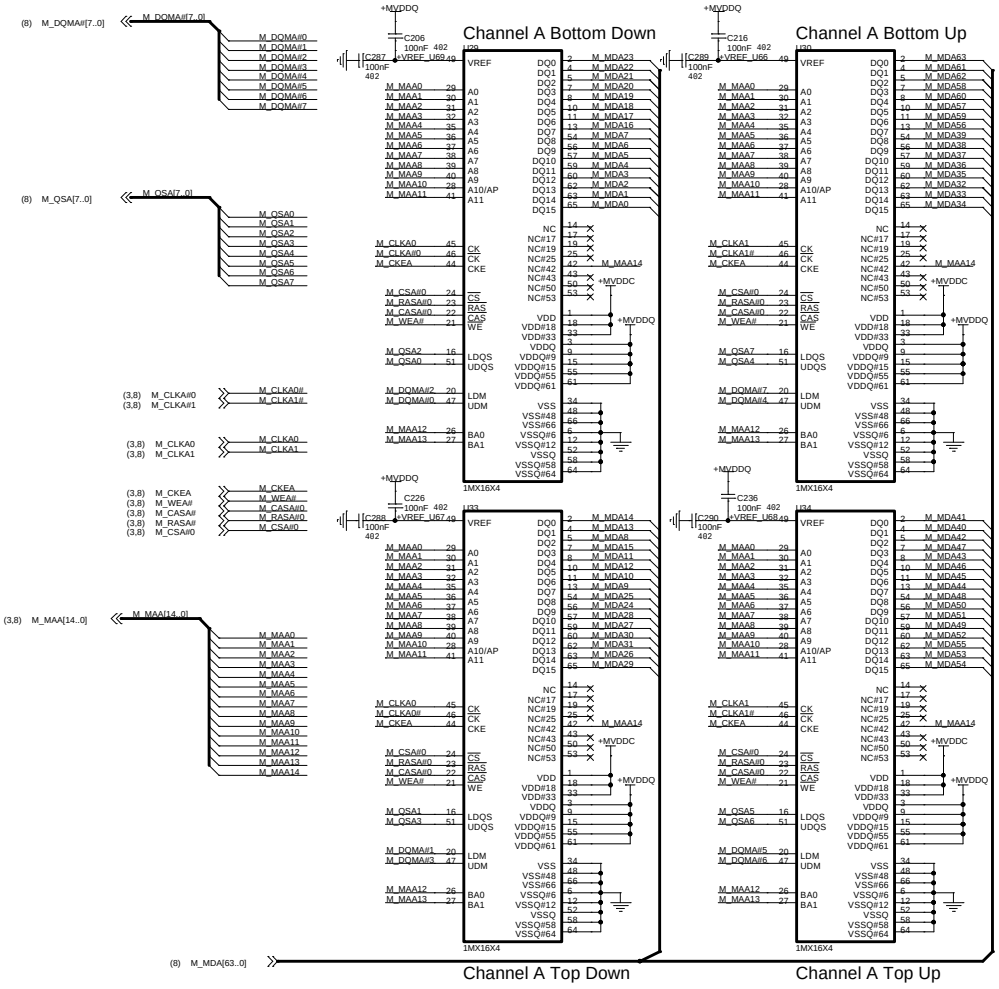
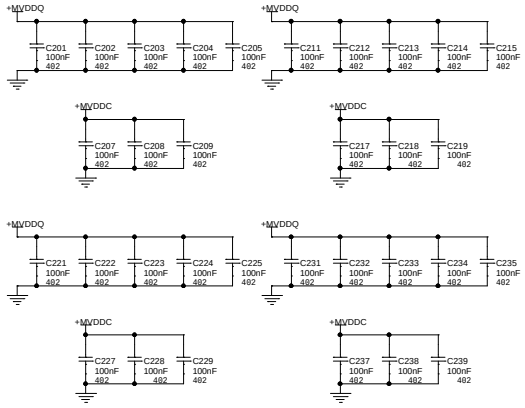
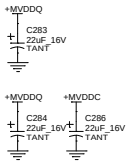
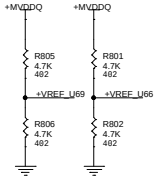
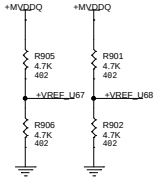


Put 1 1uF cap per power pin of memory









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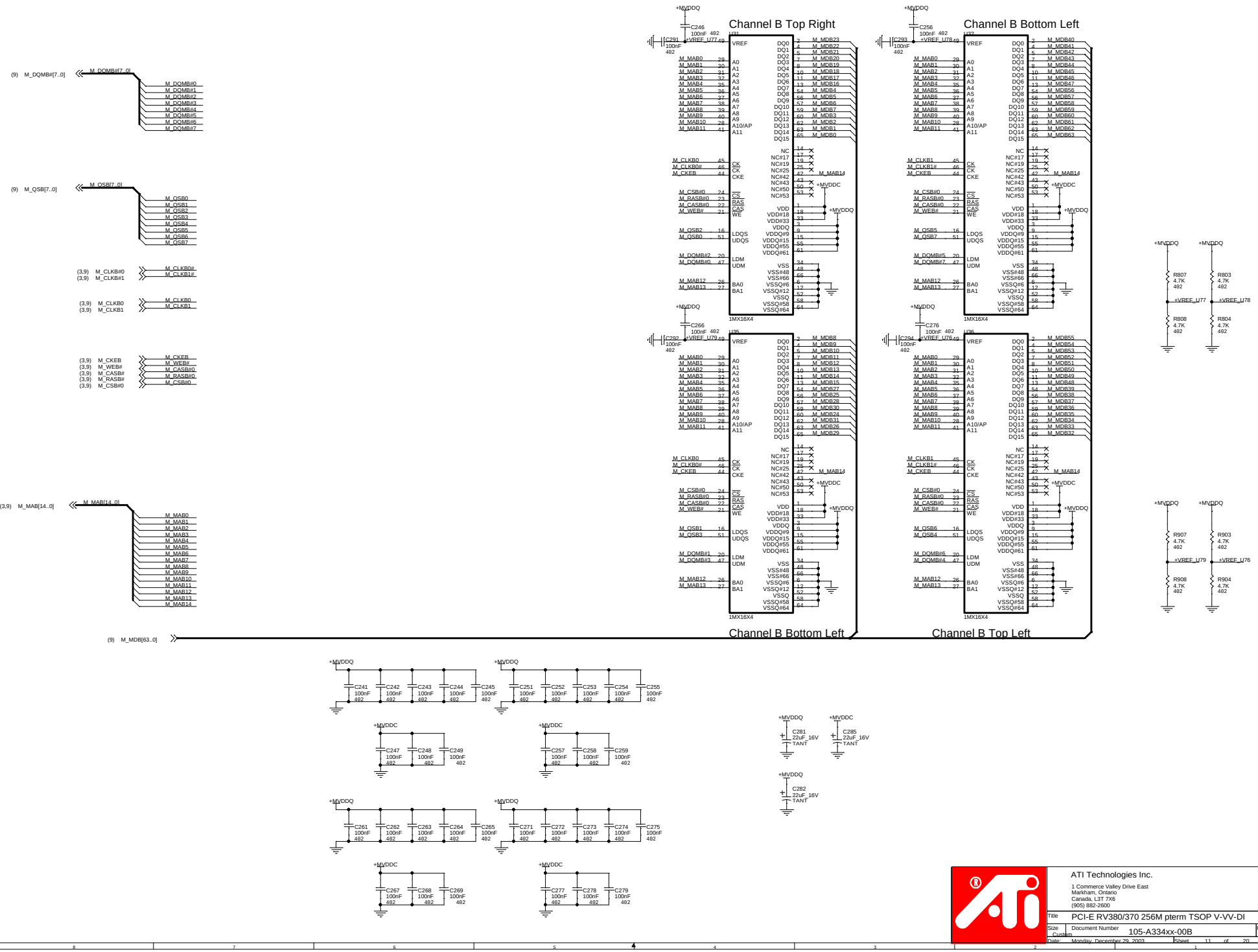

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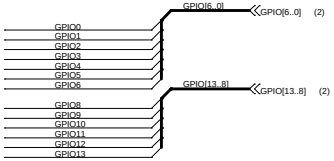
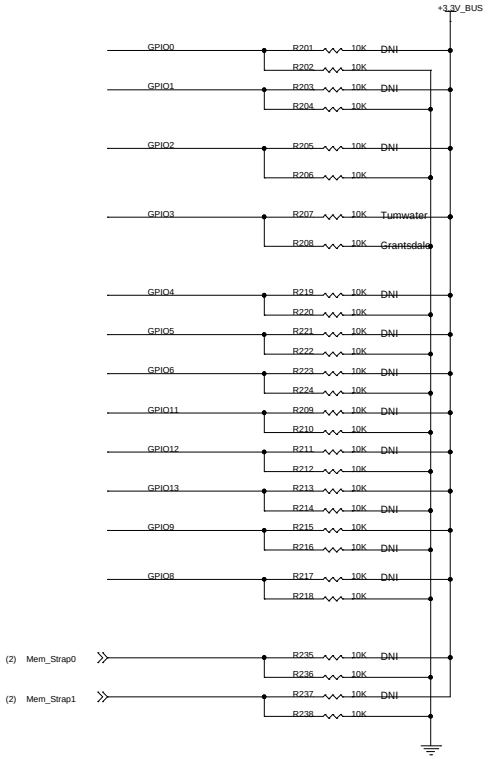
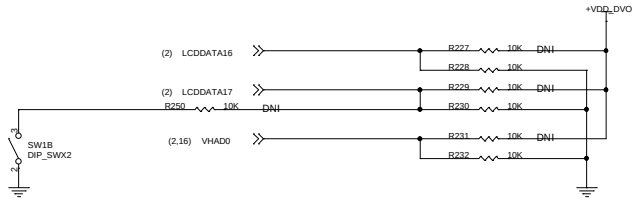
OPTION STRAPS





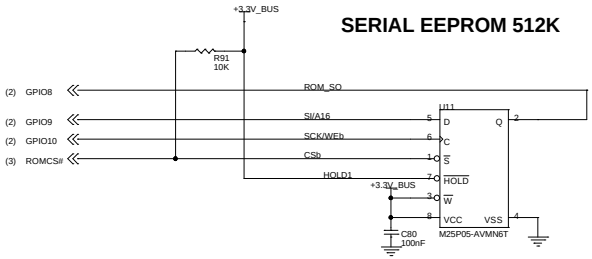
STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
CAL_BG_BACKUP	GPIO0	PCI-Express Current Calibration Bandgap Backup 0: use reference voltage from Bandgap 1: use reference voltage from resistor divider	0
PLL_CAL_FORCE_EN	GPIO1	PCI-Express PLL Calibration force enable 0: Disable PLL force calibration 1: Enable PLL force calibration	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode 01: RESERVED 10: PCI Express 1.0 mode 11: RESERVED	00
CAL_OFF	GPIO4	**Turn off PCI-Express impedance / strength calibration.** **0: enable** **1: disable** **Also used to demux** **VCOREF** **CALREF**	0
BYPASS_PLL	GPIO5	Bypass PCI-Express PLL	0
ICOMP	GPIO6	PCI-Express transmitter current compensation 0: Normal 1: Inject extra current for output buffer switching	0
DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25P011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	



STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K



<Variant Name>

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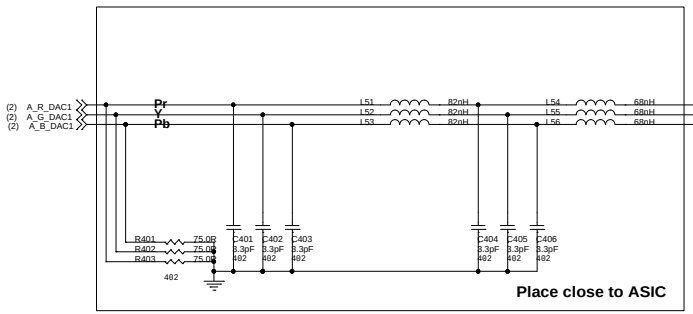
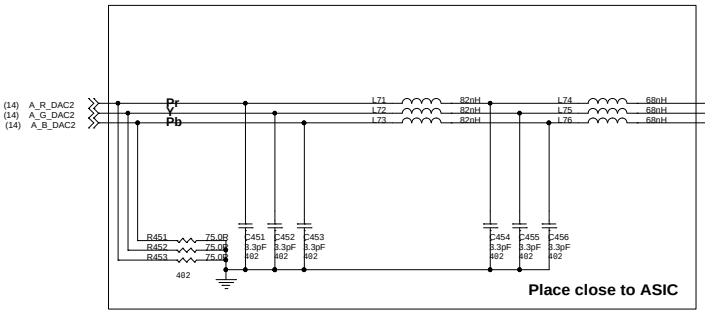
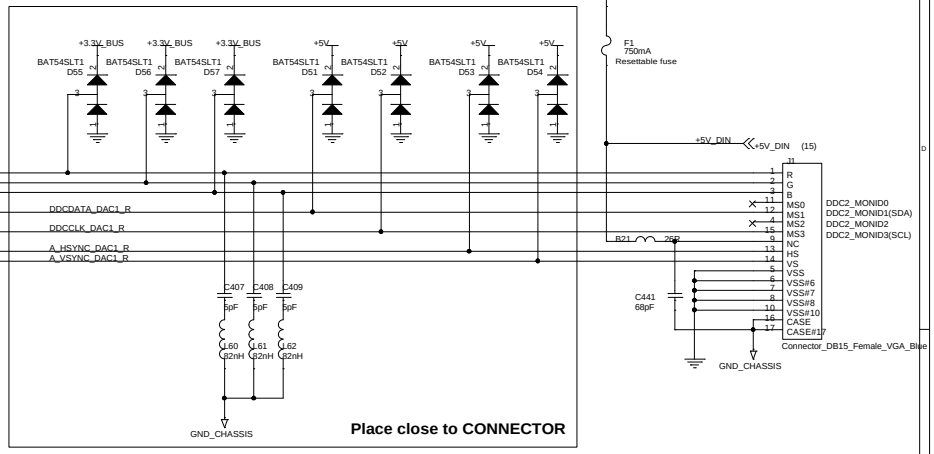
PRIMARY CRT

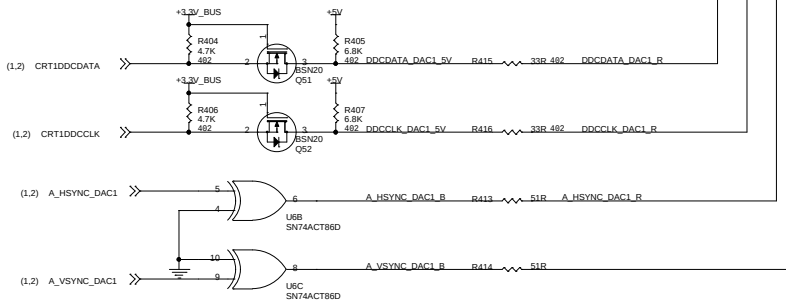


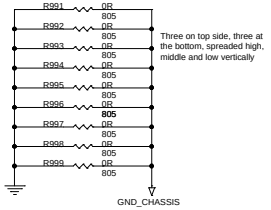
SECONDARY CRT



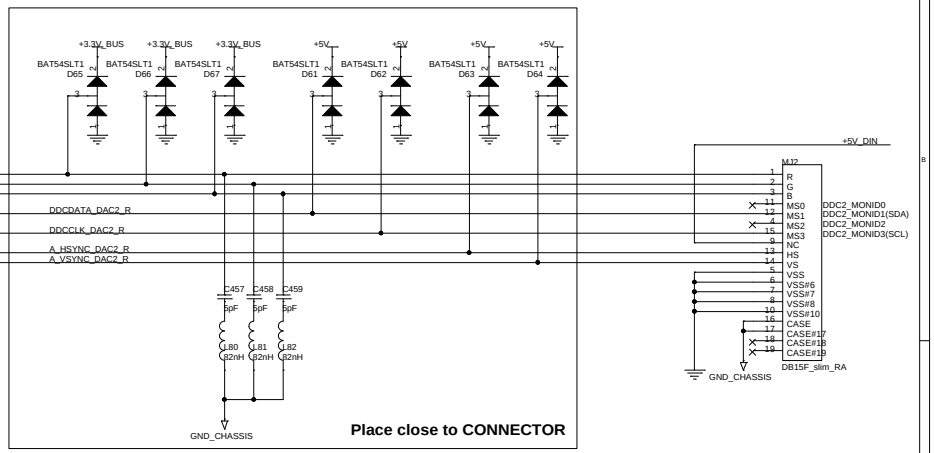
OPTIONAL ESD/HOTPLUG PROTECTION DIODES







OPTIONAL ESD/HOTPLUG PROTECTION DIODES



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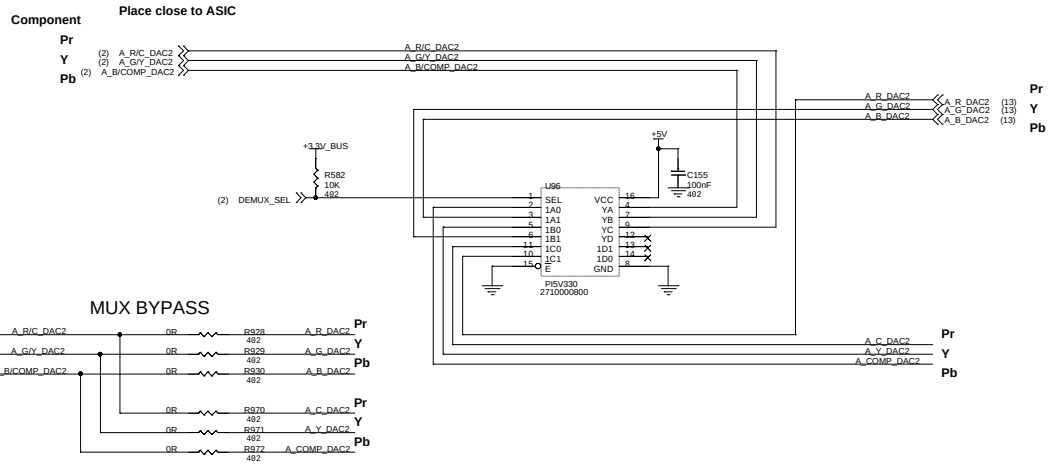

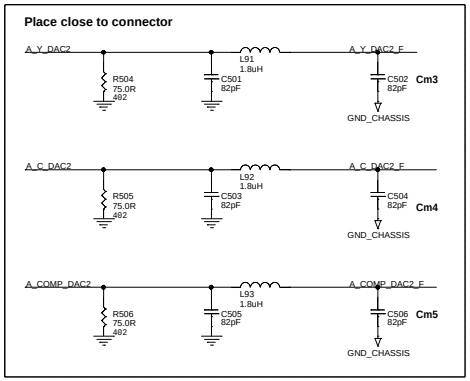

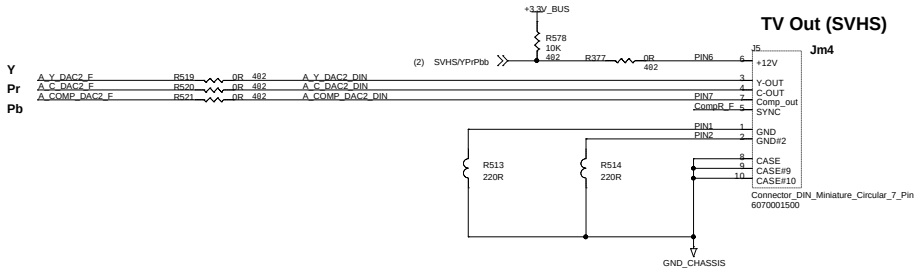

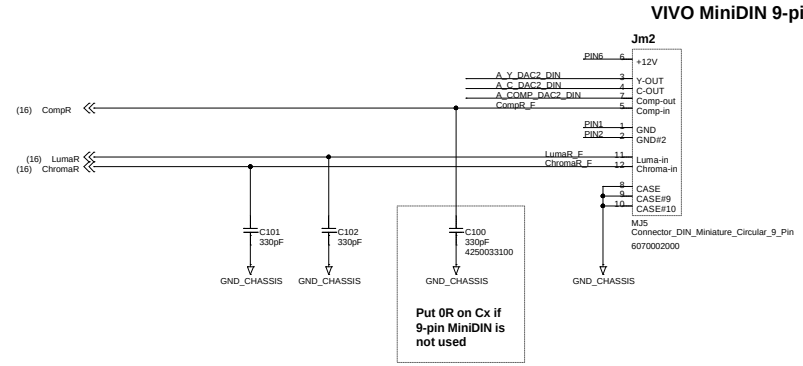

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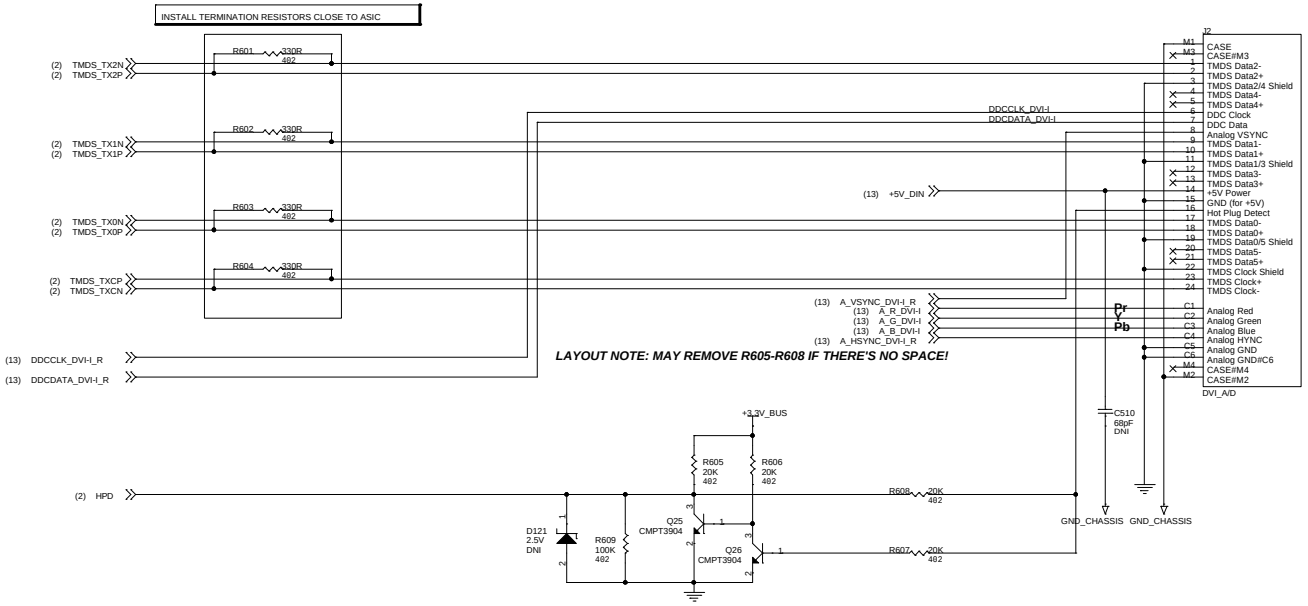
PRIMARY DVI-I CONNECTOR



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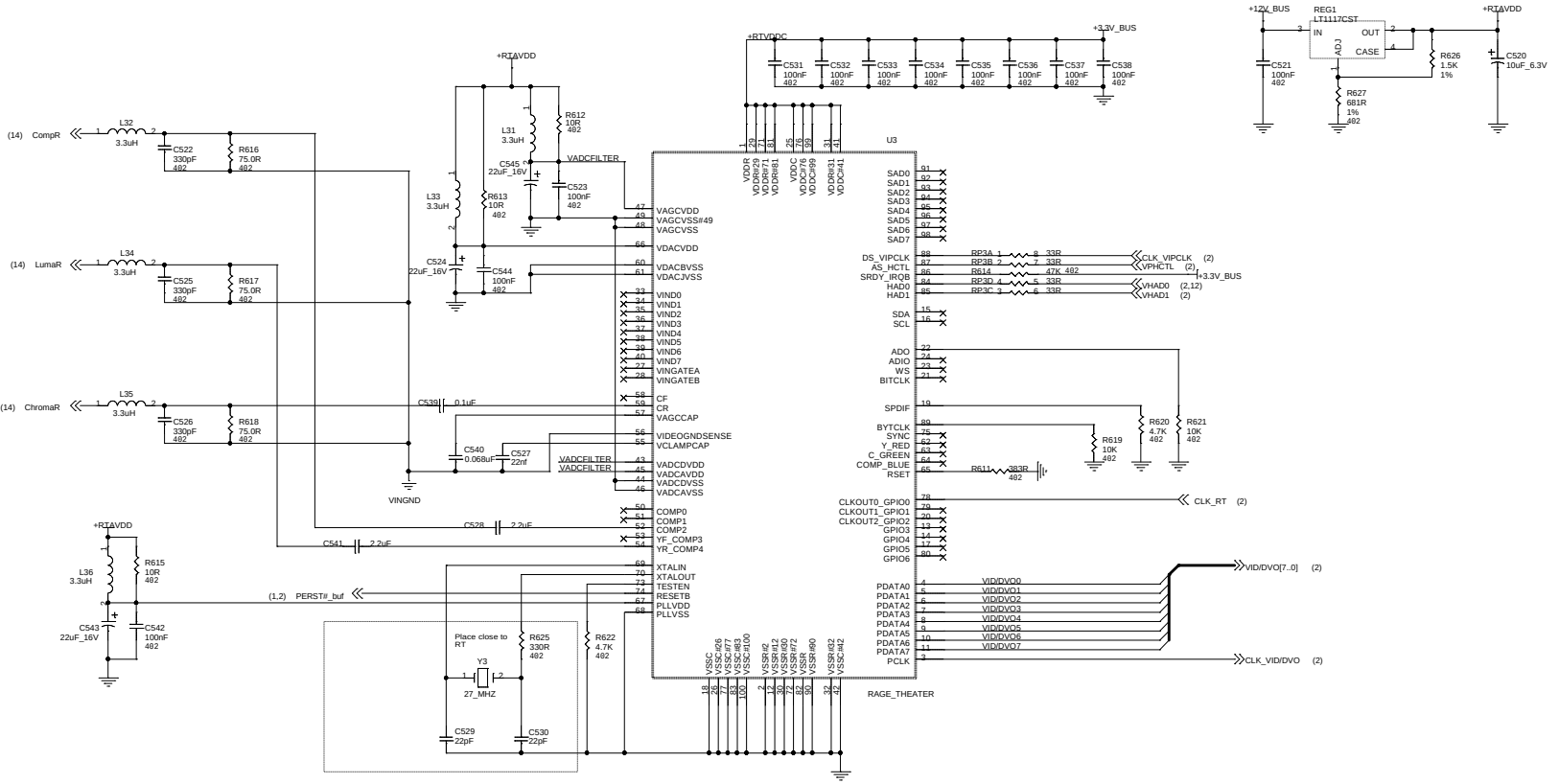

Layout Guide line of THEATER

#1 : C27 and C28 have to be placed as close as possible to the respective pins of Rage THEATER

#2 : VINGND should be seperated from Digital or Chassis Ground and have no loops

#3 : VINGND should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

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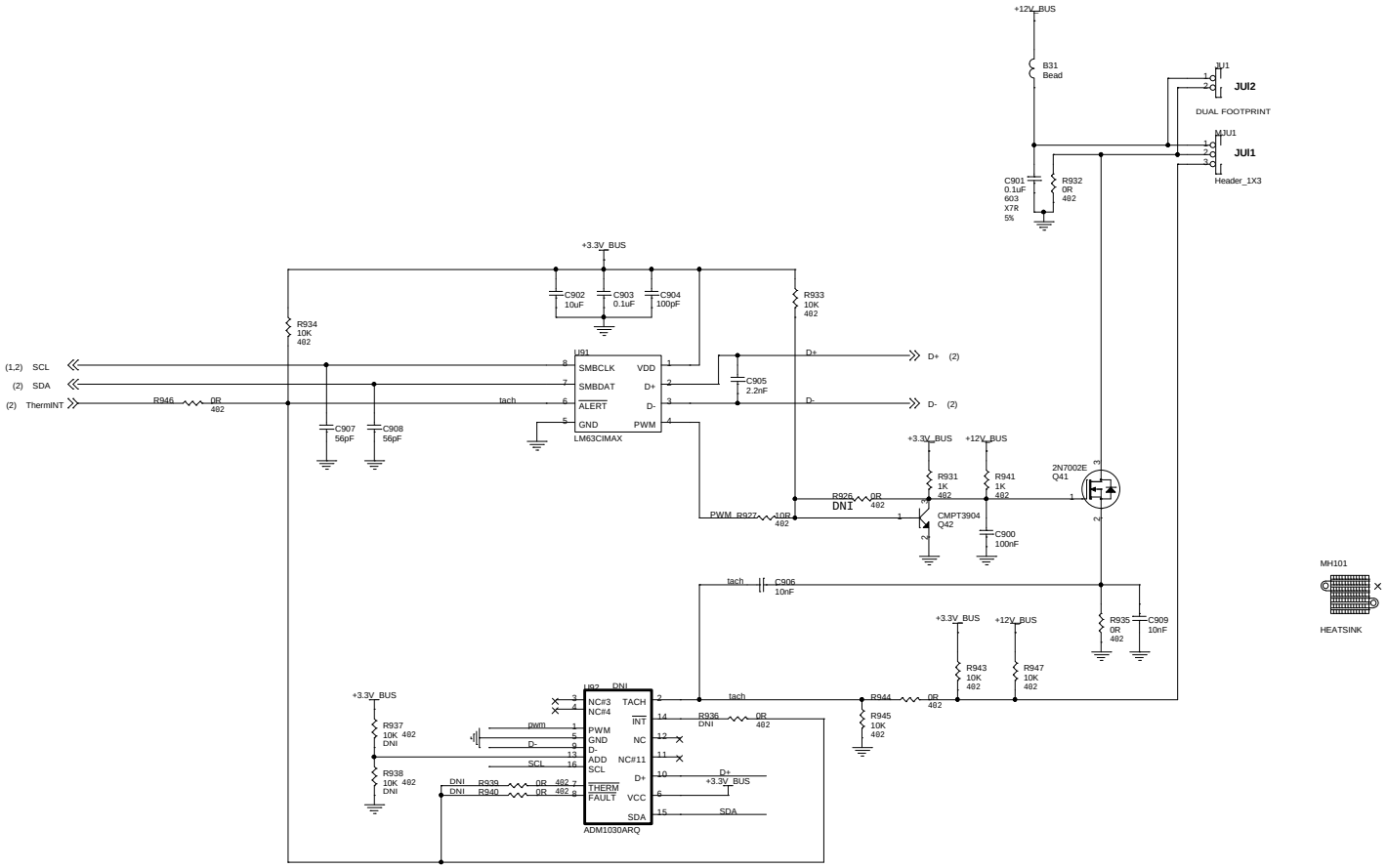
TEMPERATURE SENSE AND SPEED CONTROLLED FAN



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ASSY1

SCREW
JACKSCREW
<3rd part field>

ASSY2

SCREW
JACKSCREW
<3rd part field>

ASSY3

SCREW
JACKSCREW
<3rd part field>

ASSY4

SCREW
JACKSCREW
<3rd part field>

MISC. BOARD PARTS

ASSY7

ANTISTATIC
BAG

6_X_11
<3rd part field>

9040000900

REF5

ATI LOGO
LABEL

ATI_LOGO_LABEL

ASSY8

BLANK
LABEL

1.5W_X_0.50H
<ATIPartNumbers>

ASSY11

BRACKET

DVI, DIN, VGA, 335

MT1
MT_Hole_0.136_in.

GND_CHASSIS

<Variant Name>

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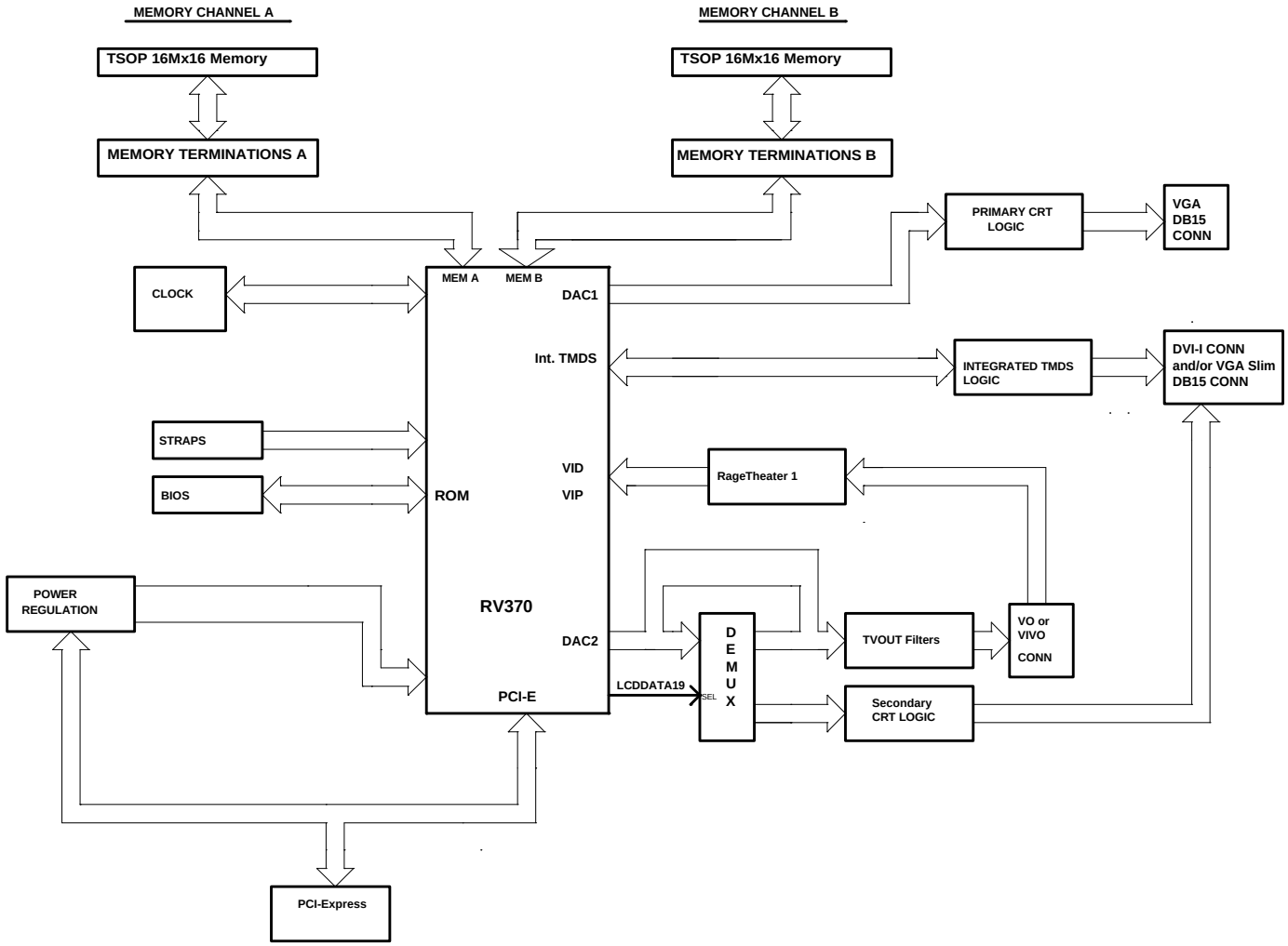

<Variant Name>

REFERENCE DESIGN

THESE SCHEMATICS ARE SUBJECT TO MODIFICATION AND DESIGN IMPROVEMENTS. PLEASE CONTACT ATI FIELD APPLICATION ENGINEERING BEFORE USING THE INFORMATION CONTAINED HEREIN.

RESTRICTION NOTICE

ATI Technologies Inc.
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<Variant Name>

Title	Schematic No.	Date:
PCI-E RV380/370 256M pterm TSOP V-VV-DI	105-A334xx-00B	**Monday, December 29, 2003**

REVISION HISTORY

Rev 1

Sch Rev	Date	REVISION DESCRIPTION
0 00A	2003-11-24	PRELIMINARY BASED ON 105-A297xx-00A 03-11-24
1 00B	2003-12-29	- (pg 02) Swap DVI DDC clock and data lines - (pg 07) Add R1043 for power dissipation - (Layout) Move C284, blocking Grantsdale PCIE connector latch