P402-A02 DESIGN -- G84/G86, 540/702 128/256 MB DDR3, VGA, DVI-I, SD/HDTV

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10402-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10402-0000-200	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
2	SKU0010	600-10402-0010-200	G86-400-500/700Mhz 256/128 MB 16Mx32 BGA135 GDDR3 DVI+VGA_HDTV-Out
3	SKU0500	600-50402-0500-200	G84-875, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
4	SKU9100	600-10402-9100-200	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

PAGE SUMMARY:

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	TABLE OF CONTENTS & REVISION HISTORY

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
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NV_PN	600-10402-0000-200 H		
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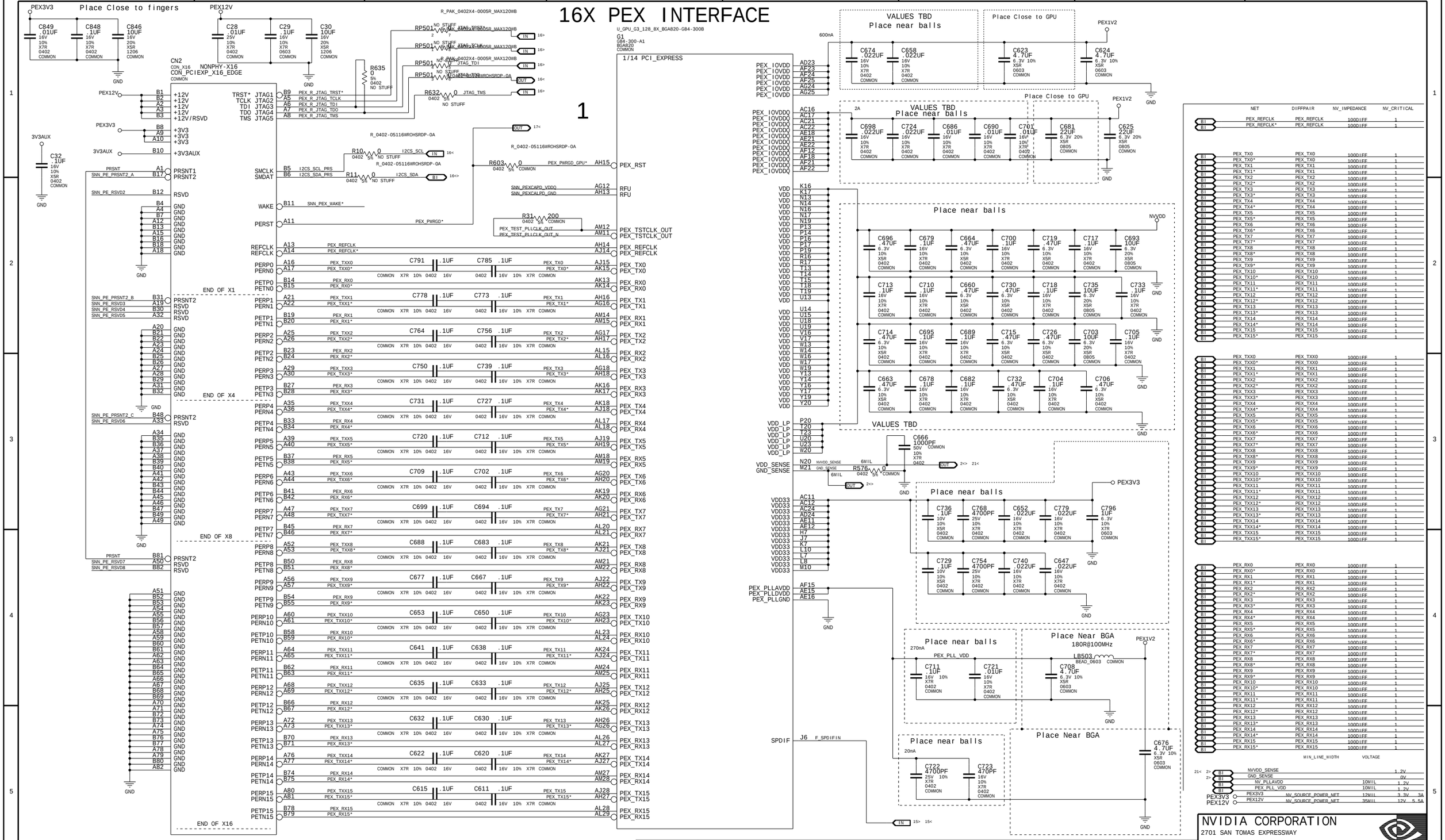
16X PEX INTERFACE



NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL
PEX_REFCLK	PEX_REFCLK	100DIFF	1
PEX_REFCLK*	PEX_REFCLK	100DIFF	1
PEX_TX0	PEX_TX0	100DIFF	1
PEX_TX0*	PEX_TX0	100DIFF	1
PEX_TX1	PEX_TX1	100DIFF	1
PEX_TX1*	PEX_TX1	100DIFF	1
PEX_TX2	PEX_TX2	100DIFF	1
PEX_TX2*	PEX_TX2	100DIFF	1
PEX_TX3	PEX_TX3	100DIFF	1
PEX_TX3*	PEX_TX3	100DIFF	1
PEX_TX4	PEX_TX4	100DIFF	1
PEX_TX4*	PEX_TX4	100DIFF	1
PEX_TX5	PEX_TX5	100DIFF	1
PEX_TX5*	PEX_TX5	100DIFF	1
PEX_TX6	PEX_TX6	100DIFF	1
PEX_TX6*	PEX_TX6	100DIFF	1
PEX_TX7	PEX_TX7	100DIFF	1
PEX_TX7*	PEX_TX7	100DIFF	1
PEX_TX8	PEX_TX8	100DIFF	1
PEX_TX8*	PEX_TX8	100DIFF	1
PEX_TX9	PEX_TX9	100DIFF	1
PEX_TX9*	PEX_TX9	100DIFF	1
PEX_TX10	PEX_TX10	100DIFF	1
PEX_TX10*	PEX_TX10	100DIFF	1
PEX_TX11	PEX_TX11	100DIFF	1
PEX_TX11*	PEX_TX11	100DIFF	1
PEX_TX12	PEX_TX12	100DIFF	1
PEX_TX12*	PEX_TX12	100DIFF	1
PEX_TX13	PEX_TX13	100DIFF	1
PEX_TX13*	PEX_TX13	100DIFF	1
PEX_TX14	PEX_TX14	100DIFF	1
PEX_TX14*	PEX_TX14	100DIFF	1
PEX_TX15	PEX_TX15	100DIFF	1
PEX_TX15*	PEX_TX15	100DIFF	1
PEX_TXX0	PEX_TXX0	100DIFF	1
PEX_TXX0*	PEX_TXX0	100DIFF	1
PEX_TXX1	PEX_TXX1	100DIFF	1
PEX_TXX1*	PEX_TXX1	100DIFF	1
PEX_TXX2	PEX_TXX2	100DIFF	1
PEX_TXX2*	PEX_TXX2	100DIFF	1
PEX_TXX3	PEX_TXX3	100DIFF	1
PEX_TXX3*	PEX_TXX3	100DIFF	1
PEX_TXX4	PEX_TXX4	100DIFF	1
PEX_TXX4*	PEX_TXX4	100DIFF	1
PEX_TXX5	PEX_TXX5	100DIFF	1
PEX_TXX5*	PEX_TXX5	100DIFF	1
PEX_TXX6	PEX_TXX6	100DIFF	1
PEX_TXX6*	PEX_TXX6	100DIFF	1
PEX_TXX7	PEX_TXX7	100DIFF	1
PEX_TXX7*	PEX_TXX7	100DIFF	1
PEX_TXX8	PEX_TXX8	100DIFF	1
PEX_TXX8*	PEX_TXX8	100DIFF	1
PEX_TXX9	PEX_TXX9	100DIFF	1
PEX_TXX9*	PEX_TXX9	100DIFF	1
PEX_TXX10	PEX_TXX10	100DIFF	1
PEX_TXX10*	PEX_TXX10	100DIFF	1
PEX_TXX11	PEX_TXX11	100DIFF	1
PEX_TXX11*	PEX_TXX11	100DIFF	1
PEX_TXX12	PEX_TXX12	100DIFF	1
PEX_TXX12*	PEX_TXX12	100DIFF	1
PEX_TXX13	PEX_TXX13	100DIFF	1
PEX_TXX13*	PEX_TXX13	100DIFF	1
PEX_TXX14	PEX_TXX14	100DIFF	1
PEX_TXX14*	PEX_TXX14	100DIFF	1
PEX_TXX15	PEX_TXX15	100DIFF	1
PEX_TXX15*	PEX_TXX15	100DIFF	1
PEX_RX0	PEX_RX0	100DIFF	1
PEX_RX0*	PEX_RX0	100DIFF	1
PEX_RX1	PEX_RX1	100DIFF	1
PEX_RX1*	PEX_RX1	100DIFF	1
PEX_RX2	PEX_RX2	100DIFF	1
PEX_RX2*	PEX_RX2	100DIFF	1
PEX_RX3	PEX_RX3	100DIFF	1
PEX_RX3*	PEX_RX3	100DIFF	1
PEX_RX4	PEX_RX4	100DIFF	1
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PEX_RX5	PEX_RX5	100DIFF	1
PEX_RX5*	PEX_RX5	100DIFF	1
PEX_RX6	PEX_RX6	100DIFF	1
PEX_RX6*	PEX_RX6	100DIFF	1
PEX_RX7	PEX_RX7	100DIFF	1
PEX_RX7*	PEX_RX7	100DIFF	1
PEX_RX8	PEX_RX8	100DIFF	1
PEX_RX8*	PEX_RX8	100DIFF	1
PEX_RX9	PEX_RX9	100DIFF	1
PEX_RX9*	PEX_RX9	100DIFF	1
PEX_RX10	PEX_RX10	100DIFF	1
PEX_RX10*	PEX_RX10	100DIFF	1
PEX_RX11	PEX_RX11	100DIFF	1
PEX_RX11*	PEX_RX11	100DIFF	1
PEX_RX12	PEX_RX12	100DIFF	1
PEX_RX12*	PEX_RX12	100DIFF	1
PEX_RX13	PEX_RX13	100DIFF	1
PEX_RX13*	PEX_RX13	100DIFF	1
PEX_RX14	PEX_RX14	100DIFF	1
PEX_RX14*	PEX_RX14	100DIFF	1
PEX_RX15	PEX_RX15	100DIFF	1
PEX_RX15*	PEX_RX15	100DIFF	1

	MIN_LINE_WIDTH	VOLTAGE
NVVDD_SENSE		1.2V
GND_SENSE		0V
NV_PLLAVDD	10MIL	1.2V
PEX_PLL_VDD	10MIL	1.2V
PEX3V3	12MIL	3.3V 3A
PEX12V	35MIL	12V 5.5A

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	PCI EXPRESS 16X, NVVDD DECOUPLING CAPS,PEX_IOVDD/Q DECOUPLING CAPS

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U_GPU_G3_128_8X_BGA820-G84-300B

G1
G84-300-A1
BGA820
COMMON

2/14 FBA

0	FBAD<0>	N27	FBAD0
1	FBAD<1>	M27	FBAD1
2	FBAD<2>	N28	FBAD2
3	FBAD<3>	L29	FBAD3
4	FBAD<4>	K27	FBAD4
5	FBAD<5>	K28	FBAD5
6	FBAD<6>	J29	FBAD6
7	FBAD<7>	J28	FBAD7
8	FBAD<8>	P30	FBAD8
9	FBAD<9>	N31	FBAD9
10	FBAD<10>	N30	FBAD10
11	FBAD<11>	N32	FBAD11
12	FBAD<12>	L31	FBAD12
13	FBAD<13>	L30	FBAD13
14	FBAD<14>	J30	FBAD14
15	FBAD<15>	L32	FBAD15
16	FBAD<16>	H30	FBAD16
17	FBAD<17>	K30	FBAD17
18	FBAD<18>	H31	FBAD18
19	FBAD<19>	F30	FBAD19
20	FBAD<20>	H32	FBAD20
21	FBAD<21>	E31	FBAD21
22	FBAD<22>	D30	FBAD22
23	FBAD<23>	E30	FBAD23
24	FBAD<24>	H28	FBAD24
25	FBAD<25>	H29	FBAD25
26	FBAD<26>	E29	FBAD26
27	FBAD<27>	J27	FBAD27
28	FBAD<28>	F27	FBAD28
29	FBAD<29>	E27	FBAD29
30	FBAD<30>	E28	FBAD30
31	FBAD<31>	F28	FBAD31
32	FBAD<32>	AD29	FBAD32
33	FBAD<33>	AE29	FBAD33
34	FBAD<34>	AD28	FBAD34
35	FBAD<35>	AC28	FBAD35
36	FBAD<36>	AB29	FBAD36
37	FBAD<37>	AA30	FBAD37
38	FBAD<38>	Y28	FBAD38
39	FBAD<39>	AB30	FBAD39
40	FBAD<40>	AM30	FBAD40
41	FBAD<41>	AF30	FBAD41
42	FBAD<42>	AJ31	FBAD42
43	FBAD<43>	AJ30	FBAD43
44	FBAD<44>	AJ32	FBAD44
45	FBAD<45>	AK29	FBAD45
46	FBAD<46>	AM31	FBAD46
47	FBAD<47>	AL30	FBAD47
48	FBAD<48>	AE32	FBAD48
49	FBAD<49>	AE30	FBAD49
50	FBAD<50>	AE31	FBAD50
51	FBAD<51>	AD30	FBAD51
52	FBAD<52>	AC31	FBAD52
53	FBAD<53>	AC32	FBAD53
54	FBAD<54>	AB32	FBAD54
55	FBAD<55>	AB31	FBAD55
56	FBAD<56>	AG27	FBAD56
57	FBAD<57>	AF28	FBAD57
58	FBAD<58>	AH28	FBAD58
59	FBAD<59>	AG28	FBAD59
60	FBAD<60>	AG29	FBAD60
61	FBAD<61>	AD27	FBAD61
62	FBAD<62>	AF27	FBAD62
63	FBAD<63>	AE28	FBAD63

FBVDD	A12		
FBVDD	A18		
FBVDD	A21		
FBVDD	A24		
FBVDD	A27		
FBVDD	A3		
FBVDD	A30		
FBVDD	A6		
FBVDD	A9		
FBVDD	AA32		
FBVDD	AD32		
FBVDD	AG32		
FBVDD	AK32		
FBVDD	C32		
FBVDD	F32		
FBVDD	J32		
FBVDD	M32		
FBVDD	R32		
FBVDDQ	AA25		
FBVDDQ	AA26		
FBVDDQ	AB25		
FBVDDQ	AB26		
FBVDDQ	G11		
FBVDDQ	G12		
FBVDDQ	G15		
FBVDDQ	G18		
FBVDDQ	G21		
FBVDDQ	G22		
FBVDDQ	H11		
FBVDDQ	H12		
FBVDDQ	H15		
FBVDDQ	H18		
FBVDDQ	H21		
FBVDDQ	H22		
FBVDDQ	L25		
FBVDDQ	L26		
FBVDDQ	M25		
FBVDDQ	M26		
FBVDDQ	R25		
FBVDDQ	R26		
FBVDDQ	V25		
FBVDDQ	V26		

FBA_CMD0	P32	FBA_CMD<0>	0
FBA_CMD1	U27	FBA_CMD<1>	1
FBA_CMD2	P31	FBA_CMD<2>	2
FBA_CMD3	U30	FBA_CMD<3>	3
FBA_CMD4	Y31	FBA_CMD<4>	4
FBA_CMD5	W32	FBA_CMD<5>	5
FBA_CMD6	W31	FBA_CMD<6>	6
FBA_CMD7	T32	FBA_CMD<7>	7
FBA_CMD8	V27	FBA_CMD<8>	8
FBA_CMD9	T28	FBA_CMD<9>	9
FBA_CMD10	T31	FBA_CMD<10>	10
FBA_CMD11	U32	FBA_CMD<11>	11
FBA_CMD12	W29	FBA_CMD<12>	12
FBA_CMD13	W30	FBA_CMD<13>	13
FBA_CMD14	T27	SNN_FBA_CMD<14>	
FBA_CMD15	V28	FBA_CMD<15>	15
FBA_CMD16	V30	FBA_CMD<16>	16
FBA_CMD17	U31	FBA_CMD<17>	17
FBA_CMD18	R27	FBA_CMD<18>	18
FBA_CMD19	V29	FBA_CMD<19>	19
FBA_CMD20	T30	FBA_CMD<20>	20
FBA_CMD21	W28	FBA_CMD<21>	21
FBA_CMD22	R29	FBA_CMD<22>	22
FBA_CMD23	R30	FBA_CMD<23>	23
FBA_CMD24	P29	FBA_CMD<24>	24
FBA_CMD25	U28	FBA_CMD<25>	25
FBA_CMD26	Y32	SNN_FBA_CMD<26>	
FBA_CMD27	Y30	SNN_FBA_CMD<27>	
FBA_CMD28	V32	SNN_FBA_CMD<28>	

FBA_CMD<26..0> OUT 4< 4>

FBA_CLK0	P28	FBA_CLK0	OUT 4<
FBA_CLK0	R28	FBA_CLK0*	OUT 4<
FBA_CLK1	Y27	FBA_CLK1	OUT 4<
FBA_CLK1	AA27	FBA_CLK1*	OUT 4<
FBA_DEBUG	AC27	LTP_FBA_DEBUG	TP505

NO STUFF

H_PLLAVDD	G23	PLLAVDD	
FBA_PLLAVDD	G25		
FBA_PLLGND	G24		

NC1	D31	SNN_GPU_NC1
NC2	D32	SNN_GPU_NC2

0	FBADQM<0>	M29	FBADQM0
1	FBADQM<1>	M30	FBADQM1
2	FBADQM<2>	G30	FBADQM2
3	FBADQM<3>	F29	FBADQM3
4	FBADQM<4>	AA29	FBADQM4
5	FBADQM<5>	AK30	FBADQM5
6	FBADQM<6>	AC30	FBADQM6
7	FBADQM<7>	AG30	FBADQM7

FBADQM<7..0> OUT 4<

0	FBADQ_WP<0>	L28	FBADQS_WP0
1	FBADQ_WP<1>	K31	FBADQS_WP1
2	FBADQ_WP<2>	G32	FBADQS_WP2
3	FBADQ_WP<3>	G28	FBADQS_WP3
4	FBADQ_WP<4>	AB28	FBADQS_WP4
5	FBADQ_WP<5>	AL32	FBADQS_WP5
6	FBADQ_WP<6>	AF32	FBADQS_WP6
7	FBADQ_WP<7>	AH30	FBADQS_WP7

FBADQS_WP<7..0> B1 4<>

0	FBADQS_RN<0>	M28	FBADQS_RN0
1	FBADQS_RN<1>	K32	FBADQS_RN1
2	FBADQS_RN<2>	G31	FBADQS_RN2
3	FBADQS_RN<3>	G27	FBADQS_RN3
4	FBADQS_RN<4>	AA28	FBADQS_RN4
5	FBADQS_RN<5>	AL31	FBADQS_RN5
6	FBADQS_RN<6>	AF31	FBADQS_RN6
7	FBADQS_RN<7>	AH29	FBADQS_RN7

FBADQS_RN<7..0> B1 4<>

FBVDDQ

Rtop R590 0402 1% NO STUFF

Rbot R562 1.27K 0402 1% NO STUFF

C627 .1UF 16V 10% X7R 0402 COMMON

FBA_VREF E32 FB_VREF1

GND

VREF = FBVDDQ * Rbot/(Rtop + Rbot)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 2.7K/(1.15K + 2.7K)

2

FBVDDQ

C645 .47UF 6.3V 10% X5R 0402 COMMON
C725 .47UF 6.3V 10% X5R 0402 COMMON
C654 .1UF 16V 10% X7R 0402 COMMON
C757 .1UF 16V 10% X7R 0402 COMMON
C680 .1UF 16V 10% X7R 0402 COMMON

C697 .1UF 16V 10% X7R 0402 COMMON
C749 .1UF 16V 10% X7R 0402 COMMON

C687 .1UF 16V 10% X7R 0402 COMMON
C642 1UF 6.3V 10% X7R 0603 COMMON

C684 .47UF 6.3V 10% X5R 0402 COMMON
C661 .47UF 6.3V 10% X5R 0402 COMMON
C716 .1UF 16V 10% X7R 0402 COMMON
C662 .1UF 16V 10% X7R 0402 COMMON
C707 1UF 6.3V 10% X7R 0603 COMMON

C659 .1UF 16V 10% X7R 0402 COMMON
C675 .1UF 16V 10% X7R 0402 COMMON
C691 .1UF 16V 10% X7R 0402 COMMON
C692 .47UF 6.3V 10% X5R 0402 COMMON
C646 .47UF 6.3V 10% X5R 0402 COMMON

GND

PLACE BELOW GPU

PLACE close to balls

C671 .01UF 16V 10% X7R 0402 COMMON
C670 .1UF 16V 10% X7R 0402 COMMON
C669 1UF 6.3V 10% X5R 0603 COMMON

GND

PEX1V2

240R@100MHz LB502 BEAD_0402 COMMON

NET	MIN_LINE_WIDTH
B1 PLLAVDD	10MIL
B1 FBA_PLLAVDD_R	10MIL

FBVDDQ

C601 10UF 6.3V 20% X5R 0805 COMMON
C602 10UF 6.3V 20% X5R 0805 COMMON
C607 10UF 6.3V 20% X5R 0805 COMMON
C840 10UF 6.3V 20% X5R 0805 COMMON

GND

PLACE MIDWAY BETWEEN GPU AND MEMORY

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBA MEMORY INTERFACE, GPU FBVDD/Q DECOUPLING CAPS

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NV_PN	600-10402-0000-200 H		
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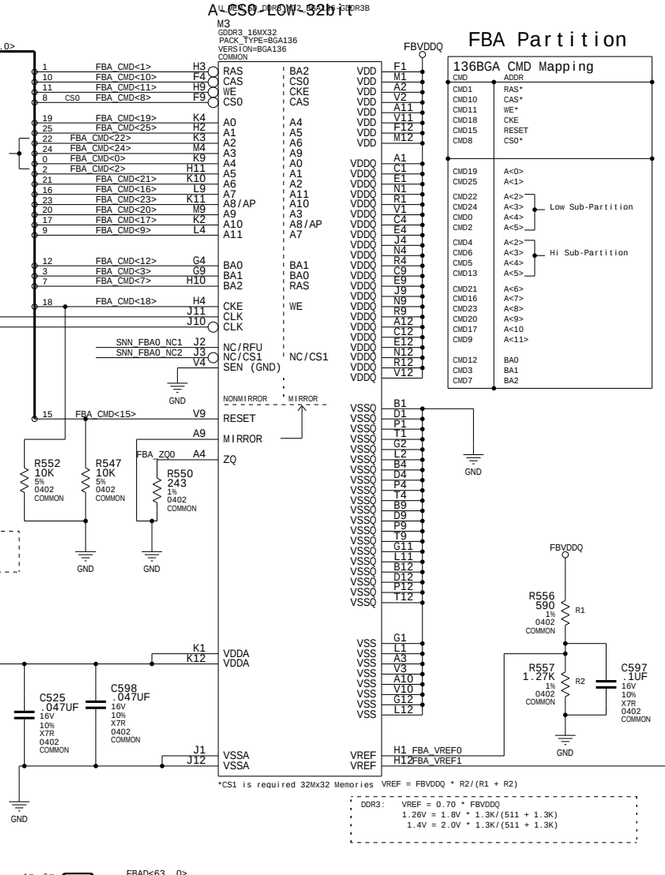
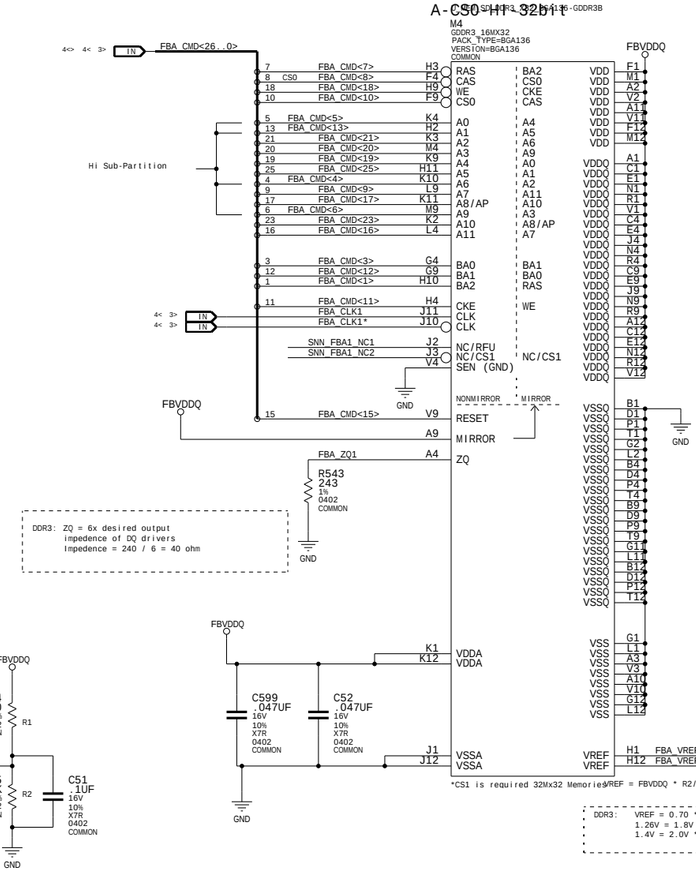
FrameBuffer: Partition A 8Mx32 BGA136 DDR3



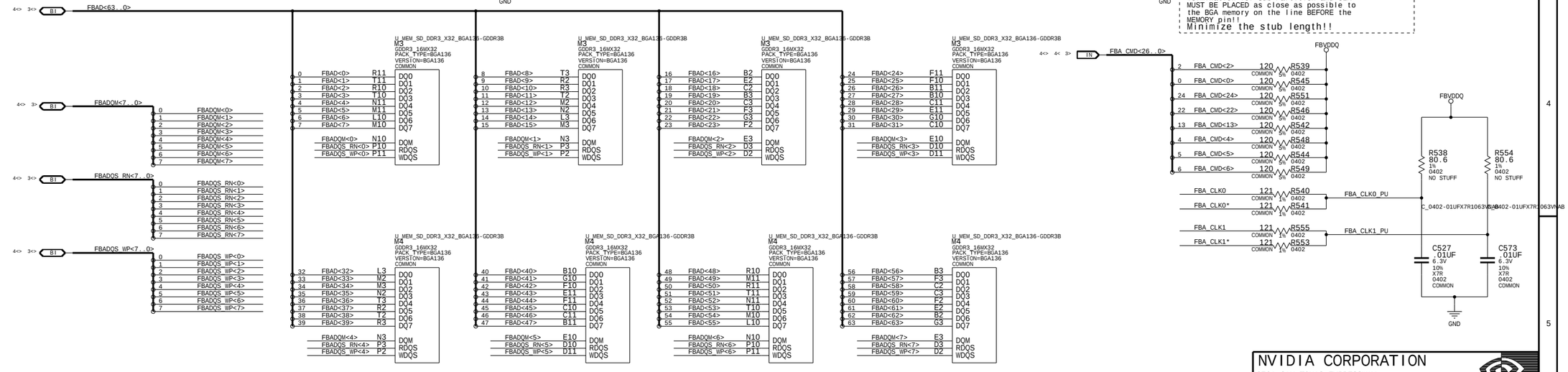


NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
FBA_CLK0	FBA_CLK0	80DIFF	1
FBA_CLK0*	FBA_CLK0	80DIFF	1
FBA_CLK1	FBA_CLK1	80DIFF	1
FBA_CLK1*	FBA_CLK1	80DIFF	1
FBAD<63..0>		40OHM	1
FBADQM<7..0>		40OHM	1
FBA_CMD<26:0>		40OHM	1

MIN_LINE_WIDTH

FBA_VREF0	12MIL
FBA_VREF1	12MIL
FBA_VREF2	12MIL
FBA_VREF3	12MIL

NV_IMPEDANCE	DIFFPAIR	NV_CRITICAL_NET
FBADQS_WP<7:0>		1
FBADQS_RN<7:0>		1



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBA 8Mx32 DDR3 MEMORIES, FBA COMMAND BUS PU'S, FBA CLK TERMS

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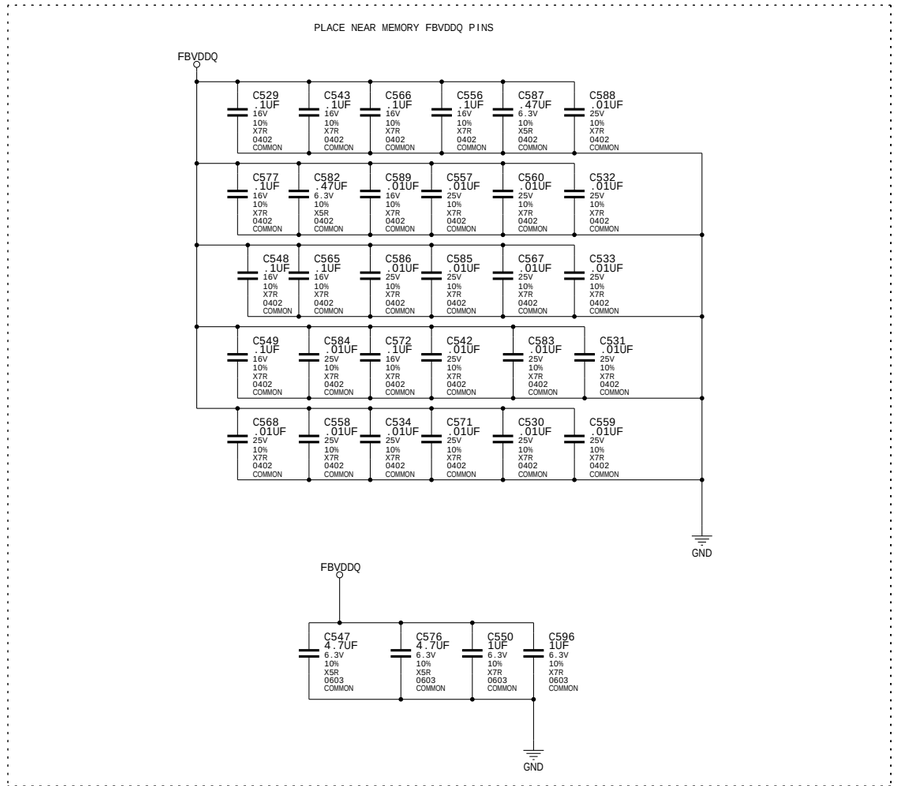
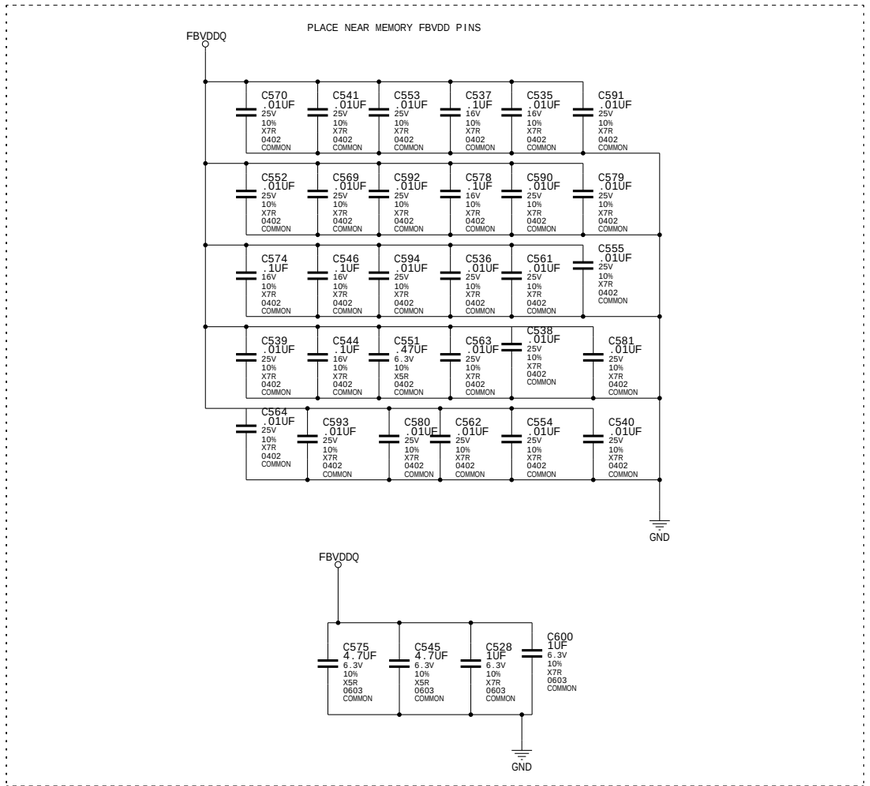
FRAME BUFFER: PARTITION A DECOUPLING

Decoupling for FBA 0..31



Decoupling for FBA 32..63



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBA MEMORY FBVDD/Q DECOUPLING CAPS

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U_GPU_G3_128_8X_BGA820-G84-300-A1

G1

G84-300-A1
BGA820
COMMON

3/14 FBC

7<>	BI	FBCD<63..0>	
0	FBCD<0>	B7	FBCD0
1	FBCD<1>	A7	FBCD1
2	FBCD<2>	C7	FBCD2
3	FBCD<3>	A2	FBCD3
4	FBCD<4>	B2	FBCD4
5	FBCD<5>	C4	FBCD5
6	FBCD<6>	A5	FBCD6
7	FBCD<7>	B5	FBCD7
8	FBCD<8>	F9	FBCD8
9	FBCD<9>	F10	FBCD9
10	FBCD<10>	D12	FBCD10
11	FBCD<11>	D9	FBCD11
12	FBCD<12>	E12	FBCD12
13	FBCD<13>	D11	FBCD13
14	FBCD<14>	E8	FBCD14
15	FBCD<15>	D8	FBCD15
16	FBCD<16>	E7	FBCD16
17	FBCD<17>	F7	FBCD17
18	FBCD<18>	D6	FBCD18
19	FBCD<19>	D5	FBCD19
20	FBCD<20>	D3	FBCD20
21	FBCD<21>	E4	FBCD21
22	FBCD<22>	C3	FBCD22
23	FBCD<23>	B4	FBCD23
24	FBCD<24>	C10	FBCD24
25	FBCD<25>	B10	FBCD25
26	FBCD<26>	C9	FBCD26
27	FBCD<27>	A10	FBCD27
28	FBCD<28>	C11	FBCD28
29	FBCD<29>	C12	FBCD29
30	FBCD<30>	A11	FBCD30
31	FBCD<31>	B11	FBCD31
32	FBCD<32>	B28	FBCD32
33	FBCD<33>	C27	FBCD33
34	FBCD<34>	C26	FBCD34
35	FBCD<35>	B26	FBCD35
36	FBCD<36>	C30	FBCD36
37	FBCD<37>	B31	FBCD37
38	FBCD<38>	C29	FBCD38
39	FBCD<39>	A31	FBCD39
40	FBCD<40>	D28	FBCD40
41	FBCD<41>	D27	FBCD41
42	FBCD<42>	F26	FBCD42
43	FBCD<43>	D24	FBCD43
44	FBCD<44>	E23	FBCD44
45	FBCD<45>	E26	FBCD45
46	FBCD<46>	E24	FBCD46
47	FBCD<47>	F23	FBCD47
48	FBCD<48>	B23	FBCD48
49	FBCD<49>	A23	FBCD49
50	FBCD<50>	C25	FBCD50
51	FBCD<51>	C23	FBCD51
52	FBCD<52>	A22	FBCD52
53	FBCD<53>	C22	FBCD53
54	FBCD<54>	C21	FBCD54
55	FBCD<55>	B22	FBCD55
56	FBCD<56>	E22	FBCD56
57	FBCD<57>	D22	FBCD57
58	FBCD<58>	D21	FBCD58
59	FBCD<59>	E21	FBCD59
60	FBCD<60>	E18	FBCD60
61	FBCD<61>	D19	FBCD61
62	FBCD<62>	D18	FBCD62
63	FBCD<63>	E19	FBCD63

7<>	OUT	FBCDQM<7..0>	
0	FBCDQM<0>	A4	FBCDQM0
1	FBCDQM<1>	E11	FBCDQM1
2	FBCDQM<2>	F5	FBCDQM2
3	FBCDQM<3>	C9	FBCDQM3
4	FBCDQM<4>	C28	FBCDQM4
5	FBCDQM<5>	F24	FBCDQM5
6	FBCDQM<6>	C24	FBCDQM6
7	FBCDQM<7>	E20	FBCDQM7

7<>	BI	FBCDQS_WP<7..0>	
0	FBCDQS_WP<0>	C5	FBCDQS_WP0
1	FBCDQS_WP<1>	E10	FBCDQS_WP1
2	FBCDQS_WP<2>	E5	FBCDQS_WP2
3	FBCDQS_WP<3>	B8	FBCDQS_WP3
4	FBCDQS_WP<4>	A29	FBCDQS_WP4
5	FBCDQS_WP<5>	D25	FBCDQS_WP5
6	FBCDQS_WP<6>	B25	FBCDQS_WP6
7	FBCDQS_WP<7>	F20	FBCDQS_WP7

7<>	BI	FBCDQS_RN<7..0>	
0	FBCDQS_RN<0>	C6	FBCDQS_RN0
1	FBCDQS_RN<1>	E9	FBCDQS_RN1
2	FBCDQS_RN<2>	E6	FBCDQS_RN2
3	FBCDQS_RN<3>	A8	FBCDQS_RN3
4	FBCDQS_RN<4>	B29	FBCDQS_RN4
5	FBCDQS_RN<5>	E25	FBCDQS_RN5
6	FBCDQS_RN<6>	A25	FBCDQS_RN6
7	FBCDQS_RN<7>	F21	FBCDQS_RN7

SNN_FBC_VREF_A28 — A28 — FB_VREF2

FBVTT	AA23	SNN_FBVTT_AA23
FBVTT	AB23	SNN_FBVTT_AB23
FBVTT	H16	SNN_FBVTT_H16
FBVTT	H17	SNN_FBVTT_H17
FBVTT	J10	SNN_FBVTT_J10
FBVTT	J23	SNN_FBVTT_J23
FBVTT	J24	SNN_FBVTT_J24
FBVTT	J9	SNN_FBVTT_J9
FBVTT	K11	SNN_FBVTT_K11
FBVTT	K12	SNN_FBVTT_K12
FBVTT	K21	SNN_FBVTT_K21
FBVTT	K22	SNN_FBVTT_K22
FBVTT	K24	SNN_FBVTT_K24
FBVTT	K9	SNN_FBVTT_K9
FBVTT	L23	SNN_FBVTT_L23
FBVTT	M23	SNN_FBVTT_M23
FBVTT	T25	SNN_FBVTT_T25
FBVTT	U25	SNN_FBVTT_U25

FBC_CMD<26..0> OUT 7<

FBC_CMD0	C13	FBC_CMD<0>	0
FBC_CMD1	A16	FBC_CMD<1>	1
FBC_CMD2	A13	FBC_CMD<2>	2
FBC_CMD3	B17	FBC_CMD<3>	3
FBC_CMD4	B20	FBC_CMD<4>	4
FBC_CMD5	A19	FBC_CMD<5>	5
FBC_CMD6	B19	FBC_CMD<6>	6
FBC_CMD7	B14	FBC_CMD<7>	7
FBC_CMD8	E16	FBC_CMD<8>	8
FBC_CMD9	A14	FBC_CMD<9>	9
FBC_CMD10	C15	FBC_CMD<10>	10
FBC_CMD11	B16	FBC_CMD<11>	11
FBC_CMD12	F17	FBC_CMD<12>	12
FBC_CMD13	C19	FBC_CMD<13>	13
FBC_CMD14	D15	SNN_FBC_CMD<14>	
FBC_CMD15	C17	FBC_CMD<15>	15
FBC_CMD16	A17	FBC_CMD<16>	16
FBC_CMD17	C16	FBC_CMD<17>	17
FBC_CMD18	D14	FBC_CMD<18>	18
FBC_CMD19	F16	FBC_CMD<19>	19
FBC_CMD20	C14	FBC_CMD<20>	20
FBC_CMD21	C18	FBC_CMD<21>	21
FBC_CMD22	E14	FBC_CMD<22>	22
FBC_CMD23	B13	FBC_CMD<23>	23
FBC_CMD24	E15	FBC_CMD<24>	24
FBC_CMD25	F15	FBC_CMD<25>	25
FBC_CMD26	A20	SNN_FBC_CMD<26>	
FBC_CMD27	C20	SNN_FBC_CMD<27>	
FBC_CMD28	A15	SNN_FBC_CMD<28>	

FBC_CLK0	E13	FBC_CLK0	OUT 7<
FBC_CLK0	F13	FBC_CLK0*	OUT 7<
FBC_CLK1	F18	FBC_CLK1	OUT 7<
FBC_CLK1	E17	FBC_CLK1*	OUT 7<

FBC_DEBUG — F12 — LTP_FBC_DEBUG — FP3

NO STUFF

FBC_PLLVDD	G8	SNN_FBC_PLLVDD_G8	
FBC_PLLAVDD	G10	FBC_PLLAVDD	
FBC_PLLGND	G9		GND

FBCAL_PD_VDDQ	K26	FBCAL_PD	R573 43.2 0402 1% COMMON	FBVDDQ
FBCAL_PU_GND	H26	FBCAL_PU	R575 40.2 0402 1% COMMON	
FBCAL_TERM_GND	J26	FBCAL_TERM	R572 40.2 0402 1% COMMON	GND

Place close to balls

L_BEAD_0402-240R100MHZFERRITB

FBC_PLLAVDD → LB504 240R@100MHz BEAD_0402 COMMON → PEX1V2

C743	.01UF	16V	10% X7R 0402 COMMON
C742	.1UF	16V	10% X7R 0402 COMMON
C741	1UF	6.3V	10% X5R 0402 COMMON
C746	4.7UF	6.3V	10% X5R 0603 COMMON

GND

NET	MIN_LINE_WIDTH
FBC_PLLVDD	10MIL
FBC_PLLAVDD	10MIL
FBC_PLLAVDD_R	10MIL

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBC MEMORY INTERFACE, GPU FBVTT

NV_PN	600-10402-0000-200 H		
ID	p402	PAGE	6 OF 21
NAME	broth	DATE	03-APR-2007

FRAMEBUFFER: PARTITION C 8Mx32 BGA136 DDR3

A-CS0-LOW-32bit

U_MEM_SD_DDR3_X32_BGA136-GDDR3B
M1
GDDR3_16MX32
PACK_TYPE=BGA136
VERSION=BGA136
COMMON

FBC_CMD<26..0> (IN)

1	FBC_CMD<1>	H3	RAS	BA2	VDD	F1
10	FBC_CMD<10>	F4	CAS	CS0	VDD	M1
11	FBC_CMD<11>	H9	WE	CKE	VDD	A2
8	FBC_CMD<8>	F9	CS0	CAS	VDD	V2
					VDD	A11
19	FBC_CMD<19>	K4	A0	A4	VDD	V11
25	FBC_CMD<25>	H2	A1	A5	VDD	F12
22	FBC_CMD<22>	K3	A2	A6	VDD	M12
24	FBC_CMD<24>	M4	A3	A9		
0	FBC_CMD<0>	K9	A4	A0	VDDQ	A1
2	FBC_CMD<2>	H11	A5	A1	VDDQ	C1
21	FBC_CMD<21>	K10	A6	A2	VDDQ	E1
16	FBC_CMD<16>	L9	A7	A11	VDDQ	N1
23	FBC_CMD<23>	K11	A8/AP	A10	VDDQ	R1
20	FBC_CMD<20>	M9	A9	A3	VDDQ	V1
17	FBC_CMD<17>	K2	A10	A8/AP	VDDQ	C4
9	FBC_CMD<9>	L4	A11	A7	VDDQ	E4
					VDDQ	J4
					VDDQ	N4
12	FBC_CMD<12>	G4			VDDQ	R4
3	FBC_CMD<3>	G9	BA0	BA1	VDDQ	C9
7	FBC_CMD<7>	H10	BA1	BA0	VDDQ	E9
			BA2	RAS	VDDQ	J9
18	FBC_CMD<18>	H4			VDDQ	N9
	FBC_CLK0 (IN)	J11	CKE	WE	VDDQ	R9
	FBC_CLK0* (IN)	J10	CLK		VDDQ	A12
					VDDQ	C12
	SNN_FBCO_NC1	J2	NC/RFU		VDDQ	E12
	SNN_FBCO_NC2	J3	NC/CS1	NC/CS1	VDDQ	N12
		V4	SEN (GND)		VDDQ	R12
					VDDQ	V12
			NONMIRROR	MIRROR		
15	FBC_CMD<15>	V9	RESET		VSSQ	B1
		A9	MIRROR		VSSQ	D1
	FBC_ZQ0	A4	ZQ		VSSQ	P1
					VSSQ	T1
					VSSQ	G2
					VSSQ	L2
					VSSQ	B4
					VSSQ	D4
					VSSQ	P4
					VSSQ	T4
					VSSQ	B9
					VSSQ	D9
					VSSQ	P9
					VSSQ	T9
					VSSQ	G11
					VSSQ	L11
					VSSQ	B12
					VSSQ	D12
					VSSQ	P12
					VSSQ	T12
					VSS	G1
					VSS	L1
					VSS	A3
					VSS	V3
					VSS	A10
					VSS	V10
					VSS	G12
					VSS	L12
		K1	VDDA			
		K12	VDDA			
		J1	VSSA			
		J12	VSSA			
					VREF	H1 FBC_VREF0
					VREF	H12 FBC_VREF1

Low Sub-Partition

*CS1 is required 32Mx32 Memories

DDR3: ZQ = 6x desired output
Impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

DDR3: CKE DETERMINES THE ODT VALUE FOR CMD PINS
CKE = 0 --> ODT = ZQ/2
CKE = 1 --> ODT = ZQ

R578 10K 5% 0402 COMMON
R577 10K 5% 0402 COMMON
R615 243 1% 0402 COMMON

C789 .047UF 16V 10% X7R 0402 COMMON
C792 .047UF 16V 10% X7R 0402 COMMON

FBVDDQ
GND

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 1.3K/(511 + 1.3K)
1.4V = 2.0V * 1.3K/(511 + 1.3K)

R605 590 1% 0402 COMMON R1
R601 1.27K 1% 0402 COMMON R2
C798 .1UF 16V 10% X7R 0402 COMMON
R29 590 1% 0402 COMMON R1
R30 1.27K 1% 0402 COMMON R2
C39 .1UF 16V 10% X7R 0402 COMMON

FBA Partition

136BGA CMD Mapping

CMD	ADDR
CMD1	RAS*
CMD10	CAS*
CMD11	WE*
CMD18	CKE
CMD15	RESET
CMD8	CS0*
CMD19	A<0>
CMD25	A<1>
CMD22	A<2>
CMD24	A<3> (Low Sub-Partition)
CMD0	A<4>
CMD2	A<5>
CMD4	A<2>
CMD6	A<3> (Hi Sub-Partition)
CMD5	A<4>
CMD13	A<5>
CMD21	A<6>
CMD16	A<7>
CMD23	A<8>
CMD20	A<9>
CMD17	A<10
CMD9	A<11>
CMD12	BA0
CMD3	BA1
CMD7	BA2

A2-CS0-HI-32bit

U_MEM_SD_DDR3_X32_BGA136-GDDR3B
M2
GDDR3_16MX32
PACK_TYPE=BGA136
VERSION=BGA136
COMMON

FBC_CMD<26..0>

7	FBC_CMD<7>	H3	RAS	BA2	VDD	F1
8	FBC_CMD<8>	F4	CAS	CS0	VDD	M1
18	FBC_CMD<18>	H9	WE	CKE	VDD	A2
10	FBC_CMD<10>	F9	CS0	CAS	VDD	V2
					VDD	A11
5	FBC_CMD<5>	K4	A0	A4	VDD	V11
13	FBC_CMD<13>	H2	A1	A5	VDD	F12
21	FBC_CMD<21>	K3	A2	A6	VDD	M12
20	FBC_CMD<20>	M4	A3	A9		
19	FBC_CMD<19>	K9	A4	A0	VDDQ	A1
25	FBC_CMD<25>	H11	A5	A1	VDDQ	C1
4	FBC_CMD<4>	K10	A6	A2	VDDQ	E1
9	FBC_CMD<9>	L9	A7	A11	VDDQ	N1
17	FBC_CMD<17>	K11	A8/AP	A10	VDDQ	R1
6	FBC_CMD<6>	M9	A9	A3	VDDQ	V1
23	FBC_CMD<23>	K2	A10	A8/AP	VDDQ	C4
16	FBC_CMD<16>	L4	A11	A7	VDDQ	E4
					VDDQ	J4
					VDDQ	N4
3	FBC_CMD<3>	G4			VDDQ	R4
12	FBC_CMD<12>	G9	BA0	BA1	VDDQ	C9
1	FBC_CMD<1>	H10	BA1	BA0	VDDQ	E9
			BA2	RAS	VDDQ	J9
11	FBC_CMD<11>	H4			VDDQ	N9
	FBC_CLK1 (IN)	J11	CKE	WE	VDDQ	R9
	FBC_CLK1* (IN)	J10	CLK		VDDQ	A12
					VDDQ	C12
	SNN_FBC1_NC1	J2	NC/RFU		VDDQ	E12
	SNN_FBC1_NC2	J3	NC/CS1	NC/CS1	VDDQ	N12
		V4	SEN (GND)		VDDQ	R12
					VDDQ	V12
			NONMIRROR	MIRROR		
15	FBC_CMD<15>	V9	RESET		VSSQ	B1
		A9	MIRROR		VSSQ	D1
	FBC_ZQ1	A4	ZQ		VSSQ	P1
					VSSQ	T1
					VSSQ	G2
					VSSQ	L2
					VSSQ	B4
					VSSQ	D4
					VSSQ	P4
					VSSQ	T4
					VSSQ	B9
					VSSQ	D9
					VSSQ	P9
					VSSQ	T9
					VSSQ	G11
					VSSQ	L11
					VSSQ	B12
					VSSQ	D12
					VSSQ	P12
					VSSQ	T12
					VSS	G1
					VSS	L1
					VSS	A3
					VSS	V3
					VSS	A10
					VSS	V10
					VSS	G12
					VSS	L12
		K1	VDDA			
		K12	VDDA			
		J1	VSSA			
		J12	VSSA			
					VREF	H1 FBC_VREF2
					VREF	H12 FBC_VREF3

Hi Sub-Partition

*CS1 is required 32Mx32 Memories

DDR3: ZQ = 6x desired output
impedence of DQ drivers
impedence = 240 / 6 = 40 ohm

R560 243 1% 0402 COMMON

C634 .047UF 16V 10% X7R 0402 COMMON
C40 .047UF 16V 10% X7R 0402 COMMON

FBVDDQ
GND

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 1.3K/(511 + 1.3K)
1.4V = 2.0V * 1.3K/(511 + 1.3K)

R33 590 1% 0402 COMMON R1
R32 1.27K 1% 0402 COMMON R2
C41 .1UF 16V 10% X7R 0402 COMMON
R564 590 1% 0402 COMMON R1
R563 1.27K 1% 0402 COMMON R2
C629 .1UF 16V 10% X7R 0402 COMMON

NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
FBC_CLK0 (IN)	FBC_CLK0	80DIFF	1
FBC_CLK0* (IN)	FBC_CLK0	80DIFF	1
FBC_CLK1 (IN)	FBC_CLK1	80DIFF	1
FBC_CLK1* (IN)	FBC_CLK1	80DIFF	1
FBCD<63..0> (BI)		40OHM	1
FBCDQM<7..0> (BI)		40OHM	1
FBC_CMD<26..0> (IN)		40OHM	1
FBC_VREF0 (BI)		MIN_LINE_WIDTH 12MIL	
FBC_VREF1 (BI)		12MIL	
FBC_VREF2 (BI)		12MIL	
FBC_VREF3 (BI)		12MIL	
FBCDQS_WP<7:0> (BI)		40OHM	1
FBCDQS_RN<7:0> (BI)		40OHM	1

NV_IMPEDANCE	DIFFPAIR	NV_CRITICAL_NET

FBCD<63..0> (BI)

FBCDQM<7..0> (BI)

FBCDQS_RN<7..0> (BI)

FBCDQS_WP<7..0> (BI)

U_MEM_SD_DDR3_X32_BGA136-GDDR3B
M1 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

0	FBCD<0>	B2	DQ0	
1	FBCD<1>	C2	DQ1	
2	FBCD<2>	E2	DQ2	
3	FBCD<3>	F2	DQ3	
4	FBCD<4>	G3	DQ4	
5	FBCD<5>	F3	DQ5	
6	FBCD<6>	C3	DQ6	
7	FBCD<7>	B3	DQ7	
	FBCDQM<0>	E3	DQM	
	FBCDQS_RN<0>	D3	RDQS	
	FBCDQS_WP<0>	D2	WDQS	

U_MEM_SD_DDR3_X32_BGA136-GDDR3B
M1 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

8	FBCD<8>	M11	DQ0	
9	FBCD<9>	T10	DQ1	
10	FBCD<10>	R11	DQ2	
11	FBCD<11>	N11	DQ3	
12	FBCD<12>	T11	DQ4	
13	FBCD<13>	R10	DQ5	
14	FBCD<14>	L10	DQ6	
15	FBCD<15>	M10	DQ7	
	FBCDQM<1>	N10	DQM	
	FBCDQS_RN<1>	P10	RDQS	
	FBCDQS_WP<1>	P11	WDQS	

U_MEM_SD_DDR3_X32_BGA136-GDDR3B
M1 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

16	FBCD<16>	B10	DQ0	
17	FBCD<17>	G10	DQ1	
18	FBCD<18>	F11	DQ2	
19	FBCD<19>	F10	DQ3	
20	FBCD<20>	C11	DQ4	
21	FBCD<21>	E11	DQ5	
22	FBCD<22>	B11	DQ6	
23	FBCD<23>	C10	DQ7	
	FBCDQM<2>	E10	DQM	
	FBCDQS_RN<2>	D10	RDQS	
	FBCDQS_WP<2>	D11	WDQS	

U_MEM_SD_DDR3_X32_BGA136-GDDR3B
M1 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

24	FBCD<24>	M2	DQ0	
25	FBCD<25>	N2	DQ1	
26	FBCD<26>	L3	DQ2	
27	FBCD<27>	M3	DQ3	
28	FBCD<28>	R2	DQ4	
29	FBCD<29>	R3	DQ5	
30	FBCD<30>	T2	DQ6	
31	FBCD<31>	T3	DQ7	
	FBCDQM<3>	N3	DQM	
	FBCDQS_RN<3>	P3	RDQS	
	FBCDQS_WP<3>	P2	WDQS	

U_MEM_SD_DDR3_X32_BGA136-GDDR3B
M1 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

32	FBCD<32>	E11	DQ0	
33	FBCD<33>	F11	DQ1	
34	FBCD<34>	F10	DQ2	
35	FBCD<35>	G10	DQ3	
36	FBCD<36>	B11	DQ4	
37	FBCD<37>	C10	DQ5	
38	FBCD<38>	C11	DQ6	
39	FBCD<39>	B10	DQ7	
	FBCDQM<4>	E10	DQM	
	FBCDQS_RN<4>	D10	RDQS	
	FBCDQS_WP<4>	D11	WDQS	

U_MEM_SD_DDR3_X32_BGA136-GDDR3B
M2 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

40	FBCD<40>	E2	DQ0	
41	FBCD<41>	F2	DQ1	
42	FBCD<42>	B3	DQ2	
43	FBCD<43>	F3	DQ3	
44	FBCD<44>	F2	DQ4	
45	FBCD<45>	C3	DQ5	
46	FBCD<46>	C2	DQ6	
47	FBCD<47>	G3	DQ7	
	FBCDQM<5>	E3	DQM	
	FBCDQS_RN<5>	D3	RDQS	
	FBCDQS_WP<5>	D2	WDQS	

U_MEM_SD_DDR3_X32_BGA136-GDDR3B
M2 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

48	FBCD<48>	T10	DQ0	
49	FBCD<49>	T11	DQ1	
50	FBCD<50>	M11	DQ2	
51	FBCD<51>	R11	DQ3	
52	FBCD<52>	N11	DQ4	
53	FBCD<53>	R10	DQ5	
54	FBCD<54>	L10	DQ6	
55	FBCD<55>	M10	DQ7	
	FBCDQM<6>	N10	DQM	
	FBCDQS_RN<6>	P10	RDQS	
	FBCDQS_WP<6>	P11	WDQS	

U_MEM_SD_DDR3_X32_BGA136-GDDR3B
M2 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

56	FBCD<56>	N2	DQ0	
57	FBCD<57>	M2	DQ1	
58	FBCD<58>	L3	DQ2	
59	FBCD<59>	M3	DQ3	
60	FBCD<60>	R2	DQ4	
61	FBCD<61>	R3	DQ5	
62	FBCD<62>	T2	DQ6	
63	FBCD<63>	T3	DQ7	
	FBCDQM<7>	N3	DQM	
	FBCDQS_RN<7>	P3	RDQS	
	FBCDQS_WP<7>	P2	WDQS	

Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!

FBC_CMD<26..0>

2	FBC_CMD<2>	120 COMMON 5% 0402	R599
0	FBC_CMD<0>	120 COMMON 5% 0402	R597
24	FBC_CMD<24>	120 COMMON 5% 0402	R590
22	FBC_CMD<22>	120 COMMON 5% 0402	R594
13	FBC_CMD<13>	120 COMMON 5% 0402	R565
4	FBC_CMD<4>	120 COMMON 5% 0402	R566
5	FBC_CMD<5>	120 COMMON 5% 0402	R567
6	FBC_CMD<6>	120 COMMON 5% 0402	R568
	FBC_CLK0	121 COMMON 1% 0402	R600 → FBC_CLK0_PU
	FBC_CLK0*	121 COMMON 1% 0402	R596
	FBC_CLK1	121 COMMON 1% 0402	R570 → FBC_CLK1_PU
	FBC_CLK1*	121 COMMON 1% 0402	R569

G73 - STUFF 0.01uf CAPS
NV43 - STUFF 0 OHM PUs

R598 80.6 1% 0402 NO STUFF
R571 80.6 1% 0402 NO STUFF
C_0402-01UFX7R1063VNAB
C804 .01UF 6.3V 10% X7R 0402 COMMON
C644 .01UF 6.3V 10% X7R 0402 COMMON

FBVDDQ
GND

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBC 8MX32 DDR3 MEMORIES, FBC CMD BUS PU'S, FBC CLK TERMS

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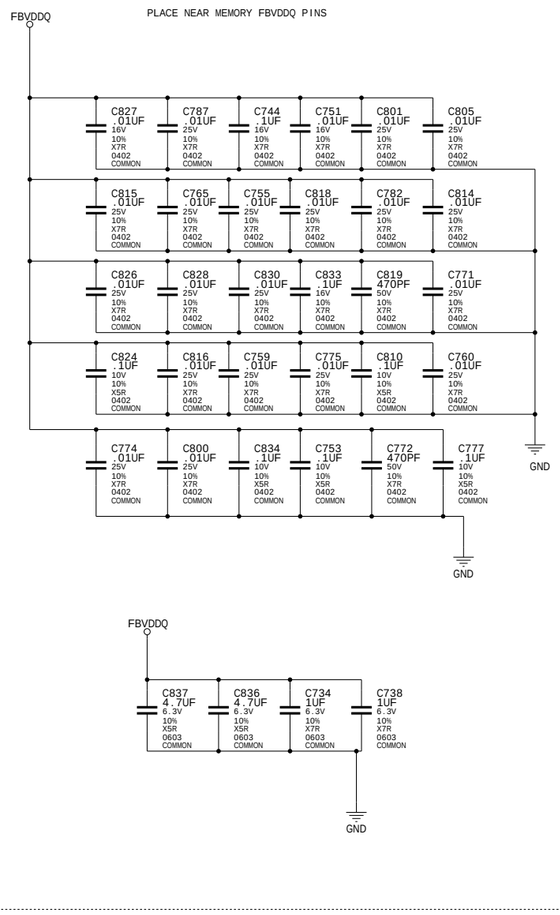
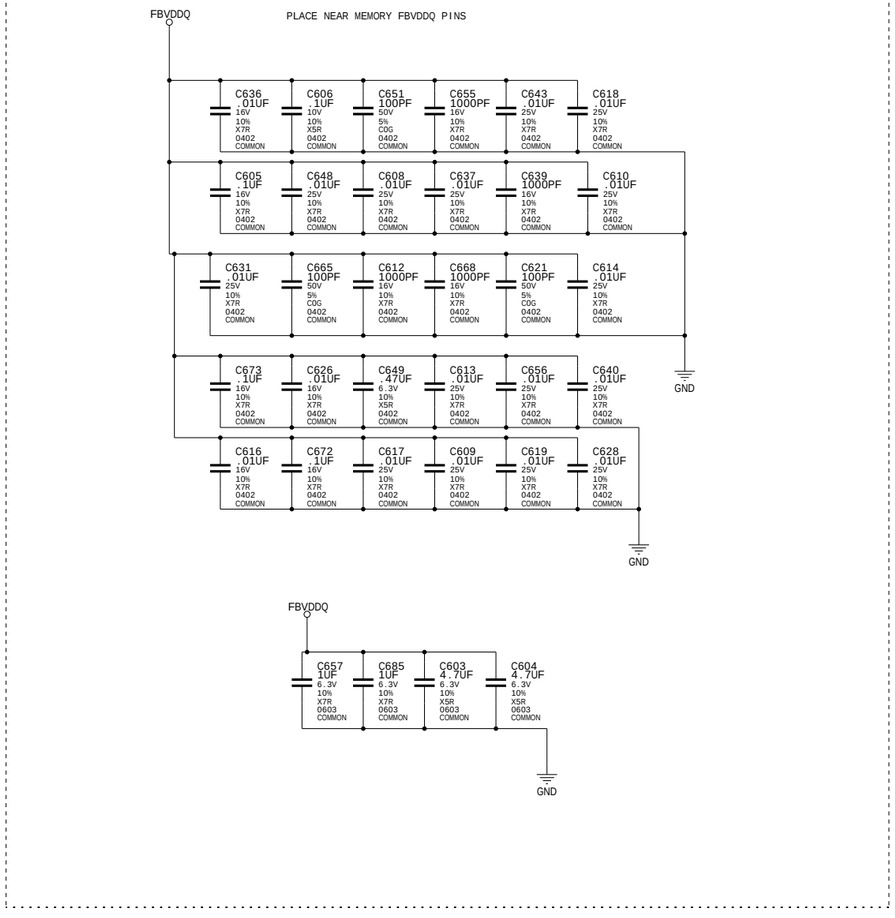
FRAMEBUFFER: PARTITION C DECOUPLING

Decoupling for FBC 0..31



Decoupling for FBC 32..63



U_GPU_G3_128_8X_BGA820-G84-300B

G1
G84-300-A1
BGA820
COMMON

14/14 _GND_

AA12	GND	GND	K10
AA2	GND	GND	K23
AA21	GND	GND	K29
AA31	GND	GND	K4
AB27	GND	GND	L27
AB6	GND	GND	L6
AC10	GND	GND	M12
AC23	GND	GND	M2
AC29	GND	GND	M31
AC4	GND	GND	N15
AD16	GND	GND	N18
AD17	GND	GND	N29
AD2	GND	GND	N4
AD31	GND	GND	P15
AE17	GND	GND	P18
AE27	GND	GND	P27
AE6	GND	GND	P6
AF11	GND	GND	R13
AF26	GND	GND	R14
AF29	GND	GND	R15
AF4	GND	GND	R18
AF7	GND	GND	R19
AG10	GND	GND	R2
AG11	GND	GND	R20
AG14	GND	GND	R31
AG15	GND	GND	T16
AG19	GND	GND	T17
AG2	GND	GND	T24
AG22	GND	GND	T29
AG31	GND	GND	T4
AG8	GND	GND	U16
AH24	GND	GND	U17
AJ10	GND	GND	U24
AJ13	GND	GND	U29
AJ16	GND	GND	U8
AJ17	GND	GND	V13
AJ20	GND	GND	V14
AJ23	GND	GND	V15
AJ26	GND	GND	V18
AJ29	GND	GND	V19
AJ4	GND	GND	V2
AJ7	GND	GND	V20
AK2	GND	GND	V31
AK28	GND	GND	W15
AK31	GND	GND	W18
AL11	GND	GND	W27
AL14	GND	GND	W6
AL19	GND	GND	Y15
AL22	GND	GND	Y18
AL25	GND	GND	Y29
AL3	GND	GND	Y4
AL6	GND	GND	AL10
AL9	GND	GND	AM10
AM13	GND	GND	AG13
AM16	GND		
AM17	GND		
AM20	GND		
AM23	GND		
AM26	GND		
AM29	GND		
B12	GND		
B15	GND		
B18	GND		
B21	GND		
B24	GND		
B27	GND		
B3	GND		
B30	GND		
B6	GND		
B9	GND		
C2	GND		
C31	GND		
D10	GND		
D13	GND		
D16	GND		
D17	GND		
D20	GND		
D23	GND		
D26	GND		
D29	GND		
D4	GND		
D7	GND		
F11	GND		
F14	GND		
F19	GND		
F2	GND		
F22	GND		
F25	GND		
F31	GND		
F8	GND		
G26	GND		
G29	GND		
G4	GND		
G7	GND		
H27	GND		
H6	GND		
J16	GND		
J17	GND		
J2	GND		
J31	GND		

GND

GND

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBC MEMORY FBVDD/Q DECOUPLING CAPS, GPU GND CONNECTIONS

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Primary Display (DACA), Slim DB15

DACA RGB-FILTER

NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACA_VDD			12MIL
DACA_VREF			12MIL
DACA_RSET			12MIL
DACA_RED	1	75OHM	
DACA_GREEN	1	75OHM	
DACA_BLUE	1	75OHM	
DACA_RED_C	1	75OHM	
DACA_GREEN_C	1	75OHM	
DACA_BLUE_C	1	75OHM	
DACA_HSYNC	1	50OHM	
DACA_VSYNC	1	50OHM	
AVB	1	50OHM	
AHB	1	50OHM	
DACA_VSYNC_BUF	1	50OHM	
DACA_HSYNC_BUF	1	50OHM	
DACA_VSYNC_C	1	50OHM	
DACA_HSYNC_C	1	50OHM	

Route DAC RGB with ~37.5ohm Impedence

FOR ESD DIODES

Place in output filter section!

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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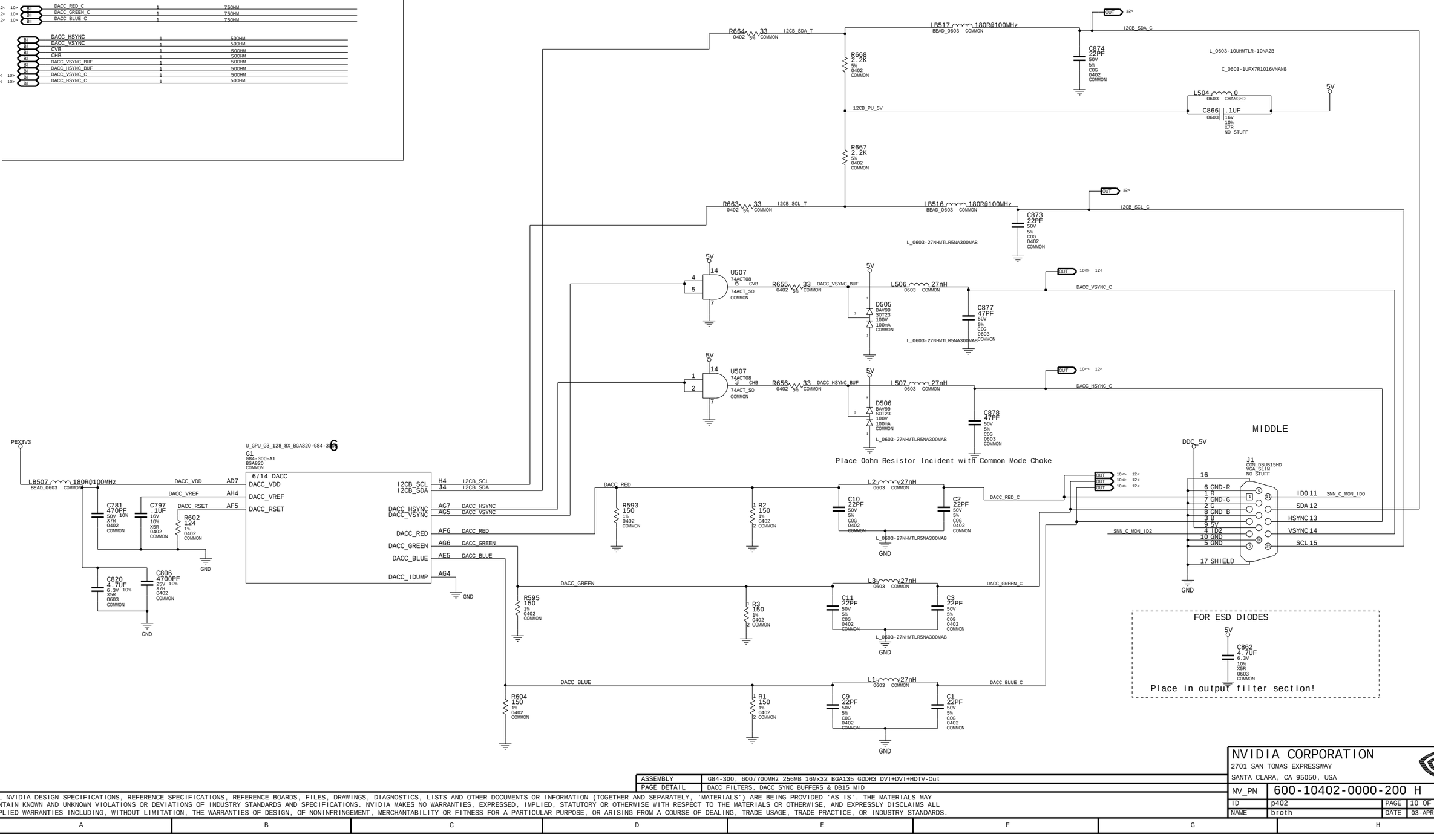
Secondary Display (DACC), Slim DB15

DACC RGB-FILTER

NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACC_VDD			12MIL
DACC_VREF			12MIL
DACC_RSET			12MIL
DACC_RED	1	75OHM	
DACC_GREEN	1	75OHM	
DACC_BLUE	1	75OHM	
DACC_RED_C	1	75OHM	
DACC_GREEN_C	1	75OHM	
DACC_BLUE_C	1	75OHM	
DACC_HSYNC	1	50OHM	
DACC_VSYNC	1	50OHM	
CVB	1	50OHM	
CHB	1	50OHM	
DACC_VSYNC_BUF	1	50OHM	
DACC_HSYNC_BUF	1	50OHM	
DACC_VSYNC_C	1	50OHM	
DACC_HSYNC_C	1	50OHM	



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID

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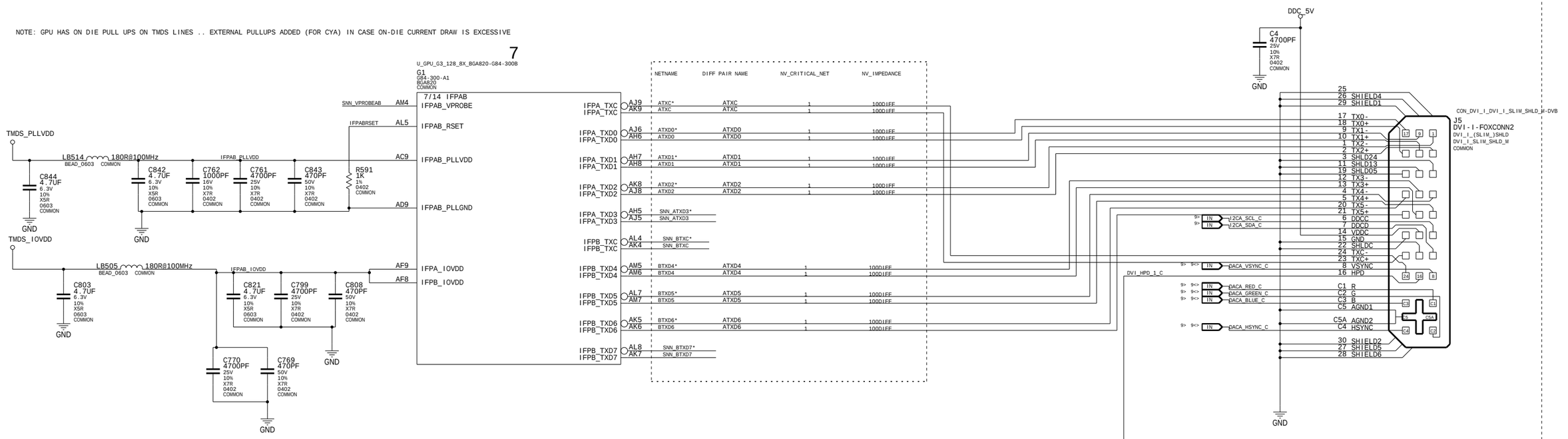
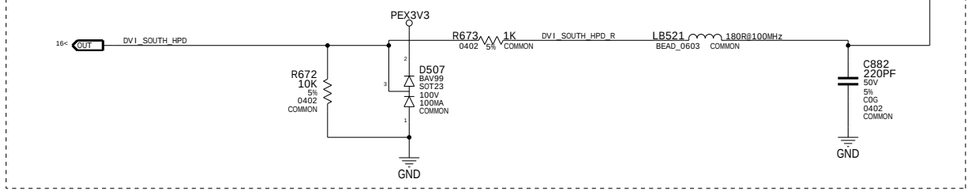
INTERNAL TMDS .. LINK A & B

NOTE: GPU HAS ON DIE PULL UPS ON TMDS LINES .. EXTERNAL PULLUPS ADDED (FOR CYA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE



Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
BI IFPAB_PLLVDD	12MIL	1.8V
TMDS_IOVDD TMDS_IOVDD	12MIL	3.3V
BI IFPAB_IOVDD	12MIL	3.3V
BI IFPABRSET	12MIL	
BI TMDS_IOBACK	12MIL	

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	TMDS LINK A/B & PU's, TMDS IO BACKDRIVE PREVENTION,DVI CONNECTOR SOUTH

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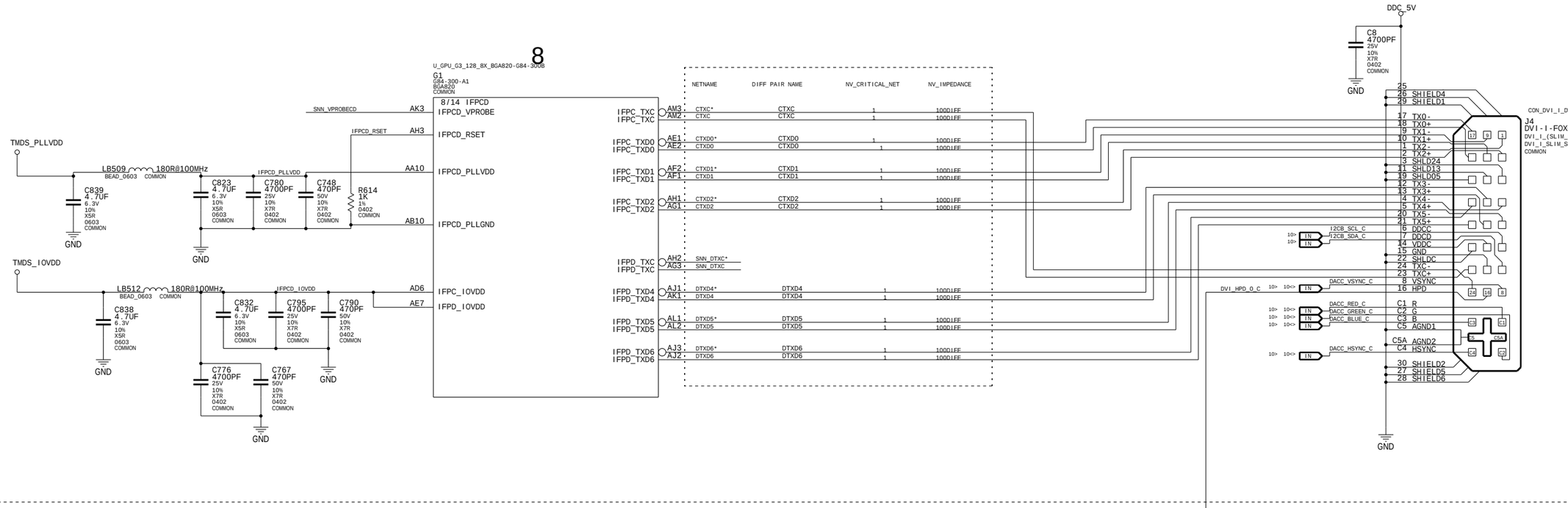
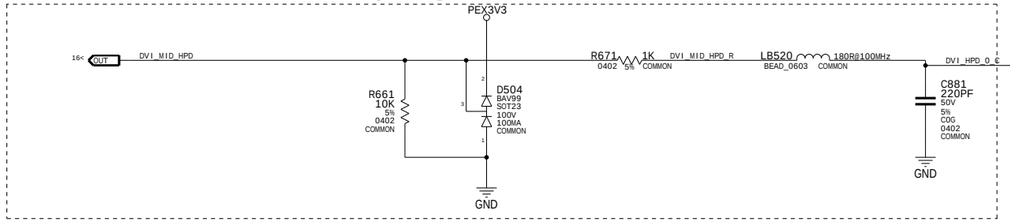
INTERNAL TMDS .. LINK C & D



Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
IFPCD_RSET	12MIL	
IFPCD_PLLVDD	12MIL	1.8V
IFPCD_IOVDD	12MIL	3.3V

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	TMDS LINK C/D & PU's,DVI CONNECTOR MID

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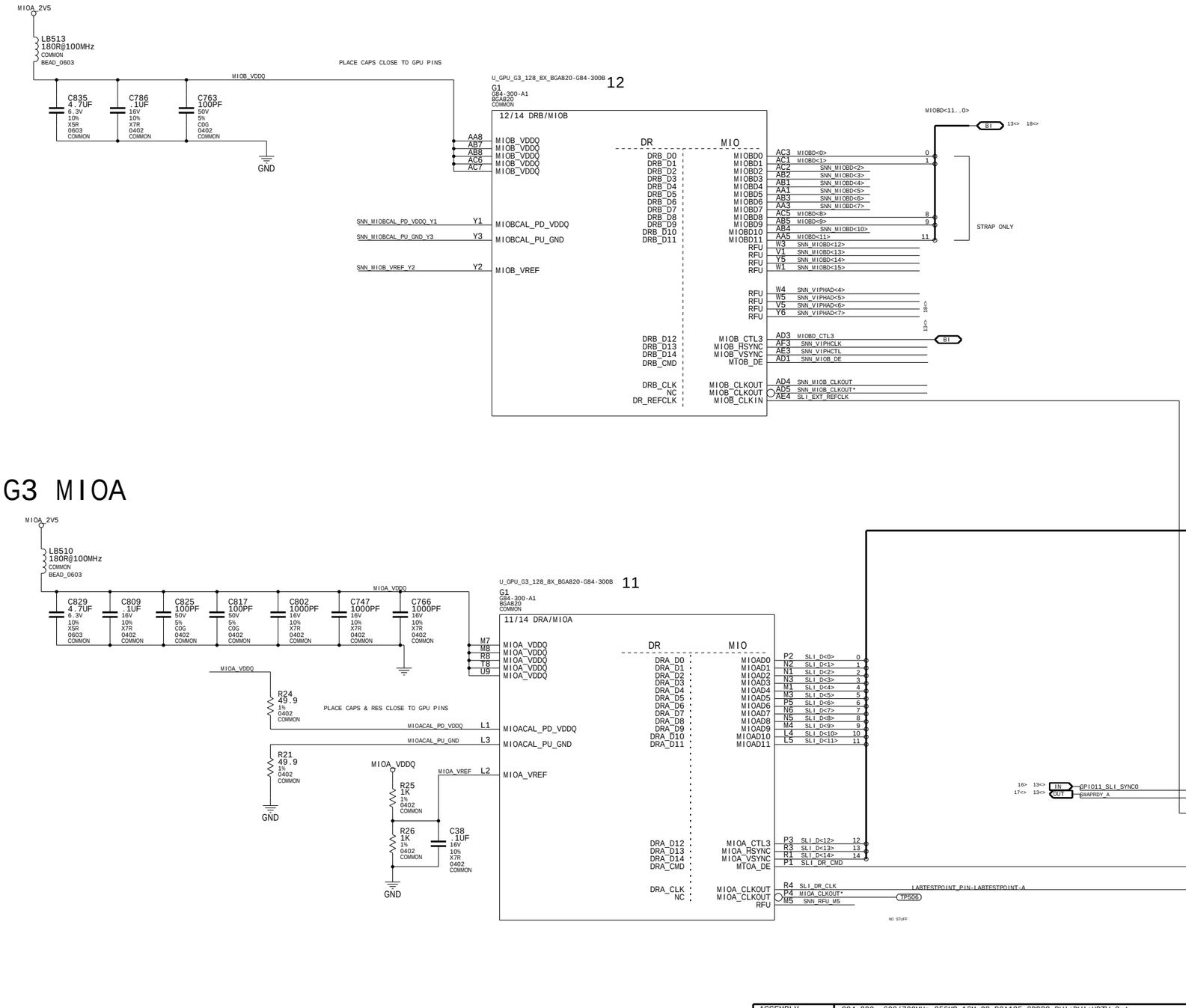
G3 VIP/MIOB



NETNAME	NV_CRITICAL_NET	NV_IMPEDANCE
18<> 13<> BI SLI_D<14..0>	2	50OHM
BI SLI_DR_CMD	2	50OHM
BI SLI_DR_CLK	2	50OHM
BI SLI_EXT_REFCLK	2	50OHM
BI MIOA_CLKOUT	2	50OHM
16> 13< BI GPIO11_SLI_SYNCO	2	50OHM
17<> 13> BI SWAPRDY_A	2	50OHM

NETNAME	MIN_LINE_WIDTH	
18<> 13<> BI MIOBD<7..0>	2	50OHM
MIOB_VDDQ	12MIL	
BI MIOB_VREF	12MIL	
18<> 13<> BI MIOBD_CTL3	12MIL	
MIOA_VDDQ	12MIL	
BI MIOA_VREF	12MIL	

G3 MIOA

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	MIOA & MIOB, SLI CONNECTOR

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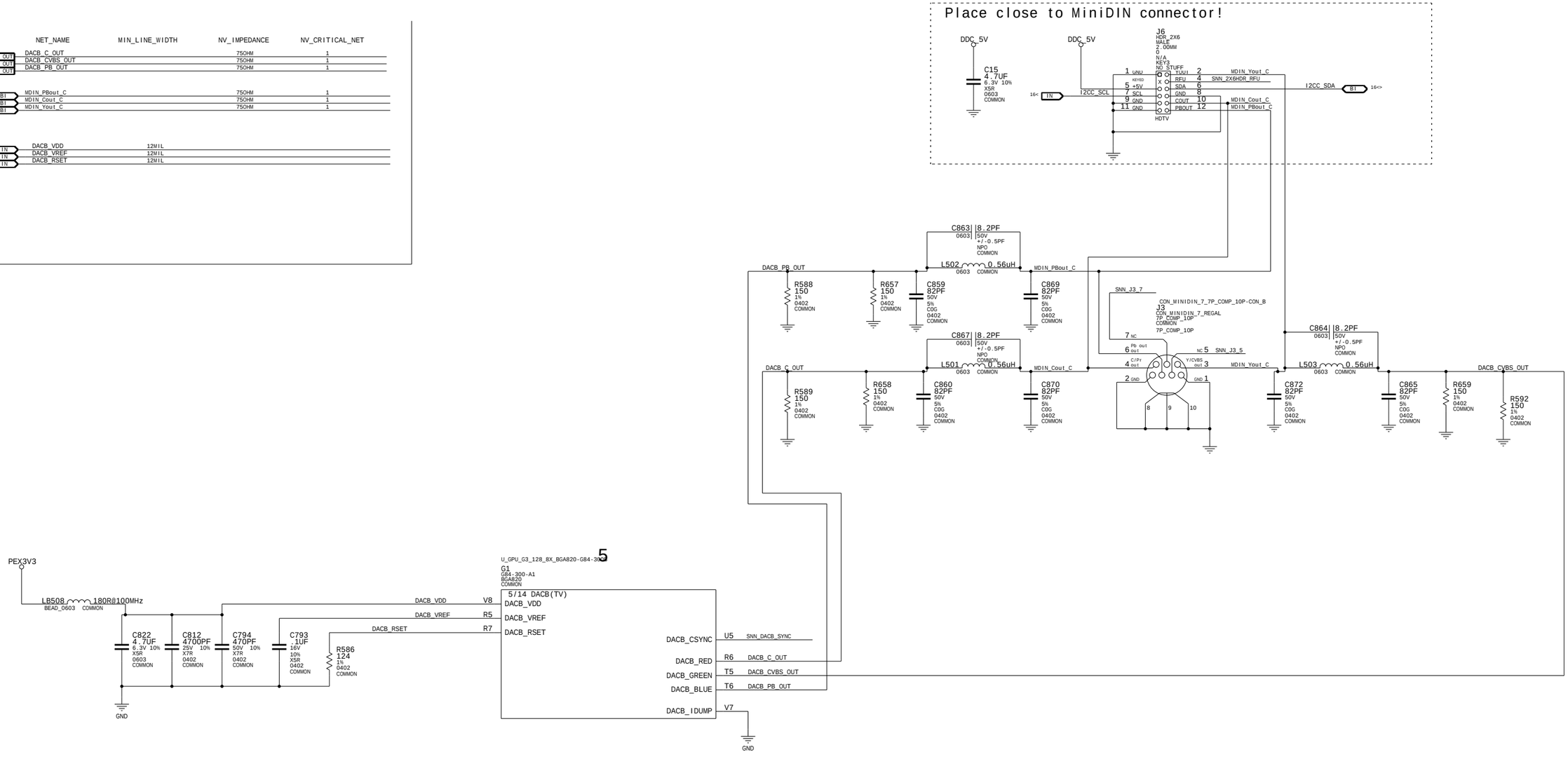
DACB .. MiniDIN VIDEO OUT CONNECTOR

	NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
OUT	DACB_C_OUT		75OHM	1
OUT	DACB_CVBS_OUT		75OHM	1
OUT	DACB_PB_OUT		75OHM	1
BI	MDIN_PBout_C		75OHM	1
BI	MDIN_Cout_C		75OHM	1
BI	MDIN_Yout_C		75OHM	1
IN	DACB_VDD	12MIL		
IN	DACB_VREF	12MIL		
IN	DACB_RSET	12MIL		



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	DACB FILTERS, MINIDIN CONNECTOR NORTH, COMPONENT VIDEO OUTPUT CONNECTOR

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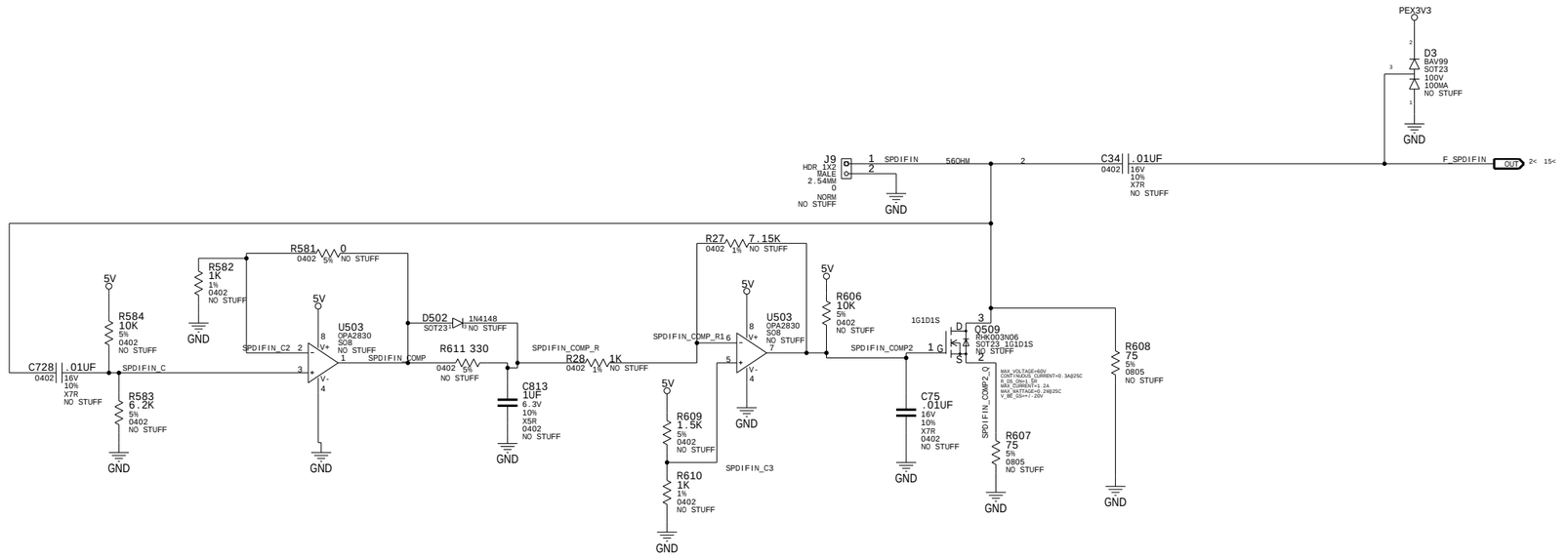
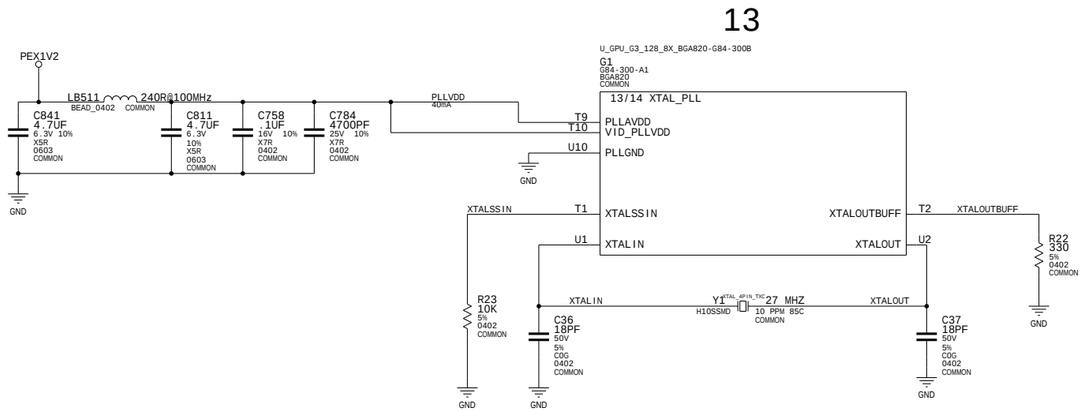
XTAL/PLLVDD/SPDIF IN

SPDIF IN



XTAL/PLLVDD



NETNAME		MIN_LINE_WIDTH	
XTALIN	IN	10MIL	
XTALOUT	IN	10MIL	
PLLVDD_R	IN	12MIL	
PLLVDD	IN	12MIL	
VID_PLLVDD	IN	12MIL	
XTALSSIN	IN	10MIL	
XTALOUTBUFF	IN	10MIL	
SPDIFIN	IN	560HM	2
SPDIFIN_C	IN	560HM	2
SPDIFIN_C2	IN	560HM	2
SPDIFIN_COMP	IN	560HM	2
SPDIFIN_COMP_R	IN	560HM	2
SPDIFIN_COMP_R1	IN	560HM	2
SPDIFIN_C3	IN	560HM	2
SPDIFIN_COMP2	IN	560HM	2
SPDIFIN_COMP2_Q	IN	560HM	2
F_SPDIFIN	IN	560HM	2

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	SPDIF-IN HEADER, XTAL

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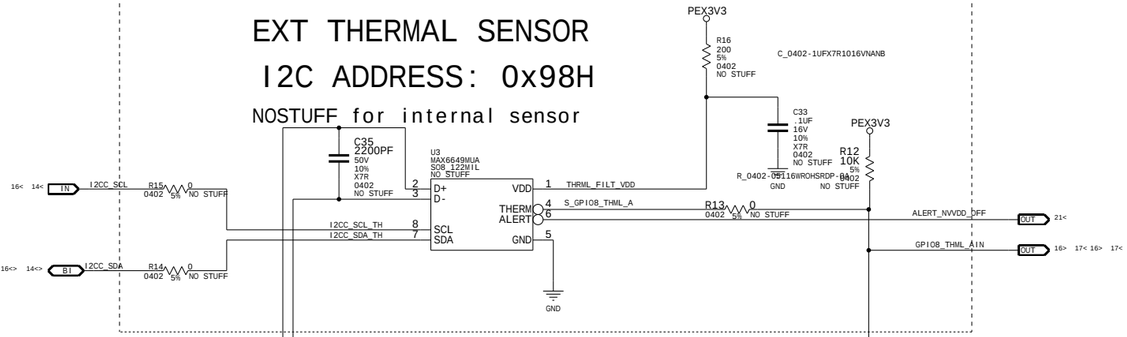
NETNAME	MIN_LINE_WIDTH	VOLTAGE
THERMDC	10MIL	
THERMDA	10MIL	
FAN_PWM	12MIL	
FAN_PWM_B	12MIL	
FAN_PWM_C	12MIL	
FAN_PWM_D	12MIL	

EXT THERMAL SENSOR

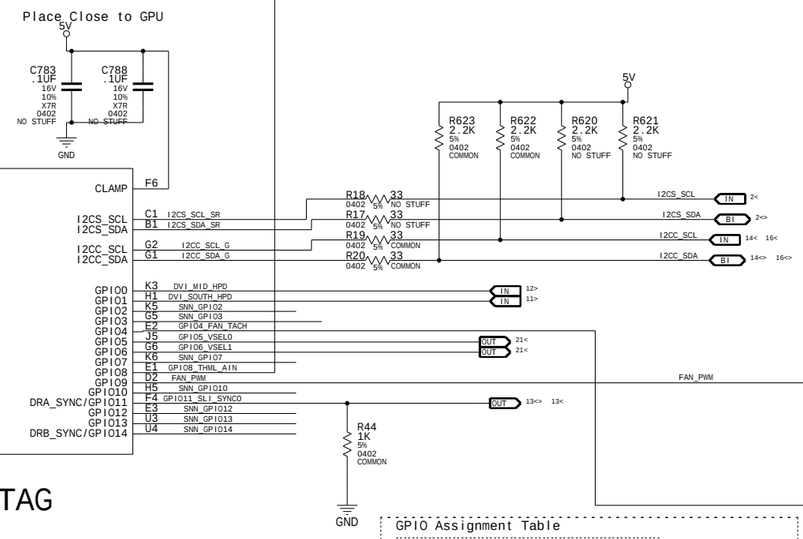
I2C ADDRESS: 0x98H

NOSTUFF for internal sensor

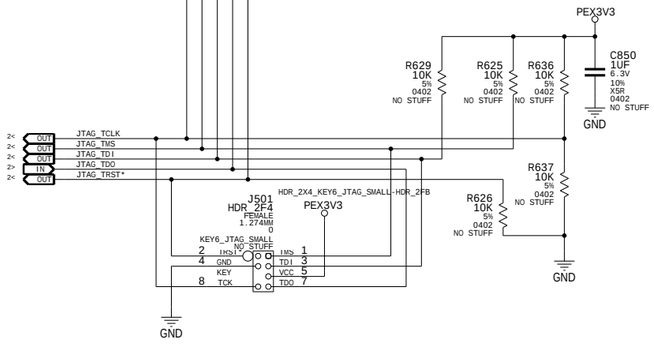


Use 10MIL Guard(GND) Trace around THERMDC and THERMDA

Place Close to GPU

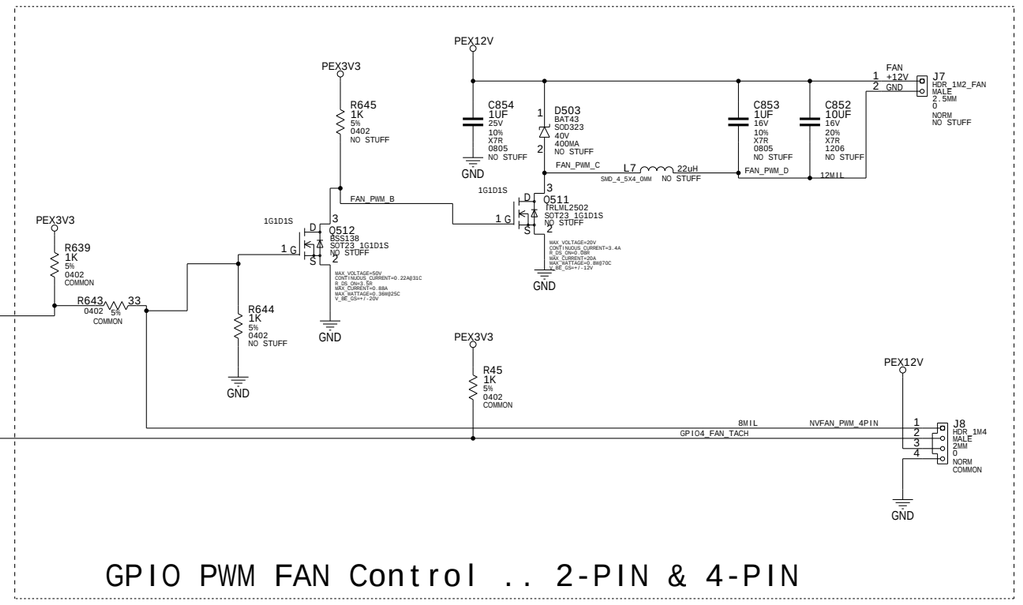


GPIO & JTAG



GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	DVI SOUTH HOTPLUG DET
2	IN/OUT	RESERVED
3	IN	G84 THERMAL ODS IN
4	IN	FAN_TACH
5	OUT	NVVDD VOLTAGE SELECT 0
6	OUT	NVVDD VOLTAGE SELECT 1
7	OUT	RESERVED
8	IN	THERMAL ALERT IN
9	OUT	PWM FAN
10	OUT	RESERVED
11	OUT	SLI SYNC0
12	OUT	RESERVED
13	IN	RESERVED
14	IN	RESERVED



GPIO PWM FAN Control .. 2-PIN & 4-PIN

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	EXTERNAL THERMAL SENSOR, 2PIN / 4PIN FAN CONTROL, GPIO

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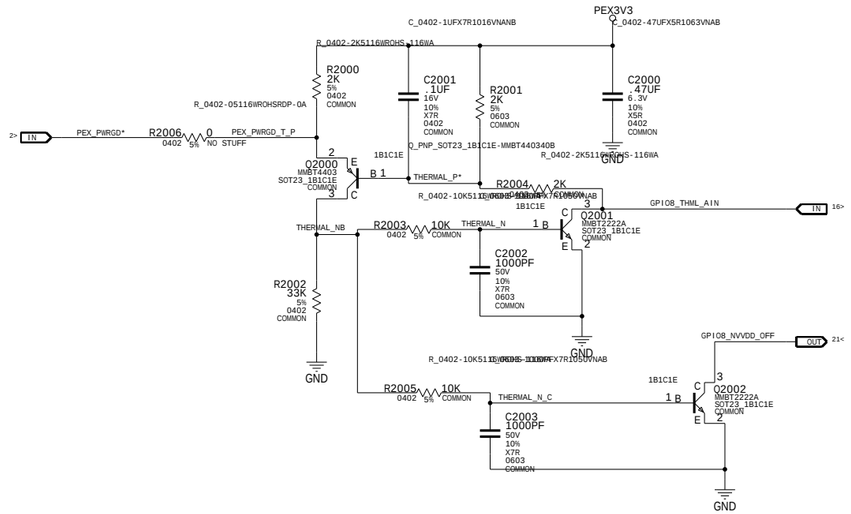
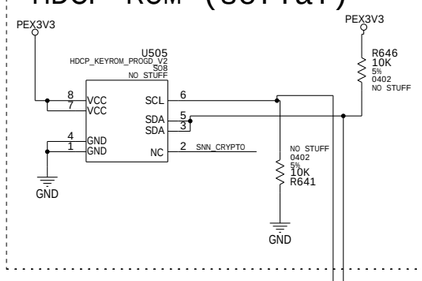
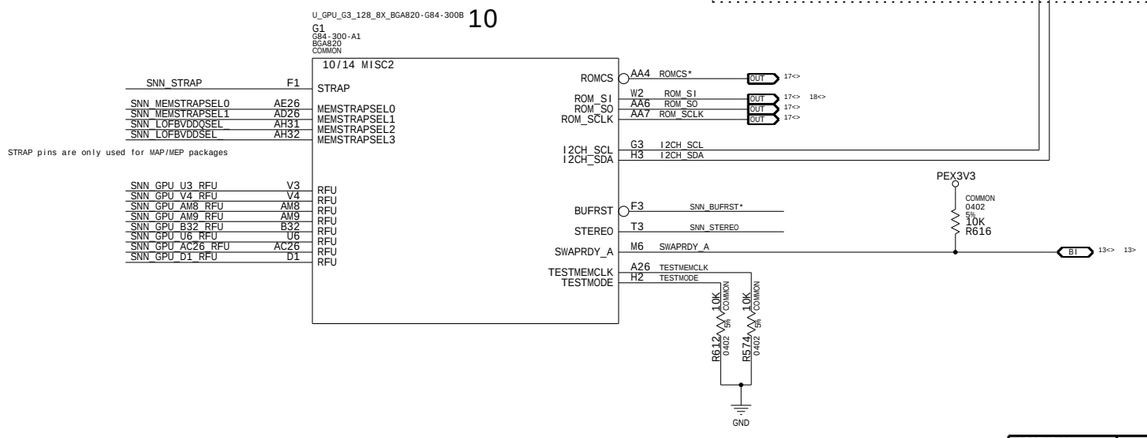
Thermal Protection

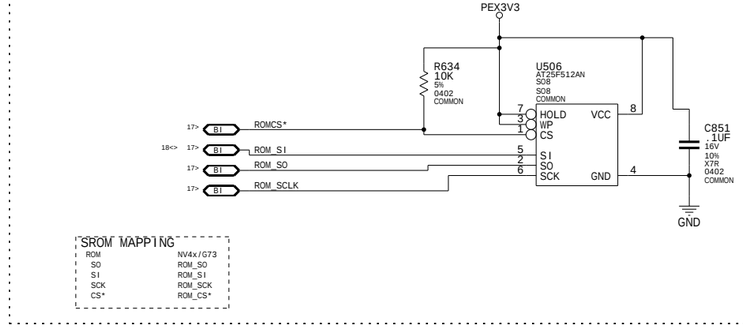


HDCP ROM (serial)





BIOS ROM(serial)



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	BIOS ROM, HDCP ROM

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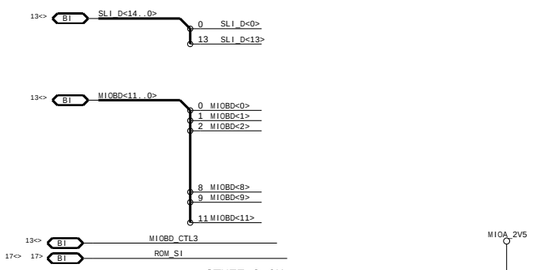
BIOS, Straps, Misc

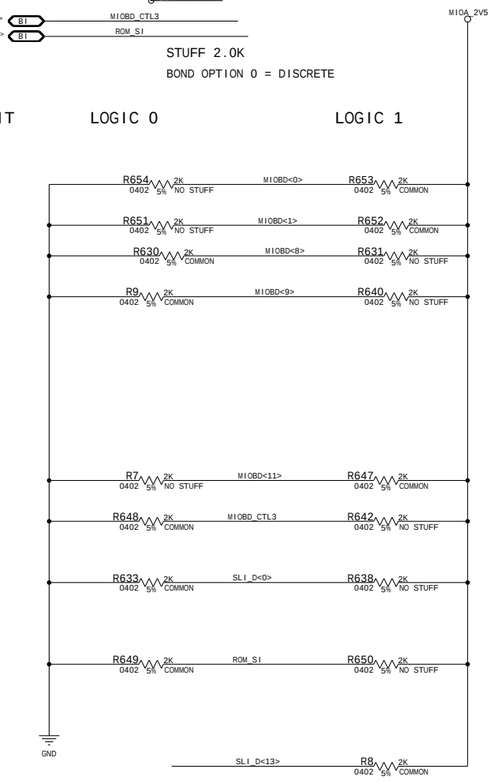
STRAPS

Assembly: BIOS

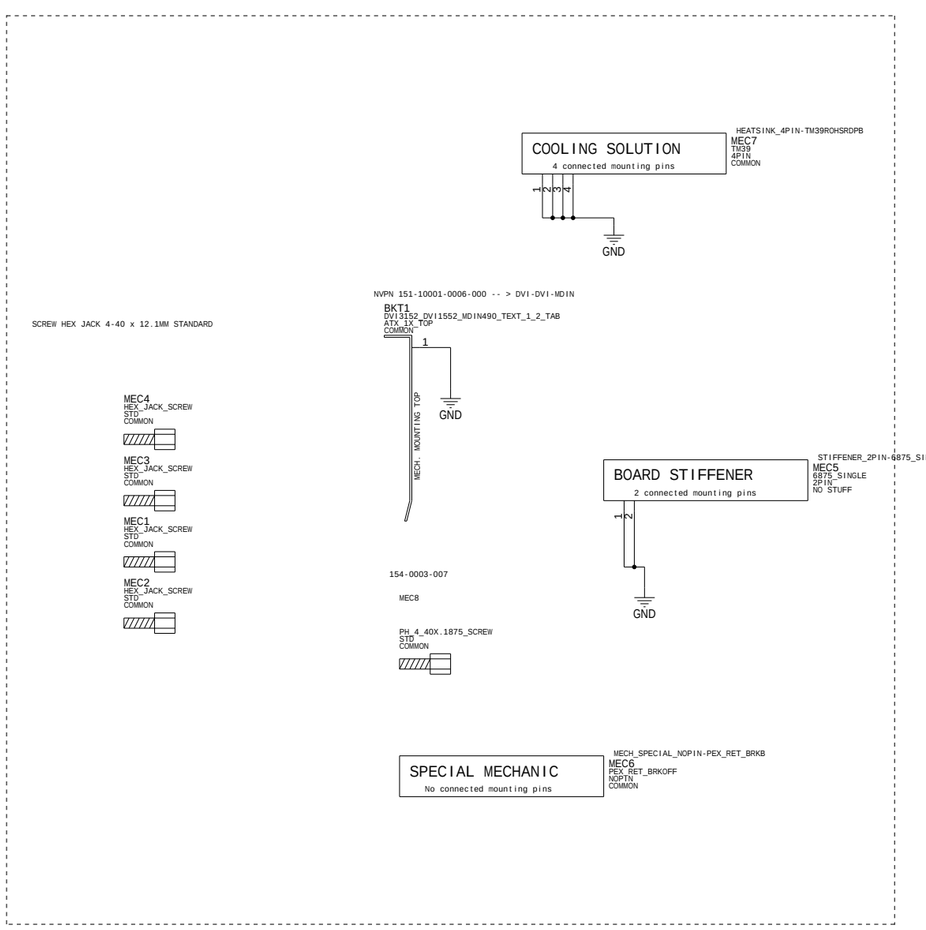


STUFF 2.0K

BOND OPTION 0 = DISCRETE



MECHANICALS & THERMALS



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	BIOS STRAPS & MECHANICALS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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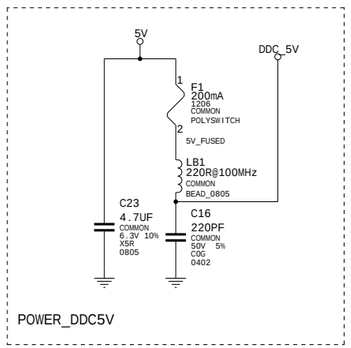
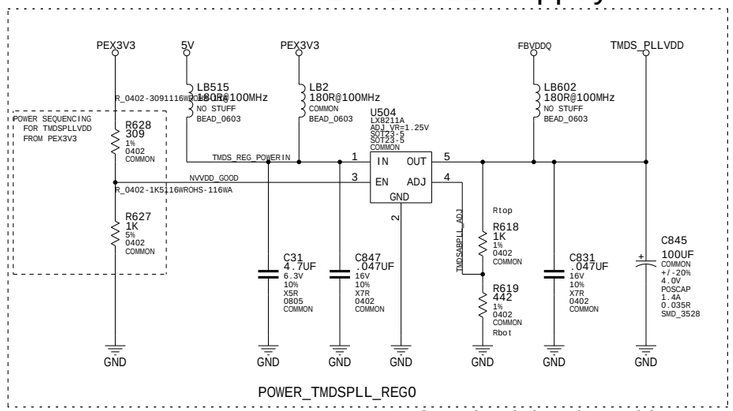
Power Supply ... TMDS, MIOA_VDDQ, DDC5V

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	1A	12MIL	5V
DDC_5V		12MIL	5V
5V	1A		5V
TMDSABPLL_ADJ		10MIL	3.3V
TMDS_PLLVDD		12MIL	1.8V
MIOA_2V5	1A	12MIL	2.5V
GND		16MIL	0V

DDC 5V

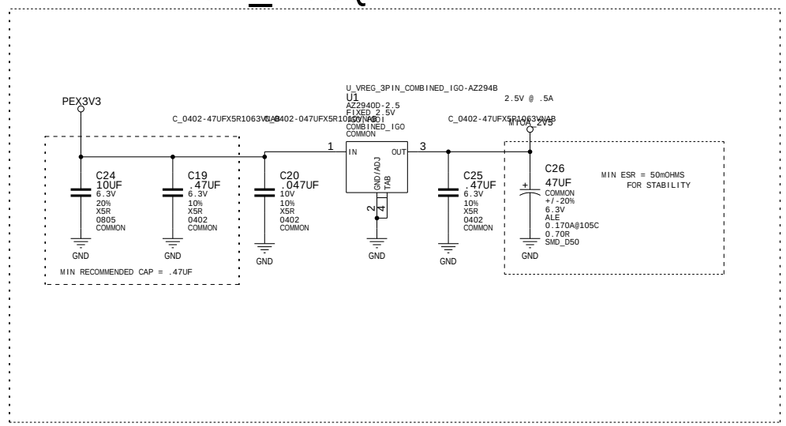


TMDS AB/CD PLL Supply



Vout = VRef * (1+(Rbot/Rtop))
1.8V = 1.25V * (1+(442/1000))

MIOA_VDDQ



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	POWER SUPPLY LINEARS: DDC5V, TMDS PLLVDD, DACB VDD, MIOA_VDDQ

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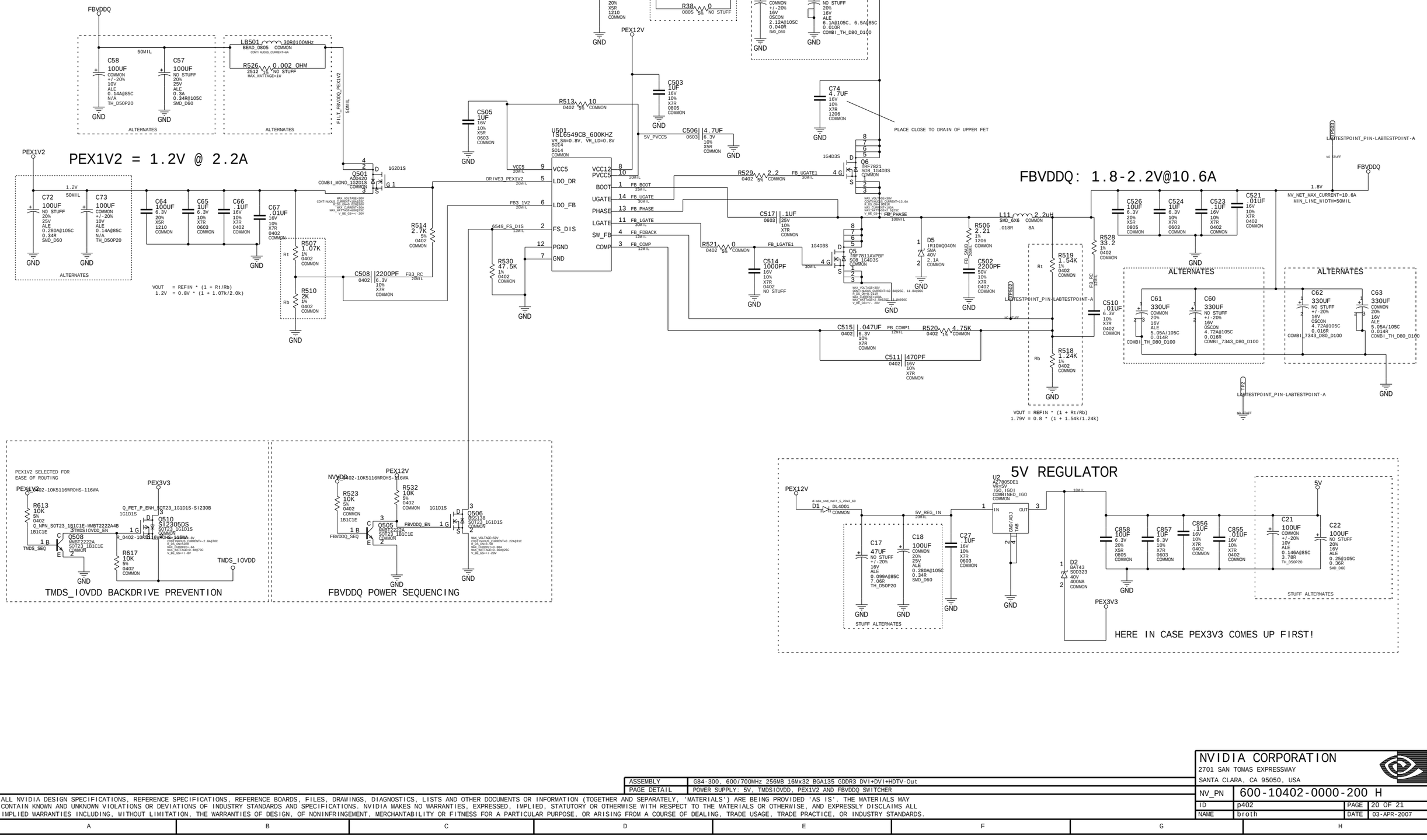
POWER SUPPLY .. FBVDDQ, PEX1V2



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	POWER SUPPLY: 5V, TMDSIOVDD, PEX1V2 AND FBVDDQ SWITCHER

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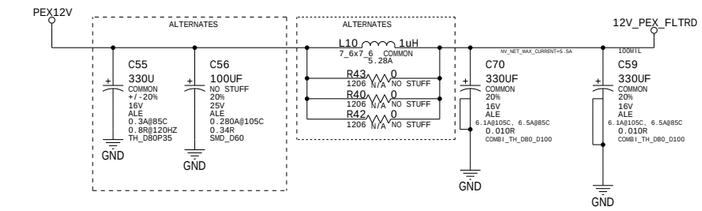
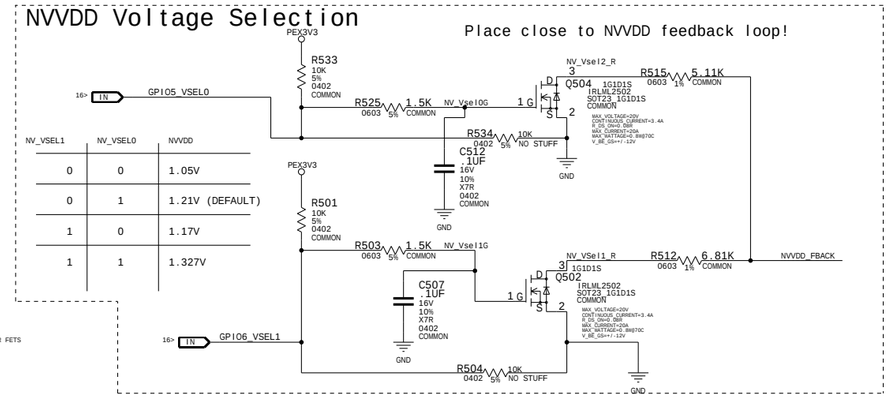
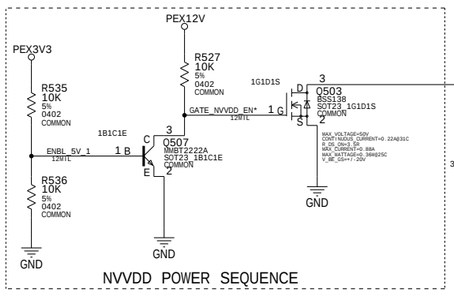
NVVDD POWER SUPPLY







ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	POWER SUPPLY: SINGLE PHASE NVVDD, NVVDD SET CONTROL

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