Title	Schematic No.	Date:
RH LP RV710 DDR3 VGA (header) TVO DVI	105-B754XX-00	Monday, July 14, 2008

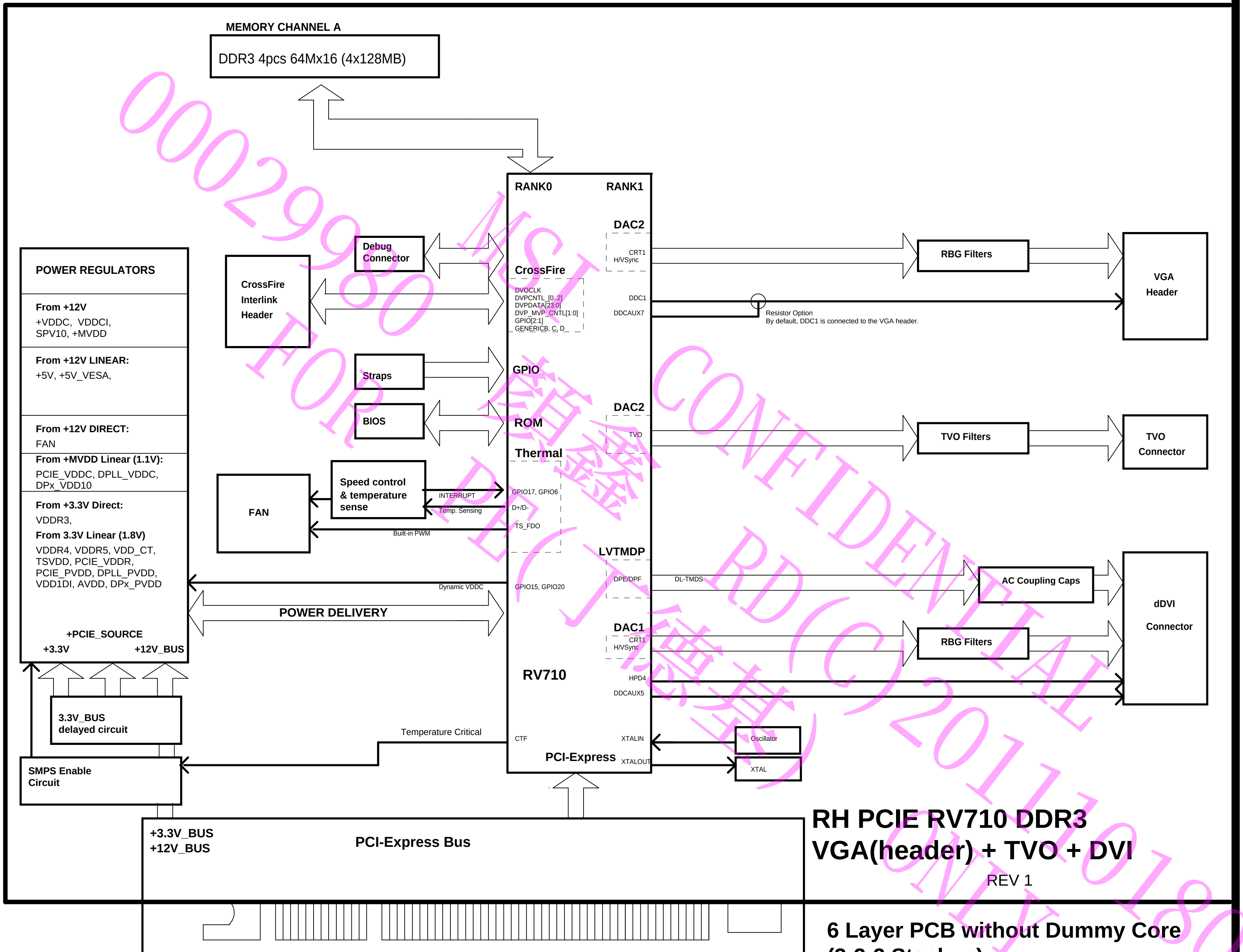
REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 1

RV710 CUSTOM

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
01	00A	2008.06.06	INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.
01	00B	2008.06.25	Based on -00A PCB - removed BB - changed PERST cct - changed DDC pull-ups - changed R861 to 1202 package - added net names to schematic - added more VDDC_Source stitching caps



RH PCIE RV710 DDR3 VGA(header) + TVO + DVI

REV 1

6 Layer PCB without Dummy Core (2-2-2 Stackup)

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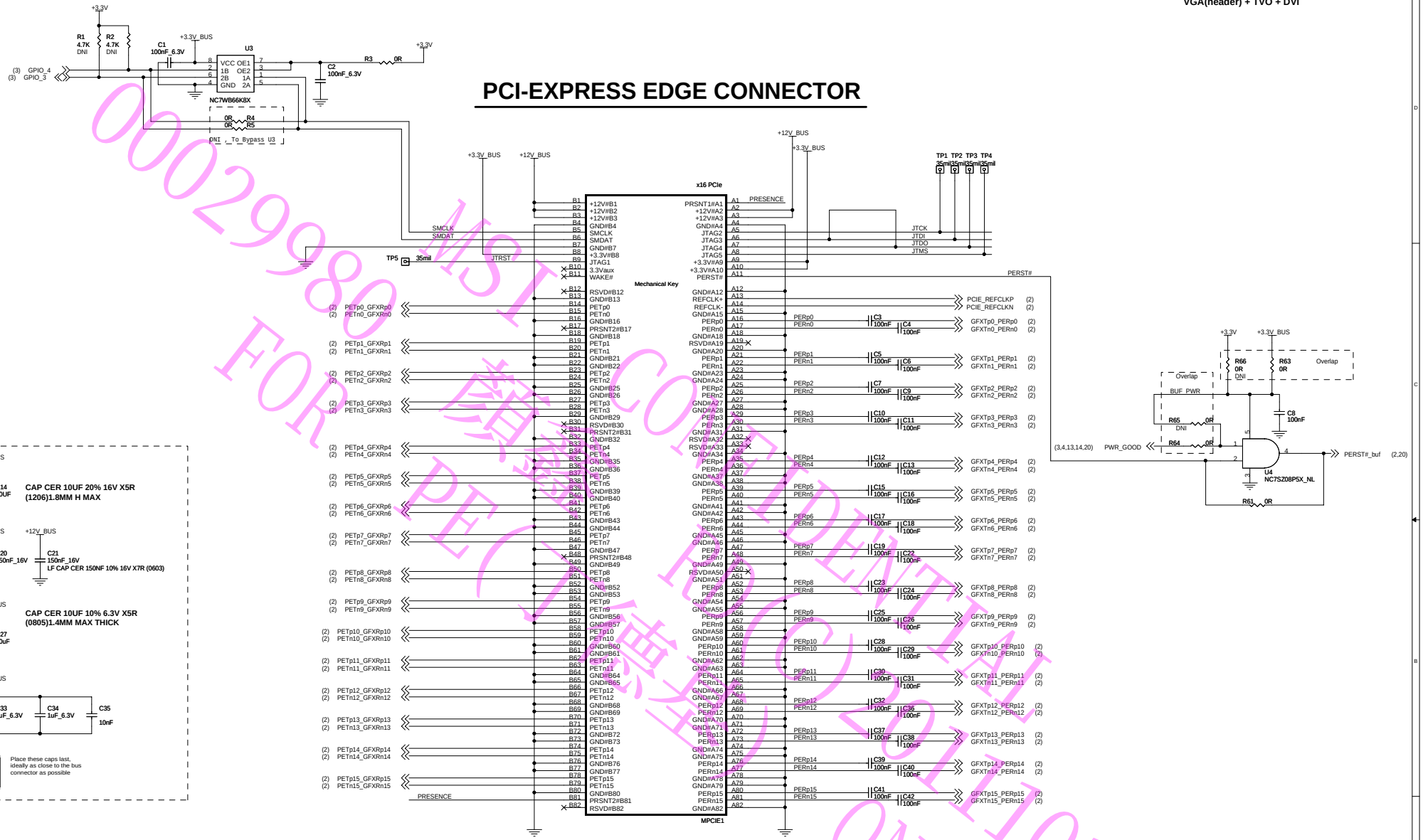
PCI-EXPRESS EDGE CONNECTOR



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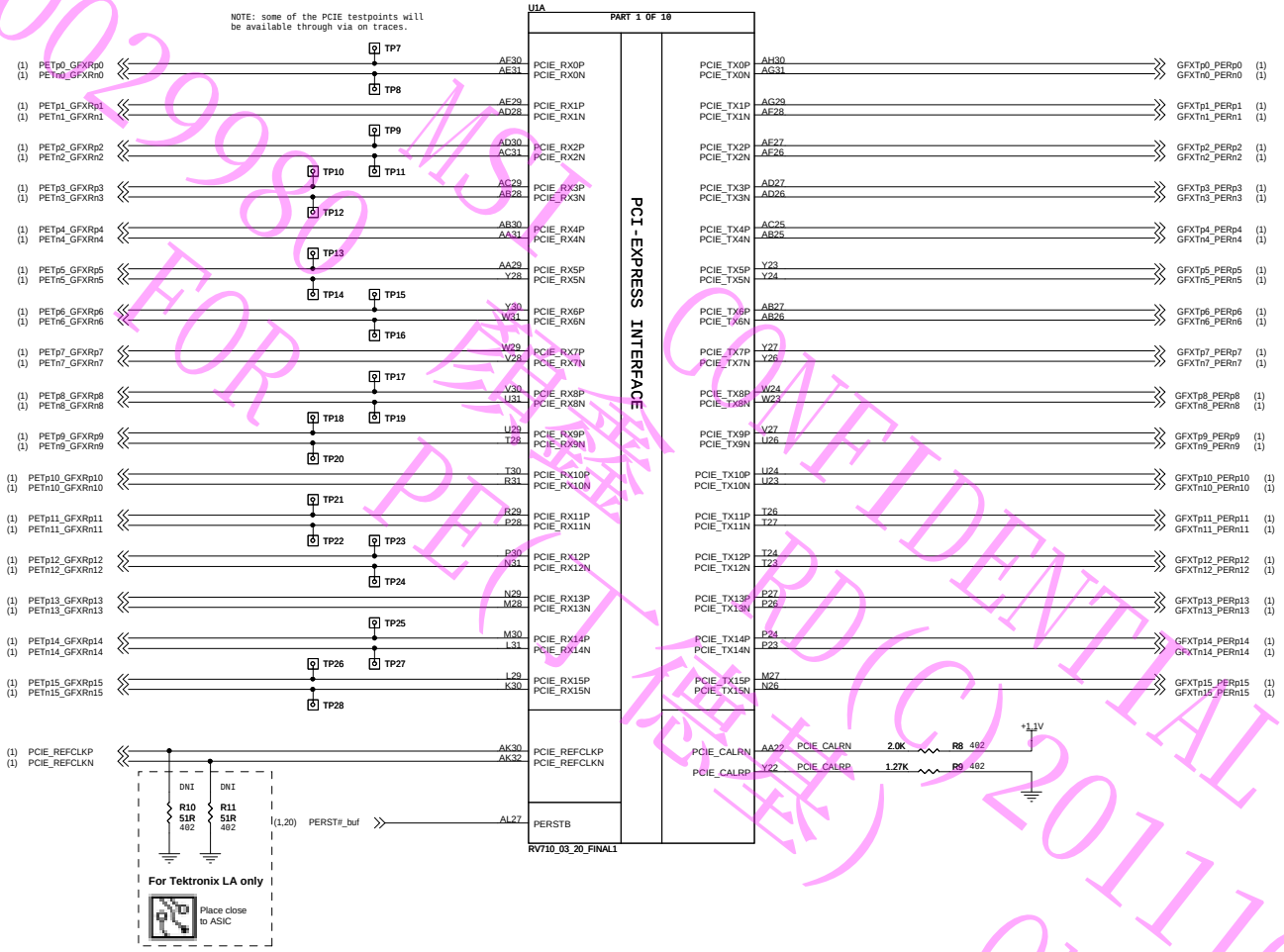

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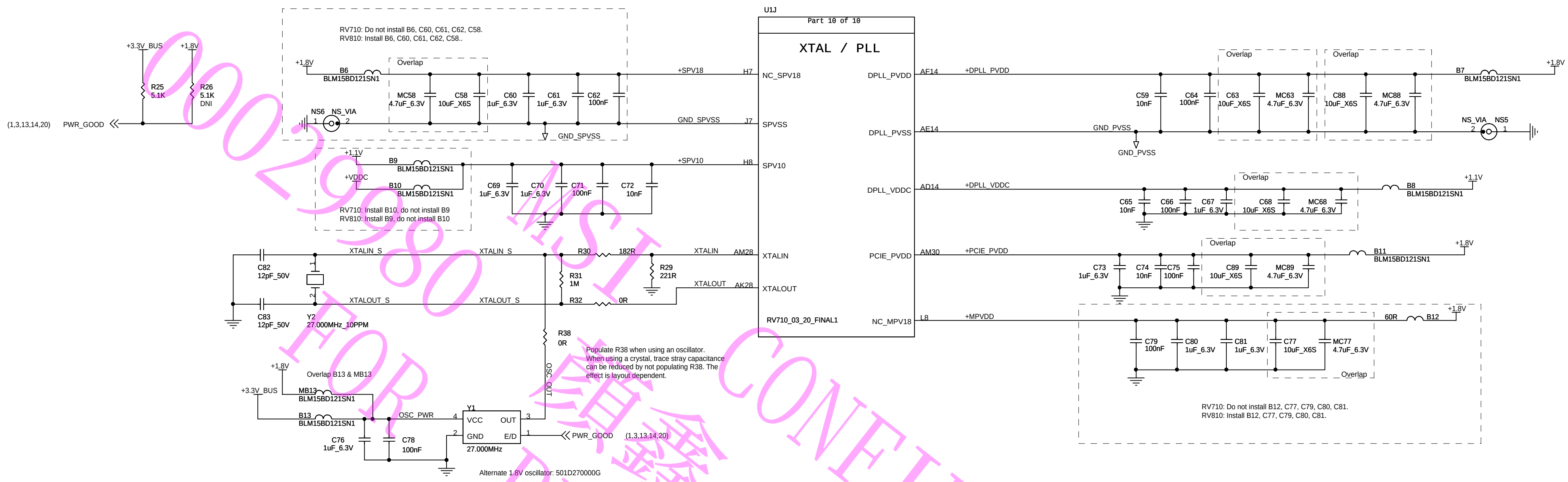
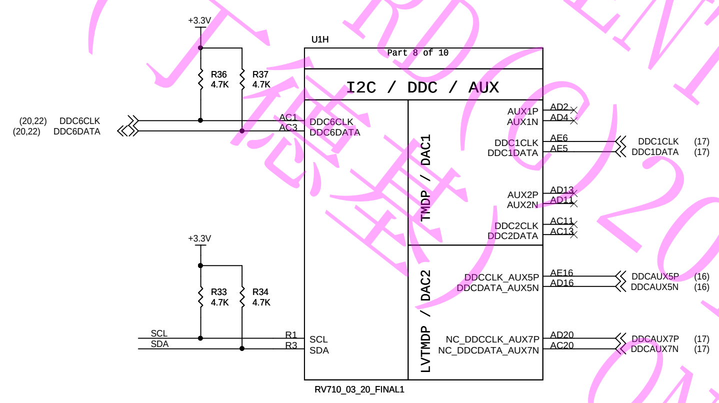


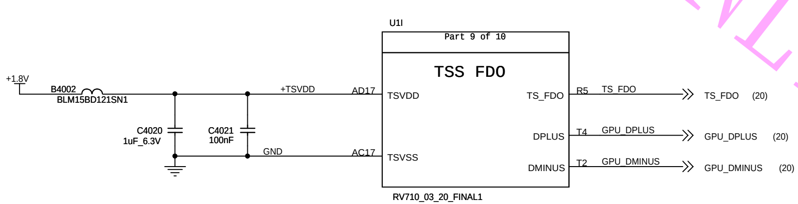


DDC6 BUS:

I2C Address	Function	Device
0x90	I2C VDDC Control	DS4402
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A



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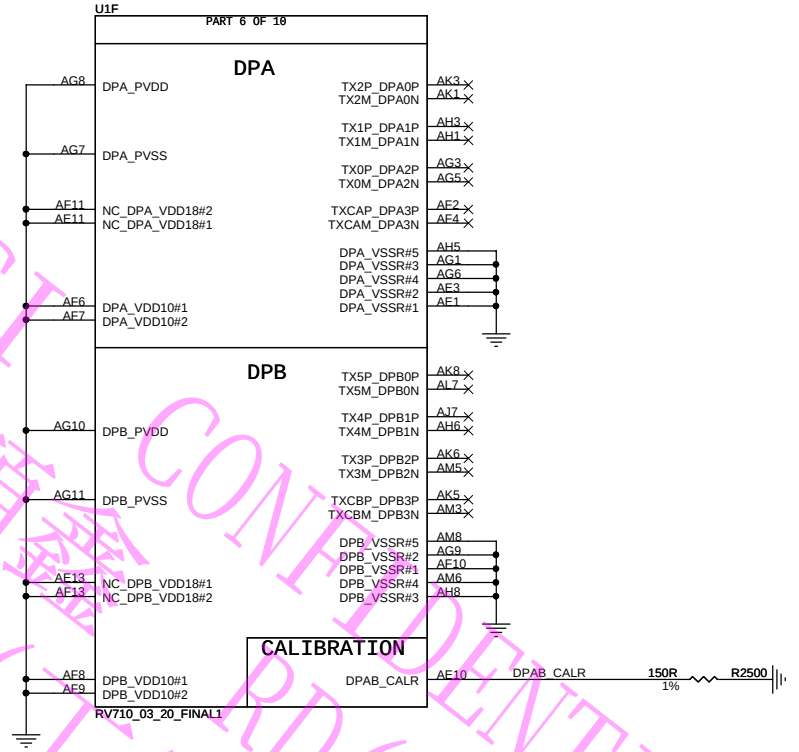
TMDP INTERFACE



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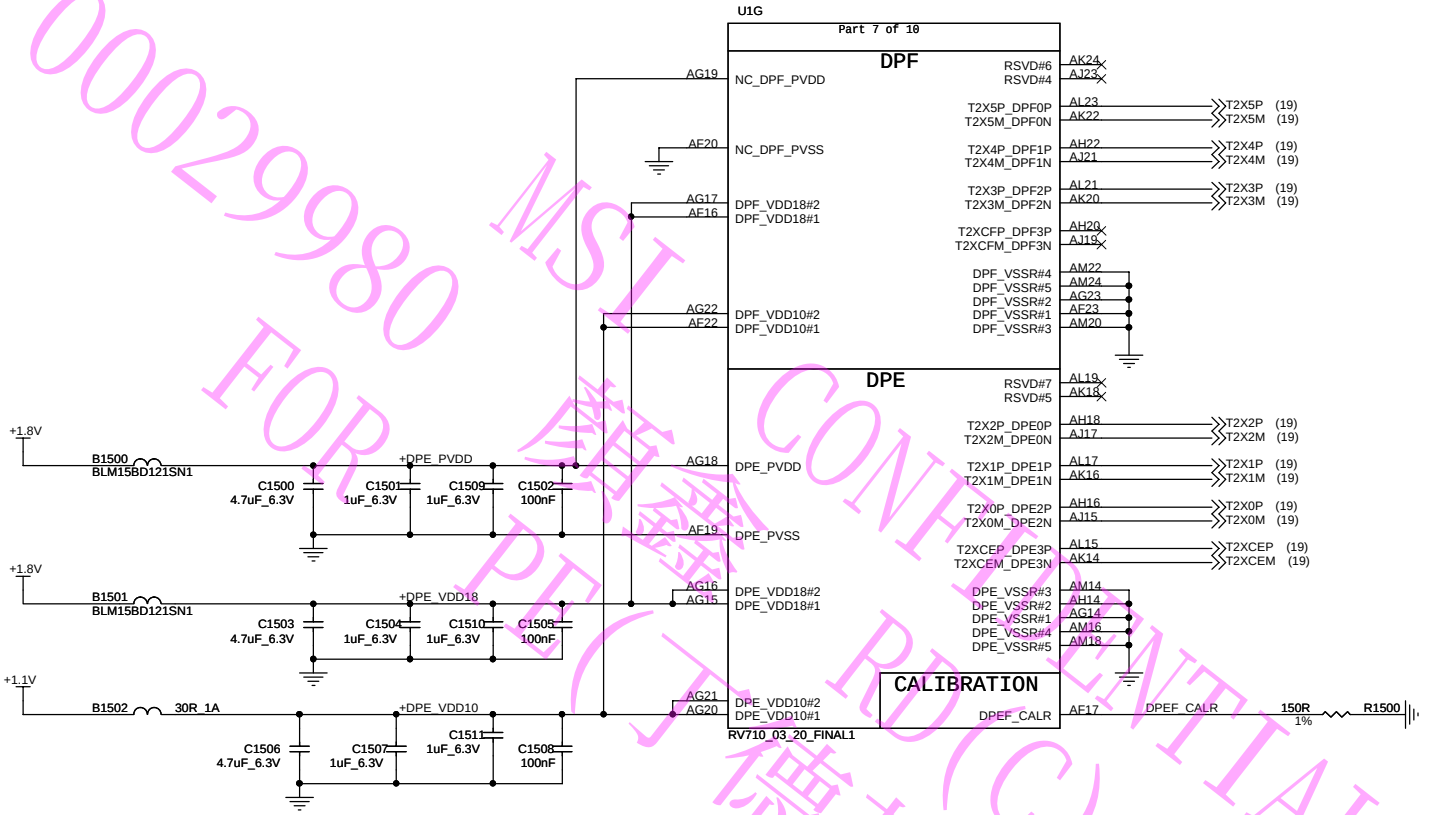
LVTMDP INTERFACE



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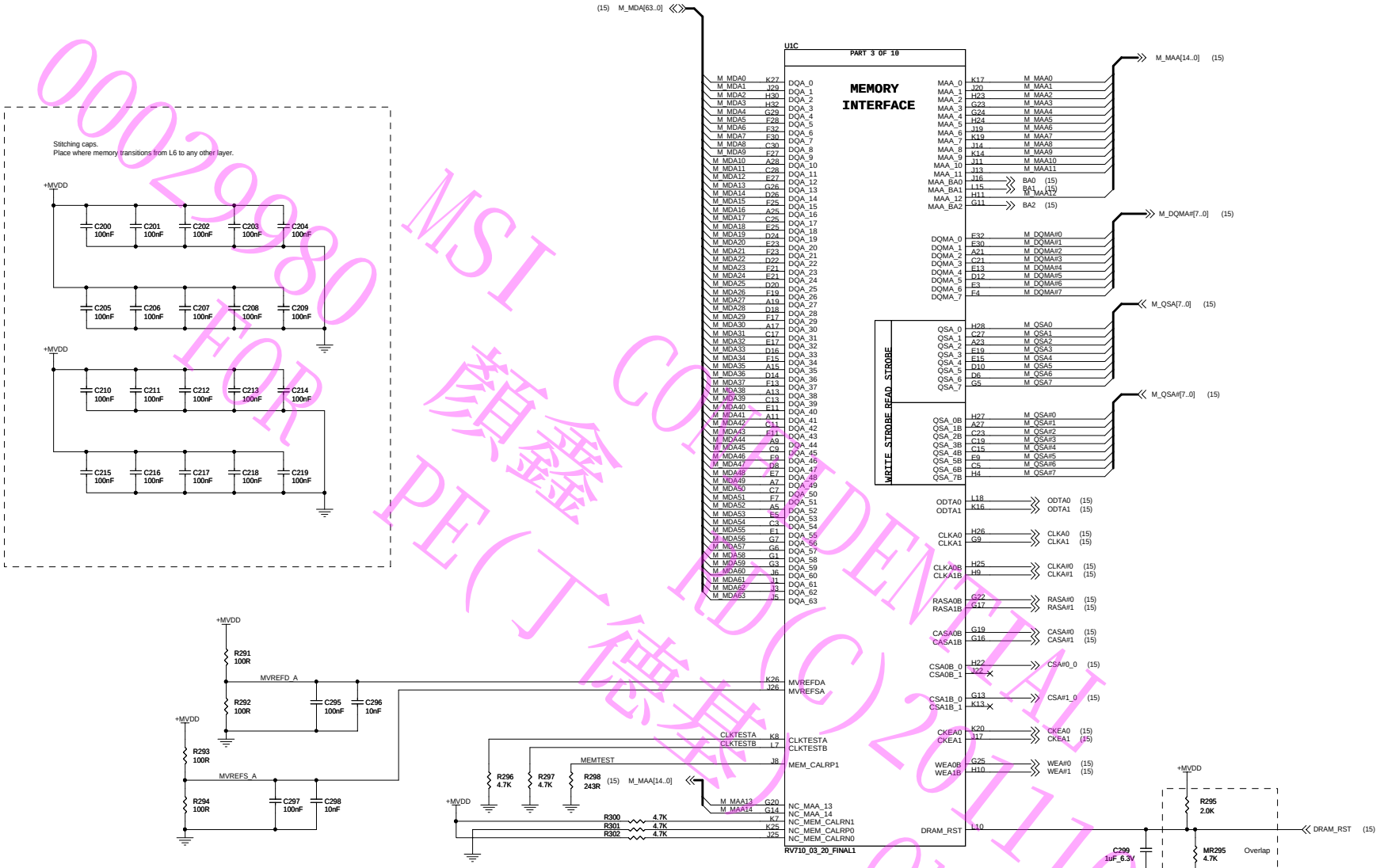
MEMORY INTERFACE



DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R

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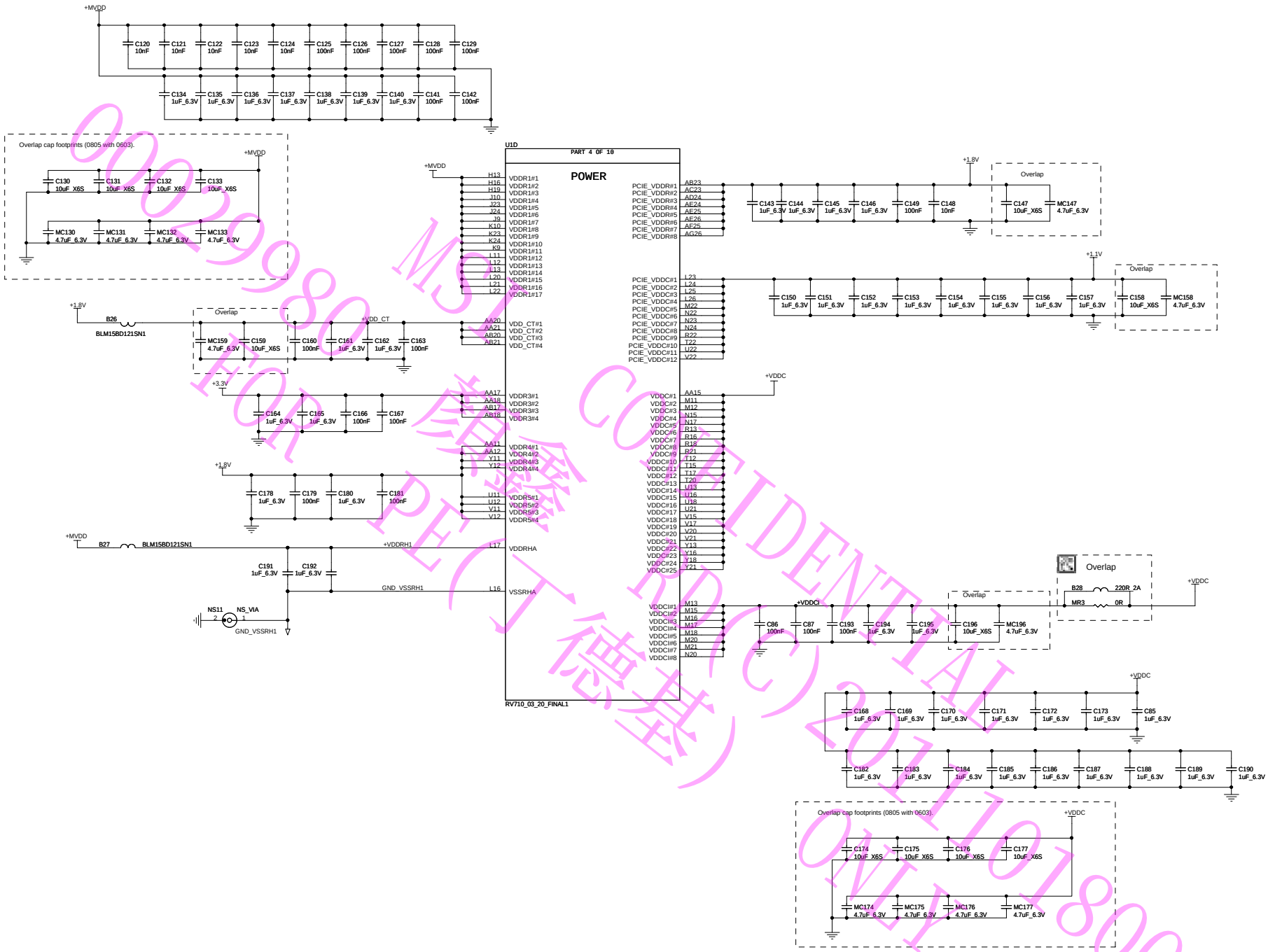

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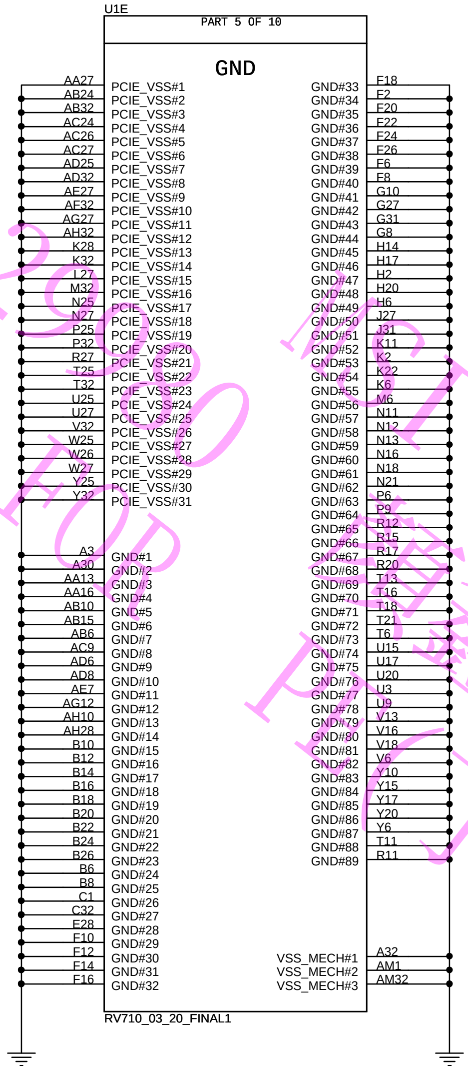

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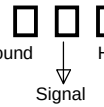
PIN BASED STRAPS

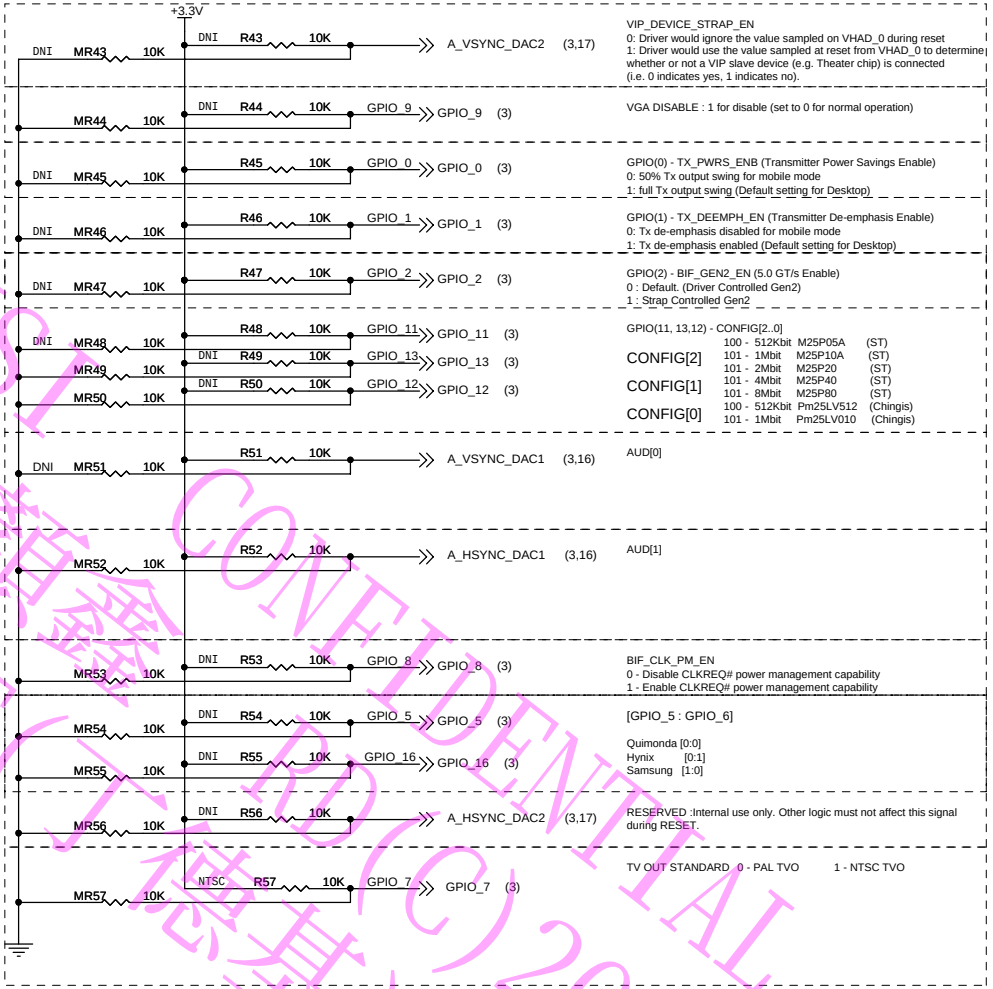
Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout



PIN BASED STRAPS



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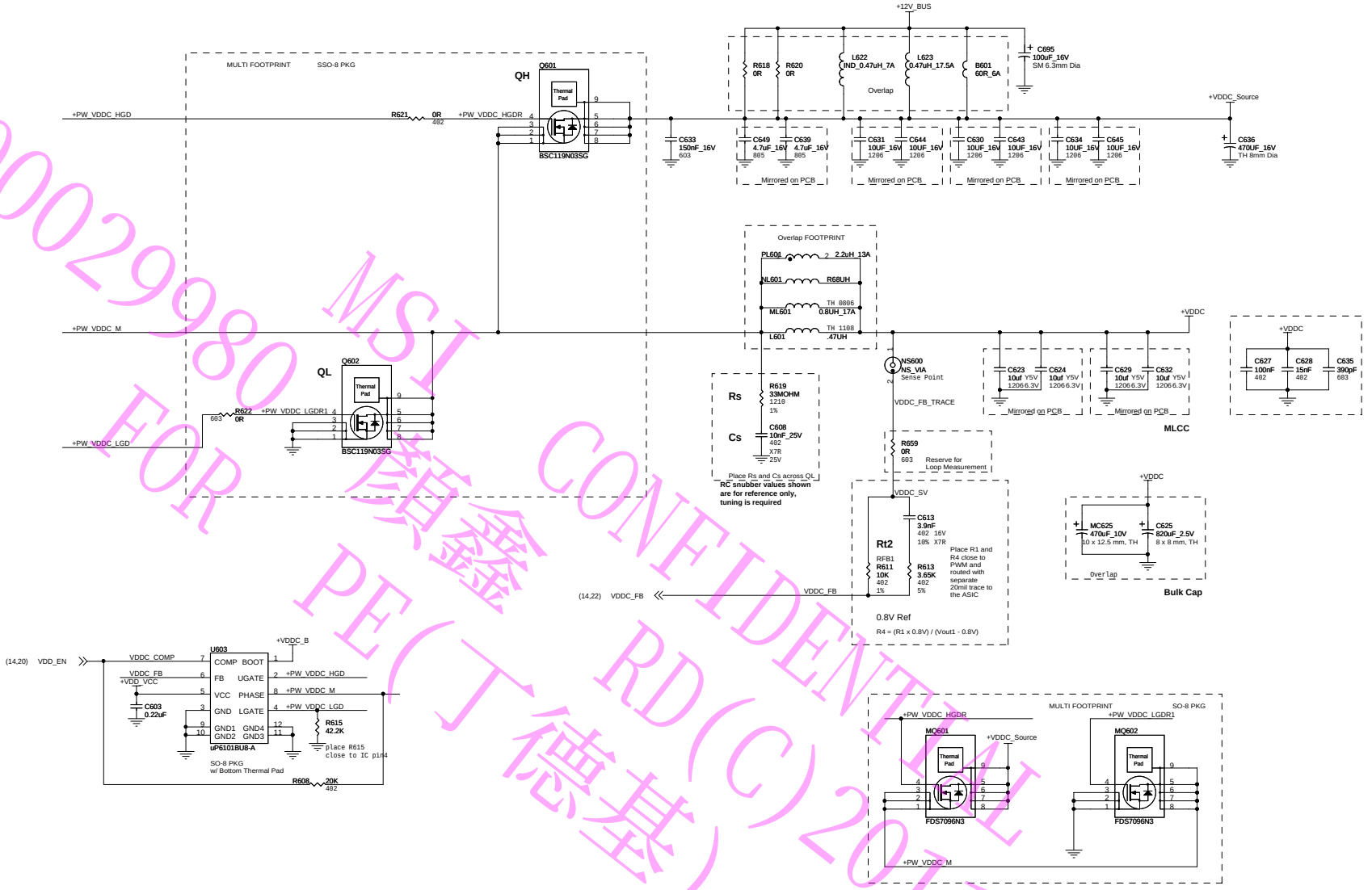
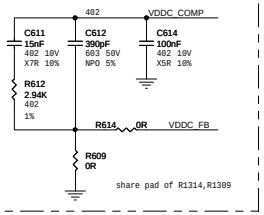
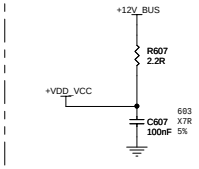


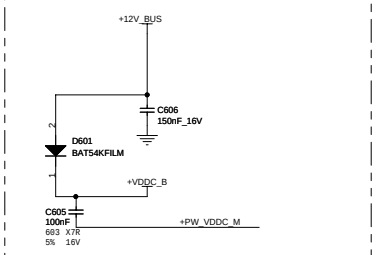
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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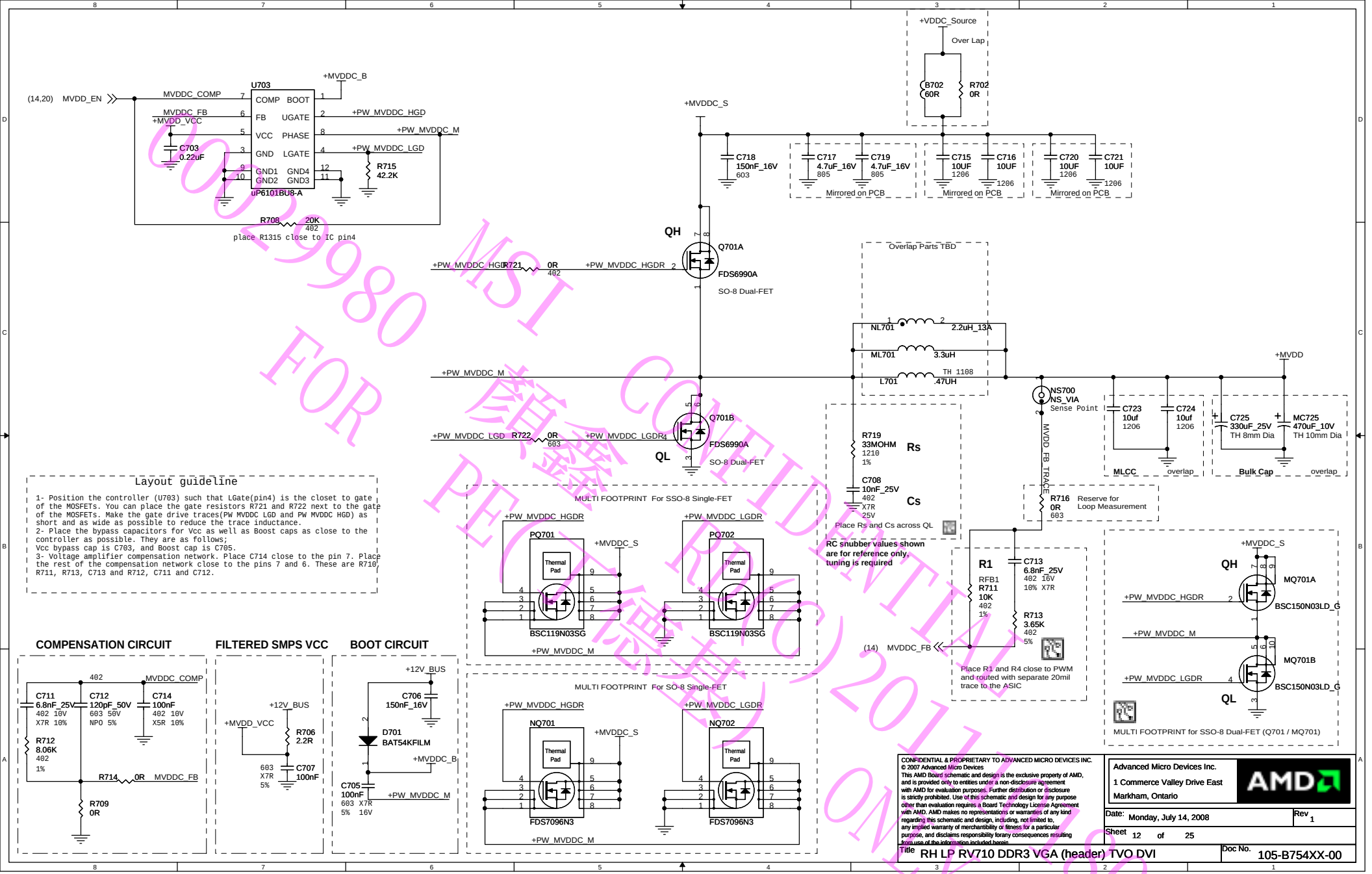
(14,20) MVDD_EN
U703
MVDDC_COMP
MVDDC_FB
+MVDD_VCC
COMP BOOT
FB UGATE
VCC PHASE
GND LGATE
GND1 GND4
GND2 GND3
uP6101BU8-A
+MVDDC_B
+PW_MVDDC_HGD
+PW_MVDDC_M
+PW_MVDDC_LGD
C703 0.22uF
R715 42.2K
R708 20K 402
place R1315 close to IC pin4
+VDDC_Source
Over Lap
B702 60R
R702 0R
+MVDDC_S
C718 150nF_16V 603
C717 4.7uF_16V 805
C719 4.7uF_16V 805
C715 10UF 1206
C716 10UF 1206
C720 10UF 1206
C721 10UF 1206
Mirrored on PCB
QH
Q701A
FDS6990A
SO-8 Dual-FET
+PW_MVDDC_HGDR
R721 0R 402
+PW_MVDDC_HGDR_2
Overlap Parts TBD
NL701 2.2uH_13A
ML701 3.3uH
L701 .47UH TH 1108
+MVDD
+PW_MVDDC_M
NS700 NS_VIA Sense Point
C723 10uf 1206
C724 10uf 1206
C725 330uF_25V TH 8mm Dia
MC725 470uF_10V TH 10mm Dia
MLCC overlap
Bulk Cap overlap
Q701B
QL
+PW_MVDDC_LGD
R722 0R 603
+PW_MVDDC_LGDR_4
R719 33MOHM 1210 1%
Rs
C708 10nF_25V 402 X7R 25V
Cs
Place Rs and Cs across QL
RC snubber values shown are for reference only, tuning is required
MVDD_FB_TRACE
R716 0R 603
Reserve for Loop Measurement
MULTI FOOTPRINT For SSO-8 Single-FET
+PW_MVDDC_HGDR
+PW_MVDDC_LGDR
PQ701
PQ702
Thermal Pad
BSC119N03SG
+PW_MVDDC_M
R1 RFB1
R711 10K 402 1%
C713 6.8nF_25V 402 16V 10% X7R
R713 3.65K 402 5%
(14) MVDDC_FB
Place R1 and R4 close to PWM and routed with separate 20mil trace to the ASIC
MQ701A
MQ701B
BSC150N03LD_G
MULTI FOOTPRINT for SSO-8 Dual-FET (Q701 / MQ701)
NQ701
NQ702
FDS7096N3
Layout guideline
1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.
COMPENSATION CIRCUIT
C711 6.8nF_25V 402 10V X7R 10%
C712 120pF_50V 603 50V NPO 5%
C714 100nF 402 10V X5R 10%
R712 8.06K 402 1%
R714 0R
R709 0R
FILTERED SMPS VCC
+12V_BUS
+MVDD_VCC
R706 2.2R
C707 100nF 603 X7R 5%
BOOT CIRCUIT
C706 150nF_16V
D701 BAT54KFILM
C705 100nF 603 X7R 5% 16V
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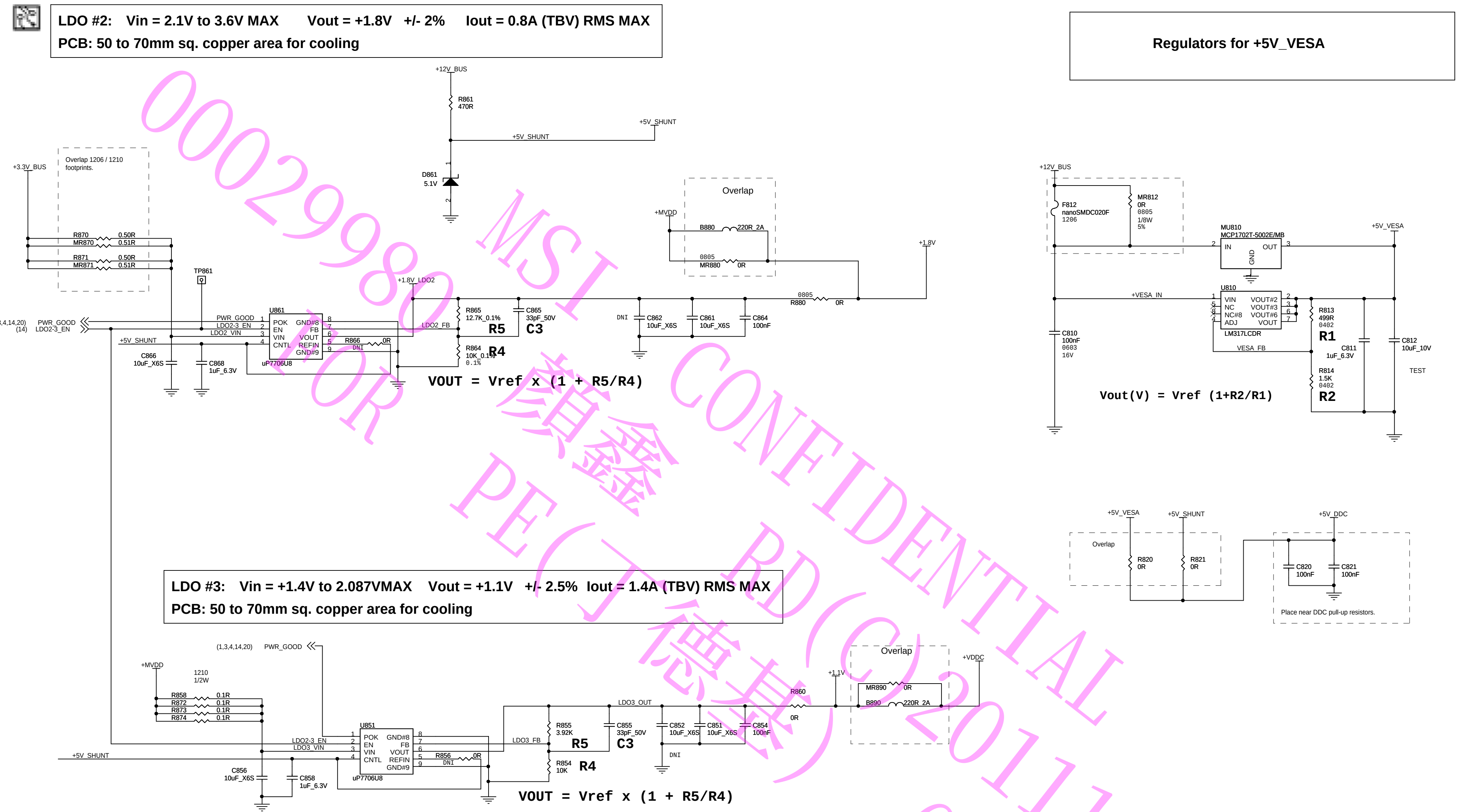

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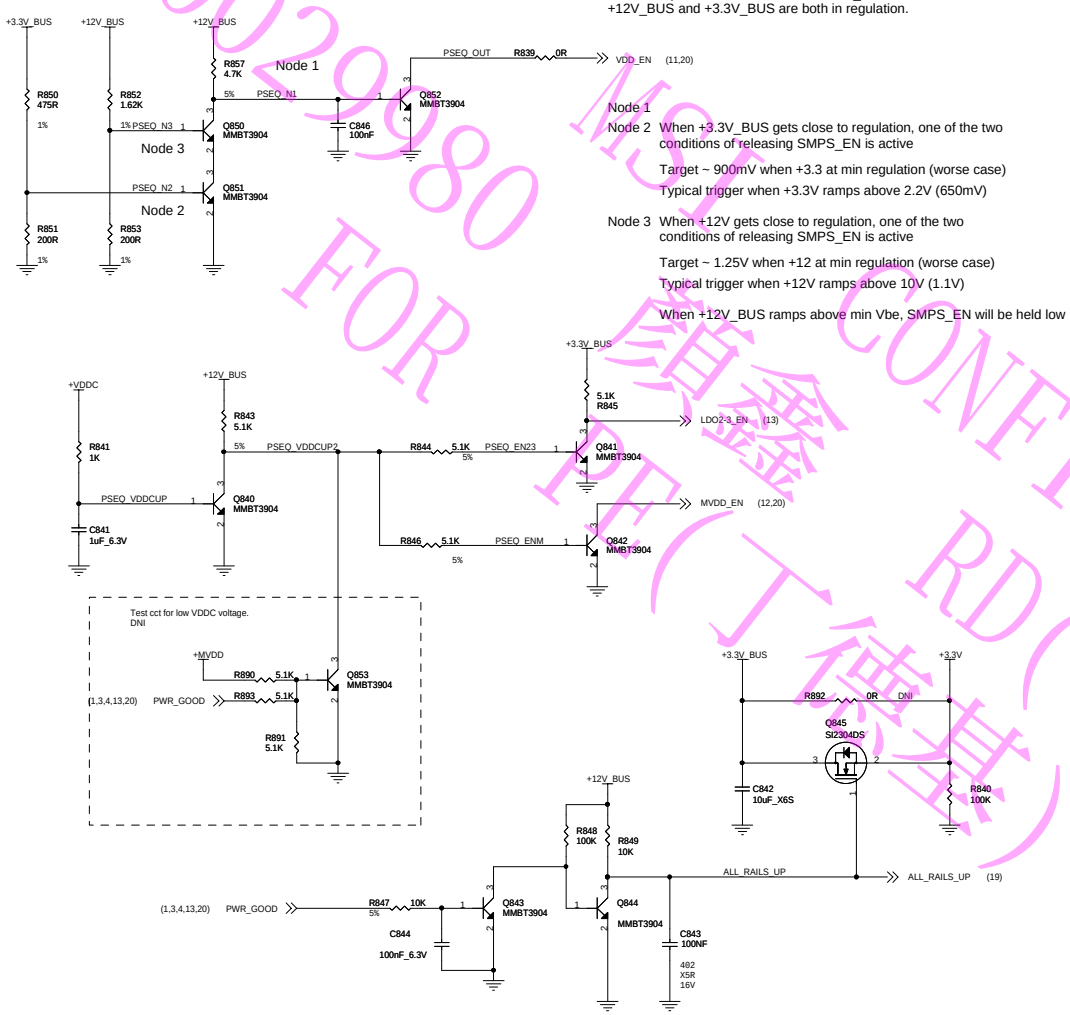
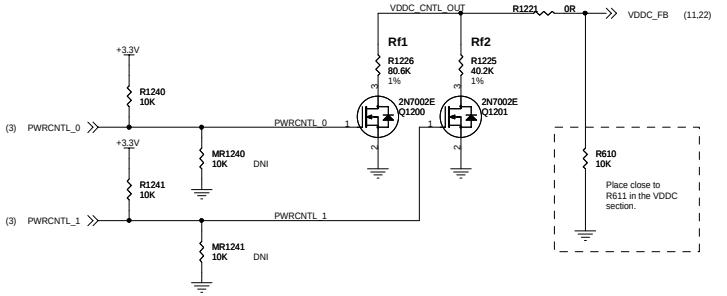
Power up/down Sequencing



Power Play

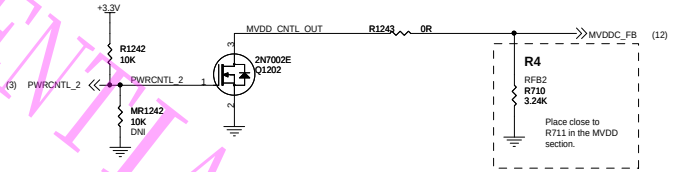
VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0	0				
0	1				
1	0				
1	1	1 0 1			Power-up Default



MVDD Voltage Settings Using GPIOs

PWRCNTL_2 GPIO_6	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0				
1	1 0 1			Power-up Default



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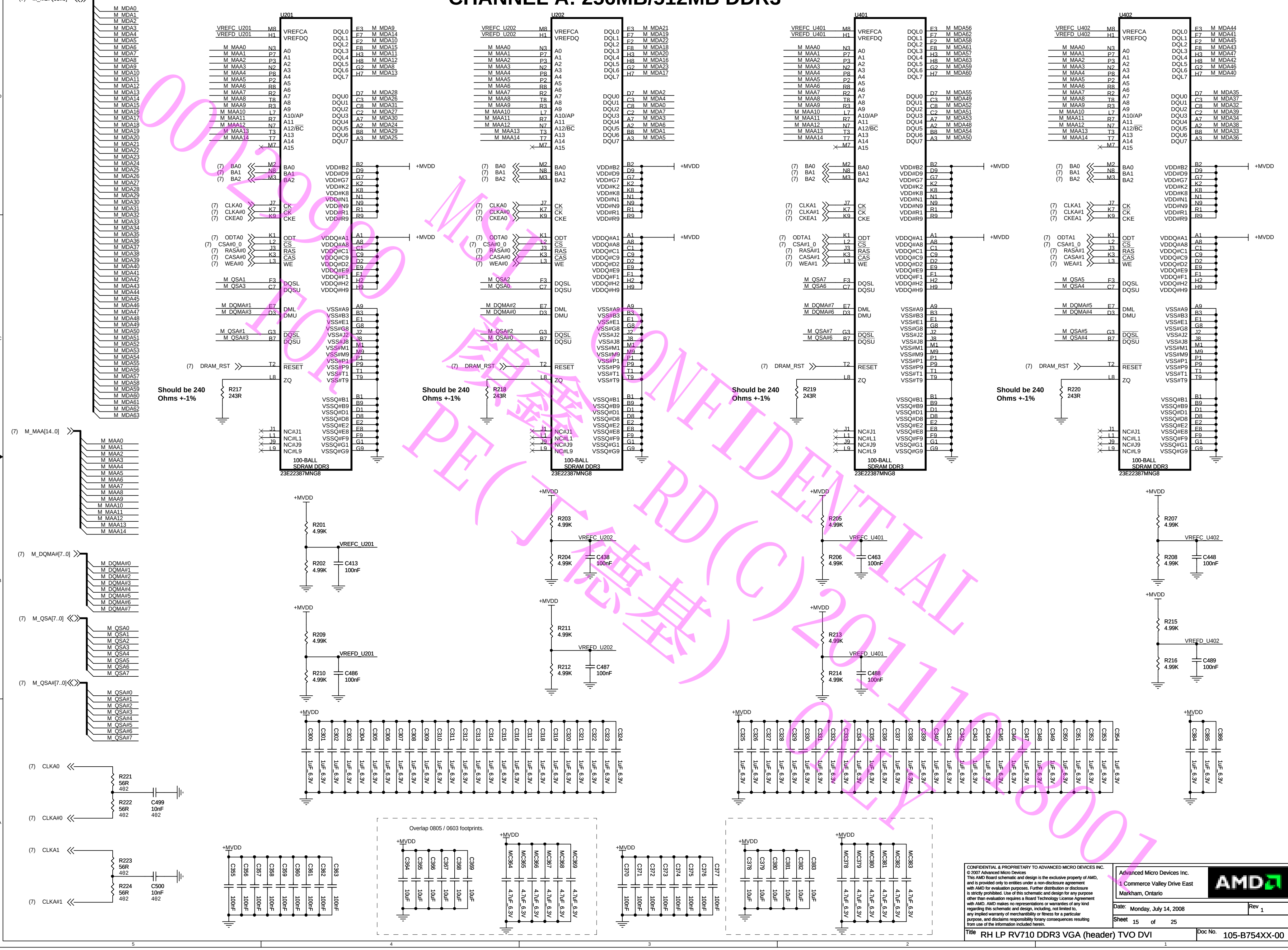
CHANNEL A: 256MB/512MB DDR3



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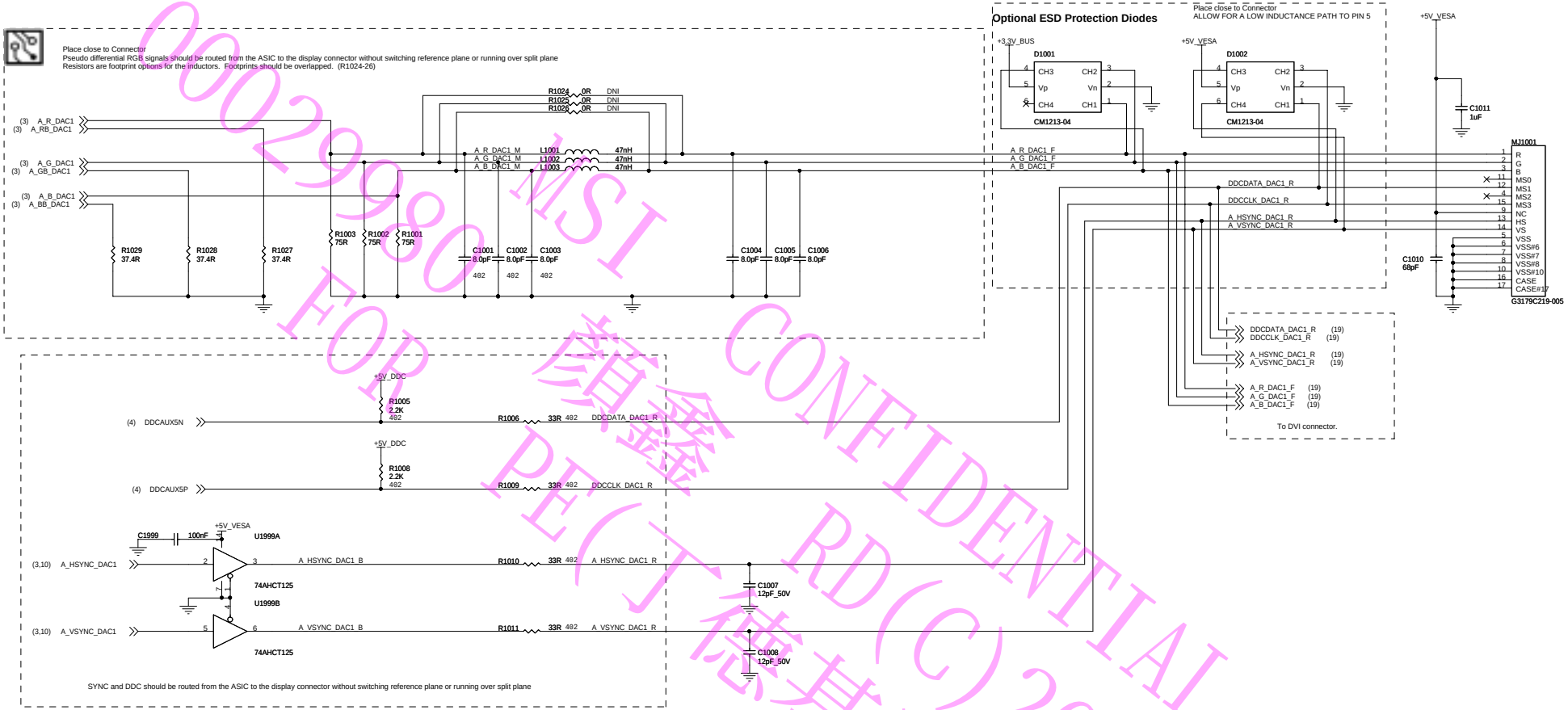
DAC 1 OUTPUT



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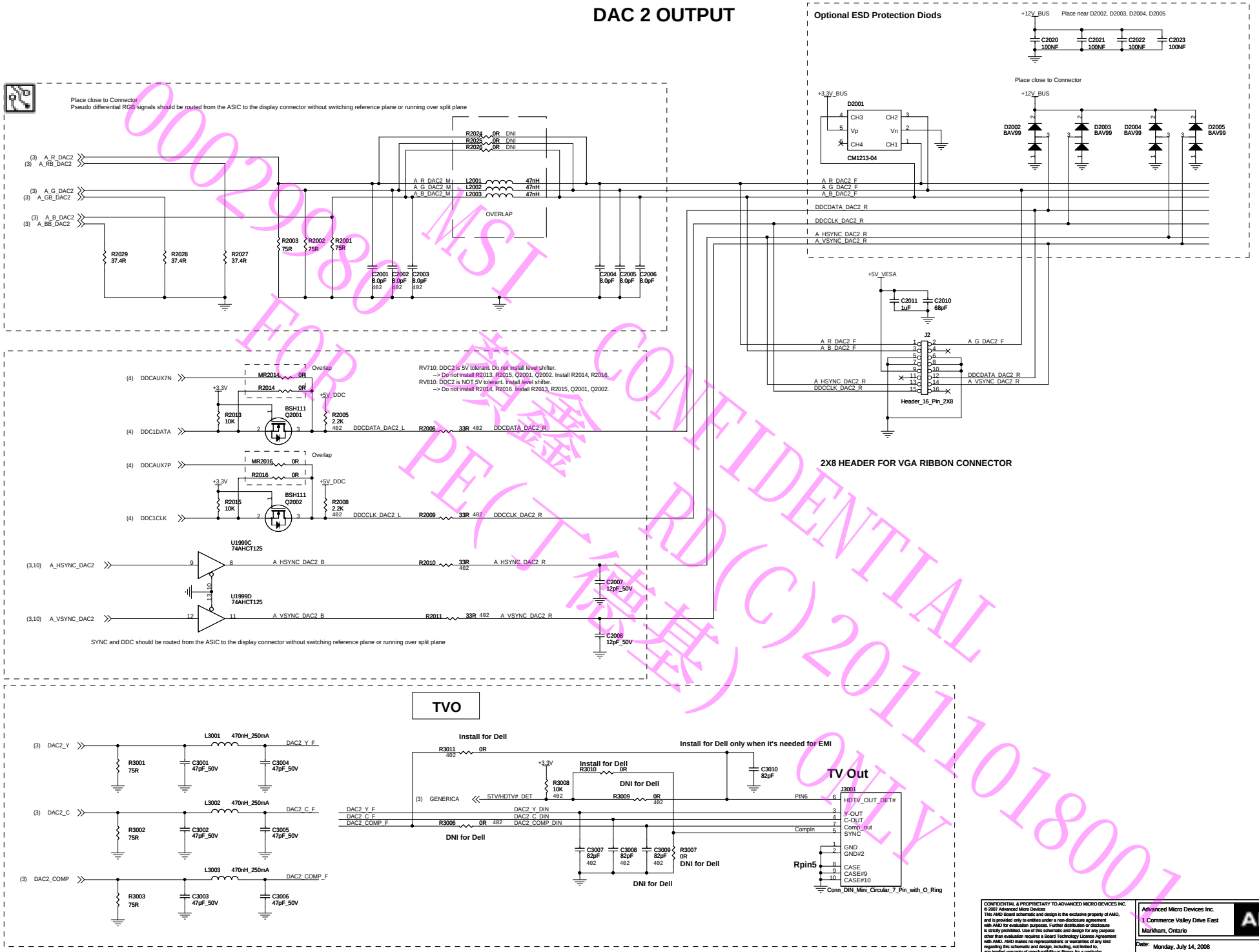
DAC 2 OUTPUT



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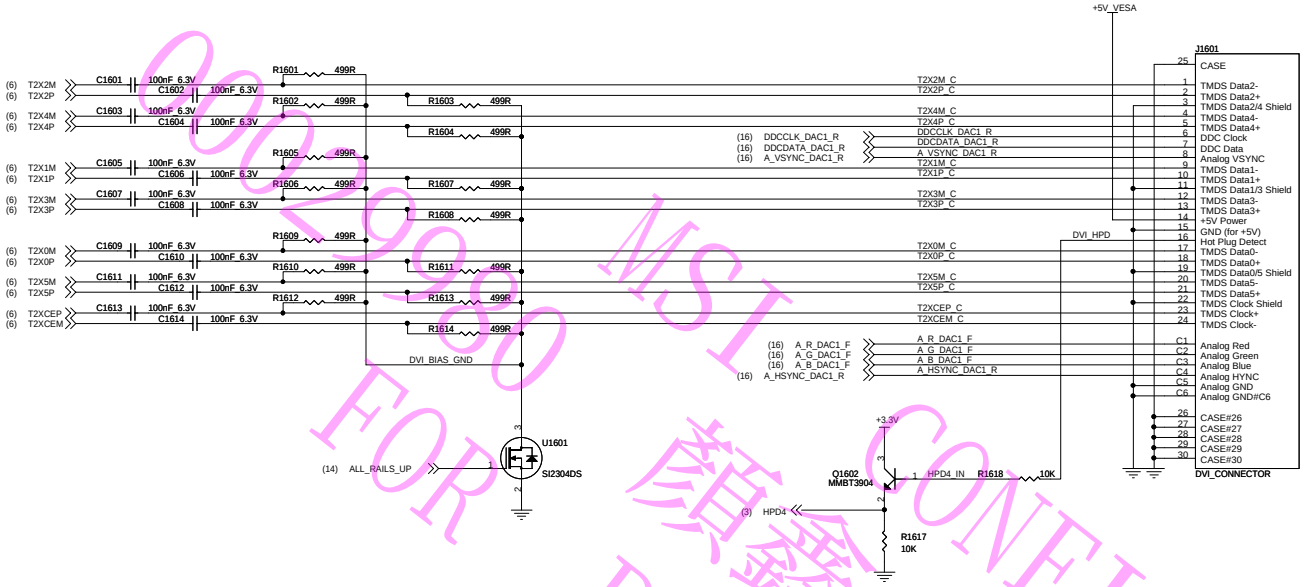
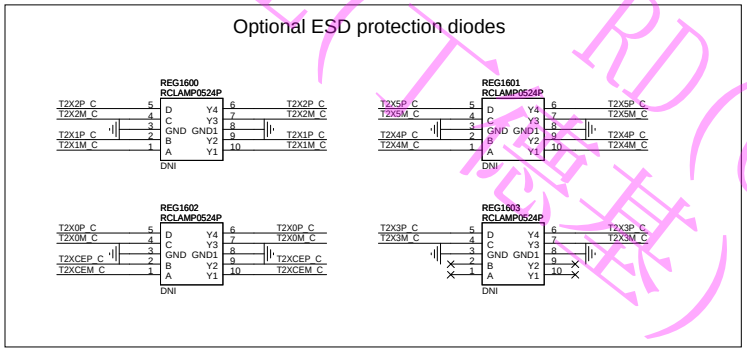
DPE / DPF OUTPUT





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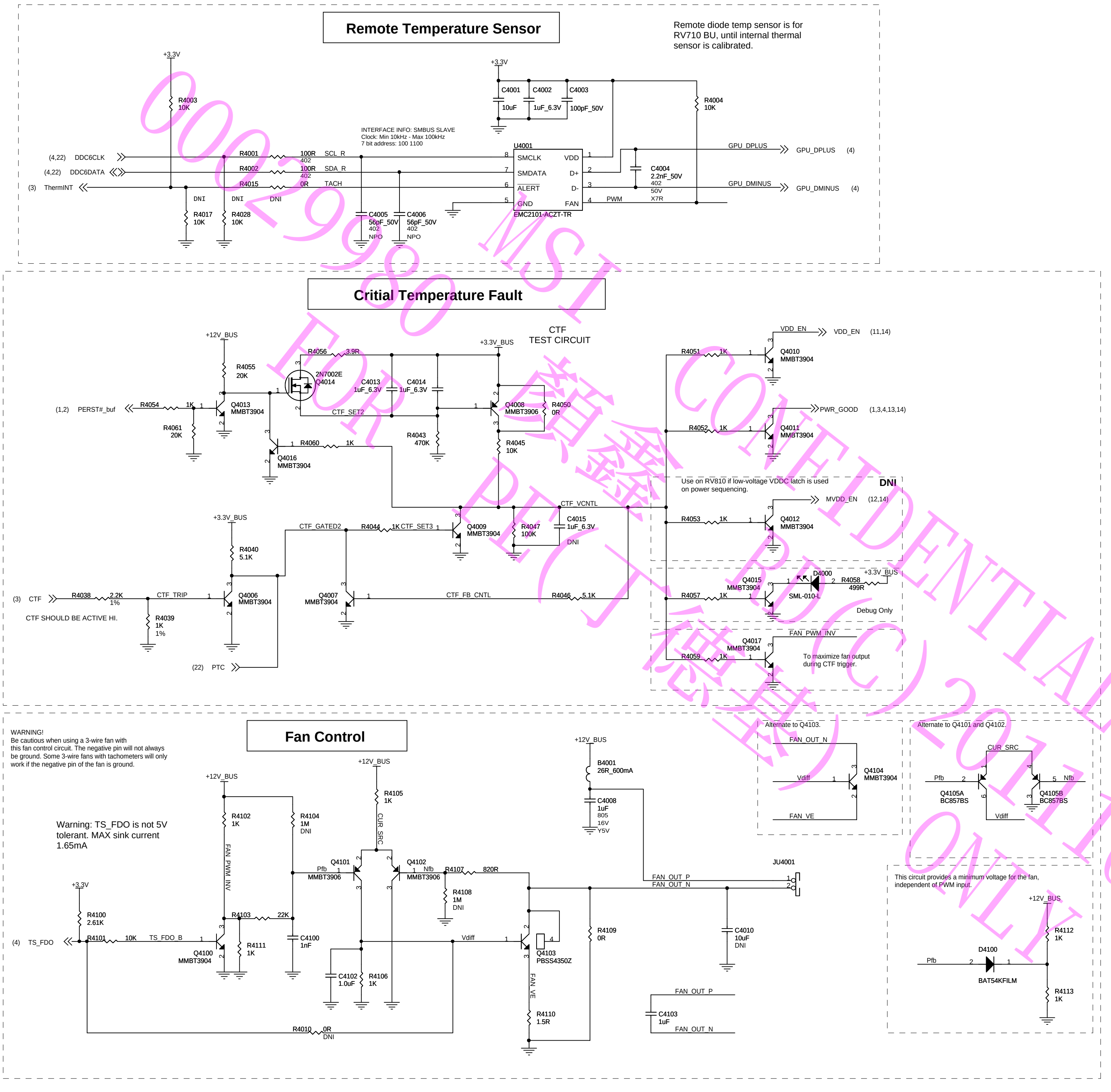
THERMAL MANAGEMENT



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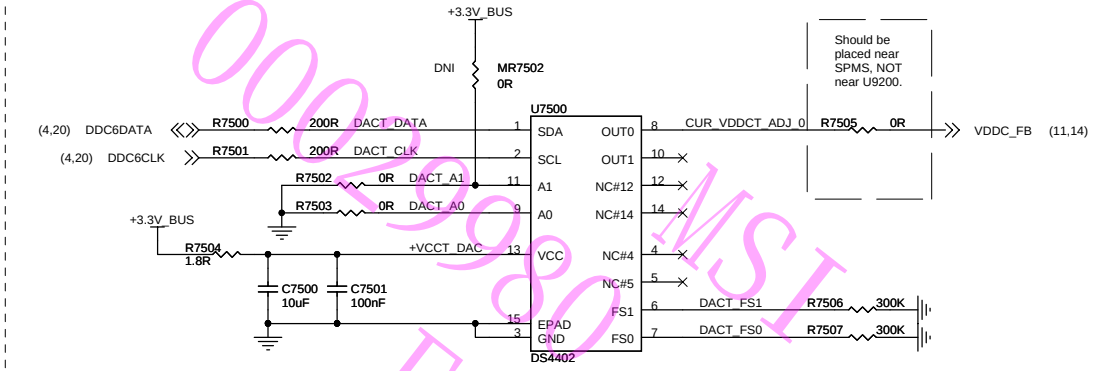
I2C VDDC Control



VDDC, MVDD Thermal Protection

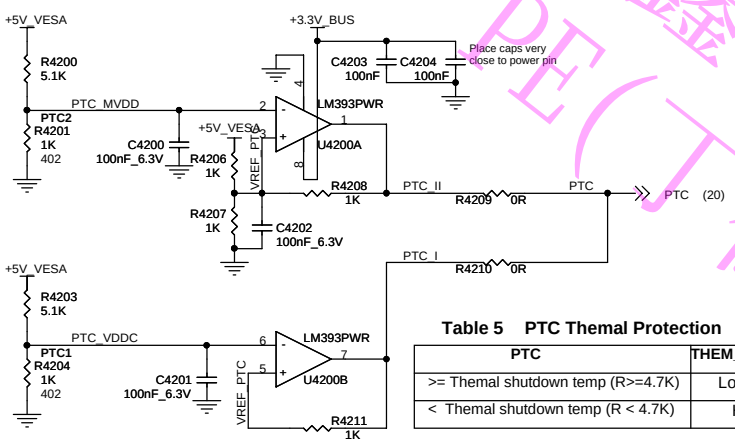


Table 5 PTC Themal Protection

PTC	THEM_PRT
>= Themal shutdown temp (R>=4.7K)	Low
< Themal shutdown temp (R < 4.7K)	Hi

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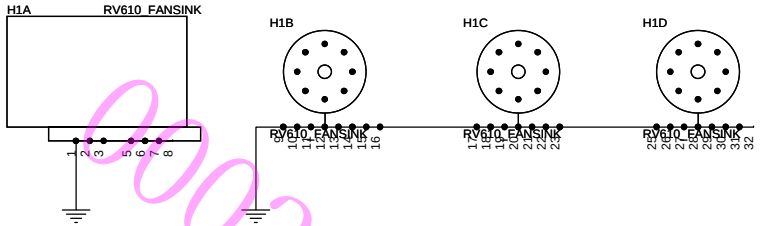

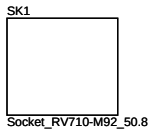

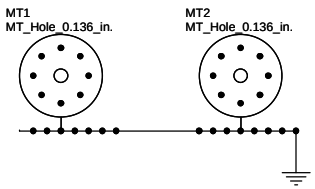

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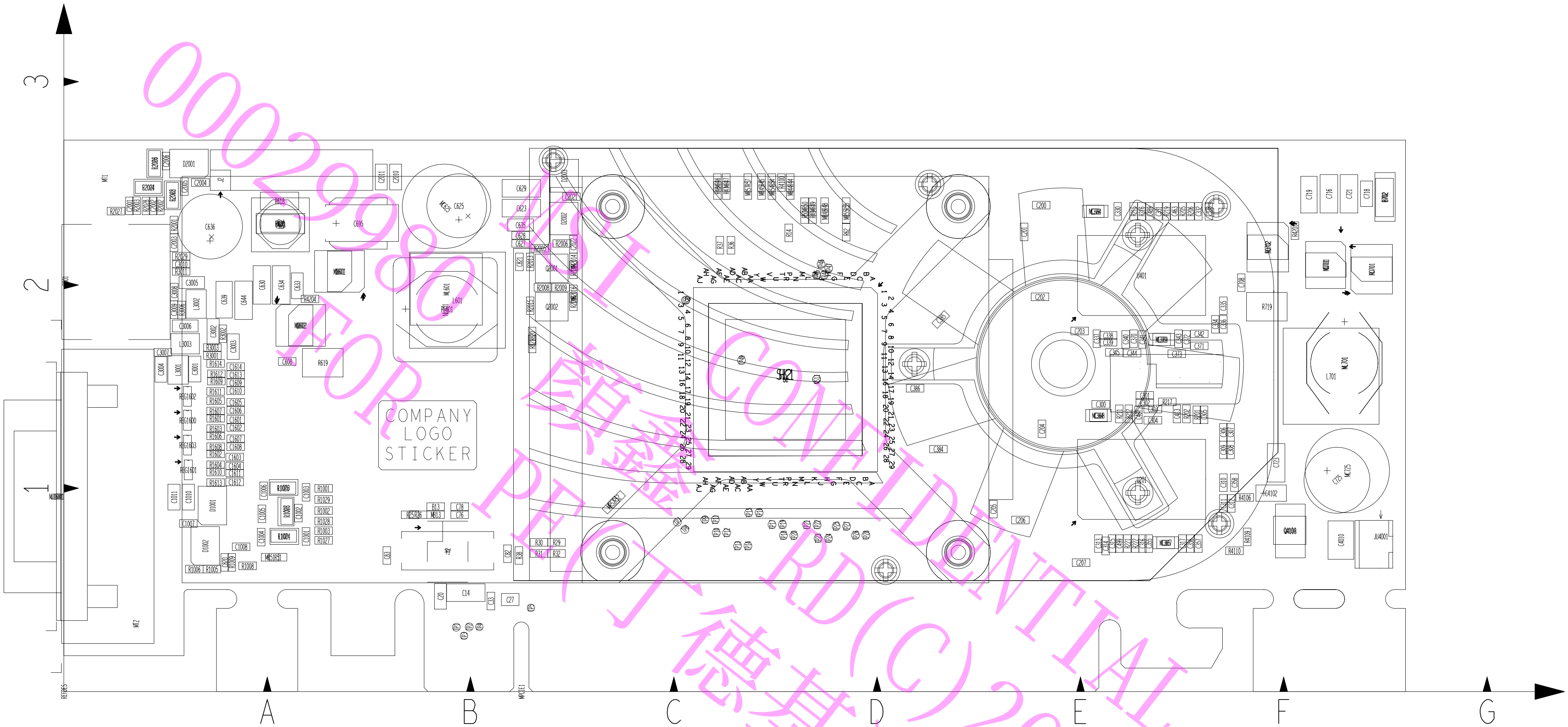

AMD
ADVANCED MICRO DEVICES
PCBCAD GROUP

HR RV710 DDR3 512 MB 64MX16 DDVI VO VGA HEADER No DC

PN 109-B75431-00B
JUNE 23, 2008
SVETLANA OSTROVSKY

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ADVANCED MICRO DEVICES PCBCAD GROUP	HR RV710 DDR3 512 MB 64MX16 DDI VO VGA HEADER No DC PN 109-B75431-00B JUNE 23, 2008 SVETLANA OSTROVSKY