

V034-10 NV44 128 MB DDR2, VGA, DVI-I, SD/HDTV

REVIEW HISTORY

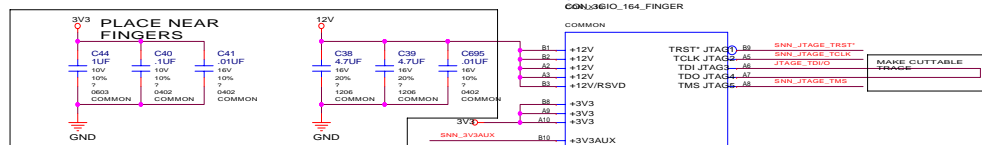
- 01. Cover page
- 02. PEX interface
- 03. GPU FB-interface
- 04. MEMORY Bit 0..31
- 05. MEMORY Bit 32..64
- 06. DAC-A, DB15 Con.
- 07. DAC-B, MUX, DB15
- 08. Internal TMDS
- 09. MIOA, MIOB
- 10. Straps
- 11. BIOS, GPIO, FAN Con.
- 12. Mini DIN
- 13. Power :NVVDD/FBVDD
- 14. Power others

A01

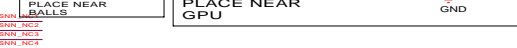
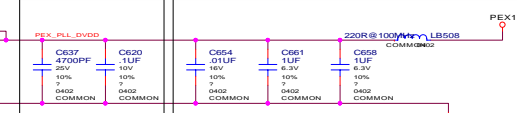
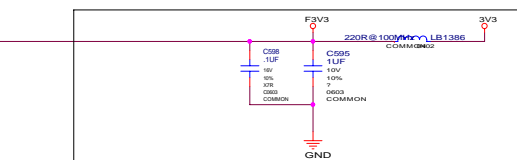
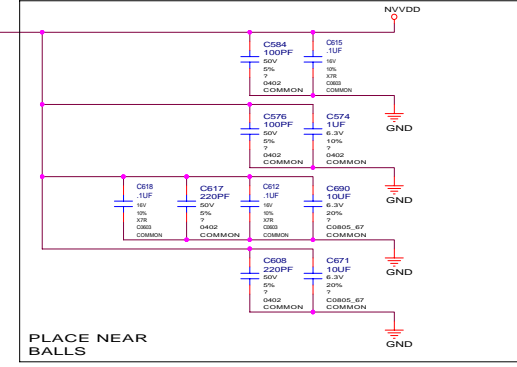
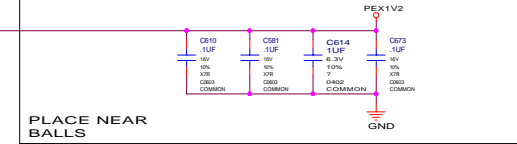
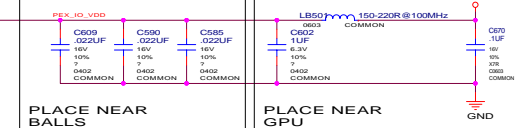
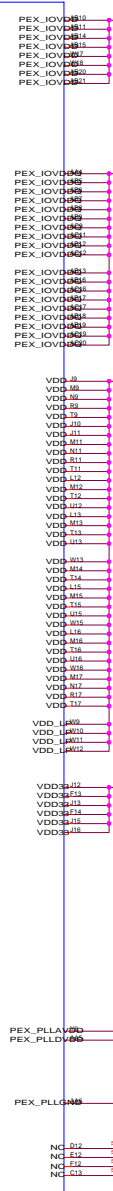
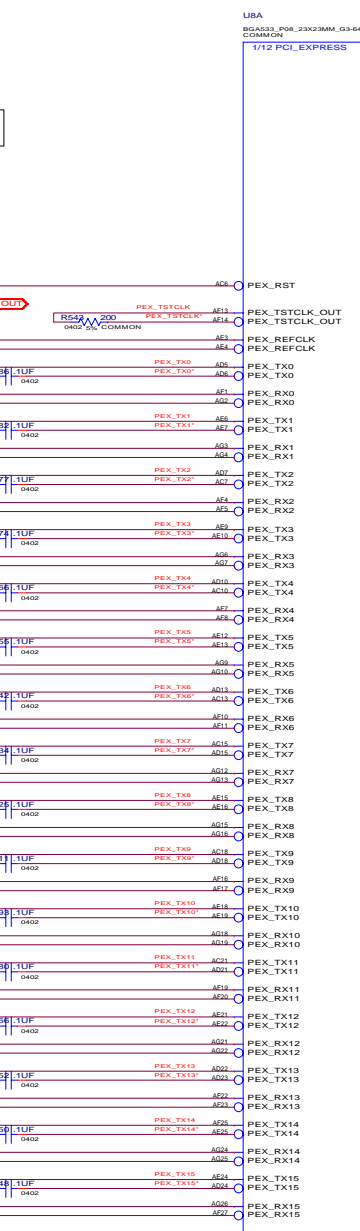
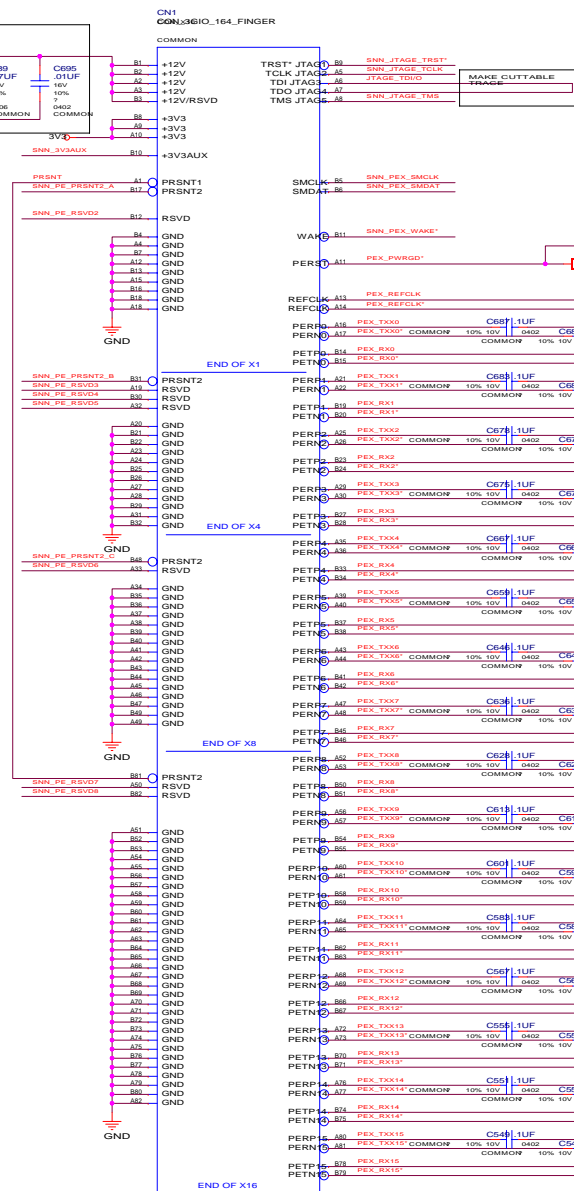
- 9/22/2004:
 - Changed TMDS_PLLVDD to PLLVDD
 - Added bead option to PLLVDD rail of NV44
 - Changed RSET values for DACA and DACB
 - Changed DACB RSET FET to a dual package with GPIO11 control-Macrovision
 - Added F3V3 bypass to PLLVDD linear regulator
 - Changed location of R62

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10999-xxxx-xx	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
1	0000	600-10262-0000-000	AND NOT FINAL
2	0001	600-10262-0001-000	<UNDEFINED>
3	0002	600-10262-0002-000	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

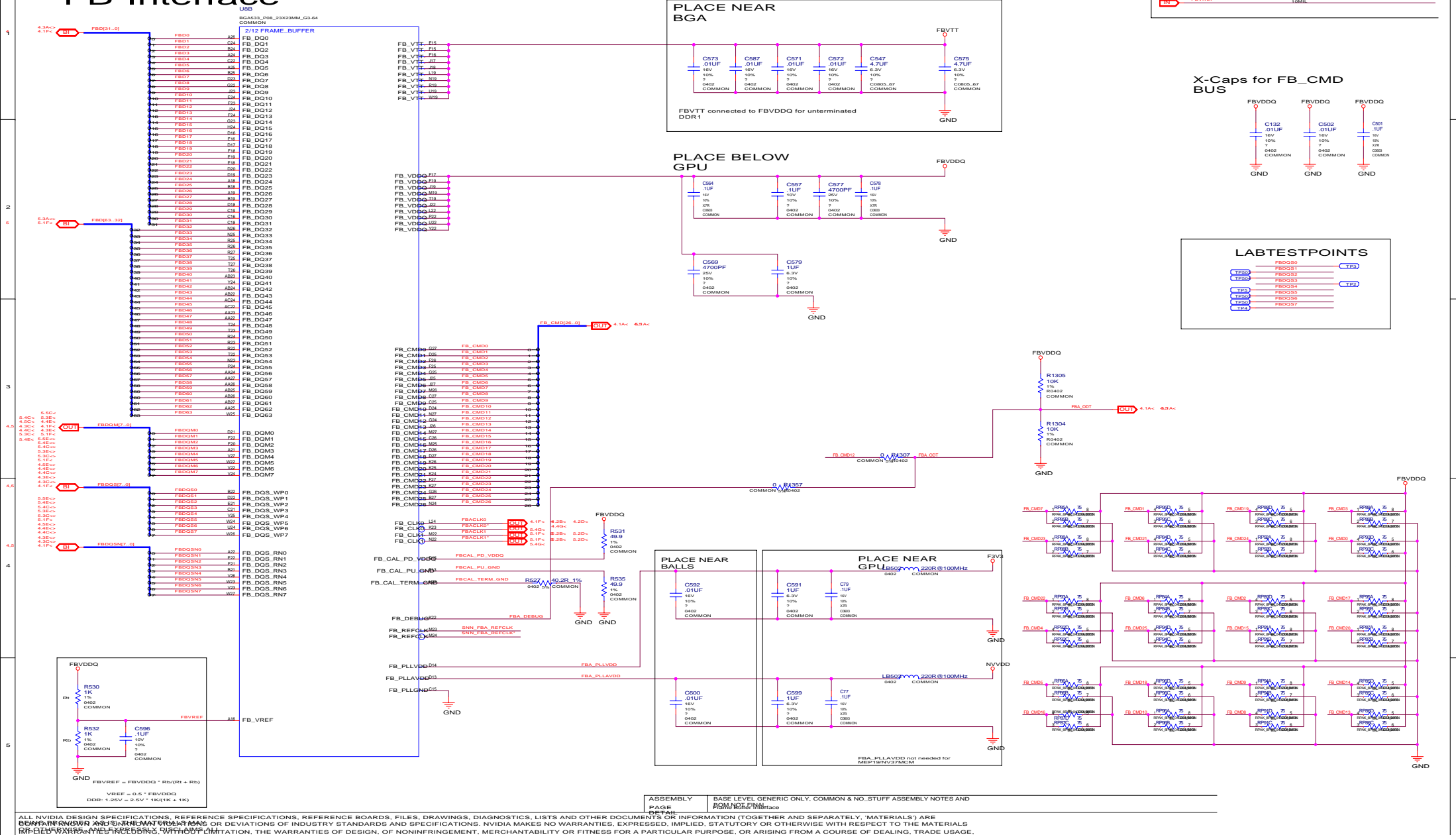
PEX-Interface



	Net Name	DIFF_PAIR	NET_SPACING	TYPE
1	PEX_TSTCLK	PEX_TST	25MM	
2	PEX_TSTCLK	PEX_TST	25MM	
3				
4	PEX_TX0	PEX_TX0	25MM	
5	PEX_TX0	PEX_TX0	25MM	
6	PEX_TX1	PEX_TX1	25MM	
7	PEX_TX1	PEX_TX1	25MM	
8	PEX_TX2	PEX_TX2	25MM	
9	PEX_TX2	PEX_TX2	25MM	
10	PEX_TX3	PEX_TX3	25MM	
11	PEX_TX3	PEX_TX3	25MM	
12	PEX_TX4	PEX_TX4	25MM	
13	PEX_TX4	PEX_TX4	25MM	
14	PEX_TX5	PEX_TX5	25MM	
15	PEX_TX5	PEX_TX5	25MM	
16	PEX_TX6	PEX_TX6	25MM	
17	PEX_TX6	PEX_TX6	25MM	
18	PEX_TX7	PEX_TX7	25MM	
19	PEX_TX7	PEX_TX7	25MM	
20	PEX_TX8	PEX_TX8	25MM	
21	PEX_TX8	PEX_TX8	25MM	
22	PEX_TX9	PEX_TX9	25MM	
23	PEX_TX9	PEX_TX9	25MM	
24	PEX_TX10	PEX_TX10	25MM	
25	PEX_TX10	PEX_TX10	25MM	
26	PEX_TX11	PEX_TX11	25MM	
27	PEX_TX11	PEX_TX11	25MM	
28	PEX_TX12	PEX_TX12	25MM	
29	PEX_TX12	PEX_TX12	25MM	
30	PEX_TX13	PEX_TX13	25MM	
31	PEX_TX13	PEX_TX13	25MM	
32	PEX_TX14	PEX_TX14	25MM	
33	PEX_TX14	PEX_TX14	25MM	
34	PEX_TX15	PEX_TX15	25MM	
35	PEX_TX15	PEX_TX15	25MM	
36				
37	PEX_TX00	PEX_TX00	25MM	
38	PEX_TX01	PEX_TX00	25MM	
39	PEX_TX01	PEX_TX01	25MM	
40	PEX_TX02	PEX_TX02	25MM	
41	PEX_TX02	PEX_TX02	25MM	
42	PEX_TX03	PEX_TX03	25MM	
43	PEX_TX04	PEX_TX03	25MM	
44	PEX_TX04	PEX_TX04	25MM	
45	PEX_TX05	PEX_TX04	25MM	
46	PEX_TX05	PEX_TX05	25MM	
47	PEX_TX06	PEX_TX06	25MM	
48	PEX_TX07	PEX_TX06	25MM	
49	PEX_TX07	PEX_TX07	25MM	
50	PEX_TX08	PEX_TX08	25MM	
51	PEX_TX09	PEX_TX08	25MM	
52	PEX_TX09	PEX_TX09	25MM	
53	PEX_TX10	PEX_TX09	25MM	
54	PEX_TX10	PEX_TX10	25MM	
55	PEX_TX11	PEX_TX10	25MM	
56	PEX_TX11	PEX_TX11	25MM	
57	PEX_TX12	PEX_TX11	25MM	
58	PEX_TX12	PEX_TX12	25MM	
59	PEX_TX13	PEX_TX12	25MM	
60	PEX_TX13	PEX_TX13	25MM	
61	PEX_TX14	PEX_TX13	25MM	
62	PEX_TX14	PEX_TX14	25MM	
63	PEX_TX15	PEX_TX14	25MM	
64	PEX_TX15	PEX_TX15	25MM	
65	PEX_TX15	PEX_TX15	25MM	
66				
67	PEX_RX0	PEX_RX0	25MM	
68	PEX_RX0	PEX_RX0	25MM	
69	PEX_RX1	PEX_RX0	25MM	
70	PEX_RX1	PEX_RX1	25MM	
71	PEX_RX2	PEX_RX1	25MM	
72	PEX_RX2	PEX_RX2	25MM	
73	PEX_RX3	PEX_RX2	25MM	
74	PEX_RX3	PEX_RX3	25MM	
75	PEX_RX4	PEX_RX3	25MM	
76	PEX_RX4	PEX_RX4	25MM	
77	PEX_RX5	PEX_RX4	25MM	
78	PEX_RX5	PEX_RX5	25MM	
79	PEX_RX6	PEX_RX5	25MM	
80	PEX_RX6	PEX_RX6	25MM	
81	PEX_RX7	PEX_RX6	25MM	
82	PEX_RX7	PEX_RX7	25MM	
83	PEX_RX8	PEX_RX7	25MM	
84	PEX_RX8	PEX_RX8	25MM	
85	PEX_RX9	PEX_RX8	25MM	
86	PEX_RX9	PEX_RX9	25MM	
87	PEX_RX10	PEX_RX9	25MM	
88	PEX_RX10	PEX_RX10	25MM	
89	PEX_RX11	PEX_RX10	25MM	
90	PEX_RX11	PEX_RX11	25MM	
91	PEX_RX12	PEX_RX11	25MM	
92	PEX_RX12	PEX_RX12	25MM	
93	PEX_RX13	PEX_RX12	25MM	
94	PEX_RX13	PEX_RX13	25MM	
95	PEX_RX14	PEX_RX13	25MM	
96	PEX_RX14	PEX_RX14	25MM	
97	PEX_RX15			

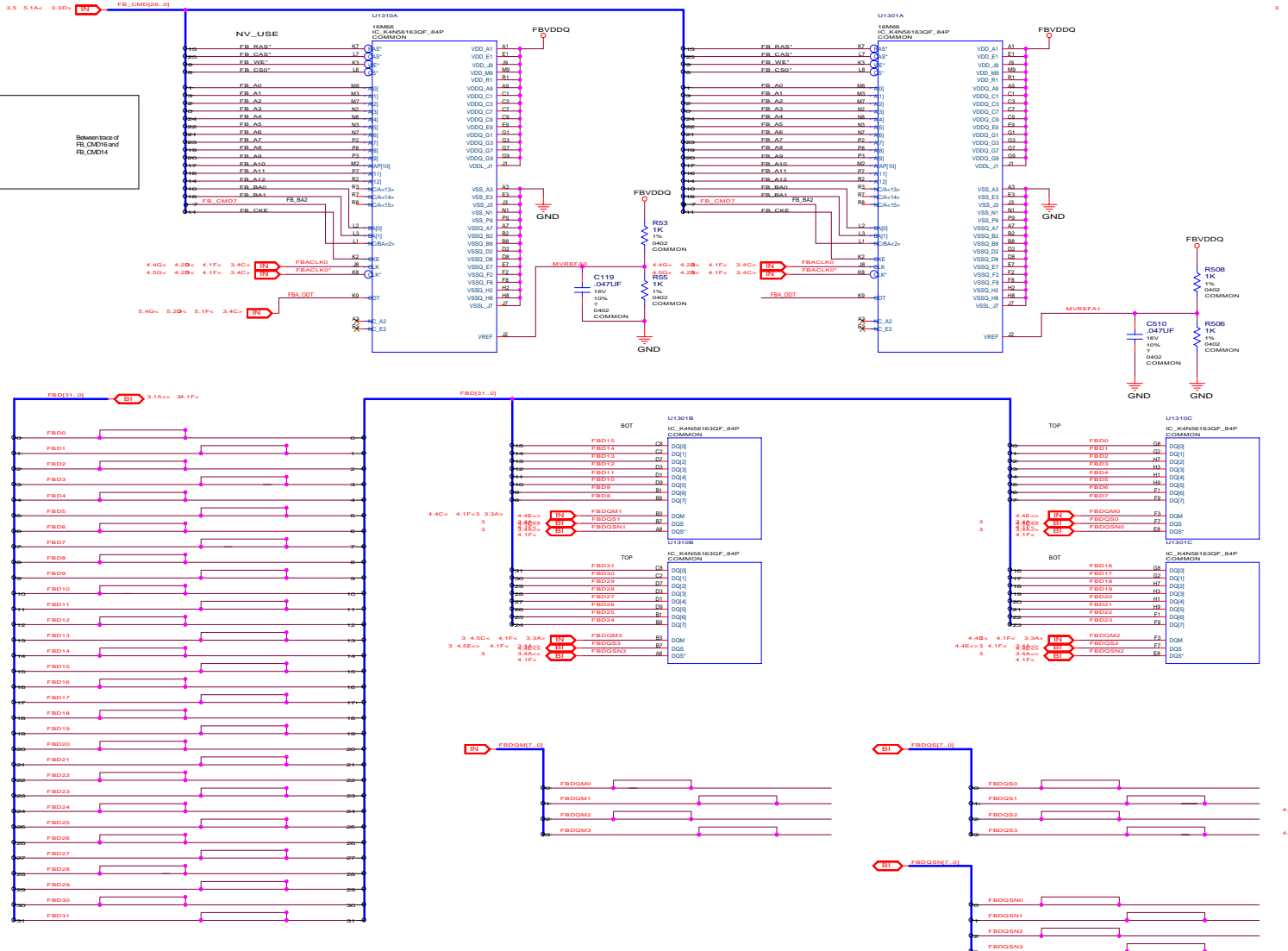


GPU: FB-Interface

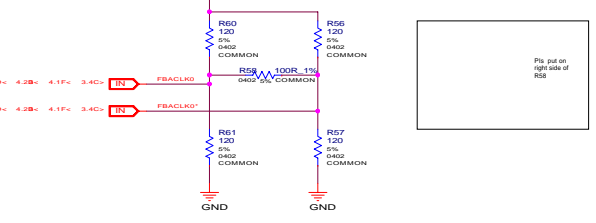
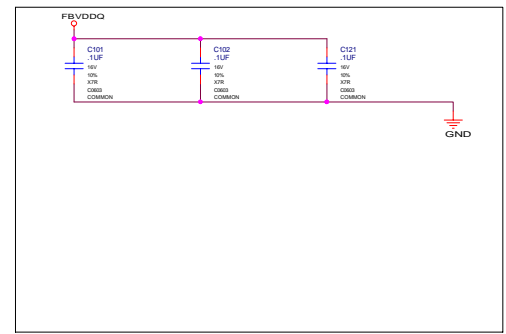
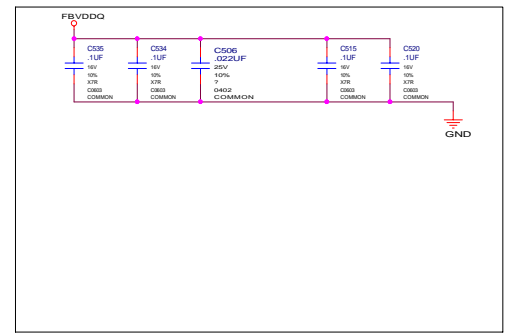


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED TO YOU ON AN "AS IS" BASIS. NVIDIA MAKES NO REPRESENTATIONS OR WARRANTIES, EXPRESSED OR IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. BY ACCEPTING AND USING THE MATERIALS, YOU AGREE TO RELEASE, DEFEND AND HOLD NVIDIA AND ITS SUPPLIERS HARMLESS FROM AND AGAINST ALL SUCH CLAIMS AND DAMAGES. WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE

Memory Bit 0..31



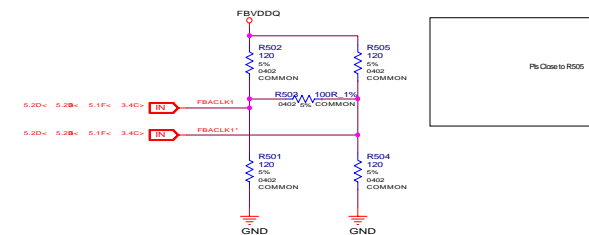
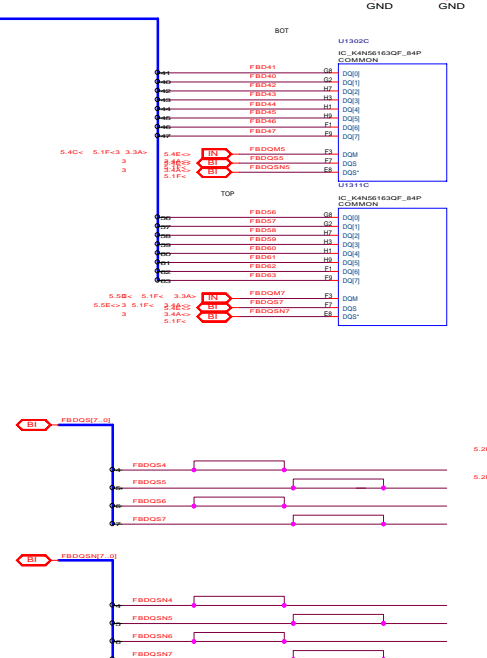
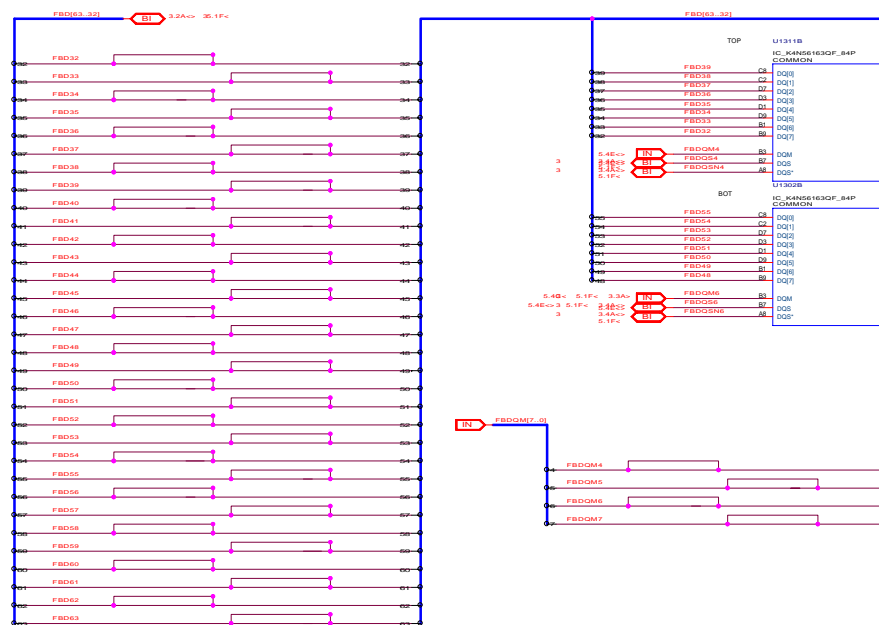
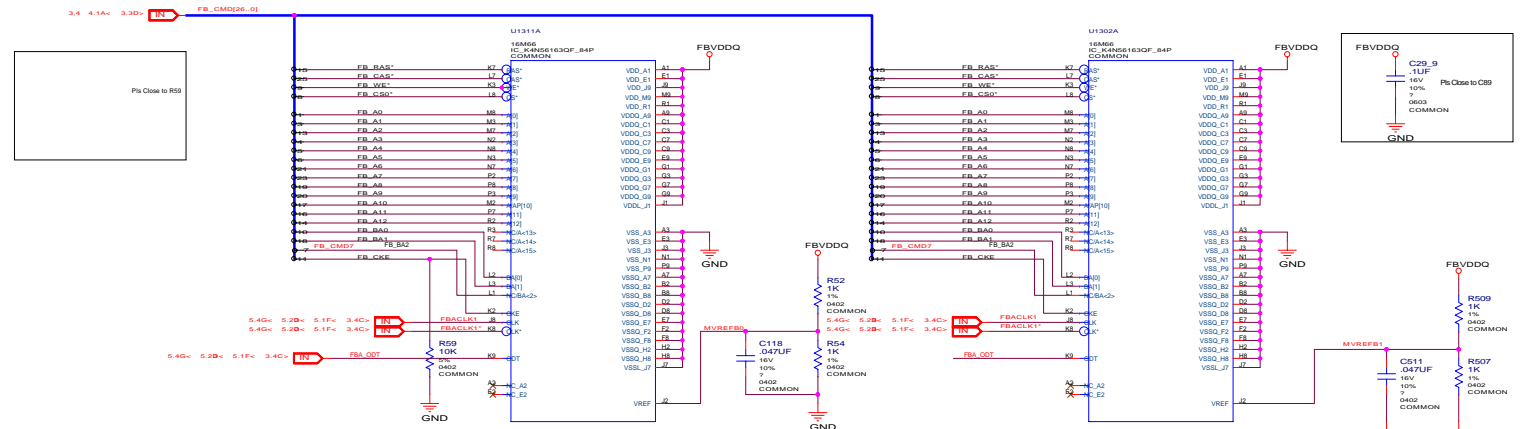
Net	Diffpair	NET_SPACING_RULE
FB_CMD16	FB_CMD16	25MIL
FB_CMD14	FB_CMD14	25MIL
FB_CMD12	FB_CMD12	25MIL
FB_CMD10	FB_CMD10	25MIL
FB_CMD8	FB_CMD8	25MIL
FB_CMD6	FB_CMD6	25MIL
FB_CMD4	FB_CMD4	25MIL
FB_CMD2	FB_CMD2	25MIL
FB_CMD0	FB_CMD0	25MIL
FB_CMD16	FB_CMD16	25MIL
FB_CMD14	FB_CMD14	25MIL
FB_CMD12	FB_CMD12	25MIL
FB_CMD10	FB_CMD10	25MIL
FB_CMD8	FB_CMD8	25MIL
FB_CMD6	FB_CMD6	25MIL
FB_CMD4	FB_CMD4	25MIL
FB_CMD2	FB_CMD2	25MIL
FB_CMD0	FB_CMD0	25MIL



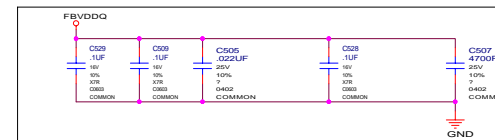
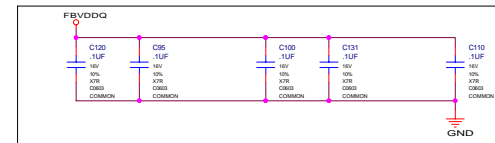
ASSEMBLY PAGE	BASE LEVEL GENERIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BENEFITING FROM THE INVENTION OF THE INVENTOR. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS.
ASSEMBLY PAGE	BASE LEVEL GENERIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BENEFITING FROM THE INVENTION OF THE INVENTOR. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS.

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BENEFITING FROM THE INVENTION OF THE INVENTOR. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS.

Memory Bit 32..63

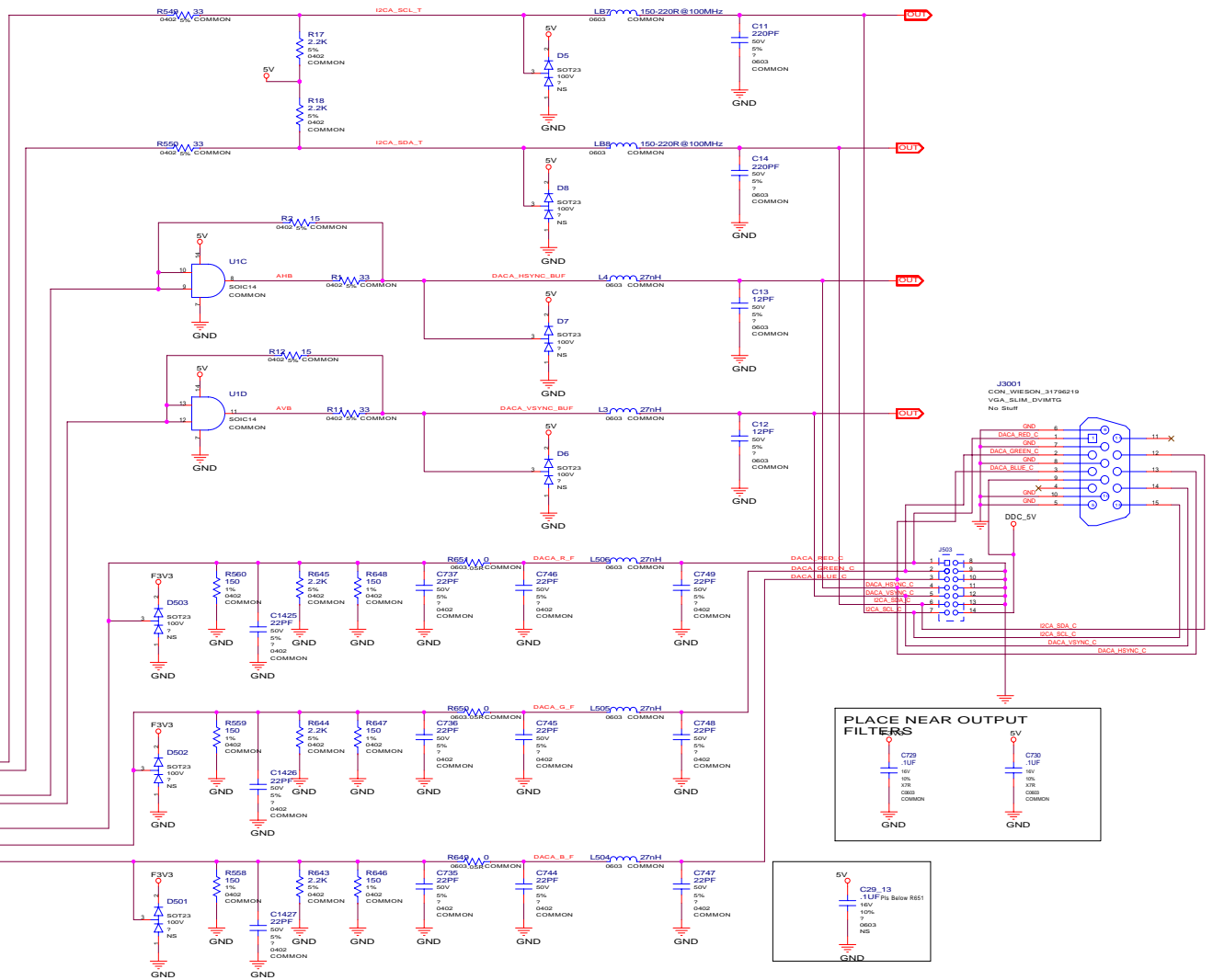
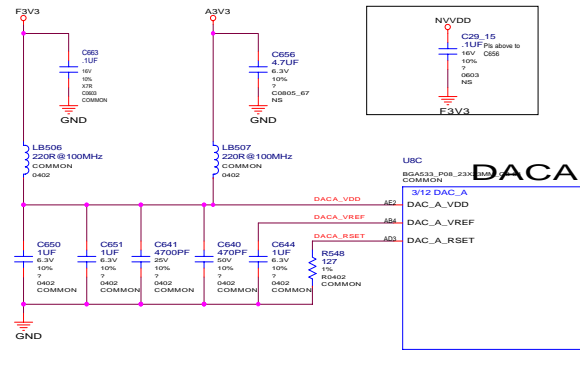
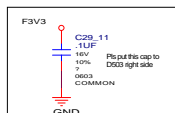
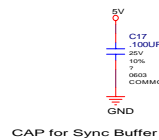


Net	Diffpair	NET_SPACING_RULE
IN	FBACLK1	25MMI
IN	FBACLK1	25MMI
IN	FBIOB3_30	10MMI
IN	FBIOB3_4	10MMI
IN	FBIOB5_7_9	10MMI
IN	FBIOB5_7_9	10MMI



DAC-A, DB15 Connector

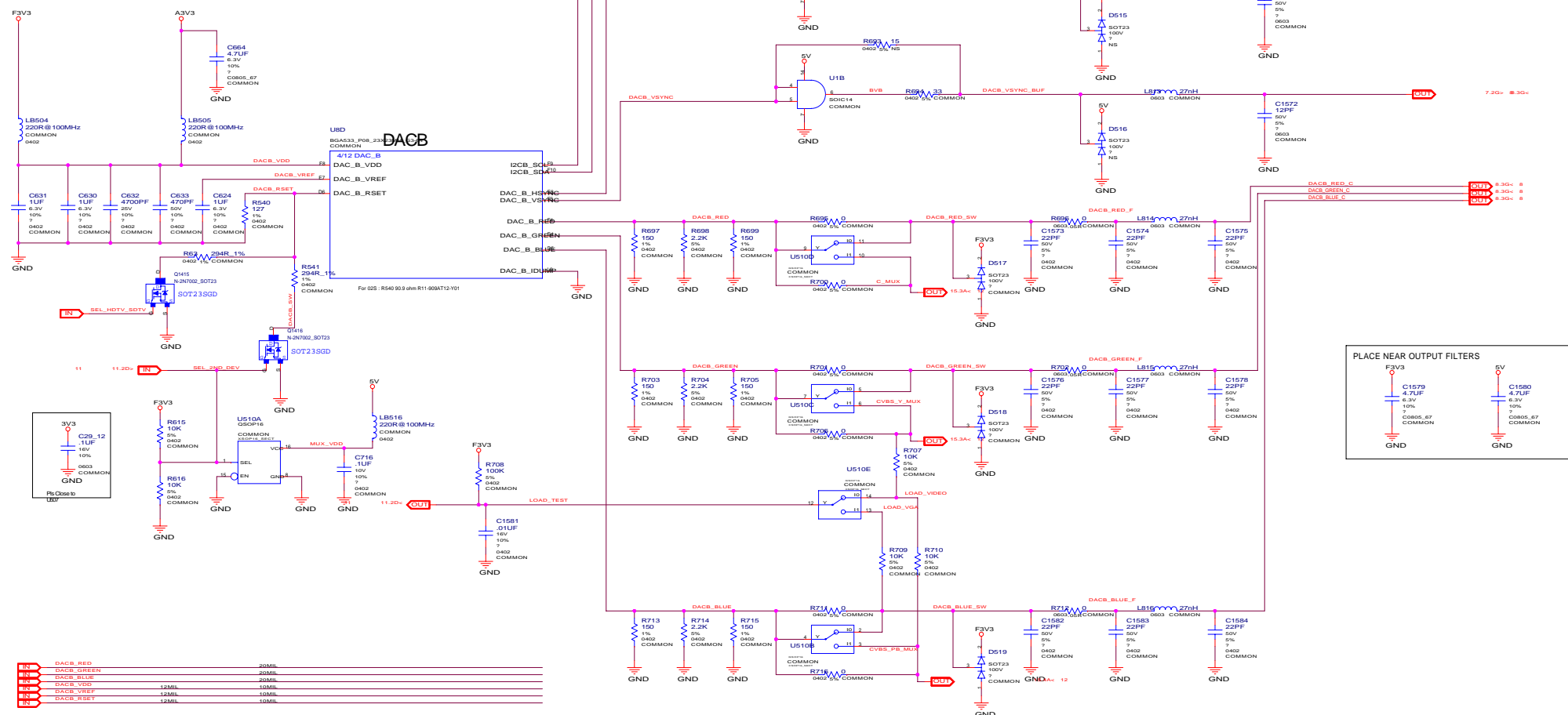
Net		MIN_LINE_WIDTH=NET_SPACING_TYPE
	Name	
R21	DCDC_PSVN	10MIL
R22	DCDC_PSVN2	10MIL
R23	DCDC_PSVN3	10MIL
R24	DCDC_VEN1	10MIL
R25	DCDC_VEN2	10MIL
R26	DCDC_VEN3	10MIL
R27	DCDC_GREEN	20MIL
R28	DCDC_BLUE	20MIL
R29	DCDC_VDD	20MIL
R30	DCDC_VDD	12MIL
R31	DCDC_R_F	20MIL
R32	DCDC_R_F	20MIL
R33	DCDC_B_F	20MIL
R34	DCDC_RED_C	20MIL
R35	DCDC_GREEN_C	20MIL
R36	DCDC_BLUE_C	20MIL



ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND
PAGE	BOM NOT FINAL DATA, DABC, DACC, Sync

					DETAIL	Bulleted
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE	BENEFIT PROVIDER AND ITS MATERIALS MAY	OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED OR IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS.	OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL	LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE		
TRADE PRACTICE, OR INDUSTRY STANDARDS.						

A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

DAC-B, MUX,
DB15

PLACE NEAR OUTPUT FILTERS

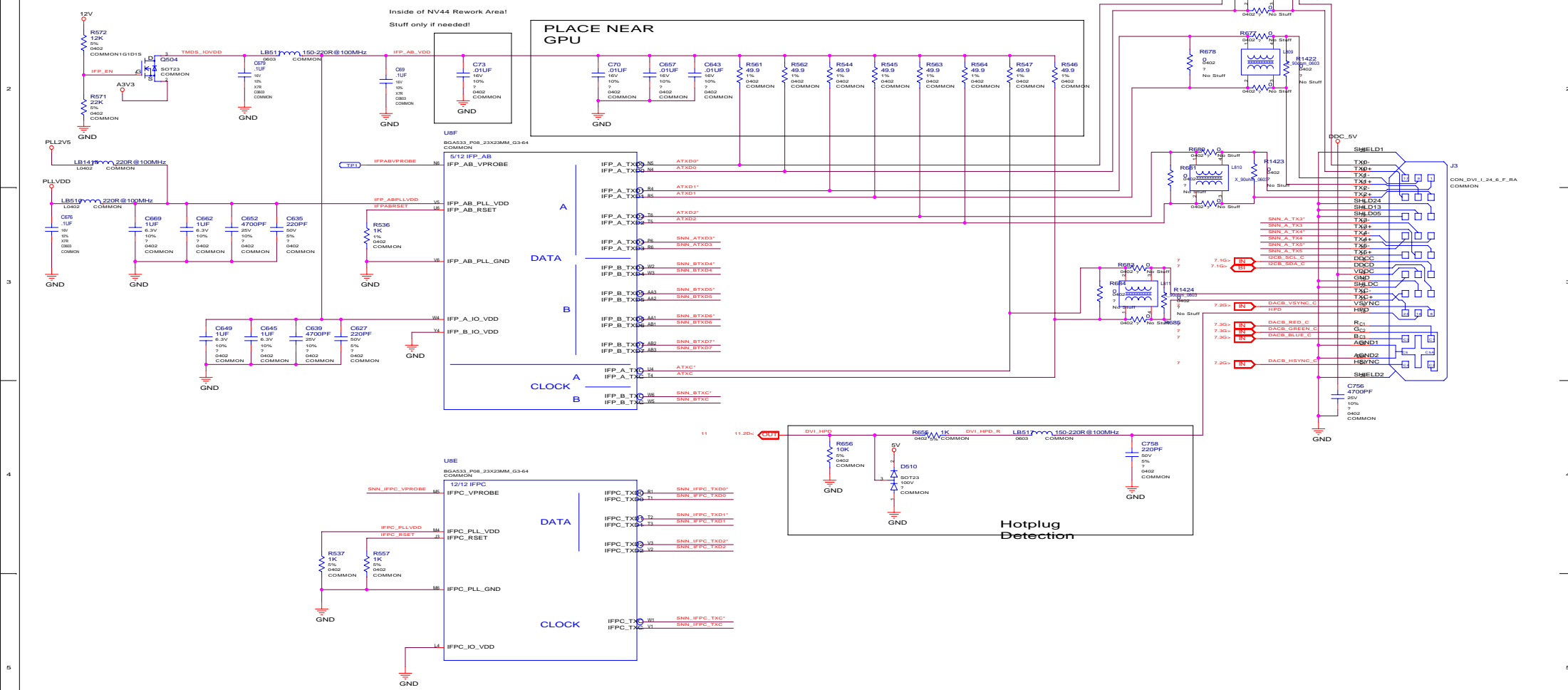
Diagram illustrating the placement of electrolytic capacitors near output filters for two voltage regulators:

- Left Circuit (3V3):** A 3V3 regulator is connected to a 6.3V 10% electrolytic capacitor (C1579, 4.7UF) which is connected to GND. The capacitor is marked with a 7 and COB05, 67 COMMON.
- Right Circuit (5V):** A 5V regulator is connected to a 6.3V 10% electrolytic capacitor (C1580, 4.7UF) which is connected to GND. The capacitor is marked with a 7 and COB05, 67 COMMON.

IN	DACS_RED	20MIL
IN	DACS_GREEN	20MIL
IN	DACS_BLUE	20MIL
IN	DACS_VDD	12MIL
IN	DACS_VREF	10MIL
IN	DACS_RSET	10MIL

Internal TMDs, DVI-Connector

Net Name	Diffpair	NET_SPACING_RULE	voltage
IFP_AB_VDD			3.3V
ATX0	ATX0	25MIL	3.3V
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	
ATX0	ATX0	25MIL	



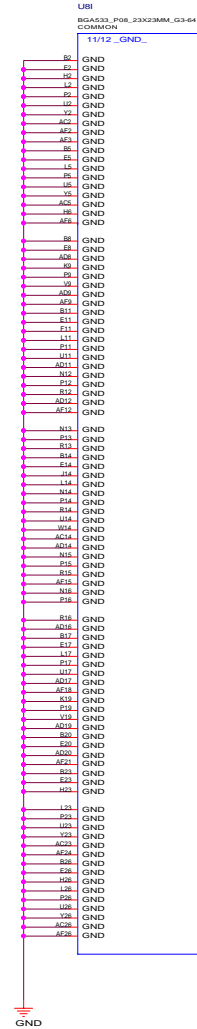
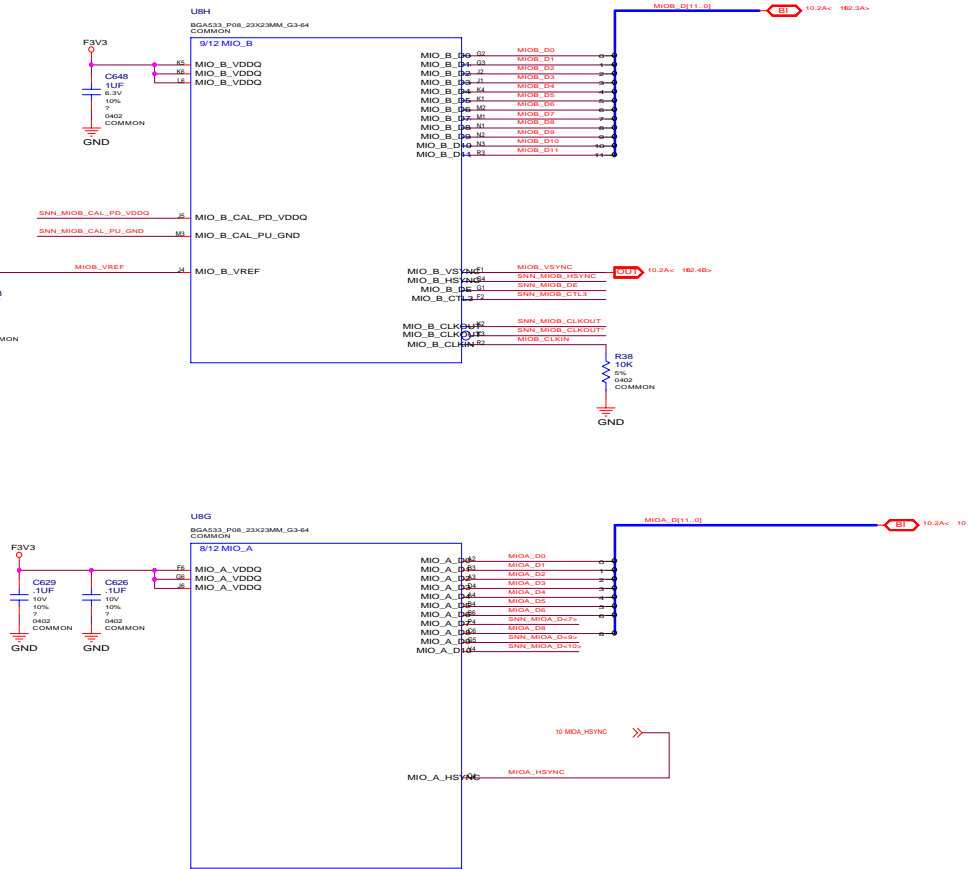
ASSEMBLY PAGE	BASE LEVEL GENERIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND INFORMATION. NOT FINAL
---------------	--

V034

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE HEREBY INCORPORATED BY REFERENCE INTO THIS DOCUMENT. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. NVIDIA DISCLAIMS ALL WARRANTIES, INCLUDING THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, OR CUSTOMER SPECIFICATIONS.

A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

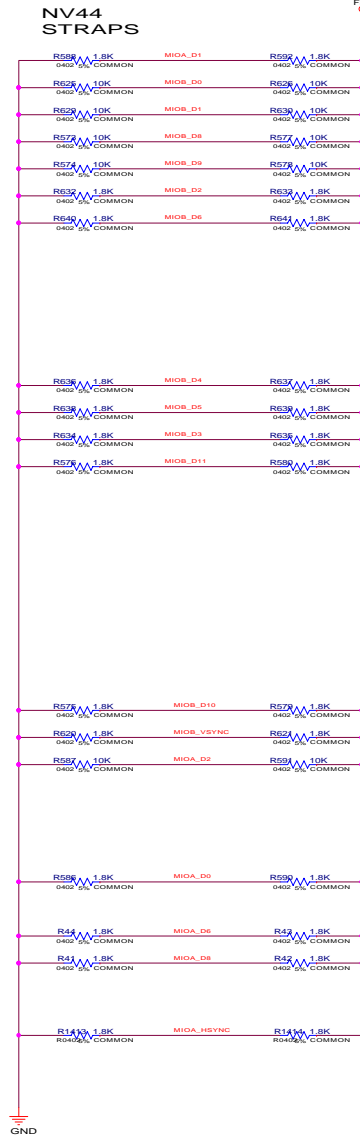
MIOA, MIOB
Interface,
LPC-ROM



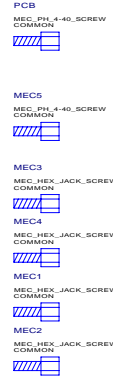
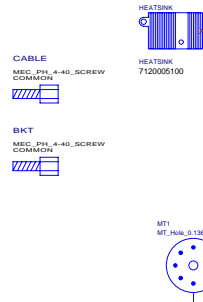
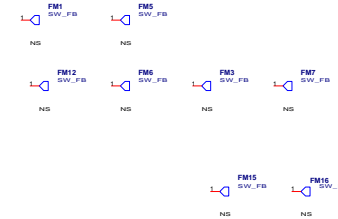
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE
BEING PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS
RENEWED WARRANTIES, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE,
TRADE PRACTICE OR INDUSTRY STANDARDS.

ASSEMBLY
PAGE
LPC-ROM
MIOA, MIOB Interface.

STRAPS, Mechanical Parts

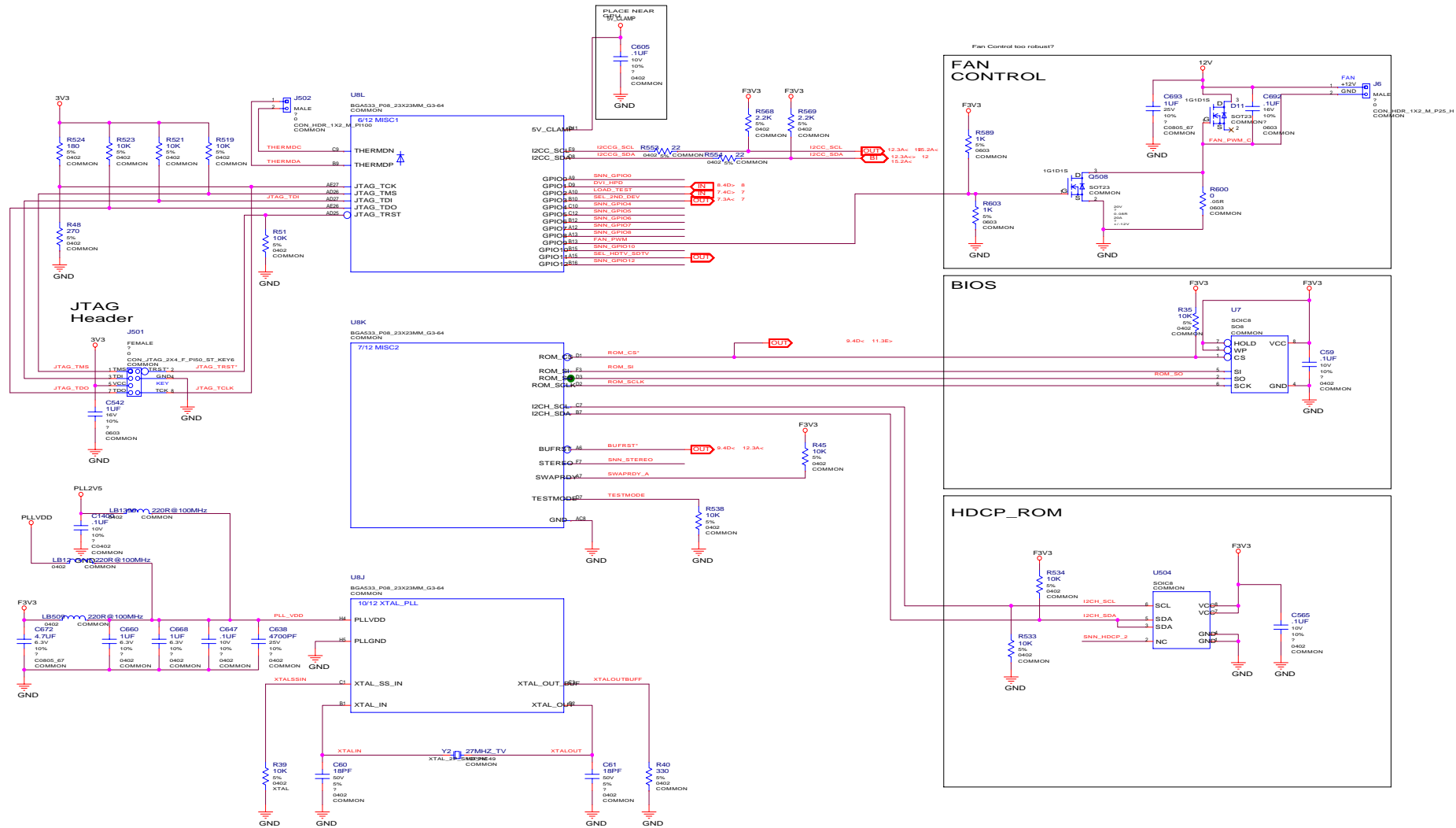


Bit Signal	Values
00: PCI_AD_SWAP	0 REVERSED 1 NORMAL
01: SUB_VENDOR	0 VENDOR FROM 1 VENDOR FROM
02: RAM_CFG_0	0000 1000 0001 8Mbx16DDR WbH 0010 8Mbx16DDR WbH 0011 8Mb WbH 0100 8Mb WbH 0101 8Mb WbH 0110 8Mb WbH 0111 8Mb WbH 1000 8Mb WbH 1001 8Mb WbH 1010 8Mb WbH 1011 8Mb WbH 1100 8Mb WbH 1101 8Mb WbH 1110 8Mb WbH 1111 8Mb WbH
03: RAM_CFG_1	0000 1000 0001 8Mbx16DDR WbH 0010 8Mb WbH 0011 8Mb WbH 0100 8Mb WbH 0101 8Mb WbH 0110 8Mb WbH 0111 8Mb WbH 1000 8Mb WbH 1001 8Mb WbH 1010 8Mb WbH 1011 8Mb WbH 1100 8Mb WbH 1101 8Mb WbH 1110 8Mb WbH 1111 8Mb WbH
04: RAM_CFG_2	0000 1000 0001 8Mbx16DDR WbH 0010 8Mb WbH 0011 8Mb WbH 0100 8Mb WbH 0101 8Mb WbH 0110 8Mb WbH 0111 8Mb WbH 1000 8Mb WbH 1001 8Mb WbH 1010 8Mb WbH 1011 8Mb WbH 1100 8Mb WbH 1101 8Mb WbH 1110 8Mb WbH 1111 8Mb WbH
05: RAM_CFG_3	0000 1000 0001 8Mbx16DDR WbH 0010 8Mb WbH 0011 8Mb WbH 0100 8Mb WbH 0101 8Mb WbH 0110 8Mb WbH 0111 8Mb WbH 1000 8Mb WbH 1001 8Mb WbH 1010 8Mb WbH 1011 8Mb WbH 1100 8Mb WbH 1101 8Mb WbH 1110 8Mb WbH 1111 8Mb WbH
06: CRYSTAL_0	00 13.500 MHz 01 14.31818 MHz 10 27.000 MHz 11 UNKNOWN
22: CRYSTAL_1	00 13.500 MHz 01 14.31818 MHz 10 27.000 MHz 11 UNKNOWN
07: TV_MODE_0	00 2FCAM 01 2FCAM 10 2FCAM 11 2FCAM
08: TV_MODE_1	00 2FCAM 01 2FCAM 10 2FCAM 11 2FCAM
09: AGP_30_Bx	0 AGP30x 1 AGP30x 2 AGP30x 3 AGP30x 4 AGP30x 5 AGP30x 6 AGP30x 7 AGP30x
10: AGP_SBA	0 SBA 1 SBA 2 SBA 3 SBA 4 SBA 5 SBA 6 SBA 7 SBA
11: AGP_FASTWR	0 FW 1 FW 2 FW 3 FW 4 FW 5 FW 6 FW 7 FW
12: PCI_DEVID_0	1100 (default 0x00FC)
13: PCI_DEVID_1	1100 (default 0x00FC)
20: PCI_DEVID_2	1100 (default 0x00FC)
21: PCI_DEVID_3	1100 (default 0x00FC)
14: BUS_TYPE	0 PCI 1 AGP
15: FP_IFACE	0 24Bn 1 12Bn 2 12Bn 3 12Bn 4 12Bn 5 12Bn 6 12Bn 7 12Bn
23: FB_0	0 8M 1 8M 2 8M 3 8M 4 8M 5 8M 6 8M 7 8M
24: FB_1	0 8M 1 8M 2 8M 3 8M 4 8M 5 8M 6 8M 7 8M
25: BR	0 BRIDGE 1 BRIDGE 2 BRIDGE 3 BRIDGE 4 BRIDGE 5 BRIDGE 6 BRIDGE 7 BRIDGE
26: BR_128M	0 BRIDGE 1 BRIDGE 2 BRIDGE 3 BRIDGE 4 BRIDGE 5 BRIDGE 6 BRIDGE 7 BRIDGE
27: BR_AGP	0 BRIDGE 1 BRIDGE 2 BRIDGE 3 BRIDGE 4 BRIDGE 5 BRIDGE 6 BRIDGE 7 BRIDGE
28: BR_IO	0 BRIDGE 1 BRIDGE 2 BRIDGE 3 BRIDGE 4 BRIDGE 5 BRIDGE 6 BRIDGE 7 BRIDGE
29: ROM_TYPE_0	00 0PARALLEL 01 0PARALLEL 10 0PARALLEL 11 0PARALLEL 20 0PARALLEL 21 0PARALLEL 30 0PARALLEL 31 0PARALLEL 40 0PARALLEL 41 0PARALLEL 50 0PARALLEL 51 0PARALLEL 60 0PARALLEL 61 0PARALLEL 70 0PARALLEL 71 0PARALLEL
30: ROM_TYPE_1	00 0PARALLEL 01 0PARALLEL 10 0PARALLEL 11 0PARALLEL 20 0PARALLEL 21 0PARALLEL 30 0PARALLEL 31 0PARALLEL 40 0PARALLEL 41 0PARALLEL 50 0PARALLEL 51 0PARALLEL 60 0PARALLEL 61 0PARALLEL 70 0PARALLEL 71 0PARALLEL
16: USER_0	0000 (DEFAULT)
17: USER_1	0000 (DEFAULT)
18: USER_2	0000 (DEFAULT)
19: USER_3	0000 (DEFAULT)
PEX_FLL_EN_TERM100	
3GIO_PADCFG_LUT_ADDR[0]	
3GIO_PADCFG_LUT_ADDR[1]	



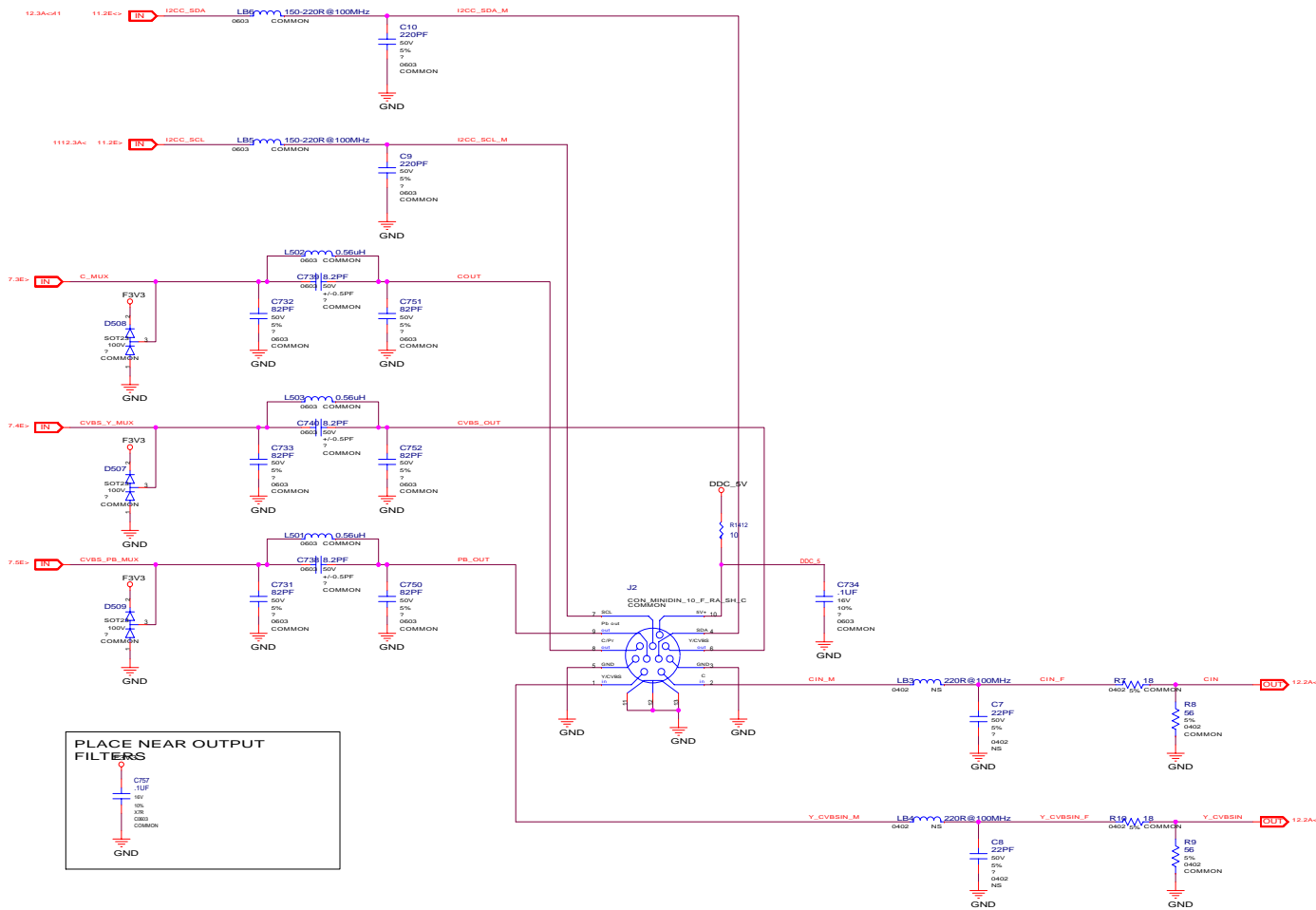
XTAL, GPIO, BIOS, Fan Control, JTAG Headers

Net		NET_PHYSICAL_TYPENET_SPACING_RULE
Name		
R1	NAME	NAME
R2	P_LLCVDD	20MIL_TRACE
R3	P_LLVDD	20MIL_TRACE
R4	DHP_P_LLVDD	12MIL_TRACE
R5	DHP_P_LLVDD	12MIL_TRACE
R6	DHP_P_LLVDD	10MIL_TRACE



VIDEO CONNECTORS: MiniDIN, 2x6 HDR

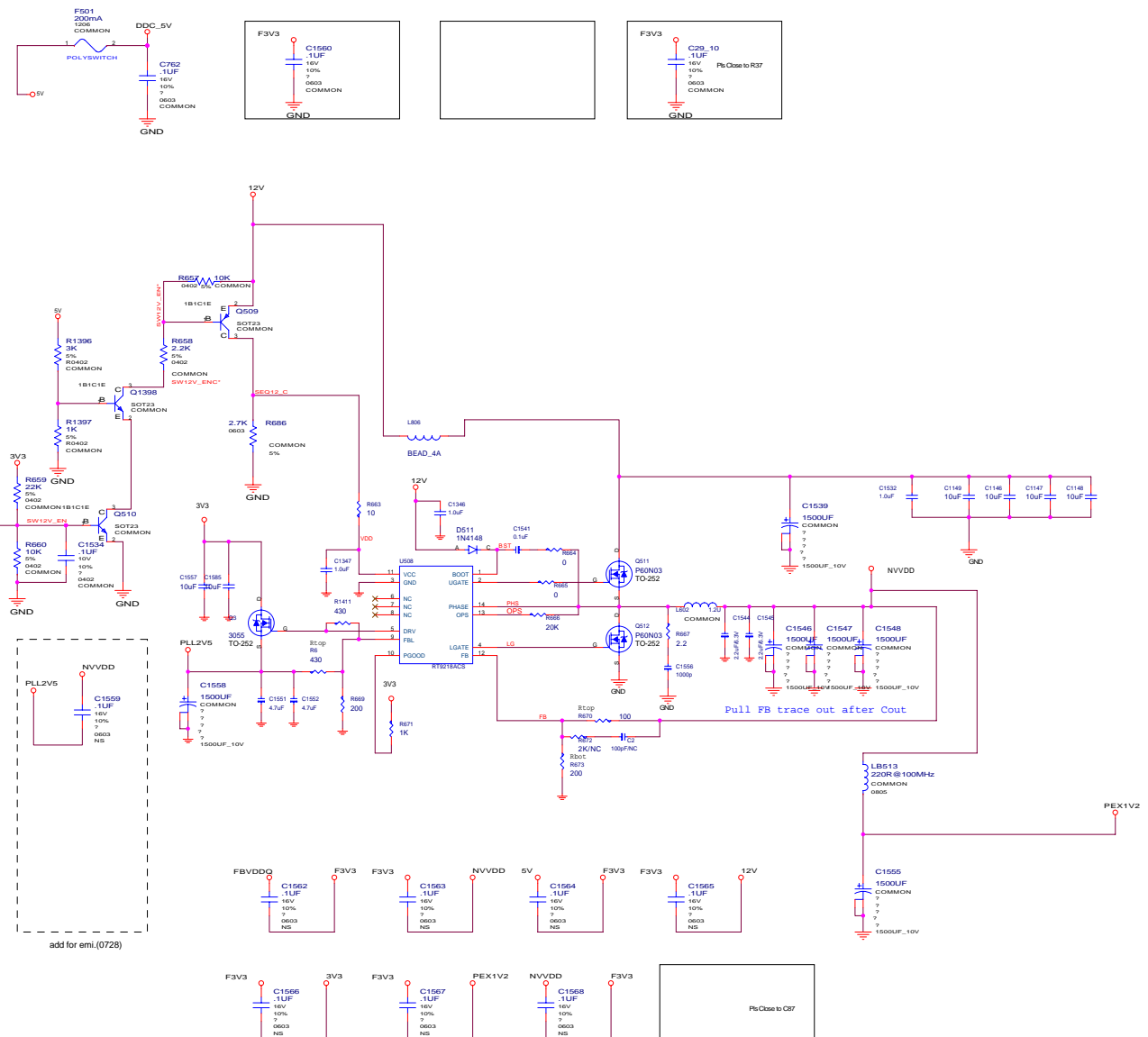
12V SV_FUSED 12MIL 5V



ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND
PAGE	00000000
DETAIL	CONNECTORS: MiniDIN, 2x6 HDR

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARD FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS-IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. NVIDIA DISCLAIMS ALL WARRANTIES, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICES OR INDUSTRY STANDARDS.

PowerSupplyII: 5V, DDC5V, A3V3, F3V3, TMDS_PLLVDD



FBVDDQ

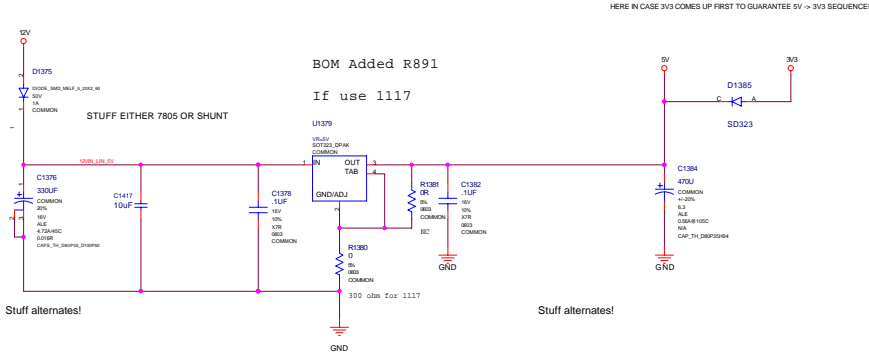
$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$

$1.8V = 0.8V * (1 + (200/160)) \quad (RT9218)$

$2.0V = 0.8V * (1 + (240/160)) \quad (RT9218)$

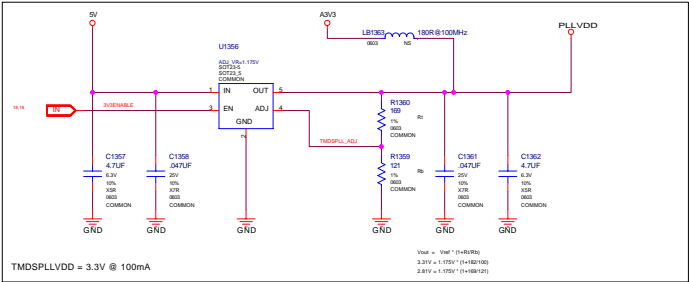
14 Others Power Supply (Linears)

5V,FBVDDQ,A3V3,3V3,TMDS_PLLVDD,TMDS_IOVDD,FBVTT

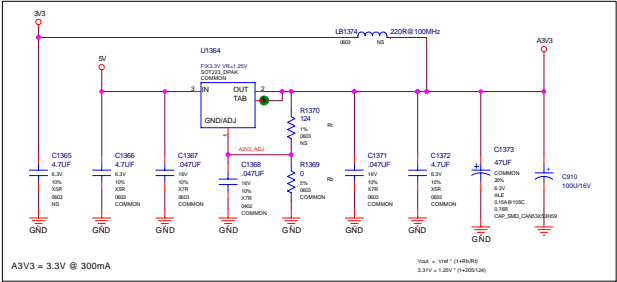


5V LOW COST REGULATOR

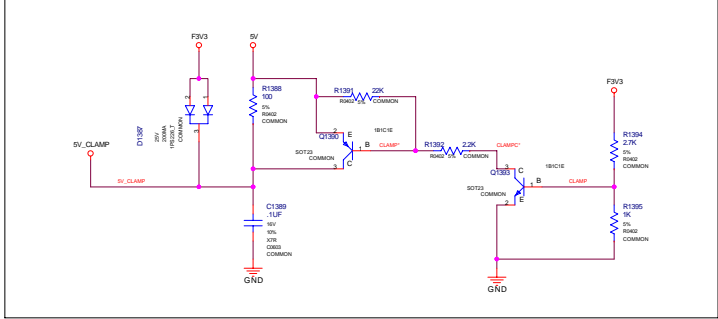
TMDS PLL Supply



A3V3 Power Supply



5V_CLAMP



Power Sequencing

