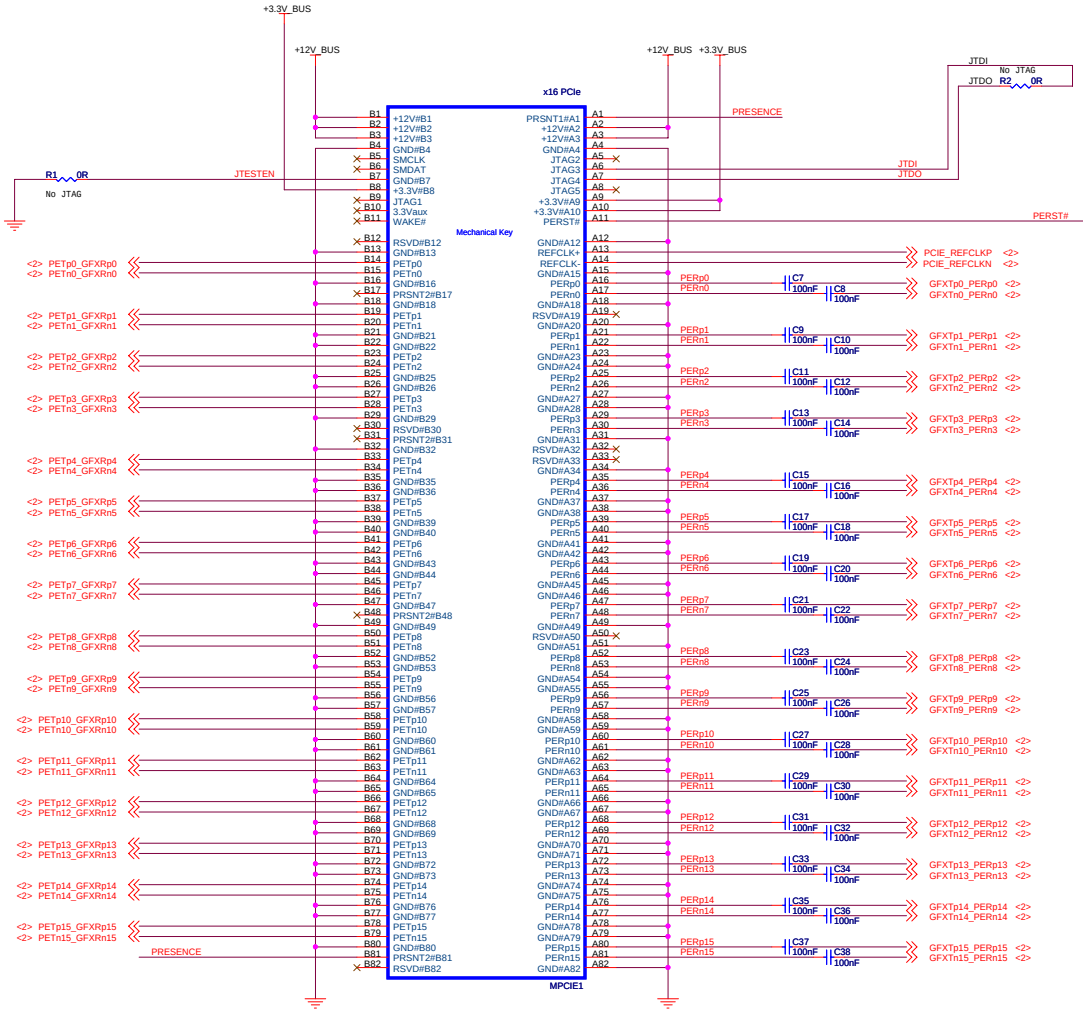
PCI-EXPRESS EDGE CONNECTOR



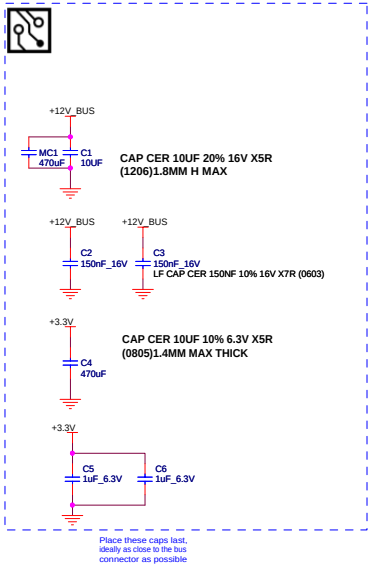


Table 1: Connection for JTAG

Production (No JTAG)	**Install R1, R2 & Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R1 or R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 AND #7 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & #7 closed (ON)**

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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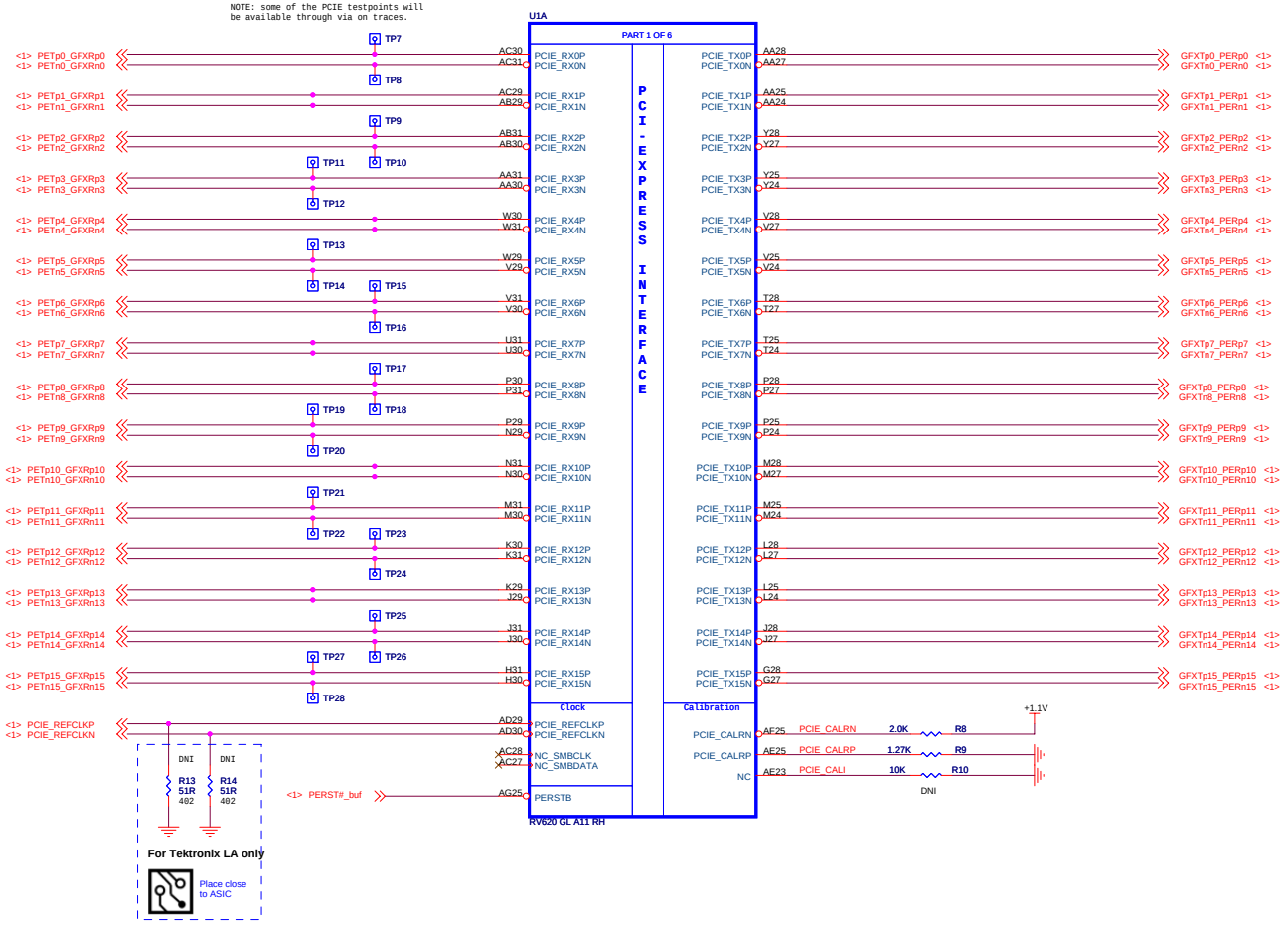
Sheet 1 of 21

Title RH RV620 - PCI-E Edge Connector

Doc No. 105-B408xx-00C



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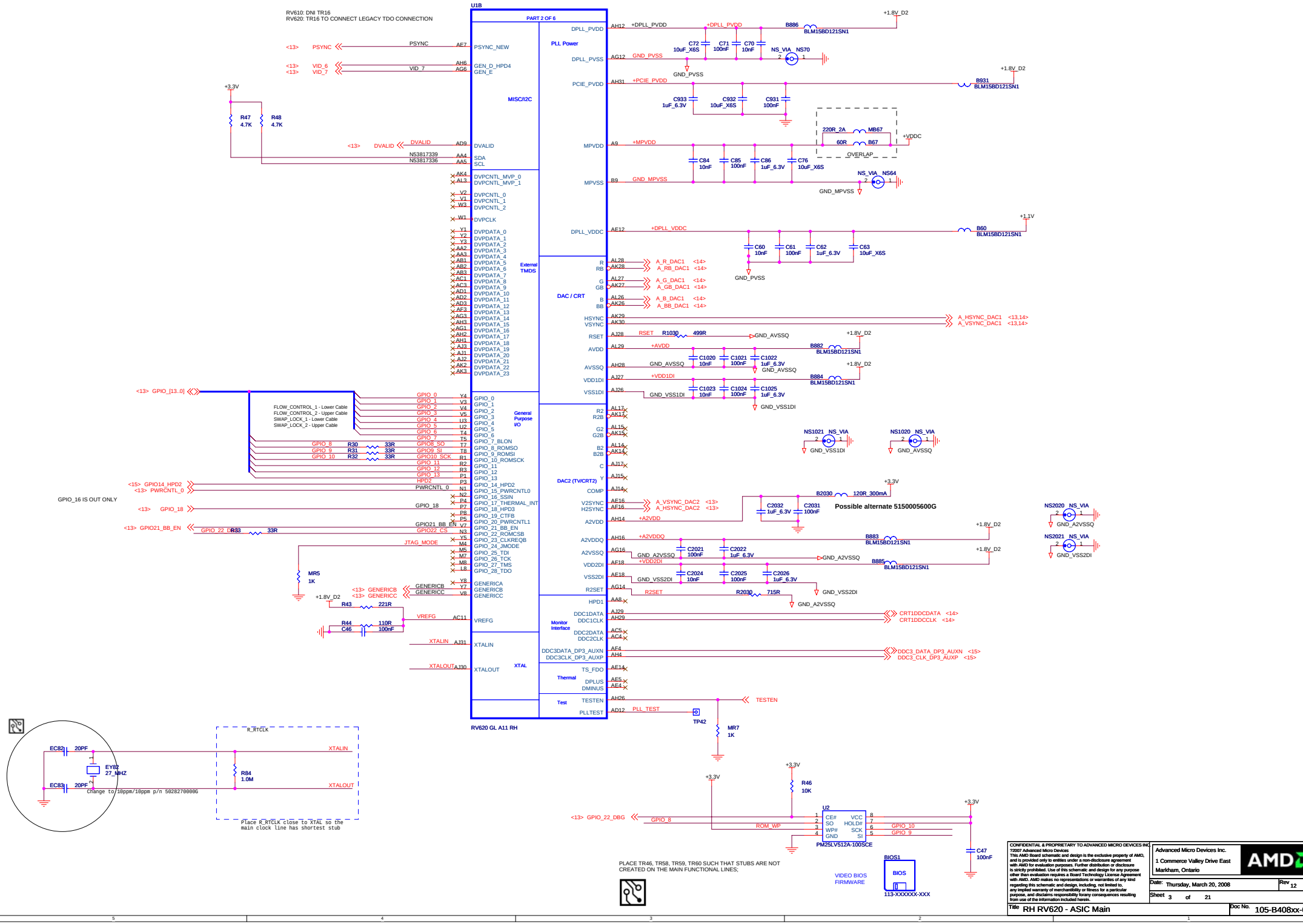
Sheet 2 of 21

Title RH RV610 - ASIC PCIE Interface

Doc No. 105-B408xx-00C


RV610: DNI TR16
RV620: TR16 TO CONNECT LEGACY TDO CONNECTION
U1B
PART 2 OF 6
RV620 GL A11 RH
MISC/I2C
PSYNC
VID_6
VID_7
DVALID
SDA
SCL
External TMDS
DAC / CRT
DAC2 (TV/CRT2)
General Purpose I/O
GPIO_16 IS OUT ONLY
FLOW_CONTROL_1 - Lower Cable
FLOW_CONTROL_2 - Upper Cable
SWAP_LOCK_1 - Lower Cable
SWAP_LOCK_2 - Upper Cable
JTAG_MODE
PLL Power
Monitor Interface
Thermal
Test
XTAL
Possible alternate 5150005600G
R_RTCLK
EY82 27_MHZ
Change to 10ppm/10ppm p/n 5028270000G
Place R_RTCLK close to XTAL so the main clock line has shortest stub
PLACE TR46, TR58, TR59, TR60 SUCH THAT STUBS ARE NOT CREATED ON THE MAIN FUNCTIONAL LINES;
VIDEO BIOS FIRMWARE
PM25LV512A-100SCE
113-XXXXXX-XXX
CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC
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Date: Thursday, March 20, 2008
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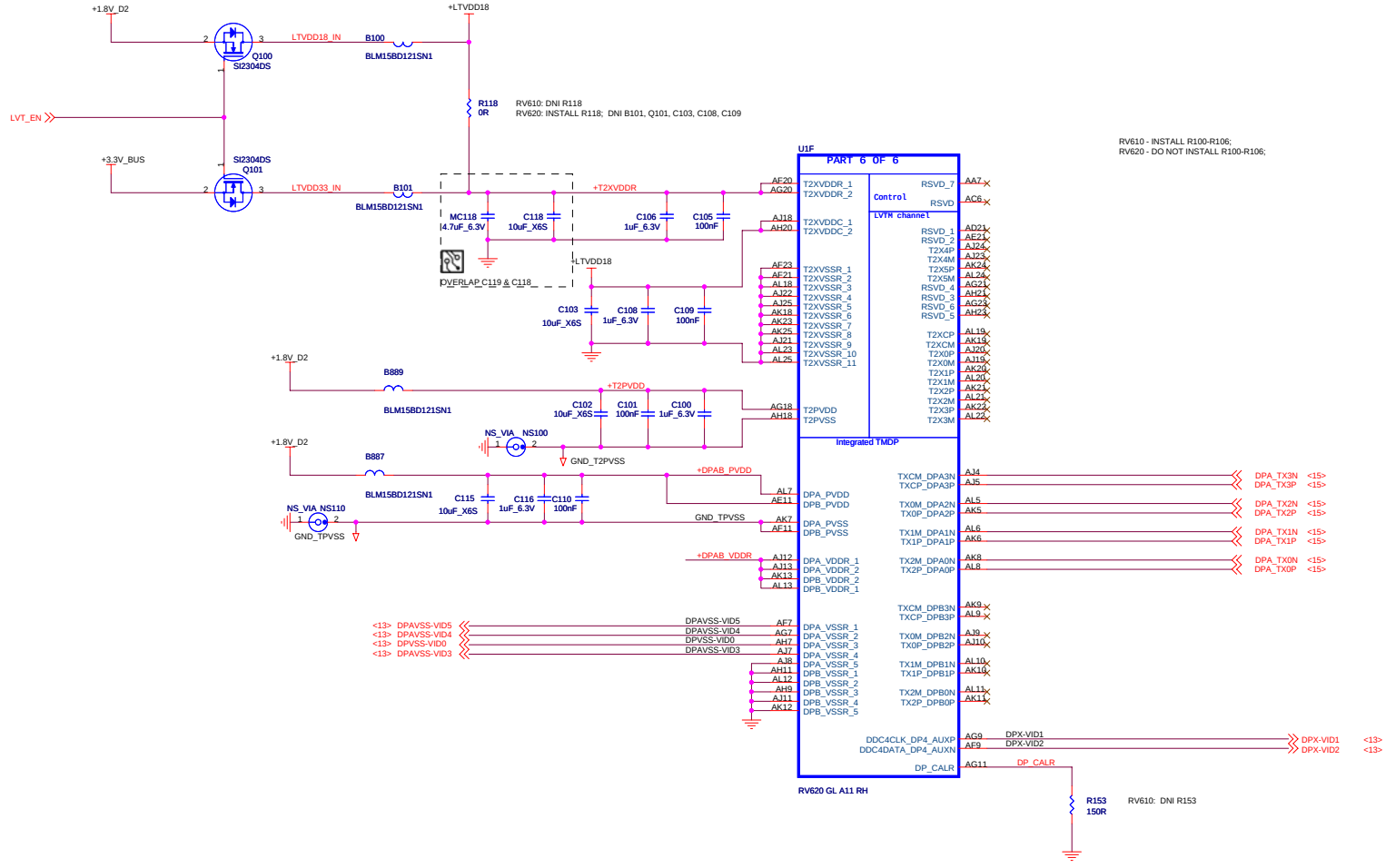
Sheet 3 of 21
Title RH RV620 - ASIC Main
Doc No. 105-B408xx-00C



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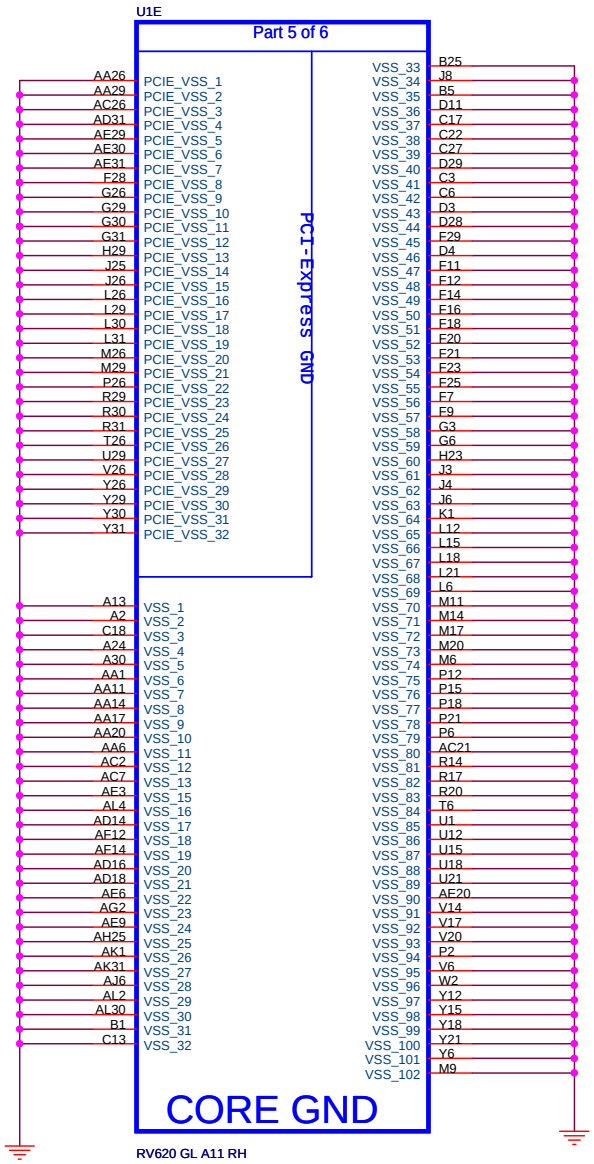
Sheet 4 of 21	
Title RH RV620 - ASIC TMDP/LVTM Interface	Doc No. 105-B408xx-00C



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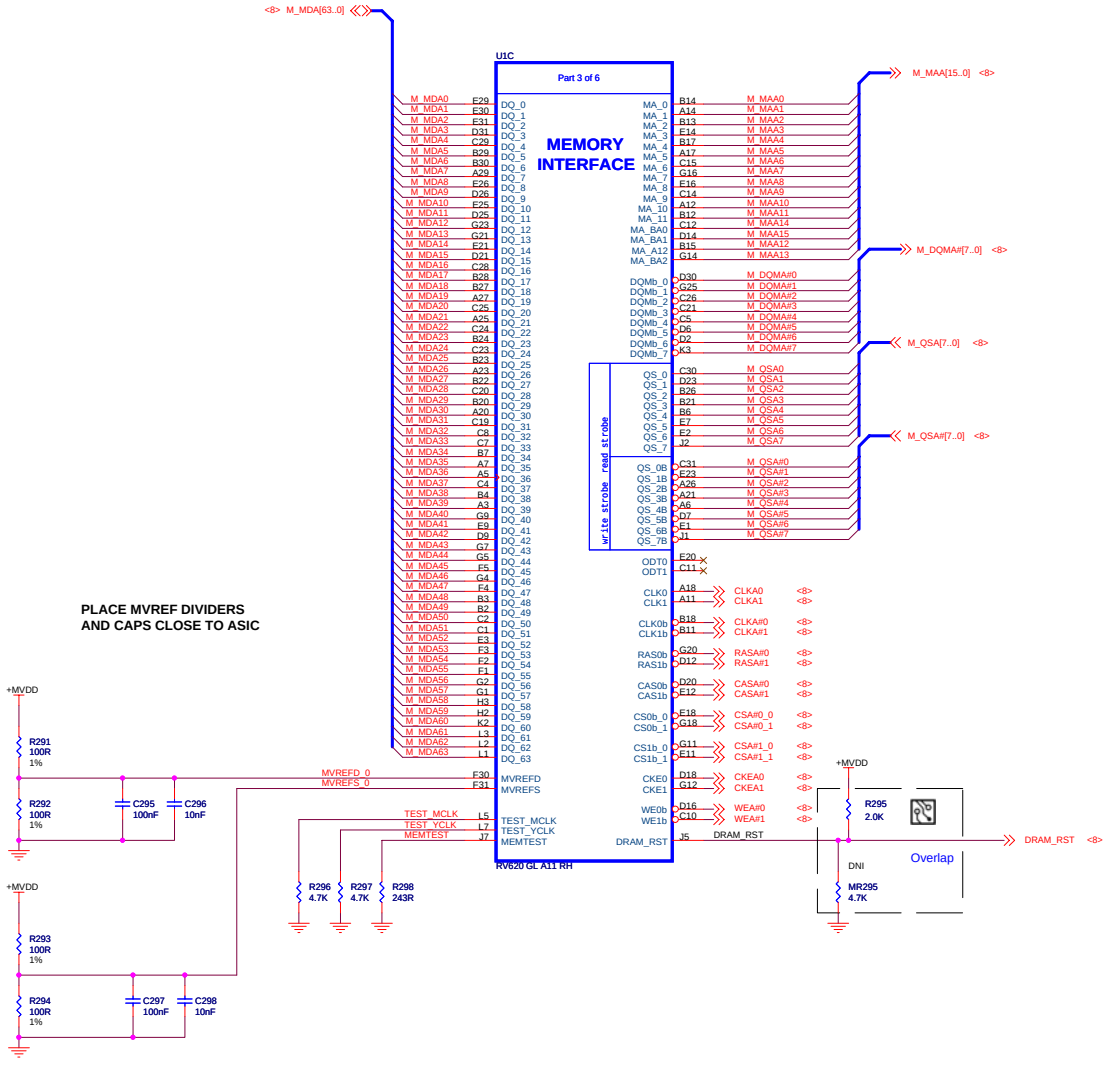
Sheet 5 of 21

Title RH RV620 - ASIC Ground

Doc No. 105-B408xx-00C



DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

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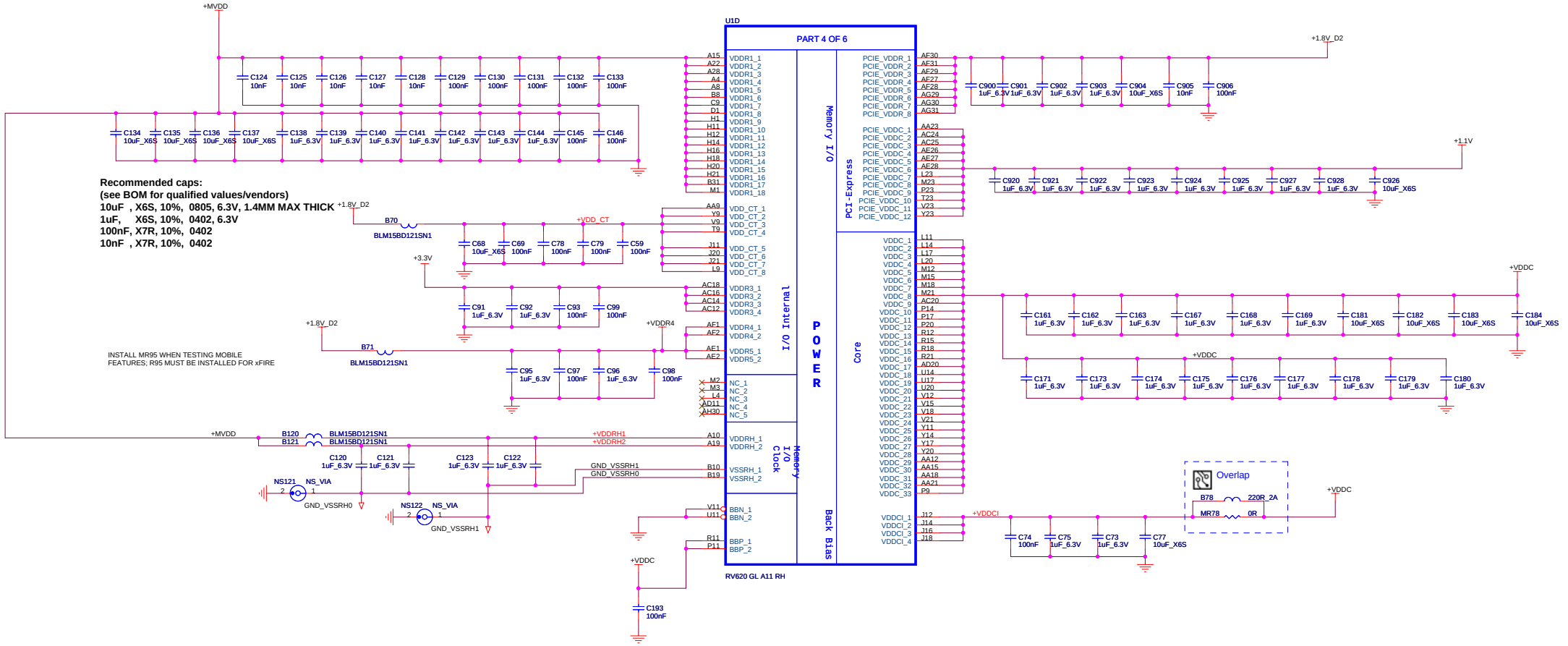
Title RH RV620 - ASIC Memory Interface

Doc No. 105-B408xx-00C



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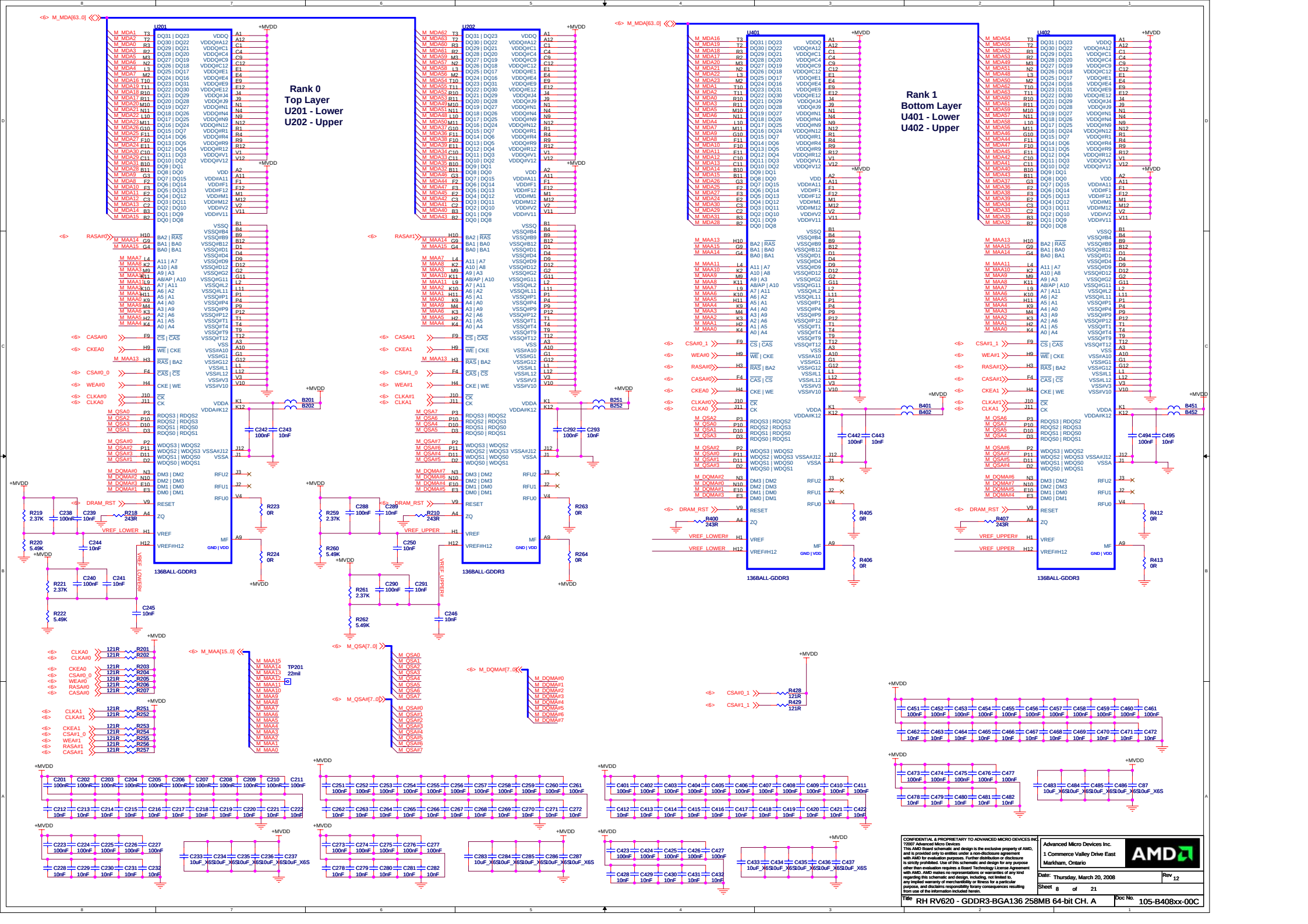
Title: RH RV620 - ASIC Power

Doc No. 105-B408xx-00C



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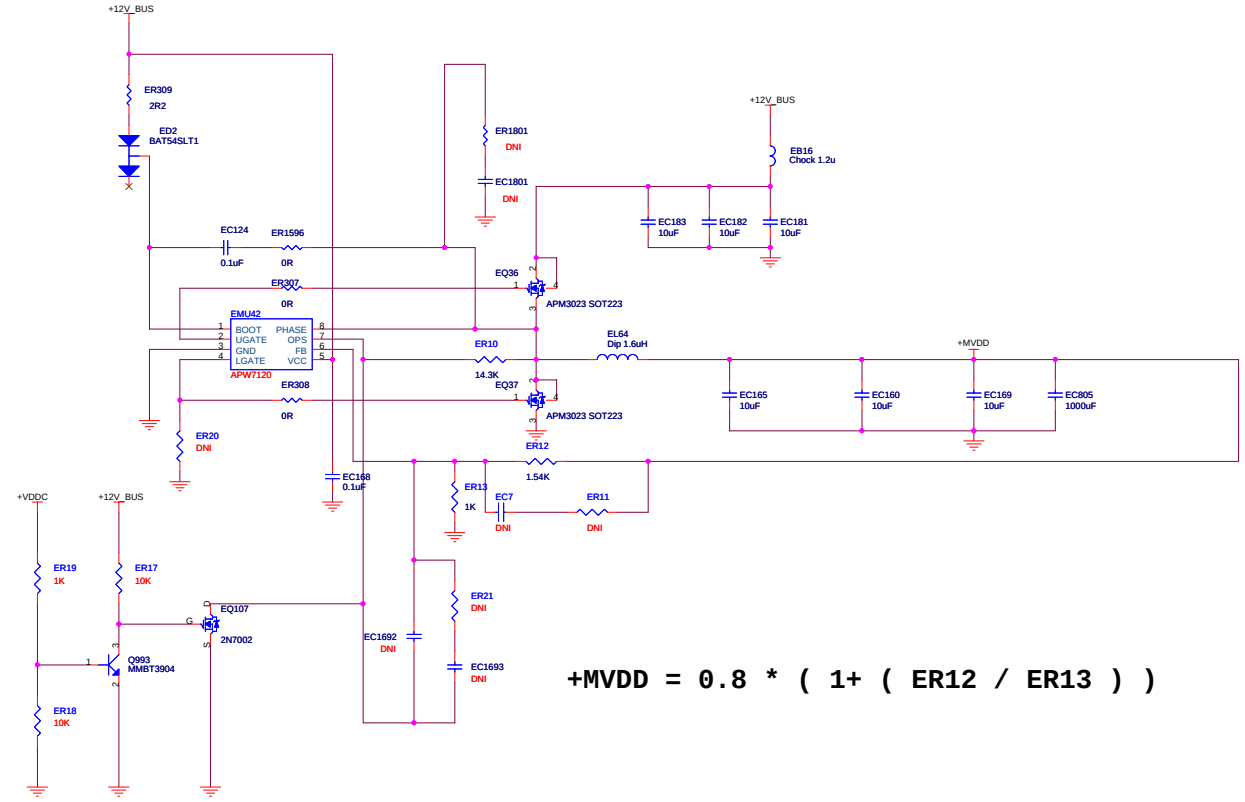
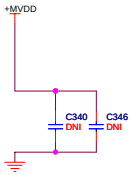
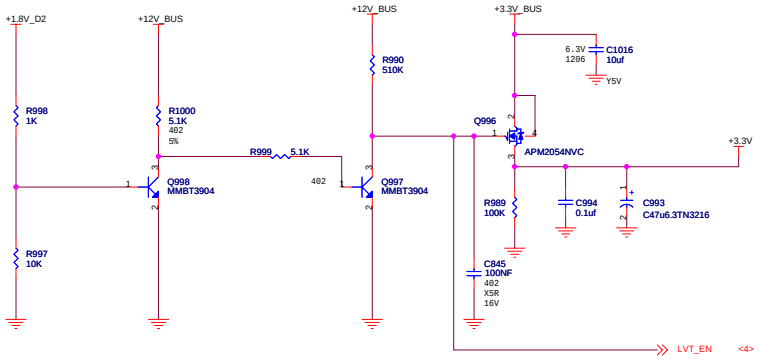
Sheet	8 of 21
Title	RH RV620 - GDDR3-BGA136 258MB 64-bit CH. A
Doc No.	105-B408xx-00C

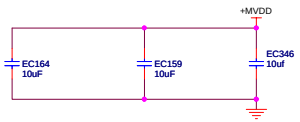


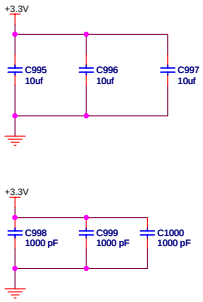
+MVDD = 0.8 * (1+ (ER12 / ER13))

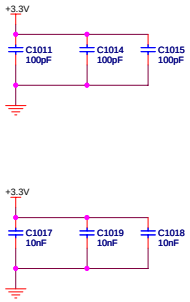


Memory Power Seq









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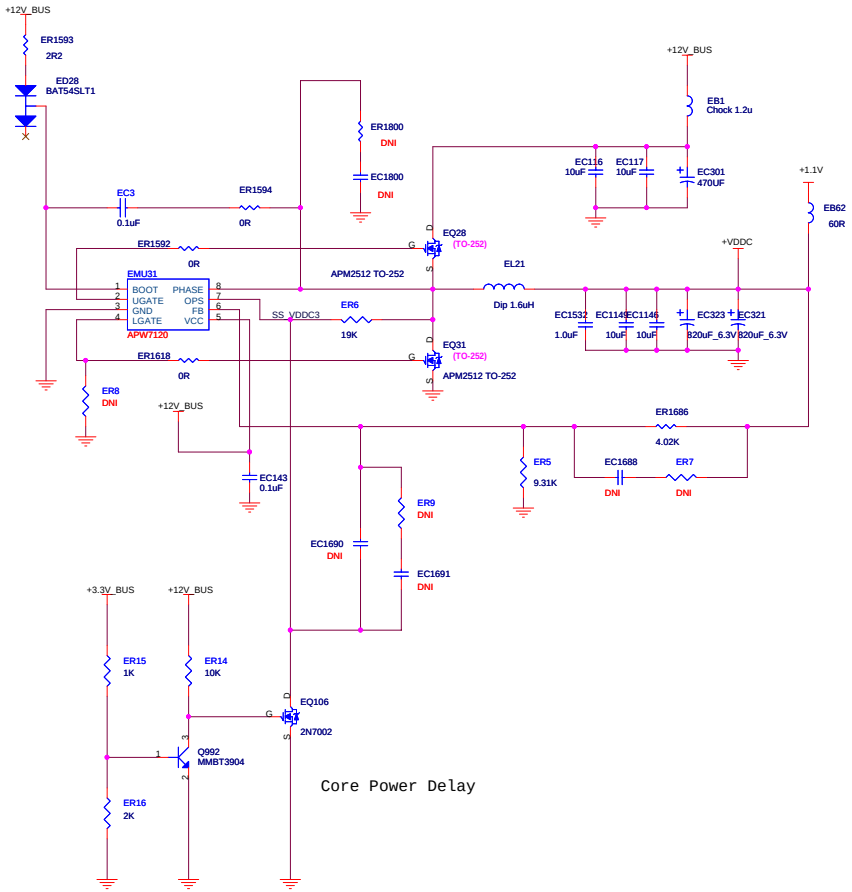
Title RH RV620 - MVDD SMPS

Doc No. 105-B408xx-00C

CORE REGULATOR +VDDC



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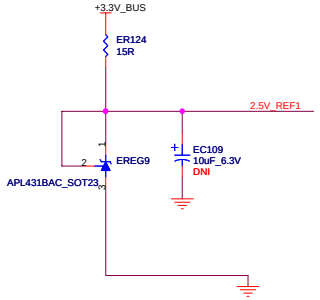
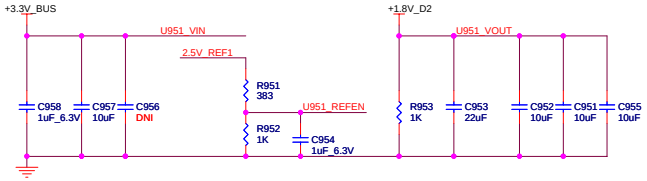
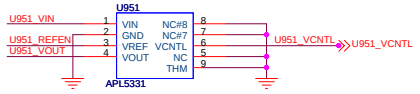
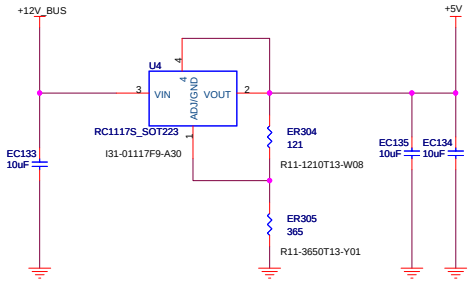
Sheet	10 of 21
Title	RH RV620 - VDDC SMPS
Doc No.	105-B408xx-00C

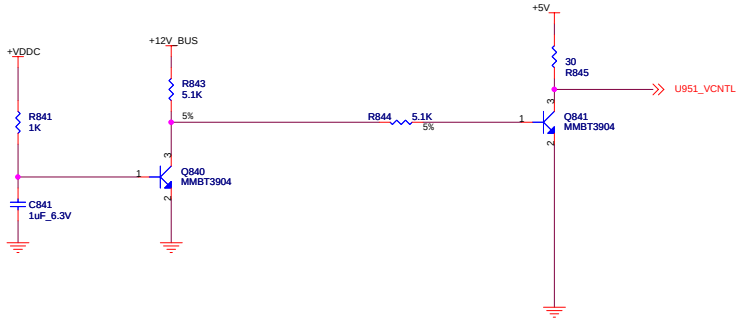


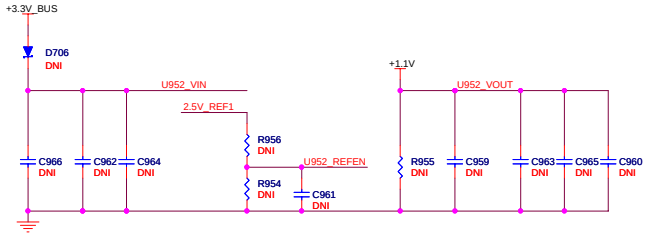


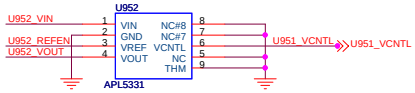




Vout=1.25V* [1+(ER305/ER304)]







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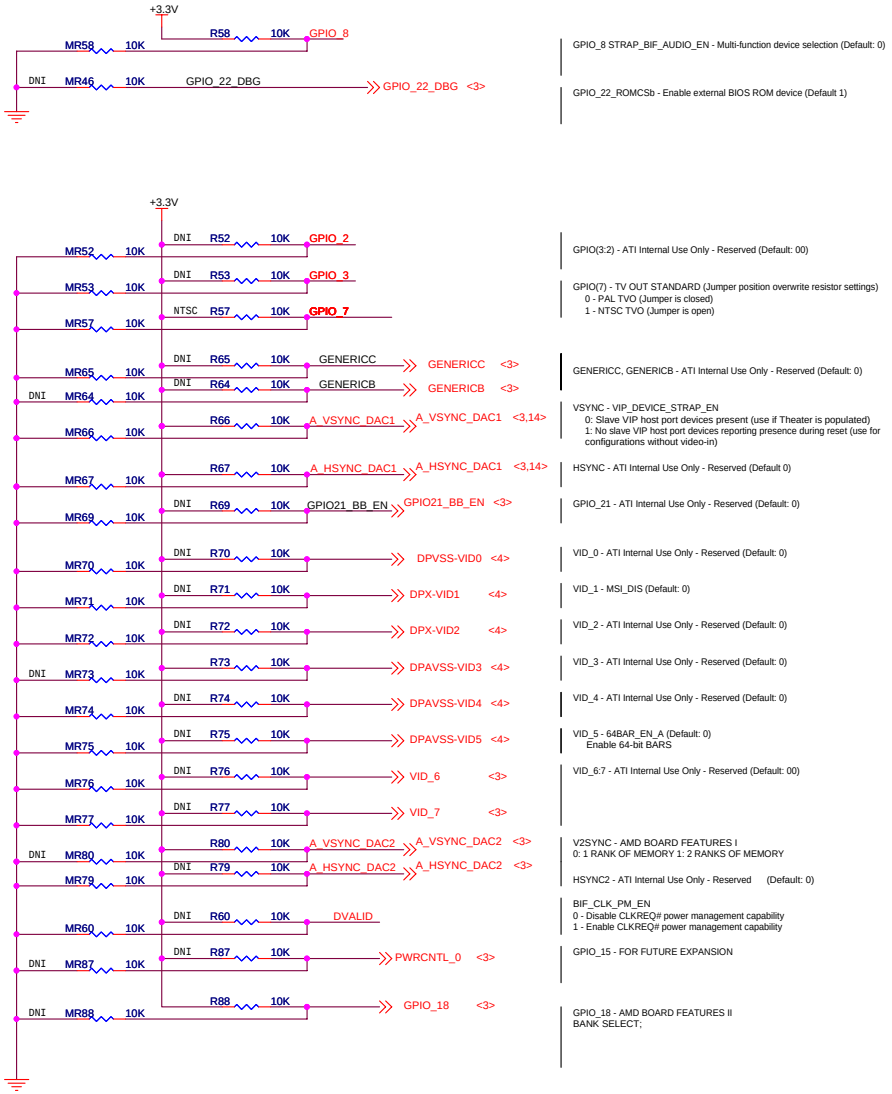
Title RH RV620 - LINEAR REGULATORS Doc No. 105-B408xx-00C

PIN BASED STRAPS



PSYNC <3>
DVALID <3>

GENERICB <3>
GENERICC <3>

DE for Lower Cable

DVP_MVP_CNTL_R_0 - DE for bits D[12..23]
DVP_MVP_CNTL_R_1 - CLK for bits D[12..23]

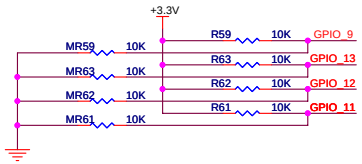
GPIO_3 - FLOW_CONTROL_1 - Lower Cable
GPIO_4 - FLOW_CONTROL_2 - Upper Cable
GPIO_5 - SWAP_LOCK_1 - Lower Cable
GPIO_6 - SWAP_LOCK_2 - Upper Cable

ROM CONFIG PIN STRAPS

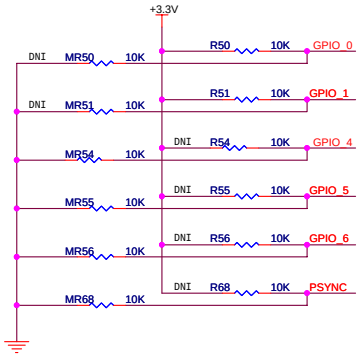
GPIO(9,13:11) - CONFIG[3..0] IF BIOS_ROM_EN=1 [default] (GPIO_22)
tmel - AT25F512A (512 kbit)0010
AT25F1024A (1 Mbit)0011
ST Microelectronics- M25P05A (512 kbit) 0100
M25P10A (1 Mbit) 0101
M25P20 (2 Mbit) 0101
Chingis (formerly PMC) -
Pm25LV512 (512 kbit) 0100
Pm25LV010 (1 Mbit) 0101

If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. (Config 3 = don care).
x000 128MB
x001 256MB
x010 64MB
x011 32MB
x100 512MB
x101 1GB
x110 2GB
x111 4GB

PLEASE CONTACT AMD FOR ALL QUALIFIED ROM DEVICES.



AMD INTERNAL STRAPS - BUO



PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(4) - DEBUG_ACCESS (ATI Internal Use Only - Reserved (Default: 0))
GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)
GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)

Pull-Down Resistors are for BU until built-in pull-downs are verified.

<3> GPIO_[13..0]
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_11
GPIO_12
GPIO_13

RV610:
RV620: R71, R72 MUST BE INSTALLED. MR70, MR73, MR74, MR75 _MUST_ BE INSTALLED 0 OHM.

RV610: INSTALL MR58
RV620: INSTALL R58

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground High logic voltage

Signal

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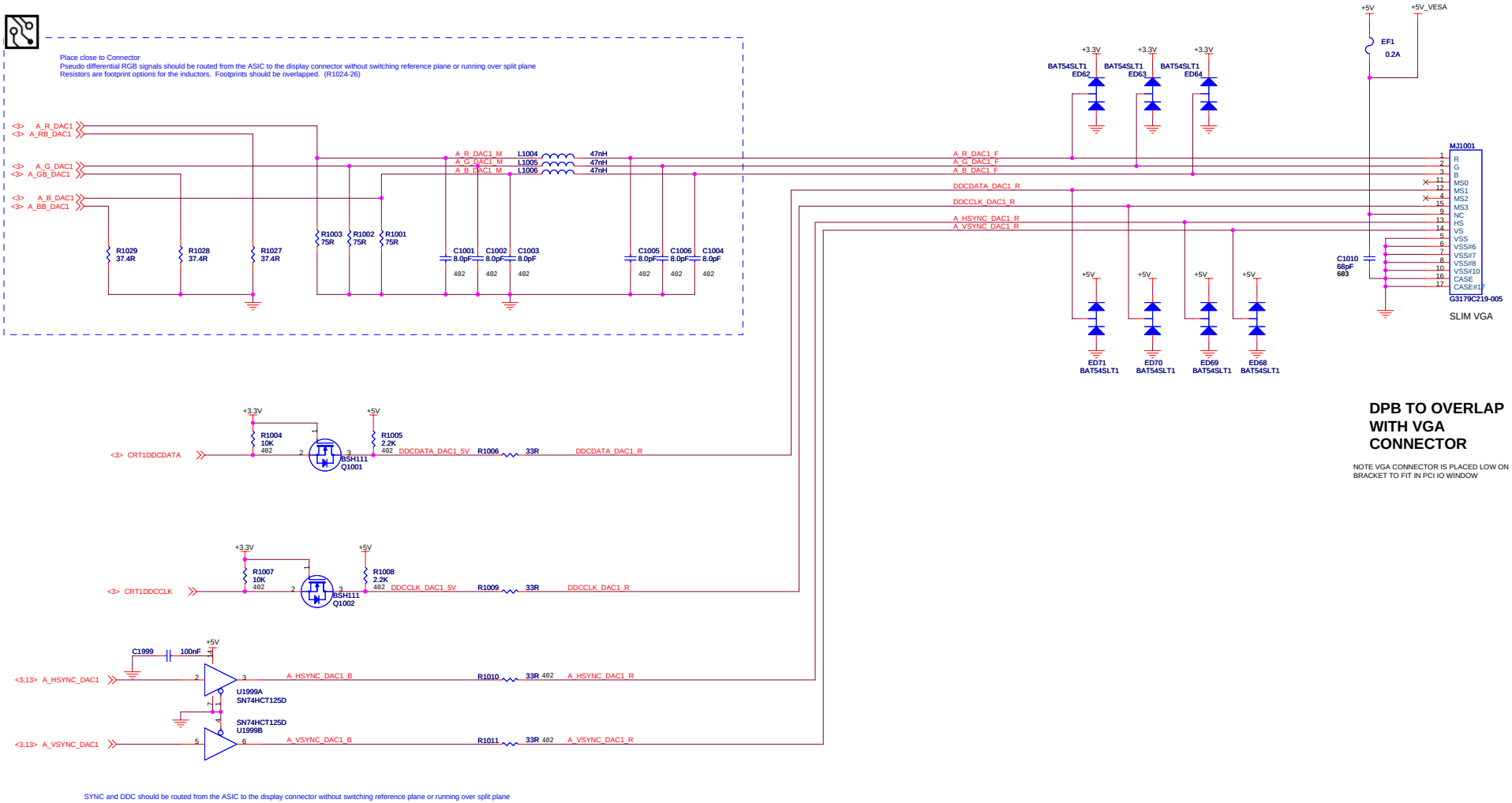
Title RH RV620 - STRAPS AND CROSSFIRE

Doc No. 105-B408xx-00C



DPB TO OVERLAP WITH VGA CONNECTOR

NOTE VGA CONNECTOR IS PLACED LOW ON BRACKET TO FIT IN PCI IO WINDOW

DAC_1-CRT

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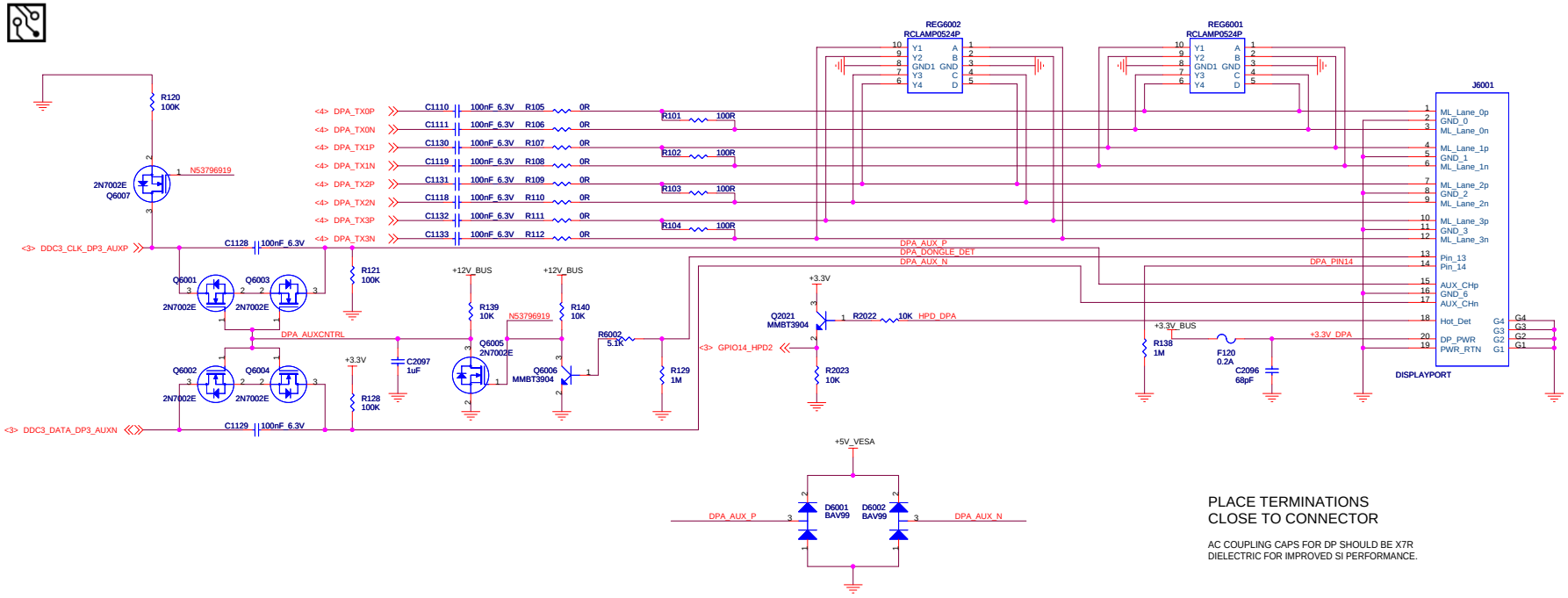
Title RH RV620 - DAC2 Doc No. 105-B408xx-00C



PLACE TERMINATIONS
CLOSE TO CONNECTOR

AC COUPLING CAPS FOR DP SHOULD BE X7R
DIELECTRIC FOR IMPROVED SI PERFORMANCE.

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Title RH RV620 - TVO, DAC1

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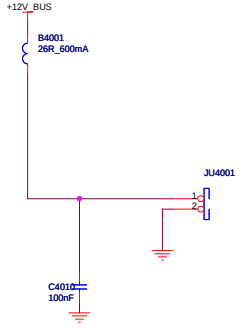

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Title RH RV620 - THERMAL MANAGEMENT | Doc No. 105-B408xx-00C

DVI/VGA SCREWS

ASSY-SCREW1

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW5

SCREW

SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

ASSY-SCREW3

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW2

SCREW

ASSY
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT

ASSY-SCREW4

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY1

BRACKET

8020046300G

BRACKET, TOP TAB
DVI, VGA, DIN

ASSY2

BRACKET

8020044300G

BRACKET, TOP TAB
DVI, DVI, DIN

SK1

BGA_Socket_RV620

FM1
SW_FB

FM4
SW_FB

FM2
SW_FB

FM5
SW_FB

FM3
SW_FB

FM6
SW_FB

J1

X_PIN1*2

J4

X_PIN1*2

J7

X_PIN1*2

J2

3 1
4 2

impedence

J8

X_PIN1*2

J5

3 1
4 2

impedence

J11

3 1
4 2

impedence

J10

X_PIN1*2

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Title RH RV620 - MECHANICAL

Doc No. 105-B408xx-00C

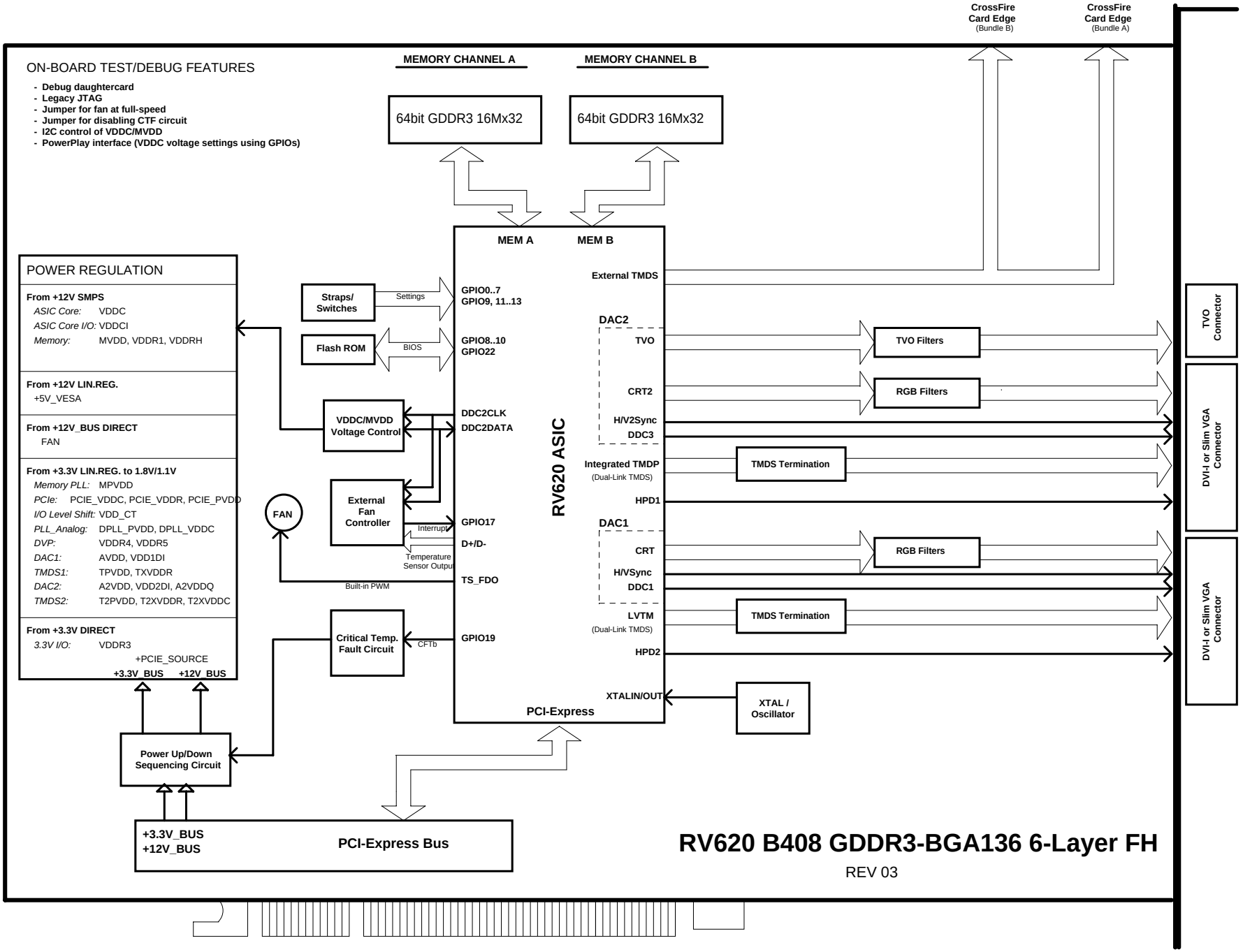
Title	Schematic No.	Date:
RH PCIE RV670 512MB GDDR4 DUAL DL-DVI-I VO FH	105-B408xx-00C	Thursday, March 20, 2008

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 12

Sch Rev	PCB Rev	Date	REDSTAR REVISION DESCRIPTION
01	00A	2007.07.30	START NEW SCHEMATIC. DERIVED FROM B368rev25 SCHEMATIC. REMOVING SPECIFIC HWQ TESTING CIRCUITRY, LVDS OUTPUT, BACKBIAS AND SPREAD SPECTRUM; ADD U1210 FOR MVDD I2C CONTROL (REDUCE STUBS);
02	00A	2007.07.30	FIXED GPIO_22_DBG/+3.3V SHORT (p.13); UPDATE BLOCK DIAGRAM (p. 99);
03	00A	2007.08.10	ADD R85, R838; REMOVE REG861, R869, R867, C867, MR861, R862, MR862; ADD R1012, R2012; CHANGE D1001, D2001 TO *_BUS; FAN - ADD R4019, R4031, REMOVE PLUG/JUMPER;
04	00A	2007.08.13	REMOVE R47, R48;
05	00A	AUG 14 2007	CHANGE U1200, U1210 TO +3.3V;
06	00B	SEP 12 2007	ADD R1 FOR NO JTAG PRODUCTION OPTION. CONNECT JTESTEN TO TSW1.7 FOR EASY GROUNDING; p12 - REMOVE +5V REGULATOR - WAS NOT USED, SCHEM MISTAKE; CHANGE R1226/R1225 TO 0402 (NO NEED FOR LARGER SIZE); CONNECT J1001 TO HPD2 - CORRECT MISTAKE;
07	00B	SEP 18 2007	ADD C812 FOR TEST ONLY;
08	00B	SEP 18 2007	UPDATE BRACKETS; UPDATE BLOCK DIAGRAM;
09	00C	NOV 12 2007	p. 18 - REMOVE JU1250 - OPTION TO DISABLE NO LONGER REQUIRED, FEATURE IS A GO; p. 14 - ADD OPTIONAL ESD PROTECTION DIODES
10	00C	NOV 14 2007	p. 14 - PIN SWAP REG6001-4 FOR LAYOUT EASEMENT
11	00C	NOV 14 2007	p. 4 - ASIC SYMBOL UPDATED - BALL NAMES FOR DESKTOP CHANGED TO REFLECT DP ROUTING; p. 4 - SCHEMATIC NOTE UPDATED TO REFLECT C110-C1127 SHOULD BE 100nF (NOTE HAD STATED 180nF PREVIOUSLY)
12	00C	NOV 14 2007	p. 4 - CHANGE NET NAMES TO REFLECT NEW SYMBOL BALL NAMES;



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Title RH RV620 - BLOCK DIAGRAM	Doc No. 105-B408xx-00C