

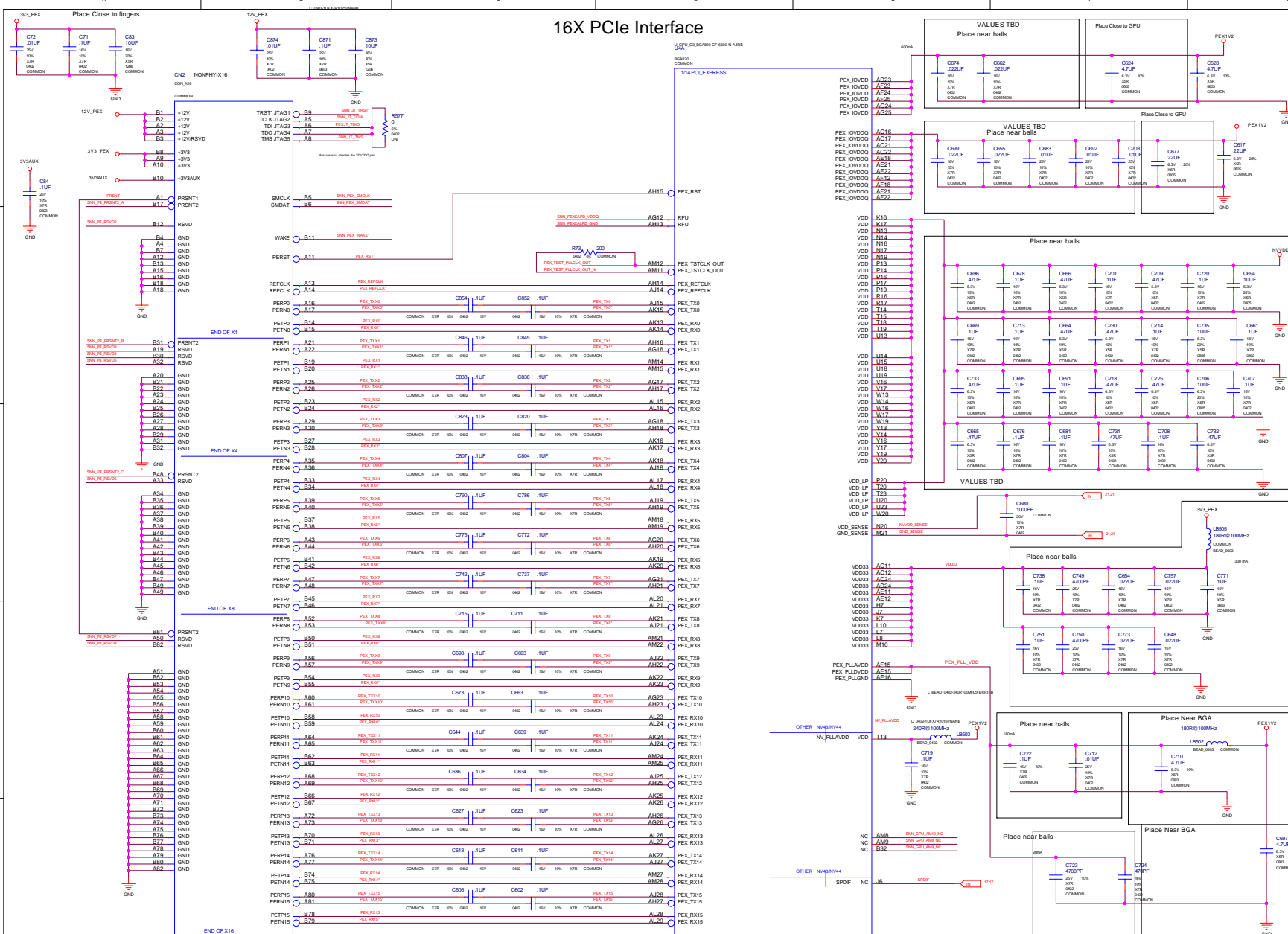
P345-A01 DESIGN -- G73, 256 MB DDR2, VGA, DVI-I, HDTV, VIVO

PAGE SUMMARY:

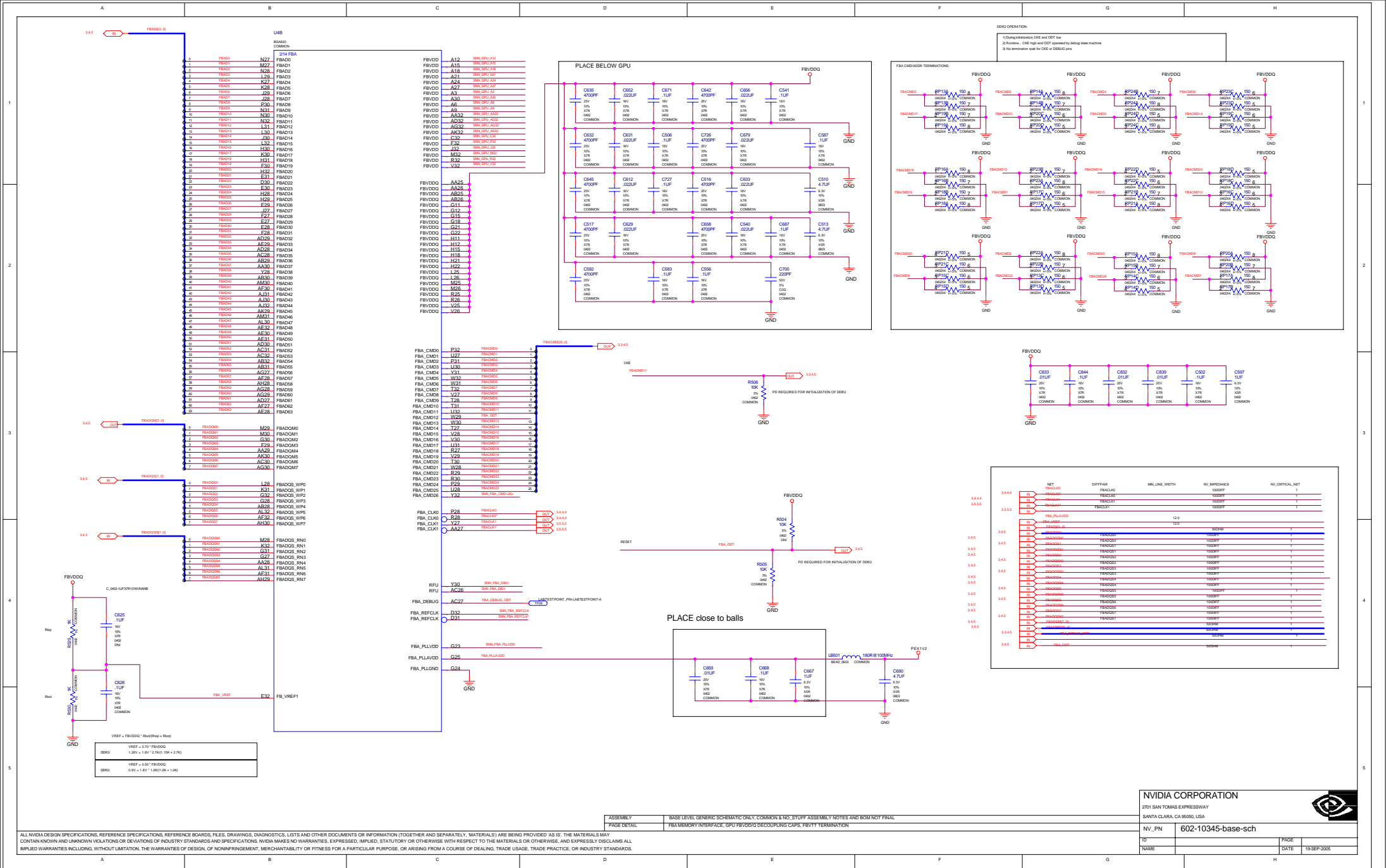
- Page1: TABLE OF CONTENTS & REVISION HISTORY
- Page2: PCI EXPRESS 16X, NVVDD DECOUPLING CAPS,PEX_IOVDD/Q DECOUPLING CAPS
- Page3: FBA MEMORY INTERFACE, FBVDD/Q DECOUPLING CAPS,TERMINATION
- Page4: FBA 16Mx16 DDR2 MEMORIES
- Page5: FBA 16Mx16 DDR2 MEMORIES
- Page6: FBC MEMORY INTERFACE, FBVDD/Q DECOUPLING CAPS,TERMINATION
- Page7: FBC 16Mx16 DDR2 MEMORIES
- Page8: FBC 16Mx16 DDR2 MEMORIES
- Page9: DACA FILTERS,DACA SYNC BUFFER &DB15 SOUTH
- Page10: DACC FILTERS, DACC SYNC BUFFERS & DB15 MID
- Page11: TMDS LINK A,B , DVI CONNECTOR SOUTH
- Page12: TMDS LINK C , DVI CONNECTOR MID
- Page13: MIOA & MIOB, SLI CONNECTOR
- Page14: PHILIPS SAA7115 VIDEO DECODER
- Page15: DACB FILTERS, MINIDIN CONNECTOR NORTH, 12-Pin Video HEADER
- Page16: GPU GND CONNECTION, XTAL
- Page17: JTAG, BIOS ROM, HDCP ROM, FAN CONTROL, TEMP SENSOR & GPIO
- Page18: BIOS STRAPS & MECHANICALS
- Page19: POWER SUPPLY: DDC5V, TMDS PLL VDD , A3V3 LINEAR
- Page20: POWER SUPPLY: ISL6549 FBVDDQ and PEX1V2
- Page21: POWER SUPPLY: ISL6549 NVVDD 5V, POWER SEQUENCE

REV	VARIANT	NVPN	ASSEMBLY
B	000	602-10345-000-100	G73 400352MHz 256MB 128M DDR2 16MX16 DVI-I+VGA+HDTVOUT
1	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
2	002	602-10345-002-100	G73 V 375350MHz 128MB 64Mx DDR2 16MX16 DVI-I+VGA+HDTVOUT
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

16X PCIe Interface



NET	NO. CAPS	NO. DIFFERENCES	DIFFERENCE
PEX_P0VDD	1	1000000	PEX_P0VDD
PEX_P1VDD	1	1000000	PEX_P1VDD
PEX_P2VDD	1	1000000	PEX_P2VDD
PEX_P3VDD	1	1000000	PEX_P3VDD
PEX_P4VDD	1	1000000	PEX_P4VDD
PEX_P5VDD	1	1000000	PEX_P5VDD
PEX_P6VDD	1	1000000	PEX_P6VDD
PEX_P7VDD	1	1000000	PEX_P7VDD
PEX_P8VDD	1	1000000	PEX_P8VDD
PEX_P9VDD	1	1000000	PEX_P9VDD
PEX_P10VDD	1	1000000	PEX_P10VDD
PEX_P11VDD	1	1000000	PEX_P11VDD
PEX_P12VDD	1	1000000	PEX_P12VDD
PEX_P13VDD	1	1000000	PEX_P13VDD
PEX_P14VDD	1	1000000	PEX_P14VDD
PEX_P15VDD	1	1000000	PEX_P15VDD
PEX_P16VDD	1	1000000	PEX_P16VDD
PEX_P17VDD	1	1000000	PEX_P17VDD
PEX_P18VDD	1	1000000	PEX_P18VDD
PEX_P19VDD	1	1000000	PEX_P19VDD
PEX_P20VDD	1	1000000	PEX_P20VDD
PEX_P21VDD	1	1000000	PEX_P21VDD
PEX_P22VDD	1	1000000	PEX_P22VDD
PEX_P23VDD	1	1000000	PEX_P23VDD
PEX_P24VDD	1	1000000	PEX_P24VDD
PEX_P25VDD	1	1000000	PEX_P25VDD
PEX_P26VDD	1	1000000	PEX_P26VDD
PEX_P27VDD	1	1000000	PEX_P27VDD
PEX_P28VDD	1	1000000	PEX_P28VDD
PEX_P29VDD	1	1000000	PEX_P29VDD
PEX_P30VDD	1	1000000	PEX_P30VDD
PEX_P31VDD	1	1000000	PEX_P31VDD
PEX_P32VDD	1	1000000	PEX_P32VDD
PEX_P33VDD	1	1000000	PEX_P33VDD
PEX_P34VDD	1	1000000	PEX_P34VDD
PEX_P35VDD	1	1000000	PEX_P35VDD
PEX_P36VDD	1	1000000	PEX_P36VDD
PEX_P37VDD	1	1000000	PEX_P37VDD
PEX_P38VDD	1	1000000	PEX_P38VDD
PEX_P39VDD	1	1000000	PEX_P39VDD
PEX_P40VDD	1	1000000	PEX_P40VDD
PEX_P41VDD	1	1000000	PEX_P41VDD
PEX_P42VDD	1	1000000	PEX_P42VDD
PEX_P43VDD	1	1000000	PEX_P43VDD
PEX_P44VDD	1	1000000	PEX_P44VDD
PEX_P45VDD	1	1000000	PEX_P45VDD
PEX_P46VDD	1	1000000	PEX_P46VDD
PEX_P47VDD	1	1000000	PEX_P47VDD
PEX_P48VDD	1	1000000	PEX_P48VDD
PEX_P49VDD	1	1000000	PEX_P49VDD
PEX_P50VDD	1	1000000	PEX_P50VDD
PEX_P51VDD	1	1000000	PEX_P51VDD
PEX_P52VDD	1	1000000	PEX_P52VDD
PEX_P53VDD	1	1000000	PEX_P53VDD
PEX_P54VDD	1	1000000	PEX_P54VDD
PEX_P55VDD	1	1000000	PEX_P55VDD
PEX_P56VDD	1	1000000	PEX_P56VDD
PEX_P57VDD	1	1000000	PEX_P57VDD
PEX_P58VDD	1	1000000	PEX_P58VDD
PEX_P59VDD	1	1000000	PEX_P59VDD
PEX_P60VDD	1	1000000	PEX_P60VDD
PEX_P61VDD	1	1000000	PEX_P61VDD
PEX_P62VDD	1	1000000	PEX_P62VDD
PEX_P63VDD	1	1000000	PEX_P63VDD
PEX_P64VDD	1	1000000	PEX_P64VDD
PEX_P65VDD	1	1000000	PEX_P65VDD
PEX_P66VDD	1	1000000	PEX_P66VDD
PEX_P67VDD	1	1000000	PEX_P67VDD
PEX_P68VDD	1	1000000	PEX_P68VDD
PEX_P69VDD	1	1000000	PEX_P69VDD
PEX_P70VDD	1	1000000	PEX_P70VDD
PEX_P71VDD	1	1000000	PEX_P71VDD
PEX_P72VDD	1	1000000	PEX_P72VDD
PEX_P73VDD	1	1000000	PEX_P73VDD
PEX_P74VDD	1	1000000	PEX_P74VDD
PEX_P75VDD	1	1000000	PEX_P75VDD
PEX_P76VDD	1	1000000	PEX_P76VDD
PEX_P77VDD	1	1000000	PEX_P77VDD
PEX_P78VDD	1	1000000	PEX_P78VDD
PEX_P79VDD	1	1000000	PEX_P79VDD
PEX_P80VDD	1	1000000	PEX_P80VDD
PEX_P81VDD	1	1000000	PEX_P81VDD
PEX_P82VDD	1	1000000	PEX_P82VDD
PEX_P83VDD	1	1000000	PEX_P83VDD
PEX_P84VDD	1	1000000	PEX_P84VDD
PEX_P85VDD	1	1000000	PEX_P85VDD
PEX_P86VDD	1	1000000	PEX_P86VDD
PEX_P87VDD	1	1000000	PEX_P87VDD
PEX_P88VDD	1	1000000	PEX_P88VDD
PEX_P89VDD	1	1000000	PEX_P89VDD
PEX_P90VDD	1	1000000	PEX_P90VDD
PEX_P91VDD	1	1000000	PEX_P91VDD
PEX_P92VDD	1	1000000	PEX_P92VDD
PEX_P93VDD	1	1000000	PEX_P93VDD
PEX_P94VDD	1	1000000	PEX_P94VDD
PEX_P95VDD	1	1000000	PEX_P95VDD
PEX_P96VDD	1	1000000	PEX_P96VDD
PEX_P97VDD	1	1000000	PEX_P97VDD
PEX_P98VDD	1	1000000	PEX_P98VDD
PEX_P99VDD	1	1000000	PEX_P99VDD
PEX_P100VDD	1	1000000	PEX_P100VDD
PEX_P101VDD	1	1000000	PEX_P101VDD
PEX_P102VDD	1	1000000	PEX_P102VDD
PEX_P103VDD	1	1000000	PEX_P103VDD
PEX_P104VDD	1	1000000	PEX_P104VDD
PEX_P105VDD	1	1000000	PEX_P105VDD
PEX_P106VDD	1	1000000	PEX_P106VDD
PEX_P107VDD	1	1000000	PEX_P107VDD
PEX_P108VDD	1	1000000	PEX_P108VDD
PEX_P109VDD	1	1000000	PEX_P109VDD
PEX_P110VDD	1	1000000	PEX_P110VDD
PEX_P111VDD	1	1000000	PEX_P111VDD
PEX_P112VDD	1	1000000	PEX_P112VDD
PEX_P113VDD	1	1000000	PEX_P113VDD
PEX_P114VDD	1	1000000	PEX_P114VDD
PEX_P115VDD	1	1000000	PEX_P115VDD
PEX_P116VDD	1	1000000	PEX_P116VDD
PEX_P117VDD	1	1000000	PEX_P117VDD
PEX_P118VDD	1	1000000	PEX_P118VDD
PEX_P119VDD	1	1000000	PEX_P119VDD
PEX_P120VDD	1	1000000	PEX_P120VDD
PEX_P121VDD	1	1000000	PEX_P121VDD
PEX_P122VDD	1	1000000	PEX_P122VDD
PEX_P123VDD	1	1000000	PEX_P123VDD
PEX_P124VDD	1	1000000	PEX_P124VDD
PEX_P125VDD	1	1000000	PEX_P125VDD
PEX_P126VDD	1	1000000	PEX_P126VDD
PEX_P127VDD	1	1000000	PEX_P127VDD
PEX_P128VDD	1	1000000	PEX_P128VDD
PEX_P129VDD	1	1000000	PEX_P129VDD
PEX_P130VDD	1	1000000	PEX_P130VDD
PEX_P131VDD	1	1000000	PEX_P131VDD
PEX_P132VDD	1	1000000	PEX_P132VDD
PEX_P133VDD	1	1000000	PEX_P133VDD
PEX_P134VDD	1	1000000	PEX_P134VDD
PEX_P135VDD	1	1000000	PEX_P135VDD
PEX_P136VDD	1	1000000	PEX_P136VDD
PEX_P137VDD	1	1000000	PEX_P137VDD
PEX_P138VDD	1	1000000	PEX_P138VDD
PEX_P139VDD	1	1000000	PEX_P139VDD
PEX_P140VDD	1	1000000	PEX_P140VDD
PEX_P141VDD	1	1000000	PEX_P141VDD
PEX_P142VDD	1	1000000	PEX_P142VDD
PEX_P143VDD	1	1000000	PEX_P143VDD
PEX_P144VDD	1	1000000	PEX_P144VDD
PEX_P145VDD	1	1000000	PEX_P145VDD
PEX_P146VDD	1	1000000	PEX_P146VDD
PEX_P147VDD	1	1000000	PEX_P147VDD
PEX_P148VDD	1	1000000	PEX_P148VDD
PEX_P149VDD	1	1000000	PEX_P149VDD
PEX_P150VDD	1	1000000	PEX_P150VDD
PEX_P151VDD	1	1000000	PEX_P151VDD
PEX_P152VDD	1	1000000	PEX_P152VDD
PEX_P153VDD	1	1000000	PEX_P153VDD
PEX_P154VDD	1	1000000	PEX_P154VDD
PEX_P155VDD	1	1000000	PEX_P155VDD
PEX_P156VDD	1	1000000	PEX_P156VDD
PEX_P157VDD	1	1000000	PEX_P157VDD
PEX_P158VDD	1	1000000	PEX_P158VDD
PEX_P159VDD	1	1000000	PEX_P159VDD
PEX_P160VDD	1	1000000	PEX_P160VDD
PEX_P161VDD	1	1000000	PEX_P161VDD
PEX_P162VDD	1	1000000	PEX_P162VDD
PEX_P163VDD	1	1000000	PEX_P163VDD
PEX_P164VDD	1	1000000	PEX_P164VDD
PEX_P165VDD	1	1000000	PEX_P165VDD
PEX_P166VDD	1	1000000	PEX_P166VDD
PEX_P167VDD	1	1000000	PEX_P167VDD
PEX_P168VDD	1	1000000	PEX_P168VDD
PEX_P169VDD	1	1000000	PEX_P169VDD
PEX_P170VDD	1	1000000	PEX_P170VDD
PEX_P171VDD	1	1000000	PEX_P171VDD
PEX_P172VDD	1	1000000	PEX_P172VDD
PEX_P173VDD	1	1000000	PEX_P173VDD
PEX_P174VDD	1	1000000	PEX_P174VDD
PEX_P175VDD	1	1000000	PEX_P175VDD
PEX_P176VDD	1	1000000	PEX_P176VDD
PEX_P177VDD	1	1000000	PEX_P177VDD
PEX_P178VDD	1	1000000	PEX_P178VDD
PEX_P179VDD	1	1000000	PEX_P179VDD
PEX_P180VDD	1	1000000	PEX_P180VDD
PEX_P181VDD	1	1000000	PEX_P181VDD
PEX_P182VDD	1	1000000	PEX_P182VDD
PEX_P183VDD	1	1000000	PEX_P183VDD
PEX_P184VDD	1	1000000	PEX_P184VDD
PEX_P185VDD	1	1000000	PEX_P185VDD
PEX_P186VDD	1	1000000	PEX_P186VDD
PEX_P187VDD	1	1000000	PEX_P187VDD
PEX_P188VDD	1	1000000	PEX_P188VDD
PEX_P189VDD	1	1000000	PEX_P189VDD
PEX_P190VDD	1	1000000	PEX_P190VDD
PEX_P191VDD	1	1000000	PEX_P191VDD
PEX_P192VDD	1	1000000	PEX_P192VDD
PEX_P193VDD	1	1000000	PEX_P193VDD
PEX_P194VDD	1	1000000	PEX_P194VDD
PEX_P195VDD	1	1000000	PEX_P195VDD
PEX_P196VDD	1	1000000	PEX_P196VDD
PEX_P197VDD	1	1000000	PEX_P197VDD
PEX_P198VDD	1	1000000	PEX_P198VDD
PEX_P199VDD	1	1000000	PEX_P199VDD
PEX_P200VDD	1	1000000	PEX_P200VDD



2701 SAN TOMAS EXPRESSWAY

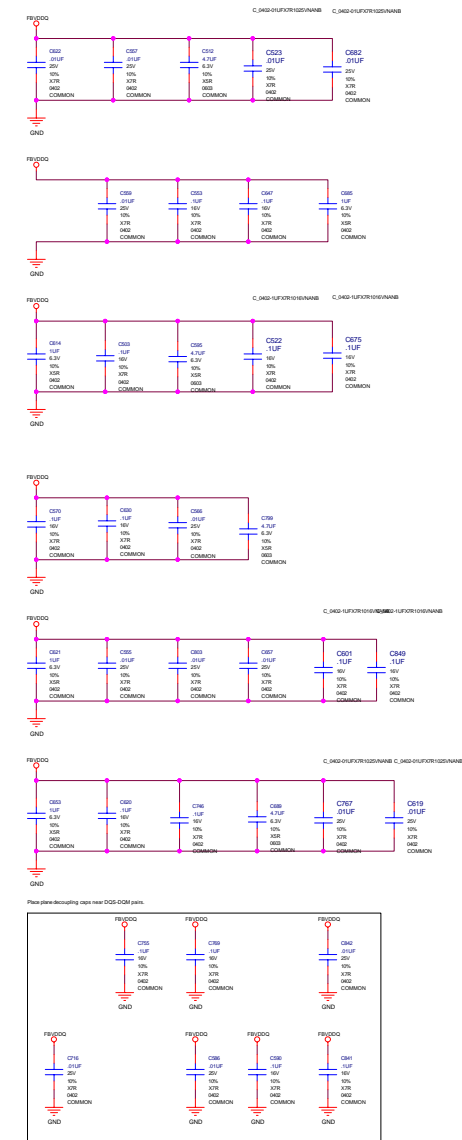


NV_PN	602-10345-base-sch
-------	--------------------

ID		PAGE	
NAME		DATE	19-SEP-2006

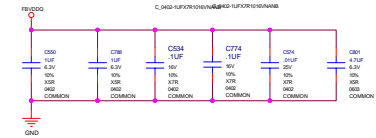
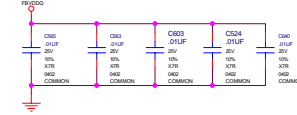
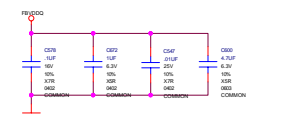
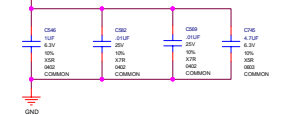
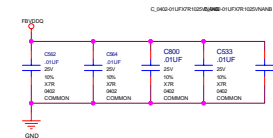
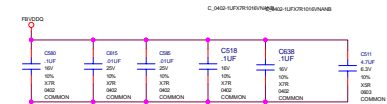
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY INTERFACE, GPU FBVDDIO DECOUPLING CAPS, FBVTT TERMINATION

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



ID		PAGE	
NAME		DATE	19-SEP-2005

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



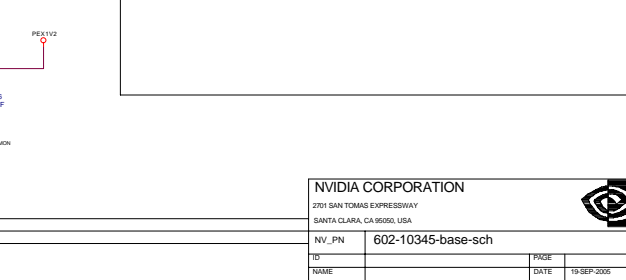
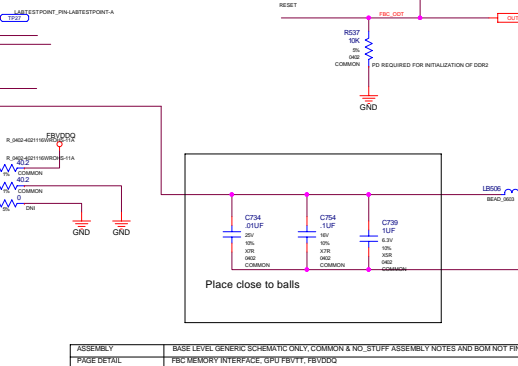
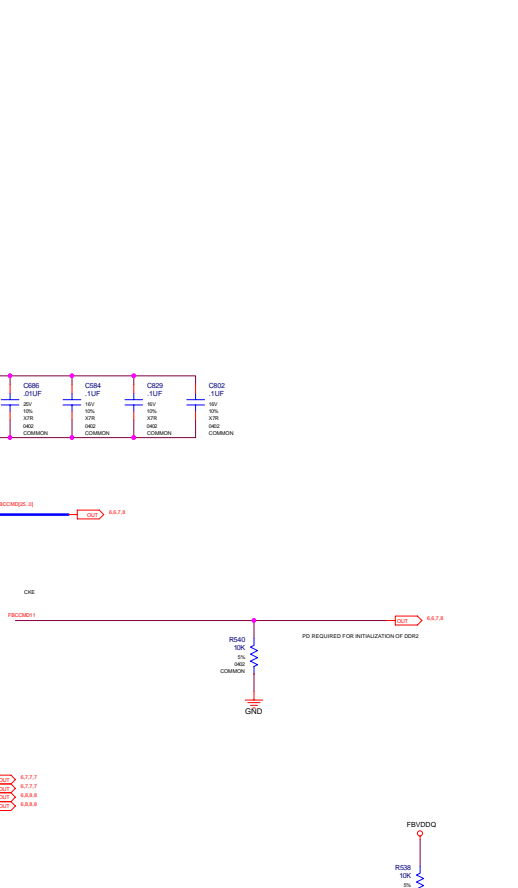
ID

NAME

PAGE	
DATE	19-SEP-2005

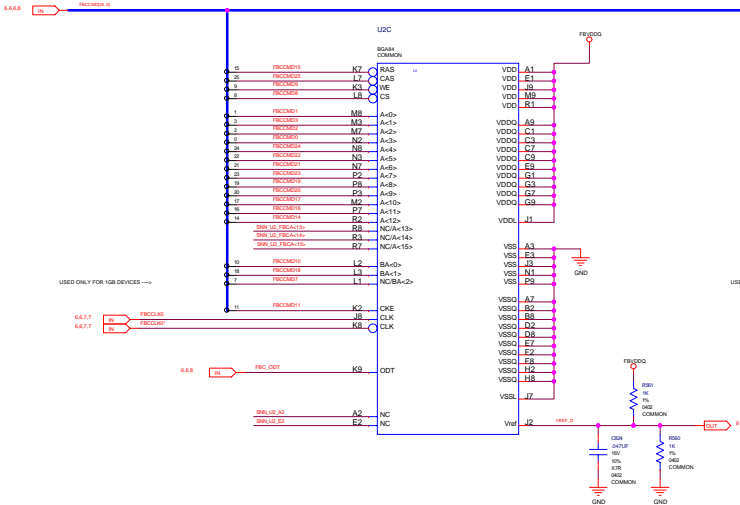
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARD.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16Mx16 DDR2 MEMORIES, 1ST BANK 32..63

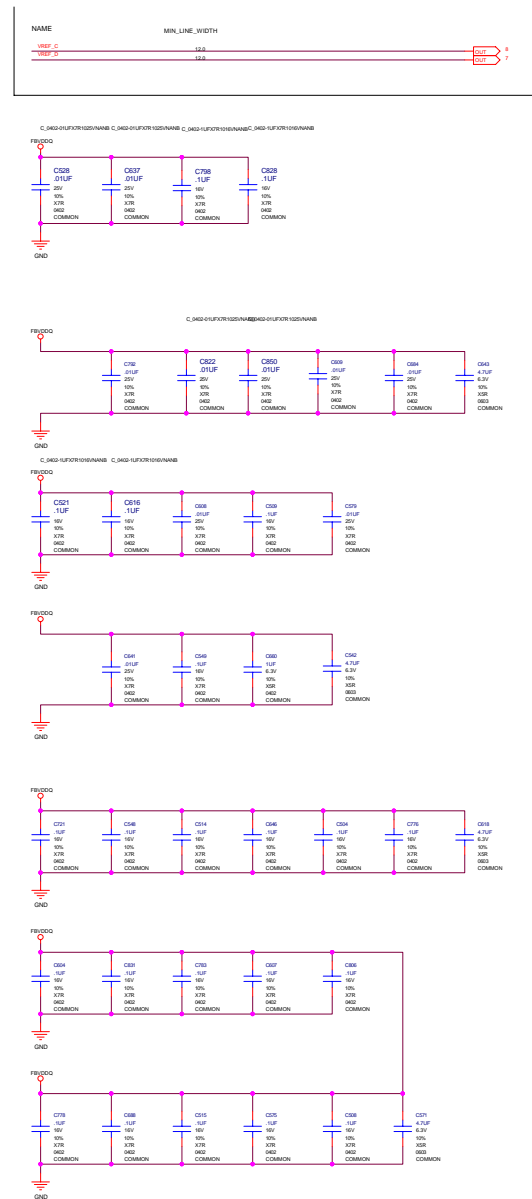


FBC MEMORY 2nd bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16Mx16 DDR2 MEMORIES, 2ND BANK 32..63

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10345-base-sch
-------	--------------------

	ID
--	----

NAME

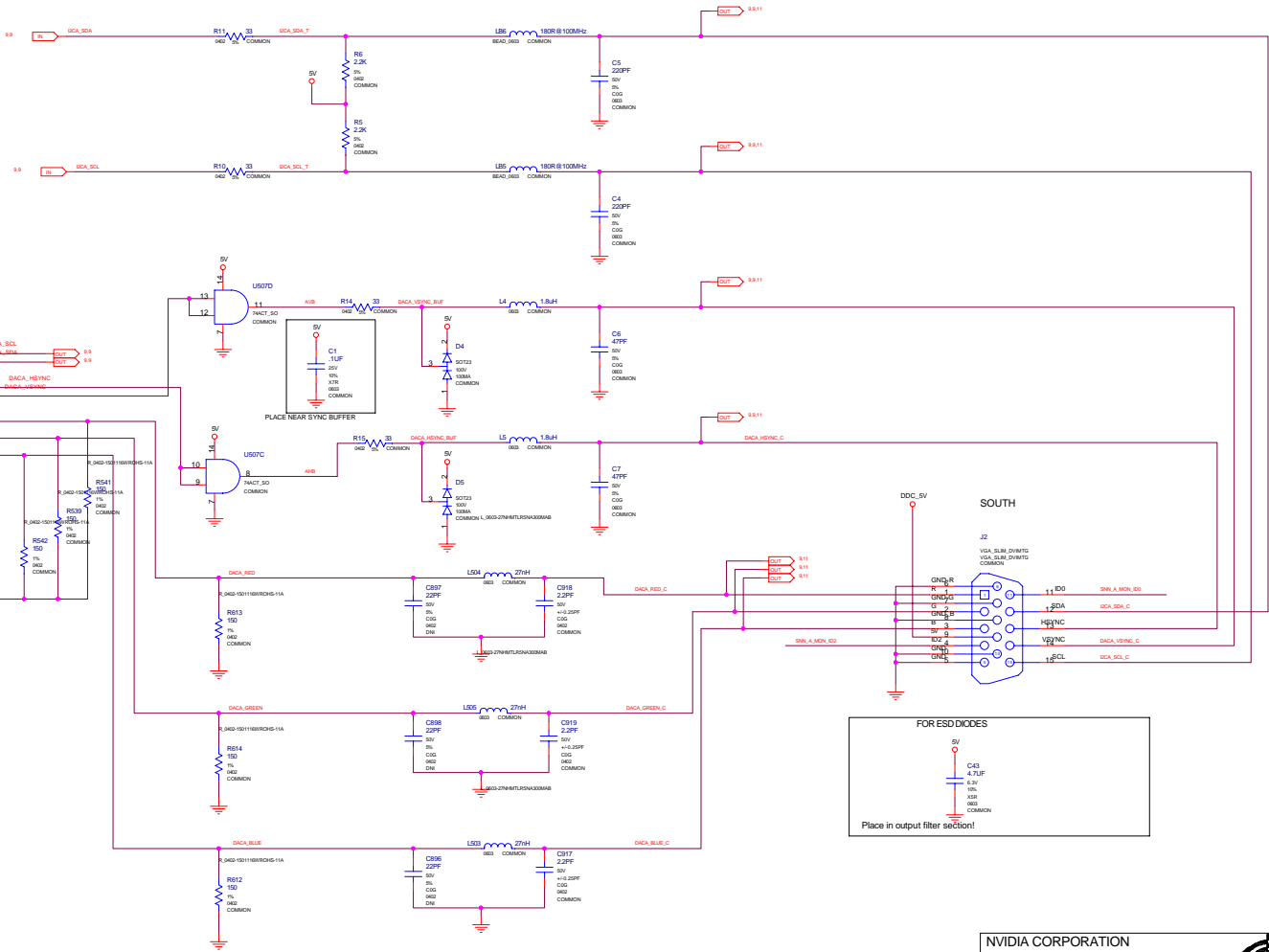
PAGE	
DATE	19-SEP-2006

DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACA_RED	1	75OHM	
DACA_GREEN	1	75OHM	
DACA_BLUE	1	75OHM	
DACA_RED_C	1	75OHM	
DACA_GREEN_C	1	75OHM	
DACA_BLUE_C	1	75OHM	
DACA_HSYNC	2	50OHM	
DACA_VSYNC	2	50OHM	
A_VS	2	50OHM	
AHS	2	50OHM	
DACA_HSYNC_BUF	2	50OHM	
DACA_VSYNC_BUF	2	50OHM	
DACA_HSYNC_C	2	50OHM	
DACA_VSYNC_C	2	50OHM	
DACA_SCL	1	50OHM	
DACA_SDA	1	50OHM	
DACA_SCL_T	1	50OHM	
DACA_SDA_T	1	50OHM	
DACA_SCL_C	1	50OHM	
DACA_SDA_C	1	50OHM	
DACA_VREF	1	50OHM	
DACA_RESET	1	50OHM	
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACA_VDD	3.3000V	0.07	16.0

Primary Display (DACA), Slim DB15

DACA RGB-FILTER



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN 602-10345-base-sch

ID

NAME

DATE 16 SEP 2006



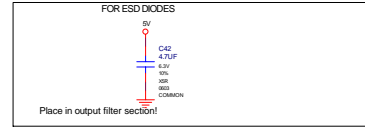
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

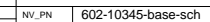
NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
1	0	0	0
2	0	0	0
3	0	0	0
4	0	0	0
5	0	0	0
6	0	0	0
7	0	0	0
8	0	0	0
9	0	0	0
10	0	0	0
11	0	0	0
12	0	0	0
13	0	0	0
14	0	0	0
15	0	0	0
16	0	0	0
17	0	0	0
18	0	0	0
19	0	0	0
20	0	0	0
21	0	0	0
22	0	0	0
23	0	0	0
24	0	0	0
25	0	0	0
26	0	0	0
27	0	0	0
28	0	0	0
29	0	0	0
30	0	0	0
31	0	0	0
32	0	0	0
33	0	0	0
34	0	0	0
35	0	0	0
36	0	0	0
37	0	0	0
38	0	0	0
39	0	0	0
40	0	0	0
41	0	0	0
42	0	0	0
43	0	0	0
44	0	0	0
45	0	0	0
46	0	0	0
47	0	0	0
48	0	0	0
49	0	0	0
50	0	0	0
51	0	0	0
52	0	0	0
53	0	0	0
54	0	0	0
55	0	0	0
56	0	0	0
57	0	0	0
58	0	0	0
59	0	0	0
60	0	0	0
61	0	0	0
62	0	0	0
63	0	0	0
64	0	0	0
65	0	0	0
66	0	0	0
67	0	0	0
68	0	0	0
69	0	0	0
70	0	0	0
71	0	0	0
72	0	0	0
73	0	0	0
74	0	0	0
75	0	0	0
76	0	0	0
77	0	0	0
78	0	0	0
79	0	0	0
80	0	0	0
81	0	0	0
82	0	0	0
83	0	0	0
84	0	0	0
85	0	0	0
86	0	0	0
87	0	0	0
88	0	0	0
89	0	0	0
90	0	0	0
91	0	0	0
92	0	0	0
93	0	0	0
94	0	0	0
95	0	0	0
96	0	0	0
97	0	0	0
98	0	0	0
99	0	0	0
100	0	0	0

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACC_VDD	3.30000	0.14	16.0

DACC RGB-FILTER



2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95060, USA



ID	PAGE
NAME	DATE 19-SEP-2005

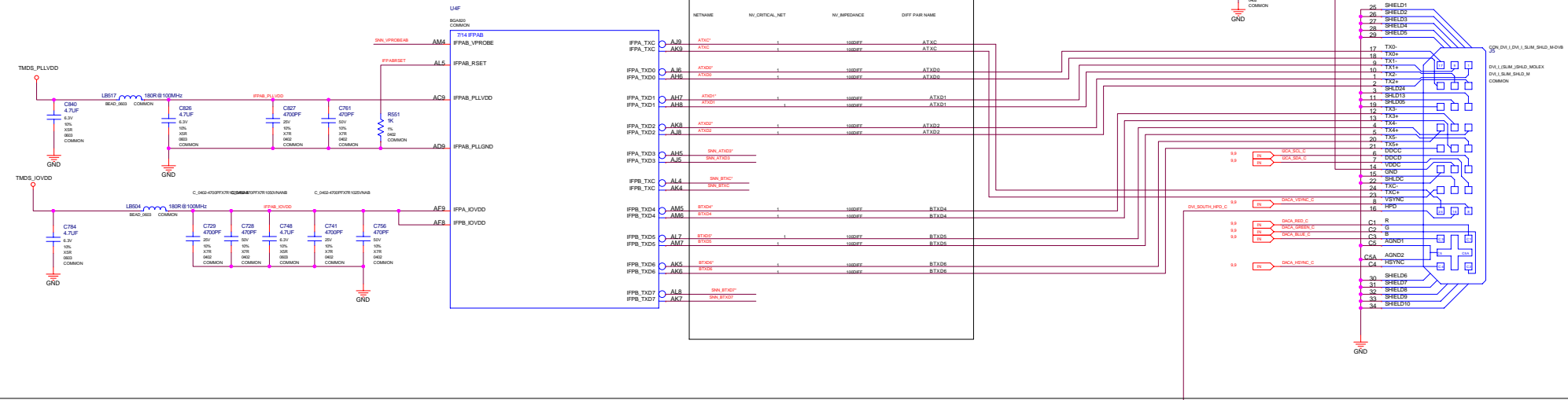
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VULNERABILITIES OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

INTERNAL TMDS .. LINK A & B

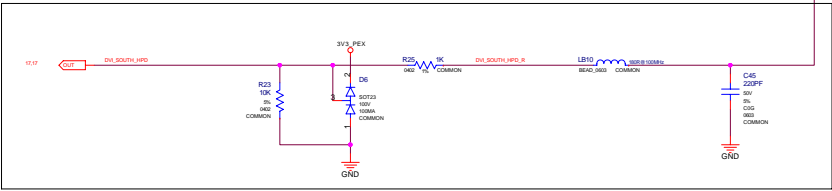
IFPAB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RSET	1	50OHM	
DVI_SOUTH_HPD_C	1	50OHM	
DVI_SOUTH_HPD_B	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_FLLVDD	3.300V	0.04	16.0
IFPAB_IJVVDD	3.300V	0.04	16.0



Hotplug Detection



NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL: TMDS LINK A & PUT, DVI CONNECTOR SOUTH







NV_PN: 602-10345-base-sch

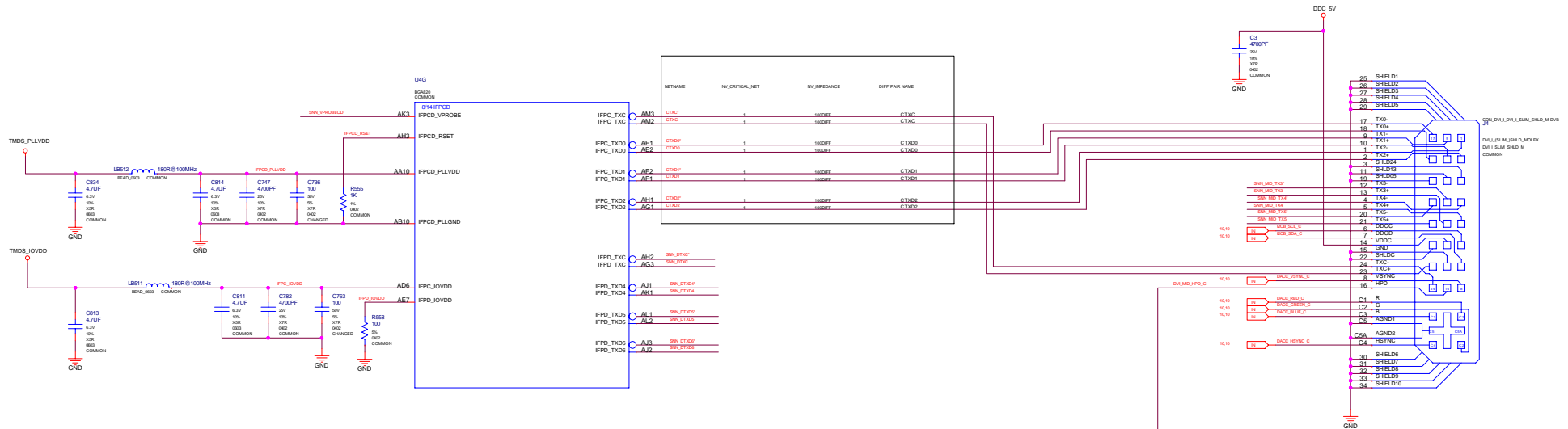
TO:	NAME:	DATE:
		16 SEP 2006

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE PRACTICE, OR INDUSTRY STANDARDS.

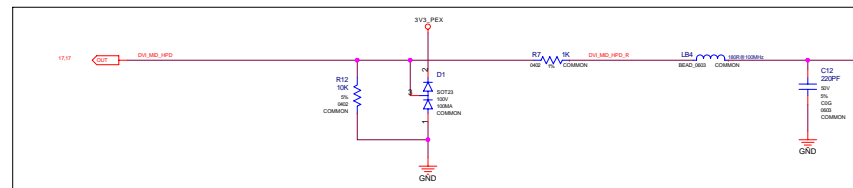
INTERNAL TMDS .. LINK C

IFPAB NET RULES

	NET	NC, CRITICAL	NV, IMPEDANCE	DIFFRAI
11	 IFAIN, RESET  DIVL, MPD, C  DIVL, MPD, A	1 1 1	50OHM 50OHM 50OHM	
	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
	 IFAIN, PALLVD	3.3000	0.14	16.0
	 IFAIN, PALLVD	3.3000	0.12	16.0
	 IFAIN, PALLVD	3.3000	0.12	16.0



Hotplug Detection



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



NV_PN	602-10345-base-sch
-------	--------------------

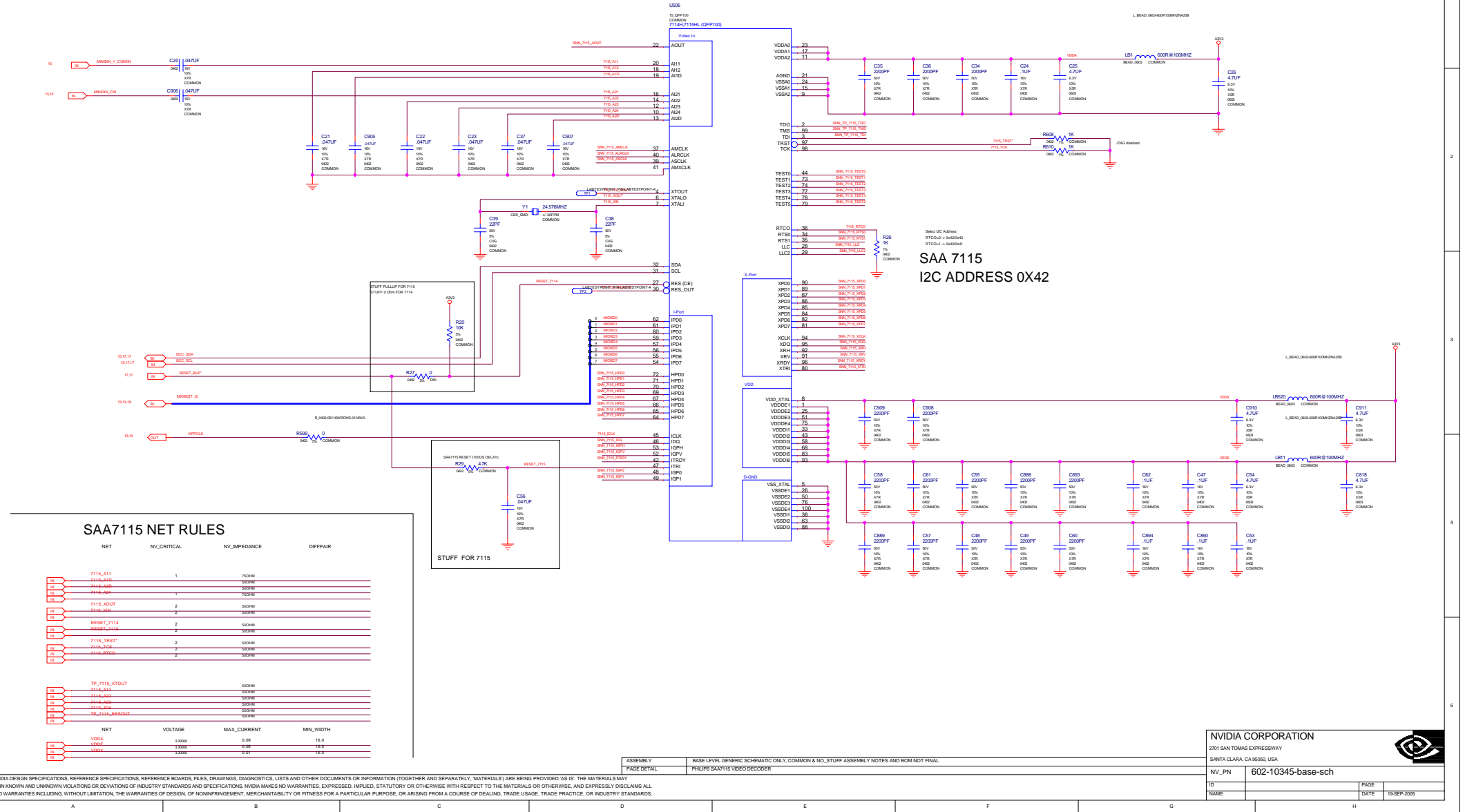
ID	PAGE
NAME	DATE 19-SEP-2005

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
----------	---

PAGE DETAIL	TMD5 LINK C & PU's,DVI CONNECTOR MID
-------------	--------------------------------------

PHILIPS VIDEO CAPTURE



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV_PN

602-10345-base-sch

TO

NAME

PAGE

DATE

16 SEP 2005

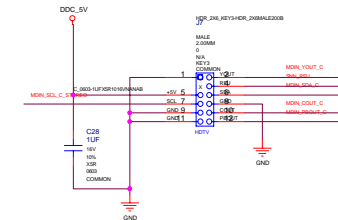
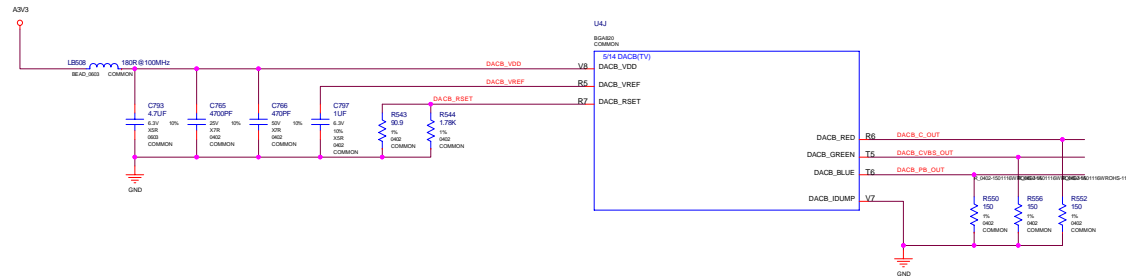
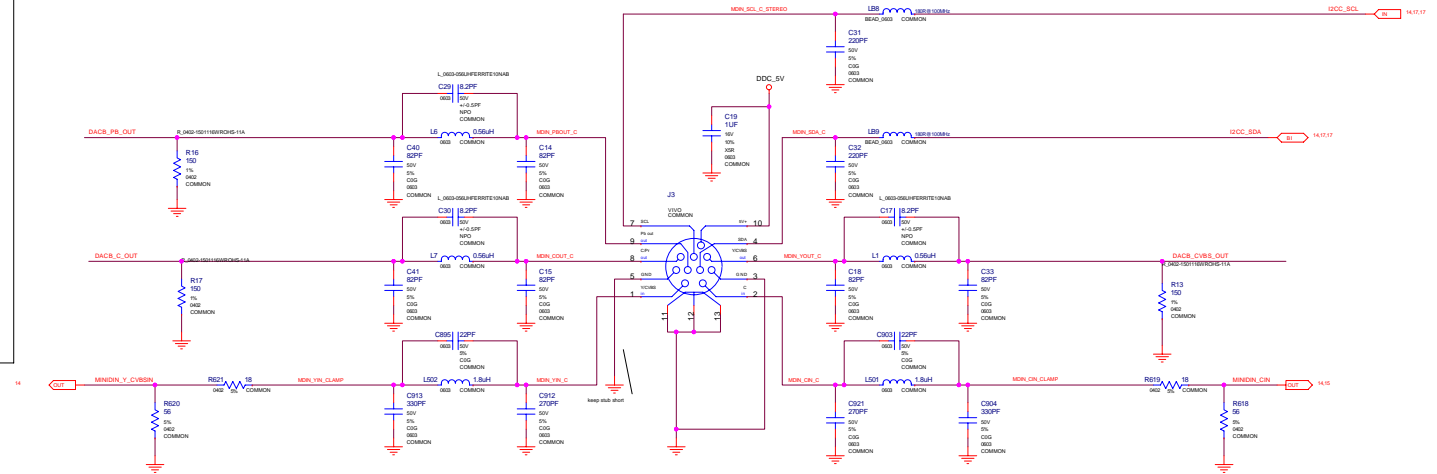
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

DACB .. MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES

DACB NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
21	DACB_C_OUT	1	750M	
21	MONA_COUT_C	1	750M	
21	DACB_CVBS_OUT	1	750M	
21	MONA_COUT_C	1	750M	
21	DACB_PSE_OUT	1	750M	
21	MONA_PSEOUT_C	1	750M	
21	MONMON_T_CVBSYEN	1	750M	
21	MONA_OUT_CLAMP	1	750M	
21	MONA_OUT_C	1	750M	
21	MONMON_CN	1	750M	
21	MONA_CN_CLAMP	1	750M	
21	MONA_CN_C	1	750M	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
	DACB_VDD	3.3000	0.07	16.0
R0	DACB_VDD			16.0
R1	DACB_VDD			16.0
R2	DACB_VDD			16.0
	MODN_GND1	0.0V		16MIL
R0	MODN_GND1	0.0V		16MIL
R1	MODN_GND1	0.0V		16MIL



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10345-base-sch
-------	--------------------

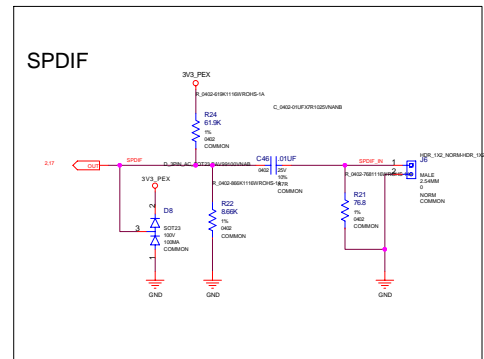
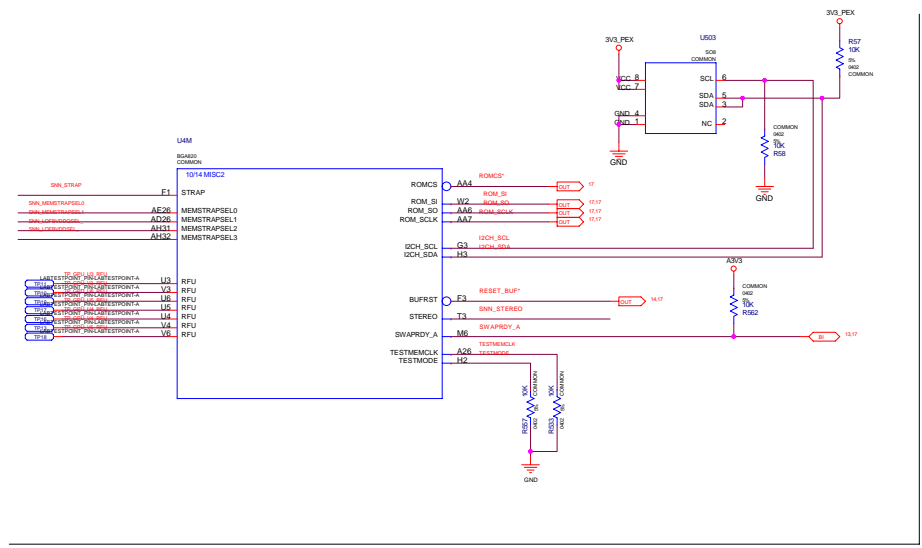
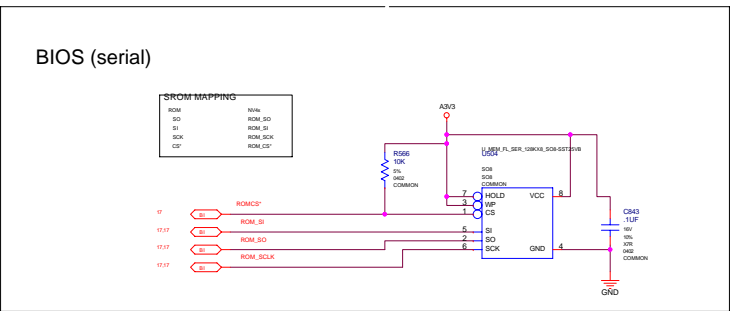
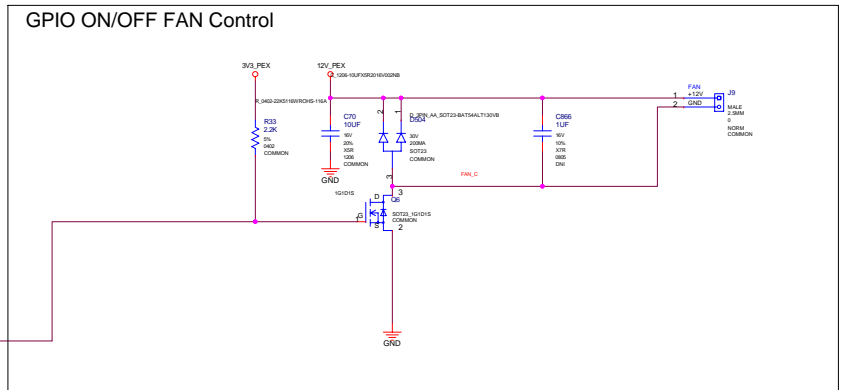
ID	
NAME	

PAGE	
DATE	19-SEP-2006



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS: THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VULNERABILITIES OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

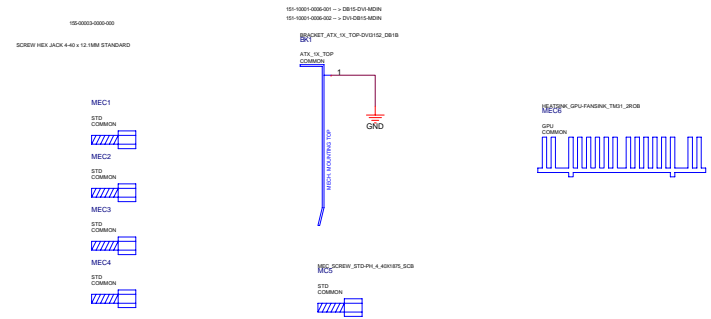
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, SYNC STRIPPER, MINIDIN CONNECTOR NORTH, HDTV HEADER



		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
14,15,17	14	GDG_BCL		NODM	
14,15,17	15	GDG_BWA		NODM	
	16	GDG_BCL-B		NODM	
	17	GDG_BWA-B		NODM	
	18	GDH_BCL		NODM	
	19	GDH_BWA		NODM	
	20	ROM_CS*	2	NODM	
17,21	21	ROM_SI	2	NODM	
17,21	22	ROM_SO	2	NODM	
17,21	23	ROM_STACK	2	NODM	
14,17	24	RESET_BUP*	2	NODM	
14,17	25	TESTMODE* A	2	NODM	
	26	TESTMODECLK	2	NODM	
	27	TESTMODE	2	NODM	
11,17	28	DVI_SOUTH_HPO		NODM	
12,17	29	DVI_TEST_HPO		NODM	
	30	TP_GPD0_BRNCK_DETECT		NODM	
	31	TP_GPD0_BRNCK_POWER		NODM	
	32	TP_GPD0_VIO_BST		NODM	
	33	TP_GPD0_VIOCL		NODM	
	34	TP_GPD0_VIOCT		NODM	
	35	TP_GPD0_VIO_S0		NODM	
	36	TP_GPD0_VIORES_ALERT1*		NODM	
	37	TP_GPD0_VIO_INT		NODM	
	38	TP_GPD01_1_GPD0_DETECT		NODM	
	39	TP_GPD1_103_RFU		NODM	
	40	TP_GPD1_VIO_RFU		NODM	
	41	TP_GPD1_VIO_RFU		NODM	
	42	TP_GPD1_VIO_RFU		NODM	
	43	TP_GPD1_VIO_RFU		NODM	
	44	TP_GPD1_VIO_RFU		NODM	
	45	TP_GPD1_VIO_RFU		NODM	
	46	TP_GPD1_VIO_RFU		NODM	
	47	TP_GPD1_VIO_RFU		NODM	
	48	TP_GPD1_VIO_RFU		NODM	
	49	TP_GPD1_VIO_RFU		NODM	
	50	TP_GPD1_VIO_RFU		NODM	
	51	TP_GPD1_VIO_RFU		NODM	
	52	TP_GPD1_VIO_RFU		NODM	
	53	TP_GPD1_VIO_RFU		NODM	
	54	TP_GPD1_VIO_RFU		NODM	
	55	TP_GPD1_VIO_RFU		NODM	
	56	TP_GPD1_VIO_RFU		NODM	
	57	TP_GPD1_VIO_RFU		NODM	
	58	TP_GPD1_VIO_RFU		NODM	
	59	TP_GPD1_VIO_RFU		NODM	
	60	TP_GPD1_VIO_RFU		NODM	
	61	TP_GPD1_VIO_RFU		NODM	
	62	TP_GPD1_VIO_RFU		NODM	
	63	TP_GPD1_VIO_RFU		NODM	
	64	TP_GPD1_VIO_RFU		NODM	
	65	TP_GPD1_VIO_RFU		NODM	
	66	TP_GPD1_VIO_RFU		NODM	
	67	TP_GPD1_VIO_RFU		NODM	
	68	TP_GPD1_VIO_RFU		NODM	
	69	TP_GPD1_VIO_RFU		NODM	
	70	TP_GPD1_VIO_RFU		NODM	
	71	TP_GPD1_VIO_RFU		NODM	
	72	TP_GPD1_VIO_RFU		NODM	
	73	TP_GPD1_VIO_RFU		NODM	
	74	TP_GPD1_VIO_RFU		NODM	
	75	TP_GPD1_VIO_RFU		NODM	
	76	TP_GPD1_VIO_RFU		NODM	
	77	TP_GPD1_VIO_RFU		NODM	
	78	TP_GPD1_VIO_RFU		NODM	
	79	TP_GPD1_VIO_RFU		NODM	
	80	TP_GPD1_VIO_RFU		NODM	
	81	TP_GPD1_VIO_RFU		NODM	
	82	TP_GPD1_VIO_RFU		NODM	
	83	TP_GPD1_VIO_RFU		NODM	
	84	TP_GPD1_VIO_RFU		NODM	
	85	TP_GPD1_VIO_RFU		NODM	
	86	TP_GPD1_VIO_RFU		NODM	
	87	TP_GPD1_VIO_RFU		NODM	
	88	TP_GPD1_VIO_RFU		NODM	
	89	TP_GPD1_VIO_RFU		NODM	
	90	TP_GPD1_VIO_RFU		NODM	
	91	TP_GPD1_VIO_RFU		NODM	
	92	TP_GPD1_VIO_RFU		NODM	
	93	TP_GPD1_VIO_RFU		NODM	
	94	TP_GPD1_VIO_RFU		NODM	
	95	TP_GPD1_VIO_RFU		NODM	
	96	TP_GPD1_VIO_RFU		NODM	
	97	TP_GPD1_VIO_RFU		NODM	
	98	TP_GPD1_VIO_RFU		NODM	
	99	TP_GPD1_VIO_RFU		NODM	
	100	TP_GPD1_VIO_RFU		NODM	
	101	TP_GPD1_VIO_RFU		NODM	
	102	TP_GPD1_VIO_RFU		NODM	
	103	TP_GPD1_VIO_RFU		NODM	
	104	TP_GPD1_VIO_RFU		NODM	
	105	TP_GPD1_VIO_RFU		NODM	
	106	TP_GPD1_VIO_RFU		NODM	
	107	TP_GPD1_VIO_RFU		NODM	
	108	TP_GPD1_VIO_RFU		NODM	
	109	TP_GPD1_VIO_RFU		NODM	
	110	TP_GPD1_VIO_RFU		NODM	
	111	TP_GPD1_VIO_RFU		NODM	
	112	TP_GPD1_VIO_RFU		NODM	
	113	TP_GPD1_VIO_RFU		NODM	
	114	TP_GPD1_VIO_RFU		NODM	
	115	TP_GPD1_VIO_RFU		NODM	
	116	TP_GPD1_VIO_RFU		NODM	
	117	TP_GPD1_VIO_RFU		NODM	
	118	TP_GPD1_VIO_RFU		NODM	
	119	TP_GPD1_VIO_RFU		NODM	
	120	TP_GPD1_VIO_RFU		NODM	
	121	TP_GPD1_VIO_RFU		NODM	
	122	TP_GPD1_VIO_RFU		NODM	
	123	TP_GPD1_VIO_RFU		NODM	
	124	TP_GPD1_VIO_RFU		NODM	
	125	TP_GPD1_VIO_RFU		NODM	
	126	TP_GPD1_VIO_RFU		NODM	
	127	TP_GPD1_VIO_RFU		NODM	
	128	TP_GPD1_VIO_RFU		NODM	
	129	TP_GPD1_VIO_RFU		NODM	
	130	TP_GPD1_VIO_RFU		NODM	
	131	TP_GPD1_VIO_RFU		NODM	
	132	TP_GPD1_VIO_RFU		NODM	
	133	TP_GPD1_VIO_RFU		NODM	
	134	TP_GPD1_VIO_RFU		NODM	
	135	TP_GPD1_VIO_RFU		NODM	
	136	TP_GPD1_VIO_RFU		NODM	
	137	TP_GPD1_VIO_RFU		NODM	
	138	TP_GPD1_VIO_RFU		NODM	
	139	TP_GPD1_VIO_RFU		NODM	
	140	TP_GPD1_VIO_RFU		NODM	
	141	TP_GPD1_VIO_RFU		NODM	
	142	TP_GPD1_VIO_RFU		NODM	
	143	TP_GPD1_VIO_RFU		NODM	
	144	TP_GPD1_VIO_RFU		NODM	
	145	TP_GPD1_VIO_RFU		NODM	
	146	TP_GPD1_VIO_RFU		NODM	
	147	TP_GPD1_VIO_RFU		NODM	
	148	TP_GPD1_VIO_RFU		NODM	
	149	TP_GPD1_VIO_RFU		NODM	
	150	TP_GPD1_VIO_RFU		NODM	
	151	TP_GPD1_VIO_RFU		NODM	
	152	TP_GPD1_VIO_RFU		NODM	
	153	TP_GPD1_VIO_RFU		NODM	
	154	TP_GPD1_VIO_RFU		NODM	
	155	TP_GPD1_VIO_RFU		NODM	
	156	TP_GPD1_VIO_RFU		NODM	
	157	TP_GPD1_VIO_RFU		NODM	
	158	TP_GPD1_VIO_RFU		NODM	
	159	TP_GPD1_VIO_RFU		NODM	
	160	TP_GPD1_VIO_RFU		NODM	
	161	TP_GPD1_VIO_RFU		NODM	
	162	TP_GPD1_VIO_RFU		NODM	
	163	TP_GPD1_VIO_RFU		NODM	
	164	TP_GPD1_VIO_RFU		NODM	
	165	TP_GPD1_VIO_RFU		NODM	
	166	TP_GPD1_VIO_RFU		NODM	
	167	TP_GPD1_VIO_RFU		NODM	
	168	TP_GPD1_VIO_RFU		NODM	
	169	TP_GPD1_VIO_RFU		NODM	
	170	TP_GPD1_VIO_RFU		NODM	
	171	TP_GPD1_VIO_RFU		NODM	
	172	TP_GPD1_VIO_RFU		NODM	
	173	TP_GPD1_VIO_RFU		NODM	
	174	TP_GPD1_VIO_RFU		NODM	
	175	TP_GPD1_VIO_RFU		NODM	
	176	TP_GPD1_VIO_RFU		NODM	
	177	TP_GPD1_VIO_RFU		NODM	
	178	TP_GPD1_VIO_RFU		NODM	
	179	TP_GPD1_VIO_RFU		NODM	
	180	TP_GPD1_VIO_RFU		NODM	
	181	TP_GPD1_VIO_RFU		NODM	
	182	TP_GPD1_VIO_RFU		NODM	
	183	TP_GPD1_VIO_RFU		NODM	
	184	TP_GPD1_VIO_RFU		NODM	
	185	TP_GPD1_VIO_RFU		NODM	
	186	TP_GPD1_VIO_RFU		NODM	
	187	TP_GPD1_VIO_RFU		NODM	
	188	TP_GPD1_VIO_RFU		NODM	
	189	TP_GPD1_VIO_RFU		NODM	
	190	TP_GPD1_VIO_RFU		NODM	
	191	TP_GPD1_VIO_RFU		NODM	
	192	TP_GPD1_VIO_RFU		NODM	
	193	TP_GPD1_VIO_RFU		NODM	
	194	TP_GPD1_VIO_RFU		NODM	
	195	TP_GPD1_VIO_RFU		NODM	
	196	TP_GPD1_VIO_RFU		NODM	
	197	TP_GPD1_VIO_RFU		NODM	
	198	TP_GPD1_VIO_RFU		NODM	
	199	TP_GPD1_VIO_RFU		NODM	
	200	TP_GPD1_VIO_RFU		NODM	
	201	TP_GPD1_VIO_RFU		NODM	
	202	TP_GPD1_VIO_RFU		NODM	
	203	TP_GPD1_VIO_RFU		NODM	
	204	TP_GPD1_VIO_RFU		NODM	
	205	TP_GPD1_VIO_RFU		NODM	
	206	TP_GPD1_VIO_RFU		NODM	
	207	TP_GPD1_VIO_RFU		NODM	
	208	TP_GPD1_VIO_RFU		NODM	
	209	TP_GPD1_VIO_RFU		NODM	
	210	TP_GPD1_VIO_RFU		NODM	
	211	TP_GPD1_VIO_RFU		NODM	
	212	TP_GPD1_VIO_RFU		NODM	
	213	TP_GPD1_VIO_RFU		NODM	
	214	TP_GPD1_VIO_RFU		NODM	
	215	TP_GPD1_VIO_RFU		NODM	
	216	TP_GPD1_VIO_RFU		NODM	
	217	TP_GPD1_VIO_RFU		NODM	
	218	TP_GPD1_VIO_RFU		NODM	
	219	TP_GPD1_VIO_RFU		NODM	
	220	TP_GPD1_VIO_RFU		NODM	
	221	TP_GPD1_VIO_RFU		NODM	
	222	TP_GPD1_VIO_RFU		NODM	
	223	TP_GPD1_VIO_RFU		NODM	
	224	TP_GPD1_VIO_RFU		NODM	
	225	TP_GPD1_VIO_RFU		NODM	
	226	TP_GPD1_VIO_RFU		NODM	
	227	TP_GPD1_VIO_RFU		NODM	
	228	TP_GPD1_VIO_RFU		NODM	
	229	TP_GPD1_VIO_RFU		NODM	
	230	TP_GPD1_VIO_RFU		NODM	
	231	TP_GPD1_VIO_RFU		NODM	
	232	TP_GPD1_VIO_RFU		NODM	
	233	TP_GPD1_VIO_RFU		NODM	
	234	TP_GPD1_VIO_RFU		NODM	
	235	TP_GPD1_VIO_RFU		NODM	
	236	TP_GPD1_VIO_RFU		NODM	
	237	TP_GPD1_VIO_RFU		NODM	
	238	TP_GPD1_VIO_RFU		NODM	
	239	TP_GPD1_VIO_RFU		NODM	
	240	TP_GPD1_VIO_RFU		NODM	
	241	TP_GPD1_VIO_RFU		NODM	
	242	TP_GPD1_VIO_RFU		NODM	
	243	TP_GPD1_VIO_RFU		NODM	
	244	TP_GPD1_VIO_RFU		NODM	
	245	TP_GPD1_VIO_RFU		NODM	
	246	TP_GPD1_VIO_RFU		NODM	
	247	TP_GPD1_VIO_RFU		NODM	
	248	TP_GPD1_VIO_RFU		NODM	
	249	TP_GPD1_VIO_RFU		NODM	
	250	TP_GPD1_VIO_RFU		NODM	
	251	TP_GPD1_VIO_RFU		NODM	
	252	TP_GPD1_VIO_RFU		NODM	
	253	TP_GPD1_VIO_RFU		NODM	
	254	TP_GPD1_VIO_RFU		NODM	
	255	TP_GPD1_VIO_RFU		NODM	
	256	TP_GPD1_VIO_RFU		NODM	
	257	TP_GPD1_VIO_RFU		NODM	
	258	TP_GPD1_VIO_RFU		NODM	
	259	TP_GPD1_VIO_RFU		NODM	
	260	TP_GPD1_VIO_RFU		NODM	
	261	TP_GPD1_VIO_RFU		NODM	
	262	TP_GPD1_VIO_RFU		NODM	
	263	TP_GPD1_VIO_RFU		NODM	
	264	TP_GPD1_VIO_RFU		NODM	
	265	TP_GPD1_VIO_RFU		NODM	
	266	TP_GPD1_VIO_RFU		NODM	
	267	TP_GPD1_VIO_RFU		NODM	
	268	TP_GPD1_VIO_RFU		NODM	
	269	TP_GPD1_VIO_RFU		NODM	
	270	TP_GPD1_VIO_RFU		NODM	
	271	TP_GPD1_VIO_RFU		NODM	
	272	TP_GPD1_VIO_RFU		NODM	
	273	TP_GPD1_VIO_RFU		NODM	
	274	TP_GPD1_VIO_RFU		NODM	
	275	TP_GPD1_VIO_RFU		NODM	
	276	TP_GPD1_VIO_RFU		NODM	
	277	TP_GPD1_VIO_RFU		NODM	
	278	TP_GPD1_VIO_RFU		NODM	
	279	TP_GPD1_VIO_RFU		NODM	
	280	TP_GPD1_VIO_RFU		NODM	
	281	TP_GPD1_VIO_RFU		NODM	
	282	TP_GPD1_VIO_RFU		NODM	
	283	TP_GPD1_VIO_RFU		NODM	
	284	TP_GPD1_VIO_RFU		NODM	
	285	TP_GPD1_VIO_RFU		NODM	
	286	TP_GPD1_VIO_RFU		NODM	
	287	TP_GPD1_VIO_RFU		NODM	
	288	TP_GPD1_VIO_RFU		NODM	
	289	TP_GPD1_VIO_RFU		NODM	
	290	TP_GPD1_VIO_RFU		NODM	
	291	TP_GPD1_VIO_RFU		NODM	
	292	TP_GPD1_VIO_RFU		NODM	
	293	TP_GPD1_VIO_RFU		NODM	
	294	TP_GPD1_VIO_RFU		NODM	
	295	TP_GPD1_VIO_RFU		NODM	
	296				

Straps

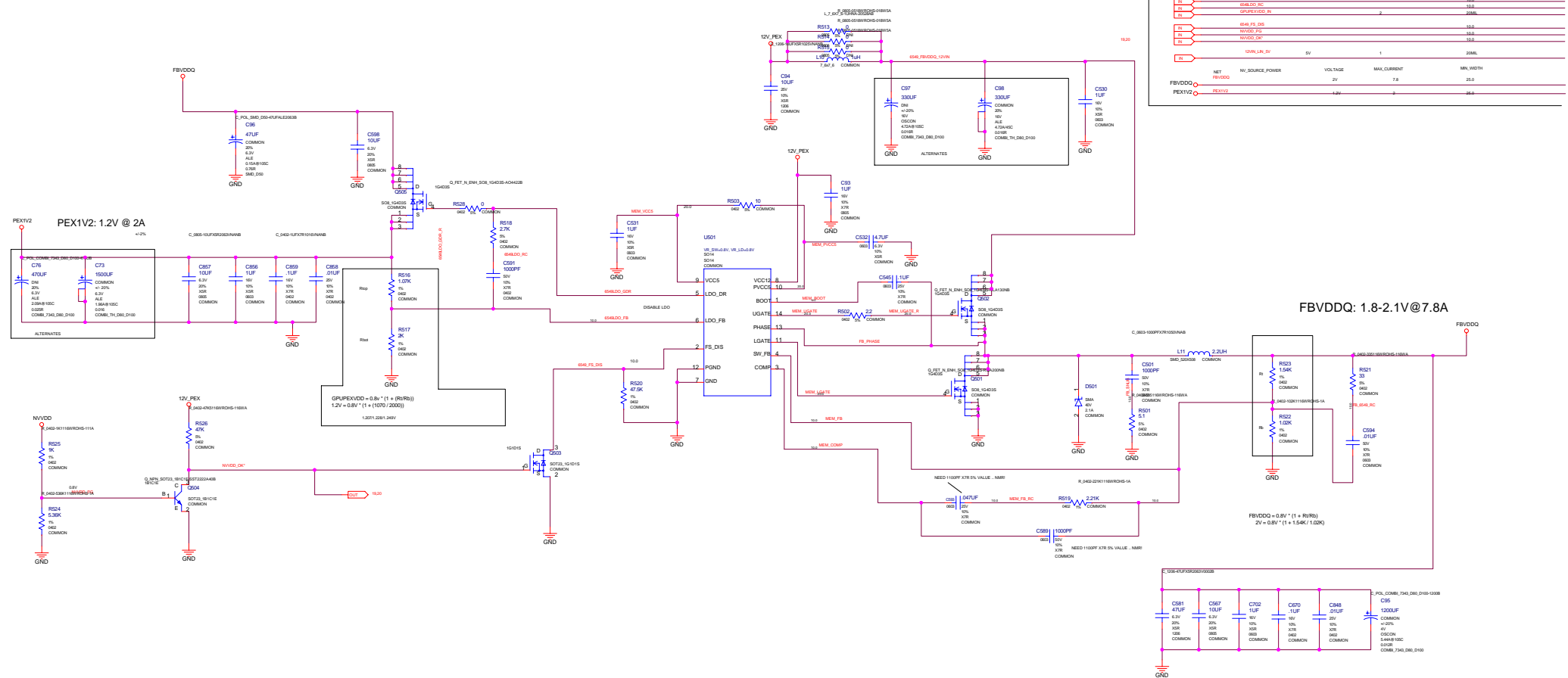
Mechanical parts



DATE	19-SEP-2006
------	-------------

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

PowerSupply ISL6549 FBVDDQ/PEX1V2



	VOLTAGE	MAX. CURRENT	MAX. VOLTAGE
U1	MEM_VCCCS		20.0
U2	MEM_B00P		12.0
U3	MEM_VCC1N		20.0
U4	MEM_VCC1N_R		20.0
U5	PE_VCC1N	7.8	20.0
U6	PE_VCC1N_R		20.0
U7	PE_VCC1N		10.0
U8	MEM_VCC		10.0
U9	MEM_VCC		10.0
U10	PE_VCC1N		10.0
U11	PE_VCC1N		10.0
U12	PE_VCC1N		10.0
U13	MEM_VCCCS		20.0
U14	GRAPHS_CSR		10.0
U15	GRAPHS_VB		10.0
U16	GRAPHS_CSR_R		10.0
U17	GRAPHS_VB_R		10.0
U18	GRAPHS_CSR_R	2	200mA
U19	GRAPHS_VB		10.0
U20	GRAPHS_VB		10.0
U21	GRAPHS_CSR		10.0
U22	GRAPHS_CSR		10.0
U23	GRAPHS_CSR		10.0
U24	GRAPHS_CSR		10.0
U25	GRAPHS_CSR		10.0
U26	GRAPHS_CSR		10.0
U27	GRAPHS_CSR		10.0
U28	GRAPHS_CSR		10.0
U29	GRAPHS_CSR		10.0
U30	GRAPHS_CSR		10.0
U31	GRAPHS_CSR		10.0
U32	GRAPHS_CSR		10.0
U33	GRAPHS_CSR		10.0
U34	GRAPHS_CSR		10.0
U35	GRAPHS_CSR		10.0
U36	GRAPHS_CSR		10.0
U37	GRAPHS_CSR		10.0
U38	GRAPHS_CSR		10.0
U39	GRAPHS_CSR		10.0
U40	GRAPHS_CSR		10.0
U41	GRAPHS_CSR		10.0
U42	GRAPHS_CSR		10.0
U43	GRAPHS_CSR		10.0
U44	GRAPHS_CSR		10.0
U45	GRAPHS_CSR		10.0
U46	GRAPHS_CSR		10.0
U47	GRAPHS_CSR		10.0
U48	GRAPHS_CSR		10.0
U49	GRAPHS_CSR		10.0
U50	GRAPHS_CSR		10.0
U51	GRAPHS_CSR		10.0
U52	GRAPHS_CSR		10.0
U53	GRAPHS_CSR		10.0
U54	GRAPHS_CSR		10.0
U55	GRAPHS_CSR		10.0
U56	GRAPHS_CSR		10.0
U57	GRAPHS_CSR		10.0
U58	GRAPHS_CSR		10.0
U59	GRAPHS_CSR		10.0
U60	GRAPHS_CSR		10.0
U61	GRAPHS_CSR		10.0
U62	GRAPHS_CSR		10.0
U63	GRAPHS_CSR		10.0
U64	GRAPHS_CSR		10.0
U65	GRAPHS_CSR		10.0
U66	GRAPHS_CSR		10.0
U67	GRAPHS_CSR		10.0
U68	GRAPHS_CSR		10.0
U69	GRAPHS_CSR		10.0
U70	GRAPHS_CSR		10.0
U71	GRAPHS_CSR		10.0
U72	GRAPHS_CSR		10.0
U73	GRAPHS_CSR		10.0
U74	GRAPHS_CSR		10.0
U75	GRAPHS_CSR		10.0
U76	GRAPHS_CSR		10.0
U77	GRAPHS_CSR		10.0
U78	GRAPHS_CSR		10.0
U79	GRAPHS_CSR		10.0
U80	GRAPHS_CSR		10.0
U81	GRAPHS_CSR		10.0
U82	GRAPHS_CSR		10.0
U83	GRAPHS_CSR		10.0
U84	GRAPHS_CSR		10.0
U85	GRAPHS_CSR		10.0
U86	GRAPHS_CSR		10.0
U87	GRAPHS_CSR		10.0
U88	GRAPHS_CSR		10.0
U89	GRAPHS_CSR		10.0
U90	GRAPHS_CSR		10.0
U91	GRAPHS_CSR		10.0
U92	GRAPHS_CSR		10.0
U93	GRAPHS_CSR		10.0
U94	GRAPHS_CSR		10.0
U95	GRAPHS_CSR		10.0
U96	GRAPHS_CSR		10.0
U97	GRAPHS_CSR		10.0
U98	GRAPHS_CSR		10.0
U99	GRAPHS_CSR		10.0
U100	GRAPHS_CSR		10.0
U101	GRAPHS_CSR		10.0
U102	GRAPHS_CSR		10.0
U103	GRAPHS_CSR		10.0
U104	GRAPHS_CSR		10.0
U105	GRAPHS_CSR		10.0
U106	GRAPHS_CSR		10.0
U107	GRAPHS_CSR		10.0
U108	GRAPHS_CSR		10.0
U109	GRAPHS_CSR		10.0
U110	GRAPHS_CSR		10.0
U111	GRAPHS_CSR		10.0
U112	GRAPHS_CSR		10.0
U113	GRAPHS_CSR		10.0
U114	GRAPHS_CSR		10.0
U115	GRAPHS_CSR		10.0
U116	GRAPHS_CSR		10.0
U117	GRAPHS_CSR		10.0
U118	GRAPHS_CSR		10.0
U119	GRAPHS_CSR		10.0
U120	GRAPHS_CSR		10.0
U121	GRAPHS_CSR		10.0
U122	GRAPHS_CSR		10.0
U123	GRAPHS_CSR		10.0
U124	GRAPHS_CSR		10.0
U125	GRAPHS_CSR		10.0
U126	GRAPHS_CSR		10.0
U127	GRAPHS_CSR		10.0
U128	GRAPHS_CSR		10.0
U129	GRAPHS_CSR		10.0
U130	GRAPHS_CSR		10.0
U131	GRAPHS_CSR		10.0
U132	GRAPHS_CSR		10.0
U133	GRAPHS_CSR		10.0
U134	GRAPHS_CSR		10.0
U135	GRAPHS_CSR		10.0
U136	GRAPHS_CSR		10.0
U137	GRAPHS_CSR		10.0
U138	GRAPHS_CSR		10.0
U139	GRAPHS_CSR		10.0
U140	GRAPHS_CSR		10.0
U141	GRAPHS_CSR		10.0
U142	GRAPHS_CSR		10.0
U143	GRAPHS_CSR		10.0
U144	GRAPHS_CSR		10.0
U145	GRAPHS_CSR		10.0
U146	GRAPHS_CSR		10.0
U147	GRAPHS_CSR		10.0
U148	GRAPHS_CSR		10.0
U149	GRAPHS_CSR		10.0
U150	GRAPHS_CSR		10.0
U151	GRAPHS_CSR		10.0
U152	GRAPHS_CSR		10.0
U153	GRAPHS_CSR		10.0
U154	GRAPHS_CSR		10.0
U155	GRAPHS_CSR		10.0
U156	GRAPHS_CSR		10.0
U157	GRAPHS_CSR		10.0
U158	GRAPHS_CSR		10.0
U159	GRAPHS_CSR		10.0
U160	GRAPHS_CSR		10.0
U161	GRAPHS_CSR		10.0
U162	GRAPHS_CSR		10.0
U163	GRAPHS_CSR		10.0
U164	GRAPHS_CSR		10.0
U165	GRAPHS_CSR		10.0
U166	GRAPHS_CSR		10.0
U167	GRAPHS_CSR		10.0
U168	GRAPHS_CSR		10.0
U169	GRAPHS_CSR		10.0
U170	GRAPHS_CSR		10.0
U171	GRAPHS_CSR		10.0
U172	GRAPHS_CSR		10.0
U173	GRAPHS_CSR		10.0
U174	GRAPHS_CSR		10.0
U175	GRAPHS_CSR		10.0
U176	GRAPHS_CSR		10.0
U177	GRAPHS_CSR		10.0
U178	GRAPHS_CSR		10.0
U179	GRAPHS_CSR		10.0
U180	GRAPHS_CSR		10.0
U181	GRAPHS_CSR		10.0
U182	GRAPHS_CSR		10.0
U183	GRAPHS_CSR		10.0
U184	GRAPHS_CSR		10.0
U185	GRAPHS_CSR		10.0
U186	GRAPHS_CSR		10.0
U187	GRAPHS_CSR		10.0
U188	GRAPHS_CSR		10.0
U189	GRAPHS_CSR		10.0
U190	GRAPHS_CSR		10.0
U191	GRAPHS_CSR		10.0
U192	GRAPHS_CSR		10.0
U193	GRAPHS_CSR		10.0
U194	GRAPHS_CSR		10.0
U195	GRAPHS_CSR		10.0
U196	GRAPHS_CSR		10.0
U197	GRAPHS_CSR		10.0
U198	GRAPHS_CSR		10.0
U199	GRAPHS_CSR		10.0
U200	GRAPHS_CSR		10.0
U201	GRAPHS_CSR		10.0
U202	GRAPHS_CSR		10.0
U203	GRAPHS_CSR		10.0
U204	GRAPHS_CSR		10.0
U205	GRAPHS_CSR		10.0
U206	GRAPHS_CSR		10.0
U207	GRAPHS_CSR		10.0
U208	GRAPHS_CSR		10.0
U209	GRAPHS_CSR		10.0
U210	GRAPHS_CSR		10.0
U211	GRAPHS_CSR		10.0
U212	GRAPHS_CSR		10.0
U213	GRAPHS_CSR		10.0
U214	GRAPHS_CSR		10.0
U215	GRAPHS_CSR		10.0
U216	GRAPHS_CSR		10.0
U217	GRAPHS_CSR		10.0
U218	GRAPHS_CSR		10.0
U219	GRAPHS_CSR		10.0
U220	GRAPHS_CSR		10.0
U221	GRAPHS_CSR		10.0
U222	GRAPHS_CSR		10.0
U223	GRAPHS_CSR		10.0
U224	GRAPHS_CSR		10.0
U225	GRAPHS_CSR		10.0
U226	GRAPHS_CSR		10.0
U227	GRAPHS_CSR		10.0
U228	GRAPHS_CSR		10.0
U229	GRAPHS_CSR		10.0
U230	GRAPHS_CSR		10.0
U231	GRAPHS_CSR		10.0
U232	GRAPHS_CSR		10.0
U233	GRAPHS_CSR		10.0
U234	GRAPHS_CSR		10.0
U235	GRAPHS_CSR		10.0
U236	GRAPHS_CSR		10.0
U237	GRAPHS_CSR		10.0
U238	GRAPHS_CSR		10.0
U239	GRAPHS_CSR		10.0
U240	GRAPHS_CSR		10.0
U241	GRAPHS_CSR		10.0
U242	GRAPHS_CSR		10.0
U243	GRAPHS_CSR		10.0
U244	GRAPHS_CSR		10.0
U245	GRAPHS_CSR		10.0
U246	GRAPHS_CSR		10.0
U247	GRAPHS_CSR		10.0
U248	GRAPHS_CSR		10.0
U249	GRAPHS_CSR		10.0
U250	GRAPHS_CSR		10.0
U251	GRAPHS_CSR		10.0
U252	GRAPHS_CSR		10.0
U253	GRAPHS_CSR		10.0
U254	GRAPHS_CSR		10.0
U255	GRAPHS_CSR		10.0
U256	GRAPHS_CSR		10.0
U257	GRAPHS_CSR		10.0
U258	GRAPHS_CSR		10.0
U259	GRAPHS_CSR		10.0
U260	GRAPHS_CSR		10.0
U261	GRAPHS_CSR		10.0
U262	GRAPHS_CSR		10.0
U263	GRAPHS_CSR		10.0
U264	GRAPHS_CSR		10.0
U265	GRAPHS_CSR		10.0
U266	GRAPHS_CSR		10.0
U267	GRAPHS_CSR		10.0
U268	GRAPHS_CSR		10.0
U269	GRAPHS_CSR		10.0
U270	GRAPHS_CSR		10.0
U271	GRAPHS_CSR		10.0
U272	GRAPHS_CSR		10.0
U273	GRAPHS_CSR		10.0
U274	GRAPHS_CSR		10.0
U275	GRAPHS_CSR		10.0
U276	GRAPHS_CSR		10.0
U277	GRAPHS_CSR		10.0
U278	GRAPHS_CSR		10.0
U279	GRAPHS_CSR		10.0
U280	GRAPHS_CSR		10.0
U281	GRAPHS_CSR		10.0
U282	GRAPHS_CSR		10.0
U283	GRAPHS_CSR		10.0
U284	GRAPHS_CSR		10.0
U285	GRAPHS_CSR		10.0
U286	GRAPHS_CSR		10.0
U287	GRAPHS_CSR		10.0
U288	GRAPHS_CSR		10.0
U289	GRAPHS_CSR		10.0
U290	GRAPHS_CSR		10.0
U291	GRAPHS_CSR		10.0
U292	GRAPHS_CSR		10.0
U293	GRAPHS_CSR		10.0
U294	GRAPHS_CSR		10.0
U295	GRAPHS_CSR		10.0
U296	GRAPHS_CSR		10.0
U297	GRAPHS_CSR		10.0
U298	GRAPHS_CSR		10.0
U299	GRAPHS_CSR		10.0
U300	GRAPHS_CSR		10.0
U301	GRAPHS_CSR		10.0
U302	GRAPHS_CSR		10.0
U303	GRAPHS_CSR		10.0
U304	GRAPHS_CSR		10.0
U305	GRAPHS_CSR		10.0
U306	GRAPHS_CSR		10.0
U307	GRAPHS_CSR		10.0
U308	GRAPHS_CSR		10.0
U309	GRAPHS_CSR		10.0
U310	GRAPHS_CSR		10.0
U311	GRAPHS_CSR		10.0
U312	GRAPHS_CSR		10.0
U313	GRAPHS_CSR		10.0
U314	GRAPHS_CSR		10.0
U315	GRAPHS_CSR		10.0
U316	GRAPHS_CSR		10.0
U317	GRAPHS_CSR		10.0
U318	GRAPHS_CSR		10.0
U319	GRAPHS_CSR		10.0
U320	GRAPHS_CSR		10.0
U321	GRAPHS_CSR		10.0
U322	GRAPHS_CSR		10.0
U323	GRAPHS_CSR		10.0
U324	GRAPHS_CSR		10.0
U325	GRAPHS_CSR		10.0
U326	GRAPHS_CSR		10.0
U327	GRAPHS_CSR		10.0
U328	GRAPHS_CSR		10.0
U329	GRAPHS_CSR		10.0
U330	GRAPHS_CSR		10.0
U331	GRAPHS_CSR		10.0
U332	GRAPHS_CSR		10.0
U333	GRAPHS_CSR		10.0
U334	GRAPHS_CSR		10.0
U335	GRAPHS_CSR		10.0
U336	GRAPHS_CSR		10.0
U337	GRAPHS_CSR		10.0
U338	GRAPHS_CSR		10.0
U339	GRAPHS_CSR		10.0
U340	GRAPHS_CSR		10.0
U341	GRAPHS_CSR		10.0
U342	GRAPHS_CSR		10.0
U343	GRAPHS_CSR		10.0
U344	GRAPHS_CSR		10.0
U345	GRAPHS_CSR		10.0
U346	GRAPHS_CSR		10.0
U347	GRAPHS_CSR		10.0
U348	GRAPHS_CSR		10.0
U349	GRAPHS_CSR		10.0
U350	GRAPHS_CSR		10.0
U351	GRAPHS_CSR		10.0
U352	GRAPHS_CSR		10.0
U353	GRAPHS_CSR		10.0
U354	GRAPHS_CSR		10.0
U355	GRAPHS_CSR		10.0
U356			

NVIDIA CORPORATION

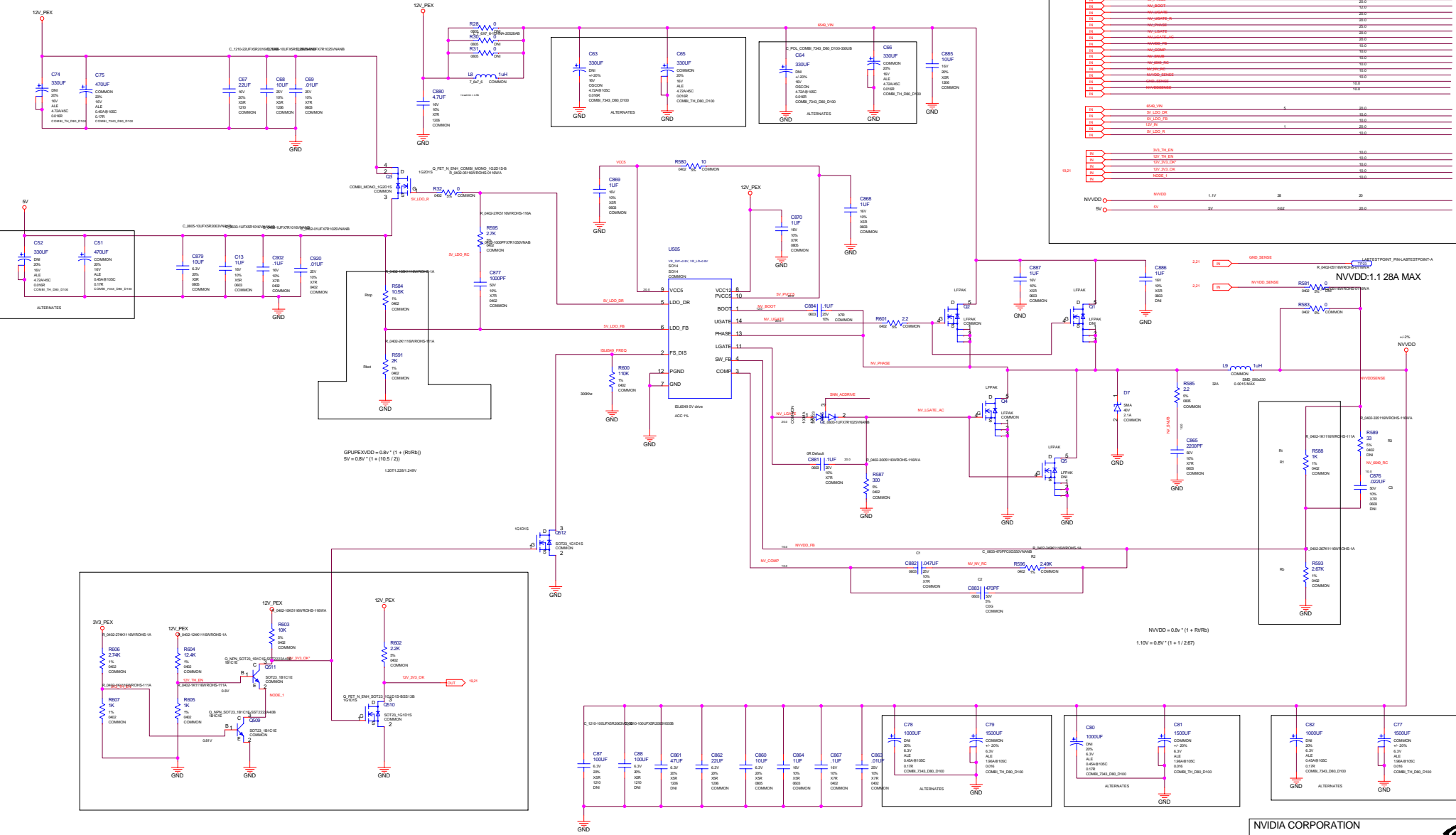
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



NV_PN	602-10345-base-sch		
ID		PAGE	
NAME		DATE	19-SEP-2005

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS; THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

Power Supply .. ISL6549 NVVDD,5V



ASSEMBLY		BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL	
PAGE DETAIL		POWER SUPPLY ISL6549 NVVDD, 5V	
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, OR INDUSTRY STANDARDS.		NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA	
NV_PN		602-10345-base-sch	
ID		PAGE	
NAME		DATE	
		19 SEP 2005	