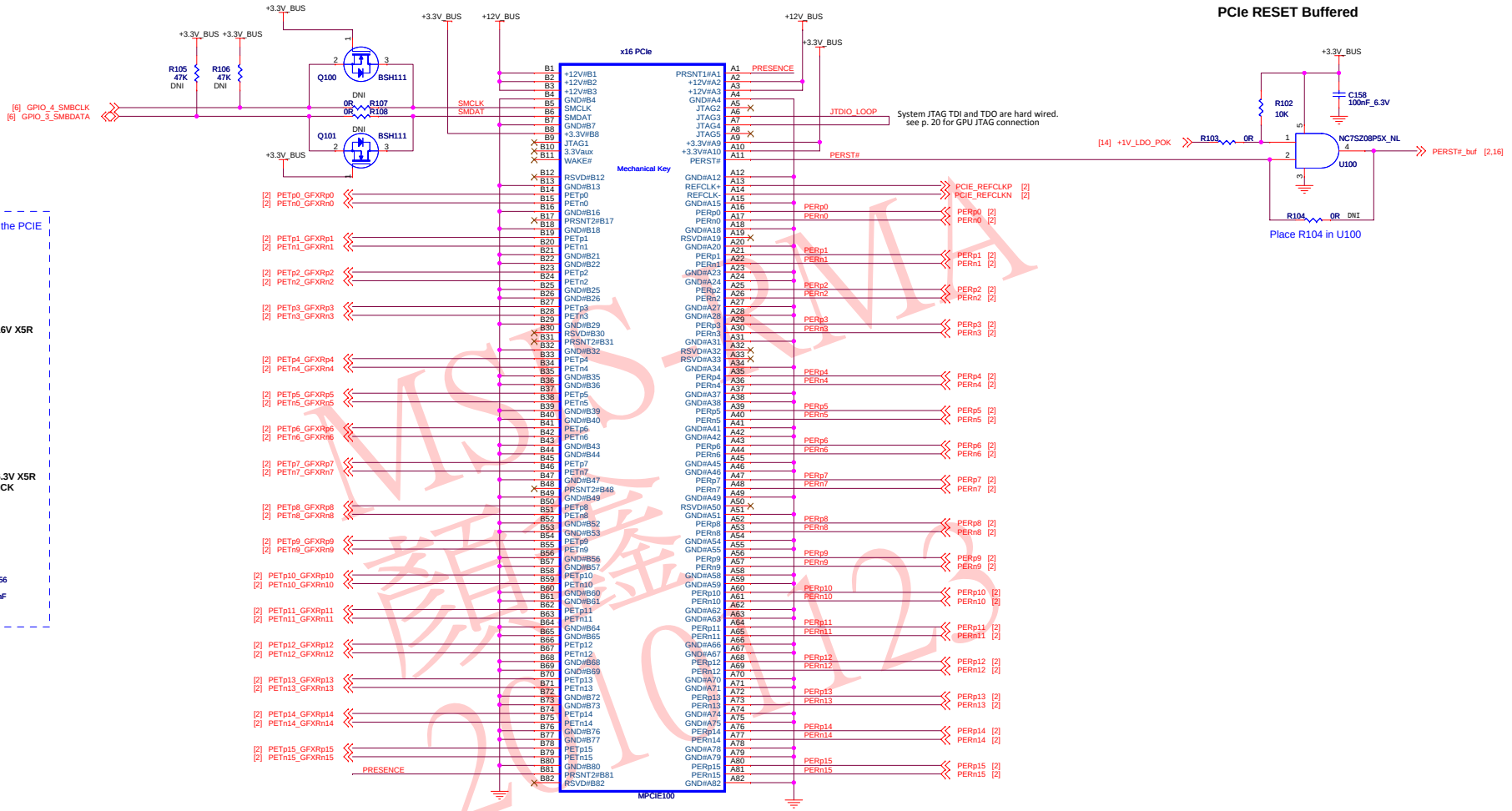
PCI-EXPRESS EDGE CONNECTOR

REDWOOD WOLVERINE



PCIe RESET Buffered

Place these caps as close to the PCIE connector as possible

+12V_BUS
C157 10UF
CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX

+12V_BUS
C151 150nF_16V
C152 150nF_16V

+3.3V_BUS
C153 10uF_X6S
CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

+3.3V_BUS
C154 100nF_6.3V
C155 1uF_6.3V
C156 10nF

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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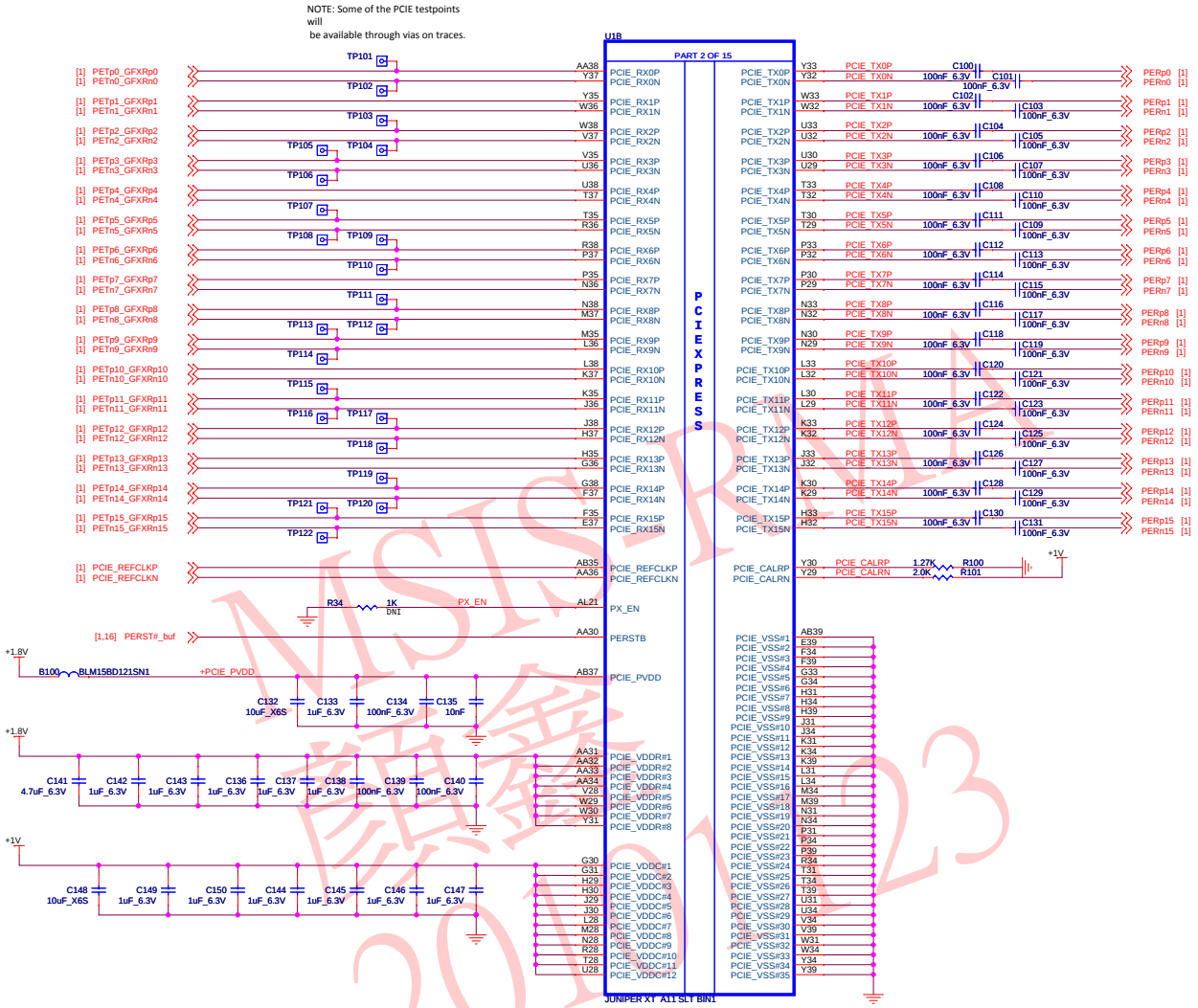
(2) REDWOOD PCIe Interface



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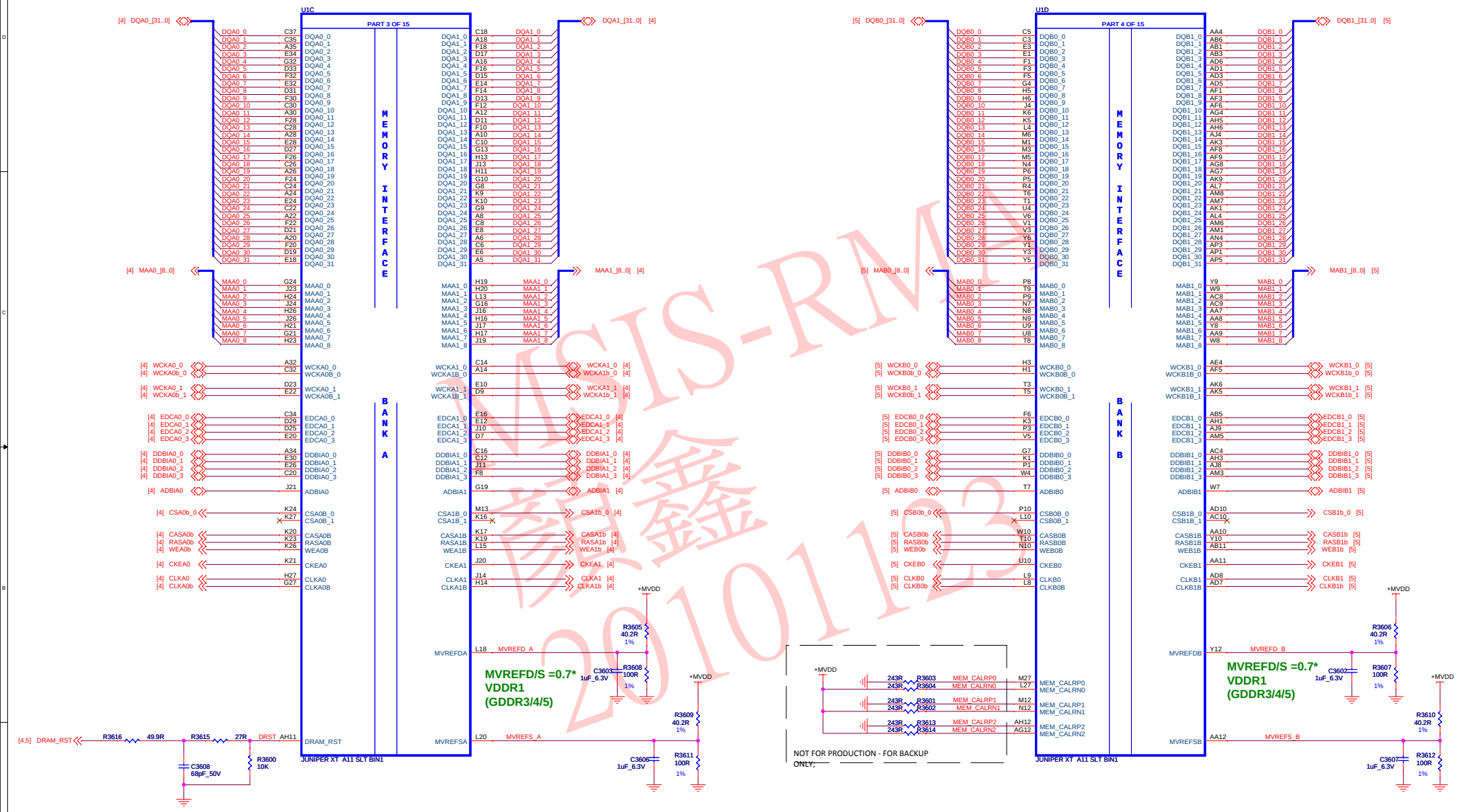
(3) REDWOOD MEM Interface Ch A&B



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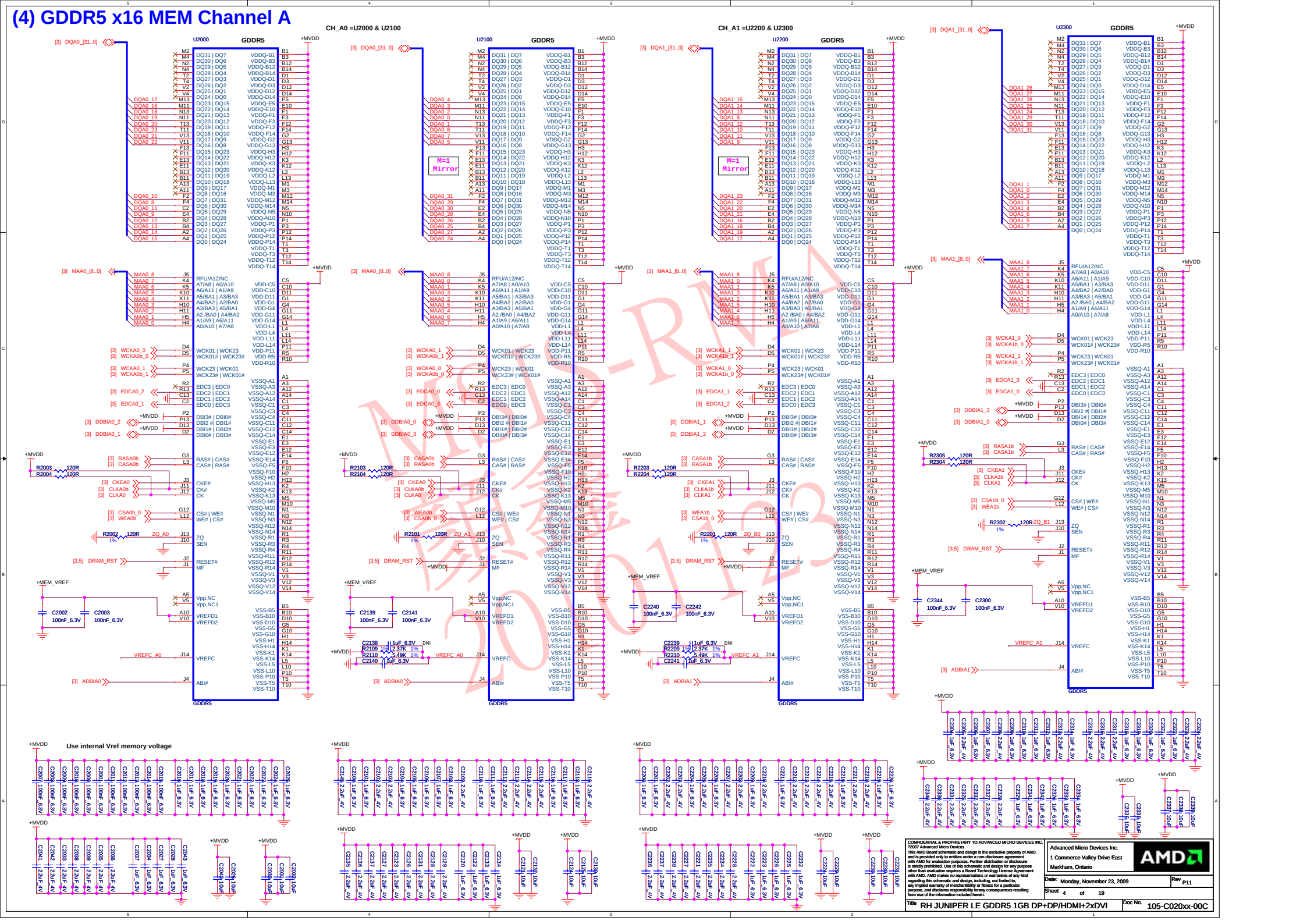
(4) GDDR5 x16 MEM Channel A



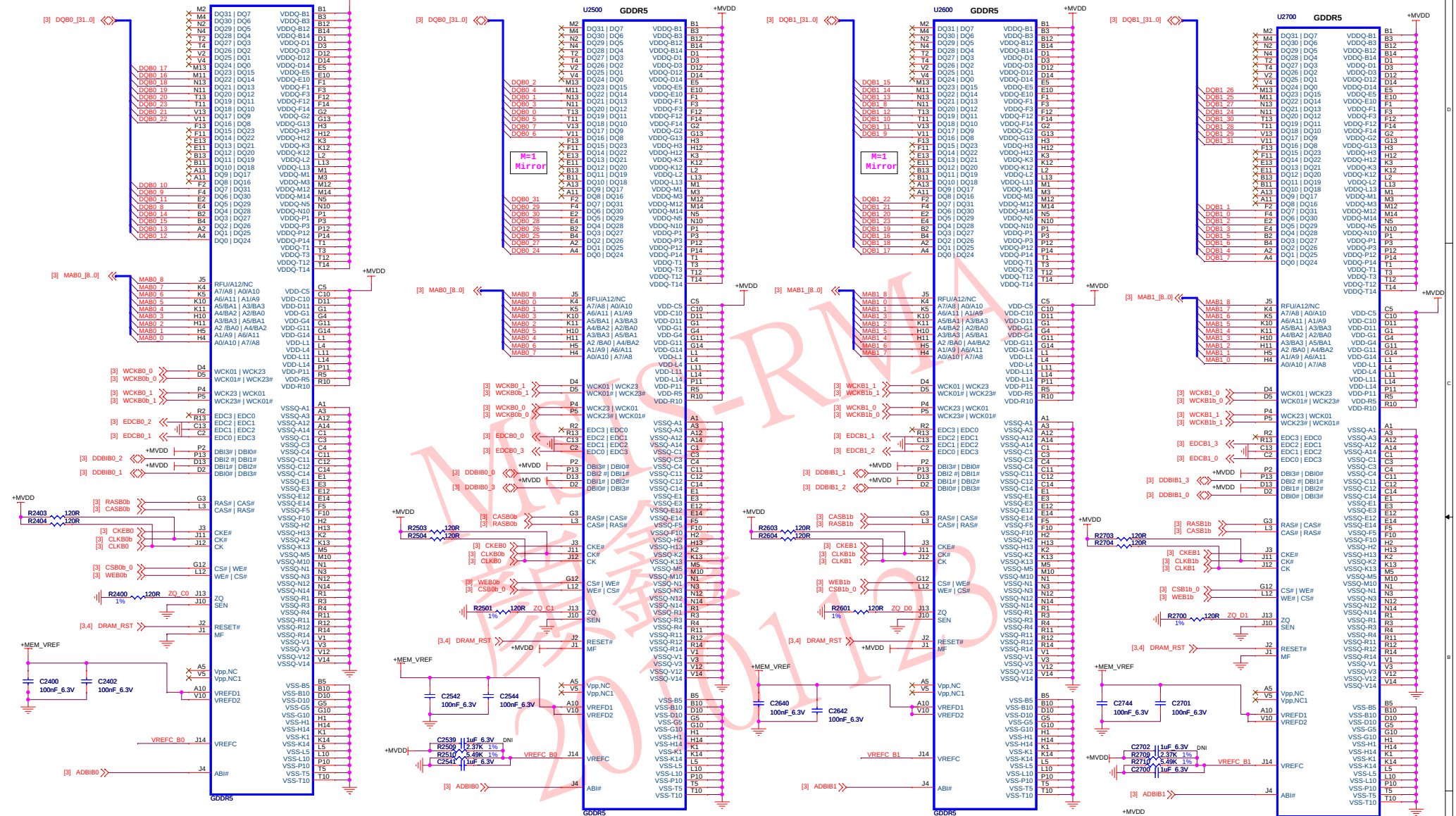
(5) GDDR5 x16 MEM Channel B

CH_B0 =U2400 & U2500

CH_B1 =U2600 & U2700

BOTTOM

TOP



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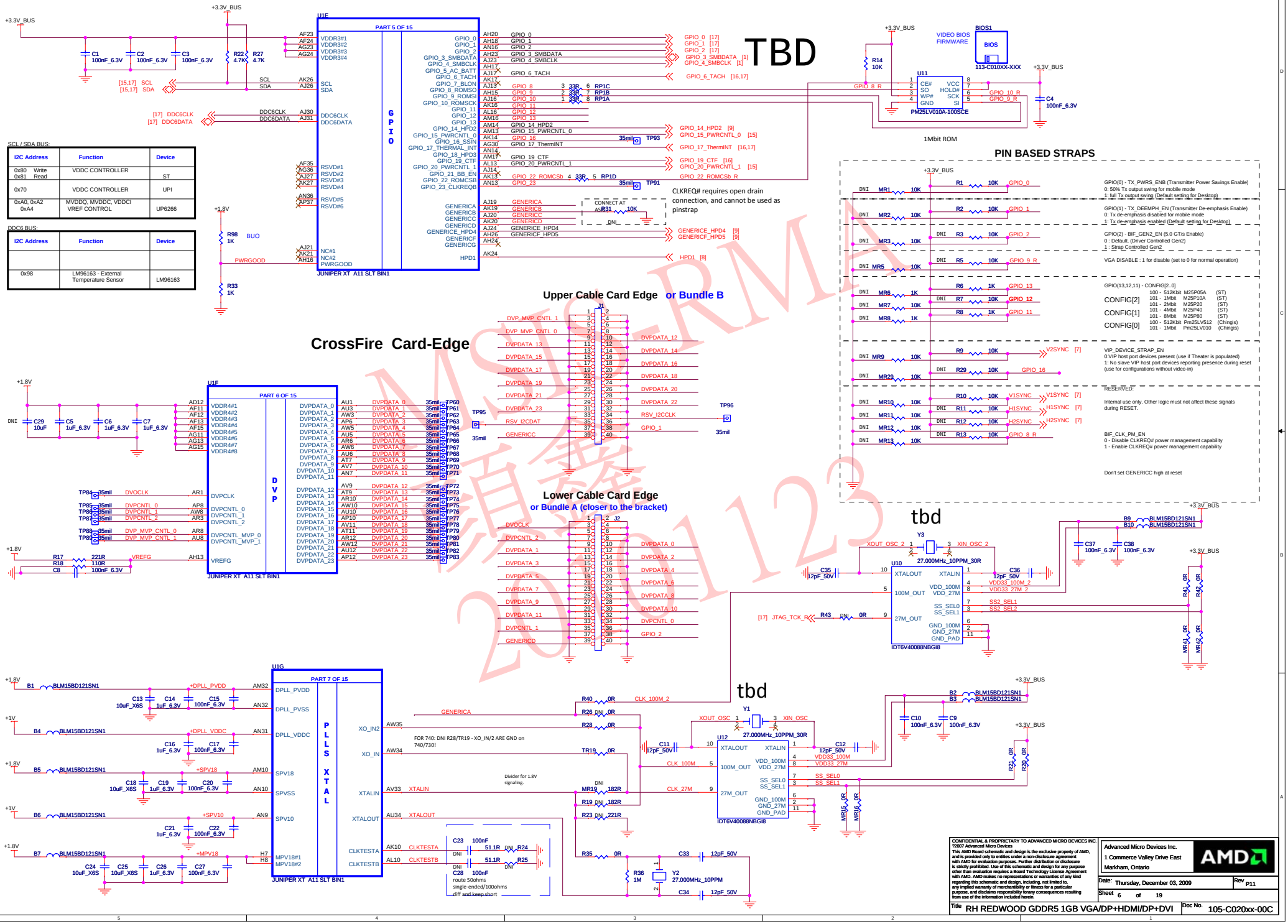
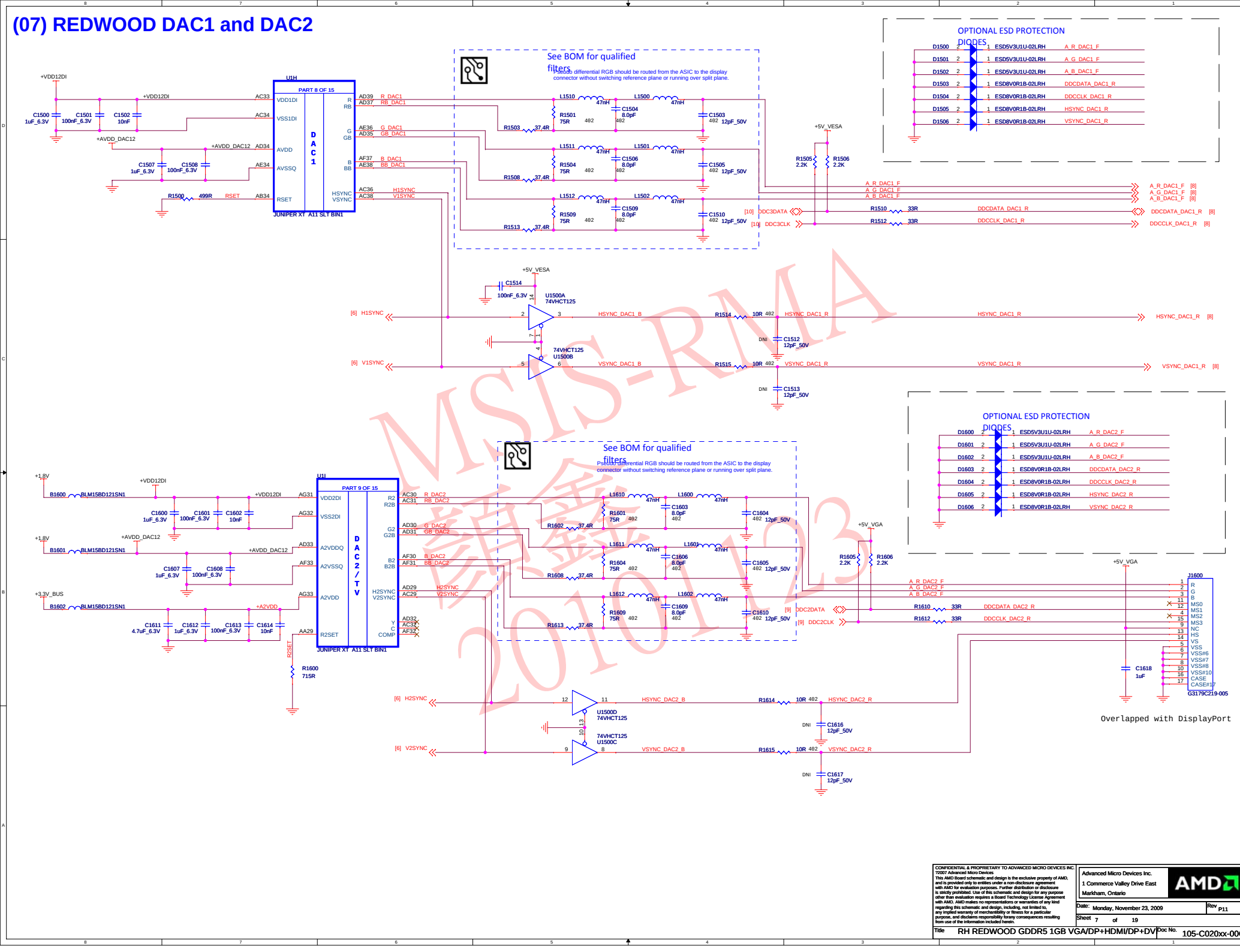
(06) REDWOOD GPIOs Strap CF XTAL OSC



(07) REDWOOD DAC1 and DAC2



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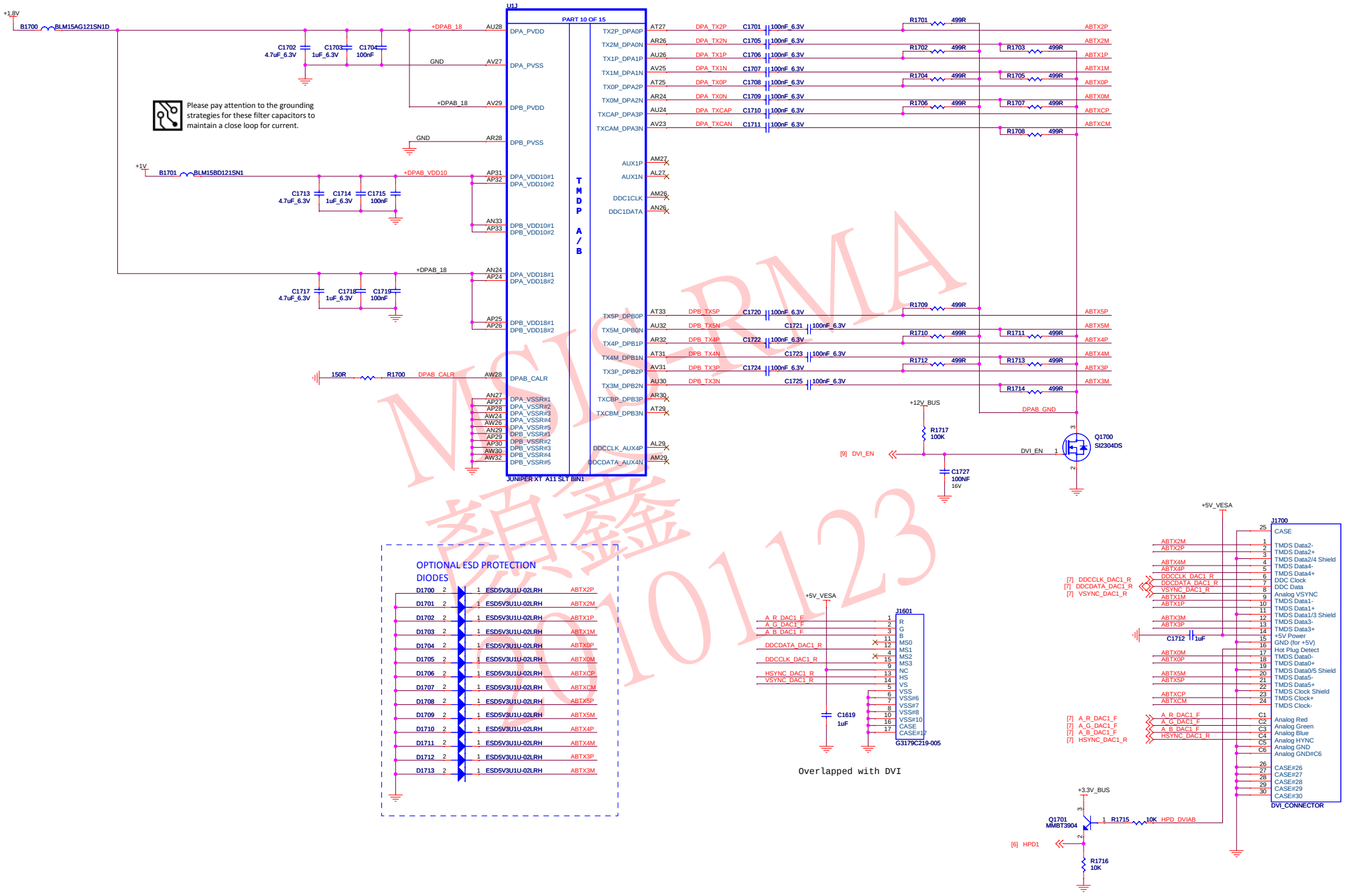
(08) REDWOOD TMDP A&B dDVI-I TOP



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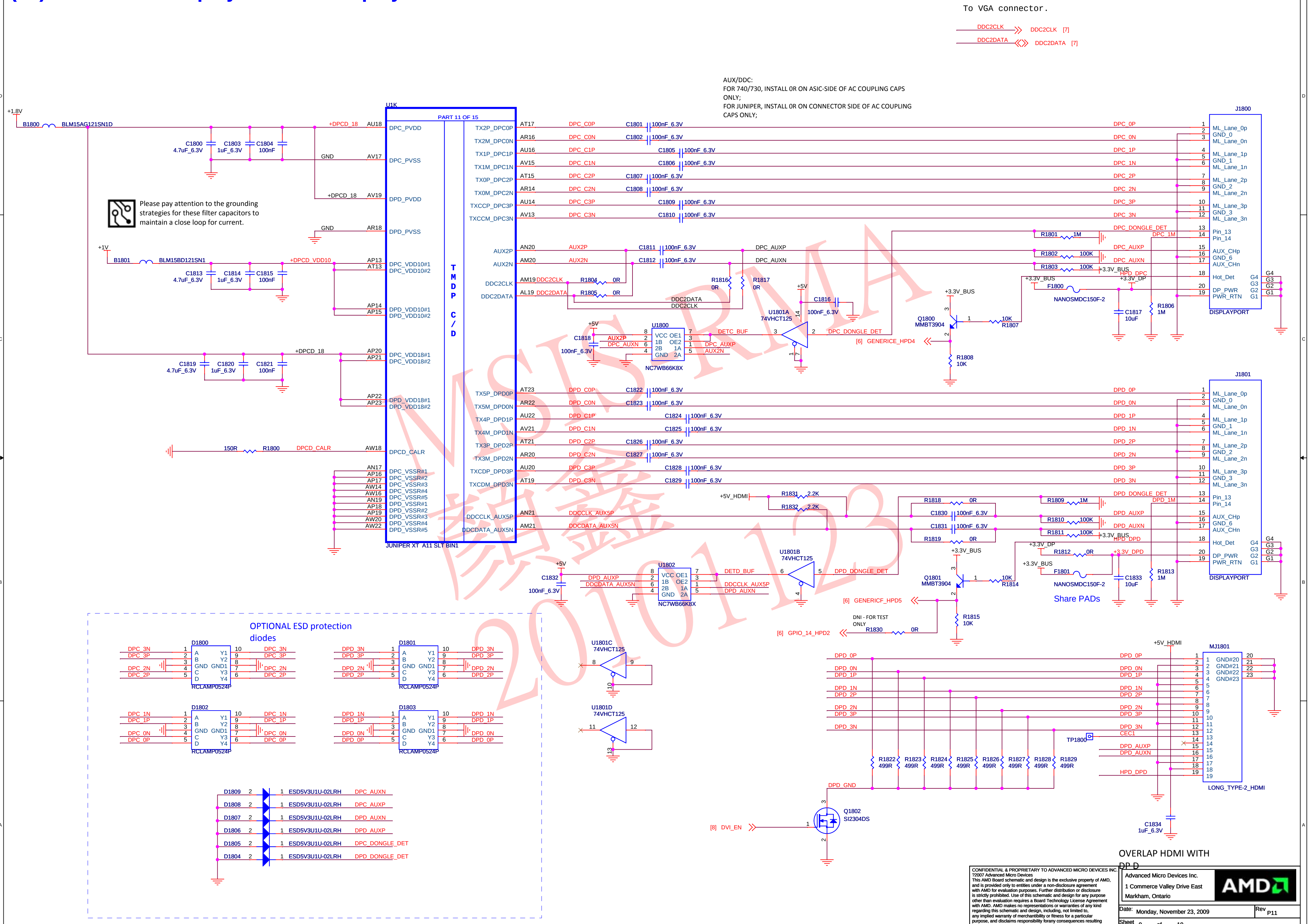
(09) REDWOOD Display Port C & Display Port/HDMI D



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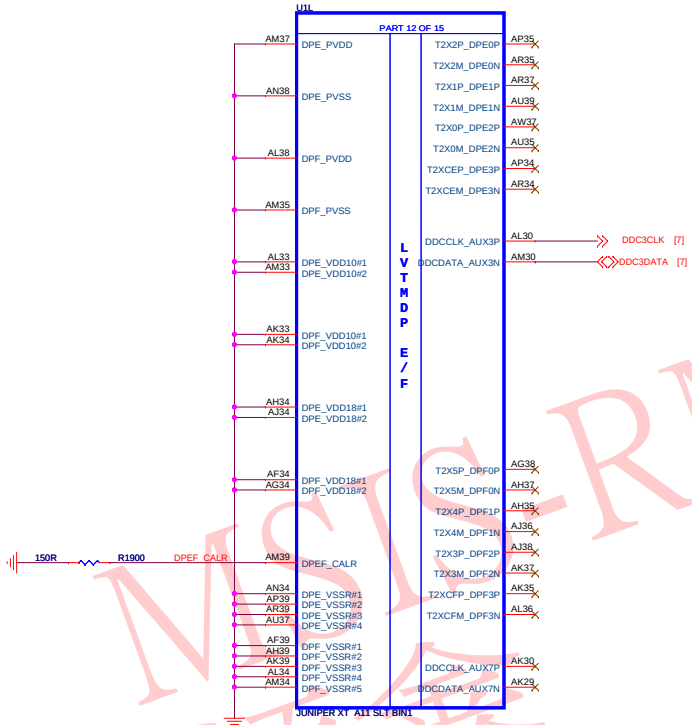
(10) REDWOOD LVTMDP E&F



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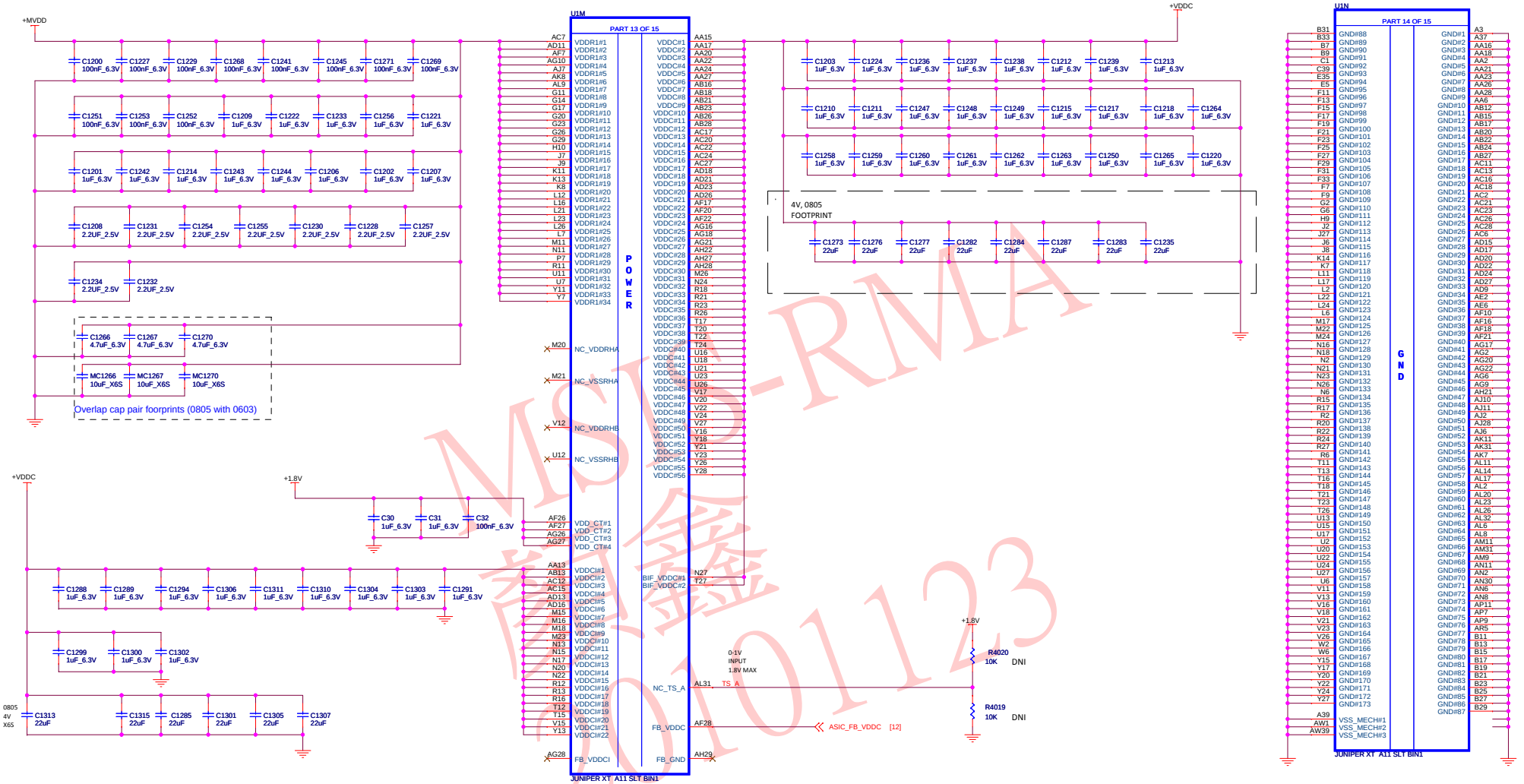
(11) REDWOOD Power & GND



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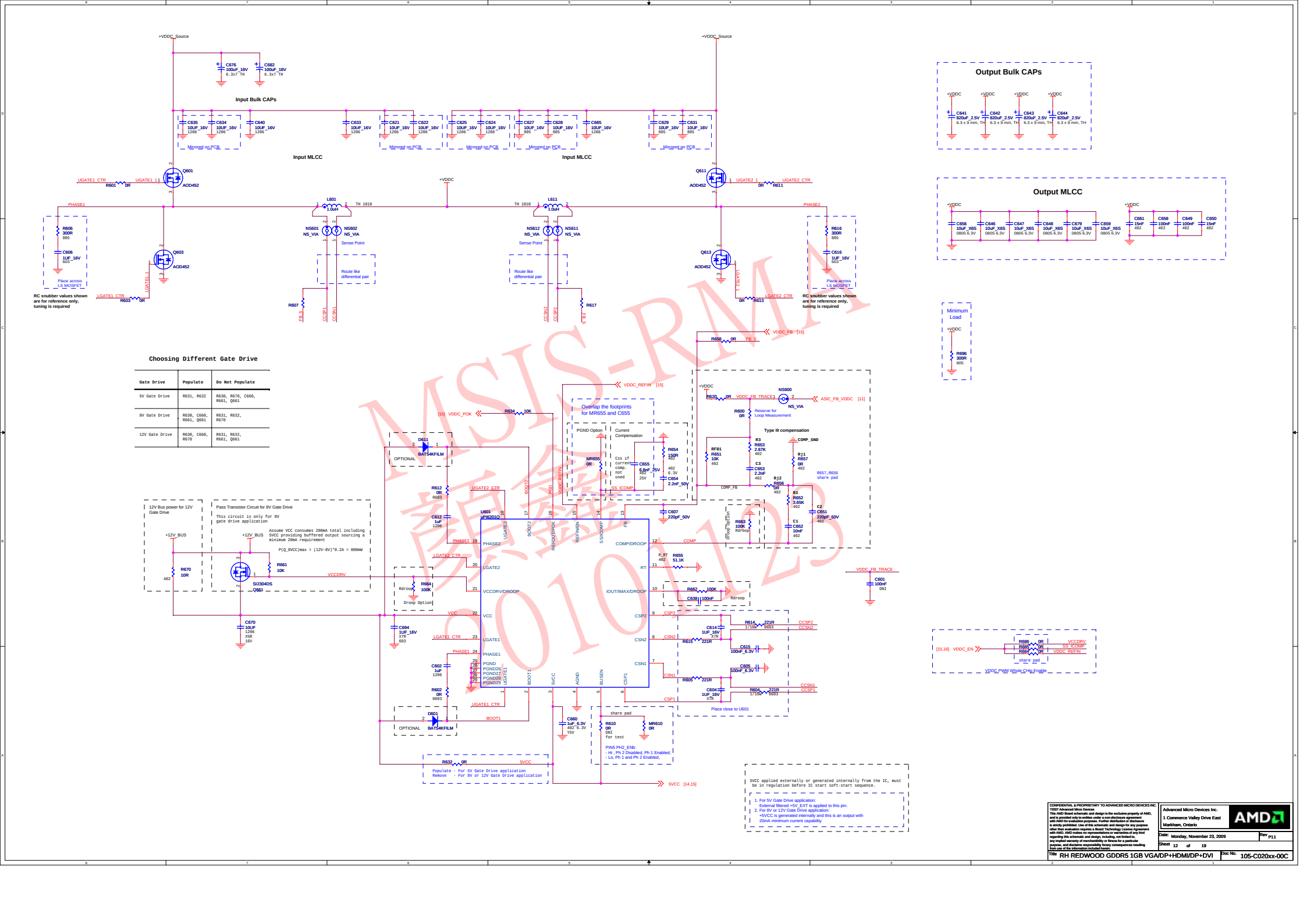
Input Bulk CAPs
Input MLCC
Output Bulk CAPs
Output MLCC
Minimum Load
Choosing Different Gate Drive
Gate Drive | Populate | Do Not Populate
5V Gate Drive | R631, R632 | R630, R670, C660, R661, Q661
8V Gate Drive | R630, C660, R661, Q661 | R631, R632, R670
12V Gate Drive | R630, C660, R670 | R631, R632, R661, Q661
Pass Transistor Circuit for 8V Gate Drive
This circuit is only for 8V gate drive application
Assume VCC consumes 200mA total including 5VCC providing buffered output sourcing a minimum 20mA requirement
P(Q_8VCC)max = (12V-8V)*0.2A = 800mW
12V Bus power for 12V Gate Drive
Overlap the footprints for MR655 and C655
Reserve for Loop Measurement
Type III compensation
Place close to U601
RC snubber values shown are for reference only, tuning is required
5VCC applied externally or generated internally from the IC, must be in regulation before IC start soft-start sequence.
1. For 5V Gate Drive application: External filtered +5V_EXT is applied to this pin.
2. For 8V or 12V Gate Drive application: +5VCC is generated internally and this is an output with 20mA minimum current capability
VDDC PWM Whole Chip Enable
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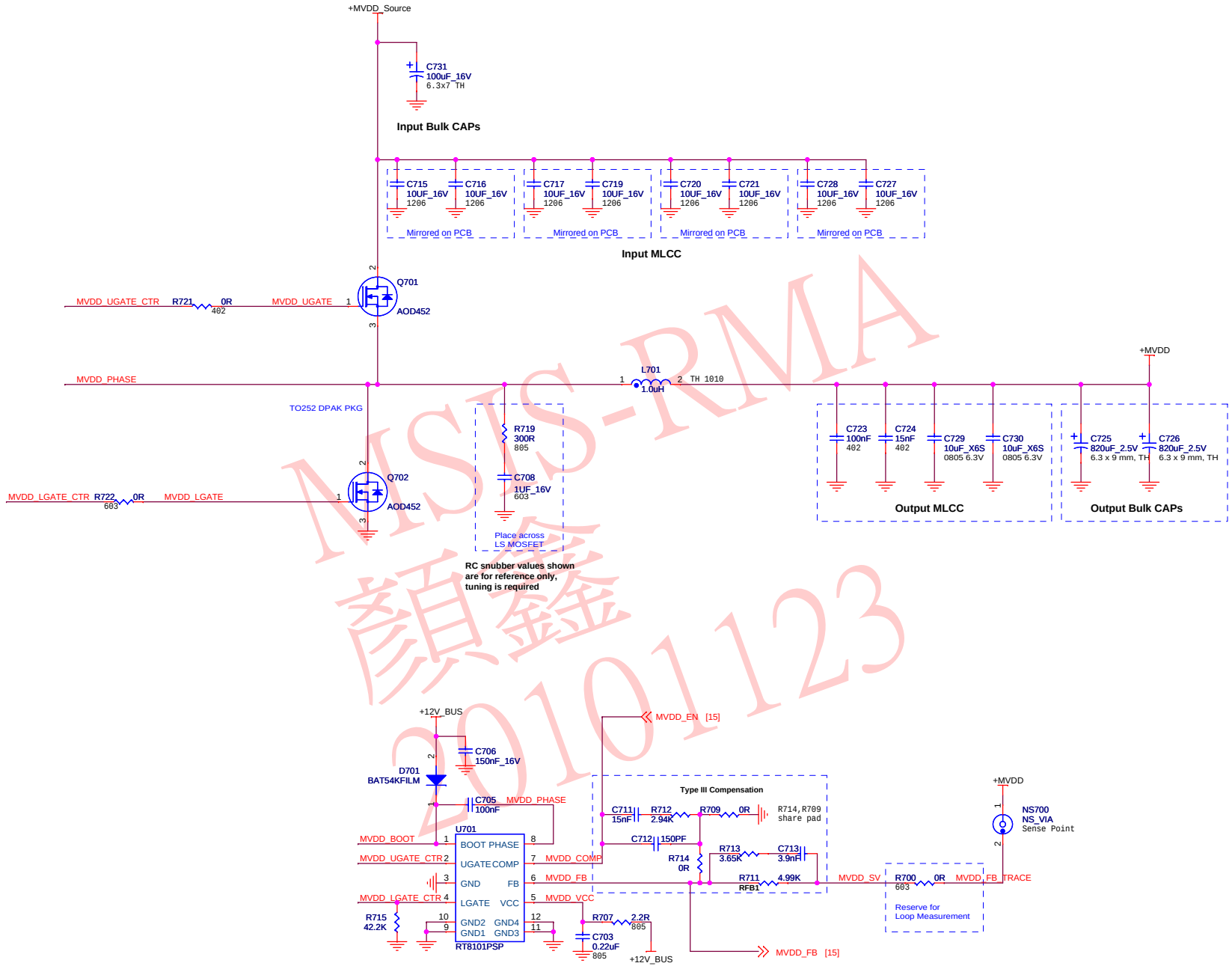

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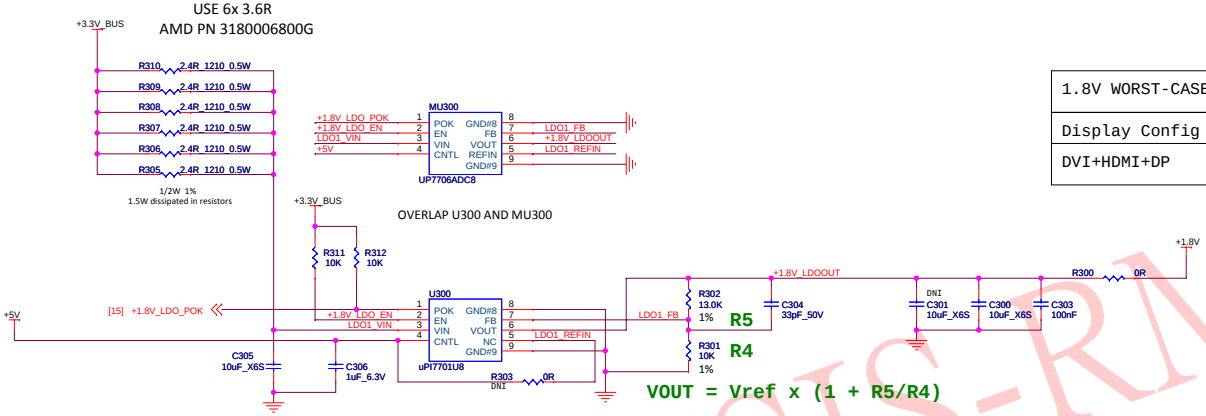
(15) Linear Regulators

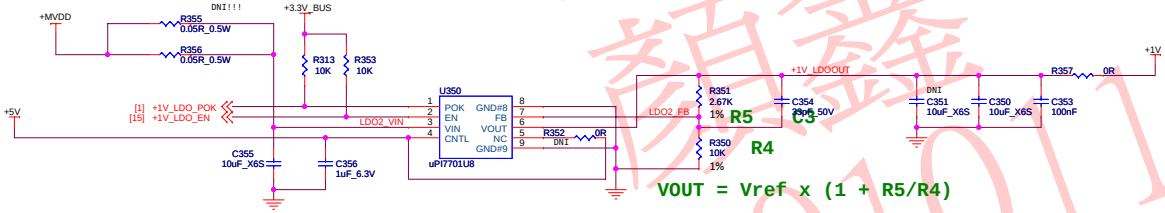
Regulators for +5V, +5V_VESA and +5V_HDMI

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



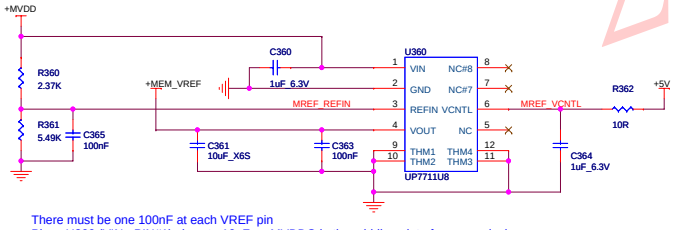
1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

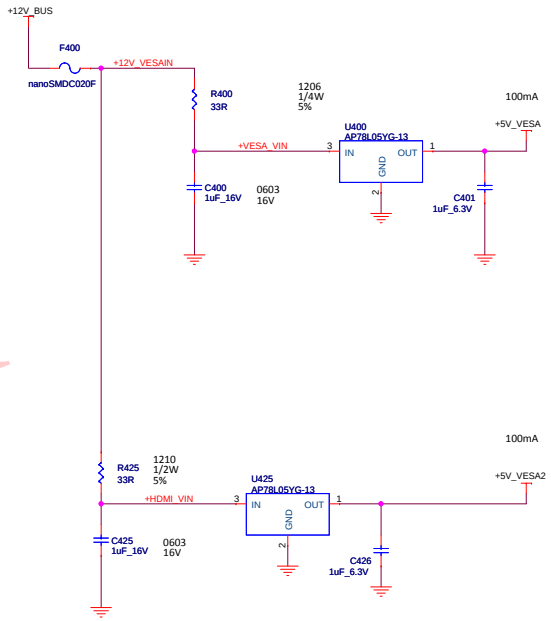


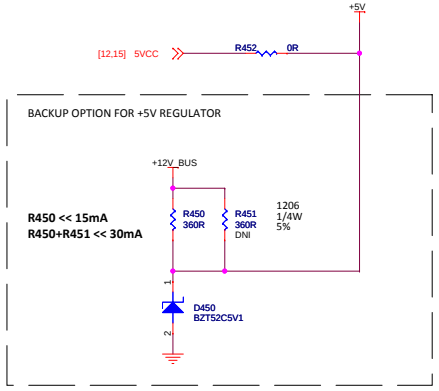
1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA

Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ



There must be one 100nF at each VREF pin
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices





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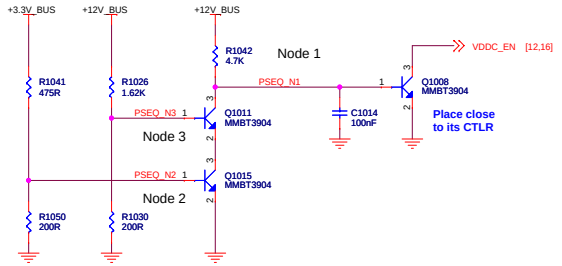
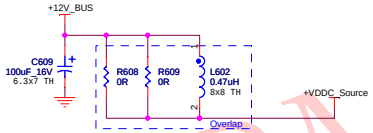
(16) Power Management - Power Gating and Dynamic Voltage Control

12V_BUS & 3V3_BUS POWER SEQUENCING



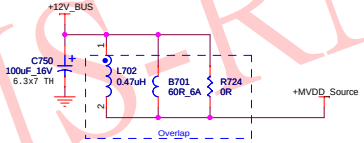
Install R1010 to gate 1V LDO with 1.8V LDO.

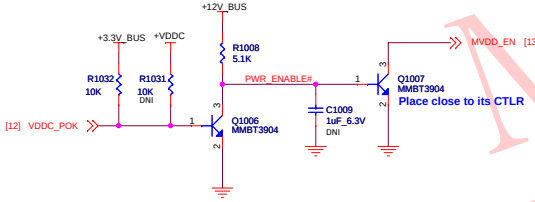
[14] +1.8V_LDO_POK — R1010 0R — +1V_LDO_EN [14]



MVDD Low Side Divider

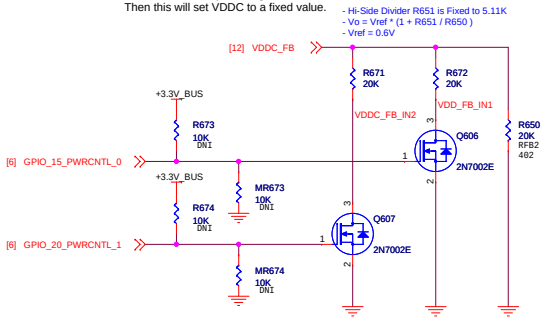
POWER SEQUENCING CIRCUIT

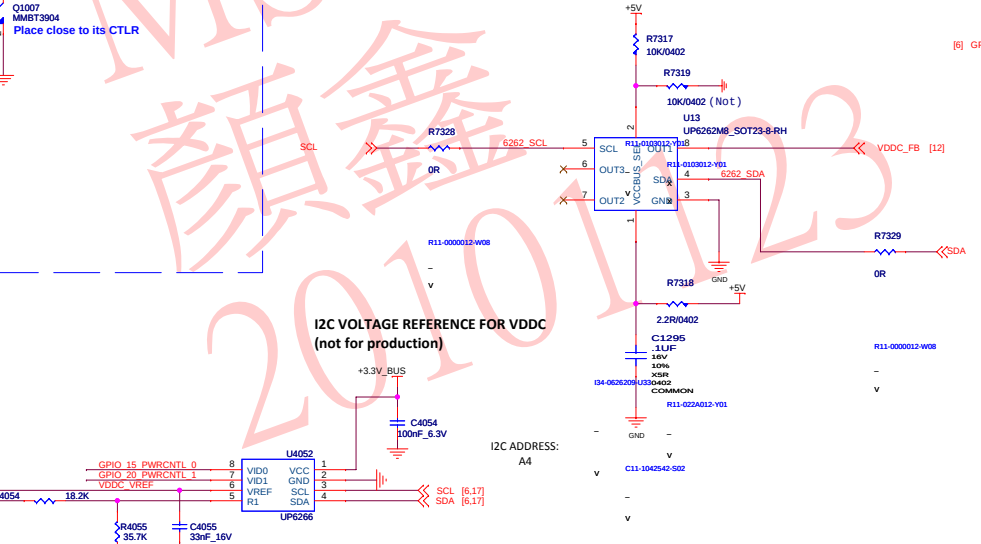




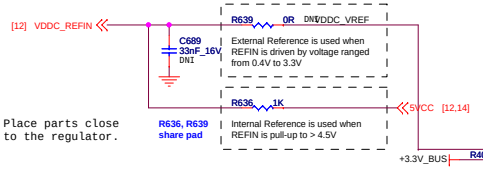
VDDC Low Side Divider

R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.





VDDC Reference Voltage Selection



I2C VOLTAGE REFERENCE FOR VDDC (not for production)

I2C ADDRESS: A4

VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

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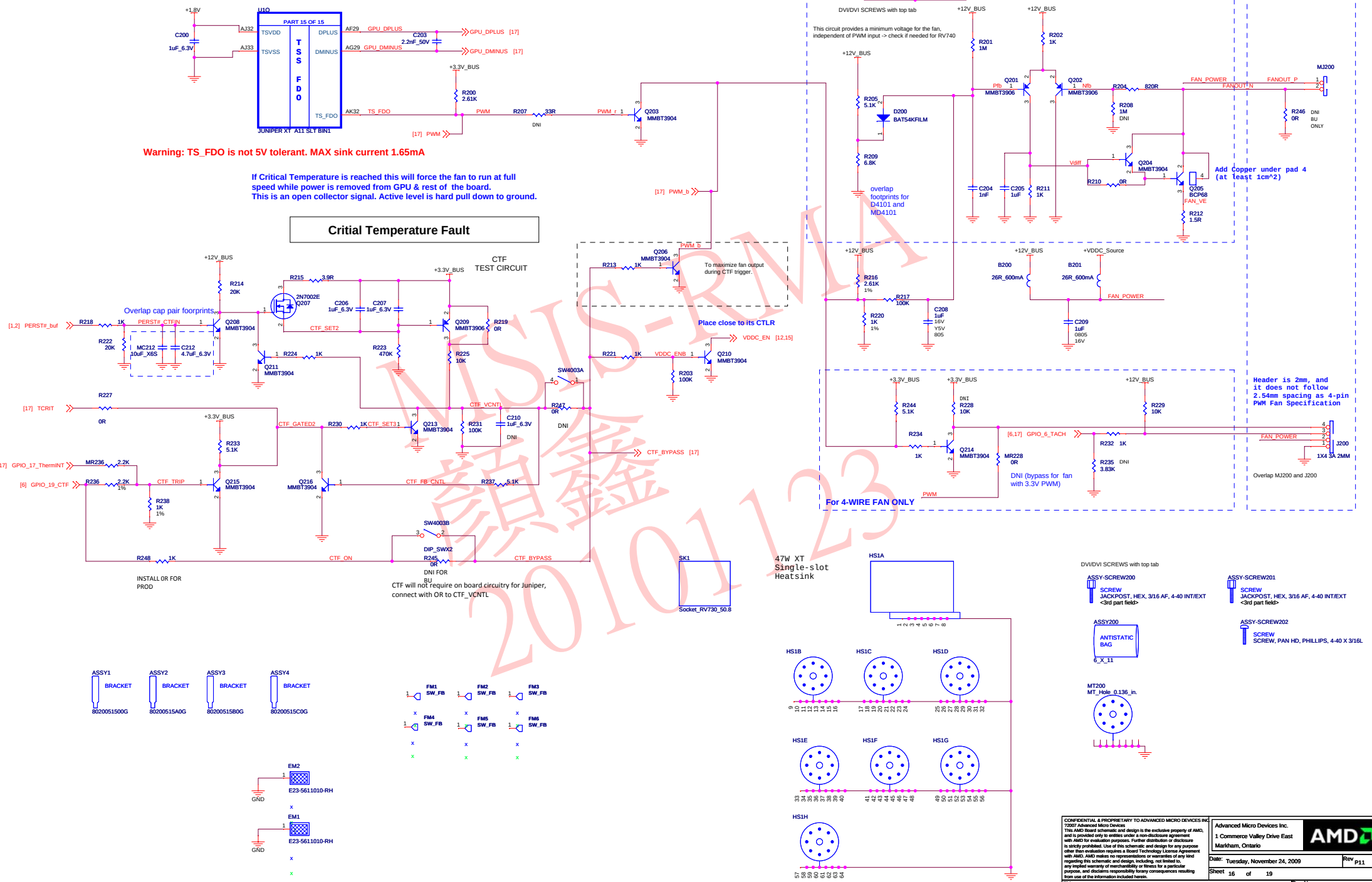
(19) Mechanical and Thermal Management



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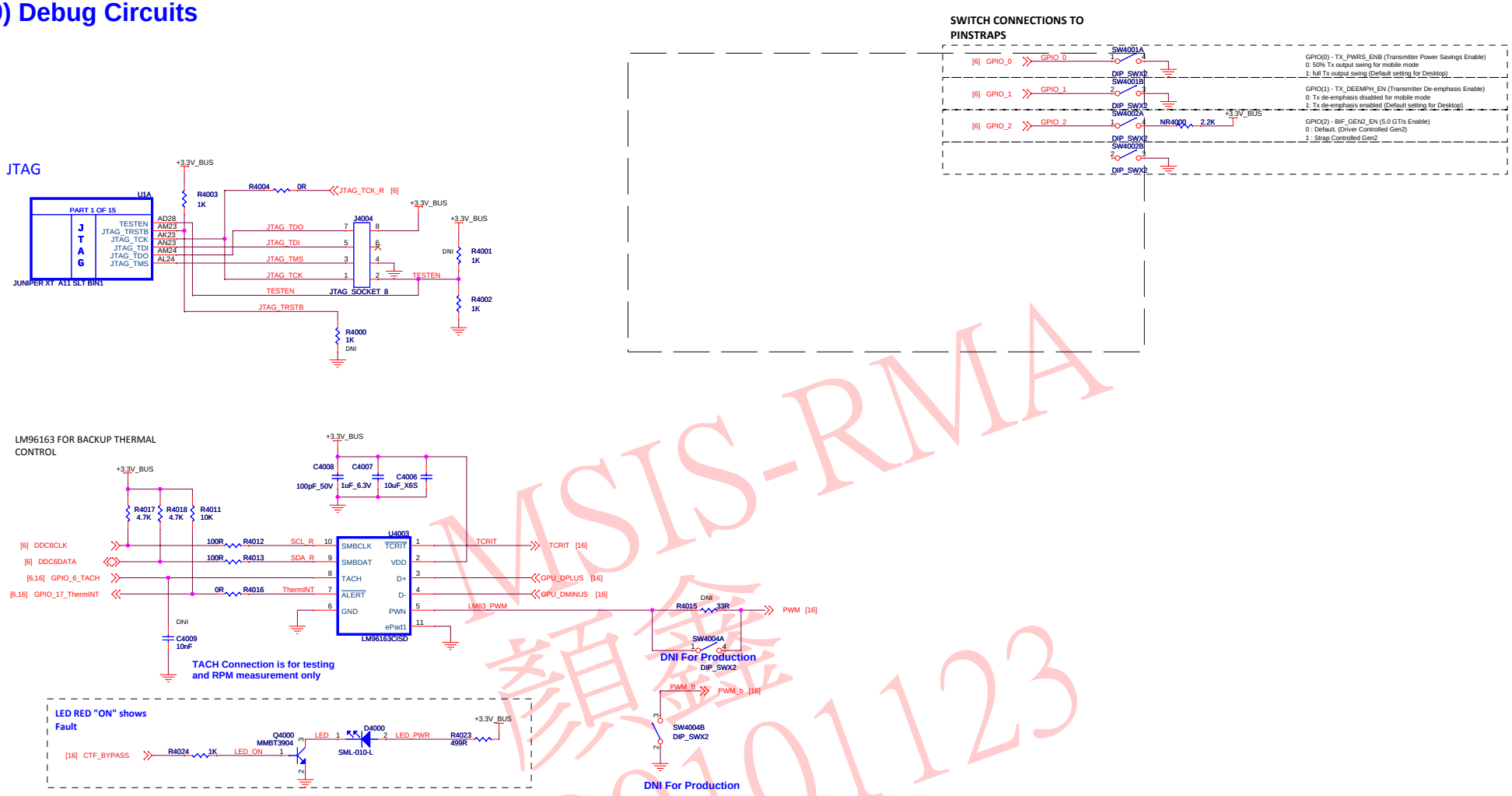
(19) Debug Circuits



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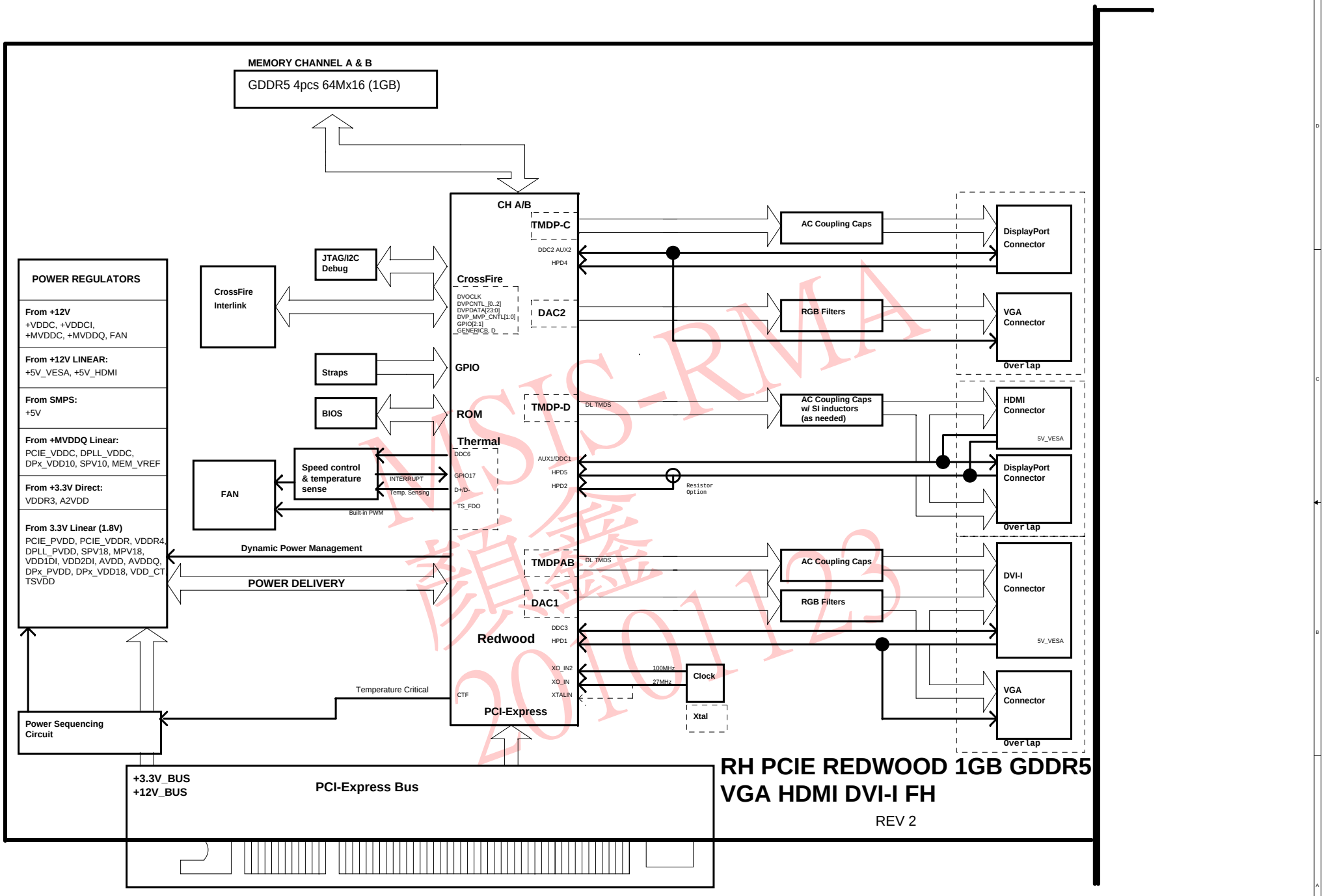

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Title	Schematic No.	Date:
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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI旧, ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

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Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/05/08	
01	00B	2009/08/20	
02	00C	2009/09/28	REDWOOD XT GDDR5 1GB - Initial Release