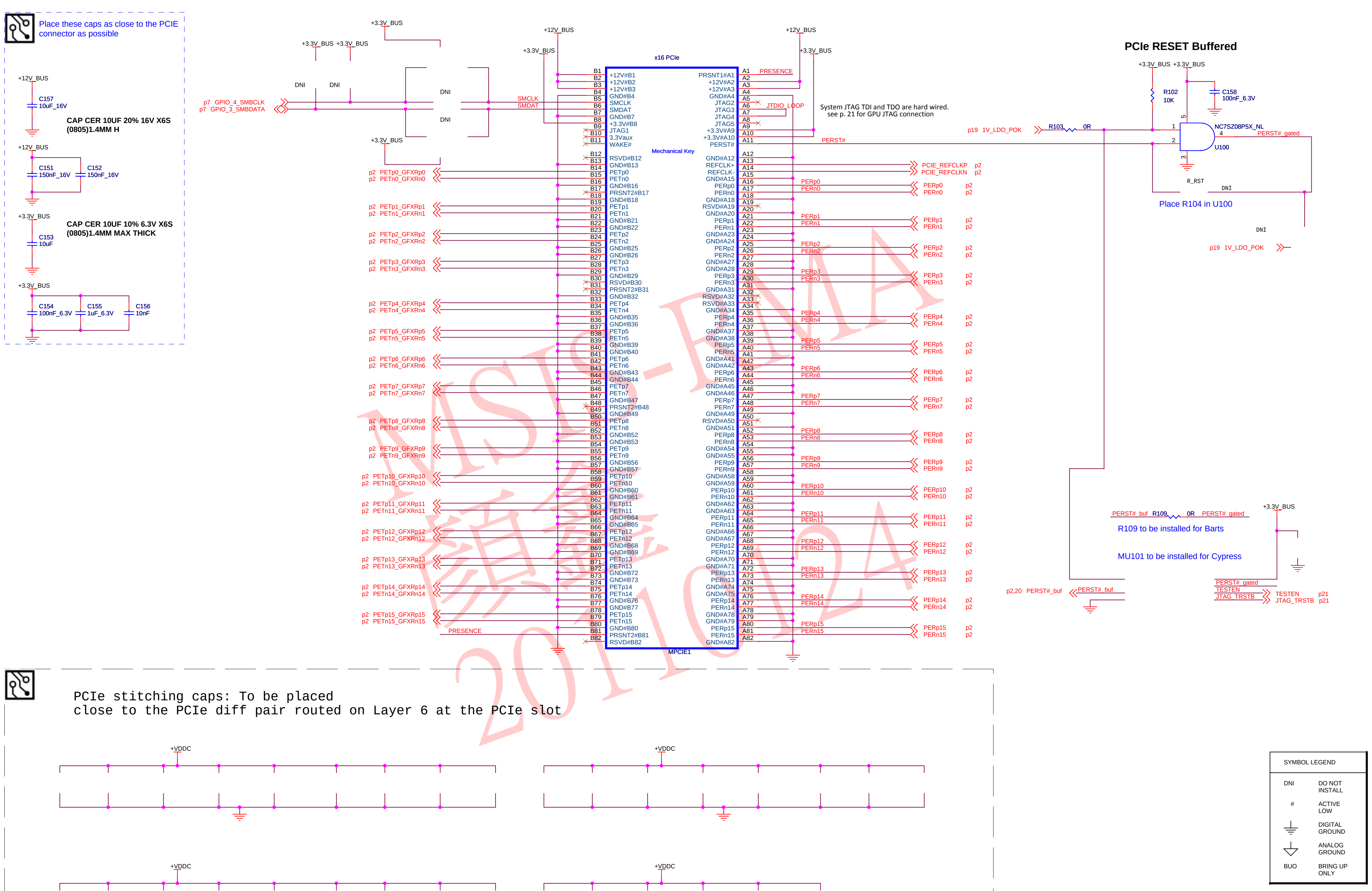
PCI-EXPRESS EDGE CONNECTOR



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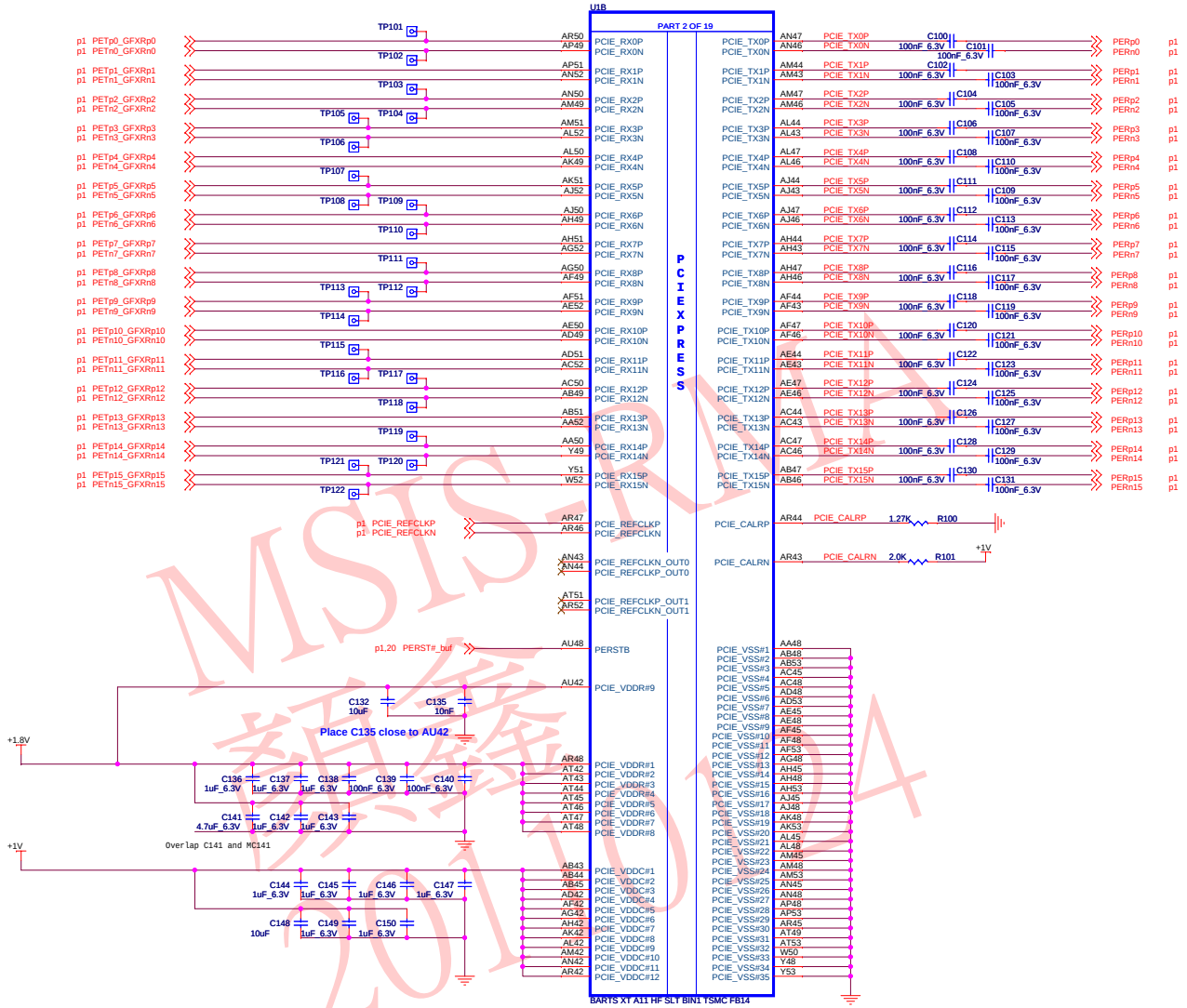
Date:	Friday, October 29, 2010
Rev	53
Sheet	1 of 23
Title	PCIE EDGE CONNECTOR
Doc No.	102-C22201-01

(2) BARTS/ CYPRESS PCIE Interface

NOTE: Some of the PCIE testpoints will be available through vias on traces.



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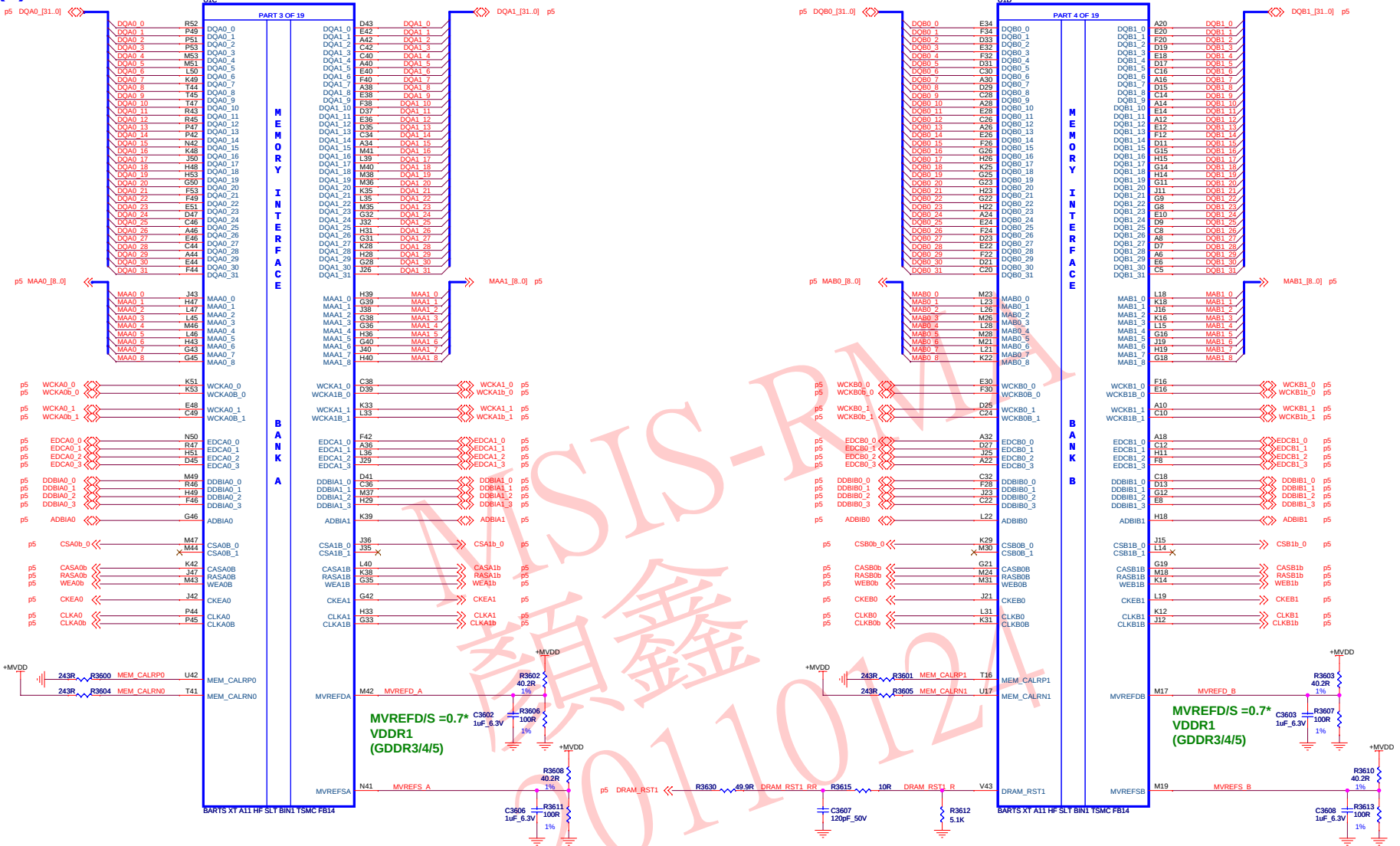
Date:	Friday, October 29, 2010
Rev	53
Sheet	2 of 23
Title	ASIC PCIE Interface
Doc No.	102-C22201-01

(3) BARTS / CYPRESS MEM Interface Ch A&B



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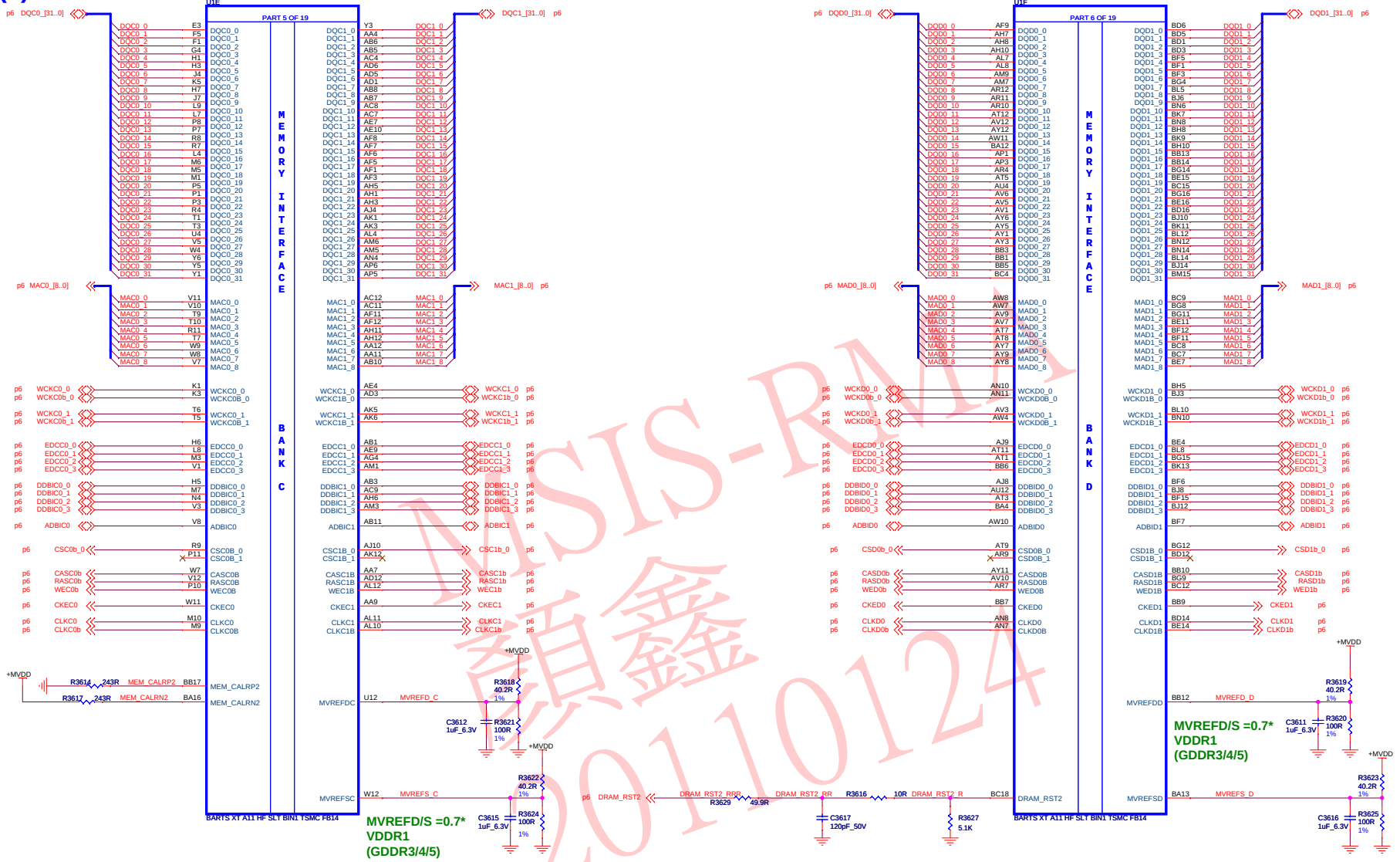
Markham, Ontario

Date:	Friday, October 29, 2010
Rev	53
Sheet	3 of 23
Title	ASIC Memory Ch A & B
Doc No.	102-C22201-01

(4) BARTS / CYPRESS MEM Interface Ch C&D



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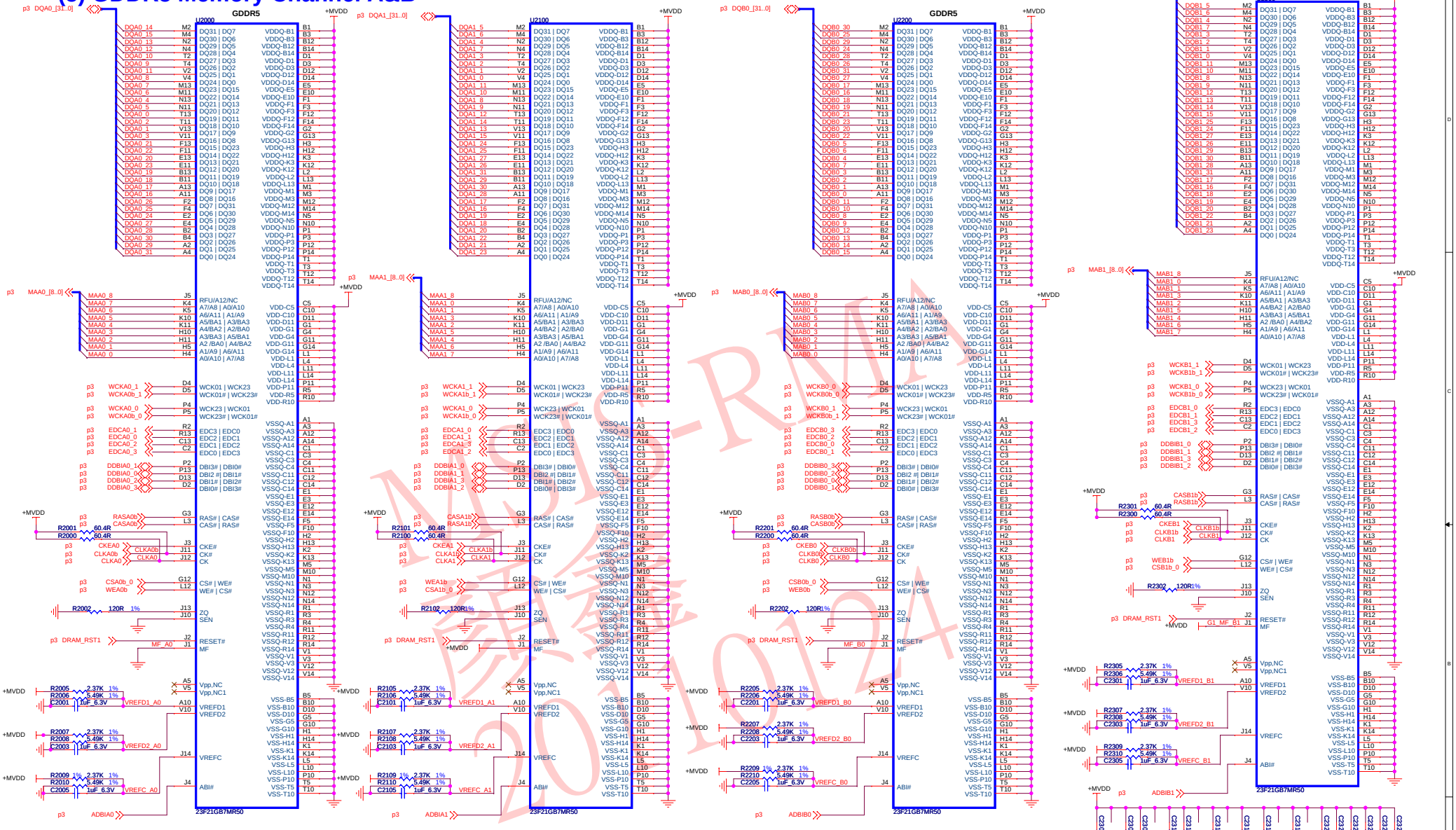
Markham, Ontario

Date:	Friday, October 29, 2010
Rev	53
Sheet	4 of 23
Title	ASIC Memory Ch C & D
Doc No.	102-C22201-01

(5) GDDR5 Memory Channel A&B



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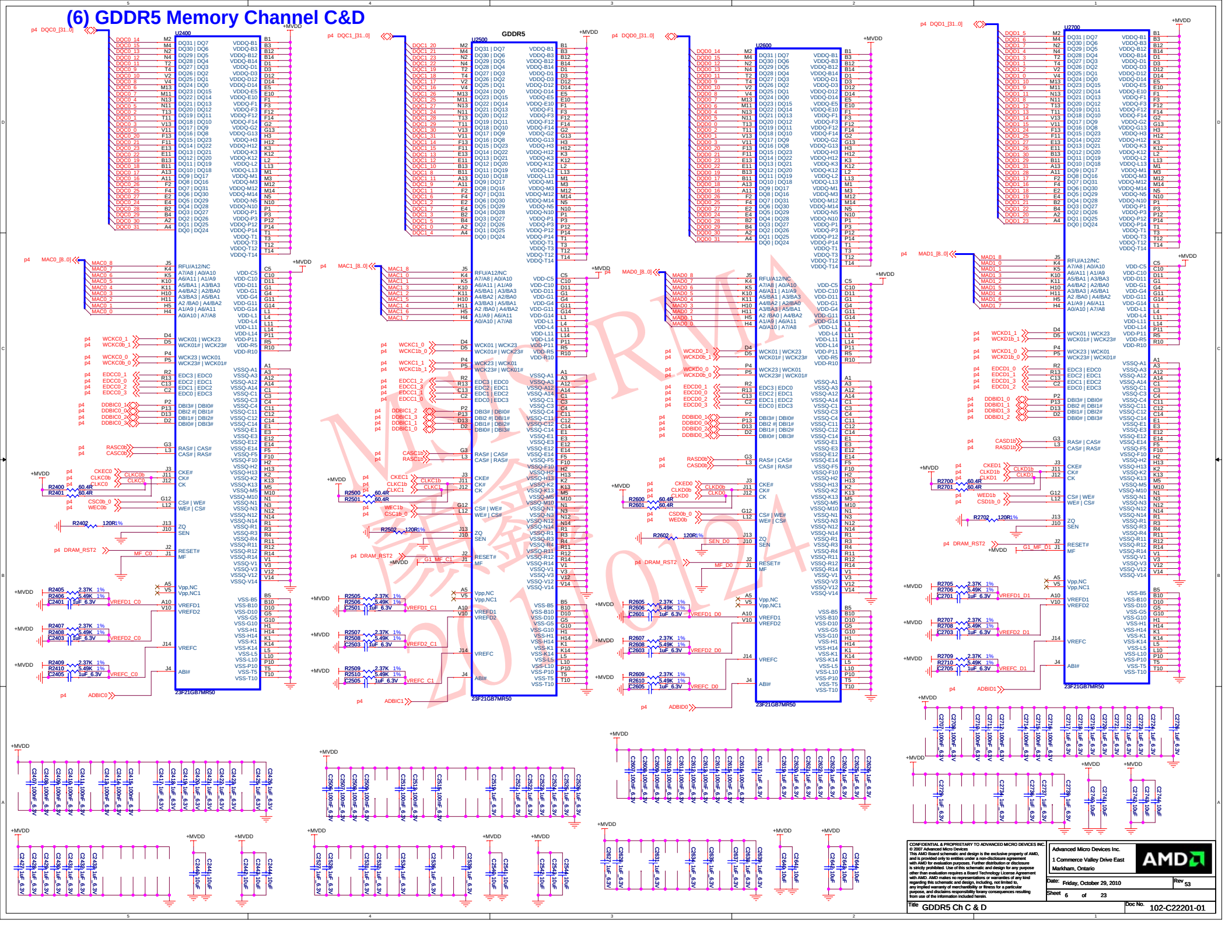
Markham, Ontario

Date:	Friday, October 29, 2010
Rev	53
Sheet	5 of 23
Title	GDDR5 Ch A & B
Doc No.	102-C22201-01

(6) GDDR5 Memory Channel C&D



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Date:	Friday, October 29, 2010
Rev	53
Sheet	6 of 23
Title	GDDR5 Ch C & D
Doc No.	102-C22201-01

(07) BARTS / Cypress GPIOs Strap CF XTAL OSC

PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

SCL / SDA BUS:

I2C Address	Function	Device
0x60	Chil VDDC REG	

DDC6 BUS:

I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

PWRGOOD must be connected to GND for normal operation

PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO(13,12,11) - CONFIG[2..0]

CONFIG[2]	100 - 512Kbit	M25P05A	(ST)
	101 - 1Mbit	M25P10A	(ST)
CONFIG[1]	101 - 2Mbit	M25P20	(ST)
	101 - 4Mbit	M25P40	(ST)
CONFIG[0]	101 - 8Mbit	M25P80	(ST)
	100 - 512Kbit	Pm25LV512	(Chingis)
	101 - 1Mbit	Pm25LV010	(Chingis)

RESERVED:
Internal use only. Other logic must not affect these signals during RESET.

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

RESERVED:
STRAP_BIOS_ROM_EN
CLKREQ# that requires open drain connection, and cannot be used as pinstrap
Don't set high at reset

CrossFire Card-Edge

Lower Cable Card Edge

Place the crossfire testpoints near the ASIC and not the connector

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

Keep XIN_OSC and XOUT_OSC as short as possible to minimize stray capacitance

Share pad R26 and R19

Divider for 1.8V signaling.

Route 50ohms single-ended/100ohms diff and keep short

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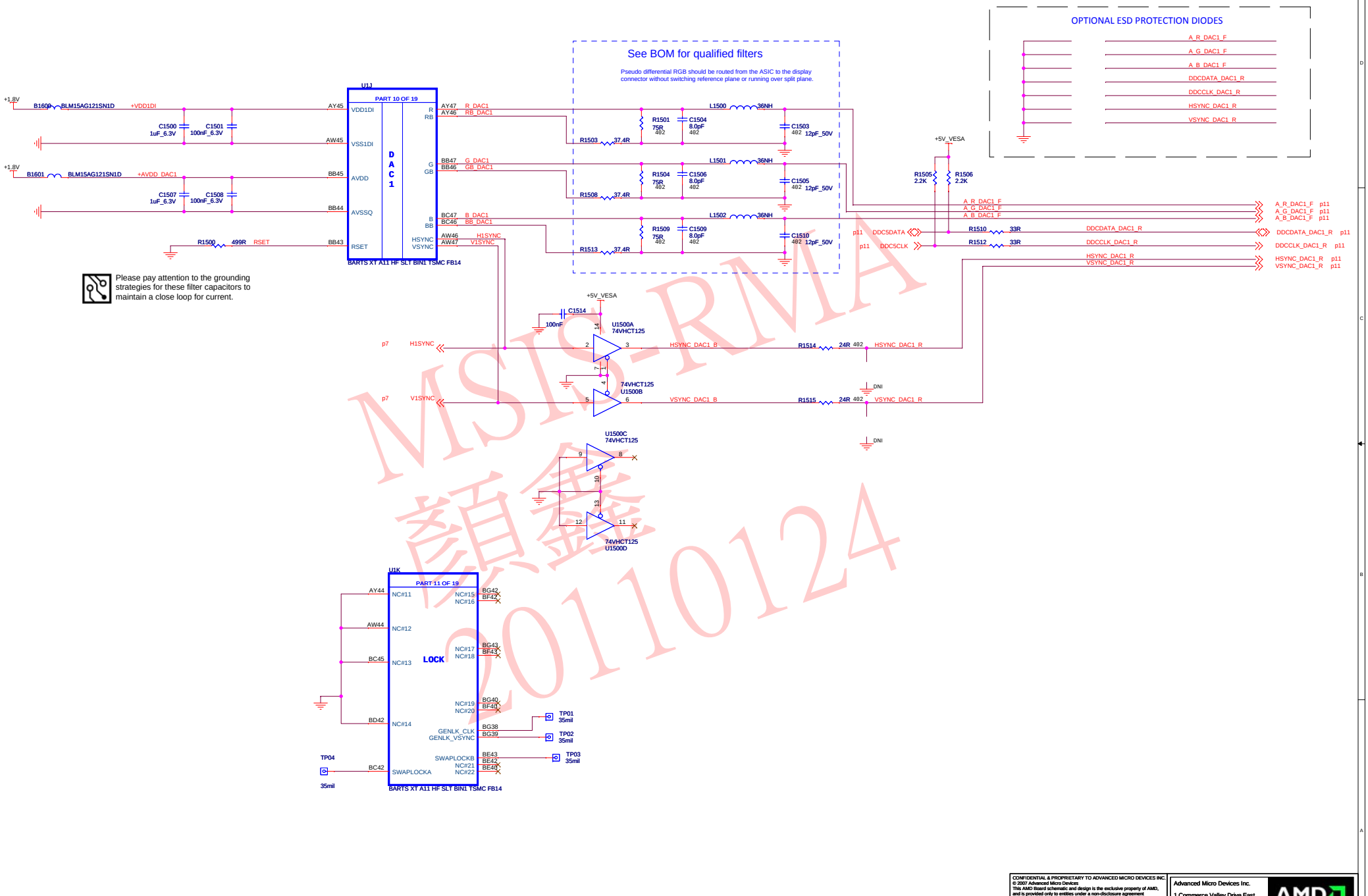
Date:	Friday, October 29, 2010
Rev	53
Sheet	7 of 23
Title	ASIC GPIO, STRAPS,CF, and XTAL
Doc No.	102-C22201-01

(08) BARTS / CYPRESS DAC1



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Friday, October 29, 2010
Rev	53
Sheet	8 of 23
Title	Power Management
Doc No.	102-C22201-01

(09) BARTS / CYPRESS TMDS A&B

HDMI/DVI MUX:
0.1uF cap to be used, placed close to VDD power pins
Place 1x to top and 1x to bottom of the package
Use 5 ground vias for the ground pad: 1 via at each corner of the ground pad and 1 in the center of the ground pad
TDFN package to be used: 2600009800G
SEL is 1.8V only

Disp. Out	DVI	HDMI
SEL	0	1

PLEASE NOTE +5V NEEDS TO HAVE A SEPARATE REGULATOR FOR HDMI!

OVERLAP HDMI WITH DP

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

U1L
PART 12 OF 19
TMDP A/B
BARTS XT A11 HF SLT BIN1 TSMC FB14

PI3HDMI412FT-BZHE
U1700

J2501
HDMI

J1700B
STACKED_DVI

Optional ESD protection dioes

TOP

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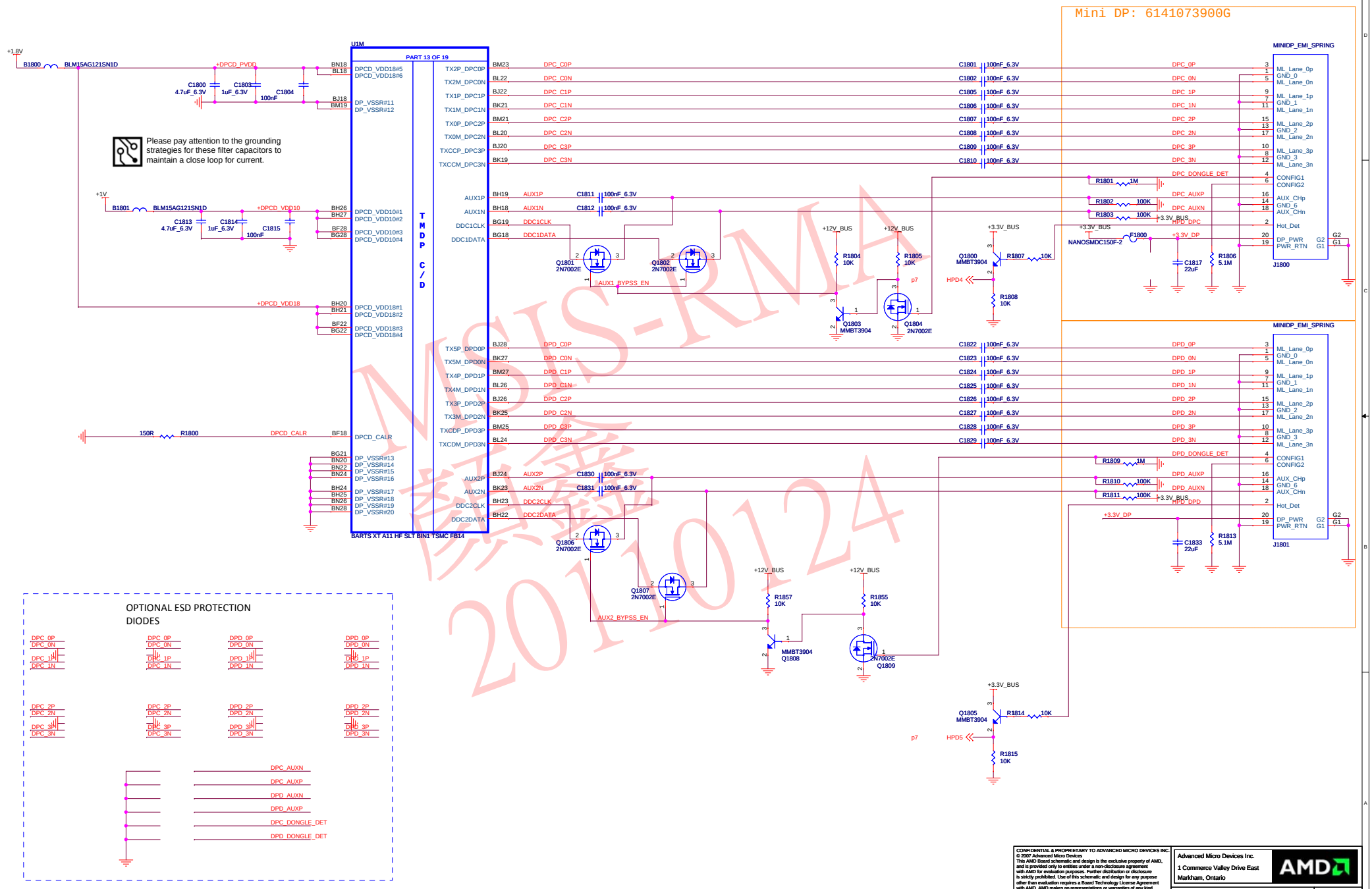
Date: Friday, October 29, 2010
Rev 53
Sheet 9 of 23
Title ASIC TMDS AB
Doc No. 102-C22201-01

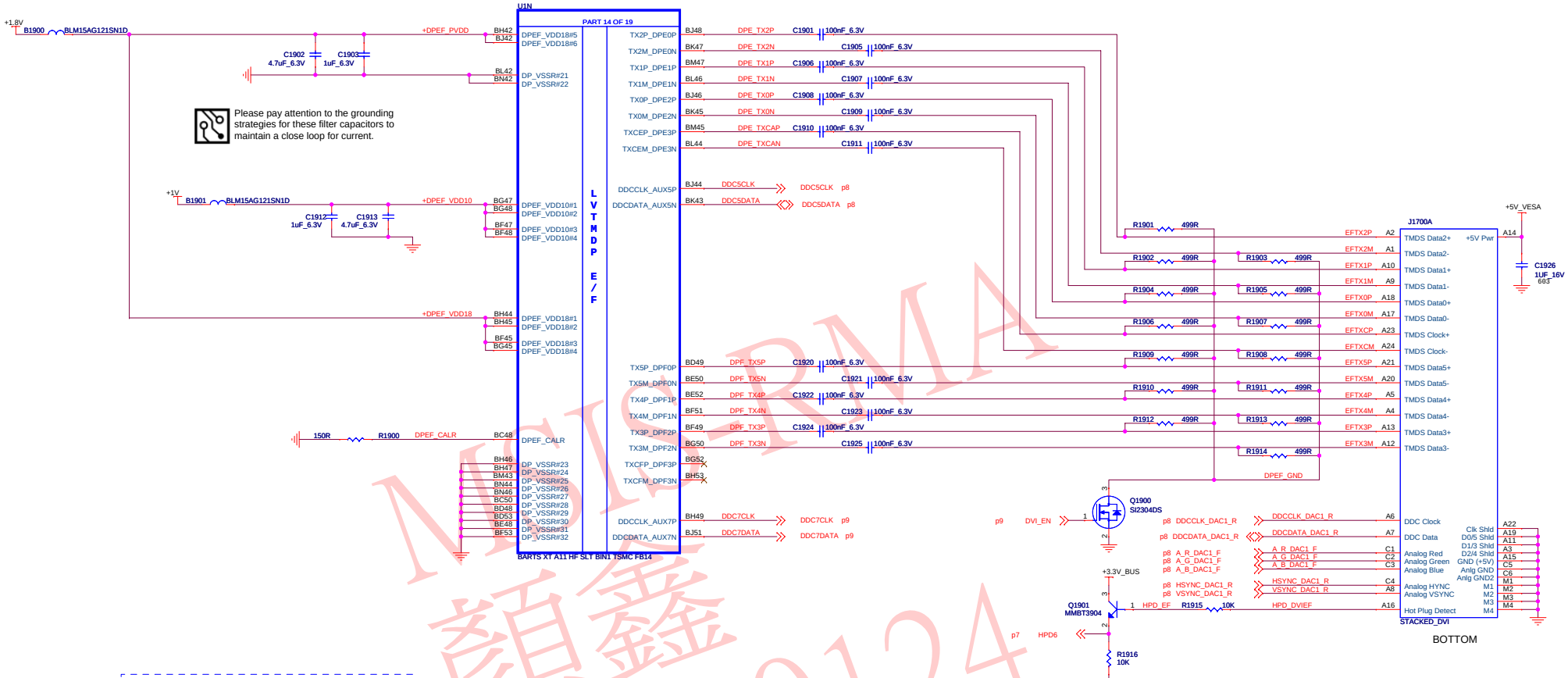
(10) BARTS / CYPRESS Display Port/HDMI C&D



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Friday, October 29, 2010
Rev	53
Sheet	10 of 23
Title	ASIC DP C,D
Doc No.	102-C22201-01

(11) BARTS / CYPRESS LVTMDP E&F



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
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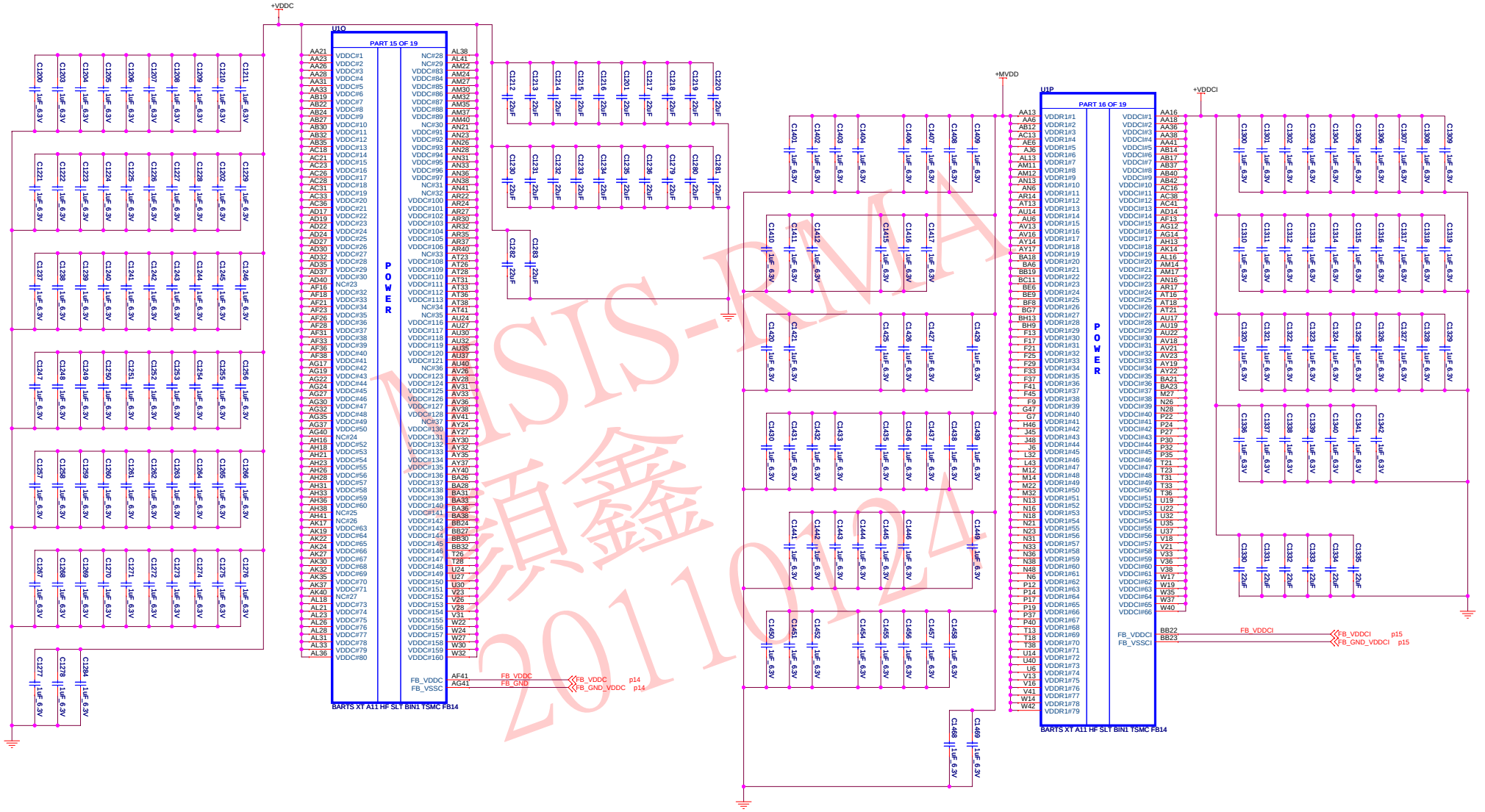
Date:	Friday, October 29, 2010
Rev	53
Sheet	11 of 23
Title	ASIC TMDS EF
Doc No.	102-C22201-01

(12) BARTS / CYPRESS Power



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1 Commerce Valley Drive East
Markham, Ontario

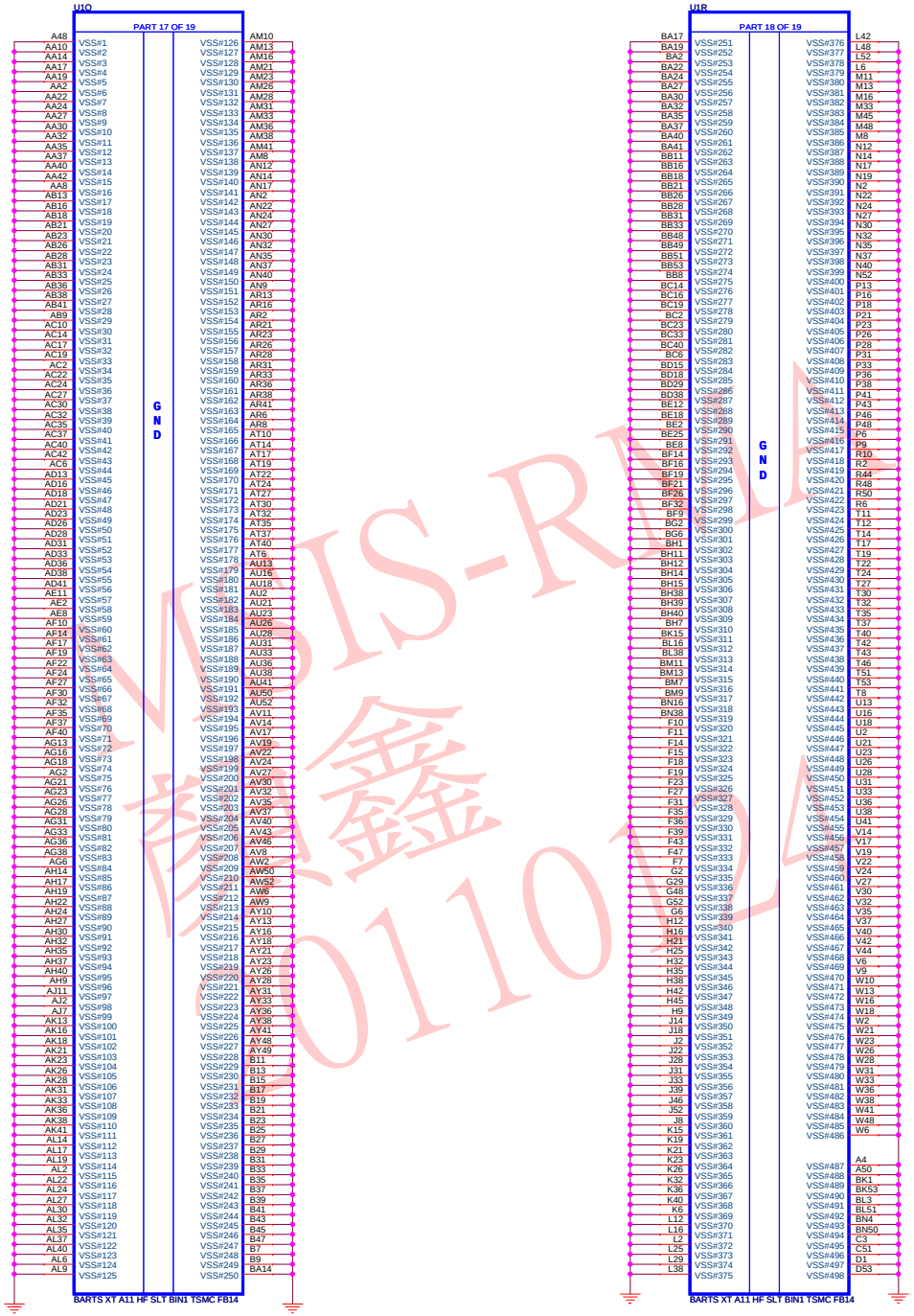
Date: Friday, October 29, 2010 Rev 53

Sheet 12 of 23

Title ASIC POWER

Doc No. 102-C22201-01

(13) BARTS / CYPRESS GND



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1 Commerce Valley Drive East
Markham, Ontario

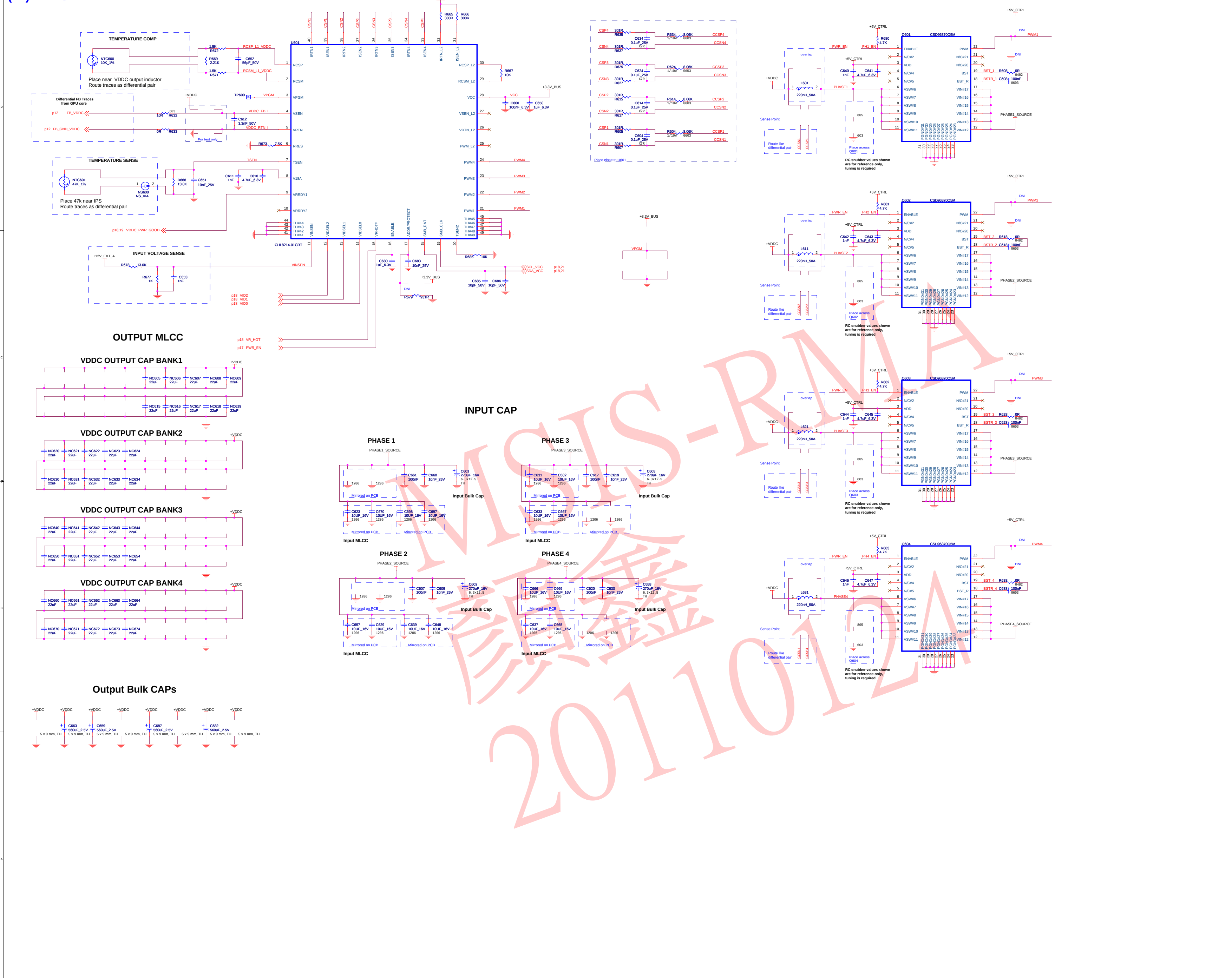
Date: Friday, October 29, 2010 Rev 53

Sheet 13 of 23

Title ASIC GND

Doc No. 102-C22201-01

(14) VDDC



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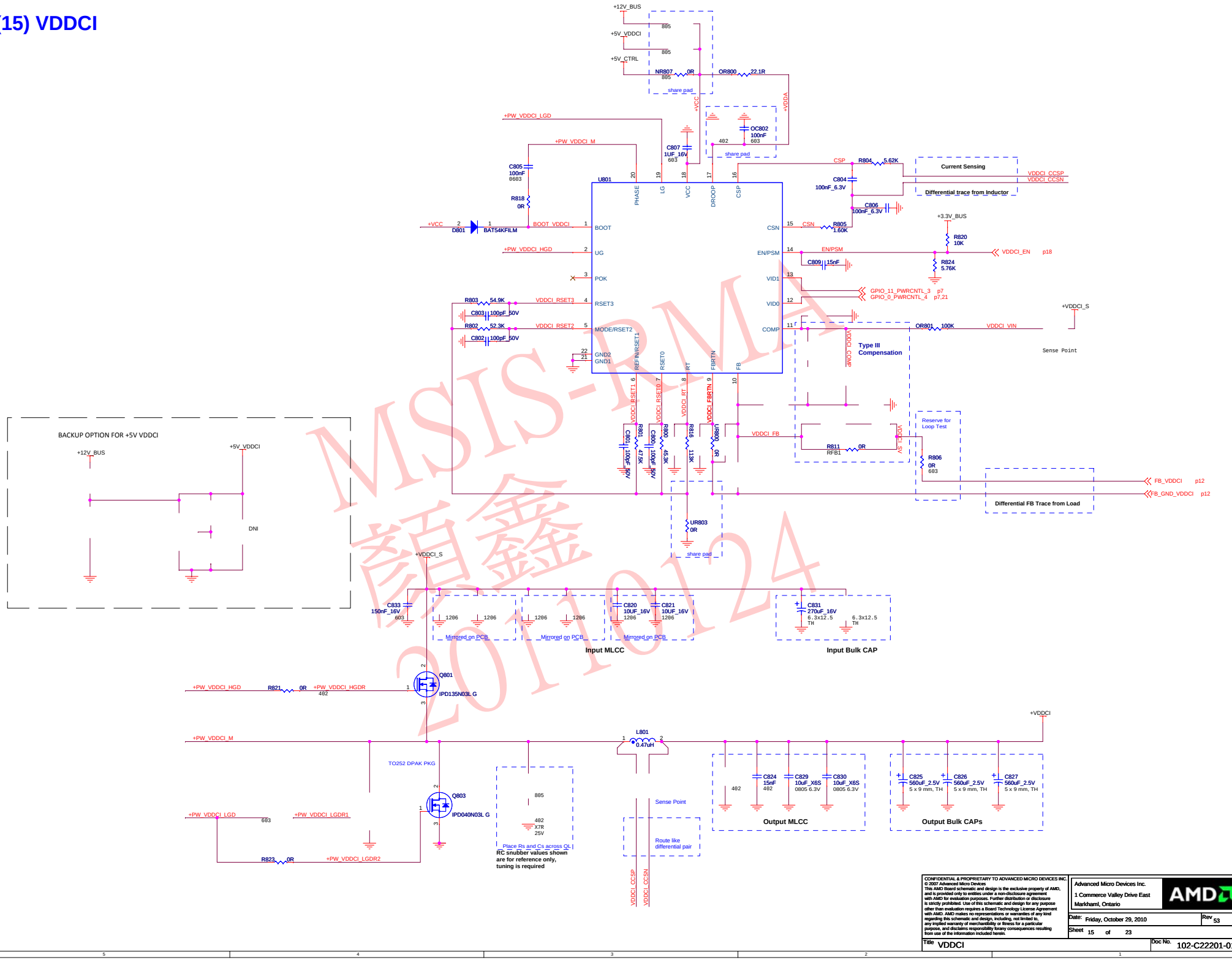
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, October 29, 2010
Sheet 14 of 23
Title: VDDC
Doc No. 102-C22201-01

(15) VDDCI



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
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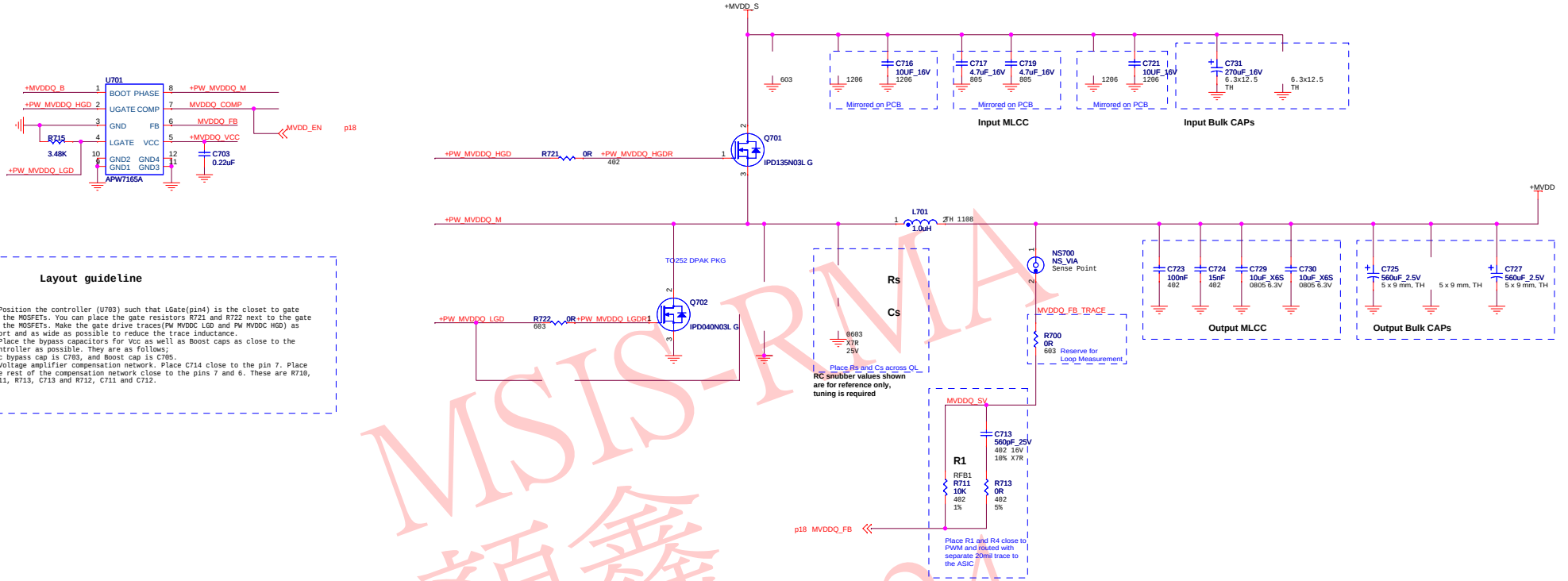
Date:	Friday, October 29, 2010
Rev	53
Sheet	15 of 23
Title	VDDCI
Doc No.	102-C22201-01

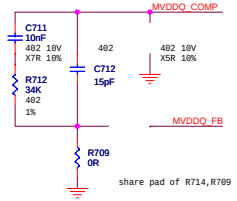
(16) MVDD



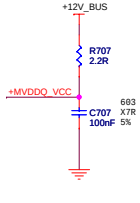
Layout guideline

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

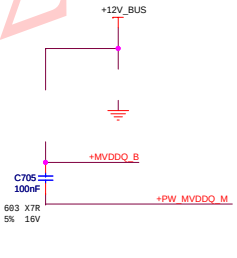
COMPENSATION CIRCUIT



FILTERED SMPS VCC



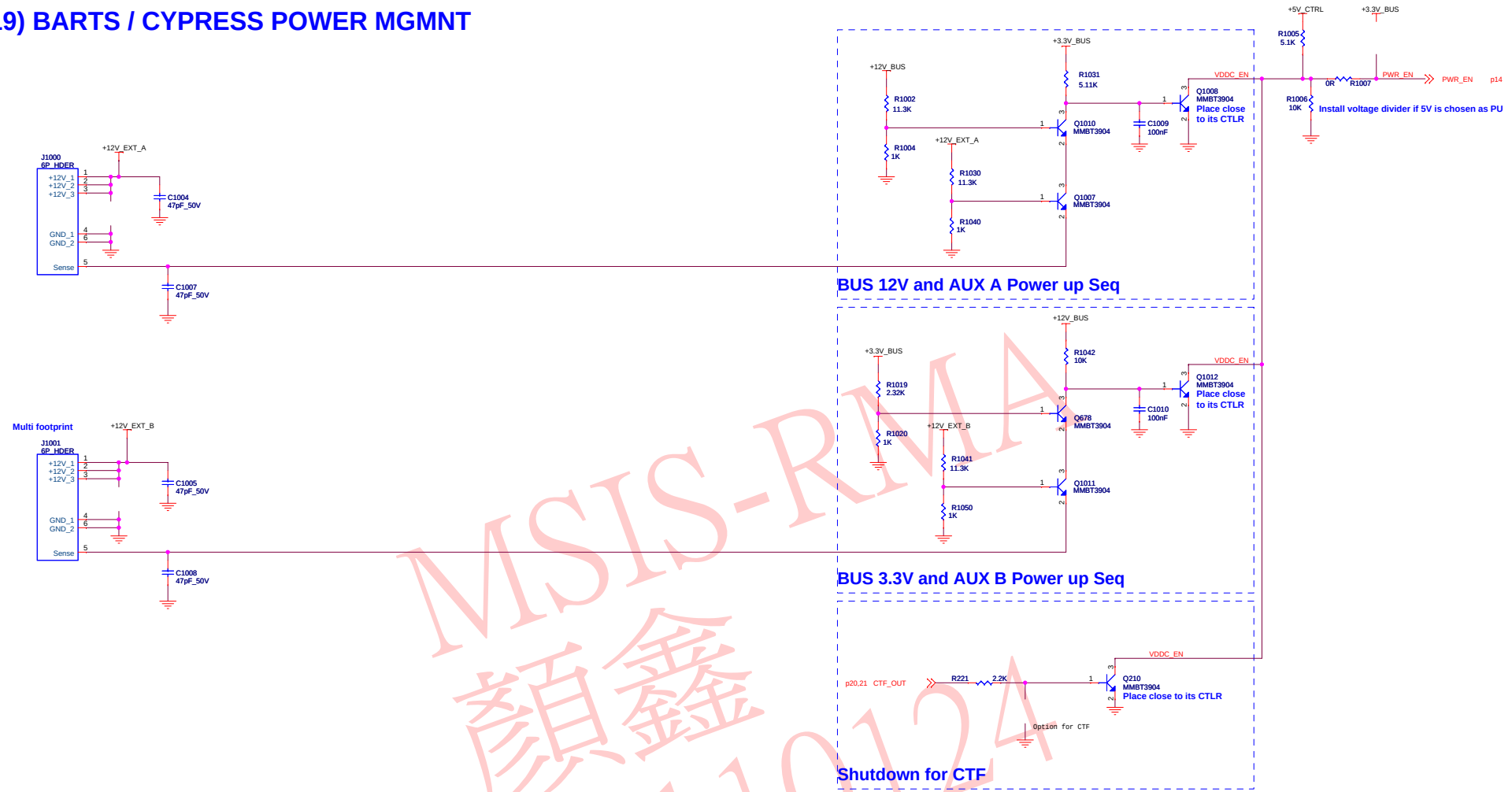
BOOT CIRCUIT



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Friday, October 29, 2010
Rev	53
Sheet	16 of 23
Title	MVDD
Doc No.	102-C22201-01

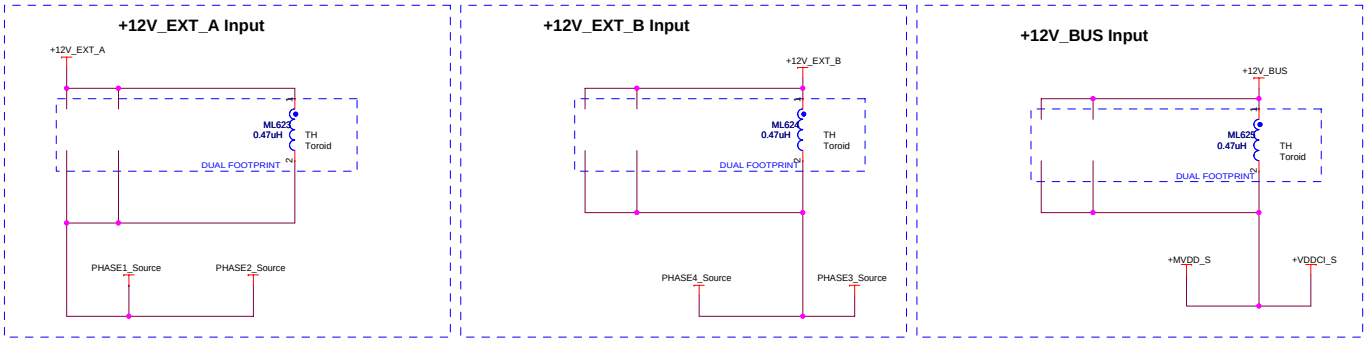
(19) BARTS / CYPRESS POWER MGMNT

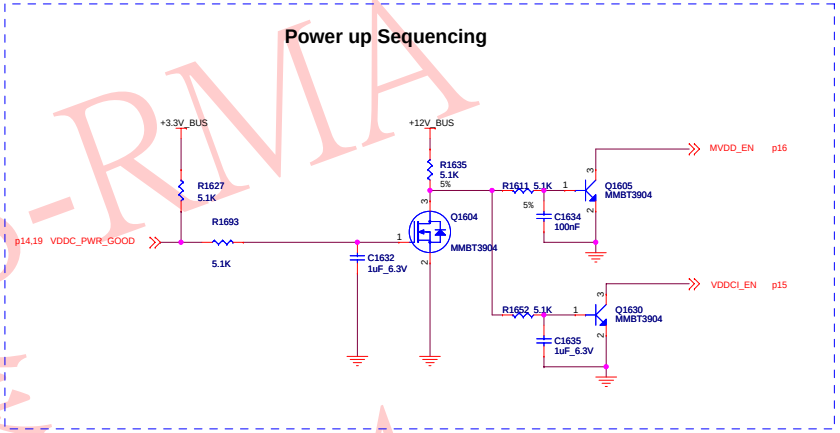


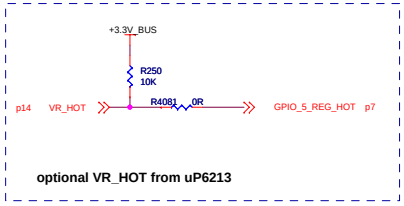
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

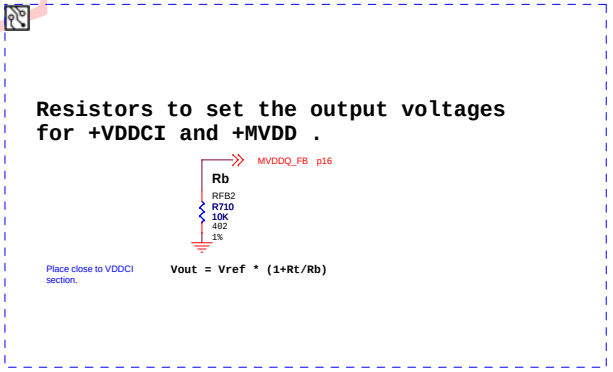
Date: Friday, October 29, 2010	Rev 53
Sheet 17 of 23	
Title Power Management	Doc No. 102-C22201-01

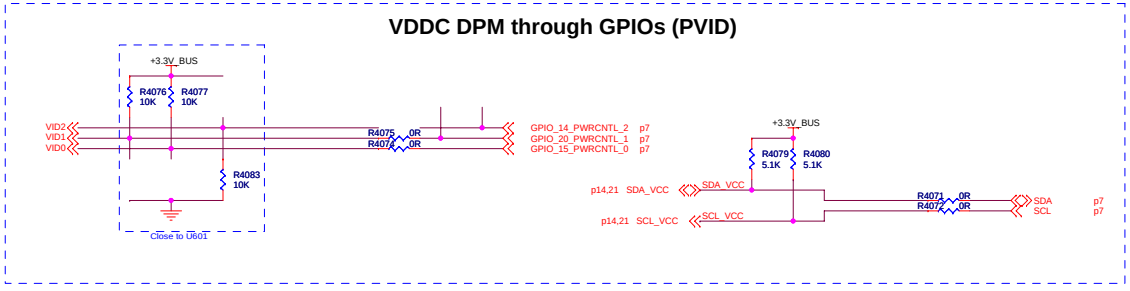
(17) BARTS / CYPRESS VDDCI POWER PLAY









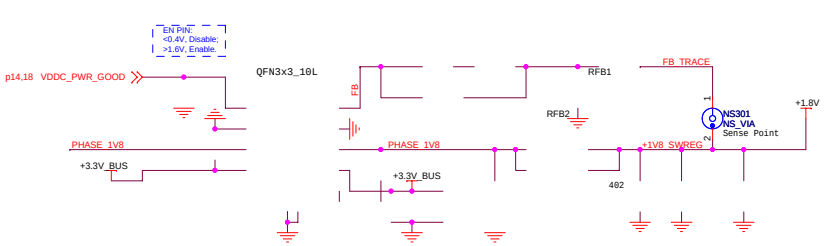


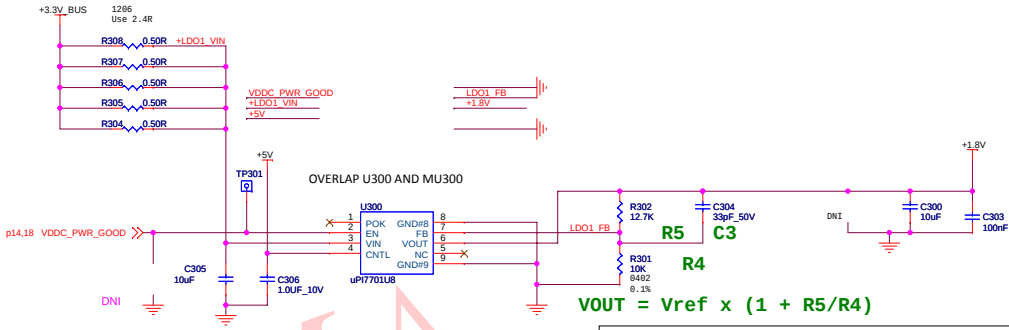
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Friday, October 29, 2010	Rev 53
Sheet 18 of 23	
Title Power Management 2	Doc No. 102-C22201-01

(18) BARTS / CYPRESS Small Rail Regulators

LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

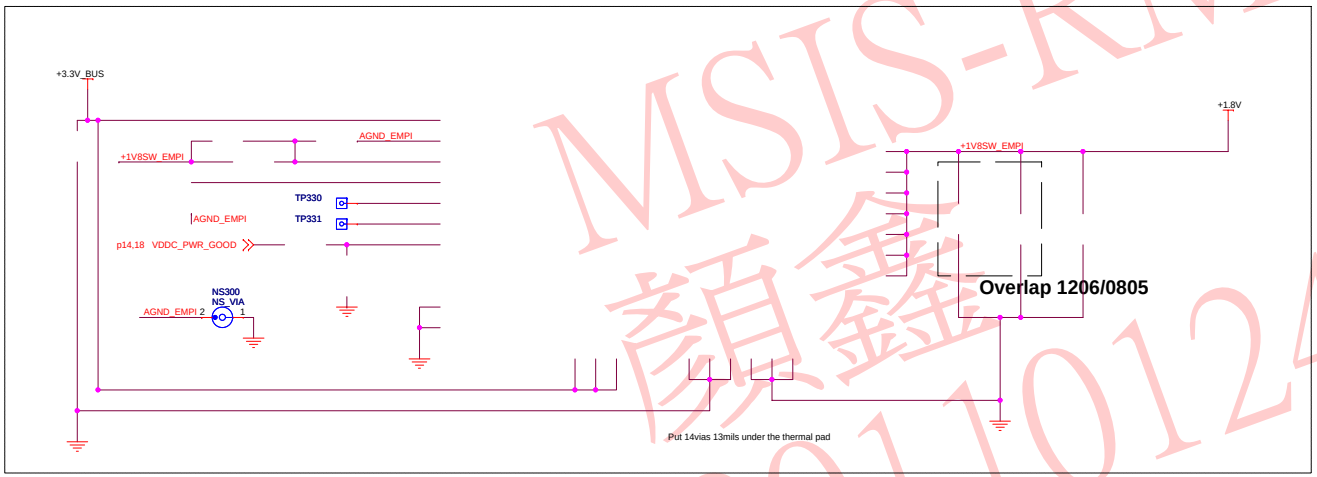


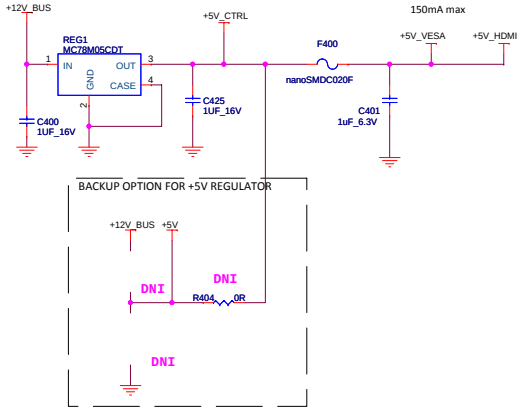


VOUT = Vref x (1 + R5/R4)

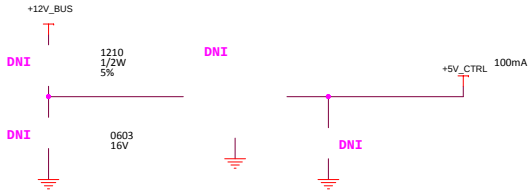
Regulators for +5V, +5V_VESA and +5V_HDMI
Iout max = 150mA (DVI+HDMI)

Other cheaper solution at 5MHz switching for 1.8V



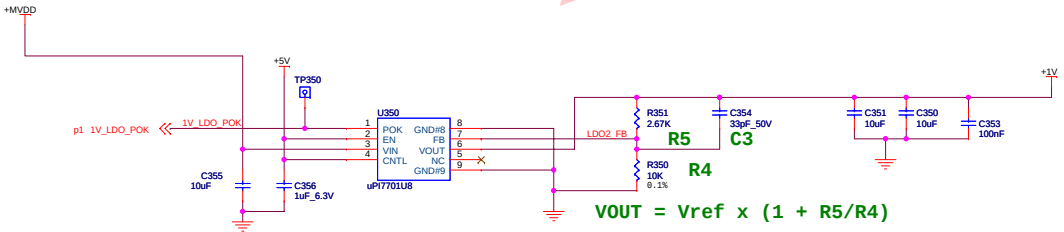


optional 5V power for VDDC regulator;



LDO #2: Vin = +1.35V to 1.8VMAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

OVERLAP ALTERNATE CAP FOOTPRINTS

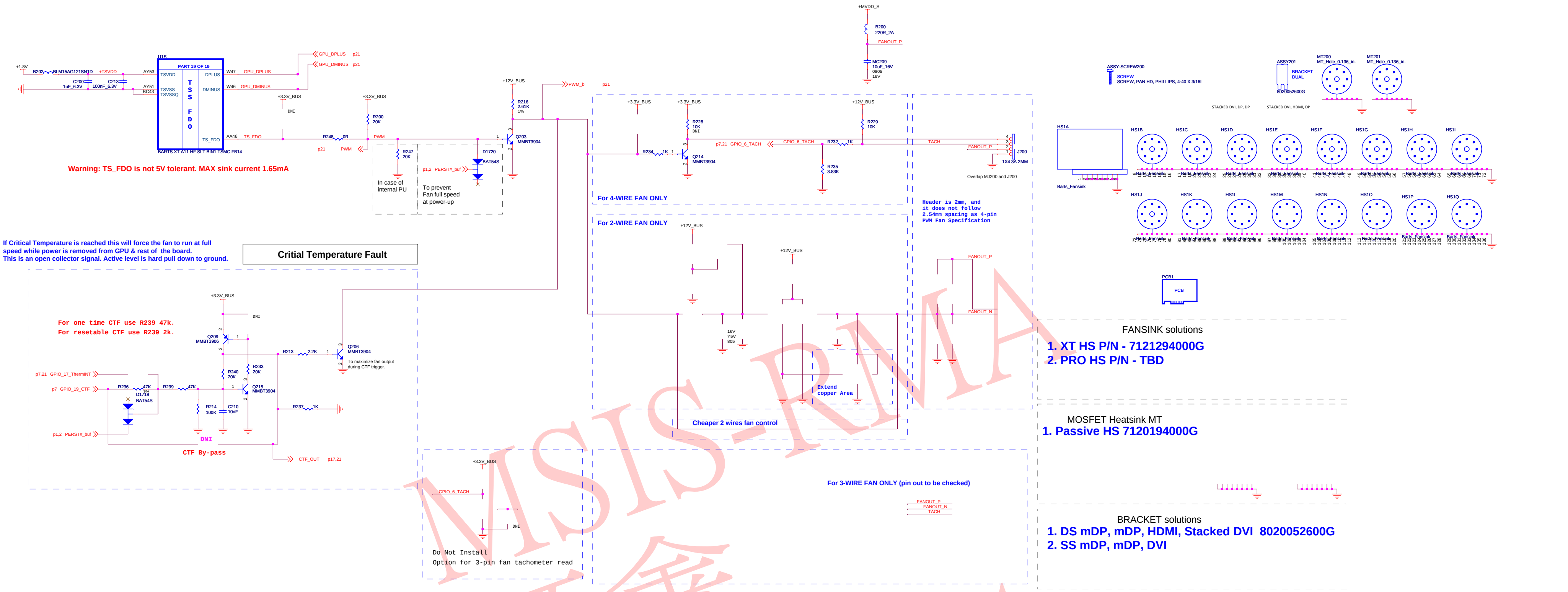


VOUT = Vref x (1 + R5/R4)

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Friday, October 29, 2010
Rev	53
Sheet	19 of 23
Title	Small Rail Regulators
Doc No.	102-C22201-01

(20) BARTS / CYPRESS Mechanical and Thermal Management



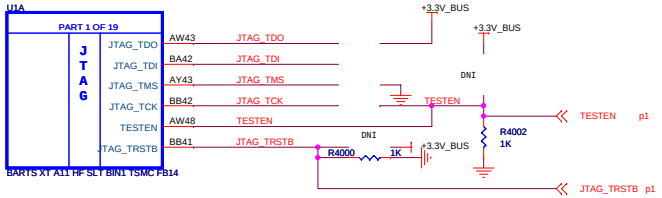
FANSINK solutions
1. XT HS P/N - 7121294000G
2. PRO HS P/N - TBD

MOSFET Heatsink MT
1. Passive HS 7120194000G

BRACKET solutions
1. DS mDP, mDP, HDMI, Stacked DVI 8020052600G
2. SS mDP, mDP, DVI

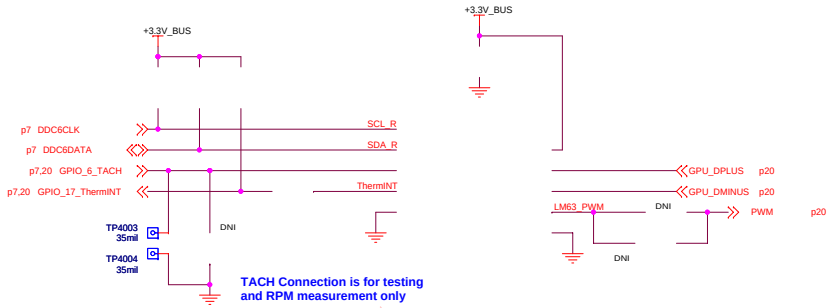
(21) CYPRESS Debug Circuits

JTAG



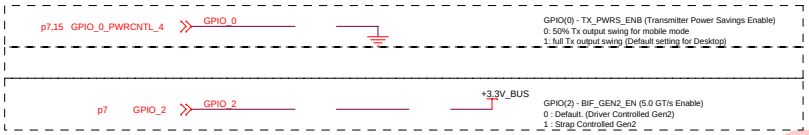
For ALL bringup boards DNI R4000 and stuff R4003 otherwise the TAPC will be struck in Test-Logic-Reset and be useless since TRSTB is not on the connector.

LM96163 FOR BACKUP THERMAL CONTROL



TACH Connection is for testing and RPM measurement only

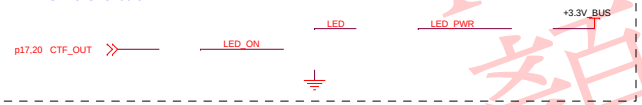
SWITCH CONNECTIONS TO PINSTRAPS



Bypass Switch (not for production)

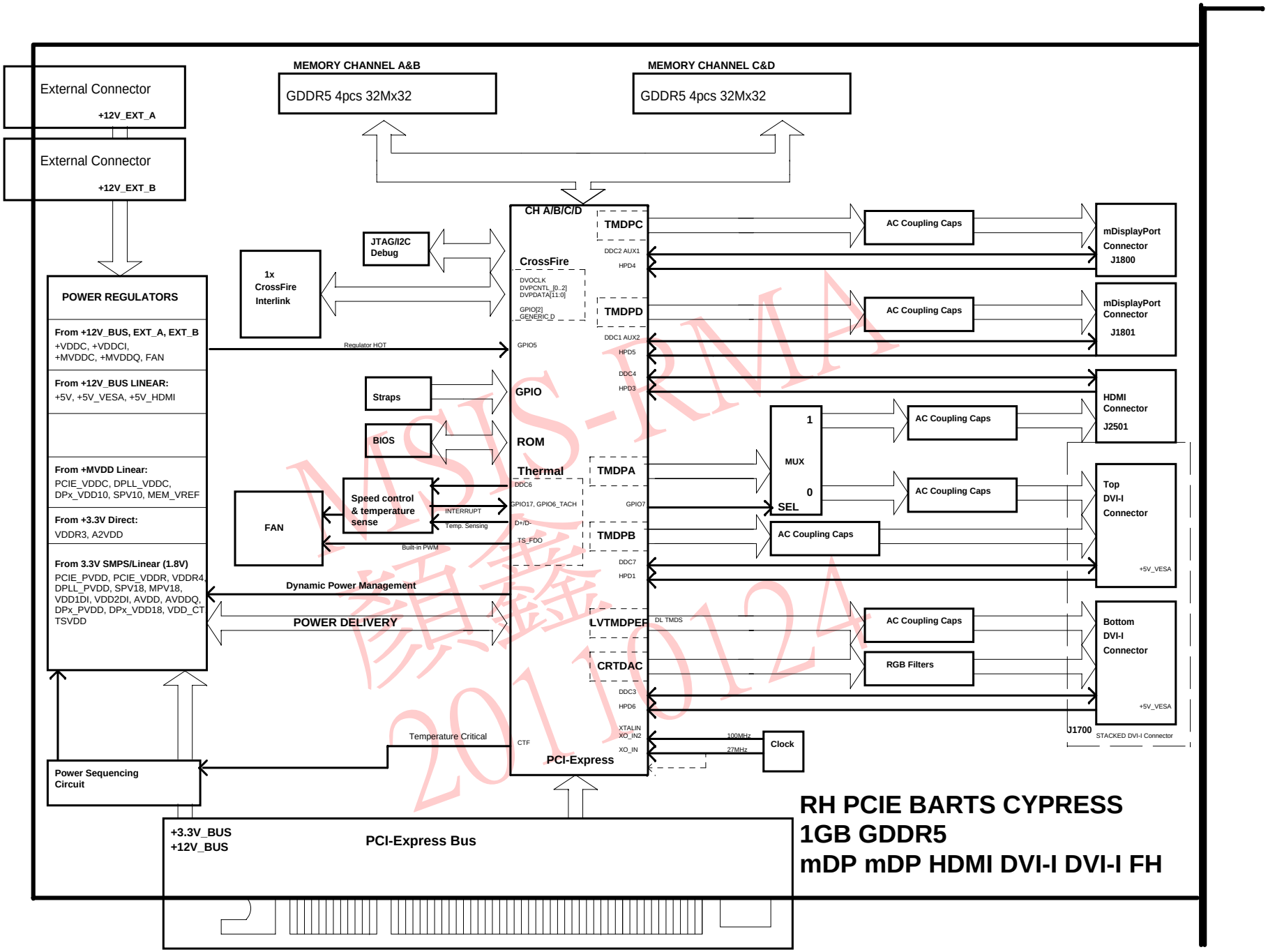
DNI For Production

LED RED "ON" shows Fault



To ACCESS the VDDC CONTROLLER through I2C

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario
Date: Friday, October 29, 2010
Rev 53
Sheet 21 of 23
Title Debug Circuits
Doc No. 102-C22201-01



RH PCIE BARTS CYPRESS
1GB GDDR5
mDP mDP HDMI DVI-I DVI-I FH

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Canada, L3T 7X6 (905) 882-2600

Date:	Friday, October 29, 2010
Rev	53
Sheet	22 of 23
Title	Block Diagram
Doc No.	102-C22201-01

Title	Schematic No.	Date:
RH BARTS CYPRESS GDDR5 mDP-mDP-HDMI-DVII-DVII	102-C22201-01	Friday, October 29, 2010

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 53

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	19/04/2010	Initial release. Based on C220
1	00B	09/08/2010	Page01: Added direct connection from Pull-Up for MU101 for Cypress Page09: remove the inductor for top DVI line Page14: update Q601,Q602,Q603,Q604 symbol Page17: add C211 Page20: add R201, R237, R241. Page18: add optional 3-pin fan tach circuitry; Page50: update block diagram