P360-A00 Base Design

P360-A00, G92, 16Mx32 GDDR3 (900MHz),TV(OPTION)
DVI-I-DL, DVI-I-DL

Table of Contents:

V186-1.0 Base on P360

1.PAGE11: ADD VGA display connector
2.PAGE12: Move IFP C/D HMDI to page 13
3.PAGE13: Unused DACB Interface, ADD IFP C/D HMDI interface
4.PAGE15: Use I2CC for HDMI control, add GPIO10/14 for HDMI control
5.PAGE18:Add FM1~FM6

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10360-base-000	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0050	600-10360-0050-000	P360 G92-287 512MB GDDR3 16Mx32 DVI-I+DVI-I
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview

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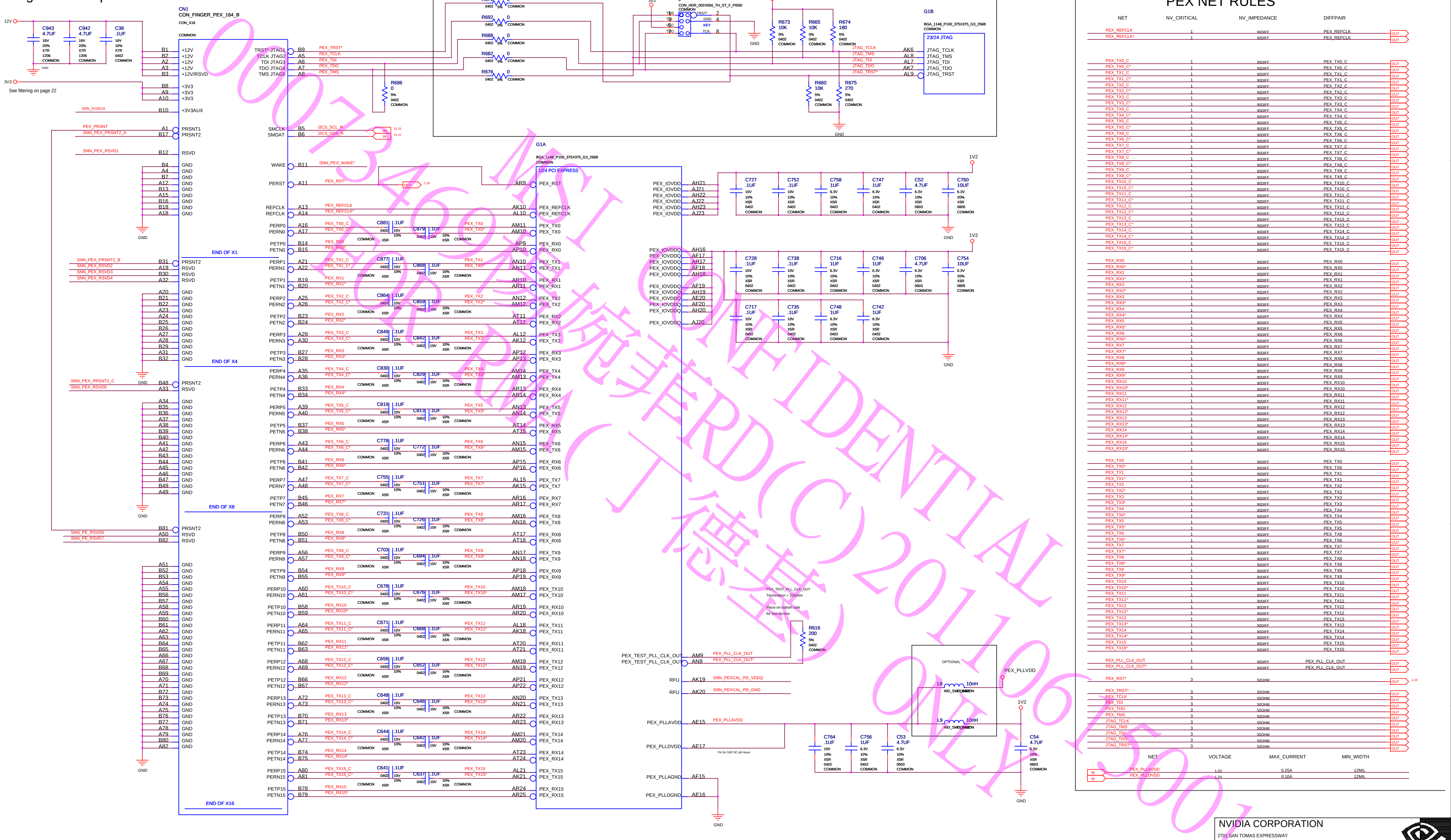
Page2: PCI Express 1.0



ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express 1.0

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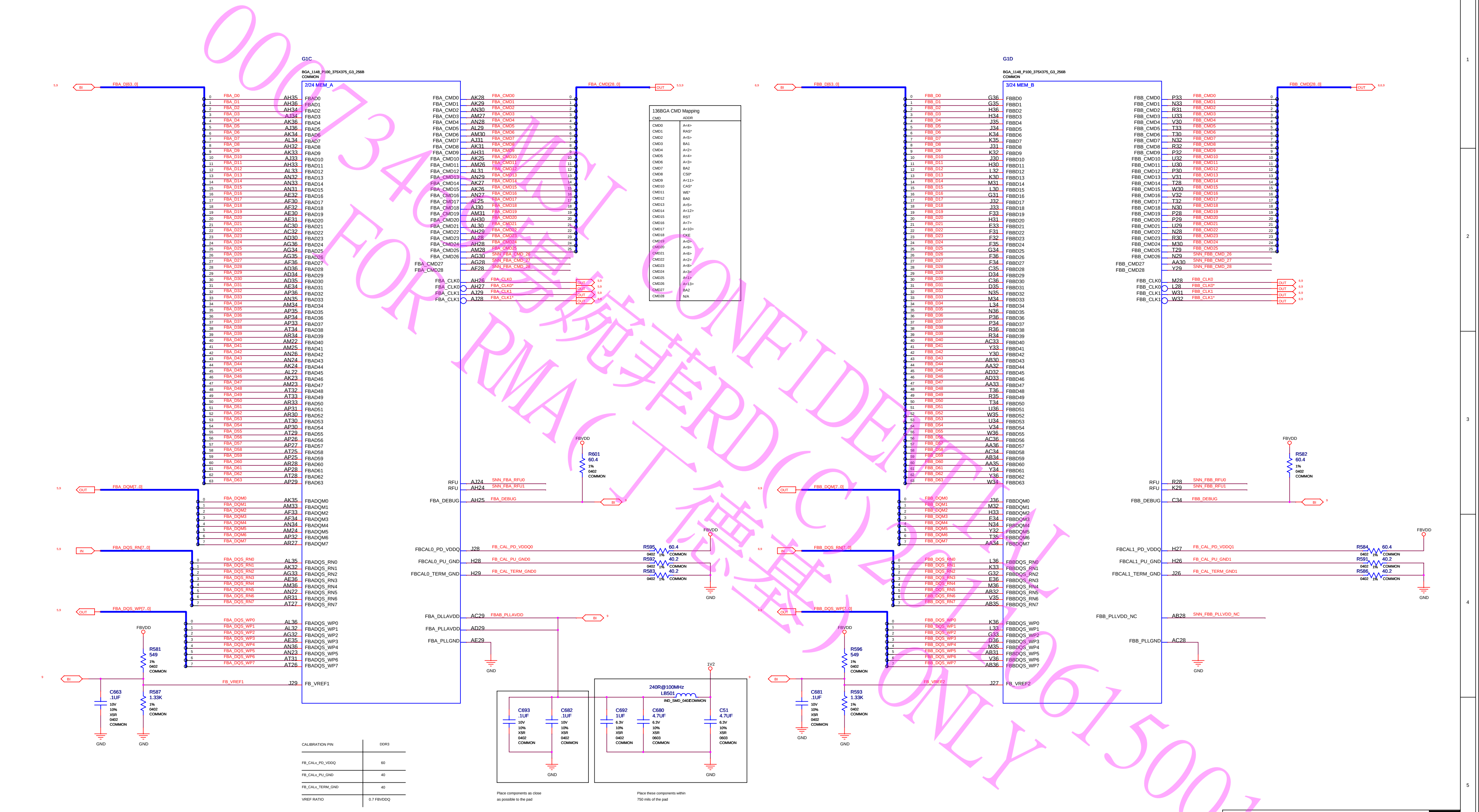
Page3: MEMORY: GPU Partition A/B



ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: GPU Partition A/B

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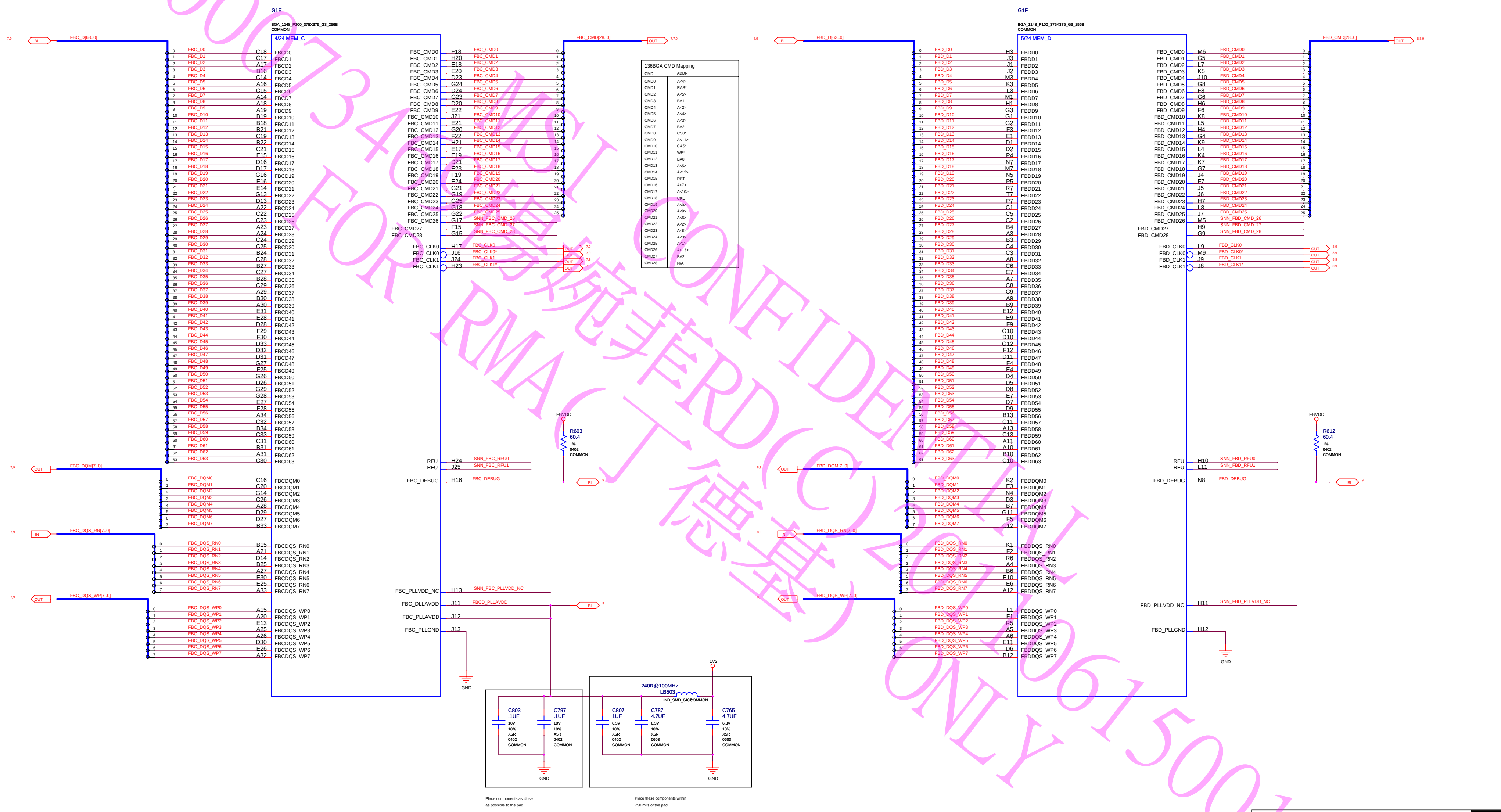
Page4: MEMORY: GPU Partition C/D



Place components as close as possible to the pad

Place these components within 750 mils of the pad

ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: GPU Partition C/D

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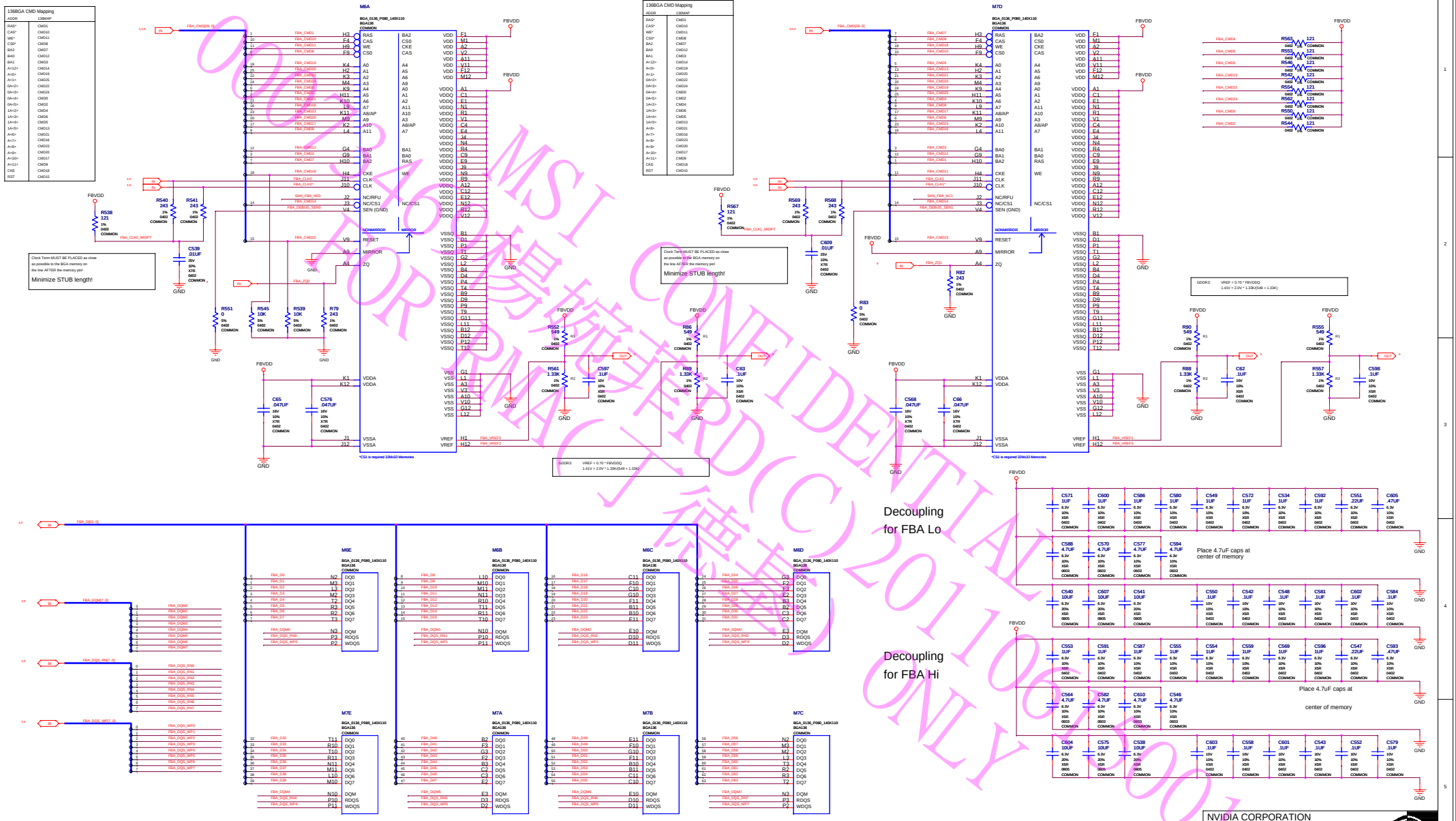
Page5: FBA Partition



ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA Partition

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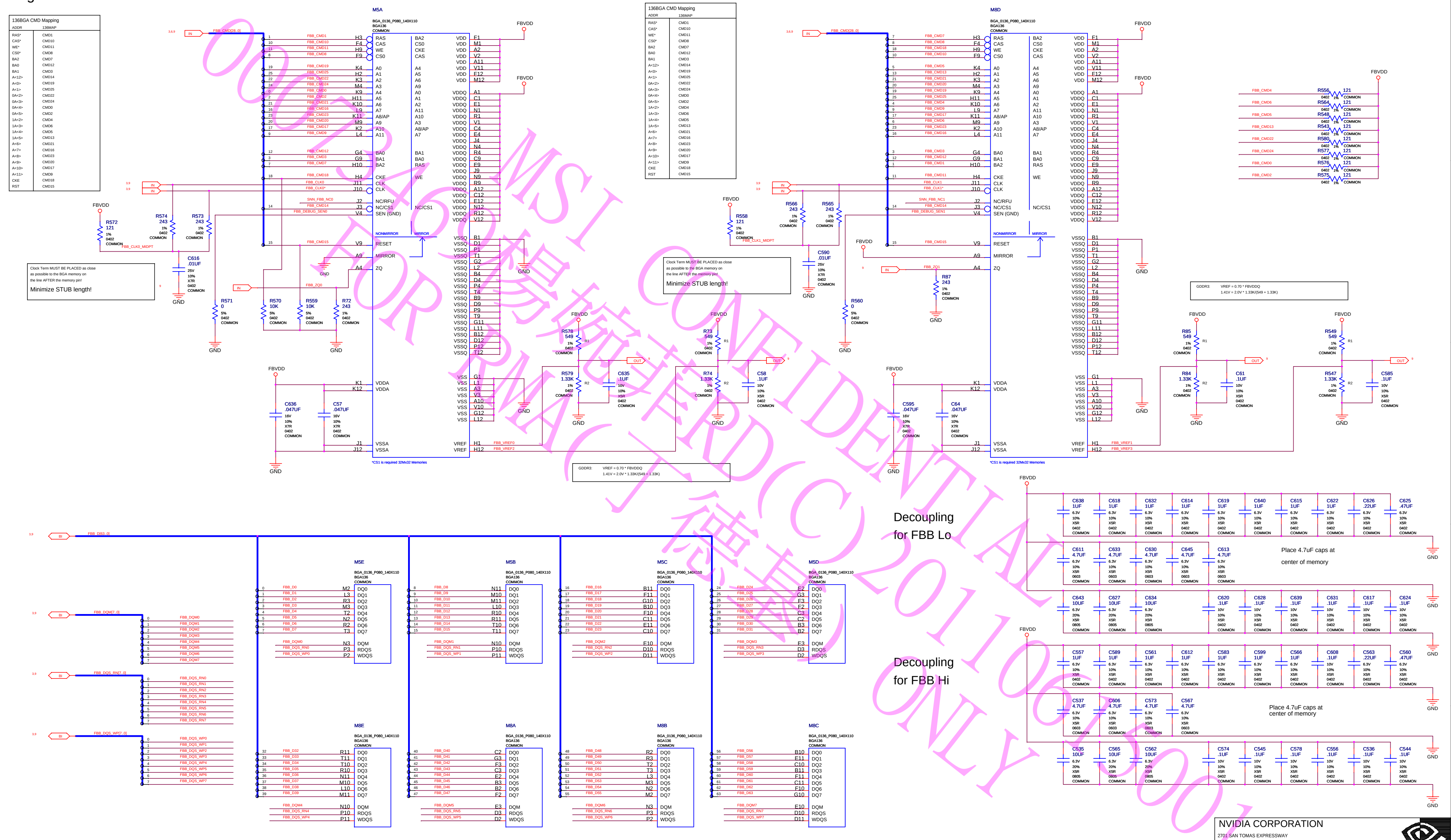
Page6: FBB Partition



136BGA CMD Mapping	
ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

136BGA CMD Mapping	
ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBB Partition

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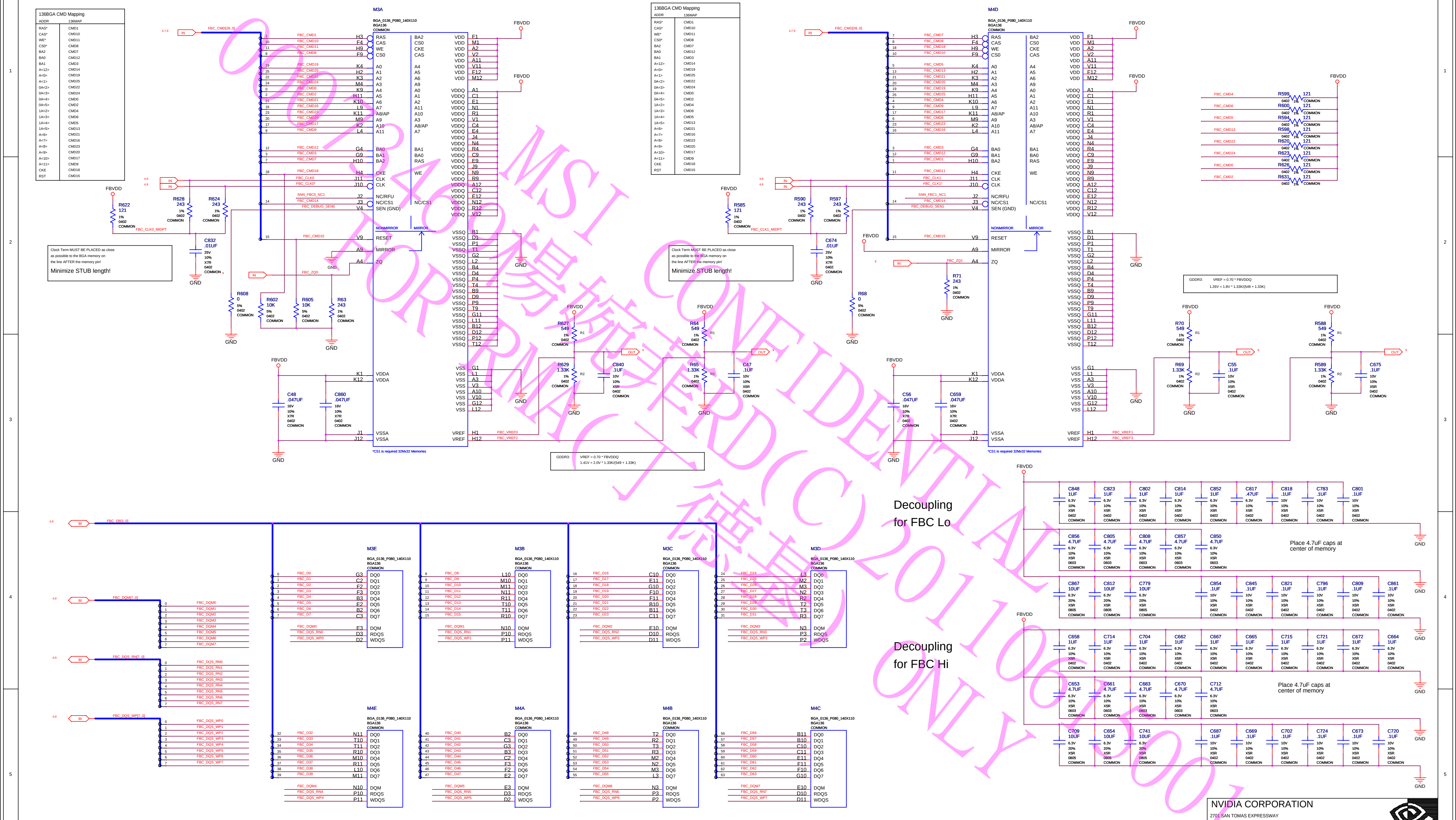
Page7: FBC Partition



ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC Partition

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Page8: FBD Partition

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
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1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
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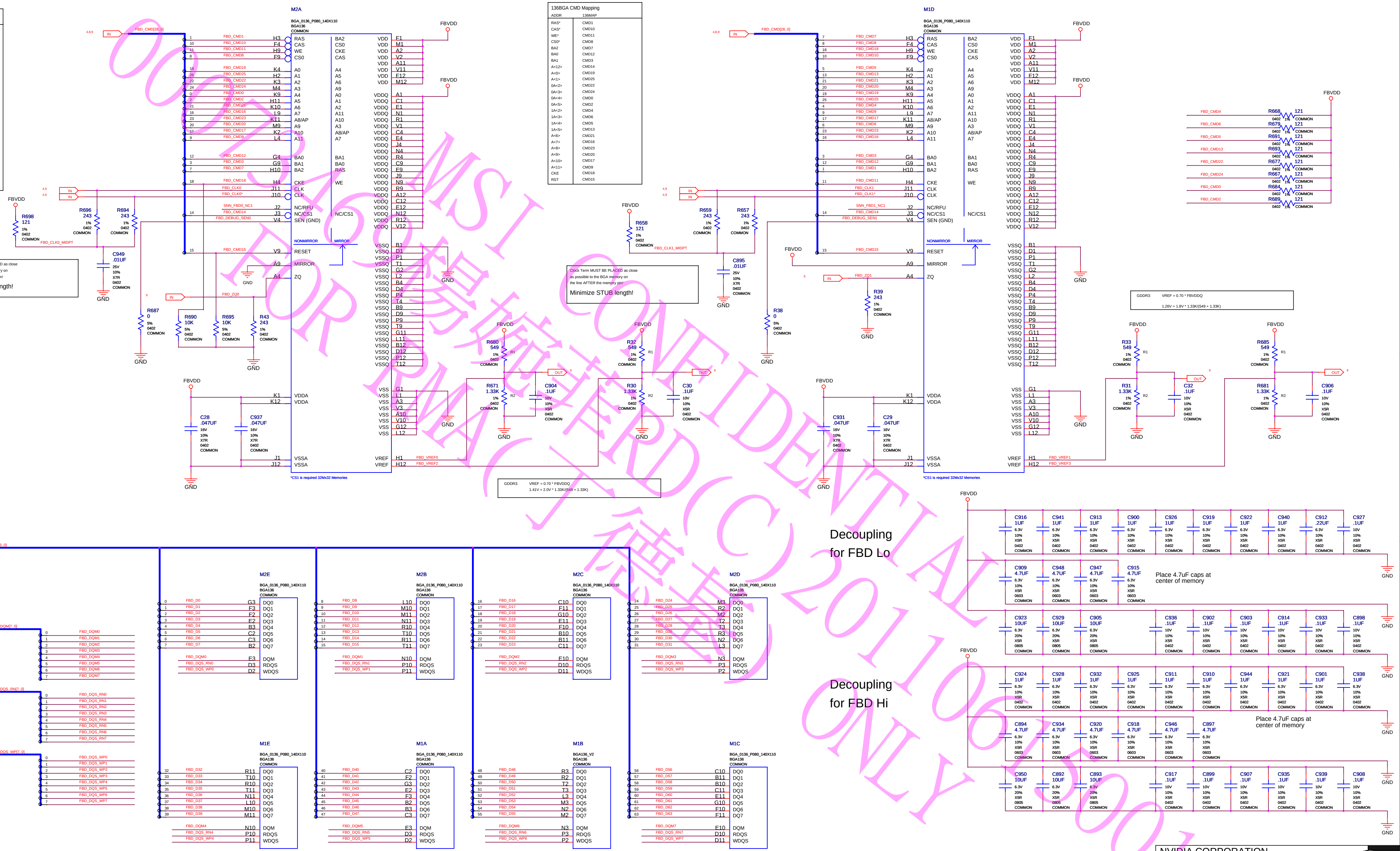
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15



ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBD Partition

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Page9: FrameBuffer Net Rules

NET RULES for FrameBuffer A/B

Page ref	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
3,5	OUT	FBA_CLK0	1	80DIFF	FBA_CLK0
3,5	OUT	FBA_CLK0*	1	80DIFF	FBA_CLK0
3,5	OUT	FBA_CLK1	1	80DIFF	FBA_CLK1
3,5	OUT	FBA_CLK1*	1	80DIFF	FBA_CLK1
3,5,5	OUT	FBA_CMD[28..0]	1	40OHM	
3,5	OUT	FBA_DQS_WP[7..0]	1	40OHM	
3,5	IN	FBA_DQS_RN[7..0]	1	40OHM	
3,5	OUT	FBA_DQM[7..0]	1	40OHM	
3,5	BI	FBA_D[63..0]	1	40OHM	

Page ref	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
3,6	OUT	FBB_CLK0	1	80DIFF	FBB_CLK0
3,6	OUT	FBB_CLK0*	1	80DIFF	FBB_CLK0
3,6	OUT	FBB_CLK1	1	80DIFF	FBB_CLK1
3,6	OUT	FBB_CLK1*	1	80DIFF	FBB_CLK1
3,6,6	OUT	FBB_CMD[28..0]	1	40OHM	
3,6	OUT	FBB_DQS_WP[7..0]	1	40OHM	
3,6	IN	FBB_DQS_RN[7..0]	1	40OHM	
3,6	OUT	FBB_DQM[7..0]	1	40OHM	
3,6	BI	FBB_D[63..0]	1	40OHM	
3	BI	FBA_DEBUG	1	40OHM	
3	BI	FBB_DEBUG	1	40OHM	

Page ref	Port	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
3	BI	FBAB_PLLAVDD	1.2V	0.02A	12MIL
5	BI	FBA_VREF0	1.26V	0.02A	12MIL
5	BI	FBA_VREF1	1.26V	0.02A	12MIL
5	BI	FBA_VREF2	1.26V	0.02A	12MIL
5	BI	FBA_VREF3	1.26V	0.02A	12MIL
5	BI	FBA_ZQ0	1.8V	0.02A	12MIL
5	BI	FBA_ZQ1	1.8V	0.02A	12MIL
6	BI	FBB_VREF0	1.26V	0.02A	12MIL
6	BI	FBB_VREF1	1.26V	0.02A	12MIL
6	BI	FBB_VREF2	1.26V	0.02A	12MIL
6	BI	FBB_VREF3	1.26V	0.02A	12MIL
6	BI	FBB_ZQ0	1.8V	0.02A	12MIL
6	BI	FBB_ZQ1	1.8V	0.02A	12MIL
3	BI	FB_VREF1	1.26V	0.02A	12MIL
3	BI	FB_VREF2	1.26V	0.02A	12MIL

NET RULES for FrameBuffer C/D

Page ref	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
4,7	OUT	FBC_CLK0	1	80DIFF	FBC_CLK0
4,7	OUT	FBC_CLK0*	1	80DIFF	FBC_CLK0
4,7	OUT	FBC_CLK1	1	80DIFF	FBC_CLK1
4,7	OUT	FBC_CLK1*	1	80DIFF	FBC_CLK1
4,7,7	OUT	FBC_CMD[28..0]	1	40OHM	
4,7	OUT	FBC_DQS_WP[7..0]	1	40OHM	
4,7	IN	FBC_DQS_RN[7..0]	1	40OHM	
4,7	OUT	FBC_DQM[7..0]	1	40OHM	
4,7	BI	FBC_D[63..0]	1	40OHM	

Page ref	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
4,8	OUT	FBD_CLK0	1	80DIFF	FBD_CLK0
4,8	OUT	FBD_CLK0*	1	80DIFF	FBD_CLK0
4,8	OUT	FBD_CLK1	1	80DIFF	FBD_CLK1
4,8	OUT	FBD_CLK1*	1	80DIFF	FBD_CLK1
4,8,8	OUT	FBD_CMD[28..0]	1	40OHM	
4,8	OUT	FBD_DQS_WP[7..0]	1	40OHM	
4,8	IN	FBD_DQS_RN[7..0]	1	40OHM	
4,8	OUT	FBD_DQM[7..0]	1	40OHM	
4,8	BI	FBD_D[63..0]	1	40OHM	
4	BI	FBC_DEBUG	1	40OHM	
4	BI	FBD_DEBUG	1	40OHM	

Page ref	Port	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
4	BI	FBCD_PLLAVDD	1.2V	0.02A	12MIL
7	BI	FBC_VREF0	1.26V	0.02A	12MIL
7	BI	FBC_VREF1	1.26V	0.02A	12MIL
7	BI	FBC_VREF2	1.26V	0.02A	12MIL
7	BI	FBC_VREF3	1.26V	0.02A	12MIL
7	BI	FBC_ZQ0	1.8V	0.02A	12MIL
7	BI	FBC_ZQ1	1.8V	0.02A	12MIL
8	BI	FBD_VREF0	1.26V	0.02A	12MIL
8	BI	FBD_VREF1	1.26V	0.02A	12MIL
8	BI	FBD_VREF2	1.26V	0.02A	12MIL
8	BI	FBD_VREF3	1.26V	0.02A	12MIL
8	BI	FBD_ZQ0	1.8V	0.02A	12MIL
8	BI	FBD_ZQ1	1.8V	0.02A	12MIL

ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FrameBuffer Net Rules

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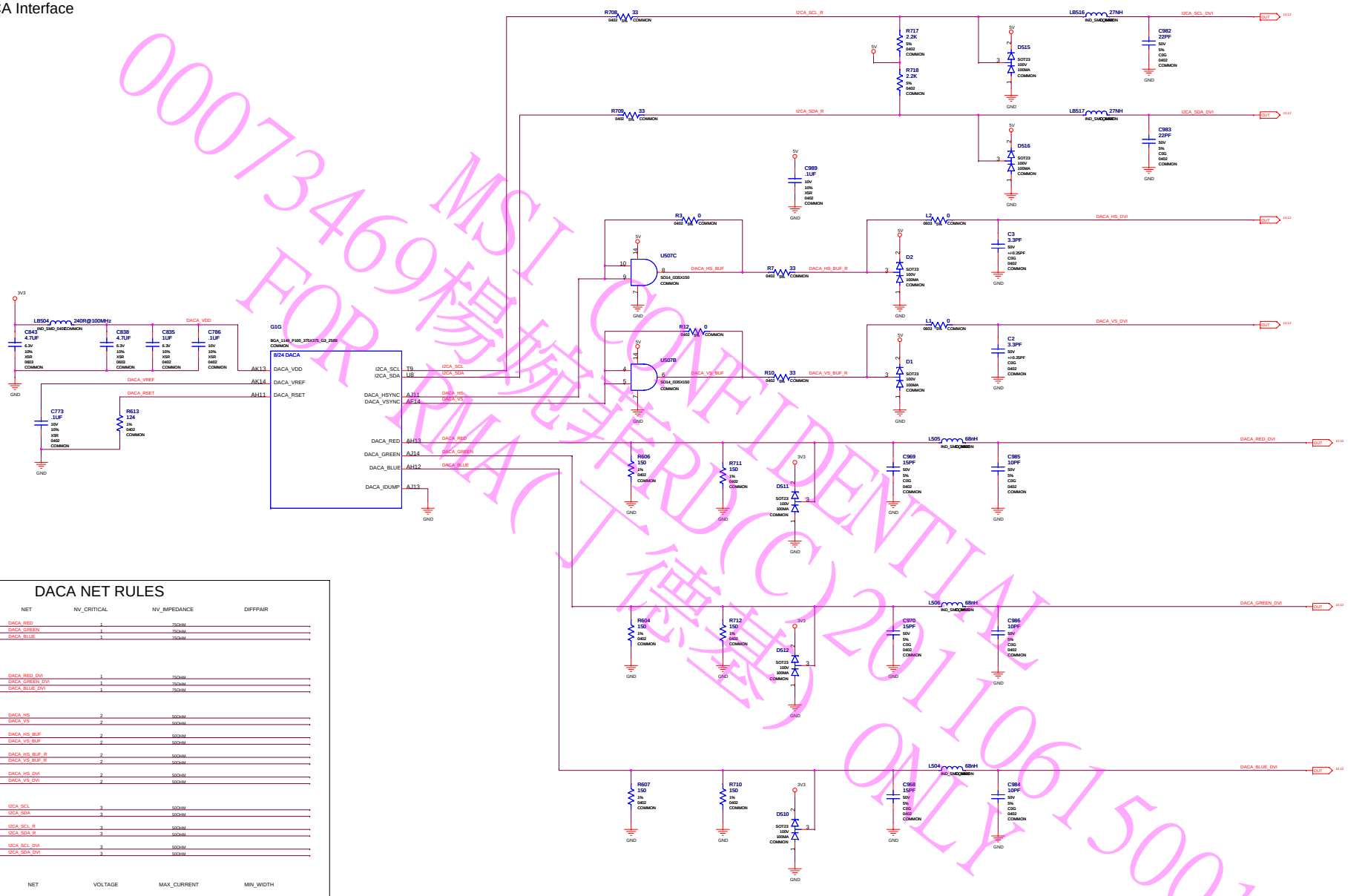
Page10: DACA Interface



DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACA_RED	1	75OHM	
DACA_GREEN	1	75OHM	
DACA_BLUE	1	75OHM	
DACA_RED_DVI	1	75OHM	
DACA_GREEN_DVI	1	75OHM	
DACA_BLUE_DVI	1	75OHM	
DACA_HS	2	50OHM	
DACA_VS	2	50OHM	
DACA_HS_BUF	2	50OHM	
DACA_VS_BUF	2	50OHM	
DACA_HS_BUF_R	2	50OHM	
DACA_VS_BUF_R	2	50OHM	
DACA_HS_DVI	2	50OHM	
DACA_VS_DVI	2	50OHM	
I2CA_SCL	3	50OHM	
I2CA_SDA	3	50OHM	
I2CA_SCL_R	3	50OHM	
I2CA_SDA_R	3	50OHM	
I2CA_SCL_DVI	3	50OHM	
I2CA_SDA_DVI	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACA_VREF			12MIL
DACA_RSET			12MIL
DACA_VDD	3.3V	0.100A	18MIL

ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA Interface

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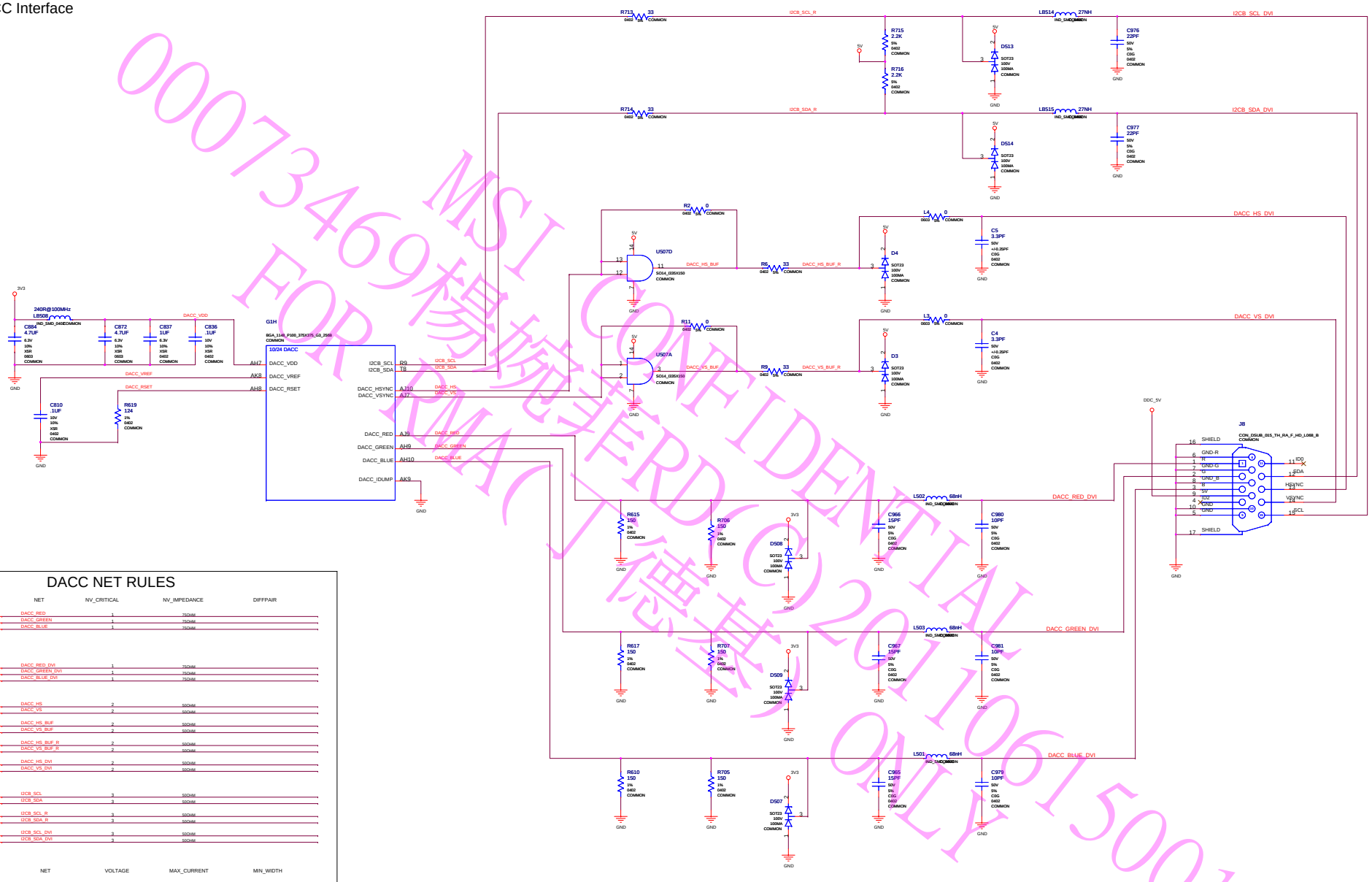
Page11: DACC Interface



DACC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACC_RED	1	75OHM	
DACC_GREEN	1	75OHM	
DACC_BLUE	1	75OHM	
DACC_RED_DVI	1	75OHM	
DACC_GREEN_DVI	1	75OHM	
DACC_BLUE_DVI	1	75OHM	
DACC_HS	2	50OHM	
DACC_VS	2	50OHM	
DACC_HS_BUF	2	50OHM	
DACC_VS_BUF	2	50OHM	
DACC_HS_BUF_R	2	50OHM	
DACC_VS_BUF_R	2	50OHM	
DACC_HS_DVI	2	50OHM	
DACC_VS_DVI	2	50OHM	
I2CB_SCL	3	50OHM	
I2CB_SDA	3	50OHM	
I2CB_SCL_R	3	50OHM	
I2CB_SDA_R	3	50OHM	
I2CB_SCL_DVI	3	50OHM	
I2CB_SDA_DVI	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACC_VREF			12MIL
DACC_RSET			12MIL
DACC_VDD	3.3V	0.100A	18MIL

ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC Interface

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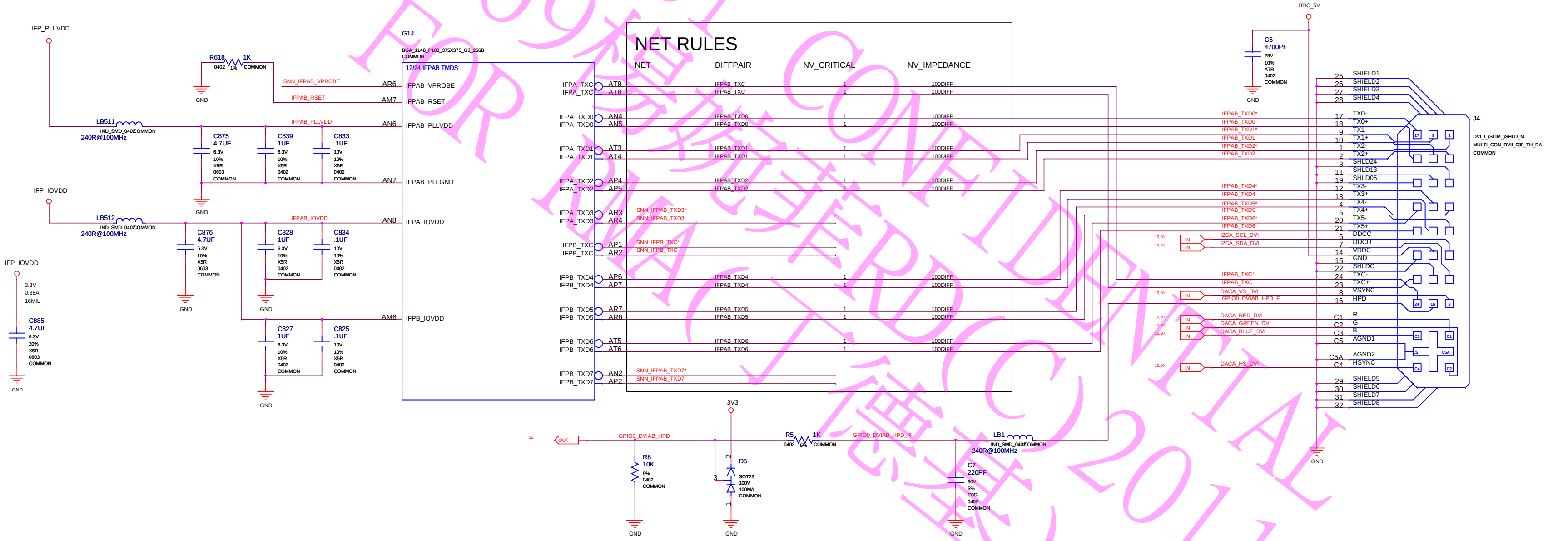
Page12: IFP A/B DVI Interface

IFPABCD NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RSET			12MIL
GPIO0_DVIAB_HPD_F	3	50OHM	
GPIO0_DVIAB_HPD_R	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLLVDD	1.8V	0.03A	16MIL
IFPAB_IOVDD	3.3V	0.09A	16MIL



ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP A/B and C/D Interface

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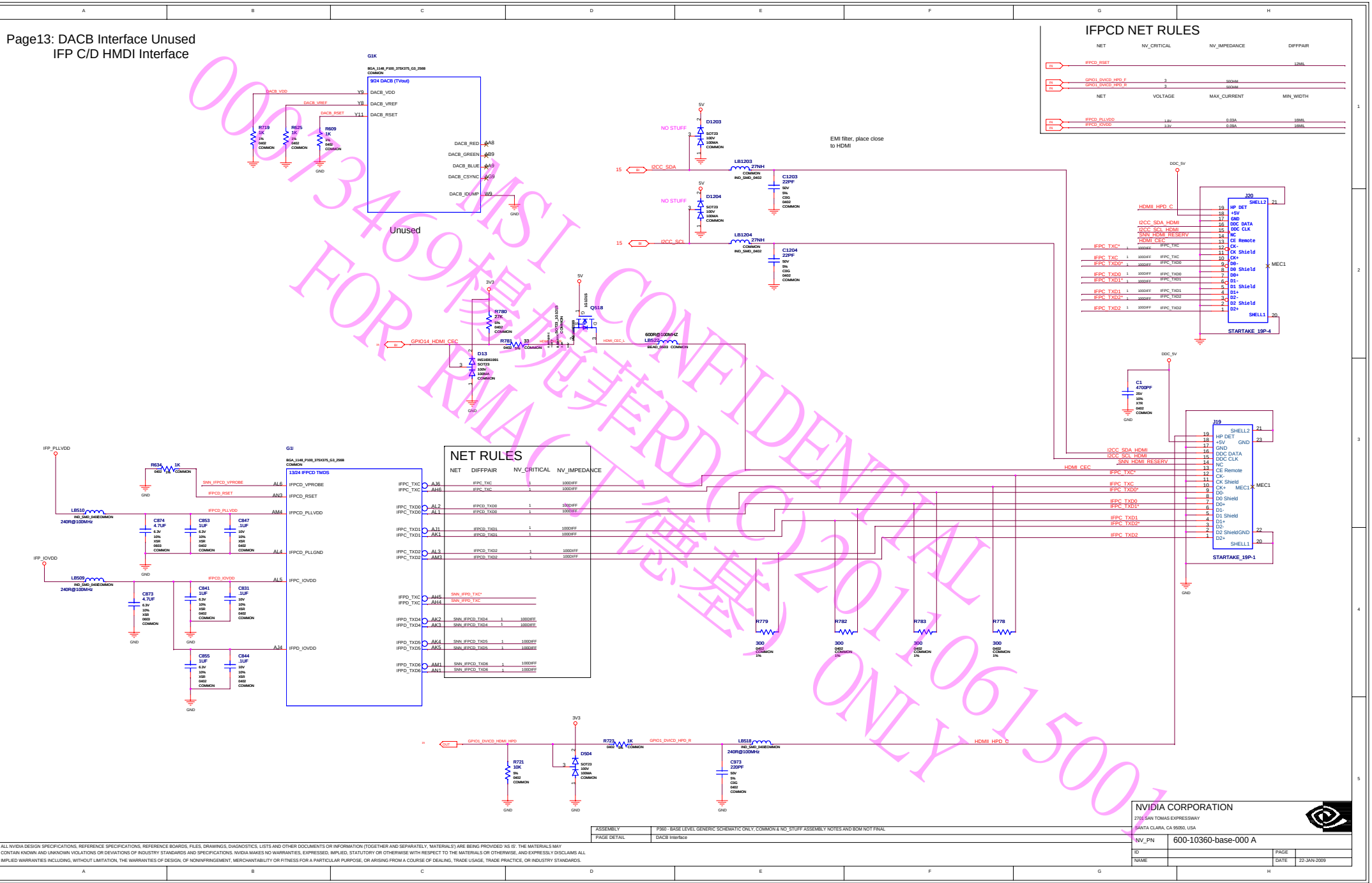
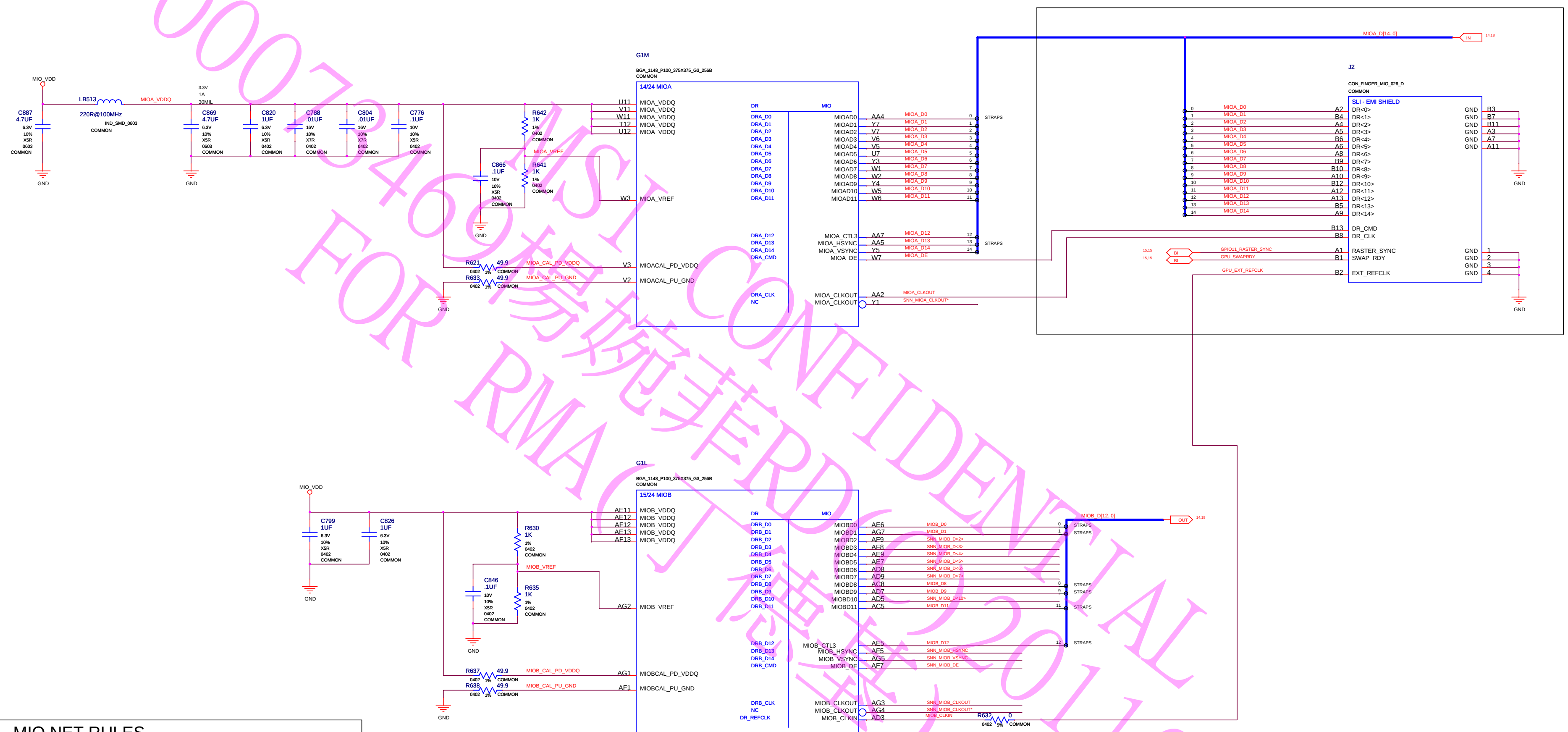
Page13: DACB Interface Unused
IFP C/D HMDI Interface



Page14: Multi-use IO(MIO) Interface

MIO Feature Connector



MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
MIOA_D[14..0]	1	50OHM	
MIOA_CLKOUT	1	50OHM	
MIOA_DE	1	50OHM	
MIOB_D[12..0]	1	50OHM	
MIOB_CLKIN	1	50OHM	
GPU_EXT_REFCLK	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	1.65V		12MIL
MIOACAL_PD_VDDQ			12MIL
MIOACAL_PU_GND			12MIL
MIOB_VREF	1.65V		12MIL
MIOBCAL_PD_VDDQ			12MIL
MIOBCAL_PU_GND			12MIL

ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Multi-use IO(MIO) Interface

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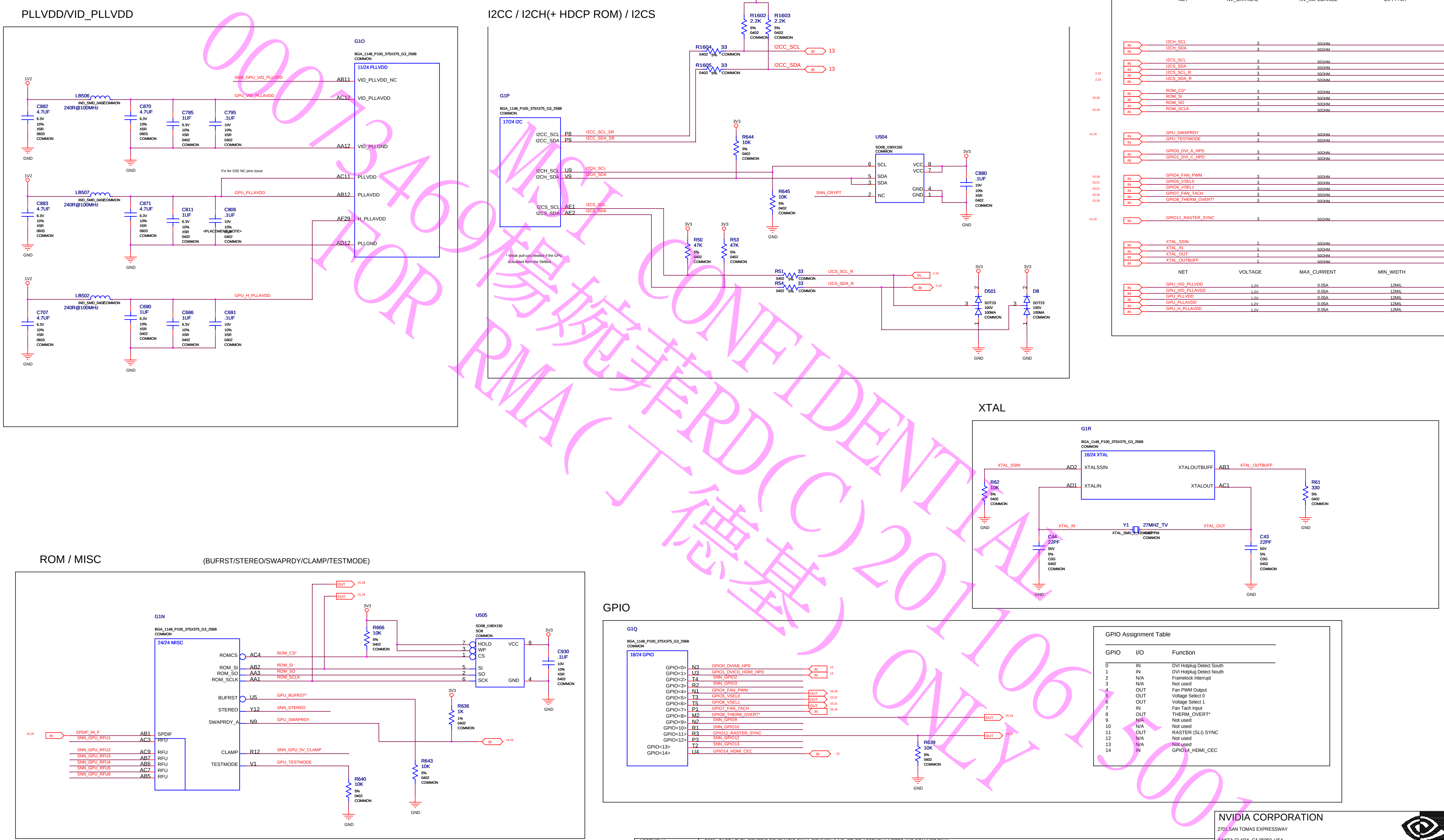
Page15: MISC: GPIO, I2C, BIOS, PLL, and XTAL



MISC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
I2CH_SCL	3	50OHM	
I2CH_SDA	3	50OHM	
I2CS_SCL	3	50OHM	
I2CS_SDA	3	50OHM	
I2CS_SCL_R	3	50OHM	
I2CS_SDA_R	3	50OHM	
ROM_CS*	3	50OHM	
ROM_SI	3	50OHM	
ROM_SO	3	50OHM	
ROM_SCLK	3	50OHM	
GPU_SWAPRDY	3	50OHM	
GPU_TESTMODE	3	50OHM	
GPIO0_DVI_A_HPD	3	50OHM	
GPIO1_DVI_C_HPD	3	50OHM	
GPIO4_FAN_PWM	3	50OHM	
GPIO5_VSEL0	3	50OHM	
GPIO6_VSEL1	3	50OHM	
GPIO7_FAN_TACH	3	50OHM	
GPIO8_THERM_OVERT*	3	50OHM	
GPIO11_RASTER_SYNC	3	50OHM	
XTAL_SSIN	1	50OHM	
XTAL_IN	1	50OHM	
XTAL_OUT	1	50OHM	
XTAL_OUTBUFF	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
GPU_VID_PLLVDD	1.2V	0.05A	12MIL
GPU_VID_PLLAVDD	1.2V	0.05A	12MIL
GPU_PLLVDD	1.2V	0.05A	12MIL
GPU_PLLAVDD	1.2V	0.05A	12MIL
GPU_H_PLLAVDD	1.2V	0.05A	12MIL

GPIO Assignment Table

GPIO	I/O	Function
0	IN	DVI Hotplug Detect South
1	IN	DVI Hotplug Detect Nouth
2	N/A	Framelock Interrupt
3	N/A	Not used
4	OUT	Fan PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fan Tach Input
8	OUT	THERM_OVERT*
9	N/A	Not used
10	N/A	Not used
11	OUT	RASTER (SLI) SYNC
12	N/A	Not used
13	N/A	Not used
14	IN	GPIO14_HDMI_CEC

ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO, I2C, BIOS, PLL, and XTAL

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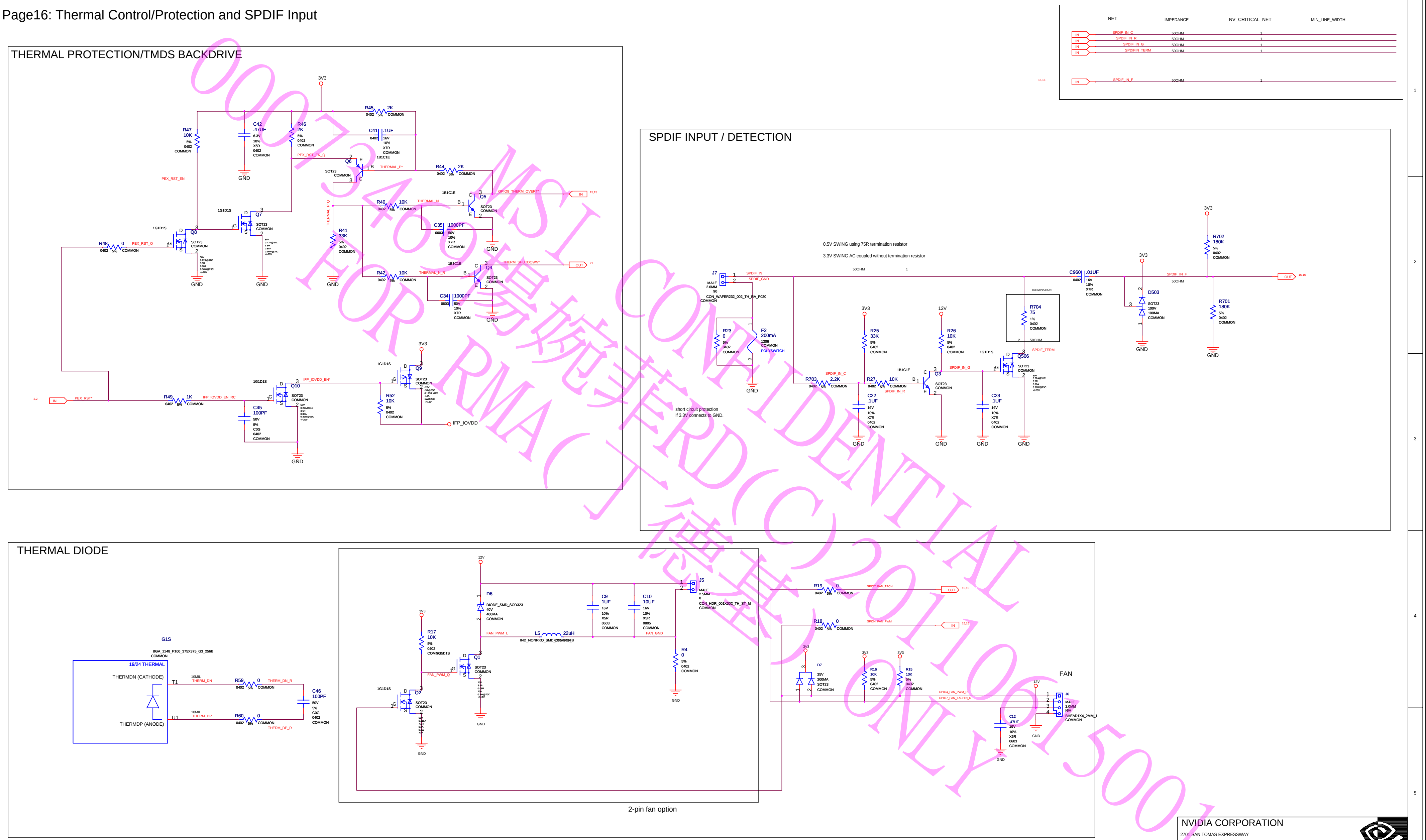
Page16: Thermal Control/Protection and SPDIF Input



ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Control/Protection and SPDIF Input

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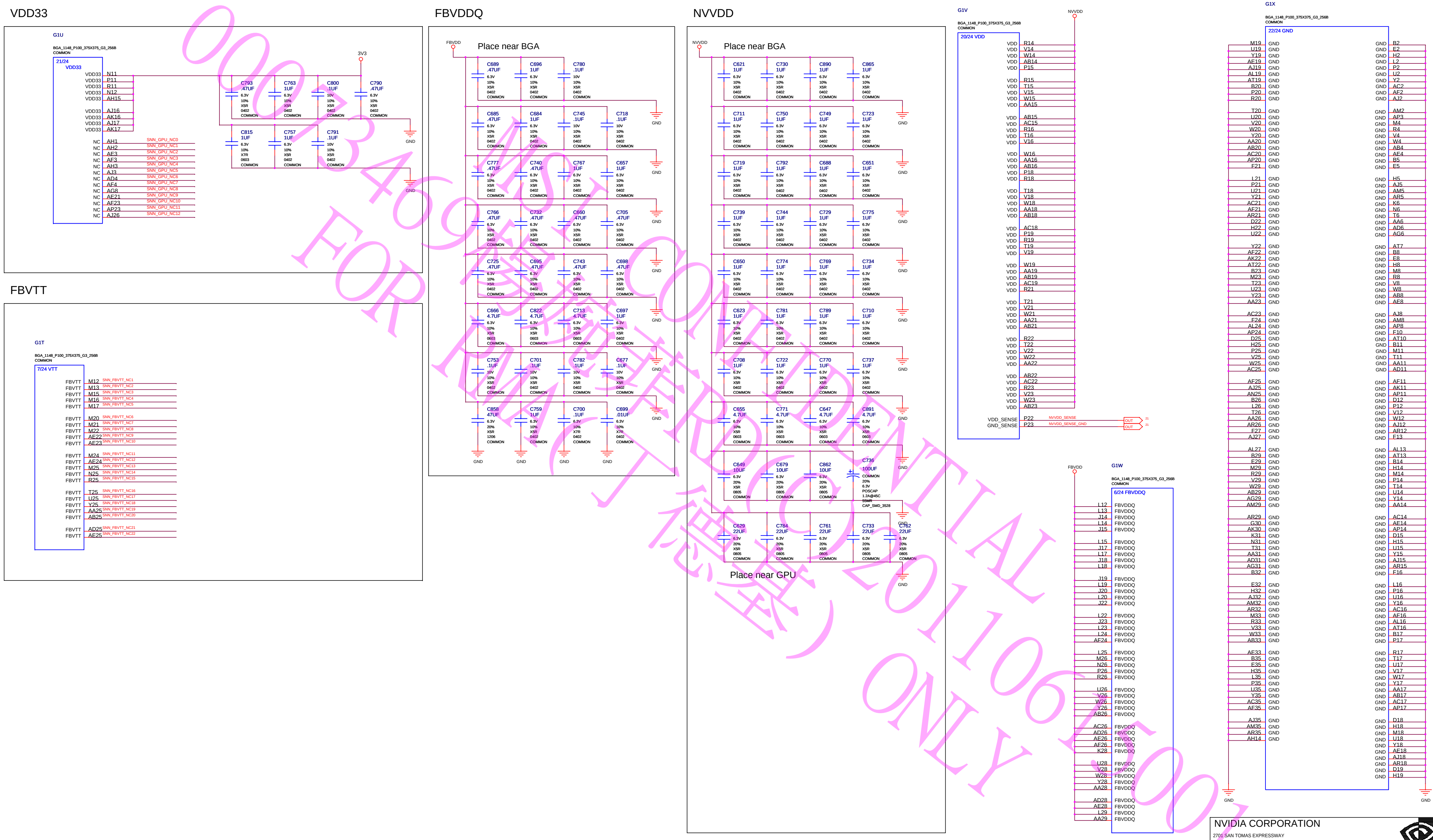
Page17: Power/GND and Decoupling

NVVVD and FBVVD decoupling need final data from SI



ASSEMBLY	P360 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power/GND and Decoupling

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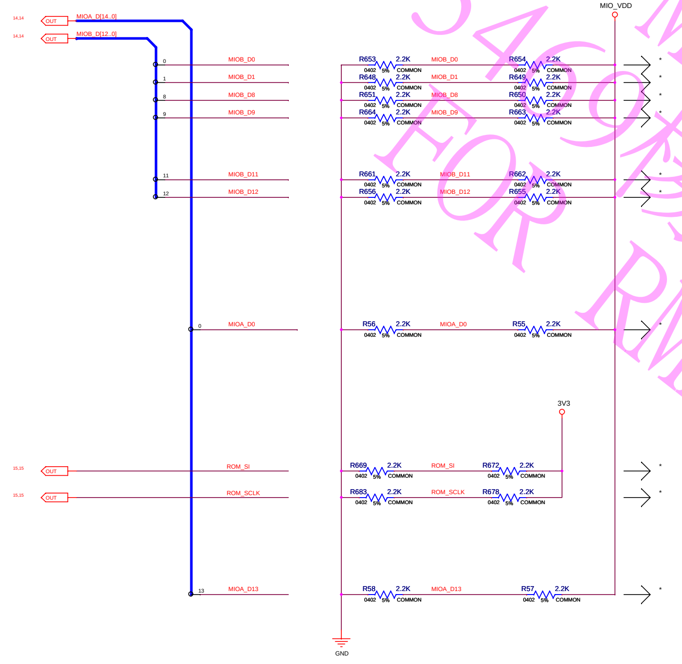
Page18: Configuration Straps and Mechanical

STRAPS



STRAP 0

	Samsung 256b 8Mx32 256MB	Samsung 256b 16Mx32 512MB	Hynix 256b 8Mx32 256MB	Hynix 256b 16Mx32 512MB	Qimonda 256b 16Mx 32 521MB
* 02: RAM_CFG[0]	1	1	0	0	1
* 03: RAM_CFG[1]	1	1	1	1	0
* 04: RAM_CFG[2]	1	0	1	0	0
* 05: RAM_CFG[3]	0	0	0	0	0

4 3

* 13: PCI_DEVID[3] DEVID = 0x0614 DT0 G92-279 0001 0100

* 28: PCI_DEVID[4] 0x0614 DT50 G92-289 0001 0100

* 17: PEX_PLL_EN_TERM100

Per G92 Guide (PEX term)..
* Strap definition inverted
  - set to 0x1 to enable
  - set to 0x0 to disable

STRAP 1

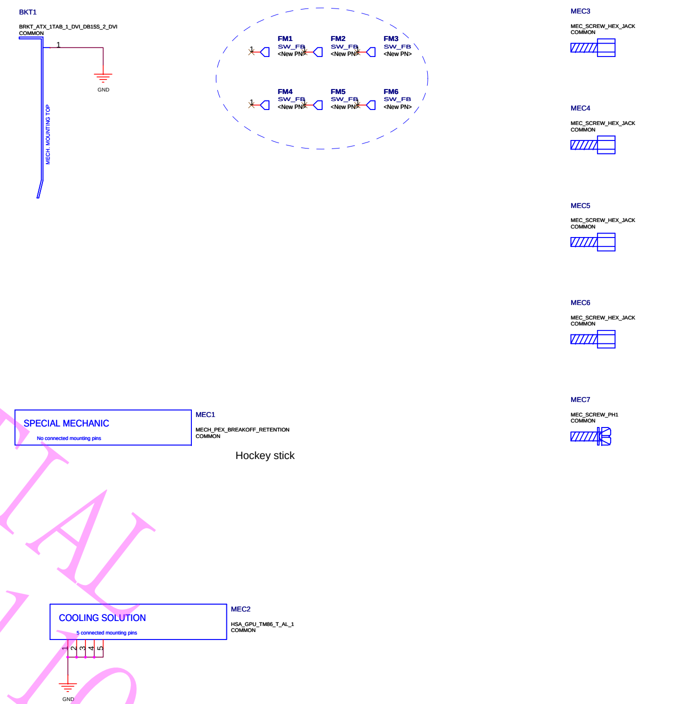
* 12: MIO_EN_33V_0 — DEFAULT = 1 (3.3V), MIOA = 0 (2.5V)

* 13: MIO_EN_33V_1 — DEFAULT = 1 (3.3V), MIOB = 0 (2.5V)

* 15: SLOT_CLK_CFG — DISABLE = 0; ENABLE = 1

MECHANICAL

Mechanical parts need be updated when we have the final solution



Hockey stick

Currently it's a preliminary symbol.

New fansink will be updated to BOM.

ASSEMBLY

PAGE DETAIL: Configuration Straps and Mechanical

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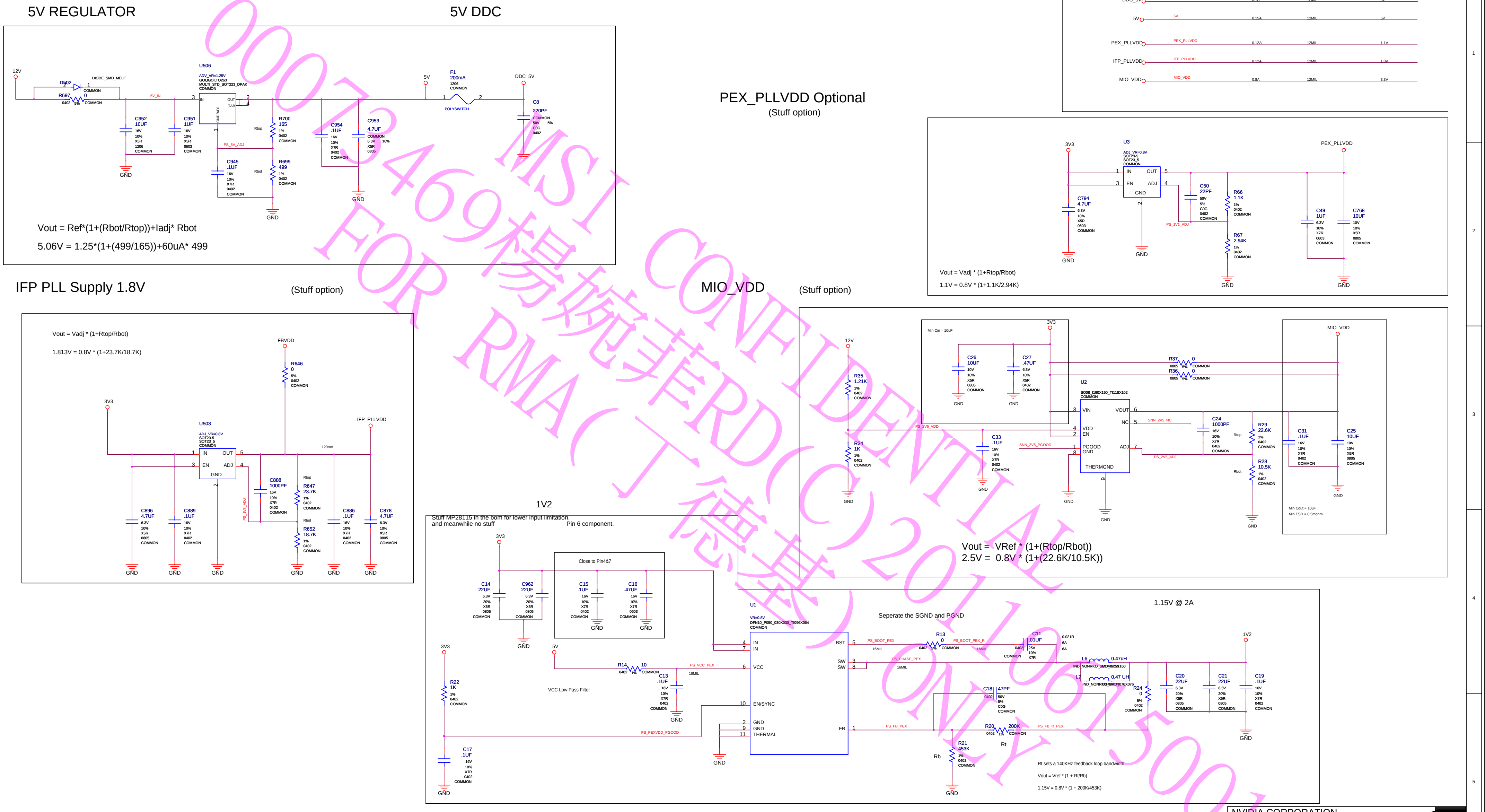
Page 19:Power Supply:IFP_PLLVDD,MIO_VDD,PEX_PLLVDD Option,DDV_5V

NETNAME		MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	DDC_5V	0.1A	12MIL	5V
5V	5V	0.15A	12MIL	5V
PEX_PLLVDD	PEX_PLLVDD	0.12A	12MIL	1.1V
IFP_PLLVDD	IFP_PLLVDD	0.12A	12MIL	1.8V
MIO_VDD	MIO_VDD	0.8A	12MIL	3.3V



ASSEMBLY	
PAGE DETAIL	Power Supply:IFP_PLLVDD,MIO_VDD,PEX_PLLVDD Option,DDV_5V

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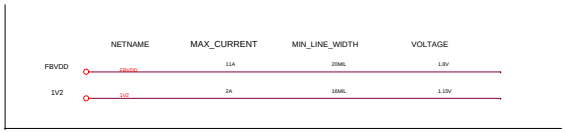
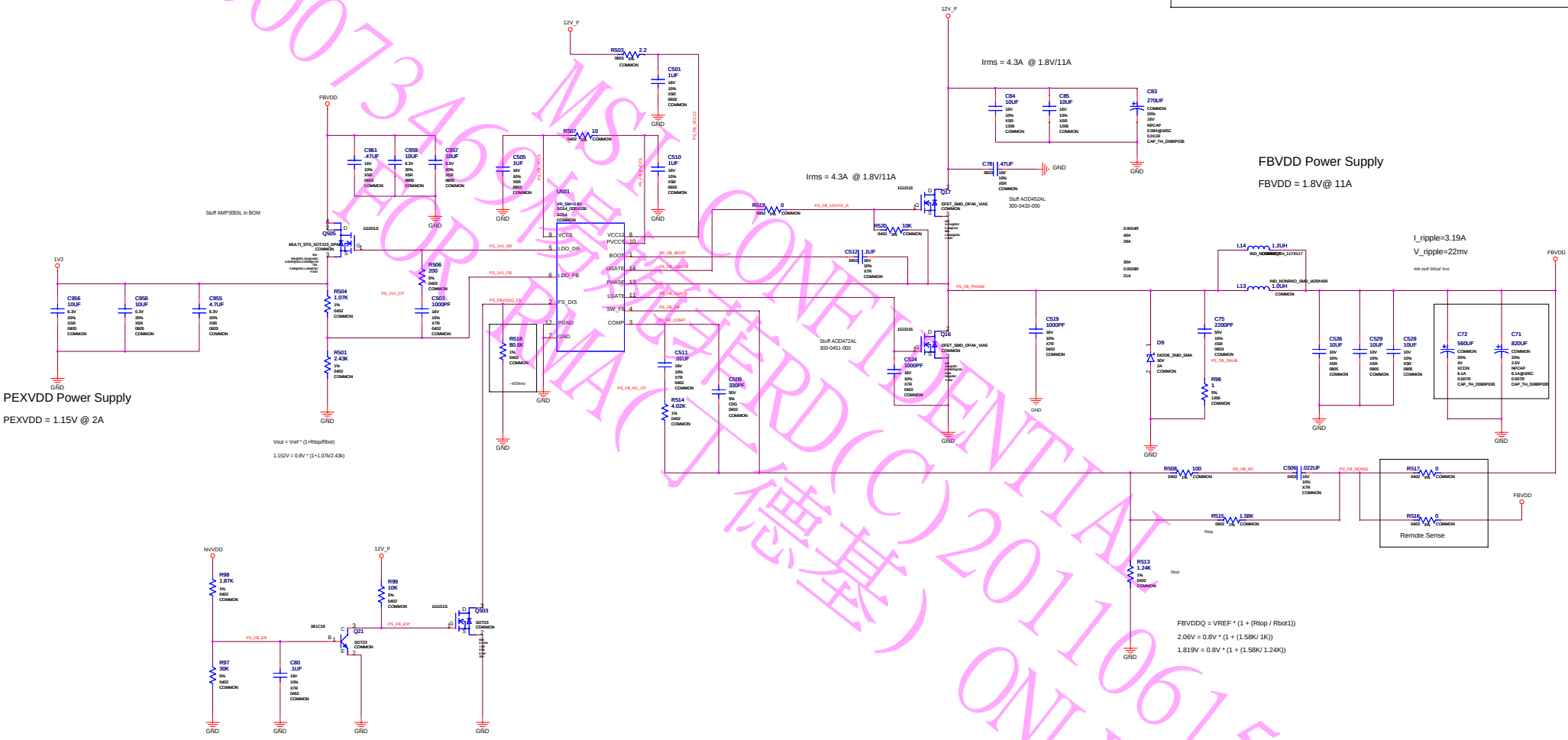
Page20:POWER SUPPLY: FBVDD,PEX_VDD





ASSEMBLY	
PAGE DETAIL	POWER SUPPLY: FBVDD,PEX_VDD

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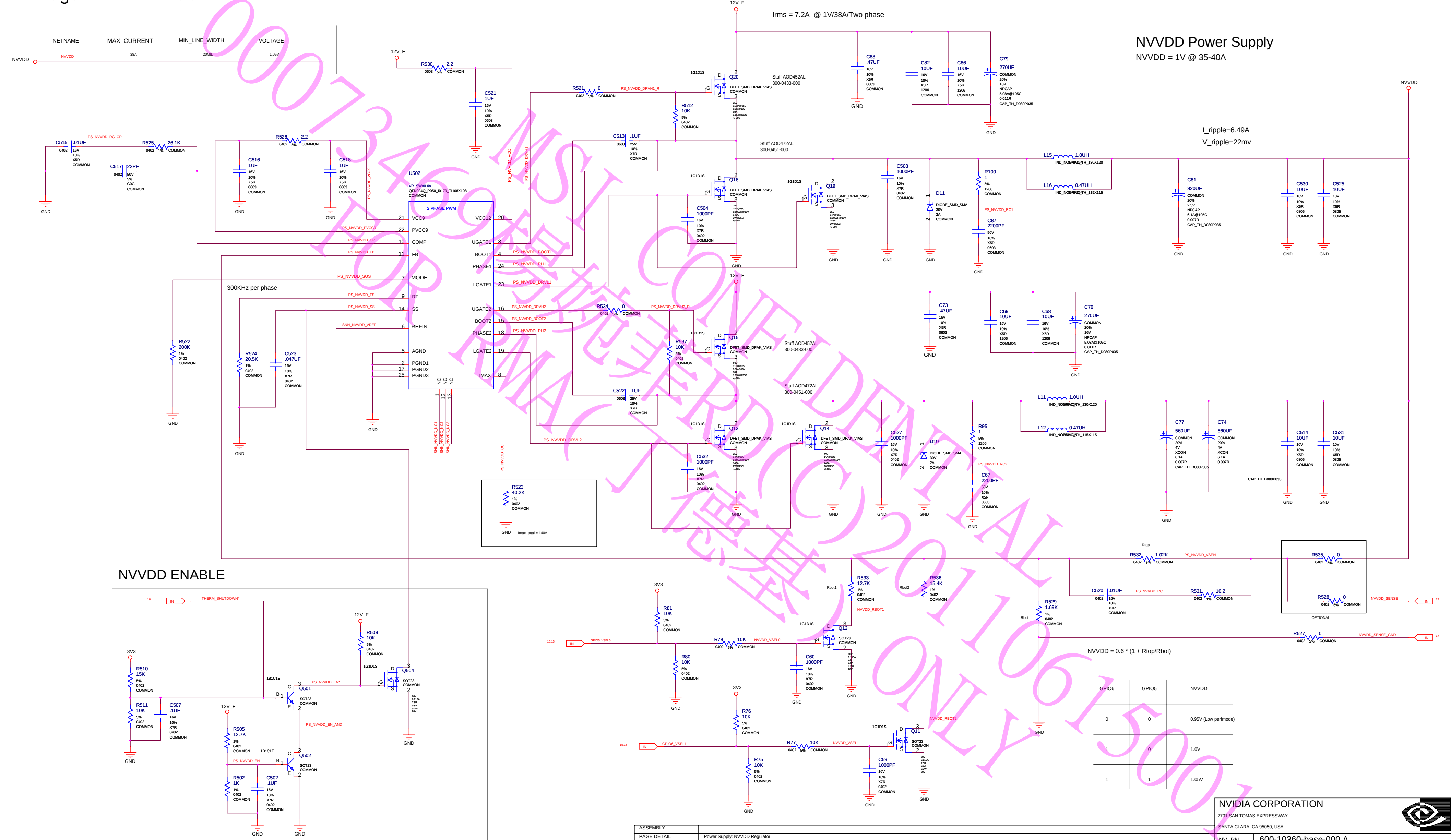
Page21:POWER SUPPLY: NVVDD

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
NVVDD	38A	20MIL	1.05V



GPIO6	GPIO5	NVVDD
0	0	0.95V (Low perfmode)
1	0	1.0V
1	1	1.05V

ASSEMBLY
PAGE DETAIL: Power Supply: NVVDD Regulator

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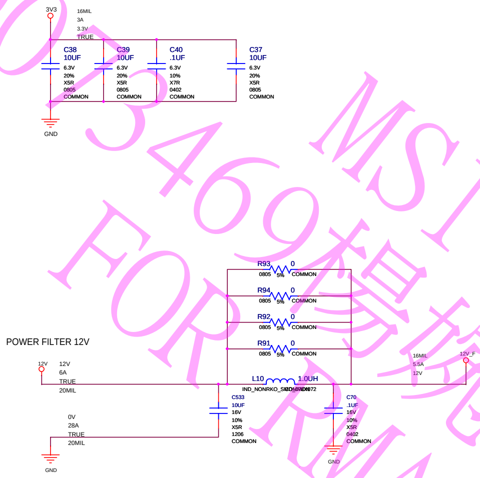
Page22: Power Supply: Filter of 12V,3V3



ASSEMBLY	
PAGE DETAIL	Power Supply: Filter of 3V3, 12V

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