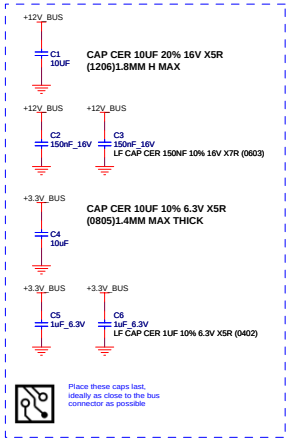
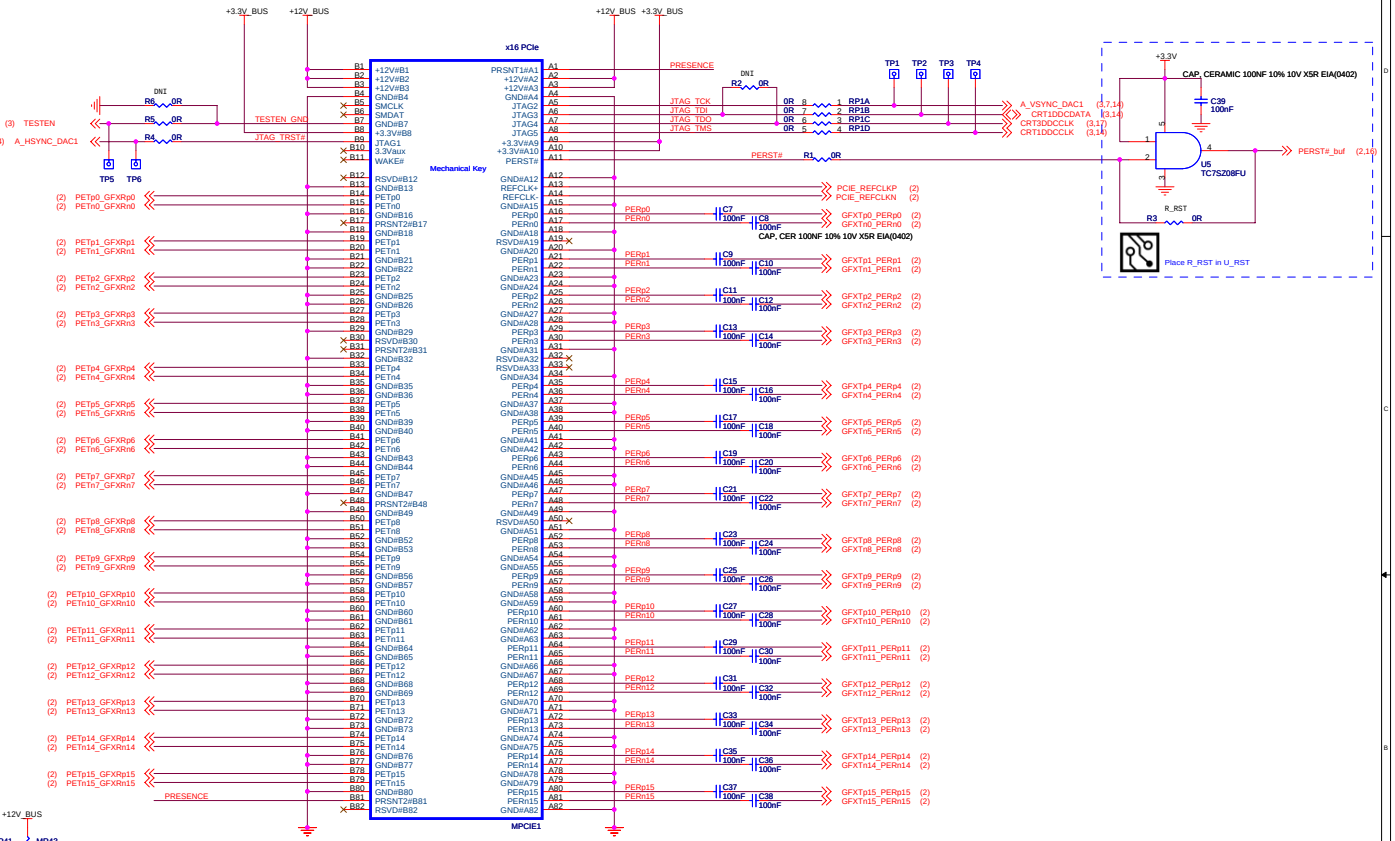
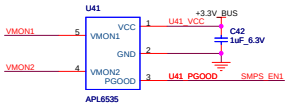
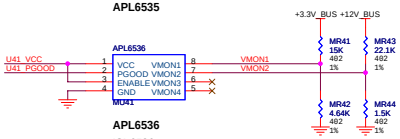
PCI-EXPRESS EDGE CONNECTOR

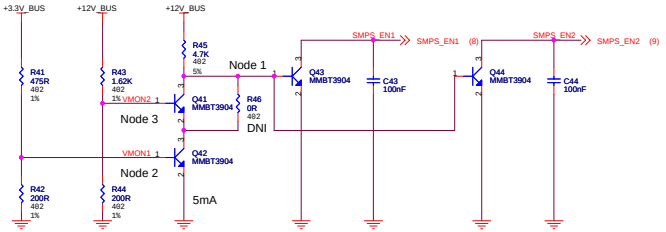




POWER SEQUENCING







Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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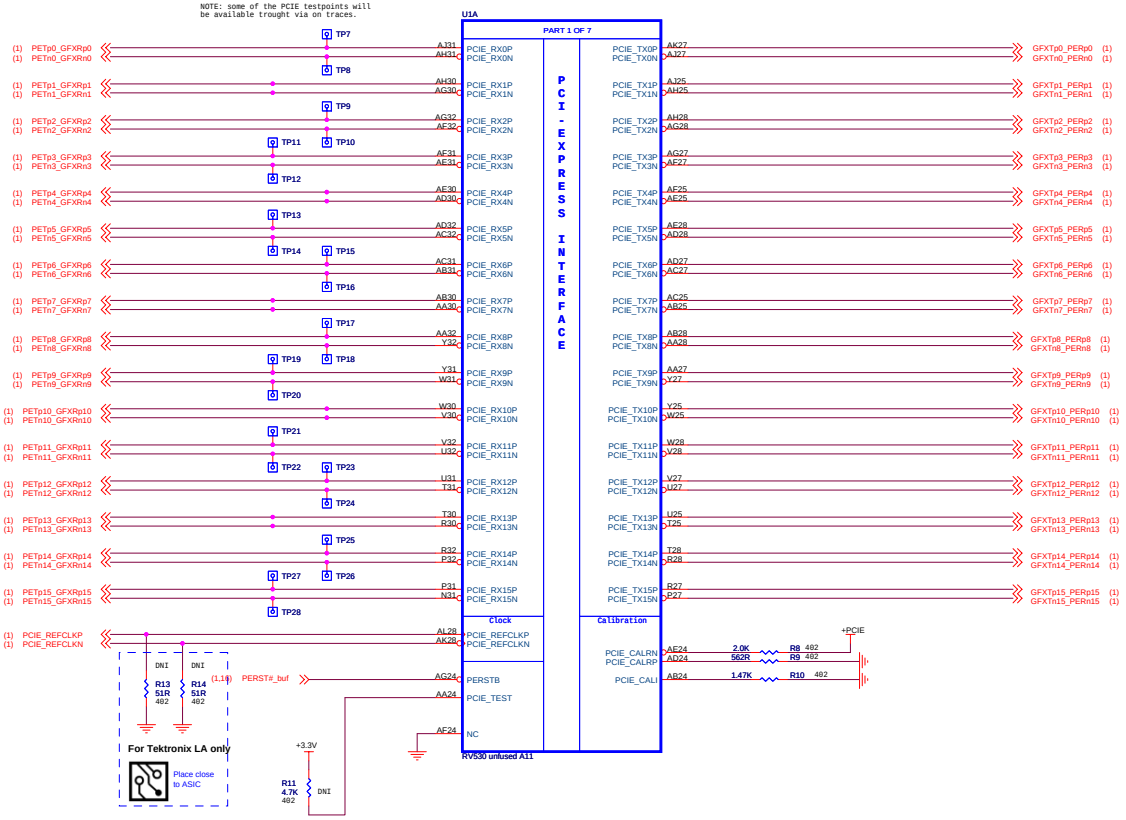
Size C	Document Number 105-A676xx-00C		Rev 2
Date: Saturday, August 06, 2005		Sheet 1 of 20	



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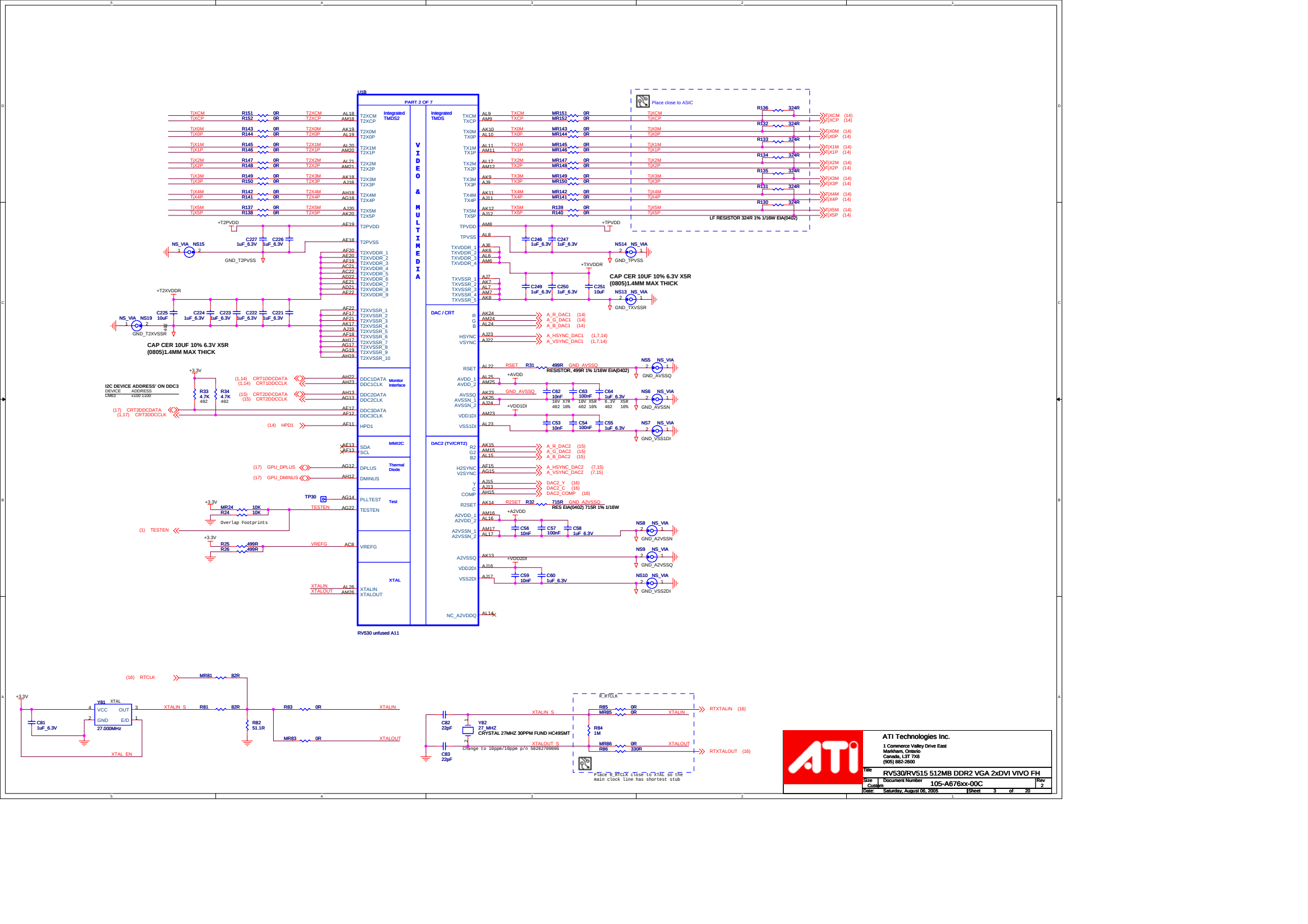
U1B
PART 2 OF 7
VIDEO & MULTIMEDIA
Integrated TMDS2
Integrated TMDS
DAC / CRT
DAC2 (TV/CRT2)
Monitor Interface
MMI2C
Thermal Diode
Test
XTAL
RV530 unfused A11
Place close to ASIC
LF RESISTOR 324R 1% 1/16W EIA(0402)
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK
I2C DEVICE ADDRESS' ON DDC3
RESISTOR, 499R 1% 1/16W EIA(0402)
RES EIA(0402) 715R 1% 1/16W
Overlap Footprints
Change to 18ppm/18ppm p/n 5028270800G
Place R_RTCLK close to XTAL so the main clock line has shortest stub
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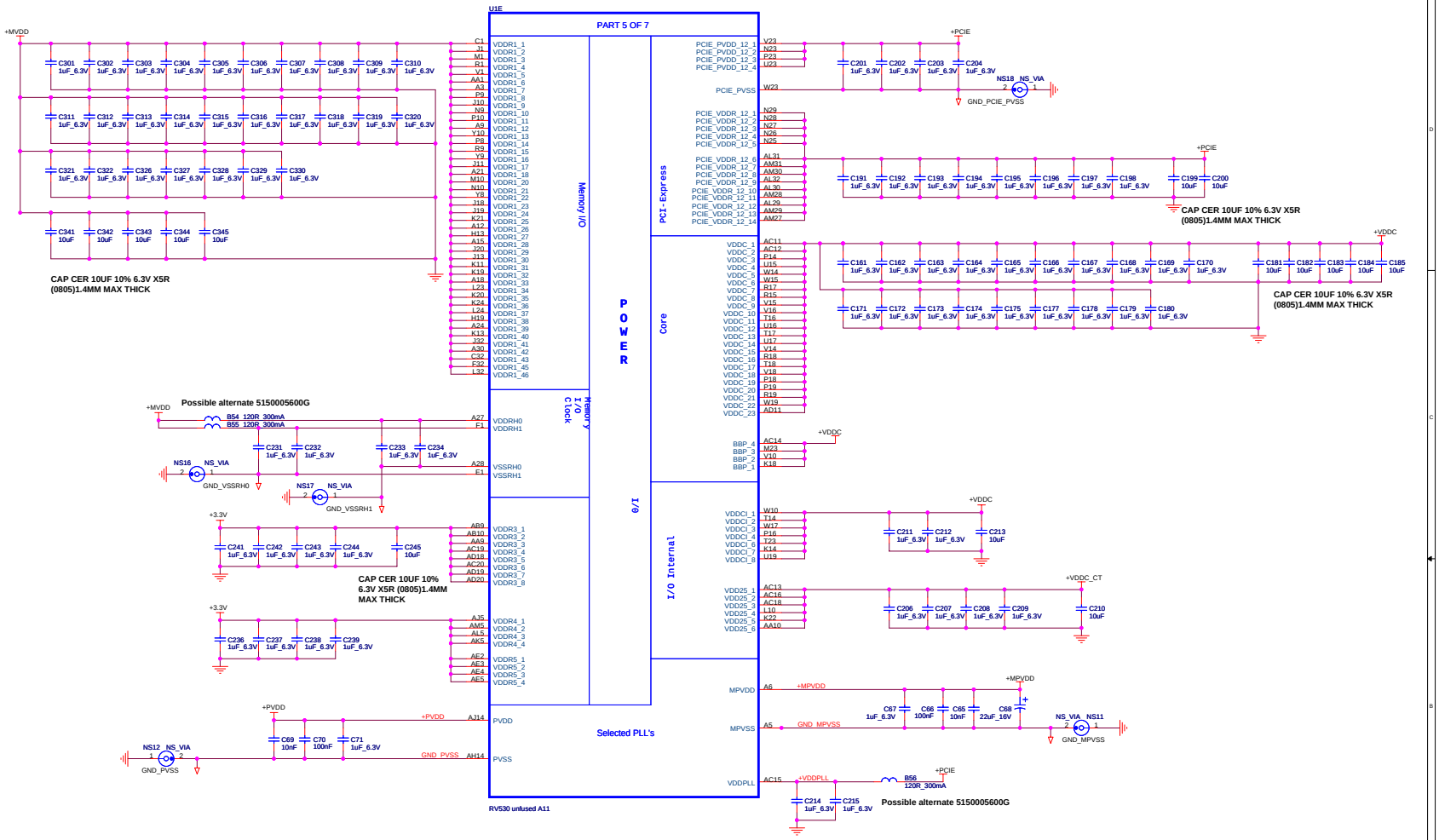

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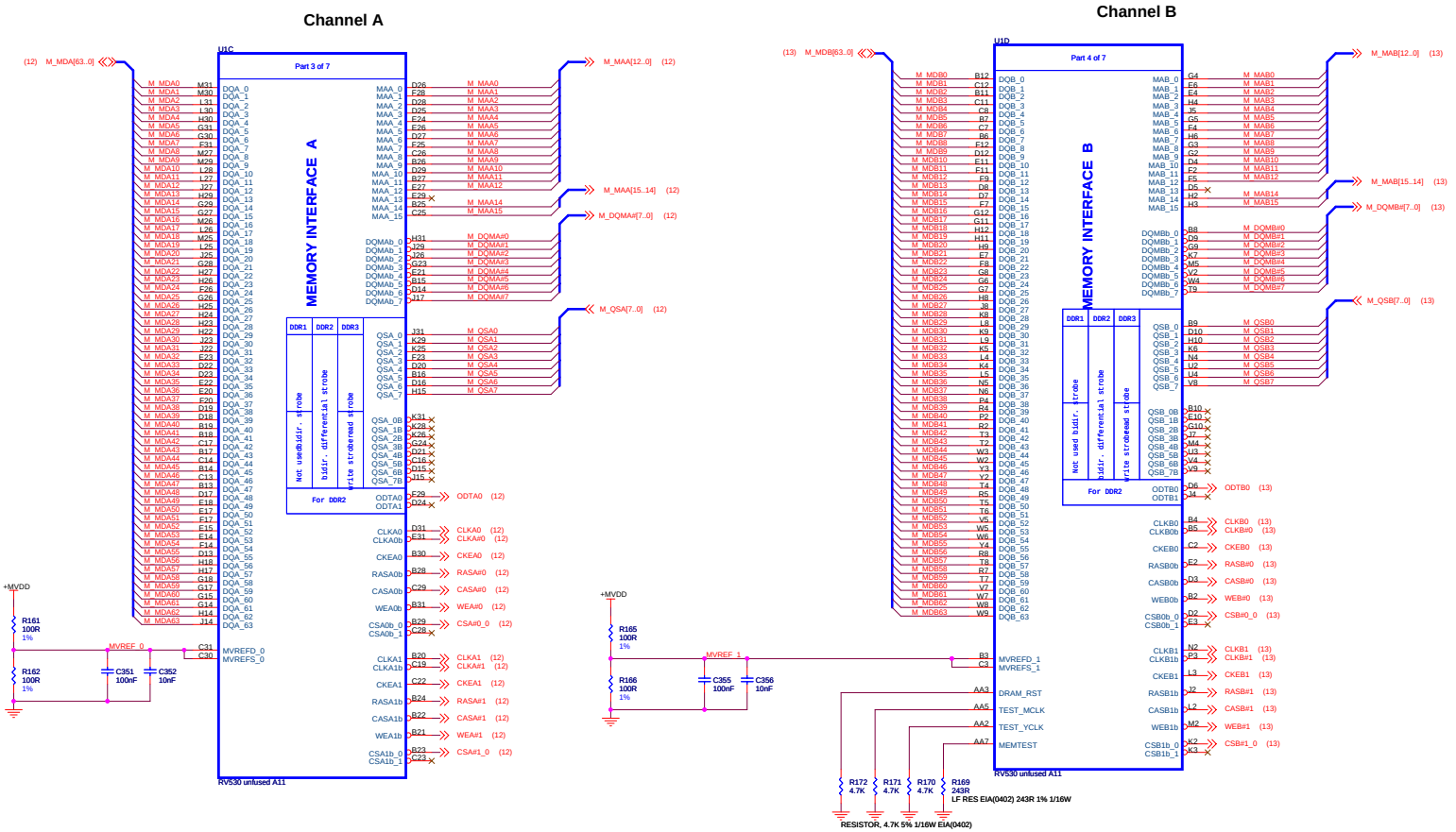
RV530 MEMORY CHANNELS A and B



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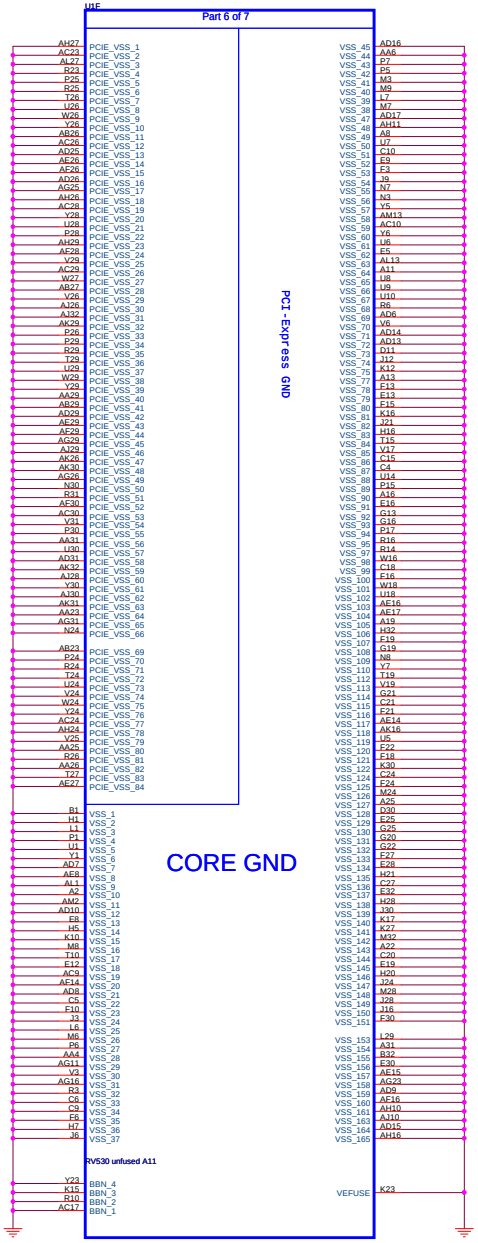

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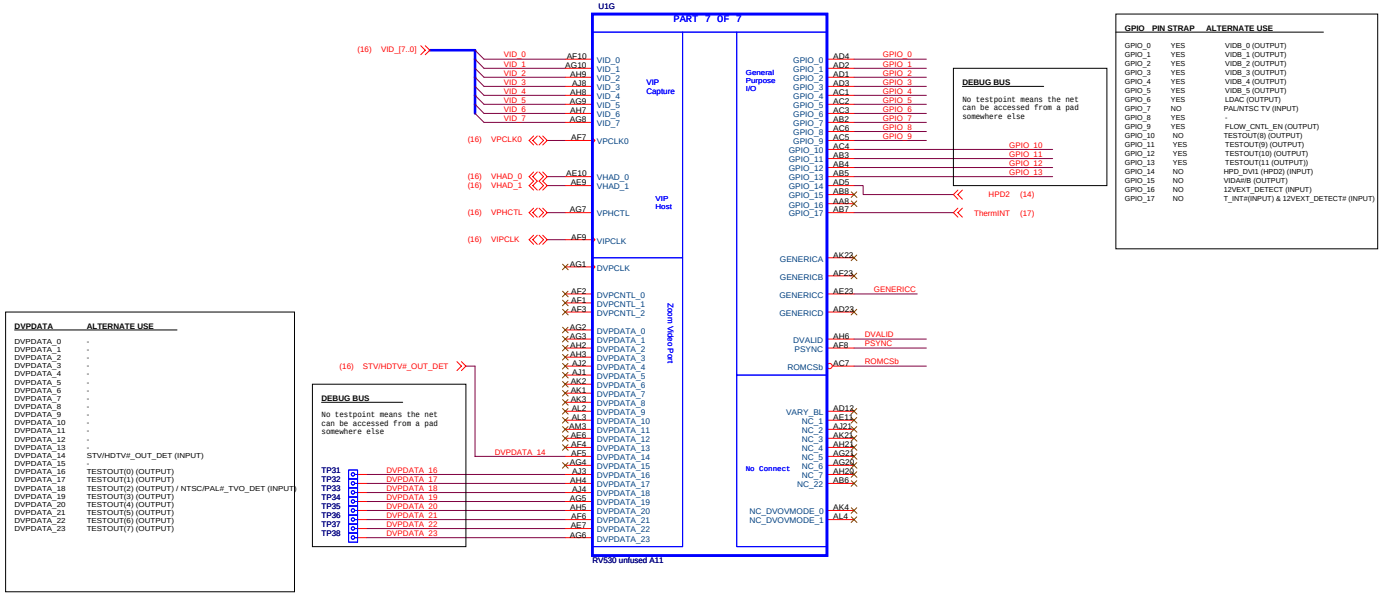
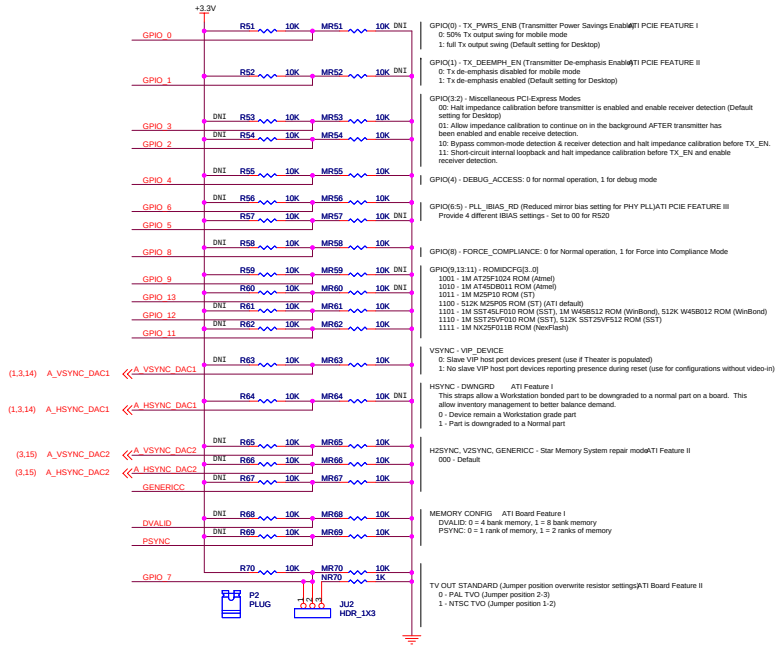
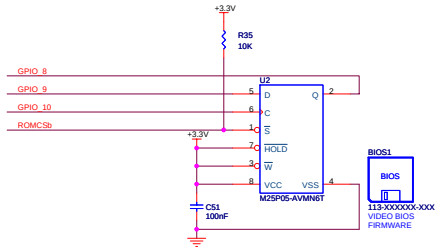


PIN BASED STRAPS





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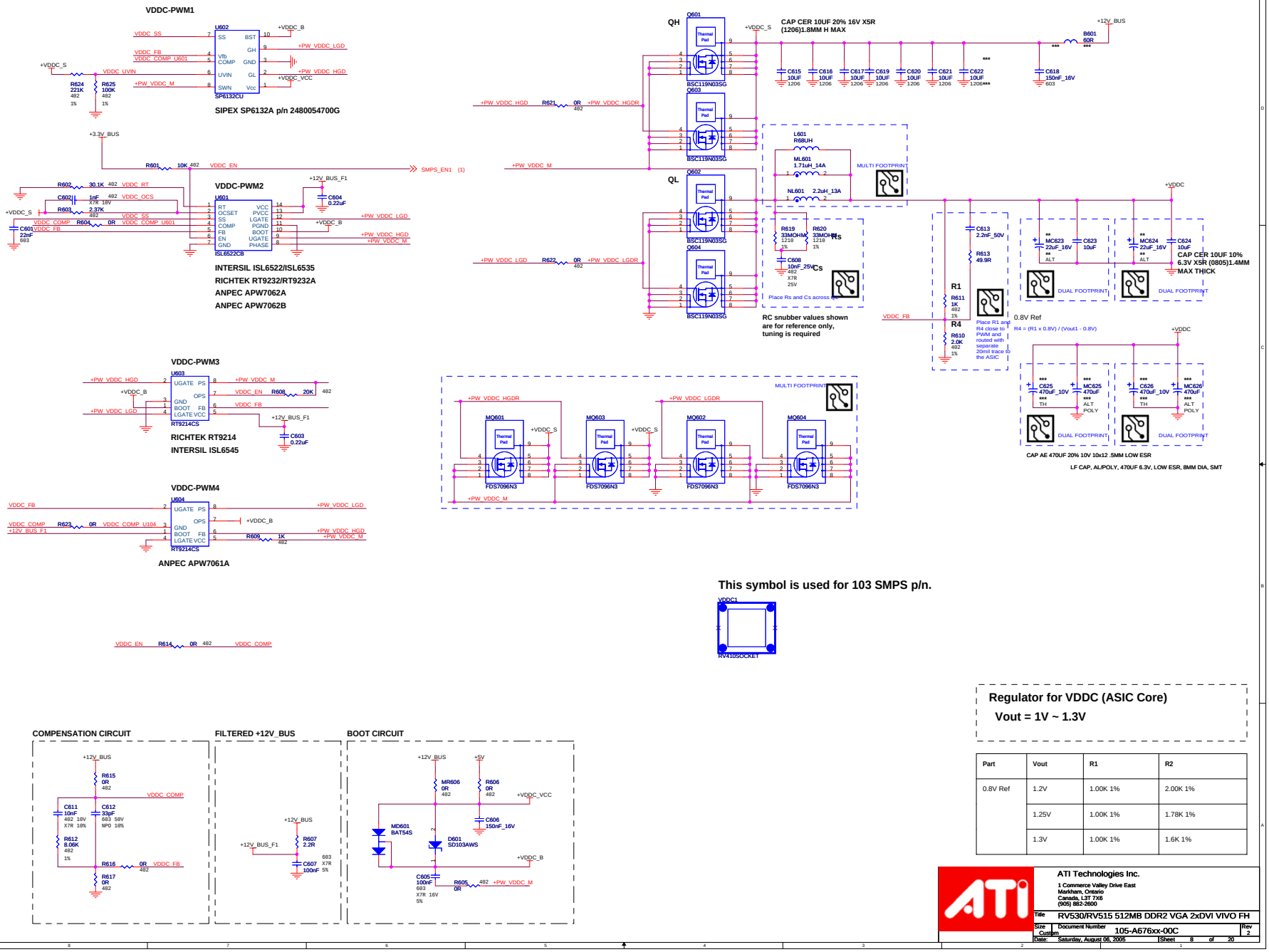

Regulator for VDDC (ASIC Core)

Vout = 1V ~ 1.3V

Part	Vout	R1	R2
0.8V Ref	1.2V	1.00K 1%	2.00K 1%
	1.25V	1.00K 1%	1.78K 1%
	1.3V	1.00K 1%	1.6K 1%

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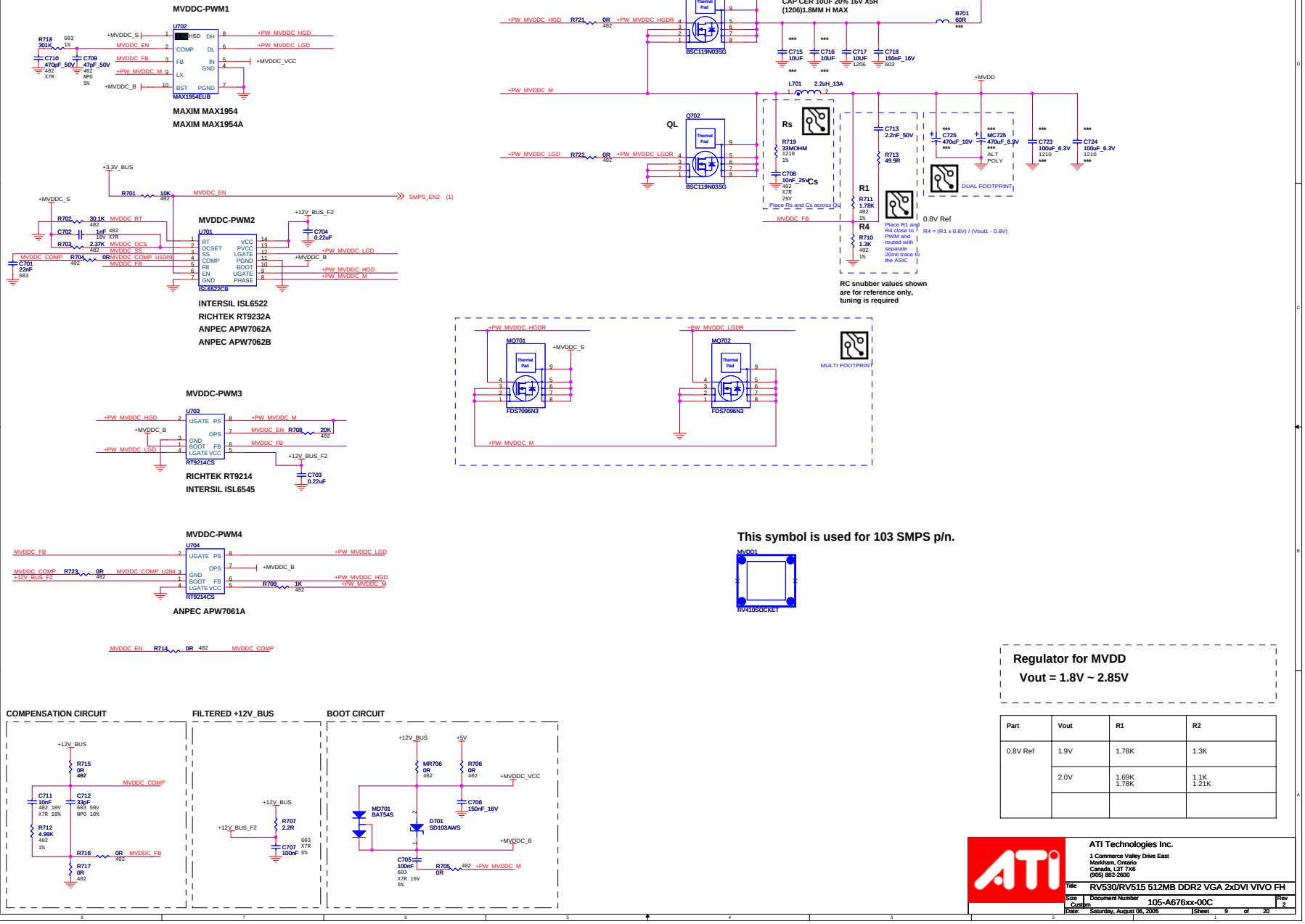

Part	Vout	R1	R2
0.8V Ref	1.9V	1.78K	1.3K
	2.0V	1.69K 1.78K	1.1K 1.21K

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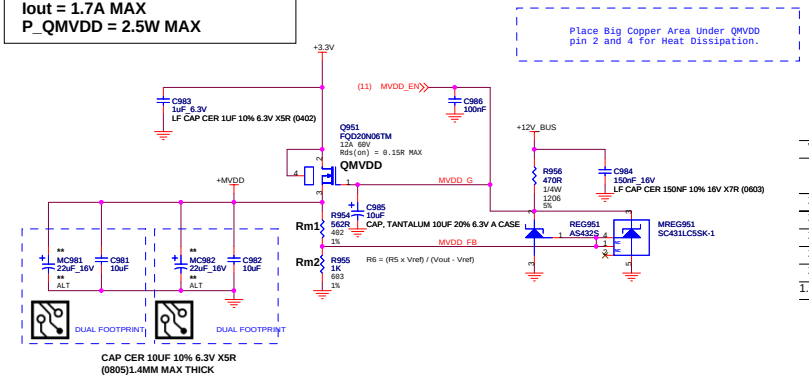
Regulator for +MVDDQ
Vout = 1.85V ~ 2.65V
Iout = 1.7A MAX
P_QMVDD = 2.5W MAX



Voltage Req.	Rm1		Rm2		
2.85V					
2.55V	22.1R	316022R100G	1.1K	3240110100G	2.5V Ref.
2.5V	0R	3150000000	DNI		2.5V Ref.
2.1V min	681R	3160681000G	953R	3240953000	1.24V Ref.
2.0V min	681R	3160681000G	1.1K	3240110100G	1.24V Ref.
1.9V min, 1.94V nom.	562R	3160562000G	1K	3160100100G	1.24V Ref.

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Alt regulator for +MPVDD
Vout = 1.2V (not tracking to VDDC)
Iout = 10mA MAX

Possible alternate 5150005600G

	Rt1		Rt2	
1.52V	432R	3240432000 3160432000	2.15K	3160215100
1.61V	432R	3240432000	1.5K 1.5K	3230015200 3160150100
1.69V	432R	3240432000	1.21K	3240121100
1.718V	562R	3240562000	1.5K 1.5K	3230015200 3160150100
1.75V	604R	3160604000	1.5K 1.5K	3230015200 3160150100
1.8V	604R	3160604000	1.37K	3160137100

Optional regulator for +PCIE
Vout = 1.2V ~1.25V
Iout = 1.2A MAX

CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

Supported footprint:
RT9173C/RT9199A/RT9199
APL5331

RT9199 p/n 2480054800G (480mR RdsON Max)
RT9199A (300mR RdsON Max)
RT9173C (250mR RdsON Max)
APL5331 p/n 2480054200G (350mR MAX for 2A)

Optional regulator for +2.5V
Vout = 2.5V
Iout = 600mA MAX

CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

Supported footprint:
RT9173C/RT9199A/RT9199
APL5331

Place caps very close to power pin

CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

~ 2.5V Drop MAX
200mW MAX
1/4 W

270mW MAX for 60mA

CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX

Optional Regulator for +VDDC_CT
Vout = 2.5V ~ 2.85V
Iout = 100mA MAX

CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

Supported footprint:
RT9173C/RT9199A/RT9199
APL5331

Req = 120.7R
Use 845R, 1206, 1/4W

CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX

Multi-footprint

Req = 120.7R
Use 845R, 1206, 1/4W

CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX

Multi-footprint

Req ~= 0.78R
Vdrop_max = 0.95V @ 1.2A
+PCIE_SOURCE ~= 2.35V
For 1.2A, each resistor (250mW rated) dissipates 0.2A or 190mW

Possible alternate 5150005600G

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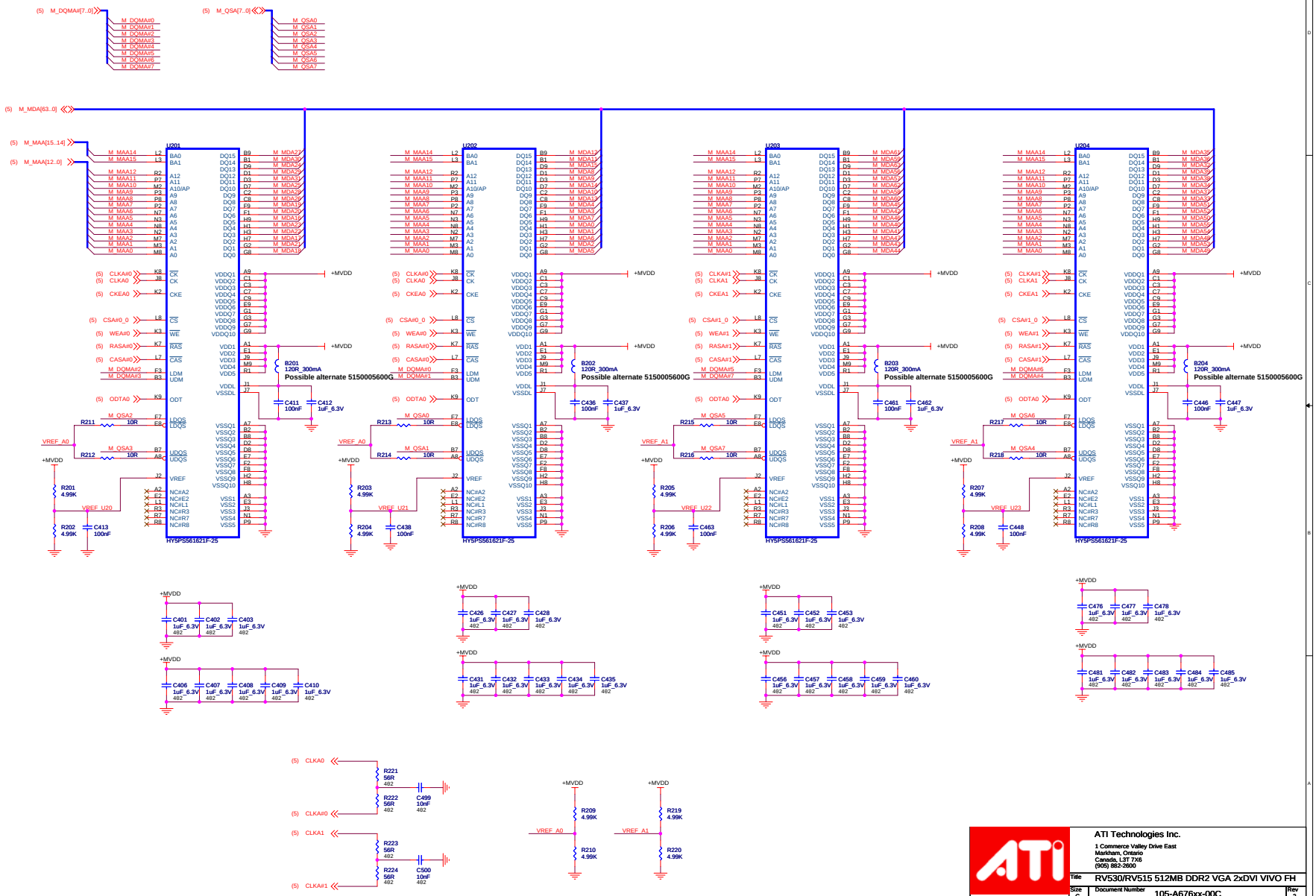
CHANNEL A: RANK 0 128MB DDR2



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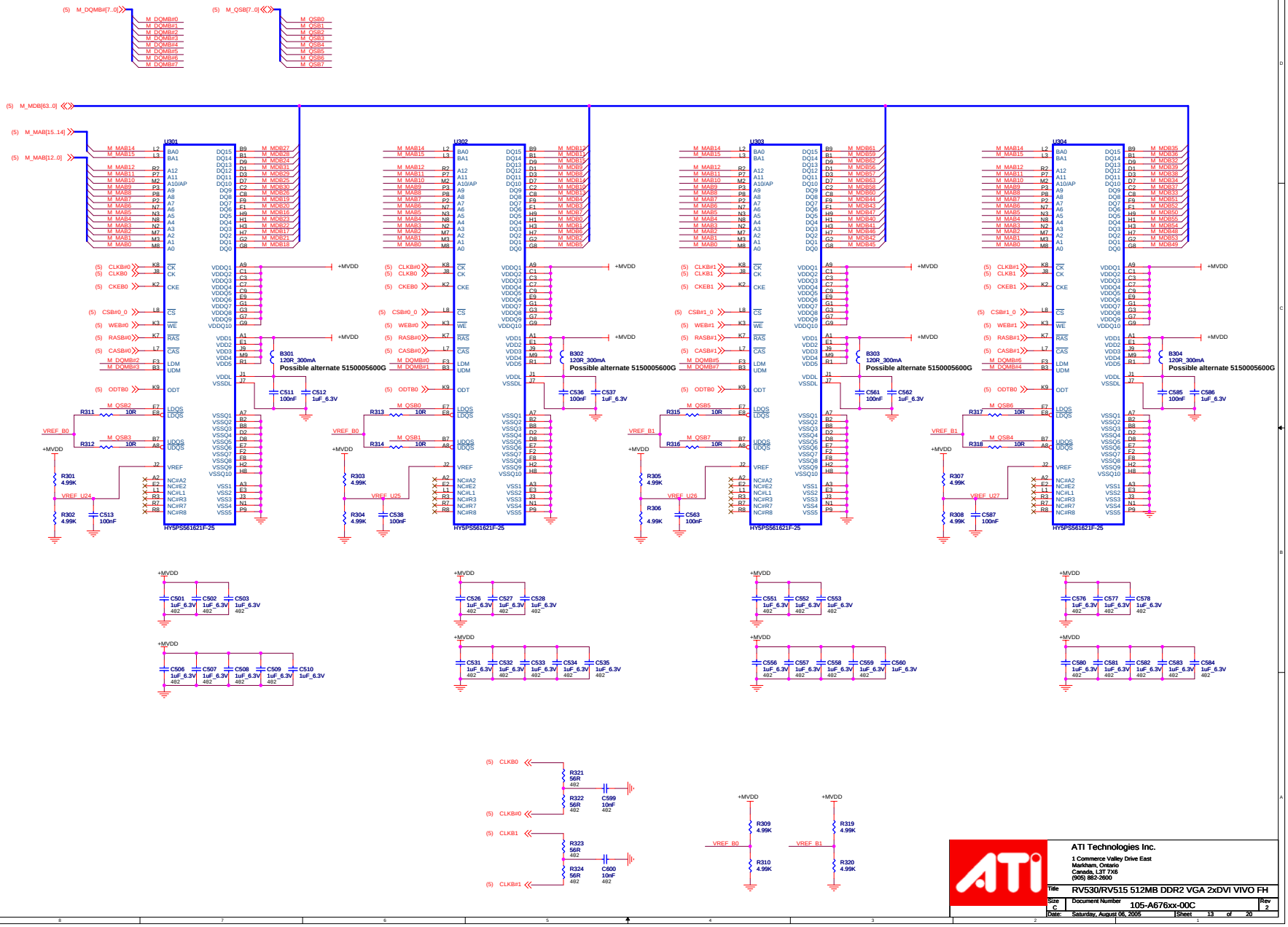
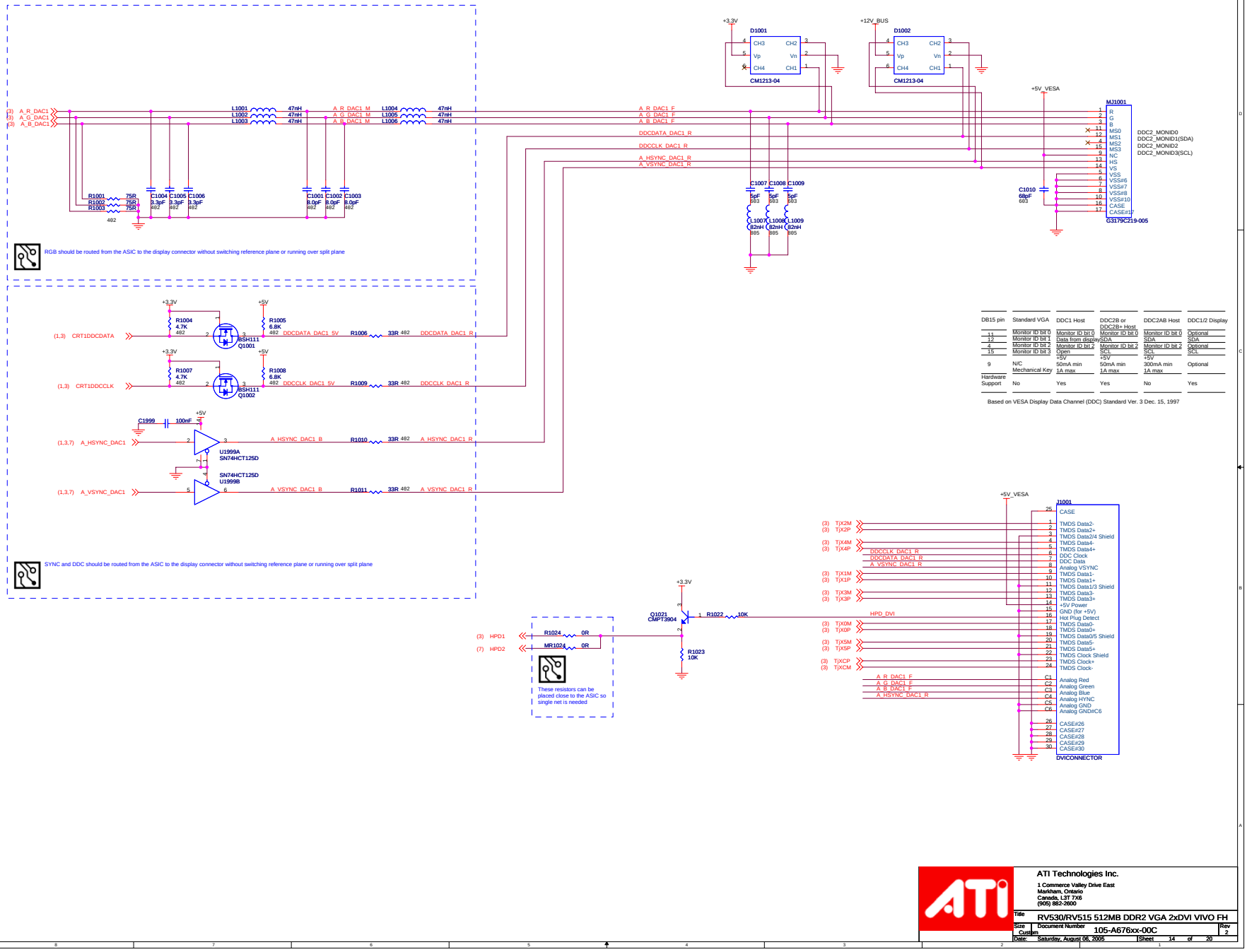
CHANNEL B: RANK 0 128MB DDR2





DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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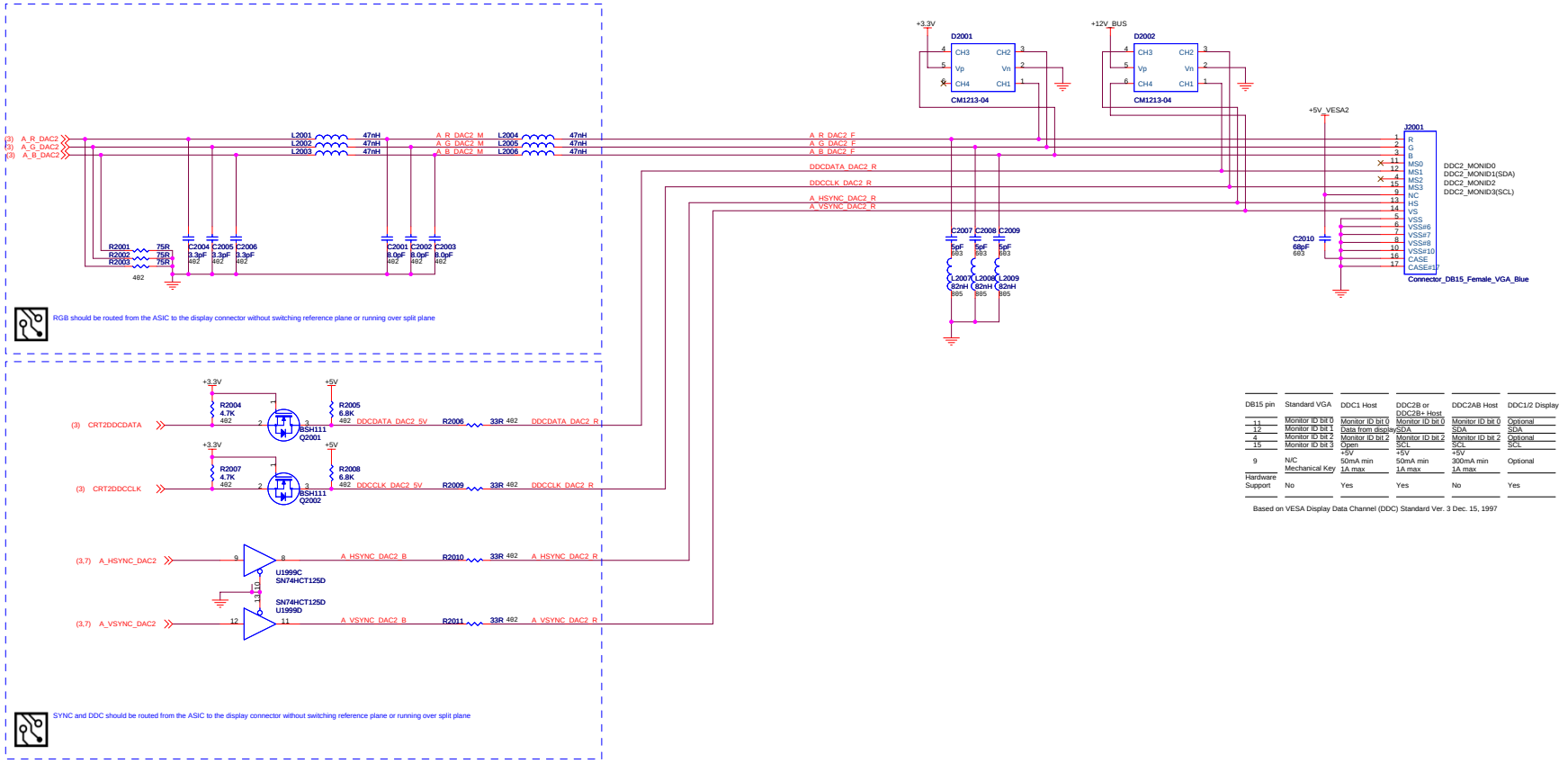

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V	+5V	+5V	Optional
	Mechanical Key	50mA min	50mA min	300mA min	
Hardware Support		1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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+RTAVDD
Vout = 3.3V
Iout = 125mA MAX, 80mA RMS

These capacitors are for clossing references

Overlap with Rpin5

TV Out

Place near connector
0R leaves footprint for Ferrite Beads if req'd for EMI

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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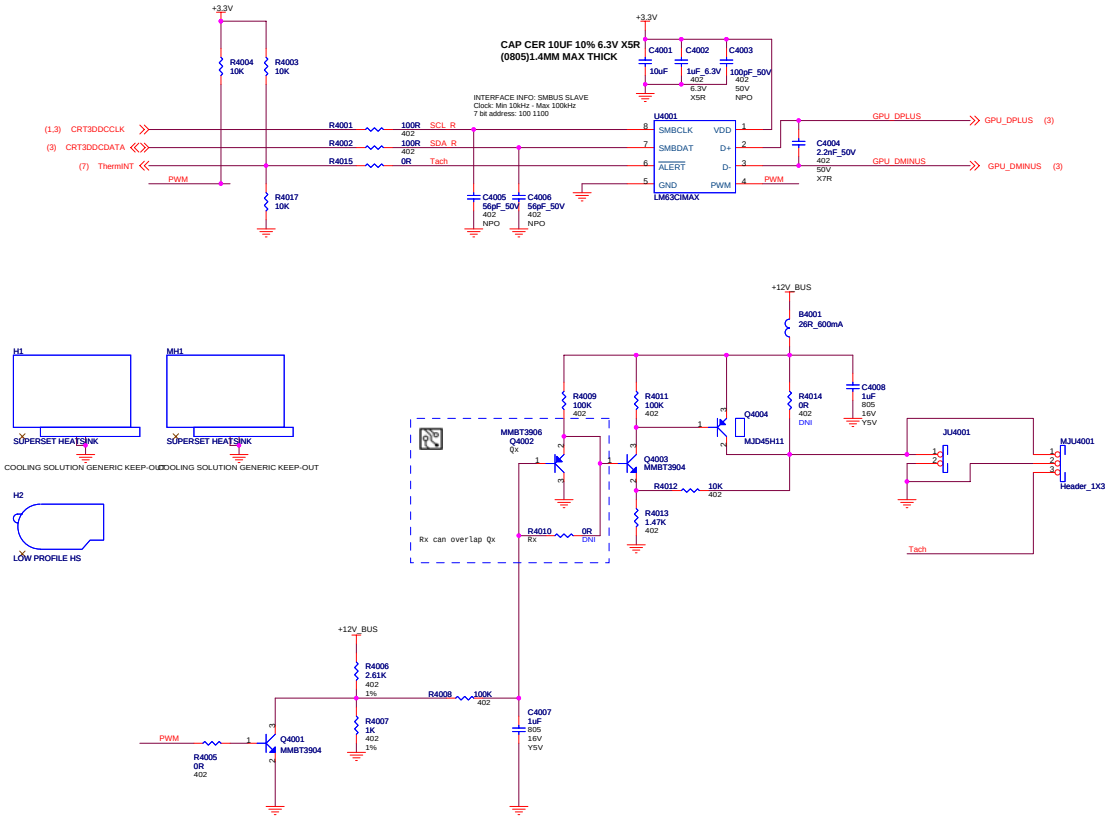

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DVI/VGA SCREWS

ASSY-SCREW1
SCREW
JACKSCREW
ASSY
7020000800

ASSY-SCREW2
SCREW
JACKSCREW
ASSY
7020000800

ASSY-SCREW5
SCREW
PAN_HEAD
7020001700

ASSY-SCREW3
SCREW
JACKSCREW
ASSY
7020000800

ASSY-SCREW4
SCREW
JACKSCREW
ASSY
7020000800

MT1
MT_Hole_0.136_in.
DNI

MT2
MT_Hole_0.136_in_6VIA
DNI

DNI

SK1

RV410SOCKET

PCB1

RV410SOCKET

<Variant Name>

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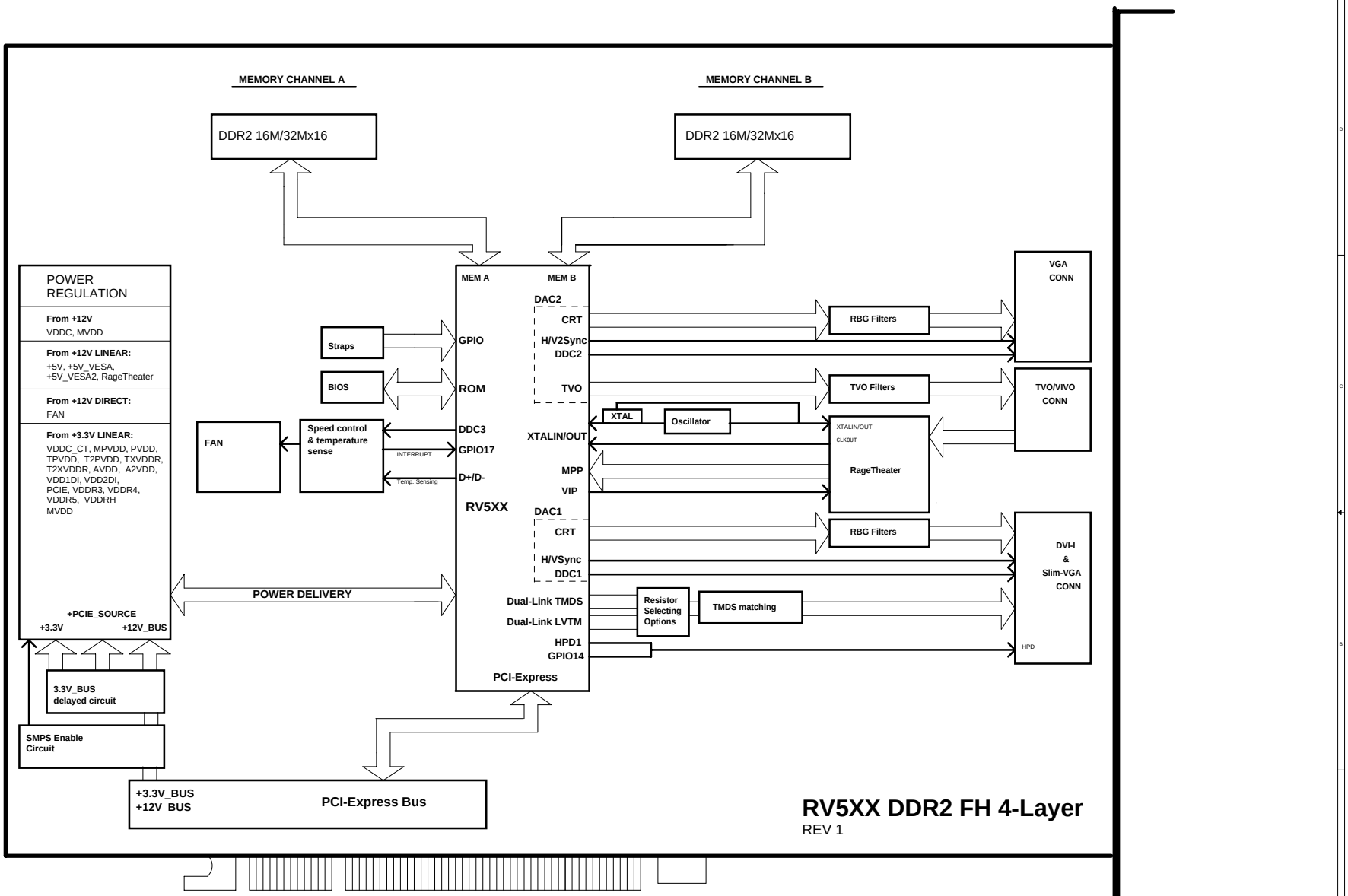
<variant_name>

Title	Schematic No.	Date:
RV530/RV515 512MB DDR2 VGA 2xDVI VIVO FH	105-A676xx-00C	**Saturday, August 06, 2005**

REVISION HISTORY

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	05/05/01	New design from scratch
1	00B	05/07/14	(Layout) Critical layout change (L1) Reduce +PW_MVDDC_M planes and replace it with GND (L1) Correct silkscreen "SMPS A601-00A TILE" (L3) Replace +PW_VDDC_M, +VDDC_S and +MVDDC_S planes with GND (pg 01) Correct clock circuitry to support RT (pg 08) Swap R603 and R604 to match layout for documentation purposes (pg 09) Swap R703 and R704 to match layout for documentation purposes (pg 10) Add MVDD linear regulator option (pg 11) Add R986, R987, R988; replace redundant power sequence circuit with +5V_EN and MVDD_EN (pg 11) Add MR911, R918 for +MPVDD for no-tracking option (pg 16) Change C3103 to 603 footprint, change RT to power from 3.3V_BUS to avoid leakage, remove redundant RT clock resistors
2	00C	05/07/29	(Layout) Critical layout change Add 2 to 3 more power vias for MOSFET source pin of VDDC (L3) Remove ground planes under the PWM IC Remove +MVDDC/+MVDDQ reference, use only +MVDD



RV5XX DDR2 FH 4-Layer

REV 1

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