PG142-B00

DP + DP + DP + HDMI/DP

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<Variant Name>

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<OrgName>	**Engineer:** **Water**	
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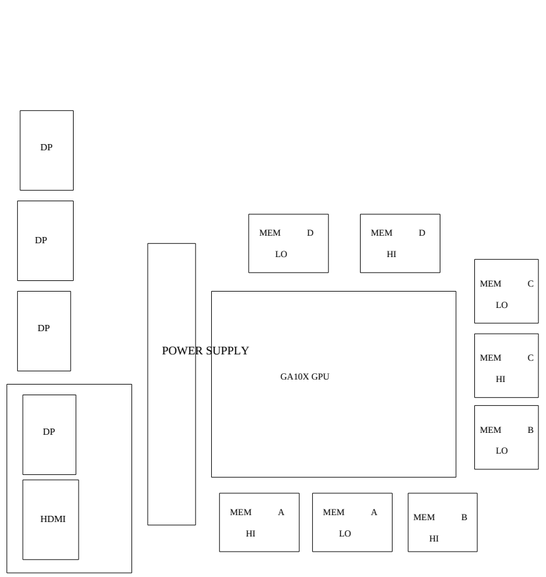
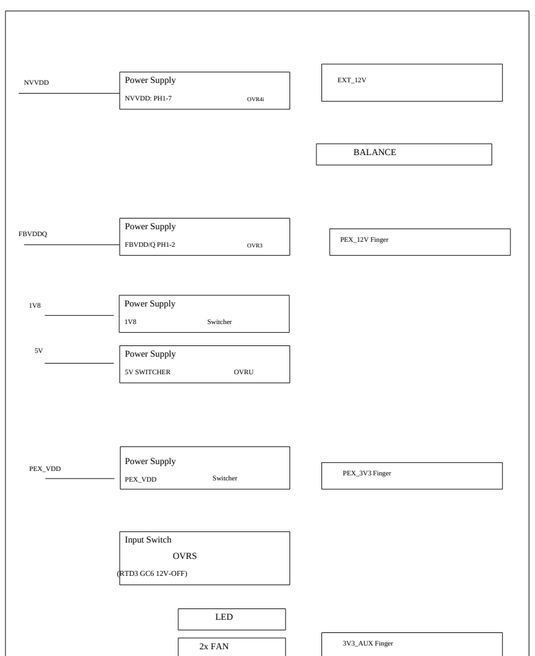
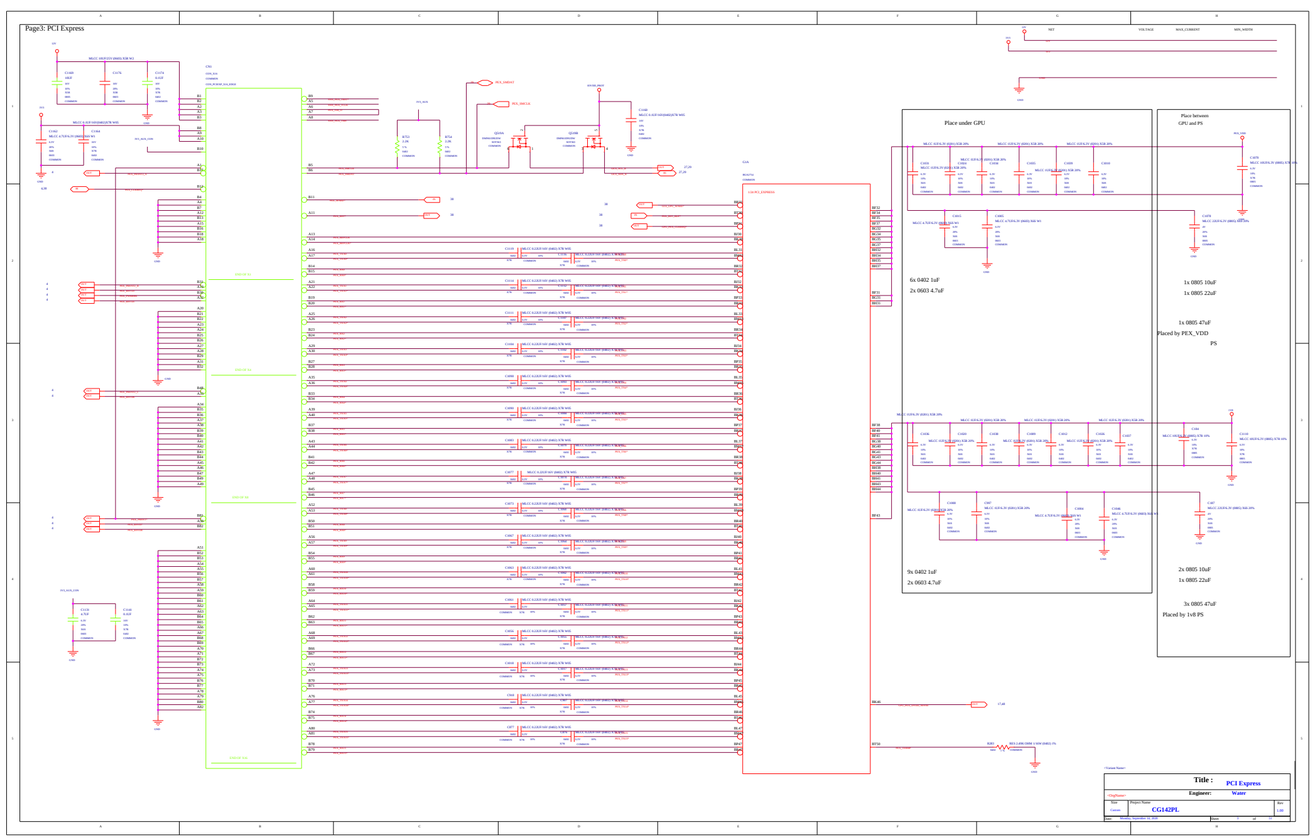
Page2: Block Diagram






Page3: PCI Express
Place under GPU
Place between GPU and PS
6x 0402 1uF
2x 0603 4.7uF
1x 0805 10uF
1x 0805 22uF
1x 0805 47uF
Placed by PEX_VDD
PS
9x 0402 1uF
2x 0603 4.7uF
2x 0805 10uF
1x 0805 22uF
3x 0805 47uF
Placed by 1v8 PS
Title : PCI Express
Engineer: Water
CG142PL

Page4: PCIE GEN4 RC TERMINATIONS


3,38 IN PEX_CLKREQ* C1140 MLCC 1PF/50V (0402) NP0 W05 0402 50V 0.25pF C0G COMMON PEX_CLKREQ_RC* R749 RES 40.2 OHM 1/16W (0402) 1% 0402 1 % COMMON GND
PLACE CLOSE TO B12
3 IN PEX_PRSNT2_A C1136 MLCC 1PF/50V (0402) NP0 W05 0402 50V 0.25pF C0G COMMON PEX_PRSNT2_A_RC R748 RES 40.2 OHM 1/16W (0402) 1% 0402 1 % COMMON GND
PLACE CLOSE TO B17
3 IN PEX_PWRBRK C832 MLCC 1PF/50V (0402) NP0 W05 0402 50V 0.25pF C0G COMMON PEX_PWRBRK_RC R695 RES 40.2 OHM 1/16W (0402) 1% 0402 1 % COMMON GND
3 IN PEX_PRSNT2_B C808 MLCC 1PF/50V (0402) NP0 W05 0402 50V 0.25pF C0G COMMON PEX_PRSNT2_B_RC R693 RES 40.2 OHM 1/16W (0402) 1% 0402 1 % COMMON GND
3 IN PEX_PRSNT2_C C749 MLCC 1PF/50V (0402) NP0 W05 0402 50V 0.25pF C0G COMMON PEX_PRSNT2_C_RC R680 RES 40.2 OHM 1/16W (0402) 1% 0402 1 % COMMON GND
PLACE CLOSE TO B81
3 IN PEX_PRSNT* C297 MLCC 1PF/50V (0402) NP0 W05 0402 50V 0.25pF C0G COMMON R331 RES 40.2 OHM 1/16W (0402) 1% 0402 1 % COMMON GND
3 IN PEX_RSVD8 C298 MLCC 1PF/50V (0402) NP0 W05 0402 50V 0.25pF C0G COMMON PEX_RSVD8_RC R332 RES 40.2 OHM 1/16W (0402) 1% 0402 1 % COMMON GND
3 IN PEX_RSVD3 C1129 MLCC 1PF/50V (0402) NP0 W05 0402 50V 0.25pF C0G COMMON PEX_RSVD3_RC R747 RES 40.2 OHM 1/16W (0402) 1% 0402 1 % COMMON GND
3 IN PEX_RSVD5 C783 MLCC 1PF/50V (0402) NP0 W05 0402 50V 0.25pF C0G COMMON R687 RES 40.2 OHM 1/16W (0402) 1% 0402 1 % COMMON GND
3 IN PEX_RSVD6 C772 MLCC 1PF/50V (0402) NP0 W05 0402 50V 0.25pF C0G COMMON R683 RES 40.2 OHM 1/16W (0402) 1% 0402 1 % COMMON GND
3 IN PEX_RSVD7 C723 MLCC 1PF/50V (0402) NP0 W05 0402 50V 0.25pF C0G COMMON PEX_RSVD7_RC R677 RES 40.2 OHM 1/16W (0402) 1% 0402 1 % COMMON GND

<Variant Name>

Title : PCIE GEN4 RC TERMINATIONS

<OrgName> Engineer: Water

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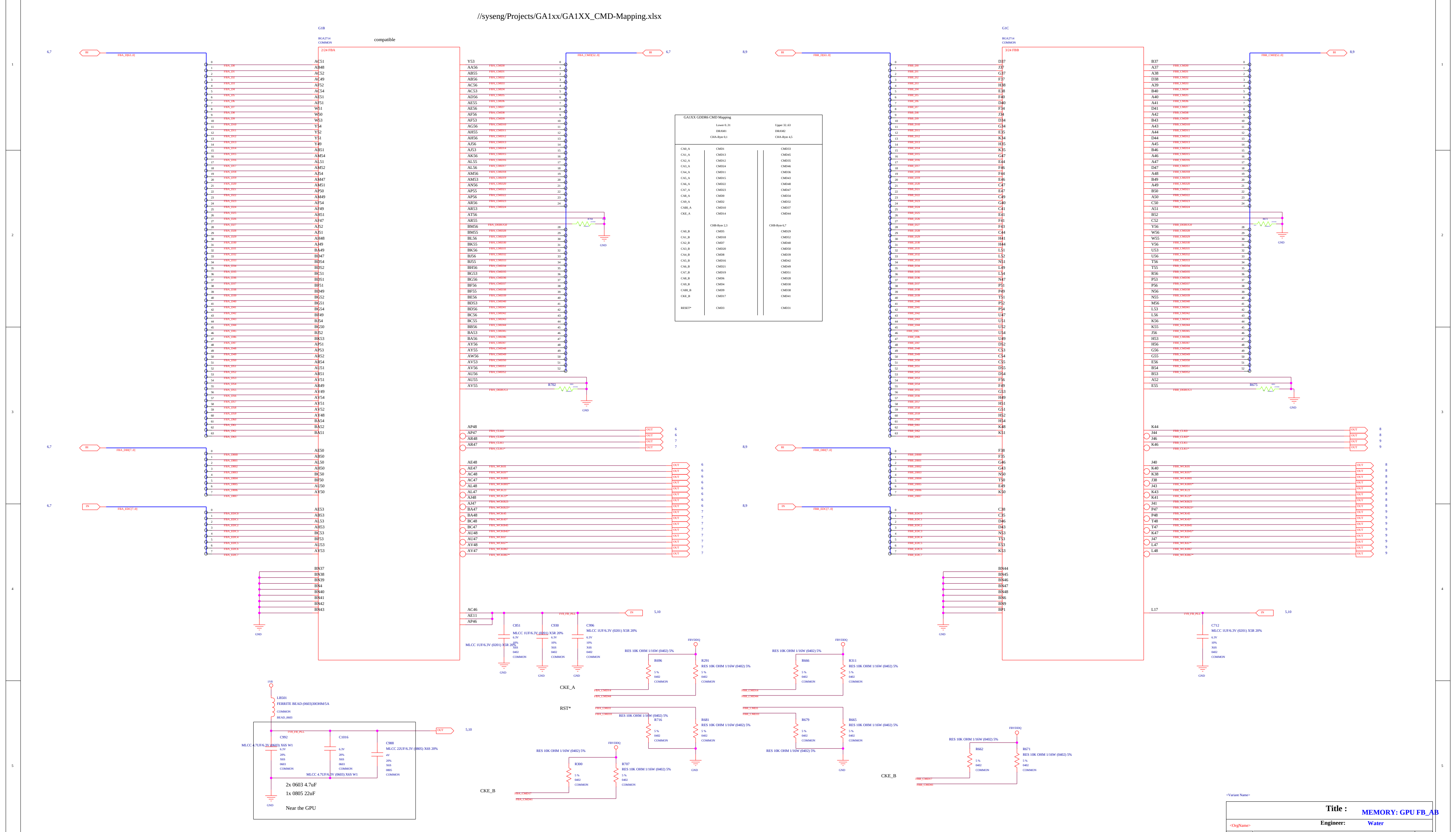
Page5: MEMORY: GPU Partition A/B

//syseng/Projects/GA1xx/GA1XX_CMD-Mapping.xlsx



<Variant Name>

Title : MEMORY: GPU FB_AB		
<OrgName> Engineer: Water		
Size: Custom	Project Name: CG142PL	Rev: 1.00
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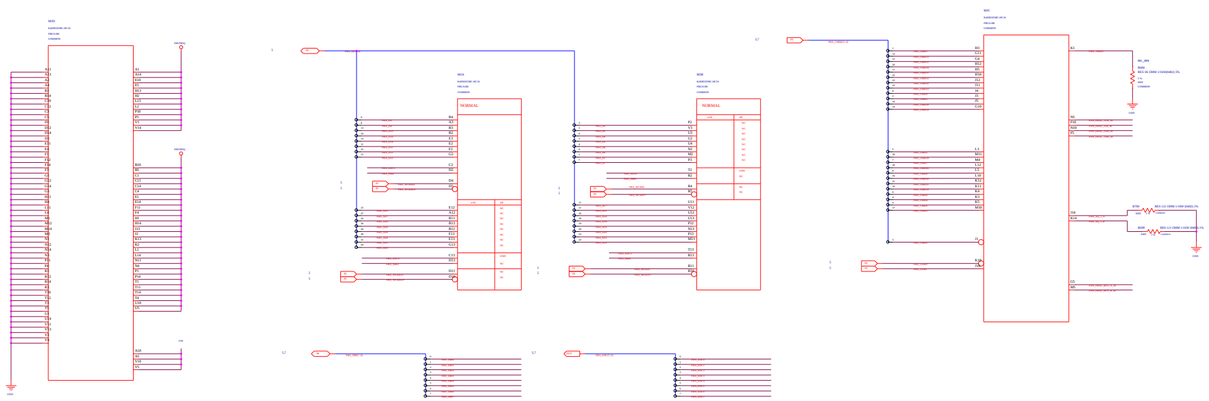
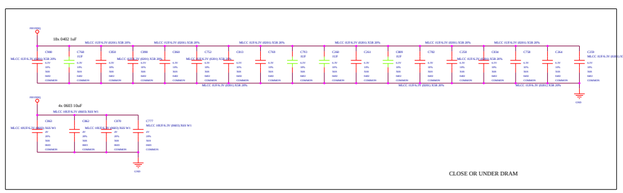
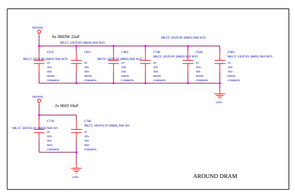
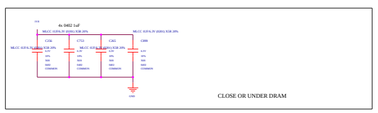
Page6: MEMORY: FBA Partition 31..0



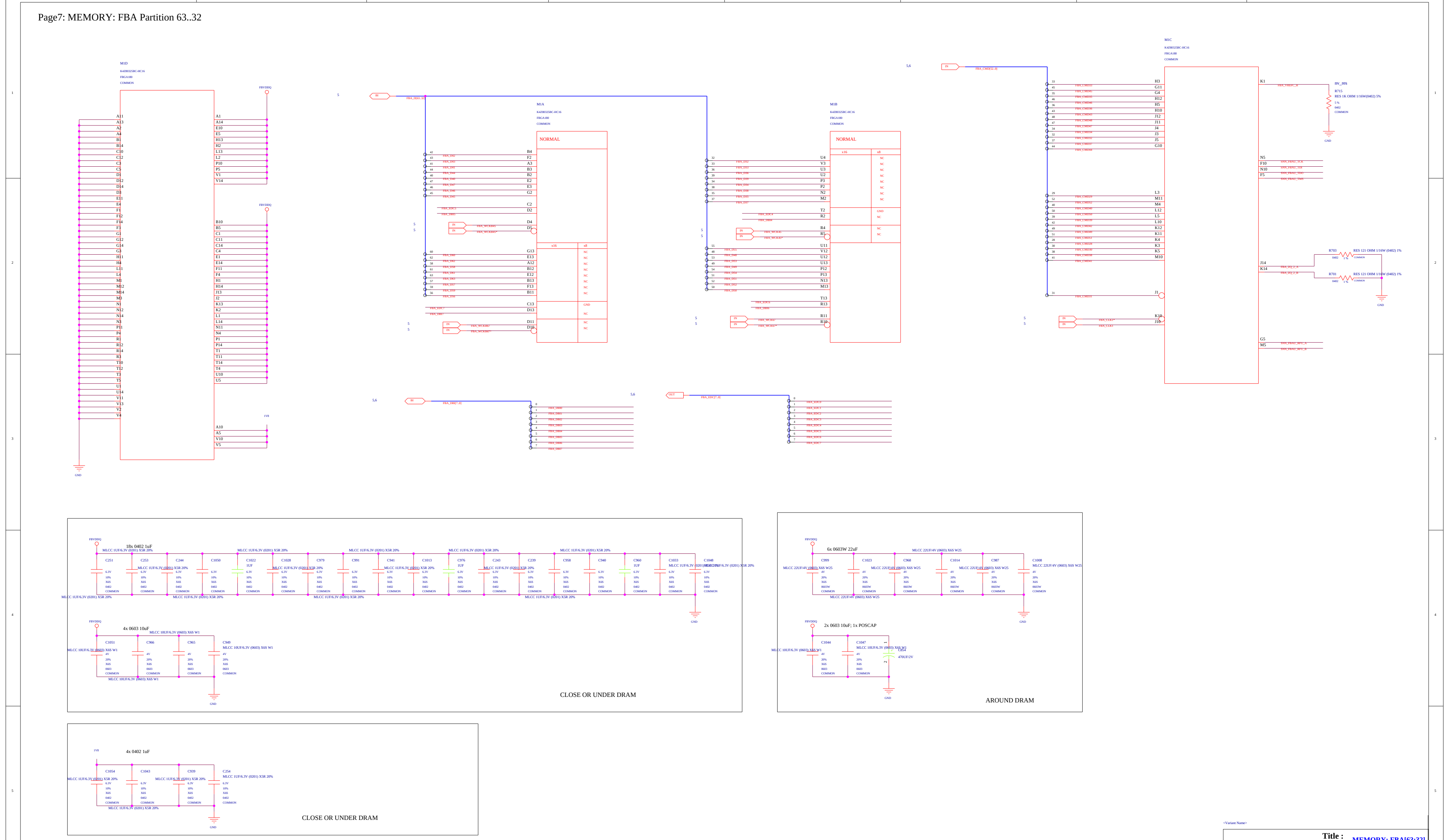
decap via : at least 2 gnd vias and 2 power vias for each cap







Title : MEMORY: FBA[31:0]
Engineer: Water
Project Name:
CG142PL



<Variant Name>

		Title :	**MEMORY: FBA[63:32]**
<OrgName>		**Engineer:**	**Water**
Size: Custom	Project Name: **CG142PL**		Rev: 1.00
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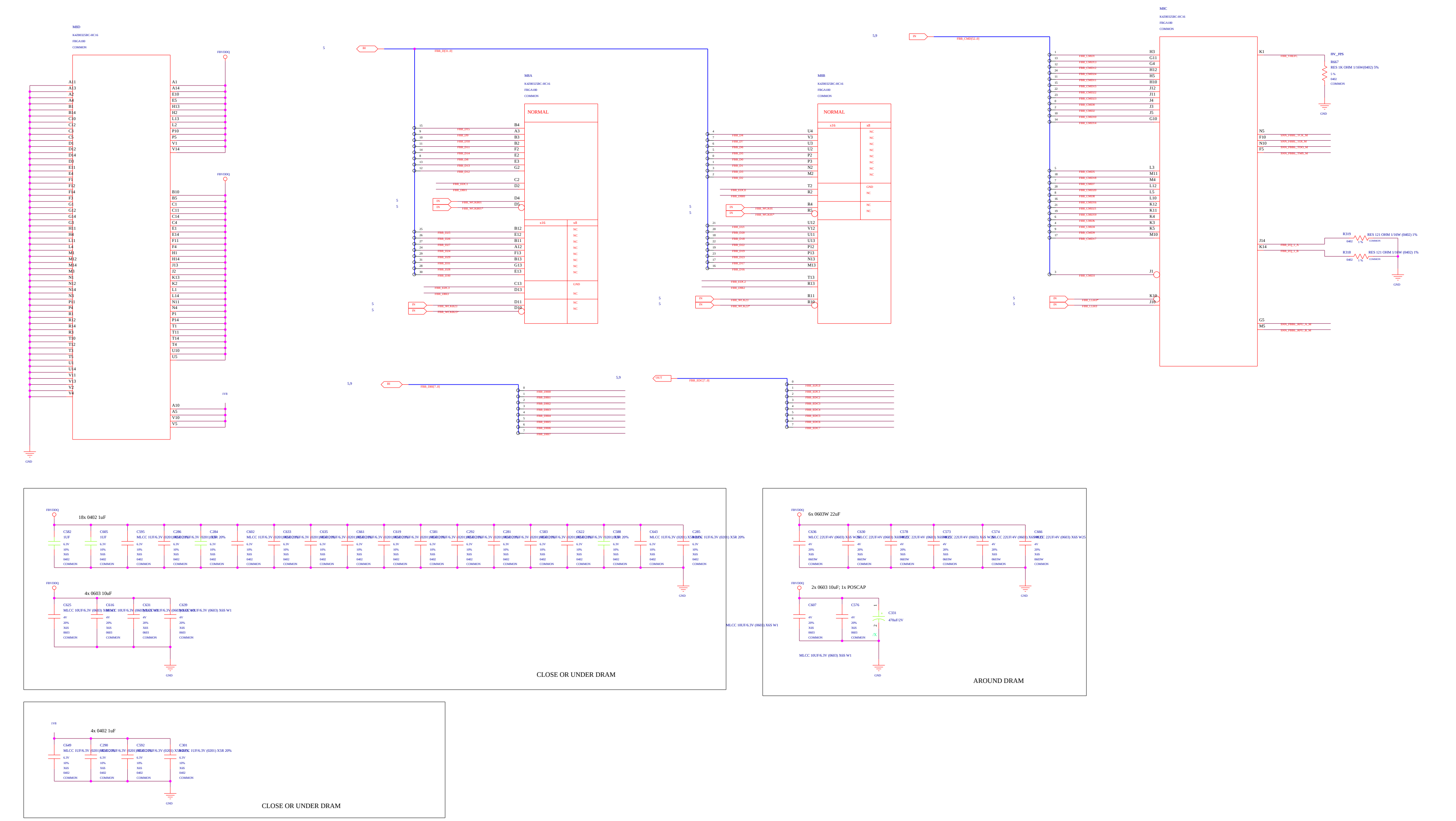
Page8: MEMORY: FBB Partition 31..0



<Variant Name>

	Title :	MEMORY: FBB[31:0]	
<OrgName>	Engineer:	Water	
Size: Custom	Project Name: CG142PL		Rev: 1.00
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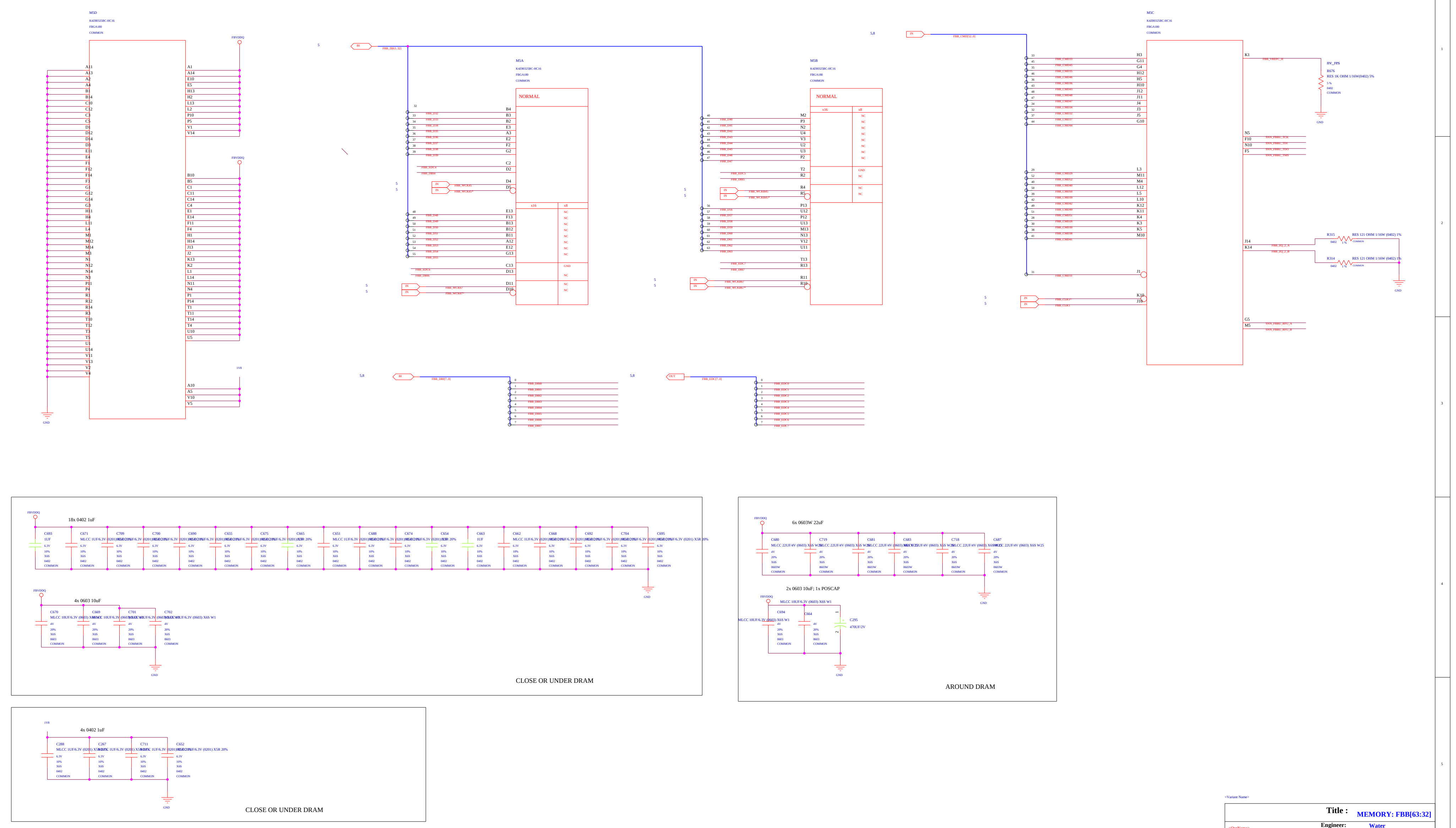
Page9: MEMORY: FBB Partition 63..32



<Variant Name>

Title : MEMORY: FBB[63:32]		
<OrgName>	Engineer: Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
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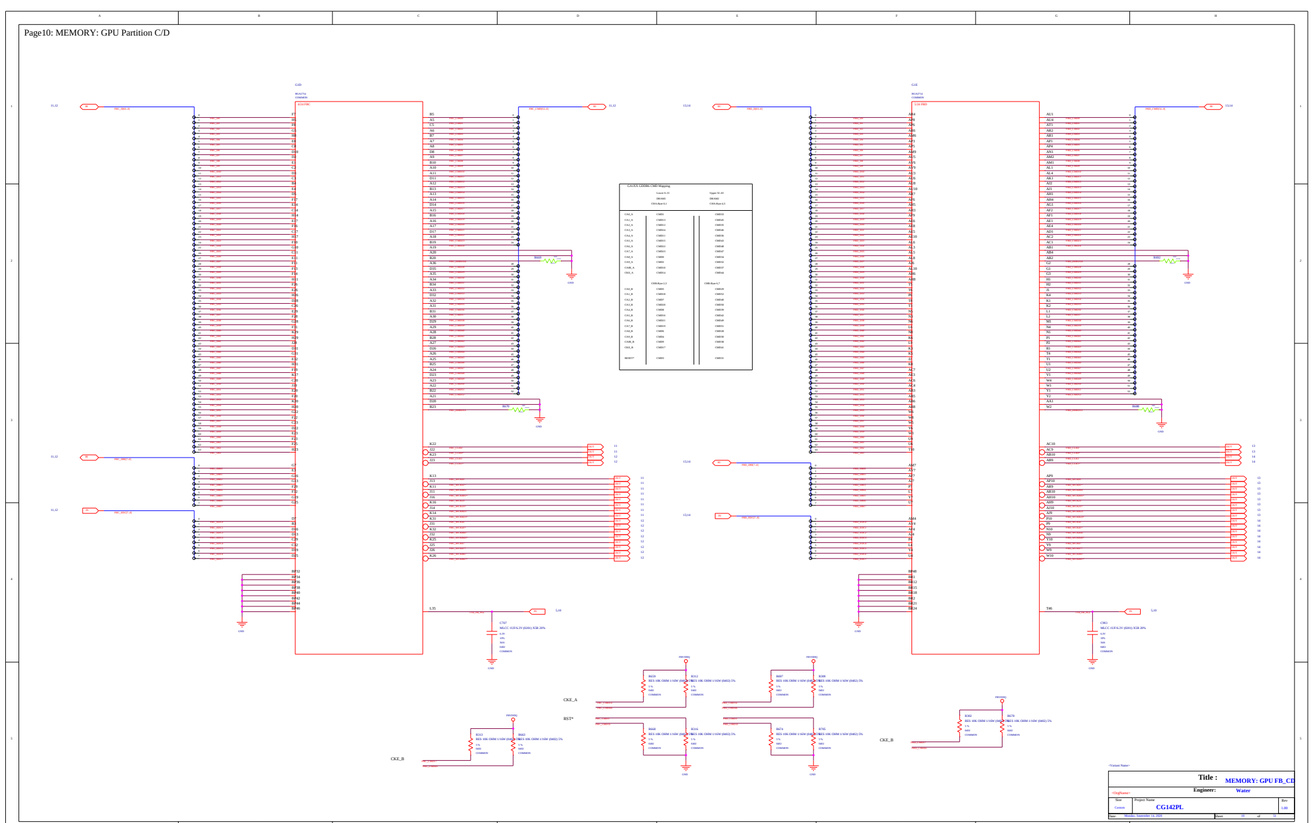
Page10: MEMORY: GPU Partition C/D

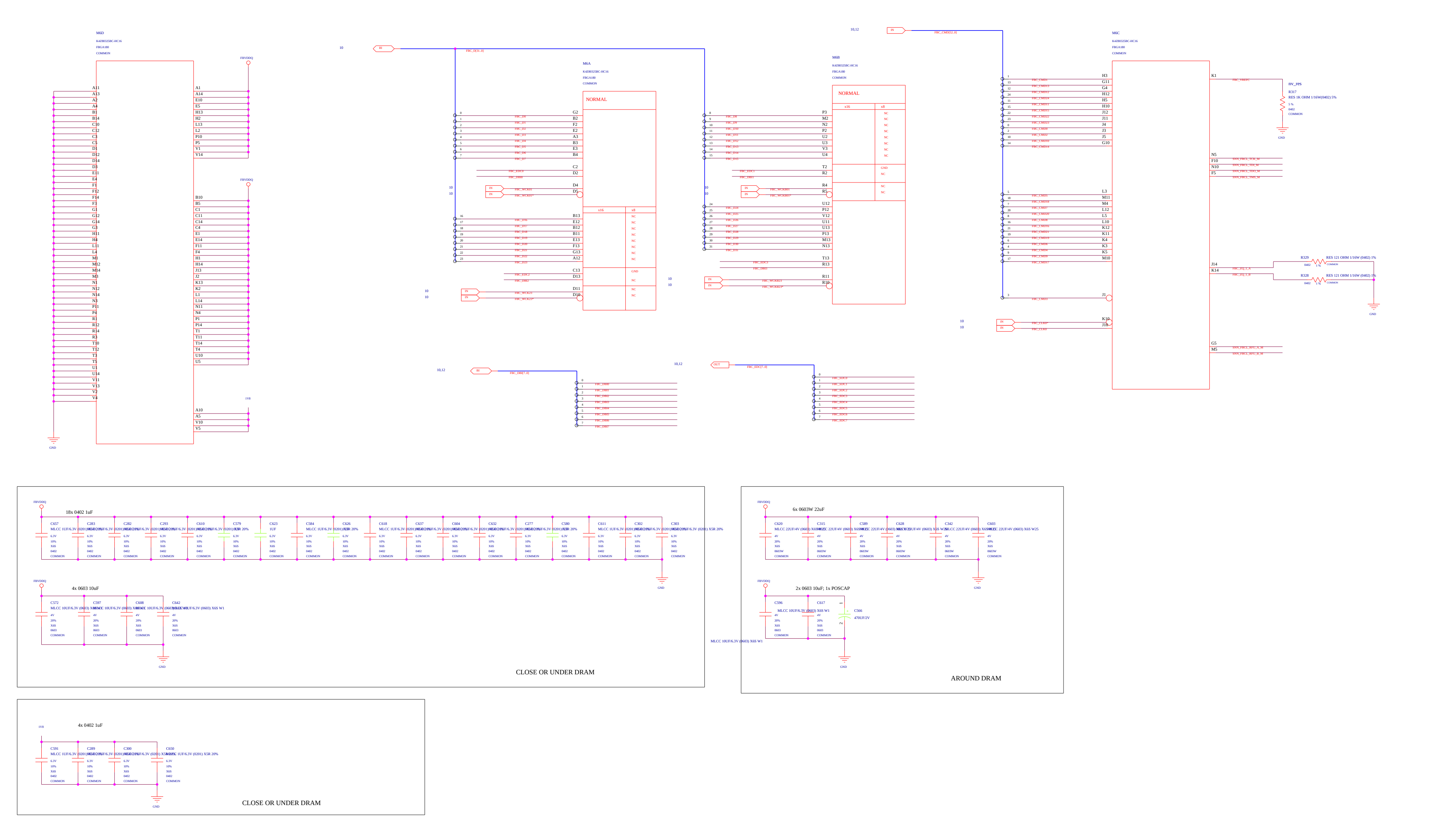


Title : MEMORY: GPU FB_CD

Engineer: Water

CG142PL

Page11: MEMORY: FBC Partition 31..0



<Variant Name>

Title :	MEMORY: FBC[31:0]	
<OrgName>	Engineer: Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
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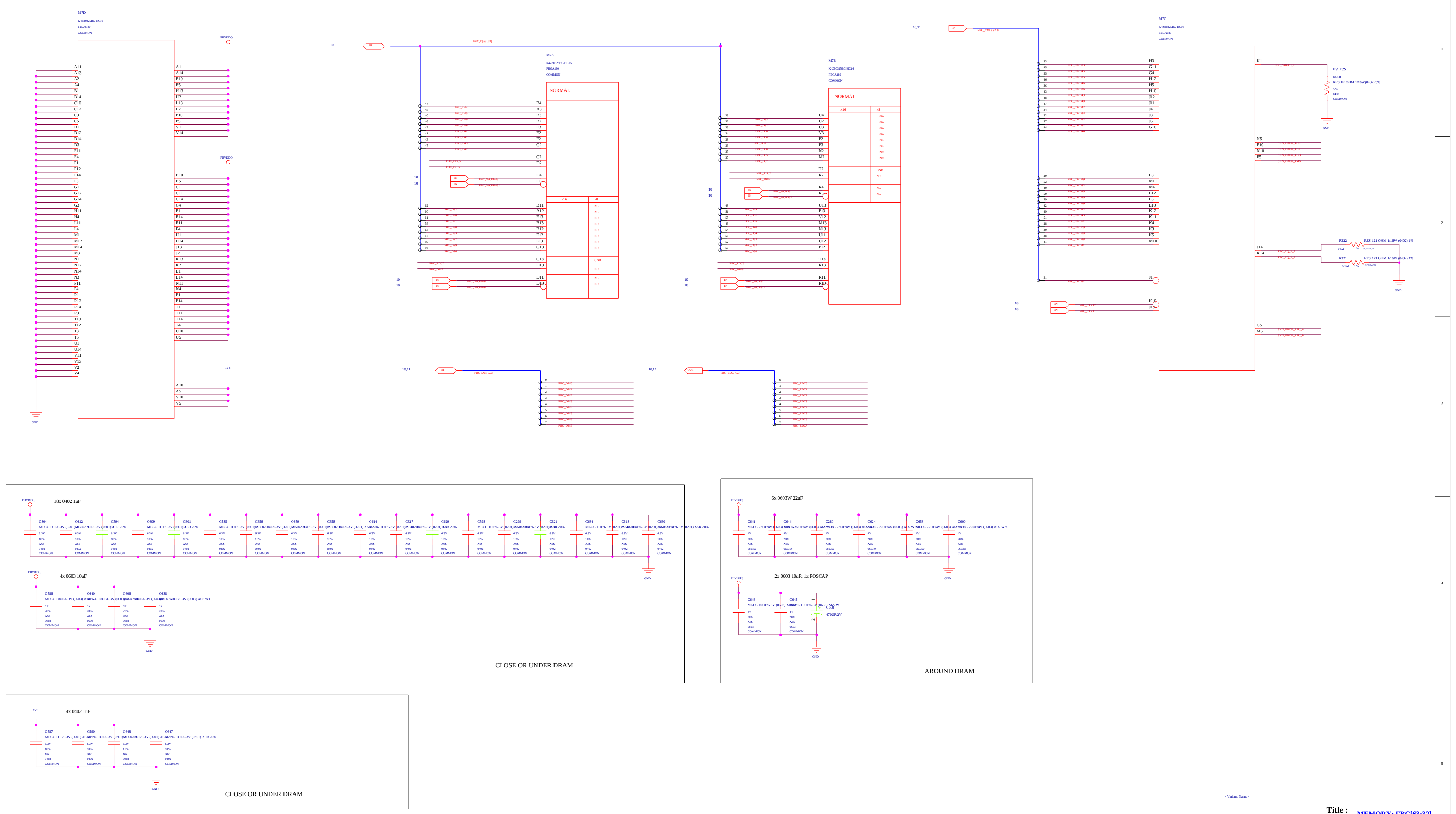
Page12: MEMORY: FBC Partition 63..32



<Variant Name>

Title : MEMORY: FBC[63:32]		
<OrgName>	Engineer: Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
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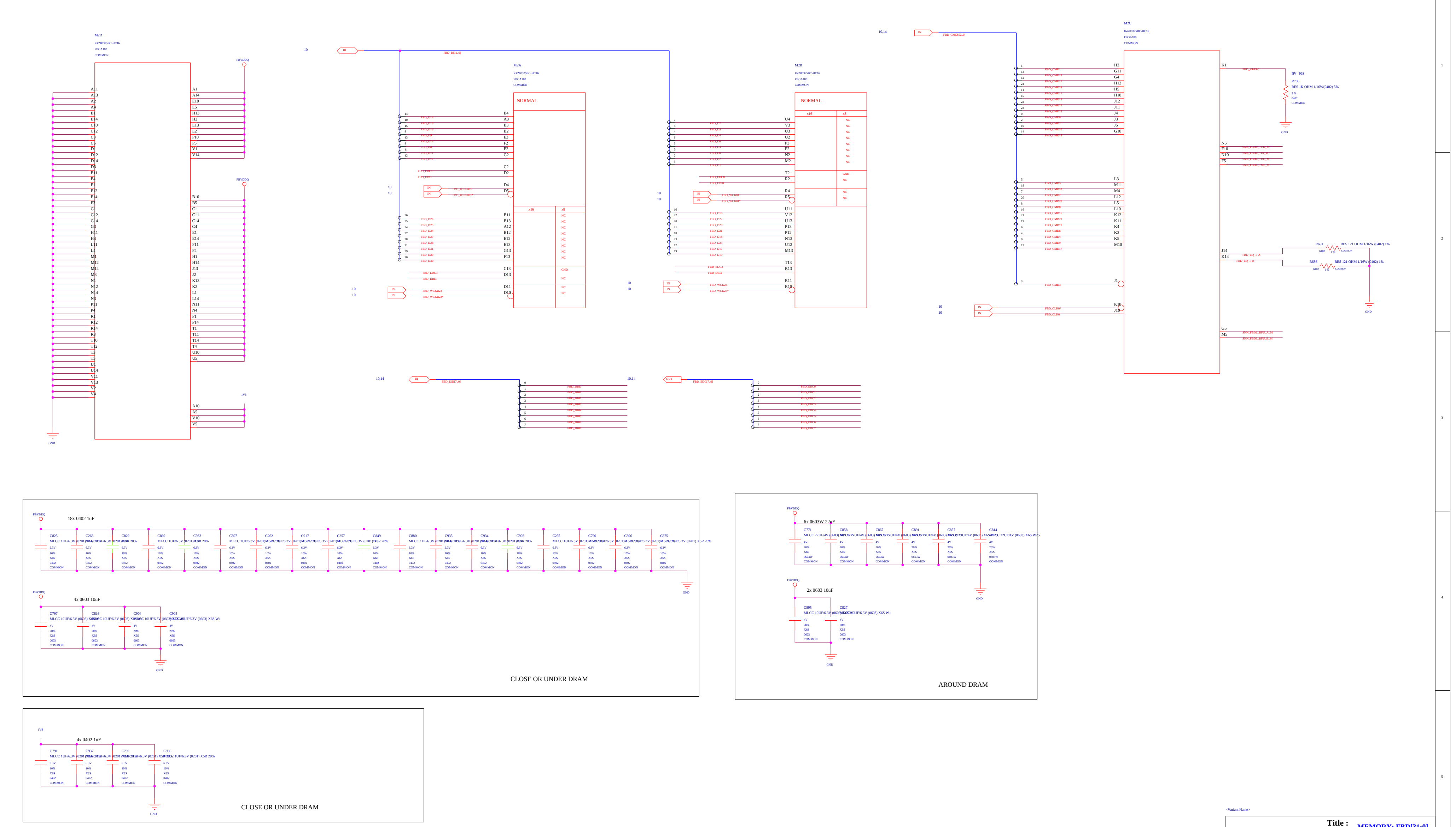
Page13: MEMORY: FBD Partition 31..0



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Title : MEMORY: FBD[31:0]		
<OrgName>	Engineer: Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
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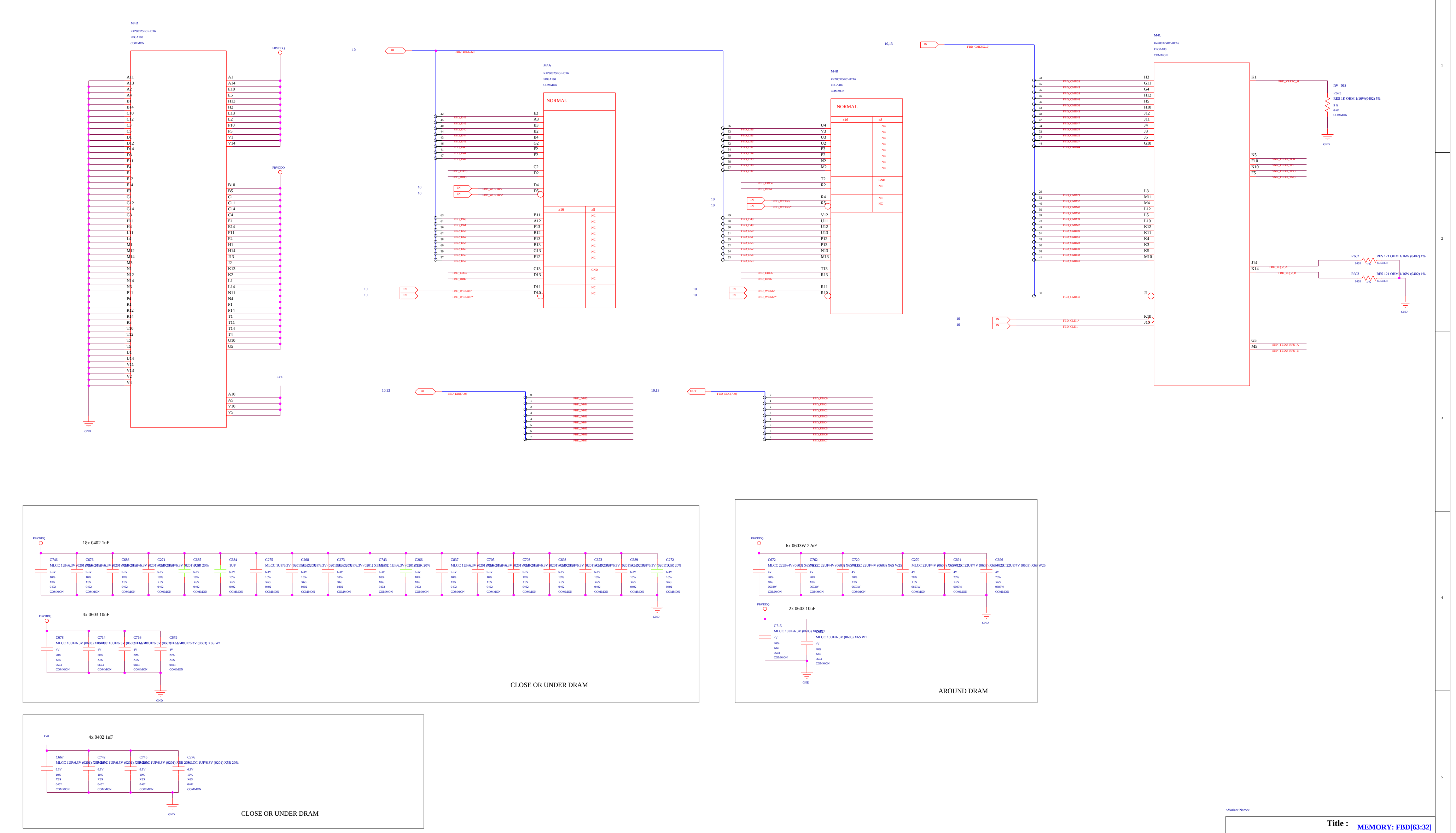
Page14: MEMORY: FBD Partition 63..32



<Variant Name>

Title :	**MEMORY: FBD[63:32]**	
<OrgName>	**Engineer:**	**Water**
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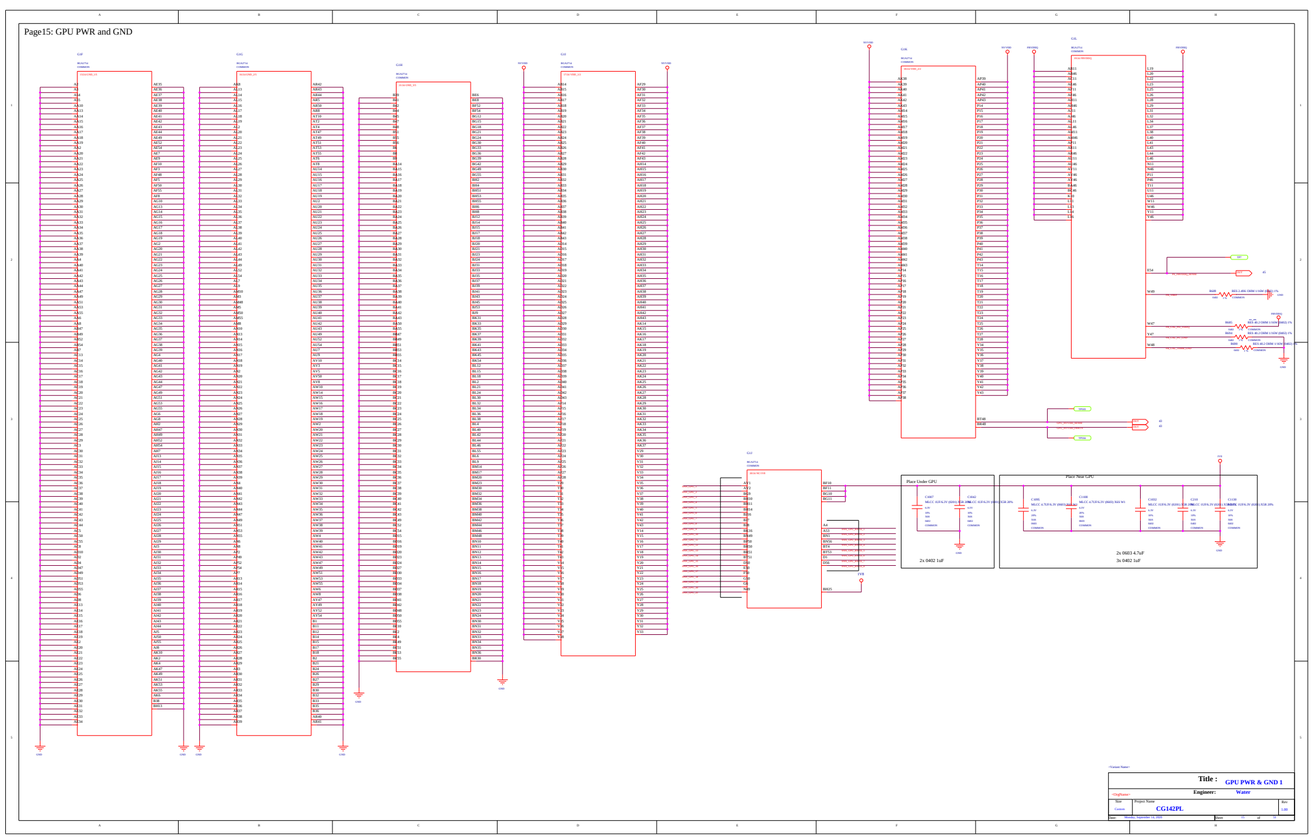
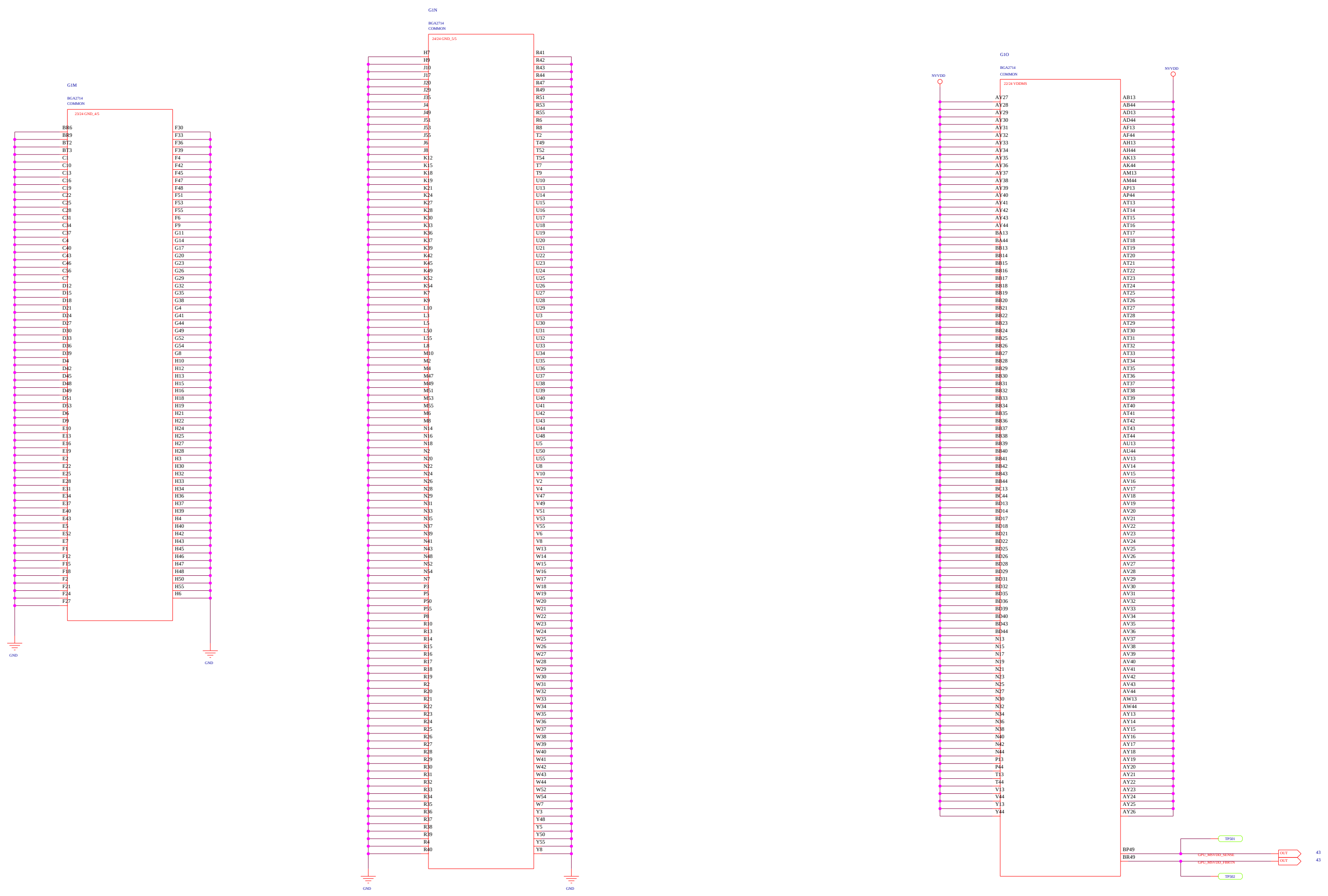
Page15: GPU PWR and GND



Page16: GPU PWR and GND 2



<Variant Name>

Title :	GPU PWR & GND 2		
<OrgName>	Engineer:	Water	
Size: Custom	Project Name: CG142PL		Rev: 1.00
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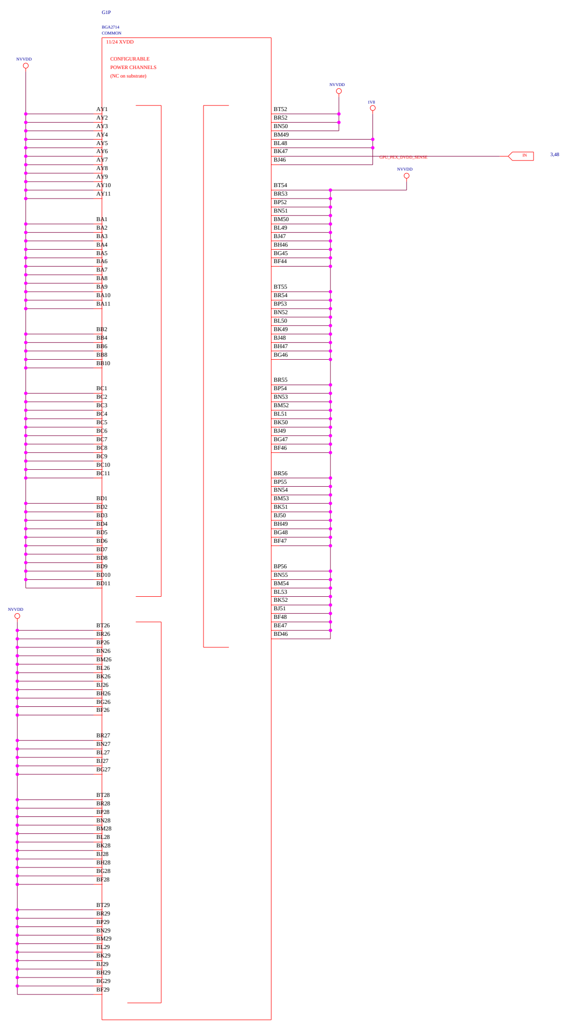
Page17: XVDD



<Variant Name>

Title : GPU PWR & GND 3 (XVDD)		
<OrgName>	Engineer: Water	
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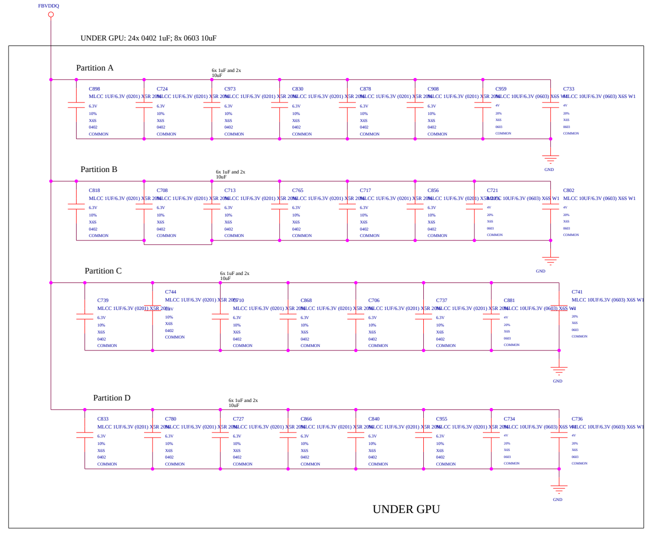
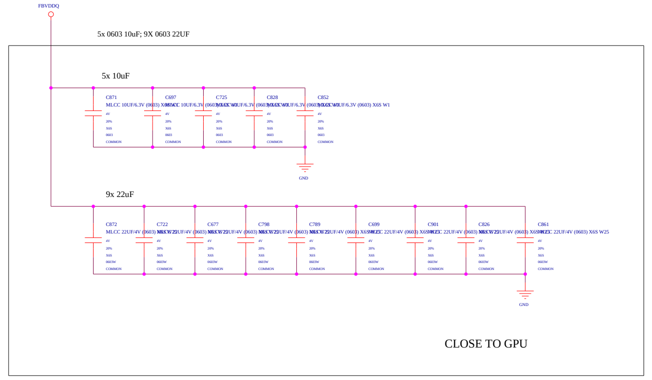
Page18: GPU DECOUPLING FBVDDQ

FBVDDQ

UNDER GPU: 24x 0402 1uF; 8x 0603 10uF


FBVDDQ
Partition A
6x 1uF and 2x 10uF
C898 C724 C973 C830 C878 C908
MLCC 1UF/6.3V (0201) X5R 20%
6.3V 10% X6S 0402 COMMON
C959 C733
MLCC 10UF/6.3V (0603) X6S W1
4V 20% X6S 0603 COMMON
GND
Partition B
6x 1uF and 2x 10uF
C818 C708 C713 C765 C717 C856
C721 C802
GND
Partition C
6x 1uF and 2x 10uF
C739 C744 C710 C868 C706 C737
C881 C741
GND
Partition D
6x 1uF and 2x 10uF
C833 C780 C727 C866 C840 C955
C734 C736
GND
UNDER GPU

5x 0603 10uF; 9X 0603 22UF



<Variant Name>

Title : GPU DECOUPLING FBVDDQ		
<OrgName>	**Engineer:** Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
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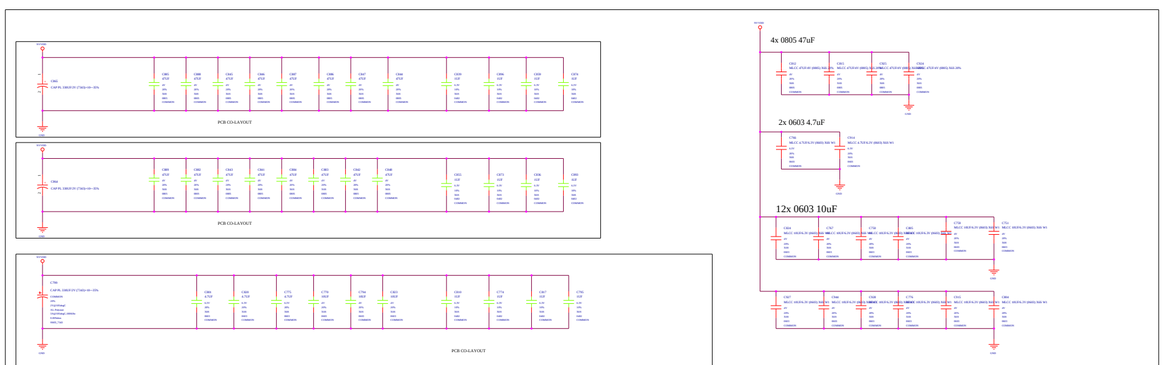
Page19: GPU DECOUPLING NVVDD



4x 0805 47uF

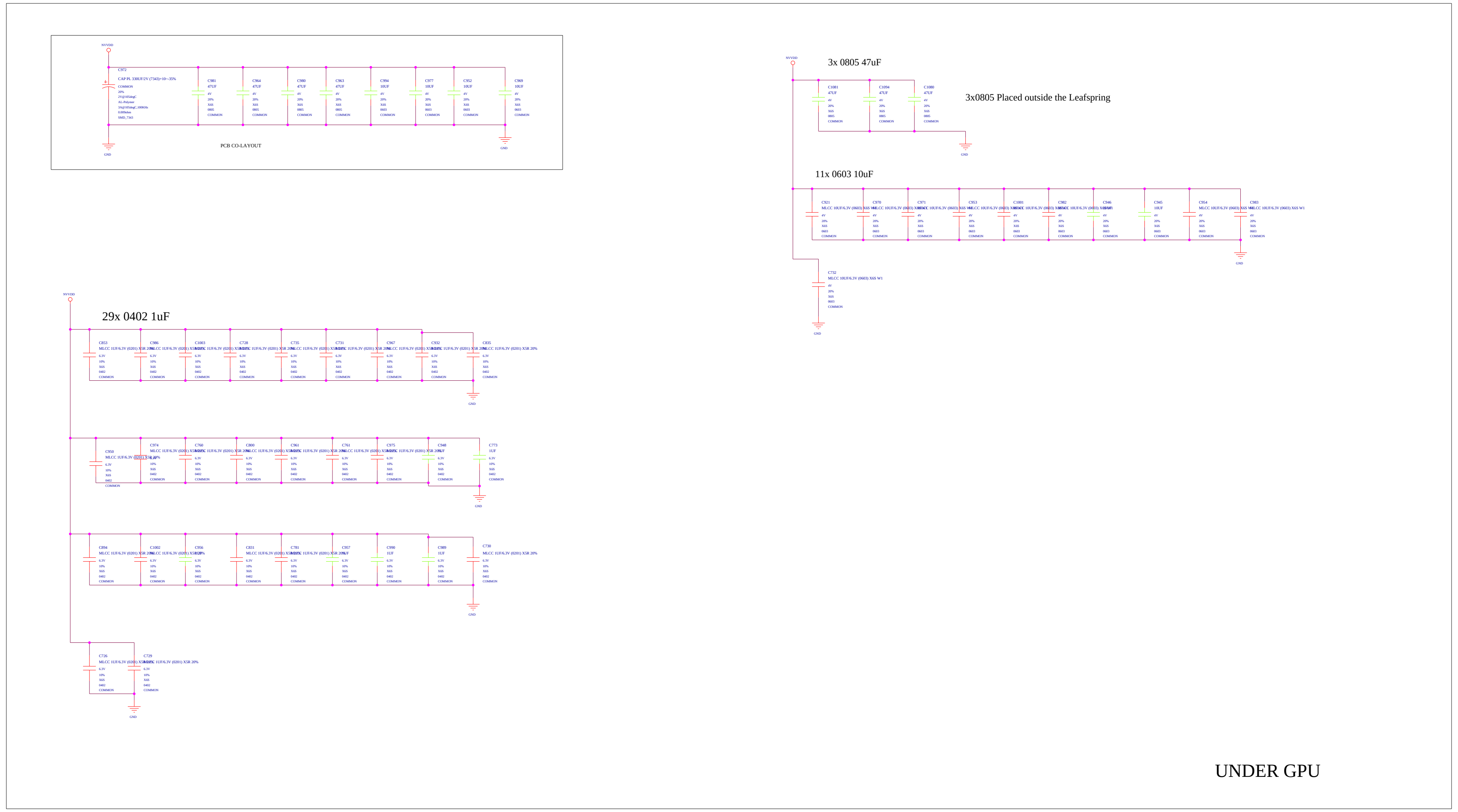
2x 0603 4.7uF

12x 0603 10uF

37 x 0402 1uF

UNDER GPU

Page20: GPU DECOUPLING NVVDD



<Variant Name>

Title : GPU DECOUPLING NVVDD		
<OrgName>	Engineer: Water	
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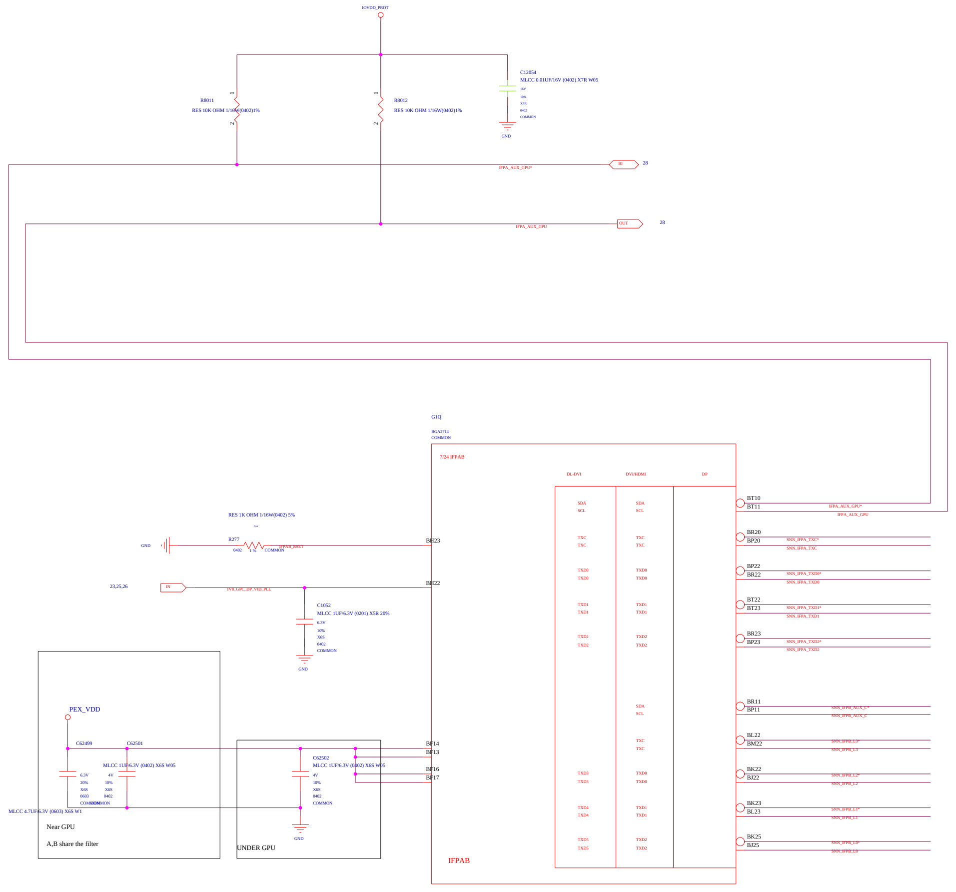
Page21: IFPAB NC



<Variant Name>

	Title :	**IO: IFPAB FRU ROM**
<OrgName>	**Engineer:**	**Water**
Size: Custom	Project Name: **CG142PL**	Rev: 1.00
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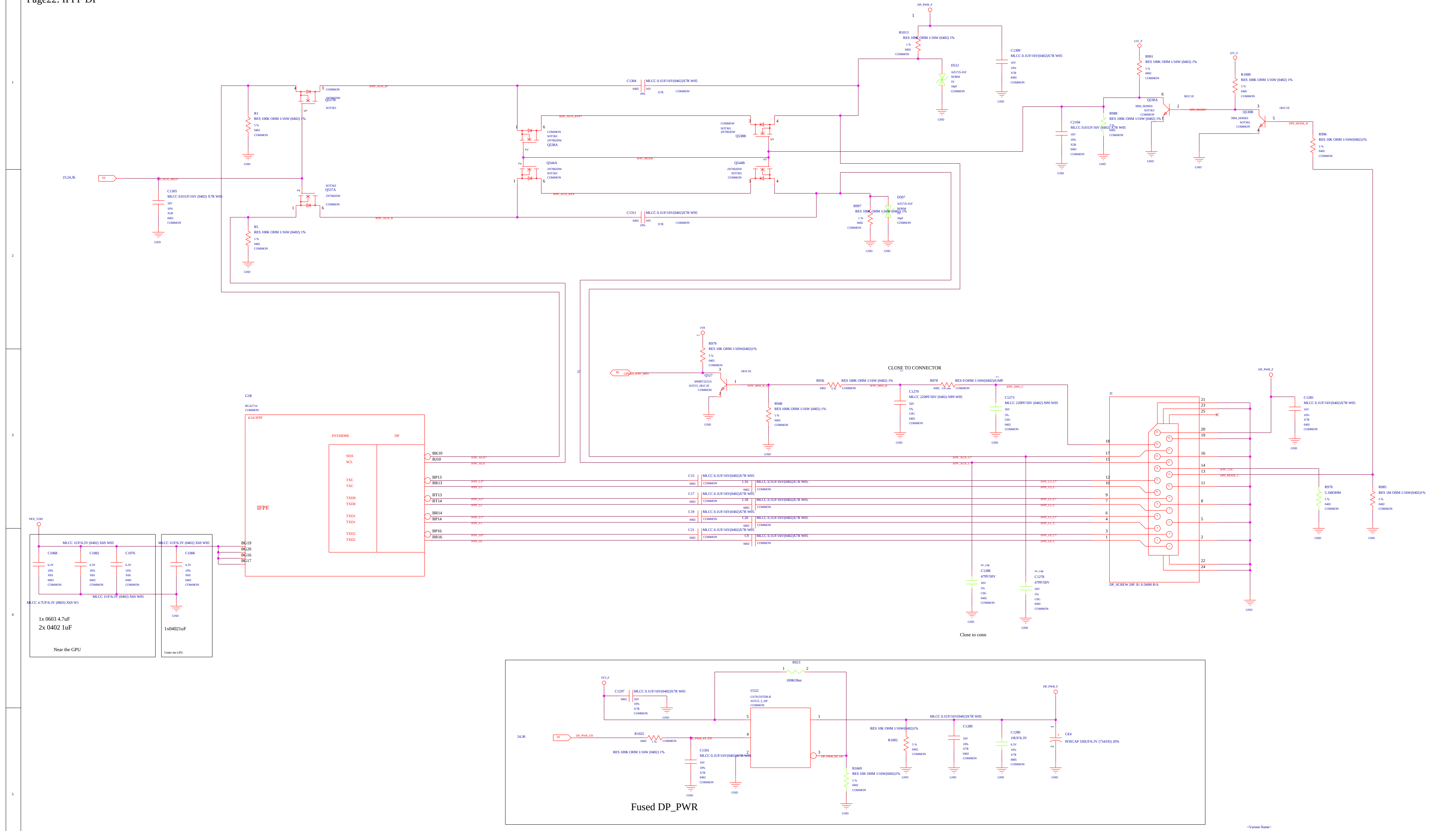
Page22: IFPF DP



<Variant Name>

Title : IO: IFPF DP		
<OrgName>	**Engineer:** Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
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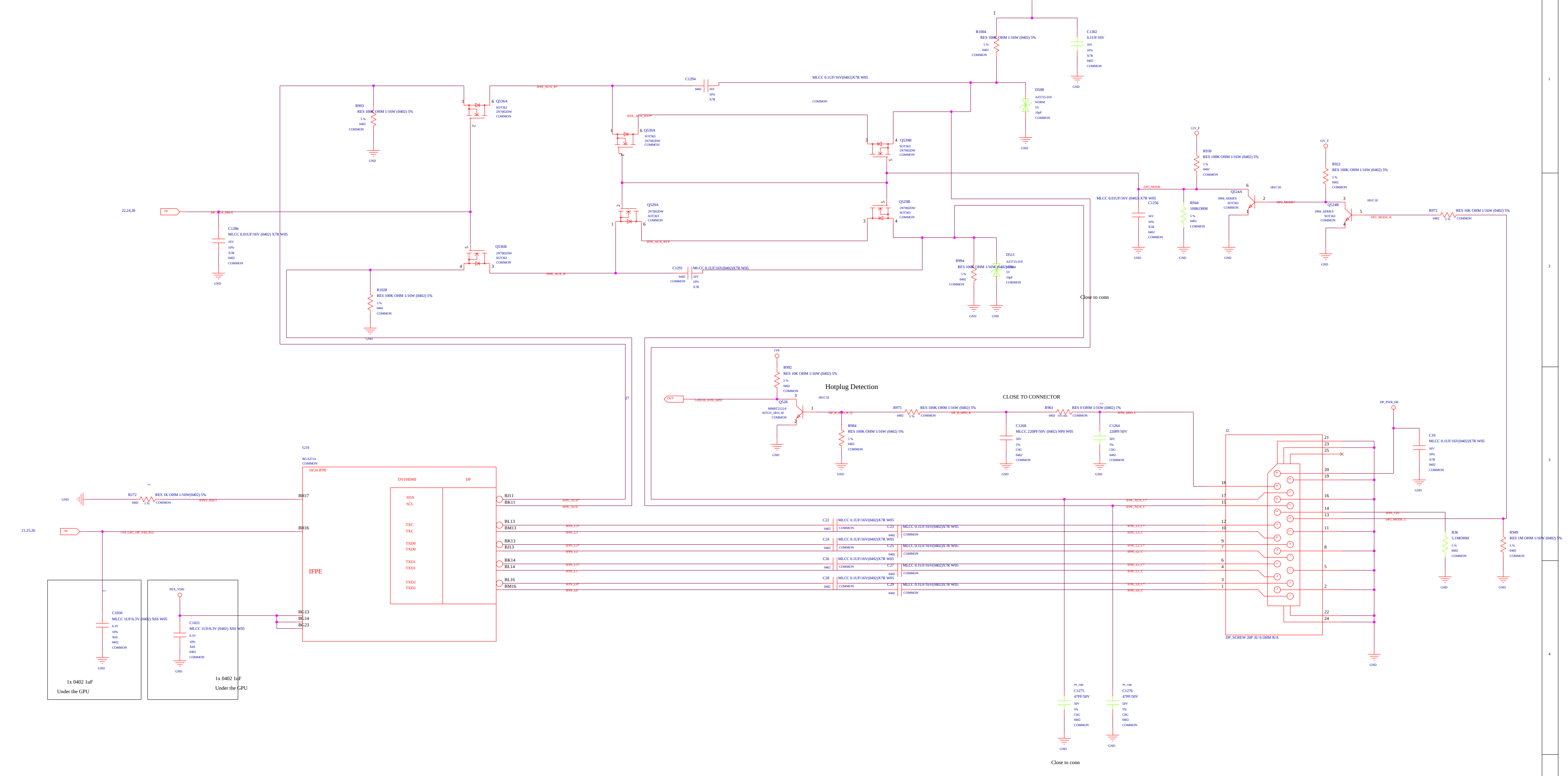
Page23: IFPE DP



ASSEMBLY | <ASSEMBLY_DESCRIPTION>
PAGE DETAIL | IO: IFPE DP

<Variant Name>

Title : IO: IFPE DP

<OrgName> **Engineer:** Water

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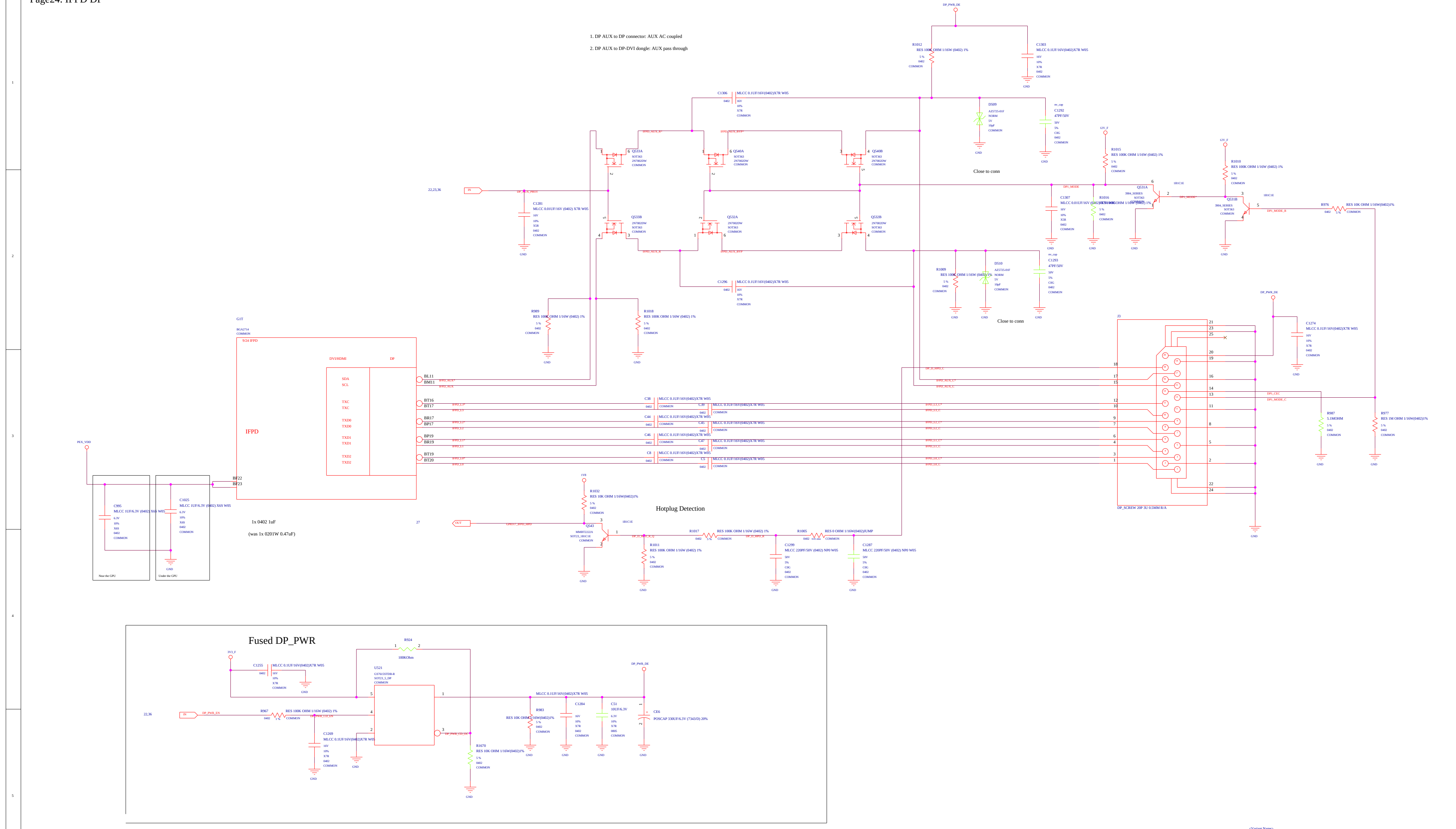
Page24: IFPD DP



<Variant Name>

Title : IO: IFPD DP		
<OrgName>	Engineer: Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
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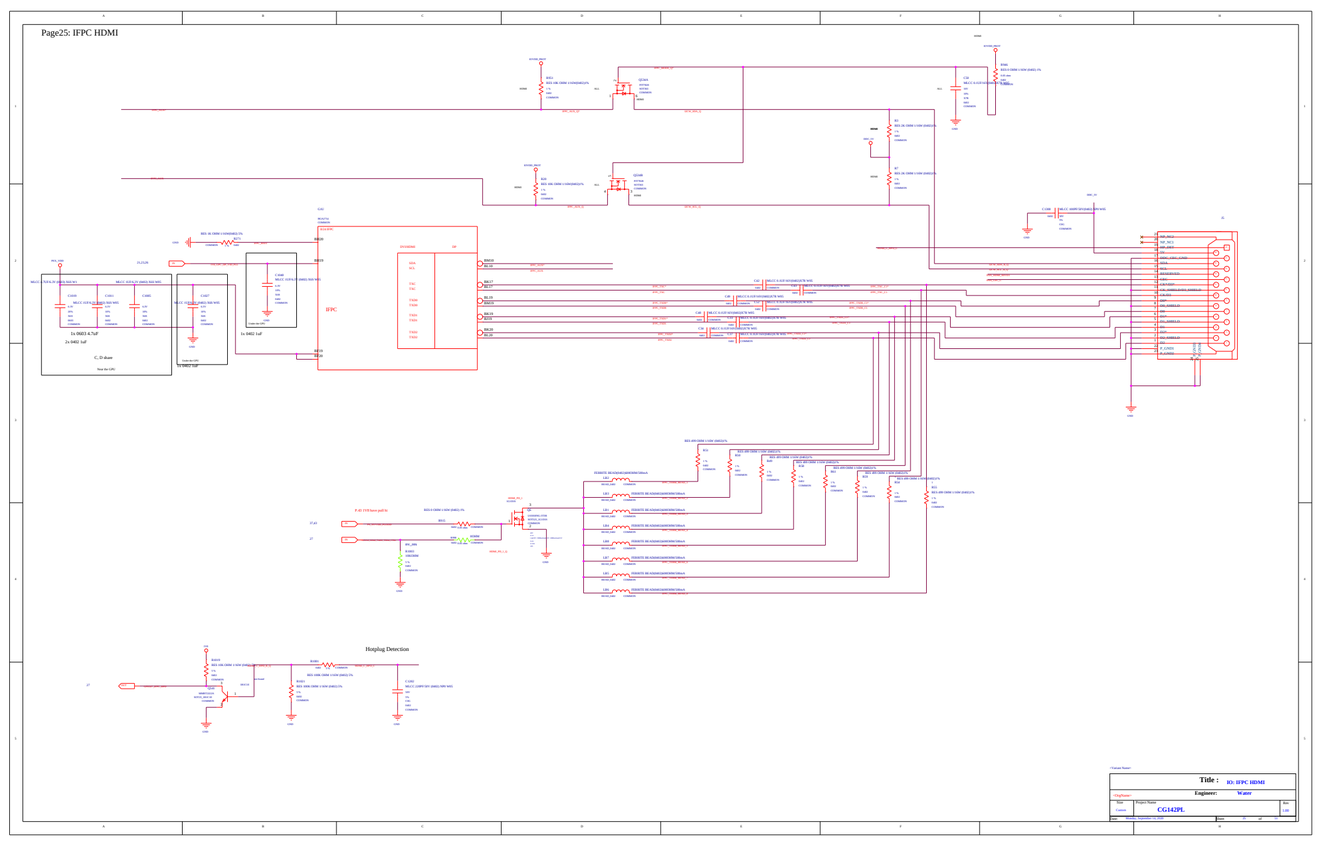
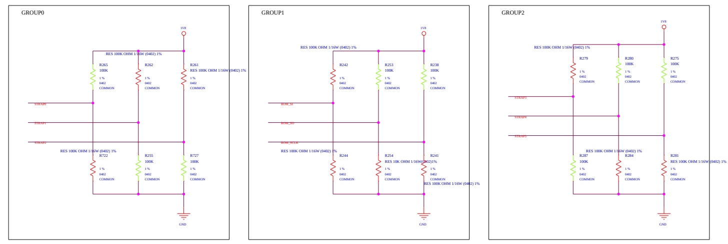
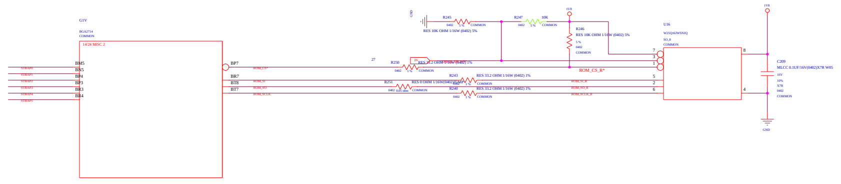

Page25: IFPC HDMI
IFPC
Hotplug Detection
Title : IO: IFPC HDMI
Engineer: Wamer
CG142PL

Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
		TBD		

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V





ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
H	H	H	0111	FS_OVERT ENABLE	DEFAULT
H	H	M	0000	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

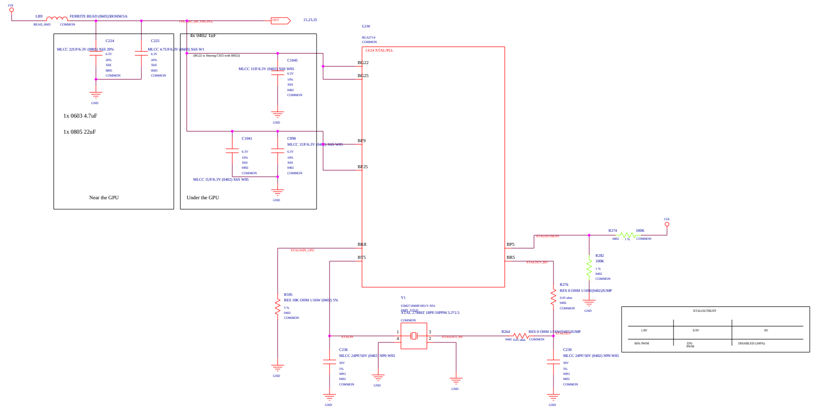
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



<Variant Name>

Title : MISC1: ROM, XTAL,STRAPS		
<OrgName> Engineer: Water		
Size D	Project Name CG142PL	Rev 1.00
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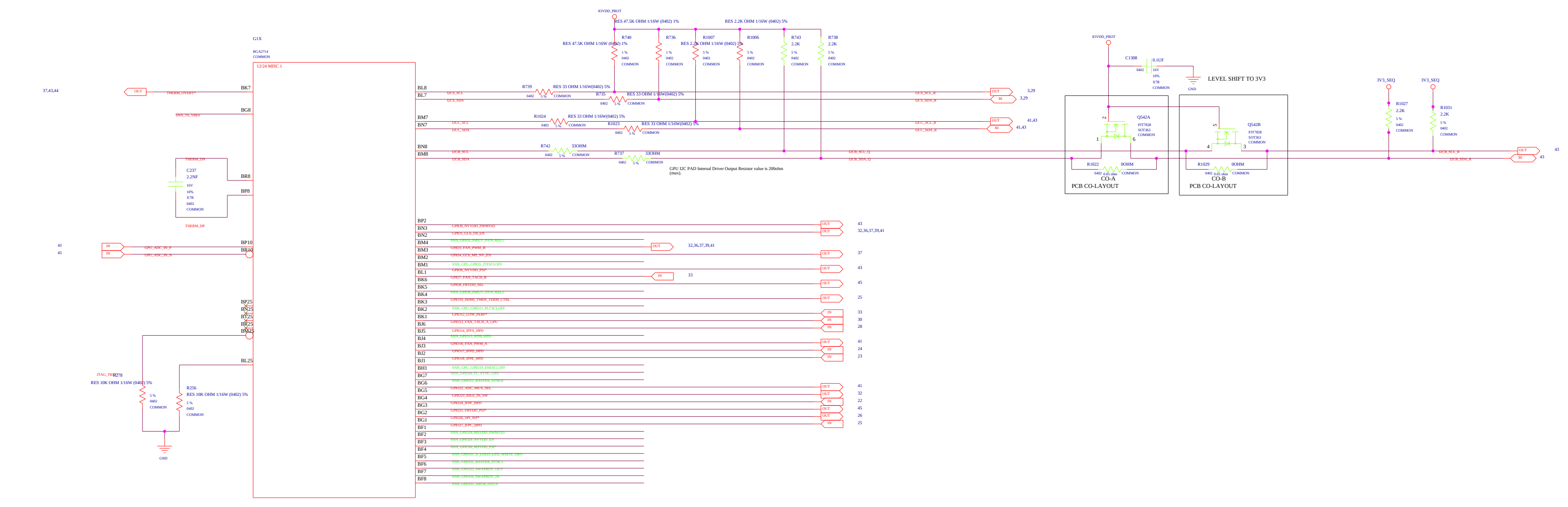
Page27: MISC1: JTAG, GPIO, ADC, I2C, OVERT



<Variant Name>

Title : MISC2_ JTAG,GPIO,ADC,I2C,F		
<OrgName>	Engineer: Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
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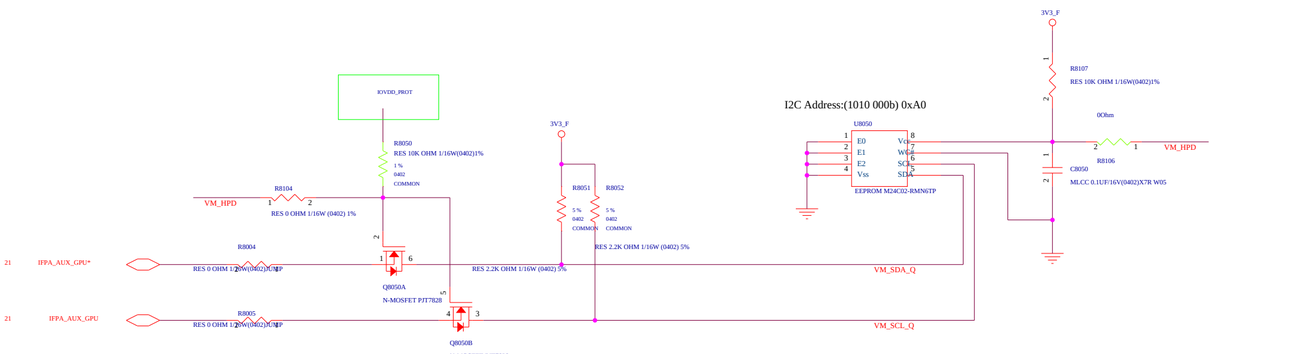

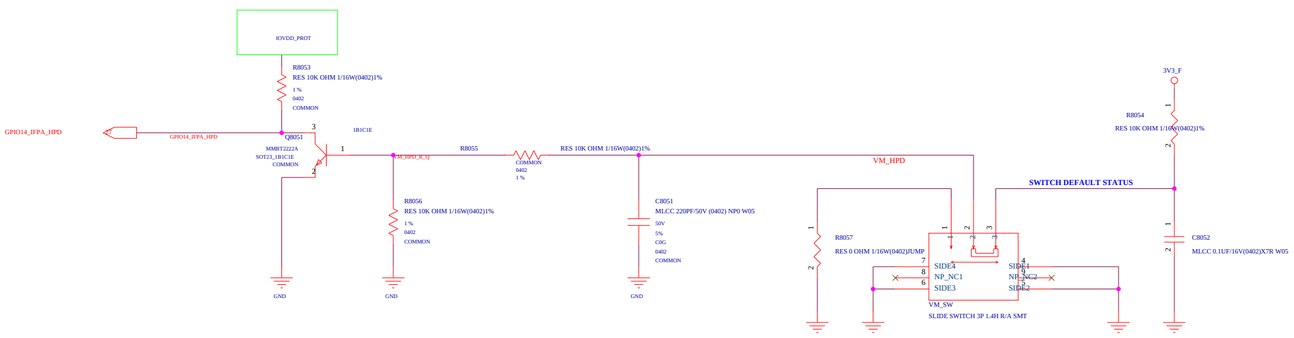

<Variant Name>

Title :	**Virtual Monitor**	
<OrgName>	**Engineer:** **Water**	
Size: A4	Project Name: **CG142PL**	Rev: 1.00
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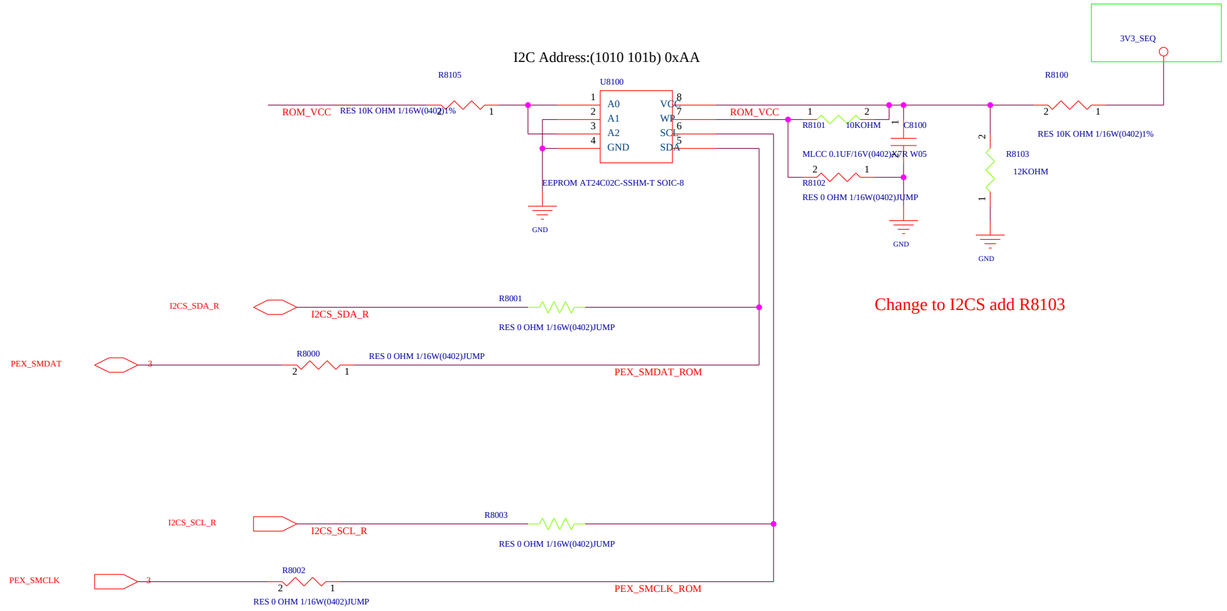
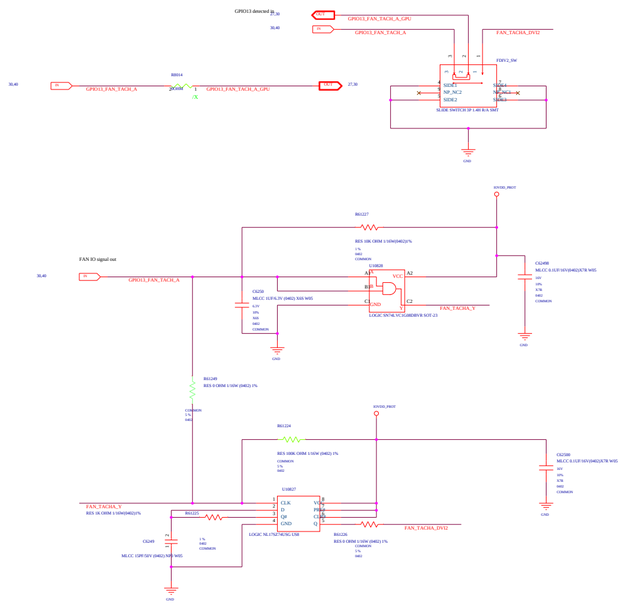


<Variant Name>

Title :	**FRU ROM**	
<OrgName>	**Engineer:** **Water**	
Size: A	Project Name: **CG142PL**	Rev: 1.00



<Variant Name>

	Title : FAN_FreqDiv2	
<OrgName>	**Engineer:** Water	
Size: Custom	Project Name: **CG142PL**	Rev: 1.00
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Page31: Input Power Balancing Switcher

<Variant Name>

Title : PS_ OVRS_INPUT POWER BALAN		
<OrgName> Engineer: Water		
Size Custom	Project Name CG142PL	Rev 1.00
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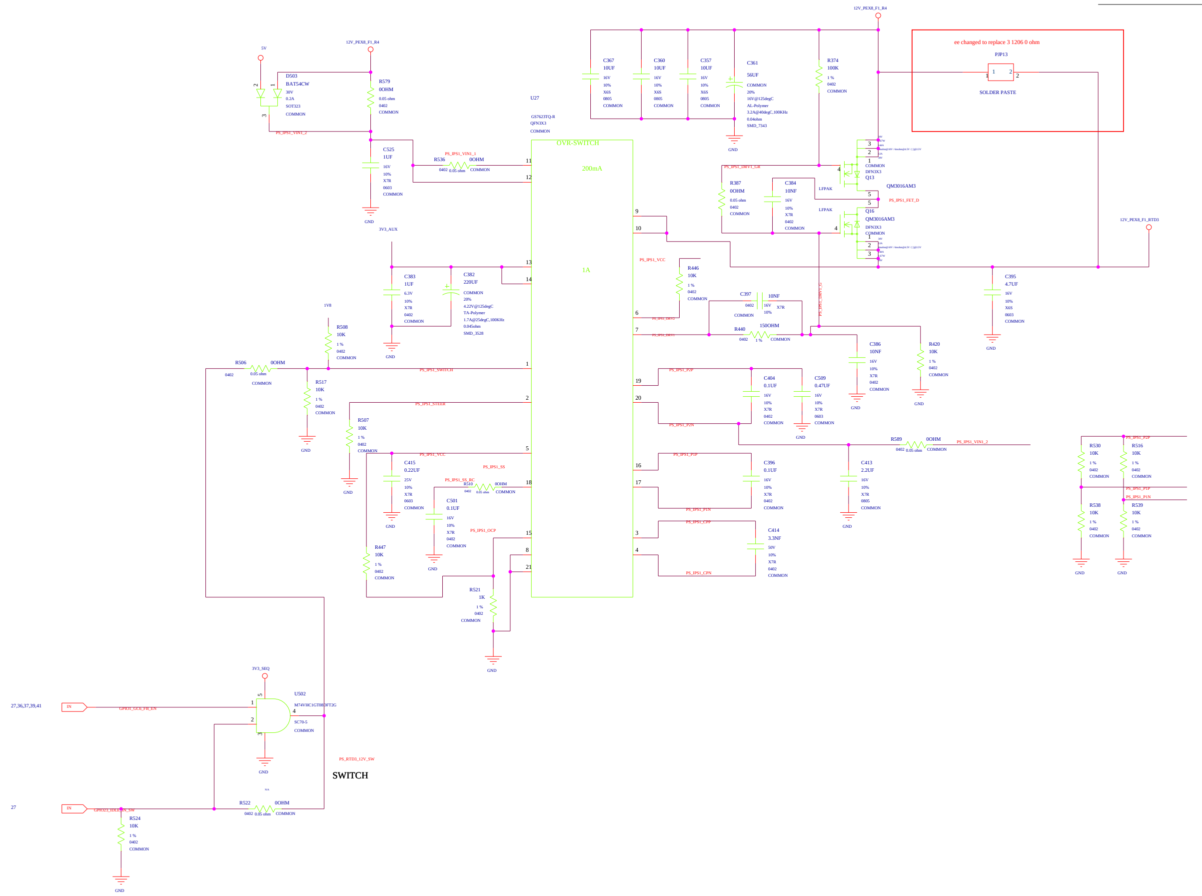
Page32: INPUT SWITCH RTD3 (12V & 3V3_A SWITCHER)

AND GATE LOGIC

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V
0	1	0	12V
1	0	0	12V
1	1	1	3V3A

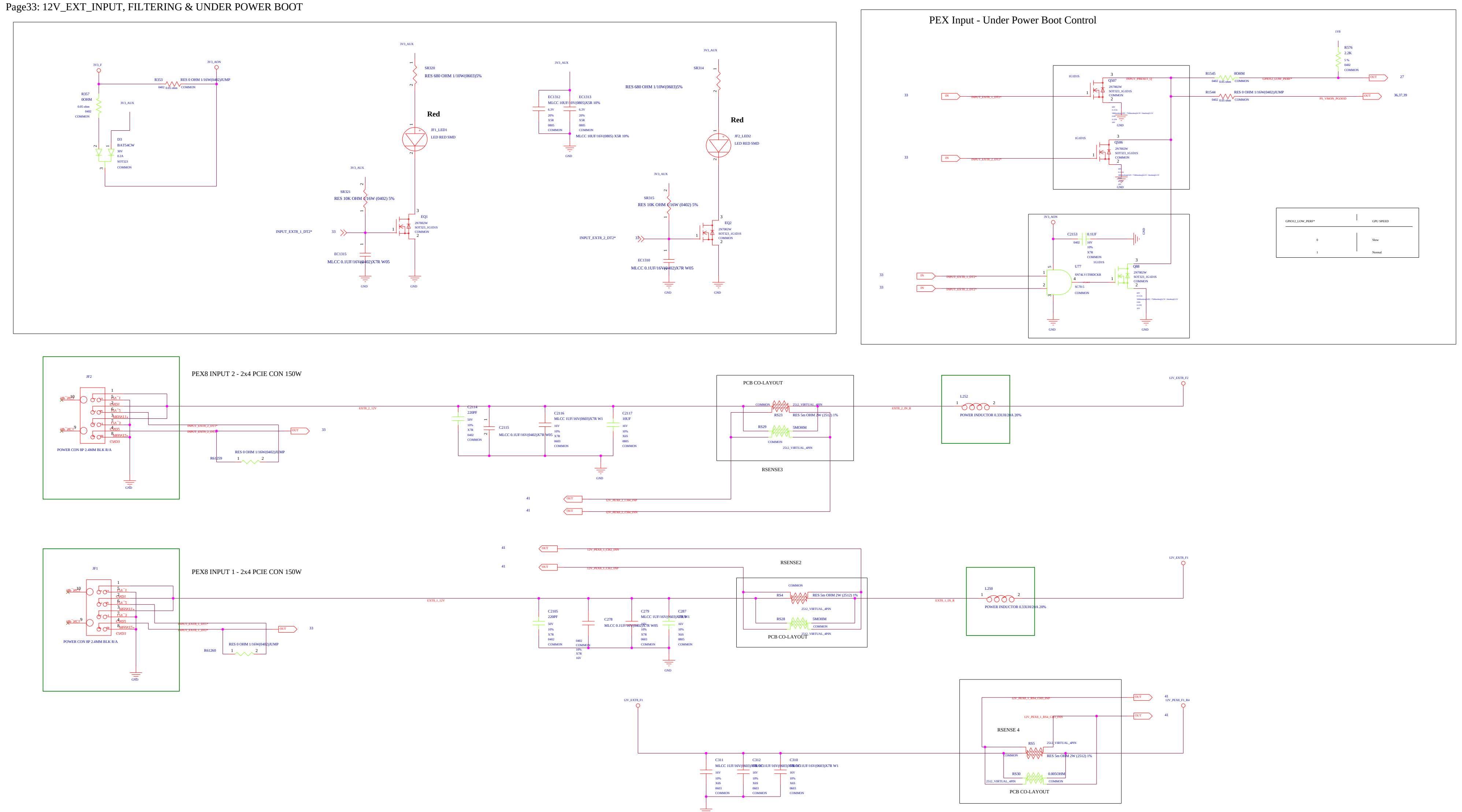
SWITCH	VOUT
0	VOUT = VIN1
1	VOUT = VIN2



<Variant Name>

Title : PS_ RDT3_12V & 3V3_A Switc		
<OrgName>	Engineer: Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
Date: Monday, September 14, 2020	Sheet 32 of 51	

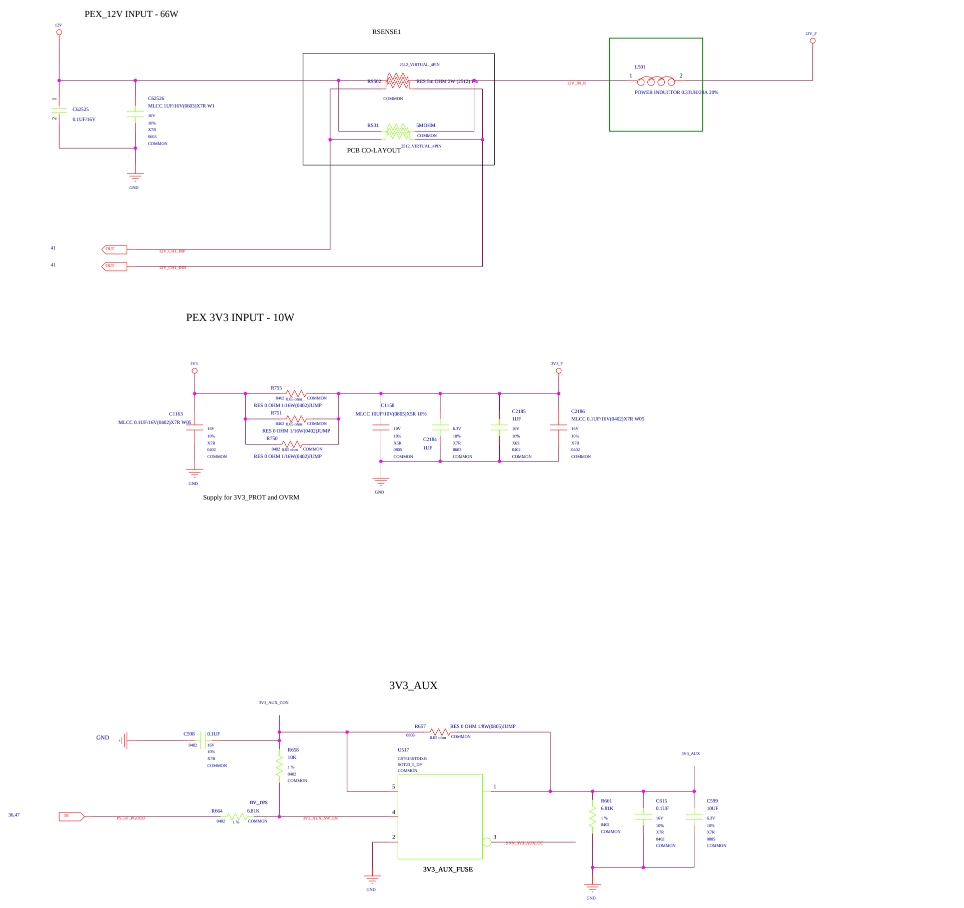
Page33: 12V_EXT_INPUT, FILTERING & UNDER POWER BOOT



<Variant Name>

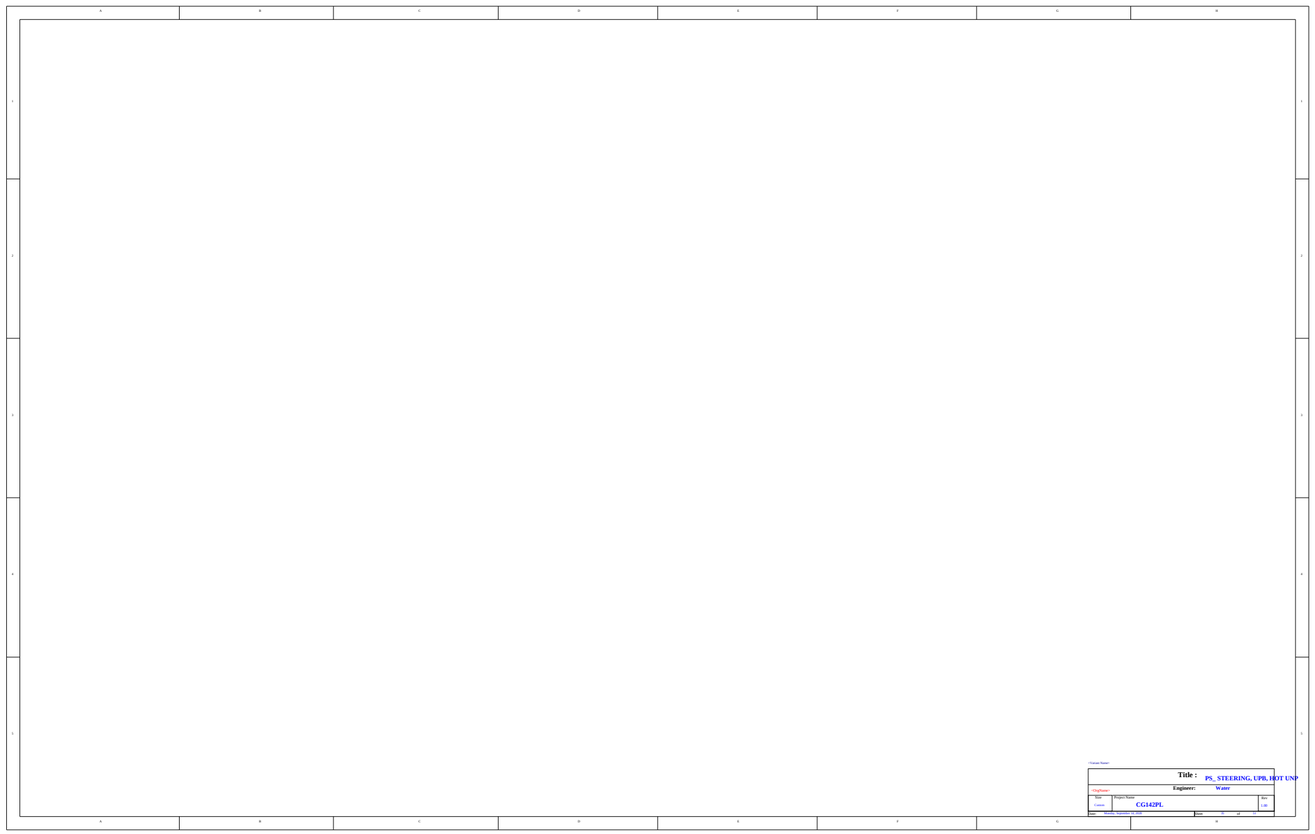
Title : PS_ INPUTS, FILTERING		
<OrgName>	**Engineer:** Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
Date: Monday, September 14, 2020	Sheet 33 of 51	

Page34: PEX_INPUT & FILTERING, PEX_3V3, 3V3_AUX

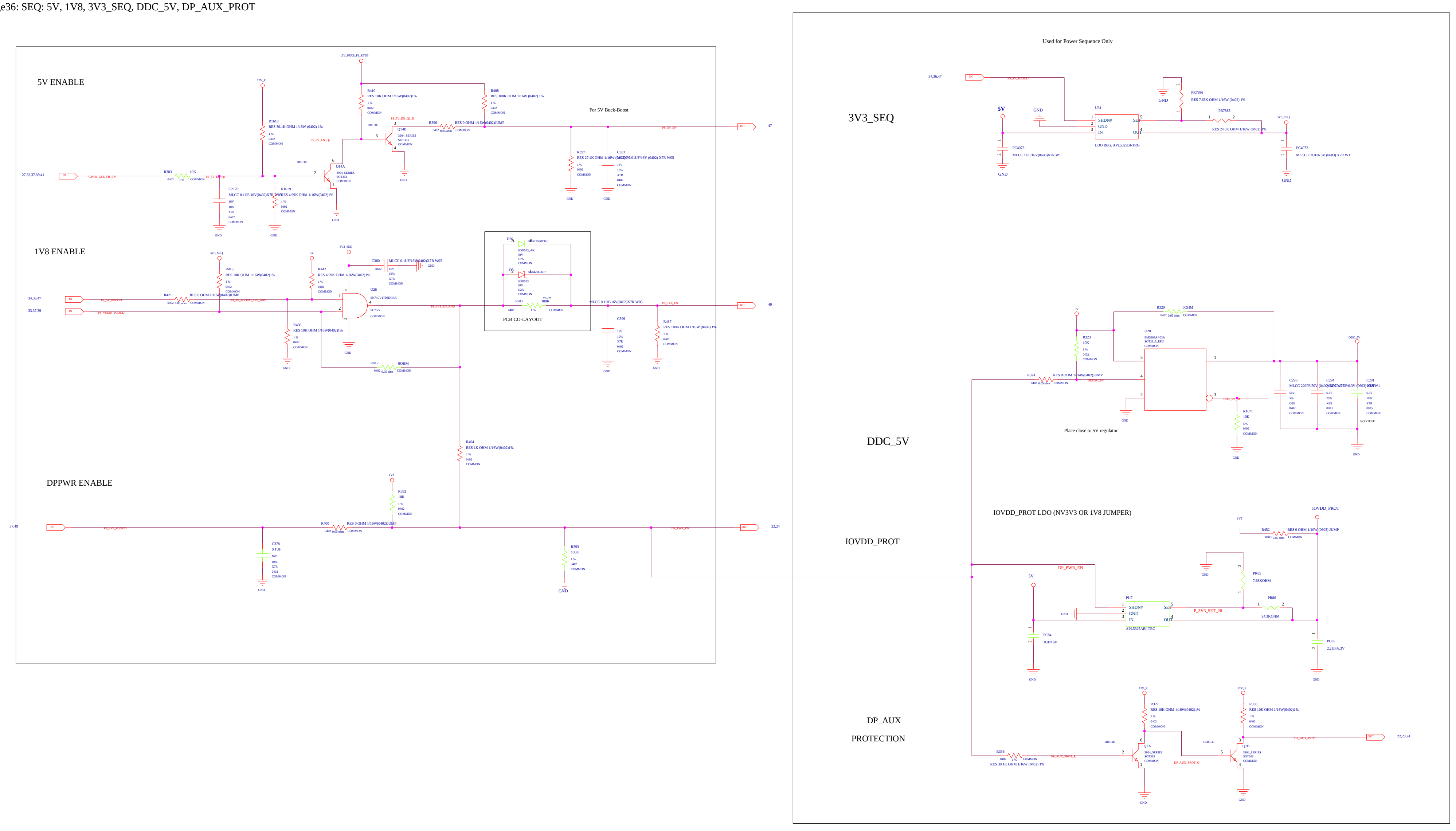


<Variant Name>

	Title :	**PS_ PEX_12V, PEX_3V3 AND A**	
<OrgName>	**Engineer:**	**Water**	
Size: Custom	Project Name: **CG142PL**		Rev: 1.00
Date: Monday, September 14, 2020	Sheet 34 of 51		


Title : PS_ STEERING, UPR, HOT UNP
Engineer: Water
CG142PL

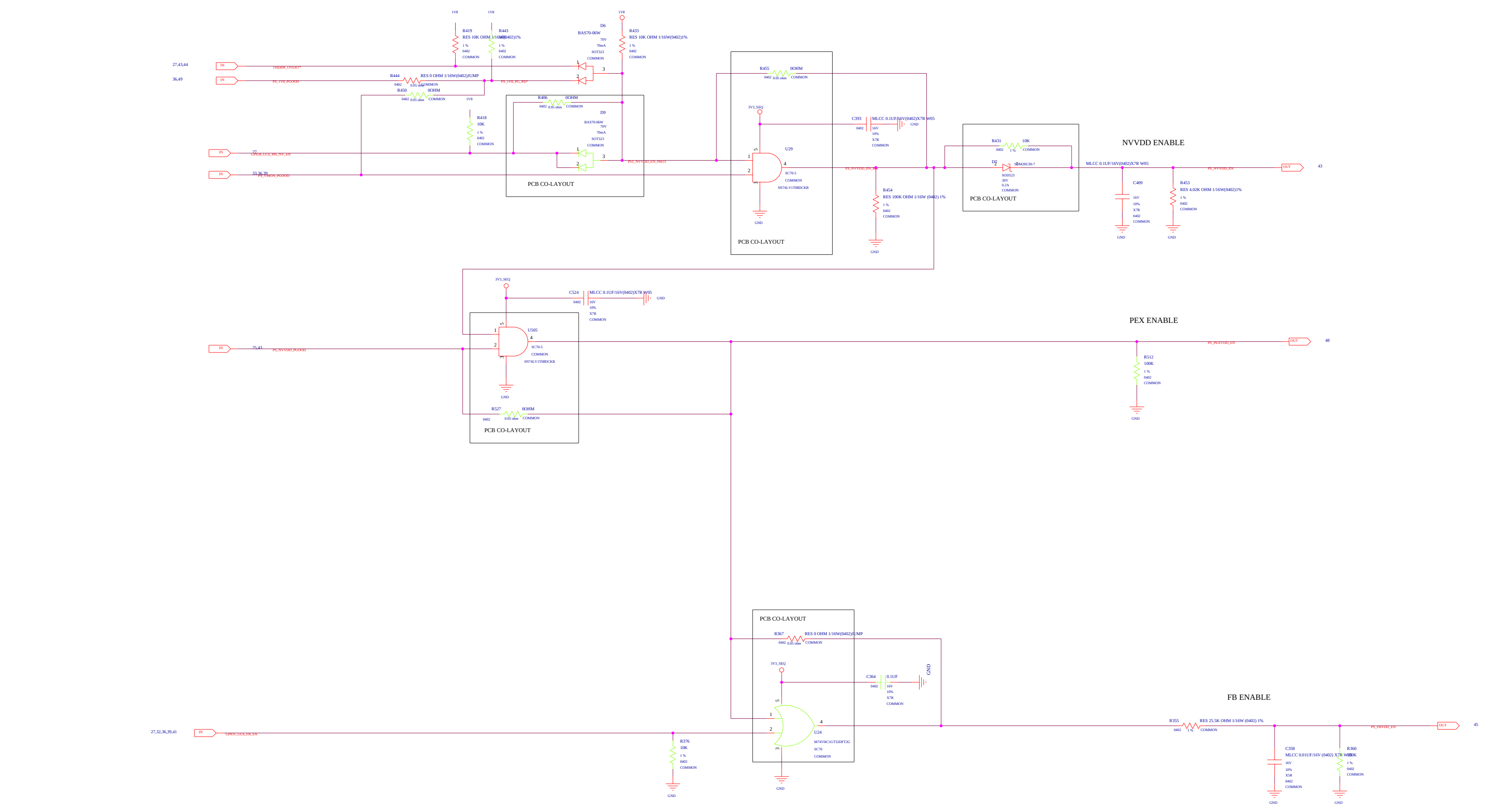
Page36: SEQ: 5V, 1V8, 3V3_SEQ, DDC_5V, DP_AUX_PROT



<Variant Name>

Title : SEQ_ 5V, 1V8, 3V3_SEQ		
<OrgName> Engineer: Water		
Size: Custom	Project Name: CG142PL	Rev: 1.00
Date: Monday, September 14, 2020	Sheet 36 of 51	

Page37: SEQ:NVVDD, PEX, FBVDDQ ENABLE



<Variant Name>

Title : SEQ_ NVVDD, PEX, FBVDDQ EN		
<OrgName>	Engineer: Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
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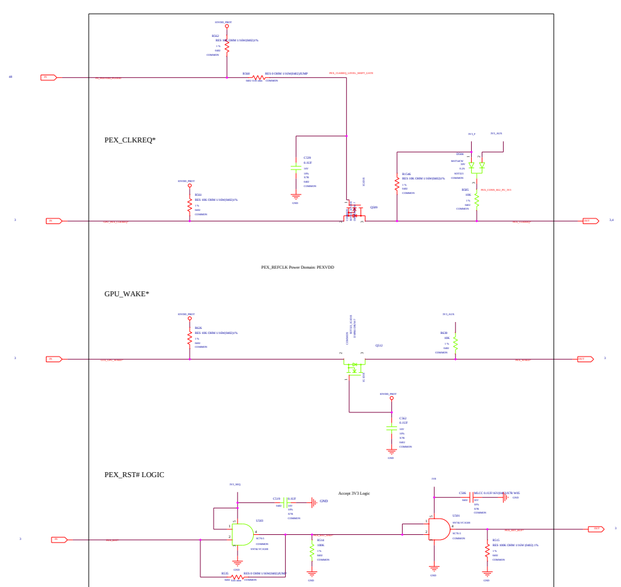
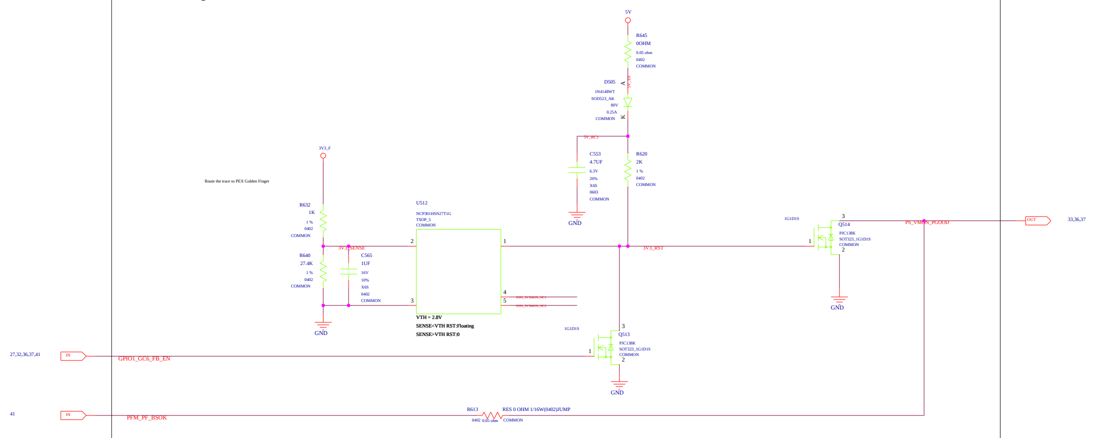
Page38: SEQ:MISC



Title :	SEQ_MISC
Engineer:	Water
Project Name:	CG142PL
Rev:	1.01

Page 39: SEQUENCE:Voltage Monitor

3V3PEX Voltage Monitor



BOM Configuration

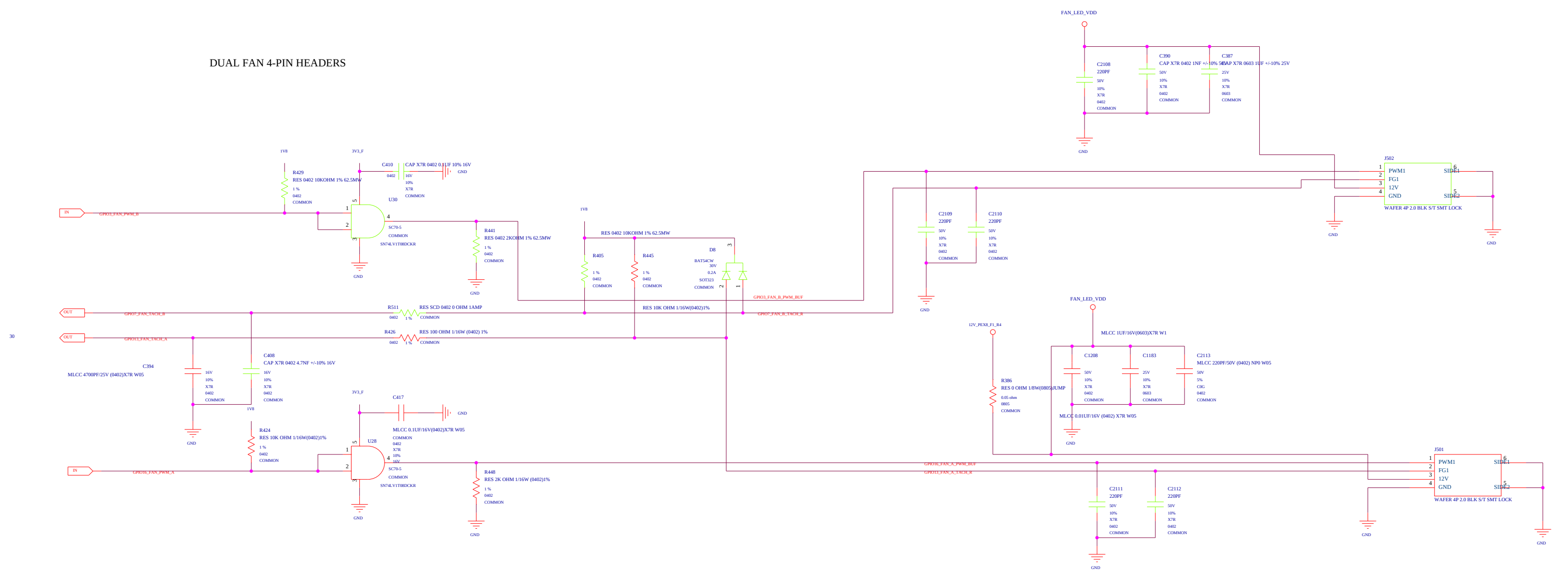
OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

<Variant Name>

Title : SEQ_ VOLTAGE MONITOR		
<OrgName>	Engineer: Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
Date: Monday, September 14, 2020	Sheet 39 of 51	

Page40: FAN&LED



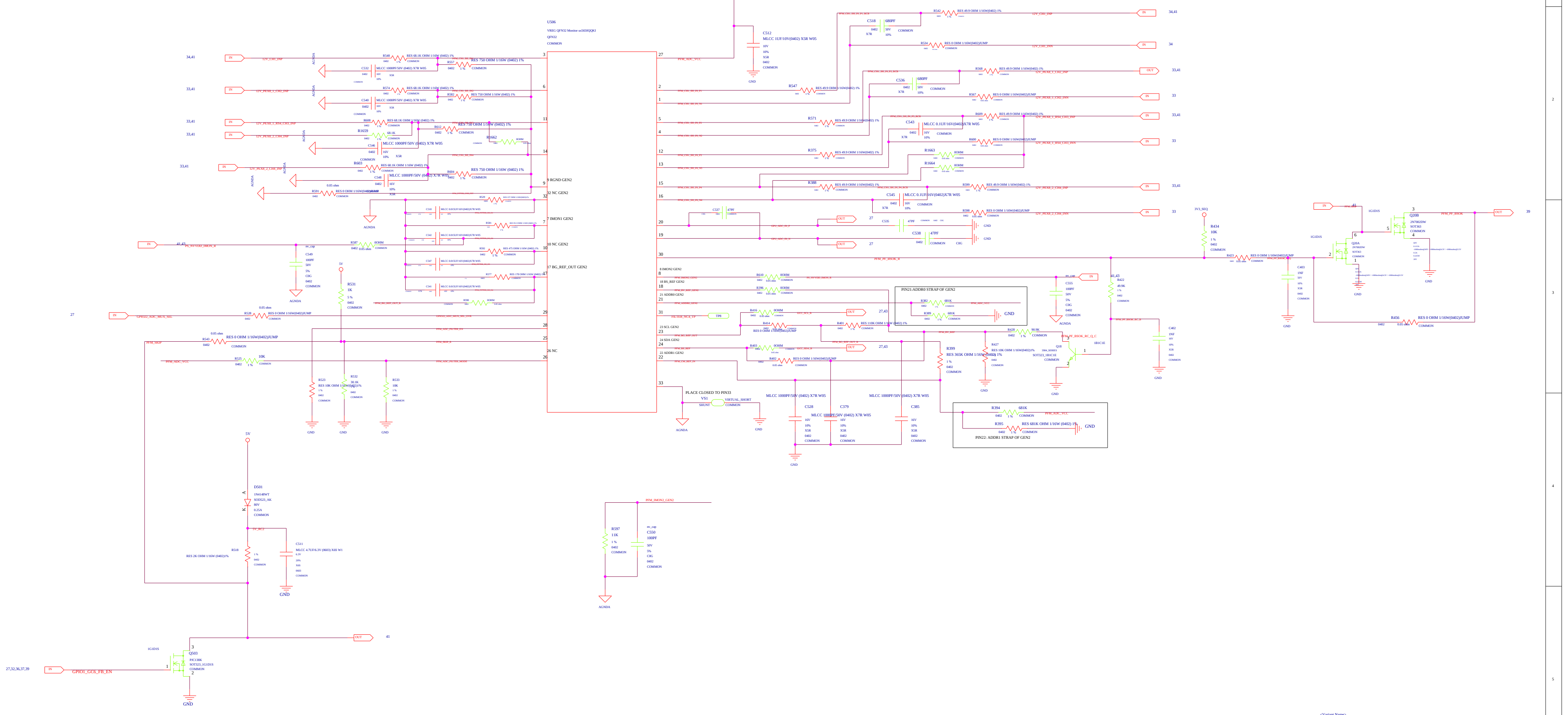
<Variant Name>

	Title : FAN & LED		
<OrgName>	Engineer: Water		
Size: Custom	Project Name: CG142PL		Rev: 1.00
Date: Monday, September 14, 2020		Sheet 40 of 51	

Page41: OVRM_PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

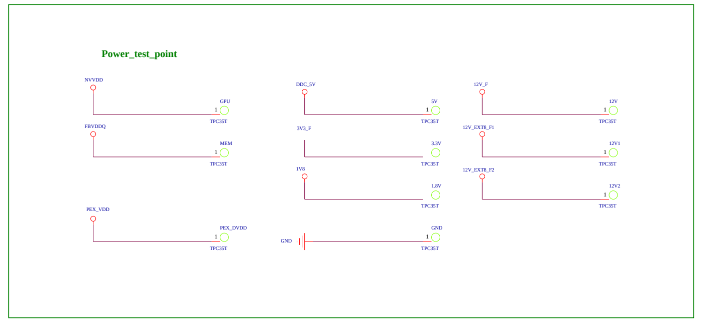
ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY

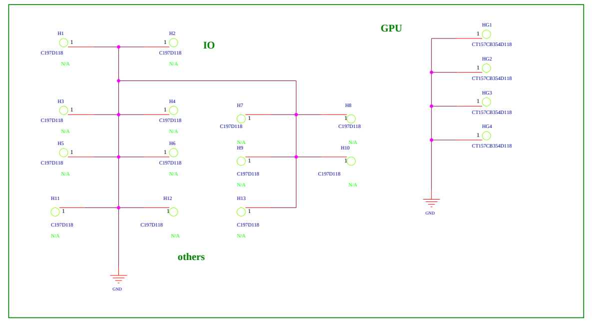


<Variant Name>

Title : PS_OVRM_PWR_SENSE		
<OrgName>	Engineer: Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
Date: Monday, September 14, 2020	Sheet 41 of 51	

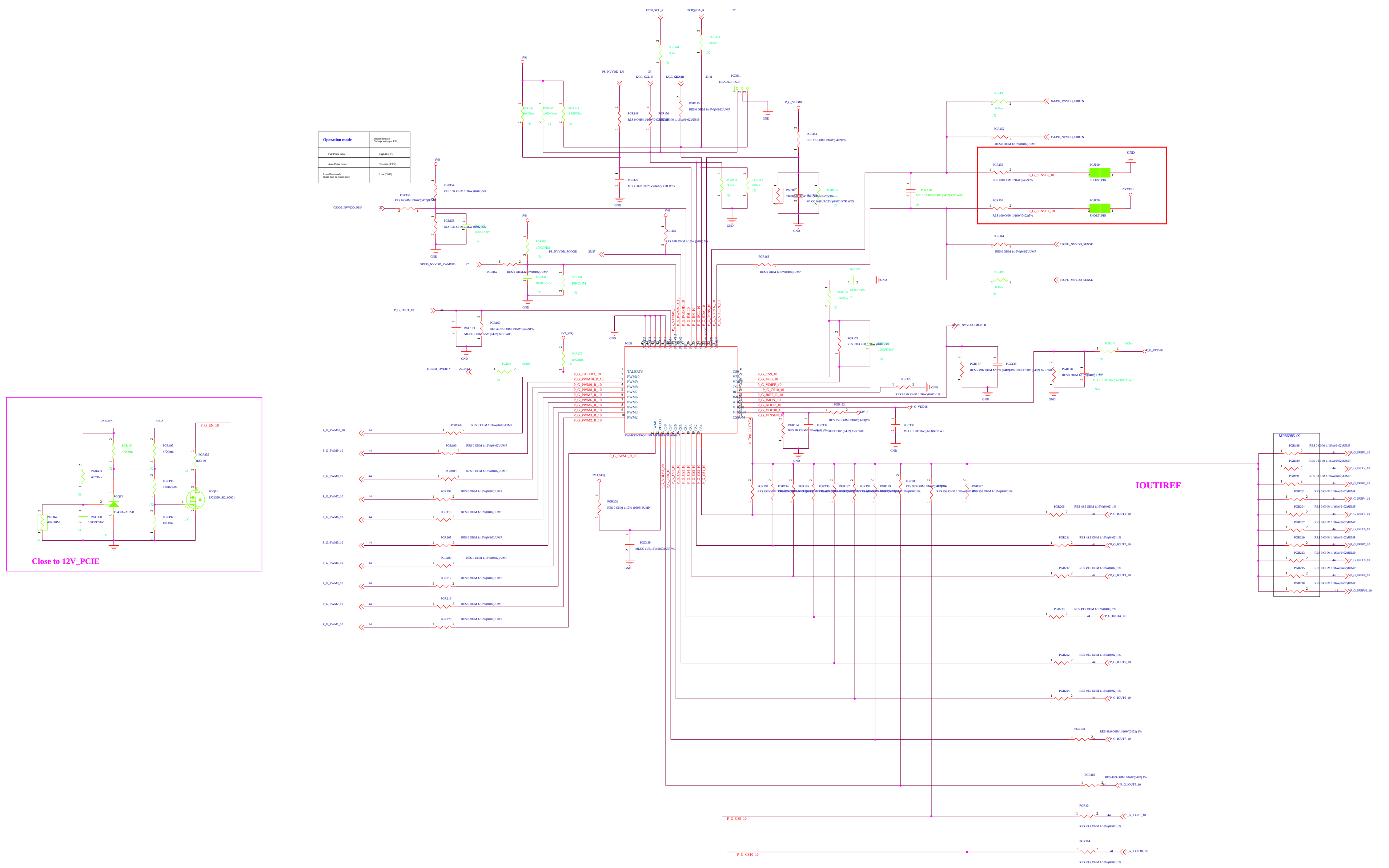
Page42: MECH





<Variant Name>

Title : MECH		
<OrgName> Engineer: Water		
Size Custom	Project Name CG142PL	Rev 1.00
Date: Monday, September 14, 2020	Sheet 42 of 51	



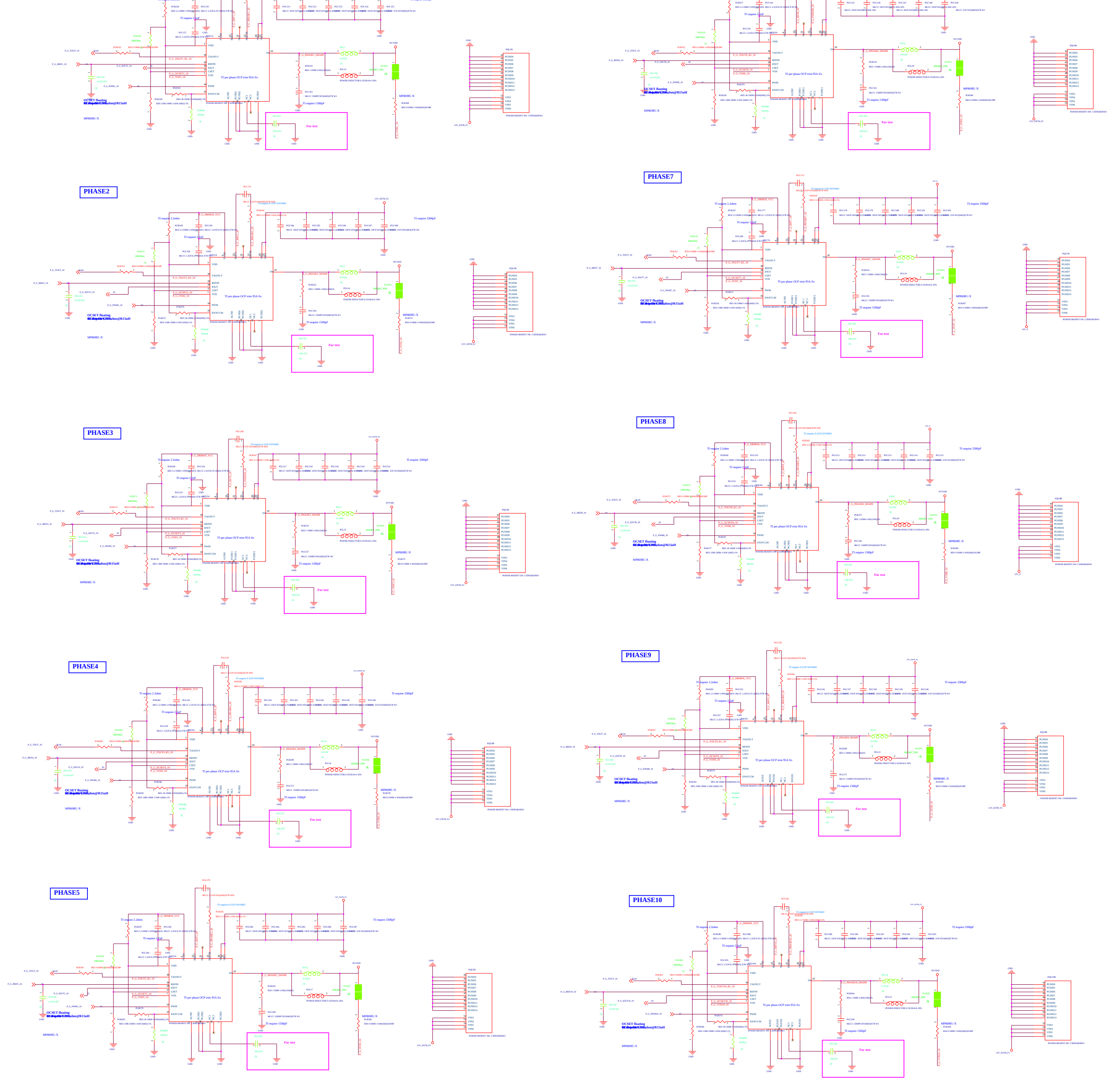
<Variant Name>

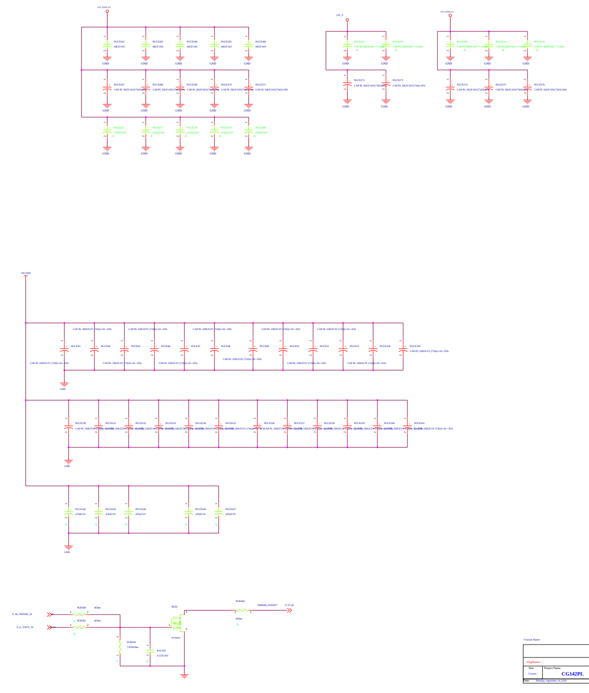
Title : NVVDD_10 controller(MP2888)		
<OrgName> Engineer: Water		
Size: Custom	Project Name: CG142PL	Rev: 1.00
Date: Monday, September 14, 2020	Sheet 43 of 51	

PHASE1

PHASE6

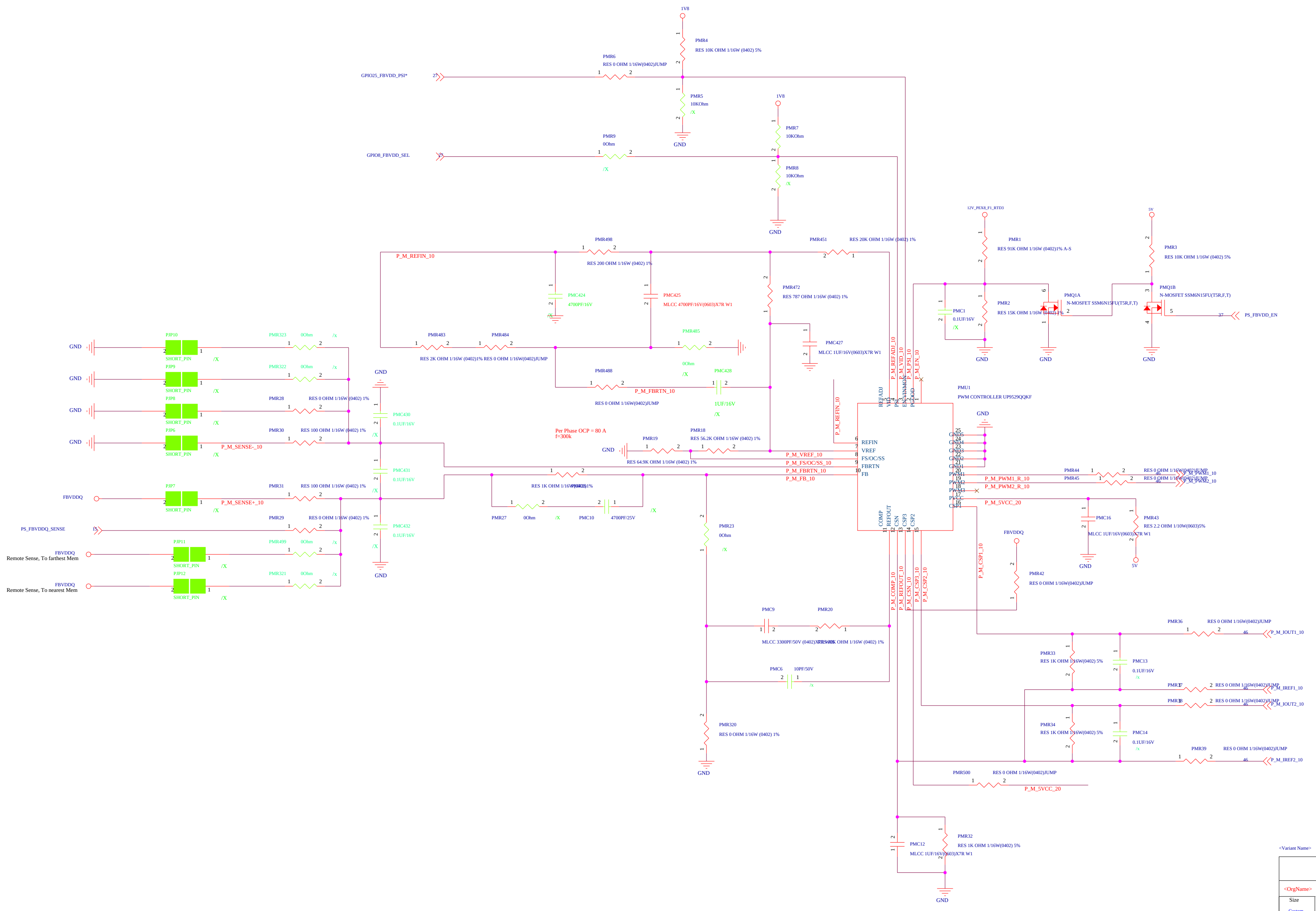
phase1 location	PGR238	PGR369	PGR232
CSD95480	130K	0 ohm	0 ohm
TDA21462	/X	0 ohm	0 ohm
FDMF3160	/X	/X	/X
NCP303151	0 ohm	/X	0 ohm





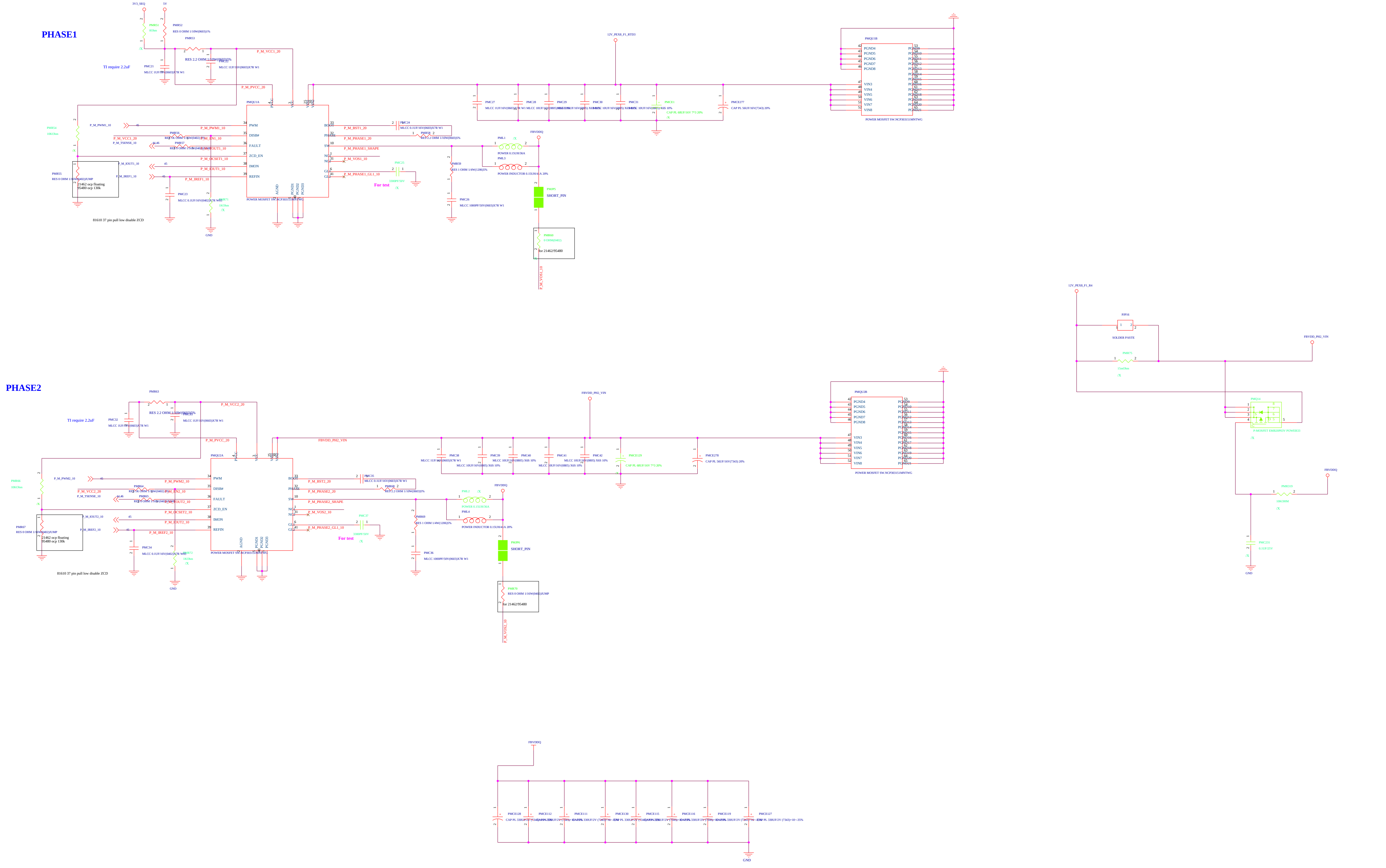
<Variant Name>

Title : NVVDD_10 DR-MOS(CSD95481)		
<OrgName> Engineer: Water		
Size: Custom	Project Name: CG142PL	Rev: 1.00
Date: Monday, September 14, 2020	Sheet 44 of 51	



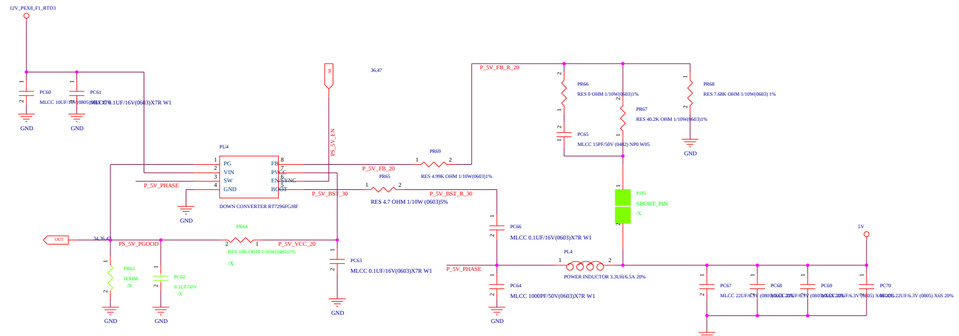
<Variant Name>

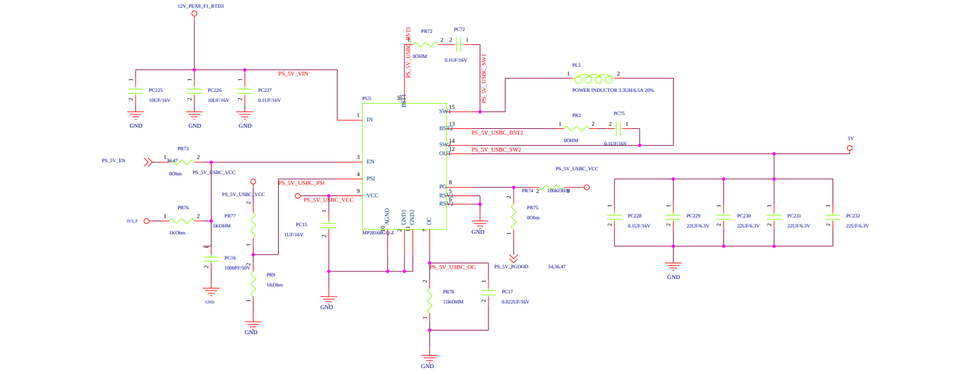
Title : FBVDDQ_2 controller(UP9529Q		
<OrgName>	**Engineer:** Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
Date: Monday, September 14, 2020	Sheet 45 of 51	



<Variant Name>

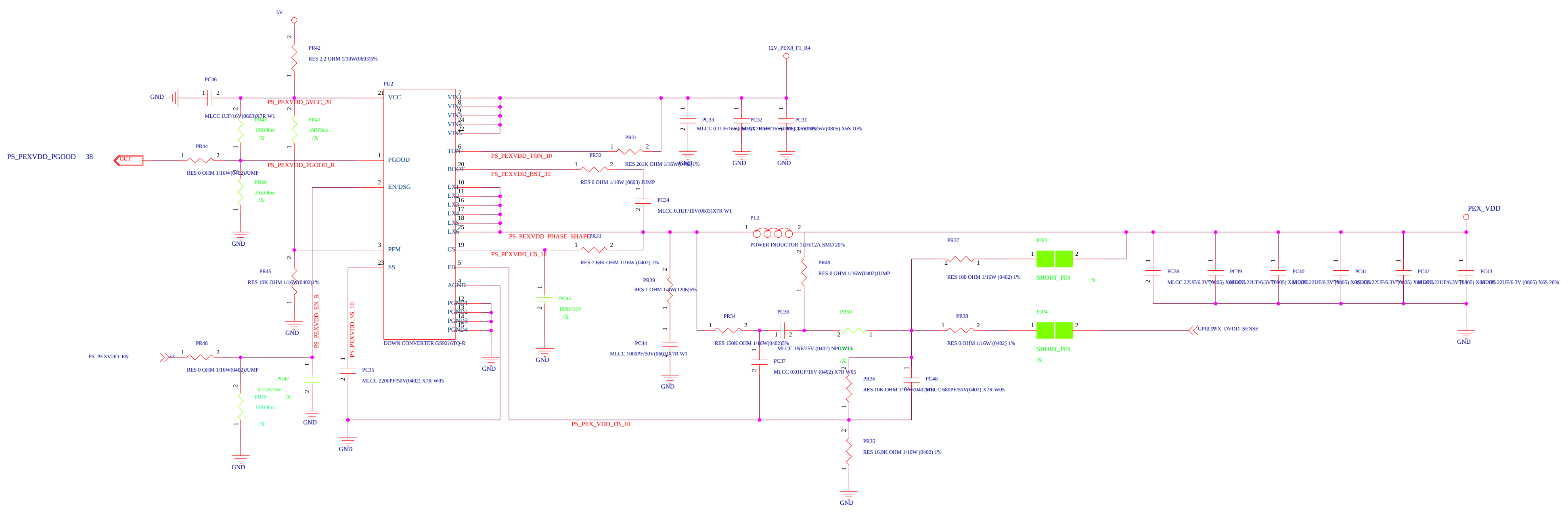
	Title : FBVDDQ_2 DR-MOS(303151)		
<OrgName>	Engineer: Water		
Size Custom	Project Name CG142PL		Rev 1.00
Date: Monday, September 14, 2020		Sheet 46 of 51	





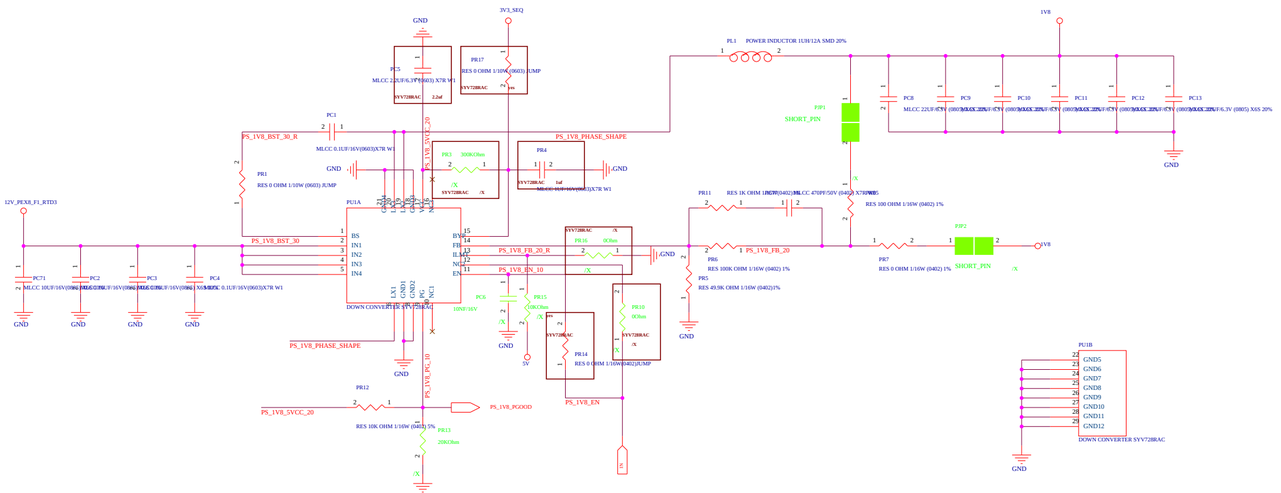
<Variant Name>

	Title : 5V(RT7296/MP1475)	
<OrgName>	**Engineer:** Water	
Size: A3	Project Name: **CG142PL**	Rev: 1.00



<Variant Name>

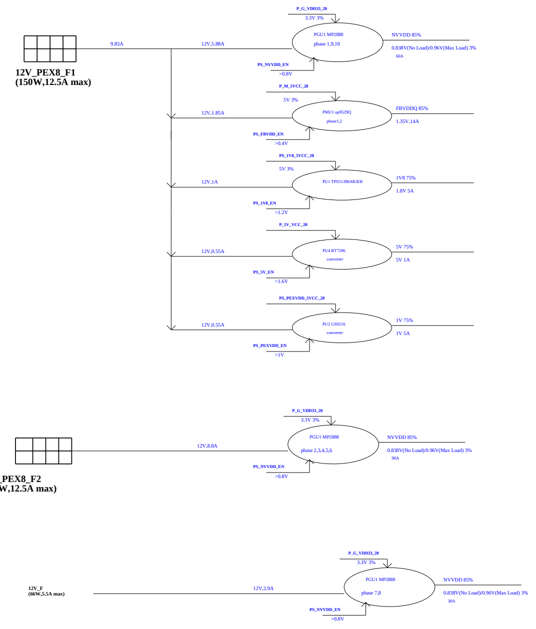
Title : PEX_VDD(GS9216TQ-R)		
<OrgName>	**Engineer:** Water	
Size: Custom	Project Name: **CG142PL**	Rev: 1.00
Date: Monday, September 14, 2020	Sheet 48 of 51	



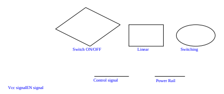
<Variant Name>

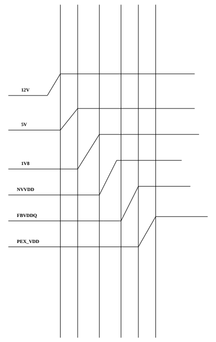
	Title : 1V8(TPS51396/SYV728RAC)	
<OrgName>	**Engineer:** Water	
Size: B	Project Name: **CG142PL**	Rev: 1.00
Date: Monday, September 14, 2020	Sheet 49 of 53	

PS: Power Flow



P_G_VDD33_20
3.3V 3%
9.83A
12V,5.88A
PGU1 MP2888
phase 1,9,10
NVVDD 85%
0.838V(No Load)/0.96V(Max Load) 3%
60A
PS_NVVDD_EN
>0.8V
12V_PEX8_F1
(150W,12.5A max)
P_M_5VCC_20
5V 3%
12V,1.85A
PMU1 up9529Q
phase1,2
FBVDDQ 85%
1.35V,14A
PS_FBVDD_EN
>0.4V
PS_1V8_5VCC_20
5V 3%
12V,1A
PU1 TPS51396ARJER
1V8 75%
1.8V 5A
PS_1V8_EN
>1.2V
P_5V_VCC_20
12V,0.55A
PU4 RT7296
converter
5V 75%
5V 1A
PS_5V_EN
>1.6V
PS_PEXVDD_5VCC_20
12V,0.55A
PU2 GS9216
converter
1V 75%
1V 5A
PS_PEXVDD_EN
>1V
P_G_VDD33_20
3.3V 3%
12V,8.8A
PGU1 MP2888
phase 2,3,4,5,6
NVVDD 85%
0.838V(No Load)/0.96V(Max Load) 3%
90A
PS_NVVDD_EN
>0.8V
12V_PEX8_F2
(150W,12.5A max)
P_G_VDD33_20
3.3V 3%
12V_F
(66W,5.5A max)
12V,2.9A
PGU1 MP2888
phase 7,8
NVVDD 85%
0.838V(No Load)/0.96V(Max Load) 3%
30A
PS_NVVDD_EN
>0.8V





<Variant Name>

Title : PS_ Power Flow		
<OrgName>	Engineer: Water	
Size: Custom	Project Name: CG142PL	Rev: 1.00
Date: Monday, September 14, 2020	Sheet 50 of 50	