電子類元件 零件承認書文件 CHECK LIST

零件廠商：AOS **品名規格：DR MOS AOZ5311NQI 50A AOS**

技嘉料號：10IFD-505311-00R

項次	文件項目
	Data Sheet 檢核項目
1	DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2**
8	零件樣品 20PCS(Chipset 等高單價，至少 1PCS)
9	**電子零件承認基本調查表。註 3**
10	以上資料電子檔為 PDF 檔，且是同 1 個 File
	GSCM 綠色產品管理系統-物料管制文件檢核清單
物料管制文件 1	GSCM 綠色產品管理系統：零件照片
物料管制文件 2	GSCM 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4**
物料管制文件 3	GSCM 綠色產品管理系統：Data Sheet
	GSCM 綠色產品管理系統-MCD 表格
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
	其他文件 (僅適用電阻、電容類之系列元件)
附件 1	危害物質測試報告 Test Report of Hazardous Substances。**註 5**
附件 2	元件調查表 Component Composition Table

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等

※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)

2.1. 基本需符合 JEDEC 規範

2.2. Ambient Temp. (Reflow Temp endurace): >225℃, 70 sec. 零件塑膠材質需 PA9T(含)等級以上

2.3. PASTE IN HOLE 零件塑膠材質需 PA9T(含)等級以上

※ **3. 電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G*,11T***

非 IC 類：10C*,11C*,10L*,11L*,10X*,11X*,10R*,11B*

※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”

※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

電子零件承認基本調查表

一、原物料規格/來源

項次	部位名稱/規格	材質	原物料來源產地
1	Bonding wire	Metal	SINGAPORE, PANDAN
2	Chip	Wafer	U.S., Oregon
3	Clip	Metal	CHINA, JIANGSU
4	Die attach material 1	Adhesives	U.S., CALIFORNIA
5	Die attach material 2	Soldering	SINGAPORE, kian teck avenue
6	Encapsulation	Epoxy Resin	JAPAN, FUKUOKA
7	Lead Frame	Metal	CHINA, SHENZHEN
8	Lead Frame Plating	Metal materials plating layer	CHINA, SHENZHEN
9	Lead-finished	Metal materials plating layer	CHINA, KUNSHAN

二、晶圓廠(非 IC 類免填)

項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	Jireh	U.S., Oregon	8	100	自有

三、封裝廠(IC 類)；成品之生產製造工廠(非 IC 類)

項次	工廠名稱	生產產地	投產比率(%)	自有/外包
1	Nissi (ALPHA & OMEGA Semiconductor (Shanghai), Ltd.)	China	100	自有

四、產能

總產能(月/PCS)	可供技嘉產能(月/PCS)

※ 1. IC 類之晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ **2. 非 IC 類零件之成品生產製造工廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動（包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件**

※ **3. 以上資訊欄位若有不足，可自行增加行數**

文曄科技
WT MICROELECTRONICS
地址：台北縣中和市中正路 738 號 14 樓
14F., NO.738,CHUNG CHENG ROAD ., CHUNG HO CITY ,
TAIPEI HSIEN, TAIWAN, R.O.C
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承 認 書
APPROVAL SHEET

□	送測日期 ： TEST DATE	3-Jul-20
□	客戶名稱 ： CUSTOMER	技嘉科技股份有限公司
□	品 名 ： PART NAME	**AOZ5311NQI** **10IFD-505311-00R**
□	廠 牌 ： BRAND	**AOS**
□	包 裝 ： PACKAGE	**QFN-31**
□	承認日期 ： APPROVED DATE	3-Jul-20

AOZ5311NQI

High-Current, High-Performance DrMOS Power Module

General Description

The AOZ5311NQI is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High-Side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low-Side MOSFET has ultra low ON resistance to minimize conduction loss.

The AOZ5311NQI uses a PWM input for accurate control of the power MOSFETs switching activities, is compatible with 3V and 5V (CMOS) logic and supports Tri-State PWM.

A number of features are provided making the AOZ5311NQI a highly versatile power module. The boot-strap switch is integrated in the driver. The Low-Side MOSFET can be driven into diode emulation mode to provide asynchronous operation and improve light-load performance. The pin-out is also optimized for low parasitics, keeping their effects to a minimum.

Features

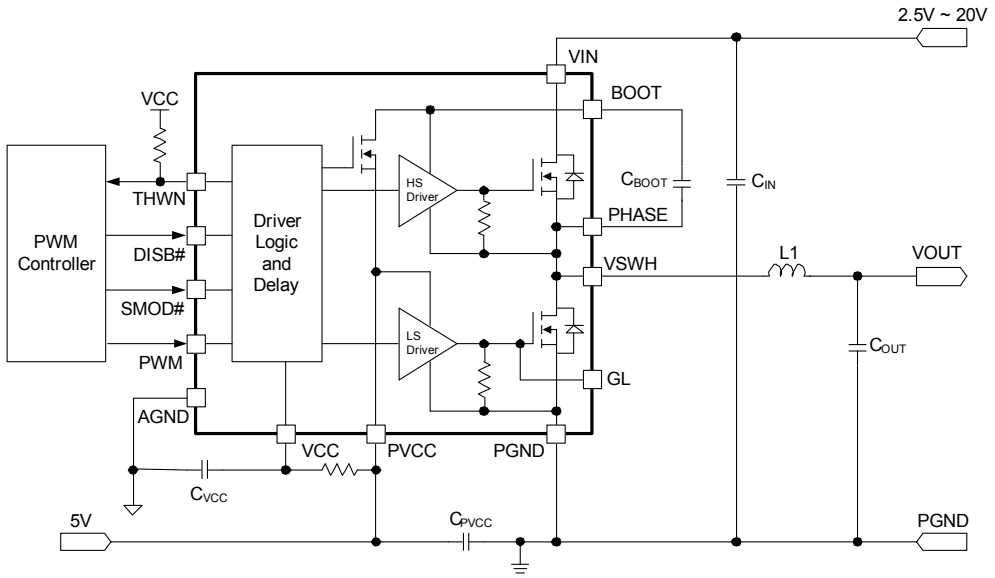
- 2.5V to 20V power supply range
- 4.5V to 5.5V driver supply range
- 50A continuous output current
  - Up to 80A for 10ms on pulse
  - Up to 120A for 10us on pulse
- Up to 2MHz switching operation
- 3V / 5V PWM / Tri-State input compatible
- Under-Voltage lockout protection
- SMOD# control for Diode Emulation / CCM operation
- Low Profile 5x5 QFN-31L package

Applications

- Memory and graphic cards
- VRMs for motherboards
- Point of load DC/DC converters
- Video gaming console

Green Product

Typical Application Circuit

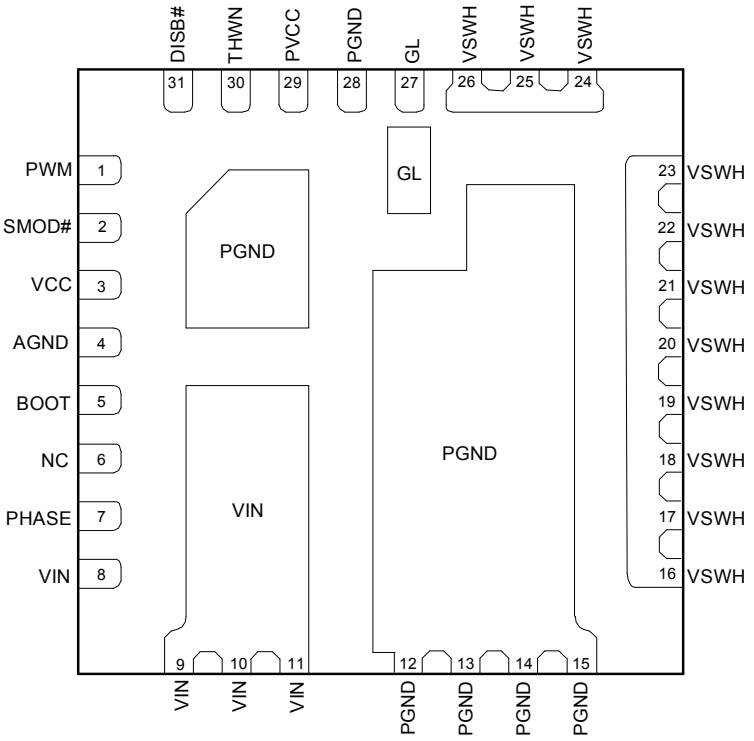


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5311NQI	-40°C to 125°C	QFN5x5-31L	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

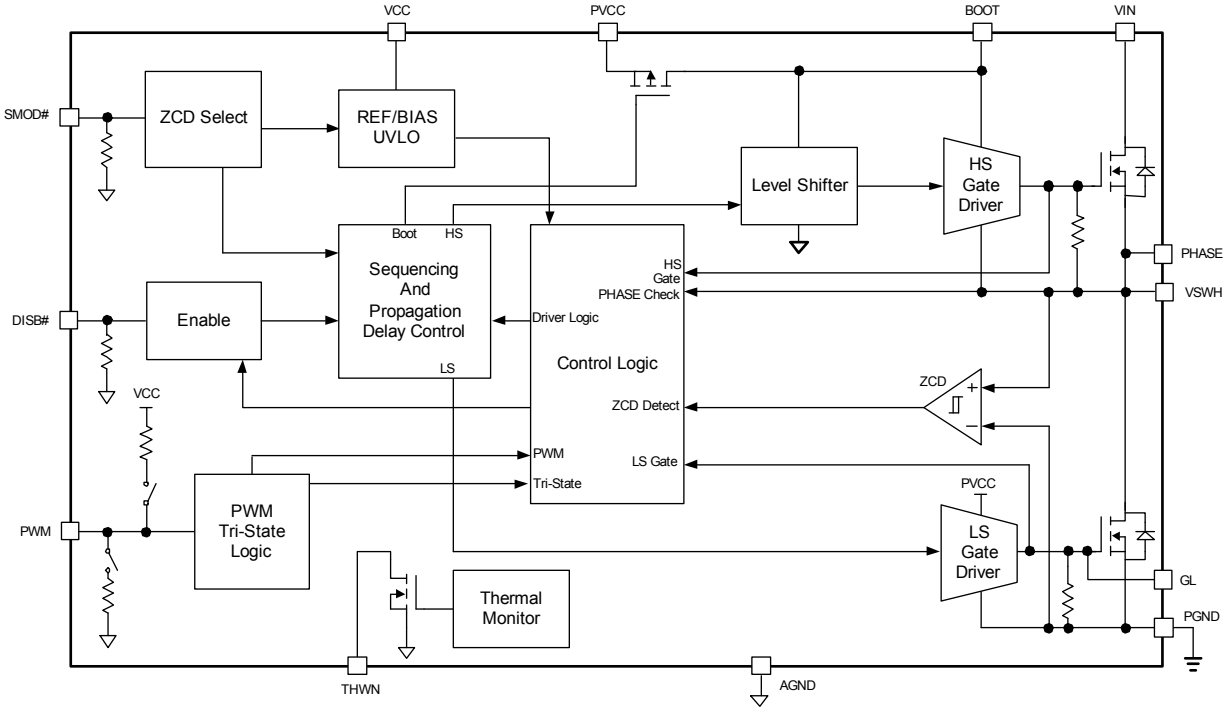


QFN5x5-31L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PWM	PWM input signal from the controller IC. When DISB#=0V, the internal resistor divider will be disconnected and this pin will be at high impedance.
2	SMOD#	Pull low to enable Discontinuous Mode of Operation (DCM), Diode Emulation or Skip Mode. There is an internal pull-down resistor to AGND.
3	VCC	5V Bias for Internal Logic Blocks. Ensure to position a 1µF MLCC directly between VCC and AGND (Pin 4).
4	AGND	Signal Ground.
5	BOOT	High-Side MOSFET Gate Driver supply rail. Connect a 100nF ceramic capacitor between BOOT and the PHASE (Pin 7).
6	NC	Internally connected to VIN paddle. It can be left floating (no connect) or tied to VIN.
7	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 5).
8, 9, 10, 11	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).
12, 13, 14, 15	PGND	Power Ground pin for power stage (Source connection of Low-Side MOSFET).
16,17,18,19, 20,21,22, 23, 24, 25, 26	VSWH	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal.
27	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
28	PGND	Power Ground pin for High-Side and Low-Side MOSFET Gate Drivers. Ensure to connect 1µF directly between PGND and PVCC (Pin 29).
29	PVCC	5V power rail for High-Side and Low-Side MOSFET gate drivers. Ensure to position a 1µF MLCC directly between PVCC to PGND (Pin 28).
30	THWN	Thermal warning indicator. This is an open−drain output. When the temperature at the driver IC die reaches the Over Temperature Threshold, this pin is pulled low.
31	DISB#	Output disable pin. When this pin is pulled to a logic low level, the IC is disabled. There is an internal pull−down resistor to AGND.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC, PVCC)	-0.3V to 7V
High Voltage Supply (VIN)	-0.3V to 25V
Control Inputs (PWM, SMOD#, DISB#)	-0.3V to (VCC+0.3V)
Output (THWN)	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 28V
Bootstrap Voltage Transient(1) (BOOT-PGND)	-8V to 30V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3V to 7V
BOOT Voltage Transient(1) (BOOT-PHASE/VSWH)	-0.3V to 9V
Switch Node Voltage DC (PHASE/VSWH)	-0.3V to 25V
Switch Node Voltage Transient(1) (PHASE/VSWH)	-8V to 33V
Low-Side Gate Voltage DC (GL)	(PGND-0.3V) to (PVCC+0.3V)
Low-Side Gate Voltage Transient(2) (GL)	(PGND-2.5V) to (PVCC+0.3V)
VSWH Current DC	50A
VSWH Current 10ms Pulse	80A
VSWH Current 10us Pulse	120A
Storage Temperature (T_S)	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
ESD Rating(3)	2kV

Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Peak voltages can be applied for 20ns per switching cycle.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	2.5V to 20V
Low Voltage/ MOSFET Driver Supply (VCC, PVCC)	4.5V to 5.5V
Control Inputs (PWM, SMOD#, DISB#)	0V to VCC
Output (THWN)	0V to VCC
Operating Frequency	200kHz to 2MHz

Electrical Characteristics[4]

T_A = 25°C to 125°C. Typical values reflect 25°C ambient temperature; VIN = 12V, VCC= PVCC= DISB# = 5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
GENERAL						
V_{IN}	Power Stage Power Supply		2.5		20	V
V_{CC}	Low Voltage Bias Supply	PVCC = VCC	4.5		5.5	V
$R_{\theta JC}$[5]	Thermal Resistance	Reference to High-Side MOSFET temperature rise		2.5		°C/W
$R_{\theta JA}$[5]		Freq = 300kHz. AOS Demo Board		12.5		°C/W
INPUT SUPPLY AND UVLO						
V_{CC_UVLO}	Under-Voltage Lockout	VCC Rising		3.5	3.9	V
V_{CC_HYST}		VCC Hysteresis		400		mV
I_{VCC}	Control Circuit Bias Current	DISB# = 0V		1		µA
		SMOD# = 5V, PWM = 0V		550		µA
		SMOD# = 0V, PWM = 0V		535		µA
		SMOD# = 0V, PWM =1.65V		430		µA
I_{PVCC}	Drive Circuit Operating Current	PWM = 400kHz, 20% Duty Cycle		13		mA
		PWM = 1MHz, 20% Duty Cycle		33		mA
PWM INPUT						
V_{PWMH}	Logic High Input Voltage		2.7			V
V_{PWML}	Logic Low Input Voltage				0.72	V
I_{PWM_SRC}	PWM Pin Input Current	PWM = 0V		-150		µA
I_{PWM_SNK}		PWM = 3.3V		150		µA
V_{TRI}	PWM Input Tri-State Window		1.35		1.95	V
V_{PMW_FLOAT}	PWM Tri-State Voltage Clamp	PWM = Floating		1.65		V
DISB# INPUT						
$V_{DISB\#\_ON}$	Enable Input Voltage		2.0			V
$V_{DISB\#\_OFF}$	Disable Input Voltage				0.8	V
$R_{DISB\#}$	DISB# Input Resistance	Pull-Down Resistor		850		kΩ
SMOD# INPUT						
$V_{SMOD\#\_H}$	Logic High Input Voltage		2.0			V
$V_{SMOD\#\_L}$	Logic Low Input Voltage				0.8	V
$R_{SMOD\#}$	SMOD# Input Resistance	Pull-Down Resistor		850		kΩ
GATE DRIVER TIMING						
t_{PDLU}	PWM to High-Side Gate	PWM: H⟶L, VSWH: H⟶L		30		ns
t_{PDLL}	PWM to Low-Side Gate	PWM: L → H, GL: H → L		25		ns
t_{PDHU}	Low-side to High-Side Gate Deadtime	GL: H → L, GH[6]: L → H		15		ns
t_{PDHL}	High-Side to Low-side Gate Deadtime	VSWH: H → 1V, GL: L → H		13		ns
t_{TSSHD}	Tri-State Shutdown Delay	PWM: L → V_{TRI}, GL: H → L and PWM: H → V_{TRI}, VSWH: H → L		25		ns
t_{TSEXIT}	Tri-State Propagation Delay	PWM: V_{TRI} → H, VSWH: L → H PWM: V_{TRI} → L, GL: L → H		35		ns
t_{LGMIN}	Low-Side Minimum On-Time	SMOD# = L		350		ns

Electrical Characteristics[4]

T_A = 25°C to 125°C. Typical values reflect 25°C ambient temperature; VIN = 12V, VCC= PVCC= DISB# = 5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
THERMAL NOTIFICATION[5]						
T_{JTHWN}	Junction Thermal Threshold	Temperature Rising		150		°C
T_{JHYST}	Junction Thermal Hysteresis			30		°C
V_{THWN}	THWN Pin Output Low	I_{THWN} = 0.5mA		60		mV
R_{THWN}	THWN Pull-Down Resistance			120		Ω

Notes:

4. All voltages are specified with respect to the corresponding AGND pin.
5. Characterization value. Not tested in production.
6. GH is the internal pin.

Timing Diagram

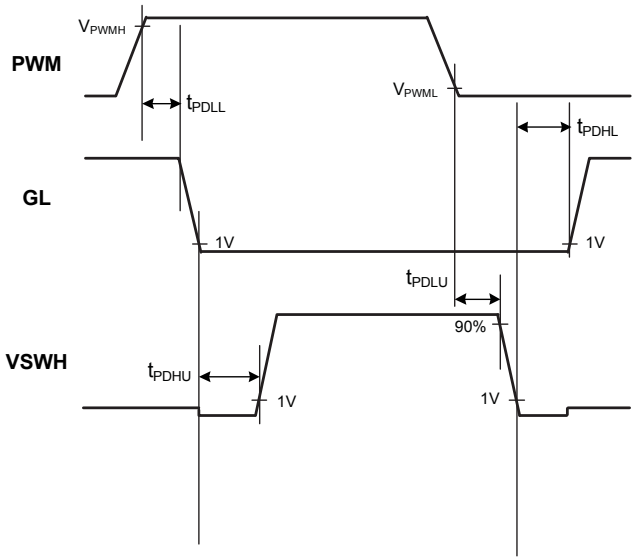


Figure 1. PWM Logic Input Timing Diagram

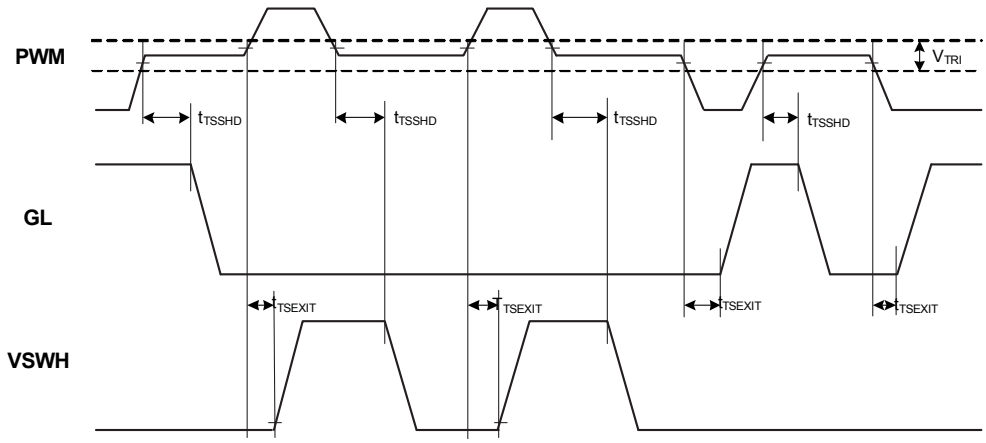


Figure 2. PWM Tri-State Hold Off and Exit Timing Diagram

Table 1. Input Control Truth Table

DISB#	SMOD#	PWM[7]	GH (Not a Pin)	GL
L	X	X	L	L
H	L	H	H	L
H	L	H to Tri-State	L	H, Forward I_L L, Reverse I_L
H	L	L to Tri-State	L	L
H	L	L	L	H
H	H	H	H	L
H	H	L	L	H
H	H	Tri-state	L	L

Note:

7. Diode emulation mode is activated when SMOD# is LOW and PWM transition from HIGH to Tri-State.Zero Cross Detection (ZCD) at I_L*$Rdson_{(LS)}$ = 0.5mV to turn off GL.

Typical Performance Characteristics

T_A = 25°C, VIN = 12V, PVCC = VCC = 5V, unless otherwise specified.

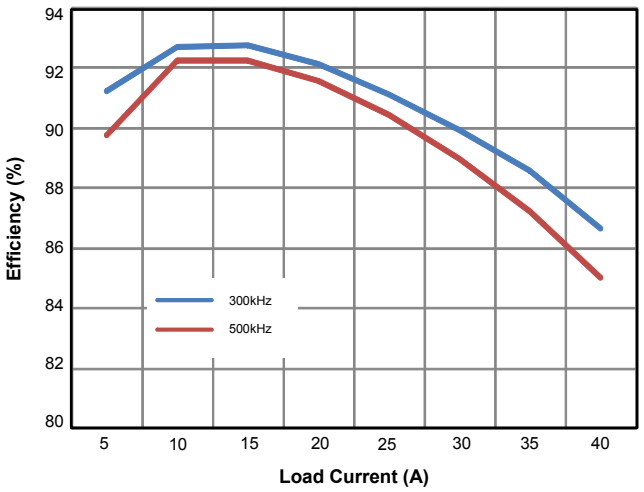


Figure 3. Efficiency vs. Load Current

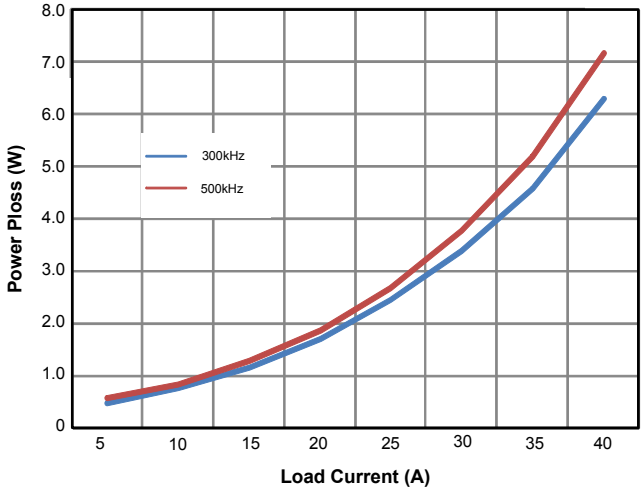


Figure 4. Power Loss vs. Load Current

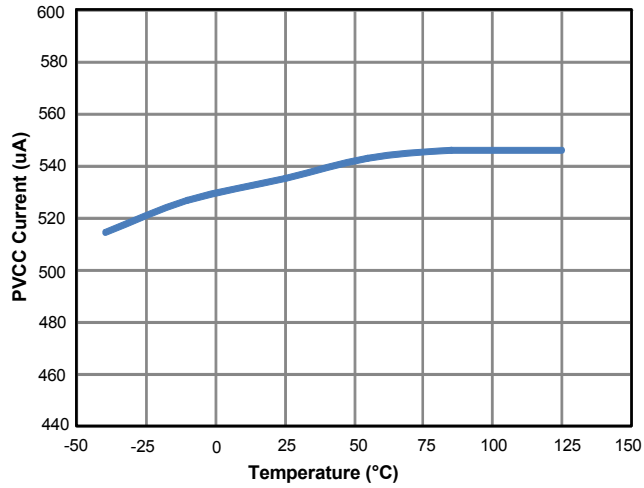


Figure 5. Supply Current (I_{PVCC}) vs. Temperature

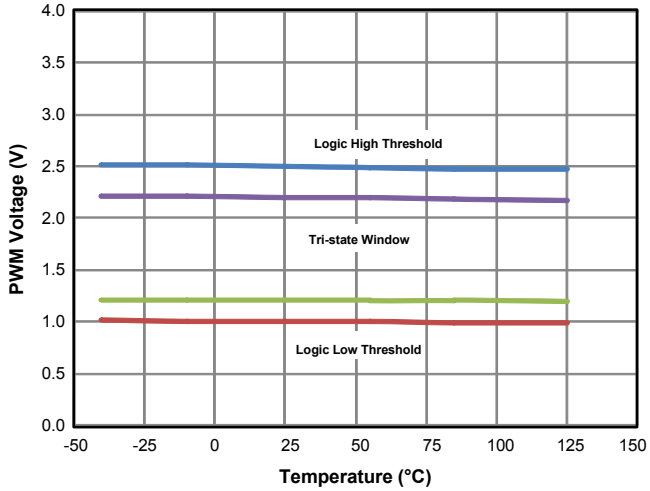


Figure 6. PWM Threshold vs. Temperature

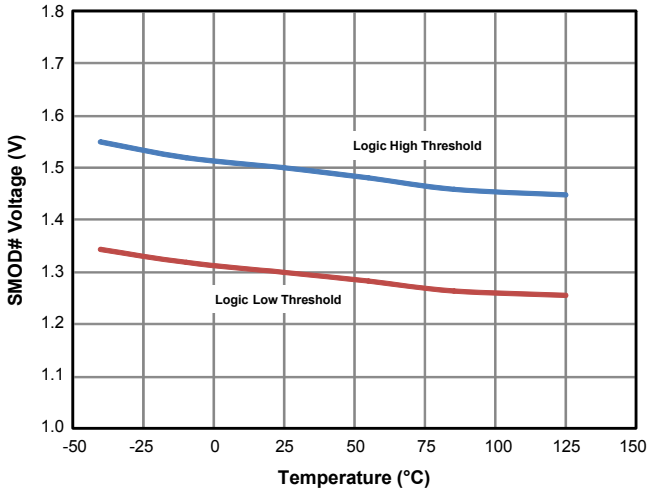


Figure 7. SMOD# Threshold vs. Temperature

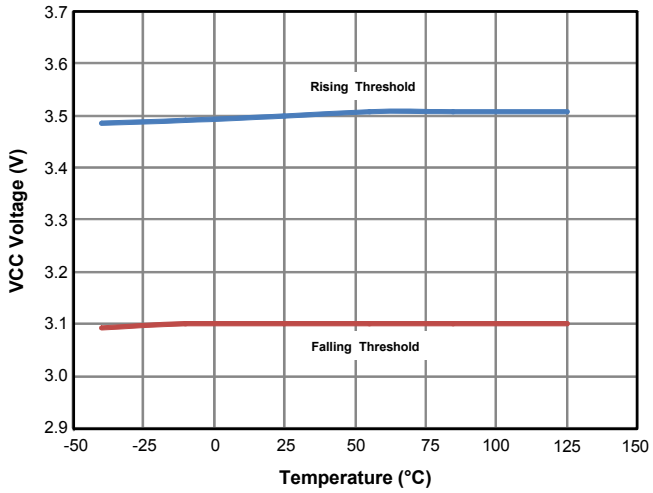


Figure 8. UVLO (VCC) Threshold vs. Temperature

Typical Performance Characteristics

T_A = 25°C, VIN = 12V, PVCC = VCC = 5V, unless otherwise specified.

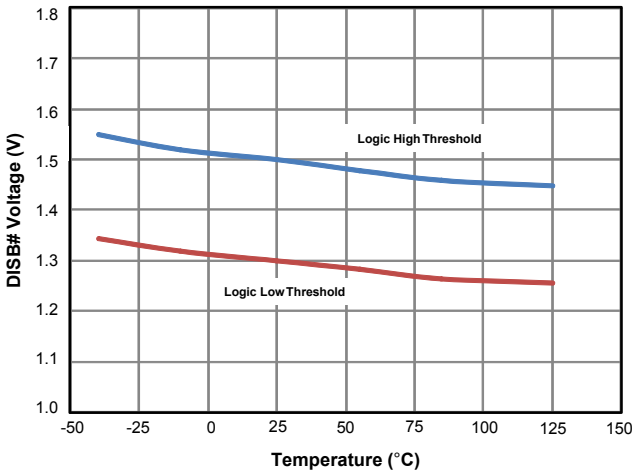


Figure 9. DISB# Thereshold vs. Temperature

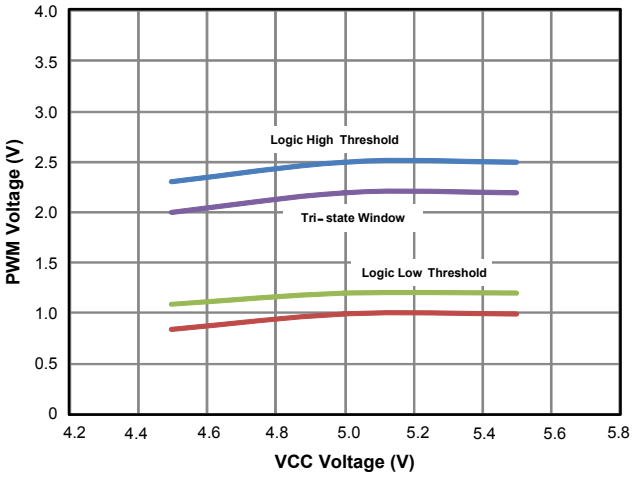


Figure 10. PWM Threshold vs. VCC Voltage

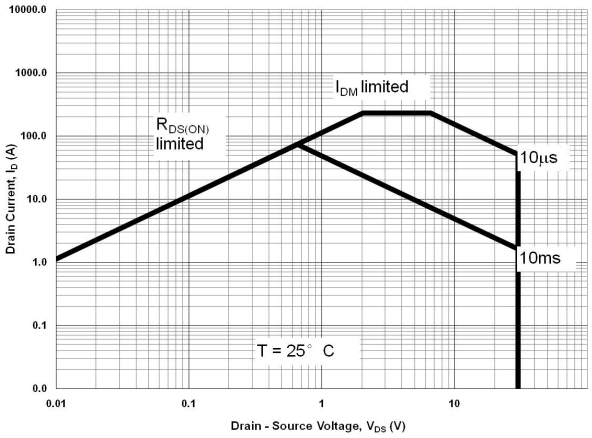


Figure 11. High-Side MOSFET SOA

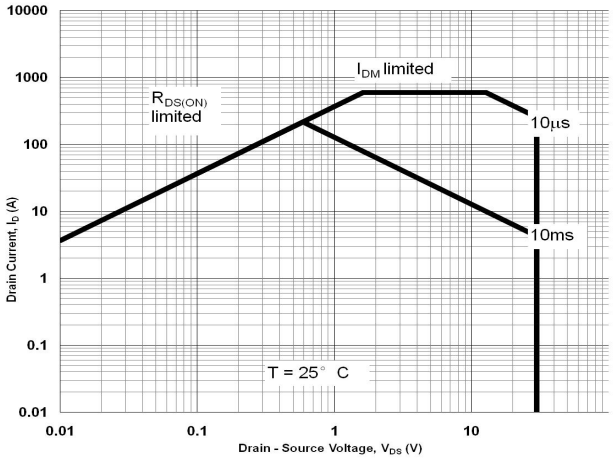


Figure 12. Low-Side MOSFET SOA

Application Information

AOZ5311NQI is a fully integrated power module designed to work over an input voltage range of 2.5V to 20V with a separate 5V supply for gate drive and internal control circuitry. The MOSFETs are individually optimized for efficient operation on both High-Side and Low-Side for a low duty cycle synchronous buck converter. High current MOSFET Gate Drivers are integrated in the package to minimize parasitic loop inductance for optimum switching efficiency.

Powering the Module and the Gate Drives

An external supply PVCC = 5V is required for driving the MOSFETs. The MOSFETs are designed with optimally customized gate thresholds voltages to achieve the most advantageous compromise between fast switching speed and minimal power loss. The integrated gate driver is capable of supplying large peak current into the Low-Side MOSFET to achieve fast switching. A ceramic bypass capacitor of 1μF or higher is recommended from PVCC (Pin 29) to PGND (Pin 28). The control logic supply VCC (Pin 3) can be derived from the gate drive supply PVCC (Pin 29) through an RC filter to bypass the switching noise (See Typical Application Circuit).

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor (100nF) between the BOOT (Pin 5) and the switching node PHASE (Pin 7). It is recommended that this capacitor C_{BOOT} should be connected to the device across Pin 5 and Pin 7 as close as possible. A bootstrap switch is integrated into the device to reduce external component count. An optional resistor R_{BOOT} in series with C_{BOOT} between 1Ω to 5Ω can be used to slow down the turn on speed of the High-Side MOSFET to achieve both short switching time and low VSWH switching node spikes at the same time.

Under-Voltage Lockout

AOZ5311NQI starts up to normal operation when VCC rises above the Under-Voltage Lock-Out (UVLO) threshold voltage. The UVLO release is set at 3.5V typically. Since the PWM control signal is provided from an external controller or a digital processor, extra caution must be taken during start up. AOZ5311NQI must be powered up before PWM input is applied.

Normal system operation begins with a soft start sequence by the controller to minimize in-rush current during start up. Powering the module with a full duty cycle PWM signal may lead to many undesirable consequences due to excessive power. AOZ5311NQI provides some protections such as UVLO and thermal monitor. For system level protection, the PWM controller should monitor the current output and protect the load under all possible operating and transient conditions.

Disable (DISB#) Function

The AOZ5311NQI can be enabled and disabled through DISB# (Pin 31). The driver output is disabled when DISB# input is connected to AGND. The module would be in standby mode with low quiescent current of less than 1μA. The module will be active when DISB# is connected to VCC Supply. The driver output will follow PWM input signal. A weak pull-down resistor is connected between DISB# and AGND.

Power up sequence design must be implemented to ensure proper coordination between the module and external PWM controller for soft start and system enable/disable. It is recommended that the AOZ5311NQI should be disabled before the PWM controller is disabled. This would make sure AOZ5311NQI will be operating under the recommended conditions.

Input Voltage VIN

AOZ5311NQI is rated to operate over a wide input range from 2.5V to 20V. For high current synchronous buck converter applications, large pulse current at high frequency and high current slew rates (di/dt) will be drawn by the module during normal operation. It is strongly recommended to place a bypass capacitor very close to the package leads at the input supply (VIN). Both X7R or X5R quality surface mount ceramic capacitors are suitable.

The High-Side MOSFET is optimized for fast switching by using low gate charges (Q_G) device. When the module is operated at high duty cycle ratio, conduction loss from the High-Side MOSFET will be higher. The total power loss for the module is still relatively low but the High-Side MOSFET higher conduction loss may have higher temperature. The two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation. It is recommended that worst case junction temperature be measured for both High-Side MOSFET and Low-Side MOSFET to ensure that they are operating within Safe Operating Area (SOA).

PWM Input

AOZ5311NQI is compatible with 3V and 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives. AOZ5311NQI is compatible with 3V and 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives.

The PWM is also compatible with Tri-State input. When the PWM output from the external PWM controller is in high impedance or not connected both High-Side and Low-Side MOSFETs are turned off and VSWH is in high impedance state. Table 2 shows the thresholds level for high-to-low and low-to-high transitions as well as Tri-State window.

There is a Hold-off Delay between the corresponding PWM Tri-State signal and the MOSFET gate drivers to prevent spurious triggering of Tri-State mode which may be caused by noise or PWM signal glitches. The Hold-off Delay is typically 25ns.

Table 2. PWM Input and Tri-State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5311NQI	2.7 V	0.72 V	1.35 V	1.95 V

Note: See Figure 2 for propagation delays and tri-state window.

Diode Mode Emulation of Low Side MOSFET (SMOD#)

AOZ5311NQI can be operated in the diode emulation or pulse skipping mode using SMOD# (Pin 2). This enables the converter to operate in asynchronous mode during start up, light load or under pre-bias conditions.

When SMOD# is high, the module will operate in Continuous Conduction Mode (CCM). The Driver logic will use the PWM signal and generate both the High-Side and Low-Side complementary gate drive outputs with minimal anti-overlap delays to avoid cross conduction.

When SMOD# is low, the module can operate in Discontinuous Conduction Mode (DCM). The High-Side MOSFET gate drive output is not affected but Low-Side MOSFET will enter diode emulation mode. See Table 2 for all truth table for DISB#, SMOD# and PWM inputs.

Gate Drives

AOZ5311NQI has an internal high current high speed driver that generates the floating gate driver for the High-Side MOSFET and a complementary driver for the Low-Side MOSFET. An internal shoot through protection scheme is implemented to ensure that both MOSFETs cannot be turned on at the same time. The operation of PWM signal transition is illustrated as below.

1. PWM from logic Low to logic High

When the falling edge of Low-Side Gate Driver output GL goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHU}), the complementary High-Side Gate Driver output GH is turned on.

2. PWM from logic High to logic Low

When the falling edge of switching node VSWH goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHL}), the complementary Low-Side Gate Driver output GL is turned on

This mechanism prevents cross conduction across the input bus line VIN and PGND. The anti-overlap circuit monitors the switching node VSWH to ensure a smooth transition between the two MOSFETs under any load transient conditions.

Thermal Warning (THWN)

The driver IC temperature is internally monitored and an thermal warning flag at THWN (Pin 30) is asserted if it exceeds 150°C. This warning flag is reset when the temperature drop back to 120°C. THWN is an open drain output that is pulled to AGND to indicate an over-temperature condition. It should be connected to VCC through a resistor for monitoring purpose. The device will not power down during the over temperature condition.

PCB Layout Guidelines

AOZ5311NQI is a high current module rated for operation up to 2MHz. This requires fast switching speed to keep the switching losses and device temperatures within limits. An integrated gate driver within the package eliminates driver-to-MOSFET gate pad parasitic of the package or on PCB.

To achieve high switching speeds, high levels of slew rate (dv/dt and di/dt) will be present throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the path of the primary switching current loop formed by the High-Side MOSFET, Low-Side MOSFET, and the input bypass capacitor C_{IN}. The PCB design is greatly simplified by the optimization of the AOZ5311NQI pin out. The power inputs of VIN and PGND are located adjacent to each other and the input bypass capacitors C_{IN} should be placed as close as possible to these pins. The area of the secondary switching loop is formed by Low-Side MOSFET, output inductor L1, and output capacitor C_{OUT} is the next critical requirement. This requires second layer or “Inner 1” to be the PGND plane. VIAs should then be placed near PGND pads.

While AOZ5311NQI is a highly efficient module, it is still dissipating significant amount of heat under high power conditions. Special attention is required for thermal design. MOSFETs in the package are directly attached to individual exposed pads (VIN and PGND) to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal relief

pads should be placed to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the high voltage system input, is desirable and VIAs should be provided near the device to connect the VIN pads to the power plane. Significant amount of heat can also be dissipated through multiple PGND pins. A large copper area connected to the PGND pins in addition to the system ground plane through VIAs will further improve thermal dissipation.

As shown on Figure. 13, the top most layer of the PCB should comprise of wide and exposed copper area for the primary AC current loop which runs along VIN pad originating from the input capacitors C10, C11 and C12 that are mounted to a large PGND pad. They serve as thermal relief as heat flows down to the VIN exposed pad that fan out to a wider area. Adding VIAs will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

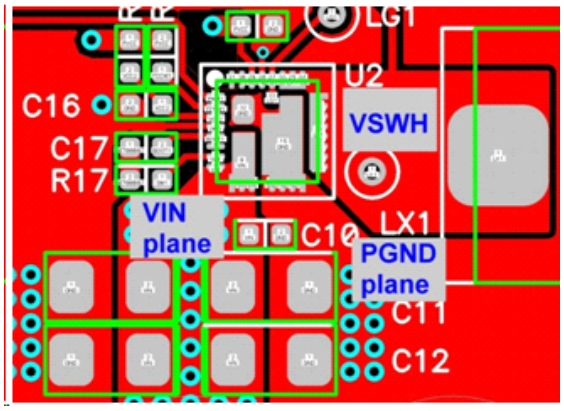


Figure 13. Top Layer of Demo Board, VIN, VSWH and PGND Copper Planes

As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spike appear at the VSWH terminal which are caused by the large internal di/dt produced by the package parasitic. To minimize the effects of this interference at the VSWH terminal, at which the main inductor L1 is mounted, size just enough for the inductor to physically fit. The goal is to employ the least amount of copper area for this VSWH terminal, only enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH pad or inductor terminal is voided and the shape of this void is replicated descending down through the rest of the layers. Refer to Figure 14.

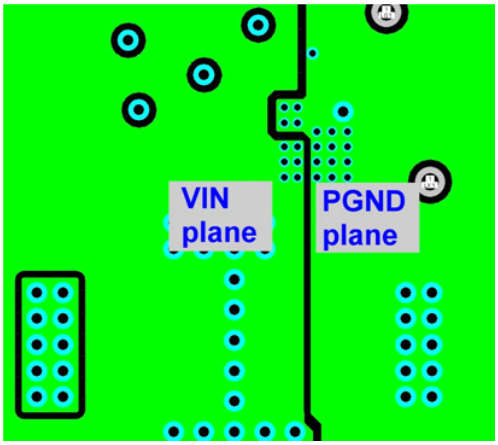
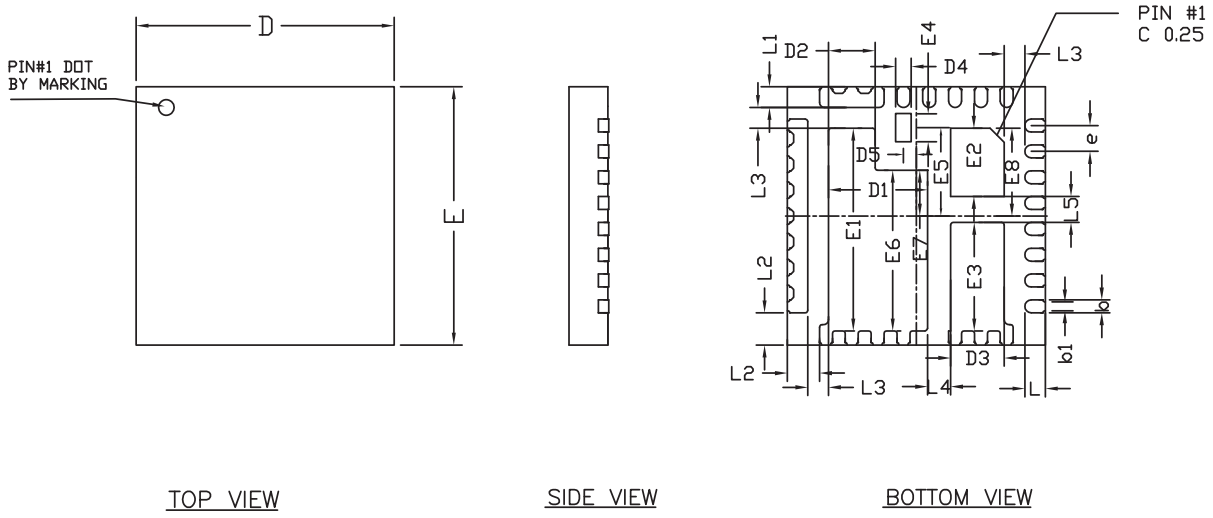


Figure 14. Bottom Layer PCB layout, VSWH Copper Plane Voided on Descending Layers

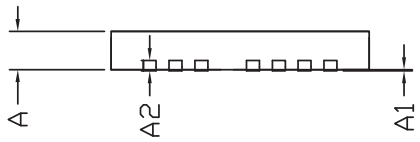
Positioning via through the landing pattern of the VIN and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer. (See RECOMMENDED LANDING PATTERN AND VIA PLACEMENT section).

The exposed pads dimensional footprint of the 5x5 QFN package is shown on the package dimensions page. For optimal thermal relief, it is recommended to fill the PGND and VIN exposed landing pattern with 10mil diameter VIAs. 10mil diameter is a commonly used via diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.

Package Dimensions, QFN5x5A-31L, EP3_S

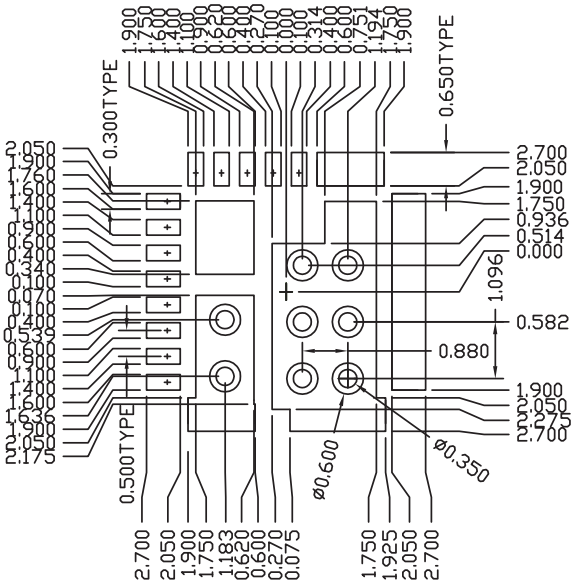


TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



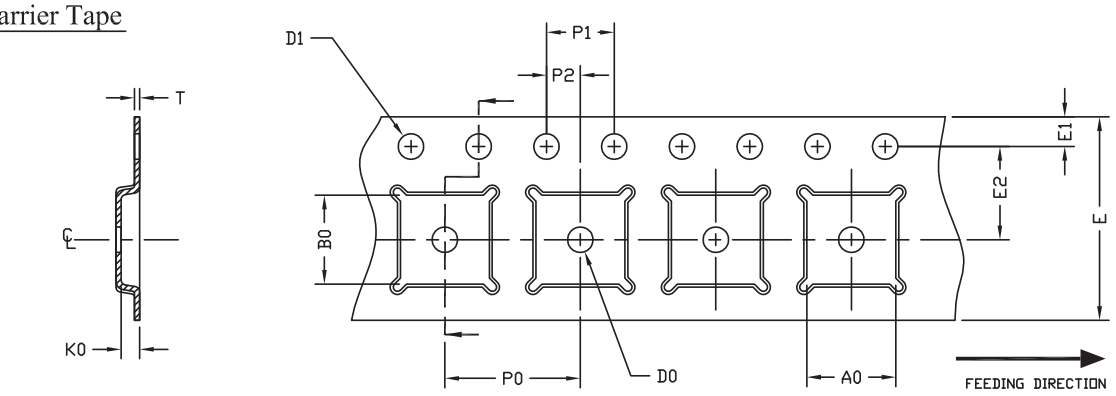
SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	-	0.050	0.000	-	0.002
A2	0.200REF			0.008REF		
D	4.900	5.000	5.100	0.193	0.197	0.201
E	4.900	5.000	5.100	0.193	0.197	0.201
D1	1.870	1.920	1.970	0.074	0.076	0.078
D2	0.850	0.900	0.950	0.033	0.035	0.037
D3	0.990	1.040	1.090	0.039	0.041	0.043
D4	0.250	0.300	0.350	0.010	0.012	0.014
D5	0.200	0.250	0.300	0.008	0.010	0.012
E1	3.875	3.925	3.975	0.153	0.155	0.156
E2	1.270	1.320	1.370	0.050	0.052	0.054
E3	2.050	2.100	2.150	0.081	0.083	0.085
E4	0.500	0.550	0.600	0.020	0.022	0.024
E5	1.661	1.711	1.761	0.065	0.067	0.069
E6	3.061	3.111	3.161	0.121	0.122	0.124
E7	0.836	0.886	0.936	0.033	0.035	0.037
E8	1.650	1.700	1.750	0.065	0.067	0.069
L	0.350	0.400	0.450	0.014	0.016	0.018
L1	0.350	0.400	0.450	0.014	0.016	0.018
L2	0.575	0.625	0.675	0.023	0.025	0.027
L3	0.350	0.400	0.450	0.014	0.016	0.018
L4	0.400	0.450	0.500	0.016	0.018	0.020
L5	0.450	0.500	0.550	0.018	0.020	0.022
b	0.200	0.250	0.300	0.008	0.010	0.012
b1	0.130	0.180	0.230	0.005	0.007	0.009
e	0.500BSC			0.020BSC		

UNIT: mm

NOTE
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN5x5A-31L, EP3_S

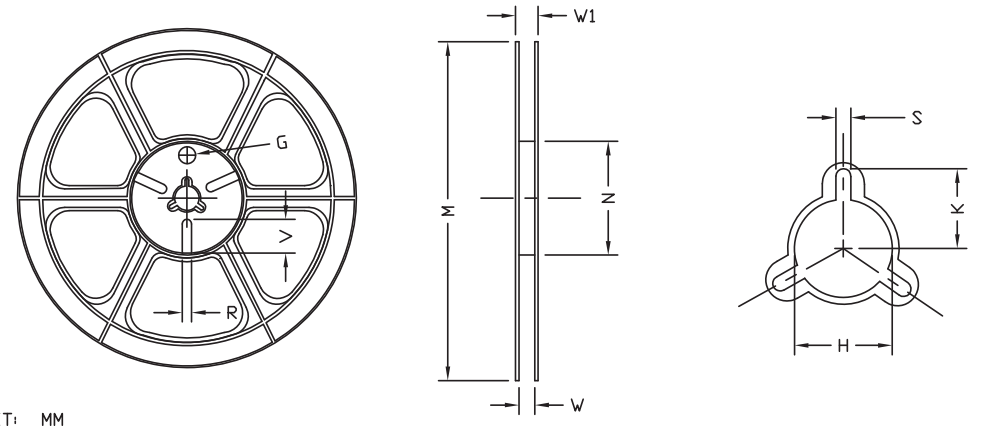
Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 −0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

Reel

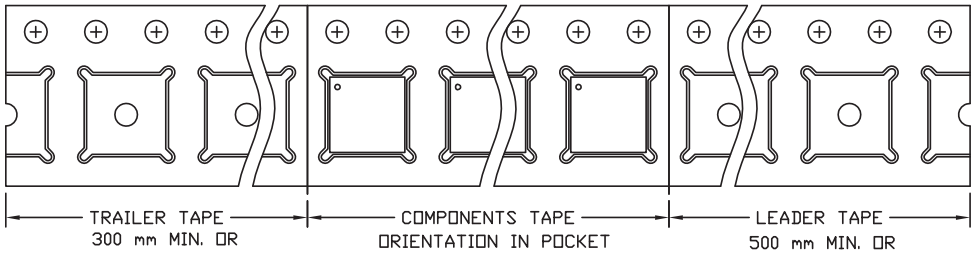


UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0 −0.0	17.0 +2.6 −1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

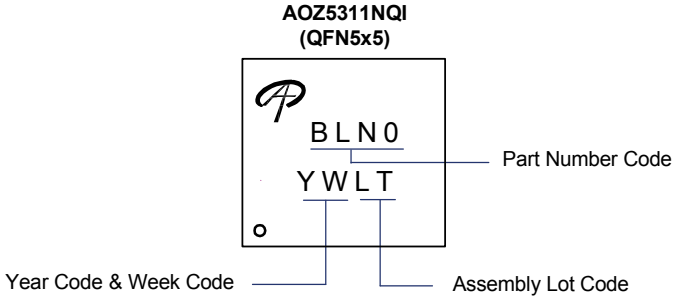
Tape

Leader / Trailer & Orientation



Unit Per Reel: 3000pcs

Part Marking



ALPHA & OMEGA SEMICONDUCTOR

Document No.	PD-03311
Version	A
Title	AOZ5311NQI Marking Description

QFN5x5A Power IC PACKAGE MARKING DESCRIPTION

Green product

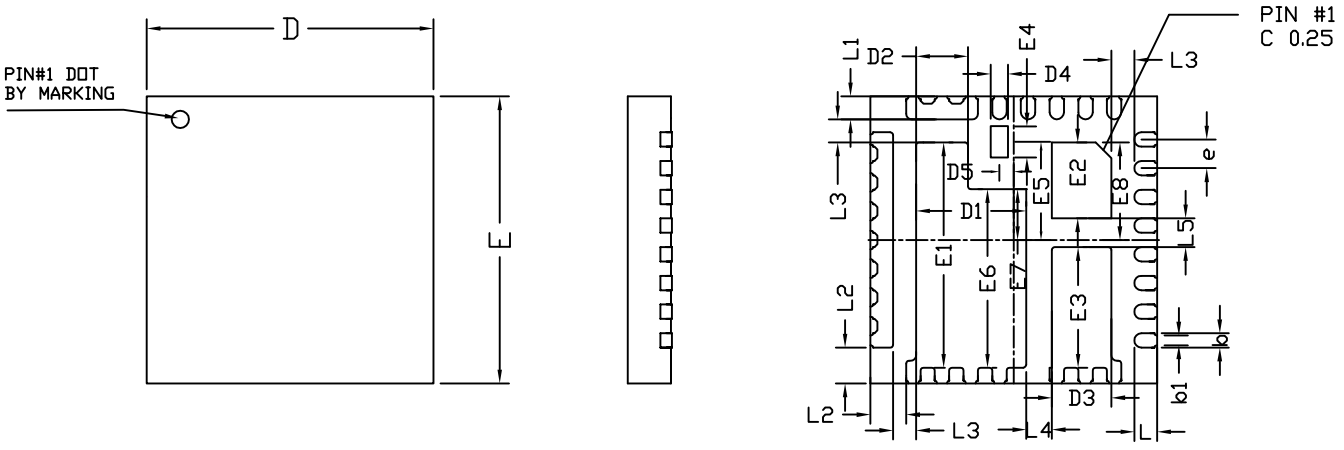
NOTE:
LOGO - AOS Logo
BLN0 - Part number code
Y - Year code
W - Week code
L&T - Assembly lot code

PART NO.	DESCRIPTION	CODE
AOZ5311NQI	Green product	BLN0

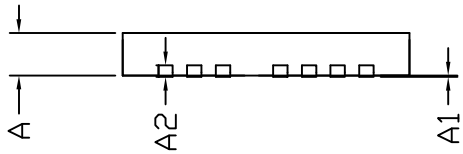
ALPHA & OMEGA SEMICONDUCTOR

Document No.	PO-00237
Version	I

QFN5x5A_31L_EP3_S PACKAGE OUTLINE

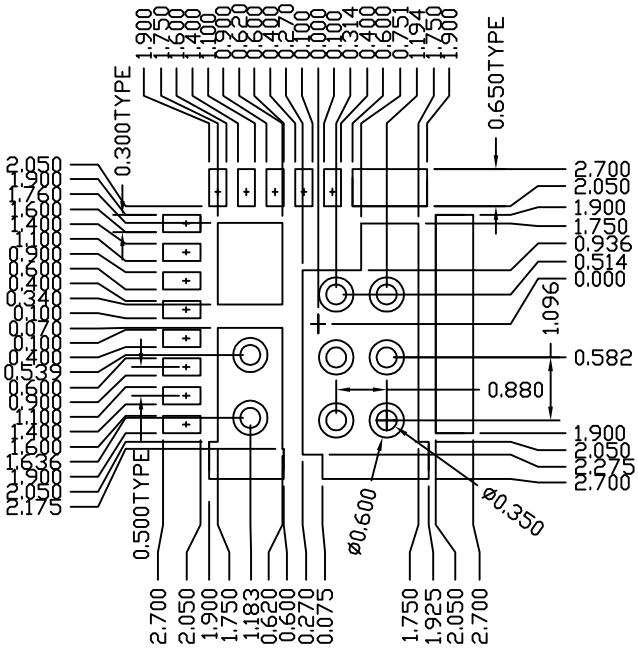


TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	-	0.050	0.000	-	0.002
A2		0.200REF			0.008REF	
D	4.900	5.000	5.100	0.193	0.197	0.201
E	4.900	5.000	5.100	0.193	0.197	0.201
D1	1.870	1.920	1.970	0.074	0.076	0.078
D2	0.850	0.900	0.950	0.033	0.035	0.037
D3	0.990	1.040	1.090	0.039	0.041	0.043
D4	0.250	0.300	0.350	0.010	0.012	0.014
D5	0.200	0.250	0.300	0.008	0.010	0.012
E1	3.875	3.925	3.975	0.153	0.155	0.156
E2	1.270	1.320	1.370	0.050	0.052	0.054
E3	2.050	2.100	2.150	0.081	0.083	0.085
E4	0.500	0.550	0.600	0.020	0.022	0.024
E5	1.661	1.711	1.761	0.065	0.067	0.069
E6	3.061	3.111	3.161	0.121	0.122	0.124
E7	0.836	0.886	0.936	0.033	0.035	0.037
E8	1.650	1.700	1.750	0.065	0.067	0.069
L	0.350	0.400	0.450	0.014	0.016	0.018
L1	0.350	0.400	0.450	0.014	0.016	0.018
L2	0.575	0.625	0.675	0.023	0.025	0.027
L3	0.350	0.400	0.450	0.014	0.016	0.018
L4	0.400	0.450	0.500	0.016	0.018	0.020
L5	0.450	0.500	0.550	0.018	0.020	0.022
b	0.200	0.250	0.300	0.008	0.010	0.012
b1	0.130	0.180	0.230	0.005	0.007	0.009
e		0.500BSC			0.020BSC	

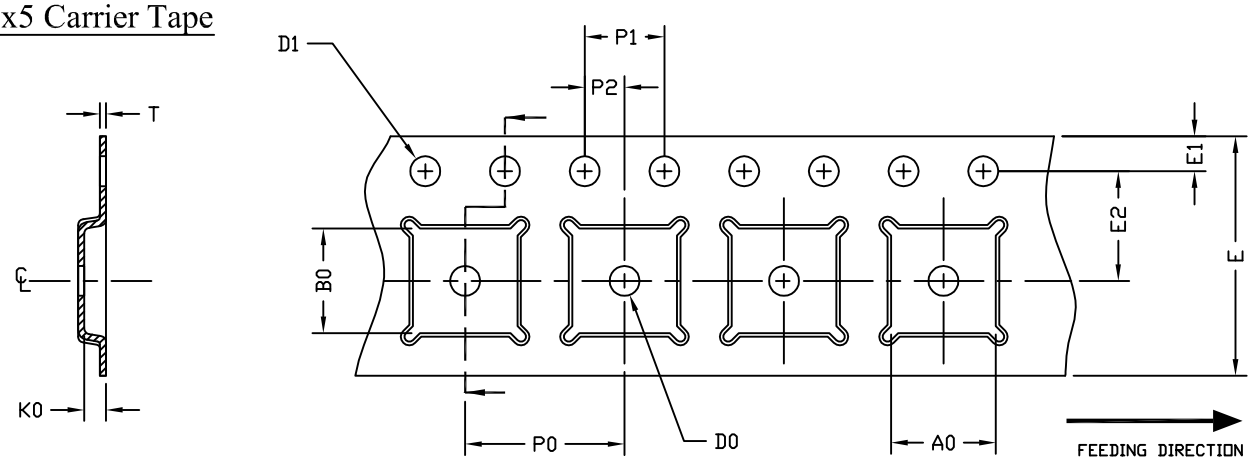
UNIT: mm

NOTE
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

ALPHA & OMEGA SEMICONDUCTOR

QFN5x5 Tape and Reel Data

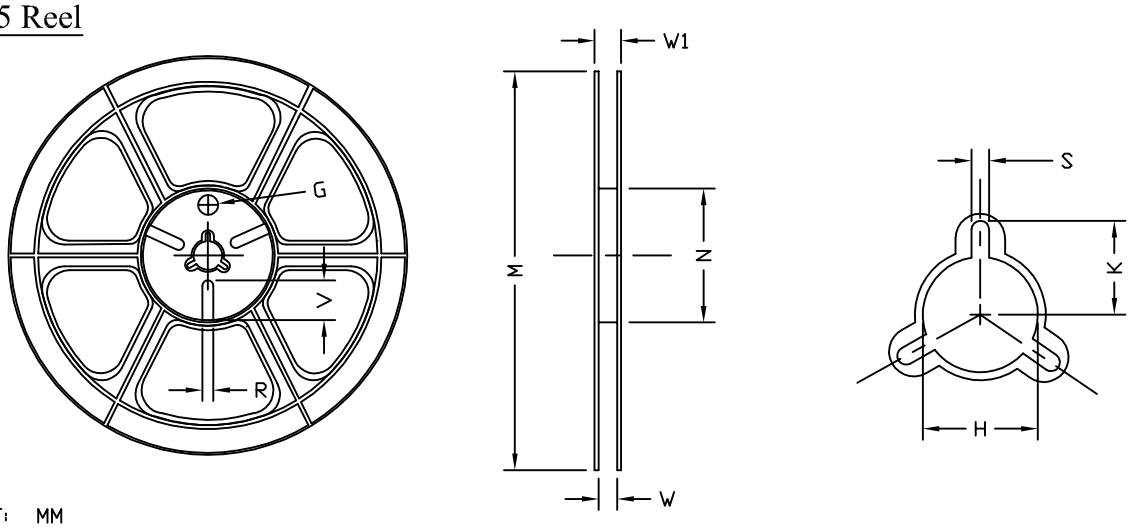
QFN5x5 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 $^{+0.1}_{-0.0}$	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

QFN5x5 Reel



UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 $^{+2.0}_{-0.0}$	17.0 $^{+2.6}_{-1.2}$	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

ALPHA & OMEGA SEMICONDUCTOR

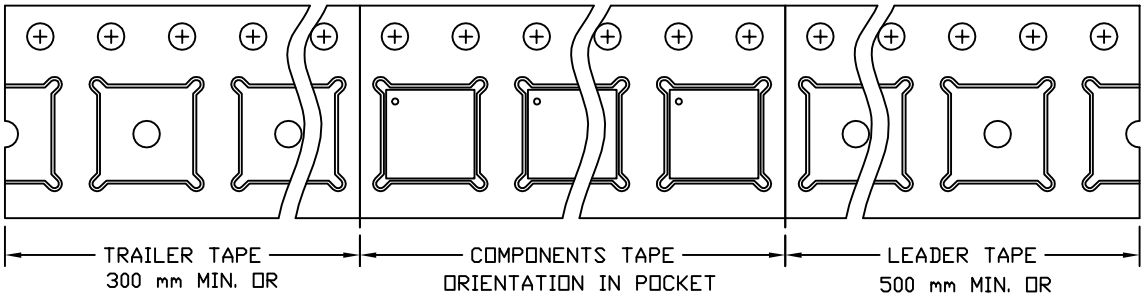
QFN5x5 Tape and Reel Data

QFN5x5 Tape

Leader / Trailer
& Orientation

NORMAL

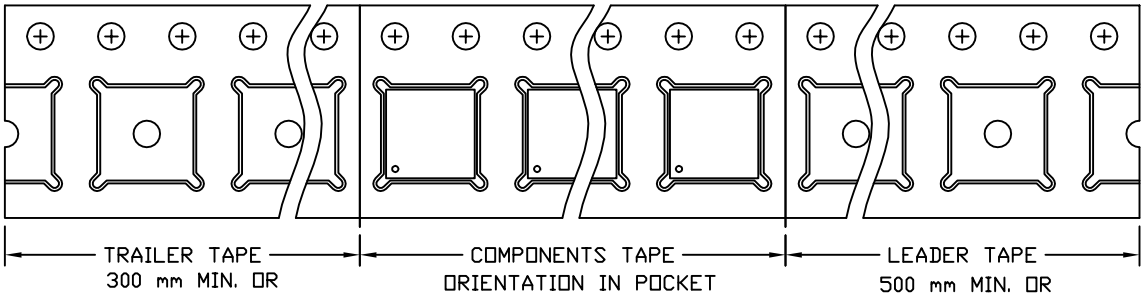
Unit Per Reel:
3000pcs



Leader / Trailer
& Orientation

SPECIAL

Unit Per Reel:
3000pcs



AOS Semiconductor
Product Reliability Report

AOZ5311NQI rev 1.1

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

475 Oakmead Parkway
Sunnyvale, CA 94085
United States

Tel: (408)830-9742
www.aosmd.com

May, 2019

This AOS product reliability report summarizes the qualification results for AOZ5311NQI in QFN5x5 - 31L package.

Review of the electrical test results confirmed that AOZ5311NQI passes AOS quality and reliability requirements for final product and package release.

I. Table of Contents:

General Description:

AOZ5311NQI is a high-efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. AOZ5311NQI is available in a tiny 5mm x 5mm 31-pin QFN package and is rated over a -40°C to +125°C operating temperature range.

Absolute Maximum Ratings	
Parameter	
Low Voltage Supply VCC, PVCC	-0.3V to 7V
High Voltage Supply VIN	-0.3V to 25V
Control Inputs PWM, FCCM	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT - PGND)	-0.3V to 32V
Bootstrap Voltage DC (BOOT - VSWH)	-0.3V to 7V
Bootstrap Voltage Transient (1) (BOOT - VSWH)	-0.3V to 9V
Switching Node Voltage DC VSWH	-0.3V to 25V
Switching Node Voltage Transient (2) VSWH	-8V to 33V
Low Side Gate Voltage DC GL	(PGND-0.3V) to (PVCC+0.3V)
Low Side Gate Voltage Transient (2) GL	(PGND-2.5V) to (PVCC+0.3V)
Storage Temperature (Ts)	-65°C to 150°C
Max Junction Temperature (Tj)	150°C
ESD Rating (3)	2kV
Recommended Operating Ratings	
High Voltage Supply VIN, VSWH	4.5V to 20V
Low Voltage Supply, Logic VCC, PVCC	4.5V to 5.5V

Note:

(1) Peak voltages can be applied for 10ns per switching cycle
(2) Peak voltages can be applied for 20ns per switching cycle
(3) Devices are inherently ESD sensitive. Handling precautions are required. Human Body Model rating: 1.5 kΩ in series with 100 pF

ALPHA & OMEGA SEMICONDUCTOR

II. Package and Die Information:

Product ID	AOZ5311NQI
Package Type	QFN5x5-31L
Die Size	IC: 960x1040 um2 HS MOSFET: 1150x1820 um2 LS MOSFET: 1800x2250 um2
Die attach material	IC: non-conductive epoxy MOSFETs: solder paste
Bond wire	Au, 1.0 mil
Mold Material	EME-G700HC D14*5.8g
Lead Plating	Pure Sn
MSL	Level 1

III. Qualification Tests Requirements

- AOZ5311NQI is a derivative product
  - 3 lots 1000hrs HTOL
  - 3 lots preconditioning, 96hr PCT, 96hr uHAST, 1000 cycle TC, 1000hr HTS
  - 1 lot HBM, CDM ESD, Latchup
  - 2 lots 1000hr HTRB, HTGB (MOSFETs, derivative qualification)
  - 3x IR reflow + 250 cycle TC

IV. Qualification Tests Result

Test Item	Test Condition	Sample Size	Result	Comment
HTOL	**Per JESD 22-A108B** **V_{IN} = 25V** **T_J = 150˚C**	**3 lots (80 /lot)**	**pass 1000hrs**	
ESD	**JESD 22-A114E (HBM)** **JESD 22-A115A (MM)** **JESD 22-C101C (CDM)**	**3 units**	**pass**	**2.0kV (HBM)** **200V (MM)** **1.0kV (CDM)**
Latch-up	**Per JESD 78A**	**6 units**	**pass**	**± 100mA**
Power Cycling	**V_{IN} = 19V, V_{OUT} = 1.0V, F_{SW} = 800kHz, I_{OUT} = 30A, VCC cycled 0V-5V**	**10 units**	**pass**	**35hr,** **>63k cycles**
HTGB (MOSFETs)	**Temp = 150˚C** **V_{GS} = 12V**	**1 lot HS MOSFET (77 pcs)** **1 lot LS MOSFET (77 pcs)** **9 lots MOSFET (77/lot)**	**pass 1000hrs** **pass 1000hrs** **pass 1000hrs**	**Derivative process** **Derivative process** **Platform process**
HTRB (MOSFETs)	**Temp = 150˚C** **V_{DS} = 25V**	**1 lot HS MOSFET (77 pcs)** **1 lot LS MOSFET (77 pcs)** **9 lots MOSFET (77/lot)**	**pass 1000hrs** **pass 1000hrs** **pass 1000hrs**	**Derivative process** **Derivative process** **Platform process**
H3TRB (MOSFETs)	**T_A = 85˚C, 85% RH, V_{DS} = 25V**	**3 lots (77/lot)**	**Pass 1000hr**	**Platform process**
HAST (MOSFETs)	**130˚C +/- 2˚C, 85% RH, 33.3 psi**	**3 lots (77/lot)**	**pass 96hrs**	**Platform process**
Power Cycling (MOSFETs)	**T_A = 25˚C, T_J = 125˚C**	**3 lots (77/lot)**	**pass 15k cycles**	**Platform process**

Test Item	Test Condition	Sample Size	Result	Comment
3x IR reflow and 250 Temperature Cycles	**3x IR reflow @ 260˚C; TC test condition: -65 ˚C to +150˚C, air to air (2cyc/hr)**	**3 lots (3000 /lot)**	**pass**	
Pre-Conditioning (MSL1)	**Per JESD 22-A113 85˚C, 85% RH, 3 cycle reflow @ 260˚C**	**3 lots (308 /lot)**	**pass MSL1**	
PCT	**121˚C, 15 ± 1 PSI, RH = 100%**	**3 lots (77 /lot)**	**pass 96hrs**	
UHAST	**130 +/- 2˚C, 85% RH, 33.3 psi**	**3 lots (77/lot)**	**pass 96hrs**	
Temperature Cycle	**-65˚C to +150˚C, air to air (2cyc/hr)**	**3 lots (77 /lot)**	**pass 1000 cycles**	
HTS	**T_A = +150˚C**	**3 lots (77 /lot)**	**pass 1000hrs**	

V. Reliability Evaluation

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size of the product. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

FIT rate (failures per billion device hours): 0.150
MTTF = 6,649.6 million hrs
Condition: V_o = 20V, T_o = 55°C, $V_{s(DriverIC)}$ = 28V, $V_{s(MOSFET)}$ = 25V and T_s = 150°C
Sample Size: MOSFET = 6,153, Driver IC = 3,874

The failure rate (λ) is calculated as follows:
$\lambda = \chi^2[CL,(2f+2)]\ /2 \times [1/(SS \times t \times AF)]$; [equation 1] where CL = % of confidence level
f = number of failure
SS = sample size
t = stress time

Looking up the χ^2 /2 table for zero failure (burn-in) with 60% confidence, the value of $\chi^2[CL,(2f+2)]$ /2 is 0.92.

The Acceleration Factor (AF) is calculated from the following formula (both temperature and voltage acceleration factors are used in the final acceleration factor calculation) :
$AF = AF_T \times AF_V = \exp[(E_a/k) \times (1/T_0-1/T_s)] \times \exp[\beta (Vs-Vo)]$ where
E_a = activation energy
k = Boltzmann constant
T_o = operating T_J
T_s = stress T_J
V_s = stress voltage
V_o = operating voltage
β = voltage acceleration coefficient

Assuming typical operating environment, V_o = 20V, T_o = 55°C, E_a = 0.7eV, $V_{s(DriverIC)}$ = 28V, $V_{s(MOSFET)}$ = 25V, T_s = 150°C, β = 0.5 (silicon defect)

$$AF(DriverIC) = \exp\left[\left(\frac{0.7}{8.617E-5}\right)\bullet\left(\frac{1}{273+55}-\frac{1}{273+150}\right)\right]\bullet\exp[0.5\bullet(28V-20V)]$$

$$AF(MOSFET) = \exp\left[\left(\frac{0.7}{8.617E-5}\right)\bullet\left(\frac{1}{273+55}-\frac{1}{273+150}\right)\right]\bullet\exp[0.5\bullet(25V-20V)]$$

Substituting the values in equation 1, we have $\lambda = 2\bullet\lambda(MOSFET) + \lambda(DriverIC) =$

$$0.92 \bullet \frac{2}{Sample\ \ Size \bullet Stress\ \ Duration\ \bullet AF(MOSFET)} + \frac{1}{sample\ \ Size \bullet Stress\ \ Duration\ \bullet AF(DriverIC)} hr^{-1}$$

λ = 0.150 10^{-9} hr $^{-1}$ or 0.150 FIT; MTTF = (1/ λ) = 6,649.6 million hrs = 759,089 years

The calculation shows failure rate is 0.150 FIT, MTTF is 6,649.6 million hours under typical operating conditions.

The qualification test results confirm that AOZ5311NQI passes AOS quality and reliability requirements for product manufacturing release.

Revision	Release Date	Comments
1.0	April 1, 2019	Initial Release
1.1	May 1, 2019	Updated FIT to include voltage acceleration factor

ALPHA & OMEGA SEMICONDUCTOR

Recommended Temperature Profile For Soldering AOS Product with Lead Free Solder

For AOS internal reliability precondition profile see Appendix A

TITLE: Soldering Temperature Profile of AOS Product with Lead free solder

1 PURPOSE

This document defines the recommendation of soldering temperature profiles for all the Alpha & Omega Semiconductor (AOS) products. Using temperature and time duration not to exceed these conditions will prevent damage to the parts during the mounting processes, and also help to ensure the quality and reliability of AOS parts.

2 SCOPE

This procedure is applicable to all of AOS product/packages that are required to perform soldering on to PCB (Printed circuit board)

3 REFERENCE DOCUMENTS

JESD22-A113，Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

IPC/JEDEC J-STD-020D，Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

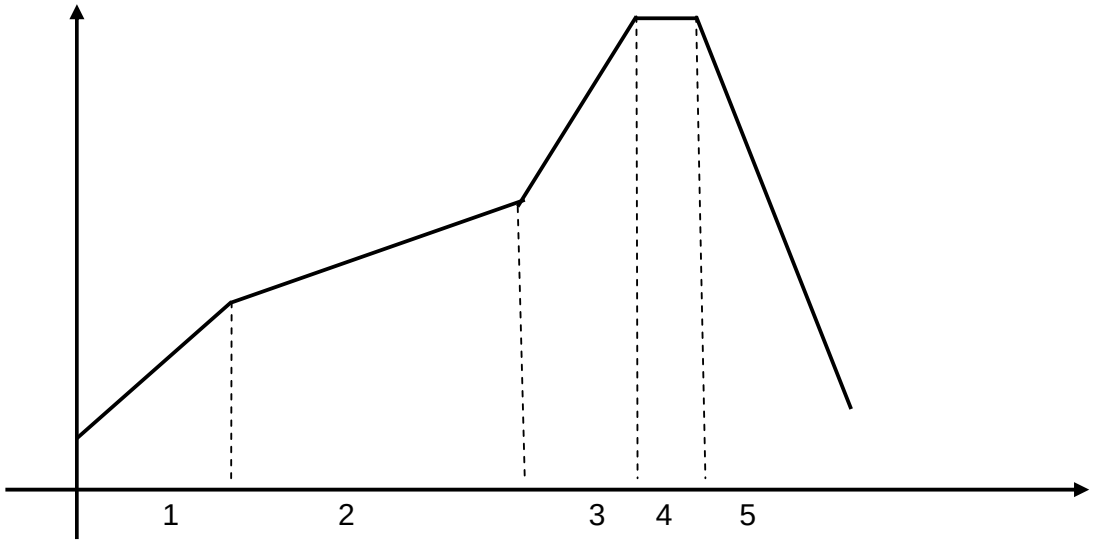
4 GENERAL

Soldering profile is used in PCB assembly. Since different system, different components and different solder are used by different customer, the optimum soldering condition to insure the solder integrity and reliability can only be determined by user (customer). AOS does not assume any responsibilities for the recommendation outlined in this document.

However during the reliability qualification, AOS parts are subject to very severe condition in accordance with the IPC/JEDEC J-STD-20D document (see profile in Appendix A), which involves one week moisture absorption in 85 ºC and 85% relative humidity follow by three solder reflows simulation for 30 sec at peak temperature between 255 ºC and 260 ºC. By using temperature and time duration not to exceed these recommended conditions will be obviously not damage AOS parts.

5 Recommended Soldering Profile

5.1 Reflow Soldering Profile:



Profile Feature	**Requirement**
1. Ramp up	1-4 ºC/second
2. Soak	150 ºC~200 ºC 60-180 seconds
3. Ramp up	1-4ºC/second
4. Peak soak *	245~260 ºC 10 seconds max
5. Ramp-down Rate	1~6 ºC/second max.

* Maximum thermal excursion allowed during the reflow assembly is as follow:

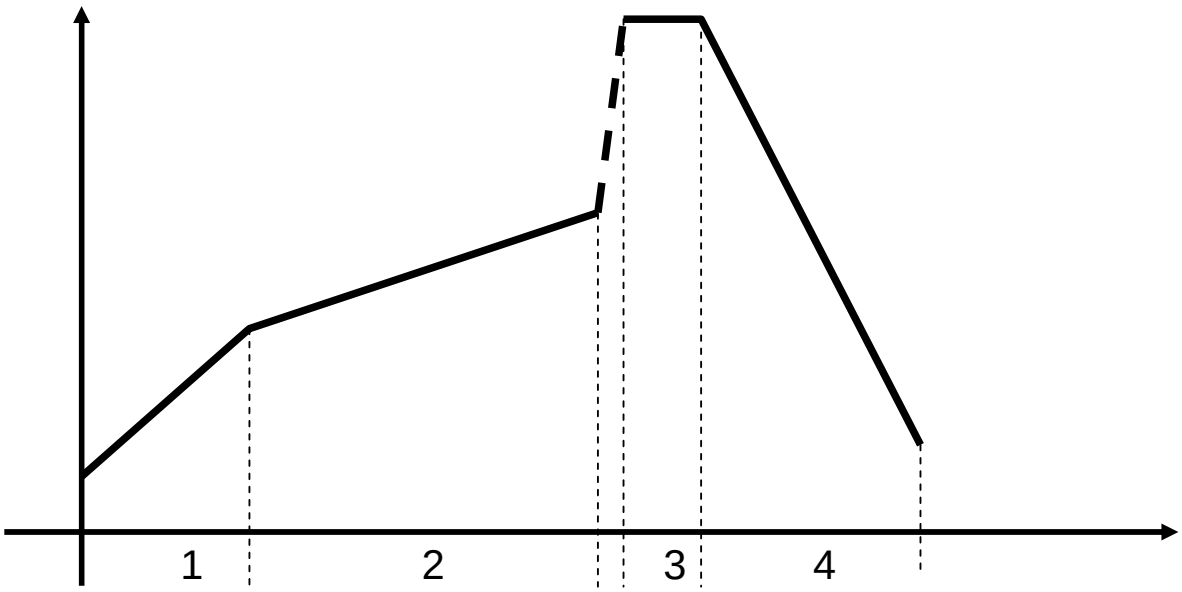
Temperature: 255 ºC ~ 260 ºC

Duration at peak soak: 30 sec

Number of reflow: 3

5.2 Wave Soldering Profile:

Not recommended for leadless package



Profile Feature	**Recommended Condition**
1. Preheat - Ramp up rate	1-7 ºC/second
2. Soak - Temprature: - Time:	80ºC ramp to 140ºC 60-120 seconds
3. Peak - Peak package body temperature - Time	245 ºC to 260 ºC 10 seconds max.
4. Ramp down: - Ramp down rate:	1-7 ºC/second

5.3 Hand Soldering:

Not recommended for mass production. For engineering project or re-work should be used with cautious

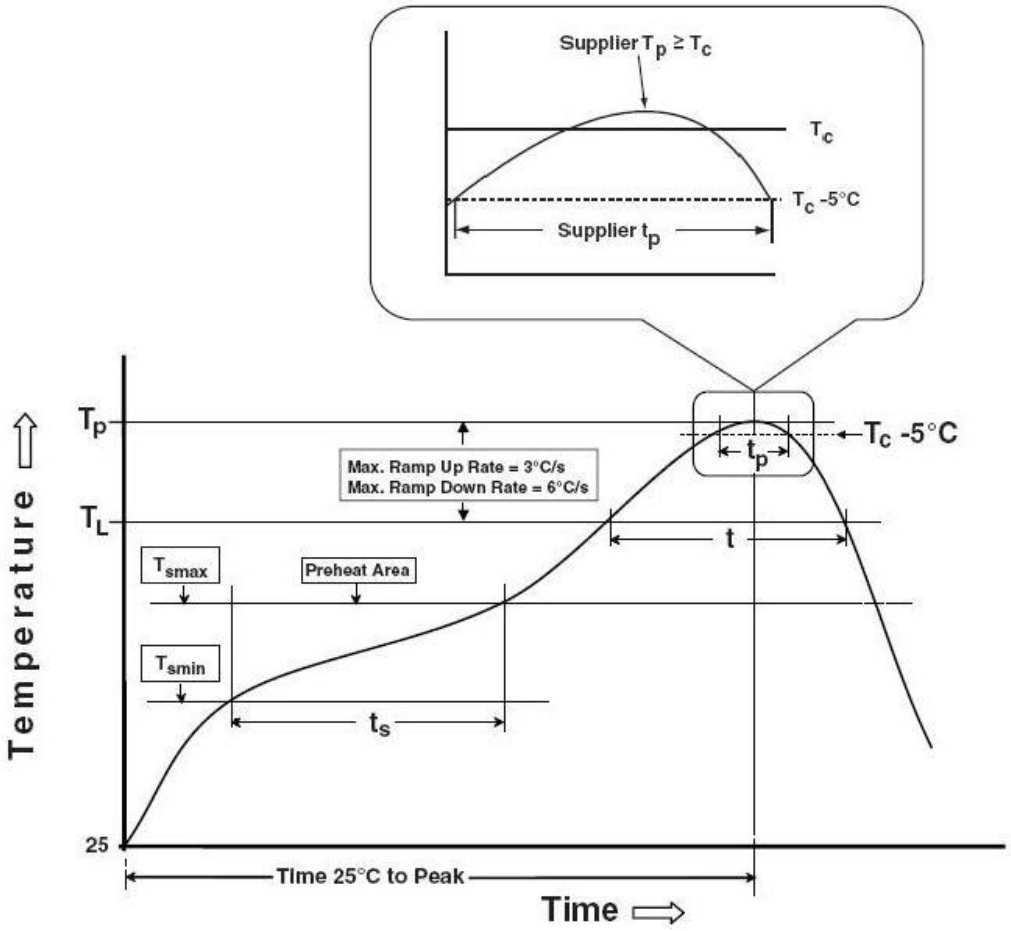
Parameters	**Recommended Condition**
Tip Temperature	350 ±10 ºC
Time*	3 seconds

*Maximum duration is 5 seconds

ALPHA & OMEGA SEMICONDUCTOR

Appendix A

AOS internal reflow profile for reliability test precondition is as follow:



Profile Feature	**Condition**
Preheat & Soak - Temperature Min ($T_{S(min)}$): - Temperature Max ($T_{S(min)}$): - Time (min to max)(ts):	 150 ºC 200 ºC 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 ºC/second max
Liquidous Temperature (T_L): Time (t_L):	217 ºC 60-150 seconds
Peak Package body Temperature(T_p)*: See IPC/JEDEC J-STD-020 for detail	Tp must equal to or exceed the Classification Temperature. Typically Tp = 260 ºC
Time t_p within 5ºC of specified classification temperature (T_C):	30 seconds min.
Ramp-down Rate (T_p to $T_{smax)}$:	6 ºC/second max.
Time 25 ºC to Peak Temp. :	8 minutes max