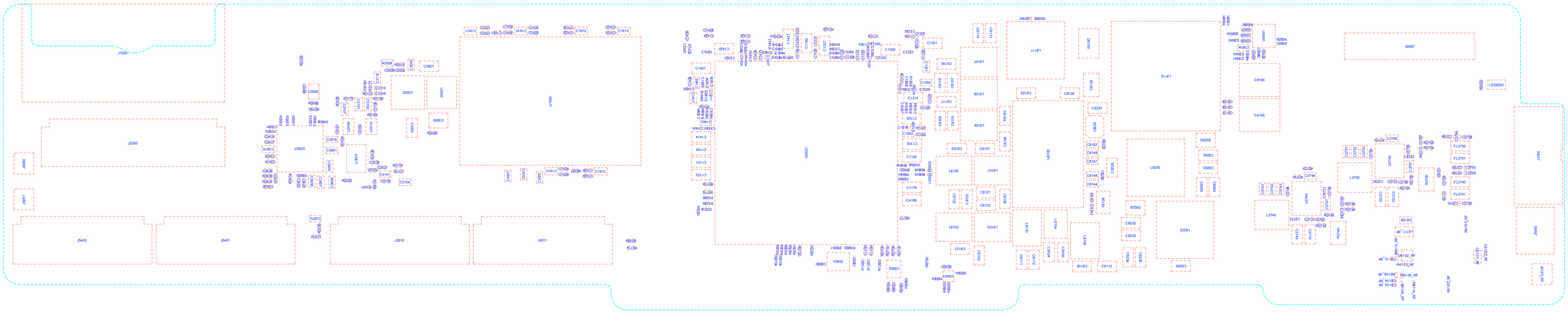
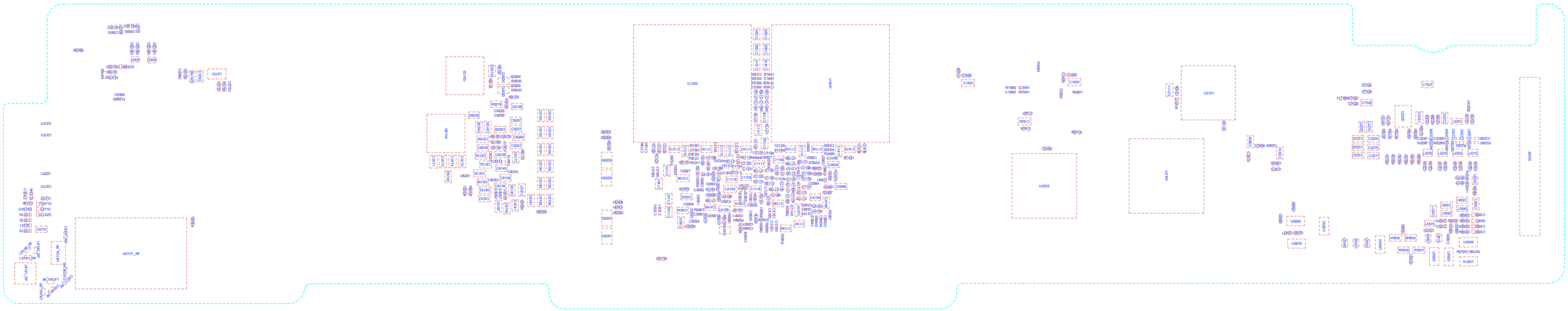
820-3249-06-TOP MLB 位置圖



820-3249-06-BOT MLB 位置圖



1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0001507347	ENGINEERING RELEASED	2012-06-21

X140 MLB - DVT

LAST_MODIFIED=Thu Jun 21 15:28:37 2012

PDF	CSA	CONTENTS	SYNC MASTER	DATE	(SYSTEM DRI)
1	1	Table of Contents	N/A	N/A	(AMANDA)
2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A	(AMANDA)
3	4	BOM TABLES	N/A	N/A	(AMANDA)
4	6	AP: MAIN	N/A	N/A	(TERRY)
5	7	AP: I/Os	N/A	N/A	(AMANDA)
6	8	AP: NAND	N/A	N/A	(TERRY)
7	9	AP: TV,DP,MIPI	N/A	N/A	(TERRY)
8	10	AP: DDR	N/A	N/A	(TERRY)
9	11	AP: POWER	N/A	N/A	(TERRY)
10	12	AP: MISC & ALIASES	N/A	N/A	(TERRY)
11	13	DDR 0 AND 1	N/A	N/A	(TERRY)
12	14	DDR 2 AND 3	N/A	N/A	(TERRY)
13	16	NAND	N/A	N/A	(AMANDA)
14	21	ALIASES	N/A	N/A	(AMANDA)
15	22	VIDEO: EDP CONNECTOR	N/A	N/A	(JOE)
16	30	GRAPE: GROUNDHOG,CONN,BOOST	N/A	N/A	(AMANDA)
17	31	GRAPE: Z1, Z2	N/A	N/A	(AMANDA)
18	36	AUDIO: L81 CODEC	N/A	N/A	(TERRY)
19	37	AUDIO: SPEAKER AMP	N/A	N/A	(TERRY)
20	54	SENSOR FLEX CONN	N/A	N/A	(MARK)
21	55	SENSOR CONN FILTERS 1	N/A	N/A	(MARK)
22	56	SENSOR CONN FILTERS 2	N/A	N/A	(MARK)
23	57	E75 DOCK SUPPORT	N/A	N/A	(JOE)
24	58	IO FLEX CONN	N/A	N/A	(JOE)
25	59	TRISTAR	N/A	N/A	(JOE)
26	60	CONNECTOR: CELLULAR	N/A	N/A	(AMANDA)
27	61	WIFI/BT	N/A	N/A	(MATT)
28	75	POWER: BATTERY CONNECTOR	MADHAVI	12/06/2011	(MADHAVI)
29	81	PMU: ADRIANA PAGE 1	MADHAVI	12/06/2011	(MADHAVI)
30	82	PMU: ADRIANA PAGE 2	MADHAVI	12/06/2011	(MADHAVI)
31	83	PMU: ADRIANA PAGE 3	MADHAVI	12/06/2011	(MADHAVI)
32	90	DEBUG/MISC.	MLB	11/09/2011	(AMANDA)
33	93	TEST/HOLES/FIDUCUALS	N/A	N/A	(AMANDA)
34	121	POWER ALIASES	N/A	N/A	(MADHAVI)
35	150	CONSTRAINTS: MLB RULES	MIKE	11/30/2011	(AMANDA)
36	151	CONSTRAINTS: LOW SPEED BUS	MIKE	11/30/2011	(AMANDA)
37	152	CONSTRAINTS: DISPLAY/AUDIO	MIKE	11/30/2011	(AMANDA)
38	153	CONSTRAINTS: DDR/FMI	MIKE	11/30/2011	(AMANDA)
39	154	CONSTRAINTS: POWER / GND	MIKE	11/30/2011	(AMANDA)

DRAWING
MLB
DRAWING

DRAWING TITLE
SCH,MLB,X140

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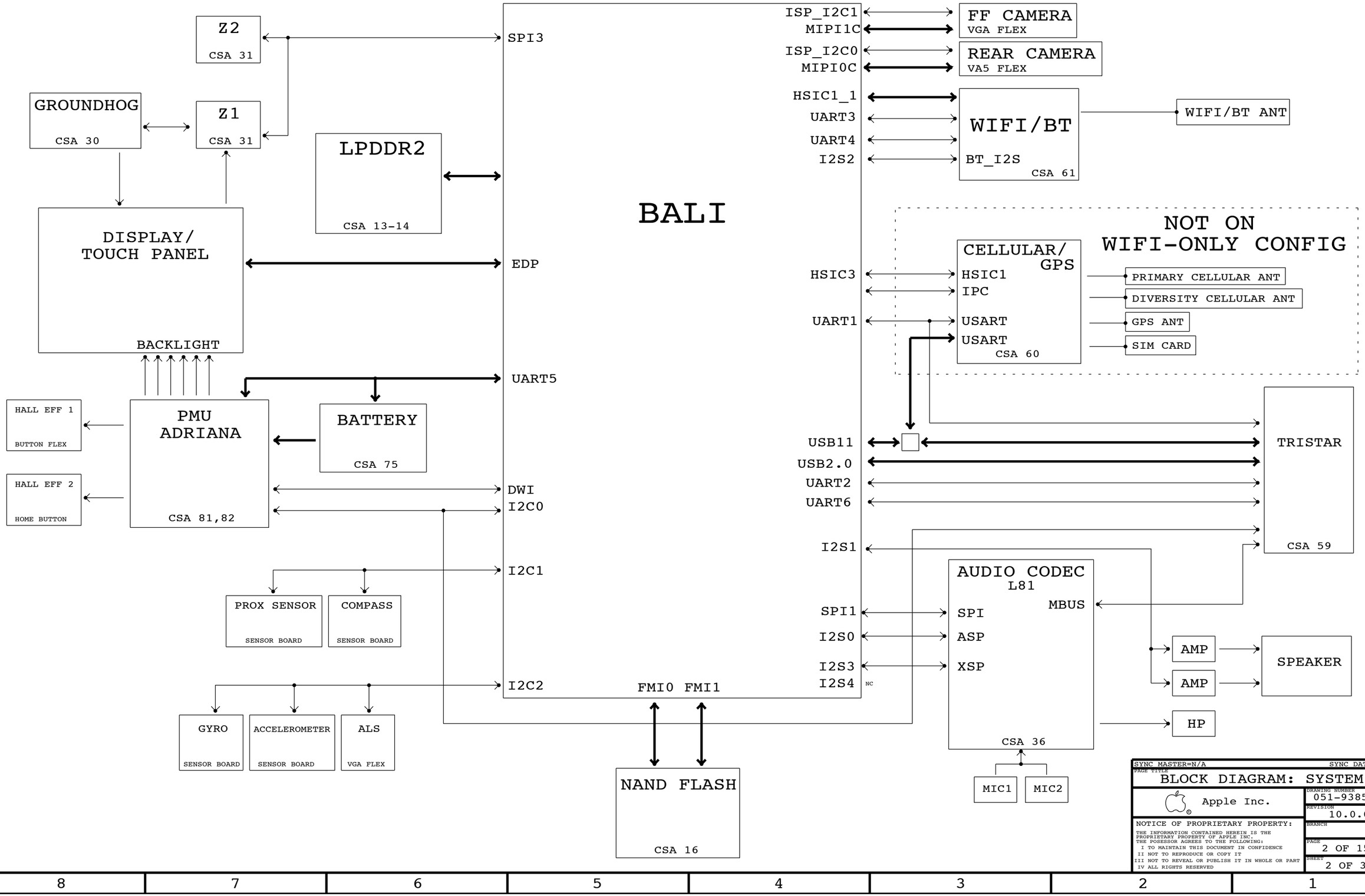

SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE

BLOCK DIAGRAM: SYSTEM

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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD: 16GB CONFIG
32GB_PROD: 32GB CONFIG
64GB_PROD: 64 GB CONFIG
DEV: DEV BOARD ONLY

MLB: MLB BOARD ONLY
MLB_A: WIFI ONLY CONFIG
MLB_B: CELLULAR CONFIG
MLB_C: CELLULAR CONFIG
MLB_D: LEGACY CELLULAR CONFIG
MLB_E: LEGACY CELLULAR CONFIG

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE

MECHANICAL PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
NAND	806-4195	1	FENCE,NAND,TOP,MLB,X140	PD_FENCE_NAND	CRITICAL	
SOC/PMU	806-3493	1	FENCE,LARGE,TOP,MLB,X140	PD_FENCE_LARGE	CRITICAL	
AUDIO	806-3956	1	FENCE,AMP,MLB,X140	PD_FENCE_AMP	CRITICAL	
GRAPE	806-4196	1	FENCE,1,BTM,MLB,X140	PD_FENCE_BTM1	CRITICAL	
MEMORY	806-3492	1	FENCE,2,BTM,MLB,X140	PD_FENCE_BTM2	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7838	1	EEEE FOR 639-3736 (MLB A 16G)	EEEE_F1WD	CRITICAL	EEEE_MLB_A_16G
825-7838	1	EEEE FOR 639-3737 (MLB A 32G)	EEEE_F1WH	CRITICAL	EEEE_MLB_A_32G
825-7838	1	EEEE FOR 639-3738 (MLB A 64G)	EEEE_F1W8	CRITICAL	EEEE_MLB_A_64G
825-7838	1	EEEE FOR 639-3263 (MLB B 16G)	EEEE_DWKG	CRITICAL	EEEE_MLB_B_16G
825-7838	1	EEEE FOR 639-3739 (MLB B 32G)	EEEE_F1W7	CRITICAL	EEEE_MLB_B_32G
825-7838	1	EEEE FOR 639-3740 (MLB B 64G)	EEEE_F1WC	CRITICAL	EEEE_MLB_B_64G
825-7838	1	EEEE FOR 639-3741 (MLB C 16G)	EEEE_F1WG	CRITICAL	EEEE_MLB_C_16G
825-7838	1	EEEE FOR 639-3742 (MLB C 32G)	EEEE_F1WF	CRITICAL	EEEE_MLB_C_32G
825-7838	1	EEEE FOR 639-3743 (MLB C 64G)	EEEE_F1W9	CRITICAL	EEEE_MLB_C_64G

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9385	1	SCH,MLB,X140	SCH1	CRITICAL	
820-3249	1	PCBF,MLB,X140	PCB1	CRITICAL	

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0598	1	IC,SOC,H5G,FCBGA1089,0.5MM	U0600	CRITICAL	

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0622	1	IC,PMU,ADRIANA,D2018A1,FCBGA	U8100	CRITICAL	

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0636	2	LPDDR2,533MHZ,512MB,SAMSUNG,35NM	U1300,U1400	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0637	333S0636		U1300,U1400	LPDDR2,533MHZ,HYNIX,38NM
333S0638	333S0636		U1400,U1400	LPDDR2,533MHZ,ELPIDA,38NM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0878	1	TOSHIBA PPN1.5 16GB	U1600	CRITICAL	16GB_PROD

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0879	1	TOSHIBA PPN1.5 32GB	U1600	CRITICAL	32GB_PROD

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0880	1	TOSHIBA PPN1.5 64GB	U1600	CRITICAL	64GB_PROD

SYNC_MASTER=N/A SYNC_DATE=N/A

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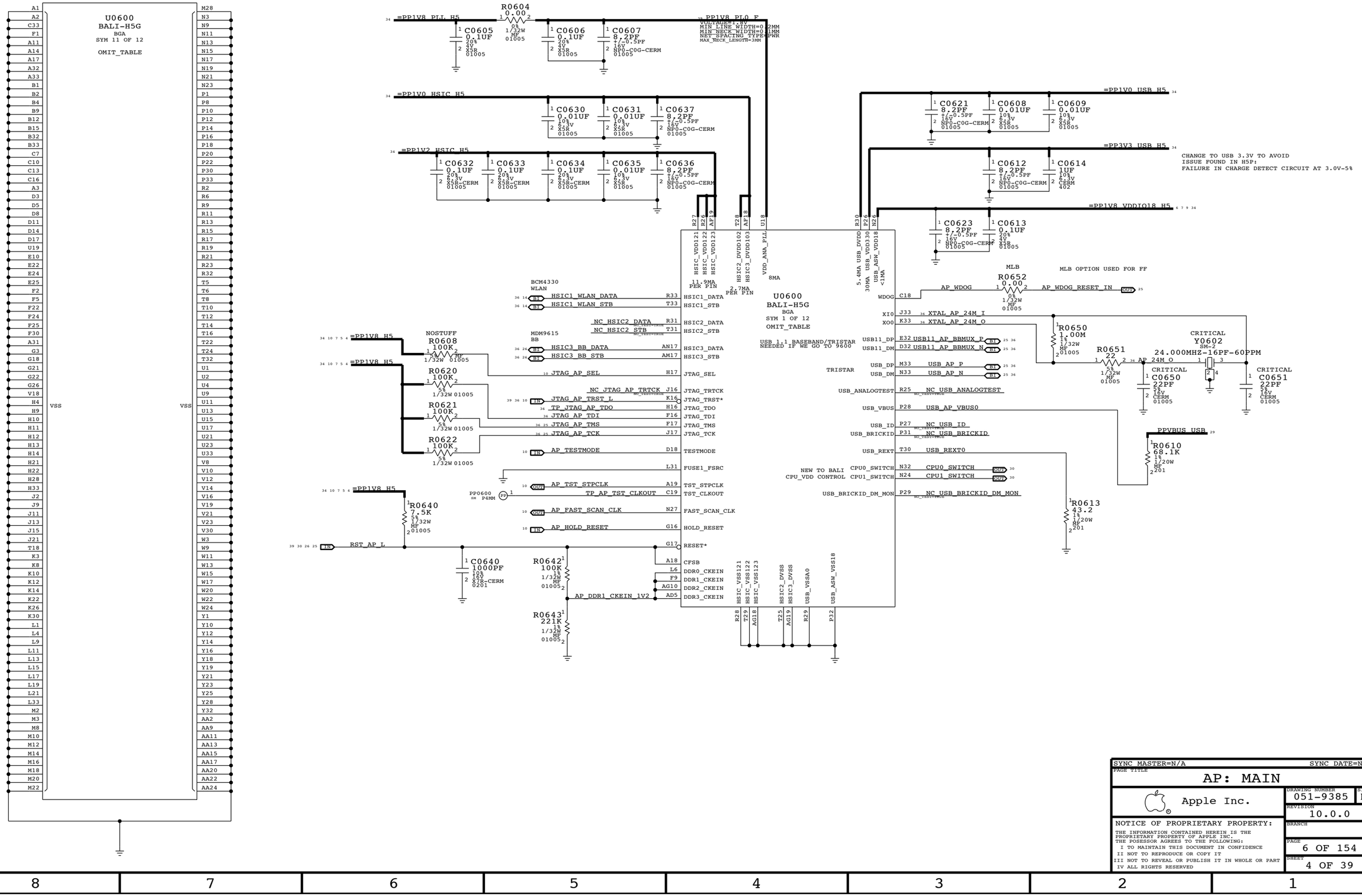
U0600
BALI-H5G
BGA
SYM 11 OF 12
OMIT_TABLE
VSS
U0600
BALI-H5G
BGA
SYM 1 OF 12
OMIT_TABLE
R0604 0.00
C0605 0.1UF
C0606 0.1UF
C0607 8.2PF
=PP1V8_PLL_H5
=PP1V0_HSIC_H5
=PP1V2_HSIC_H5
C0630 0.01UF
C0631 0.01UF
C0637 8.2PF
C0632 0.1UF
C0633 0.1UF
C0634 0.1UF
C0635 0.01UF
C0636 8.2PF
BCM4330
WLAN
HSIC1_WLAN_DATA
HSIC1_WLAN_STB
MDM9615
BB
HSIC3_BB_DATA
HSIC3_BB_STB
JTAG_AP_SEL
NC_JTAG_AP_TRTCK
JTAG_AP_TRST_L
TP_JTAG_AP_TDO
JTAG_AP_TDI
JTAG_AP_TMS
JTAG_AP_TCK
AP_TESTMODE
AP_TST_STPCLK
TP_AP_TST_CLKOUT
AP_FAST_SCAN_CLK
AP_HOLD_RESET
RST_AP_L
NOSTUFF
R0608 100K
R0620 100K
R0621 100K
R0622 100K
R0640 7.5K
C0640 1000PF
R0642 100K
R0643 221K
AP_DDR1_CKEIN_1V2
HSIC1_DATA
HSIC1_STB
HSIC2_DATA
HSIC2_STB
HSIC3_DATA
HSIC3_STB
JTAG_SEL
JTAG_TRTCK
JTAG_TRST*
JTAG_TDO
JTAG_TDI
JTAG_TMS
JTAG_TCK
TESTMODE
FUSE1_FSRC
TST_STPCLK
TST_CLKOUT
FAST_SCAN_CLK
HOLD_RESET
RESET*
CFSB
DDR0_CKEIN
DDR1_CKEIN
DDR2_CKEIN
DDR3_CKEIN
HSIC_VSS121
HSIC_VSS122
HSIC_VSS123
HSIC2_DVSS
HSIC3_DVSS
USB_VSSA0
USB_ASW_VSS18
=PP1V8_PLL_H5
PP1V8_PLL_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.12MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3MM
HSIC_VDD121
HSIC_VDD122
HSIC_VDD123
HSIC2_DVDD102
HSIC3_DVDD103
VDD_ANA_PLL
11.9MA PER PIN
2.7MA PER PIN
8MA
5.4MA USB_DVDD
30MA USB_VDD330
USB_ASW_VDD18
<1MA
=PP1V0_USB_H5
=PP3V3_USB_H5
=PP1V8_VDDIO18_H5
C0621 8.2PF
C0608 0.01UF
C0609 0.01UF
C0612 8.2PF
C0614 1UF
C0623 8.2PF
C0613 0.1UF
CHANGE TO USB 3.3V TO AVOID
ISSUE FOUND IN H5P:
FAILURE IN CHARGE DETECT CIRCUIT AT 3.0V-5%
MLB
MLB OPTION USED FOR FF
R0652 0.00
AP_WDOG
AP_WDOG_RESET_IN
WDOG
XTAL_AP_24M_I
XTAL_AP_24M_O
R0650 1.00M
R0651 22
CRITICAL
Y0602
24.000MHZ-16PF-60PPM
CRITICAL
C0650 22PF
CRITICAL
C0651 22PF
USB11_AP_BBMUX_P
USB11_AP_BBMUX_N
USB_AP_P
USB_AP_N
TRISTAR
USB_ANALOGTEST
NC_USB_ANALOGTEST
USB_VBUS
USB_AP_VBUS0
USB_ID
NC_USB_ID
USB_BRICKID
NC_USB_BRICKID
USB_REXT
USB_REXT0
R0610 68.1K
PPVBUS_USB
NEW TO BALI
CPU_VDD CONTROL
CPU0_SWITCH
CPU1_SWITCH
USB_BRICKID_DM_MON
NC_USB_BRICKID_DM_MON
R0613 43.2
USB 1.1 BASEBAND/TRISTAR
NEEDED IF WE GO TO 9600
SYNC_MASTER=N/A
SYNC_DATE=N/A
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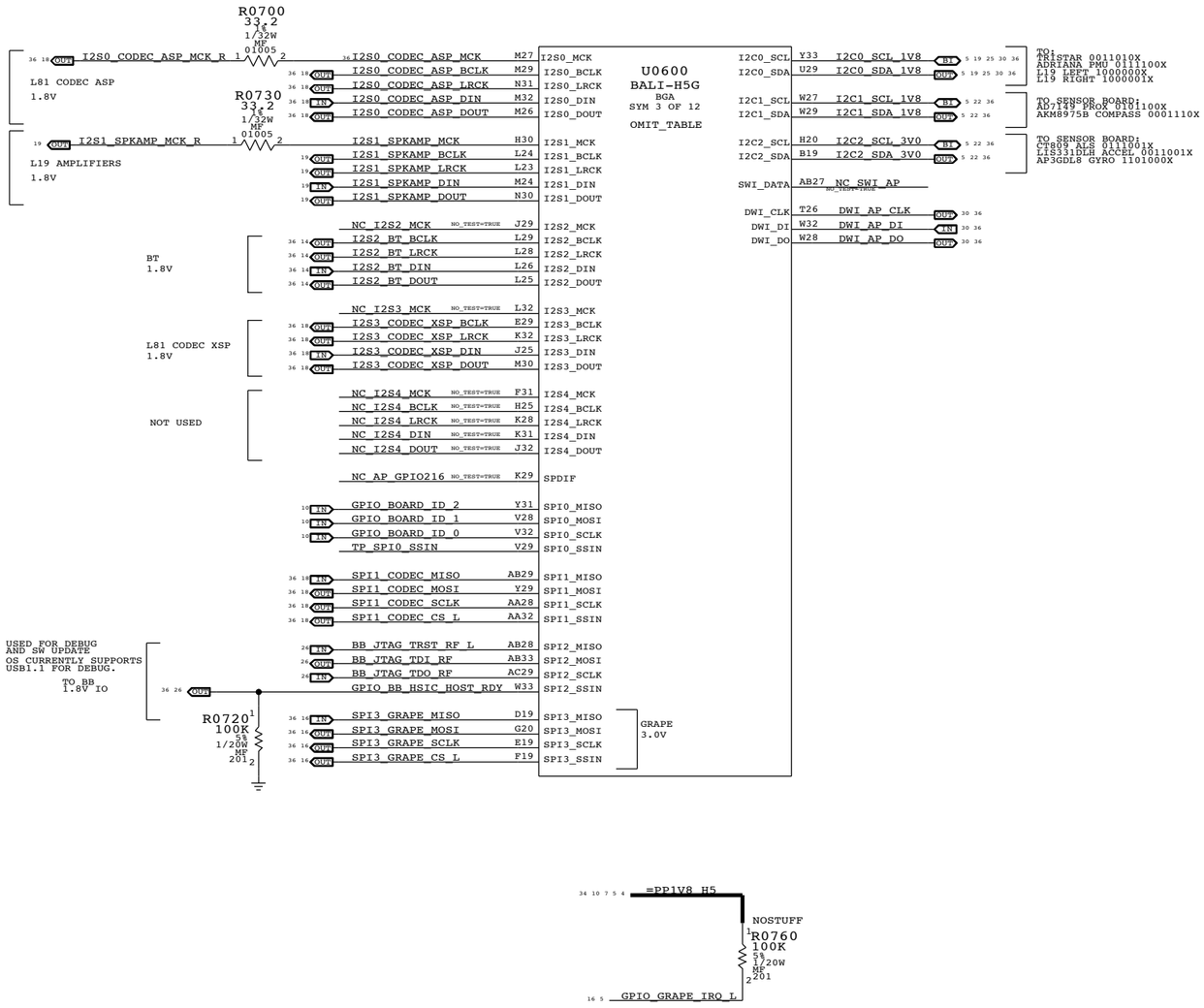

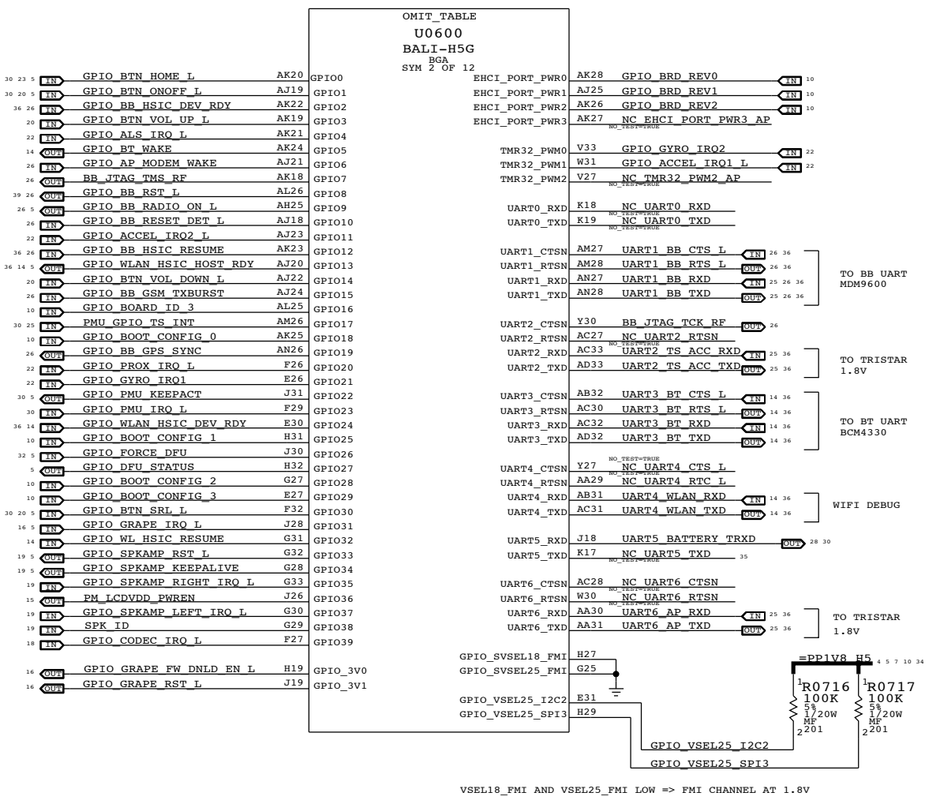

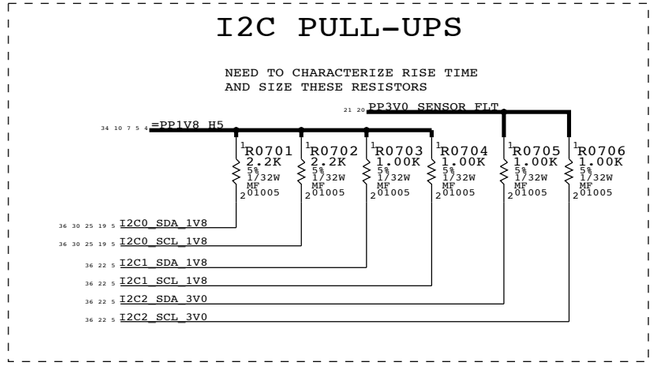

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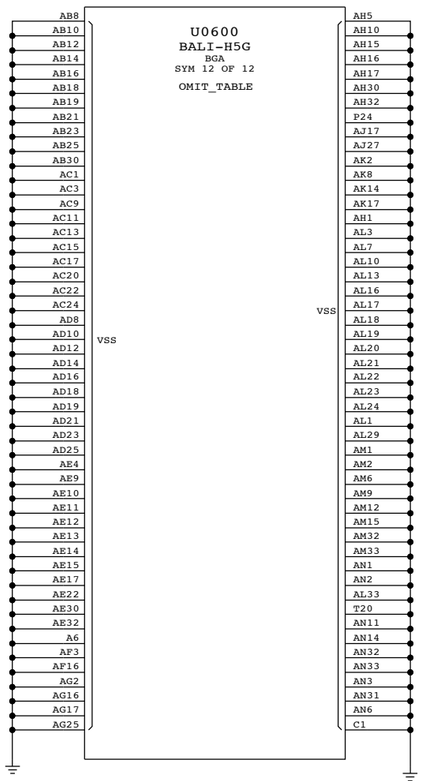

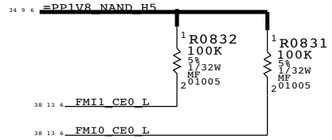

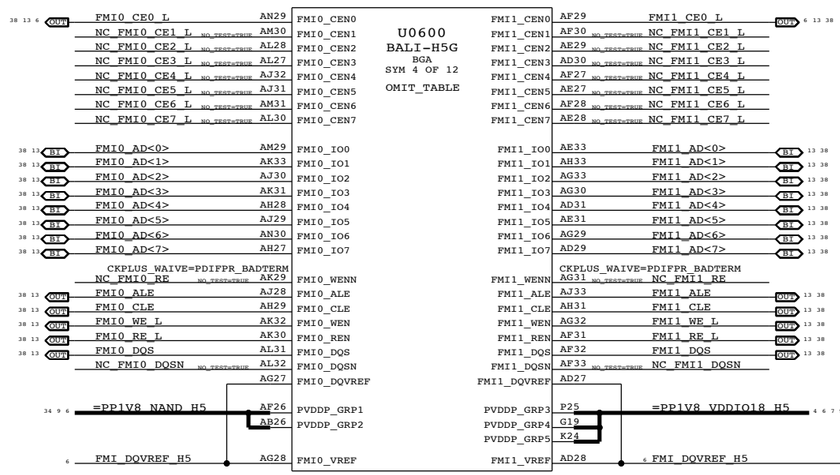

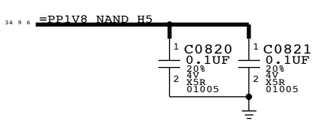

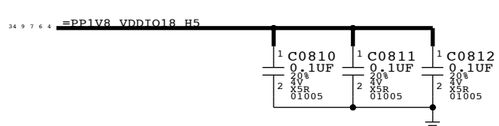

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0725	155S0359	?	FL0910	<RDAR://PROBLEM/11104943>

=PP1V0_DP_PAD_DVDD_H5 — C0910 8.2PF ±0.1PF% 25V CER 0201

=PP1V8_EDP_H5 — R0911 0 5% 1/20W MF 201 — =PP1V8_EDP_AVDD_AUX

C0931 56PF 5% 6.3V NPO-C0G 01005
C0928 8.2PF +/-0.5PF 16V NPO-C0G-CERM 01005
C0929 8.2PF +/-0.5PF 16V NPO-C0G-CERM 01005
C0930 56PF 5% 6.3V NPO-C0G 01005
C0932 0.22UF 20% 6.3V X5R 402
C0933 0.22UF 20% 6.3V X5R 402
C0934 0.22UF 20% 6.3V X5R 402

=PP1V0_EDP_PAD_DVDD_H5 — C0909 0.1UF 10% 6.3V X5R 201

=PP1V8_DP_H5 — C0927 0.1UF 20% 6.3V X5R 01005 — C0924 56PF 5% 6.3V NPO-C0G 01005

=PP1V8_VDDIO18_H5 — C0953 0.01UF 10% 6.3V X5R 01005

=PP1V8_VDDIO18_H5 — C0951 0.1UF 20% 6.3V X5R 01005 — C0952 0.01UF 10% 6.3V X5R 01005

NOSTUFF FL0911 240-OHM-0.2A-0.8-OHM — =PP1V8_VDDIO18_H5 — 0201 — DAC_AP_COMP_FTR

NOSTUFF C0956 0.1UF 10% 6.3V X5R 201

NOSTUFF C0955 0.1UF 10% 6.3V X5R 201

NOSTUFF R0950 6.34K 1% 1/20W MF 201

DAC_AP_VREF — DAC_AP_IREF — DAC_AP_COMP

VOLTAGE=1.8V MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3MM

U0600 BALI-H5G BGA SYM 6 OF 12 OMIT_TABLE

C31	VDD	DP_PAD_DVDD	15MA
B31	VDD	DP_PAD_AVDDX	22MA
D29	VDD	DP_PAD_AVDDP0	10MA
D25	VDD	DP_PAD_AVDD3	65MA PER PIN
D26	VDD	DP_PAD_AVDD2	
C27	VDD	DP_PAD_AVDD1	
C28	VDD	DP_PAD_AVDD0	
D30	VDD	DP_PAD_AVDD_AUX	16MA
C24	VDD	DP_PAD_DVDD	15MA
C23	VDD	DP_PAD_AVDDX	22MA
D21	VDD	DP_PAD_AVDDP0	10MA
A20	VDD	DP_PAD_AVDD3	65MA PER PIN
B20	VDD	DP_PAD_AVDD2	
E20	VDD	DP_PAD_AVDD1	
E21	VDD	DP_PAD_AVDD0	
D22	VDD	DP_PAD_AVDD_AUX	16MA
H23	VDD	DAC_AVDD18D	15MA
H24	VDD	DAC_AVDD18A	15MA

J23	DAC_VREF	DAC_OUT3	D33 NO_TEST=TRUE NC_DAC_AP_OUT3
J24	DAC_IREF	DAC_OUT2	E33 NO_TEST=TRUE NC_DAC_AP_OUT2
K23	DAC_COMP	DAC_OUT1	F33 NO_TEST=TRUE NC_DAC_AP_OUT1
E18	EDP_HPD	DP_HPD	B18 NO_TEST=TRUE NC_DP_HPD
C30	EDP_PAD_AUXP	DP_PAD_AUXP	A26 NO_TEST=TRUE NC_DP_AUX_P
C29	EDP_PAD_AUXN	DP_PAD_AUXN	A25 NO_TEST=TRUE NC_DP_AUX_N
A30	EDP_PAD_TX0P	DP_PAD_TX0P	D24 NO_TEST=TRUE NC_DP_DATA_P<0>
A29	EDP_PAD_TX0N	DP_PAD_TX0N	D23 NO_TEST=TRUE NC_DP_DATA_N<0>
D28	EDP_PAD_TX1P	DP_PAD_TX1P	B24 NO_TEST=TRUE NC_DP_DATA_P<1>
D27	EDP_PAD_TX1N	DP_PAD_TX1N	B23 NO_TEST=TRUE NC_DP_DATA_N<1>
B28	EDP_PAD_TX2P	DP_PAD_TX2P	C22 NO_TEST=TRUE NC_DP_DATA_P<2>
B27	EDP_PAD_TX2N	DP_PAD_TX2N	C21 NO_TEST=TRUE NC_DP_DATA_N<2>
C26	EDP_PAD_TX3P	DP_PAD_TX3P	A22 NO_TEST=TRUE NC_DP_DATA_P<3>
C25	EDP_PAD_TX3N	DP_PAD_TX3N	A21 NO_TEST=TRUE NC_DP_DATA_N<3>
E28	EDP_PAD_R_BIAS	DP_PAD_R_BIAS	E23
F28	EDP_PAD_DC_TP	DP_PAD_DC_TP	F23 TP_DP_AP_ANALOG_TEST

NOTE: 0.6V ANALOG REF

AP_EDP_R_BIAS — NOSTUFF C0957 0.01UF 10% 6.3V X5R 01005 — R0921 4.99K 1% 1/32W MF 01005 — TP_EDP_AP_ANALOG_TEST

DP_R_BIAS — NOTE: 0.6V ANALOG REF — R0920 4.99K 1% 1/32W MF 01005 — NOSTUFF C0950 0.01UF 10% 6.3V X5R 01005

B25	VSS	EDP_PAD_AVSS3	
B26	VSS	EDP_PAD_AVSS2	
A27	VSS	EDP_PAD_AVSS1	
A28	VSS	EDP_PAD_AVSS0	
D31	VSS	EDP_PAD_DVSS	
C32	VSS	EDP_PAD_AVSSX	
B29	VSS	EDP_PAD_AVSSP0	
B30	VSS	EDP_PAD_AVSS_AUX	
A24	VSS	DP_PAD_DVSS	
A23	VSS	DP_PAD_AVSSX	
B21	VSS	DP_PAD_AVSSP0	
C20	VSS	DP_PAD_AVSS3	
F20	VSS	DP_PAD_AVSS1	
D20	VSS	DP_PAD_AVSS2	
F21	VSS	DP_PAD_AVSS0	
B22	VSS	DP_PAD_AVSS_AUX	
G23	VSS	DAC_AVSS18D	
G24	VSS	DAC_AVSS18A	

FL0910 80-OHM-0.2A-0.4-OHM — =PP1V0_MIPI_PLL_H5 — 0201-1 — PP1V0_MIPI_PLL_F

VOLTAGE=1.0V MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3MM

C0980 1UF 10% 6.3V CERM 402
C0981 0.01UF 10% 6.3V X5R 01005
C0982 56PF 5% 6.3V NPO-C0G 01005

=PP1V0_MIPI_H5

C0935 1UF 10% 6.3V CERM 402
C0908 0.1UF 10% 6.3V X5R 201
C0903 0.1UF 10% 6.3V X5R 201
C0904 8.2PF ±0.5PF 16V NP0-C0G-CERM 01005

=PP1V8_MIPI_H5 — C0907 0.1UF 10% 6.3V X5R 201

PP0V4_MIPI1D — C0960 2.2NF 10% 10V X5R-CERM 0201

VOLTAGE=0.4V MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3MM

PP0V4_MIPI1D — C0961 2.2NF 10% 10V X5R-CERM 0201

=PP1V8_H5 — R0930 1.00K 1% 1/32W MF 01005 — R0931 1.00K 1% 1/32W MF 01005 — R0932 1.00K 1% 1/32W MF 01005 — R0933 1.00K 1% 1/32W MF 01005

U0600 BALI-H5G BGA SYM 5 OF 12 OMIT_TABLE

AF20	VDD10	MIPI_VDD10_PLL	40MA
AF21	VDD10	MIPI_VDD10_PLL	
AF22	VDD10	MIPI_VDD10_PLL	
AH19	VDD18	MIPI0D_VDD18	3.2MA
AH24	VDD18	MIPI1D_VDD18	2MA
AF20	VREG_0P4V	MIPI0D_VREG_0P4V	2MA PER PIN
AH23	VREG_0P4V	MIPI1D_VREG_0P4V	

U27	MIPI_VSYNC	NC_MIPI_VSYNC_H5	NO_TEST=TRUE
AM22	MIPI0C_DPDATA0	MIPI0C_CAM_RF_DATA_P<0>	IN
AN22	MIPI0C_DNDATA0	MIPI0C_CAM_RF_DATA_N<0>	IN
AM21	MIPI0C_DPDATA1	MIPI0C_CAM_RF_DATA_P<1>	IN
AN21	MIPI0C_DNDATA1	MIPI0C_CAM_RF_DATA_N<1>	IN
AM19	MIPI0C_DPDATA2	NC_MIPI0C_CAM_RF_DATA_P<2>	NO_TEST=TRUE
AN19	MIPI0C_DNDATA2	NC_MIPI0C_CAM_RF_DATA_N<2>	NO_TEST=TRUE
AM18	MIPI0C_DPDATA3	NC_MIPI0C_CAM_RF_DATA_P<3>	NO_TEST=TRUE
AN18	MIPI0C_DNDATA3	NC_MIPI0C_CAM_RF_DATA_N<3>	NO_TEST=TRUE
AM20	MIPI0C_DPCLK	MIPI0C_CAM_RF_CLK_P	IN
AN20	MIPI0C_DNCLK	MIPI0C_CAM_RF_CLK_N	IN

M25	ISP0_FLASH	ISP0_CAM_RF_RST_L	OUTP
M31	ISP0_PRE_FLASH	NC_ISP0_CAM_RF_FLASH	NO_TEST=TRUE
AA27	ISP0_SCL	ISP0_CAM_RF_I2C_SCL	OUTP
U28	ISP0_SDA	ISP0_CAM_RF_I2C_SDA	BI
N25	ISP1_FLASH	SOCHOT1_L	
L30	ISP1_PRE_FLASH	SOCHOT0_L	
AA33	ISP1_SCL	ISP1_CAM_FF_I2C_SCL	OUTP
U30	ISP1_SDA	ISP1_CAM_FF_I2C_SDA	BI
V31	SENSOR0_CLK	ISP0_CAM_RF_CLK_R	0.00 1% 1/32W MF 01005 — R0900 — ISP0_CAM_RF_CLK
U32	SENSOR0_RST	ISP0_CAM_RF_SHUTDOWN	OUTP
V31	SENSOR1_CLK	ISP1_CAM_FF_CLK_R	0.00 1% 1/32W MF 01005 — R0940 — ISP1_CAM_FF_CLK
T27	SENSOR1_RST	ISP1_CAM_FF_SHUTDOWN_L	OUTP

SHUTDOWN IS ACTIVE HIGH

SHUTDOWN IS ACTIVE LOW

AM23	MIPI1C_DPDATA0	MIPI1C_CAM_FF_DATA_P<0>	IN
AN23	MIPI1C_DNDATA0	MIPI1C_CAM_FF_DATA_N<0>	IN
AM25	MIPI1C_DPDATA1	NC_MIPI1C_CAM_FF_DATA_P<1>	NO_TEST=TRUE
AN25	MIPI1C_DNDATA1	NC_MIPI1C_CAM_FF_DATA_N<1>	NO_TEST=TRUE
AM24	MIPI1C_DPCLK	MIPI1C_CAM_FF_CLK_P	IN
AN24	MIPI1C_DNCLK	MIPI1C_CAM_FF_CLK_N	IN

MIPI_VSS — AG20 AG21 AG22 AG23 AG24

=PP1V8_H5 — NOSTUFF R0942 100K 5% 1/32W MF 01005 — R0941 100K 5% 1/32W MF 01005

SOCHOT1_L PULL-UP ON CSA 90

SOCHOT1_L — SOCHOT0_L

SYNC_MASTER=N/A — SYNC_DATE=N/A

PAGE TITLE: AP: TV,DP,MIPI

Apple Inc.

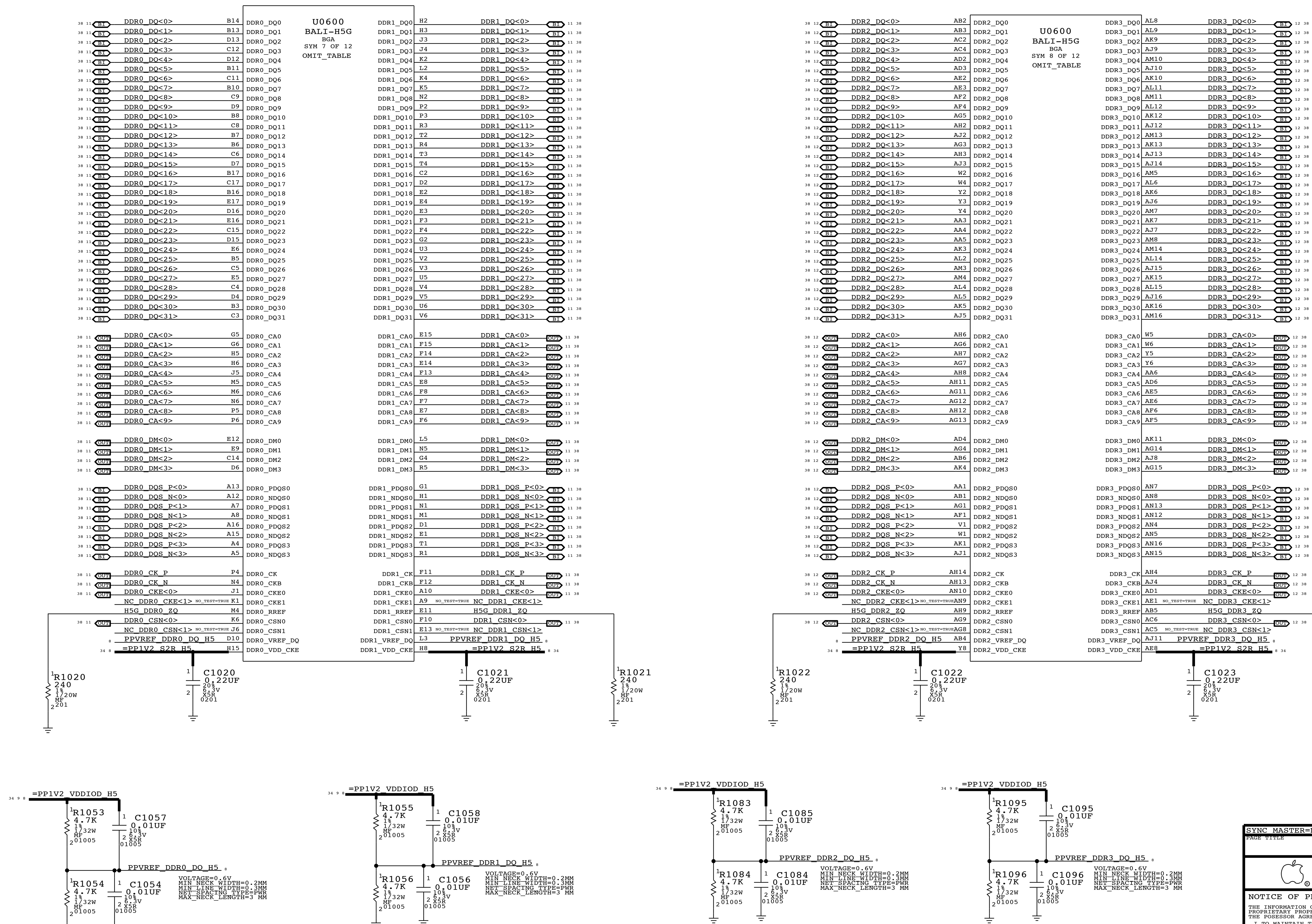
DRAWING NUMBER: 051-9385 — SIZE: D

REVISION: 10.0.0

BRANCH:

PAGE: 9 OF 154

SHEET: 7 OF 39



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PAGE TITLE

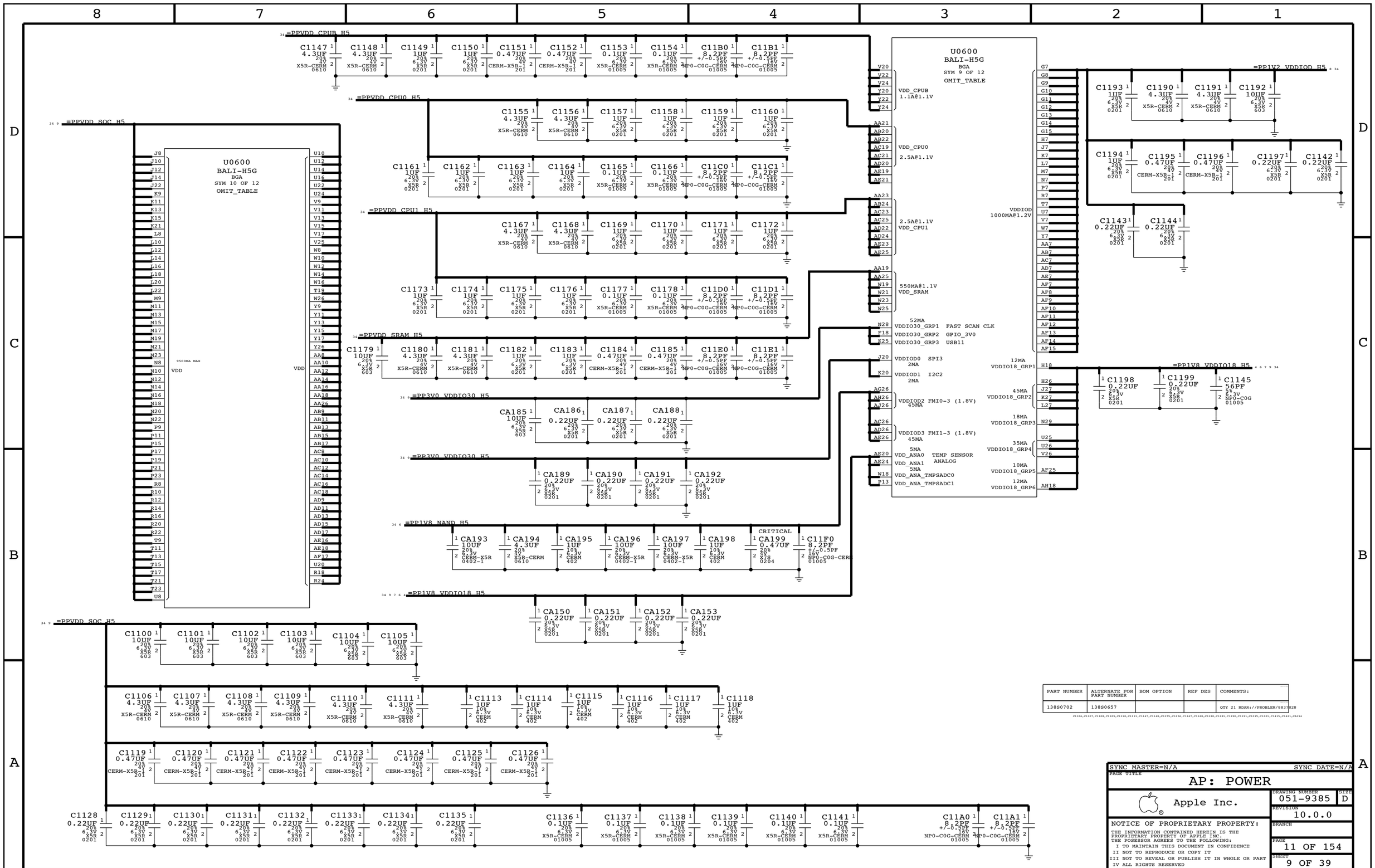
AP: DDR

Apple Inc.

DRAWING NUMBER 051-9385 SIZE D

REVISION 10.0.0

BRANCH



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657			QTY 21 RDAR://PROBLEM/8837828

C1106,C1107,C1108,C1109,C1110,C1111,C1147,C1148,C1155,C1156,C1167,C1168,C1180,C1181,C1190,C1191,C1315,C1321,C1415,C1421,C4194

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

AP: POWER

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DRAWING NUMBER 051-9385 SIZE D

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BRANCH

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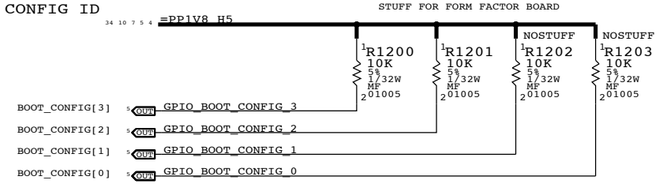
BOOT CONFIG ID



BOOT_CONFIG[3-0]	
1100	FMI0/1 2/2 CS
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS WITH TEST

CURRENT SETTING --->

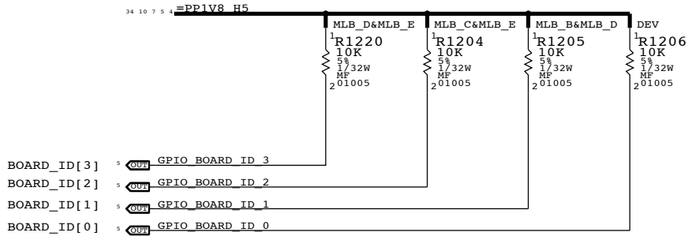
S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

FOR REFERENCE

BOOT_CONFIG[3:0]	
0000	SPI0
0001	SPI1
0010	SPI0 W/TEST
0011	SPI1 W/TEST
0100	FMI0 2CS
0101	FMI0 4CS
0110	FMI0 4CS W/TEST
0111	RESERVED
1000	FMI1 2 CS
1001	FMI1 4 CS
1010	FMI1 4CS W/TEST
1100	FMI0/1 2/2 CS
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS W/TEST
1111	RESERVED

BOARD ID

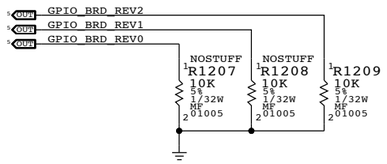


BOARD_ID[3-0]	
0000	X140 AP WLAN (MLB A)
0001	X140 DEV WLAN
0010	X140 AP BB_41 (MLB B)
0011	X140 DEV BB_41
0100	X140 AP BB_42 (MLB C)
0101	X140 DEV BB_42
1010	X140 AP BB_26A (MLB D)
1011	X140 DEV BB_26A
1110	X140 AP BB_26 (MLB E)
1111	X140 DEV BB_26

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION



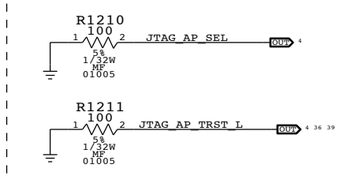
BRD_REV[2-0]	
000	PROTO
001	PROTO 2
010	EVT
011	DVT

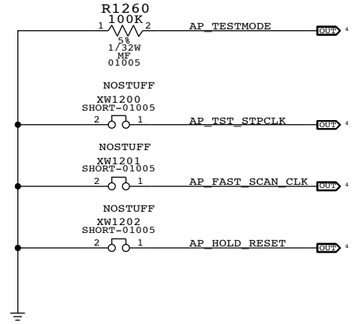
CURRENT SETTING --->

S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

JTAG





SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

AP: MISC & ALIASES

Apple Inc.

DRAWING NUMBER 051-9385 SIZE D

REVISION 10.0.0

BRANCH

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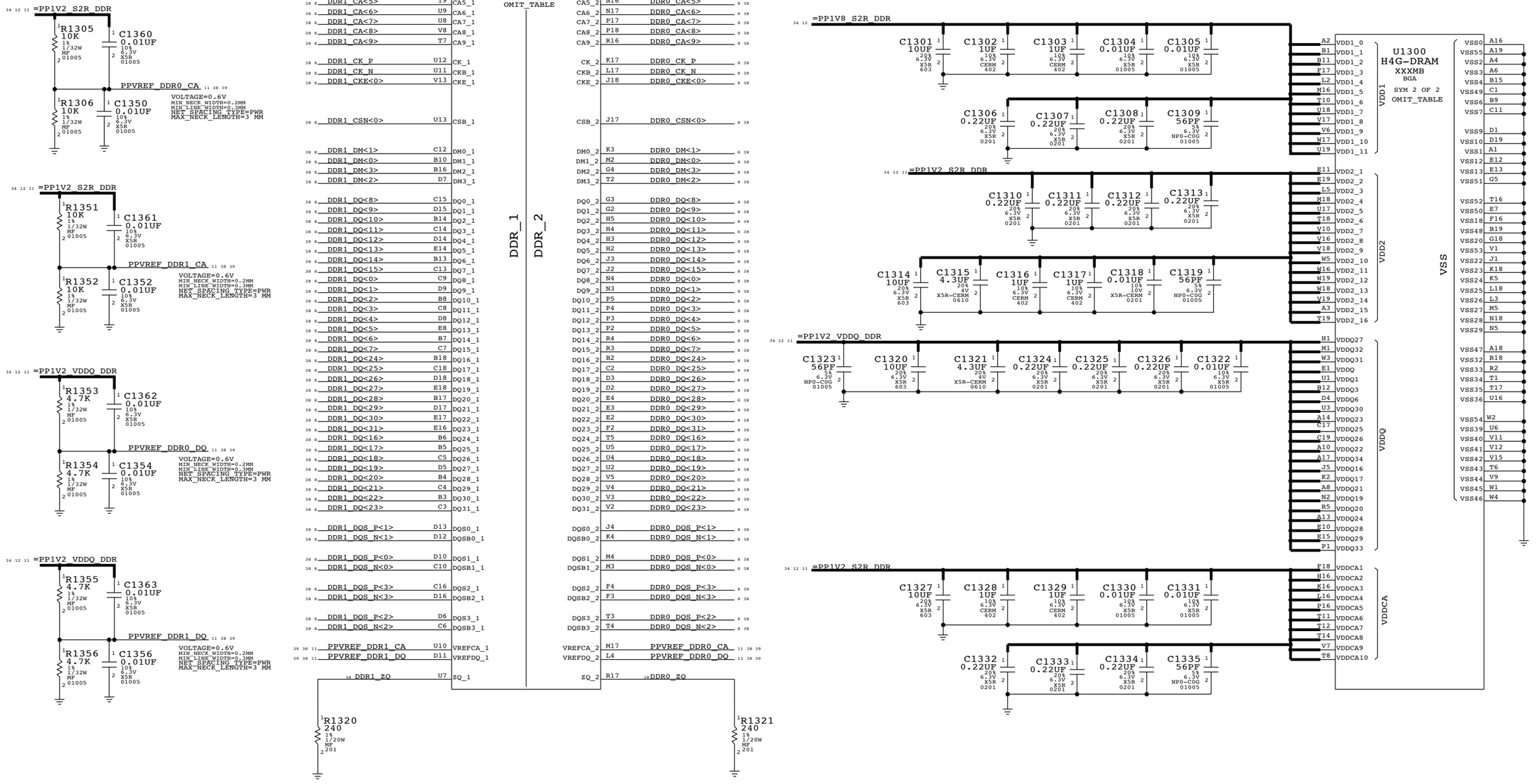

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

DDR 0 AND 1

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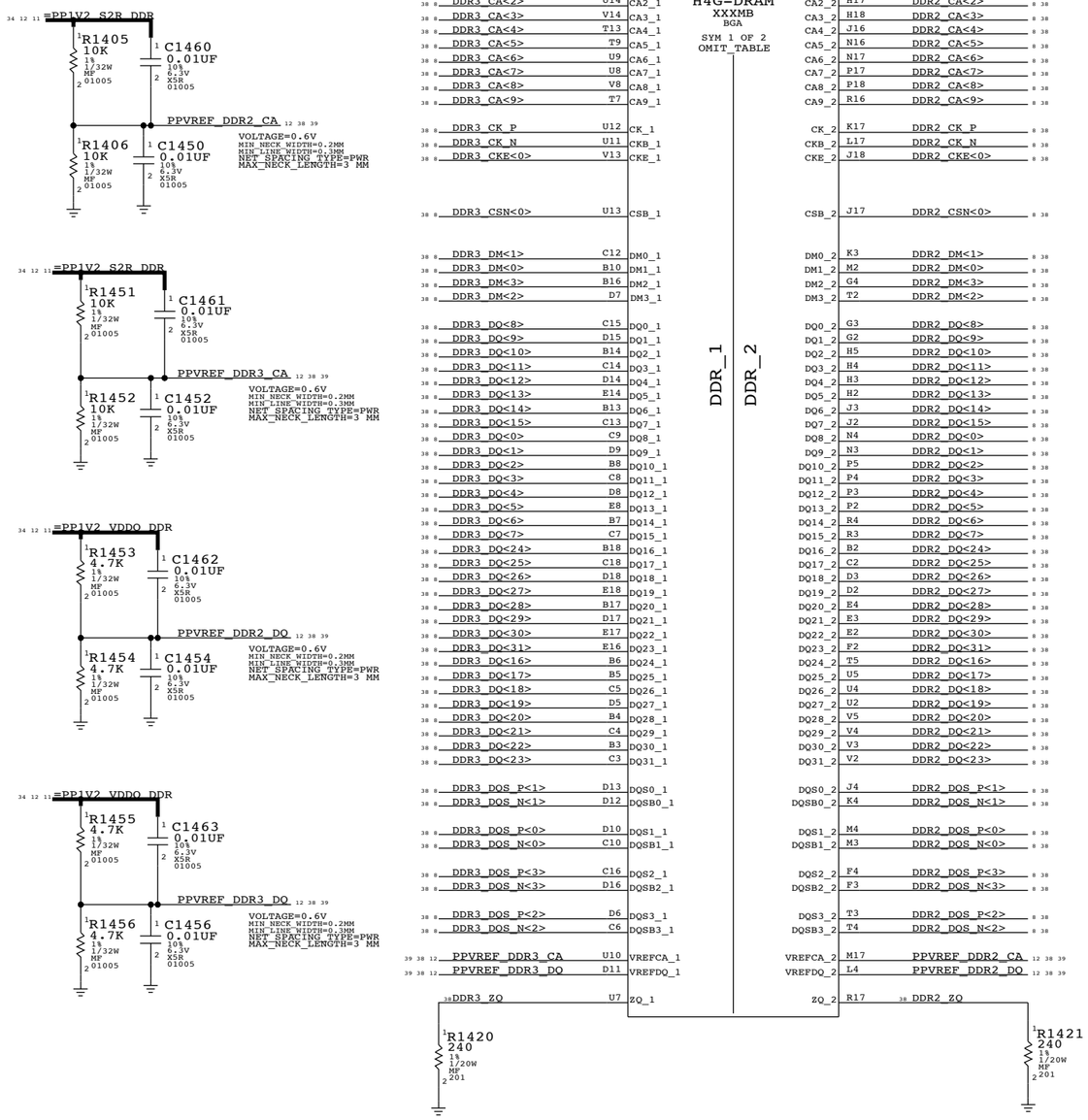

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

DDR 2 AND 3

Apple Inc.

DRAWING NUMBER 051-9385 SIZE D

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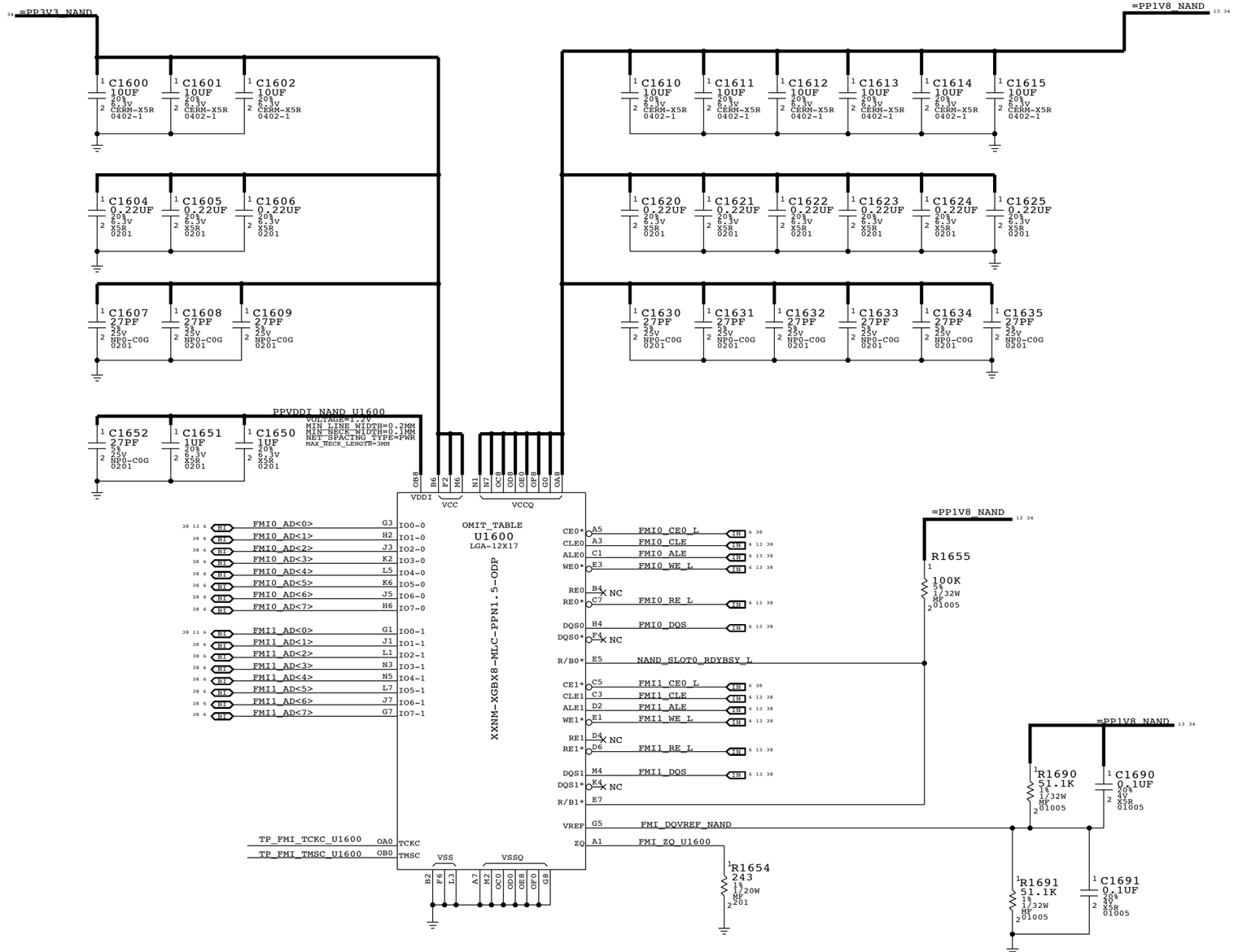

TEST POINTS

DO NOT PLACE IN NAND SINGLE PCS SHIELD CAN AREA

FMI0_AD<0> TP1600
FMI0_ALE TP1601
FMI0_CLE TP1602
FMI0_RE_L TP1603
FMI0_WE_L TP1605
FMI0_DQS TP1613
FMI1_AD<0> TP1606
FMI1_ALE TP1607
FMI1_CLE TP1608
FMI1_RE_L TP1609
FMI1_WE_L TP1611
FMI1_DQS TP1615

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: NAND

Apple Inc.

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WIFI ALIASES

36 4	HSIC1_WLAN_DATA	MAKE_BASE=TRUE	50_HSIC_WLAN_DATA	27
36 4	HSIC1_WLAN_STB	MAKE_BASE=TRUE	50_HSIC_WLAN_STROBE	27
36 5	GPIO_WLAN_HSIC_HOST_RDY	MAKE_BASE=TRUE	AP_HSIC3_RDY	27
36 5	GPIO_WLAN_HSIC_DEV_RDY	MAKE_BASE=TRUE	DEV_HSIC3_RDY	27
30	PMU_GPIO_WLAN_REG_ON	MAKE_BASE=TRUE	WLAN_REG_ON	27
30	PMU_GPIO_WLAN_HOST_WAKE	MAKE_BASE=TRUE	HOST_WAKE_WLAN	27
30	PMU_GPIO_BT_REG_ON	MAKE_BASE=TRUE	BT_REG_ON	27
30	PMU_GPIO_BT_HOST_WAKE	MAKE_BASE=TRUE	HOST_WAKE_BT	27
5	GPIO_BT_WAKE	MAKE_BASE=TRUE	BT_WAKE	27
36 5	UART3_BT_RXD	MAKE_BASE=TRUE	BT_UART_TXD	27
36 5	UART3_BT_TXD	MAKE_BASE=TRUE	BT_UART_RXD	27
36 5	UART3_BT_CTS_L	MAKE_BASE=TRUE	BT_UART_RTS_L	27
36 5	UART3_BT_RTS_L	MAKE_BASE=TRUE	BT_UART_CTS_L	27
36 30	PMU_GPIO_CLK_32K_WLAN	MAKE_BASE=TRUE	CLK32K_AP	27
36 5	I2S2_BT_BCLK	MAKE_BASE=TRUE	BT_PCM_CLK	27
36 5	I2S2_BT_DOUT	MAKE_BASE=TRUE	BT_PCM_IN	27
36 5	I2S2_BT_DIN	MAKE_BASE=TRUE	BT_PCM_OUT	27
36 5	I2S2_BT_LRCK	MAKE_BASE=TRUE	BT_PCM_SYNC	27
36 5	UART4_WLAN_RXD	MAKE_BASE=TRUE	WLAN_UART_TXD	27
36 5	UART4_WLAN_TXD	MAKE_BASE=TRUE	WLAN_UART_RXD	27
5	GPIO_WL_HSIC_RESUME	MAKE_BASE=TRUE	WLAN_HSIC3_RESUME	27
34	VDDIO_WLAN_BT_1V8	MAKE_BASE=TRUE	PP_WL_BT_VDDIO_AP	27

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

ALIASES

Apple Inc.

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REVISION 10.0.0

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EDP CONNECTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0667	155S0583		L2242,L5500,L5510,L5520,L5530,L5540,L5930,L5931	RDAR://PROBLEM/8616060, RADAR://PROBLEM/9015335
155S0625	155S0559		L2202,L2212,L2222,L2232	RDAR://PROBLEM/9017591

=PP3V3_LCD

PPVCC_MAIN

C2240 0.1UF 10% 6.3V X5R 201

C2239 0.1UF 10% 6.3V X5R 201

U2200 SLG5AP302 TDFN CRITICAL

VDD CAP ON GND D S

LCD_RAMP

PM_LCDVDD_PWREN

R2205 100K 5% 1/20W MF 201

C2241 3900PF 10% 50V X7R 0402

LAYOUT NOTE:
PUT THERMAL VIAS AROUND U2200 IN CASE OF SHORTED CONDITION

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM

PP3V3_S0_LCD_FERR

CRITICAL
L2201 FERR-120-OHM-1.5A 0402A

C2203 0.1UF 10% 6.3V X5R 201

C2202 1UF 10% 6.3V CERM 402

R2290 47K 5% 1/20W MF 201 NOSTUFF

C2230 82PF 5% 25V NPO-C0G-CERM 0201

C2232 8.2PF +/-0.1PF 25V CER 0201

C2206 1000PF 10% 16V X7R-CERM 0201

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM

PP3V3_LCDVDD_SW_F

R2280 1.00M 01005 CONN_EDP_DATA_EMI_N<0>

C2280 1.2PF +/-0.1PF 16V NP0-C0G 01005 NOSTUFF

R2281 1.00M 01005 CONN_EDP_DATA_EMI_P<0>

C2281 1.2PF +/-0.1PF 16V NP0-C0G 01005 NOSTUFF

R2282 1.00M 01005 CONN_EDP_DATA_EMI_N<1>

C2282 1.2PF +/-0.1PF 16V NP0-C0G 01005 NOSTUFF

R2283 1.00M 01005 CONN_EDP_DATA_EMI_P<1>

C2283 1.2PF +/-0.1PF 16V NP0-C0G 01005 NOSTUFF

R2284 1.00M 01005 CONN_EDP_DATA_EMI_N<2>

C2284 1.2PF +/-0.1PF 16V NP0-C0G 01005 NOSTUFF

R2285 1.00M 01005 CONN_EDP_DATA_EMI_P<2>

C2285 1.2PF +/-0.1PF 16V NP0-C0G 01005 NOSTUFF

R2286 1.00M 01005 CONN_EDP_DATA_EMI_N<3>

C2286 1.2PF +/-0.1PF 16V NP0-C0G 01005 NOSTUFF

R2287 1.00M 01005 CONN_EDP_DATA_EMI_P<3>

C2287 1.2PF +/-0.1PF 16V NP0-C0G 01005 NOSTUFF

PP3V3_S0_LCD_FERR

R2240 100K 1% 1/32W MF 01005

R2241 100K 1% 1/32W MF 01005

EDP_AUX_N — C2250 0.1UF 201 6.3V 10% X5R — EDP_AUX_EMI_N — CRITICAL TCM0605-1 — CONN_EDP_AUX_EMI_N

EDP_AUX_P — C2251 0.1UF 201 6.3V 10% X5R — EDP_AUX_EMI_P — CRITICAL 90-OHM-50MA L2242 — CONN_EDP_AUX_EMI_P

EDP_DATA_N<0> — C2242 0.1UF 201 6.3V 10% X5R — EDP_DATA_EMI_N<0> — CRITICAL — CONN_EDP_DATA_EMI_N<0>

EDP_DATA_P<0> — C2243 0.1UF 201 6.3V 10% X5R — EDP_DATA_EMI_P<0> — CRITICAL TCM0806-4SM 12-OHM-100MA-8.5GHZ L2212 — CONN_EDP_DATA_EMI_P<0>

EDP_DATA_N<1> — C2244 0.1UF 201 6.3V 10% X5R — EDP_DATA_EMI_N<1> — CRITICAL — CONN_EDP_DATA_EMI_N<1>

EDP_DATA_P<1> — C2245 0.1UF 201 6.3V 10% X5R — EDP_DATA_EMI_P<1> — CRITICAL TCM0806-4SM 12-OHM-100MA-8.5GHZ L2222 — CONN_EDP_DATA_EMI_P<1>

EDP_DATA_N<2> — C2246 0.1UF 201 6.3V 10% X5R — EDP_DATA_EMI_N<2> — CRITICAL — CONN_EDP_DATA_EMI_N<2>

EDP_DATA_P<2> — C2247 0.1UF 201 6.3V 10% X5R — EDP_DATA_EMI_P<2> — CRITICAL TCM0806-4SM 12-OHM-100MA-8.5GHZ L2232 — CONN_EDP_DATA_EMI_P<2>

EDP_DATA_N<3> — C2248 0.1UF 201 6.3V 10% X5R — EDP_DATA_EMI_N<3> — CRITICAL — CONN_EDP_DATA_EMI_N<3>

EDP_DATA_P<3> — C2249 0.1UF 201 6.3V 10% X5R — EDP_DATA_EMI_P<3> — CRITICAL TCM0806-4SM 12-OHM-100MA-8.5GHZ L2202 — CONN_EDP_DATA_EMI_P<3>

518S0827
CRITICAL
J2200
502250-8051-B
F-RT-SM

EDP_HPD

R2242 100K 1% 1/32W MF 01005

CONN_EDP_AUX_EMI_P

NC

CONN_EDP_AUX_EMI_N
CONN_EDP_DATA_EMI_N<0>
CONN_EDP_DATA_EMI_P<0>
CONN_EDP_DATA_EMI_N<1>
CONN_EDP_DATA_EMI_P<1>
CONN_EDP_DATA_EMI_N<2>
CONN_EDP_DATA_EMI_P<2>
CONN_EDP_DATA_EMI_N<3>
CONN_EDP_DATA_EMI_P<3>

J2200_29_GND
LED_IO_5_B
LED_IO_3_B
LED_IO_1_B
LED_IO_6_A
LED_IO_4_A
LED_IO_2_A
J2200_43_GND

LED_IO_6_B
LED_IO_4_B
LED_IO_2_B
J2200_36_GND
LED_IO_5_A
LED_IO_3_A
LED_IO_1_A

R2295 0 5% 1/20W MF 201 — J2200_29_GND

R2296 0 5% 1/20W MF 201 — J2200_36_GND

R2297 0 5% 1/20W MF 201 — J2200_43_GND

CRITICAL
L2210 FERR-240-OHM-25%-300MA 0402

=PPLED_REG_B
VOLTAGE=20.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

PPLED_BACK_REG_B

C2253 100PF 5% 50V CERM 0402

C2270 820PF 10% 50V CERM 0402

C2271 8.2PF +/-0.25PF 50V CERM 402-1

CRITICAL
L2200 FERR-240-OHM-25%-300MA 0402

=PPLED_REG_A
VOLTAGE=20.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

PPLED_BACK_REG_A

C2233 100PF 5% 50V CERM 0402

C2220 820PF 10% 50V CERM 0402

C2221 8.2PF +/-0.25PF 50V CERM 402-1

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
VIDEO: EDP CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9385 SIZE D
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BRANCH
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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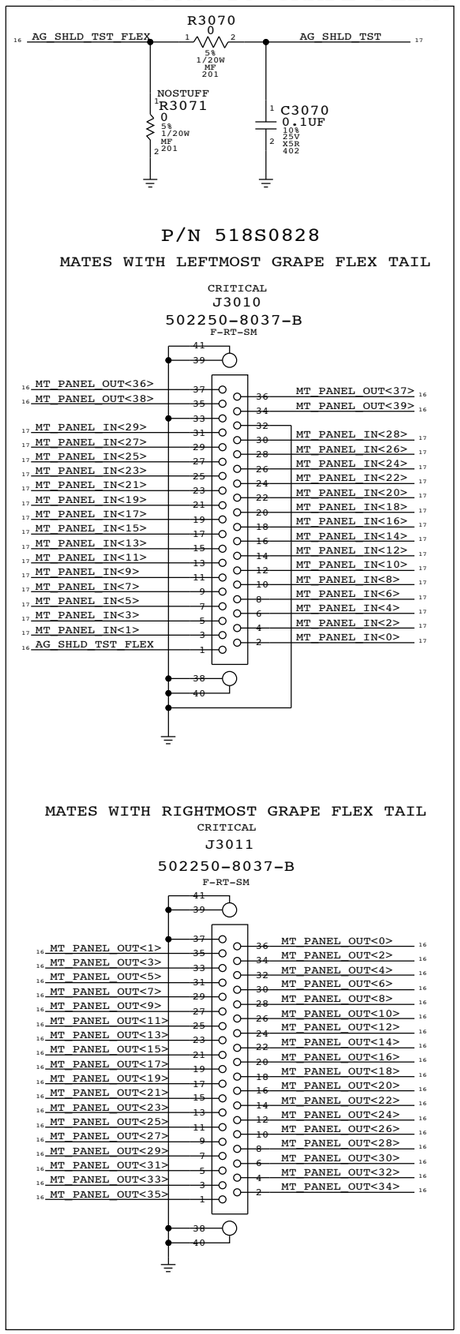
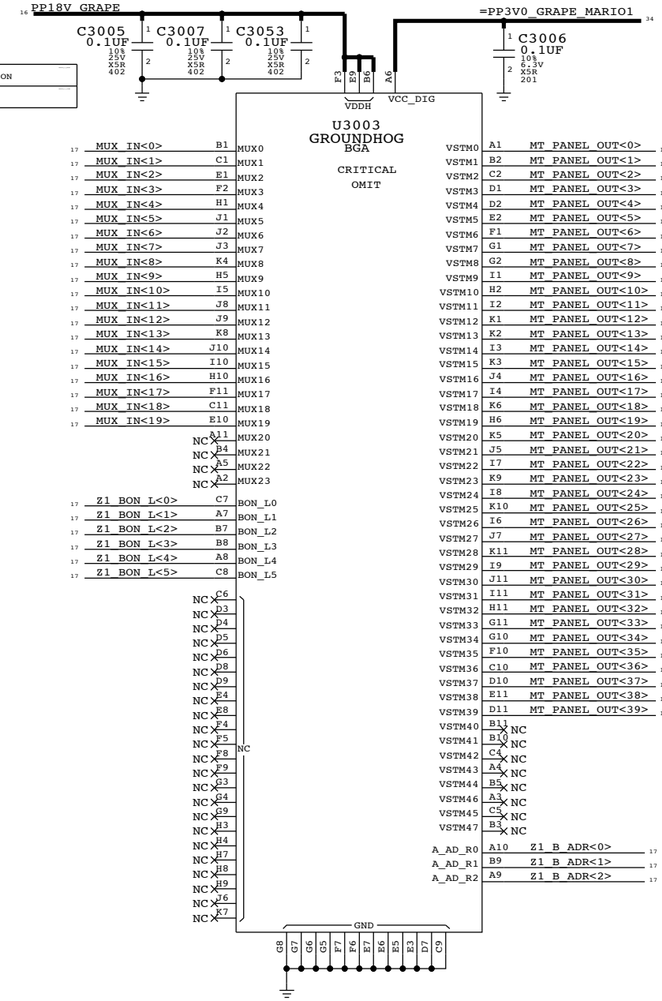
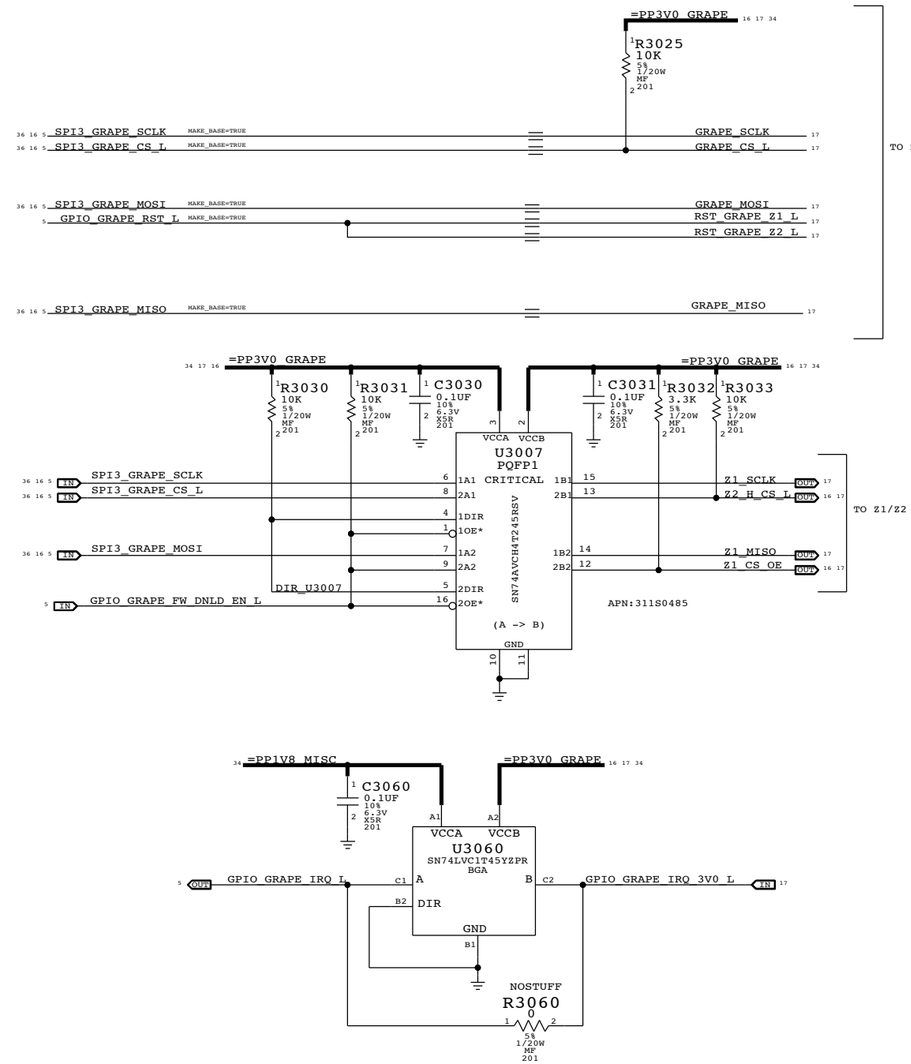
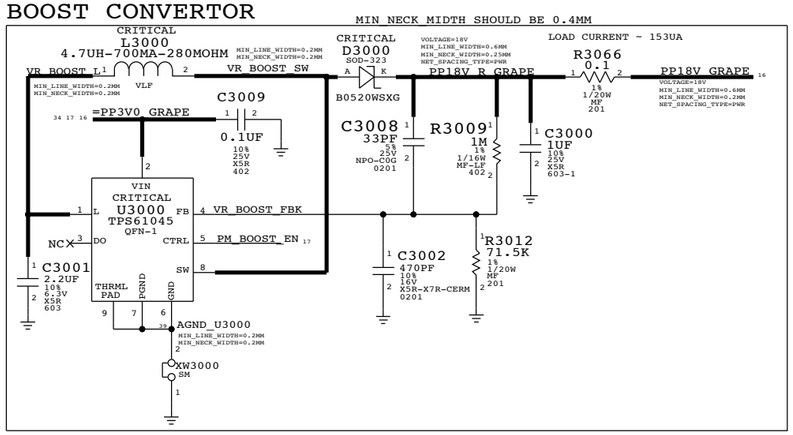
CONNECTORS TO GREPE FLEX

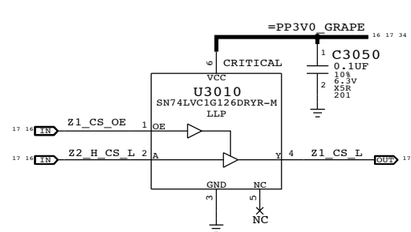


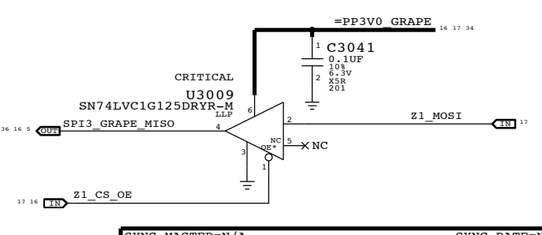




BOOST CONVERTOR







PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

GRAPE: GROUNDHOG,CONN,BOOST

Apple Inc.

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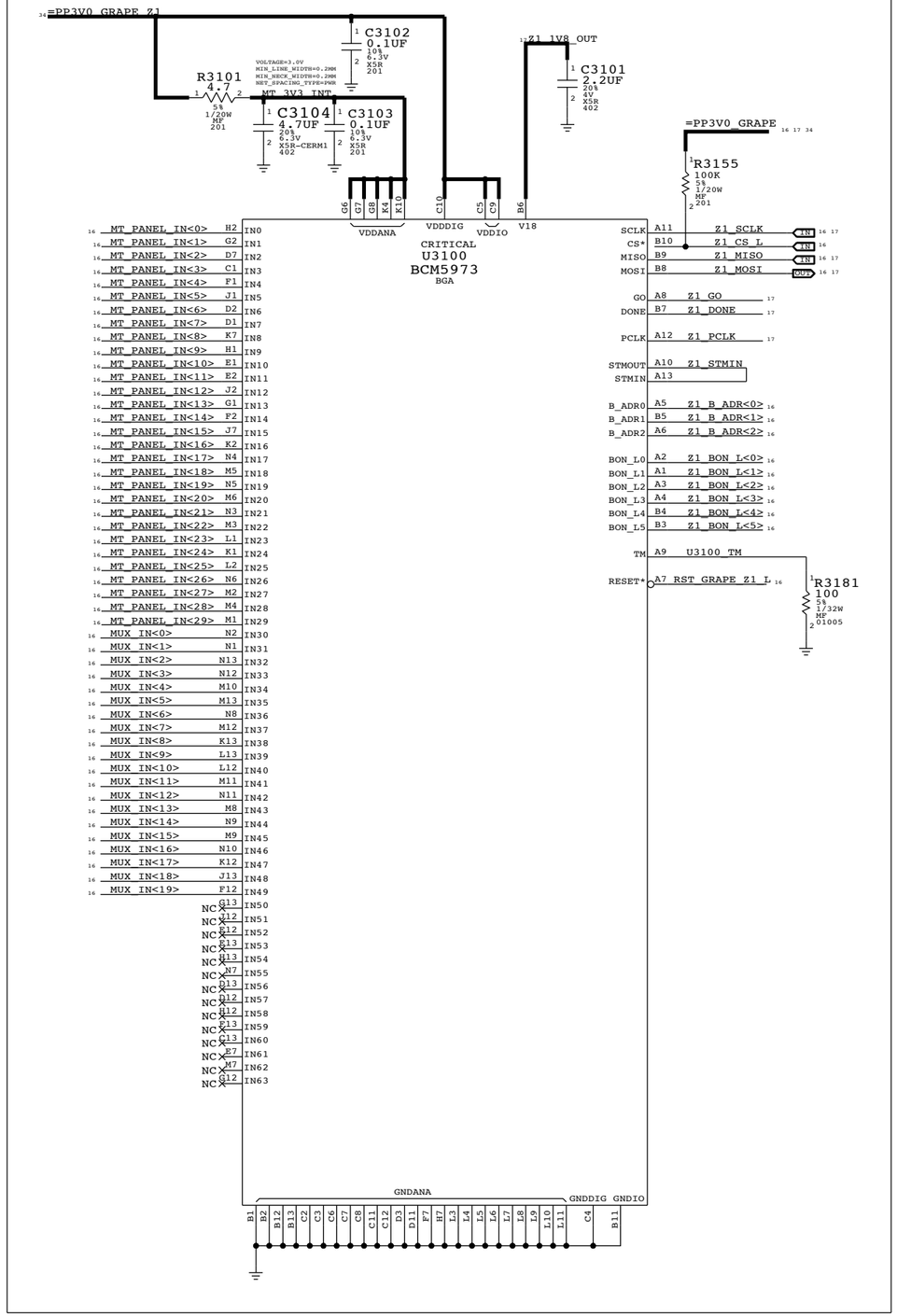
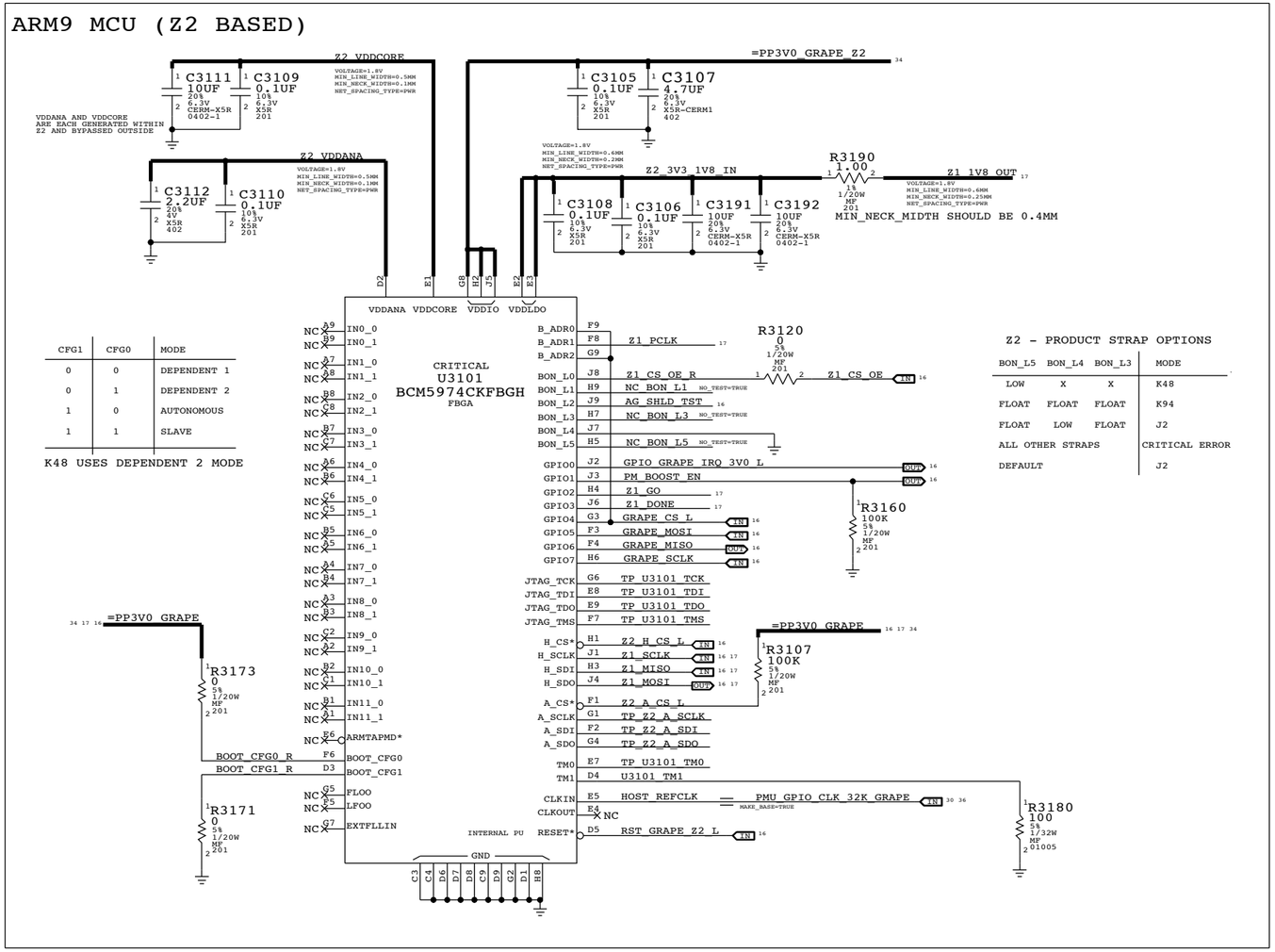
ZEPHYR 1+ ASIC



ARM9 MCU (Z2 BASED)



CFG1	CFG0	MODE
0	0	DEPENDENT 1
0	1	DEPENDENT 2
1	0	AUTONOMOUS
1	1	SLAVE

K48 USES DEPENDENT 2 MODE

Z2 - PRODUCT STRAP OPTIONS

BON_L5	BON_L4	BON_L3	MODE
LOW	X	X	K48
FLOAT	FLOAT	FLOAT	K94
FLOAT	LOW	FLOAT	J2
ALL OTHER STRAPS			CRITICAL ERROR
DEFAULT			J2

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: GRAPE: Z1, Z2

Apple Inc.

DRAWING NUMBER: 051-9385 SIZE: D

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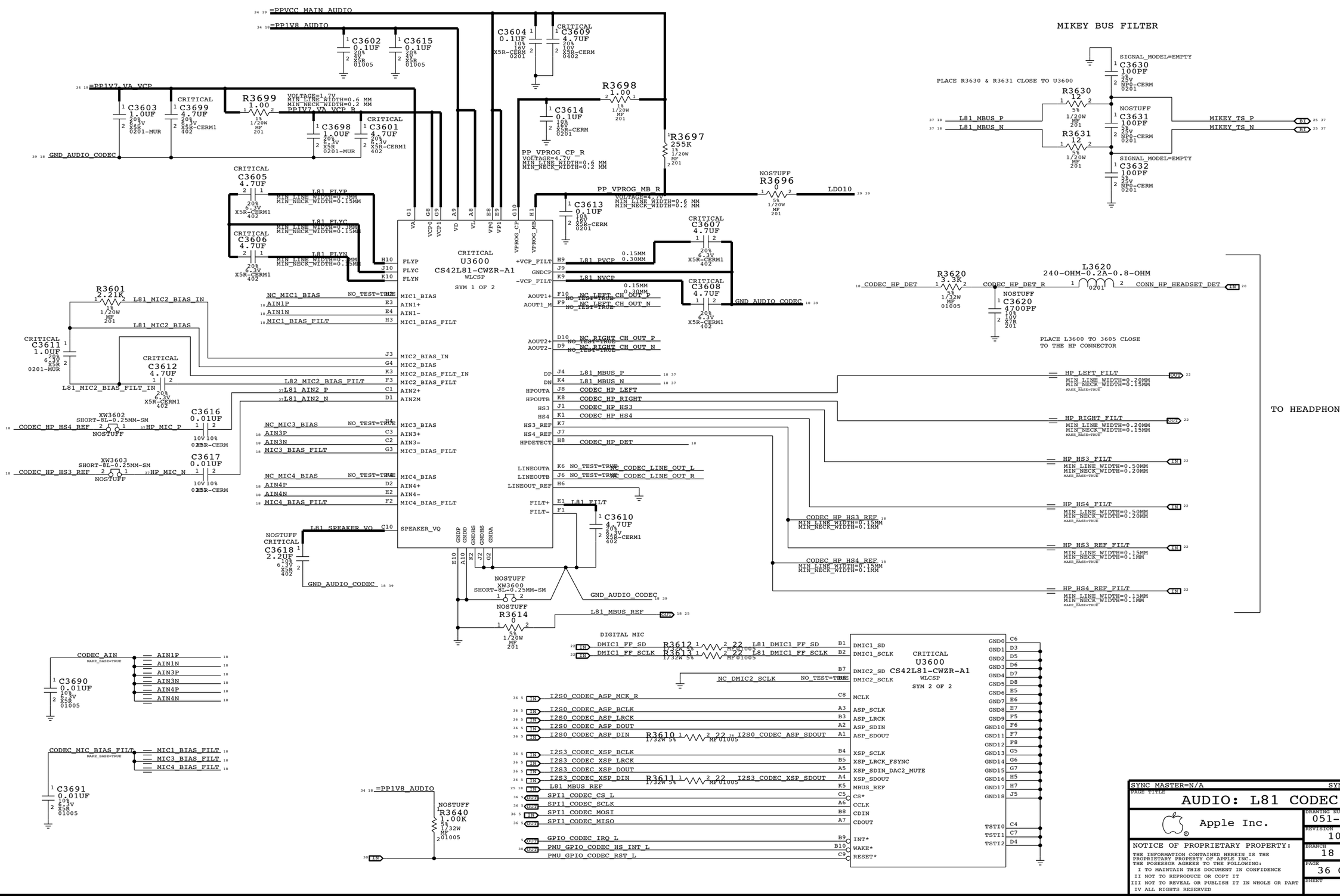

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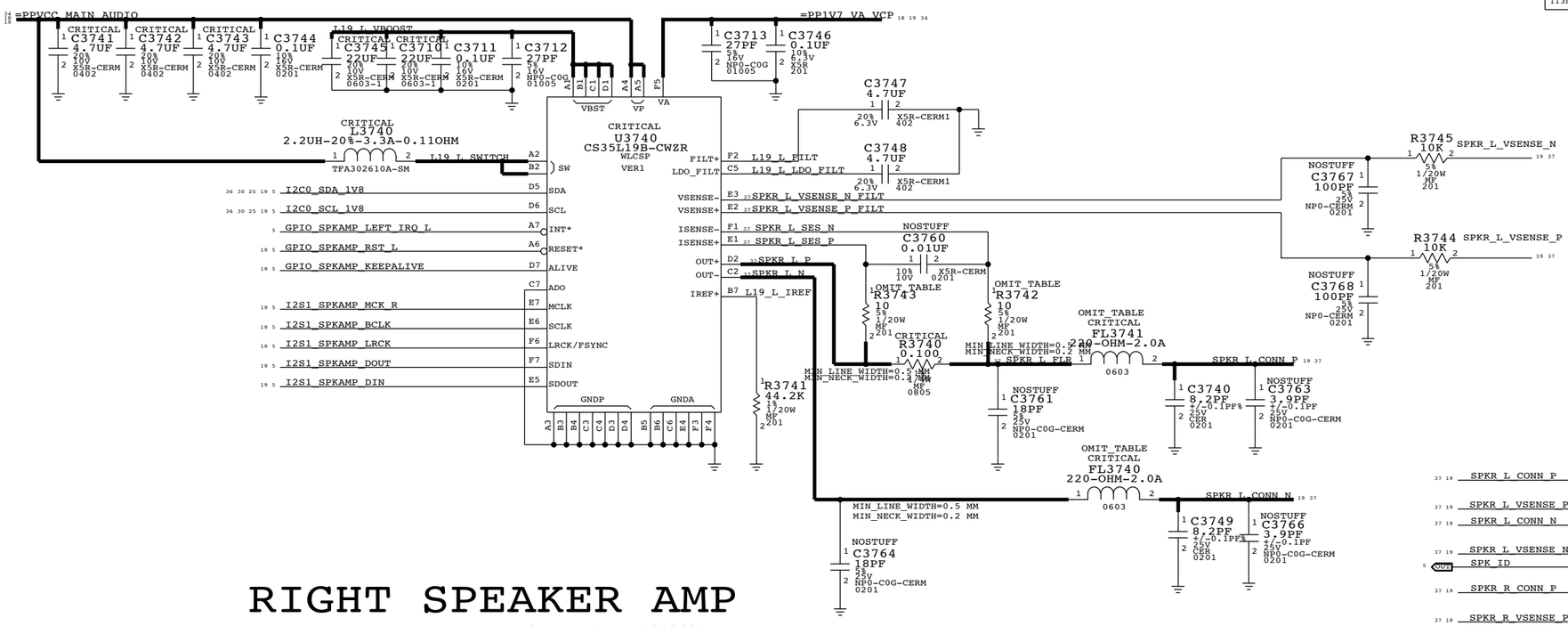
Apple Inc.	DRAWING NUMBER 051-9385 · SIZE D · REVISION 10.0.0 · BRANCH 18 OF 39 · PAGE 36 OF 154 · SHEET

LEFT SPEAKER AMP

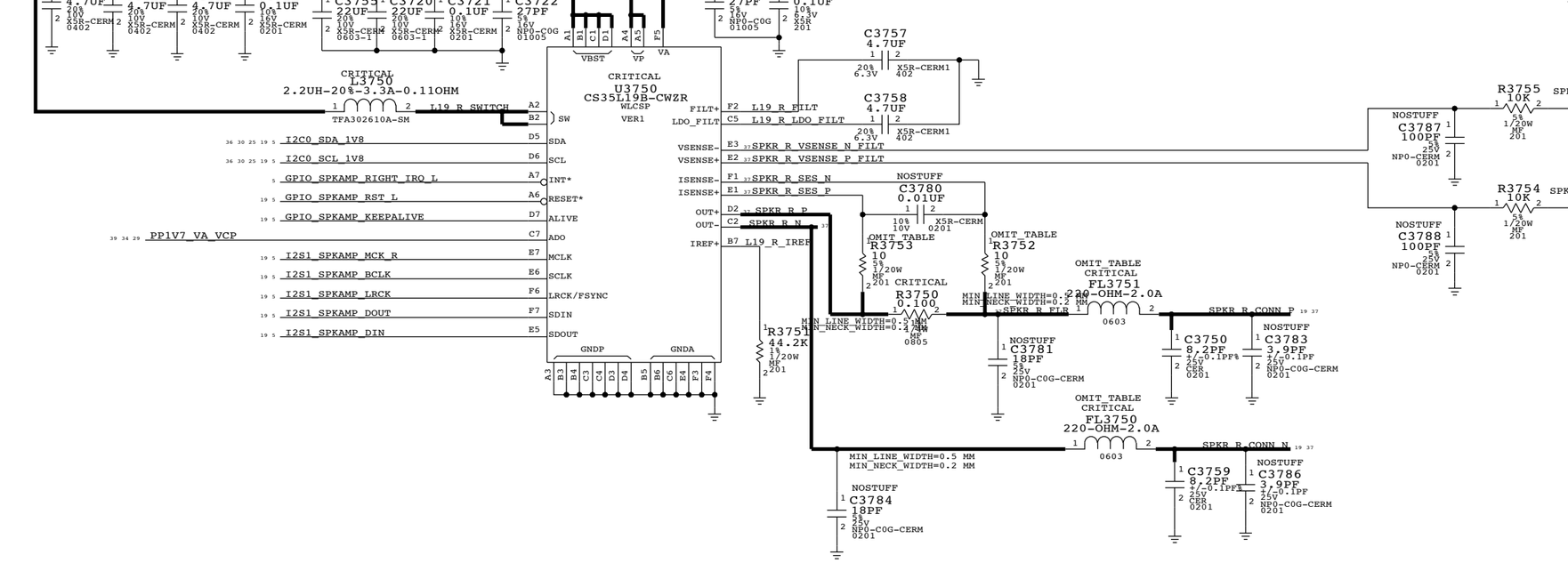
I2C ADDRESS: 1000000X

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0002	4	RES,MF,1/20W,0.00HM,5,0201,SMD	R3742,R3743,R3752,R3753	?	?
113S0022	4	RES,MF,1/10W,00HM,5,0603,SMD,LF	FL3740,FL3741,FL3750,FL3751	?	?

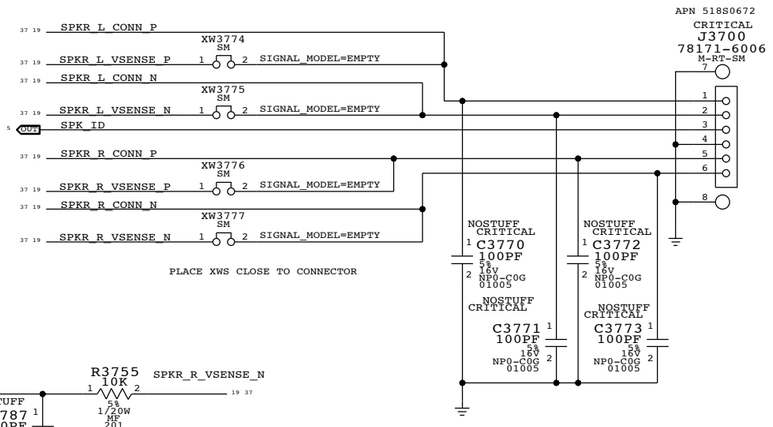


RIGHT SPEAKER AMP

I2C ADDRESS: 1000001X



SPEAKER CONNECTOR



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

AUDIO: SPEAKER AMP

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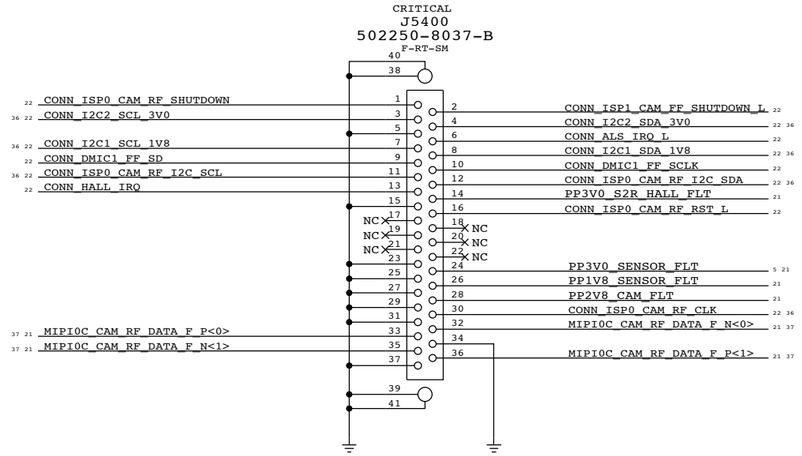
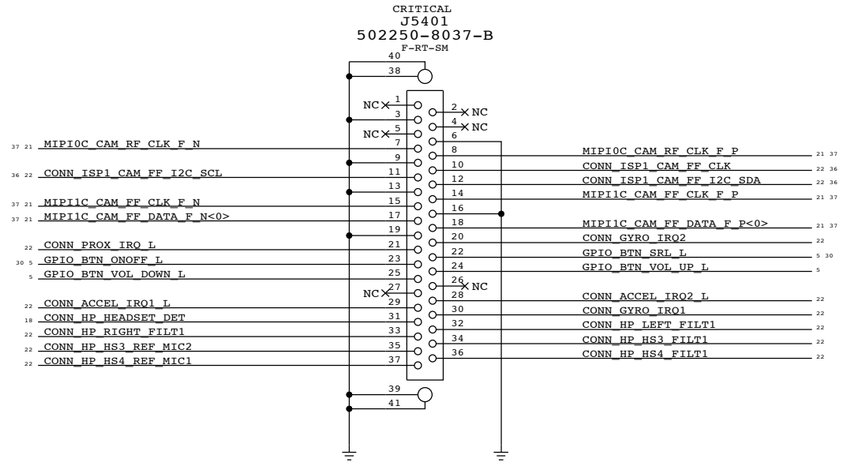
APN: 518S0828



APN: 518S0828



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PAGE TITLE

SENSOR FLEX CONN

Apple Inc.

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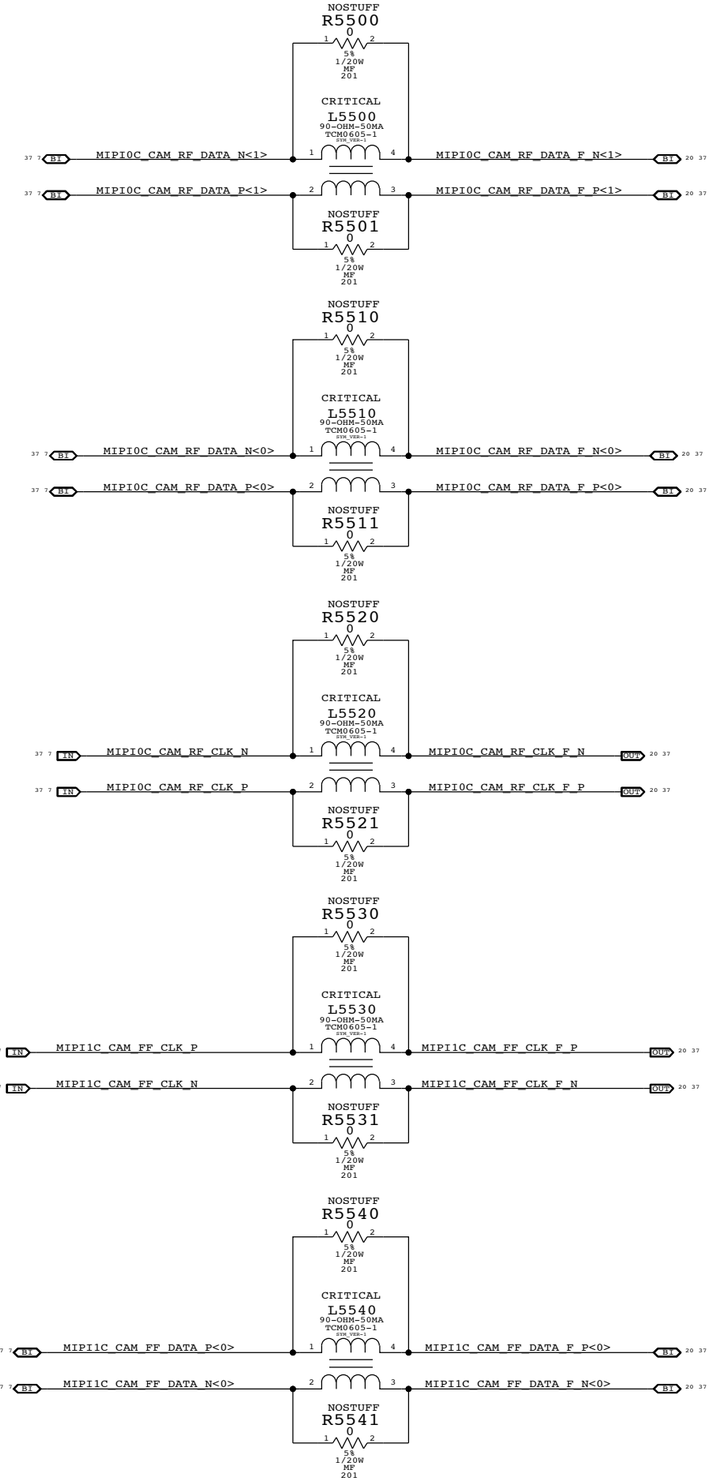

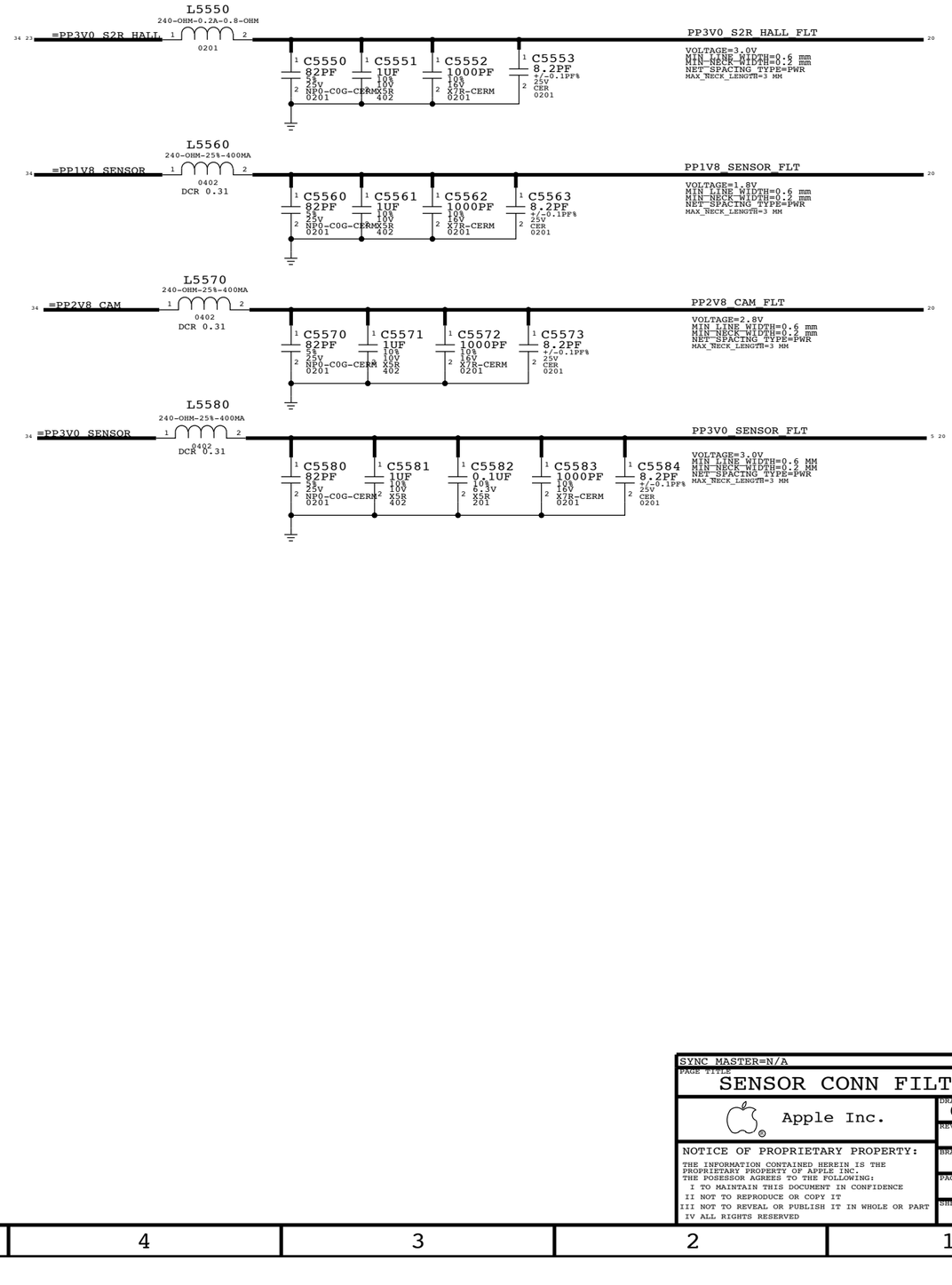

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PAGE TITLE

SENSOR CONN FILTERS 1

Apple Inc.

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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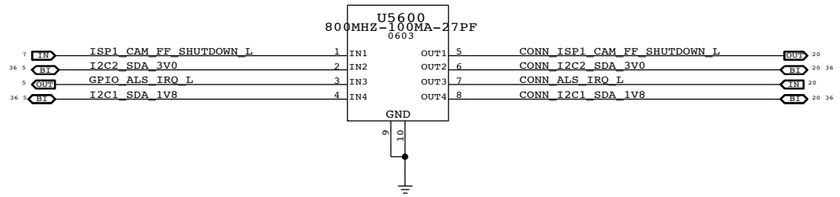

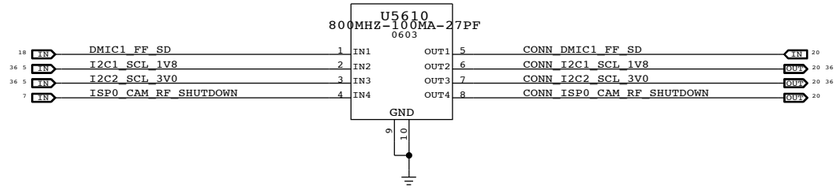

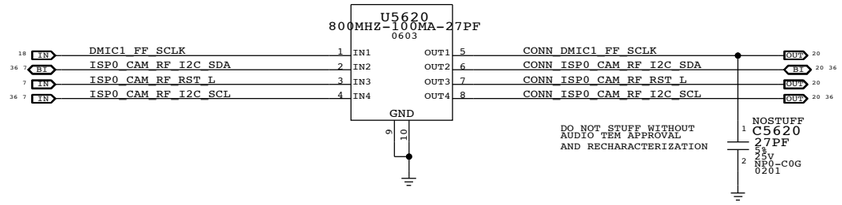

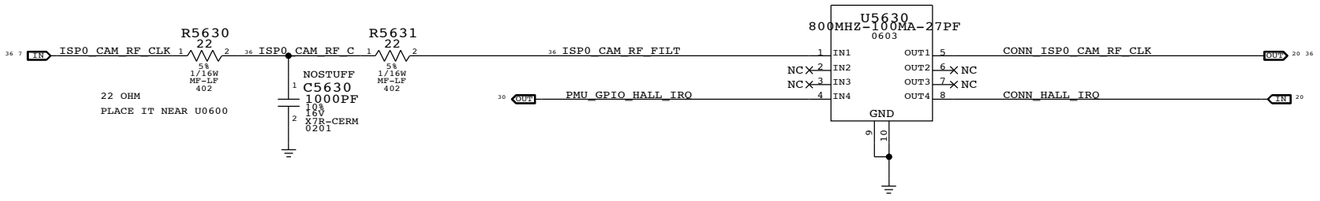

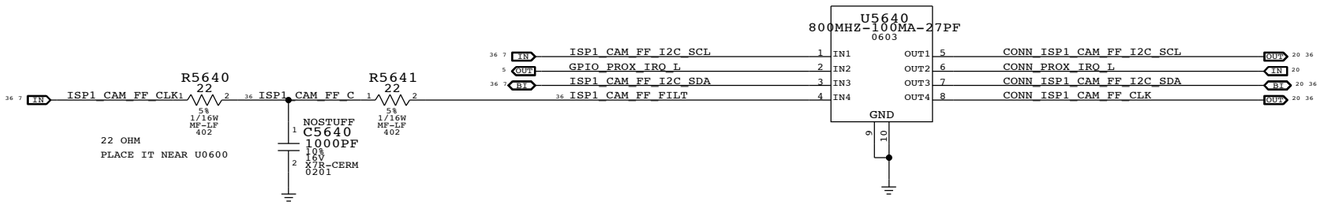

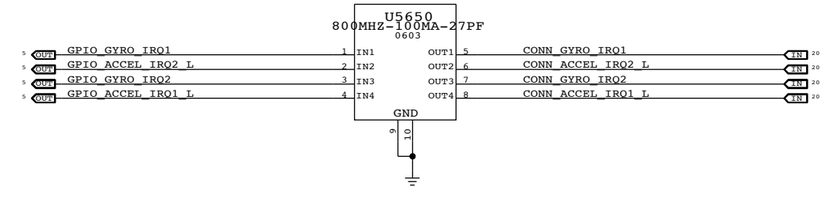

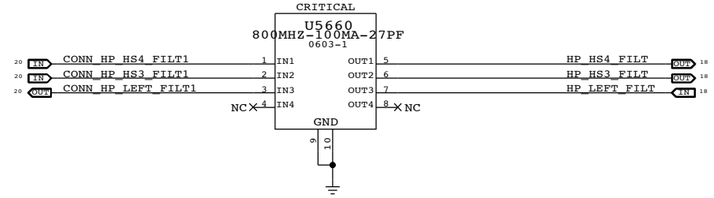

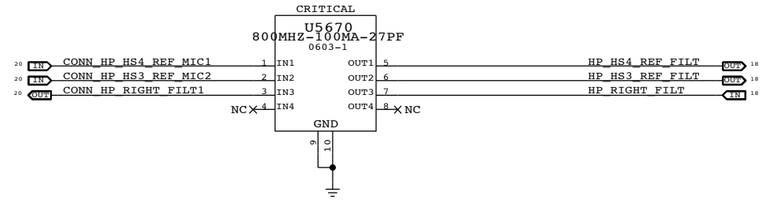

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PAGE TITLE
SENSOR CONN FILTERS 2

Apple Inc.

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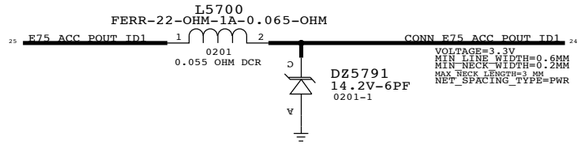

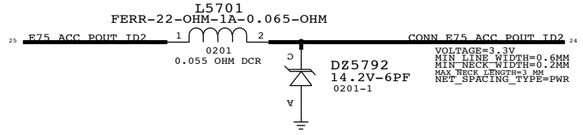

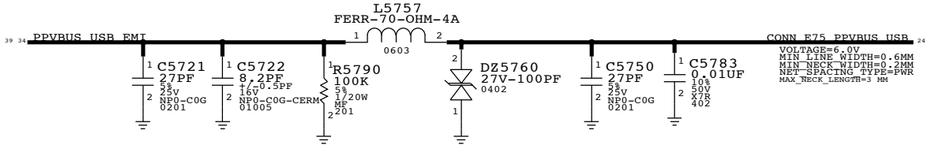

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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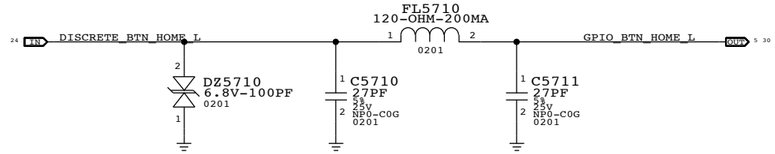
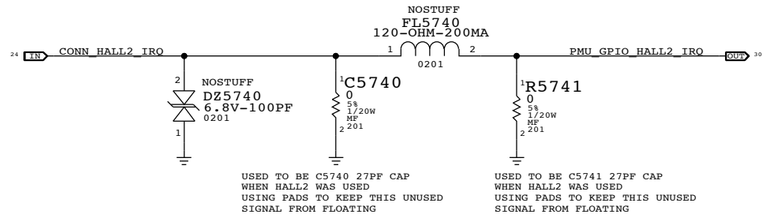
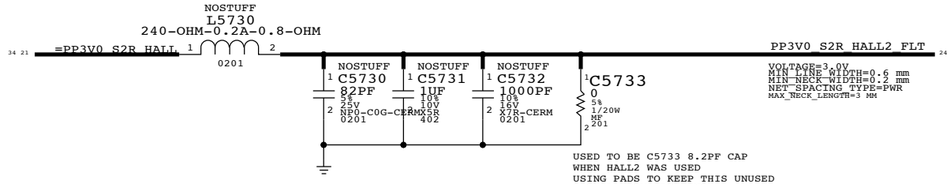
155S0657	155S0537		FL5710,FL5750	
155S0741	155S0397		L5757	<RDAR://PROBLEM/11238851>





USED TO BE C5740 27PF CAP
WHEN HALL2 WAS USED
USING PADS TO KEEP THIS UNUSED
SIGNAL FROM FLOATING

USED TO BE C5741 27PF CAP
WHEN HALL2 WAS USED
USING PADS TO KEEP THIS UNUSED
SIGNAL FROM FLOATING



USED TO BE C5733 8.2PF CAP
WHEN HALL2 WAS USED
USING PADS TO KEEP THIS UNUSED
SIGNAL FROM FLOATING

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
E75 DOCK SUPPORT

Apple Inc.

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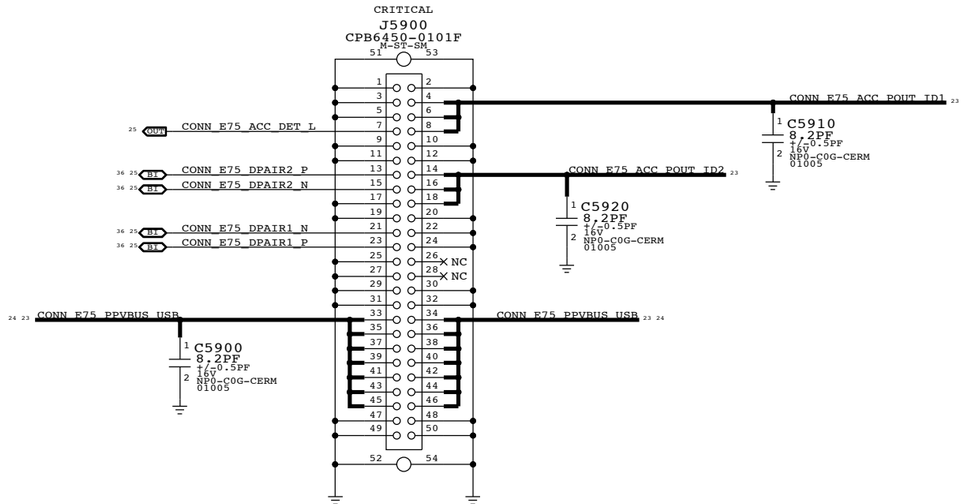
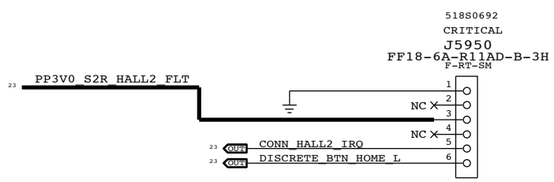
IO FLEX CONNECTOR

PN 516S0542 (PLUG - MALE)





SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE: IO FLEX CONN

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0614	1	IC,ASIC,TRISTAR,CBTL1608,A1,WLCSP36	U5900	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15580773	15580453	?	FL5990	<RDAR://PROBLEM/10882925>

TRISTAR BASEBAND USB MUX (NEEDED FOR MDM9600 BB)

BASEBAND USB MUX BYPASS

SEL	Y+	Y-
0	M+	M-
1	D+	D-

DEFAULT =>

NOTE: ISOLATE SELECT SIGNAL FROM PMU ON MLB_B AND MLB_C SO THE MUX IS PERMANENTLY POINTED TO THE DOCK

SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE	TRISTAR
DRAWING NUMBER	051-9385
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CELLULAR/GPS HOTBAR PADS

OMIT
998-3732
J6000
HOT-BAR-PADS
BB-SM

5	IN	BB_JTAG_TMS_RF	1	
			2	
34		=BATT_POS_F_3G	3	
			4	
			5	
			6	
			7	
			8	
			9	
27	IN	WLAN_TX_BLANK	10	
39 30 25 4	OUT	RST_AP_L	11	
5	IN	GPIO_BB_RADIO_ON_L	12	
30	IN	PMU_GPIO_BB_PMU_RST_L	13	
5	OUT	GPIO_BB_GSM_TXBURST	14	
39 5	IN	GPIO_BB_RST_L	15	
5	OUT	GPIO_BB_RESET_DET_L	16	
			17	
36 5	IN	GPIO_BB_HSIC_HOST_RDY	18	
36 5	OUT	GPIO_BB_HSIC_RESUME	19	
5	OUT	BB_JTAG_TDO_RF	20	
5	IN	BB_JTAG_TDI_RF	21	
5	IN	BB_JTAG_TRST_RF_L	22	
5	OUT	GPIO_BB_GPS_SYNC	23	
30	OUT	PMU_GPIO_BB_HOST_WAKE	24	
			25	
30	IN	BB_VBUS_DET	26	
36 25	BI	USB_BBMUX_BB_P	27	
36 25	BI	USB_BBMUX_BB_N	28	
			29	
36 25 5	OUT	UART1_BB_RXD	30	
36 25 5	IN	UART1_BB_TXD	31	
36 5	OUT	UART1_BB_CTS_L	32	
36 5	IN	UART1_BB_RTS_L	33	
			34	
5	BI	GPIO_AP_MODEM_WAKE	35	
36 5	OUT	GPIO_BB_HSIC_DEV_RDY	36	
			37	
36 26 4	BI	HSIC3_BB_STB	38	
			39	
36 26 4	BI	HSIC3_BB_DATA	40	
			41	
5	IN	BB_JTAG_TCK_RF	42	

DEBUG

NOSTUFF
J6050
MM4829-2702
F-ST-SM

36 26 4 HSIC3_BB_STB — 1

NOSTUFF
J6051
MM4829-2702
F-ST-SM

36 26 4 HSIC3_BB_DATA — 1

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: CELLULAR

Apple Inc.

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WLAN/BT

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0171	1	WIFI MODULE - MURATA	U6101_RF	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0175	339S0171		U6101_RF	WIFI MODULE - USI
311S0548	311S0398		U6102_RF	

ANTENNA CONNECTOR

CRITICAL
J6190_RF
MM4829-2702
F-ST-SM

CRITICAL
L6193_RF
1.3NH+/-0.2NH-T.2A-17MOHM
0402

RF_ANT
WIFI 50S
50_OHM

RF_ANT_MATCH1
WIFI 50S
50_OHM

NOSTUFF
L6190_RF
5.6NH+/-0.3NH
0402

CRITICAL
C6191_RF
0.3PF
+/-0.1PF
50V
CERM
0402

CONDUCTED TEST PORT

CRITICAL
J6191_RF
MM8030-2600RK0
F-ST-SM

RF_CAL
WIFI 50S
50_OHM

CRITICAL
C6192_RF
8.2PF
+/-0.25PF%
25V
NP0-C0G
0201

RF_CAL_MATCH
WIFI 50S
50_OHM

NOSTUFF
L6191_RF
5.6NH-3%-0.35A
0201

NOSTUFF
L6192_RF
5.6NH-3%-0.35A
0201

CRITICAL
U6104_RF
DPX205850DT-9038A1SJ
SM

XW6102_RF
SHORT-0402

=BATT_VCC

BATT_VCC_WLAN

C6101_RF
10UF
20%
6.3V
CERM-X5R
0402-1

C6102_RF
27PF
5%
16V
NP0-C0G
01005

PP_WLAN_VDDIO_1V8
VOLTAGE=1.8V

R6108_RF
0.00
0%
1/32W
MF
01005

PP_WL_BT_VDDIO_AP
VOLTAGE=1.8V

C6103_RF
0.01UF
10%
6.3V
X5R
01005

C6104_RF
27PF
5%
16V
NP0-C0G
01005

NOSTUFF
R6105_RF
10K
5%
1/32W
MF
01005

R6107_RF
10K
5%
1/32W
MF
01005

VDDIO_1P8V

BATT_VCC

VBATT_RF_VCC

VBATT_RF_VCC

32K INTERFACE TO AP

XW6101_RF
SHORT-01005

CLK32K_AP

WLAN_CLK32K

CLK32K_AP

GPIO_6

GPIO_6

WLAN_BUCK_OUT

VIN_1P2LDO

CRITICAL
L6111_RF
2.5UH-30%-0.7A-0.24OHM
0603

C6109
4.7UF
20%
6.3V
X5R-CERM1
402

WLAN_REG_ON

WL_REG_ON

BT_REG_ON

BT_REG_ON

JTAG_SEL

JTAG_SEL

WLAN_SR_VLX1

SR_VLX

50_HSIC_WLAN_DATA

WLAN_HSIC_DATA

50_HSIC_WLAN_STROBE

WLAN_HSIC_STROBE

R6109_RF
10K
5%
1/32W
MF
01005

NC

RF_SW_CTRL_3

NO LONGER NEEDED BASED ON AND GATE REMOVAL

U6101_RF
LBEE5ZHTWC501
LGA
OMIT_TABLE

2G_ANT

5G_ANT

50_WLAN_G

50_WLAN_A

HOST_WAKE_BT

BT_WAKE

BT_UART_RXD

BT_UART_TXD

BT_UART_RTS*

BT_UART_CTS*

BT_PCM_CLK

BT_PCM_SYNC

BT_PCM_OUT

BT_PCM_IN

GPIO_0 HOST_WAKE_WLAN

GPIO_1 AP_HSIC3_RDY

GPIO_2 WLAN_HSIC3_RESUME

GPIO_3 AGG_CHANNEL

GPIO_4 WLAN_UART_RXD

GPIO_5 WLAN_UART_TXD

GPIO_12 HSIC_DEVICE_RDY

GND

THRML_PAD

CRITICAL
C6107_RF
8.2PF
+/-0.25PF%
25V
NP0-C0G
0201

50_WLAN_G_1

CRITICAL
C6108_RF
4.7PF
+/-0.1PF
25V
C0G-CERM
0201

50_WLAN_A_DIPLX

NOSTUFF
C6111_RF
0.2PF
+/-0.1PF
25V
C0G-CERM
201

R6111_RF
10K
5%
1/32W
MF
01005

PULL DOWN RESISTORS

GPIO6	SDIO_DATA<1>	SDIO_DATA<2>	MODE	DEFAULT ARM STATE
0	X	X	SDIO	IN RESET
1	X	0	GSPI	IN RESET
1	0	1	HSIC	OUT OF RESET
1	1	1	BOOTLESS HSIC	IN RESET

PP_WL_BT_VDDIO_AP

R6113_RF
10K
5%
1/32W
MF
01005

HSIC_DEVICE_RDY

U6102_RF
74AUP1G08GF
SOT891

R6112_RF
1.00M
1%
1/32W
MF
01005

WLAN_REG_ON

WLAN_REG_ON_RC

C6110_RF
0.22UF
20%
6.3V
X5R
0201

NC

DEV_HSIC3_RDY

R6114_RF
0.00
0%
1/32W
MF
01005

AGG_CHANNEL

WLAN_TX_BLANK

WLAN_REG_ON PP6102_RF P4MM

HOST_WAKE_WLAN PP6103_RF P4MM

AP_HSIC3_RDY PP6104_RF P4MM

DEV_HSIC3_RDY PP6105_RF P4MM

WLAN_UART_RXD PP6106_RF P4MM

WLAN_UART_TXD PP6107_RF P4MM

AGG_CHANNEL PP6109_RF P4MM

50_HSIC_WLAN_DATA PP6110_RF P4MM

50_HSIC_WLAN_STROBE PP6111_RF P4MM

HSIC_DEVICE_RDY PP6112_RF P4MM

CHANGE LIST

07FEB2012 MUSHTAQ COPIED FROM N41, ADDED J2 ANT MATCH/CONN
C6107 FROM 20PF TO 8.2PF, C6108 FROM 10PF TO 4.7PF
U6104 FROM SOSHIN TO MURATA LFD212G45DS5D355

13FEB2012 AMANDA CHANGED OMIT TO OMIT_TABLE AND UPDATED
BOM OPTION TABLES TO ALTERNATE TABLES
REMOVED BOM TABLE FOR C6111_RF (NOW ALWAYS NOSTUFF)

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: WIFI/BT

Apple Inc.

DRAWING NUMBER: 051-9385 SIZE: D

REVISION: 10.0.0

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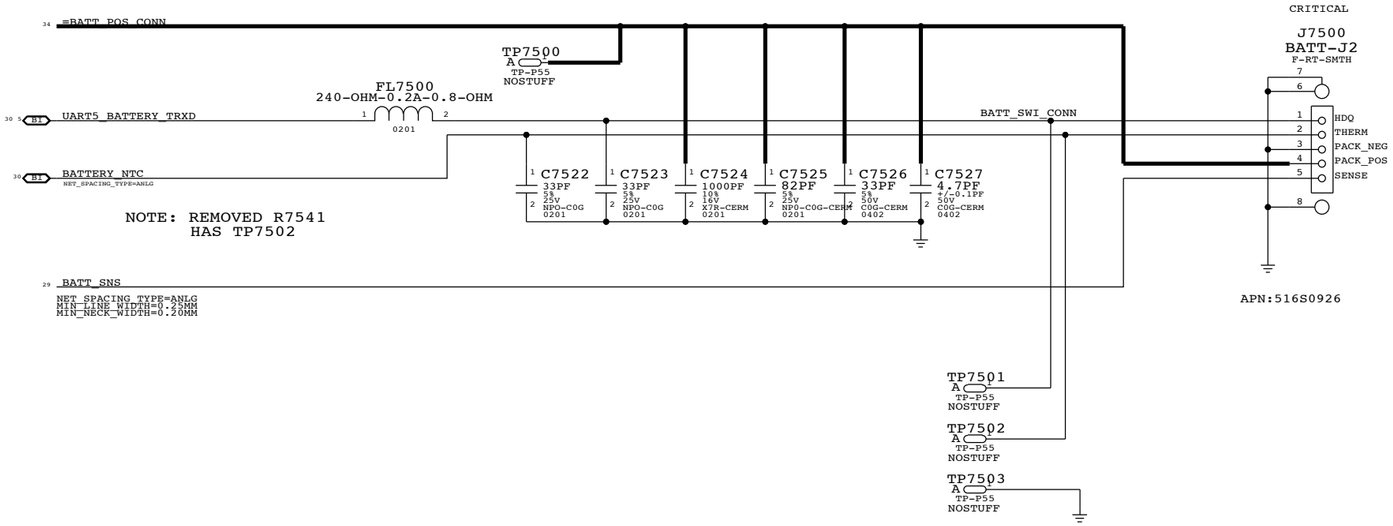
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0274	?		<RADAR://PROBLEM/11282371>

FL7500,L3620,L5550,L5730



SYNC MASTER=MADHAVI SYNC DATE=12/06/2011

PAGE TITLE

POWER: BATTERY CONNECTOR

Apple Inc.

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REVISION 10.0.0

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VCC_MAIN BYPASS

TOTAL CAPS = ~400UF

PLACE ONE 10UF CAP AT EACH VDD INPUT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1637	6	IND,1.0UH,20%,59MO,2.74A	L8100,L8101,L8102,L8103,L8109,L8110	CRITICAL	
152S1638	1	IND,1.0UH,20%,64MO,2.3A	L8104	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1452	152S1292	?	L8111	RDAR://PROBLEM/8376462
138S0676	138S0654	?		?

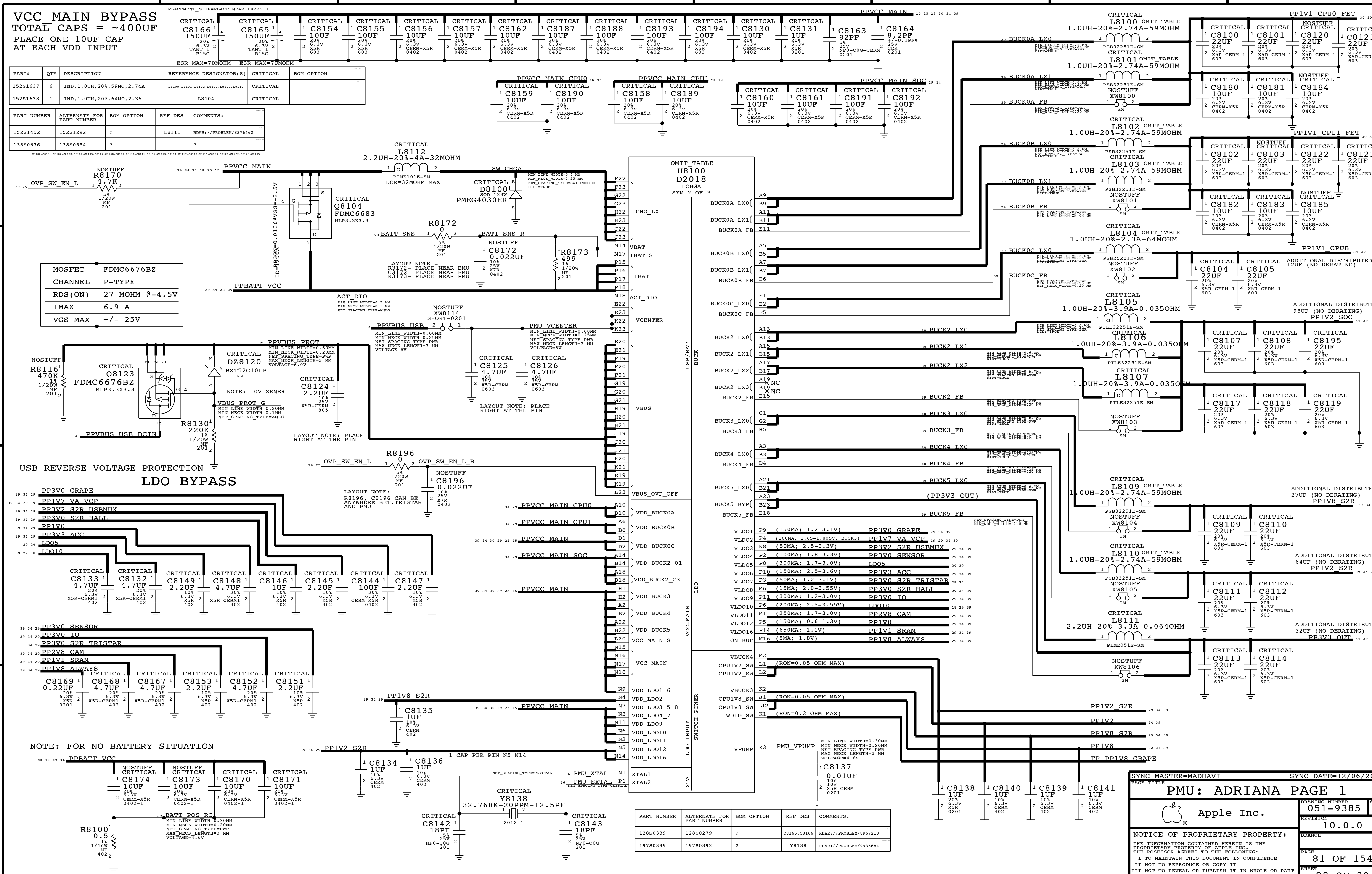
C8100,C8101,C8102,C8103,C8104,C8105,C8107,C8108,C8109,C8110,C8111,C8112,C8113,C8114,C8117,C8118,C8119,C8120,C8121,C8222,C8123,C8195

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

USB REVERSE VOLTAGE PROTECTION

LDO BYPASS

NOTE: FOR NO BATTERY SITUATION



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0339	128S0279	?	C8165,C8166	RDAR://PROBLEM/8967213
197S0399	197S0392	?	Y8138	RDAR://PROBLEM/9936684

SYNC_MASTER=MADHAVI SYNC_DATE=12/06/2011

PAGE TITLE: PMU: ADRIANA PAGE 1

Apple Inc.

DRAWING NUMBER: 051-9385 SIZE: D

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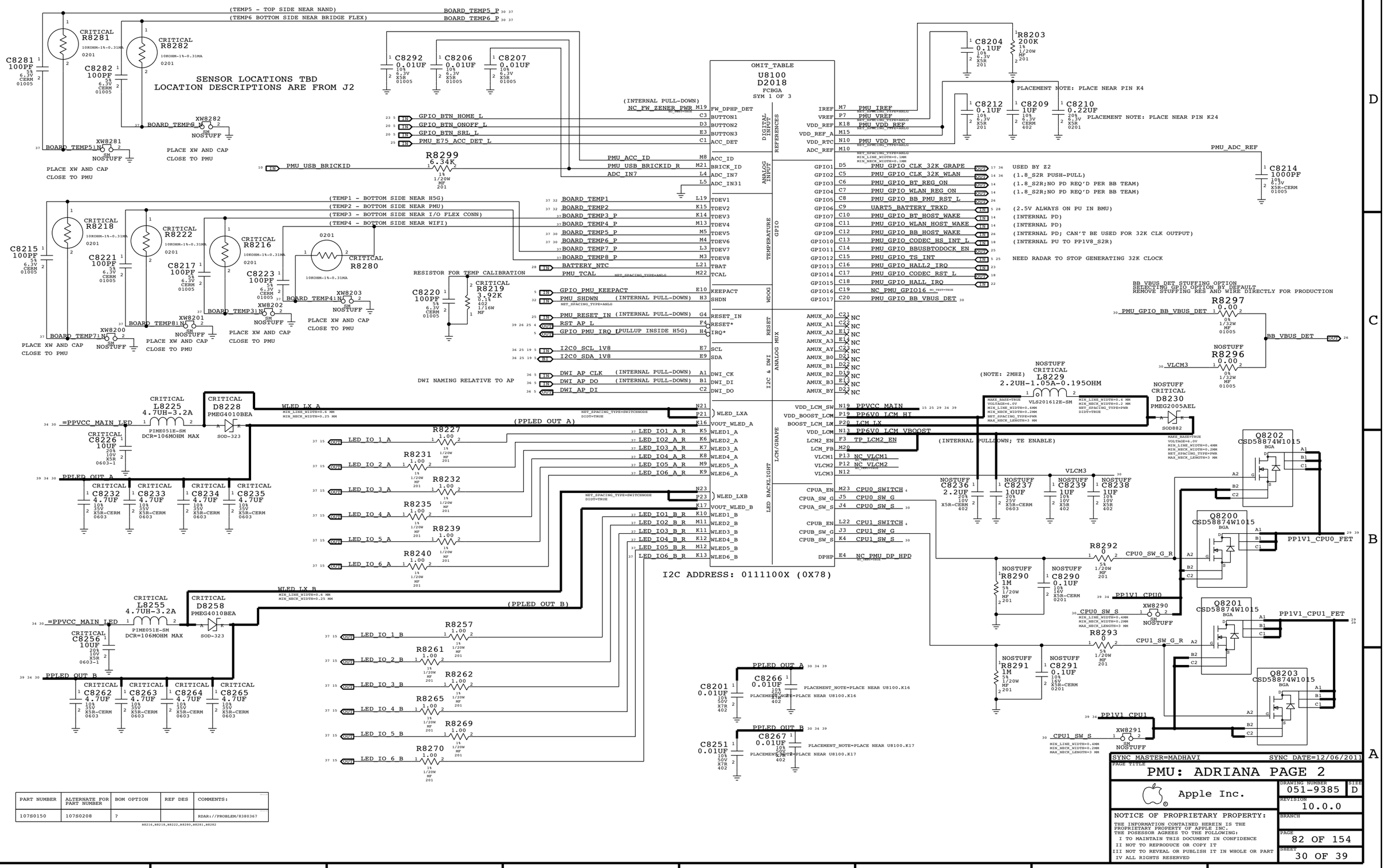
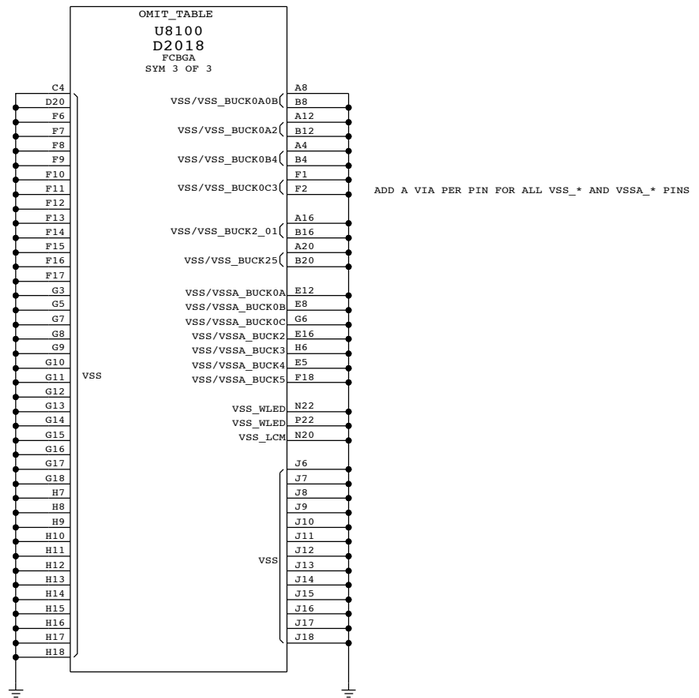


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	?		RDAR://PROBLEM/8380367

88216,88218,88222,88280,88281,88282



SYNC_MASTER=MADHAVI SYNC_DATE=12/06/2011

PAGE TITLE

PMU: ADRIANA PAGE 3

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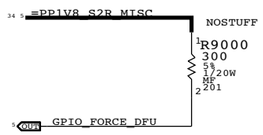
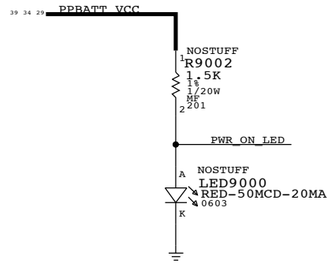
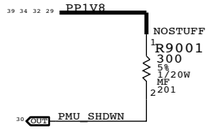
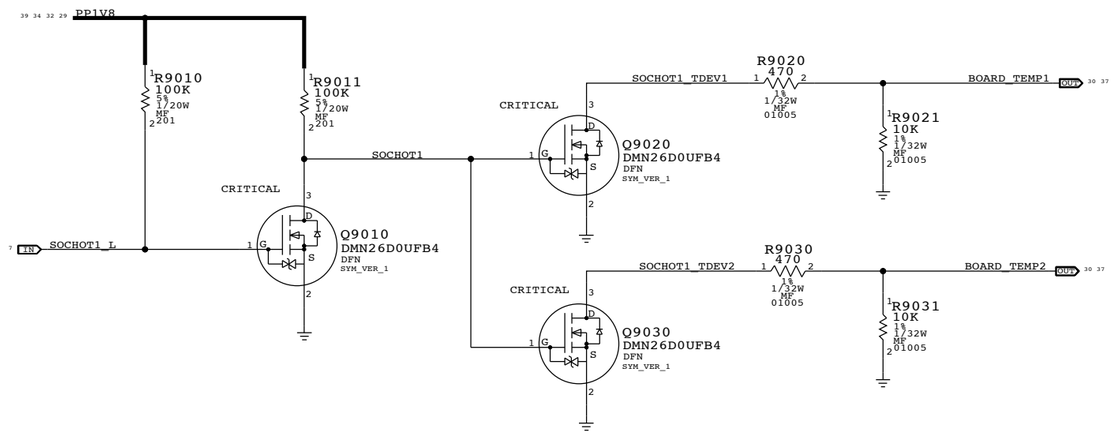
DEBUG RESET ACCESS







SOCHOT TO PMU TDEV1/TDEV2



SYNC_MASTER=MLB SYNC_DATE=11/09/2011

PAGE TITLE

DEBUG/MISC.

Apple Inc.

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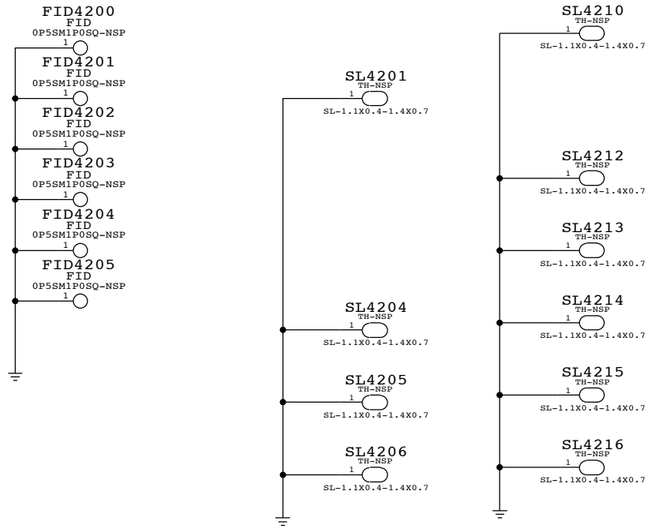
PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM



SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE
TEST/HOLES/FIDUCUALS

Apple Inc.

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POWER CONNECTIONS

BUCK0A

39 30 PP1V1_CPU0 → =PPVDD_CPU0_H5 9

MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK0B

39 30 PP1V1_CPU1 → =PPVDD_CPU1_H5 9

MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK0C

39 29 PP1V1_CPUB → =PPVDD_CPUB_H5 9

MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK2

39 29 PP1V2_SOC → =PPVDD_SOC_H5 9

MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK3

39 29 PP1V8_S2R
- → =PP1V8_S2R_MISC 5 32
- → VDDIO_WLAN_BT_1V8 14
- → =PP1V8_S2R_USBMUX 25
- → =PP1V8_S2R_DDR 11 12

MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK4

39 29 PP1V2_S2R
- → =PP1V2_S2R_H5 8
- → =PP1V2_S2R_DDR 11 12

MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK3_SW

CPU1V8_SW

32 29 39 PP1V8
- → =PP1V8_SENSOR 21
- → =PP1V8_AUDIO 18
- → =PP1V8_VDDIO18_H5 4 6 7 9
- → =PP1V8_H5 4 5 7 10
- → =PP1V8_MIPI_H5 7
- → =PP1V8_DP_H5 7
- → =PP1V8_EDP_H5 7
- → =PP1V8_NAND_H5 6 9
- → =PP1V8_NAND 13
- → =PP1V8_PLL_H5 4
- → =PP1V8_MISC 16

MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3MM

BUCK4_SW

CPU1V2_SW

39 29 PP1V2
- → =PP1V2_VDDQ_DDR 11 12
- → =PP1V2_VDDIOD_H5 8 9
- → =PP1V2_HSIC_H5 4

MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK5

39 29 PP3V3_OUT
- → =PP3V3_NAND 13
- → =PP3V3_USB_H5 4
- → =PP3V3_LCD 15

MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BACKLIGHT BOOST

39 30 PPLED_OUT_A → =PPLED_REG_A 15

MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

39 30 PPLED_OUT_B → =PPLED_REG_B 15

MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO1

39 29 PP3V0_GRAPE
- → =PP3V0_GRAPE 16 17
- → =PP3V0_GRAPE_MARIO1 16
- → =PP3V0_GRAPE_Z1 17
- → =PP3V0_GRAPE_Z2 17

MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO2

39 29 19 PP1V7_VA_VCP → =PP1V7_VA_VCP 18 19

MAKE_BASE=TRUE
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO3 (NO LONGER NEEDED)

39 29 PP3V2_S2R_USBMUX → =PP3V2_S2R_USBMUX 25

MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO4

39 29 PP3V0_SENSOR → =PP3V0_SENSOR 21

MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO6

39 29 PP3V3_ACC → =PP3V3_ACC 25

MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO7

29 PP3V0_S2R_TRISTAR → =PP3V0_S2R_TRISTAR 25

MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO8

39 29 PP3V0_S2R_HALL → 1927 =PP3V0_S2R_HALL 21 23

MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO9

39 29 PP3V0_IO → =PP3V0_VDDIO30_H5 9

MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO11

39 29 PP2V8_CAM → =PP2V8_CAM 21

MAKE_BASE=TRUE
VOLTAGE=2.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO12

39 29 PP1V0
- → =PP1V0_MIPI_H5 7
- → =PP1V0_DP_PAD_DVDD_H5 7
- → =PP1V0_EDP_PAD_DVDD_H5 7
- → =PP1V0_USB_H5 4
- → =PP1V0_HSIC_H5 4
- → =PP1V0_MIPI_PLL_H5 7

MAKE_BASE=TRUE
VOLTAGE=1.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO16

39 29 PP1V1_SRAM → =PPVDD_SRAM_H5 9

MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

39 29 PP1V8_ALWAYS → =PP1V8_ALWAYS 5

MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

CHARGER MAIN

39 30 29 25 15 PPVCC_MAIN
- → =PPVCC_MAIN_AUDIO 18 19
- → =PPVCC_MAIN_LED 30
- → PPVCC_MAIN_CPU0 29
- → PPVCC_MAIN_CPU1 29
- → PPVCC_MAIN_SOC 29

MAKE_BASE=TRUE
VOLTAGE=4.7V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BATTERY

39 32 29 PPBATT_VCC
- → =BATT_POS_CONN 28
- → =BATT_POS_F_3G 26 — CELLULAR RADIO
- → =BATT_VCC 27 — WLAN

MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

USB POWER INPUT

39 23 PPVBUS_USB_EMI → PPVBUS_USB_DCIN 29

MAKE_BASE=TRUE
VOLTAGE=6V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
POWER ALIASES

Apple Inc.

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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,BOTTOM	NO_TYPE,BGA,BGA06-06,BGA_P4	MM	16.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	3.0 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES 45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL2,ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL3,ISL8	Y	0.065 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4,ISL7	Y	0.053 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL5	Y	0.072 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL6	Y	0.059 MM	0.055 MM	3.0 MM		

90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
90_OHM_DIFF	ISL2,ISL9	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL3,ISL8	Y	0.062 MM	0.052 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL4,ISL7	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL5,ISL6	Y	0.052 MM	0.052 MM	=STANDARD	0.105 MM	0.105 MM

DDR 45 OHMS SINGLE-ENDED PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_45_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.105 MM	3.0 MM		
DDR_45_OHM_SE	ISL2	Y	0.055 MM	0.055 MM	3.0 MM		
DDR_45_OHM_SE	ISL3	Y	0.065 MM	0.065 MM	3.0 MM		
DDR_45_OHM_SE	ISL4	Y	0.053 MM	0.053 MM	3.0 MM		
DDR_45_OHM_SE	ISL5,ISL6	Y	0.072 MM	0.072 MM	3.0 MM		
DDR_45_OHM_SE	*	N	0.055 MM	0.055 MM	3.0 MM		

DDR 90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_90_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
DDR_90_OHM_DIFF	ISL2	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL3	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL4	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL5,ISL6	Y	0.066 MM	0.066 MM	=STANDARD	0.180 MM	0.180 MM
DDR_90_OHM_DIFF	*	N	0.056 MM	0.056 MM	=STANDARD	0.180 MM	0.180 MM

WIFI PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WIFI_50S	TOP,BOTTOM	Y	0.245 MM	0.2 MM	=STANDARD		
WIFI_50S	*	N	=STANDARD	=STANDARD	=STANDARD		
WIFI_PWR100	*	Y	0.10 MM	0.050 MM	=STANDARD		
WIFI_PWR1000	*	Y	1.00 MM	0.100 MM	=STANDARD		

MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.5 MM	0.20 MM	10 MM	0.10 MM	0.10 MM
AUDIO_DIFF	*	Y	0.1 MM	0.09 MM	10 MM	0.10 MM	0.10 MM
LED	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM
TEMP_SENSE	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

TCF VERSION (USING SPACING RULE)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TCF_VERSION	*	0.104 MM	?

0.104 - 11/30/2011

E1 TCF_VERSION NC_UART5_TXD : ASSIGNING RULE TO NC NET

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.100 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?
BGA_P4_SPA	*	0.200 MM	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.050 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.075 MM	?
2:1_SPACING	*	0.100 MM	?
2.5:1_SPACING	*	0.125 MM	?
3:1_SPACING	*	0.150 MM	?
4:1_SPACING	*	0.200 MM	?
5:1_SPACING	*	0.250 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?
0P2_SPACING	*	0.20 MM	?

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	
GND_P1SPACING	*	0.1 MM	
SWITCHNODE	*	0.2 MM	

POWER

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PWR	*	Y	0.6MM	0.20 MM	3.0 MM		
GND_PH	*	Y	0.6MM	0.075 MM	3.0 MM		
PWR_PMU	*	Y	0.6MM	0.20 MM	3.0 MM		

MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING
*	*	BGA_P4	BGA_P4_SPA

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

SYNC MASTER=MIKE SYNC DATE=11/30/2011

PAGE TITLE
CONSTRAINTS: MLB RULES

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B16	CLK_50S	CLK	PMU_GPIO_CLK_32K_GRAPE	17 30
B17	CLK_50S	CLK	PMU_GPIO_CLK_32K_WLAN	14 30
B18	CLK_50S	CLK	ISP1_CAM_FF_CLK	7 22
B19	CLK_50S	CLK	CONN_ISP1_CAM_FF_CLK	20 22
B20	CLK_50S	CLK	ISP0_CAM_RF_CLK	7 22
B21	CLK_50S	CLK	CONN_ISP0_CAM_RF_CLK	20 22
B22	I2S_50S	I2S	I2S0_CODEC_ASP_MCK	5 36
B23	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R	5 18 36
B24	CLK_50S	CLK	ISP0_CAM_RF_CLK_R	7
B25	CLK_50S	CLK	ISP1_CAM_FF_CLK_R	7
B26	CLK_50S	CLK	ISP1_CAM_FF_C	22
B27	CLK_50S	CLK	ISP0_CAM_RF_C	22
B28	CLK_50S	CLK	ISP1_CAM_FF_FILT	22
B29	CLK_50S	CLK	ISP0_CAM_RF_FILT	22

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	3:1_SPACING
UART	UART	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B29	UART_50S	UART	UART2_TS_ACC_RXD	5 25
B30	UART_50S	UART	UART2_TS_ACC_TXD	5 25
B31	UART_50S	UART	UART4_WLAN_RXD	5 14
B32	UART_50S	UART	UART4_WLAN_TXD	5 14
B33	UART_50S	UART	UART1_BB_CTS_L	5 26
B34	UART_50S	UART	UART1_BB_RTS_L	5 26
B35	UART_50S	UART	UART1_BB_TXD	5 25 26
B36	UART_50S	UART	UART1_BB_RXD	5 25 26
B37	UART_50S	UART	UART3_BT_CTS_L	5 14
B38	UART_50S	UART	UART3_BT_RTS_L	5 14
B39	UART_50S	UART	UART3_BT_RXD	5 14
B40	UART_50S	UART	UART3_BT_TXD	5 14
B41	UART_50S	UART	UART6_AP_RXD	5 25
B42	UART_50S	UART	UART6_AP_TXD	5 25

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B183	SPI_50S	SPI	SPI3_GRAPE_MISO	5 16
B184	SPI_50S	SPI	SPI3_GRAPE_MOSI	5 16
B185	SPI_50S	SPI	SPI3_GRAPE_SCLK	5 16
B186	SPI_50S	SPI	SPI3_GRAPE_CS_L	5 16
B187	SPI_50S	SPI	SPI2_IPC_MISO	
B188	SPI_50S	SPI	SPI2_IPC_MOSI	
B189	SPI_50S	SPI	SPI2_IPC_SCLK	
B190	SPI_50S	SPI	GPIO_BB_HSIC_RESUME	5 26
B240	SPI_50S	SPI	SPI1_CODEC_MISO	5 18
B241	SPI_50S	SPI	SPI1_CODEC_MOSI	5 18
B242	SPI_50S	SPI	SPI1_CODEC_SCLK	5 18
B243	SPI_50S	SPI	SPI1_CODEC_CS_L	5 18

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B152		DWI	DWI_AP_CLK	5 30
B153		DWI	DWI_AP_DI	5 30
B154		DWI	DWI_AP_DO	5 30

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B16		JTAG	JTAG_AP_TCK	4 25
B15		JTAG	JTAG_AP_TMS	4 25
B14		JTAG	JTAG_AP_TDI	4
B13		JTAG	TP_JTAG_AP_TDO	4
B25		RST	JTAG_AP_TRST_L	4 10 39

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B19	I2C_50S	I2C	I2C1_SDA_1V8	5 22
B20	I2C_50S	I2C	I2C1_SCL_1V8	5 22
B21	I2C_50S	I2C	I2C0_SDA_1V8	5 19 25 30
B22	I2C_50S	I2C	I2C0_SCL_1V8	5 19 25 30
B23	I2C_50S	I2C	I2C2_SDA_3V0	5 22
B24	I2C_50S	I2C	I2C2_SCL_3V0	5 22
B26	I2C_50S	I2C	ISP0_CAM_RF_I2C_SCL	7 22
B27	I2C_50S	I2C	ISP0_CAM_RF_I2C_SDA	7 22
B28	I2C_50S	I2C	ISP1_CAM_FF_I2C_SCL	7 22
B29	I2C_50S	I2C	ISP1_CAM_FF_I2C_SDA	7 22
B30	I2C_50S	I2C	CONN_I2C1_SDA_1V8	20 22
B31	I2C_50S	I2C	CONN_I2C1_SCL_1V8	20 22
B32	I2C_50S	I2C	CONN_I2C2_SCL_3V0	20 22
B33	I2C_50S	I2C	CONN_I2C2_SDA_3V0	20 22
B34	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SCL	20 22
B35	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SDA	20 22
B36	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SCL	20 22
B37	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SDA	20 22

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B19		CRYSTAL	XTAL_AP_24M_I	4
B20		CRYSTAL	XTAL_AP_24M_O	4
B21		CRYSTAL	AP_24M_O	4
B22		CRYSTAL	PMU_XTAL	29
B23		CRYSTAL	PMU_EXTAL	29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B19	I2S_50S	I2S	I2S0_CODEC_ASP_BCLK	5 18
B20	I2S_50S	I2S	I2S0_CODEC_ASP_LRCK	5 18
B21	I2S_50S	I2S	I2S0_CODEC_ASP_DIN	5 18
B22	I2S_50S	I2S	I2S0_CODEC_ASP_DOUT	5 18
B23	I2S_50S	I2S	I2S0_CODEC_ASP_SDOUT	18
B24	I2S_50S	I2S	I2S0_CODEC_ASP_MCK	5 36
B25	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R	5 18 36
B27	I2S_50S	I2S	I2S3_CODEC_XSP_BCLK	5 18
B28	I2S_50S	I2S	I2S3_CODEC_XSP_LRCK	5 18
B29	I2S_50S	I2S	I2S3_CODEC_XSP_DIN	5 18
B30	I2S_50S	I2S	I2S3_CODEC_XSP_DOUT	5 18
B31	I2S_50S	I2S	I2S0_CODEC_XSP_SDOUT	
B34	I2S_50S	I2S	I2S2_BT_BCLK	5 14
B35	I2S_50S	I2S	I2S2_BT_LRCK	5 14
B36	I2S_50S	I2S	I2S2_BT_DIN	5 14
B38	I2S_50S	I2S	I2S2_BT_DOUT	5 14

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B5	USB_90D	USB	USB_AP_P	4 25
B6	USB_90D	USB	USB_AP_N	4 25
B246	USB_90D	USB	USB_BBMUX_BB_P	25 26
B247	USB_90D	USB	USB_BBMUX_BB_N	25 26
B248	USB_90D	USB	USB_TS_BBMUX_P	25
B249	USB_90D	USB	USB_TS_BBMUX_N	25
B270	USB_90D	USB	USB11_AP_BBMUX_P	4 25
B271	USB_90D	USB	USB11_AP_BBMUX_N	4 25
B258	USB_90D	USB	CONN_E75_DPAIR1_P	24 25
B259	USB_90D	USB	CONN_E75_DPAIR1_N	24 25
B260	USB_90D	USB	CONN_E75_DPAIR2_P	24 25
B261	USB_90D	USB	CONN_E75_DPAIR2_N	24 25
B262	USB_90D	USB	TS_E75_DPAIR1_P	25
B264	USB_90D	USB	TS_E75_DPAIR1_N	25
B265	USB_90D	USB	TS_E75_DPAIR2_P	25
B266	USB_90D	USB	TS_E75_DPAIR2_N	25

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	4:1_SPACING
HSIC_RDY	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B181	HSIC	HSIC	HSIC3_BB_DATA	4 26
B183	HSIC	HSIC	HSIC3_BB_STB	4 26
B191	HSIC	HSIC	HSIC1_WLAN_DATA	4 14
B192	HSIC	HSIC	HSIC1_WLAN_STB	4 14
B195	HSIC	HSIC_RDY	GPIO_BB_HSIC_DEV_RDY	5 26
B196	HSIC	HSIC_RDY	GPIO_BB_HSIC_HOST_RDY	5 26
B197	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY	5 14 36
B198	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY	5 14 36
B199	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_DEV_RDY	5 14

SYNC_MASTER=MIKE SYNC_DATE=11/30/2011

PAGE TITLE

CONSTRAINTS: LOW SPEED BUS

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MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI0C	*	*	4:1_SPACING
MIPI1C	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
J215	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_P	7 21
J216	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_N	7 21
J243	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_P<0>	7 21
J242	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_N<0>	7 21
J211	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_P<1>	7 21
J212	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_N<1>	7 21
J205	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_F_P	20 21
J204	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_F_N	20 21
J318	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_P<0>	20 21
J316	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_N<0>	20 21
J321	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_P<1>	20 21
J320	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_N<1>	20 21
J345	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_P	7 21
J346	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_N	7 21
J367	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_P<0>	7 21
J368	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_N<0>	7 21
J356	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_P	20 21
J358	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_N	20 21
J415	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_P<0>	20 21
J416	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_N<0>	20 21

AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
E584	AUDIO_DIFF	AUDIO	HP_MIC_P	18
E585	AUDIO_DIFF	AUDIO	HP_MIC_N	18
E587	AUDIO_DIFF	AUDIO	L81_AIN2_P	18
E586	AUDIO_DIFF	AUDIO	L81_AIN2_N	18
E589	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N_FILT	19
E588	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P_FILT	19
E591	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N	19
E590	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P	19
E592	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N_FILT	19
E593	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P_FILT	19
E594	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N	19
E595	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P	19
E597	SPEAKER	AUDIO	SPKR_L_P	19
E596	SPEAKER	AUDIO	SPKR_L_N	19
E598	SPEAKER	AUDIO	SPKR_L_CONN_P	19
E599	SPEAKER	AUDIO	SPKR_L_CONN_N	19
E606	SPEAKER	AUDIO	SPKR_R_P	19
E607	SPEAKER	AUDIO	SPKR_R_N	19
E608	SPEAKER	AUDIO	SPKR_R_CONN_P	19
E609	SPEAKER	AUDIO	SPKR_R_CONN_N	19
E610	SPEAKER	AUDIO	SPKR_L_FLR	19
E611	SPEAKER	AUDIO	SPKR_R_FLR	19
E564	AUDIO_DIFF	AUDIO	SPKR_L_SES_N	19
E565	AUDIO_DIFF	AUDIO	SPKR_L_SES_P	19
E566	AUDIO_DIFF	AUDIO	SPKR_R_SES_N	19
E567	AUDIO_DIFF	AUDIO	SPKR_R_SES_P	19
E602	USB_90D	USB	MIKEY_TS_P	18 25
E603	USB_90D	USB	MIKEY_TS_N	18 25
E600	USB_90D	USB	L81_MBUS_P	18
E601	USB_90D	USB	L81_MBUS_N	18

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
E435	EDP_90D	EDP	EDP_AUX_P	7 15
E436	EDP_90D	EDP	EDP_AUX_N	7 15
E437	EDP_50S	EDP	EDP_HPD	7 15
E438	EDP_90D	EDP	EDP_DATA_P<0>	7 15
E439	EDP_90D	EDP	EDP_DATA_N<0>	7 15
E440	EDP_90D	EDP	EDP_DATA_P<1>	7 15
E442	EDP_90D	EDP	EDP_DATA_N<1>	7 15
E443	EDP_90D	EDP	EDP_DATA_P<2>	7 15
E444	EDP_90D	EDP	EDP_DATA_N<2>	7 15
E447	EDP_90D	EDP	EDP_DATA_P<3>	7 15
E445	EDP_90D	EDP	EDP_DATA_N<3>	7 15
E447	EDP_90D	EDP	EDP_AUX_EMI_P	15
E446	EDP_90D	EDP	EDP_AUX_EMI_N	15
E449	EDP_90D	EDP	EDP_DATA_EMI_P<0>	15
E448	EDP_90D	EDP	EDP_DATA_EMI_N<0>	15
E450	EDP_90D	EDP	EDP_DATA_EMI_P<1>	15
E451	EDP_90D	EDP	EDP_DATA_EMI_N<1>	15
E453	EDP_90D	EDP	EDP_DATA_EMI_P<2>	15
E452	EDP_90D	EDP	EDP_DATA_EMI_N<2>	15
E455	EDP_90D	EDP	EDP_DATA_EMI_P<3>	15
E454	EDP_90D	EDP	EDP_DATA_EMI_N<3>	15
E457	EDP_90D	EDP	CONN_EDP_AUX_EMI_P	15
E456	EDP_90D	EDP	CONN_EDP_AUX_EMI_N	15
E458	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<0>	15
E460	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<0>	15
E459	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<1>	15
E462	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<1>	15
E461	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<2>	15
E463	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<2>	15
E464	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<3>	15
E465	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<3>	15

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LEDA	*	*	3:1_SPACING
LEDB	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
J482	LED	LEDA	LED_IO1_A_R	30
J484	LED	LEDB	LED_IO1_B_R	30
J483	LED	LEDA	LED_IO2_A_R	30
J485	LED	LEDB	LED_IO2_B_R	30
J487	LED	LEDA	LED_IO3_A_R	30
J486	LED	LEDB	LED_IO3_B_R	30
J488	LED	LEDA	LED_IO4_A_R	30
J489	LED	LEDB	LED_IO4_B_R	30
J490	LED	LEDA	LED_IO5_A_R	30
J491	LED	LEDB	LED_IO5_B_R	30
J492	LED	LEDA	LED_IO6_A_R	30
J493	LED	LEDB	LED_IO6_B_R	30
J494	LED	LEDA	LED_IO_1_A	15 30
J495	LED	LEDB	LED_IO_1_B	15 30
J496	LED	LEDA	LED_IO_2_A	15 30
J497	LED	LEDB	LED_IO_2_B	15 30
J498	LED	LEDA	LED_IO_3_A	15 30
J499	LED	LEDB	LED_IO_3_B	15 30
J500	LED	LEDA	LED_IO_4_A	15 30
J501	LED	LEDB	LED_IO_4_B	15 30
J502	LED	LEDA	LED_IO_5_A	15 30
J503	LED	LEDB	LED_IO_5_B	15 30
J504	LED	LEDA	LED_IO_6_A	15 30
J505	LED	LEDB	LED_IO_6_B	15 30

TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
BOARD_TEMP	*	TEMP_SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BOARD_TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
J372		BOARD_TEMP	BOARD_TEMP1	30 32
J374		BOARD_TEMP	BOARD_TEMP2	30 32
J376	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_P	30
J377	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_N	30
J378	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_P	30
J379	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_N	30
J380	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_P	30
J381	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_N	30
J382	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_P	30
J383	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_N	30
E602	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_P	30
E603	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_N	30
E604	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_P	30
E605	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_N	30

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DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	DDR_45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DDR_90_OHM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I222	DDR_50S	DDR	DDR0_CA<9..0>	8 11
I222	DDR_50S	DDR	DDR0_DM<3..0>	8 11
I222	DDR_90D	DDR	DDR0_CK_P	8 11
I222	DDR_90D	DDR	DDR0_CK_N	8 11
I222	DDR_50S	DDR	DDR0_CKE<1..0>	8 11
I222	DDR_50S	DDR	DDR0_CSN<2..0>	8 11
I222	DDR_50S	DDR	DDR0_ZQ	11
I231	DDR_50S	DDR	DDR0_DQ<7..0>	8 11
I229	DDR_90D	DDR	DDR0_DQS_P<0>	8 11
I229	DDR_90D	DDR	DDR0_DQS_N<0>	8 11
I233	DDR_50S	DDR	DDR0_DQ<15..8>	8 11
I233	DDR_90D	DDR	DDR0_DQS_P<1>	8 11
I233	DDR_90D	DDR	DDR0_DQS_N<1>	8 11
I238	DDR_50S	DDR	DDR0_DQ<23..16>	8 11
I238	DDR_90D	DDR	DDR0_DQS_P<2>	8 11
I237	DDR_90D	DDR	DDR0_DQS_N<2>	8 11
I236	DDR_50S	DDR	DDR0_DQ<31..24>	8 11
I239	DDR_90D	DDR	DDR0_DQS_P<3>	8 11
I240	DDR_90D	DDR	DDR0_DQS_N<3>	8 11
I201	DDR_50S	DDR	DDR1_CA<9..0>	8 11
I207	DDR_50S	DDR	DDR1_DM<3..0>	8 11
I207	DDR_90D	DDR	DDR1_CK_P	8 11
I207	DDR_90D	DDR	DDR1_CK_N	8 11
I206	DDR_50S	DDR	DDR1_CKE<1..0>	8 11
I206	DDR_50S	DDR	DDR1_CSN<2..0>	8 11
I206	DDR_50S	DDR	DDR1_ZQ	11
I210	DDR_50S	DDR	DDR1_DQ<7..0>	8 11
I209	DDR_90D	DDR	DDR1_DQS_P<0>	8 11
I211	DDR_90D	DDR	DDR1_DQS_N<0>	8 11
I215	DDR_50S	DDR	DDR1_DQ<15..8>	8 11
I213	DDR_90D	DDR	DDR1_DQS_P<1>	8 11
I214	DDR_90D	DDR	DDR1_DQS_N<1>	8 11
I218	DDR_50S	DDR	DDR1_DQ<23..16>	8 11
I216	DDR_90D	DDR	DDR1_DQS_P<2>	8 11
I217	DDR_90D	DDR	DDR1_DQS_N<2>	8 11
I219	DDR_50S	DDR	DDR1_DQ<31..24>	8 11
I219	DDR_90D	DDR	DDR1_DQS_P<3>	8 11
I220	DDR_90D	DDR	DDR1_DQS_N<3>	8 11
I181	DDR_50S	DDR	DDR2_CA<9..0>	8 12
I187	DDR_50S	DDR	DDR2_DM<3..0>	8 12
I187	DDR_90D	DDR	DDR2_CK_P	8 12
I188	DDR_90D	DDR	DDR2_CK_N	8 12
I186	DDR_50S	DDR	DDR2_CKE<1..0>	8 12
I186	DDR_50S	DDR	DDR2_CSN<2..0>	8 12
I186	DDR_50S	DDR	DDR2_ZQ	12
I190	DDR_50S	DDR	DDR2_DQ<7..0>	8 12
I189	DDR_90D	DDR	DDR2_DQS_P<0>	8 12
I191	DDR_90D	DDR	DDR2_DQS_N<0>	8 12
I192	DDR_50S	DDR	DDR2_DQ<15..8>	8 12
I197	DDR_90D	DDR	DDR2_DQS_P<1>	8 12
I197	DDR_90D	DDR	DDR2_DQS_N<1>	8 12
I194	DDR_50S	DDR	DDR2_DQ<23..16>	8 12
I195	DDR_90D	DDR	DDR2_DQS_P<2>	8 12
I195	DDR_90D	DDR	DDR2_DQS_N<2>	8 12
I196	DDR_50S	DDR	DDR2_DQ<31..24>	8 12
I199	DDR_90D	DDR	DDR2_DQS_P<3>	8 12
I200	DDR_90D	DDR	DDR2_DQS_N<3>	8 12
I81	DDR_50S	DDR	DDR3_CA<9..0>	8 12
I92	DDR_50S	DDR	DDR3_DM<3..0>	8 12
I41	DDR_90D	DDR	DDR3_CK_P	8 12
I44	DDR_90D	DDR	DDR3_CK_N	8 12
I43	DDR_50S	DDR	DDR3_CKE<1..0>	8 12
I47	DDR_50S	DDR	DDR3_CSN<2..0>	8 12
I48	DDR_50S	DDR	DDR3_ZQ	12
I37	DDR_50S	DDR	DDR3_DQ<7..0>	8 12
I179	DDR_90D	DDR	DDR3_DQS_P<0>	8 12
I177	DDR_90D	DDR	DDR3_DQS_N<0>	8 12
I175	DDR_50S	DDR	DDR3_DQ<15..8>	8 12
I173	DDR_90D	DDR	DDR3_DQS_P<1>	8 12
I174	DDR_90D	DDR	DDR3_DQS_N<1>	8 12
I172	DDR_50S	DDR	DDR3_DQ<23..16>	8 12
I170	DDR_90D	DDR	DDR3_DQS_P<2>	8 12
I171	DDR_90D	DDR	DDR3_DQS_N<2>	8 12
I169	DDR_50S	DDR	DDR3_DQ<31..24>	8 12
I167	DDR_90D	DDR	DDR3_DQS_P<3>	8 12
I168	DDR_90D	DDR	DDR3_DQS_N<3>	8 12

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND0	*	*	2:1_SPACING
NAND1	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I68	NAND_50S	NAND0	FMI0_AD<0>	6 13
I69	NAND_50S	NAND0	FMI0_AD<1>	6 13
I70	NAND_50S	NAND0	FMI0_AD<2>	6 13
I71	NAND_50S	NAND0	FMI0_AD<3>	6 13
I72	NAND_50S	NAND0	FMI0_AD<4>	6 13
I73	NAND_50S	NAND0	FMI0_AD<5>	6 13
I74	NAND_50S	NAND0	FMI0_AD<6>	6 13
I75	NAND_50S	NAND0	FMI0_AD<7>	6 13
I76	NAND_50S	NAND0	FMI0_ALE	6 13
I77	NAND_50S	NAND0	FMI0_CE0_L	6 13
I78	NAND_50S	NAND0	TP_FMI0_CE1_L	
I120	NAND_50S	NAND0	TP_FMI0_CE2_L	
I121	NAND_50S	NAND0	TP_FMI0_CE3_L	
I122	NAND_50S	NAND0	TP_FMI0_CE4_L	
I123	NAND_50S	NAND0	TP_FMI0_CE5_L	
I124	NAND_50S	NAND0	TP_FMI0_CE6_L	
I125	NAND_50S	NAND0	TP_FMI0_CE7_L	
I126	NAND_50S	NAND0	FMI0_CLE	6 13
I128	NAND_50S	NAND0	FMI0_DQS	6 13
I131	NAND_50S	NAND0	FMI0_RE_L	6 13
I132	NAND_50S	NAND0	FMI0_WE_L	6 13
I133	NAND_50S	NAND1	FMI1_AD<0>	6 13
I134	NAND_50S	NAND1	FMI1_AD<1>	6 13
I135	NAND_50S	NAND1	FMI1_AD<2>	6 13
I136	NAND_50S	NAND1	FMI1_AD<3>	6 13
I139	NAND_50S	NAND1	FMI1_AD<4>	6 13
I140	NAND_50S	NAND1	FMI1_AD<5>	6 13
I141	NAND_50S	NAND1	FMI1_AD<6>	6 13
I142	NAND_50S	NAND1	FMI1_AD<7>	6 13
I143	NAND_50S	NAND1	FMI1_ALE	6 13
I144	NAND_50S	NAND1	FMI1_CE0_L	6 13
I146	NAND_50S	NAND1	TP_FMI1_CE2_L	
I148	NAND_50S	NAND1	TP_FMI1_CE4_L	
I149	NAND_50S	NAND1	TP_FMI1_CE5_L	
I150	NAND_50S	NAND1	TP_FMI1_CE6_L	
I151	NAND_50S	NAND1	TP_FMI1_CE7_L	
I152	NAND_50S	NAND1	FMI1_CLE	6 13
I154	NAND_50S	NAND1	FMI1_DQS	6 13
I159	NAND_50S	NAND1	FMI1_RE_L	6 13
I160	NAND_50S	NAND1	FMI1_WE_L	6 13

WIFI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
WIFI_50S	*	WIFI_50S
WIFI_PWR100	*	WIFI_PWR100
WIFI_PWR1000	*	WIFI_PWR1000

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I240	WIFI_50S		50_WLAN_G	27
I240	WIFI_50S		50_WLAN_A	27
I240	WIFI_50S		50_WLAN_G_1	27
I240	WIFI_50S		50_WLAN_A_DIPLX	27
I240	WIFI_50S		50_WIFI_ANT_FD_2	
I250	WIFI_50S		50_WIFI_ANT_FD_1	
I251	WIFI_50S		50_WIFI_ANT_FD	

DDR VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I100		PWR	PPVREF_DDR0_CA	11 39
I100		PWR	PPVREF_DDR0_DQ	11 39
I100		PWR	PPVREF_DDR1_CA	11 39
I100		PWR	PPVREF_DDR1_DQ	11 39
I244		PWR	PPVREF_DDR2_CA	12 39
I244		PWR	PPVREF_DDR2_DQ	12 39
I243		PWR	PPVREF_DDR3_CA	12 39
I243		PWR	PPVREF_DDR3_DQ	12 39

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PWR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PP_PWR	*	PWR_PMU

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PWR	*	*	3:1_SPACING

	VOLTAGE	NET_TYPE PHYSICAL	SPACING		
P22	1.1V	PP_PWR	PWR	BUCK0A_LX0	29
P6	1.1V	PP_PWR	PWR	BUCK0A_LX1	29
P7	1.1V	PP_PWR	PWR	BUCK0A_FB	29
P8	1.1V	PP_PWR	PWR	PP1V1_CPU0_FET	29 30
P9	1.1V	PP_PWR	PWR	BUCK0B_LX0	29
P10	1.1V	PP_PWR	PWR	BUCK0B_LX1	29
P11	1.1V	PP_PWR	PWR	BUCK0B_FB	29
P12	1.1V	PP_PWR	PWR	PP1V1_CPU1_FET	29 30
P4	1.1V	PP_PWR	PWR	BUCK0C_LX0	29
P5	1.1V	PP_PWR	PWR	BUCK0C_FB	29
P6	1.1V	PP_PWR	PWR	PP1V1_CPUB	29 34
P13	1.2V	PP_PWR	PWR	BUCK2_LX0	29
P14	1.2V	PP_PWR	PWR	BUCK2_LX1	29
P15	1.2V	PP_PWR	PWR	BUCK2_LX2	29
P16	1.2V	PP_PWR	PWR	BUCK2_FB	29
P17	1.2V	PP_PWR	PWR	PP1V2_SOC	29 34
P18	1.8V	PP_PWR	PWR	BUCK3_LX0	29
P19	1.8V	PP_PWR	PWR	BUCK3_FB	29
P20	1.8V	PP_PWR	PWR	PP1V8_S2R	29 34
P21	1.2V	PP_PWR	PWR	BUCK4_LX0	29
P23	1.2V	PP_PWR	PWR	BUCK4_FB	29
P24	1.2V	PP_PWR	PWR	PP1V2_S2R	29 34
P25	1.1V	PP_PWR	PWR	BUCK5_LX0	29
P26	1.1V	PP_PWR	PWR	BUCK5_FB	29
P27	3.3V	PP_PWR	PWR	PP3V3_OUT	29 34
P28	3.0V	PP_PWR	PWR	PP3V0_GRAPE	29 34
P29	1.7V	PP_PWR	PWR	PP1V7_VA_VCP	19 29 34
P30	3.0V	PP_PWR	PWR	PP3V2_S2R_USBMUX	29 34 39
P31	3.2V	PP_PWR	PWR	LDO5	29
P32	3.3V	PP_PWR	PWR	PP3V3_ACC	29 34
P33	3.0V	PP_PWR	PWR	PP3V0_S2R_HALL	29 34
P34	3.0V	PP_PWR	PWR	PP3V2_S2R_USBMUX	29 34 39
P35	3.0V	PP_PWR	PWR	PP3V0_IO	29 34
P36	3.0V	PP_PWR	PWR	PP3V0_SENSOR	29 34
P37	2.8V	PP_PWR	PWR	PP2V8_CAM	29 34
P38	1.0V	PP_PWR	PWR	PP1V0	29 34
P39	1.1V	PP_PWR	PWR	PP1V1_SRAM	29 34
P40	1.8V	PP_PWR	PWR	PP1V8_ALWAYS	29 34
P41	1.2V	PP_PWR	PWR	PP1V2	29 34
P42		PP_PWR	PWR	DSP_SW	
P43	1.8V	PP_PWR	PWR	PP1V8	29 32 34
P44	1.8V	PP_PWR	PWR	PP1V8_GRAPE	
P45	4.7V	PP_PWR	PWR	PPVCC_MAIN	15 25 29 30 34
P46	4.2V	PWR500	PWR	PPBATT_VCC	29 32 34
P47	6.0V	PP_PWR	PWR	PP6V0_LCM_HI	30
P48	6.0V	PP_PWR	PWR	LCM_LX	30
P49	6.0V	PP_PWR	PWR	PP6V0_LCM_VBOOST	30
P50	5.25V	PP_PWR	PWR	PP5V25_VLCM1	
P51	1.1V	PP_PWR	PWR	PP1V1_CPU0	30 34
P52	1.1V	PP_PWR	PWR	PP1V1_CPU1	30 34
P53	20.4V	PP_PWR	PWR	PPLED_OUT_A	30 34
P54	20.4V	PP_PWR	PWR	PPLED_OUT_B	30 34
P55	1.8V	PP_PWR	PWR	PP1V8_PL0_F	4
P56	1.0V	PP_PWR	PWR	PP1V0_MIPI_PLL_F	7
P57	1.8V	PP_PWR	PWR	PP1V8_EDP_AVDD_AUX	7
P58	1.8V	PP_PWR	PWR	PP1V8_DP_AVDD_AUX	
P59	3.3V	PP_PWR	PWR	PP3V3_S0_LCD_FERR	15
P60	3.3V	PP_PWR	PWR	PP3V3_LCDVDD_SW_F	15
P61	20.4V	PWR500	PWR	PPLED_BACK_REG_B	15
P62	20.4V	PP_PWR	PWR	PPLED_BACK_REG_A	15
P63	6V	PP_PWR	PWR	PPVBUS_USB_EMI	23 34
P64	0.6V	PP_PWR	PWR	PPVREF_DDR0_CA	11 38
P65	0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ	11 38
P66	0.6V	PP_PWR	PWR	PPVREF_DDR1_CA	11 38
P67	0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ	11 38
P68	0.6V	PP_PWR	PWR	PPVREF_DDR2_CA	12 38
P69	0.6V	PP_PWR	PWR	PPVREF_DDR2_DQ	12 38
P70	0.6V	PP_PWR	PWR	PPVREF_DDR3_CA	12 38
P71	0.6V	PP_PWR	PWR	PPVREF_DDR3_DQ	12 38
P72		PP_PWR	PWR	DAC_AP_VREF	7
P73	4.6V	PP_PWR	PWR	BATT_POS_RC	29
P224	4.6V	PP_PWR	PWR	BATT_VCC_WLAN	27
P225	1.8V	PP_PWR	PWR	PP_WLAN_VDDIO_1V8	27
P227	3.55V	PP_PWR	PWR	LDO10	18 29

GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_PH

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
P199	VOLTAGE=0V	GND	GND	GND	
P198	VOLTAGE=0V	GND	GND	GND_AUDIO_CODEC	18
P197	VOLTAGE=0V	GND	GND	GND_SPKR_AMP1	
P196	VOLTAGE=0V	GND	GND	GND_SPKR_AMP2	
P17	VOLTAGE=0V	GND	GND	AGND_U3000	16
P224	VOLTAGE=0V	GND	GND	J2200_29_GND	15
P222	VOLTAGE=0V	GND	GND	J2200_36_GND	15
P220	VOLTAGE=0V	GND	GND	J2200_43_GND	15

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	4:1_SPACING

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
P145			RST	BB_TRST_L	
P146			RST	DBG_RST	
P147			RST	DEBUG_RST_L	
P171			RST	GSM_TXBURST_IND	
P148			RST	JTAG_AP_TRST_L	4 10 36
P139			RST	RST_AP_1V8_L	
P168			RST	RST_AP_L	4 25 26 30
P132			RST	GPIO_BB_RST_L	5 26
P134			RST	RST_BB_PMU_L	
P133			RST	RST_BT_L	
P135			RST	RST_DET_L	
P136			GRAPE	RST_GRAPE_L	
P137			RST	RST_L63_L	
P138			RST	RST_PMU_IN	
P169			RST	RST_WLAN_L	
P141			RST	SIMCRD_RST	
P142			RST	UD881_RST	
P143			RST	UD882_RST	

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