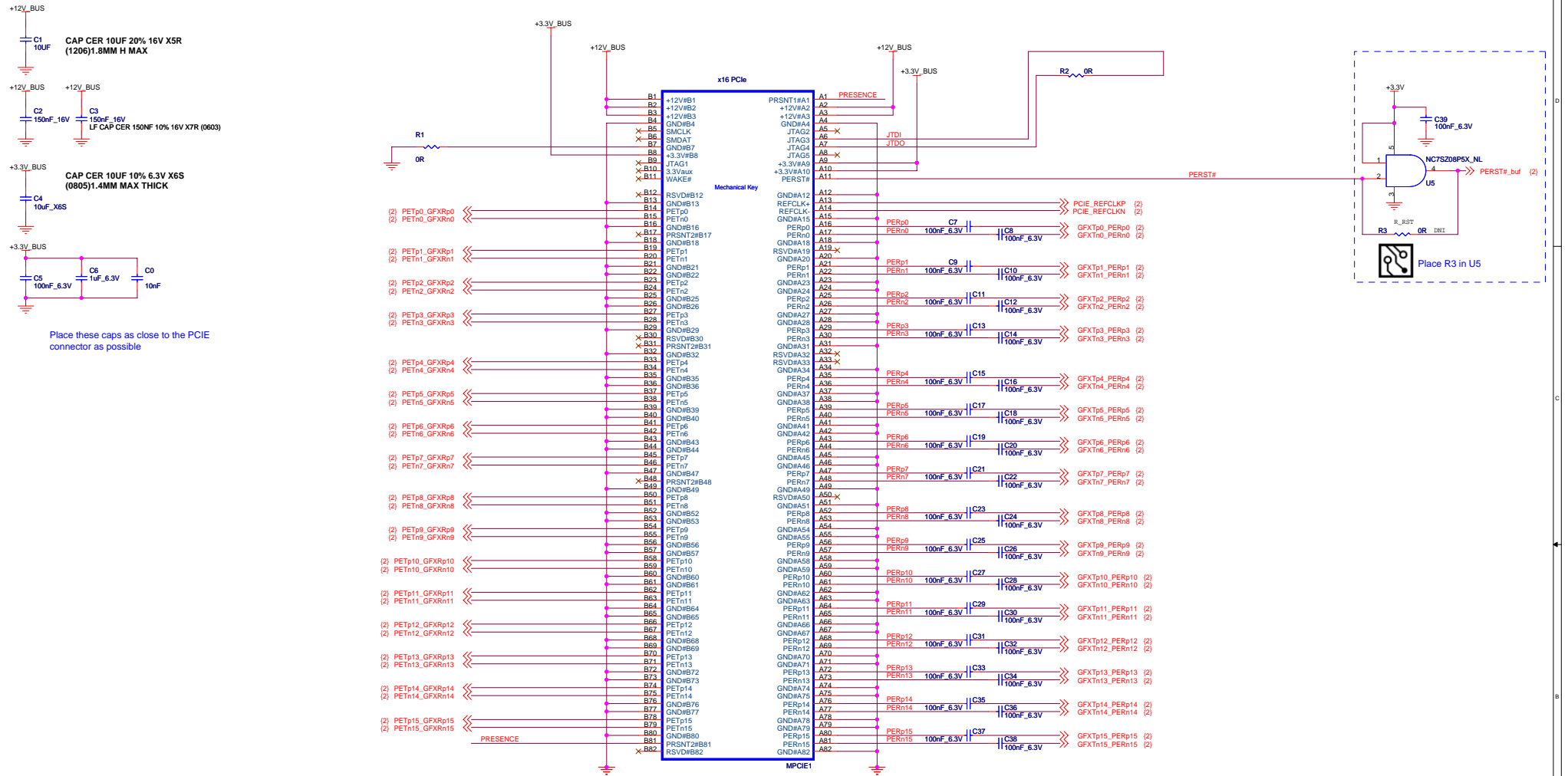
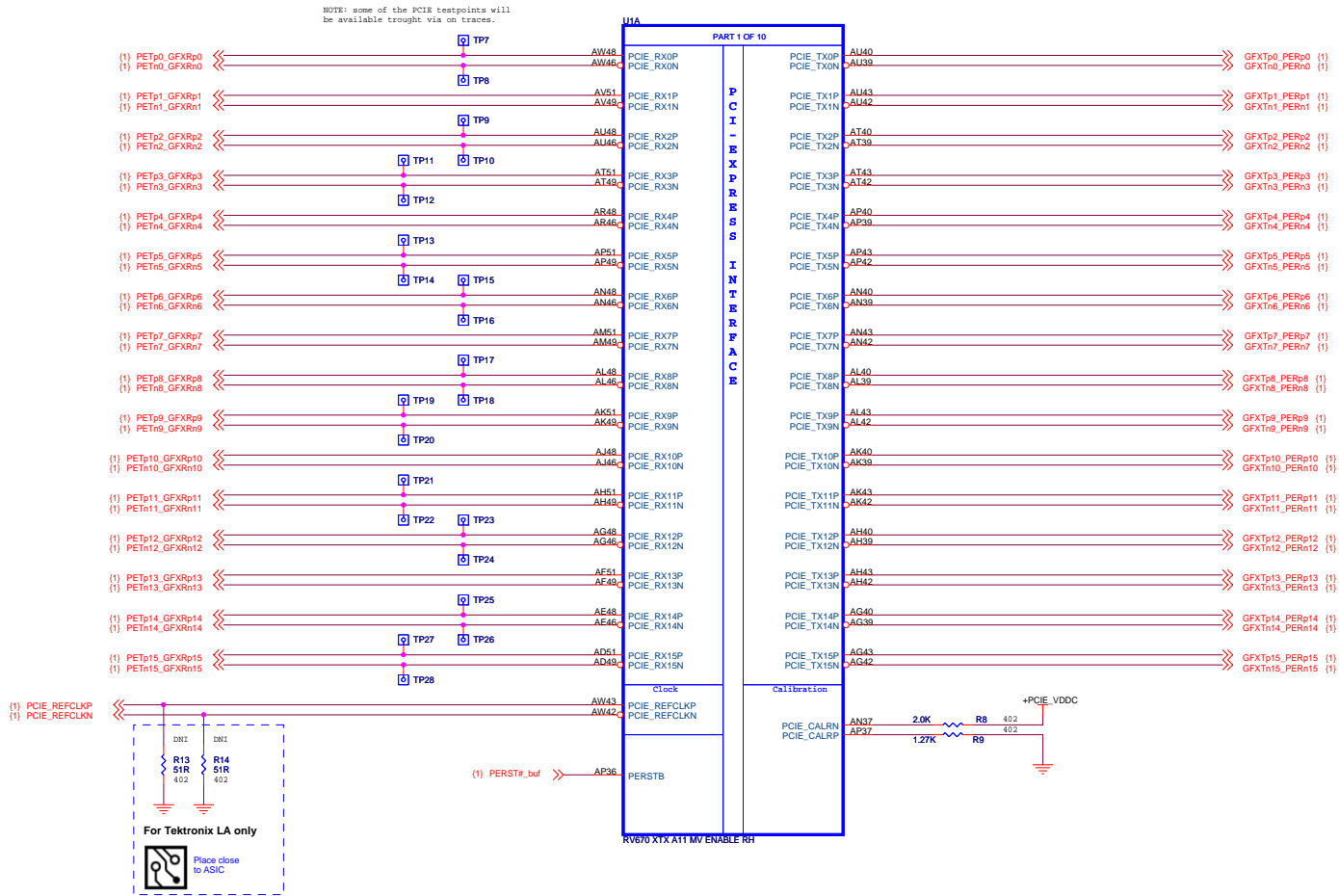


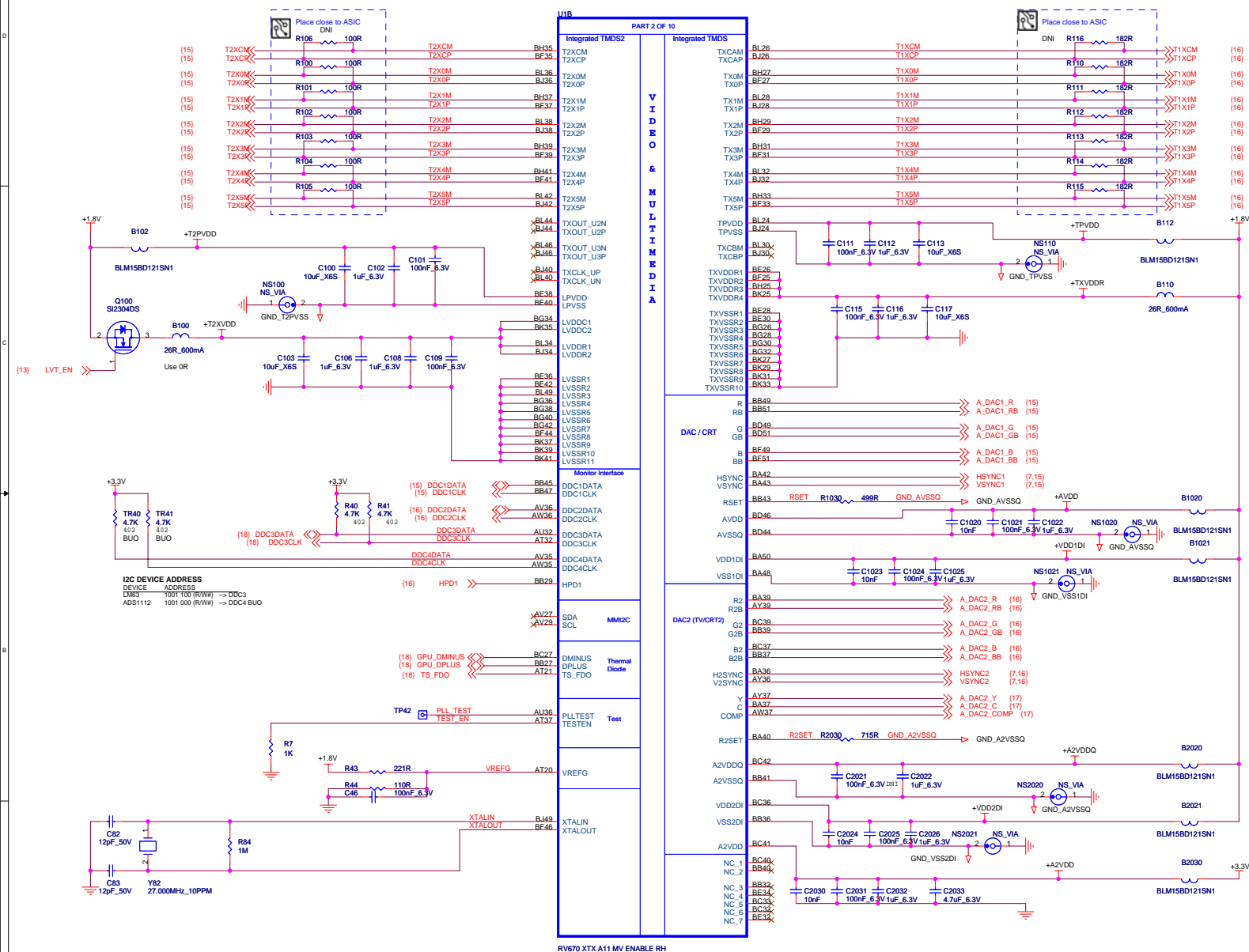
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BLU	BRING UP ONLY



Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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Title RH RV670 - ASIC MAIN

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0,	1 Commerce Valley Drive East
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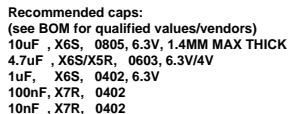
Date: Tuesday, February 19, 20

Sheet 3 of 21

Rev .

[illegible]

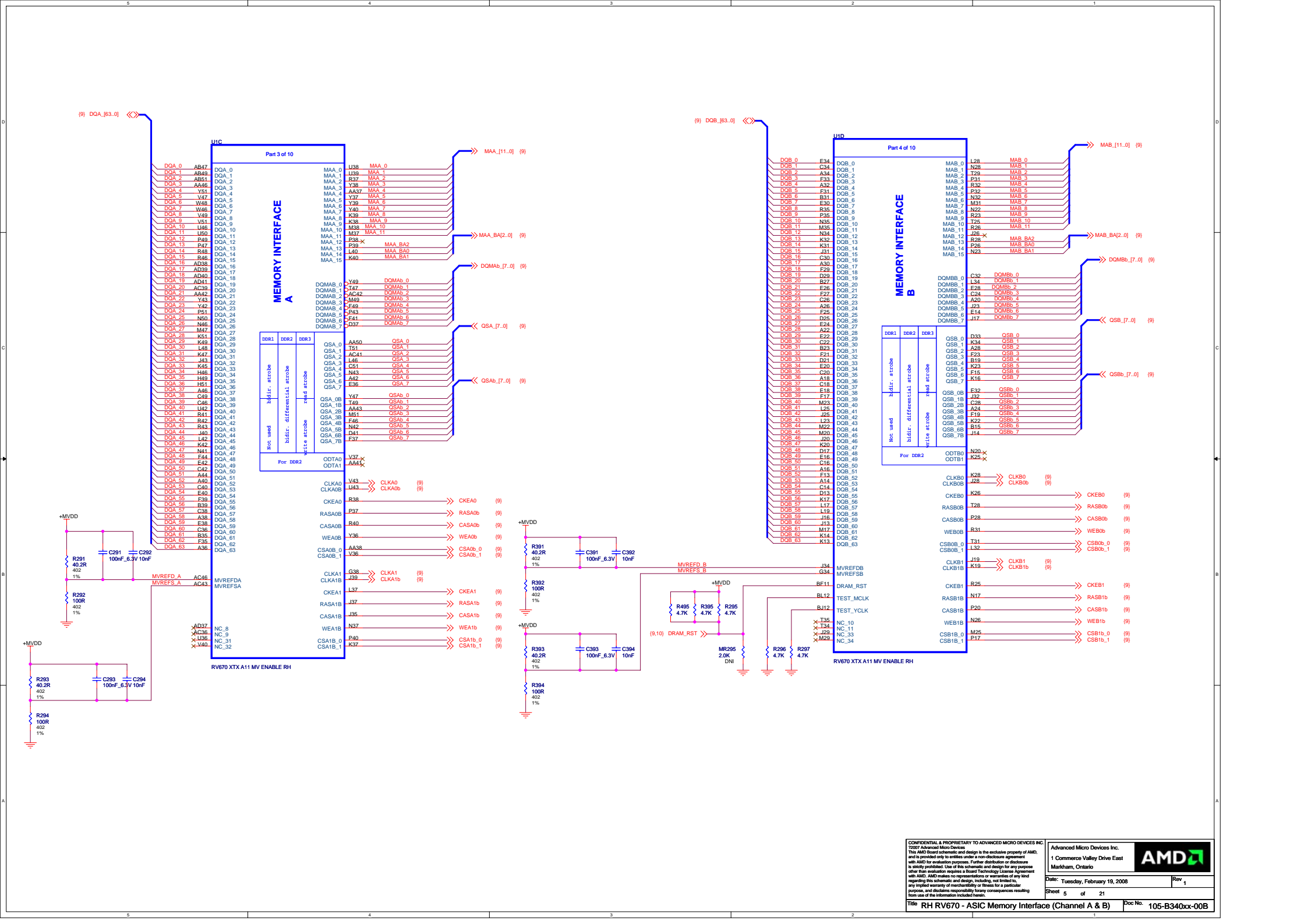
Doc No.	105-B340xx-00B
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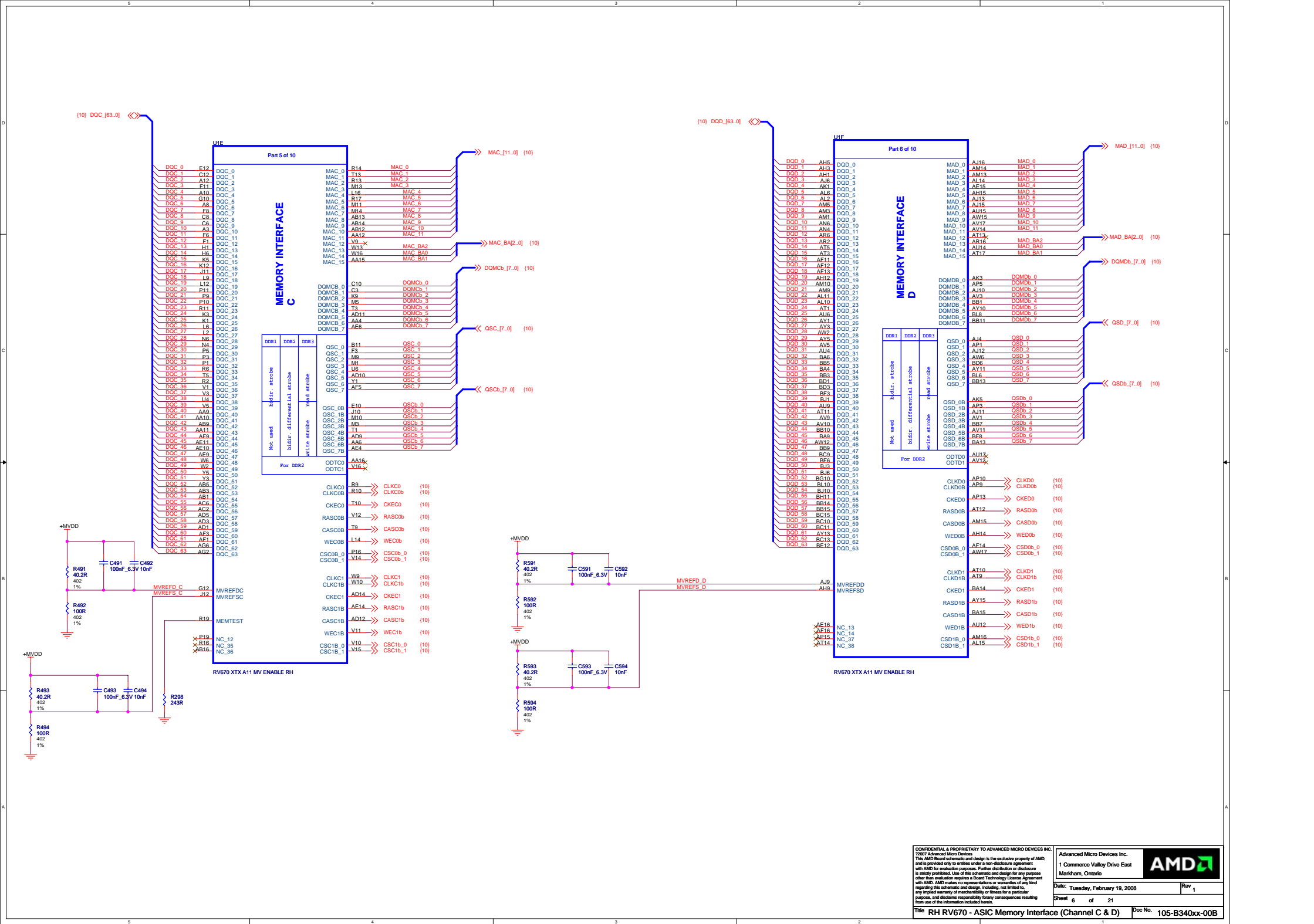


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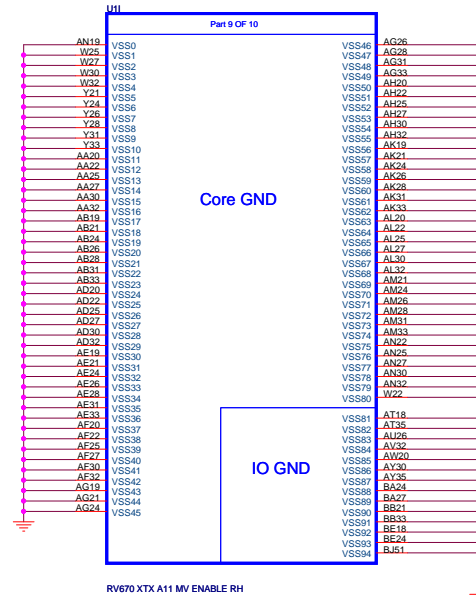
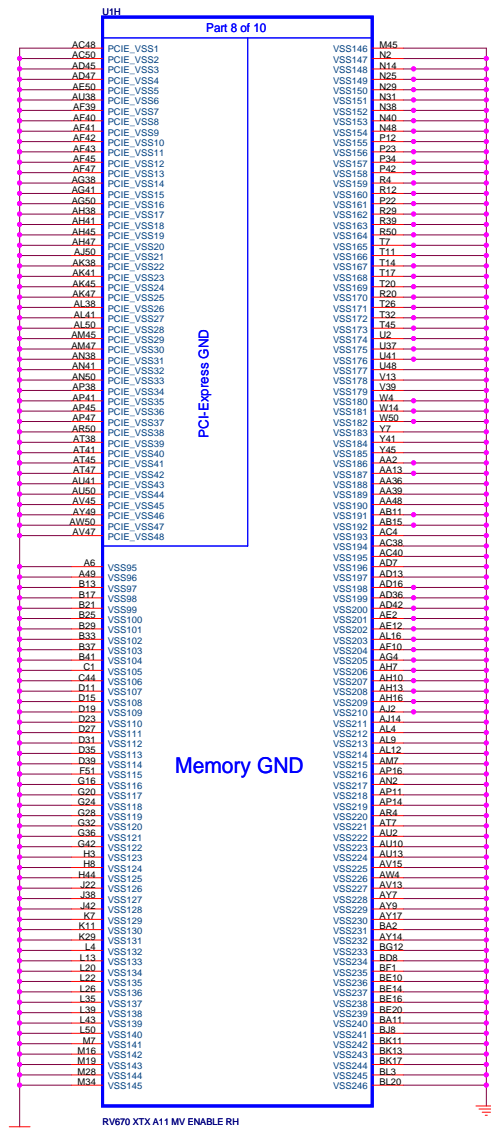
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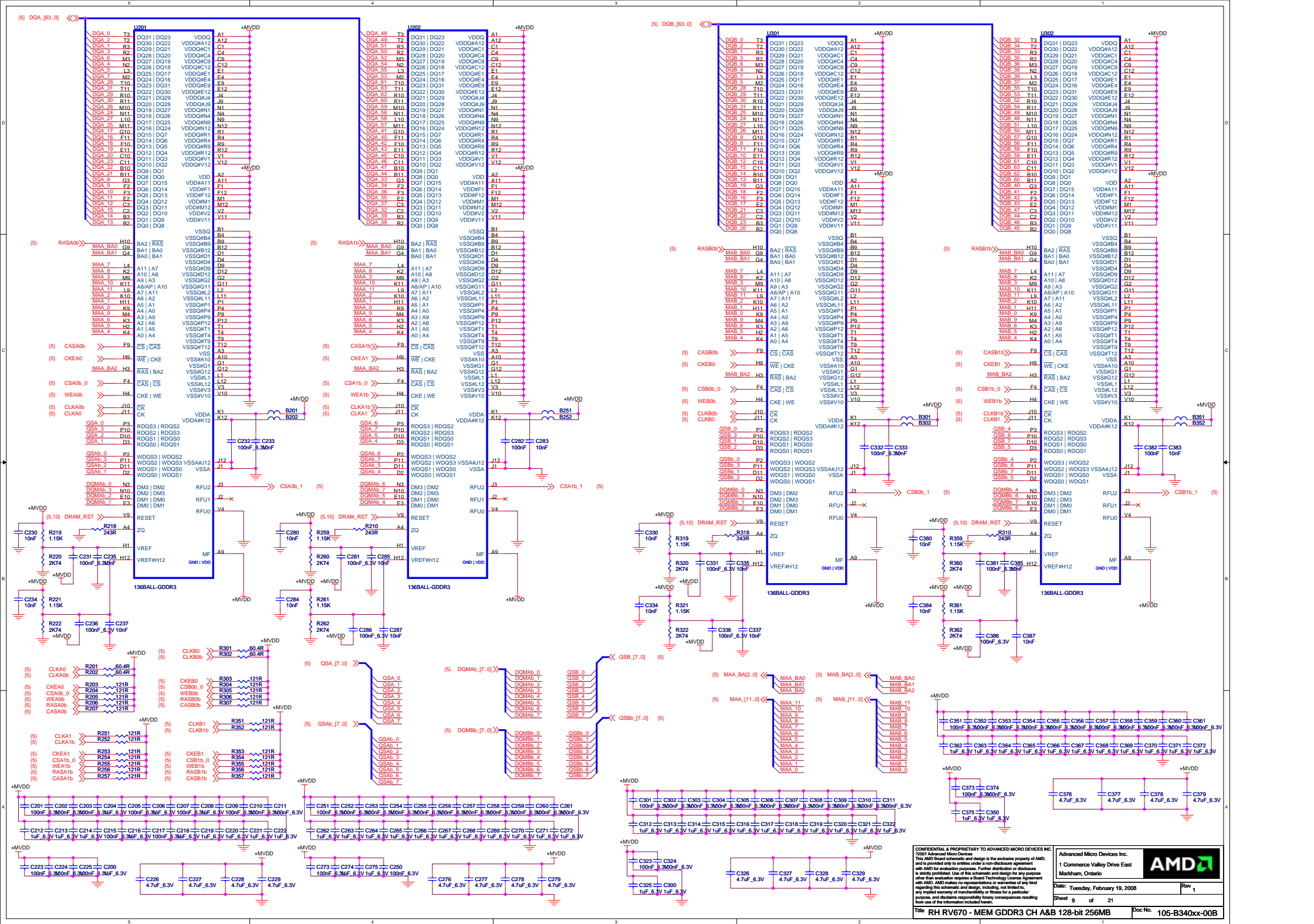
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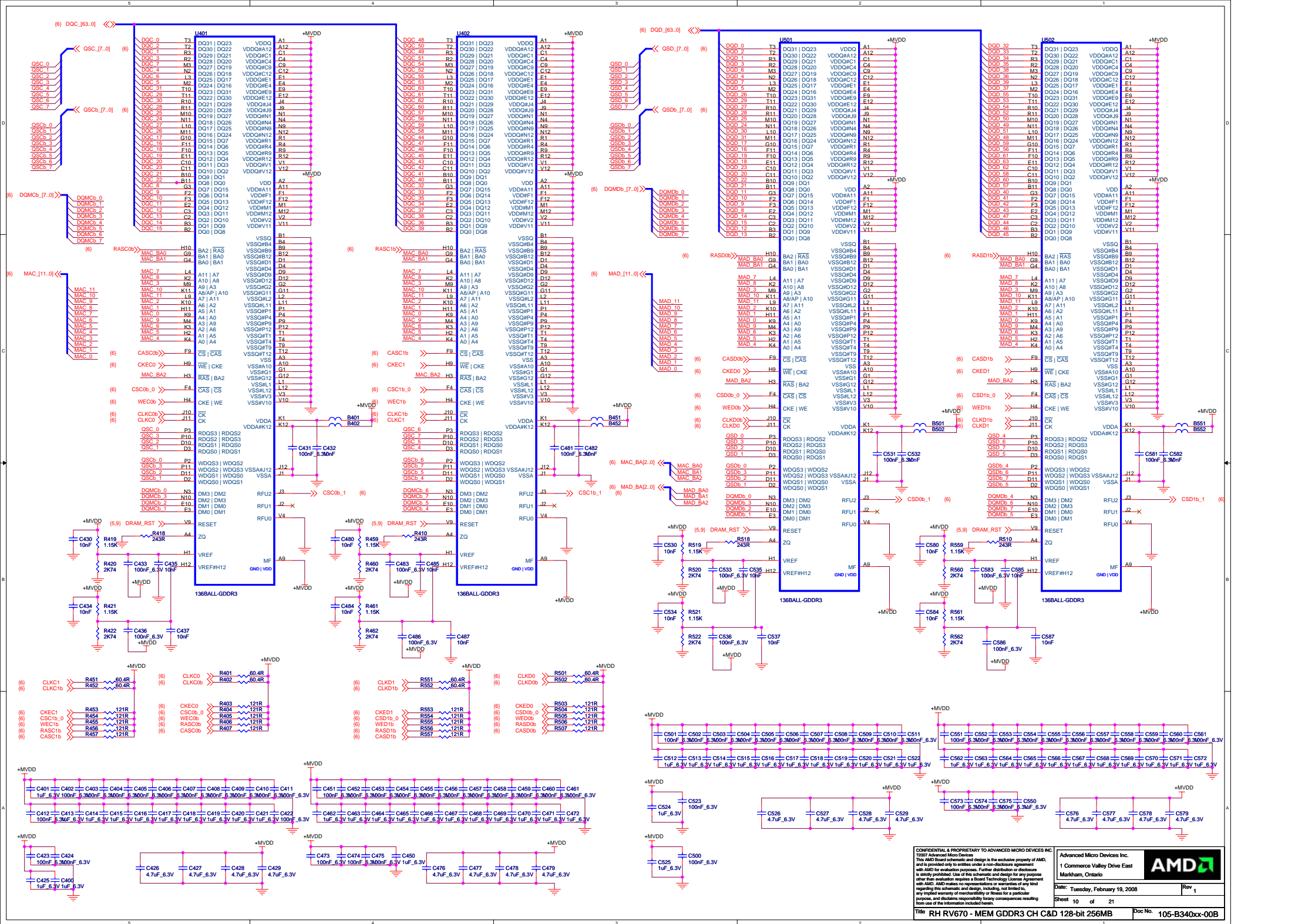




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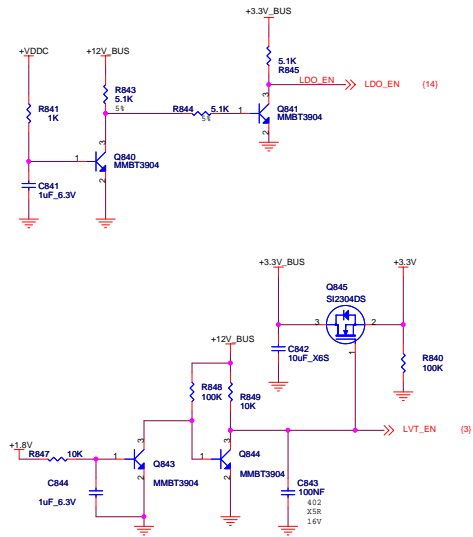


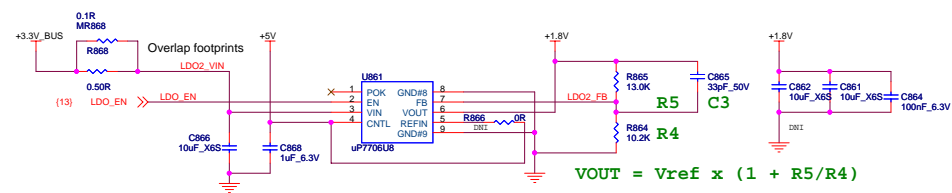
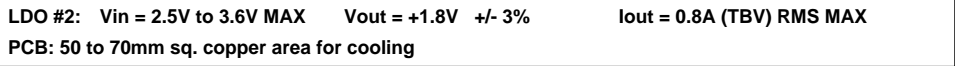




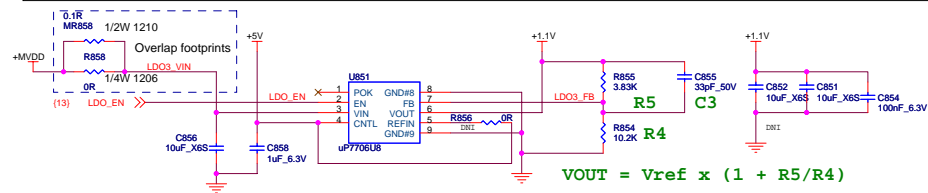


Power up Sequencing



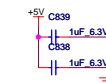
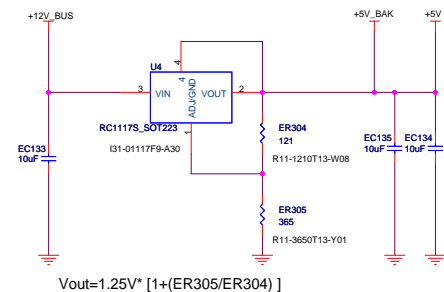
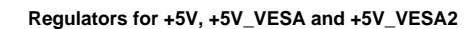
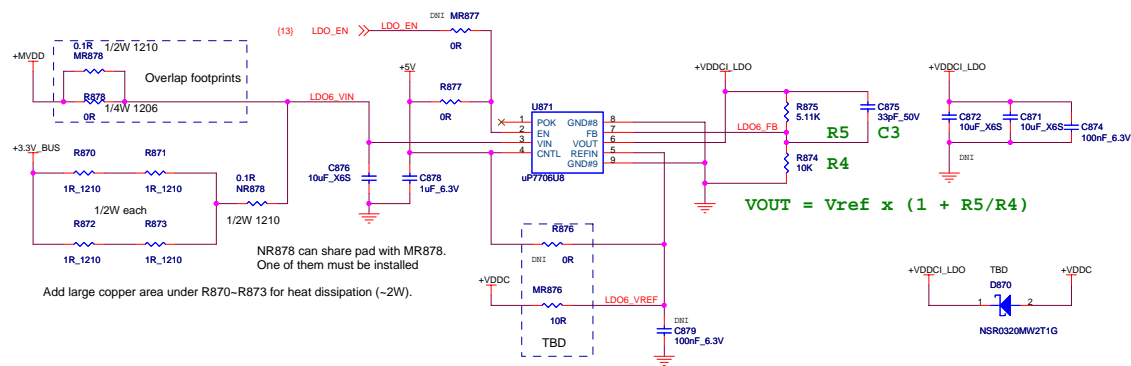



LDO #3: Vin = +1.70V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

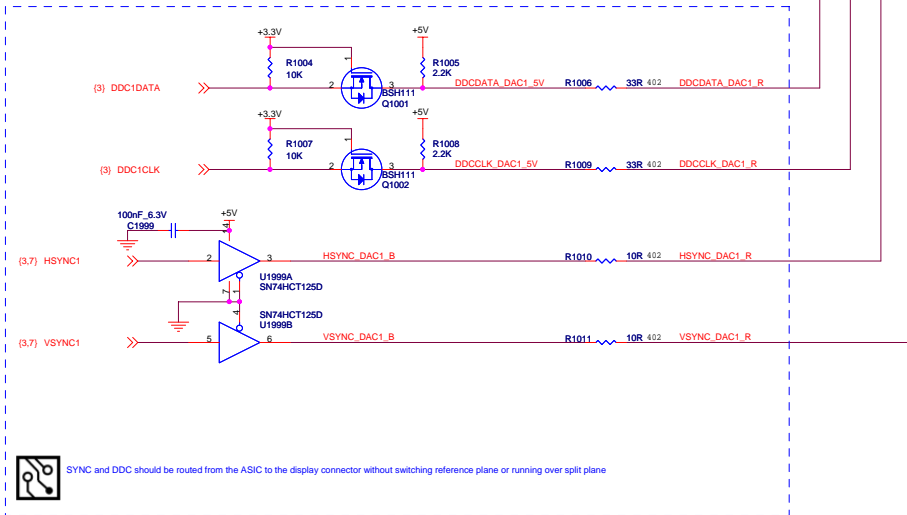
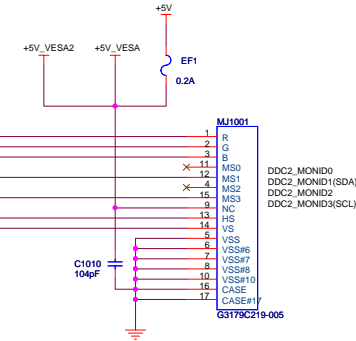
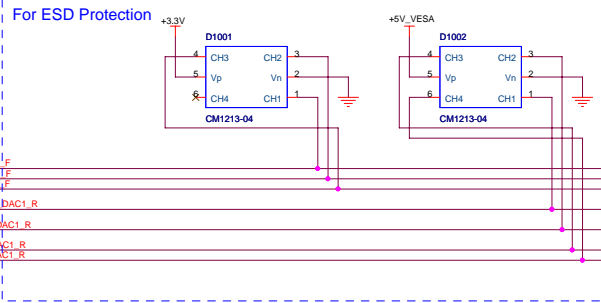
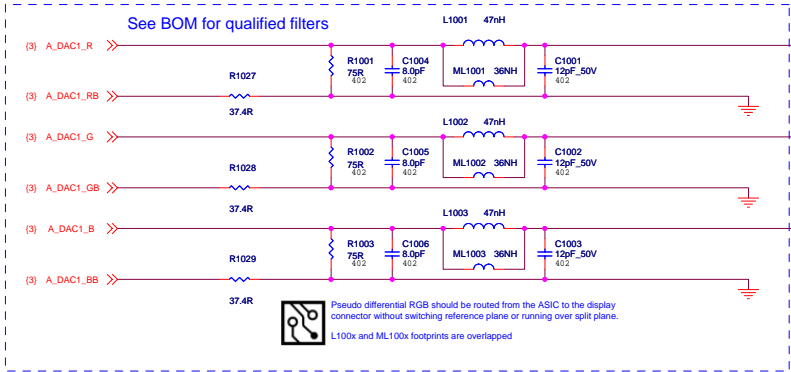


LDO #6: For fixed output voltage: $V_{in} = +1.70V$ to $2.1V$ MAX $V_{out} = +1.20V \pm 3\%$ $I_{out} = 1.3A$ (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

LDO #6: For tracking VDDC: $V_{in} = TBD$ $V_{out} = TBD$ $I_{out} = 1.3A$ (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

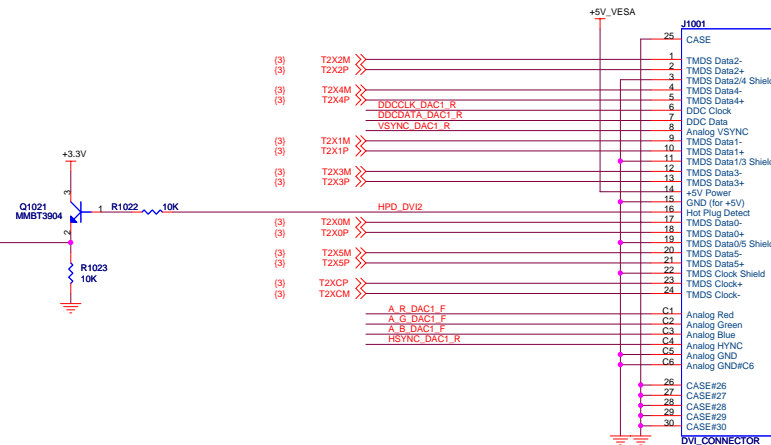


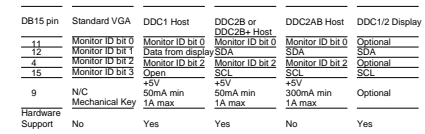
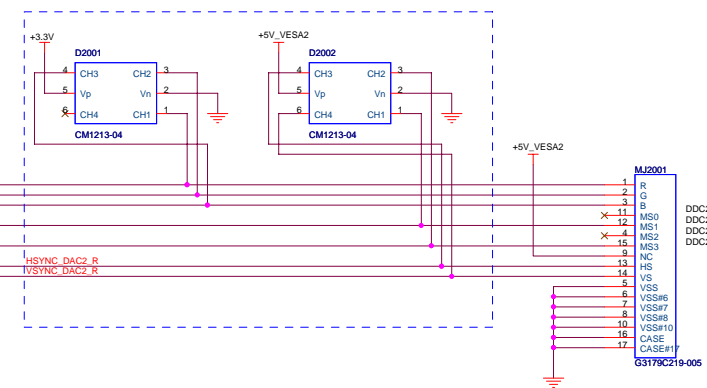
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<p>Title RH RV670 - Linear Regulators</p>	<p>Doc No. 105-B340xx-00B</p>



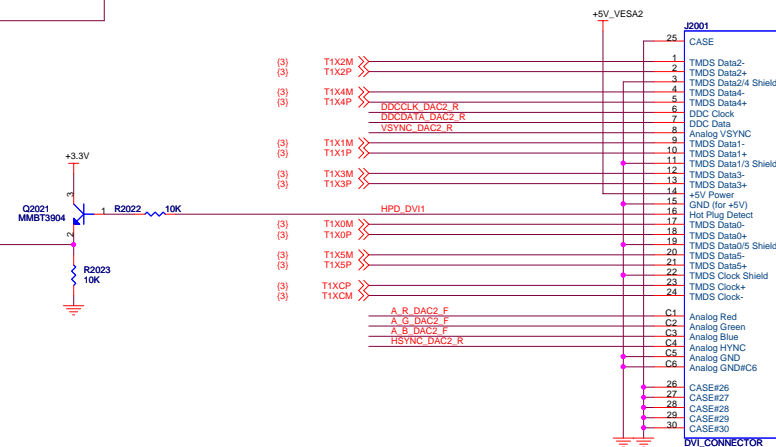
DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional SDA
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional SCL
15	Monitor ID bit 3	Open	Open	Open	Optional SCL
9	N/C	+5V	+5V	+5V	Optional
Support	No	Yes	Yes	No	Yes

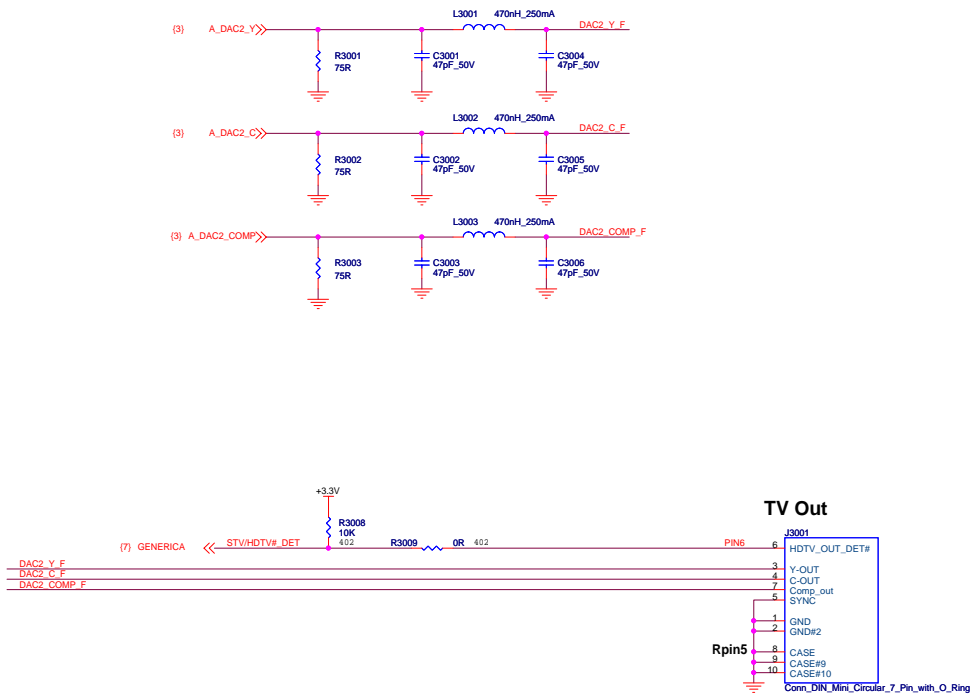
Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





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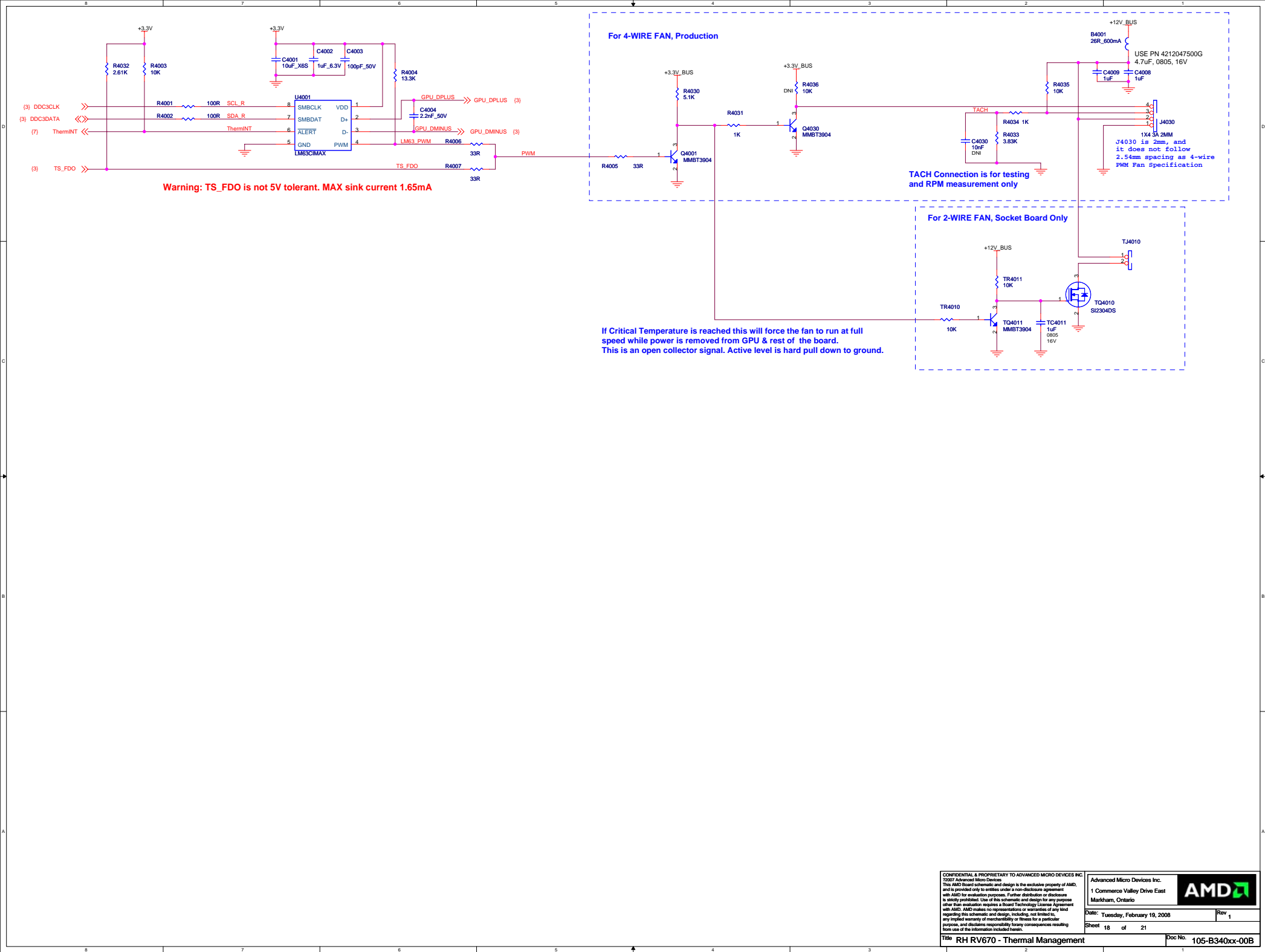
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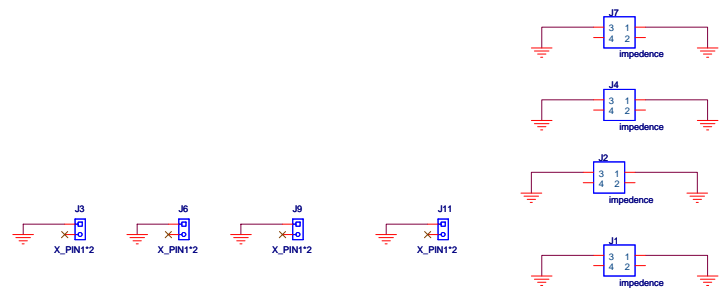
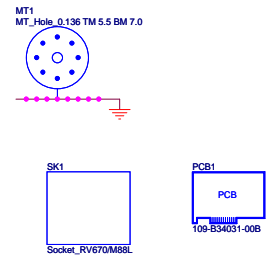
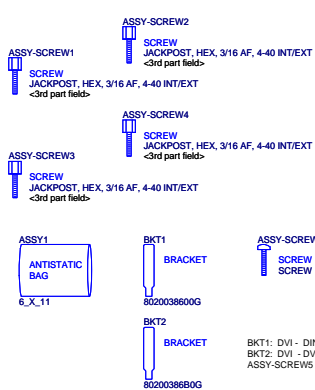
Rev 1

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Title RH RV670 - TV OUT

Doc No. 105-B340xx-00B







Title	RH PCIE RV670 512MB GDDR3 DUAL DL-DVI-I VO FH
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Schematic No.
105-B340xx-00B

Date:
Tuesday, February 19, 2008

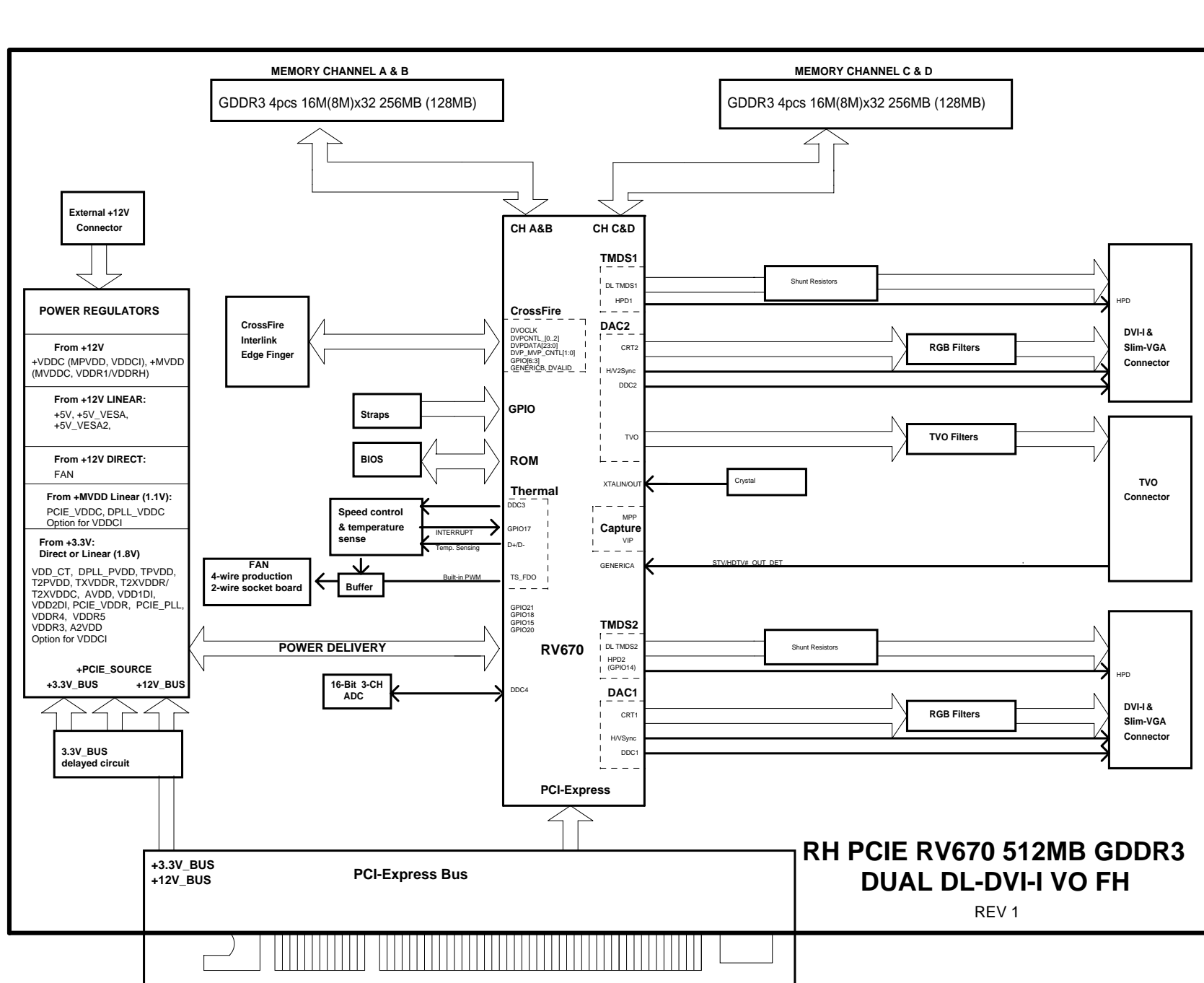
REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
 For Stuffing options (component values, DNI , ? please consult the product specific BOM.
 Please contact AMD representative to obtain latest BOM closest to the application desired.

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1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/05/11	Initial design for RV670 GDDR3 (Revival) based on B339
1	00B	07/08/1	(pg 1) Adding R1 and connecting switch #7 of TSW1. Some mother boards require B7 to be grounded. Table-1 updated accordingly (pg 7) Adding R64 and MR64 to select HOT_PLUG_DET or ThermlNT as the interrupt source. (pg 13) Adding R1617, MR1617, R1616, Q1613, R1615, R1618, and R1619 as option to support hot plug detection of external cable. (pg 13) Adding R1282, MR1282, R1283, MR1283, R1284, MR1284, R1281, R1285, Q1280, and C1280 as option for thermal protection for VDDC SMPS MOSFETs (pg 13) Adding MC1603 (overlapped with C1603) (pg 14) Adding D870 as option for power up sequencing (pg 18) Adding heatsink symbol/footprint (Layout) Increasing spacing between DDC4DATA & DDC4CLK going to U1270 to reduce the crosstalk



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Date: Tuesday, February 26, 2008

Rev 1

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Title: RH PCIE RV670 512MB GDDR3 DUAL DL-DVI-I VO FH Doc No. 105-B340xx-00B