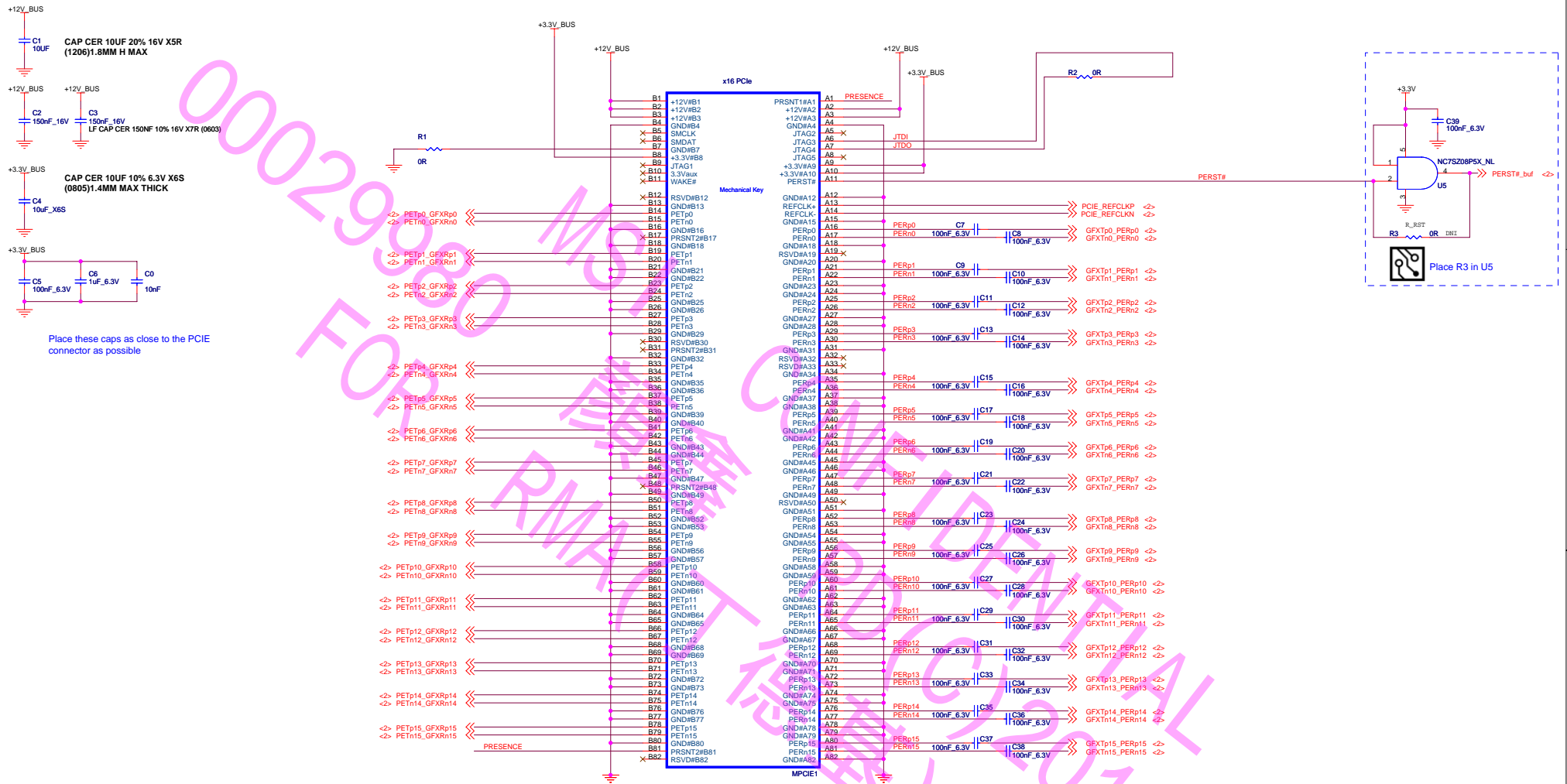


# PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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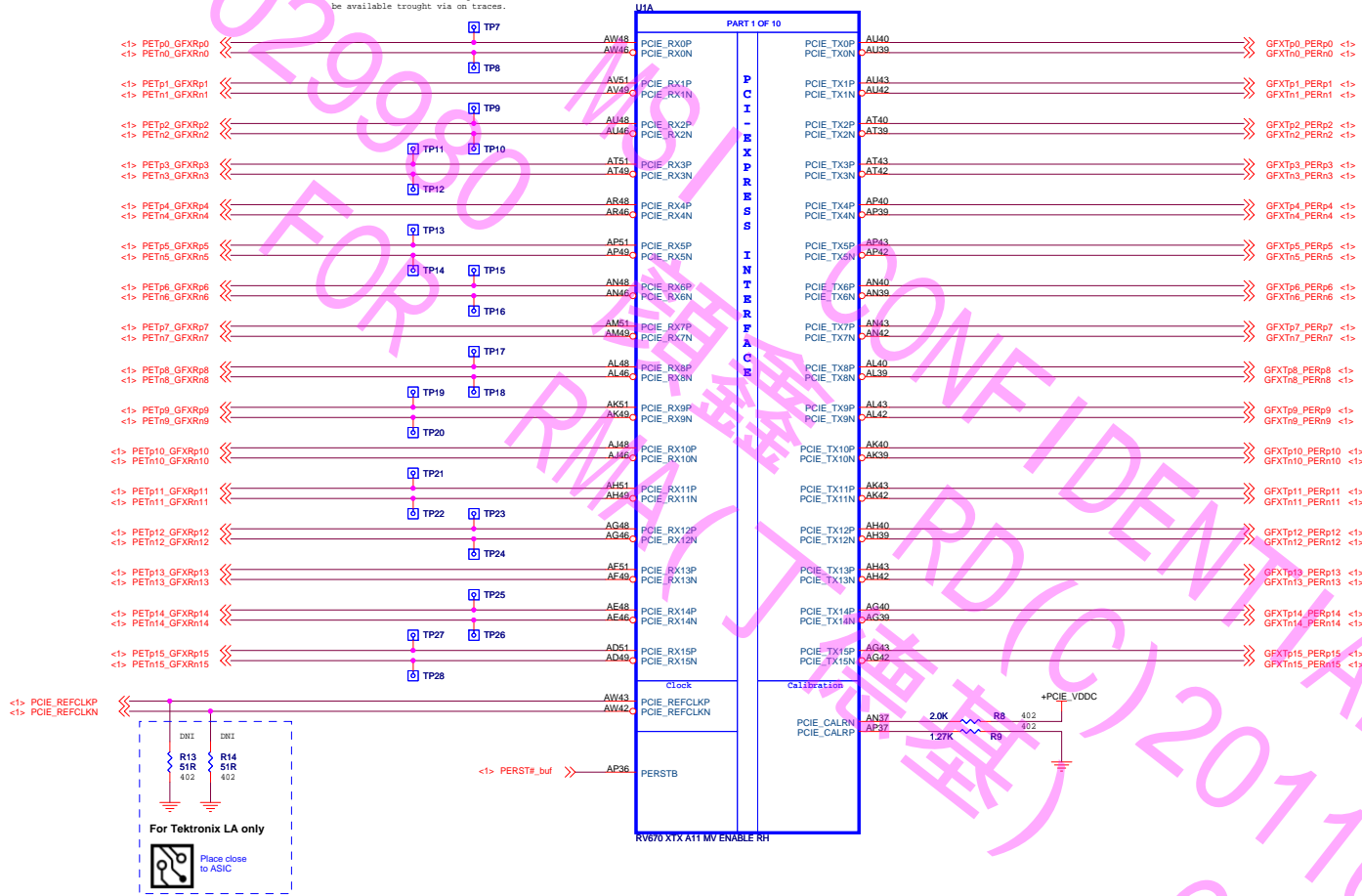
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 Markham, Ontario  
 Date: Wednesday, March 10, 2008  
 Sheet 1 of 23  
 Rev 1

00029980 (C) 20110816001

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ONLY

NOTE: some of the PCIe testpoints will be available through via on traces.



**Recommended caps:**  
 (see BOM for qualified values/vendors)  
 10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK  
 4.7uF , X6S/X5R, 0603, 6.3V/4V  
 1uF , X6S, 0402, 6.3V  
 100nF, X7R, 0402  
 10nF , X7R, 0402

**Place close to ASIC**  
 DNI

**Place close to ASIC**  
 DNI

**VIDEO & MULTIMEDIA**

**I2C DEVICE ADDRESS**

**Thermal Diode**


**Test**

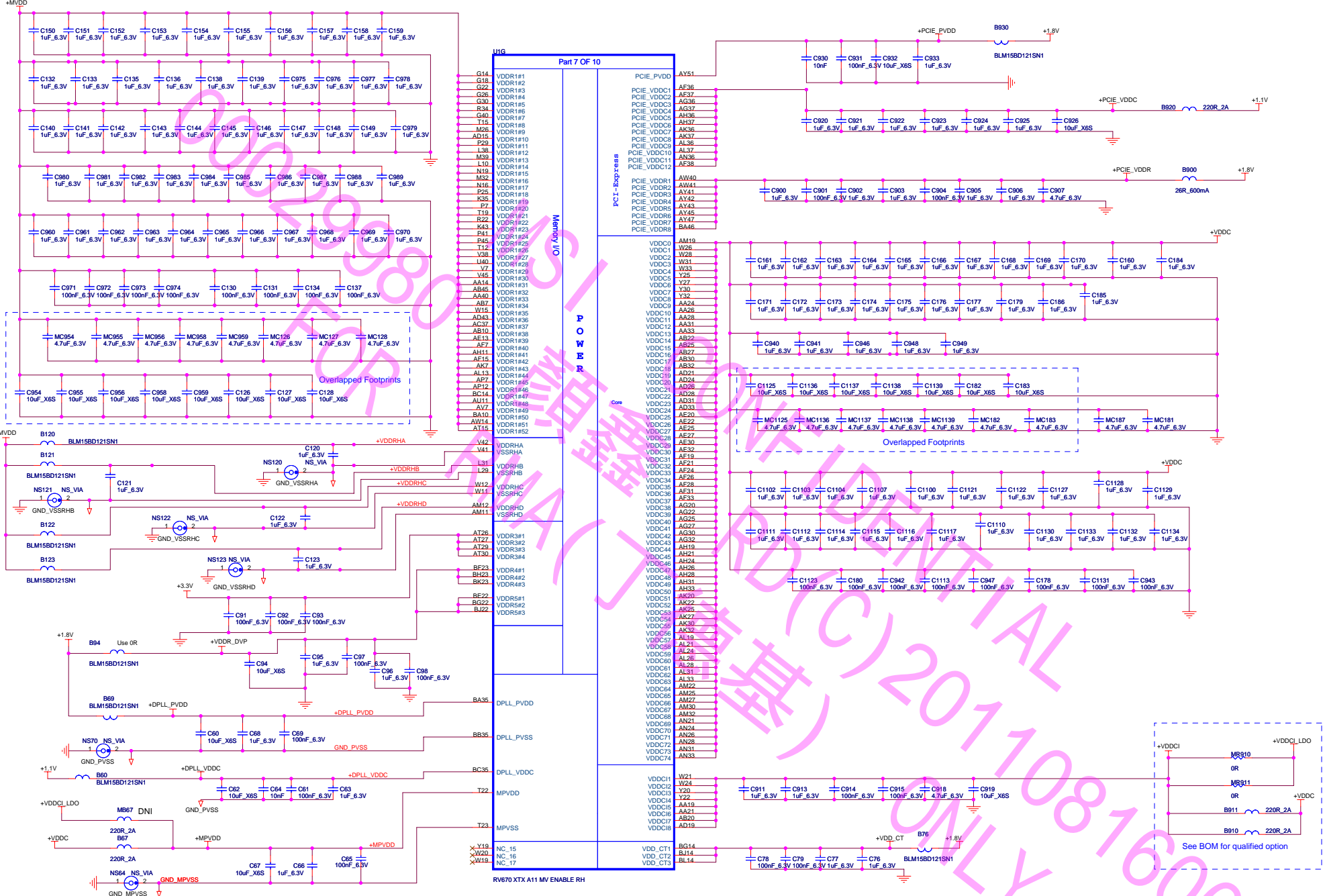
**RV670 ATX 11V ENABLE RH**

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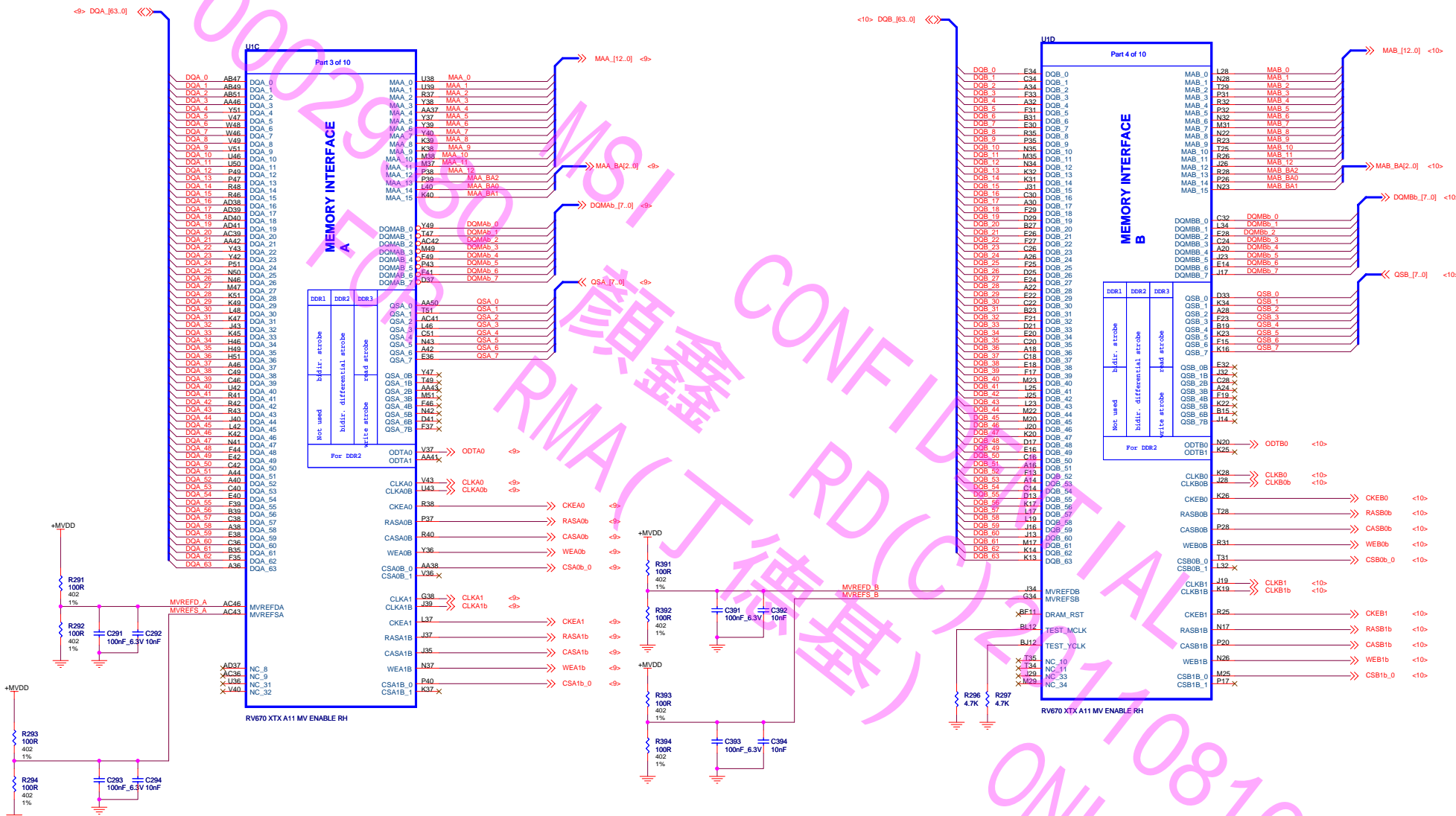
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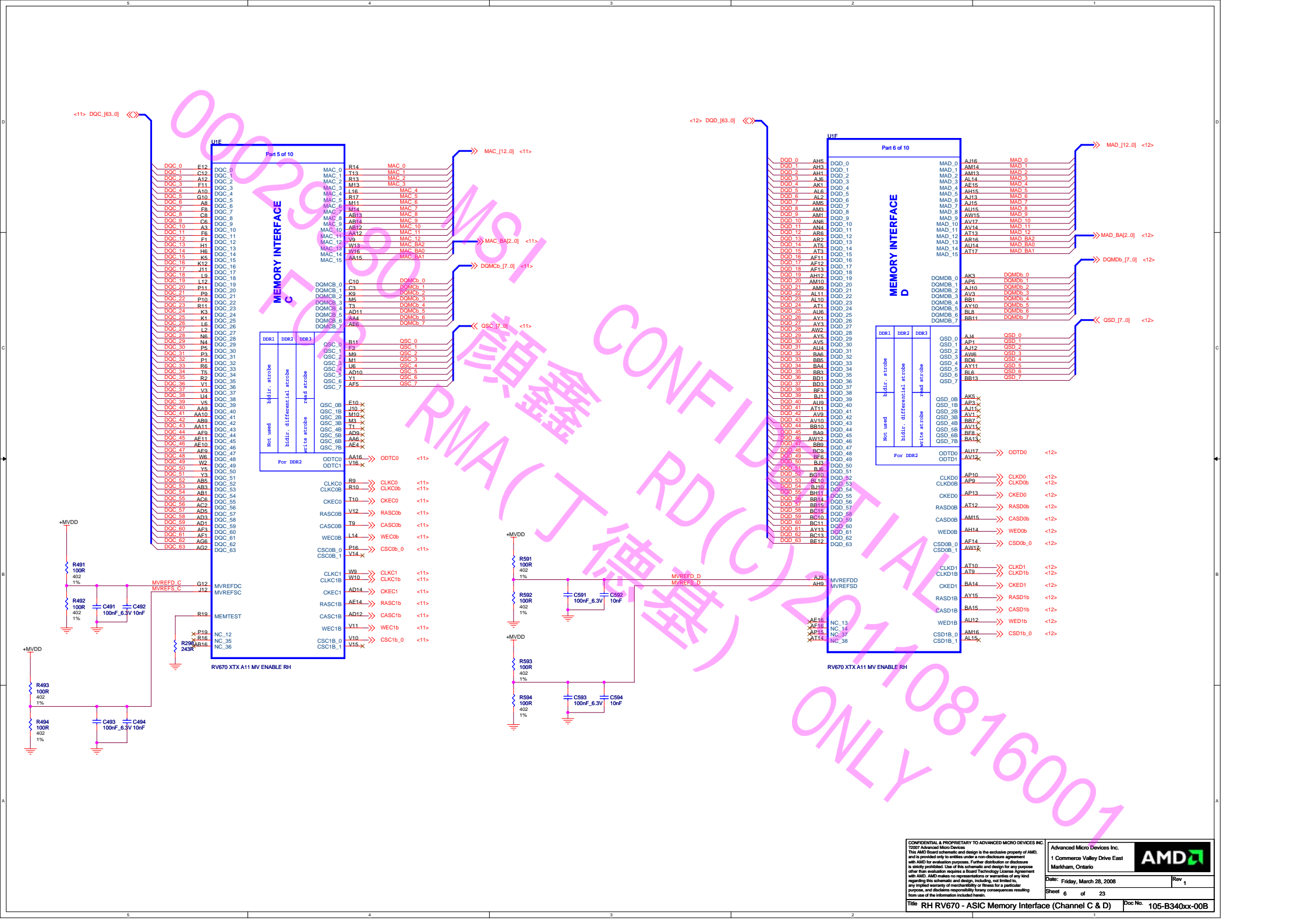
Date: Wednesday, March 26, 2008 Rev 1  
 Sheet 3 of 23  
 Title RH RV670 - ASIC MAIN Doc No. 105-B340xx-00B

INC.	Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario			
Date:	Wednesday, March 26, 2008		Rev	1
Sheet	3	of	23	
Doc No.			105-B340xx-00B	

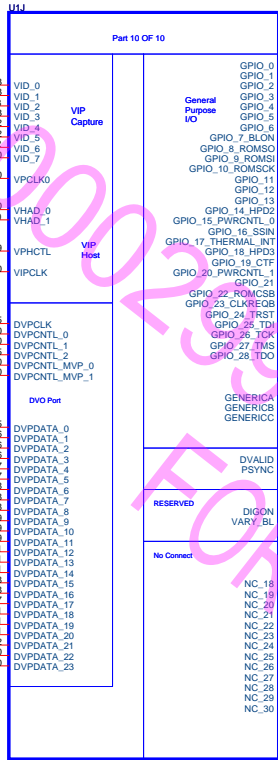


Recommended caps:  
(see BOM for qualified values/vendors)  
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK  
4.7uF , X6S/XSR, 0603, 6.3V/4V  
1uF, X6S, 0402, 6.3V  
100nF, X7R, 0402  
10nF , X7R, 0402









Place SW1 & SW2 on the bottom side (easily accessible).  
Clearly Mark A & B contacts on the silkscreen.

CrossFire

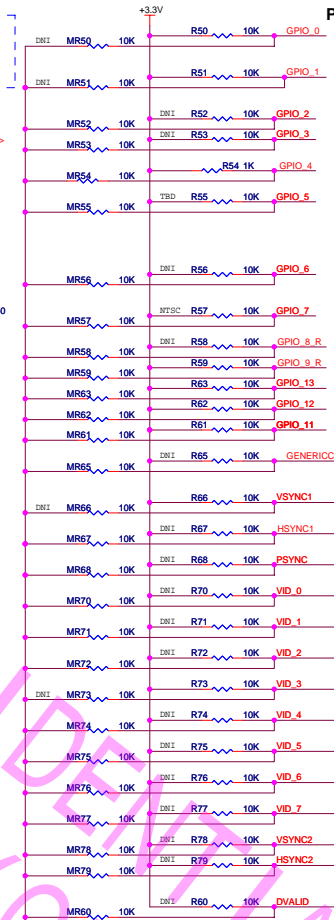
FLOW\_CONTROL\_1 - Lower Cable  
FLOW\_CONTROL\_2 - Upper Cable  
SWAP\_LOCK\_1 - Lower Cable  
SWAP\_LOCK\_2 - Upper Cable

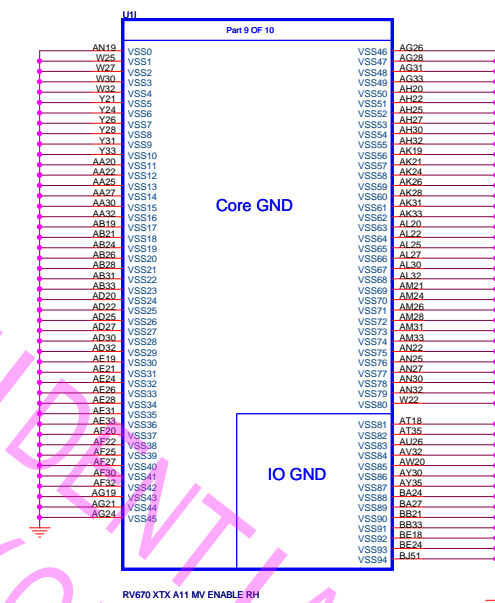
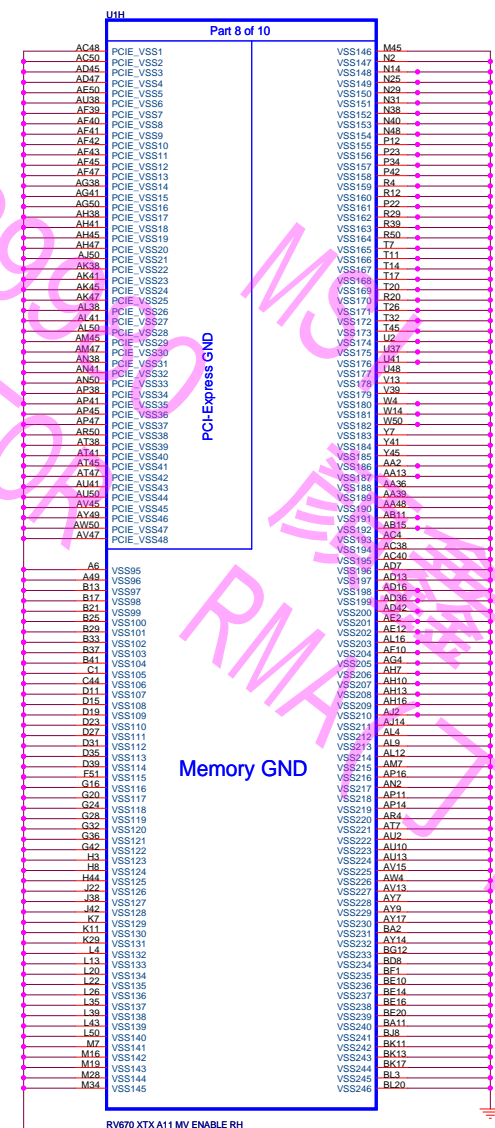
ThermINT <20>

HPD2 <17>

GENERIC\_A <19>

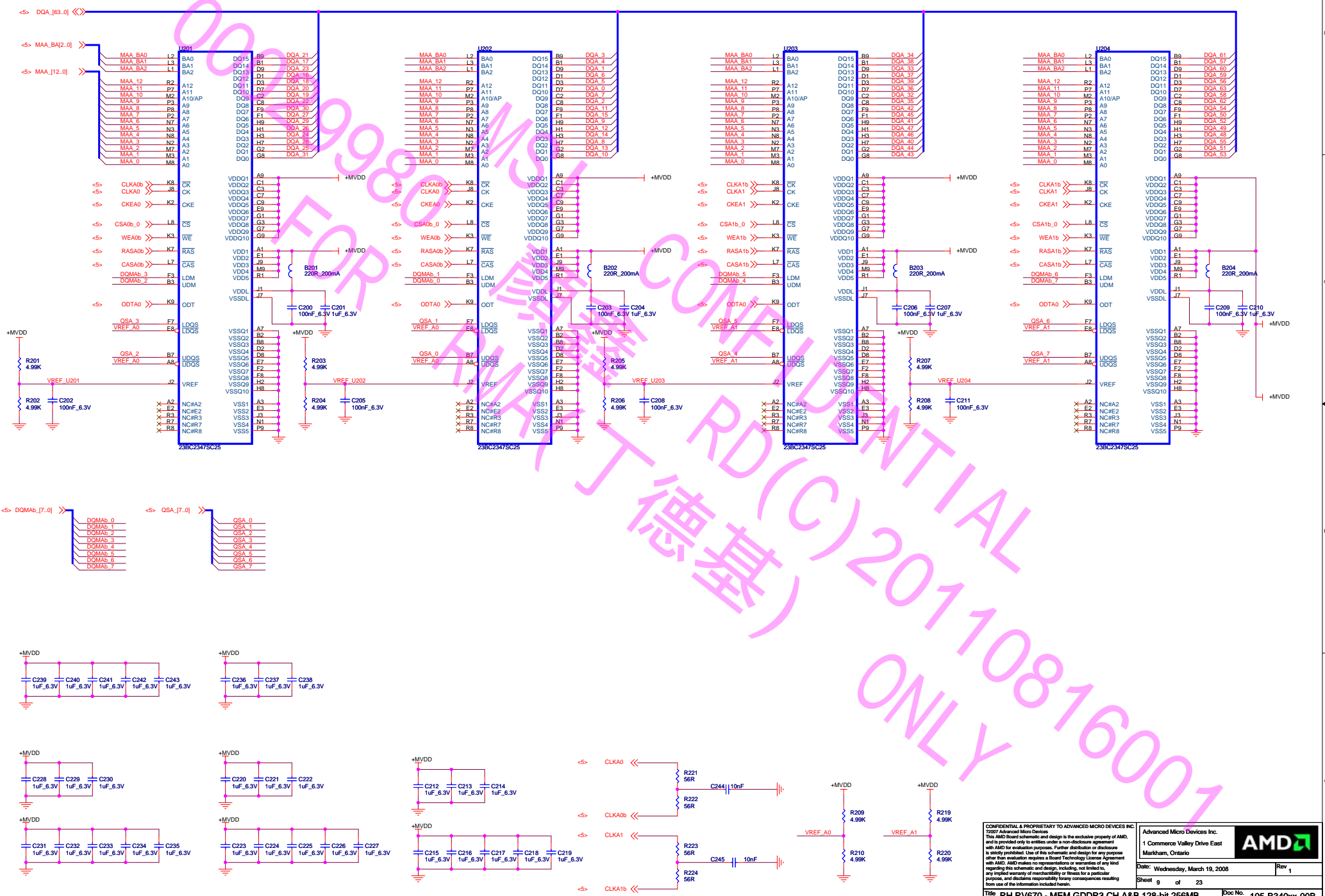
## PIN BASED STRAPS



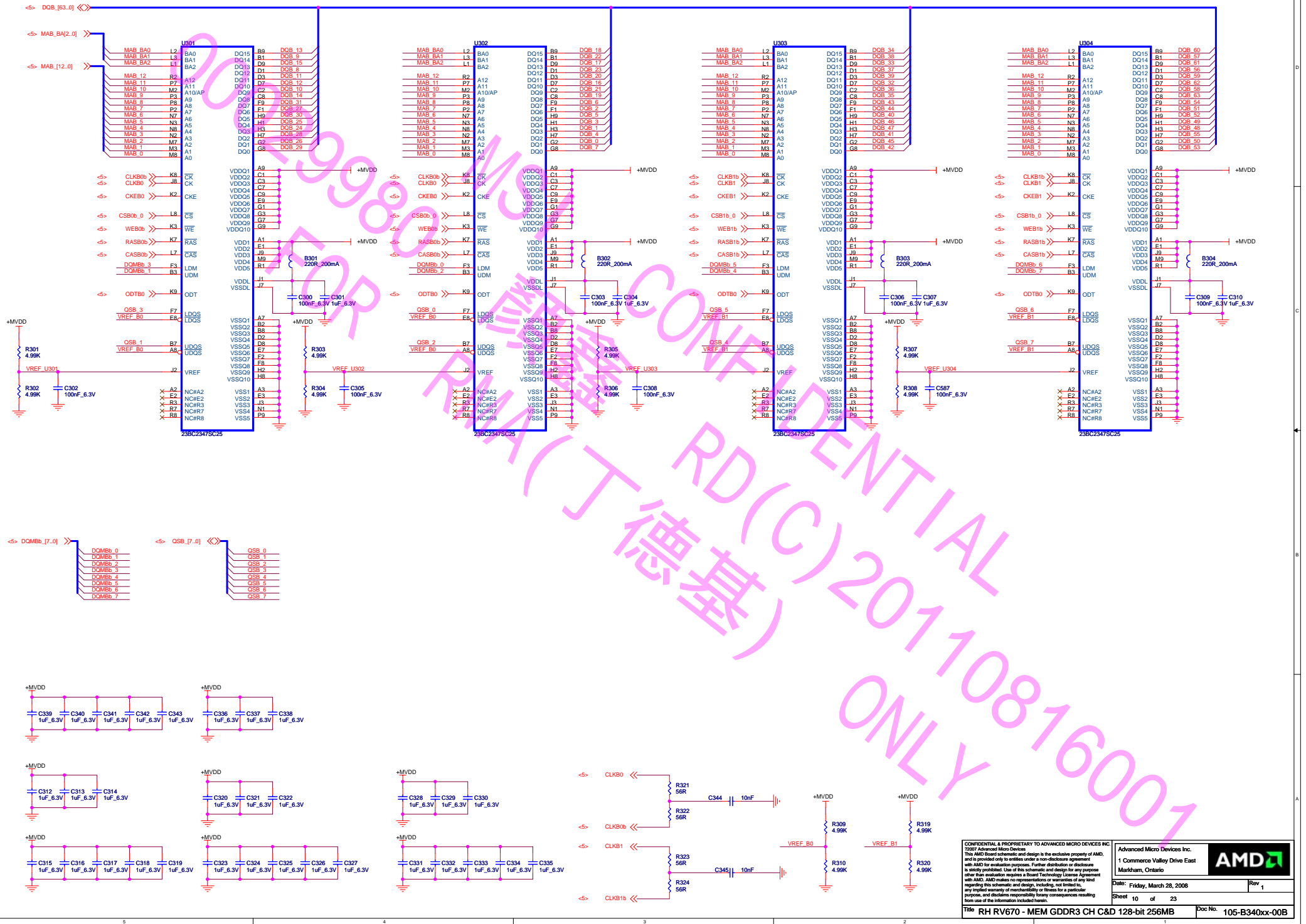




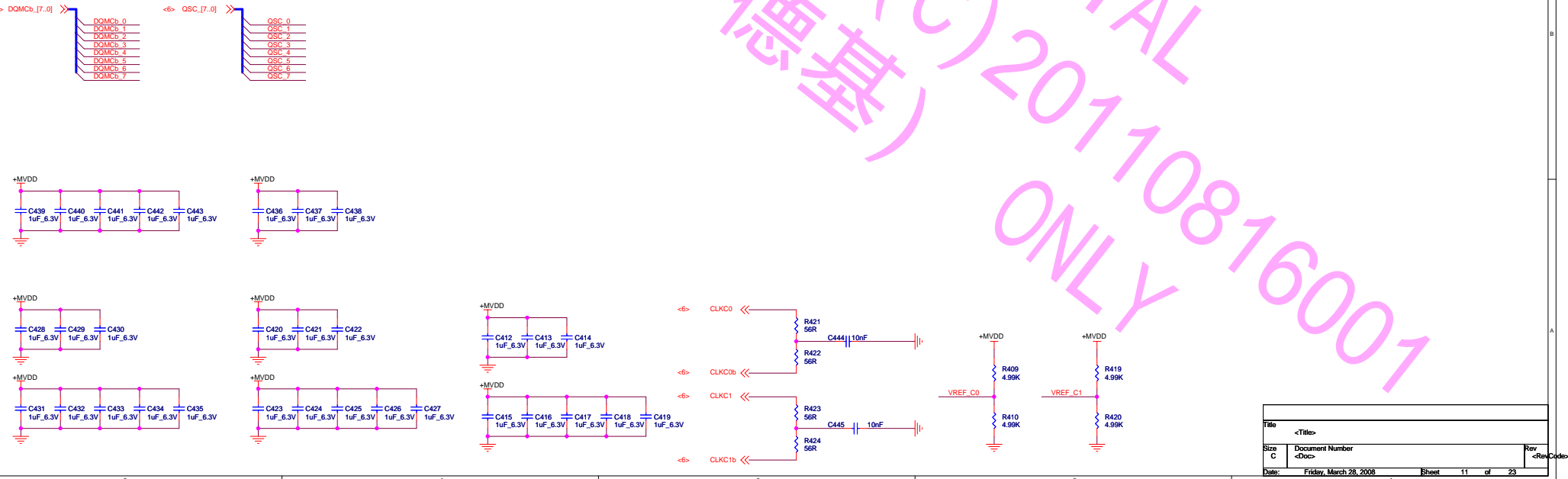
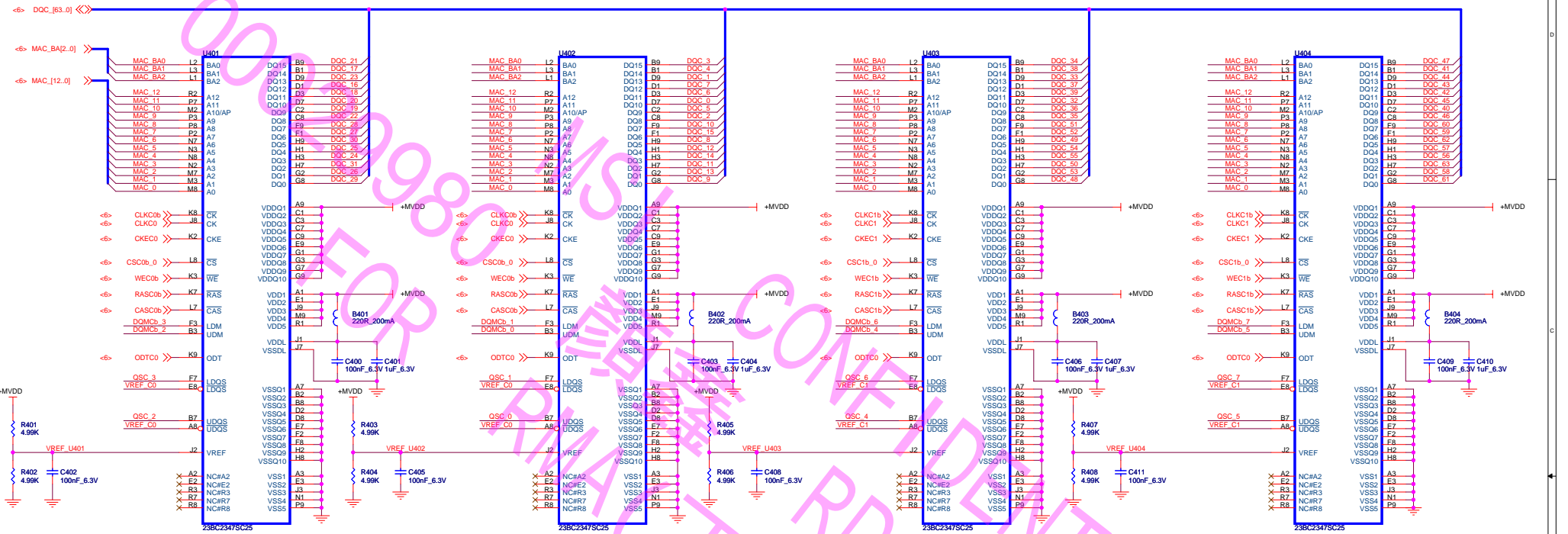
# CHANNEL A: 128MB/256MB DDR2



**CHANNEL B: 128MB/256MB DDR2**

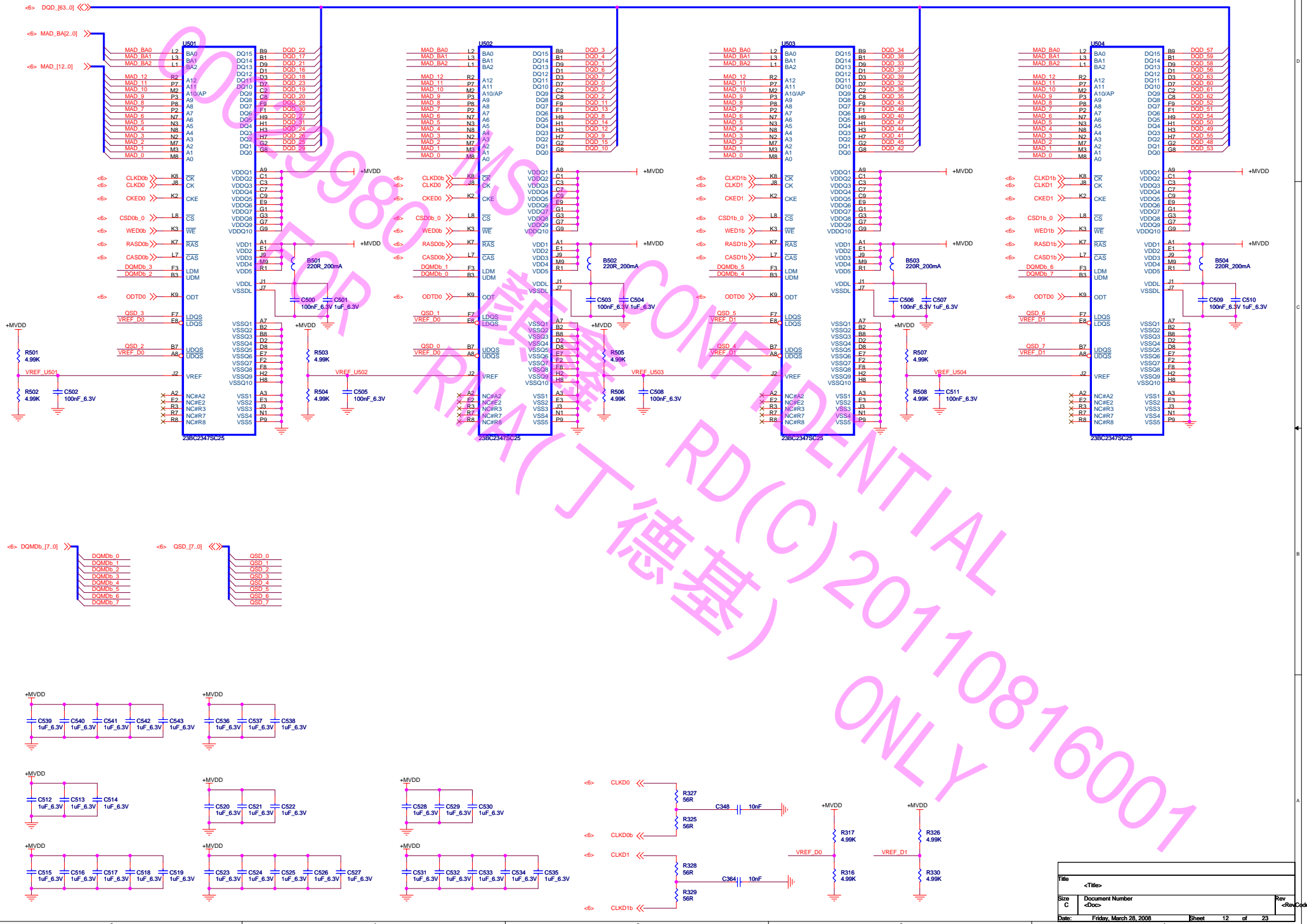


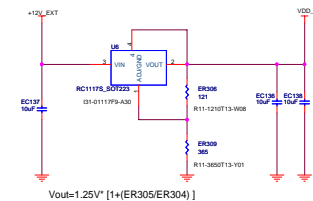
# CHANNEL C: 128MB/256MB DDR2

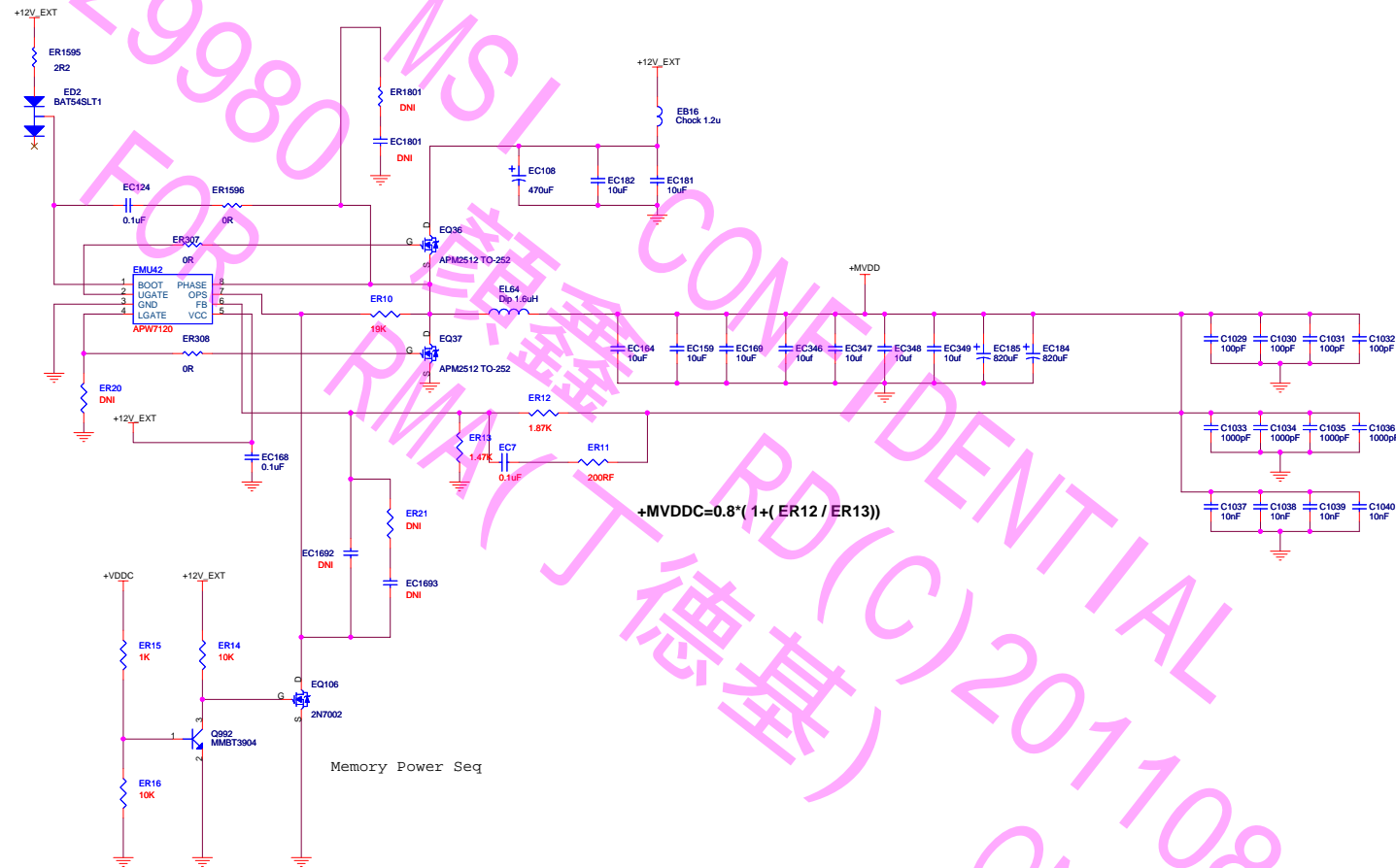


File	<Title>	Rev
Size	Document Number	<Doc>
Date	Friday, March 28, 2008	Sheet 11 of 23

# CHANNEL D: 128MB/256MB DDR2

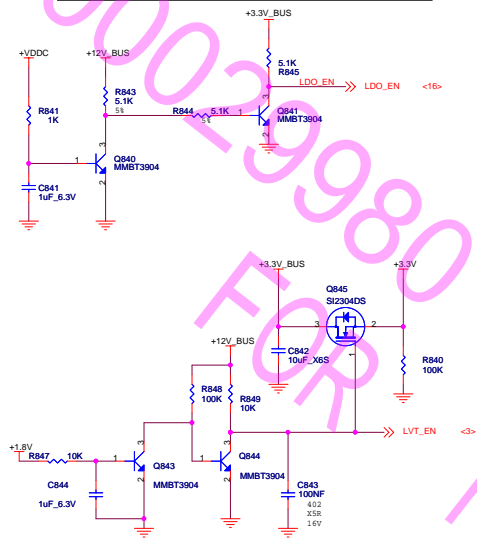




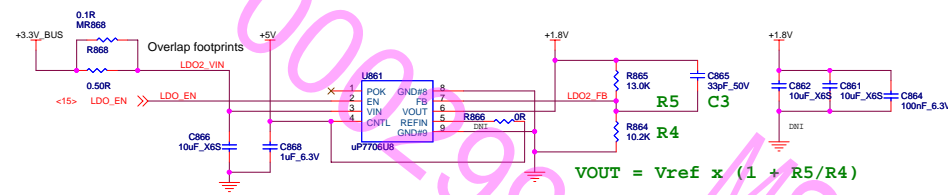




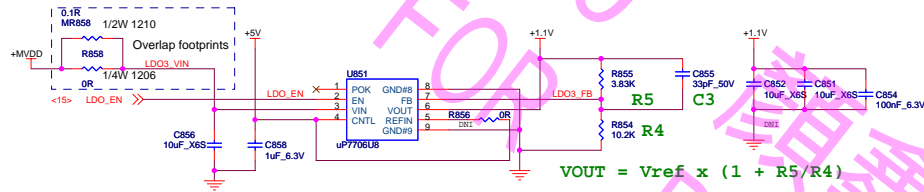
Power up Sequencing



**LDO #2:** Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 0.8A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling

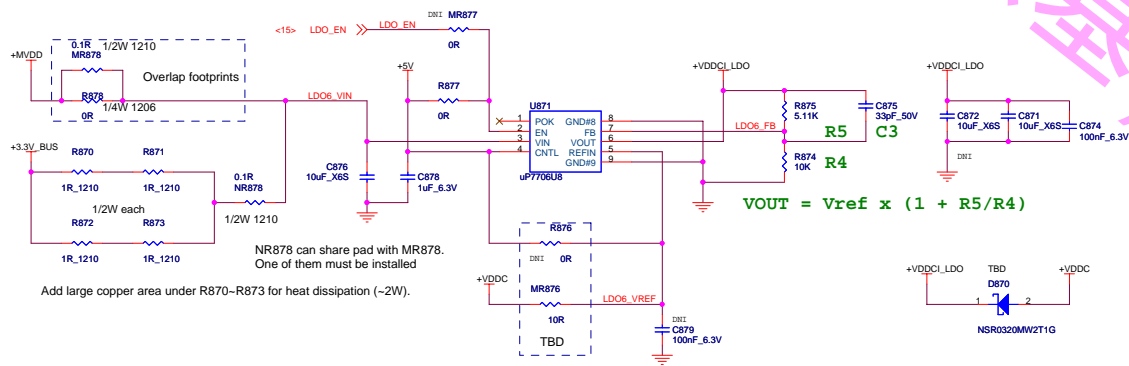


**LDO #3:** Vin = +1.70V to 2.1V MAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling

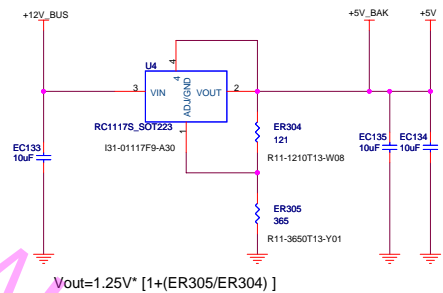


**LDO #6:** For fixed output voltage: Vin = +1.70V to 2.1V MAX Vout = +1.20V +/- 3% Iout = 1.3A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling

**LDO #6:** For tracking VDDC: Vin = TBD Vout = TBD Iout = 1.3A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling



## Regulators for +5V, +5V\_VESA and +5V\_VESA2



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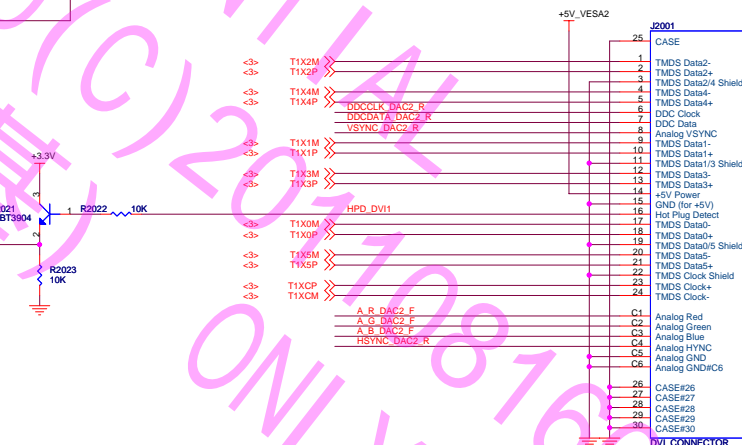
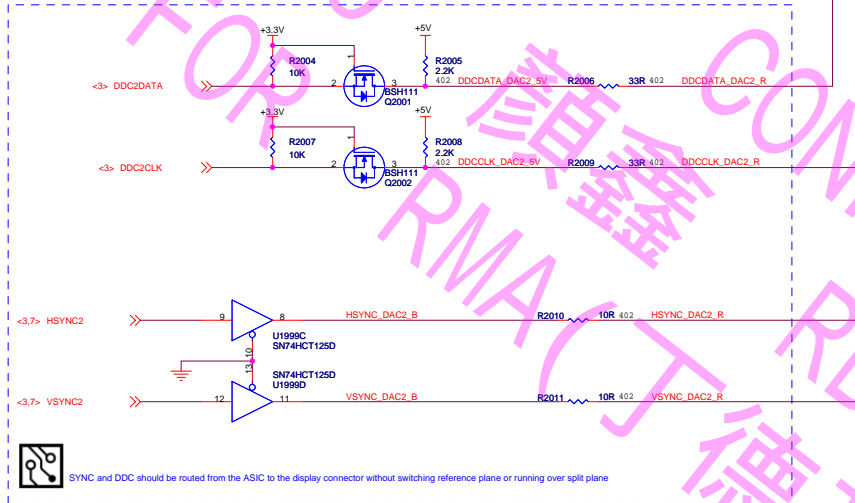
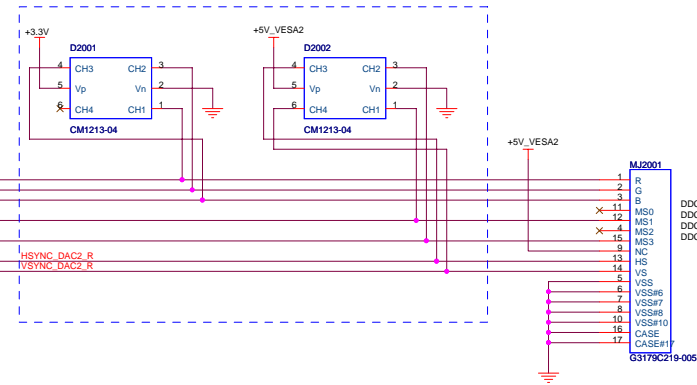
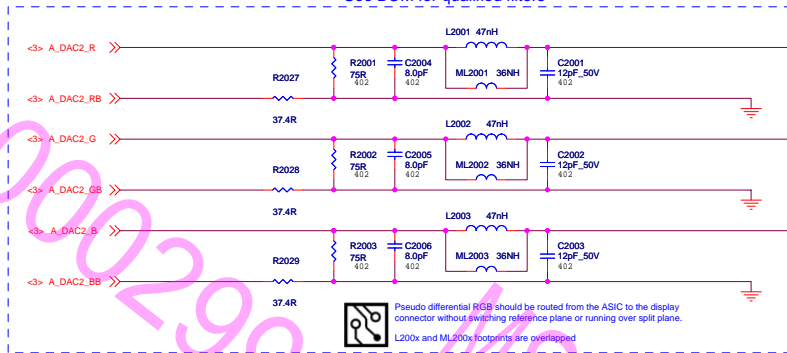
Date: Wednesday, March 10, 2008  
Sheet 16 of 23

Rev 1

Title: RH RV670 - Linear Regulators

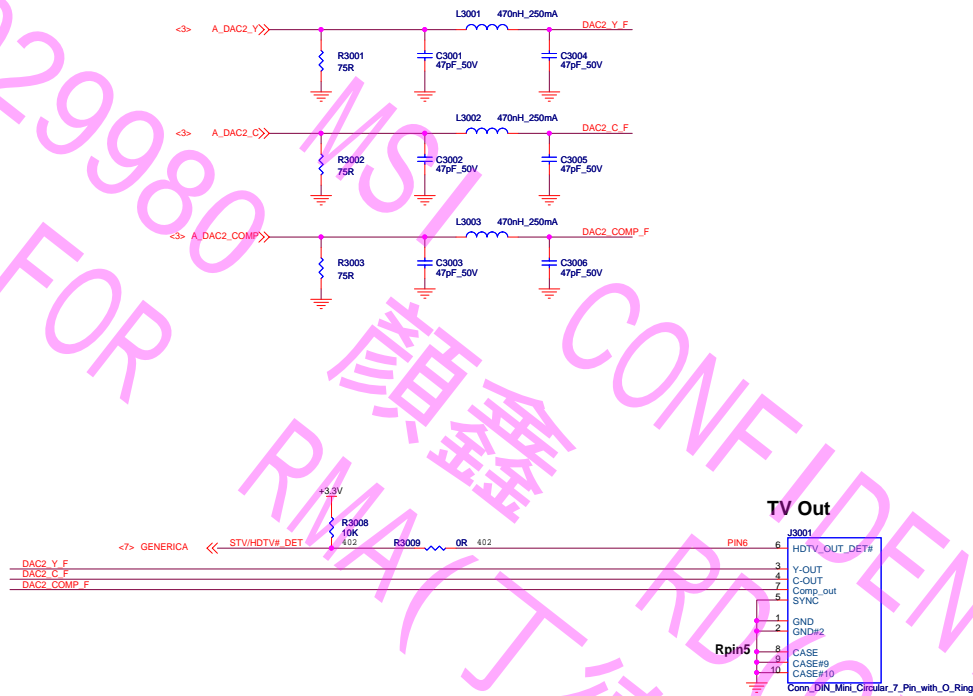
Doc No. 105-B340xx-00B





DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	Open	Open	Optional
9	N/C	+5V	+5V	+5V	Optional
Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



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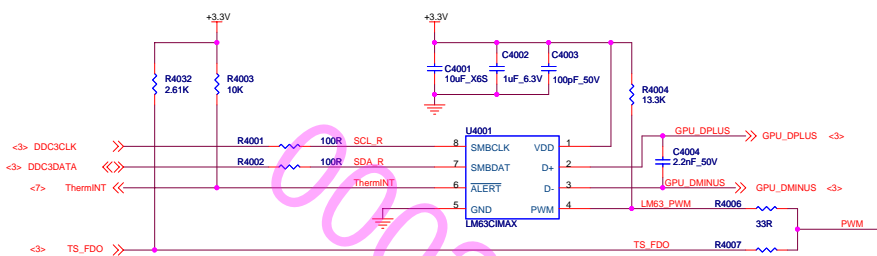
Date: Wednesday, March 10, 2008

Rev 1

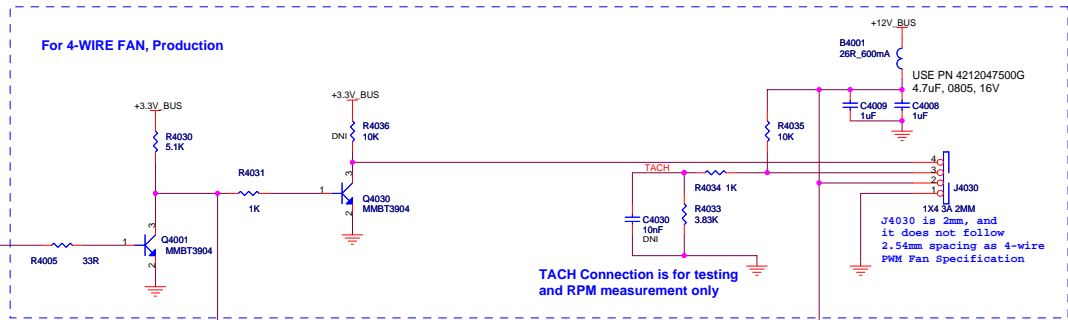
Sheet 19 of 23

Title RH RV670 - TV OUT

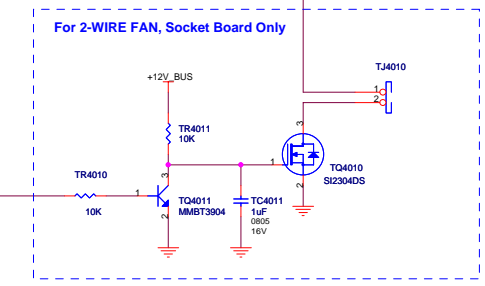
Doc No. 105-B340xx-00B



Warning: TS\_FDO is not 5V tolerant. MAX sink current 1.65mA

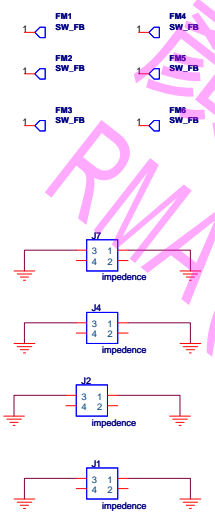
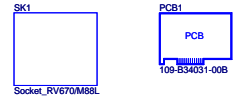
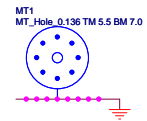
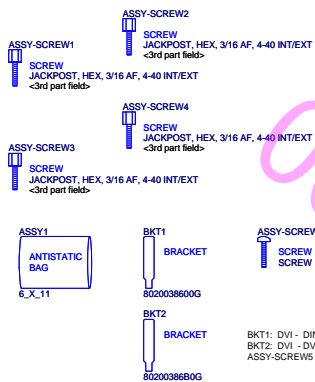


TACH Connection is for testing and RPM measurement only



If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.





<div>AMD</div>			Title RH PCIE RV670 512MB GDDR3 DUAL DL-DVI-I VO FH		Schematic No. 105-B340xx-00B	Date: Thursday, March 13, 2008	
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.				Rev 1
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION				
0	00A	07/05/11	Initial design for RV670 GDDR3 (Revival) based on B339				
1	00B	07/08/1	<p>(pg 1) Adding R1 and connecting switch #7 of TSW1. Some mother boards require B7 to be grounded. Table-1 updated accordingly</p> <p>(pg 7) Adding R64 and MR64 to select HOT_PLUG_DET or ThermINT as the interrupt source.</p> <p>(pg 13) Adding R1617, MR1617, R1616, Q1613, R1615, R1618, and R1619 as option to support hot plug detection of external cable.</p> <p>(pg 13) Adding R1282, MR1282, R1283, MR1283, R1284, MR1284, R1281, R1285, Q1280, and C1280 as option for thermal protection for VDDC SMPS MOSFETs</p> <p>(pg 13) Adding MC1603 (overlapped with C1603)</p> <p>(pg 14) Adding D870 as option for power up sequencing</p> <p>(pg 18) Adding heatsink symbol/footprint</p> <p>(Layout) Increasing spacing between DDC4DATA &amp; DDC4CLK going to U1270 to reduce the crosstalk</p>				

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