

NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X


PCI DEVICE ID 0X0=0X200 FOR NV20.

NVVD SET TO: 1.52V  
FBVDD SET TO: 3.47V  
FBVDDQ SET TO: 2.59V

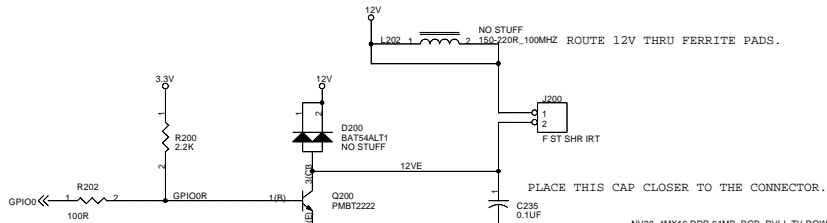
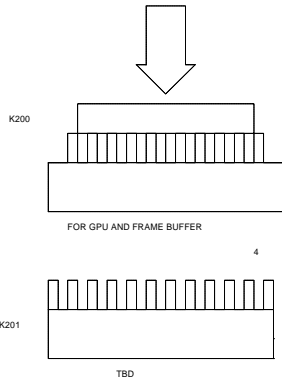
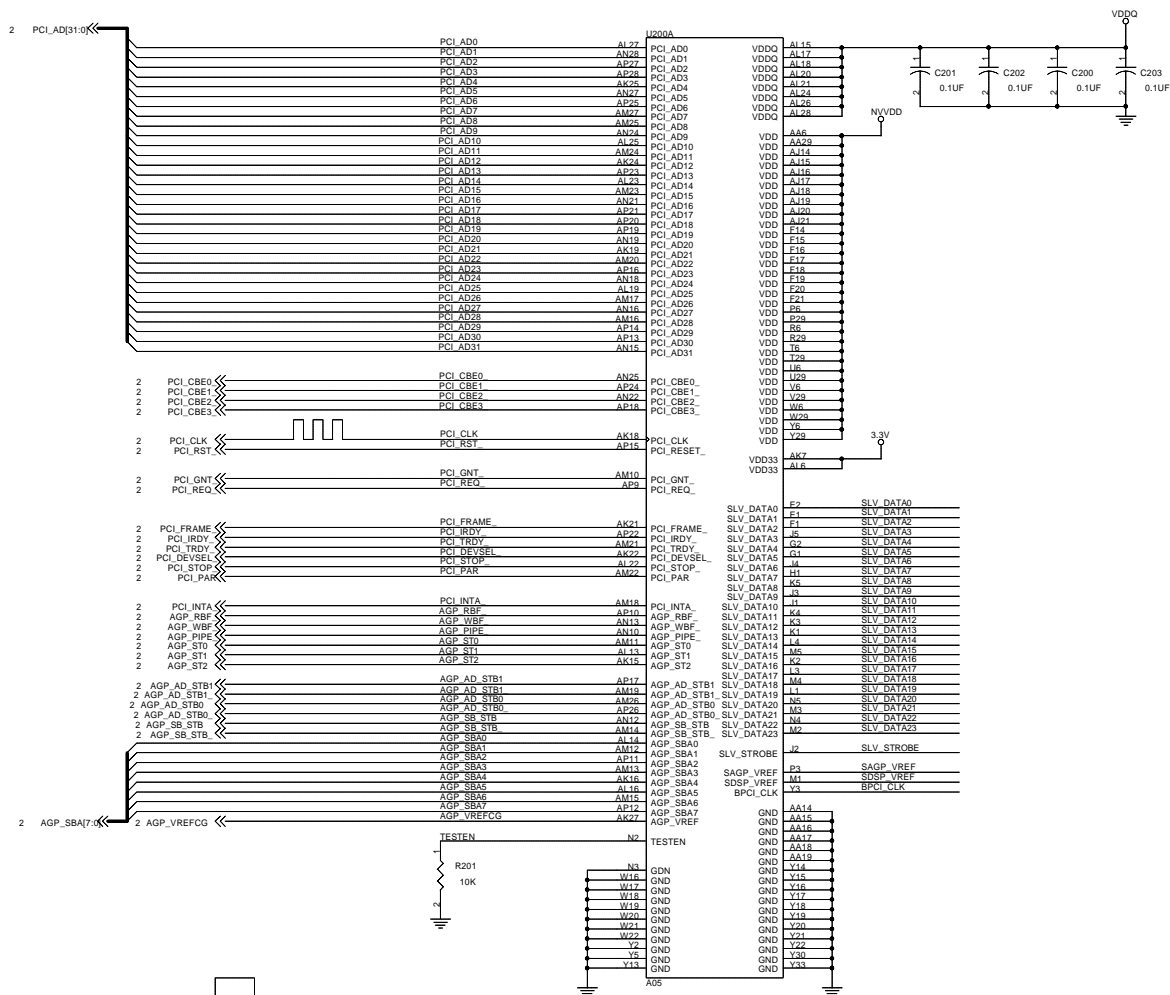
HISTORY REVISION:

- X00: Based on P50-A06
- See change list in 149- file.
  - Set FBVDDQ=2.59V
- P50-A07-X01:
- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)
- P50-A08:
- X04: - Delay PLL\_VDD to come up after NVVDD.
  - X05: - Added 1UF accross R257.
  - X06: - Removed X04-5 above, added a switcher generated PLL delay option.
    - SSEN cap for 2nd SW changed to 1UF.
    - A05 Si, NVVDD=1.52V
- P50-A09:
- X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.
  - X03: - Added option to pull up power good to 12V
- ECO1235: - Changed R841 PU to 10K (from 4.7K)


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602-P0050-0000-A09			
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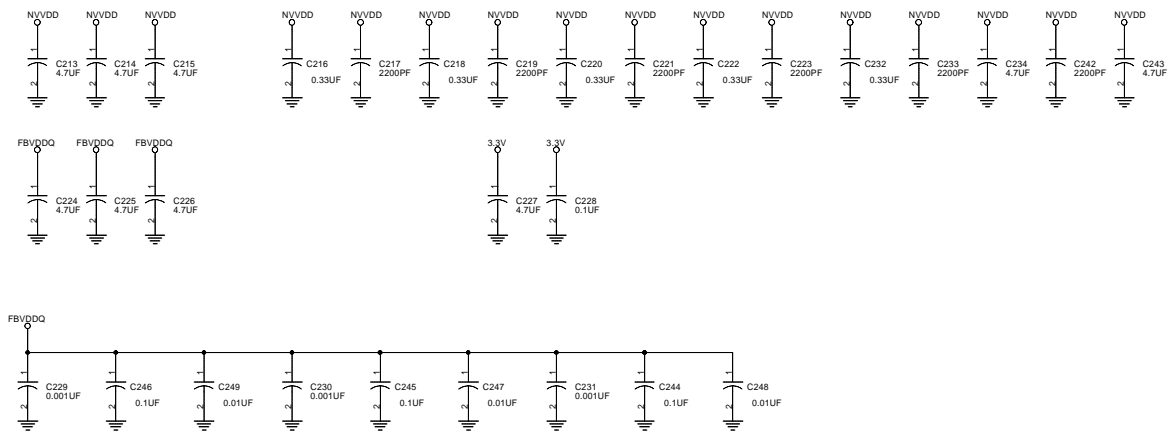




## 2.1 NV20 HOST


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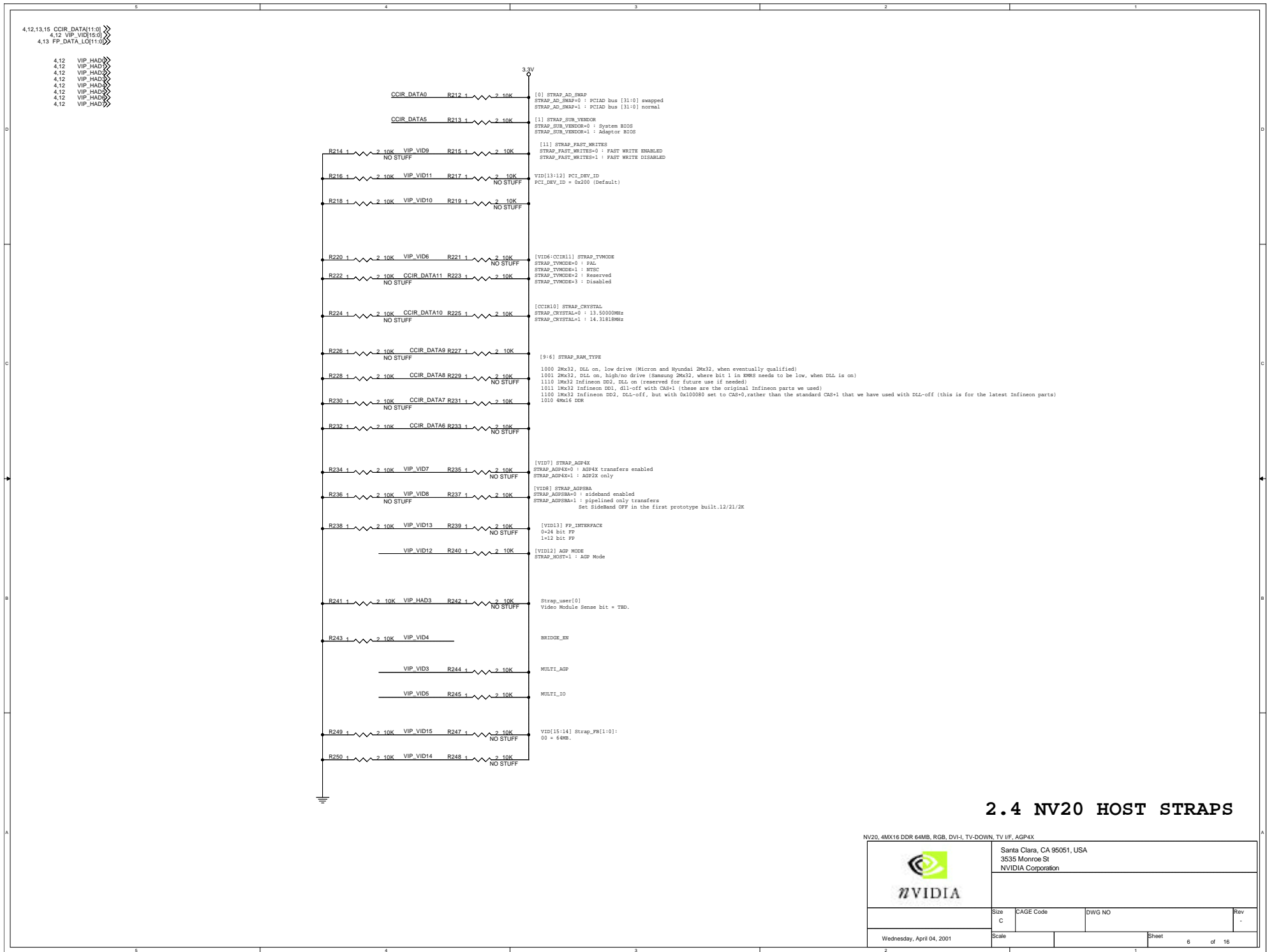




## 2.3 NV20 DECOUPLING


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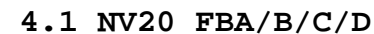


## 2.4 NV20 HOST STRAPS

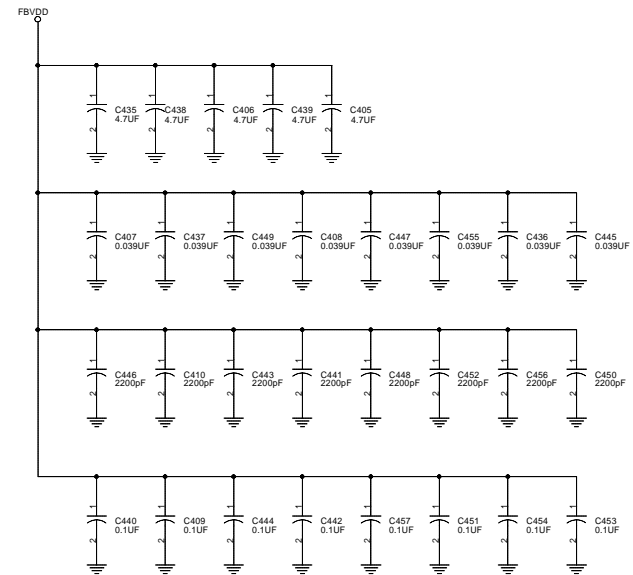
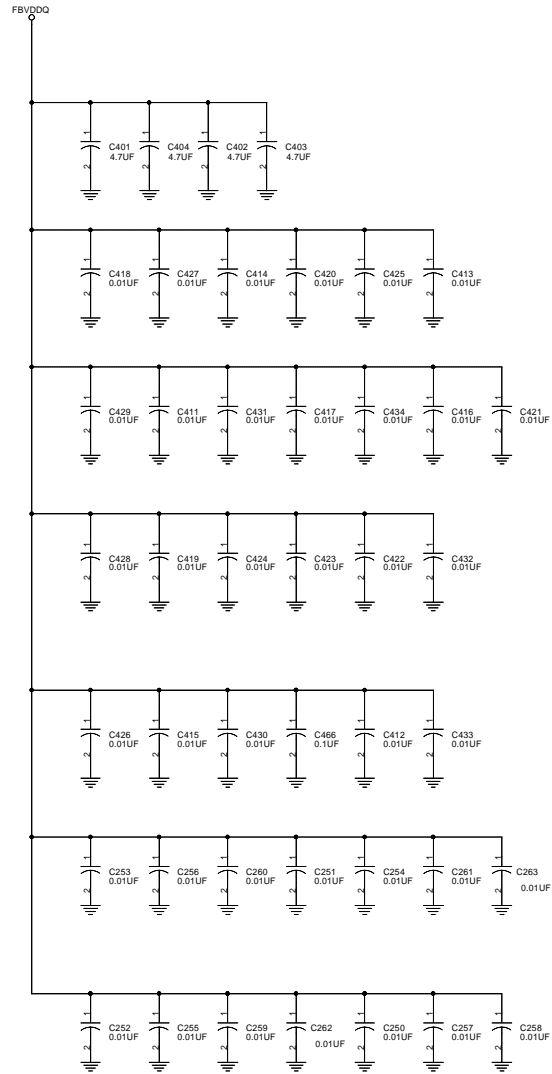
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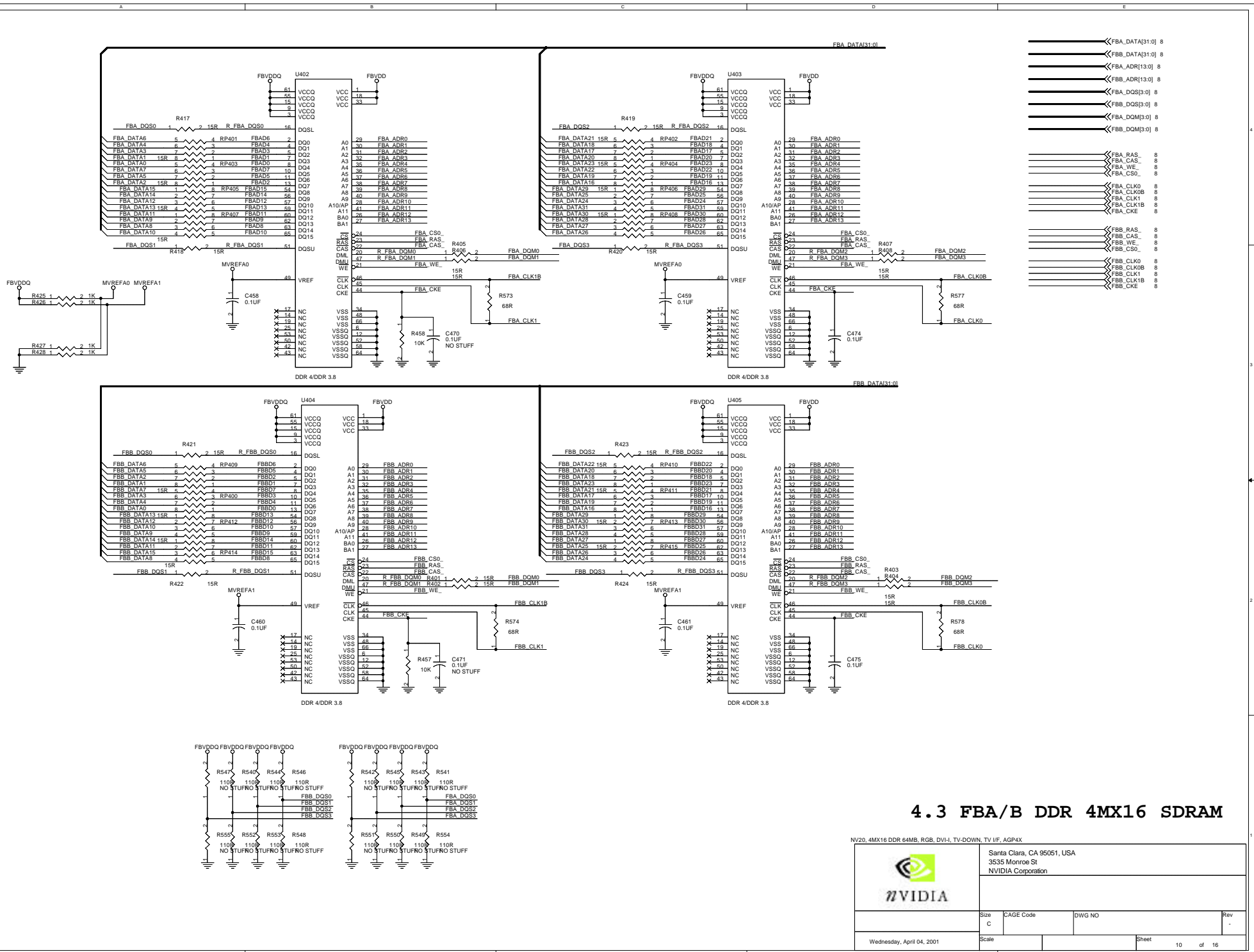




## 4.2 FB DECOUPLING 4MX16 SDRAM

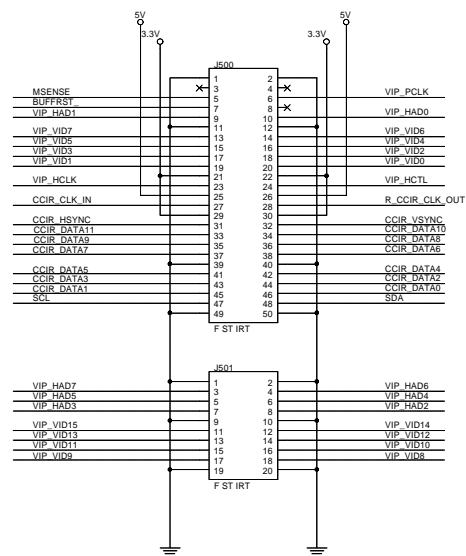
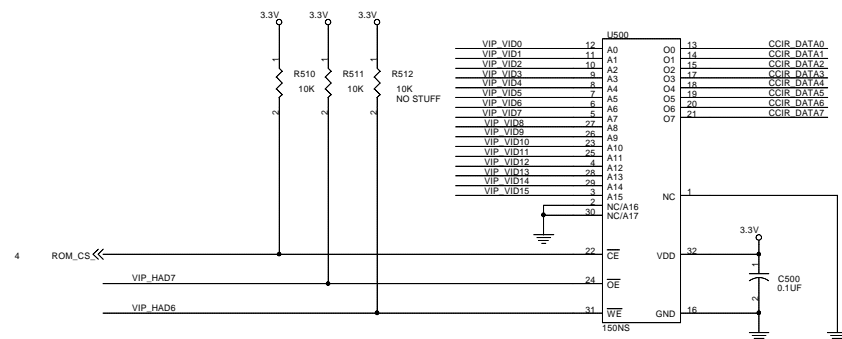
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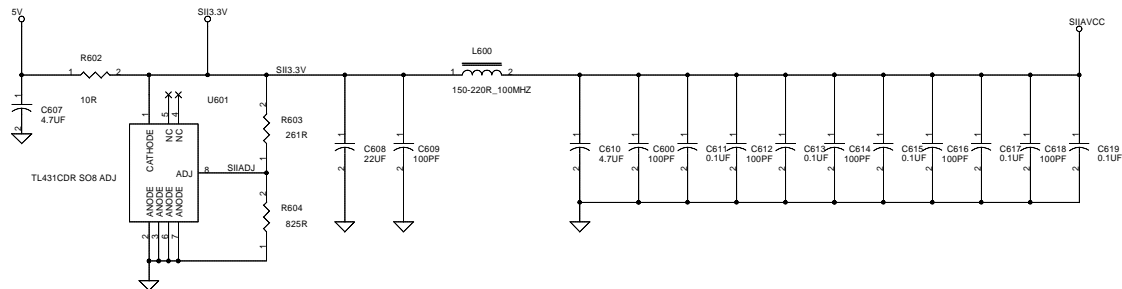
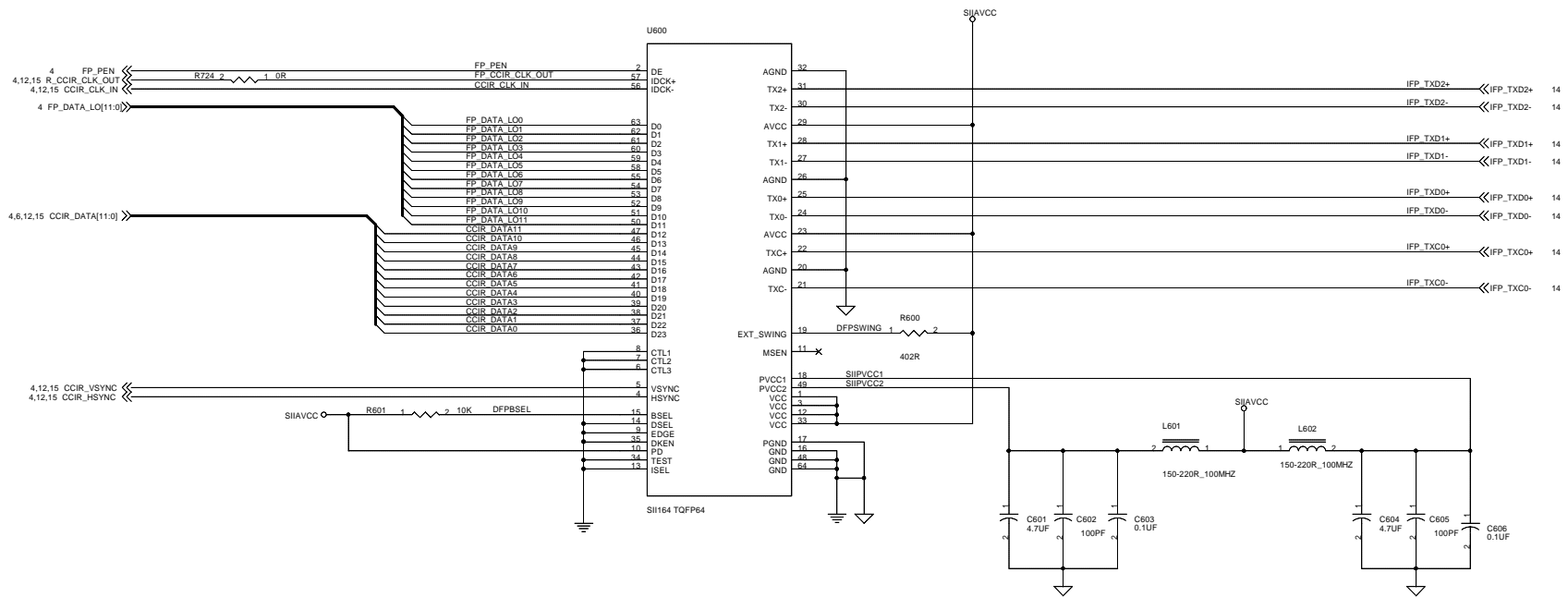
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 4 VIP\_PCLK <<  
 4 VIP\_HCLK <<  
 4 VIP\_HCTL <<  
 4 VIP\_HAD0 >>  
 4 VIP\_HAD1 >>  
 4 VIP\_HAD2 >>  
 4.6 VIP\_HAD3 >>  
 4 VIP\_HAD4 >>  
 4 VIP\_HAD5 >>  
 4 VIP\_HAD6 >>  
 4 VIP\_HAD7 >>  
 4.6,13,15 CCIR\_DATA[11:0] >>  
 4,13,15 CCIR\_HSYNC <<  
 4,13,15 CCIR\_VSYNC <<  
 4,13,15 CCIR\_CLK\_IN <<  
 4,13,15 R\_CCIR\_CLK\_OUT <<  
 4,15 BUFFERST <<  
 4,14,15 SCL <<  
 4,14,15 SDA <<



## 5.1 ROM VIP & VIDEO IF


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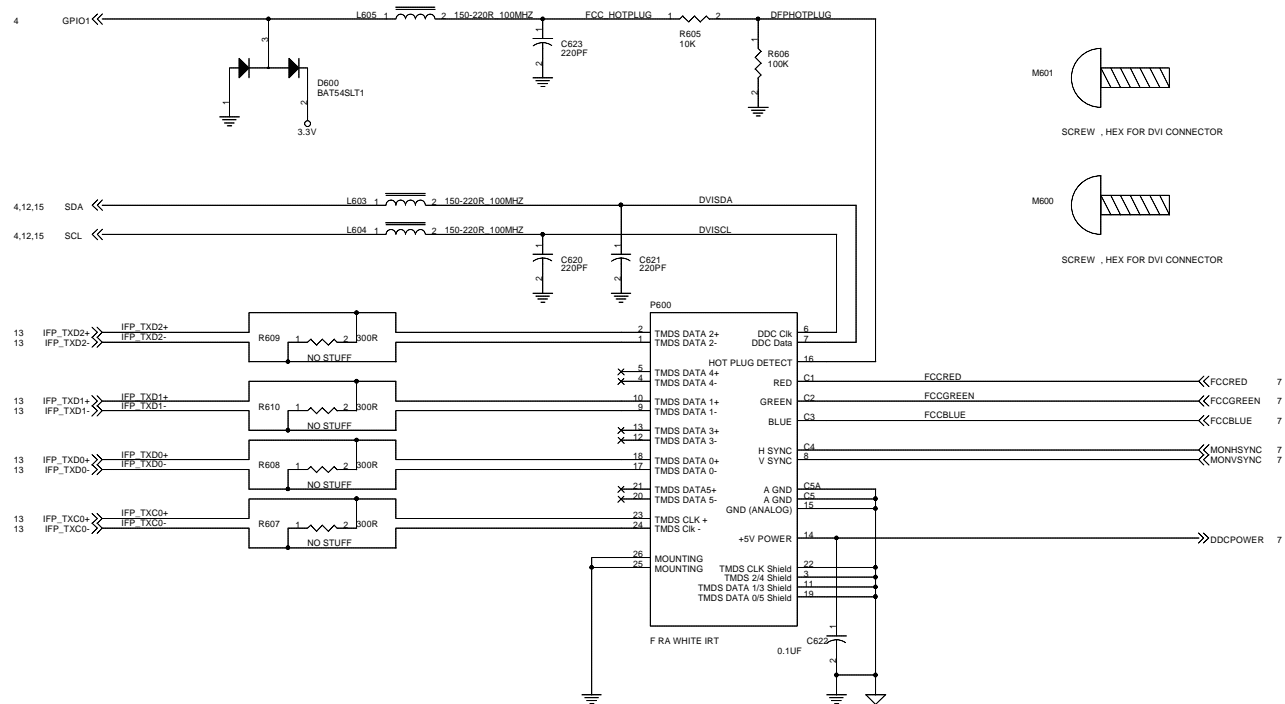
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## 6.1 EXTERNAL DFP/DVI

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## 6.2 DVI-I I/O

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