<variant_name>

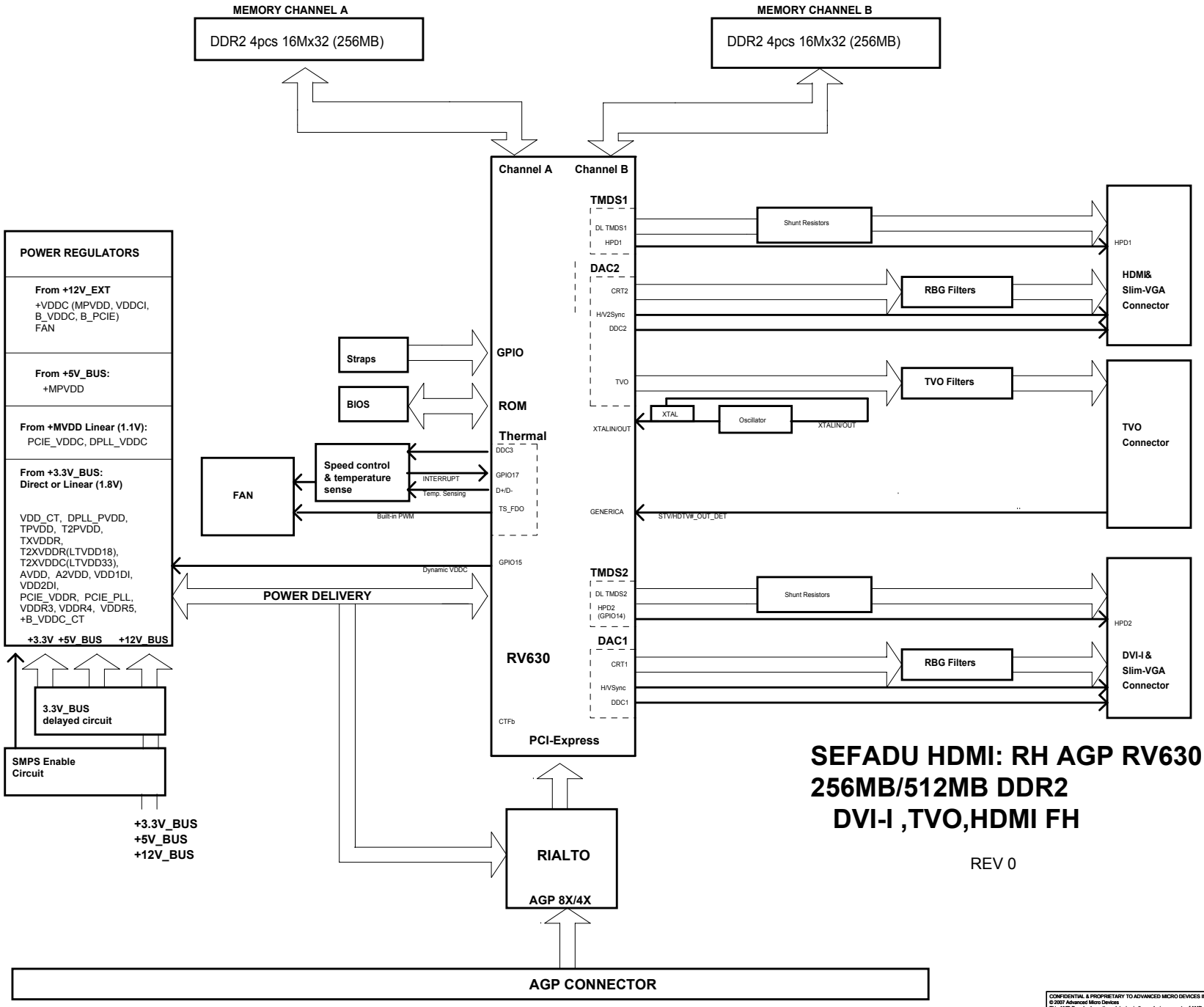
Title: RV630 DDR2-REVISION HISTORY	Schematic No.: 105-B281xx-00A	Date: Friday, May 04, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/04/20	Initial design for RV630 DDR2 AGP, BASES ON B236



SEFADU HDMI: RH AGP RV630 256MB/512MB DDR2 DVI-I ,TVO,HDMI FH

REV 0

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Title	RV630 DDR2-BLOCK DIAGRAM
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AGP EDGE CONNECTOR

LAYOUT NOTE: SOME OF THE CAPS BELOW MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

+12V_BUS: C1509 10uF_20V

+5V_BUS: C1506 47uF_6.3V

+3.3V_BUS: C1501 47uF_6.3V

+VDDQ_BUS: C1508 100uF_6.3V

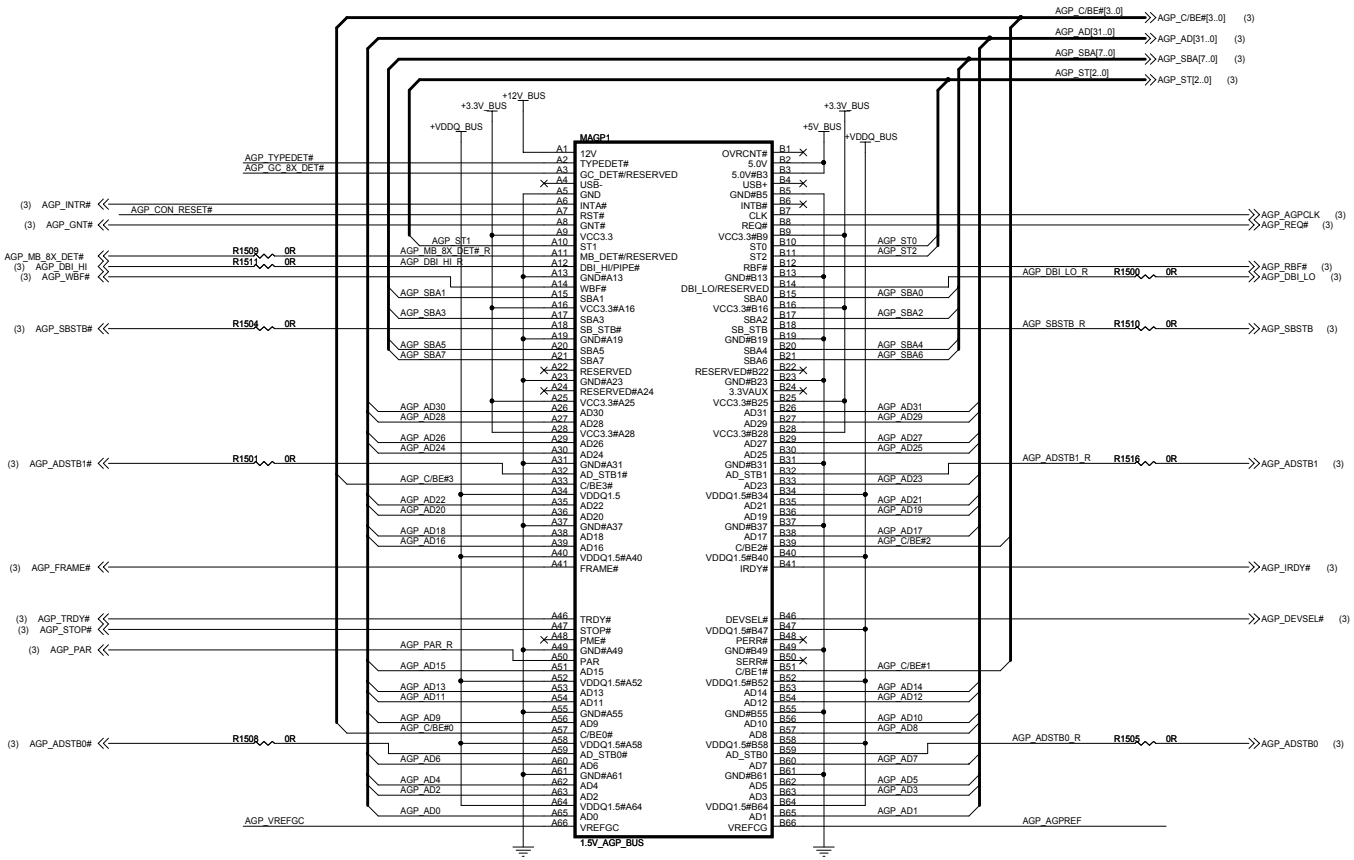
Use 47uF Tant. 16V 20% D size (P/N 4230047600), 800mR Max. ESR and Max. ripple 430mA @ 100kHz
or
100uF, Alum. 6.3V 20% 6.3mm dia (P/N 4261010700), 440mR Max. ESR and Max. ripple 230mA @ 100kHz
or
47uF, Alum. 6.3V 20% 5mm dia (P/N 4262047600), 760mR Max. ESR and Max. ripple 150mA @ 100kHz

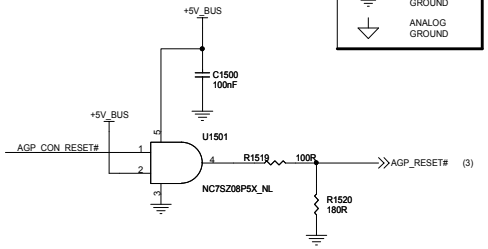
Place C2 on left side of AGP connector

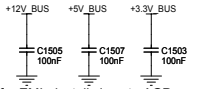
SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

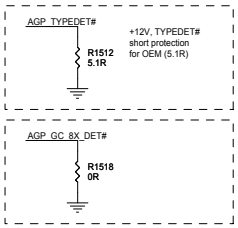
4X/8X AGP BUS



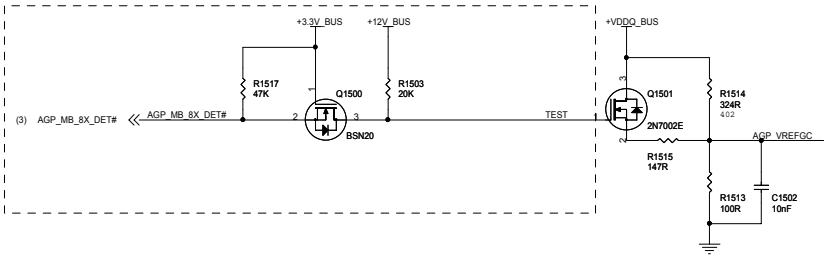




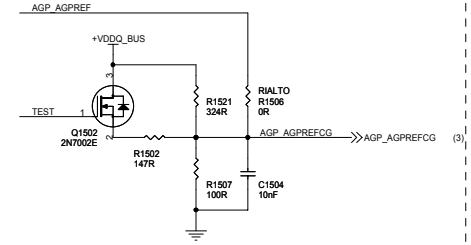
Caps for EMI - install close to AGP connector



UNIVERSAL VREFGC CIRCUIT (4X, 8X)



UNIVERSAL VREFCG CIRCUIT (4X, 8X)



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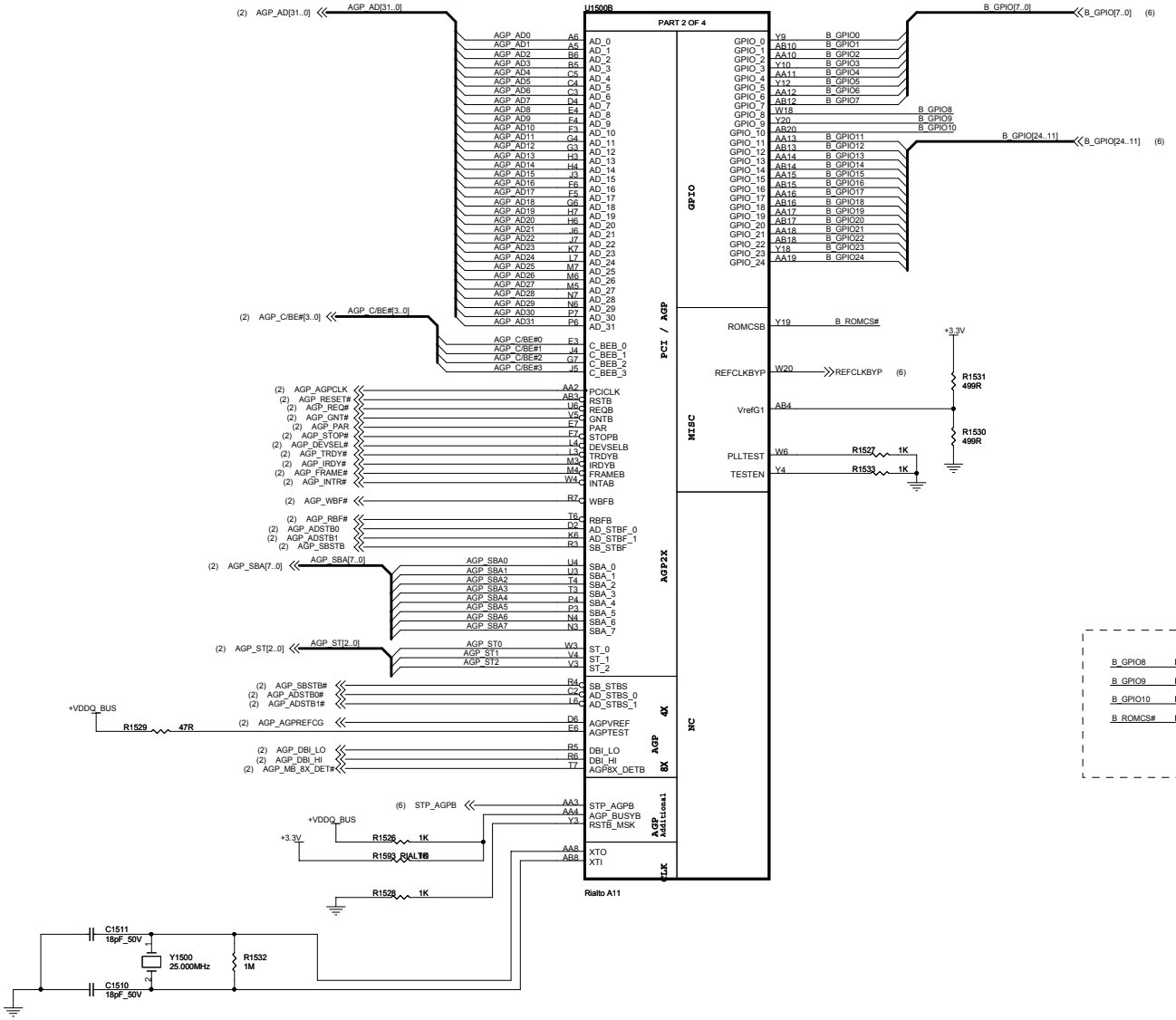
Title	RH AGP RV560 256MB GDDR3 DUAL DL-DVI-I VIVO
Doc No.	105-B281xx-00A



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Title RH AGP RV560 256MB GDDR3 DUAL DL-DVI-I VIVO

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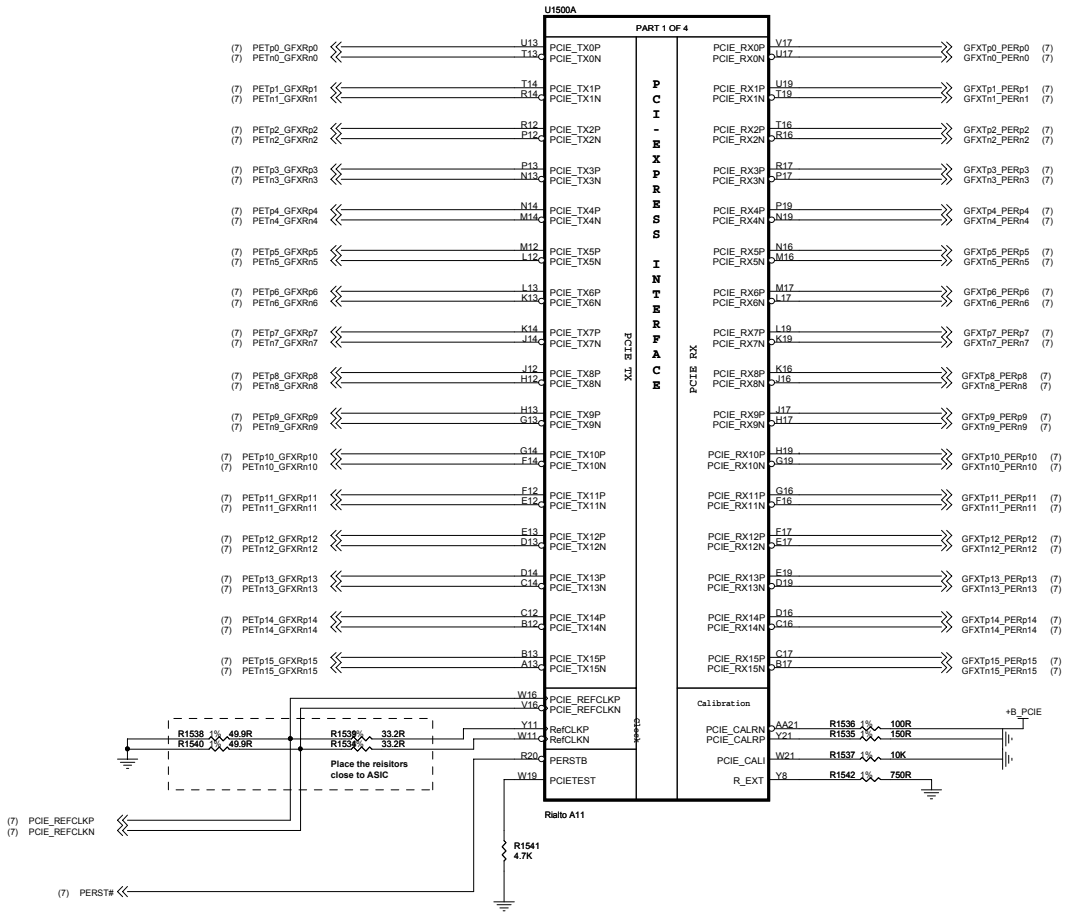
Rialto ASIC p/n is: 218BAPAGA11F



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Title RH AGP RV560 256MB GDDR3 DUAL DL-DVI-I VIVO

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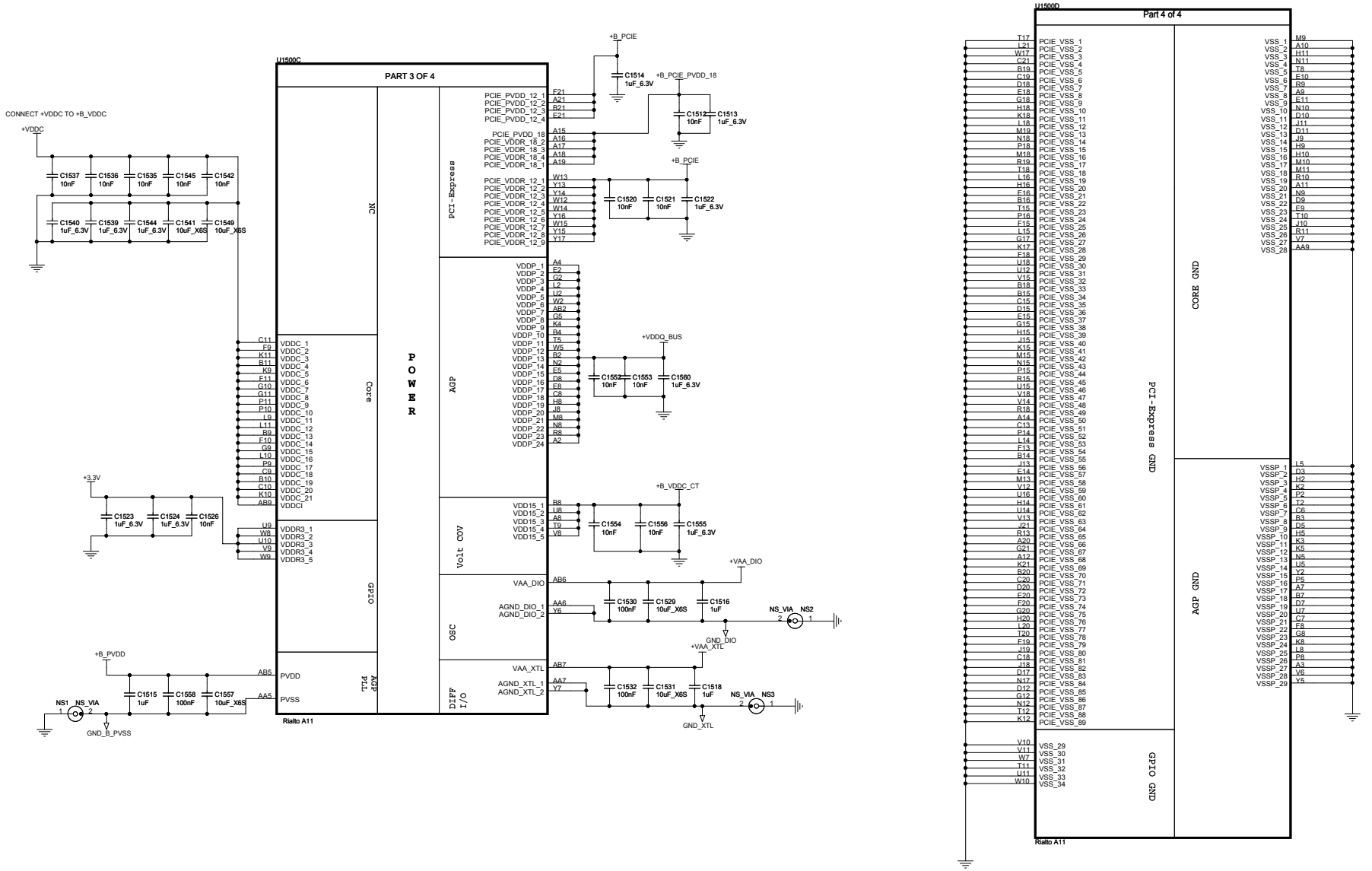

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Title RH AGP RV560 256MB GDDR3 DUAL DL-DVI-I VIVO

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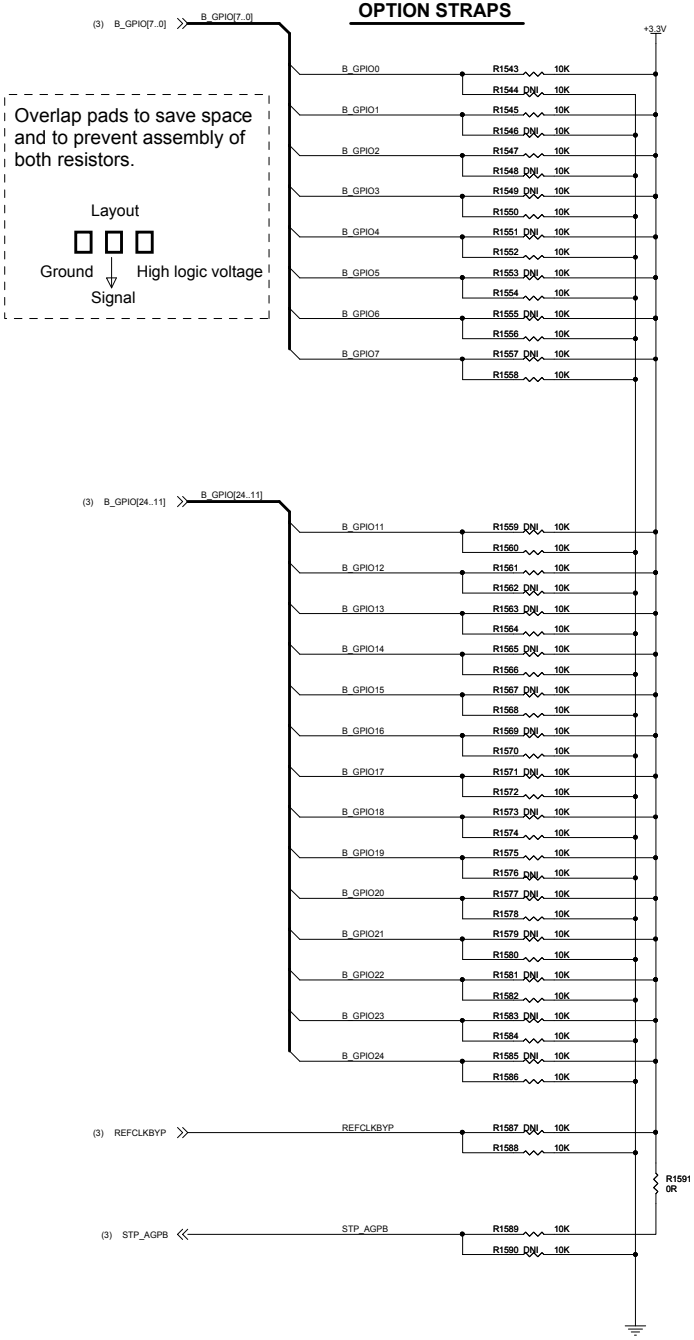
OPTION STRAPS



PCIE_AGP_Bridge Shared Straps

STRAPS	PIN	DESCRIPTION	DEFAULT
PCIE_PTX_PWRS_ENB	GPIO(0)	PCI Express transmitter power-saving enable bar 0 - 50% Tx output swing for mobile applications 1 - Full output swing	1
PCIE_PTX_DEEMPH_EN	GPIO(1)	PCI Express transmitter de-emphasis enable 0 - de-emphasis disenable 1 - de-emphasis enable	1
PCIE_ICP (1:0)	GPIO(3:2)	Charge pump current setting 00 - 5.0uA 01 - 10.0uA **10 - 15.0uA** 11 - 20.0uA	01
PCIE_PTX_IEXT	GPIO(4)	PCI Express transmitter extra ouptput current 0 - no extra current 1 - extra current in output stage	0
DEBUG_ACCESS	GPIO(5)	1 - Set the debug bus muxes to bring out debug signals even if registers are inaccessable	0
PCIE_PPLL_BW	GPIO(6)	PCI Express PLL bandwidth setting 0 - Full PLL bandwidth 1 - Reduces PLL bandwidth	0
PCIE_REVERSE_ALL	GPIO(7)	0 - Don't reverse physical PCIE lanes 1 - Reverse physical PCIE lanes	0
ROMIDCFG(1:0)	GPIO(12:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 00 - No ROM, CHG_ID=0 01 - 512Kb Serial AT25F512 ROM (Atmel) or AT24F1024 ROM (Atmel) **10 - 512K Serial M25P05A ROM (ST) or PM25LV512 (PMC)** 11 - 1M Serial M25P10A ROM (ST) or PM25LV010 (PMC)	10
PCI_RETRY_ENb	GPIO(13)	0 - Enable all PCI read/write retry, retry cycle 0x3 1 - Disable PCI read/write retry	0
VGA_MONO_MODE(1:0)	GPIO(24, 14)	00 - only VGA controller 01 - only MONO controller 10 - neither VGA/MONO controller 11 - both VGA/MONO controller	00
REFCLK_LINK_CONFIG	GPIO(15)	One of the strap bit to encode the combination of: SEND_LINK_TRAINING_IMMEDIATELY MOBILE_EN AGP_ONLY ..... etc,	0
MULTIFUNC	GPIO(16)	For MULTIFUNC, when TESTEN(pin)=0, 0 = 00 - Single function device 1 = 01 - Two function device. No AGP in either function	0
PCIE_FORCE_ COMPLIANCE		For PCIE_FORCE_COMPLIANCE, when TESTEN(pin)=1, 0 - Normal operation 1 - Force LC into compliance mode	0
AGPFBSKEW(1:0)	GPIO(18:17)	AGP 1xclock feedback phase adjustment wrt refclk(cpuclk) 00 - refclk slightly earlier than feedback 01 - refclk 1 tap later than feedback 10 - refclk 1 tap earlier than feedback 11 - refclk 2 tap earlier than feedback clock	00 internal pulldown
X1CLK_SKEW(1:0)	GPIO(20:19)	Clock phase adjustment between x1clk and x2clk 00 - 0 tap delay 01 - 1 tap delay 10 - 2 tap delay 11 - 3 tap delay	00 internal pulldown
BUSCFG	GPIO(21)	Control BUS type, CLK PLL select	0 internal pulldown
AGP_ONLY	GPIO(22)	0 - normal operation, assume VPU is working 1 - for debugging, shut off VPU so the bridge is working in AGP only mode	0
PCIE_LINK_TIMEOUT _OVERRIDE	GPIO(23)	0 - Timeout is active 1 - Timeout is disabled	0
MOBILE_EN	REFCLKBYP		0
BUS_PCI_CFG_ RETRY_Enb	STP_AGPB	when internal MOBILE_EN=0 STRAP_BUS_PCI_CFG_RETRY_Enb	1

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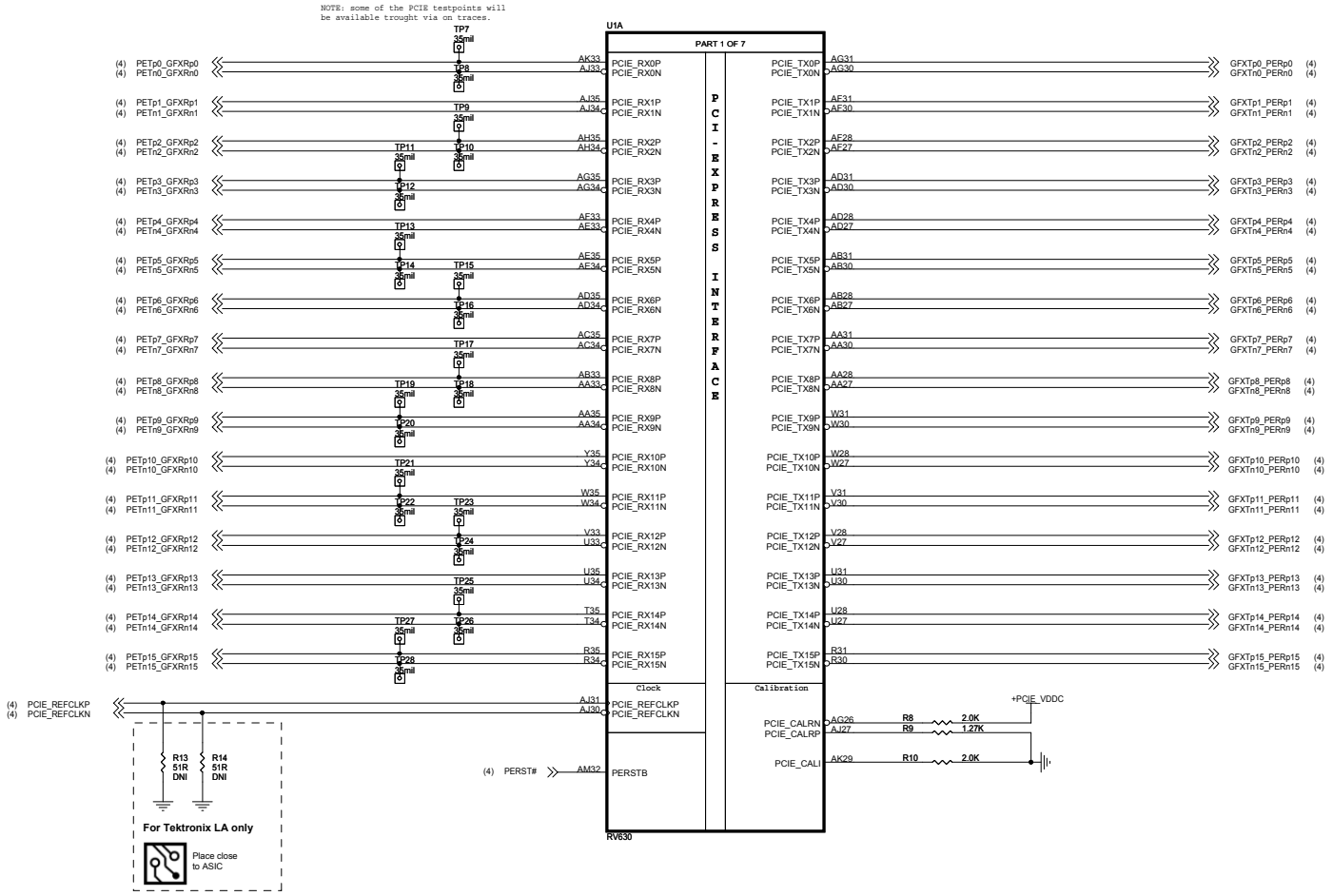

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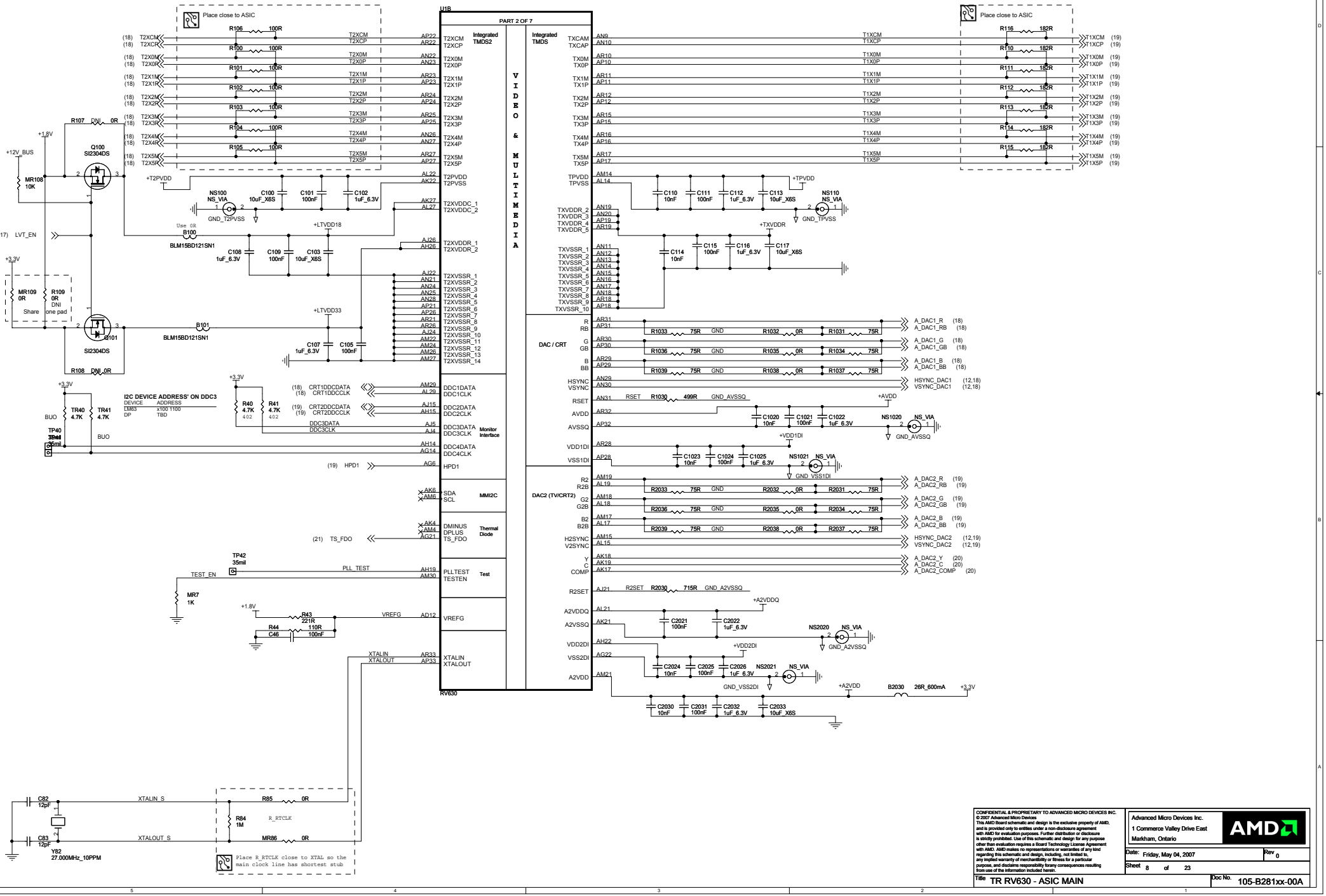
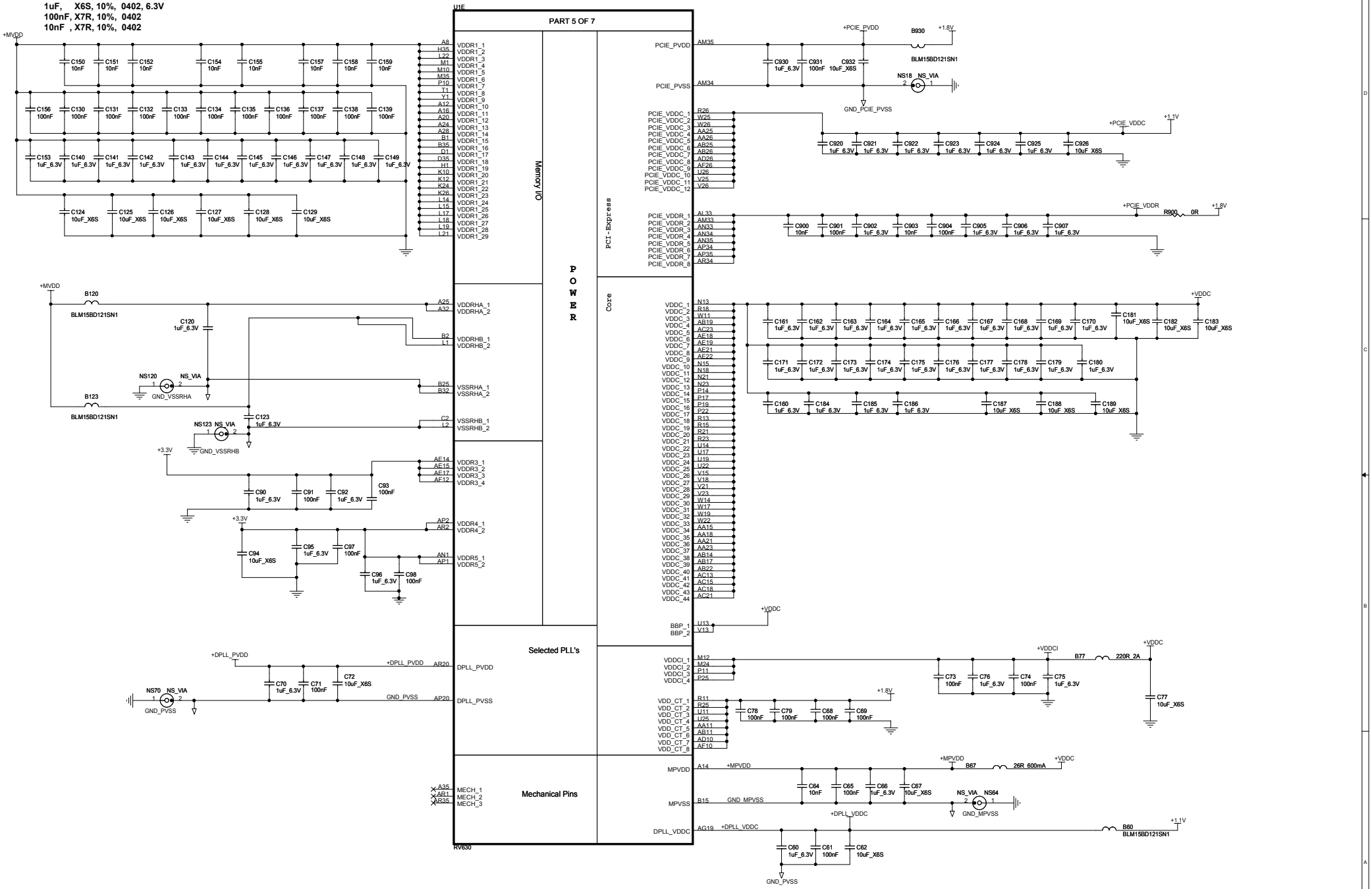
Title RV630 DDR2- ASIC PCIE I/F

Doc No. 105-B281xx-00A

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402



Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402



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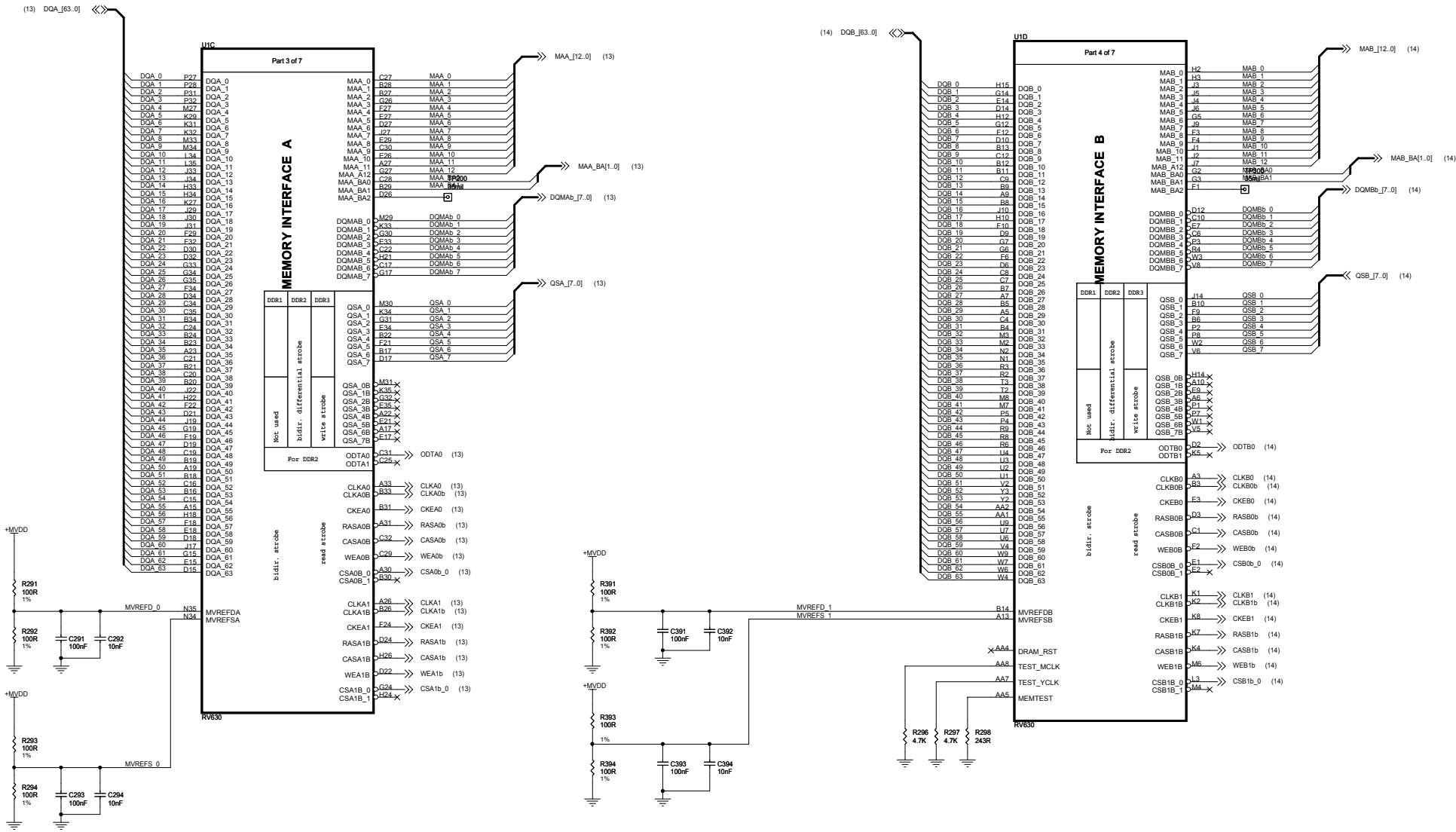
Title RV630 DDR2- ASIC POWERS

Doc No. 105-B281xx-00A



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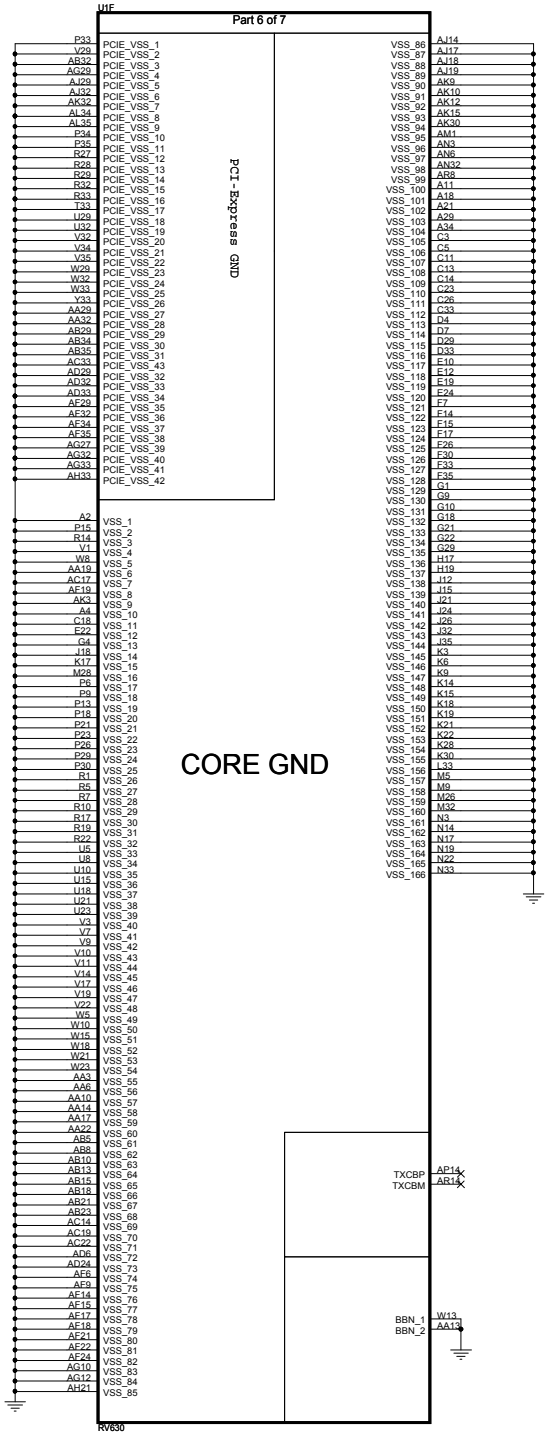
Title RV630 DDR2- ASIC MEM

Doc No. 105-B281xx-00A



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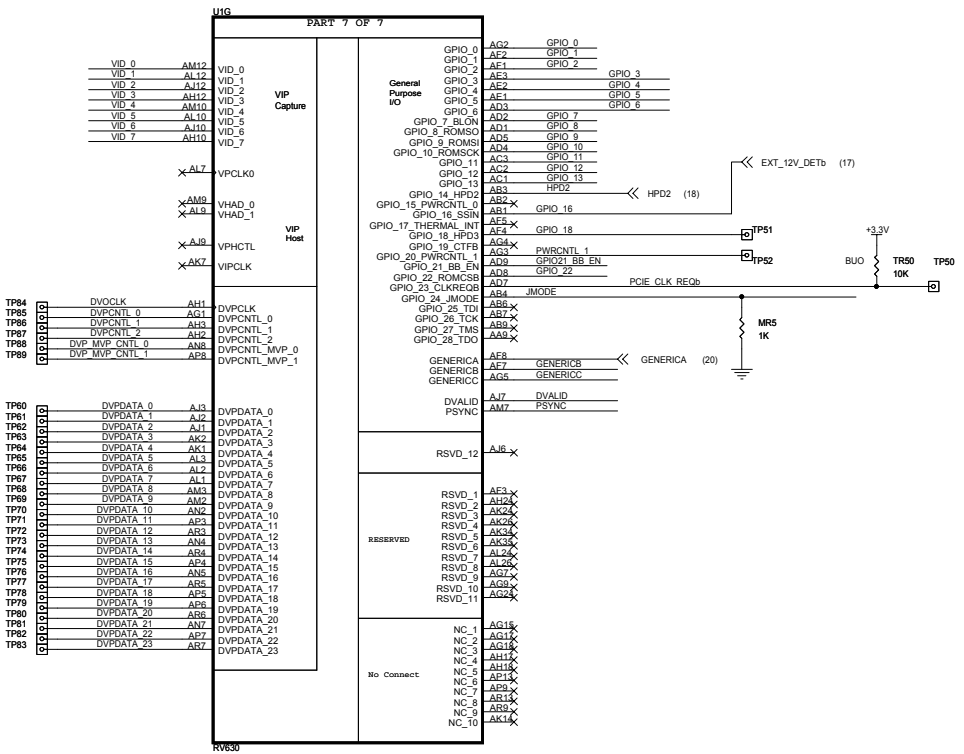
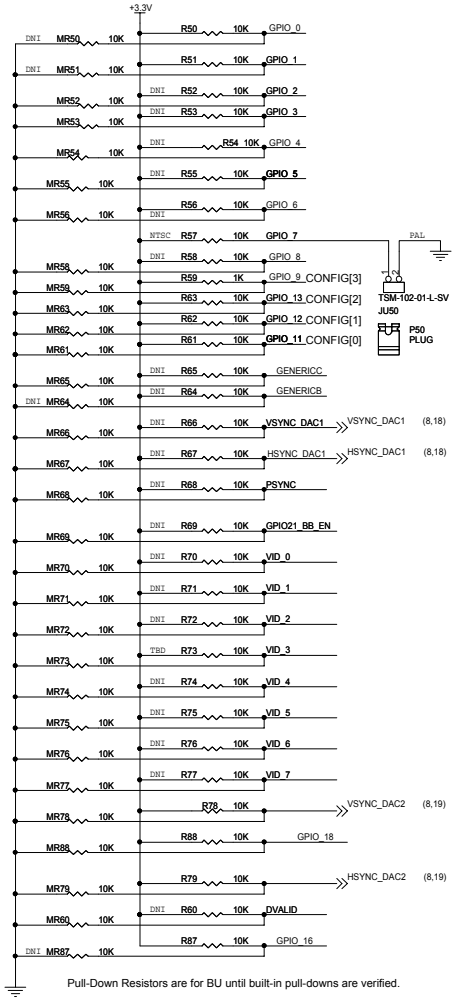
Title RV630 DDR2- ASIC GROUNDS

Doc No. 105-B281xx-00A



PIN BASED STRAPS



GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

ATI Internal Use Only - Reserved (Default: 00)

DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

ATI Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0]
0010 - 512Kbit AT25F512A (Atmel)
0011 - 1Mbit AT25F1024A (Atmel)
0100 - 512Kbit M25P05A (ST)
0101 - 1Mbit M25P10A (ST)
0101 - 2Mbit M25P20 (ST)
0100 - 512Kbit Pm25LV512 (Chingis)
0101 - 1Mbit Pm25LV010 (Chingis)

ATI Internal Use Only - Reserved (Default: 0)

VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

ATI Internal Use Only - Reserved

VGA DISABLE : 1 for disable (set to 0 for normal operation)

ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

MSI_DIS (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

BIF_AUDIO_EN
0 - Disable HD Audio 1- Enable HD Audio

ATI Internal Use Only - Reserved (Default: 0)

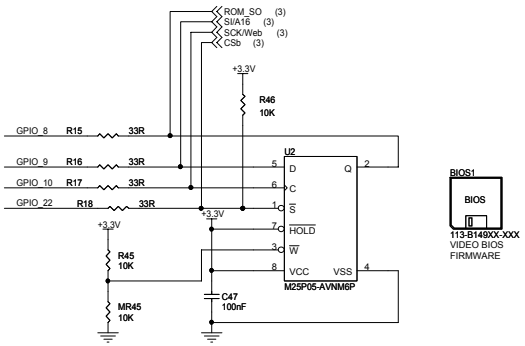
64BAR_EN_A (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

MEMORY CONFIG ATI Board Feature I
VSYNC_DAC2 CHECK ATI MEMORY
GPIO18 TUNING DOCUMENT

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability



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Title	RV630 DDR2- ASIC DVO-BOOT SRAPS
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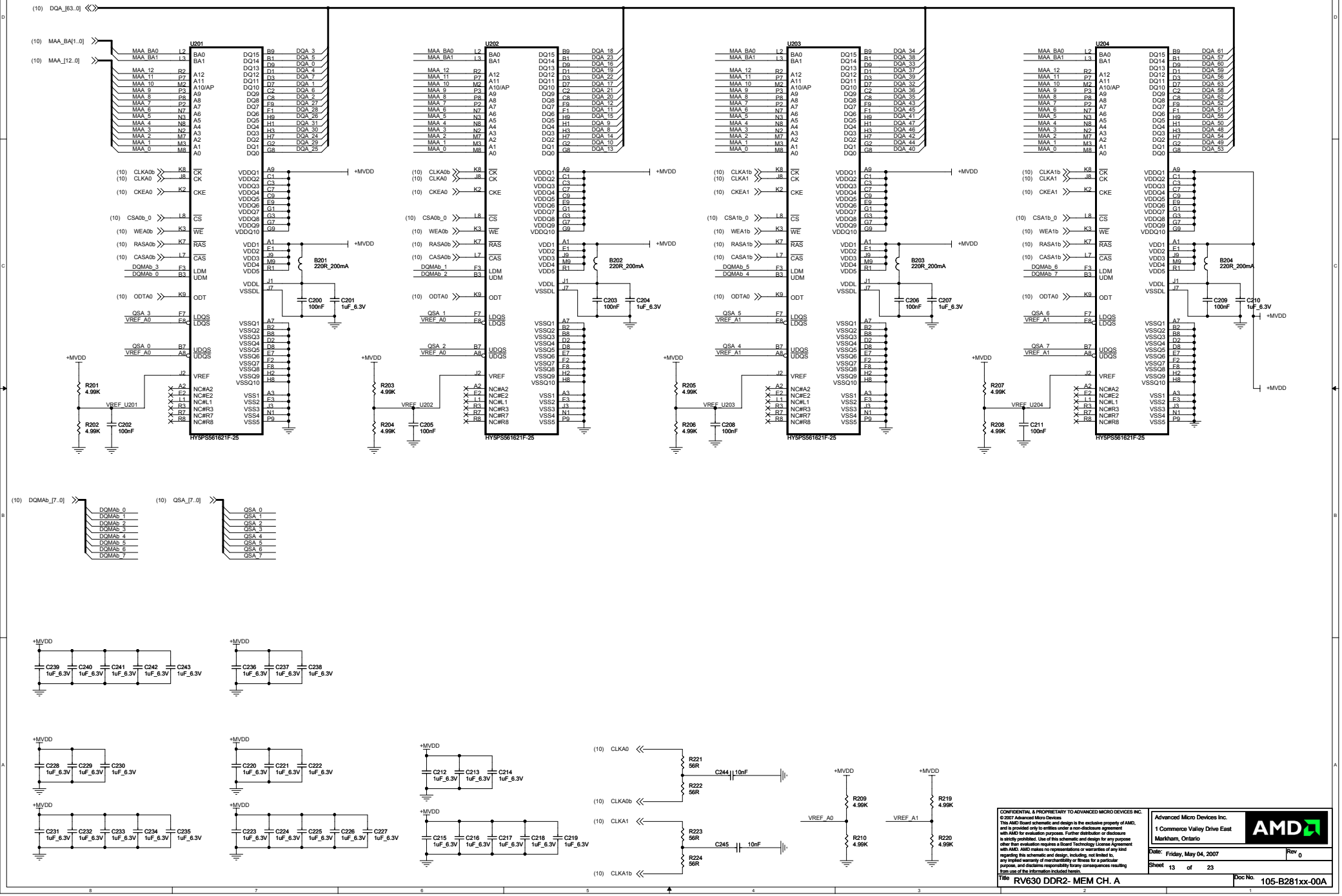
CHANNEL A: 128MB/256MB DDR2



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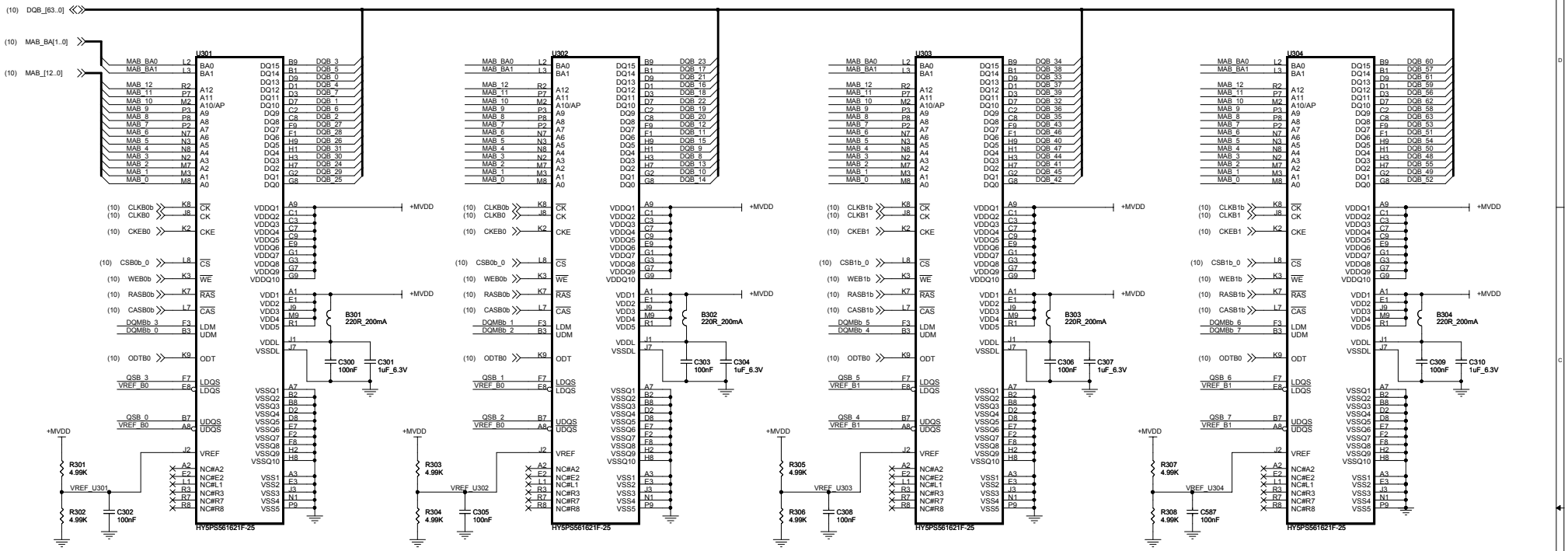
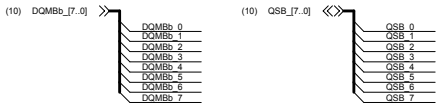
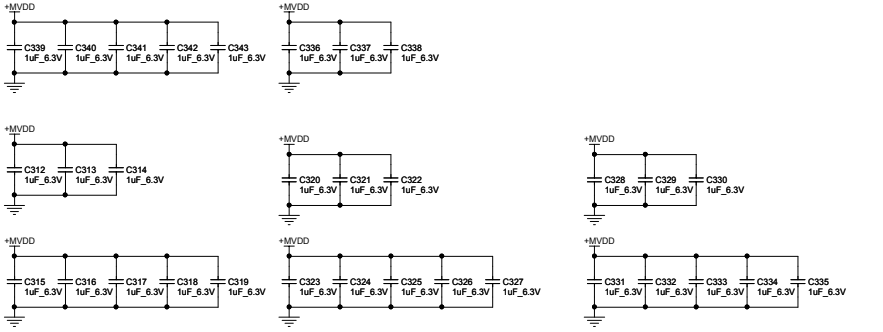
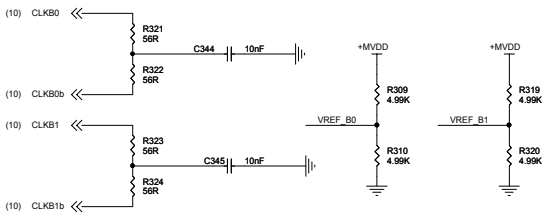
CHANNEL B: 128MB/256MB DDR2









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Title RV630 DDR2- MEM CH. B

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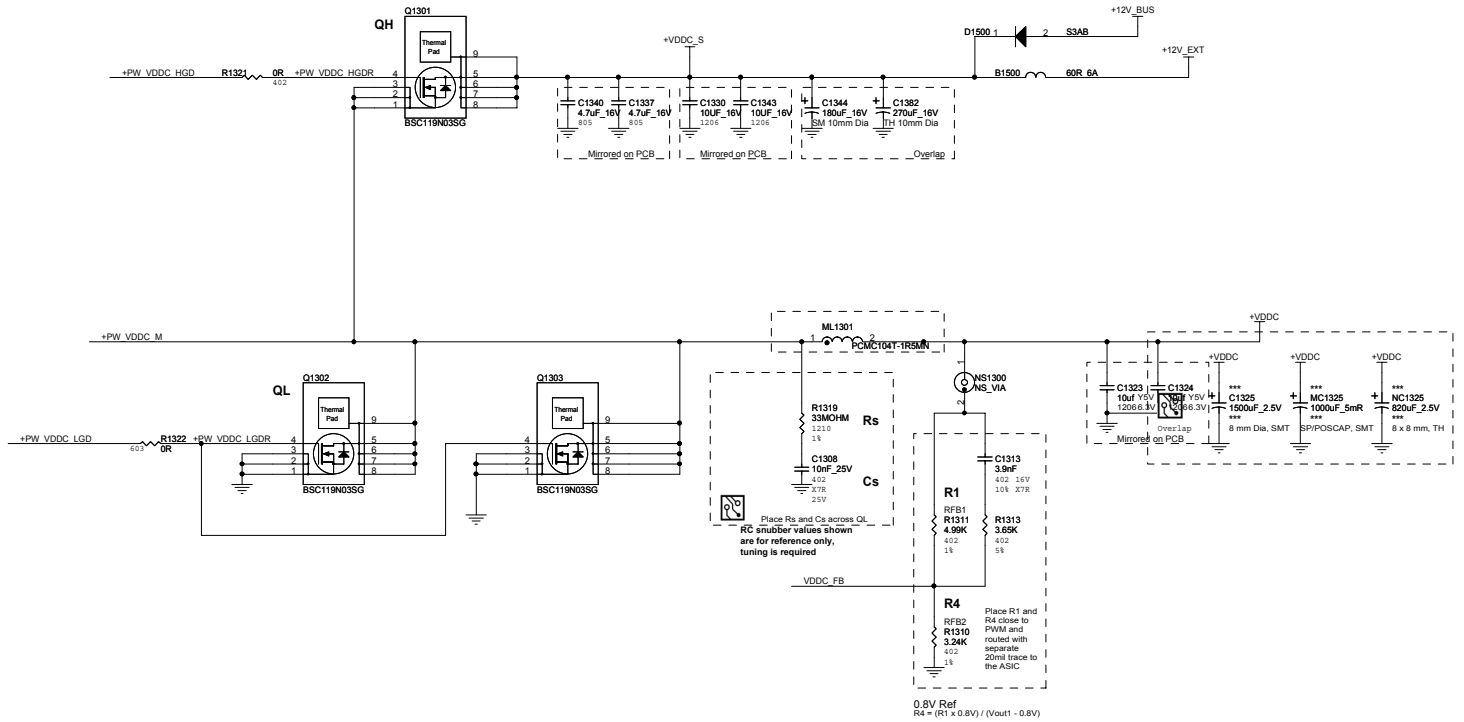
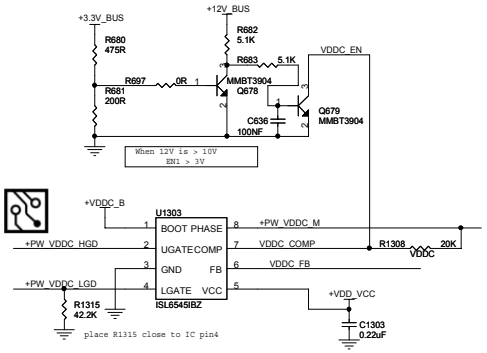
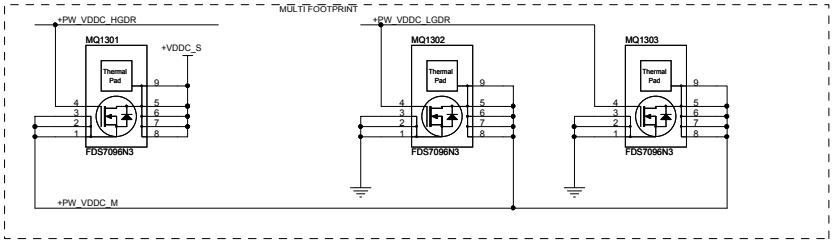






SMPS02- Regulator for VDDC

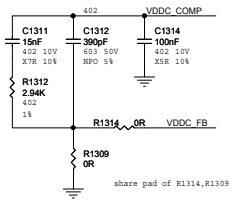
Vout = .9V ~ 1.2V, DEFAULT : 1.2V

	VDDC	RS1	
0.6V Ref	1.2V	10K, 1% ATI # 31600100200G	10K, 1% ATI # 31600100200G

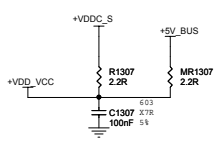
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

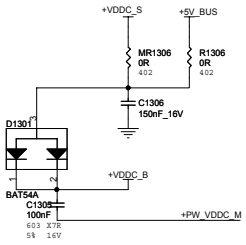
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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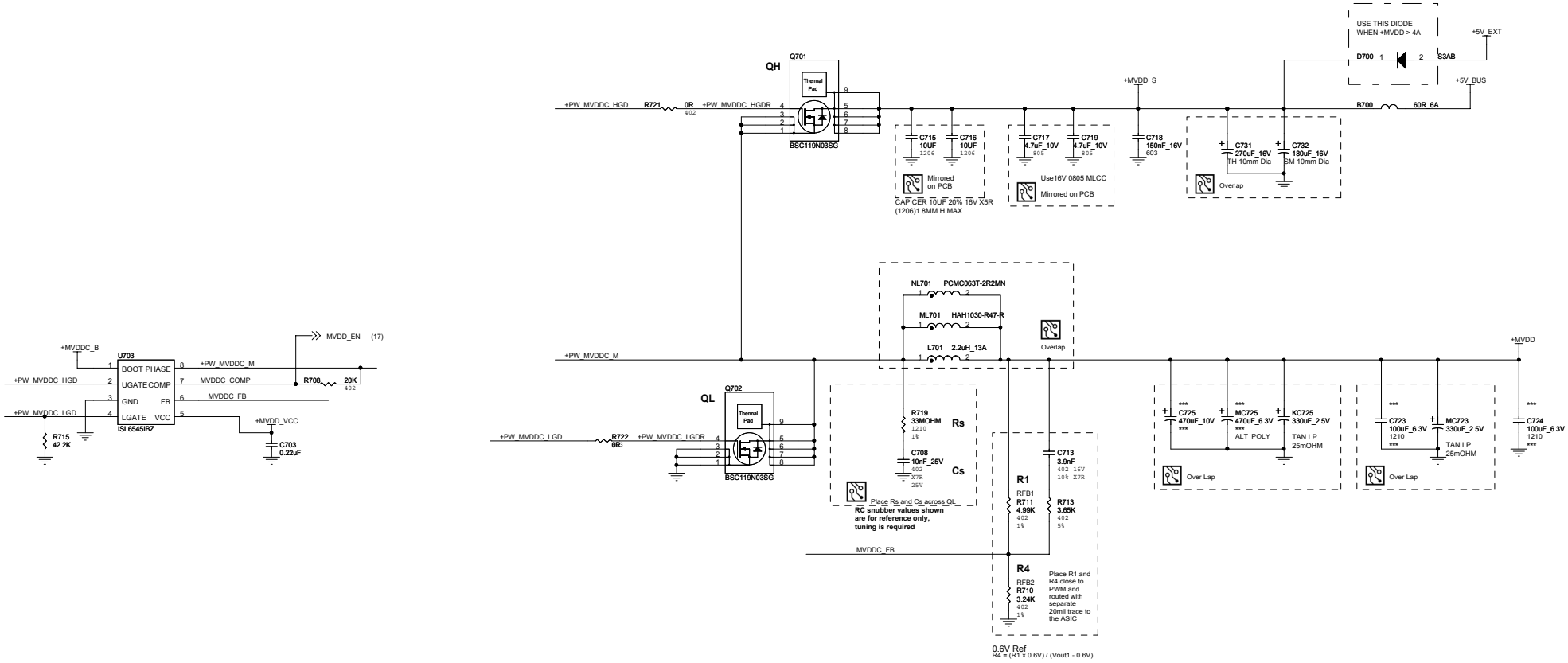
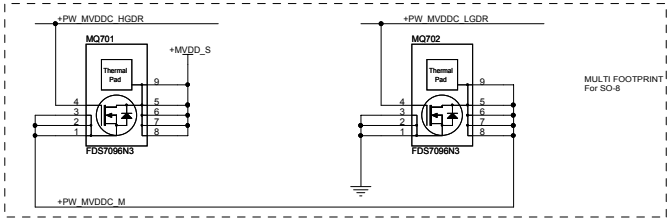
Title	TR RV630 - MVDD SMPS02
Doc No.	105-B281xx-00A





SMPS02- Regulator for MVDD

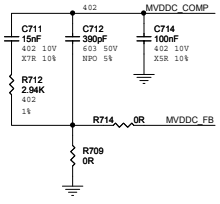
Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.6V Ref	1.8V (1.98V~2.08V)	10K p/n 3160100200G	4.99K p/n 3160499100G

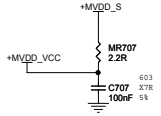
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

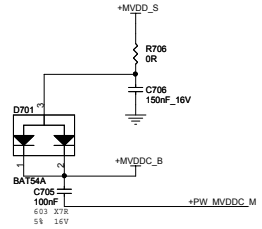
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



Layout guideline for Nexsem NX2114/2307

1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

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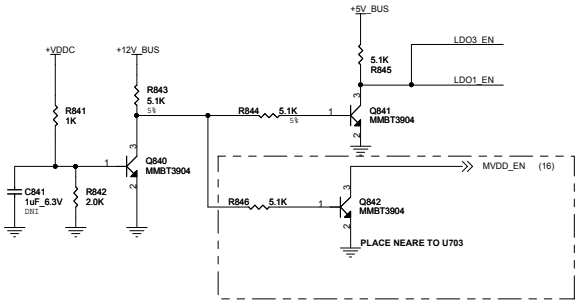
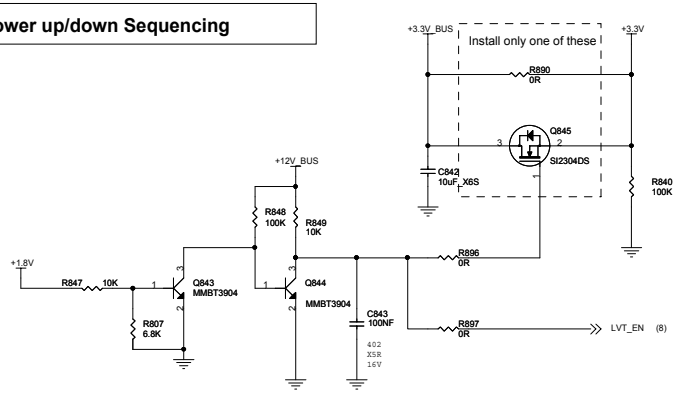
Title TR RV630 - MVDD SMPS02

Doc No. 105-B281xx-00A

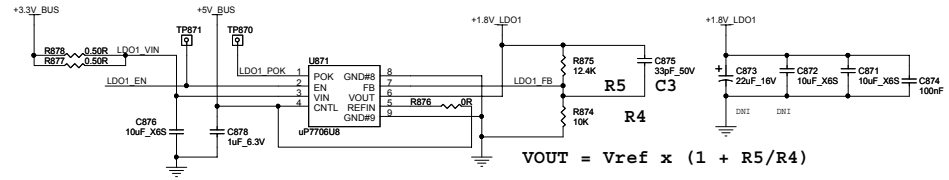
Power up/down Sequencing





LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX

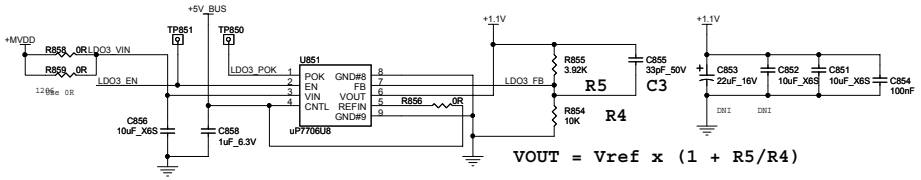
PCB: 50 to 70mm sq. copper area for cooling



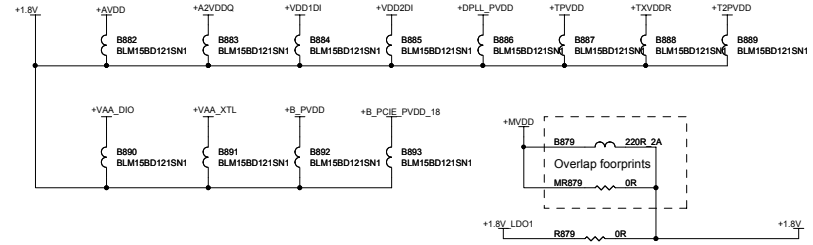
DELETE LDO2

LDO #3: Vin = +1.45V to 2.1VMAX Vout = +1.1V +/- 2% Iout = 1.1A (TBV) RMS MAX

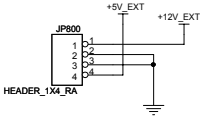
PCB: 50 to 70mm sq. copper area for cooling

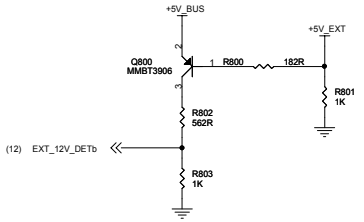


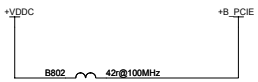
Shared Power Rails



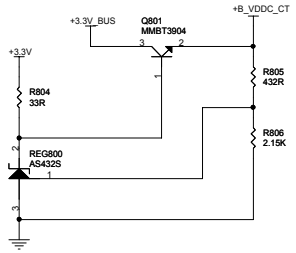
EXTERNAL CONNECTOR FOR AGP DESIGN







+B_VDDC_CT = +1.5V @ 80 mA



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Title TR RV630 - Linear Regulators

Doc No. 105-B281xx-00A

See BOM for qualified filters

(8) A_DAC1_R — R1001 75R — C1004 8.0pF — L1001 68nH_300mA — R1024 0R — A_R_DAC1_M — C1001 12pF_50V — L1004 36NH

(8) A_DAC1_RB — R1027 37.4R

(8) A_DAC1_G — R1002 75R — C1005 8.0pF — L1002 68nH_300mA — R1025 0R — A_G_DAC1_M — C1002 12pF_50V — L1005 36NH

(8) A_DAC1_GB — R1028 37.4R

(8) A_DAC1_B — R1003 75R — C1006 8.0pF — L1003 68nH_300mA — R1026 0R — A_B_DAC1_M — C1003 12pF_50V — L1006 36NH

(8) A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

For ESD Protection

+3.3V — D1001 CM1213-04 — +5V_BUS — D1002 CM1213-04

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

+5V_BUS — MJ1001 G3179C219-005

1	R	
2	G	
3	B	
11	MS0	DDC2_MONID0
12	MS1	DDC2_MONID1(SDA)
4	MS2	DDC2_MONID2
15	MS3	DDC2_MONID3(SCL)
9	NC	
13	HS	
14	VS	
5	VSS	
6	VSS#6	
7	VSS#7	
8	VSS#8	
10	VSS#10	
16	CASE	
17	CASE#17	

C1010 68pF 603

(8) CRT1DDCDATA — +3.3V — R1004 10K — +5V_BUS — R1005 2.2K — Q1001 BSH111 — DDCDATA_DAC1_5V — R1006 33R — DDCDATA_DAC1_R

(8) CRT1DDCCLK — +3.3V — R1007 10K — +5V_BUS — R1008 2.2K — Q1002 BSH111 — DDCCLK_DAC1_5V — R1009 33R — DDCCLK_DAC1_R

C1999 100nF — +5V_BUS — U1999A 74VHC125 — U1999B 74VHC125

(8,12) HSYNC_DAC1 — HSYNC_DAC1_B — R1010 10R — HSYNC_DAC1_R

(8,12) VSYNC_DAC1 — VSYNC_DAC1_B — R1011 10R — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

+3.3V — Q1021 MMBT3904 — R1022 10K — HPD_DVI2 — (12) HPD2 — R1023 10K

+5V_BUS — J1001 DVI_CONNECTOR

(8) T2X2M	1	TMDS Data2-
(8) T2X2P	2	TMDS Data2+
	3	TMDS Data2/4 Shield
(8) T2X4M	4	TMDS Data4-
(8) T2X4P	5	TMDS Data4+
DDCCLK_DAC1_R	6	DDC Clock
DDCDATA_DAC1_R	7	DDC Data
VSYNC_DAC1_R	8	Analog VSYNC
(8) T2X1M	9	TMDS Data1-
(8) T2X1P	10	TMDS Data1+
	11	TMDS Data1/3 Shield
(8) T2X3M	12	TMDS Data3-
(8) T2X3P	13	TMDS Data3+
	14	+5V Power
	15	GND (for +5V)
HPD_DVI2	16	Hot Plug Detect
(8) T2X0M	17	TMDS Data0-
(8) T2X0P	18	TMDS Data0+
	19	TMDS Data0/5 Shield
(8) T2X5M	20	TMDS Data5-
(8) T2X5P	21	TMDS Data5+
	22	TMDS Clock Shield
(8) T2XCP	23	TMDS Clock+
(8) T2XCM	24	TMDS Clock-
A_R_DAC1_F	C1	Analog Red
A_G_DAC1_F	C2	Analog Green
A_B_DAC1_F	C3	Analog Blue
HSYNC_DAC1_R	C4	Analog HYNC
	C5	Analog GND
	C6	Analog GND#C6
	26	CASE#26
	27	CASE#27
	28	CASE#28
	29	CASE#29
	30	CASE#30
	25	CASE

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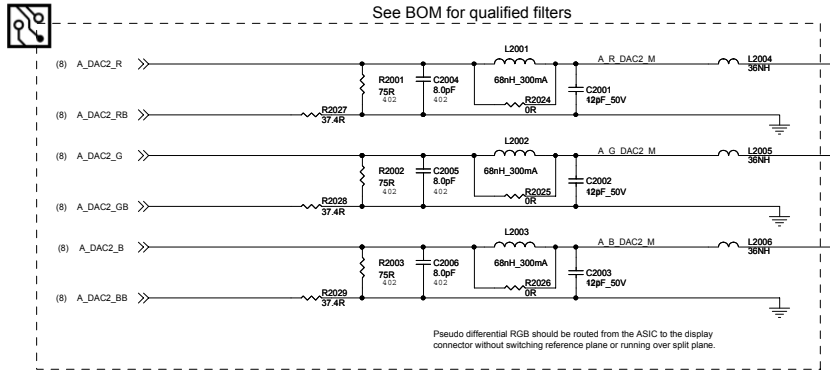
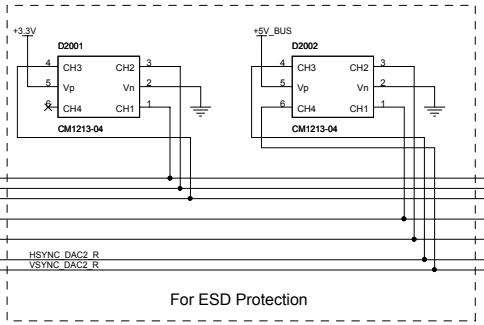
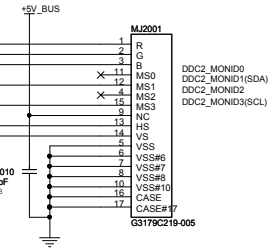
Title RV630 DDR2- DAC1&TMDS2

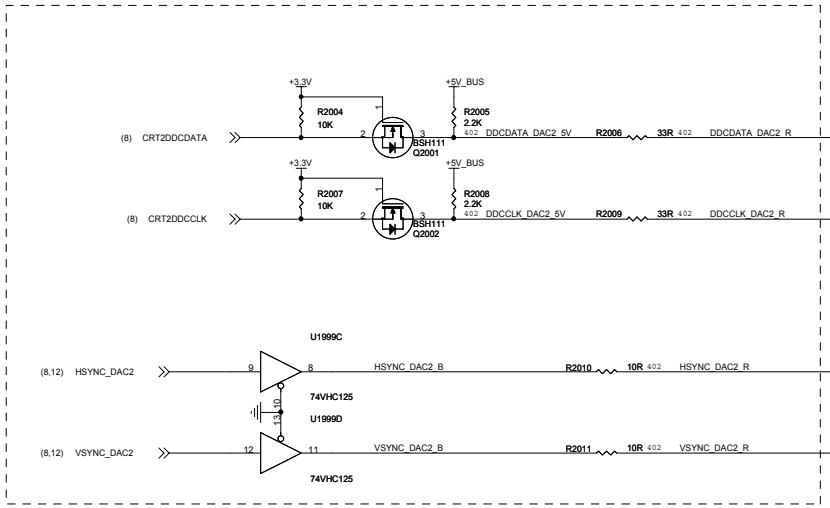
Doc No. 105-B281xx-00A

See BOM for qualified filters



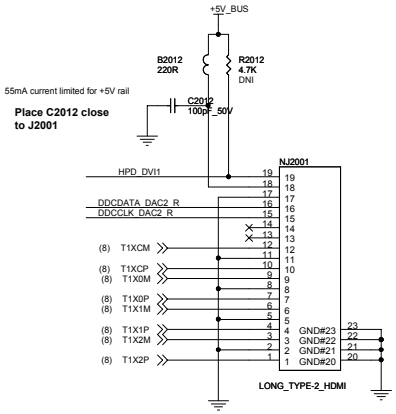


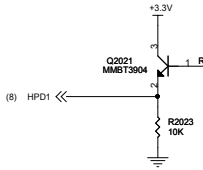


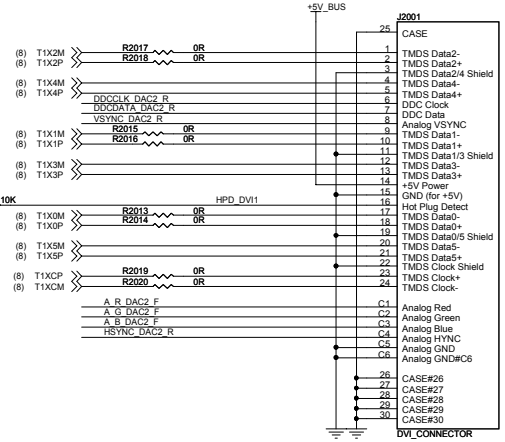


DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V	+5V	+5V	
	Mechanical Key	50mA min	50mA min	300mA min	Optional
Hardware Support	No	1A max Yes	1A max Yes	1A max No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997







NOTE: J2002, MJ2001, NJ2001 SHOULD BE PLACED SUCH THAT WE CAN USE EITHER ONE OF THEM FOR SEPERATE BOM SKU

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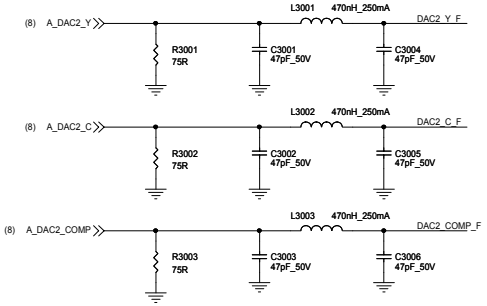
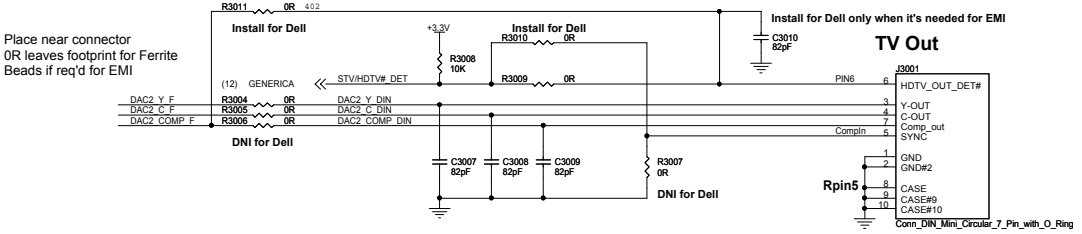
Title RV630 DDR2-DAC2/TMDS1

Doc No. 105-B281xx-00A





The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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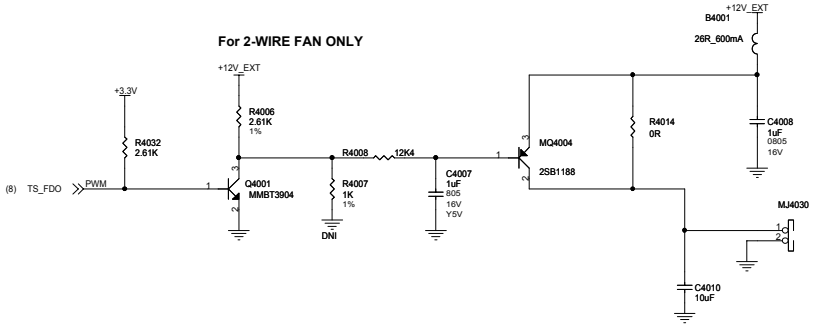
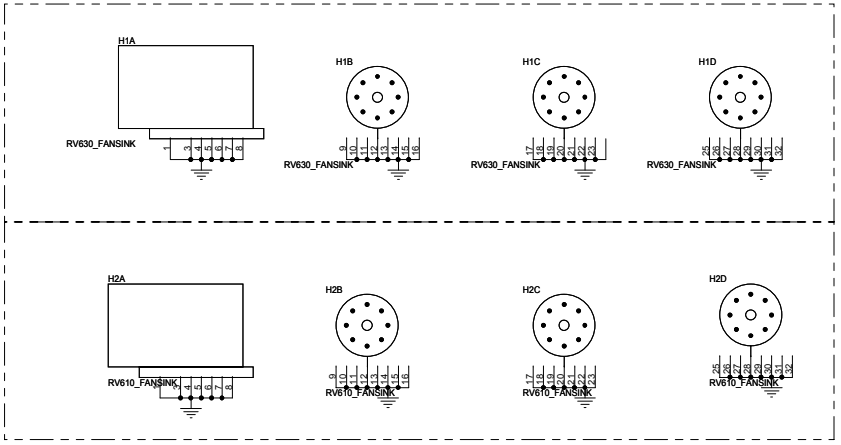
Title RV630 DDR2 - TVO

Doc No. 105-B281xx-00A





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Title RV630 DDR2-THERMAL MANAGEMENT

Doc No. 105-B281xx-00A

DVI/DVI SCREWS with top tab

ASSY-SCREW1

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT

ASSY-SCREW2

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT

ASSY-SCREW3

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT

ASSY-SCREW4

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY-SCREW

ASSY1

ANTISTATIC
BAG

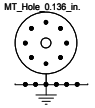
6_X_11

ASSY2

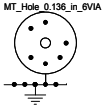
BRACKET

8020038600G

MT1
MT_Hole_0.136_in.



MT2
MT_Hole_0.136_in_6VIA

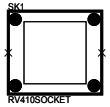


PCB1

PCB

109-B14931-00C

SK1



RV410SOCKET

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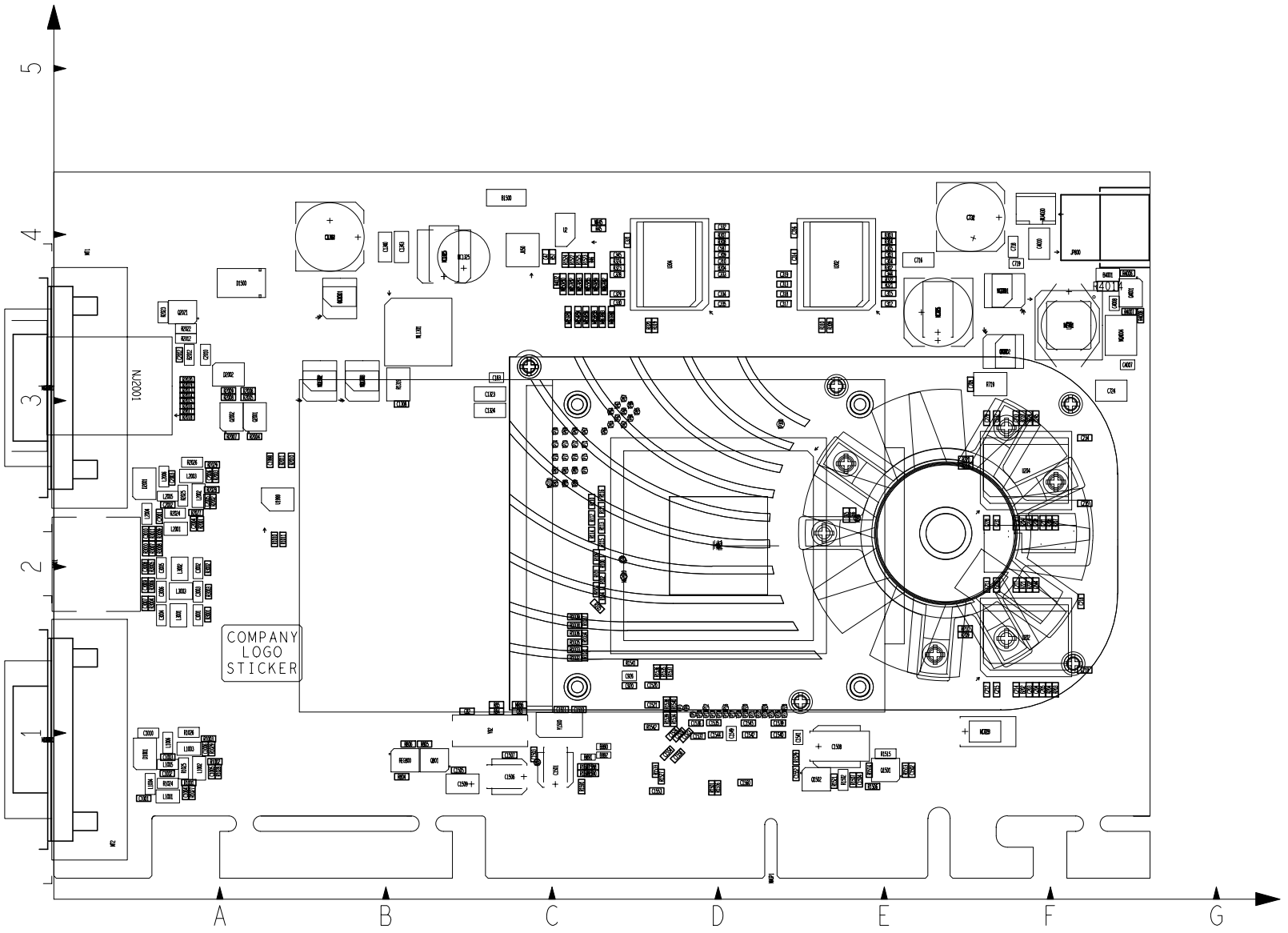
Title RV630 DDR2-MECHANICAL

Doc No. 105-B281xx-00A



AMD ADVANCED MICRO DEVICES PCBCAD GROUP	RH RV630 DDR2 Sefadu AGP P/N 109-B28131-00A April 30, 2007 Subcontractor ASSEMBLY TOP SHEET 1 OF 2

ADVANCED MICRO DEVICES PCBCAD GROUP	RH RV630 DDR2 Setadu AGP P/N 109-BS8131-00A April 30, 2007 Subcontractor

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