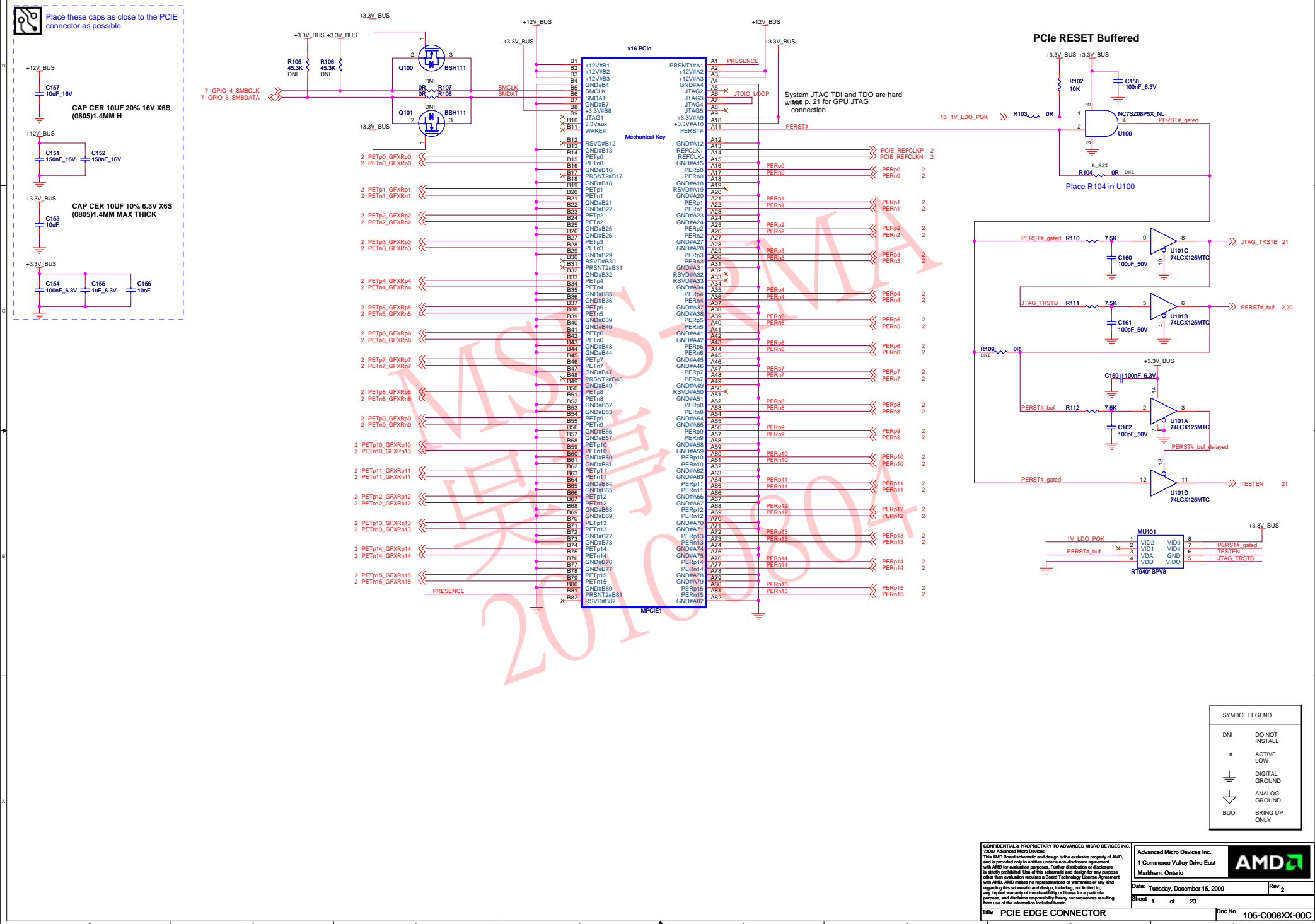
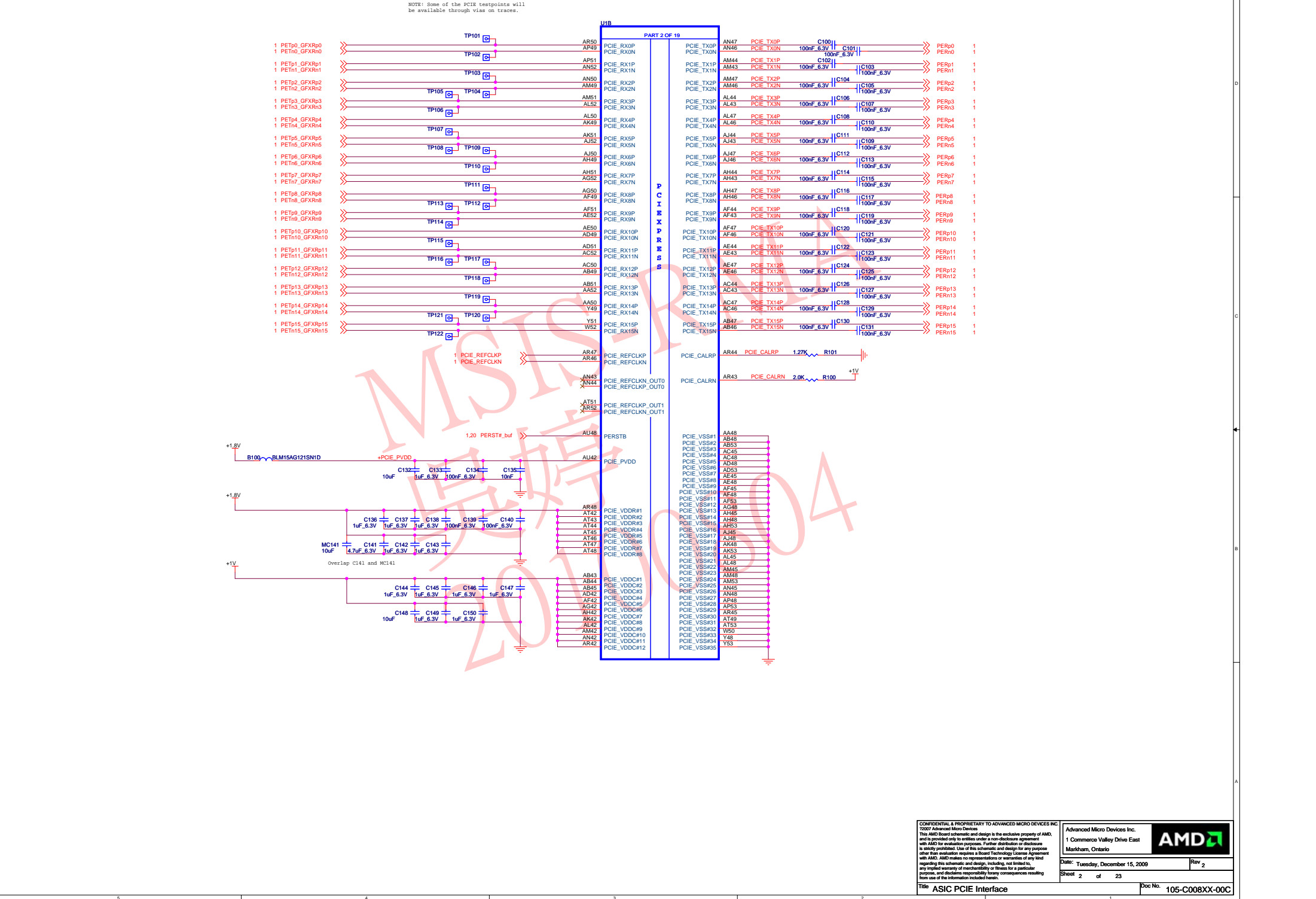


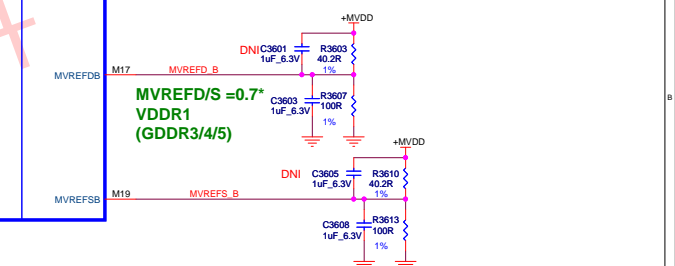
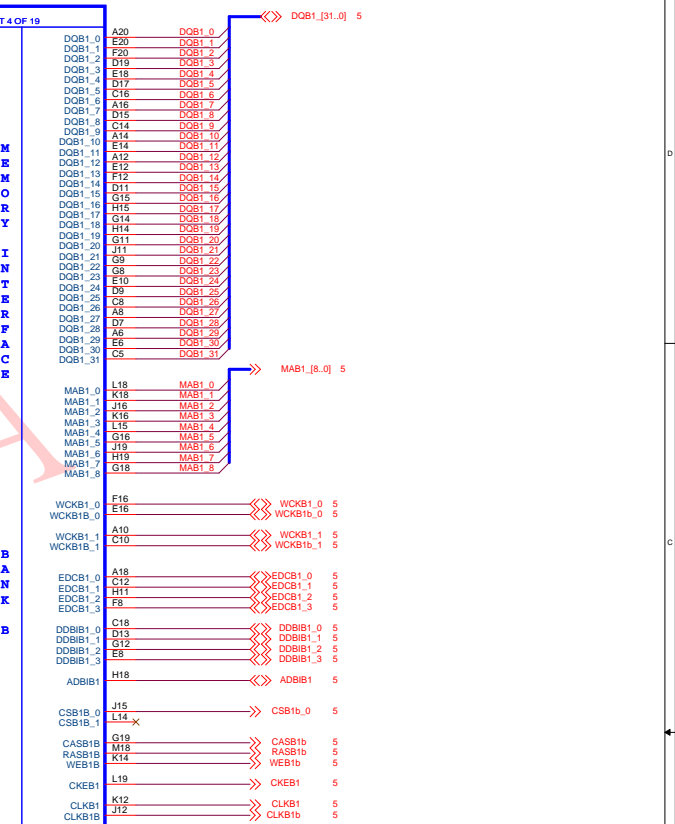
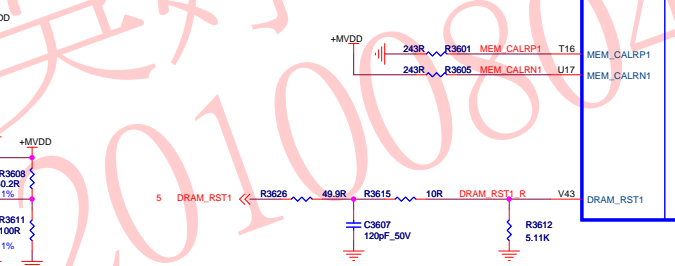
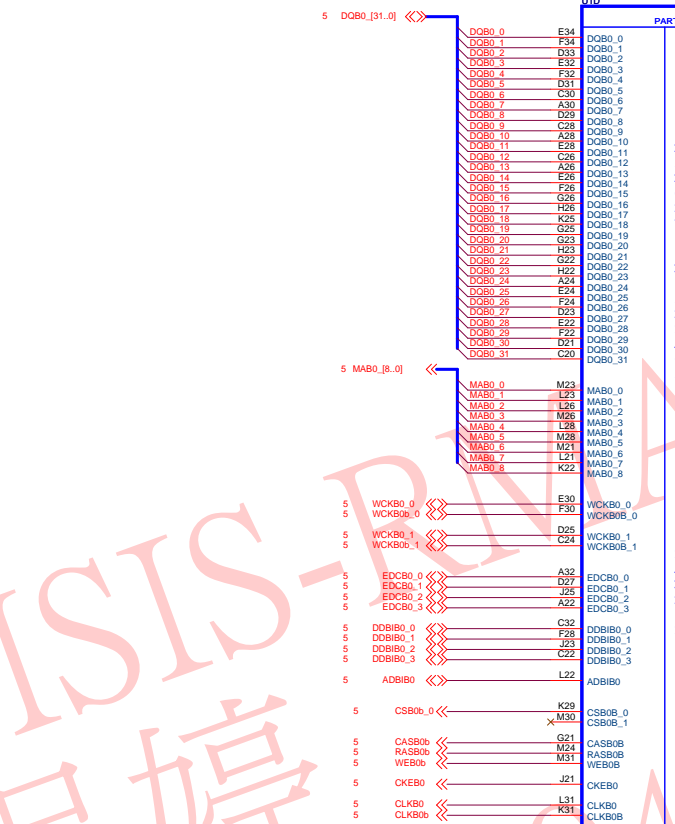
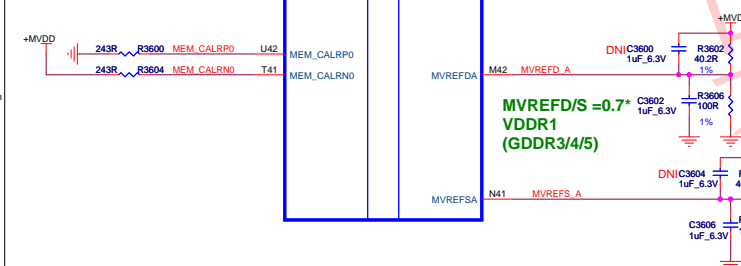
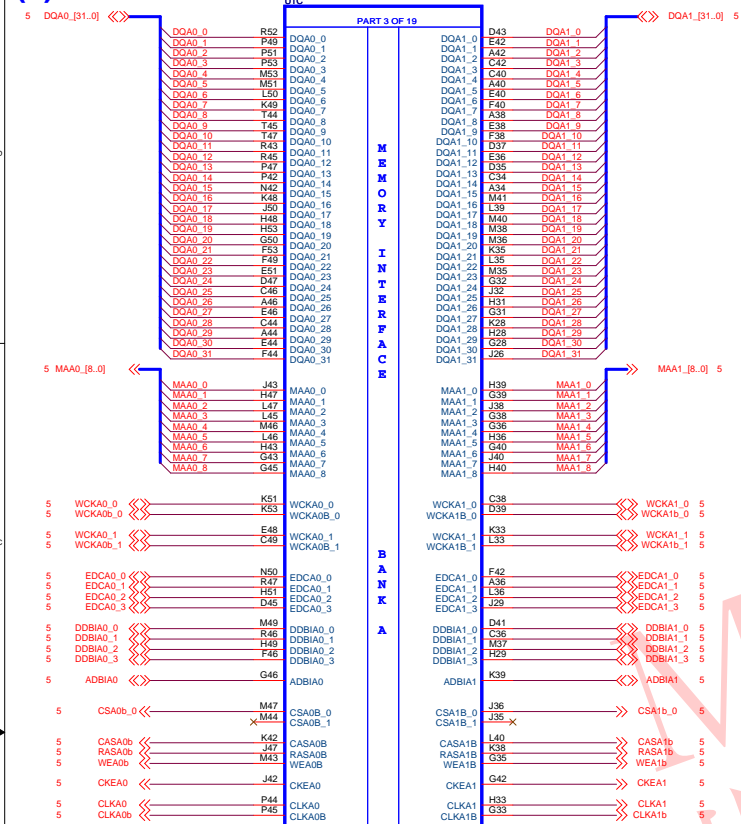
PCI-EXPRESS EDGE CONNECTOR



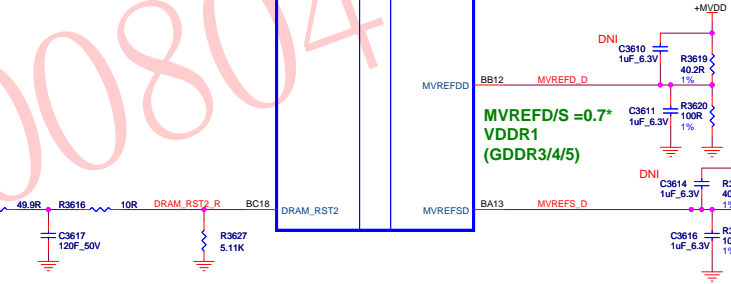
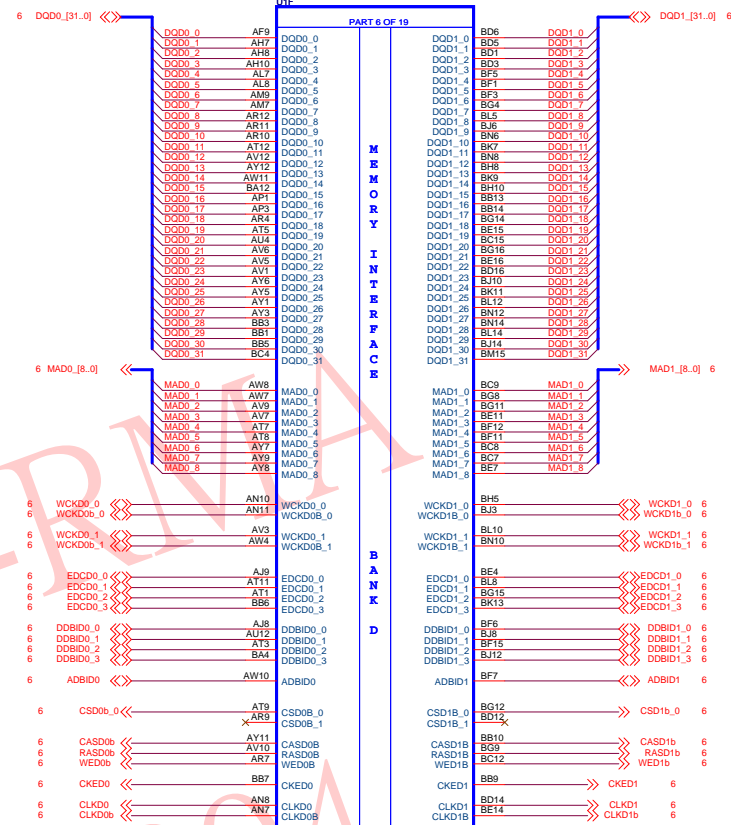
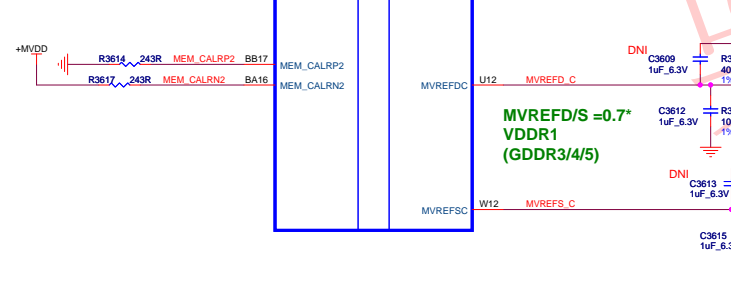
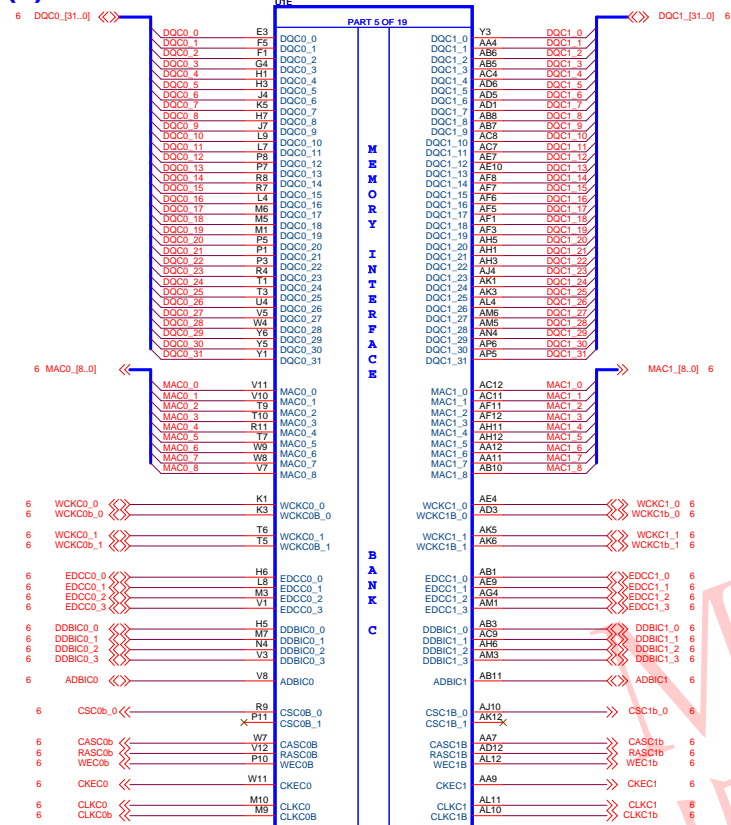
(2) CYPRESS PCIE Interface



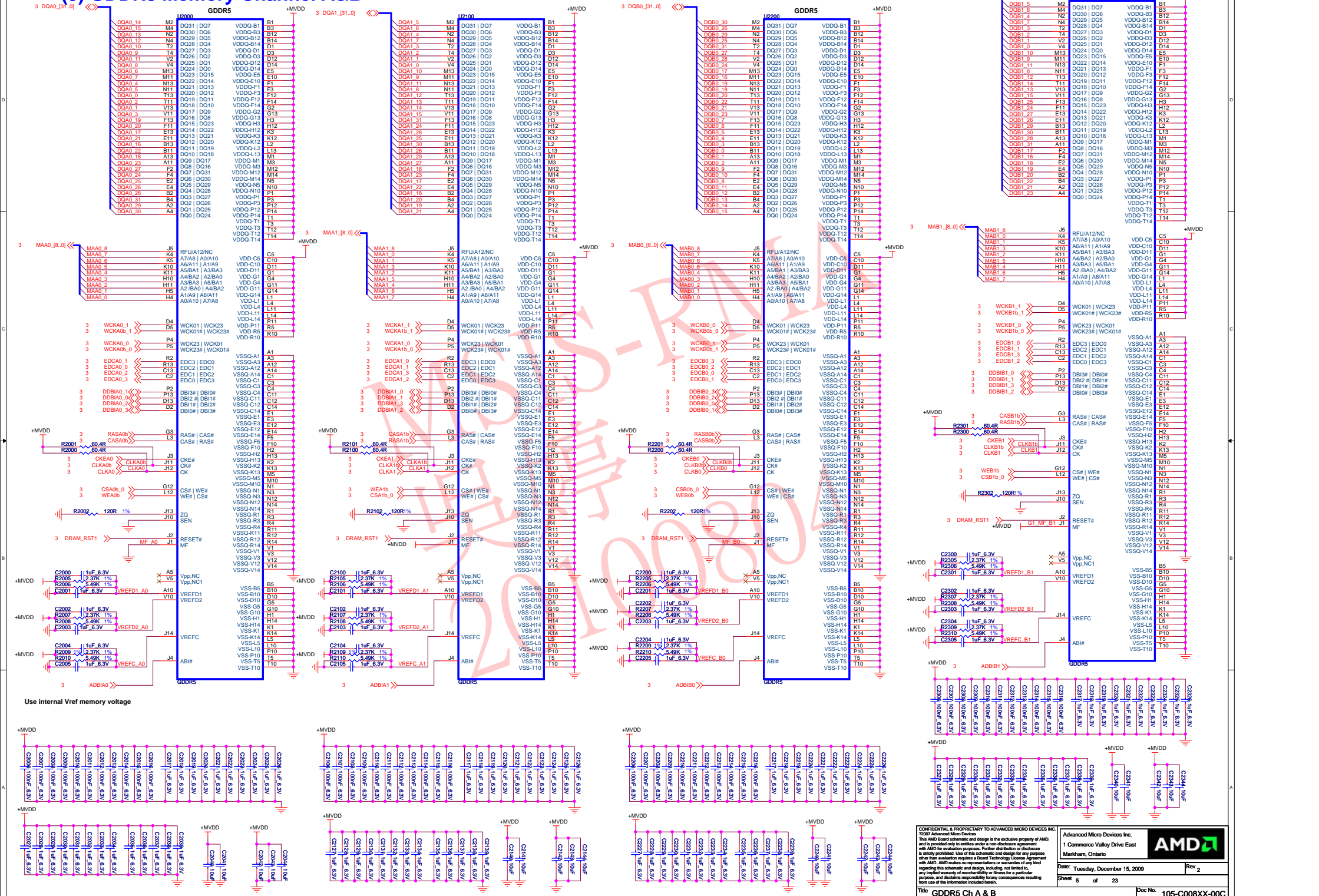
(3) CYPRESS MEM Interface Ch A&B



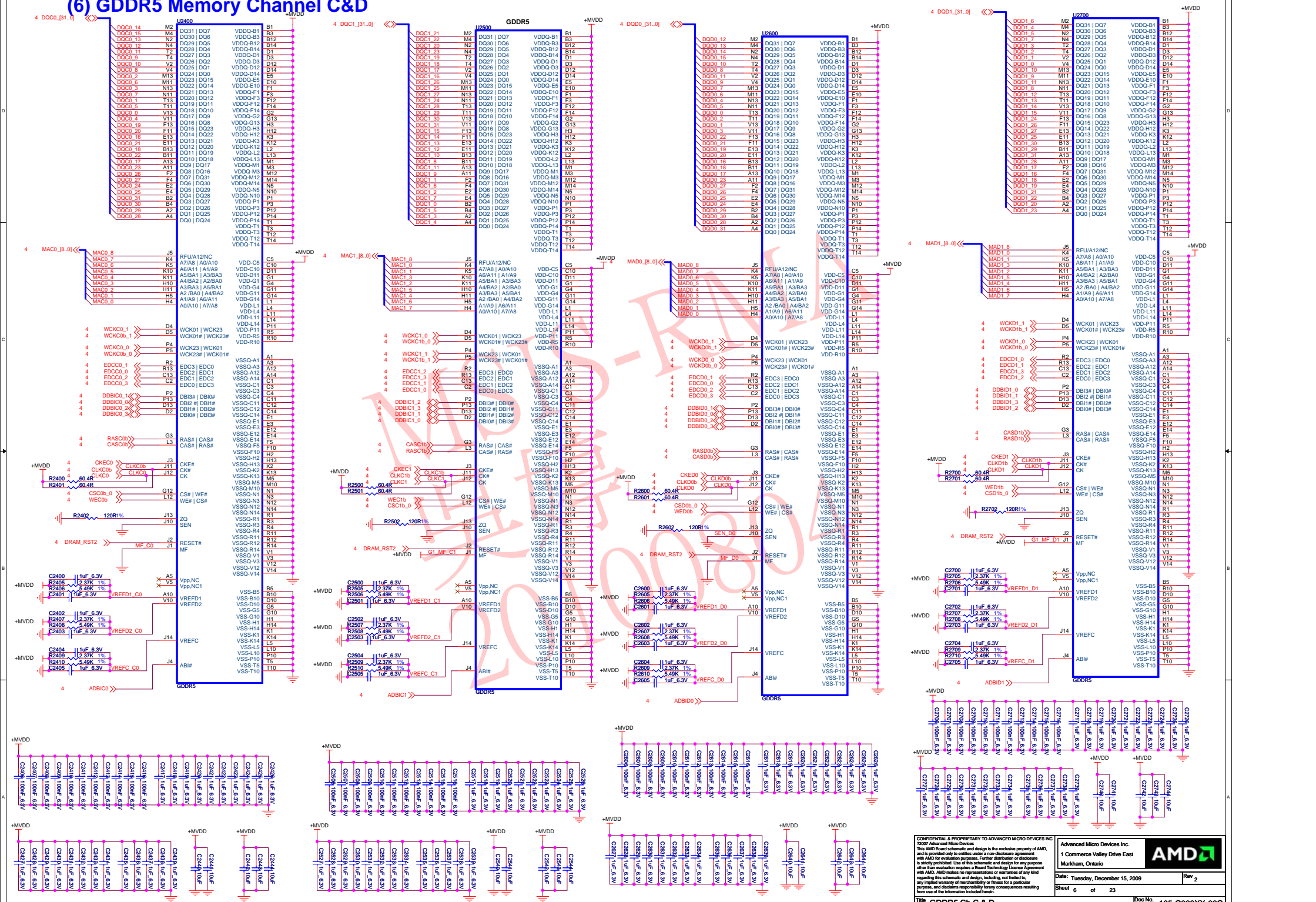
(4) CYPRESS MEM Interface Ch C&D



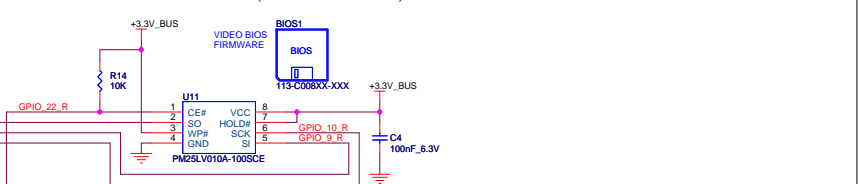
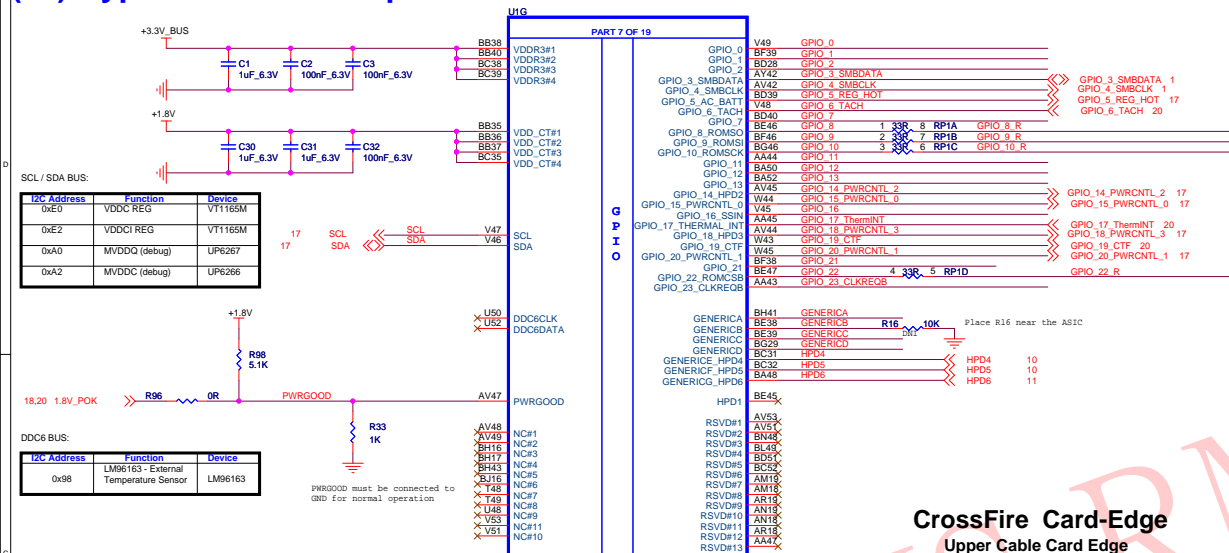
(5) GDDR5 Memory Channel A&B



(6) GDDR5 Memory Channel C&D



(07) Cypress GPIOs Strap CF XTAL OSC

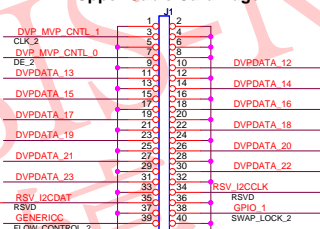


PIN BASED STRAPS

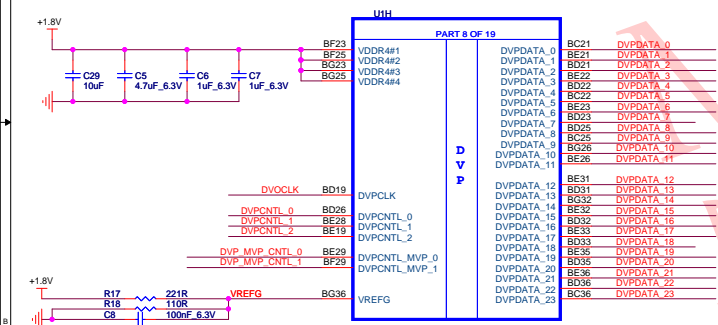
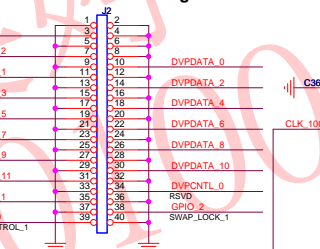



CrossFire Card-Edge


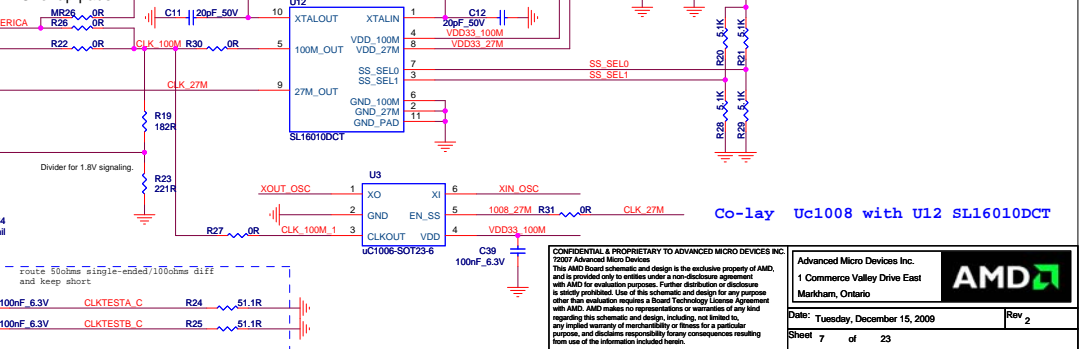
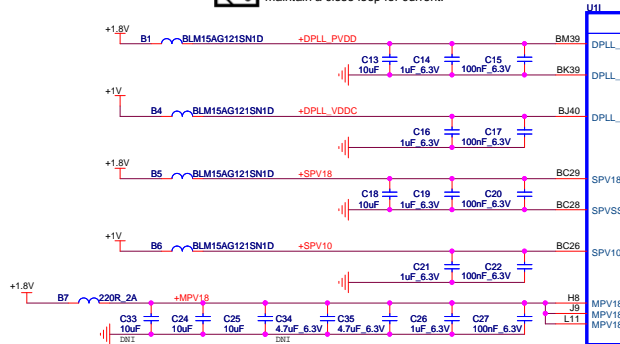
Upper Cable Card Edge



Lower Cable Card Edge




 Place the crossfire testpoints near the ASIC and not the connector

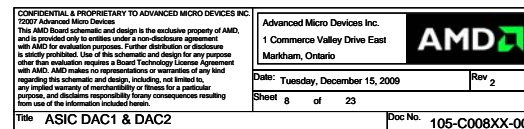
 Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

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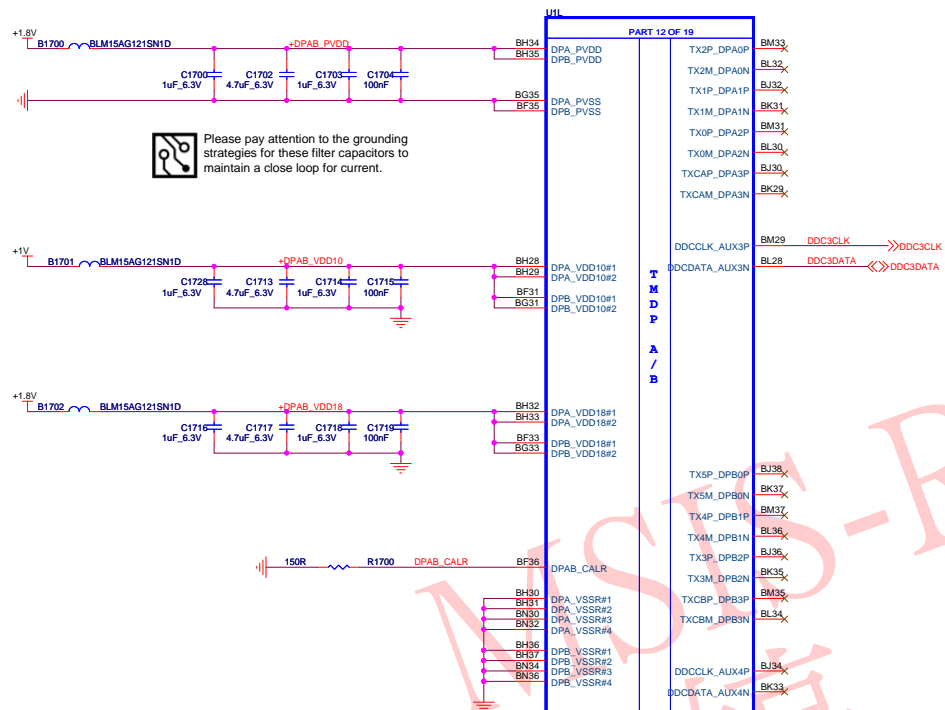
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Date: Tuesday, December 15, 2009		Rev 2	
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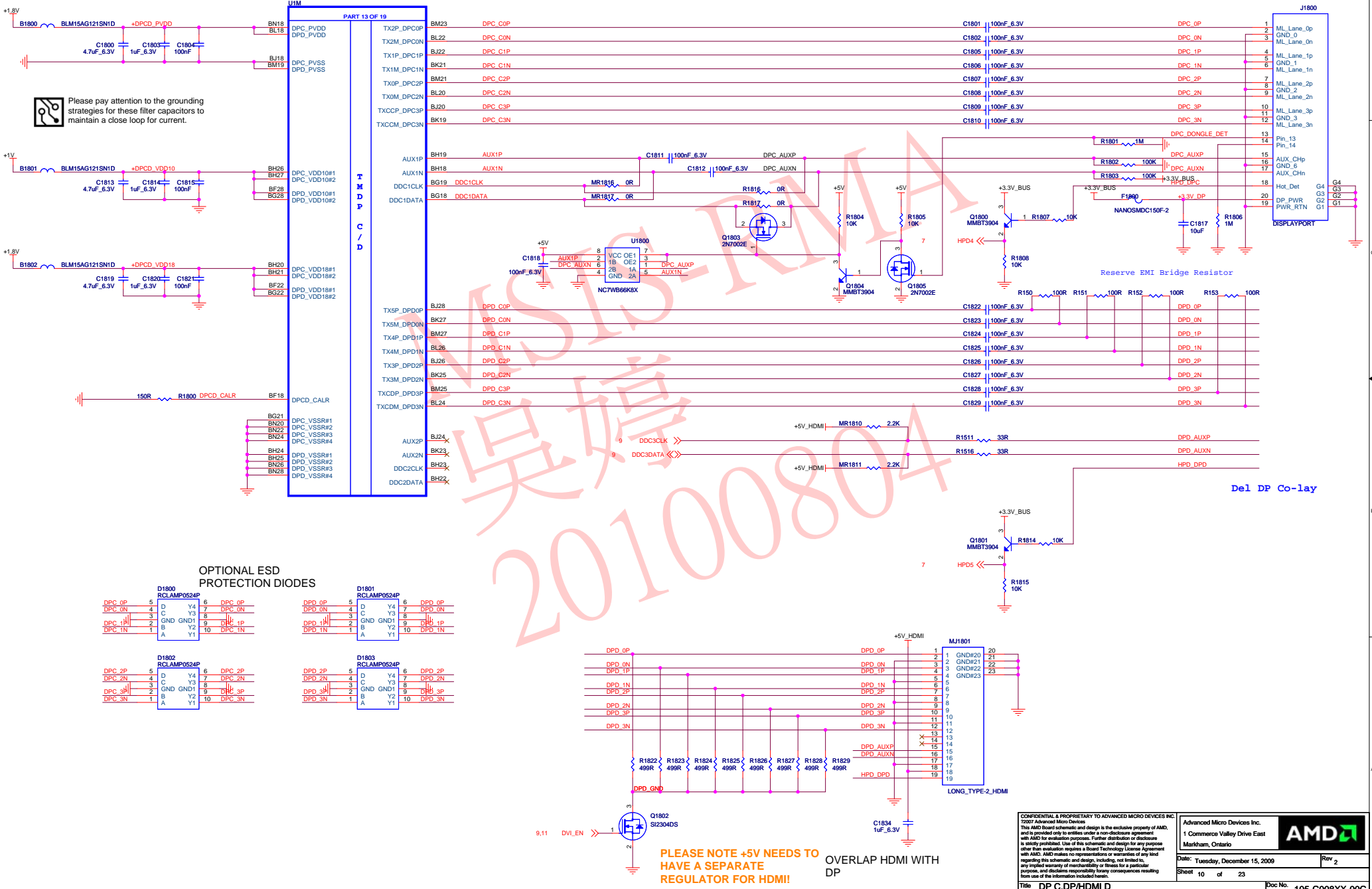
Del Optional ECD protection DIODES



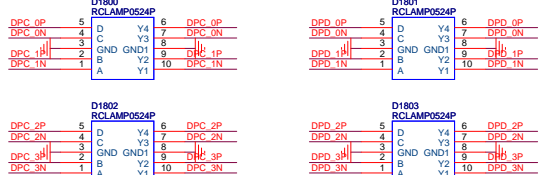
(09) CYPRESS TMD5 A&B



(10) CYPRESS Display Port/HDMI C&D



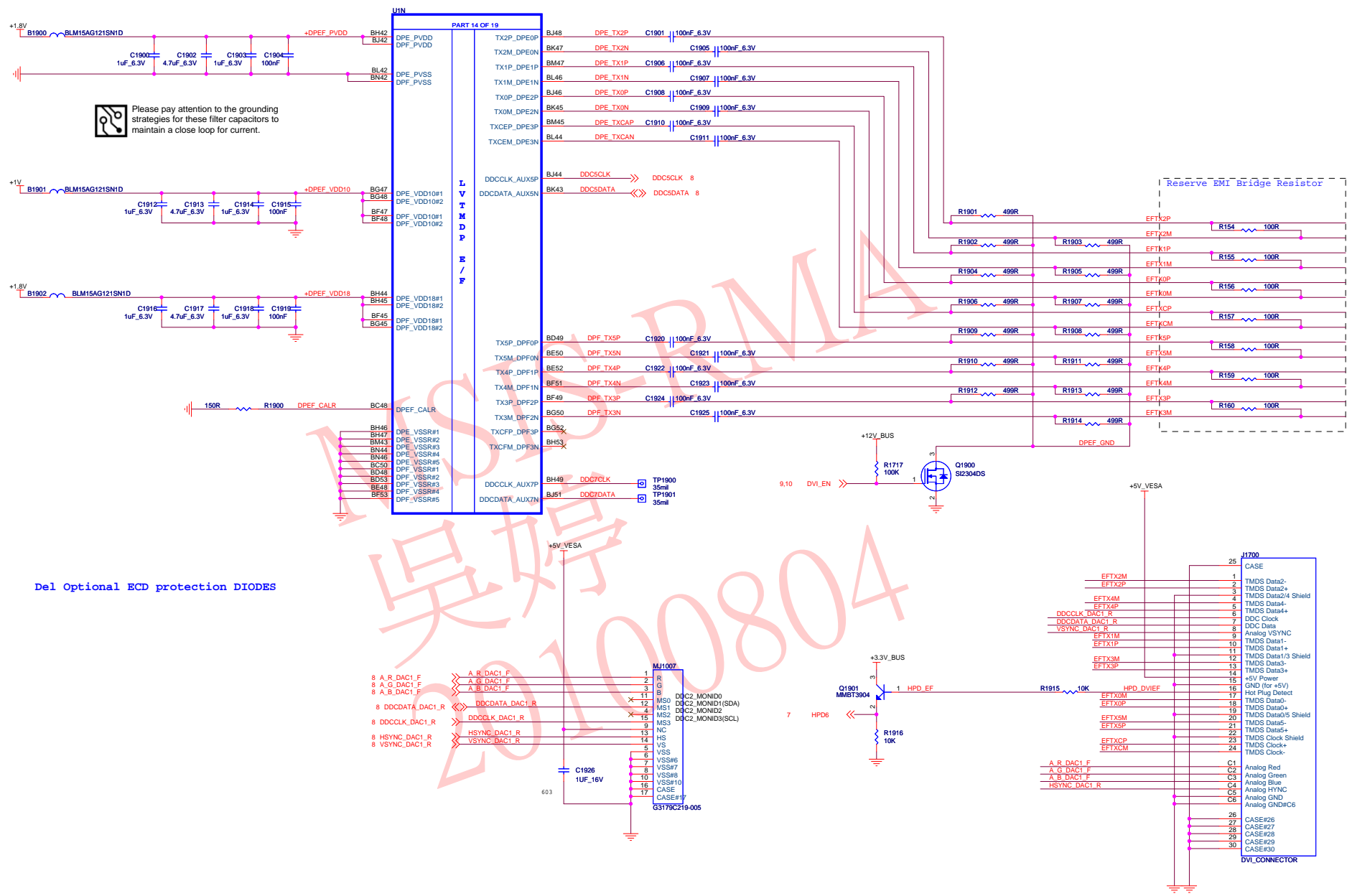
OPTIONAL ESD PROTECTION DIODES



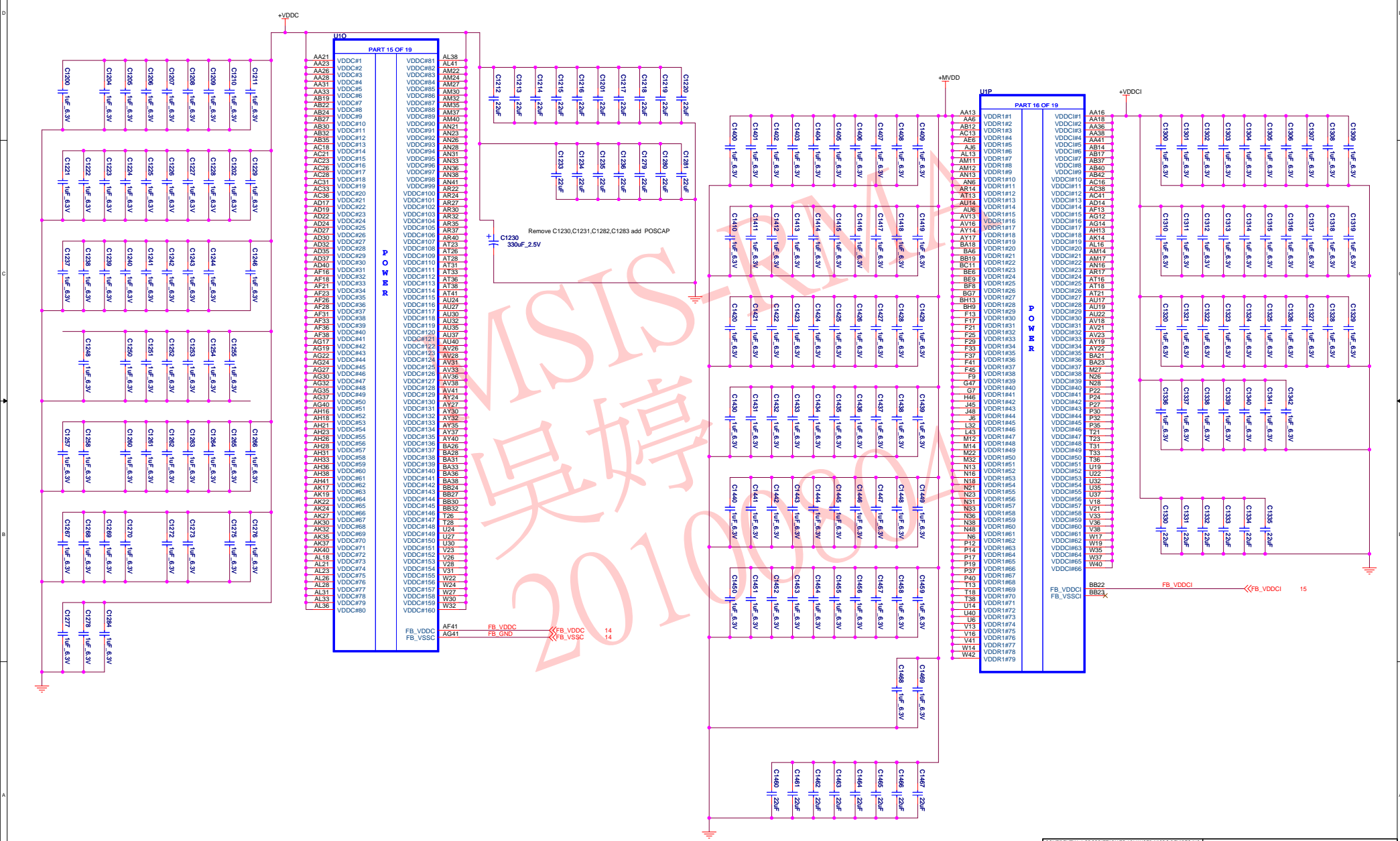
PLEASE NOTE +5V NEEDS TO HAVE A SEPARATE REGULATOR FOR HDMI!!

OVERLAP HDMI WITH DP

(11) CYPRESS LVTMDP E&F



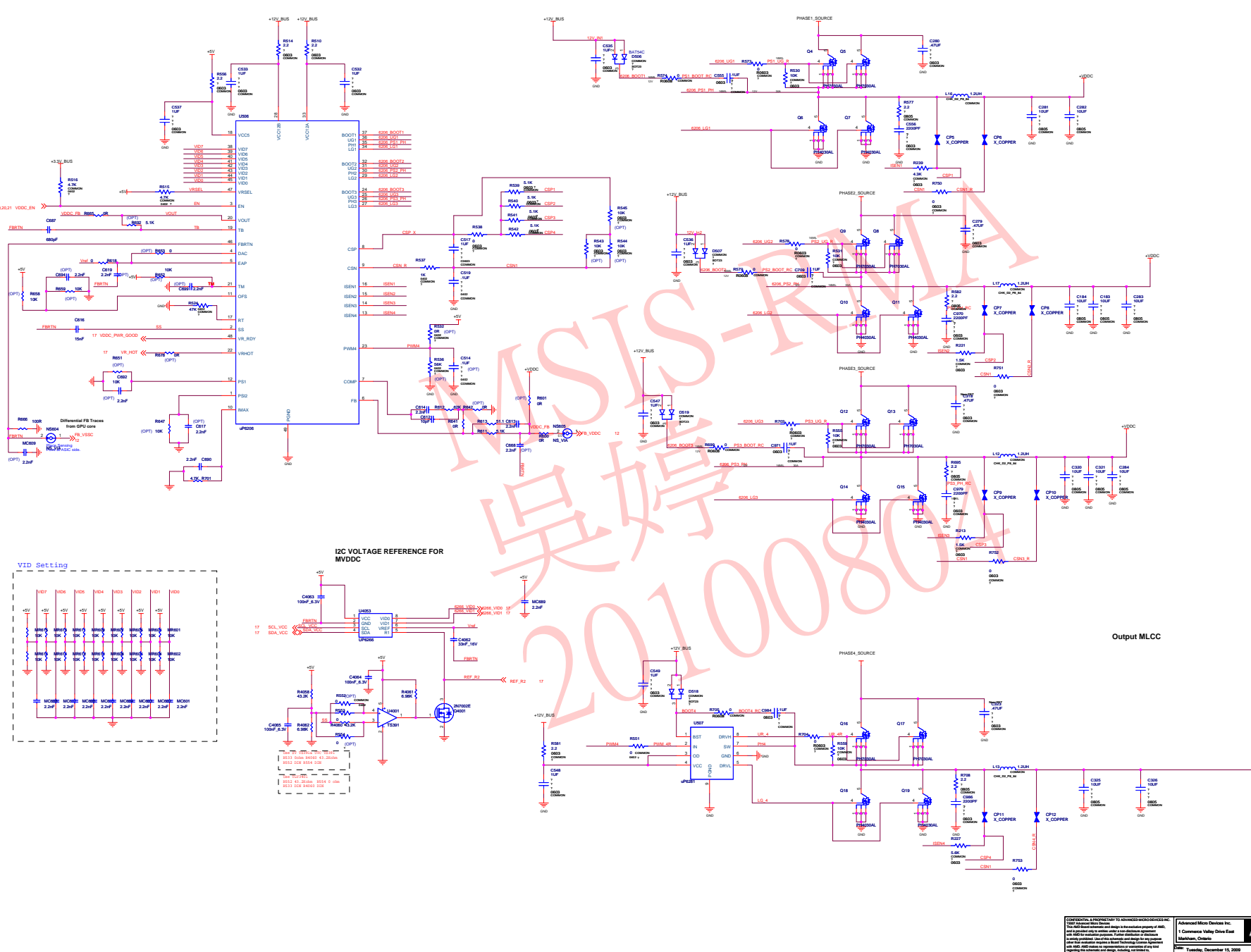
(12) CYPRESS Power



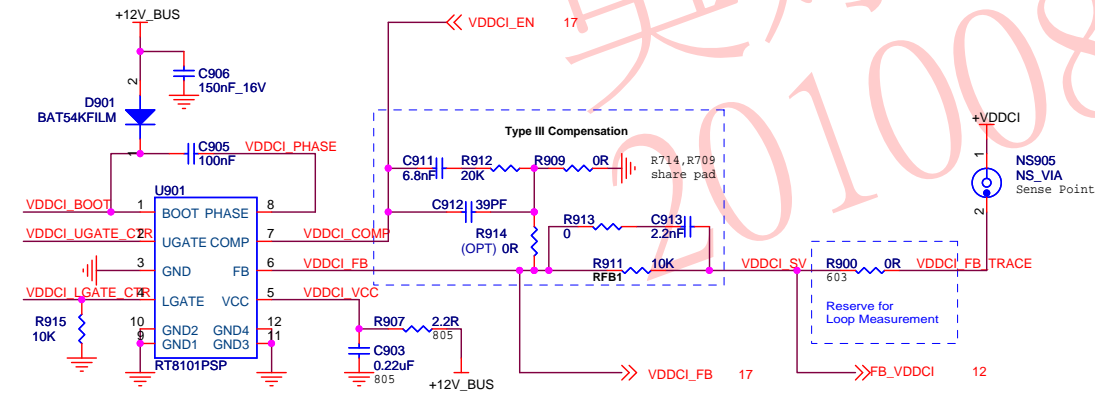
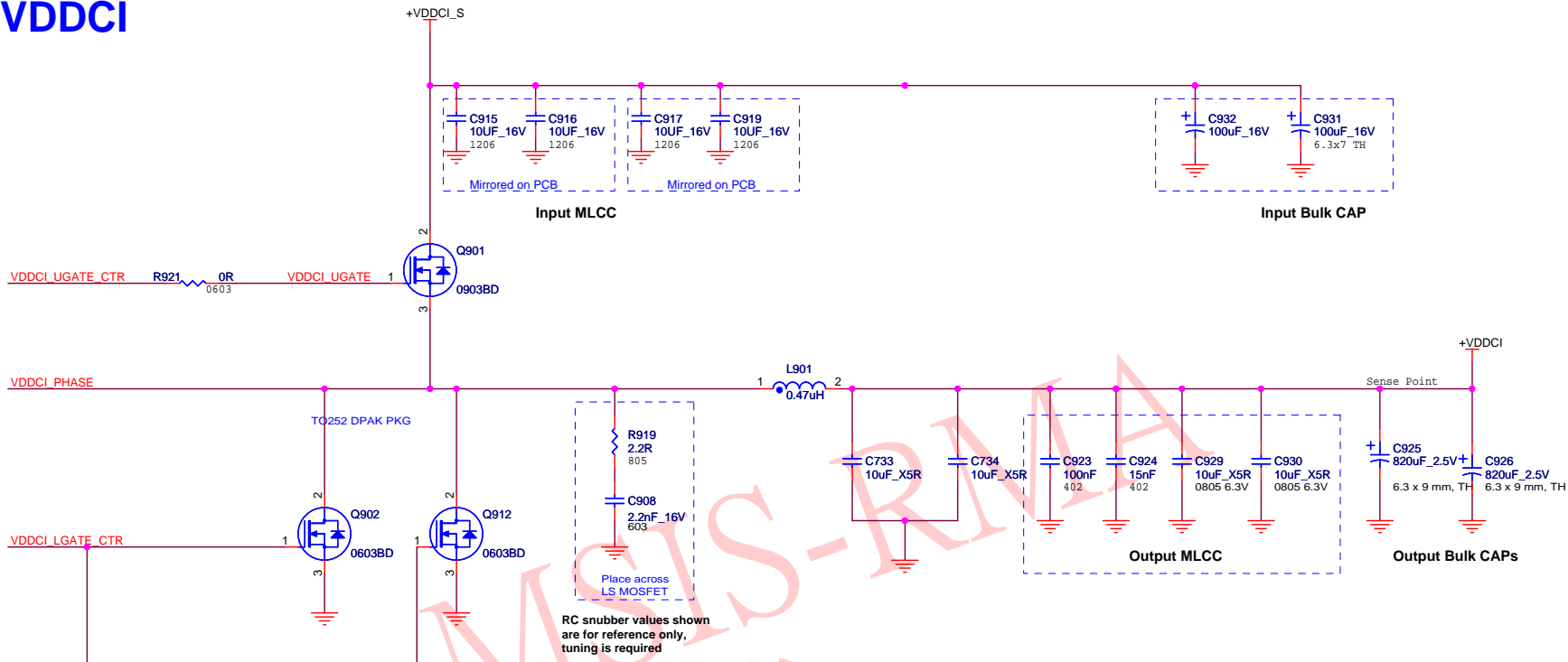
(13) CYPRESS GND

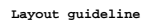
UIC			UIR		
PART 17 OF 19			PART 18 OF 19		
A46	VSS#1	AM0	BA17	VSS#251	L42
AA10	VSS#2	AM13	BA19	VSS#252	L48
AA14	VSS#3	AM16	BA20	VSS#253	L52
AA17	VSS#4	AM21	BA22	VSS#254	L5
AA19	VSS#5	AM23	BA24	VSS#255	VSS#379
AA2	VSS#6	AM26	BA27	VSS#256	M13
AA22	VSS#7	AM28	BA30	VSS#257	VSS#381
AA24	VSS#8	AM31	BA32	VSS#258	VSS#382
AA27	VSS#9	AM33	BA35	VSS#259	VSS#383
AA30	VSS#10	AM36	BA37	VSS#260	VSS#384
AA32	VSS#11	AM38	BA40	VSS#261	VSS#385
AA35	VSS#12	AM41	BA44	VSS#262	VSS#386
AA37	VSS#13	AM46	BB17	VSS#263	VSS#387
AA40	VSS#14	AM51	BB19	VSS#264	VSS#388
AA42	VSS#15	AM56	BB20	VSS#265	VSS#389
AA4	VSS#16	AM58	BB22	VSS#266	N2
AB13	VSS#17	AN2	BB26	VSS#267	VSS#391
AB16	VSS#18	AN22	BB28	VSS#268	N24
AB18	VSS#19	AN24	BB31	VSS#269	N27
AB21	VSS#20	AN27	BB33	VSS#270	VSS#393
AB23	VSS#21	AN30	BB40	VSS#271	N30
AB26	VSS#22	AN32	BB44	VSS#272	N32
AB28	VSS#23	AN35	BB51	VSS#273	VSS#397
AB31	VSS#24	AN37	BB53	VSS#274	N40
AB33	VSS#25	AN40	BB5	VSS#275	VSS#399
AB36	VSS#26	AN9	BC14	VSS#276	VSS#400
AB38	VSS#27	AR16	BC16	VSS#277	VSS#401
AB41	VSS#28	AR2	BC19	VSS#278	VSS#402
AB9	VSS#29	AR22	BC2	VSS#279	VSS#403
AC10	VSS#30	AR23	BC23	VSS#280	VSS#404
AC14	VSS#31	AR26	BC33	VSS#281	VSS#405
AC17	VSS#32	AR28	BC40	VSS#282	VSS#406
AC19	VSS#33	AR31	BC4	VSS#283	VSS#407
AC2	VSS#34	AR33	BD15	VSS#284	VSS#408
AC22	VSS#35	AR36	BD16	VSS#285	VSS#409
AC24	VSS#36	AR38	BD20	VSS#286	VSS#410
AC27	VSS#37	AR41	BD38	VSS#287	VSS#411
AC30	VSS#38	AR46	BE12	VSS#288	VSS#412
AC32	VSS#39	AR51	BE16	VSS#289	VSS#413
AC35	VSS#40	AT10	BE2	VSS#290	VSS#414
AC37	VSS#41	AT17	BE25	VSS#291	VSS#415
AC40	VSS#42	AT19	BF14	VSS#292	VSS#416
AC42	VSS#43	AT22	BF16	VSS#293	R10
AC6	VSS#44	AT24	BF19	VSS#294	VSS#417
AD13	VSS#45	AT27	BF21	VSS#295	VSS#419
AD16	VSS#46	AT30	BF26	VSS#296	R2
AD18	VSS#47	AT32	BF32	VSS#297	R44
AD21	VSS#48	AT35	BF9	VSS#298	VSS#420
AD23	VSS#49	AT37	BQ2	VSS#299	R48
AD26	VSS#50	AT40	BQ4	VSS#300	R50
AD28	VSS#51	AT46	BH1	VSS#301	VSS#422
AD31	VSS#52	AT48	BH11	VSS#302	T11
AD33	VSS#53	AT51	BH12	VSS#303	T12
AD36	VSS#54	AT56	BH14	VSS#304	VSS#426
AD38	VSS#55	AT58	BH15	VSS#305	T24
AD41	VSS#56	AT62	BH30	VSS#306	VSS#430
AE1	VSS#57	AU21	BH39	VSS#307	VSS#431
AE2	VSS#58	AU23	BH40	VSS#308	T32
AE5	VSS#59	AU26	BH7	VSS#309	VSS#433
AF10	VSS#60	AU28	BK15	VSS#310	VSS#434
AF14	VSS#61	AU31	BL16	VSS#311	VSS#435
AF17	VSS#62	AU33	BL38	VSS#312	T40
AF19	VSS#63	AU36	BL39	VSS#313	VSS#437
AF22	VSS#64	AU41	BM11	VSS#314	T43
AF23	VSS#65	AU46	BM15	VSS#315	VSS#438
AF27	VSS#66	AU50	BM7	VSS#316	VSS#439
AF30	VSS#67	AV11	BN16	VSS#317	T53
AF35	VSS#68	AV14	BN38	VSS#318	VSS#442
AF37	VSS#69	AV17	F10	VSS#319	T8
AF40	VSS#70	AV19	F11	VSS#320	U13
AG13	VSS#71	AV22	F14	VSS#321	U16
AG16	VSS#72	AV24	F15	VSS#322	U18
AG18	VSS#73	AV27	F19	VSS#323	U21
AG2	VSS#74	AV30	F23	VSS#324	U23
AG21	VSS#75	AV35	F27	VSS#325	U28
AG23	VSS#76	AV37	F31	VSS#326	U31
AG26	VSS#77	AV40	F35	VSS#327	U33
AG28	VSS#78	AV43	F36	VSS#328	VSS#452
AG31	VSS#79	AV46	F39	VSS#329	U36
AG33	VSS#80	AV50	F43	VSS#330	U38
AG36	VSS#81	AW2	F49	VSS#331	U41
AG38	VSS#82	AW50	G2	VSS#332	VSS#455
AG6	VSS#83	AW52	G29	VSS#333	VSS#457
AH10	VSS#84	AW6	G43	VSS#334	VSS#458
AH17	VSS#85	AW9	G52	VSS#335	VSS#459
AH19	VSS#86	AY10	G6	VSS#336	VSS#460
AH22	VSS#87	AY13	H12	VSS#337	VSS#461
AH24	VSS#88	AY16	H16	VSS#338	VSS#462
AH27	VSS#89	AY18	H21	VSS#339	VSS#463
AH30	VSS#90	AY21	H25	VSS#340	VSS#464
AH32	VSS#91	AY23	H32	VSS#341	VSS#465
AH36	VSS#92	AY26	H35	VSS#342	VSS#466
AH37	VSS#93	AY28	H36	VSS#343	VSS#467
AH40	VSS#94	AY33	H42	VSS#344	VSS#468
AH9	VSS#95	AY36	H45	VSS#345	VSS#469
AH11	VSS#96	AY41	H9	VSS#346	VSS#470
AJ2	VSS#97	AY46	J1	VSS#347	VSS#471
AJ7	VSS#98	AY48	J18	VSS#348	VSS#472
AK13	VSS#99	AY52	J22	VSS#349	VSS#473
AK16	VSS#100	AY58	J28	VSS#350	VSS#474
AK19	VSS#101	AY62	J31	VSS#351	VSS#475
AK21	VSS#102	AY66	J33	VSS#352	W21
AK23	VSS#103	AY70	J35	VSS#353	W22
AK26	VSS#104	AY73	J39	VSS#354	W23
AK31	VSS#105	AY76	J40	VSS#355	W26
AK33	VSS#106	AY78	J42	VSS#356	W28
AK36	VSS#107	AY82	J43	VSS#357	W31
AK38	VSS#108	AY86	J45	VSS#358	W33
AK39	VSS#109	AY90	J46	VSS#359	W36
AK41	VSS#110	AY93	J49	VSS#360	W38
AL14	VSS#111	AY96	K21	VSS#361	W41
AL17	VSS#112	AY98	K23	VSS#362	W48
AL19	VSS#113	AY100	K25	VSS#363	W6
AL2	VSS#114	AY103	K26	VSS#364	A4
AL22	VSS#115	AY106	K28	VSS#365	VSS_MECH#1
AL24	VSS#116	AY108	K32	VSS#366	A50
AL27	VSS#117	AY110	K35	VSS#367	VSS_MECH#2
AL30	VSS#118	AY113	K37	VSS#368	BK1
AL32	VSS#119	AY116	K39	VSS#369	VSS_MECH#3
AL35	VSS#120	AY118	K40	VSS#370	VSS_MECH#4
AL37	VSS#121	AY120	K42	VSS#371	VSS_MECH#5
AL40	VSS#122	AY123	K43	VSS#372	VSS_MECH#6
AL6	VSS#123	AY126	K45	VSS#373	VSS_MECH#7
AL9	VSS#124	AY128	K46	VSS#374	VSS_MECH#8
	VSS#125	AY130	K47	VSS#375	VSS_MECH#9
		AY133	K49		VSS_MECH#10
		AY136	K51		VSS_MECH#11
		AY138	K52		VSS_MECH#12
		AY140	K53		VSS_MECH#13
		AY143	K54		VSS_MECH#14
		AY146	K55		VSS_MECH#15
		AY148	K56		VSS_MECH#16
		AY150	K57		VSS_MECH#17
		AY153	K58		VSS_MECH#18
		AY156	K59		VSS_MECH#19
		AY158	K60		VSS_MECH#20
		AY160	K61		VSS_MECH#21
		AY163	K62		VSS_MECH#22
		AY166	K63		VSS_MECH#23
		AY168	K64		VSS_MECH#24
		AY170	K65		VSS_MECH#25
		AY173	K66		VSS_MECH#26
		AY176	K67		VSS_MECH#27
		AY178	K68		VSS_MECH#28
		AY180	K69		VSS_MECH#29
		AY183	K70		VSS_MECH#30
		AY186	K71		VSS_MECH#31
		AY188	K72		VSS_MECH#32
		AY190	K73		VSS_MECH#33
		AY193	K74		VSS_MECH#34
		AY196	K75		VSS_MECH#35
		AY198	K76		VSS_MECH#36
		AY200	K77		VSS_MECH#37
		AY203	K78		VSS_MECH#38
		AY206	K79		VSS_MECH#39
		AY208	K80		VSS_MECH#40
		AY210	K81		VSS_MECH#41
		AY213	K82		VSS_MECH#42
		AY216	K83		VSS_MECH#43
		AY218	K84		VSS_MECH#44
		AY220	K85		VSS_MECH#45
		AY223	K86		VSS_MECH#46
		AY226	K87		VSS_MECH#47
		AY228	K88		VSS_MECH#48
		AY230	K89		VSS_MECH#49
		AY233	K90		VSS_MECH#50
		AY236	K91		VSS_MECH#51
		AY238	K92		VSS_MECH#52
		AY240	K93		VSS_MECH#53
		AY243	K94		VSS_MECH#54
		AY246	K95		VSS_MECH#55
		AY248	K96		VSS_MECH#56
		AY250	K97		VSS_MECH#57
		AY253	K98		VSS_MECH#58
		AY256	K99		VSS_MECH#59
		AY258	K100		VSS_MECH#60
		AY260	K101		VSS_MECH#61
		AY263	K102		VSS_MECH#62
		AY266	K103		VSS_MECH#63
		AY268	K104		VSS_MECH#64
		AY270	K105		VSS_MECH#65
		AY273	K106		VSS_MECH#66
		AY276	K107		VSS_MECH#67
		AY278	K108		VSS_MECH#68
		AY280	K109		VSS_MECH#69
		AY283	K110		VSS_MECH#70
		AY286	K111		VSS_MECH#71
		AY288	K112		VSS_MECH#72
		AY290	K113		VSS_MECH#73
		AY293	K114		VSS_MECH#74
		AY296	K115		VSS_MECH#75
		AY298	K116		VSS_MECH#76
		AY300	K117		VSS_MECH#77
		AY303	K118		VSS_MECH#78
		AY306	K119		VSS_MECH#79
		AY308	K120		VSS_MECH#80
		AY310	K121		VSS_MECH#81
		AY313	K122		VSS_MECH#82
		AY316	K123		VSS_MECH#83
		AY318	K124		VSS_MECH#84
		AY320	K125		VSS_MECH#85
		AY323	K126		VSS_MECH#86
		AY326	K127		VSS_MECH#87
		AY328	K128		VSS_MECH#88
		AY330	K129		VSS_MECH#89
		AY333	K130		VSS_MECH#90
		AY336	K131		VSS_MECH#91
		AY338	K132		VSS_MECH#92
		AY340	K133		VSS_MECH#93
		AY343	K134		VSS_MECH#94
		AY346	K135		VSS_MECH#95
		AY348	K136		VSS_MECH#96
		AY350	K137		VSS_MECH#97
		AY353	K138		VSS_MECH#98
		AY356	K139		VSS_MECH#99
		AY358	K140		VSS_MECH#100
		AY360	K141		VSS_MECH#101
		AY363	K142		VSS_MECH#102
		AY366	K143		VSS_MECH#103
		AY368	K144		VSS_MECH#104
		AY370	K145		VSS_MECH#105
		AY373	K146		VSS_MECH#106
		AY376	K147		VSS_MECH#107
		AY378	K148		VSS_MECH#108
		AY380	K149		VSS_MECH#109
		AY383	K150		VSS_MECH#110
		AY386	K151		VSS_MECH#111
		AY388	K152		VSS_MECH#112
		AY390	K153		VSS_MECH#113
		AY393	K154		VSS_MECH#114
		AY396	K155		VSS_MECH#115
		AY398	K156		VSS_MECH#116
		AY400	K157		VSS_MECH#117
		AY403	K158		VSS_MECH#118
		AY406	K159		VSS_MECH#119
		AY408	K160		VSS_MECH#120
		AY410	K161		VSS_MECH#121
		AY413	K162		VSS_MECH#122
		AY416	K163		VSS_MECH#123
		AY418	K164		VSS_MECH#124
		AY420	K165		VSS_MECH#125
		AY423	K166		VSS_MECH#126
		AY426	K167		VSS_MECH#127
		AY428	K168		VSS_MECH#128
		AY430	K169		

(14) VDDC



(15) VDDCI



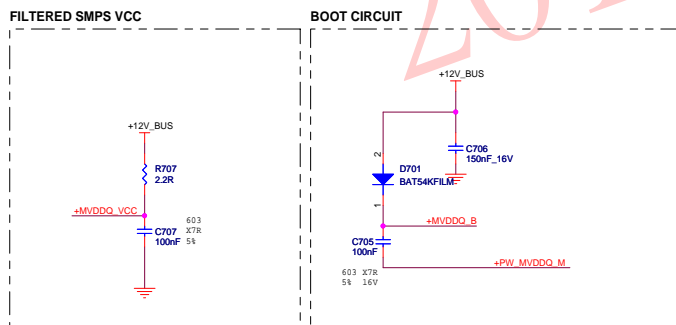
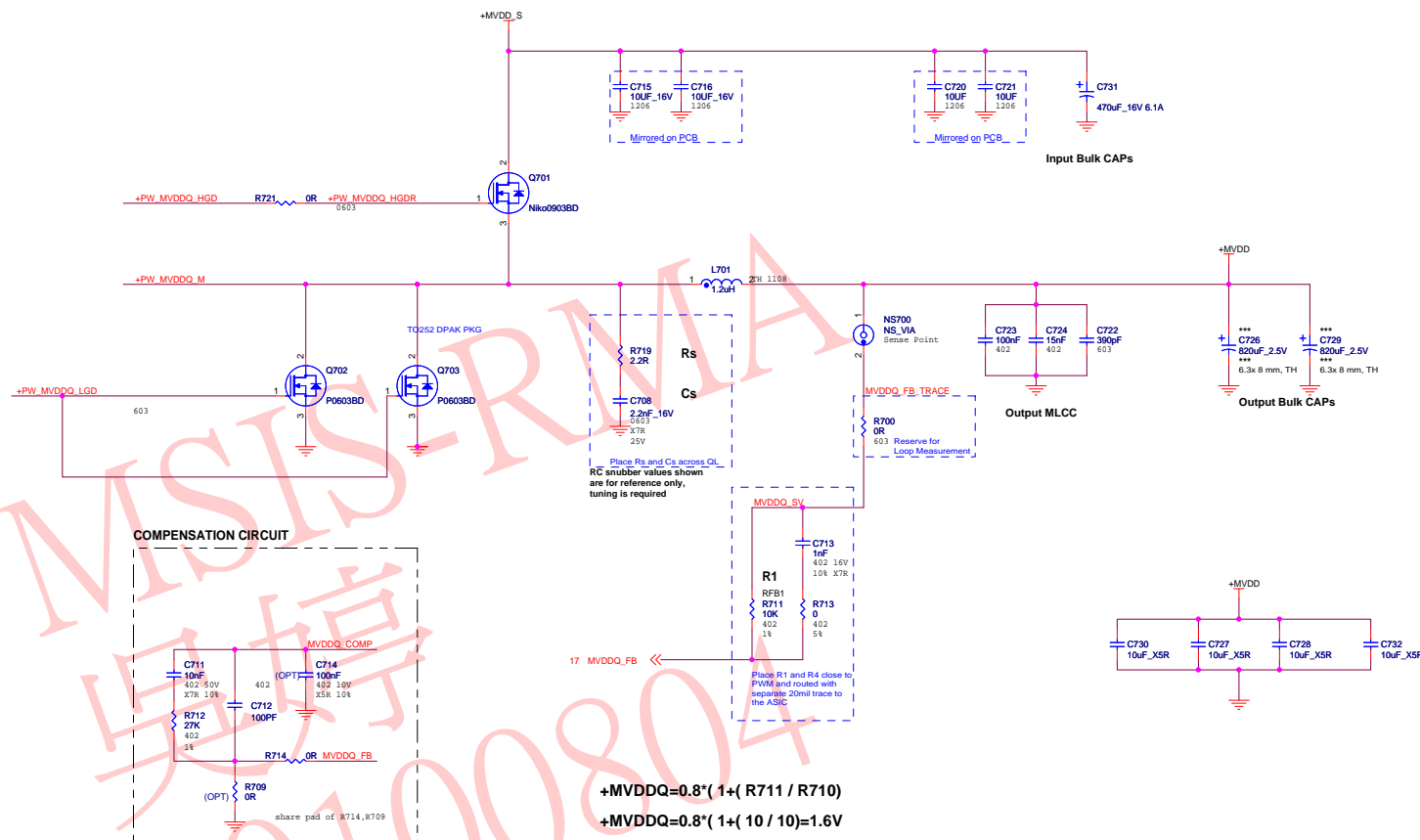


1-Position the controller (U703) such that LGate(pin4) is the closest to gate of the MOSFETS. You can place the gate resistors R71 and R722 next to the gate of the MOSFETS. Make the gate drive traces (PW MVDDC LGB and PW MVDDC HGB) as short and as wide as possible to reduce the trace inductance.

2-Place the bypass capacitors (C703 and C705) as close as possible to the controller as possible. They are as follows:

- 1- Cvc bypass cap is C703, and Boost cap is C705.

3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network as close to the pins as possible. These are R710, R711, R713, C718 and R712, C711 and C712.



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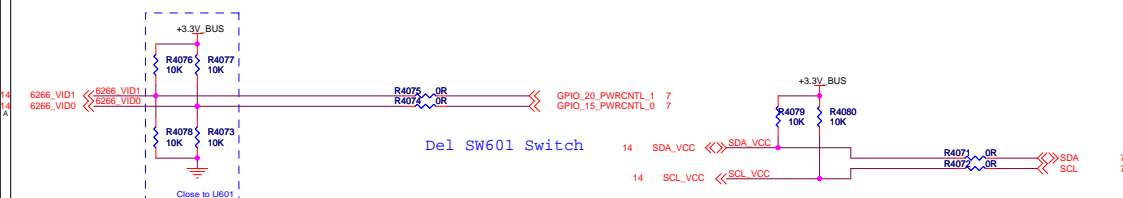
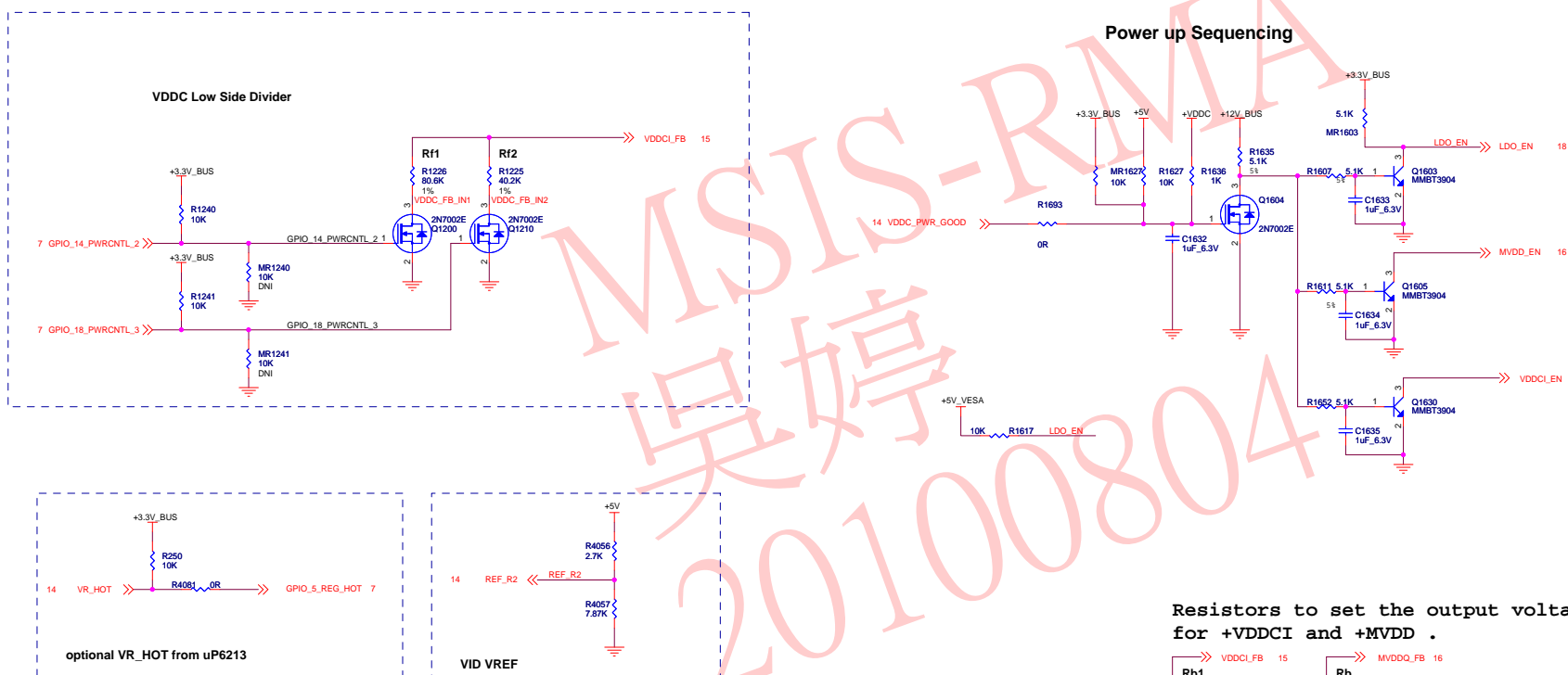
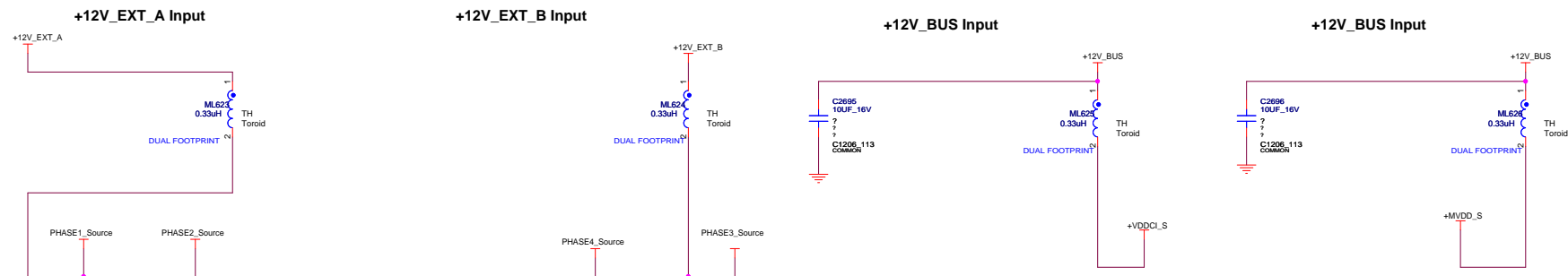
Sheet 16 of 23

Rev 2

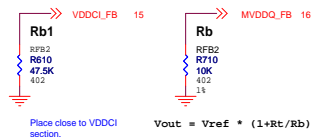
Title	MVDD
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Doc No.	105-C008XX-00C
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(17) CYPRESS VDDCI POWER PLAY



Resistors to set the output voltages
for +VDDCI and +MVDD .



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Sheet 17 of 23

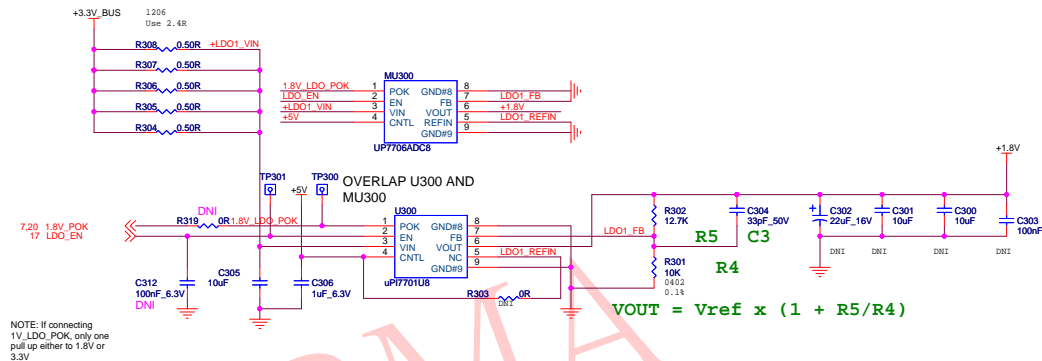
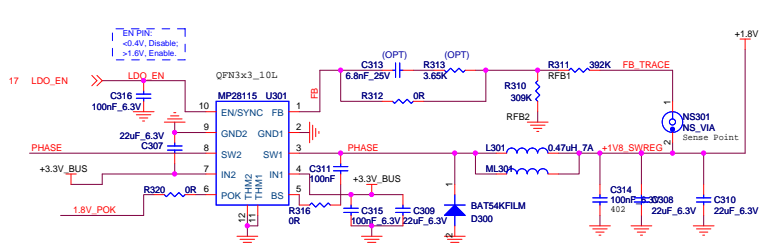
Rev 2

Title	Power Management 2
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Doc No.	105-C008XX-00C
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(18) CYPRESS Small Rail Regulators

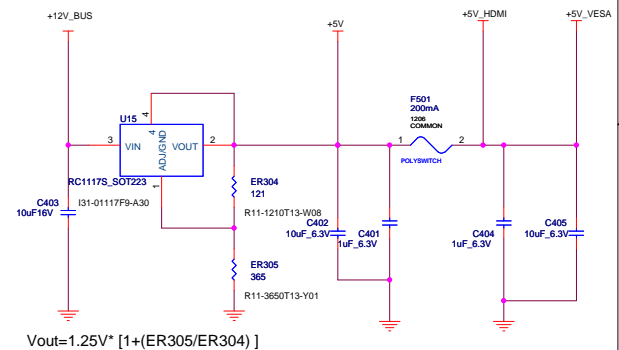
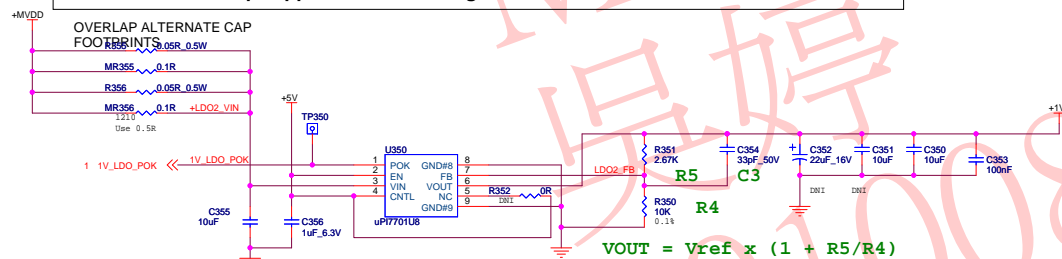
LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



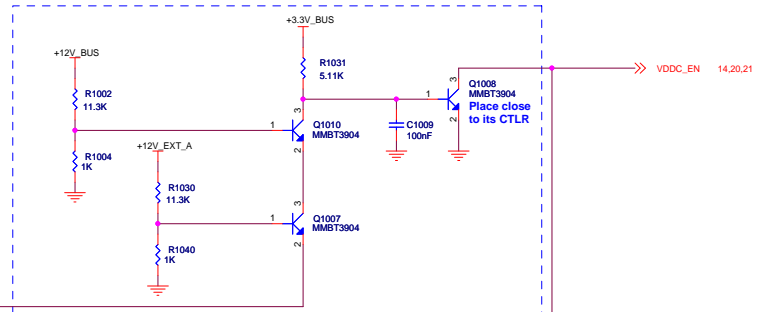
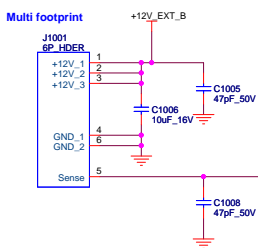
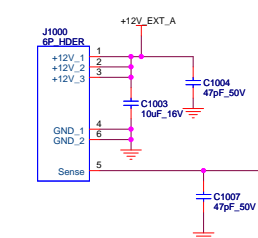
NOTE: If connecting 1V_LDO_POK, only one pull up either to 1.8V or 3.3V

optional 5V power for VDDC regulator;

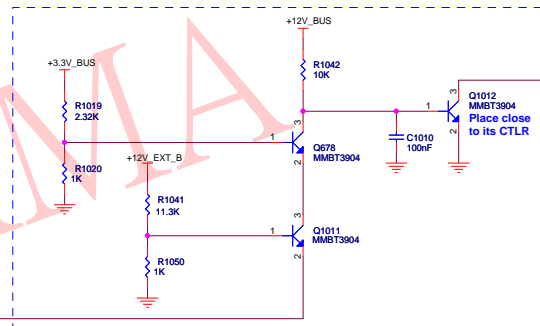
LDO #2: Vin = +1.35V to 1.8VMAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



(19) CYPRESS POWER MGMNT



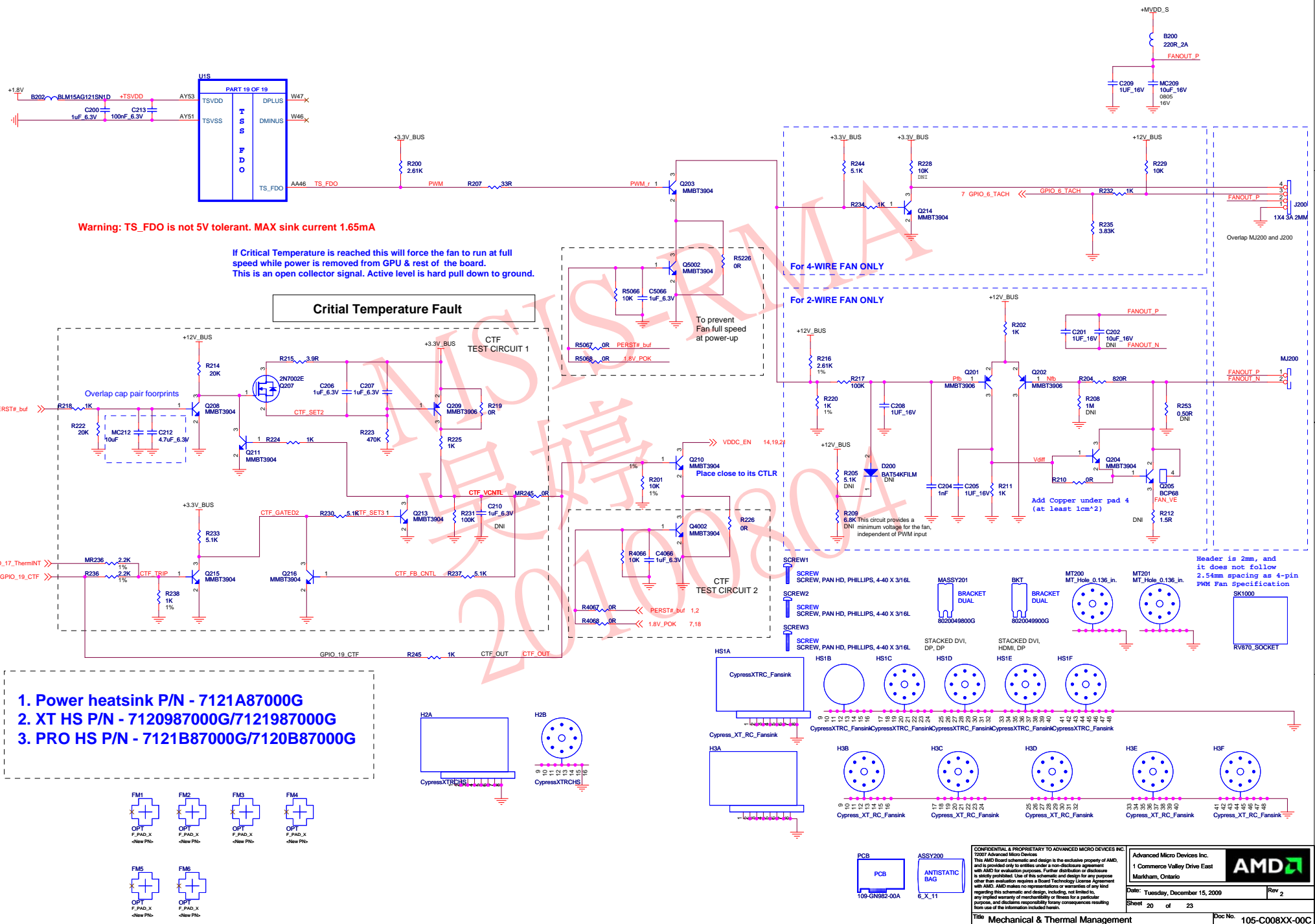
BUS 12V and AUX A Power up Seq



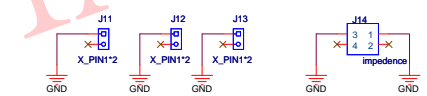
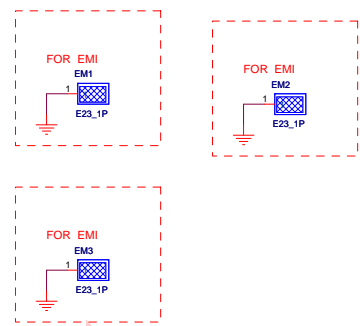
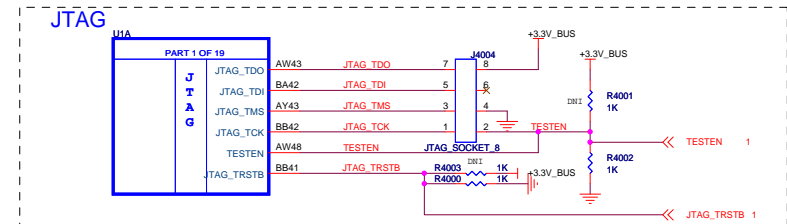
BUS 3.3V and AUX B Power up Seq

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(20) CYPRESS Mechanical and Thermal Management

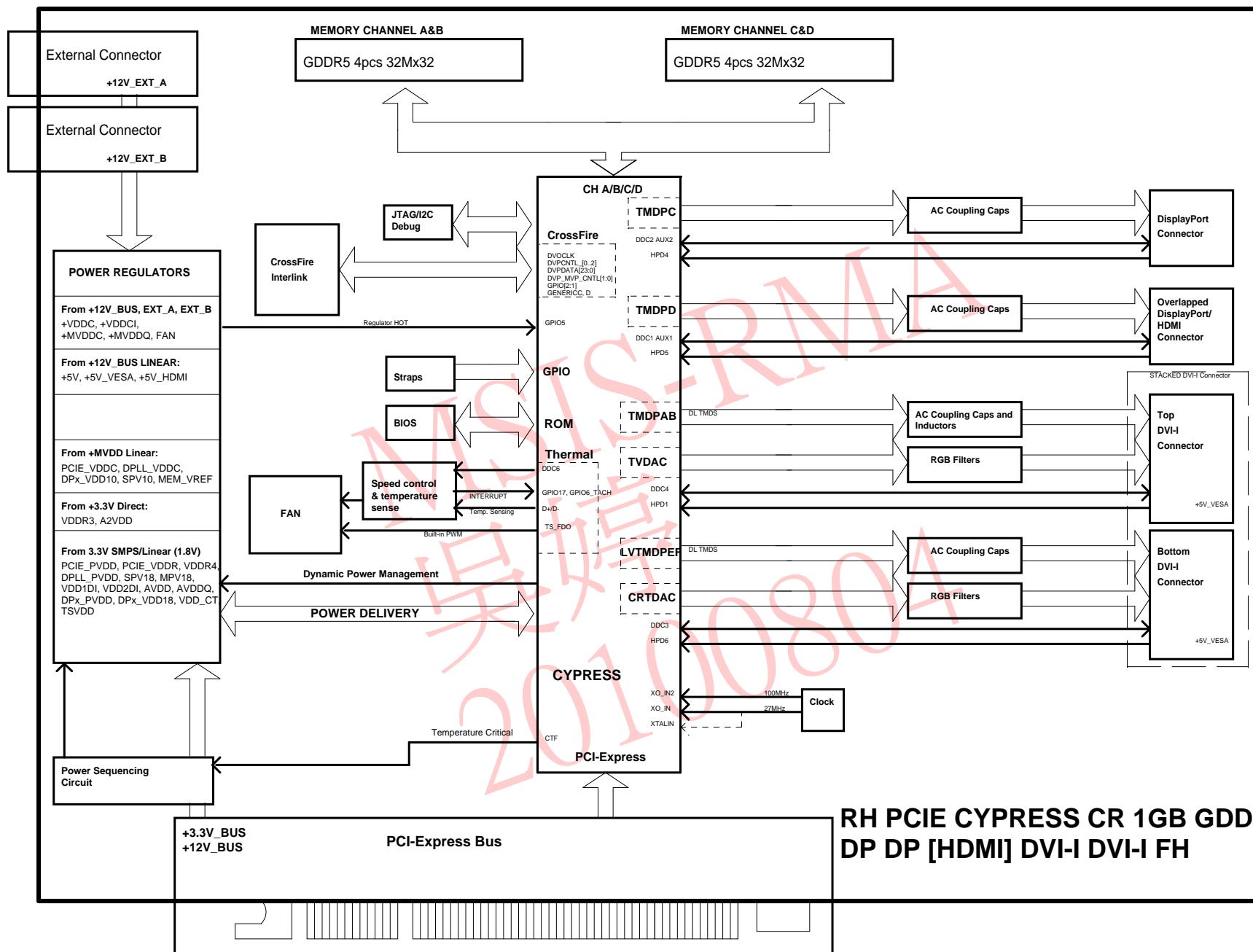


(21) CYPRESS Debug Circuits



Del PTC protect circuit.

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**RH PCIE CYPRESS CR 1GB GDDR5
DP DP [HDMI] DVI-I DVI-I FH**



Title RH CYPRESS GDDR5 DP-HDMI-DVII-DVII		Schematic No. 105-C008XX-00C	Date: Tuesday, December 15, 2009
REVISION HISTORY		NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.	Rev 2
REVISION DESCRIPTION			
Initial release. Based on CYPRESS XT C001 00 PCB			
Based on CYPRESS XT C008 0C PCB			
1. Page 7 Change U2 SL16010DCT to U1006 and Co-lay U1008 with U12 SL16010DCT 2. Page 8 Del DAC2 RGB 3. Page 9 Disable TMDP AB and disable DDC_AUX3,DDC_AUX4 4. Page 10 Del DP co-lay with HDMI 5. Page 11 Del Dual DVI Connector Change to Single DVI and Co-lay Slim D-Sub 6. Page 12 Remove C1230,C1231,C1282,C1283 add POSCAP 7. Page 14 Change VDDC PWM to Up6206 8. Page 18 Change +5V circuit. 9. Page 21 Del PTC protect circuit. 10. Page3,4 changing the DRAM reset circuit 11. Page10 chang HDMI DDC to DDC3 12. Page 14 co-lay U4001 with TLV3401			

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