

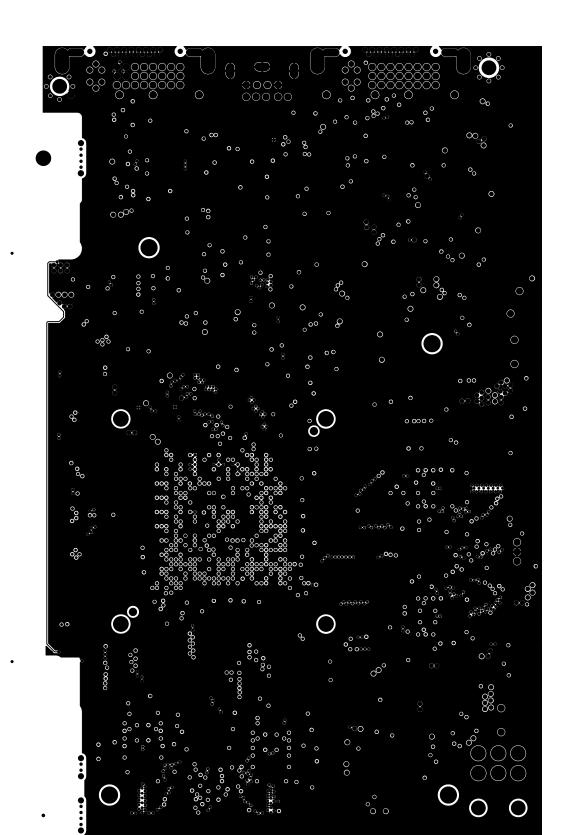


RH PCIe RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH PN 109-B06731-00B LAYER 1

FILM 1 OF 13

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RH PCIe RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH PN 109-B06731-00B LAYER 2

AUG. 14, 2006

DESIGNER DORINA A.

L2 INNER FILM 2 OF 13

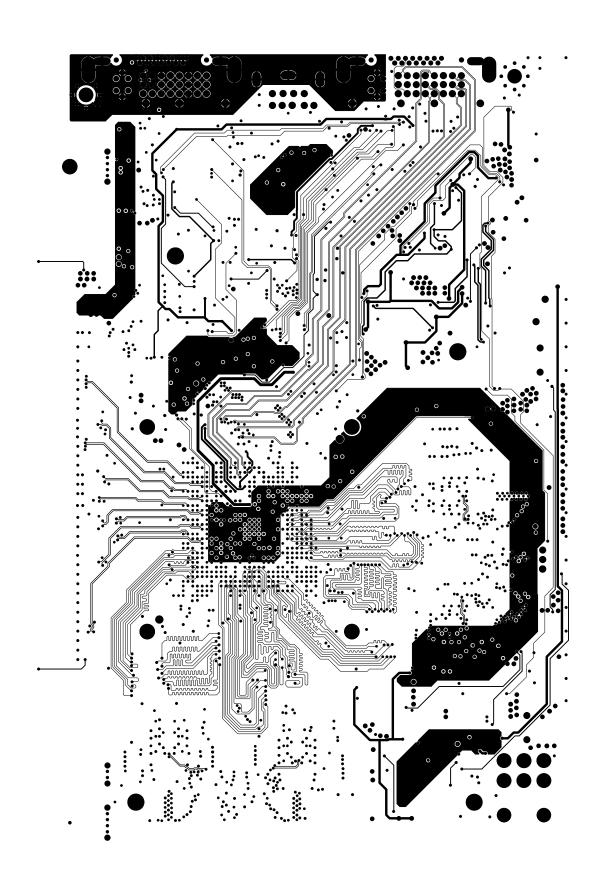


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DESIGNER DORINA A.

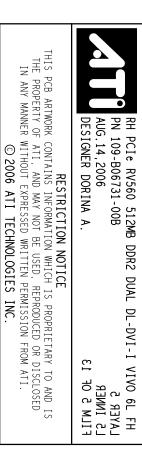
RH PCIe RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH PN 109-B06731-00B \$\text{A} \text{A} \text{

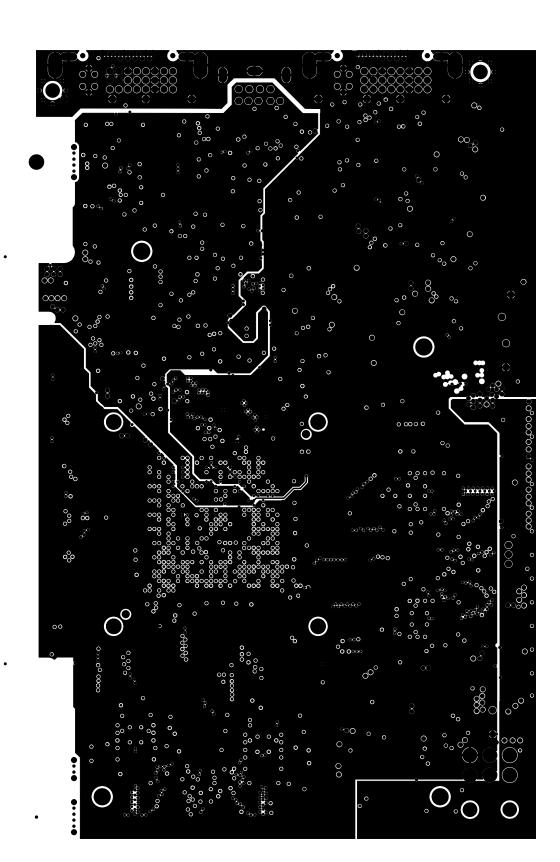
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LIFM 4 OL F4 IMMEB FVAEB 4

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DESIGNER DORINA A.

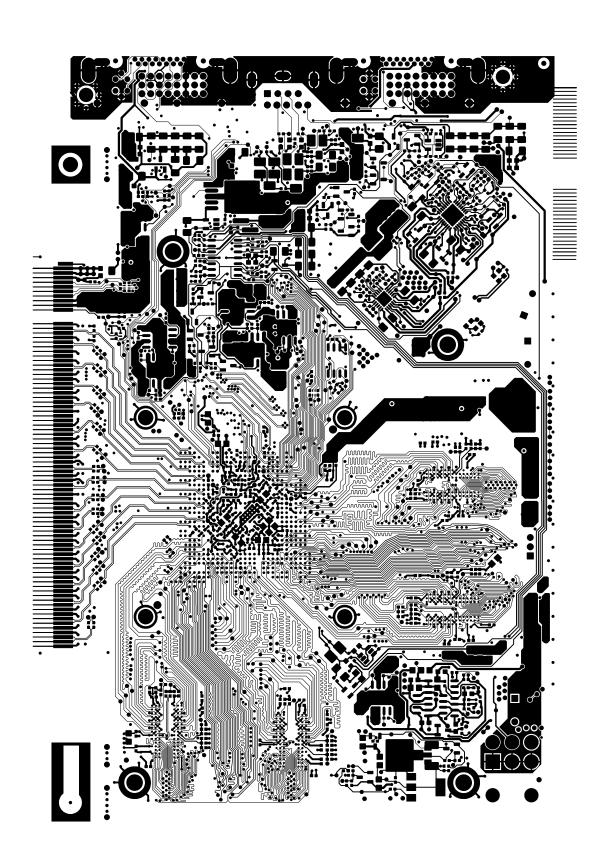
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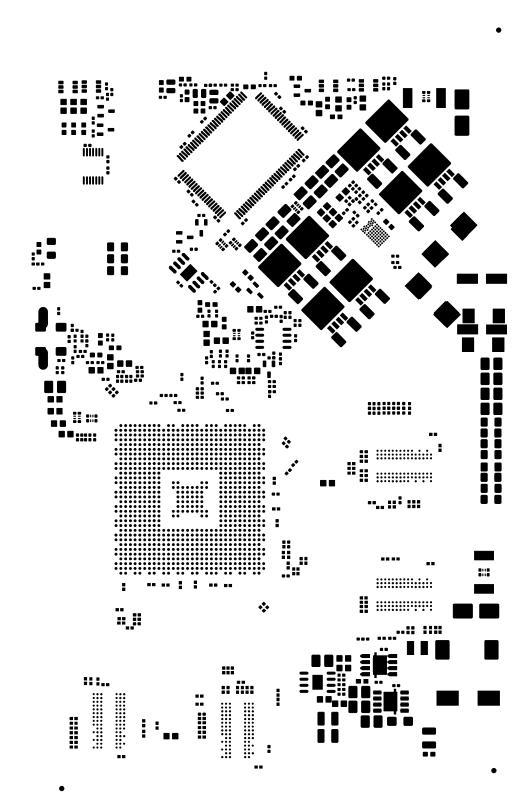
LIFW @ OL F@ BOLLOW FVEB @

AUG. 14, 2006

PN 109-B06731-00B

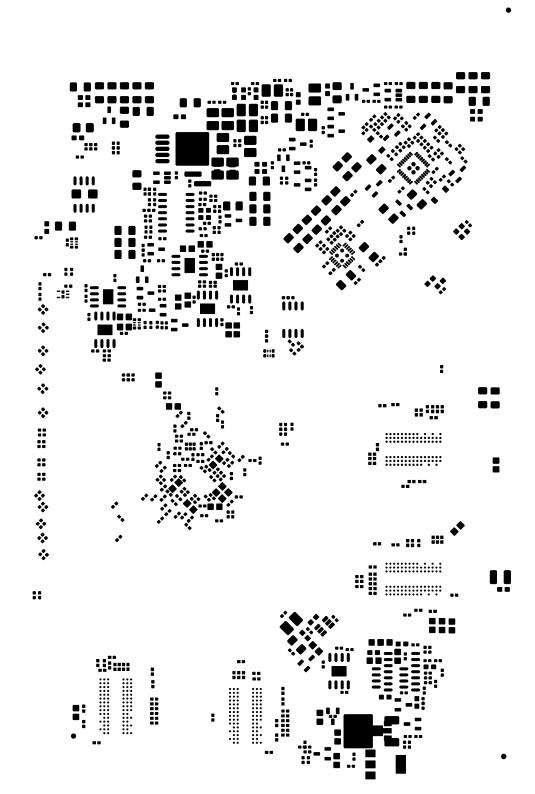
RH PCIe RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH







RH PCIe RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH PN 109-B06731-00B AUG.14,2006 DESIGNER DORINA A. SOLDER PASTE TOP FILM 7 OF 13



RH PCIe RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH

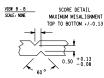
PN 109-B06731-00B AUG. 14, 2006 DESIGNER DORINA A

EIFW 8 OE 13 SOFDEB BYSEI BOLLOW

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PCIe CHAMFER TO BE ROUTED. BEVELLING SHALL BE SMOOTH, FREE OF BURRS, SLIVERS AND SHARP EDGES.

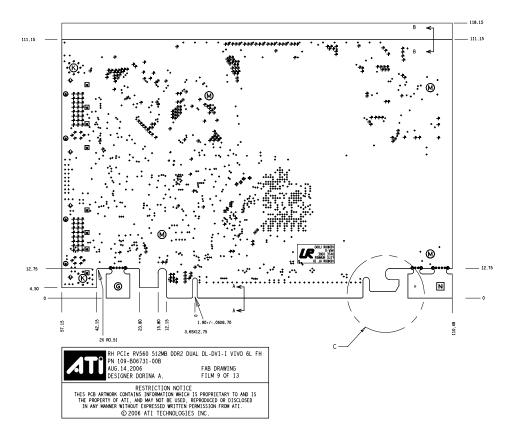


6 LAYER CRO	SS SECTION BUILD -	CONTROL	ED IMPEDANCE
MASK TOP			ROUTING
	PREPREG 0.100		
L2_INNER	PREPREG 0.100	1	PLANE
L3_INNER	PREPREG 0.978	1/2 02	ROUTING
L4_INNER	PREPREG [0.100	1/2 oz	ROUTING
L5_INNER		2 oz	PLANE
BOTTOM	PREPREG 0.100	1/2 07	ROUTING

BOARD THICKNESS AFTER PLATING: [1.57mm] */-0.13mm AS MEASURED AT GOLD PLATED FINGERS (IF PRESENT)

			D1	DIFFERENTIAL 95 ohms +/	
141	MICROSTRIP IN	PEDANCE		Trace Width:	0.127 mm
M1	57 ohms +/	10%		Spacing:	0.180 mm
	Trace Midth:	0.099 mm		On Layers:	1,6
	On Layers:	1,6		Referenced To:	2,5
	Referenced to:	2,5		Note: PCIE	
-	Note: Mem Data & A	dd. Branch			
M2	MICROSTRIP IMPEDANCE		D2	DIFFERENTIAL 95 ohms +/	
IVIL	51 ohms +/			Trace Width:	0,127 📾
- 1	Trace Nidth;	0,130 mm		Spacing:	0.180 mm
- 1	On Layers:	6		On Layers:	4
- 1	Referenced to:	5		Referenced To-	5
	Note: Hemory Address Trunk			Note: PCIE	-
<u> </u>	DIFFERENTIA	Meening	7		
Ш	D4 DIFFERENTIAL IMPEDANCE 100 ohms -/- 10%		_ D3	DIFFERENTIAL IMPEDANCE 100 ohrs +/- 10%	
	Trace Width:	0.0689 mm	⊣ ՝	Trace Width:	0.0889 m
	Spacing:	0,2109 mm		Seacing:	0.1409 m
	On Layers:	1,6	4	On Layers;	4
	Referenced To:	2,5		Referenced To:	5
	Note: TMDS Signals				-
			_	Note: TMDS Signals	

(unless	TOLERANCES otherwise spi	cified)
0.X	0.XX	ANGLES
•/- 0.3	•/- 0.13	•/ -5*
ALL DIMENSIONS APPLY AFTER FINISHING ALL DIMENSIONS IN MILLIMETERS		



DRILL CHART: TOP to BOTTOM (# TOL */- 0.075mm)					
SYMBOL	SIZE	ALL UNITS ARE TOLERANCE	IN MI	LLIMETERS PLATING	SLOT
		IUCENWILE			
•	0,03	*	6	PLATED	1.00 x 2.19
\$	0.11	*	4	PLATED	1.00 x 3.05
�	0.19		4	PLATED	2.00 x 4.50
•	0.25	+0.00 - 0.15	2132	PLATED	
٠	0.33		14	PLATED	
+	0,43		255	PLATED	
•	0,6		30	PLATED	
+	0.65	*	12	PLATED	
+	0.9	*	64	PLATED	
+	1.0		11	PLATED	
◙	1.1	٠	8	PLATED	
Ð	1.8	٠	6	PLATED	
•	0.61	٠	10	NON-PLATED	
•	1,2	•/- 0.05	6	NON-PLATED	
Φ	1,65	•/- 0.05	2	NON-PLATED	
•	1.95	•/- 0.05	8	NON-PLATED	
€	3.0	•/- 0.05	2	NON-PLATED	
©	3.175	•/- 0.05	5	NON-PLATED	
N	3,175	•/- 0.05	1	NON-PLATED	
€	3,4	+/- 0.05	2	NON-PLATED	
0	3.5	•/- 0.05	4	NON-PLATED	

- [NUIES	(FOR FABRICATION 1550E5 EMAIL: attipcocaasupportgroupgati.com)
	 ACCEPTABILITY: 	PRINTED WIRING BOARD SHALL MEET THE REQUIREMENTS OF IPC-6012 CLASS 2
	2. MATERIAL:	GLASS EPOXY FR-4 FIRE RETARDANT AND UL 94V-0 RATING

GLASS EPOXY FR-4 FIRE RETARDANT AND UL 94V-0 RATING BOARD OPERATING TEMPERATURE MUST BE UL APPROVED TO A MAX 130 Deg C MATERIAL SHOULD MEET IPC-4101/ST BE UL APPROVED TO A MAX 130 Deg C MATERIAL SHALL ALSO MEET THE RELIABILITY REQUIREMENTS FOR MULTIPLE THERMAL PROFILES USED IN LEAD FREE ASSEMBLIES

3. CLEANLINESS: PRINTED WIRING BOARD CLEANLINESS SHALL MEET J-STD-001 PRIOR TO APPLICATION OF SOLDER MASK,

4. SOLDER MASK

SMALL MEET REQUIRMENTS OF IPC-SM-840 CLASS T,COLOUR RED. PLUG all non functional vias prior to solder mask application, then completely cover plugged vias over with solder mask. All functional vias shall will be all the solder mask and in the solder mask and the solder mask and the solder mask are solder mask and the solder mask registration across panel to be maintained.

IMMERSION SILVER AS PER IPC-4553 Specification for Immersion Silver Plating for Printed Circuit Boards. 5. FINISH:

NON-CONDUCTIVE EPOXY INK, WHITE COLOUR DO NOT CLEAR SILKSCREEN FOR AGENCY MARKINGS CE, FCC, ICES AND DECLARATION OF CONFORMITY THAT ARE OVER VIAS.CLEAR SILKSCREEN OVER THROUGH HOLE AND SAUD PADS AND ANY FUNCTIONAL VIAS (TEST POINTS). 6. SILKSCREEN:

7. BOW AND TWIST: SHALL NOT EXCEED 0.75% OF MAXIMUM DIMENSION WHEN TESTED ACCORDING TO IPC-TM-650.

BOARD MANUFACTURER'S LOGO, DATE CODE UL FLAMMABILITY RATING, FILE NUMBER AND UR SYMBOL SHALL APPEAR ON SILKSCREEN TOP IN AREA SHOWN OR IF MIRRORED ON SILKSCREEN BOTTOM IN AREA SHOWN, IR LOGO CAN BE SIZE ADJUSTABLE BUT LEGI 8. VENDOR'S LOGO:

VENDOR LOSO
94Y-0
0AY-0
0AY-0
0AY-0
0AY-0
0AY-0
0-VM0
0-VM0
0-VM0
3000 37AQ
41.00 31AQ
41.00 43.11A

ALL HOLES SHALL BE DRILLED WITHIN 0.18 MM DIAMETER OF TRUE POSITION AT A MAXIMUM MATERIAL CONDITION RELATIVE TO MATERIAL AREA CENTRES. FINISHED HOLE SIZES SHOWN ARE APPLICABLE AFTER PLATING. 9. HOLES:

THE EDGE FINGER CONTACTS, IF PRESENT, SHALL BE NICKEL-GOLD PLATED WITH A MINIMUM THICKNESS OF 0.25 MICRONS OF GOLD OVER 2.54 MICRONS OF NICKEL

THE PCB SUPPLIER SHALL PROVIDE A SIGNED CERTIFICATE OF COMPLIANCE BY AN AUTHORIZED ON REPRESENTATIVE THE BASE MATERIAL OF PCB SHALL NOT CONTAIN THE ABANDED SUBSTANCE, LISTED IN THE CERTIFICATE OF COMPLIANCE, FINAL PRODUCT MUST BE ROBS COMPLIANT TO ATI ENVIRONMENTAL SPECIFICATION; COD-00

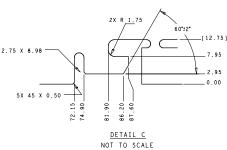
12. INNER LAYER PADS: ALL UNUSED PADS ON THE INNER LAYERS SHOULD BE REMOVED.

ALL ANTIPADS DIAMETERS ON INNER LAYERS MUST NOT VARY MORE THAN +/-0.03MM 13. ANTIPADS: 14. PAD TOLERANCE: ALL OUTER LAYER PADS WITH A DIMENSION EQUAL OR LESS THAN 0.50 MM REQUIRE +/-0.03 MM TOLERANCE. THE REST OF THE PADS SHOULD FOLLOW THE IPC 6012

IT IS ALLOWED TO BREAK PADS AT NON-NECK LOCATION FOR VIAS WITH DIAMMETERS EQUAL OR LESS THAN 0,50 MM AS LONG AS A GUARANTEED ANNULAR RING OF 0,03 MM IS PROVIDED AT NECK LOCATION, SEE IPC.4-800F/2,10 FOR CLASS 2.

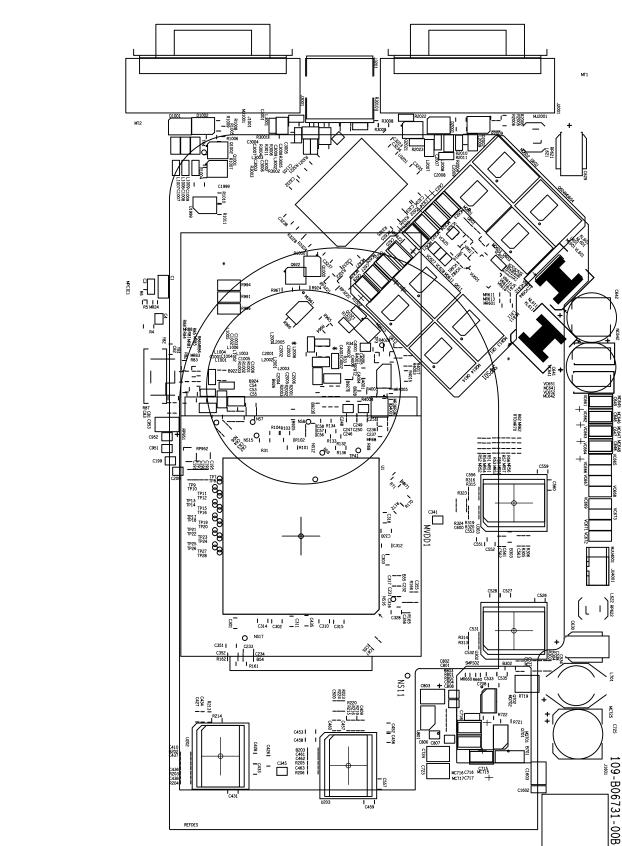
16. TEAR DROPS: DUE TO THE DIFFICULTY WITH THE ETCH FACTOR USING SILVER FINISH, TEARDROPS MUST BE ADDED TO ALL TRACES WIDTHS 0,254MM OR LESS TO ENSURE PLOTTED TRACE WIDTHS AFE MET.

17. Micro Vias: IF PRESENT. ALL MICROVIAS (0.16MM DIA. or LESS) ARE TO BE FILLED WITH A NON CONDUCTIVE MATERIAL AND CAPPED WITH COPPER.



C725



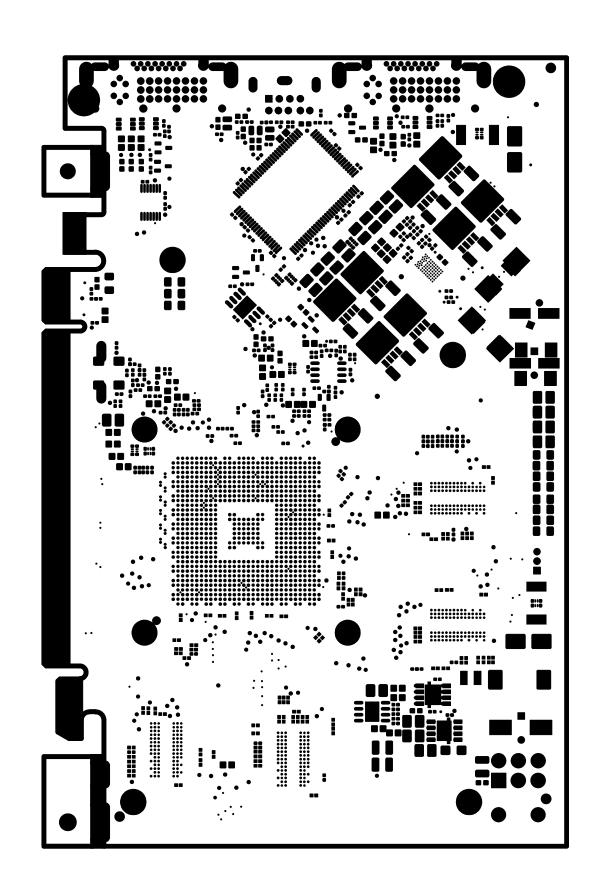


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CSSS4
CS010
CS010
CS041 MR63R63 MR64R64 R85 C921 0921 2022 R977 | U961 R972 MR961 C974 R971 CSLO CSLO R998 R982
R988 G979 R982
R988 G979 R982
R982 G984
R982 G984
R982 G984
R982 G984
R982 G984
R983 R981
R983 R981 - S3 VC674 NS14O 8 2NM BEODUCT LABEL HEEE PLACE PERMANENT P/N' BARCODE' 8929 8930 | | (22) | | (22) | | (23) 9696 | C211 | C215 | B301 | B301 | C213 **⊘**¢ C599 R309 C599 R310 R321 R312 R322 R311 C501 TED TO THE TOTAL T --88 C508 C509 C510 88003 8005 8001 C406 C403 9028 9472 9472 2472 24872 25 2028 26 8472 26 8028 27 8028 27 8028 27 8028 Apparatus Claims of U.S. patent nos. 4,631,603, 4,577,216, 4,819,098, 4,907,093 Licensed for limited viewing uses only R4012 R4001 R4001 R4001 M04004 N04004



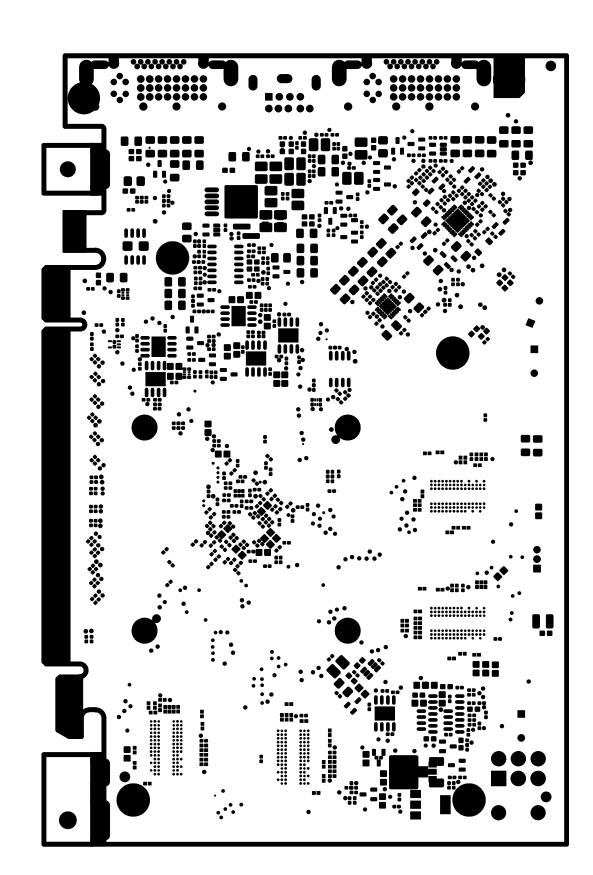


SOLDER MASK TOP FILM 12 OF 13

RH PCIe RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH PN 109-B06731-00B

AUG. 14, 2006

DESIGNER DORINA A.





RH PCIe RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH PN 109-B06731-00B

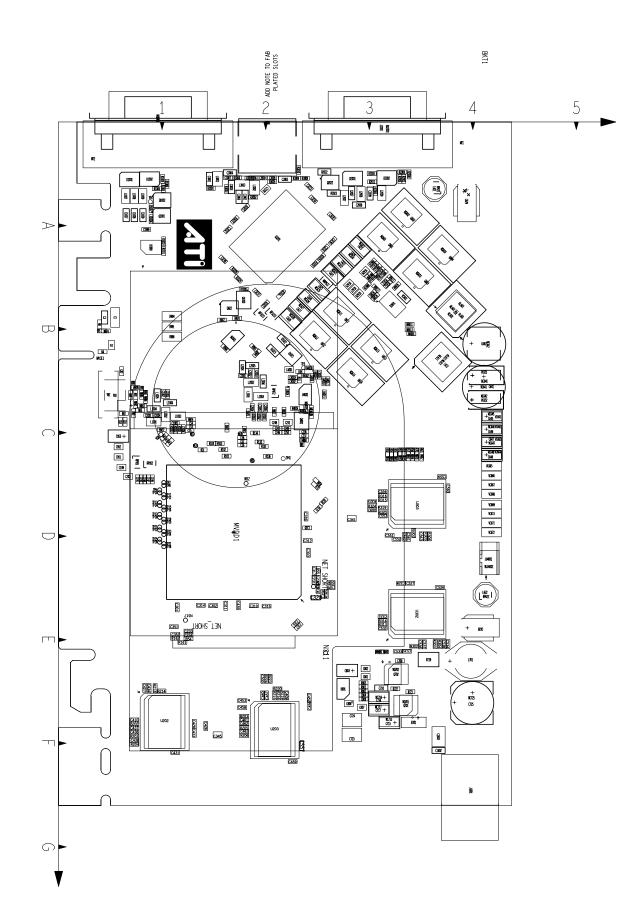
AUG. 14, 2006

EIFW 13 OE 13 SOFDEB WYZK BOLLOM

DESIGNER DORINA A.

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