NV11,2Mx32 SDR, DUAL RGB, TVOUT, PCI.

PCI DEVICE ID 0X0=0X110 FOR NV11.

STRAPS: ADP BIOS, NORMAL PCIAD, 14.318MHZ

STRAP_RAM_TYPE [5:2]=0000 2Mx32 SDR SDRAM

HISTORY REV. A00:
1) A00: Imported P0045-A00

10/03/00 - By EP

2) A00: EXTERNAL DAC - Added HSYNC/VSYNC buffer and filter circuit
3) A00: EXTERNAL DAC - Completed I2C filter circuit to the external DAC
4) A00: NVXX HOST - Changed VDDQ netlist names to 3.3V

10/04/00 - By EP
5) A00: DAC I/O - Changed F200 to MINISMD050 1812 package
6) A00: EXTERNAL DAC - Removed duplicated pullups (R602, R603) and series resistors (R605, R604) for I2C
7) A00: NVXX DAC - Removed ferrite bead connected to XTALOUT on L213
8) A00: NVXX DAC - Removed 10uF (C221) on PLLVDD filter
9) A00: EXTERNAL DAC - Tied U100E.AA2 & V3 to 3.3V
10)A00: EXTERNAL DAC - Tied U100E.AA4 to GND
11)A00: POWER REGULATOR - Changed C922 to 4.7UF X5R
12)A00: POWER REGULATOR - Moved D903 closer to the FETS
13)A00: TV-ENCODERS - Moved C716 to the CHDACVDD side
14)A00: TV-ENCODERS - Added 33R damping resistor to TVECLKIN on R215
15)A00: TV-ENCODERS - Tied BLANK signal on U700 to 10K pullup (R719) to VAA3.3V
16)A00: TV-ENCODERS - Created 0R jumper options for VAAFUSE with R919 & R920
17)A00: TV-ENCODERS - Added 0R strapping resistor (R921) between TVY & CVBS
18)A00: NVXXDAC - Changed C216, C220 from 0.001UF to 150PF
19)A00: NVXXDAC - Changed C215, C219 from 0.1UF to 0.022UF
20)A00: TV-ENCODERS - Changed the following net names:

      TVECLKOUTR to TVECLKOUT
      CVBS_PB to PB
      TVCVB_PBFCC2 to PB_OUT
      TVCFCC2 to TVC_OUT
      TVYFCC2 to TVY_TVCVBS_OUT
      CVBS_PB to CVBS

21)A00: DAC I/O - Added substitute MINISMD035 1210 fuse

10/09/00 - By KL
22)B00: Added nets for NAND tree testing changed package on Y200 to Xtal_2P

23)B00: Connected the anode of D903 to GND instead of NVVDD; Added strapping resistors for the DFP modes.

23)B00: Added C930 and C931 for EMI compliance and C720 and C354 possible use

11/30/2000   By KL
24) B02: Change external DAC Rset (R620) to RES 0603 1% 536 to get RGB DC swing levels within VESA specs.
25) B02: Connect DIODE DUAL SERIES SOT23 BAT54SLT1 (091-10001-0000-000) on D802, D803, D804 to the 3.3V rails instead of the 5V.
26) B02: Add CAP Y5V 0805 4.7UF 10V +80/-20% (037-30475-0048-000) in parallel with C923 to decrease 5V noise to the switcher input from 800mV to 200mV.
27) B02: Add 0.1uF cap option to 5VDAC. Currntly list as no-stuff. this is being added as a CYA for now.
28) B02: Add 680pf stuff option across D903. currently leave as no-stuff untill we get FCC data back from Chuck.
29) B02: Added Series termination resistor R548 to DFPCLK

12/13/00   By KL
1) B03: Added 4.7UF and 2200pf cap for the 3.3Vrail for the protection diodes on the external dac
1) B03: Changed .33UF decoupling caps for NV11 to 0.22UF

{Item}\t{Quantity}\t{Reference}\t{Source Package} {User Define}\t{Value}\t{Assembly}

01/09/01 - By EP

1) B03: Changed C202, C205, C208 from 22pF to 27pF to help
        pass FCC scans.
2) B03: Changed L201, L202, L205, L206, L209, L210 from
        0.082UH to 0.1UH to help pass FCC scans.

602-P0048-0000-B03

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3535 Monroe St
Santa Clara, CA 95051, USA

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Size B	CAGE Code		DWG NO		Rev
Wednesday, May 23, 2001	Scale			Sheet 1	of 14

P200-2
SCREW

P200-1
SCREW

BRACKET
BRACKET

U100A

PCIAD[31:0]

Signal	Pin		Signal	Pin
PCIAD0	AJ28	PCIAD0	VDDQ	AE24
PCIAD1	AH27	PCIAD1	VDDQ	AF11
PCIAD2	AH26	PCIAD2	VDDQ	AF13
PCIAD3	AJ27	PCIAD3	VDDQ	AF18
PCIAD4	AJ24	PCIAD4	VDDQ	AF20
PCIAD5	AH26	PCIAD5	VDDQ	AF24
PCIAD6	AJ24	PCIAD6	VDDQ	AF26
PCIAD7	AK27	PCIAD7	VDDQ	AG25
PCIAD8	AH24	PCIAD8		
PCIAD9	AK23	PCIAD9	NVVDD	AA26
PCIAD10	AK25	PCIAD10	VDD	AE10
PCIAD11	AJ23	PCIAD11	VDD	AF12
PCIAD12	AG23	PCIAD12	VDD	AF19
PCIAD13	AH23	PCIAD13	VDD	AF21
PCIAD14	AH22	PCIAD14	VDD	AF23
PCIAD15	AJ22	PCIAD15	VDD	E10
PCIAD16	AG19	PCIAD16	VDD	E11
PCIAD17	AH19	PCIAD17	VDD	E12
PCIAD18	AJ19	PCIAD18	VDD	E13
PCIAD19	AG18	PCIAD19	VDD	E18
PCIAD20	AK19	PCIAD20	VDD	E19
PCIAD21	AJ18	PCIAD21	VDD	E20
PCIAD22	AH18	PCIAD22	VDD	E21
PCIAD23	AK16	PCIAD23	VDD	K5
PCIAD24	AK17	PCIAD24	VDD	K26
PCIAD25	AK16	PCIAD25	VDD	L5
PCIAD26	AH15	PCIAD26	VDD	L26
PCIAD27	AJ15	PCIAD27	VDD	M5
PCIAD28	AH14	PCIAD28	VDD	M26
PCIAD29	AG15	PCIAD29	VDD	N26
PCIAD30	AG14	PCIAD30	VDD	V5
PCIAD31	AK14	PCIAD31	VDD	V26
			VDD	W5
PCICBE0	AJ24	PCICBE#0	VDD	W26
PCICBE1	AG22	PCICBE#1	VDD	Y5
PCICBE2	AK21	PCICBE#2	VDD	Y26
PCICBE3	AK18	PCICBE#3		
			VD50CLAMP	AA5
PCICLK	AG16	PCICLK	VD50CLAMP	AB6
PCIRST	AK15	PCIRST#	VD50CLAMP	AF8
			VD50CLAMP	F6
PCIGNT	AH11	PCIGNT#		
PCIREQ_	AK11	PCIREQ#		
			VDD33	AD5
PCIFRAME	AH20	PCIFRAME#	VDD33	AD6
PCIIRDY	AG20	PCIIRDY#	VDD33	AE5
PCITRDY	AK20	PCITRDY#	VDD33	AE7
PCIDEVSEL	AG21	PCIDEVSEL#	VDD33	AF4
PCISTOP	AH21	PCISTOP#	VDD33	AF6
PCIPAR	AJ21	PCIPAR	VDD33	AF7
			VDD33	AG5
PCIINTA	AH16	PCIINTA#	VDD33	AG6
AGPRBF	AH12	AGPRBF#	VDD33	G4
AGPWBF	AH13	AGPWBF#	VDD33	H5
AGPPIPE	AG13	AGPPIPE#		
AGPST0	AG12	AGPST0		
AGPST1	AJ12	AGPST1		
AGPST2	AK12	AGPST2		
			GND	N5
AGPADSTB1	AG17	AGPADSTB1	GND	P4
AGPADSTB1	AH17	AGPADSTB1#	GND	P29
AGPADSTB0	AK25	AGPADSTB0	GND	U2
AGPADSTB2	AJ25	AGPADSTB0#	GND	U29
			GND	V2
AGPBUSY	AK13	AGPBUSY#	GND	V29
AGPSTOP_	AJ13	AGPSTOP#		
			TESTMODE0	AK2	TEST0
AGPVREF	AK28	AGPVREF	TESTMODE1	AK29	TEST1

A01

3.3V

C840 0.1UF
C841 0.1UF
C842 0.1UF
C843 0.1UF

5V

C214 0.1UF

3.3V
R624 1K

3.3V
R566 10K

R572 10K

R100 10K

1a. NVXX HOST

5V

C90 10uF   C84 0.1UF   C83 0.1UF   C92 0.1UF   C91 0.1UF   C77 10uF

PCI3.3V

C89 0.1UF   C88 0.1UF   C87 0.1UF

PCB

B05 5V	A58	QPCIAD0
A05 5V	A57	QPCIAD1
B06 5V	A56	QPCIAD2
A06 5V	A55	QPCIAD3
A61 5V	A54	QPCIAD4
B61 5V	A53	QPCIAD5
A62 5V	A52	QPCIAD6
B62 5V	A49	QPCIAD7

AD0 A58 QPCIAD0
AD1 A57 QPCIAD1
AD2 A56 QPCIAD2
AD3 A55 QPCIAD3
AD4 A54 QPCIAD4
AD5 A53 QPCIAD5
AD6 A52 QPCIAD6
AD7 A49 QPCIAD7
AD8 A48 QPCIAD8
AD9 A47 QPCIAD9
AD10 A46 QPCIAD10
AD11 A45 QPCIAD11
AD12 A44 QPCIAD12
AD13 A32 QPCIAD13
AD14 A31 QPCIAD14
AD15 A30 QPCIAD15
AD16 A29 QPCIAD16
AD17 A28 QPCIAD17
AD18 A27 QPCIAD18
AD19 A26 QPCIAD19
AD20 A25 QPCIAD20
AD21 A24 QPCIAD21
AD22 A23 QPCIAD22
AD23 A22 QPCIAD23
AD24 A21 QPCIAD24
AD25 A20 QPCIAD25
AD26 A22 QPCIAD26
AD27 A21 QPCIAD27
AD28 A20 QPCIAD28
AD29 A20 QPCIAD29
AD30 A20 QPCIAD30
AD31 QPCIAD31

A10 VIO
A16 VIO
A19 VIO
A59 VIO
B59 VIO

3.3V KEY
3.3V KEY
3.3V KEY
3.3V KEY

A09 RESERVED
B10 RESERVED
B11 RESERVED
B14 RESERVED
A14 RESERVED
A10 RESERVED

C/BE0# A52 QPCICBE0
C/BE1# B44 QPCICBE1
C/BE2# B33 QPCICBE2
C/BE3# B26 QPCICBE3

CLK B16 QPCICLK
RST# A15 QPCIRST

QPCIREQ   B18 REQ#
A60 REQ64#

GNT# A17 QPCIGNT
ACK64# B60

IDSEL A26 QAGPRBF
FRAME# A34 QPCIFRAME
IRDY# B36 QPCIIRDY
TRDY# A36 QPCITRDY
DEVSEL# A38 QPCIDEVSEL
STOP# A40 QPCISTOP
SDONE A41
SBO# B42
SERR# A42
PAR A43 QPCIPAR

B09 PRSNT1#   INTA# A06 QPCIINTA
B11 PRSNT2#   INTB# B07
INTC# A07
INTD# B08

A01 TRST#   LOCK# B39
B02 TCK   PERR# B40
A03 TMS   TDO B04
A04 TDI

B03 GND   +12V A02
B17 GND
A18 GND   -12V B01   C146 0.01UF
B22 GND
A24 GND
B28 GND
A30 GND   5V KEY B51
B34 GND   5V KEY A51
A35 GND   5V KEY B50
B37 GND   5V KEY A50
A38 GND
B45 GND   3.3V KEY B12
A46 GND   3.3V KEY A12
B49 GND   M66EN/GND
A56 GND
B57 GND

PCB 6 LAYERS

U14

PCIAD0	2	1A1	1B1	54	QPCIAD0
PCIAD1	3	1A2	1B2	53	QPCIAD1
PCIAD2	4	1A3	1B3	52	QPCIAD2
PCIAD3	5	1A4	1B4	51	QPCIAD3
PCIAD4	7	1A5	1B5	50	QPCIAD4
PCIAD5	8	1A6	1B6	48	QPCIAD5
PCIAD6	9	1A7	1B7	47	QPCIAD6
PCIAD7	10	1A8	1B8	46	QPCIAD7
PCICBE0	11	1A9	1B9	45	QPCICBE0
PCIAD8	12	1A10	1B10	44	QPCIAD8
PCIAD9	13	1A11	1B11	44	QPCIAD9
PCIAD10	14	1A12	1B12	42	QPCIAD10

1OE#   NC

PCIAD11	15	2A1	2B1	41	QPCIAD11
PCIAD12	16	2A2	2B2	40	QPCIAD12
PCIAD13	18	2A3	2B3	39	QPCIAD13
PCIAD14	20	2A4	2B4	37	QPCIAD14
PCIAD15	21	2A5	2B5	36	QPCIAD15
PCICBE1	22	2A6	2B6	34	QPCICBE1
PCIPAR	23	2A7	2B7	33	QPCIPAR
PCISTOP	24	2A8	2B8	32	QPCISTOP
PCIDEVSEL	25	2A9	2B9	31	QPCIDEVSEL
PCITRDY	26	2A10	2B10	30	QPCITRDY
PCIIRDY	27	2A11	2B11	29	QPCIIRDY
PCIFRAME	28	2A12	2B12		QPCIFRAME

2OE#   GND
VCC   GND   GND

TSSOP56

5V   D9   VCC4.3V_1
R38 10K   C80 0.1UF
BAT 54 ALT1   VCC4.3V_2

2 PCIDEVSEL_
2 PCITRDY_
2 PCIIRDY_
2 PCIFRAME_
2 PCIAD[31:0]
2 PCIPAR_
2 PCISTOP_
2 PCIREQ_
2 PCIGNT_
2 PCICLK_
2 PCIRST_
2 PCIINTA_
2 PCICBE0_
2 PCICBE1_
2 PCICBE2_
2 PCICBE3_
2 AGPRBF_

U13

PCICBE2	2	1A1	1B1	54	QPCICBE2
PCIAD16	3	1A2	1B2	53	QPCIAD16
PCIAD17	4	1A3	1B3	52	QPCIAD17
PCIAD18	5	1A4	1B4	51	QPCIAD18
PCIAD19	7	1A5	1B5	50	QPCIAD19
PCIAD20	8	1A6	1B6	48	QPCIAD20
PCIAD21	9	1A7	1B7	47	QPCIAD21
PCIAD22	10	1A8	1B8	46	QPCIAD22
PCIAD23	11	1A9	1B9	45	QPCIAD23
AGPRBF	12	1A10	1B10	44	QAGPRBF
PCICBE3	13	1A11	1B11		QPCICBE3
PCIAD24	14	1A12	1B12	42	QPCIAD24

1OE#   NC

PCIAD25	15	2A1	2B1	41	QPCIAD25
PCIAD26	16	2A2	2B2	40	QPCIAD26
PCIAD27	18	2A3	2B3	39	QPCIAD27
PCIAD28	20	2A4	2B4	37	QPCIAD28
PCIAD29	21	2A5	2B5	36	QPCIAD29
PCIAD30	22	2A6	2B6	34	QPCIAD30
PCIAD31	23	2A7	2B7	33	QPCIAD31
PCIREQ	24	2A8	2B8	32	QPCIGNT
PCIGNT	25	2A9	2B9	31	QPCIGNT
PCICLK	26	2A10	2B10	30	QPCICLK
PCIRST	27	2A11	2B11	29	QPCIRST
PCIINTA	28	2A12	2B12		QPCIINTA

2OE#   GND
VCC   GND   GND

TSSOP56

R37 10K   C79 0.1UF

3.3V   J100   5V
R101 2.2K   J101
NO STUFF   D100 BAT 54 ALT1   F ST SHR IRT
F ST SHR IRT   NO STUFF   NO STUFF
GPIO0G

12 GPIO8   R102 100R NO STUFF   GPIO8R
Q100 PMBT2222 NO STUFF

NVVDD

C137	C127	C361	C362	C363	C364	C368	C369	C370	C371
10uF	10uF	2200PF	2200PF	2200PF	2200PF	0.22UF	0.22UF	0.22UF	0.22UF

C354
680PF
NO STUFF

3.3V

C851	C852	C853	C358	C359	C360	C365	C366	C367
10uF	10uF	10uF	2200PF	2200PF	2200PF	0.22UF	0.22UF	0.22UF

3.3V

C139	C901	C902	C150	C149	C148	C147
10uF	0.22UF	2200PF	0.1UF	0.1UF	0.1UF	0.1UF

1y. NVXX DECOUPLING

3.3V

7,11,12,13 TVED[11:0]
7,11 VIPD[7:0]
12 DFPD[11:0]

R119 1 10K 2 DFPD3 R120 1 10K 2
NO STUFF
DFPD[3] STRAP_DFP_WIDTH
0=24-BIT
1=12-BIT

R123 1 10K 2 DFPD2 R124 1 10K 2
NO STUFF
DFPD[2:1] PCI_DEV_ID
PCI_DEV_ID (0x0) = 0x110

R121 1 10K 2 DFPD1 R122 1 10K 2
NO STUFF

R125 1 10K 2 DFPD0
DFPD[0] STRAP_FAST_WRITES
STRAP_FAST_WRITES=0 : FAST WRITE ENABLED
STRAP_FAST_WRITES=1 : FAST WRITE DISABLED

R142 1 10K 2 TVED11
TVED[11] STRAP_HOST=0 : PCI Mode

TVED10 R140 1 10K 2
TVED[10] STRAP_AGPSBA
STRAP_AGPSBA=1 : pipelined only transfers

R137 1 10K 2 TVED9
TVED[9] STRAP_AGP4X
STRAP_AGP4X=0 : AGP4X transfers enabled
STRAP_AGP4X=1 : AGP2X only

R127 1 10K 2 TVED6 R128 1 10K 2
NO STUFF
TVED[6] STRAP_CRYSTAL
STRAP_CRYSTAL=1 : 14.31818MHz

R129 1 10K 2 TVED5 R130 1 10K 2
NO STUFF
TVED[5:2] STRAP_RAM_TYPE

R131 1 10K 2 TVED4 R132 1 10K 2
NO STUFF
0000 = 2Mx32 SDR SDRAM

R133 1 10K 2 TVED3 R134 1 10K 2
NO STUFF

R135 1 10K 2 TVED2 R136 1 10K 2
NO STUFF

TVED1 R118 1 10K 2
TVED[1] STRAP_SUB_VENDOR
STRAP_SUB_VENDOR=1 : Adaptor BIOS

TVED0 R117 1 10K 2
TVED[0] STRAP_AD_SWAP
STRAP_AD_SWAP=1 : PCIAD bus [31:0] normal

1z. NVXX HOST STRAPS

2a. DAC I/O

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nVIDIA

Size	CAGE Code		DWG NO		Rev
C					

Wednesday, May 23, 2001 | Scale | | | Sheet 6 of 14 |

2b. NVXX DAC

U100D

Pin	Signal
AG7	DDCSCL
AH6	DDCSDA
AH5	I2CSCL
AK5	I2CSDA
A8	VIPHCLK
B7	VIPHCTL
A4	VIPHAD0
C4	VIPHAD1
AC3	VIPHAD2
AC4	VIPHAD3
C8	VIPHAD4
AK3	VIPHAD5
AH1	VIPHAD6
AD4	VIPHAD7

CDDCSCL 6
CDDCSDA 6
CSCL 11
CSDA 11

VIPHCLK
VIPHCTL

VIPHAD0 11
VIPHAD1 11
VIPHAD2 11
VIPHAD3 11
VIPHAD4 11
VIPHAD5
VIPHAD6
VIPHAD7

B4 VIPPCLK VIPPCLK
H3 VIPD0 VIPD0
F1 VIPD1 VIPD1
H4 VIPD2 VIPD2
G2 VIPD3 VIPD3
E1 VIPD4 VIPD4
G3 VIPD5 VIPD5
D1 VIPD6 VIPD6
F2 VIPD7 VIPD7
F3 VIPD8 VIPD8
G4 VIPD9 VIPD9

VIPD[7:0] 11

3.3V
L211 150-220R_100MHZ
DACVDD AK9 DACVDD
PLLVDD AK8 PLLVDD

C215 0.022UF
C216 150PF
C217 0.01UF

DACCOMP AG11 DACCOMP
DACVREF AK10 DACVREF
DACRSET AJ10 DACRSET

C218 0.01UF
R212 102R

AJ9 DACGND

BUFFRST_ 13 BUFFRST_ B10 BUF_RST#
TVEVSYNC 13 TVVSYNC AE1 TVVSYNC
TVEHSYNC 13 TVHSYNC AD3 TVHSYNC

DACRED AG10 DACRED DACRED 6
R211 75R

DACGREEN AH10 DACGREEN DACGREEN 6
R213 75R

DACBLUE AH9 DACBLUE DACBLUE 6
R214 75R

TVED0	AJ4	TVD0
TVED1	AK4	TVD1
TVED2	AH4	TVD2
TVED3	AJ3	TVD3
TVED4	AG1	TVD4
TVED5	AG2	TVD5
TVED6	AE2	TVD6
TVED7	AE3	TVD7
TVED8	AF3	TVD8
TVED9	AF1	TVD9
TVED10	AG3	TVD10
TVED11	AH2	TVD11

5,11,12,13 TVED[11:0]

VIDHSYNC AG8 DACHSYNC DACHSYNC 6,11
VIDVSYNC AH7 DACVSYNC DACVSYNC 6

TVECLKOUT 13 TVECLKOUT R215 2 1 33R CTVECLKOUT AD1 TVCLKOUT
CTVECLKIN 13 CTVECLKIN AD2 TVCLKIN

XTALSOUT AH8
XTALSIN AG9
AK7 XTALIN XTALOUT AJ7

R216 220K

A01

3.3V
L212 150-220R_100MHZ
PLLVDD

C219 0.022UF
C220 150PF

100_100_20 14.31818MHZ
Y200
DACXTALIN 1 2 DACXTALOUT

C223 10PF
C224 10PF

Use thick (non-impedance controlled) traces on XTALIN/OUT

TVED[11:0] 5,11,12,13
VIPD[7:0] 11

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Wednesday, May 23, 2001

Size B
CAGE Code
DWG NO
Rev
Scale
Sheet 7 of 14

3a. NVXX FBA/FBB

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Size C	CAGE Code	DWG NO	Rev

Wednesday, May 23, 2001 | Scale | | Sheet 8 of 14

U100B
A01

U100C
A01

FBD[127:0]   10

CFBAA[13:0]   10
FBAA[13:0]   10
CFBARAS_   10
CFBACAS_   10
CFBAWE_   10
CFBACS0_   10
CFBDQS[7:0]   10
FBDQM[7:0]   10
FBDQM[15:8]   10
CFBACKE   10
CFBACLK0   10
CFBACLK1   10

3.3V
R89
1K
11 ROMCS_
FBVREF
ROMCS#

3.3V

| C306 22UF | C383 0.1UF | C308 2200PF | C309 0.1UF | C311 0.1UF |

3.3V

| C335 2200PF | C340 0.1UF | C341 0.1UF | C356 0.1UF | C343 0.1UF | C344 2200PF | C331 2200PF | C316 0.1UF | C373 2200PF | C372 2200PF | C314 0.1UF |

| C355 2200PF | C342 2200PF | C357 2200PF | C301 22UF | C302 0.1UF | C303 2200PF | C315 2200PF |

| C322 2200PF | C323 2200PF | C324 0.1UF | C821 0.1UF | C312 0.1UF | C313 2200PF | C310 2200PF |

| C328 0.1UF | C329 2200PF | C330 0.1UF | C325 2200PF | C326 0.1UF | C317 2200PF |

3b. FB DECOUPLING

3c1. FBA 2MX32 SDRAM

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Size	CAGE Code	DWG NO	Rev
C			A

Wednesday, May 23, 2001

Scale

Sheet 10 of 14

5V   5V

R402   R403
2.2K   2.2K

R404 1 ——/\/\/— 2 33R   SCL   SCL   12,13
R405 1 ——/\/\/— 2 33R   SDA   SDA   12,13

5,7,12,13 TVED[11:0]   TVED[11:0]

U400

TVED0	12	A0	O0	13	VIPD0
TVED1	11	A1	O1	14	VIPD1
TVED2	10	A2	O2	15	VIPD2
TVED3	9	A3	O3	17	VIPD3
TVED4	8	A4	O4	18	VIPD4
TVED5	7	A5	O5	19	VIPD5
TVED6	6	A6	O6	20	VIPD6
TVED7	5	A7	O7	21	VIPD7

TVED8   27   A8
TVED9   26   A9
TVED10 23   A10
TVED11 25   A11

7 VIPHAD2   4   A12
7 VIPHAD3   28 A13
7 VIPHAD4   29 A14
6,7 DACHSYNC 3 A15   NC   1

30 NC/A16
2   NC/A17

8 ROMCS_   22 CE   VDD 32

7 VIPHAD0 24 OE

7 VIPHAD1 31 WE   GND 16

VIPD[7:0]   7

3.3V

C480
0.1UF

4a. ROM VIP & VIDEO IF

NVIDIA Corporation
3535 Monroe St
Santa Clara, CA 95051, USA

*n*VIDIA

| Size C | CAGE Code | DWG NO | | Rev |
| Wednesday, May 23, 2001 | Scale | | Sheet 11 of 14 | |

5b. EXTERNAL RAMDAC

NVIDIA Corporation
3535 Monroe St
Santa Clara, CA 95051, USA

nVIDIA

Size	CAGE Code	DWG NO	Rev
C			A

Wednesday, May 23, 2001 | Scale | | Sheet 12 of 14

5a1. TV ENCODERS

NVIDIA Corporation
3535 Monroe St
Santa Clara, CA 95051, USA

Parts for Chrontel CH7008/8A only

Size	CAGE Code	DWG NO	Rev
C			
Scale		Sheet 13 of 14	

Wednesday, May 23, 2001

R817=((LINEAR OUT/1.26)-1)*100(R818)

Place C923 as close to Q901 as practical

Place C913 as close to Q902 as practical

NVIDIA Corporation
3535 Monroe St
Santa Clara, CA 95051, USA

6a. POWER REGULATOR

Size	CAGE Code	DWG NO		Rev
C				

Wednesday, May 23, 2001

Scale | Sheet 14 of 14