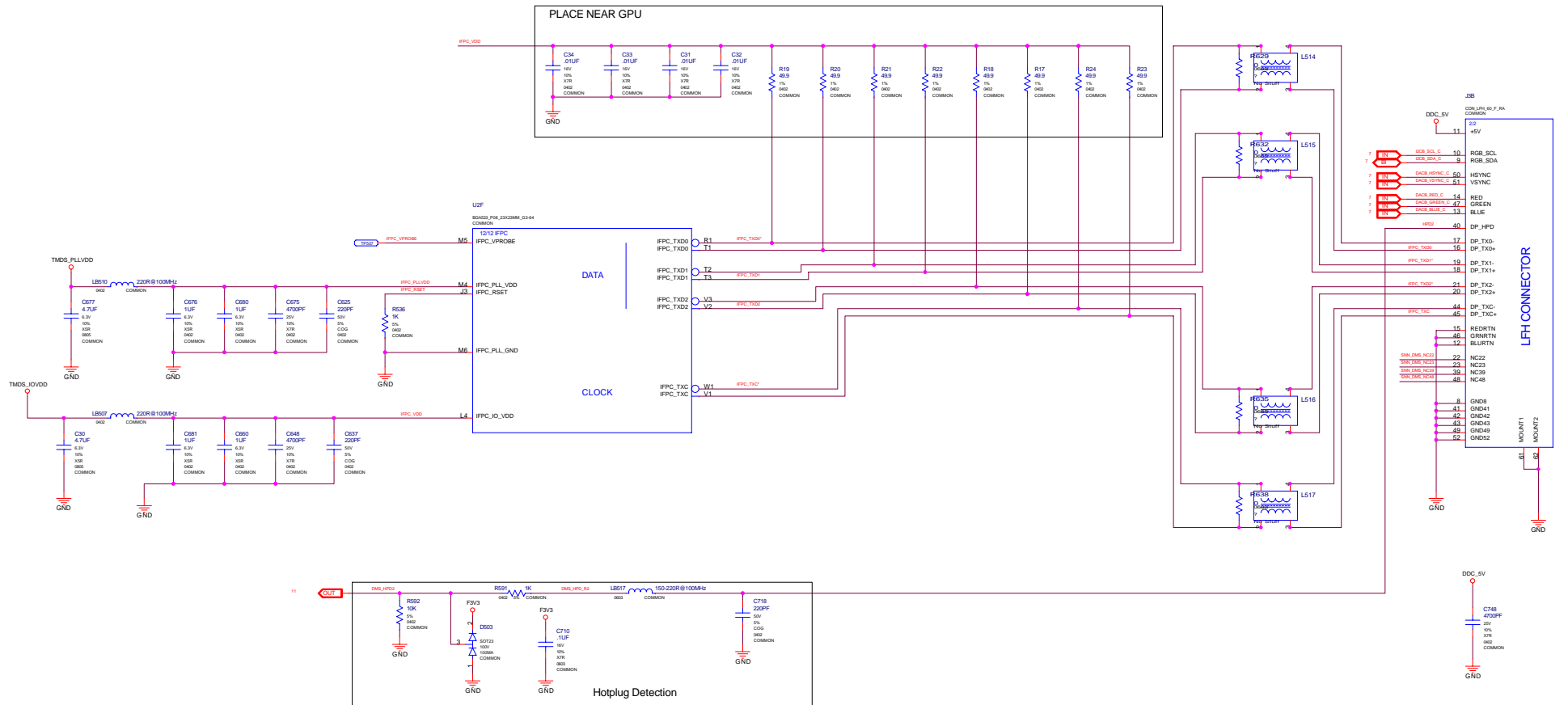


Internal TMDS Link-C DMS Connector

Net Name	Diffpair	NET_SPACING_RULE	Voltage
DIFF_P141009			3.3V
DIFF_P141010			3.3V
DIFF_P141011	DIFF_P141012	200M	
DIFF_P141013	DIFF_P141014	200M	
DIFF_P141015	DIFF_P141016	200M	
DIFF_P141017	DIFF_P141018	200M	
DIFF_P141019	DIFF_P141020	200M	
DIFF_P141021	DIFF_P141022	200M	
DIFF_P141023	DIFF_P141024	200M	
DIFF_P141025	DIFF_P141026	200M	
DIFF_P141027	DIFF_P141028	200M	



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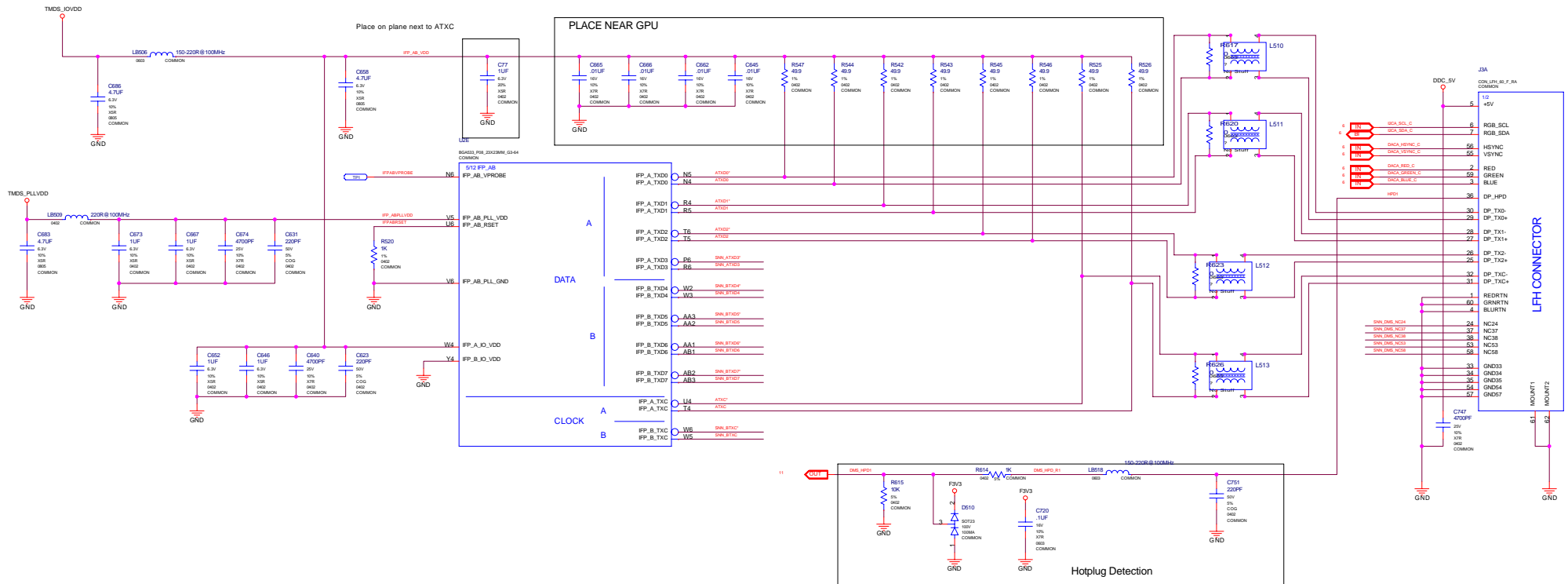


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PAGE DETAIL	TMDS LINK-C

Internal TMDS LINK-A DMS Connector

	Net Name	Diffpair	NET_SPACING_RULE	Voltage
1	RP_HBPL1_VDD			3.3V
2	RP_HB_VDD			3.3V
3	AT1C	AT1C	200M	
4	AT1C1	AT1C	200M	
5	AT1C2	AT1C	200M	
6	AT1C3	AT1C	200M	
7	AT1C4	AT1C	200M	
8	AT1C5	AT1C	200M	
9	AT1C6	AT1C	200M	
10	AT1C7	AT1C	200M	
11	AT1C8	AT1C	200M	
12	AT1C9	AT1C	200M	
13	AT1C10	AT1C	200M	
14	AT1C11	AT1C	200M	
15	AT1C12	AT1C	200M	
16	AT1C13	AT1C	200M	
17	AT1C14	AT1C	200M	
18	AT1C15	AT1C	200M	
19	AT1C16	AT1C	200M	
20	AT1C17	AT1C	200M	
21	AT1C18	AT1C	200M	
22	AT1C19	AT1C	200M	
23	AT1C20	AT1C	200M	
24	AT1C21	AT1C	200M	
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29	AT1C26	AT1C	200M	
30	AT1C27	AT1C	200M	
31	AT1C28	AT1C	200M	
32	AT1C29	AT1C	200M	
33	AT1C30	AT1C	200M	
34	AT1C31	AT1C	200M	
35	AT1C32	AT1C	200M	
36	AT1C33	AT1C	200M	
37	AT1C34	AT1C	200M	
38	AT1C35	AT1C	200M	
39	AT1C36	AT1C	200M	
40	AT1C37	AT1C	200M	
41	AT1C38	AT1C	200M	
42	AT1C39	AT1C	200M	
43	AT1C40	AT1C	200M	
44	AT1C41	AT1C	200M	
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284	AT1C281	AT1C	200M	
285	AT1C282	AT1C	200M	
286	AT1C283	AT1C	2	



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PAGE DETAIL	TMDS Interface

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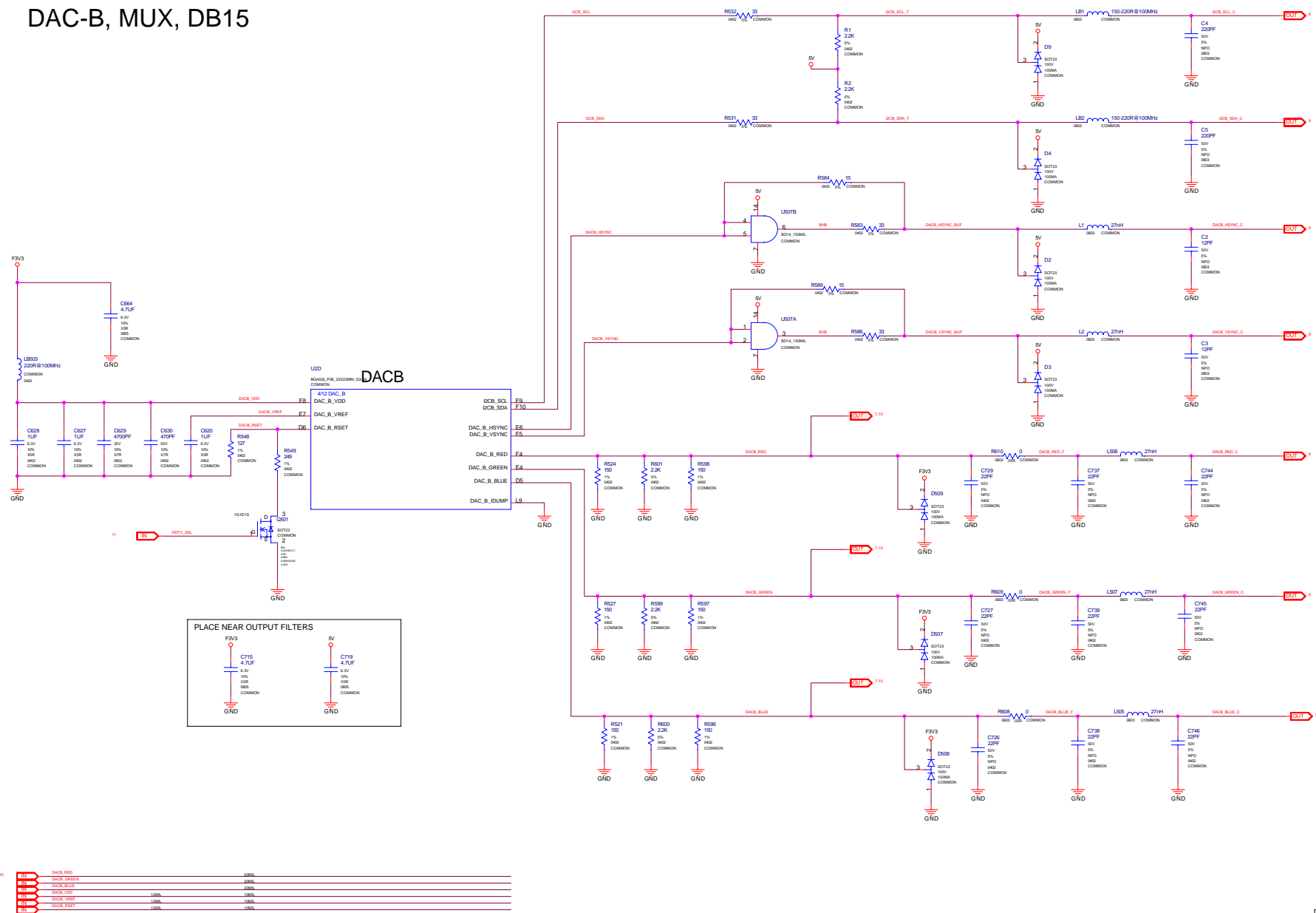
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DAC-B, MUX, DB15



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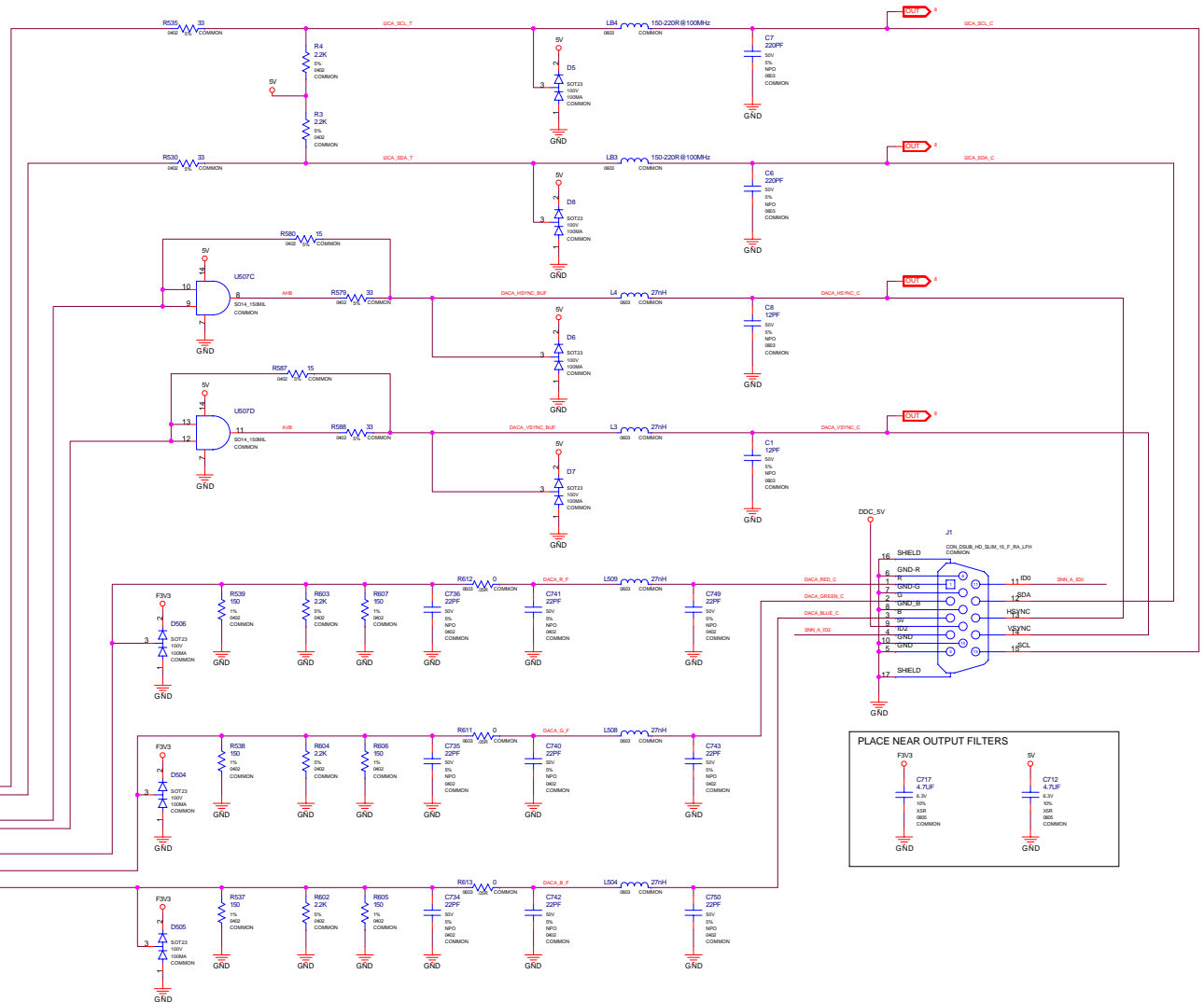
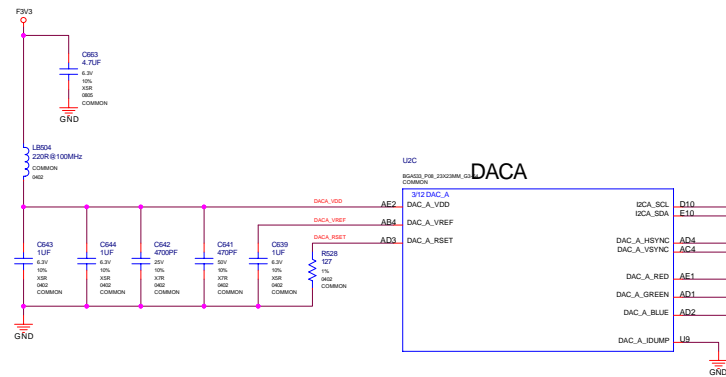
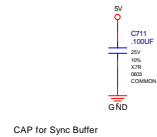
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[illegible]


DAC-A, DB15 Connector

	Net Name	MIN_LINE_WIDTH	NET_SPACING_TYPE
01	DRCA_B0L		100M
02	DRCA_B0L		100M
03	DRCA_V100M		100M
04	DRCA_V100M		100M
05	DRCA_B0L		100M
06	DRCA_B0L		100M
07	DRCA_B0L		100M
08	DRCA_B0L		100M
09	DRCA_V00	100M	100M
01	DRCA_B_F		200M
02	DRCA_B_F		200M
03	DRCA_B_F		200M
01	DRCA_B0D_C		100M
02	DRCA_B0D0D_C		100M
03	DRCA_B0D_C		100M



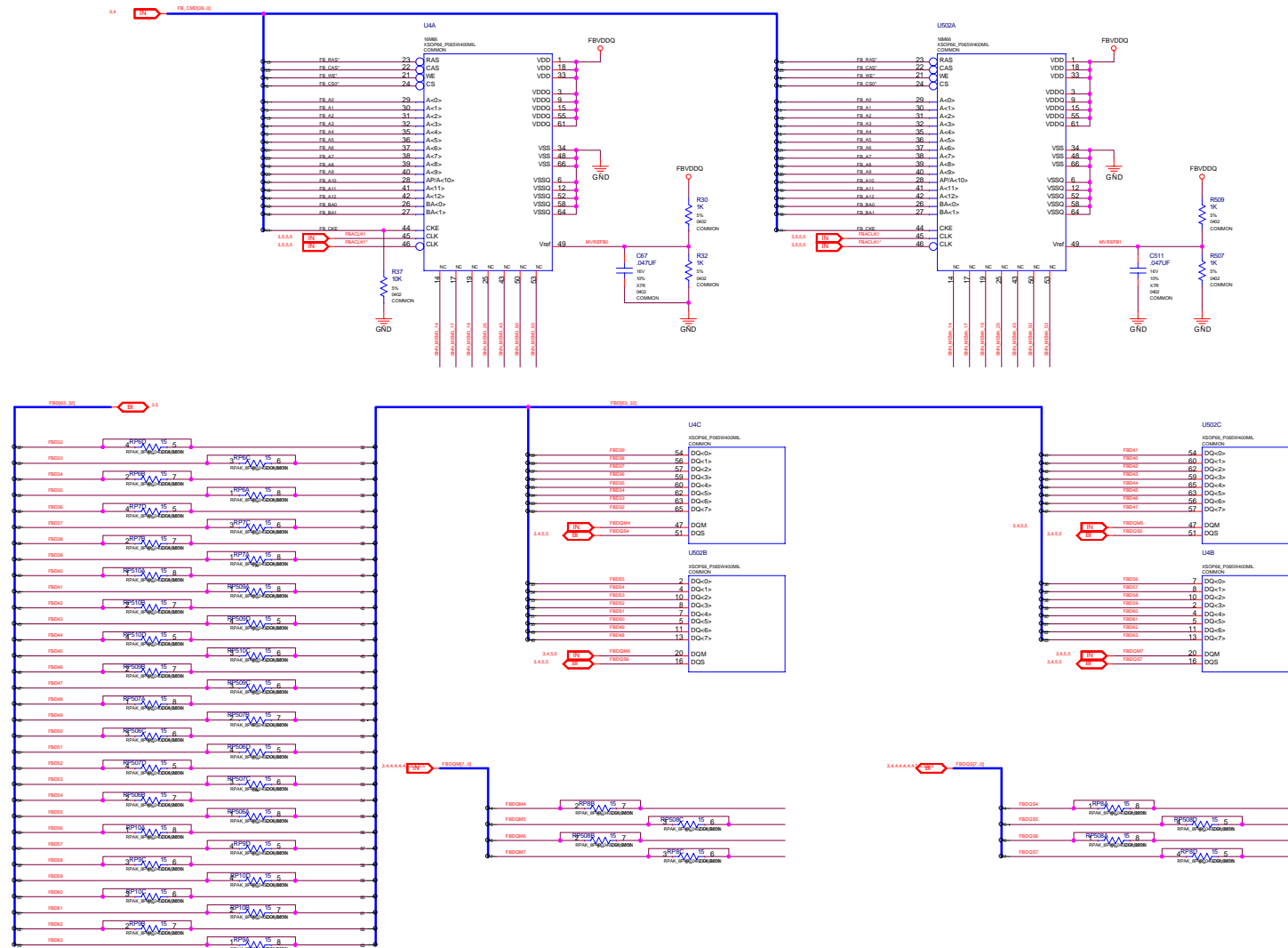
PLACE NEAR OUTPUT FILTERS

Two circuit diagrams illustrating the placement of output filters. The left diagram shows a 5V input connected to a 4.7uF capacitor (C717) which is connected to GND. The right diagram shows a 5V input connected to a 4.7uF capacitor (C712) which is connected to GND. Both capacitors are labeled with 4.7uF, 10%, XGR, and 0805 COMMON.

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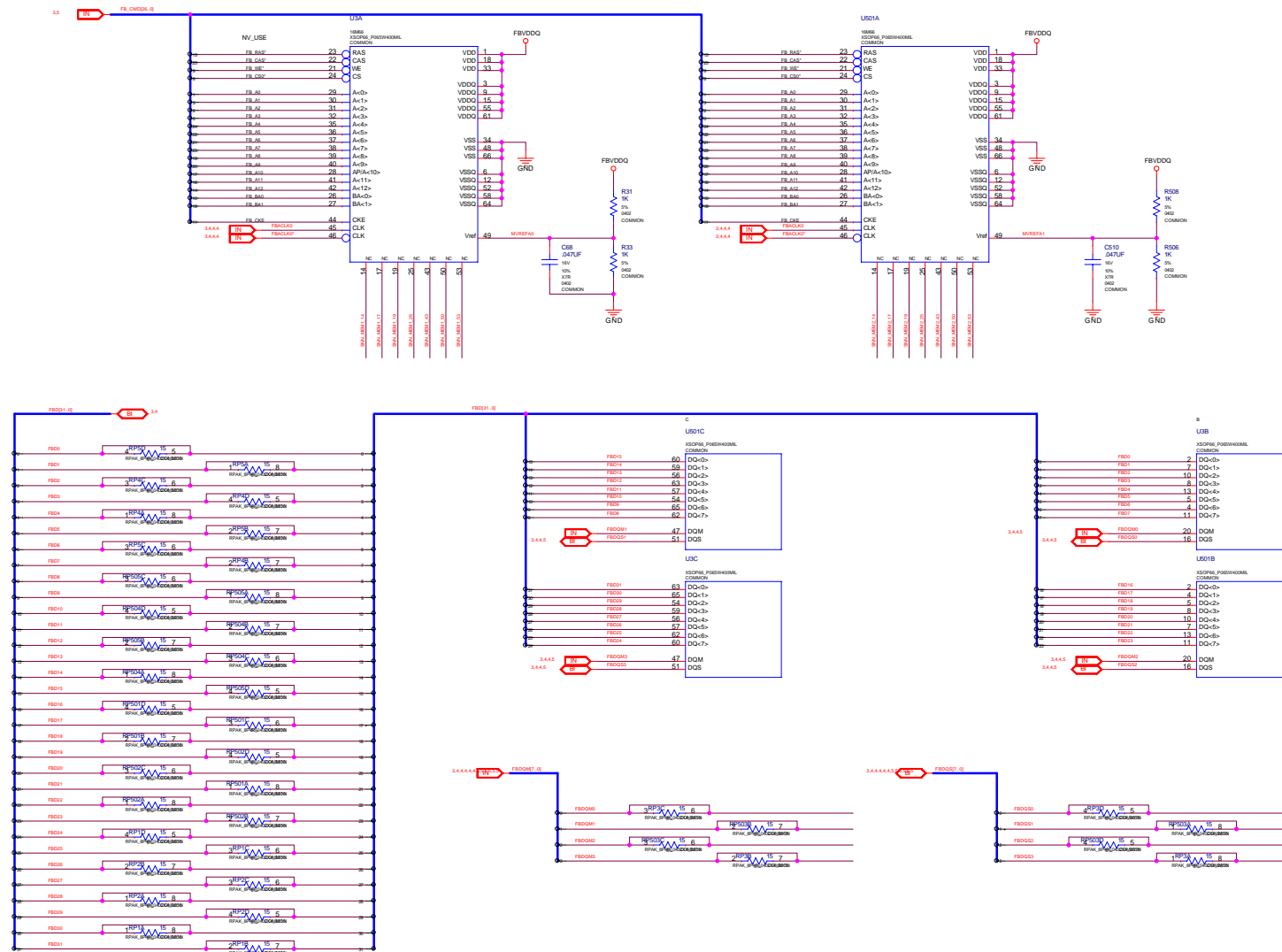
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Memory Bit 32..63

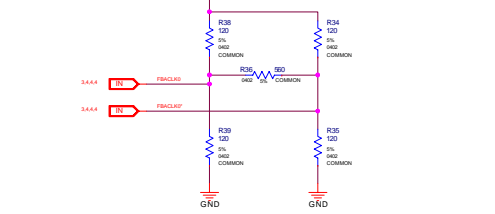
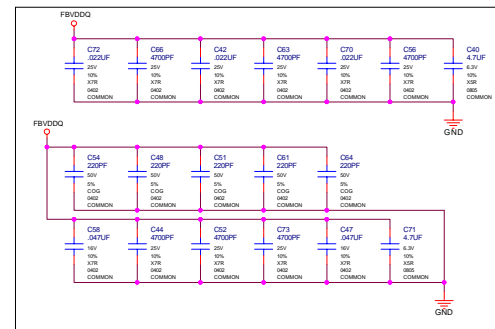
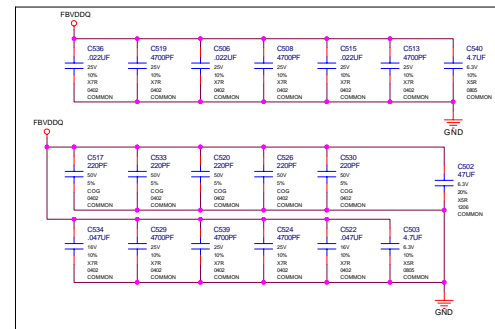


Net Name **Diffpair** **NET_SPACING_RULE**

Memory Bit 0..31



Net Name	Dffpair	NET_SPACING_RULE
34.44	FBVDDQ	34.44
34.44	FBVSSQ	34.44
34.44	FBVDDQ	34.44
34.44	FBVSSQ	34.44
34.44	FBVDDQ	34.44
34.44	FBVSSQ	34.44



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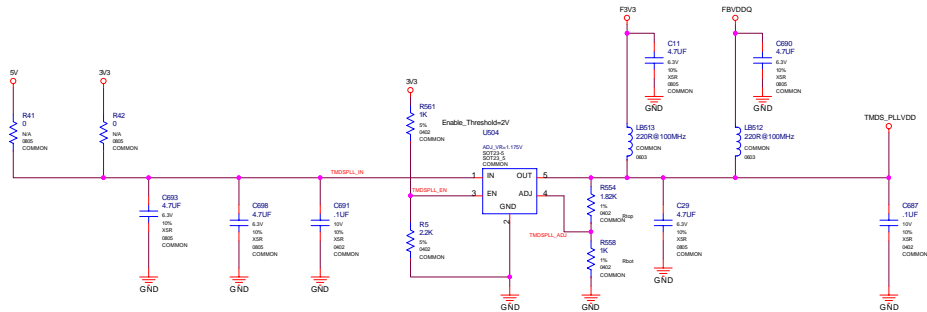
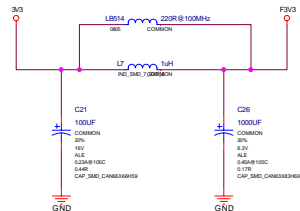
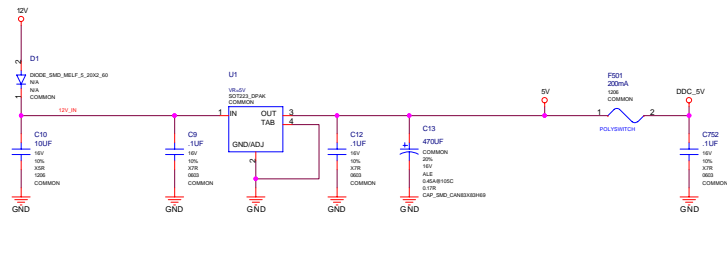
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Memory bit 0..31

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PowerSupplyII: 5V, DDC5V, A3V3, F3V3, TMDS_PLLVDD

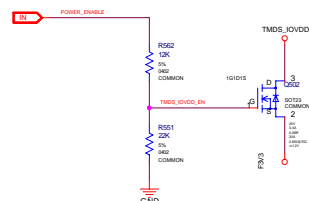


TMDS_PLLVDD

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

$$2.5 = V_{Ref} * (1 + R_{top}/R_{bot})$$

Net Name	NET_PHYSICAL_TYPE	Voltage
5V	5V	5V
DDC_5V	DDC_5V	5V
F3V3	F3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	3.3V
12V	12V_IN	12V
TMDS_IOVDD	TMDS_IOVDD	3.3V

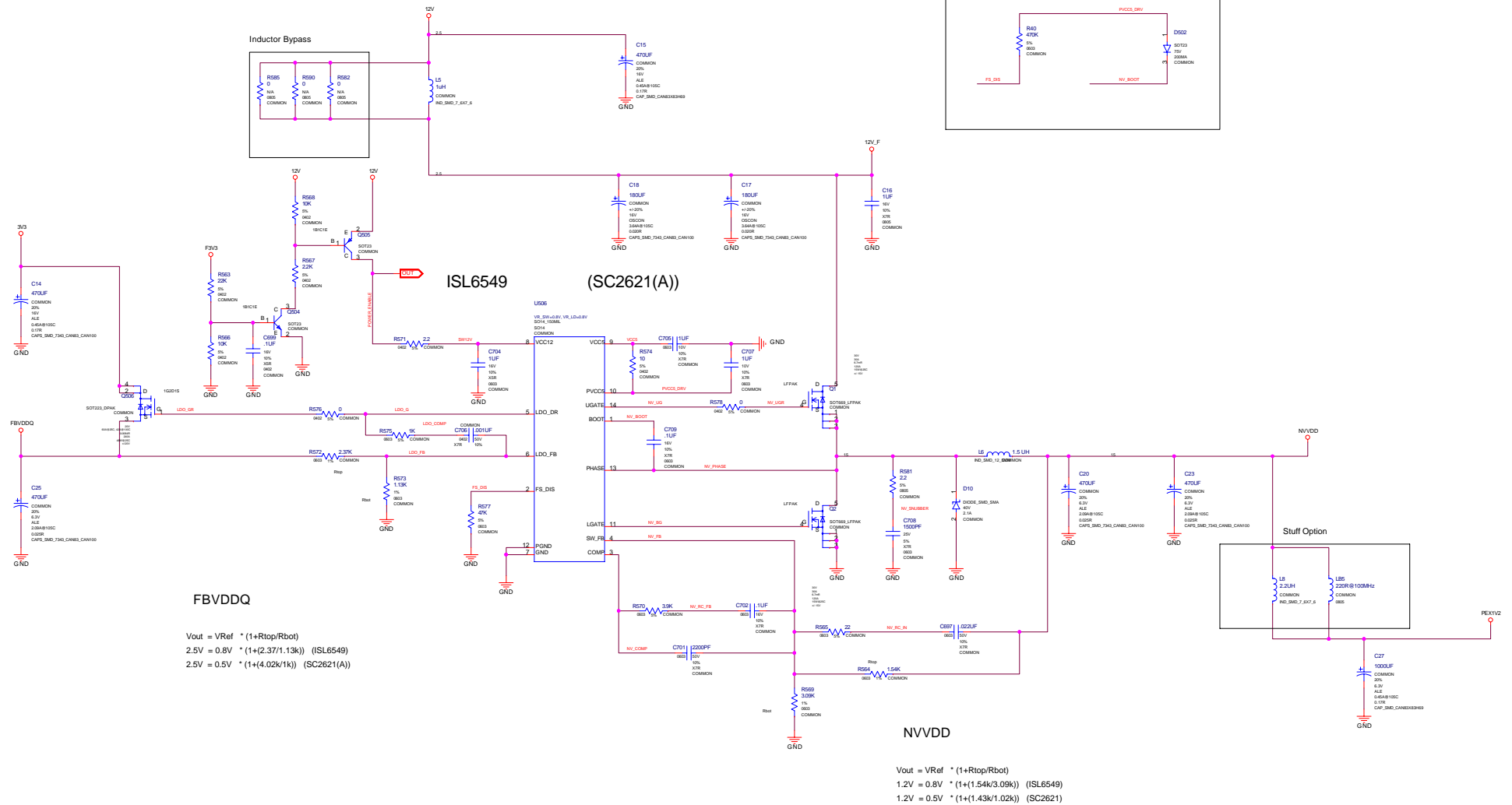


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOA NOT FINAL
TRADE DETAIL	P0605222X 5V, DDC5V, A3V3, F3V3, TMDS_PLLVDD

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TD		DATE	3/08/2004

PowerSupply1: NVVDD, FBVDDQ



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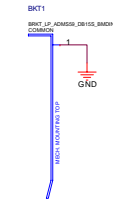
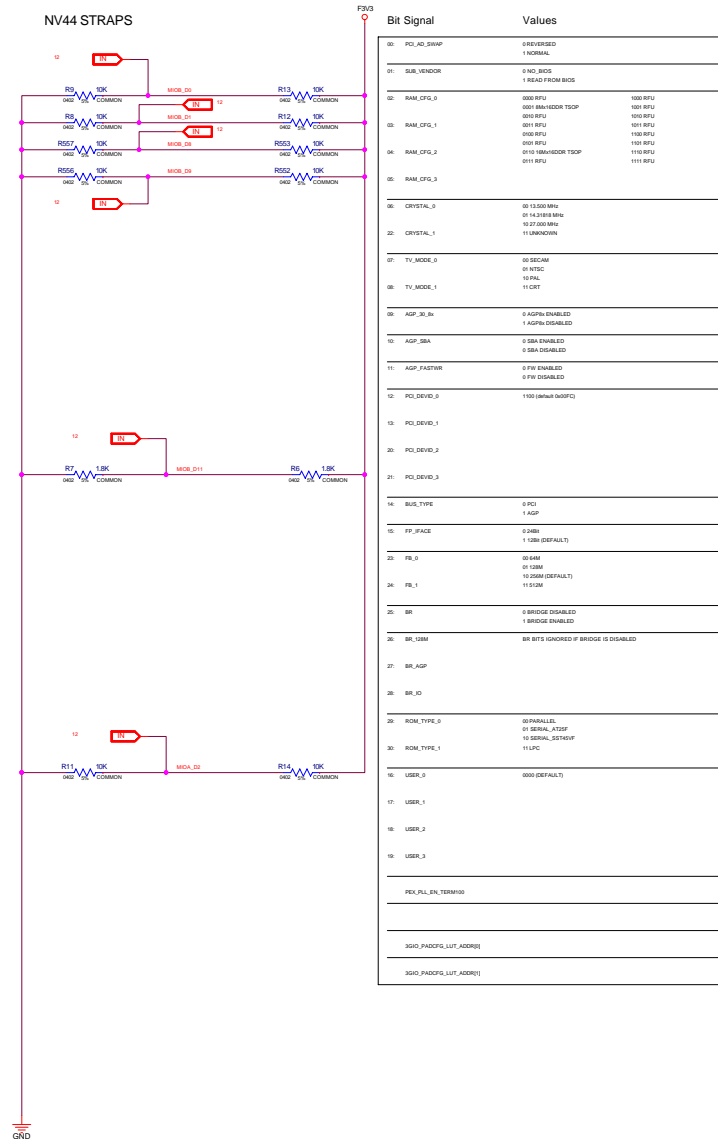
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STRAPS, Mechanical Parts



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	STRAPS, Mechanical Parts

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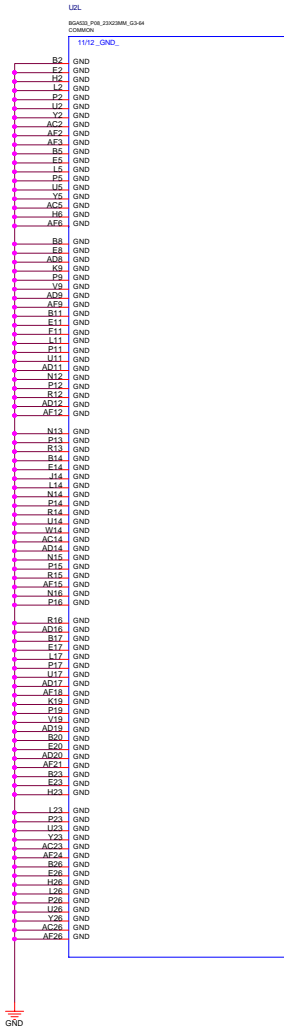
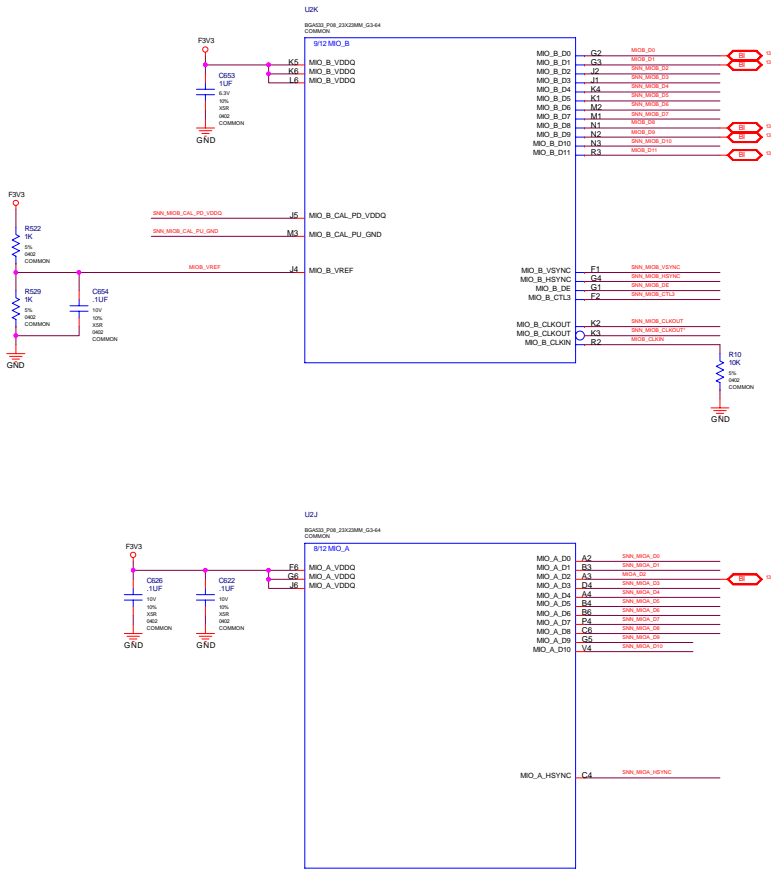
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NAME	DATE	FILE NO.

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MIOA, MIOB Interface, LPC-ROM



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PADE DETAIL	MIOA, MIOB Interface; LPC-ROM

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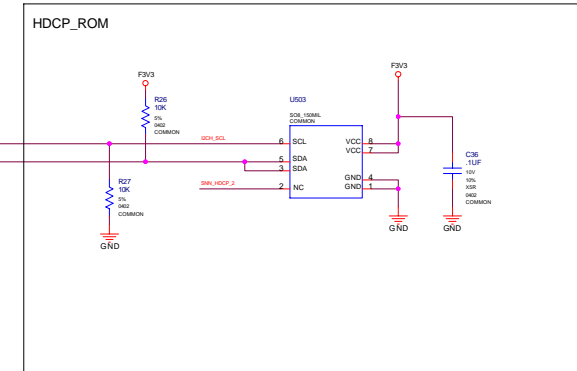
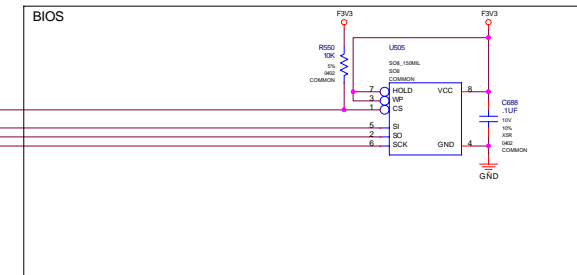
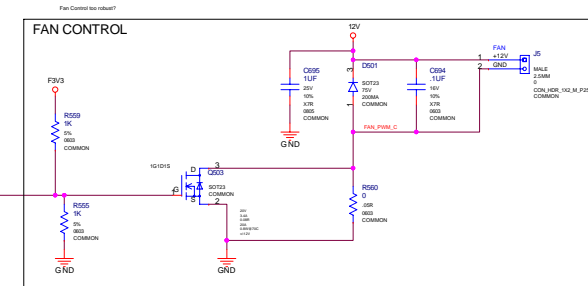
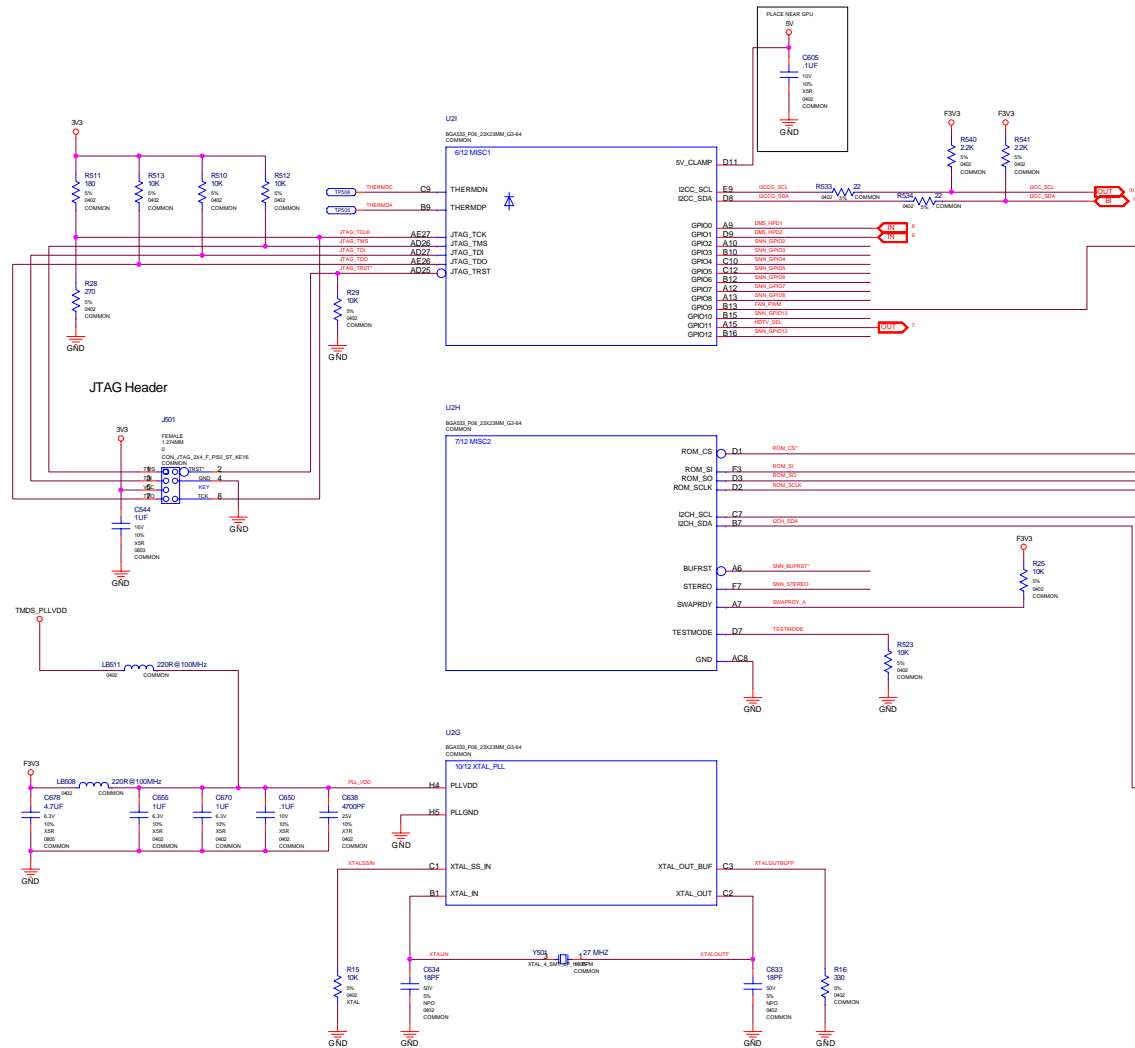



NV_PN 600-f0ppp-xxxx-vvv

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7000E			

XTAL, GPIO, BIOS, Fan Control, JTAG Headers

Net Name	NET_PHYSICAL_TYPE	NET_SPACING_RULE
BTAIN	DRILL_TRACE	20MIL
BTAINDRILL	DRILL_TRACE	20MIL
BTAINVIA	DRILL_TRACE	20MIL
BTAINPOLYVIA	DRILL_TRACE	20MIL



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P283: LOW PROFILE NV44/G3-64, TSOP MEMORY x16

REV HISTORY

- Page1: P262 Overview
- Page2: PCI Express Interface
- Page3: Frame Buffer Interface
- Page4: Memory 1st bank 0..31
- Page5: Memory 1st bank 32..63
- Page6: DACA VGA
- Page7: DACB RGB
- Page8: TMDS LINK A
- Page9: TMDS LINK C
- Page10:TVO Connector
- Page11: GPIO, PLL, BIOS
- Page12: MIO
- Page13: STRAPS, Mechanical Parts
- Page14: NVVDD & FBVDDQ
- Page15: TMDS_IOVDD,TMDS_PLLVDD,5V,F3V3


REV	VARIANT	NVPN	ASSEMBLY
8	BASE	600f0ppp-xxxx-ww	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	WORKSTATION_SKU00	600502B3-0000-100	N/S SKU00
2	001	600-102B3-0001-000	SR0.01 - NV44 G3-64, VGA+HDTV, 350275MHz, 64 bit 64MB MEMORY INTERFACE
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
TRADE DETAIL	P283 Overview

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