

G94-P545-A01 - GDDR3, DVI/VGA + DVI/VGA + HDTV/SDTV-Out

REV	VARIANT	NVPIN	ASSEMBLY
B	BASE	600-10545-xxxx-100	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SRU0100	600-10545-9100-100	G94-400 600MHz/1000MHz 512MB 18MA32 BGAT136 GDDR3, DVI+DL+DVI+DL+HDTV-Out (Bring Up SRU)
2	SRU0000	600-10545-0000-100	G94-400 600MHz/1000MHz 512MB 18MA32 BGAT136 GDDR3, DVI+DL+DVI+DL+HDTV-Out
3	SRU0010	600-10545-0010-100	G94-300 600MHz/800MHz 512MB 18MA32 BGAT136 GDDR3, DVI+DL+DVI+DL+HDTV-Out
4	SRU0020	600-10545-0020-100	G94-200 600MHz/800MHz 384MB 18MA32 BGAT136 GDDR3, DVI+DL+DVI+DL+HDTV-Out
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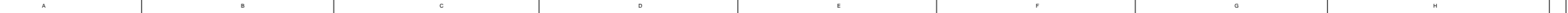
V127-0A Base on P545

- 1.PAGE18: ADD Display port circuit
2.PAGE21: ADD GPIO circuit
3.PAGE 21: change SPDIF circuit
4.PAGE 27: remove PEX_VDD power switch circuit
5.PAGE 27: remove IFP_PLLVDD/2V5 power switch circuit cahnge APL5713 and APL5910 circuit
6.PAGE 28: remove FBVDDQ power switch circuit change APW7067N power circuit
7.PAGE 29: remove NVVDD VID circuit
8.PAGE 30: change NNVDD POWER APW7088 circuit
9.PAGE 16/17 : ADD EMI bridge R
10.PAGE 17 CO-LAYOUT HDIM CONNECT
11.PAGE 15 remove J2 D_SUB SLIM CONNECT
12.PAGE 29 ADD CH7322 circuit

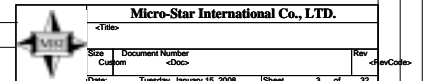
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PAGE DETAIL	Overview

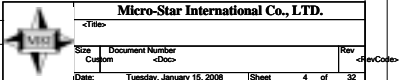
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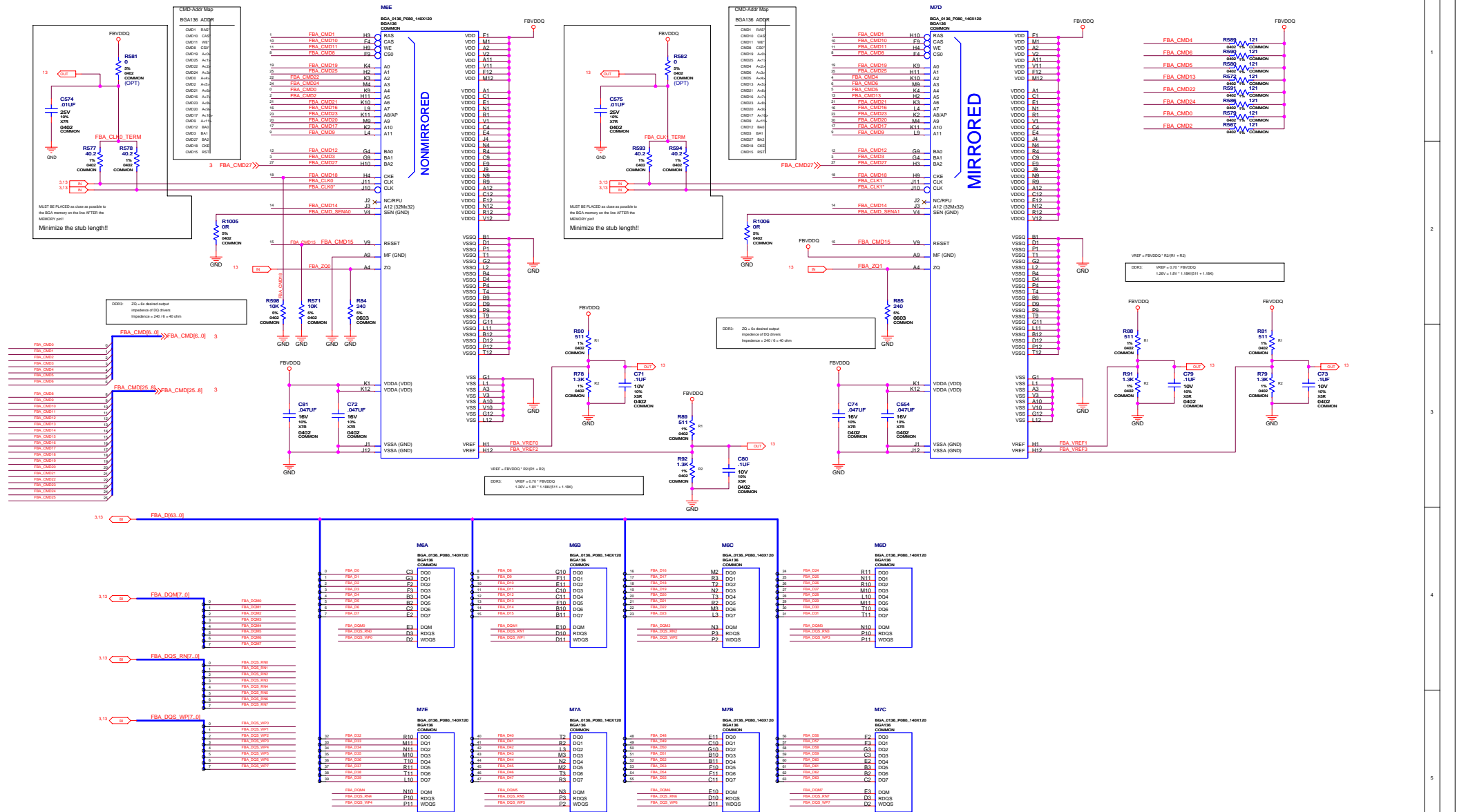
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CALIBRATION PIN	DOE3
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FB_CALX_PU_GND	40
FB_CALX_TERM_GND	40
VREF RATIO	0.7 FB/VDDQ

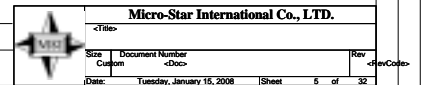


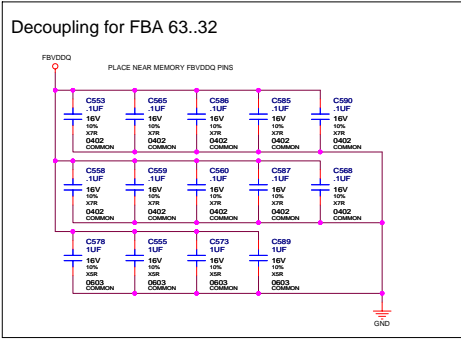
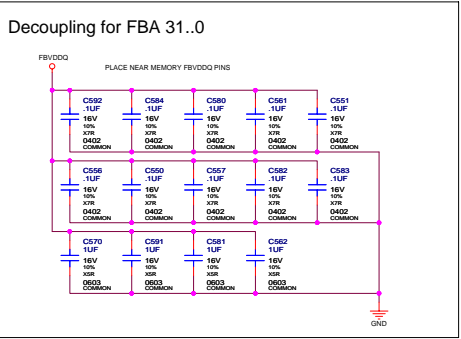




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PAGE DETAIL	FBA Partion





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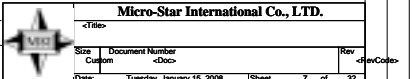
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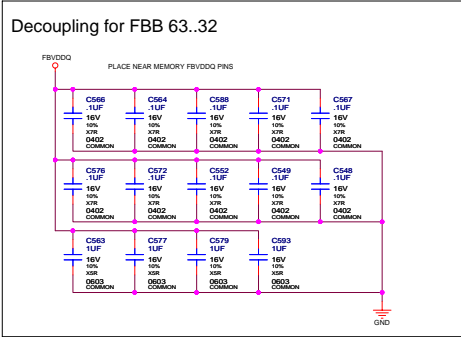
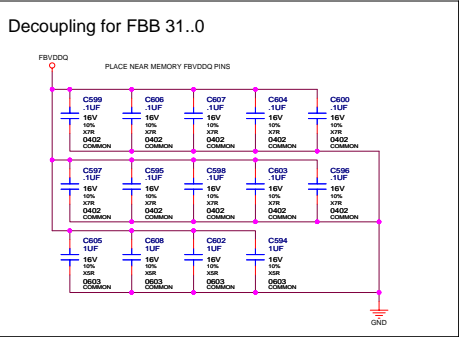


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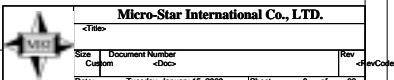
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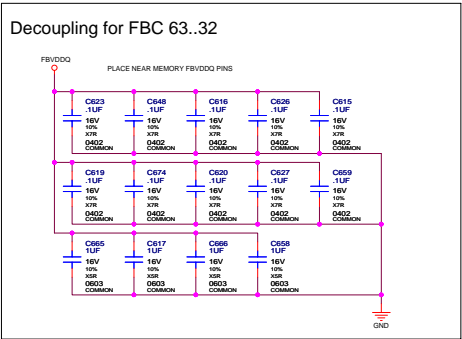
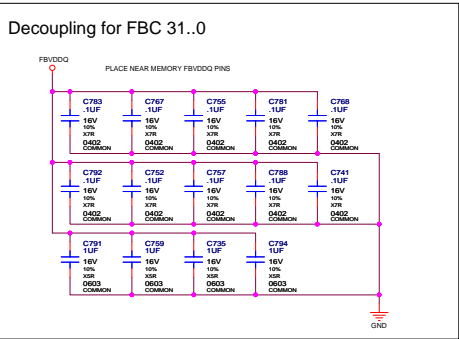
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FBB Partition Decoupling



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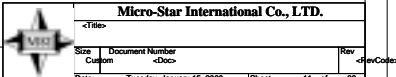
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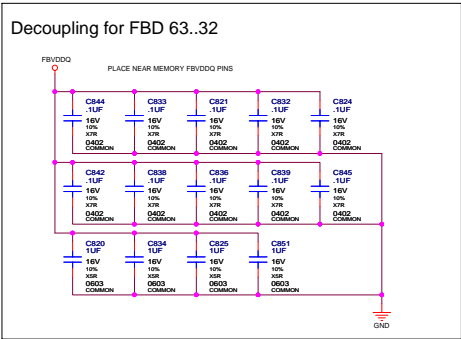
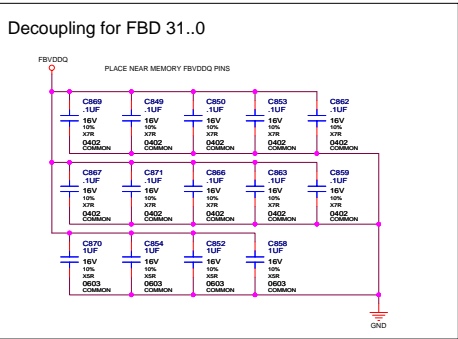


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FBD Partition Decoupling









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NET RULES for FBA and FBB

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
3.5  FBA_CLK0	1	80OHM	FBA_CLK0
3.5  FBB_CLK0	1	80OHM	FBA_CLK0
3.5  FBA_CLK0_TERM	1	80OHM	FBA_CLK0
3.5  FBA_CLK1	1	80OHM	FBA_CLK1
3.5  FBB_CLK1	1	80OHM	FBA_CLK1
3.5  FBA_CLK1_TERM	1	80OHM	FBA_CLK1









NET	NV_CRITICAL_NET	IMPEDANCE
3.5  FBA_DQS_WRT0	1	80OHM
3.5  FBB_DQS_WRT0	1	80OHM
3.5  FBA_DQS0	1	80OHM
3.5  FBB_DQS0	1	80OHM
3.5  FBA_VREF	1	80OHM

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
3.7  FBB_CLK0	1	80OHM	FBB_CLK0
3.7  FBB_CLK0_TERM	1	80OHM	FBB_CLK0
7  FBB_CLK0_TERM	1	80OHM	FBB_CLK0
7  FBB_CLK1	1	80OHM	FBB_CLK1
7  FBB_CLK1_TERM	1	80OHM	FBB_CLK1
7.13  FBB_CLK1_TERM	1	80OHM	FBB_CLK1









NET	NV_CRITICAL_NET	IMPEDANCE
3.7  FBB_DQS_WRT0	1	80OHM
3.7  FBB_DQS_WRT0	1	80OHM
3.7  FBB_DQS0	1	80OHM
3.7  FBB_VREF	1	80OHM

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
3  FB_PLAVDD0	12MIL	1.1V	0.00A
3  FB_VREF	12MIL	1.20V	0.00A
5  FBA_VREF0	12MIL	1.20V	0.00A
5  FBB_VREF0	12MIL	1.20V	0.00A
5  FBA_VREF2	12MIL	1.20V	0.00A
5  FBB_VREF2	12MIL	1.20V	0.00A
5  FBA_VREF3	12MIL	1.20V	0.00A
5  FBB_VREF3	12MIL	1.20V	0.00A
5  FBA_Z00	12MIL	1.20V	0.00A
5  FBB_Z00	12MIL	1.20V	0.00A
7  FBB_VREF0	12MIL	1.20V	0.00A
7  FBB_VREF2	12MIL	1.20V	0.00A
7  FBB_VREF3	12MIL	1.20V	0.00A
7  FBB_VREF3	12MIL	1.20V	0.00A
7  FBB_Z00	12MIL	1.20V	0.00A
7  FBB_Z00	12MIL	1.20V	0.00A


















NET RULES for FBC and FBD

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
4.9  FBC_CLK0	1	80OHM	FBC_CLK0
4.9  FBB_CLK0	1	80OHM	FBC_CLK0
4.9  FBC_CLK0_TERM	1	80OHM	FBC_CLK0
9  FBC_CLK0_TERM	1	80OHM	FBC_CLK0
4.9  FBC_CLK1	1	80OHM	FBC_CLK1
4.9  FBB_CLK1	1	80OHM	FBC_CLK1
4.9  FBC_CLK1_TERM	1	80OHM	FBC_CLK1
9  FBC_CLK1_TERM	1	80OHM	FBC_CLK1

NET	NV_CRITICAL_NET	IMPEDANCE
4.9  FBC_DQS_WRT0	1	80OHM
4.9  FBB_DQS_WRT0	1	80OHM
4.9  FBC_DQS0	1	80OHM
4.9  FBB_DQS0	1	80OHM
4.9  FBC_VREF	1	80OHM

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
4.11  FBC_CLK0	1	80OHM	FBC_CLK0
4.11  FBB_CLK0	1	80OHM	FBC_CLK0
11  FBC_CLK0_TERM	1	80OHM	FBC_CLK0
11  FBC_CLK0_TERM	1	80OHM	FBC_CLK0
3.7.1  FBC_CLK1	1	80OHM	FBC_CLK1
3.7.1  FBB_CLK1	1	80OHM	FBC_CLK1
3.7.1  FBC_CLK1_TERM	1	80OHM	FBC_CLK1
7.13  FBC_CLK1_TERM	1	80OHM	FBC_CLK1

NET	NV_CRITICAL_NET	IMPEDANCE
4.11  FBC_DQS_WRT0	1	80OHM
4.11  FBB_DQS_WRT0	1	80OHM
4.11  FBC_DQS0	1	80OHM
4.11  FBB_DQS0	1	80OHM
4.11  FBC_VREF	1	80OHM

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
4  FB_PLAVDD1	12MIL	1.1V	0.00A
9  FBC_VREF0	12MIL	1.20V	0.00A
9  FBB_VREF0	12MIL	1.20V	0.00A
9  FBC_VREF2	12MIL	1.20V	0.00A
9  FBB_VREF2	12MIL	1.20V	0.00A
9  FBC_VREF3	12MIL	1.20V	0.00A
9  FBB_VREF3	12MIL	1.20V	0.00A
9  FBC_Z00	12MIL	1.20V	0.00A
9  FBB_Z00	12MIL	1.20V	0.00A
11  FBC_VREF0	12MIL	1.20V	0.00A
11  FBB_VREF0	12MIL	1.20V	0.00A
11  FBC_VREF2	12MIL	1.20V	0.00A
11  FBB_VREF2	12MIL	1.20V	0.00A
11  FBC_VREF3	12MIL	1.20V	0.00A
11  FBB_VREF3	12MIL	1.20V	0.00A
11  FBC_Z00	12MIL	1.20V	0.00A
11  FBB_Z00	12MIL	1.20V	0.00A

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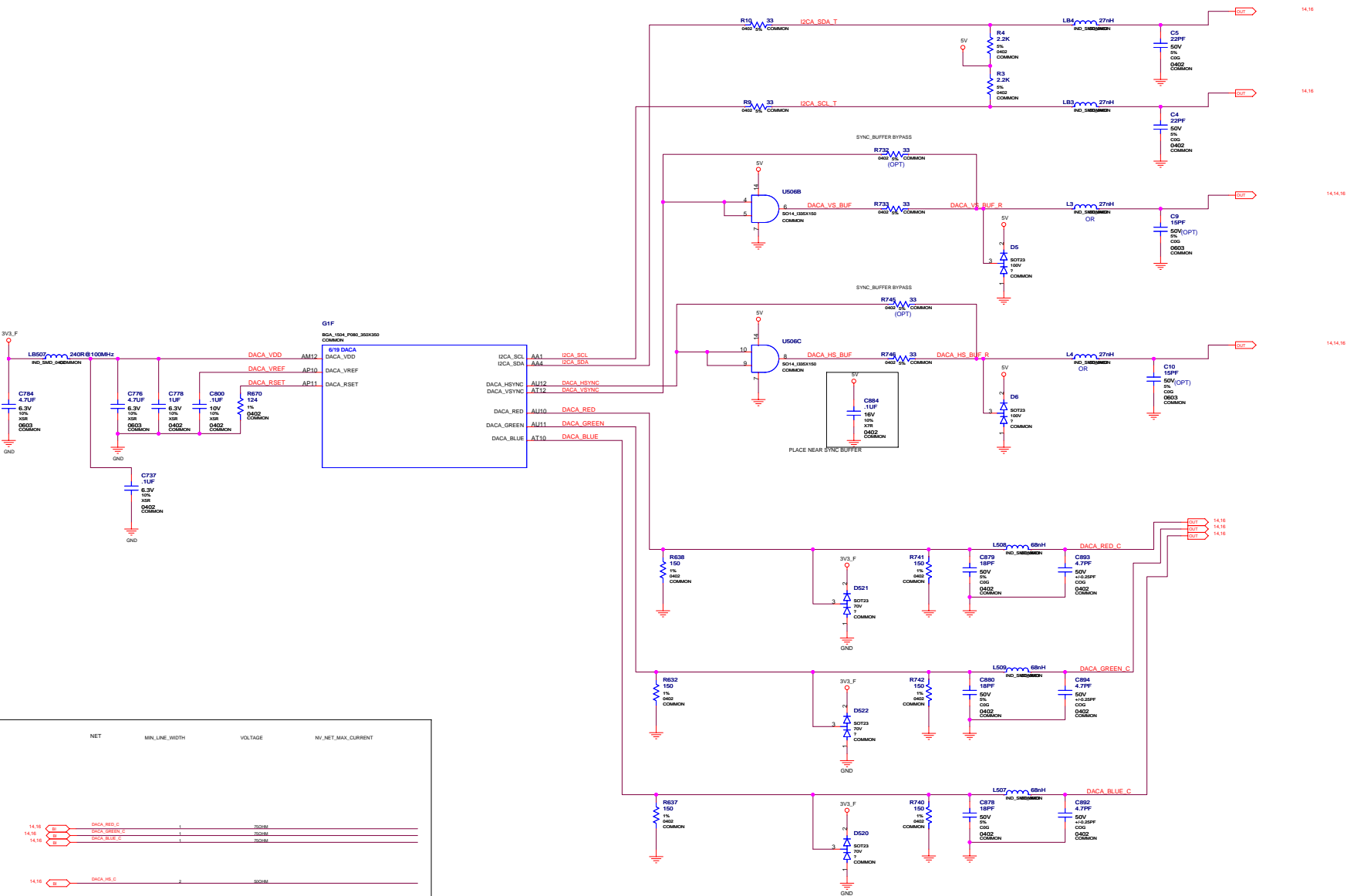
ASSEMBLY PAGE DETAIL PCB BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL FB Net Properties



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DACA RGB-FILTER



NET	MIN_LINE_WIDTH	VOLTAGE	WIRE_MAX_CURRENT
14.16	1	3.3V	300M
14.16	1	3.3V	300M
14.16	1	3.3V	300M
14.16	2	3.3V	300M
14.16	2	3.3V	300M

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DACA Interface

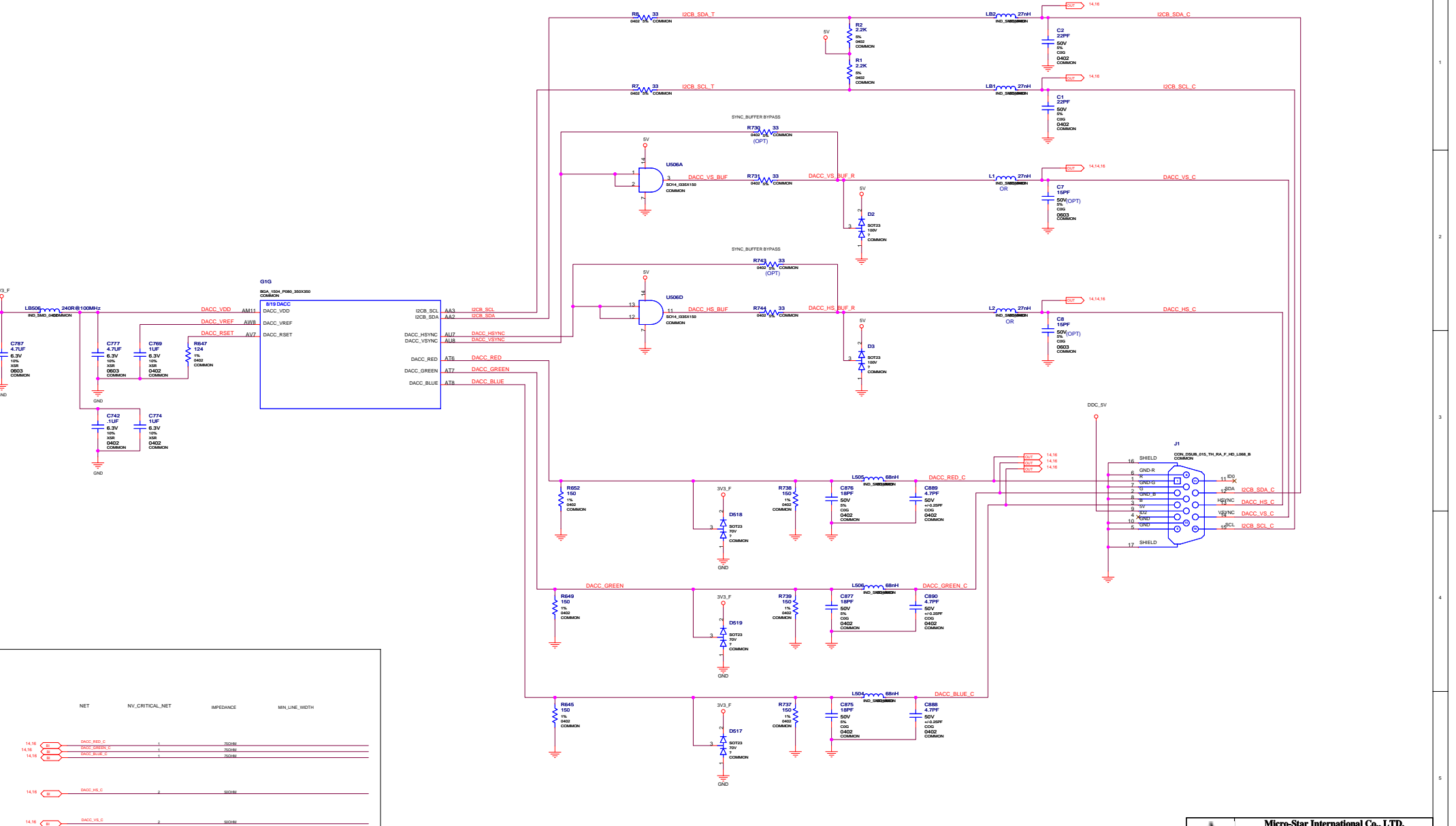
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DACC RGB-FILTER



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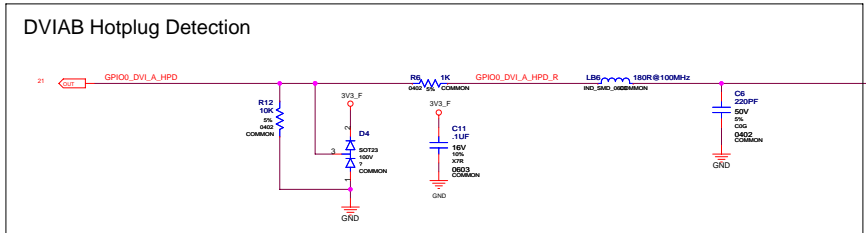


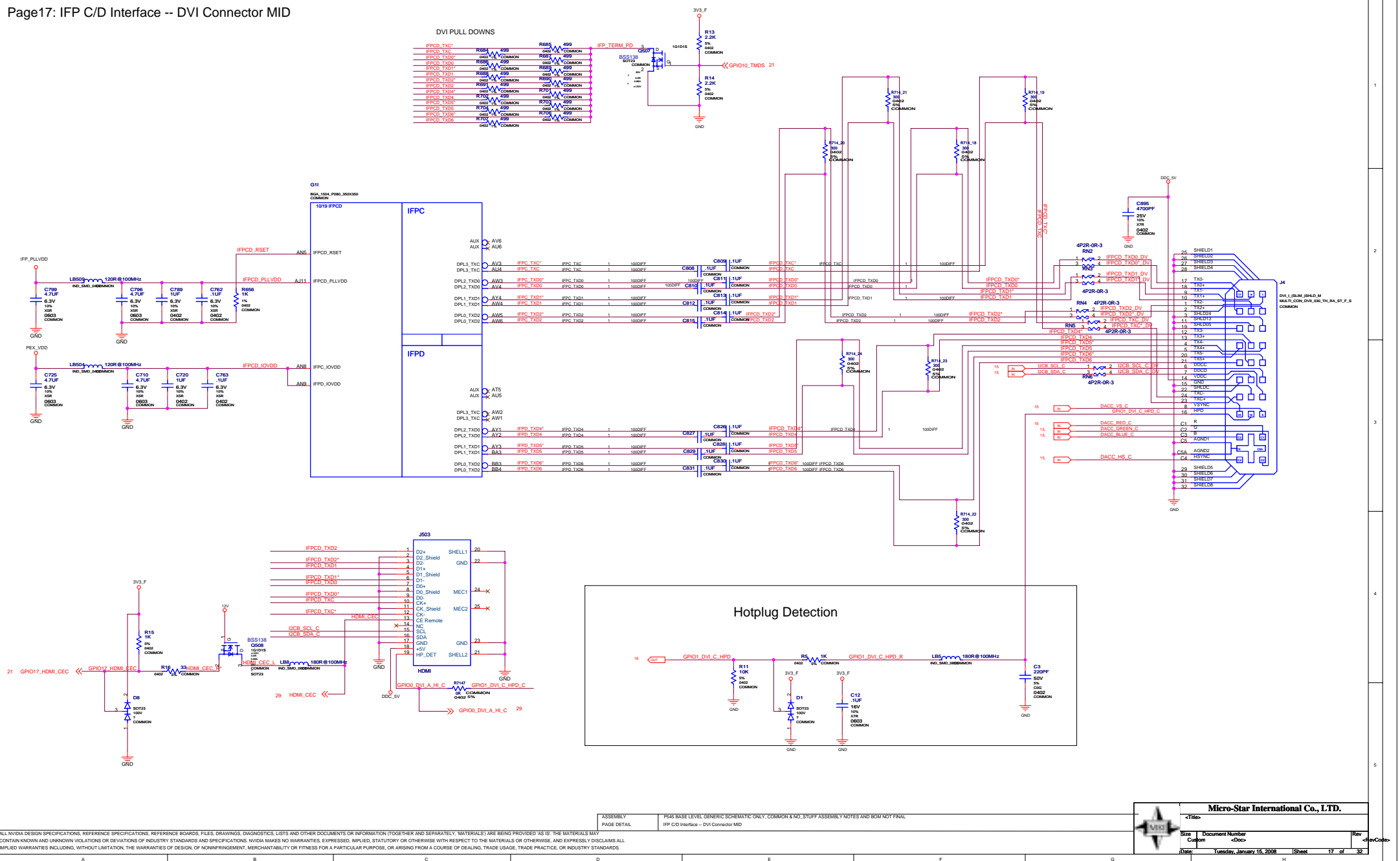
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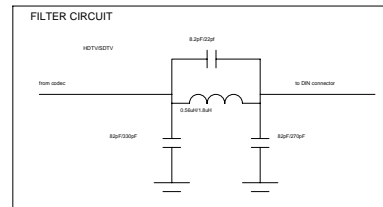
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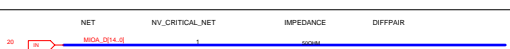
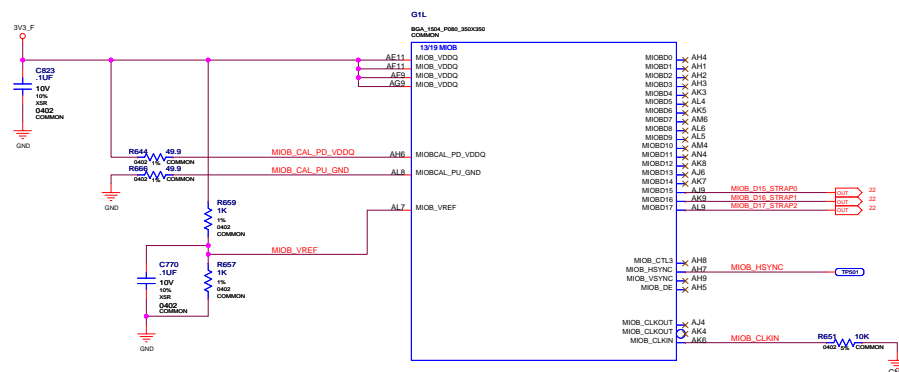
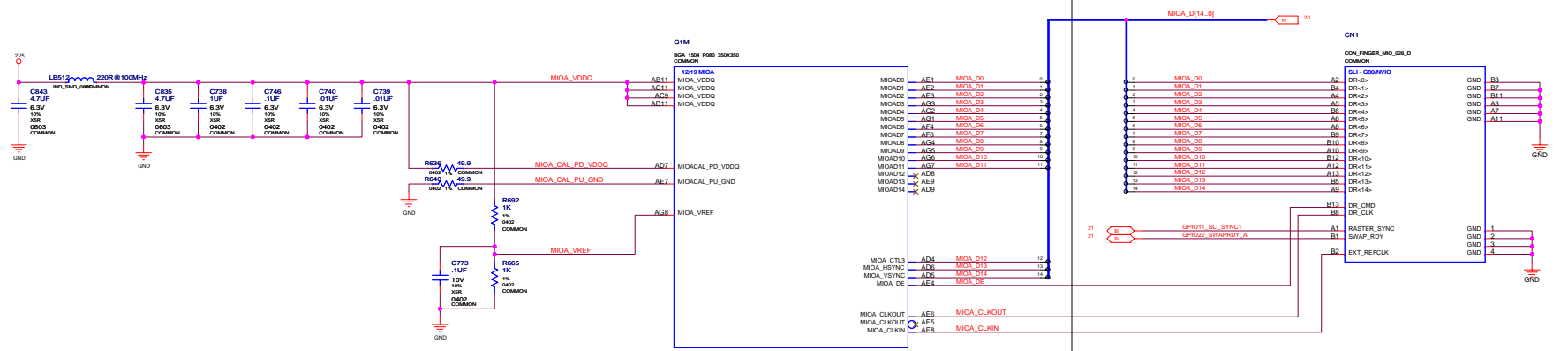
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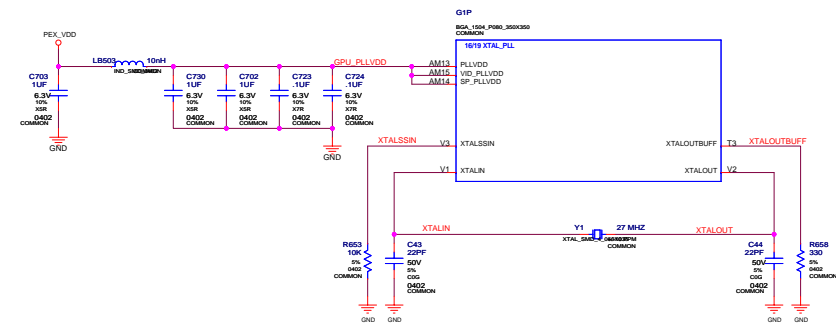
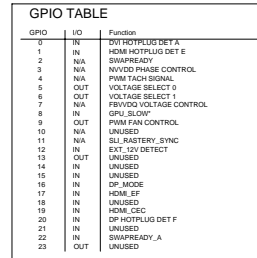
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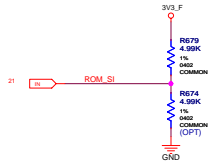




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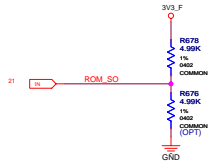




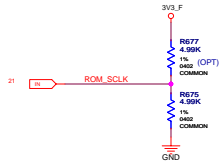


STRAP PIN	STRAP NAME
ROM_SI	PCI_DEVID_EXT

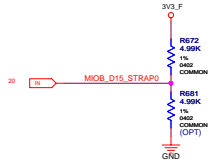
3V3		GND
5K	1	0



STRAP PIN	STRAP NAME
ROM_SO	SLOT_CLK_CFG



STRAP PIN	STRAP NAME
ROM_SCLK	PCI_DEVID[3]



STRAP PIN	STRAP NAME	
STRAP0	RAMCFG0	
STRAP1	RAMCFG1	
STRAP2	RAMCFG2	

* RAMCFG[2:0]

256MB (8Mx32)	512MB (16Mx32)	1024MB (32Mx32)
101 --- 256-bit Qimonda	001 --- 256-bit Qimonda	101 --- 256-bit Hynix
110 --- 256-bit Hynix	010 --- 256-bit Hynix	110 --- 256-bit Hynix
111 --- 256-bit Samsung	011 --- 256-bit Samsung	111 --- 256-bit Samsung

* VBIOS will be defined on a per SKU basis.

G1Q	
BGA_1554_P1560_3503392	
COMMON	
ACM3	NC
ACM4	NC
ACM5	NC
ACM6	NC
AF34	NC
AF35	NC
AF36	NC
AF37	NC
AG34	NC
AG35	NC
AG36	NC
AG37	NC
AL34	NC
AL35	NC
AL36	NC
AM34	NC
AM35	NC
AM36	NC
AM37	NC
AP34	NC
AP35	NC
AT34	NC
AT35	NC
AU34	NC
AU35	NC
AU36	NC
AV34	NC
AV35	NC
AV36	NC
C34	NC
E34	NC
E35	NC
F34	NC
F35	NC
F36	NC
F37	NC
G14	NC
G15	NC
G16	NC
G17	NC
H34	NC
H35	NC
H36	NC
H37	NC
I34	NC
I35	NC
I36	NC
I37	NC
J34	NC
J35	NC
J36	NC
J37	NC
K34	NC
K35	NC
K36	NC
K37	NC
L34	NC
L35	NC
L36	NC
L37	NC
M34	NC
M35	NC
M36	NC
M37	NC
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N35	NC
N36	NC
N37	NC
O34	NC
O35	NC
O36	NC
O37	NC
P34	NC
P35	NC
P36	NC
P37	NC
Q34	NC
Q35	NC
Q36	NC
Q37	NC
R34	NC
R35	NC
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S34	NC
S35	NC
S36	NC
S37	NC
T34	NC
T35	NC
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V34	NC
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V37	NC

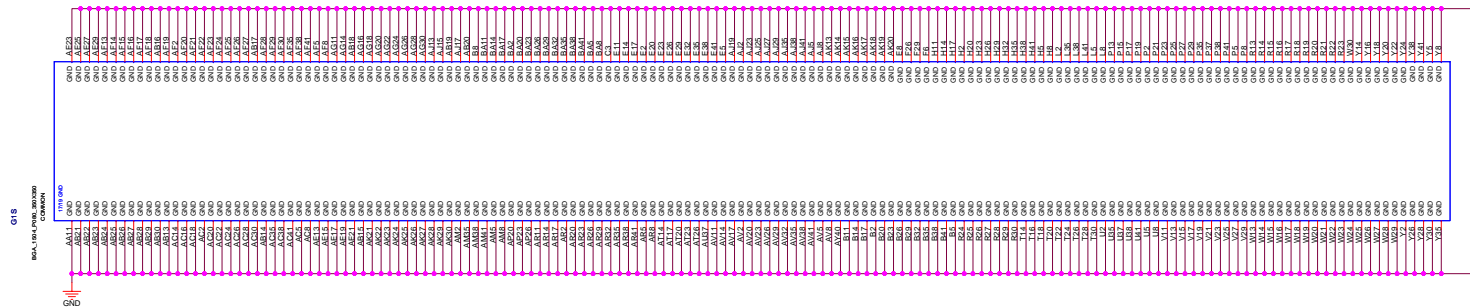
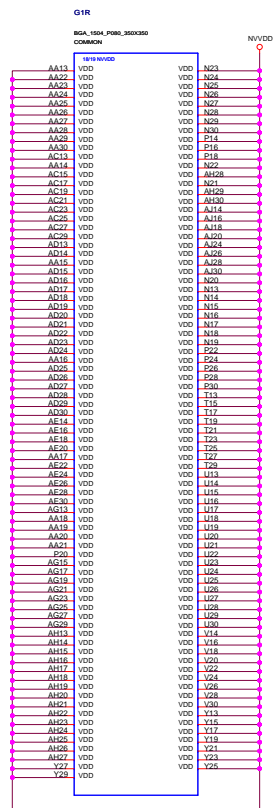
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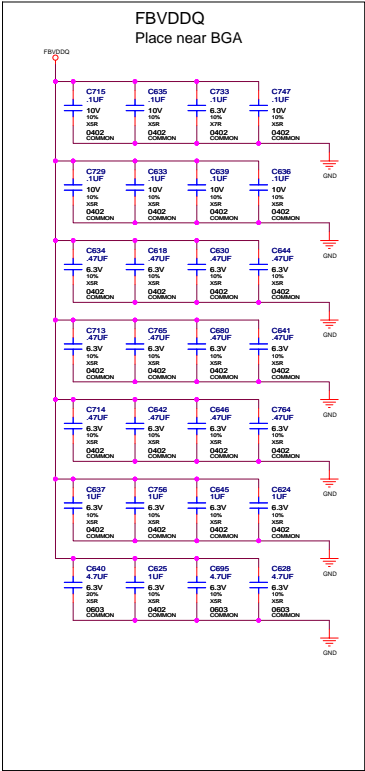
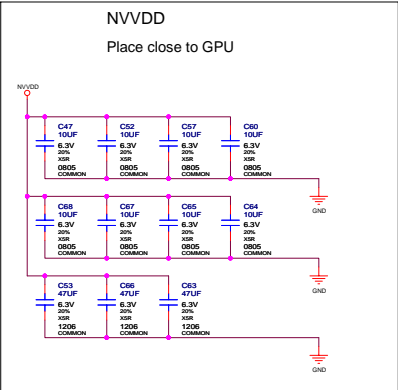
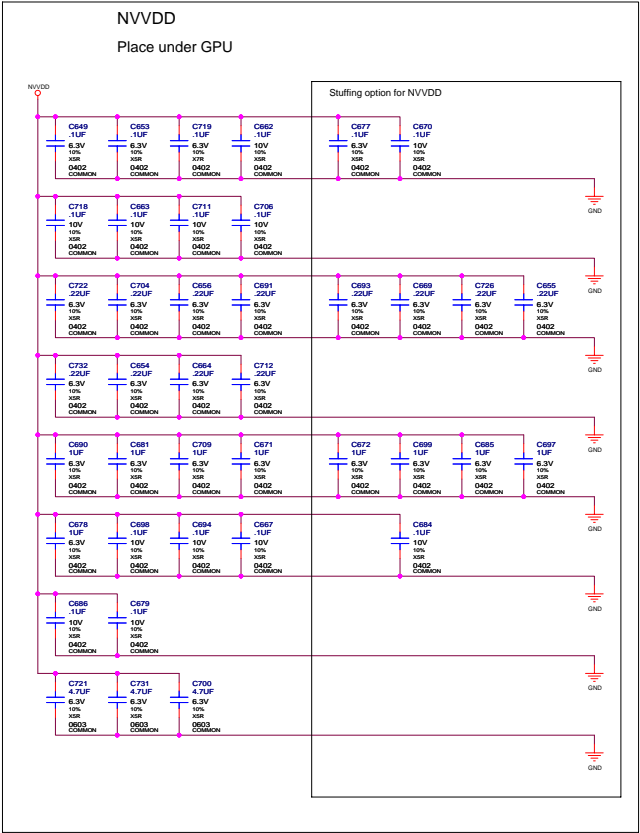
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PER-BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Strap Configuration



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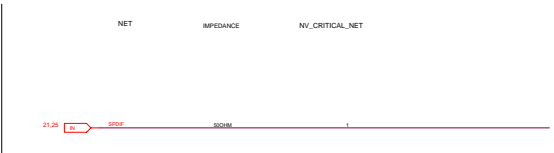
ASSEMBLY
PAGE DETAIL

PCB BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
NVVDD and FBVDDQ Decoupling

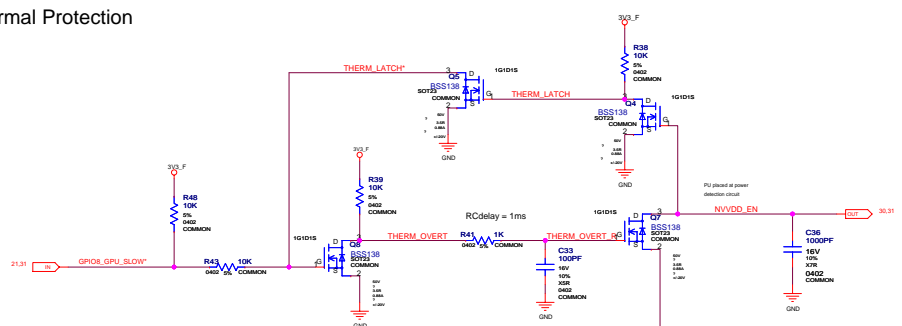


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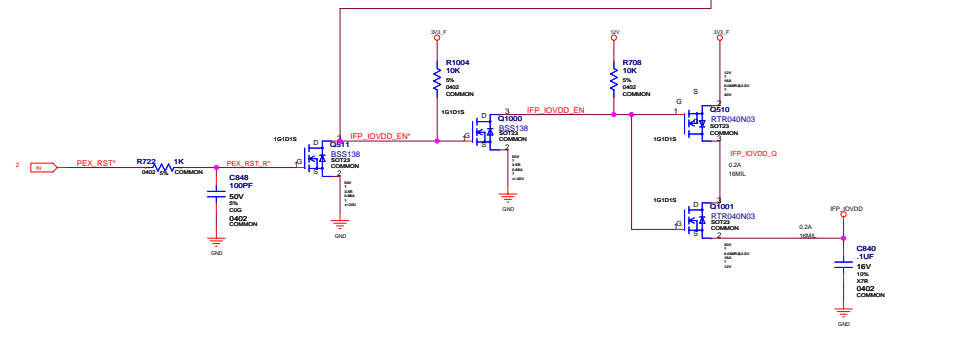


Thermal Protection

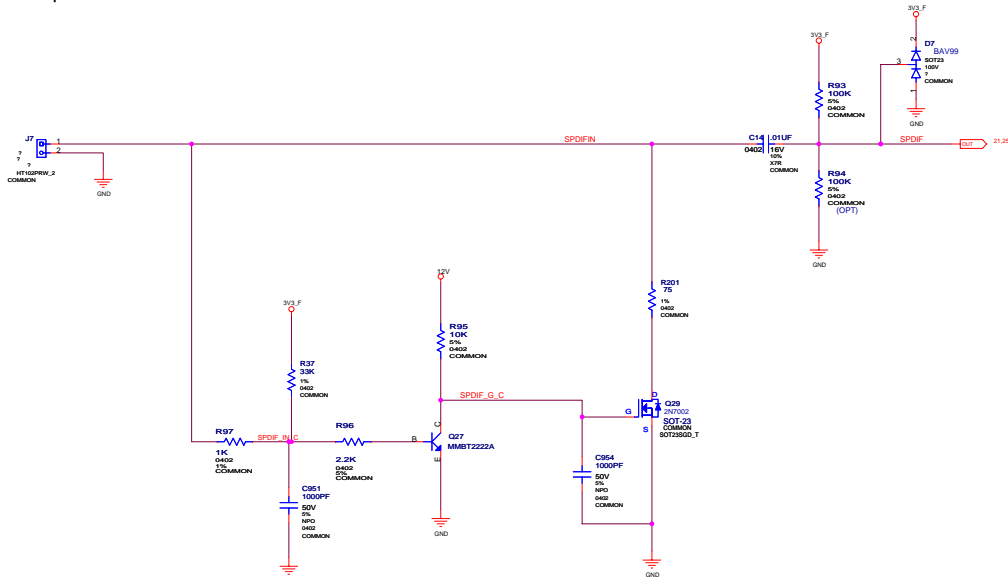


IFP_IOVDD Backdrive Prevention

Stuffing possibilities for thermal control and protection



SPDIF Input



ASSEMBLY	PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF Input, Backdrive Protection, and IFF_IOVDD Power Supply

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«Title»

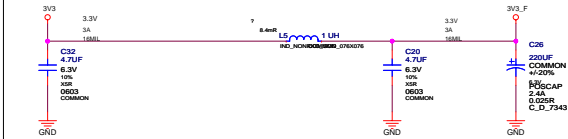
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3V3 Power Supply Filter

3V3_F = 3.3V @ 2.5A



12V Power Supply Filter

12V_F = 12V @ 5.5A

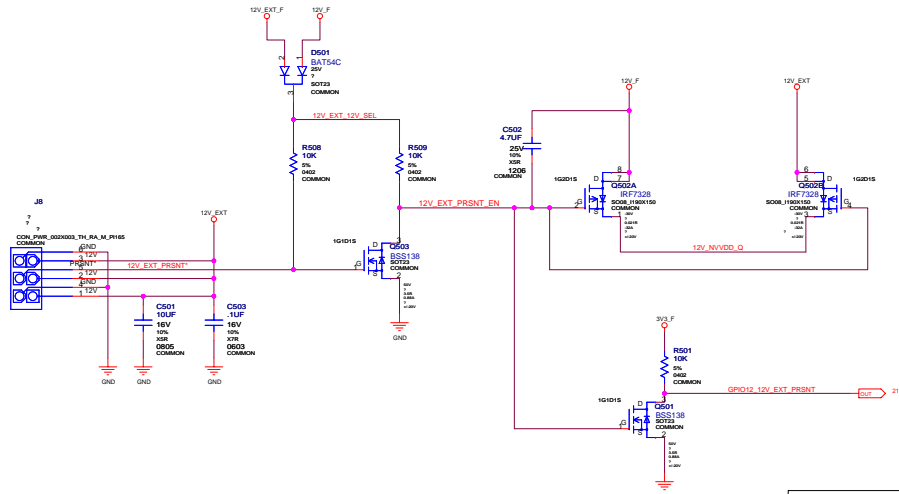


12V_EXT Power Supply Filter

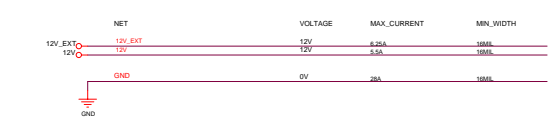
12V_EXT_F = 12V @ 6.25A

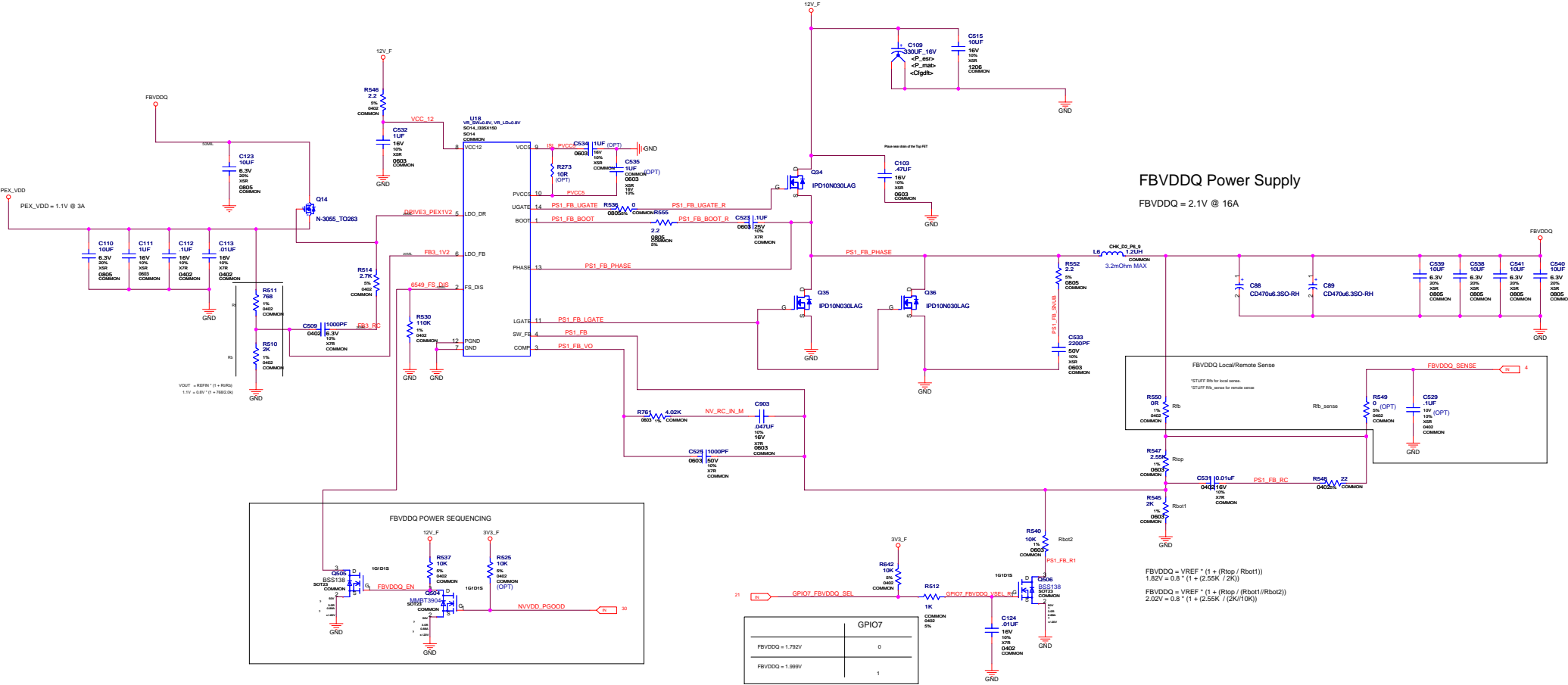


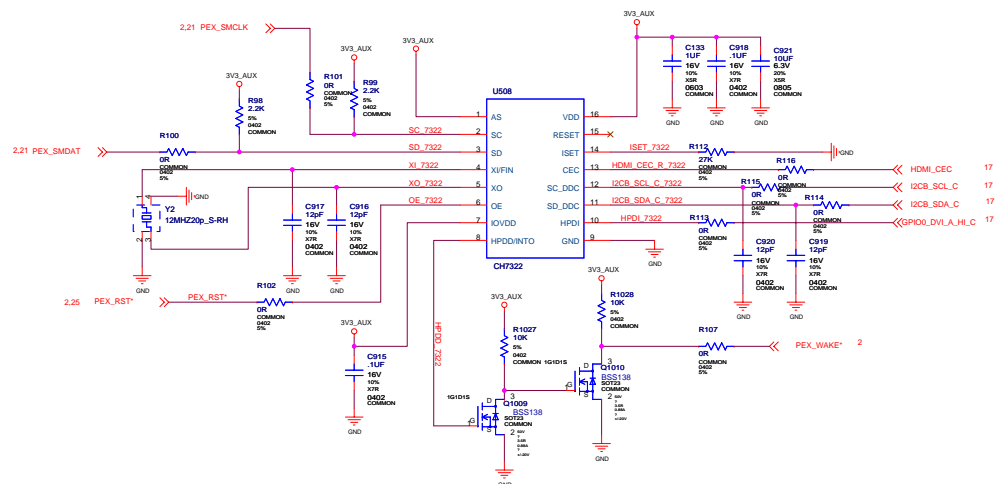
INPUT POWER SELECTION for NVVDD



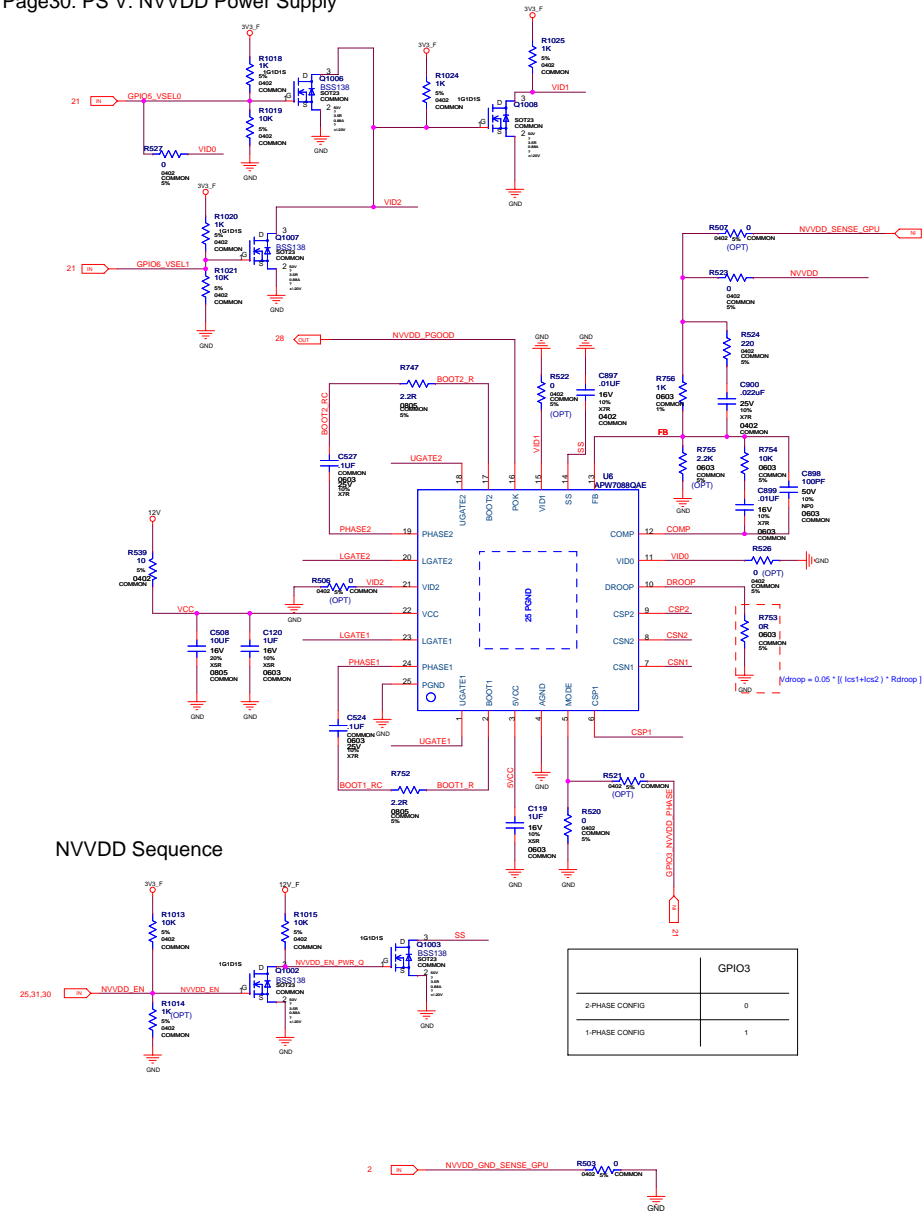
GPIO12	
EMERGENCY MODE (12V_EXT present)	0
150W POWER MODE (12V_EXT NOT present)	1



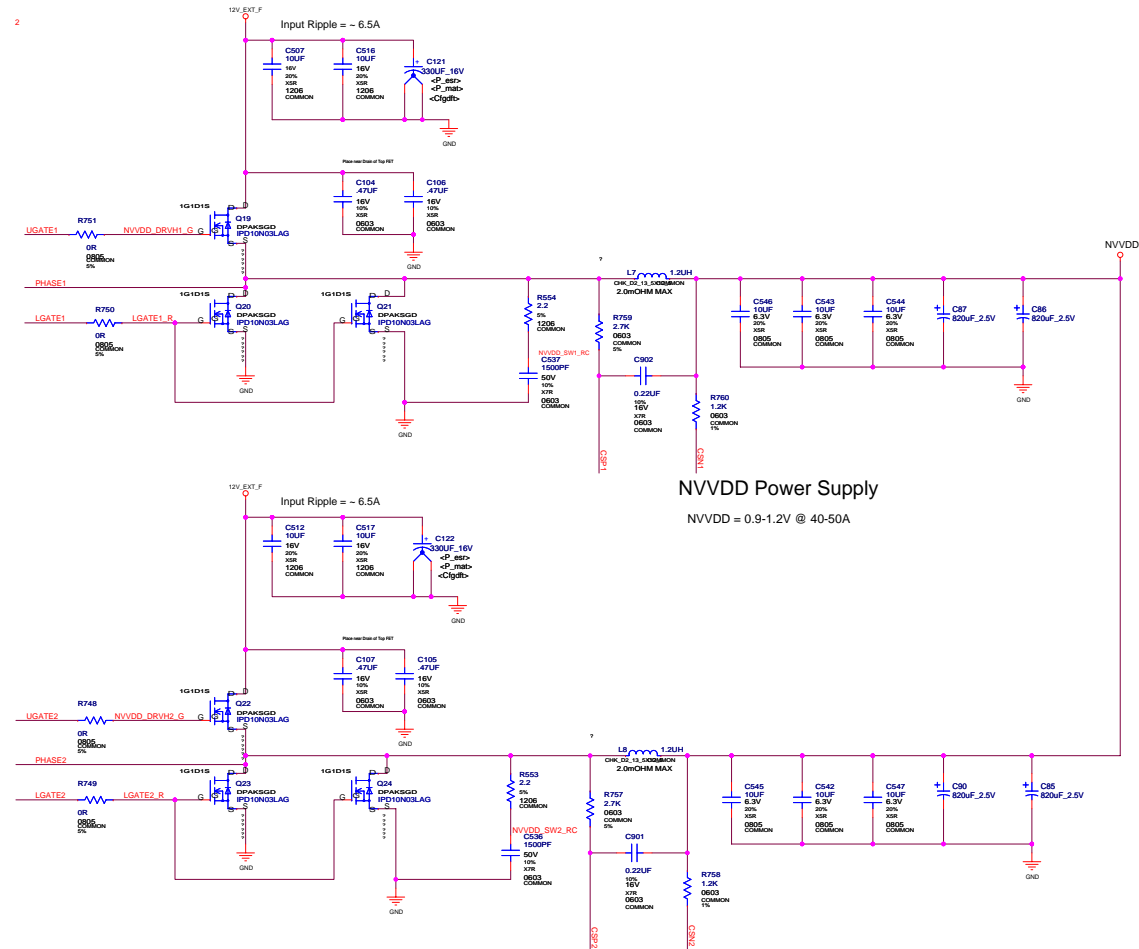




NVDD Voltage Select						NVDD	
NVDD range 0.80V-1.40V							
Register: ADR202							
Control via NV_GPCs NV_VSEL[1..0]							
VID						NVDD	
						G94	
6	5	4	3	1	0	VID	
0	1	1	0	0	0	0.80V	
0	1	1	0	1	0	0.85V	
0	1	1	0	0	1	0.90V	
0	1	1	1	0	0	0.95V	
0	1	0	1	0	0	1.00V	⇒ Default
0	1	0	1	1	0	1.05V	⇒ Voltage1
0	1	0	0	0	0	1.10V	⇒ Voltage2
0	1	0	0	1	0	1.15V	
0	1	0	1	1	1	1.20V	
0	1	0	1	0	1	1.25V	
0	1	0	0	1	1	1.30V	
0	0	0	1	1	1	1.35V	
0	0	0	1	0	1	1.40V	




GPIO6	GPIO5	NVVDD
1	0	1.1V
0	1	1.05V
0	0	1.0V



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ASSEMBLY PAGE DETAIL
PG V: NVVDD Power Supply



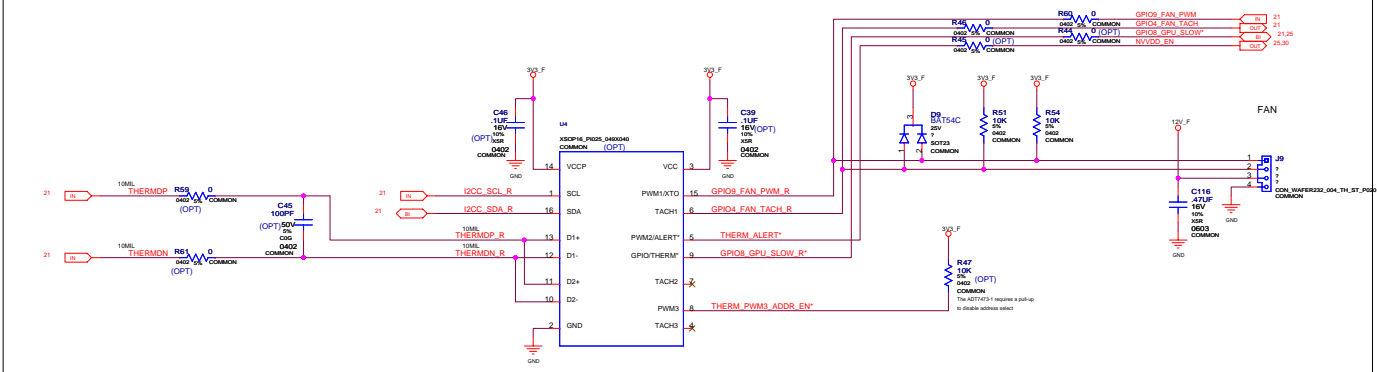
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ADT7473 External Fan/Thermal Control

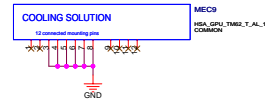


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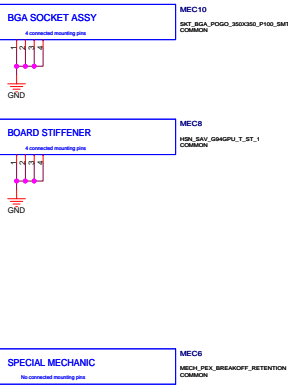
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Thermal Diode and Fan Control

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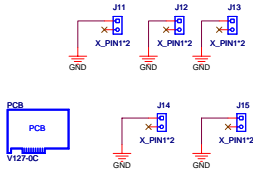
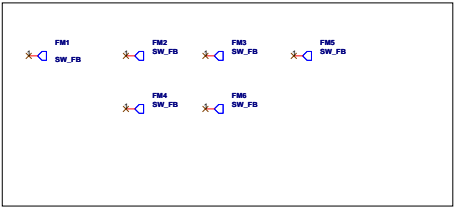
Thermal



Mechanical



Bracket



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