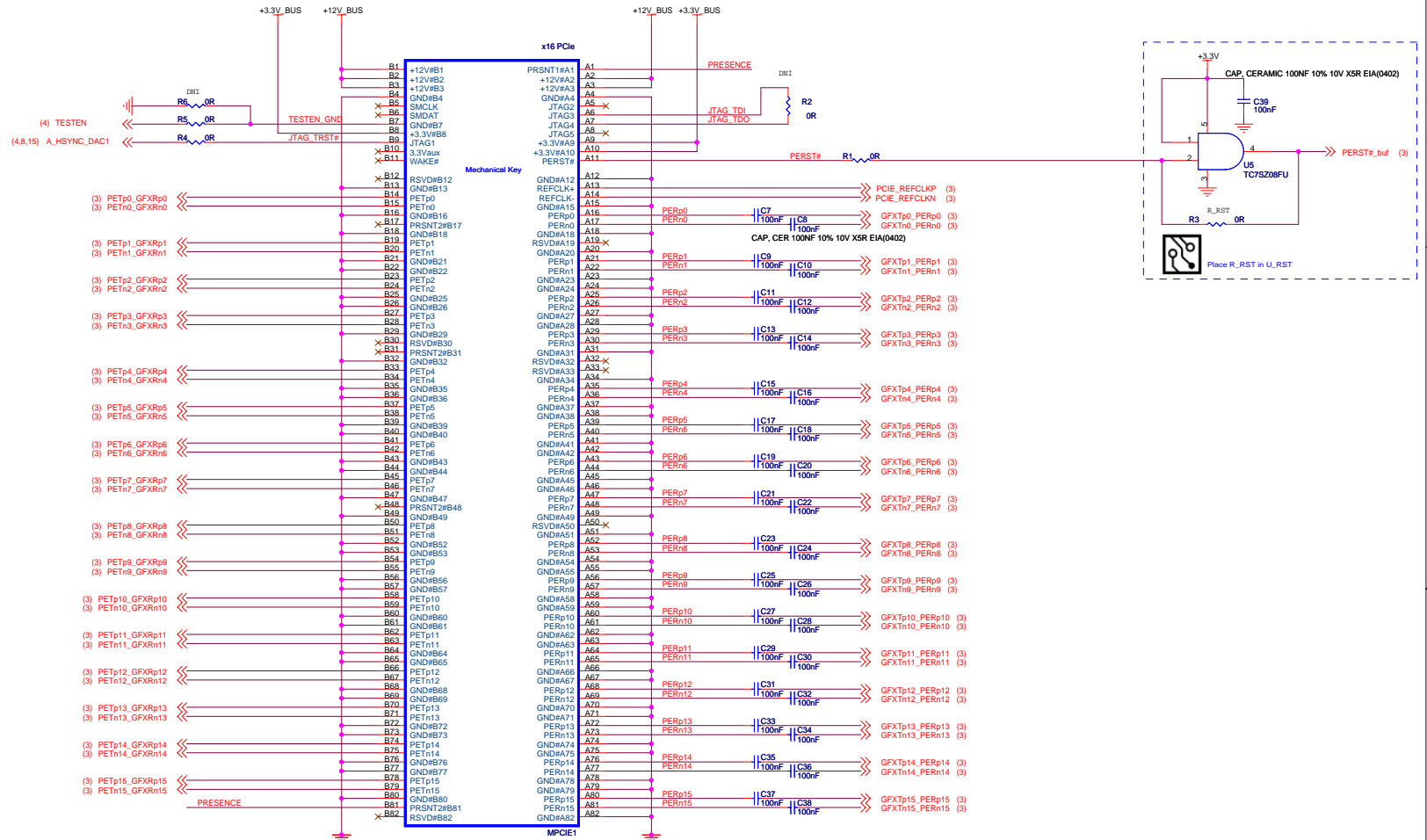
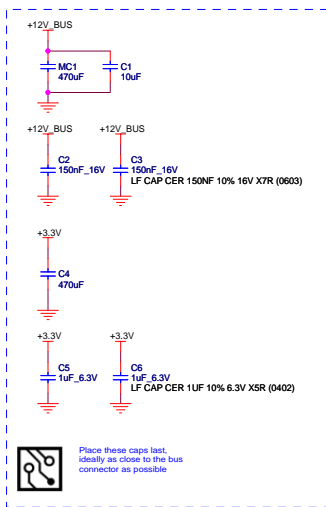


RV530 DDR2 FH 4-Layer



PCI-EXPRESS EDGE CONNECTOR



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation. Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be held low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND



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MS-V040 RV530/DDRII

Size C

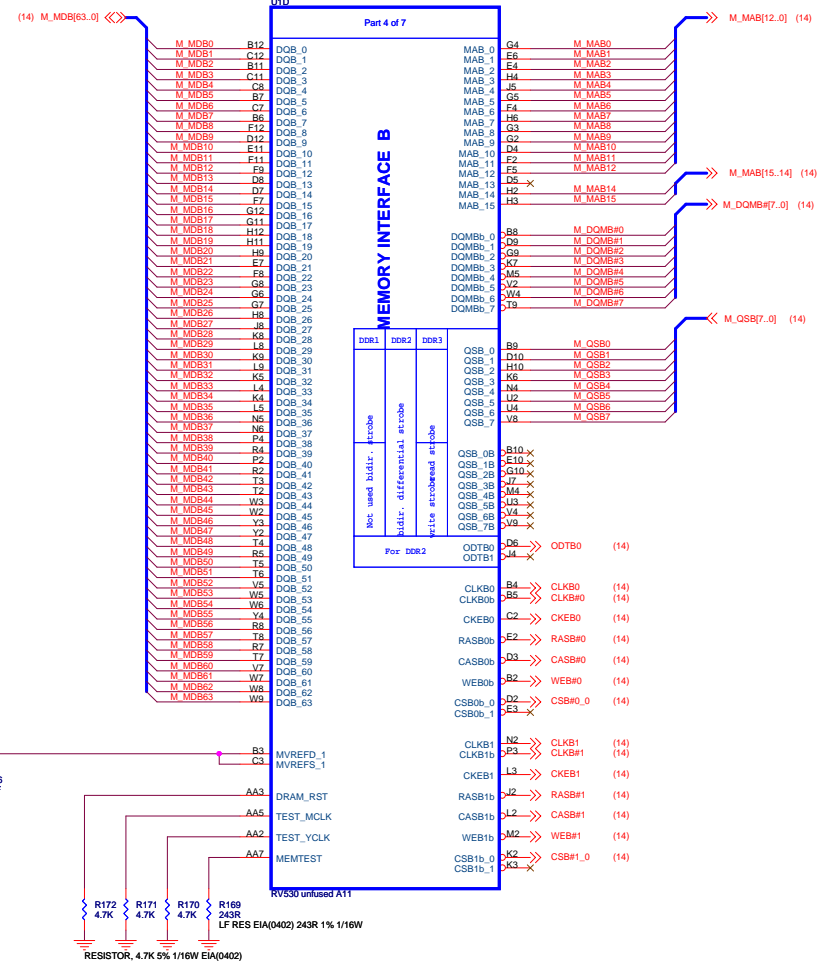
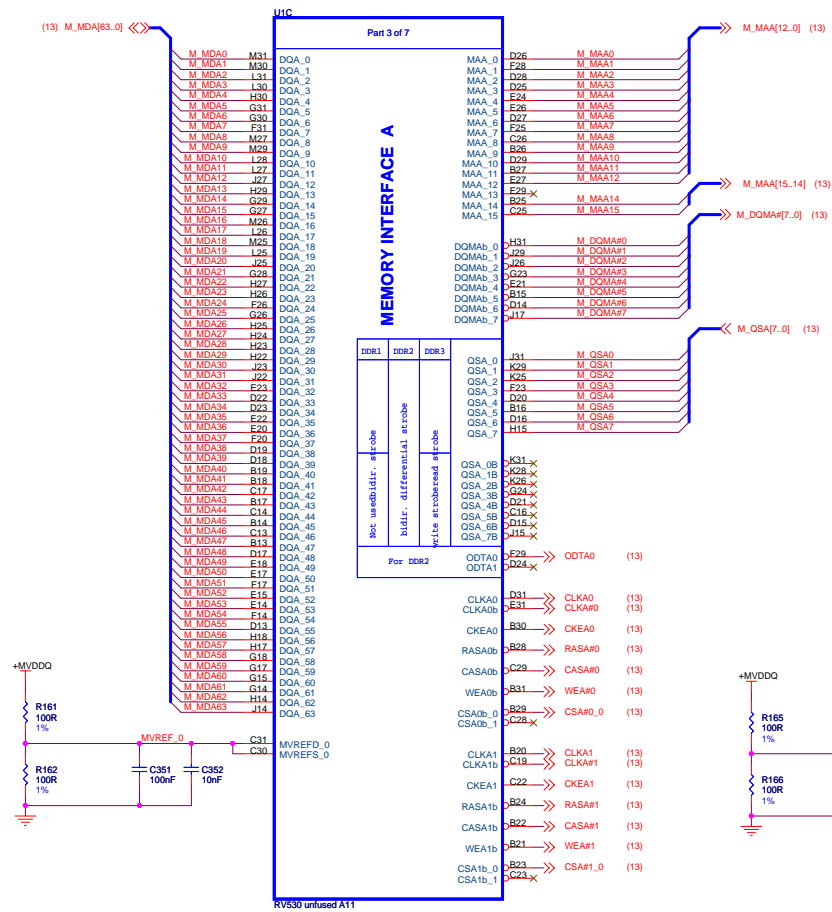
Document Number

Date: Friday, March 24, 2006

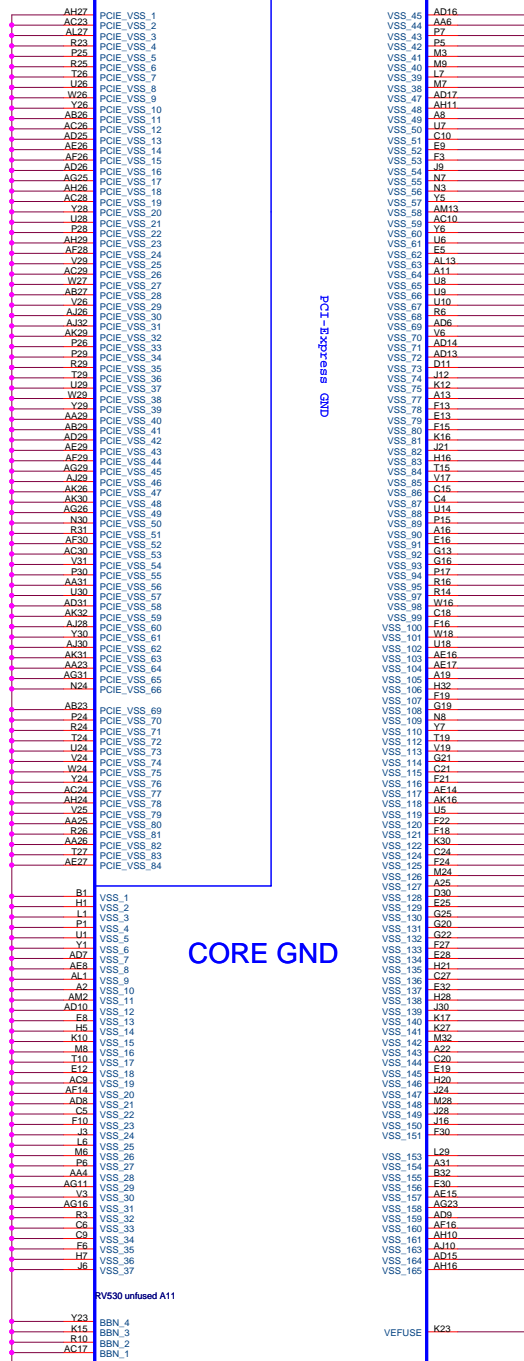
Sheet 2 of 19

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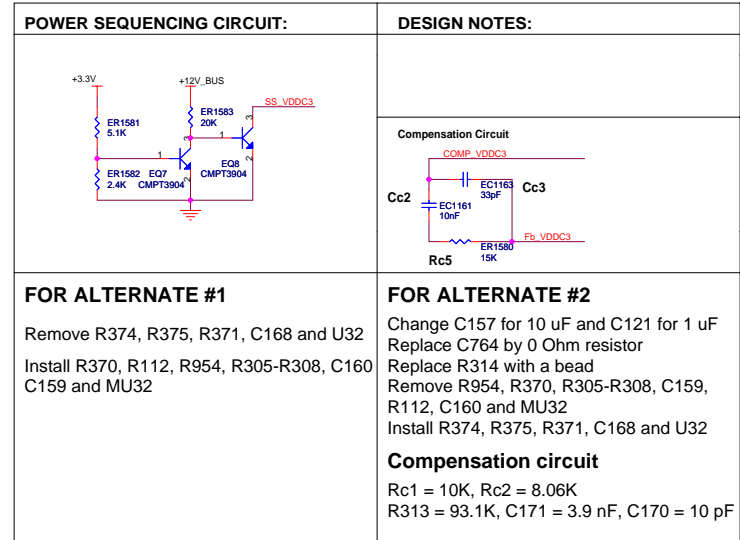
Channel B

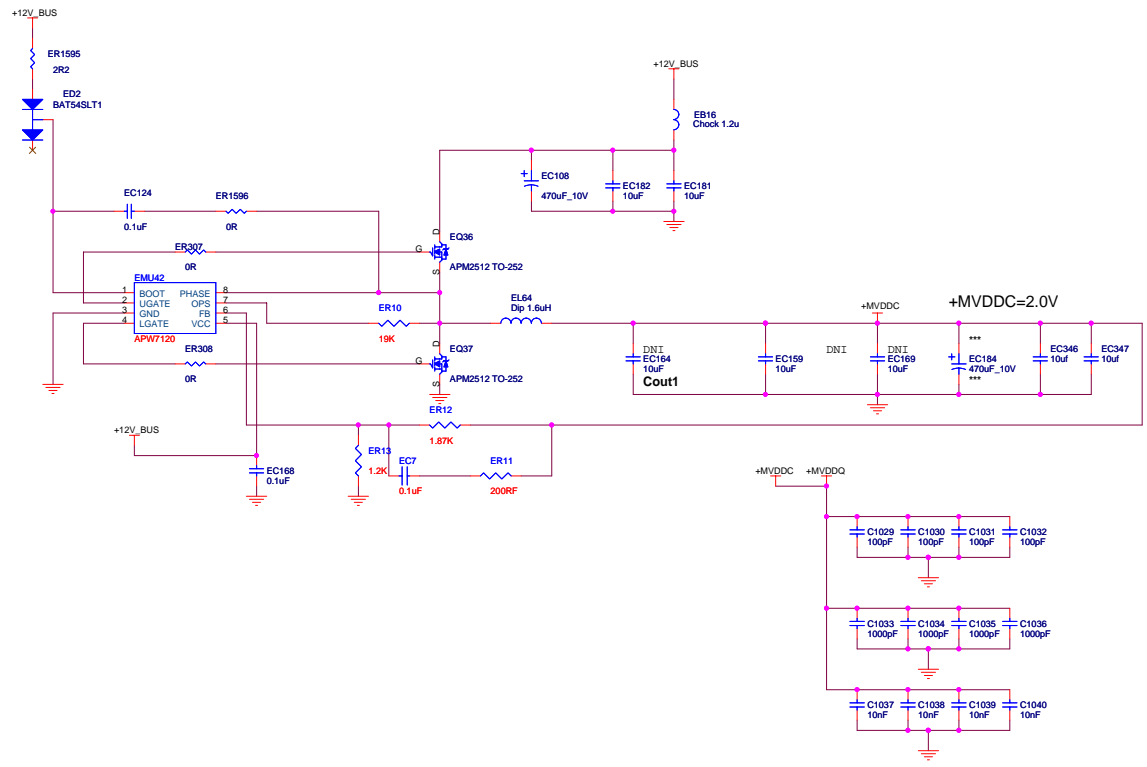


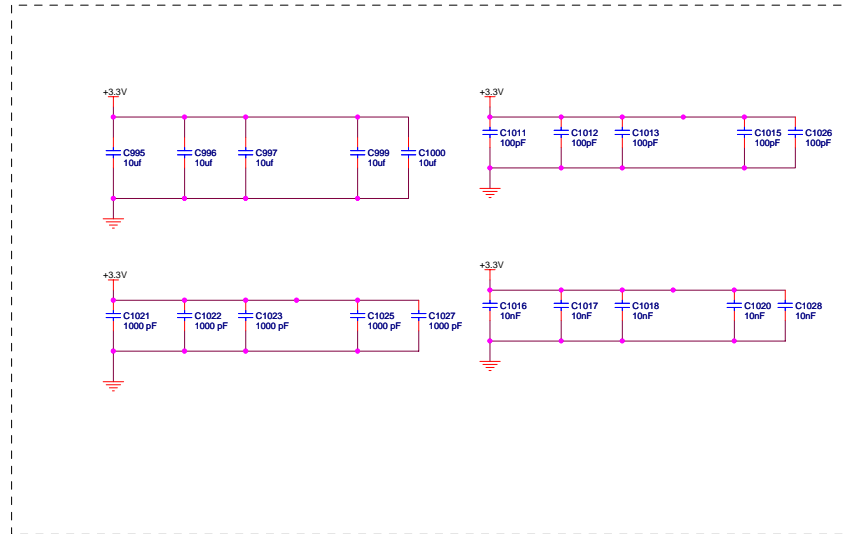
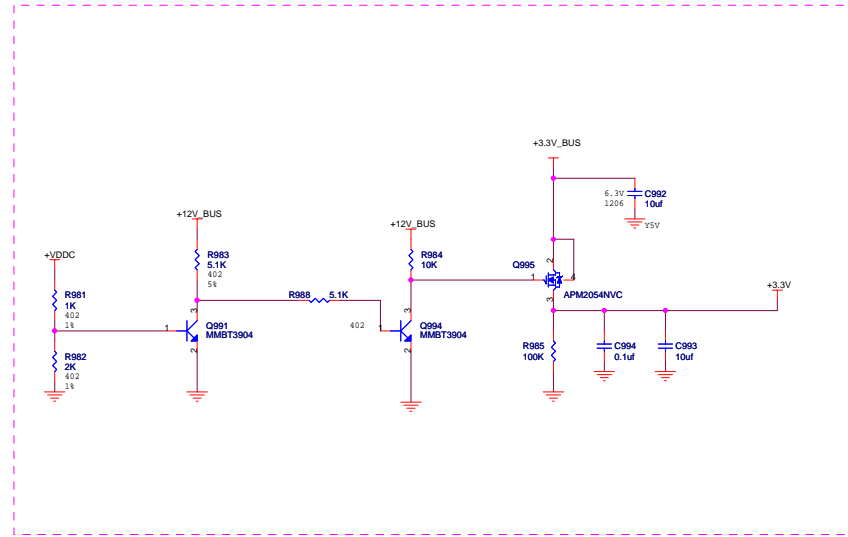
Part 6 of 7



Lower MOSFET should be surrounded by a lot of copper for heat dissipation



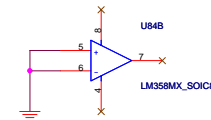
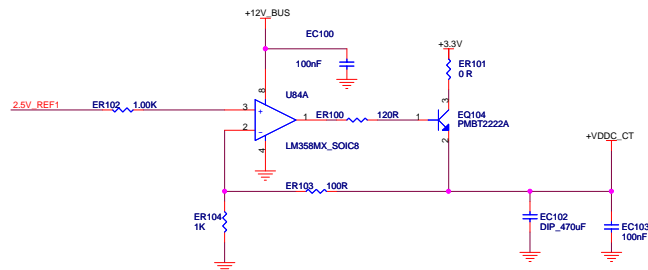
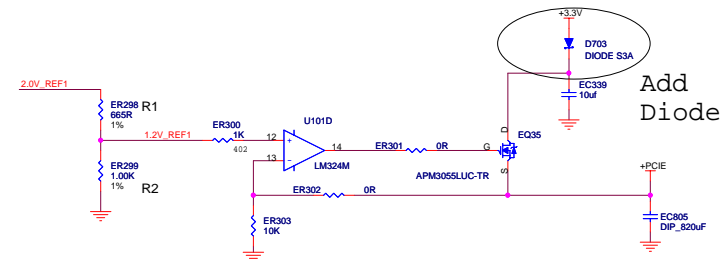
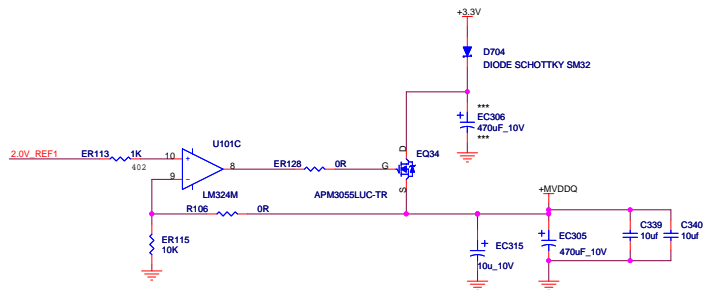
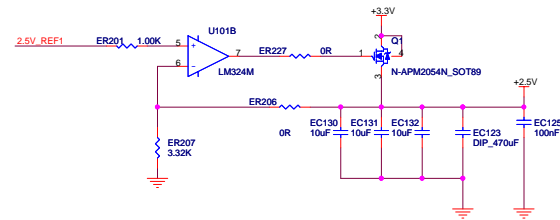
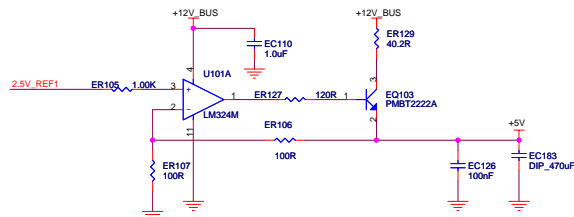
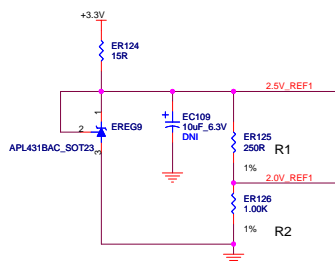




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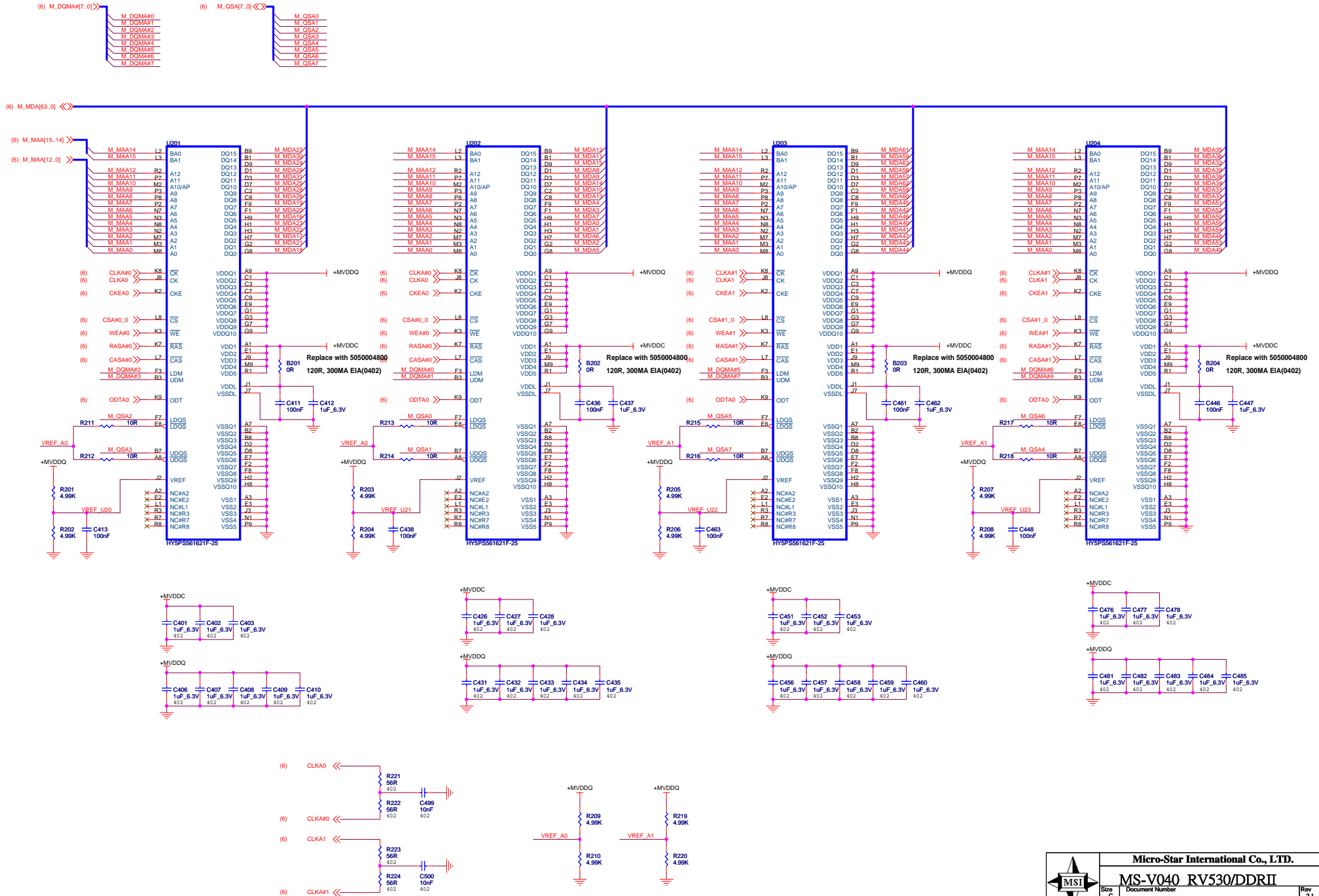
MS-V040 RV530/DDRII

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Custom		2.1
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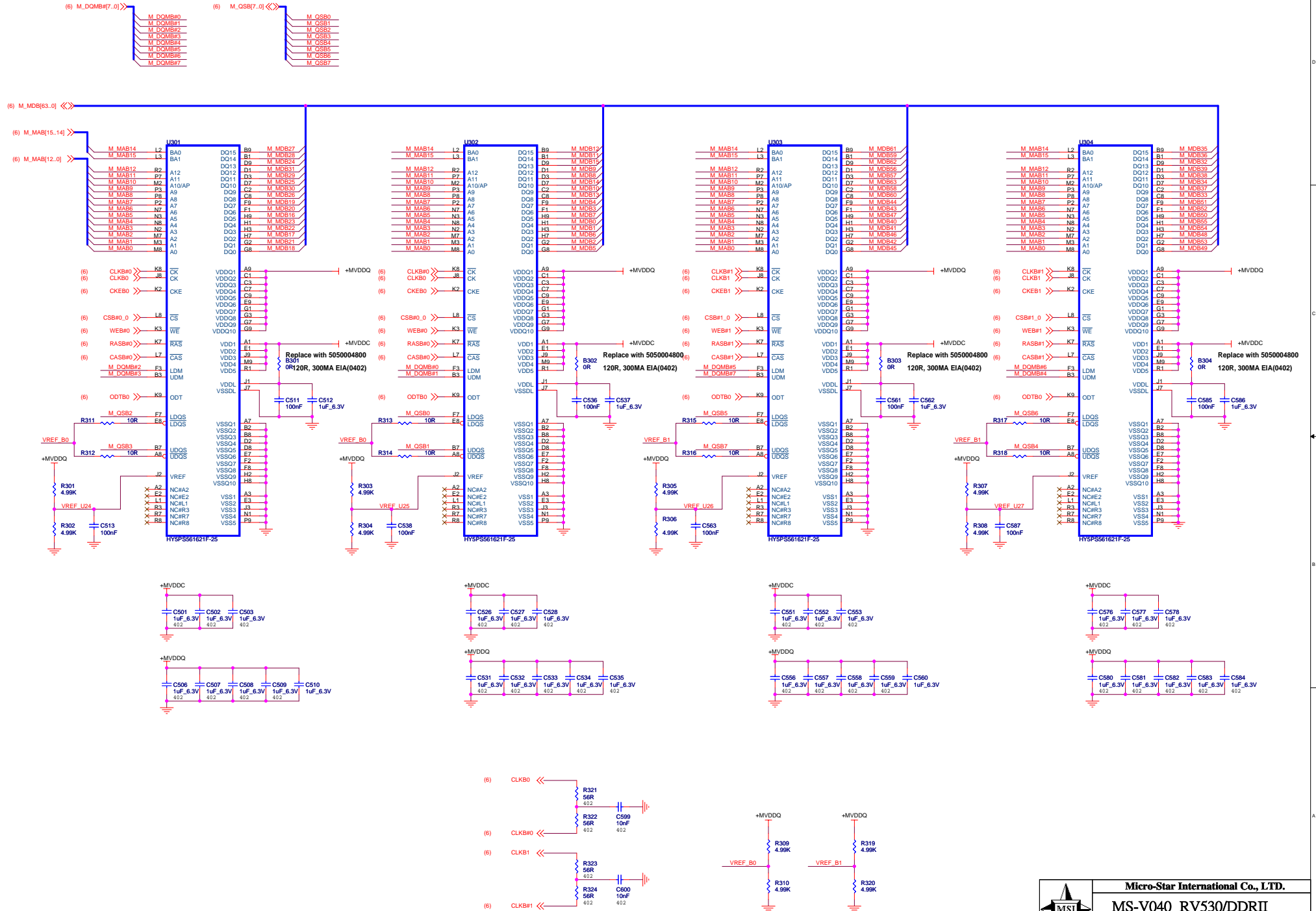


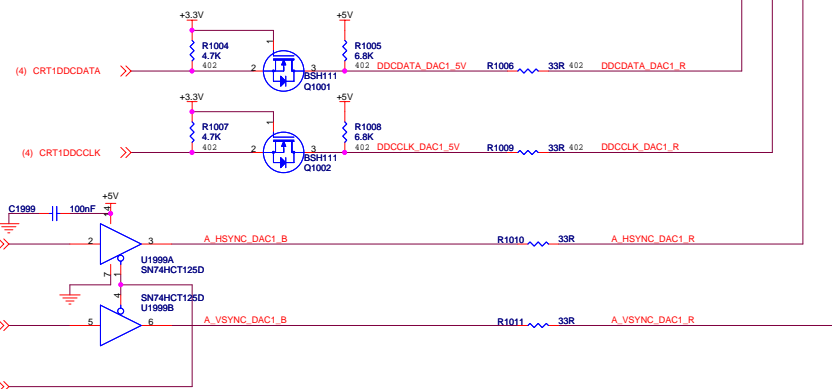
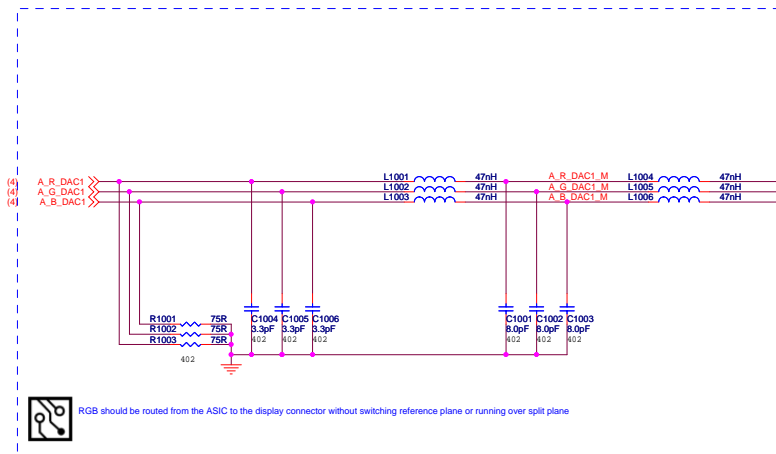
Replace with S050004800
120R, 300MA EIA(0402)

CHANNEL A: RANK 0 128MB DDR2

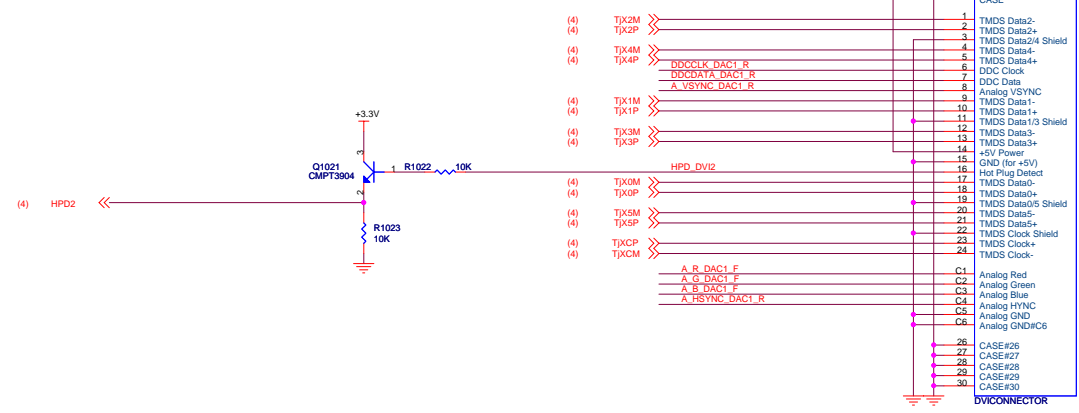


CHANNEL B: RANK 0 128MB DDR2





SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional	Optional
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional	Optional
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional	Optional
15	Monitor ID bit 3	Open	Open	Optional	Optional
9	N/C	+5V	+5V	+5V	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

(4) A_R_DAC2
(4) A_G_DAC2
(4) A_B_DAC2

L2001 47nH
L2002 47nH
L2003 47nH
L2004 47nH
L2005 47nH
L2006 47nH

R2001 75R
R2002 75R
R2003 75R
C2004 3.3pF
C2005 3.3pF
C2006 3.3pF
C2001 8.0pF
C2002 8.0pF
C2003 8.0pF



RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane

(4) CRT2DDCCDATA

+3.3V
R2004 4.7K
Q2001

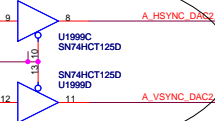
+5V
R2005 6.8K
Q2001

(4) CRT2DDCLK

+3.3V
R2007 4.7K
Q2002

+5V
R2008 6.8K
Q2002

(4,8) A_HSYNC_DAC2



(4,8) A_VSYNC_DAC2

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

(4) DAC2_Y

L3001 470nH
R3001 75R
C3001 47pF
C3004 47pF

(4) DAC2_C

L3002 470nH
R3002 75R
C3002 47pF
C3005 47pF

(4) DAC2_COMP

L3003 470nH
R3003 75R
C3003 47pF
C3006 47pF

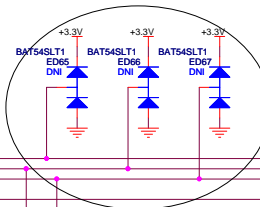
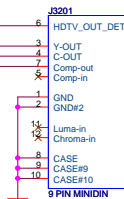


(8) HPD1

+3.3V
Q2021 MMBT3904
R2022 10K
R2023 10K

(8) STV/HDTVw_OUT_DET

+3.3V
R3008 10K
R3009 0R

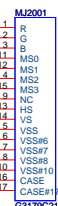


A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F

DDCDATA_DAC2_R
DDCLK_DAC2_R
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R

C2007 5pF
C2008 5pF
C2009 5pF
L2007 62nH (50nH)
L2008 62nH (50nH)
L2009 62nH (50nH)

+5V_VESA2
EF2 1.5A

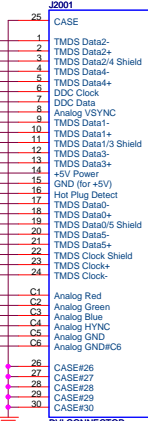


DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

(4) T2X2M
(4) T2X2P
(4) T2X4M
(4) T2X4P
(4) T2X1M
(4) T2X1P
(4) T2X3M
(4) T2X3P
(4) T2X0M
(4) T2X0P
(4) T2X5M
(4) T2X5P
(4) T2XCP
(4) T2XCM

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
A_HSYNC_DAC2_R

+5V_VESA2



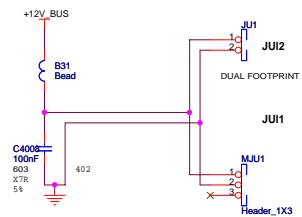
DVI CONNECTOR



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DVI/VGA SCREWS

- SCREW1

SCREW
JACKSCREW
ASSY
7020000800
- SCREW2

SCREW
JACKSCREW
ASSY
7020000800
- SCREW3

SCREW
JACKSCREW
ASSY
7020000800
- SCREW4

SCREW
JACKSCREW
ASSY
7020000800

