PG600-B02 NIGHTHAWK

GB3B-384, 6GB GDDR5 128Mx32

DP + HDMI/DP + DP + DP + DVI-I

TABLE OF CONTENTS

V325 -10 bason on GM200 modify

Page 03 modify JTAG , change 1206 footprint 0805,remove power_Brake
Page 04 ~18 modify memory nat name
Page 22 change DVI footprint,add ESD
Page 23,25 chnage DP footprint
Page 24 chnage HDMI footprint ,remove co-lay DP circuit, add ESD
Page 26 remove co-lay SLI circuit
Page 27 remove STEREO HEADER and R145 and JTAG circuit
Page 28 add dual BIOS circuit
Page 29 change 5V and PEX_VDD circuit , add driver VCC 5V circuit
Page 30/31 change FBVDD and PEX_VDD power circuit
Page 32~35 change NVVDD power circuit
Page 36 add NTC7511 circuit
Page 37 modify 12V to 12VF circuit , add and modify POWER connector circuit, remove 3V3_FILTER
Page 38 add 新增 POWER connector circuit ,
Page 39 add V check point and OC board circuit , remove MEC2 , add 螺絲孔
Page 40 add 12V current steering circuit
Page 41 add micro LED circuit
Page 42 rmove MCU circuit

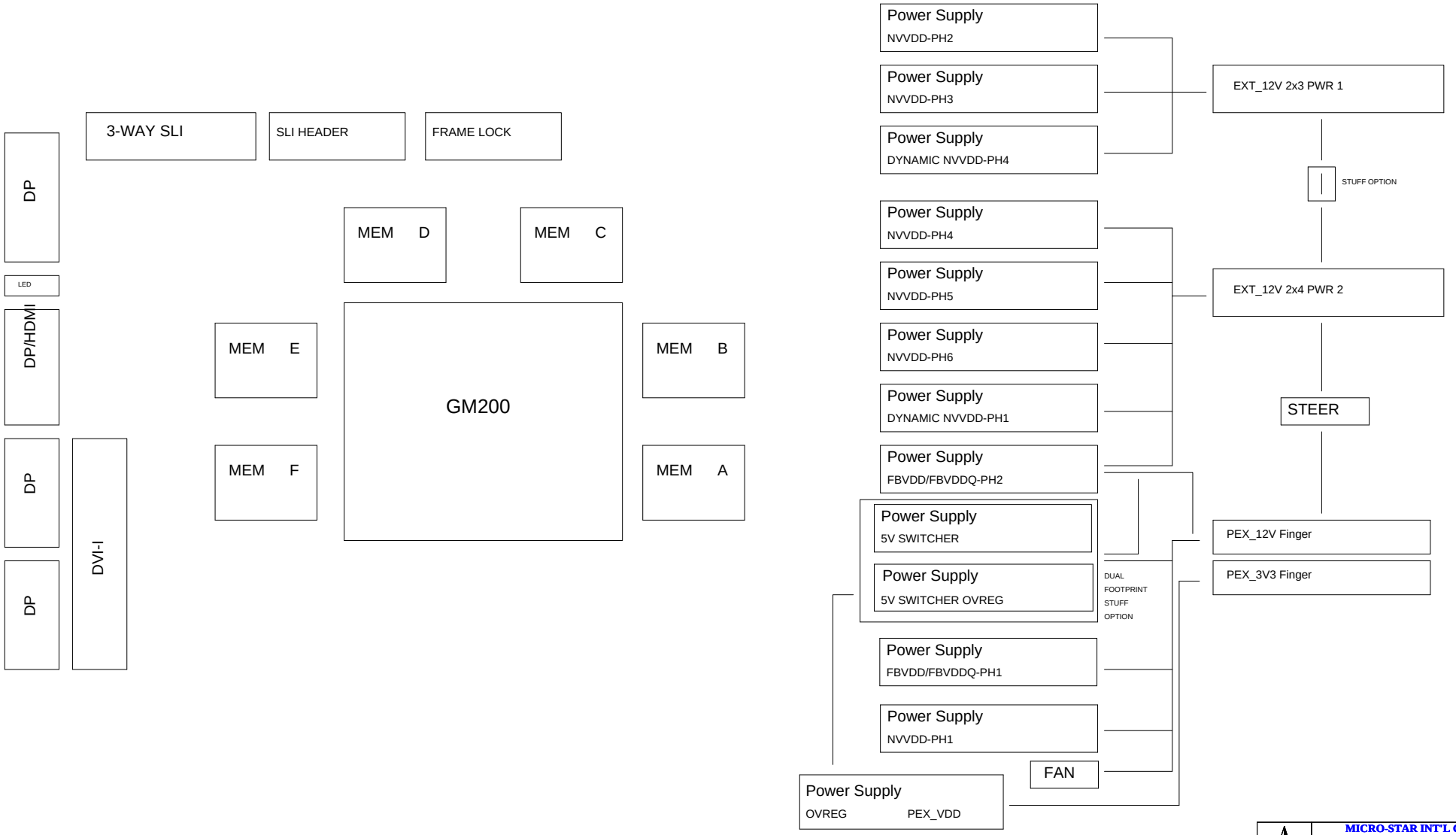
MICRO-STAR INT'L CO.,LTD

MS-V325

Size	Document Description	Rev
Custom	TABLE OF CONTENTS	1.0

Date: Thursday, May 21, 2015 Sheet 1 of 42

Page2: Block Diagram



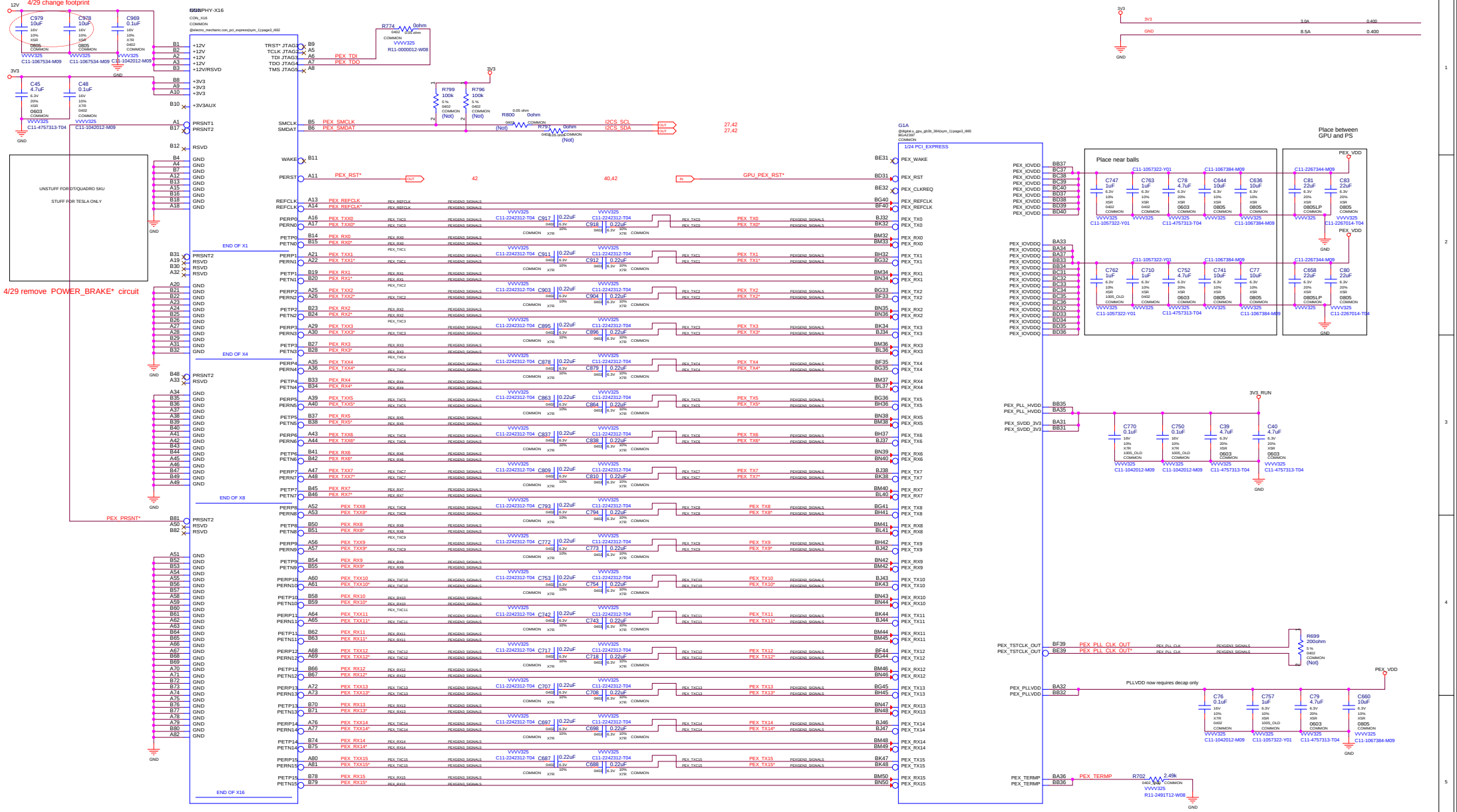
MICRO-STAR INT'L CO.,LTD

MS-V325

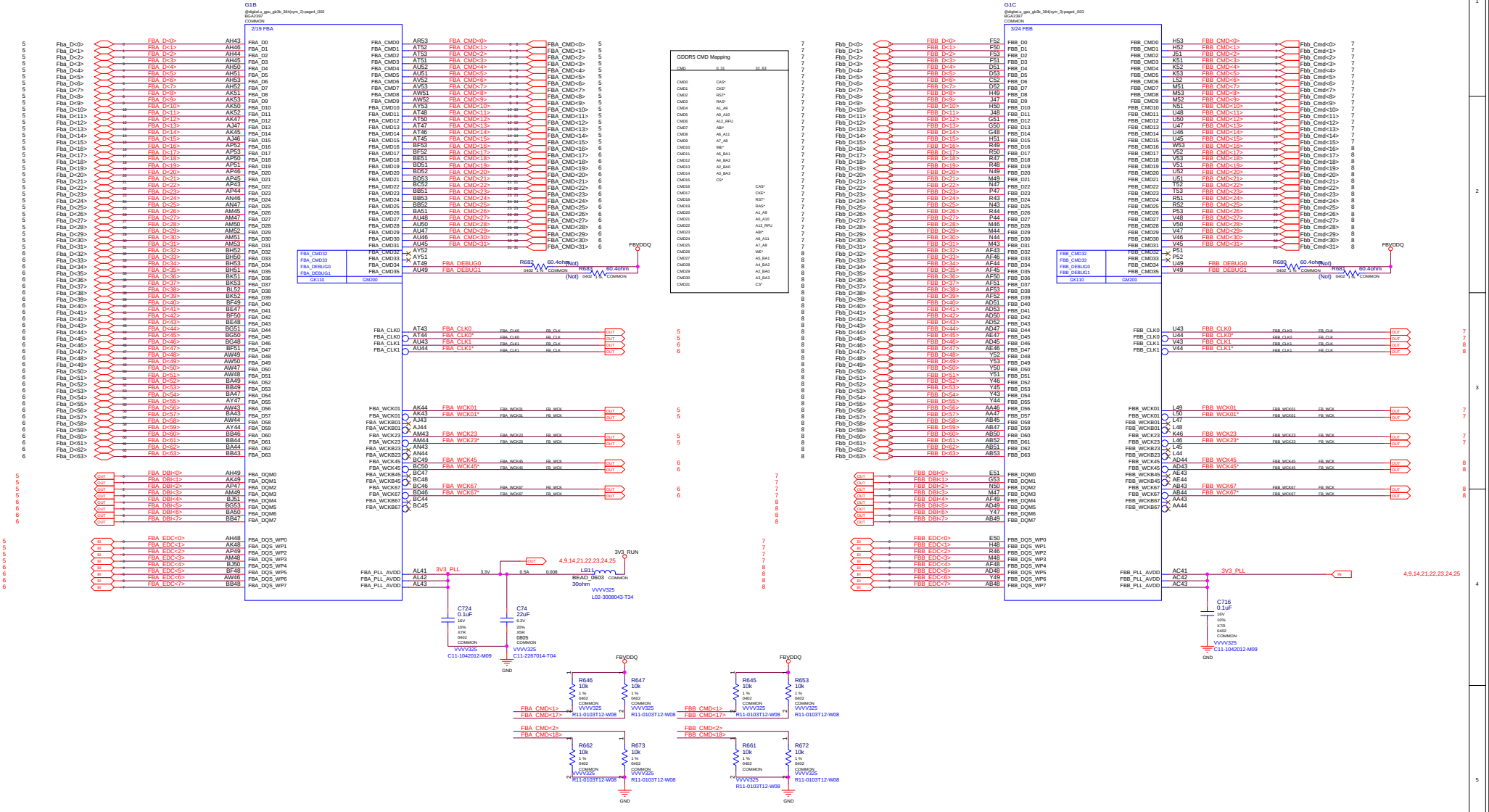
Size: Custom | Document Description: TABLE OF CONTENTS | Rev: 1.0

Date: Thursday, May 21, 2015 | Sheet 2 of 42

Page3: PCI Express

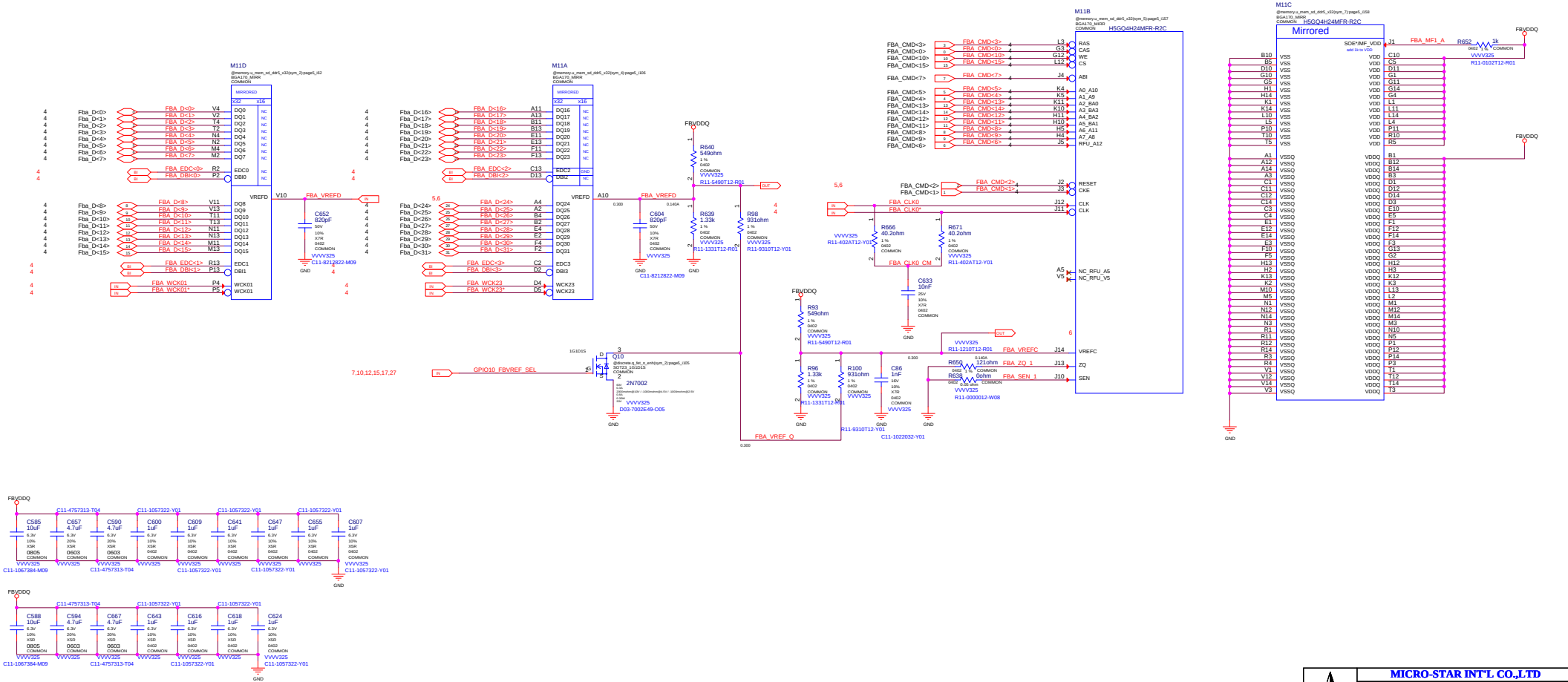


Page4: MEMORY: GPU Partition A/B



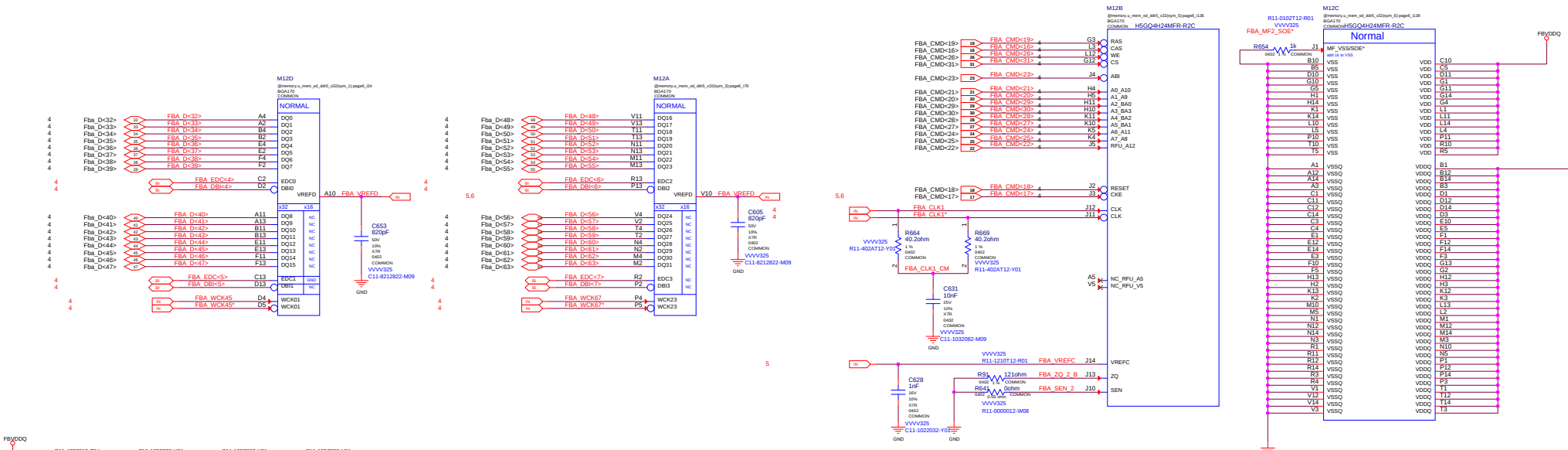
MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 4 of 42

Page5: MEMORY: FBA Partition 31..0



MICRO-STAR INT'L CO.,LTD			
MS-V325			
Size: Custom	Document Description: TABLE OF CONTENTS		Rev: 1.0
Date: Thursday, May 21, 2015	Sheet 5 of 42		

Page6: MEMORY: FBA Partition 63..32



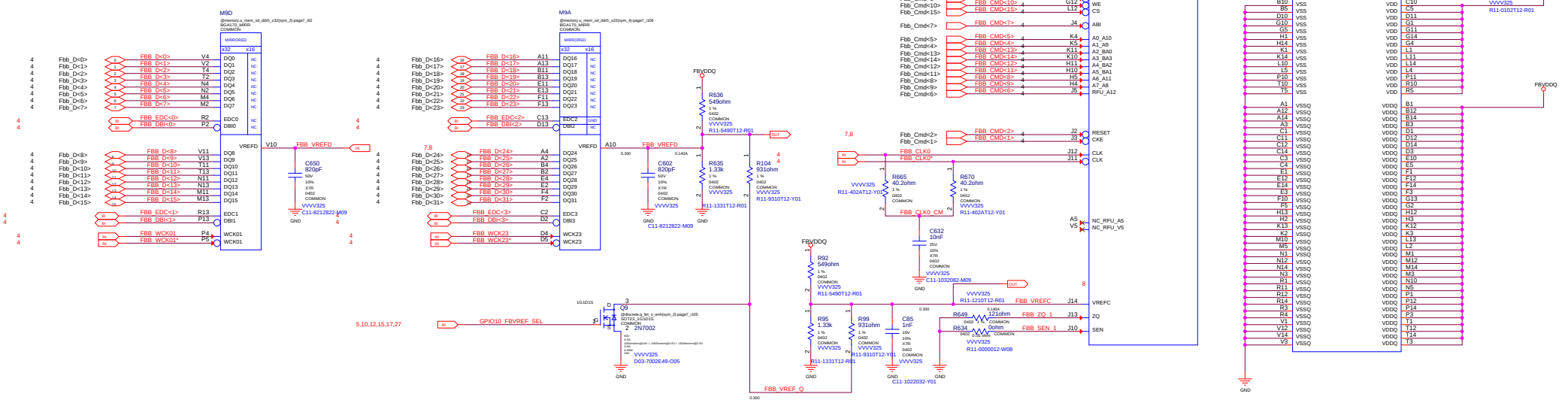
MICRO-STAR INT'L CO.,LTD

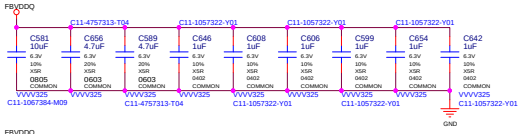
MS-V325

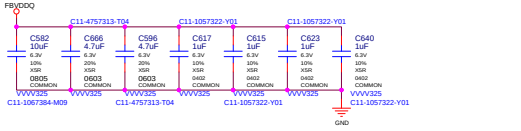
Size	Document Description	Rev
Custom	TABLE OF CONTENTS	1.0

Date: Thursday, May 21, 2015 | Sheet 6 of 42

Page7: MEMORY: FBB Partition 31..0

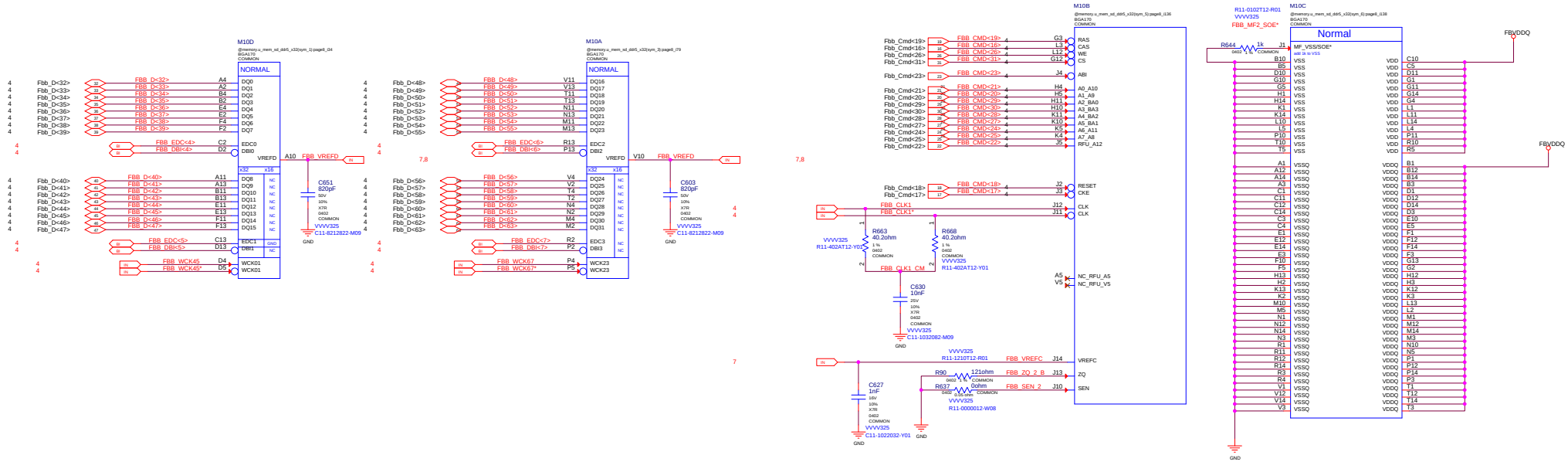


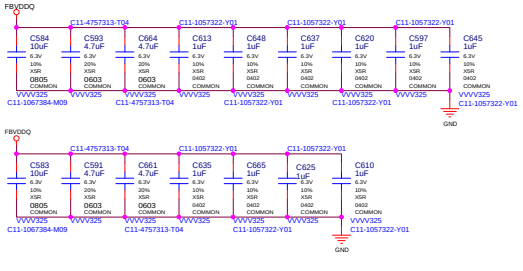




MICRO-STAR INT'L CO.,LTD		
MS-V325		
Size: Custom	Document Description: TABLE OF CONTENTS	Rev: 1.0
Date: Thursday, May 21, 2015	Sheet 7 of 42	

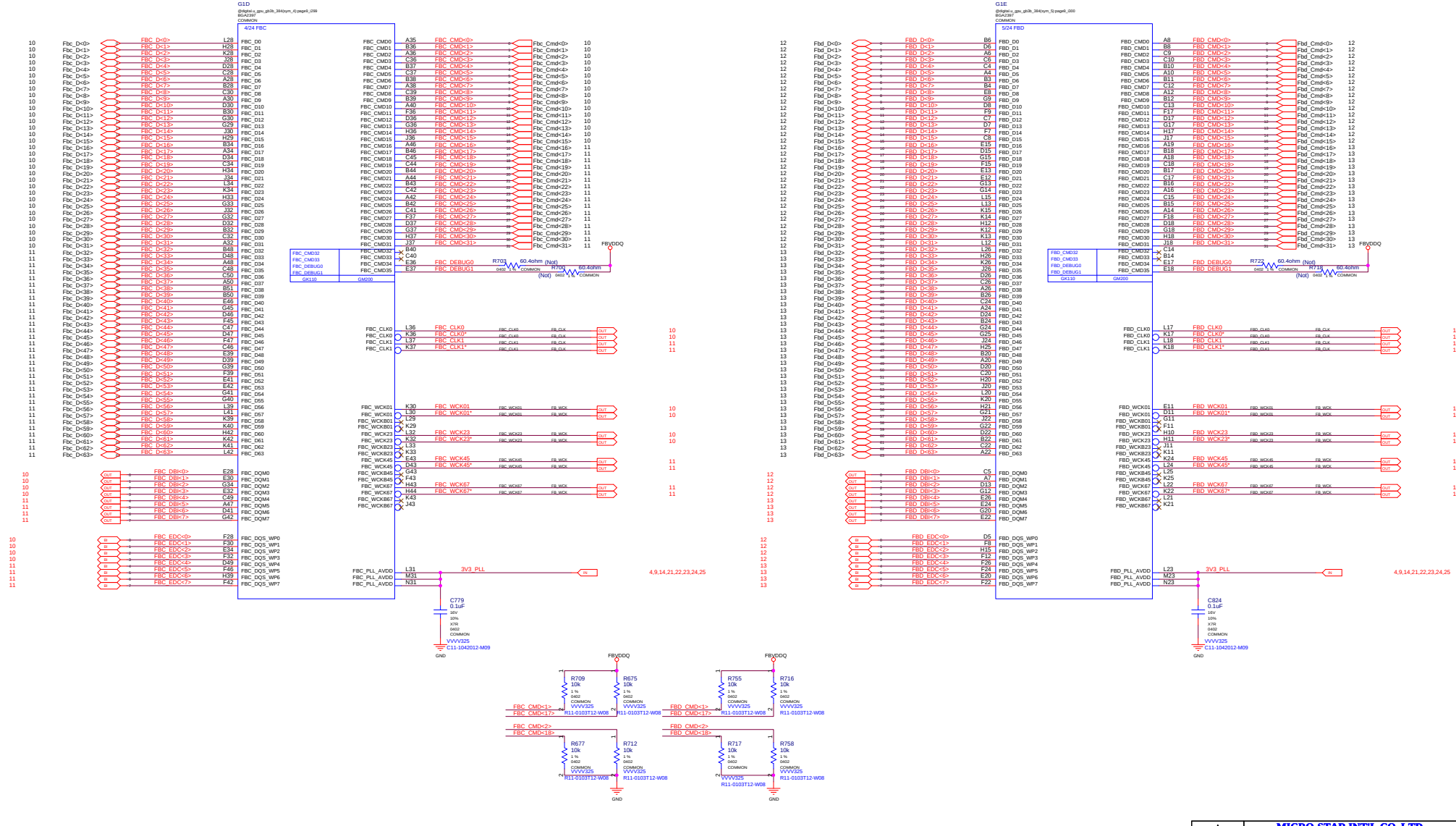
Page8: MEMORY: FBB Partition 63..32





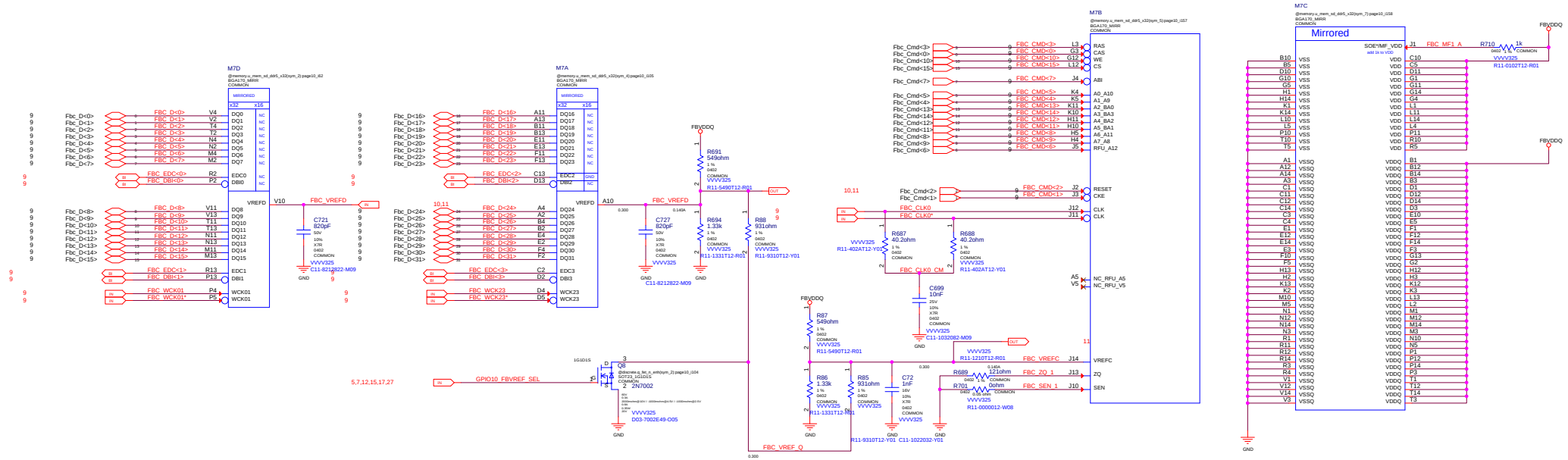
MICRO-STAR INT'L CO.,LTD		
MS-V325		
Size: Custom	Document Description: TABLE OF CONTENTS	Rev: 1.0
Date: Thursday, May 21, 2015	Sheet 8 of 42	

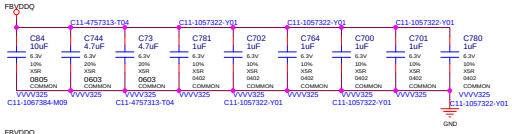
Page9: MEMORY: GPU Partition C/D

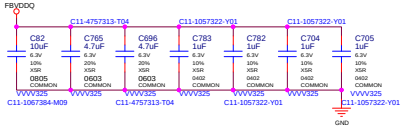


MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 9 of 42

Page10: MEMORY: FBC Partition 31..0

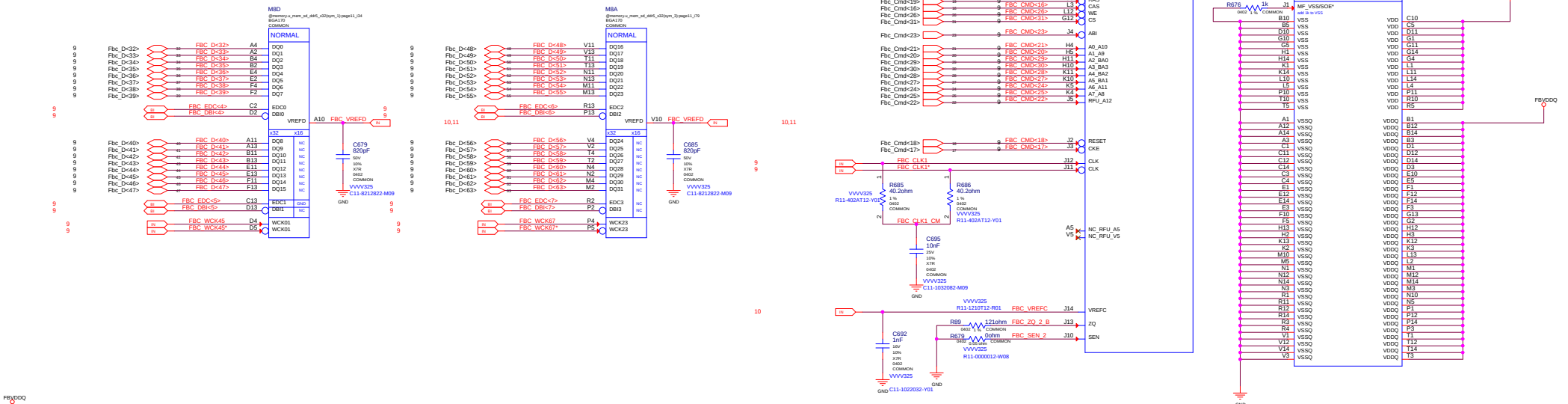






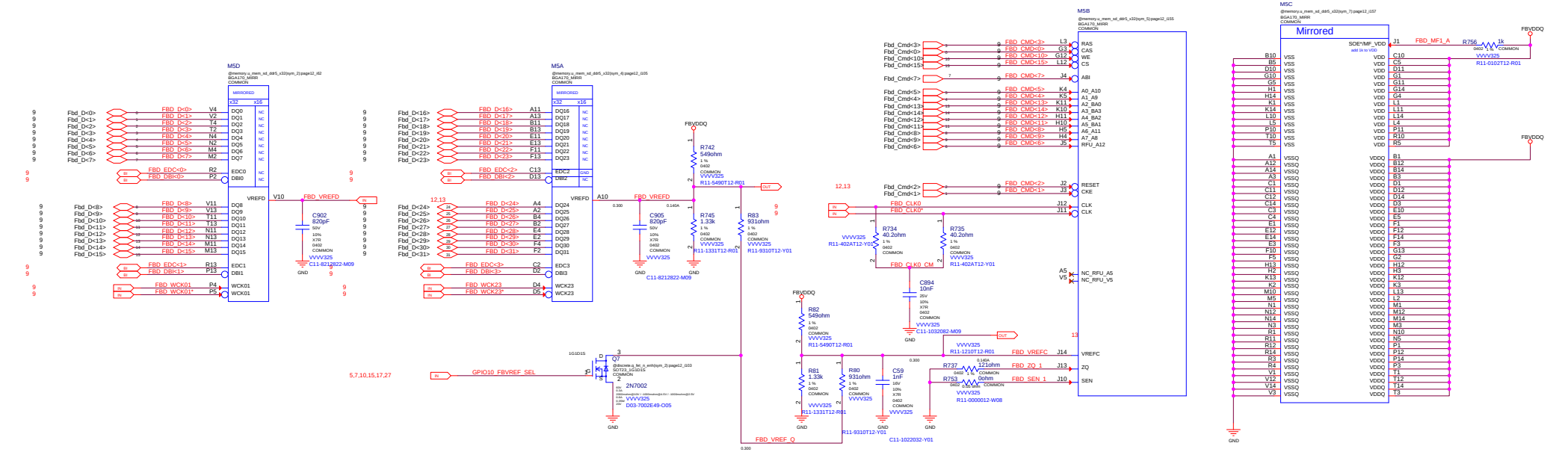
MICRO-STAR INT'L CO.,LTD		
MS-V325		
Size: Custom	Document Description: TABLE OF CONTENTS	Rev: 1.0
Date: Thursday, May 21, 2015	Sheet 10 of 42	

Page11: MEMORY: FBC Partition 63..32



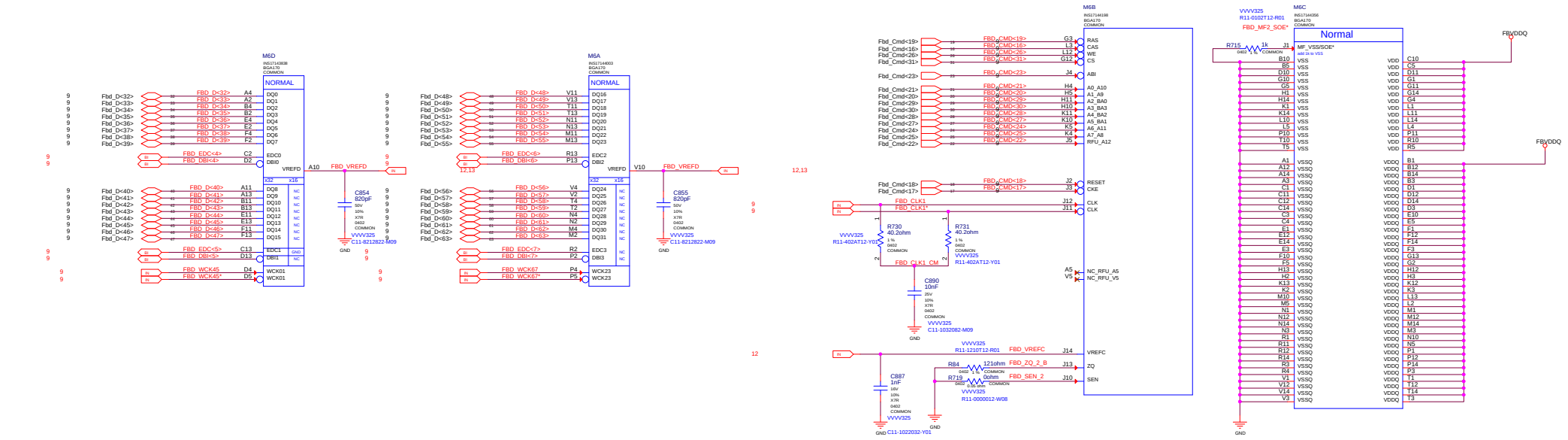
MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 11 of 42

Page12: MEMORY: FBD Partition 31..0



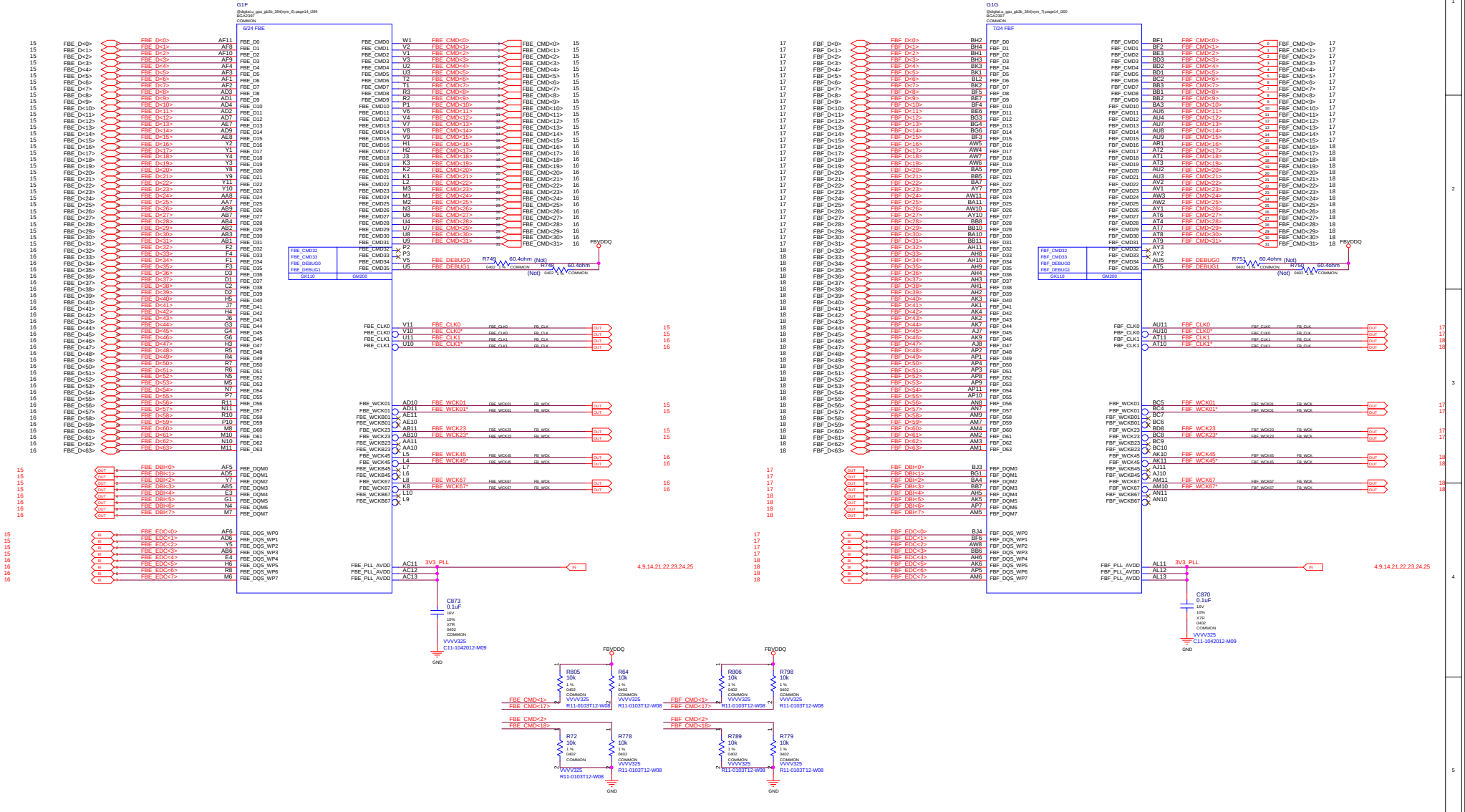
MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 12 of 42

Page13: MEMORY: FBD Partition 63..32

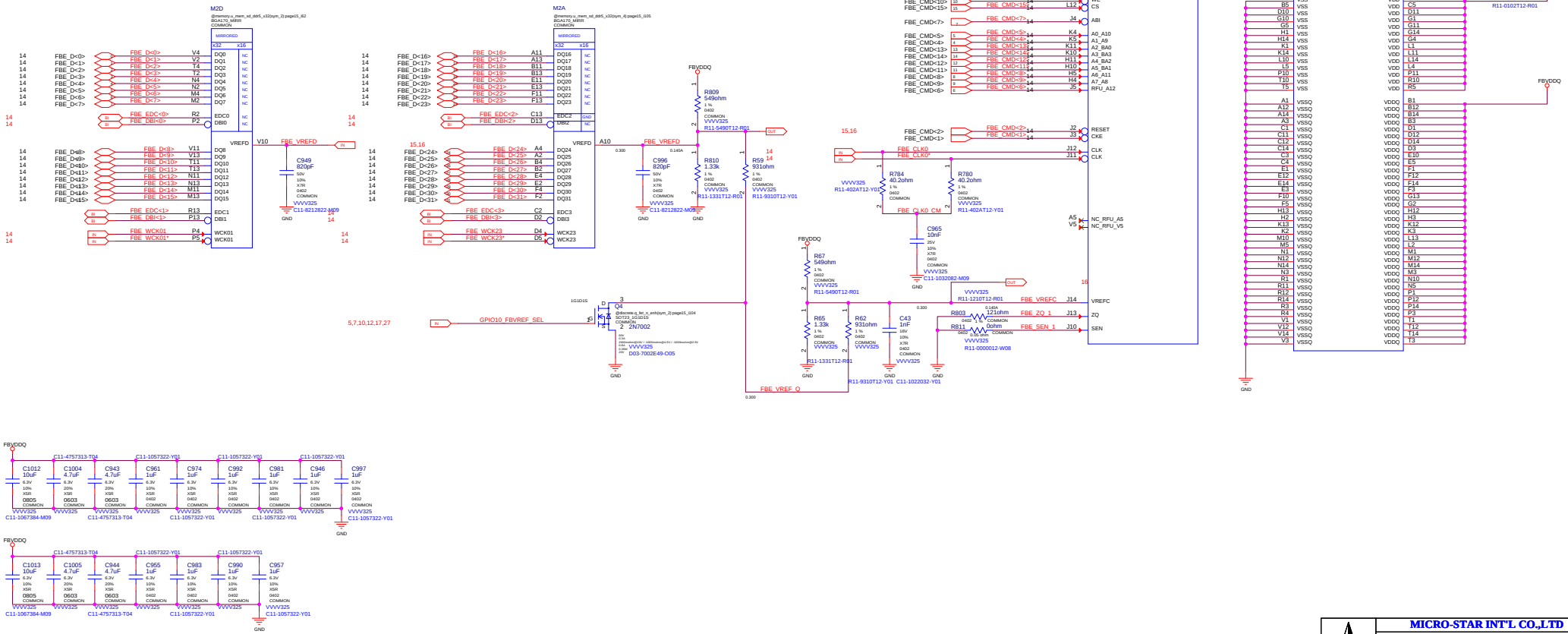


Company	MICRO-STAR INT'L CO.,LTD
Model	MS-V325
Size	Custom
Document Description	TABLE OF CONTENTS
Rev	1.0
Date	Thursday, May 21, 2015
Sheet	13 of 42

Page14: MEMORY: GPU Partition E/F

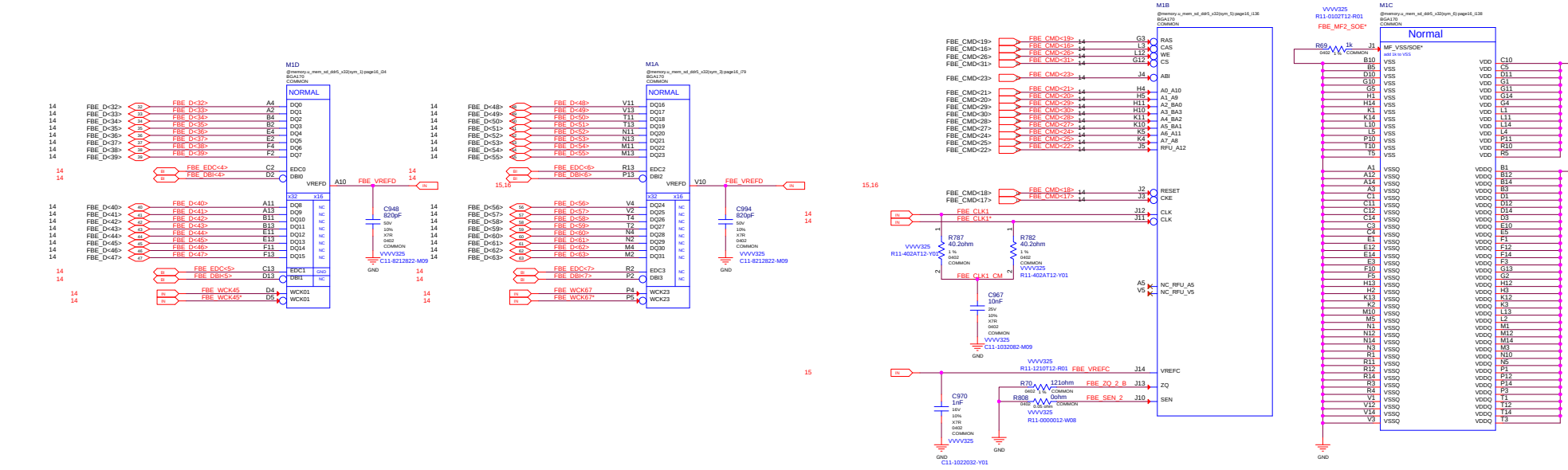


Page15: MEMORY: FBE Partition 31..0



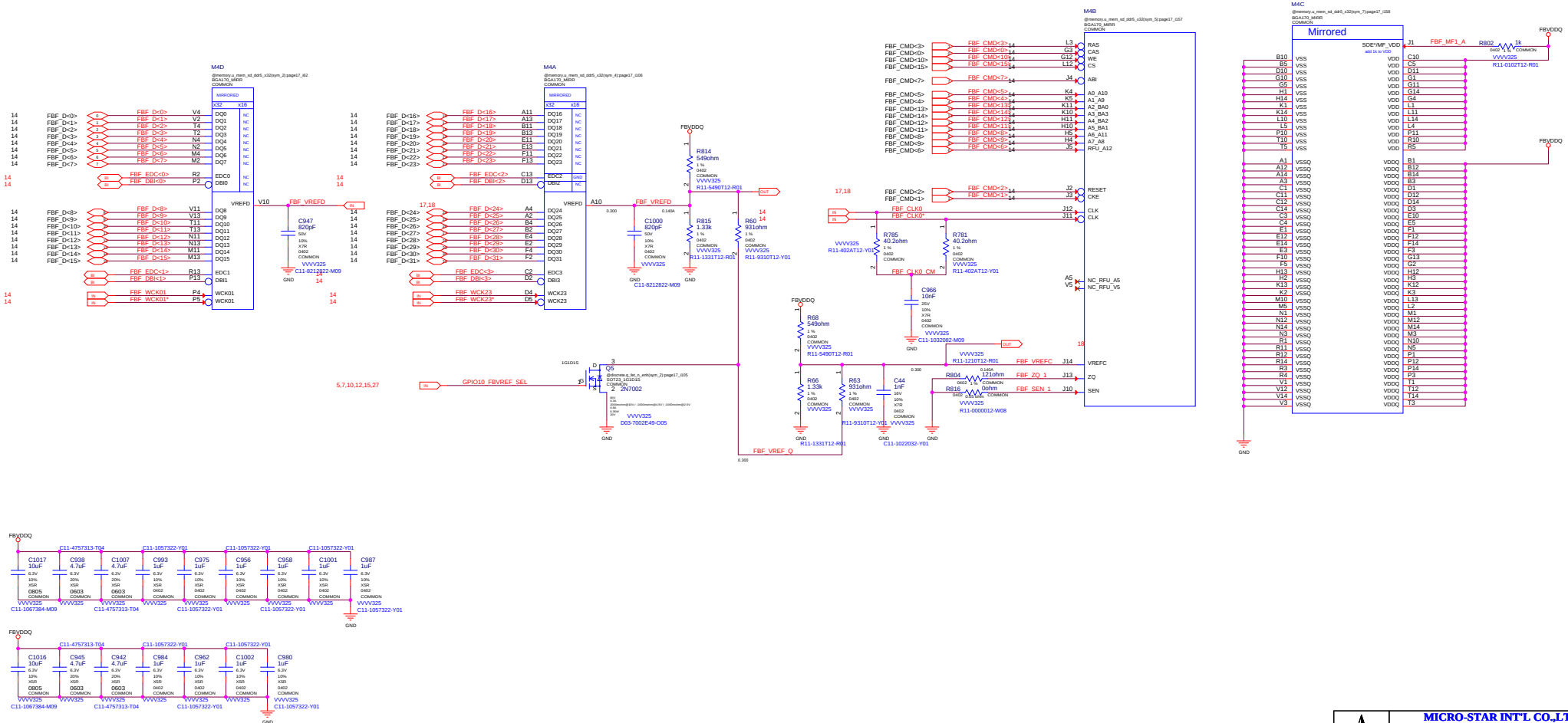
MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 15 of 42

Page16: MEMORY: FBE Partition 63..32



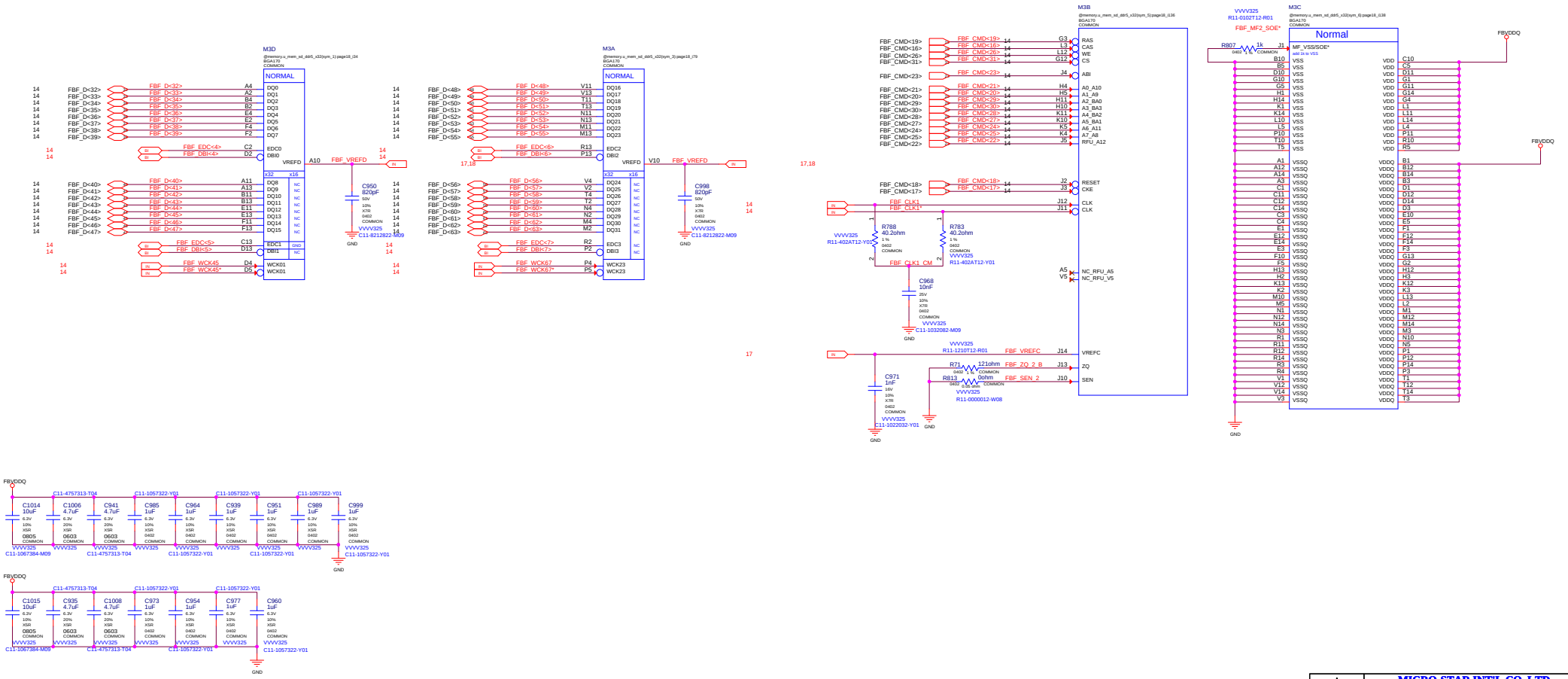
MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 16 of 42

Page17: MEMORY: FBF Partition 31..0



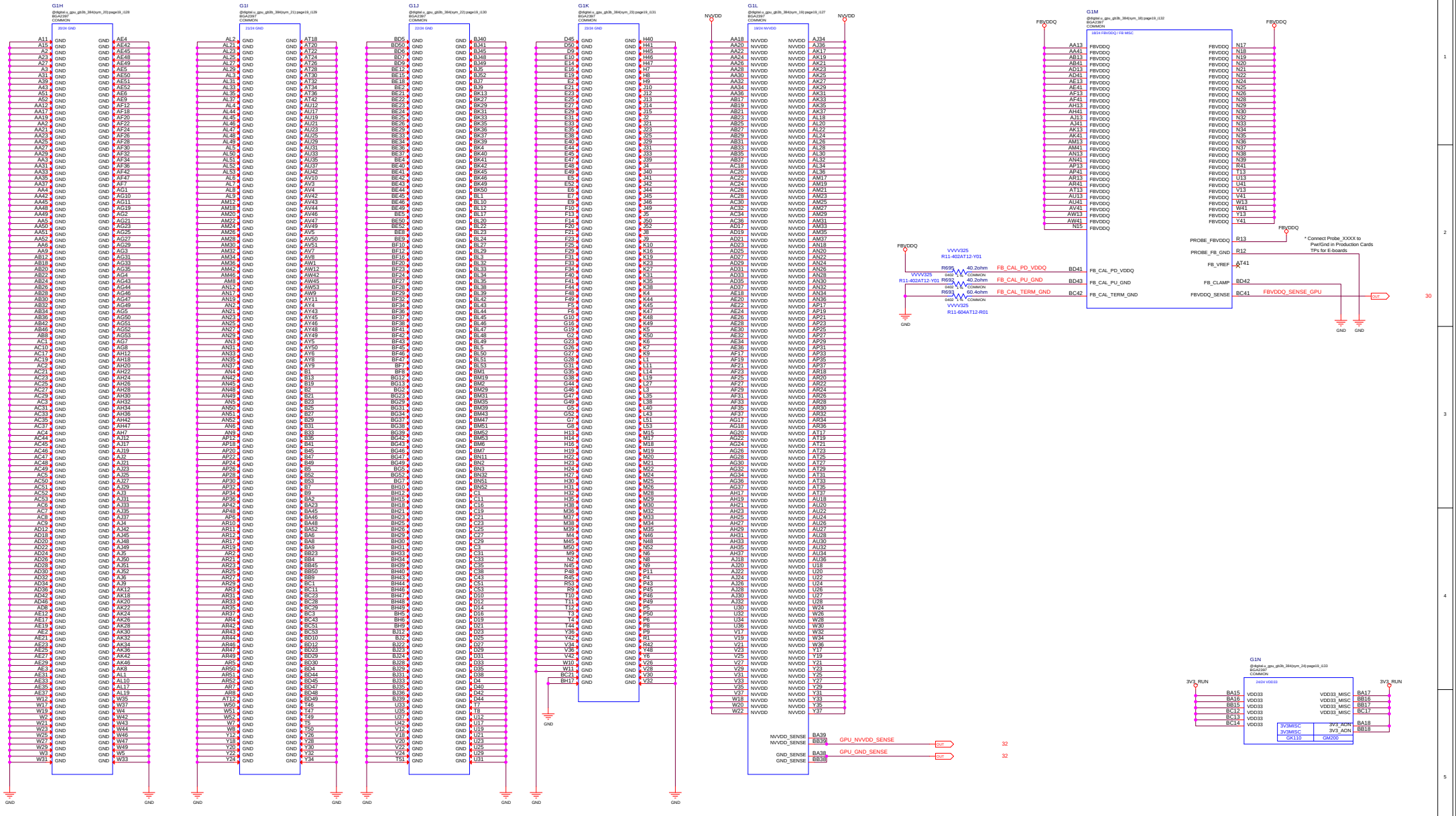
MICRO-STAR INT'L CO.,LTD		
MS-V325		
Size: Custom	Document Description: TABLE OF CONTENTS	Rev: 1.0
Date: Thursday, May 21, 2015	Sheet 17 of 42	

Page18: MEMORY: FBF Partition 63..32



MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 18 of 42

Page19: GPU PWR and GND



Page20: GPU Decoupling

Based on GB3-X GDDR5 FBVDDQ Decap Guideline

FBVDDQ

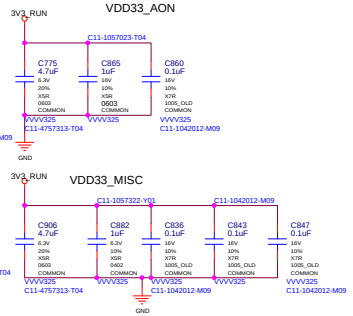
0.1uF, 1uF, 0402 (Place Under GPU)

4.7uF, 0603 (Place Near GPU)

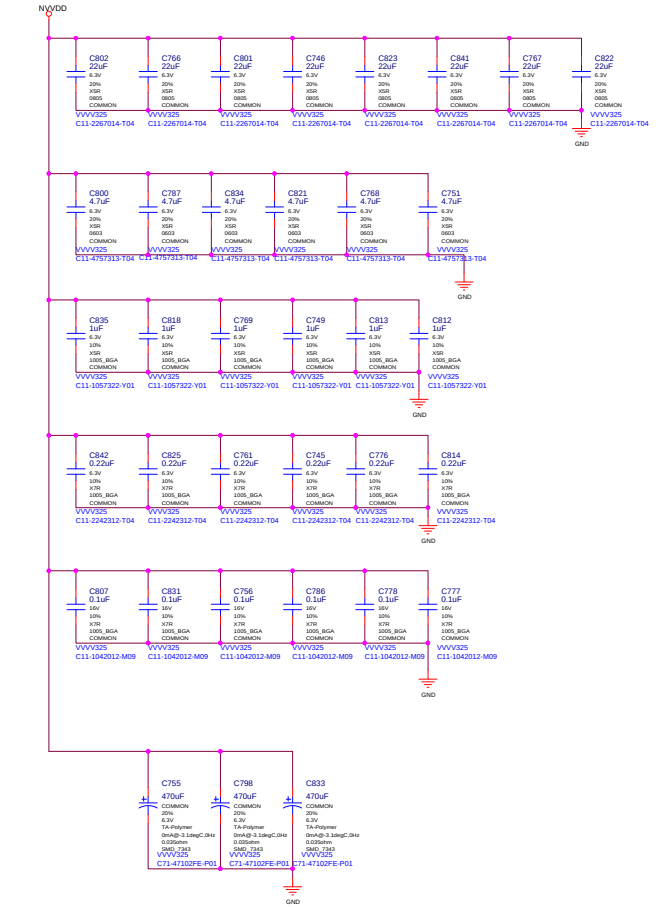
10uF, 0805 (Place Near GPU)

22uF, 0805 (Place Near GPU)

VDD33

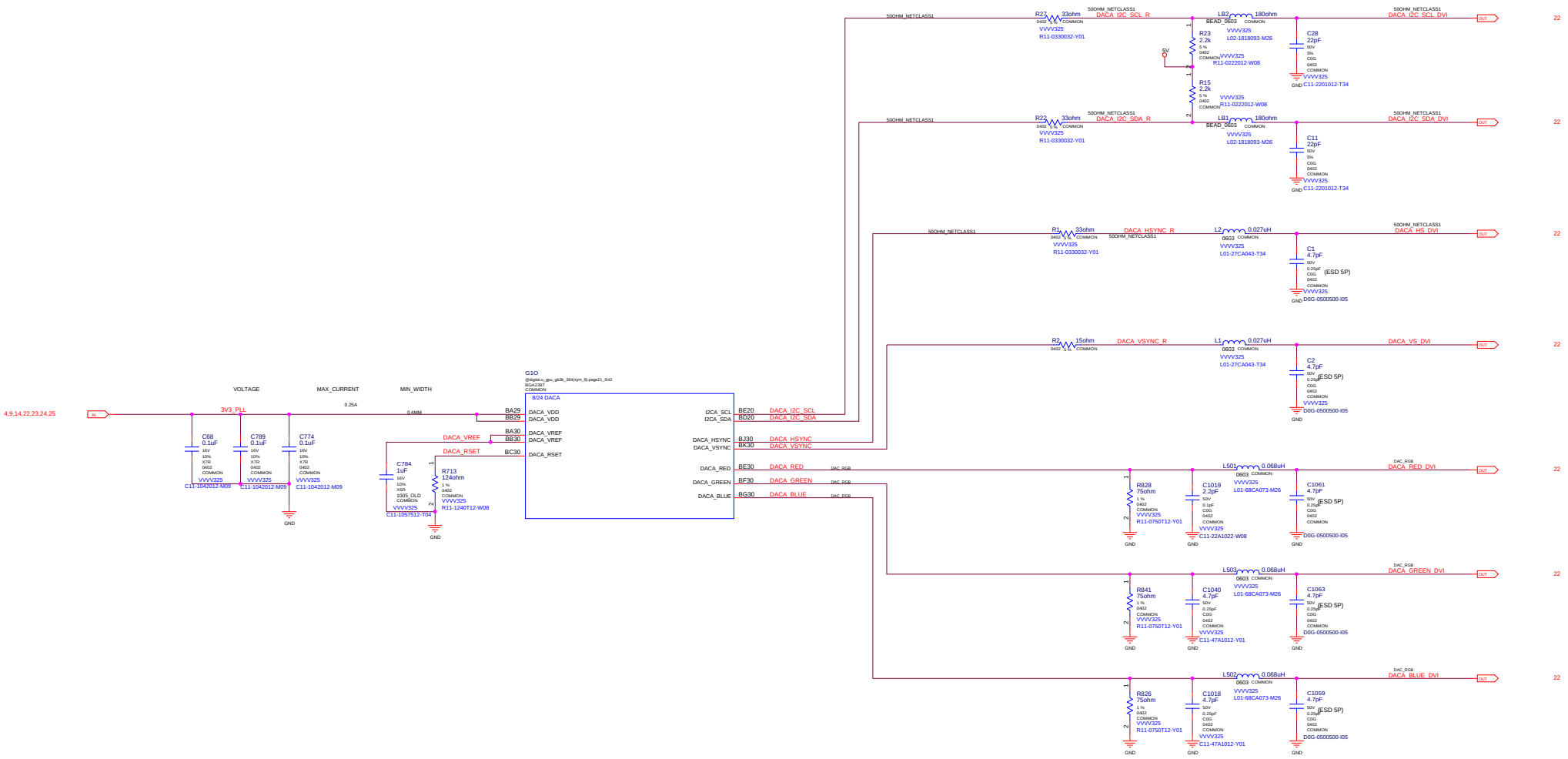


NVVDD Decoupling caps. Place under GPU.



MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 20 of 42

Page21: DACA Interface

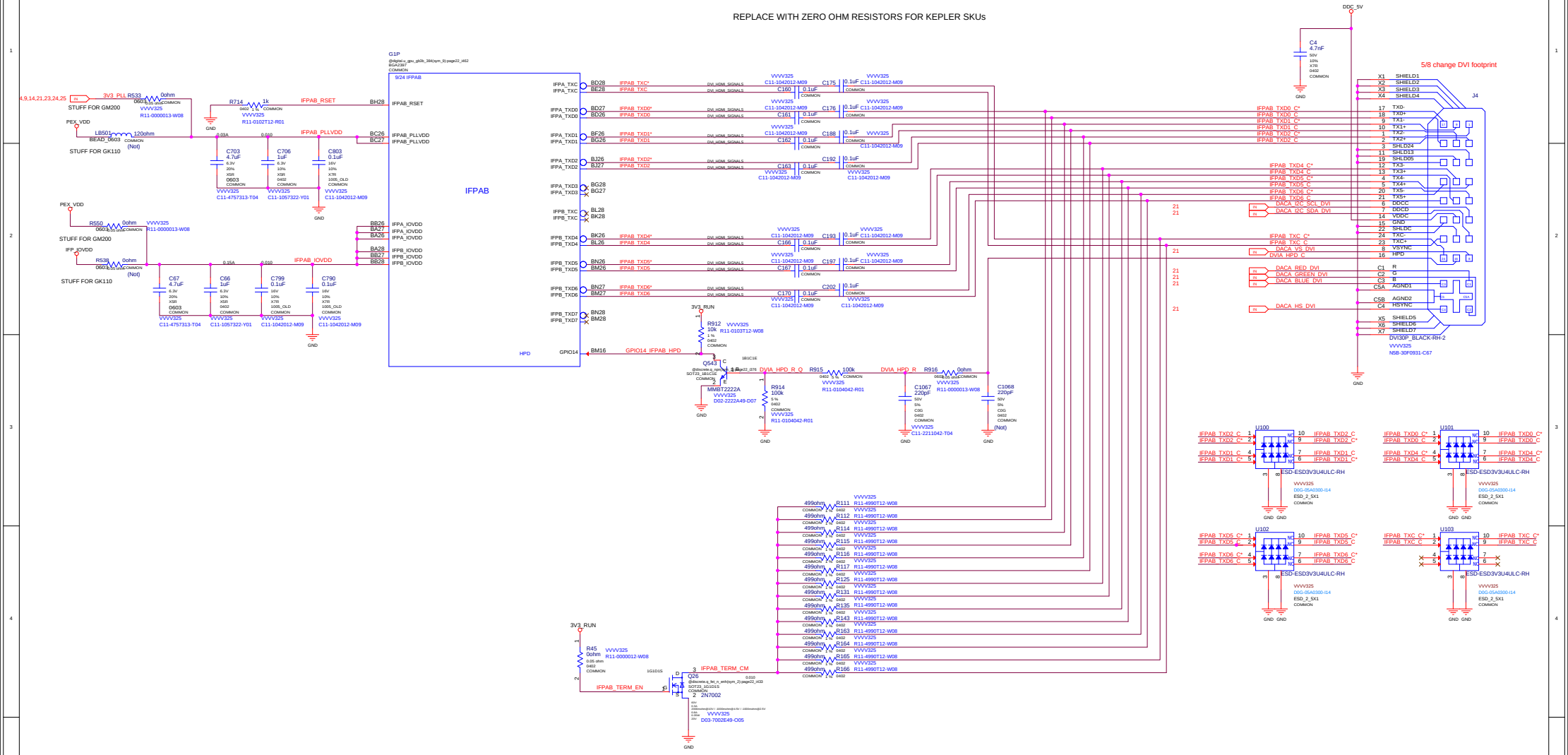


MICRO-STAR INT'L CO.,LTD		
MS-V325		
Size: Custom	Document Description: TABLE OF CONTENTS	Rev: 1.0
Date: Thursday, May 21, 2015	Sheet 21 of 42	

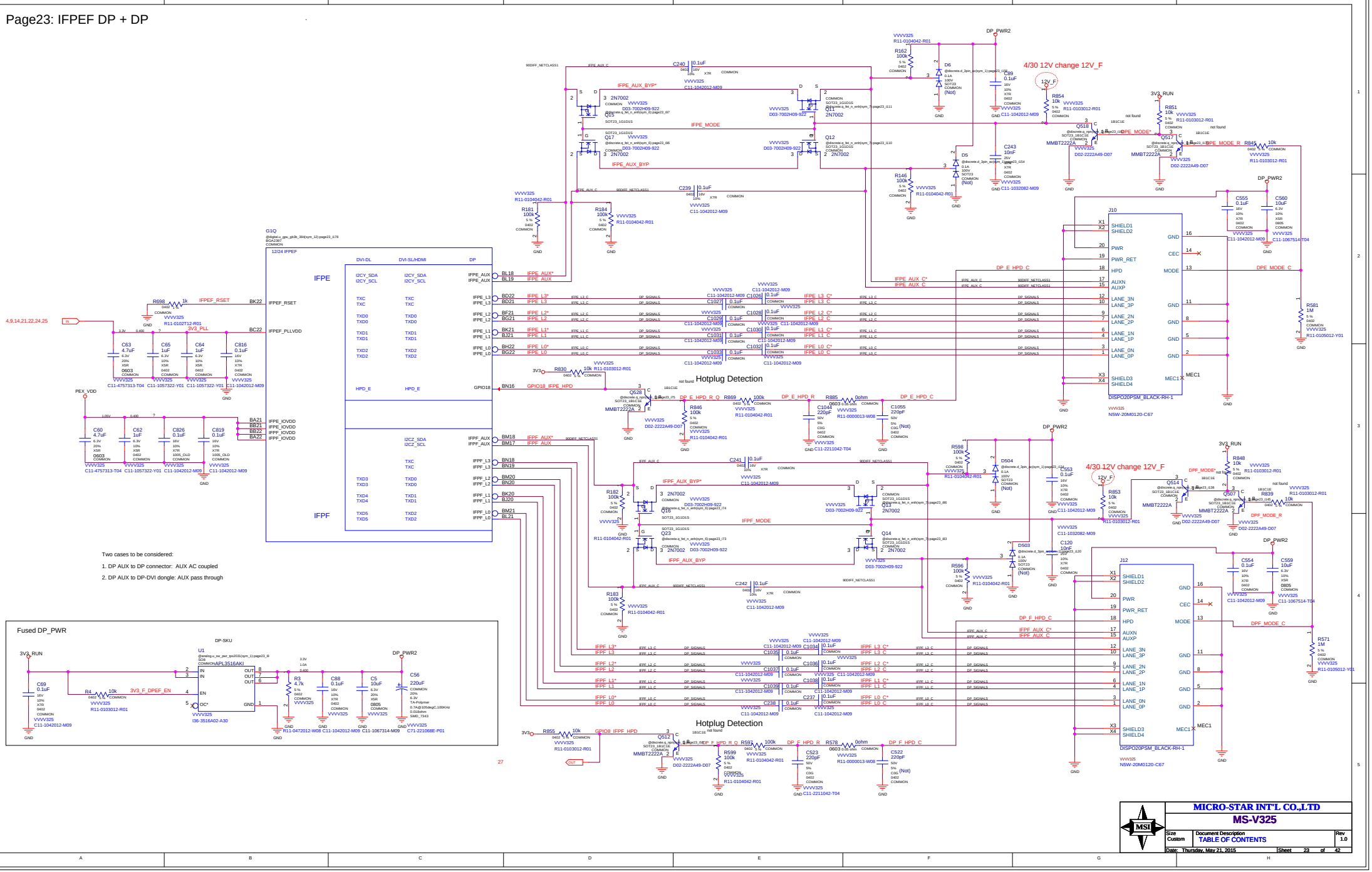
Page22: IFPAB DVI-I-DL

AC COUPLING NOT NEEDED for KEPLER

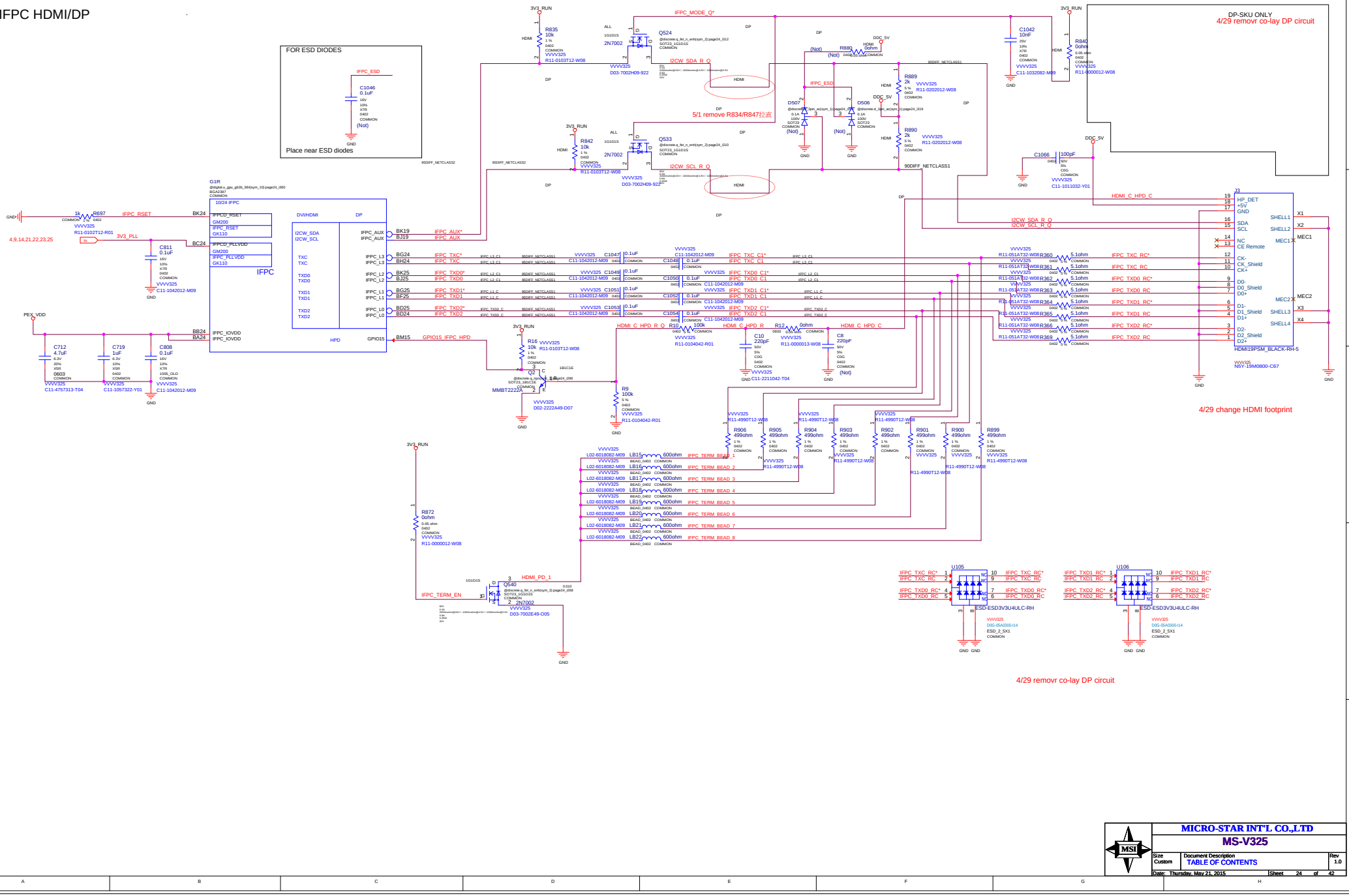
REPLACE WITH ZERO OHM RESISTORS FOR KEPLER SKUs



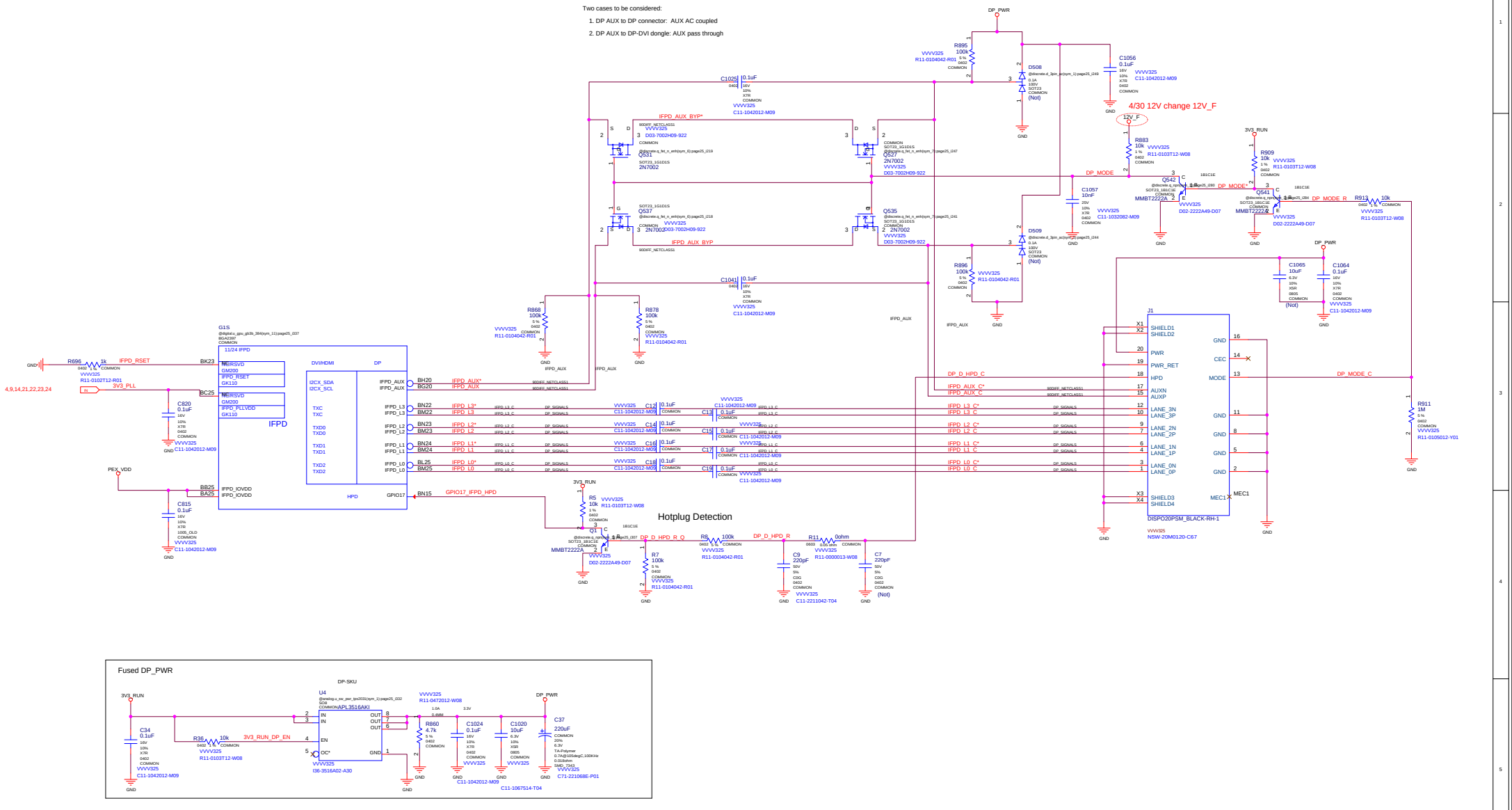
Page23: IFPEF DP + DP



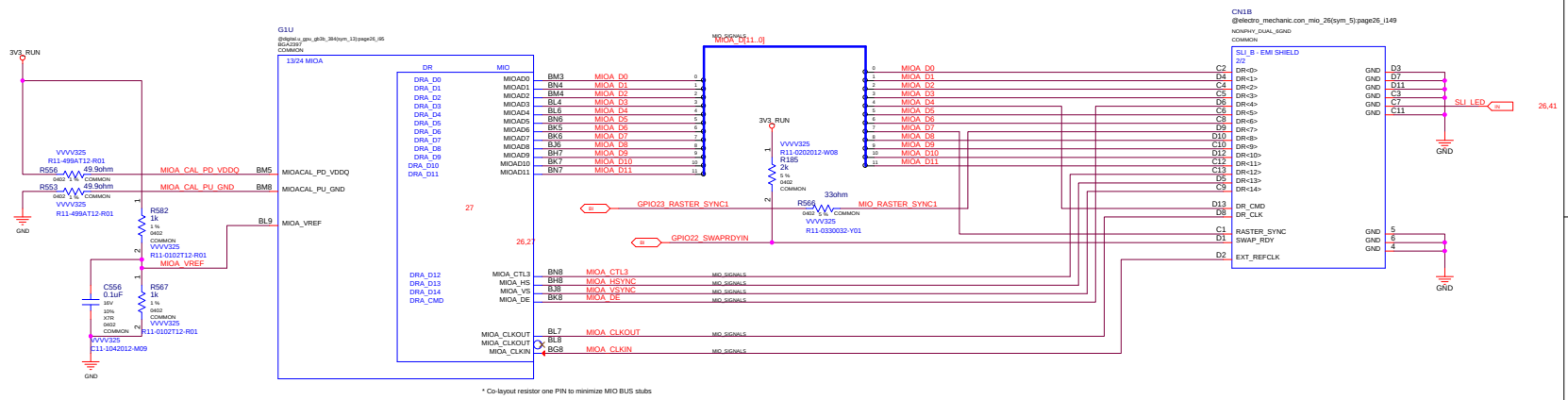
Page24: IFPC HDMI/DP



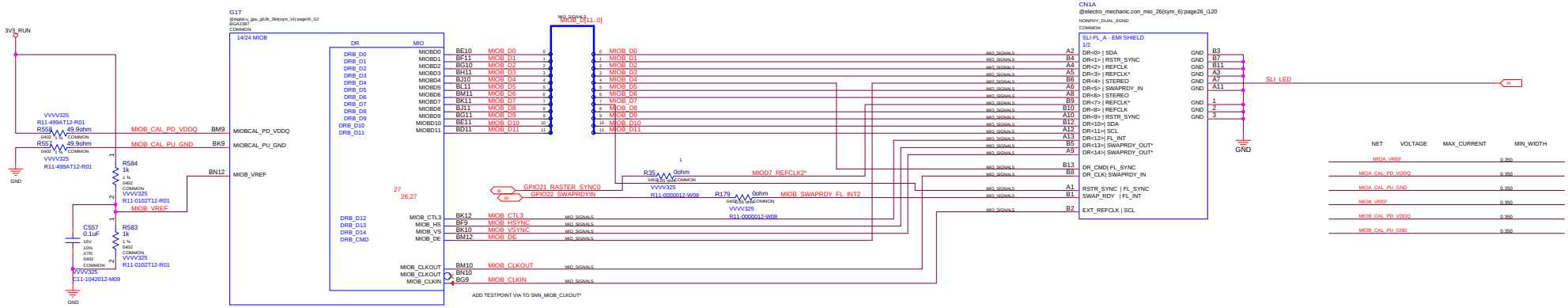
Page25: IFPD DP



Page26: MIOA/B and FRAMELOCK Interface



4/29 remove co-lay circuit



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF			0.350
MIOA_CAL_PD_VDDQ			0.350
MIOA_CAL_PU_GND			0.350
MIOB_VREF			0.350
MIOB_CAL_PD_VDDQ			0.350
MIOB_CAL_PU_GND			0.350

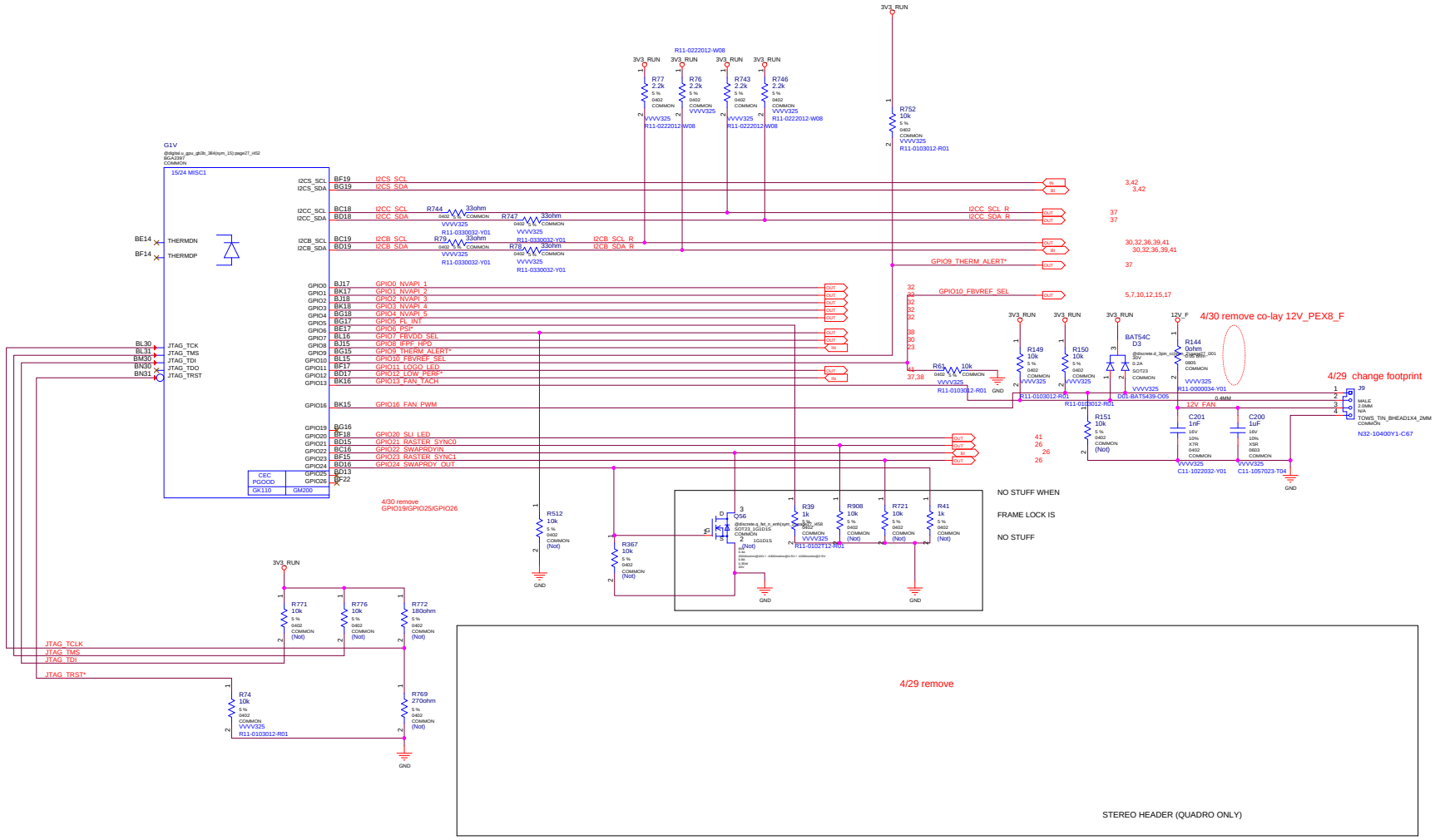
MICRO-STAR INT'L CO.,LTD

MS-V325

Size	Document Description	Rev
Custom	TABLE OF CONTENTS	1.0

Date: Thursday, May 21, 2015 | Sheet 26 of 42

Page27: MISC1: Fan, Thermal, JTAG, GPIO



MICRO-STAR INT'L CO.,LTD				
MS-V325				
Size: Custom	Document Description: TABLE OF CONTENTS			Rev: 1.0
Date: Thursday, May 21, 2015		Sheet 27 of 42		

195-0005-000
100k

Page28: MISC2: ROM, XTAL, Straps

		GK110	GM200	
STRAP0	USER_BIT [3:0]*	0000*	GC6_ENABLE(3.3V) PU	
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	N/A	
STRAP2	PCI_DEVID [3:0]*	100A*	N/A	
STRAP3	SOR_EXPOSED [3:0]*	1111*	N/A	
STRAP4 [LSB]	DP_PLL_VDD_33V*	1*	N/A	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	N/A	
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	N/A	
[MSB]	RESERVED	0*	N/A	
ROM_SI [LSB]	RAMCFG[0]*	1*	RAMCFG[0]*	
	RAMCFG[1]*	0*	RAMCFG[1]*	
	RAMCFG[2]*	1*	RAMCFG[2]*	
[MSB]	RAMCFG[3]*	0*	RAMCFG[3]*	
ROM_SO [LSB]	VGA_DEVICE*	1*	VGA_DEVICE*	1* For Enable
	SMB_ALT_ADDR*	0*	SMB_ALT_ADDR	0* For Disable
	FB[0]_APERTURE_SIZE*	1* For 128MB*	PCIE_CFG	0* For Desktop
[MSB]	FB[1]_APERTURE_SIZE*	0* For 128MB*	DEVID_SEL	0* For DEVID A
ROM_SCLK [LSB]	PEX_PLL_EN_TERM100*	0* DISABLED*	SOR0_EXPOSED	
	PCI_DEVID_EXT[5]*	0*	SOR1_EXPOSED	
	SUB_VENDOR*	1* Dedicated BIOS*	SOR2_EXPOSED	
[MSB]	PCI_DEVID_EXT[4]*	0*	SOR3_EXPOSED	

MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

x32 DENSITY MODE STRAPS

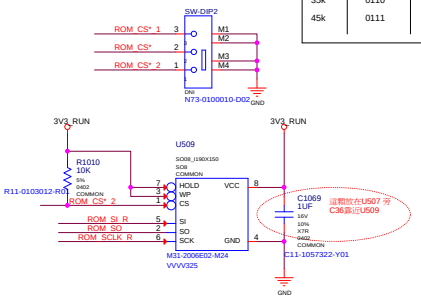
CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	128Mx32 384-bit	Elpida
0010	128Mx32 384-bit	Hynix
0011	128Mx32 384-bit	Samsung
0100	64Mx32 384-bit	Hynix B
0101	64Mx32 384-bit	Elpida
0110	64Mx32 384-bit	Hynix
0111	64Mx32 384-bit	Samsung
1000	Reserved	
1001	128Mx32 320-bit	Elpida
1010	128Mx32 320-bit	Hynix
1011	128Mx32 320-bit	Samsung
1100	64Mx32 320-bit	Hynix B
1101	64Mx32 320-bit	Elpida
1110	64Mx32 320-bit	Hynix
1111	128Mx32 320-bit	Samsung

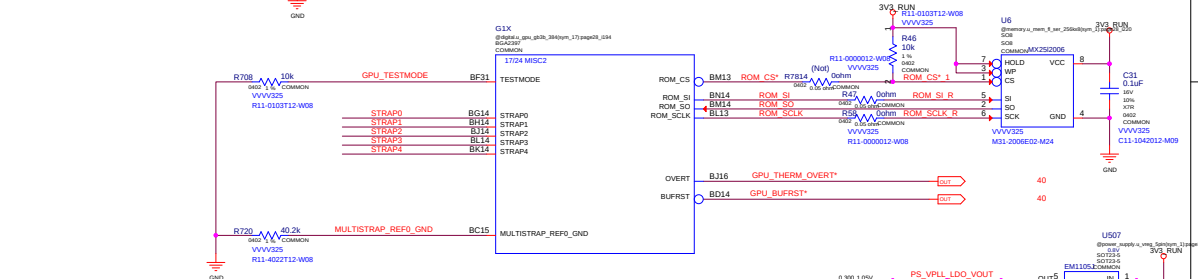
x16 DENSITY MODE STRAPS

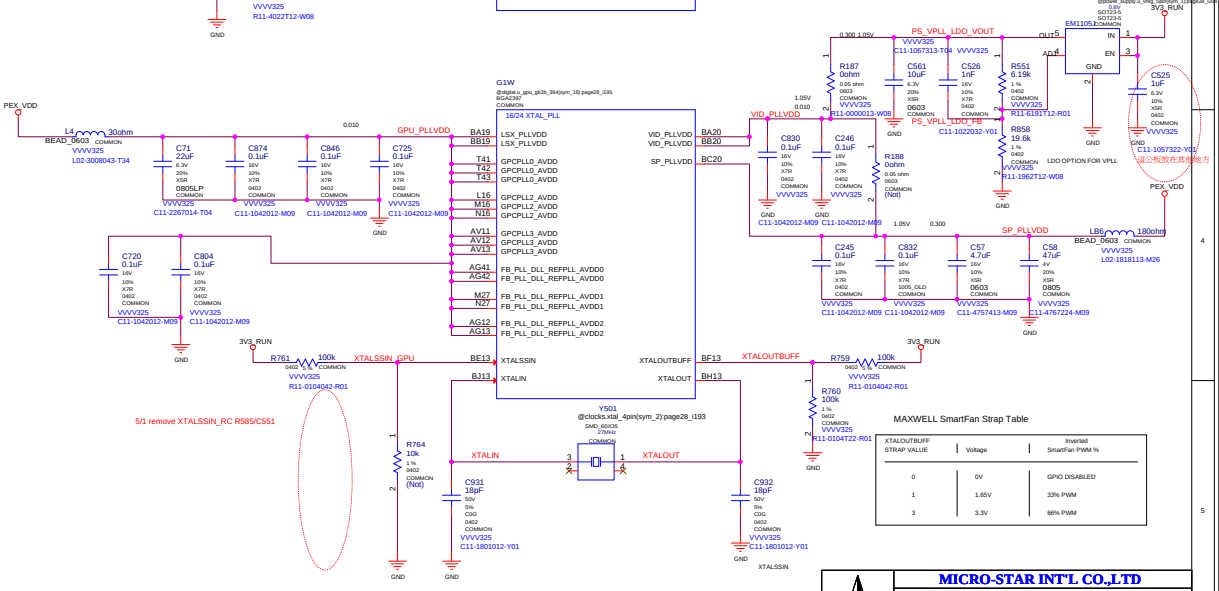
CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	256Mx16 384-bit	Elpida
0010	256Mx16 384-bit	Hynix
0011	256Mx16 384-bit	Samsung
0100	128Mx16 384-bit	Hynix B
0101	128Mx16 384-bit	Elpida
0110	128Mx16 384-bit	Hynix
0111	128Mx16 384-bit	Samsung
1000	Reserved	
1001	256Mx16 320-bit	Elpida
1010	256Mx16 320-bit	Hynix
1011	256Mx16 320-bit	Samsung
1100	128Mx16 320-bit	Hynix B
1101	128Mx16 320-bit	Elpida
1110	128Mx16 320-bit	Hynix
1111	128Mx16 320-bit	Samsung

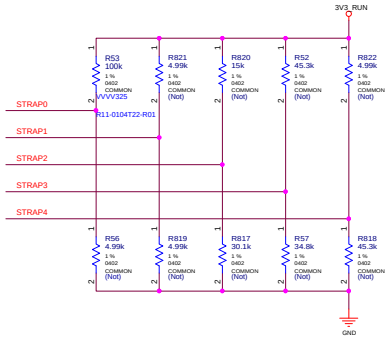
4/27 add circuit

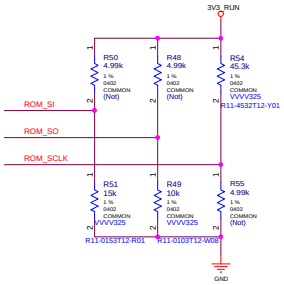
Dual BIOS











MAXWELL SmartFan Strap Table

XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	1.65V	33% PWM
3	3.3V	66% PWM

MICRO-STAR INT'L CO.,LTD

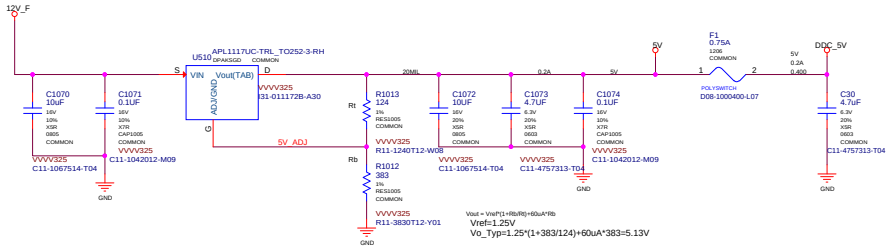
MS-V325

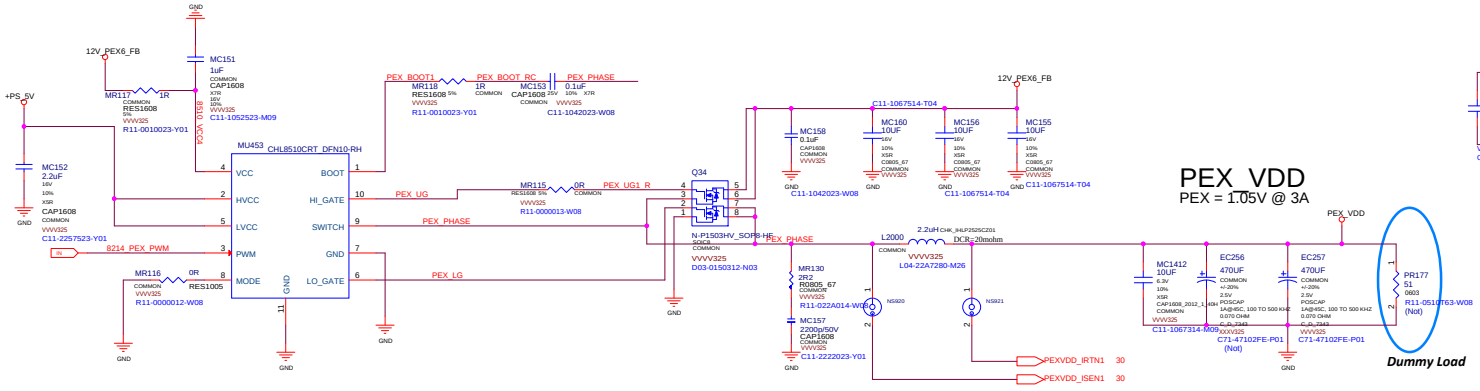
Size	Document Description	Rev
Custom	TABLE OF CONTENTS	1.0

Date: Thursday, May 21, 2015 Sheet 28 of 42

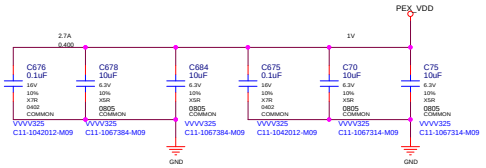
Page29: PS: 5V, PEX_VDD

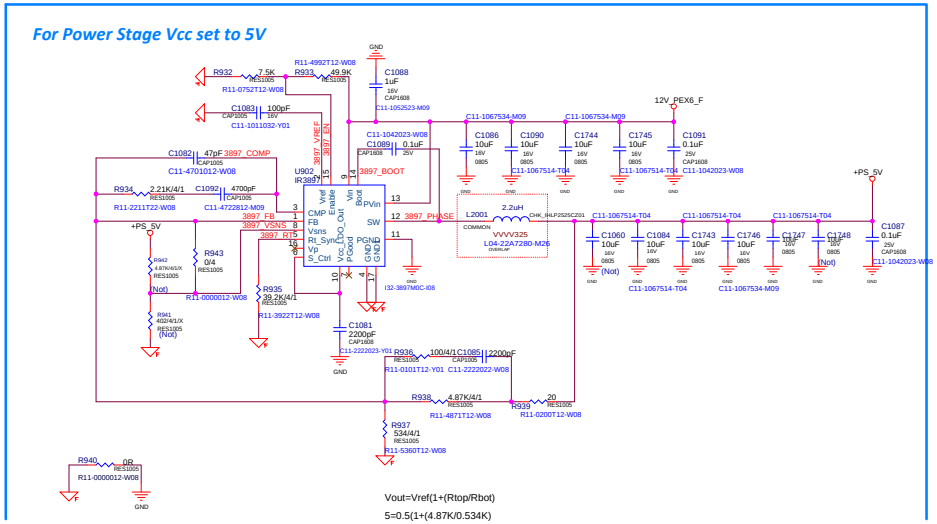
4/27 change 5V circuit
4/29 chnage PEX_VDD circuit
4/29 add 5V Driver Vcc





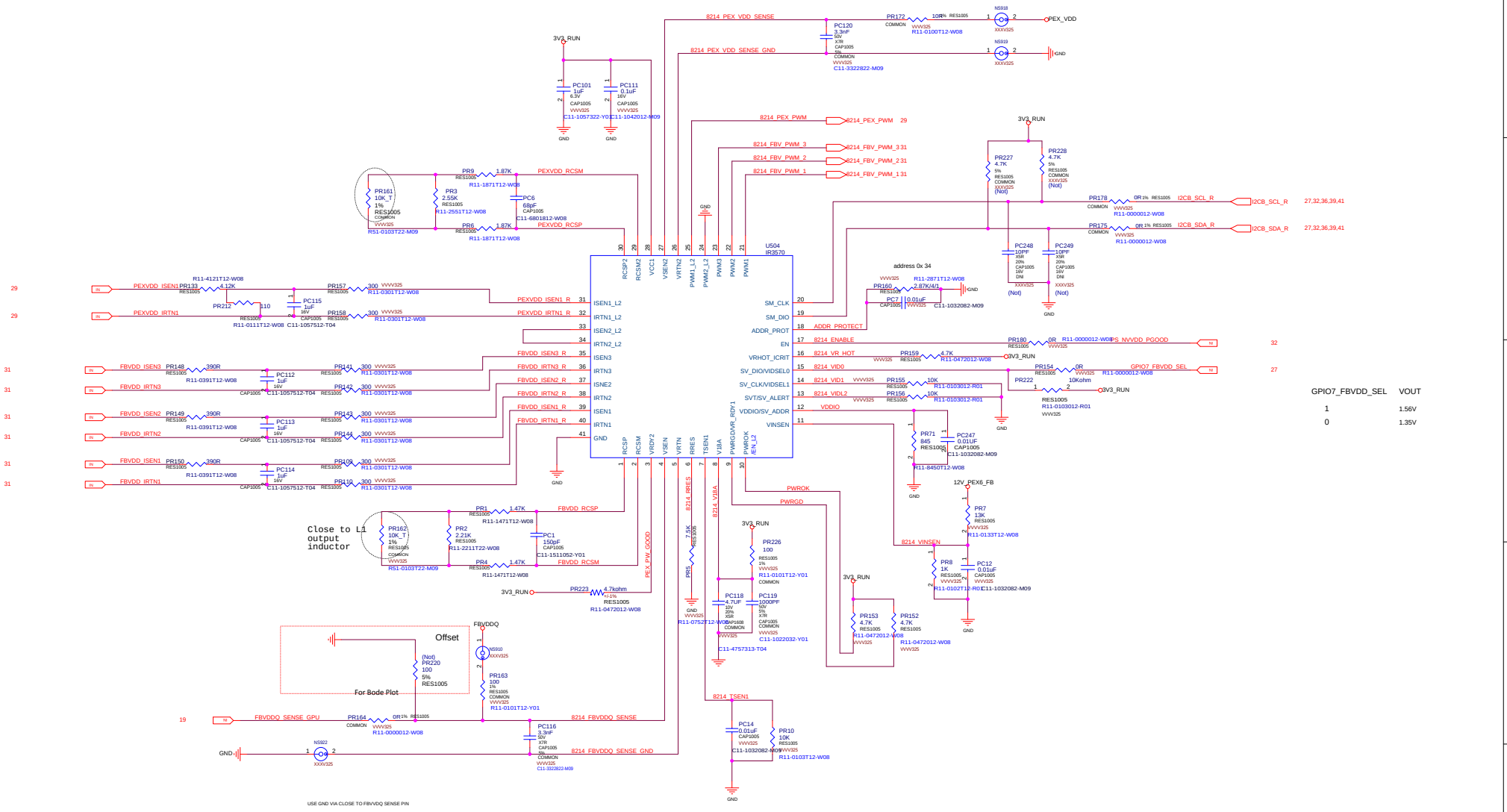
PEX_VDD
PEX = 1.05V @ 3A





Vout=Vref(1+(Rtop/Rbot)
5=0.5(1+(4.87K/0.534K)
7=0.5(1+(4.87K/0.374K)
8=0.5(1+(4.87K/0.324K)
9=0.5(1+(4.87K/0.287K)
10=0.5(1+(4.87K/0.255K)

MICRO-STAR INT'L CO.,LTD		
MS-V325		
Size: Custom	Document Description: TABLE OF CONTENTS	Rev: 1.0
Date: Thursday, May 21, 2015	Sheet 29 of 42	



GPIO7_FBVDD_SEL	VOUT
1	1.56V
0	1.35V

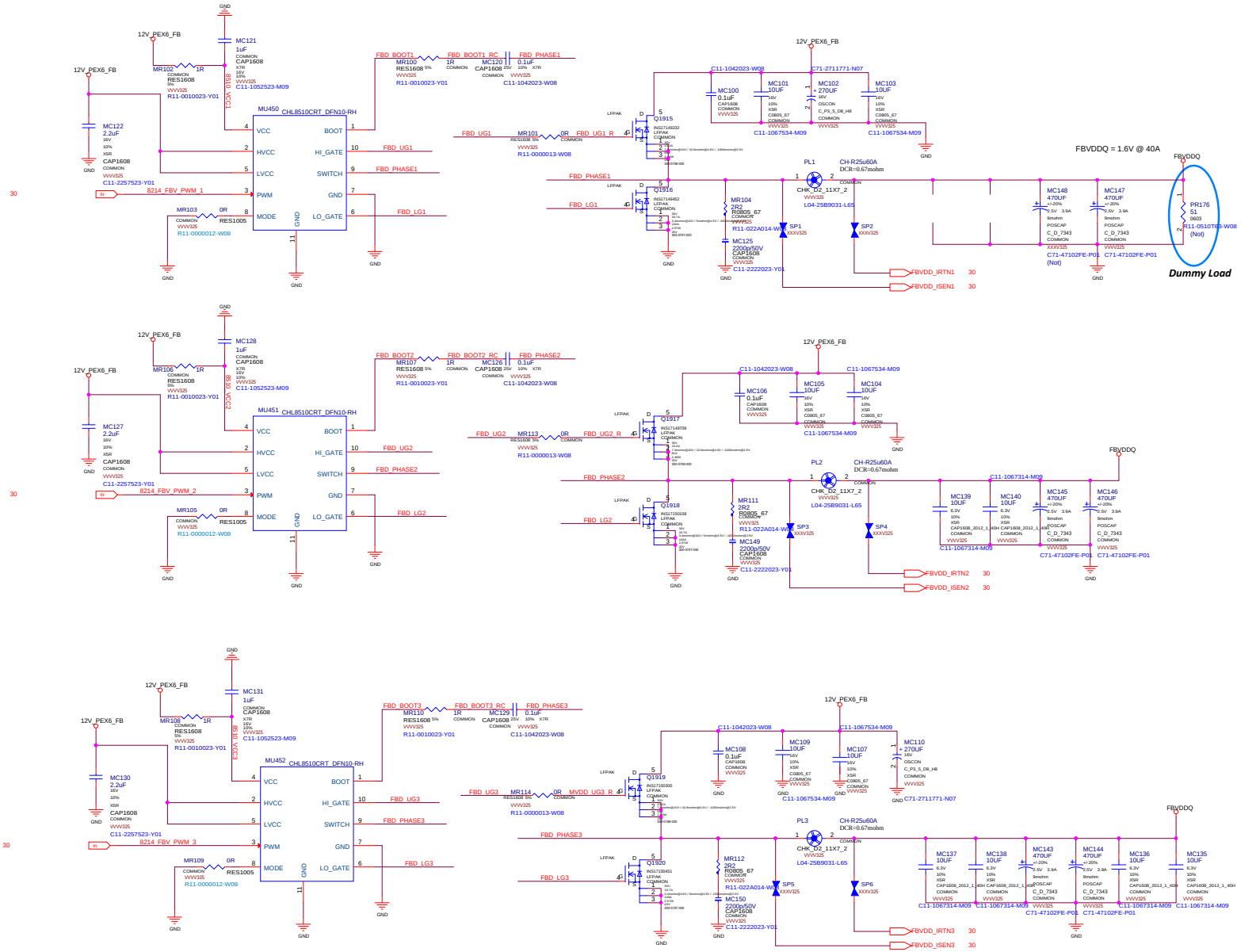
MICRO-STAR INT'L CO.,LTD

MS-V325

Size: Custom | Document Description: TABLE OF CONTENTS | Rev: 1.0

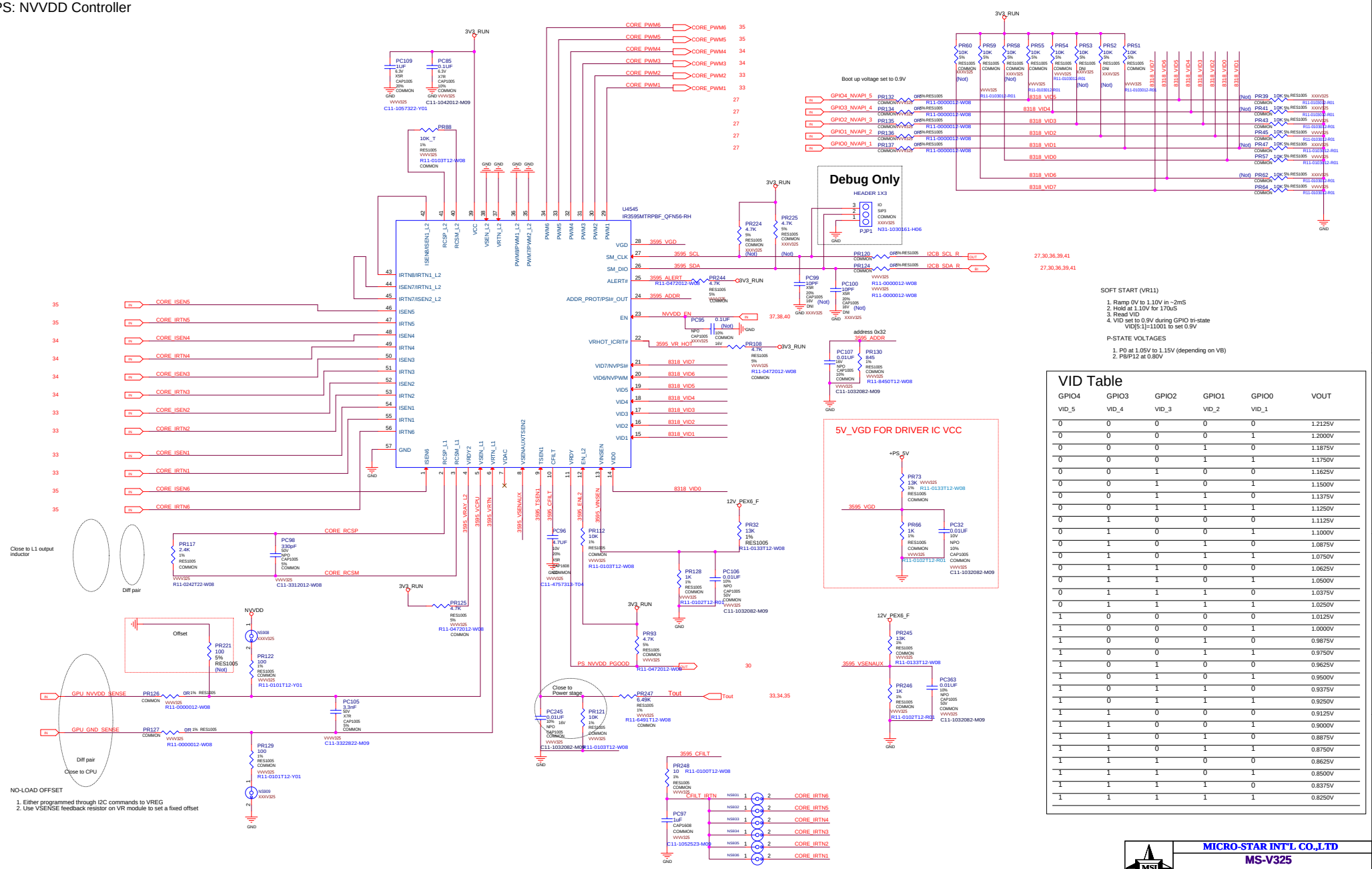
Date: Friday, May 22, 2015 | Sheet 30 of 42

Page31: PS: FBVDDQ



MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 31 of 42

Page32: PS: NVVDD Controller

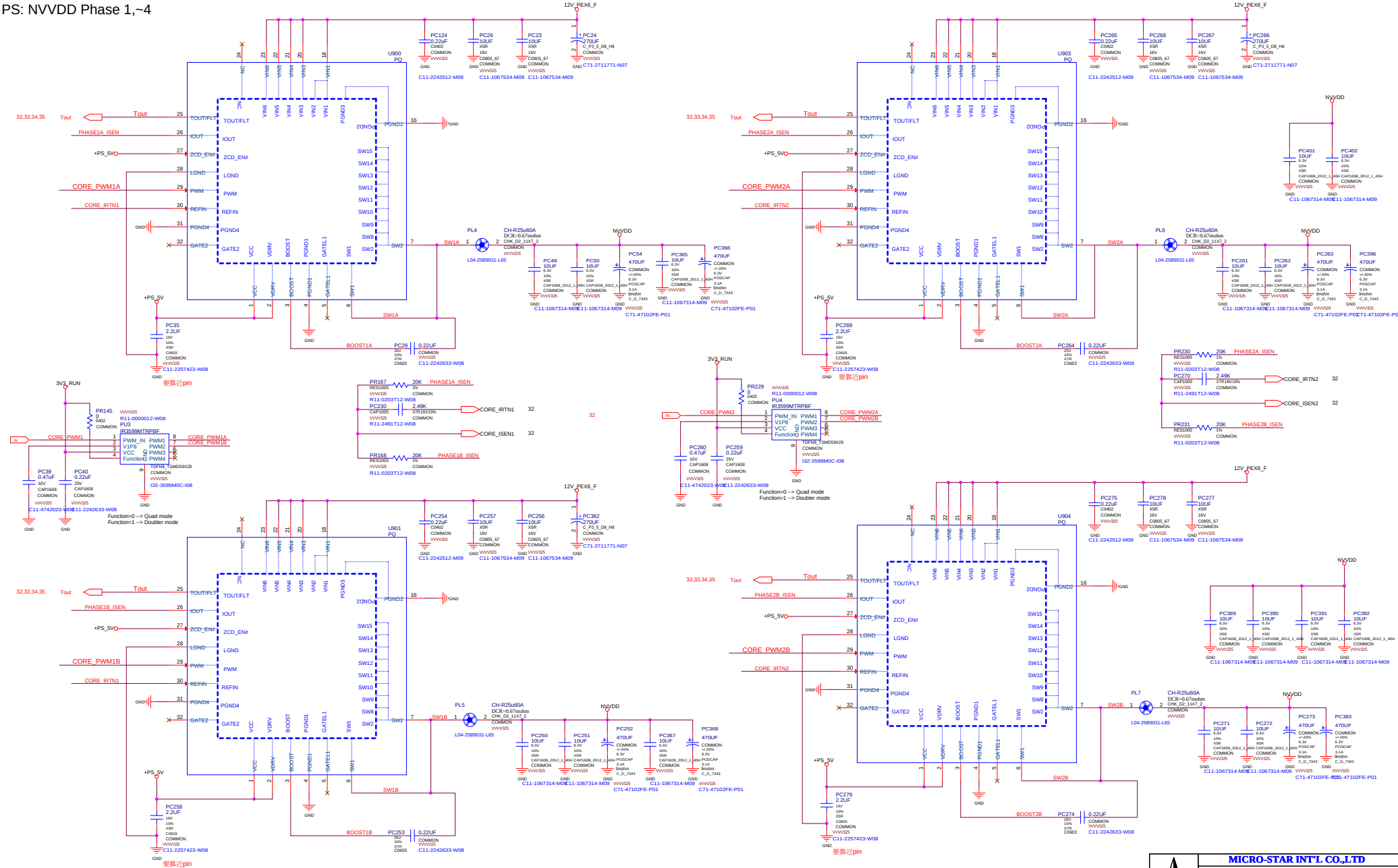


VID Table

GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

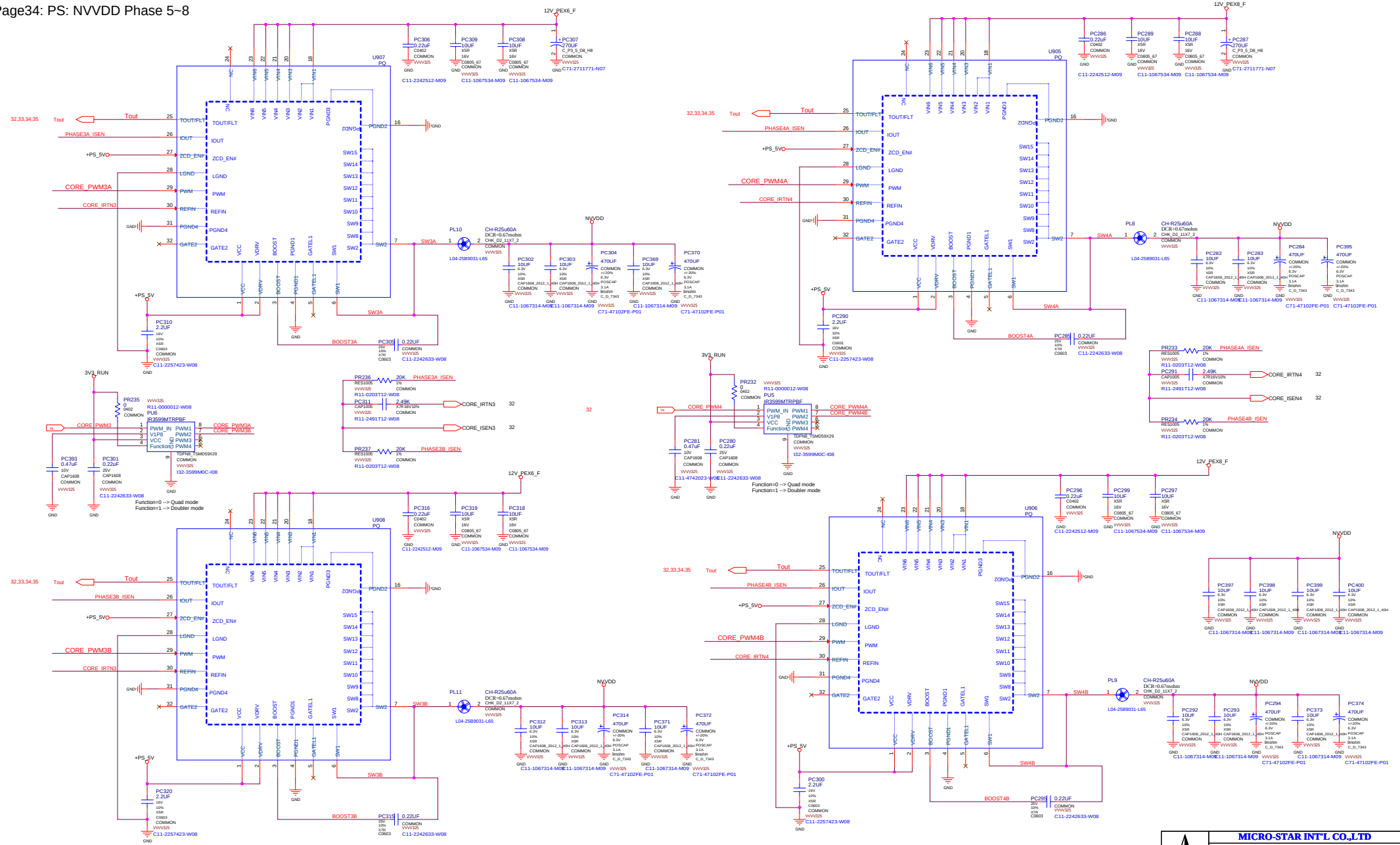
MICRO-STAR INT'L CO.,LTD		
MS-V325		
Size: Custom	Document Description: TABLE OF CONTENTS	Rev: 1.0
Date: Friday, May 22, 2015	Sheet 32 of 42	

Page33 PS: NVVDD Phase 1,~4



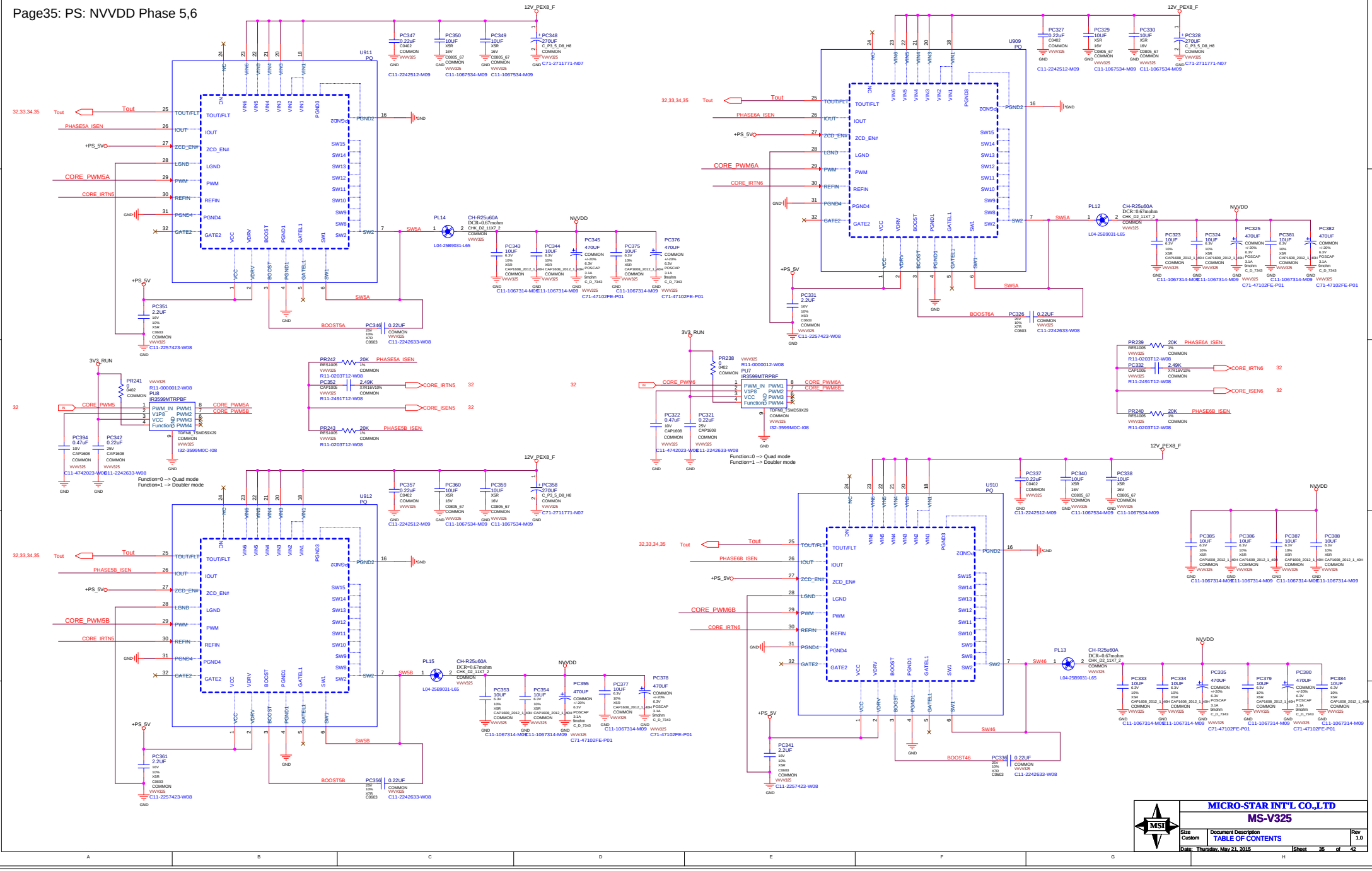
MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 33 of 42

Page34: PS: NVVDD Phase 5~8



MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 34 of 42

Page35: PS: NVVDD Phase 5,6



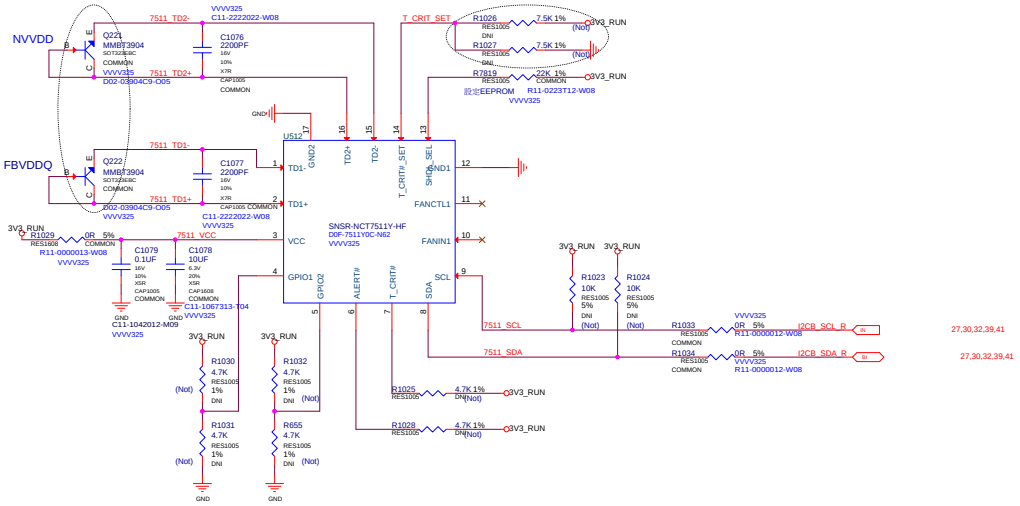
Page36: PS: NVVDD Dynamic Switch Phases

Thermal IC : NCT7511Y

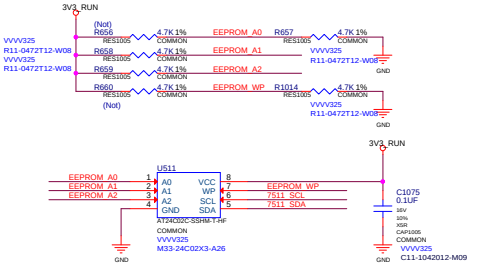
Layout notice :
*Add ground shielding for D+ and Dtraces.
*D+/D- route has to be away from the high noise area.
*The recommended traces width and ground shielding spacing are 10mils.

Please refer datasheet
TCRIT_SET Table
If floating,shutdown temp. set to 65℃

Thermal Diode



EEPROM

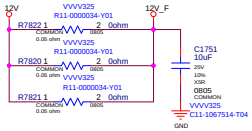


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS	Rev: 1.0
Date: Thursday, May 21, 2015	Sheet 36 of 42	

Page37: PS: Inputs, Filtering, and Monitoring

4/29 remove 12V_PEX8_VIN2 to 12V_PEX_VIN1, change and add EXT-POWER connector circuit

PEX_12V INPUT - 66W



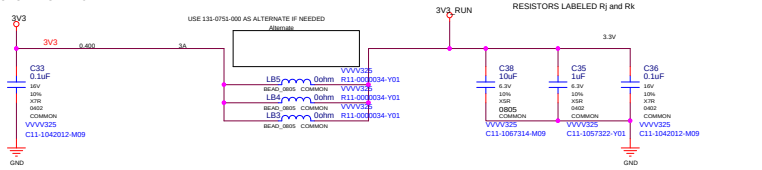
PEX 3V3 INPUT - 10W

DEFAULT STUFFING IS THE BEAD.
IN CASE INDUCTOR NEEDS TO BE STUFFED YOU NEED TO MAKE SURE THAT ITS LOWER HEIGHT THAN 2.7MM

3V3_FILTER CONNECTS to 3V3_RUN.

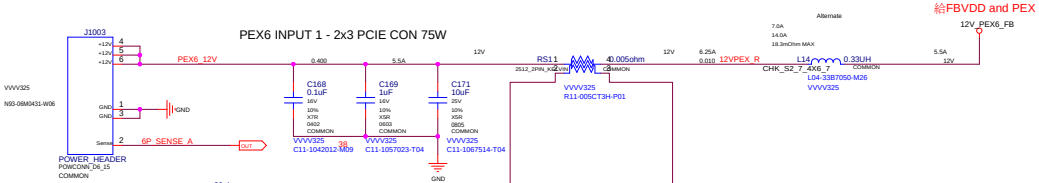
VIA CIRCUITRY FOUND ON THE MCU PAGE.

USING EITHER THE FET LABELED Qx OR RESISTORS LABELED Rj and Rk

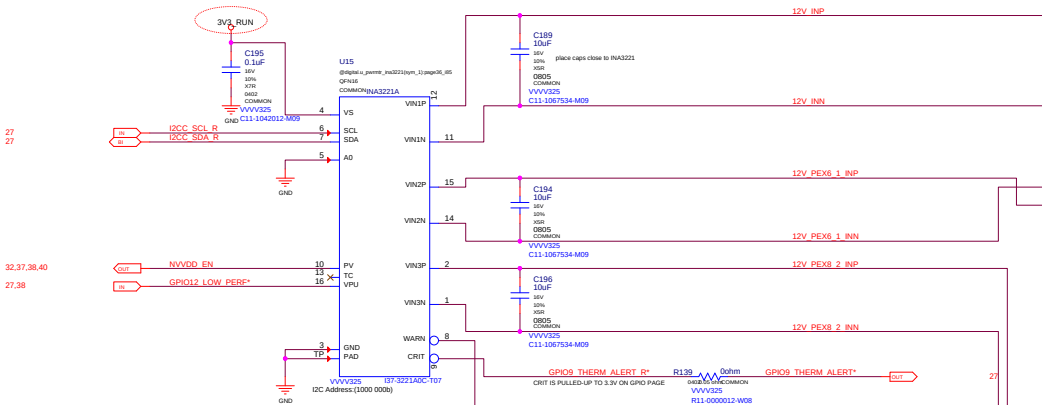


PEX6 INPUT 1 - 2x3 PCIE CON 75W

給FBVDD and PEX

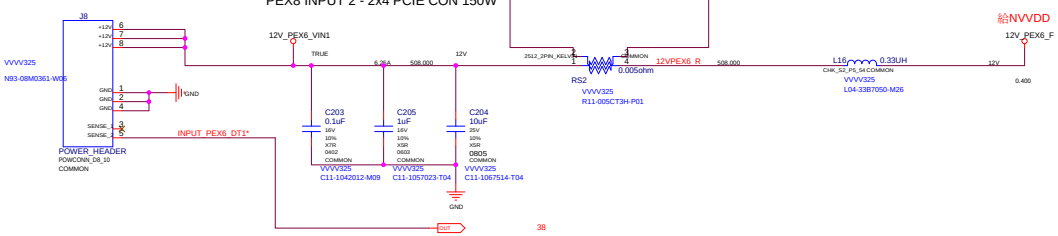


4/30 3V3 change 3V3_RUN



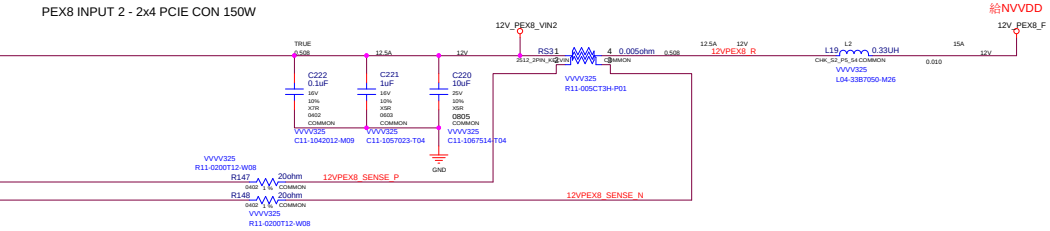
PEX8 INPUT 2 - 2x4 PCIE CON 150W

給NVVDD



PEX8 INPUT 2 - 2x4 PCIE CON 150W

給NVVDD



L1/L2 CO LAYOUT

L1 STUFFED FOR DESKTOP

L2 STUFFED FOR 2x4 EAST CONNECTOR STUFFED

STUFF for CPU 8-PIN Power Connector

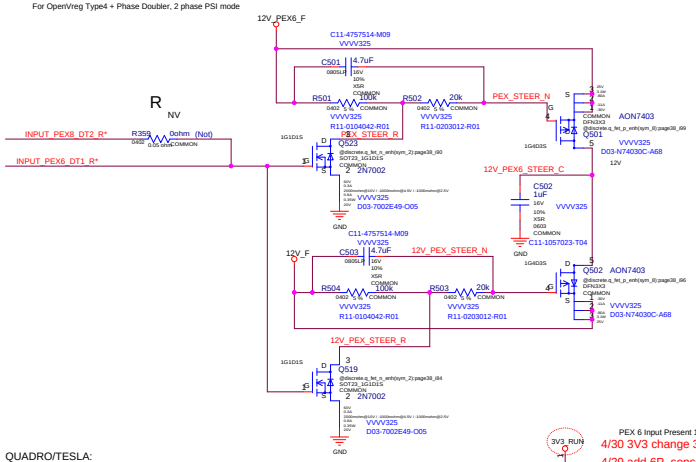
MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 37 of 42

Page38: PS: 12V Current Steering & Hot Unplug Detect

12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



QUADRO/TESLA:

PEX 6 INPUT CONNECTOR IS NOT LOADED

PEX 6 INPUT DETECT MUST BE DISABLED

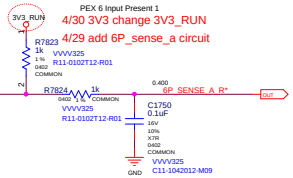
PEX 8 INPUT DETECT MUST BE USED TO CONTROL STEERING

STUFF Rnv IN STEERING CIRCUIT

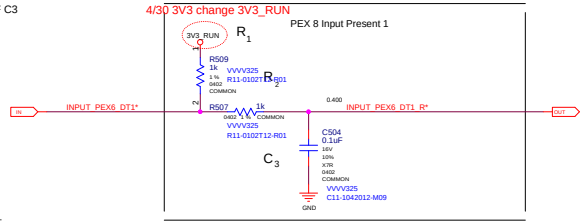
NO STUFF R1

NO STUFF R2

NO STUFF C3



4/30 3V3 change 3V3_RUN



GeFORCE:

PEX 6 INPUT CONNECTOR IS LOADED

PEX 6 INPUT DETECT MUST BE USED TO CONTROL STEERING

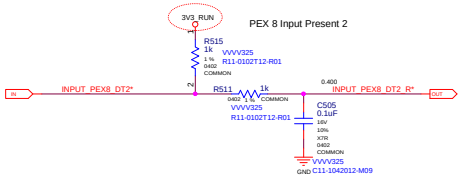
NO STUFF Rnv IN STEERING CIRCUIT

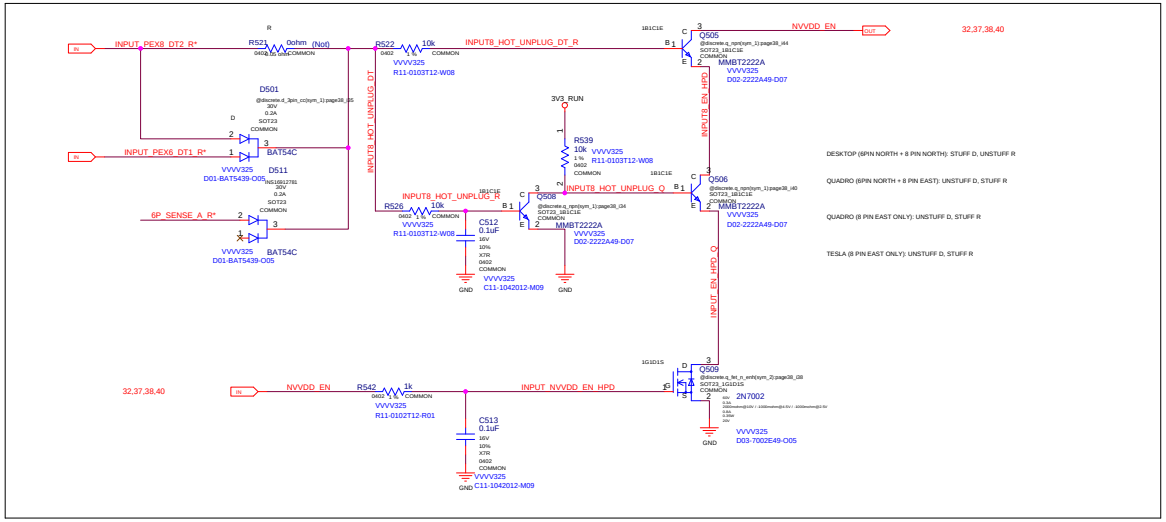
STUFF R1

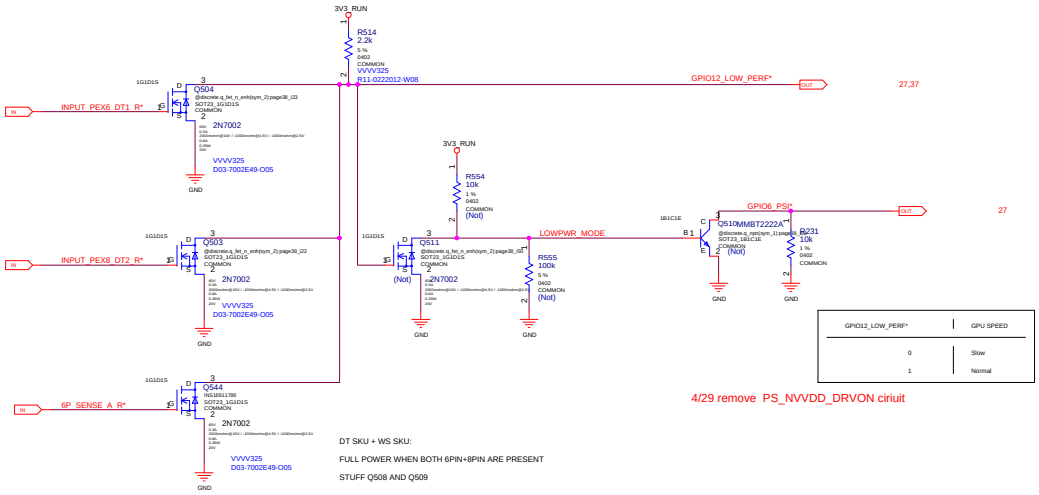
STUFF R2

STUFF C3

4/30 3V3 change 3V3_RUN

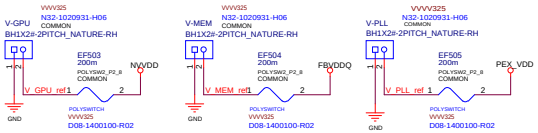


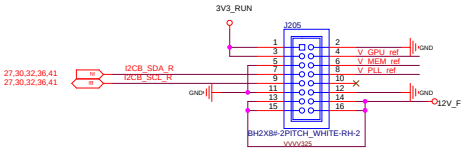




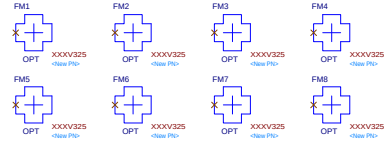
MICRO-STAR INT'L CO.,LTD	
MS-V325	
Size: Custom	Document Description: TABLE OF CONTENTS
Rev: 1.0	
Date: Thursday, May 21, 2015	Sheet 38 of 42

Page39: Mechanical: Bracket/Thermal Solution

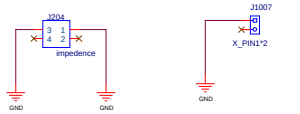


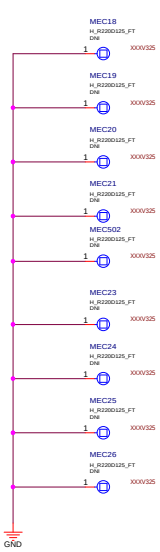


optical cross point



Top & bottom each layer set 4 points

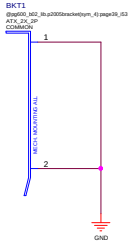




Mechanical Holes Symbol

Brackets:

DVIDVI_HDMI_DP : 151-10001-0441-092



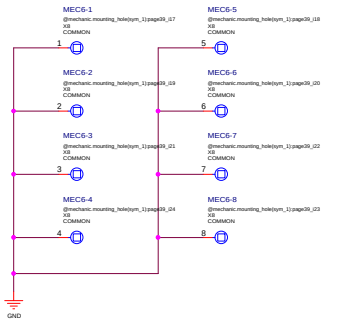
Bracket Screw

Stiffener

GPU SOCKET

GPU Stiffener (BRING-UP COOLER)

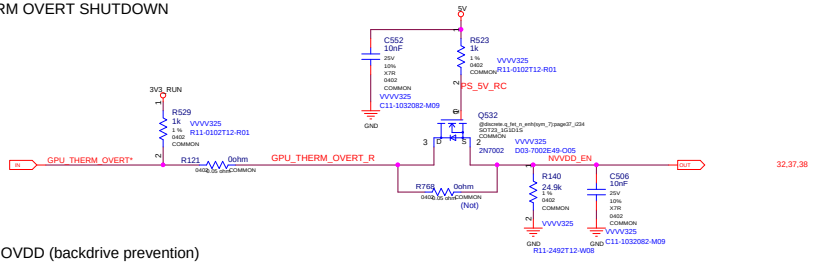
Bring Up Cooler



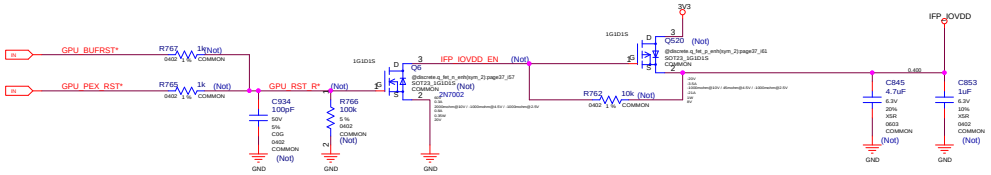
MICRO-STAR INT'L CO.,LTD		
MS-V325		
Size: Custom	Document Description: TABLE OF CONTENTS	Rev: 1.0
Date: Thursday, May 21, 2015	Sheet 39 of 42	

Page40: PS: Shutdown & IFP_IOVDD & INPUT POWER CONNECTOR DETECTION

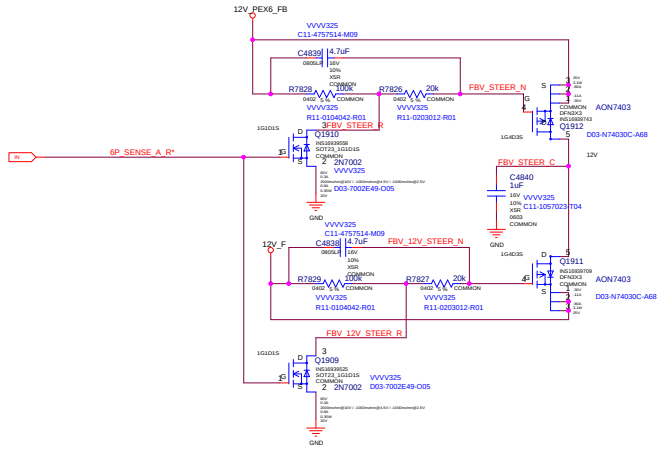
THERM OVERT SHUTDOWN



IFP_IOVDD (backdrive prevention)



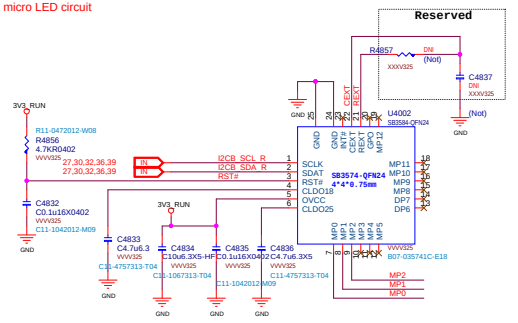
4/29 add FB 12 current steering circuit

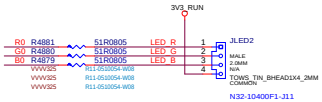


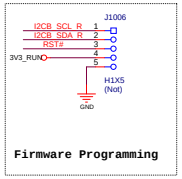
MICRO-STAR INT'L CO.,LTD		
MS-V325		
Size: Custom	Document Description: TABLE OF CONTENTS	Rev: 1.0
Date: Thursday, May 21, 2015	Sheet 40 of 42	

Page41: POWER BRAKE, GEFORCE LED AND SLI LED

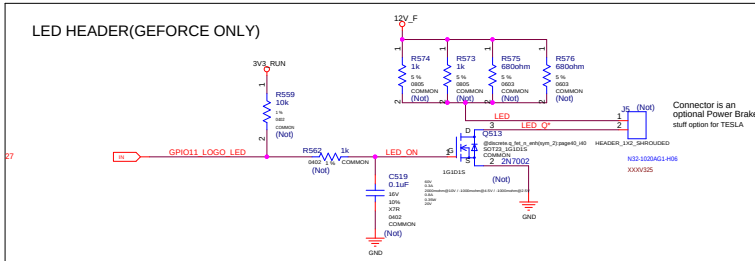
4/29 add ENE micro LED circuit



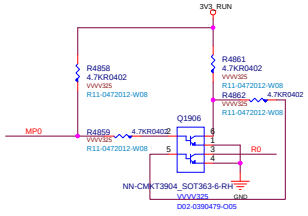




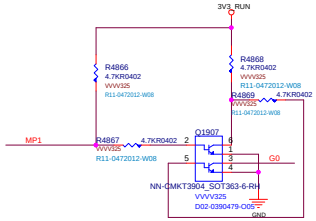
LED HEADER(GEFORCE ONLY)



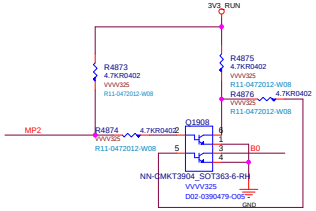
LED(R)



LED(G)



LED(B)



USING GPIO5 TO DIM GEFORCE AND SLI LED

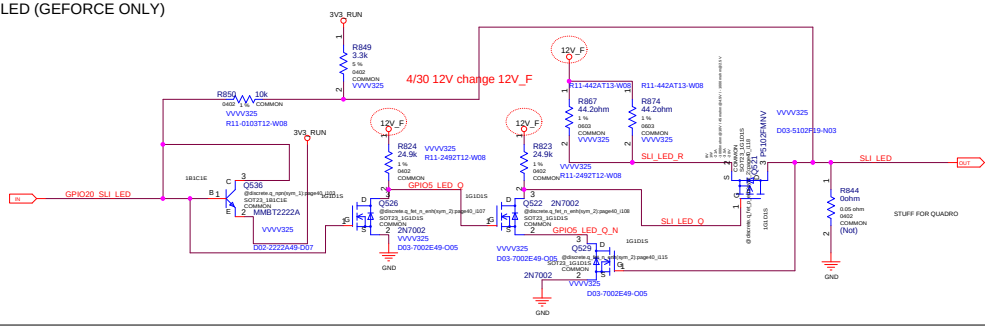
LED FOR QUADRO

PLACE BETWEEN DP Connectors

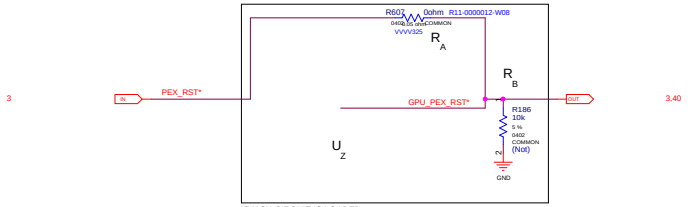
CONNECTORS

4/289 remove

SLI LED (GEFORCE ONLY)



Page42: MCU

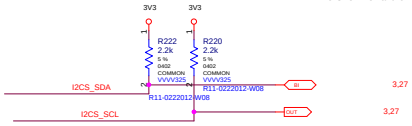


IF MCU CIRCUIT IS LOADED

STUFF Uz and Cz and RB. NO STUFF RA.

IF MCU CIRCUIT IS UNLOADED

NO STUFF Uz and Cz and RB. STUFF RA.



IF MCU CIRCUIT IS LOADED

STUFF Qx and NO STUFF Rj and Rk

IF MCU CIRCUIT IS UNLOADED

NO STUFF Qx and STUFF Rj and Rk

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Size: Custom	Document Description: TABLE OF CONTENTS	Rev: 1.0
Date: Thursday, May 21, 2015	Sheet 42 of 42	