

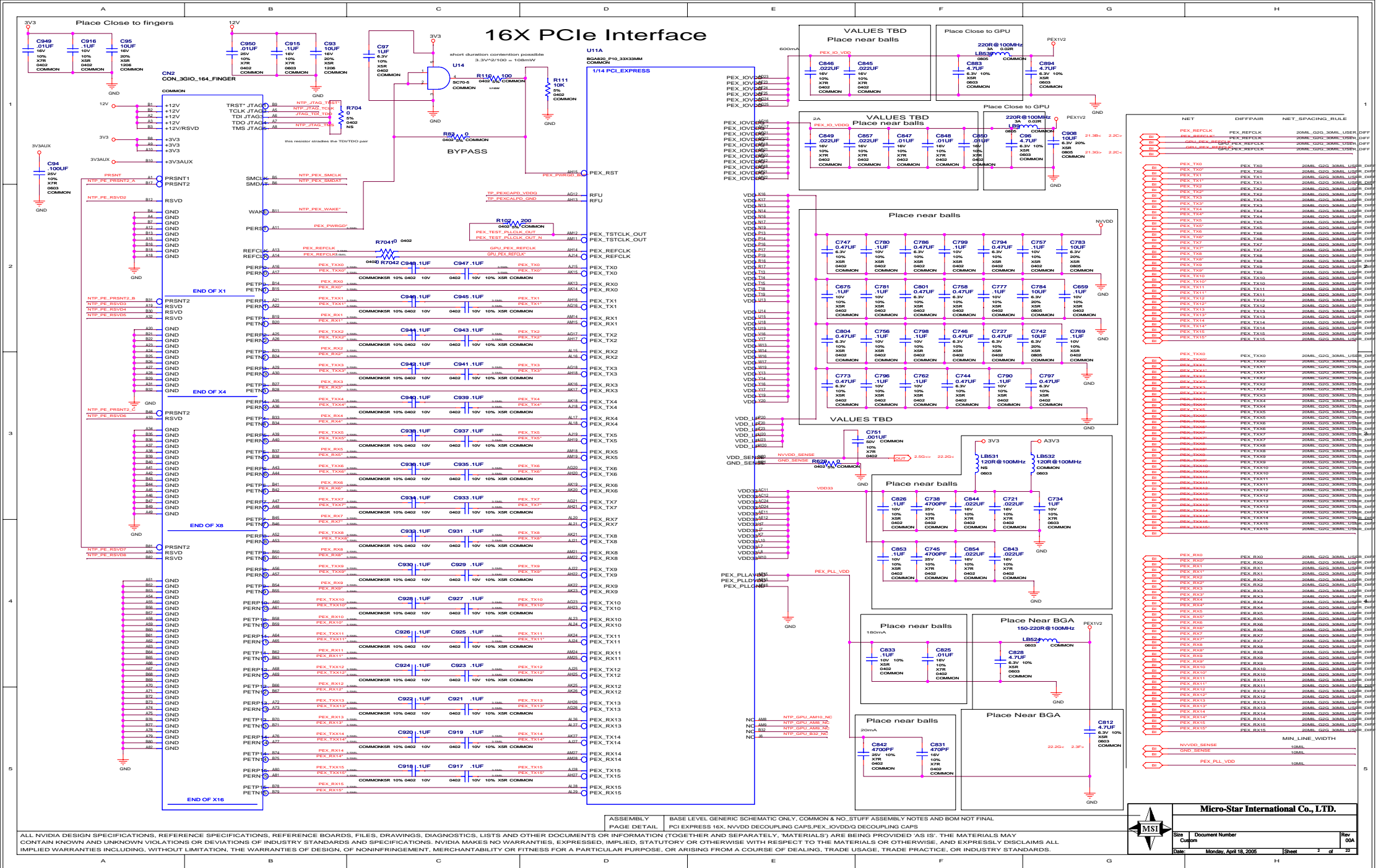
P216-A02 DESIGN -- NV43, 128 MB DDR3, VGA, DVI-I, SD/HDTV, VIVO

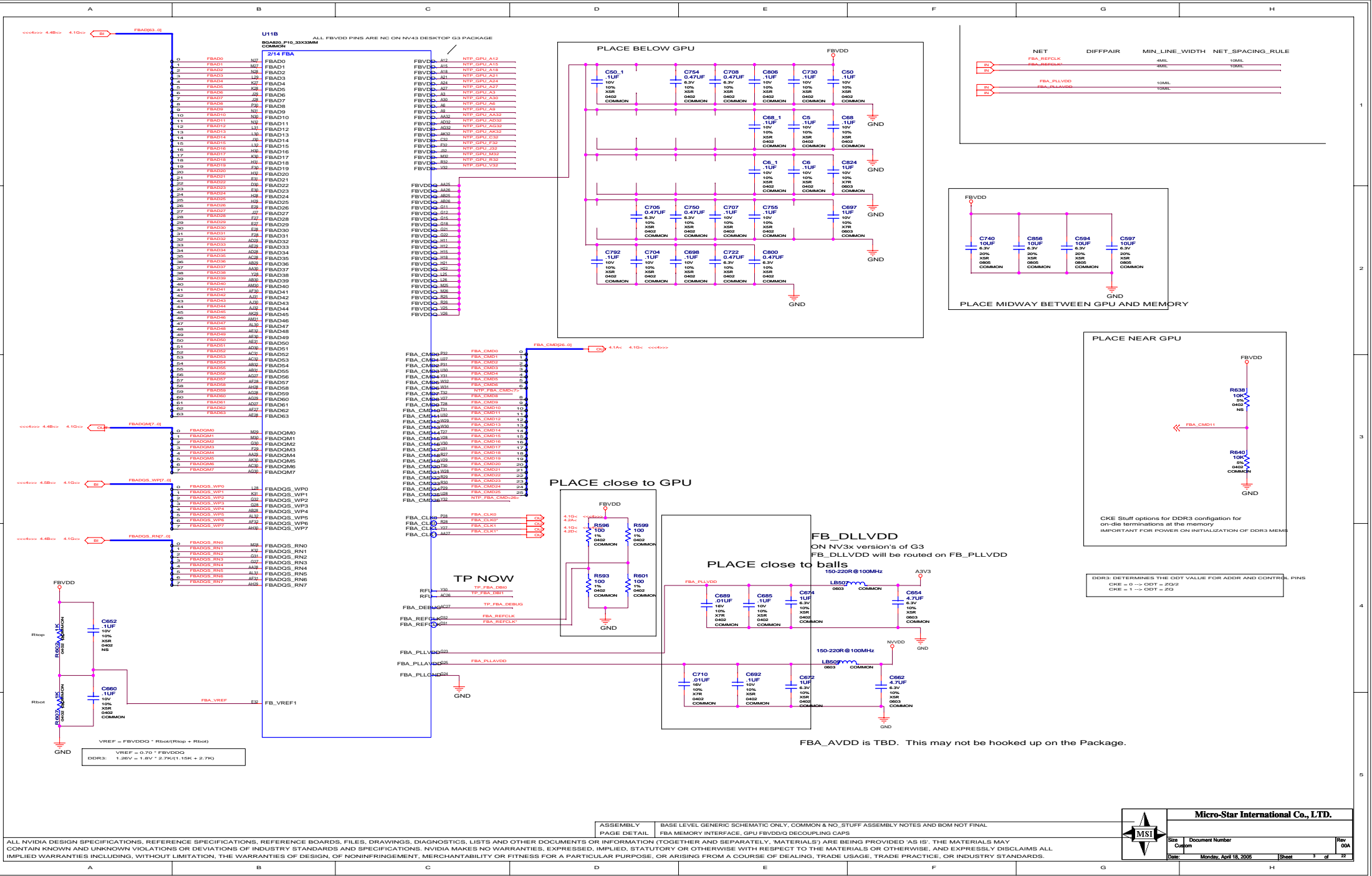
PAGE SUMMARY:

20050203 Verson 10

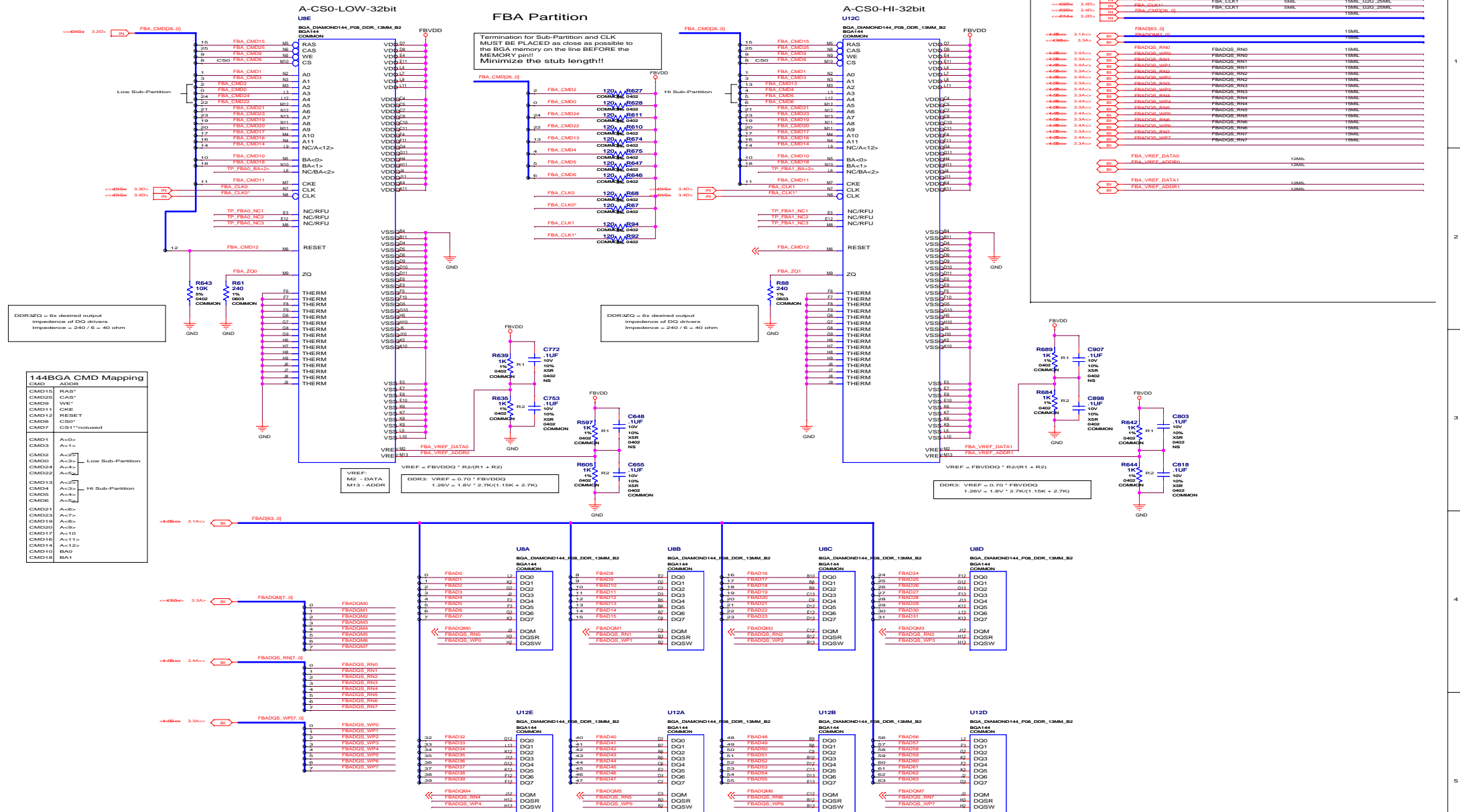
- Adding BJT into 1155 VID4 to solve always pull low issue.
- ATS2G GPIO contorller reset pin set to 3v3.
- Adding OVT &SMI# Func. with F75387
- Remove FAN JU1(12V only)
- Solve Cap dummy issue with 3 pin
- Adding EMI Fucn. into south DVI
- Change GPIO to GPU & Memory -2005-0214

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	602-10216-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	000	602-10216-0000-200	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HDTVOUT
2	001	602-10216-0001-200	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HDTVIVO
3	002	602-10216-0002-200	NV43-U 350/350MHZ 128MB DDR3 8MX32 DVI+VGA+HDTVOUT
4	003	602-10216-0003-200	NV43-U 400/400MHZ 128MB DDR3 8MX32 DVI+VGA+HDTVOUT
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>



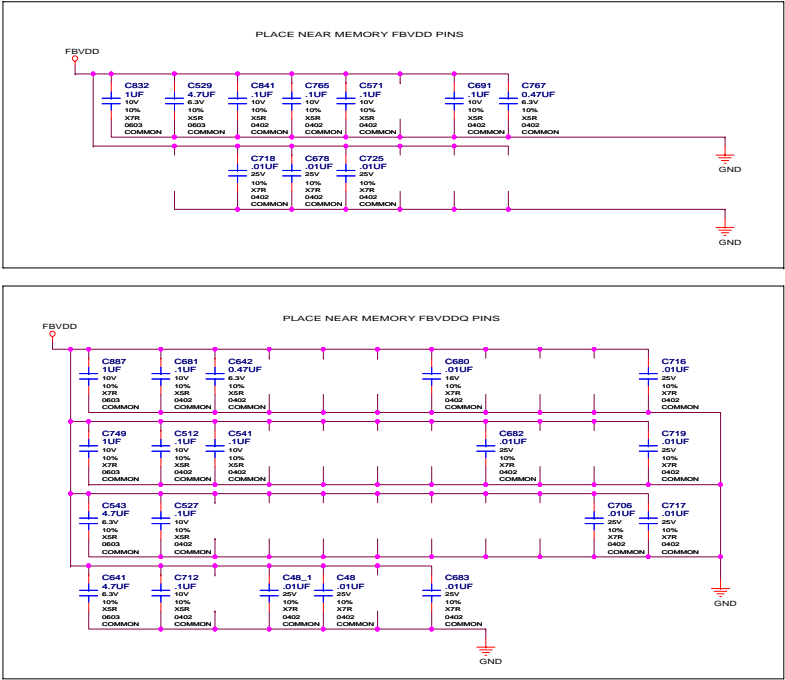


5 FrameBuffer: Partition A 8Mx32 BGA144 DDR3

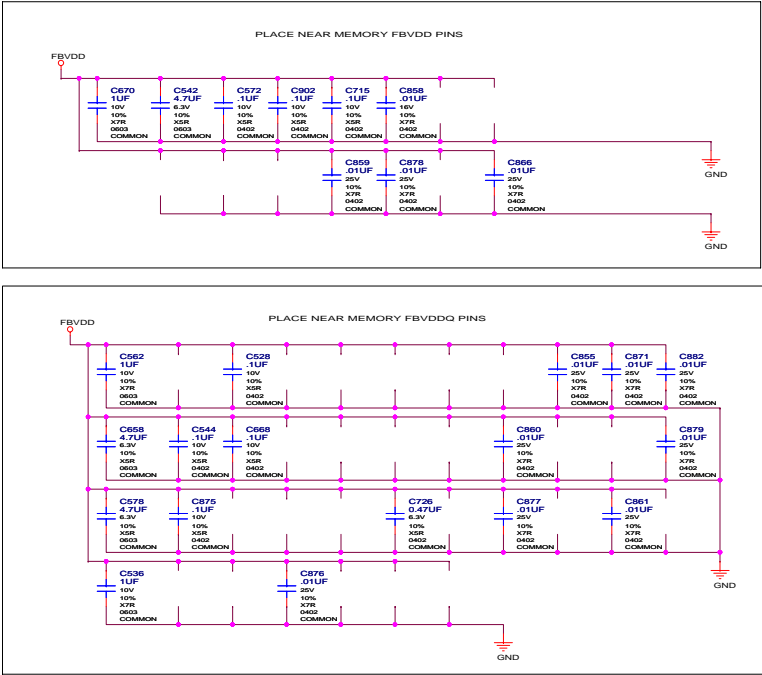


FRAME BUFFER: PARTITION A DECOUPLING

Decoupling for FBA 0..31



Decoupling for FBA 32..63



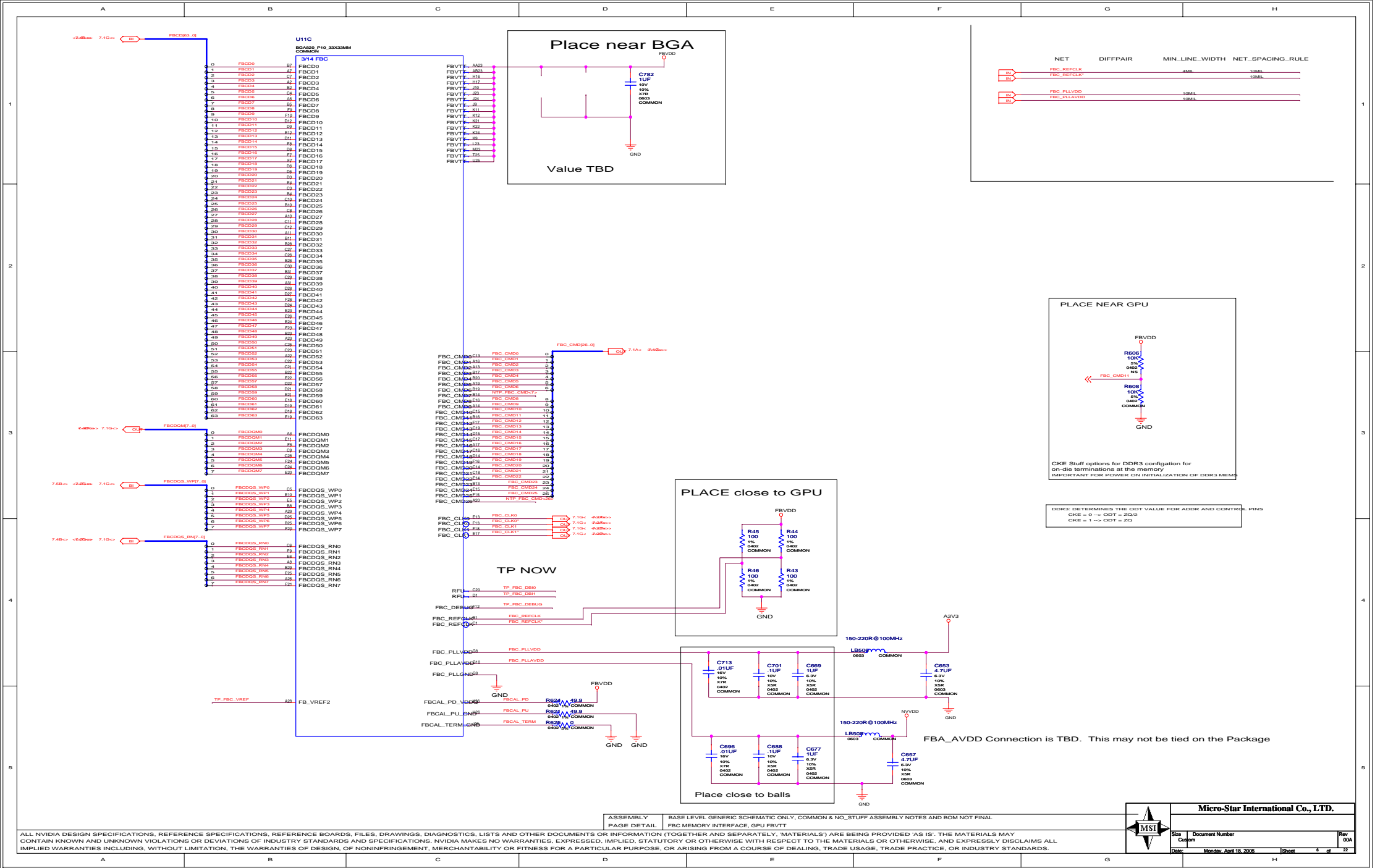
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ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
FBA MEMORY FBVDD0 DECOUPLING CAPS



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Docu Document Number Rev 00A
Date: Monday, April 18, 2005 Sheet 5 of 22



FRAMEBUFFER: PARTITION C 8Mx32 BGA144 DDR3

A-CS0-LOW-32bit

USE

BGA_DIAMOND144_P08_DDR_13MM_B2

BGA144 COMMON

FBVDD

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FBC Partition

Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to the BGA memory on the line BEFORE the MEMORY pin!!
Minimize the stub length!!

A-CS0-HI-32bit

USE

BGA_DIAMOND144_P08_DDR_13MM_B2

BGA144 COMMON

FBVDD

FBVDD

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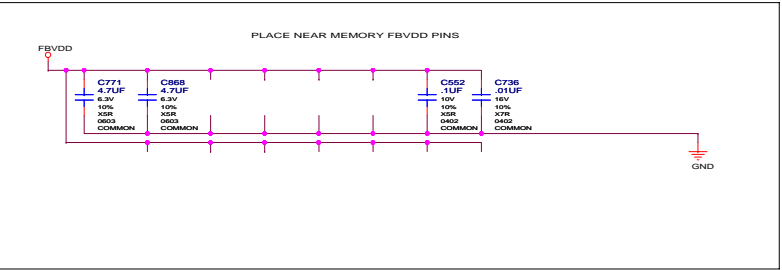
FBVDD

NET DIFFPAIR MIN_LINE_WIDTH SPACING

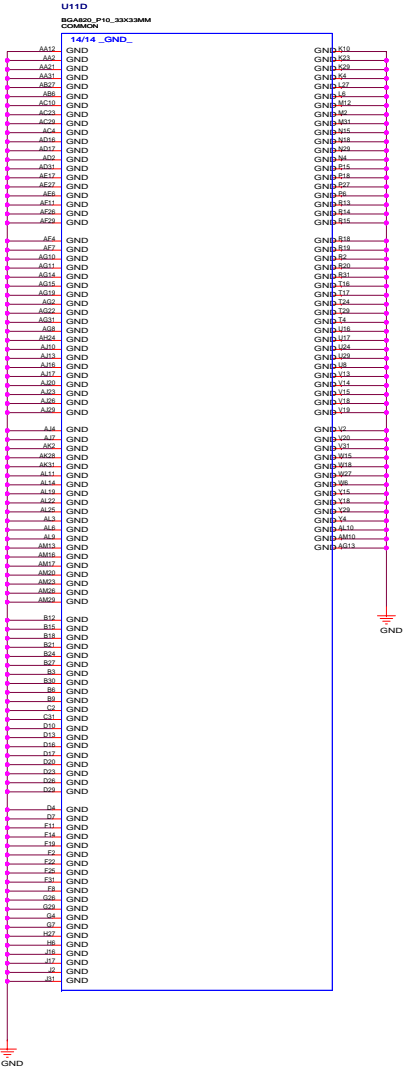
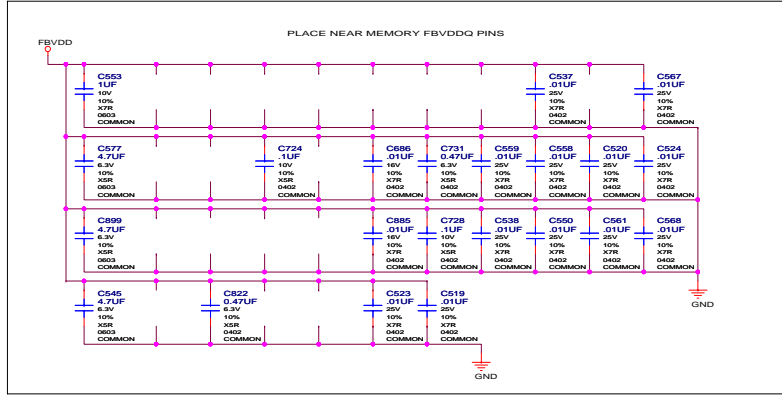
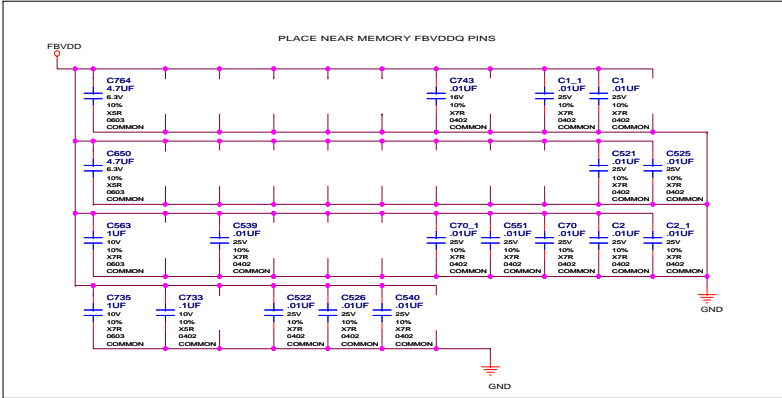
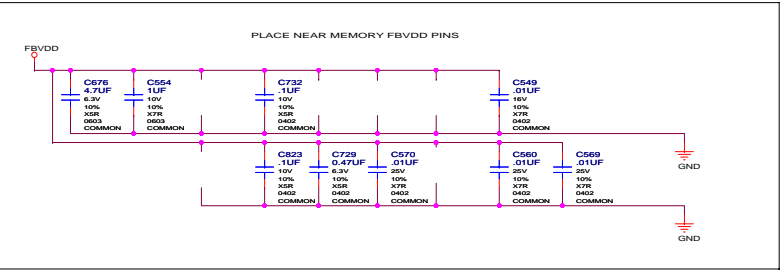
NET	DIFFPAIR	MIN_LINE_WIDTH	SPACING
FBC_CMD0	FBC_CMD0	5MIL	15MIL G20_25MIL
FBC_CMD1	FBC_CMD1	5MIL	15MIL G20_25MIL
FBC_CMD2	FBC_CMD2	5MIL	15MIL G20_25MIL
FBC_CMD3	FBC_CMD3	5MIL	15MIL G20_25MIL
FBC_CMD4	FBC_CMD4	5MIL	15MIL G20_25MIL
FBC_CMD5	FBC_CMD5	5MIL	15MIL G20_25MIL
FBC_CMD6	FBC_CMD6	5MIL	15MIL G20_25MIL
FBC_CMD7	FBC_CMD7	5MIL	15MIL G20_25MIL
FBC_CMD8	FBC_CMD8	5MIL	15MIL G20_25MIL
FBC_CMD9	FBC_CMD9	5MIL	15MIL G20_25MIL
FBC_CMD10	FBC_CMD10	5MIL	15MIL G20_25MIL
FBC_CMD11	FBC_CMD11	5MIL	15MIL G20_25MIL
FBC_CMD12	FBC_CMD12	5MIL	15MIL G20_25MIL
FBC_CMD13	FBC_CMD13	5MIL	15MIL G20_25MIL
FBC_CMD14	FBC_CMD14	5MIL	15MIL G20_25MIL
FBC_CMD15	FBC_CMD15	5MIL	15MIL G20_25MIL
FBC_CMD16	FBC_CMD16	5MIL	15MIL G20_25MIL
FBC_CMD17	FBC_CMD17	5MIL	15MIL G20_25MIL
FBC_CMD18	FBC_CMD18	5MIL	15MIL G20_25MIL
FBC_CMD19	FBC_CMD19	5MIL	15MIL G20_25MIL
FBC_CMD20	FBC_CMD20	5MIL	15MIL G20_25MIL
FBC_CMD21	FBC_CMD21	5MIL	15MIL G20_25MIL
FBC_CMD22	FBC_CMD22	5MIL	15MIL G20_25MIL
FBC_CMD23	FBC_CMD23	5MIL	15MIL G20_25MIL
FBC_CMD24	FBC_CMD24	5MIL	15MIL G20_25MIL
FBC_CMD25	FBC_CMD25	5MIL	15MIL G20_25MIL
FBC_CMD26	FBC_CMD26	5MIL	15MIL G20_25MIL
FBC_CMD27	FBC_CMD27	5MIL	15MIL G20_25MIL
FBC_CMD28	FBC_CMD28	5MIL	15MIL G20_25MIL
FBC_CMD29	FBC_CMD29	5MIL	15MIL G20_25MIL
FBC_CMD30	FBC_CMD30	5MIL	15MIL G20_25MIL
FBC_CMD31	FBC_CMD31	5MIL	15MIL G20_25MIL
FBC_CMD32	FBC_CMD32	5MIL	15MIL G20_25MIL
FBC_CMD33	FBC_CMD33	5MIL	15MIL G20_25MIL
FBC_CMD34	FBC_CMD34	5MIL	15MIL G20_25MIL
FBC_CMD35	FBC_CMD35	5MIL	15MIL G20_25MIL
FBC_CMD36	FBC_CMD36	5MIL	15MIL G20_25MIL
FBC_CMD37	FBC_CMD37	5MIL	15MIL G20_25MIL
FBC_CMD38	FBC_CMD38	5MIL	15MIL G20_25MIL
FBC_CMD39	FBC_CMD39	5MIL	15MIL G20_25MIL
FBC_CMD40	FBC_CMD40	5MIL	15MIL G20_25MIL
FBC_CMD41	FBC_CMD41	5MIL	15MIL G20_25MIL
FBC_CMD42	FBC_CMD42	5MIL	15MIL G20_25MIL
FBC_CMD43	FBC_CMD43	5MIL	15MIL G20_25MIL
FBC_CMD44	FBC_CMD44	5MIL	15MIL G20_25MIL
FBC_CMD45	FBC_CMD45	5MIL	15MIL G20_25MIL
FBC_CMD46	FBC_CMD46	5MIL	15MIL G20_25MIL
FBC_CMD47	FBC_CMD47	5MIL	15MIL G20_25MIL
FBC_CMD48	FBC_CMD48	5MIL	15MIL G20_25MIL
FBC_CMD49	FBC_CMD49	5MIL	15MIL G20_25MIL
FBC_CMD50	FBC_CMD50	5MIL	15MIL G20_25MIL
FBC_CMD51	FBC_CMD51	5MIL	15MIL G20_25MIL
FBC_CMD52	FBC_CMD52	5MIL	15MIL G20_25MIL
FBC_CMD53	FBC_CMD53	5MIL	15MIL G20_25MIL
FBC_CMD54	FBC_CMD54	5MIL	15MIL G20_25MIL
FBC_CMD55	FBC_CMD55	5MIL	15MIL G20_25MIL
FBC_CMD56	FBC_CMD56	5MIL	15MIL G20_25MIL
FBC_CMD57	FBC_CMD57	5MIL	15MIL G20_25MIL
FBC_CMD58	FBC_CMD58	5MIL	15MIL G20_25MIL
FBC_CMD59	FBC_CMD59	5MIL	15MIL G20_25MIL
FBC_CMD60	FBC_CMD60	5MIL	15MIL G20_25MIL
FBC_CMD61	FBC_CMD61	5MIL	15MIL G20_25MIL
FBC_CMD62	FBC_CMD62	5MIL	15MIL G20_25MIL
FBC_CMD63	FBC_CMD63	5MIL	15MIL G20_25MIL
FBC_CMD64	FBC_CMD64	5MIL	15MIL G20_25MIL
FBC_CMD65	FBC_CMD65	5MIL	15MIL G20_25MIL
FBC_CMD66	FBC_CMD66	5MIL	15MIL G20_25MIL
FBC_CMD67	FBC_CMD67	5MIL	15MIL G20_25MIL
FBC_CMD68	FBC_CMD68	5MIL	15MIL G20_25MIL
FBC_CMD69	FBC_CMD69	5MIL	15MIL G20_25MIL
FBC_CMD70	FBC_CMD70	5MIL	15MIL G20_25MIL
FBC_CMD71	FBC_CMD71	5MIL	15MIL G20_25MIL
FBC_CMD72	FBC_CMD72	5MIL	15MIL G20_25MIL
FBC_CMD73	FBC_CMD73	5MIL	15MIL G20_25MIL
FBC_CMD74	FBC_CMD74	5MIL	15MIL G20_25MIL
FBC_CMD75	FBC_CMD75	5MIL	15MIL G20_25MIL
FBC_CMD76	FBC_CMD76	5MIL	15MIL G20_25MIL
FBC_CMD77	FBC_CMD77	5MIL	15MIL G20_25MIL
FBC_CMD78	FBC_CMD78	5MIL	15MIL G20_25MIL
FBC_CMD79	FBC_CMD79	5MIL	15MIL G20_25MIL
FBC_CMD80	FBC_CMD80	5MIL	15MIL G20_25MIL
FBC_CMD81	FBC_CMD81	5MIL	15MIL G20_25MIL
FBC_CMD82	FBC_CMD82	5MIL	15MIL G20_25MIL
FBC_CMD83	FBC_CMD83	5MIL	15MIL G20_25MIL
FBC_CMD84	FBC_CMD84	5MIL	15MIL G20_25MIL
FBC_CMD85	FBC_CMD85	5MIL	15MIL G20_25MIL
FBC_CMD86	FBC_CMD86	5MIL	15MIL G20_25MIL
FBC_CMD87	FBC_CMD87	5MIL	15MIL G20_25MIL
FBC_CMD88	FBC_CMD88	5MIL	15MIL G20_25MIL
FBC_CMD89	FBC_CMD89	5MIL	15MIL G20_25MIL
FBC_CMD90	FBC_CMD90	5MIL	15MIL G20_25MIL
FBC_CMD91	FBC_CMD91	5MIL	15MIL

FRAMEBUFFER: PARTITION C DECOUPLING

Decoupling for FBC 0..31



Decoupling for FBC 32..63



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11

DACA RGB-FILTER



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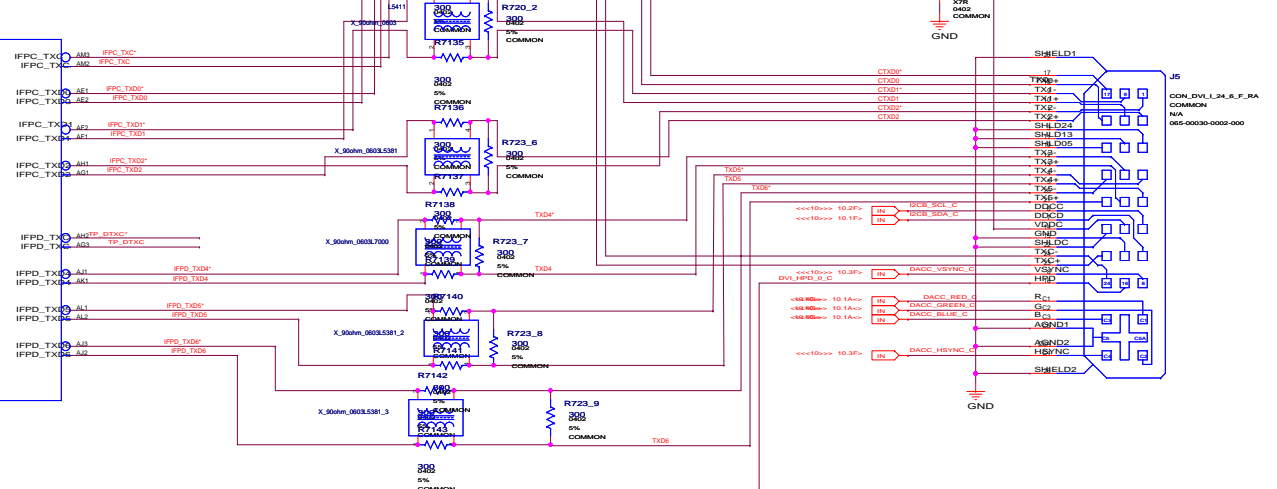
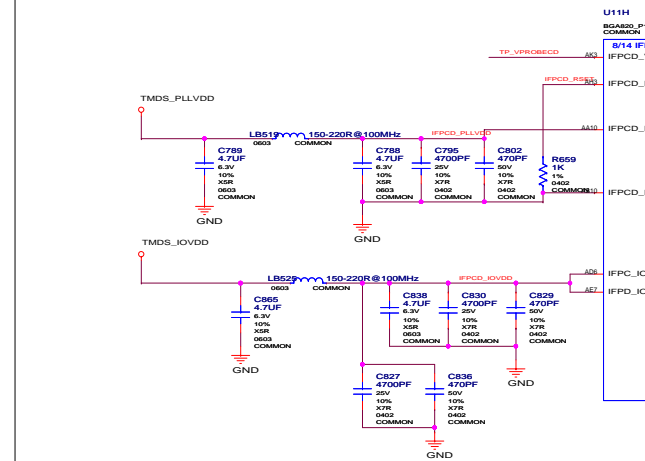
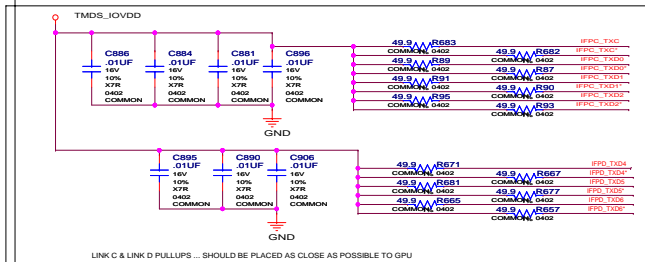
1

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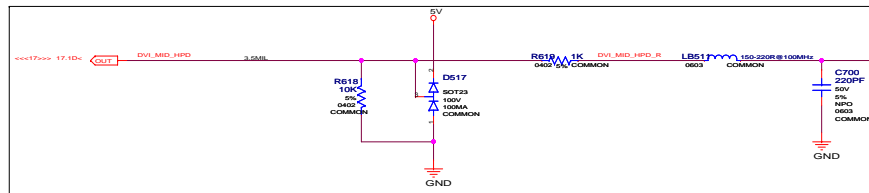


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INTERNAL TMDS .. LINK C & D



Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
IFPCD_RSET	12MIL	3.3V
IFPCD_PLVDD	12MIL	3.3V
IFPCD_I0VDD	12MIL	3.3V

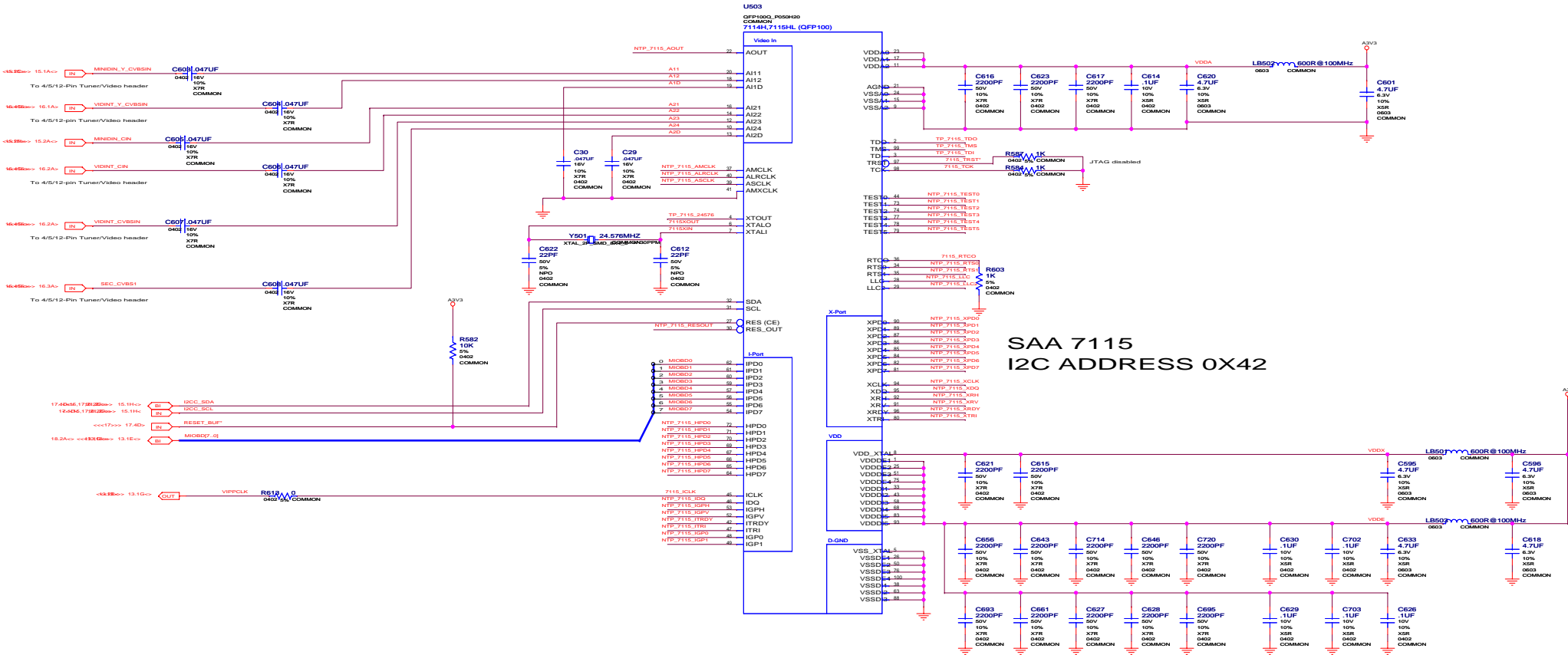
ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL TMDS LINK C/D & P_U+D_VI CONNECTOR MID

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Small			
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PHILIPS VIDEO CAPTURE

NETNAME	MIN_LINE_WIDTH
VDDA	12MIL
VDDX	12MIL
VDDI	12MIL



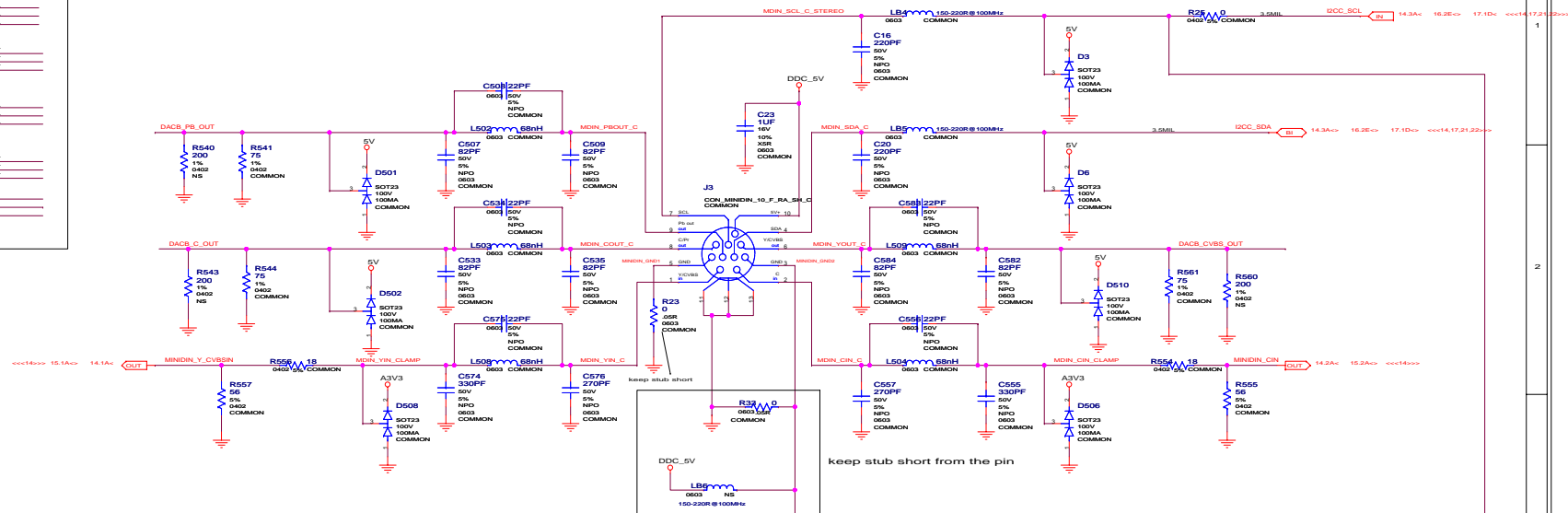
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DACB .. MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES

[illegible]

FILTER NOTES:
SD: USE L=1.8UH
HD: USE L=?

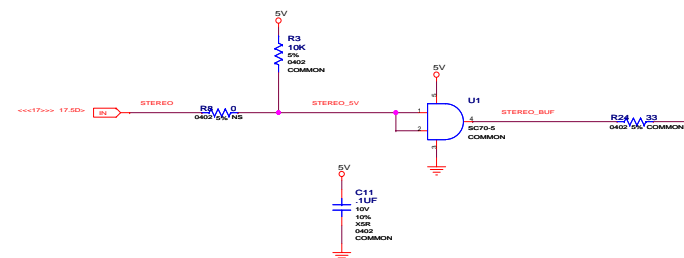


PLACE NEAR CONNECTOR

For STEREO GLASSES 3pin MiniDIN only:
Stuff bead!
And replace 0 Ohm resistor with 220PF cap!

STEREO GLASSES BUFFER

Place close to MiniDIN connector!



FOR DEBUG PURPOSES ONLY .. DEFAULT IS NO STUFF

ASSEMBLY PAGE DETAIL	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL DACB FILTERS. MINIDIN CONNECTOR NORTH
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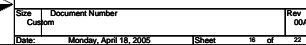
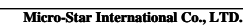
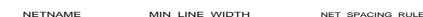
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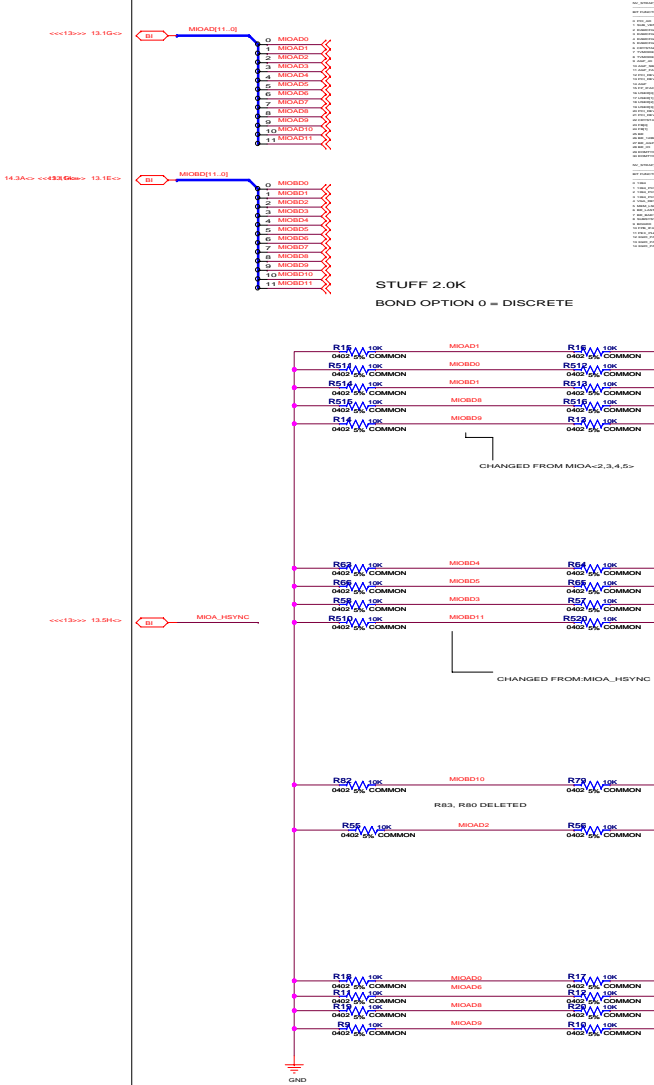
EXTERNAL 4-PIN VIDEO IN CONNECTOR



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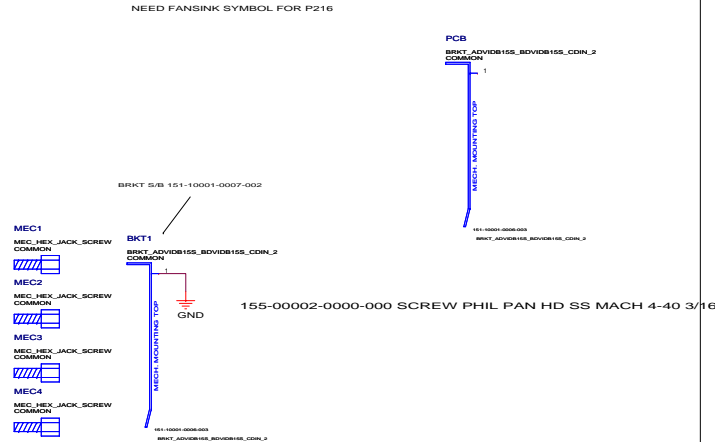
BIOS, Straps, Misc

Straps



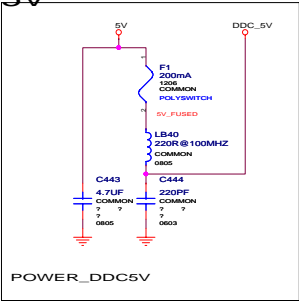
REG: NV_PEXTDEV_BOOT_0		
Bit Signal	VALUE_ID	VALUES
00: PCI_AD_SWAP[PCI_AD_SWAP]	0 REVERSED	
01: SUB_VENDOR SUB_VENDOR	0 NO_BIOS	
02: RAM_CFG_0 RAM_CFG[3:0]	1 Read from BIOS	
03: RAM_CFG_1	0000 REFU	1000 REFU
04: RAM_CFG_2	0010 REFU	1010 REFU
05: RAM_CFG_3	0100 REFU	1100 REFU
06: CRYSTAL_0 CRYSTAL[1:0]	00 13.500 Mhz	01 14.31818 Mhz
22: CRYSTAL_1	10 27.000 Mhz	11 unknown
07: TV_MODE_0 TV_MODE[1:0]	00 SECAM	01 INTSC
08: TV_MODE_1	10 PAL	11 CRT
09: AGP_ENABLE AGP_30_8x	0 AGP8x enabled	1 AGP8x disabled
10: AGP_SBA AGP_SBA[0]	0 SBA enabled	1 SBA disabled
11: AGP_FASTWR AGP_FASTWR[0]	0 enabled	1 disabled
12: PCI_DEVID_0 PCI_DEVID[3:0]	0000 (default 0x140) ... 1111 0x014F	
13: PCI_DEVID_1	0000 (default 0x140)	0101 (0x145)
20: PCI_DEVID_2		
21: PCI_DEVID_3		
14: BUS_TYPE BUS_TYPE[0]	0 PCI	1 AGP
15: FP_IFACE FP_IFACE[0]	0 248B	1 288B (DEFAULT)
23: FB_0 FB[1:0]	00 64M	01 128M
24: FB_1	10 256M (DEFAULT)	11 512M
25: BR BR[0]	0 BRIDGE disabled	1 BRIDGE enabled
26: BR_128M	BR bits are ignored if BRIDGE is disabled	
27: BR_AGP		
28: BR_IO		
29: ROM_TYPE_0 ROM_TYPE[1:0]	00 Parallel	01 Serial_AT32F
30: ROM_TYPE_1	10 Serial_SST45VF	11 REFU
16: USER_0 STRAP_USER[3:0] 0000 (default)		
17: USER_1		
18: USER_2		
19: USER_3		
REG: NV_STRAP_1		
Bit Signal	VALUE_ID	VALUES
11: PEX_PLL_EN_TERM100	0 (default -- internal term on)	
12: 3GIO_PADCFG_LUT_ADR[0]		
13: 3GIO_PADCFG_LUT_ADR[1]		
14: 3GIO_PADCFG_LUT_ADR[2]		

Mechanical parts

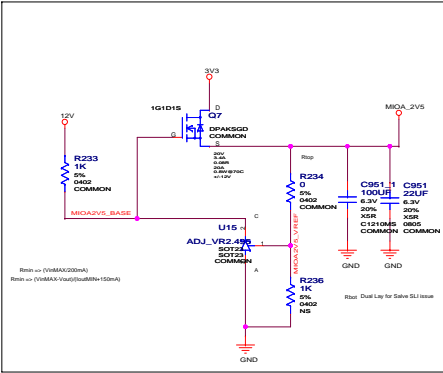


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Power Supply ...
/A3V3
DDC
5V



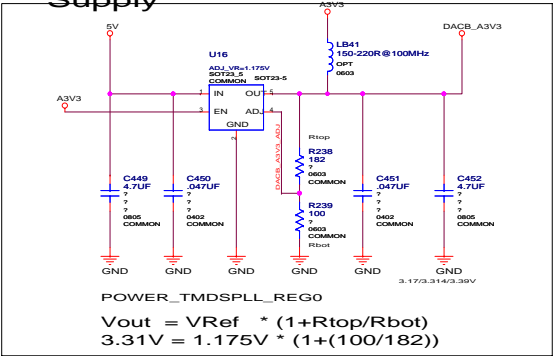
MIOA_VDDQ



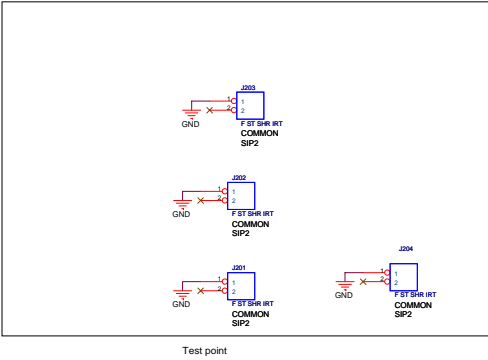
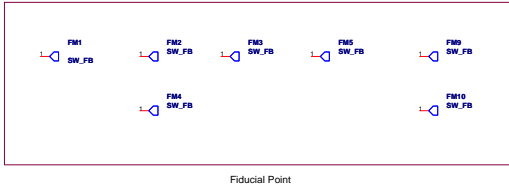
Vref = 2.5V
Vout = 2.495(1+Rtop/Rbot) + (Iref + Rtop)
For Vout = Vref (Rtop = 0ohm, Rbot = NO STUFF)

NETNAME	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	12MIL	5V
3V3	12MIL	3.3V
5V	12MIL	5V
TMDSPLLVDD	12MIL	3.3V
12V	30MIL	12V
MIOA_2V5	12MIL	2.5V
GND	30MIL	0V
DACB_A3V3_ADJ	10MIL	3.3V
DACB_A3V3	12MIL	3.3V


DACB
Supply



Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+(100/182))





	Micro-Star International Co., LTD.		
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VID4	VID3	VID2	VID1	VID0	VID12.5	VDC(V)
1	0	1	1	0	0	1.3125
1	0	0	0	1	1	1.325
1	0	1	0	1	1	1.375
1	0	1	0	0	1	1.35
1	0	1	0	0	0	1.3625
1	0	0	1	1	1	1.375
1	0	0	1	1	0	1.3875
1	0	0	1	0	1	1.4
1	0	0	1	0	1	1.4125
1	0	0	0	1	1	1.425
1	0	0	0	1	0	1.4375
1	0	0	0	0	1	1.45
1	0	0	0	0	1	1.4625
0	1	1	1	1	1	1.475
0	1	1	1	1	0	1.4875
0	1	1	1	1	1	1.5

