P410: G3-128, 128/256MB, 128-bit, 8/16Mx32 DDR2 LVDS,TV_OUT,VGA

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HISTORY:

A01: INITIAL VERSION

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10410-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10410-0001-100	P410-A01 SKU1 G84 256MB DDR2
2	SKU0003	600-10410-0003-100	P410-A01 SKU3 G86 128MB DDR2
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	Overview

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NV_PN	600-10410-0001-100 A		
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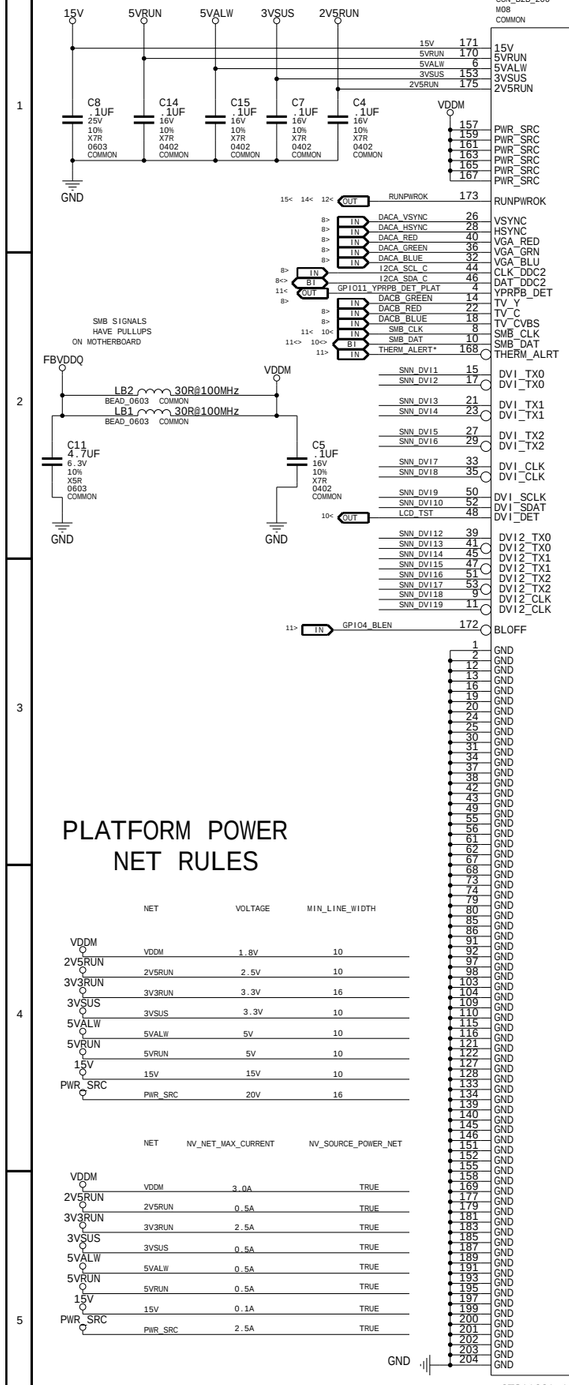
MOTHERBOARD CONNECTOR

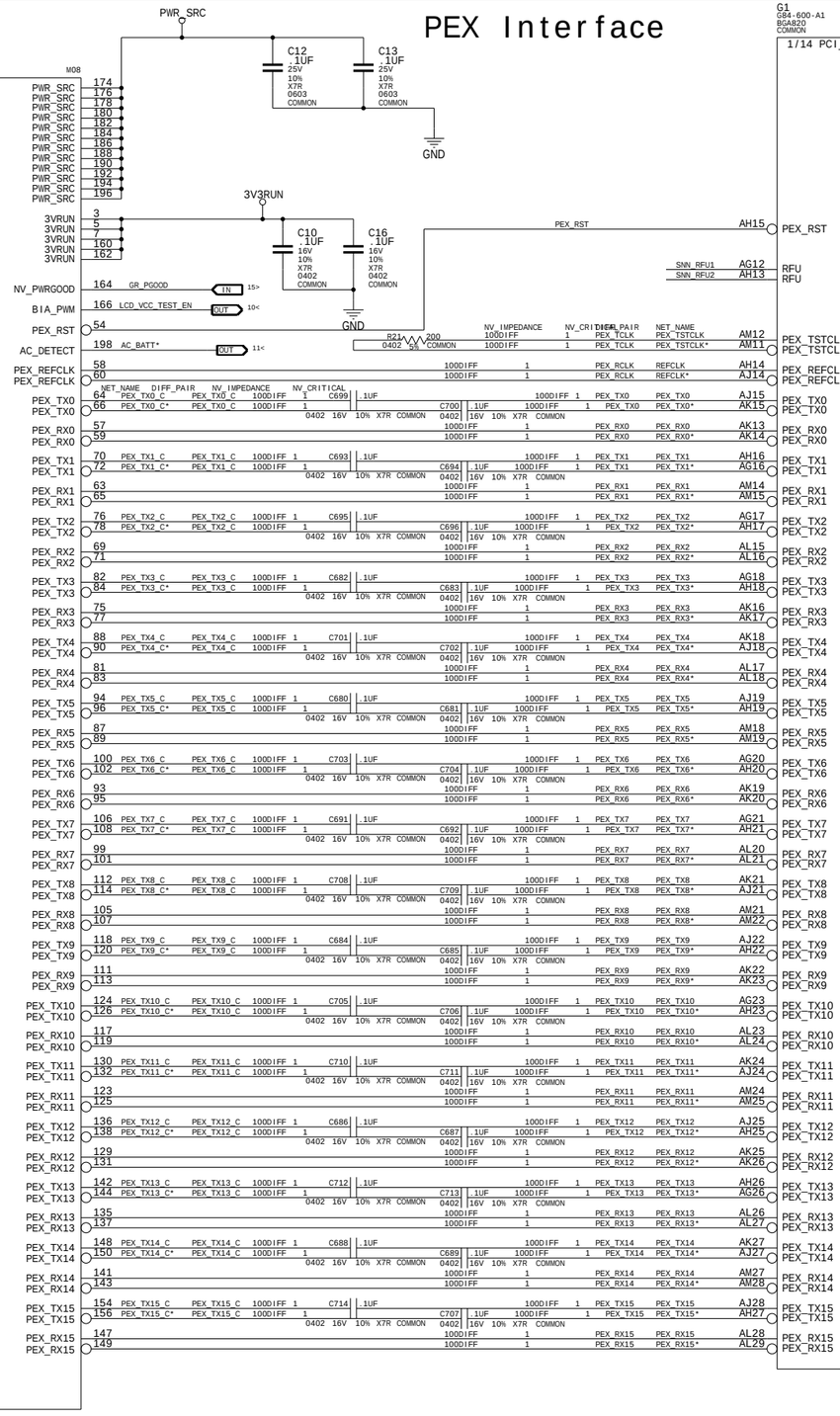


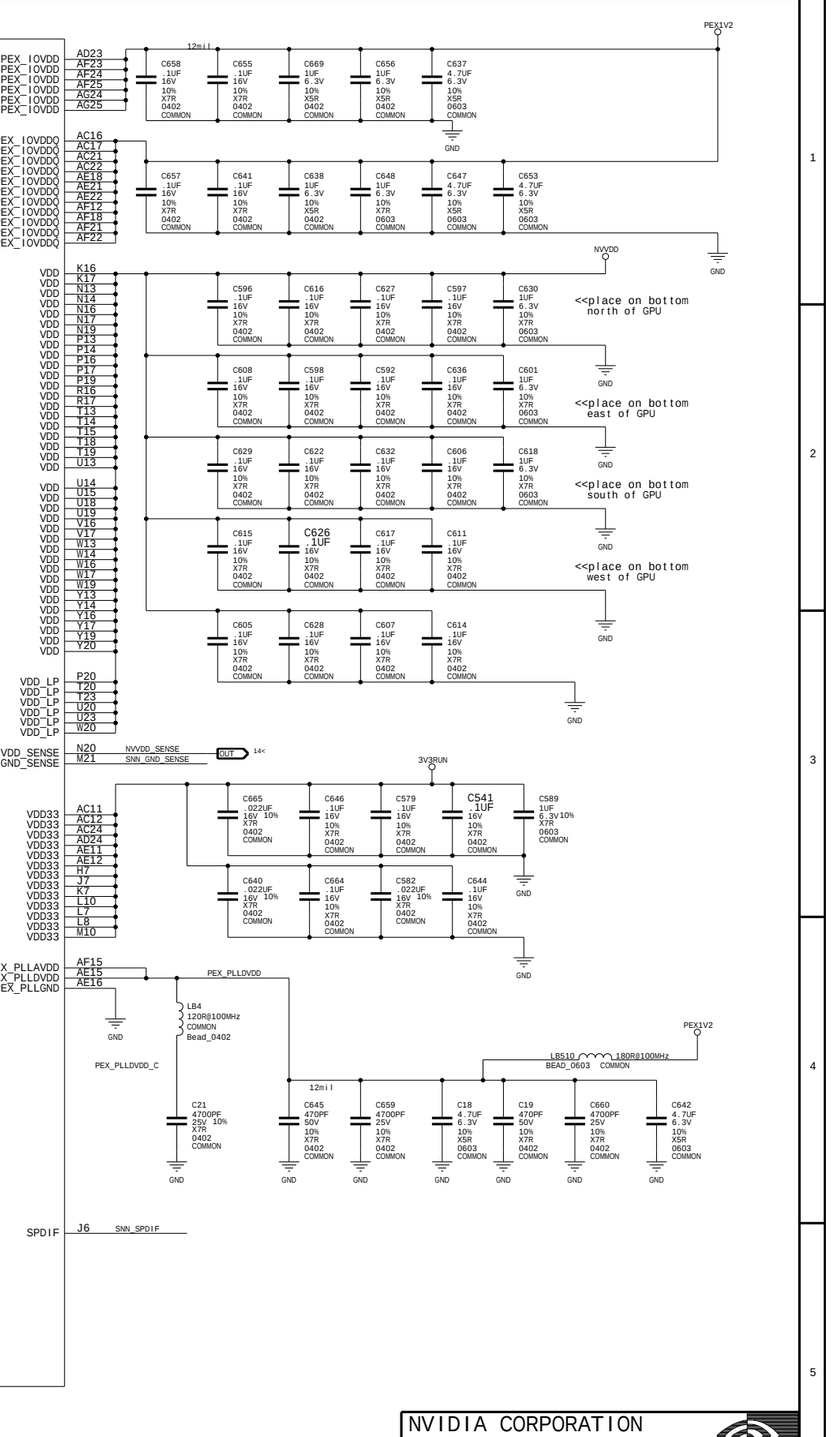
PLATFORM POWER NET RULES

NET	VOLTAGE	MIN_LINE_WIDTH
VDDM	1.8V	10
2V5RUN	2.5V	10
3V3RUN	3.3V	16
3VSUS	3.3V	10
5VALW	5V	10
5VRUN	5V	10
15V	15V	10
PWR_SRC	20V	16

NET	NV_NET_MAX_CURRENT	NV_SOURCE_POWER_NET	
VDDM	3.0A		TRUE
2V5RUN	0.5A		TRUE
3V3RUN	2.5A		TRUE
3VSUS	0.5A		TRUE
5VALW	0.5A		TRUE
5VRUN	0.5A		TRUE
15V	0.1A		TRUE
PWR_SRC	2.5A		TRUE

PEX Interface





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ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	PCI EXPRESS Interface

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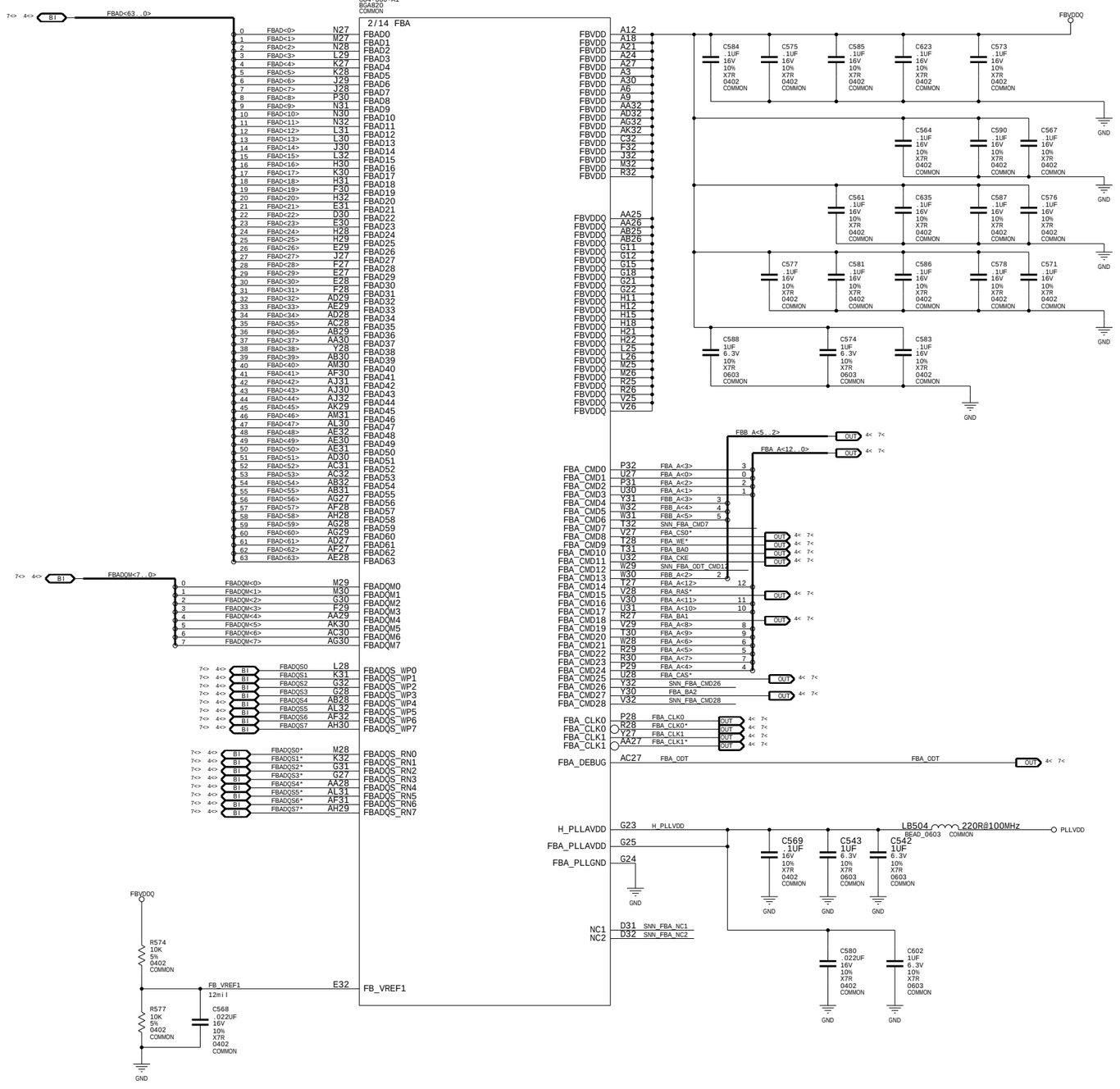
OTS1100A-1021

Frame Buffer A GPU



ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	Frame Buffer A GPU

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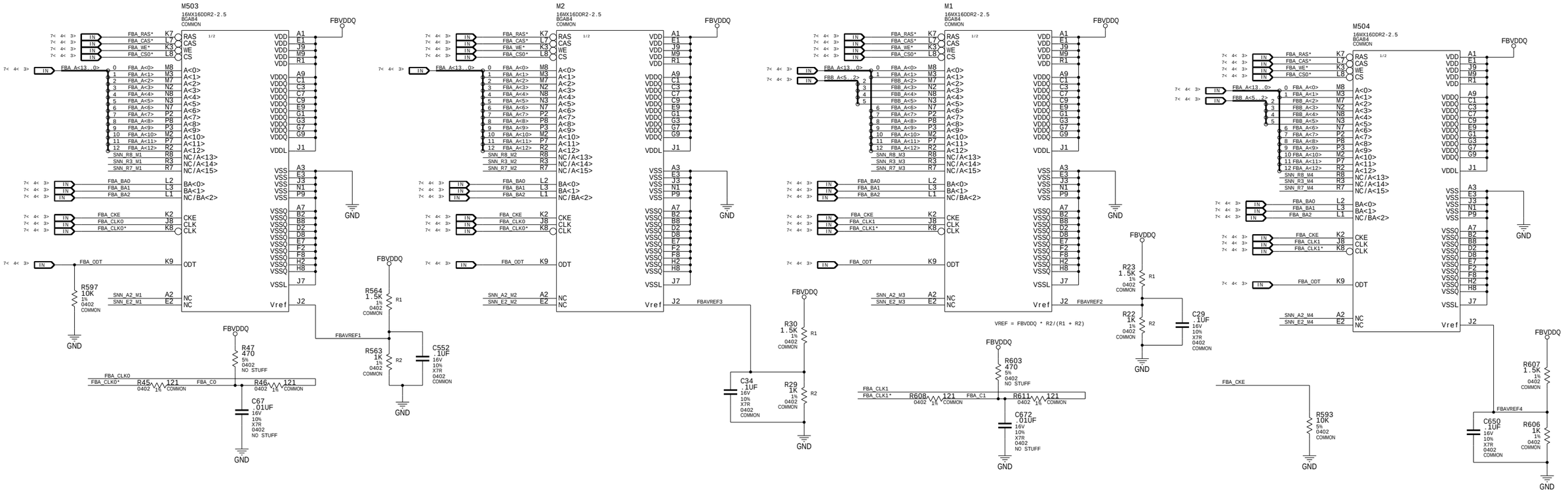
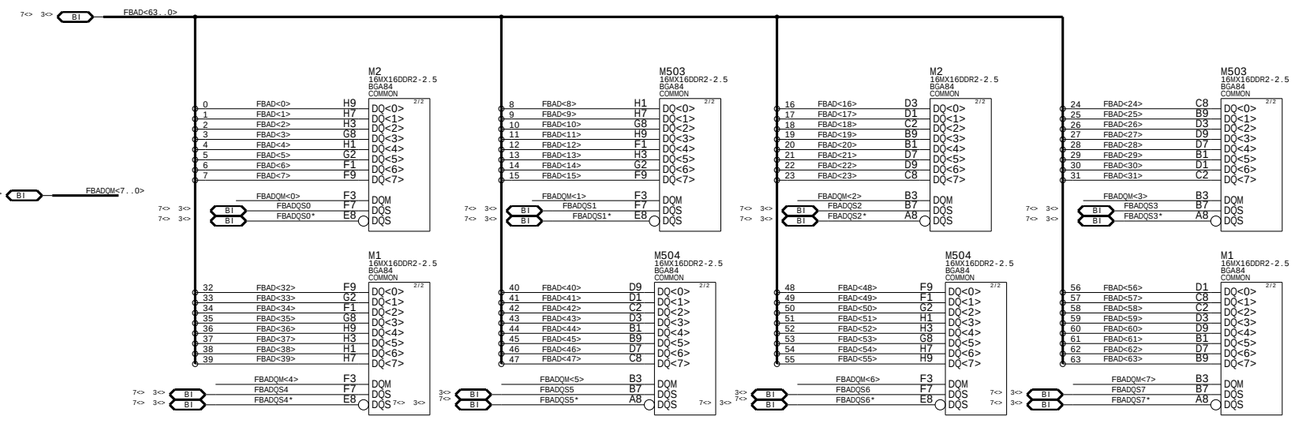
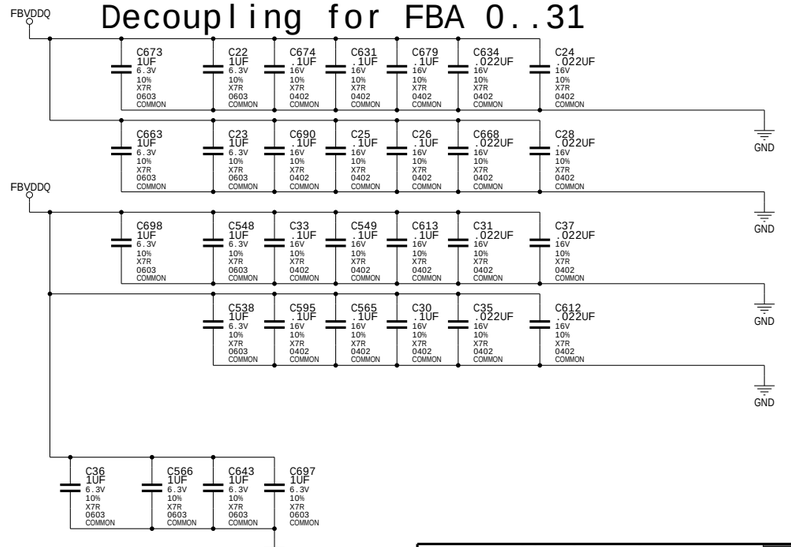
PAGE 4) MEMORY PARTITION A







ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	Frame Buffer A Memories

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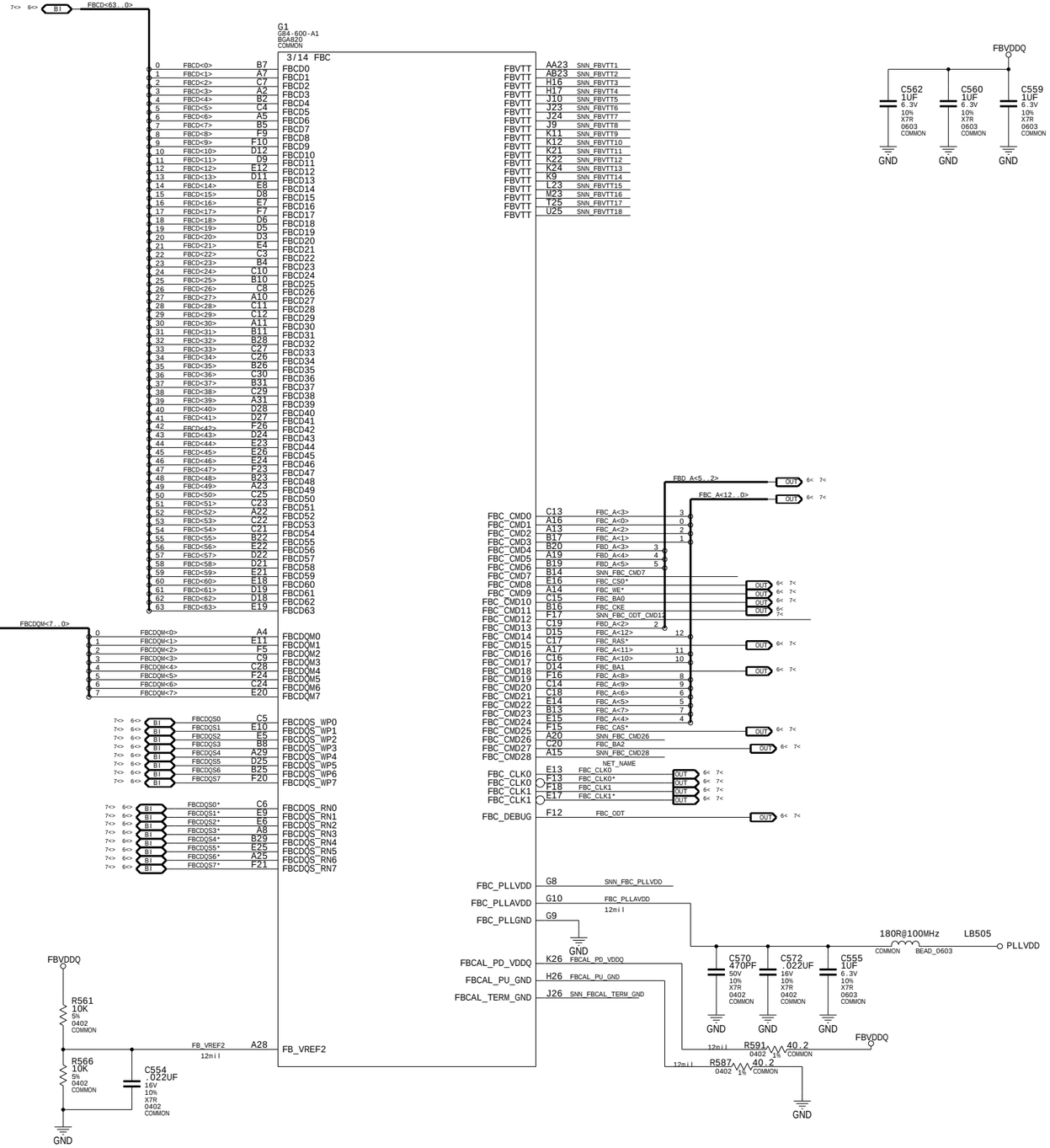
Frame Buffer C GPU



ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	Frame Buffer C GPU

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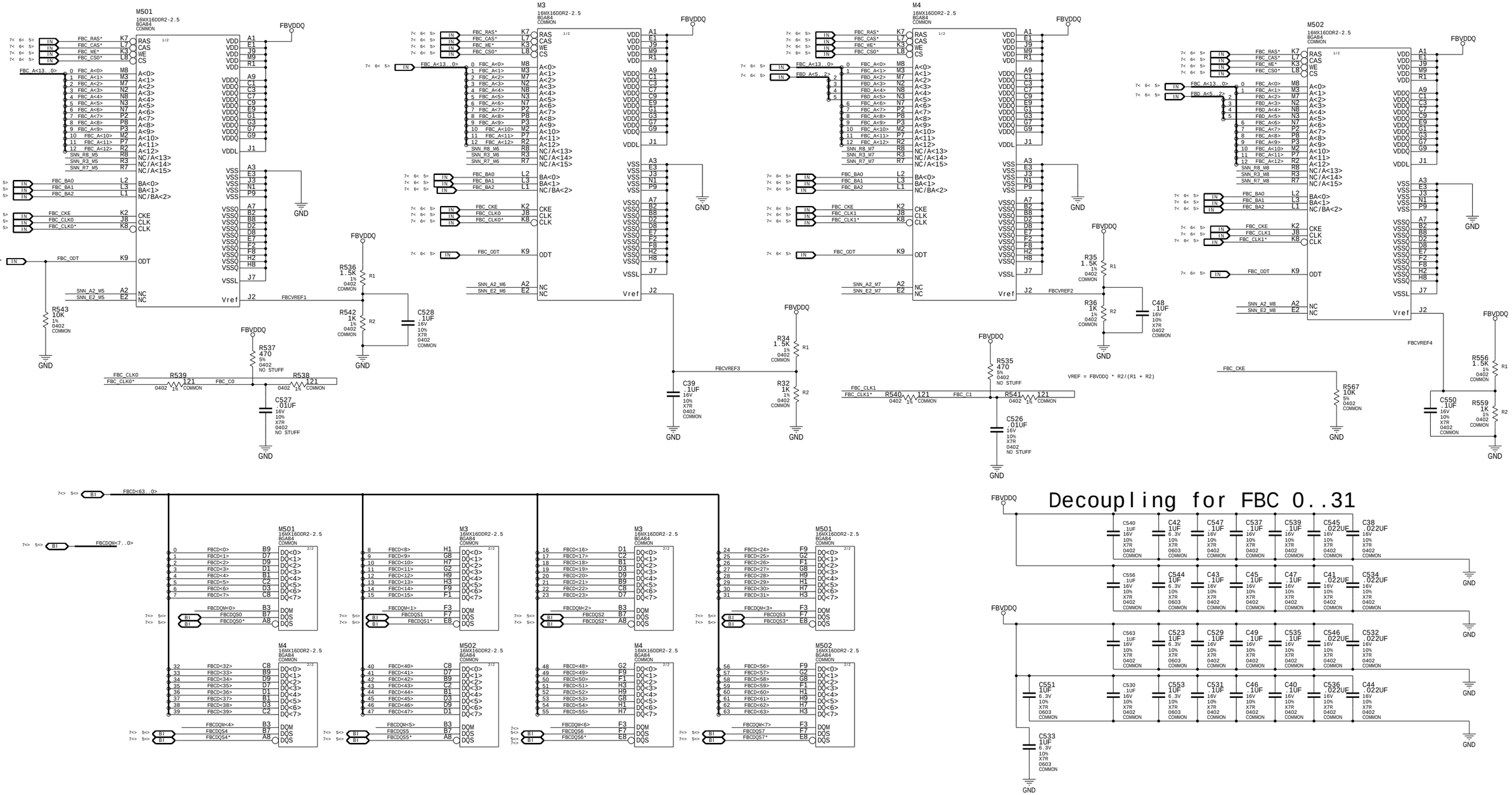
MEMORY PARTITION C



ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	Frame Buffer C Memories

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FrameBuffer Net Rules

NET RULES for FrameBuffer A

		NET	DIFFPAIR	CRITICAL	IMPEDANCE
4< 3>	IN	FBA_CLK0	FBA_CLK0	1	100DIFF
4< 3>	IN	FBA_CLK0*	FBA_CLK0	1	100DIFF
4< 3>	IN	FBA_CLK1	FBA_CLK1	1	100DIFF
4< 3>	IN	FBA_CLK1*	FBA_CLK1	1	100DIFF
4<> 3<>	BI	FBADQS0	FBADQS0	1	100DIFF
4<> 3<>	BI	FBADQS0*	FBADQS0	1	100DIFF
4<> 3<>	BI	FBADQS1	FBADQS1	1	100DIFF
4<> 3<>	BI	FBADQS1*	FBADQS1	1	100DIFF
4<> 3<>	BI	FBADQS2	FBADQS2	1	100DIFF
4<> 3<>	BI	FBADQS2*	FBADQS2	1	100DIFF
4<> 3<>	BI	FBADQS3	FBADQS3	1	100DIFF
4<> 3<>	BI	FBADQS3*	FBADQS3	1	100DIFF
4<> 3<>	BI	FBADQS4	FBADQS4	1	100DIFF
4<> 3<>	BI	FBADQS4*	FBADQS4	1	100DIFF
4<> 3<>	BI	FBADQS5	FBADQS5	1	100DIFF
4<> 3<>	BI	FBADQS5*	FBADQS5	1	100DIFF
4<> 3<>	BI	FBADQS6	FBADQS6	1	100DIFF
4<> 3<>	BI	FBADQS6*	FBADQS6	1	100DIFF
4<> 3<>	BI	FBADQS7	FBADQS7	1	100DIFF
4<> 3<>	BI	FBADQS7*	FBADQS7	1	100DIFF
4< 3>	IN	FBA_A<12..0>		2	50OHM
4< 3>	IN	FBB_A<5..2>		2	50OHM
4< 3>	IN	FBA_BA0		2	50OHM
4< 3>	IN	FBA_BA1		2	50OHM
4< 3>	IN	FBA_CKE		2	50OHM
4< 3>	IN	FBA_BA2		2	50OHM
4< 3>	IN	FBA_RAS*		2	50OHM
4< 3>	IN	FBA_CAS*		2	50OHM
4< 3>	IN	FBA_WE*		2	50OHM
4< 3>	IN	FBA_CS0*		2	50OHM
	IN	FBA_CS1*		2	50OHM
4<> 3<>	BI	FBAD<63..0>		2	50OHM
4<> 3<>	BI	FBADQM<7..0>		2	50OHM
4< 3>	IN	FBA_ODT		2	50OHM

NET RULES for FrameBuffer C

		NET	DIFFPAIR	CRITICAL	IMPEDANCE
6< 5>	IN	FBC_CLK0	FBC_CLK0	1	100DIFF
6< 5>	IN	FBC_CLK0*	FBC_CLK0	1	100DIFF
6< 5>	IN	FBC_CLK1	FBC_CLK1	1	100DIFF
6< 5>	IN	FBC_CLK1*	FBC_CLK1	1	100DIFF
6<> 5<>	BI	FBCDQS0	FBCDQS0	1	100DIFF
6<> 5<>	BI	FBCDQS0*	FBCDQS0	1	100DIFF
6<> 5<>	BI	FBCDQS1	FBCDQS1	1	100DIFF
6<> 5<>	BI	FBCDQS1*	FBCDQS1	1	100DIFF
6<> 5<>	BI	FBCDQS2	FBCDQS2	1	100DIFF
6<> 5<>	BI	FBCDQS2*	FBCDQS2	1	100DIFF
6<> 5<>	BI	FBCDQS3	FBCDQS3	1	100DIFF
6<> 5<>	BI	FBCDQS3*	FBCDQS3	1	100DIFF
6<> 5<>	BI	FBCDQS4	FBCDQS4	1	100DIFF
6<> 5<>	BI	FBCDQS4*	FBCDQS4	1	100DIFF
6<> 5<>	BI	FBCDQS5	FBCDQS5	1	100DIFF
6<> 5<>	BI	FBCDQS5*	FBCDQS5	1	100DIFF
6<> 5<>	BI	FBCDQS6	FBCDQS6	1	100DIFF
6<> 5<>	BI	FBCDQS6*	FBCDQS6	1	100DIFF
6<> 5<>	BI	FBCDQS7	FBCDQS7	1	100DIFF
6<> 5<>	BI	FBCDQS7*	FBCDQS7	1	100DIFF
6< 5>	IN	FBC_A<12..0>		2	50OHM
6< 5>	IN	FBD_A<5..2>		2	50OHM
6< 5>	IN	FBC_BA0		2	50OHM
6< 5>	IN	FBC_BA1		2	50OHM
6< 5>	IN	FBC_CKE		2	50OHM
6< 5>	IN	FBC_BA2		2	50OHM
6< 5>	IN	FBC_RAS*		2	50OHM
6< 5>	IN	FBC_CAS*		2	50OHM
6< 5>	IN	FBC_WE*		2	50OHM
6< 5>	IN	FBC_CS0*		2	50OHM
	IN	FBC_CS1*		2	50OHM
6<> 5<>	BI	FBCD<63..0>		2	50OHM
6<> 5<>	BI	FBCDQM<7..0>		2	50OHM
6< 5>	IN	FBC_ODT		2	50OHM

ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	Frame Buffer Physical Constrains

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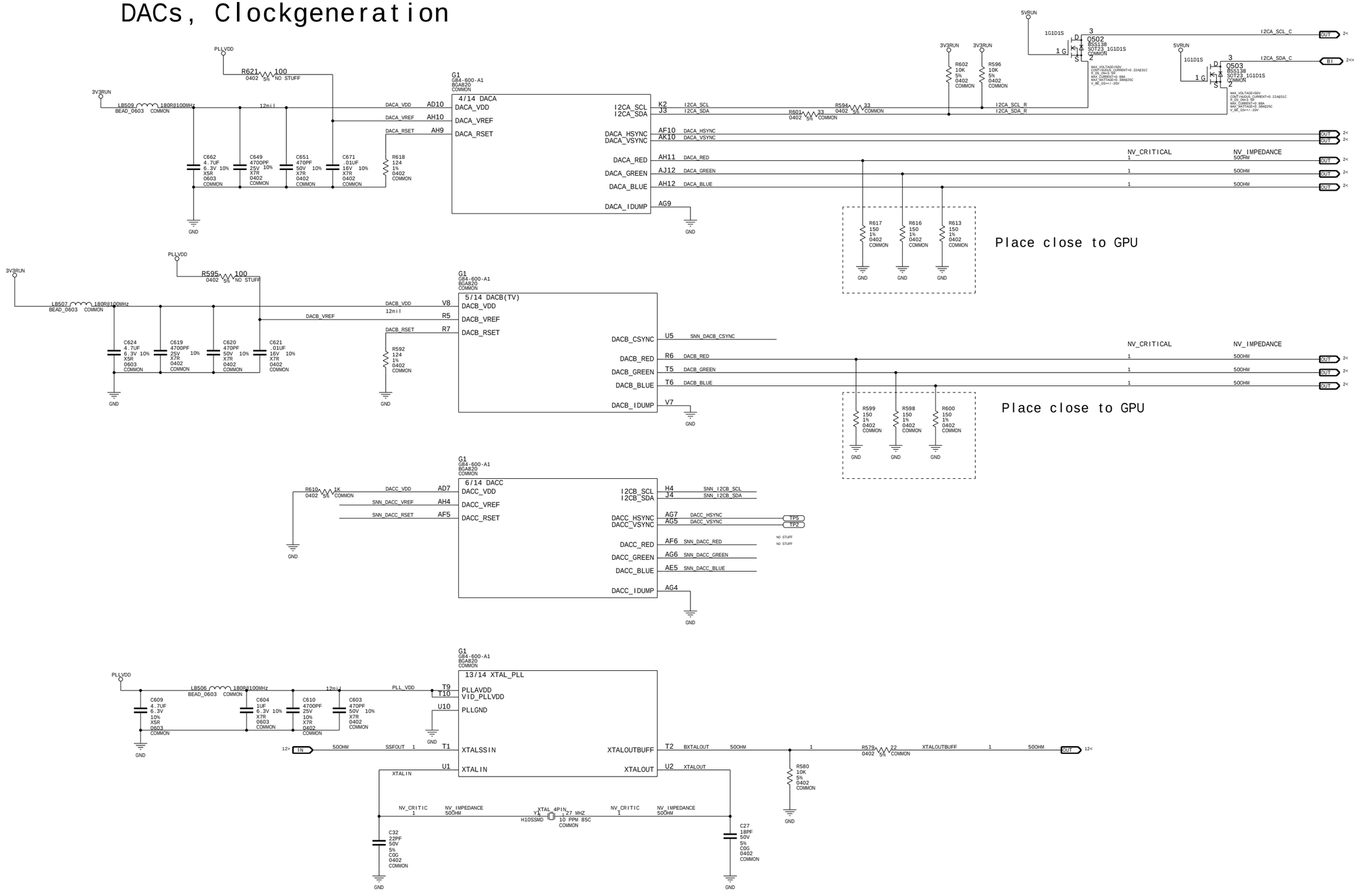
DACs, Clockgeneration



ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	DACs, Clock-Generation

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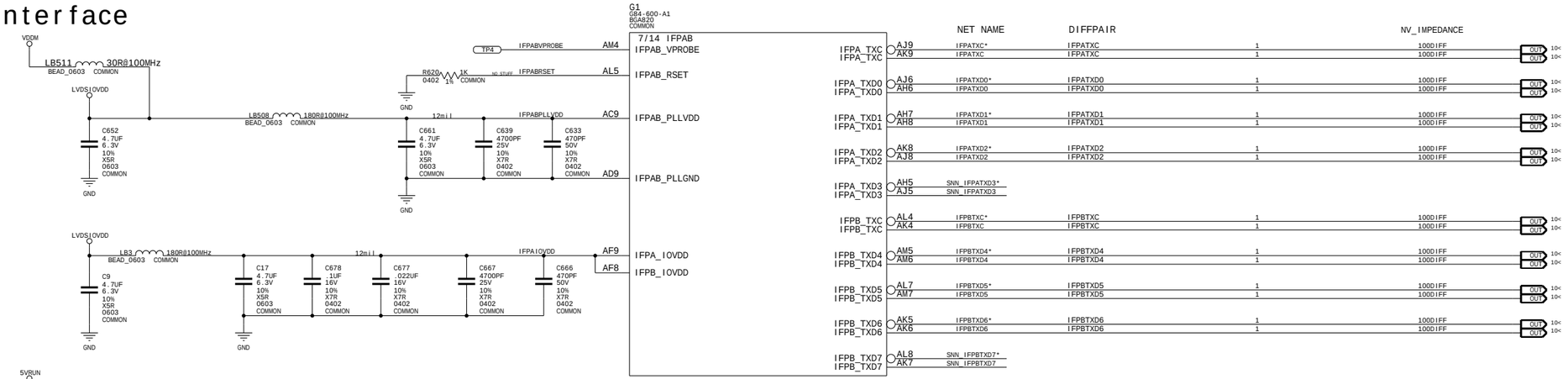
LVDS / TMDS Interface



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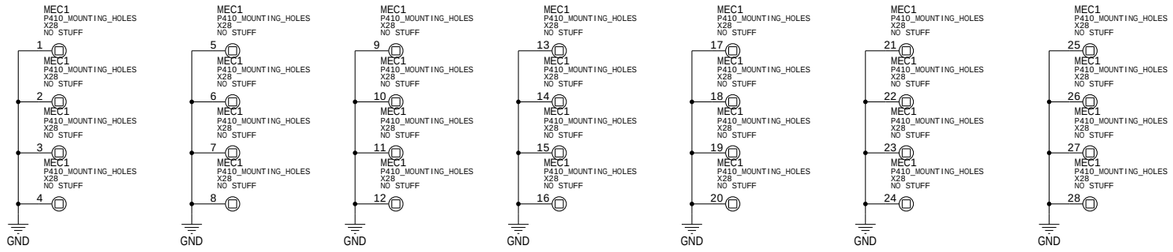

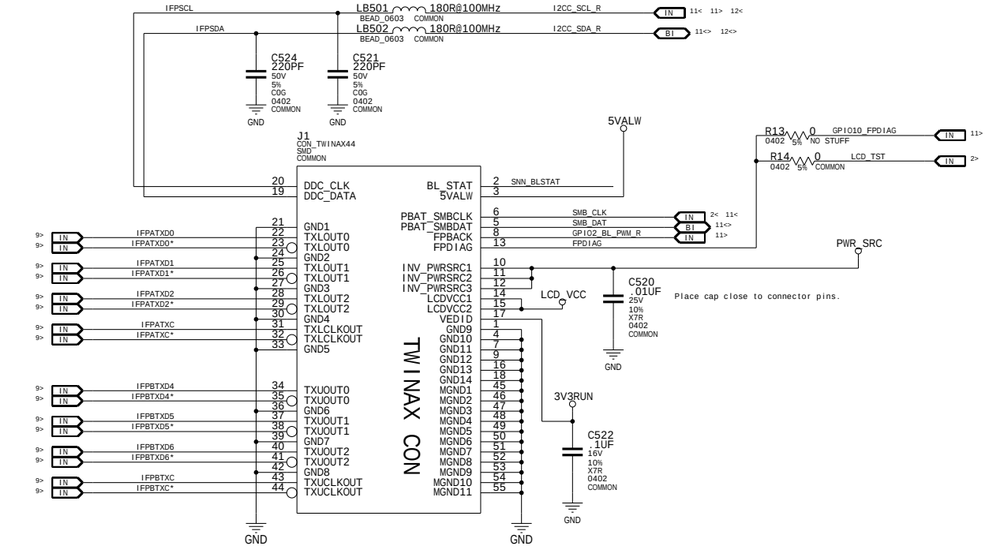

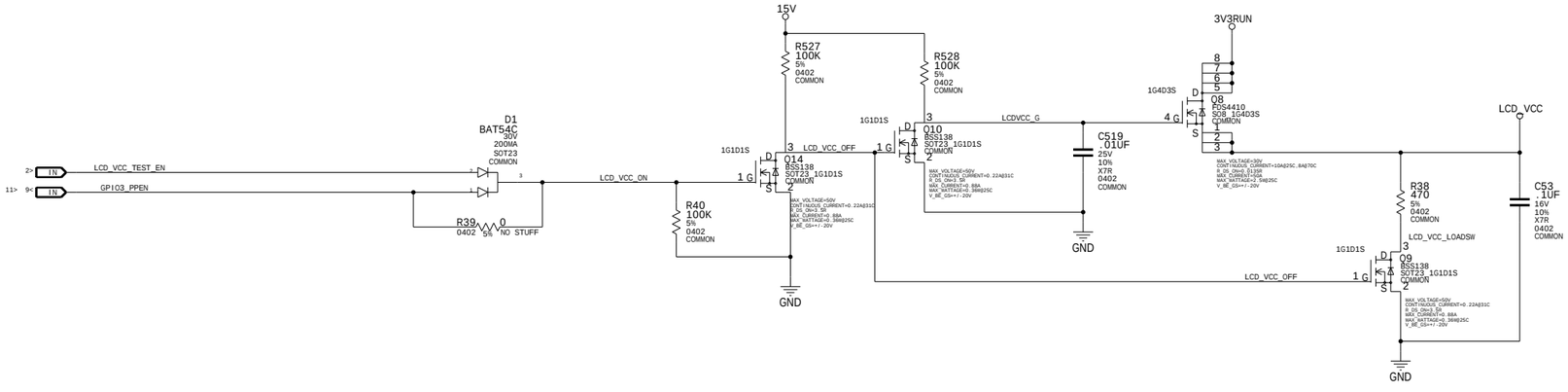

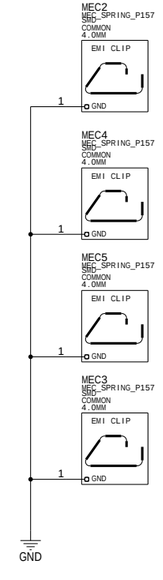

ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	LVDS I/O

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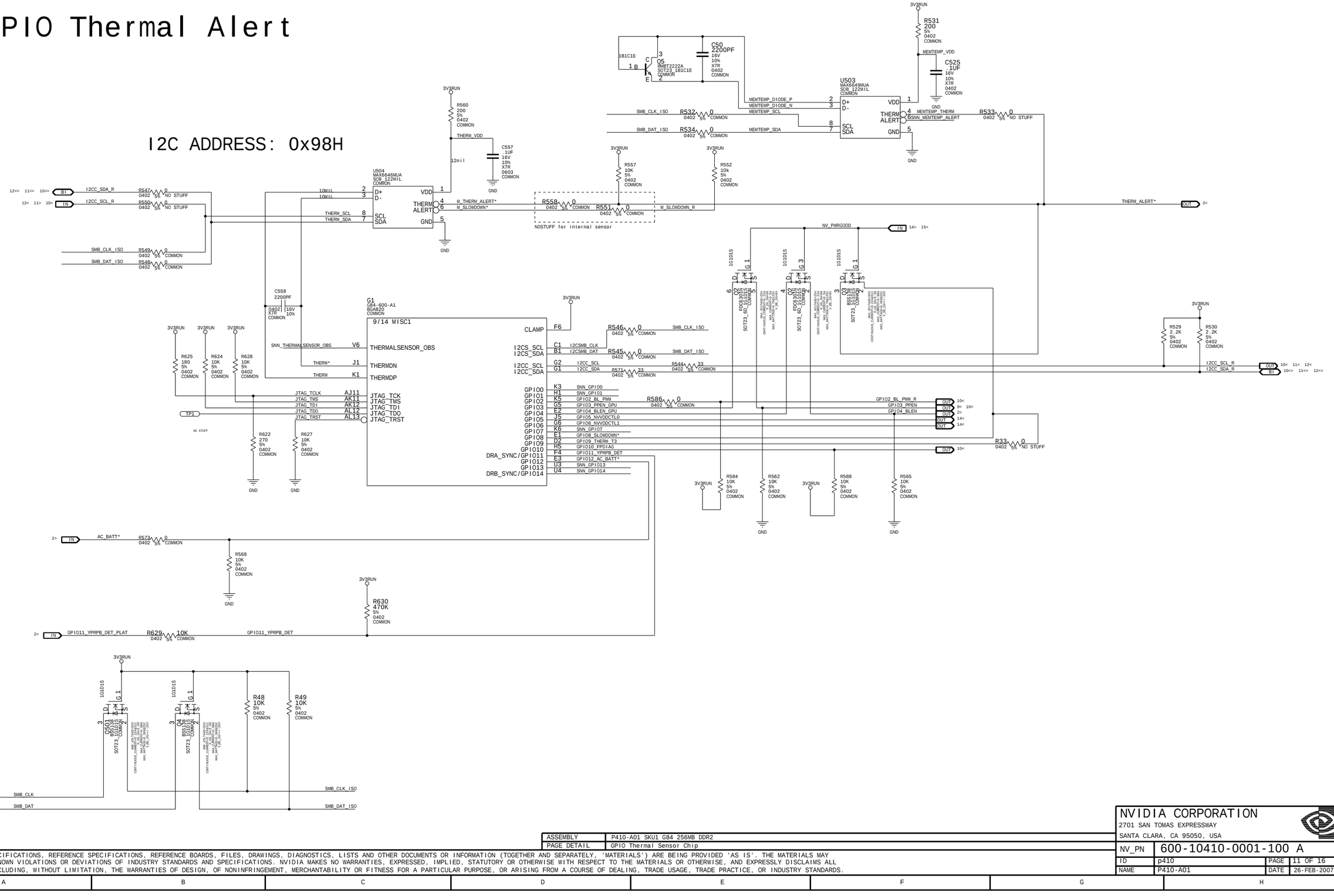
GPIO Thermal Alert

I2C ADDRESS: 0x98H



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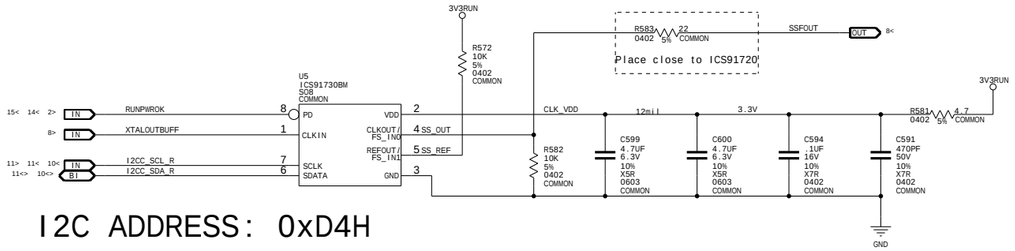
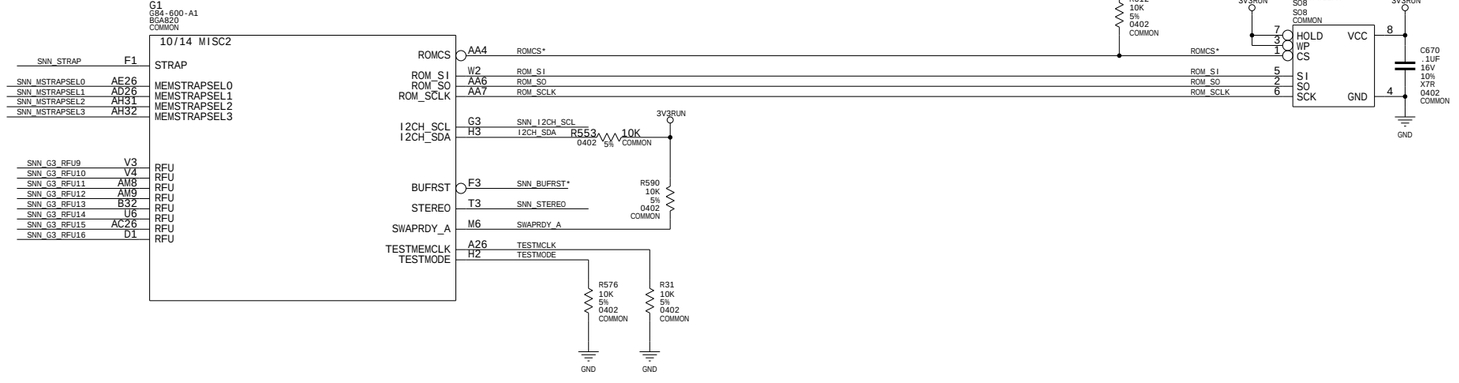
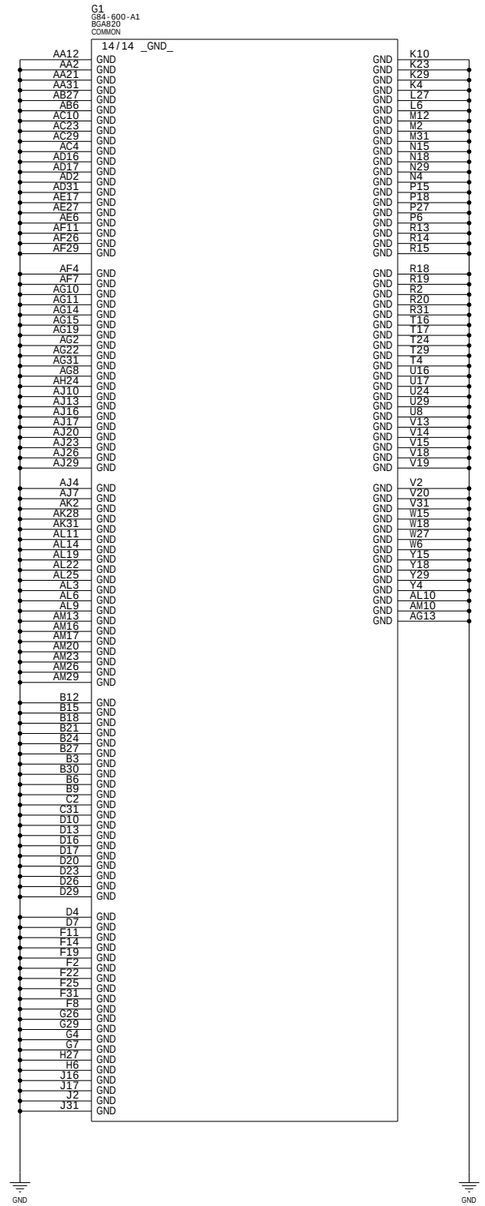
SPREAD SPECTRUM CLOCK



I2C ADDRESS: 0xD4H

ROM Interface





ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	Spread Spectrum, BIOS

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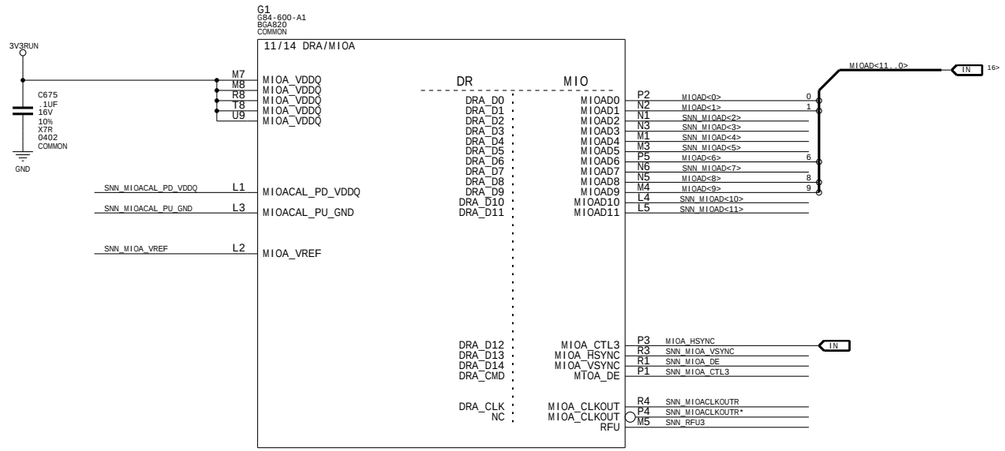
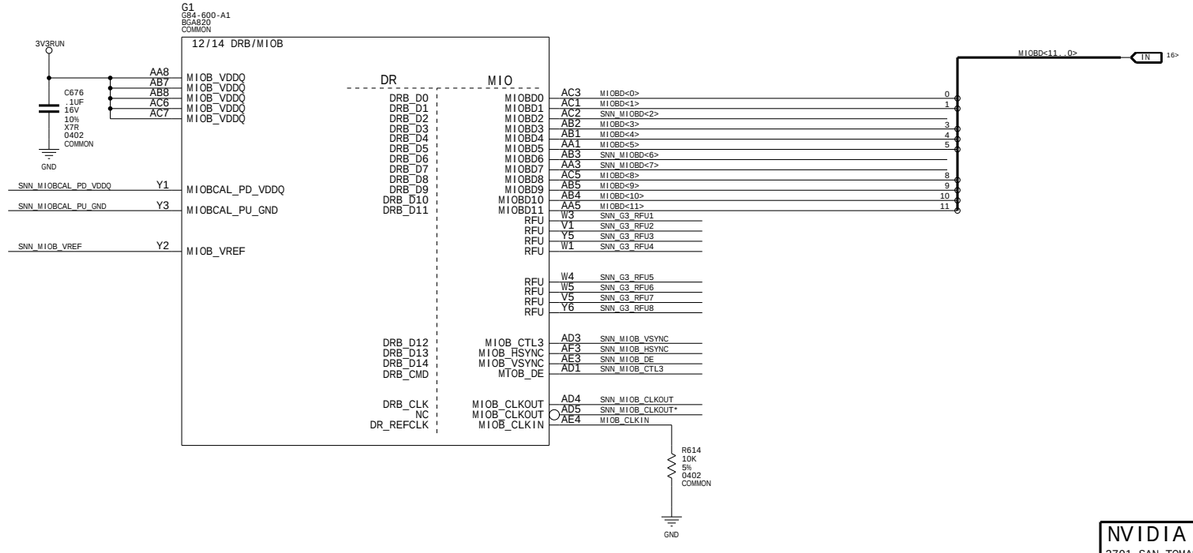
MIOA



MIOB



ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	MIOA, MIOB

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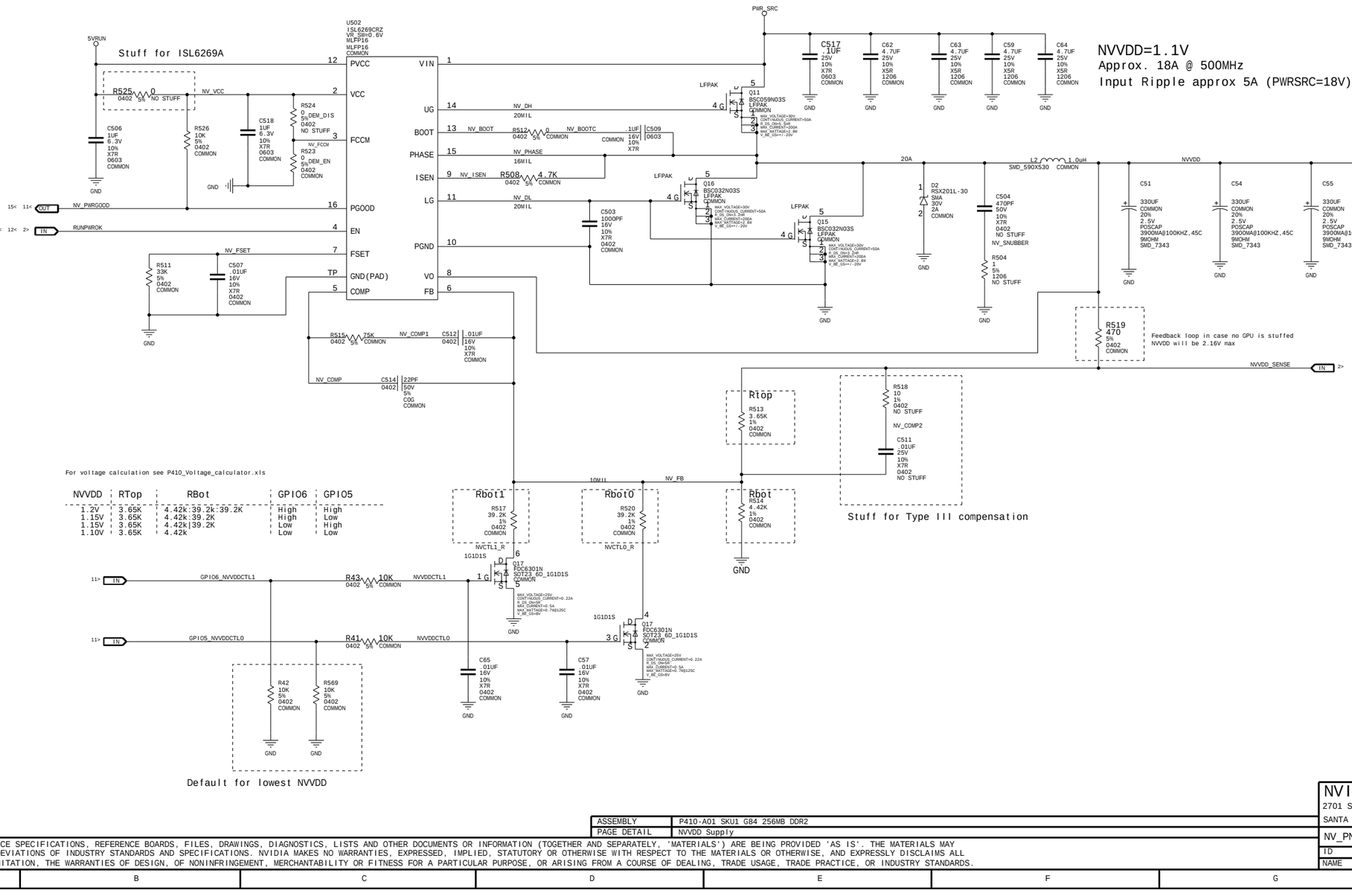
NVVDD SUPPLY

NET	MIN_LINE_WIDTH	VOLTAGE
FBVDDQ	12MIL	1.8V
NVVDD	12MIL	1.2V



NVVDD	RTop	RBot	GPIO6	GPIO5
1.2V	3.65K	4.42k:39.2k:39.2K	High	High
1.15V	3.65K	4.42k:39.2K	High	Low
1.15V	3.65K	4.42k|39.2K	Low	High
1.10V	3.65K	4.42k	Low	Low

ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	NVVDD Supply

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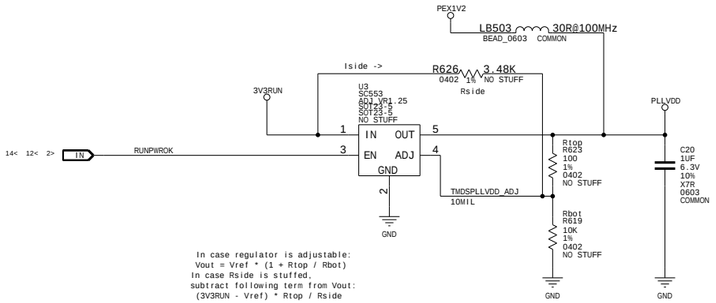
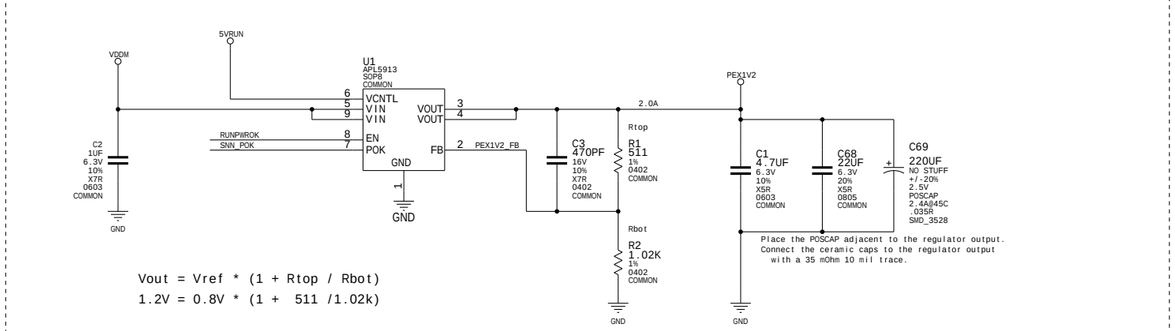
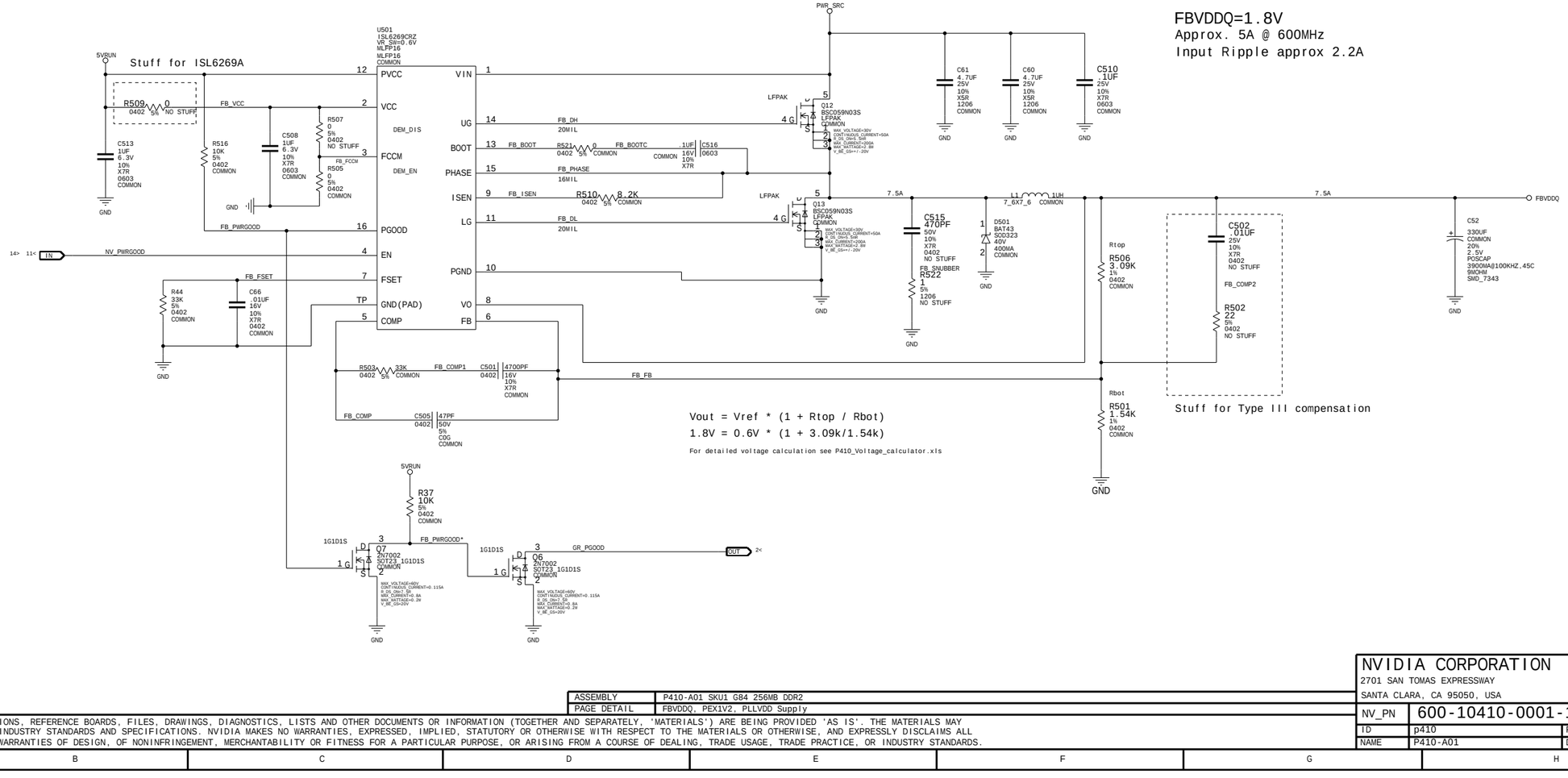
PLLVDD SUPPLY



PEX1V2 SUPPLY



FBVDDQ SWITCHER



FBVDDQ=1.8V
Approx. 5A @ 600MHz
Input Ripple approx 2.2A

ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	FBVDDQ, PEX1V2, PLLVDD Supply

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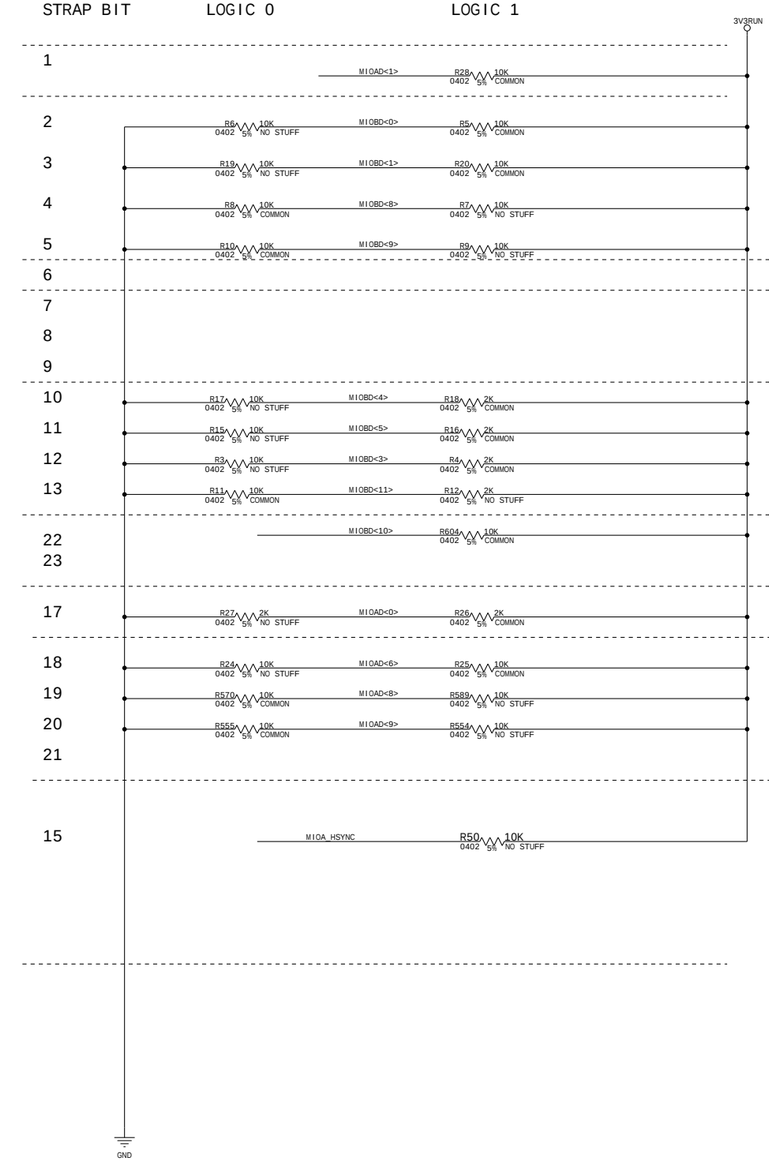
13< OUT MIOBD<11..0>

13< OUT MIOAD<11..0>

OUT MIOA_HSYNC



STRAP BIT	LOGIC 0	LOGIC 1
REG: NV_STRAP_0		
1	SUB_VENDOR	0: SYSTEM BIOS 1: ADAPTER BIOS DEFAULT
2	RAM_CFG_0	RAM_CFG[3:0] MS_0001:
3	RAM_CFG_1	MS_0011:
4	RAM_CFG_2	MS_0101: MS_0111:
5	RAM_CFG_3	MS_0111: MS_1xxx: same as above 64 Bit wide
6	CRYSTAL_0	0: 27MHz DEFAULT 1: RESERVED
7	TV_MODE_0	
8	TV_MODE_1	MS_001: NTSC_J DEFAULT
9	TV_MODE_2	
10	PCI_DEVID_0	MS_0100:
11	PCI_DEVID_1	
12	PCI_DEVID_2	
13	PCI_DEVID_3	
22	ROM_TYPE_0	MS_00: PARALLEL MS_01: SERIAL AT25F DEFAULT MS_10: SERIAL SST45VF MS_11: RESERVED
23	ROM_TYPE_1	
17	PEX_PLL_EN_TERM100	0: 100 Ohm termination disabled 1: Enabled
18	3GIO_PADCFG_LUT_ADR[0]	
19	3GIO_PADCFG_LUT_ADR[1]	
20	3GIO_PADCFG_LUT_ADR[2]	
21	3GIO_PADCFG_LUT_ADR[3]	
REG: NV_STRAP_1		
15	SLOT_CLK_CFG	

ASSEMBLY	P410-A01 SKU1 G84 256MB DDR2
PAGE DETAIL	Straps

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