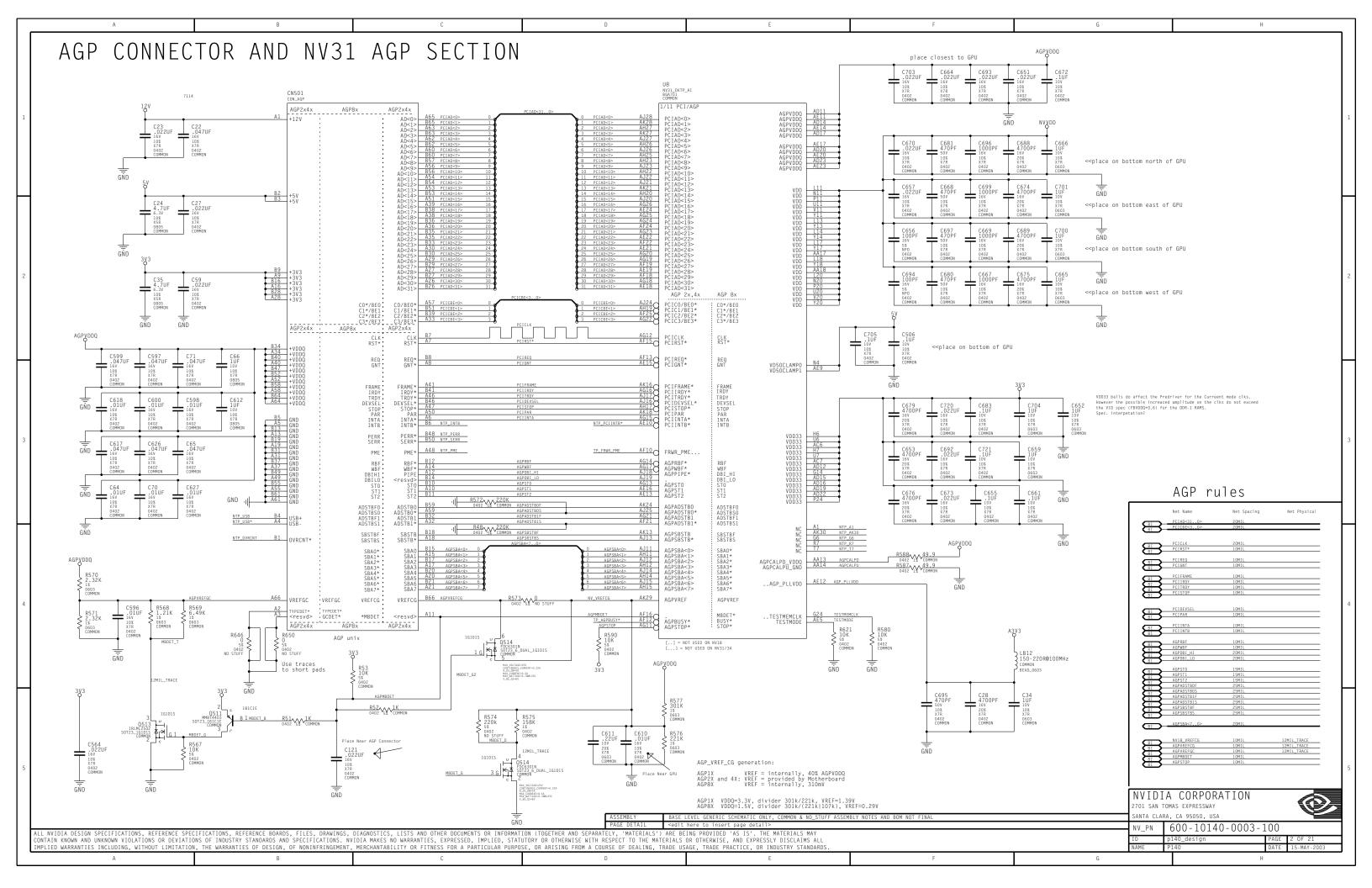
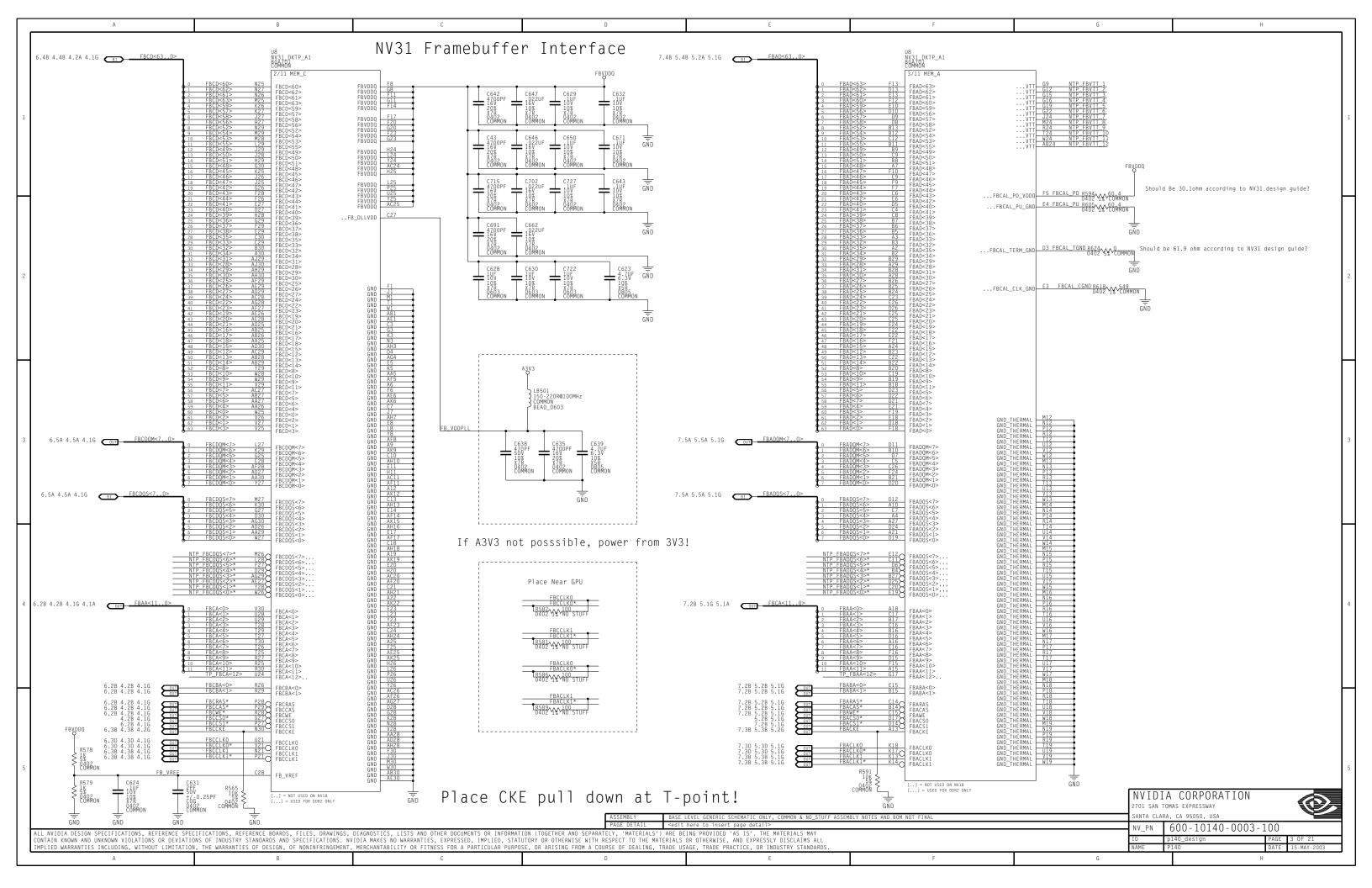
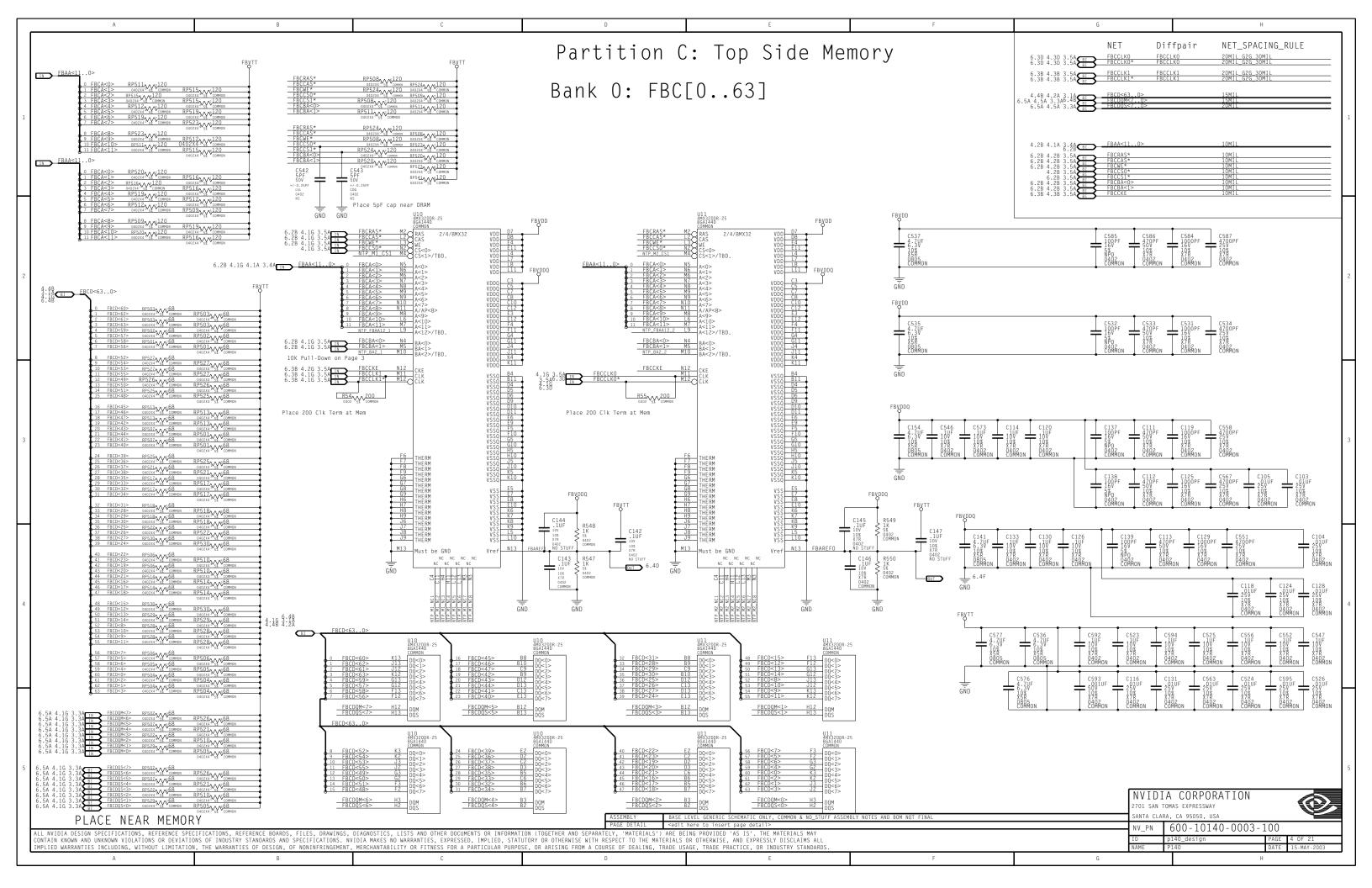
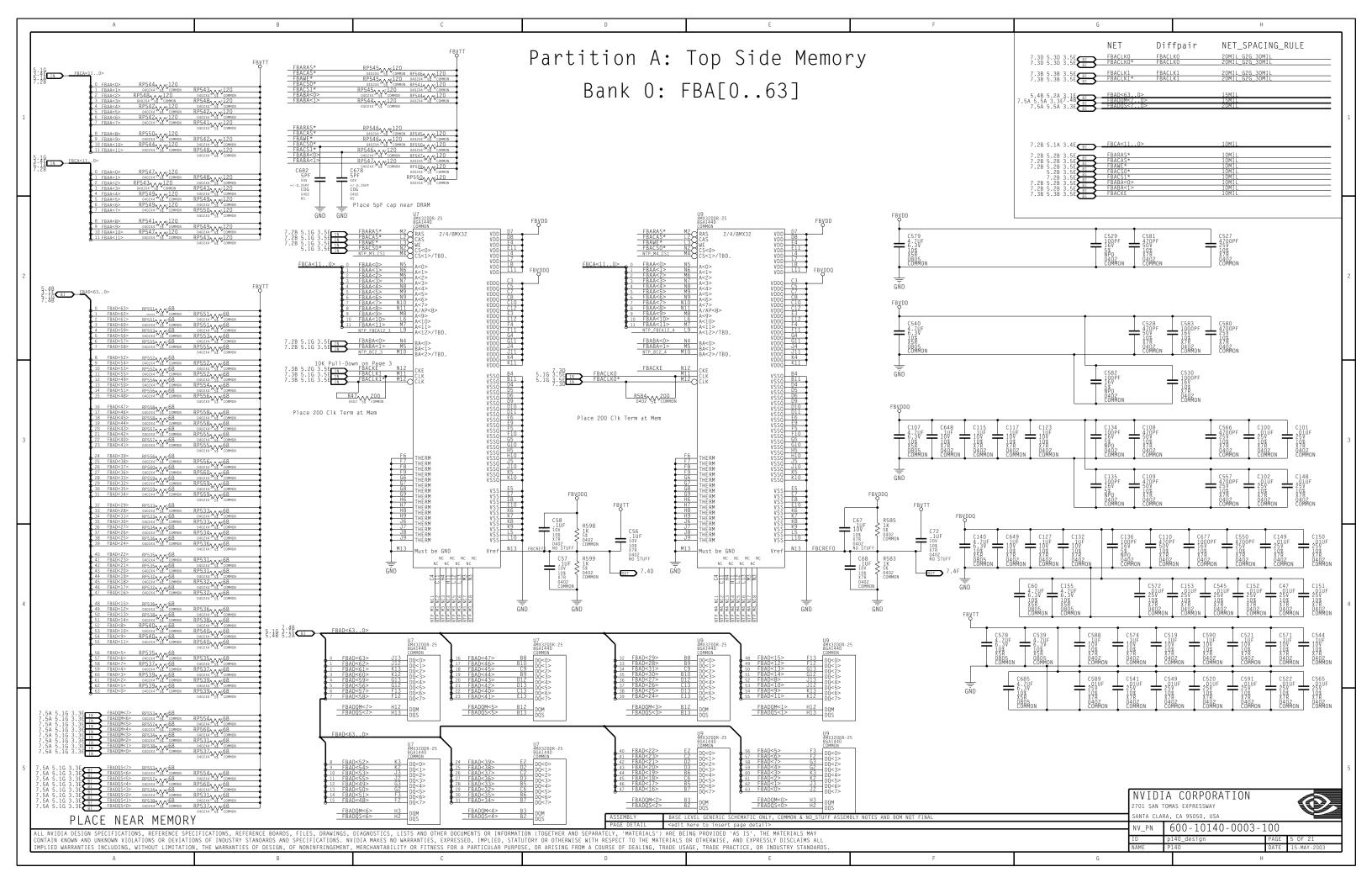
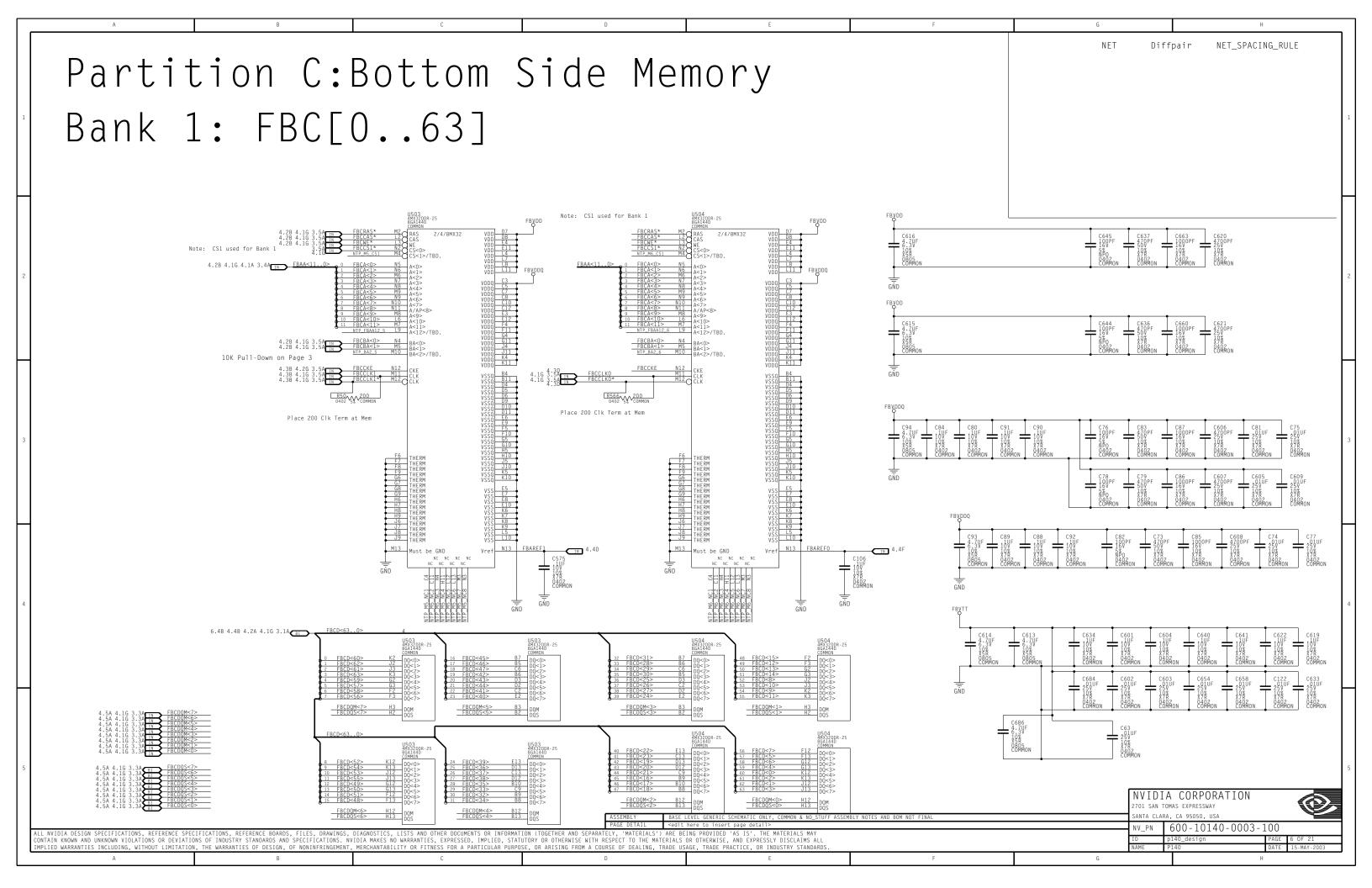
P140, NV31, 4Mx32, 128MB, VIDEO IN/OUT, DVI-I, VGA HISTORY: A00Page Overview INITIAL VERSION First Review 1 31P140 OVERVIEW X00 - 12/04/02: Updated D30 Diode on Page 16 2 NV31 AGP Section and AGP connector X00 - 12/05/02: Changed VGA Connectors to Slim. Added Bracket. Added 2X5 Connector for TUNER Card 3 NV31 FRAMEBUFFER Interface X00 - 12/06/02: Changed Pri VGA back to Original, 4 MEMORY Partition C Bits 0...31 Changed Sec VGA to SLIM_DVIMTG, Hooked up 10 Pin Tuner Con Replaced 27Mhz Crystal with low profile version 5 MEMORY Partition A Bits 31..63 Corrected Error with PGND on 6529 circuit 6 MEMORY Partition C Bits 0..31 X00 - 12/09/02: Added C Partition 120 ohm RPacks Changed and Deleted components on all 3 Switchers 7 MEMORY Partition A Bits 31..63 Deleted Parallel ROM. 8 NV31 DACA, DACB output, SYNC amplifier X00 - 12/10/02: Replaced L26 and L31 with SMD_12X5MM Jedec type Rearranged Mem U5.U7.U8.and U4 to be on the same pages PLL Section Added Other TMDS DVI connector with Hot Plug detect 9 PRIMARY DISPLAY (DACA) Filter and DB15 Connector Changed Pri VGA connector to SLIM_MTG X00 - 12/11/02: Swapped out J4 2X5 with 1X10 Header 10 SECONDARY DISPLAY (DACB) Added two 200 ohm CLK term. Resistors DACB Multiplexer Filter long DB15 Connector Added 2nd TMDS Diff Spacing Constraints Added Power Supply I. II. and III Spacing Constraints 11 NV31 INTERNAL TMDS Transmitter Backet Changed for Correct Jedec Type TMDS Backdrive circuit Changed C571,C567,C562 to 7343 pkg to fit under FANSINK X00 - 12/12/02: Changed R223 to 95.3K, Deleted 52MM HEATSINK symbol Hotplug detection and DVI-I Connector X00 - 12/16/02: Added additional decoupling caps to Memory; Cleaned share footprint notes 12 VIDEO CAPTURE Philips 7114 I/O Changed COMMON Attribute on a few components to NS (NO STUFF) 13 VIDEO IN/OUT, Filter and Connector A01 X00 - 01/22/03: Changed a few Rset values page 8, Crystal cap values, TV out ind value added 2 res for USER_O Strap (Apple), NVVDD changed D31, 12V_EXT to 5V_EXT VIDEO INTERNAL Input NVVDD changed a few Compensation component values, Added Optional Linear for A3V3 14 VIP. DVO. GPIO. FAN Control. and TEMP Sensor Section X00 - 01/23/03: X00 - 01/29/03: Removed FBVDD ISL6529 and Linear Reg for A3V3 and Current Share 15 BIOS Srapping, Serial ROM Changed stuff option NVDD33 reg from 3V3 to A3V3. Changed VGA conn to Regular. 16 Power Supply I , NVVDD, 3V3TMDS, TMDSPLLVDD ISL6522 NVVDD Supply changes: L27, C588, C586, C587, C584, added two share footprint ALE's Changed a few other Power supply component values but no pkg changes. 17 Power Supply II , FBVDD/Q, FBVTT ISL6225 Changed VGA / DVI-I conn. to a Slim VGA, Removed J9 Link C DVI-I and Link C components. 18 Power Supply III, A3.3V Linear Reg, Current Share Changed TV in/out Inductors, deleted 2 filter caps on tuner header. 01/30/03: Added 2 Strap resistors for PCI DEVIDE31 Glbond. EXT_5V and EXT_12V Changed Current Share circuit to 0805 size, Change D30 and D33 diodes to FETS. 02/04/03: Deleted NVDD33 Linear not needed because no amplitude DDR-1 spec. violation. Moved AGPSTOP pull-up to A3V3 from NVDD33. Added CGND2 to J3.25,R121,R94. Changed Current Share Net Names and Changed BKT1 Jedec type. VARIANT 02/04/03: AGPSTOP R to net 3V3, R121 back to CGND, J2.16 to CGND2, fixed all un-named nets 00-10140-0000-004 UNDEFINED> 02/05/03: Modified BRK1 for correct Jedec type and NVPN, Current share R value change <UNDEFINED: <UNDEFINED: INDEFINED> 02/06/03: Added 6 more 0805 R's to NVVDD Current Share CKT. <UNDEFINED>
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<UNDEFINED> 02/07/03: Cosmetic Cleanup and Added Notes Only. UNDEFINED> UNDEFINED: <UNDEFINED> UNDEFINED> A02 <UNDEFINED> UNDEFINED> :UNDEFINED> 03/10/03: FMI fixes. Combine CGND to GND remove CGND to GND resistors. EMI fix. Added Series Resistor to GND on TMDS IFPAIOGND and IFPBIOGND. <UNDEFINED> UNDEFINED> UNDEFINED> 03/14/03: Moving C708 & C735 to the IFPAIOGND and IFPBIOGND nets. So at least one decoupling <UNDEFINED> UNDEFINED> :UNDEFINED> <UNDEFINED> UNDEFINED> SUNDEFINED> cap is near the ball. Changed ISL6225 VIN pin 14 to be 6225_VCC_IN_F net. This provides <UNDEFINED> <UNDEFINED> <UNDEFINED> UNDEFINED> UNDEFINED> UNDEFINED> Feed-Forward rejection of the Input voltage variation. A03 04/25/03: Added New TMDS termination to Link A, changed U509 3V3TMDS regulator to LT1117 (800ma) Added bulk cap near Fan connector J6 and series resistor and cap on GPIO fan control. Deleted R65 and R66 IFPxIOGND resistors because it did not help EMI Changed TP4 to 52P32 size. Removed Link B from DVI connector. A04 05/15/03: No Changes. PCB INT1 Layer change. 602-10140-0003-100 NV31 Flip Chip Schematic NVIDIA CORPORATION 701 SAN TOMAS EXPRESSWAY ANTA CLARA CA 95050 IISA 600-10140-0003-100 ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS

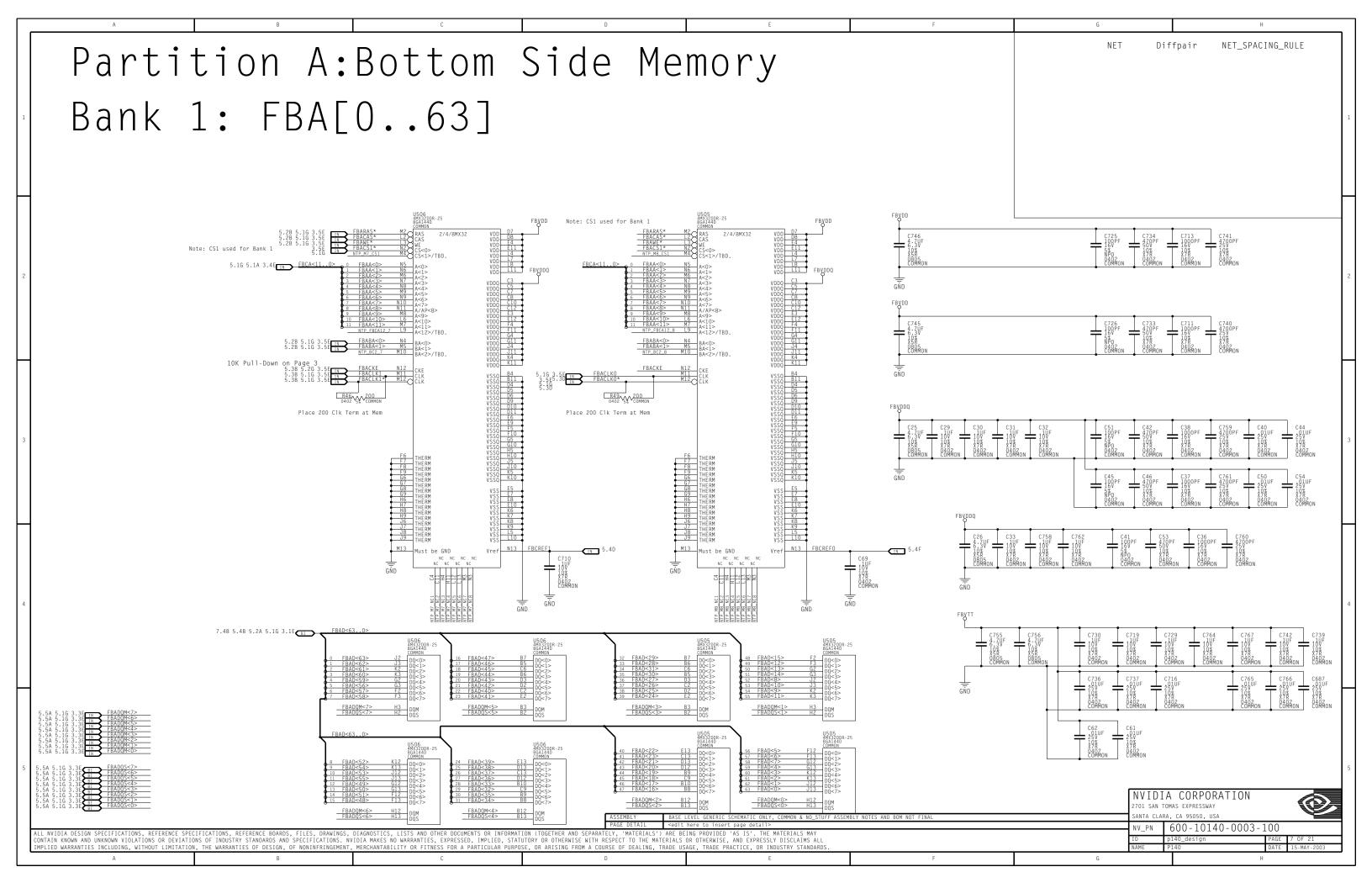


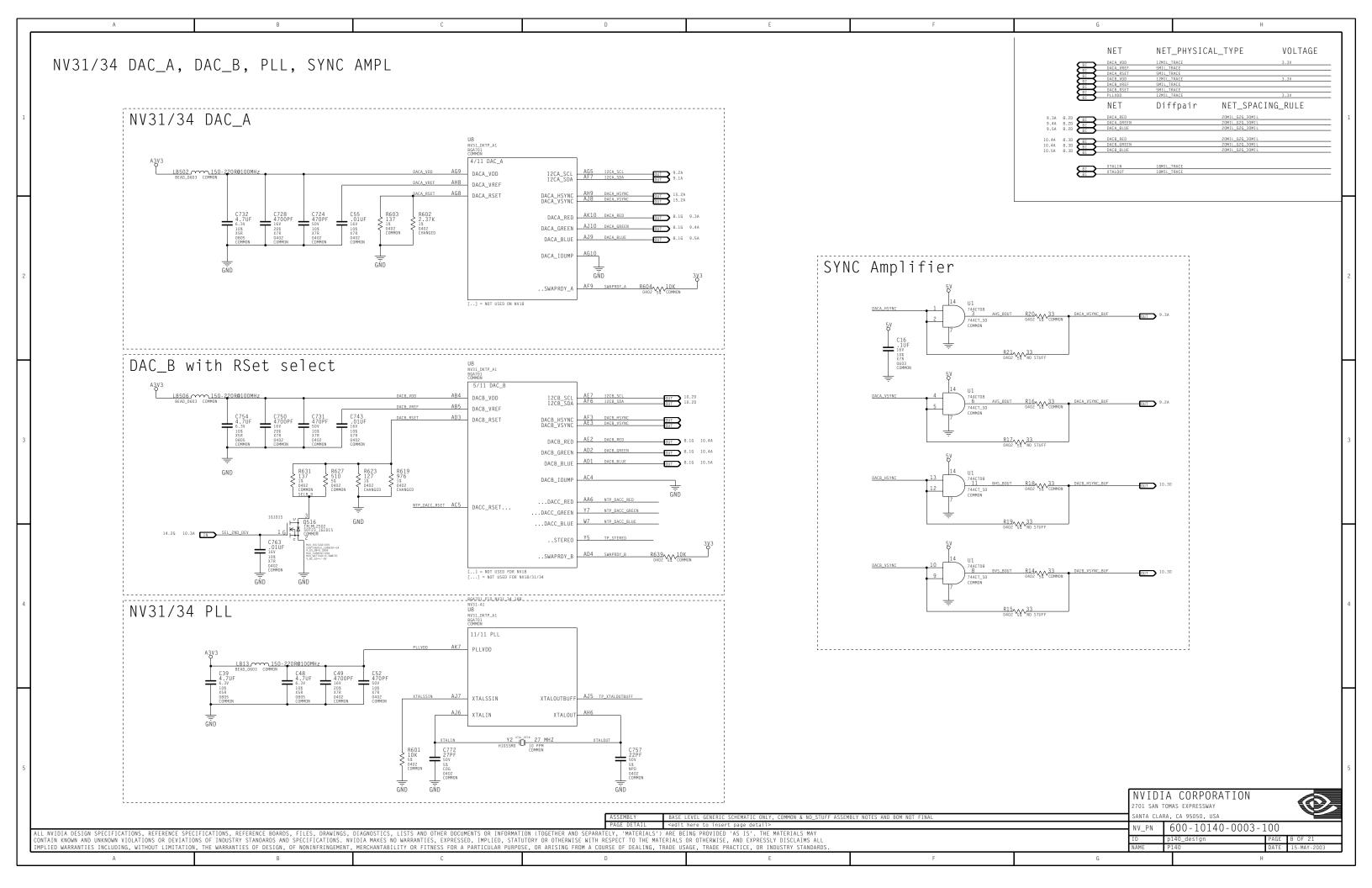


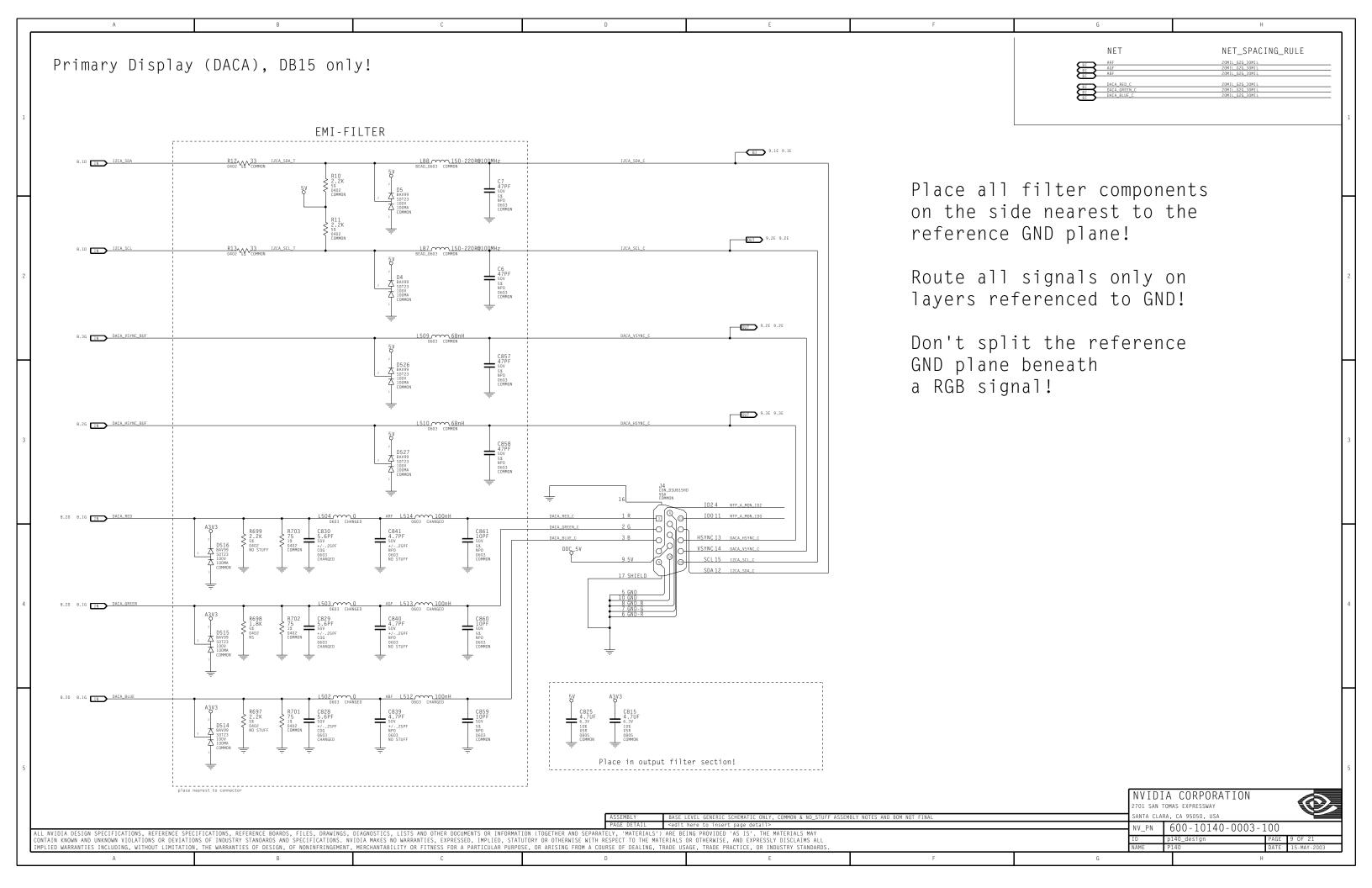


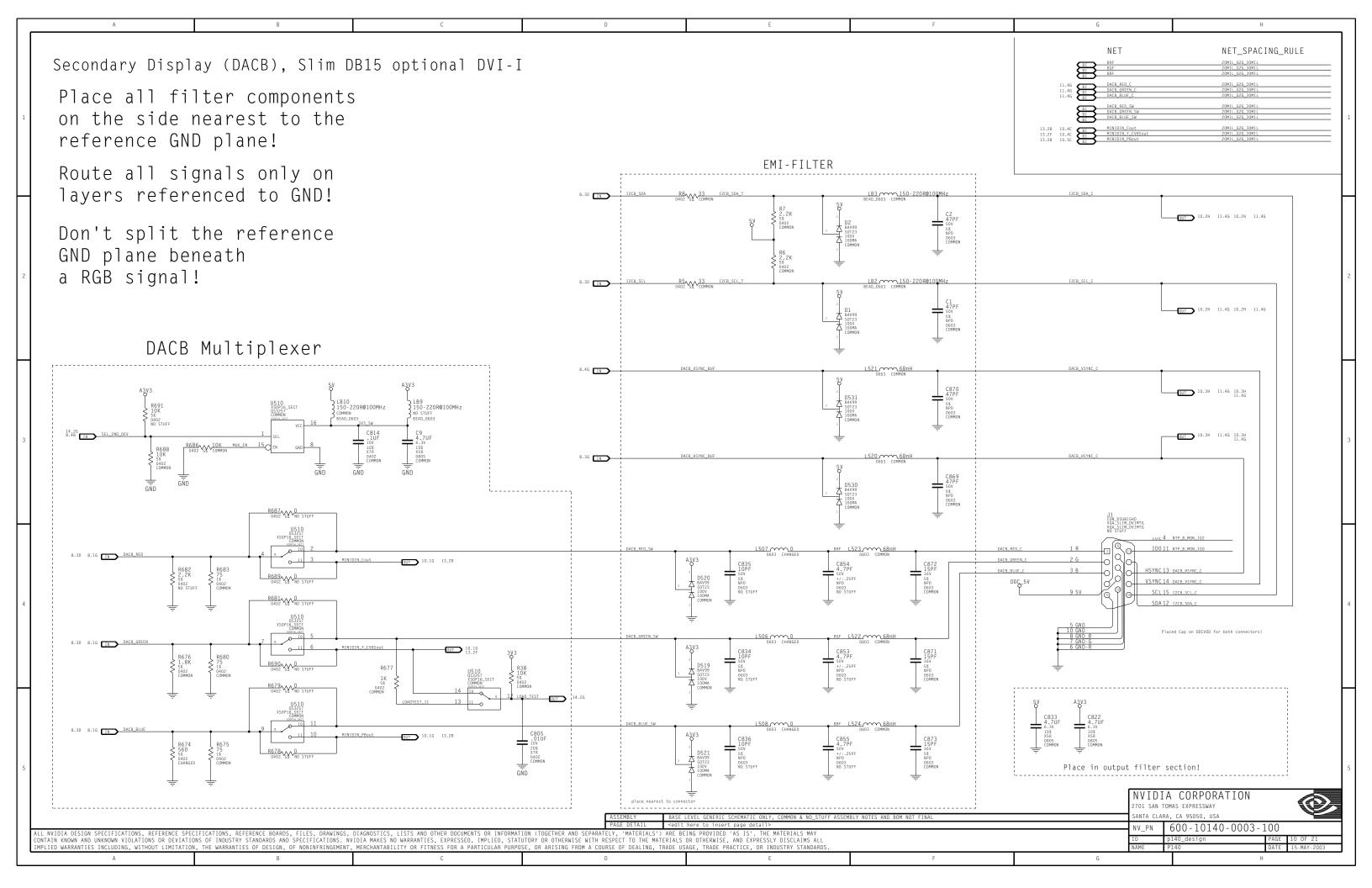


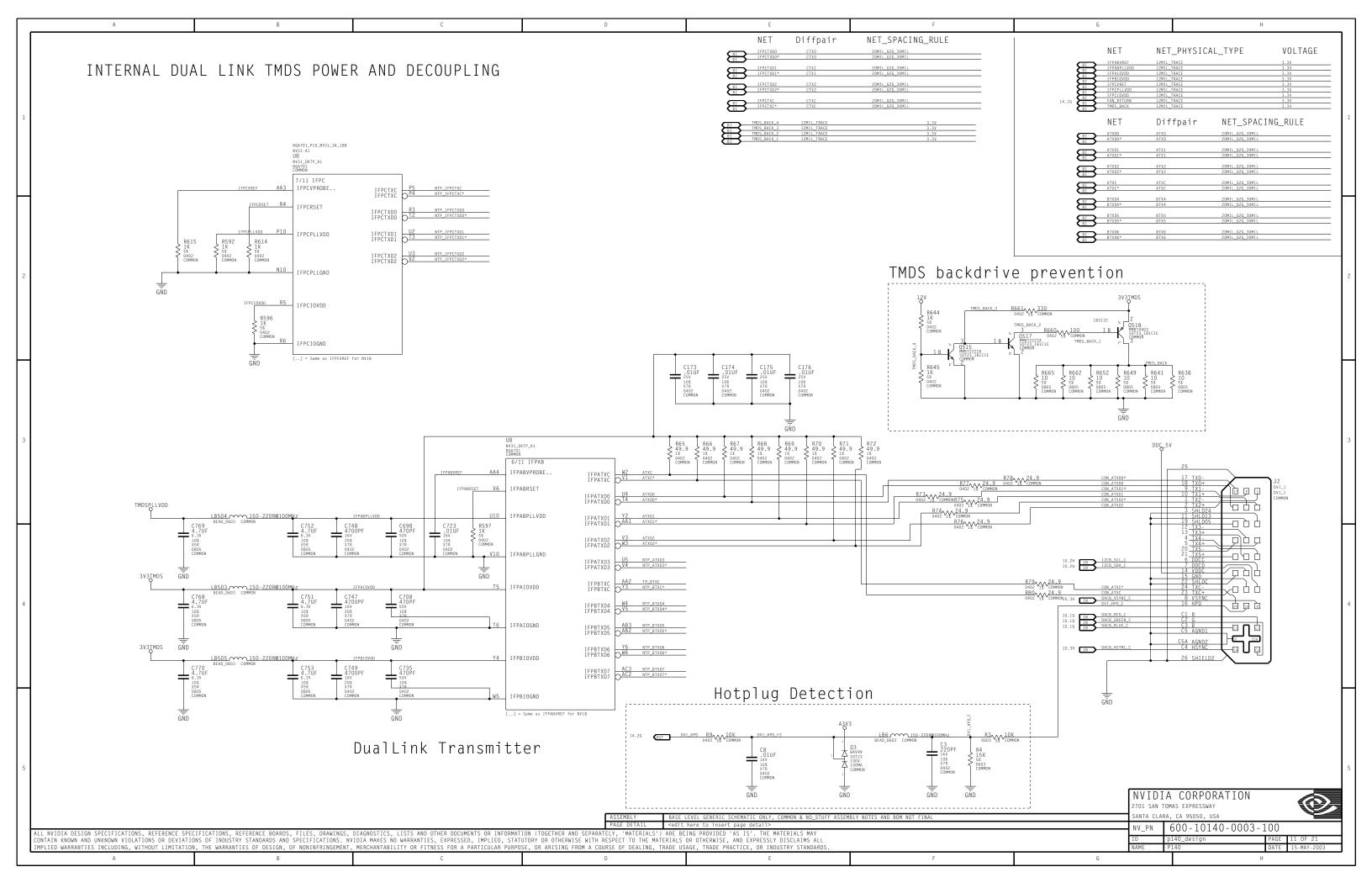


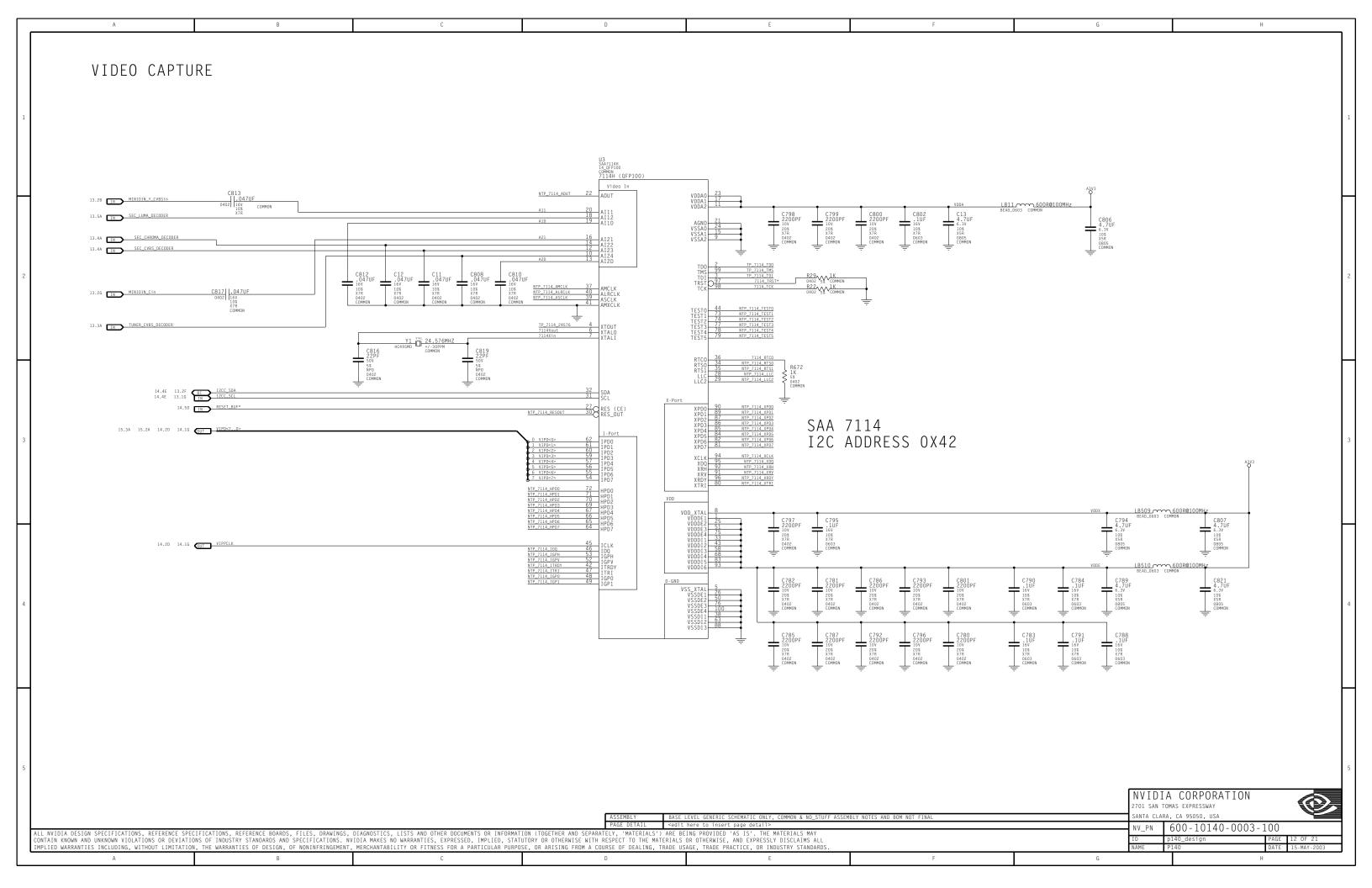


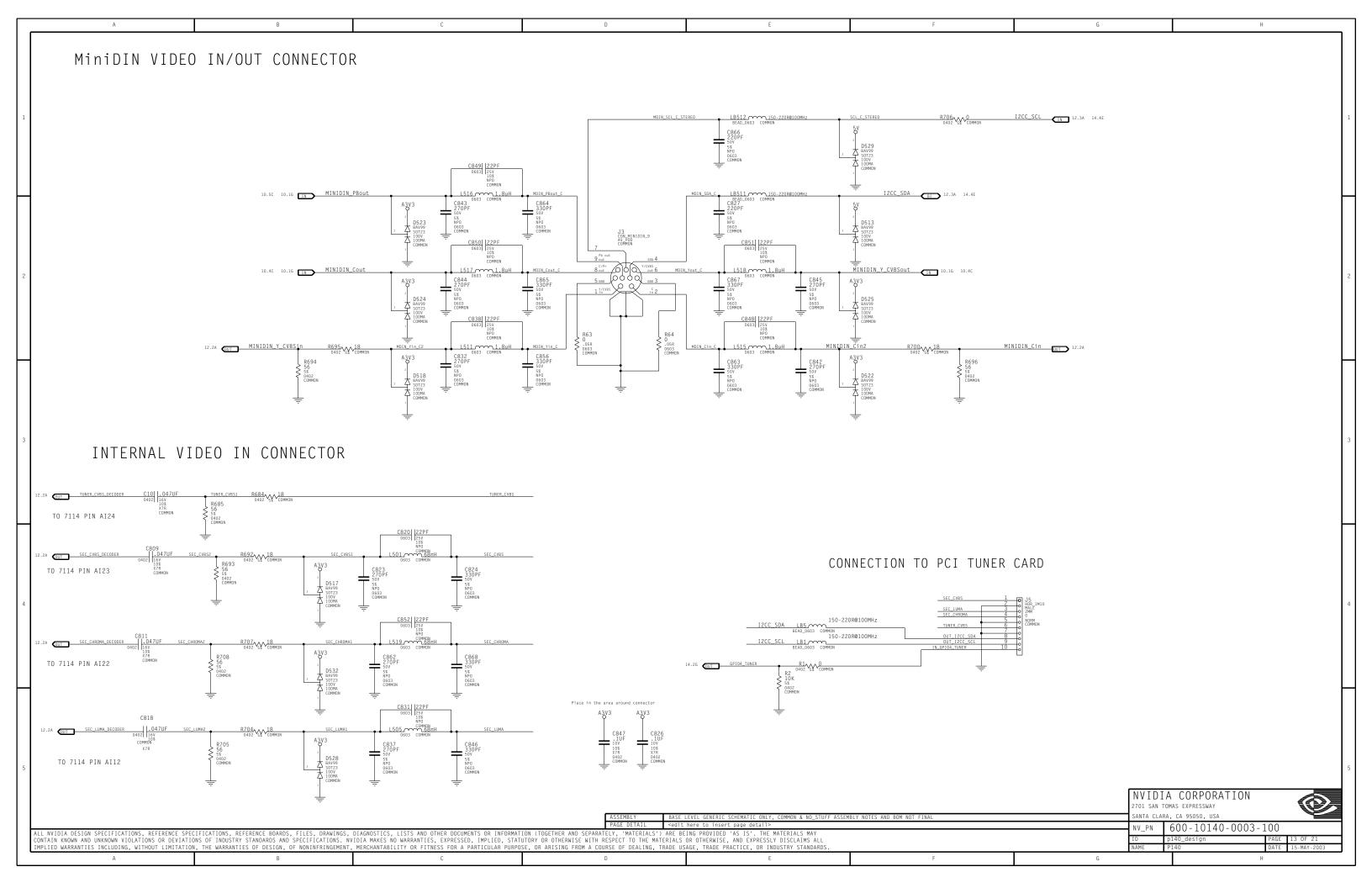


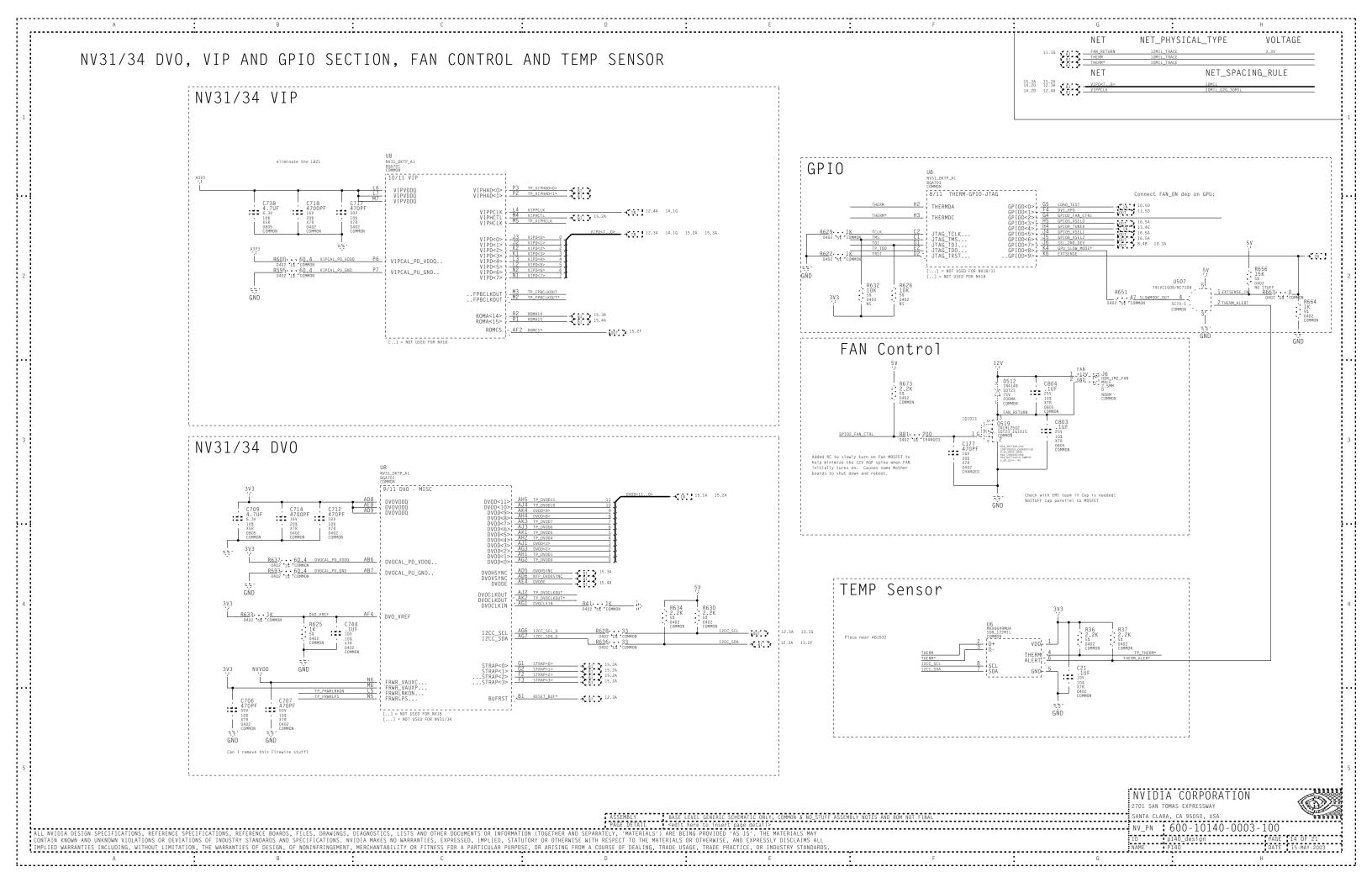


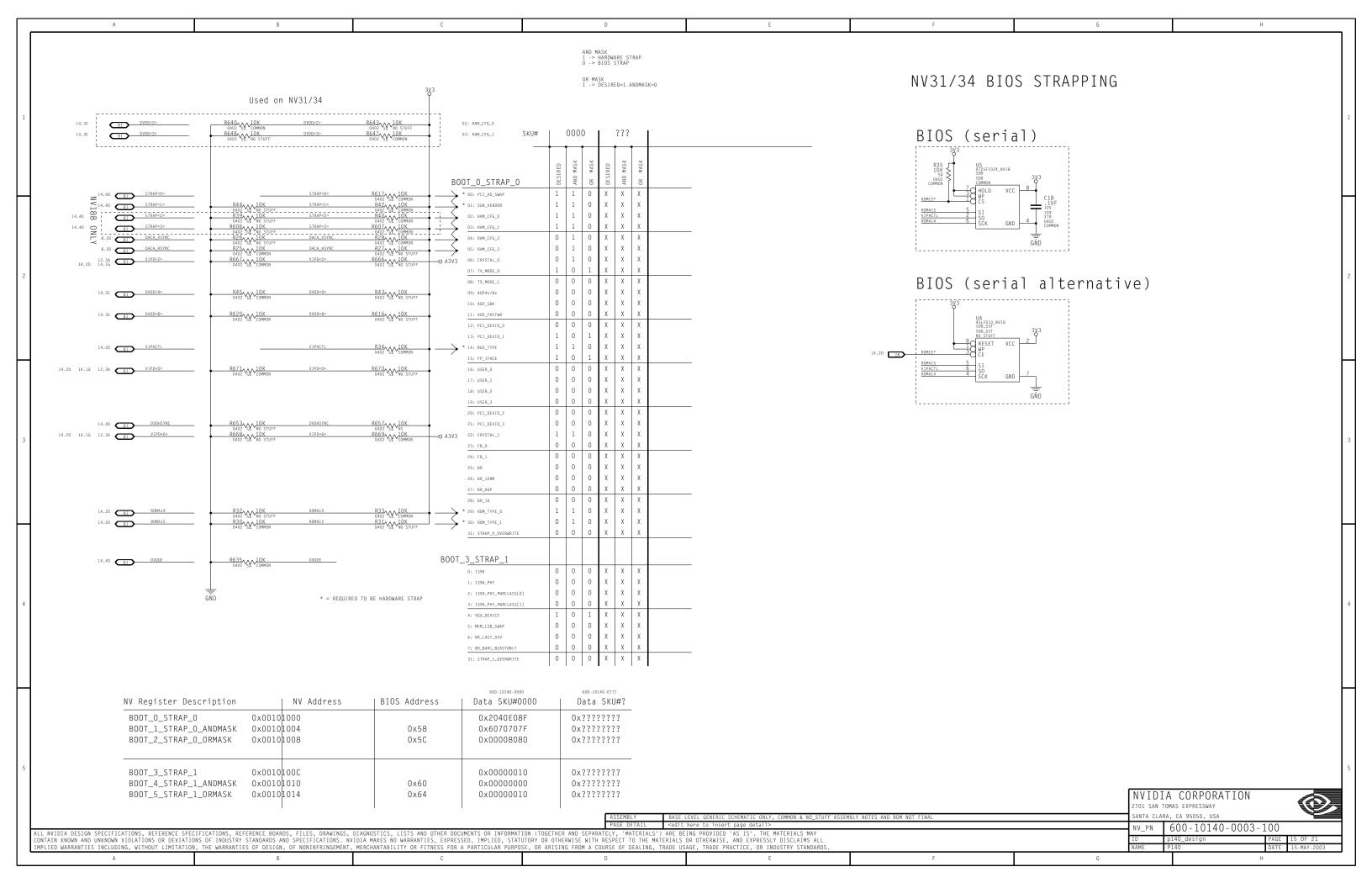


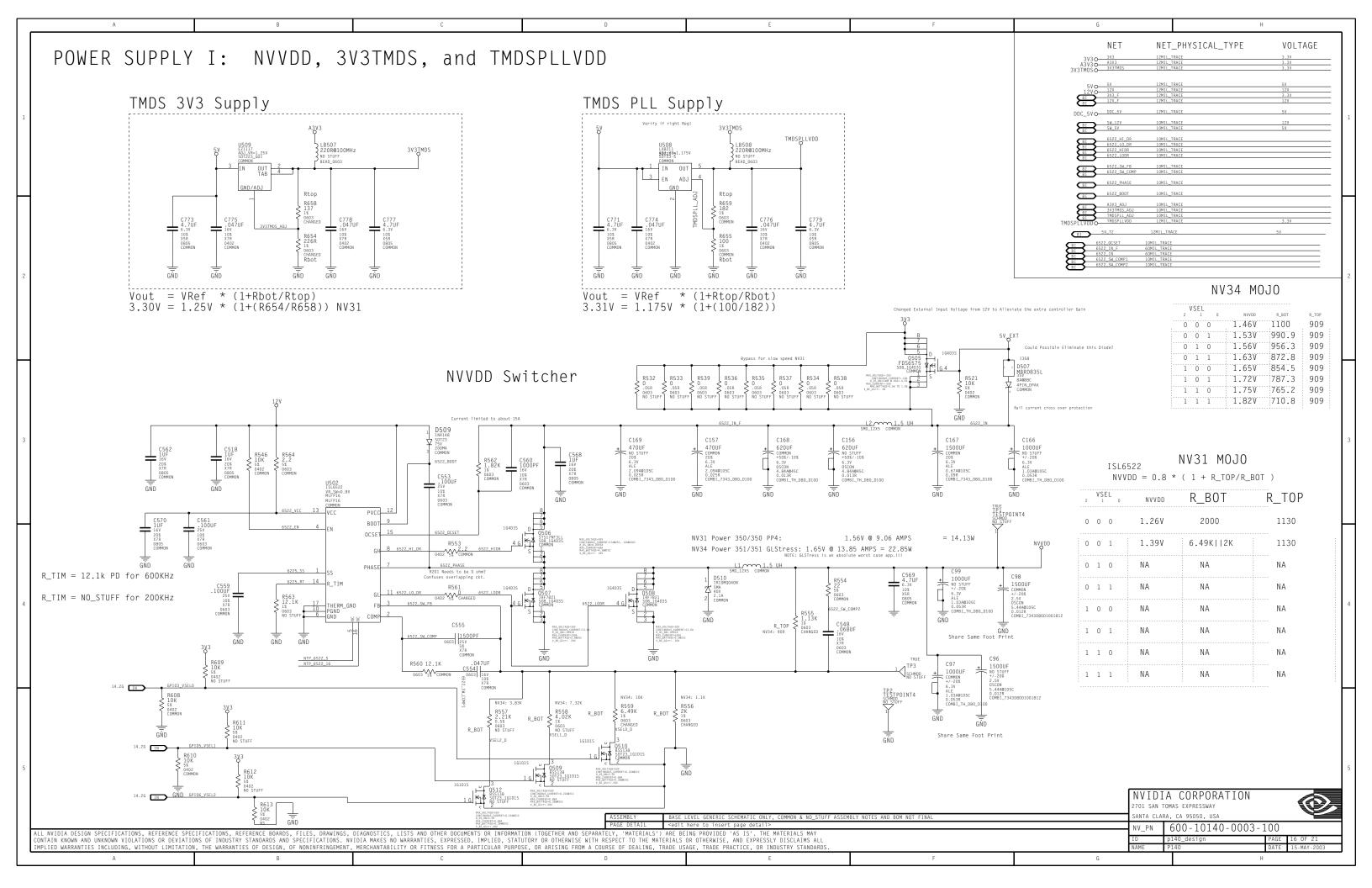


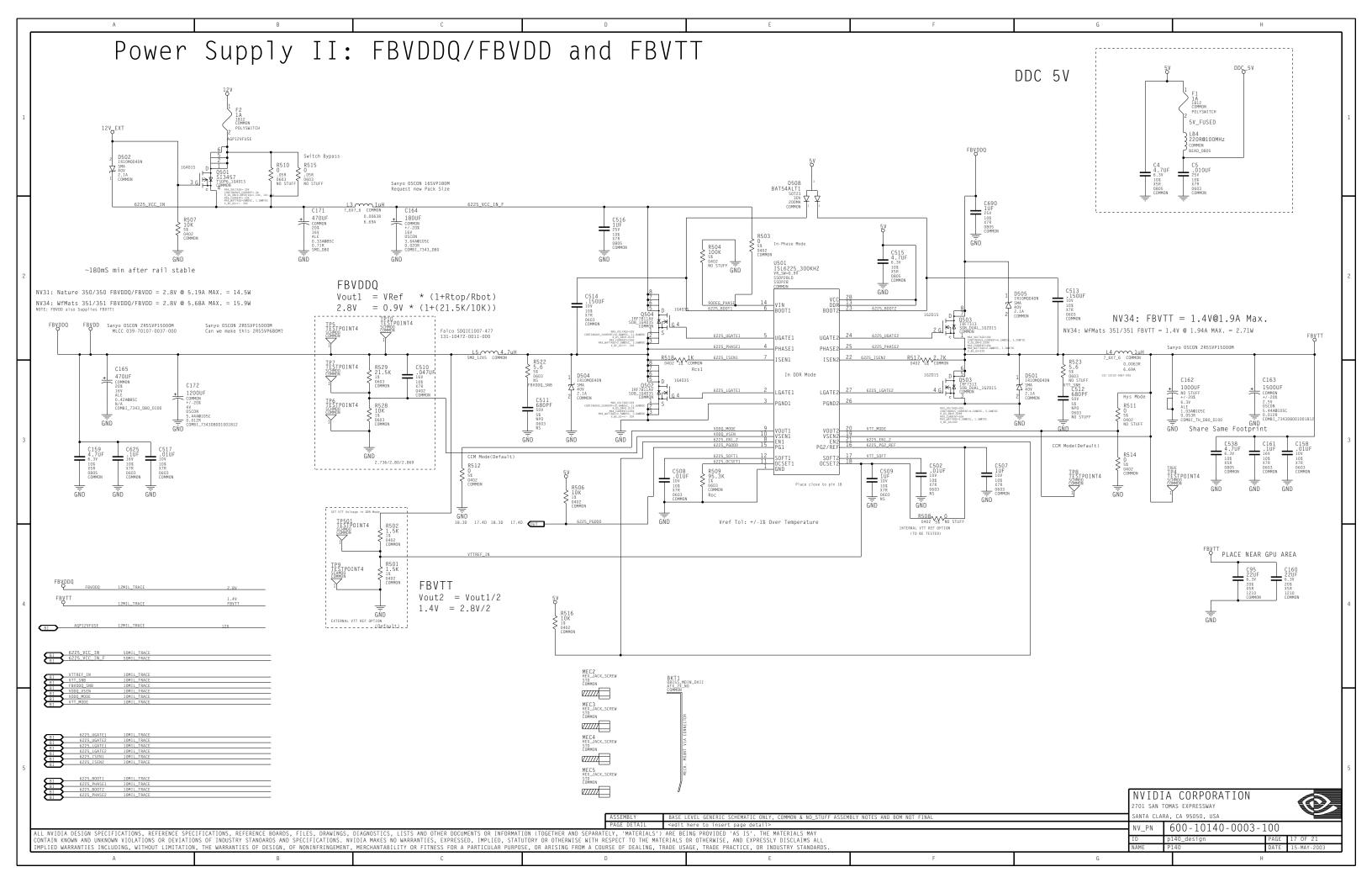


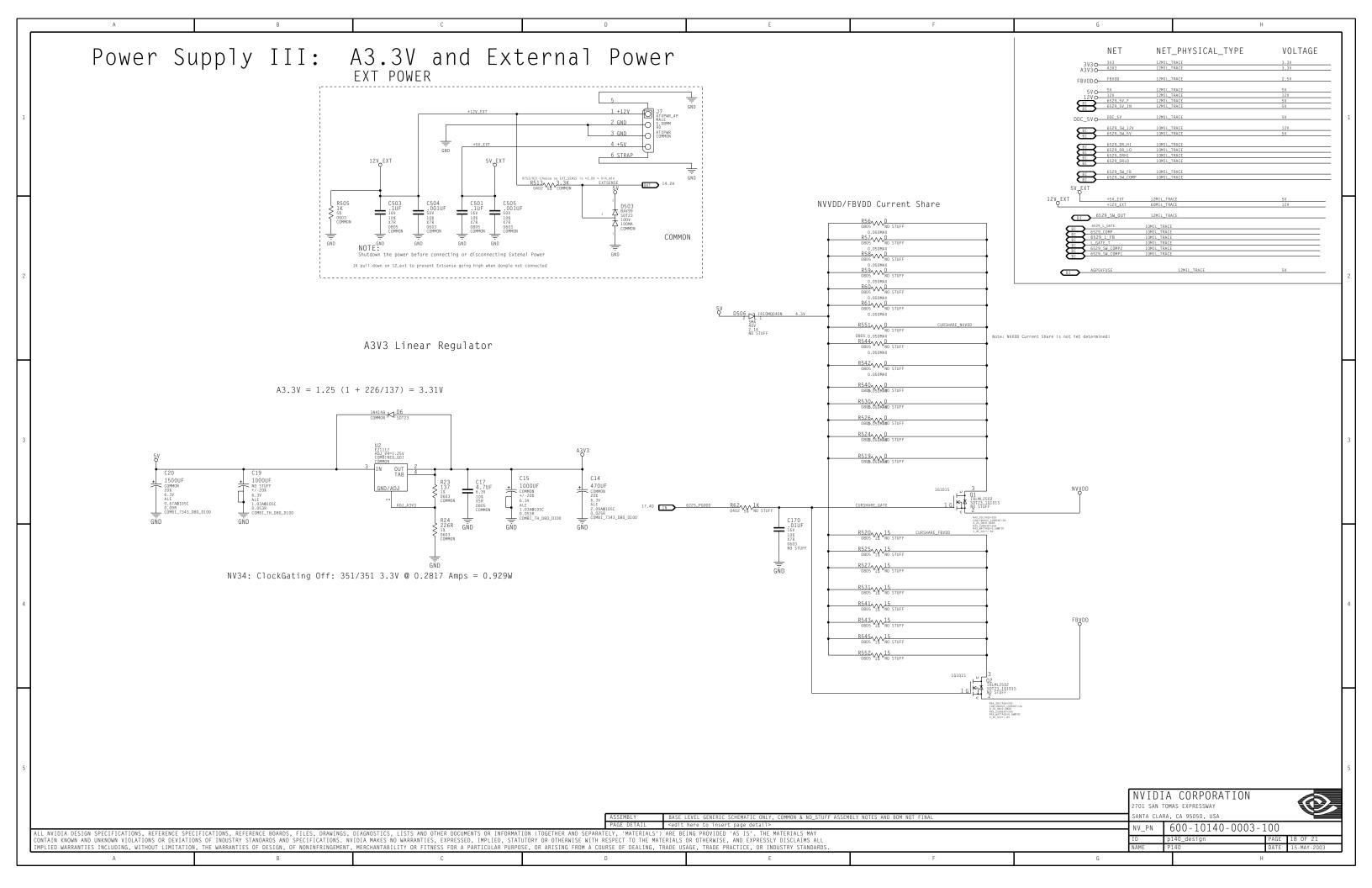














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