

POWER FLOW

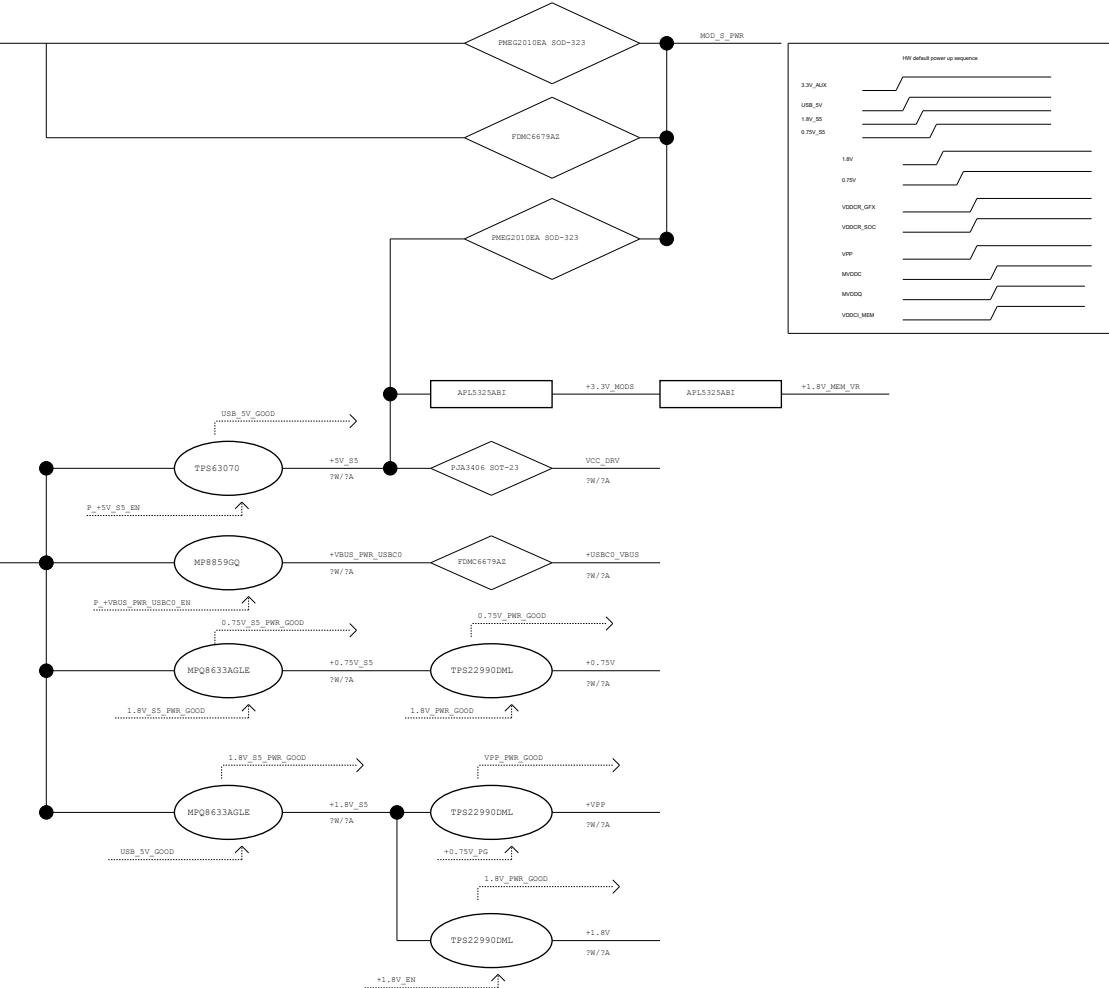
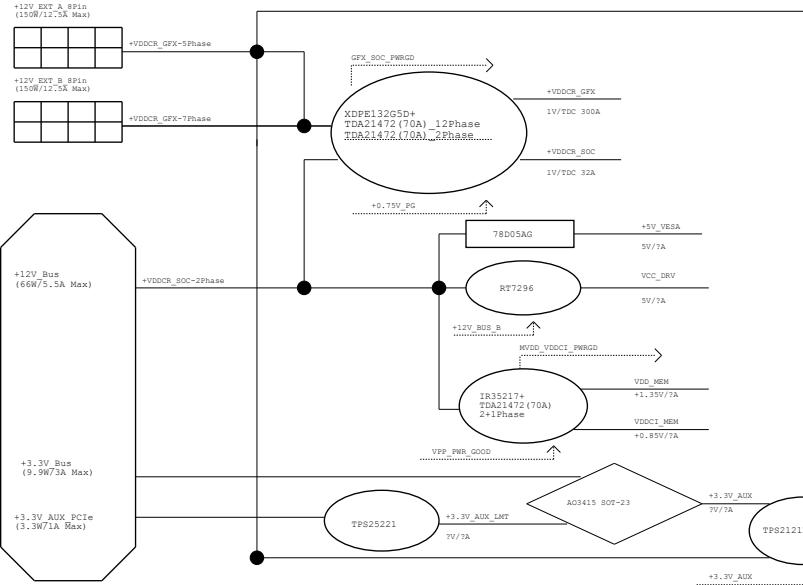
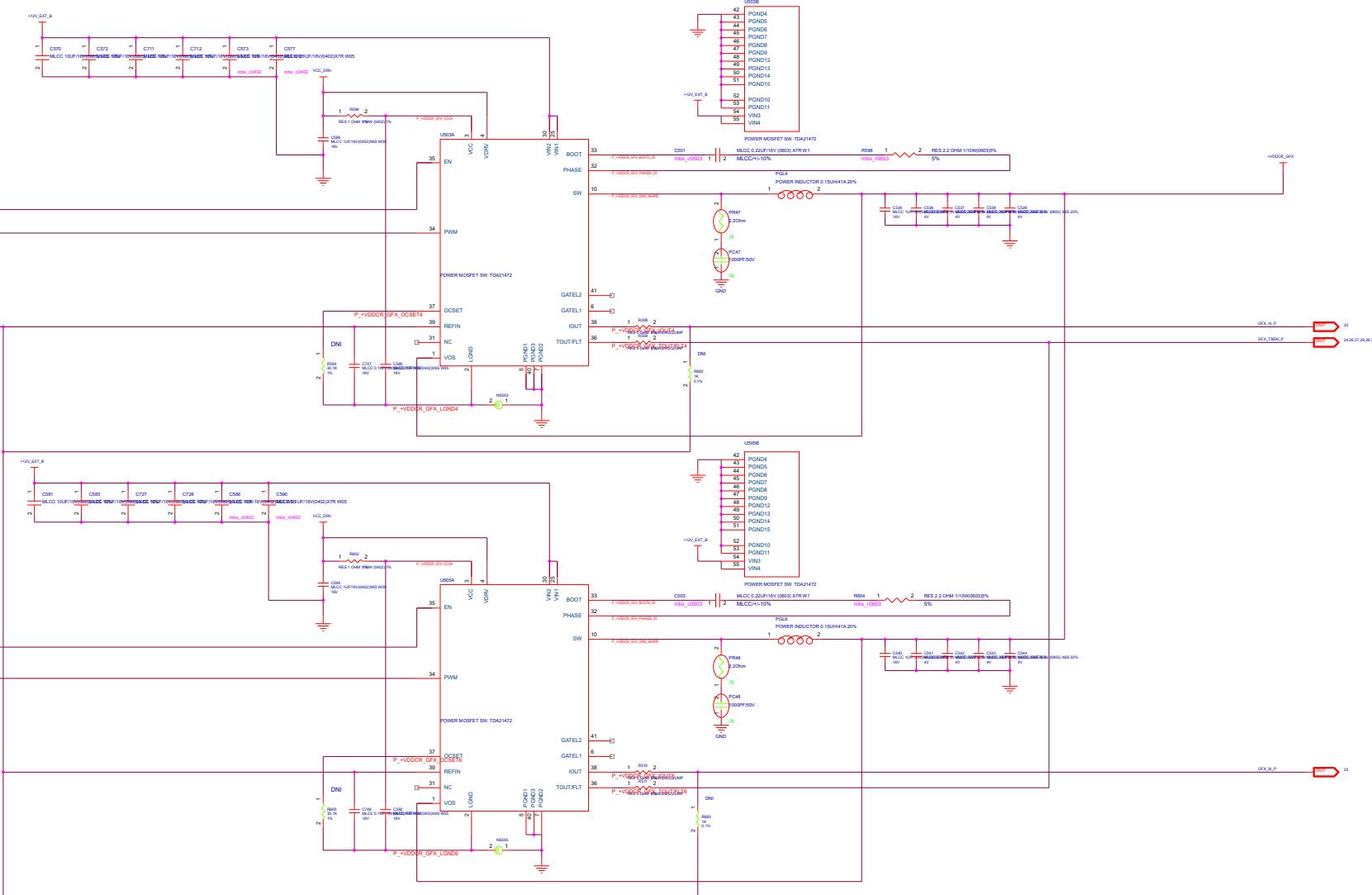
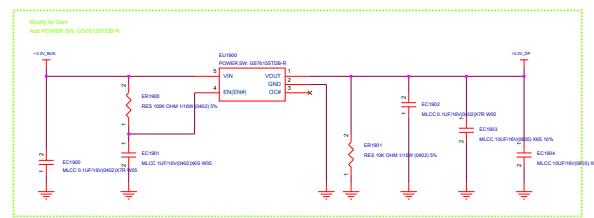
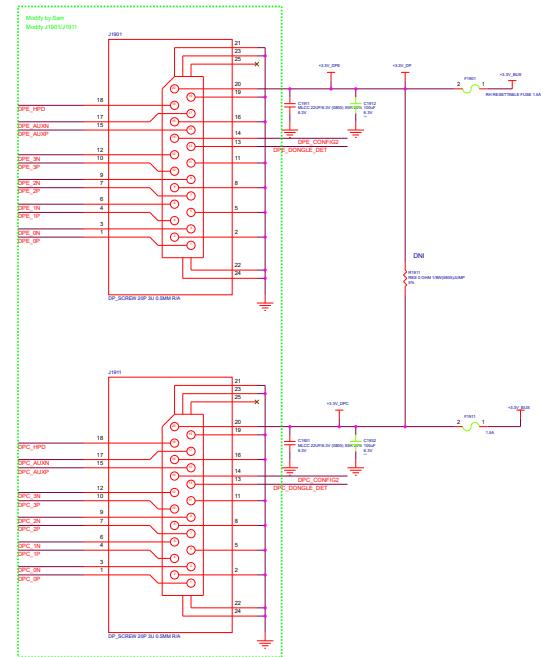
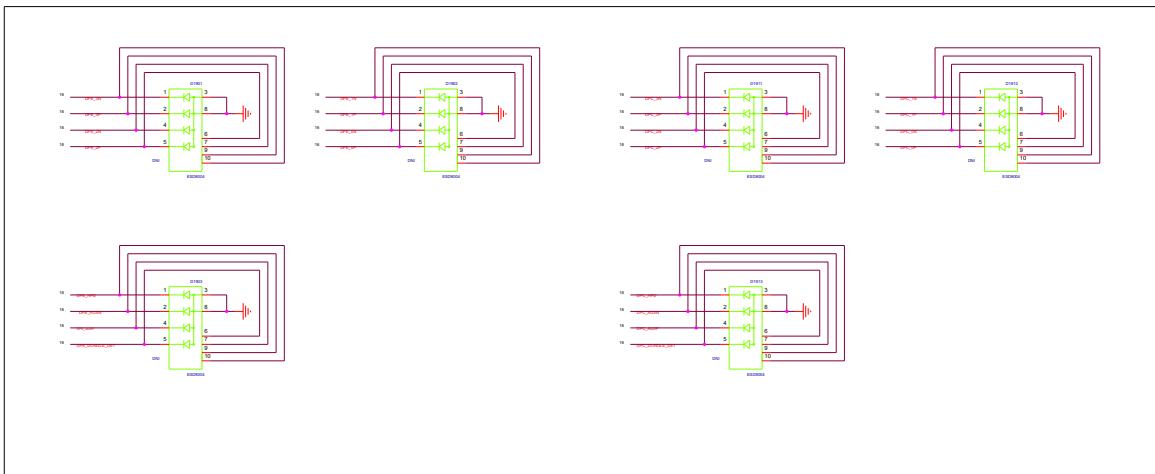
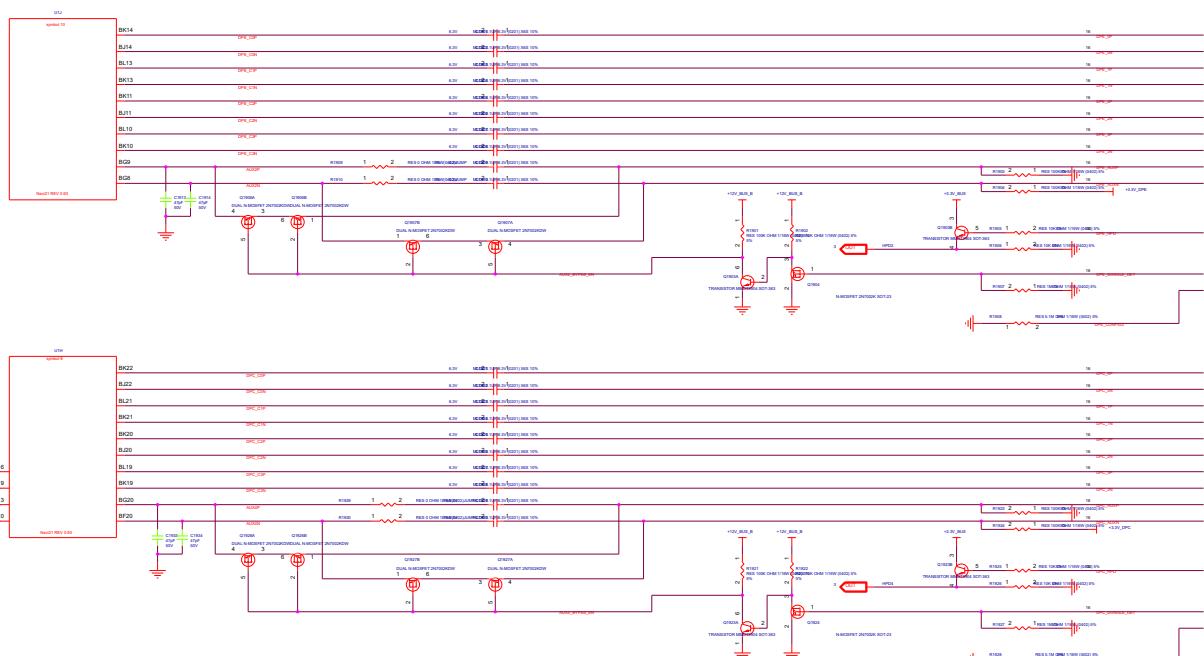
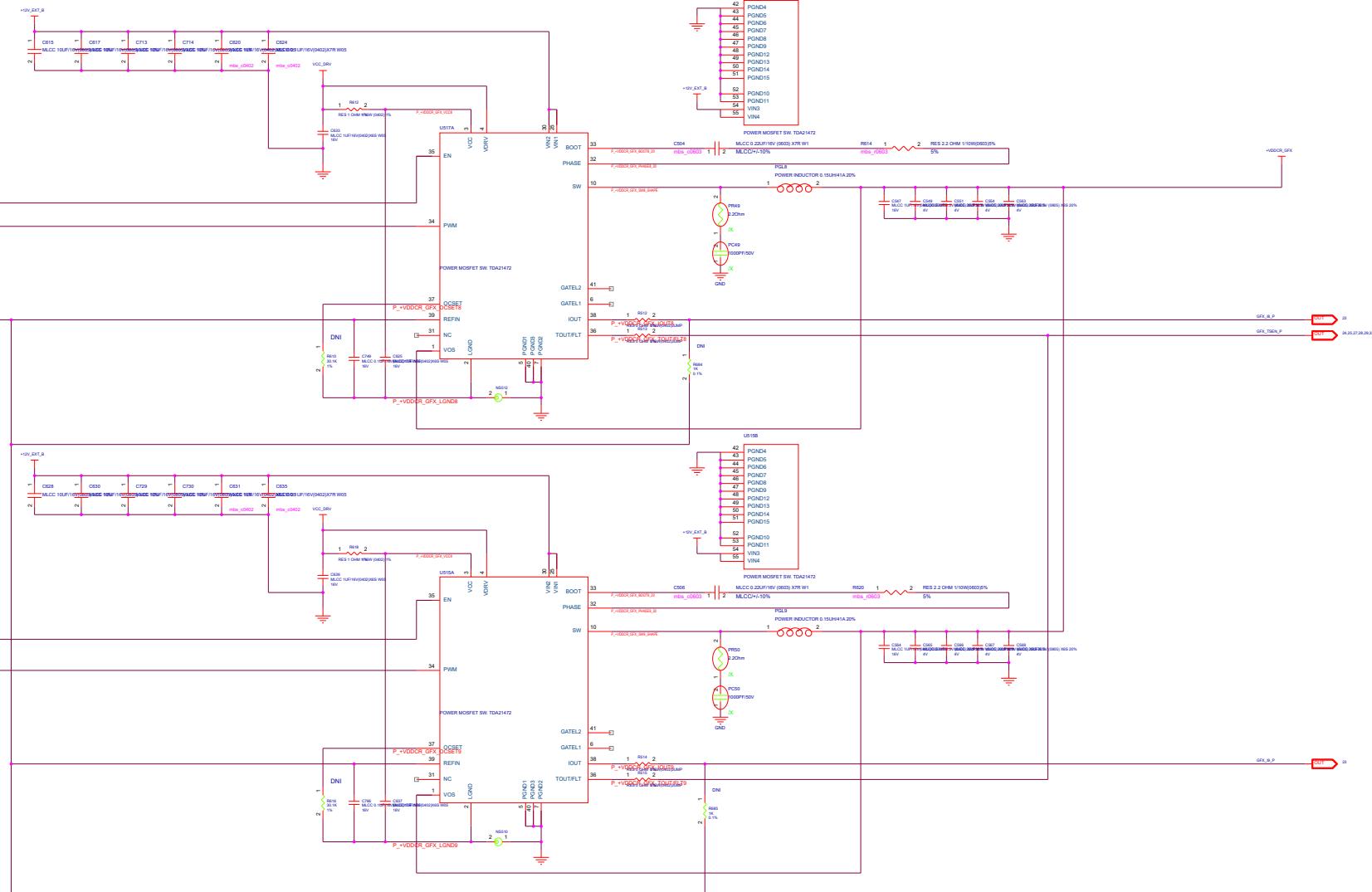


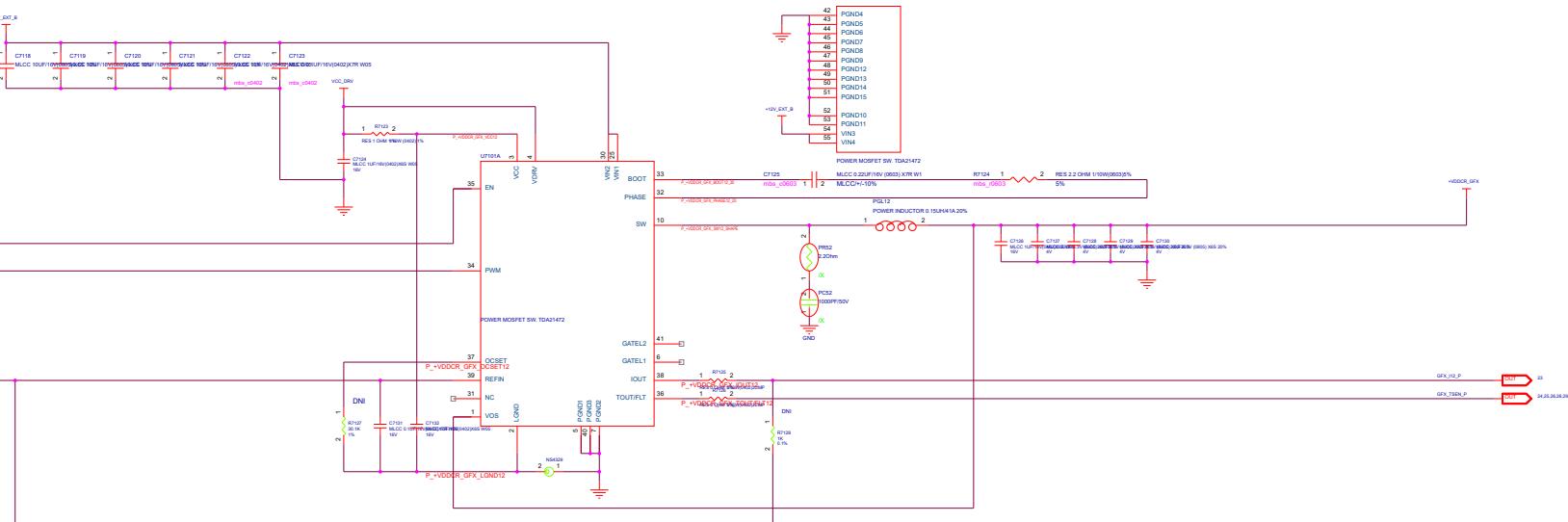
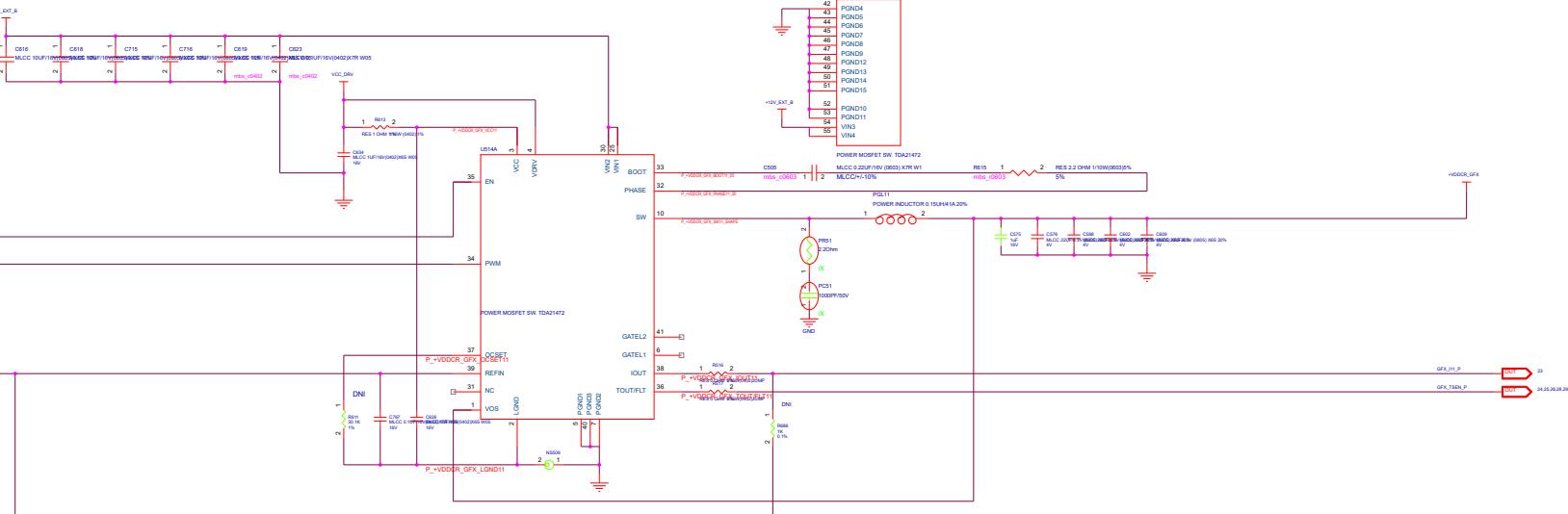
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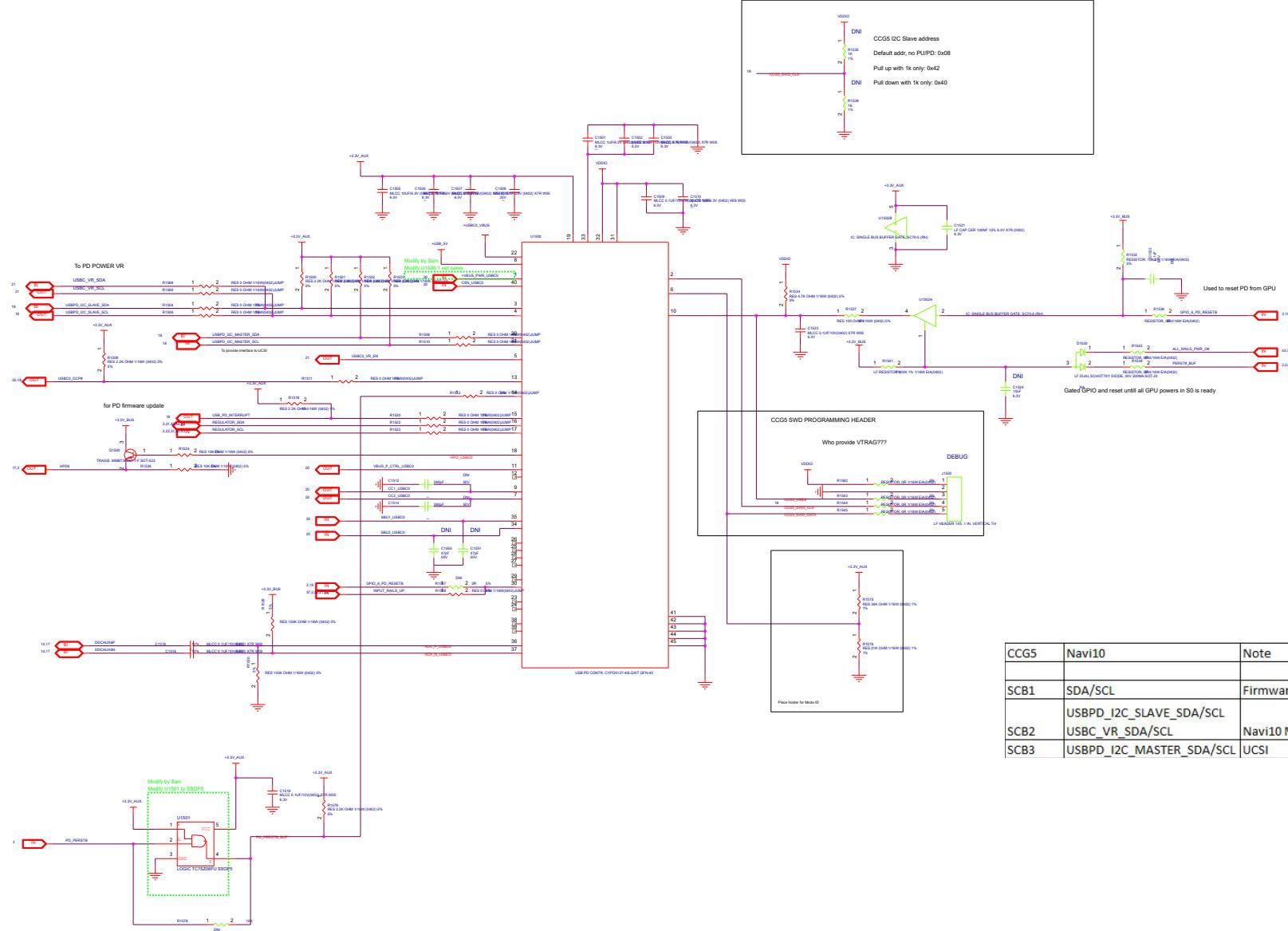
SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	GFX PHASES 8&9
2	NAVI 21 - PCIe Interface	27	GFX PHASES 11
3	NAVI 21 - GPIOs	28	GFX PHASES 5&7
4	NAVI 21 XTAL	29	GFX PHASES 3&10
5	XGMI	30	SOC PHASE 1&2
6	NAVI 21 MEM CH AB	31	VDD_MEM & VDDCI CONTROLLER
7	NAVI 21 MEM CH CD	32	VDD_MEM PHASES 1&2
8	NAVI 21 MEM CH EF	33	VDDCI_MEM PHASE 1
9	NAVI 21 MEM CH GH	34	NAVI 21 DECAPS
10	GDDR6 MEM CH CD	35	NAVI 21 POWER
11	GDDR6 MEM CH EF	36	NAVI 21_POWER and GND
12	GDDR6 MEM CH GH	37	POWER_MANAGEMENT
13	GDDR6 MEM CH AB	38	ClampWA
14	NAV121 TMDDPA - USB-C	39	SVI2 & BxMACO
15	NAV121 TMDDP - HDMI	40	THERMAL
16	NAV121 TMDDPC&E - DP	41	DPM_Status_LED & GDDR6_JTAG
17	NAV121 TMDDPA	42	Pi Debug
18	NAV121 USB	43	DEBUG
19	PD Controller	44	History
20	USB-C PORT 1		
21	USB_5V_1.8V_0.75V		
22	MODS CONTROL & POWER		
23	GFX & SOC CONTROLLER		
24	GFX PHASES 1&2		
25	GFX PHASES 4&6		

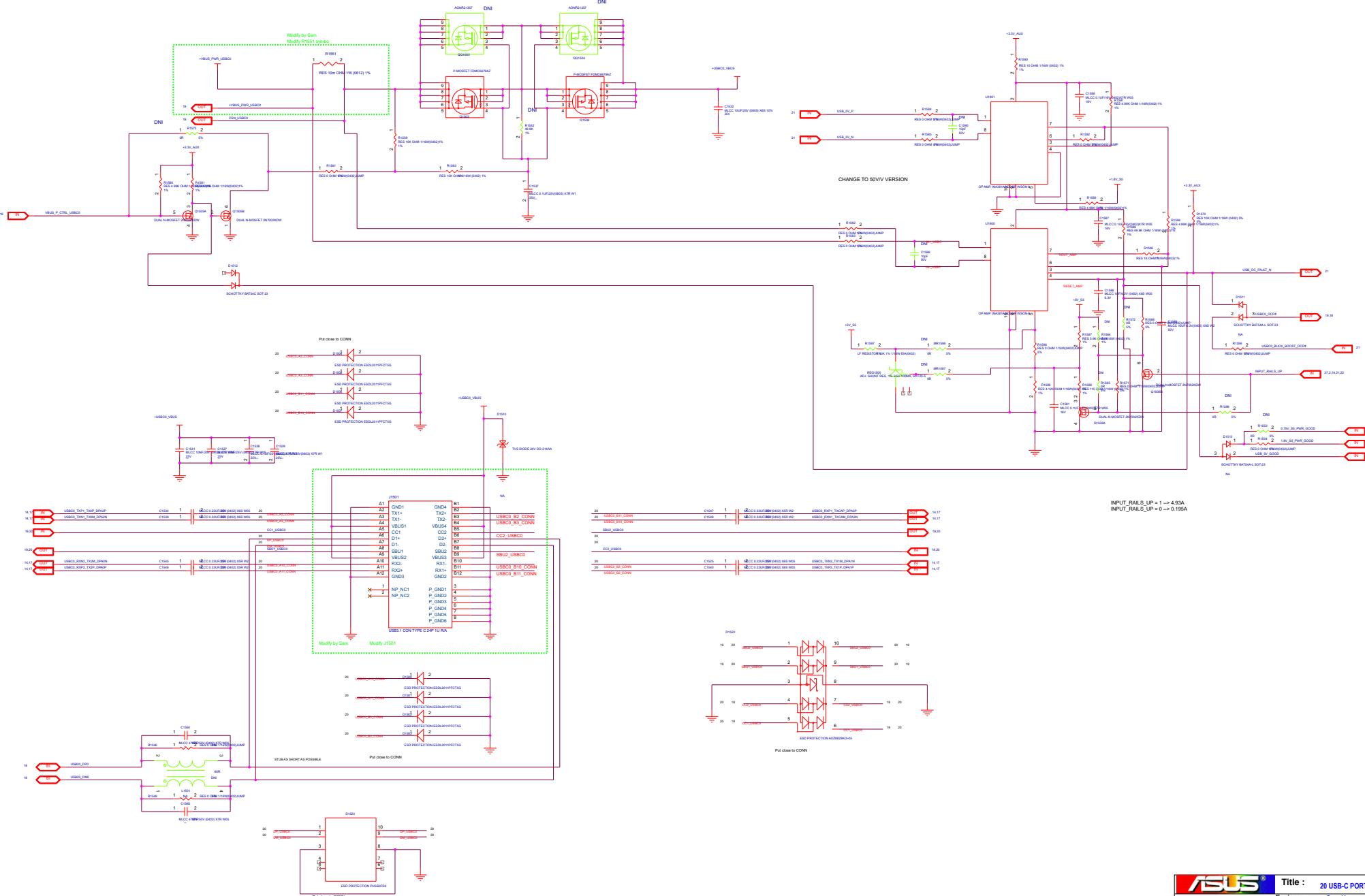


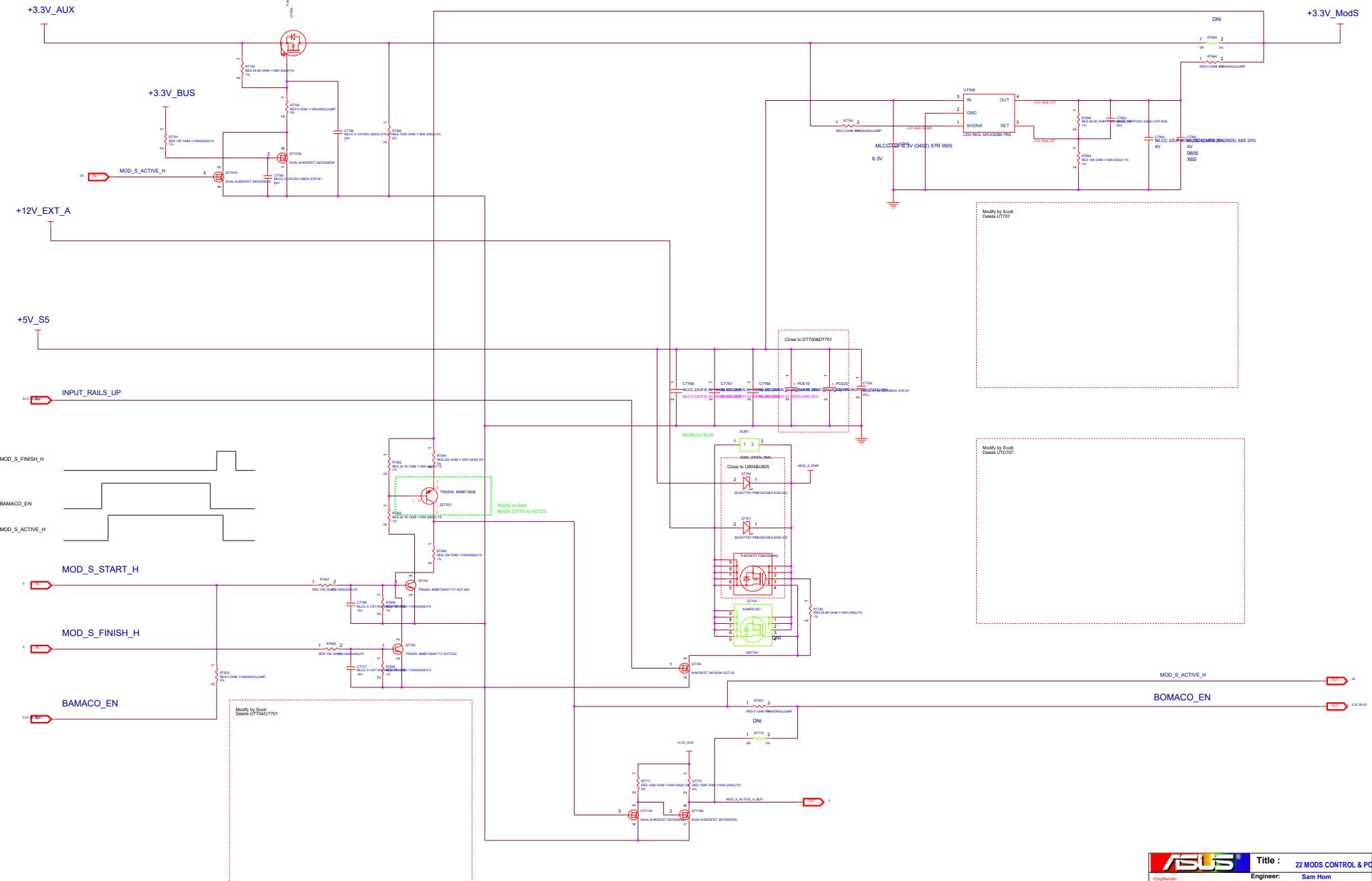


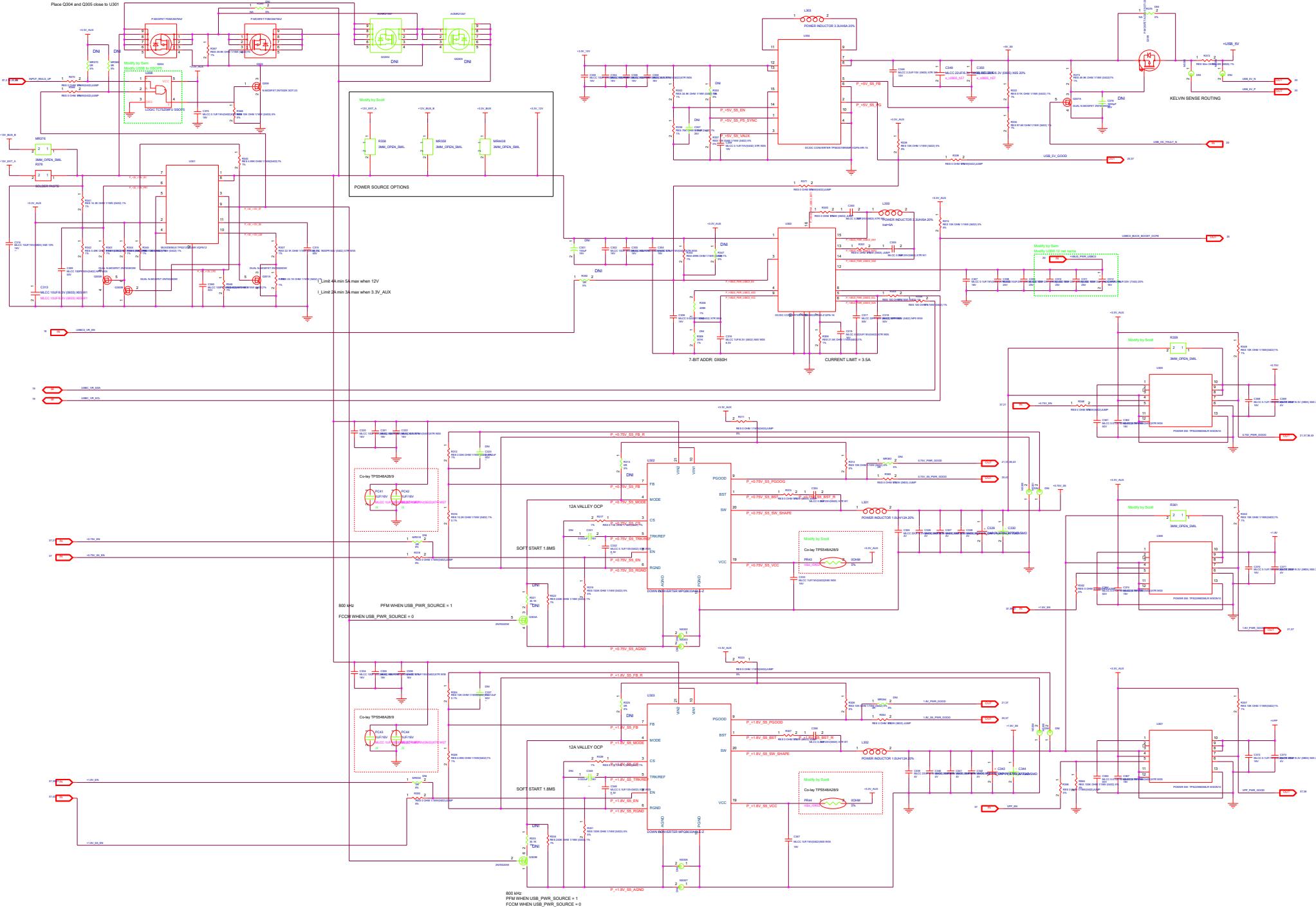


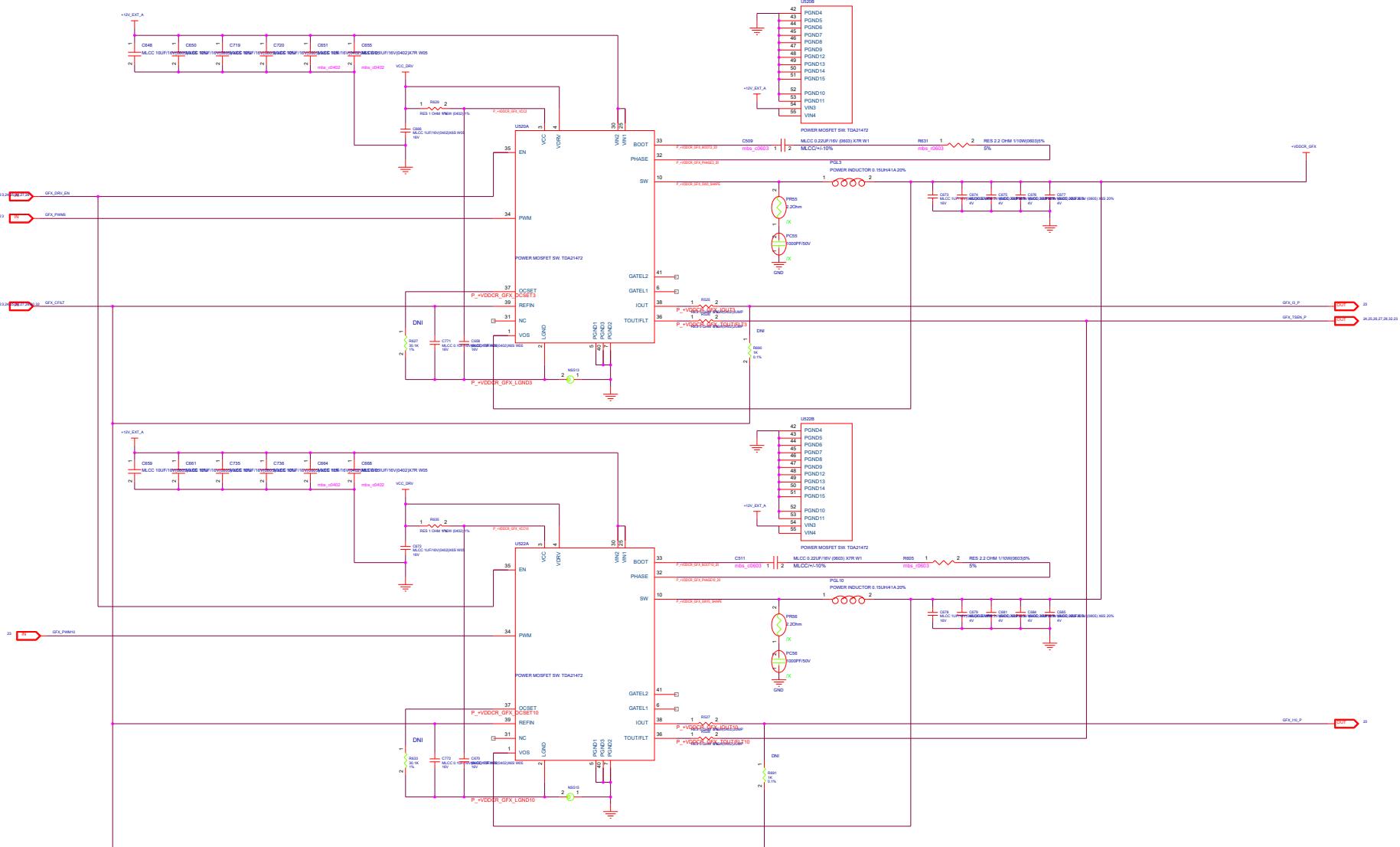




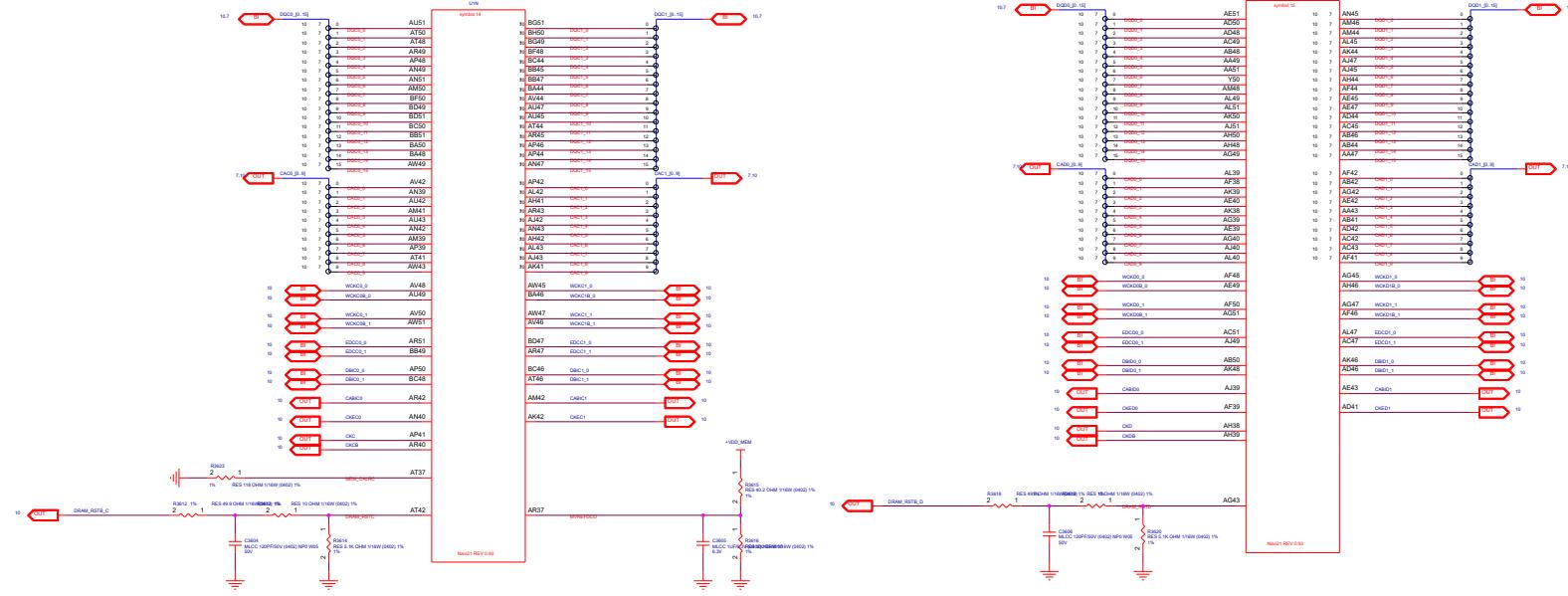


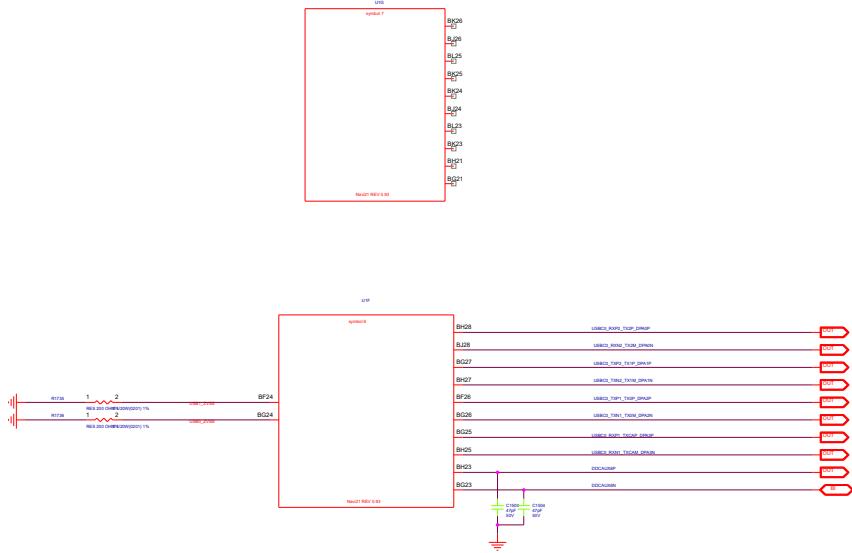


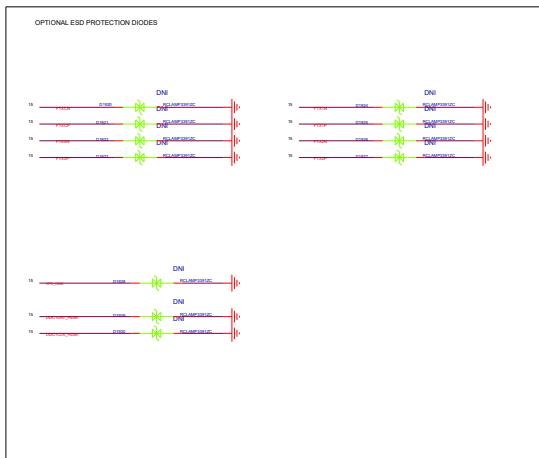
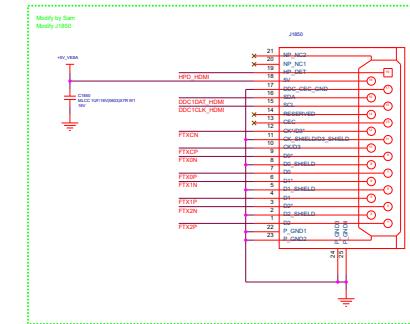
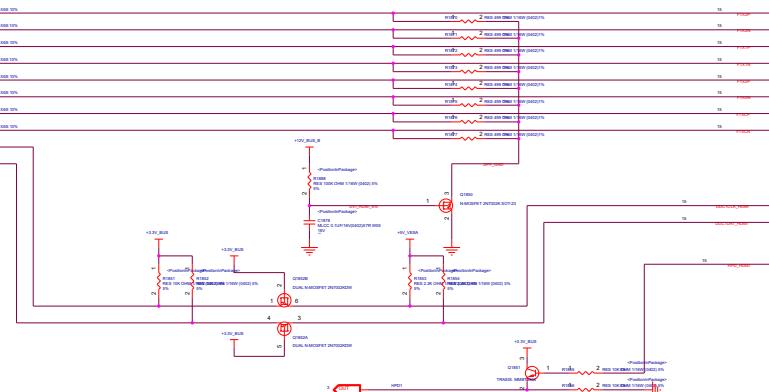


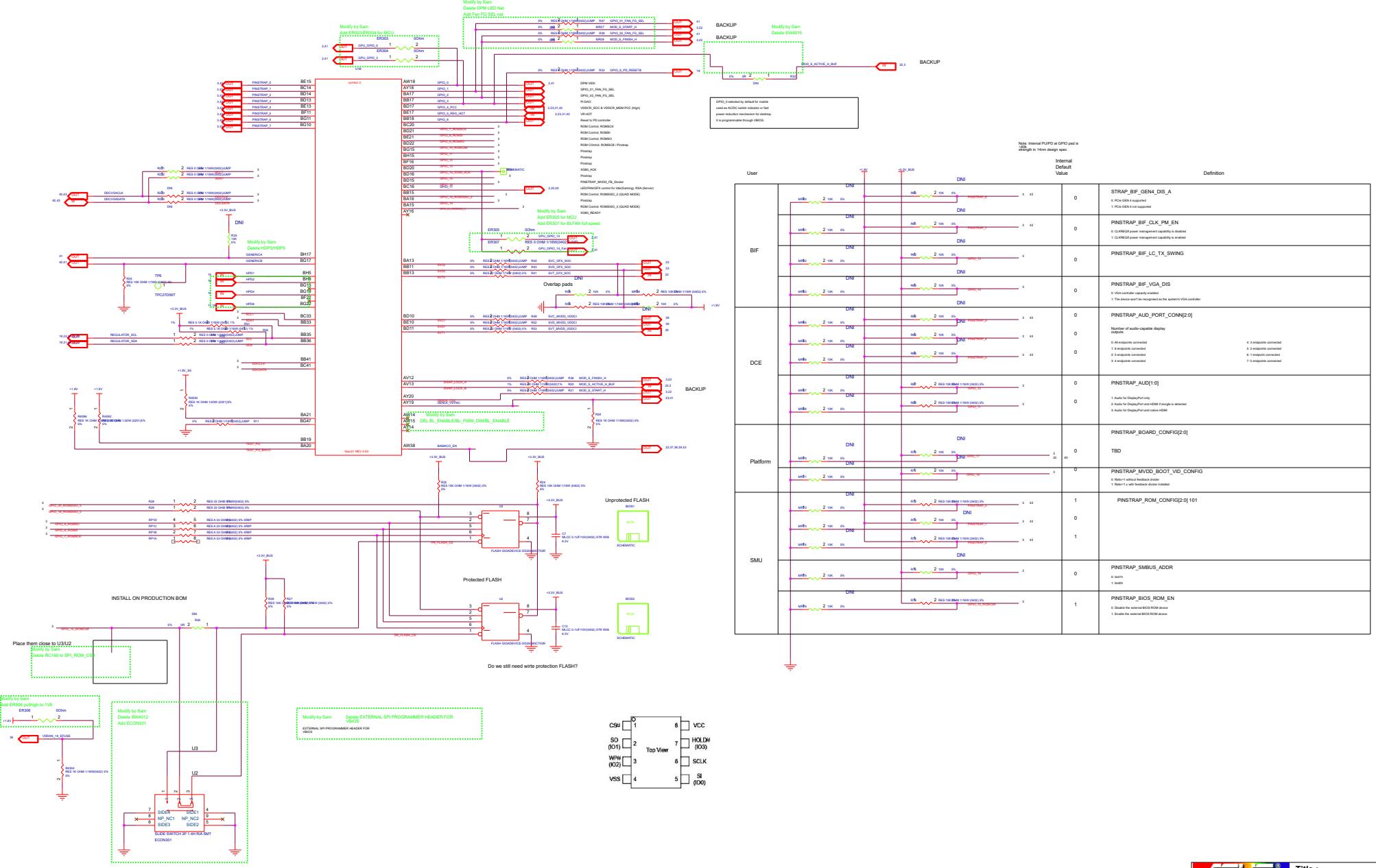


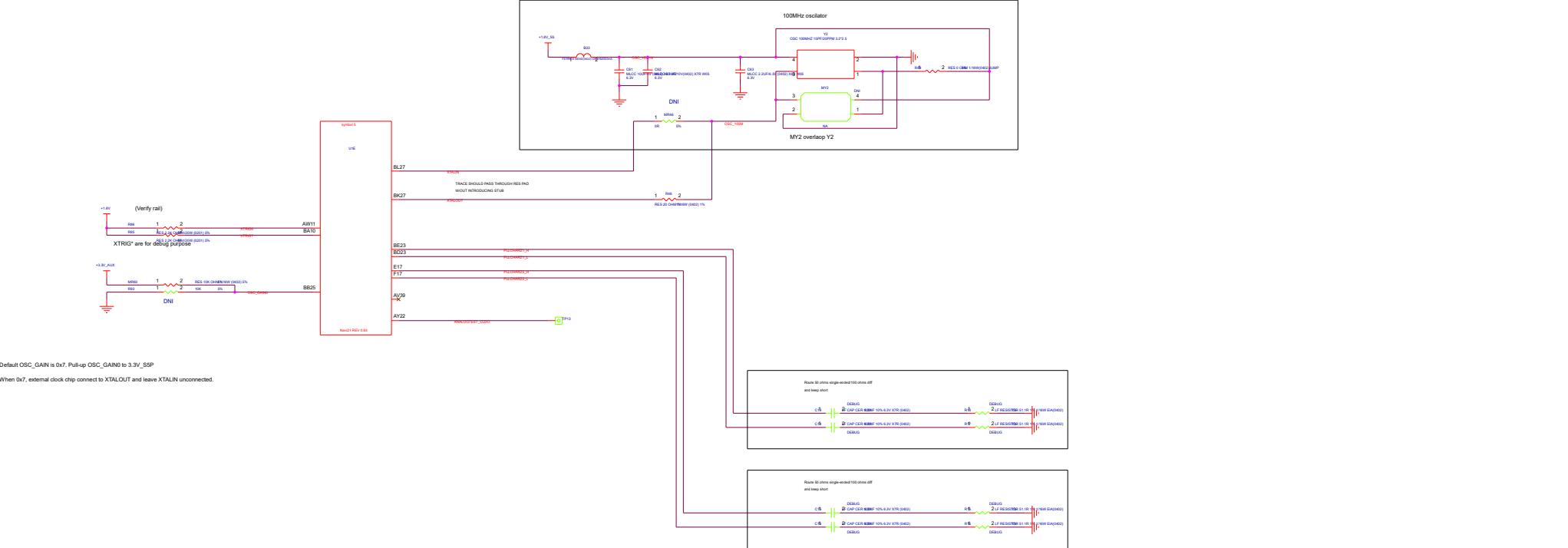


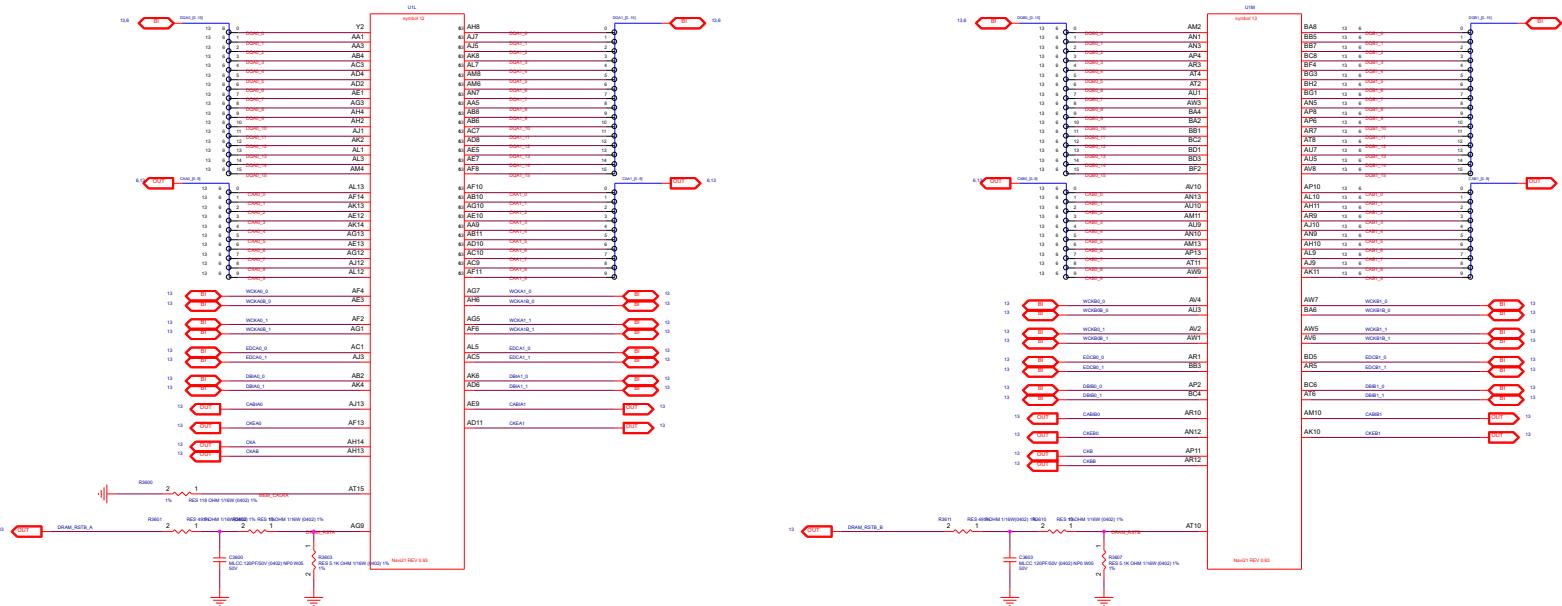


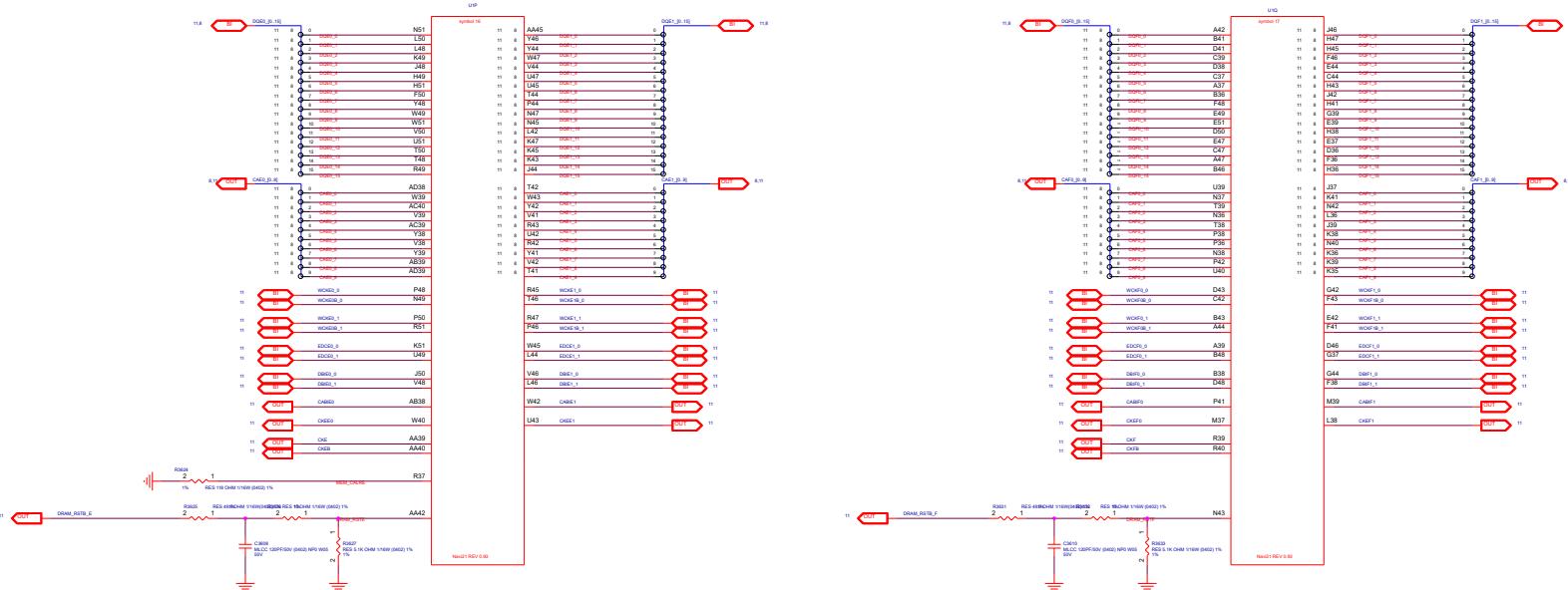


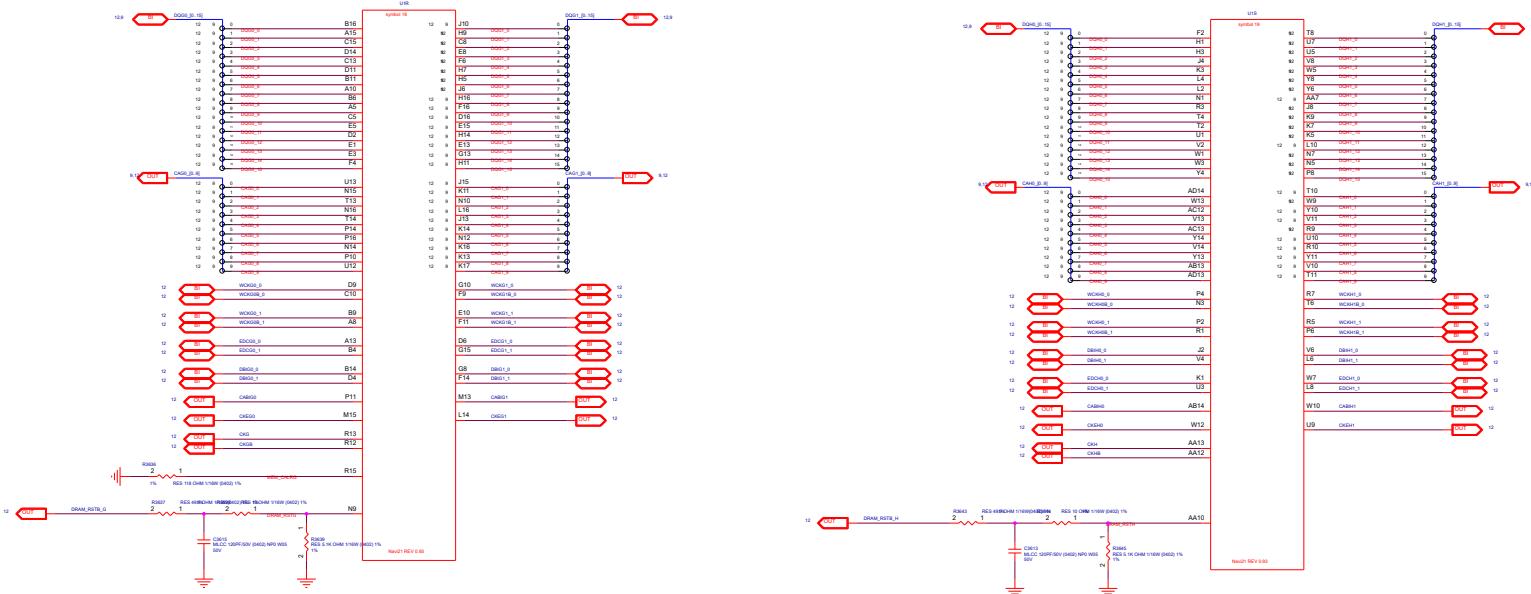




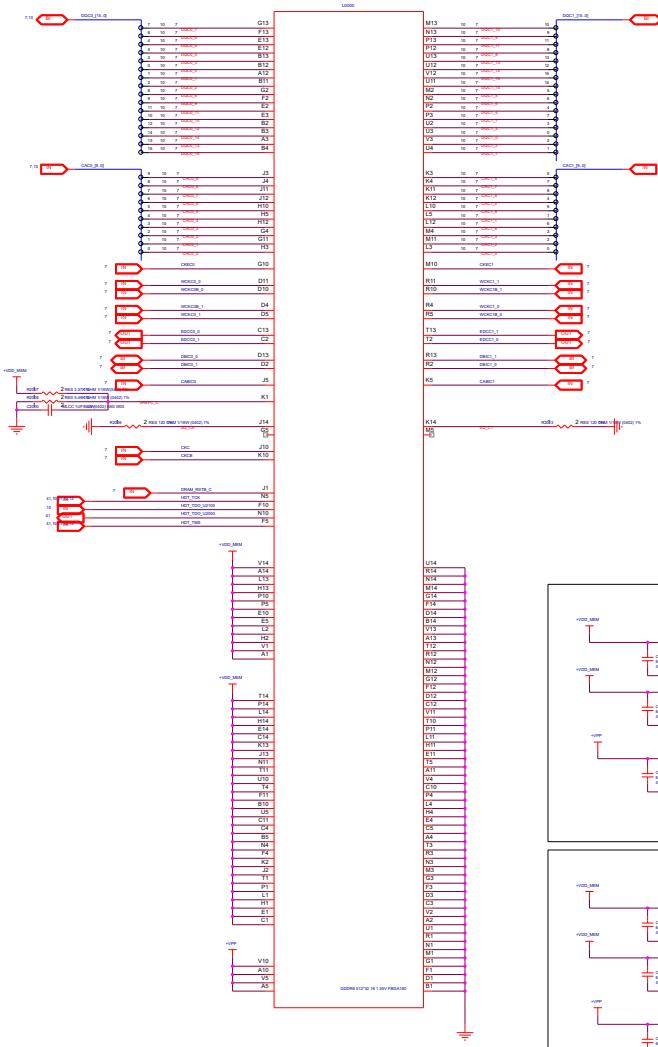




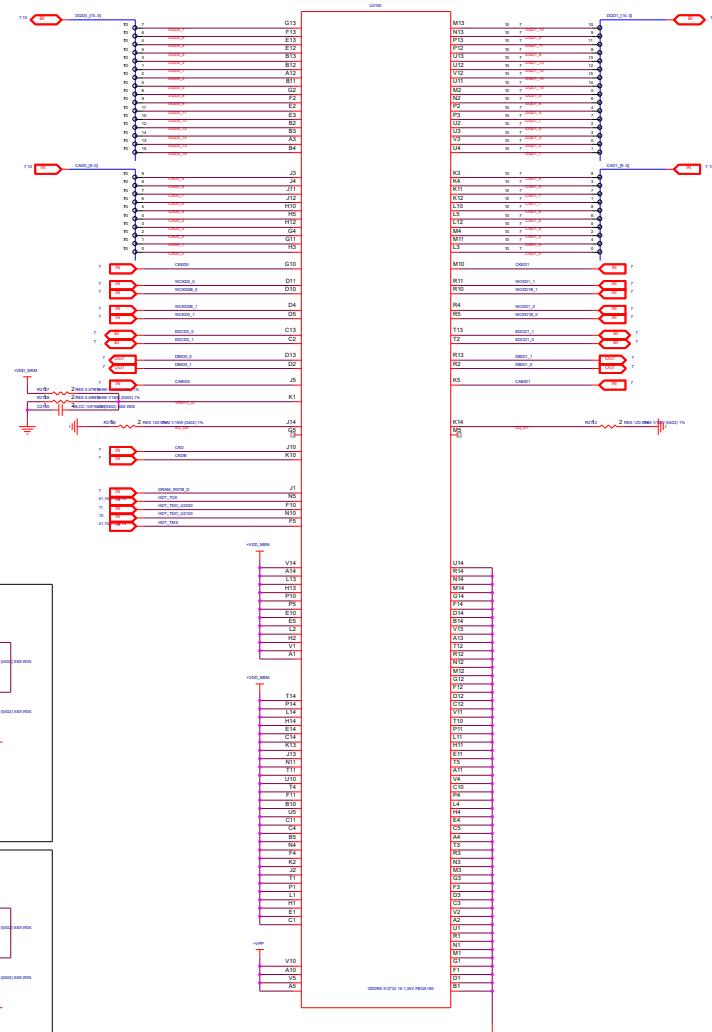


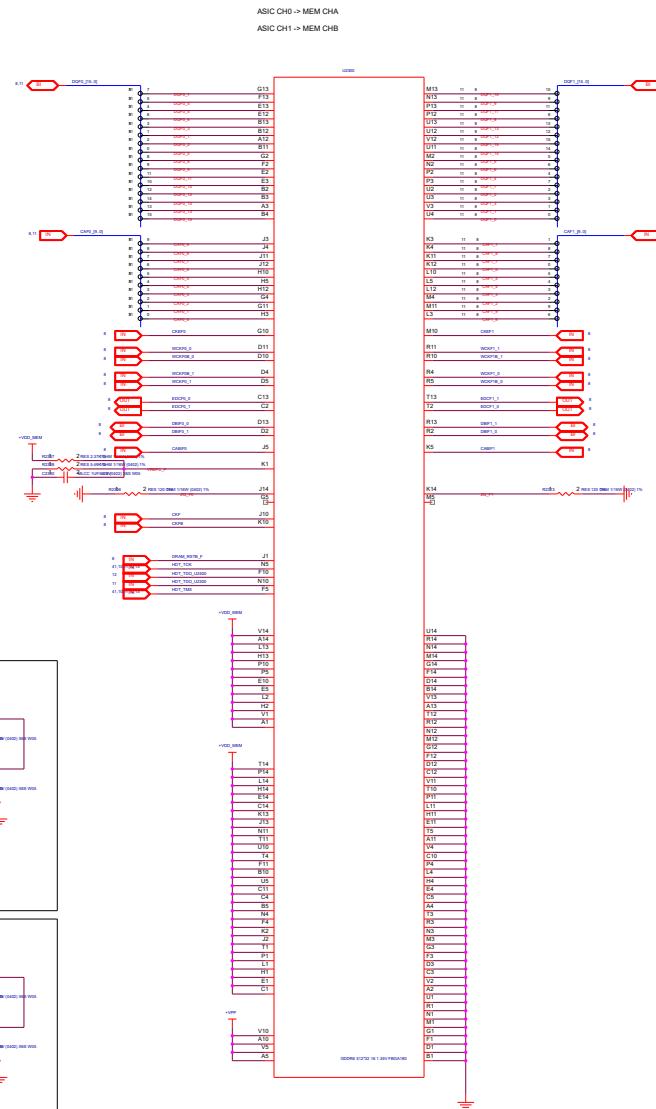
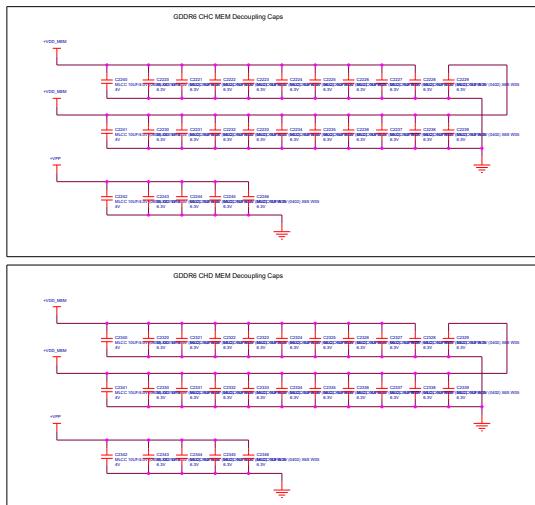
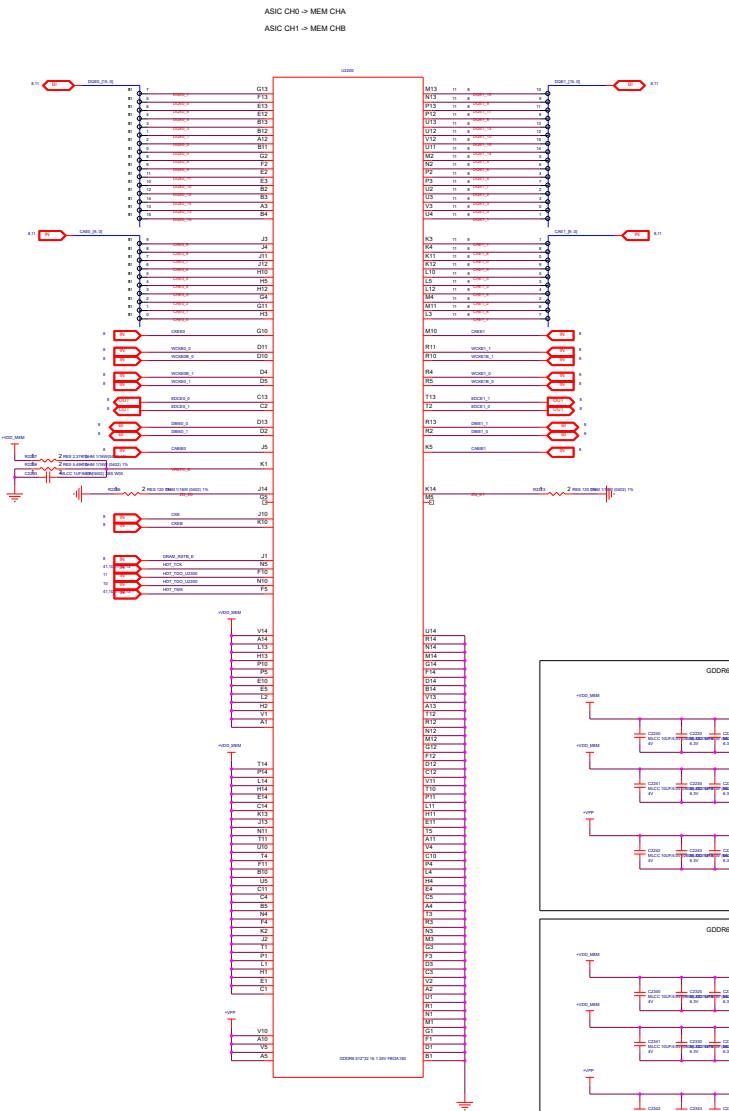


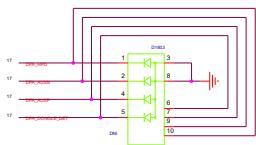
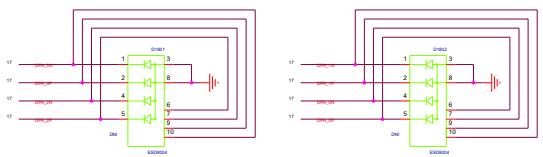
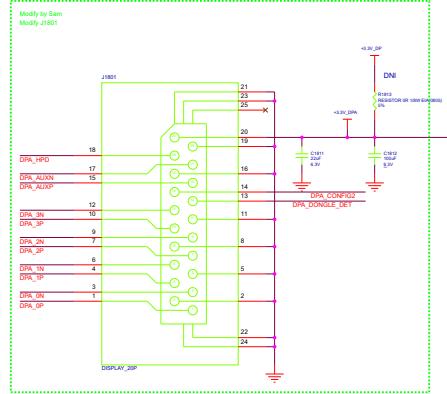
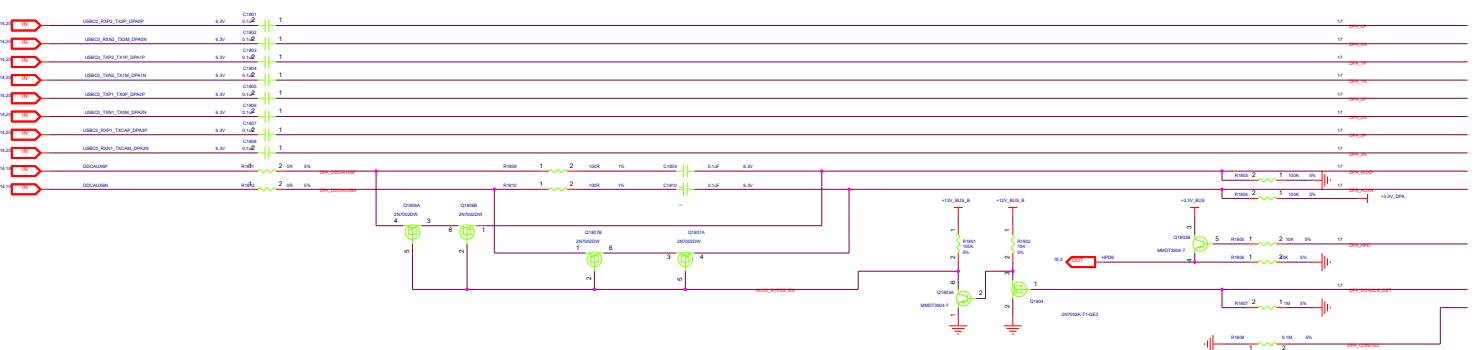
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ASIC CH1 -> MEM CHB

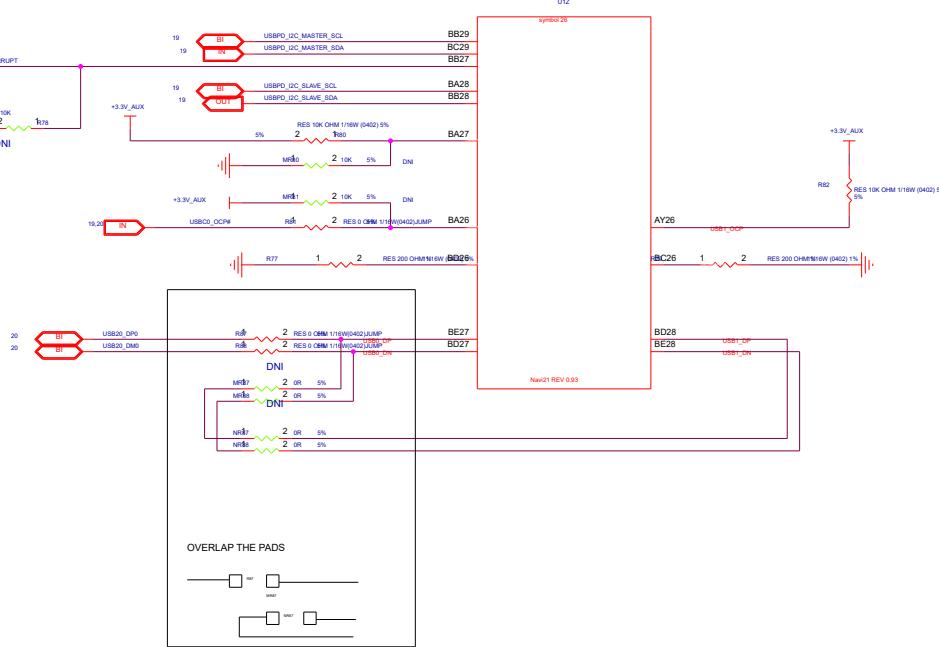


ASIC CH0 -> MEM C

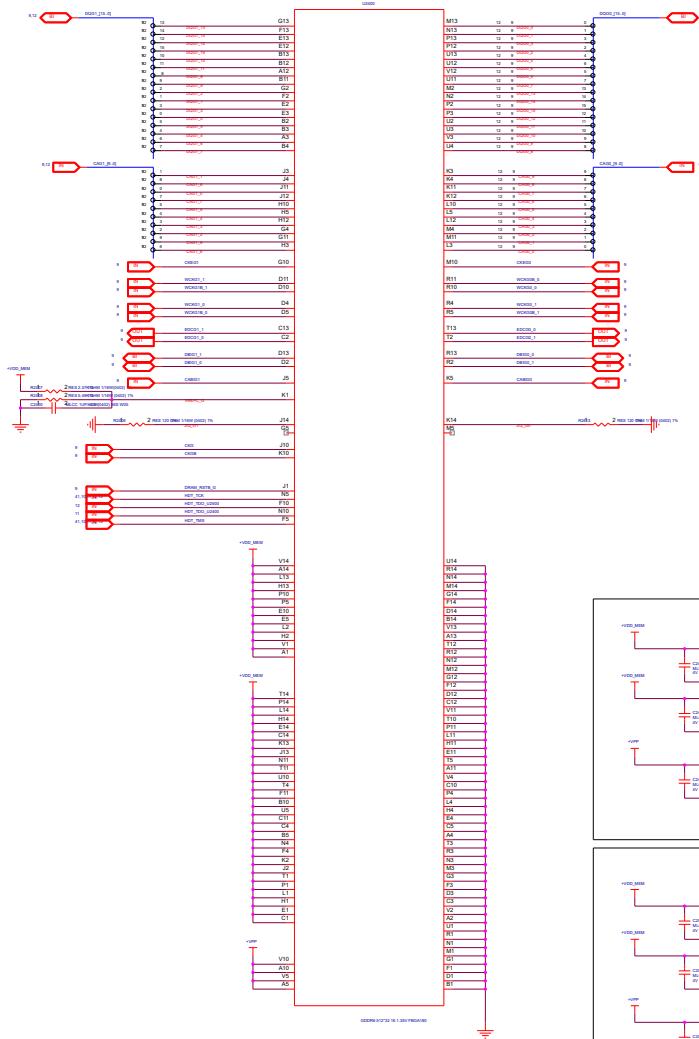




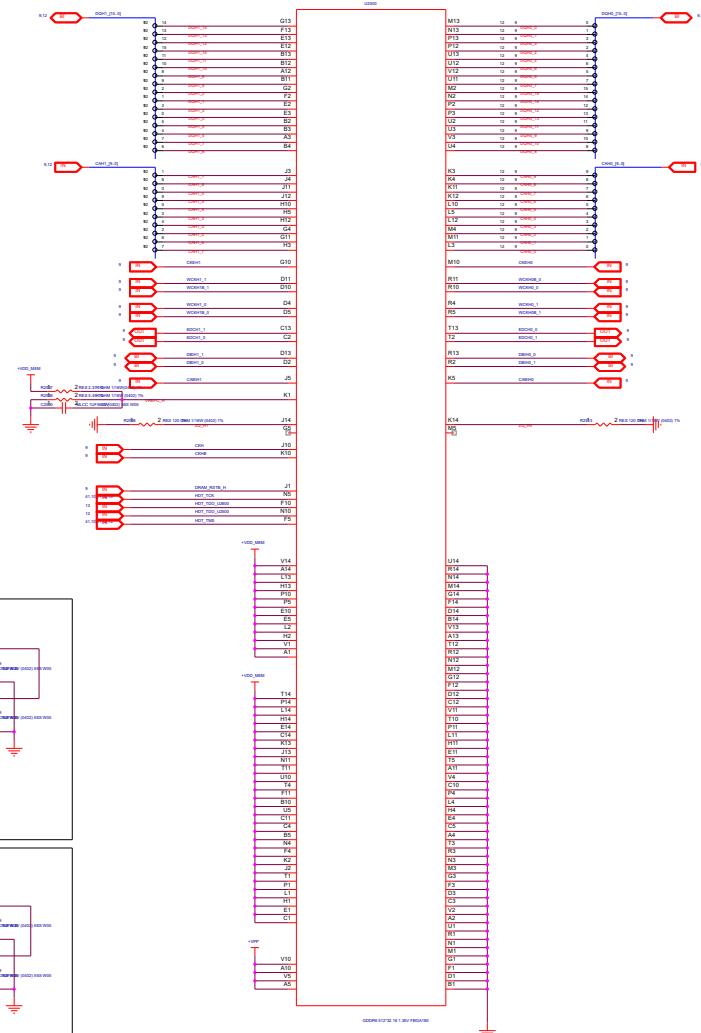


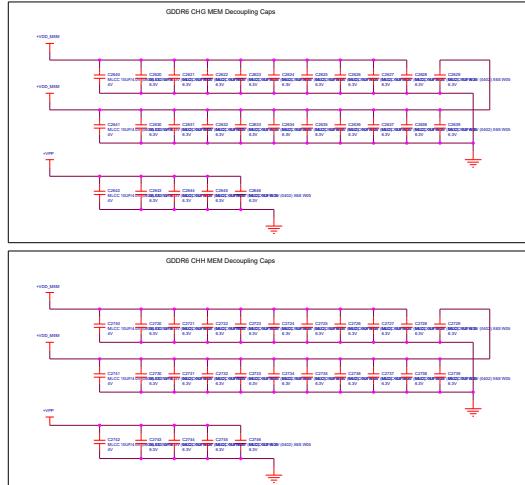
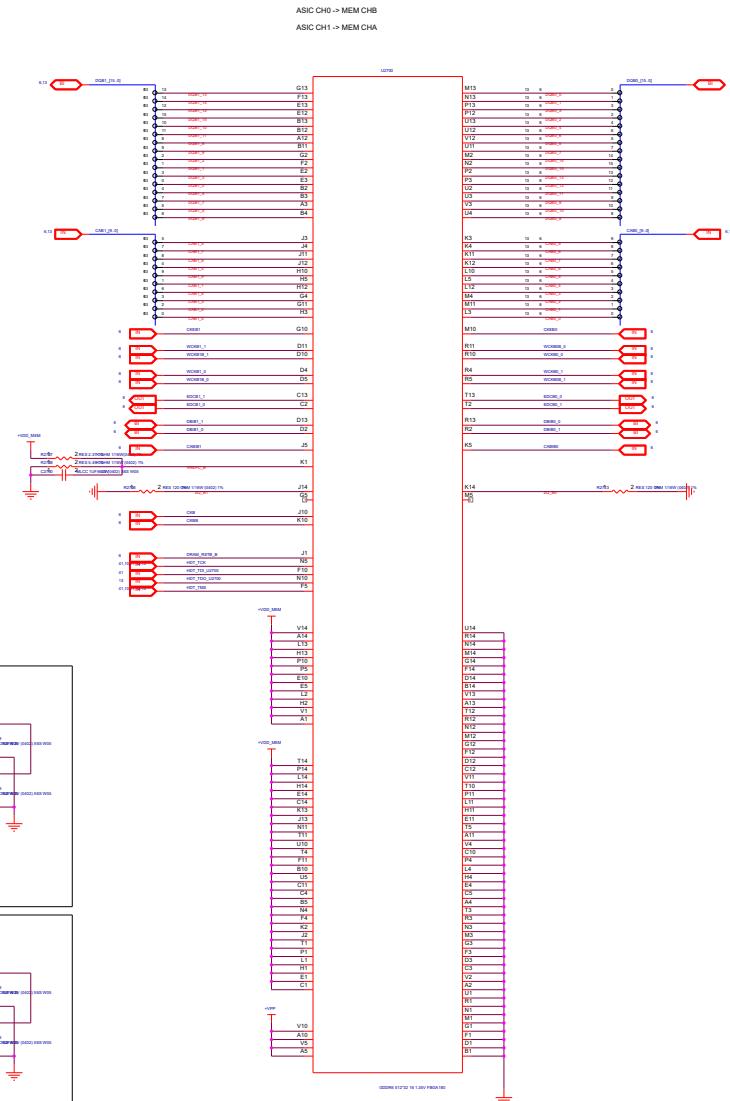
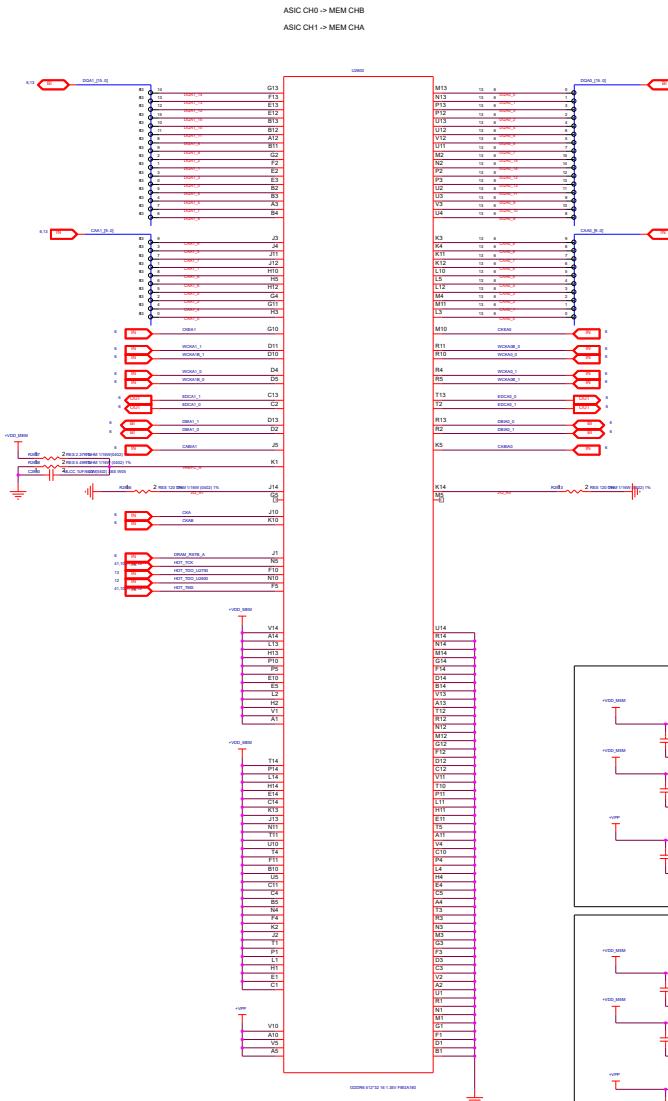


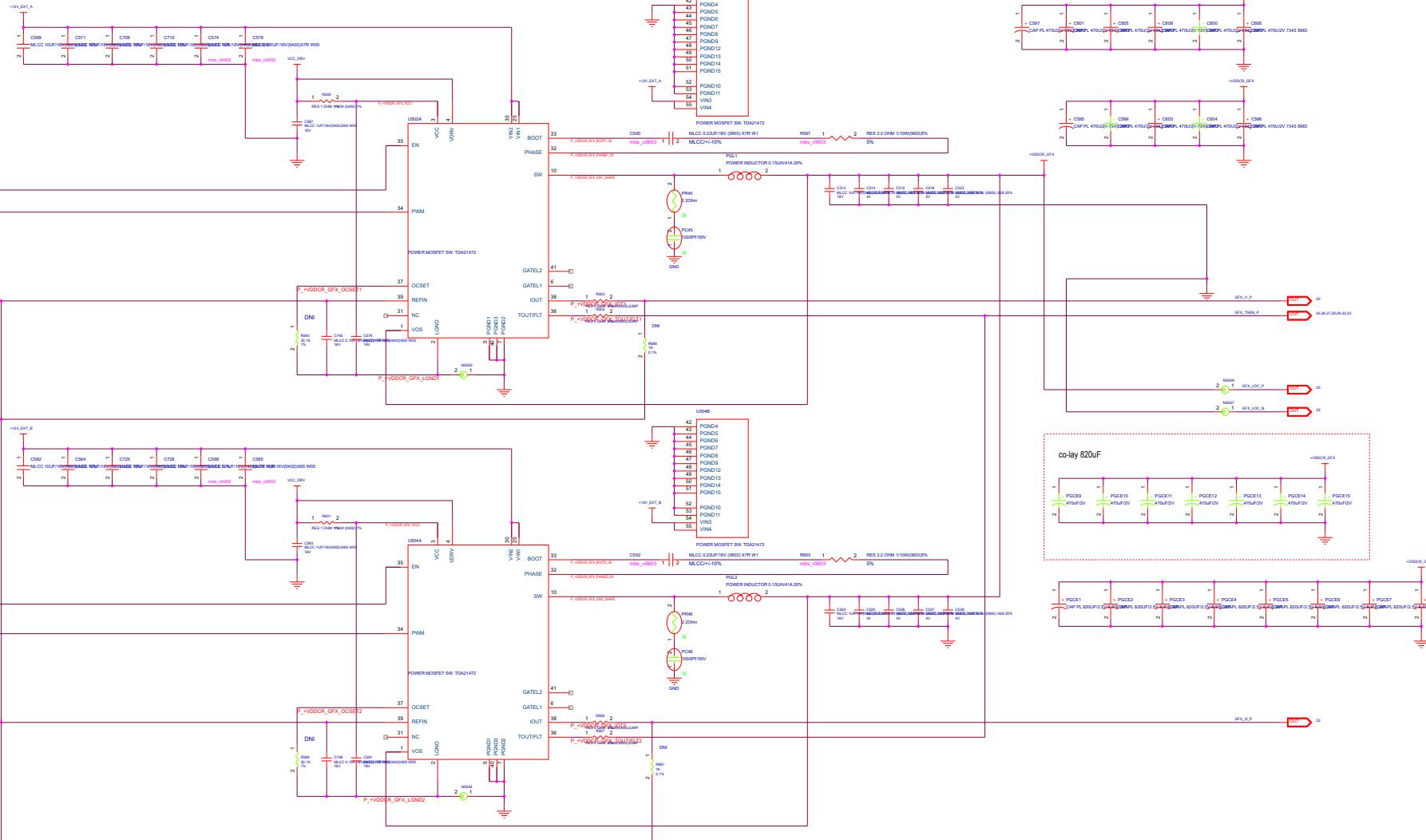
ASIC CH0 -> MEM CHB
ASIC CH1 -> MEM CHA



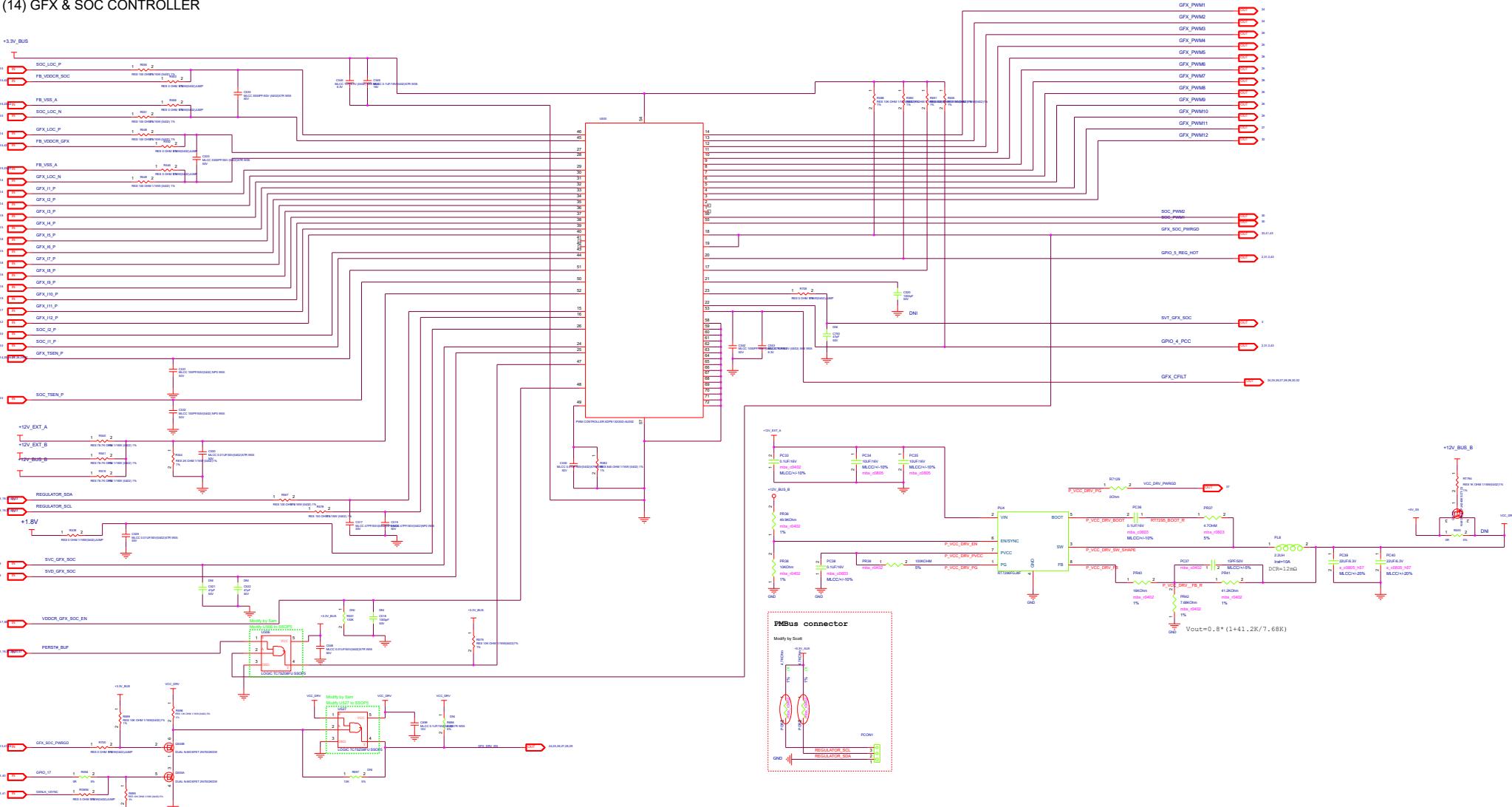
ASIC CH0 -> MEM CHB
ASIC CH1 -> MEM CHA

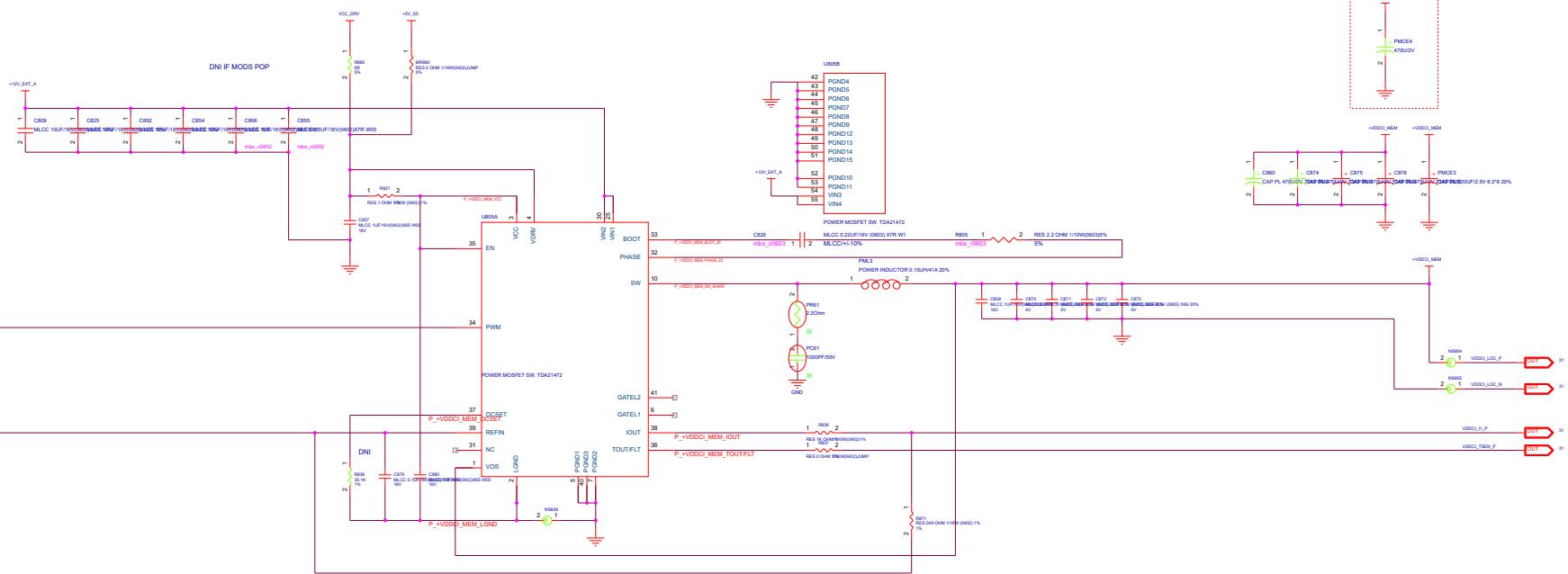


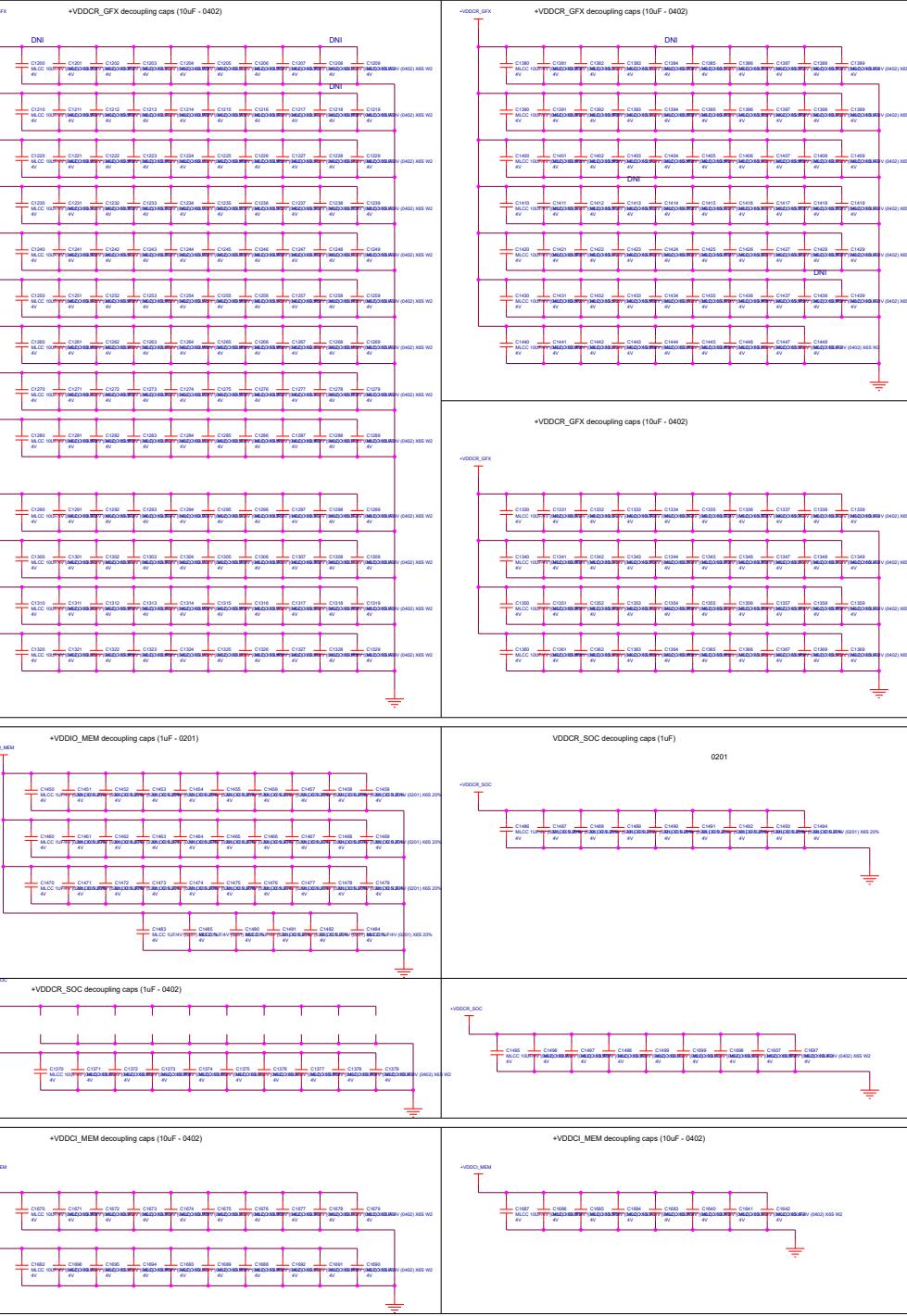


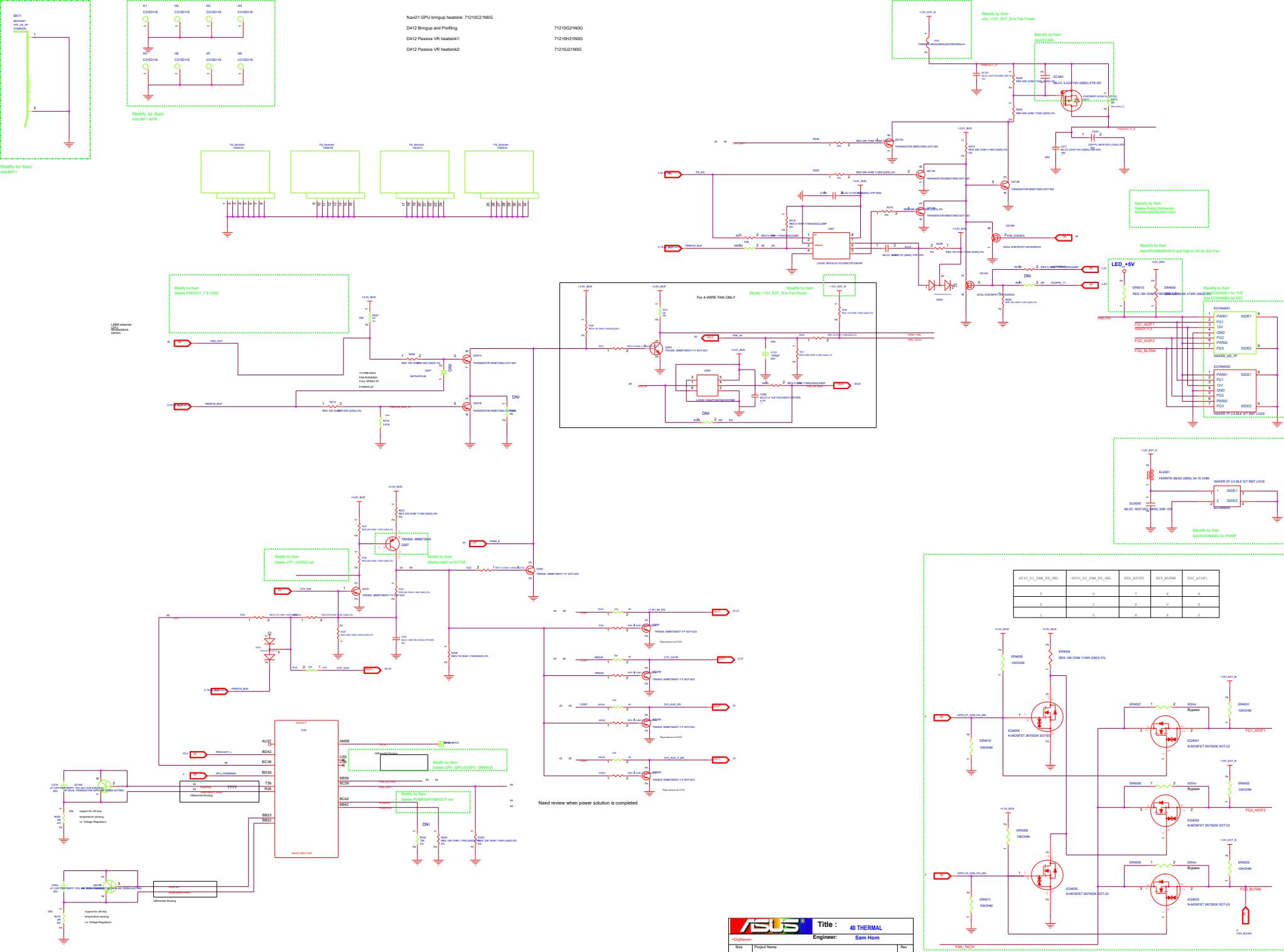


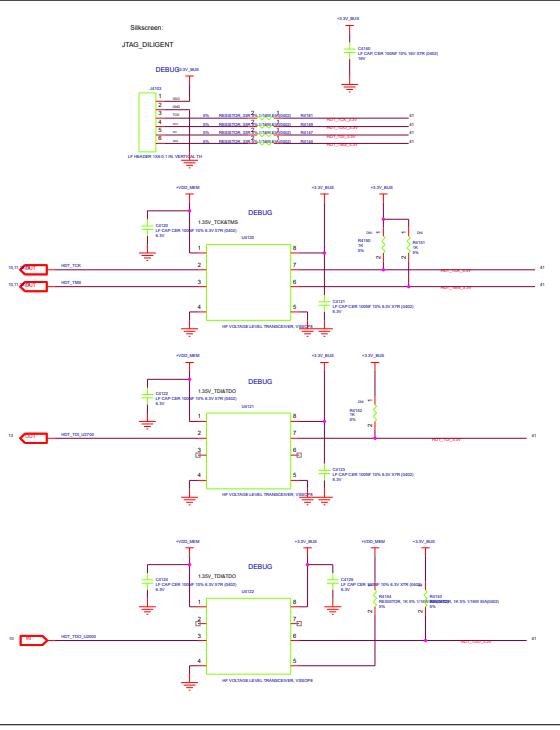
(14) GFX & SOC CONTROLLER









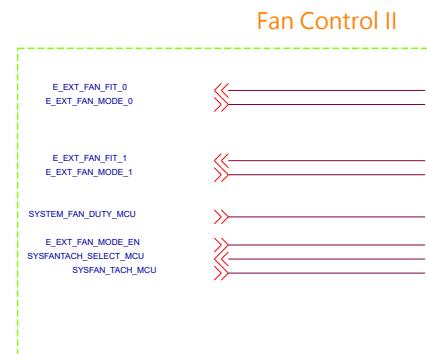
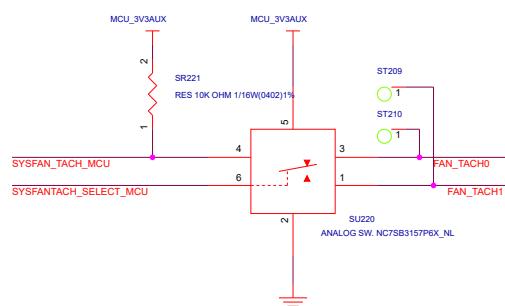
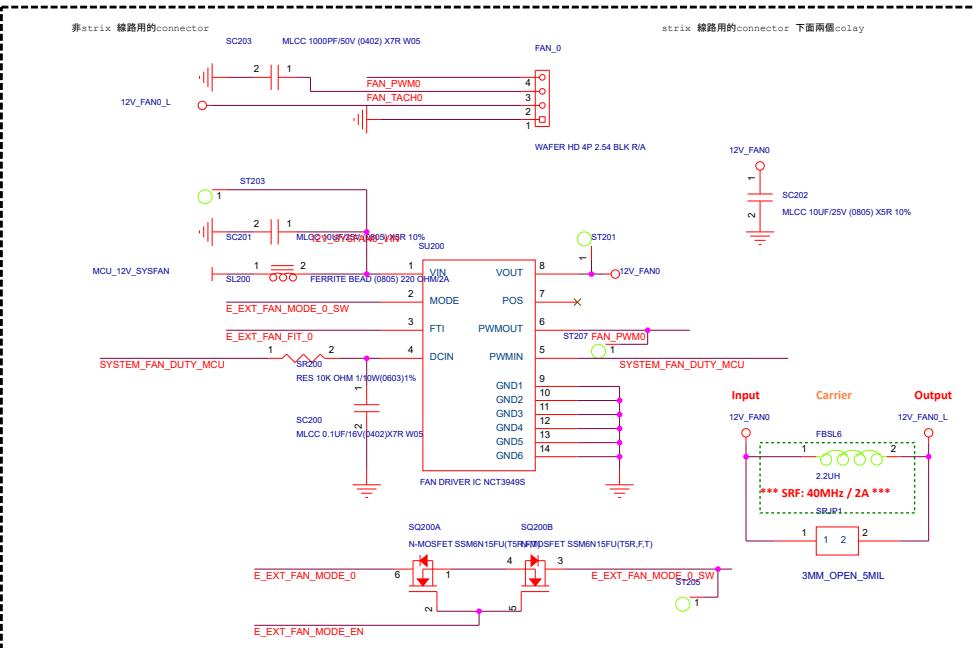


Modify by Sam
Delete RGB LED header
Delete RADEON Lightbar

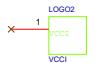
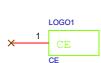
FOR PI DAUGHTER CARD
Modify by Sam
Date 12/05/14 08:03 AM 2012

1 -00B
Mon 11
2018
Added MODS circuit

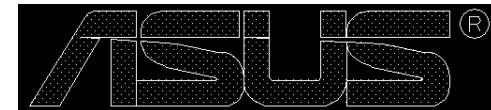
1 -00C
Sun 13
2018
Connected +12V_50 to OSC_VDD18
Gated +VBUS_PWR_USB03 by
USB4C_D007 Power protection
comes from +12V_50



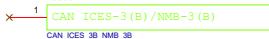
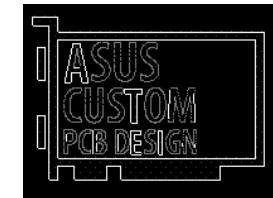
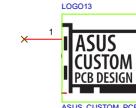
ASUS VGA PCB Logo



PCB MADE IN CHINA



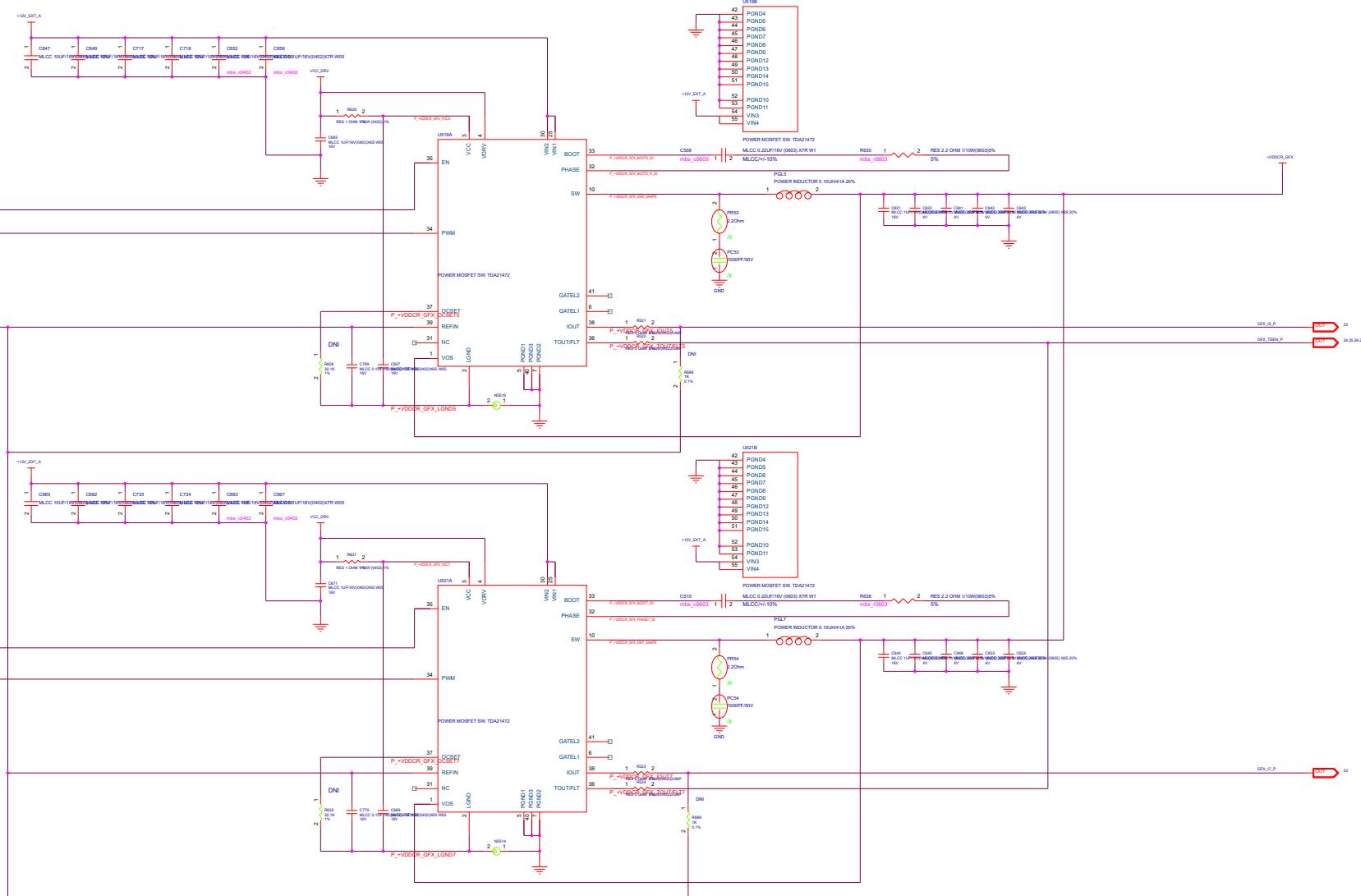
ASUS Re-design logo
Do not place this on reference board

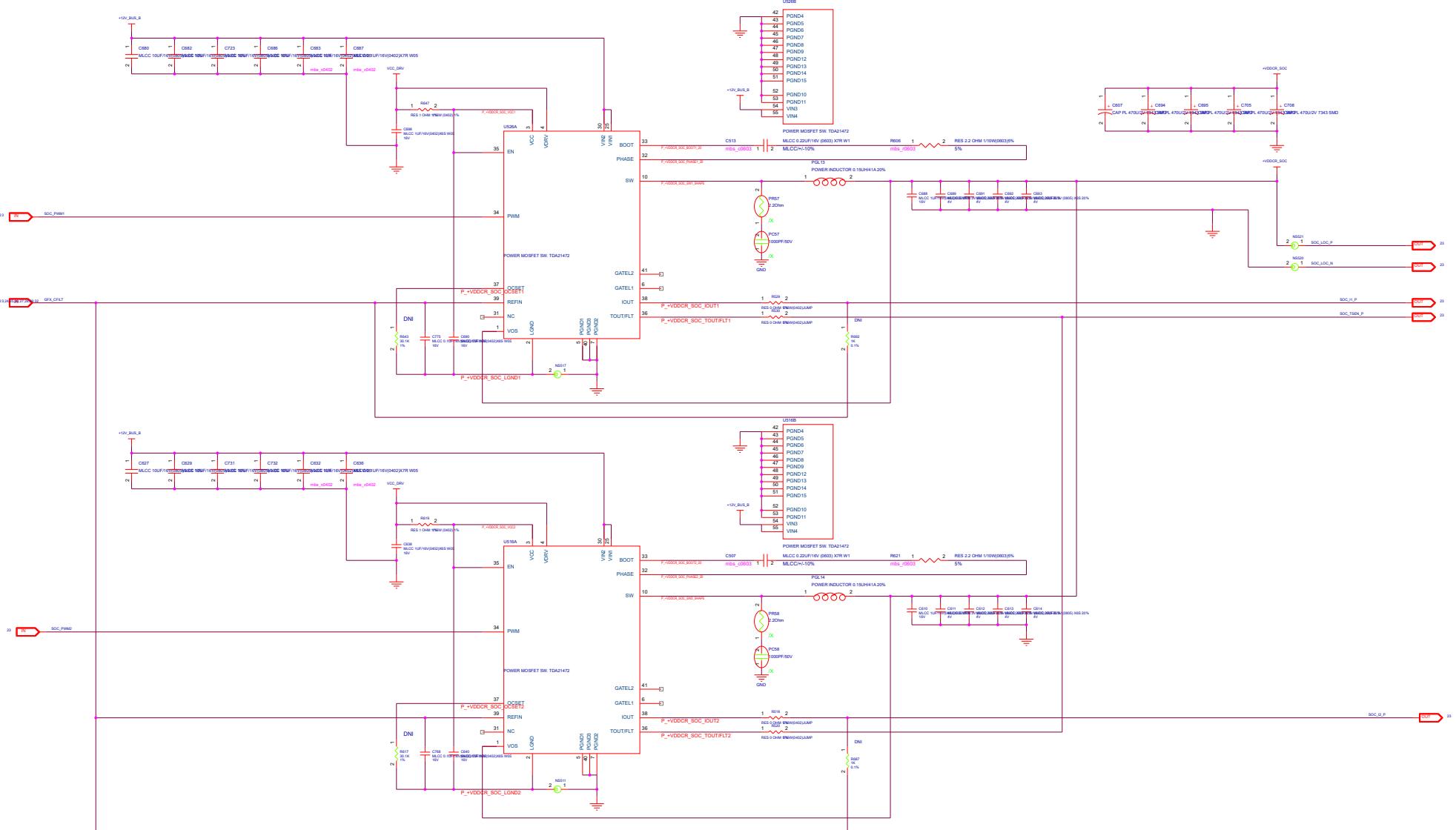


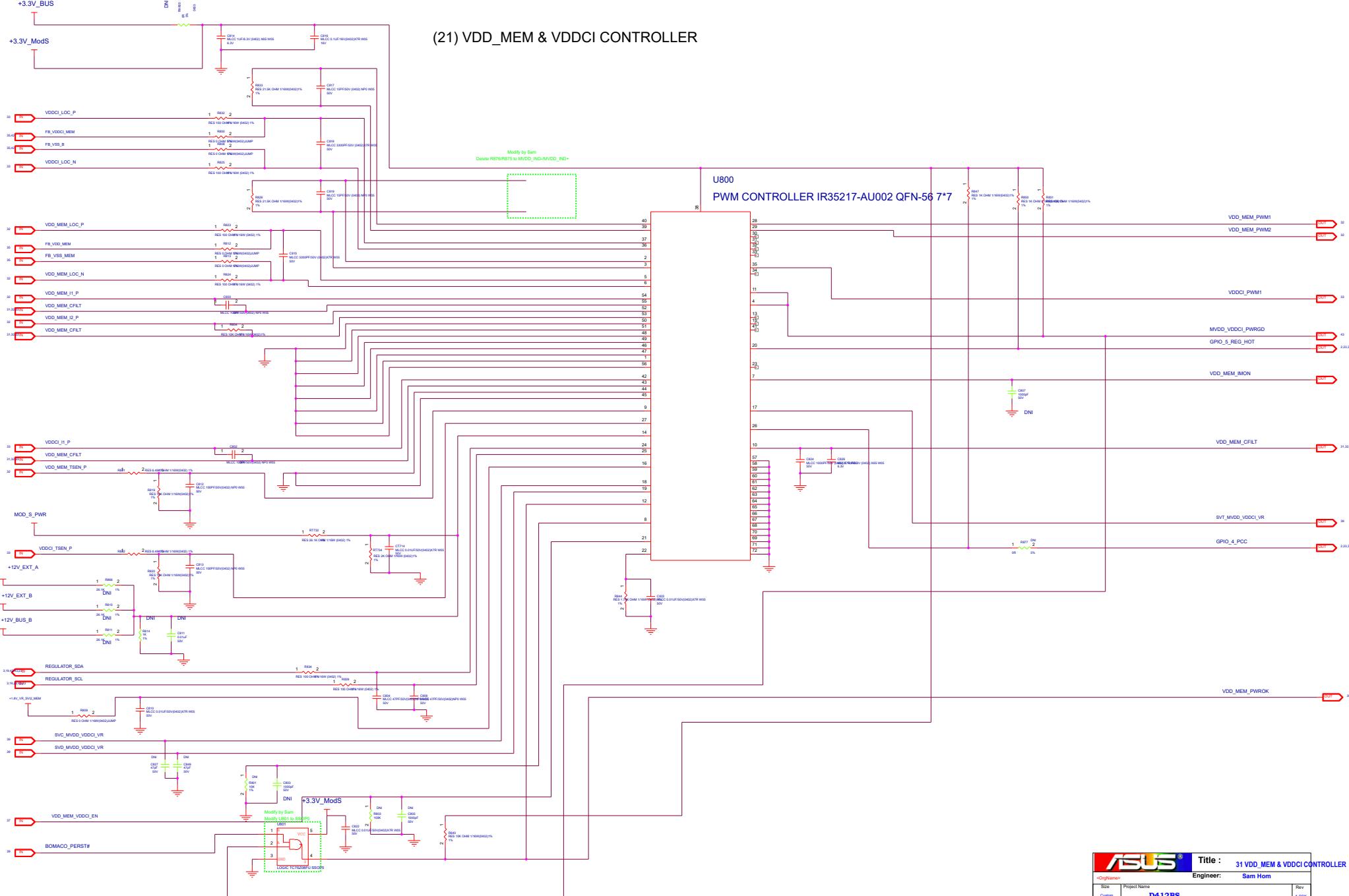
CAN ICES-3 (B) / NMB-3(B)

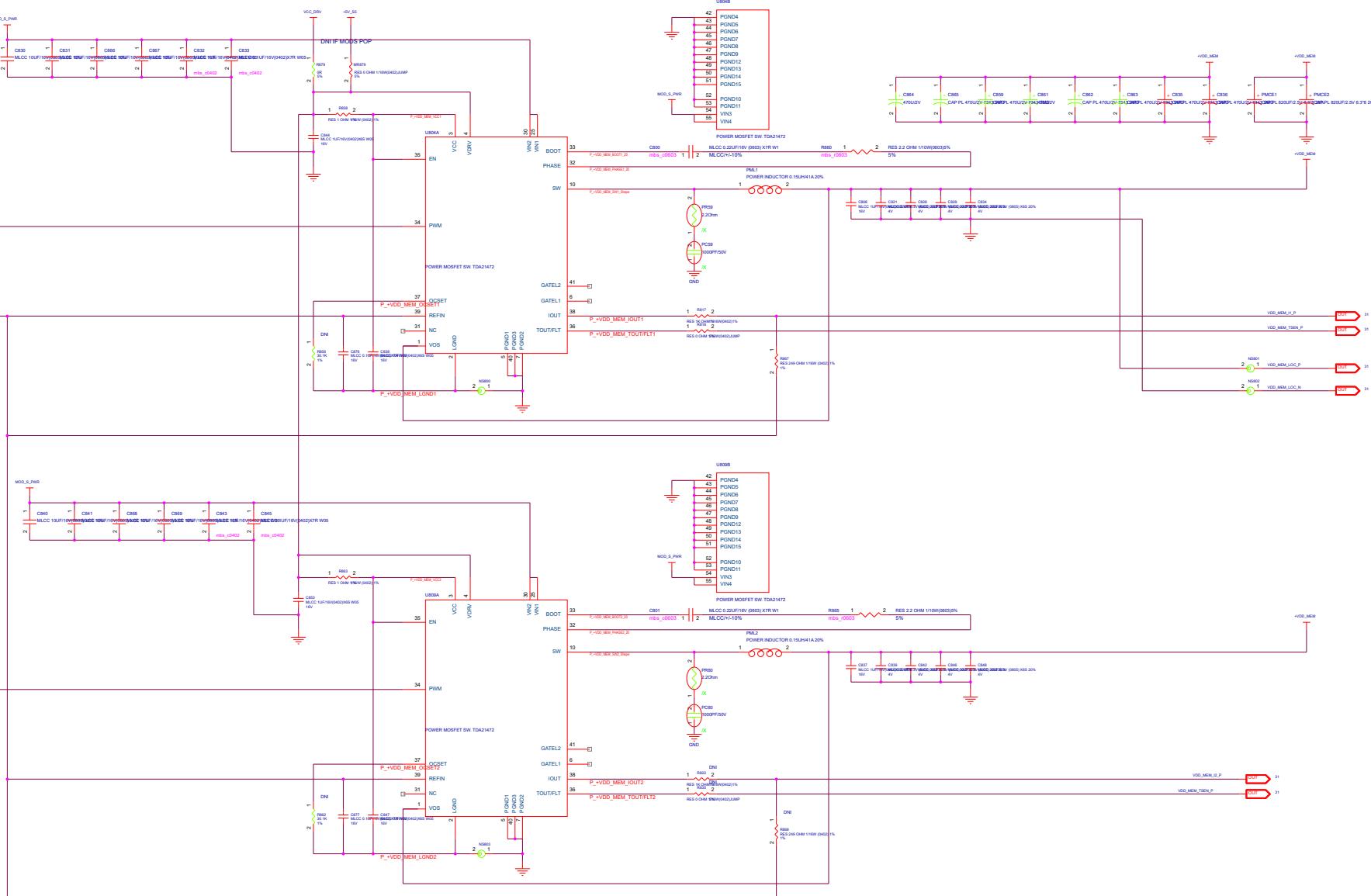


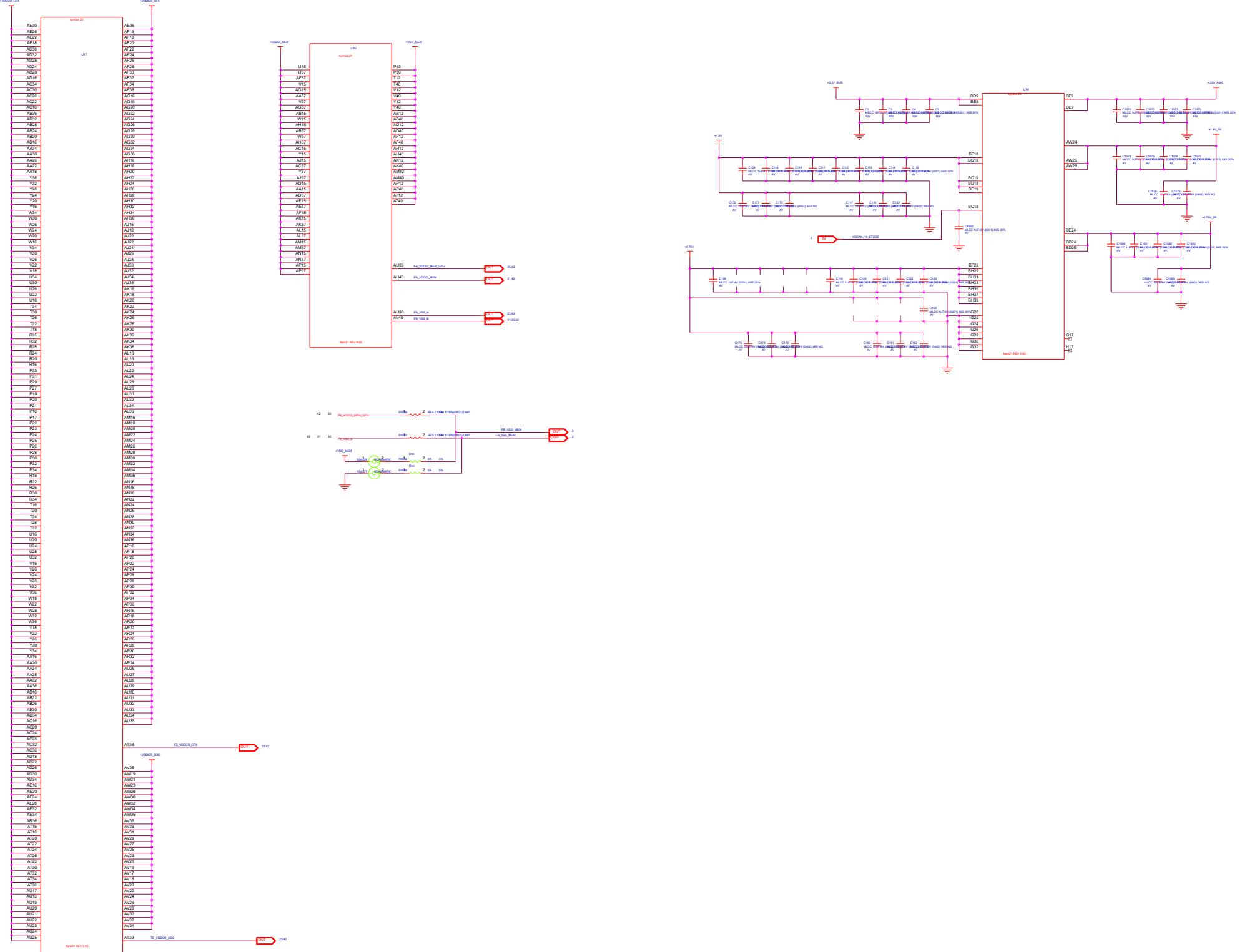
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<OrgName>	Project Name
Size	Rev
A3	D412BS
Date: Monday August 24, 2020	Sheet S1 of S1

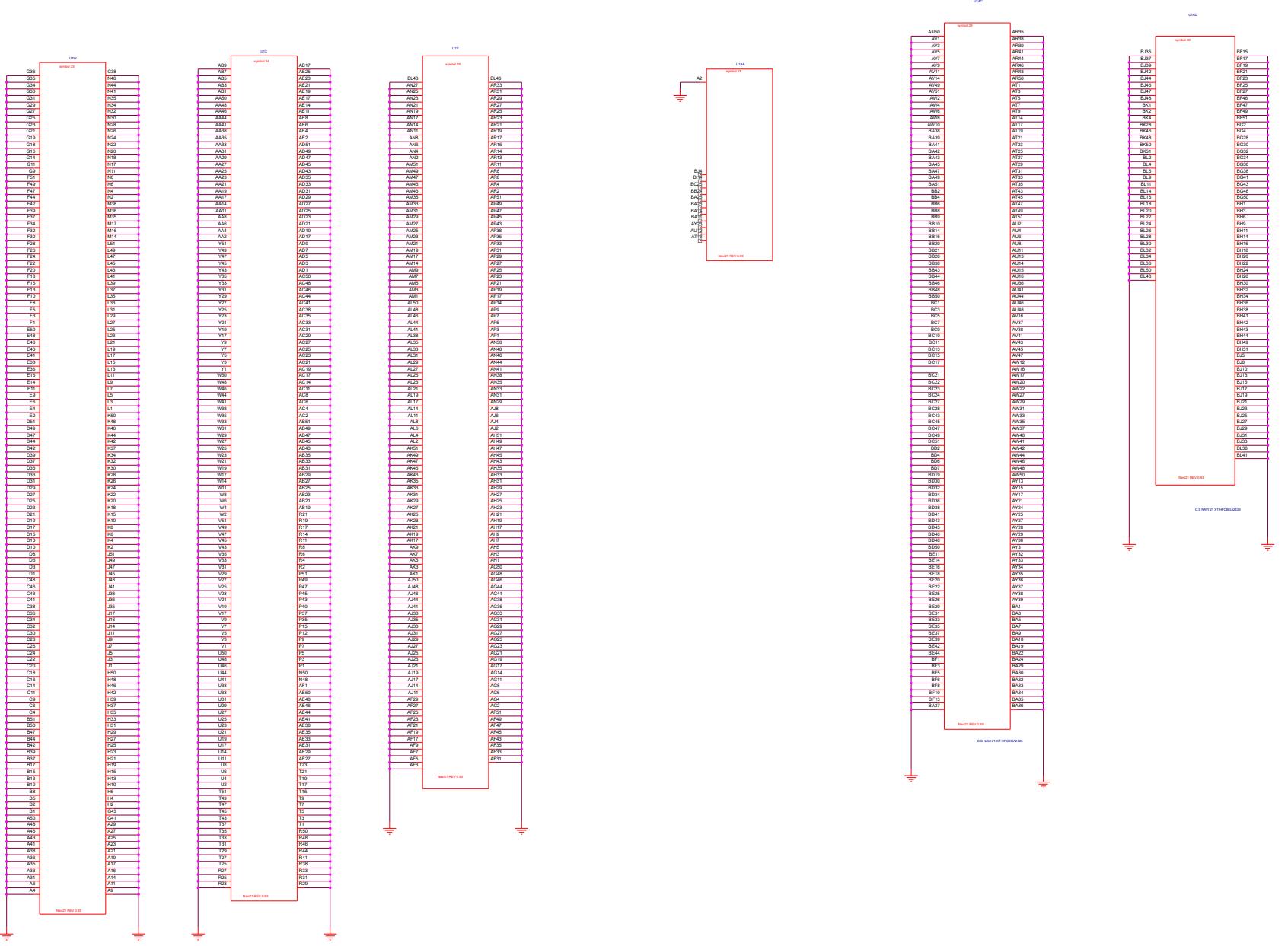


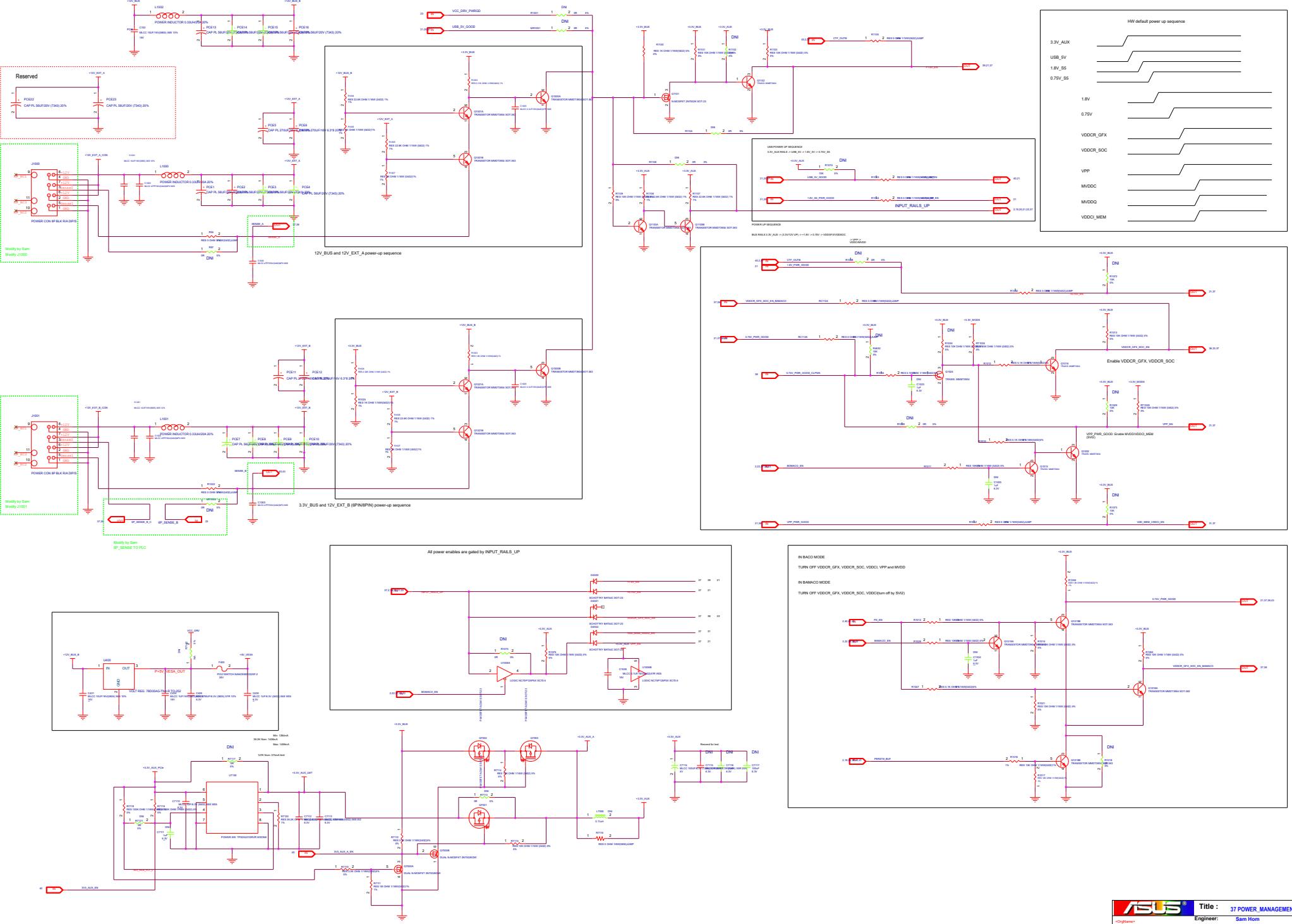


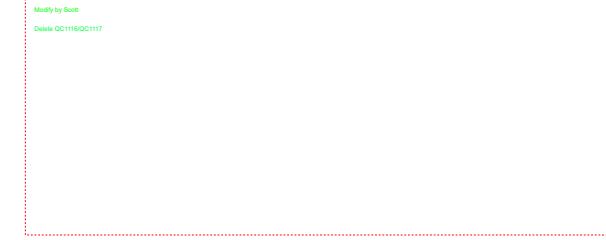
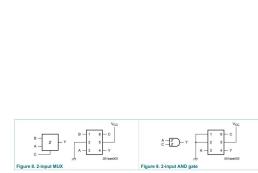
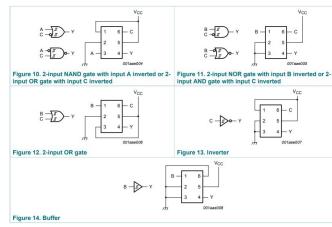












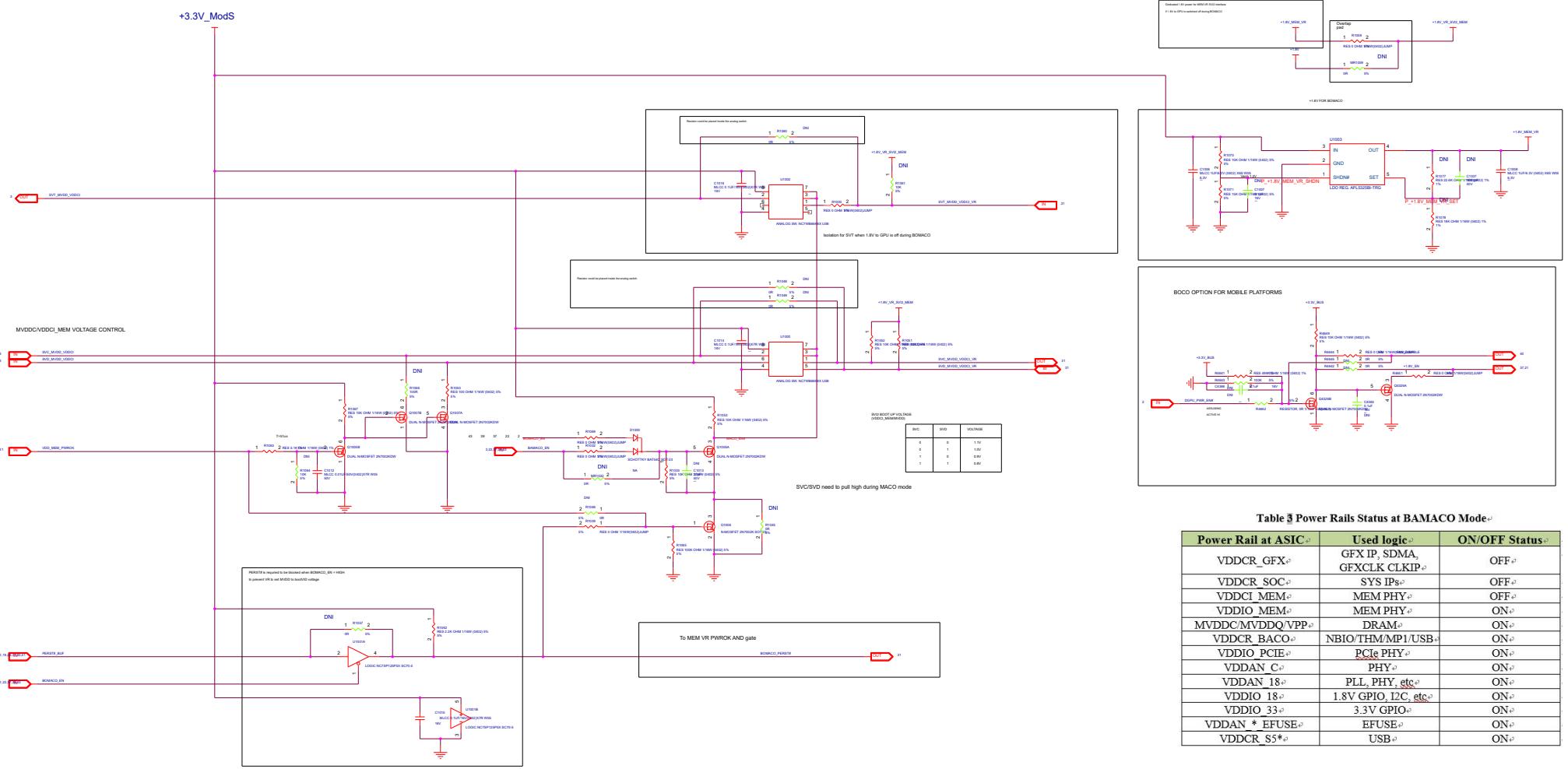


Table 3 Power Rails Status at BAMACO Mode^c

Power Rail at ASIC	Used logic	ON/OFF Status
VDDCR_GF0	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IP	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BAC0	NBIO/THM/MP1/USB	ON
VDDIO_PCIE	PCIe PHY	ON
VDDAN_C0	PHY	ON
VDDAN_18	PLL, PHY, etc	ON
VDDIO_18	1.8V GPIO, I2C, etc	ON
VDDIO_33	3.3V GPIO	ON
VDDAN_*_EFUSE	EFUSE	ON
VDDCR_S5*	USB	ON

Table 3 Power Rails Status at BOMACO Mode

Power Rail at ASIC ^o	Used logic ^o	ON/OFF Status for BOMACO-A ^o
VDDCR_GFX ^o	GFX IP, SDMA, GFXCLK CLKIP ^o	OFF ^o
VDDCR_SOC ^o	SYS IPS ^o	OFF ^o
VDDCI_MEM ^o	MEM PHY ^o	OFF ^o
VDDIO_MEM ^o	MEM PHY ^o	ON ^o
MVDDC/MVDDQ/VPP ^o	DRAM ^o	ON ^o
VDDCR_BACO ^o	NBIO/THM/MP1/USB ^o	OFF ^o
VDDIO_PCIE ^o	PCIe PHY ^o	OFF ^o
VDDAN_C ^o	PHY ^o	OFF ^o
VDDAN_18 ^o	PLL, PHY, etc. ^o	OFF ^o
VDDIO_18 ^o	1.8V GPIO, I _C , etc. ^o	OFF ^o
VDDIO_33 ^o	3.3V GPIO ^o	OFF ^o
VDDAN_EFUSE ^o	EFUSE ^o	OFF ^o
VDDCR_SS ^o	USB ^o	ON ^o

Table 4 Key Signals at Different PM Modes

Signals	Default	BOCO	BOMACO
PX EN ^c	LOW ^c	N/A ^c	N/A ^c
MACO EN ^c	N/A ^c	N/A ^c	N/A ^c
PERSTB ^c	HIGH ^c	1>0>1 ^c	1>0>1 ^c
PWR EN ^c	HIGH ^c	LOW ^c	LOW ^c
BOMACO EN ^c	LOW ^c	LOW ^c	HIGH ^c

Table 5 Platform to Support BOMACO+

BOMACO EN	SVC PU/PD	SVD PU/PD
HIGH ^o	PU ^o	PU ^o
LOW ^o	bootVID ^o	bootVID ^o

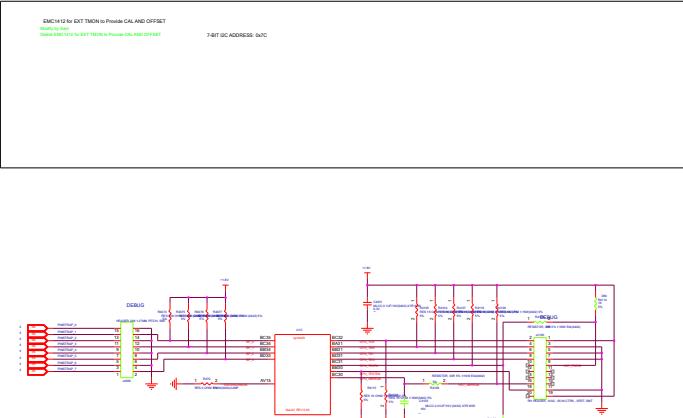
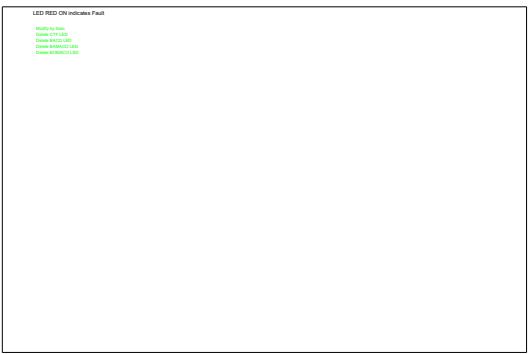
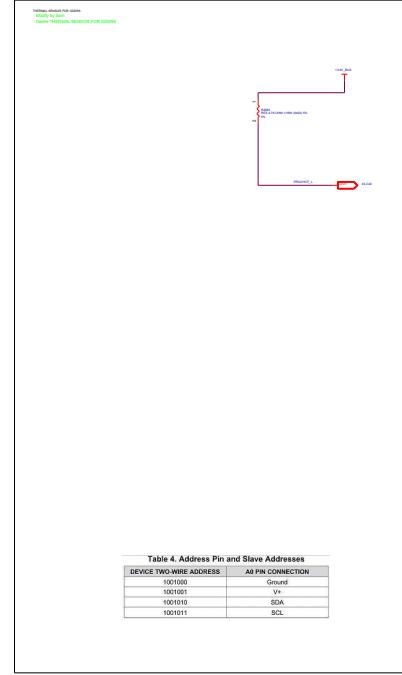
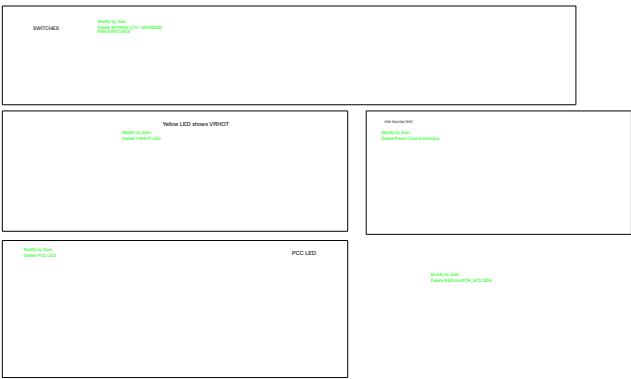
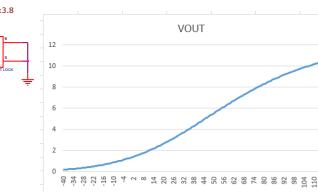
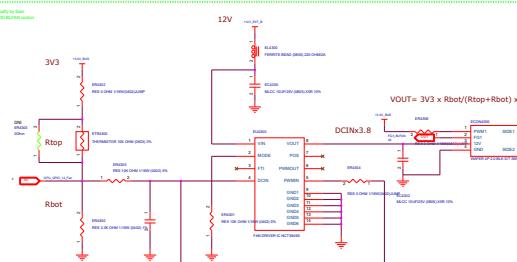
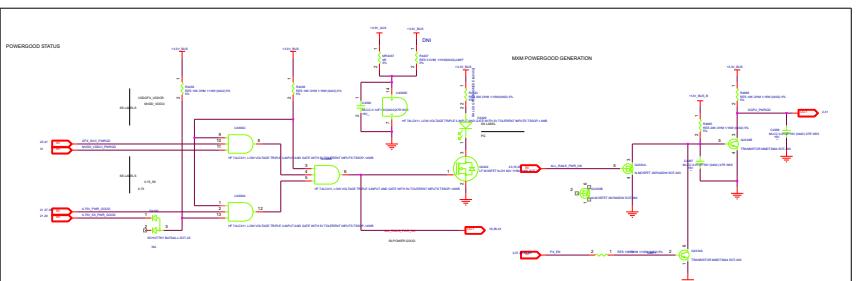
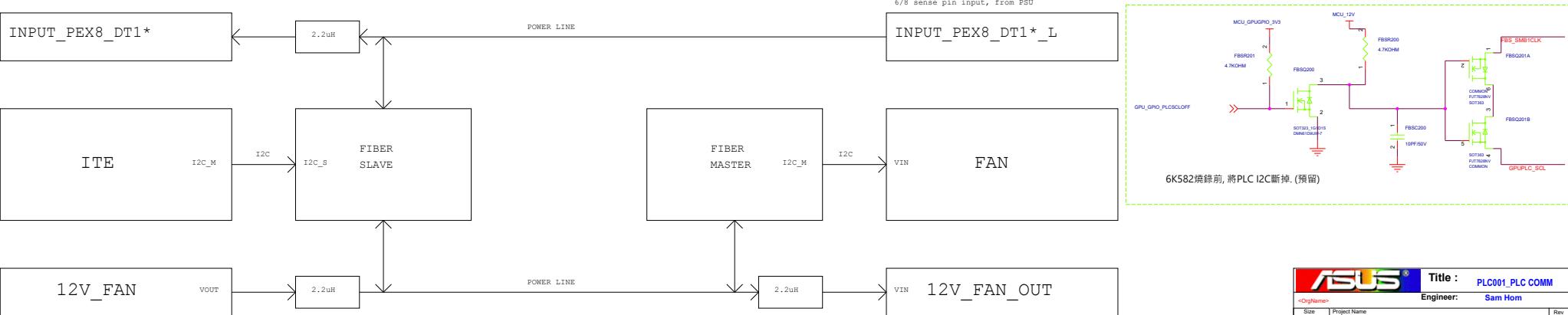
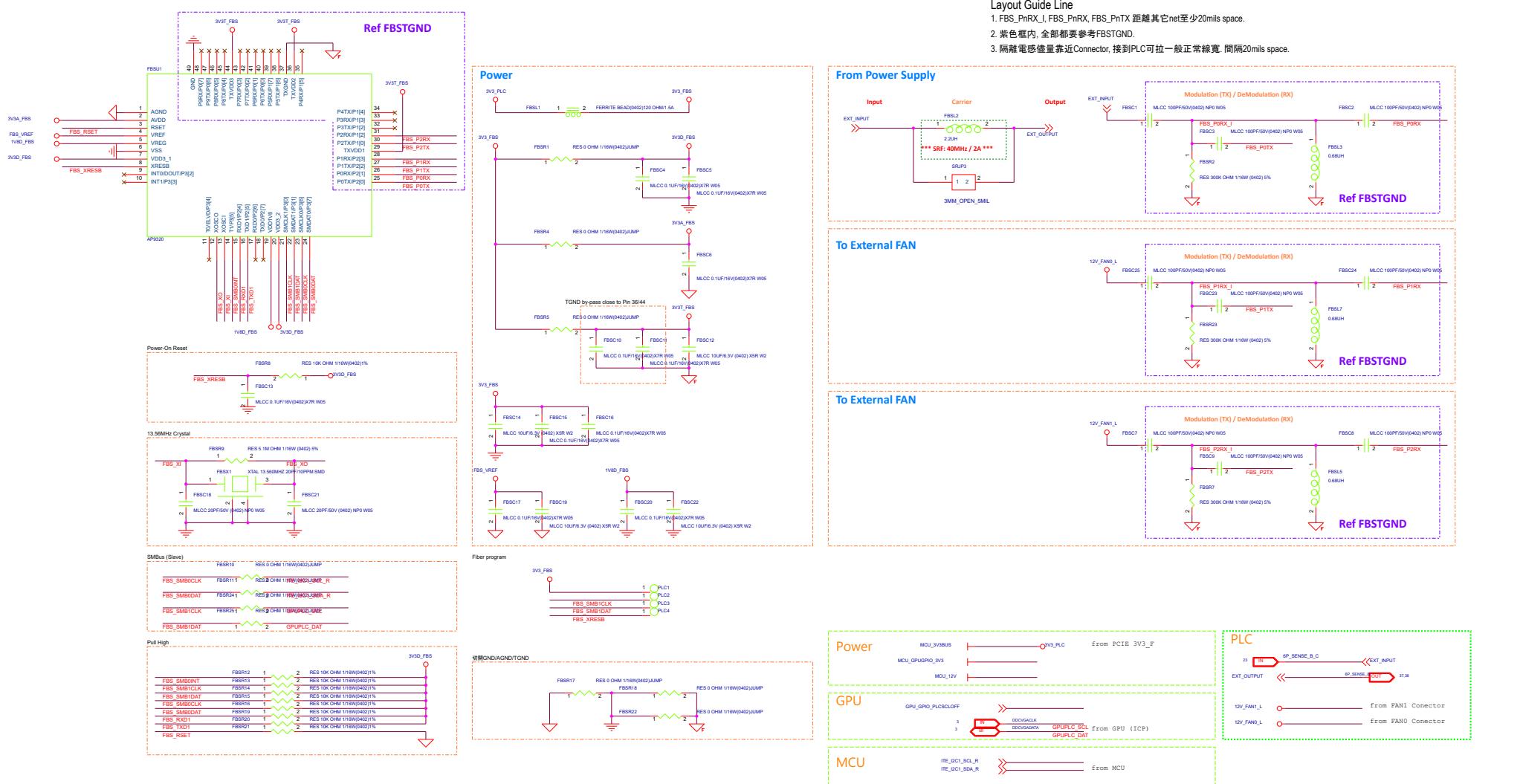


Table 4. Address Pin and Slave Addresses	
DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V _{DD}
1001010	SDA
1001011	SCL



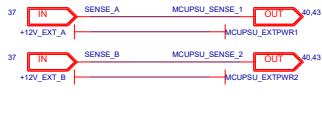


Power



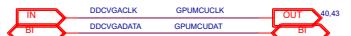
From 12V (for 外接式風扇使用, 任一組12V皆可)
From PCIE 3V3_AUX (for ITE)
From BUS 3V3 (for ITE logic判斷)
For 12V to 5V ARGB PWR

PSU DETECT INPUT



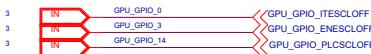
From EXT 0 (外部電源第一組)
From EXT1 (外部電源第二組)
From EXT1 (外部電源第三組)

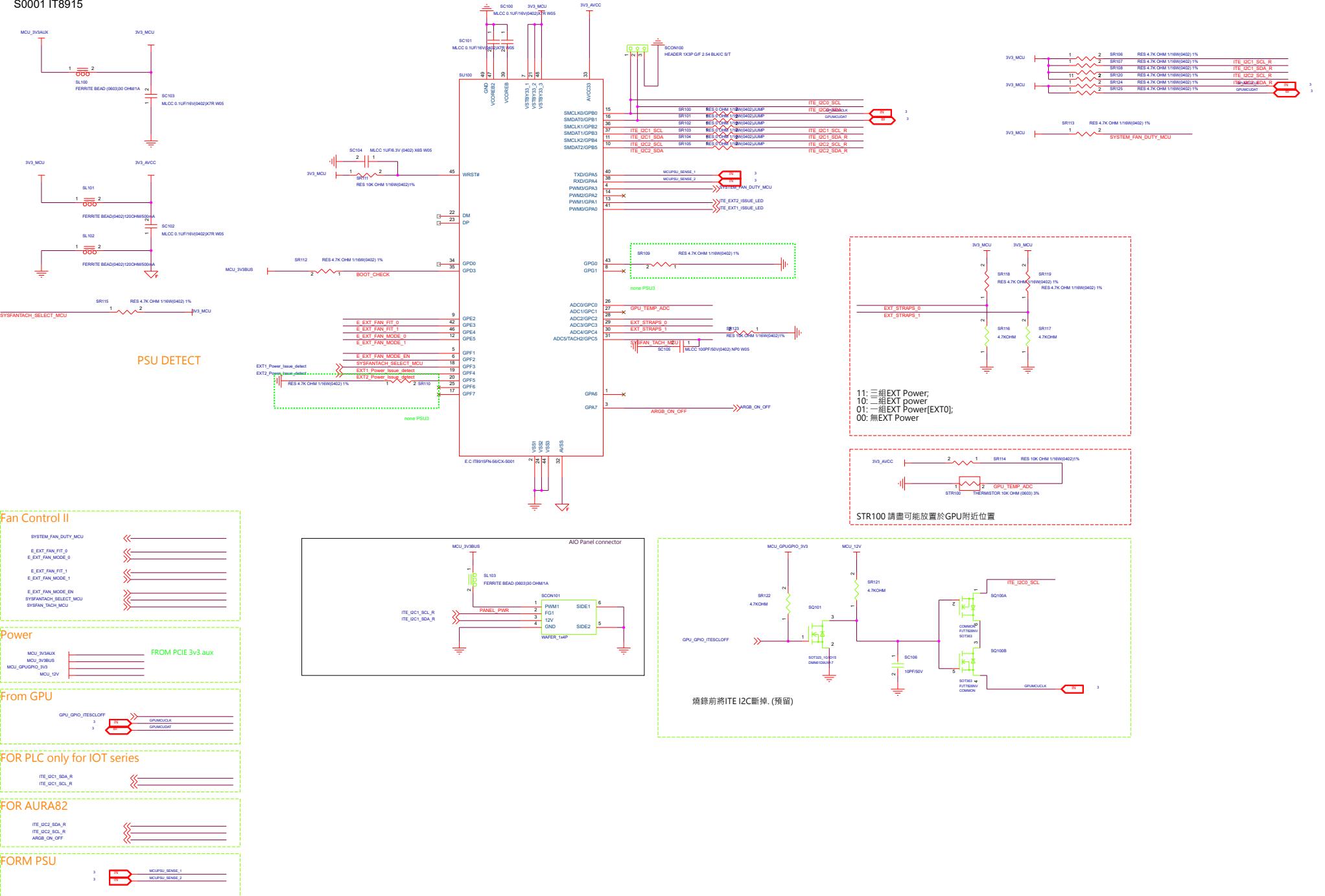
I2C

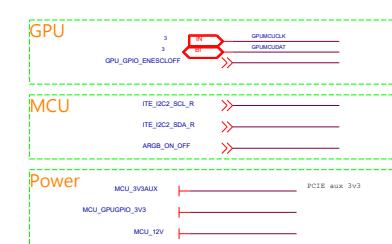
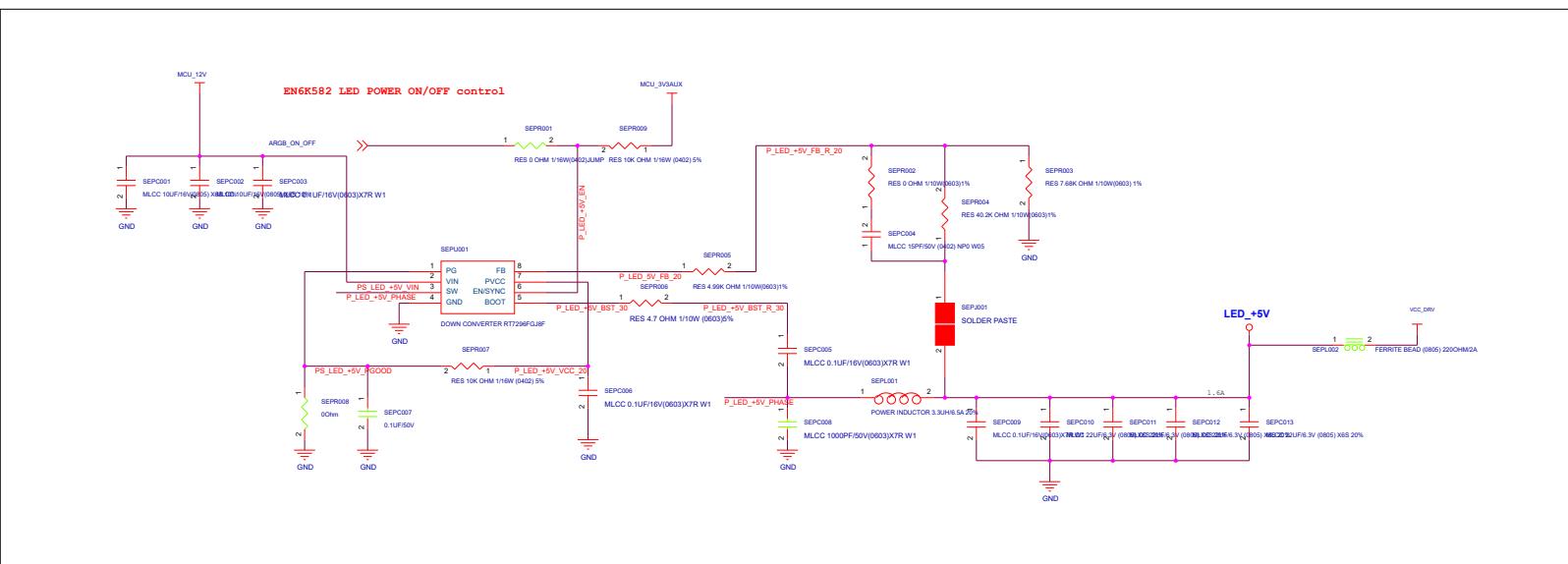
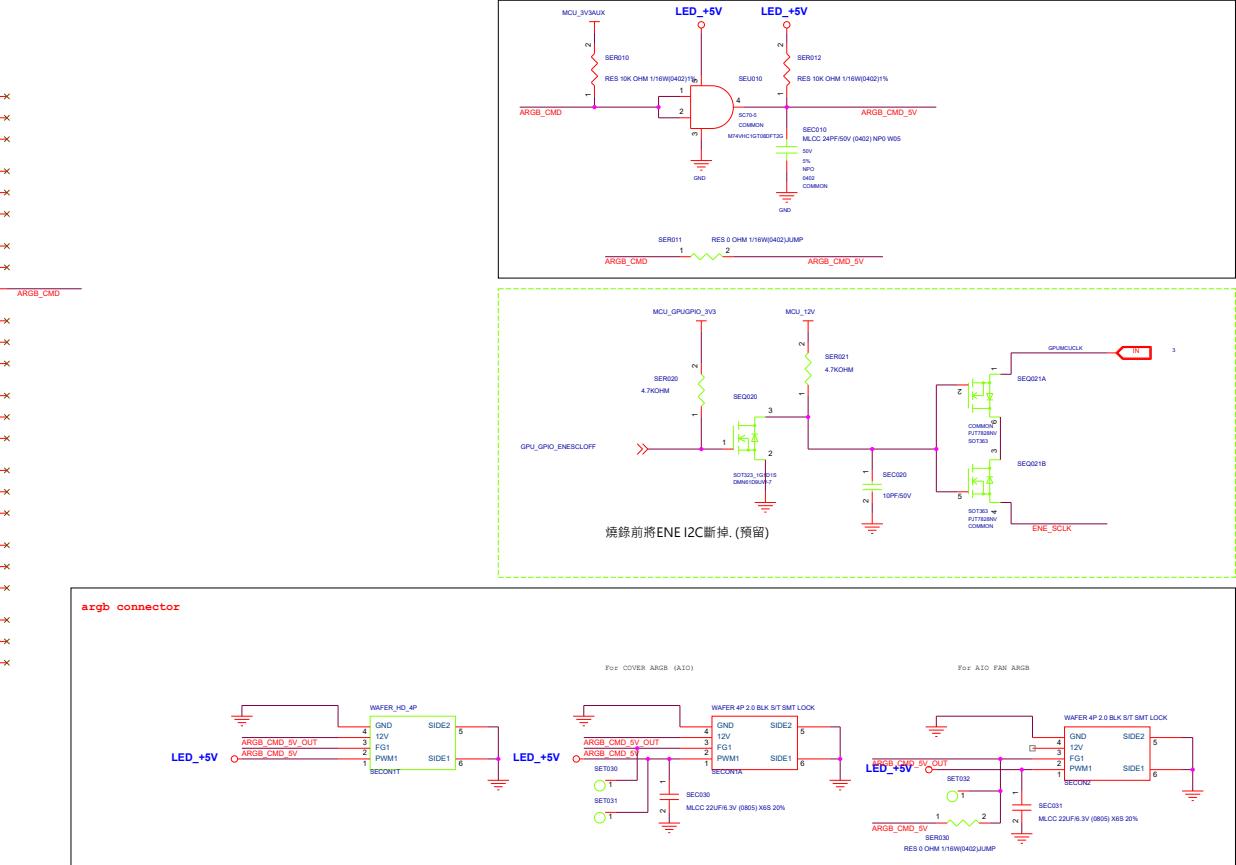
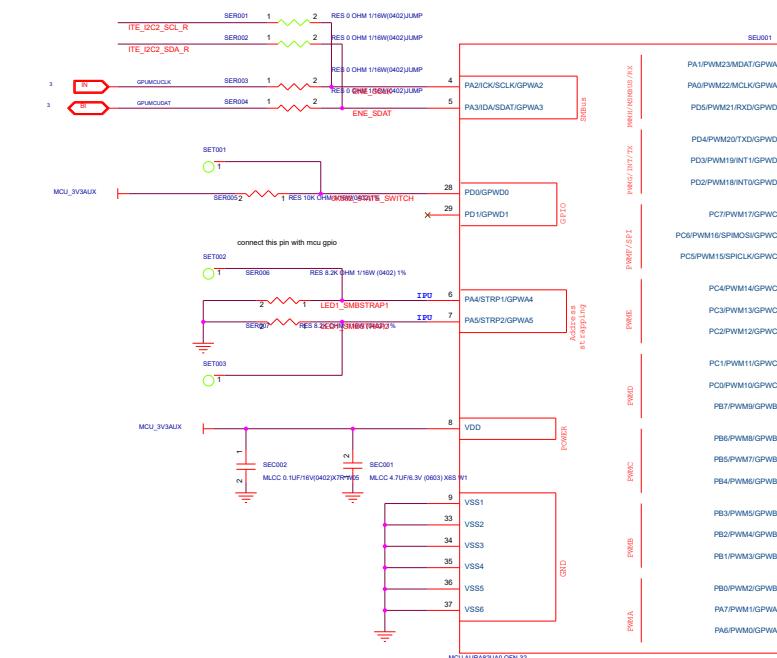


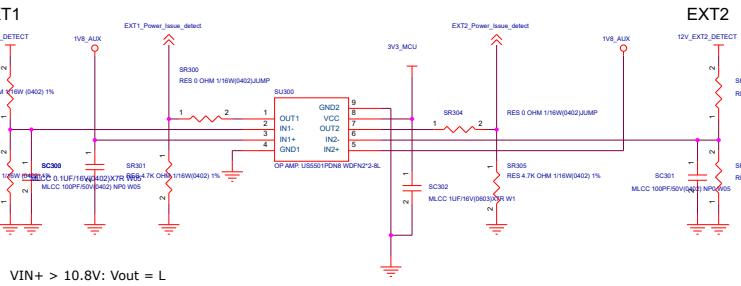
GPU I2CB Master (for ITE / ENE)

GPU_GPIO









MCUPSU_EXTPOWER1 | SL300 2 1 FERRITE BEAD (960330 OHM/1A) | 12V_EXT1_DETECT
MCUPSU_EXTPOWER2 | SL301 2 1 FERRITE BEAD (960330 OHM/1A) | 12V_EXT2_DETECT

