

**CONFIDENTIAL & PROPRIETARY** ADVANCED MICRO DEVICES INC.  
© 2007 Advanced Micro Devices Inc.

This AMD schematic and design is the exclusive property of AMD and is provided only to entities under a non-disclosure agreement with AMD. This document contains confidential information and is intended solely for the use of the addressee and for no other purpose. Reproduction or distribution of this document without prior written permission from AMD is prohibited. Use of this schematic and design for any purpose other than that which creates a third party licensing agreement with AMD, AMD makes no representations or warranties of any kind regarding AMD's status as owner, creator, inventor, licensee, or assignee of the schematic and design, including, but not limited to, any implied warranty of merchantability or suitability for a particular purpose, and disclaims responsibility for consequences resulting therefrom.

Title Cedar DDR3 MxM3.0

Advanced Micro Devices Inc.  
1 Commonwealth Valley Drive East  
Markham, Ontario

**AMD**

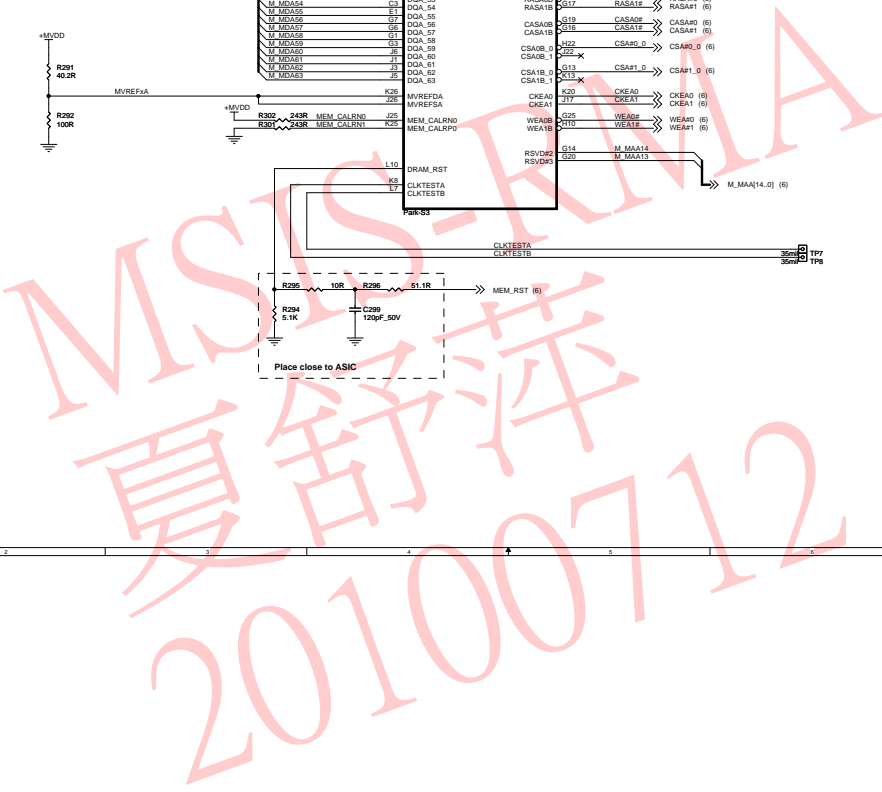
Date: \_\_\_\_\_  
\_\_\_\_\_ Wednesday, February 24, 2010


Rev 1

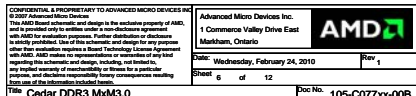
Sheet \_\_\_\_\_ of \_\_\_\_\_

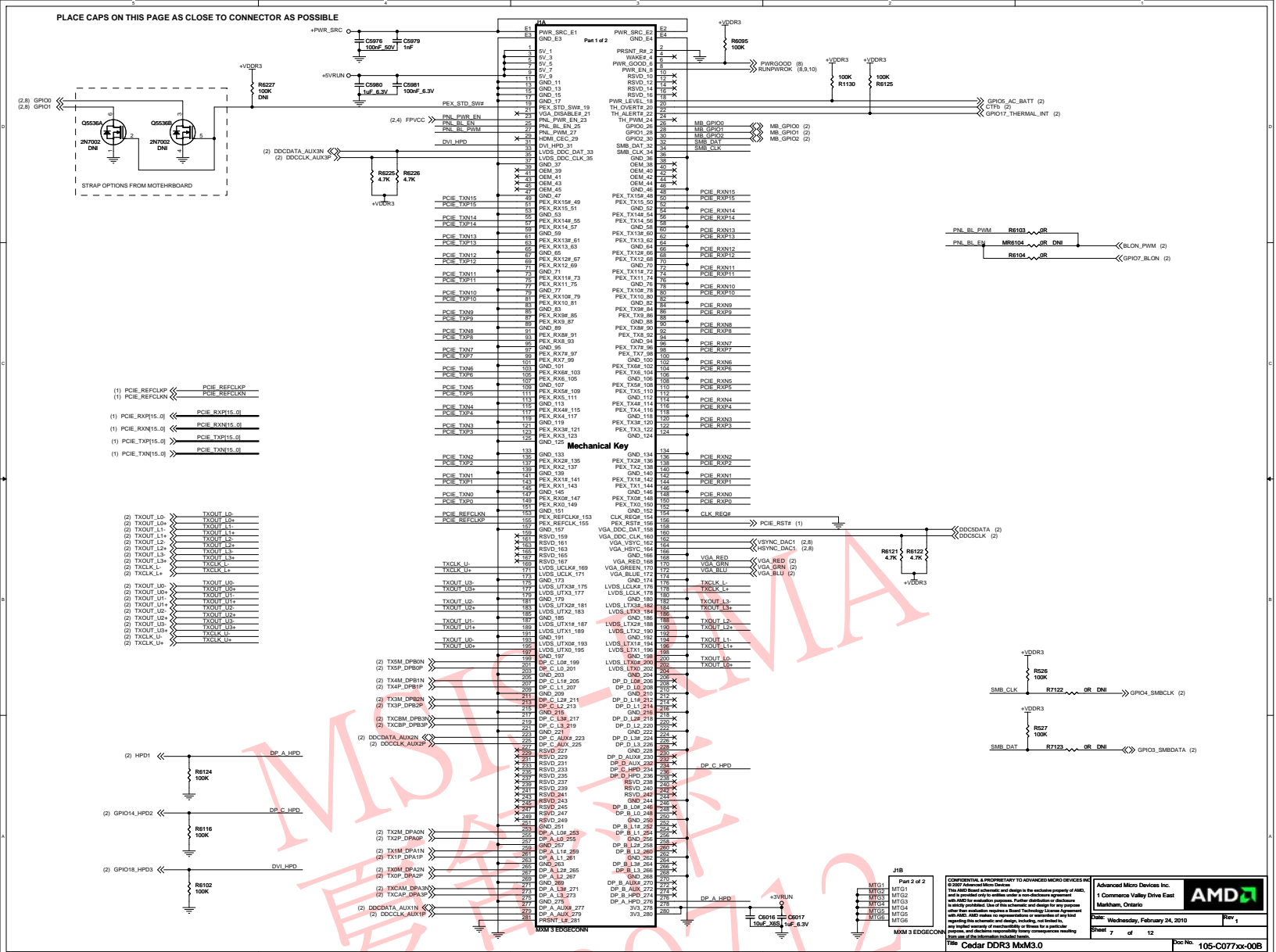
Doc No. 106-C077Xxx-00B





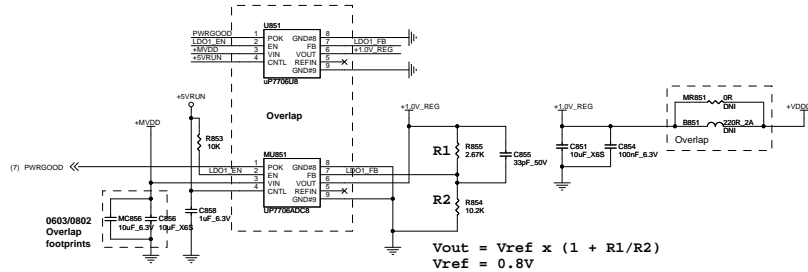
Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario			
Date: Wednesday, February 24, 2010		Rev 1	
Sheet 5 of 12		Doc No. 105-C077xx-00F	





### Voltage Settings and Power Play

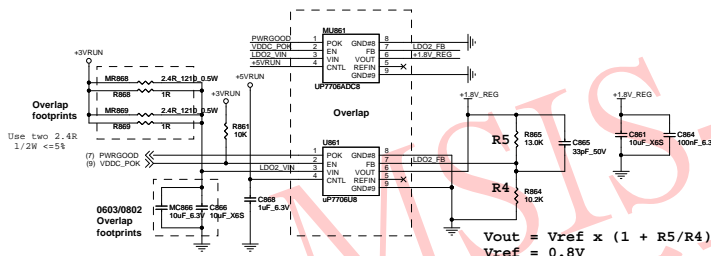
**LDO1      Vin = +1.5V +/-2%      Vout = +1.0V +/- 2%      Iout = 1.5A RMS MAX (TBV)**  
**PCB: 50 to 70mm sq. copper area for cooling**



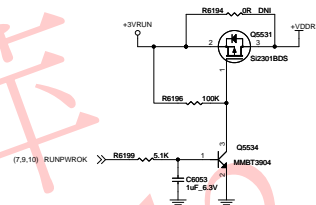
## PIN STRAPS

- | GPIO             | Pin    | Function | IO Mode | IO Type | IO Direction |
|------------------|--------|----------|---------|---------|--------------|
| (2,7) GPIO0      | GPIO0  | R6134    | 10K     |         |              |
| (2,7) GPIO1      | GPIO1  | R6135    | 10K     |         |              |
| (2,7) GPIO2      | GPIO2  | R6136    | 10K     |         |              |
| (2) GPIO9        | GPIO9  | R6138    | 10K     | DNI     |              |
| (2) GPIO11       | GPIO11 | R6139    | 10K     | DNI     |              |
| (2) GPIO12       | GPIO12 | R6140    | 10K     | DNI     |              |
| (2) GPIO13       | GPIO13 | R6141    | 10K     |         |              |
| (2) GPIO22       | GPIO22 | R6147    | 10K     |         |              |
| (2,7) VSYNC_DAC1 | V1SYNC | R6142    | 10K     |         |              |
| (2,7) HSYNC_DAC1 | H1SYNC | R6143    | 10K     |         |              |
| (2) VSYNC_DAC2   | V2SYNC | R6145    | 10K     |         |              |
| (2) HSYNC_DAC2   | H2SYNC | R6146    | 10K     | DNI     |              |

LDO2       $V_{in} = +3.3V \pm 6\%$        $V_{out} = +1.8V \pm 2\%$        $I_{out} = 0.8A \text{ RMS MAX (TBV)}$   
PCB: 50 to 70mm sq. copper area for cooling



## VDDR3 GATING



## CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET**

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_EN	GPIO0	Full Power Saving Enable # EN: TX output enabled # TX output swing	1
TX_DEEMPH_EN	GPIO1	PCIe Transmitter De-emphasis Enable # TX de-emphasis disabled # TX de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIe Gen2 Enable # 1. Advertises the PCIe device as 5.0GT/s capable at power-on	1
BIF_VGA_DS	GPIO3	VGA Control # VGA controller capability enabled # VGA controller capability disabled (for multi-GPU)	0
ROMCFGCFG[0]	GPIO1[1:11]	Serial ROM type or Memory Aperture Size Select # GPIO2[1:1, defines ROM type # GPIO2[2:11, defines ROM type 101 - 512Kbit M28P01A (ST) 101 - 1Mbit M28P01A (ST) 101 - 1Mbit M28P01B (ST) 101 - 4Mbit M28P01B (ST) 101 - 4Mbit M28P01C (ST) 101 - 512Kbit M28P01E2 (Chipsale) 101 - 1Mbit M28P01V01E2 (Chipsale)	XXXX
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM Device 1 - Enabled	1
AUD[1] AUD[0]	HSYNC VSYNC	# Do the audio function 0 - Audio for DP only 1 - Audio for HDMI # HDMI mode for HDMI/DP display is disabled 1 - Audio for both DP and HDMI # HDMI mode must be enabled on external monitors that are legally certified. It is the responsibility of the system designer to ensure that the system is enabled to support this feature.	XX
VIP_DEVICE_STRAP_DS	V2SYNC	VIP Device Strap Disabled 0 - Slave VIP host port device present 1 - No slave VIP host port device requires supporting presence	1
SMS_EN_HARD	H2SYNC	Reserved	0

CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
© 2007 Advanced Micro Devices

This AMD schematic and design is the exclusive property of AMD, and is provided only to assist under a non-disclosure agreement for the purpose of enabling you to prepare your own schematic and design. It is not intended for public use. It is strictly confidential and for your personal use only. You shall maintain its confidentiality and shall not disclose, copy, reproduce, or otherwise use it in any manner without the prior written consent of AMD. AMD makes no representations or warranties of any kind and shall not be responsible for any damages or losses, including any indirect or consequential damages or losses, arising from the use of any implied warranty of merchantability or fitness for a particular purpose, or any other damages or losses, including any indirect or consequential damages or losses, resulting from the use of the information included herein.

Advanced Micro Devices Inc.  
1 Commerce Valley Drive East  
Markham, Ontario

**AMD**

Date: Wednesday, February 24, 2010 Rev # 1  
Sheet 8 of 12

Title Cedar DDR3 Mm3.0 Doc No. 105-C077X-00B



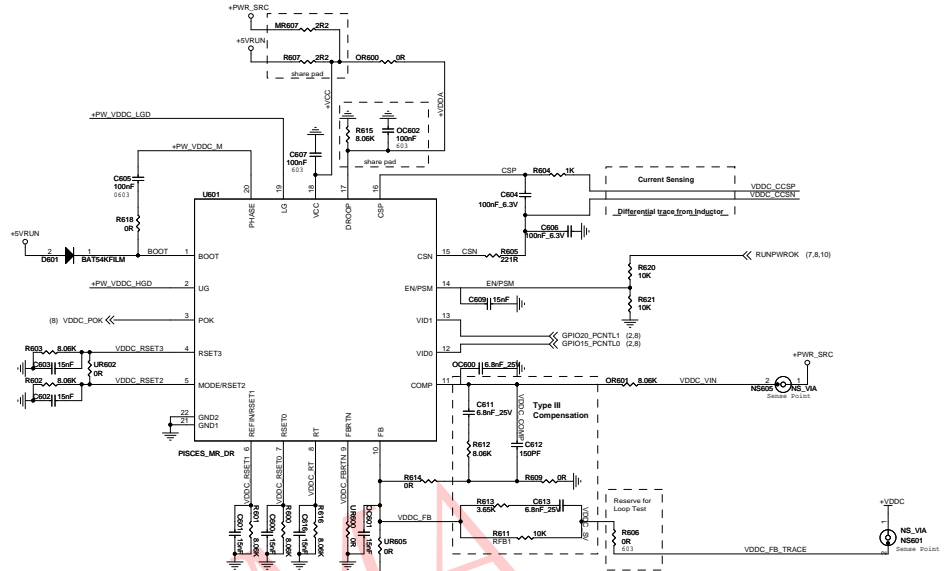
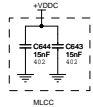


Figure 10 shows a schematic diagram of the power supply decoupling network. It features three capacitors in parallel with resistors, connected to a power supply. The components are labeled as follows:

- C639:** 330µF, SPIPOSCAP, SMT 7343, Hmax=1.5mm
- C640:** 330µF, SPIPOSCAP, SMT 7343, Hmax=1.5mm
- C641:** 220µF, SPIPOSCAP, SMT 7343, Hmax=1.2mm

The diagram also indicates the maximum allowed dimensions for the capacitors: Hmax=1.5mm for C639 and C640, and Hmax=1.2mm for C641.



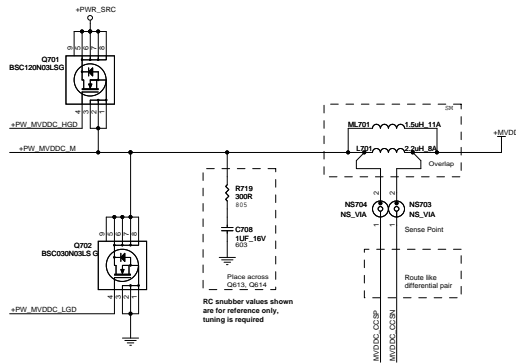
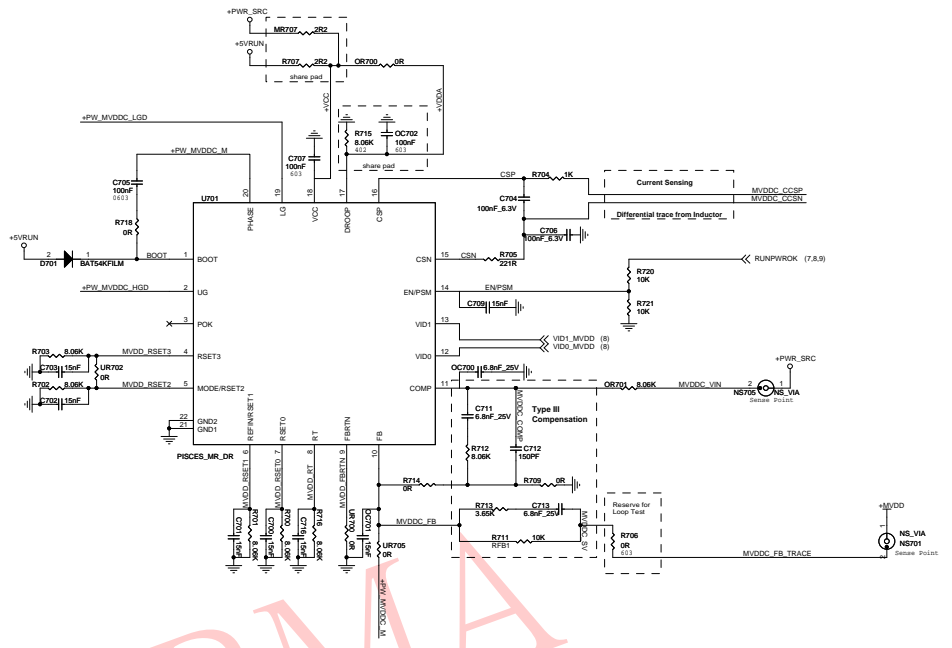

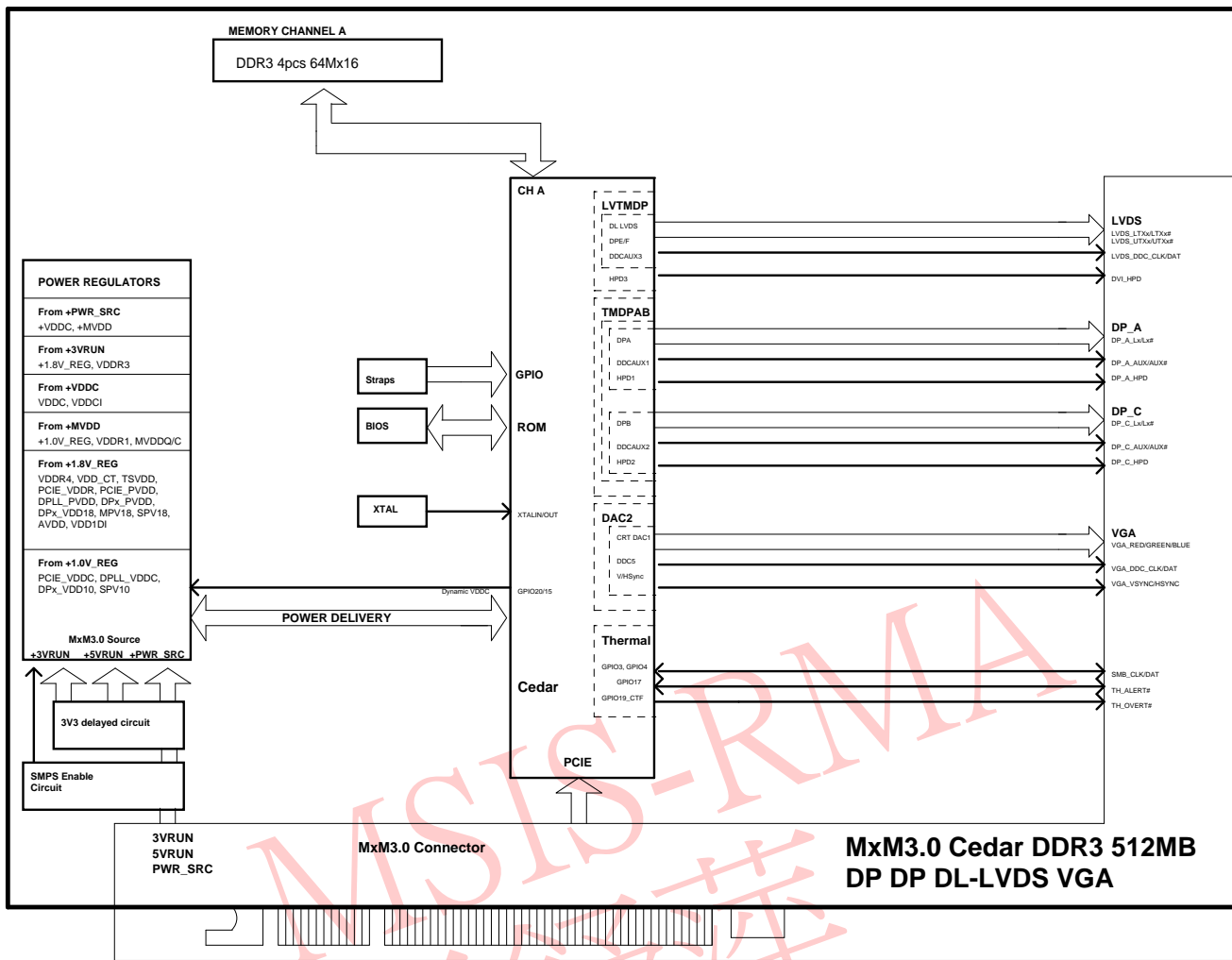


Figure 1 compares two capacitor types: a Low Profile POSCAP and an MLCC. The POSCAP (C737, 330µF) is shown with a height of 1.5mm. The MLCC (C741, 150µF) is shown with a height of 402. Both are connected to +MVDD and ground.



CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC. © 2007 Advanced Micro Devices The AMD Board schematic and design is the exclusive property of AMD, and is not to be used, copied or otherwise reproduced in any form without the prior written consent of AMD. This document is provided for your information purposes only and is not intended for general distribution. Use of this schematic and design for any purpose other than that intended by AMD is strictly prohibited. License Agreement for this evaluation requires a AMD Technology License Agreement. AMD makes no representations or warranties of any kind regarding the accuracy or completeness of the design, including but not limited to, any implied warranty of merchantability or fitness for a particular purpose. AMD shall not be held responsible for any consequences resulting from the use of the information included herein.		Advanced Micro Devices Inc. 1 Commonwealth Valley Drive East Markham, Ontario			
Date:	Wednesday, February 24, 2010	Rev:			
Sheet	10	of	12		
Title: Cedar D383 M3dM3.0				Doc No:	105-0077xoc-00B



**MxM3.0 Cedar DDR3 512MB**  
**DP DP DL-LVDS VGA**

CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
 © 2007 Advanced Micro Devices  
 The AMD Brand, logo, and design are the exclusive property of AMD.  
 All other trademarks are the property of their respective owners.  
 AMD and the AMD logo are registered trademarks of AMD.  
 AMD is not responsible for any damage or loss resulting from the use of this document.  
 AMD makes no representation or warranty of any kind regarding the accuracy or completeness of the information contained herein.  
 AMD makes no representation or warranty of any kind regarding the accuracy or completeness of the information contained herein.  
 AMD makes no representation or warranty of any kind regarding the accuracy or completeness of the information contained herein.

Advanced Micro Devices Inc.  
 1 Commerce Valley Drive East  
 Markham, Ontario



Date: Wednesday, February 24, 2010  
 Page: 1  
 Doc No: 405-C077xx-00B

<div>AMD</div>			Title		Schematic No.		Date:	
			Cedar DDR3 MxM3.0		105-C077xx-00B		Wednesday, February 24, 2010	
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.					Rev 1
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION					
0	00A	09/10/06	Initial design for Cedar DDR3 MxM3.0 Type A-4L					
1	00B	10/02/24	Layout change only (Move GPIO4_SMBCLK to the bottom layer)					
			<div>MSIS-RMA</div> <div>夏舒萍</div> <div>00712</div>					