

V133-10

P729: G96, DDR2 MEMORY 32MX16/16MX16

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REV HISTORY

- 04/02
- BOM modify
1. add R562,R563
2. Add FAN control  
remove R158  
add R158
3. add FBVDD MLCC CAP  
add C87,C101
4. add NVVDD OS-CON  
add C51
5. Change NVVDD compenation  
R310 = 10K , C306 = 330PF ,  
R314 =68ohm
6. Change DDC\_5V ADJ Resistance  
R153 =100ohm , R152 = 300ohm
7. Change common chock to 0 ohm  
remove L21,L22,L23,L24  
add R204,R205,R206,R207,R208  
add bridge R121,R122,R123,R124
- 04/02
8. Change NVVDD voltage to 1.00V  
Change R313 to 1.78K ohm
- 04/07
8. add R321,R322

REV	VARIANT	WVFN	ASSEMBLY
0	BASE	600-10729-xxxx-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10729-0000-000	G96-300-A1, 550/500MHz, 512MB 32mx16 DDR2 BGAB4 DVI-DL+VGA+HDTV
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P729 Overview

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changes to 3V3\_AUX

3V3\_AUX

3V3\_PEX

12V\_PEX

3V3\_PEX

PLACE NEAR FINGERS

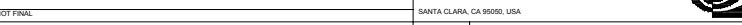
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IN	MAX_RISERCLK	PCK_BREQCLK	1	1000MHz
IN	PCK_REFCLK	PCK_BREQCLK	1	1000MHz
IN	GPU_TESTMODE		3	500UM

Net Name	MIN_LINE_WIDTH	VOLTAGE	MAX_CURRENT	
IN	PCK_PLYDD	32MIL	1.1V	0.12A
	PCK_CLK_00_10000			

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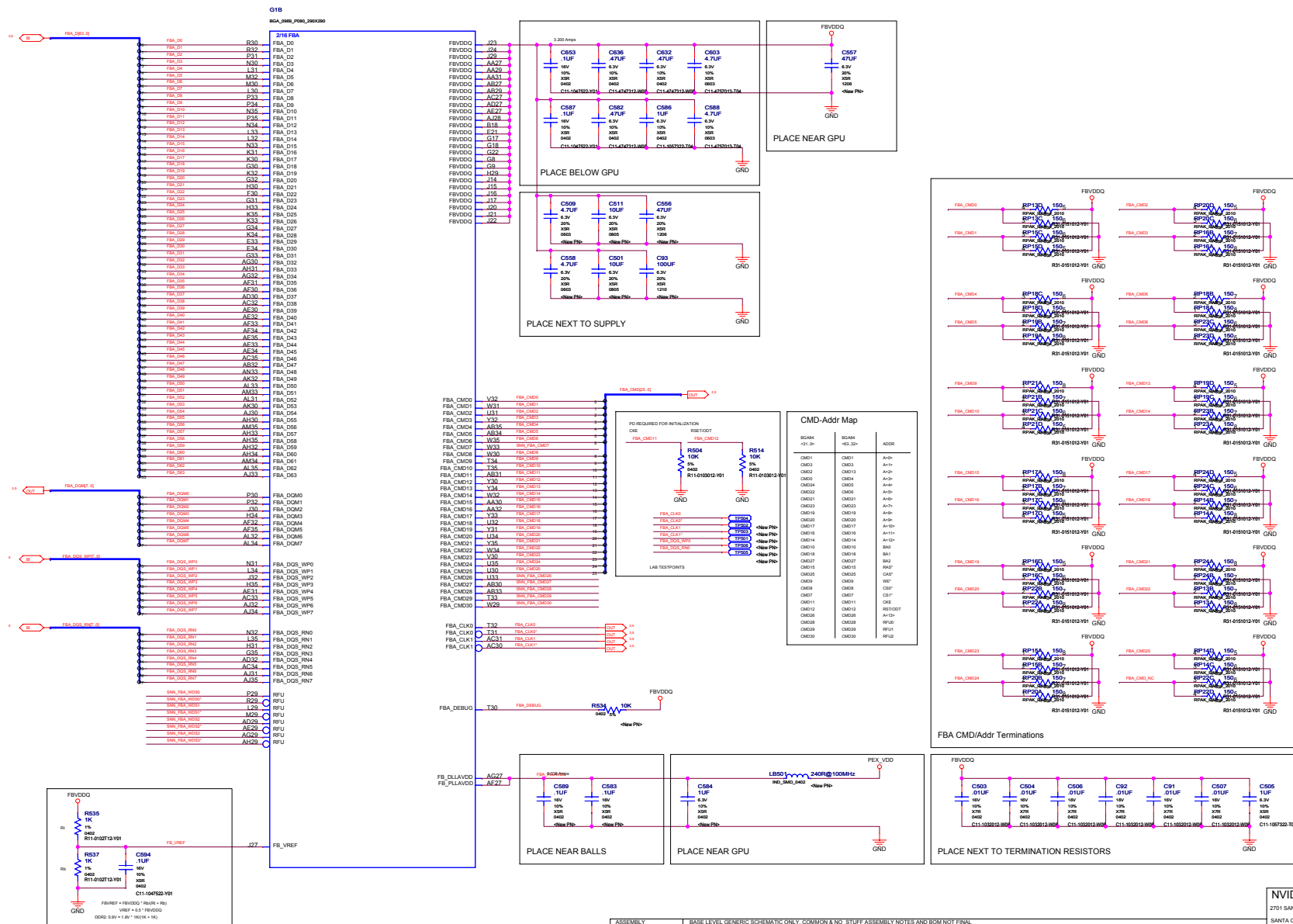
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## Partition A Frame Buffer Interface



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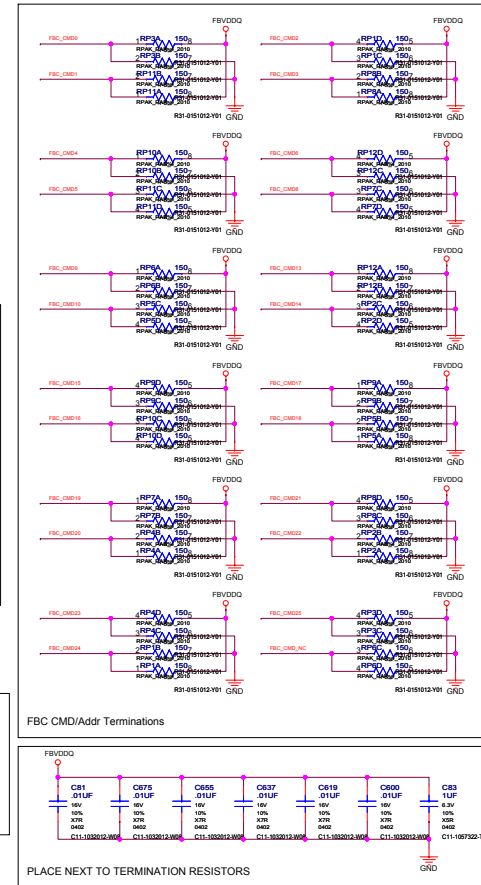
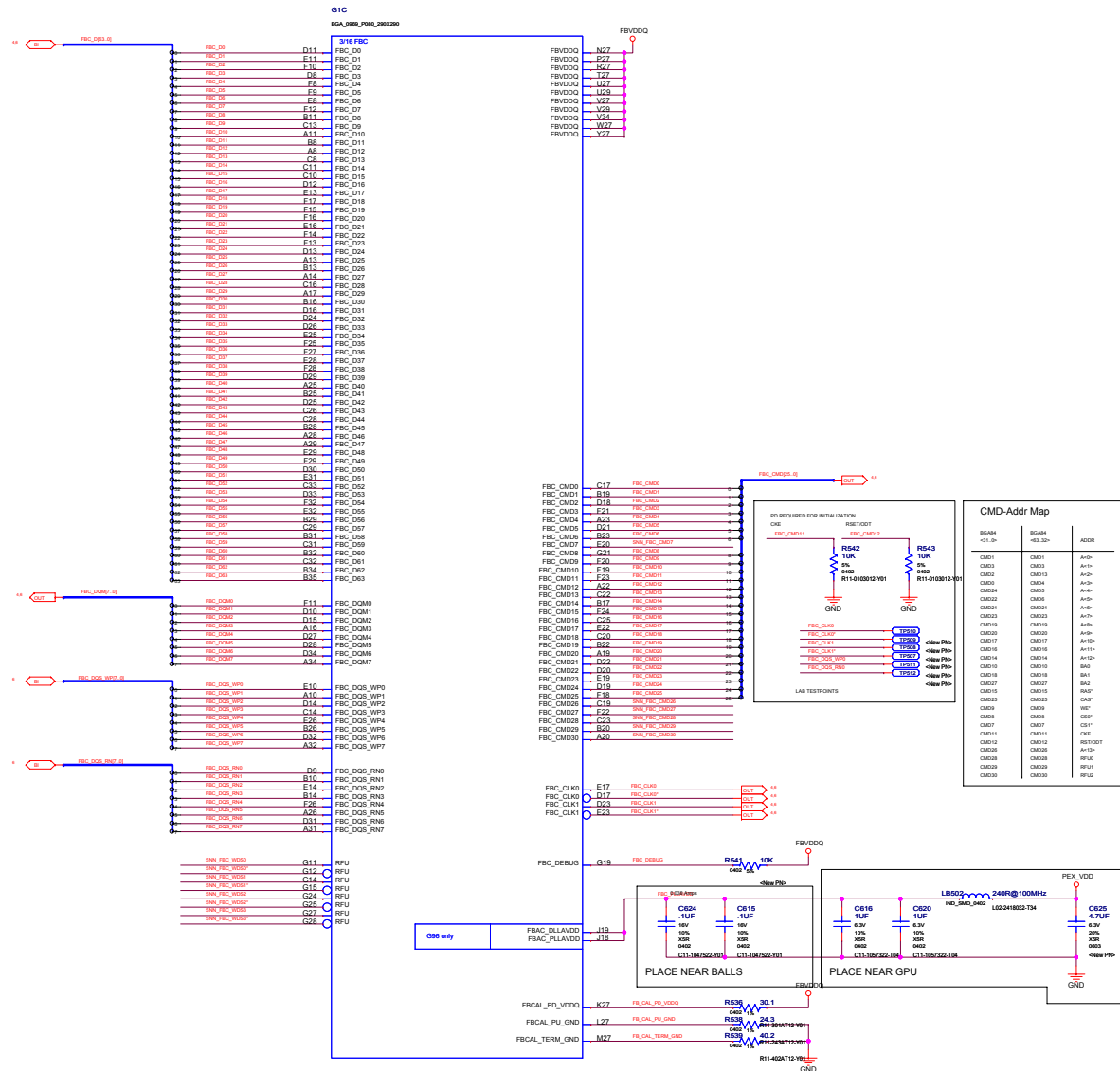


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## Partition C Frame Buffer Interface



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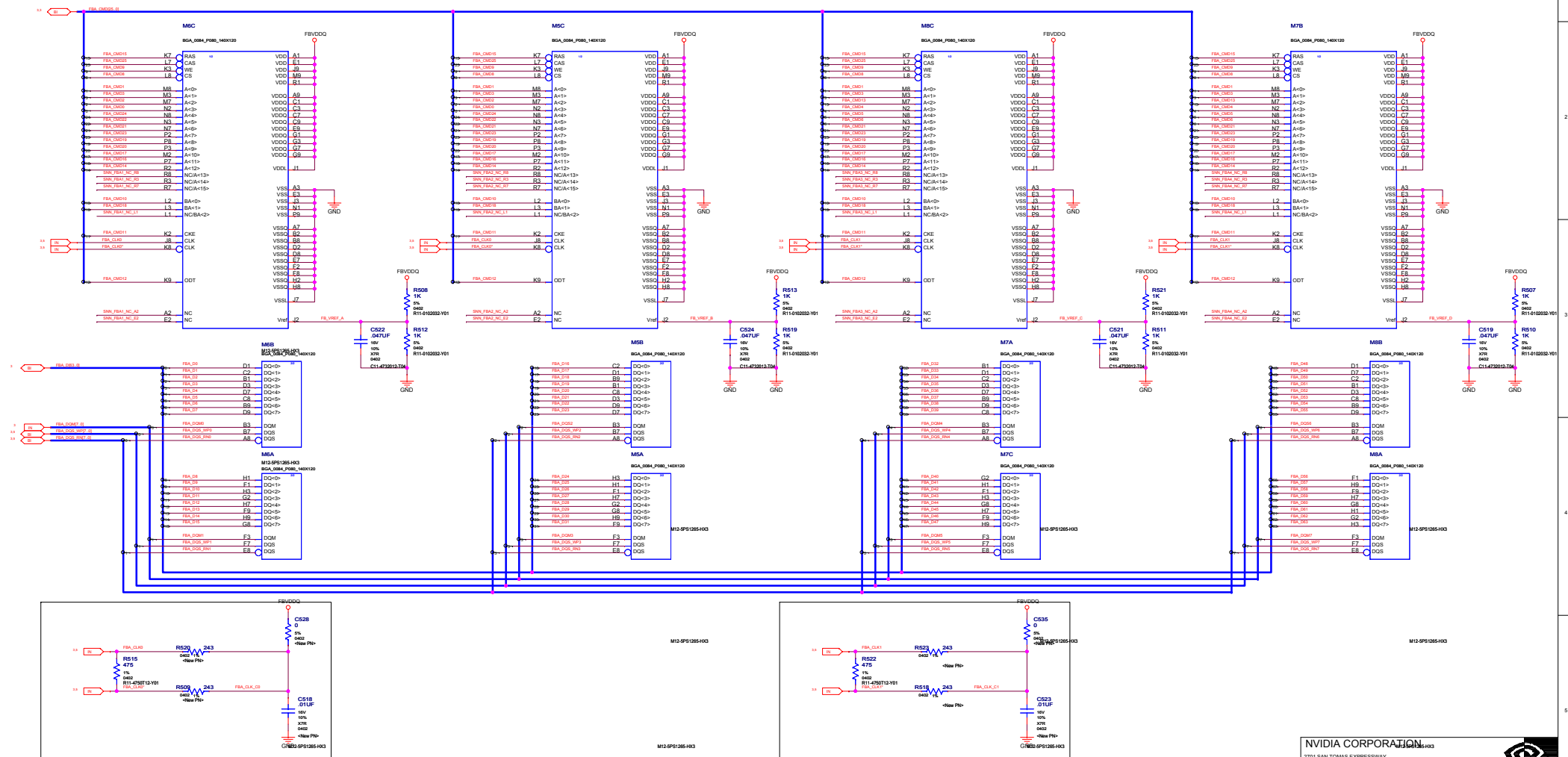
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PAGE DETAIL	Partition C Frame Buffer Interface

## Partition A Memories



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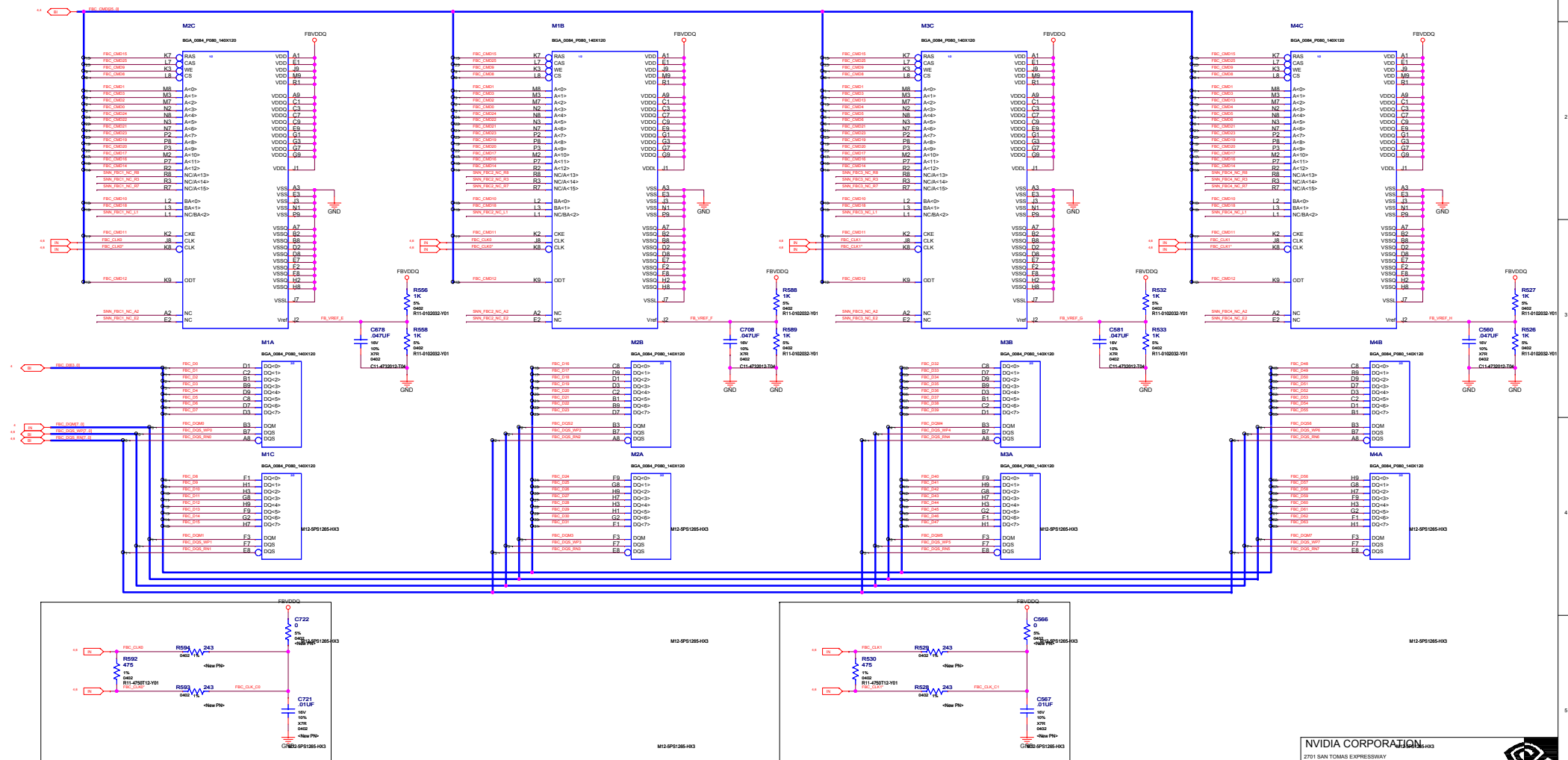
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# Partition C Memories



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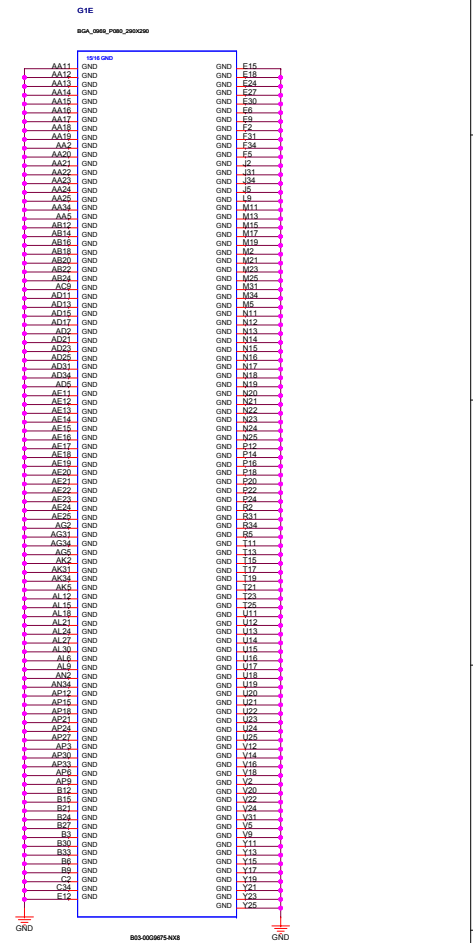
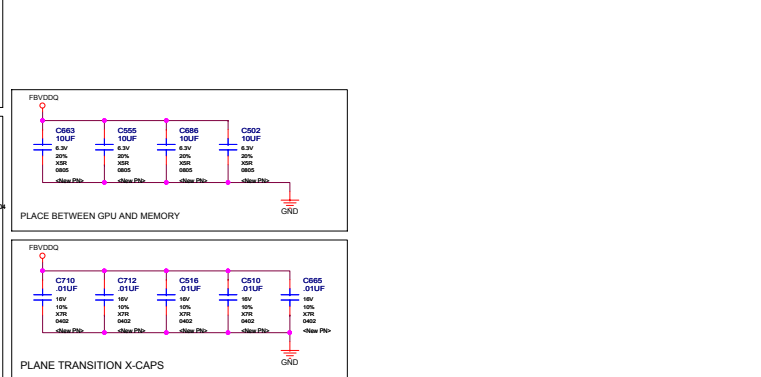
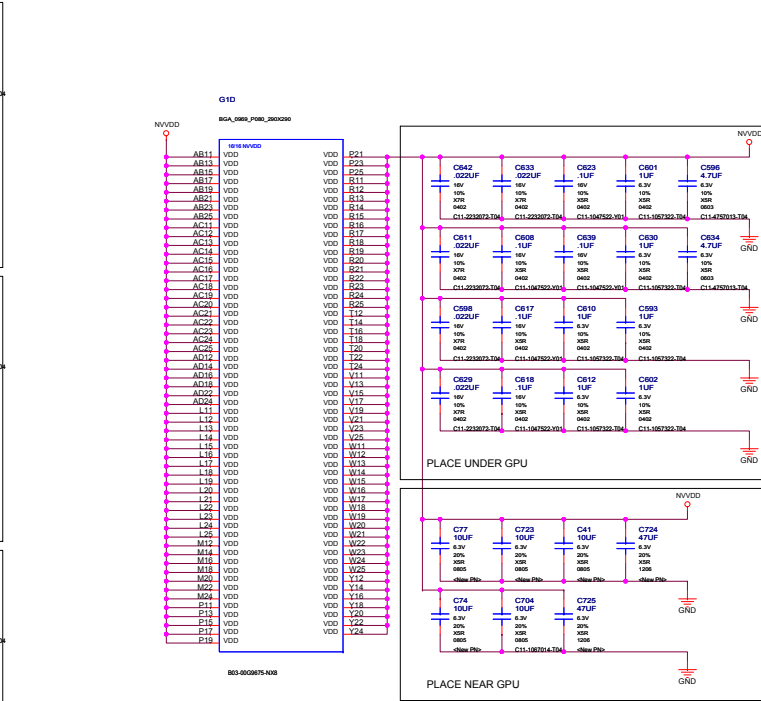
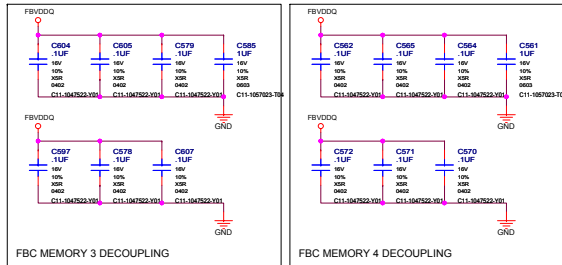
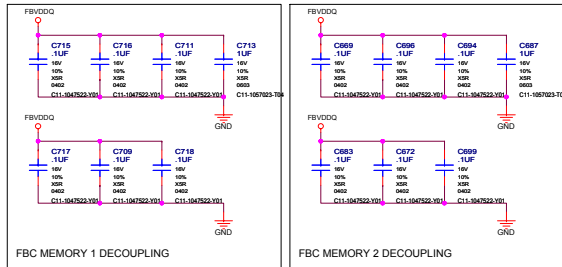
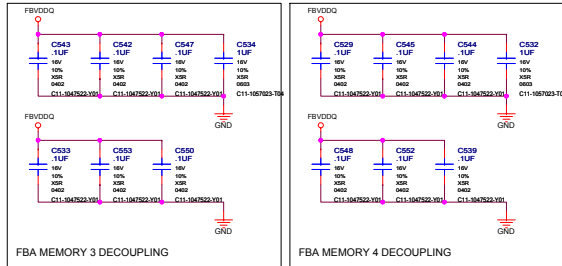
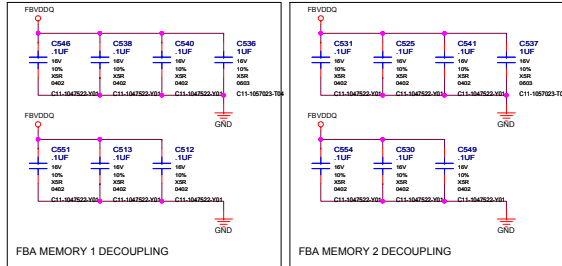


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PAGE DETAIL Partition C Memories

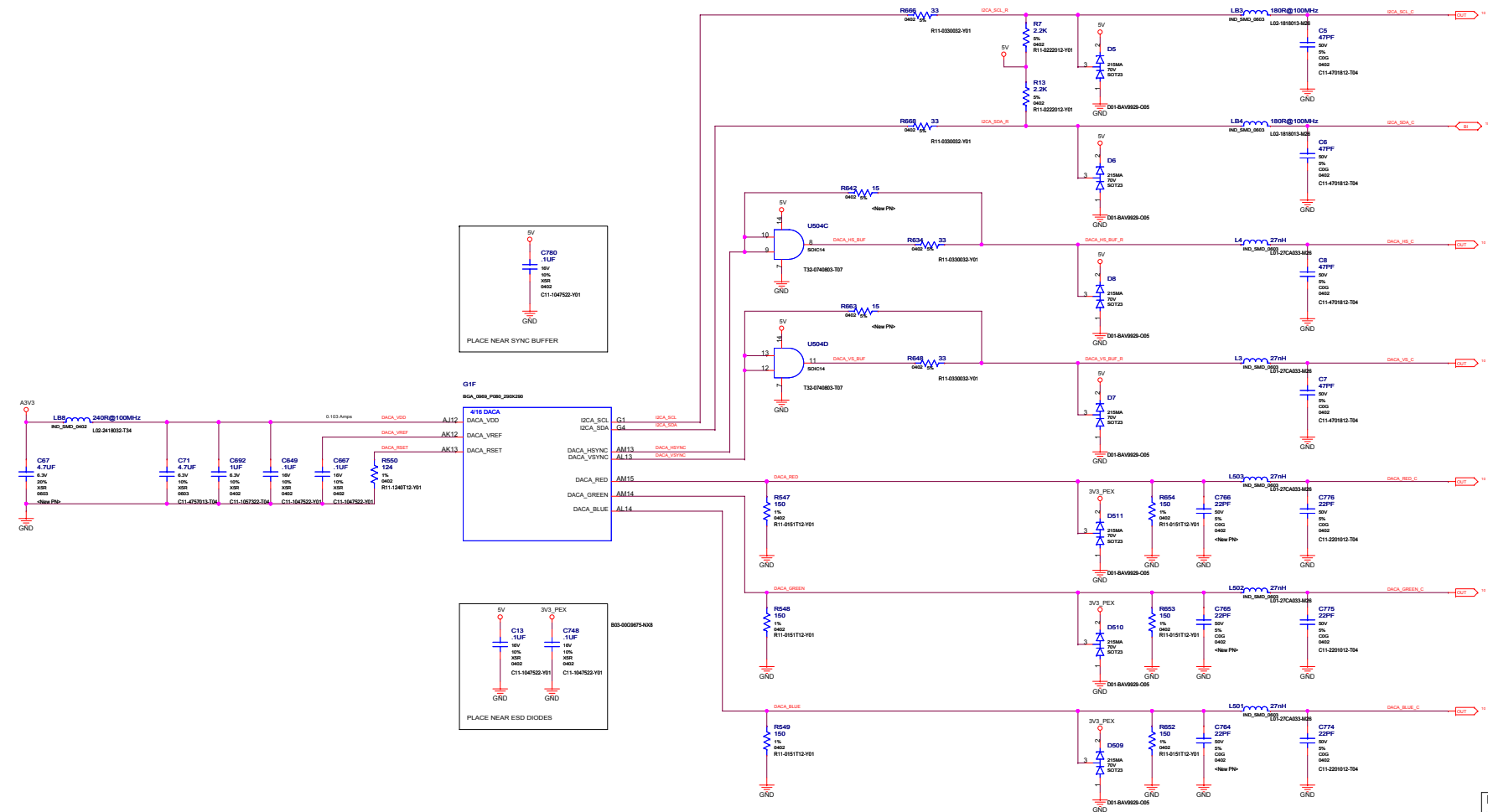
# Decoupling Caps




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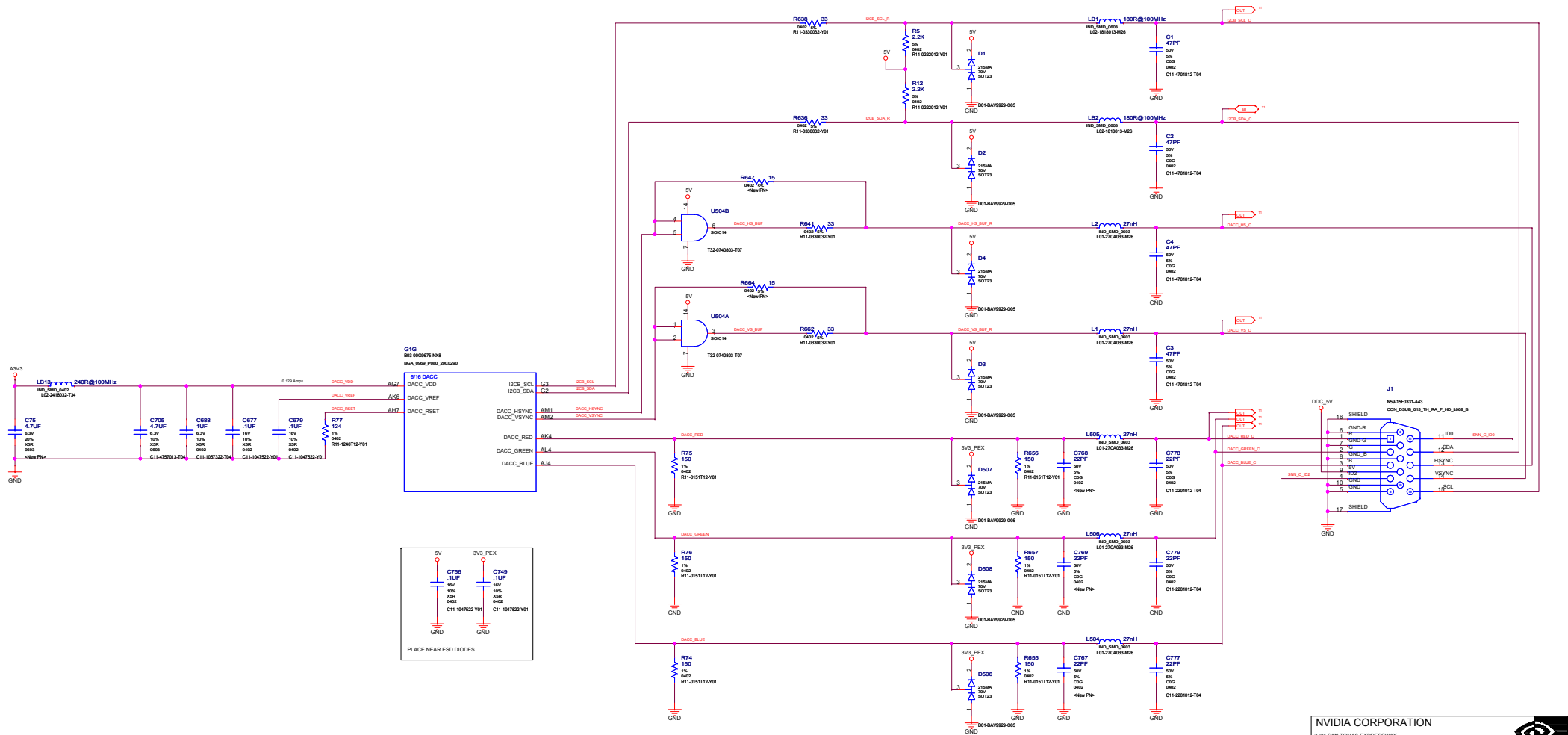
## DACA



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# DACC, Slim DB15 Connector



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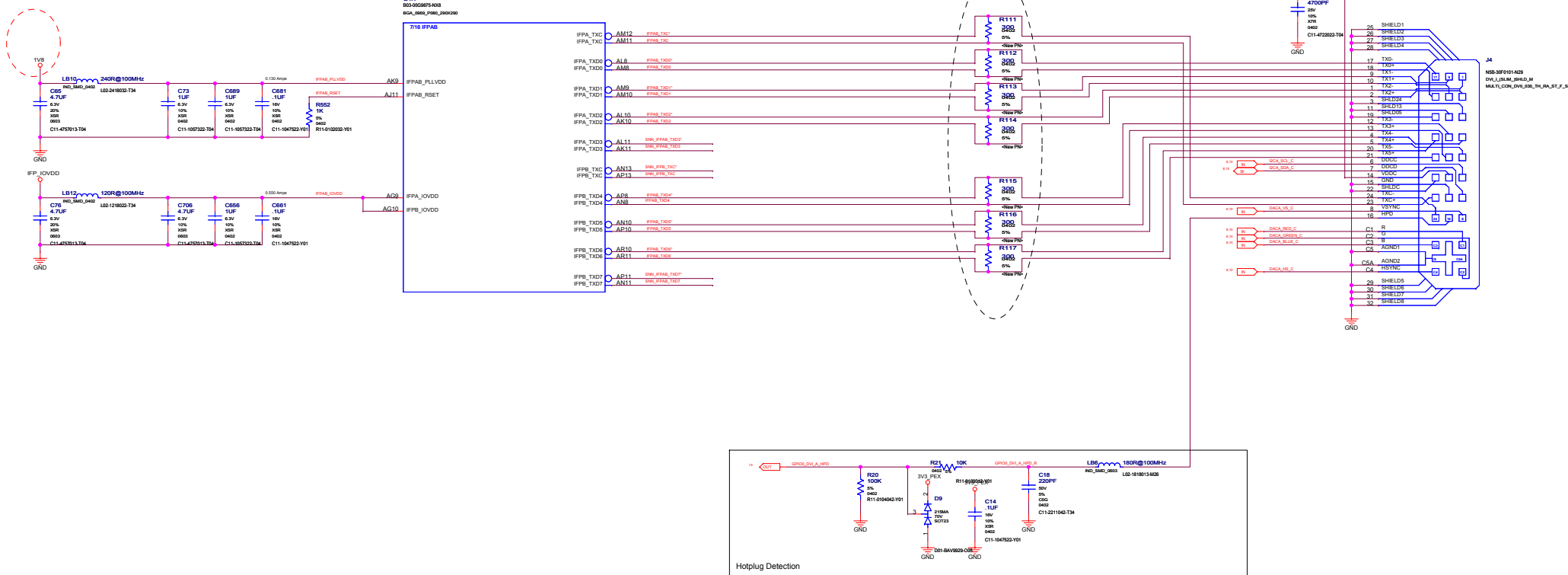
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PAGE DETAIL: DACC, Slim DB15 Connector

# Internal TMDS .. Link A & B

change FBVDDQ to 1V8



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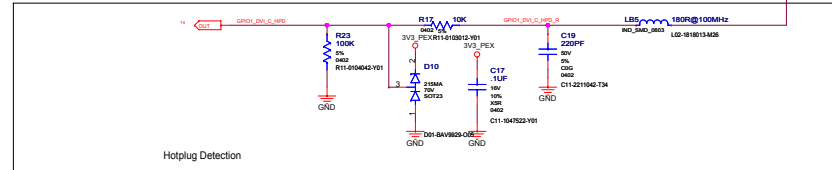
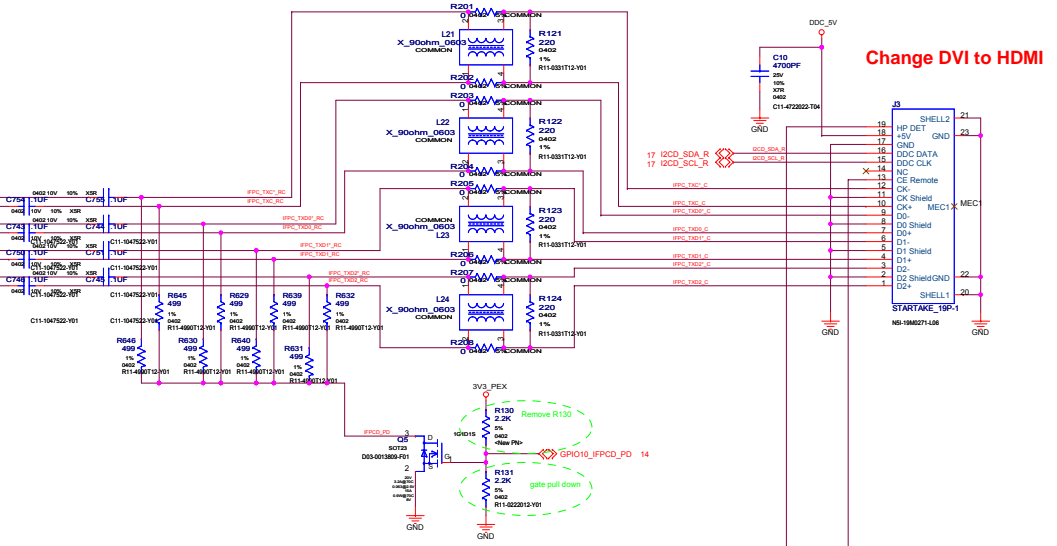
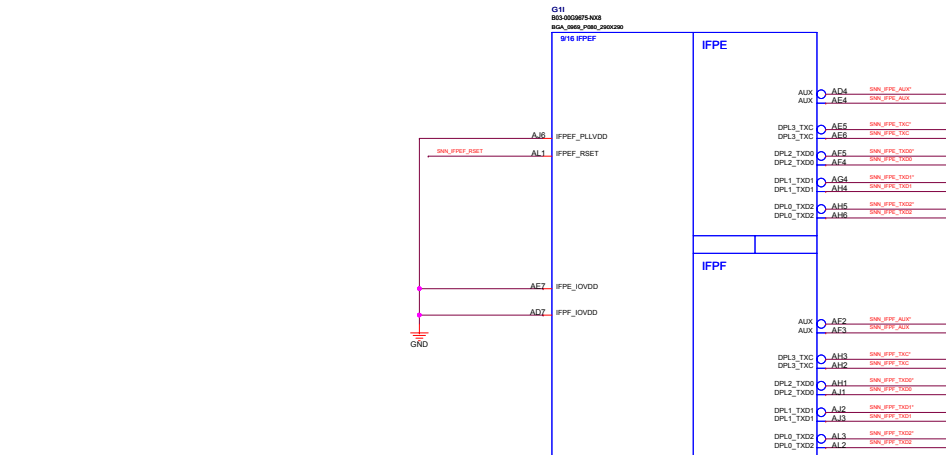
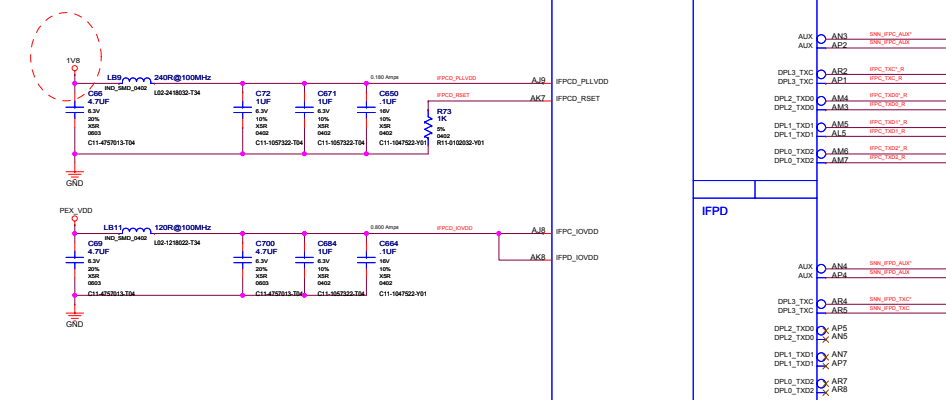
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PAGE DETAIL Internal TMDS .. Link A & B

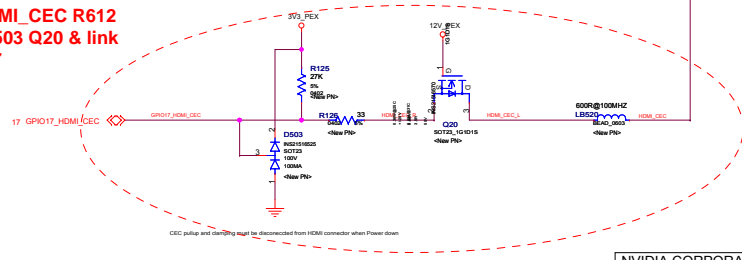
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# Internal TMDS .. Link C & D

change FBVDDQ to 1V8



Add HDMI\_CEC R612  
R613 D503 Q20 & link  
GPIO 17



Change DVI to HDMI

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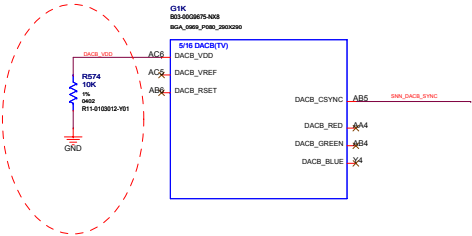
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PAGE DETAIL Internal TMDS .. Link C & D

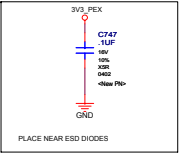
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DACB, MINIDIN Connector

Change R574 to 10K



Remove TV-OUT

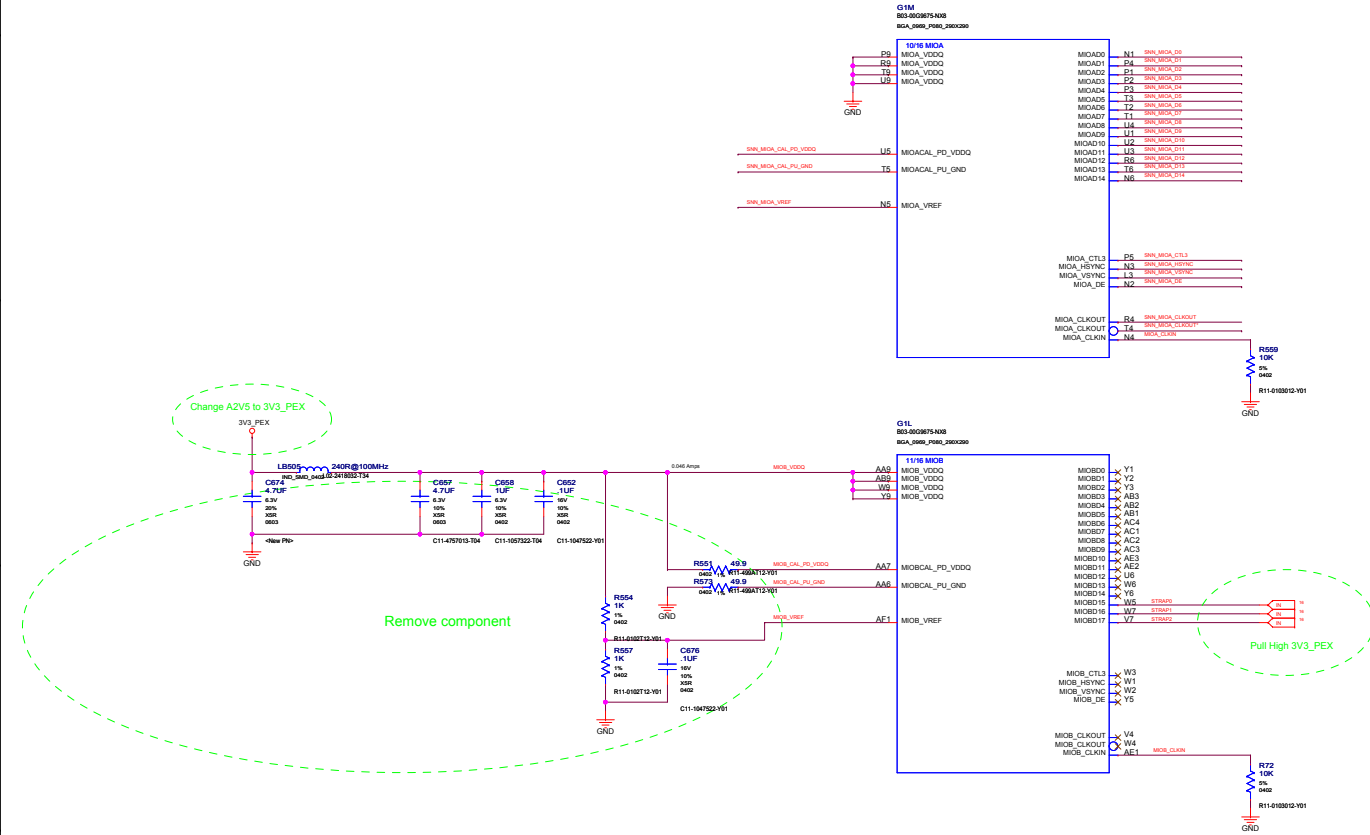


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PAGE DETAIL	DACB, MINIDIN Connector

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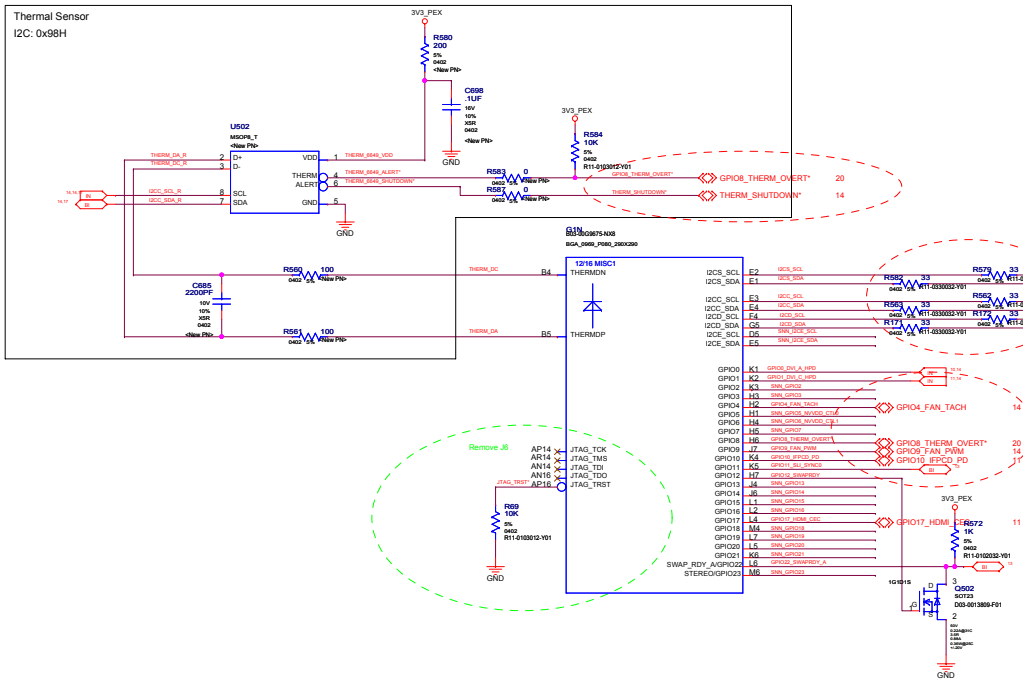
MIOA, MIOB Interface



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# Thermal Sensors, GPIOs, XTAL, JTAG, Fan



Add R171 R172 R173 R174  
I2CD\_SCL & I2CD\_SDA

Thermal protection

change Thermal protection

Change Q23 Q24 Q25 to BJT

Add 2-pin Fan Control

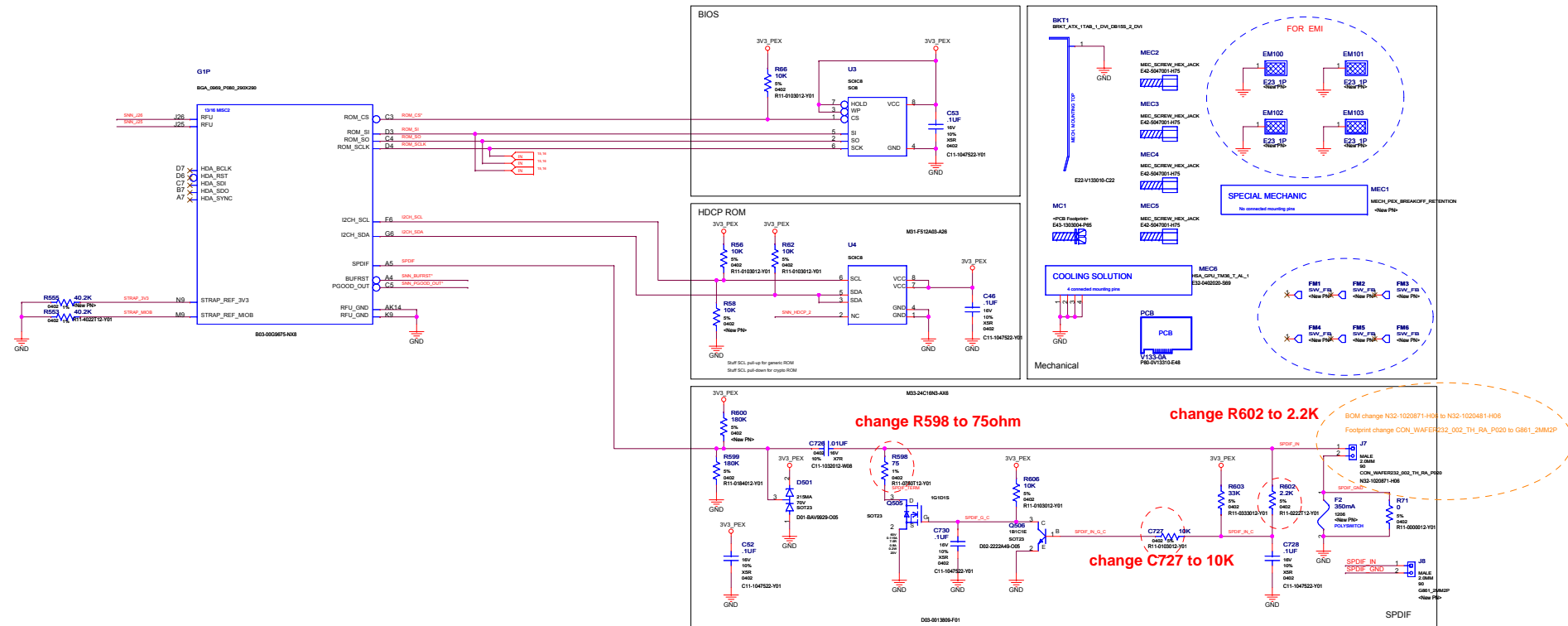
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## BIOS, HDCP, SPDIF, HDA, Mechanical



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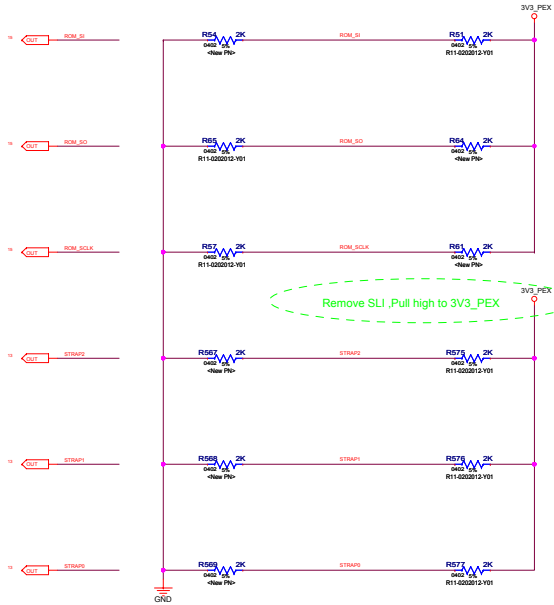
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PAGE DETAIL	BIOS, HXCP, SPDIF, HDA, Mechanical

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# Straps



## G94 Straps Multilevel Mode

Bit Signal

Values

03	ACLK_277	0 DISABLE 1 ENABLE
02	TWADD2	000 N75C_A 001 N75C_J
01	TWADD1	010 PAL_M 011 PAL_N 100 PAL_CK 101 PAL_BCD0 110 BBSER_VDD0 111 BBSER_VDD1
00	TWADD0	
03	PCL_DEV0_EXT	1 G06-300-A1
02	SUB_VENDOR	0 NO BIOS 1 BIOS
01	SLCT_CLK_CFG	0 DISABLE 1 ENABLE
00	PEX_PUL_DLA_TERM100	0 DIS 1 EN

### Multilevel Straps

5K to GND	0000
10K to GND	0001
15K to GND	0010
20K to GND	0011
25K to GND	0100
30K to GND	0101
35K to GND	0110
40K to GND	0111
5K to VCC	1000
10K to VCC	1001
15K to VCC	1010
20K to VCC	1011
25K to VCC	1100
30K to VCC	1101
35K to VCC	1110
40K to VCC	1111

03:	RAMCFG0	0000 32Mx16/16Mx16 DDR2 128-bit Elpida 0001 16Mx16 DDR2 128-bit Samsung, Micron 0010 16Mx16 DDR2 128-bit Hynix 0011 16Mx16 DDR2 128-bit Hynix 0100 32Mx16/16Mx16 DDR2 128-bit Hynix 0101 32Mx16/16Mx16 DDR2 128-bit Samsung 0110 32Mx16/16Mx16 DDR2 128-bit Hynix 0111 32Mx16/16Mx16 DDR2 128-bit Hynix	1000 32Mx16/16Mx16 DDR2 64-bit Elpida 1001 16Mx16 DDR2 64-bit Samsung, Micron 1010 16Mx16 DDR2 64-bit Hynix 1011 16Mx16 DDR2 64-bit Hynix 1100 32Mx16/16Mx16 DDR2 64-bit Hynix 1101 32Mx16/16Mx16 DDR2 64-bit Samsung 1110 32Mx16/16Mx16 DDR2 64-bit Hynix 1111 32Mx16/16Mx16 DDR2 64-bit Hynix
02:	RAMCFG1		
01:	RAMCFG2		
00:	RAMCFG3		

0111 32Mx16 DDR2 128-bit Hynix

03	PCL_DEV00	0001 G06-300-A1	
02	PCL_DEV01		
01	PCL_DEV02		
00	PCL_DEV03		
03	SGIO_PANDCFG_LUT_ADR0	0000 GSKTOP_DEFAULT 0001 MOBILE_JTTRES_DEFAULT 0010 MOBILE_JTTRES_LLAMP 0011 MOBILE_JTTRES_LLAMP 0100 MOBILE_JTTRES_HAMP 0101 MOBILE_JTTRES_HAMP 0110 MOBILE_JTTRES_HAMP 0111 MOBILE_JTTRES_HAMP	1000 GSKTOP_JTTRES 1001 MOBILE_JTTRES_HAMP 1010 MOBILE_JTTRES_LLAMP 1011 MOBILE_JTTRES_LLAMP 1100 MOBILE_JTTRES_HAMP 1101 MOBILE_JTTRES_HAMP 1110 MOBILE_JTTRES_HAMP 1111 MOBILE_JTTRES_HAMP
02	SGIO_PANDCFG_LUT_ADR1		
01	SGIO_PANDCFG_LUT_ADR2		
00	SGIO_PANDCFG_LUT_ADR3		
03	USER0	0000 DEFAULT	
02	USER1		
01	USER2		
00	USER3		

## G94 Straps Binary-Bringup Mode

Bit Signal

Values

SUB_VENDOR	0 NO BIOS 1 BIOS
SLCT_CLK_CFG	0 DISABLE 1 ENABLE
SGIO_PANDCFG_LUT_ADR0	0000 GSKTOP_DEFAULT 0001 MOBILE_JTTRES 0010 MOBILE_JTTRES_LLAMP 0011 MOBILE_JTTRES_LLAMP 0100 MOBILE_JTTRES_HAMP 0101 MOBILE_JTTRES_HAMP 0110 MOBILE_JTTRES_HAMP 0111 MOBILE_JTTRES_HAMP
SGIO_PANDCFG_LUT_ADR1	1000 GSKTOP_JTTRES 1001 MOBILE_JTTRES_HAMP 1010 MOBILE_JTTRES_LLAMP 1011 MOBILE_JTTRES_LLAMP 1100 MOBILE_JTTRES_HAMP 1101 MOBILE_JTTRES_HAMP 1110 MOBILE_JTTRES_HAMP 1111 MOBILE_JTTRES_HAMP
SGIO_PANDCFG_LUT_ADR2	
SGIO_PANDCFG_LUT_ADR3	

## G94 Straps Binary-Production Mode

Bit Signal

Values

SLCT_CLK_CFG	0 DISABLE 1 ENABLE
PCL_DEV00_EXT	10 G06-300-A1
PCL_DEV00	
RAMCFG0	000 32Mx16/16Mx16 DDR2 E6xxx 001 16Mx16 DDR2 Samsung, Micron 010 16Mx16 DDR2 G4xxx 011 16Mx16 DDR2 Hynix 100 32Mx16/16Mx16 DDR2 Hynix 101 32Mx16/16Mx16 DDR2 Samsung 110 32Mx16/16Mx16 DDR2 G4xxx 111 32Mx16/16Mx16 DDR2 Hynix
RAMCFG1	
RAMCFG2	
RAMCFG3	

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ASSEMBLY	BASIC LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	50/50

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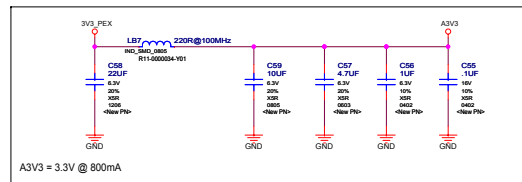
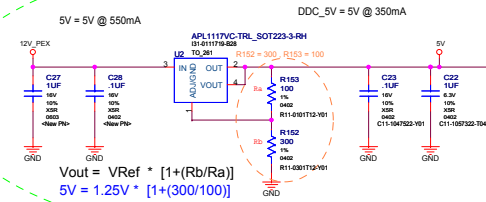


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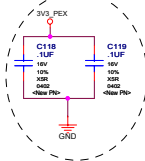
Power Supply I: 2V5, 3V3, 5V, IFP\_IOVDD

## Change DDC\_5V circuit

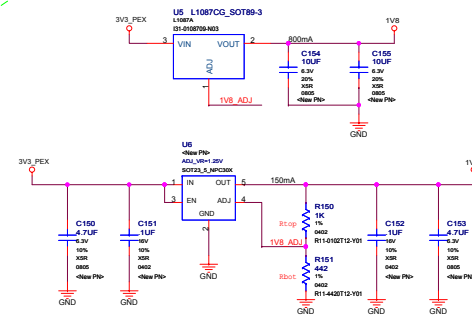


A3V3 = 3.3V @ 800mA

Add EMI CAP x 2pcs  
3V3\_PEX to GND

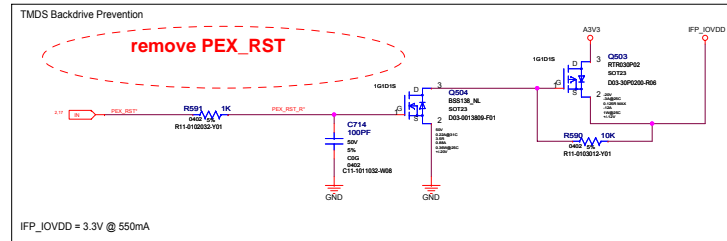


### Change 1V8 circuit



$$V_{out} = V_{Ref} * [1 + (R_{bot}/R_{top})]$$

$$1.8V = 1.25V * [1 + (442/1000)]$$



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply 1: 2V5, 3V3, 5V, IFF_J0VDD

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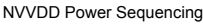
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## Power Supply III: NVVDD, PEX\_VDD



## Change Q31 Q32 to BJT

