

NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X  
PCI DEVICE ID 0X0=0X200 FOR NV20.

NVVD SET TO: 1.52V  
FBVDD SET TO: 3.47V  
FBVDDQ SET TO: 2.59V

HISTORY REVISION:

X00: Based on P50-A06  
- See change list in 149- file.  
- Set FBVDDQ=2.59V

P50-A07-X01:  
- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

P50-A08:  
X04: - Delay PLL\_VDD to come up after NVVD.  
X05: - Added 1UF across R257.  
X06: - Removed X04-5 above, added a switcher generated PLL delay option.  
- SSENNA cap for 2nd SW changed to 1UF.  
- A05 SI, NVVD=1.52V

P50-A09:  
X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.  
X03: - Added option to pull up power good to 12V

EC01235: - Changed R841 PU to 10K (from 4.7K)

EC01373: - Moved 75 ohm termination closer to filter for noise level reduction.  
Replaced C303,306,309 with 75ohm and no stuffed R208-210.

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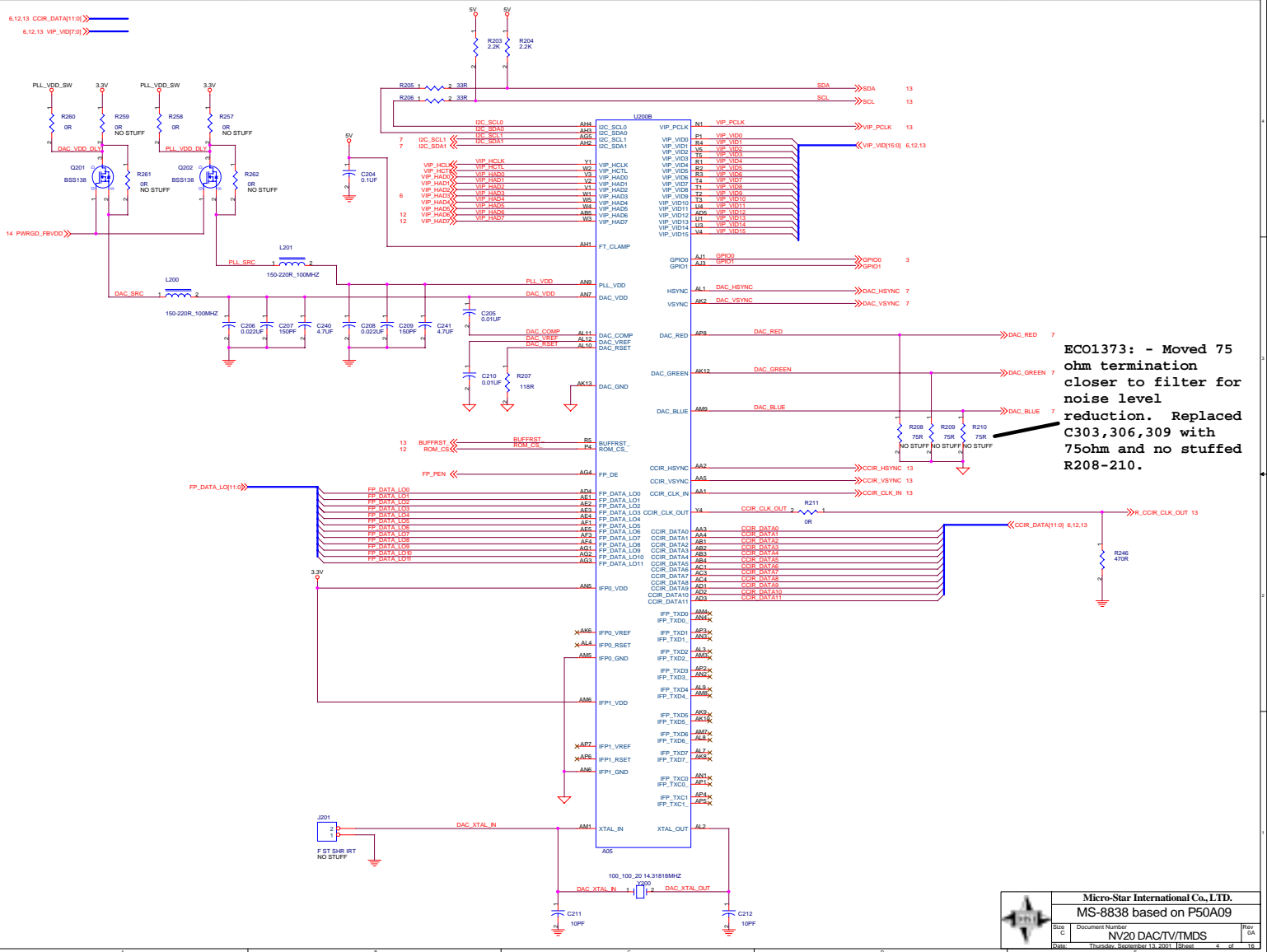
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[[assembly]]\[[source package]] [[value]]\[[top of page]]\[[reference]]\[[source package]]\[[value]]\[[assembly]]

In all cases each capacitor should be low ESR/ESL and placed as close as possible to the respective rail connector pin(s).

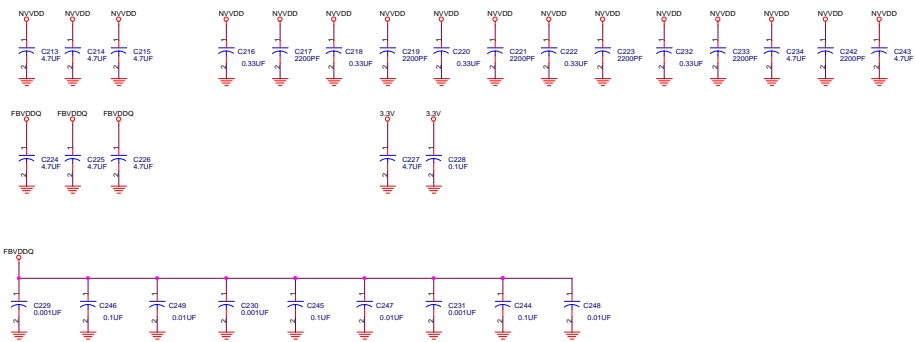
A trace across the 2 resistor pads can be cut to enable A0722 mode for debug.



6,12,13 CCR\_DATA[11:0] >>>  
6,12,13 VIP\_VID[7:0] >>>

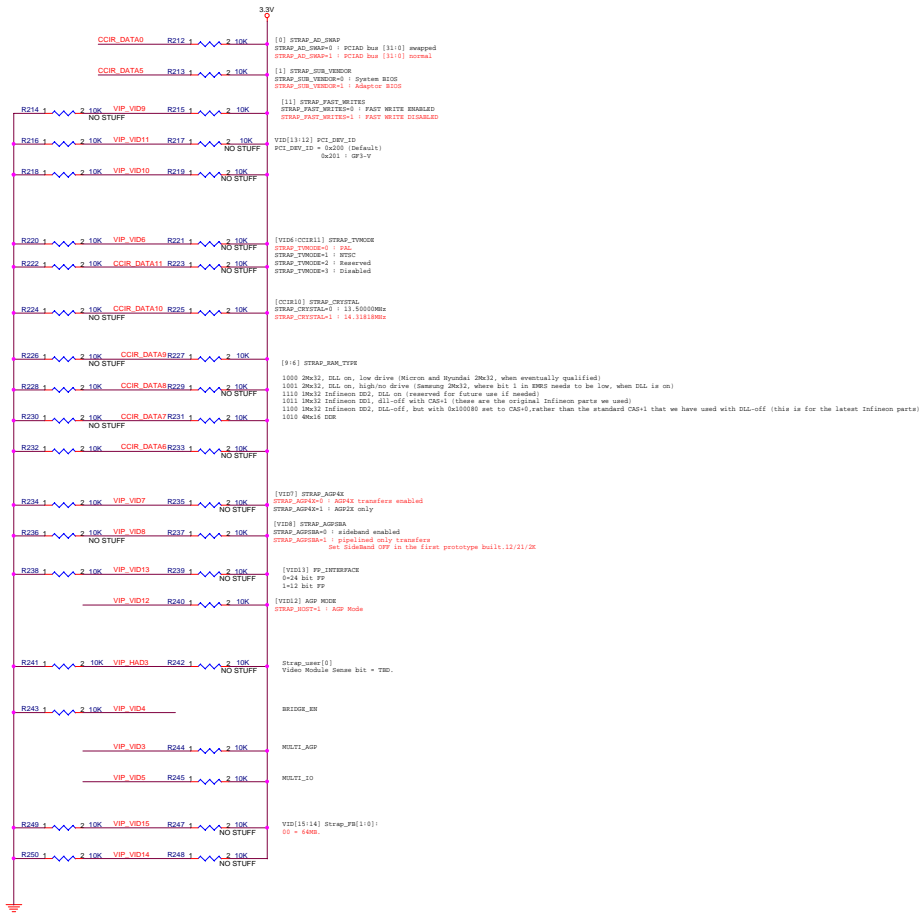


Use thick (non-impedance controlled) traces on XTALIN/OUT

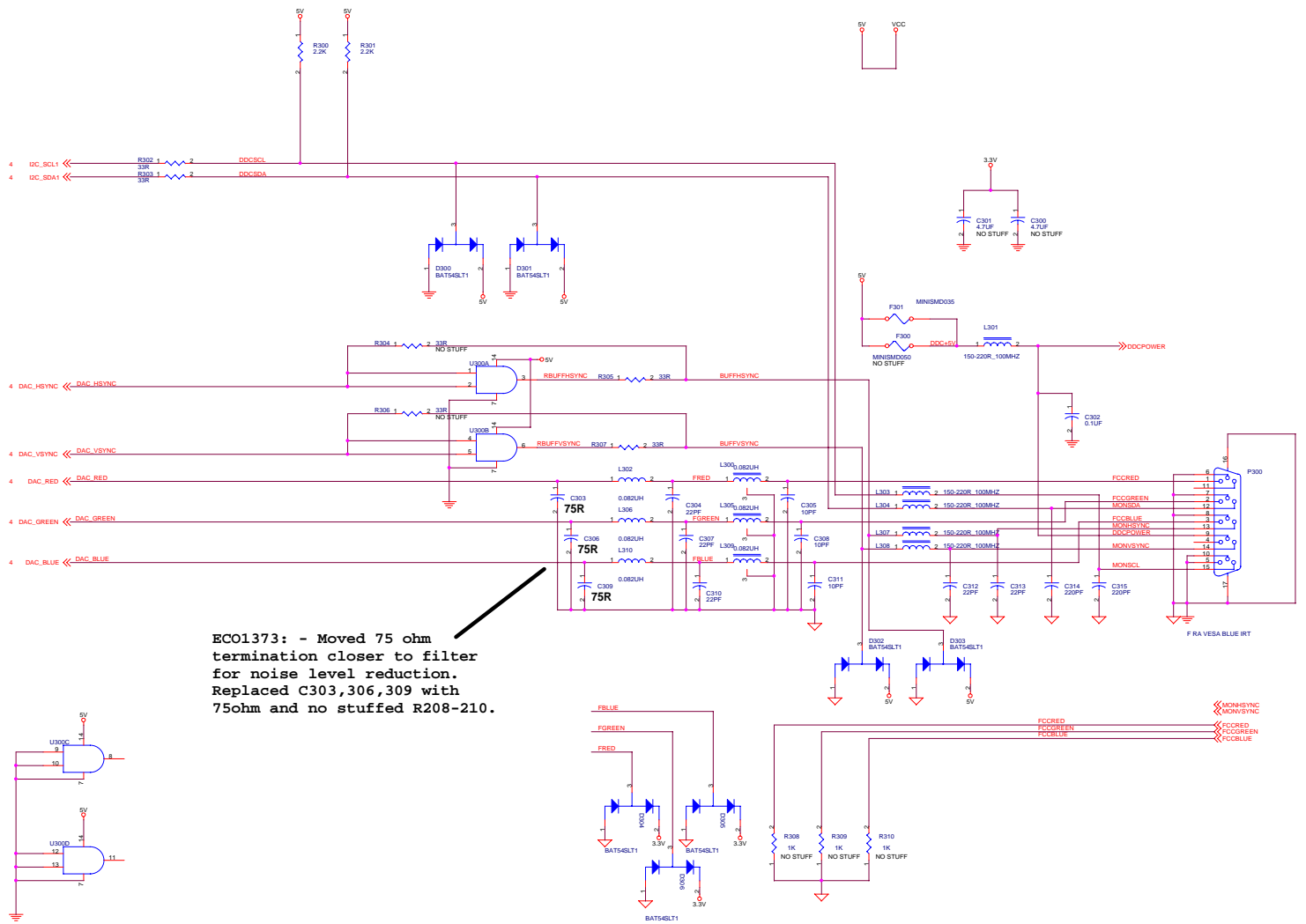


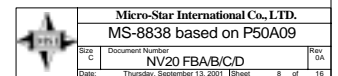
4.12.13 CCIR\_DATA[11:0]  
4.12.13 VIP\_VID[15:0]  
4 FP\_DATA\_LQ[11:0]

4 VIP\_HAD[0]  
4 VIP\_HAD[1]  
4 VIP\_HAD[2]  
4 VIP\_HAD[3]  
4 VIP\_HAD[4]  
4.12 VIP\_HAD[5]  
4.12 VIP\_HAD[6]

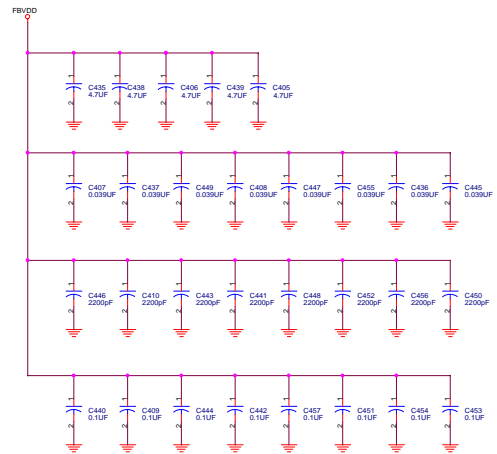
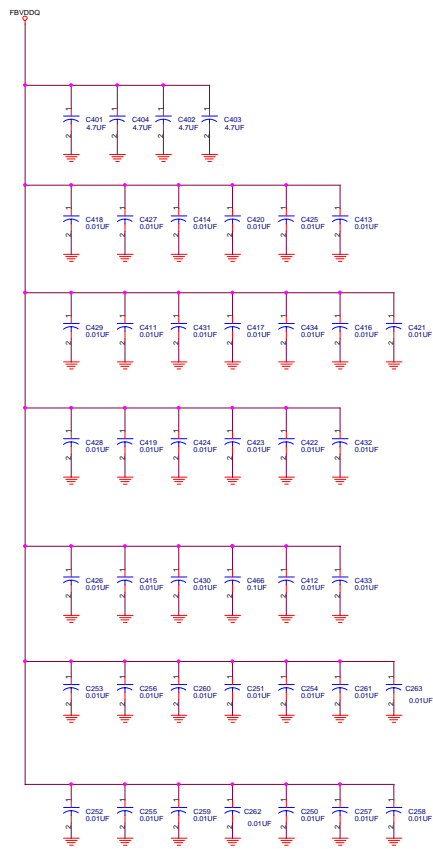


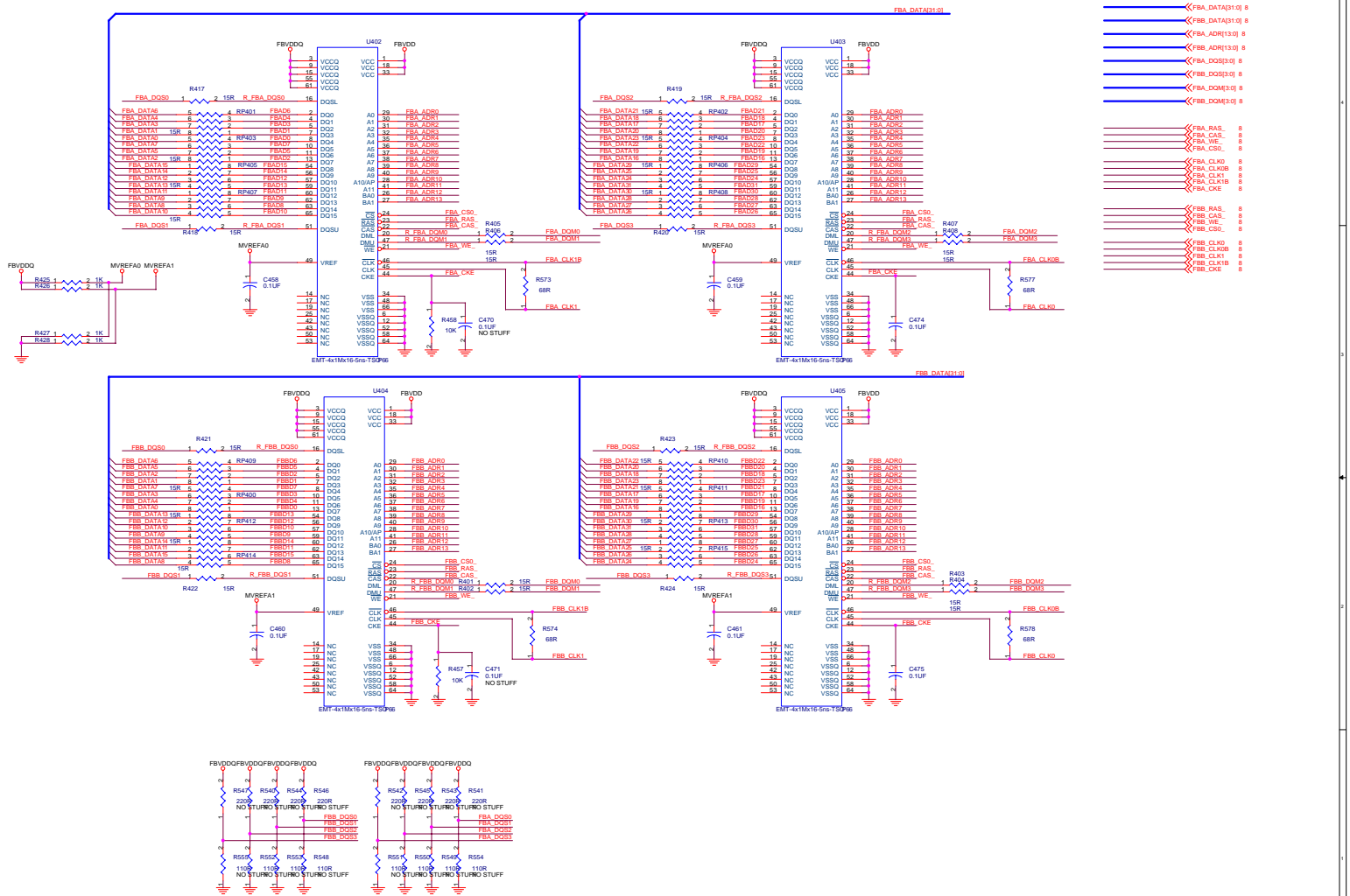
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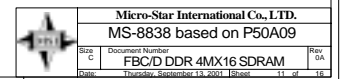




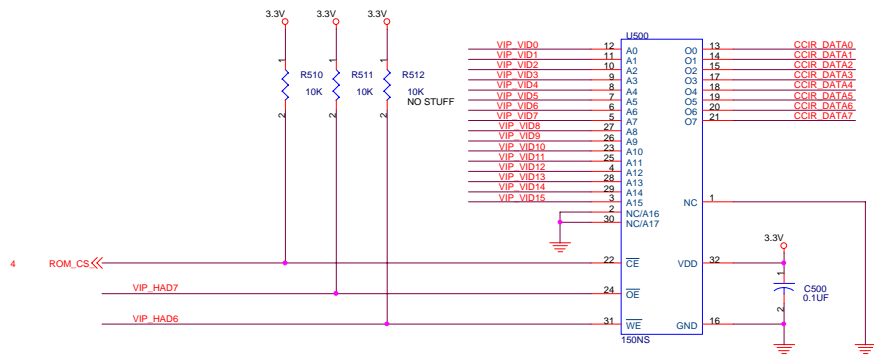






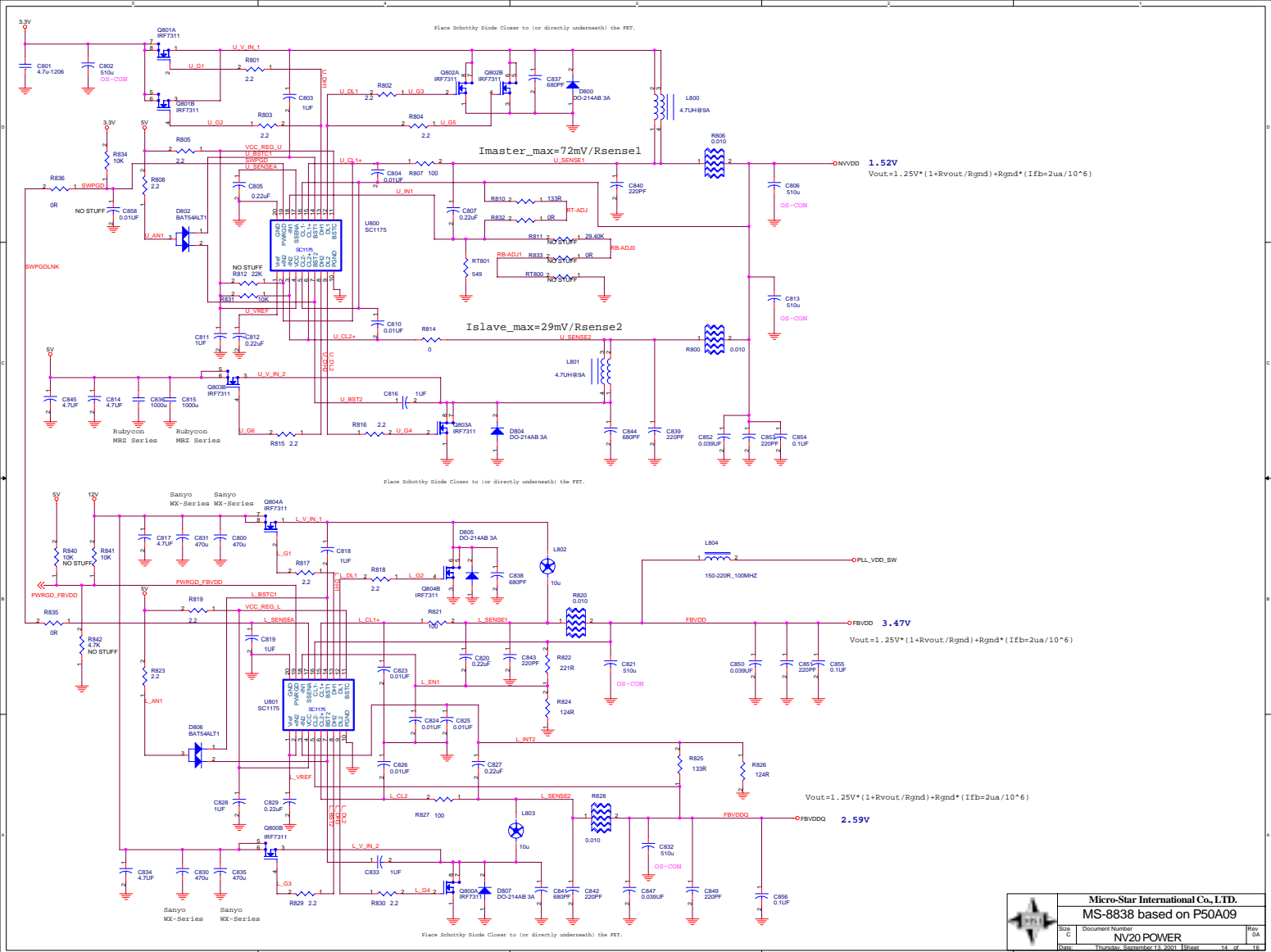


4,6,13 VIP\_VID[15:0] >>  
 4,13 VIP\_PCLK <<  
 4 VIP\_HCLK <<  
 4 VIP\_HCTL <<  
 4 VIP\_HAD0 >>  
 4 VIP\_HAD1 >>  
 4 VIP\_HAD2 >>  
 4,6 VIP\_HAD3 >>  
 4 VIP\_HAD4 >>  
 4 VIP\_HAD5 >>  
 4 VIP\_HAD6 >>  
 4 VIP\_HAD7 >>  
 4,6,13 CCIR\_DATA[11:0] >>  
 4,13 CCIR\_HSYNC <<  
 4,13 CCIR\_VSYNC <<  
 4,13 CCIR\_CLK\_IN <<  
 4,13 R\_CCIR\_CLK\_OUT <<  
 4,13 BUFRST\_ <<  
 4,13 SCL <<  
 4,13 SDA <<



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