ARTX2070-8L

History

1. add L18 with co-aly res. (11/6)
2. Remove USB power sense(11/11)
3. Remove 5V pwm ic option(11/12)
4. Remove PTC and FBVDDQ PH2 INPUT OPTION (11/14)
5. Remove 1V8_MAIN output option parts(11/14)
6. Remove J15 and parts(11/16)
7. Remove Input Power Balancing Switcher(11/16)

PG160-B02 8GB GDDR6, 256b, X16
DP + DP + HDMI/DP + DP

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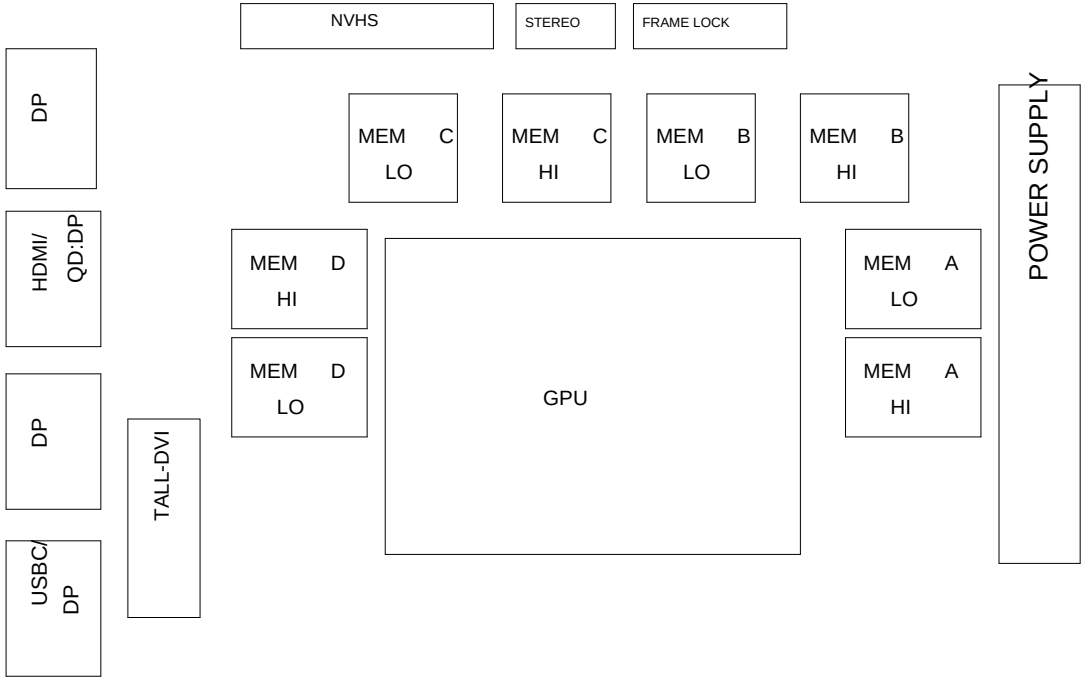
Page2: Block Diagram



Power Supply:

- Power Supply NVVDD-PH6
- Power Supply NVVDD-PH5
- Power Supply NVVDD-PH4
- Power Supply NVVDD-PH3
- Power Supply NVVDD-PH2
- Power Supply NVVDD-PH1
- Power Supply FBVDDQ-PH2
- Power Supply FBVDDQ-PH1
- Power Supply 5V
- PEX_VDD
- 1V8
- USB Open_Vreg option
- Fan
- DP_PWR

EXT_12V 2x3/4 PWR

SW

PEX_12V Finger

SW

SW

3V3_A

PEX_12V Finger

EXT_12V 2x3/4 PWR

3V3 Finger

Block Diagram

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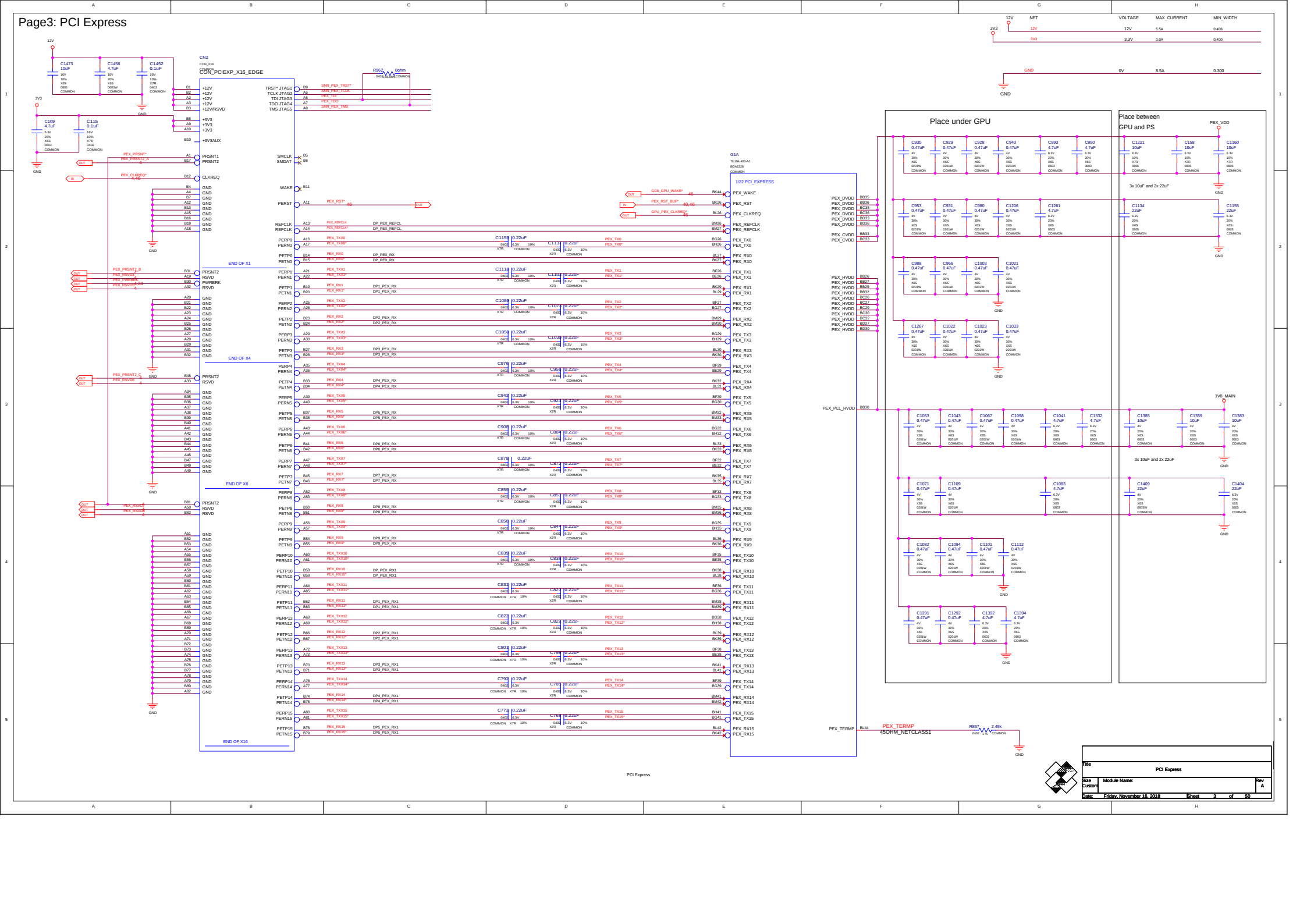
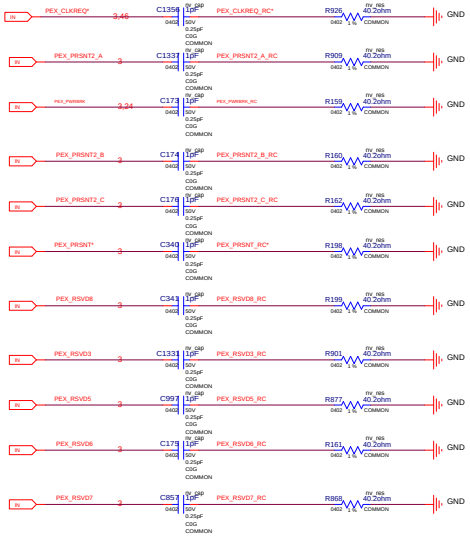
Page3: PCI Express



Page4: PCIE RC TERM



PCIE RC TERM

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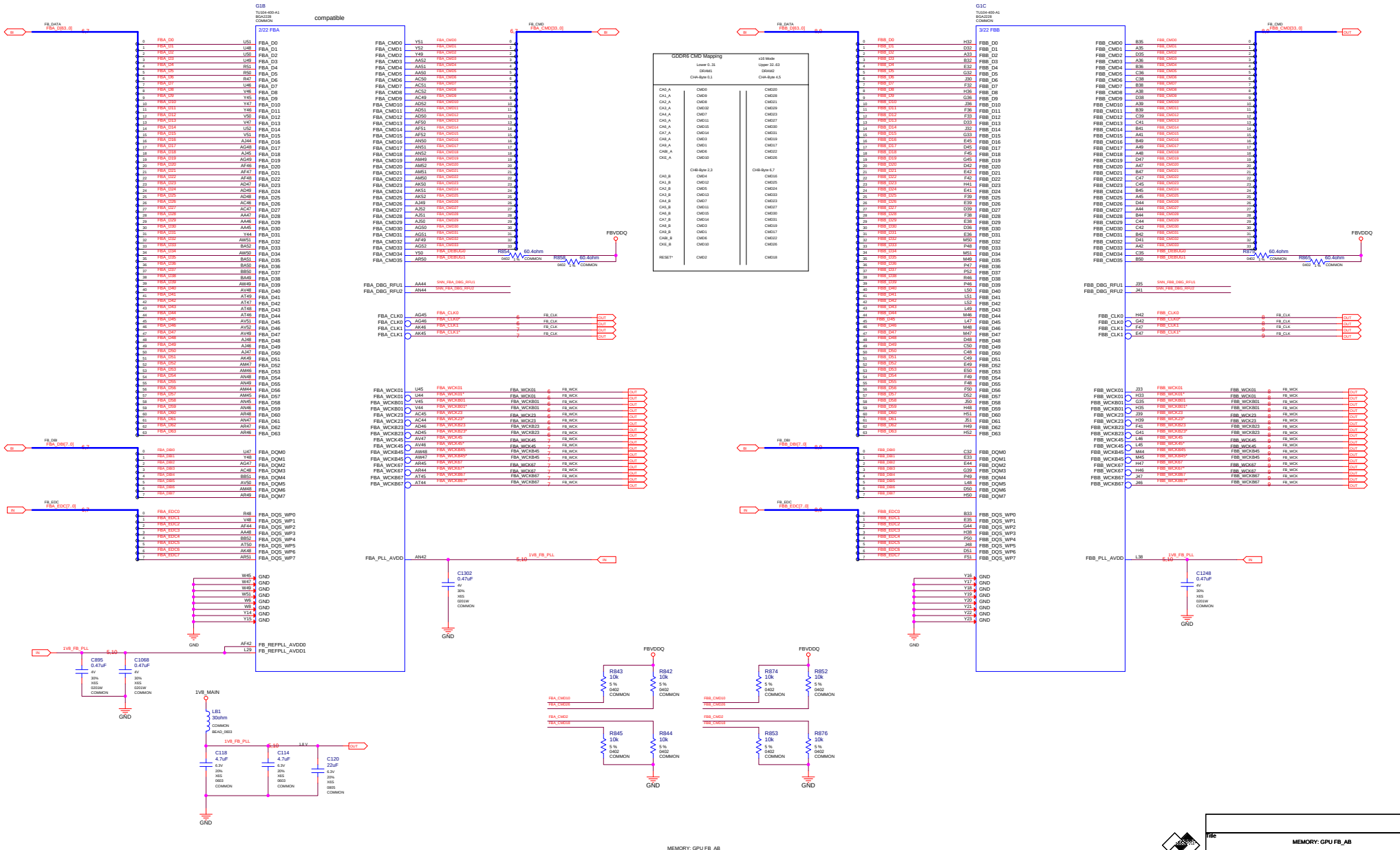
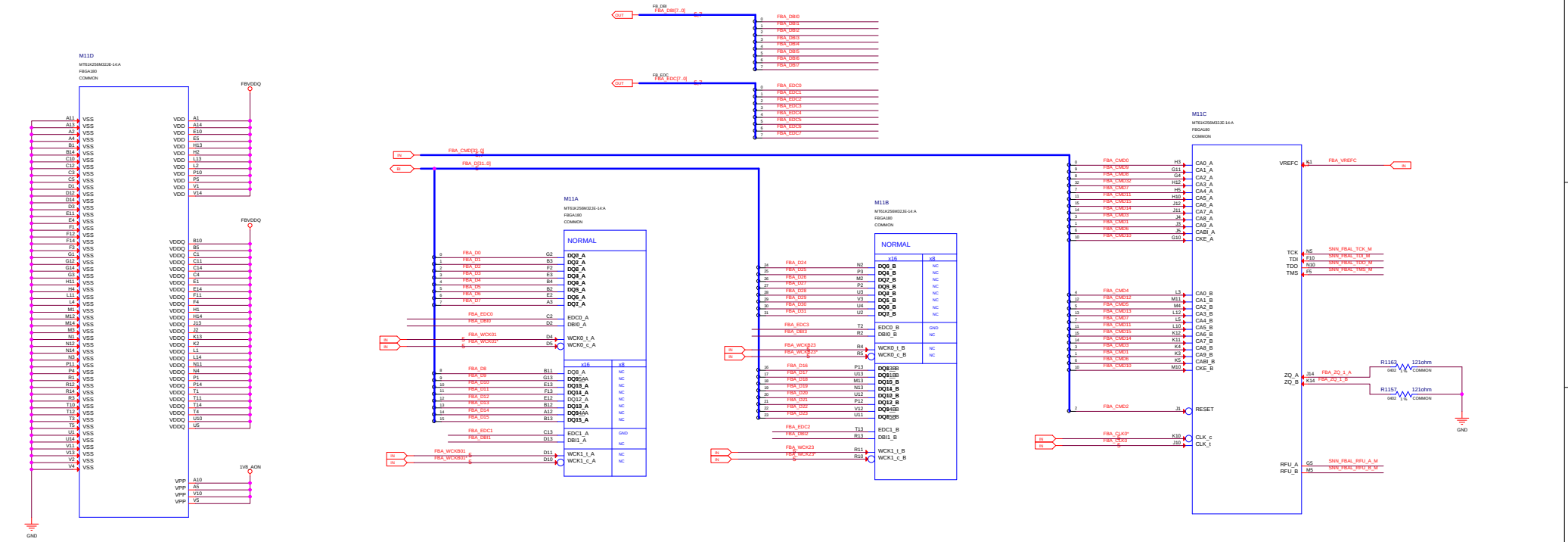
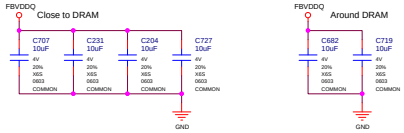
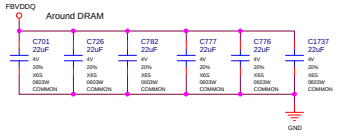
Page5: MEMORY: GPU Partition A/B

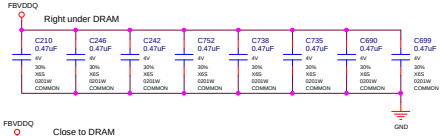


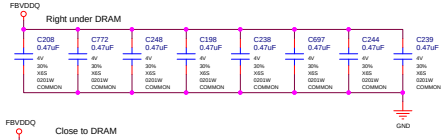
Page6: MEMORY: FBA Partition 31..0

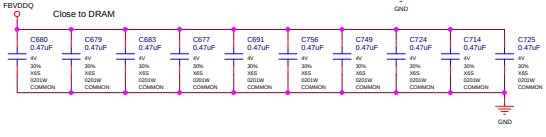


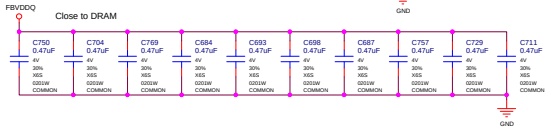




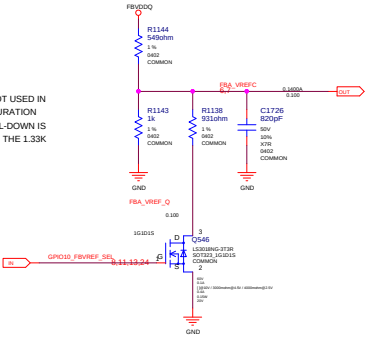








VREFC IS NOT USED IN x16 CONFIGURATION
1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R106



MEMORY: FBA[31:0]

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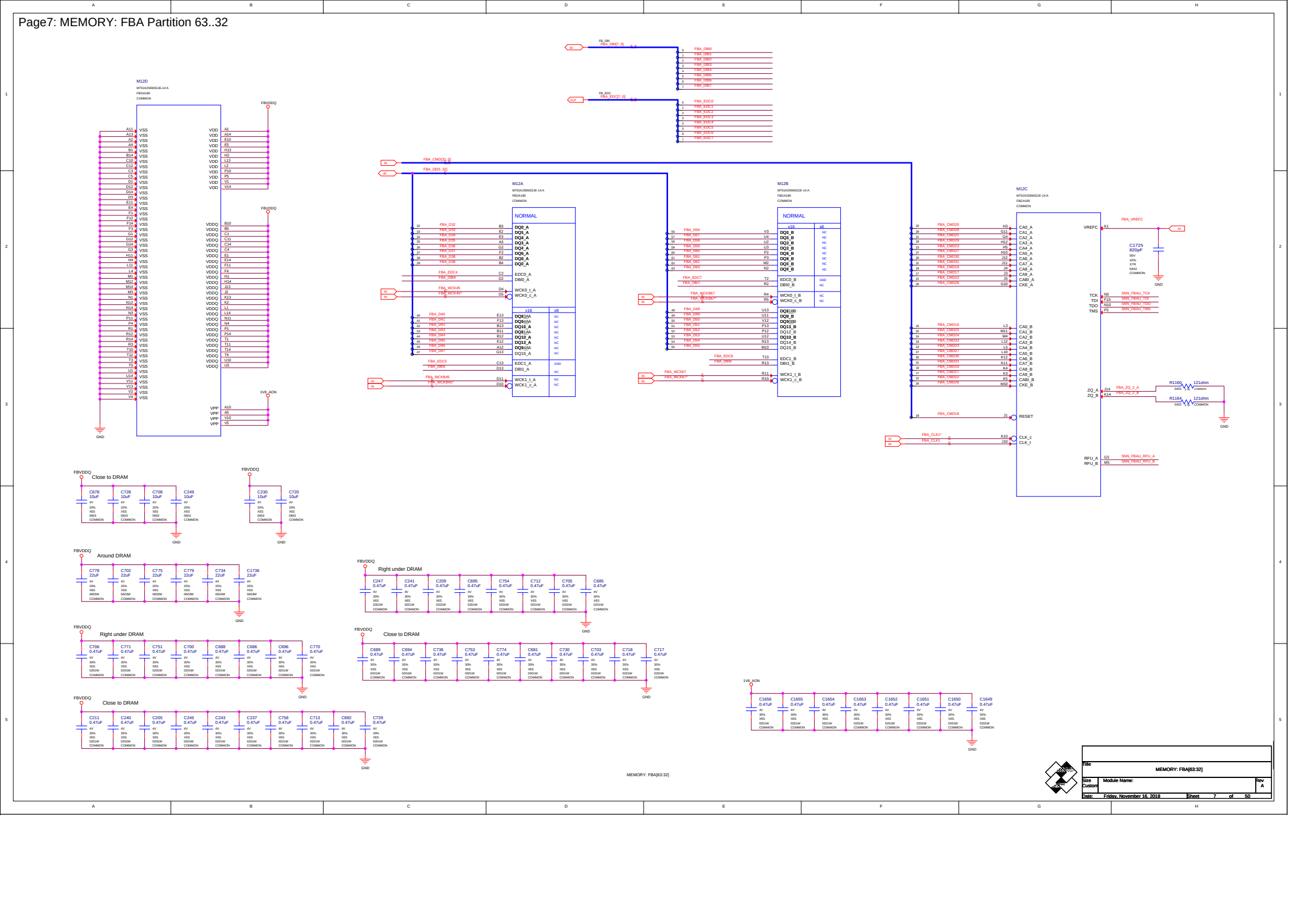
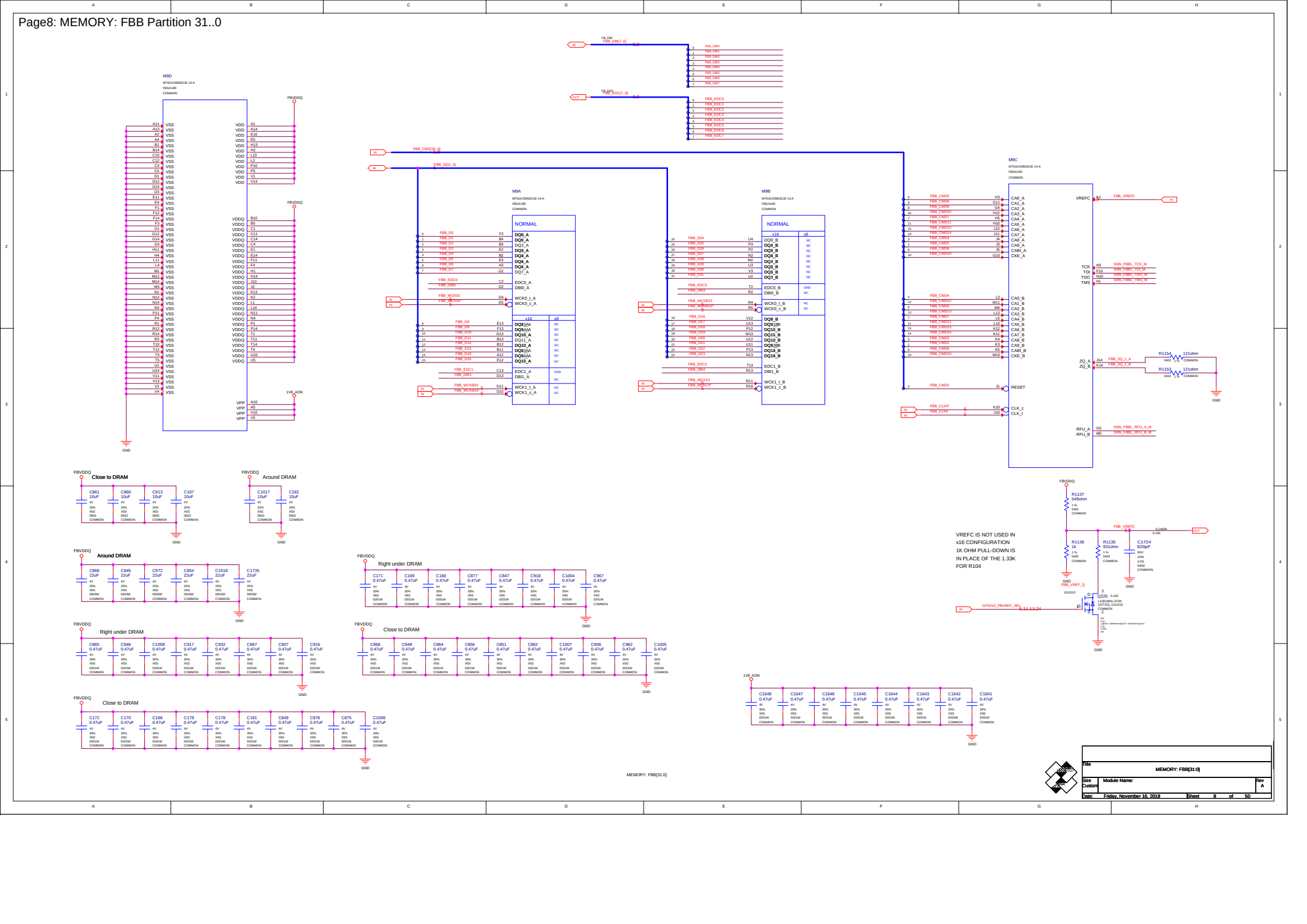
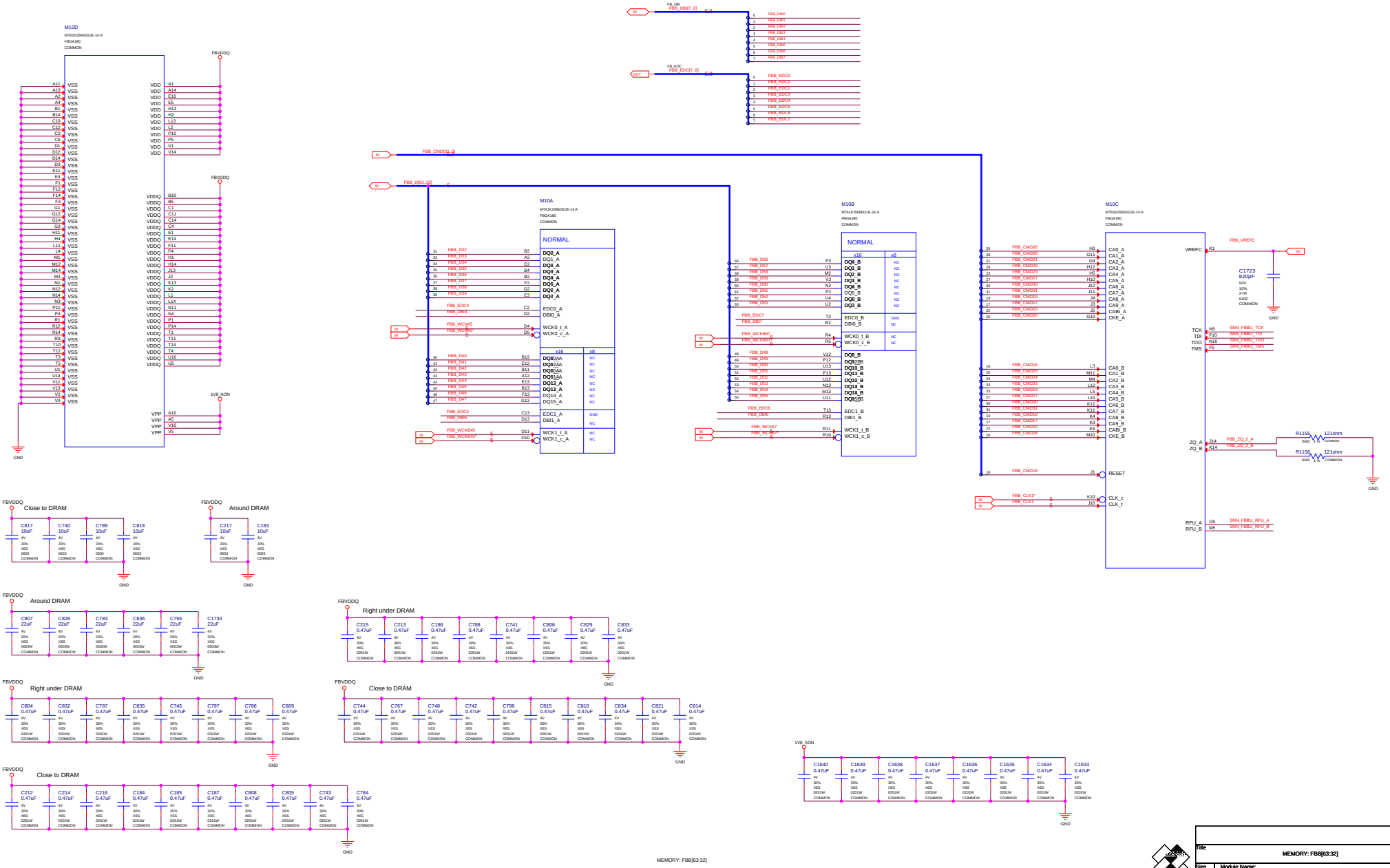
Page7: MEMORY: FBA Partition 63..32



Page8: MEMORY: FBB Partition 31..0



Page9: MEMORY: FBB Partition 63..32



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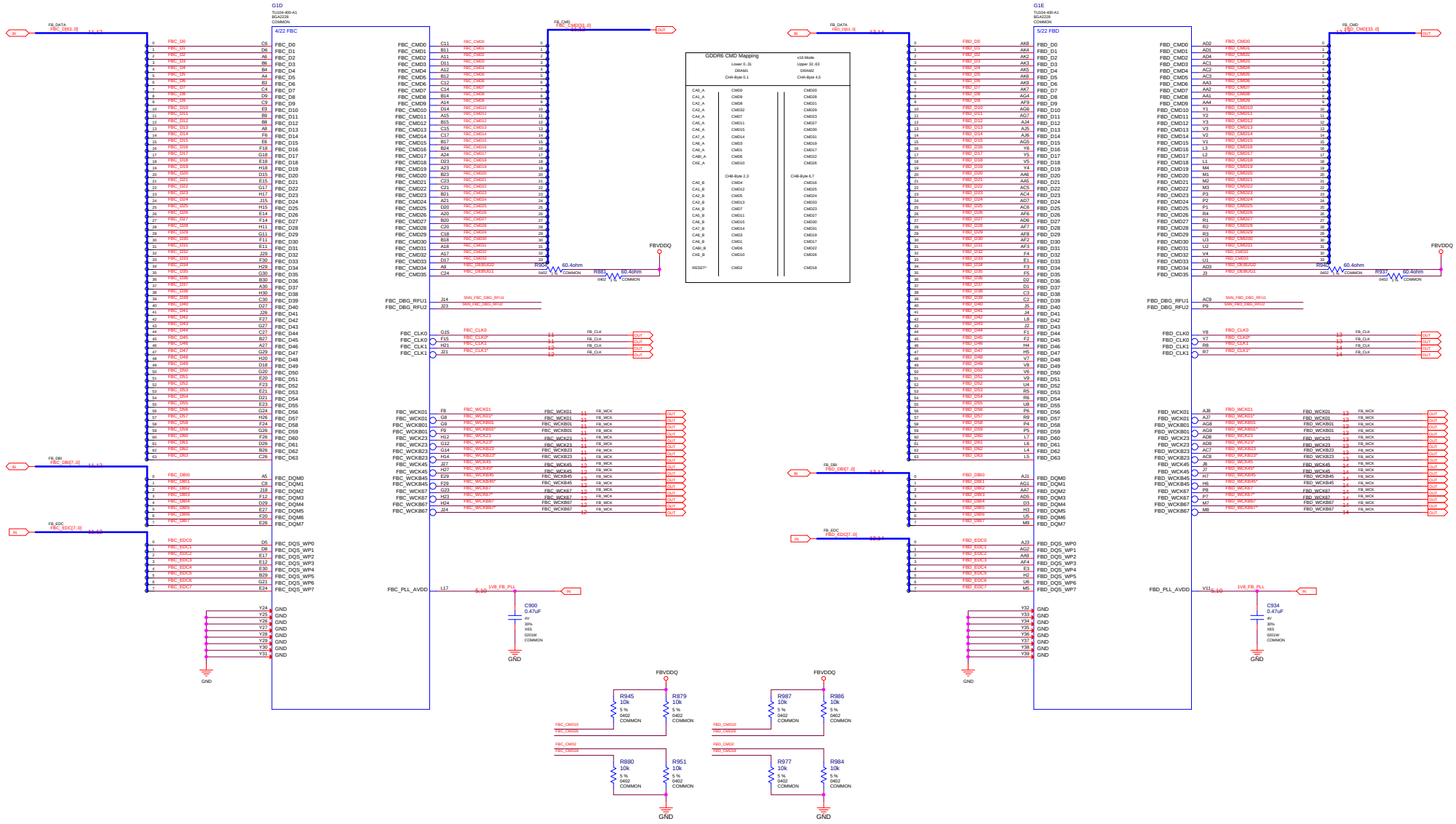
Page10: MEMORY: GPU Partition C/D



Title	MEMORY: GPU FB_CD		
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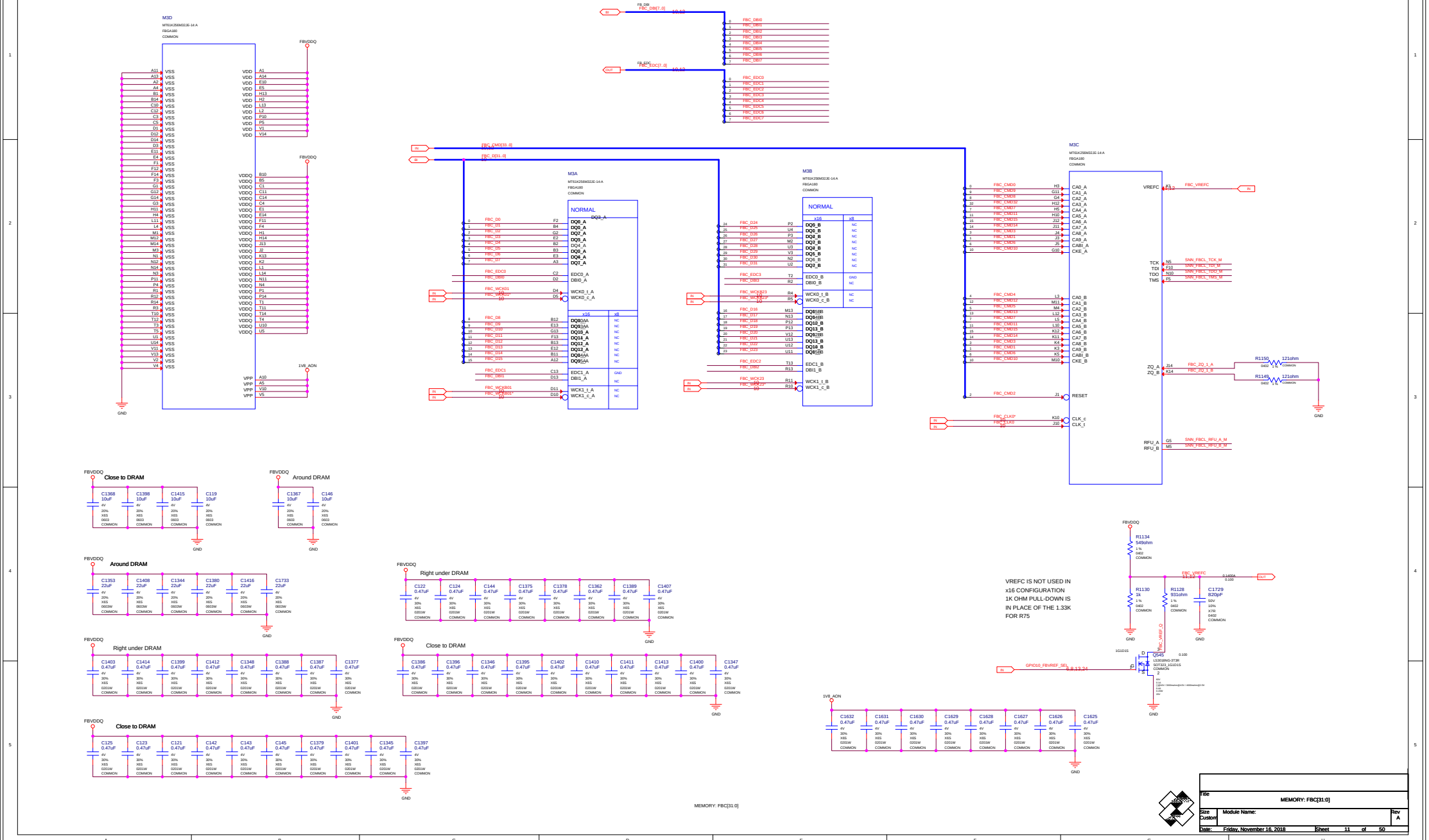
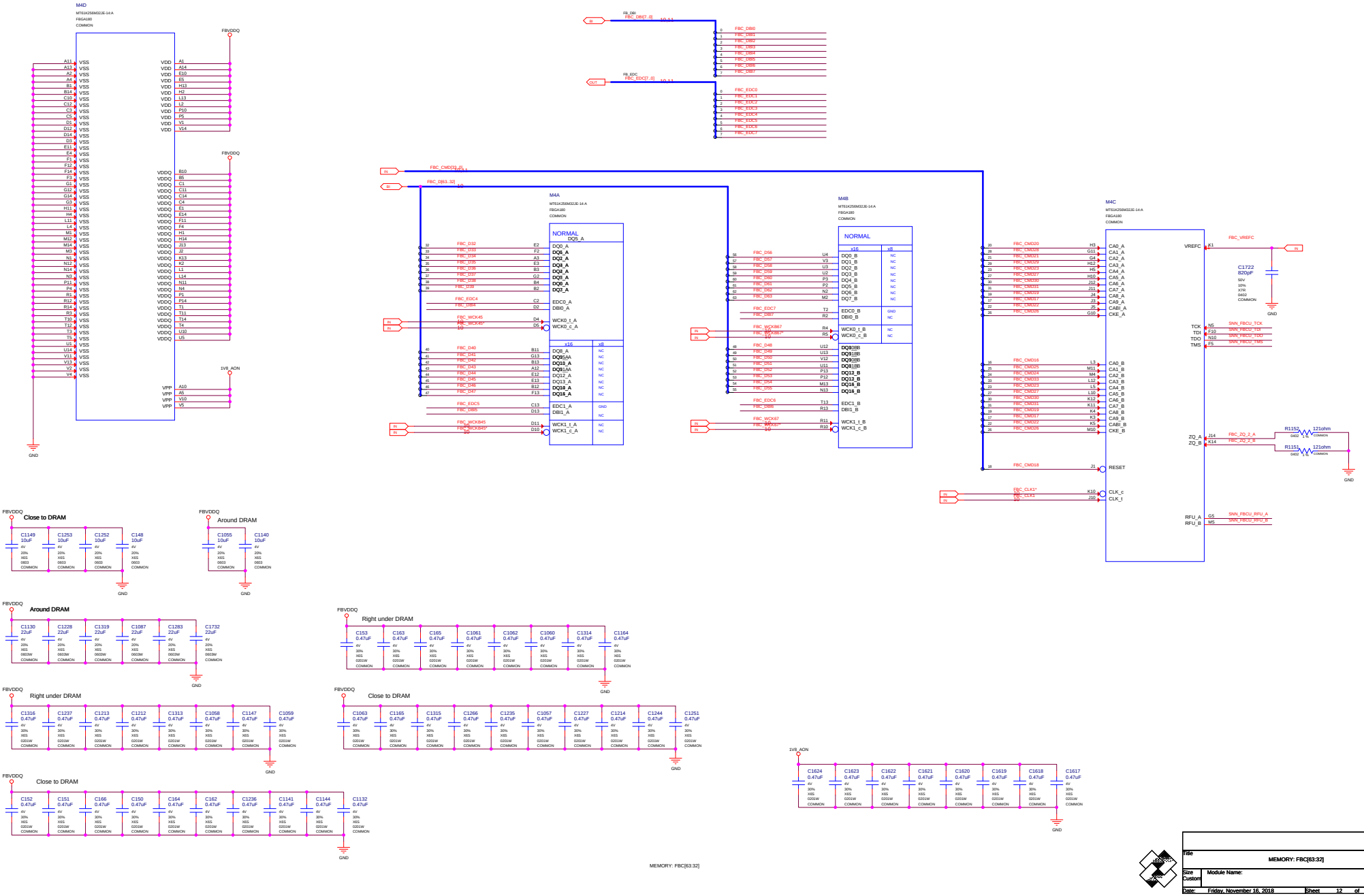


Page12: MEMORY: FBC Partition 63..32



Title	MEMORY: FBC[63:32]
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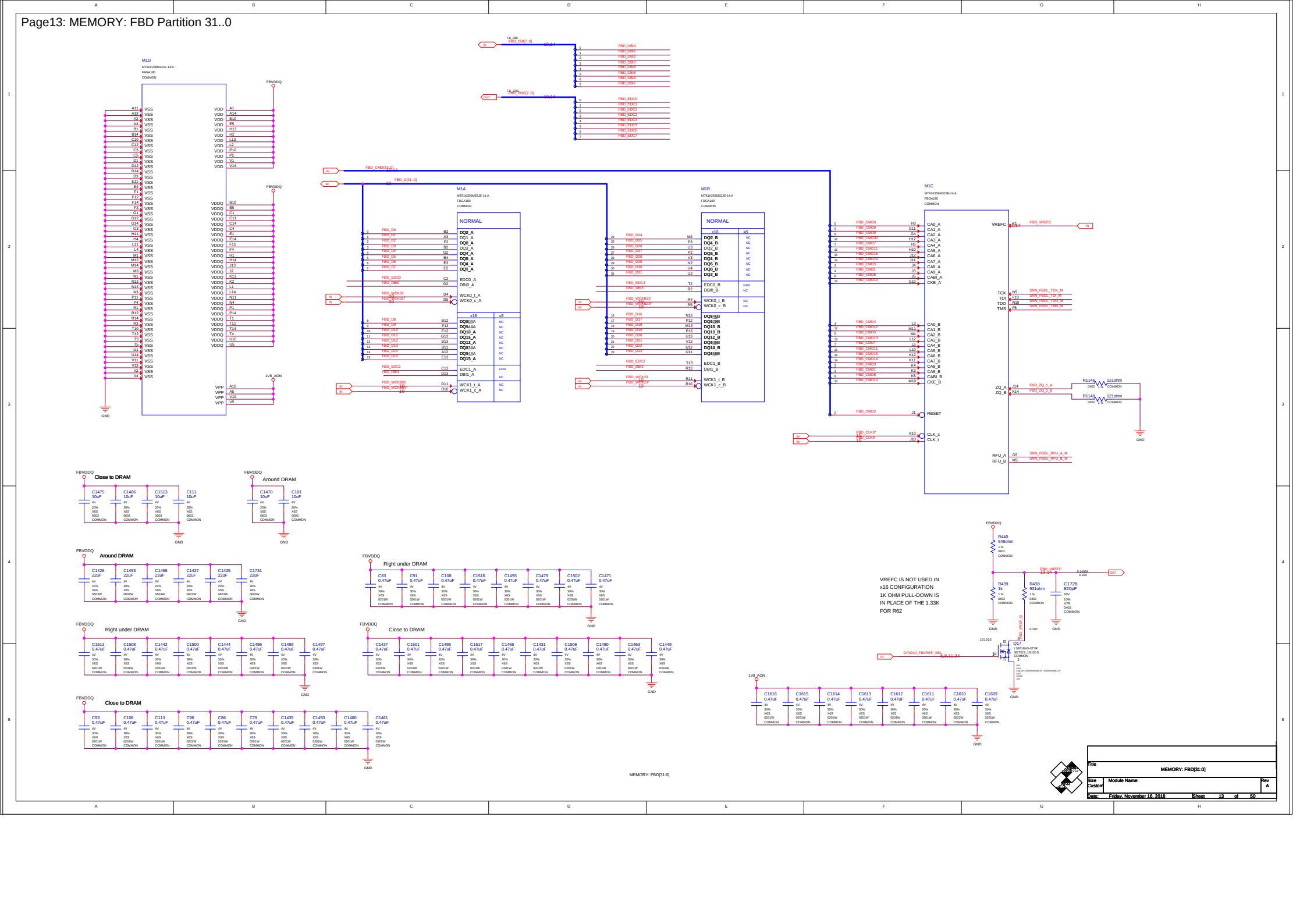
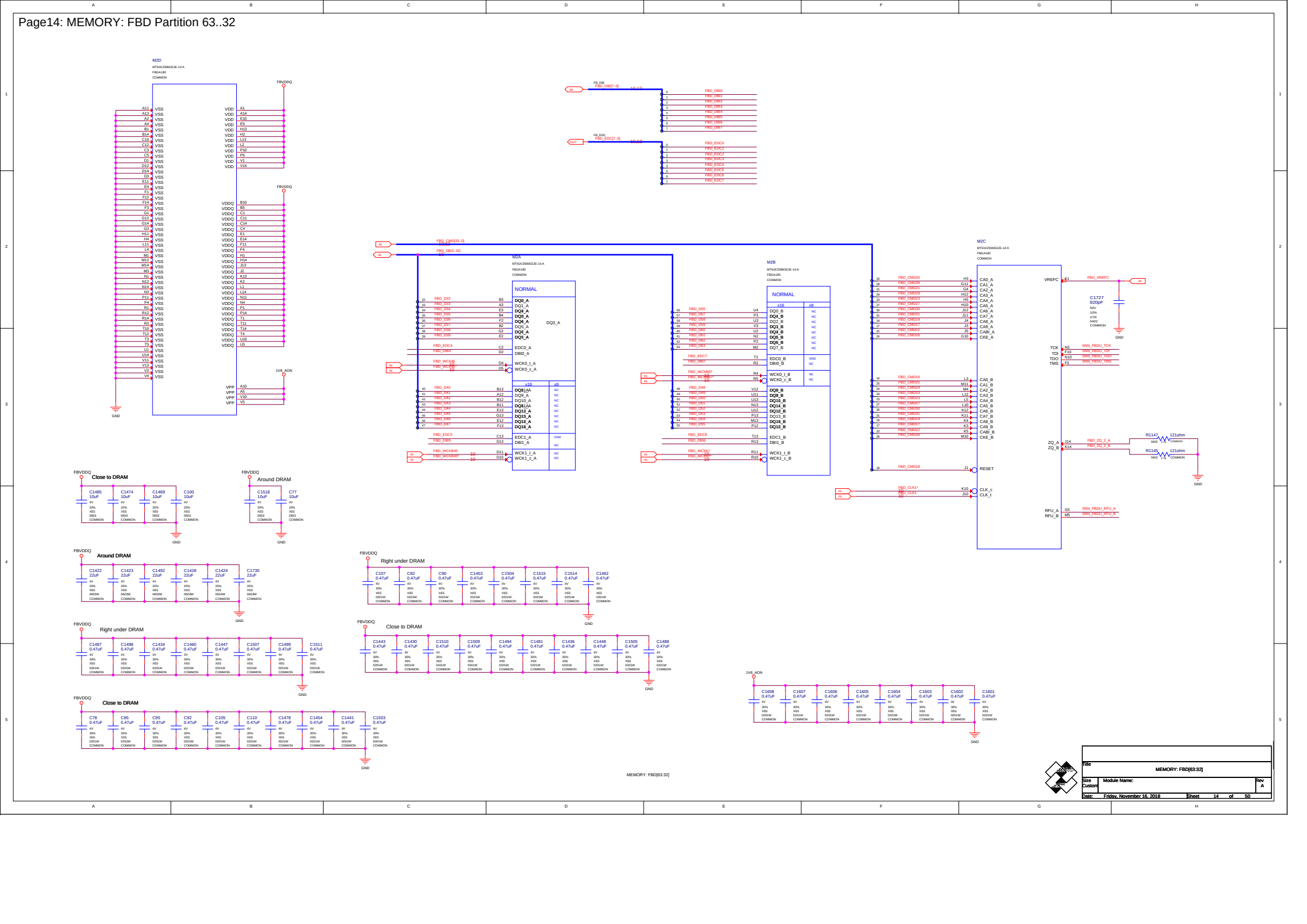
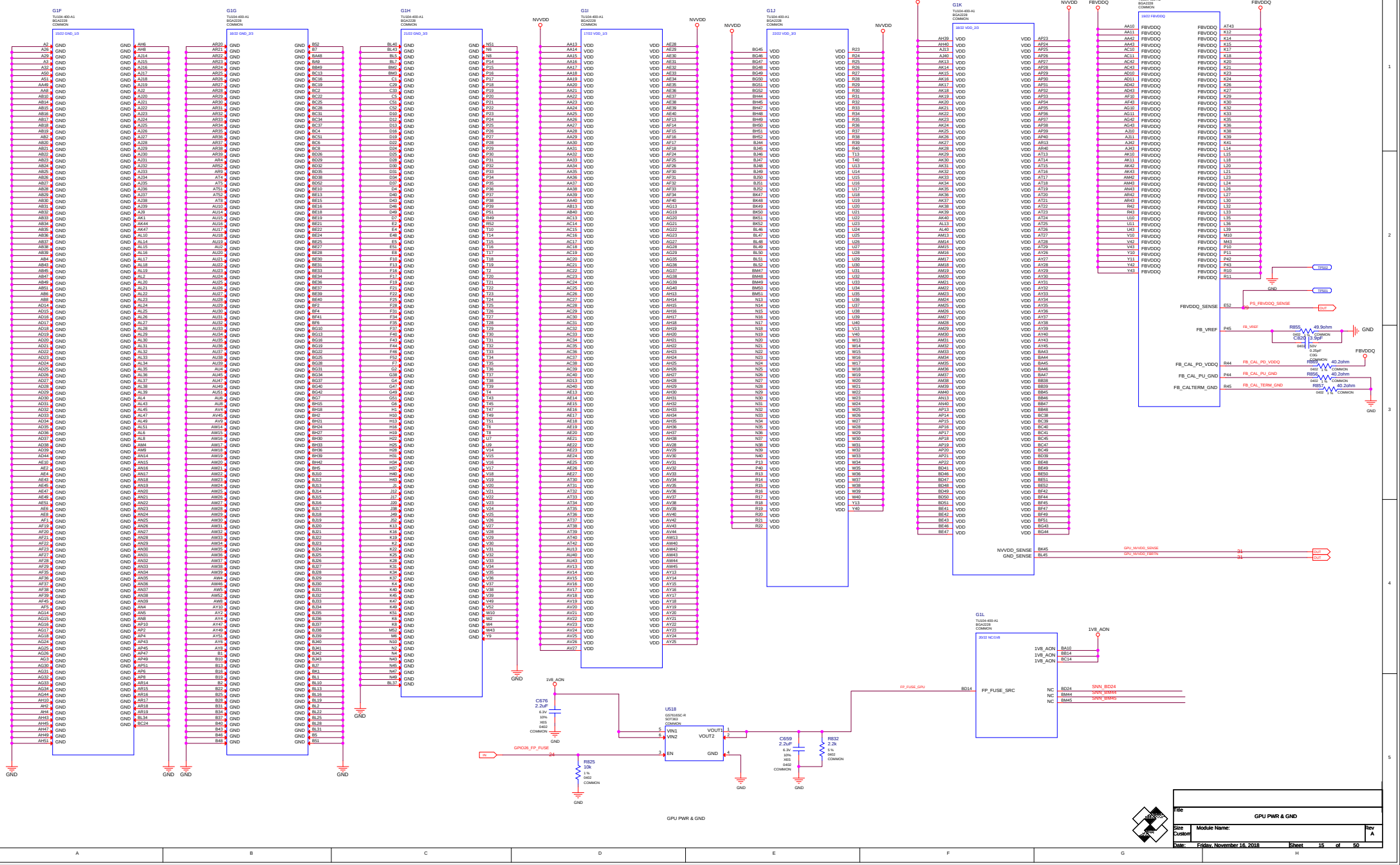
Page13: MEMORY: FBD Partition 31..0



Page14: MEMORY: FBD Partition 63..32



Page15: GPU PWR and GND



Title	GPU PWR & GND
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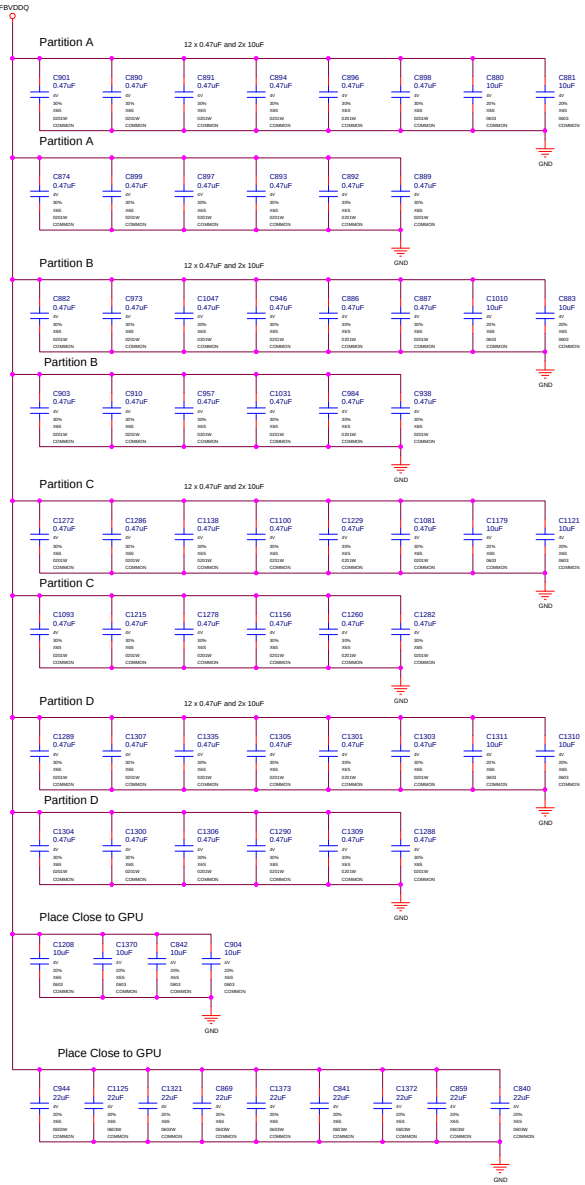
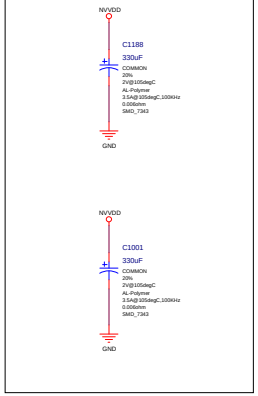
Page16: GPU Decoupling 1

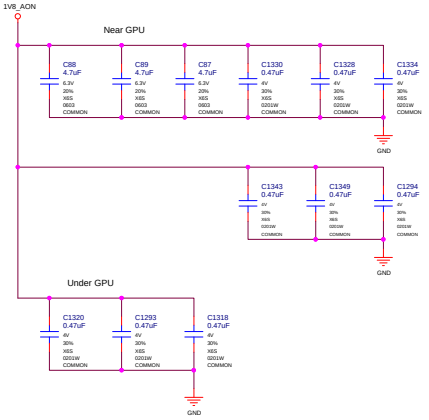
FBVDDQ



Under GPU



1V8_AON



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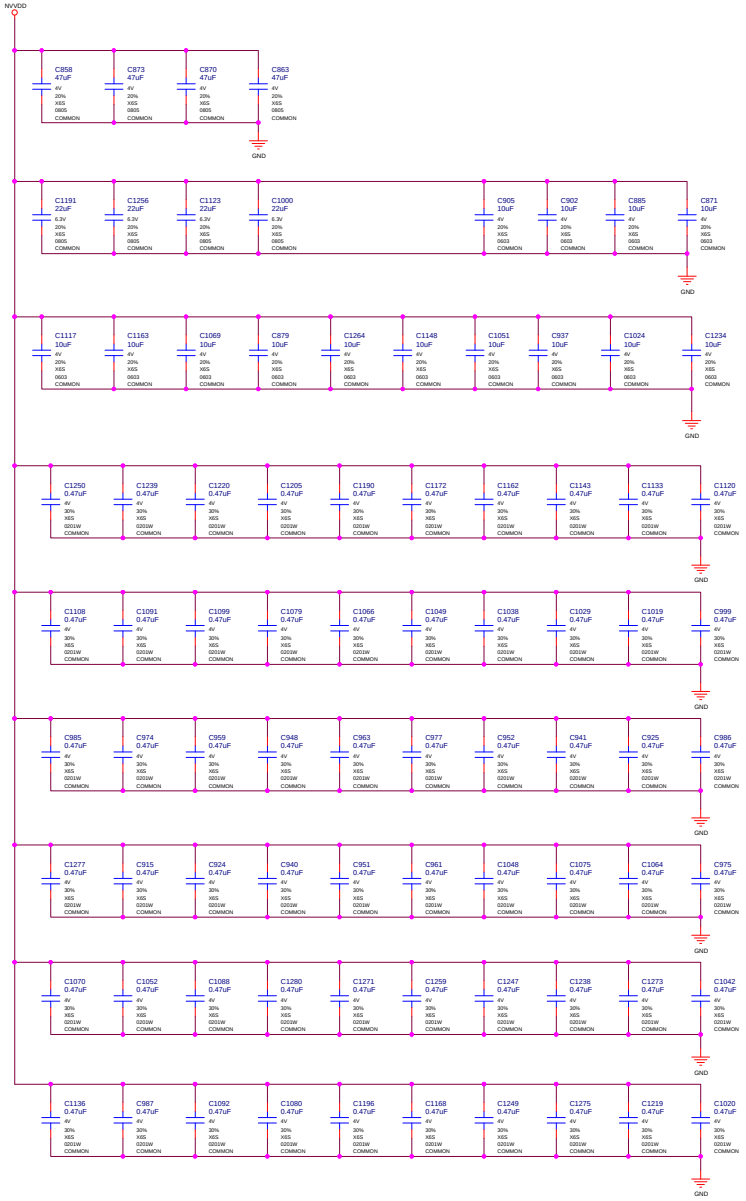
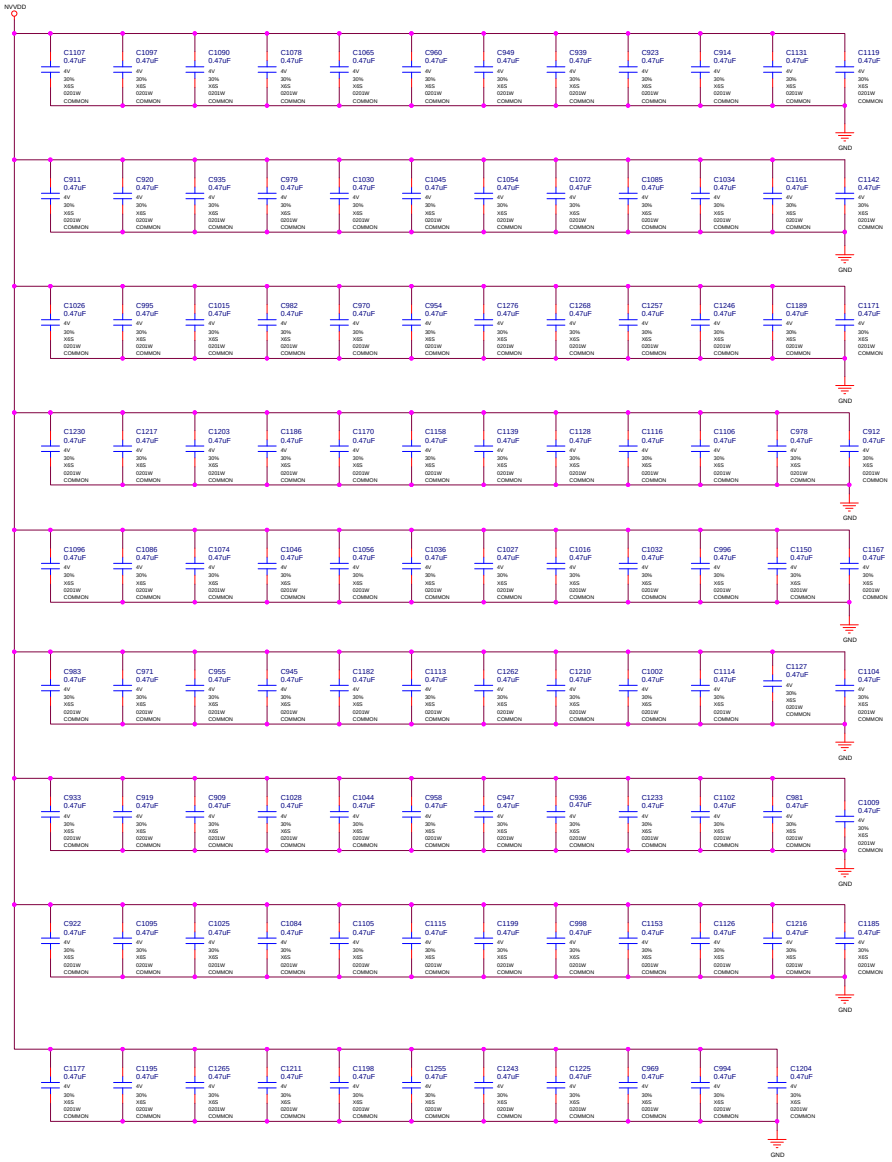
Page17: GPU Decoupling 2

NVVDD





GPU Decoupling2

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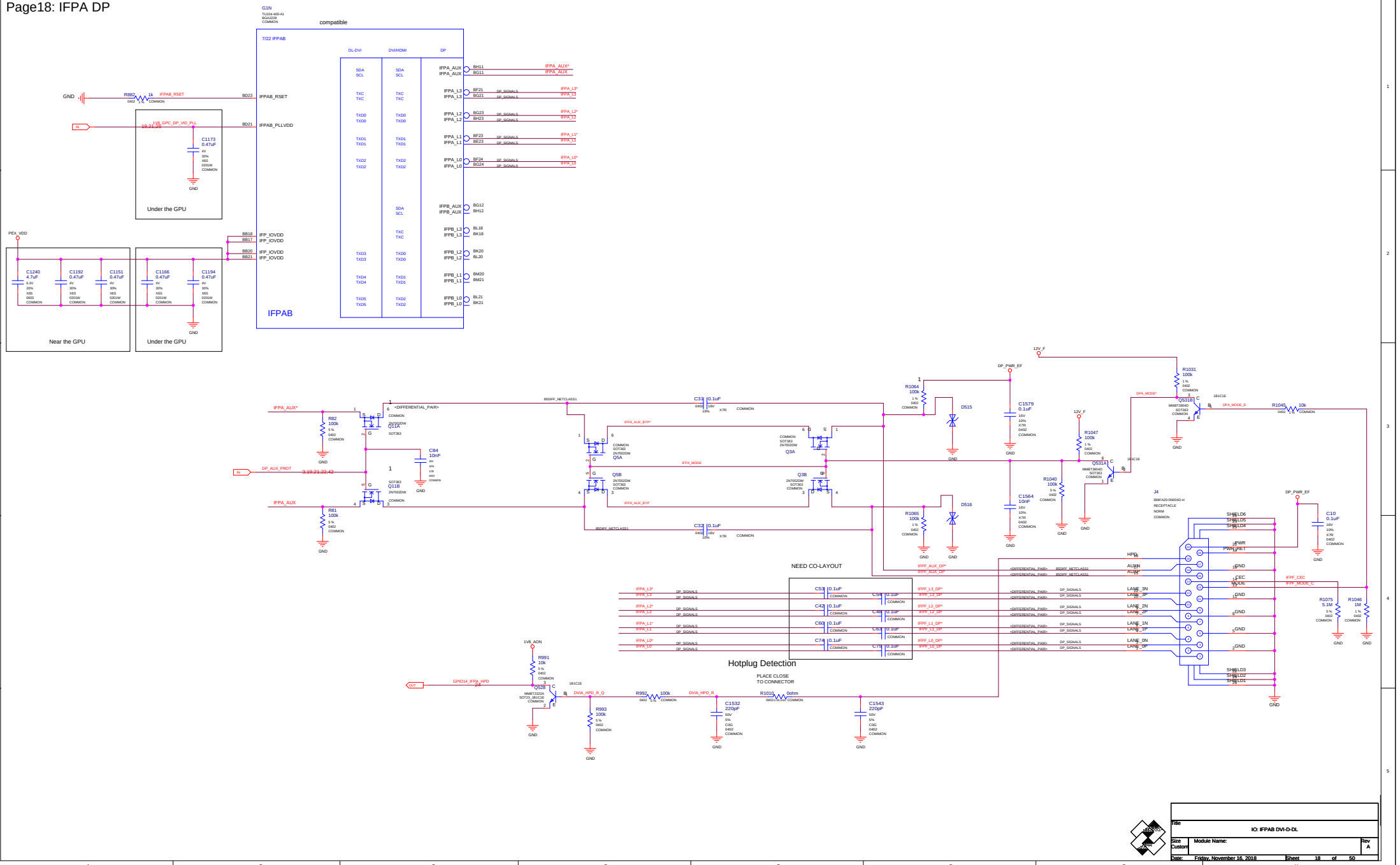
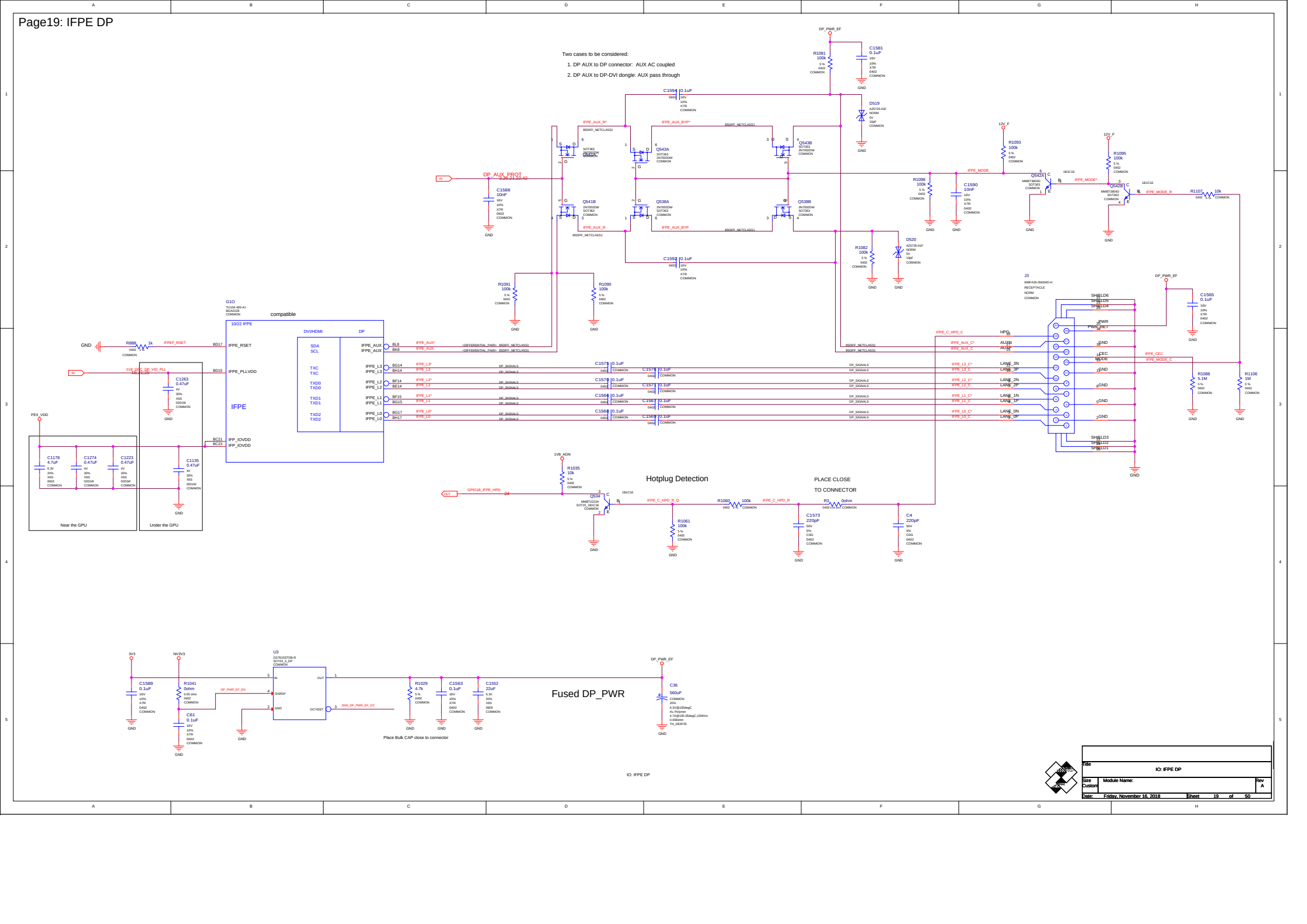
Page18: IFPA DP



Page19: IFPE DP



Title	IO: IFPE DP
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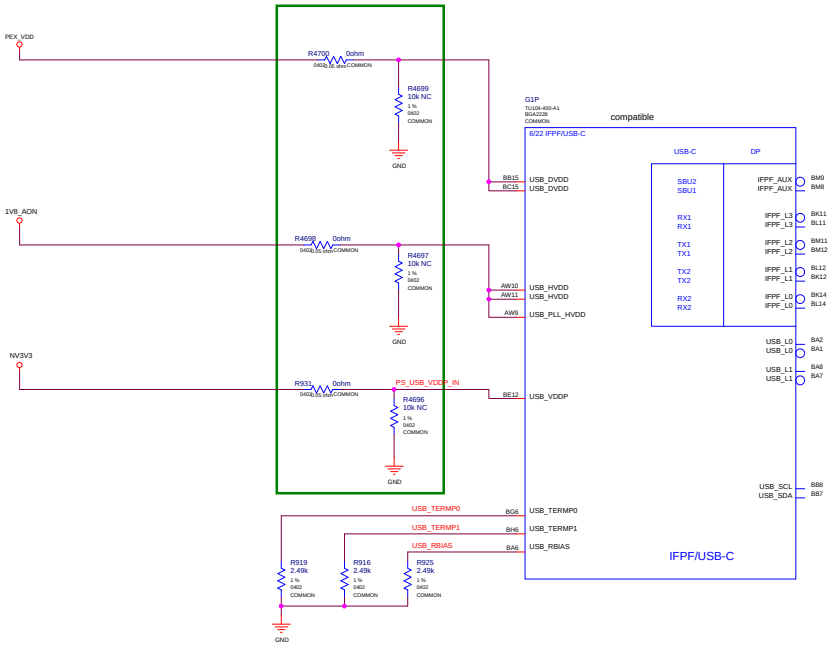
Page20: IFPF USB-C



Title	IO: IFPF USBC
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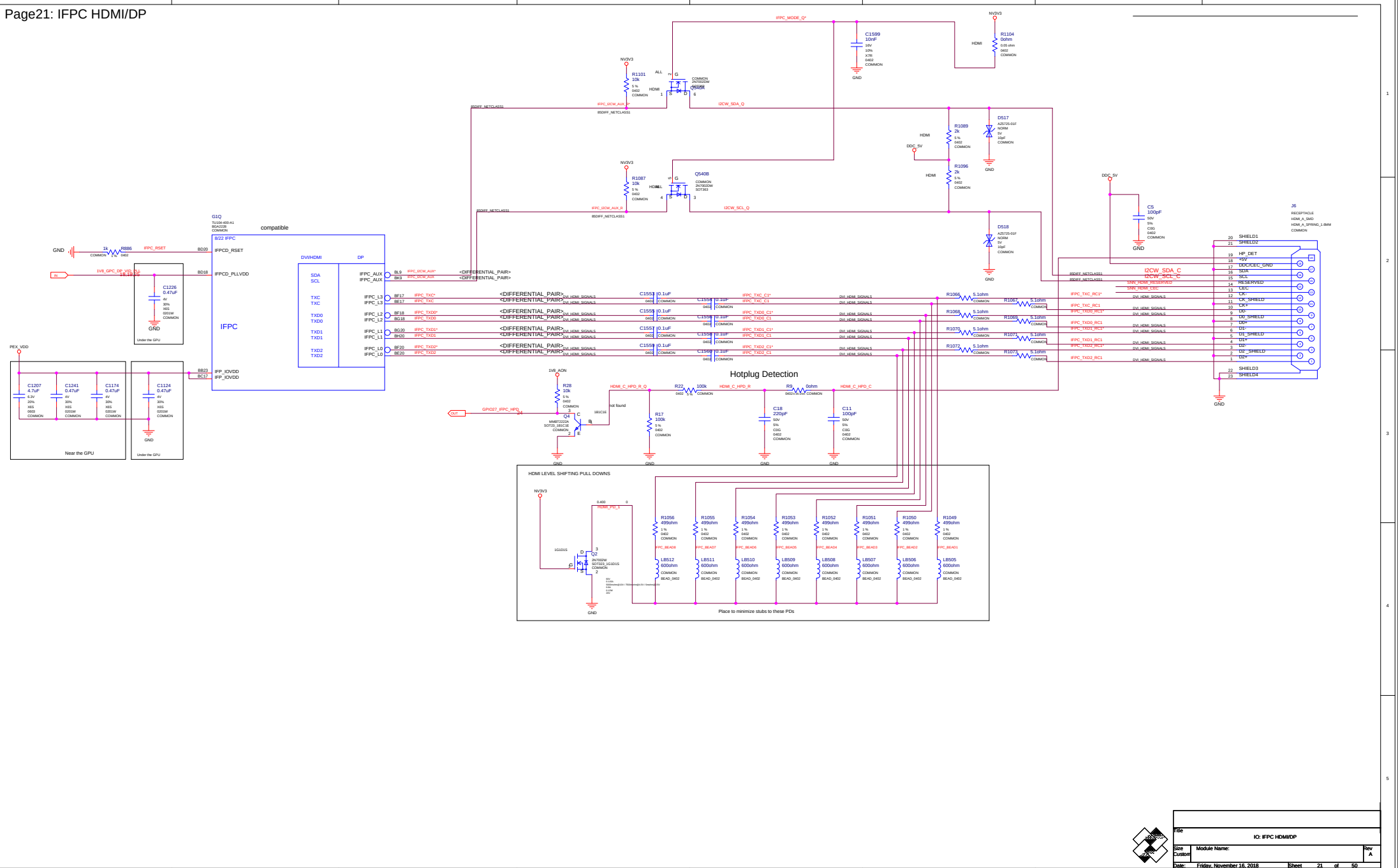
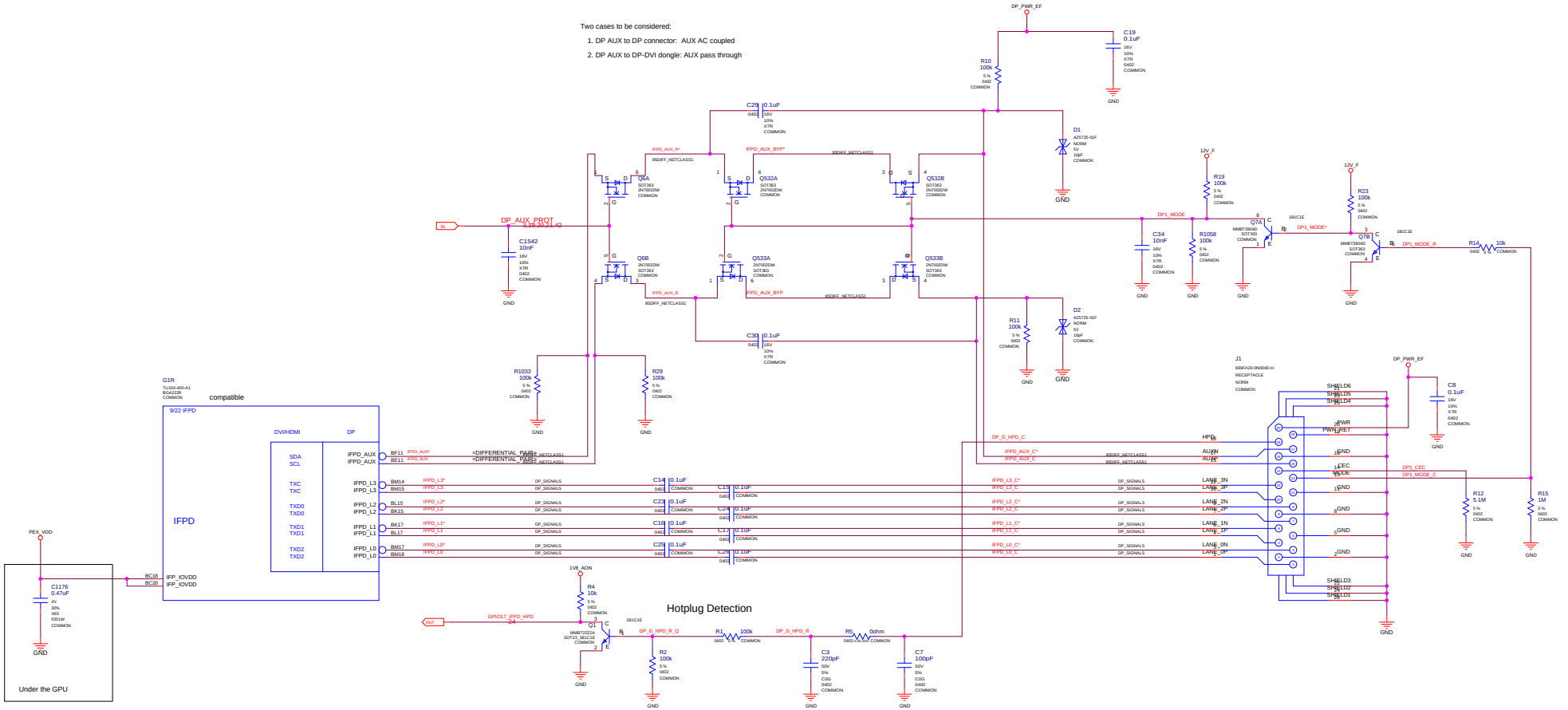
21-JUN-2018

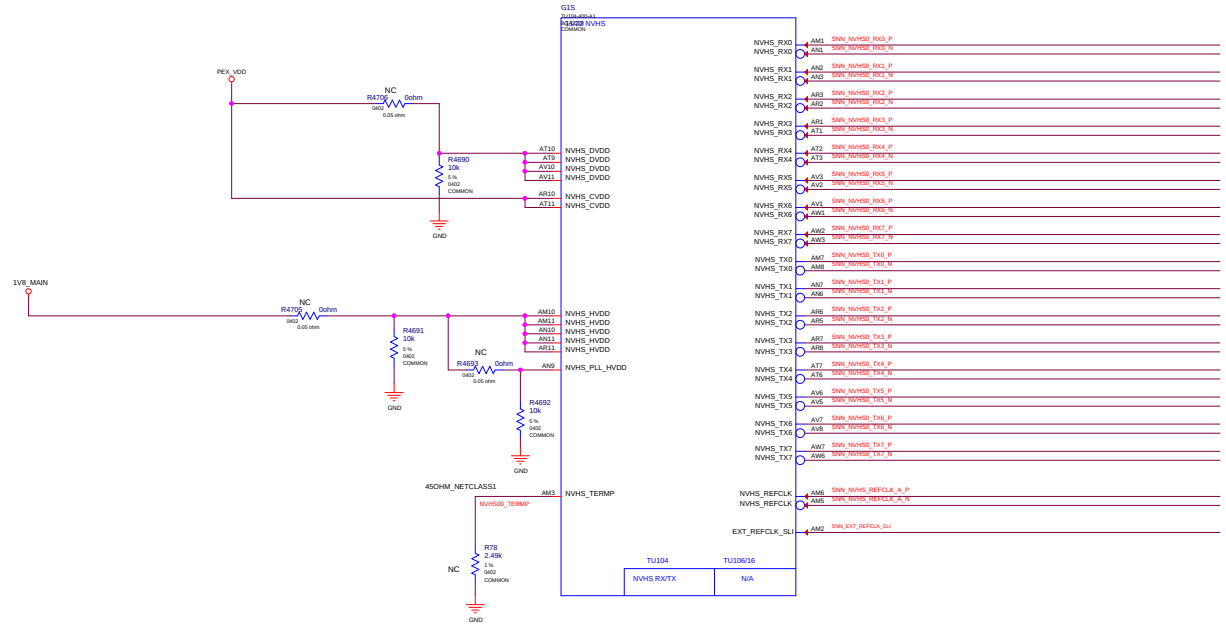
Page21: IFPC HDMI/DP



Page22: IFPD DP



Page23: NVHS Interface and Frame Lock



IO: NVHS Interface and Frame Lock

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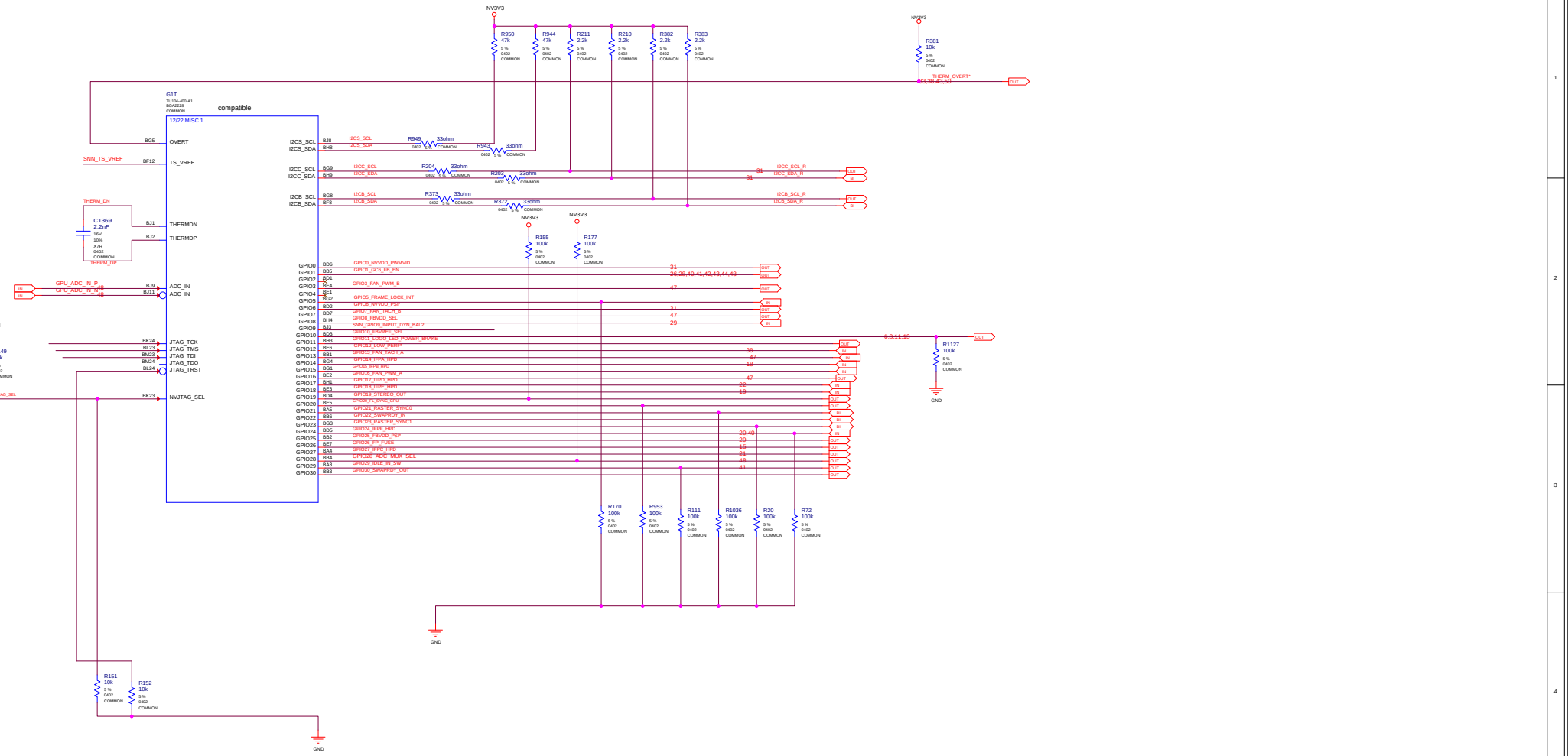
Page24: MISC1: Fan, Thermal, JTAG, GPIO



Title	MISC1: Thermal, JTAG, GPIO,STEREO		
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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

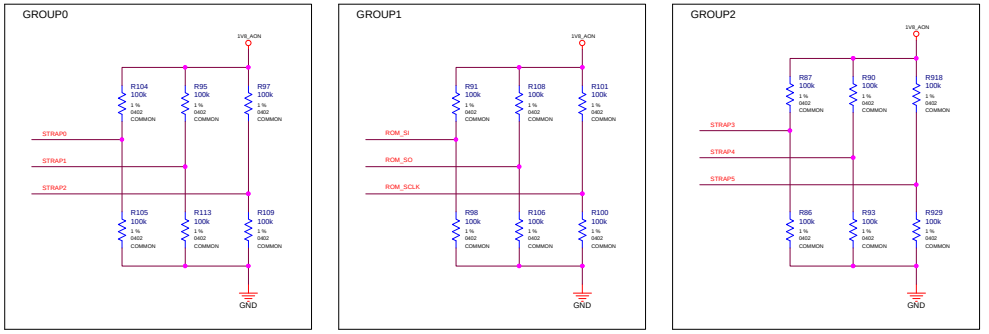
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

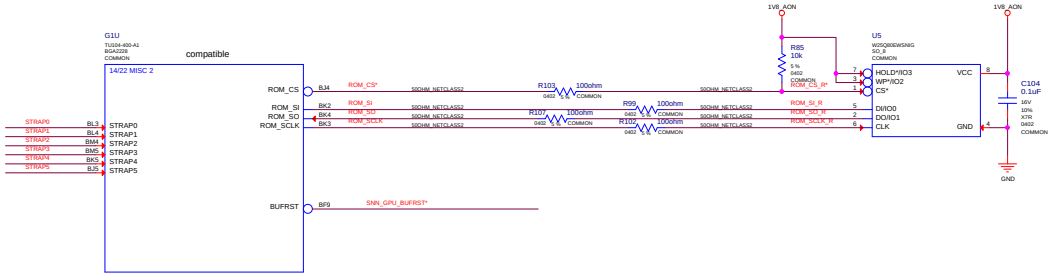
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

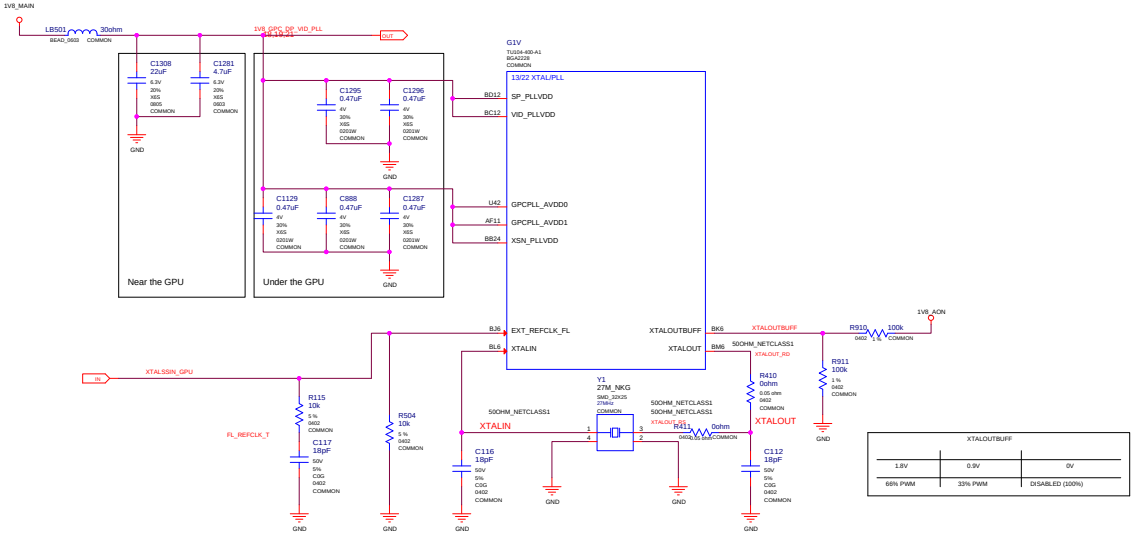
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







MISC2: ROM, XTAL,STRAPS

Title	MISC2: ROM, XTAL,STRAPS		
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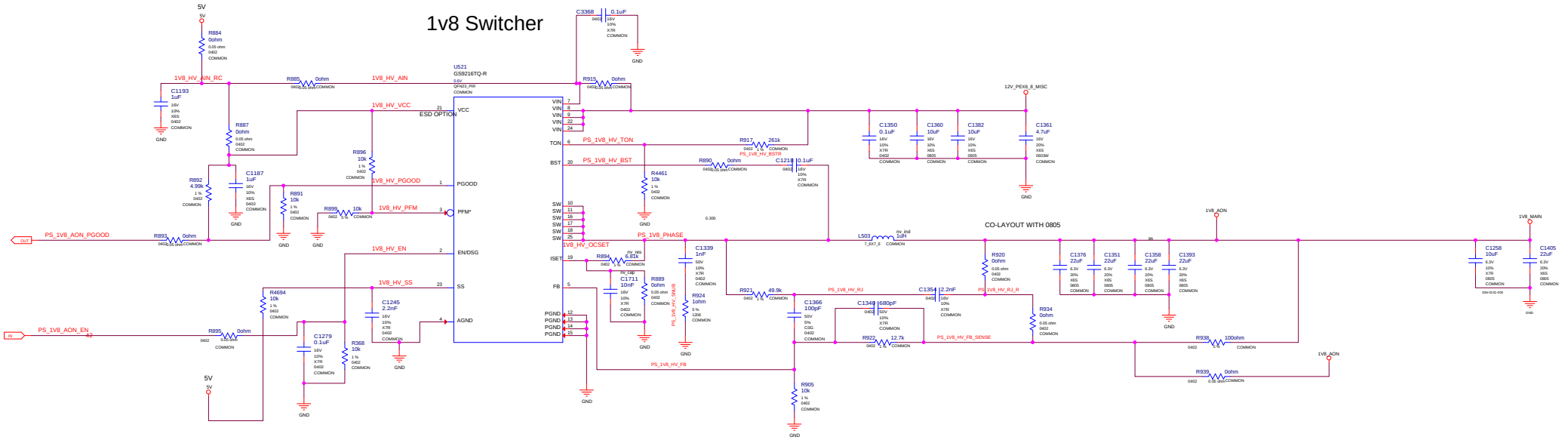
Page26: PS: 1V8 PLL, 1V8_AON



PS: 1V8_PLL, 1V8_AON

Title	PS: 1V8_PLL, 1V8_AON		
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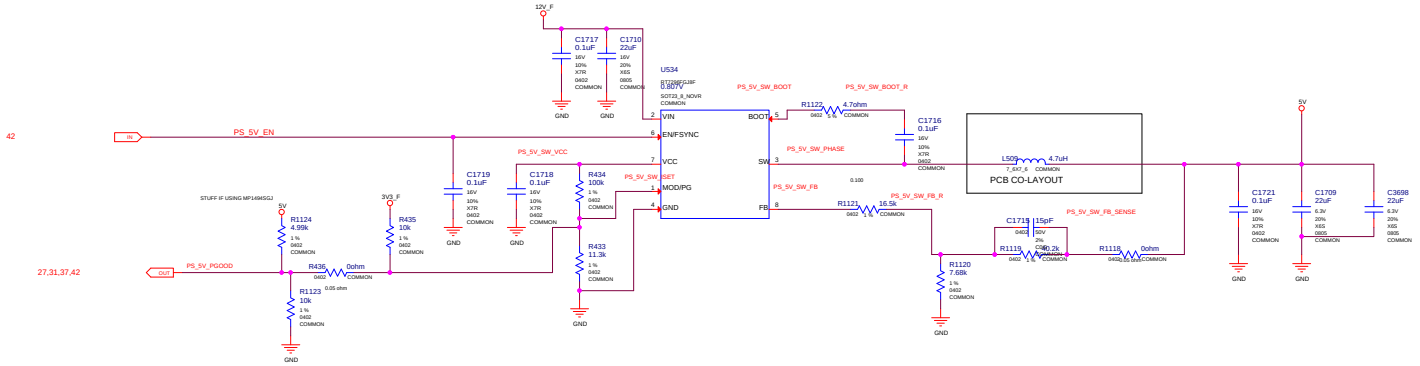
Page27: PS: 5V



PS: 5V

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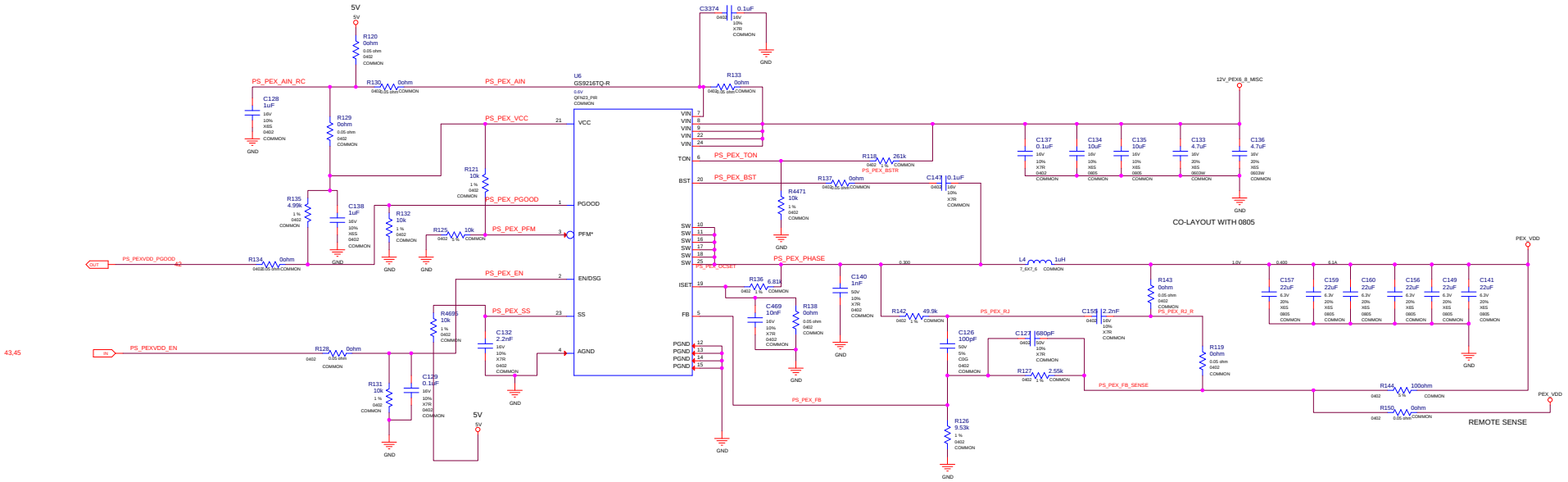
PEX Switcher



PS: PEXVDD

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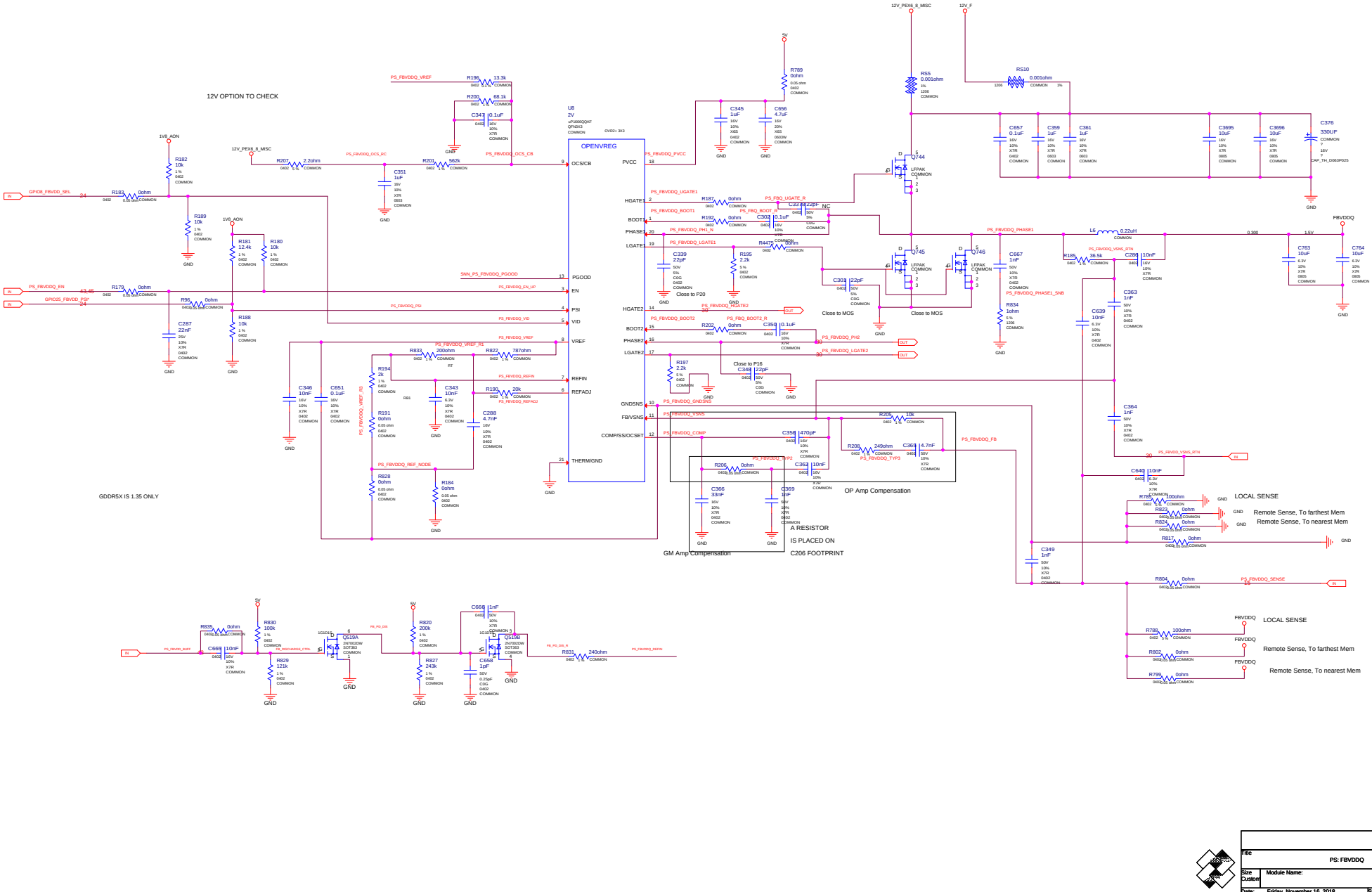
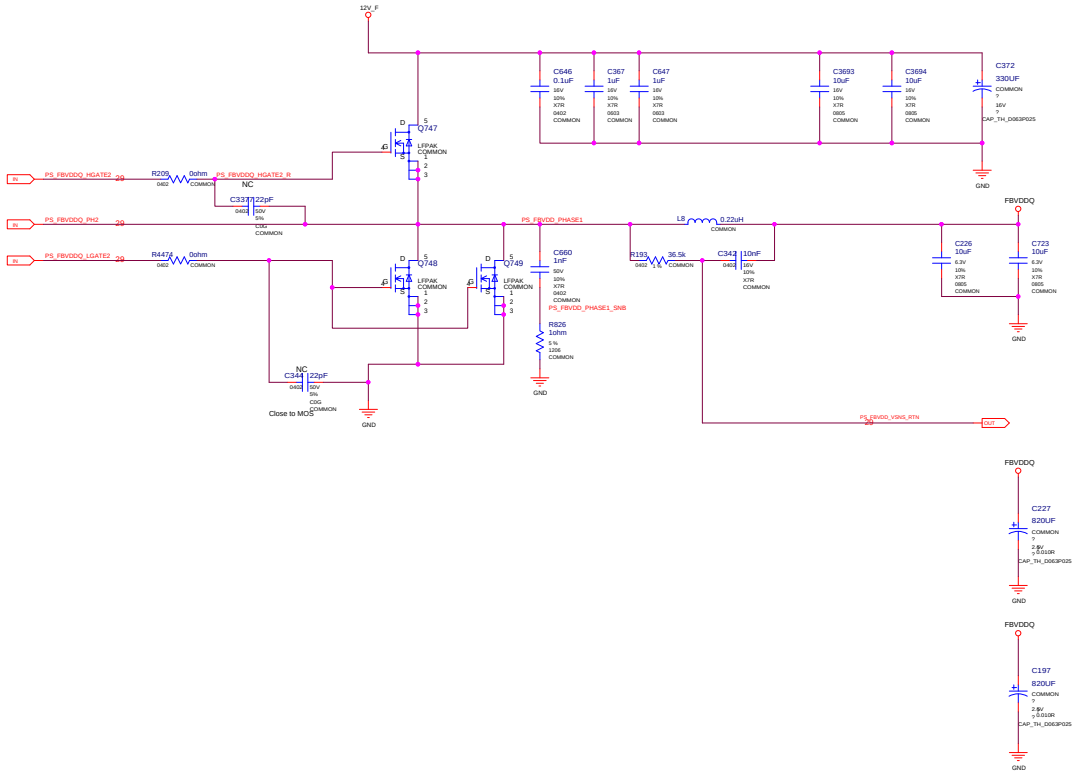
Page29: PS: FBVDDQ





Title	PS: FBVDDQ PH2
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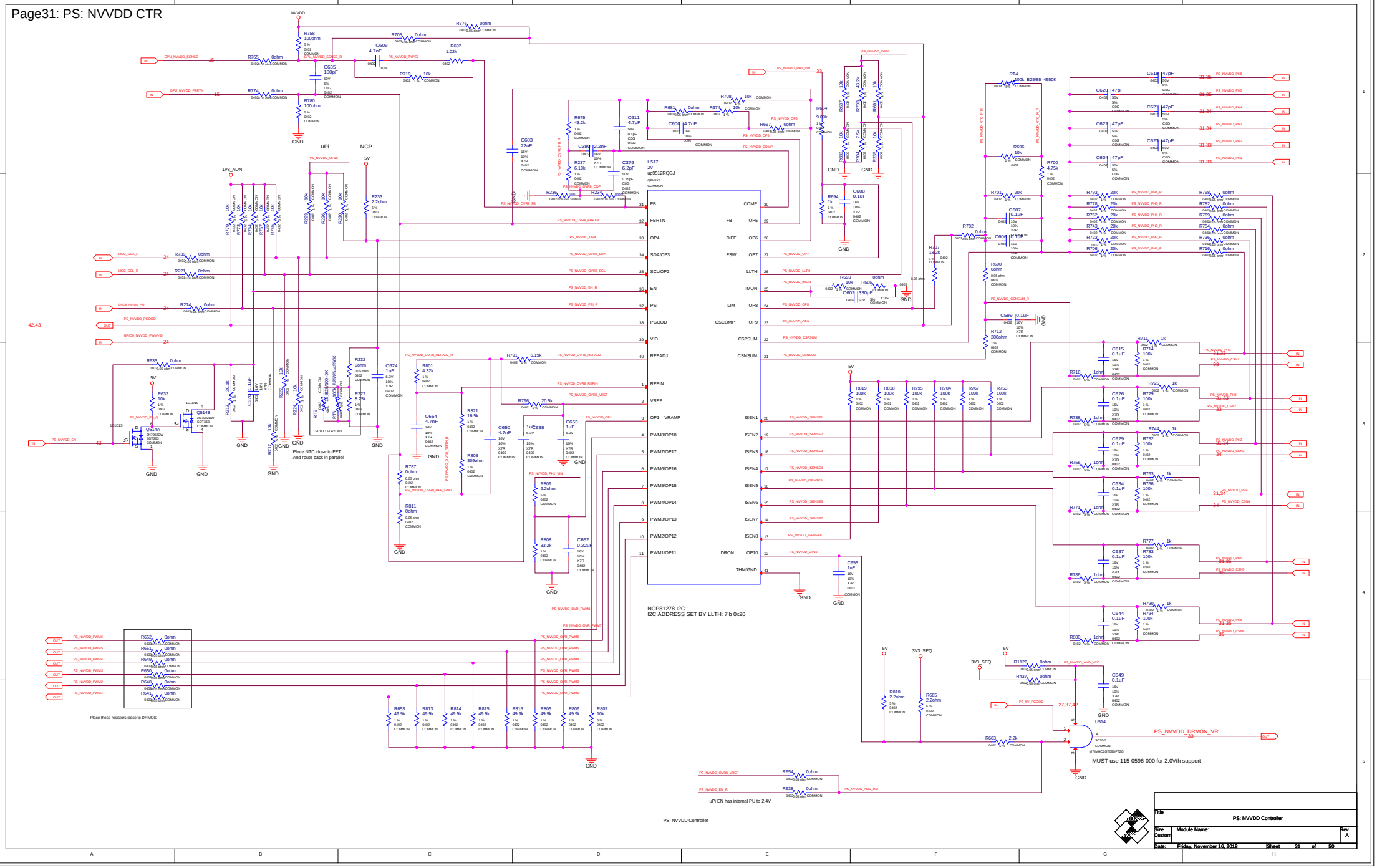
Page31: PS: NVVDD CTR
NCP81278 I2C
I2C ADDRESS SET BY LLTH: 7'b 0x20
Place NTC close to FET
And route back in parallel
Place these resistors close to DRMOS
uPI EN has internal PU to 2.4V
MUST use 115-0596-000 for 2.0Vth support
PS: NVVDD Controller
Title
PS: NVVDD Controller
Module Name:
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Page32: PS: NVVDD CTR OVR3i

Title	PS: NVVDD Controller OVR3i
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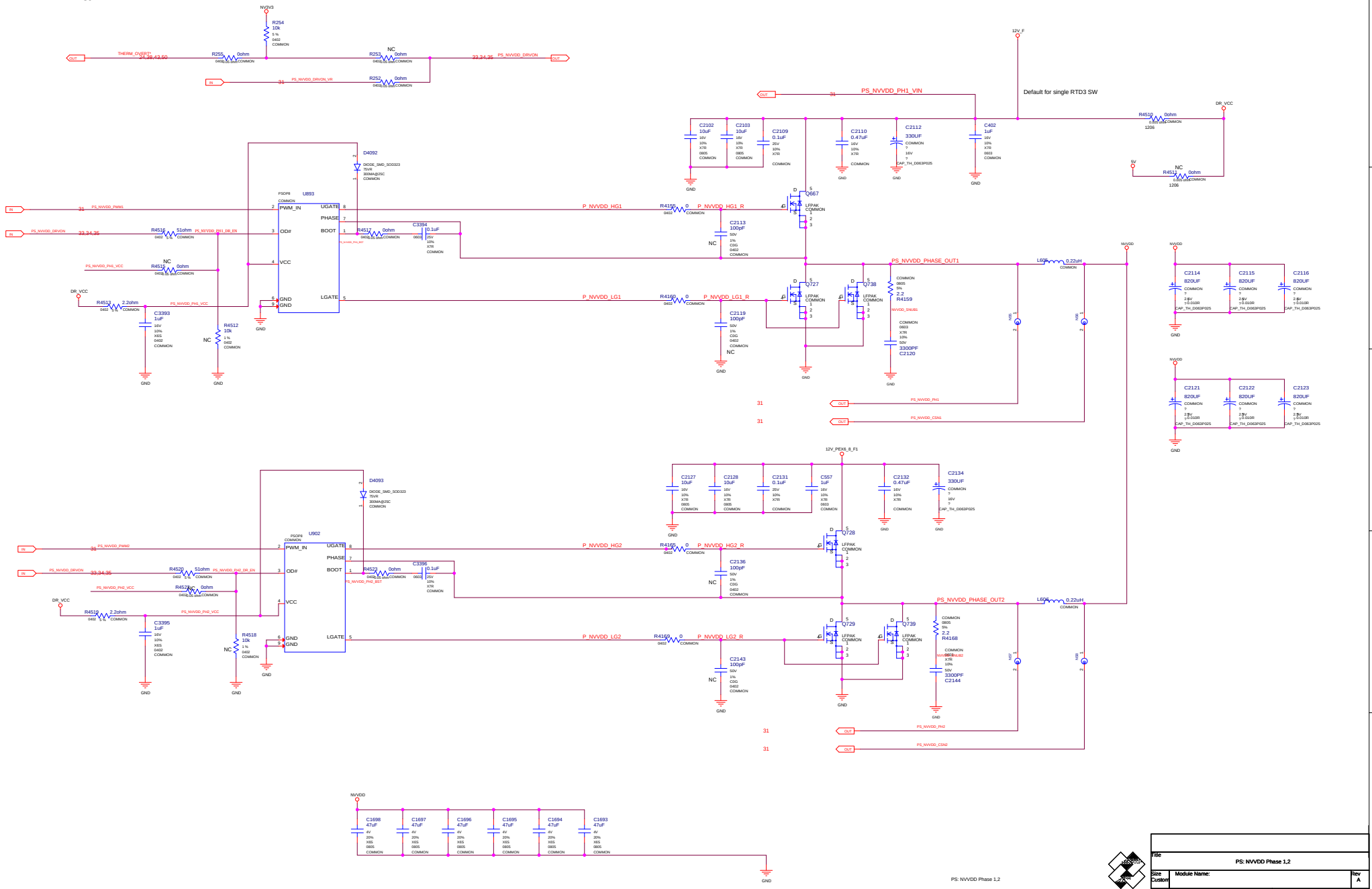
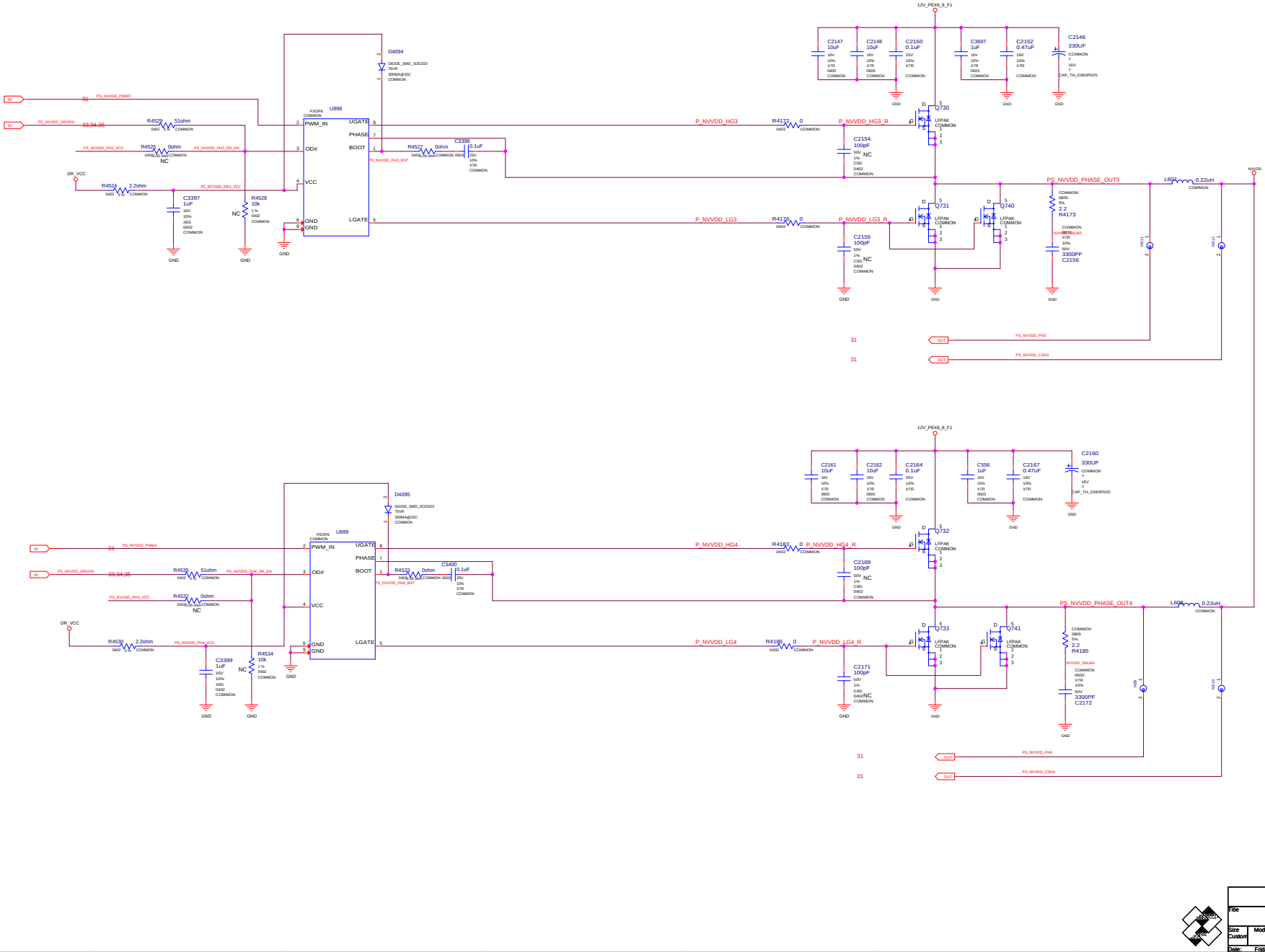
Page33: PS: NVVDD PH1&2



Page34: PS: NVVDD PH3&4



Title	PS: NVVDD Phase 3,4		
Size: Custom	Module Name:		Rev: A
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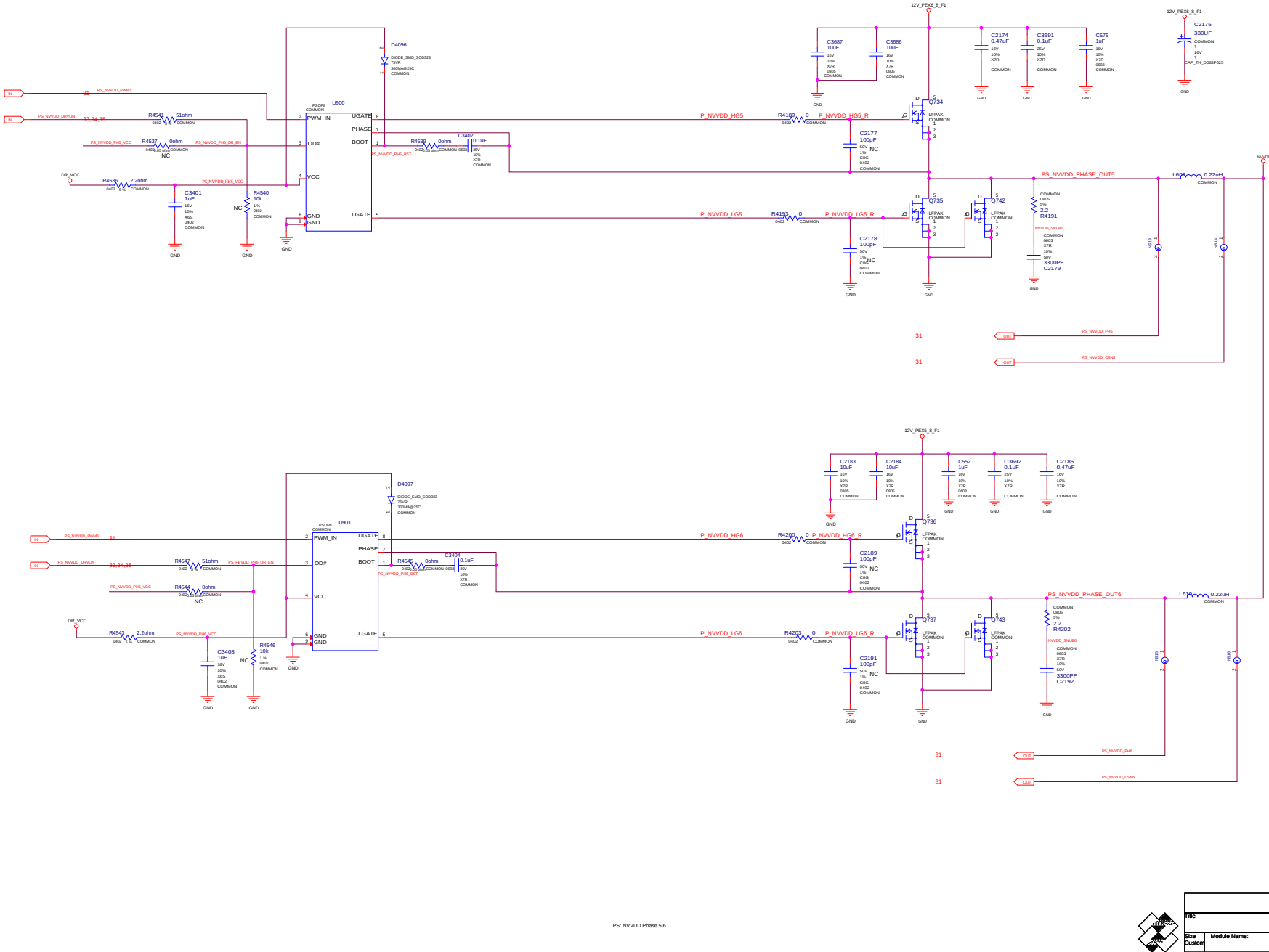
Page35: PS: NVVDD PH5&6



PS: NVVDD Phase 5,6

Title	PS: NVVDD Phase 5,6	
Size: Custom	Module Name:	Rev: A
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Page36: Input Power Balancing Switcher

Title	PS: Input Power Balancing Switcher
Size: Custom	Module Name:
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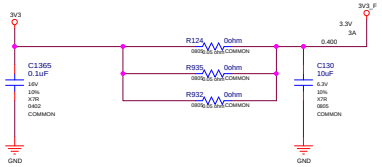
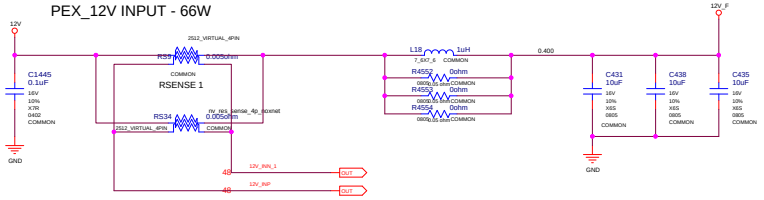
Page37: PS: Inputs, Filtering, and Monitoring

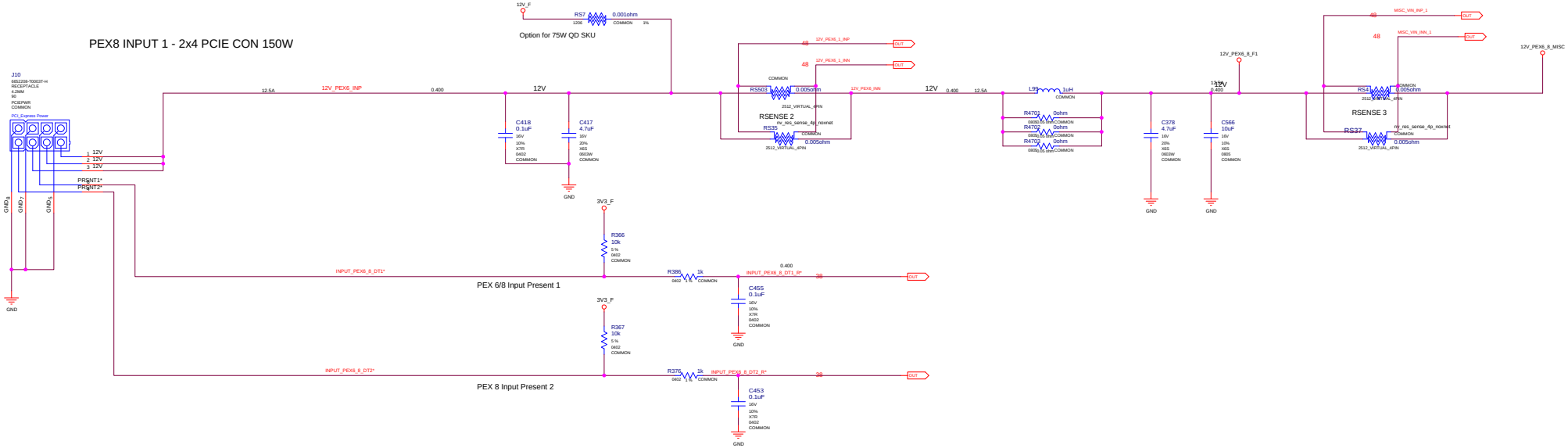
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



PS: Input, Filtering, and Monitoring

Title	PS: Input, Filtering, and Monitoring	
Size: Custom	Module Name:	Rev: A
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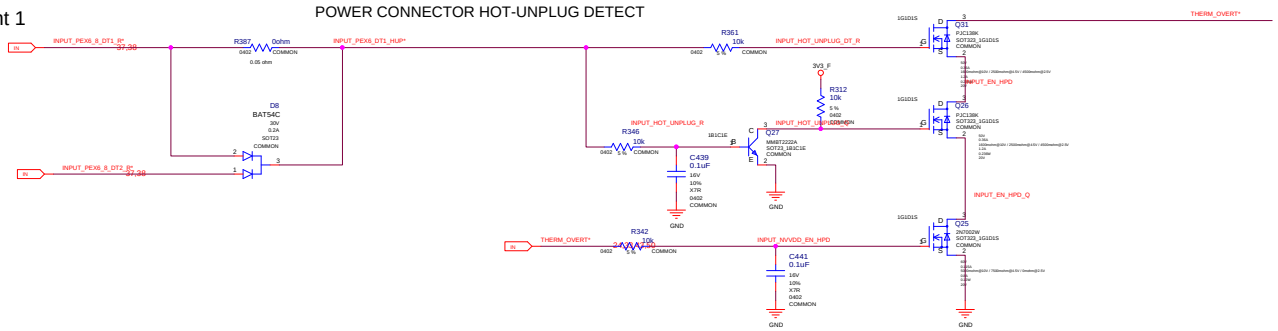
Page38: PS: STEERING, UNDER POWER BOOT & HOT-UNPLUG

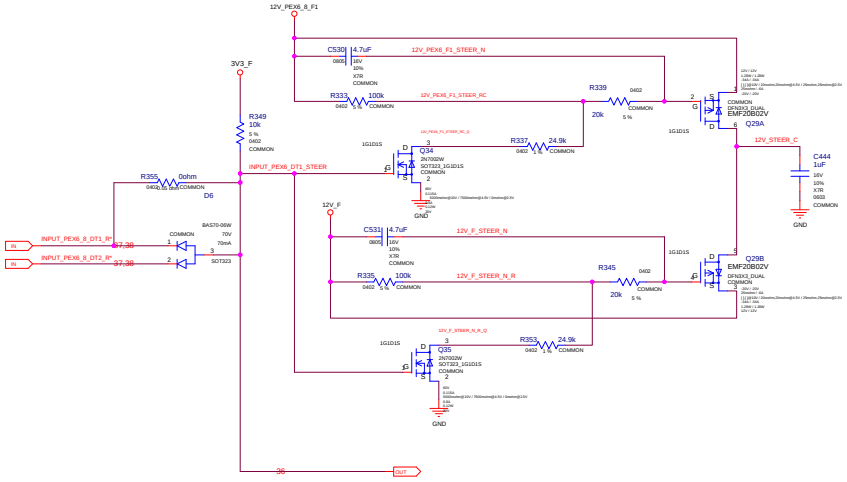
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

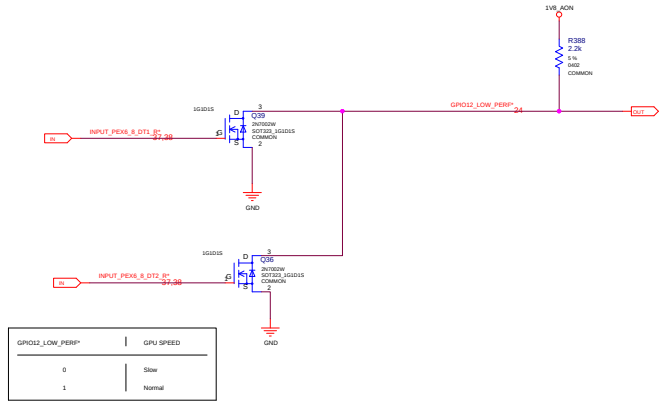


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



PS: STEERING, UPB & HOT-UNPLUG

Title	PS: STEERING, UPB & HOT-UNPLUG	
Size: Custom	Module Name:	Rev: A
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Page39: BUCKBOOST

Title	PS: Type-C BuckBoost
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Page40: PPC

Title	PD PPC
Size: Custom	Module Name:
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Page41: 12V & 3V3_A SWITCHER

Title	PS: 12V & 3V3_A SWITCHER	
Size: Custom	Module Name:	Rev: A
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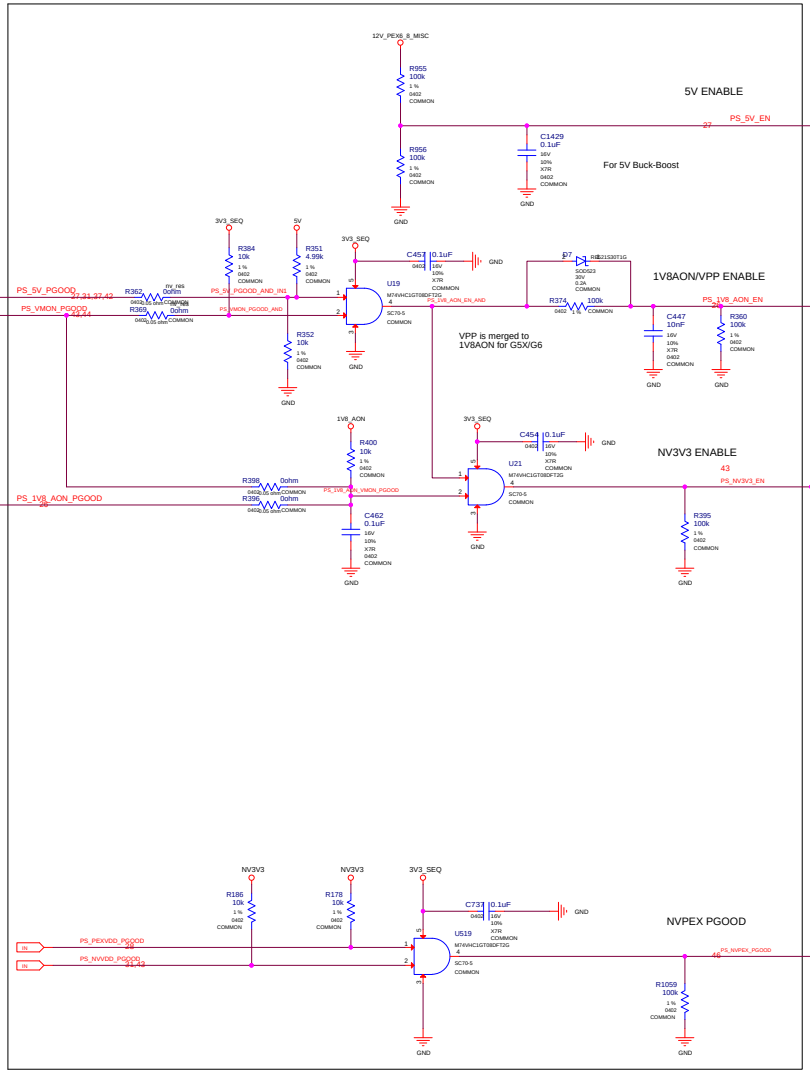
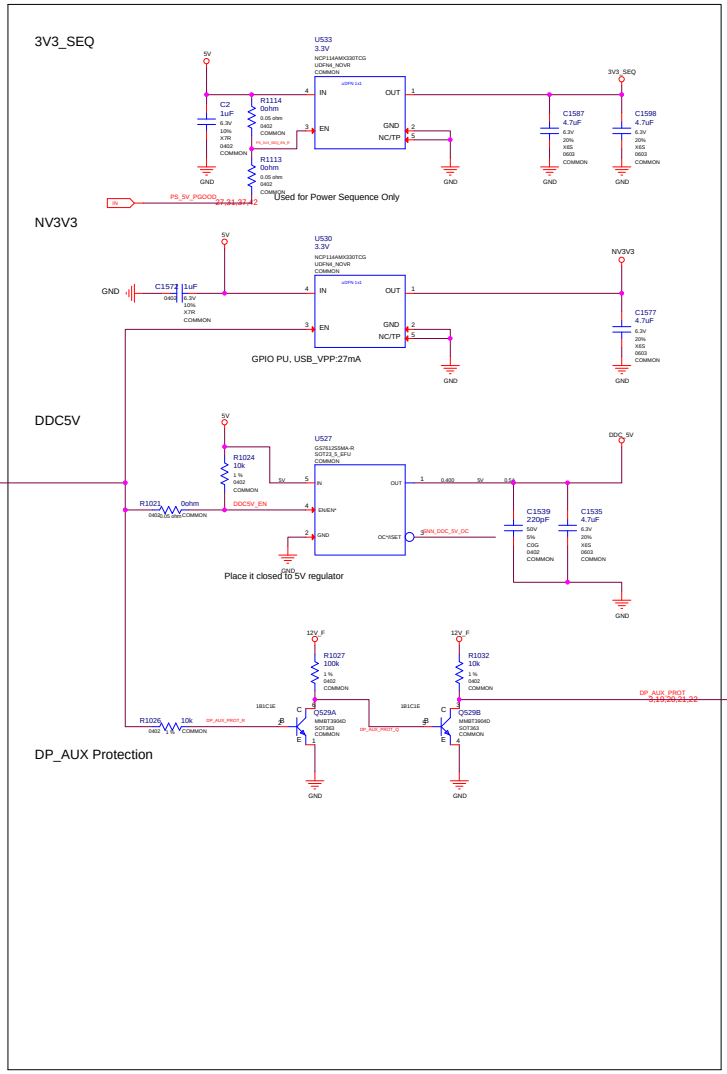
Page42: SEQ:5V,1V8,NV3V3 ENABLE





SEQ: 5V, 1V8, NV3V3 ENABLE

Title	SEQ: 5V, 1V8, NV3V3 ENABLE	
Size: Custom	Module Name:	Rev: A
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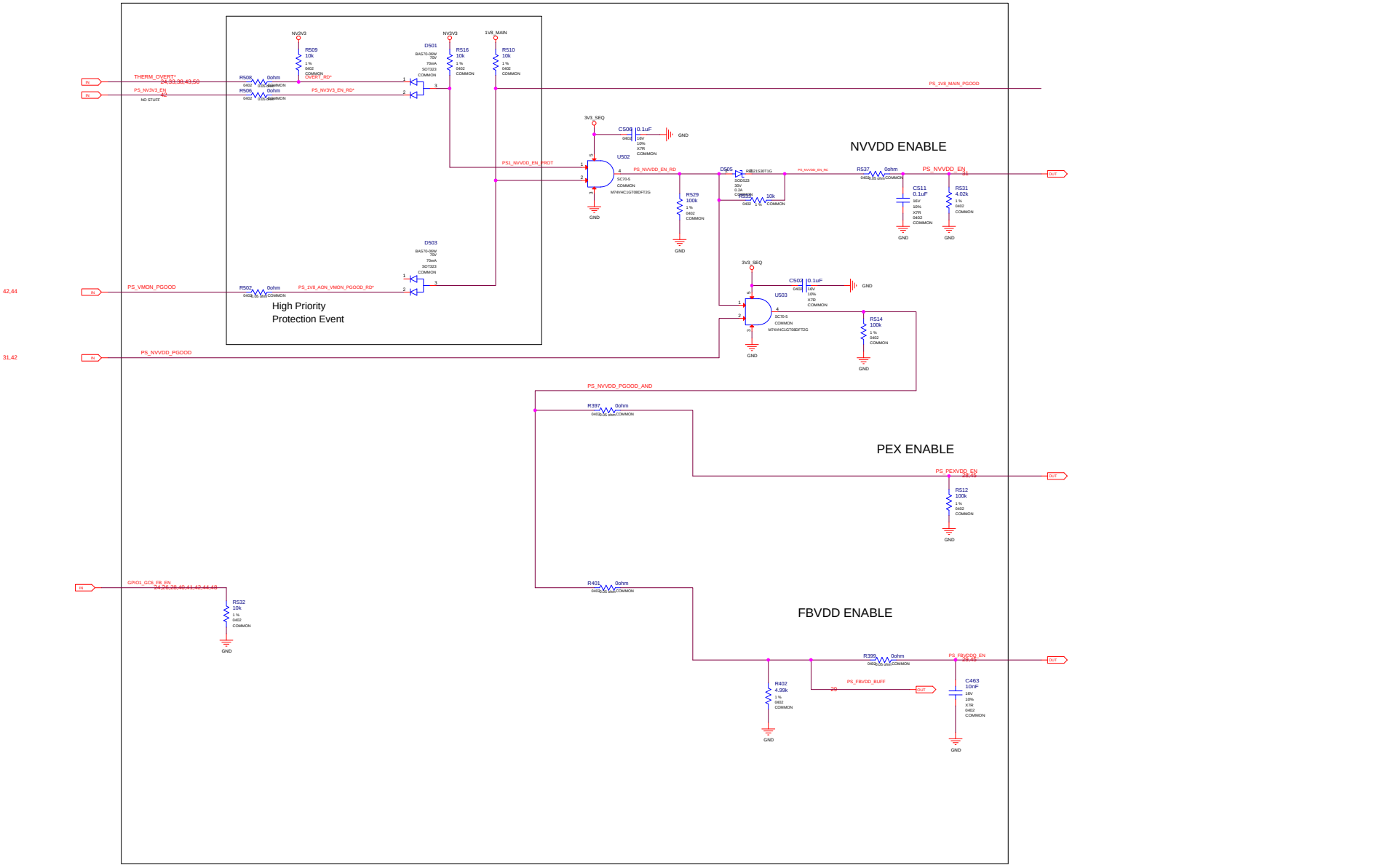
Page43: SEQ:NV,PEX,FB ENABLE



SEQ: NV, PEX, FB ENABLE

Title	SEQ: NV, PEX, FB ENABLE	
Size: Custom	Module Name:	Rev: A
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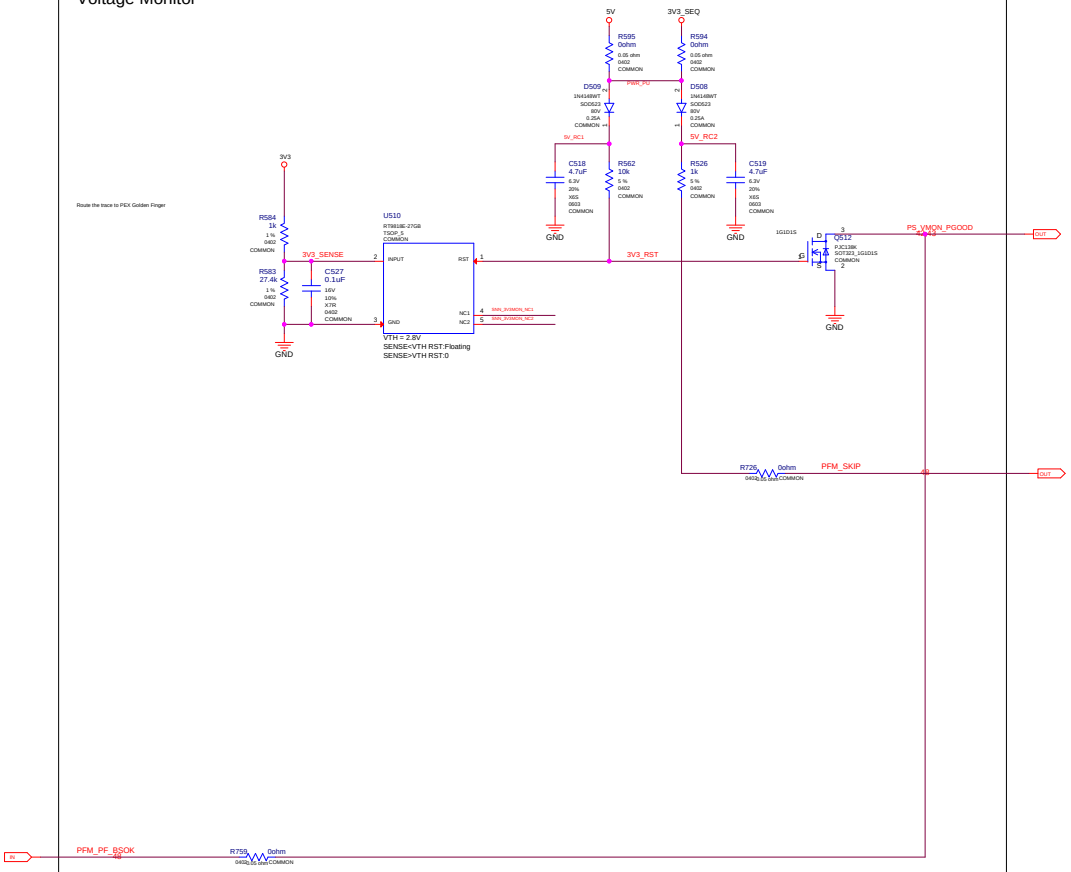
Page44: SEQUENCE:Voltage Monitor

Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

SEQ: VOLTAGE MONITOR

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Title: SEQ: VOLTAGE MONITOR

Size: Custom | Module Name: | Rev: A

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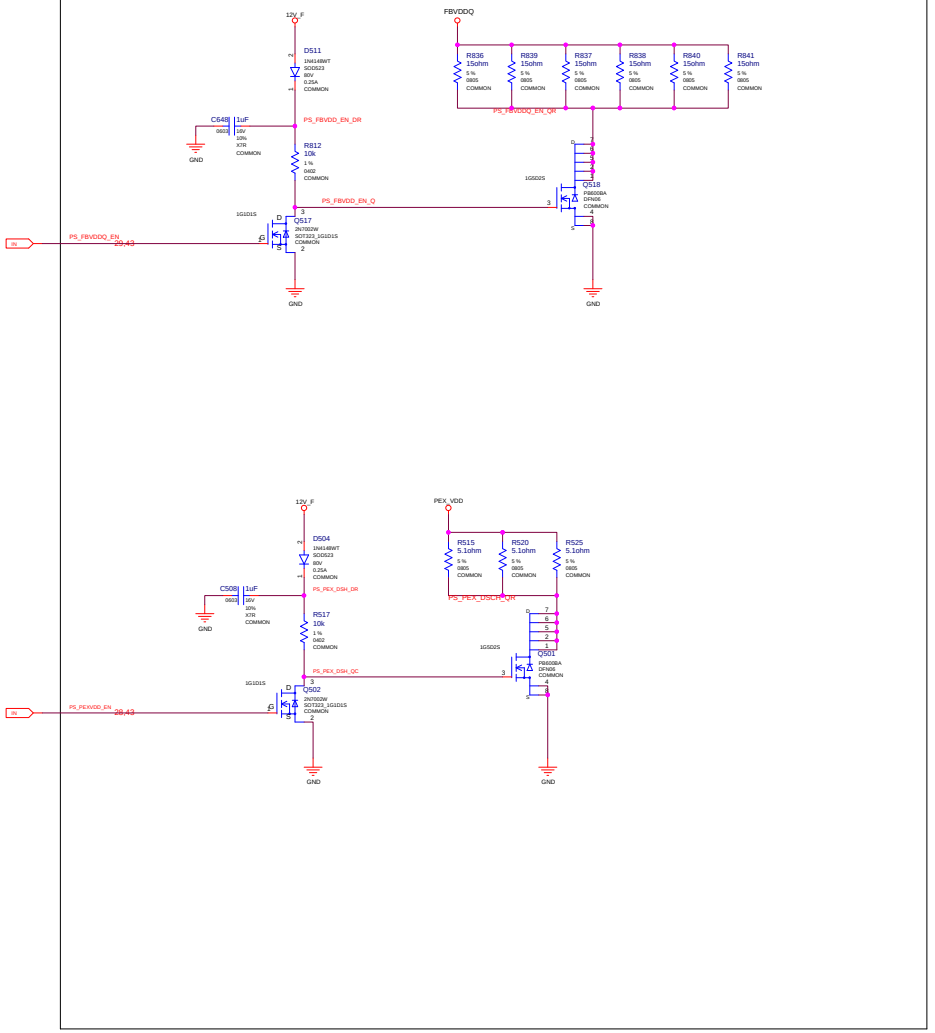
Page45: SEQUENCE:Discharge



SEQ: DISCHARGE

Title	SEQ: DISCHARGE		
Size: Custom	Module Name:		Rev: A
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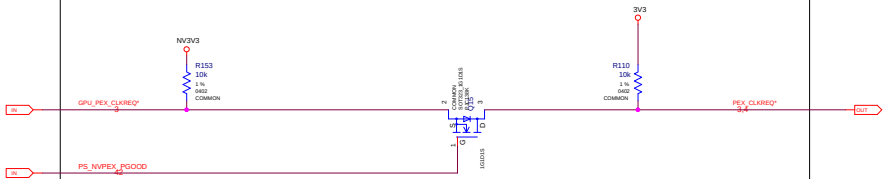
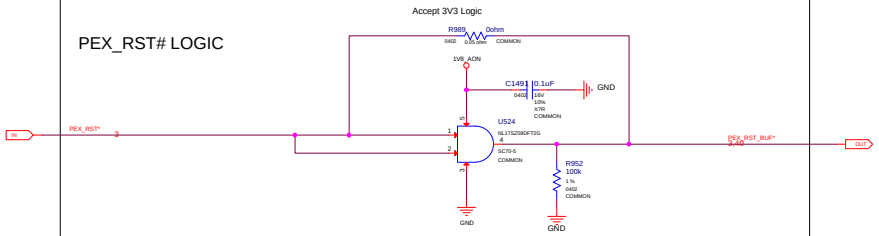
PEX_CLKREQ*



GPU_WAKE*

PEX_RST# LOGIC



SEQ: MISC

Title	SEQ: MISC	
Size: Custom	Module Name:	Rev: A
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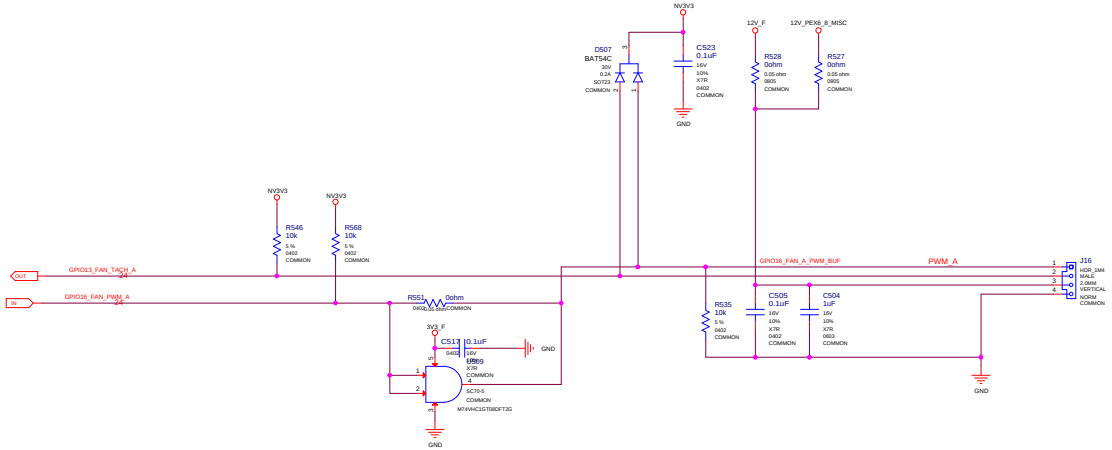
Page49: DUAL FAN



Title	DUAL FAN
Size: Custom	Module Name:
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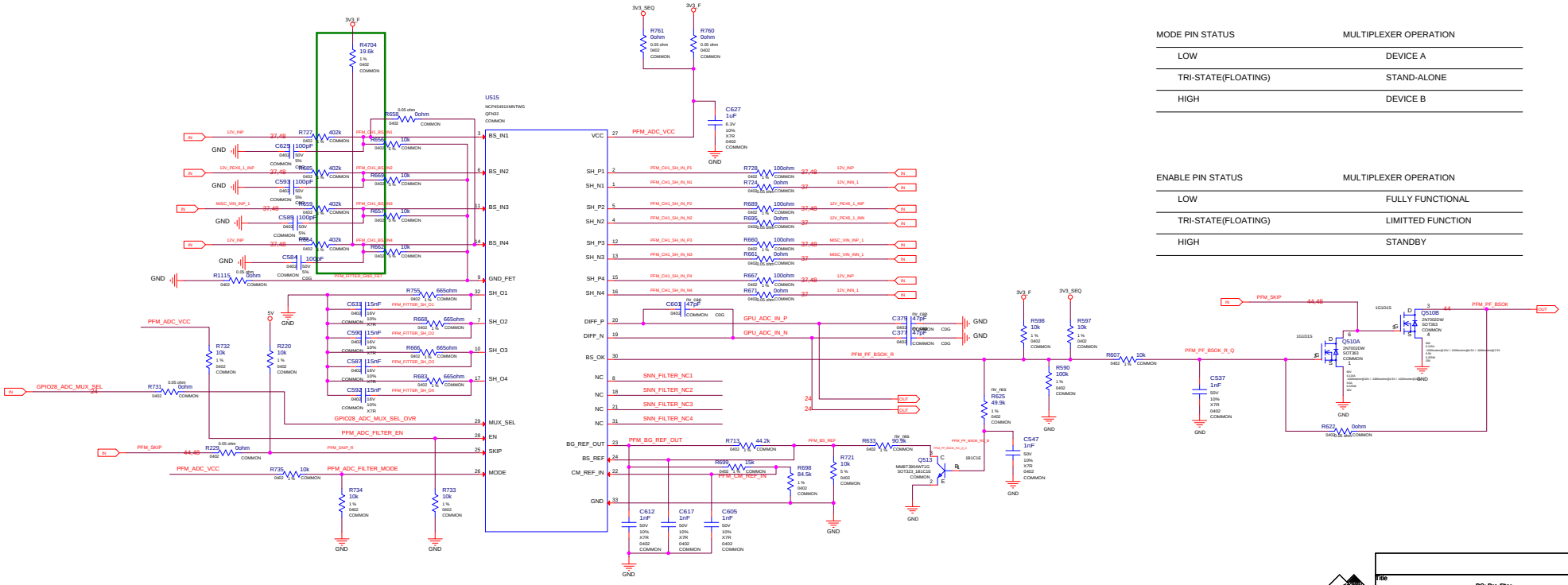

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY

Title	PS: Pre-filter	
Size: Custom	Module Name:	Rev: A
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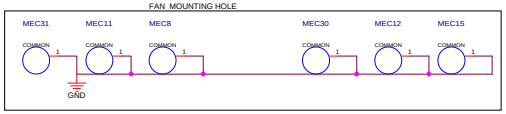
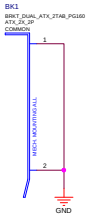
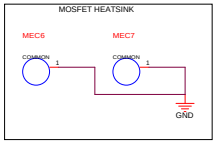
Page51: MECH

FAN_MOUNTING HOLE



Brackets:





BACK STIFFENER:

MECH

Title	MECH		
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Page52: PTC

PTC

Title	PTC
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