P403-B00 DESIGN -- G84-200, 256 MB DDR2,DVI-I, VGA, HDTV

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REV HISTORY

96/10/30 Design change to G84-G53 Large size 8400GS circuit PCB LP costdown version

1. Remove FBC 2ND 0..63
2. Remove TMDS C HDMI circuit
3. Remove SCART function form DACB
4. Change Fancontrol func to Direct driver
5. Change FBVDDQ PWM power solution to 431 LDO solution

sku	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10403-0000-200	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0020	600-10403-0020-200	P403-B00 G86-300 459/400MHz 256MB 16Mx16 BGA84 GDDR2 DVI-I-DL+VGA+HDTV-Out
2	SKU0021	600-10403-0021-200	P403-B00 G84-200 459/400MHz 256MB 16Mx16 BGA84 GDDR2 DVI-I-DL+VGA+HDTV-Out
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11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TABLE OF CONTENTS & REVISION HISTORY

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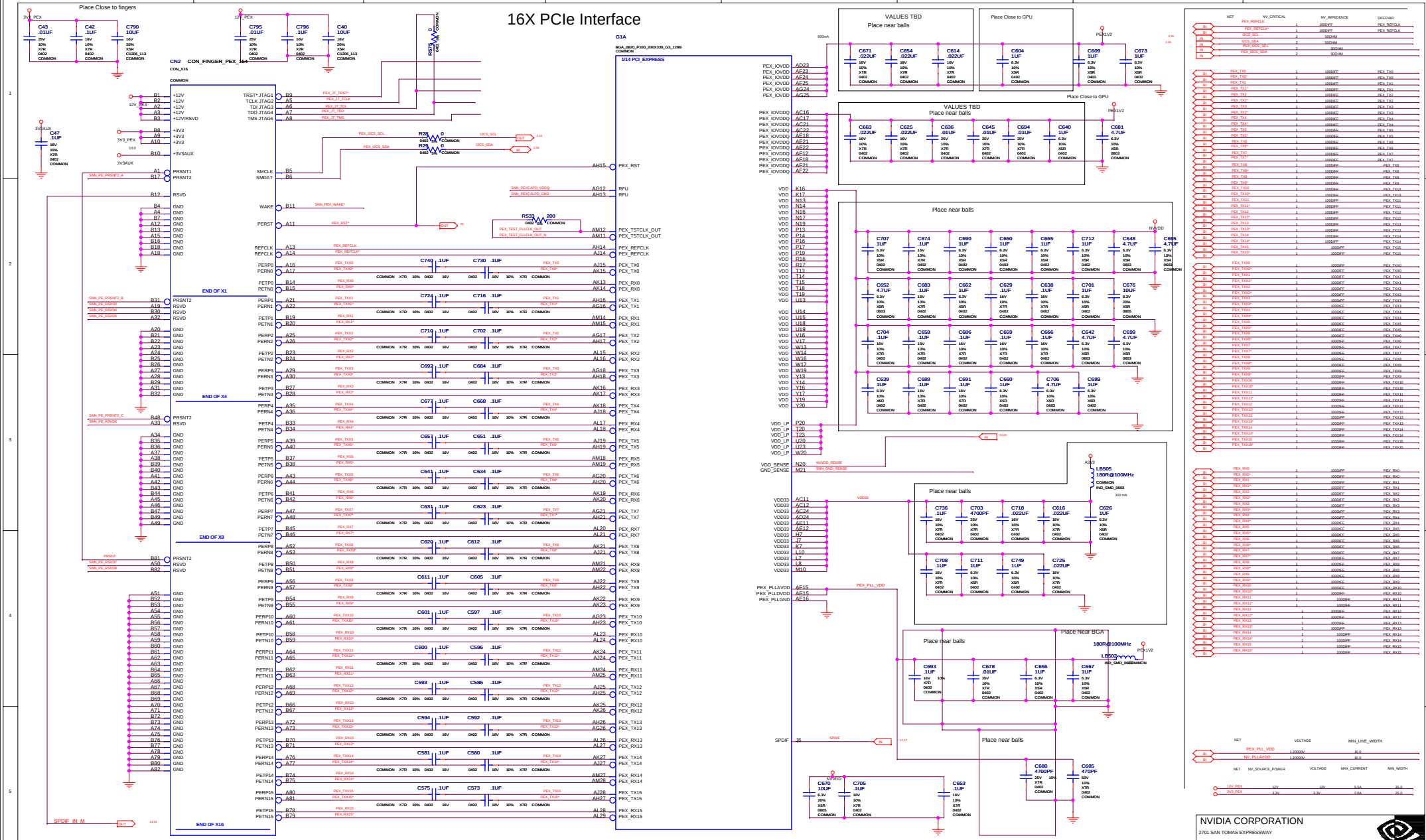
16X PCIe Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS 16X, NVVDD DECOUPLING CAPS,PEX_IOVDD/Q DECOUPLING CAPS

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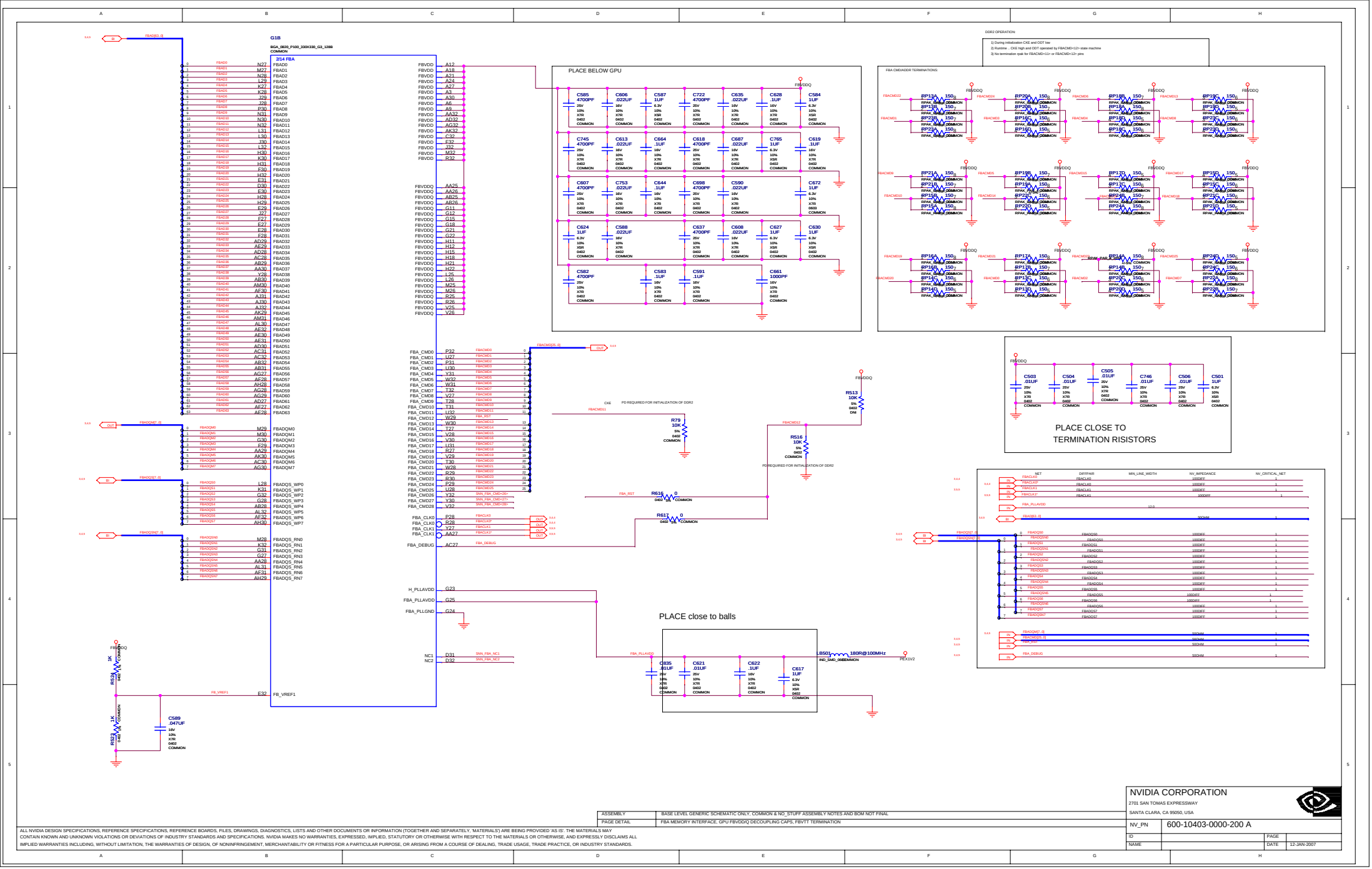

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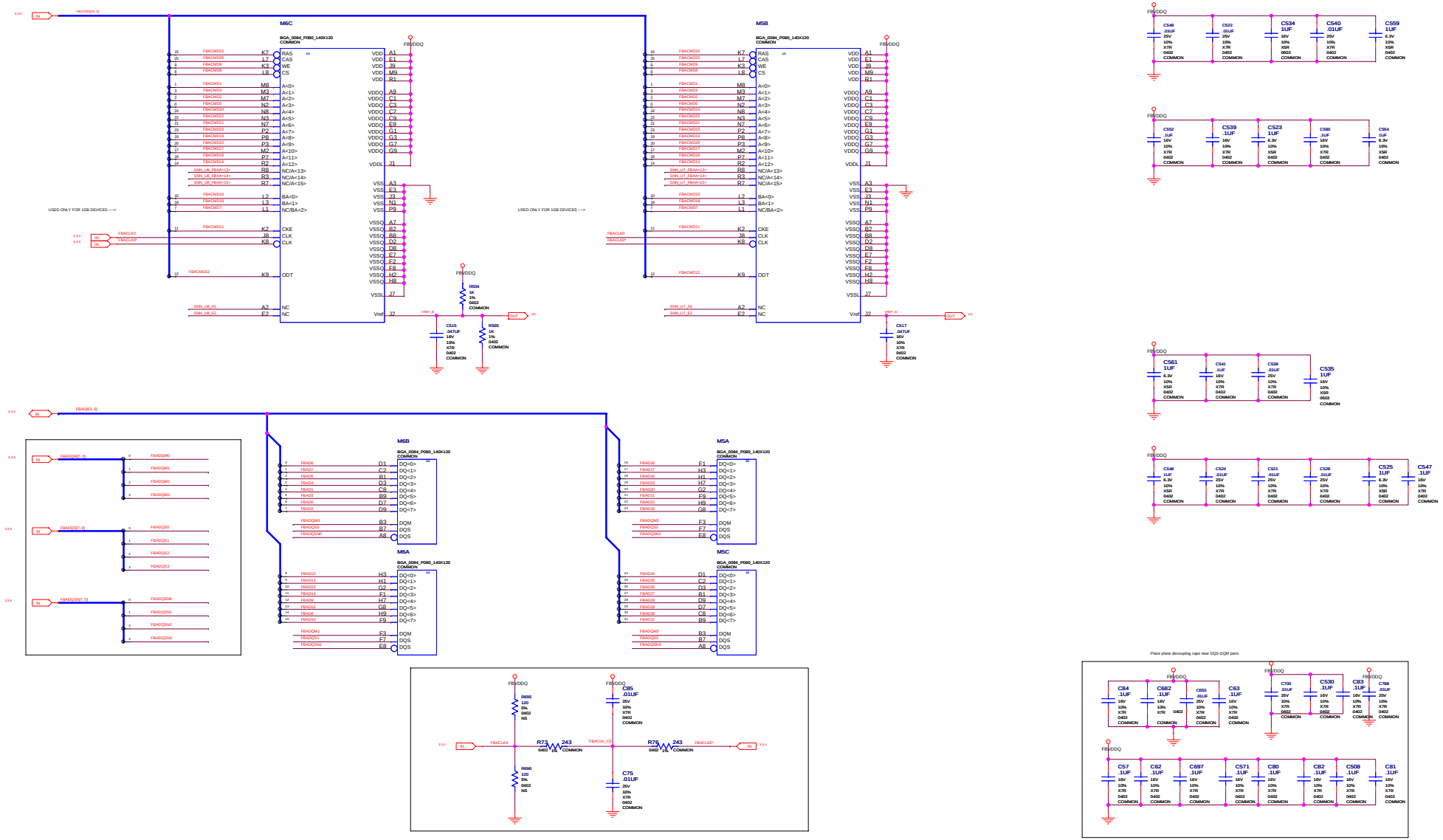
FBA MEMORY 1st bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16Mx16 DDR2 MEMORIES, BANK 0..31

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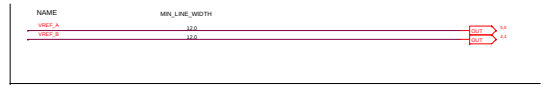
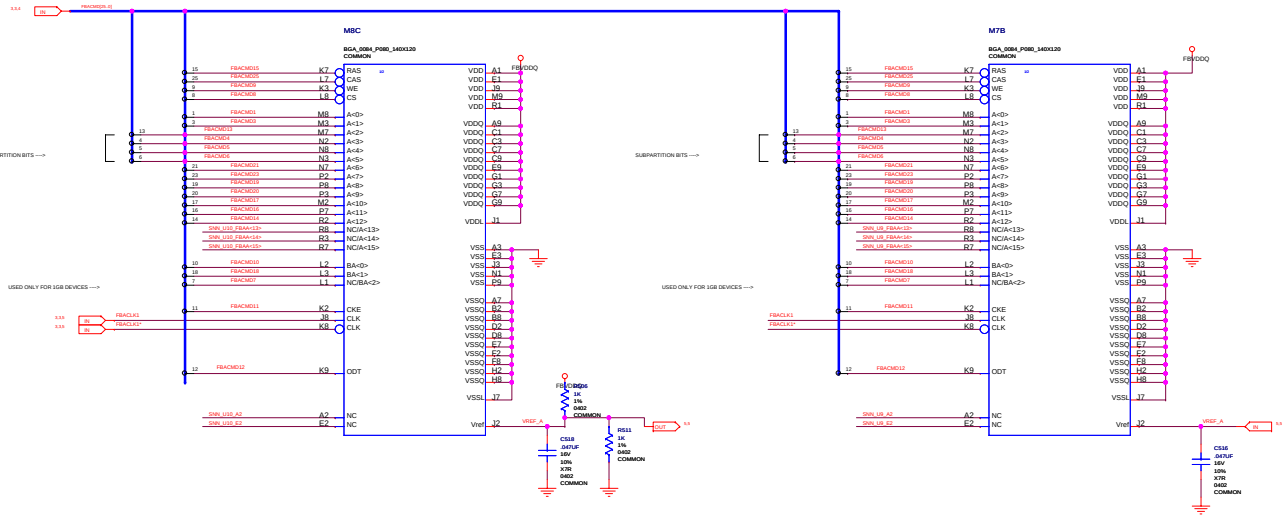
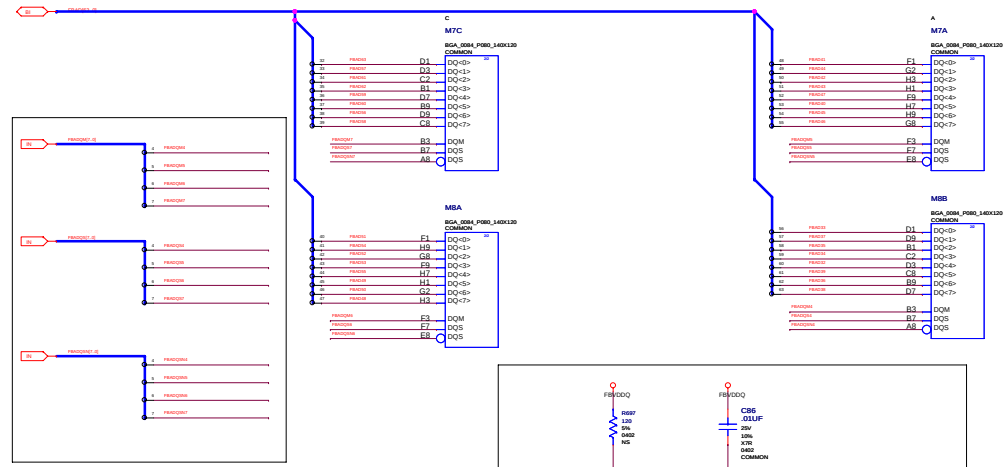
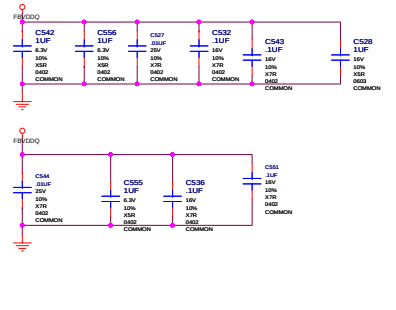
FBA MEMORY 1st bank 32..63

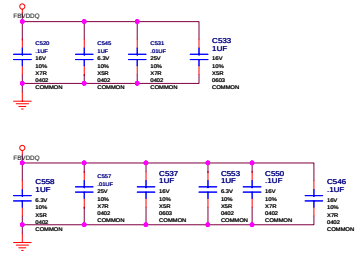
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY











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PAGE DETAIL	FBA 16Mx16 DDR2 MEMORIES, 1ST BANK 32..63

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G1C
BGA_0820_P100_330X330_G3_128B
COMMON
3/14 FBC
FBVDDQ
C65 .01UF 25V 10% X7R 0402 COMMON
C643 .01UF 25V 10% X7R 0402 COMMON
C720 .01UF 25V 10% X7R 0402 COMMON
C502 .01UF 25V 10% X7R 0402 COMMON
C696 1UF 6.3V 10% X5R 0402 COMMON
PLACE CLOSE TO TERMINATION RISISTORS
DDR2 OPERATION:
1) During initialization CKE and ODT low
2) Runtime - . CKE high and ODT operated by debug state machine
3) No termination rpak for CKE or DEBUG pins
FBC CMD/ADDR TERMINATIONS:
NET
DIFFPAIR
MIN_LINE_WIDTH
NV_IMPEDANCE
NV_CRITICAL_NET
FBC_PLLAVDD
FBCAL_PD
FBCAL_PU
FBCAL_TERM
R529 40.2 0402 1% COMMON
R528 40.2 0402 1% COMMON
R530 0 0402 1% COMMON
R535 1K 0402 1% COMMON
R536 1K 0402 1% COMMON
C595 .047UF 16V 10% X7R 0402 COMMON
C727 .01UF 25V 10% X7R 0402 COMMON
C717 .1UF 16V 10% X7R 0402 COMMON
C735 1UF 6.3V 10% X5R 0402 COMMON
C768 1UF 6.3V 10% X7R 0603 COMMON
LB505 180R@100MHz IND_SMD_0603 COMMON
PEX1V2
Place close to balls
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ASSEMBLY BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL FBC MEMORY INTERFACE, GPU FBVTT, FBVDDQ
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Primary Display (DACA), Slim DB15

DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACA_RED	1	50OHM	
DACA_GREEN	1	50OHM	
DACA_BLUE	1	50OHM	
DACA_RED_C	1	50OHM	
DACA_GREEN_C	1	50OHM	
DACA_BLUE_C	1	50OHM	
DACA_HSYNC	2	50OHM	
DACA_VSYNC	2	50OHM	
AVB	2	50OHM	
AVB	2	50OHM	
DACA_HSYNC_BUF	2	50OHM	
DACA_VSYNC_BUF	2	50OHM	
DACA_HSYNC_C	2	50OHM	
DACA_VSYNC_C	2	50OHM	
I2CA_SCL	2	50OHM	
I2CA_SDA	2	50OHM	
I2CA_SCL_T	2	50OHM	
I2CA_SDA_T	2	50OHM	
I2CA_SCL_C	2	50OHM	
I2CA_SDA_C	2	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACA_VDD	3.30000V	0.07A	16.0
DACA_VREF			10.0
DACA_RSET			10.0

DACA RGB-FILTER

PLACE NEAR SYNC BUFFER

FOR ESD DIODES

Place in output filter section!

SOUTH

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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Secondary Display (DACC), DB15

DACC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACC_RED	1	50OHM	
DACC_GREEN	1	50OHM	
DACC_BLUE	1	50OHM	
DACC_RED_C	1	50OHM	
DACC_GREEN_C	1	50OHM	
DACC_BLUE_C	1	50OHM	
DACC_HSYNC	2	50OHM	
DACC_VSYNC	2	50OHM	
CVB	2	50OHM	
CHB	2	50OHM	
DACC_HSYNC_BUF	2	50OHM	
DACC_VSYNC_BUF	2	50OHM	
DACC_HSYNC_C	2	50OHM	
DACC_VSYNC_C	2	50OHM	
I2CB_SCL	2	50OHM	
I2CB_SDA	2	50OHM	
I2CB_SCL_T	2	50OHM	
I2CB_SDA_T	2	50OHM	
I2CB_SCL_C	2	50OHM	
I2CB_SDA_C	2	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACC_VDD	3.30000V	0.14A	18.0
DACC_VREF			10.0
DACC_RSET			10.0

DACC RGB-FILTER

MIDDLE

FOR ESD DIODES

Place in output filter section!

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID

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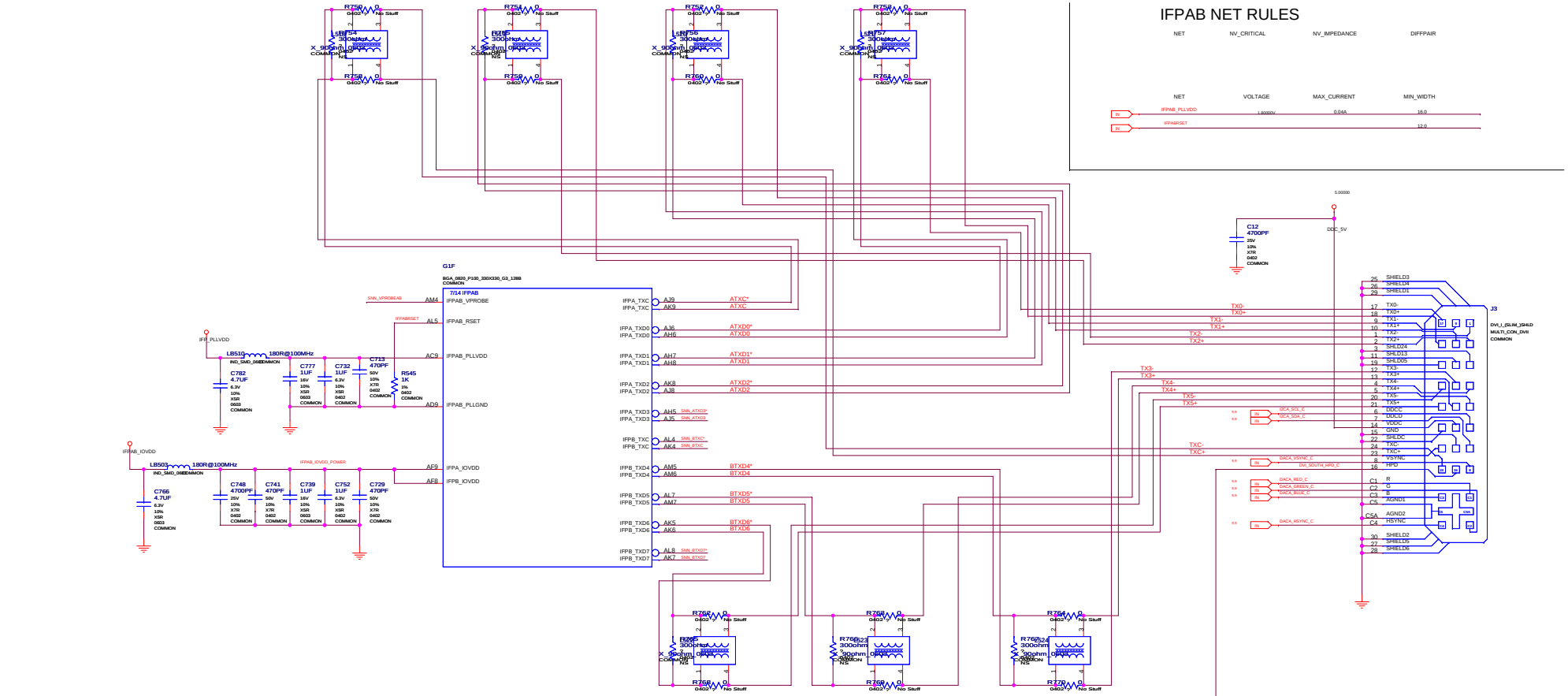
INTERNAL TMDS .. LINK A & B



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PAGE DETAIL	TMDS LINK A & PU's, DVI CONNECTOR SOUTH

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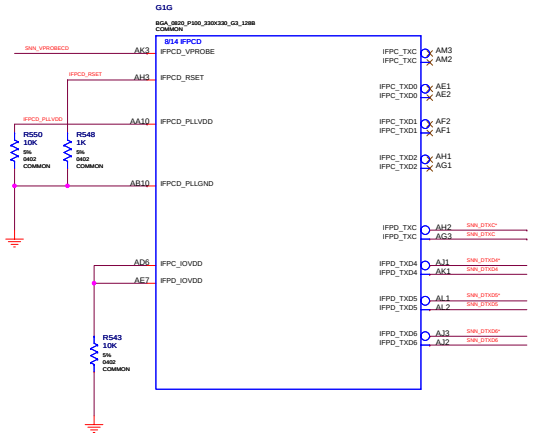
INTERNAL TMDS .. LINK C

IFPAB NET RULES

NET	MIN_WIDTH
IFPCD_RSET	12.0

NET RULES

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPCD_PLLVDD	3.30000	0.04	16.0
IFPD_IOVDD	0.000000	0	10.0
IFPC_IOVDD	3.30000	0.15	16.0



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PAGE DETAIL	TMDS LINK C

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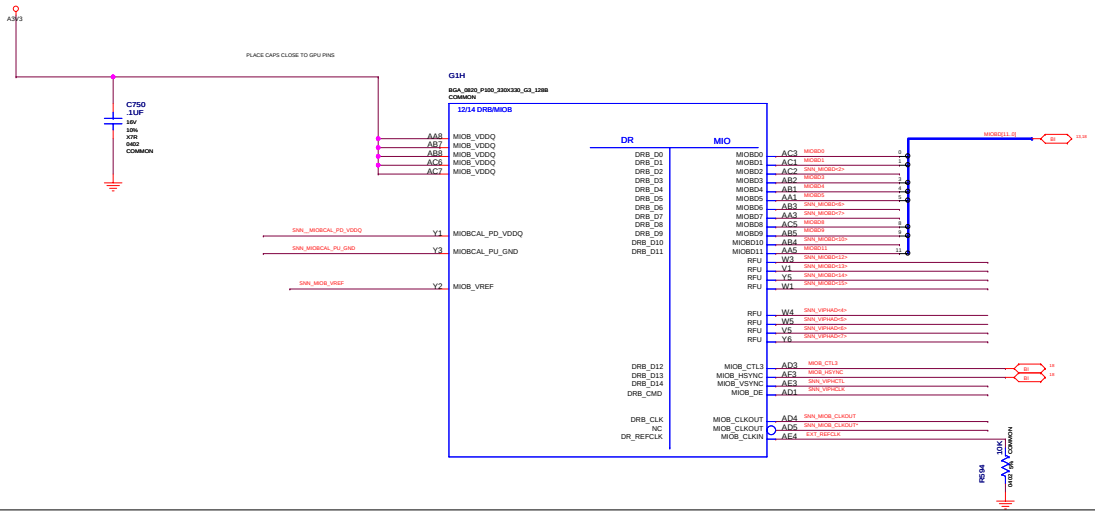
G3 VIP/MIOB

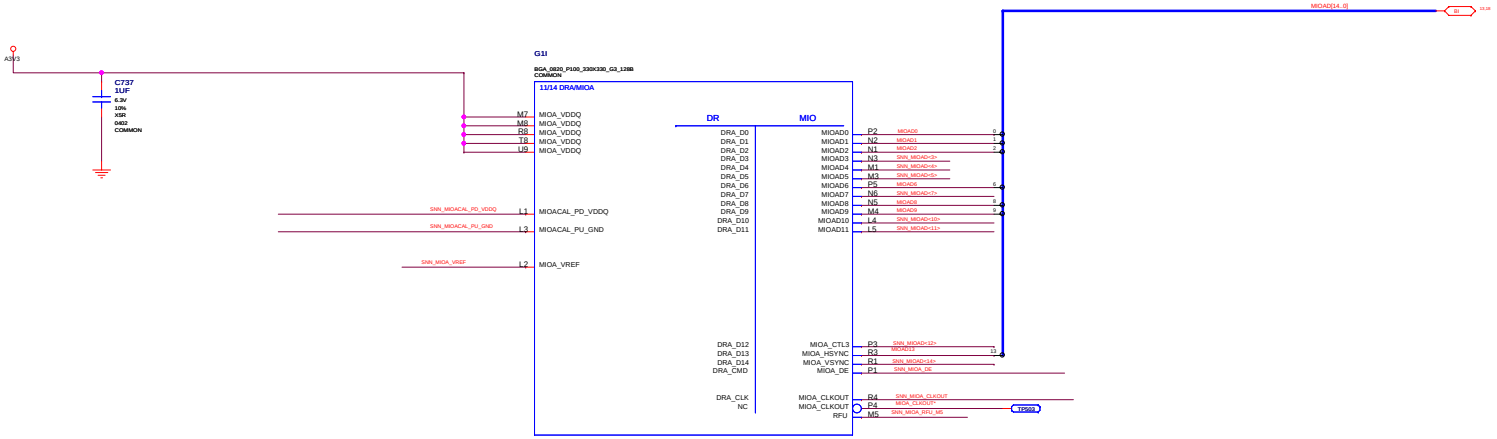


MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
MIOAD[14..0]		50OHM	
EXT_REFCLK	2	50OHM	
MIOA_CLKOUT	2	50OHM	
MIOA_DE	2	50OHM	
MIOBD[11..0]	2	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	1.25000V		12.0
MIOACAL_PD_VDDQ	2.50000V		12.0
MIOACAL_PU_GND	0.0000000V		12.0

G3 MIOA



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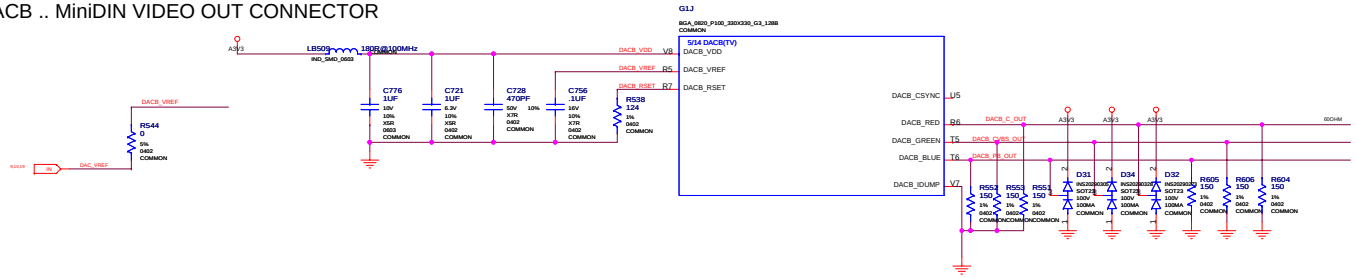
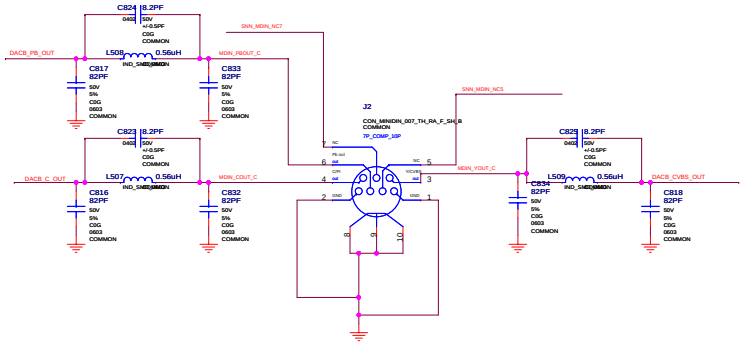
DACB .. MiniDIN VIDEO OUT CONNECTOR





DACB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACB_C_OUT	1	56OHM	
MDIN_COUT_C	1	56OHM	
DACB_CVBS_OUT	1	56OHM	
MDIN_YOUT_C	1	56OHM	
DACB_PB_OUT	1	56OHM	
MDIN_PBOUT_C	1	56OHM	
MDIN_SCL_C	2	50OHM	
MDIN_SDA_C	2	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACB_VDD	3.30000V	0.07A	16.0
DACB_VREF			16.0
DACB_RSET			16.0

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, SYNC STRIPPER, MINIDIN CONNECTOR NORTH,HDTV HEADER

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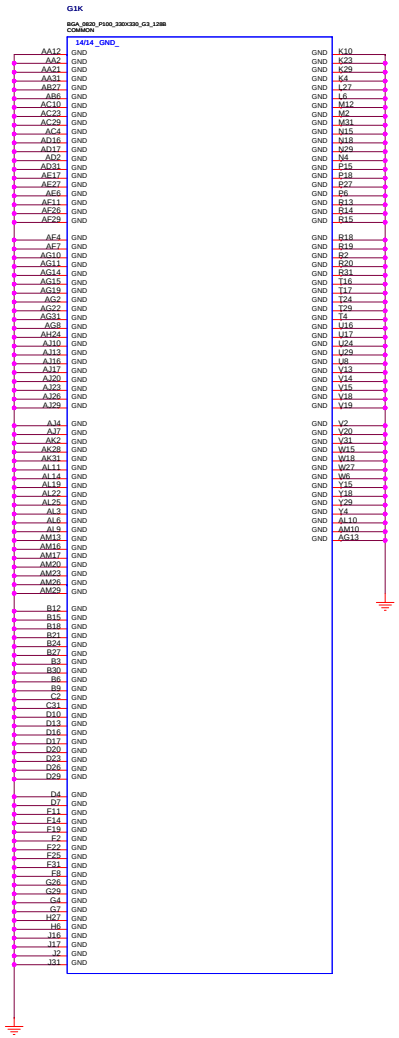
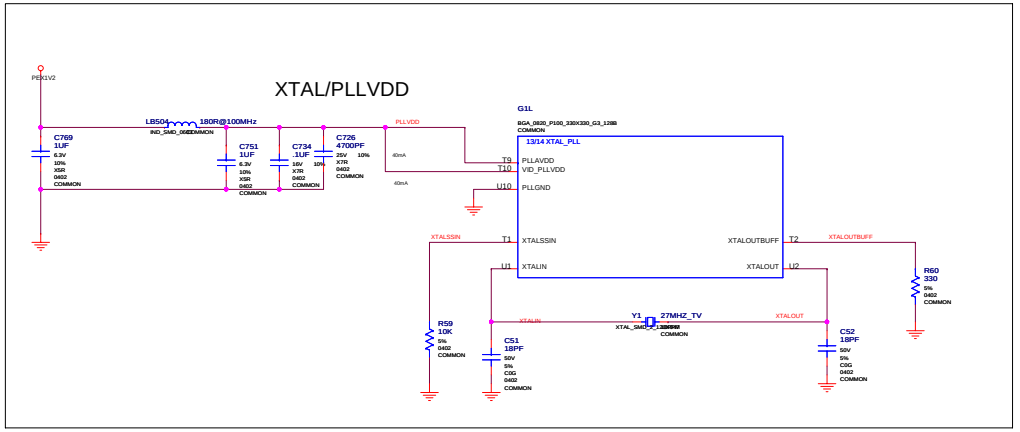
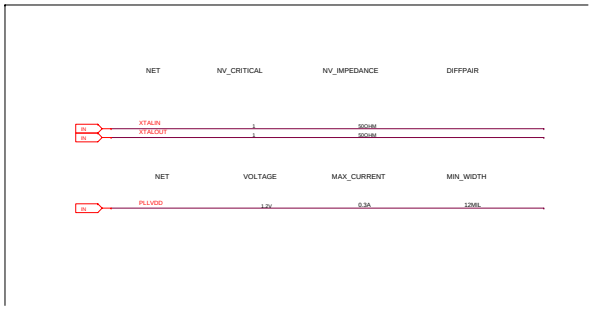
GPU GND CONNECTION, XTAL







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	GPU GND CONNECTION, XTAL

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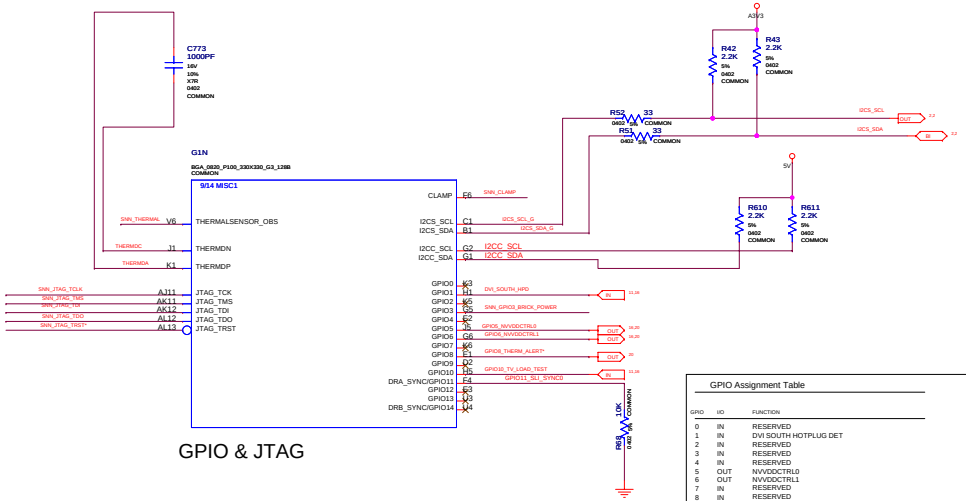
Use 10MIL Guard(GND) Trace around THERMDC and THERMDA

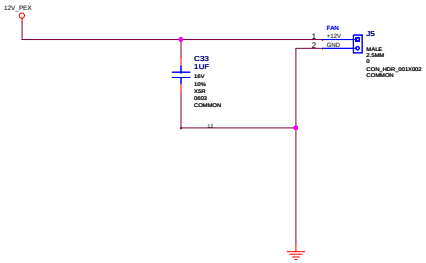


GPIO & JTAG

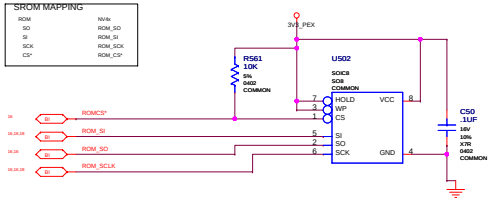
GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	RESERVED
1	IN	DVI SOUTH HOTPLUG DET
2	IN	RESERVED
3	IN	RESERVED
4	IN	RESERVED
5	OUT	NVVDDCTRL0
6	OUT	NVVDDCTRL1
7	IN	RESERVED
8	IN	RESERVED
9	OUT	FAN Control(ON/OFF)
10	OUT	RESERVED
11	IN	SLI_SYNC0
12	IN	RESERVED
13	IN	RESERVED
14	IN	RESERVED

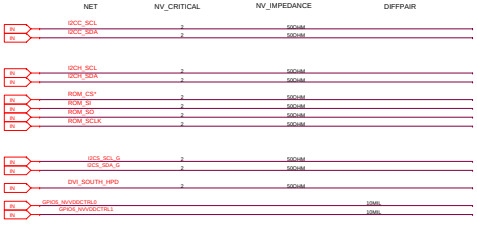
GPIO ON/OFF FAN Control

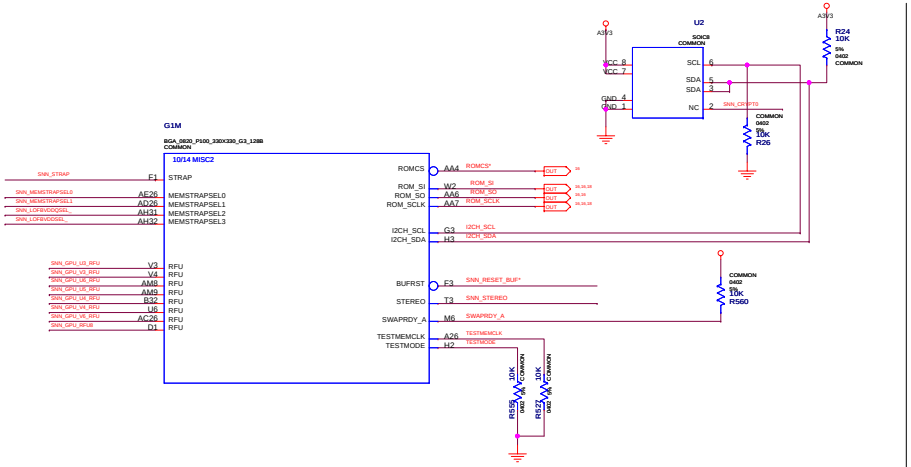


BIOS (serial)



MISC NET RULES





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	JTAG, BIOS ROM, HDCP ROM, FAN CONTROL, GPIO

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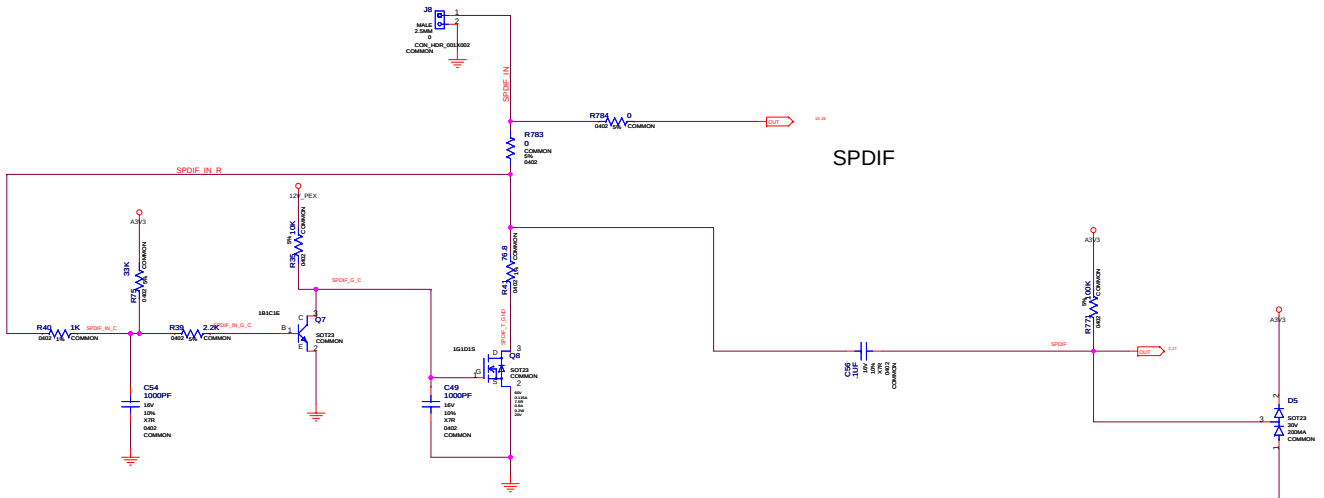
SPDIF



SPDIF

place close to GPU

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF

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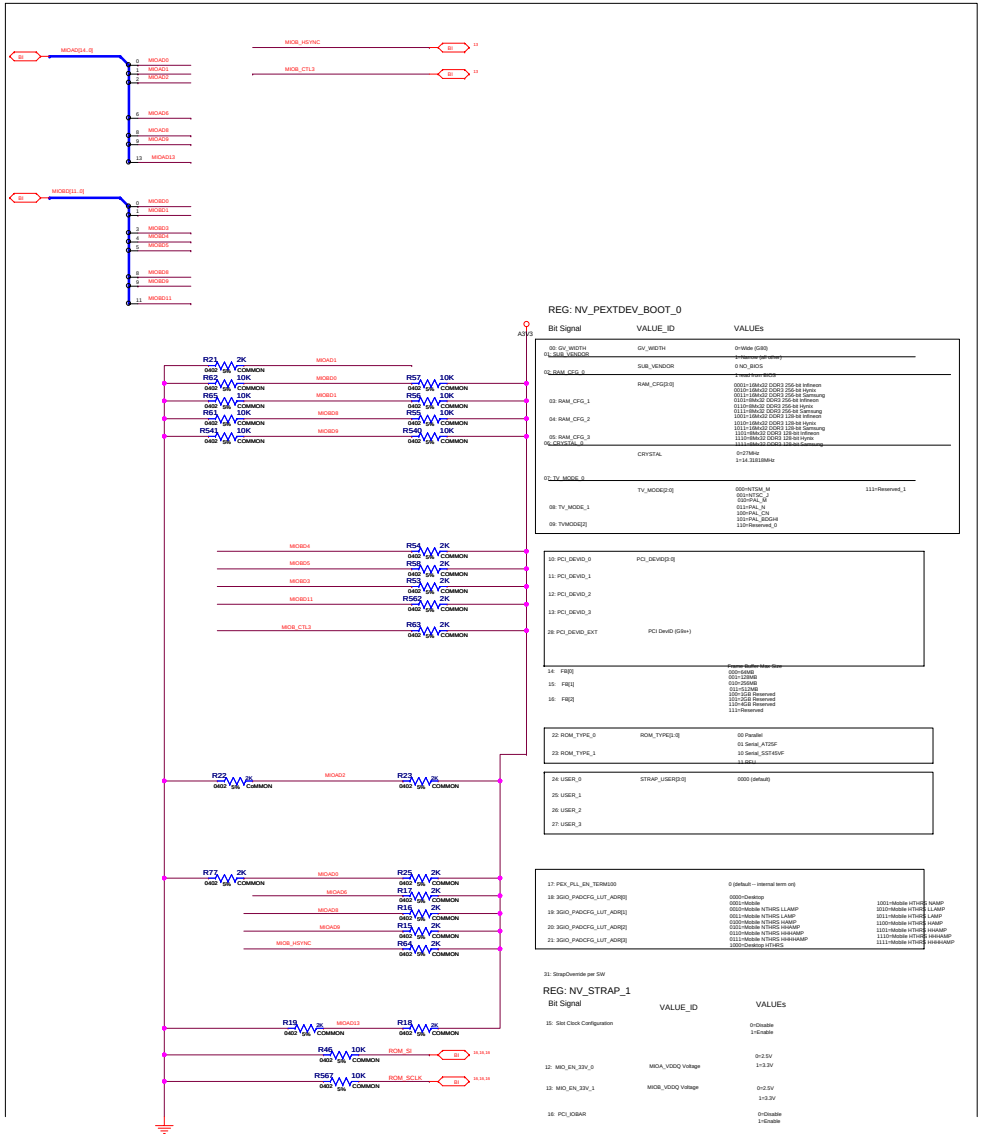
BIOS, Straps, Misc

Straps

Assembly: BIOS



REG: NV_PEXTDEV_BOOT_0

Bit	Signal	VALUE_ID	VALUEs
00: GV_WIDTH		GV_WIDTH	0=Wide (G80)
01: SUB_VENDOR		SUB_VENDOR	1=Narrow (all other) 0 NO_BIOS 1 Intel from BIOS
02: RAM_CFG_0		RAM_CFG[3:0]	0000=16Mx32 DDR3 256-bit Infineon 0010=16Mx32 DDR3 256-bit Hynix 0011=16Mx32 DDR3 256-bit Samsung 0100=8Mx32 DDR3 128-bit Elpida 0110=8Mx32 DDR3 256-bit Hynix 0111=8Mx32 DDR3 256-bit Samsung 1000=16Mx32 DDR3 128-bit Infineon 1010=16Mx32 DDR3 128-bit Hynix 1011=16Mx32 DDR3 128-bit Samsung 1101=8Mx32 DDR3 128-bit Infineon 1110=8Mx32 DDR3 128-bit Hynix 1111=8Mx32 DDR3 128-bit Samsung
03: RAM_CFG_1			
04: RAM_CFG_2			
05: RAM_CFG_3			
06: CRYSTAL_0		CRYSTAL	0=27MHz 1=14.31818MHz
07: TV_MODE_0		TV_MODE[2:0]	000=NTSM_M 001=NTSC_J 010=PAL_M 011=PAL_N 100=PAL_BGHI 101=PAL_DGHI 110=Reserved_0 111=Reserved_1
08: TV_MODE_1			
09: TVMODE[3]			

10: PCI_DEVID_0	PCI_DEVID[3:0]	
11: PCI_DEVID_1		
12: PCI_DEVID_2		
13: PCI_DEVID_3		
28: PCI_DEVID_EXT	PCI DevID (G80++)	

14: FB[0]	Frame Buffer Max Size	000=64MB 001=128MB 010=256MB 011=512MB 100=1GB Reserved 101=2GB Reserved 110=4GB Reserved 111=Reserved
15: FB[1]		
16: FB[2]		

22: ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F 10 Serial_SST45VF 11 RSV
23: ROM_TYPE_1		

24: USER_0	STRAP_USER[3:0]	0000 (default)
25: USER_1		
26: USER_2		
27: USER_3		

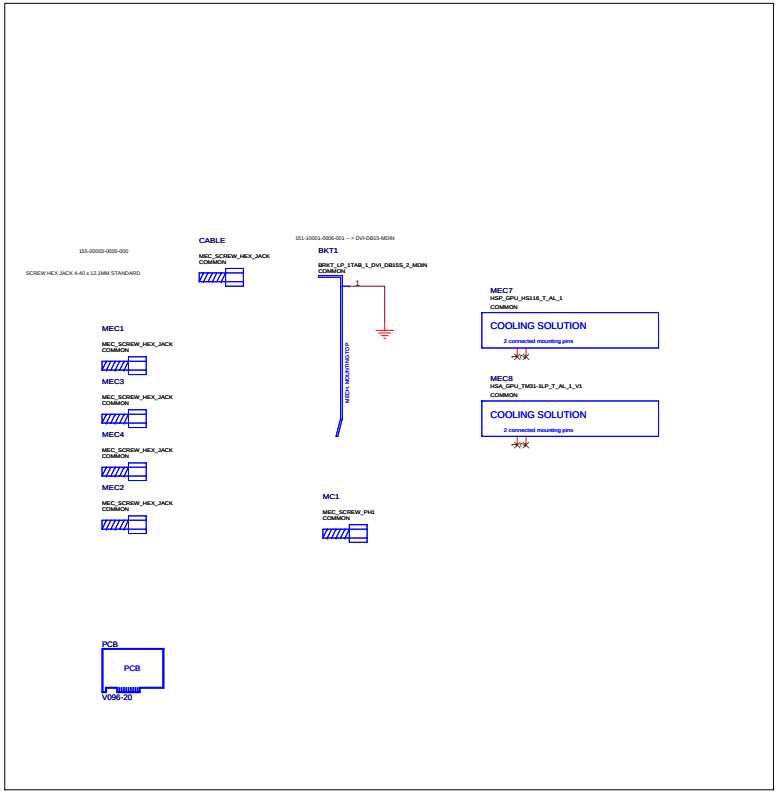
17: PEX_PLL_EN_TERM100		0 (default – internal term on)
18: 3GIO_PADCFG_LUT_ADR[0]		0000=Desktop 0001=Mobile 0010=Mobile NTHRS LLAMP 0011=Mobile NTHRS LAMP 0100=Mobile NTHRS HAMP 0101=Mobile NTHRS HHAMP 0110=Mobile NTHRS LHHAMP 0111=Mobile NTHRS HHHAMP 1000=Desktop HTHRS 1001=Mobile HTHRS NAMP 1010=Mobile HTHRS LLAMP 1011=Mobile HTHRS LAMP 1100=Mobile HTHRS HAMP 1101=Mobile HTHRS HHAMP 1110=Mobile HTHRS HHHAMP 1111=Mobile HTHRS HHHHAMP
19: 3GIO_PADCFG_LUT_ADR[1]		
20: 3GIO_PADCFG_LUT_ADR[2]		
21: 3GIO_PADCFG_LUT_ADR[3]		

31: StrapOverride per SW

REG: NV_STRAP_1

Bit	Signal	VALUE_ID	VALUEs
15: Slot Clock Configuration			0=Disable 1=Enable
12: MIO_EN_33V_0		MIOA_VDDQ Voltage	0=2.5V 1=3.3V
13: MIO_EN_33V_1		MIOB_VDDQ Voltage	0=2.5V 1=3.3V
16: PCI_IOBAR			0=Disable 1=Enable

Mechanical parts



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PAGE DETAIL	BIOS STRAPS & MECHANICALS

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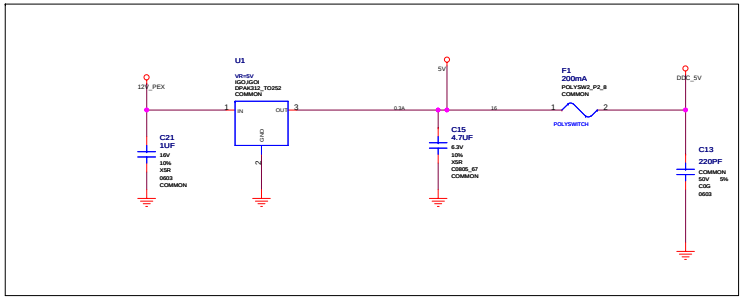
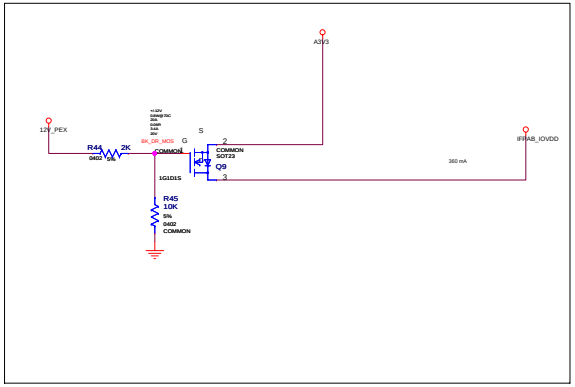
Power SupplyI:TMDS_IOVDD A3V3 DDC_5V IFP_PLLVDD FBVDDQ

DDC 5V

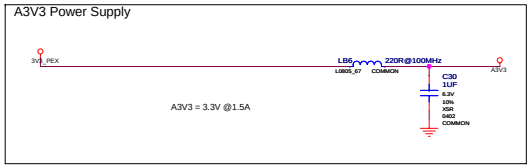


TMDS IO SUPPLY WITH BACKDRIVE PROTECTION

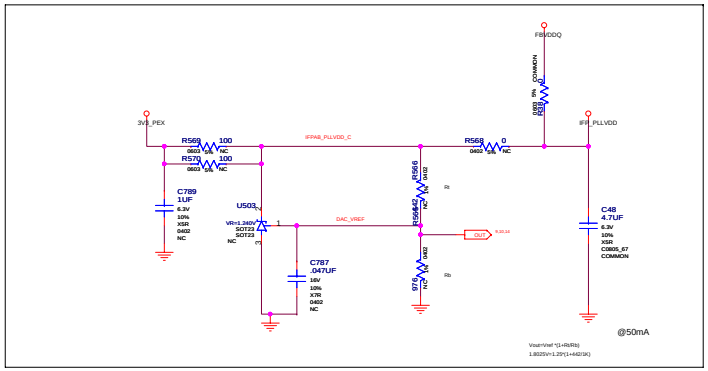


NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	0.1A	12.0	5.00000V
A3V3	1.5A	30.0	3.30000V
IFPAB_IOVDD	0.3A	16	3.30000V
GND		35.0	0.000000V
IFP_PLLVDD	0.3A	16	1.80000V

A3V3 Power Supply

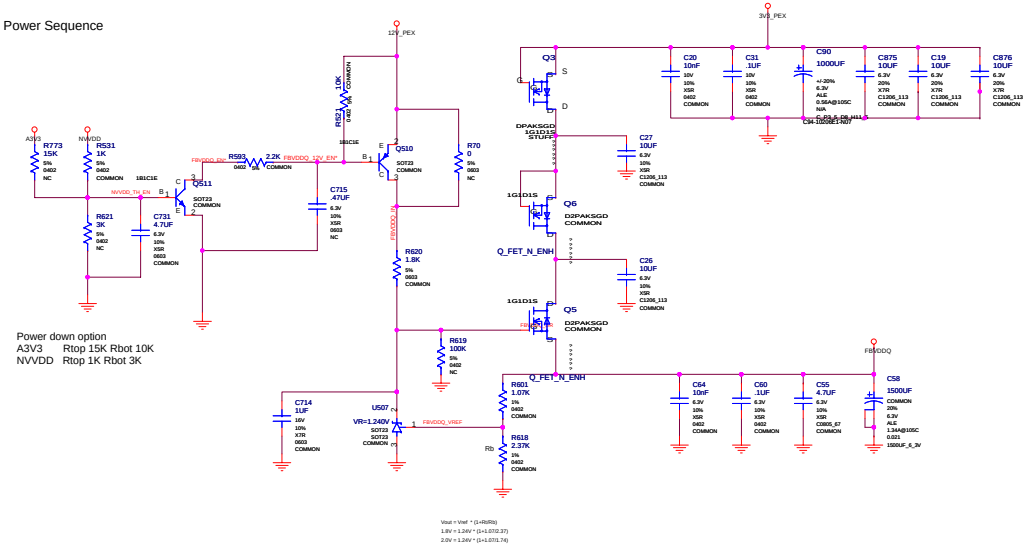


IFP_PLL SUPPLY



FBVDDQ

Power Sequence



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: TMDS IOVDD,5V,A3V3

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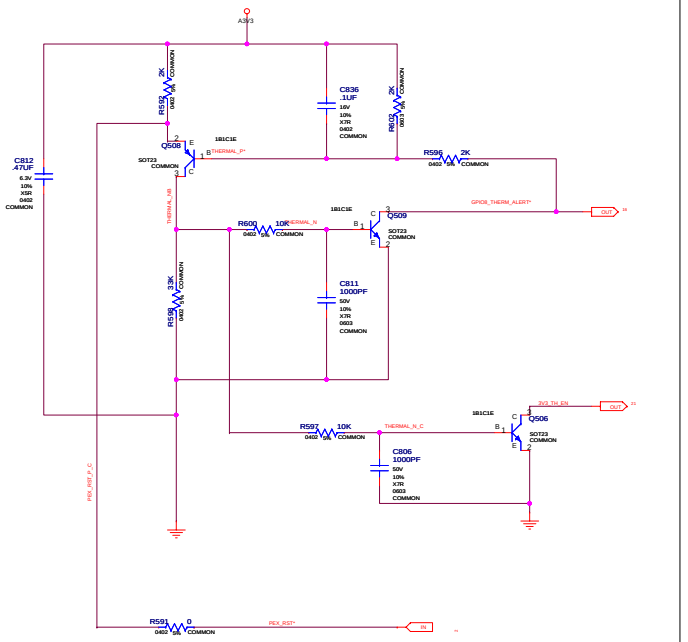
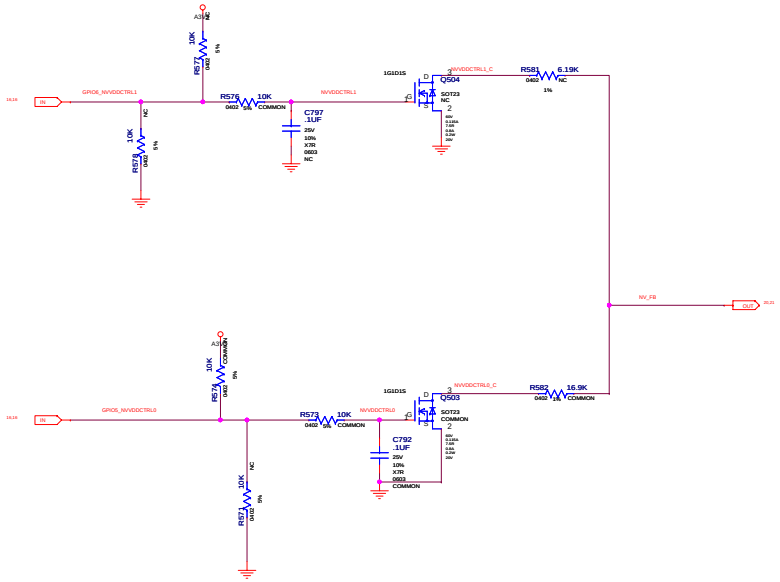
thermal protection and dynamic NVVDD



Thermal protection



dynamic NVVDD

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PAGE DETAIL	thermal protection and dynamic NVVDD

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PowerSupplyII: NVVDD

Net Name	LINE_WIDTH	Current	Voltage
NVVDD	30MIL	15A	1.2V
PEX1V2	24MIL	1.5A	1.20000
NVVDD_SENSE	10MIL	0.5A	1.3V
NVVDD_SENSE_M	10MIL	0.5A	1.2V

L6783A I32-L678303-S10

APW7065 I32-0706502-A30

co-layout

co-layout

25A

Power Sequence

NVVDD

Vout = VRef * (1+Rtop/Rbot)

1.1V = 0.8V * (1+(1.54k/4.02k)) (ISL6549)

1.2V = 0.8V * (1+(1.54k/3.09k)) (ISL6549)

1.2V = 0.8V * (1+(10k/20k)) (APW7065)

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PowerSupplyII: NVVDD

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