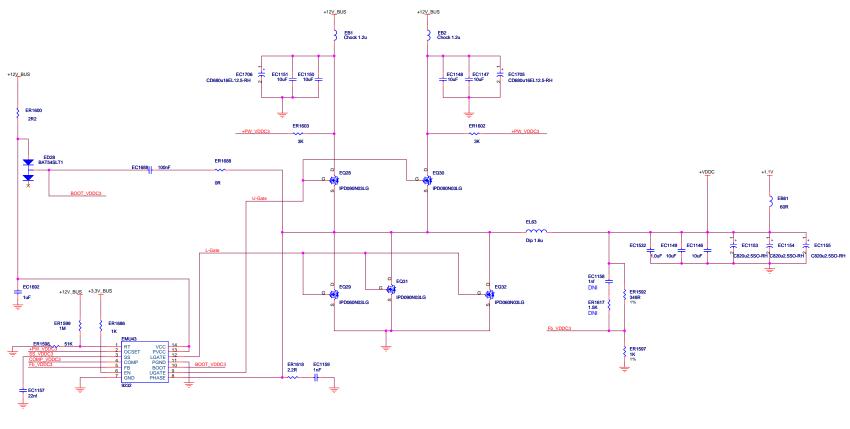
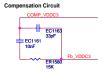


(12) VDDC

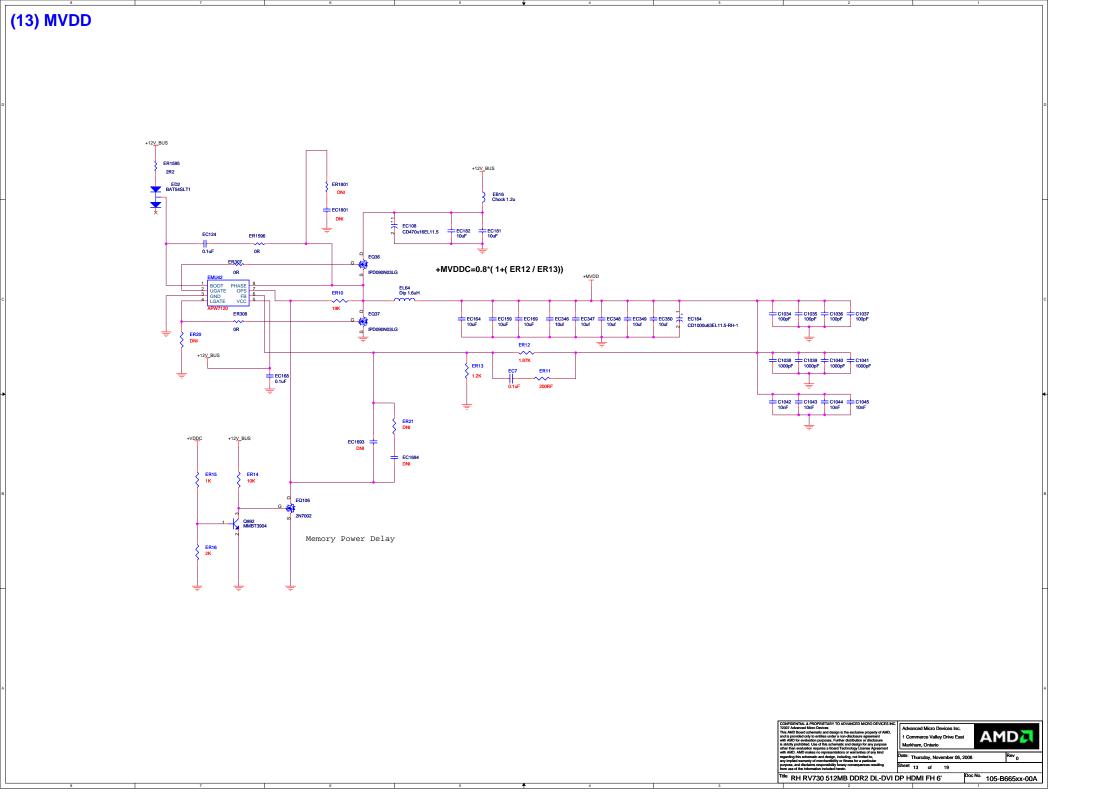
## CORE REGULATOR VDDC



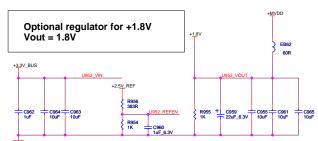
+VDDC=0.8\*( 1+( ER1592 / ER1597 ))

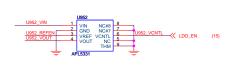


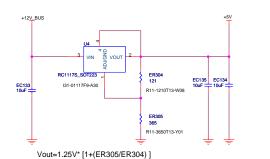




## (14) Linear Regulators Optional regulator for +1.1V Vout = 1.1V AAA01906-178\_0703-3-881 Optional regulator for +1.1V Vout = 1.1V AAA01906-178\_0703-3-881 Optional regulator for +1.1V Optional regulat







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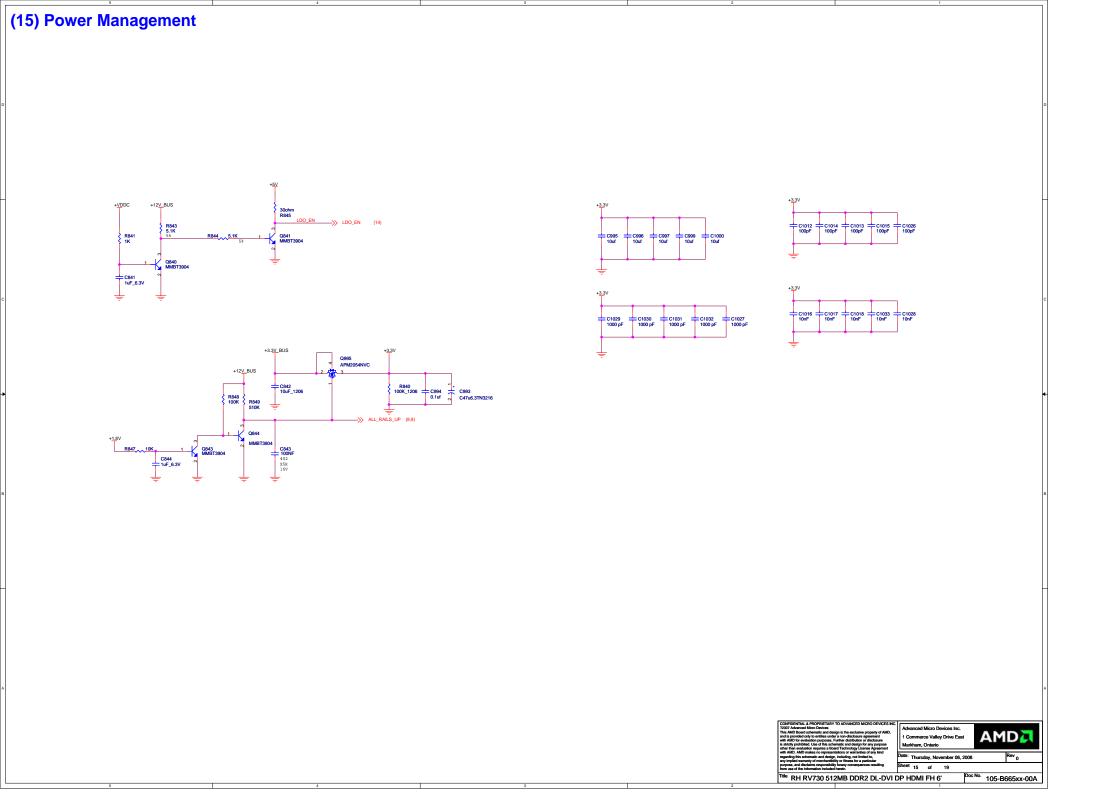
to a sindry profits. Use of this submedia or design for any propose
offer than exclusion regions a found Technology Lorent Agreement

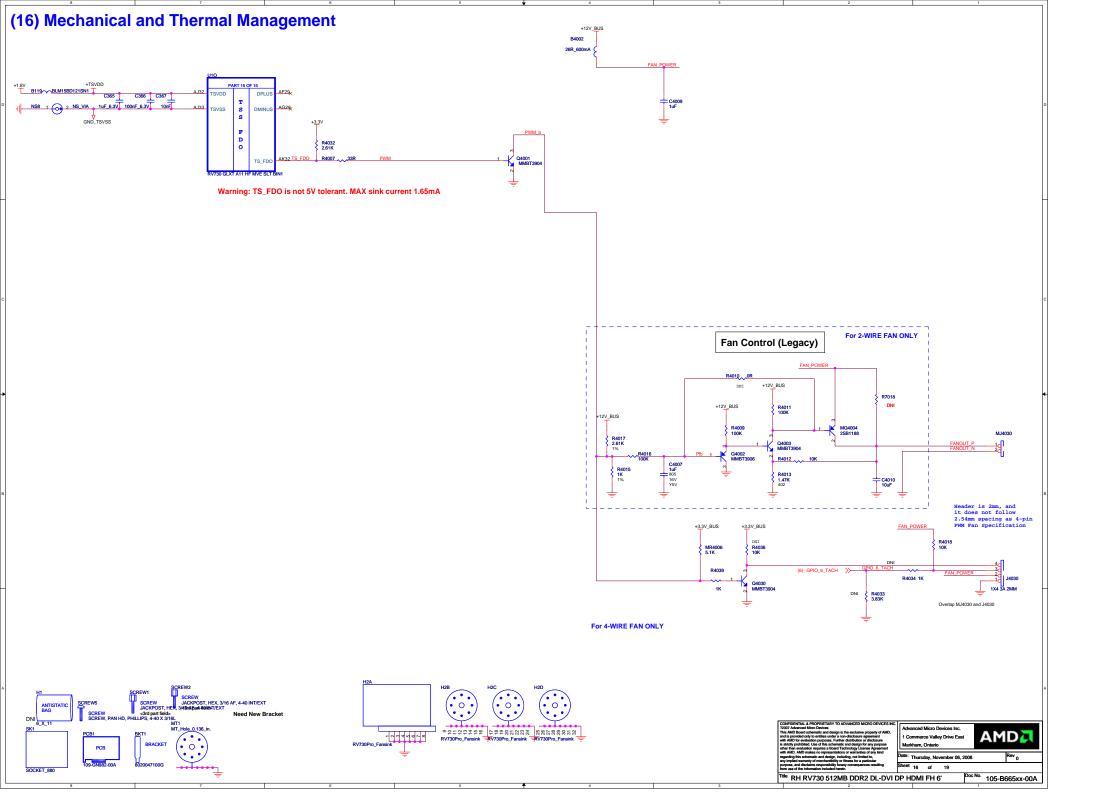
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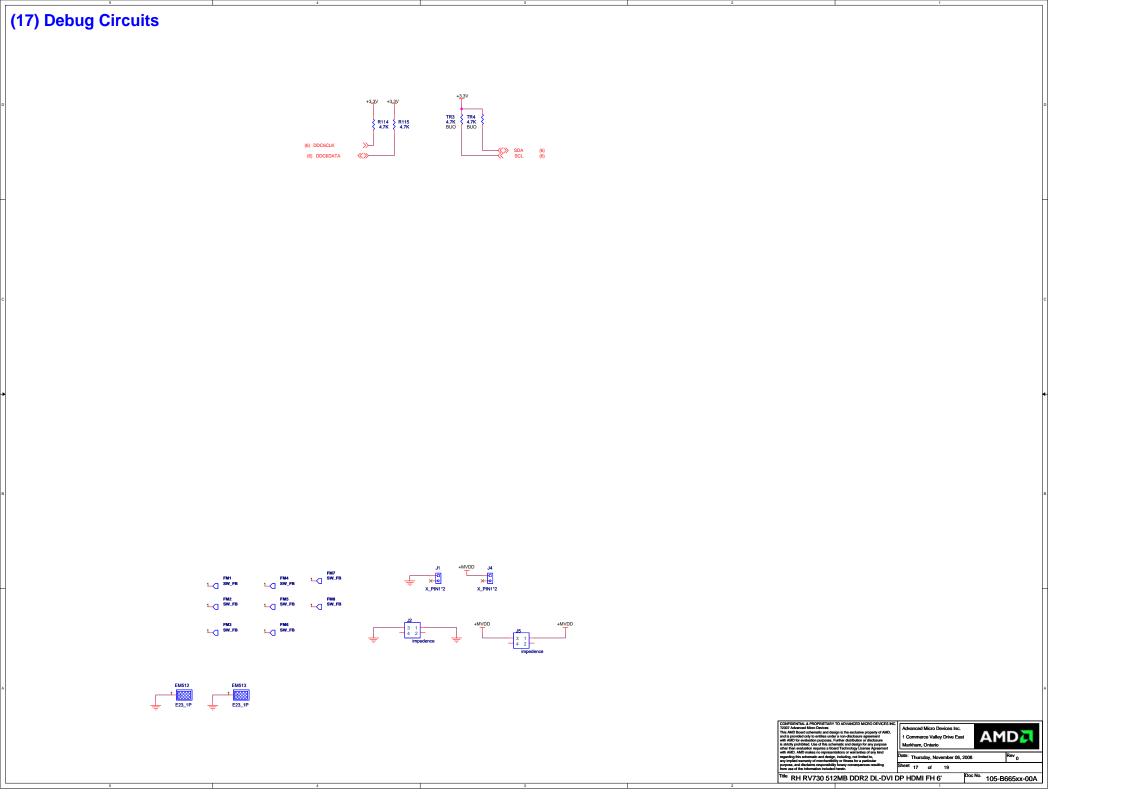
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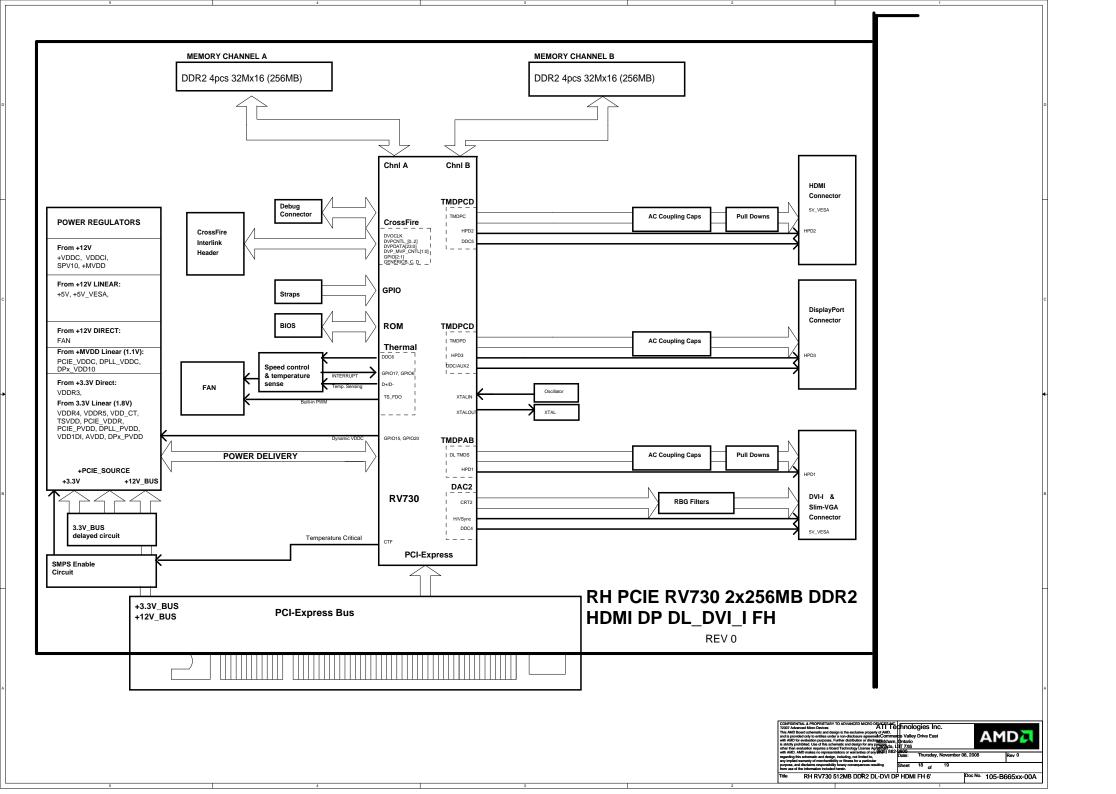
Date: Thursday, November 06, 2006 Rev 0

**AMD** 









	Δ	MC	5	Title RH RV730 512MB DDR2 DL-DVI DP HDM	II FH 6'	3	Schematic No. 105-B665xx-00A	Date: Thursday, Nove	mber 06, 2008
				REVISION HISTORY	NOTE:	This schematic represent For Stuffing options (com Please contact AMD repre	is the PCB, it does not represent any specific aponent values, DNI , ? please consult the esentative to obtain latest BOM closest to th	SKU. croduct specific BOM. e application desired.	Rev 0
	Sch Rev	PCB Rev	Date	REVISION DESCRIPTION					
	0	00A	08/04/01	Initial design for RV730 GDDR3					
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