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Page 18: POWER SUPPLY: TMDS IOVDD, 5V, A3V3  
Page 19: PowerSupplyI: NVVDD, A2V5  
Page 20: PowerSupplyII: FBVDDQ, PLLVDD

REV  
HISTORY

Base on P501\_A01 modify

- 4/13/2006:

1.PAGE:12 :INTERNAL TMDS LINK C/D  
Add DVI circuit  
2.PAGE:19/20 :Power modify 6549 circuit  
pin to pin RT9259/9259A  
3.PAGE:11/12 :TMDS Link  
Add EMI solution

- 4/14/2006:

1.PAGE:12 :INTERNAL TMDS LINK C/D  
Add DVI dual link circuit  
2.PAGE:19/20 :Power modify 6549 circuit  
reserve C840/C841 High side gate to phase

- 4/17/2006:

1.PAGE:19/20 :Power modify 6549 circuit  
Change 6549 Footprint SSOP16 to SOP14  
2.Change IC,L footprint to MSI Data Base

- 4/20/2006:

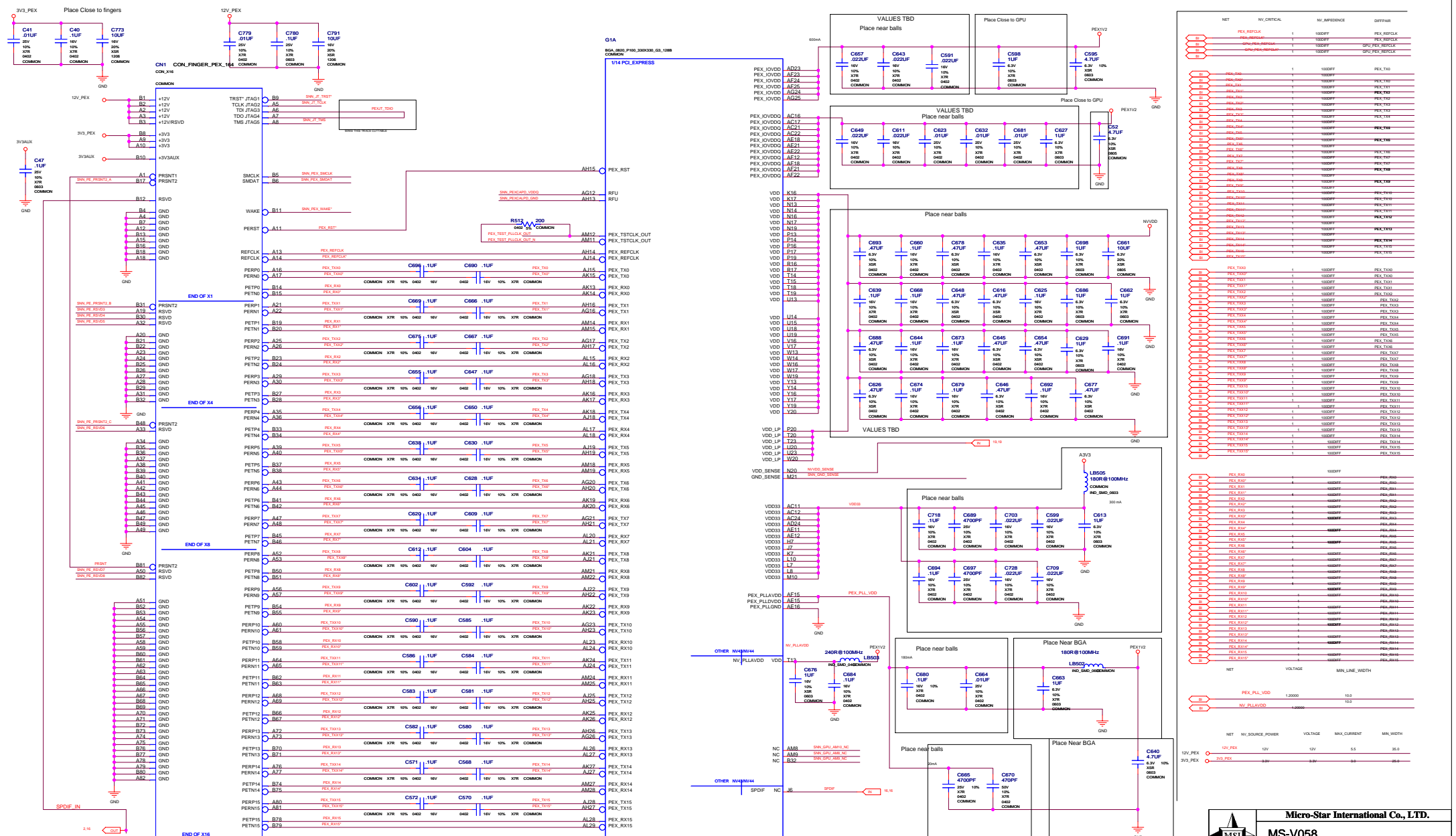
1.PAGE:18 :  
Add FM1-FM6 for ME  
Add C884-C850 for EMC suggestion reserve  
2.PAGE:19 :Remove D9/R18 SC2621A Only

- 5/24/2006:

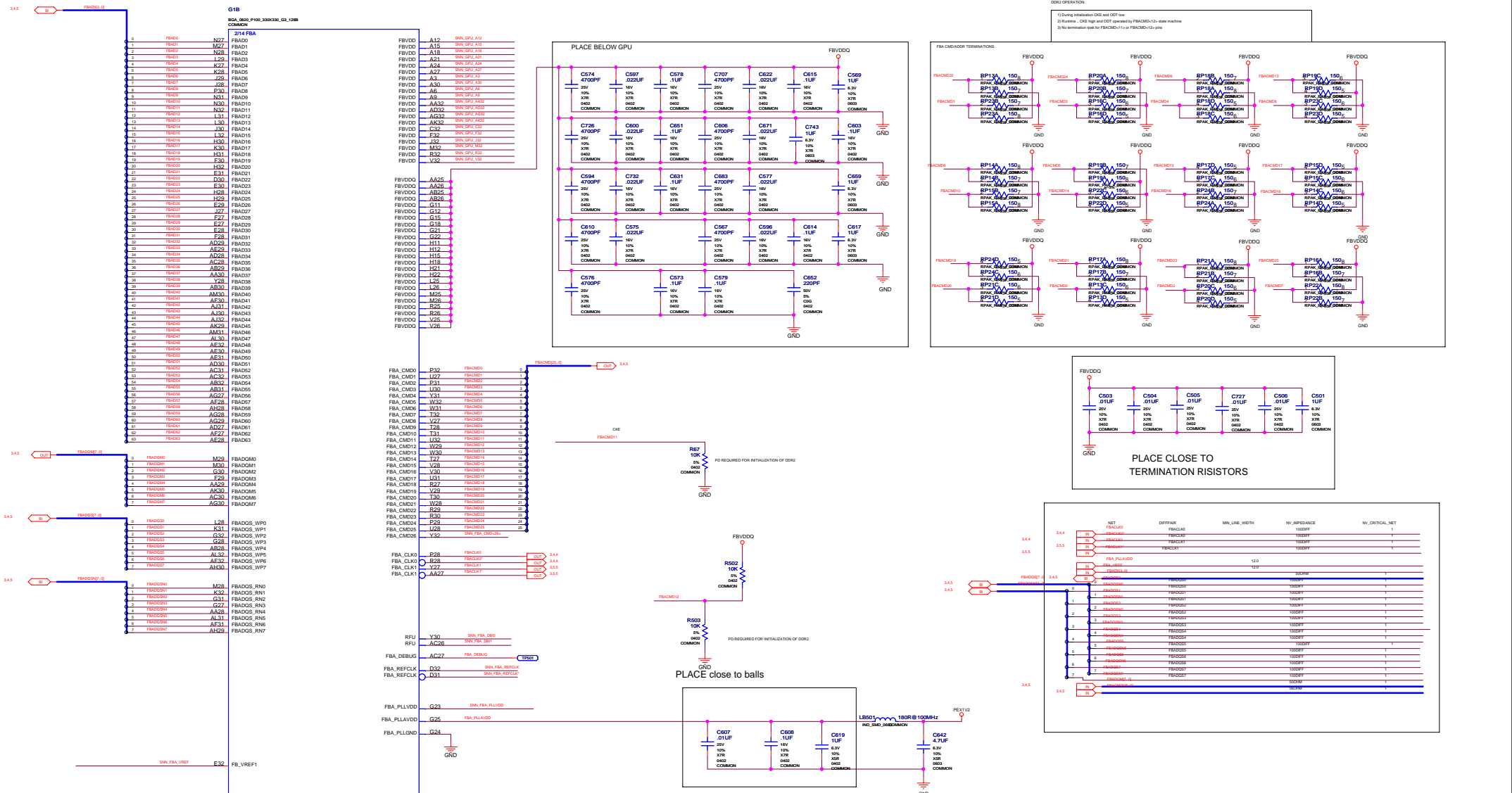
1.PAGE:12 :  
Revise TMDS A2V5 power for Link C/D  
2.PAGE:20 :  
Add R640/R641 NVVDD conect to PEX1V2  
Change C13 SMD to DIP footprint  
3.PAGE:12/13 :  
Remove DVI EMI commom choke

REV	VARIANT	NPIN	ASSEMBLY
B	0000	600-10501-0000-100	G73 400/350MHz 256MB 128bit DDR2 16MX16 DVI-I+VGA+HDTVOUT
1	0001	600-10501-0001-100	G73-V 375/350MHz 256MB 128bit DDR2 16MX16 DVI-I+VGA+HDTVOUT
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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## 16X PCIe Interface

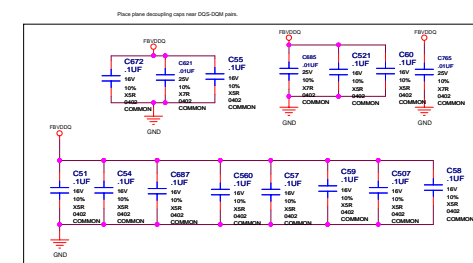
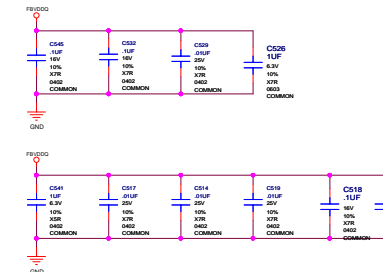
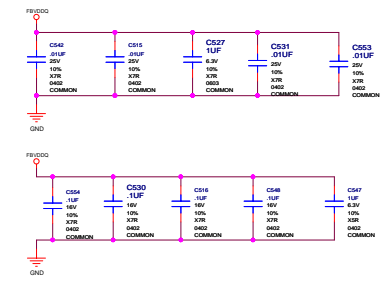
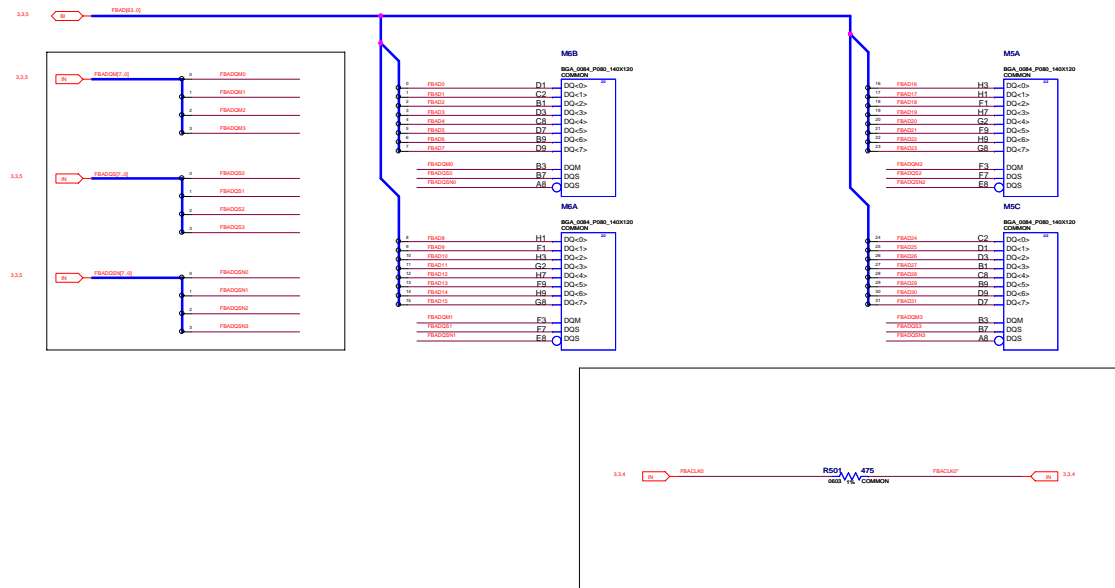
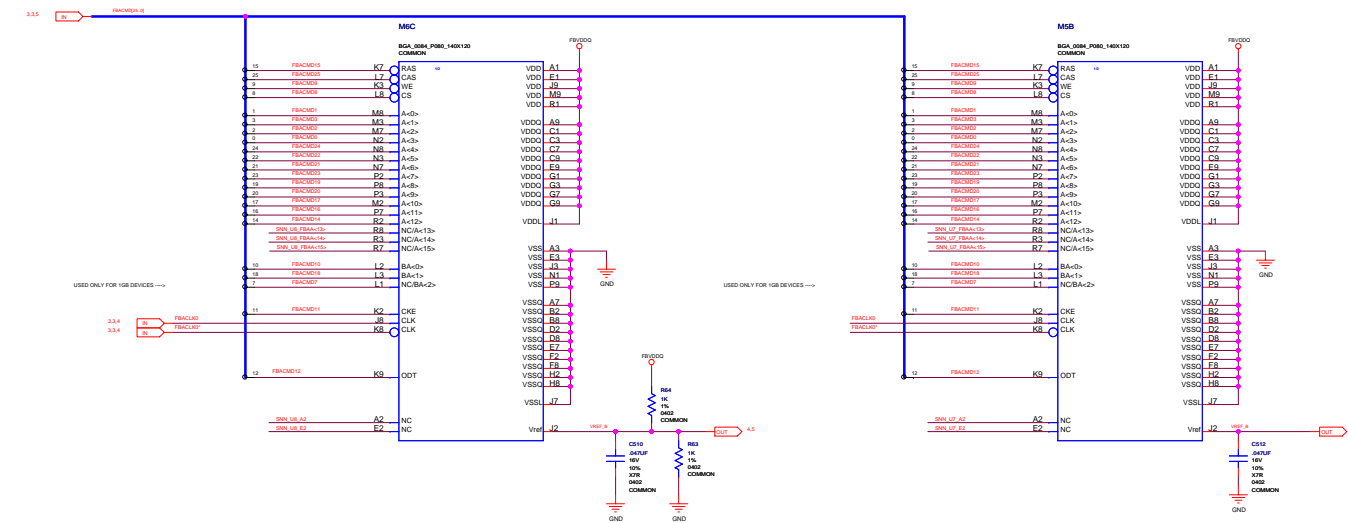


## GPU: FB-Interface A



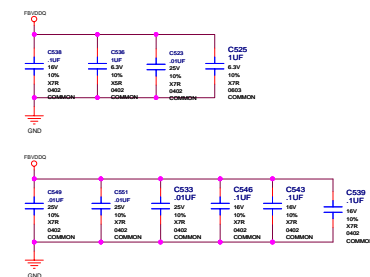
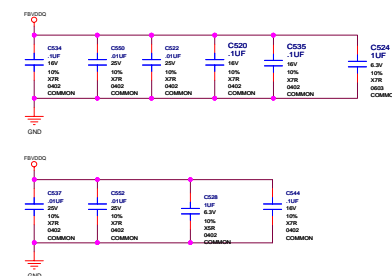
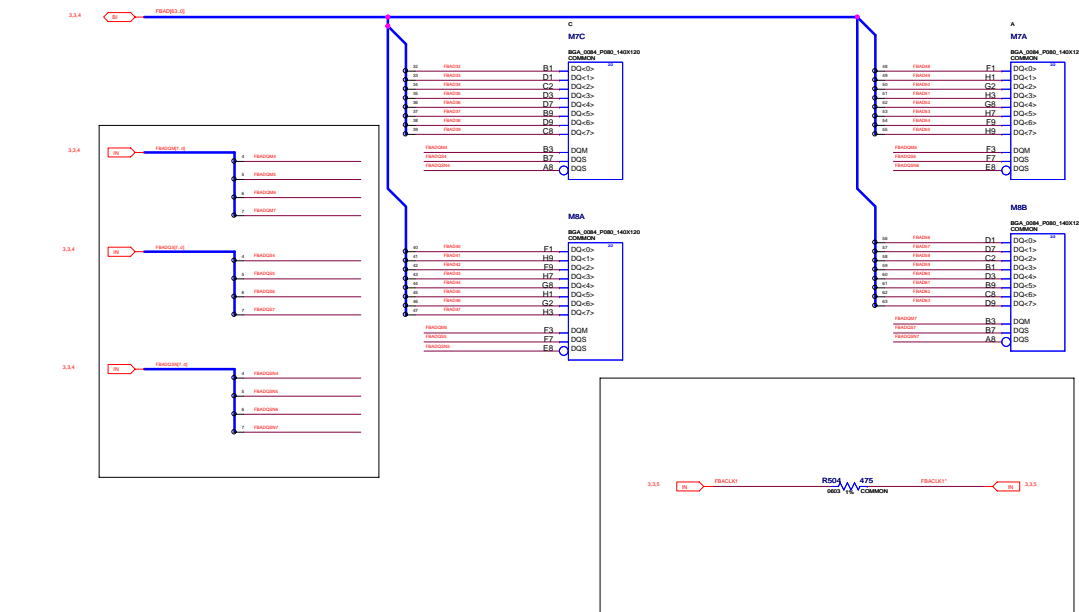
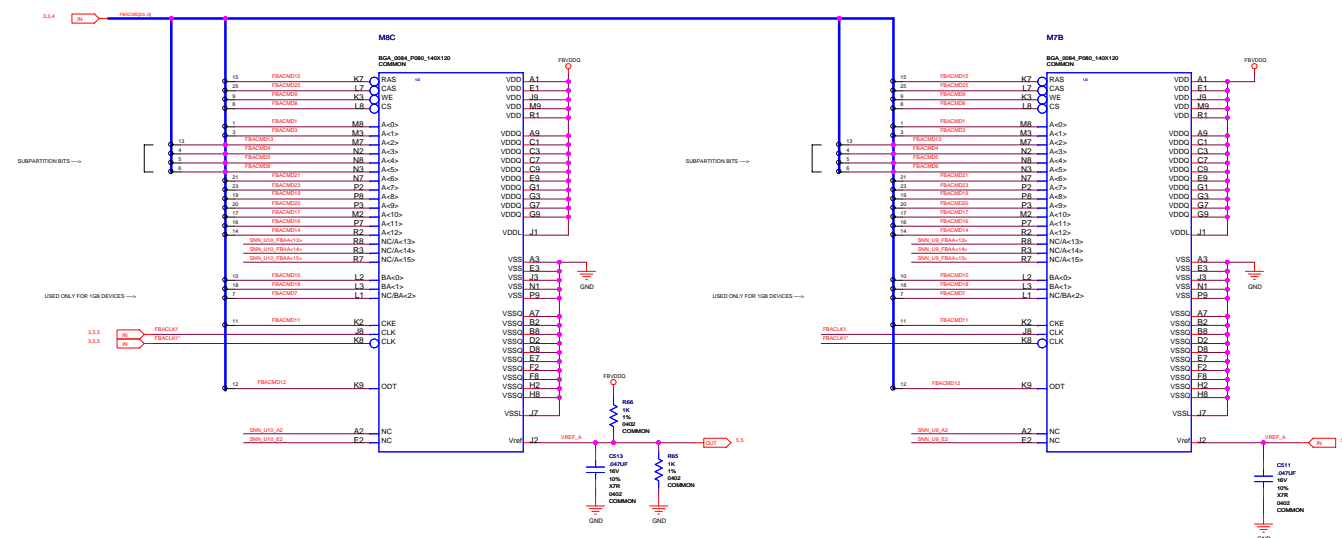
## FBA MEMORY 1st bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

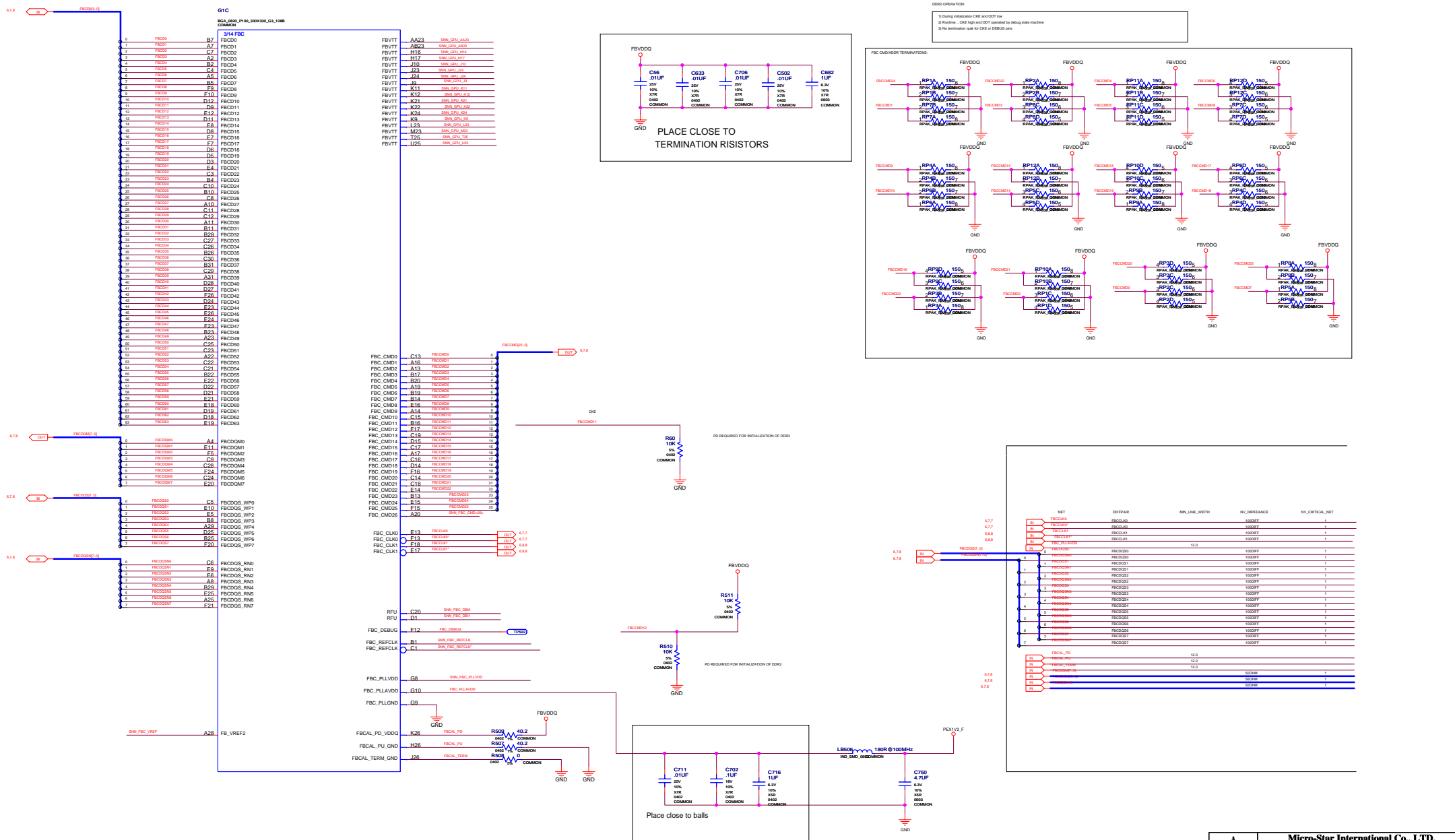


## FBA MEMORY 1st bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

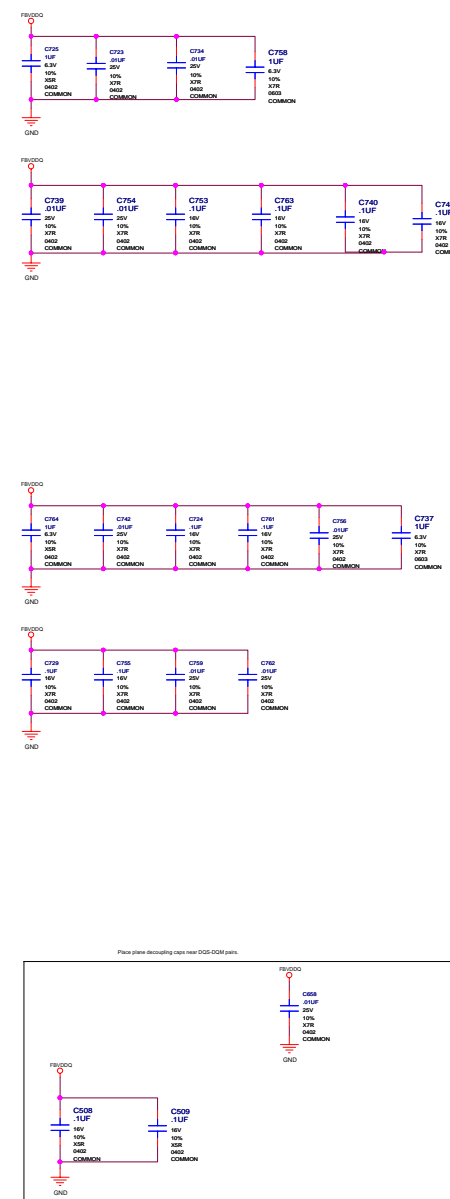
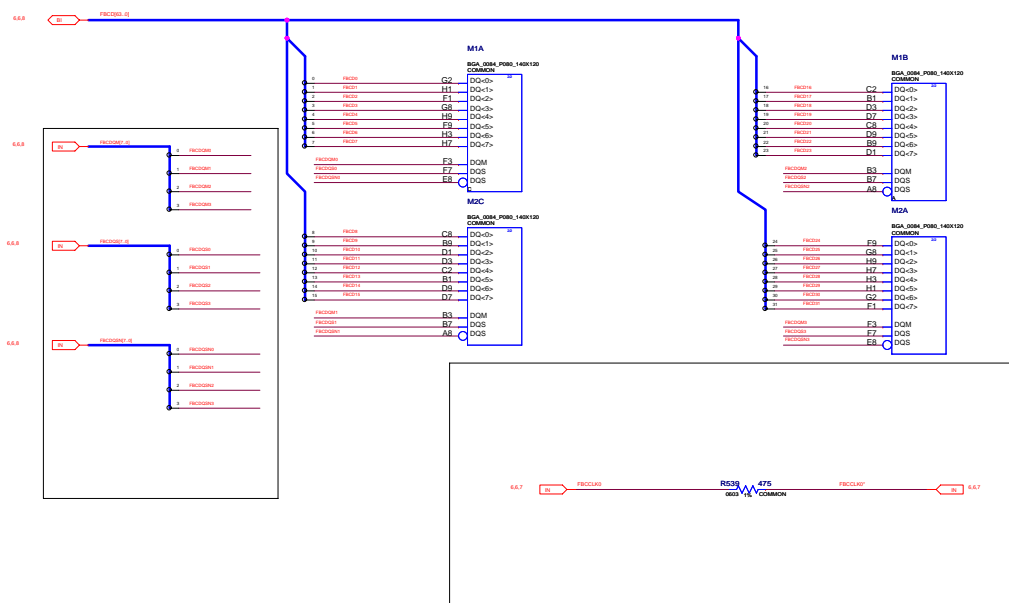
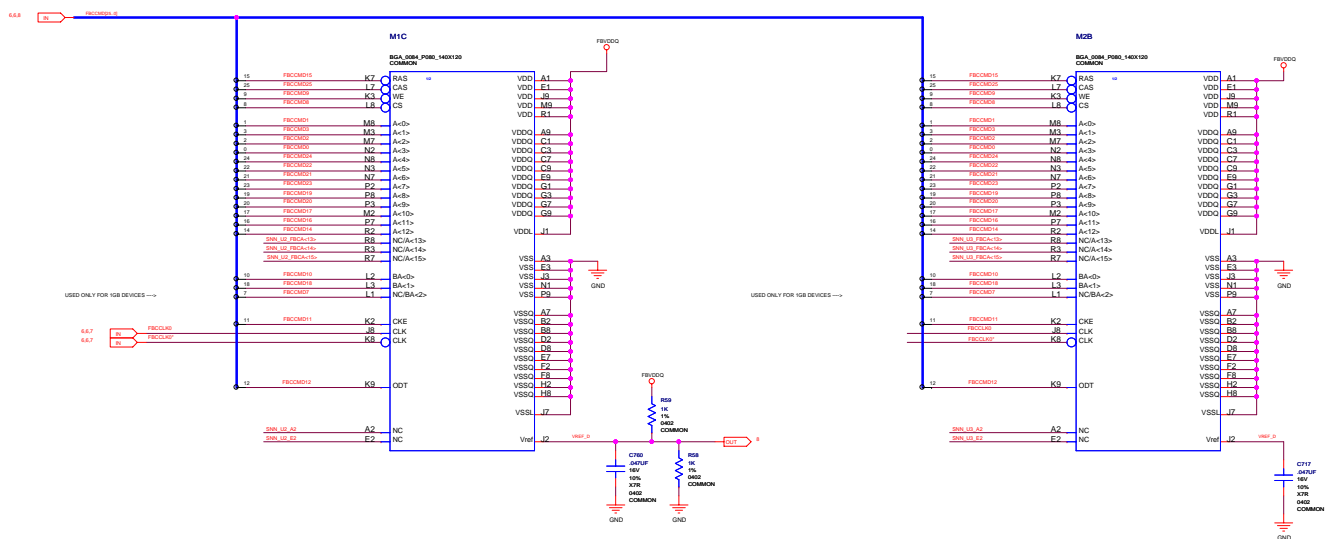


## GPU: FB-Interface C



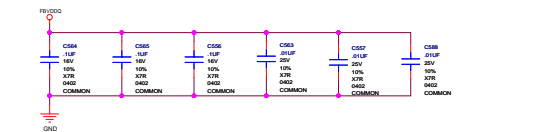
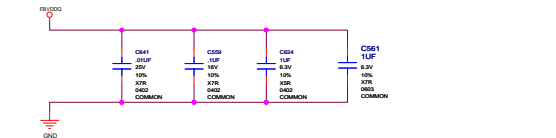
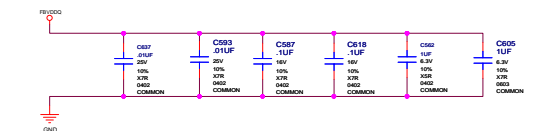
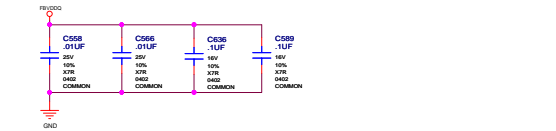
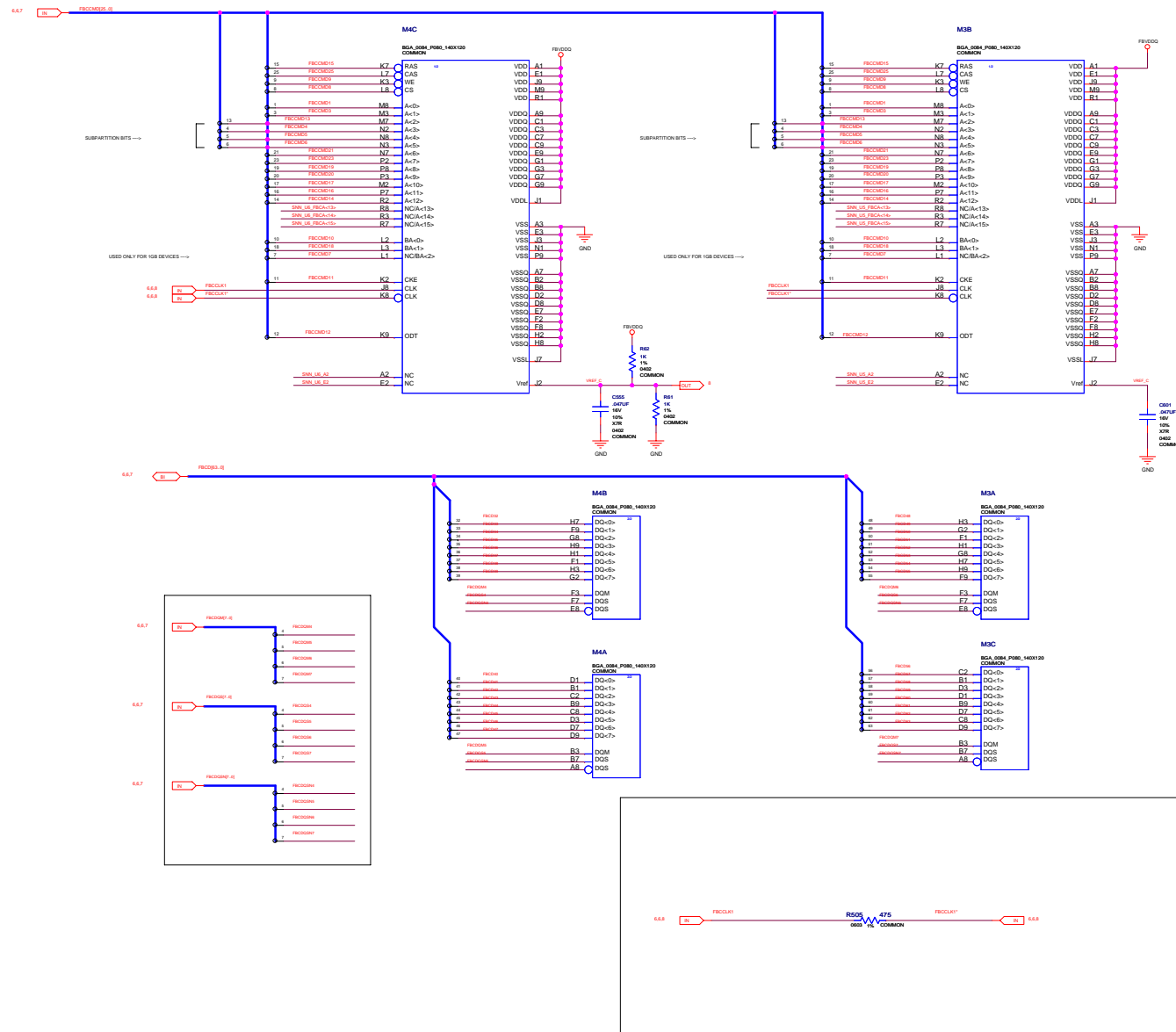
# FBC MEMORY 2nd bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



## FBC MEMORY 2nd bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



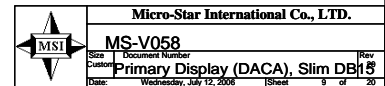
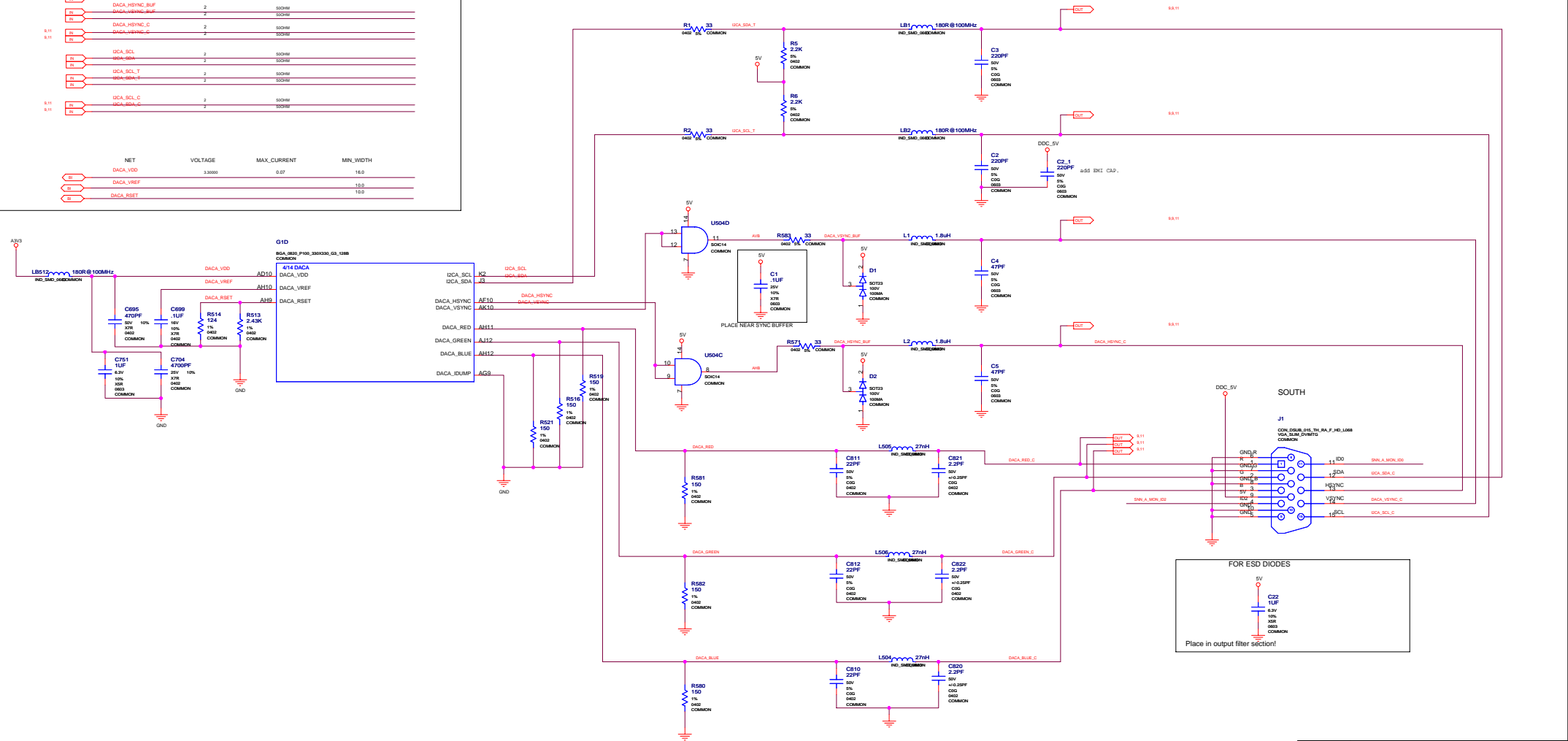


## Primary Display (DACA), Slim DB15

## DACA NET RULES

		NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
0.0		DACA_VDD	3.300000	0.07	16.0
0.0		DACA_VREF			10.0
0.0		DACA_RESET			10.0

## DACA RGB-FILTER



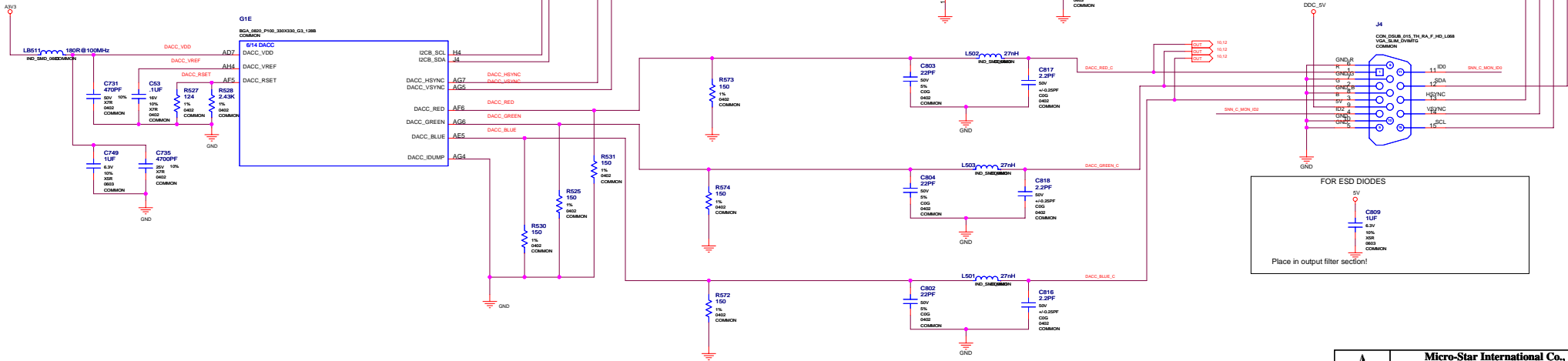
Secondary Display (DACC), DB15

DACC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACC_RED	1	50OHM	
DACC_GREEN	1	50OHM	
DACC_BLUE	1	50OHM	
DACC_RED_C	1	50OHM	
DACC_GREEN_C	1	50OHM	
DACC_BLUE_C	1	50OHM	
DACC_HSYNC	2	50OHM	
DACC_VSYNC	2	50OHM	
CVB	2	50OHM	
FSB	2	50OHM	
DACC_HSYNC_BUF	2	50OHM	
DACC_HSYNC_C	2	50OHM	
DACC_VSYNC_C	2	50OHM	
DCB_SCL	2	50OHM	
DCB_SDA	2	50OHM	
DCB_SCL_T	2	50OHM	
DCB_SDA_T	2	50OHM	
DCB_SCL_C	2	50OHM	
DCB_SDA_C	2	50OHM	
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACC_VDD	3.30000	0.14	16.0
DACC_VREF			10.0
DACC_RSET			10.0

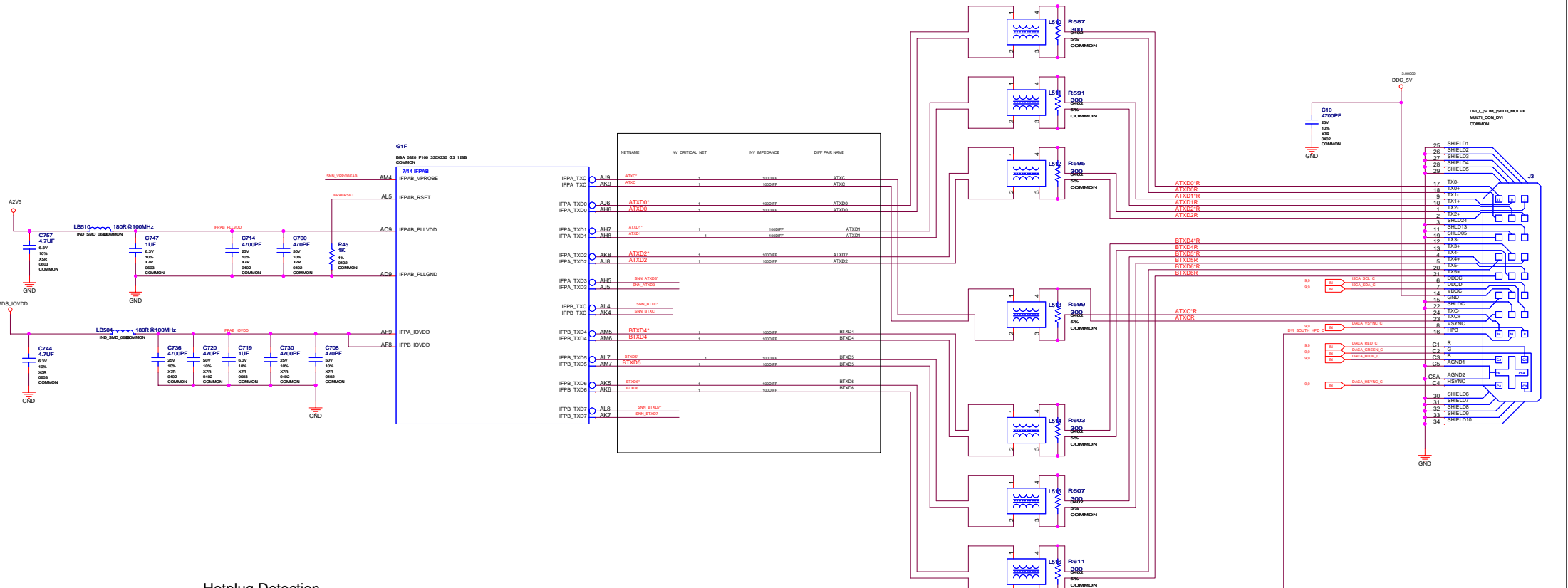
I2C B for HDMI.

DACC RGB-FILTER

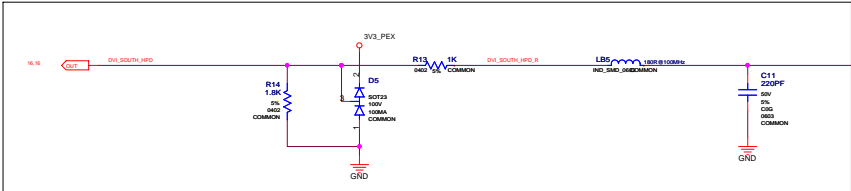


INTERNAL TMDS .. LINK A & B

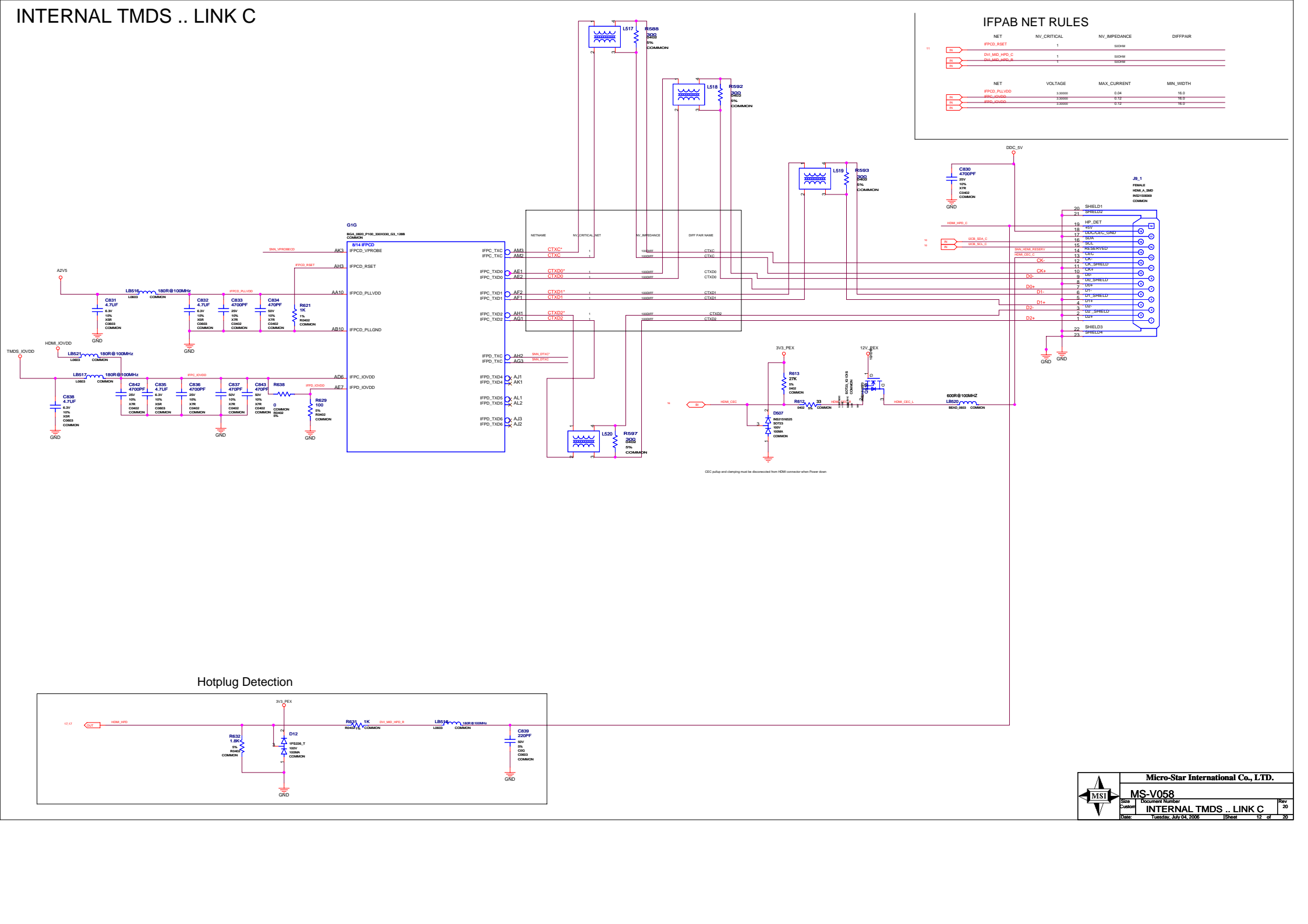
IFPAB NET RULES			
NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLLVDD	3.3000V	0.04	16.0
IFPAB_IOVDD	3.3000V	0.24	16.0
IFPABRESET			12.0
DIV_SOUTH_HPD_C	1	500M	
DIV_SOUTH_HPD_R	1	500M	



Hotplug Detection

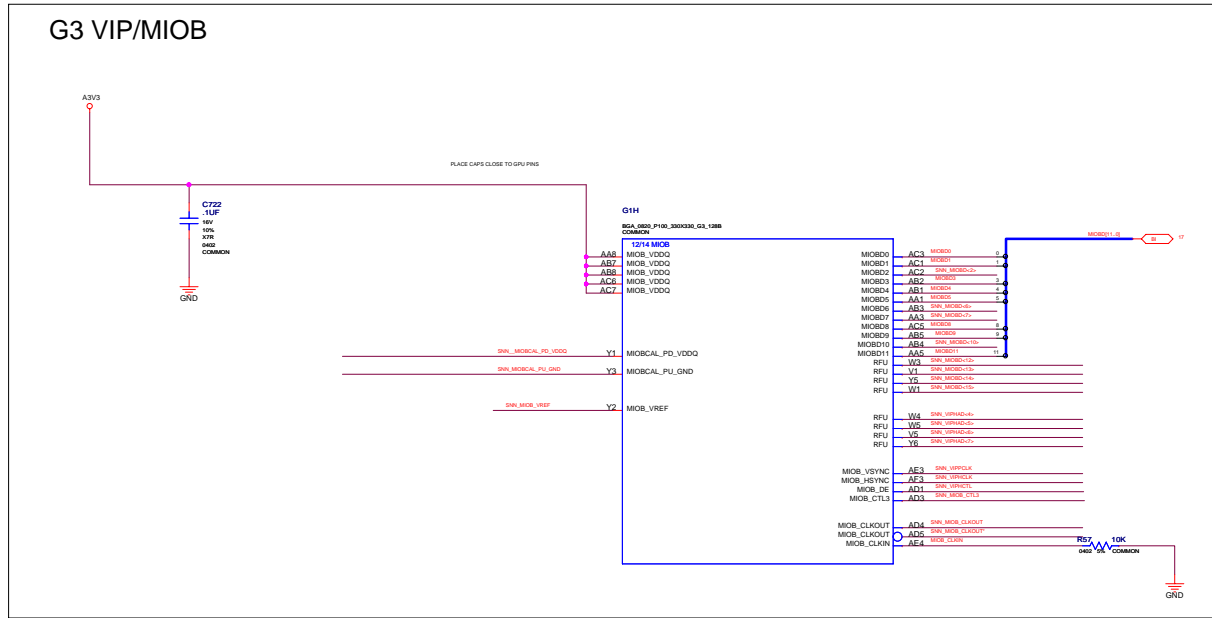


INTERNAL TMDS .. LINK C

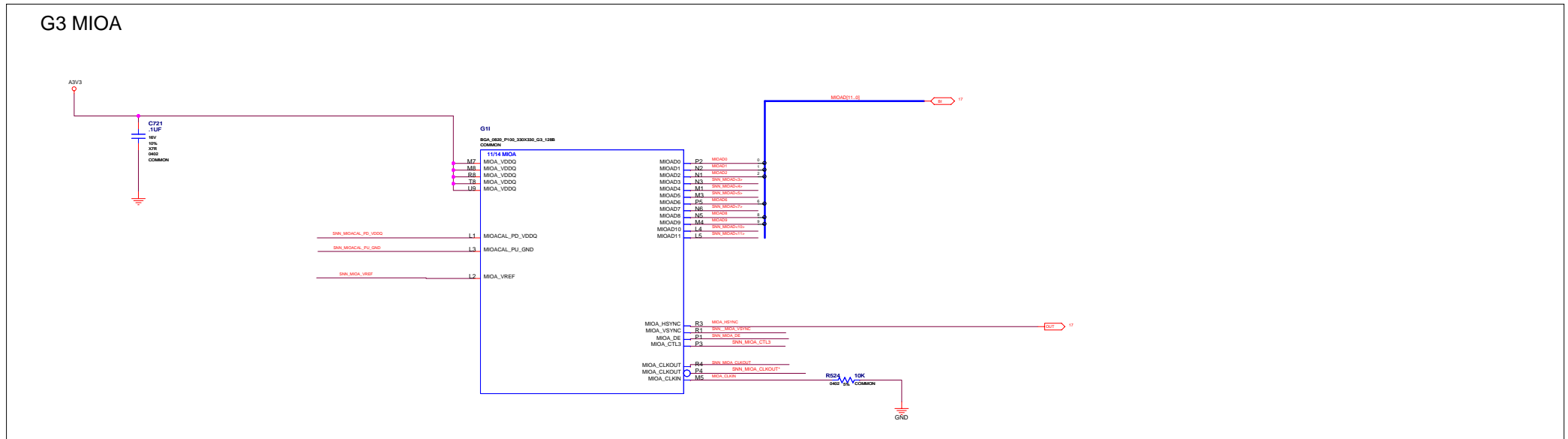


## G3 VIP/MIOB/MIOA

## G3 VIP/MIOB



## G3 MIOA



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Document Number  
**G3 VIP/MIOB/MIOA**

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## DACB .. MiniDIN VIDEO OUT CONNECTOR

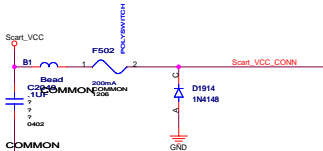
## DACB .. MiniDIN VIDEO OUT CONNECTOR

## DACB NET RULES

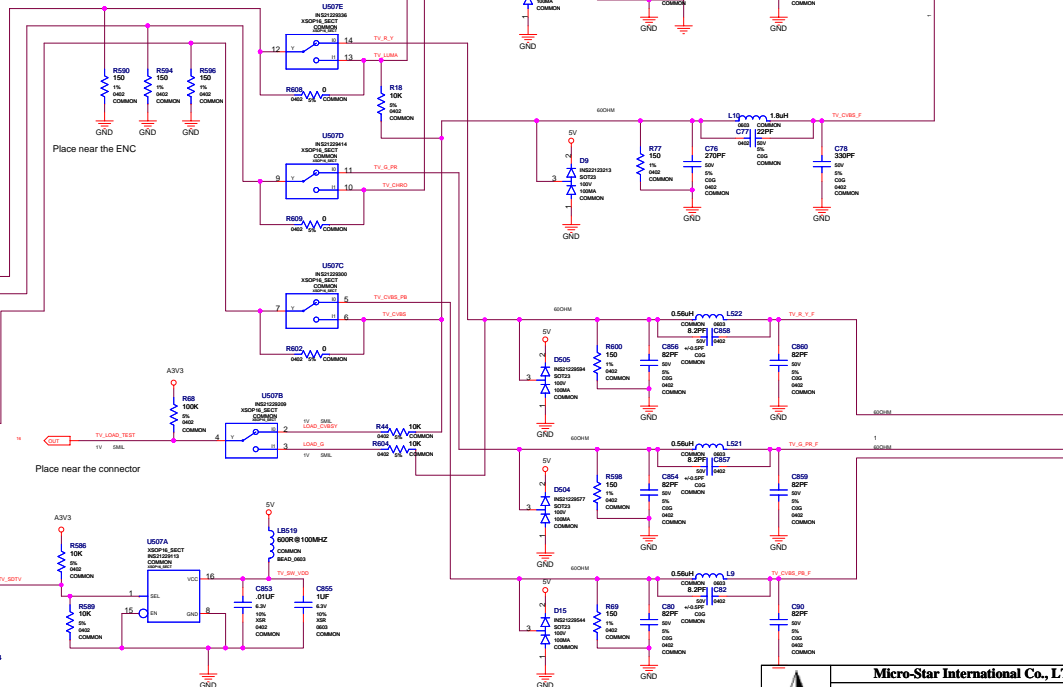
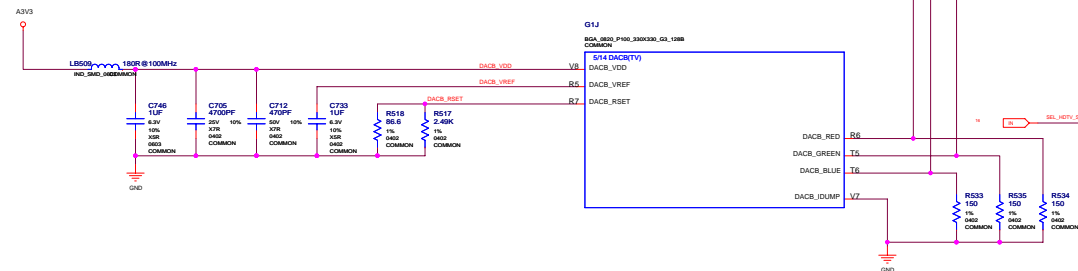
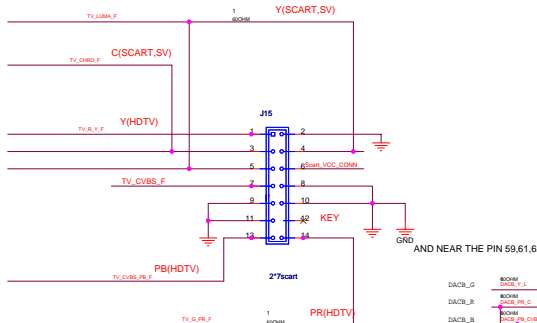
	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	DACB_C_OUT	1	SEGM	
IN	MDIN_COUT_C	1	SEGM	
IN	DACB_CHISE_OUT	1	SEGM	
IN	MDIN_YOUT_C	1	SEGM	
IN	DACB_RR_OUT	1	SEGM	
IN	MDIN_PROUT_C	1	SEGM	

Signal	Pin	Value	Unit
MDIN_SCL_C	2	500HM	
MDIN_SDA_C	2	500HM	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
	DACB_VDD	3.30000	0.07	16.0
IN	DACB_VREF			16.0
IN	DACB_RESET			16.0
IN				16.0



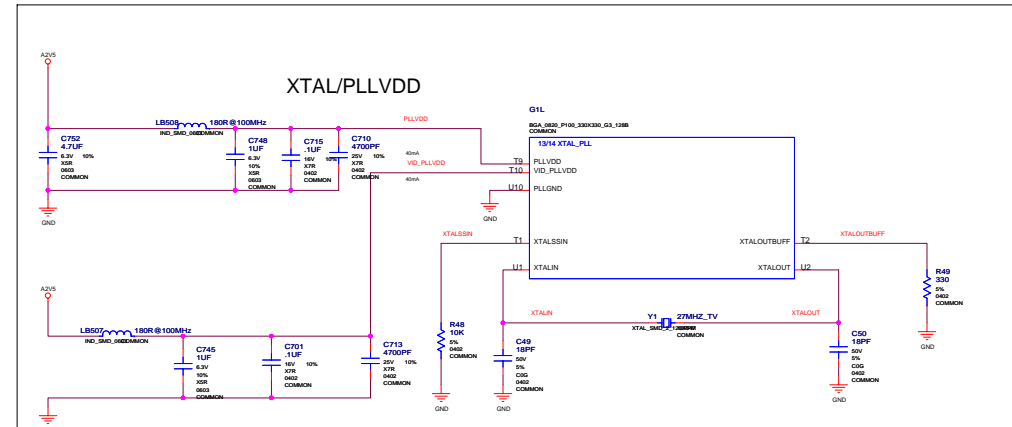
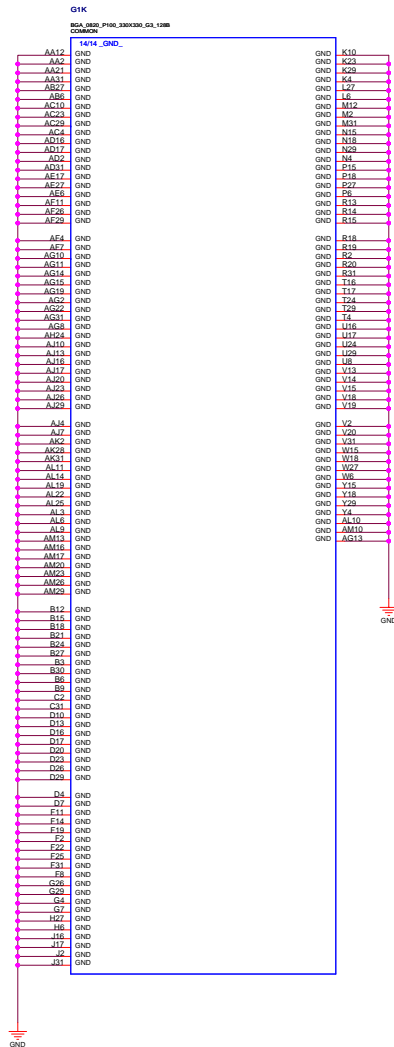
**SCART** Add Scart TV connector



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MS-V058	
Size Custom	Document Number DACB .. MiniDIN VIDEO OUT

GND/XTAL/PLLVDD

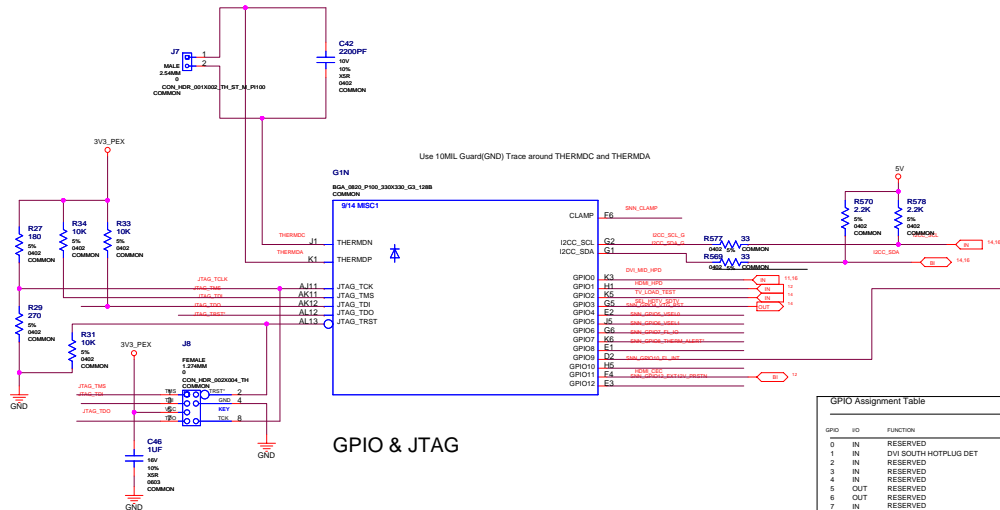


	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
25	XTALIN	L	SOIM	
26	XTALOUT	L	SOIM	

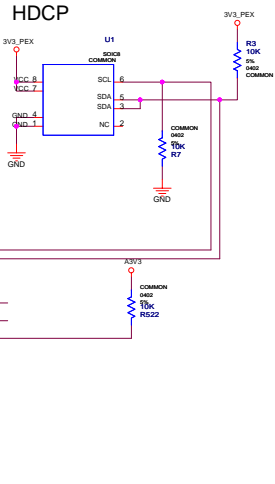
  

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
25	PXA_VDD	2.0V	0.3	18ML
26	VDD_PIO_VDD	2.0V	0.3	12.0

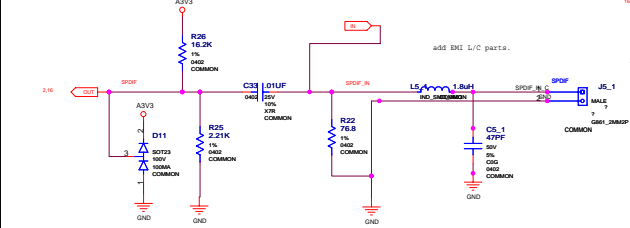
## GPIO / JTAG / HDCP / BIOS / SPDIF



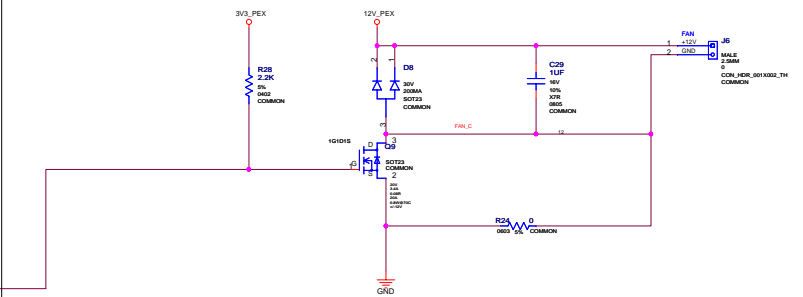
## HDCP



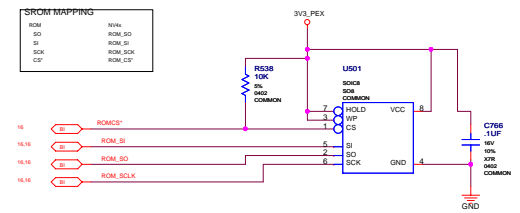
## SPDIF



## GPIO ON/OFF FAN Control



BIOS (serial)



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## MISC NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	OFFPAIR
14,18	WOC, SOL	2	SDRM	
14,18	WOC, SOL	2	SDRM	
14	WOC, SOL, G	2	SDRM	
14	WOC, SOL, G	2	SDRM	
14	WOC, SOL, G	2	SDRM	
14	WOC, SOL, G	2	SDRM	
14	WOC, SOL, G	2	SDRM	
14	WOC, SOL, G	2	SDRM	
14,18	ROM, CE	2	SDRM	
14	ROM, CE	2	SDRM	
14,18	ROM, CE	2	SDRM	
14	ROM, CE	2	SDRM	

11,56 DVL\_SOUTH\_HPO 2 50GHM

[illegible]

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Size	Document Number	Rev
Custom	<b>GPIO / JTAG / HDCP / BIOS / SPDIF</b>	20
Date:	Friday, July 14, 2006	Sheet 16 of 20

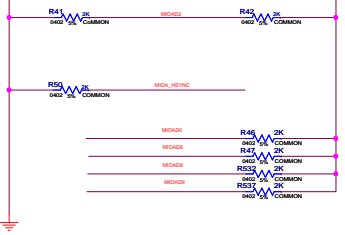
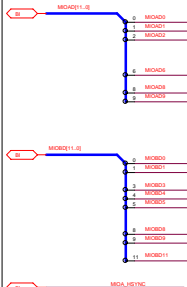
Date:	Friday, July 14, 2006	Sheet	16 of 20
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## STRAPS, Mechanical Parts

## Straps

Assembly: BIOS



REG: NV\_PEXTDEV\_BOOT\_0

[illegible]

NO. LISTED ON	ETHAN LISTED ON	00000 (date)
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17: USER: 1

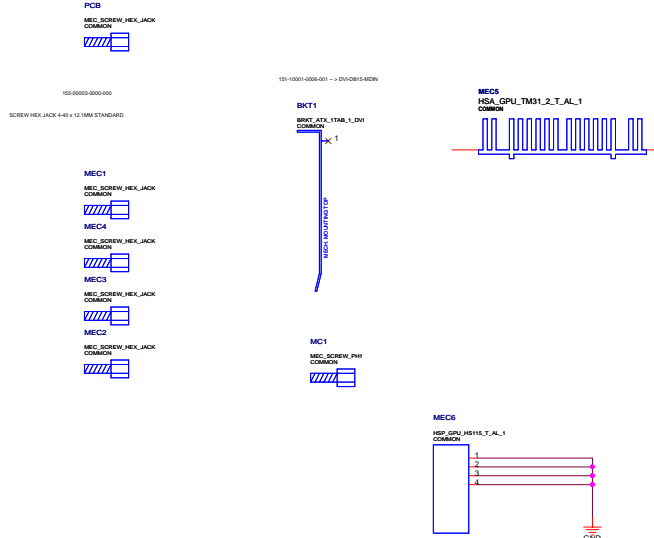
10: USER\_2

11. *Quadrifidus*

28: SLOT\_CLOCK\_CFG

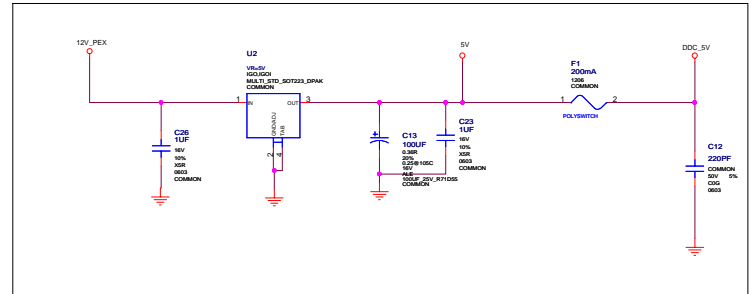
Bit Signal	VALUE_ID	VALUEs
11: PEX_PLL_EN_TSRM100		0 (default – internal trim on)
12: XGIO_PNOCFG_LUT_ADDR[0]		
13: XGIO_PNOCFG_LUT_ADDR[1]		
14: XGIO_PNOCFG_LUT_ADDR[2]		

## Mechanical parts

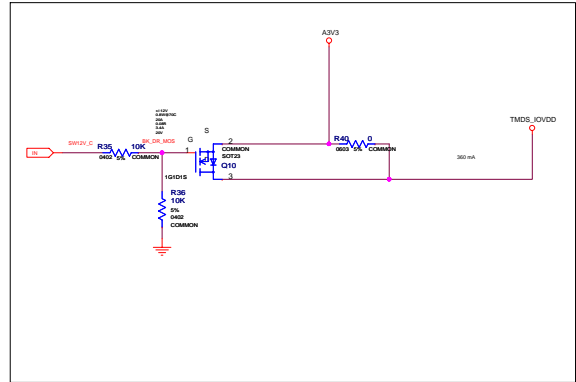


Power Supply:TMDS\_IOVDD/A3V3/5V

DDC 5V



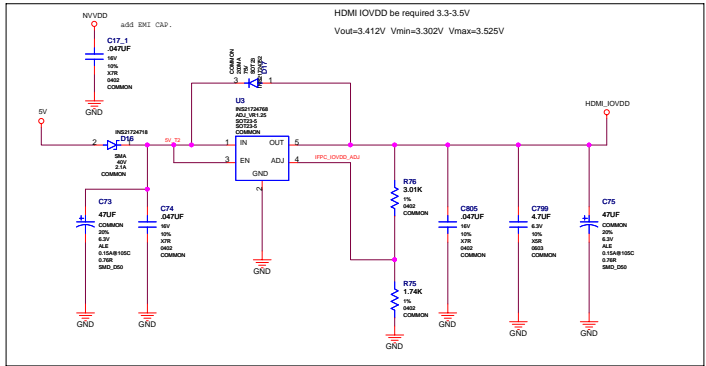
TMDS IO SUPPLY WITH BACKDRIVE PROTECTION



A3V3 Power Supply



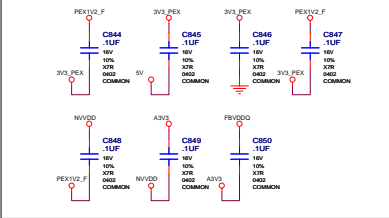
HDMI IO SUPPLY WITH BACKDRIVE PROTECTION



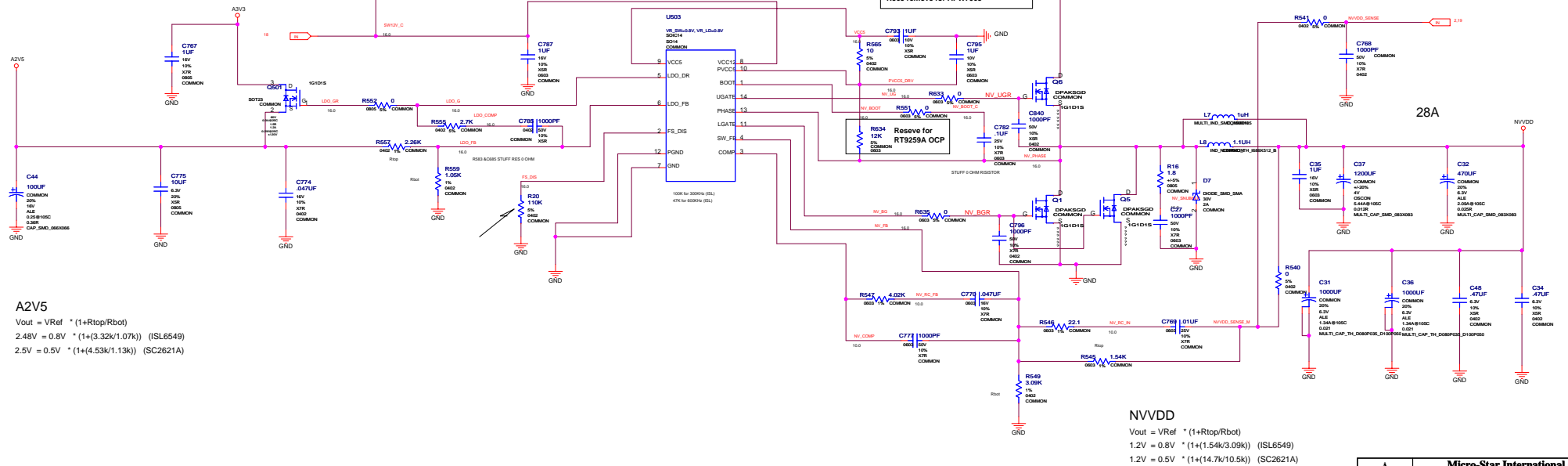
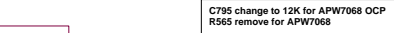
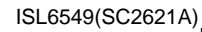
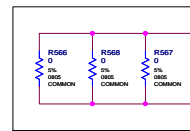
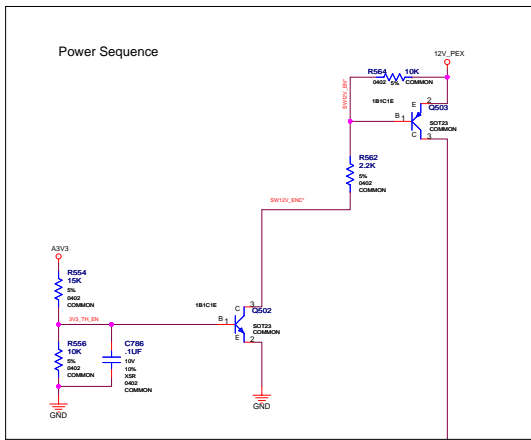
NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	500mA	12.5	5.000000
A3V3	700mA	25.0	3.300000
TMDS_IOVDD	300mA	30.0	3.300000
A3V3	700mA	25.0	3.300000
GND		35.0	0.000000



EMC suggestion reserve



PowerSupply: NVVDD, A2V5



A2V5

$$\begin{aligned} V_{out} &= V_{ref} * (1 + R_{top}/R_{bot}) \\ 2.48V &= 0.8V * (1 + (3.32k/1.07k)) \quad (ISL6549) \\ 2.5V &= 0.5V * (1 + (4.53k/1.13k)) \quad (SC2621A) \end{aligned}$$

NVVDD

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$
$$1.2V = 0.8V * (1 + (1.54k/3.09k)) \quad (ISL6549)$$
$$1.2V = 0.5V * (1 + (14.7k/10.5k)) \quad (SC2621A)$$

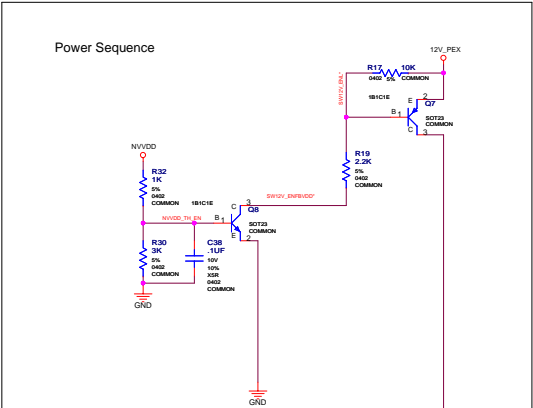


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MS-V058	
Size Custom	Document Number NVVDD, A2V5

REV  
20

PowerSupplyIII: FBVDDQ,PEX1V2



Net Name	LINE_WIDTH	CURRENT	Voltage
FBVDDQ	13MIL		2V
PEX1V2_F	2MIL	1.5	1.2V

