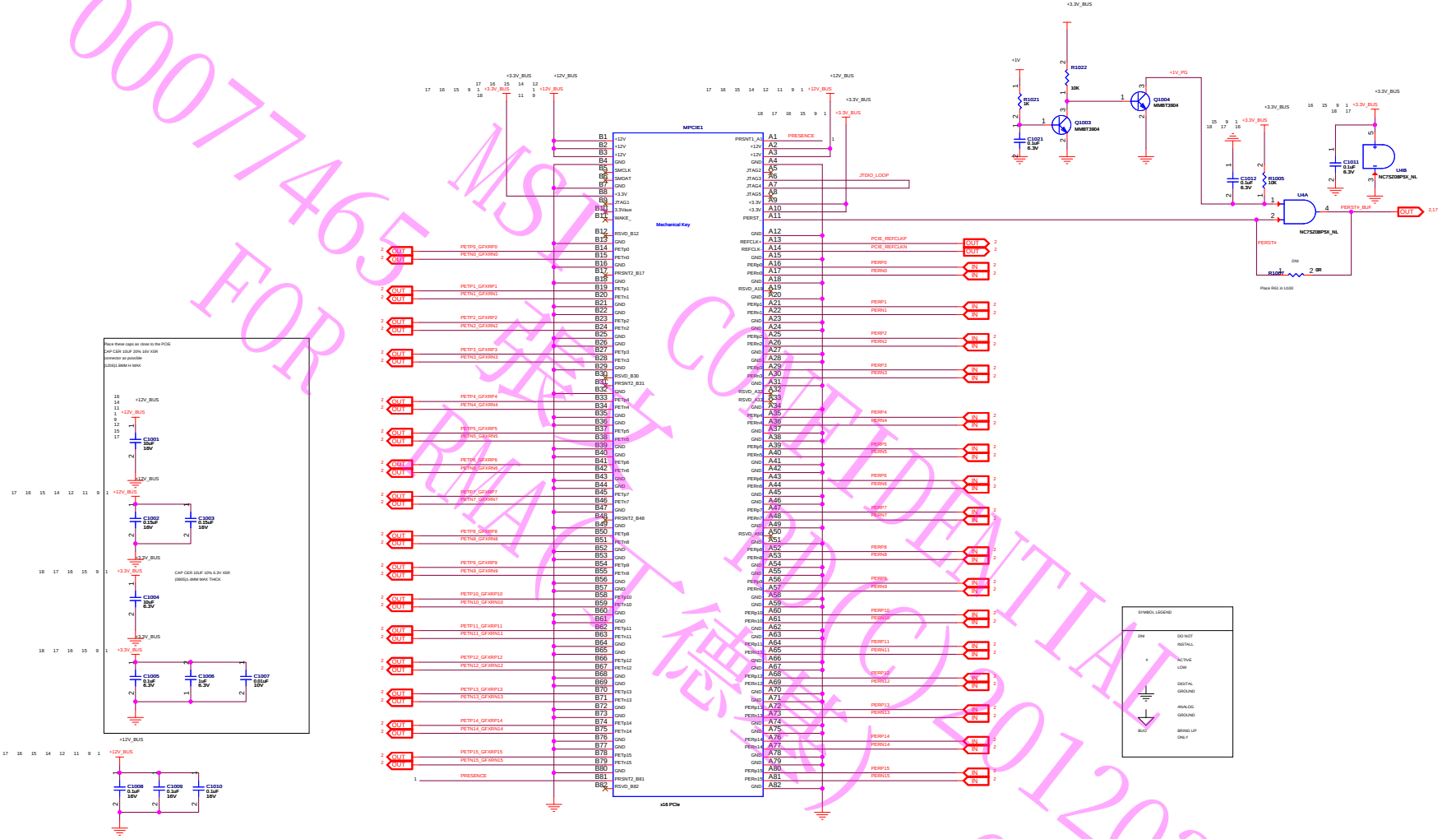
PCI-EXPRESS EDGE CONNECTOR



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FOR MSI CONFIDENTIAL
(C)2012032600
ONLY

Title	MS-V271-3.0 (AMD C445->C441)		
Size	Document Number		Rev
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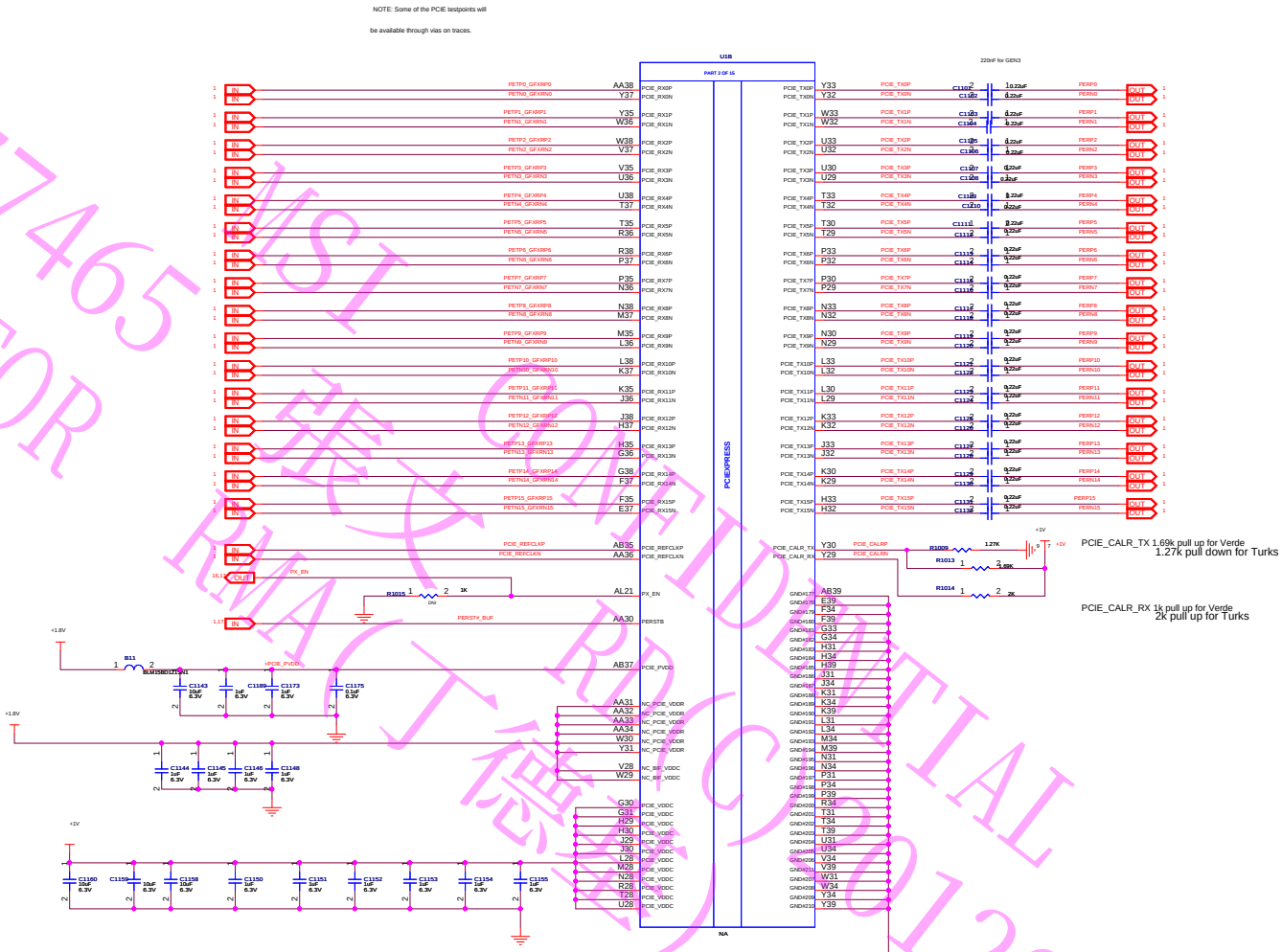
Cape_Verde PCIe Interface



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Size	Document Number		Rev
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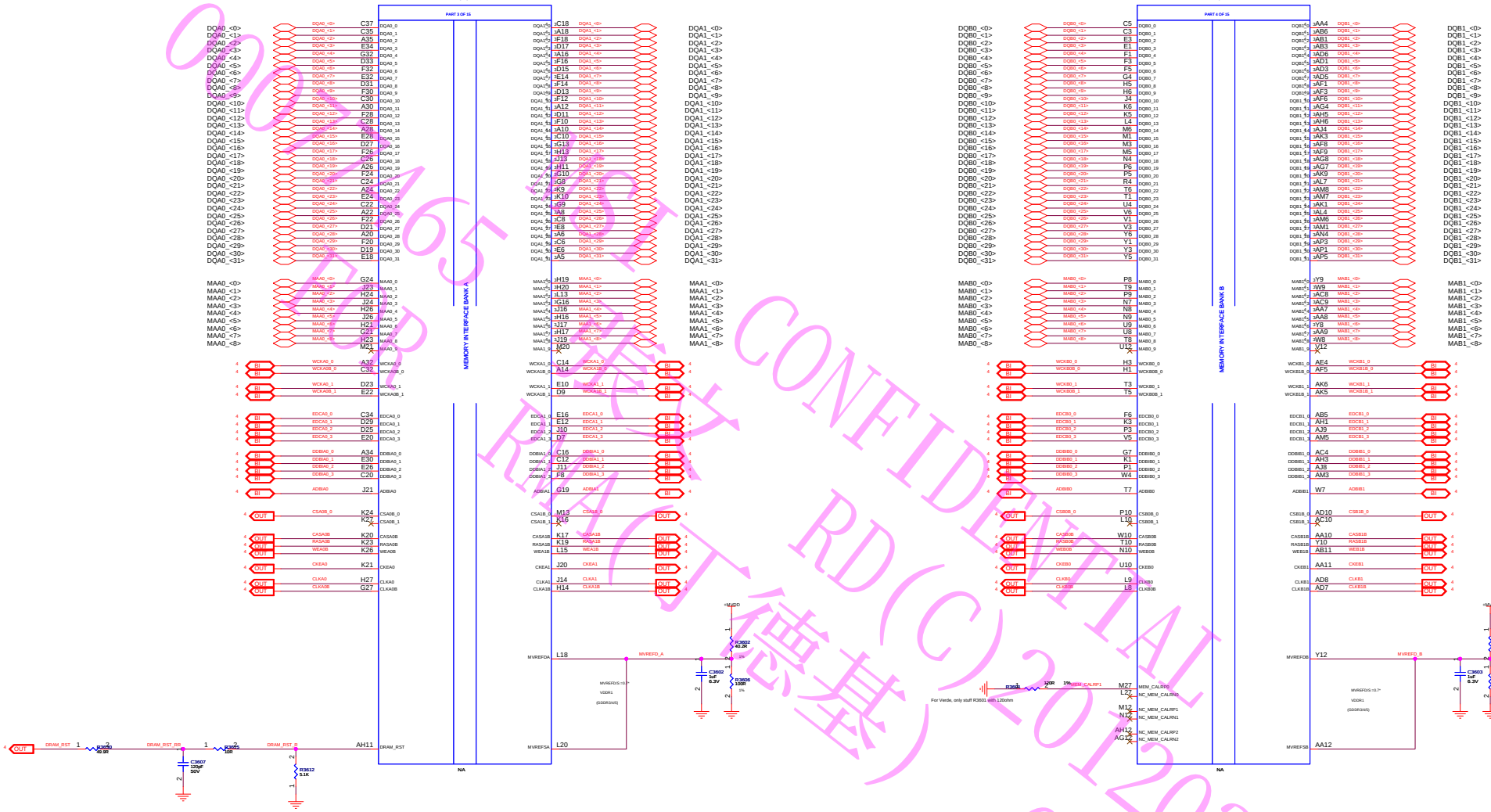
CAPE VERDE MEM Interface Ch A&B



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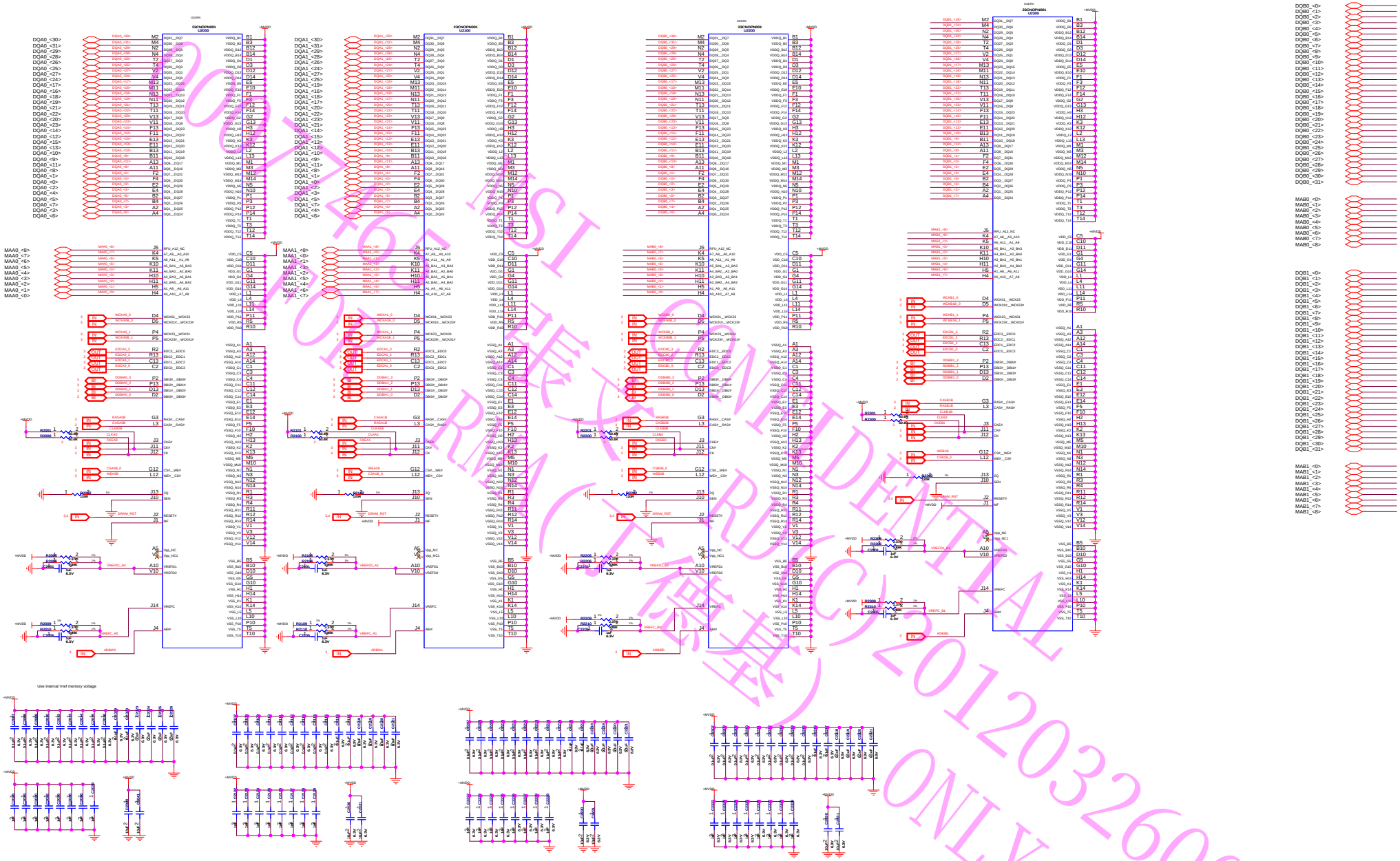
GDDR5 Memory Channel A&B



Title	MS-V271-3.0 (AMD C445->C441)	
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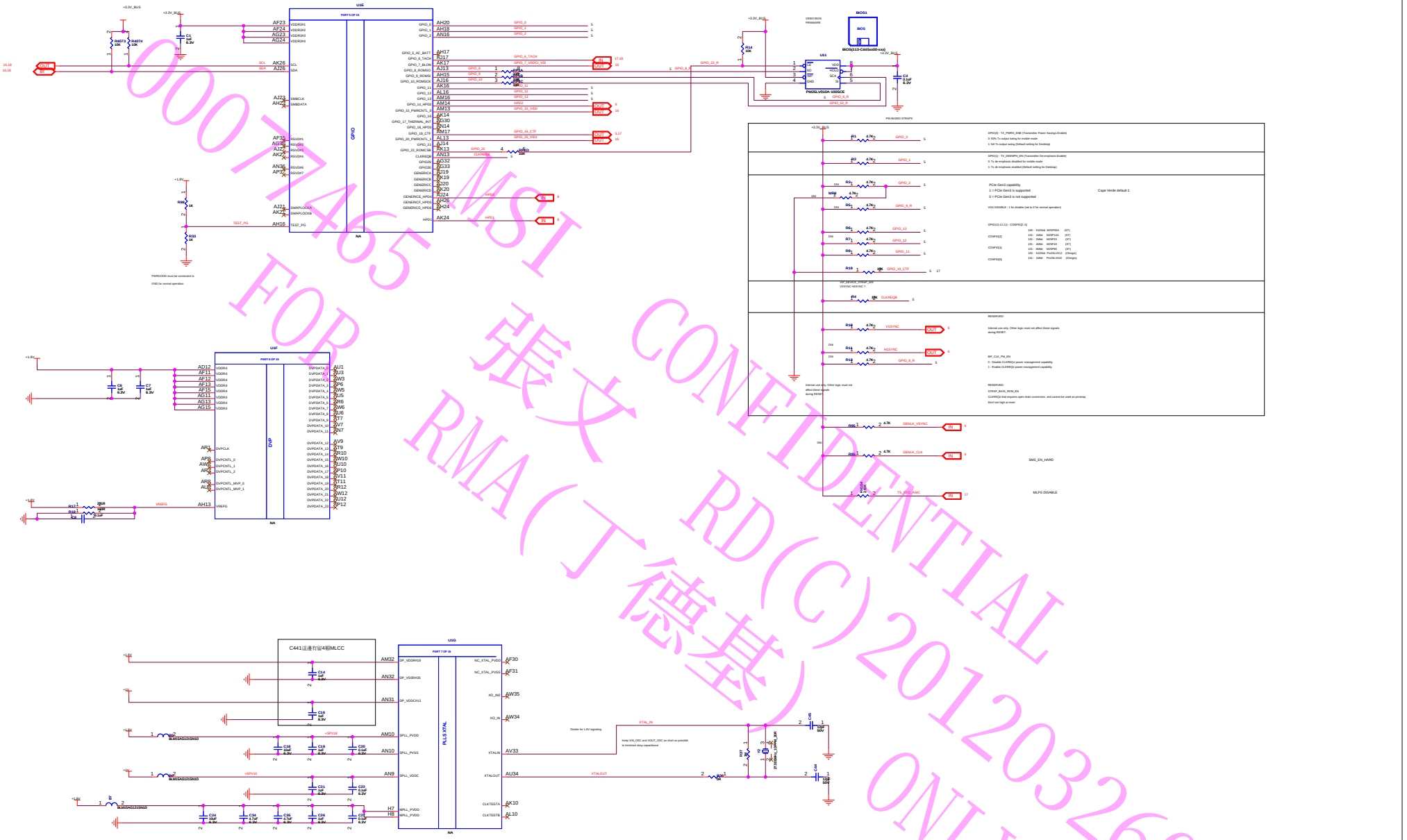
CAPE VERDE GPIOs Strap CF XTAL OSC



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Title	MS-V271-3.0 (AMD C445->C441)	
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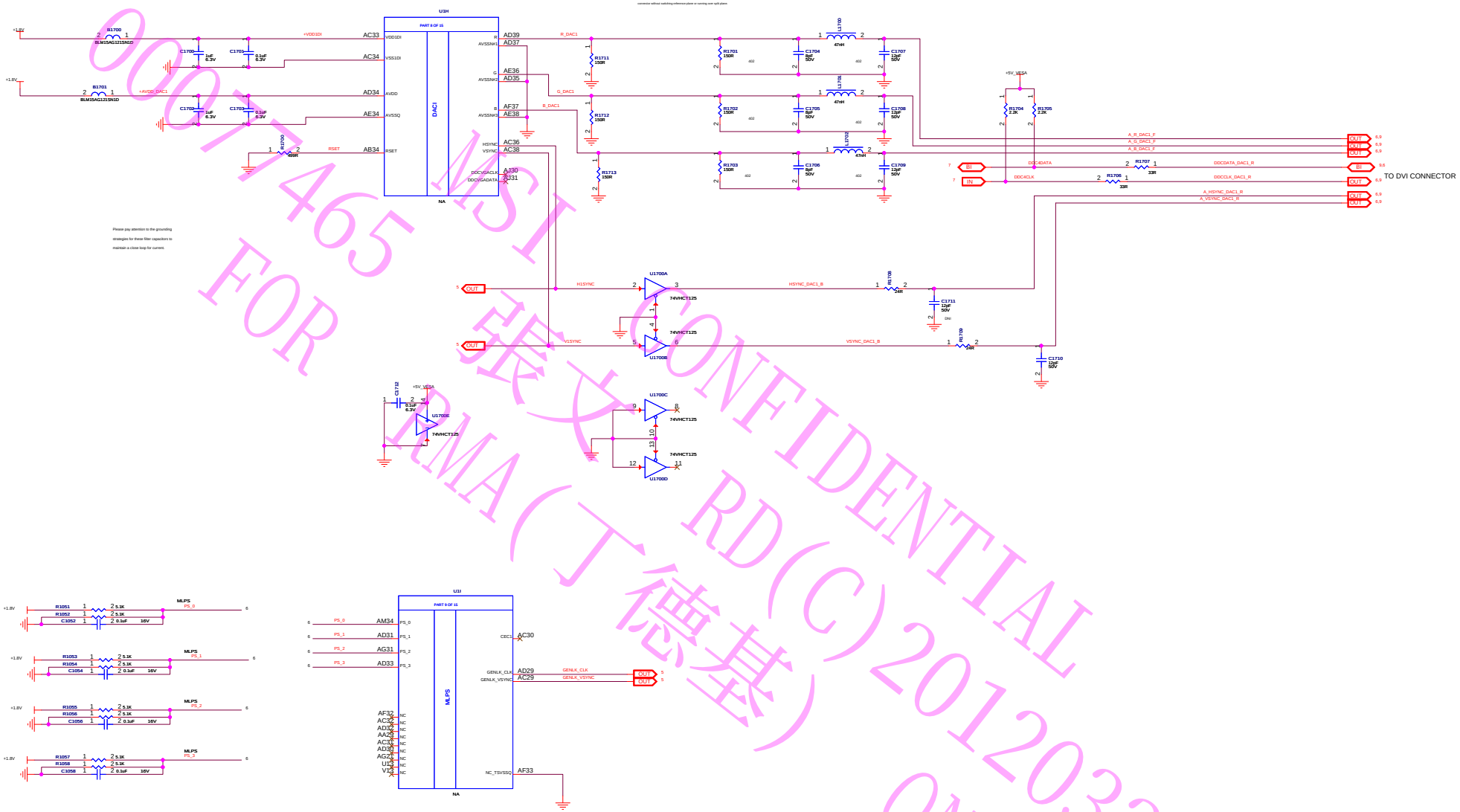

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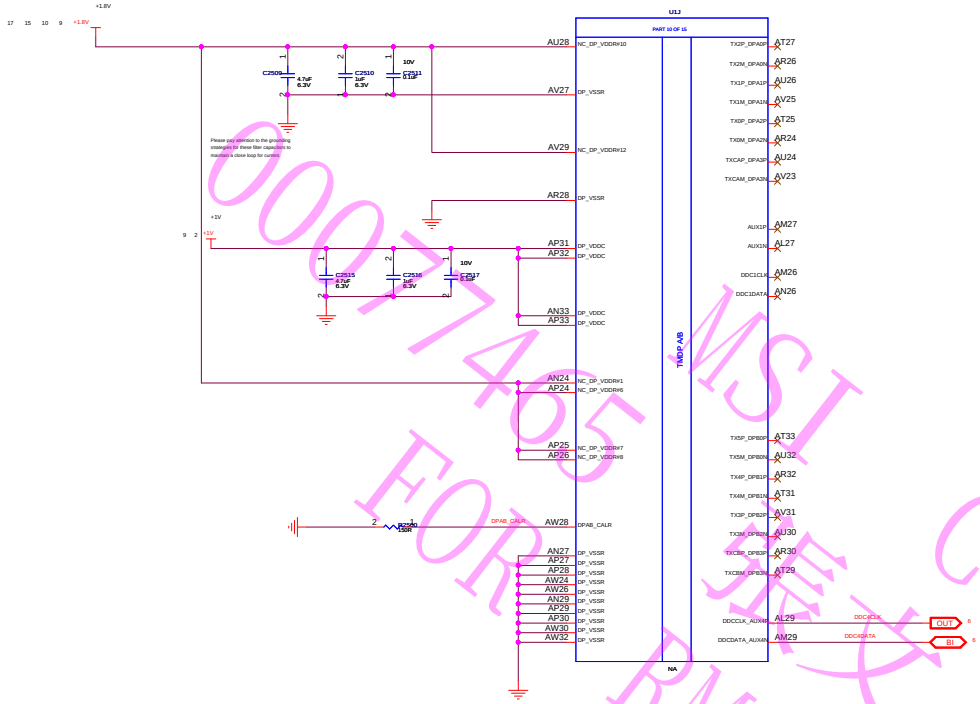

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Title	MS-V271-3.0 (AMD C445->C441)		
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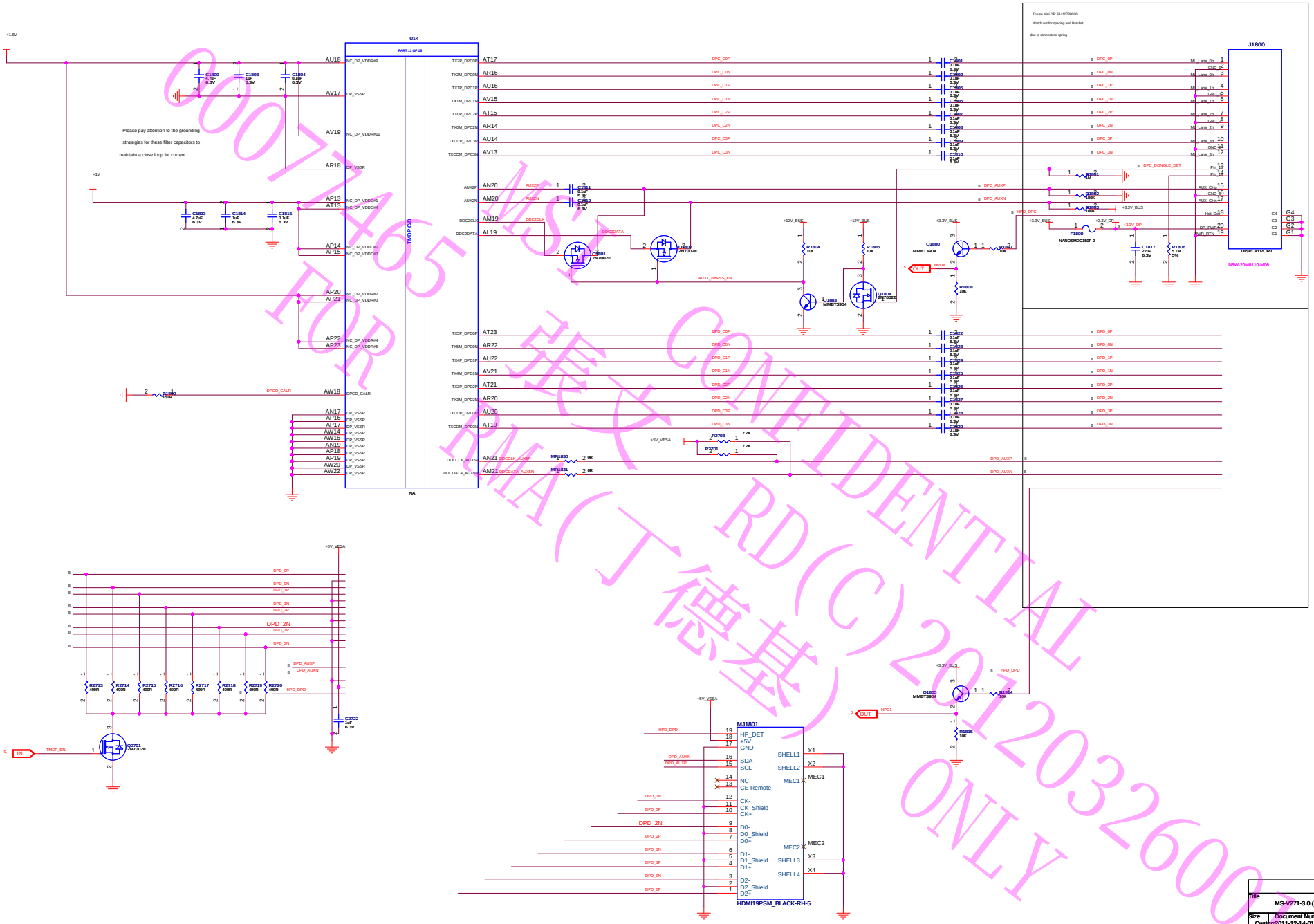

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Size: Custom	Document Number: 2011-12-14-01		Rev: 01
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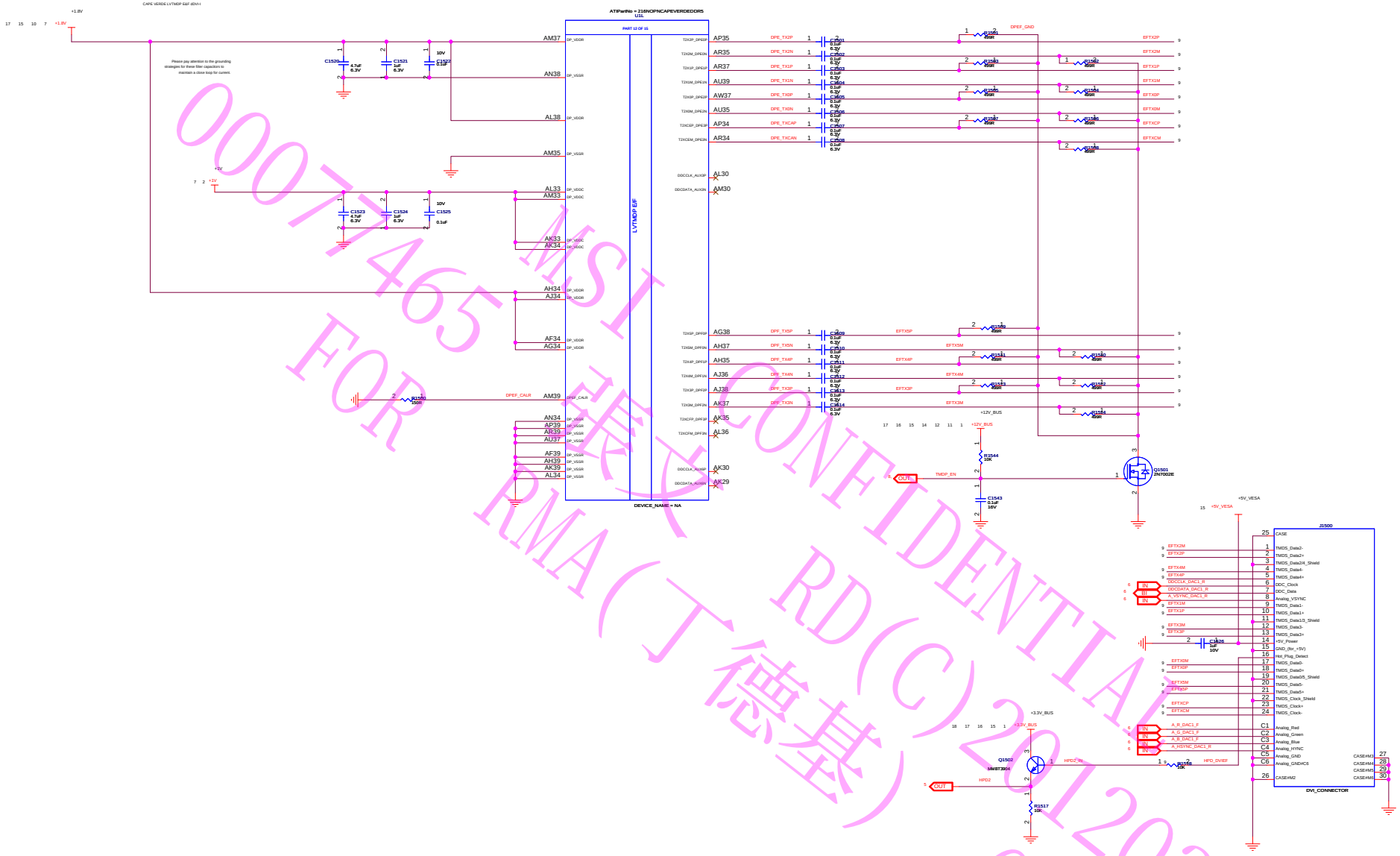

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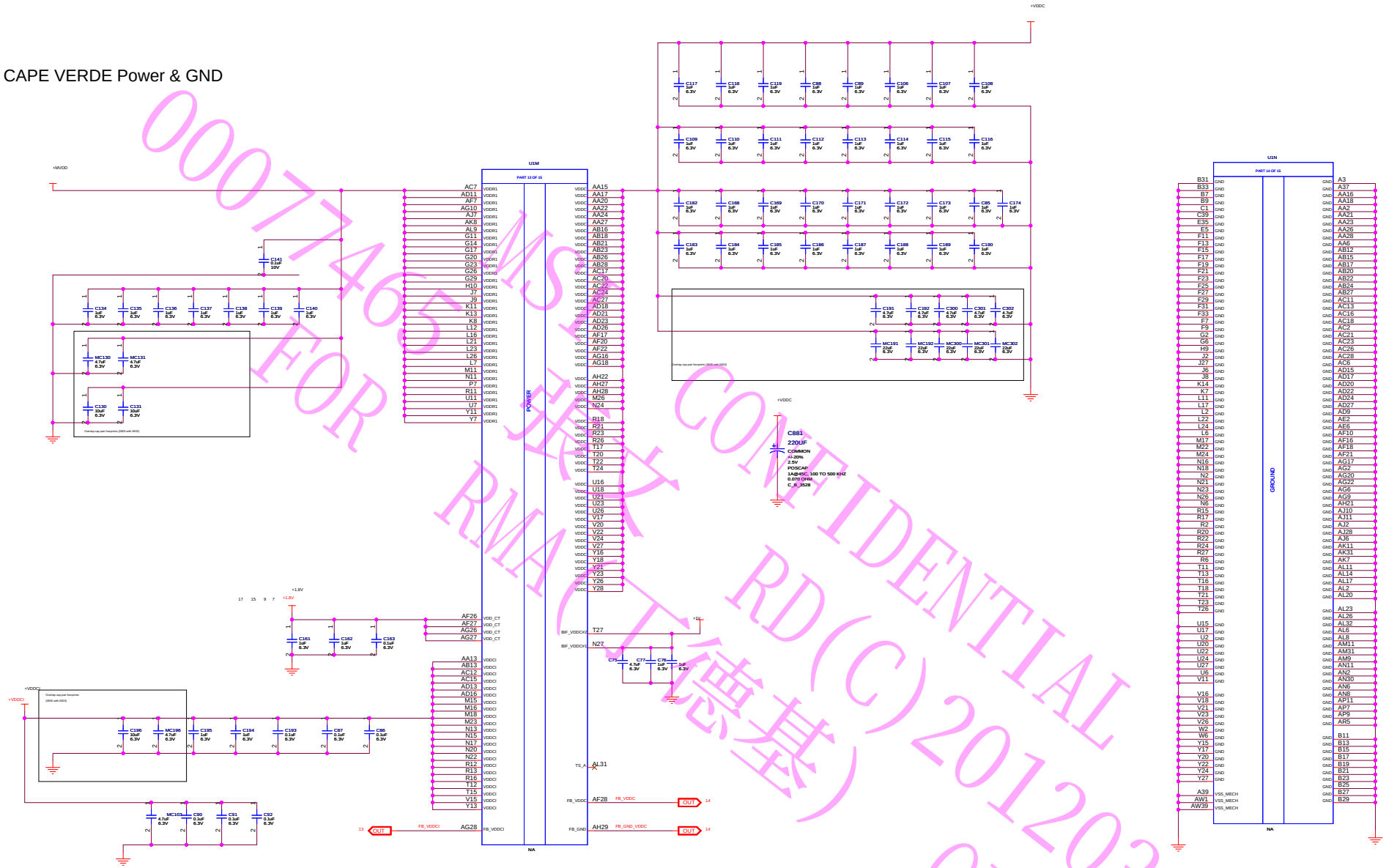
CAPE VERDE Power & GND



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Title	MS-V271-3.0 (AMD C445->C441)		
Size: Custom	Document Number: 2011-12-14-01		Rev: 01
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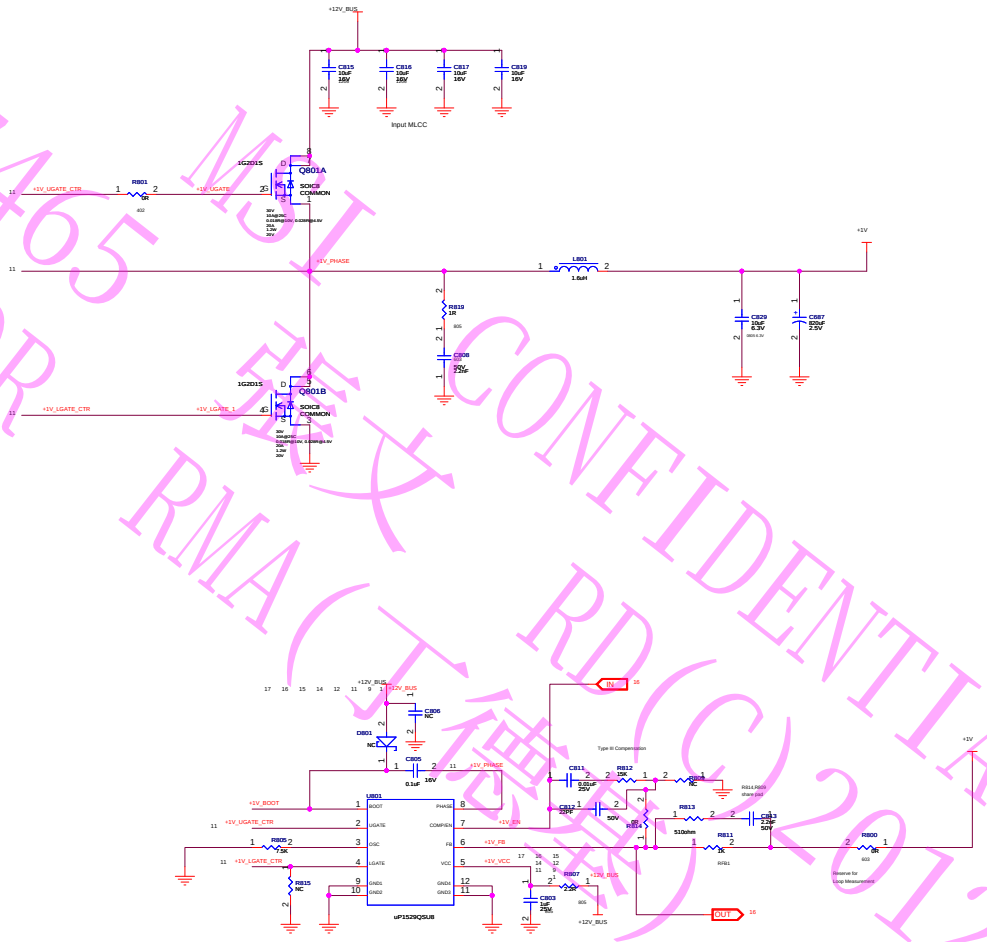

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Title	MS-V271-3.0 (AMD C445->C441)		
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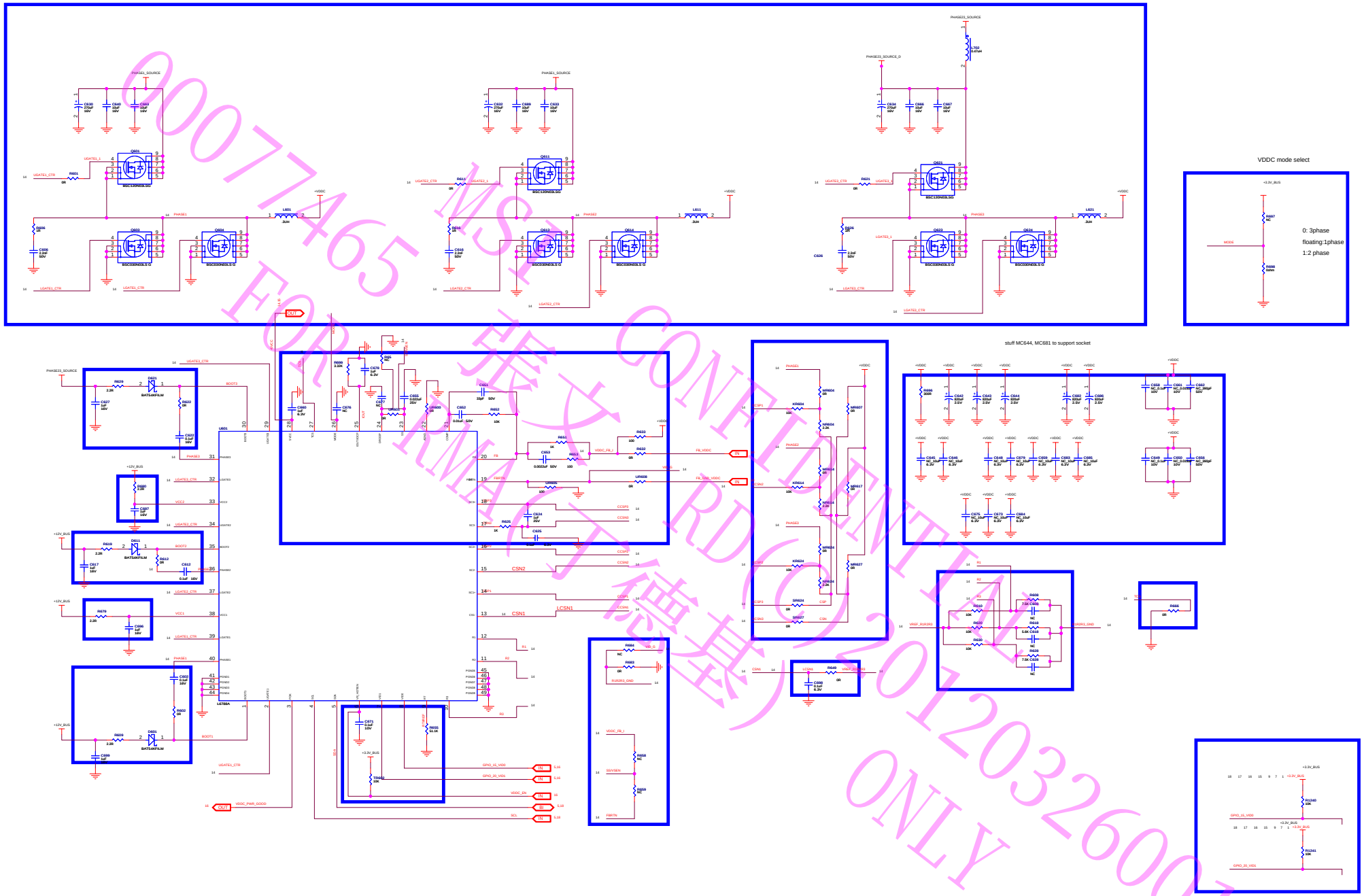

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Title	MS-V271-3.0 (AMD C445->C441)	
Size: Custom	Document Number: 2011-12-14-01	Rev: 01
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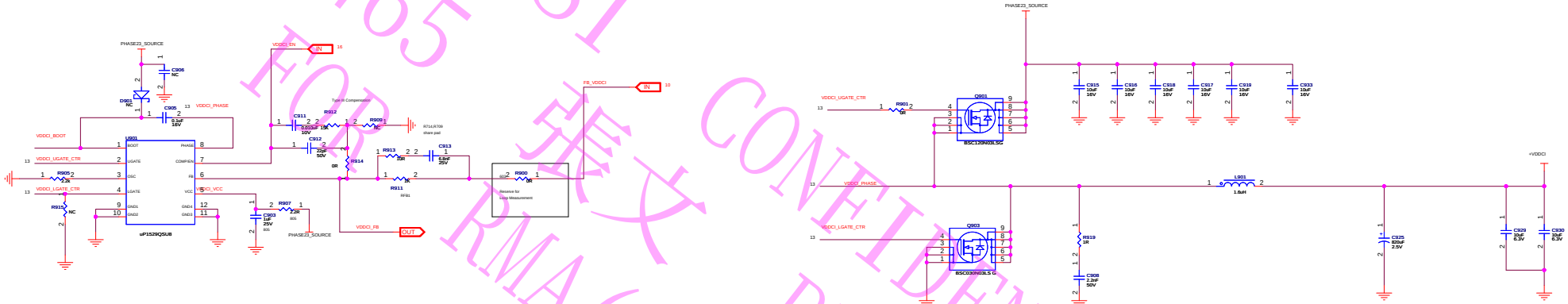

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Title	MS-V271-3.0 (AMD C445->C441)		
Size Custom	Document Number 2011-12-14-01		Rev 01
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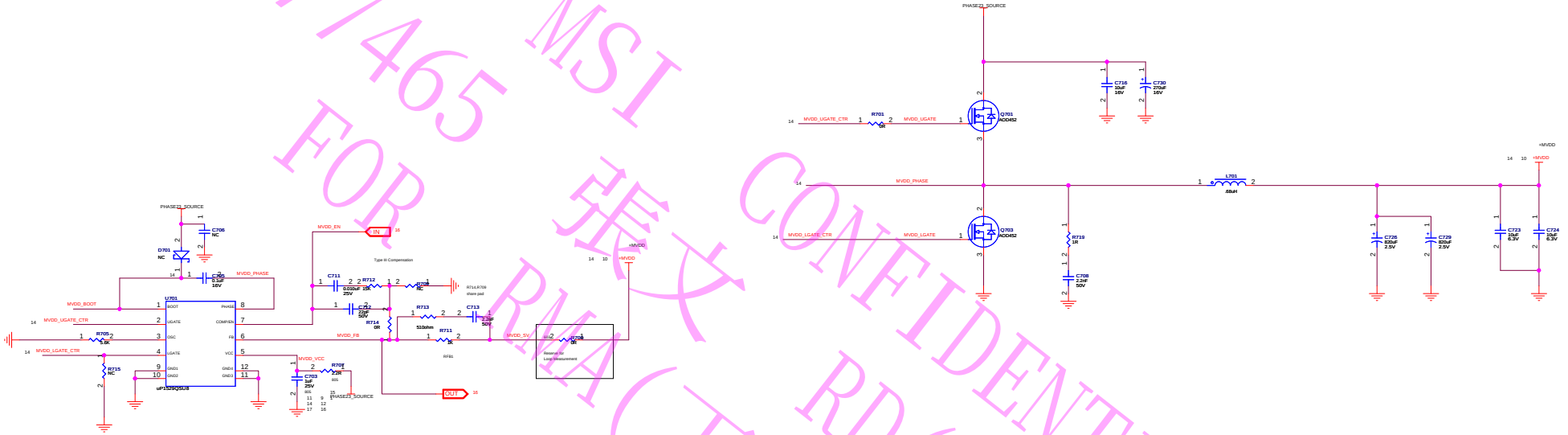

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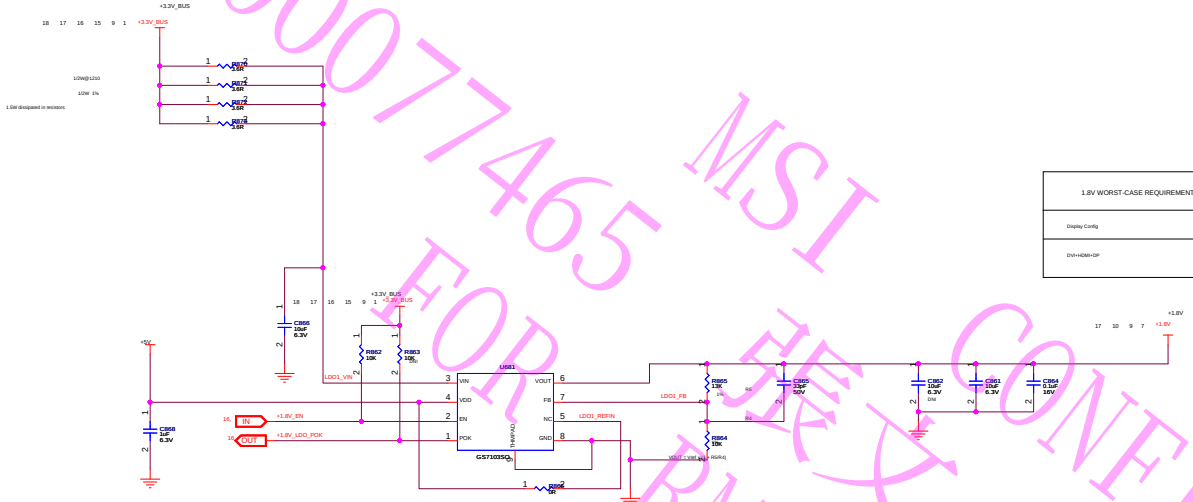
Linear Regulators

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX

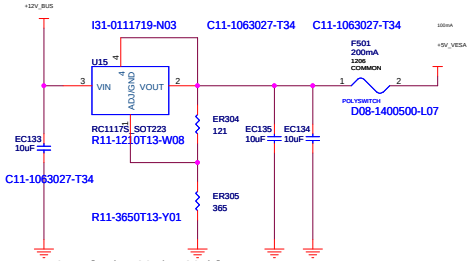
PCB: 50 to 70mm sq. copper area for cooling



1.8V WORST-CASE REQUIREMENT

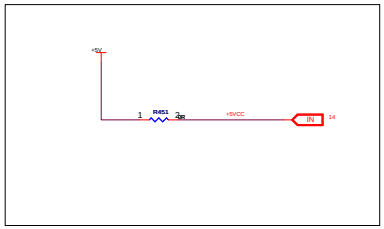
Display Config	Est. Current
DVI+HDMI+DP	1310mA

Regulators for +5V, +5V_VESA and +5V_VESA2



Vout=1.25V* [1+(ER305/ER304)]

Change +5V REGULATOR to A1117
copy from MS-V208-5.0



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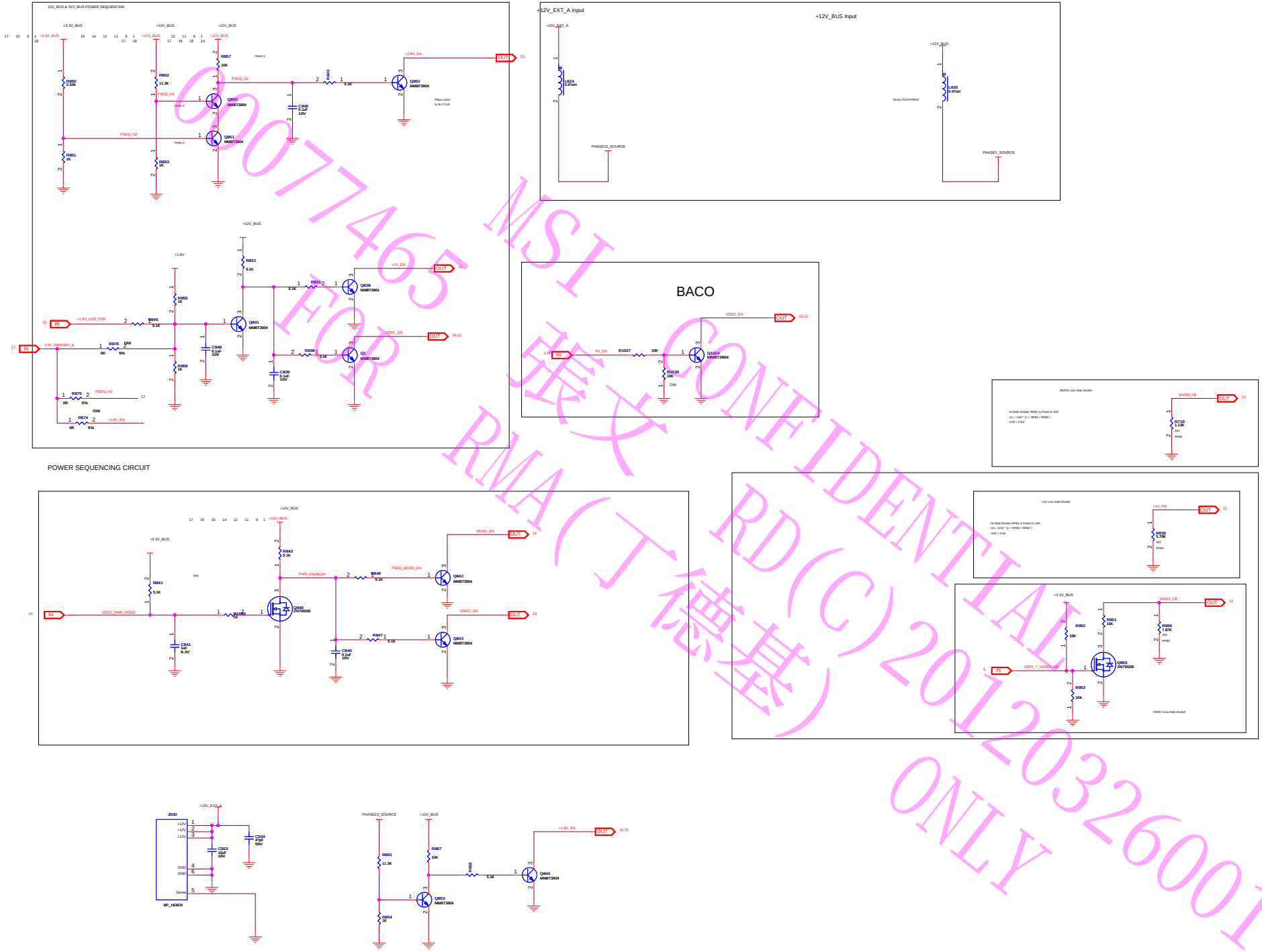
Power Management - Power Gating and Dynamic Voltage Control



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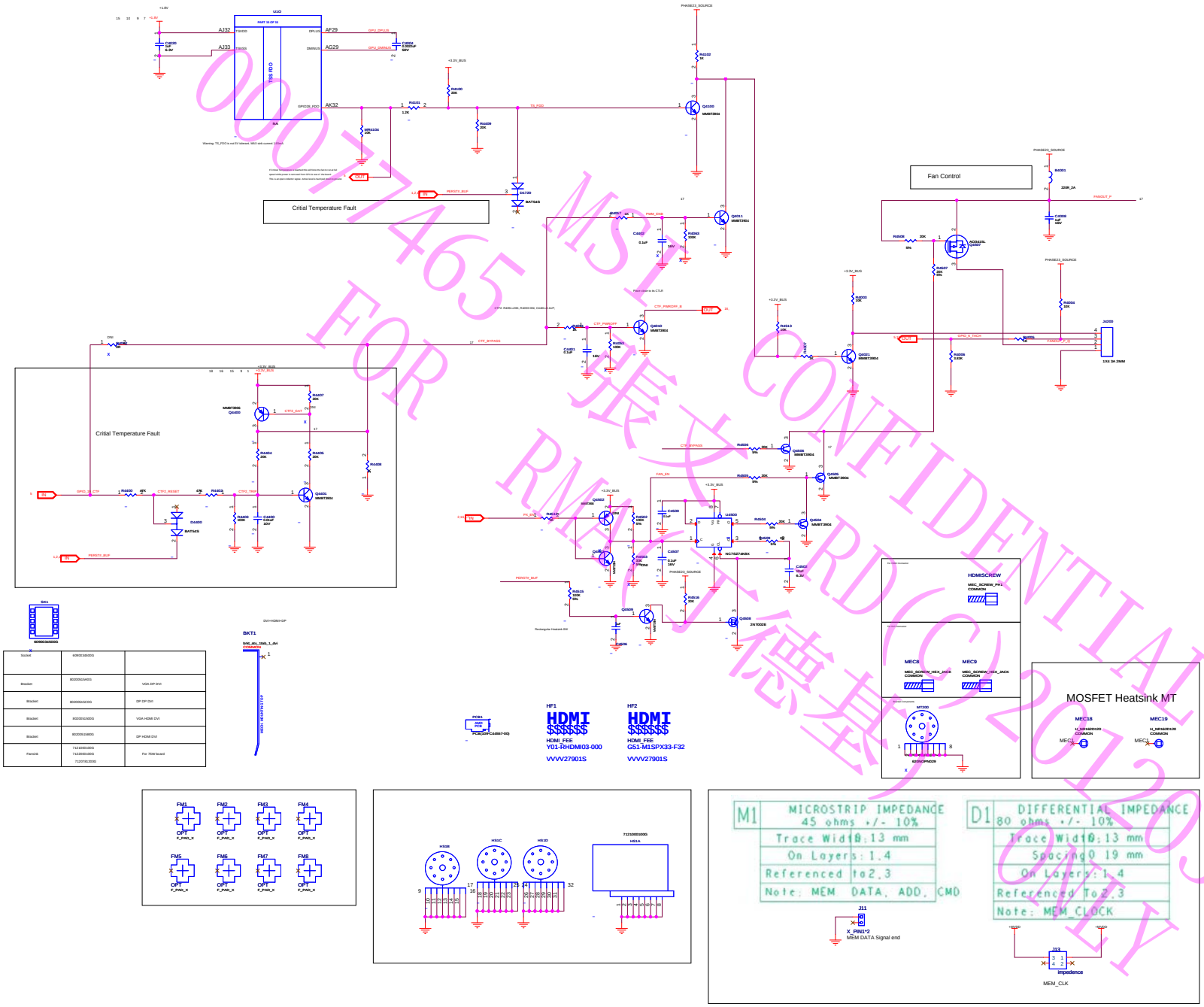
Mechanical and Thermal Management



Socket	6090310500G	
Bracket	80200615A0G	VGA DP DVI
Bracket	80200615C0G	DP DP DVI
Bracket	80200615B0G	VGA HDMI DVI
Bracket	80200615B0G	DP HDMI DVI
Panzink	712100610G0 712200610G0 712070610G0	For 7Mil board

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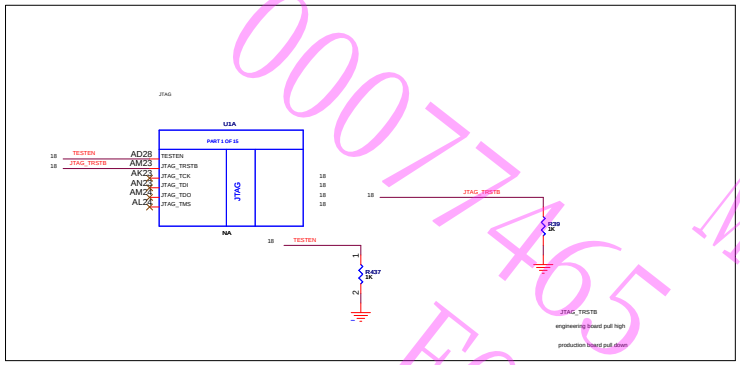
(19) Debug Circuits



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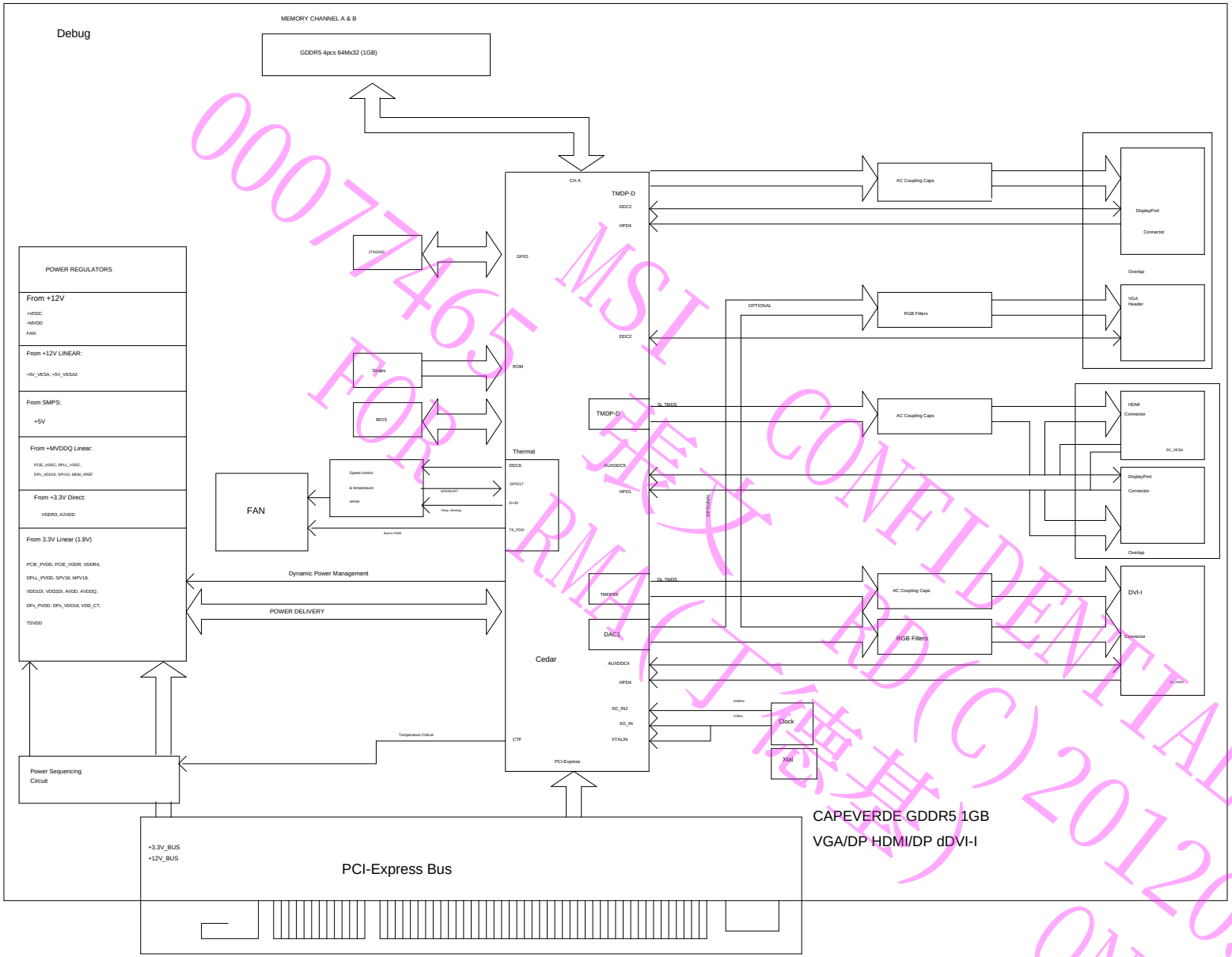

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	TITLE: CAPE VERDE PRO GDDR5 64Mx32 dDVI-I+HDMI/DP+DP/VGA	SCHEMATIC NO.: 105-C445XX-00
	DATE:	
REVISION HISTORY	NOTE: THIS SCHEMATIC REPRESENTS THE PCB. IT DOES NOT REPRESENT ANY SPECIFIC SKU. FOR STUFFING OPTIONS (COMPONENT VALUES, DNI) PLEASE CONSULT THE PRODUCT SPECIFIC BOM. PLEASE CONTACT AMD REPRESENTATIVE TO OBTAIN LASTEST BOM CLOSEST TO THE APPLICATION DESIRED.	REV: P04

SCH REV	PCB REV	DATE	REVISION DESCRIPTION
00	00A	2011/07/11	Initial CAPE VERDE schematic.
01	00B	2011/08/23	1.Update bracket DP HDMI DVI to 8D2006150800; 2. Add CAPS1288; 3. add RV870-BIF-03 to I2C DAC 4. remove BIF_VDDC
02	00C	2011/09/27	1. add BACO fet delay circuit; 2. Update 1.8V LDO symbol to G973I3; 3. Remove some debug circuit;
03	00D	2011/11/09	1. update BACO fet delay circuit;
04	00	2012/1/16	1. update CTF to shut off 1.8V;

AMD Smarter Choice

Instruction: Please specify "**PARTNER SCHEMATIC PART NUMBER:**" on the following table and please insert a "X" in the "YES" "NO" "Not Applicable" column as appropriate. Please specify "**AMD Ref schematic =**" on the following table.

PARTNER SCHEMATIC CHANGE NOTE

PARTNER SCHEMATIC PART NUMBER:

AMD REFERENCE SCHEMATIC USED: C445_00.DSN reference schematics

Partner schematic pages:	Content change description			
	YES	NO	Not Applicable	Comments
Page 1	X			1. Remove SMBus
Page 2		X		
Page 3		X		
Page 4		X		
Page 5	X			1. Delete SMBus 2. Add GPIO 5 & 6 3. Delete GPIO 17 & 29 &30 4. Delete U12 & relation
Page 6	X			1. Delete J1501 & relation 2. Delete ESD DIODES 3. Short L1710 & L1711 & L1712
Page 7		X		
Page 8	X			1. Delete J1801 & relation 2. Delete ESD solution
Page 9	X			1. Delete ESD solution
Page 10	X			1. Connect net FB_VDDCI & FB_VDDC & FB_GND_VDDC 2. Add C881 3. Delete MC176 & MC178 4. Reserve CAP for BIF_VDDC#1 & BIF_VDDC#2
Page 11	X			1. Change MOSFET & Cin & Cout 2. Short NS800 via 3. Delete low side Gate Resister. 4. Delete Cout * 2
Page 12	X			1. Delete all content & copy UPI solution from C441 2. Change Cin & Cout 3. Short NS* via
Page 13	X			1. Short NS900 via 2. Feedback sense from net FB_VDDCI 3. Delete low side Gate Resister. 4. Delete Cout * 3 5. Add Cin 10UF * 1
Page 14	X			1. Change Lin & Cin 2. Short NS700 via 3. Delete low side Gate Resister. 4. Delete Cout * 3 5. Delete Cin 10UF * 1
Page 15	X			1. Delete Vin reservation 2. Change 5V solution to 1117 3. Delete D450 & relation
Page 16	X			1. Add 6 pin EXT_12V 2. Add +12V_EXT_A power up sequence for +1.8V_EN 3. Add input 12V_BUS & 12V_EXT choke for core PWM 4. upon setting 1.~3. are copy from C441 5. Delete U680 & relation 6. Delete Vcore Rbot & relation
Page 17	X			1. Delete 2 pin fan & relation 2. Copy C441 4 pin fan & relation 3. Delete net GPU_DPLUS & GPU_DMINUS 4. Add MR4104 for MLPS 5. Reserve R4100 & R4409
Page 18	X			1. Delete U4001 & relation 2. Delete J4004 & relation
Page 19		X		
Page 20		X		

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