PCI-EXPRESS EDGE CONNECTOR

x16 PCIe

Mechanical Key

MPCIE1

PRESENCE

DNI
R2
0R

PERST#

+3.3V
C39
100nF

U5
NC7SZ08P5X_NL

R_RST
R3   0R

Place R3 in U5

PERST#_buf   [2]

PCIE_REFCLKP   [2]
PCIE_REFCLKN   [2]

+3.3V_BUS   +12V_BUS   +12V_BUS   +3.3V_BUS

Pin	Signal		Pin	Signal
B1	+12V#B1		A1	PRSNT1#A1
B2	+12V#B2		A2	+12V#A2
B3	+12V#B3		A3	+12V#A3
B4	GND#B4		A4	GND#A4
B5	SMCLK		A5	JTAG2
B6	SMDAT		A6	JTAG3
B7	GND#B7		A7	JTAG4
B8	+3.3V#B8		A8	JTAG5
B9	JTAG1		A9	+3.3V#A9
B10	3.3Vaux		A10	+3.3V#A10
B11	WAKE#		A11	PERST#

CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX
MC1 470uF   C1 10UF

CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

C2 150nF_16V   C3 150nF_16V   LF CAP CER 150NF 10% 16V X7R (0603)

C4 470uF

C5 1uF_6.3V   C6 1uF_6.3V

+12V_BUS   +3.3V

Place these caps last, ideally as close to the bus connector as possible

[2] PETp0_GFXRp0 / PETn0_GFXRn0
[2] PETp1_GFXRp1 / PETn1_GFXRn1
[2] PETp2_GFXRp2 / PETn2_GFXRn2
[2] PETp3_GFXRp3 / PETn3_GFXRn3
[2] PETp4_GFXRp4 / PETn4_GFXRn4
[2] PETp5_GFXRp5 / PETn5_GFXRn5
[2] PETp6_GFXRp6 / PETn6_GFXRn6
[2] PETp7_GFXRp7 / PETn7_GFXRn7
[2] PETp8_GFXRp8 / PETn8_GFXRn8
[2] PETp9_GFXRp9 / PETn9_GFXRn9
[2] PETp10_GFXRp10 / PETn10_GFXRn10
[2] PETp11_GFXRp11 / PETn11_GFXRn11
[2] PETp12_GFXRp12 / PETn12_GFXRn12
[2] PETp13_GFXRp13 / PETn13_GFXRn13
[2] PETp14_GFXRp14 / PETn14_GFXRn14
[2] PETp15_GFXRp15 / PETn15_GFXRn15

PRESENCE

GFXTp0_PERp0 [2] / GFXTn0_PERn0 [2]
GFXTp1_PERp1 [2] / GFXTn1_PERn1 [2]
GFXTp2_PERp2 [2] / GFXTn2_PERn2 [2]
GFXTp3_PERp3 [2] / GFXTn3_PERn3 [2]
GFXTp4_PERp4 [2] / GFXTn4_PERn4 [2]
GFXTp5_PERp5 [2] / GFXTn5_PERn5 [2]
GFXTp6_PERp6 [2] / GFXTn6_PERn6 [2]
GFXTp7_PERp7 [2] / GFXTn7_PERn7 [2]
GFXTp8_PERp8 [2] / GFXTn8_PERn8 [2]
GFXTp9_PERp9 [2] / GFXTn9_PERn9 [2]
GFXTp10_PERp10 [2] / GFXTn10_PERn10 [2]
GFXTp11_PERp11 [2] / GFXTn11_PERn11 [2]
GFXTp12_PERp12 [2] / GFXTn12_PERn12 [2]
GFXTp13_PERp13 [2] / GFXTn13_PERn13 [2]
GFXTp14_PERp14 [2] / GFXTn14_PERn14 [2]
GFXTp15_PERp15 [2] / GFXTn15_PERn15 [2]

Coupling capacitors: C7–C38, 100nF

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

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Size: C
Document Number: 105-B169xx-00A
Rev: 32
Date: Friday, June 29, 2007
Sheet 1 of 19

NOTE: some of the PCIE testpoints will
be available trought via on traces.

U1A
PART 1 OF 6

P C I - E X P R E S S I N T E R F A C E

Signal	Pin	PCIE RX	PCIE TX	Pin	Signal
[1] PETp0_GFXRp0 / [1] PETn0_GFXRn0	AC30 / AC31	PCIE_RX0P / PCIE_RX0N	PCIE_TX0P / PCIE_TX0N	AA28 / AA27	GFXTp0_PERp0 [1] / GFXTn0_PERn0 [1]
[1] PETp1_GFXRp1 / [1] PETn1_GFXRn1	AC29 / AB29	PCIE_RX1P / PCIE_RX1N	PCIE_TX1P / PCIE_TX1N	AA25 / AA24	GFXTp1_PERp1 [1] / GFXTn1_PERn1 [1]
[1] PETp2_GFXRp2 / [1] PETn2_GFXRn2	AB31 / AB30	PCIE_RX2P / PCIE_RX2N	PCIE_TX2P / PCIE_TX2N	Y28 / Y27	GFXTp2_PERp2 [1] / GFXTn2_PERn2 [1]
[1] PETp3_GFXRp3 / [1] PETn3_GFXRn3	AA31 / AA30	PCIE_RX3P / PCIE_RX3N	PCIE_TX3P / PCIE_TX3N	Y25 / Y24	GFXTp3_PERp3 [1] / GFXTn3_PERn3 [1]
[1] PETp4_GFXRp4 / [1] PETn4_GFXRn4	W30 / W31	PCIE_RX4P / PCIE_RX4N	PCIE_TX4P / PCIE_TX4N	V28 / V27	GFXTp4_PERp4 [1] / GFXTn4_PERn4 [1]
[1] PETp5_GFXRp5 / [1] PETn5_GFXRn5	W29 / V29	PCIE_RX5P / PCIE_RX5N	PCIE_TX5P / PCIE_TX5N	V25 / V24	GFXTp5_PERp5 [1] / GFXTn5_PERn5 [1]
[1] PETp6_GFXRp6 / [1] PETn6_GFXRn6	V31 / V30	PCIE_RX6P / PCIE_RX6N	PCIE_TX6P / PCIE_TX6N	T28 / T27	GFXTp6_PERp6 [1] / GFXTn6_PERn6 [1]
[1] PETp7_GFXRp7 / [1] PETn7_GFXRn7	U31 / U30	PCIE_RX7P / PCIE_RX7N	PCIE_TX7P / PCIE_TX7N	T25 / T24	GFXTp7_PERp7 [1] / GFXTn7_PERn7 [1]
[1] PETp8_GFXRp8 / [1] PETn8_GFXRn8	P30 / P31	PCIE_RX8P / PCIE_RX8N	PCIE_TX8P / PCIE_TX8N	P28 / P27	GFXTp8_PERp8 [1] / GFXTn8_PERn8 [1]
[1] PETp9_GFXRp9 / [1] PETn9_GFXRn9	P29 / N29	PCIE_RX9P / PCIE_RX9N	PCIE_TX9P / PCIE_TX9N	P25 / P24	GFXTp9_PERp9 [1] / GFXTn9_PERn9 [1]
[1] PETp10_GFXRp10 / [1] PETn10_GFXRn10	N31 / N30	PCIE_RX10P / PCIE_RX10N	PCIE_TX10P / PCIE_TX10N	M28 / M27	GFXTp10_PERp10 [1] / GFXTn10_PERn10 [1]
[1] PETp11_GFXRp11 / [1] PETn11_GFXRn11	M31 / M30	PCIE_RX11P / PCIE_RX11N	PCIE_TX11P / PCIE_TX11N	M25 / M24	GFXTp11_PERp11 [1] / GFXTn11_PERn11 [1]
[1] PETp12_GFXRp12 / [1] PETn12_GFXRn12	K30 / K31	PCIE_RX12P / PCIE_RX12N	PCIE_TX12P / PCIE_TX12N	L28 / L27	GFXTp12_PERp12 [1] / GFXTn12_PERn12 [1]
[1] PETp13_GFXRp13 / [1] PETn13_GFXRn13	K29 / J29	PCIE_RX13P / PCIE_RX13N	PCIE_TX13P / PCIE_TX13N	L25 / L24	GFXTp13_PERp13 [1] / GFXTn13_PERn13 [1]
[1] PETp14_GFXRp14 / [1] PETn14_GFXRn14	J31 / J30	PCIE_RX14P / PCIE_RX14N	PCIE_TX14P / PCIE_TX14N	J28 / J27	GFXTp14_PERp14 [1] / GFXTn14_PERn14 [1]
[1] PETp15_GFXRp15 / [1] PETn15_GFXRn15	H31 / H30	PCIE_RX15P / PCIE_RX15N	PCIE_TX15P / PCIE_TX15N	G28 / G27	GFXTp15_PERp15 [1] / GFXTn15_PERn15 [1]

Test points: TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28

Clock
[1] PCIE_REFCLKP	AD29	PCIE_REFCLKP
[1] PCIE_REFCLKN	AD30	PCIE_REFCLKN
	AC28	RSVD_1
	AC27	RSVD_2
[1] PERST#_buf	AG25	PERSTB

Calibration
PCIE_CALRN	AF25	2.0K	R8	402	+PCIE_VDDC
PCIE_CALRP	AE25	1.27K	R9	402	
PCIE_CALI	AE23	10K	R10	402	

RV610 UNFUSED A11 RH

DNI DNI
R13 R14
51R 51R
402 402

For Tektronix LA only
Place close to ASIC

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U1B PART 2 OF 6

Integrated TMDS
VIP / I2C
External TMDS
DAC / CRT
DAC2 (TV/CRT2)
General Purpose IO
PLL & XTAL
Monitor Interface
Thermal
Test

RV610 UNFUSED A11 RH

U1F PART 6 OF 6
Control
LVDS channel1

RV610 UNFUSED A11 RH

Place close to ASIC <7mm

GPIO_16 IS OUT ONLY

Note: Verify +MPVDD ripple is within specification.
(C76 changed from 10uF to 1uF)

I2C DEVICE ADDRESS' ON DDC3
DEVICE   ADDRESS
LM63   x100 1100

Place SW1 on the bottom side (easily accessible).
Clearly Mark A & B on silkscreen.
Place TR46 next to SW1

For NO ROM keep SW1B open without R46. For normal operation close SW1B or install TR46.

BIOS1
113-XXXXXX-XXX
VIDEO BIOS FIRMWARE

Possible alternate 5150005600G

Change to 10ppm/10ppm p/n 5028270000G

Place R_RtcLk close to XTAL so the main clock line has shortest stub

XTALIN
XTALOUT

EY82 27_MHZ

U1D

Memory I/O

PCI-Express

Memory I/O Internal

Memory I/O Clock

Back Bias

P O W E R

Core

RV610 UNFUSED A11 RH

Overlap

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402

+MVDD

C124 10nF C125 10nF C126 10nF C127 10nF C128 10nF C129 100nF C130 100nF C131 100nF C132 100nF C133 100nF

C134 10uF_X6S C135 10uF_X6S C136 10uF_X6S C137 10uF_X6S C138 1uF_6.3V C139 1uF_6.3V C140 1uF_6.3V C141 1uF_6.3V C142 1uF_6.3V C143 1uF_6.3V C144 1uF_6.3V C145 100nF C146 100nF

+1.8V B70 BLM15BD121SN1 +VDD_CT
C68 10uF_X6S C69 100nF C78 100nF C79 100nF C59 100nF

+3.3V +VDDR3
C91 1uF_6.3V C92 1uF_6.3V C93 100nF C99 100nF

+3.3V MR94 0R +VDDR_DVP
C94 10uF_X6S C95 1uF_6.3V C97 100nF
C96 1uF_6.3V C98 100nF

+MVDD B120 BLM15BD121SN1 B121 BLM15BD121SN1
C120 1uF_6.3V C121 1uF_6.3V C123 1uF_6.3V C122 1uF_6.3V

NS121 NS_VIA GND_VSSRH0
NS122 NS_VIA GND_VSSRH1

+VDDC
C192 1uF_6.3V C193 100nF

+PCIE_VDDR +1.8V
C900 1uF_6.3V C901 1uF_6.3V C902 1uF_6.3V C903 1uF_6.3V C904 10uF_X6S C905 10nF C906 100nF

+PCIE_VDDC B920 220R_2A +VDDC
C920 1uF_6.3V C921 1uF_6.3V C922 1uF_6.3V C923 1uF_6.3V C924 1uF_6.3V C925 1uF_6.3V C927 1uF_6.3V C928 1uF_6.3V C926 10uF_X6S

+VDDC
C161 1uF_6.3V C162 1uF_6.3V C163 1uF_6.3V C164 1uF_6.3V C165 1uF_6.3V C166 1uF_6.3V C167 1uF_6.3V C168 1uF_6.3V C169 1uF_6.3V C170 1uF_6.3V C181 10uF_X6S C182 10uF_X6S C183 10uF_X6S C184 10uF_X6S

C171 1uF_6.3V C172 1uF_6.3V C173 1uF_6.3V C174 1uF_6.3V C175 1uF_6.3V C176 1uF_6.3V C177 1uF_6.3V C178 1uF_6.3V C179 1uF_6.3V C180 1uF_6.3V

+VDDCI B78 220R_2A +VDDC
C74 100nF C75 1uF_6.3V C73 1uF_6.3V C77 10uF_X6S

[7] M_MDA[63..0]

U1C

Part 3 of 6

MEMORY
INTERFACE

M_MDA0 E29 DQ_0   MA_0 B14 M_MAA0   M_MAA[15..0] [7]
M_MDA1 E30 DQ_1   MA_1 A14 M_MAA1
M_MDA2 E31 DQ_2   MA_2 B13 M_MAA2
M_MDA3 D31 DQ_3   MA_3 E14 M_MAA3
M_MDA4 C29 DQ_4   MA_4 B17 M_MAA4
M_MDA5 B29 DQ_5   MA_5 A17 M_MAA5
M_MDA6 B30 DQ_6   MA_6 C15 M_MAA6
M_MDA7 A29 DQ_7   MA_7 G16 M_MAA7
M_MDA8 E26 DQ_8   MA_8 E16 M_MAA8
M_MDA9 D26 DQ_9   MA_9 C14 M_MAA9
M_MDA10 E25 DQ_10   MA_10 A12 M_MAA10
M_MDA11 D25 DQ_11   MA_11 B12 M_MAA11
M_MDA12 G23 DQ_12   MA_BA0 C12 M_MAA14
M_MDA13 G21 DQ_13   MA_BA1 D14 M_MAA15
M_MDA14 E21 DQ_14   MA_A12 B15 M_MAA12
M_MDA15 D21 DQ_15   MA_BA2 G14 M_MAA13
M_MDA16 C28 DQ_16
M_MDA17 B28 DQ_17   DQMb_0 D30 M_DQMA#0   M_DQMA#[7..0] [7]
M_MDA18 B27 DQ_18   DQMb_1 G25 M_DQMA#1
M_MDA19 A27 DQ_19   DQMb_2 C26 M_DQMA#2
M_MDA20 C25 DQ_20   DQMb_3 C21 M_DQMA#3
M_MDA21 A25 DQ_21   DQMb_4 C5 M_DQMA#4
M_MDA22 C24 DQ_22   DQMb_5 D6 M_DQMA#5
M_MDA23 C23 DQ_23   DQMb_6 D2 M_DQMA#6
M_MDA24 B23 DQ_24   DQMb_7 K3 M_DQMA#7
M_MDA25 A23 DQ_25
M_MDA26 B22 DQ_26   QS_0 C30 M_QSA0   M_QSA[7..0] [7]
M_MDA27 C20 DQ_27   QS_1 D23 M_QSA1
M_MDA28 B20 DQ_28   QS_2 B26 M_QSA2
M_MDA29 A20 DQ_29   QS_3 B21 M_QSA3
M_MDA30 C19 DQ_30   QS_4 B6 M_QSA4
M_MDA31 C8 DQ_31   QS_5 E7 M_QSA5
M_MDA32 C7 DQ_32   QS_6 E2 M_QSA6
M_MDA33 B7 DQ_33   QS_7 J2 M_QSA7

read strobe

M_MDA34 A7 DQ_34   QS_0B C31
M_MDA35 A5 DQ_35   QS_1B E23
M_MDA36 C4 DQ_36   QS_2B A26
M_MDA37 B4 DQ_37   QS_3B A21
M_MDA38 A3 DQ_38   QS_4B A6
M_MDA39 G9 DQ_39   QS_5B D7
M_MDA40 E9 DQ_40   QS_6B E1
M_MDA41 D9 DQ_41   QS_7B J1

write strobe

M_MDA42 G7 DQ_42
M_MDA43 G5 DQ_43   ODT0 E20   ODT [7]
M_MDA44 F5 DQ_44   ODT1 C11
M_MDA45 G4 DQ_45
M_MDA46 F4 DQ_46   CLK0 A18 CLKA0 [7]
M_MDA47 B3 DQ_47   CLK1 A11 CLKA1 [7]
M_MDA48 C2 DQ_48
M_MDA49 C1 DQ_49   CLK0b B18 CLKA#0 [7]
M_MDA50 E3 DQ_50   CLK1b B11 CLKA#1 [7]
M_MDA51 F3 DQ_51
M_MDA52 F3 DQ_52   RAS0b G20 RASA#0 [7]
M_MDA53 F1 DQ_53   RAS1b D12 RASA#1 [7]
M_MDA54 G2 DQ_54
M_MDA55 G1 DQ_55   CAS0b D20 CASA#0 [7]
M_MDA56 H3 DQ_56   CAS1b E12 CASA#1 [7]
M_MDA57 K3 DQ_57
M_MDA58 K2 DQ_58   CS0b_0 E18 CSA#0_0 [7]
M_MDA59 L3 DQ_59   CS0b_1 G18
M_MDA60 L2 DQ_60
M_MDA61 L1 DQ_61   CS1b_0 G11 CSA#1_0 [7]
M_MDA62 DQ_62   CS1b_1 E11
M_MDA63 DQ_63
                       CKE0 D18 CKEA0 [7]
MVREFD_0 F30 MVREFD   CKE1 G12 CKEA1 [7]
MVREFS_0 F31 MVREFS
                       WE0b D16 WEA#0 [7]
                       WE1b C10 WEA#1 [7]
L5 TEST_MCLK
L7 TEST_YCLK
J7 MEMTEST   DRAM_RST J5

RV610 UNFUSED A11 RH

SHOULD CS BE RUN DIFFERENTIALLY????

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

+MVDD
R291 100R
R292 100R
C295 100nF   C296 10nF

+MVDD
R293 100R
R294 100R
C297 100nF   C298 10nF

+MVDD
R295 2.0K

+MVDD
DNI
MR295 4.7K

Overlap

R296 4.7K   R297 4.7K   R298 243R

DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

U1E

Part 5 of 6

PCI-Express GND

Pin	Signal
AA26	PCIE_VSS_1
AA29	PCIE_VSS_2
AC26	PCIE_VSS_3
AD31	PCIE_VSS_4
AE29	PCIE_VSS_5
AE30	PCIE_VSS_6
AE31	PCIE_VSS_7
F28	PCIE_VSS_8
G26	PCIE_VSS_9
G29	PCIE_VSS_10
G30	PCIE_VSS_11
G31	PCIE_VSS_12
H29	PCIE_VSS_13
J25	PCIE_VSS_14
J26	PCIE_VSS_15
L26	PCIE_VSS_16
L29	PCIE_VSS_17
L30	PCIE_VSS_18
L31	PCIE_VSS_19
M26	PCIE_VSS_20
M29	PCIE_VSS_21
P26	PCIE_VSS_22
R29	PCIE_VSS_23
R30	PCIE_VSS_24
R31	PCIE_VSS_25
T26	PCIE_VSS_26
U29	PCIE_VSS_27
V26	PCIE_VSS_28
Y26	PCIE_VSS_29
Y29	PCIE_VSS_30
Y30	PCIE_VSS_31
Y31	PCIE_VSS_32

Pin	Signal
B25	VSS_33
J8	VSS_34
B5	VSS_35
D11	VSS_36
C17	VSS_37
C22	VSS_38
C27	VSS_39
D29	VSS_40
C3	VSS_41
C6	VSS_42
D3	VSS_43
D28	VSS_44
F29	VSS_45
D4	VSS_46
F11	VSS_47
F12	VSS_48
F14	VSS_49
F16	VSS_50
F18	VSS_51
F20	VSS_52
F21	VSS_53
F23	VSS_54
F25	VSS_55
F7	VSS_56
F9	VSS_57
G3	VSS_58
G6	VSS_59
H23	VSS_60
J3	VSS_61
J4	VSS_62
J6	VSS_63
K1	VSS_64
L12	VSS_65
L15	VSS_66
L18	VSS_67
L21	VSS_68
L6	VSS_69
M11	VSS_70
M14	VSS_71
M17	VSS_72
M20	VSS_73
M6	VSS_74
P12	VSS_75
P15	VSS_76
P18	VSS_77
P21	VSS_78
P6	VSS_79
AC21	VSS_80
R14	VSS_81
R17	VSS_82
R20	VSS_83
T6	VSS_84
U1	VSS_85
U12	VSS_86
U15	VSS_87
U18	VSS_88
U21	VSS_89
AE20	VSS_90
V14	VSS_91
V17	VSS_92
V20	VSS_93
P2	VSS_94
V6	VSS_95
W2	VSS_96
Y12	VSS_97
Y15	VSS_98
Y18	VSS_99
Y21	VSS_100
Y6	VSS_101
M9	VSS_102

Pin	Signal
A13	VSS_1
A2	VSS_2
C18	VSS_3
A24	VSS_4
A30	VSS_5
AA1	VSS_6
AA11	VSS_7
AA14	VSS_8
AA17	VSS_9
AA20	VSS_10
AA6	VSS_11
AC2	VSS_12
AC7	VSS_13
AE3	VSS_14
AL4	VSS_15
AD14	VSS_16
AF12	VSS_17
AF14	VSS_18
AD16	VSS_19
AD18	VSS_20
AE6	VSS_21
AG2	VSS_22
AE9	VSS_23
AH25	VSS_24
AK1	VSS_25
AK31	VSS_26
AJ6	VSS_27
AL2	VSS_28
AL30	VSS_29
B1	VSS_30
C13	VSS_31
	VSS_32

CORE GND

RV610 UNFUSED A11 RH

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CHANNEL A: RANK 0 128MB DDR2

CORE REGULATOR +VDDC

+12V_BUS

ER1593
2R2

ED28
BAT54SLT1

+12V_BUS

EB1
Chock 1.2u

EC116   EC117   EC301
10uF   10uF   470UF

EC3   ER1594
0.1uF   0R

ER1592   0R

EMU31
1 BOOT   PHASE 8
2 UGATE OPS   7
3 GND   FB   6
4 LGATE VCC   5
APW7120

ER6
15.3K

EQ28
(TO-252)

APM2512 TO-252

EL21

Dip 1.6uH

+VDDC

EC1532 EC1148 EC1146   EC323   EC321
1.0uF   10uF   10uF   820uF_6.3V 820uF_6.3V

SS_VDDC3

EQ31
(TO-252)

APM2512 TO-252

ER1618   0R

+12V_BUS

ER1686

1.87k

ER5
4.32K

EC143
0.1uF

EC1688   ER7
100nF   200RF

+3.3V_BUS   +12V_BUS

ER15   ER14
1K   10K

EQ106
2N7002

Q992
MMBT3904

Core Power Delay

ER16
2K

Title TR RV630 - MVDD SMPS02

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+MVDD

EC164
10uF
Cout1

EC159
10uF

EC346
10uf

+3.3V_BUS

6.3V
1206

C1016
10uf
Y5V

Q996
APM2054NVC

+12V_BUS

R1000
5.1K
402
5%

R999   5.1K

402

Q998
MMBT3904

+12V_BUS

R990
10K

Q997
MMBT3904

+VDDC

R998
1K
402
1%

R997
2K
402
1%

R989
100K

C994
0.1uf

C993
10uf

+3.3V

LVT_EN   [3]

+3.3V

C995
10uf

C996
10uf

C997
10uf

+3.3V

C1011
100pF

C1014
100pF

C1015
100pF

+3.3V

C998
1000 pF

C999
1000 pF

C1000
1000 pF

+3.3V

C1017
10nF

C1019
10nF

C1018
10nF

+3.3V
ER124
15R

2.5V_REF1

APL431BAC_SOT23
EREG9
EC109
10uF_6.3V
DNI
ER125 R1
1.2K
1%
1.2V_REF1
ER126 R2
1.1K
1%

+3.3V   +5V   U951_VCNTL
U951_VIN
2.5V_REF1

C958   C957   C956
1uF_6.3V 10uF   10uF

R951
383R

U951_REFEN
R952
1K
C954
1uF_6.3V

+1.8V   U951_VOUT

R953   C953   C952   C951   C955
1K   22uF   10uF   10uF   10uF

U951
VIN   NC#8
GND   NC#7
VREF   VCNTL
VOUT   NC
       THM
APL5331

U951_VIN
U951_REFEN
U951_VOUT
U951_VCNTL

+12V_BUS   +5V

U4
VIN ADJ/GND VOUT
RC1117S_SOT223
I31-01117F9-A30

EC133
10uF

ER304
121
R11-1210T13-W08

ER305
365
R11-3650T13-Y01

EC135   EC134
10uF   10uF

Vout=1.25V* [1+(ER305/ER304)]

+3.3V
DIODE SCHOTTKY SK32   D705   D704   DIODE SCHOTTKY SK32

+12V_BUS
EC100   100nF
EC339   EC340
22uf   22uf

1.2V_REF1   ER113   1K
402
U84A
LM358MX_SOC8
C1029
10nF

EQ33
APM3023LUC-TR
+MVDD

R113   510R

ER115
1K

EC805   C340   C346
DIP_1000uF 10uf 10uf

Shared Power Rails

+1.8V +AVDD   +A2VDDQ   +VDD1DI   +VDD2DI   +DPLL_PVDD   +TPVDD   +TXVDDR   +T2PVDD

B882   B883   B884   B885   B886   B887   B888   B889
BLM15BD121SN1 BLM15BD121SN1 BLM15BD121SN1 BLM15BD121SN1 BLM15BD121SN1 BLM15BD121SN1 BLM15BD121SN1 BLM15BD121SN1

PIN BASED STRAPS

+3.3V

Designator				
DNI MR50 10K	R50 10K	GPIO_0		GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)ATI PCIE FEATURE I

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)ATI PCIE FEATURE I
 0: 50% Tx output swing for mobile mode
 1: full Tx output swing (Default setting for Desktop)

DNI MR50 10K   R50 10K   GPIO_0

DNI MR51 10K   R51 10K   GPIO_1

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)ATI PCIE FEATURE II
 0: Tx de-emphasis disabled for mobile mode
 1: Tx de-emphasis enabled (Default setting for Desktop)

MR52 10K   DNI R52 10K   GPIO_2

MR53 10K   DNI R53 10K   GPIO_3

GPIO(3:2) - ATI Internal Use Only - Reserved (Default: 00)

MR54 10K   1K for BUO R54 10K   GPIO_4

GPIO(4) - DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

MR55 10K   DNI R55 10K   GPIO_5

GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)

MR56 10K   DNI R56 10K   GPIO_6

GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)

MR57 10K   NTSC R57 10K   GPIO_7

GPIO(7) - TV OUT STANDARD (Jumper position overwrite resistor settings)
 0 - PAL TVO (Jumper is closed)
 1 - NTSC TVO (Jumper is open)

MR58 10K   DNI R58 10K   GPIO_8

GPIO(8) - ATI Internal Use Only - Reserved (Default: 0)

MR59 10K   R59 10K   GPIO_9

MR63 10K   R63 10K   GPIO_13

MR62 10K   R62 10K   GPIO_12

MR61 10K   R61 10K   GPIO_11

GPIO(9,13:11) - CONFIG[3..0] IF
BIOS_ROM_EN=1 [default] (GPIO_22)
tmel - AT25F512A (512 kbit)0010
   AT25F1024A (1 Mbit)0011
ST Microelectronics- M25P05A (512 kbit) 0100
   M25P10A (1 Mbit) 0101
   M25P20 (2 Mbit) 0101
Chingis (formerly PMC) -
   Pm25LV512 (512 kbit) 0100
   Pm25LV010 (1 Mbit) 0101

If BIOS_ROM_EN = 0, then Config[2:0]
defines the primary memory aperture size.
(Config 3 = don   care).
x000 128MB
x001 256MB
x010 64MB
x011 32MB
x100 512MB
x101 1GB
x110 2GB
x111 4GB

PSYNC   PSYNC   [3]
DVALID   DVALID   [3]

GENERICB   GENERICB   [3]
GENERICC   GENERICC   [3]

MR65 10K   DNI R65 10K   GENERICC

MR64 10K   DNI R64 10K   GENERICB

GENERICC, GENERICB - ATI Internal Use Only - Reserved (Default: 0)

MR66 10K   R66 10K   A_VSYNC_DAC1   A_VSYNC_DAC1 [3,13]

VSYNC - VIP_DEVICE_STRAP_EN
 0: Slave VIP host port devices present (use if Theater is populated)
 1: No slave VIP host port devices reporting presence during reset (use for
 configurations without video-in)

MR67 10K   R67 10K   A_HSYNC_DAC1   A_HSYNC_DAC1 [3,13]

HSYNC - ATI Internal Use Only - Reserved (Default 0)

MR68 10K   DNI R68 10K   PSYNC

PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)

MR69 10K   DNI R69 10K   GPIO21_BB_EN   GPIO21_BB_EN [3]

GPIO_21 - ATI Internal Use Only - Reserved (Default: 0)

MR70 10K   DNI R70 10K   VID_0

VID_0 - ATI Internal Use Only - Reserved (Default: 0)

MR71 10K   DNI R71 10K   VID_1

VID_1 - MSI_DIS (Default: 0)

MR72 10K   DNI R72 10K   VID_2

VID_2 - ATI Internal Use Only - Reserved (Default: 0)

MR73 10K   DNI R73 10K   VID_3

VID_3 - BIF_AUDIO_EN
0 - Disable HD Audio 1- Enable HD Audio

MR74 10K   DNI R74 10K   VID_4

VID_4 - ATI Internal Use Only - Reserved (Default: 0)

MR75 10K   DNI R75 10K   VID_5

VID_5 - 64BAR_EN_A (Default: 0)
   Enable 64-bit BARS

MR76 10K   DNI R76 10K   VID_6

VID_6:7 - ATI Internal Use Only - Reserved (Default: 00)

MR77 10K   DNI R77 10K   VID_7

MR80 10K   R80 10K   A_VSYNC_DAC2   A_VSYNC_DAC2 [3]

VSYNC - MEMORY CONFIG   ATI Board Feature I
   0 = single rank memory, 1 = dual rank memory

MR79 10K   DNI R79 10K   A_HSYNC_DAC2   A_HSYNC_DAC2 [3]

HSYNC2 - ATI Internal Use Only - Reserved (Default: 0)

MR60 10K   DNI R60 10K   DVALID

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

MR87 10K   DNI R87 10K   PWRCNTL_0   [3]

GPIO_15 - FOR FUTURE EXPANSION

MR46 10K   DNI   GPIO_22   GPIO_22   [3]

GPIO_22_ROMCSb - Enable external BIOS ROM device (Default 1)

MR88 10K   DNI   R88 10K   GPIO_18   [3]

GPIO_18 - MEMORY CONFIG BANK SELECT
0 - 4 BANKS, 1 - 8 BANKS

[3] VID_[7..0]

VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
VID_7

[3] GPIO_[13..0]

GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space
and to prevent assembly of
both resistors.

Layout

Ground   High logic voltage

Signal

TMDS_2(Daul_Link) + DAC_1-CRT

Optional ESD Protection Diodes

Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)

+3.3V +3.3V +3.3V

BAT54SLT1 ED62   BAT54SLT1 ED63   BAT54SLT1 ED64

+5V   +5V_VESA

EF1
0.2A

[3] A_R_DAC1
[3] A_RB_DAC1
[3] A_G_DAC1
[3] A_GB_DAC1
[3] A_B_DAC1
[3] A_BB_DAC1

L1001 47nH   A_R_DAC1_M   L1004 47nH
L1002 47nH   A_G_DAC1_M   L1005 47nH
L1003 47nH   A_B_DAC1_M   L1006 47nH

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F

DDCDATA_DAC1_R
DDCCLK_DAC1_R
A_HSYNC_DAC1_R
A_VSYNC_DAC1_R

MJ1001
1 R
2 G
3 B
11 MS0   DDC2_MONID0
12 MS1   DDC2_MONID1(SDA)
4 MS2   DDC2_MONID2
15 MS3   DDC2_MONID3(SCL)
9 NC
13 HS
14 VS
6 VSS
7 VSS#6
8 VSS#7
9 VSS#8
10 VSS#10
17 CASE
CASE#17
G3179C219-005

SLIM VGA

R1029 75R R1040 75R R1028 75R R1041 75R R1027 75R R1042 75R
R1002 75R R1002 75R R1001 75R

C1004 3.3pF C1005 3.3pF C1006 3.3pF
C1001 8.0pF C1002 8.0pF C1003 8.0pF

C1010 100nF

Place close to Connector
SHOULD BE A LOW INDUCTANCE PATH TO PIN 5

+5V +5V +5V +5V
BAT54SLT1 ED65 BAT54SLT1 ED66 BAT54SLT1 ED67 BAT54SLT1 ED68

+3.3V +5V
R1004 24.3K R1005 19.1K
[3] CRT1DDCDATA
BSH111 Q1001   DDCDATA_DAC1_5V   R1006 33R   DDCDATA_DAC1_R

+3.3V +5V
R1007 24.3K R1008 19.1K
[3] CRT1DDCCLK
BSH111 Q1002   DDCCLK_DAC1_5V   R1009 33R   DDCCLK_DAC1_R

C1999 100nF   +5V
[3,12] A_HSYNC_DAC1
U1999A SN74HCT125D   A_HSYNC_DAC1_B   R1010 33R   A_HSYNC_DAC1_R

SN74HCT125D U1999B
[3,12] A_VSYNC_DAC1   A_VSYNC_DAC1_B   R1011 33R   A_VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	SCL	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V	+5V	+5V	Optional
Hardware Support	Mechanical Key	50mA min 1A max	50mA min 1A max	300mA min 1A max	Optional
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

+5V_VESA

J1001
25 CASE
1 TMDS Data2-
2 TMDS Data2+
3 TMDS Data2/4 Shield
4 TMDS Data4-
5 TMDS Data4+
6 DDC Clock
7 DDC Data
8 Analog VSYNC
10 TMDS Data1-
11 TMDS Data1+
12 TMDS Data1/3 Shield
13 TMDS Data3-
14 TMDS Data3+
15 +5V Power
16 GND (for +5V)
17 Hot Plug Detect
18 TMDS Data0-
19 TMDS Data0+
20 TMDS Data0/5 Shield
21 TMDS Data5-
22 TMDS Data5+
23 TMDS Clock Shield
24 TMDS Clock+
TMDS Clock-

C1 Analog Red
C2 Analog Green
C3 Analog Blue
C4 Analog HYNC
C5 Analog GND
C6 Analog GND#C6

26 CASE#26
27 CASE#27
28 CASE#28
29 CASE#29
30 CASE#30

DVI_CONNECTOR

[3] TjX2M
[3] TjX2P
[3] TjX4M
[3] TjX4P
DDCCLK_DAC1_R
DDCDATA_DAC1_R
A_VSYNC_DAC1_R
[3] TjX1M
[3] TjX1P
[3] TjX3M
[3] TjX3P
[3] TjX0M
[3] TjX0P
[3] TjX5M
[3] TjX5P
[3] TjXCP
[3] TjXCM
A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
A_HSYNC_DAC1_R

+3.3V
Q1021 MMBT3904   R1022 10K
HPD_DVI1
R1023 10K

[3] HPD1

Title: RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI

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TMDS_1(Single_Link) + DAC_2-CRT

Title
RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI

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[3] DAC2_Y

L3001 470nH_250mA
DAC2_Y_F

R3001 75R
C3001 47pF_50V
C3004 47pF_50V

[3] DAC2_C

L3002 470nH_250mA
DAC2_C_F

R3002 75R
C3002 47pF_50V
C3005 47pF_50V

[3] DAC2_COMP

L3003 470nH_250mA
DAC2_COMP_F

R3003 75R
C3003 47pF_50V
C3006 47pF_50V

+3.3V   +3.3V   +3.3V

BAT54SLT1 ED78   BAT54SLT1 ED77   BAT54SLT1 ED76

+3.3V
R3008 10K

TV Out

Component (Y)
Component (Pr)
Component (Pb)

[3] GENERICA_R   STV/HDTV#_DET
R3009   0R
40?

J3001
PIN6   6   HDTV_OUT_DET#

DAC2_Y_F   40?   DAC2_Y_DIN   3   Y-OUT
DAC2_C_F   40?   DAC2_C_DIN   4   C-OUT
DAC2_COMP_F 40?   DAC2_COMP_DIN 7   Comp_out
                                 5   SYNC
                                 1   GND
                                 2   GND#2
Rpin5   8   CASE
                                 9   CASE#9
                                 10 CASE#10
Conn_DIN_Mini_Circular_7_Pin_with_O_Ring

Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

H2

HEATSINK

MT1
MT_Hole_0.136_in.

+12V_BUS

B31
Bead

C4008
100nF
603
X7R
5%

4Ω2

JU1
1
2
JUI2

DUAL FOOTPRINT

JUI1

MJU1
1
2
3
Header_1X3

80200439A0G (DVI+HDMI+DIN)

H3A

RV610_FANSINK

H3B

RV610_FANSINK

H3C

RV610_FANSINK

H3D

RV610_FANSINK

Title
RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI

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ASSY3
BRACKET
8020040100G

FM1
SW_FB

FM5
SW_FB

FM2
SW_FB

FM6
SW_FB

FM3
SW_FB

FM4
SW_FB

<Variant Name>

ATI

Title	Schematic No.	Date:
RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA+DVI) 109-B76909xx-00A		**Friday, June 29, 2007**

REVISION HISTORY	NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact ATI representative to obtain latest BOM closest to the application desired.	Rev 32

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
		2006.12.01	UPDATE SCHEM. BOM MANAGEMENT.
		2006.12.14	UPDATE SCHEMATIC TO NETLIST WITH NO ERRORS
		2006.12.18	DORINA UPDATE MEM SWAP
		2006.12.19	REMOVE TP ON MEM - TO BE REPLCED BY 0.8MM PADS ON ALL LINES
		2006.12.20	CHANGED B67 to PN 5260014800G AND C76 to PN 4172010500G
0	00A	2006.12.21	J2 REMOVED
		2007.01.15	NC626 removed (VDDC output cap). LDO output resistor (R879, R880) moved closer to LDO. MVDD LDO input resistors changed to 1R. Debug header changed to include Gen1/2 switch. HDMI caps removed. Added thermal shutdown option to power sequencing.
		2007.01.16	REMOVE BACK BIAS, REMOVE MC624
		2007.01.17	REMOVE R5515, R5516, R5521, R5524 REMOVE R94
		2007.01.22	ADDED H3, H4, H5
		2007.01.22	DECAP CHANGES ON PAGE 3
		2007.01.23	HEATSINK GROUNDING ADJUSTED
		2007.01.23	DORINA - HEATSINK GNDING PINS ADJUSTED
		2007.01.24	RM JTAG + SMA CLOCK CONNECTIONS TO EASE LAYOUT CONGESTION
		2007.01.24	ADDED C300, C301, C302 (STITCHING CAPS) TO IMPROVE DDC LINES
		2007.01.24	FIXED ORCAD NETLIST PROBLEM; NO EFFECTIVE CHANGE.
		2007.01.24	ADD Q102 TO SOLVE A11 VDDR3 LEAKAGE PROBLEM.
1	00B	2007.01.25	CHNG REF DES OF VDDR3 LEAKAGE BLOCK TO Q/R-90
2	00C	2007.02.09	PCB mechanical updates only. No Schematic changes.

DDR2 32Mx16

DDR2 32Mx16

External TMDS

POWER REGULATION

From +12V
VDDC, MVDD

From +12V LINEAR:
+5V, +5V_VESA,
+5V_VESA2, RageTheater

From +12V DIRECT:
FAN

From +3.3V LINEAR:
VDDC_CT, MPVDD, PVDD,
TPVDD, T2PVDD, TXVDDR,
T2XVDDR, AVDD, A2VDD,
VDD1DI, VDD2DI,
PCIE, VDDR3, VDDR4,
VDDR5, VDDRH
MVDD

Straps

BIOS

FAN

Speed control & temperature sense

INTERRUPT

Temp. Sensing

MEM A   MEM B

Dual-Link LVTM

GPIO14

DAC2
CRT
H/V2Sync
DDC2

TVO

XTALIN/OUT

MPP

VIP

DAC1
CRT
H/VSync
DDC1

Dual-Link TMDS

HPD1

PCI-Express

GPIO

ROM

DDC3
GPIO17

D+/D-

RV610

TMDS matching

RBG Filters

TVO Filters

XTAL   Oscillator

XTALIN/OUT
CLKOUT

RageTheater

RBG Filters

TMDS matching

DVI-I
&
Slim-VGA
CONN
HPD

TVO/VIVO
CONN

DVI-I
&
Slim-VGA
CONN
HPD

+PCIE_SOURCE
+3.3V   +12V_BUS

POWER DELIVERY

3.3V_BUS
delayed circuit

SMPS Enable
Circuit

+3.3V_BUS
+12V_BUS

PCI-Express Bus

RV610 DDR2 FH 4-Layer

REV 0