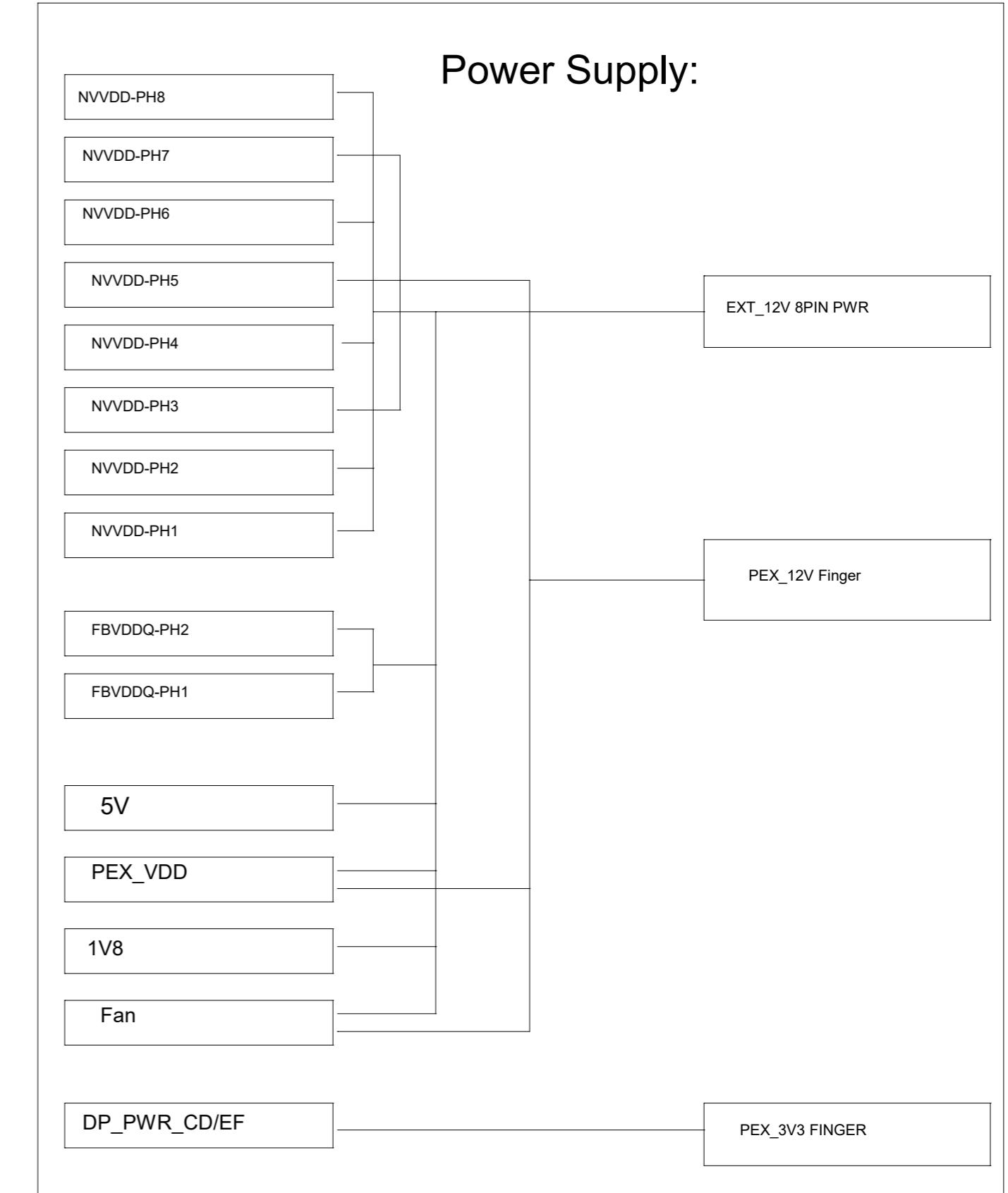
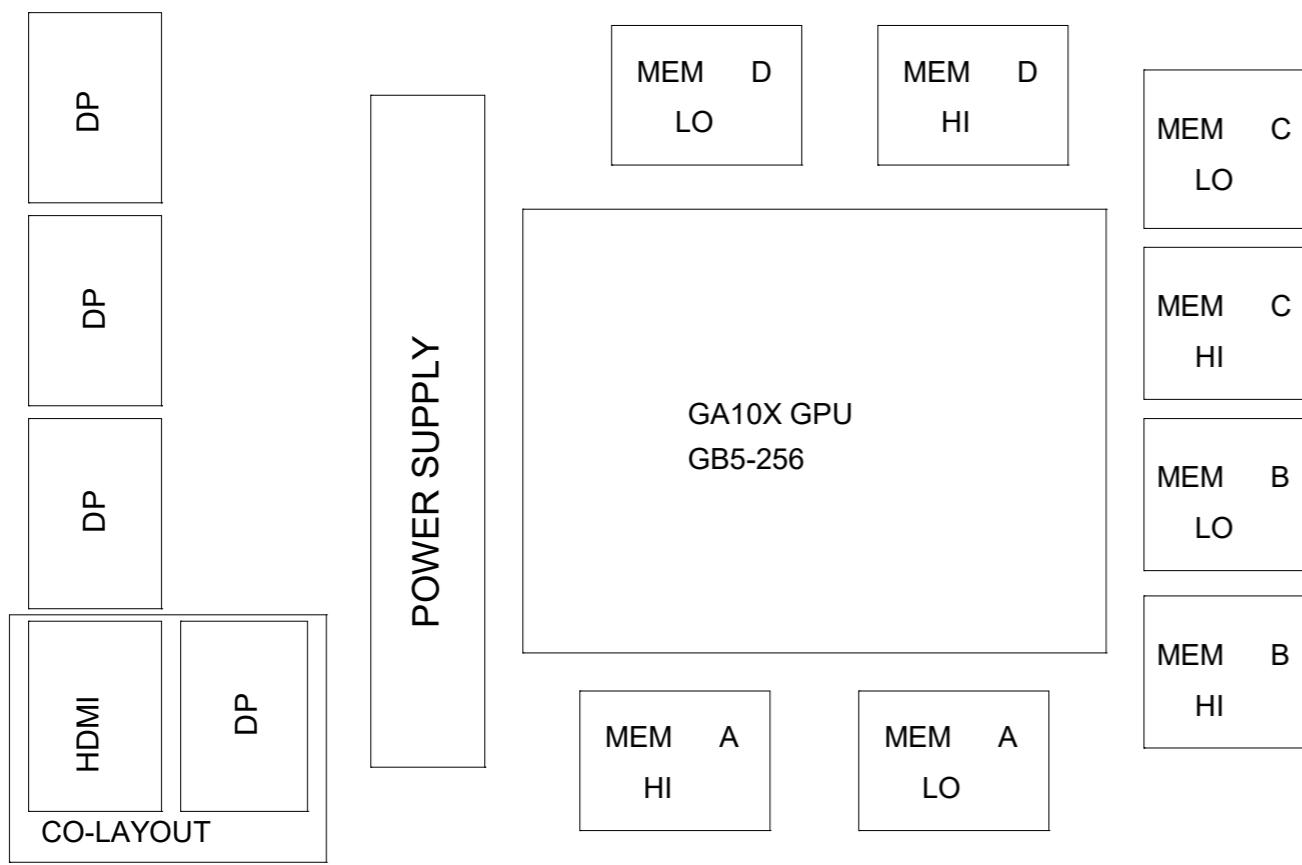


GA104/GA106 GB5256
DP + DP + DP + HDMI/DP

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Power Supply:



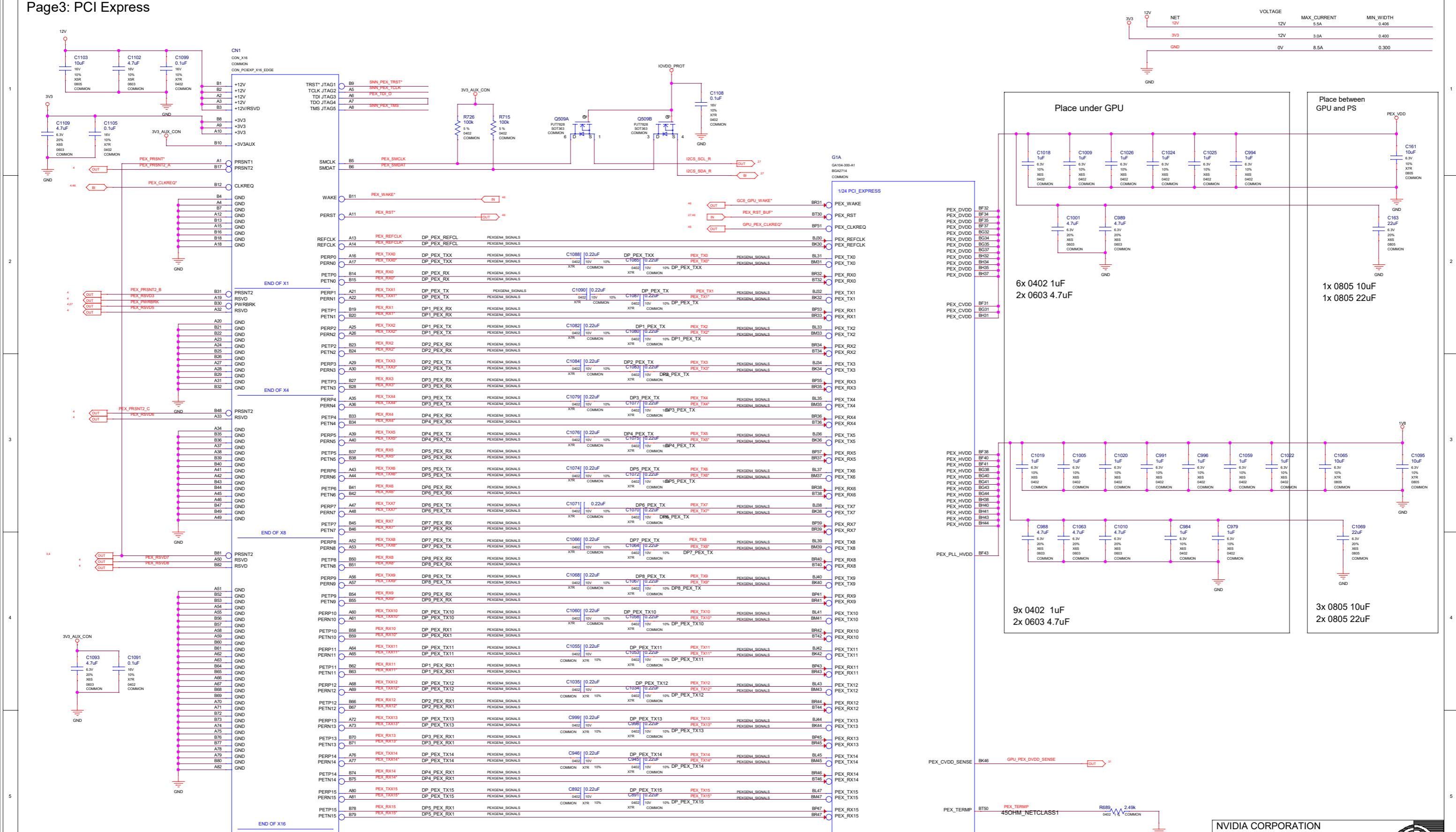
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Page3: PCI Express



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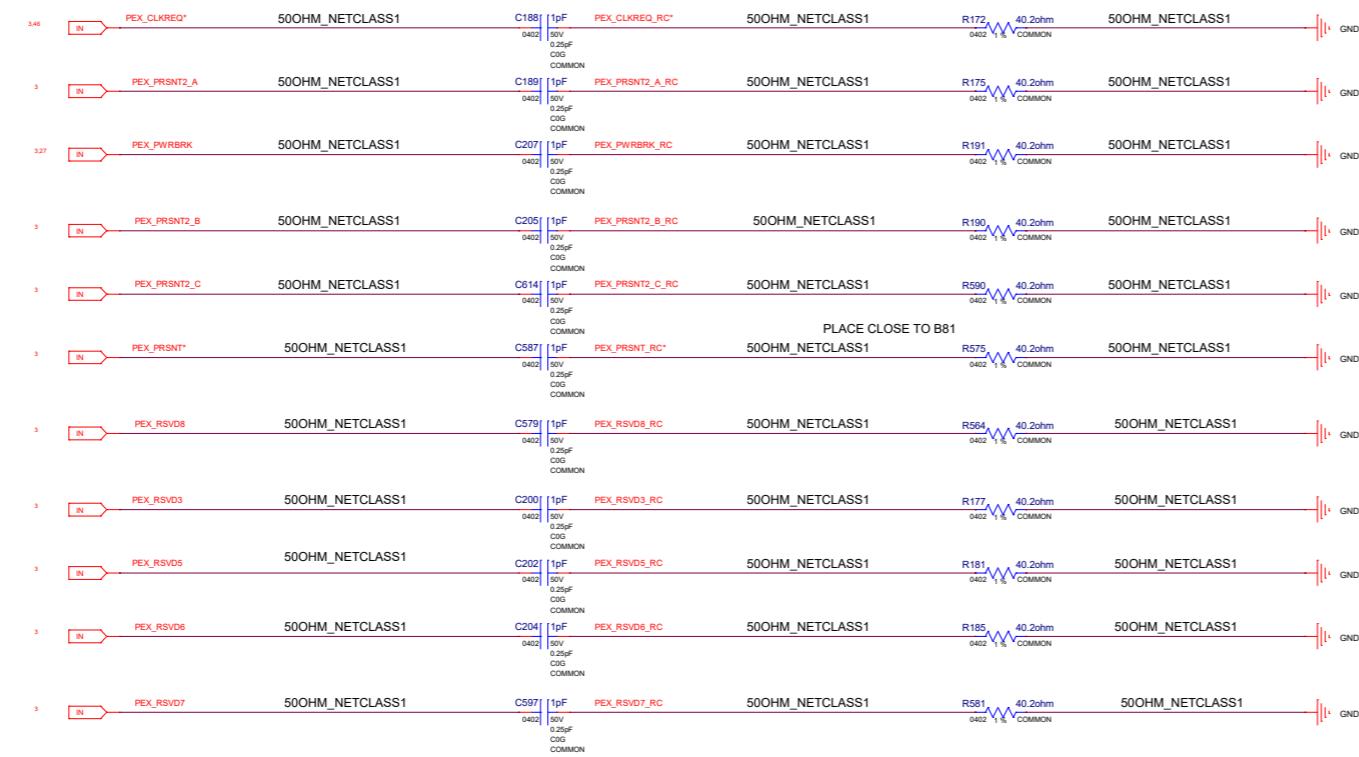
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCIe GEN4 RC Termination

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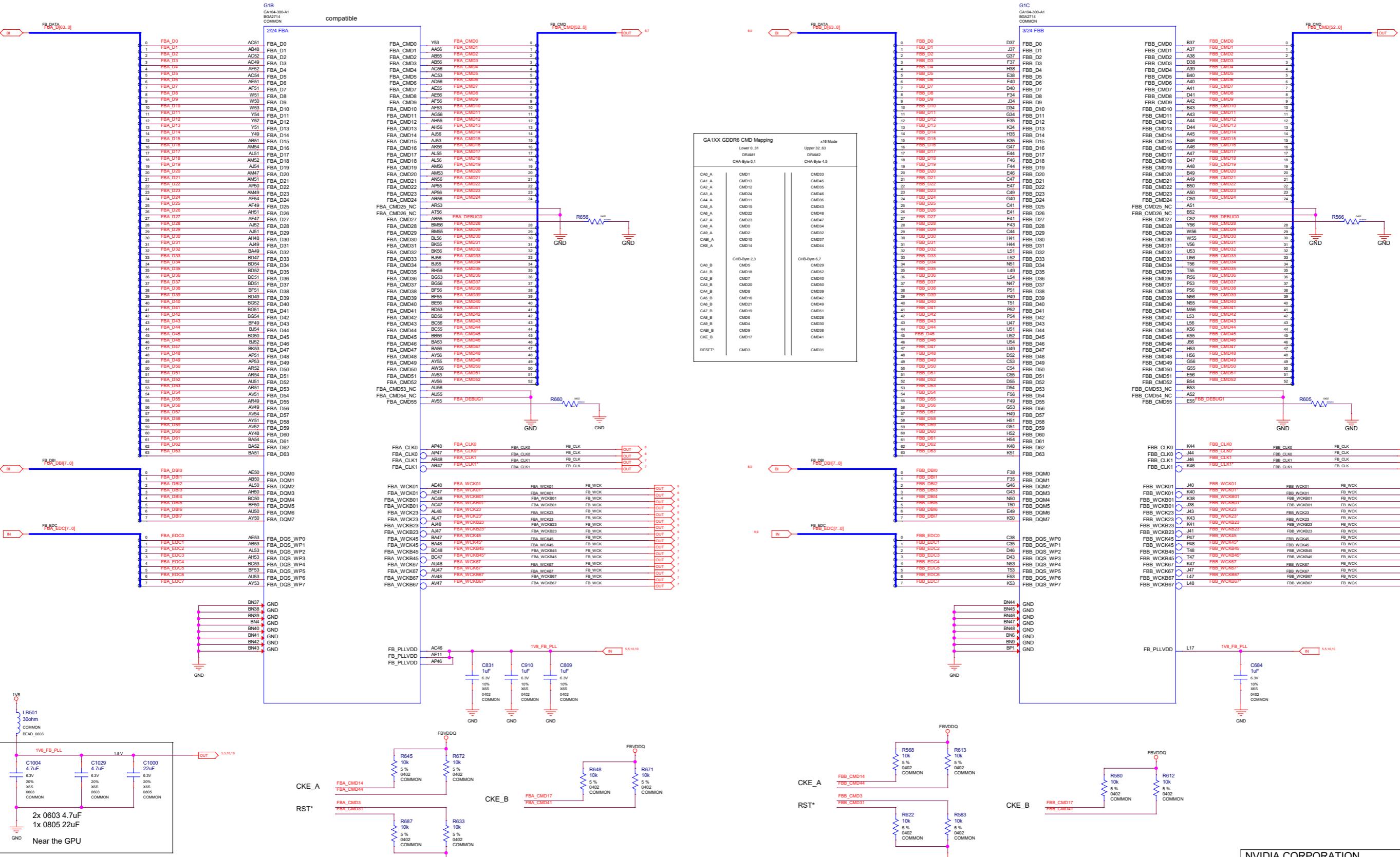
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Page5: MEMORY: GPU Partition A/B

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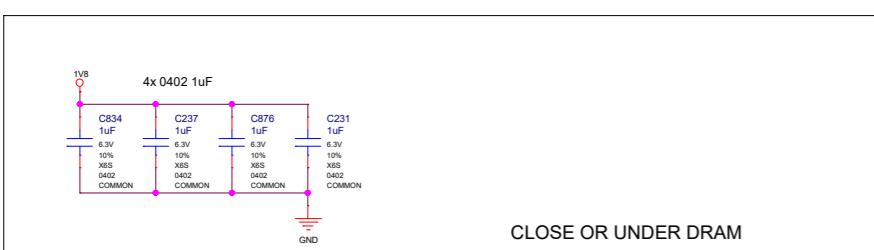
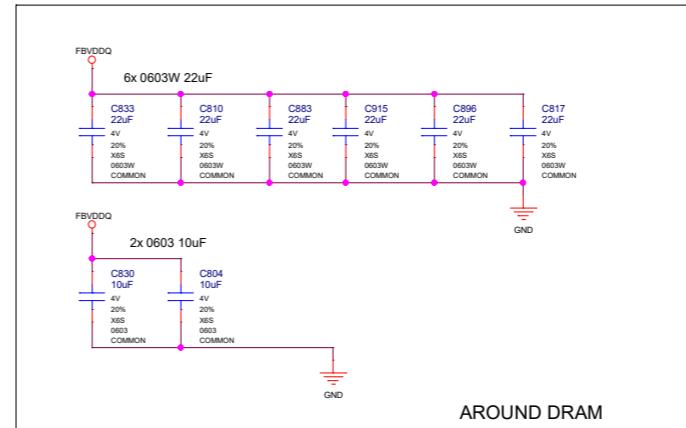
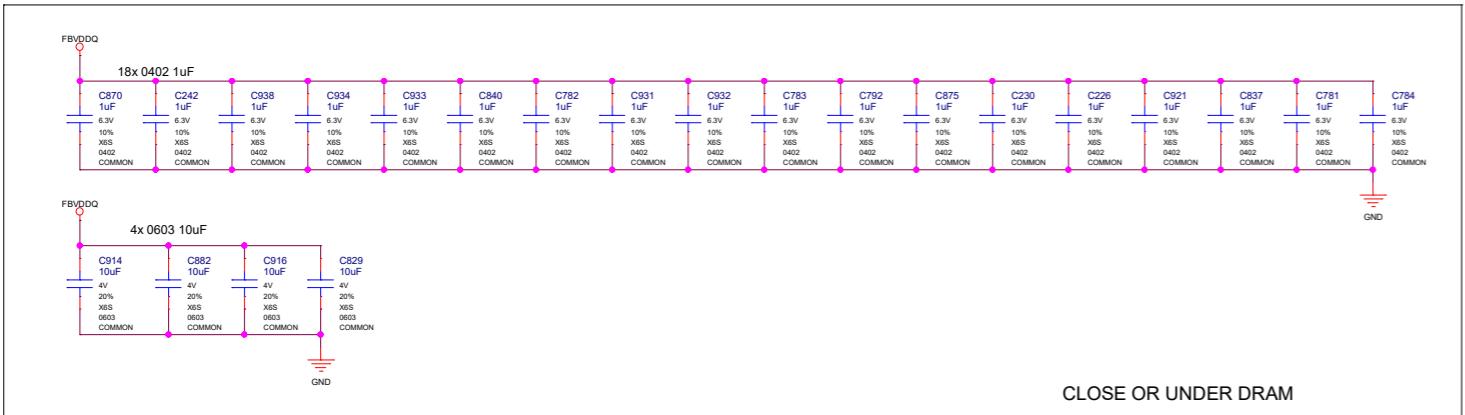
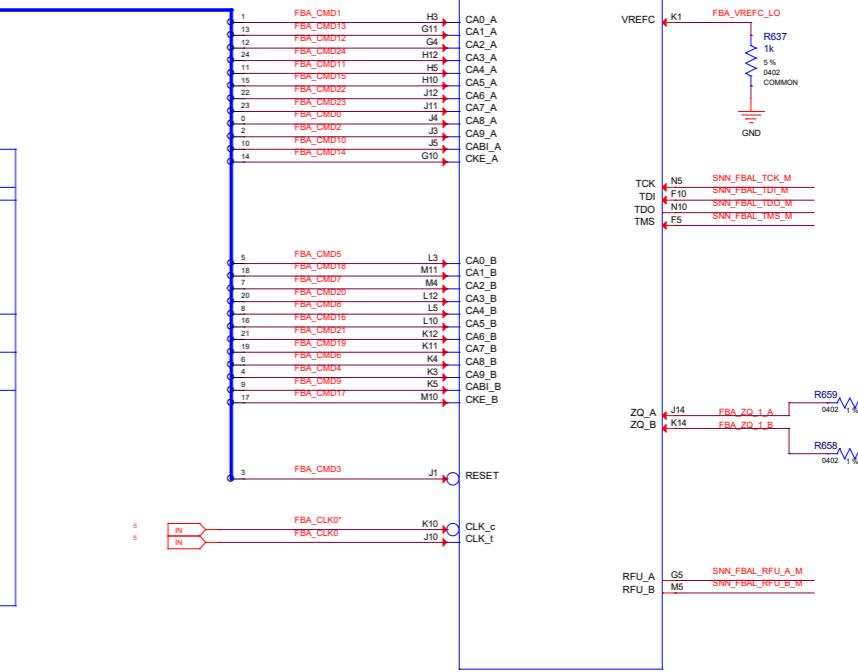
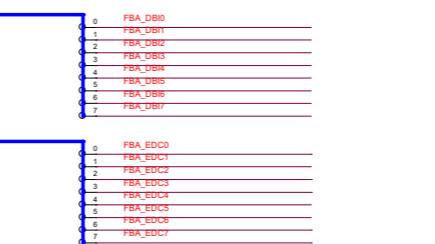
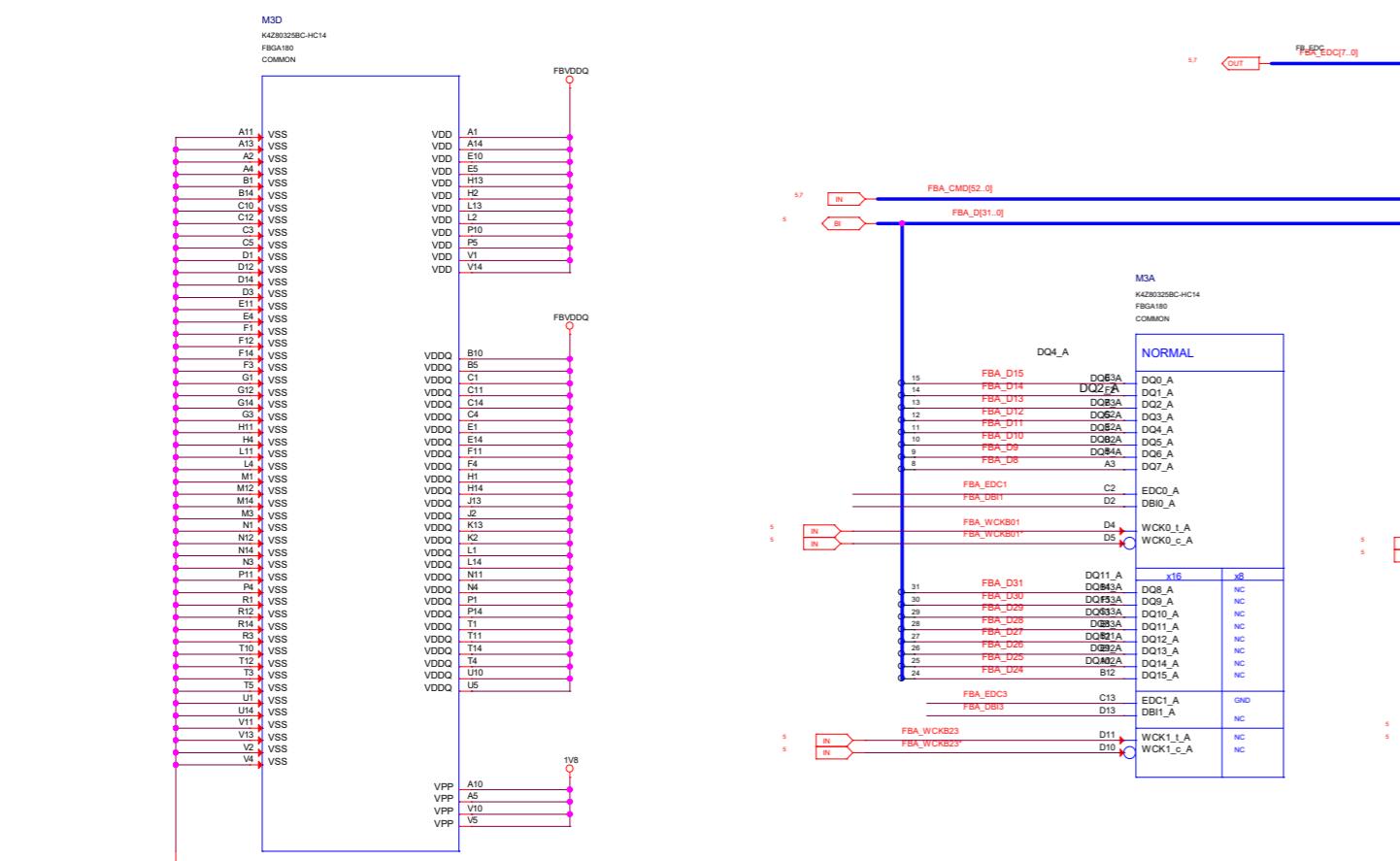
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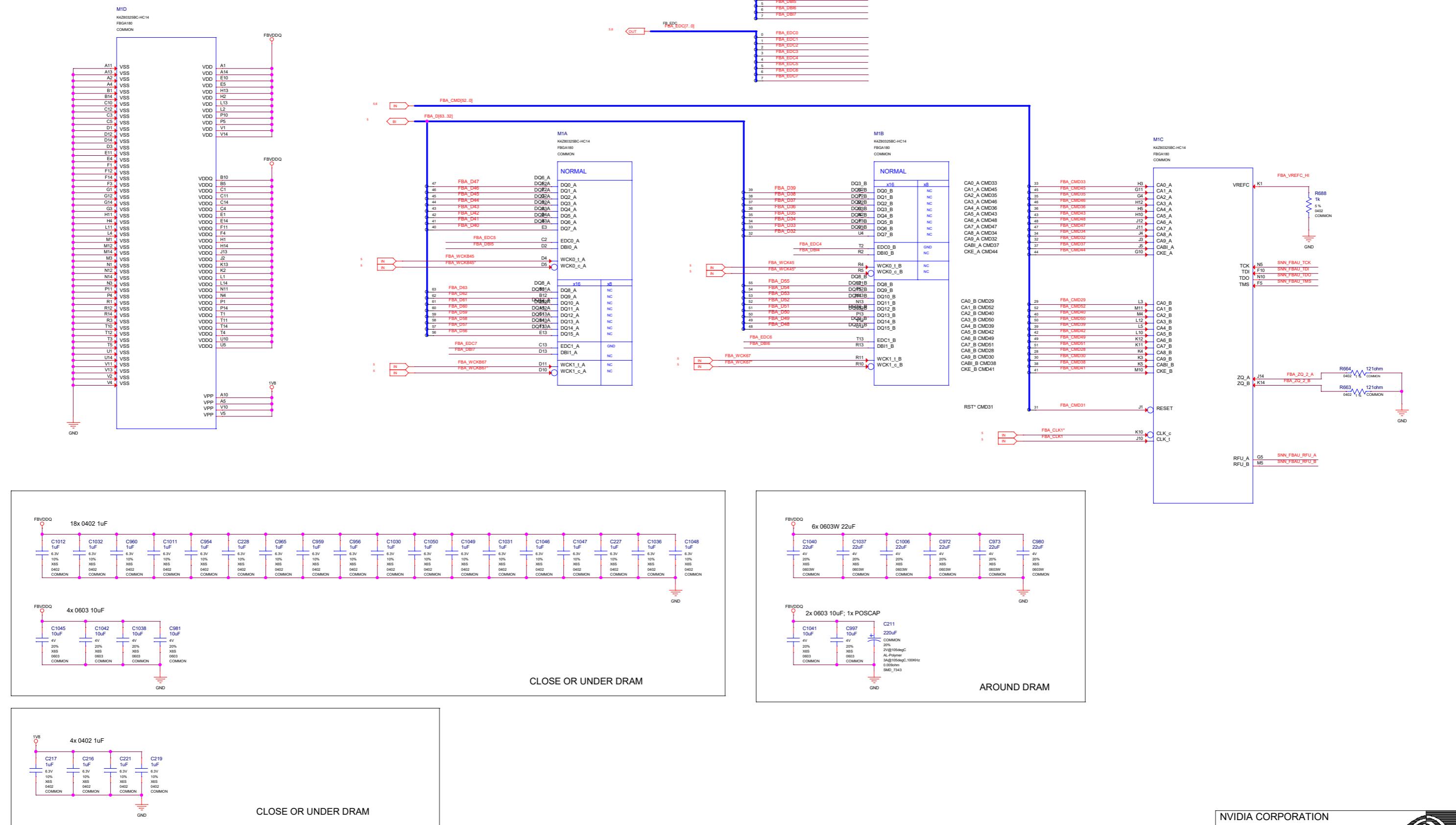
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Page7: MEMORY: FBA Partition 63..32



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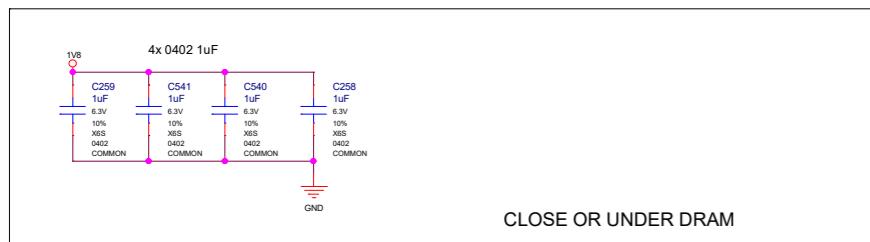
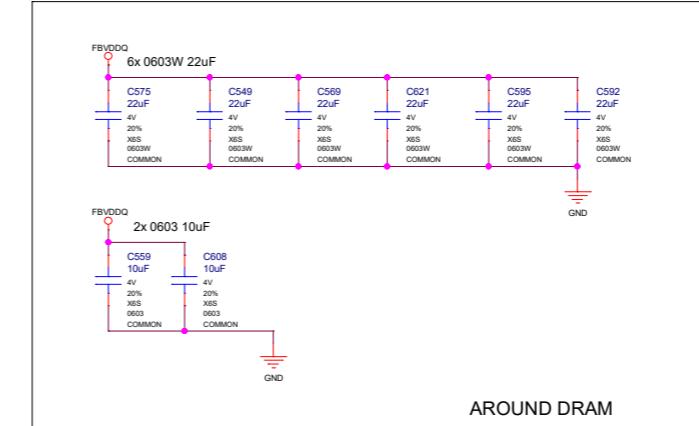
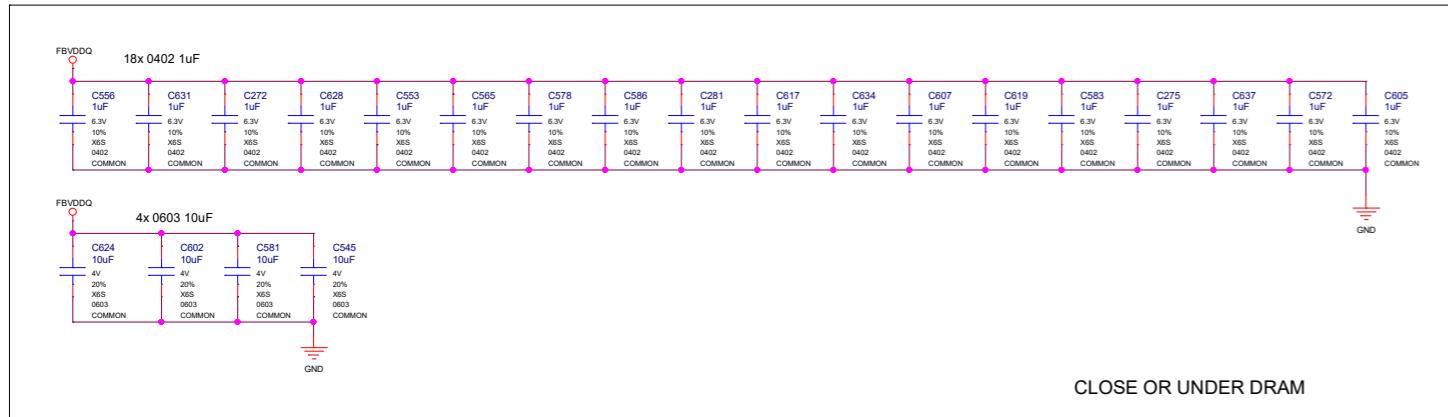
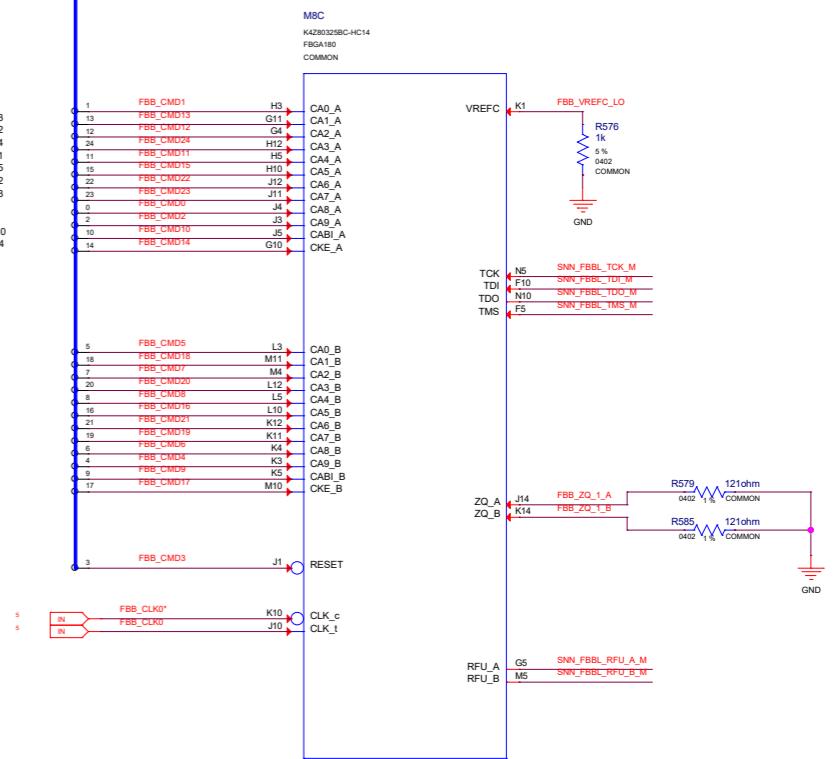
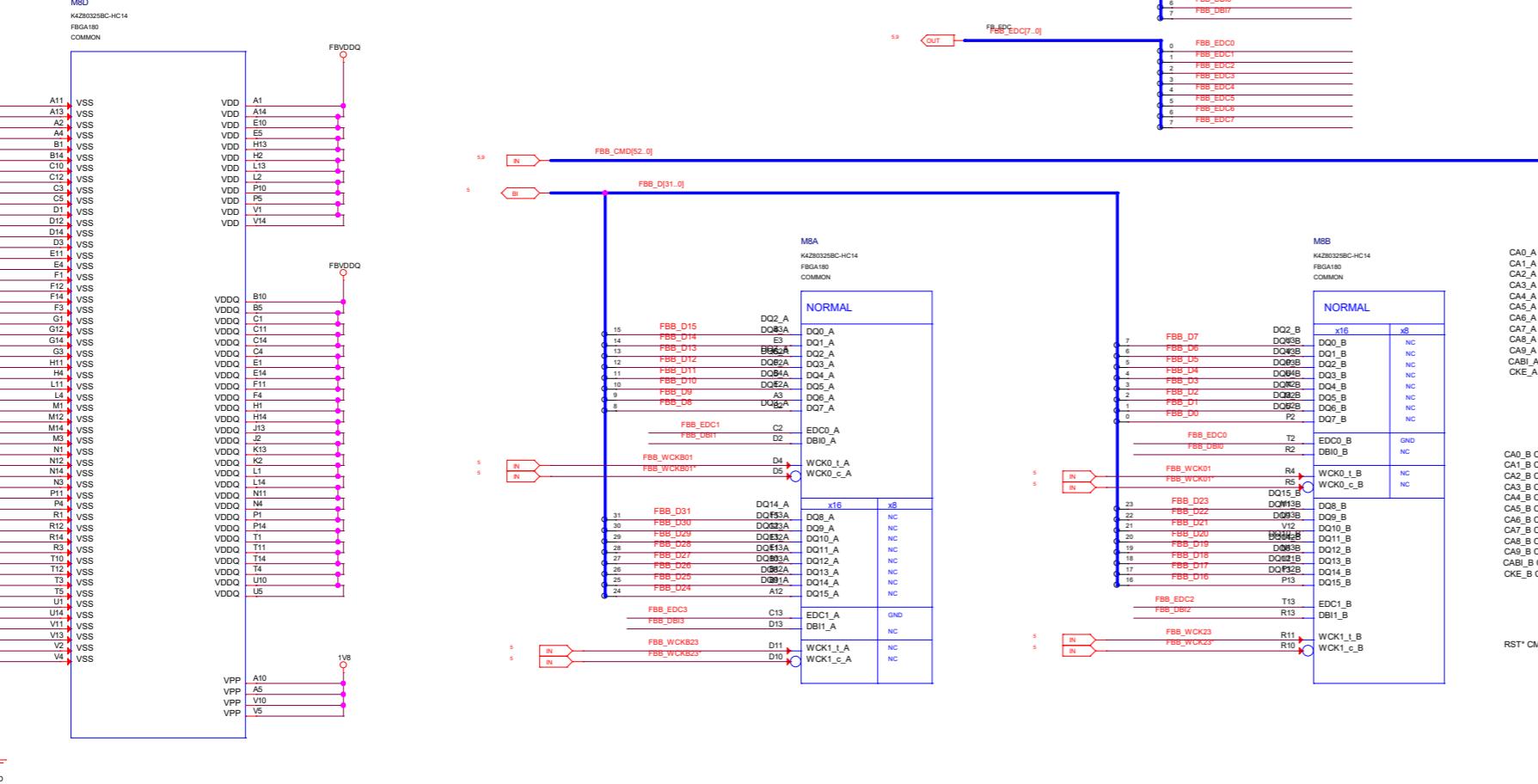
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Page8: MEMORY: FBB Partition 31..0



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PAGE DETAIL

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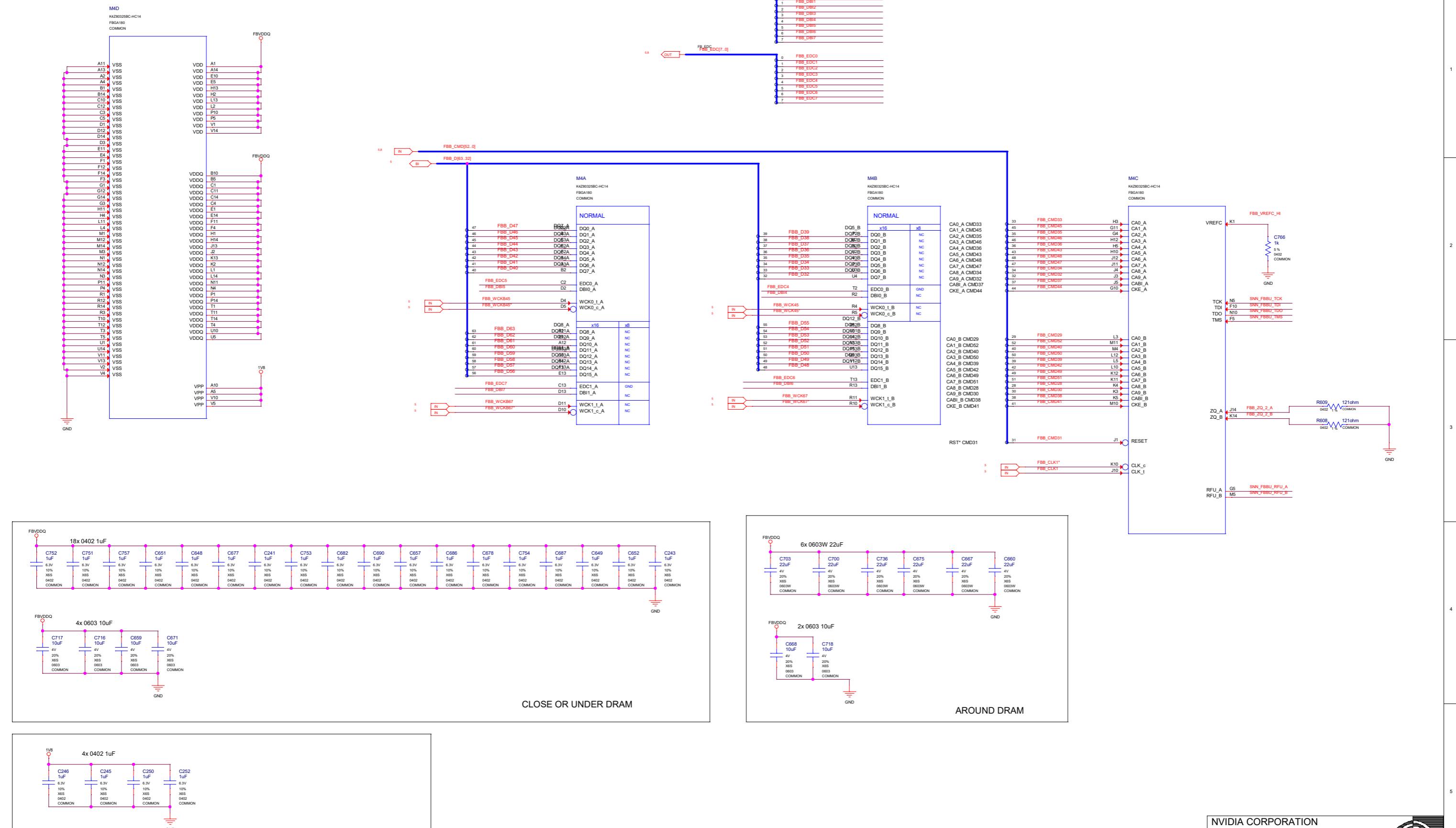
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Table 1. Summary of the main characteristics of the four groups of patients.

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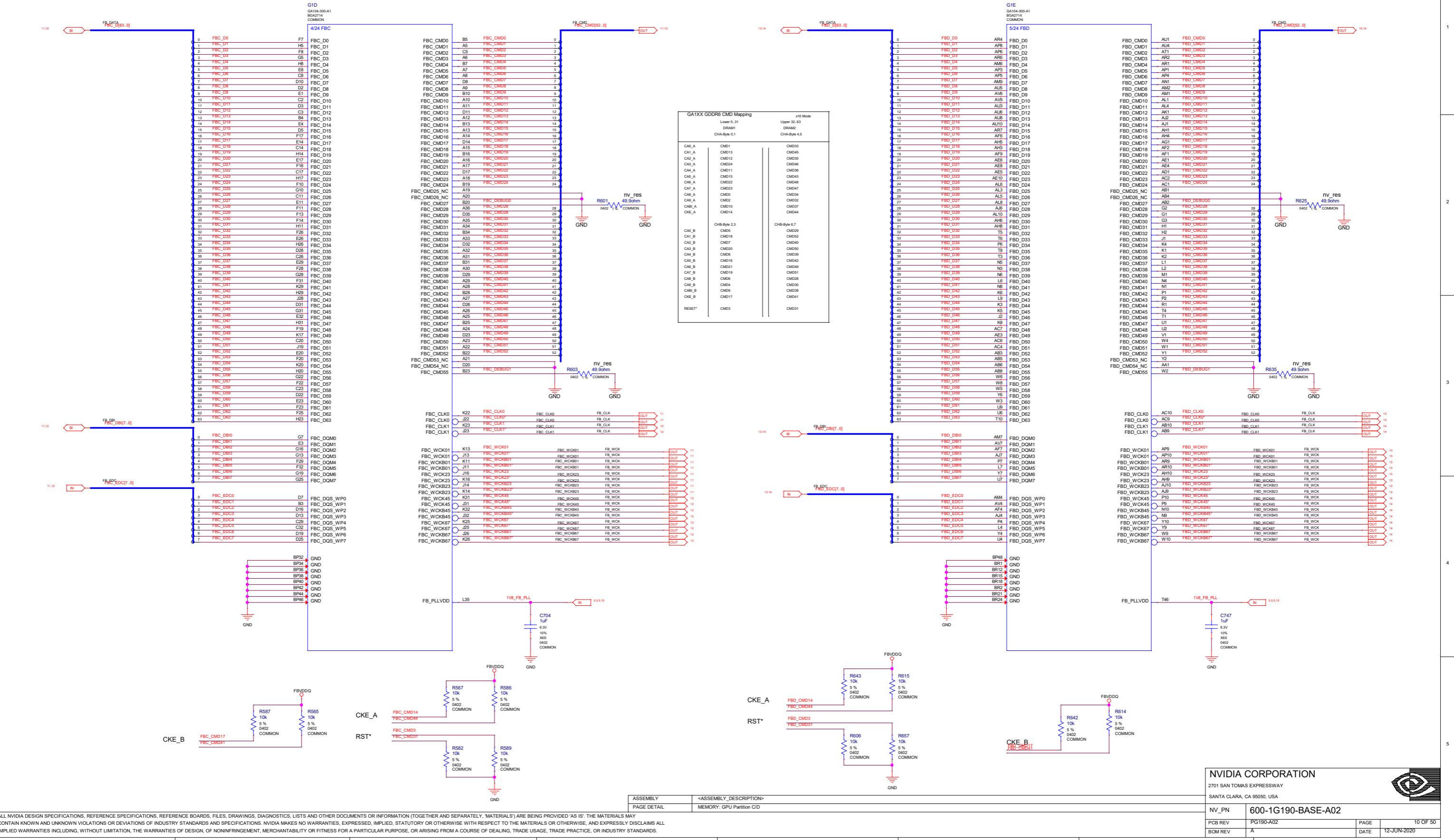
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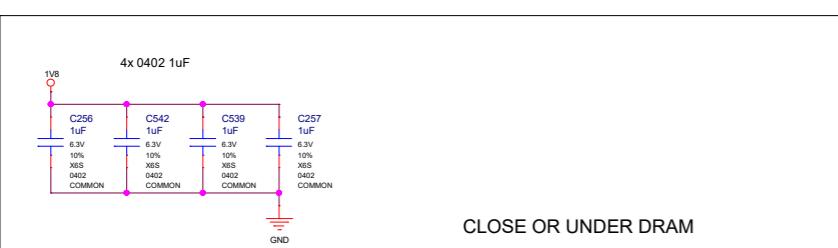
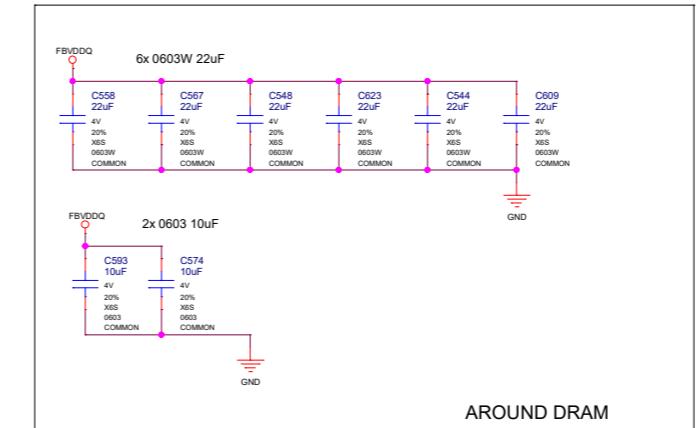
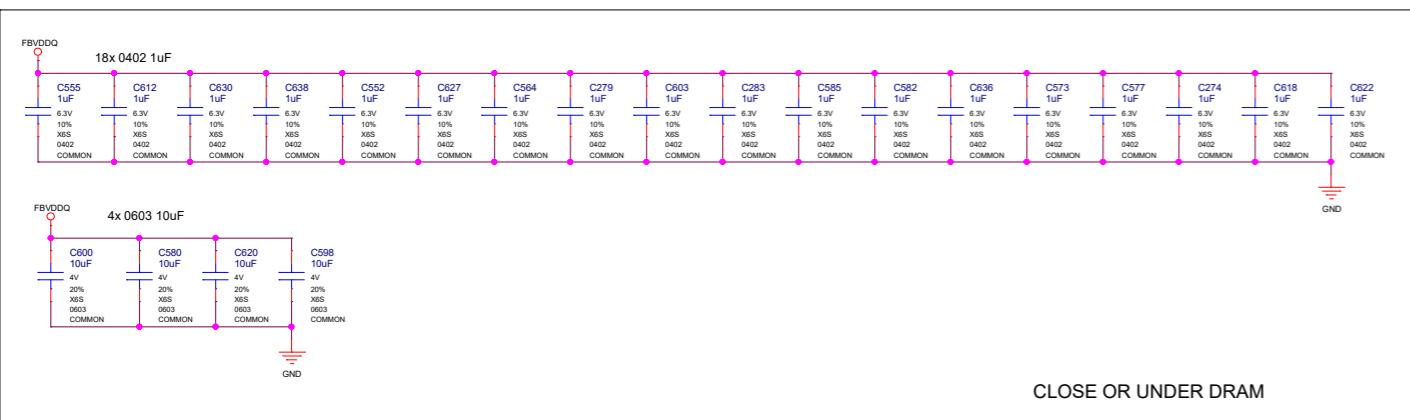
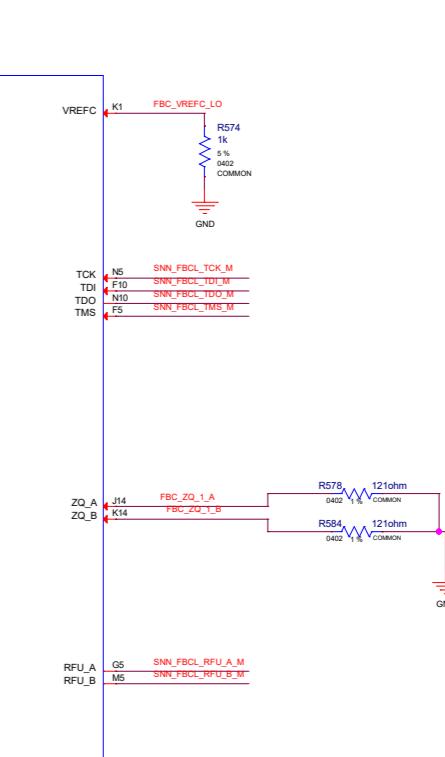
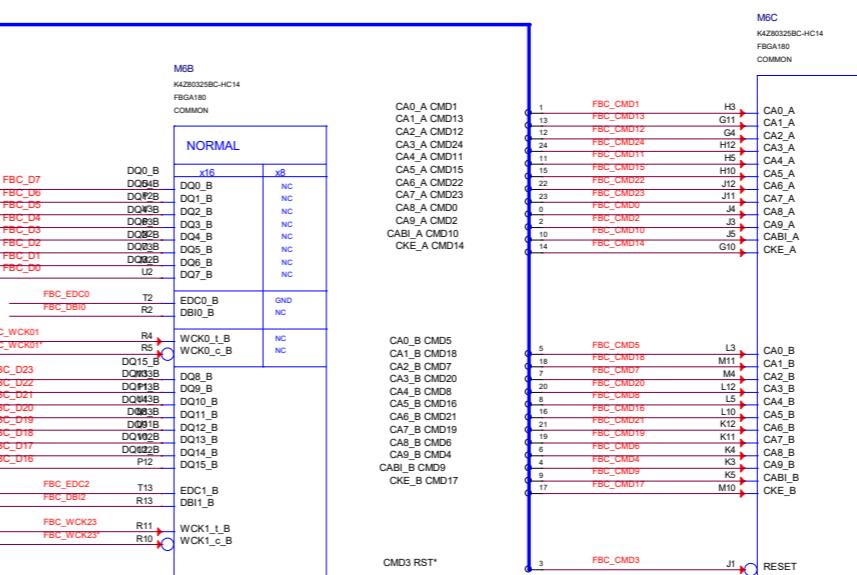
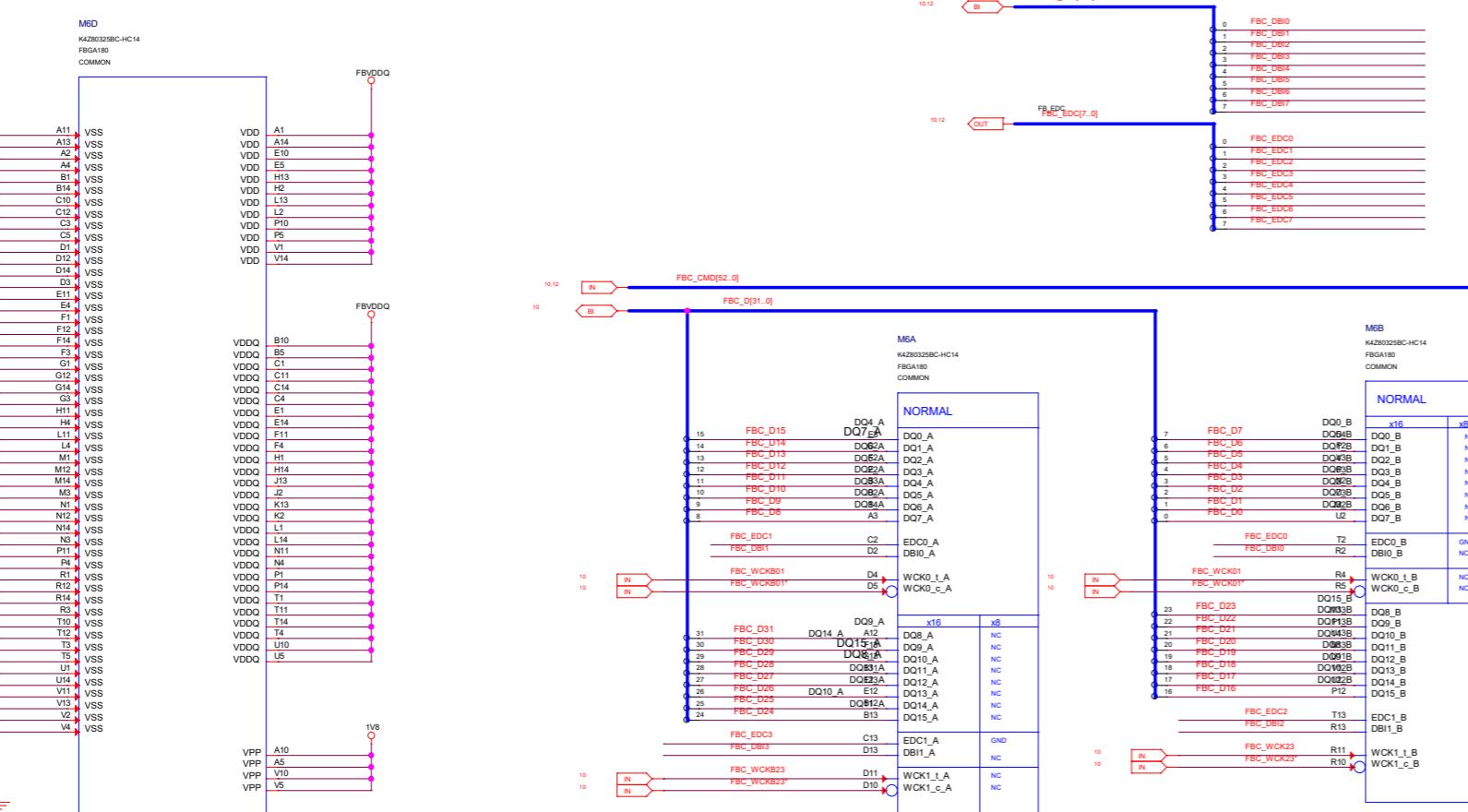
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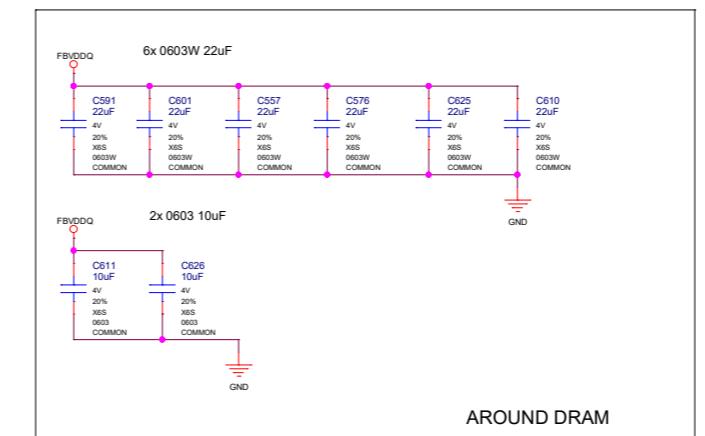
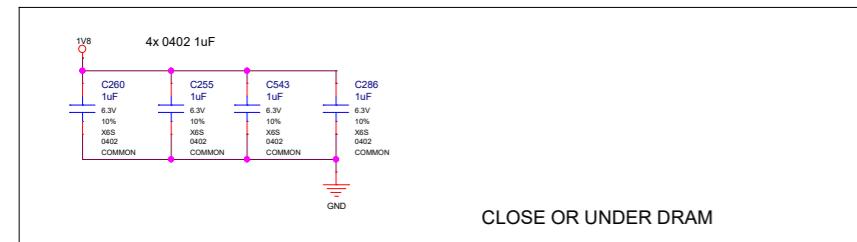
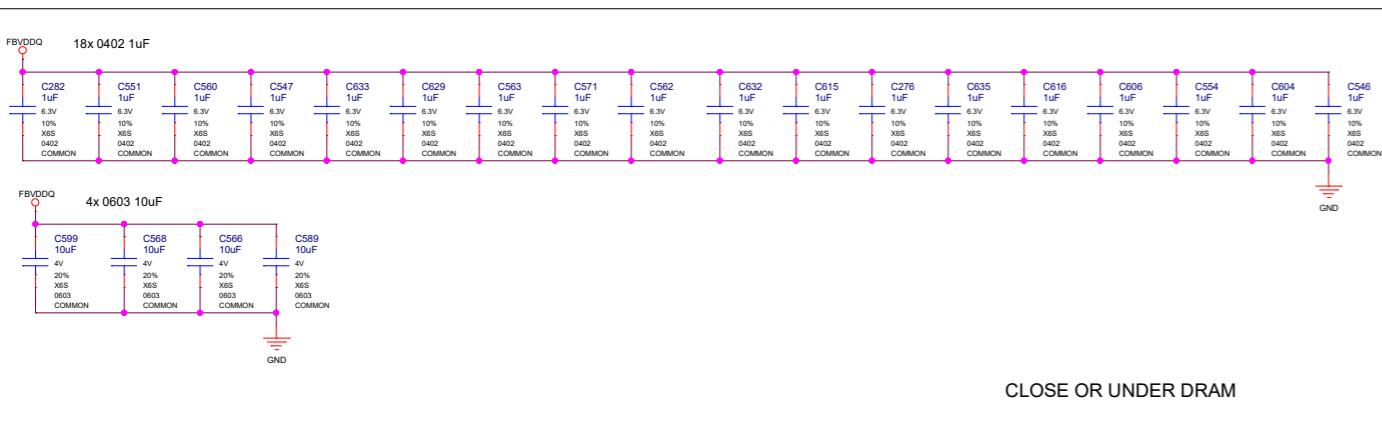
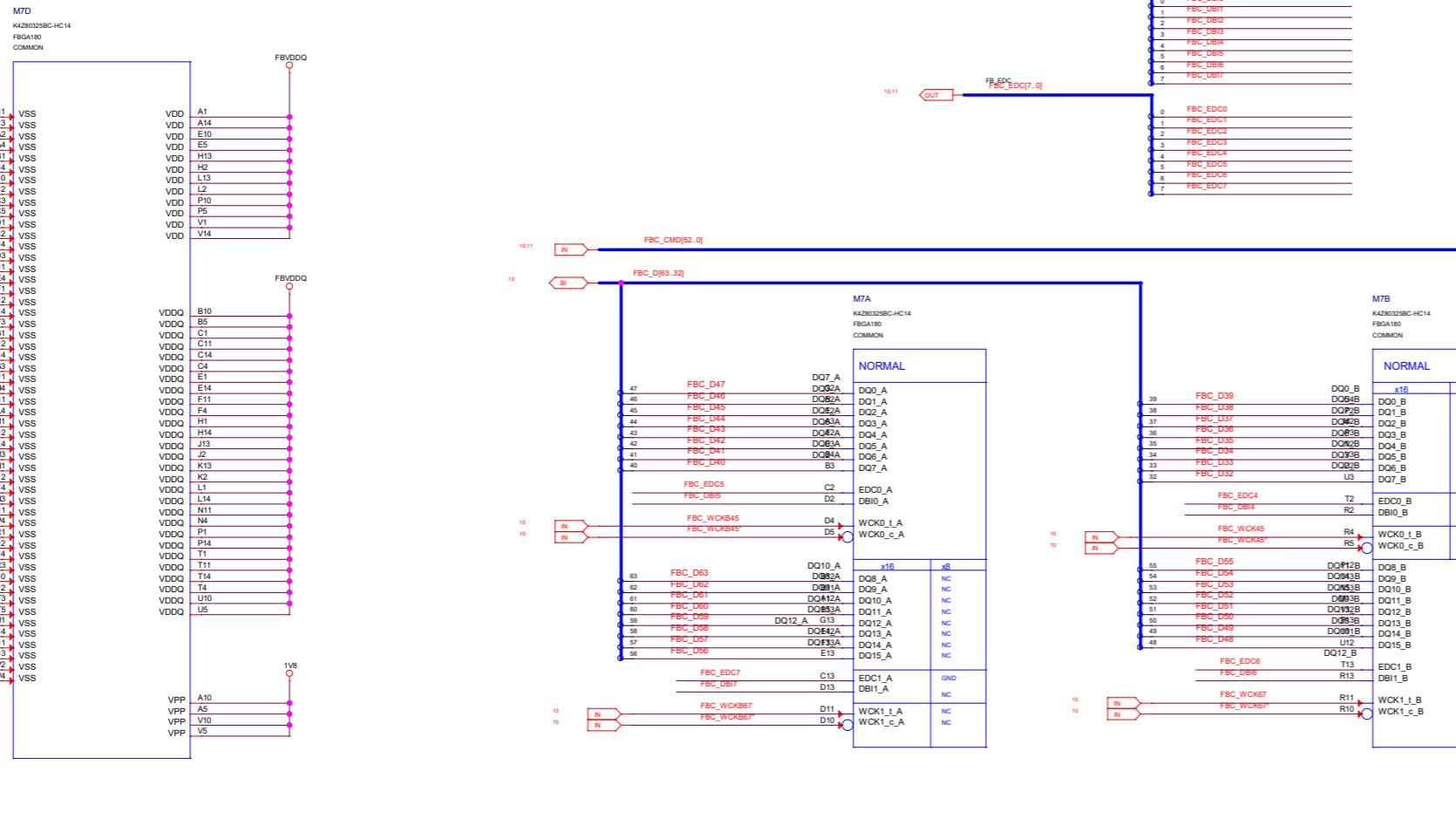
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Page12: MEMORY: FBC Partition 63..32



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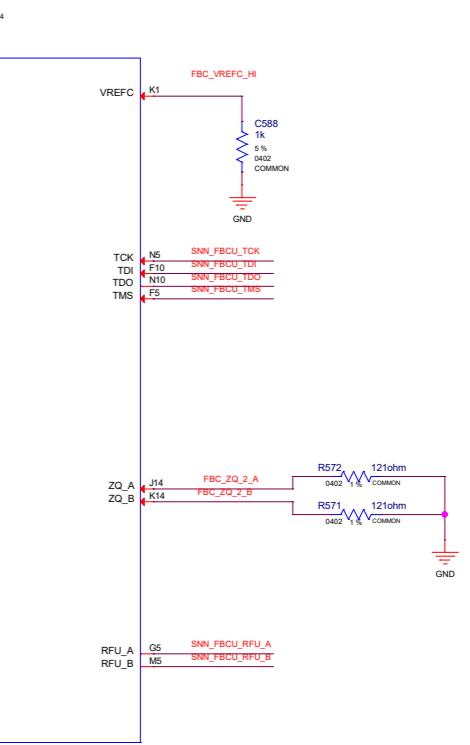


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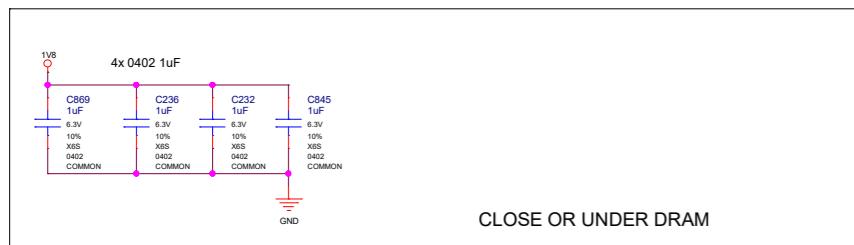
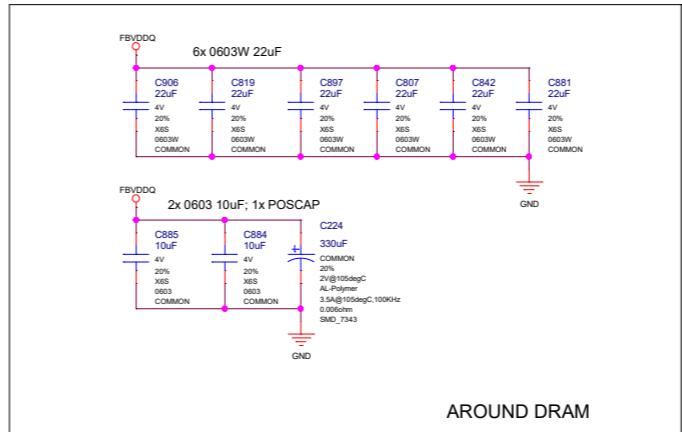
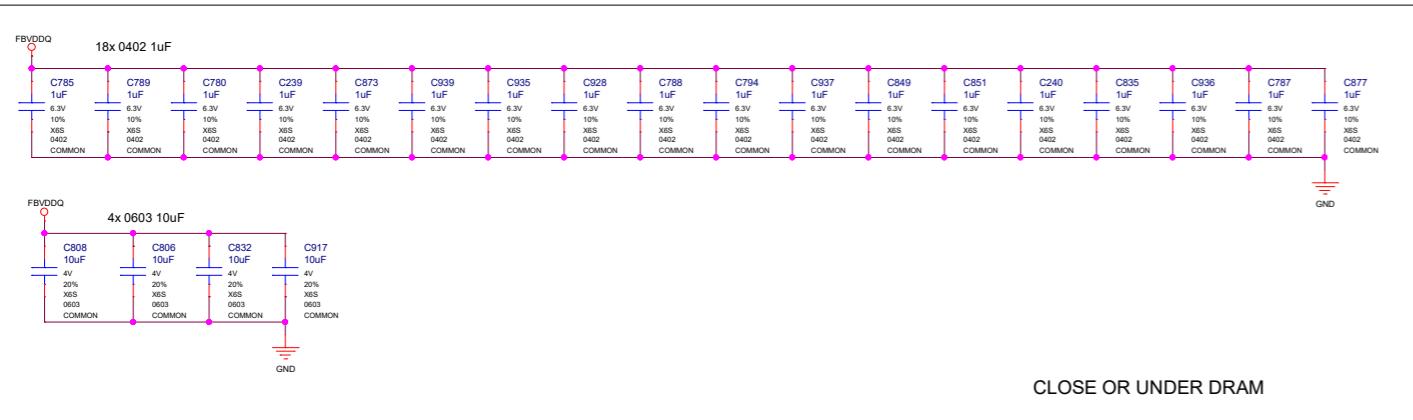
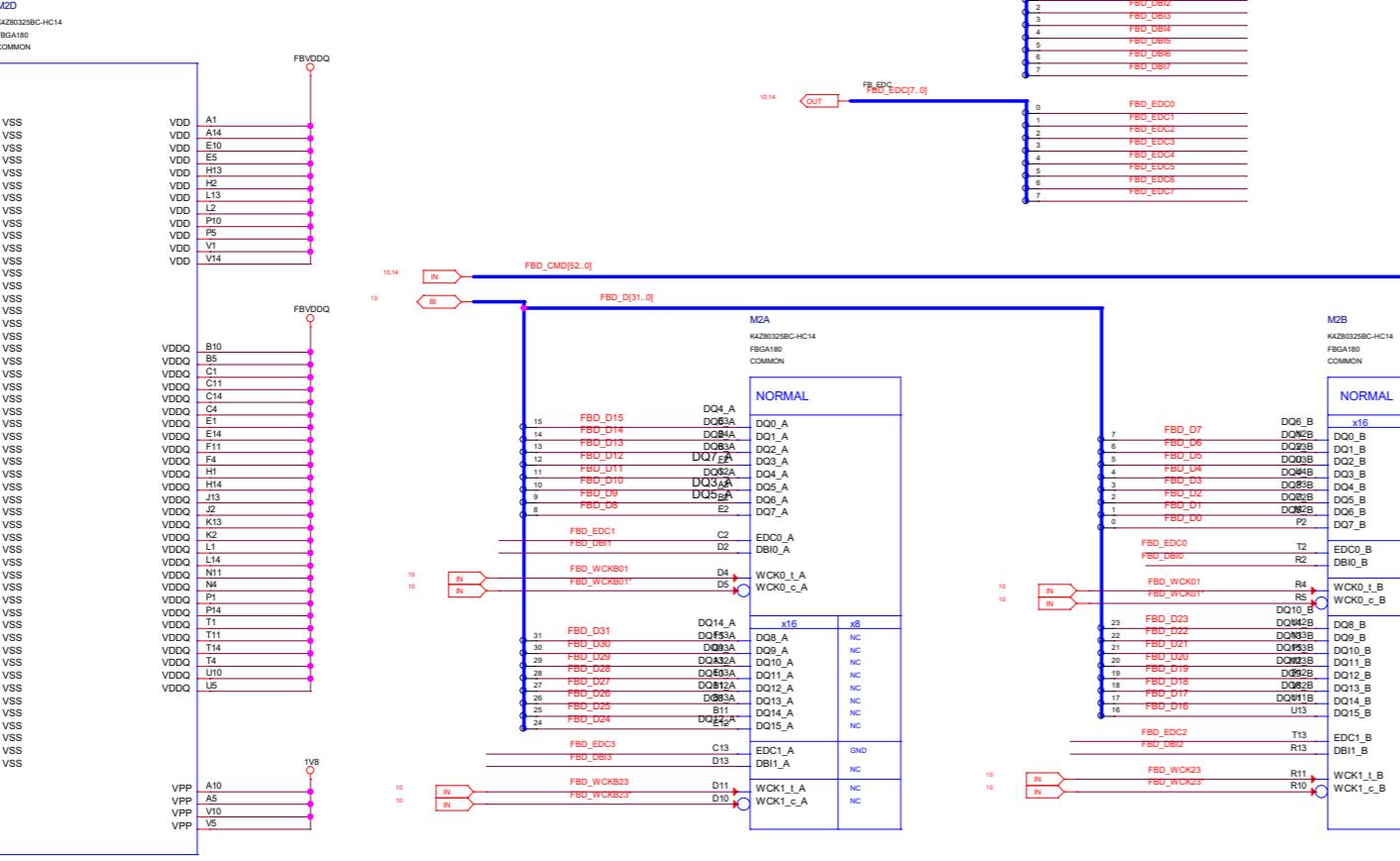
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Page13: MEMORY: FBD Partition 31..0



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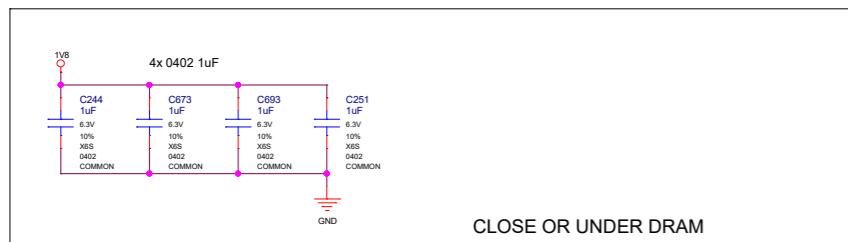
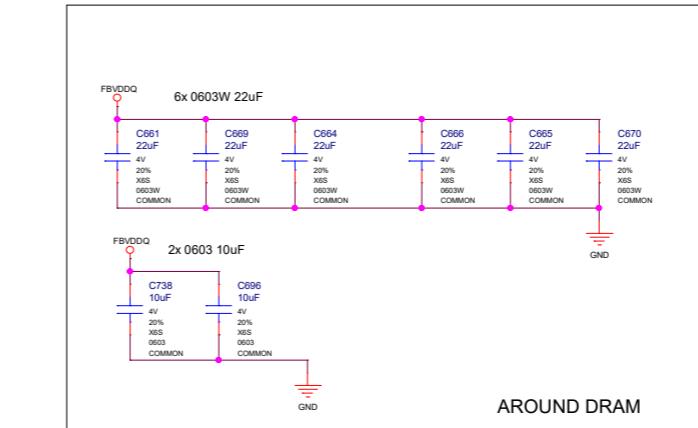
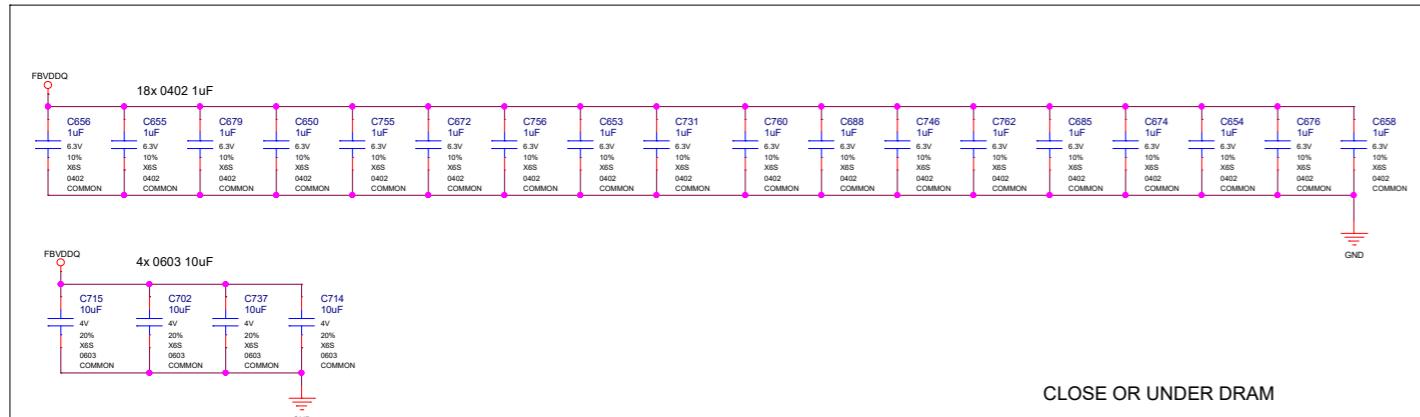
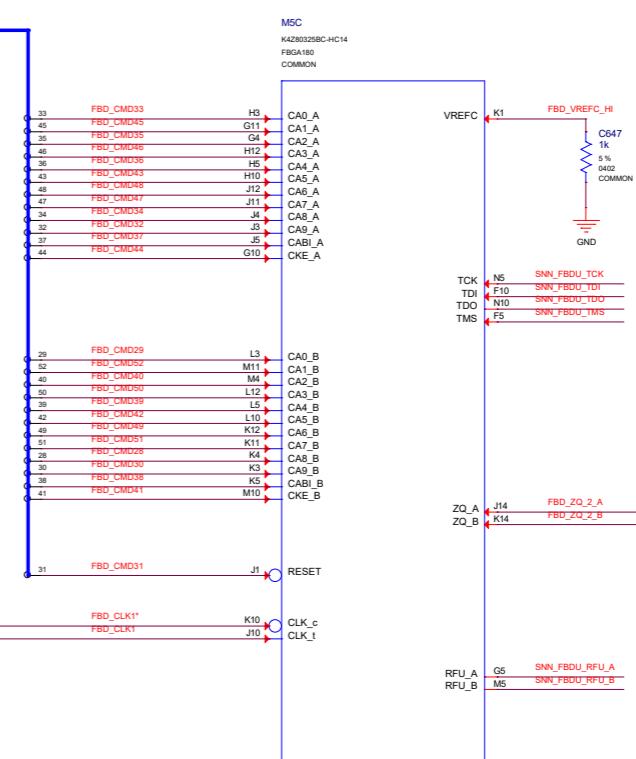
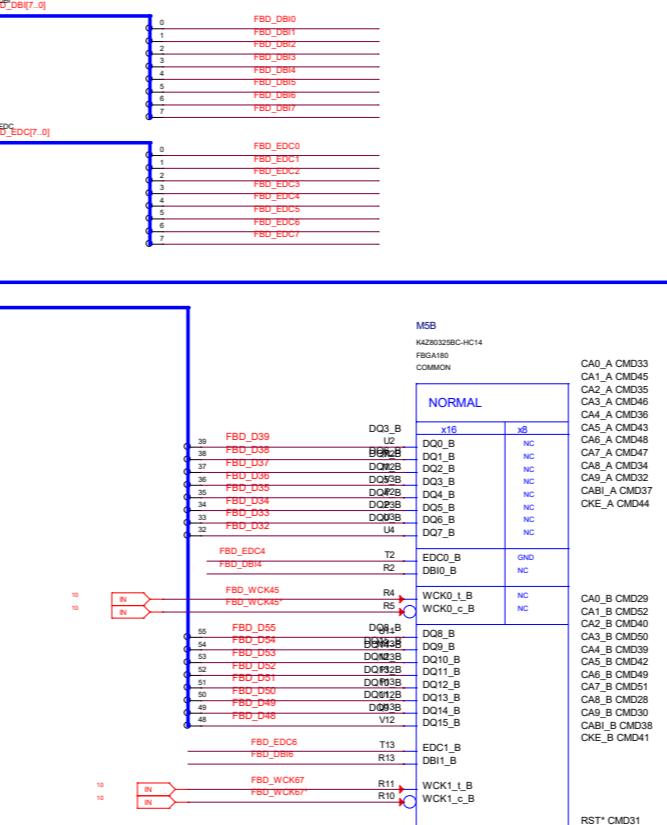
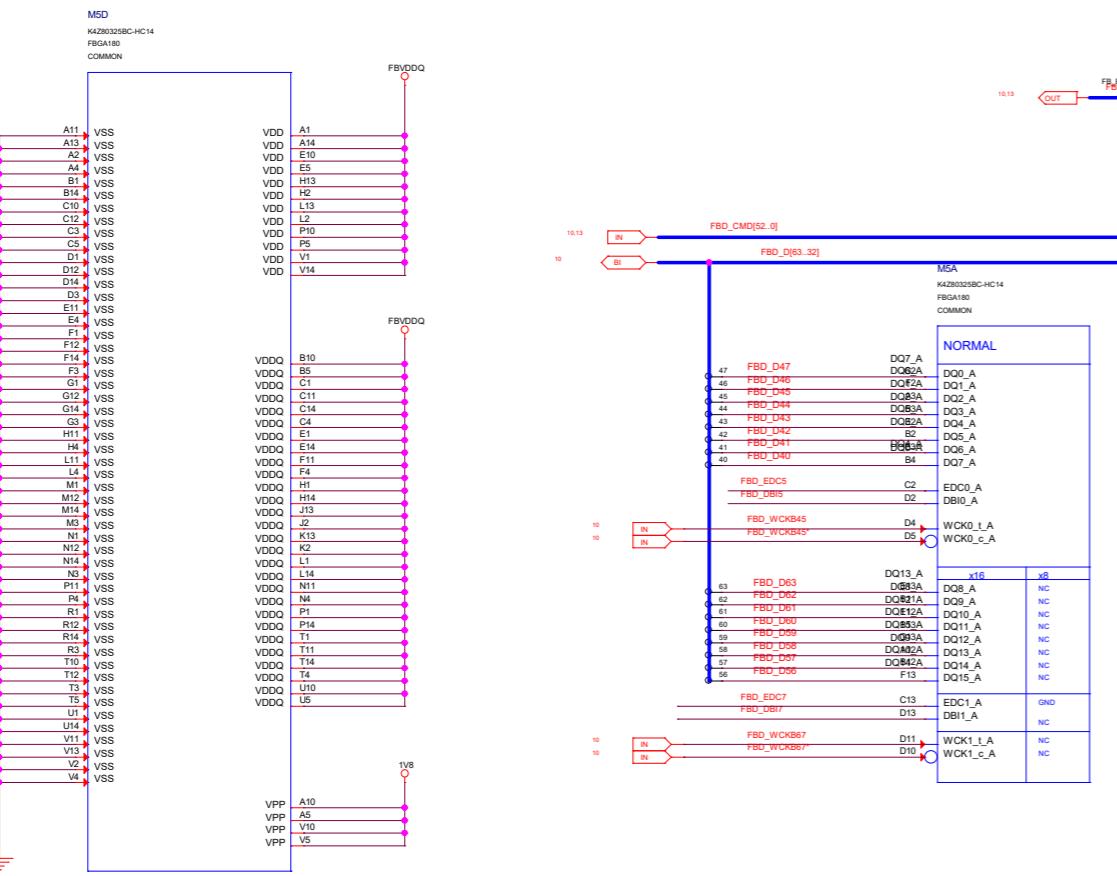
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Page14: MEMORY: FBD Partition 63..32



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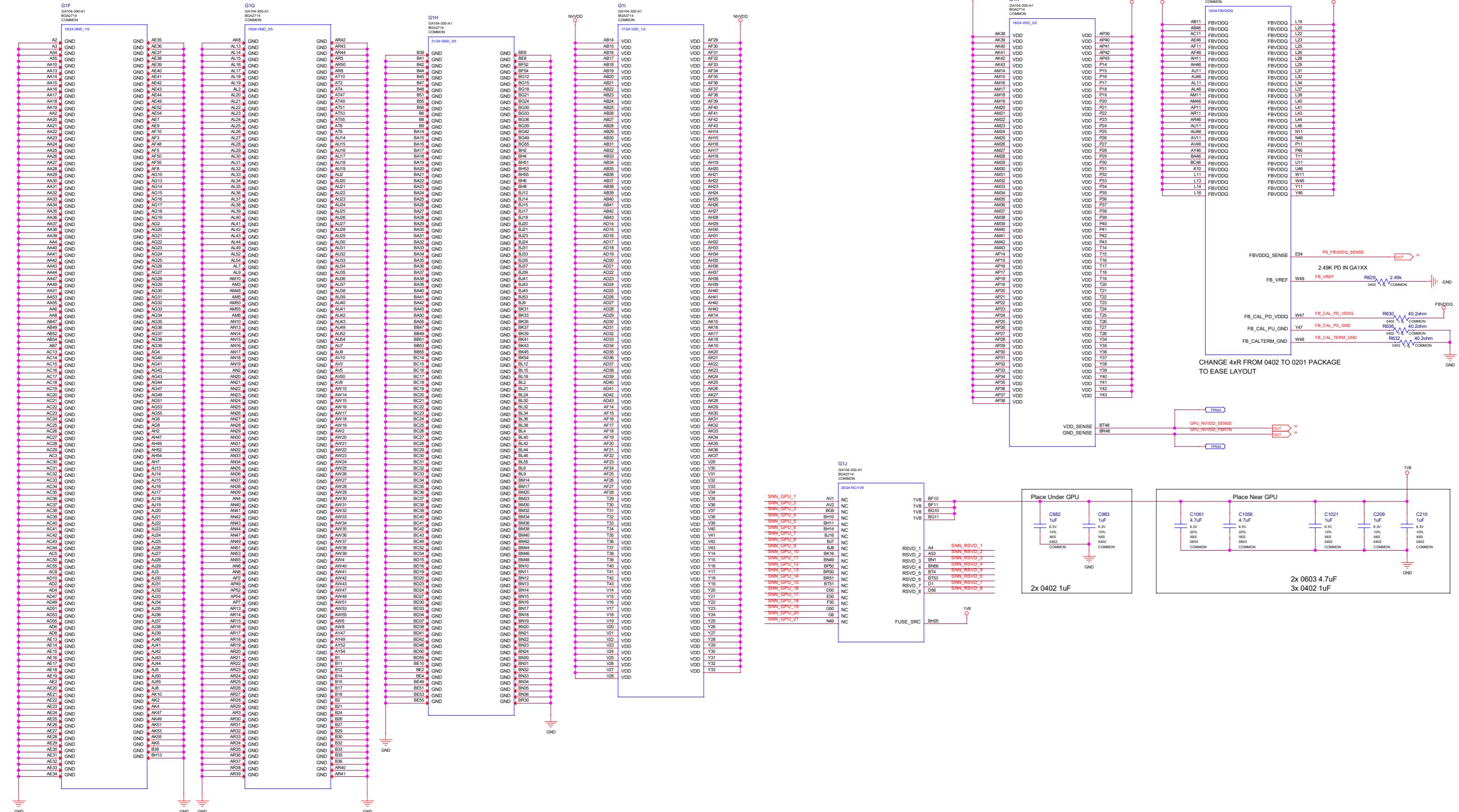
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Page15: GPU PWR and GND



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PAGE DETAIL	GPU PWR and GND

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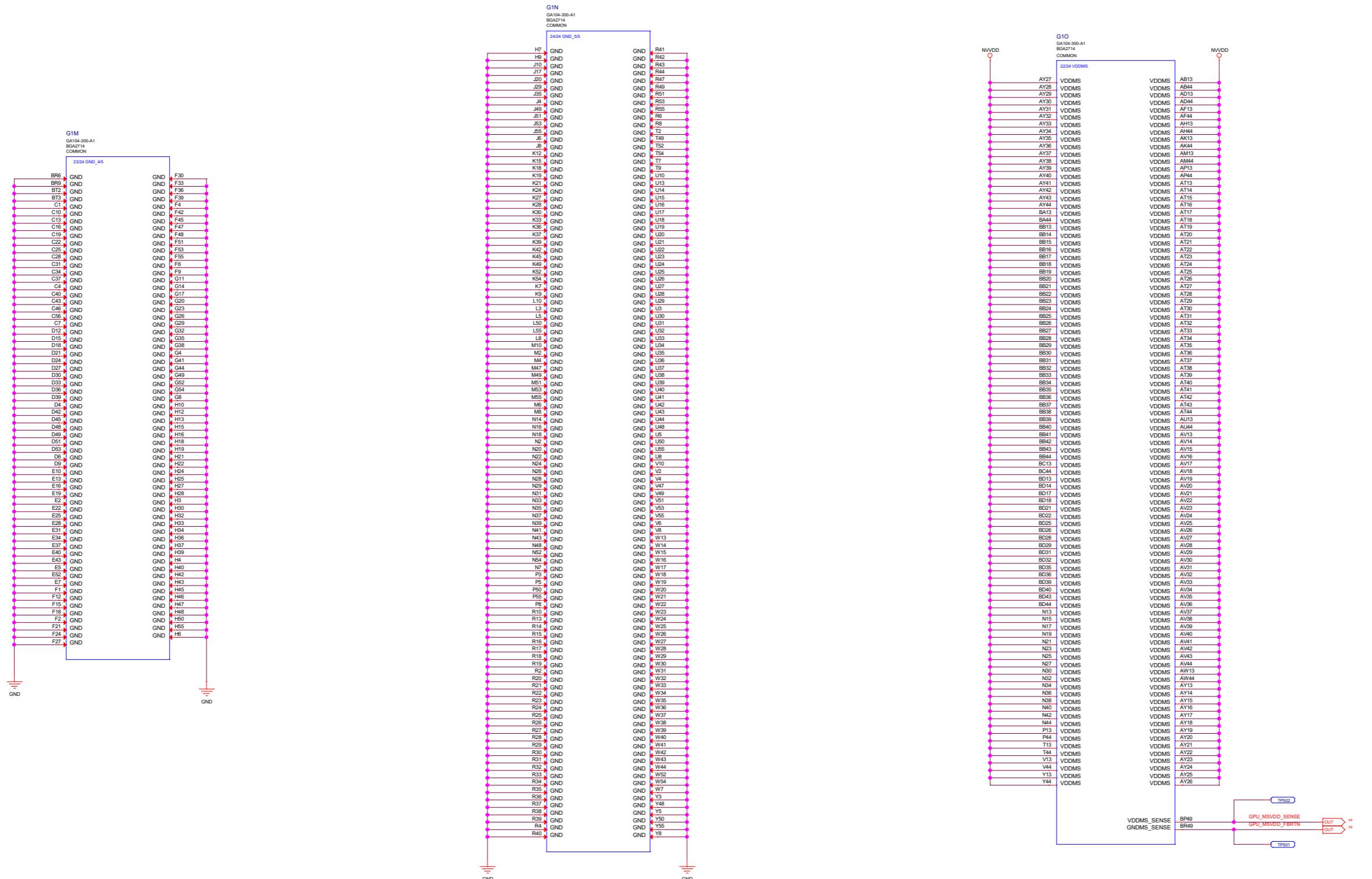
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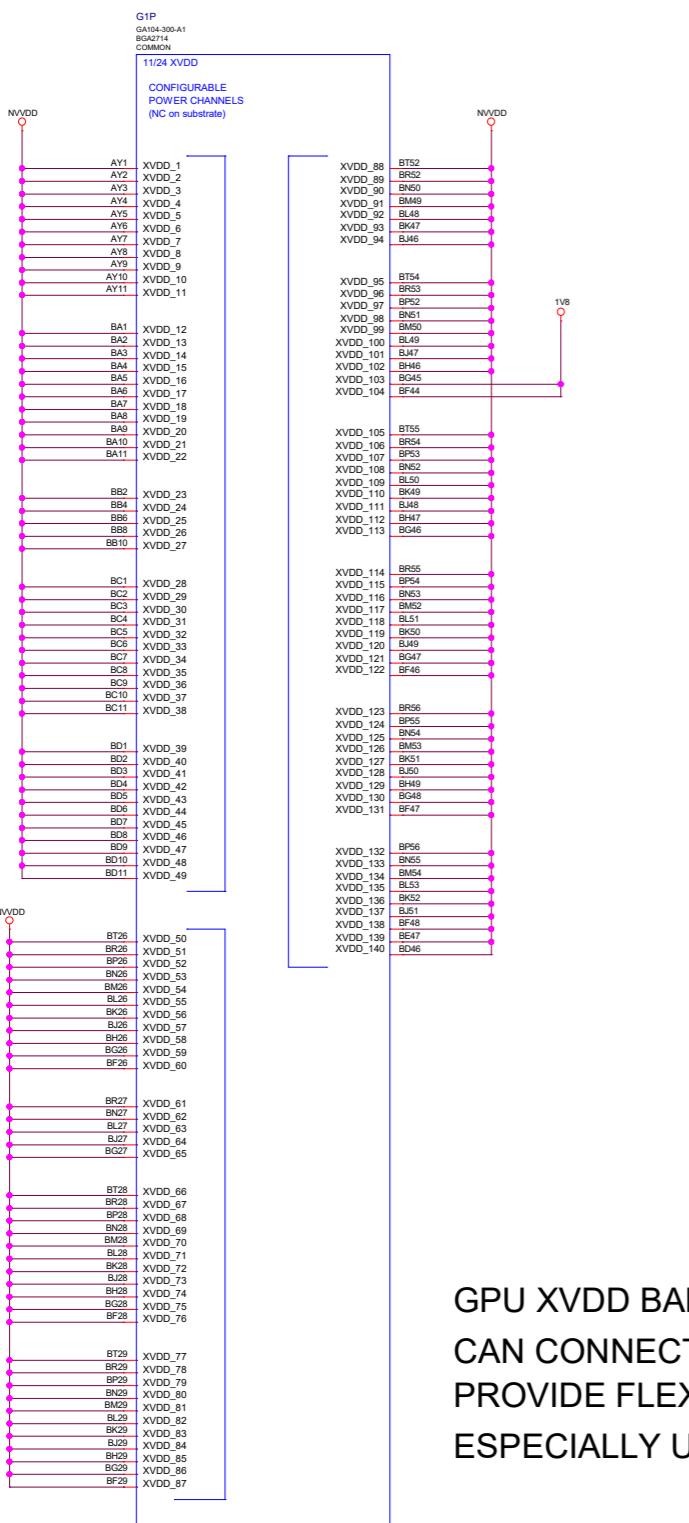
2701 SAN TOMAS EXPRESSWAY
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NV_PN 600-1G190-BASE-A02

PCB REV PG190-A02 PAGE 16 OF 50
BOM REV A DATE 12-JUN-2020

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR and GND 2



GPU XVDD BALLS (NC IN SUBSTRATE):
CAN CONNECT TO ANY POWER NET (NV/MS/1V8/PEX, etc.) ON SYSTEM BOARD,
PROVIDE FLEXIBILITY TO OPTIMIZE POWER CHANNELS ON SYSTEM BOARD,
ESPECIALLY USEFUL FOR LOW-COST DESIGN WITH REDUCED PCB LAYERS.

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU XVDD

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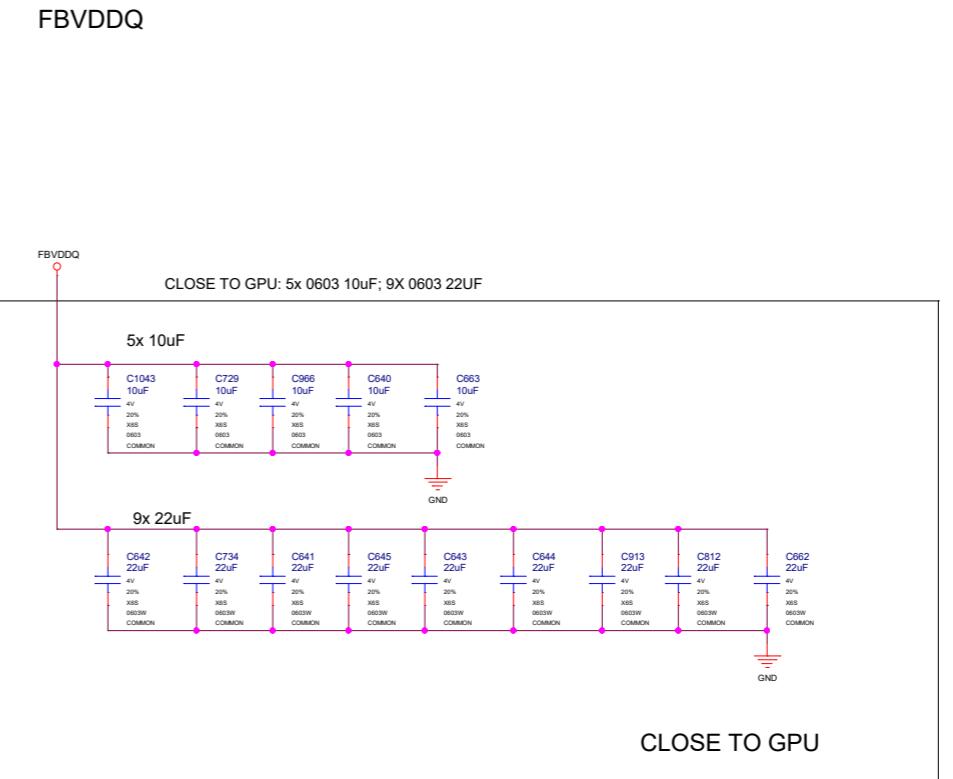
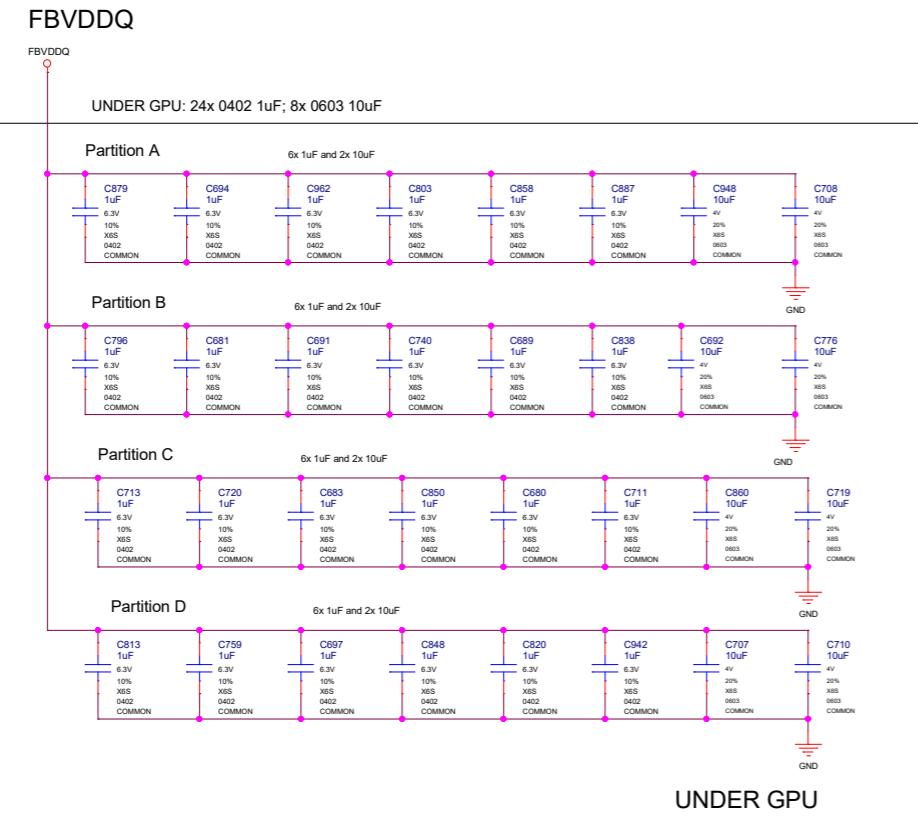
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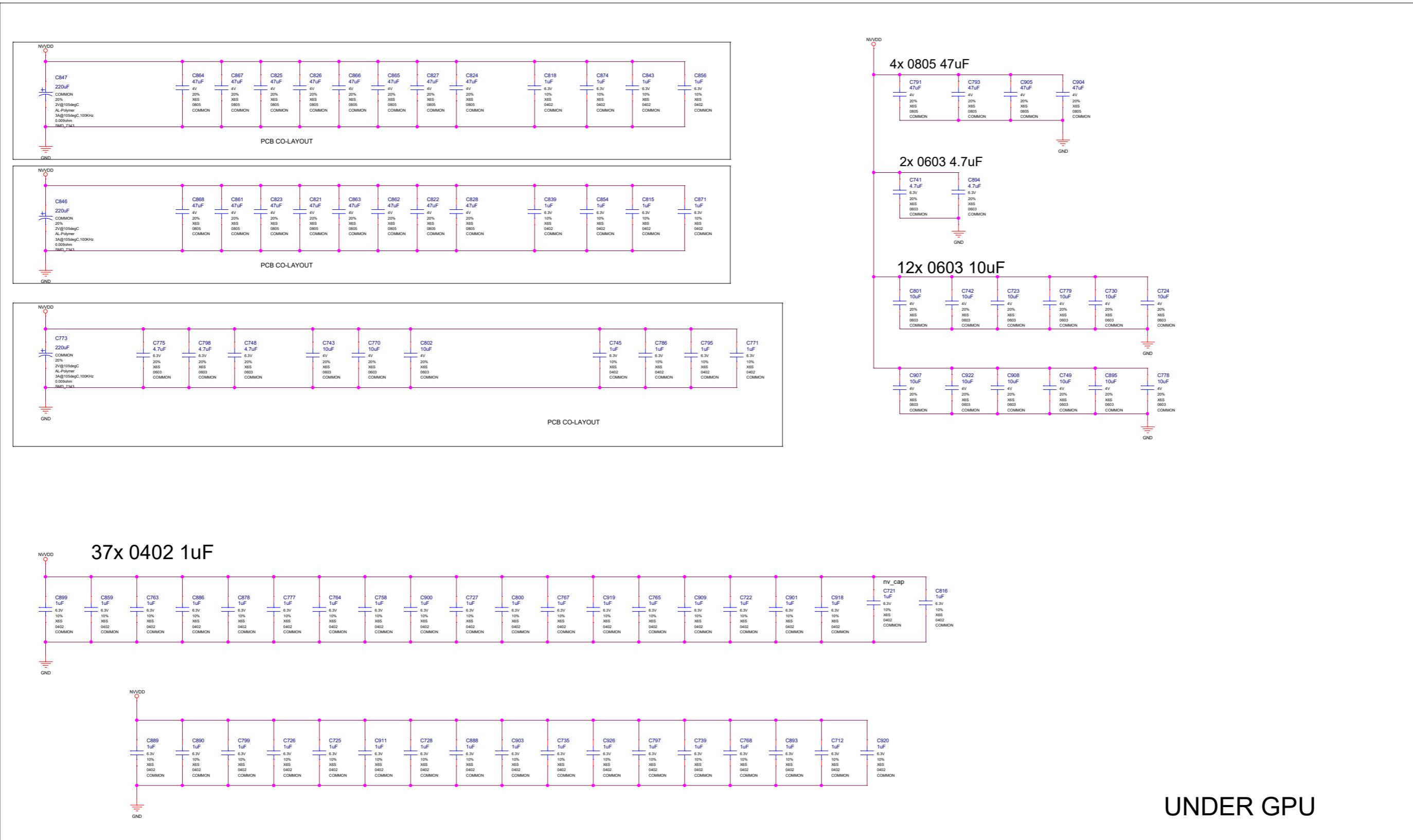


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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING FBVDDQ

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NV_PN	600-1G190-BASE-A02	PCB REV	PG190-A02
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING NVD

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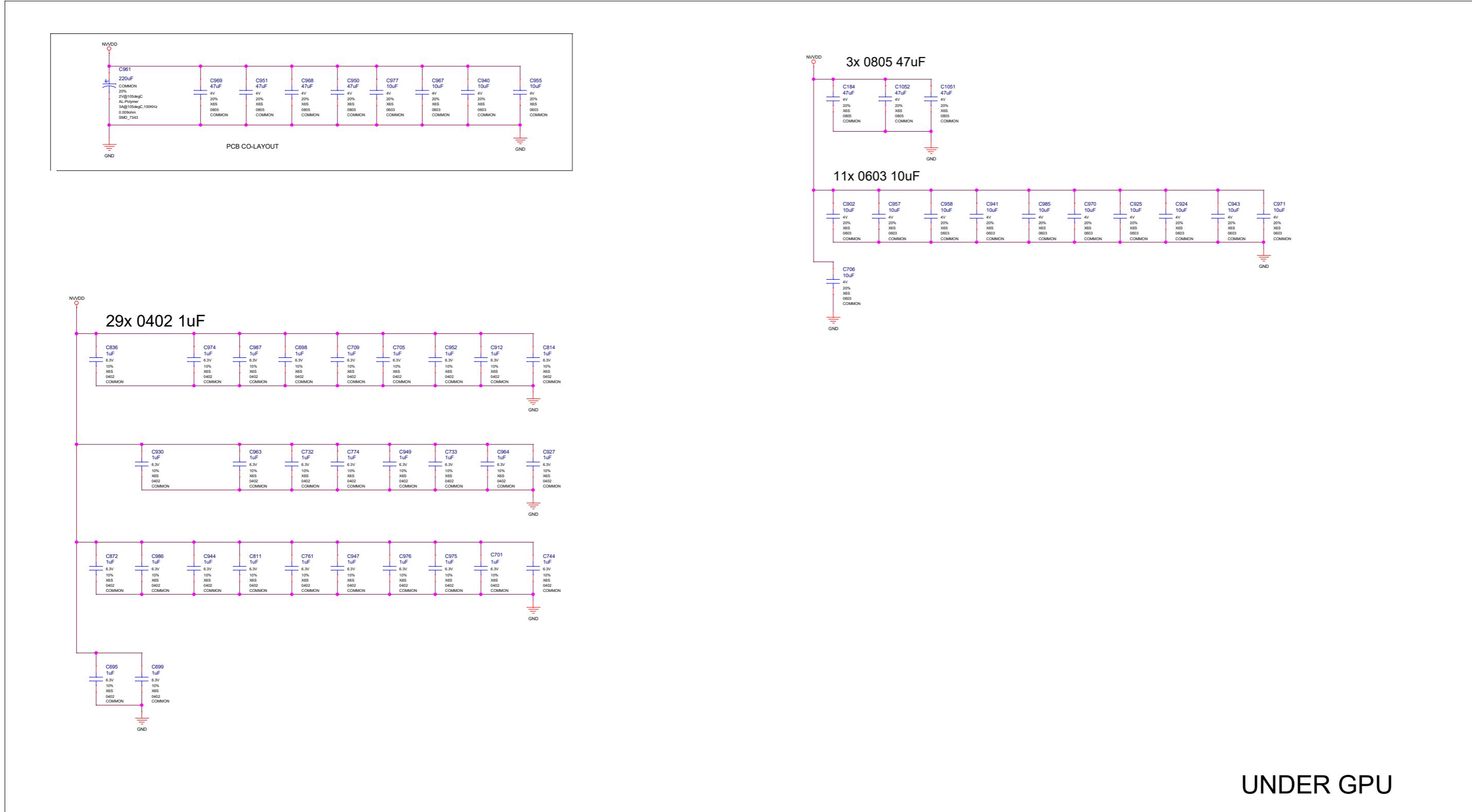
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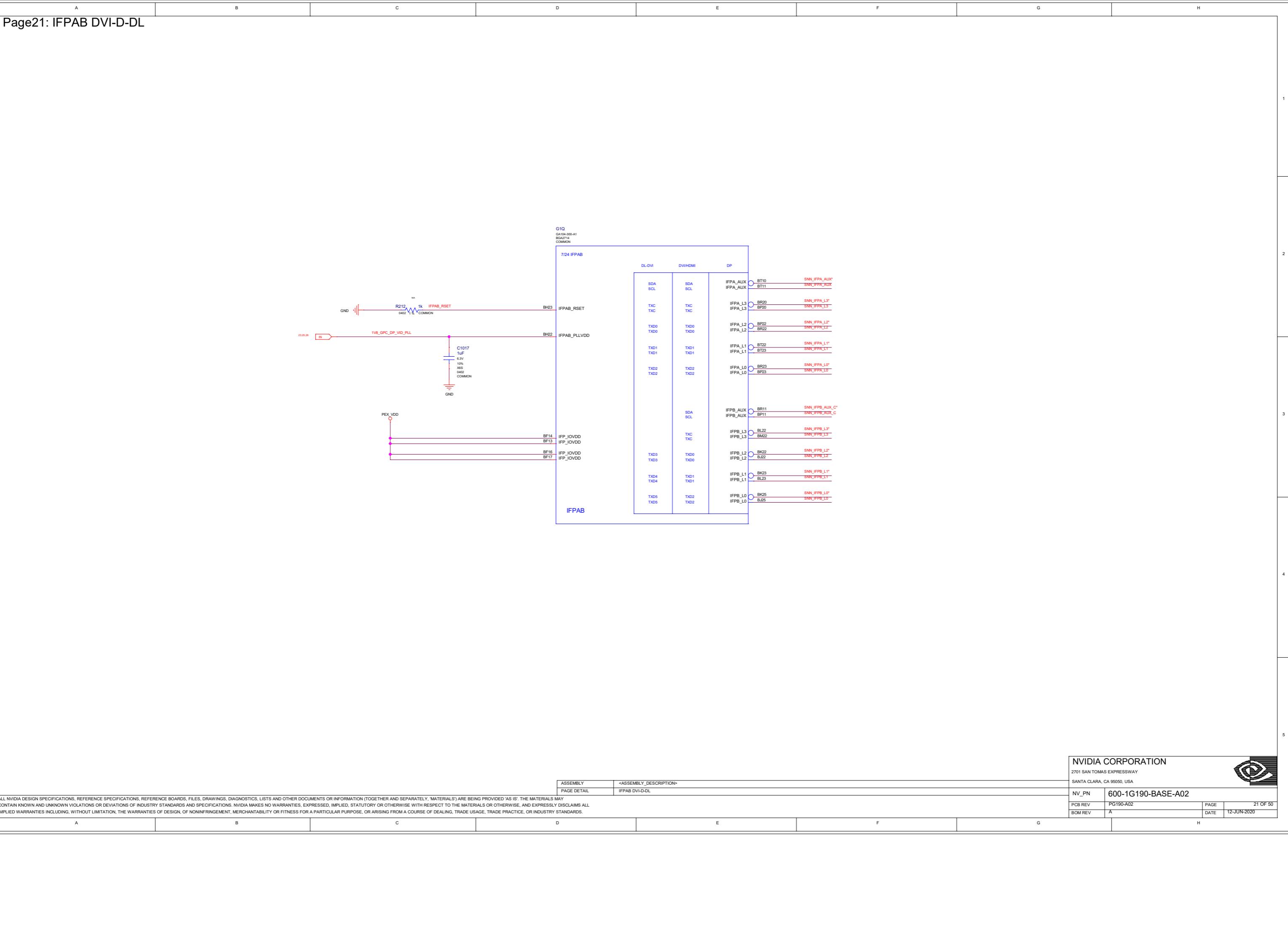
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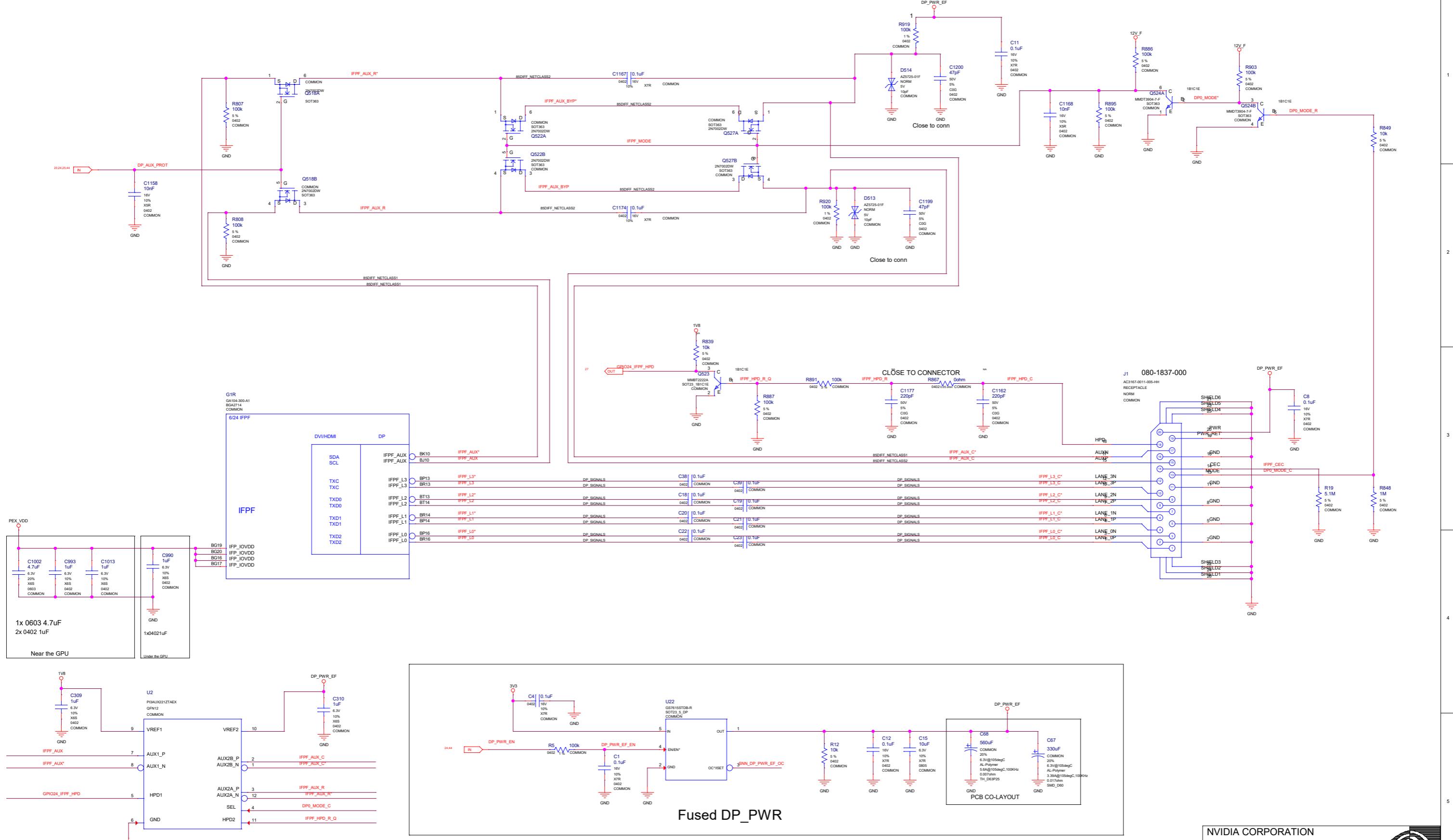
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING NVVDD 2

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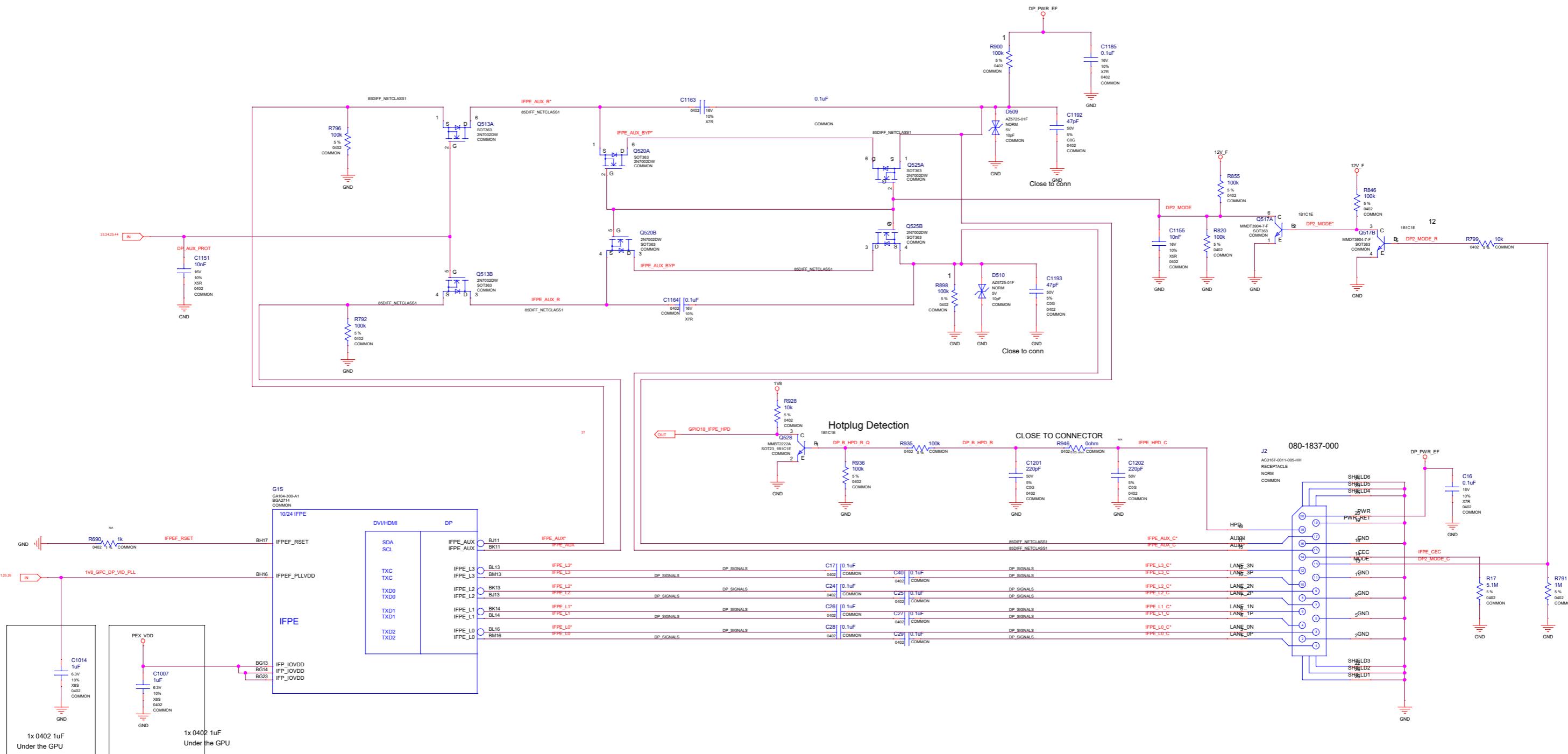
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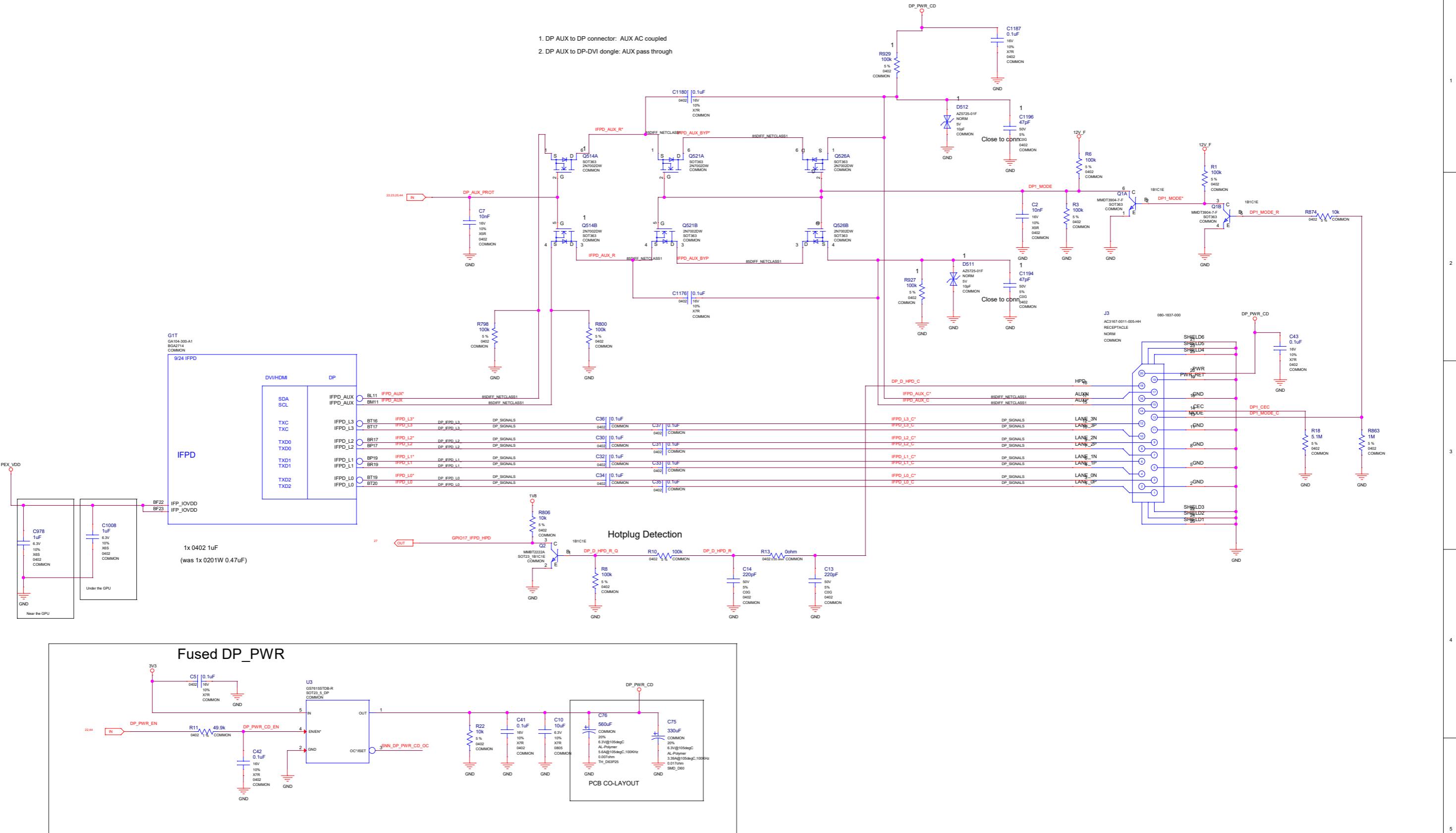
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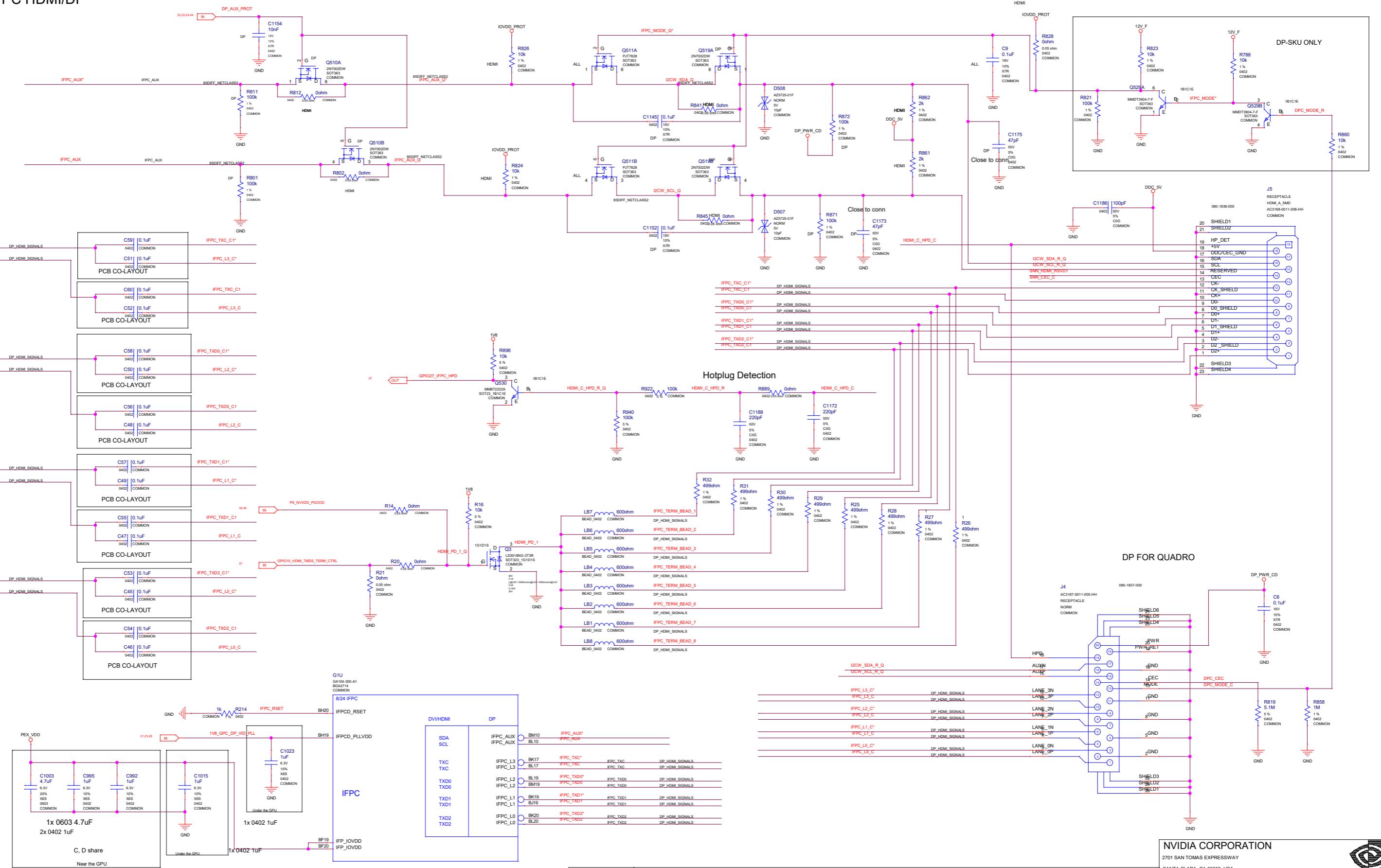
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Page25: IFPC HDMI/DP



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
AGE DETAIL	IFPC HDMI/DP

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PG190-A02

DOM REV A

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Digitized by srujanika@gmail.com

Page26: MISC: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	4'd7	FS_OVERT ENABLE
L	M	L	4'd9	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

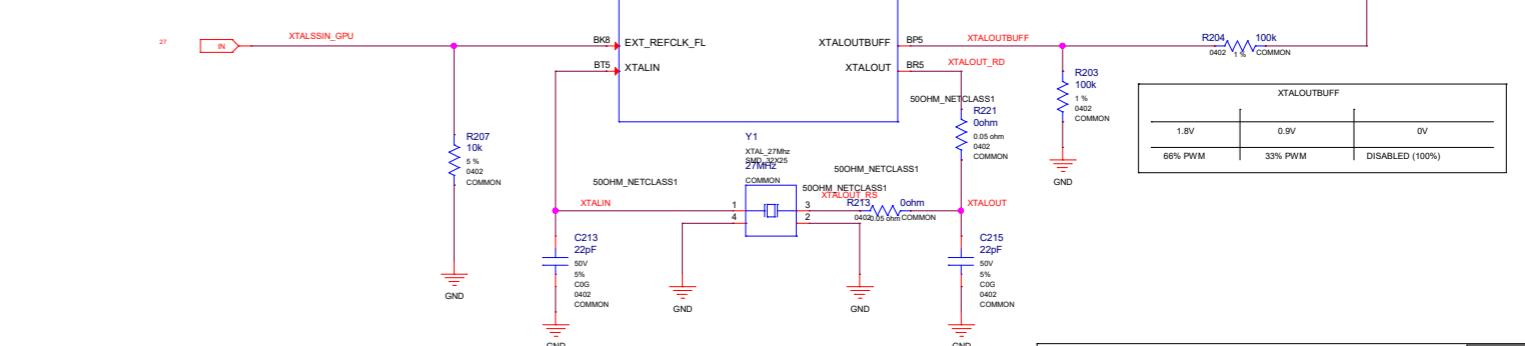
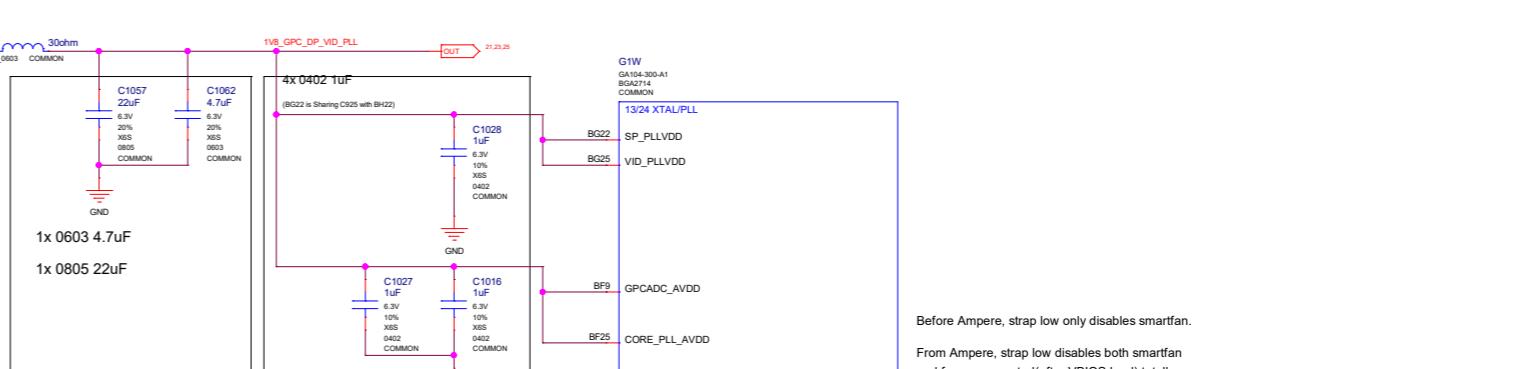
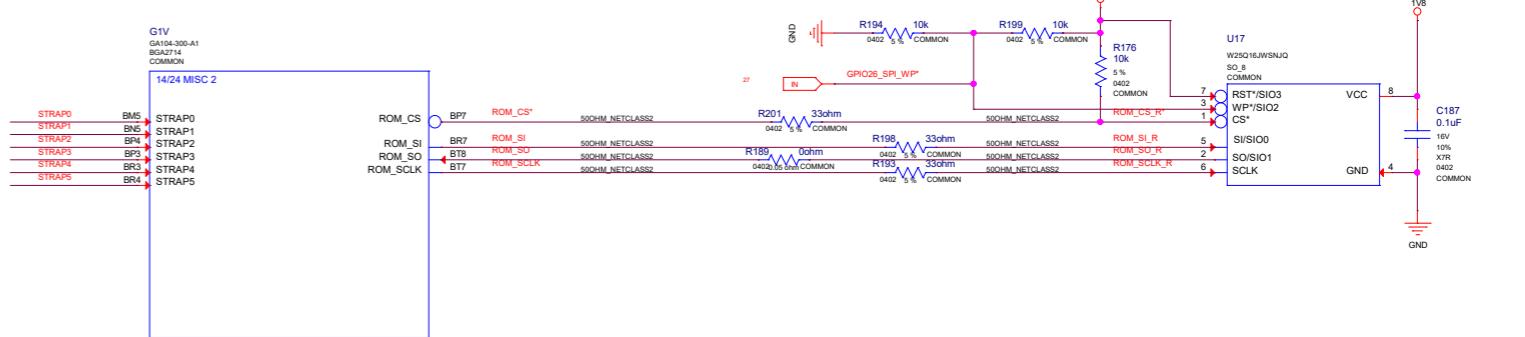
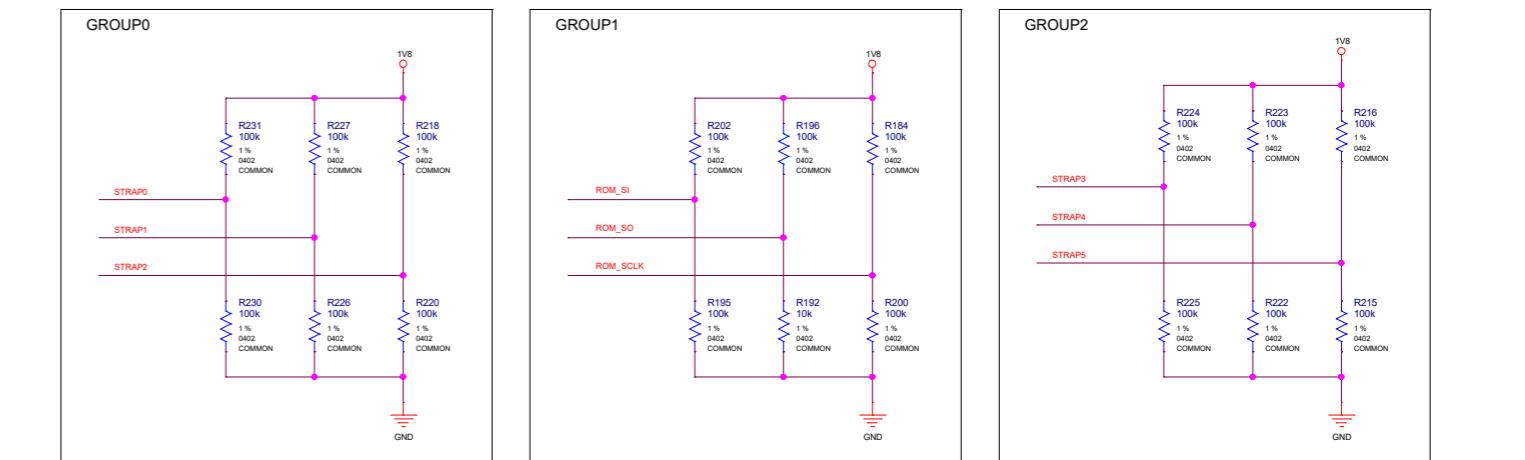
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



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ASSEMBLY

PAGE DETAIL

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MISC: ROM, XTAL, STRAPS

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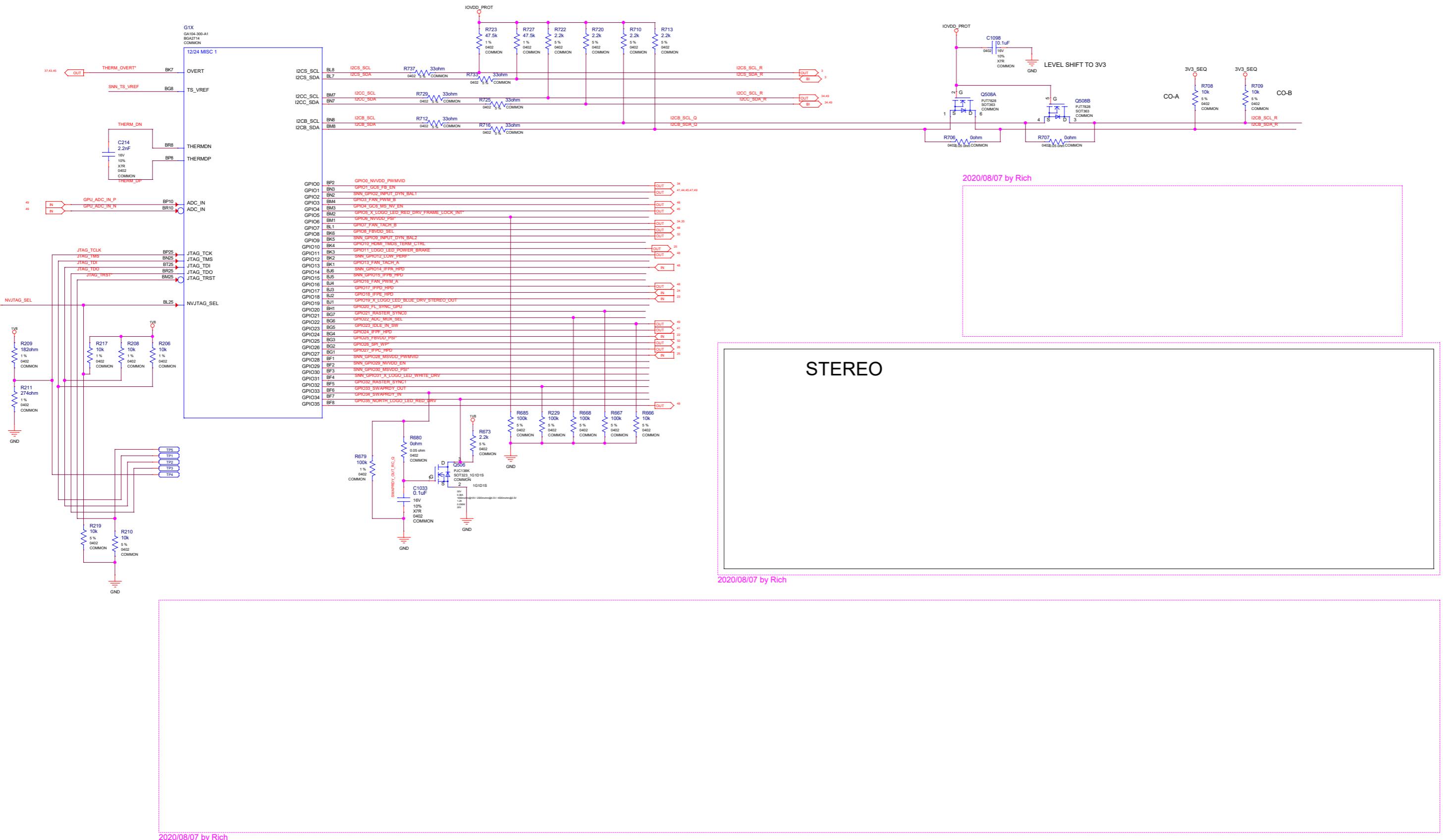
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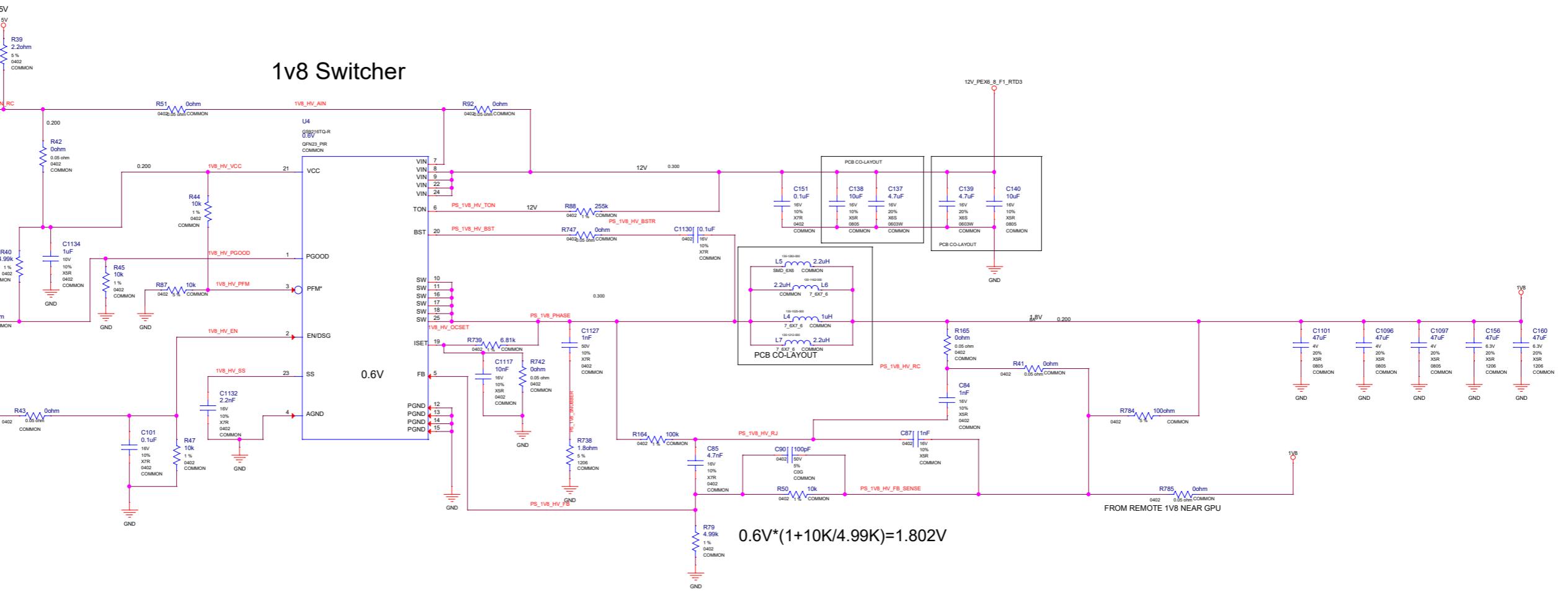
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NVIDIA CORPORATION  2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95051, USA NV_PN 600-1G190-BASE-A02 PCB REV PG190-A02 PAGE 28 OF 50 BOM REV A DATE 12-JUN-2020													
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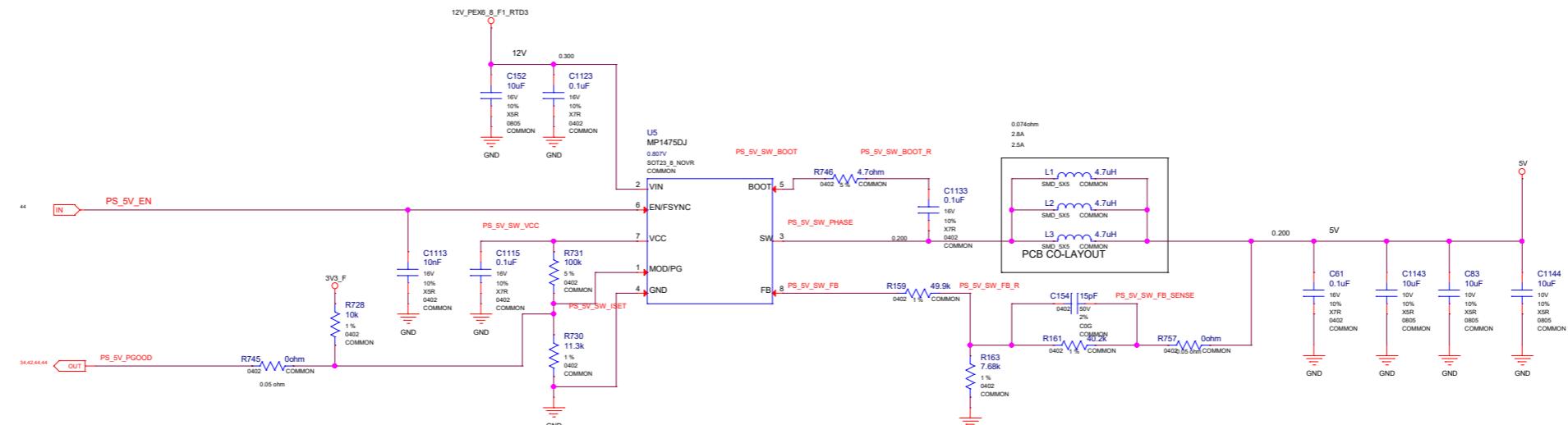
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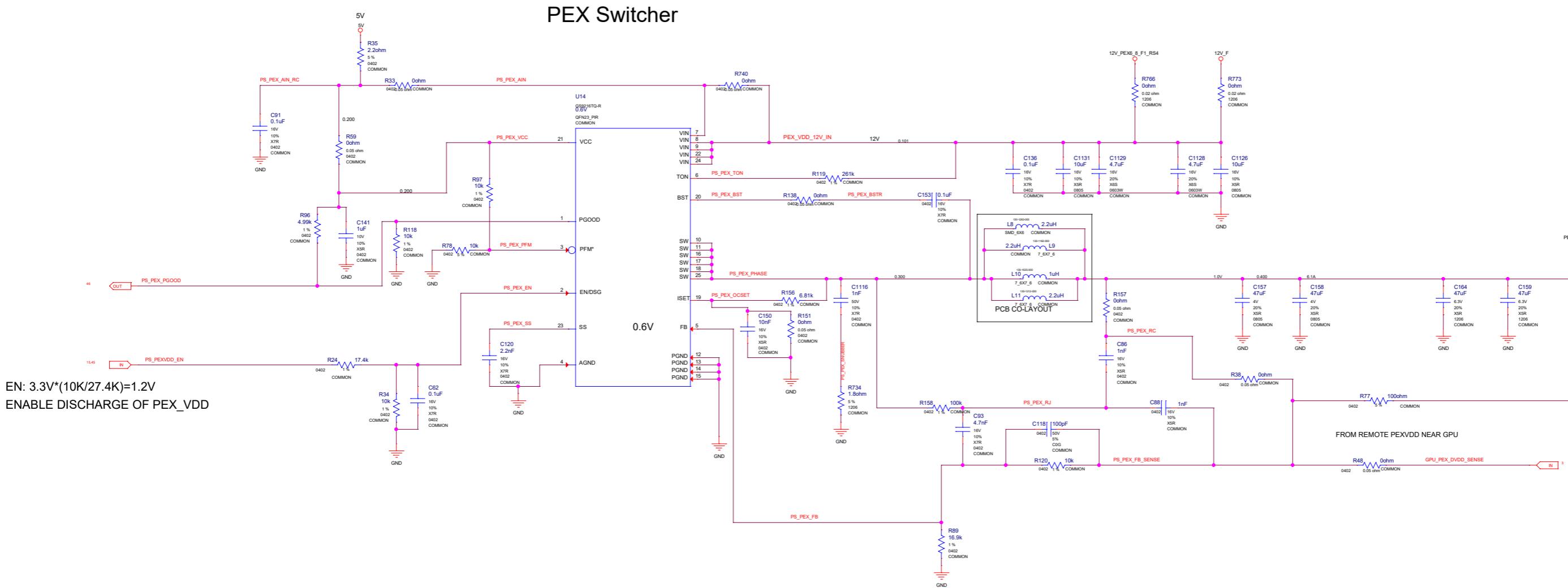


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PEX Switcher

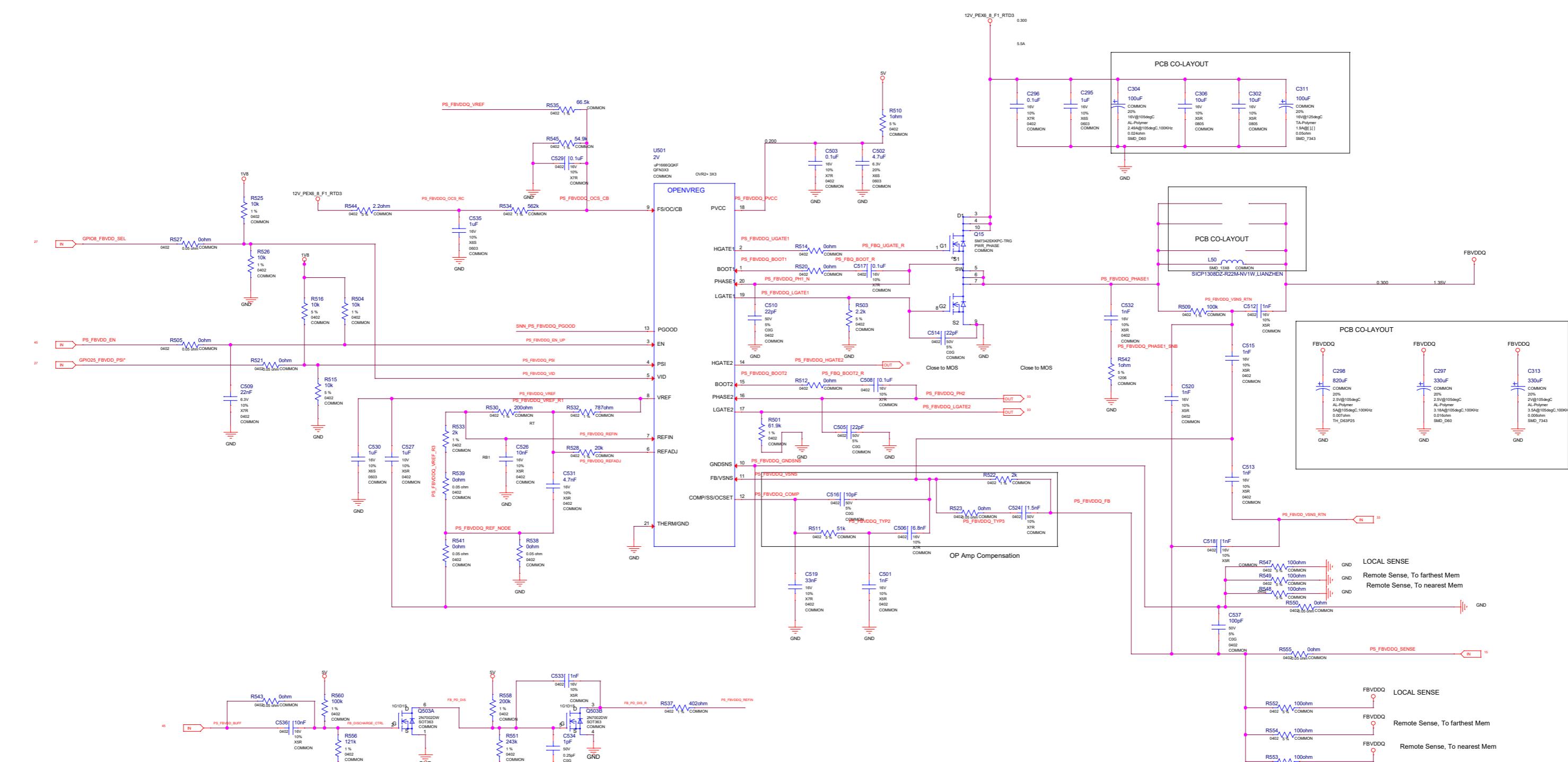


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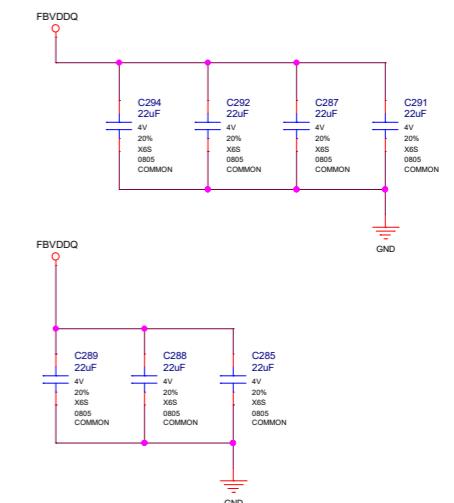
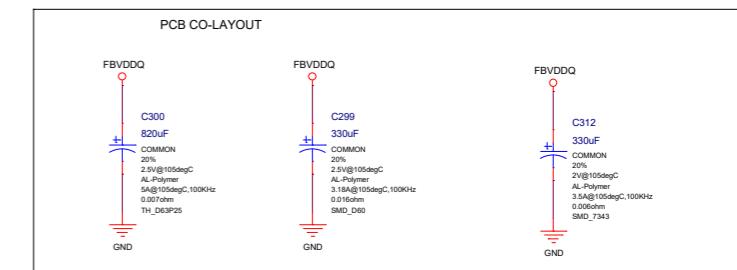
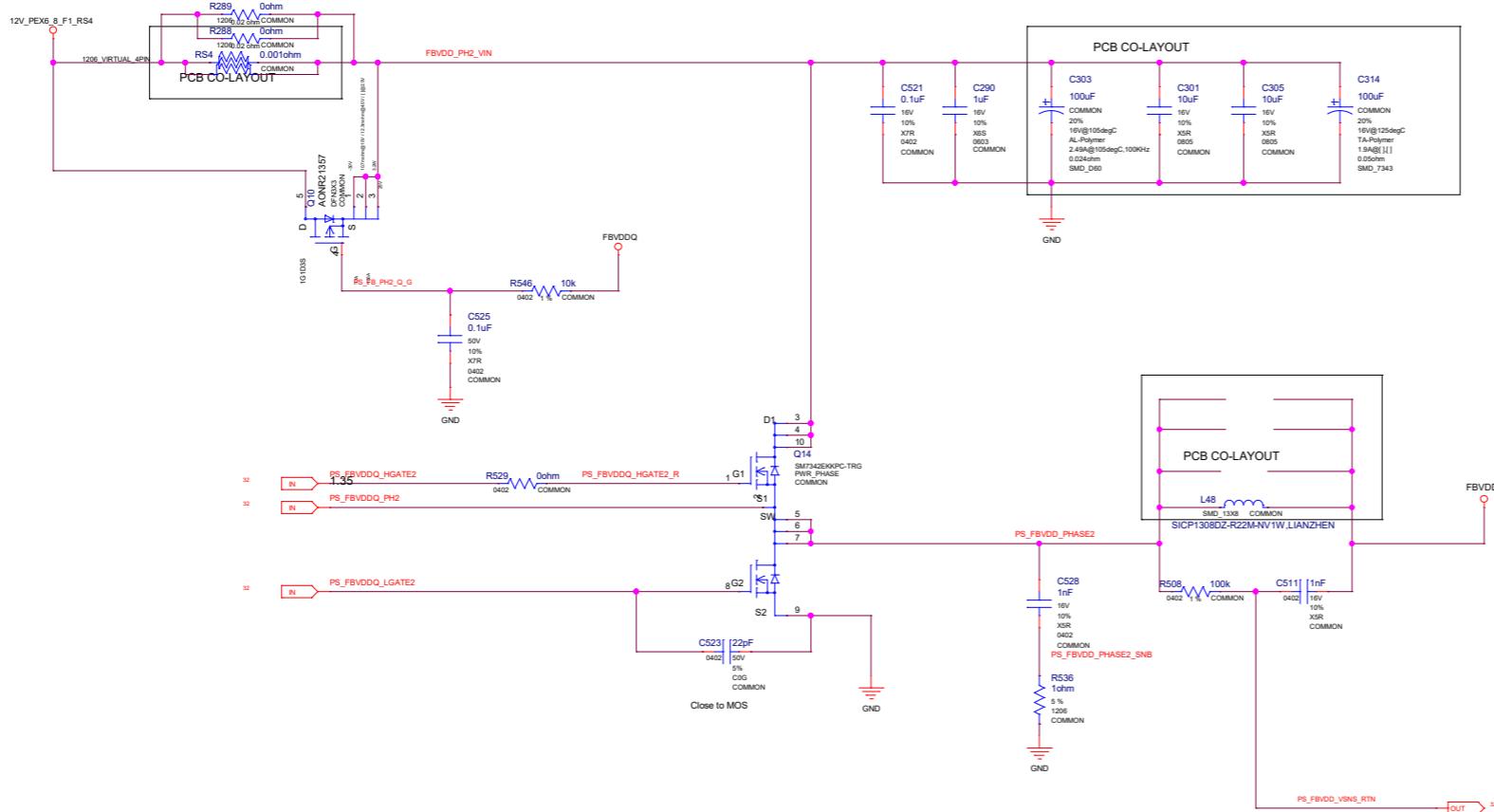


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FBVDD PH2 INPUT ANTI-BACKDRIVE



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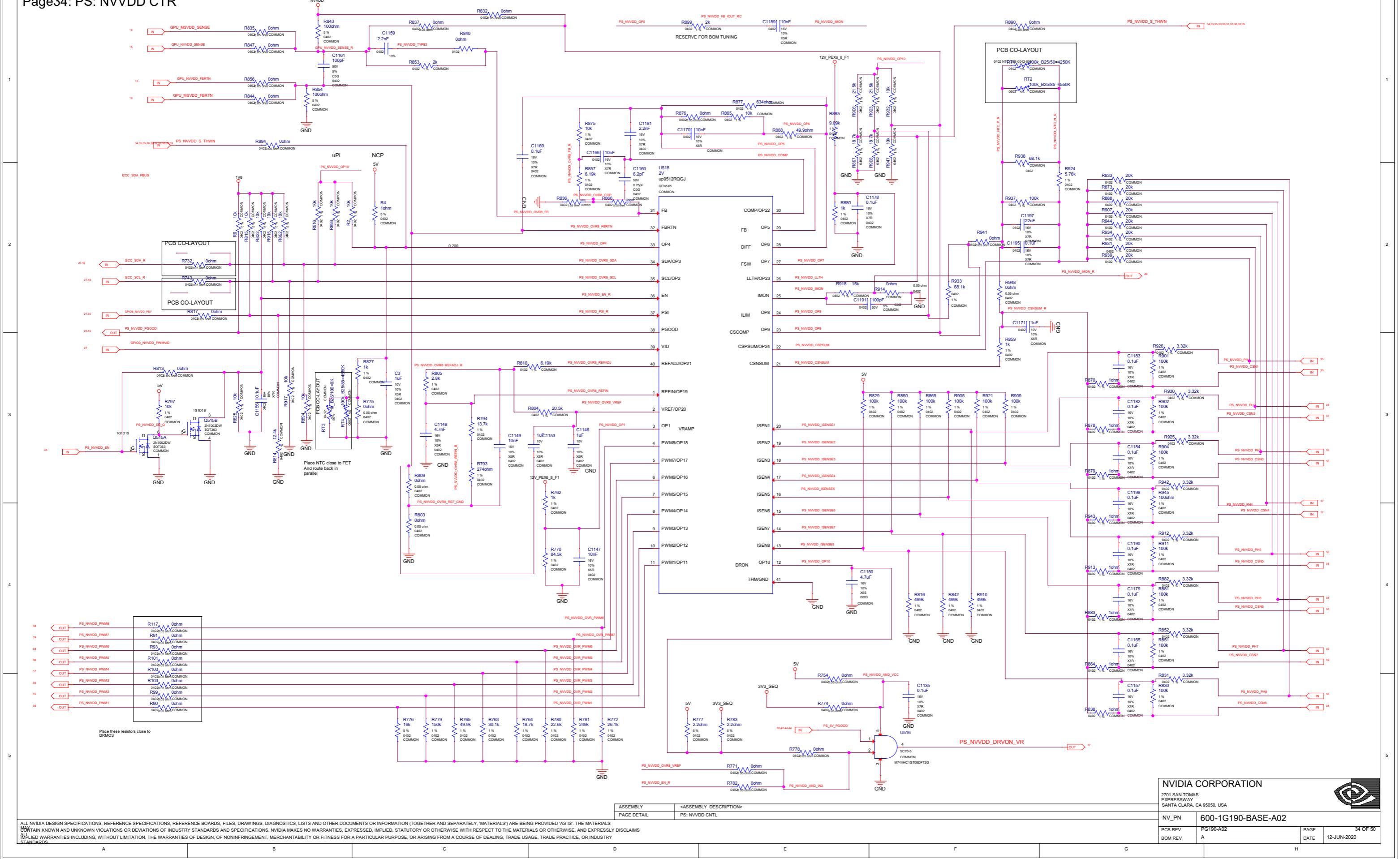
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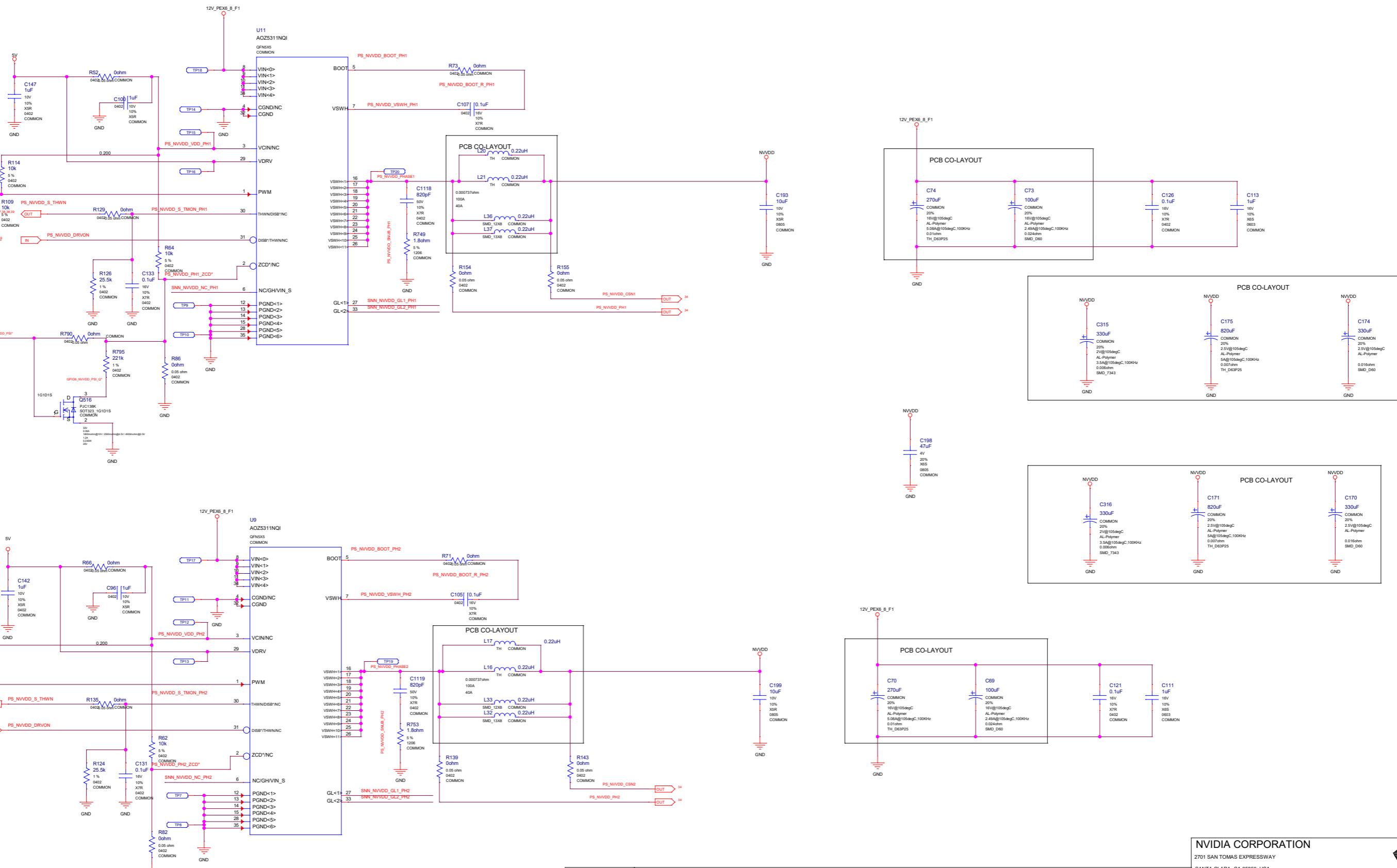
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Page34: PS: NVVDD CTR





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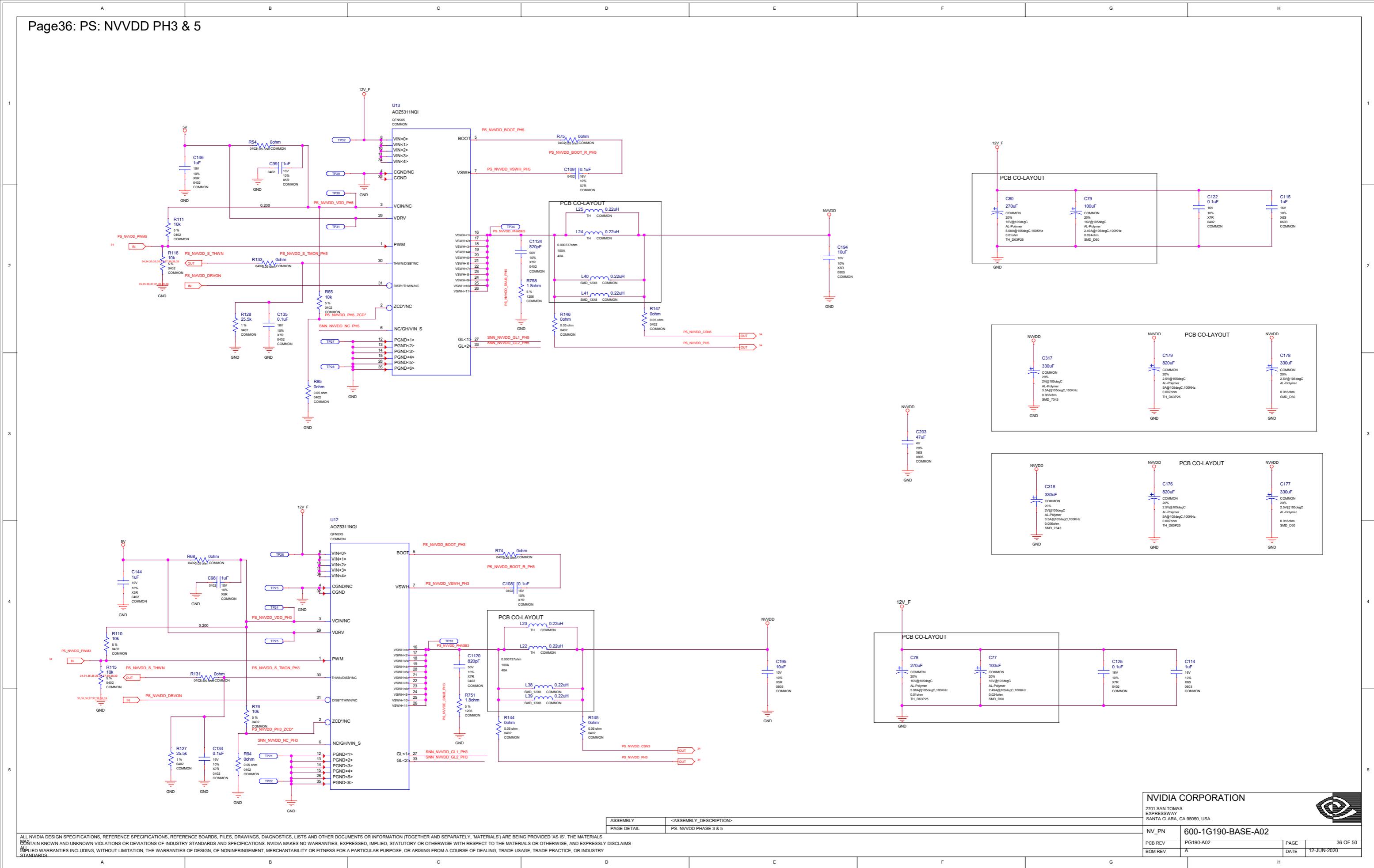
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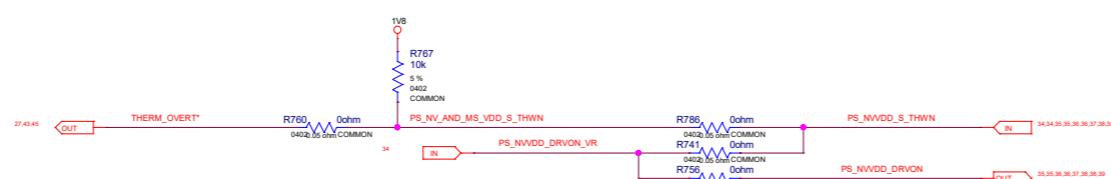
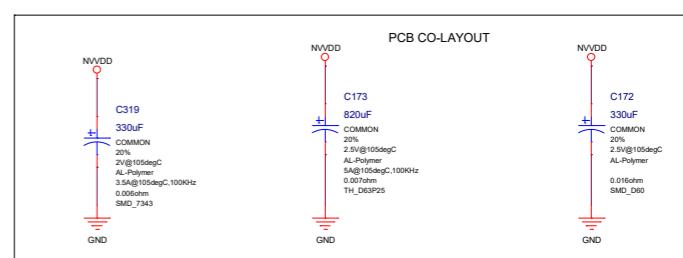
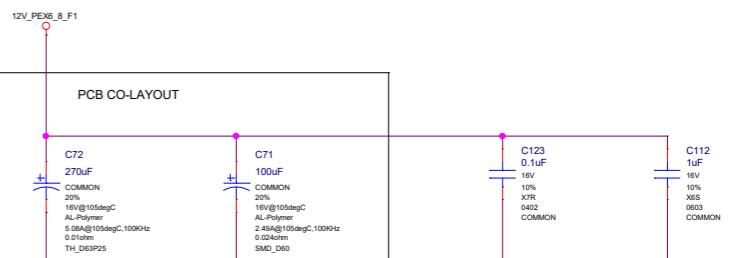
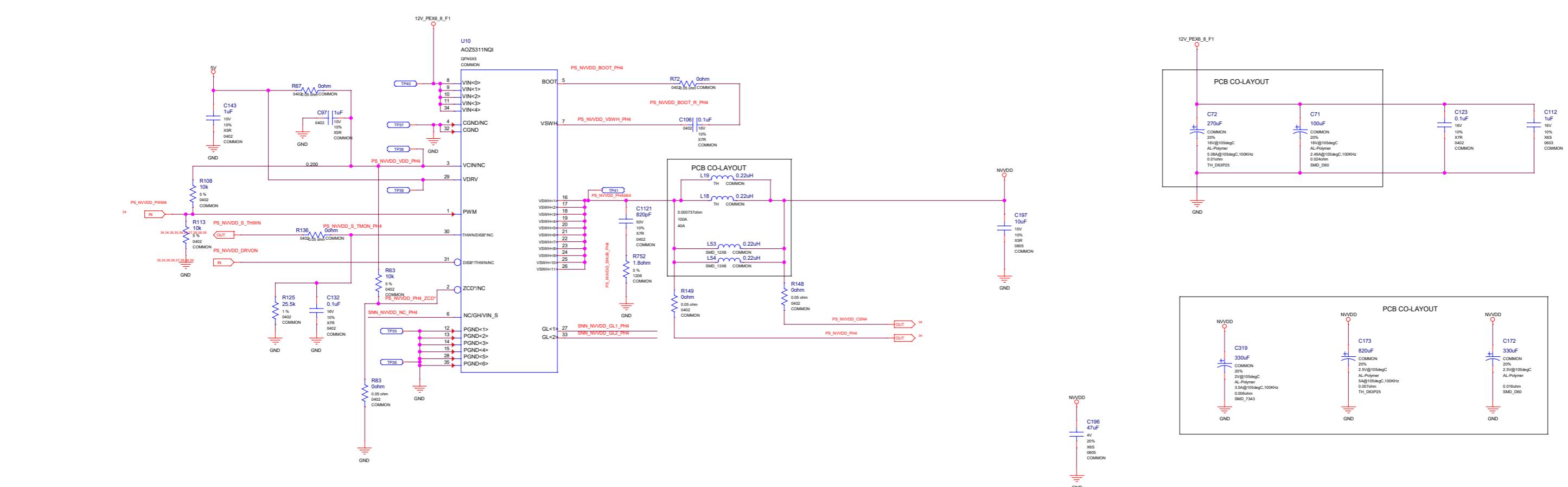
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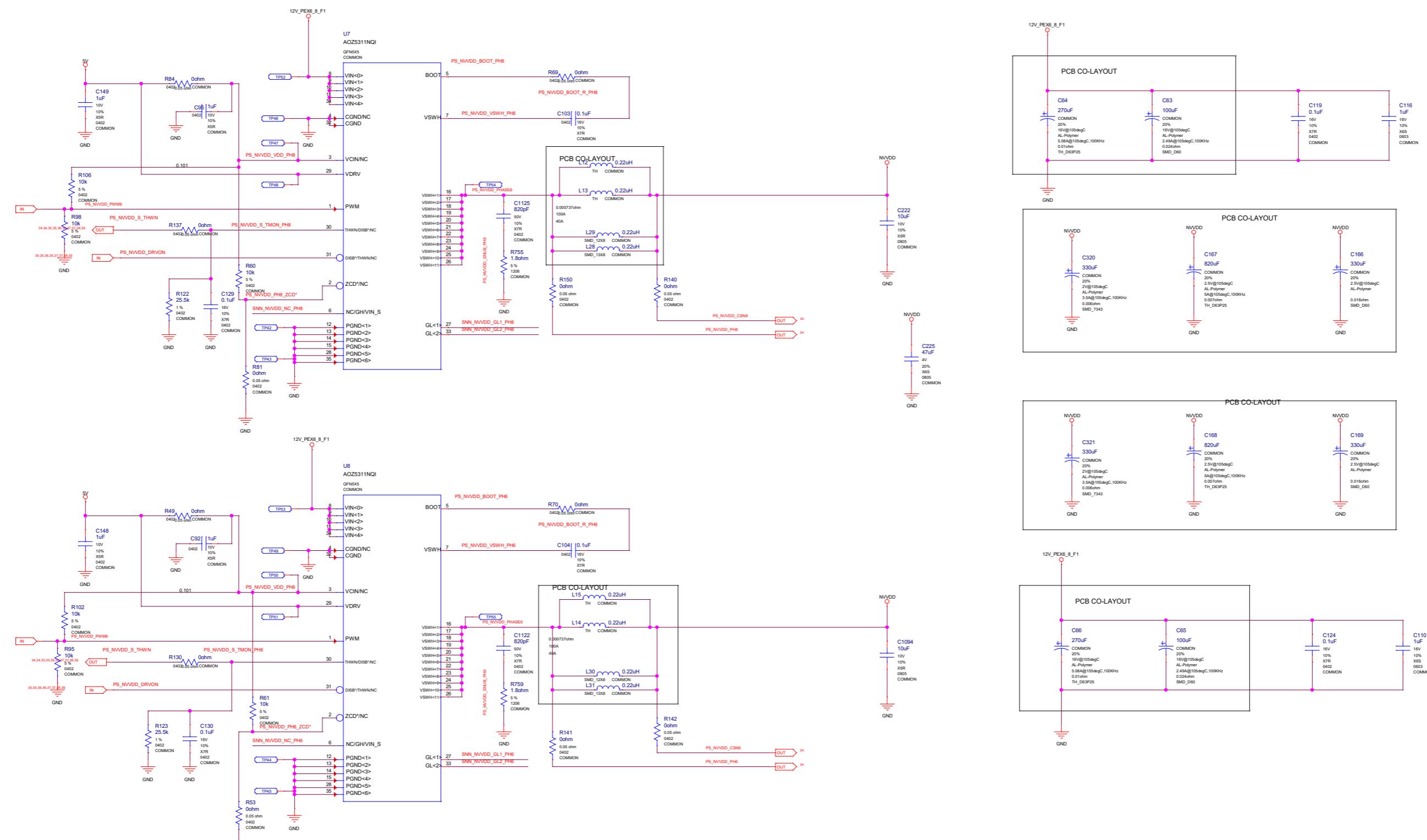


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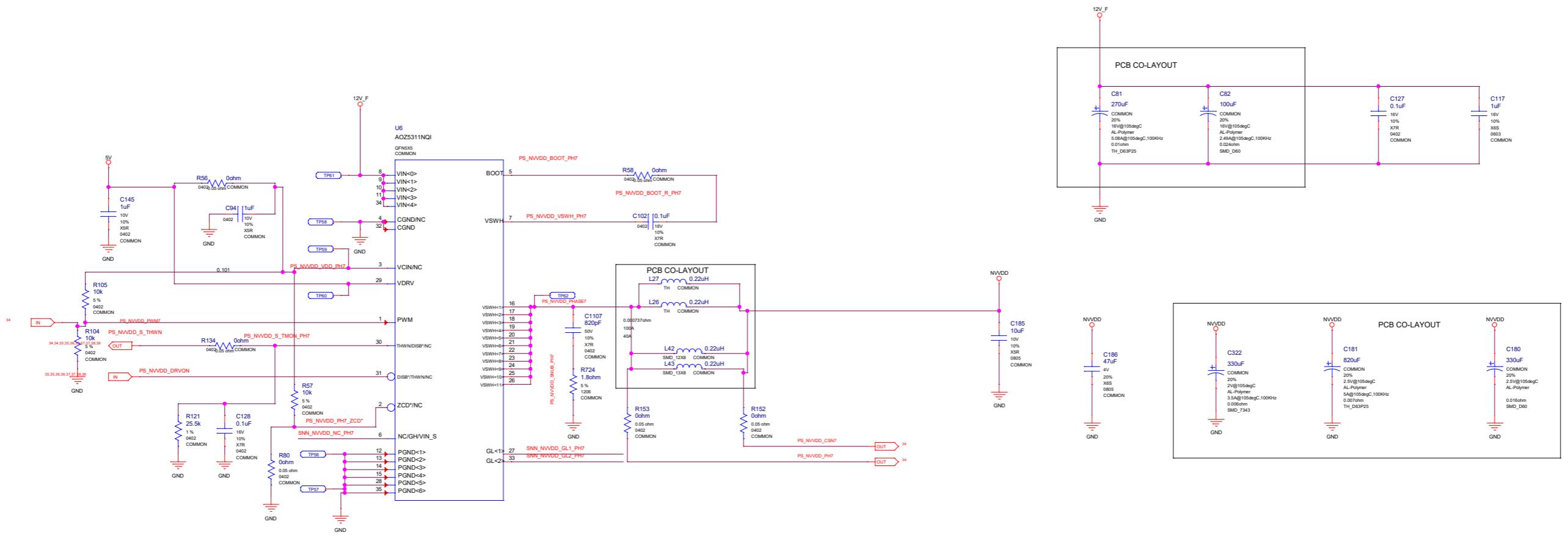
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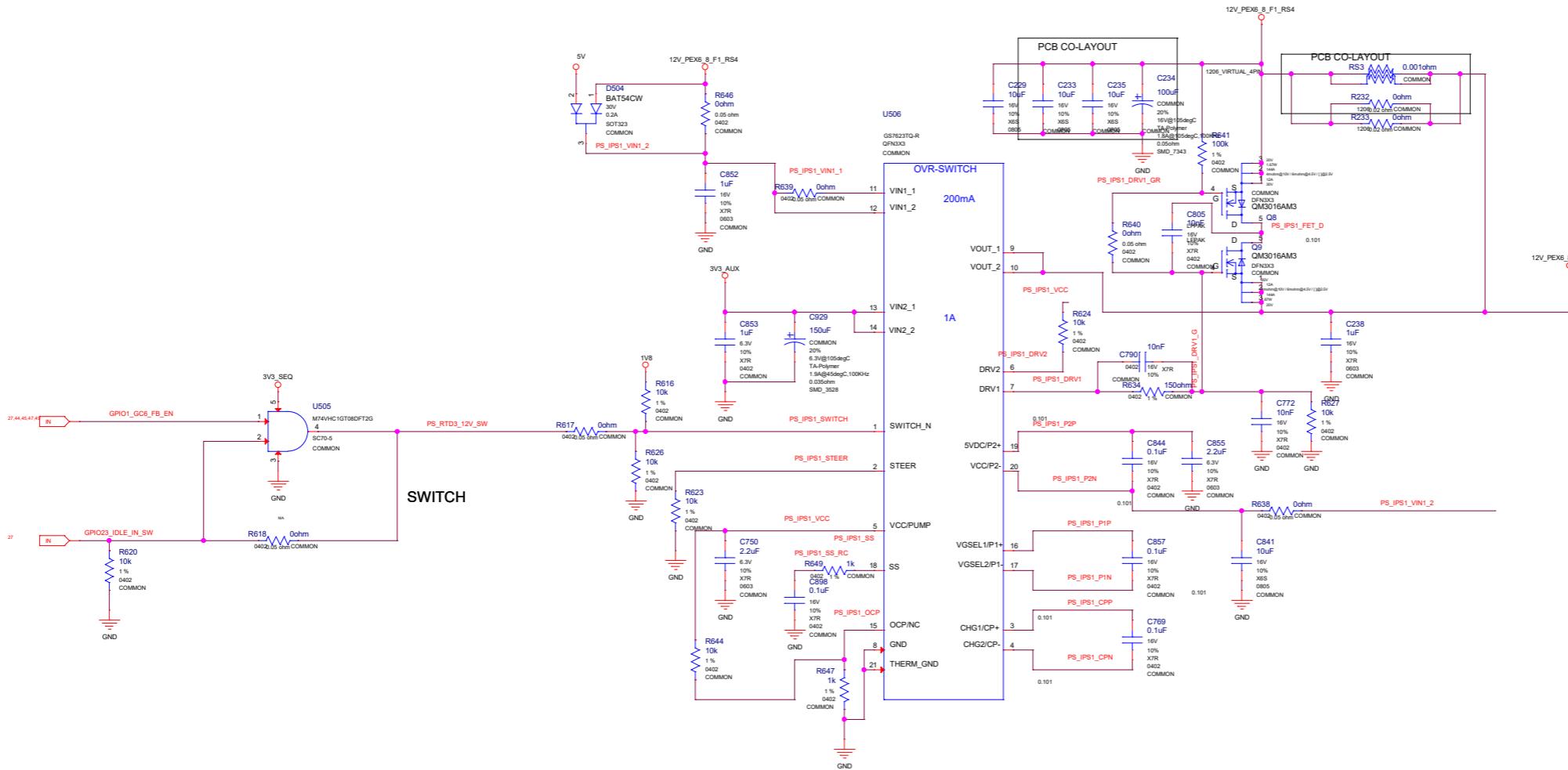
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AND GATE LOGIC			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V
0	1	0	12V
1	0	0	12V
1	1	1	3V3A



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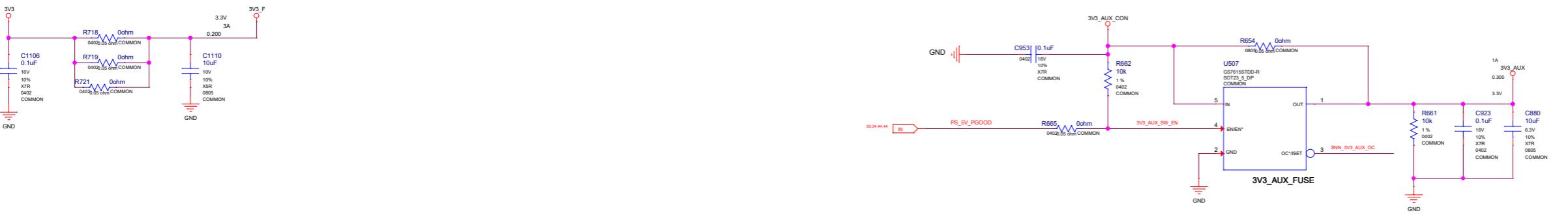
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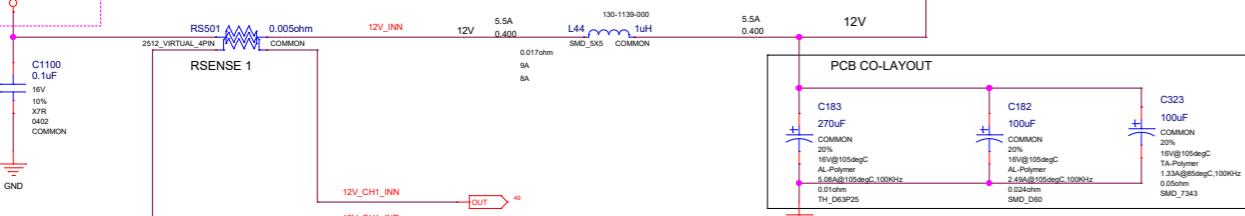
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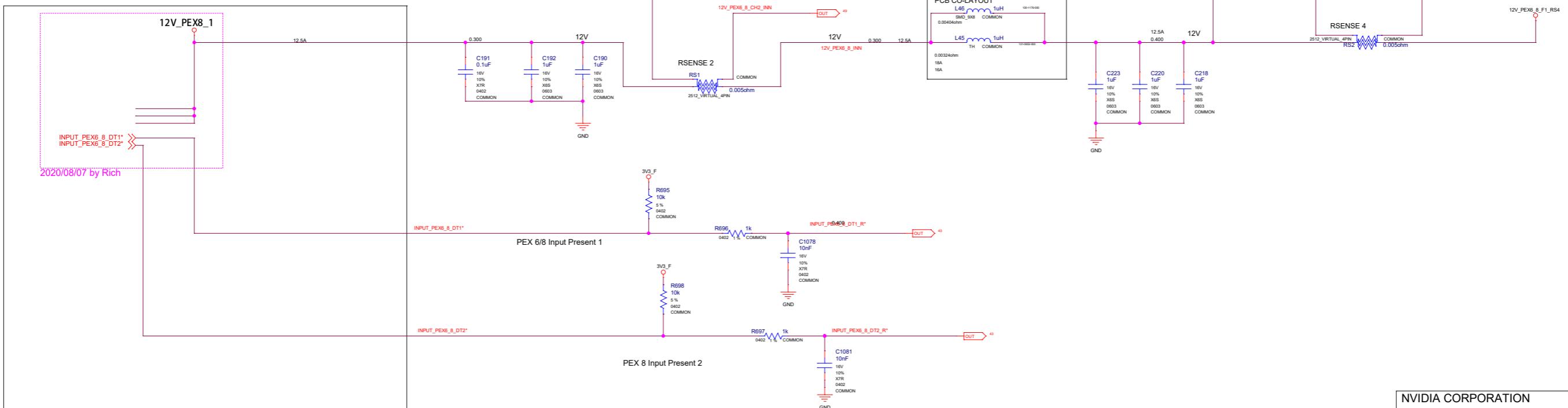


2020/08/07 by Rich

12V_FUSE PEX_12V INPUT - 66W



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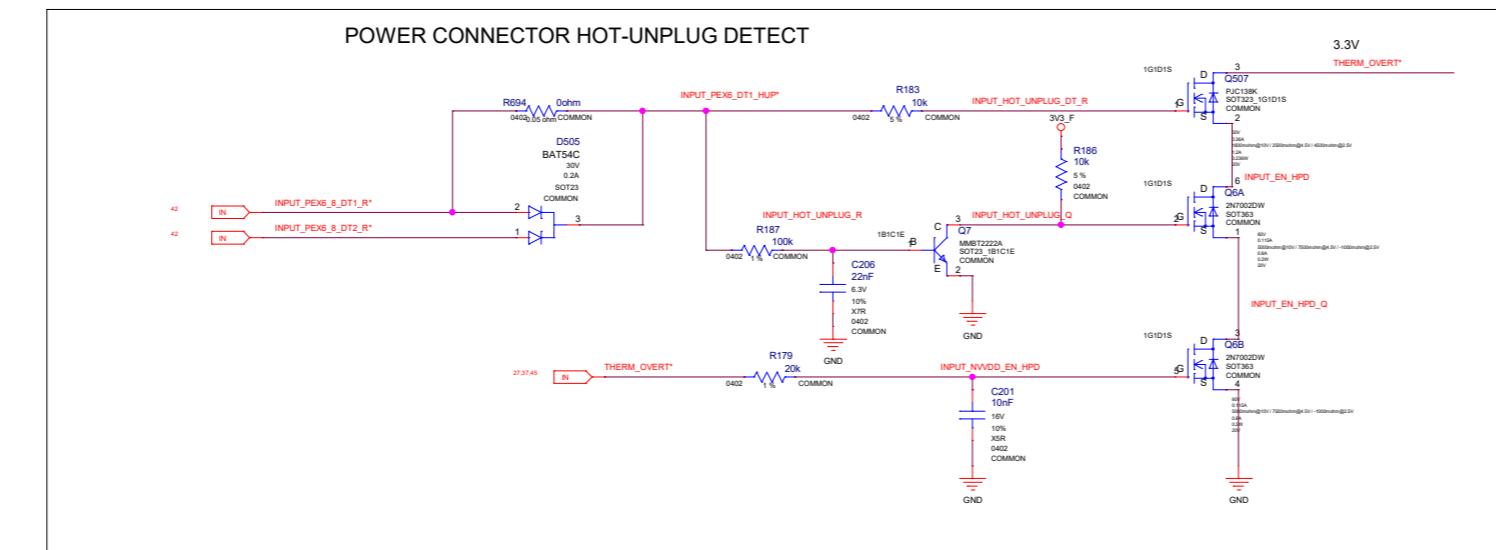


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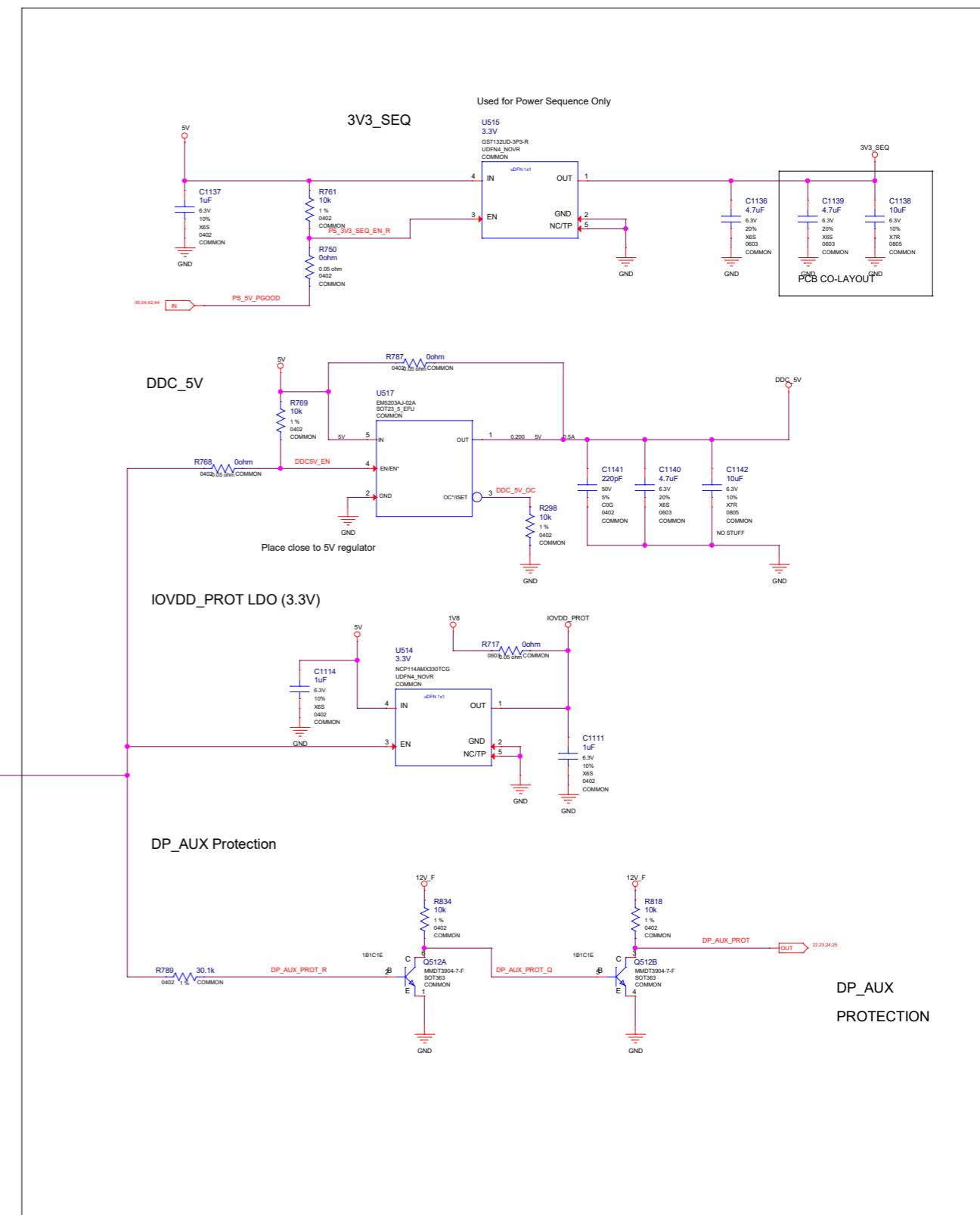
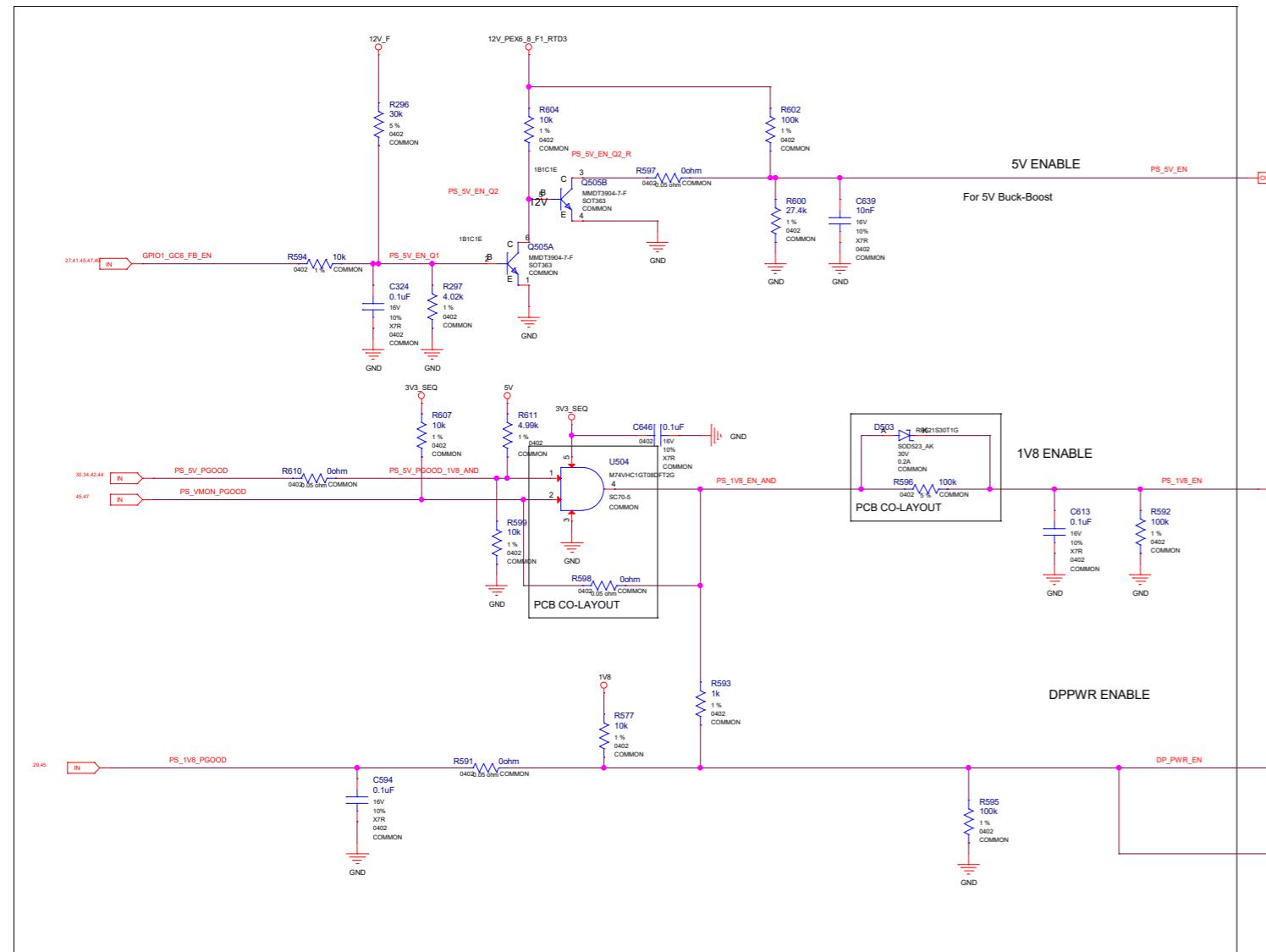


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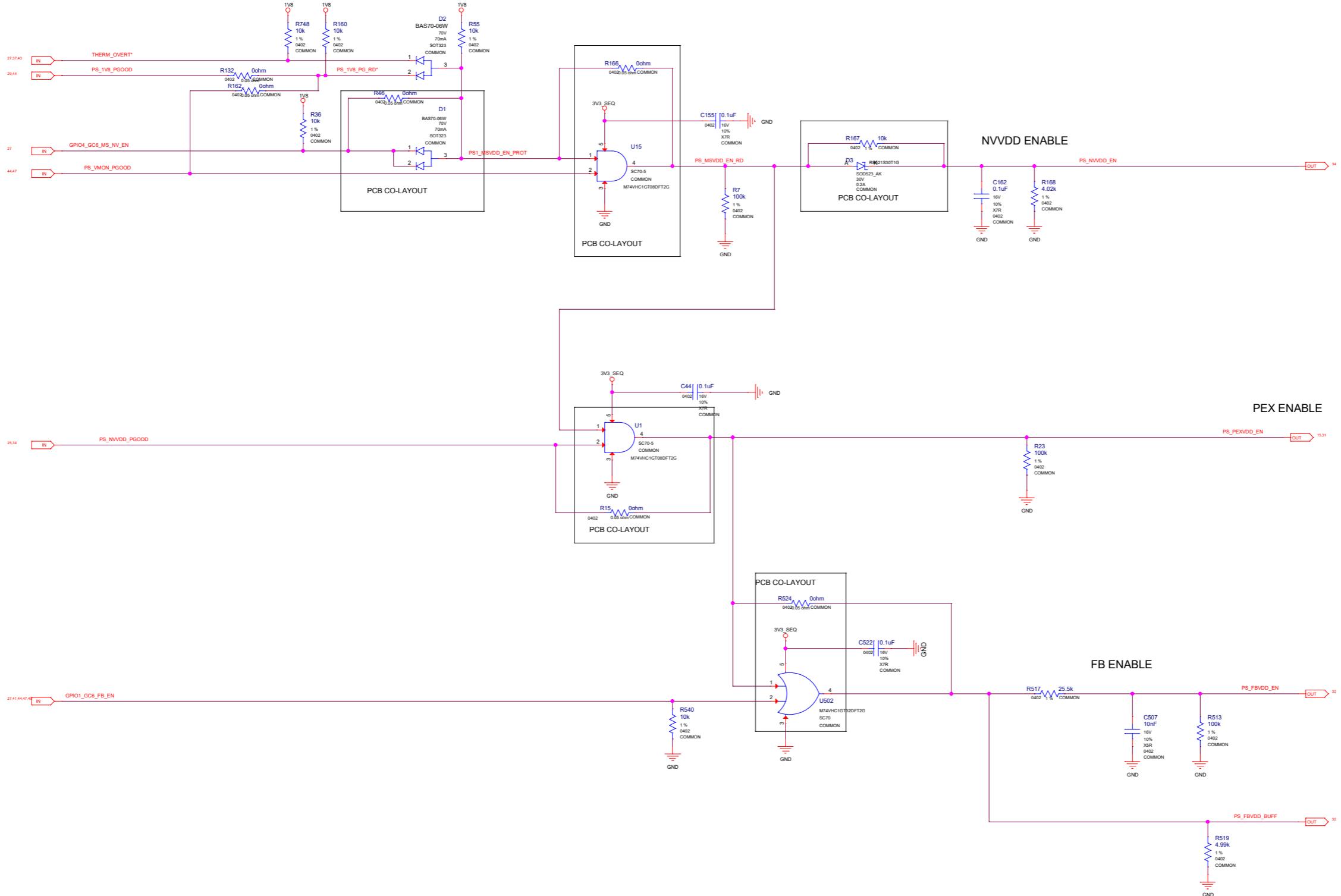
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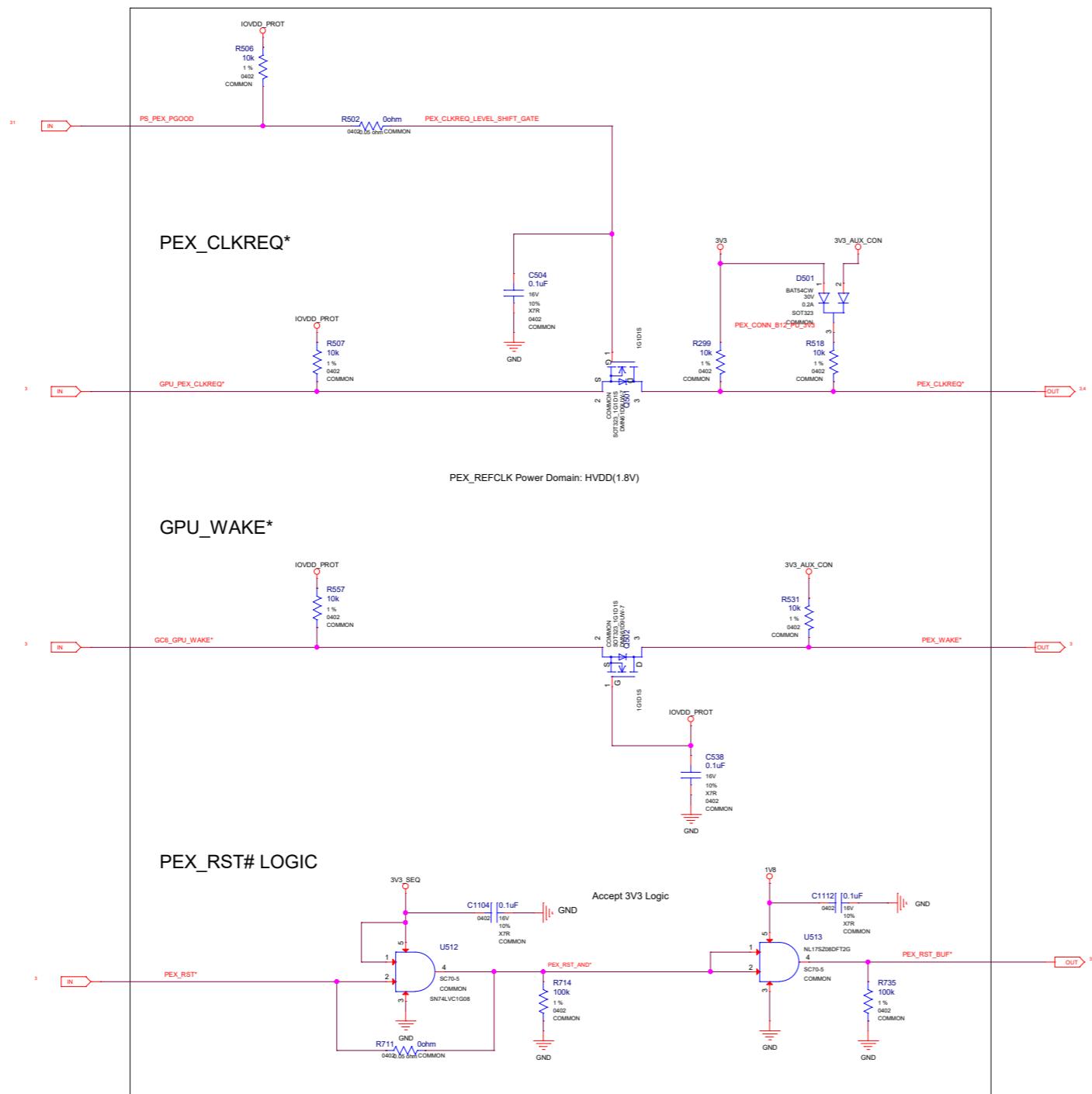
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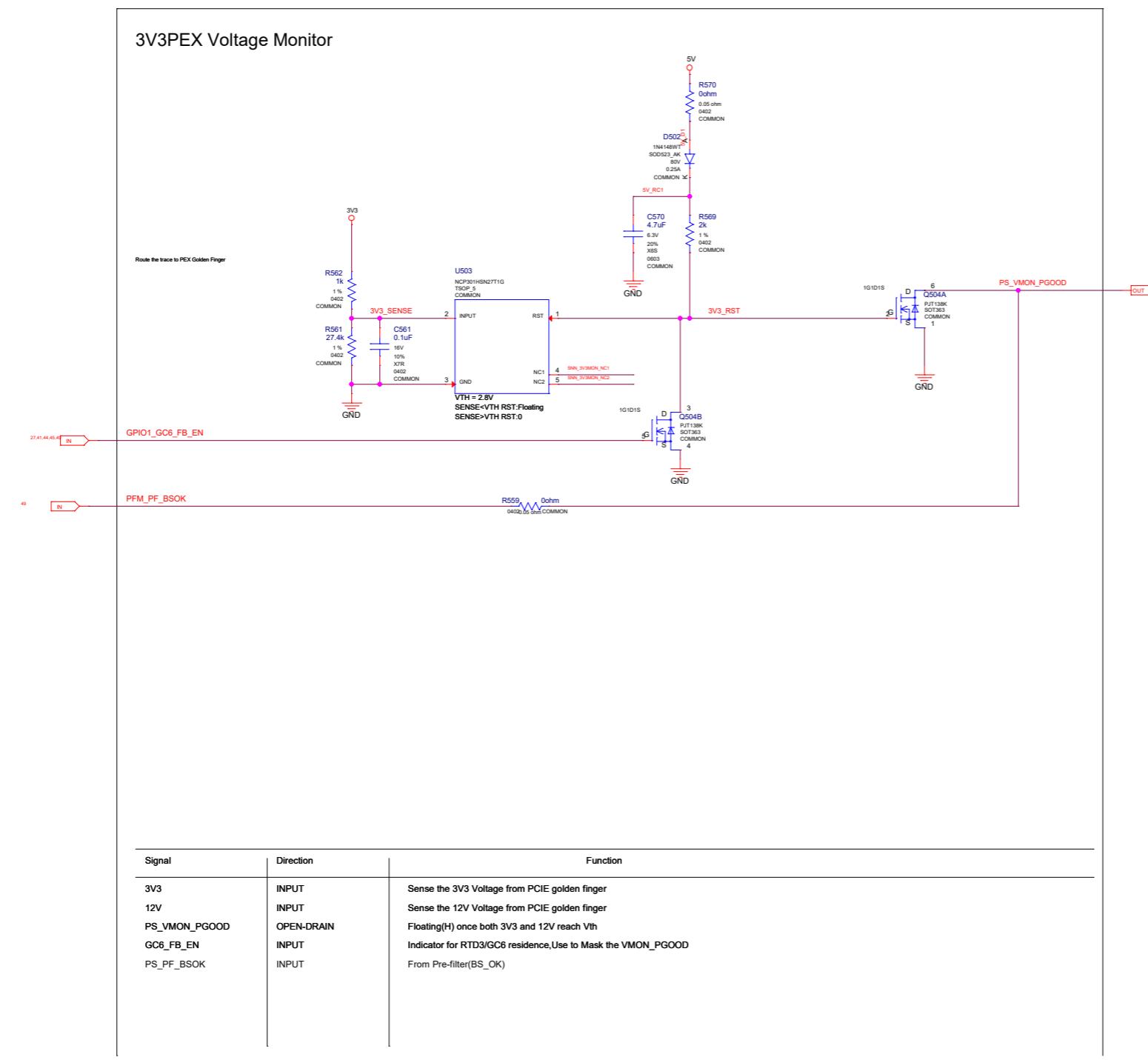
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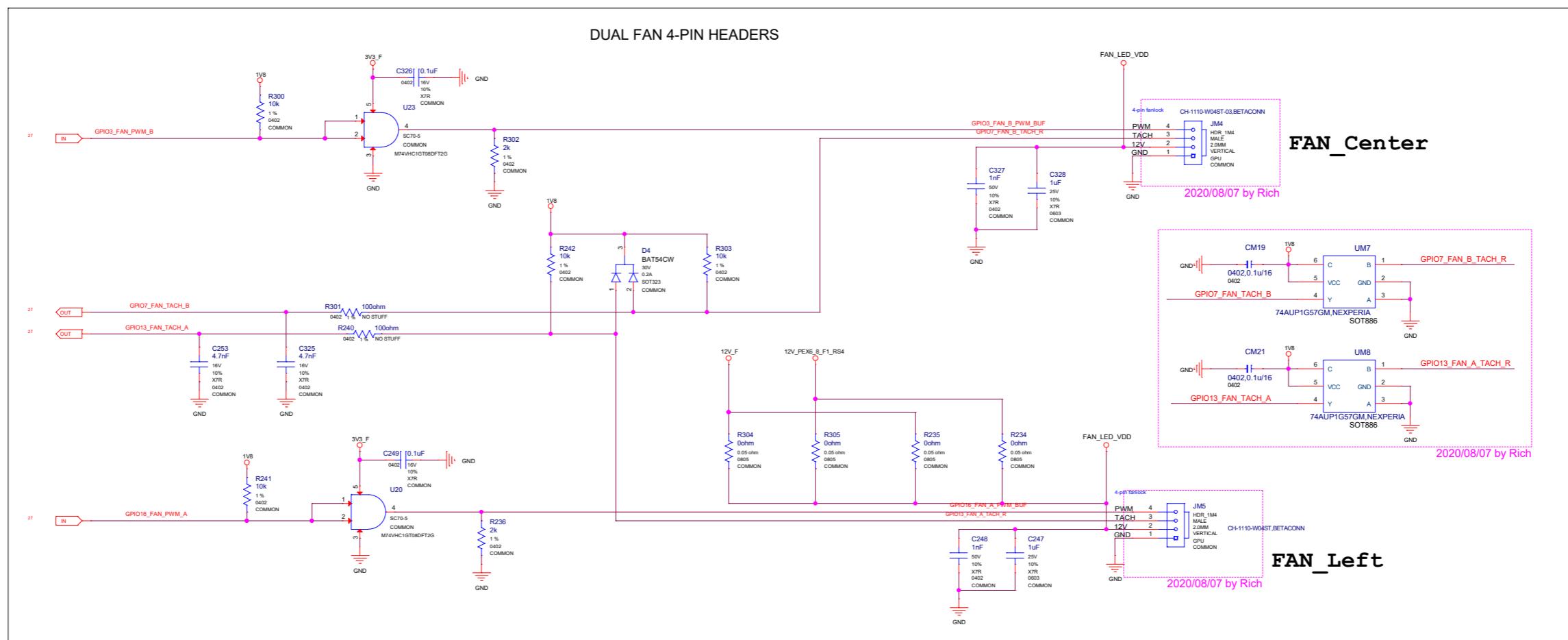
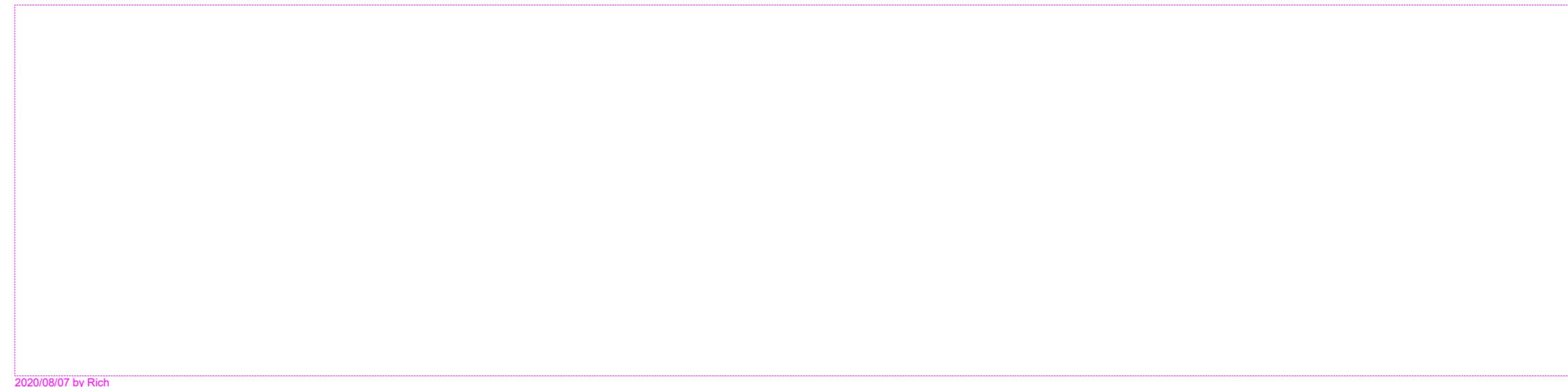
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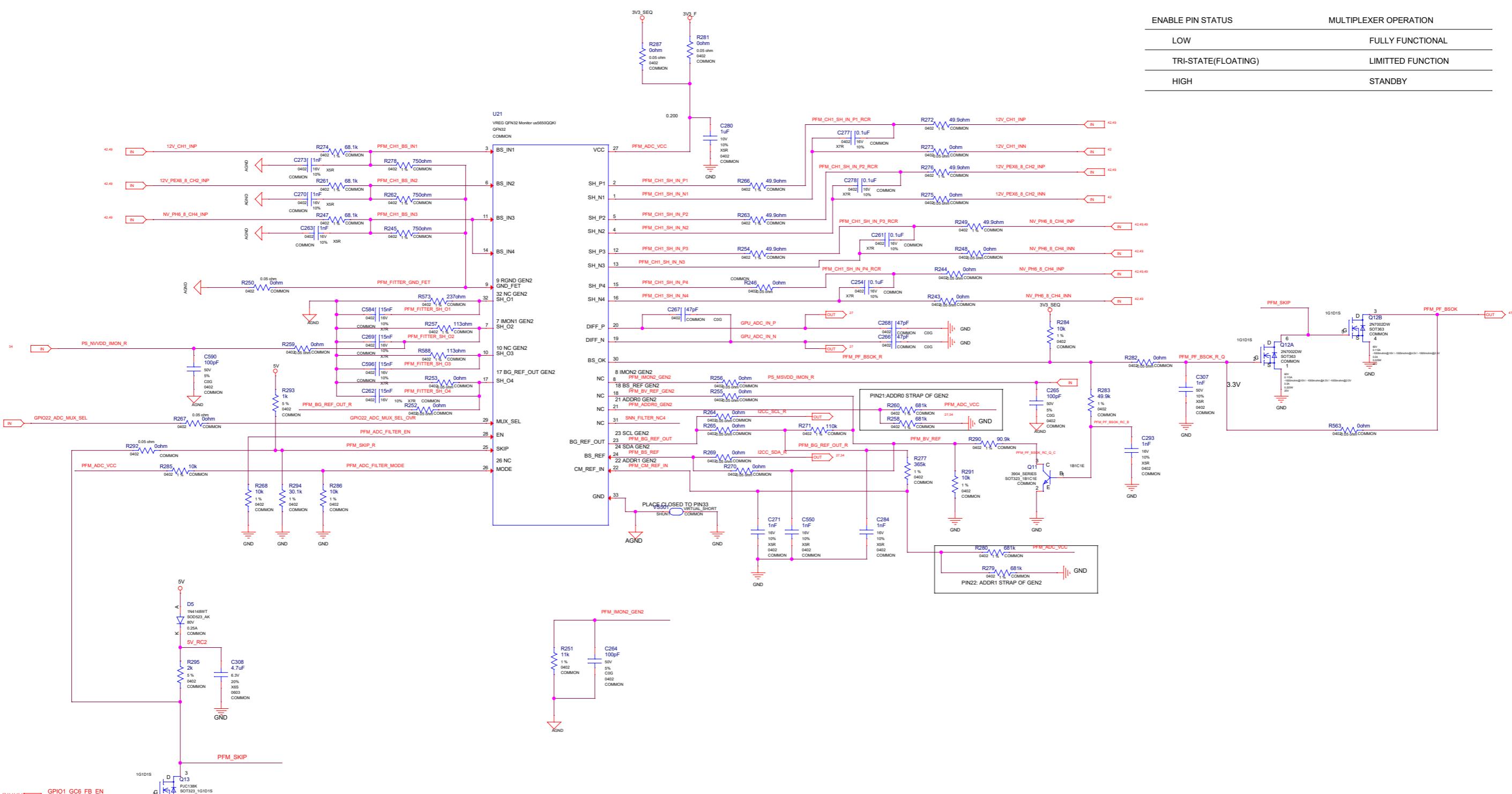
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MODE PIN STATUS		MULTIPLEXER OPERATION	
LOW	TRI-STATE(FLOATING)	DEVICE A	STAND-ALONE
HIGH		DEVICE B	
ENABLE PIN STATUS		MULTIPLEXER OPERATION	
LOW		FULLY FUNCTIONAL	
TRI-STATE(FLOATING)		LIMITED FUNCTION	
HIGH		STANDBY	



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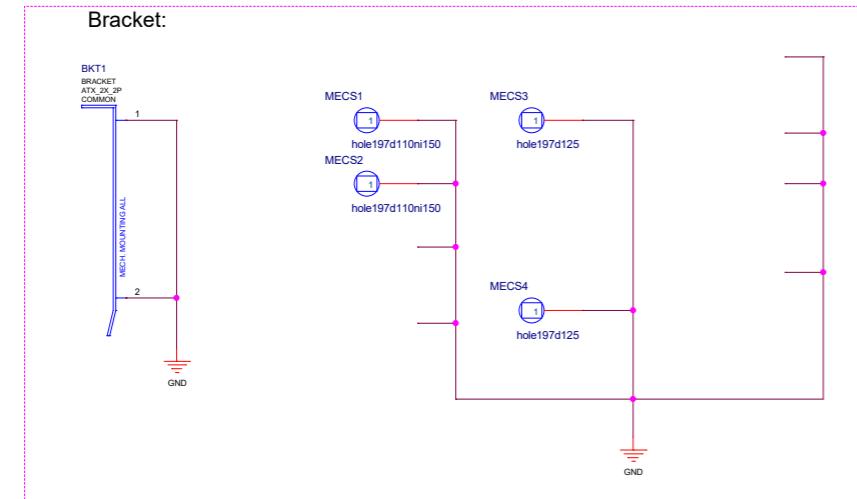
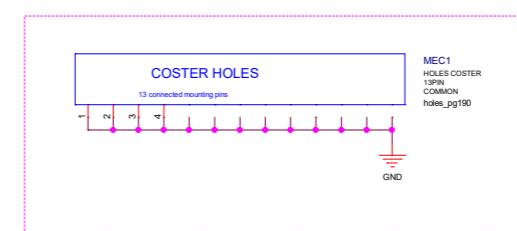
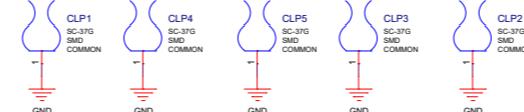
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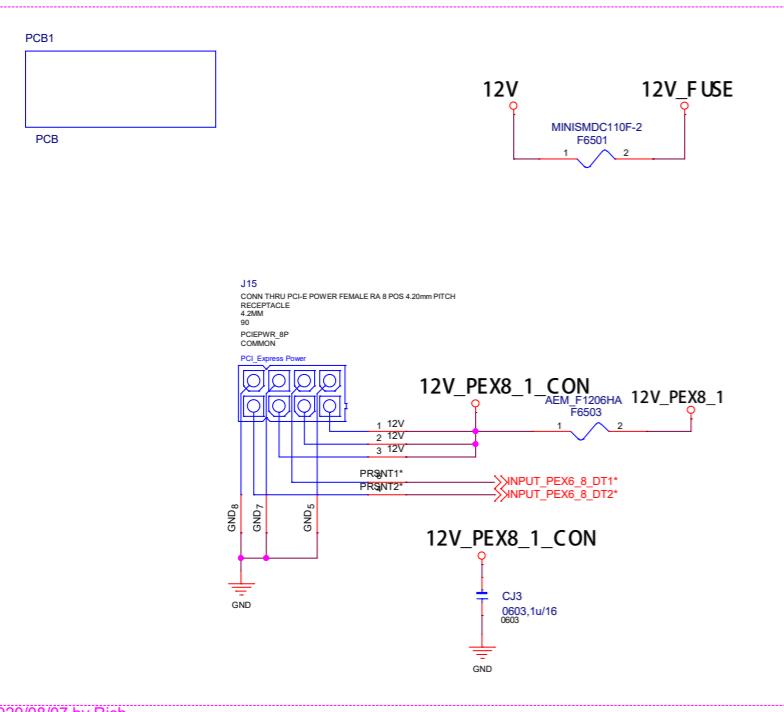
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Date: Friday, August 07, 2020	Sheet 1 of 51	

R999: History

R0.0

2020/08/07

- Page.27:** 1. Remove NV STEREO Parts
2. Remove NV J9 Parts
3. Remove NV U19 Parts

- Page.42:** 1. Move J15 to Page.R009 and change netname to 12V_PEX8_1
2. Change 12V netname to 12V_FUSE
3. Remove J8

- Page.48:** 1. Remove NV LED Parts
2. Change Fan connector J10 => JM5, J11 => JM6
3. Add filter IC UM7, UM8

- Page.50:** 1. Replace NV Brecket to EVGA
2. Modify MEC1 Pin number
3. Add hole

- Page.R009:** 1. Add fuse F6503 on PEX_8Pin
2. Add fuse F6501 on 12V

2020/08/21

- Page.32:** 1. Remove L34 / L35 / L49
2. Change L50 footprint to SMD_13X8

- Page.33:** 1. Remove L47 / L51 / L52
2. Change L48 footprint to SMD_13X8

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Date: Friday, August 21, 2020	Sheet 2 of 52	