GA102-300 GPU

New Product Notice

NPN-10043-001_v01 | xx 2020
NVIDIA CONFIDENTIAL | Prepared and Provided Under NDA

Document History

NPN-10043-001_v01

Version	Date	Authors	Description of Change
01		QL, DR	Initial release

New Product Notice

New Product Introduction

This NPN specifies the following new NVIDIA® GA102-300 GPU. This GPU is offered in the GB5-384 (3328-ball BGA, 51 mm × 51 mm) package only.

Notification	July, 2020	Planned Implementation	Per schedules below

Product Information

These new products represent the Enthusiast consumer desktop GPU segment. They are based on the new NVIDIA Ampere graphics architecture and will be manufactured using qualified suppliers per our approved suppliers' list and are RoHS and Halogen-free compliant.

Key Specifications

	GA102-300
Product Part Number	GA102-300-A1
NVIDIA Part Number (used on labels of packaging materials)	GA102-300-A1
Device ID	0x2204
Memory Interface	384-bit GDDR6X
Package	GB5-384

Impact of Change and Recommended Action

NVIDIA is committed to providing our customers with quality products that push the edge of technology and at the same time enable product segmentation. To help guarantee a rapid time-to-market launch and smooth and uninterrupted product supply, NVIDIA strongly recommends that customers qualify these GPUs as soon as possible.

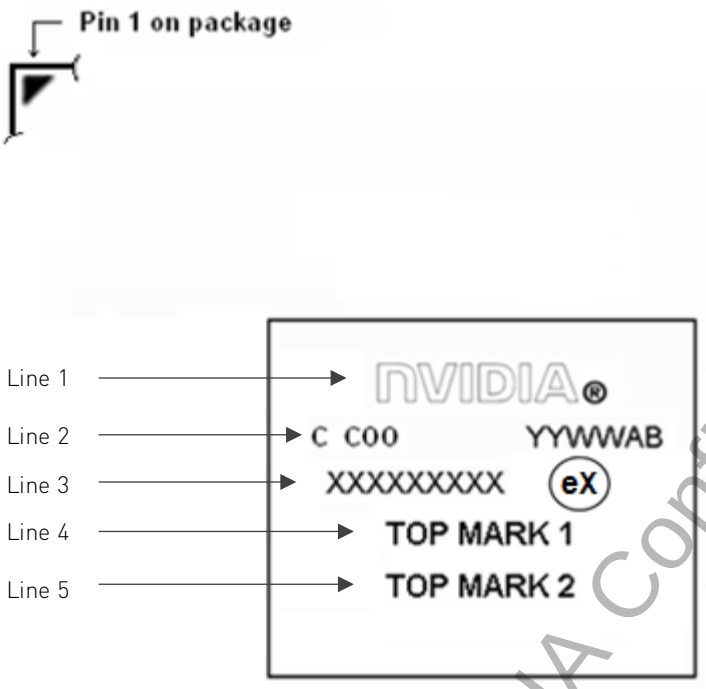
Forecasted Key Milestones

GA102-300-A1: QS ..... Mid-July, 2020

GA102-300-A1: Production ..... August, 2020

Product Marking and Traceability

GA102-300 Markings



Pin 1: Location of Pin 1 in upper left when reading the marking.

Line 1: Company Name

Line 2: Assembly information: plant identifier (C) and country of origin (COO):
- C = Plant identifier: A (ASE), B (Amkor K5), K (Amkor K4), R (ATT - Amkor Tech), S (SPIL), T (TSMC).
- COO = Country of origin: Taiwan for ASE, ATT, SPIL and TSMC, and Korea for Amkor K4 and Amkor K5.
- YYWW = Assembly date code
- AB = Mask revision

Line 3: Assembly lot number (XXXXXXXXX). The first character identifies the wafer Fab location:

eX = solder ball alloy based upon IPC/JSTD-609
e1 = SAC305

Line 4: Product Part Number, for example: XXXXX-XX-XX

Line 5: Sample level, if applicable

Products Affected/Ordering Codes

Product	Marketing Part Number for P.O.	NVIDIA Part Number[1]	Comments
GA102-300	GA102-300 -A1	GA102-300-A1	GB5-384 (3328-ball BGA, 51 mm × 51 mm)

Note:

1. The NVIDIA Part Number is provided in this document as a reference product shipping and handling at factory. This is NVIDIA confidential.

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GA102 Graphics Processing Unit

Data Sheet

DS-09809-001_v01 | July 2020
NVIDIA CONFIDENTIAL | Prepared and Provided Under NDA

Document History

DS-09809-001_v01

Version	Date	Authors	Description of Change
01	July 16, 2020	RT, SH, DR	Initial Release

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Introduction

Overview

This data sheet covers NVIDIA® Graphics Processing Unit for products listed in the title page, bringing a new level of performance and capability to visual graphics and computing applications. These GPUs support 384-bit frame buffer and 16 lanes of PCI Express GEN 4.0 interfaces.

Supported Technologies

- Direct3D 12 Ultimate and Shader Model 7.0
- OpenGL 4.6
- Vulkan 1.2
- NVIDIA® CUDA technology
- NVLink

Signal Descriptions

Overview

The signal description section contains definitions grouped under the following functions:

- "Conventions"
- "PCI Express Interface"
- "Frame Buffer Memory Interface"
- "ROM Access Signals"
- "I2C Interface"
- "Clock Reference Signals"
- "Digital Display Interface"
- "NVLink Interface"
- "Power Rail Signals"

Note: Refer to Hardware Design Guide DG-09846-001 for detailed functionality and usage.

Conventions

- The following conventions are used to describe the signals for this GPU:
- Signal names listed in the ballout are written in bold sans serif font to distinguish them from other text. Single-ended active low signals are identified by an underscore and the letter "n" (_N) after the signal. For example, PEX_TX1_N indicates an active low signal. Signal names that do not appear in the ballout, but that are used for alternate interfaces are written in sans serif font without bold.
- A full list of signals and their operational characteristics referred to as I/O state codes are provided in "GPU Signal List".

PCI Express Interface

Table 2.1 PCI Express Interface

Signal	Description
PEX_RX[15:0] PEX_RX[15:0]_N	PCI Express Receive Data Bus This is the high-speed unidirectional differential input data bus. The raw data transfer rate is: 2.5 GTs per differential pair for PCI Express 1.1, 5.0 GTs for PCI Express 2.0, 8.0 GTs for PCI Express 3.0, and 16.0 GTs for PCI Express 4.0, including the symbol overhead for an embedded clock.
PEX_TX[15:0] PEX_TX[15:0]_N	PCI Express Transmit Data Bus This is the high-speed unidirectional differential output data bus. The raw data transfer rate is: 2.5 GTs per differential pair for PCI Express 1.1, 5.0 GTs for PCI Express 2.0, 8.0 GTs for PCI Express 3.0, and 16.0 GTs for PCI Express 4.0, including the symbol overhead for an embedded clock.
PEX_REFCLK PEX_REFCLK_N	PCI Express Reference Clock The reference clock is a differential low-jitter input the GPU uses for its internal timing purposes. This input clock may be spread spectrum. Refer to the latest PCI Express specification for details on the reference clock spread spectrum.
PEX_RST_N	PCI Express Reset The PEX_RST_N signal indicates when the power supply is within its specified voltage tolerance and is stable. It goes inactive after a delay time from the power rails, achieving specified tolerance and power up. Refer to the latest PCI Express specification for details on the PCI Express reset.
PEX_TERMP	PCI Express Input/Output Termination Calibration The PEX_TERMP signal provides the reference for the internal calibation of the PCI Express input/output termination. Use a pull-down to GND that is the same value as the desired termination.
PEX_CLKREQ_N	PCI Express Clock Request This active low signal is driven to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data.
PEX_WAKE_N	PCI Express Wake Request This active low signal is driven to request that the PCI Express interfaces wakes up from a lower power state

Frame Buffer Memory Interface

This GPU frame buffer memory interface supports GDDR6 memories. Each memory partition has its own set of command signals. Refer to the Hardware Design Guide to see how the frame buffer control signals map to the memory command signals.

Table 2.2 Frame Buffer Interface

Signal	Description
FBx_CMD[55:0] (x = A,B,C,D,E,F)	Command Address Bus Inversion (CABI_n) Used to reduce power consumption on the command Address bus.
	Reset (RESET_n) Asynchronous DRAM reset signal
	Memory Clock Enable (CKE_n) Enables the clock receivers for the target RAM.
	Command Address Inputs (CA[9:0]): The CA outputs receive DDR Command and Address inputs
FBx_CLK[1:0] FBx_CLK[1:0]_N (x=A,B,C,D,E,F)	Memory Clock Signals These are separate sets of clock signals for eachmemory partition. For a further reduction in loading, there are two sets of clocks per partition. Each partition has two clock pairs that control either the most significant 32 bits or the least significant 32 bits per partition. The active low CA signals switch on the falling clock edge. The active high CA signals switch on the rising clock edge. The memory clock signals are as follows: FBx_CLK0 and FBx_CLK0_N → FBx_D[31:0] FBx_CLK1 and FBx_CLK1_N → FBx_D[63:32] x=A,B,C,D,E,F.
FBx_D[63:0] (x=A,B,C,D,E,F)	Memory Data Bus These signals connect to data signals of the memory device for each 64-bit partition.
FBx_DQM[7:0] (x=A,B,C,D,E,F)	Data Bus Inversion (DBI) FBx_DQM[7:0] signals are connected to DBI[7:0] signals of the memory. Used to reduce power consumption and VDD noise of the DRAM.
FBx_DQS_WP[7:0] (x=A,B,C,D,E,F)	Error Detection Code (EDC) FBx_DQS_WP[7:0] signals are connected to the EDC[7:0] signals of the memory. The CRC data is communicated on these signals

Table 2.2 Frame Buffer Interface (Continued)

Signal	Description
FBx_WCK01 FBx_WCK01_N FBx_WCK23 FBx_WCK23_N FBx_WCK45 FBx_WCK45_N FBx_WCK67 FBx_WCK67_N (x=A,B,C,D,E,F) FBx_WCKB01 FBx_WCKB01_N FBx_WCKB23 FBx_WCKB23_N FBx_WCKB45 FBx_WCKB45_N FBx_WCKB67 FBx_WCKB67_N (x=A,B,C,D,E,F)	Differential clocks used as the reference for read and write data latching.
FB_CAL_PD_VDDQ FB_CAL_PU_GND	Calibration Pull-Down/Pull-Up When the frame buffer bus operates in high-speed source-synchronous mode, several signals require dynamic calibration. Other slower signals are calibrated once on power-up. FB_CAL_PD_VDDQ and FB_CAL_PU_ GND are used to compute the drive strength of the frame buffer pads. FB_CAL_PD_VDDQ connects to FBVDDQ and is pulled up through a precision resistor. FB_CAL_PU_GND is pulled down to GND through a precision resistor.
FB_CAL_TERM_GND	Termination Calibration Signal When the frame buffer bus operates in high-speed source-synchronous mode, it may use internal termination provided by the GPU. This signal provides the calibration for the internal termination. It should be tied to GND through a precision resistor that is the same value as the desired termination.
FB_VREF	Frame Buffer Voltage Reference Sets switching threshold for inputs on the frame buffer when the frame buffer input pads are set to input mode. This signal also functions as inbound read calibration. Follow design guide for proper connection.
FBVDDQ_SENSE	Frame Buffer Power Rail Sense Signal.
FB_GND_SENSE	Frame Buffer Ground Sense Signal.

ROM Access Signals

Table 2.3 ROM Access Signals

Signal	Description
ROM_SCLK	Serial ROM Clock ROM_SCLK supplies the clock signal for accessing serial ROM data.
ROM_CS_N	Chip Select.
ROM_SI	Serial Output ROM_SI supplies the data signal to the SROM_SI serial ROM signal.
ROM_SO	Serial Input ROM_SO accepts the data signal input from SROM_SO of the serial ROM as input.

I2C Interface

Table 2.4 I2C Interface Signals

Signal	Description
I2CB_SCL I2CB_SDA	If not used for any external Bus, this bus may be used for embedded devices.
I2CC_SCL I2CC_SDA	Restricted to embedded devices such as voltage regulators and power monitors.
I2CS_SCL I2CS_SDA	Slave I2C-Compatible Bus Signal.

Clock Reference Signals

Table 2.5 Clock Reference Signals

Signal	Description
XTAL_IN XTAL_OUT	A series resonant crystal is connected between these two points to provide the reference clock for the internal clock synthesizers. Alternately, an external LVTTL clock oscillator output may be driven in XTAL_IN, leaving XTAL_OUT unconnected.
XTAL_OUTBUFF	XTAL_OUTBUFF is a buffered version of the XTAL_IN/ XTAL_OUT. Used as a strap to set the fan PWM.
EXT_REFCLK_FL	EXT_REFCLK_FL

Digital Display Interface

This GPU enables Links A, B, C, D, E, and F to support DisplayPort. Links can also be configured to support DVI and HDMI.

Table 2.6 Digital Display Interface Signals, Links A, B, C, D, E, and F

Signal	Description
IFPA_AUX_SCL/ IFPA_AUX_SDA_N	DisplayPort Auxiliary Lane (Link A)
IFPA_L0/IFPA_L0_N	DisplayPort Main Link Lane 0 (Link A)
IFPA_L1/IFPA_L1_N	DisplayPort Main Link Lane 1 (Link A)
IFPA_L2/IFPA_L2_N	DisplayPort Main Link Lane 2 (Link A)
IFPA_L3/IFPA_L3_N	DisplayPort Main Link Lane 3 (Link A)
IFPB_AUX_SCL IFPB_AUX_SDA_N	DisplayPort Auxiliary Lane (Link B)
IFPB_L0/IFPB_L0_N	DisplayPort Main Link Lane 0 (Link B)
IFPB_L1/IFPB_L1_N	DisplayPort Main Link Lane 1 (Link B)
IFPB_L2/IFPB_L2_N	DisplayPort Main Link Lane 2 (Link B)
IFPB_L3/IFPB_L3_N	DisplayPort Main Link Lane 3 (Link B)
IFPAB_RSET	Set Reference Current Generate a reference current through connecting an external resistor to this signal.
IFPC_AUX_SCL / IFPC_AUX_SDA_N	DisplayPort Auxiliary Lane (Link C)
IFPC_L0/IFPC_L0_N	DisplayPort Main Link Lane 0 (Link C)
IFPC_L1/IFPC_L1_N	DisplayPort Main Link Lane 1 (Link C)
IFPC_L2/IFPC_L2_N	DisplayPort Main Link Lane 2 (Link C)
IFPC_L3/IFPC_L3_N	DisplayPort Main Link Lane 3 (Link C)
IFPCD_RSET	Set Reference Current. Generates a reference current through connecting an external resistor to this signal.
IFPD_AUX_SCL/ IFPD_AUX_SDA_N	DisplayPort Auxiliary Lane (Link D)
IFPD_L0/IFPD_L0_N	DisplayPort Main Link Lane 0 (Link D)
IFPD_L1/IFPD_L1_N	DisplayPort Main Link Lane 1 (Link D)
IFPD_L2/IFPD_L2_N	DisplayPort Main Link Lane 2 (Link D)
IFPD_L3/IFPD_L3_N	DisplayPort Main Link Lane 3 (Link D)
IFPE_AUX_SCL/ IFPE_AUX_SDA_N	DisplayPort Auxiliary Lane (Link E)
IFPE_L0/IFPE_L0_N	DisplayPort Main Link Lane 0 (Link E)

Table 2.6 Digital Display Interface Signals, Links A, B, C, D, E, and F (Continued)

Signal	Description
IFPE_L1/IFPE_L1_N	DisplayPort Main Link Lane 1 (Link E)
IFPE_L2/IFPE_L2_N	DisplayPort Main Link Lane 2 (Link E)
IFPE_L3/IFPE_L3_N	DisplayPort Main Link Lane 3 (Link E)
IFPEF_RSET	Set Reference Current. Generates a reference current through connecting an external resistor to this signal
IFPF_AUX_SCL/ IFPF_AUX_SDA_N	DisplayPort Auxiliary Lane (Link F)
IFPF_L0/IFPF_L0_N	DisplayPort Main Link Lane 0 (Link F);
IFPF_L1/IFPF_L1_N	DisplayPort Main Link Lane 1 (Link F)
IFPF_L2/IFPF_L2_N	DisplayPort Main Link Lane 2 (Link F)
IFPF_L3/IFPF_L3_N	DisplayPort Main Link Lane 3 (Link F)

NVLink Interface

Table 2.7 lists the PCI Express codes used in the signal description tables

Table 2.7 NVLink Interface

Signal	Description
NVHSx_y_RXz NVHS_x_y_RXz_N (x=0; y=0,1,2,3, z=0,1,2,3)	NVLink Receive Data Bus. This is the high-speed unidirectional differential input data bus. The raw data rate is 2.5 Gbps per differential pair.
NVHSx_y_TXz NVHS_x_y_TXz_N (x=0; y=0,1,2,3, z=0,1,2,3)	NVLink Receive Data Bus. This is the high-speed unidirectional differential input data bus. The raw data rate is 2.5 Gbps per differential pair.
NVHS_REFCLK NVHS_REFCLK_N	NVLink Reference Clock. The reference clock is a differential low-jitter input the GPU uses for its internal timing purposes. Refer to the latest NVIDIA NVLink specification for details.
NVHS_TERMP	NVLink Input/Output Termination Calibration. The NVHSx_TERMP signal provides the reference for the internal calibration of the NVLink input/output termination. Refer to the NVIDIA Hardware Design Guide for the recommended resistor value.

Power Rail Signals

IFP Power Rail Signals

Table 2.8 IFP Power Rail Signals

Signal	Description
IFP_IOVDD	0.95V supply for integrated Digital Display I/O Power Rails for all IFP links.
IFPAB_PLLVDD	1.8V supply for integrated Digital Display PLL Power Rails for the IFP-A and IFP-B links.
IFPCD_PLLVDD	1.8V supply for Integrated Digital Display PLL Power Rails for the IFP-C and IFP-D links.
IFPEF_PLLVDD	1.8V supply for Integrated Digital Display PLL Power Rails for the IFP-E link.

PEX Power Rail Signals

Table 2.9 PEX Power Rail Signals

Signal	Description
PEX_CVDD / PEX_DVDD	0.95V supply for PCIe interface/PLL digital power rail
PEX_CVDD_SENSE	PCIe 0.95V power supply rail sense signal
PEX_HVDD	1.8V supply for PCIe interface/PLL analog power rail
PEX_PLL_HVDD	1.8V supply for the PEX PLL

Frame Buffer Power Rail Signals

Table 2.10 Frame Buffer Power Rail Signals

Signal	Description
FB_PLLVDD	1.8V supply for Frame Buffer Digital Power Rails
FBVDDQ	Frame Buffer Power Rail
FBVDDQ_SENSE	Frame Buffer Power Rail Sense Signal

NVLink Rail Signals

Table 2.11 NVLink Rail Signals

Signal	Description
NVHS_CVDD / NVHS_DVDD	0.95V supply for NVLink Internal Core Power Rail
NVHS_HVDD	1.8V supply for NVLink High Voltage Power Rail
NVHS0_PLL_HVDD	1.8V supply for NVLink PLL Power Rail

General Power Rail Signals

Table 2.12 General Power Rail Signals

Signal	Description
1V8	1.8V Power Rail
CORE_PLL_AVDD	Core PLL Analog Power Rail
GPCADC_AVDD	1.8V supply for Analog Power Rails for GPCs
SP_PLLVDD	1.8V supply for Core Clock PLL Analog Power Rail
VDD	Core Power Rail. Connect to NVVDD power supply
VDD_SENSE	Core Power NVVDD rail sense signal
VDDMS	Core Power Rail for NVVDD/MSVDD power rail
VDDMS_SENSE	Core Power sense signal for NVVDD/MSVDD
VID_PLLVDD	1.8V supply for Video Pixel Clock PLL Analog power rail

Test Signals

Table 2.13 Test Signals

Signal	Description
JTAG_TCK JTAG_TDI JTAG_TD0 JTAG_TMS	JTAG test signals
NVJTAG_SEL	JTAG select

Miscellaneous Signals

Table 2.14 Miscellaneous Signals

Signal	Description
STRAP[5:0]	Strap signals
THERMDP THERMDN	Thermal Monitor Signals Leave floating and unconnected.
ADC_IN / ADC_IN_N	External current sense for power monitoring
GPIO [35:0]	General Purpose I/O

Electrical Specifications

This section provides absolute maximum ratings, operating conditions and GPIO electrical specifications for GPU products covered by this data sheet.

For more information about the core graphics voltage, frame buffer clock frequency, and core clock frequency values and electrical and thermal design guidelines for these products, refer to the SKU specific Electrical and Thermal Design Guidelines.

Table 3.1 Power Rail Operating Range and Absolute Max Limits

Power Rail	Description of Power Rail	Operating Conditions range			Absolute Max Ratings	
		Min (V)	Typ (V)	Max (V)[1]	Min (V)	Max (V)[2]
1V8	1.8 V power	1.692	1.8	1.908	-0.3	1.98
CORE_PLL_AVDD	Core PLL Analog	1.692	1.8	1.908	-0.3	1.98
FB_PLLVDD	Frame buffer PLL analog	1.692	1.8	1.908	-0.3	1.98
FBVDDQ[3]	Frame buffer power	1.08	1.35	1.485	-0.3	1.485
GPCADC_AVDD	Core PLL Analog	1.692	1.8	1.908	-0.3	1.98
IFP_IOVDD	Integrated Digital Display I/O power	0.9	0.95	1	-0.3	1.05
IFPAB_PLLVDD	Integrated Digital Display PLL power	1.692	1.8	1.908	-0.3	1.98
IFPCD_PLLVDD	Integrated Digital Display PLL power	1.692	1.8	1.908	-0.3	1.98
IFPEF_PLLVDD	Integrated Digital Display PLL power	1.692	1.8	1.908	-0.3	1.98
NVHS_CVDD	NVLink Internal Core Power	0.9	0.95	1	-0.3	1.05
NVHS_DVDD	NVLink Internal Core Power	0.9	0.95	1	-0.3	1.05
NVHS_HVDD	NVLink High Voltage Power	1.692	1.8	1.908	-0.3	1.98
NVHS0_PLL_HVDD	NVLink PLL Power	1.692	1.8	1.908	-0.3	1.98
PEX_CVDD	PCIe interface/PLL digital power	0.9	0.95	1	-0.3	1.05
PEX_DVDD	PCIe interface/PLL digital power	0.9	0.95	1	-0.3	1.05
PEX_HVDD	PCIe interface/PLL analog power	1.692	1.8	1.908	-0.3	1.98
PEX_PLL_HVDD	PCIe interface PLL supply power	1.692	1.8	1.908	-0.3	1.98
SP_PLLVDD	Core clock PLL analog power	1.692	1.8	1.908	-0.3	1.98
VDD	Core power (NVVDD)	-2.5%	NVVDD[4]	+2.5%	-0.3	1.2
VDDMS	Core power (NVVDD/MSVDD)	-2.5%	NVVDD[4]	+2.5%	-0.3	1.2
VID_PLLVDD	Thermal controller/Pixel CLK PLL power	1.692	1.8	1.908	-0.3	1.98

[1]This specification defines the goals for the DC supply at VDD. Short pulses due to switching noise on VDD may exceed this limit.

[2]Stress greater than those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[3] Min/Typ/Max/ should meet memory vendor specification.

[4]NVVDD power rail voltage varies during normal operation of the GPU, this range can be found in the SKU specific Electrical and Thermal Design Guidelines.

Table 3.2 GPIO Electrical Specifications

Voh,Vih/min	Voh,Vih/max	Vol,Vil/min	Vol,Vil/max	Vi_mid max	Vi_mid min
1.50V	1.854V	0V	0.3V	0.8V	1.3V

GPU Signal List

This section contains the GPU signal list with I/O function and ball number for reference to location on the Ball Map. Refer to section "Ball Map" for more information.

Table 4.1 GPU Signal List I/O Key

B = Bidirectional signal
I = Input signal
O = Output signal
P = Power-related signal
Z= Tri-state output
AI = Analog input signal
AO = Analog output signal
NC = No Connect
RSVD = Reserved

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
1V8	BK14	P	+1.8V
1V8	BL13	P	+1.8V
1V8	BL14	P	+1.8V
1V8	BM14	P	+1.8V
ADC_IN	CB13	AI	-
ADC_IN_N	CA13	AI	-
CORE_PLL_AVDD	BK31	P	-
EXT_REFCLK_FL	BU10	I	+1.8V
EXT_REFCLK_SLI	BR8	B	-
FB_CAL_PD_VDDQ	N51	AI	FBVDDQ
FB_CAL_PU_GND	M50	AI	FBVDDQ
FB_CAL_TERM_GND	M49	AI	FBVDDQ
FB_GND_SENSE	G58	P	-
FB_PLLVDD	AE14	P	-
FB_PLLVDD	AF49	P	-
FB_PLLVDD	BA14	P	-
FB_PLLVDD	BF49	P	-
FB_PLLVDD	N26	P	-
FB_PLLVDD	N38	P	-
FB_PLLVDD	N47	P	-
FB_PLLVDD	U49	P	-
FB_PLLVDD	W14	P	-
FB_VREF	K52	AI	FBVDDQ
FBA_CLK0	BJ53	O	FBVDDQ
FBA_CLK0_N	BJ52	O	FBVDDQ
FBA_CLK1	BK52	O	FBVDDQ
FBA_CLK1_N	BK53	O	FBVDDQ
FBA_CMD0	BF60	O	FBVDDQ
FBA_CMD1	BF62	O	FBVDDQ
FBA_CMD10	BK61	O	FBVDDQ
FBA_CMD11	BL62	O	FBVDDQ
FBA_CMD12	BM60	O	FBVDDQ
FBA_CMD13	BM62	O	FBVDDQ
FBA_CMD14	BM61	O	FBVDDQ
FBA_CMD15	BN62	O	FBVDDQ
FBA_CMD16	BN61	O	FBVDDQ
FBA_CMD17	BP62	O	FBVDDQ
FBA_CMD18	BR61	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBA_CMD19	BR62	O	FBVDDQ
FBA_CMD2	BF61	O	FBVDDQ
FBA_CMD20	BR60	O	FBVDDQ
FBA_CMD21	BT62	O	FBVDDQ
FBA_CMD22	BT61	O	FBVDDQ
FBA_CMD23	BU62	O	FBVDDQ
FBA_CMD24	BV61	O	FBVDDQ
FBA_CMD25_NC	BV62	NC	-
FBA_CMD26_NC	BV60	NC	-
FBA_CMD27	BA50	O	FBVDDQ
FBA_CMD28	CB48	O	FBVDDQ
FBA_CMD29	CA49	O	FBVDDQ
FBA_CMD3	BG62	O	FBVDDQ
FBA_CMD30	CB49	O	FBVDDQ
FBA_CMD31	CA50	O	FBVDDQ
FBA_CMD32	CB50	O	FBVDDQ
FBA_CMD33	BY50	O	FBVDDQ
FBA_CMD34	CB51	O	FBVDDQ
FBA_CMD35	CA52	O	FBVDDQ
FBA_CMD36	CB52	O	FBVDDQ
FBA_CMD37	CA53	O	FBVDDQ
FBA_CMD38	CB53	O	FBVDDQ
FBA_CMD39	BY53	O	FBVDDQ
FBA_CMD4	BG61	O	FBVDDQ
FBA_CMD40	CB54	O	FBVDDQ
FBA_CMD41	CA55	O	FBVDDQ
FBA_CMD42	CB55	O	FBVDDQ
FBA_CMD43	CA56	O	FBVDDQ
FBA_CMD44	CB56	O	FBVDDQ
FBA_CMD45	CA57	O	FBVDDQ
FBA_CMD46	CB57	O	FBVDDQ
FBA_CMD47	CA58	O	FBVDDQ
FBA_CMD48	CB58	O	FBVDDQ
FBA_CMD49	CA59	O	FBVDDQ
FBA_CMD5	BH62	O	FBVDDQ
FBA_CMD50	CA60	O	FBVDDQ
FBA_CMD51	BY60	O	FBVDDQ
FBA_CMD52	BW60	O	FBVDDQ
FBA_CMD53_NC	BY61	NC	-
FBA_CMD54_NC	BW61	NC	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBA_CMD55	BL47	O	FBVDDQ
FBA_CMD6	BJ60	O	FBVDDQ
FBA_CMD7	BJ62	O	FBVDDQ
FBA_CMD8	BJ61	O	FBVDDQ
FBA_CMD9	BK62	O	FBVDDQ
FBA_D0	BG55	B	FBVDDQ
FBA_D1	BJ57	B	FBVDDQ
FBA_D10	BF57	B	FBVDDQ
FBA_D11	BD58	B	FBVDDQ
FBA_D12	BD53	B	FBVDDQ
FBA_D13	BD55	B	FBVDDQ
FBA_D14	BC52	B	FBVDDQ
FBA_D15	BF54	B	FBVDDQ
FBA_D16	BT58	B	FBVDDQ
FBA_D17	BN55	B	FBVDDQ
FBA_D18	BR57	B	FBVDDQ
FBA_D19	BM55	B	FBVDDQ
FBA_D2	BF52	B	FBVDDQ
FBA_D20	BU58	B	FBVDDQ
FBA_D21	BT59	B	FBVDDQ
FBA_D22	BU60	B	FBVDDQ
FBA_D23	BV59	B	FBVDDQ
FBA_D24	BK55	B	FBVDDQ
FBA_D25	BK57	B	FBVDDQ
FBA_D26	BK58	B	FBVDDQ
FBA_D27	BK54	B	FBVDDQ
FBA_D28	BM57	B	FBVDDQ
FBA_D29	BN57	B	FBVDDQ
FBA_D3	BG57	B	FBVDDQ
FBA_D30	BN58	B	FBVDDQ
FBA_D31	BN60	B	FBVDDQ
FBA_D32	BP50	B	FBVDDQ
FBA_D33	BN50	B	FBVDDQ
FBA_D34	BU49	B	FBVDDQ
FBA_D35	BP52	B	FBVDDQ
FBA_D36	BN49	B	FBVDDQ
FBA_D37	BR49	B	FBVDDQ
FBA_D38	BU50	B	FBVDDQ
FBA_D39	BR52	B	FBVDDQ
FBA_D4	BG53	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBA_D40	BV49	B	FBVDDQ
FBA_D41	BN46	B	FBVDDQ
FBA_D42	BU47	B	FBVDDQ
FBA_D43	BR46	B	FBVDDQ
FBA_D44	BY49	B	FBVDDQ
FBA_D45	BV46	B	FBVDDQ
FBA_D46	BU46	B	FBVDDQ
FBA_D47	BP47	B	FBVDDQ
FBA_D48	BT55	B	FBVDDQ
FBA_D49	BT56	B	FBVDDQ
FBA_D5	BG58	B	FBVDDQ
FBA_D50	BU56	B	FBVDDQ
FBA_D51	BT57	B	FBVDDQ
FBA_D52	BW58	B	FBVDDQ
FBA_D53	BV57	B	FBVDDQ
FBA_D54	BW56	B	FBVDDQ
FBA_D55	BV55	B	FBVDDQ
FBA_D56	BU53	B	FBVDDQ
FBA_D57	BY52	B	FBVDDQ
FBA_D58	BN53	B	FBVDDQ
FBA_D59	BR53	B	FBVDDQ
FBA_D6	BG60	B	FBVDDQ
FBA_D60	BV52	B	FBVDDQ
FBA_D61	BY55	B	FBVDDQ
FBA_D62	BU52	B	FBVDDQ
FBA_D63	BM53	B	FBVDDQ
FBA_D7	BJ54	B	FBVDDQ
FBA_D8	BD57	B	FBVDDQ
FBA_D9	BD60	B	FBVDDQ
FBA_DQM0	BJ56	B	FBVDDQ
FBA_DQM1	BF56	B	FBVDDQ
FBA_DQM2	BR56	B	FBVDDQ
FBA_DQM3	BM56	B	FBVDDQ
FBA_DQM4	BT50	B	FBVDDQ
FBA_DQM5	BT47	B	FBVDDQ
FBA_DQM6	BY57	B	FBVDDQ
FBA_DQM7	BT53	B	FBVDDQ
FBA_DQS_WP0	BJ59	I	FBVDDQ
FBA_DQS_WP1	BF59	I	FBVDDQ
FBA_DQS_WP2	BR59	I	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBA_DQS_WP3	BM59	I	FBVDDQ
FBA_DQS_WP4	BW50	I	FBVDDQ
FBA_DQS_WP5	BW47	I	FBVDDQ
FBA_DQS_WP6	BY59	I	FBVDDQ
FBA_DQS_WP7	BW53	I	FBVDDQ
FBA_WCK01	BD50	O	FBVDDQ
FBA_WCK01_N	BD51	O	FBVDDQ
FBA_WCK23	BG50	O	FBVDDQ
FBA_WCK23_N	BG51	O	FBVDDQ
FBA_WCK45	BL49	O	FBVDDQ
FBA_WCK45_N	BM49	O	FBVDDQ
FBA_WCK67	BM50	O	FBVDDQ
FBA_WCK67_N	BL50	O	FBVDDQ
FBA_WCKB01	BC50	O	FBVDDQ
FBA_WCKB01_N	BC51	O	FBVDDQ
FBA_WCKB23	BF51	O	FBVDDQ
FBA_WCKB23_N	BF50	O	FBVDDQ
FBA_WCKB45	BM47	O	FBVDDQ
FBA_WCKB45_N	BN47	O	FBVDDQ
FBA_WCKB67	BN52	O	FBVDDQ
FBA_WCKB67_N	BM52	O	FBVDDQ
FBB_CLK0	AJ50	O	FBVDDQ
FBB_CLK0_N	AJ51	O	FBVDDQ
FBB_CLK1	AL51	O	FBVDDQ
FBB_CLK1_N	AL50	O	FBVDDQ
FBB_CMD0	W60	O	FBVDDQ
FBB_CMD1	W62	O	FBVDDQ
FBB_CMD10	AC61	O	FBVDDQ
FBB_CMD11	AD62	O	FBVDDQ
FBB_CMD12	AE60	O	FBVDDQ
FBB_CMD13	AE62	O	FBVDDQ
FBB_CMD14	AE61	O	FBVDDQ
FBB_CMD15	AF62	O	FBVDDQ
FBB_CMD16	AF61	O	FBVDDQ
FBB_CMD17	AG62	O	FBVDDQ
FBB_CMD18	AH60	O	FBVDDQ
FBB_CMD19	AH62	O	FBVDDQ
FBB_CMD2	W61	O	FBVDDQ
FBB_CMD20	AH61	O	FBVDDQ
FBB_CMD21	AJ62	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBB_CMD22	AJ61	O	FBVDDQ
FBB_CMD23	AK62	O	FBVDDQ
FBB_CMD24	AL60	O	FBVDDQ
FBB_CMD25_NC	AL62	NC	-
FBB_CMD26_NC	AL61	NC	-
FBB_CMD27	AE50	O	FBVDDQ
FBB_CMD28	BE62	O	FBVDDQ
FBB_CMD29	BD61	O	FBVDDQ
FBB_CMD3	Y62	O	FBVDDQ
FBB_CMD30	BD62	O	FBVDDQ
FBB_CMD31	BC61	O	FBVDDQ
FBB_CMD32	BC62	O	FBVDDQ
FBB_CMD33	BC60	O	FBVDDQ
FBB_CMD34	BB62	O	FBVDDQ
FBB_CMD35	BA61	O	FBVDDQ
FBB_CMD36	BA62	O	FBVDDQ
FBB_CMD37	AY61	O	FBVDDQ
FBB_CMD38	AY62	O	FBVDDQ
FBB_CMD39	AY60	O	FBVDDQ
FBB_CMD4	Y61	O	FBVDDQ
FBB_CMD40	AW62	O	FBVDDQ
FBB_CMD41	AV61	O	FBVDDQ
FBB_CMD42	AV62	O	FBVDDQ
FBB_CMD43	AU61	O	FBVDDQ
FBB_CMD44	AU62	O	FBVDDQ
FBB_CMD45	AU60	O	FBVDDQ
FBB_CMD46	AT62	O	FBVDDQ
FBB_CMD47	AR61	O	FBVDDQ
FBB_CMD48	AR62	O	FBVDDQ
FBB_CMD49	AP61	O	FBVDDQ
FBB_CMD5	AA62	O	FBVDDQ
FBB_CMD50	AP62	O	FBVDDQ
FBB_CMD51	AP60	O	FBVDDQ
FBB_CMD52	AN62	O	FBVDDQ
FBB_CMD53_NC	AM61	NC	-
FBB_CMD54_NC	AM62	NC	-
FBB_CMD55	AU50	O	FBVDDQ
FBB_CMD6	AB60	O	FBVDDQ
FBB_CMD7	AB62	O	FBVDDQ
FBB_CMD8	AB61	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBB_CMD9	AC62	O	FBVDDQ
FBB_D0	AE52	B	FBVDDQ
FBB_D1	AC55	B	FBVDDQ
FBB_D10	AB54	B	FBVDDQ
FBB_D11	Y55	B	FBVDDQ
FBB_D12	AB52	B	FBVDDQ
FBB_D13	Y57	B	FBVDDQ
FBB_D14	AB57	B	FBVDDQ
FBB_D15	Y60	B	FBVDDQ
FBB_D16	AJ60	B	FBVDDQ
FBB_D17	AM60	B	FBVDDQ
FBB_D18	AL57	B	FBVDDQ
FBB_D19	AL54	B	FBVDDQ
FBB_D2	AC57	B	FBVDDQ
FBB_D20	AJ58	B	FBVDDQ
FBB_D21	AJ57	B	FBVDDQ
FBB_D22	AJ55	B	FBVDDQ
FBB_D23	AL52	B	FBVDDQ
FBB_D24	AF57	B	FBVDDQ
FBB_D25	AF53	B	FBVDDQ
FBB_D26	AF58	B	FBVDDQ
FBB_D27	AF60	B	FBVDDQ
FBB_D28	AH54	B	FBVDDQ
FBB_D29	AH57	B	FBVDDQ
FBB_D3	AE54	B	FBVDDQ
FBB_D30	AH52	B	FBVDDQ
FBB_D31	AJ53	B	FBVDDQ
FBB_D32	AV58	B	FBVDDQ
FBB_D33	AV60	B	FBVDDQ
FBB_D34	AV55	B	FBVDDQ
FBB_D35	AV57	B	FBVDDQ
FBB_D36	AY57	B	FBVDDQ
FBB_D37	AY54	B	FBVDDQ
FBB_D38	AV53	B	FBVDDQ
FBB_D39	AY52	B	FBVDDQ
FBB_D4	AF55	B	FBVDDQ
FBB_D40	BA51	B	FBVDDQ
FBB_D41	BA55	B	FBVDDQ
FBB_D42	BA57	B	FBVDDQ
FBB_D43	BA58	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBB_D44	BA53	B	FBVDDQ
FBB_D45	BC54	B	FBVDDQ
FBB_D46	BA60	B	FBVDDQ
FBB_D47	BC57	B	FBVDDQ
FBB_D48	AR60	B	FBVDDQ
FBB_D49	AM53	B	FBVDDQ
FBB_D5	AC58	B	FBVDDQ
FBB_D50	AP57	B	FBVDDQ
FBB_D51	AP54	B	FBVDDQ
FBB_D52	AP52	B	FBVDDQ
FBB_D53	AM55	B	FBVDDQ
FBB_D54	AM58	B	FBVDDQ
FBB_D55	AM57	B	FBVDDQ
FBB_D56	AU57	B	FBVDDQ
FBB_D57	AU54	B	FBVDDQ
FBB_D58	AU52	B	FBVDDQ
FBB_D59	AR53	B	FBVDDQ
FBB_D6	AC60	B	FBVDDQ
FBB_D60	AR58	B	FBVDDQ
FBB_D61	AR57	B	FBVDDQ
FBB_D62	AR51	B	FBVDDQ
FBB_D63	AR55	B	FBVDDQ
FBB_D7	AE57	B	FBVDDQ
FBB_D8	AC53	B	FBVDDQ
FBB_D9	Y58	B	FBVDDQ
FBB_DQM0	AE56	B	FBVDDQ
FBB_DQM1	AB56	B	FBVDDQ
FBB_DQM2	AL56	B	FBVDDQ
FBB_DQM3	AH56	B	FBVDDQ
FBB_DQM4	AY56	B	FBVDDQ
FBB_DQM5	BC56	B	FBVDDQ
FBB_DQM6	AP56	B	FBVDDQ
FBB_DQM7	AU56	B	FBVDDQ
FBB_DQS_WP0	AE59	I	FBVDDQ
FBB_DQS_WP1	AB59	I	FBVDDQ
FBB_DQS_WP2	AL59	I	FBVDDQ
FBB_DQS_WP3	AH59	I	FBVDDQ
FBB_DQS_WP4	AY59	I	FBVDDQ
FBB_DQS_WP5	BC59	I	FBVDDQ
FBB_DQS_WP6	AP59	I	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBB_DQS_WP7	AU59	I	FBVDDQ
FBB_WCK01	AC50	O	FBVDDQ
FBB_WCK01_N	AC51	O	FBVDDQ
FBB_WCK23	AH51	O	FBVDDQ
FBB_WCK23_N	AH50	O	FBVDDQ
FBB_WCK45	AV50	O	FBVDDQ
FBB_WCK45_N	AV51	O	FBVDDQ
FBB_WCK67	AM51	O	FBVDDQ
FBB_WCK67_N	AM50	O	FBVDDQ
FBB_WCKB01	AB50	O	FBVDDQ
FBB_WCKB01_N	AB51	O	FBVDDQ
FBB_WCKB23	AF51	O	FBVDDQ
FBB_WCKB23_N	AF50	O	FBVDDQ
FBB_WCKB45	AY51	O	FBVDDQ
FBB_WCKB45_N	AY50	O	FBVDDQ
FBB_WCKB67	AP51	O	FBVDDQ
FBB_WCKB67_N	AP50	O	FBVDDQ
FBC_CLK0	K53	O	FBVDDQ
FBC_CLK0_N	K54	O	FBVDDQ
FBC_CLK1	L53	O	FBVDDQ
FBC_CLK1_N	L52	O	FBVDDQ
FBC_CMD0	A47	O	FBVDDQ
FBC_CMD1	B47	O	FBVDDQ
FBC_CMD10	A52	O	FBVDDQ
FBC_CMD11	B52	O	FBVDDQ
FBC_CMD12	A53	O	FBVDDQ
FBC_CMD13	B53	O	FBVDDQ
FBC_CMD14	A54	O	FBVDDQ
FBC_CMD15	C55	O	FBVDDQ
FBC_CMD16	A55	O	FBVDDQ
FBC_CMD17	B55	O	FBVDDQ
FBC_CMD18	A56	O	FBVDDQ
FBC_CMD19	B56	O	FBVDDQ
FBC_CMD2	A48	O	FBVDDQ
FBC_CMD20	A57	O	FBVDDQ
FBC_CMD21	B58	O	FBVDDQ
FBC_CMD22	A58	O	FBVDDQ
FBC_CMD23	B59	O	FBVDDQ
FBC_CMD24	C59	O	FBVDDQ
FBC_CMD25_NC	B60	NC	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBC_CMD26_NC	C60	NC	-
FBC_CMD27	M44	O	FBVDDQ
FBC_CMD28	V62	O	FBVDDQ
FBC_CMD29	U61	O	FBVDDQ
FBC_CMD3	C49	O	FBVDDQ
FBC_CMD30	U62	O	FBVDDQ
FBC_CMD31	T61	O	FBVDDQ
FBC_CMD32	T62	O	FBVDDQ
FBC_CMD33	T60	O	FBVDDQ
FBC_CMD34	R62	O	FBVDDQ
FBC_CMD35	P61	O	FBVDDQ
FBC_CMD36	P62	O	FBVDDQ
FBC_CMD37	N61	O	FBVDDQ
FBC_CMD38	N62	O	FBVDDQ
FBC_CMD39	N60	O	FBVDDQ
FBC_CMD4	A49	O	FBVDDQ
FBC_CMD40	M62	O	FBVDDQ
FBC_CMD41	L61	O	FBVDDQ
FBC_CMD42	L62	O	FBVDDQ
FBC_CMD43	K61	O	FBVDDQ
FBC_CMD44	K62	O	FBVDDQ
FBC_CMD45	K60	O	FBVDDQ
FBC_CMD46	J62	O	FBVDDQ
FBC_CMD47	H61	O	FBVDDQ
FBC_CMD48	H62	O	FBVDDQ
FBC_CMD49	G60	O	FBVDDQ
FBC_CMD5	B49	O	FBVDDQ
FBC_CMD50	G62	O	FBVDDQ
FBC_CMD51	F62	O	FBVDDQ
FBC_CMD52	E62	O	FBVDDQ
FBC_CMD53_NC	D61	NC	-
FBC_CMD54_NC	C61	NC	-
FBC_CMD55	Y50	O	FBVDDQ
FBC_CMD6	A50	O	FBVDDQ
FBC_CMD7	B50	O	FBVDDQ
FBC_CMD8	A51	O	FBVDDQ
FBC_CMD9	C52	O	FBVDDQ
FBC_D0	E47	B	FBVDDQ
FBC_D1	H47	B	FBVDDQ
FBC_D10	H44	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBC_D11	E44	B	FBVDDQ
FBC_D12	K47	B	FBVDDQ
FBC_D13	K44	B	FBVDDQ
FBC_D14	F46	B	FBVDDQ
FBC_D15	J46	B	FBVDDQ
FBC_D16	D55	B	FBVDDQ
FBC_D17	G55	B	FBVDDQ
FBC_D18	F55	B	FBVDDQ
FBC_D19	H53	B	FBVDDQ
FBC_D2	F47	B	FBVDDQ
FBC_D20	C56	B	FBVDDQ
FBC_D21	E56	B	FBVDDQ
FBC_D22	E57	B	FBVDDQ
FBC_D23	C58	B	FBVDDQ
FBC_D24	C50	B	FBVDDQ
FBC_D25	E50	B	FBVDDQ
FBC_D26	F52	B	FBVDDQ
FBC_D27	J50	B	FBVDDQ
FBC_D28	E53	B	FBVDDQ
FBC_D29	C53	B	FBVDDQ
FBC_D3	C47	B	FBVDDQ
FBC_D30	F53	B	FBVDDQ
FBC_D31	J52	B	FBVDDQ
FBC_D32	T54	B	FBVDDQ
FBC_D33	P60	B	FBVDDQ
FBC_D34	T51	B	FBVDDQ
FBC_D35	P58	B	FBVDDQ
FBC_D36	T57	B	FBVDDQ
FBC_D37	T53	B	FBVDDQ
FBC_D38	U55	B	FBVDDQ
FBC_D39	U53	B	FBVDDQ
FBC_D4	J49	B	FBVDDQ
FBC_D40	W52	B	FBVDDQ
FBC_D41	Y51	B	FBVDDQ
FBC_D42	U57	B	FBVDDQ
FBC_D43	U58	B	FBVDDQ
FBC_D44	W54	B	FBVDDQ
FBC_D45	W57	B	FBVDDQ
FBC_D46	Y53	B	FBVDDQ
FBC_D47	U60	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBC_D48	G56	B	FBVDDQ
FBC_D49	H55	B	FBVDDQ
FBC_D5	F49	B	FBVDDQ
FBC_D50	H57	B	FBVDDQ
FBC_D51	G59	B	FBVDDQ
FBC_D52	K57	B	FBVDDQ
FBC_D53	E61	B	FBVDDQ
FBC_D54	F60	B	FBVDDQ
FBC_D55	H59	B	FBVDDQ
FBC_D56	N54	B	FBVDDQ
FBC_D57	L55	B	FBVDDQ
FBC_D58	L58	B	FBVDDQ
FBC_D59	L57	B	FBVDDQ
FBC_D6	F50	B	FBVDDQ
FBC_D60	L60	B	FBVDDQ
FBC_D61	P55	B	FBVDDQ
FBC_D62	N57	B	FBVDDQ
FBC_D63	P57	B	FBVDDQ
FBC_D7	H50	B	FBVDDQ
FBC_D8	C44	B	FBVDDQ
FBC_D9	F44	B	FBVDDQ
FBC_DQM0	G49	B	FBVDDQ
FBC_DQM1	G46	B	FBVDDQ
FBC_DQM2	E58	B	FBVDDQ
FBC_DQM3	G52	B	FBVDDQ
FBC_DQM4	T56	B	FBVDDQ
FBC_DQM5	W56	B	FBVDDQ
FBC_DQM6	K56	B	FBVDDQ
FBC_DQM7	N56	B	FBVDDQ
FBC_DQS_WP0	D49	I	FBVDDQ
FBC_DQS_WP1	D46	I	FBVDDQ
FBC_DQS_WP2	E59	I	FBVDDQ
FBC_DQS_WP3	D52	I	FBVDDQ
FBC_DQS_WP4	T59	I	FBVDDQ
FBC_DQS_WP5	W59	I	FBVDDQ
FBC_DQS_WP6	K59	I	FBVDDQ
FBC_DQS_WP7	N59	I	FBVDDQ
FBC_WCK01	L47	O	FBVDDQ
FBC_WCK01_N	M47	O	FBVDDQ
FBC_WCK23	L50	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBC_WCK23_N	K50	O	FBVDDQ
FBC_WCK45	U50	O	FBVDDQ
FBC_WCK45_N	U51	O	FBVDDQ
FBC_WCK67	N53	O	FBVDDQ
FBC_WCK67_N	N52	O	FBVDDQ
FBC_WCKB01	L46	O	FBVDDQ
FBC_WCKB01_N	M46	O	FBVDDQ
FBC_WCKB23	K49	O	FBVDDQ
FBC_WCKB23_N	L49	O	FBVDDQ
FBC_WCKB45	W51	O	FBVDDQ
FBC_WCKB45_N	W50	O	FBVDDQ
FBC_WCKB67	P53	O	FBVDDQ
FBC_WCKB67_N	P52	O	FBVDDQ
FBD_CLK0	L31	O	FBVDDQ
FBD_CLK0_N	M31	O	FBVDDQ
FBD_CLK1	M32	O	FBVDDQ
FBD_CLK1_N	L32	O	FBVDDQ
FBD_CMD0	A20	O	FBVDDQ
FBD_CMD1	B20	O	FBVDDQ
FBD_CMD10	A25	O	FBVDDQ
FBD_CMD11	B25	O	FBVDDQ
FBD_CMD12	A26	O	FBVDDQ
FBD_CMD13	B26	O	FBVDDQ
FBD_CMD14	A27	O	FBVDDQ
FBD_CMD15	C28	O	FBVDDQ
FBD_CMD16	A28	O	FBVDDQ
FBD_CMD17	B28	O	FBVDDQ
FBD_CMD18	A29	O	FBVDDQ
FBD_CMD19	B29	O	FBVDDQ
FBD_CMD2	A21	O	FBVDDQ
FBD_CMD20	A30	O	FBVDDQ
FBD_CMD21	C31	O	FBVDDQ
FBD_CMD22	A31	O	FBVDDQ
FBD_CMD23	B31	O	FBVDDQ
FBD_CMD24	A32	O	FBVDDQ
FBD_CMD25_NC	B32	NC	-
FBD_CMD26_NC	A33	NC	-
FBD_CMD27	M28	O	FBVDDQ
FBD_CMD28	B46	O	FBVDDQ
FBD_CMD29	A46	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBD_CMD3	C22	O	FBVDDQ
FBD_CMD30	C46	O	FBVDDQ
FBD_CMD31	A45	O	FBVDDQ
FBD_CMD32	B44	O	FBVDDQ
FBD_CMD33	A44	O	FBVDDQ
FBD_CMD34	B43	O	FBVDDQ
FBD_CMD35	A43	O	FBVDDQ
FBD_CMD36	C43	O	FBVDDQ
FBD_CMD37	A42	O	FBVDDQ
FBD_CMD38	B41	O	FBVDDQ
FBD_CMD39	A41	O	FBVDDQ
FBD_CMD4	A22	O	FBVDDQ
FBD_CMD40	B40	O	FBVDDQ
FBD_CMD41	A40	O	FBVDDQ
FBD_CMD42	C40	O	FBVDDQ
FBD_CMD43	A39	O	FBVDDQ
FBD_CMD44	B38	O	FBVDDQ
FBD_CMD45	A38	O	FBVDDQ
FBD_CMD46	B37	O	FBVDDQ
FBD_CMD47	A37	O	FBVDDQ
FBD_CMD48	C37	O	FBVDDQ
FBD_CMD49	A36	O	FBVDDQ
FBD_CMD5	B22	O	FBVDDQ
FBD_CMD50	B35	O	FBVDDQ
FBD_CMD51	A35	O	FBVDDQ
FBD_CMD52	B34	O	FBVDDQ
FBD_CMD53_NC	A34	NC	-
FBD_CMD54_NC	C34	NC	-
FBD_CMD55	M37	O	FBVDDQ
FBD_CMD6	A23	O	FBVDDQ
FBD_CMD7	B23	O	FBVDDQ
FBD_CMD8	A24	O	FBVDDQ
FBD_CMD9	C25	O	FBVDDQ
FBD_D0	F23	B	FBVDDQ
FBD_D1	J22	B	FBVDDQ
FBD_D10	E20	B	FBVDDQ
FBD_D11	C20	B	FBVDDQ
FBD_D12	K22	B	FBVDDQ
FBD_D13	J19	B	FBVDDQ
FBD_D14	F20	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBD_D15	H20	B	FBVDDQ
FBD_D16	F29	B	FBVDDQ
FBD_D17	L28	B	FBVDDQ
FBD_D18	H29	B	FBVDDQ
FBD_D19	M29	B	FBVDDQ
FBD_D2	F22	B	FBVDDQ
FBD_D20	C29	B	FBVDDQ
FBD_D21	E29	B	FBVDDQ
FBD_D22	K29	B	FBVDDQ
FBD_D23	F31	B	FBVDDQ
FBD_D24	E26	B	FBVDDQ
FBD_D25	C26	B	FBVDDQ
FBD_D26	F26	B	FBVDDQ
FBD_D27	J25	B	FBVDDQ
FBD_D28	F28	B	FBVDDQ
FBD_D29	H26	B	FBVDDQ
FBD_D3	E23	B	FBVDDQ
FBD_D30	J28	B	FBVDDQ
FBD_D31	K26	B	FBVDDQ
FBD_D32	H38	B	FBVDDQ
FBD_D33	C38	B	FBVDDQ
FBD_D34	E38	B	FBVDDQ
FBD_D35	F38	B	FBVDDQ
FBD_D36	M38	B	FBVDDQ
FBD_D37	F40	B	FBVDDQ
FBD_D38	J40	B	FBVDDQ
FBD_D39	K38	B	FBVDDQ
FBD_D4	C23	B	FBVDDQ
FBD_D40	F41	B	FBVDDQ
FBD_D41	H41	B	FBVDDQ
FBD_D42	C41	B	FBVDDQ
FBD_D43	K41	B	FBVDDQ
FBD_D44	E41	B	FBVDDQ
FBD_D45	J43	B	FBVDDQ
FBD_D46	F43	B	FBVDDQ
FBD_D47	L43	B	FBVDDQ
FBD_D48	J34	B	FBVDDQ
FBD_D49	K32	B	FBVDDQ
FBD_D5	H23	B	FBVDDQ
FBD_D50	H32	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBD_D51	J31	B	FBVDDQ
FBD_D52	F34	B	FBVDDQ
FBD_D53	F32	B	FBVDDQ
FBD_D54	E32	B	FBVDDQ
FBD_D55	C32	B	FBVDDQ
FBD_D56	H35	B	FBVDDQ
FBD_D57	K35	B	FBVDDQ
FBD_D58	F35	B	FBVDDQ
FBD_D59	E35	B	FBVDDQ
FBD_D6	F25	B	FBVDDQ
FBD_D60	C35	B	FBVDDQ
FBD_D61	J37	B	FBVDDQ
FBD_D62	L37	B	FBVDDQ
FBD_D63	F37	B	FBVDDQ
FBD_D7	K23	B	FBVDDQ
FBD_D8	G19	B	FBVDDQ
FBD_D9	F19	B	FBVDDQ
FBD_DQM0	G25	B	FBVDDQ
FBD_DQM1	G22	B	FBVDDQ
FBD_DQM2	G31	B	FBVDDQ
FBD_DQM3	G28	B	FBVDDQ
FBD_DQM4	G40	B	FBVDDQ
FBD_DQM5	G43	B	FBVDDQ
FBD_DQM6	G34	B	FBVDDQ
FBD_DQM7	G37	B	FBVDDQ
FBD_DQS_WP0	D25	I	FBVDDQ
FBD_DQS_WP1	D22	I	FBVDDQ
FBD_DQS_WP2	D31	I	FBVDDQ
FBD_DQS_WP3	D28	I	FBVDDQ
FBD_DQS_WP4	D40	I	FBVDDQ
FBD_DQS_WP5	D43	I	FBVDDQ
FBD_DQS_WP6	D34	I	FBVDDQ
FBD_DQS_WP7	D37	I	FBVDDQ
FBD_WCK01	M23	O	FBVDDQ
FBD_WCK01_N	L23	O	FBVDDQ
FBD_WCK23	M26	O	FBVDDQ
FBD_WCK23_N	L26	O	FBVDDQ
FBD_WCK45	L40	O	FBVDDQ
FBD_WCK45_N	M40	O	FBVDDQ
FBD_WCK67	M34	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBD_WCK67_N	L34	O	FBVDDQ
FBD_WCKB01	M22	O	FBVDDQ
FBD_WCKB01_N	L22	O	FBVDDQ
FBD_WCKB23	L25	O	FBVDDQ
FBD_WCKB23_N	M25	O	FBVDDQ
FBD_WCKB45	M41	O	FBVDDQ
FBD_WCKB45_N	L41	O	FBVDDQ
FBD_WCKB67	L35	O	FBVDDQ
FBD_WCKB67_N	M35	O	FBVDDQ
FBE_CLK0	AB13	O	FBVDDQ
FBE_CLK0_N	AB12	O	FBVDDQ
FBE_CLK1	Y13	O	FBVDDQ
FBE_CLK1_N	Y12	O	FBVDDQ
FBE_CMD0	AR3	O	FBVDDQ
FBE_CMD1	AR1	O	FBVDDQ
FBE_CMD10	AL2	O	FBVDDQ
FBE_CMD11	AK1	O	FBVDDQ
FBE_CMD12	AJ3	O	FBVDDQ
FBE_CMD13	AJ1	O	FBVDDQ
FBE_CMD14	AJ2	O	FBVDDQ
FBE_CMD15	AH1	O	FBVDDQ
FBE_CMD16	AH2	O	FBVDDQ
FBE_CMD17	AG1	O	FBVDDQ
FBE_CMD18	AF3	O	FBVDDQ
FBE_CMD19	AF1	O	FBVDDQ
FBE_CMD2	AR2	O	FBVDDQ
FBE_CMD20	AF2	O	FBVDDQ
FBE_CMD21	AE1	O	FBVDDQ
FBE_CMD22	AE2	O	FBVDDQ
FBE_CMD23	AD1	O	FBVDDQ
FBE_CMD24	AC3	O	FBVDDQ
FBE_CMD25_NC	AC1	NC	-
FBE_CMD26_NC	AC2	NC	-
FBE_CMD27	AJ13	O	FBVDDQ
FBE_CMD28	J1	O	FBVDDQ
FBE_CMD29	K2	O	FBVDDQ
FBE_CMD3	AP1	O	FBVDDQ
FBE_CMD30	K1	O	FBVDDQ
FBE_CMD31	L2	O	FBVDDQ
FBE_CMD32	L1	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBE_CMD33	L3	O	FBVDDQ
FBE_CMD34	M1	O	FBVDDQ
FBE_CMD35	N2	O	FBVDDQ
FBE_CMD36	N1	O	FBVDDQ
FBE_CMD37	P2	O	FBVDDQ
FBE_CMD38	P1	O	FBVDDQ
FBE_CMD39	P3	O	FBVDDQ
FBE_CMD4	AP2	O	FBVDDQ
FBE_CMD40	R1	O	FBVDDQ
FBE_CMD41	T2	O	FBVDDQ
FBE_CMD42	T1	O	FBVDDQ
FBE_CMD43	U2	O	FBVDDQ
FBE_CMD44	U1	O	FBVDDQ
FBE_CMD45	U3	O	FBVDDQ
FBE_CMD46	V1	O	FBVDDQ
FBE_CMD47	W2	O	FBVDDQ
FBE_CMD48	W1	O	FBVDDQ
FBE_CMD49	Y2	O	FBVDDQ
FBE_CMD5	AN1	O	FBVDDQ
FBE_CMD50	Y1	O	FBVDDQ
FBE_CMD51	Y3	O	FBVDDQ
FBE_CMD52	AA1	O	FBVDDQ
FBE_CMD53_NC	AB2	NC	-
FBE_CMD54_NC	AB1	NC	-
FBE_CMD55	T13	O	FBVDDQ
FBE_CMD6	AM3	O	FBVDDQ
FBE_CMD7	AM1	O	FBVDDQ
FBE_CMD8	AM2	O	FBVDDQ
FBE_CMD9	AL1	O	FBVDDQ
FBE_D0	AF6	B	FBVDDQ
FBE_D1	AH3	B	FBVDDQ
FBE_D10	AJ9	B	FBVDDQ
FBE_D11	AL5	B	FBVDDQ
FBE_D12	AH11	B	FBVDDQ
FBE_D13	AJ11	B	FBVDDQ
FBE_D14	AH8	B	FBVDDQ
FBE_D15	AH13	B	FBVDDQ
FBE_D16	Y9	B	FBVDDQ
FBE_D17	AB6	B	FBVDDQ
FBE_D18	AB5	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBE_D19	AB8	B	FBVDDQ
FBE_D2	AE11	B	FBVDDQ
FBE_D20	AB3	B	FBVDDQ
FBE_D21	Y6	B	FBVDDQ
FBE_D22	Y11	B	FBVDDQ
FBE_D23	W10	B	FBVDDQ
FBE_D24	AC6	B	FBVDDQ
FBE_D25	AC10	B	FBVDDQ
FBE_D26	AC9	B	FBVDDQ
FBE_D27	AB10	B	FBVDDQ
FBE_D28	AE8	B	FBVDDQ
FBE_D29	AE3	B	FBVDDQ
FBE_D3	AH5	B	FBVDDQ
FBE_D30	AE5	B	FBVDDQ
FBE_D31	AE6	B	FBVDDQ
FBE_D32	N5	B	FBVDDQ
FBE_D33	P6	B	FBVDDQ
FBE_D34	N6	B	FBVDDQ
FBE_D35	N3	B	FBVDDQ
FBE_D36	N8	B	FBVDDQ
FBE_D37	N10	B	FBVDDQ
FBE_D38	L11	B	FBVDDQ
FBE_D39	L10	B	FBVDDQ
FBE_D4	AC12	B	FBVDDQ
FBE_D40	K5	B	FBVDDQ
FBE_D41	K3	B	FBVDDQ
FBE_D42	K8	B	FBVDDQ
FBE_D43	K6	B	FBVDDQ
FBE_D44	L9	B	FBVDDQ
FBE_D45	L6	B	FBVDDQ
FBE_D46	K10	B	FBVDDQ
FBE_D47	K11	B	FBVDDQ
FBE_D48	W5	B	FBVDDQ
FBE_D49	W8	B	FBVDDQ
FBE_D5	AH6	B	FBVDDQ
FBE_D50	W3	B	FBVDDQ
FBE_D51	W6	B	FBVDDQ
FBE_D52	U11	B	FBVDDQ
FBE_D53	U9	B	FBVDDQ
FBE_D54	U6	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBE_D55	U10	B	FBVDDQ
FBE_D56	T3	B	FBVDDQ
FBE_D57	P10	B	FBVDDQ
FBE_D58	P9	B	FBVDDQ
FBE_D59	T5	B	FBVDDQ
FBE_D6	AF9	B	FBVDDQ
FBE_D60	T6	B	FBVDDQ
FBE_D61	T10	B	FBVDDQ
FBE_D62	T8	B	FBVDDQ
FBE_D63	T12	B	FBVDDQ
FBE_D7	AF10	B	FBVDDQ
FBE_D8	AJ6	B	FBVDDQ
FBE_D9	AL3	B	FBVDDQ
FBE_DQM0	AJ7	B	FBVDDQ
FBE_DQM1	AM7	B	FBVDDQ
FBE_DQM2	AC7	B	FBVDDQ
FBE_DQM3	AF7	B	FBVDDQ
FBE_DQM4	P7	B	FBVDDQ
FBE_DQM5	L7	B	FBVDDQ
FBE_DQM6	Y7	B	FBVDDQ
FBE_DQM7	U7	B	FBVDDQ
FBE_DQS_WP0	AJ4	I	FBVDDQ
FBE_DQS_WP1	AM4	I	FBVDDQ
FBE_DQS_WP2	AC4	I	FBVDDQ
FBE_DQS_WP3	AF4	I	FBVDDQ
FBE_DQS_WP4	P4	I	FBVDDQ
FBE_DQS_WP5	L4	I	FBVDDQ
FBE_DQS_WP6	Y4	I	FBVDDQ
FBE_DQS_WP7	U4	I	FBVDDQ
FBE_WCK01	AL13	O	FBVDDQ
FBE_WCK01_N	AL12	O	FBVDDQ
FBE_WCK23	AE12	O	FBVDDQ
FBE_WCK23_N	AE13	O	FBVDDQ
FBE_WCK45	P11	O	FBVDDQ
FBE_WCK45_N	P12	O	FBVDDQ
FBE_WCK67	W13	O	FBVDDQ
FBE_WCK67_N	W12	O	FBVDDQ
FBE_WCKB01	AM12	O	FBVDDQ
FBE_WCKB01_N	AM13	O	FBVDDQ
FBE_WCKB23	AF13	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBE_WCKB23_N	AF12	O	FBVDDQ
FBE_WCKB45	N11	O	FBVDDQ
FBE_WCKB45_N	N12	O	FBVDDQ
FBE_WCKB67	U12	O	FBVDDQ
FBE_WCKB67_N	U13	O	FBVDDQ
FBF_CLK0	BD12	O	FBVDDQ
FBF_CLK0_N	BD13	O	FBVDDQ
FBF_CLK1	BC12	O	FBVDDQ
FBF_CLK1_N	BC13	O	FBVDDQ
FBF_CMD0	CB6	O	FBVDDQ
FBF_CMD1	CA5	O	FBVDDQ
FBF_CMD10	BV2	O	FBVDDQ
FBF_CMD11	BU1	O	FBVDDQ
FBF_CMD12	BT3	O	FBVDDQ
FBF_CMD13	BT1	O	FBVDDQ
FBF_CMD14	BT2	O	FBVDDQ
FBF_CMD15	BR1	O	FBVDDQ
FBF_CMD16	BR2	O	FBVDDQ
FBF_CMD17	BP1	O	FBVDDQ
FBF_CMD18	BN3	O	FBVDDQ
FBF_CMD19	BN1	O	FBVDDQ
FBF_CMD2	CB5	O	FBVDDQ
FBF_CMD20	BN2	O	FBVDDQ
FBF_CMD21	BM1	O	FBVDDQ
FBF_CMD22	BM2	O	FBVDDQ
FBF_CMD23	BL1	O	FBVDDQ
FBF_CMD24	BK3	O	FBVDDQ
FBF_CMD25_NC	BK1	NC	-
FBF_CMD26_NC	BK2	NC	-
FBF_CMD27	BJ12	O	FBVDDQ
FBF_CMD28	AT1	O	FBVDDQ
FBF_CMD29	AU2	O	FBVDDQ
FBF_CMD3	CA4	O	FBVDDQ
FBF_CMD30	AU1	O	FBVDDQ
FBF_CMD31	AV2	O	FBVDDQ
FBF_CMD32	AV1	O	FBVDDQ
FBF_CMD33	AV3	O	FBVDDQ
FBF_CMD34	AW1	O	FBVDDQ
FBF_CMD35	AY2	O	FBVDDQ
FBF_CMD36	AY1	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBF_CMD37	BA2	O	FBVDDQ
FBF_CMD38	BA1	O	FBVDDQ
FBF_CMD39	BA3	O	FBVDDQ
FBF_CMD4	CA3	O	FBVDDQ
FBF_CMD40	BB1	O	FBVDDQ
FBF_CMD41	BC2	O	FBVDDQ
FBF_CMD42	BC1	O	FBVDDQ
FBF_CMD43	BD2	O	FBVDDQ
FBF_CMD44	BD1	O	FBVDDQ
FBF_CMD45	BD3	O	FBVDDQ
FBF_CMD46	BE1	O	FBVDDQ
FBF_CMD47	BF2	O	FBVDDQ
FBF_CMD48	BF1	O	FBVDDQ
FBF_CMD49	BG2	O	FBVDDQ
FBF_CMD5	BY3	O	FBVDDQ
FBF_CMD50	BG1	O	FBVDDQ
FBF_CMD51	BG3	O	FBVDDQ
FBF_CMD52	BH1	O	FBVDDQ
FBF_CMD53_NC	BJ2	NC	-
FBF_CMD54_NC	BJ1	NC	-
FBF_CMD55	AR13	O	FBVDDQ
FBF_CMD6	BY2	O	FBVDDQ
FBF_CMD7	BW2	O	FBVDDQ
FBF_CMD8	BV3	O	FBVDDQ
FBF_CMD9	BV1	O	FBVDDQ
FBF_D0	BM3	B	FBVDDQ
FBF_D1	BK10	B	FBVDDQ
FBF_D10	BM8	B	FBVDDQ
FBF_D11	BM5	B	FBVDDQ
FBF_D12	BN6	B	FBVDDQ
FBF_D13	BR6	B	FBVDDQ
FBF_D14	BR3	B	FBVDDQ
FBF_D15	BT5	B	FBVDDQ
FBF_D16	BC5	B	FBVDDQ
FBF_D17	BC10	B	FBVDDQ
FBF_D18	BD11	B	FBVDDQ
FBF_D19	BC3	B	FBVDDQ
FBF_D2	BK6	B	FBVDDQ
FBF_D20	BC6	B	FBVDDQ
FBF_D21	BC8	B	FBVDDQ

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Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBF_D22	BD6	B	FBVDDQ
FBF_D23	BD9	B	FBVDDQ
FBF_D24	BG9	B	FBVDDQ
FBF_D25	BG6	B	FBVDDQ
FBF_D26	BF6	B	FBVDDQ
FBF_D27	BG10	B	FBVDDQ
FBF_D28	BF3	B	FBVDDQ
FBF_D29	BF5	B	FBVDDQ
FBF_D3	BK9	B	FBVDDQ
FBF_D30	BF8	B	FBVDDQ
FBF_D31	BF11	B	FBVDDQ
FBF_D32	AR6	B	FBVDDQ
FBF_D33	AR10	B	FBVDDQ
FBF_D34	AR12	B	FBVDDQ
FBF_D35	AR9	B	FBVDDQ
FBF_D36	AP6	B	FBVDDQ
FBF_D37	AP8	B	FBVDDQ
FBF_D38	AP12	B	FBVDDQ
FBF_D39	AP10	B	FBVDDQ
FBF_D4	BJ5	B	FBVDDQ
FBF_D40	AP5	B	FBVDDQ
FBF_D41	AL8	B	FBVDDQ
FBF_D42	AP3	B	FBVDDQ
FBF_D43	AM6	B	FBVDDQ
FBF_D44	AL10	B	FBVDDQ
FBF_D45	AL6	B	FBVDDQ
FBF_D46	AM9	B	FBVDDQ
FBF_D47	AM11	B	FBVDDQ
FBF_D48	BA6	B	FBVDDQ
FBF_D49	BA11	B	FBVDDQ
FBF_D5	BJ8	B	FBVDDQ
FBF_D50	AY11	B	FBVDDQ
FBF_D51	BA9	B	FBVDDQ
FBF_D52	AY5	B	FBVDDQ
FBF_D53	AY3	B	FBVDDQ
FBF_D54	AY6	B	FBVDDQ
FBF_D55	AY8	B	FBVDDQ
FBF_D56	AU3	B	FBVDDQ
FBF_D57	AU6	B	FBVDDQ
FBF_D58	AU5	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBF_D59	AU8	B	FBVDDQ
FBF_D6	BJ6	B	FBVDDQ
FBF_D60	AV6	B	FBVDDQ
FBF_D61	AU11	B	FBVDDQ
FBF_D62	AV10	B	FBVDDQ
FBF_D63	AV9	B	FBVDDQ
FBF_D7	BJ3	B	FBVDDQ
FBF_D8	BM10	B	FBVDDQ
FBF_D9	BM6	B	FBVDDQ
FBF_DQM0	BN7	B	FBVDDQ
FBF_DQM1	BU5	B	FBVDDQ
FBF_DQM2	BG7	B	FBVDDQ
FBF_DQM3	BK7	B	FBVDDQ
FBF_DQM4	AV7	B	FBVDDQ
FBF_DQM5	AR7	B	FBVDDQ
FBF_DQM6	BD7	B	FBVDDQ
FBF_DQM7	BA7	B	FBVDDQ
FBF_DQS_WP0	BN4	I	FBVDDQ
FBF_DQS_WP1	BT4	I	FBVDDQ
FBF_DQS_WP2	BG4	I	FBVDDQ
FBF_DQS_WP3	BK4	I	FBVDDQ
FBF_DQS_WP4	AV4	I	FBVDDQ
FBF_DQS_WP5	AR4	I	FBVDDQ
FBF_DQS_WP6	BD4	I	FBVDDQ
FBF_DQS_WP7	BA4	I	FBVDDQ
FBF_WCK01	BJ11	O	FBVDDQ
FBF_WCK01_N	BJ10	O	FBVDDQ
FBF_WCK23	BF12	O	FBVDDQ
FBF_WCK23_N	BF13	O	FBVDDQ
FBF_WCK45	AV13	O	FBVDDQ
FBF_WCK45_N	AV12	O	FBVDDQ
FBF_WCK67	BA13	O	FBVDDQ
FBF_WCK67_N	BA12	O	FBVDDQ
FBF_WCKB01	BK11	O	FBVDDQ
FBF_WCKB01_N	BK12	O	FBVDDQ
FBF_WCKB23	BG13	O	FBVDDQ
FBF_WCKB23_N	BG12	O	FBVDDQ
FBF_WCKB45	AU12	O	FBVDDQ
FBF_WCKB45_N	AU13	O	FBVDDQ
FBF_WCKB67	AY13	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBF_WCKB67_N	AY12	O	FBVDDQ
FBVDDQ	AB14	P	-
FBVDDQ	AB49	P	-
FBVDDQ	AC14	P	-
FBVDDQ	AC49	P	-
FBVDDQ	AE49	P	-
FBVDDQ	AF14	P	-
FBVDDQ	AH14	P	-
FBVDDQ	AH49	P	-
FBVDDQ	AJ14	P	-
FBVDDQ	AJ49	P	-
FBVDDQ	AL14	P	-
FBVDDQ	AL49	P	-
FBVDDQ	AM14	P	-
FBVDDQ	AM49	P	-
FBVDDQ	AP14	P	-
FBVDDQ	AP49	P	-
FBVDDQ	AR14	P	-
FBVDDQ	AR49	P	-
FBVDDQ	AU49	P	-
FBVDDQ	AV14	P	-
FBVDDQ	AV49	P	-
FBVDDQ	AY14	P	-
FBVDDQ	AY49	P	-
FBVDDQ	BA49	P	-
FBVDDQ	BC14	P	-
FBVDDQ	BC49	P	-
FBVDDQ	BD14	P	-
FBVDDQ	BD49	P	-
FBVDDQ	BF14	P	-
FBVDDQ	BG14	P	-
FBVDDQ	BG49	P	-
FBVDDQ	BJ13	P	-
FBVDDQ	BJ50	P	-
FBVDDQ	BJ51	P	-
FBVDDQ	BK46	P	-
FBVDDQ	BK47	P	-
FBVDDQ	BK49	P	-
FBVDDQ	BK51	P	-
FBVDDQ	N28	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBVDDQ	N29	P	-
FBVDDQ	N31	P	-
FBVDDQ	N32	P	-
FBVDDQ	N34	P	-
FBVDDQ	N35	P	-
FBVDDQ	N37	P	-
FBVDDQ	N40	P	-
FBVDDQ	N41	P	-
FBVDDQ	N43	P	-
FBVDDQ	N44	P	-
FBVDDQ	N46	P	-
FBVDDQ	N49	P	-
FBVDDQ	P50	P	-
FBVDDQ	P51	P	-
FBVDDQ	T49	P	-
FBVDDQ	W49	P	-
FBVDDQ	Y14	P	-
FBVDDQ	Y49	P	-
FBVDDQ_SENSE	H58	P	-
FUSE_SRC	BN31	P	-
GND	A11	P	-
GND	A13	P	-
GND	A15	P	-
GND	A17	P	-
GND	A2	P	-
GND	A3	P	-
GND	A4	P	-
GND	A5	P	-
GND	A59	P	-
GND	A60	P	-
GND	A61	P	-
GND	A7	P	-
GND	A9	P	-
GND	AA10	P	-
GND	AA12	P	-
GND	AA14	P	-
GND	AA2	P	-
GND	AA4	P	-
GND	AA49	P	-
GND	AA51	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AA53	P	-
GND	AA55	P	-
GND	AA57	P	-
GND	AA59	P	-
GND	AA6	P	-
GND	AA61	P	-
GND	AA8	P	-
GND	AB11	P	-
GND	AB17	P	-
GND	AB18	P	-
GND	AB19	P	-
GND	AB20	P	-
GND	AB21	P	-
GND	AB22	P	-
GND	AB23	P	-
GND	AB24	P	-
GND	AB25	P	-
GND	AB26	P	-
GND	AB27	P	-
GND	AB28	P	-
GND	AB29	P	-
GND	AB30	P	-
GND	AB31	P	-
GND	AB32	P	-
GND	AB33	P	-
GND	AB34	P	-
GND	AB35	P	-
GND	AB36	P	-
GND	AB37	P	-
GND	AB38	P	-
GND	AB39	P	-
GND	AB4	P	-
GND	AB40	P	-
GND	AB41	P	-
GND	AB42	P	-
GND	AB43	P	-
GND	AB44	P	-
GND	AB45	P	-
GND	AB46	P	-
GND	AB53	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AB55	P	-
GND	AB58	P	-
GND	AB7	P	-
GND	AB9	P	-
GND	AC11	P	-
GND	AC13	P	-
GND	AC5	P	-
GND	AC52	P	-
GND	AC54	P	-
GND	AC56	P	-
GND	AC59	P	-
GND	AC8	P	-
GND	AD10	P	-
GND	AD12	P	-
GND	AD14	P	-
GND	AD17	P	-
GND	AD18	P	-
GND	AD19	P	-
GND	AD2	P	-
GND	AD20	P	-
GND	AD21	P	-
GND	AD22	P	-
GND	AD23	P	-
GND	AD24	P	-
GND	AD25	P	-
GND	AD26	P	-
GND	AD27	P	-
GND	AD28	P	-
GND	AD29	P	-
GND	AD30	P	-
GND	AD31	P	-
GND	AD32	P	-
GND	AD33	P	-
GND	AD34	P	-
GND	AD35	P	-
GND	AD36	P	-
GND	AD37	P	-
GND	AD38	P	-
GND	AD39	P	-
GND	AD4	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AD40	P	-
GND	AD41	P	-
GND	AD42	P	-
GND	AD43	P	-
GND	AD44	P	-
GND	AD45	P	-
GND	AD46	P	-
GND	AD49	P	-
GND	AD51	P	-
GND	AD53	P	-
GND	AD55	P	-
GND	AD57	P	-
GND	AD59	P	-
GND	AD6	P	-
GND	AD61	P	-
GND	AD8	P	-
GND	AE10	P	-
GND	AE4	P	-
GND	AE51	P	-
GND	AE53	P	-
GND	AE55	P	-
GND	AE58	P	-
GND	AE7	P	-
GND	AE9	P	-
GND	AF11	P	-
GND	AF17	P	-
GND	AF18	P	-
GND	AF19	P	-
GND	AF20	P	-
GND	AF21	P	-
GND	AF22	P	-
GND	AF23	P	-
GND	AF24	P	-
GND	AF25	P	-
GND	AF26	P	-
GND	AF27	P	-
GND	AF28	P	-
GND	AF29	P	-
GND	AF30	P	-
GND	AF31	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AF32	P	-
GND	AF33	P	-
GND	AF34	P	-
GND	AF35	P	-
GND	AF36	P	-
GND	AF37	P	-
GND	AF38	P	-
GND	AF39	P	-
GND	AF40	P	-
GND	AF41	P	-
GND	AF42	P	-
GND	AF43	P	-
GND	AF44	P	-
GND	AF45	P	-
GND	AF46	P	-
GND	AF5	P	-
GND	AF52	P	-
GND	AF54	P	-
GND	AF56	P	-
GND	AF59	P	-
GND	AF8	P	-
GND	AG10	P	-
GND	AG12	P	-
GND	AG14	P	-
GND	AG2	P	-
GND	AG4	P	-
GND	AG49	P	-
GND	AG51	P	-
GND	AG53	P	-
GND	AG55	P	-
GND	AG57	P	-
GND	AG59	P	-
GND	AG6	P	-
GND	AG61	P	-
GND	AG8	P	-
GND	AH10	P	-
GND	AH12	P	-
GND	AH4	P	-
GND	AH53	P	-
GND	AH55	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AH58	P	-
GND	AH7	P	-
GND	AH9	P	-
GND	AJ10	P	-
GND	AJ12	P	-
GND	AJ17	P	-
GND	AJ18	P	-
GND	AJ19	P	-
GND	AJ20	P	-
GND	AJ21	P	-
GND	AJ22	P	-
GND	AJ23	P	-
GND	AJ24	P	-
GND	AJ25	P	-
GND	AJ26	P	-
GND	AJ27	P	-
GND	AJ28	P	-
GND	AJ29	P	-
GND	AJ30	P	-
GND	AJ31	P	-
GND	AJ32	P	-
GND	AJ33	P	-
GND	AJ34	P	-
GND	AJ35	P	-
GND	AJ36	P	-
GND	AJ37	P	-
GND	AJ38	P	-
GND	AJ39	P	-
GND	AJ40	P	-
GND	AJ41	P	-
GND	AJ42	P	-
GND	AJ43	P	-
GND	AJ44	P	-
GND	AJ45	P	-
GND	AJ46	P	-
GND	AJ5	P	-
GND	AJ52	P	-
GND	AJ54	P	-
GND	AJ56	P	-
GND	AJ59	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AJ8	P	-
GND	AK10	P	-
GND	AK12	P	-
GND	AK14	P	-
GND	AK2	P	-
GND	AK4	P	-
GND	AK49	P	-
GND	AK51	P	-
GND	AK53	P	-
GND	AK55	P	-
GND	AK57	P	-
GND	AK59	P	-
GND	AK6	P	-
GND	AK61	P	-
GND	AK8	P	-
GND	AL11	P	-
GND	AL17	P	-
GND	AL18	P	-
GND	AL19	P	-
GND	AL20	P	-
GND	AL21	P	-
GND	AL22	P	-
GND	AL23	P	-
GND	AL24	P	-
GND	AL25	P	-
GND	AL26	P	-
GND	AL27	P	-
GND	AL28	P	-
GND	AL29	P	-
GND	AL30	P	-
GND	AL31	P	-
GND	AL32	P	-
GND	AL33	P	-
GND	AL34	P	-
GND	AL35	P	-
GND	AL36	P	-
GND	AL37	P	-
GND	AL38	P	-
GND	AL39	P	-
GND	AL4	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AL40	P	-
GND	AL41	P	-
GND	AL42	P	-
GND	AL43	P	-
GND	AL44	P	-
GND	AL45	P	-
GND	AL46	P	-
GND	AL53	P	-
GND	AL55	P	-
GND	AL58	P	-
GND	AL7	P	-
GND	AL9	P	-
GND	AM10	P	-
GND	AM5	P	-
GND	AM52	P	-
GND	AM54	P	-
GND	AM56	P	-
GND	AM59	P	-
GND	AM8	P	-
GND	AN10	P	-
GND	AN12	P	-
GND	AN14	P	-
GND	AN17	P	-
GND	AN18	P	-
GND	AN19	P	-
GND	AN2	P	-
GND	AN20	P	-
GND	AN21	P	-
GND	AN22	P	-
GND	AN23	P	-
GND	AN24	P	-
GND	AN25	P	-
GND	AN26	P	-
GND	AN27	P	-
GND	AN28	P	-
GND	AN29	P	-
GND	AN30	P	-
GND	AN31	P	-
GND	AN32	P	-
GND	AN33	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AN34	P	-
GND	AN35	P	-
GND	AN36	P	-
GND	AN37	P	-
GND	AN38	P	-
GND	AN39	P	-
GND	AN4	P	-
GND	AN40	P	-
GND	AN41	P	-
GND	AN42	P	-
GND	AN43	P	-
GND	AN44	P	-
GND	AN45	P	-
GND	AN46	P	-
GND	AN49	P	-
GND	AN51	P	-
GND	AN53	P	-
GND	AN55	P	-
GND	AN57	P	-
GND	AN59	P	-
GND	AN6	P	-
GND	AN61	P	-
GND	AN8	P	-
GND	AP11	P	-
GND	AP13	P	-
GND	AP4	P	-
GND	AP53	P	-
GND	AP55	P	-
GND	AP58	P	-
GND	AP7	P	-
GND	AP9	P	-
GND	AR11	P	-
GND	AR17	P	-
GND	AR18	P	-
GND	AR19	P	-
GND	AR20	P	-
GND	AR21	P	-
GND	AR22	P	-
GND	AR23	P	-
GND	AR24	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AR25	P	-
GND	AR26	P	-
GND	AR27	P	-
GND	AR28	P	-
GND	AR29	P	-
GND	AR30	P	-
GND	AR31	P	-
GND	AR32	P	-
GND	AR33	P	-
GND	AR34	P	-
GND	AR35	P	-
GND	AR36	P	-
GND	AR37	P	-
GND	AR38	P	-
GND	AR39	P	-
GND	AR40	P	-
GND	AR41	P	-
GND	AR42	P	-
GND	AR43	P	-
GND	AR44	P	-
GND	AR45	P	-
GND	AR46	P	-
GND	AR5	P	-
GND	AR50	P	-
GND	AR52	P	-
GND	AR54	P	-
GND	AR56	P	-
GND	AR59	P	-
GND	AR8	P	-
GND	AT10	P	-
GND	AT12	P	-
GND	AT14	P	-
GND	AT2	P	-
GND	AT4	P	-
GND	AT49	P	-
GND	AT51	P	-
GND	AT53	P	-
GND	AT55	P	-
GND	AT57	P	-
GND	AT59	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AT6	P	-
GND	AT61	P	-
GND	AT8	P	-
GND	AU10	P	-
GND	AU17	P	-
GND	AU18	P	-
GND	AU19	P	-
GND	AU20	P	-
GND	AU21	P	-
GND	AU22	P	-
GND	AU23	P	-
GND	AU24	P	-
GND	AU25	P	-
GND	AU26	P	-
GND	AU27	P	-
GND	AU28	P	-
GND	AU29	P	-
GND	AU30	P	-
GND	AU31	P	-
GND	AU32	P	-
GND	AU33	P	-
GND	AU34	P	-
GND	AU35	P	-
GND	AU36	P	-
GND	AU37	P	-
GND	AU38	P	-
GND	AU39	P	-
GND	AU4	P	-
GND	AU40	P	-
GND	AU41	P	-
GND	AU42	P	-
GND	AU43	P	-
GND	AU44	P	-
GND	AU45	P	-
GND	AU46	P	-
GND	AU51	P	-
GND	AU53	P	-
GND	AU55	P	-
GND	AU58	P	-
GND	AU7	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AU9	P	-
GND	AV11	P	-
GND	AV5	P	-
GND	AV52	P	-
GND	AV54	P	-
GND	AV56	P	-
GND	AV59	P	-
GND	AV8	P	-
GND	AW10	P	-
GND	AW12	P	-
GND	AW14	P	-
GND	AW17	P	-
GND	AW18	P	-
GND	AW19	P	-
GND	AW2	P	-
GND	AW20	P	-
GND	AW21	P	-
GND	AW22	P	-
GND	AW23	P	-
GND	AW24	P	-
GND	AW25	P	-
GND	AW26	P	-
GND	AW27	P	-
GND	AW28	P	-
GND	AW29	P	-
GND	AW30	P	-
GND	AW31	P	-
GND	AW32	P	-
GND	AW33	P	-
GND	AW34	P	-
GND	AW35	P	-
GND	AW36	P	-
GND	AW37	P	-
GND	AW38	P	-
GND	AW39	P	-
GND	AW4	P	-
GND	AW40	P	-
GND	AW41	P	-
GND	AW42	P	-
GND	AW43	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AW44	P	-
GND	AW45	P	-
GND	AW46	P	-
GND	AW49	P	-
GND	AW51	P	-
GND	AW53	P	-
GND	AW55	P	-
GND	AW57	P	-
GND	AW59	P	-
GND	AW6	P	-
GND	AW61	P	-
GND	AW8	P	-
GND	AY10	P	-
GND	AY4	P	-
GND	AY53	P	-
GND	AY55	P	-
GND	AY58	P	-
GND	AY7	P	-
GND	AY9	P	-
GND	B1	P	-
GND	B2	P	-
GND	B21	P	-
GND	B24	P	-
GND	B27	P	-
GND	B30	P	-
GND	B33	P	-
GND	B36	P	-
GND	B39	P	-
GND	B42	P	-
GND	B45	P	-
GND	B48	P	-
GND	B51	P	-
GND	B54	P	-
GND	B57	P	-
GND	B61	P	-
GND	B62	P	-
GND	BA10	P	-
GND	BA17	P	-
GND	BA18	P	-
GND	BA19	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BA20	P	-
GND	BA21	P	-
GND	BA22	P	-
GND	BA23	P	-
GND	BA24	P	-
GND	BA25	P	-
GND	BA26	P	-
GND	BA27	P	-
GND	BA28	P	-
GND	BA29	P	-
GND	BA30	P	-
GND	BA31	P	-
GND	BA32	P	-
GND	BA33	P	-
GND	BA34	P	-
GND	BA35	P	-
GND	BA36	P	-
GND	BA37	P	-
GND	BA38	P	-
GND	BA39	P	-
GND	BA40	P	-
GND	BA41	P	-
GND	BA42	P	-
GND	BA43	P	-
GND	BA44	P	-
GND	BA45	P	-
GND	BA46	P	-
GND	BA5	P	-
GND	BA52	P	-
GND	BA54	P	-
GND	BA56	P	-
GND	BA59	P	-
GND	BA8	P	-
GND	BB10	P	-
GND	BB12	P	-
GND	BB14	P	-
GND	BB2	P	-
GND	BB4	P	-
GND	BB49	P	-
GND	BB51	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BB53	P	-
GND	BB55	P	-
GND	BB57	P	-
GND	BB59	P	-
GND	BB6	P	-
GND	BB61	P	-
GND	BB8	P	-
GND	BC11	P	-
GND	BC17	P	-
GND	BC18	P	-
GND	BC19	P	-
GND	BC20	P	-
GND	BC21	P	-
GND	BC22	P	-
GND	BC23	P	-
GND	BC24	P	-
GND	BC25	P	-
GND	BC26	P	-
GND	BC27	P	-
GND	BC28	P	-
GND	BC29	P	-
GND	BC30	P	-
GND	BC31	P	-
GND	BC32	P	-
GND	BC33	P	-
GND	BC34	P	-
GND	BC35	P	-
GND	BC36	P	-
GND	BC37	P	-
GND	BC38	P	-
GND	BC39	P	-
GND	BC4	P	-
GND	BC40	P	-
GND	BC41	P	-
GND	BC42	P	-
GND	BC43	P	-
GND	BC44	P	-
GND	BC45	P	-
GND	BC46	P	-
GND	BC53	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BC55	P	-
GND	BC58	P	-
GND	BC7	P	-
GND	BC9	P	-
GND	BD10	P	-
GND	BD5	P	-
GND	BD52	P	-
GND	BD54	P	-
GND	BD56	P	-
GND	BD59	P	-
GND	BD8	P	-
GND	BE10	P	-
GND	BE12	P	-
GND	BE14	P	-
GND	BE17	P	-
GND	BE18	P	-
GND	BE19	P	-
GND	BE2	P	-
GND	BE20	P	-
GND	BE21	P	-
GND	BE22	P	-
GND	BE23	P	-
GND	BE24	P	-
GND	BE25	P	-
GND	BE26	P	-
GND	BE27	P	-
GND	BE28	P	-
GND	BE29	P	-
GND	BE30	P	-
GND	BE31	P	-
GND	BE32	P	-
GND	BE33	P	-
GND	BE34	P	-
GND	BE35	P	-
GND	BE36	P	-
GND	BE37	P	-
GND	BE38	P	-
GND	BE39	P	-
GND	BE4	P	-
GND	BE40	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BE41	P	-
GND	BE42	P	-
GND	BE43	P	-
GND	BE44	P	-
GND	BE45	P	-
GND	BE46	P	-
GND	BE49	P	-
GND	BE51	P	-
GND	BE53	P	-
GND	BE55	P	-
GND	BE57	P	-
GND	BE59	P	-
GND	BE6	P	-
GND	BE61	P	-
GND	BE8	P	-
GND	BF10	P	-
GND	BF4	P	-
GND	BF53	P	-
GND	BF55	P	-
GND	BF58	P	-
GND	BF7	P	-
GND	BF9	P	-
GND	BG11	P	-
GND	BG17	P	-
GND	BG18	P	-
GND	BG19	P	-
GND	BG20	P	-
GND	BG21	P	-
GND	BG22	P	-
GND	BG23	P	-
GND	BG24	P	-
GND	BG25	P	-
GND	BG26	P	-
GND	BG27	P	-
GND	BG28	P	-
GND	BG29	P	-
GND	BG30	P	-
GND	BG31	P	-
GND	BG32	P	-
GND	BG33	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BG34	P	-
GND	BG35	P	-
GND	BG36	P	-
GND	BG37	P	-
GND	BG38	P	-
GND	BG39	P	-
GND	BG40	P	-
GND	BG41	P	-
GND	BG42	P	-
GND	BG43	P	-
GND	BG44	P	-
GND	BG45	P	-
GND	BG46	P	-
GND	BG5	P	-
GND	BG52	P	-
GND	BG54	P	-
GND	BG56	P	-
GND	BG59	P	-
GND	BG8	P	-
GND	BH10	P	-
GND	BH12	P	-
GND	BH2	P	-
GND	BH4	P	-
GND	BH51	P	-
GND	BH53	P	-
GND	BH55	P	-
GND	BH57	P	-
GND	BH59	P	-
GND	BH6	P	-
GND	BH61	P	-
GND	BH8	P	-
GND	BJ4	P	-
GND	BJ55	P	-
GND	BJ58	P	-
GND	BJ7	P	-
GND	BJ9	P	-
GND	BK5	P	-
GND	BK56	P	-
GND	BK59	P	-
GND	BK60	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BK8	P	-
GND	BL10	P	-
GND	BL12	P	-
GND	BL15	P	-
GND	BL18	P	-
GND	BL2	P	-
GND	BL21	P	-
GND	BL24	P	-
GND	BL27	P	-
GND	BL30	P	-
GND	BL33	P	-
GND	BL36	P	-
GND	BL39	P	-
GND	BL4	P	-
GND	BL42	P	-
GND	BL45	P	-
GND	BL48	P	-
GND	BL51	P	-
GND	BL53	P	-
GND	BL55	P	-
GND	BL57	P	-
GND	BL59	P	-
GND	BL6	P	-
GND	BL61	P	-
GND	BL8	P	-
GND	BM4	P	-
GND	BM54	P	-
GND	BM58	P	-
GND	BM7	P	-
GND	BN12	P	-
GND	BN15	P	-
GND	BN18	P	-
GND	BN21	P	-
GND	BN24	P	-
GND	BN27	P	-
GND	BN30	P	-
GND	BN33	P	-
GND	BN36	P	-
GND	BN39	P	-
GND	BN42	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BN45	P	-
GND	BN48	P	-
GND	BN5	P	-
GND	BN51	P	-
GND	BN54	P	-
GND	BN56	P	-
GND	BN59	P	-
GND	BP19	P	-
GND	BP2	P	-
GND	BP20	P	-
GND	BP22	P	-
GND	BP25	P	-
GND	BP28	P	-
GND	BP31	P	-
GND	BP34	P	-
GND	BP37	P	-
GND	BP4	P	-
GND	BP40	P	-
GND	BP43	P	-
GND	BP46	P	-
GND	BP49	P	-
GND	BP53	P	-
GND	BP55	P	-
GND	BP57	P	-
GND	BP59	P	-
GND	BP6	P	-
GND	BP61	P	-
GND	BP8	P	-
GND	BR12	P	-
GND	BR15	P	-
GND	BR17	P	-
GND	BR18	P	-
GND	BR20	P	-
GND	BR21	P	-
GND	BR23	P	-
GND	BR24	P	-
GND	BR26	P	-
GND	BR27	P	-
GND	BR4	P	-
GND	BR45	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BR47	P	-
GND	BR48	P	-
GND	BR5	P	-
GND	BR50	P	-
GND	BR51	P	-
GND	BR54	P	-
GND	BR55	P	-
GND	BR58	P	-
GND	BR9	P	-
GND	BT30	P	-
GND	BT32	P	-
GND	BT34	P	-
GND	BT36	P	-
GND	BT38	P	-
GND	BT40	P	-
GND	BT42	P	-
GND	BT44	P	-
GND	BT46	P	-
GND	BT49	P	-
GND	BT52	P	-
GND	BT60	P	-
GND	BU12	P	-
GND	BU15	P	-
GND	BU18	P	-
GND	BU2	P	-
GND	BU21	P	-
GND	BU24	P	-
GND	BU27	P	-
GND	BU29	P	-
GND	BU31	P	-
GND	BU33	P	-
GND	BU35	P	-
GND	BU37	P	-
GND	BU39	P	-
GND	BU4	P	-
GND	BU41	P	-
GND	BU43	P	-
GND	BU45	P	-
GND	BU48	P	-
GND	BU51	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BU54	P	-
GND	BU55	P	-
GND	BU57	P	-
GND	BU59	P	-
GND	BU6	P	-
GND	BU61	P	-
GND	BU9	P	-
GND	BV17	P	-
GND	BV20	P	-
GND	BV23	P	-
GND	BV26	P	-
GND	BV47	P	-
GND	BV50	P	-
GND	BV53	P	-
GND	BV56	P	-
GND	BV58	P	-
GND	BW1	P	-
GND	BW12	P	-
GND	BW15	P	-
GND	BW16	P	-
GND	BW17	P	-
GND	BW18	P	-
GND	BW19	P	-
GND	BW20	P	-
GND	BW21	P	-
GND	BW22	P	-
GND	BW23	P	-
GND	BW24	P	-
GND	BW25	P	-
GND	BW26	P	-
GND	BW27	P	-
GND	BW28	P	-
GND	BW29	P	-
GND	BW3	P	-
GND	BW30	P	-
GND	BW31	P	-
GND	BW32	P	-
GND	BW33	P	-
GND	BW34	P	-
GND	BW35	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BW36	P	-
GND	BW37	P	-
GND	BW38	P	-
GND	BW39	P	-
GND	BW40	P	-
GND	BW41	P	-
GND	BW42	P	-
GND	BW43	P	-
GND	BW44	P	-
GND	BW45	P	-
GND	BW48	P	-
GND	BW49	P	-
GND	BW51	P	-
GND	BW52	P	-
GND	BW54	P	-
GND	BW55	P	-
GND	BW57	P	-
GND	BW59	P	-
GND	BW6	P	-
GND	BW62	P	-
GND	BW9	P	-
GND	BY1	P	-
GND	BY30	P	-
GND	BY32	P	-
GND	BY34	P	-
GND	BY36	P	-
GND	BY38	P	-
GND	BY4	P	-
GND	BY40	P	-
GND	BY42	P	-
GND	BY44	P	-
GND	BY46	P	-
GND	BY47	P	-
GND	BY56	P	-
GND	BY58	P	-
GND	BY62	P	-
GND	C1	P	-
GND	C10	P	-
GND	C12	P	-
GND	C14	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	C16	P	-
GND	C18	P	-
GND	C4	P	-
GND	C6	P	-
GND	C62	P	-
GND	C8	P	-
GND	CA1	P	-
GND	CA12	P	-
GND	CA15	P	-
GND	CA18	P	-
GND	CA2	P	-
GND	CA21	P	-
GND	CA24	P	-
GND	CA27	P	-
GND	CA30	P	-
GND	CA48	P	-
GND	CA51	P	-
GND	CA54	P	-
GND	CA6	P	-
GND	CA61	P	-
GND	CA62	P	-
GND	CA9	P	-
GND	CB2	P	-
GND	CB3	P	-
GND	CB4	P	-
GND	CB59	P	-
GND	CB60	P	-
GND	CB61	P	-
GND	D1	P	-
GND	D10	P	-
GND	D11	P	-
GND	D12	P	-
GND	D13	P	-
GND	D14	P	-
GND	D15	P	-
GND	D16	P	-
GND	D17	P	-
GND	D18	P	-
GND	D19	P	-
GND	D2	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	D20	P	-
GND	D21	P	-
GND	D23	P	-
GND	D24	P	-
GND	D26	P	-
GND	D27	P	-
GND	D29	P	-
GND	D3	P	-
GND	D30	P	-
GND	D32	P	-
GND	D33	P	-
GND	D35	P	-
GND	D36	P	-
GND	D38	P	-
GND	D39	P	-
GND	D4	P	-
GND	D41	P	-
GND	D42	P	-
GND	D44	P	-
GND	D45	P	-
GND	D47	P	-
GND	D48	P	-
GND	D5	P	-
GND	D50	P	-
GND	D51	P	-
GND	D53	P	-
GND	D54	P	-
GND	D56	P	-
GND	D59	P	-
GND	D6	P	-
GND	D60	P	-
GND	D62	P	-
GND	D7	P	-
GND	D8	P	-
GND	D9	P	-
GND	E10	P	-
GND	E11	P	-
GND	E13	P	-
GND	E14	P	-
GND	E16	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	E17	P	-
GND	E19	P	-
GND	E2	P	-
GND	E22	P	-
GND	E25	P	-
GND	E28	P	-
GND	E3	P	-
GND	E31	P	-
GND	E34	P	-
GND	E37	P	-
GND	E4	P	-
GND	E40	P	-
GND	E43	P	-
GND	E46	P	-
GND	E49	P	-
GND	E5	P	-
GND	E52	P	-
GND	E55	P	-
GND	E6	P	-
GND	E60	P	-
GND	E7	P	-
GND	E8	P	-
GND	F11	P	-
GND	F13	P	-
GND	F15	P	-
GND	F17	P	-
GND	F18	P	-
GND	F21	P	-
GND	F24	P	-
GND	F27	P	-
GND	F3	P	-
GND	F30	P	-
GND	F33	P	-
GND	F36	P	-
GND	F39	P	-
GND	F42	P	-
GND	F45	P	-
GND	F48	P	-
GND	F5	P	-
GND	F51	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	F54	P	-
GND	F56	P	-
GND	F57	P	-
GND	F58	P	-
GND	F59	P	-
GND	F61	P	-
GND	F7	P	-
GND	F9	P	-
GND	G20	P	-
GND	G23	P	-
GND	G26	P	-
GND	G29	P	-
GND	G32	P	-
GND	G35	P	-
GND	G38	P	-
GND	G41	P	-
GND	G44	P	-
GND	G47	P	-
GND	G50	P	-
GND	G53	P	-
GND	G57	P	-
GND	G61	P	-
GND	H1	P	-
GND	H10	P	-
GND	H12	P	-
GND	H14	P	-
GND	H16	P	-
GND	H18	P	-
GND	H19	P	-
GND	H2	P	-
GND	H21	P	-
GND	H22	P	-
GND	H24	P	-
GND	H25	P	-
GND	H27	P	-
GND	H28	P	-
GND	H30	P	-
GND	H31	P	-
GND	H33	P	-
GND	H34	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	H36	P	-
GND	H37	P	-
GND	H39	P	-
GND	H4	P	-
GND	H40	P	-
GND	H42	P	-
GND	H43	P	-
GND	H45	P	-
GND	H46	P	-
GND	H48	P	-
GND	H49	P	-
GND	H51	P	-
GND	H52	P	-
GND	H54	P	-
GND	H56	P	-
GND	H6	P	-
GND	H60	P	-
GND	H8	P	-
GND	J10	P	-
GND	J11	P	-
GND	J13	P	-
GND	J14	P	-
GND	J16	P	-
GND	J17	P	-
GND	J2	P	-
GND	J20	P	-
GND	J23	P	-
GND	J26	P	-
GND	J29	P	-
GND	J32	P	-
GND	J35	P	-
GND	J38	P	-
GND	J4	P	-
GND	J41	P	-
GND	J44	P	-
GND	J47	P	-
GND	J53	P	-
GND	J55	P	-
GND	J57	P	-
GND	J59	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	J6	P	-
GND	J61	P	-
GND	J8	P	-
GND	K12	P	-
GND	K15	P	-
GND	K18	P	-
GND	K21	P	-
GND	K24	P	-
GND	K25	P	-
GND	K27	P	-
GND	K28	P	-
GND	K30	P	-
GND	K31	P	-
GND	K33	P	-
GND	K34	P	-
GND	K36	P	-
GND	K37	P	-
GND	K39	P	-
GND	K4	P	-
GND	K40	P	-
GND	K42	P	-
GND	K43	P	-
GND	K45	P	-
GND	K46	P	-
GND	K48	P	-
GND	K51	P	-
GND	K55	P	-
GND	K58	P	-
GND	K7	P	-
GND	K9	P	-
GND	L29	P	-
GND	L38	P	-
GND	L44	P	-
GND	L5	P	-
GND	L54	P	-
GND	L56	P	-
GND	L59	P	-
GND	L8	P	-
GND	M10	P	-
GND	M12	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	M15	P	-
GND	M18	P	-
GND	M2	P	-
GND	M21	P	-
GND	M24	P	-
GND	M27	P	-
GND	M30	P	-
GND	M33	P	-
GND	M36	P	-
GND	M39	P	-
GND	M4	P	-
GND	M42	P	-
GND	M43	P	-
GND	M45	P	-
GND	M48	P	-
GND	M51	P	-
GND	M53	P	-
GND	M55	P	-
GND	M57	P	-
GND	M59	P	-
GND	M6	P	-
GND	M61	P	-
GND	M8	P	-
GND	N4	P	-
GND	N55	P	-
GND	N58	P	-
GND	N7	P	-
GND	N9	P	-
GND	P5	P	-
GND	P54	P	-
GND	P56	P	-
GND	P59	P	-
GND	P8	P	-
GND	R10	P	-
GND	R12	P	-
GND	R2	P	-
GND	R4	P	-
GND	R51	P	-
GND	R53	P	-
GND	R55	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	R57	P	-
GND	R59	P	-
GND	R6	P	-
GND	R61	P	-
GND	R8	P	-
GND	T11	P	-
GND	T17	P	-
GND	T18	P	-
GND	T19	P	-
GND	T20	P	-
GND	T21	P	-
GND	T22	P	-
GND	T23	P	-
GND	T24	P	-
GND	T25	P	-
GND	T26	P	-
GND	T27	P	-
GND	T28	P	-
GND	T29	P	-
GND	T30	P	-
GND	T31	P	-
GND	T32	P	-
GND	T33	P	-
GND	T34	P	-
GND	T35	P	-
GND	T36	P	-
GND	T37	P	-
GND	T38	P	-
GND	T39	P	-
GND	T4	P	-
GND	T40	P	-
GND	T41	P	-
GND	T42	P	-
GND	T43	P	-
GND	T44	P	-
GND	T45	P	-
GND	T46	P	-
GND	T50	P	-
GND	T52	P	-
GND	T55	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	T58	P	-
GND	T7	P	-
GND	T9	P	-
GND	U5	P	-
GND	U52	P	-
GND	U54	P	-
GND	U56	P	-
GND	U59	P	-
GND	U8	P	-
GND	V10	P	-
GND	V12	P	-
GND	V14	P	-
GND	V17	P	-
GND	V18	P	-
GND	V19	P	-
GND	V2	P	-
GND	V20	P	-
GND	V21	P	-
GND	V22	P	-
GND	V23	P	-
GND	V24	P	-
GND	V25	P	-
GND	V26	P	-
GND	V27	P	-
GND	V28	P	-
GND	V29	P	-
GND	V30	P	-
GND	V31	P	-
GND	V32	P	-
GND	V33	P	-
GND	V34	P	-
GND	V35	P	-
GND	V36	P	-
GND	V37	P	-
GND	V38	P	-
GND	V39	P	-
GND	V4	P	-
GND	V40	P	-
GND	V41	P	-
GND	V42	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	V43	P	-
GND	V44	P	-
GND	V45	P	-
GND	V46	P	-
GND	V49	P	-
GND	V51	P	-
GND	V53	P	-
GND	V55	P	-
GND	V57	P	-
GND	V59	P	-
GND	V6	P	-
GND	V61	P	-
GND	V8	P	-
GND	W11	P	-
GND	W4	P	-
GND	W53	P	-
GND	W55	P	-
GND	W58	P	-
GND	W7	P	-
GND	W9	P	-
GND	Y10	P	-
GND	Y17	P	-
GND	Y18	P	-
GND	Y19	P	-
GND	Y20	P	-
GND	Y21	P	-
GND	Y22	P	-
GND	Y23	P	-
GND	Y24	P	-
GND	Y25	P	-
GND	Y26	P	-
GND	Y27	P	-
GND	Y28	P	-
GND	Y29	P	-
GND	Y30	P	-
GND	Y31	P	-
GND	Y32	P	-
GND	Y33	P	-
GND	Y34	P	-
GND	Y35	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	Y36	P	-
GND	Y37	P	-
GND	Y38	P	-
GND	Y39	P	-
GND	Y40	P	-
GND	Y41	P	-
GND	Y42	P	-
GND	Y43	P	-
GND	Y44	P	-
GND	Y45	P	-
GND	Y46	P	-
GND	Y5	P	-
GND	Y52	P	-
GND	Y54	P	-
GND	Y56	P	-
GND	Y59	P	-
GND	Y8	P	-
GND_SENSE	BM46	P	-
GNDMS_SENSE	CB47	P	-
GPCADC_AVDD	AU14	P	-
GPIO0	BU8	B	+1.8V
GPIO1	BN8	B	+1.8V
GPIO10	BT6	B	+1.8V
GPIO11	BU7	B	+1.8V
GPIO12	BN9	B	+1.8V
GPIO13	BW4	B	+1.8V
GPIO14	BV6	B	+1.8V
GPIO15	BT7	B	+1.8V
GPIO16	BP11	B	+1.8V
GPIO17	BU3	B	+1.8V
GPIO18	BV4	B	+1.8V
GPIO19	BV13	B	+1.8V
GPIO2	BW5	B	+1.8V
GPIO20	BU13	B	+1.8V
GPIO21	BU11	B	+1.8V
GPIO22	BY13	B	+1.8V
GPIO23	BW11	B	+1.8V
GPIO24	BM11	B	+1.8V
GPIO25	BT11	B	+1.8V
GPIO26	BW13	B	+1.8V

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GPIO27	BN10	B	+1.8V
GPIO28	BT13	B	+1.8V
GPIO29	BN11	B	+1.8V
GPIO3	BR11	B	+1.8V
GPIO30	BW10	B	+1.8V
GPIO31	BV10	B	+1.8V
GPIO32	BV11	B	+1.8V
GPIO33	BV7	B	+1.8V
GPIO34	BR10	B	+1.8V
GPIO35	BP10	B	+1.8V
GPIO4	BR7	B	+1.8V
GPIO5	BY6	B	+1.8V
GPIO6	BT10	B	+1.8V
GPIO7	BY5	B	+1.8V
GPIO8	BV5	B	+1.8V
GPIO9	BT8	B	+1.8V
I2CB_SCL	BY14	O	+1.8V
I2CB_SDA	BW14	B	+1.8V
I2CC_SCL	BR14	O	+1.8V
I2CC_SDA	BT14	B	+1.8V
I2CS_SCL	BV14	O	+1.8V
I2CS_SDA	BU14	B	+1.8V
IFP_IOVDD	BK20	P	-
IFP_IOVDD	BK22	P	-
IFP_IOVDD	BK23	P	-
IFP_IOVDD	BK25	P	-
IFP_IOVDD	BK26	P	-
IFP_IOVDD	BK28	P	-
IFP_IOVDD	BK29	P	-
IFP_IOVDD	BL20	P	-
IFP_IOVDD	BL23	P	-
IFP_IOVDD	BL26	P	-
IFP_IOVDD	BL29	P	-
IFP_IOVDD	BM20	P	-
IFPA_AUX_SCL	CB17	O	-
IFPA_AUX_SDA_N	CB16	B	-
IFPA_L0	BY26	O	-
IFPA_L0_N	CA26	O	-
IFPA_L1	CB25	O	-
IFPA_L1_N	CB26	O	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
IFPA_L2	BY25	O	-
IFPA_L2_N	CA25	O	-
IFPA_L3	BV25	O	-
IFPA_L3_N	BU25	O	-
IFPAB_PLLVDD	BL28	P	-
IFPAB_RSET	BP29	AI	-
IFPB_AUX_SCL	BU17	O	-
IFPB_AUX_SDA_N	BT17	B	-
IFPB_L0	BN29	O	-
IFPB_L0_N	BM29	O	-
IFPB_L1	BM28	O	-
IFPB_L1_N	BN28	O	-
IFPB_L2	BU26	O	-
IFPB_L2_N	BT26	O	-
IFPB_L3	BP26	O	-
IFPB_L3_N	BN26	O	-
IFPC_AUX_SCL	BU16	O	-
IFPC_AUX_SDA_N	BV16	B	-
IFPC_L0	BM25	O	-
IFPC_L0_N	BN25	O	-
IFPC_L1	BR25	O	-
IFPC_L1_N	BT25	O	-
IFPC_L2	BU23	O	-
IFPC_L2_N	BT23	O	-
IFPC_L3	BN23	O	-
IFPC_L3_N	BM23	O	-
IFPCD_PLLVDD	BL25	P	-
IFPCD_RSET	BM26	AI	-
IFPD_AUX_SCL	BT16	O	-
IFPD_AUX_SDA_N	BR16	B	-
IFPD_L0	BY23	O	-
IFPD_L0_N	CA23	O	-
IFPD_L1	CB22	O	-
IFPD_L1_N	CB23	O	-
IFPD_L2	CA22	O	-
IFPD_L2_N	BY22	O	-
IFPD_L3	BV22	O	-
IFPD_L3_N	BU22	O	-
IFPE_AUX_SCL	BY16	O	-
IFPE_AUX_SDA_N	CA16	B	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
IFPE_L0	BR22	O	-
IFPE_L0_N	BT22	O	-
IFPE_L1	BU20	O	-
IFPE_L1_N	BT20	O	-
IFPE_L2	BY20	O	-
IFPE_L2_N	CA20	O	-
IFPE_L3	CB19	O	-
IFPE_L3_N	CB20	O	-
IFPEF_PLLVDD	BL22	P	-
IFPEF_RSET	BP23	AI	-
IFPF_AUX_SCL	CB14	O	-
IFPF_AUX_SDA_N	CA14	B	-
IFPF_L0	BR19	O	-
IFPF_L0_N	BT19	O	-
IFPF_L1	BU19	O	-
IFPF_L1_N	BV19	O	-
IFPF_L2	CA19	O	-
IFPF_L2_N	BY19	O	-
IFPF_L3	BY17	O	-
IFPF_L3_N	CA17	O	-
JTAG_TCK	BY28	I	+1.8V
JTAG_TDI	CB29	I	+1.8V
JTAG_TDO	BY29	O	+1.8V
JTAG_TMS	CA28	I	+1.8V
JTAG_TRST_N	CB28	I	+1.8V
NC	A19	NC	-
NC	B19	NC	-
NC	BK16	NC	-
NC	BK17	NC	-
NC	BL16	NC	-
NC	BL17	NC	-
NC	BM13	NC	-
NC	BM16	NC	-
NC	BM17	NC	-
NC	BM19	NC	-
NC	BM31	NC	-
NC	BN14	NC	-
NC	BN16	NC	-
NC	BN17	NC	-
NC	BN19	NC	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
NC	BN20	NC	-
NC	BN22	NC	-
NC	BN32	NC	-
NC	BP32	NC	-
NC	BP35	NC	-
NC	BP38	NC	-
NC	BP41	NC	-
NC	C19	NC	-
NC	C57	NC	-
NC	D57	NC	-
NC	D58	NC	-
NVHS_CVDD	T14	P	-
NVHS_CVDD	U14	P	-
NVHS_DVDD	M13	P	-
NVHS_DVDD	M14	P	-
NVHS_DVDD	M16	P	-
NVHS_DVDD	M17	P	-
NVHS_DVDD	M19	P	-
NVHS_DVDD	M20	P	-
NVHS_DVDD	N14	P	-
NVHS_DVDD	N16	P	-
NVHS_DVDD	N17	P	-
NVHS_DVDD	N19	P	-
NVHS_DVDD	N20	P	-
NVHS_DVDD	N22	P	-
NVHS_DVDD	N23	P	-
NVHS_DVDD	N25	P	-
NVHS_DVDD	P13	P	-
NVHS_HVDD	K13	P	-
NVHS_HVDD	K14	P	-
NVHS_HVDD	K16	P	-
NVHS_HVDD	K17	P	-
NVHS_HVDD	K19	P	-
NVHS_HVDD	K20	P	-
NVHS_HVDD	L13	P	-
NVHS_HVDD	L14	P	-
NVHS_HVDD	L16	P	-
NVHS_HVDD	L17	P	-
NVHS_HVDD	L19	P	-
NVHS_REFCLK	H5	I	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
NVHS_REFCLK_N	G5	I	-
NVHS_TERMP	G1	AI	-
NVHS0_0_RX0	H17	I	-
NVHS0_0_RX0_N	G17	I	-
NVHS0_0_RX1	G16	I	-
NVHS0_0_RX1_N	F16	I	-
NVHS0_0_RX2	H15	I	-
NVHS0_0_RX2_N	G15	I	-
NVHS0_0_RX3	G14	I	-
NVHS0_0_RX3_N	F14	I	-
NVHS0_0_TX0	A18	O	-
NVHS0_0_TX0_N	B18	O	-
NVHS0_0_TX1	B17	O	-
NVHS0_0_TX1_N	C17	O	-
NVHS0_0_TX2	A16	O	-
NVHS0_0_TX2_N	B16	O	-
NVHS0_0_TX3	B15	O	-
NVHS0_0_TX3_N	C15	O	-
NVHS0_1_RX0	F12	I	-
NVHS0_1_RX0_N	G12	I	-
NVHS0_1_RX1	G13	I	-
NVHS0_1_RX1_N	H13	I	-
NVHS0_1_RX2	G11	I	-
NVHS0_1_RX2_N	H11	I	-
NVHS0_1_RX3	F10	I	-
NVHS0_1_RX3_N	G10	I	-
NVHS0_1_TX0	A14	O	-
NVHS0_1_TX0_N	B14	O	-
NVHS0_1_TX1	B13	O	-
NVHS0_1_TX1_N	C13	O	-
NVHS0_1_TX2	A12	O	-
NVHS0_1_TX2_N	B12	O	-
NVHS0_1_TX3	B11	O	-
NVHS0_1_TX3_N	C11	O	-
NVHS0_2_RX0	F8	I	-
NVHS0_2_RX0_N	G8	I	-
NVHS0_2_RX1	H9	I	-
NVHS0_2_RX1_N	G9	I	-
NVHS0_2_RX2	F6	I	-
NVHS0_2_RX2_N	G6	I	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
NVHS0_2_RX3	G7	I	-
NVHS0_2_RX3_N	H7	I	-
NVHS0_2_TX0	A10	O	-
NVHS0_2_TX0_N	B10	O	-
NVHS0_2_TX1	B9	O	-
NVHS0_2_TX1_N	C9	O	-
NVHS0_2_TX2	A8	O	-
NVHS0_2_TX2_N	B8	O	-
NVHS0_2_TX3	B7	O	-
NVHS0_2_TX3_N	C7	O	-
NVHS0_3_RX0	F2	I	-
NVHS0_3_RX0_N	G2	I	-
NVHS0_3_RX1	F1	I	-
NVHS0_3_RX1_N	E1	I	-
NVHS0_3_RX2	F4	I	-
NVHS0_3_RX2_N	G4	I	-
NVHS0_3_RX3	G3	I	-
NVHS0_3_RX3_N	H3	I	-
NVHS0_3_TX0	A6	O	-
NVHS0_3_TX0_N	B6	O	-
NVHS0_3_TX1	B5	O	-
NVHS0_3_TX1_N	C5	O	-
NVHS0_3_TX2	B4	O	-
NVHS0_3_TX2_N	B3	O	-
NVHS0_3_TX3	C3	O	-
NVHS0_3_TX3_N	C2	O	-
NVHS0_PLL_HVDD	L20	O	-
NVJTAG_SEL	CA29	I	+1.8V
OVERT	BN13	B	+1.8V
PEX_CLKREQ_N	BR28	O	+1.8V
PEX_CVDD	BK32	P	-
PEX_CVDD	BL32	P	-
PEX_CVDD	BM32	P	-
PEX_CVDD_SENSE	BP44	P	-
PEX_DVDD	BK34	P	-
PEX_DVDD	BK35	P	-
PEX_DVDD	BK37	P	-
PEX_DVDD	BK38	P	-
PEX_DVDD	BK40	P	-
PEX_DVDD	BK41	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
PEX_DVDD	BK43	P	-
PEX_DVDD	BK44	P	-
PEX_DVDD	BL34	P	-
PEX_DVDD	BL35	P	-
PEX_DVDD	BL37	P	-
PEX_DVDD	BL38	P	-
PEX_DVDD	BL40	P	-
PEX_DVDD	BL41	P	-
PEX_DVDD	BL43	P	-
PEX_DVDD	BL44	P	-
PEX_HVDD	BM34	P	-
PEX_HVDD	BM35	P	-
PEX_HVDD	BM37	P	-
PEX_HVDD	BM40	P	-
PEX_HVDD	BM41	P	-
PEX_HVDD	BM43	P	-
PEX_HVDD	BM44	P	-
PEX_HVDD	BN34	P	-
PEX_HVDD	BN35	P	-
PEX_HVDD	BN37	P	-
PEX_HVDD	BN38	P	-
PEX_HVDD	BN40	P	-
PEX_HVDD	BN41	P	-
PEX_HVDD	BN43	P	-
PEX_HVDD	BN44	P	-
PEX_PLL_HVDD	BM38	P	-
PEX_REFCLK	BU28	I	-
PEX_REFCLK_N	BV28	I	-
PEX_RST_N	BT28	I	+1.8V
PEX_RX0	BY31	I	-
PEX_RX0_N	CA31	I	-
PEX_RX1	CA32	I	-
PEX_RX1_N	CB32	I	-
PEX_RX10	BY41	I	-
PEX_RX10_N	CA41	I	-
PEX_RX11	CA42	I	-
PEX_RX11_N	CB42	I	-
PEX_RX12	BY43	I	-
PEX_RX12_N	CA43	I	-
PEX_RX13	CA44	I	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
PEX_RX13_N	CB44	I	-
PEX_RX14	BY45	I	-
PEX_RX14_N	CA45	I	-
PEX_RX15	CA46	I	-
PEX_RX15_N	CB46	I	-
PEX_RX2	BY33	I	-
PEX_RX2_N	CA33	I	-
PEX_RX3	CA34	I	-
PEX_RX3_N	CB34	I	-
PEX_RX4	BY35	I	-
PEX_RX4_N	CA35	I	-
PEX_RX5	CA36	I	-
PEX_RX5_N	CB36	I	-
PEX_RX6	BY37	I	-
PEX_RX6_N	CA37	I	-
PEX_RX7	CA38	I	-
PEX_RX7_N	CB38	I	-
PEX_RX8	BY39	I	-
PEX_RX8_N	CA39	I	-
PEX_RX9	CA40	I	-
PEX_RX9_N	CB40	I	-
PEX_TERMP	BW46	AI	-
PEX_TX0	BR29	O	-
PEX_TX0_N	BT29	O	-
PEX_TX1	BU30	O	-
PEX_TX1_N	BV30	O	-
PEX_TX10	BR39	O	-
PEX_TX10_N	BT39	O	-
PEX_TX11	BU40	O	-
PEX_TX11_N	BV40	O	-
PEX_TX12	BR41	O	-
PEX_TX12_N	BT41	O	-
PEX_TX13	BU42	O	-
PEX_TX13_N	BV42	O	-
PEX_TX14	BR43	O	-
PEX_TX14_N	BT43	O	-
PEX_TX15	BU44	O	-
PEX_TX15_N	BV44	O	-
PEX_TX2	BR31	O	-
PEX_TX2_N	BT31	O	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
PEX_TX3	BU32	O	-
PEX_TX3_N	BV32	O	-
PEX_TX4	BR33	O	-
PEX_TX4_N	BT33	O	-
PEX_TX5	BU34	O	-
PEX_TX5_N	BV34	O	-
PEX_TX6	BR35	O	-
PEX_TX6_N	BT35	O	-
PEX_TX7	BU36	O	-
PEX_TX7_N	BV36	O	-
PEX_TX8	BR37	O	-
PEX_TX8_N	BT37	O	-
PEX_TX9	BU38	O	-
PEX_TX9_N	BV38	O	-
PEX_WAKE_N	CB30	B	-
ROM_CS_N	BY11	O	+1.8V
ROM_SCLK	CA10	O	+1.8V
ROM_SI	BY10	B	+1.8V
ROM_SO	CB10	B	+1.8V
RSVD	BK19	RSVD	-
RSVD	BL19	RSVD	-
RSVD	BP13	RSVD	-
RSVD	BP14	RSVD	-
RSVD	BP16	RSVD	-
RSVD	BP17	RSVD	-
RSVD	BR13	RSVD	-
SP_PLLVDD	BM22	P	-
STRAP0	CA7	I	+1.8V
STRAP1	CB7	I	+1.8V
STRAP2	BW8	I	+1.8V
STRAP3	BW7	I	+1.8V
STRAP4	BY7	I	+1.8V
STRAP5	BV8	I	+1.8V
THERMDN	CB11	AO	-
THERMDP	CA11	AI	-
TS_VREF	BM9	AO	-
VDD	AA17	P	-
VDD	AA18	P	-
VDD	AA19	P	-
VDD	AA20	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AA21	P	-
VDD	AA22	P	-
VDD	AA23	P	-
VDD	AA24	P	-
VDD	AA25	P	-
VDD	AA26	P	-
VDD	AA27	P	-
VDD	AA28	P	-
VDD	AA29	P	-
VDD	AA30	P	-
VDD	AA31	P	-
VDD	AA32	P	-
VDD	AA33	P	-
VDD	AA34	P	-
VDD	AA35	P	-
VDD	AA36	P	-
VDD	AA37	P	-
VDD	AA38	P	-
VDD	AA39	P	-
VDD	AA40	P	-
VDD	AA41	P	-
VDD	AA42	P	-
VDD	AA43	P	-
VDD	AA44	P	-
VDD	AA45	P	-
VDD	AA46	P	-
VDD	AC17	P	-
VDD	AC18	P	-
VDD	AC19	P	-
VDD	AC20	P	-
VDD	AC21	P	-
VDD	AC22	P	-
VDD	AC23	P	-
VDD	AC24	P	-
VDD	AC25	P	-
VDD	AC26	P	-
VDD	AC27	P	-
VDD	AC28	P	-
VDD	AC29	P	-
VDD	AC30	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AC31	P	-
VDD	AC32	P	-
VDD	AC33	P	-
VDD	AC34	P	-
VDD	AC35	P	-
VDD	AC36	P	-
VDD	AC37	P	-
VDD	AC38	P	-
VDD	AC39	P	-
VDD	AC40	P	-
VDD	AC41	P	-
VDD	AC42	P	-
VDD	AC43	P	-
VDD	AC44	P	-
VDD	AC45	P	-
VDD	AC46	P	-
VDD	AE17	P	-
VDD	AE18	P	-
VDD	AE19	P	-
VDD	AE20	P	-
VDD	AE21	P	-
VDD	AE22	P	-
VDD	AE23	P	-
VDD	AE24	P	-
VDD	AE25	P	-
VDD	AE26	P	-
VDD	AE27	P	-
VDD	AE28	P	-
VDD	AE29	P	-
VDD	AE30	P	-
VDD	AE31	P	-
VDD	AE32	P	-
VDD	AE33	P	-
VDD	AE34	P	-
VDD	AE35	P	-
VDD	AE36	P	-
VDD	AE37	P	-
VDD	AE38	P	-
VDD	AE39	P	-
VDD	AE40	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AE41	P	-
VDD	AE42	P	-
VDD	AE43	P	-
VDD	AE44	P	-
VDD	AE45	P	-
VDD	AE46	P	-
VDD	AG17	P	-
VDD	AG18	P	-
VDD	AG19	P	-
VDD	AG20	P	-
VDD	AG21	P	-
VDD	AG22	P	-
VDD	AG23	P	-
VDD	AG24	P	-
VDD	AG25	P	-
VDD	AG26	P	-
VDD	AG27	P	-
VDD	AG28	P	-
VDD	AG29	P	-
VDD	AG30	P	-
VDD	AG31	P	-
VDD	AG32	P	-
VDD	AG33	P	-
VDD	AG34	P	-
VDD	AG35	P	-
VDD	AG36	P	-
VDD	AG37	P	-
VDD	AG38	P	-
VDD	AG39	P	-
VDD	AG40	P	-
VDD	AG41	P	-
VDD	AG42	P	-
VDD	AG43	P	-
VDD	AG44	P	-
VDD	AG45	P	-
VDD	AG46	P	-
VDD	AH17	P	-
VDD	AH18	P	-
VDD	AH19	P	-
VDD	AH20	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AH21	P	-
VDD	AH22	P	-
VDD	AH23	P	-
VDD	AH24	P	-
VDD	AH25	P	-
VDD	AH26	P	-
VDD	AH27	P	-
VDD	AH28	P	-
VDD	AH29	P	-
VDD	AH30	P	-
VDD	AH31	P	-
VDD	AH32	P	-
VDD	AH33	P	-
VDD	AH34	P	-
VDD	AH35	P	-
VDD	AH36	P	-
VDD	AH37	P	-
VDD	AH38	P	-
VDD	AH39	P	-
VDD	AH40	P	-
VDD	AH41	P	-
VDD	AH42	P	-
VDD	AH43	P	-
VDD	AH44	P	-
VDD	AH45	P	-
VDD	AH46	P	-
VDD	AK17	P	-
VDD	AK18	P	-
VDD	AK19	P	-
VDD	AK20	P	-
VDD	AK21	P	-
VDD	AK22	P	-
VDD	AK23	P	-
VDD	AK24	P	-
VDD	AK25	P	-
VDD	AK26	P	-
VDD	AK27	P	-
VDD	AK28	P	-
VDD	AK29	P	-
VDD	AK30	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AK31	P	-
VDD	AK32	P	-
VDD	AK33	P	-
VDD	AK34	P	-
VDD	AK35	P	-
VDD	AK36	P	-
VDD	AK37	P	-
VDD	AK38	P	-
VDD	AK39	P	-
VDD	AK40	P	-
VDD	AK41	P	-
VDD	AK42	P	-
VDD	AK43	P	-
VDD	AK44	P	-
VDD	AK45	P	-
VDD	AK46	P	-
VDD	AM17	P	-
VDD	AM18	P	-
VDD	AM19	P	-
VDD	AM20	P	-
VDD	AM21	P	-
VDD	AM22	P	-
VDD	AM23	P	-
VDD	AM24	P	-
VDD	AM25	P	-
VDD	AM26	P	-
VDD	AM27	P	-
VDD	AM28	P	-
VDD	AM29	P	-
VDD	AM30	P	-
VDD	AM31	P	-
VDD	AM32	P	-
VDD	AM33	P	-
VDD	AM34	P	-
VDD	AM35	P	-
VDD	AM36	P	-
VDD	AM37	P	-
VDD	AM38	P	-
VDD	AM39	P	-
VDD	AM40	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AM41	P	-
VDD	AM42	P	-
VDD	AM43	P	-
VDD	AM44	P	-
VDD	AM45	P	-
VDD	AM46	P	-
VDD	AP17	P	-
VDD	AP18	P	-
VDD	AP19	P	-
VDD	AP20	P	-
VDD	AP21	P	-
VDD	AP22	P	-
VDD	AP23	P	-
VDD	AP24	P	-
VDD	AP25	P	-
VDD	AP26	P	-
VDD	AP27	P	-
VDD	AP28	P	-
VDD	AP29	P	-
VDD	AP30	P	-
VDD	AP31	P	-
VDD	AP32	P	-
VDD	AP33	P	-
VDD	AP34	P	-
VDD	AP35	P	-
VDD	AP36	P	-
VDD	AP37	P	-
VDD	AP38	P	-
VDD	AP39	P	-
VDD	AP40	P	-
VDD	AP41	P	-
VDD	AP42	P	-
VDD	AP43	P	-
VDD	AP44	P	-
VDD	AP45	P	-
VDD	AP46	P	-
VDD	AT17	P	-
VDD	AT18	P	-
VDD	AT19	P	-
VDD	AT20	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AT21	P	-
VDD	AT22	P	-
VDD	AT23	P	-
VDD	AT24	P	-
VDD	AT25	P	-
VDD	AT26	P	-
VDD	AT27	P	-
VDD	AT28	P	-
VDD	AT29	P	-
VDD	AT30	P	-
VDD	AT31	P	-
VDD	AT32	P	-
VDD	AT33	P	-
VDD	AT34	P	-
VDD	AT35	P	-
VDD	AT36	P	-
VDD	AT37	P	-
VDD	AT38	P	-
VDD	AT39	P	-
VDD	AT40	P	-
VDD	AT41	P	-
VDD	AT42	P	-
VDD	AT43	P	-
VDD	AT44	P	-
VDD	AT45	P	-
VDD	AT46	P	-
VDD	AV17	P	-
VDD	AV18	P	-
VDD	AV19	P	-
VDD	AV20	P	-
VDD	AV21	P	-
VDD	AV22	P	-
VDD	AV23	P	-
VDD	AV24	P	-
VDD	AV25	P	-
VDD	AV26	P	-
VDD	AV27	P	-
VDD	AV28	P	-
VDD	AV29	P	-
VDD	AV30	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AV31	P	-
VDD	AV32	P	-
VDD	AV33	P	-
VDD	AV34	P	-
VDD	AV35	P	-
VDD	AV36	P	-
VDD	AV37	P	-
VDD	AV38	P	-
VDD	AV39	P	-
VDD	AV40	P	-
VDD	AV41	P	-
VDD	AV42	P	-
VDD	AV43	P	-
VDD	AV44	P	-
VDD	AV45	P	-
VDD	AV46	P	-
VDD	U17	P	-
VDD	U18	P	-
VDD	U19	P	-
VDD	U20	P	-
VDD	U21	P	-
VDD	U22	P	-
VDD	U23	P	-
VDD	U24	P	-
VDD	U25	P	-
VDD	U26	P	-
VDD	U27	P	-
VDD	U28	P	-
VDD	U29	P	-
VDD	U30	P	-
VDD	U31	P	-
VDD	U32	P	-
VDD	U33	P	-
VDD	U34	P	-
VDD	U35	P	-
VDD	U36	P	-
VDD	U37	P	-
VDD	U38	P	-
VDD	U39	P	-
VDD	U40	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	U41	P	-
VDD	U42	P	-
VDD	U43	P	-
VDD	U44	P	-
VDD	U45	P	-
VDD	U46	P	-
VDD	W17	P	-
VDD	W18	P	-
VDD	W19	P	-
VDD	W20	P	-
VDD	W21	P	-
VDD	W22	P	-
VDD	W23	P	-
VDD	W24	P	-
VDD	W25	P	-
VDD	W26	P	-
VDD	W27	P	-
VDD	W28	P	-
VDD	W29	P	-
VDD	W30	P	-
VDD	W31	P	-
VDD	W32	P	-
VDD	W33	P	-
VDD	W34	P	-
VDD	W35	P	-
VDD	W36	P	-
VDD	W37	P	-
VDD	W38	P	-
VDD	W39	P	-
VDD	W40	P	-
VDD	W41	P	-
VDD	W42	P	-
VDD	W43	P	-
VDD	W44	P	-
VDD	W45	P	-
VDD	W46	P	-
VDD_SENSE	BL46	P	-
VDDMS	AA16	P	-
VDDMS	AA47	P	-
VDDMS	AB16	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	AB47	P	-
VDDMS	AC16	P	-
VDDMS	AC47	P	-
VDDMS	AD16	P	-
VDDMS	AD47	P	-
VDDMS	AE16	P	-
VDDMS	AE47	P	-
VDDMS	AF16	P	-
VDDMS	AF47	P	-
VDDMS	AG16	P	-
VDDMS	AG47	P	-
VDDMS	AH16	P	-
VDDMS	AH47	P	-
VDDMS	AJ16	P	-
VDDMS	AJ47	P	-
VDDMS	AK16	P	-
VDDMS	AK47	P	-
VDDMS	AL16	P	-
VDDMS	AL47	P	-
VDDMS	AM16	P	-
VDDMS	AM47	P	-
VDDMS	AN16	P	-
VDDMS	AN47	P	-
VDDMS	AP16	P	-
VDDMS	AP47	P	-
VDDMS	AR16	P	-
VDDMS	AR47	P	-
VDDMS	AT16	P	-
VDDMS	AT47	P	-
VDDMS	AU16	P	-
VDDMS	AU47	P	-
VDDMS	AV16	P	-
VDDMS	AV47	P	-
VDDMS	AW16	P	-
VDDMS	AW47	P	-
VDDMS	AY16	P	-
VDDMS	AY17	P	-
VDDMS	AY18	P	-
VDDMS	AY19	P	-
VDDMS	AY20	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	AY21	P	-
VDDMS	AY22	P	-
VDDMS	AY23	P	-
VDDMS	AY24	P	-
VDDMS	AY25	P	-
VDDMS	AY26	P	-
VDDMS	AY27	P	-
VDDMS	AY28	P	-
VDDMS	AY29	P	-
VDDMS	AY30	P	-
VDDMS	AY31	P	-
VDDMS	AY32	P	-
VDDMS	AY33	P	-
VDDMS	AY34	P	-
VDDMS	AY35	P	-
VDDMS	AY36	P	-
VDDMS	AY37	P	-
VDDMS	AY38	P	-
VDDMS	AY39	P	-
VDDMS	AY40	P	-
VDDMS	AY41	P	-
VDDMS	AY42	P	-
VDDMS	AY43	P	-
VDDMS	AY44	P	-
VDDMS	AY45	P	-
VDDMS	AY46	P	-
VDDMS	AY47	P	-
VDDMS	BA16	P	-
VDDMS	BA47	P	-
VDDMS	BB16	P	-
VDDMS	BB17	P	-
VDDMS	BB18	P	-
VDDMS	BB19	P	-
VDDMS	BB20	P	-
VDDMS	BB21	P	-
VDDMS	BB22	P	-
VDDMS	BB23	P	-
VDDMS	BB24	P	-
VDDMS	BB25	P	-
VDDMS	BB26	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	BB27	P	-
VDDMS	BB28	P	-
VDDMS	BB29	P	-
VDDMS	BB30	P	-
VDDMS	BB31	P	-
VDDMS	BB32	P	-
VDDMS	BB33	P	-
VDDMS	BB34	P	-
VDDMS	BB35	P	-
VDDMS	BB36	P	-
VDDMS	BB37	P	-
VDDMS	BB38	P	-
VDDMS	BB39	P	-
VDDMS	BB40	P	-
VDDMS	BB41	P	-
VDDMS	BB42	P	-
VDDMS	BB43	P	-
VDDMS	BB44	P	-
VDDMS	BB45	P	-
VDDMS	BB46	P	-
VDDMS	BB47	P	-
VDDMS	BC16	P	-
VDDMS	BC47	P	-
VDDMS	BD16	P	-
VDDMS	BD17	P	-
VDDMS	BD18	P	-
VDDMS	BD19	P	-
VDDMS	BD20	P	-
VDDMS	BD21	P	-
VDDMS	BD22	P	-
VDDMS	BD23	P	-
VDDMS	BD24	P	-
VDDMS	BD25	P	-
VDDMS	BD26	P	-
VDDMS	BD27	P	-
VDDMS	BD28	P	-
VDDMS	BD29	P	-
VDDMS	BD30	P	-
VDDMS	BD31	P	-
VDDMS	BD32	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	BD33	P	-
VDDMS	BD34	P	-
VDDMS	BD35	P	-
VDDMS	BD36	P	-
VDDMS	BD37	P	-
VDDMS	BD38	P	-
VDDMS	BD39	P	-
VDDMS	BD40	P	-
VDDMS	BD41	P	-
VDDMS	BD42	P	-
VDDMS	BD43	P	-
VDDMS	BD44	P	-
VDDMS	BD45	P	-
VDDMS	BD46	P	-
VDDMS	BD47	P	-
VDDMS	BE16	P	-
VDDMS	BE47	P	-
VDDMS	BF16	P	-
VDDMS	BF17	P	-
VDDMS	BF18	P	-
VDDMS	BF19	P	-
VDDMS	BF20	P	-
VDDMS	BF21	P	-
VDDMS	BF22	P	-
VDDMS	BF23	P	-
VDDMS	BF24	P	-
VDDMS	BF25	P	-
VDDMS	BF26	P	-
VDDMS	BF27	P	-
VDDMS	BF28	P	-
VDDMS	BF29	P	-
VDDMS	BF30	P	-
VDDMS	BF31	P	-
VDDMS	BF32	P	-
VDDMS	BF33	P	-
VDDMS	BF34	P	-
VDDMS	BF35	P	-
VDDMS	BF36	P	-
VDDMS	BF37	P	-
VDDMS	BF38	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	BF39	P	-
VDDMS	BF40	P	-
VDDMS	BF41	P	-
VDDMS	BF42	P	-
VDDMS	BF43	P	-
VDDMS	BF44	P	-
VDDMS	BF45	P	-
VDDMS	BF46	P	-
VDDMS	BF47	P	-
VDDMS	BG16	P	-
VDDMS	BG47	P	-
VDDMS	BH16	P	-
VDDMS	BH17	P	-
VDDMS	BH18	P	-
VDDMS	BH19	P	-
VDDMS	BH20	P	-
VDDMS	BH21	P	-
VDDMS	BH22	P	-
VDDMS	BH23	P	-
VDDMS	BH24	P	-
VDDMS	BH25	P	-
VDDMS	BH26	P	-
VDDMS	BH27	P	-
VDDMS	BH28	P	-
VDDMS	BH29	P	-
VDDMS	BH30	P	-
VDDMS	BH31	P	-
VDDMS	BH32	P	-
VDDMS	BH33	P	-
VDDMS	BH34	P	-
VDDMS	BH35	P	-
VDDMS	BH36	P	-
VDDMS	BH37	P	-
VDDMS	BH38	P	-
VDDMS	BH39	P	-
VDDMS	BH40	P	-
VDDMS	BH41	P	-
VDDMS	BH42	P	-
VDDMS	BH43	P	-
VDDMS	BH44	P	-

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Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	BH45	P	-
VDDMS	BH46	P	-
VDDMS	BH47	P	-
VDDMS	R16	P	-
VDDMS	R17	P	-
VDDMS	R18	P	-
VDDMS	R19	P	-
VDDMS	R20	P	-
VDDMS	R21	P	-
VDDMS	R22	P	-
VDDMS	R23	P	-
VDDMS	R24	P	-
VDDMS	R25	P	-
VDDMS	R26	P	-
VDDMS	R27	P	-
VDDMS	R28	P	-
VDDMS	R29	P	-
VDDMS	R30	P	-
VDDMS	R31	P	-
VDDMS	R32	P	-
VDDMS	R33	P	-
VDDMS	R34	P	-
VDDMS	R35	P	-
VDDMS	R36	P	-
VDDMS	R37	P	-
VDDMS	R38	P	-
VDDMS	R39	P	-
VDDMS	R40	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	R41	P	-
VDDMS	R42	P	-
VDDMS	R43	P	-
VDDMS	R44	P	-
VDDMS	R45	P	-
VDDMS	R46	P	-
VDDMS	R47	P	-
VDDMS	T16	P	-
VDDMS	T47	P	-
VDDMS	U16	P	-
VDDMS	U47	P	-
VDDMS	V16	P	-
VDDMS	V47	P	-
VDDMS	W16	P	-
VDDMS	W47	P	-
VDDMS	Y16	P	-
VDDMS	Y47	P	-
VDDMS_SENSE	CA47	P	-
VID_PLLVDD	BL31	P	-
XTAL_IN	CB8	AI	+1.8V
XTAL_OUT	CA8	AO	+1.8V
XTAL_OUTBUFF	BY8	O	+1.8V

Packaging and Mechanical Specifications

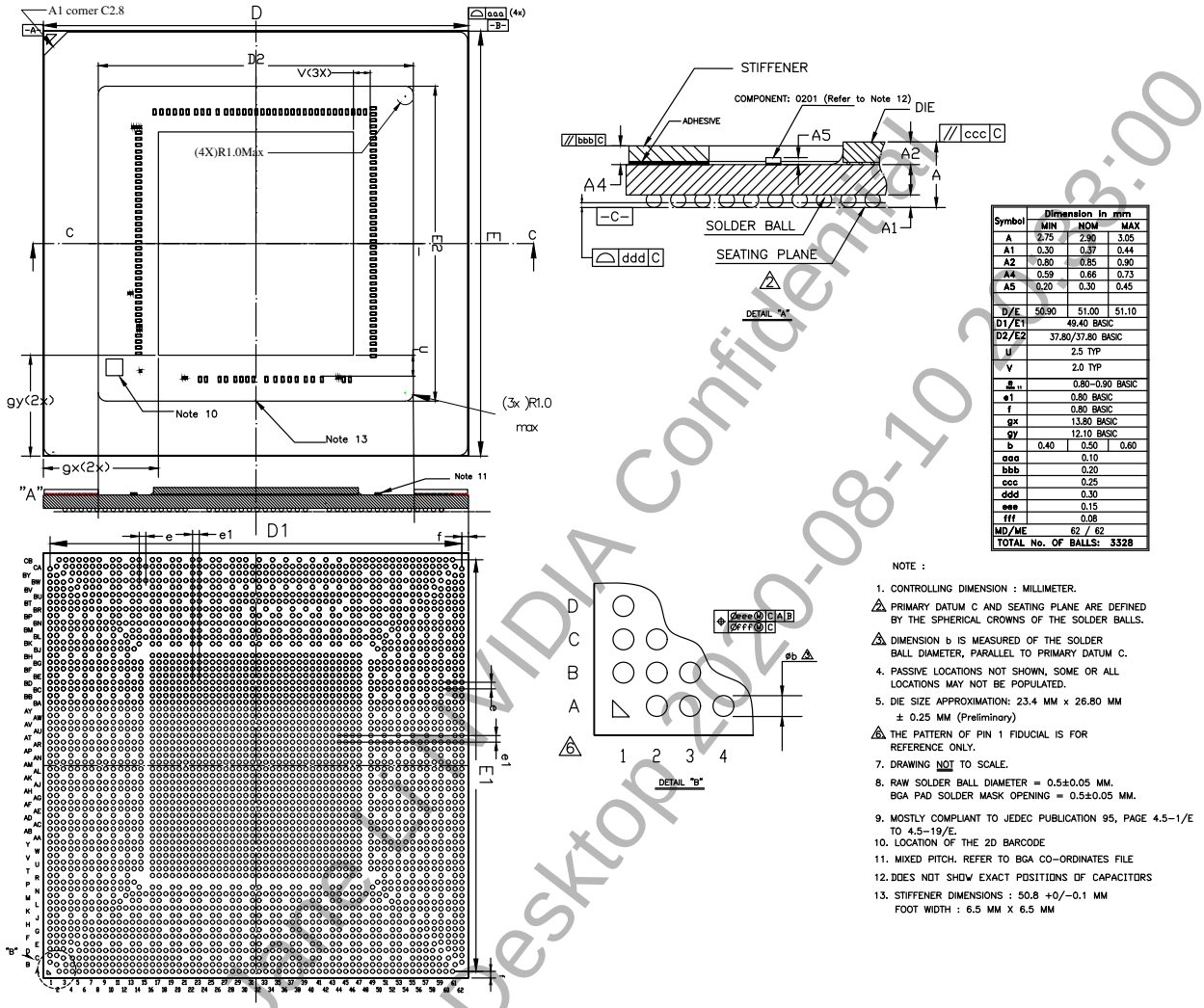
This section provides the following specifications and characteristics for this GPU.

- "Package Specifications"
- "Mechanical Specifications"
- "Environmental Conditions"

Package Specifications

Figure 5.1 shows this GPU in a 51 mm x 51 mm, 3328 ball S-FCBGA package.

Figure 5.1 Package Specification



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	2.75	2.90	3.05
A1	0.30	0.37	0.44
A2	0.80	0.85	0.90
A4	0.59	0.66	0.73
A5	0.20	0.30	0.45
D/E	50.90	51.00	51.10
D1/E1	49.40 BASIC		
D2/E2	37.80/37.80 BASIC		
u	2.5 TYP		
v	2.0 TYP		
e, e1	0.80-0.90 BASIC		
f	0.80 BASIC		
gx	13.80 BASIC		
gy	12.10 BASIC		
b	0.40	0.50	0.60
aaa	0.10		
bbb	0.20		
ccc	0.25		
ddd	0.30		
eee	0.15		
fff	0.08		
MD/ME	62 / 62		
TOTAL No. OF BALLS: 3328			

Mechanical Specifications

Table 5.1 Mechanical Specifications

Symbol	Parameter	Min	Nominal	Max	Units	Notes
P_{cont}	Maximum allowable pressure during PCA, system assembly and operation.	-	⩽60	⩽80	psi	1
T_{reflow}	Maximum package temperature during surface mount to printed circuit board	Refer to NVIDIA specifications 630-0011-001				
e_{max}	Maximum allowable strain during PCA, system assembly or operation			⩽500	µstrains	2

Notes:

1) This specification is based on the following conditions:

a. This specification is based on solder ball deformation and die chips and cracks. Additional requirements may be needed to meet the thermal performance and/or long term reliability as to specific application,
b. When a compliant thermal interface is used between die and heat sink, the bond line thickness must have less than 20% in variation.
he pressure should be measured on the top of the die surface by an instrument equipped pressure sensors. See details in "GPU Load Distribution Measurement Application Note".
d. Nominal pressure is the total force divided by the die surface area. Since the pressure may have variations across the whole surfaces. The following additional requirement is applied:

i. The pressure has to be measured from the top of the die surface with a grid resolution of 1x1mm2 for the pressure sensor.

e. Both nominal and maximum pressure requirement must be met.

2) Strain measurement shall follow IPC-9704, particularly on following items:

a. The strain shall be measured on the top side of PCB close to the four corners of the package. A rigid PCB is assumed.

b. For generic application, the max. allowable strain must be no more than 500 µstrains for a board thickness from 1.0 to 3.2mm. A separate requirement may be specified and the qualification test should be performed if

i. A sensitive PCB laminate and build up structure is used where the pad cratering occurs at a PCB strain of 500 µstrains or below.

ii. A weak surface finish of PCB is used where cracked solder joint has been observed at a PCB strain of 500 µstrains or below.

iii. The strain rate is too high (.5000 µstrains/second) during the PCA operations.

c. For PCB thickness less than 1,0mm, the max. allowable strain shall follow IPC 9704.

Environmental Conditions

Table 5.2 Environmental Conditions

Environment	Condition
Storage temperature	-40 °C to 125 °C
Operating humidity	5% to 90% RH
Storage humidity	5% to 95% RH

Ball Map

The GPU ball map is shown below.

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62		
1	A	~x	GND	GND	GND	GND	NVHS0_3_TX	GND	NVHS0_2_TX	GND	NVHS0_2_TX	GND	NVHS0_1_TX	GND	NVHS0_1_TX	GND	NVHS0_0_TX	GND	NVHS0_0_TX	NC	FBD_CMD0	FBD_CMD2	FBD_CMD4	FBD_CMD6	FBD_CMD8	FBD_CMD10	FBD_CMD12	FBD_CMD14	FBD_CMD16	FBD_CMD18	FBD_CMD20	FBD_CMD22	FBD_CMD24	FBD_CMD26_NC	FBD_CMD53_NC	FBD_CMD51	FBD_CMD49	FBD_CMD47	FBD_CMD45	FBD_CMD43	FBD_CMD41	FBD_CMD39	FBD_CMD37	FBD_CMD35	FBD_CMD33	FBD_CMD31	FBD_CMD29	FBC_CMD0	FBC_CMD2	FBC_CMD4	FBC_CMD6	FBC_CMD8	FBC_CMD10	FBC_CMD12	FBC_CMD14	FBC_CMD16	FBC_CMD18	FBC_CMD20	FBC_CMD22	GND	GND	GND	~x	A	1
2	B	GND	GND	VHS0_3_TX2	NVHS0_3_TX	NVHS0_3_TX	VHS0_3_TX0	NVHS0_2_TX	VHS0_2_TX2	NVHS0_2_TX	VHS0_2_TX0	NVHS0_1_TX	VHS0_1_TX2	NVHS0_1_TX	VHS0_1_TX0	NVHS0_0_TX	VHS0_0_TX2	NVHS0_0_TX	VHS0_0_TX0	NC	FBD_CMD1	GND	FBD_CMD5	FBD_CMD7	GND	FBD_CMD11	FBD_CMD13	GND	FBD_CMD17	FBD_CMD19	GND	FBD_CMD23	FBD_CMD25_NC	GND	FBD_CMD52	FBD_CMD50	GND	FBD_CMD46	FBD_CMD44	GND	FBD_CMD40	FBD_CMD38	GND	FBD_CMD34	FBD_CMD32	GND	FBD_CMD28	FBC_CMD1	GND	FBC_CMD5	FBC_CMD7	GND	FBC_CMD11	FBC_CMD13	GND	FBC_CMD17	FBC_CMD19	GND	FBC_CMD21	FBC_CMD23	FBC_CMD25_NC	GND	GND	B	2
3	C	GND	VHS0_3_TX3	NVHS0_3_TX	GND	VHS0_3_TX1	GND	VHS0_2_TX3	GND	VHS0_2_TX1	GND	VHS0_1_TX3	GND	VHS0_1_TX1	GND	VHS0_0_TX3	GND	VHS0_0_TX1	GND	NC	FBD_D11	~x	FBD_CMD3	FBD_D4	~x	FBD_CMD9	FBD_D25	~x	FBD_CMD15	FBD_D20	~x	FBD_CMD21	FBD_D55	~x	FBD_CMD54_NC	FBD_D60	~x	FBD_CMD48	FBD_D33	~x	FBD_CMD42	FBD_D42	~x	FBD_CMD36	FBC_D8	~x	FBD_CMD30	FBC_D3	~x	FBC_CMD3	FBC_D24	~x	FBC_CMD9	FBC_D29	~x	FBC_CMD15	FBC_D20	NC	FBC_D23	FBC_CMD24	FBC_CMD26_NC	FBC_CMD54_NC	GND	C	3
4	D	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	FBD_DQS_WP1	GND	GND	FBD_DQS_WP0	GND	GND	FBD_DQS_WP3	GND	GND	FBD_DQS_WP2	GND	GND	FBD_DQS_WP6	GND	GND	FBD_DQS_WP7	GND	GND	FBD_DQS_WP4	GND	GND	FBD_DQS_WP5	GND	GND	FBC_DQS_WP1	GND	GND	FBC_DQS_WP0	GND	GND	FBC_DQS_WP3	GND	GND	FBC_D16	GND	NC	NC	GND	GND	FBC_CMD53_NC	GND	D	4
5	E	VHS0_3_RX1	GND	GND	GND	GND	GND	GND	GND	~x	GND	GND	~x	GND	GND	~x	GND	GND	~x	GND	FBD_D10	~x	GND	FBD_D3	~x	GND	FBD_D24	~x	GND	FBD_D21	~x	GND	FBD_D54	~x	GND	FBD_D59	~x	GND	FBD_D34	~x	GND	FBD_D44	~x	GND	FBC_D11	~x	GND	FBC_D0	~x	GND	FBC_D25	~x	GND	FBC_D28	~x	GND	FBC_D21	FBC_D22	FBC_DQM2	FBC_DQS_WP2	GND	FBC_D53	FBC_CMD52	E	5
6	F	NVHS0_3_RX	NVHS0_3_RX	GND	NVHS0_3_RX	GND	NVHS0_2_RX	GND	NVHS0_2_RX	GND	NVHS0_1_RX	GND	NVHS0_1_RX	GND	VHS0_0_RX3	GND	VHS0_0_RX1	GND	GND	FBD_D9	FBD_D14	GND	FBD_D2	FBD_D0	GND	FBD_D6	FBD_D26	GND	FBD_D28	FBD_D16	GND	FBD_D23	FBD_D53	GND	FBD_D52	FBD_D58	GND	FBD_D63	FBD_D35	GND	FBD_D37	FBD_D40	GND	FBD_D46	FBC_D9	GND	FBC_D14	FBC_D2	GND	FBC_D5	FBC_D6	GND	FBC_D26	FBC_D30	GND	FBC_D18	GND	GND	GND	GND	FBC_D54	GND	FBC_CMD51	F	6
7	G	NVHS_TERM	VHS0_3_RX0	NVHS0_3_RX	VHS0_3_RX2	HS_REFCLK	VHS0_2_RX2	NVHS0_2_RX	VHS0_2_RX0	VHS0_2_RX1	VHS0_1_RX3	NVHS0_1_RX	VHS0_1_RX0	NVHS0_1_RX	NVHS0_0_RX	VHS0_0_RX2	NVHS0_0_RX	VHS0_0_RX0	~x	FBD_D8	GND	~x	FBD_DQM1	GND	~x	FBD_DQM0	GND	~x	FBD_DQM3	GND	~x	FBD_DQM2	GND	~x	FBD_DQM6	GND	~x	FBD_DQM7	GND	~x	FBD_DQM4	GND	~x	FBD_DQM5	GND	~x	FBC_DQM1	GND	~x	FBC_DQM0	GND	~x	FBC_DQM3	GND	~x	FBC_D17	FBC_D48	GND	B_GND_SENS	FBC_D51	FBC_CMD49	GND	FBC_CMD50	G	7
8	H	GND	GND	VHS0_3_RX3	GND	NVHS_REFCL	GND	VHS0_2_RX3	GND	NVHS0_2_RX	GND	VHS0_1_RX2	GND	VHS0_1_RX1	GND	NVHS0_0_RX	GND	NVHS0_0_RX	GND	GND	FBD_D15	GND	GND	FBD_D5	GND	GND	FBD_D29	GND	GND	FBD_D18	GND	GND	FBD_D50	GND	GND	FBD_D56	GND	GND	FBD_D32	GND	GND	FBD_D41	GND	GND	FBC_D10	GND	GND	FBC_D1	GND	GND	FBC_D7	GND	GND	FBC_D19	GND	FBC_D49	GND	FBC_D50	BVDDQ_SENS	FBC_D55	GND	FBC_CMD47	FBC_CMD48	H	8
9	J	FBE_CMD28	GND	~x	GND	~x	GND	~x	GND	~x	GND	GND	~x	GND	GND	~x	GND	GND	~x	FBD_D13	GND	~x	FBD_D1	GND	~x	FBD_D27	GND	~x	FBD_D30	GND	~x	FBD_D51	GND	~x	FBD_D48	GND	~x	FBD_D61	GND	~x	FBD_D38	GND	~x	FBD_D45	GND	~x	FBC_D15	GND	~x	FBC_D4	FBC_D27	~x	FBC_D31	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBC_CMD46	J	9
10	K	FBE_CMD30	FBE_CMD29	FBE_D41	GND	FBE_D40	FBE_D43	GND	FBE_D42	GND	FBE_D46	FBE_D47	GND	IVHS_HVD	IVHS_HVD	GND	IVHS_HVD	IVHS_HVD	GND	IVHS_HVD	IVHS_HVD	GND	FBD_D12	FBD_D7	GND	GND	FBD_D31	GND	GND	FBD_D22	GND	GND	FBD_D49	GND	GND	FBD_D57	GND	GND	FBD_D39	GND	GND	FBD_D43	GND	GND	FBC_D13	GND	GND	FBC_D12	GND	FBC_WCKB23	FBC_WCK23_N	GND	FB_VREF	FBC_CLK0	FBC_CLK0_N	GND	FBC_DQM6	FBC_D52	GND	FBC_DQS_WP6	FBC_CMD45	FBC_CMD43	FBC_CMD44	K	10
11	L	FBE_CMD32	FBE_CMD31	FBE_CMD33	FBE_DQS_WP5	GND	FBE_D45	FBE_DQM5	GND	FBE_D44	FBE_D39	FBE_D38	~x	IVHS_HVD	IVHS_HVD	~x	IVHS_HVD	IVHS_HVD	~x	IVHS_HVD	NVHS0_PLL_HVD	~x	FBD_WCKB01_N	FBD_WCK01_N	~x	FBD_WCKB23	FBD_WCK23_N	~x	FBD_D17	GND	~x	FBD_CLK0	FBD_CLK1_N	~x	FBD_WCK67_N	FBD_WCKB67	~x	FBD_D62	GND	~x	FBD_WCK45	FBD_WCKB45_N	~x	FBD_D47	GND	~x	FBC_WCKB01	FBC_WCK01	~x	FBC_WCKB23_N	FBC_WCK23	~x	FBC_CLK1_N	FBC_CLK1	GND	FBC_D57	GND	FBC_D59	FBC_D58	GND	FBC_D60	FBC_CMD41	FBC_CMD42	L	11
12	M	FBE_CMD34	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	IVHS_DVD	IVHS_DVD	GND	IVHS_DVD	IVHS_DVD	GND	IVHS_DVD	IVHS_DVD	GND	FBD_WCKB01	FBD_WCK01	GND	FBD_WCKB23_N	FBD_WCK23	GND	FBD_CMD27	FBD_D19	GND	FBD_CLK0_N	FBD_CLK1	GND	FBD_WCK67	FBD_WCKB67_N	GND	FBD_CMD55	FBD_D36	GND	FBD_WCK45_N	FBD_WCKB45	GND	GND	FBC_CMD27	GND	FBC_WCKB01_N	FBC_WCK01_N	GND	CAL_TERM_	CAL_PU_G	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBC_CMD40	M	12
13	N	FBE_CMD36	FBE_CMD35	FBE_D35	GND	FBE_D32	FBE_D34	GND	FBE_D36	GND	FBE_D37	FBE_WCKB45	FBE_WCKB45_N	~x	IVHS_DVD	~x	IVHS_DVD	IVHS_DVD	~x	IVHS_DVD	IVHS_DVD	~x	IVHS_DVD	IVHS_DVD	~x	IVHS_DVD	FB_PLLVDD	~x	FBVDDQ	FBVDDQ	~x	FBVDDQ	FBVDDQ	~x	FBVDDQ	FBVDDQ	~x	FBVDDQ	FB_PLLVDD	~x	FBVDDQ	FBVDDQ	~x	FBVDDQ	FBVDDQ	~x	FBVDDQ	FB_PLLVDD	~x	FBVDDQ	~x	CAL_PD_VD	FBC_WCK67_N	FBC_WCK67	FBC_D56	GND	FBC_DQM7	FBC_D62	GND	FBC_DQS_WP7	FBC_CMD39	FBC_CMD37	FBC_CMD38	N	13
14	P	FBE_CMD38	FBE_CMD37	FBE_CMD39	FBE_DQS_WP4	GND	FBE_D33	FBE_DQM4	GND	FBE_D58	FBE_D57	FBE_WCK45	FBE_WCK45_N	IVHS_DVD	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	FBVDDQ	FBVDDQ	FBC_WCKB67_N	FBC_WCKB67	GND	FBC_D61	GND	FBC_D63	FBC_D35	GND	FBC_D33	FBC_CMD35	FBC_CMD36	P	14
15	R	FBE_CMD40	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	~x	~x	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	~x	~x	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBC_CMD34	R	15
16	T	FBE_CMD42	FBE_CMD41	FBE_D56	GND	FBE_D59	FBE_D60	GND	FBE_D62	GND	FBE_D61	GND	FBE_D63	FBE_CMD55	NVHS_CVDD	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	FBVDDQ	GND	FBC_D34	GND	FBC_D37	FBC_D32	GND	FBC_DQM4	FBC_D36	GND	FBC_DQS_WP4	FBC_CMD33	FBC_CMD31	FBC_CMD32	T	16
17	U	FBE_CMD44	FBE_CMD43	FBE_CMD45	FBE_DQS_WP7	GND	FBE_D54	FBE_DQM7	GND	FBE_D53	FBE_D55	FBE_D52	FBE_WCKB67	FBE_WCKB67_N	NVHS_CVDD	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	FB_PLLVDD	FBC_WCK45	FBC_WCK45_N	GND	FBC_D39	GND	FBC_D38	GND	FBC_D42	FBC_D43	GND	FBC_D47	FBC_CMD29	FBC_CMD30	U	17
18	V	FBE_CMD46	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBC_CMD28	V	18
19	W	FBE_CMD48	FBE_CMD47	FBE_D50	GND	FBE_D48	FBE_D51	GND	FBE_D49	GND	FBE_D23	GND	FBE_WCK67_N	FBE_WCK67	FB_PLLVDD	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	FBVDDQ	FBC_WCKB45_N	FBC_WCKB45	FBC_D40	GND	FBC_D44	GND	FBC_DQM5	FBC_D45	GND	FBC_DQS_WP5	FBB_CMD0	FBB_CMD2	FBB_CMD1	W	19
20	Y	FBE_CMD50	FBE_CMD49	FBE_CMD51	FBE_DQS_WP6	GND	FBE_D21	FBE_DQM6	GND	FBE_D16	GND	FBE_D22	FBE_CLK1_N	FBE_CLK1	FBVDDQ	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	FBVDDQ	FBC_CMD55	FBC_D41	GND	FBC_D46	GND	FBB_D11	GND	FBB_D13	FBB_D9	GND	FBB_D15	FBB_CMD4	FBB_CMD3	Y	20
21	AA	FBE_CMD52	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBB_CMD5	AA	21
22	AB	FBE_CMD54_NC	FBE_CMD53_NC	FBE_D20	GND	FBE_D18	FBE_D17	GND	FBE_D19	GND	FBE_D27	GND	FBE_CLK0_N	FBE_CLK0	FBVDDQ	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	FBVDDQ	FBB_WCKB01	FBB_WCKB01_N	FBB_D12	GND	FBB_D10	GND	FBB_DQM1	FBB_D14	GND	FBB_DQS_WP1	FBB_CMD6	FBB_CMD8	FBB_CMD7	AB	22
23	AC	FBE_CMD25_NC	FBE_CMD26_NC	FBE_CMD24	FBE_DQS_WP2	GND	FBE_D24	FBE_DQM2	GND	FBE_D26	FBE_D25	GND	FBE_D4	GND	FBVDDQ	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	FBVDDQ	FBB_WCK01	FBB_WCK01_N	GND	FBB_D8	GND	FBB_D1	GND	FBB_D2	FBB_D5	GND	FBB_D6	FBB_CMD10	FBB_CMD9	AC	23
24	AD	FBE_CMD23	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBB_CMD11	AD	24
25	AE	FBE_CMD21	FBE_CMD22	FBE_D29	GND	FBE_D30	FBE_D31	GND	FBE_D28	GND	GND	FBE_D2	FBE_WCK23	FBE_WCK23_N	FB_PLLVDD	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	FBVDDQ	FBB_CMD27	GND	FBB_D0	GND	FBB_D3	GND	FBB_DQM0	FBB_D7	GND	FBB_DQS_WP0	FBB_CMD12	FBB_CMD14	FBB_CMD13	AE	25
26	AF	FBE_CMD19	FBE_CMD20	FBE_CMD18	FBE_DQS_WP3	GND	FBE_D0	FBE_DQM3	GND	FBE_D6	FBE_D7	GND	FBE_WCKB23_N	FBE_WCKB23	FBVDDQ	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	FB_PLLVDD	FBB_WCKB23_N	FBB_WCKB23	GND	FBB_D25	GND	FBB_D4	GND	FBB_D24	FBB_D26	GND	FBB_D27	FBB_CMD16	FBB_CMD15	AF	26
27	AG	FBE_CMD17	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBB_CMD17	AG	27
28	AH	FBE_CMD15	FBE_CMD16	FBE_D1	GND	FBE_D3	FBE_D5	GND	FBE_D14	GND	GND	FBE_D12	GND	FBE_D15	FBVDDQ	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	FBVDDQ	FBB_WCK23_N	FBB_WCK23	FBB_D30	GND	FBB_D28	GND	FBB_DQM3	FBB_D29	GND	FBB_DQS_WP3	FBB_CMD18	FBB_CMD20	FBB_CMD19	AH	28
29	AJ	FBE_CMD13	FBE_CMD14	FBE_CMD12	FBE_DQS_WP0	GND	FBE_D8	FBE_DQM0	GND	FBE_D10	GND	FBE_D13	GND	FBE_CMD27	FBVDDQ	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	FBVDDQ	FBB_CLK0	FBB_CLK0_N	GND	FBB_D31	GND	FBB_D22	GND	FBB_D21	FBB_D20	GND	FBB_D16	FBB_CMD22	FBB_CMD21	AJ	29
30	AK	FBE_CMD11	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBB_CMD23	AK	30
31	AL	FBE_CMD9	FBE_CMD10	FBE_D9	GND	FBE_D11	FBF_D45	GND	FBF_D41	GND	FBF_D44	GND	FBE_WCK01_N	FBE_WCK01	FBVDDQ	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	FBVDDQ	FBB_CLK1_N	FBB_CLK1	FBB_D23	GND	FBB_D19	GND	FBB_DQM2	FBB_D18	GND	FBB_DQS_WP2	FBB_CMD24	FBB_CMD26_NC	FBB_CMD25_NC	AL	31
32	AM	FBE_CMD7	FBE_CMD8	FBE_CMD6	FBE_DQS_WP1	GND	FBF_D43	FBE_DQM1	GND	FBF_D46	GND	FBF_D47	FBE_WCKB01	FBE_WCKB01_N	FBVDDQ	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	FBVDDQ	FBB_WCK67_N	FBB_WCK67	GND	FBB_D49	GND	FBB_D53	GND	FBB_D55	FBB_D54	GND	FBB_D17	FBB_CMD53_NC	FBB_CMD54_NC	AM	32
33	AN	FBE_CMD5	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBB_CMD52	AN	33
34	AP	FBE_CMD3	FBE_CMD4	FBF_D42	GND	FBF_D40	FBF_D36	GND	FBF_D37	GND	FBF_D39	GND	FBF_D38	GND	FBVDDQ	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	FBVDDQ	FBB_WCKB67_N	FBB_WCKB67	FBB_D52	GND	FBB_D51	GND	FBB_DQM6	FBB_D50	GND	FBB_DQS_WP6	FBB_CMD51	FBB_CMD49	FBB_CMD50	AP	34
35	AR	FBE_CMD1	FBE_CMD2	FBE_CMD0	FBF_DQS_WP5	GND	FBF_D32	FBF_DQM5	GND	FBF_D35	FBF_D33	GND	FBF_D34	FBF_CMD55	FBVDDQ	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	FBVDDQ	GND	FBB_D62	GND	FBB_D59	GND	FBB_D63	GND	FBB_D61	FBB_D60	GND	FBB_D48	FBB_CMD47	FBB_CMD48	AR	35
36	AT	FBF_CMD28	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBB_CMD46	AT	36
37	AU	FBF_CMD30	FBF_CMD29	FBF_D56	GND	FBF_D58	FBF_D57	GND	FBF_D59	GND	GND	FBF_D61	FBF_WCKB45	FBF_WCKB45_N	GPCADC_AVDD	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	FBVDDQ	FBB_CMD55	GND	FBB_D58	GND	FBB_D57	GND	FBB_DQM7	FBB_D56	GND	FBB_DQS_WP7	FBB_CMD45	FBB_CMD43	FBB_CMD44	AU	37
38	AV	FBF_CMD32	FBF_CMD31	FBF_CMD33	FBF_DQS_WP4	GND	FBF_D60	FBF_DQM4	GND	FBF_D63	FBF_D62	GND	FBF_WCK45_N	FBF_WCK45	FBVDDQ	~x	VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS	~x	FBVDDQ	FBB_WCK45	FBB_WCK45_N	GND	FBB_D38	GND	FBB_D34	GND	FBB_D35	FBB_D32	GND	FBB_D33	FBB_CMD41	FBB_CMD42	AV	38
39	AW	FBF_CMD34	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBB_CMD40	AW	39
40	AY	FBF_CMD36	FBF_CMD35	FBF_D53	GND	FBF_D52	FBF_D54	GND	FBF_D55	GND	GND	FBF_D50	FBF_WCKB67_N	FBF_WCKB67	FBVDDQ	~x	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	~x	FBVDDQ	FBB_WCKB45_N	FBB_WCKB45	FBB_D39	GND	FBB_D37	GND	FBB_DQM4	FBB_D36	GND	FBB_DQS_WP4	FBB_CMD39	FBB_CMD37	FBB_CMD38	AY	40
41	BA	FBF_CMD38	FBF_CMD37	FBF_CMD39	FBF_DQS_WP7	GND	FBF_D48	FBF_DQM7	GND	FBF_D51	GND	FBF_D49	FBF_WCK67_N	FBF_WCK67	FB_PLLVDD	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	FBVDDQ	FBA_CMD27	FBB_D40	GND	FBB_D44	GND	FBB_D41	GND	FBB_D42	FBB_D43	GND	FBB_D46	FBB_CMD35	FBB_CMD36	BA	41
42	BB	FBF_CMD40	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBB_CMD34	BB	42
43	BC	FBF_CMD42	FBF_CMD41	FBF_D19	GND	FBF_D16	FBF_D20	GND	FBF_D21	GND	FBF_D17	GND	FBF_CLK1	FBF_CLK1_N	FBVDDQ	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	FBVDDQ	FBA_WCKB01	FBA_WCKB01_N	FBA_D14	GND	FBB_D45	GND	FBB_DQM5	FBB_D47	GND	FBB_DQS_WP5	FBB_CMD33	FBB_CMD31	FBB_CMD32	BC	43
44	BD	FBF_CMD44	FBF_CMD43	FBF_CMD45	FBF_DQS_WP6	GND	FBF_D22	FBF_DQM6	GND	FBF_D23	GND	FBF_D18	FBF_CLK0	FBF_CLK0_N	FBVDDQ	~x	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	~x	FBVDDQ	FBA_WCK01	FBA_WCK01_N	GND	FBA_D12	GND	FBA_D13	GND	FBA_D8	FBA_D11	GND	FBA_D9	FBB_CMD29	FBB_CMD30	BD	44
45	BE	FBF_CMD46	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBB_CMD28	BE	45
46	BF	FBF_CMD48	FBF_CMD47	FBF_D28	GND	FBF_D29	FBF_D26	GND	FBF_D30	GND	GND	FBF_D31	FBF_WCK23	FBF_WCK23_N	FBVDDQ	~x	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	~x	FB_PLLVDD	FBA_WCKB23_N	FBA_WCKB23	FBA_D2	GND	FBA_D15	GND	FBA_DQM1	FBA_D10	GND	FBA_DQS_WP1	FBA_CMD0	FBA_CMD2	FBA_CMD1	BF	46
47	BG	FBF_CMD50	FBF_CMD49	FBF_CMD51	FBF_DQS_WP2	GND	FBF_D25	FBF_DQM2	GND	FBF_D24	FBF_D27	GND	FBF_WCKB23_N	FBF_WCKB23	FBVDDQ	~x	VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS	~x	FBVDDQ	FBA_WCK23	FBA_WCK23_N	GND	FBA_D4	GND	FBA_D0	GND	FBA_D3	FBA_D5	GND	FBA_D6	FBA_CMD4	FBA_CMD3	BG	47
48	BH	FBF_CMD52	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	~x	~x	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	~x	~x	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBA_CMD5	BH	48
49	BJ	FBF_CMD54_NC	FBF_CMD53_NC	FBF_D7	GND	FBF_D4	FBF_D6	GND	FBF_D5	GND	FBF_WCK01_N	FBF_WCK01	FBF_CMD27	FBVDDQ	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	~x	FBVDDQ	FBVDDQ	FBA_CLK0_N	FBA_CLK0	FBA_D7	GND	FBA_DQM0	FBA_D1	GND	FBA_DQS_WP0	FBA_CMD6	FBA_CMD8	FBA_CMD7	BJ	49
50	BK	FBF_CMD25_NC	FBF_CMD26_NC	FBF_CMD24	FBF_DQS_WP3	GND	FBF_D2	FBF_DQM3	GND	FBF_D3	FBF_D1	FBF_WCKB01	FBF_WCKB01_N	~x	1V8	~x	NC	NC	~x	RSVD	IFP_IOVDD	~x	IFP_IOVDD	IFP_IOVDD	~x	IFP_IOVDD	IFP_IOVDD	~x	IFP_IOVDD	IFP_IOVDD	~x	RE_PLL_AV	PEX_CVDD	~x	PEX_DVDD	PEX_DVDD	~x	PEX_DVDD	PEX_DVDD	~x	PEX_DVDD	PEX_DVDD	~x	PEX_DVDD	PEX_DVDD	~x	FBVDDQ	FBVDDQ	~x	FBVDDQ	~x	FBVDDQ	FBA_CLK1	FBA_CLK1_N	FBA_D27	FBA_D24	GND	FBA_D25	FBA_D26	GND	GND	FBA_CMD10	FBA_CMD9	BK	50
51	BL	FBF_CMD23	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	1V8	1V8	GND	NC	NC	GND	RSVD	IFP_IOVDD	GND	PEF_PLLV	IFP_IOVDD	GND	PCD_PLLV	IFP_IOVDD	GND	PAB_PLLV	IFP_IOVDD	GND	VID_PLLVDD	PEX_CVDD	GND	PEX_DVDD	PEX_DVDD	GND	PEX_DVDD	PEX_DVDD	GND	PEX_DVDD	PEX_DVDD	GND	PEX_DVDD	PEX_DVDD	GND	VDD_SENSE	FBA_CMD55	GND	FBA_WCK45	FBA_WCK67_N	GND	~x	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBA_CMD11	BL	51
52	BM	FBF_CMD21	FBF_CMD22	FBF_D0	GND	FBF_D11	FBF_D9	GND	FBF_D10	TS_VREF	FBF_D8	GPIO24	~x	NC	1V8	~x	NC	NC	~x	NC	IFP_IOVDD	~x	SP_PLLVDD	IFPC_L3_N	X	IFPC_L0	IFPCD_RSET	X	IFPB_L1	IFPB_L0_N	X	NC	PEX_CVDD	X	PEX_HVDD	PEX_HVDD	X	PEX_HVDD	PEX_PLL_HVDD	X	PEX_HVDD	PEX_HVDD	~x	PEX_HVDD	PEX_HVDD	~x	GND_SENSE	FBA_WCKB45	~x	FBA_WCK45_N	FBA_WCK67	~x	FBA_WCKB67_N	FBA_D63	GND	FBA_D19	FBA_DQM3	FBA_D28	GND	FBA_DQS_WP3	FBA_CMD12	FBA_CMD14	FBA_CMD13	BM	52
53	BN	FBF_CMD19	FBF_CMD20	FBF_CMD18	FBF_DQS_WP0	GND	FBF_D12	FBF_DQM0	GPIO1	GPIO12	GPIO27	GPIO29	GND	OVERT	NC	GND	NC	NC	GND	NC	NC	GND	NC	IFPC_L3	GND	IFPC_L0_N	IFPB_L3_N	GND	IFPB_L1_N	IFPB_L0	GND	FUSE_SRC	NC	GND	PEX_HVDD	PEX_HVDD	GND	PEX_HVDD	PEX_HVDD	GND	PEX_HVDD	PEX_HVDD	GND	PEX_HVDD	PEX_HVDD	GND	FBA_D41	FBA_WCKB45_N	GND	FBA_D36	FBA_D33	GND	FBA_WCKB67	FBA_D58	GND	FBA_D17	GND	FBA_D29	FBA_D30	GND	FBA_D31	FBA_CMD16	FBA_CMD15	BN	53
54	BP	FBF_CMD17	GND	~x	GND	~x	GND	~x	GND	X	GPIO35	GPIO16	~x	RSVD	RSVD	~x	RSVD	RSVD	~x	GND	GND	X	GND	IFPEF_RSET	~x	GND	IFPB_L3	X	GND	IFPAB_RSET	X	GND	NC	X	GND	NC	X	GND	NC	X	GND	NC	~x	GND	PEX_CVDD	~x	GND	FBA_D47	~x	GND	FBA_D32	~x	FBA_D35	GND	~x	GND	~x	GND	~x	GND	~x	GND	FBA_CMD17	BP	54
55	BR	FBF_CMD15	FBF_CMD16	FBF_D14	GND	GND	FBF_D13	GPIO4	T_REFCLK_	GND	GPIO34	GPIO3	GND	RSVD	I2CC_SCL	GND	IFPD_AUX_	GND	GND	IFPF_L0	GND	GND	IFPE_L0	GND	GND	IFPC_L1	GND	GND	EX_CLKREQ	PEX_TX0	X	PEX_TX2	X	PEX_TX4	X	PEX_TX6	X	PEX_TX8	X	PEX_TX10	X	PEX_TX12	X	PEX_TX14	X	GND	FBA_D43	GND	GND	FBA_D37	GND	GND	FBA_D39	FBA_D59	GND	GND	FBA_DQM2	FBA_D18	GND	FBA_DQS_WP2	FBA_CMD20	FBA_CMD18	FBA_CMD19	BR	55
56	BT	FBF_CMD13	FBF_CMD14	FBF_CMD12	FBF_DQS_WP1	FBF_D15	GPIO10	GPIO15	GPIO9	~x	GPIO6	GPIO25	~x	GPIO28	I2CC_SDA	~x	FPD_AUX_SC	PB_AUX_SDA	~x	IFPF_L0_N	IFPE_L1_N	X	IFPE_L0_N	IFPC_L2_N	~x	IFPC_L1_N	IFPB_L2_N	X	PEX_RST_N	PEX_TX0_N	GND	PEX_TX2_N	GND	PEX_TX4_N	GND	PEX_TX6_N	GND	PEX_TX8_N	GND	PEX_TX10_N	GND	PEX_TX12_N	GND	PEX_TX14_N	GND	X	GND	FBA_DQM5	X	GND	FBA_DQM4	X	GND	FBA_DQM7	~x	FBA_D48	FBA_D49	FBA_D51	FBA_D16	FBA_D21	GND	FBA_CMD22	FBA_CMD21	BT	56
57	BU	FBF_CMD11	GND	GPIO17	GND	FBF_DQM1	GND	GPIO11	GPIO0	GND	XT_REFCLK_	GPIO21	GND	GPIO20	I2CS_SDA	GND	FPC_AUX_SC	FPB_AUX_SC	GND	IFPF_L1	IFPE_L1	GND	IFPD_L3_N	IFPC_L2	GND	IFPA_L3_N	IFPB_L2	GND	PEX_REFCLK	GND	PEX_TX1	GND	PEX_TX3	GND	PEX_TX5	GND	PEX_TX7	GND	PEX_TX9	GND	PEX_TX11	GND	PEX_TX13	GND	PEX_TX15	GND	FBA_D46	FBA_D42	GND	FBA_D34	FBA_D38	GND	FBA_D62	FBA_D56	GND	GND	FBA_D50	GND	FBA_D20	GND	FBA_D22	GND	FBA_CMD23	BU	57
58	BV	FBF_CMD9	FBF_CMD10	FBF_CMD8	GPIO18	GPIO8	GPIO14	GPIO33	STRAP5	~x	GPIO31	GPIO32	~x	GPIO19	I2CS_SCL	~x	PC_AUX_SDA	GND	~x	IFPF_L1_N	GND	X	IFPD_L3	GND	X	IFPA_L3	GND	X	PEX_REFCLK_N	X	PEX_TX1_N	X	PEX_TX3_N	X	PEX_TX5_N	X	PEX_TX7_N	X	PEX_TX9_N	X	PEX_TX11_N	X	PEX_TX13_N	X	PEX_TX15_N	X	FBA_D45	GND	X	FBA_D40	GND	X	FBA_D60	GND	~x	FBA_D55	GND	FBA_D53	GND	FBA_D23	FBA_CMD26_NC	FBA_CMD24	FBA_CMD25_NC	BV	58
59	BW	GND	FBF_CMD7	GND	GPIO13	GPIO2	GND	STRAP3	STRAP2	GND	GPIO30	GPIO23	GND	GPIO26	I2CB_SDA	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PEX_TERMP	FBA_DQS_WP5	GND	GND	FBA_DQS_WP4	GND	GND	FBA_DQS_WP7	GND	GND	FBA_D54	GND	FBA_D52	GND	FBA_CMD52	FBA_CMD54_NC	GND	BW	59
60	BY	GND	FBF_CMD6	FBF_CMD5	GND	GPIO7	GPIO5	STRAP4	TAL_OUTBUF	~x	ROM_SI	ROM_CS_N	~x	GPIO22	I2CB_SCL	~x	FPE_AUX_SC	IFPF_L3	~x	IFPF_L2_N	IFPE_L2	X	IFPD_L2_N	IFPD_L0	X	IFPA_L2	IFPA_L0	X	JTAG_TCK	JTAG_TDO	GND	PEX_RX0	GND	PEX_RX2	GND	PEX_RX4	GND	PEX_RX6	GND	PEX_RX8	GND	PEX_RX10	GND	PEX_RX12	GND	PEX_RX14	GND	GND	X	FBA_D44	FBA_CMD33	X	FBA_D57	FBA_CMD39	~x	FBA_D61	GND	FBA_DQM6	GND	FBA_DQS_WP6	FBA_CMD51	FBA_CMD53_NC	GND	BY	60
61	CA	GND	GND	FBF_CMD4	FBF_CMD3	FBF_CMD1	GND	STRAP0	XTAL_OUT	GND	ROM_SCLK	THERMDP	GND	ADC_IN_N	PF_AUX_SDA	GND	PE_AUX_SDA	IFPF_L3_N	GND	IFPF_L2	IFPE_L2_N	GND	IFPD_L2	IFPD_L0_N	GND	IFPA_L2_N	IFPA_L0_N	GND	JTAG_TMS	NVJTAG_SEL	GND	PEX_RX0_N	PEX_RX1	PEX_RX2_N	PEX_RX3	PEX_RX4_N	PEX_RX5	PEX_RX6_N	PEX_RX7	PEX_RX8_N	PEX_RX9	PEX_RX10_N	PEX_RX11	PEX_RX12_N	PEX_RX13	PEX_RX14_N	PEX_RX15	DDMS_SENS	GND	FBA_CMD29	FBA_CMD31	GND	FBA_CMD35	FBA_CMD37	GND	FBA_CMD41	FBA_CMD43	FBA_CMD45	FBA_CMD47	FBA_CMD49	FBA_CMD50	GND	GND	CA	61
62	CB	~x	GND	GND	GND	FBF_CMD2	FBF_CMD0	STRAP1	XTAL_IN	~x	ROM_SO	THERMDN	~x	ADC_IN	FPF_AUX_SC	~x	PA_AUX_SDA	FPA_AUX_SC	~x	IFPE_L3	IFPE_L3_N	X	IFPD_L1	IFPD_L1_N	X	IFPA_L1	IFPA_L1_N	X	JTAG_TRST_N	JTAG_TDI	PEX_WAKE_	X	PEX_RX1_N	X	PEX_RX3_N	X	PEX_RX5_N	X	PEX_RX7_N	X	PEX_RX9_N	X	PEX_RX11_N	X	PEX_RX13_N	X	PEX_RX15_N	NDMS_SENS	FBA_CMD28	FBA_CMD30	FBA_CMD32	FBA_CMD34	FBA_CMD36	FBA_CMD38	FBA_CMD40	FBA_CMD42	FBA_CMD44	FBA_CMD46	FBA_CMD48	GND	GND	GND	~x	CB	62
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62		

Note: "~x" means skip ball.

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