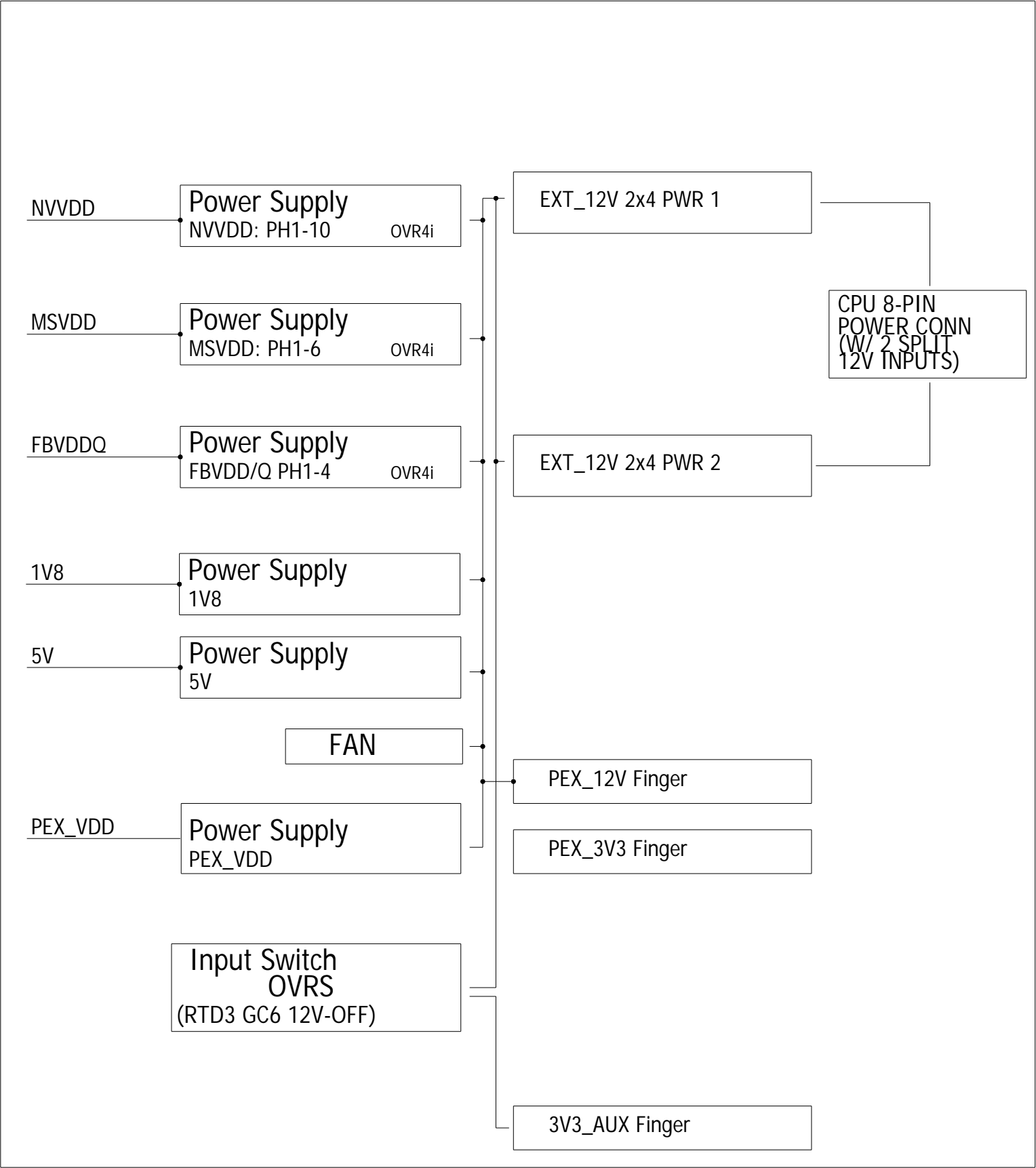
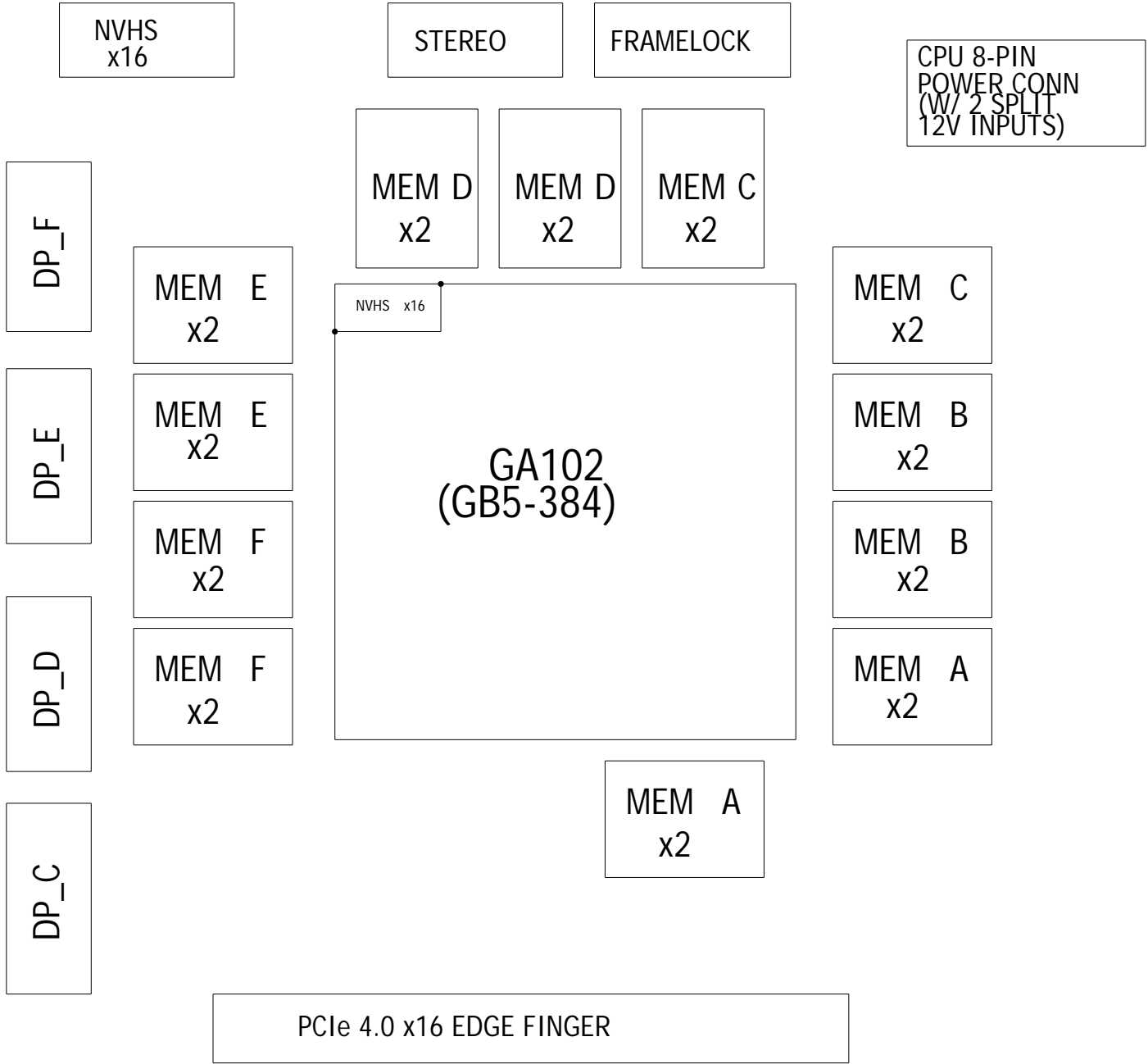


## 1

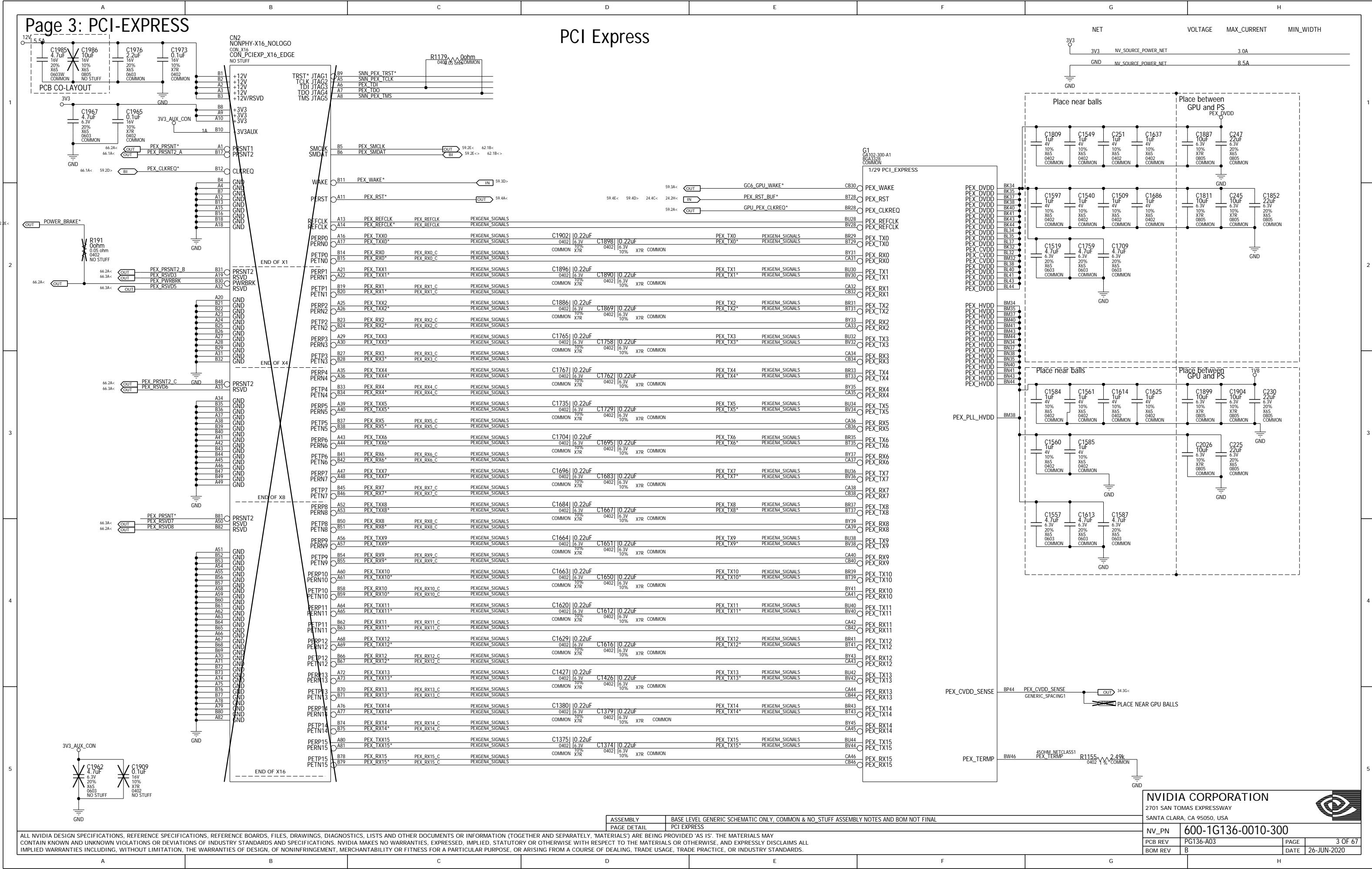
## 2

345

Page 2: Block Diagram



PCI Express



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ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO\_STUFF ASSEMBLY NOTES AND BOM NOT FINAL PCI EXPRESS

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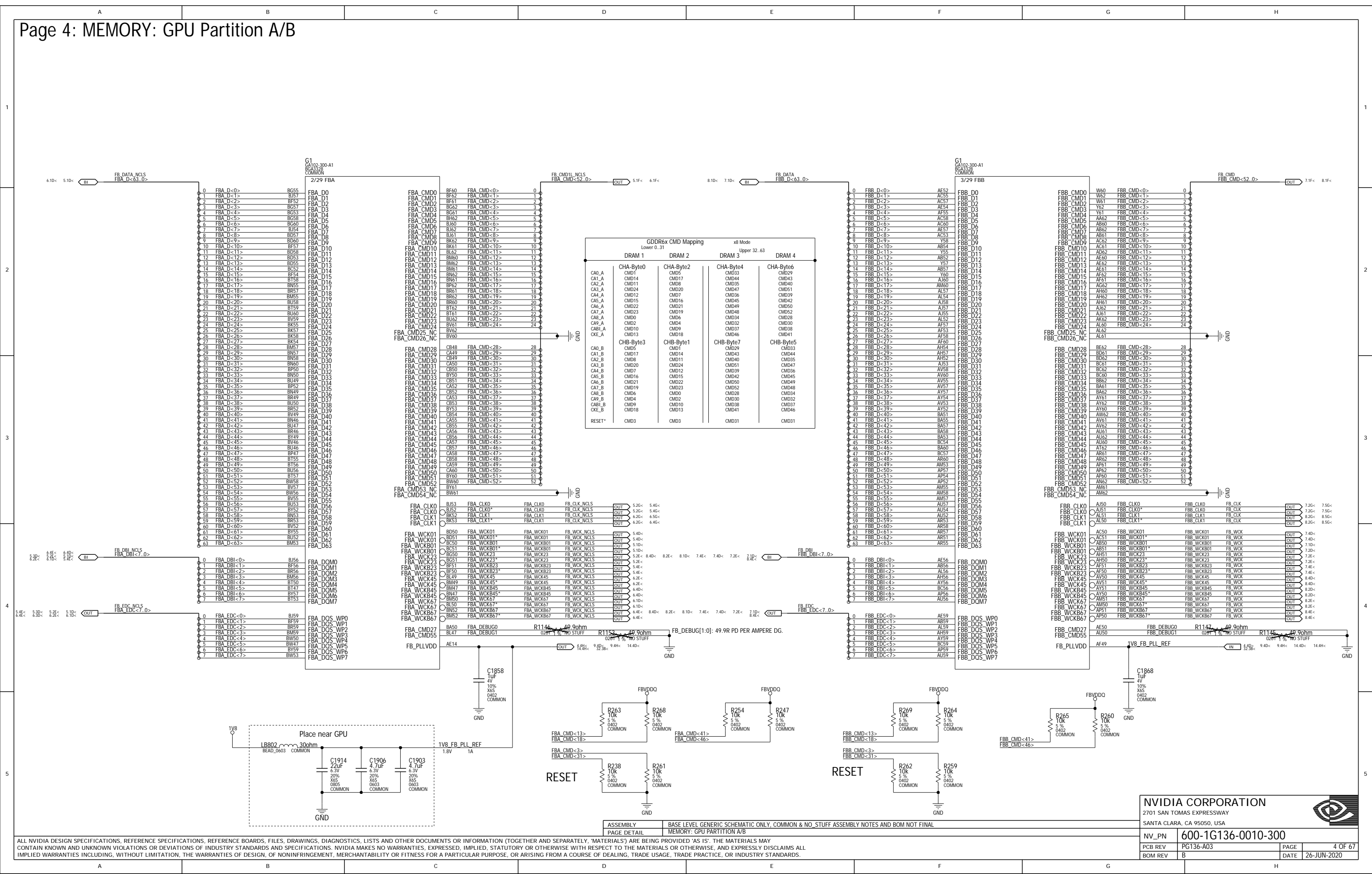
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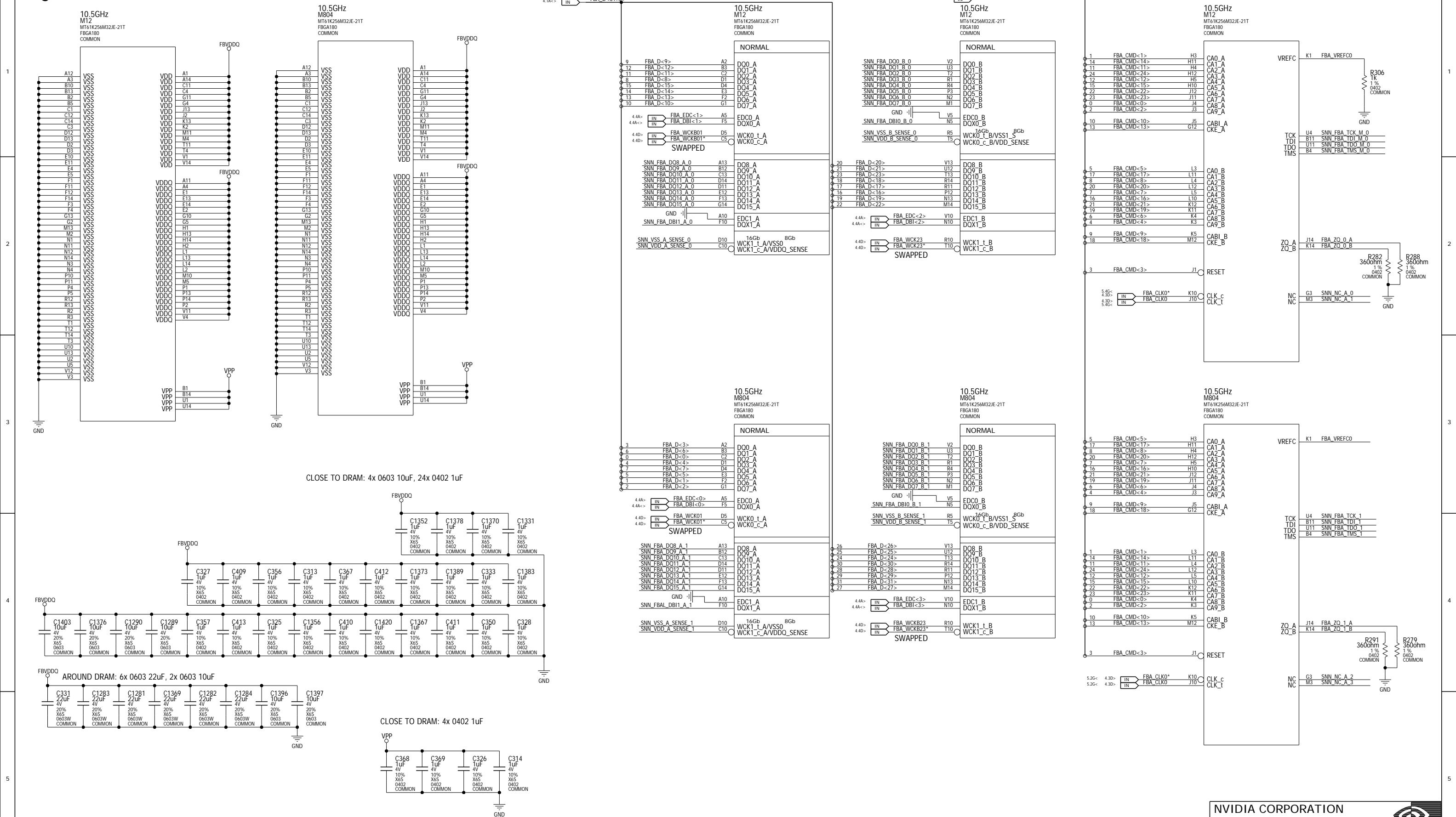
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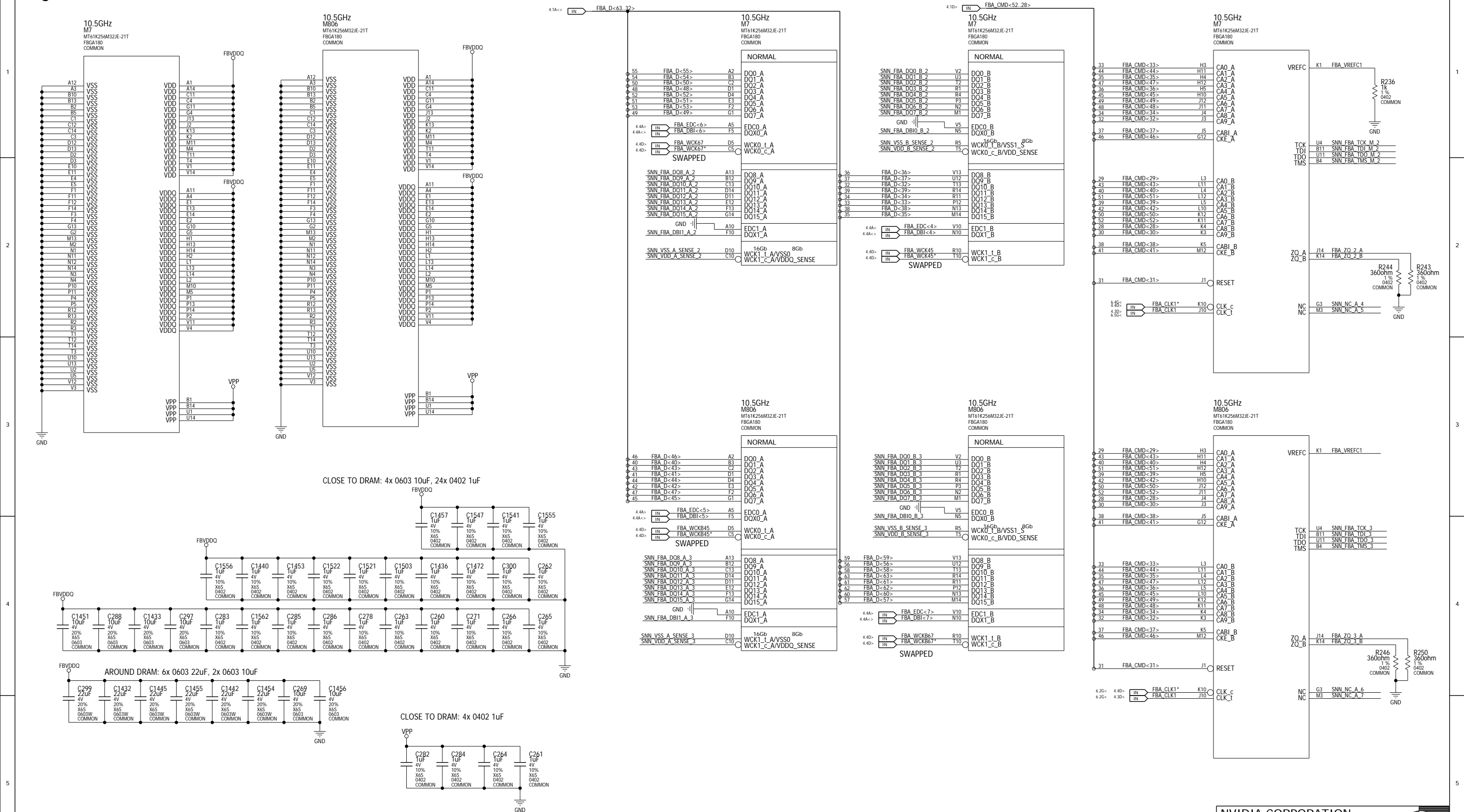
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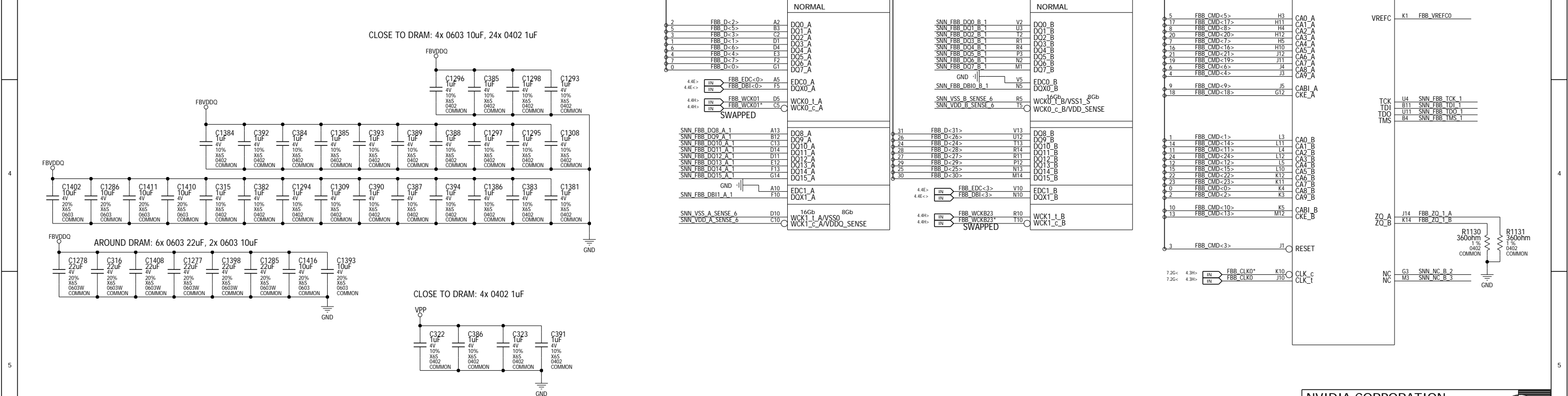
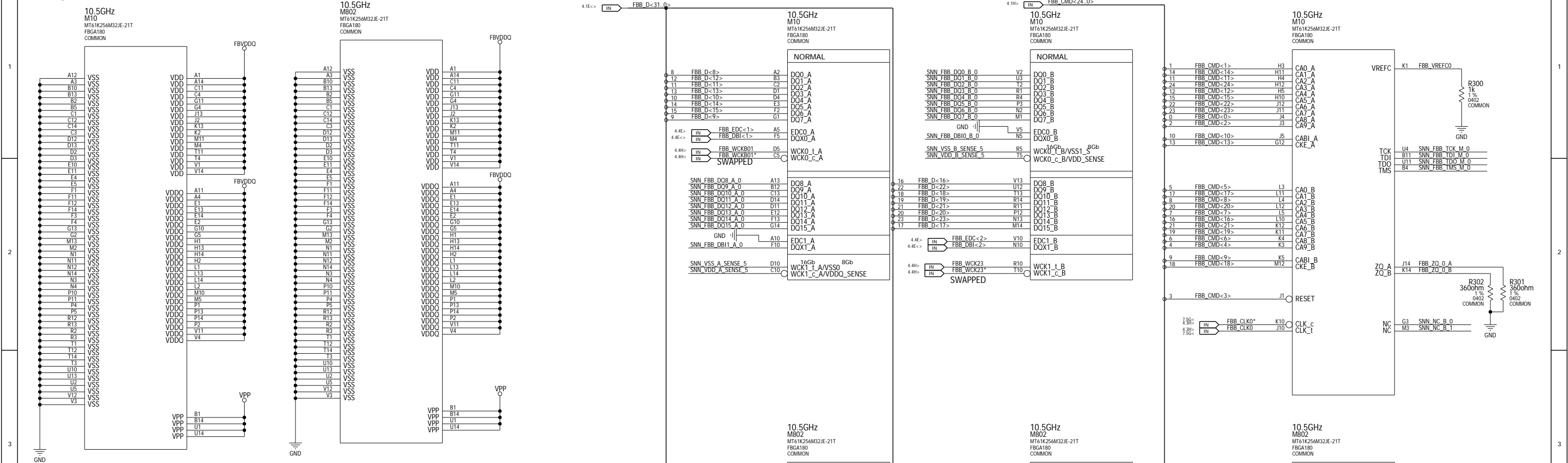
## Page5: MEMORY: FBA Partition 31..0



## Page6: MEMORY: FBA Partition 63..32

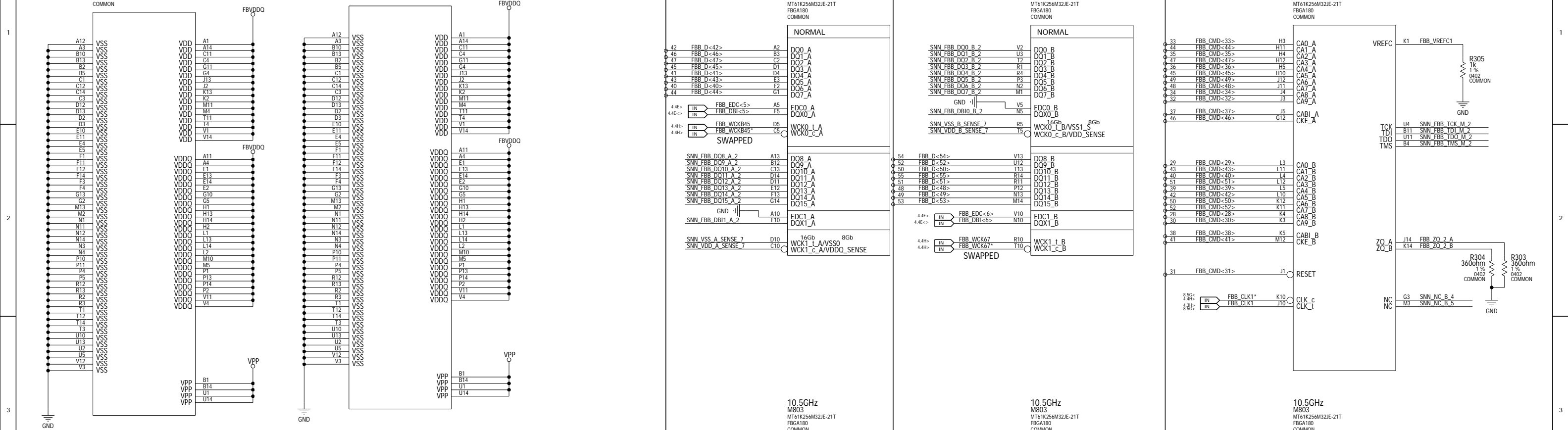


## Page7: MEMORY: FBB Partition 31..0

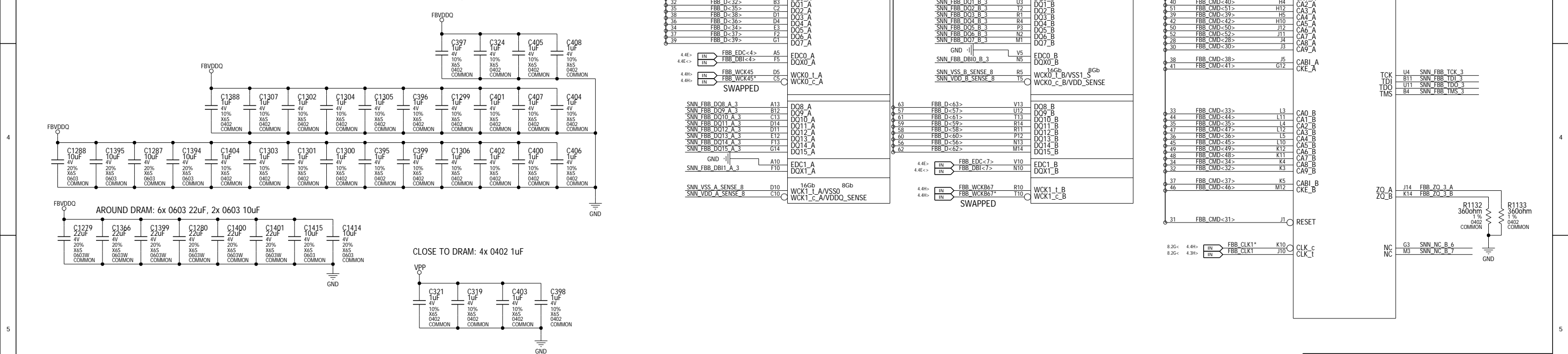


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PAGE DETAIL	MEMORY: FBB PARTITION[31:0]

10.5GHz	10.5GHz
M11	M803
MT61K256M32JE-21T	MT61K256M32JE-21T
FBGA180	FBGA180
	COMMON



CLOSE TO DRAM: 4x 0603 10uF, 24x 0402 1uF

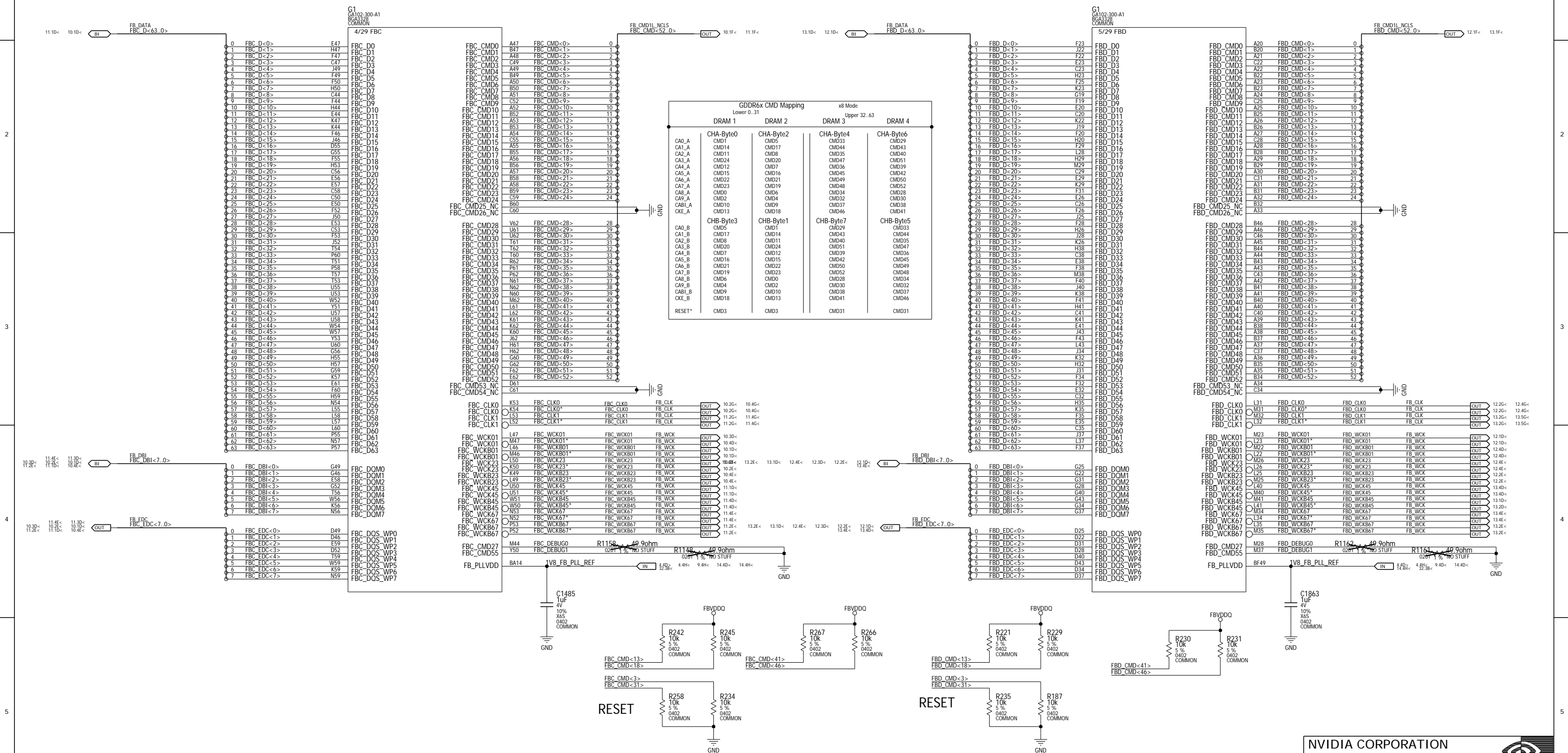


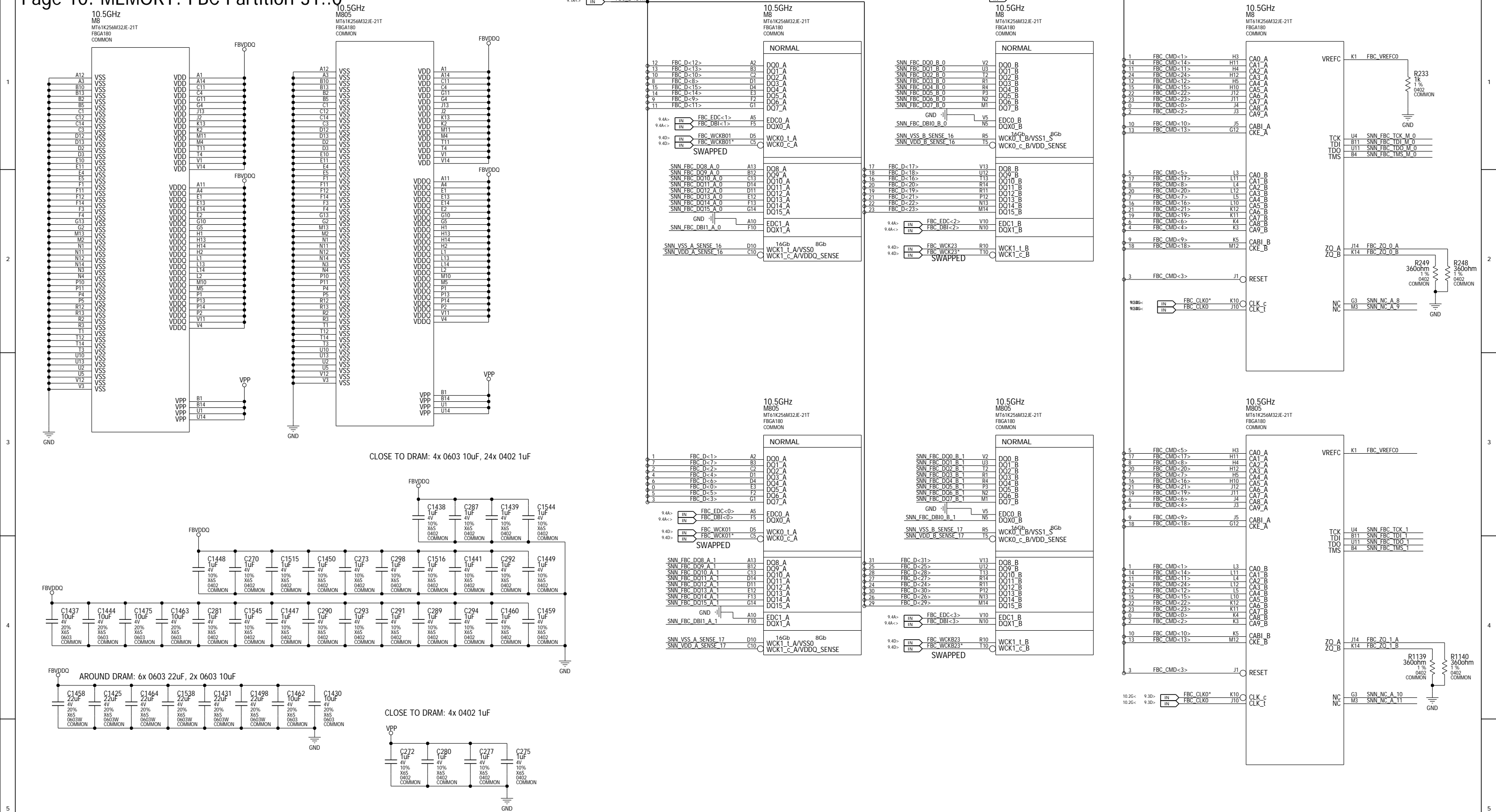
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PAGE DETAIL	MEMORY: FBB PARTITION[63:31]

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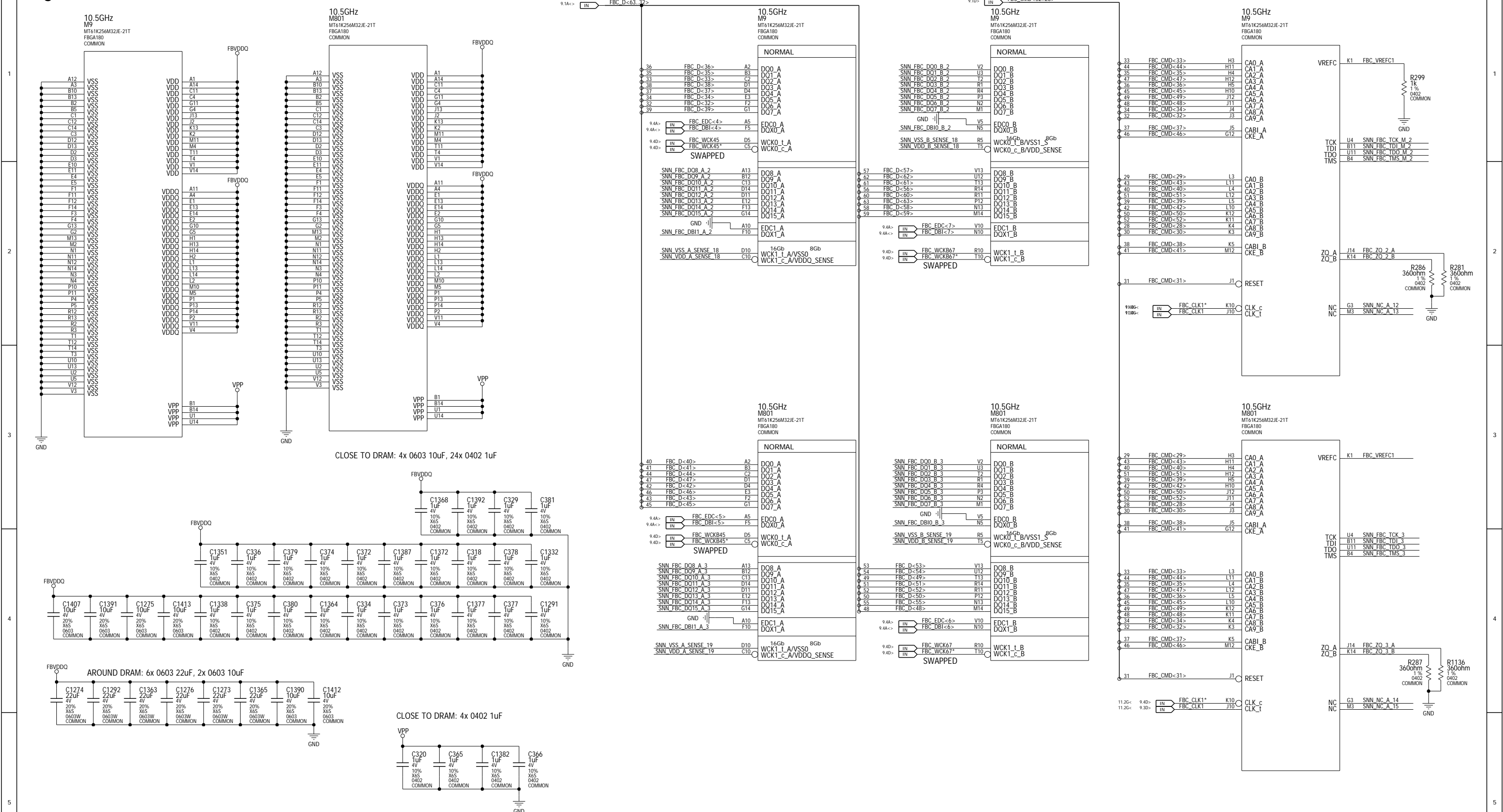








## Page 11: MEMORY: FBC Partition 63..32



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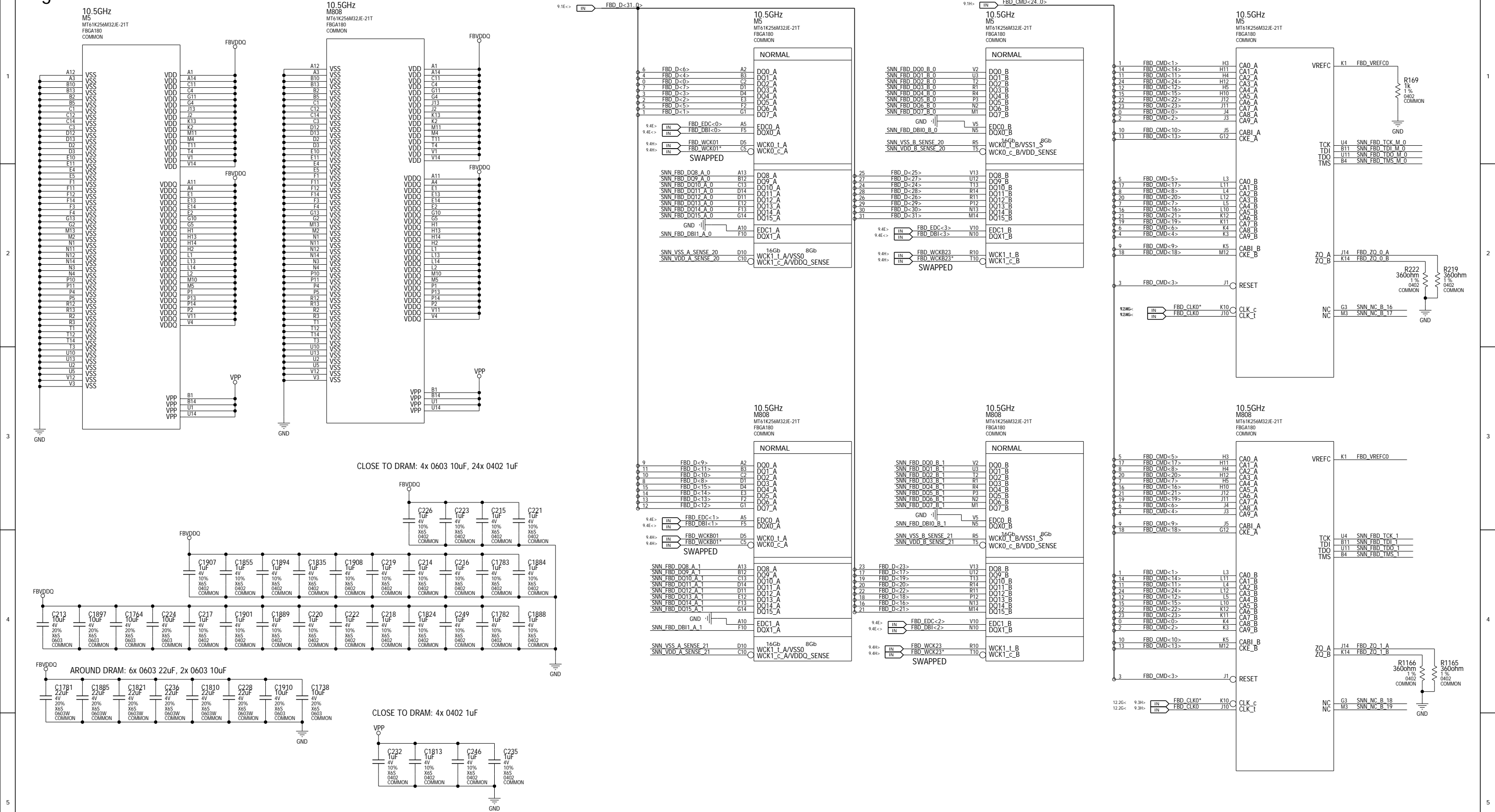
PAGE	11 OF 67
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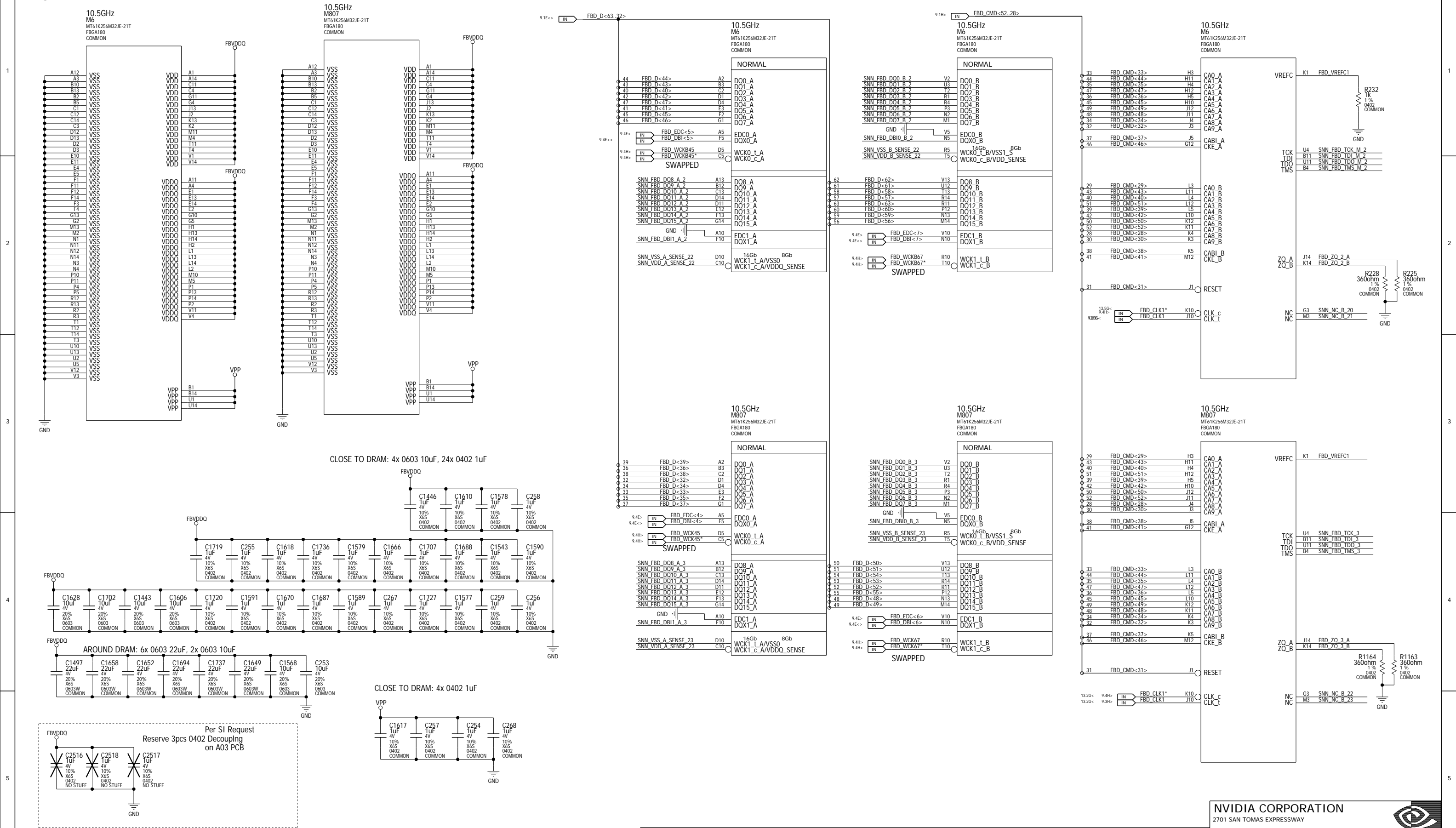
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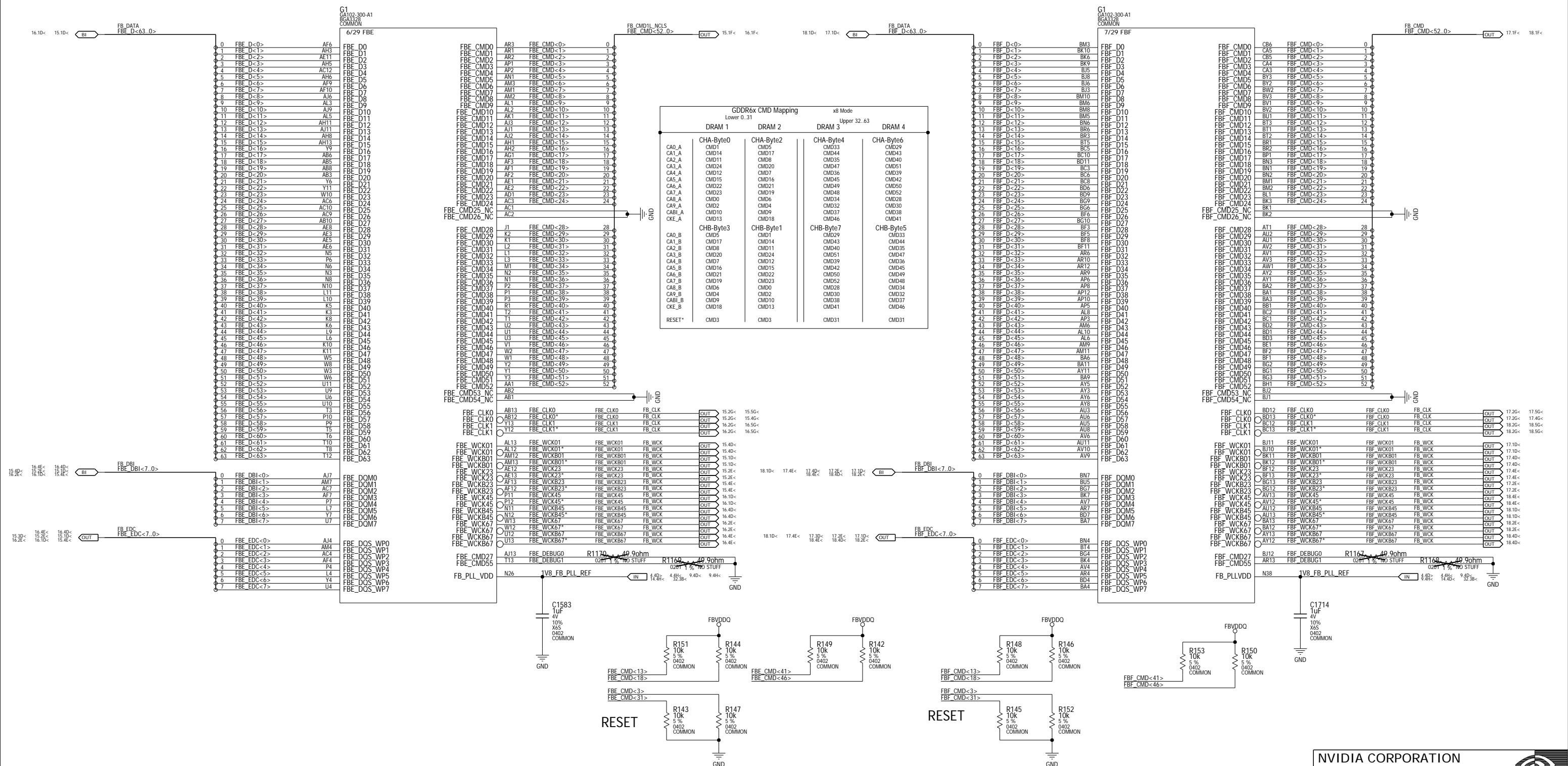
DATE	26-JUN-2020
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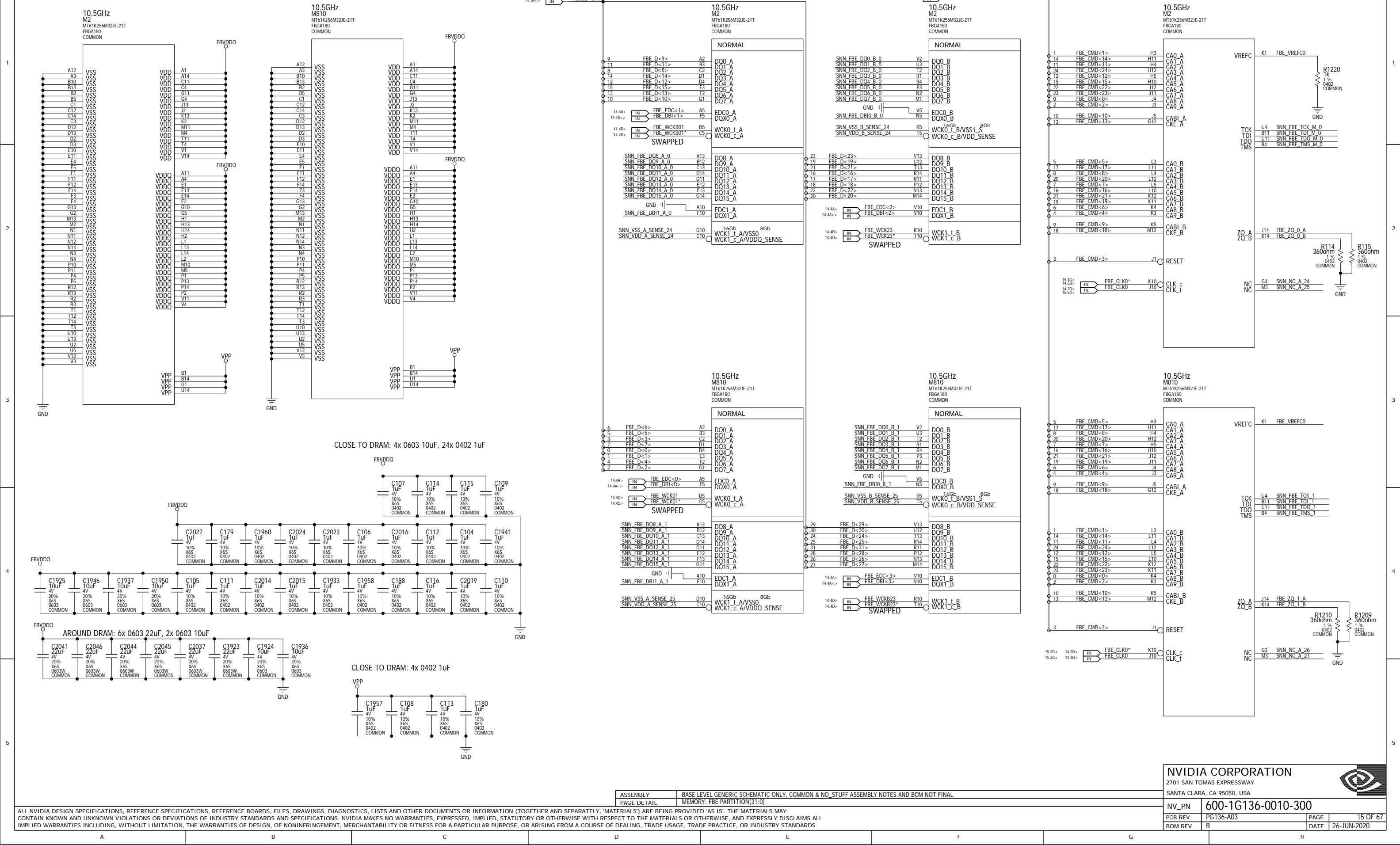
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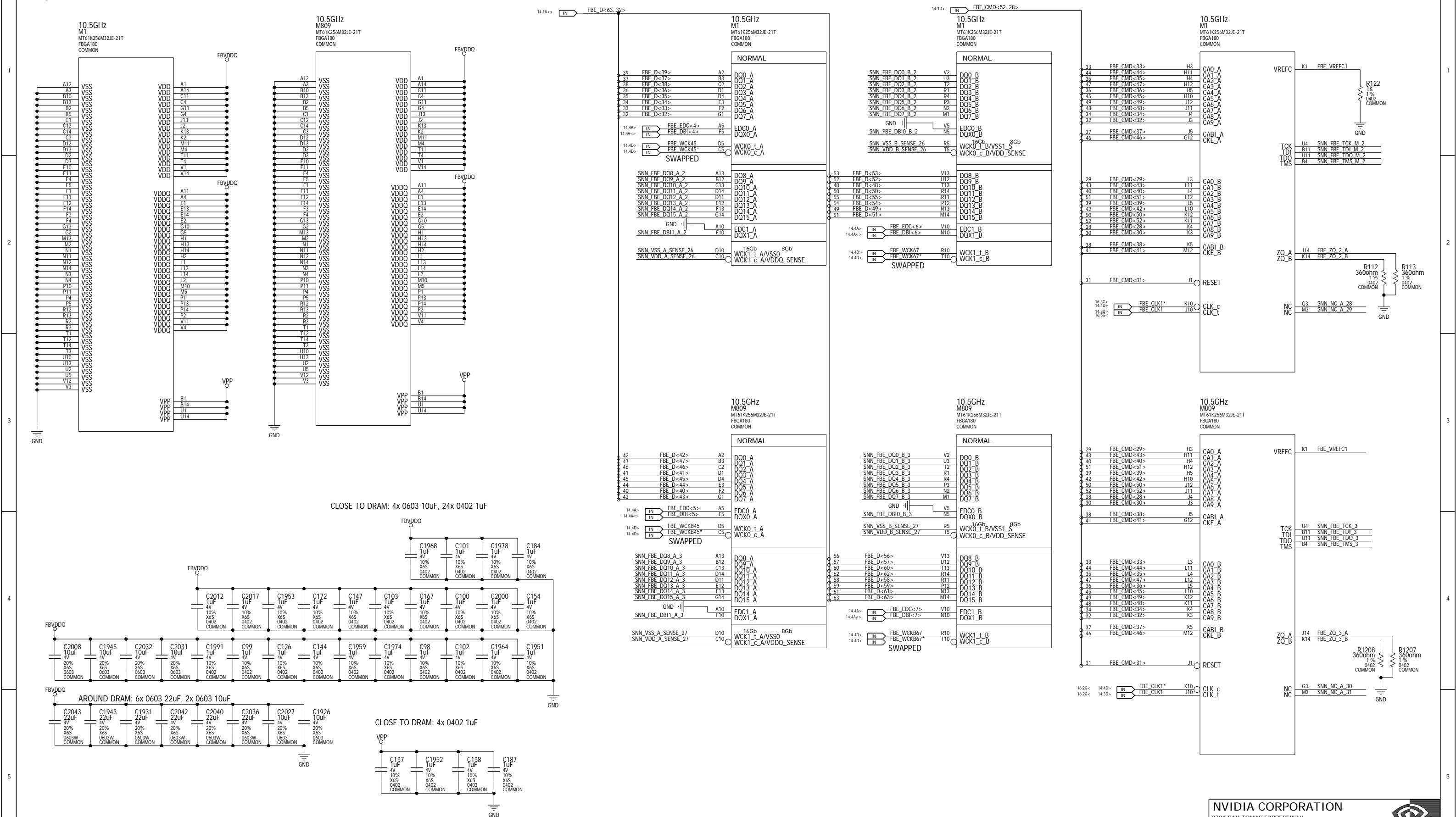
## Page 12: MEMORY: FBD Partition 31..0



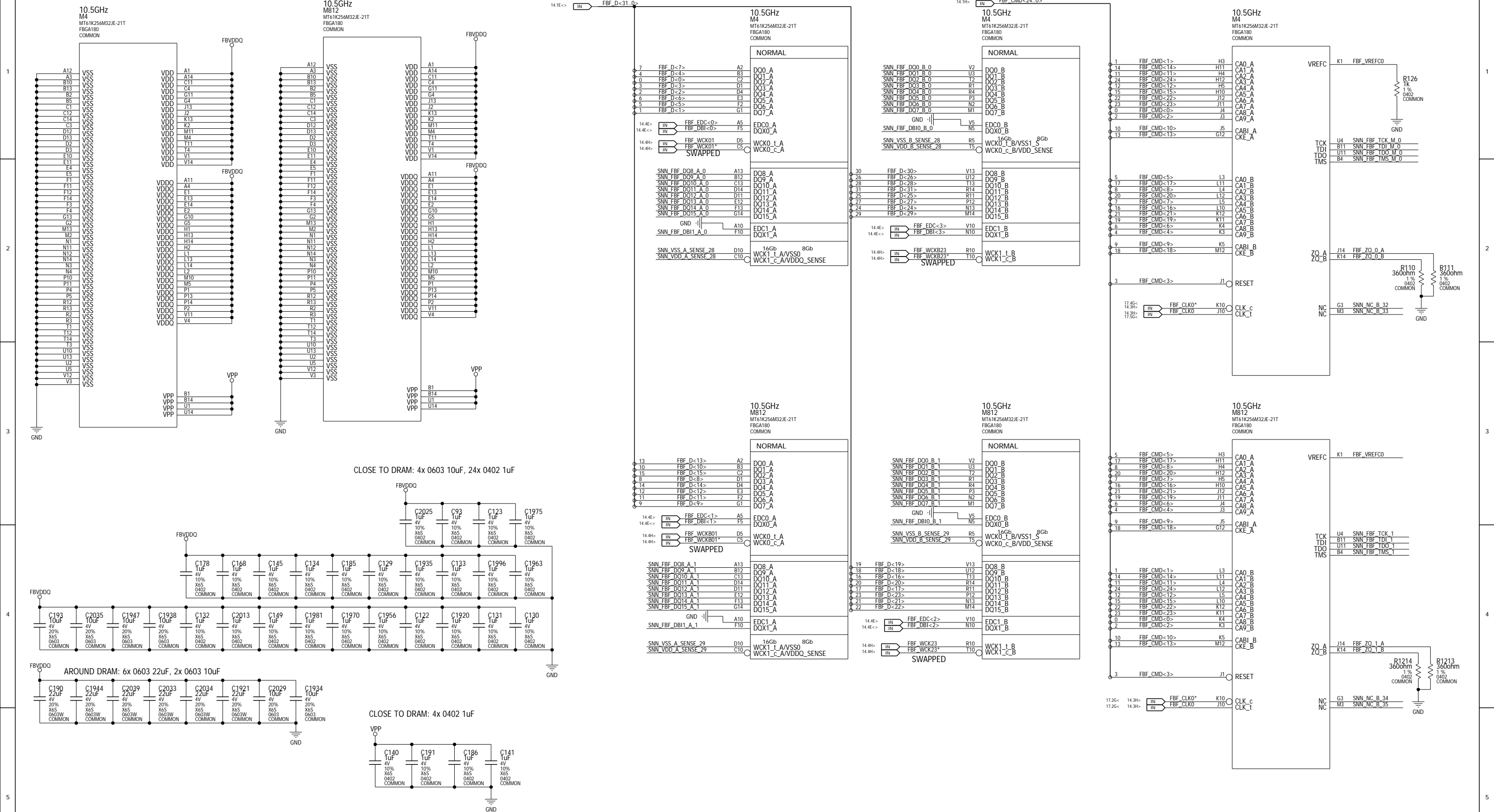


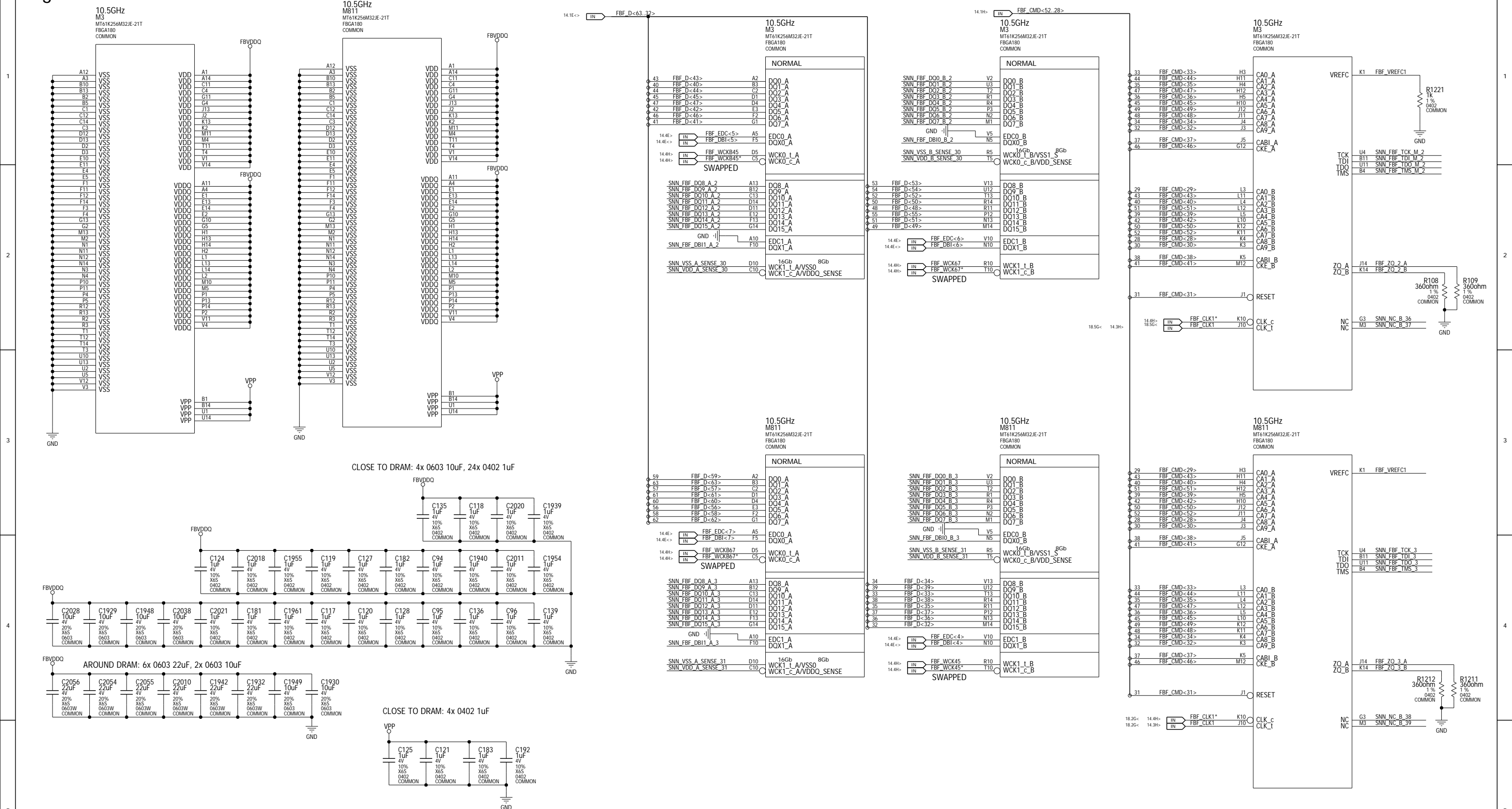




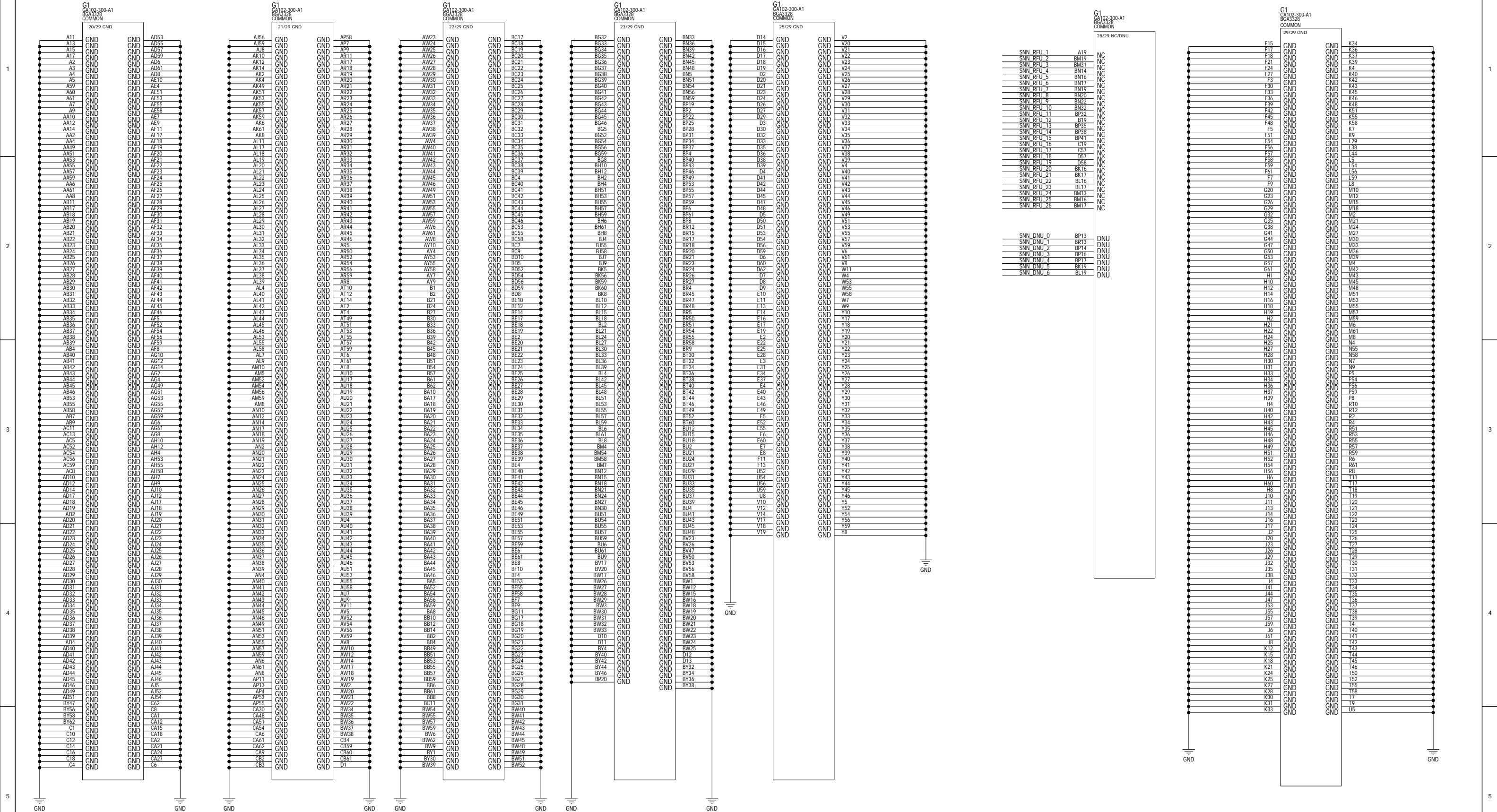








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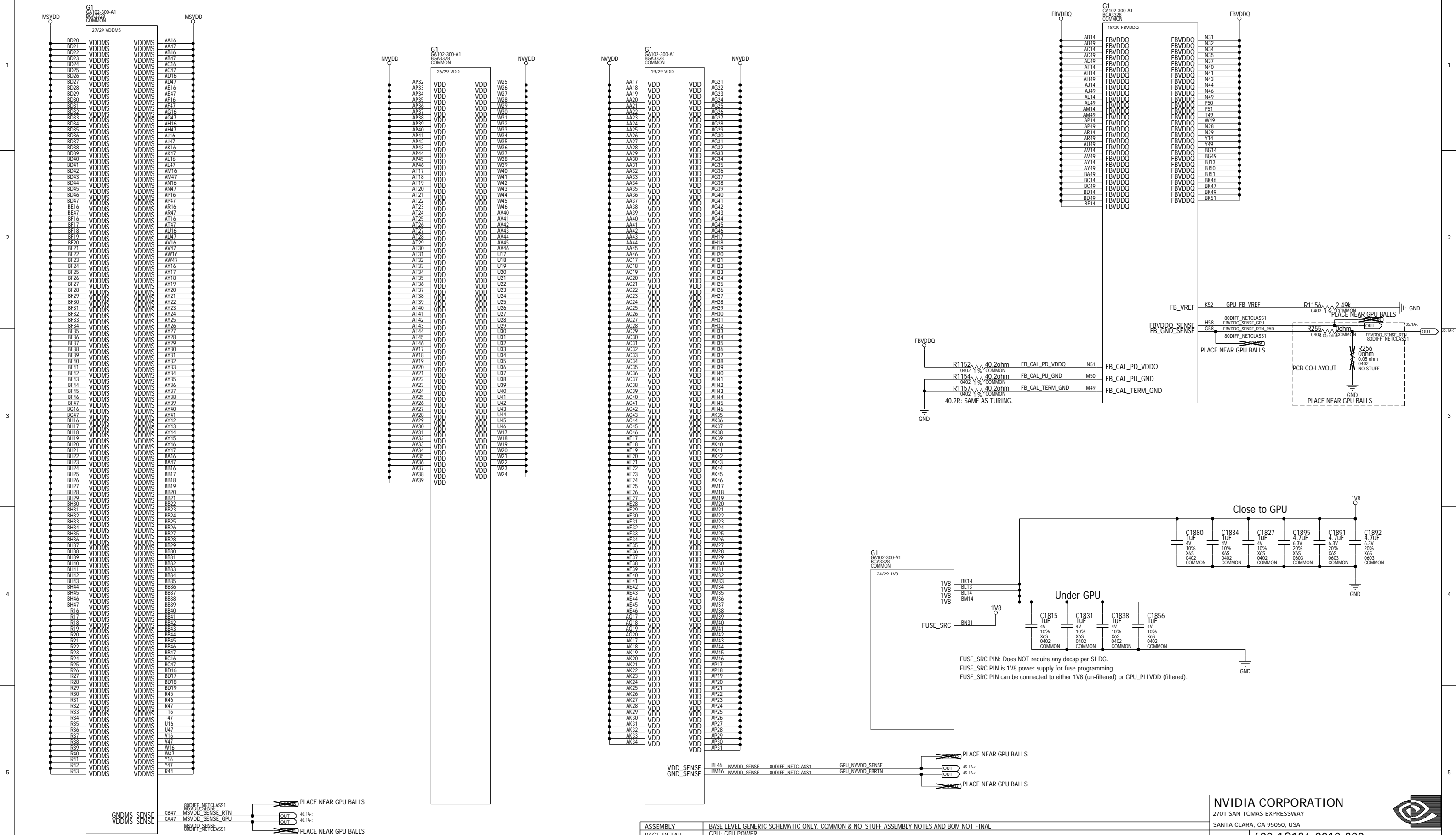
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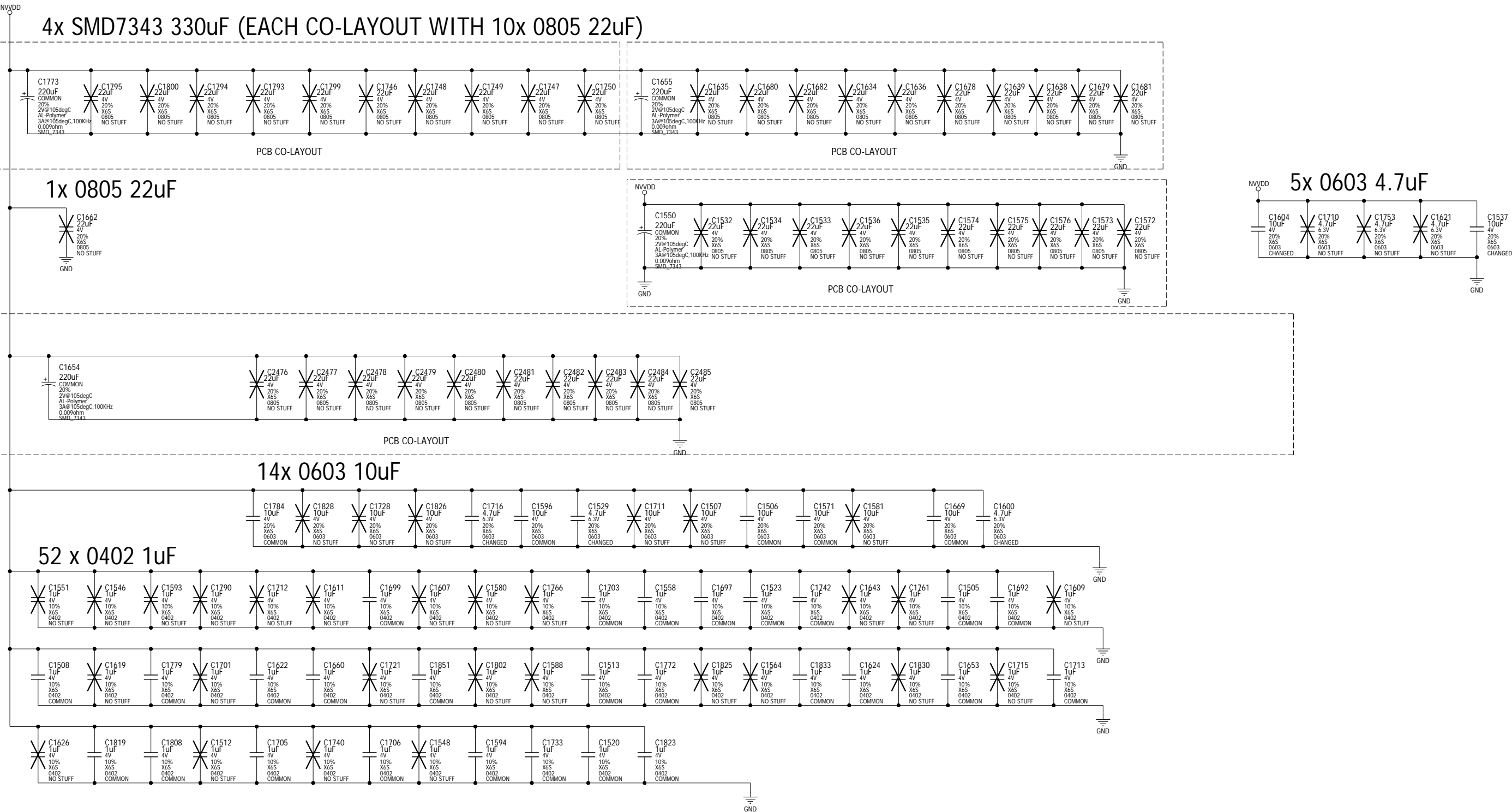
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PAGE DETAIL	GPU: GND, NC



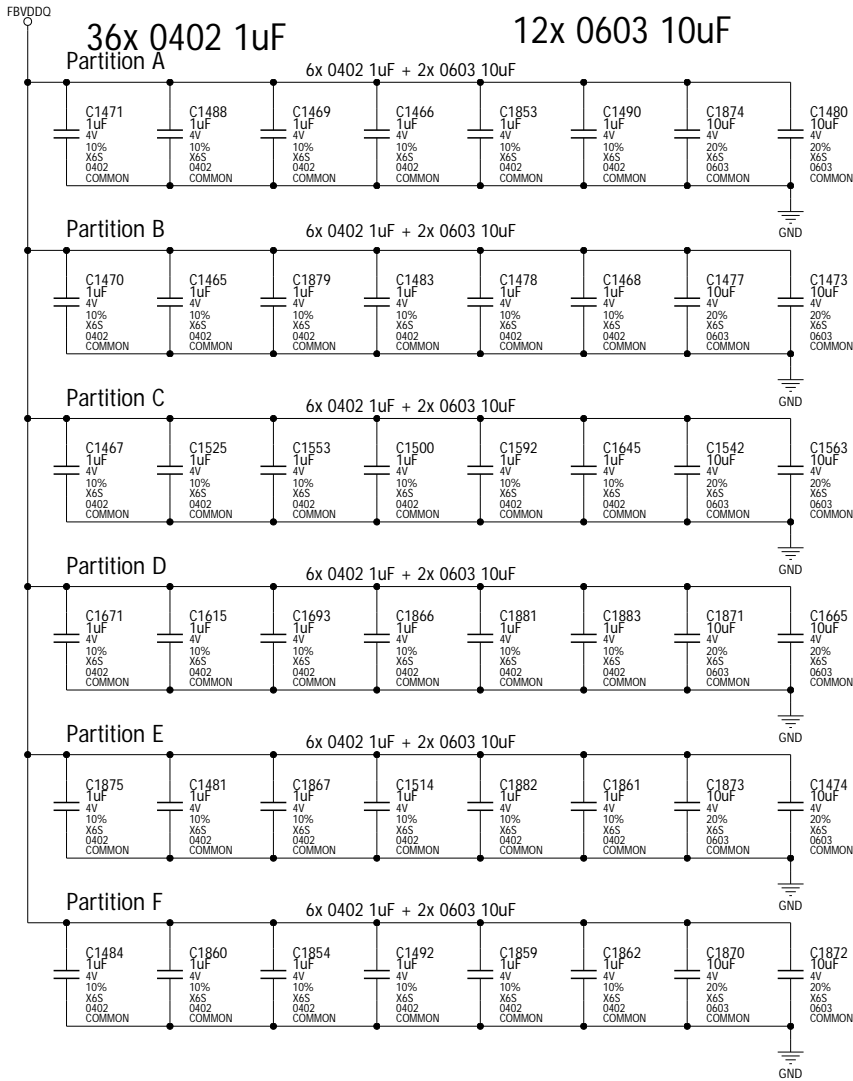
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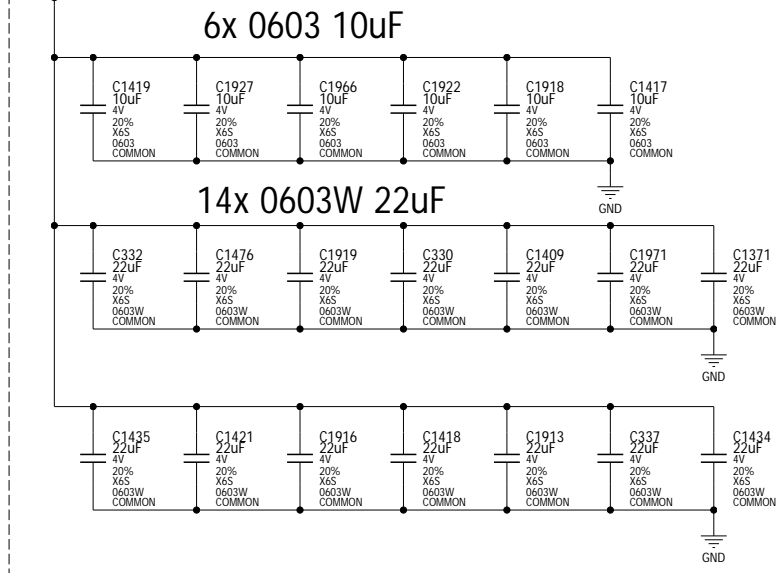
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FBVDDQ

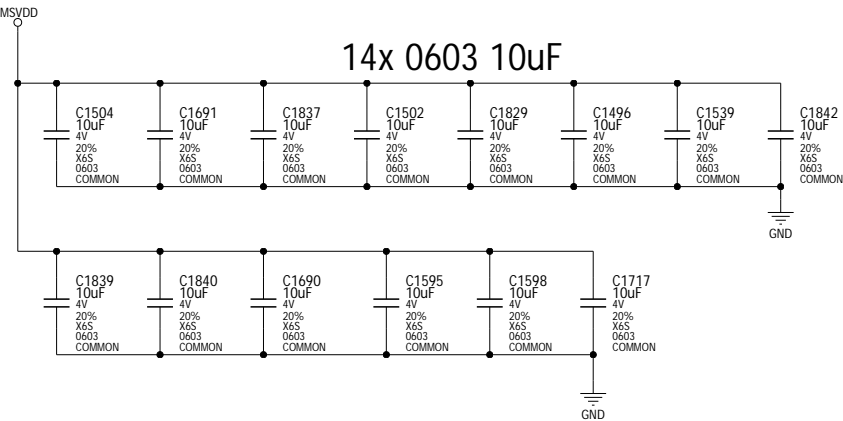
Under GPU



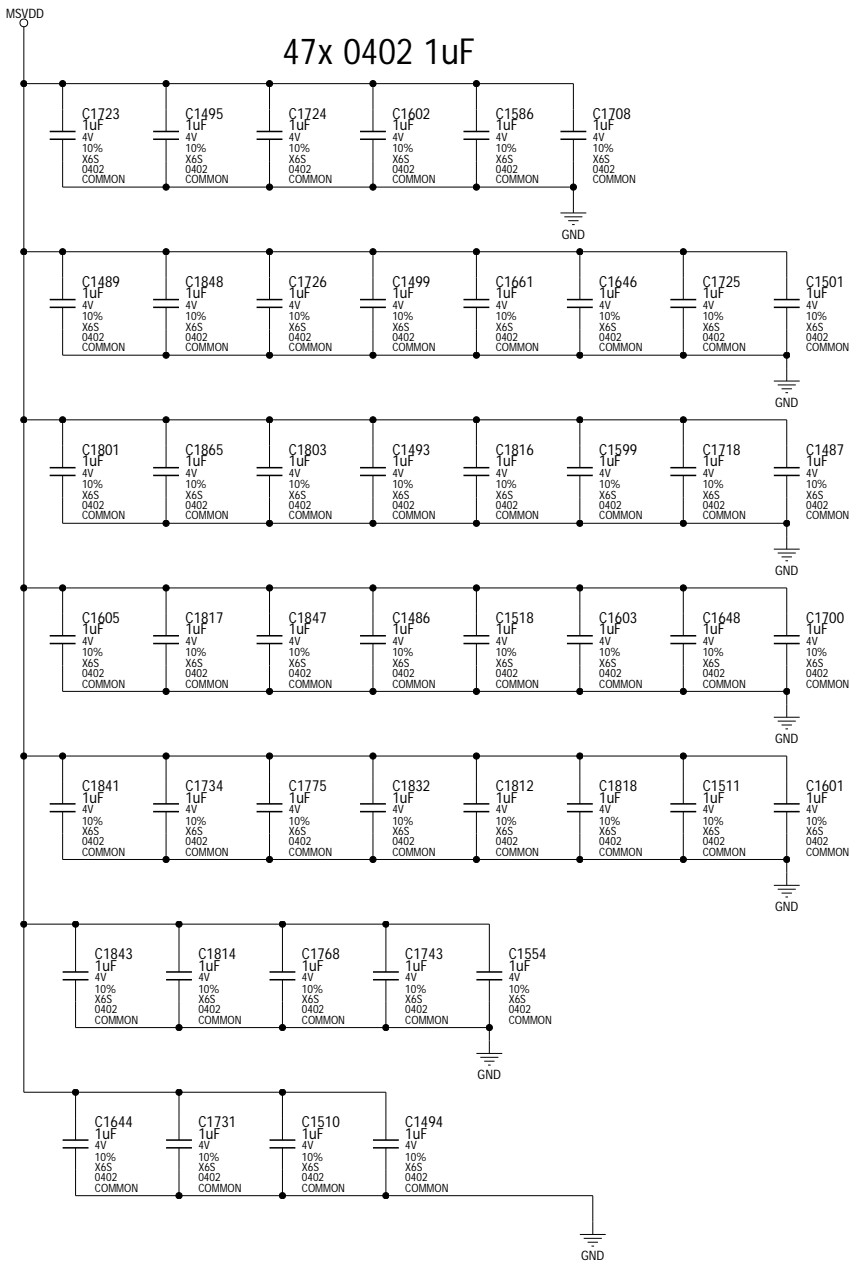
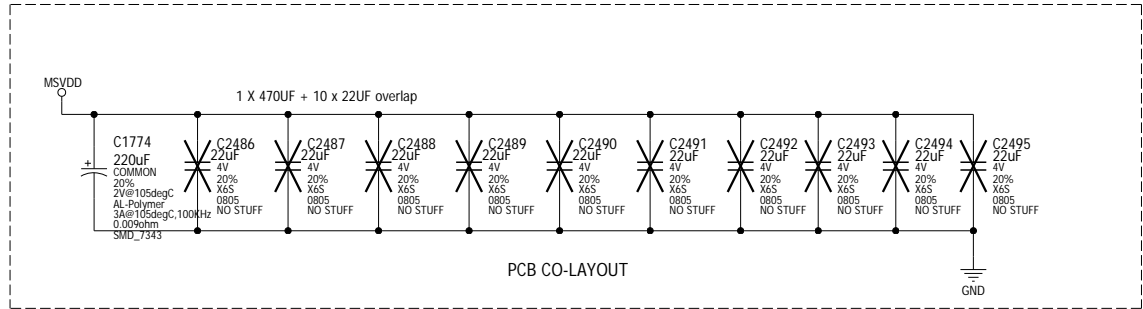
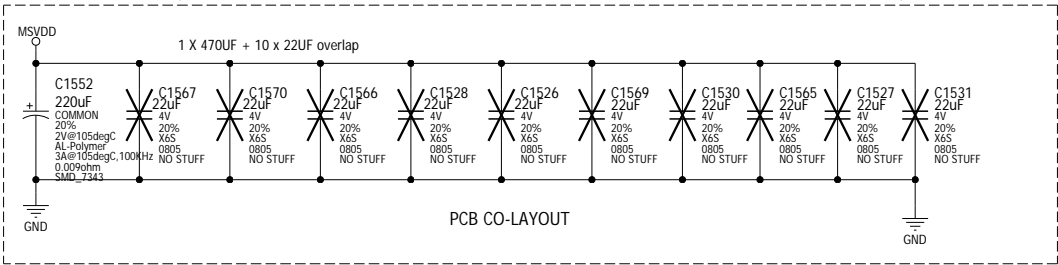
Close to GPU



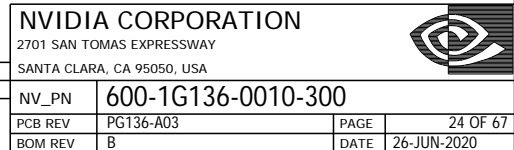
# UNDER GPU



2x SMD7343 330uF (EACH CO-LAYOUT WITH 10x 22uF 0805)

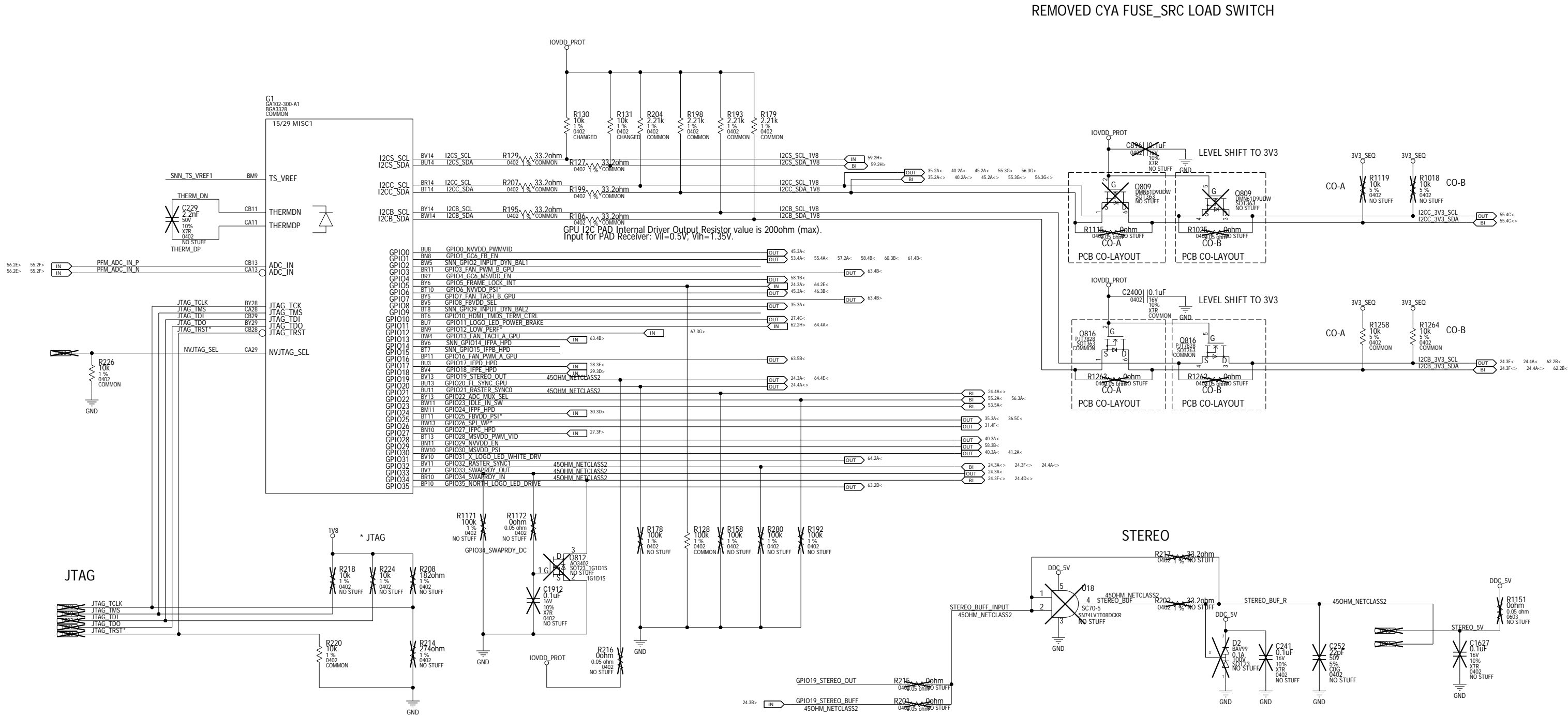


REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION



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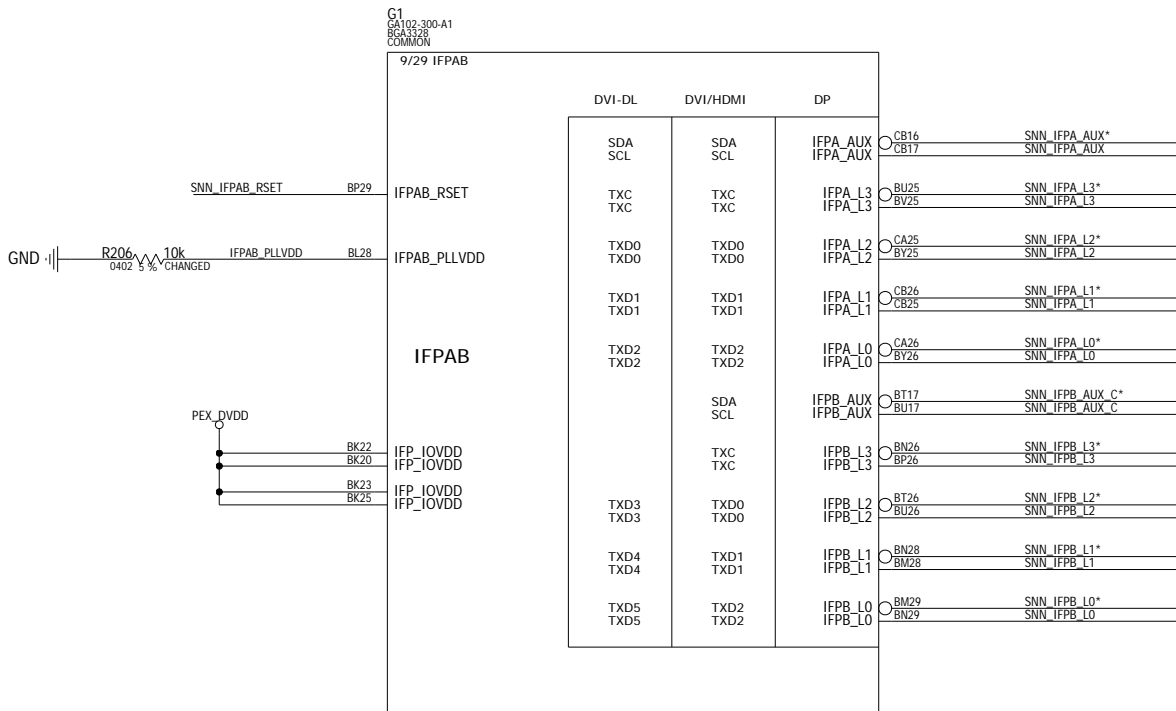
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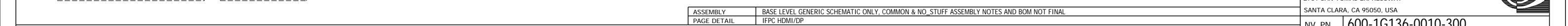
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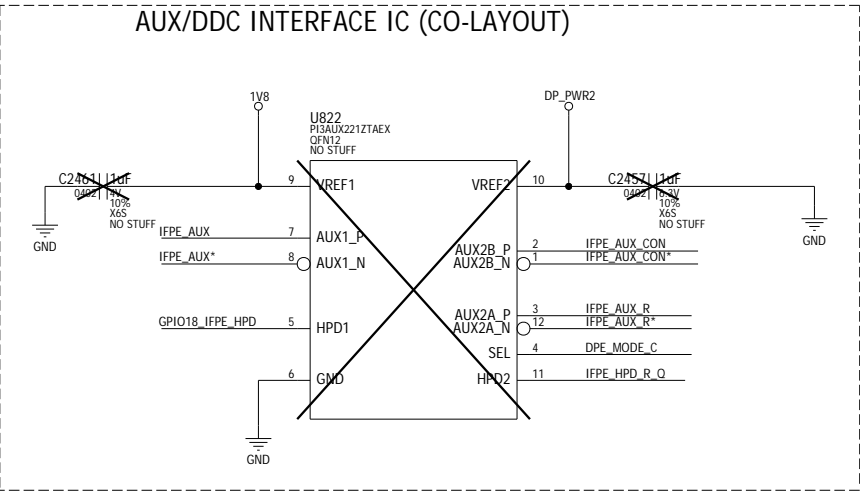
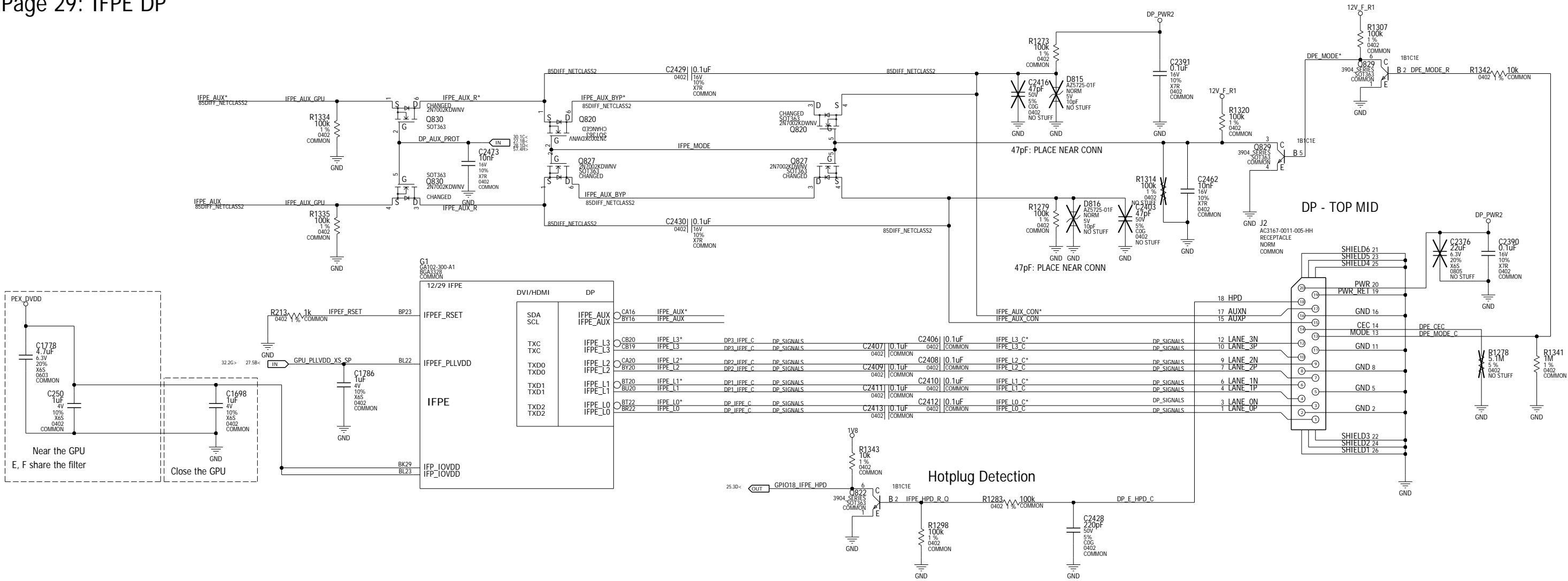


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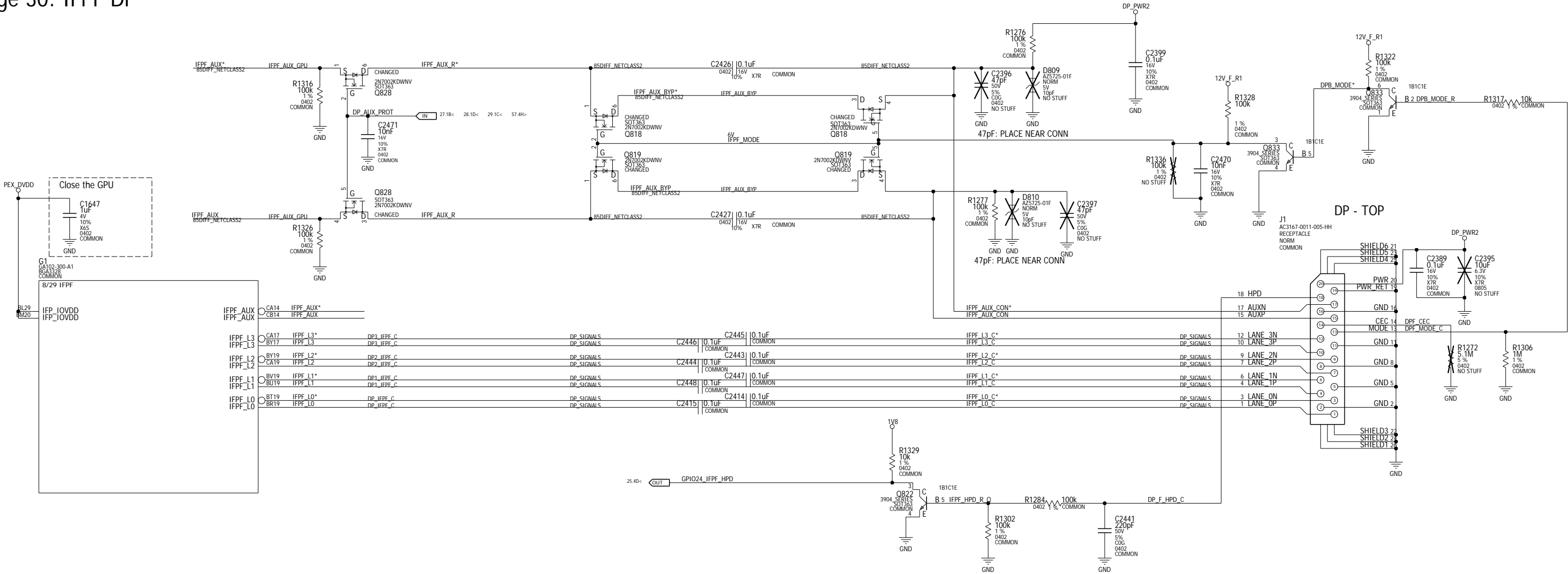
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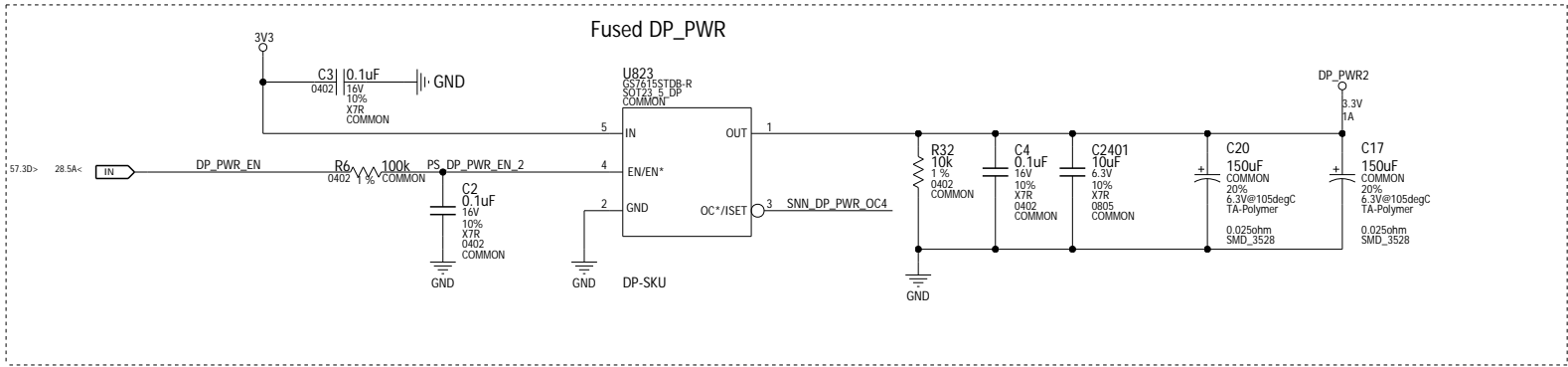
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4

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Fused DP\_PWR



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PAGE DETAIL	IFPF DP

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Page 31: MISC: ROM, Straps

GROUP0

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	H	00001
L	H	L	00010
L	H	H	00011
L	H	M	01101
H	H	H	00111

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

DEFAULT

GROUP1

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	M	L	1001	FAN0/1=33%33%, FS_OVERT ENABLE

<-DEFAULT

GROUP2

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

Default

SKU 200

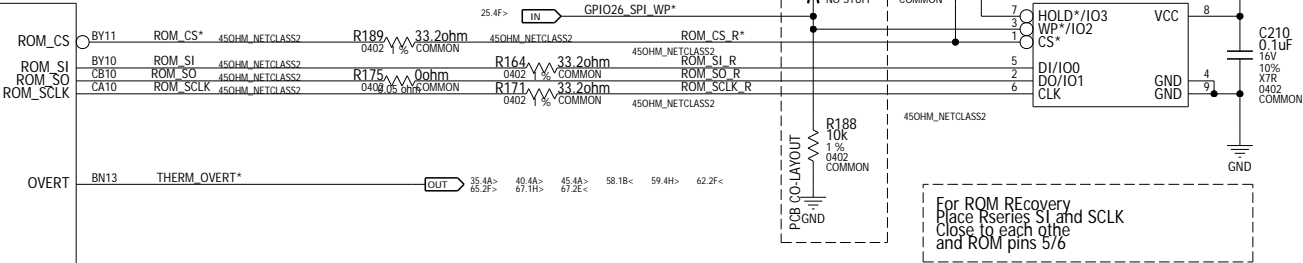
STRAP0	CA7	STRAP0
STRAP1	CB7	STRAP1
STRAP2	BW8	STRAP2
STRAP3	BW7	STRAP3
STRAP4	BY7	STRAP4
STRAP5	BV8	STRAP4

G1  
GA103-300-A1  
BGA328  
COMMON

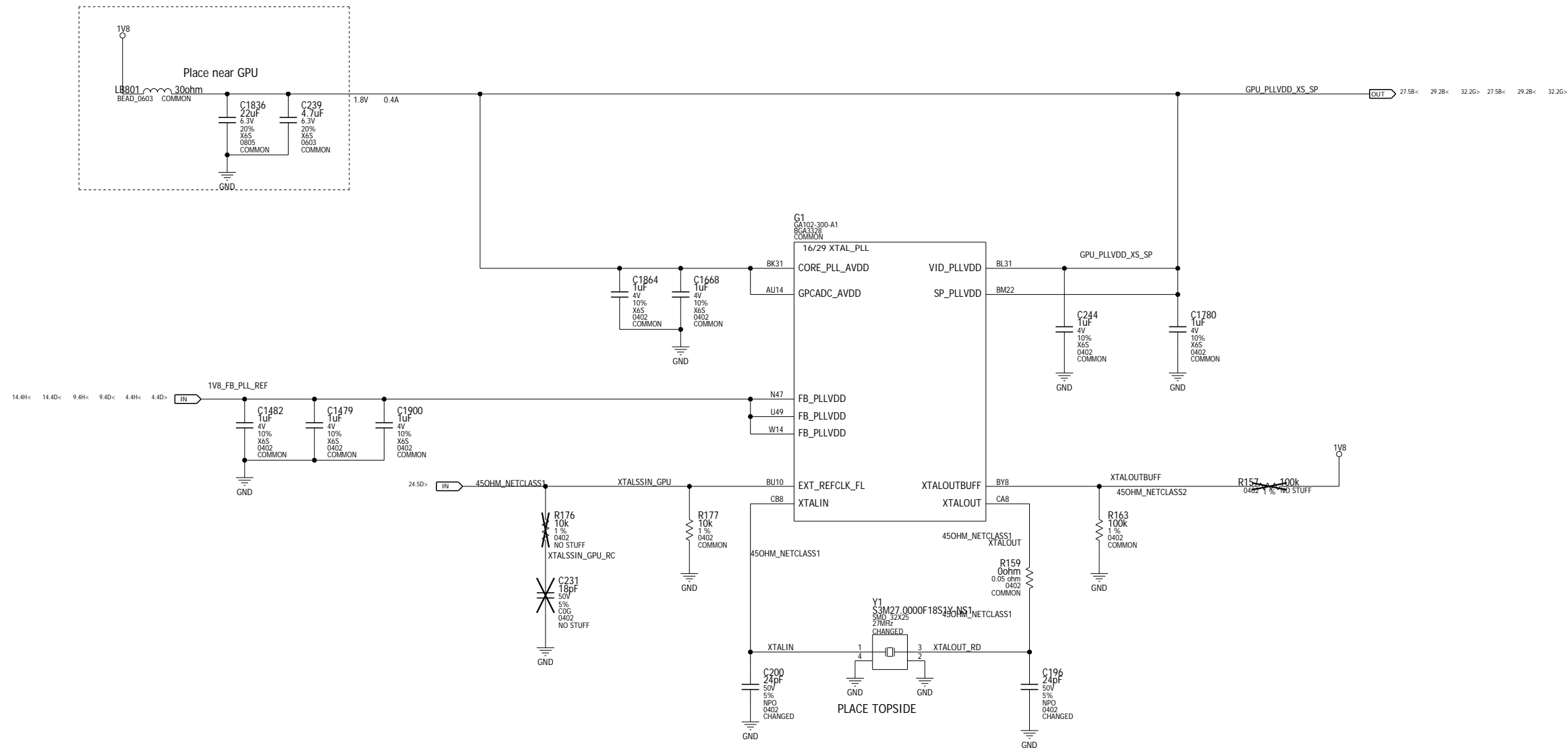
17/29 MISC2

ROM\_CS  
ROM\_SI  
ROM\_SO  
ROM\_SCLK

OVERT



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PAGE DETAIL	MISC. XTAL, PLL

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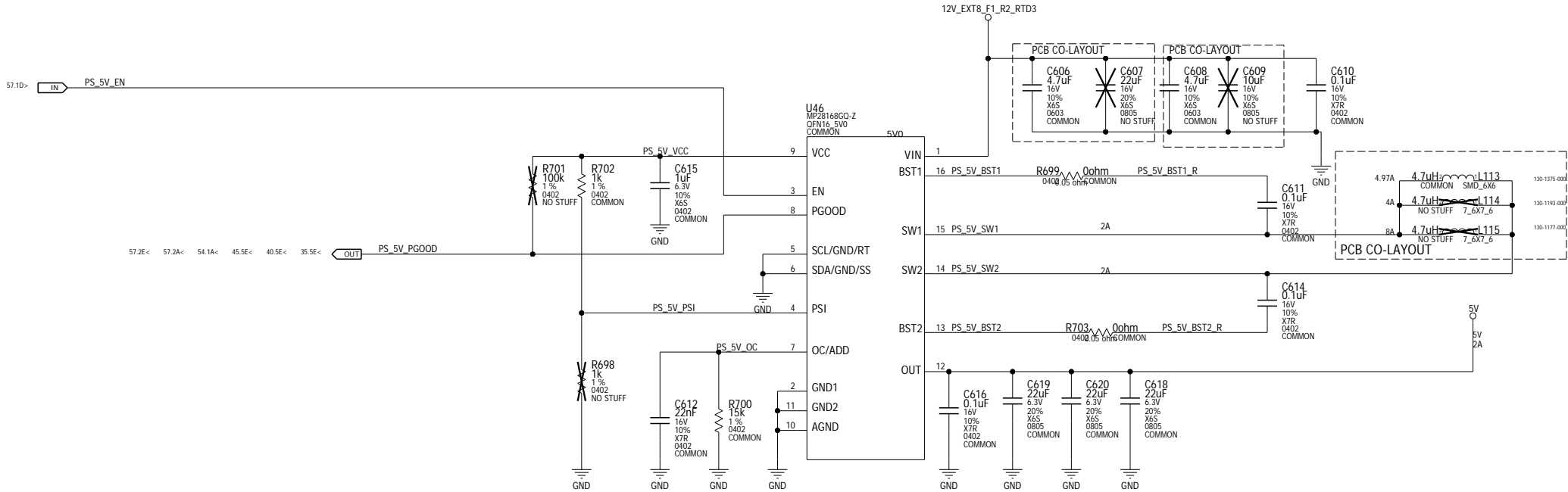
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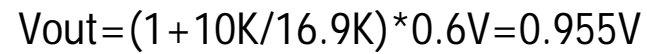
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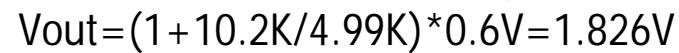





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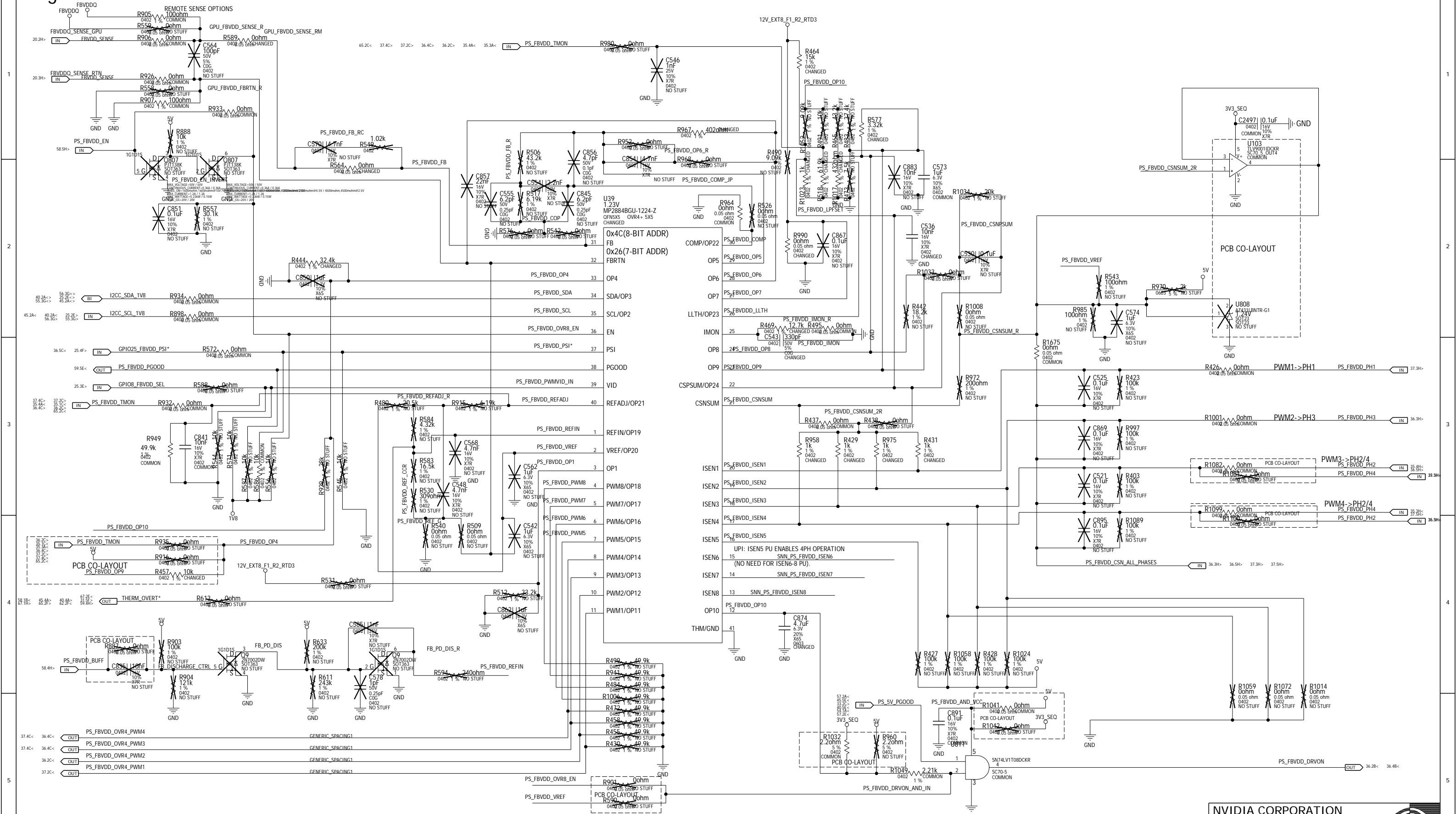
1V8



<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
<b>NV_PN</b> PCB REV BOM REV	<b>600-1G136-0010-300</b> PG136-A03 B	<b>PAGE</b> <b>DATE</b>	<b>34 OF 67</b> <b>26-JUN-2020</b>

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## Page 35: PS: FBVDD Controller



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

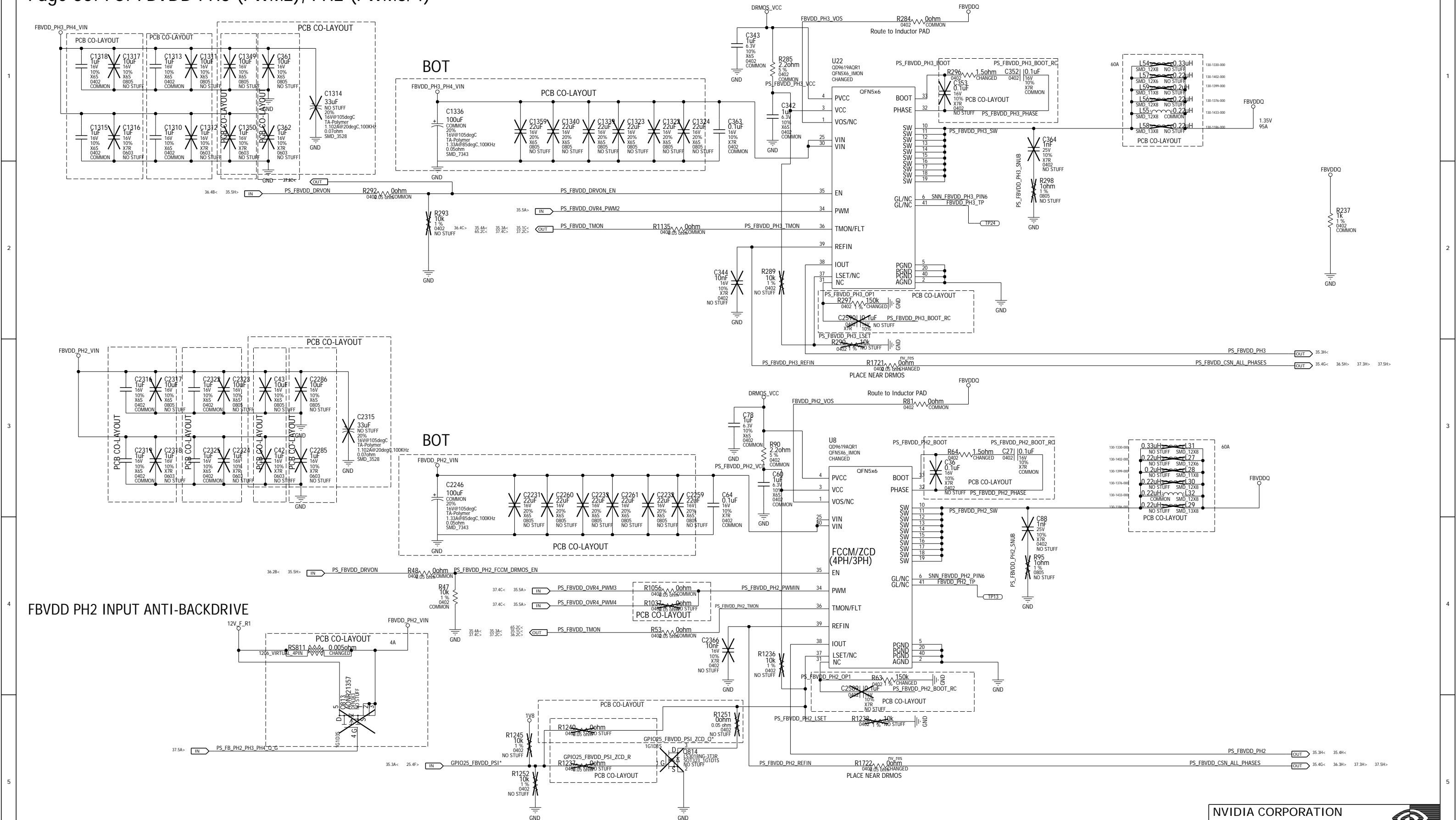
SANTA CLARA, CA 95050, USA

NV_PN	600-1G136-0010-300
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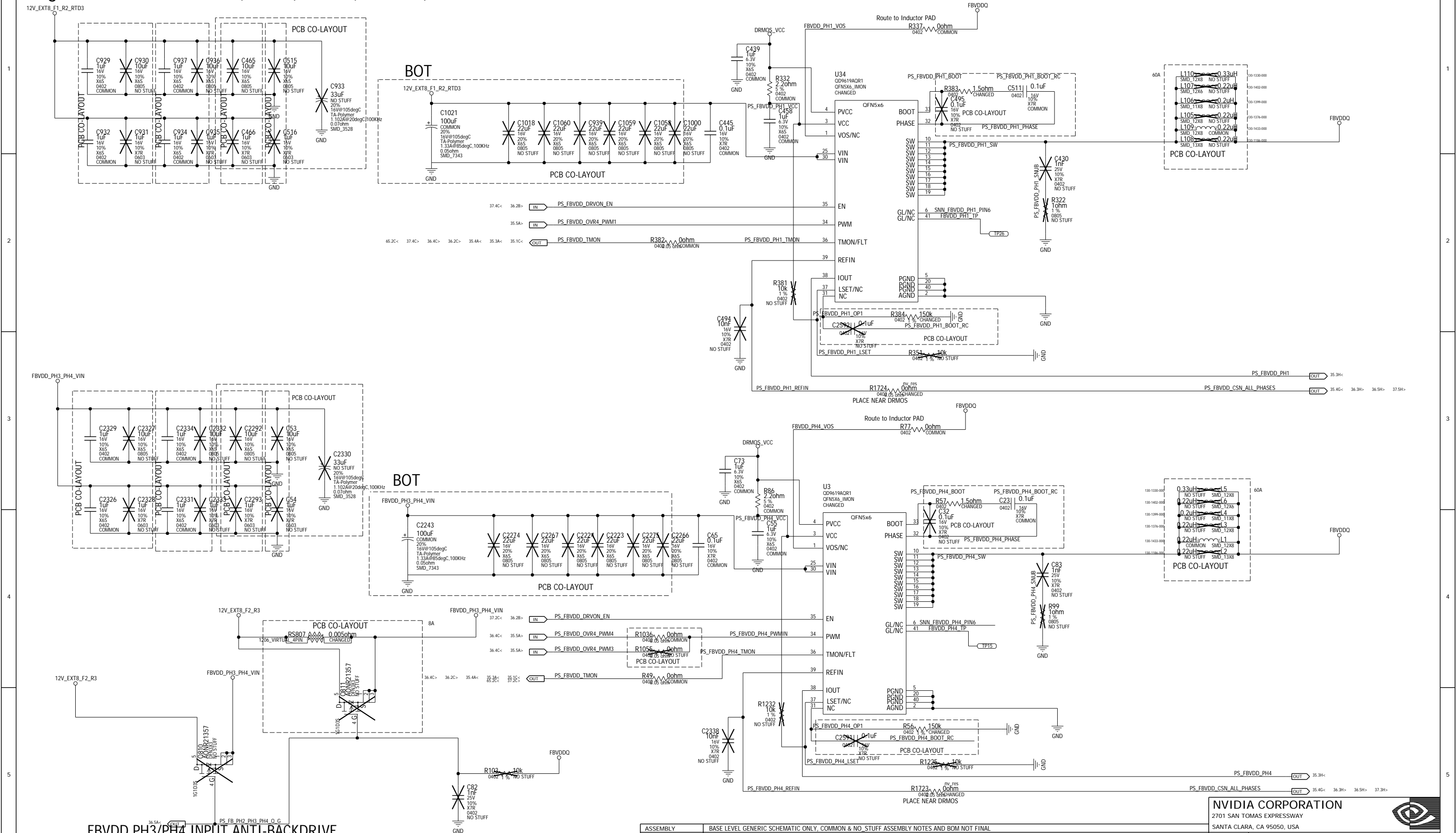
PCB REV	PG136-A03	PAGE	35 OF 67
BOM REV	B	DATE	26-JUN-2020

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: FBVDD CONTROLLER OVR4I



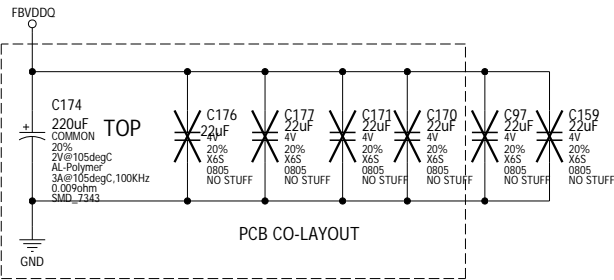
## Page 37: PS: FBVDD PH1 (PWM1), PH4 (PWM3/4)



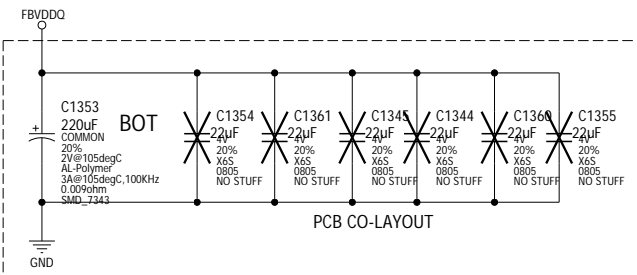
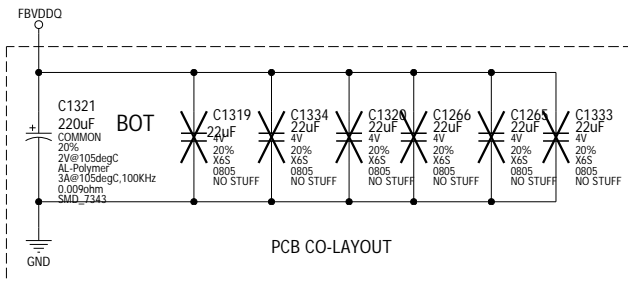
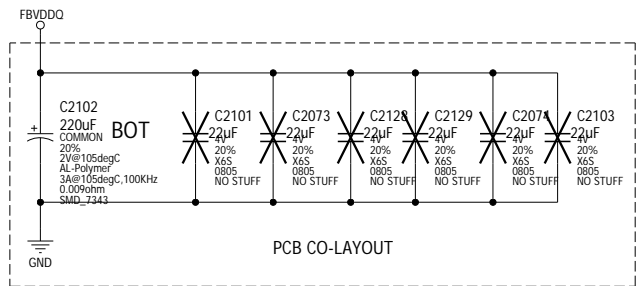
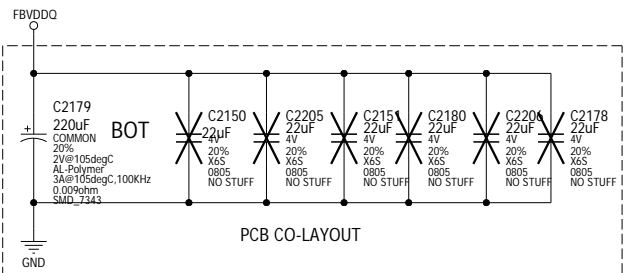
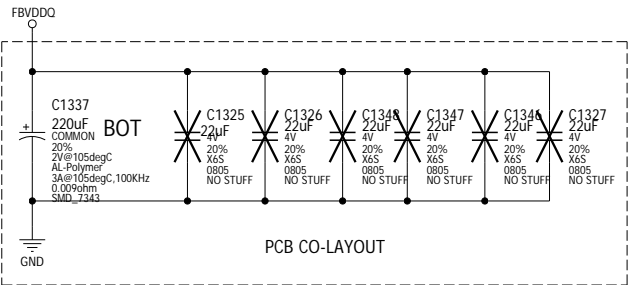
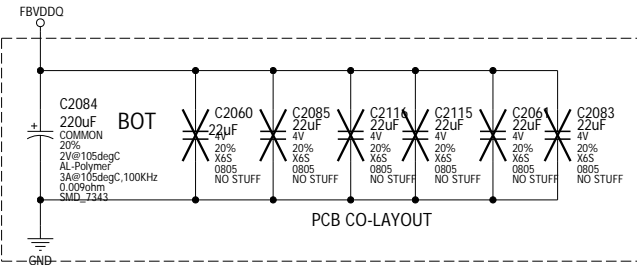
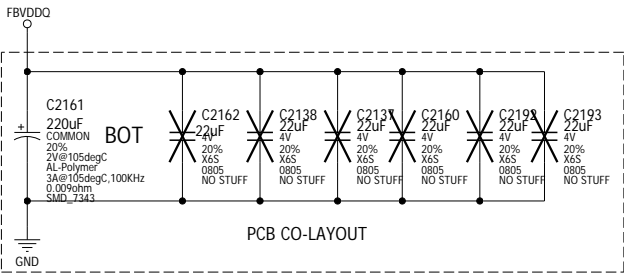
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL	SANTA CLARA, CA 95050, USA			
PAGE DETAIL	PS: FBVDD PH1 (PWM1 ) and PH4 (PWM3/4 )	NV_PN	600-1G136-0010-300		
MATERIALS) ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY PECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.		PCB REV	PG136-A03	PAGE	37 OF 67
		BOM REV	B	DATE	26-JUN-2020

PLACE NEAR POWER SUPPLY  
8x SMD7343 330uF CO-LAYOUT WITH 48x 0805 22uF



TOP WEST OF PCB

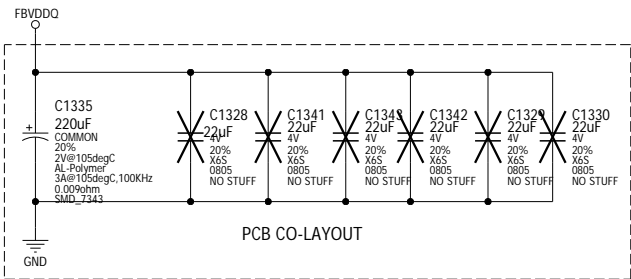
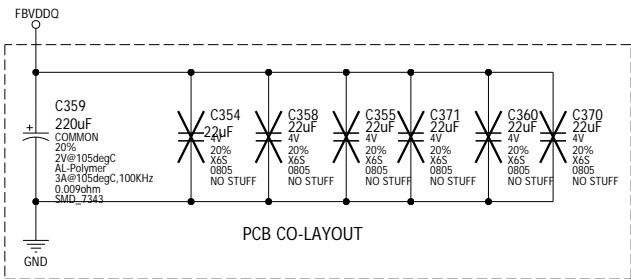
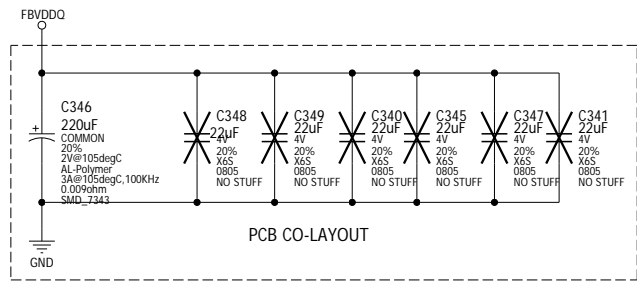
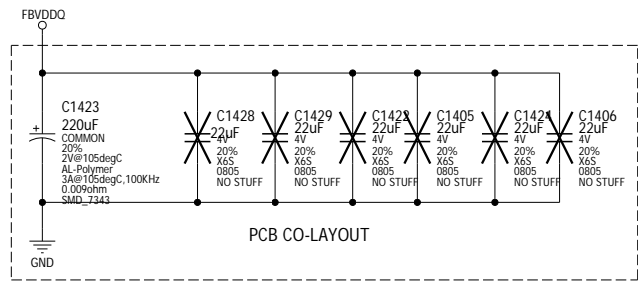
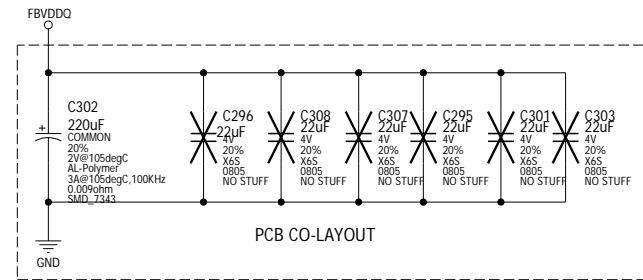
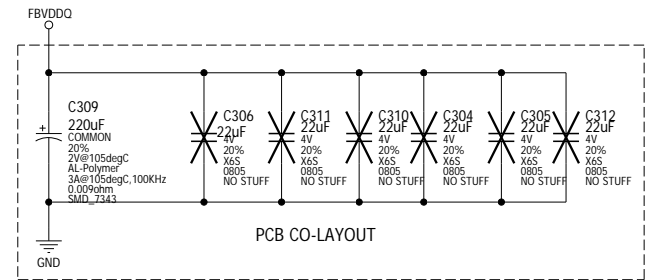
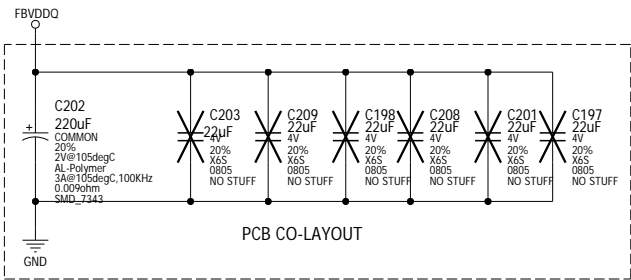
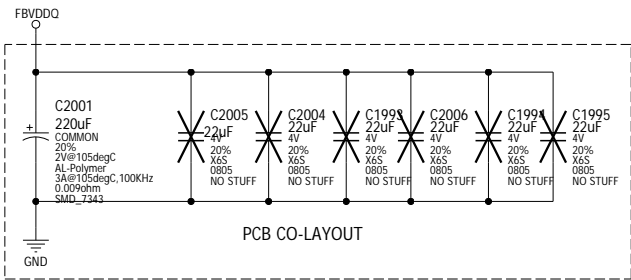


BACK EAST OF PCB

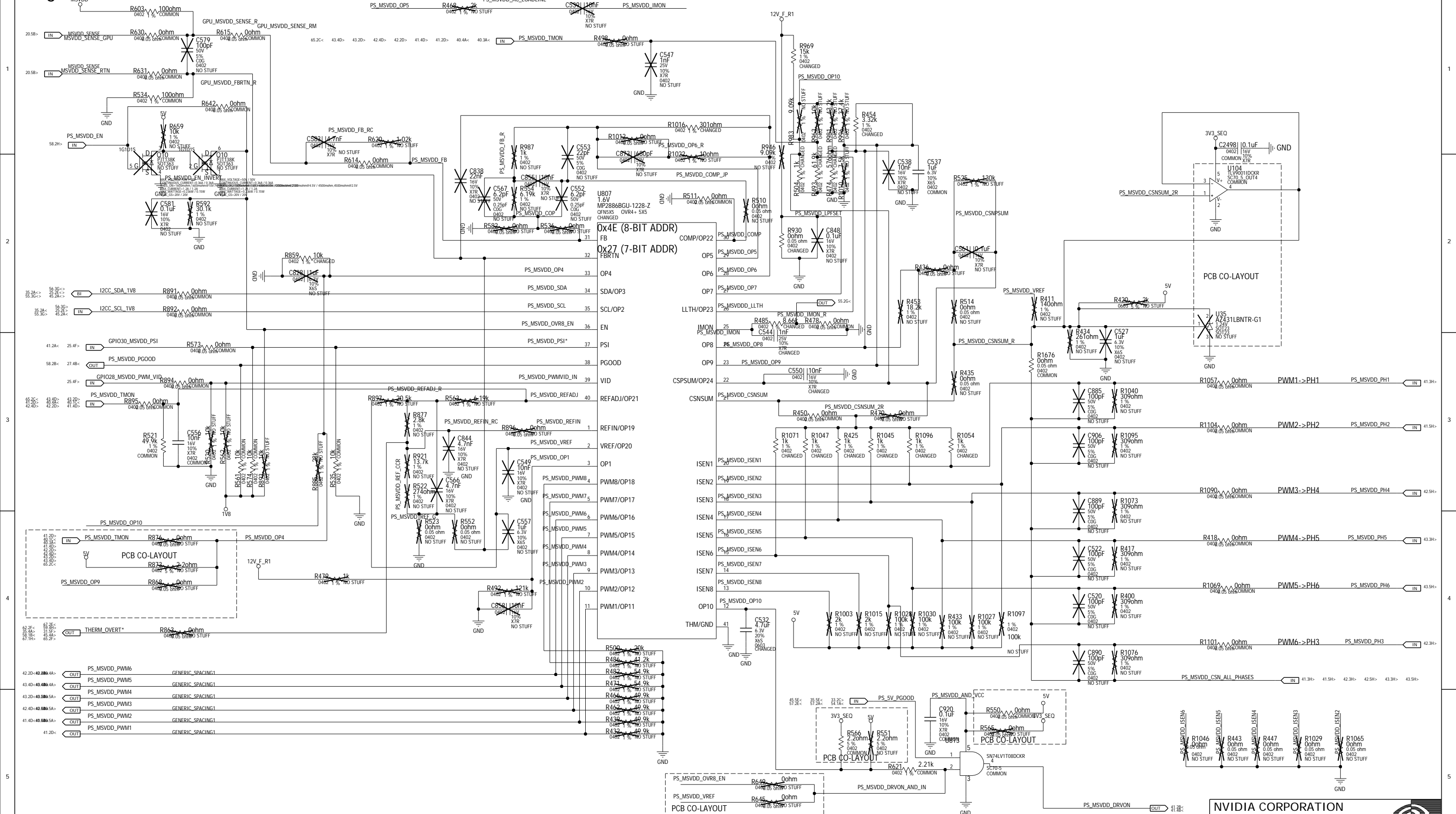
BACK WEST OF PCB

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PLACE NEAR MEMORY




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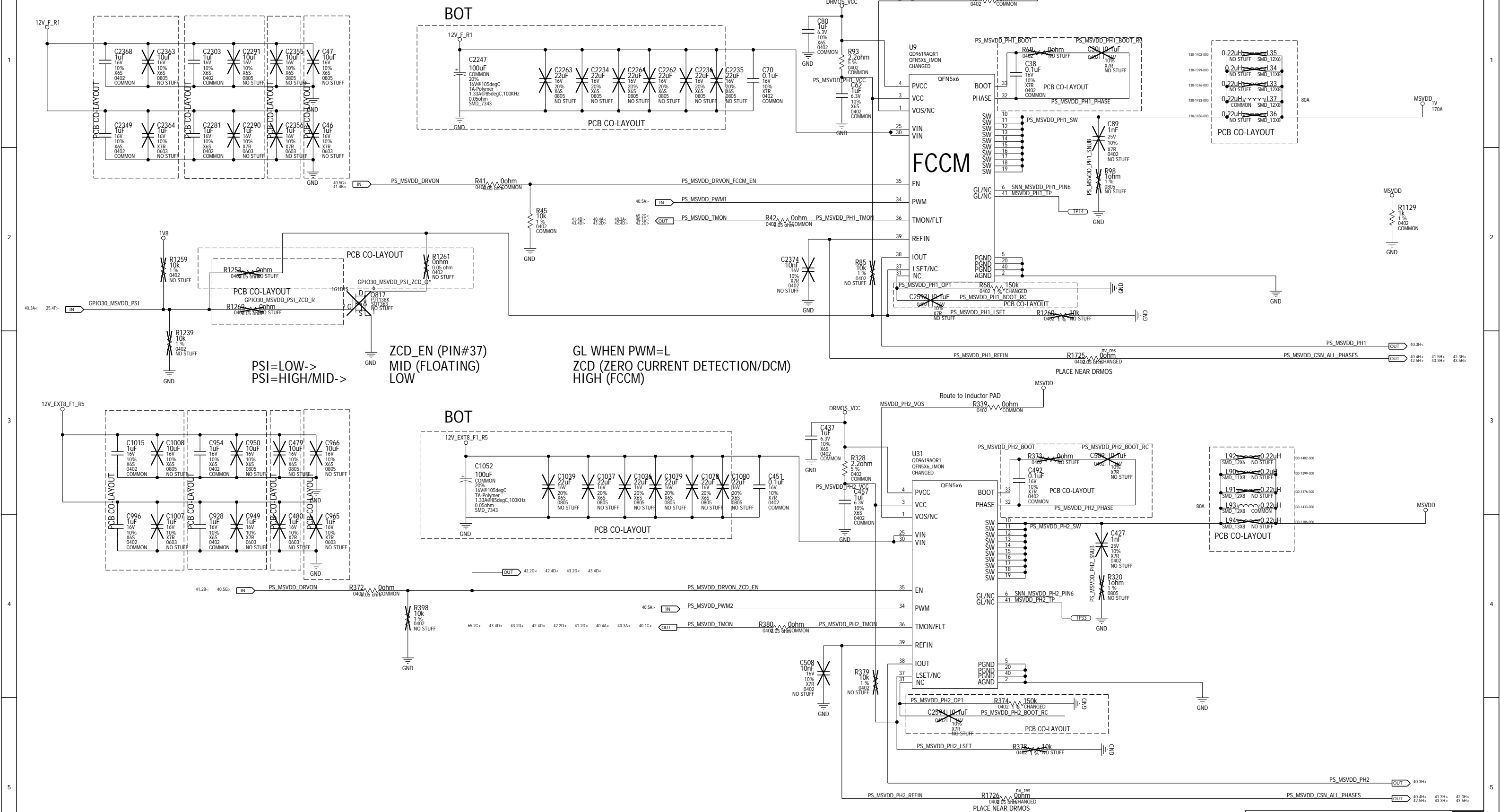


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: MSVDD CONTROLLER OVR4i

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<b>NV_PN</b> PCB REV BOM REV	<b>600-1G136-0010-300</b> PG136-A03 B		PAGE DATE 26-JUN-2020
		40 OF 67	



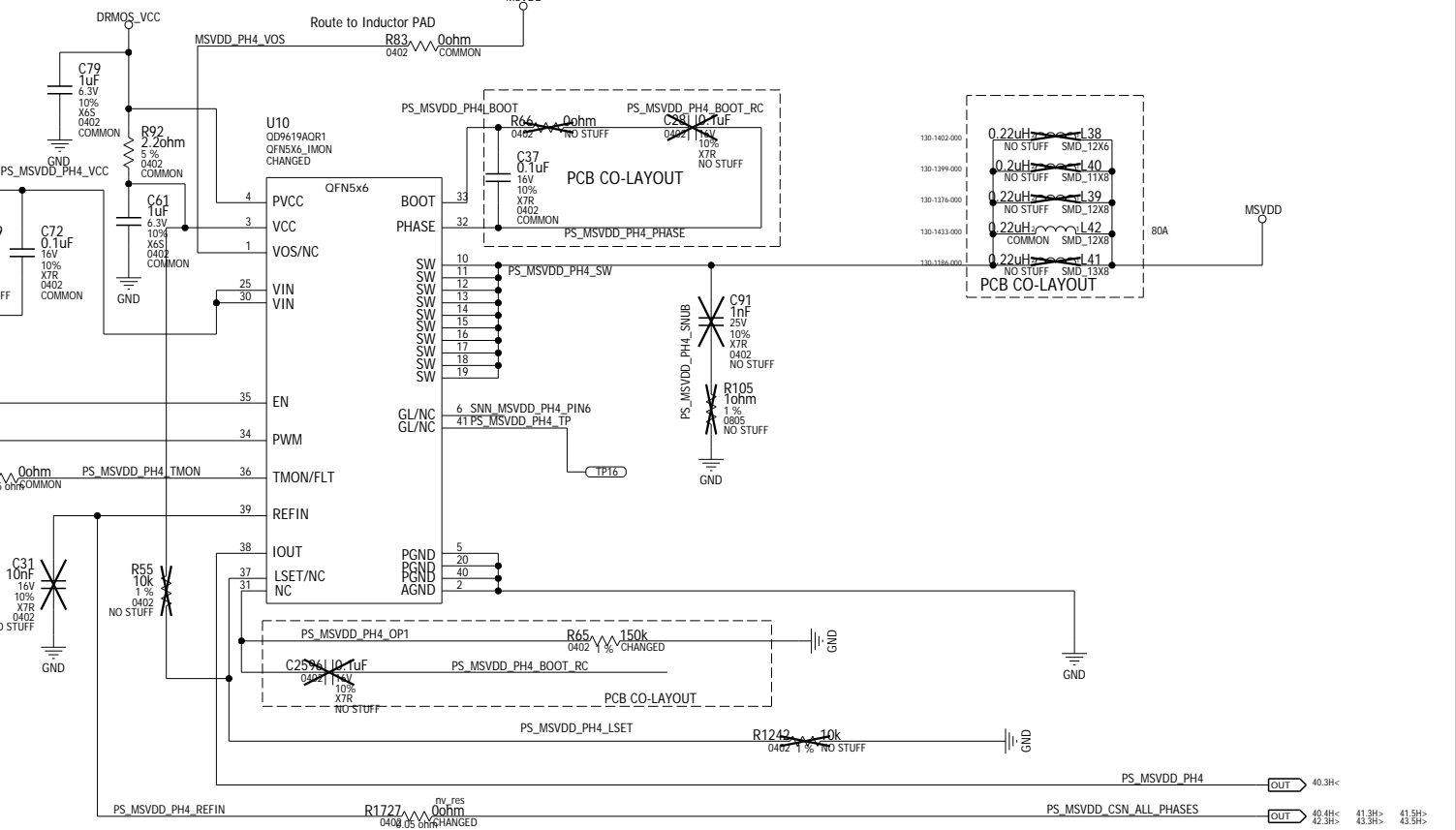
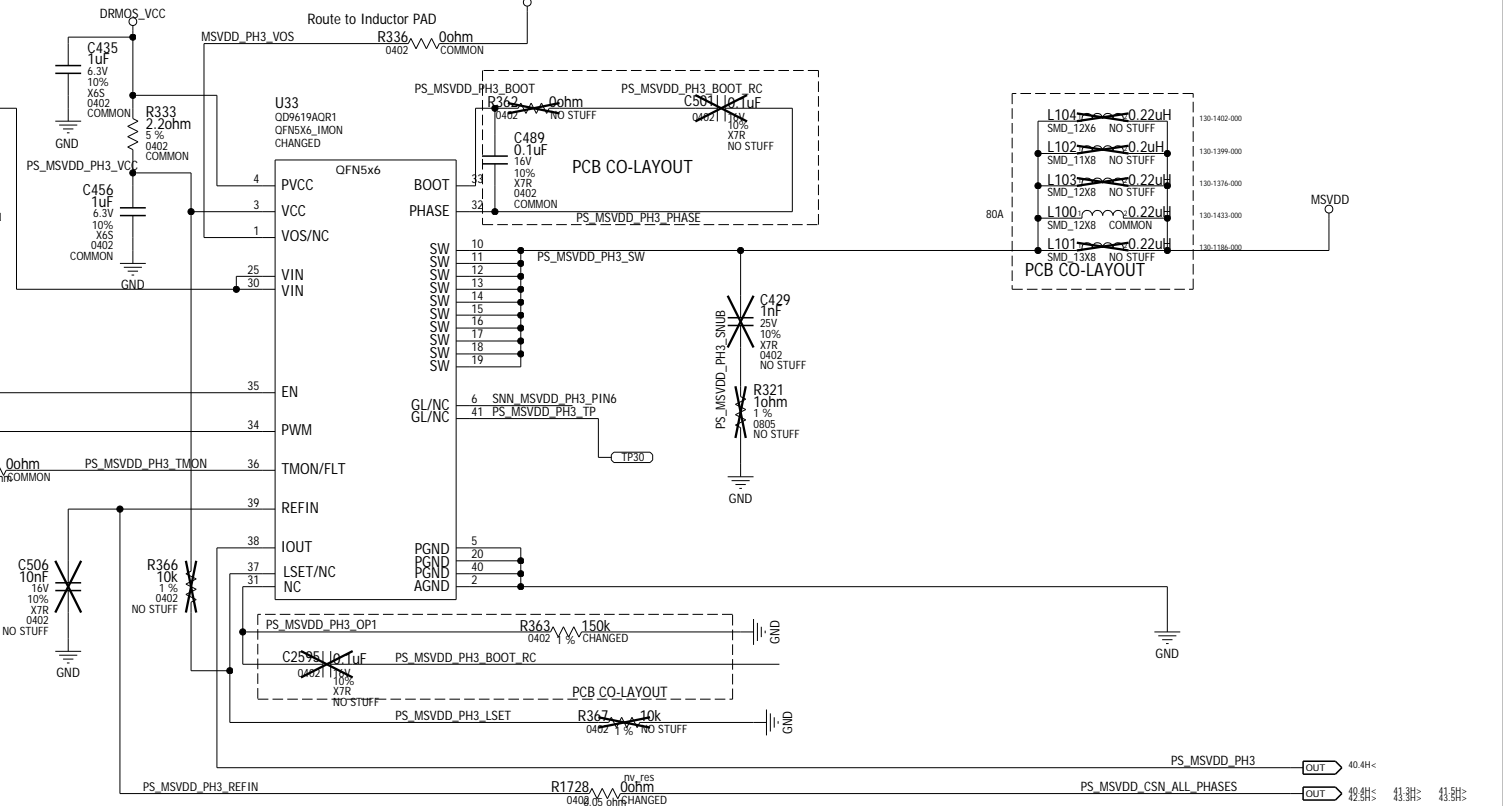
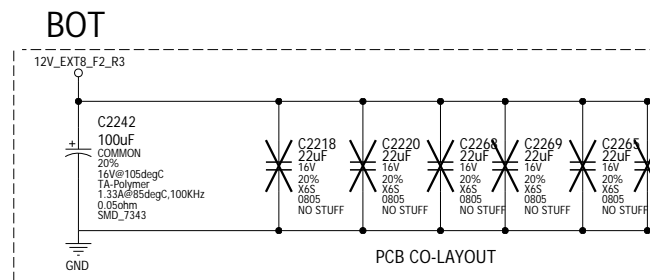
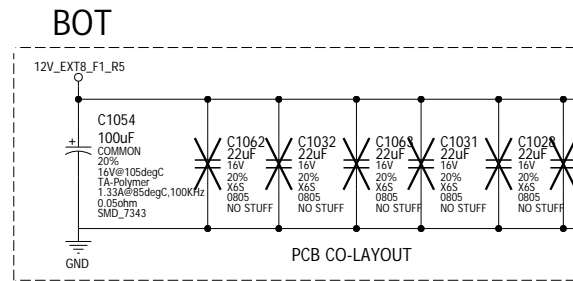
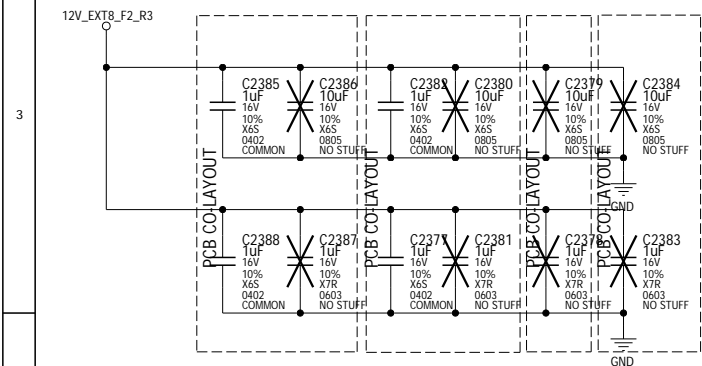
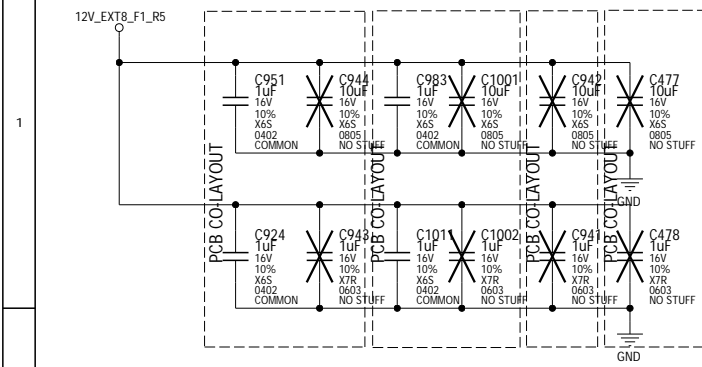


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: MSVDD PH1 (PWM1 ) and PH2 (PWM2 )

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<b>NV_PN</b>		<b>600-1G136-0010-300</b>	
<b>PCB REV</b>	<b>PG136-A03</b>	<b>PAGE</b>	<b>41 OF 67</b>
<b>BOM REV</b>	<b>B</b>	<b>DATE</b>	<b>26-JUN-2020</b>

## Page 42: PS: MSVDD PH3 (PWM6), PH4 (PWM3)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: MSVDD PH3 (PWM6 ) and PH4 (PWM3 )

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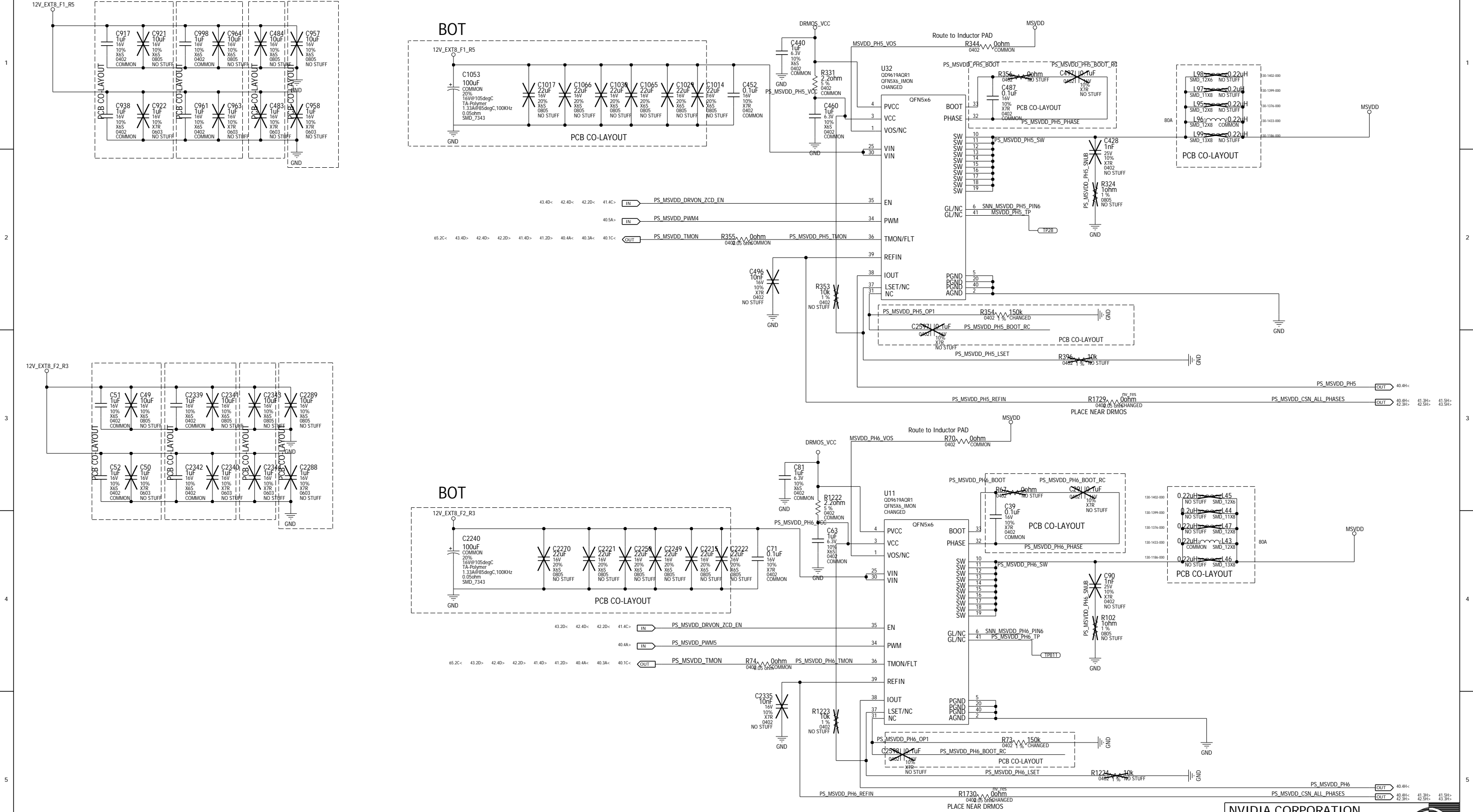
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NV PN	600-1G136-0010-300
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PCB REV	PG136-A03	PAGE	42 OF 67
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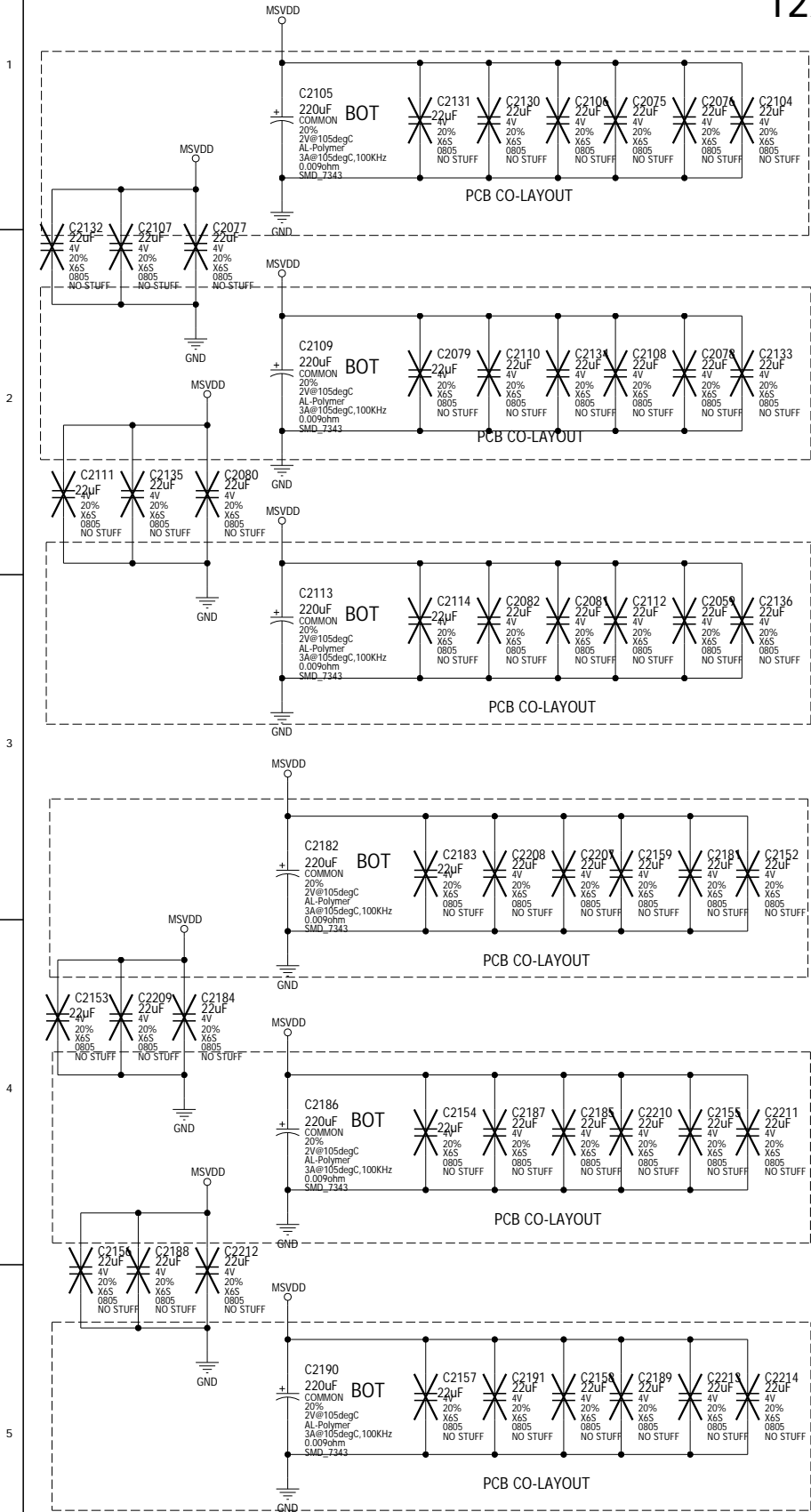
PCB REV	PG138-A03	PAGE	42 OF 67
BOM REV	B	DATE	26-JUN-2020

Page 43: PS:MSVDD PH 5 (PWM4), PH 6 (PWM5)

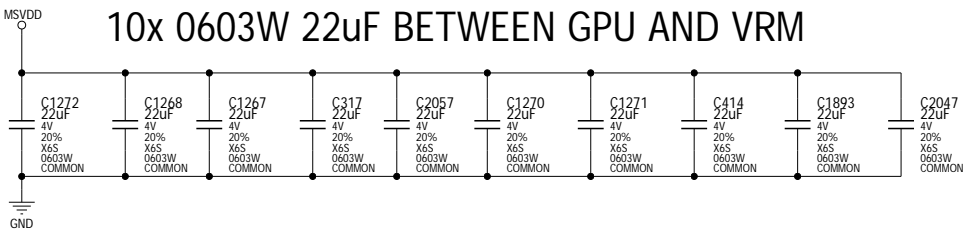


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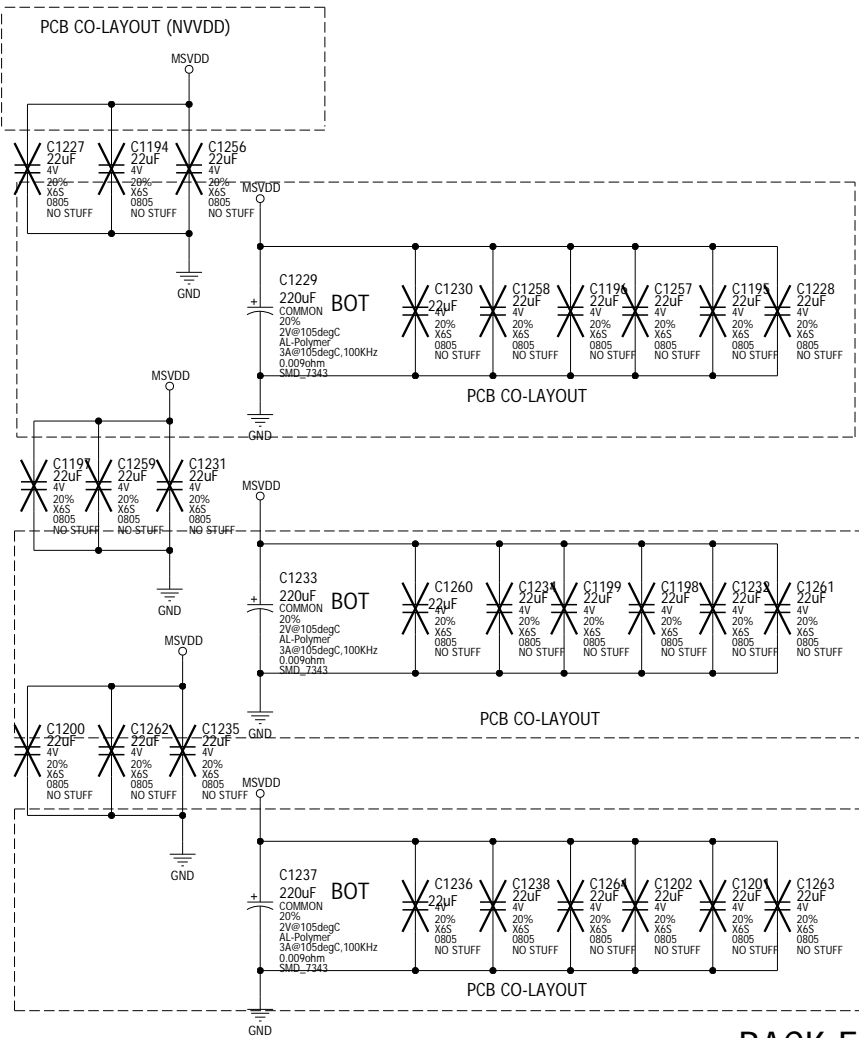
12x SMD7343 330uF CO-LAYOUT WITH 72x 0805 22uF



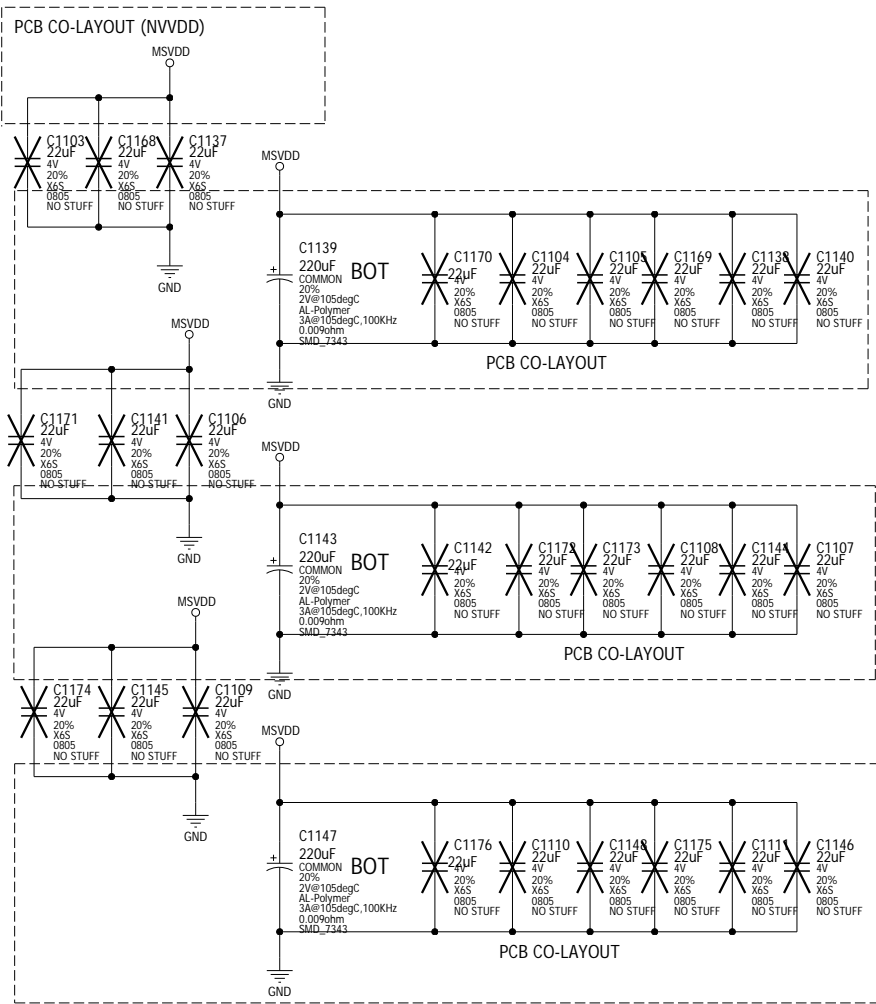
BACK WEST OF PCB



10x 0603W 22uF BETWEEN GPU AND VRM

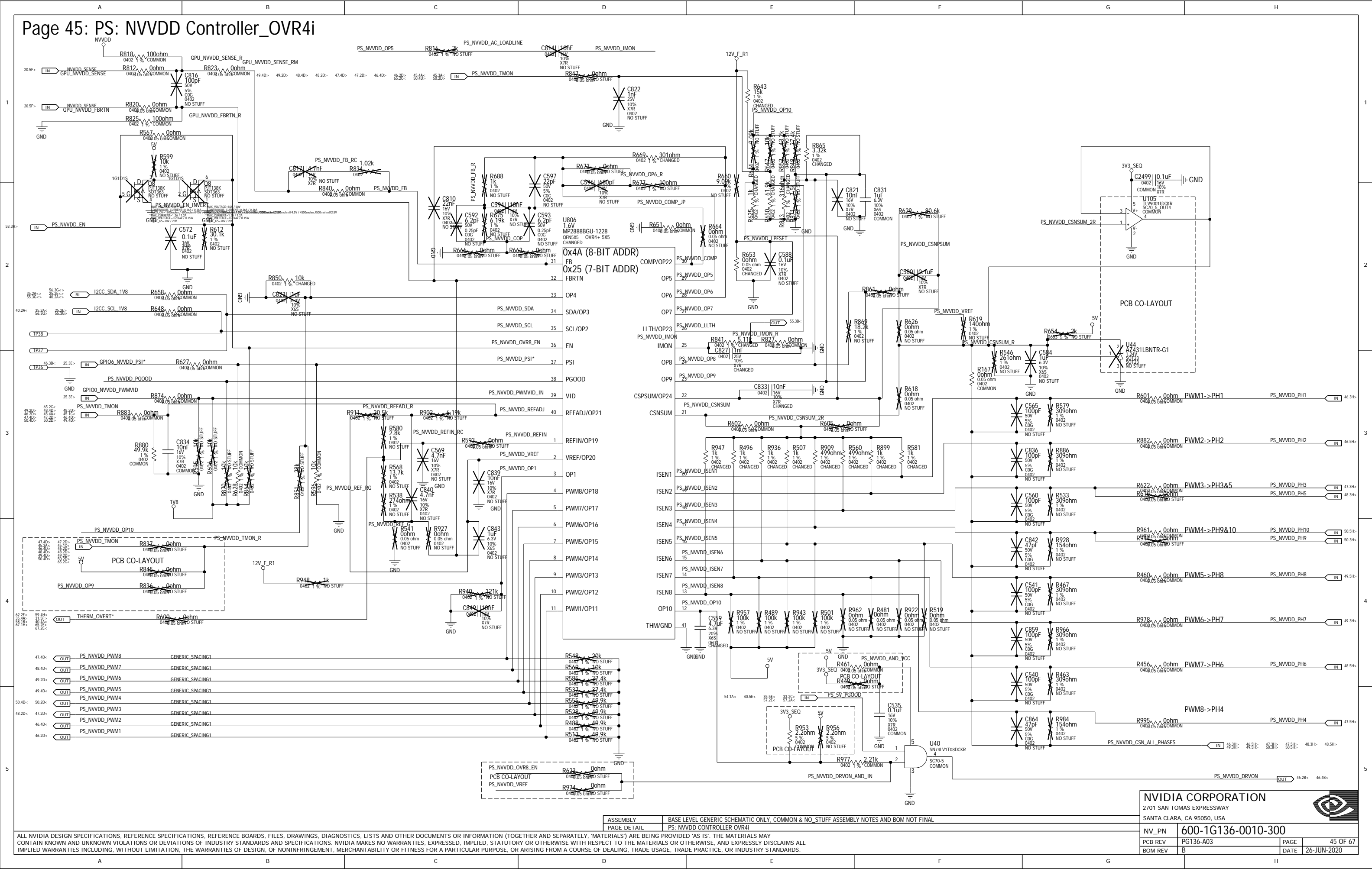


BACK EAST OF PCB



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD CONTROLLER_OVR4i

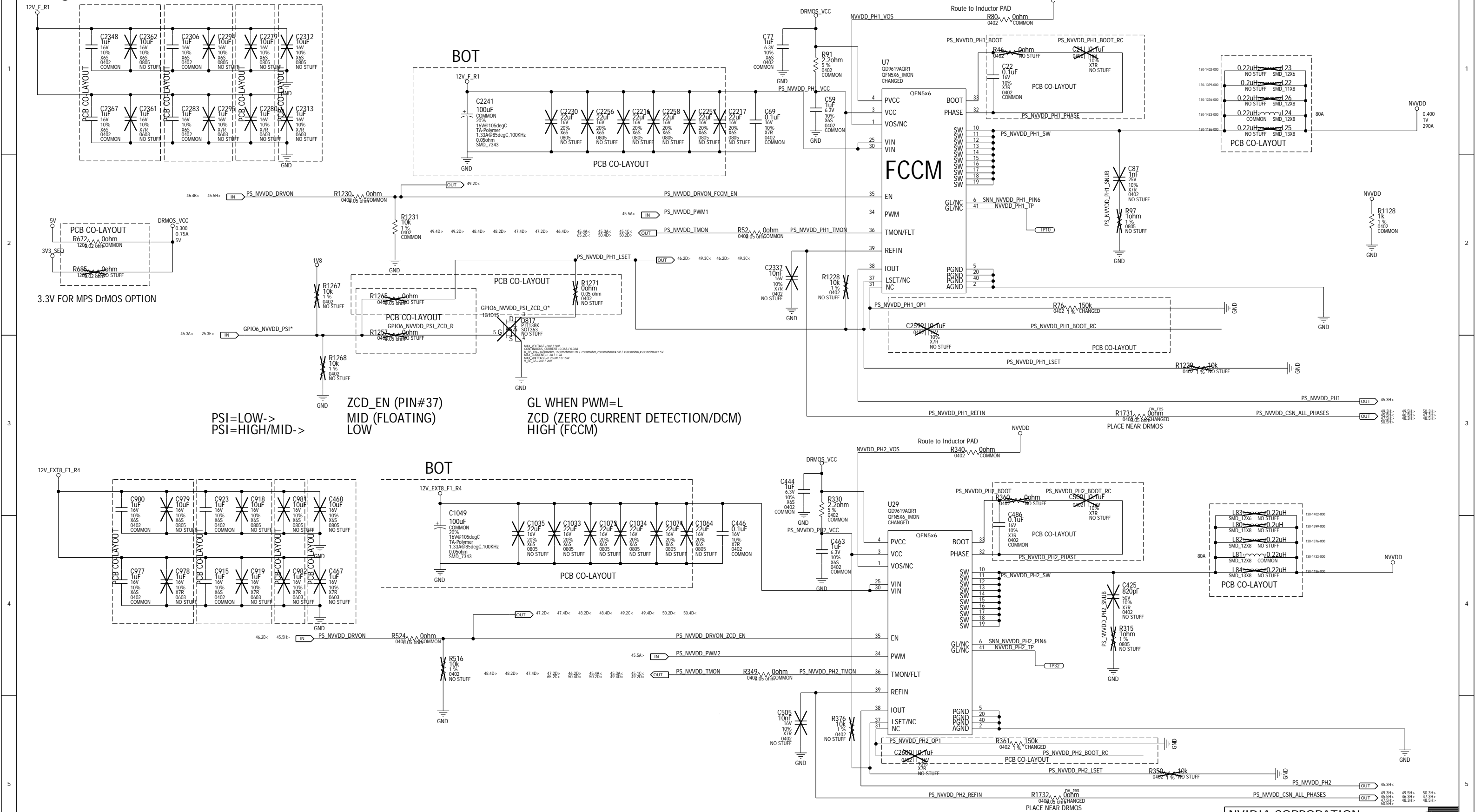
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NV_PN	600-1G136-0010-300
PCB REV	PG136-A03
BOM REV	B
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DATE	26-JUN-2020

## Page 46: PS: NVVDD PH 1 (PWM1), PH 2 (PWM2)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD PH1 (PWM1 ) and PH2 (PWM2 )

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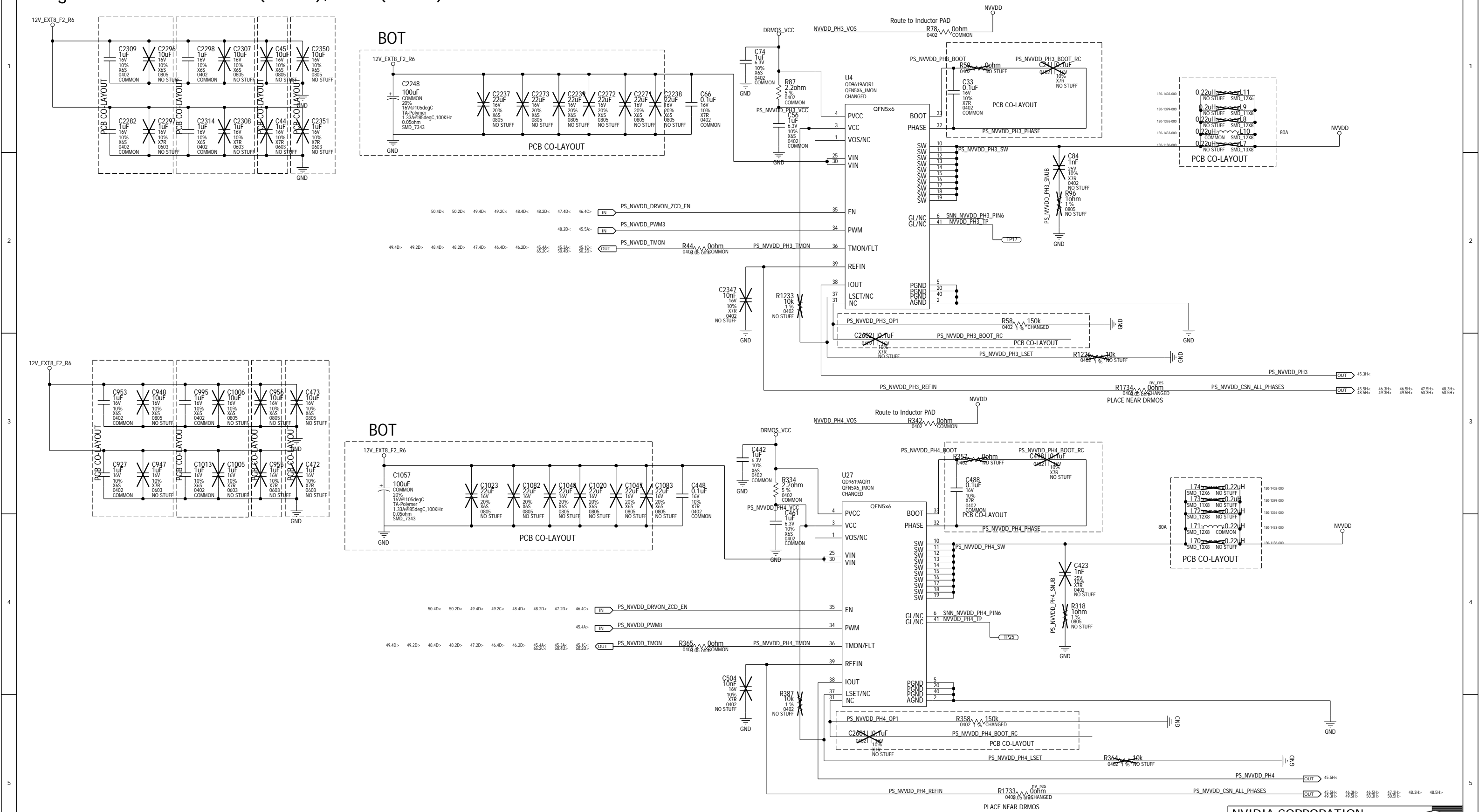
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SANTA CLARA, CA 95050, USA



NV_PN	600-1G136-0010-300
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## Page 47: PS: NVVDD PH 3 (PWM3), PH 4 (PWM8)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD PH3 (PWM3 ) and PH4 (PWM8 )

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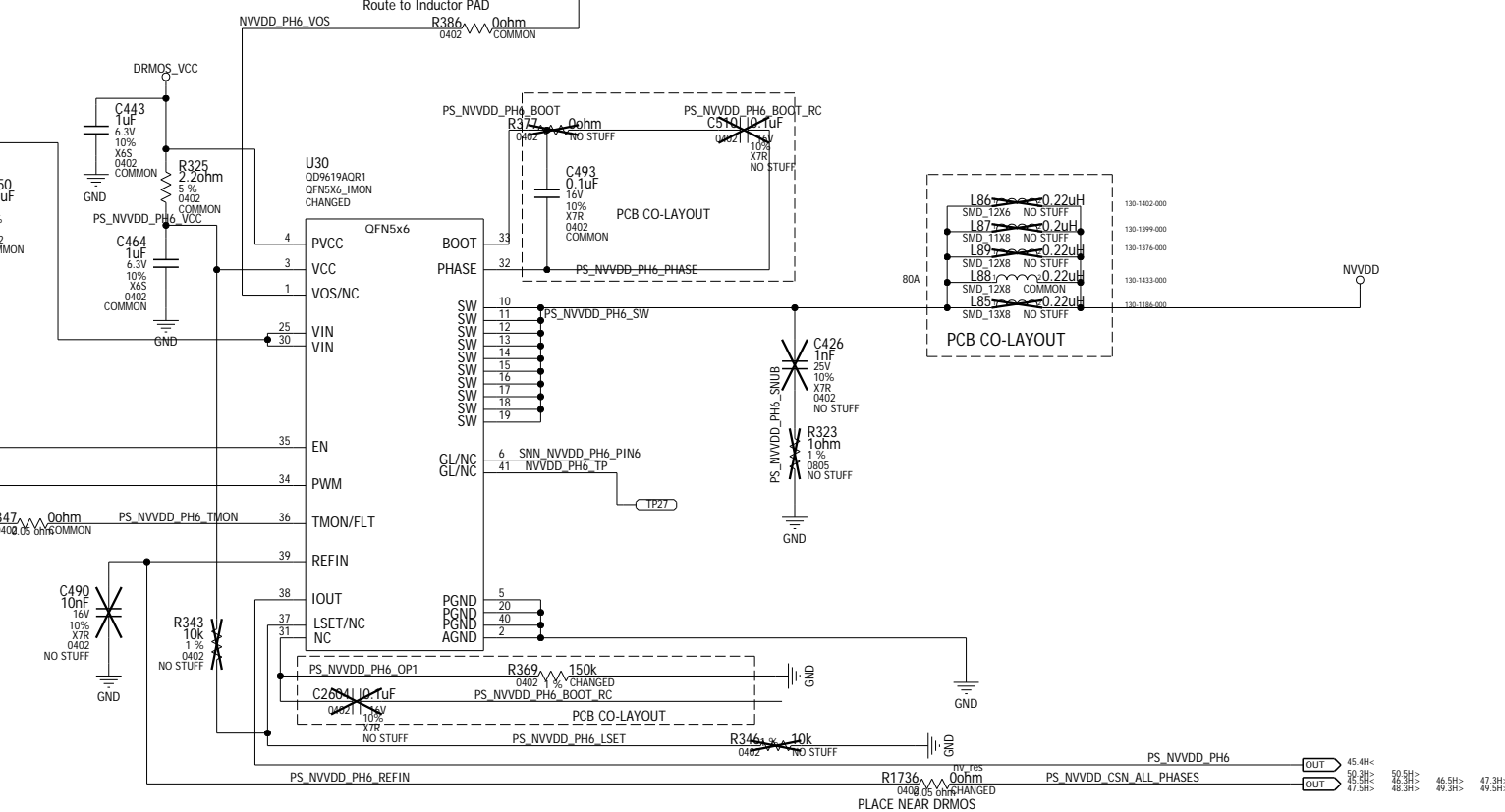
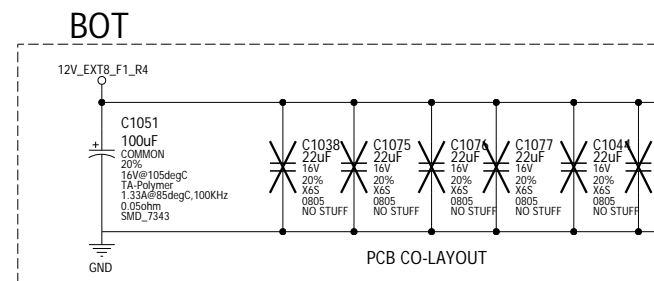
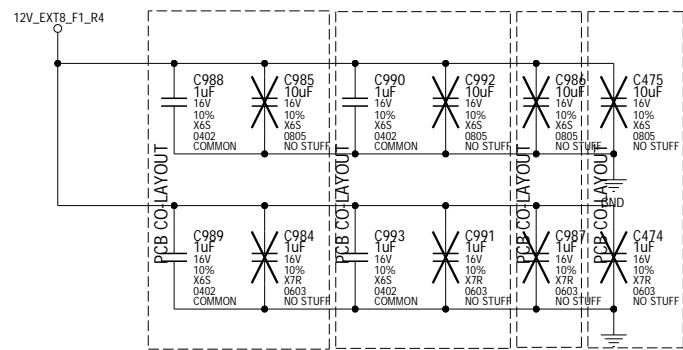
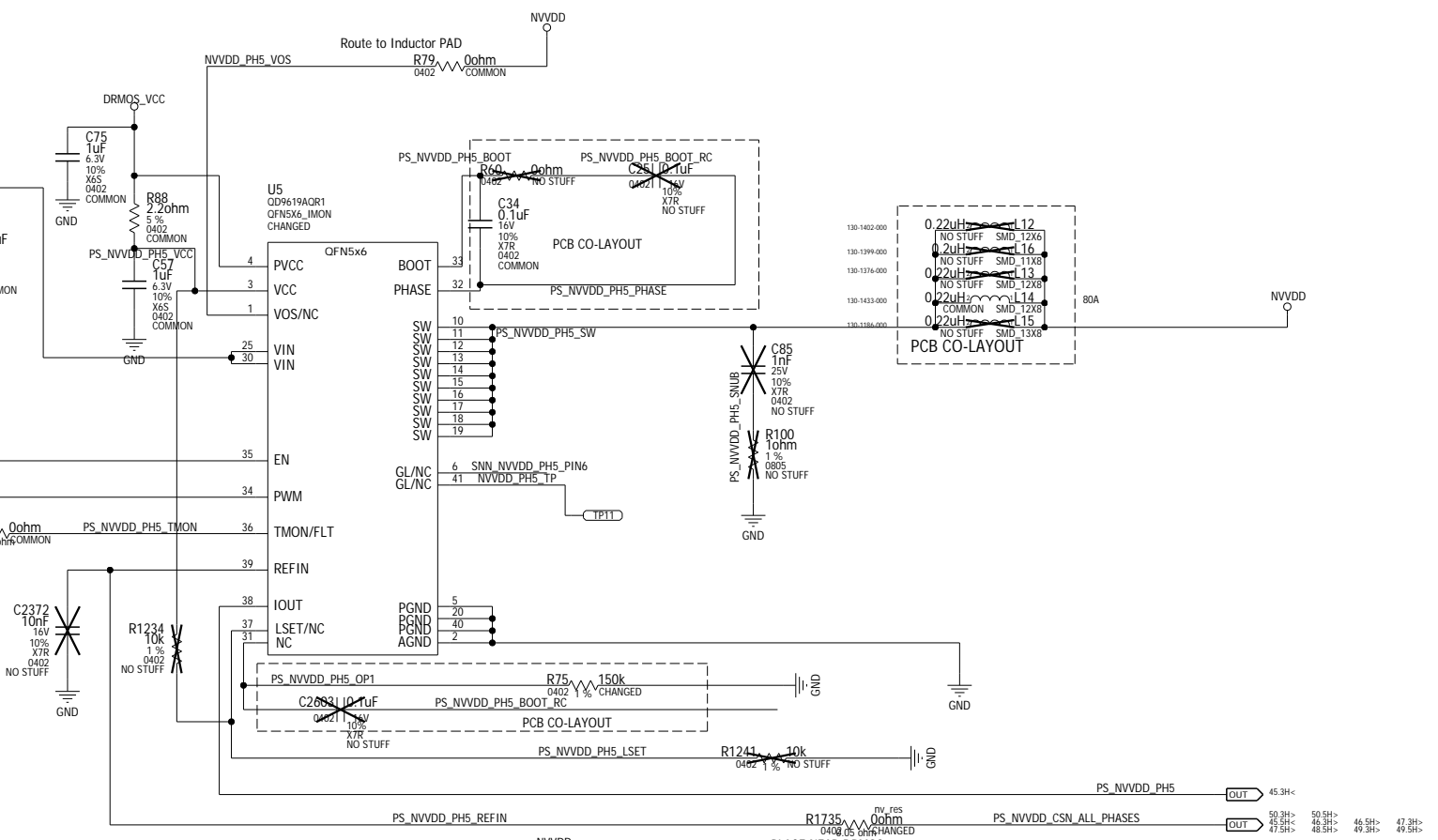
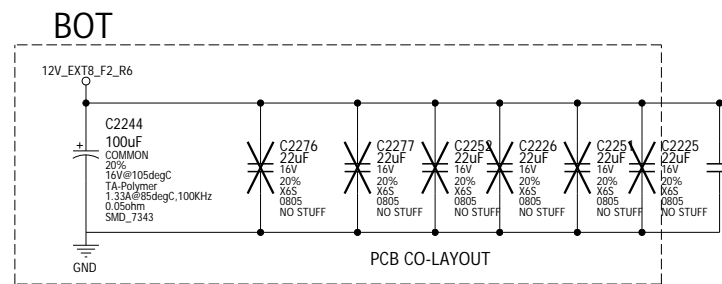
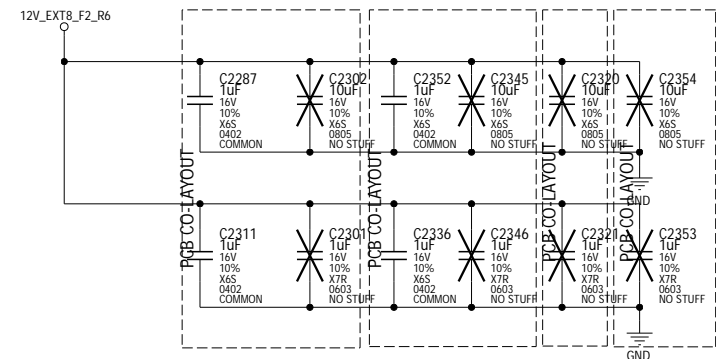
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PCB REV	PG136-A03	PAGE	47 OF 67
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD PH5 (PWM3 ) and PH6 (PWM7 )

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NV_PN	600-1G136-0010-300
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PCB REV	PG136-A03
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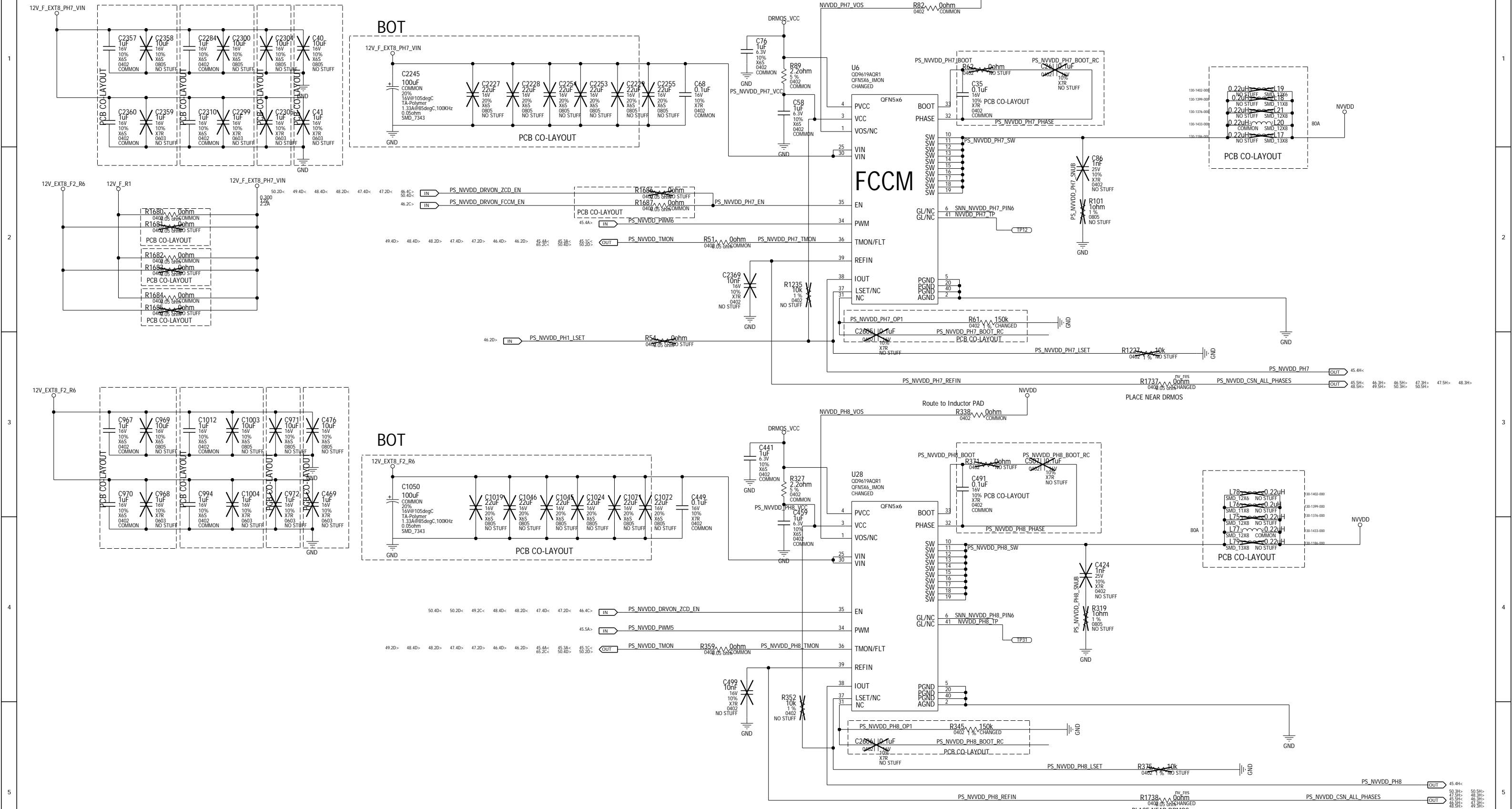
PAGE	48 OF 67
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DATE	26-JUN-2020
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Page 49: PS: NVVDD PH 7 (PWM6), PH8 (PWM5)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NWDD PH7 (PWM6 ) and PH8 (PWM5 )

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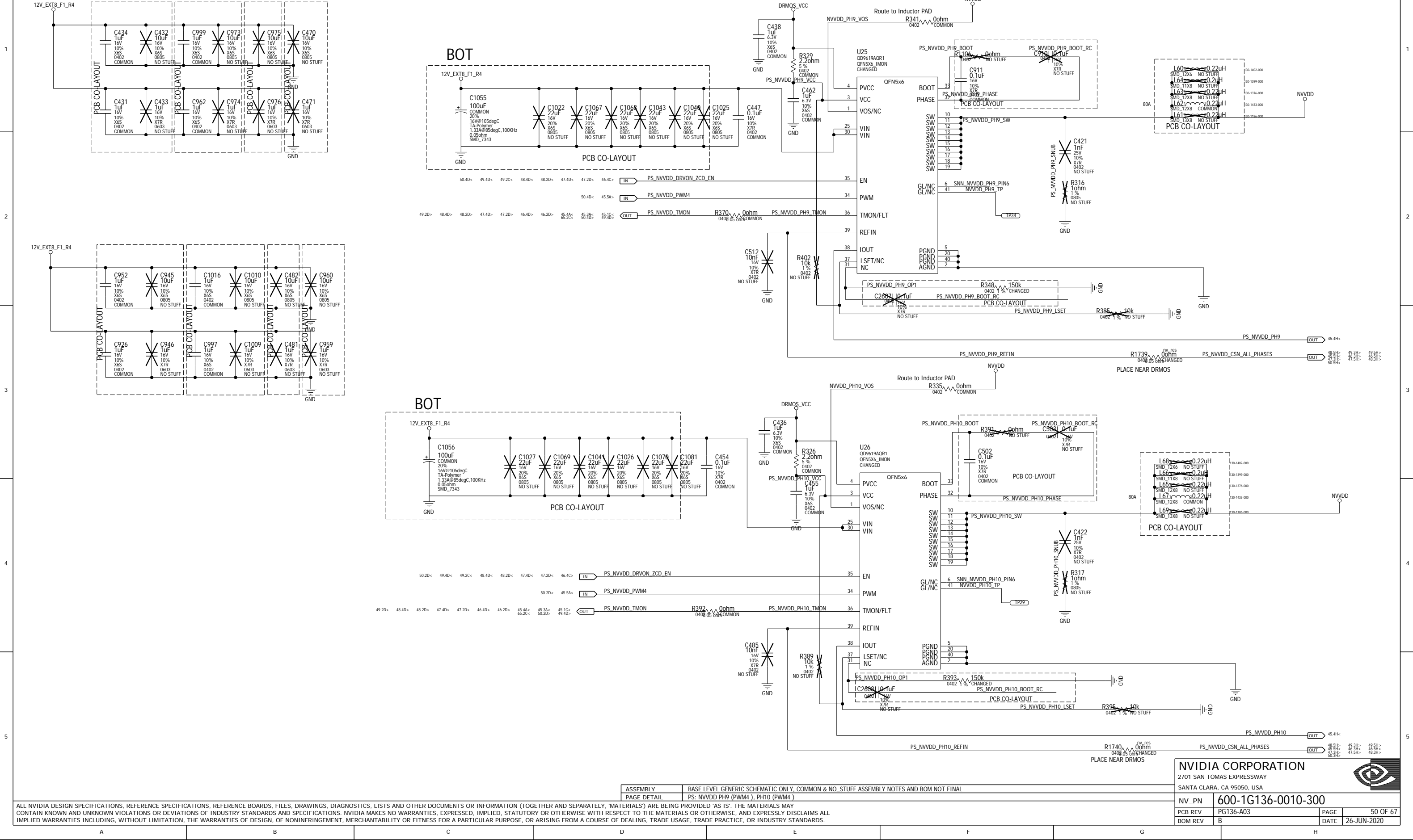
SANTA CLARA, CA 95050, USA

NV_PN	600-1G136-0010-300
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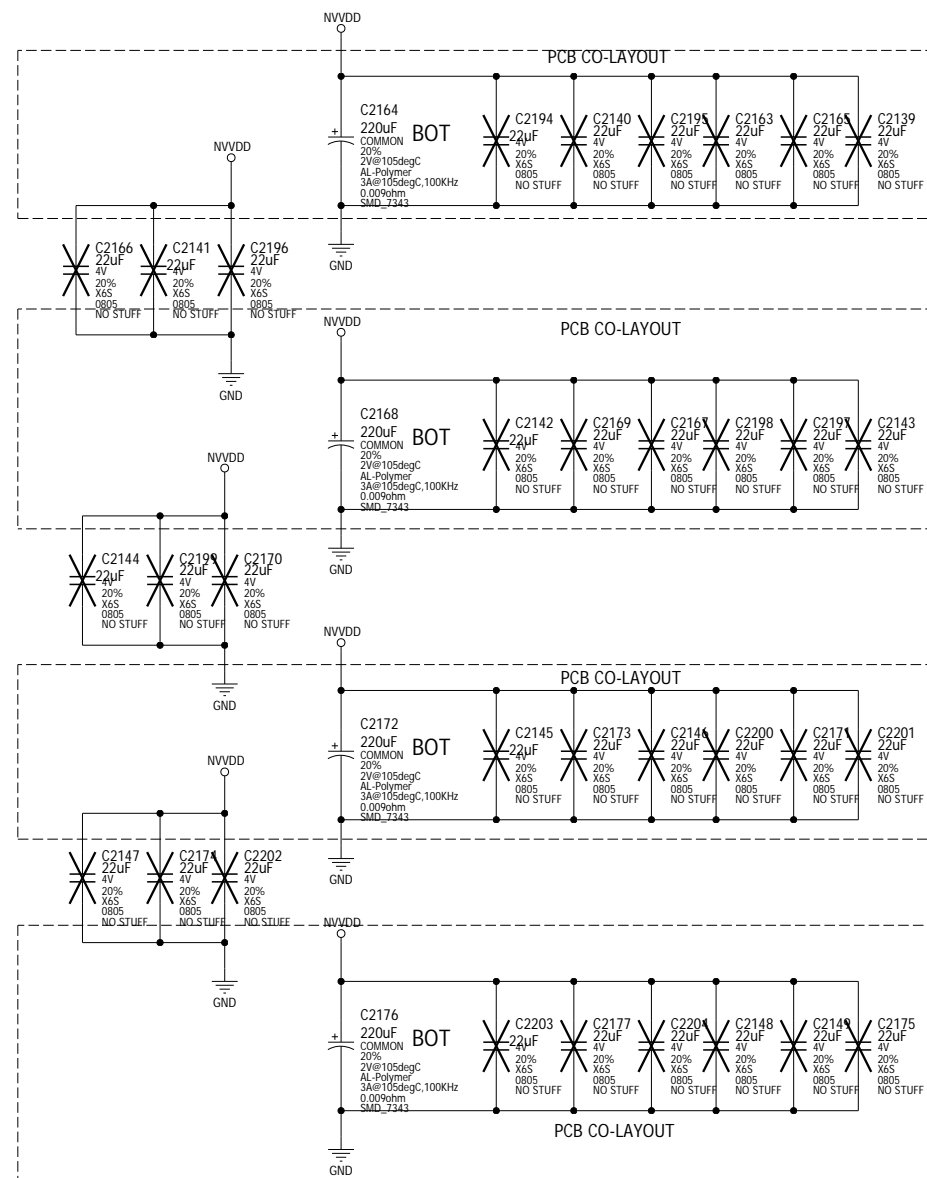
PCB REV	PG136-A03	PAGE	49 OF 67
BOM REV	B	DATE	26-JUN-2020



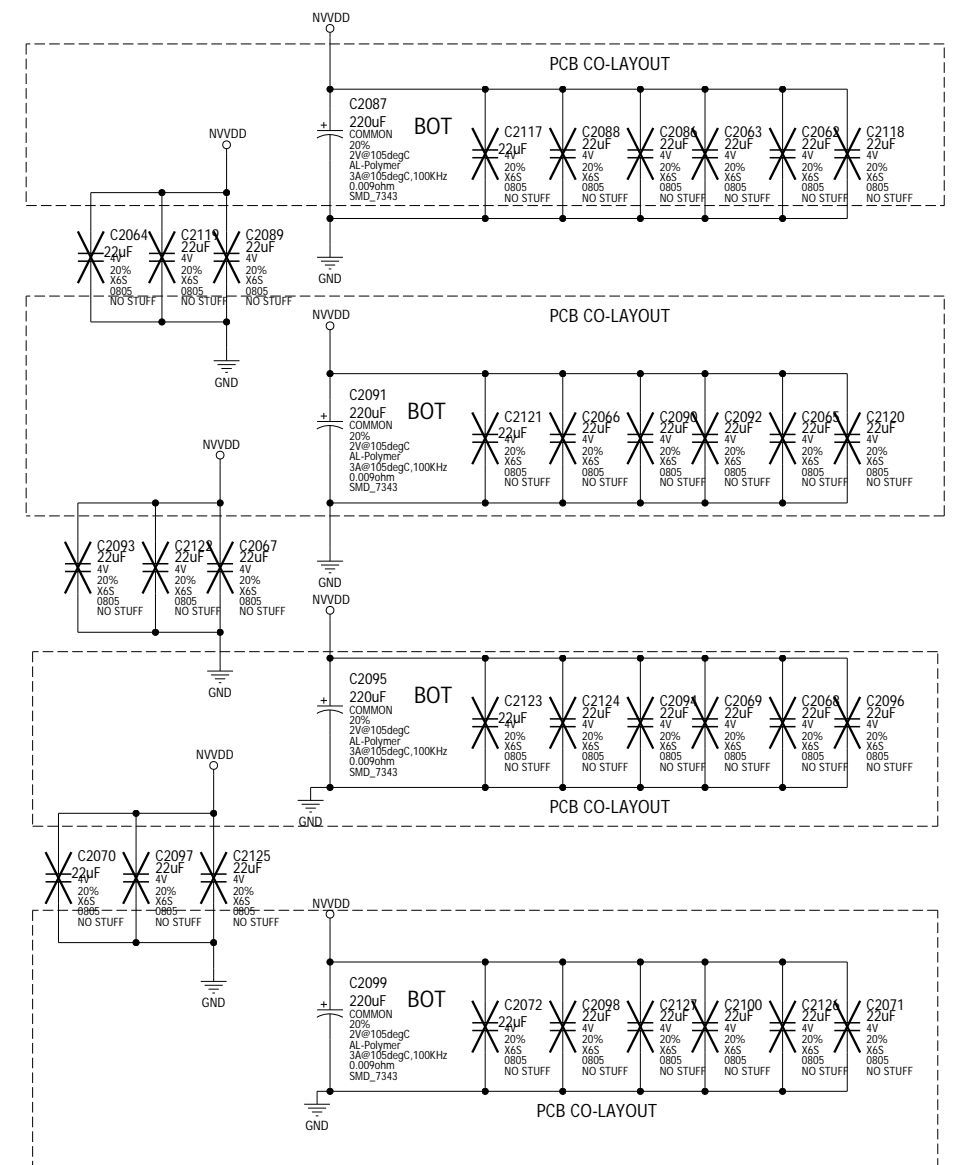
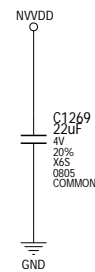
Page 50: PS: NVVDD PH9 (PWM4), PH 10 (PWM4)




## 20x SMD7343 330uF CO-LAYOUT WITH 120x 0805 22uF



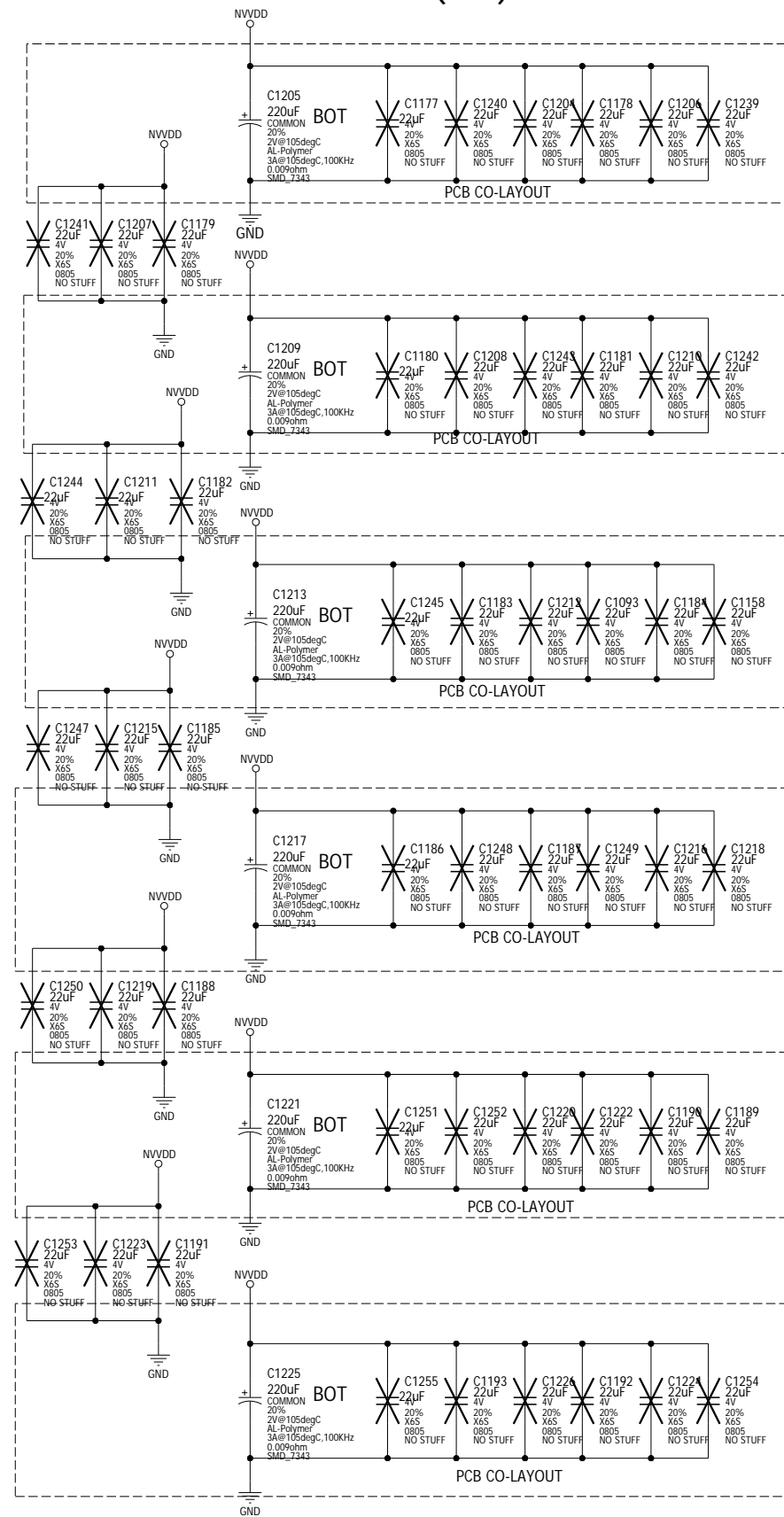
BACK WEST OF PCB



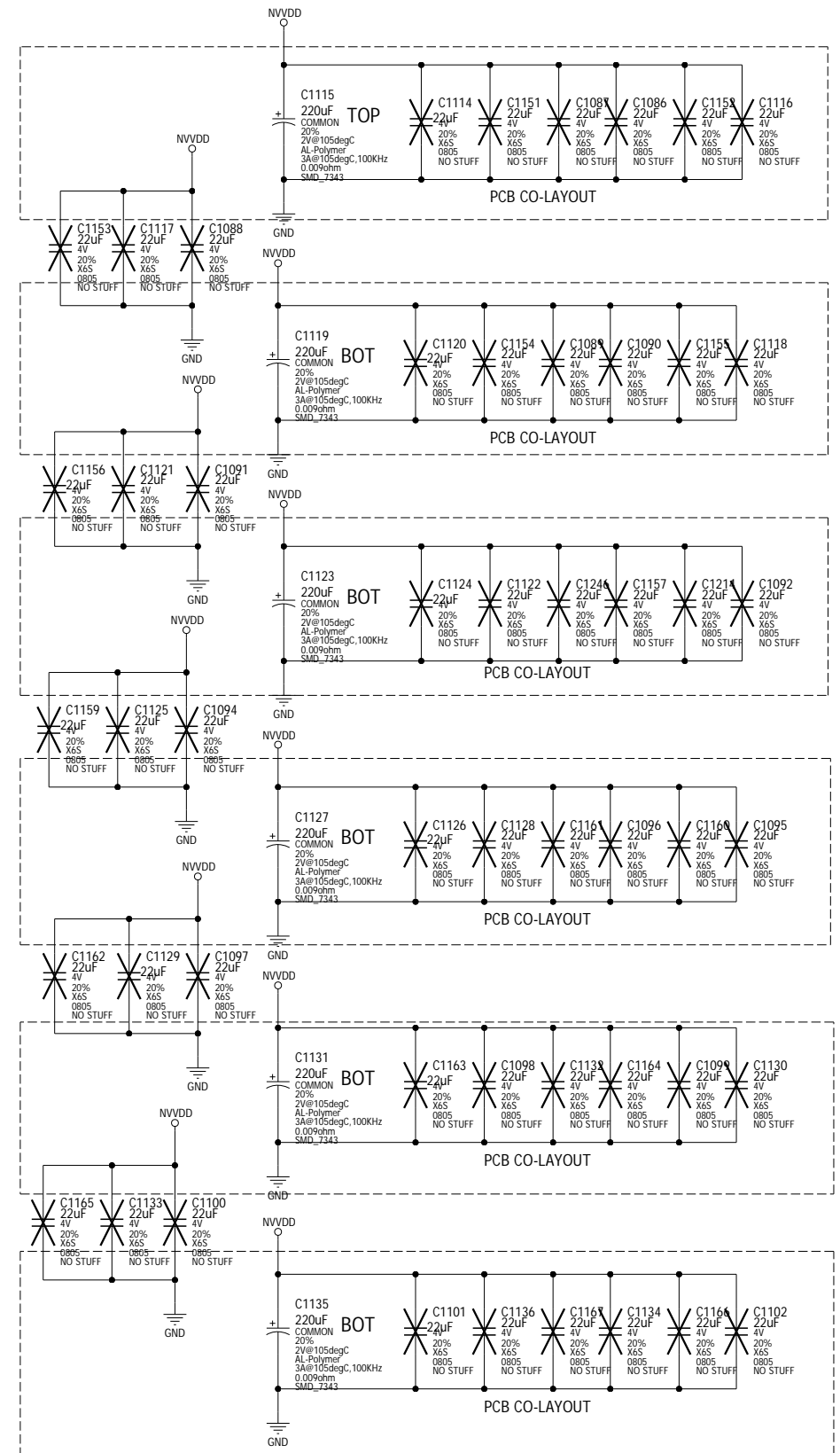
BACK WEST OF PCB

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<b>NV_PN</b> 600-1G136-0010-300			
PCB REV	PG136-A03	PAGE	51 OF 67
BOM REV	B	DATE	26-JUN-2020


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BACK EAST OF PCB



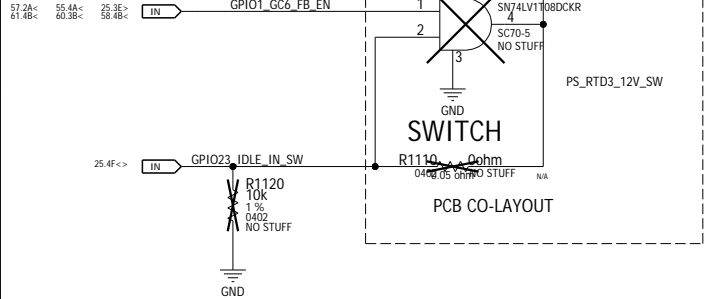
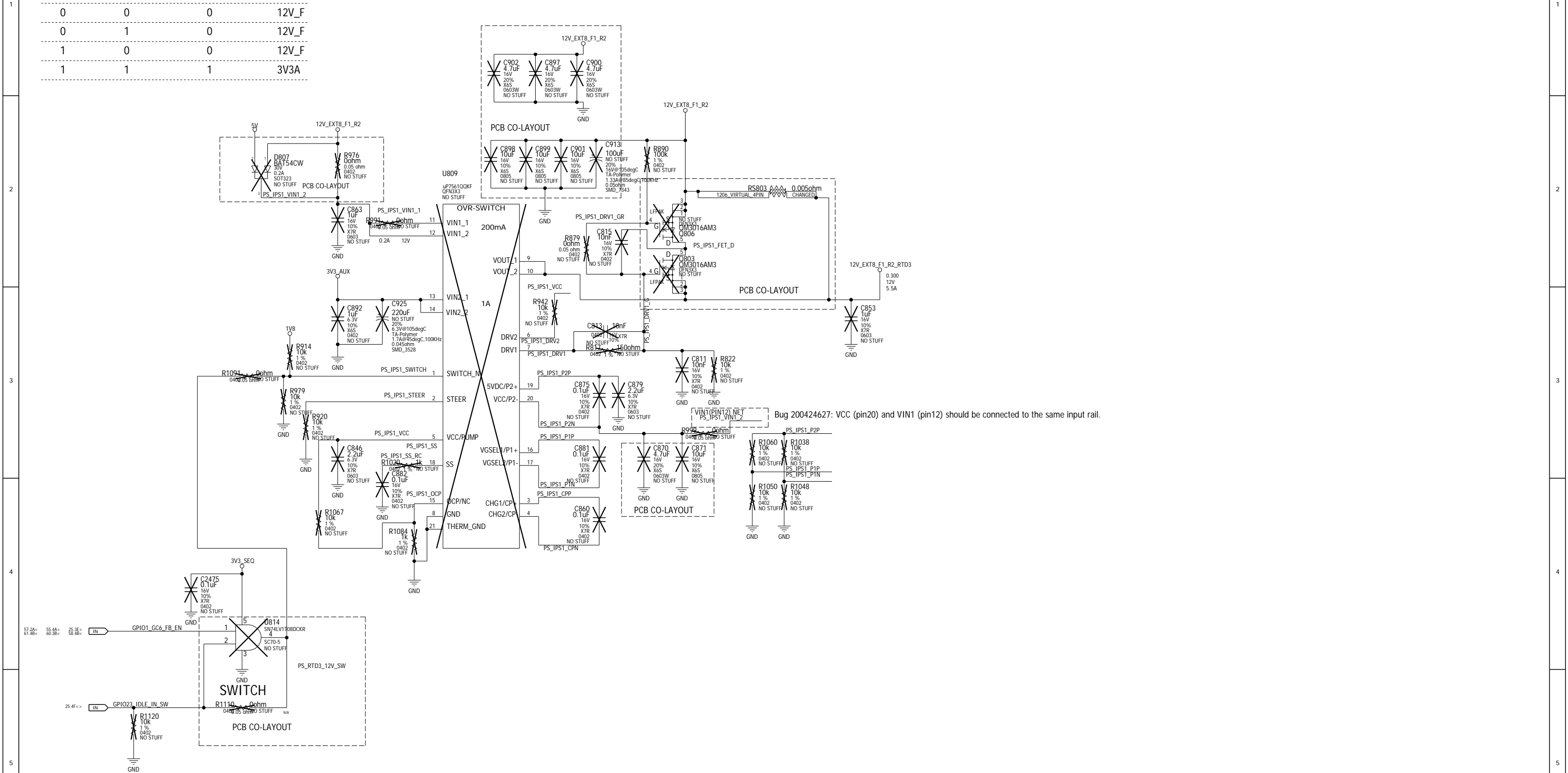
BACK EAST OF PCB

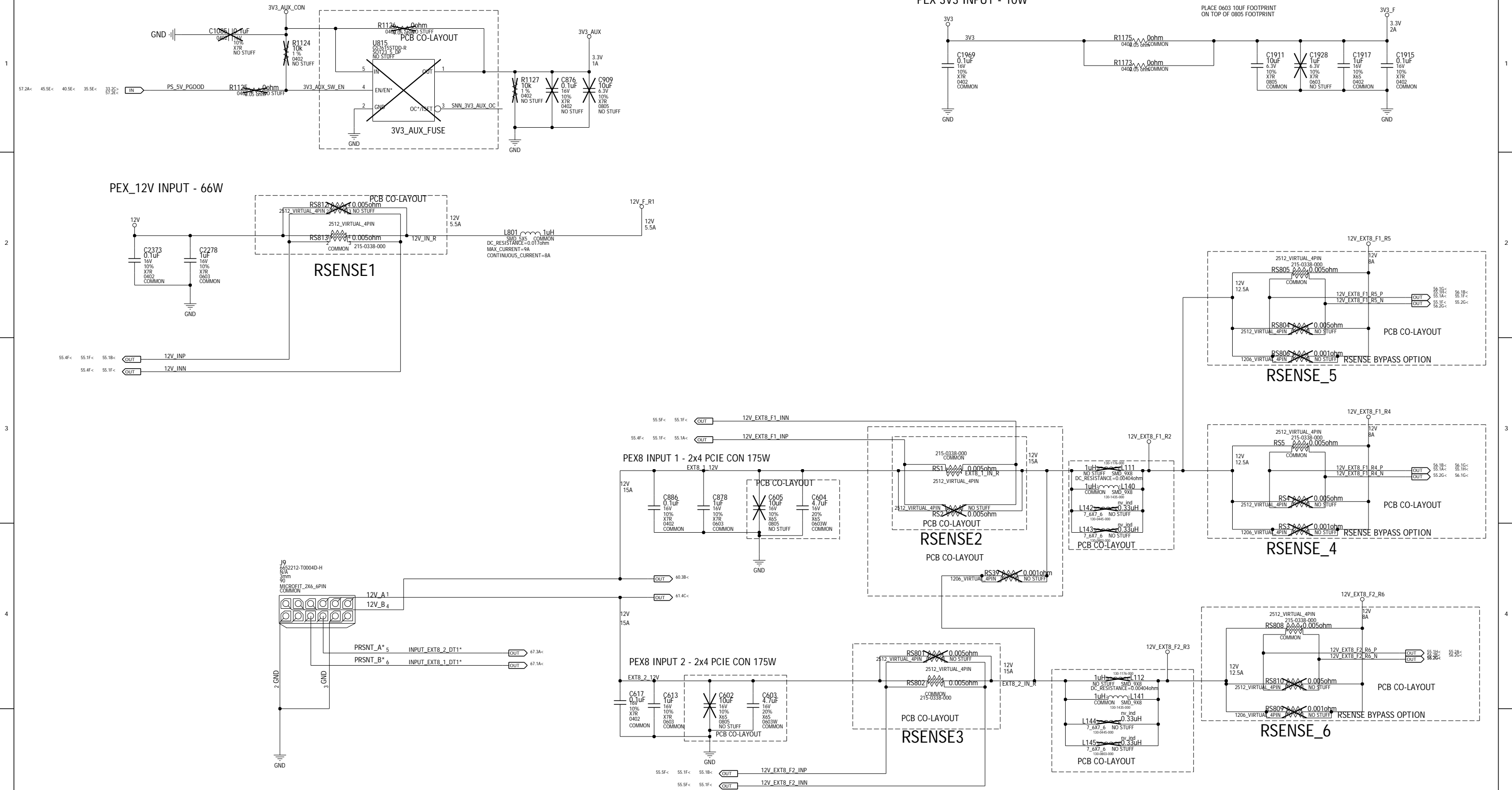
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PCB REV	P136-A03	PAGE	52 OF 67
BOM REV	B	DATE	26-JUN-2020

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AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A





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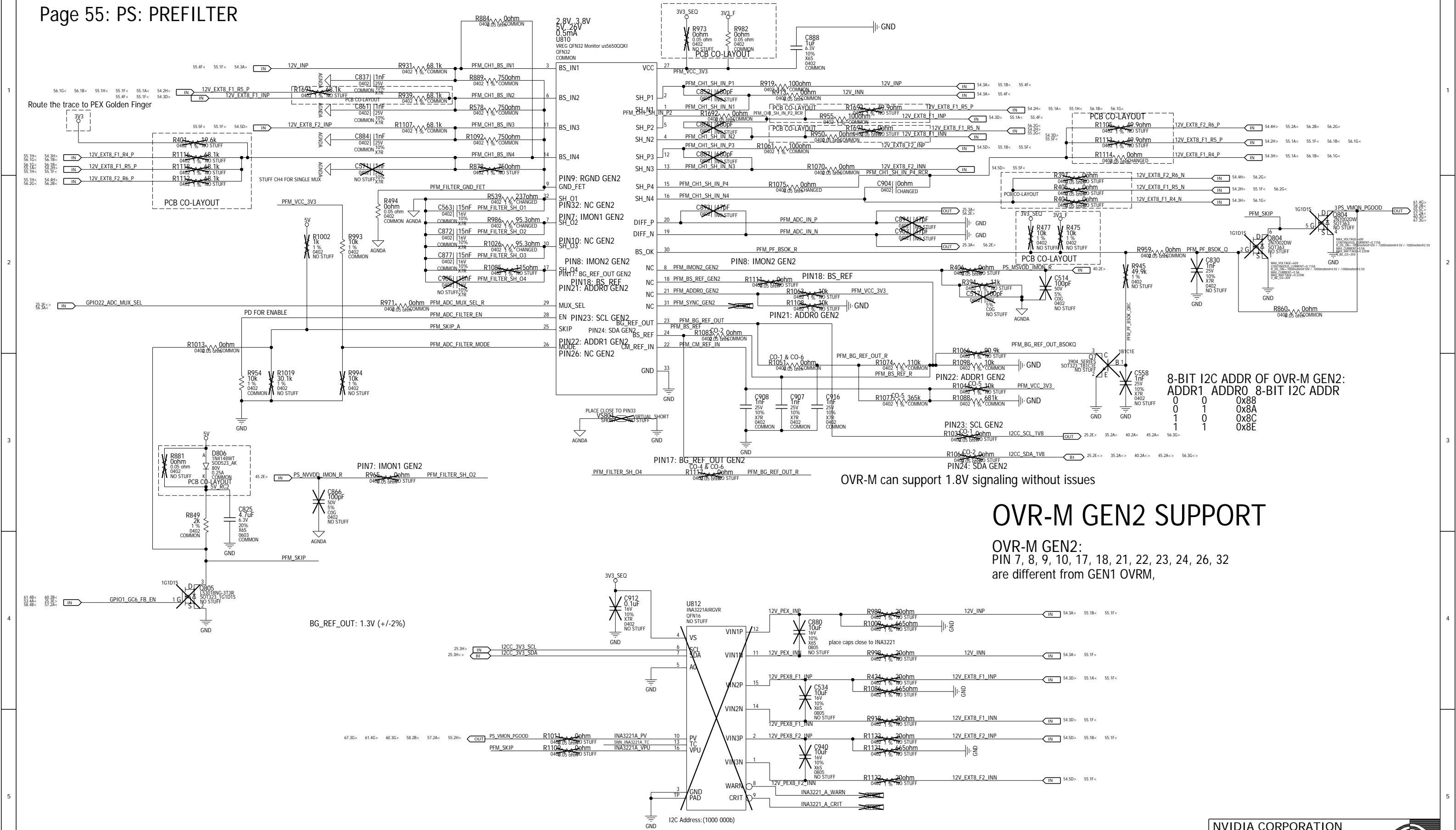
BOM REV B

PAGE 54 OF 67

DATE 26-JUN-2020

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: INPUTS, FILTERING, MONITORING



OVR-M can support 1.8V signaling without issues

# OVR-M GEN2 SUPPORT

OVR-M GEN2:  
PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32  
are different from GEN1 OVRM,

8-BIT I2C ADDR OF OVR-M GEN2:		
ADDR1	ADDR0	8-BIT I2C ADDR
0	0	0x88
0	1	0x8A
1	0	0x8C
1	1	0x8E

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: PREFILTER A/INA3221

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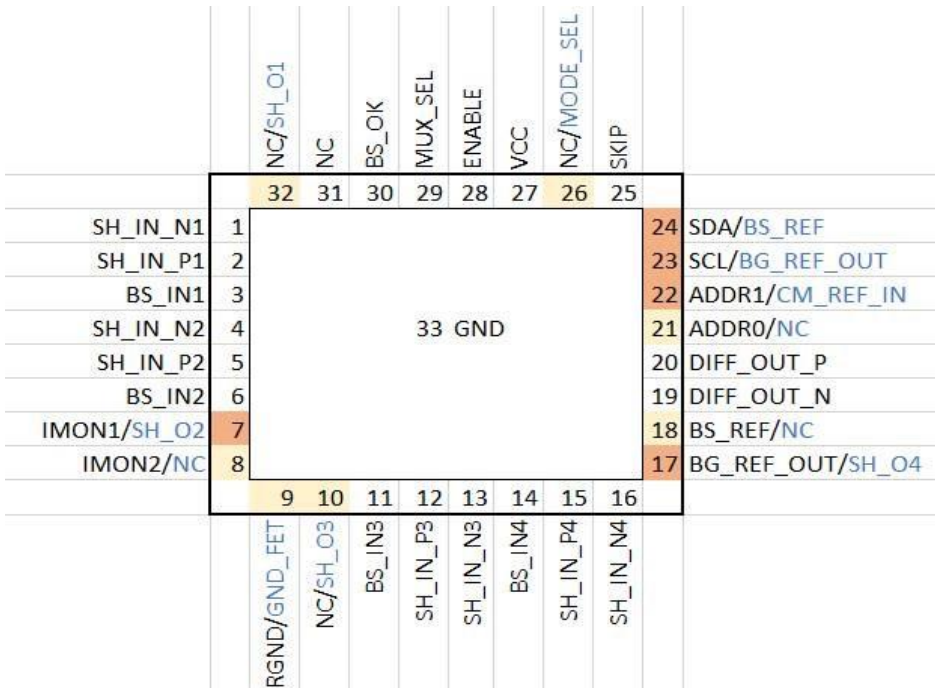
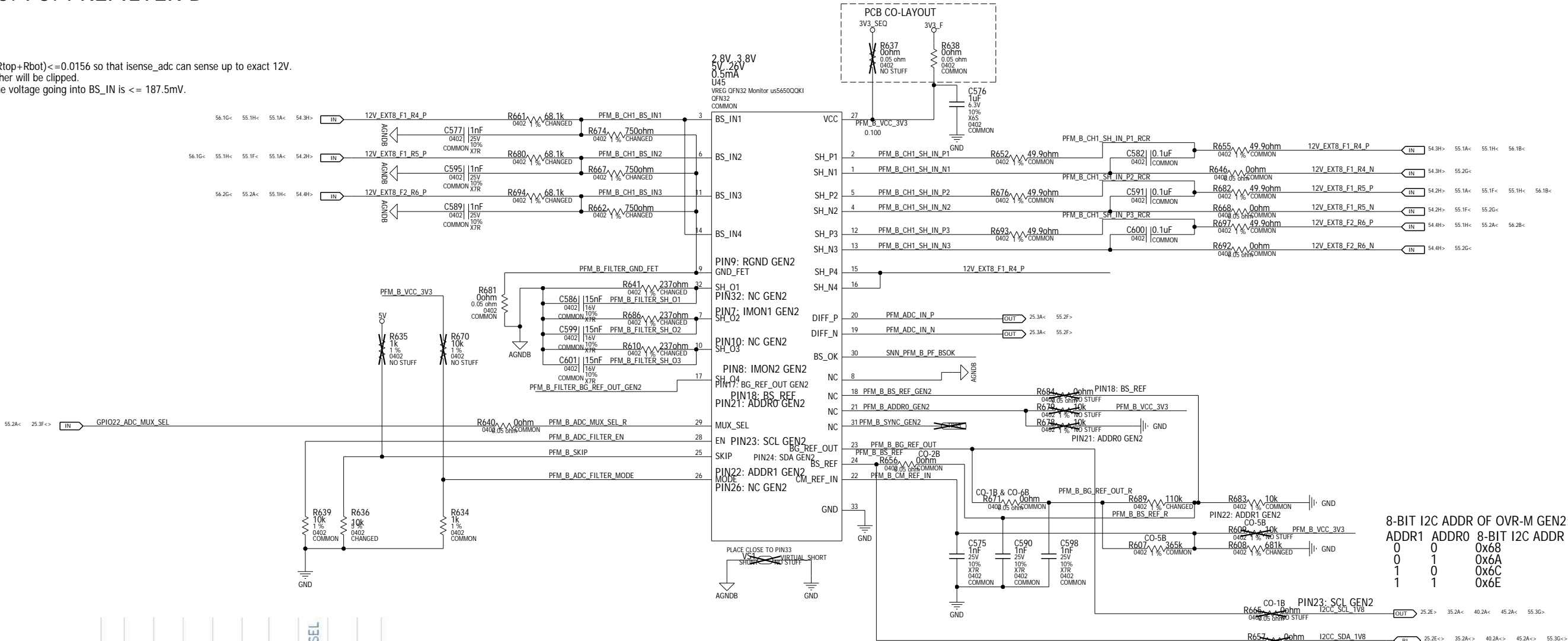
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BUS:  $R_{bot}/(R_{top}+R_{bot}) < 0.0156$  so that `isense_adc` can sense up to exact 12V.  
Anything higher will be clipped.  
Make sure the voltage going into `BS_IN` is  $\leq 187.5\text{mV}$ .



# OVR-M GEN2 SUPPORT

OVR-M GEN2:  
PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32  
are different from GEN1 OVRM,

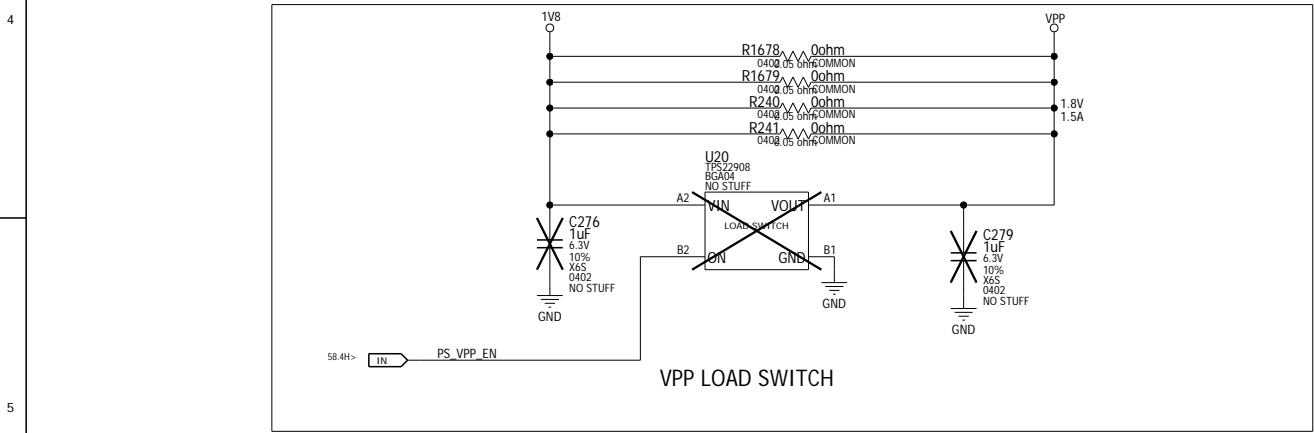
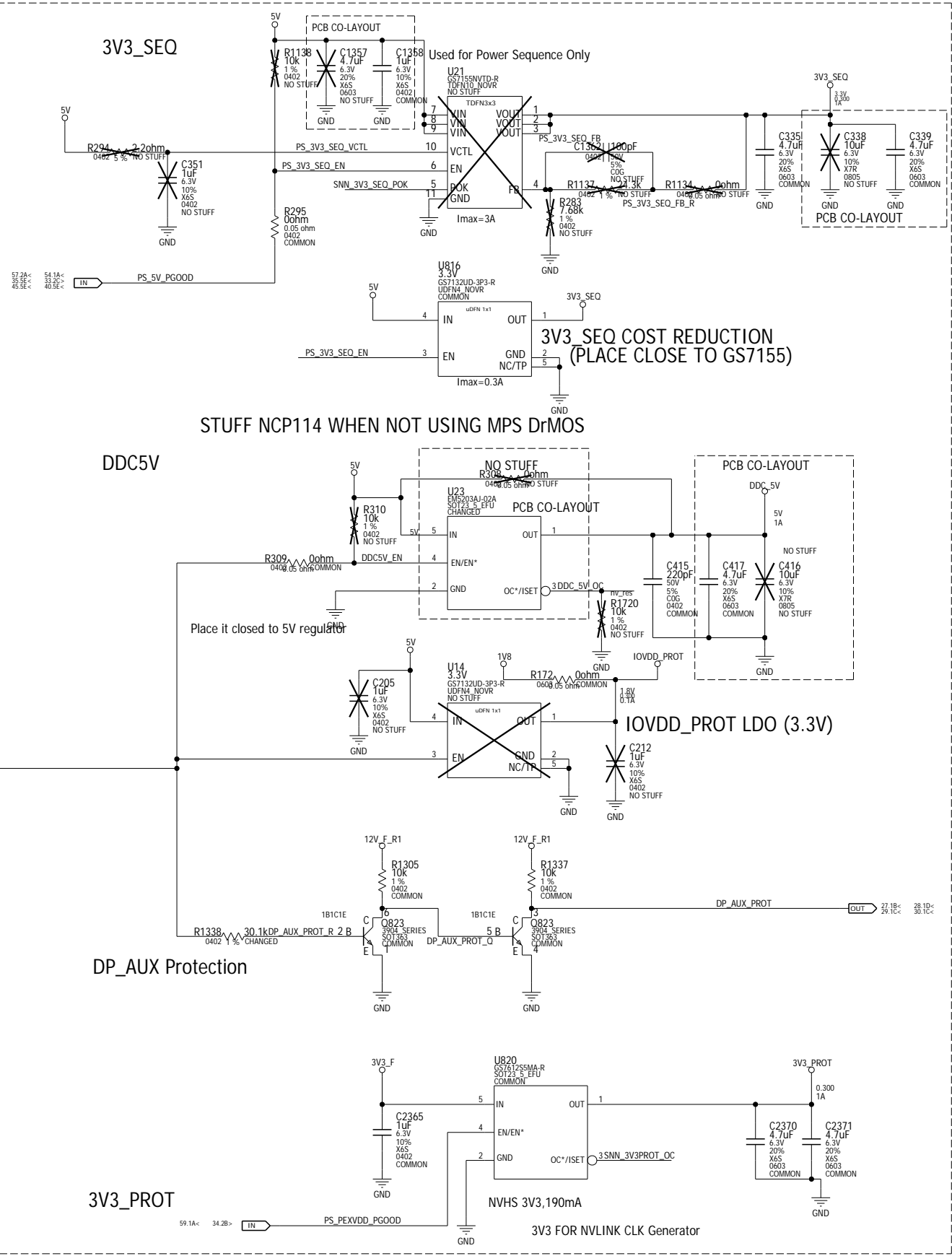
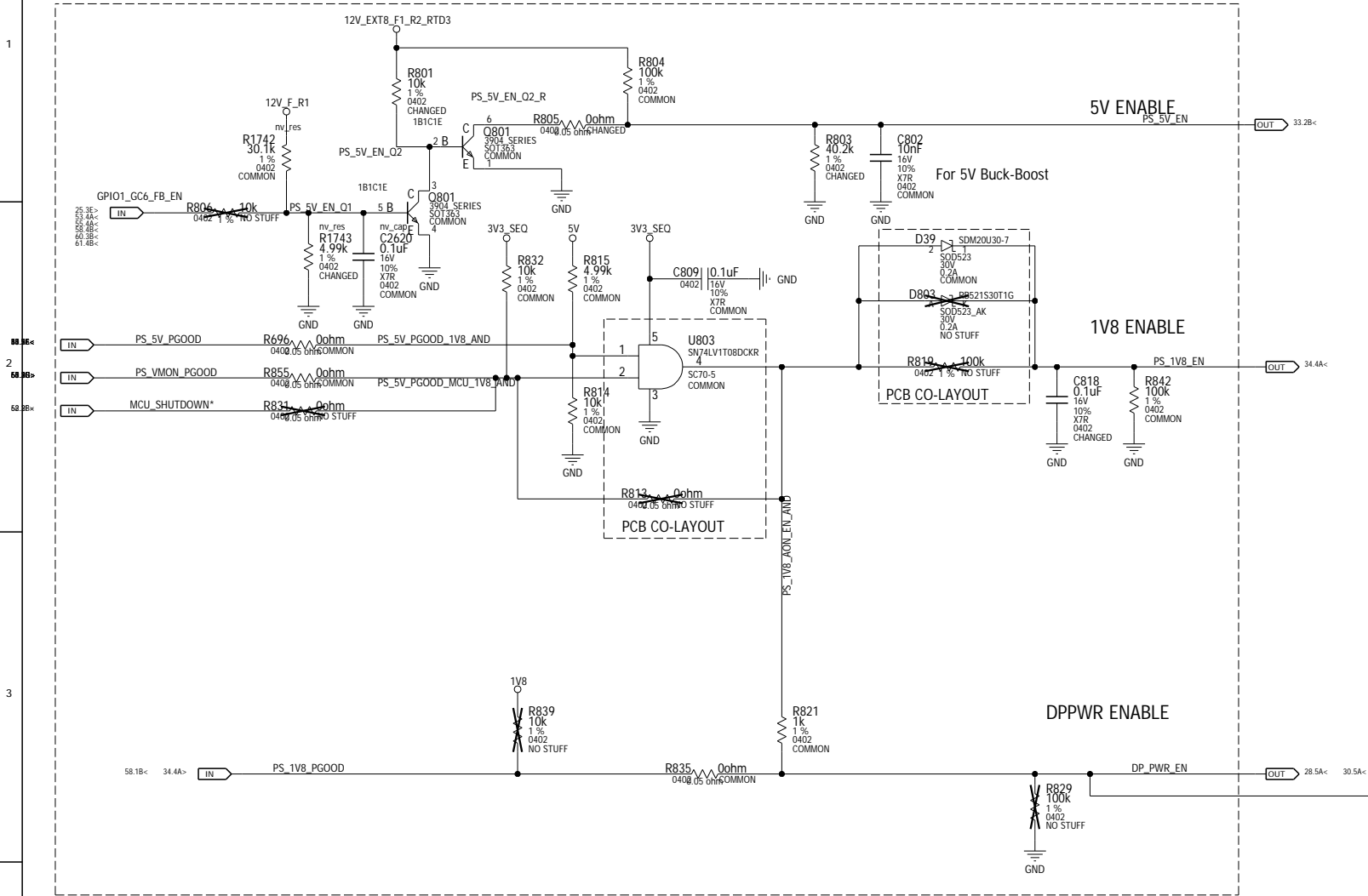
OVR-M can support 1.8V signaling without issues

8-BIT I2C ADDR OF OVR-M GEN2:		
ADDR1	ADDR0	8-BIT I2C ADDR
0	0	0x68
0	1	0x6A
1	0	0x6C
1	1	0x6E

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: PREFILTER B

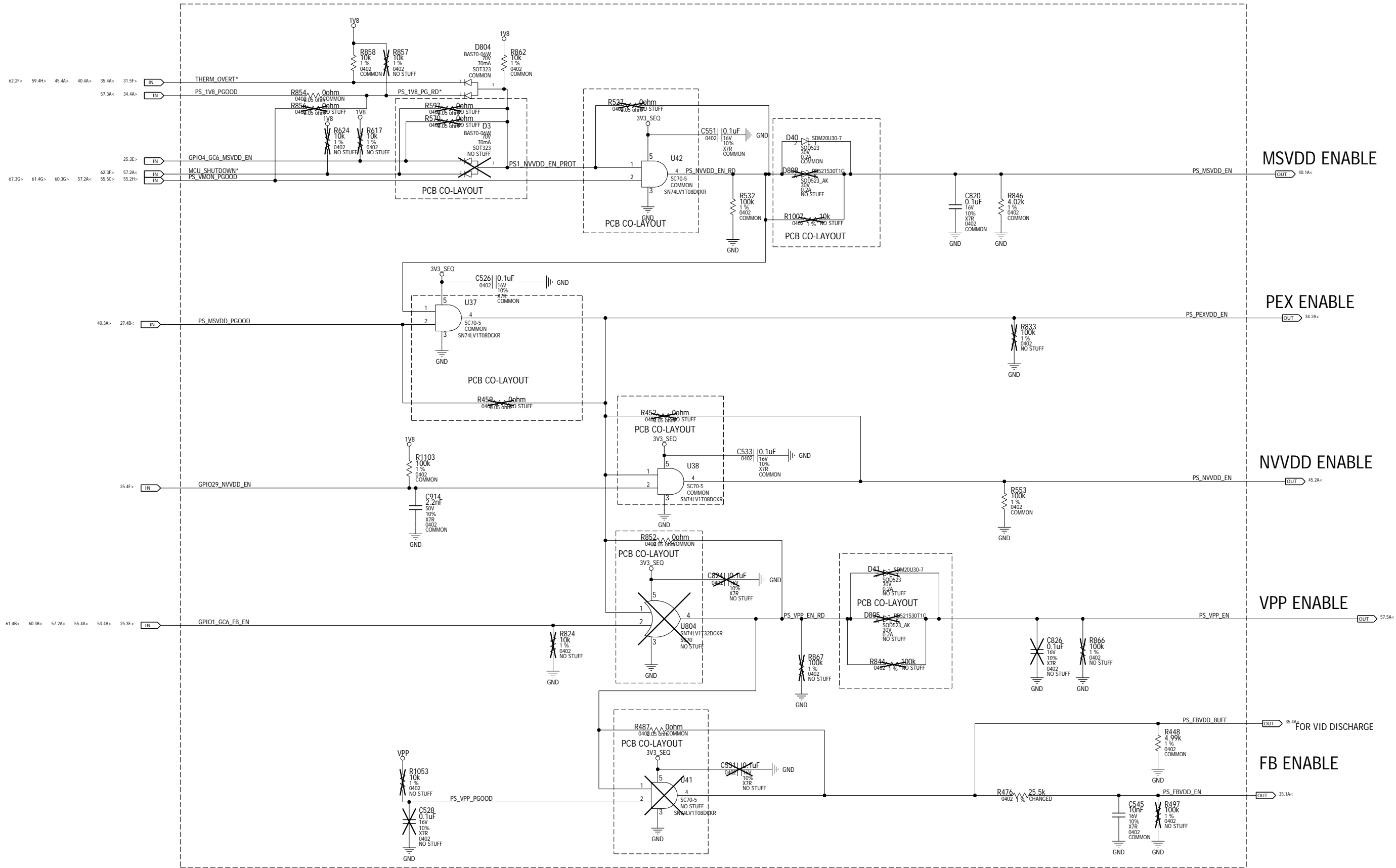
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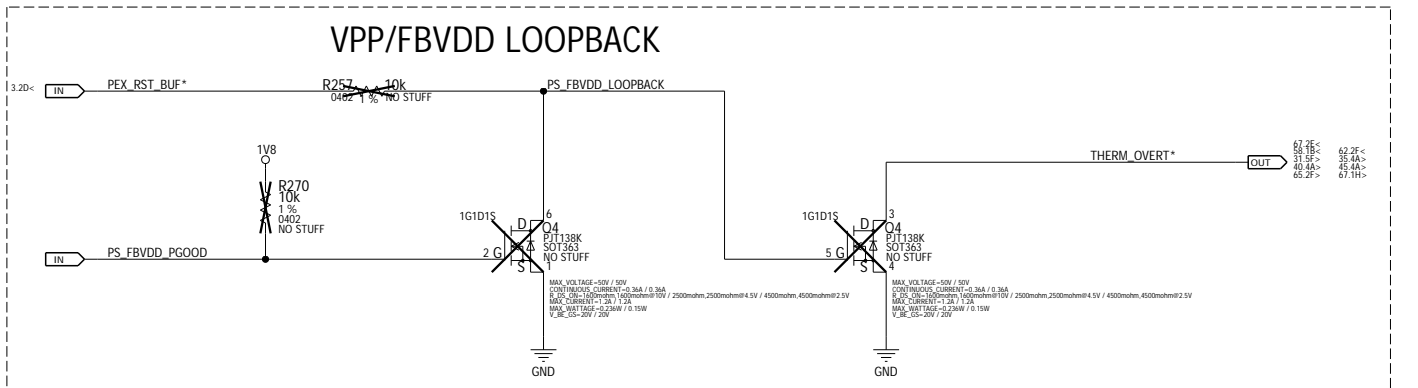
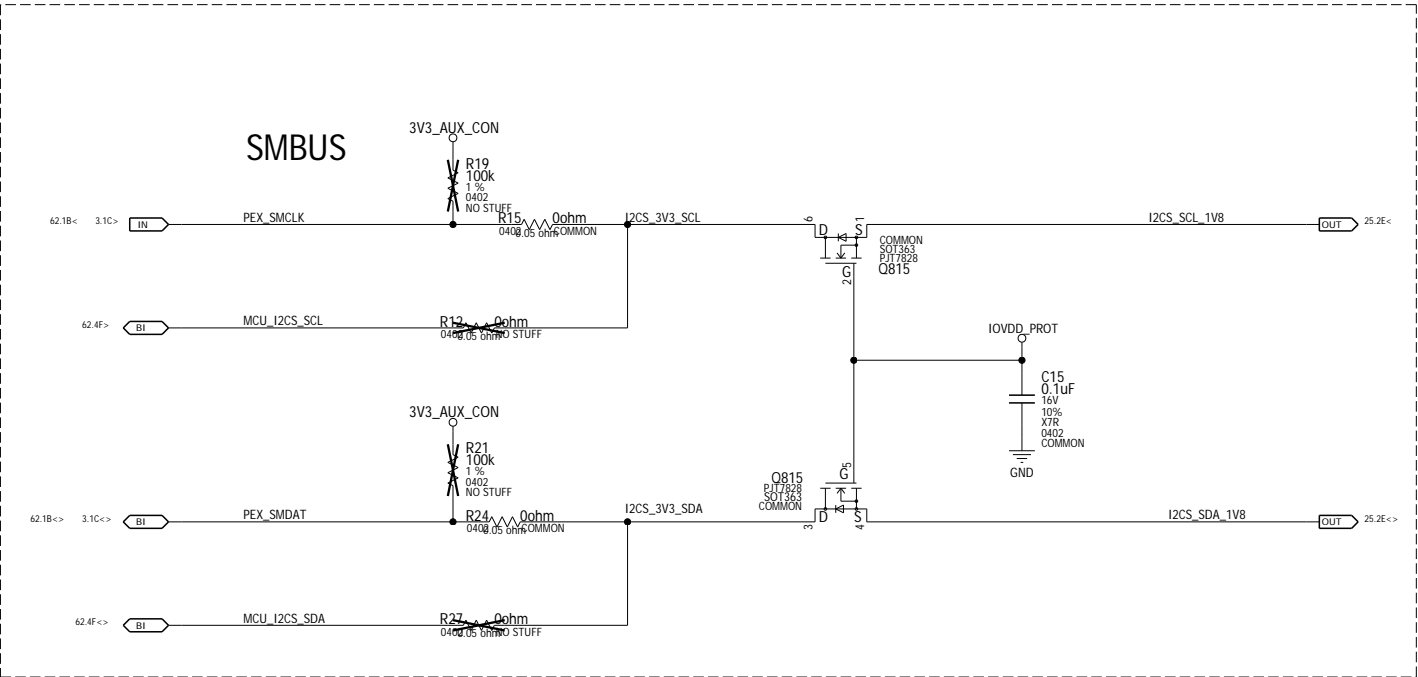
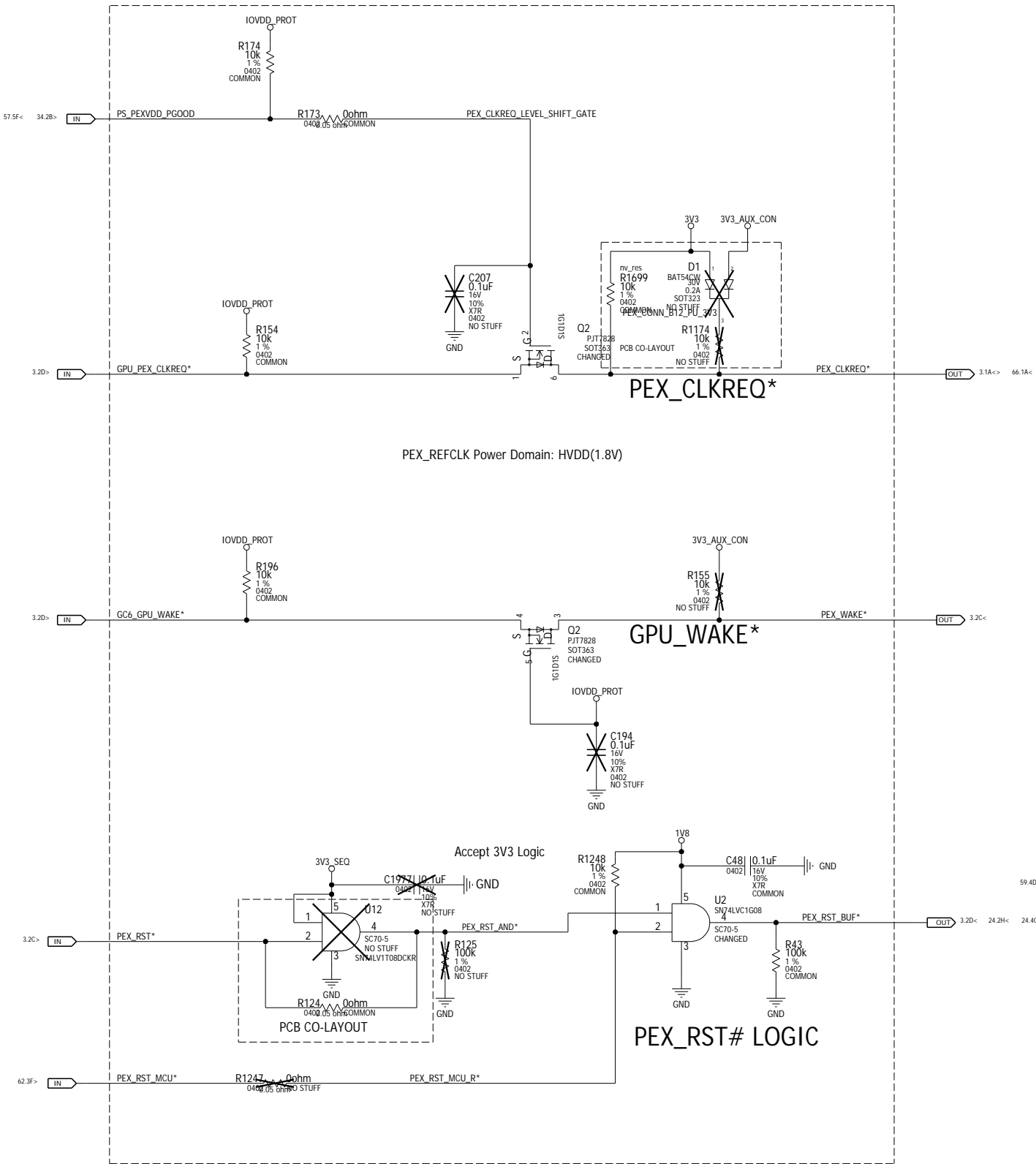


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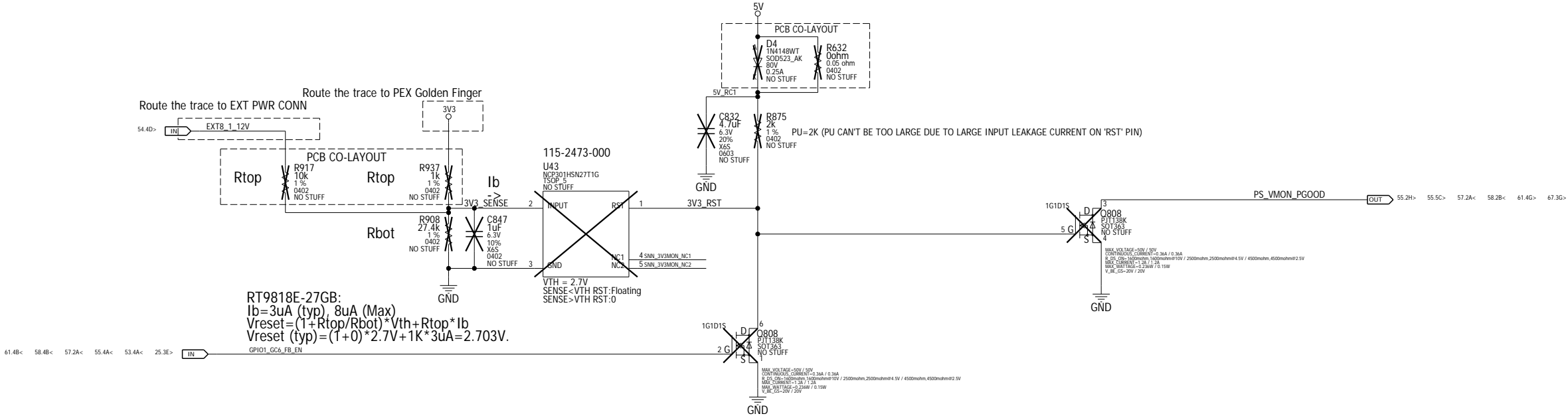
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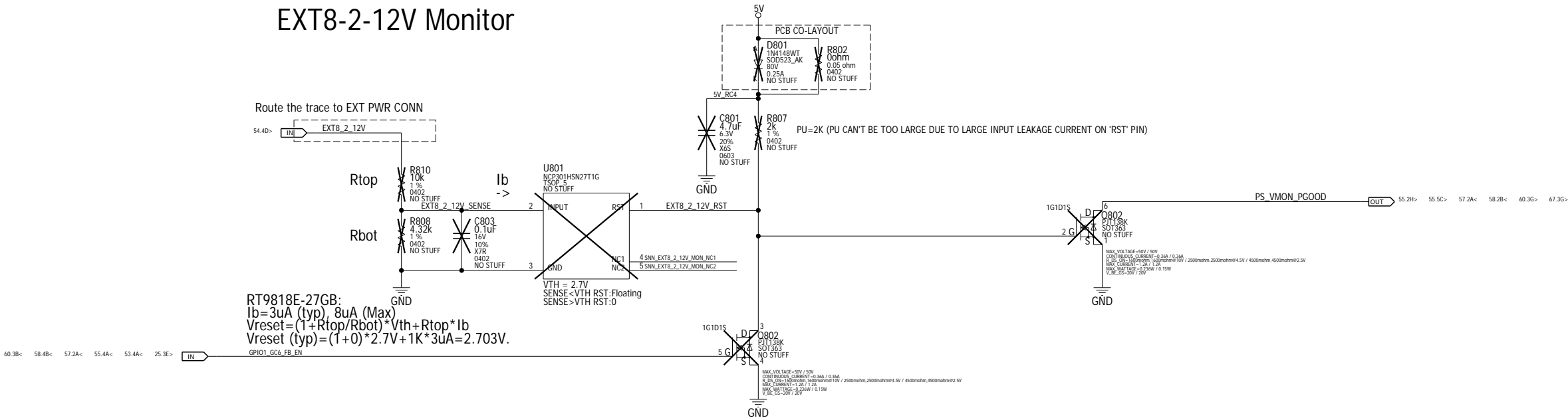
PEX3V3 or EXT8-1-12V Monitor

Vth=2.7V (+/- 0.0405V/1.5%). Vhys(Typ)=0.01\*Vth, Vhys(Max)=0.016\*Vth  
1) Suppose that at t=0s, Vin is greater than (2.7V + Vhys), Vreset=LOW. After Vin decreases to 2.7V (+/- 0.0405V), Vreset=floating.  
2) Suppose that at t=0s, Vin is smaller than (2.7V), Vreset=floating. After Vin increases to [2.7V (+/- 0.0405V) + Vhys], Vreset=LOW.

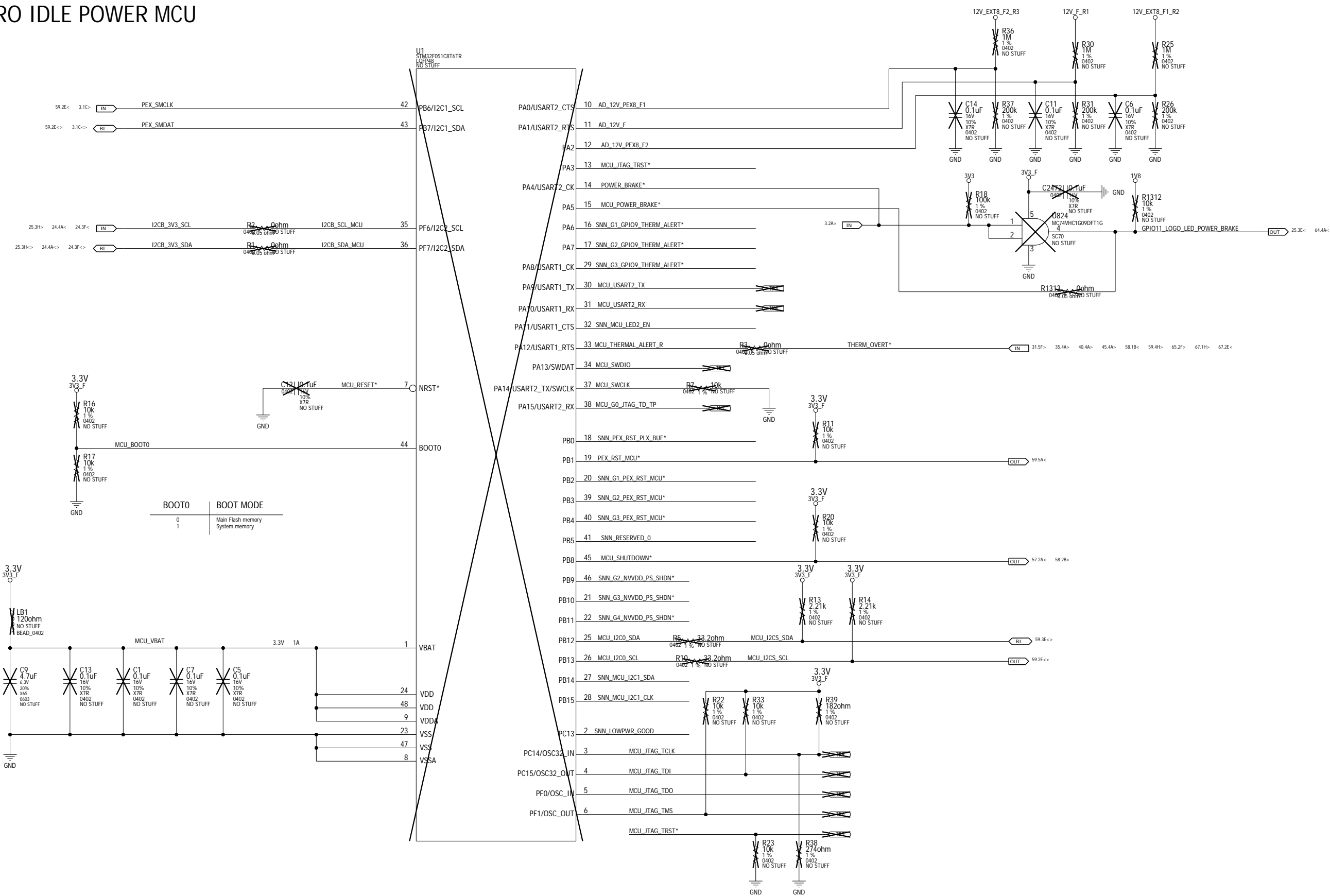


EXT8-1-12V Monitor: Co-layout with PEX3V3 Monitor

EXT8-2-12V Monitor



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2-PIN LED HEADER FOR NORTH LOGO LED (WHITE)

White LED: Preliminary Vf = 2.7V-3.3V @ 20mA

NORTH LOGO LED (WHITE)

(LED should not blink during boot)

NOTE: LED POR IS NOT SET YET.

PCB CO-LAYOUT

DUAL FAN 6-PIN FFC HEADERS W/ 0.5MM PITCH

FAN B (RIGHT)

FAN A (LEFT)

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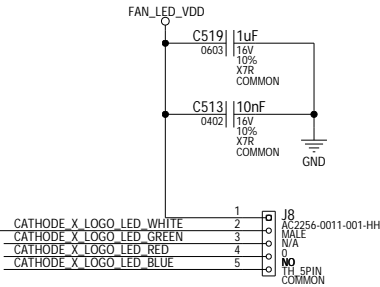
BOM REV B

PAGE 63 OF 67

DATE 26-JUN-2020

NOTE: LED POR IS NOT SET YET.

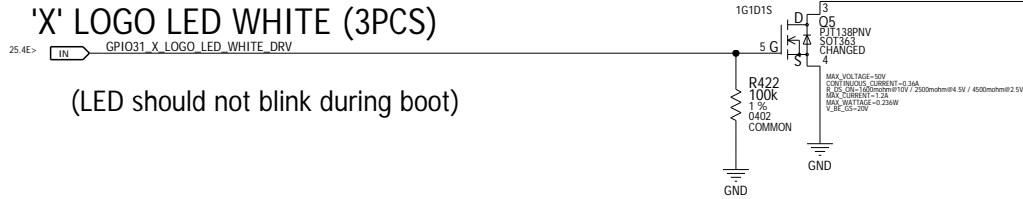
5-PIN POGO-PIN HEADERS FOR 'X' LOGO LEDS



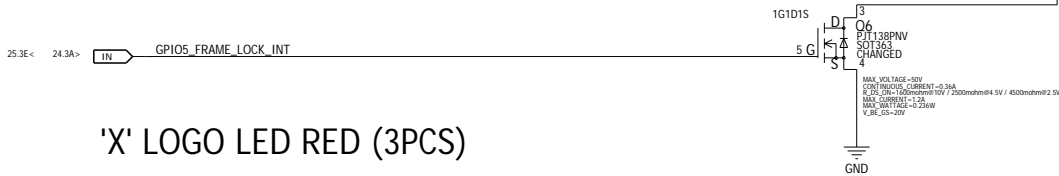
- 1: 12V
- 2: White
- 3: GREEN
- 4: RED
- 5: Blue

'X' LOGO LED WHITE (3PCS)

(LED should not blink during boot)

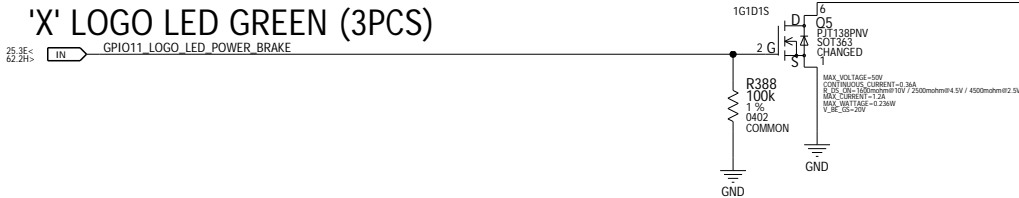


'X' LOGO LED RED (3PCS)



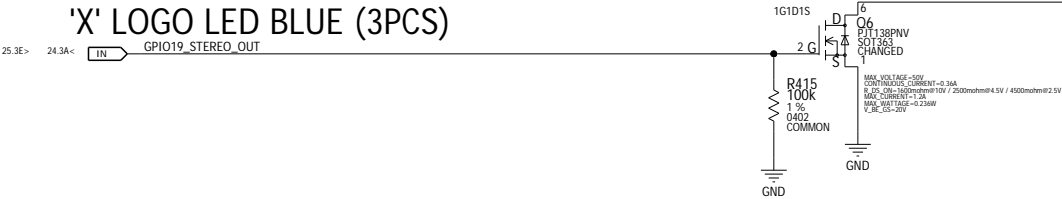
Green LED: Vf = ??V @ ??mA

'X' LOGO LED GREEN (3PCS)



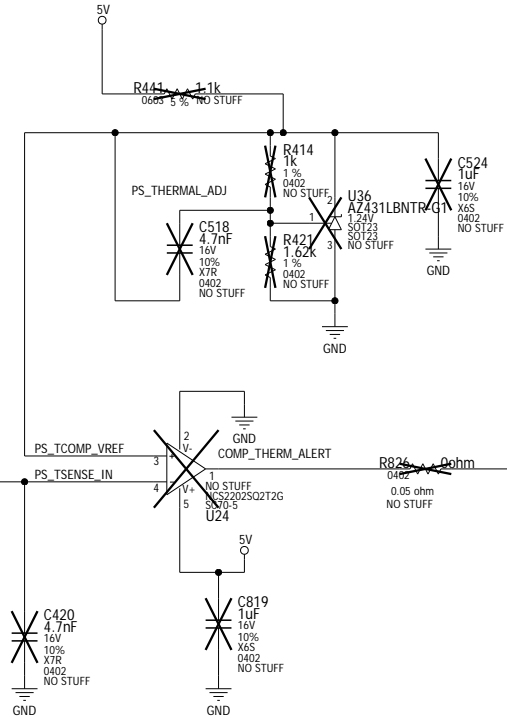
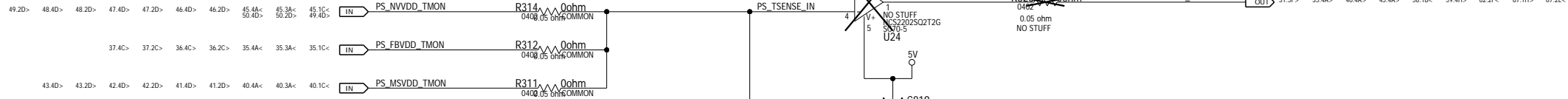
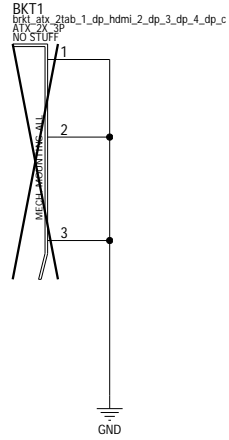
Blue LED: Vf = ??V @ ??mA

'X' LOGO LED BLUE (3PCS)

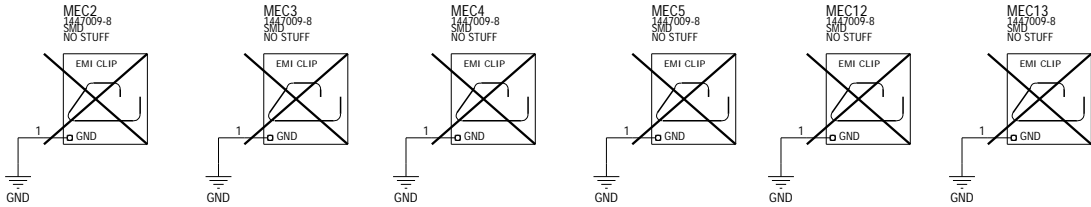


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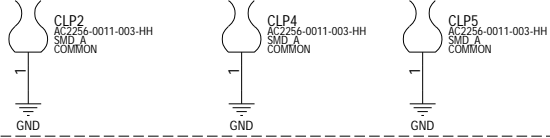




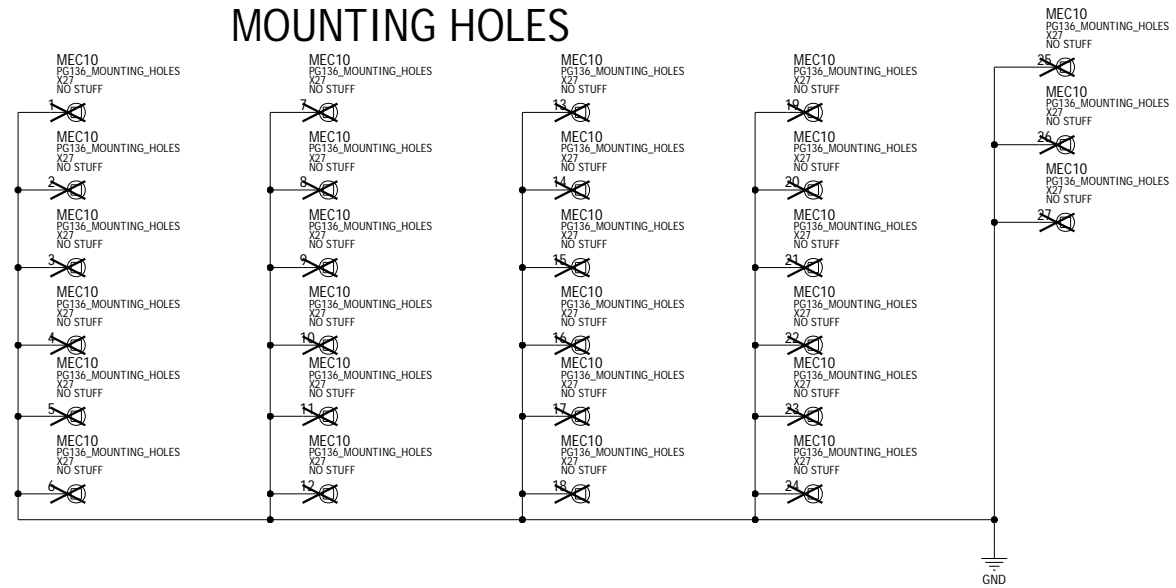
## TOP: 6x EMI CLIPS



## BOT: 3x RETENTION SPRINGS



## MOUNTING HOLES



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MECH & VR THERMAL PROTECTION

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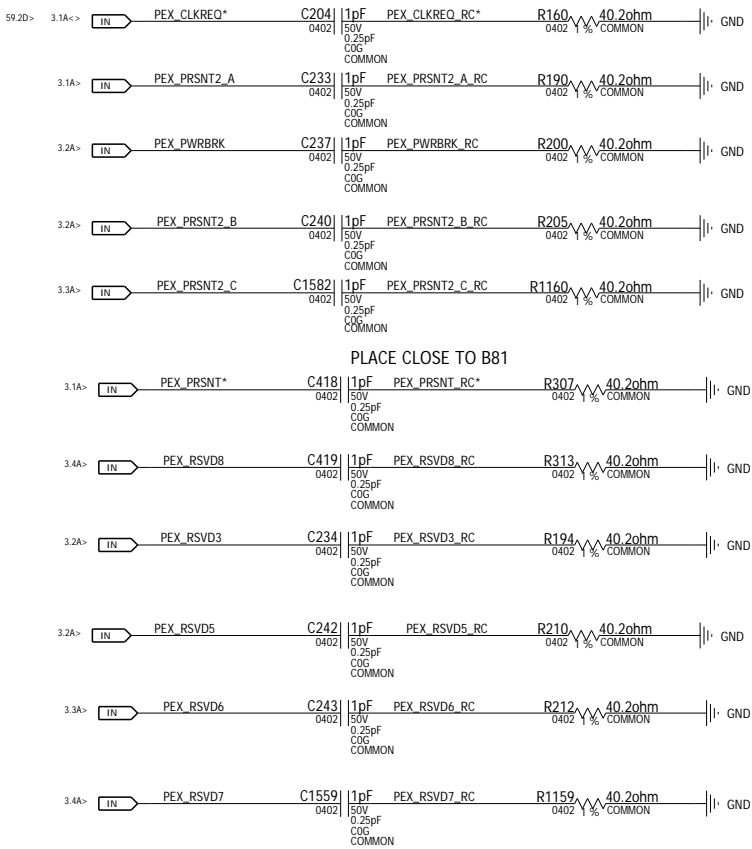
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