P393-A01 Base Design

P393-A01, G92, 8Mx32/16Mx32 GDDR3 (800/1000 MHz), DVI-I-DL, DVI-I-DL/DisplayPort, HDTVout/Stereo

Table of Contents:

1.V117-0C Base on P393
2.page 2 del Q1209,R1219,R58,R55, circuit ,del net pex_rst link page27
3.page 10 del I2CA_SCR_R,I2CA_SDA_R link net Page 27
4.page 11 del I2CB_SCR_R,I2CB_SDA_R link net page27
5.page 15 del Display port circuit
6.page 16 del I2CS for Hybrid power circuit , del GPIO 4/10 net, R91 link gnd, del R66,R75
7.page 14 del MIOB_D2/3/4/5/6/7/10 net link page 19
8.page 20 del DP_POWER circuit
9.page 27 del Hybrid power circuit
10.page 3/5/6. update FBA_CMD(25..0)/FBB_CMD(25..0)
11.page 4/7/8. update FBC_CMD(25..0)/FBD_CMD(25..0)
12.page 17. del GPIO4_FAN_PWM_R net
13.page 17. Del SPDIF circuit , change p403 SPDIF circuit
14.page 12. add EMI

BRD	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10393-base-100	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU_DT_0000	600-10393-0000-100	P393 G92-300 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
2	SKU_DT_0002	600-10393-0002-100	P393 G92-200 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
3	SKU_WS_0500	600-50393-0500-100	P393 G92-875 512MB GDDR3 16Mx32 DVI-I+DP+STEREO
4	SKU_WS_0501	600-50393-0501-100	P393 G92-850 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
5	SKU_DT_0004	600-10393-0004-100	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview

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SUMMARY

Size	Document Number	Rev
Custom	MS-V117	100

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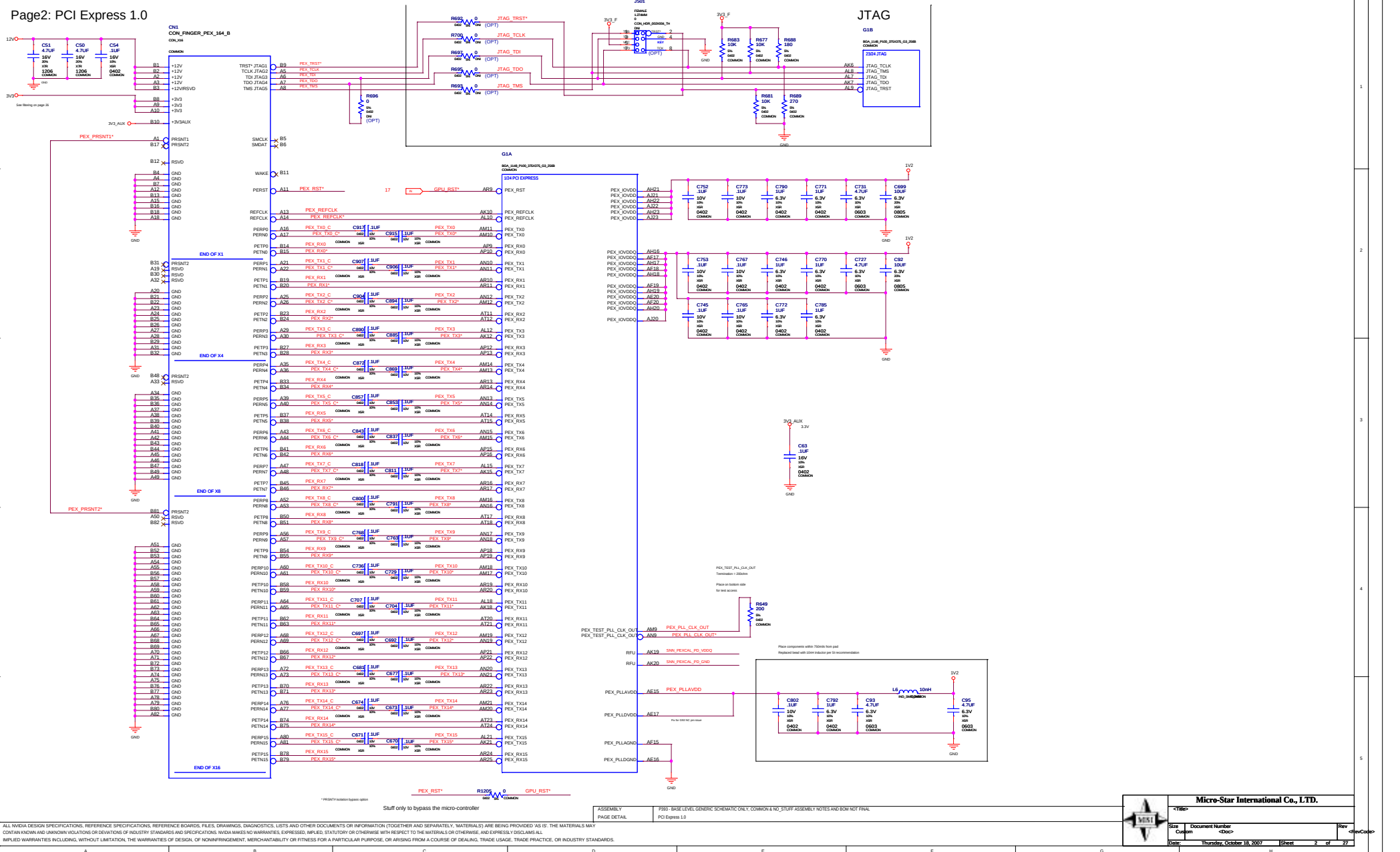
Page2: PCI Express 1.0



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ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express 1.0

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Custom	<Doc>	<RevCode>

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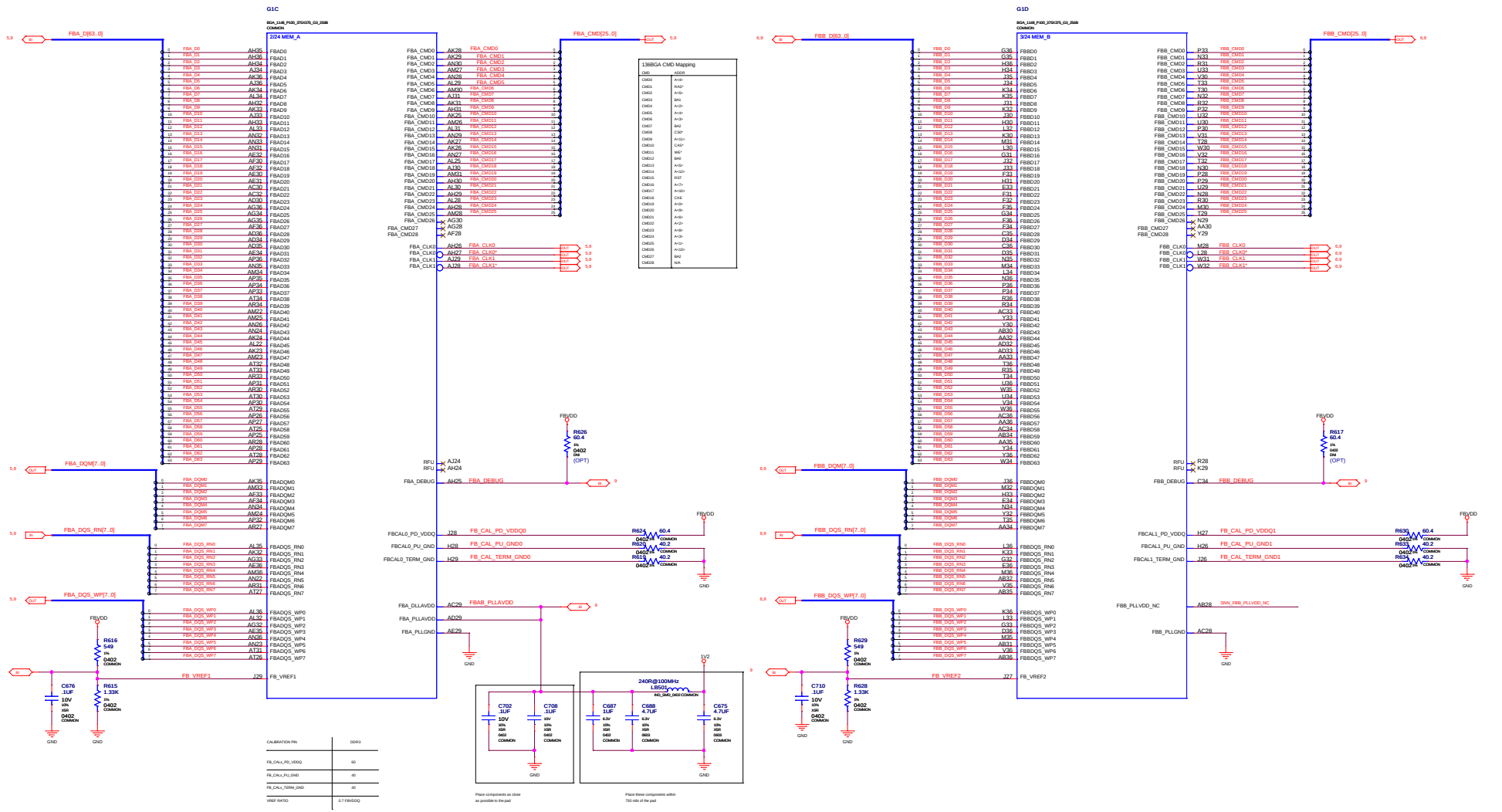
Page3: MEMORY: GPU Partition A/B



CALIBRATION PIN	DDR3
FB_CAL_PD_VDDQ	60
FB_CAL_PU_GND	60
FB_CAL_TERM_GND	60
VREF RATIO	0.7 FBVDDQ

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: GPU Partition A/B

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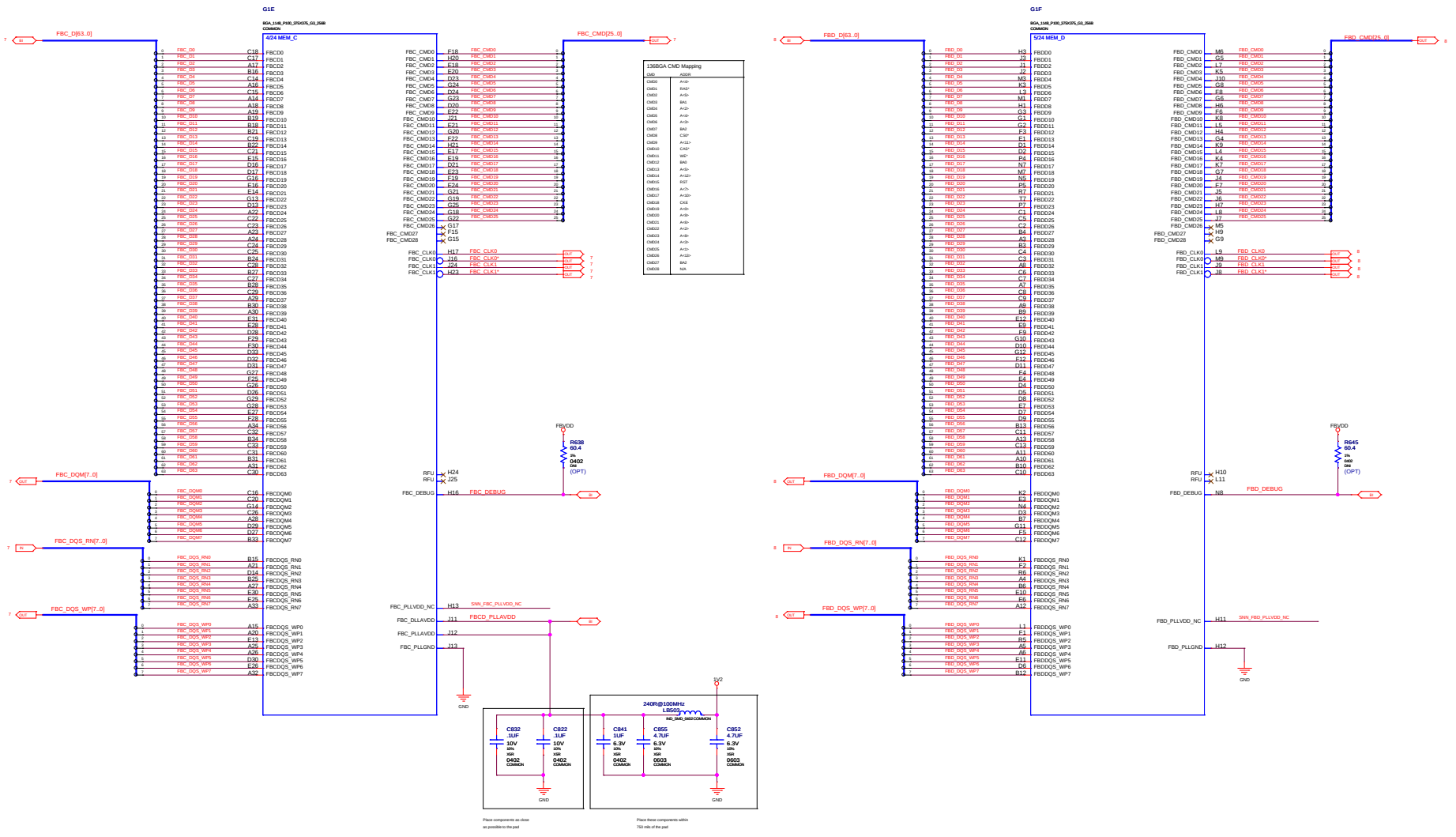
Date: Thursday, October 18, 2007 Sheet 3 of 27

Page4: MEMORY: GPU Partition C/D



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: GPU Partition C/D

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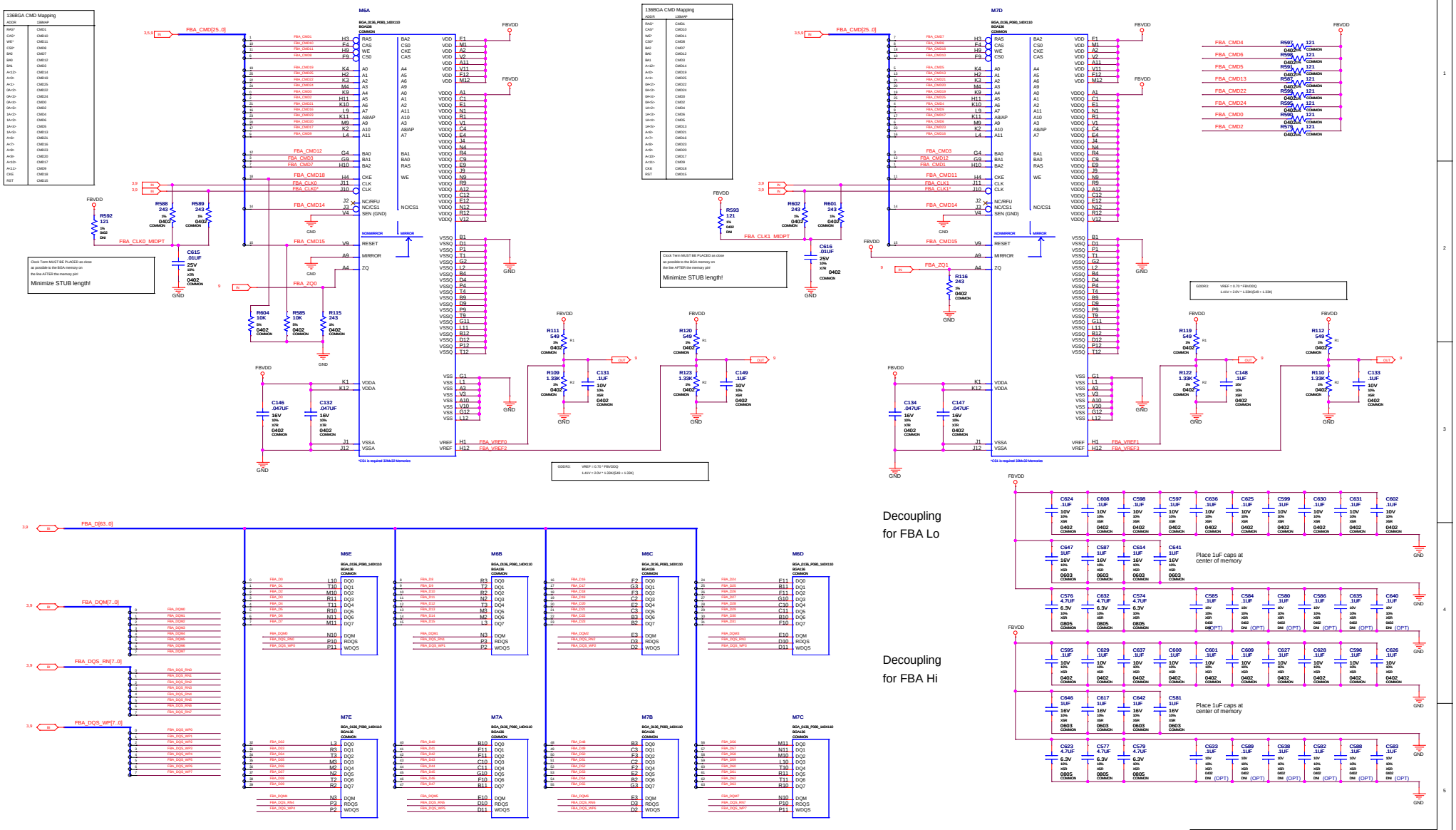
Page5: FBA Partition



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA Partition

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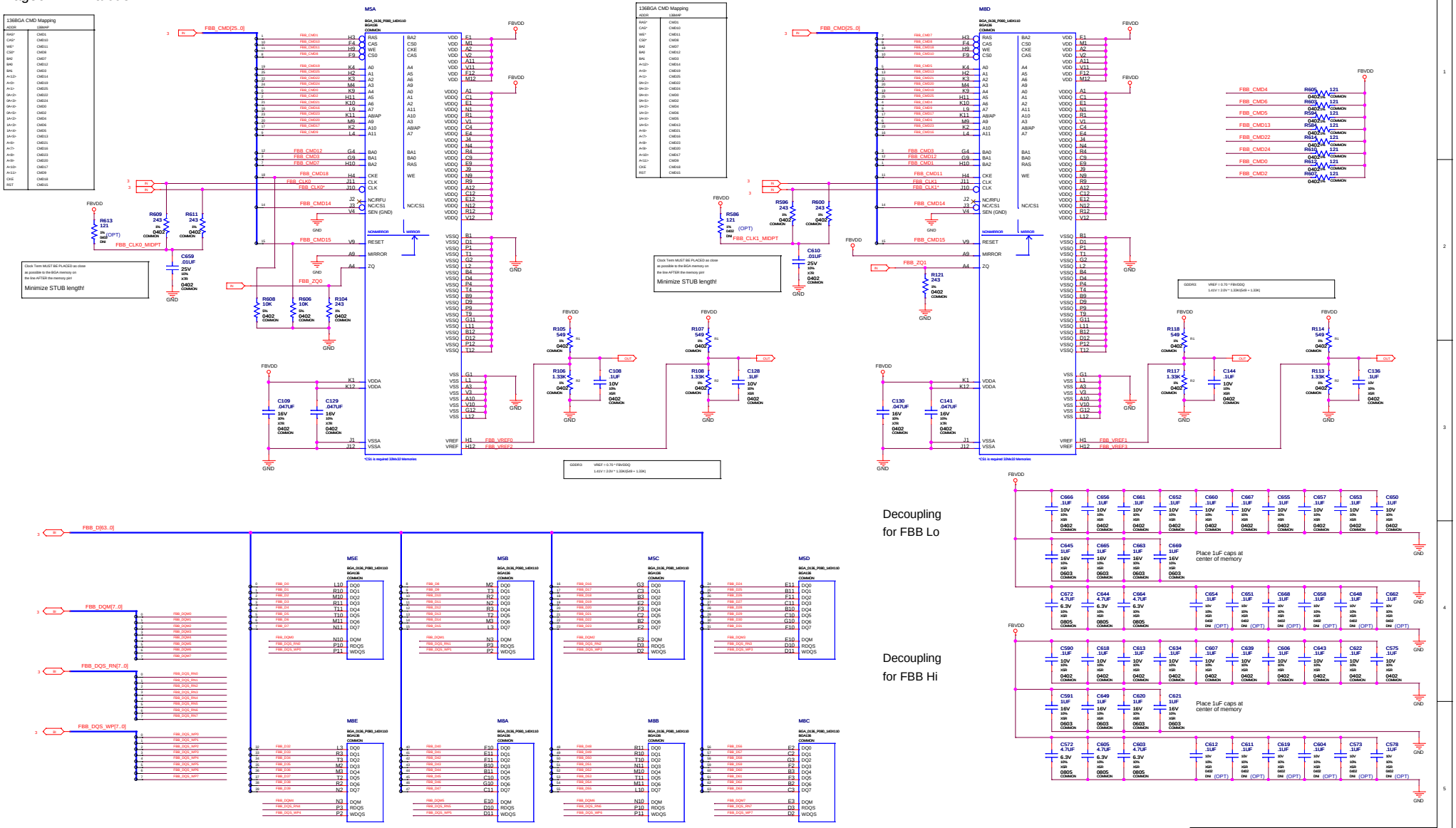
Page6: FBB Partition



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PAGE DETAIL	FBB Partition

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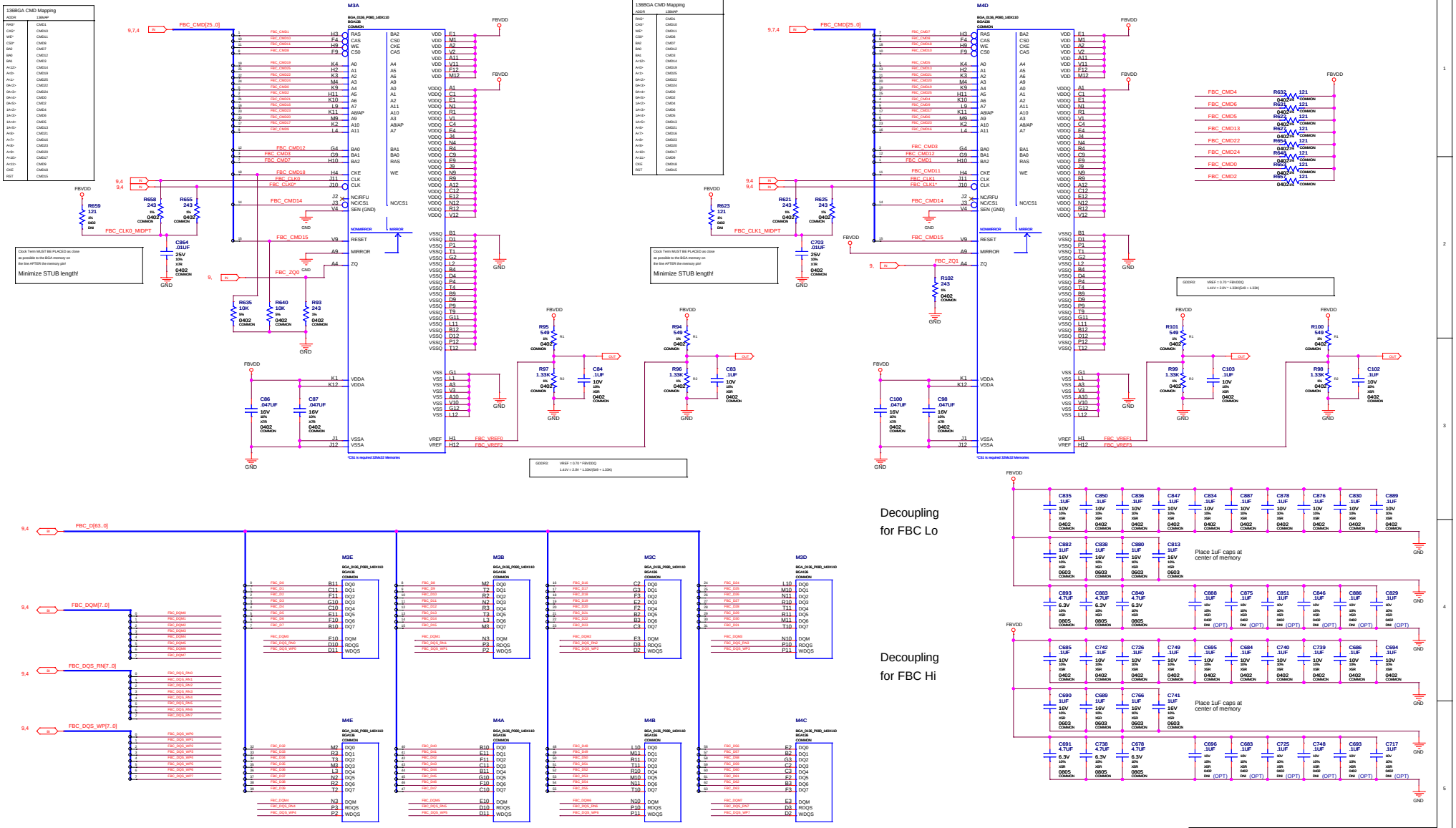
Page7: FBC Partition



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PAGE DETAIL	FBC Partition

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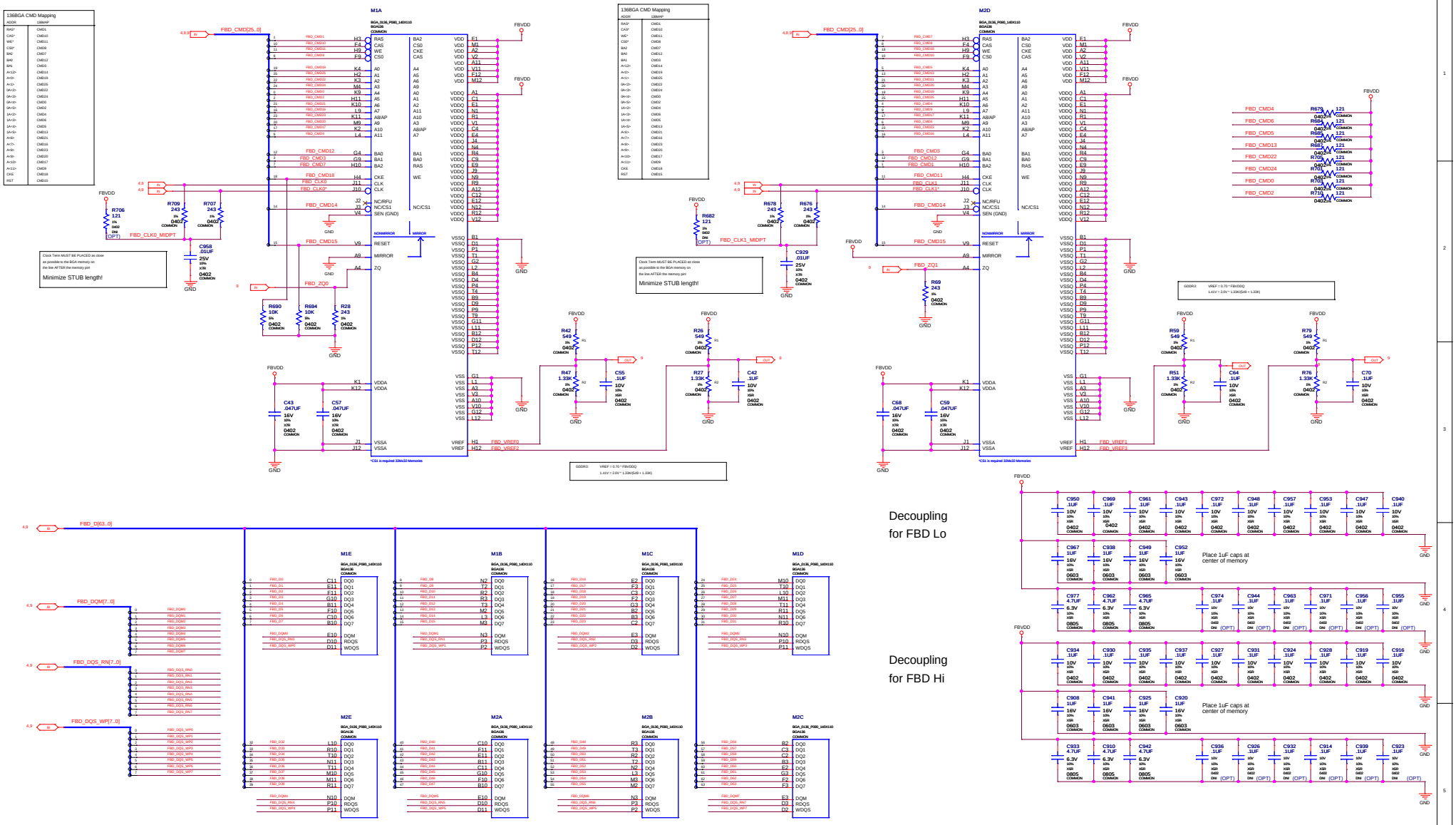
Page8: FBD Partition



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBD Partition

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Page9: FrameBuffer Net Rules

NET RULES for FrameBuffer A/B

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBA_CLK0	1	80OHM	FBA_CLK0
FBA_CLK0*	1	80OHM	FBA_CLK0
FBA_CLK1	1	80OHM	FBA_CLK1
FBA_CLK1*	1	80OHM	FBA_CLK1
FBA_CMD[25..0]	1	40OHM	
FBA_DQ3_WP7_0]	1	40OHM	
FBA_DQ3_RN7_0]	1	40OHM	
FBA_DQM7_0]	1	40OHM	
FBA_DB3_0]	1	40OHM	

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBB_CLK0	1	80OHM	FBB_CLK0
FBB_CLK0*	1	80OHM	FBB_CLK0
FBB_CLK1	1	80OHM	FBB_CLK1
FBB_CLK1*	1	80OHM	FBB_CLK1
FBB_CMD[25..0]	1	40OHM	
FBB_DQ3_WP7_0]	1	40OHM	
FBB_DQ3_RN7_0]	1	40OHM	
FBB_DQM7_0]	1	40OHM	
FBB_DB3_0]	1	40OHM	
FBA_DEBUG	1	40OHM	
FBB_DEBUG	1	40OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBAB_PLLAVDD	1.2V	0.02A	12MIL
FBA_VREF0	1.45V	0.02A	12MIL
FBA_VREF1	1.45V	0.02A	12MIL
FBA_VREF2	1.45V	0.02A	12MIL
FBA_VREF3	1.45V	0.02A	12MIL
FBA_ZQ0	2.0V	0.02A	12MIL
FBA_ZQ1	2.0V	0.02A	12MIL
FBB_VREF0	1.45V	0.02A	12MIL
FBB_VREF1	1.45V	0.02A	12MIL
FBB_VREF2	1.45V	0.02A	12MIL
FBB_VREF3	1.45V	0.02A	12MIL
FBB_ZQ0	2.0V	0.02A	12MIL
FBB_ZQ1	2.0V	0.02A	12MIL
FB_VREF1	1.45V	0.02A	12MIL
FB_VREF2	1.45V	0.02A	12MIL

NET RULES for FrameBuffer C/D

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBC_CLK0	1	80OHM	FBC_CLK0
FBC_CLK0*	1	80OHM	FBC_CLK0
FBC_CLK1	1	80OHM	FBC_CLK1
FBC_CLK1*	1	80OHM	FBC_CLK1
FBC_CMD[25..0]	1	40OHM	
FBC_DQ3_WP7_0]	1	40OHM	
FBC_DQ3_RN7_0]	1	40OHM	
FBC_DQM7_0]	1	40OHM	
FBC_DB3_0]	1	40OHM	

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBD_CLK0	1	80OHM	FBD_CLK0
FBD_CLK0*	1	80OHM	FBD_CLK0
FBD_CLK1	1	80OHM	FBD_CLK1
FBD_CLK1*	1	80OHM	FBD_CLK1
FBD_CMD[25..0]	1	40OHM	
FBD_DQ3_WP7_0]	1	40OHM	
FBD_DQ3_RN7_0]	1	40OHM	
FBD_DQM7_0]	1	40OHM	
FBD_DB3_0]	1	40OHM	
FBC_DEBUG	1	40OHM	
FBD_DEBUG	1	40OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBCD_PLLAVDD	1.2V	0.02A	12MIL
FBC_VREF0	1.45V	0.02A	12MIL
FBC_VREF1	1.45V	0.02A	12MIL
FBC_VREF2	1.45V	0.02A	12MIL
FBC_VREF3	1.45V	0.02A	12MIL
FBC_ZQ0	2.0V	0.02A	12MIL
FBC_ZQ1	2.0V	0.02A	12MIL
FBD_VREF0	1.45V	0.02A	12MIL
FBD_VREF1	1.45V	0.02A	12MIL
FBD_VREF2	1.45V	0.02A	12MIL
FBD_VREF3	1.45V	0.02A	12MIL
FBD_ZQ0	2.0V	0.02A	12MIL
FBD_ZQ1	2.0V	0.02A	12MIL

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FrameBuffer Net Rules

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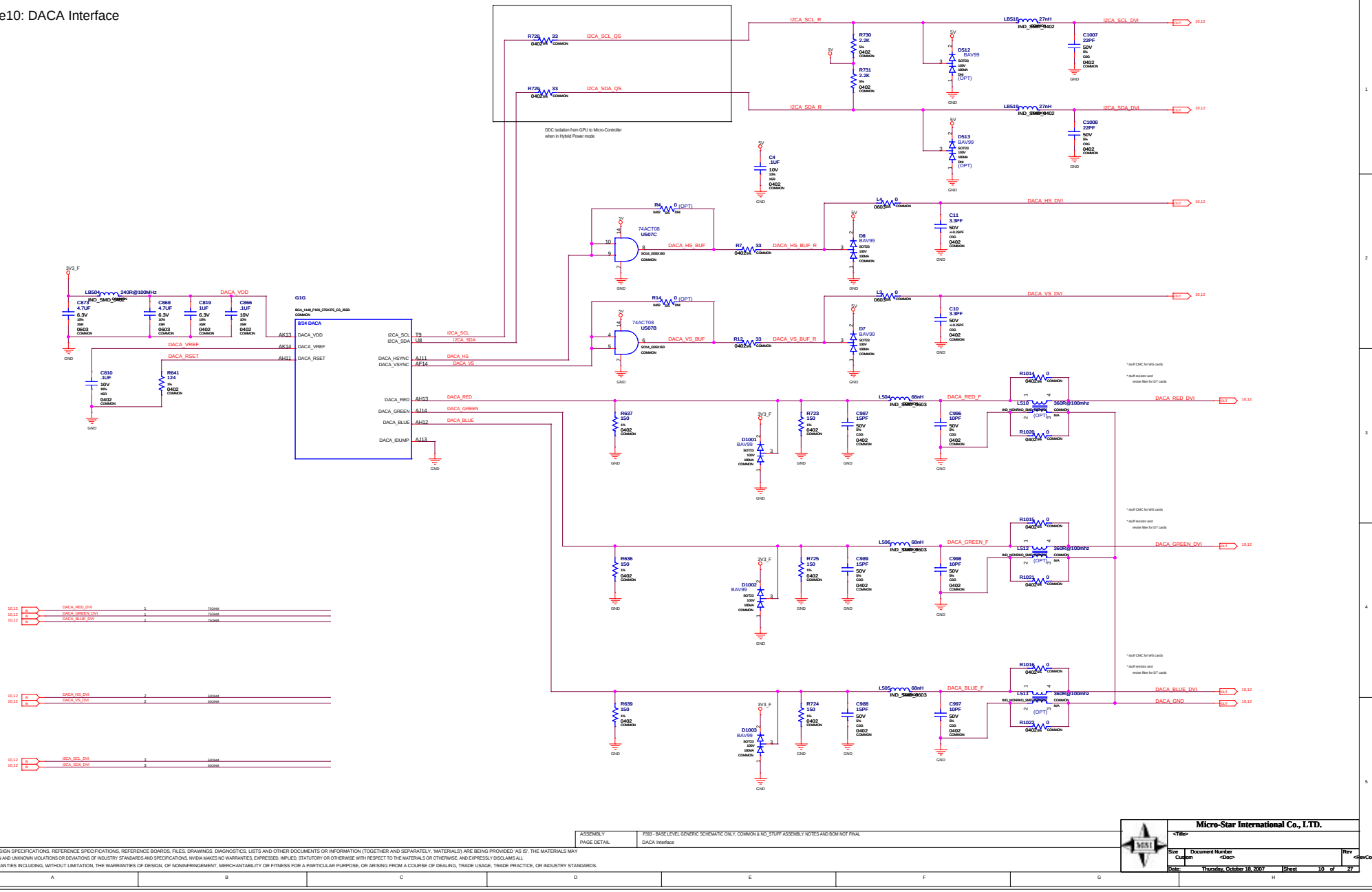
Page10: DACA Interface



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA Interface

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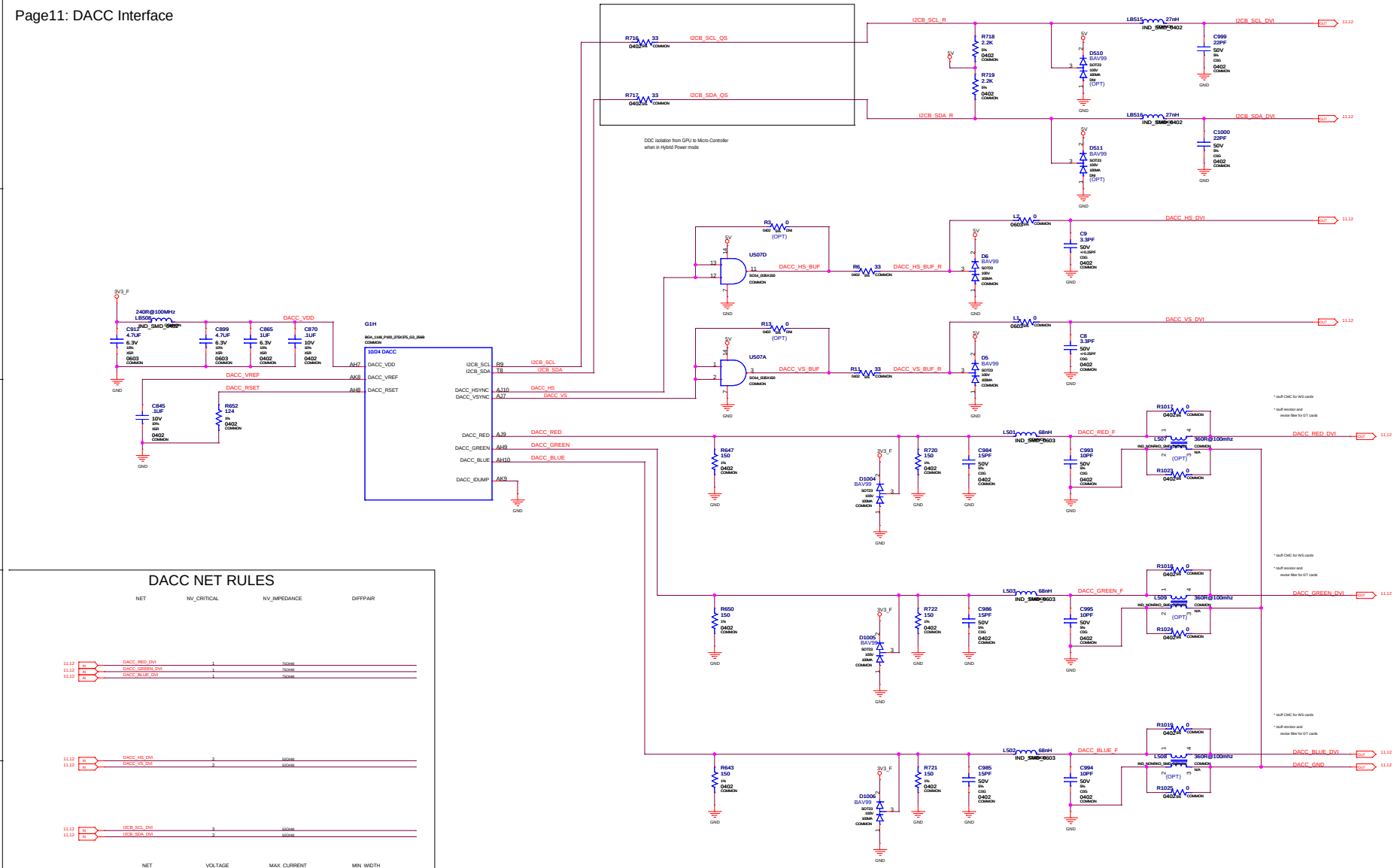
Page11: DACC Interface



DACC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACC_RED_DVI		75OHM	
DACC_GREEN_DVI		75OHM	
DACC_BLUE_DVI		75OHM	
DACC_HS_DVI		50OHM	
DACC_VS_DVI		50OHM	
I2CB_SCL_DVI		50OHM	
I2CB_SDA_DVI		50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC Interface

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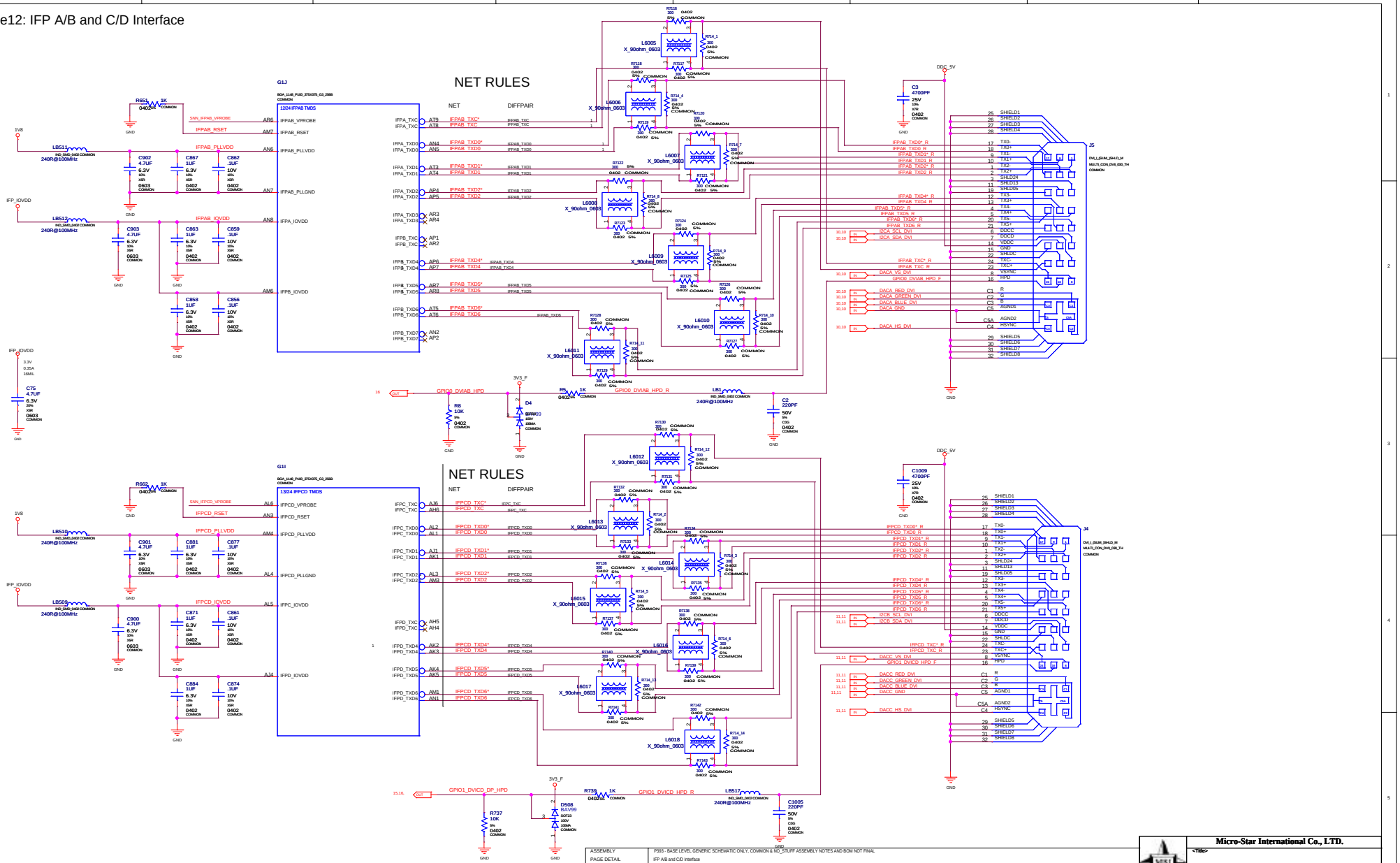
Page12: IFP A/B and C/D Interface

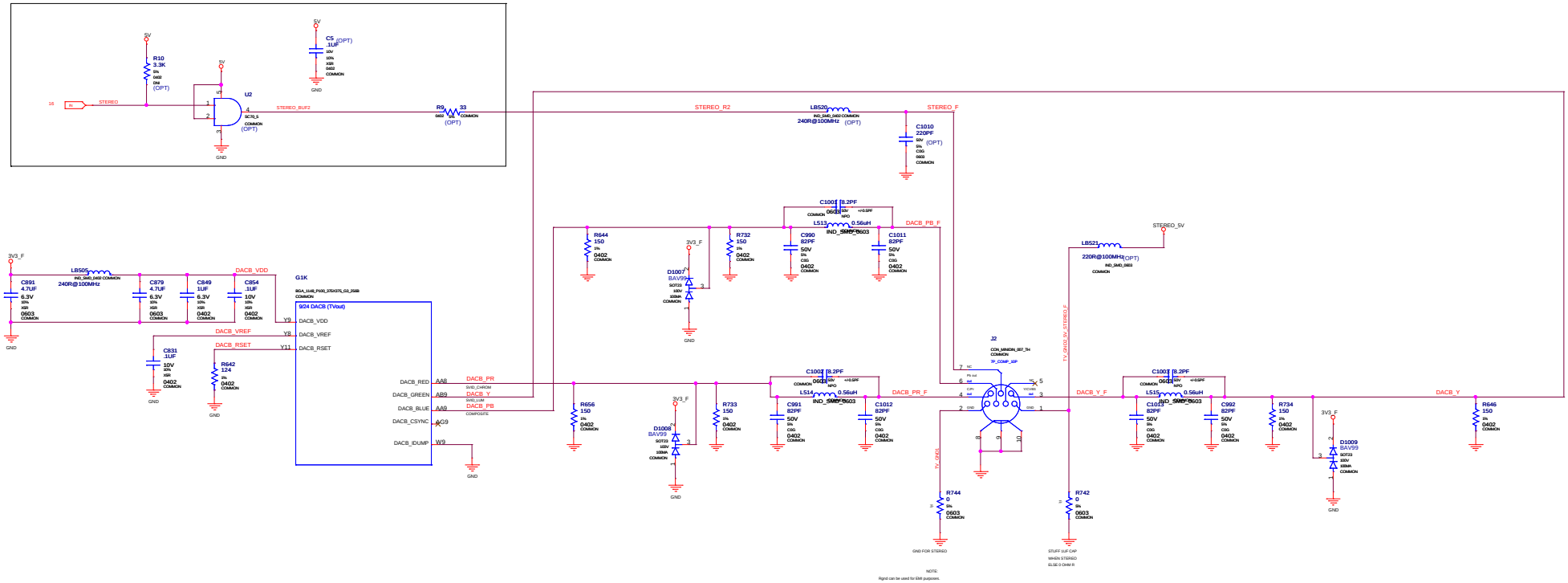


Page13: DACB and Stereo Interface

DACB,STEREO, FL NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR

Stereo



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB and Stereo Interface

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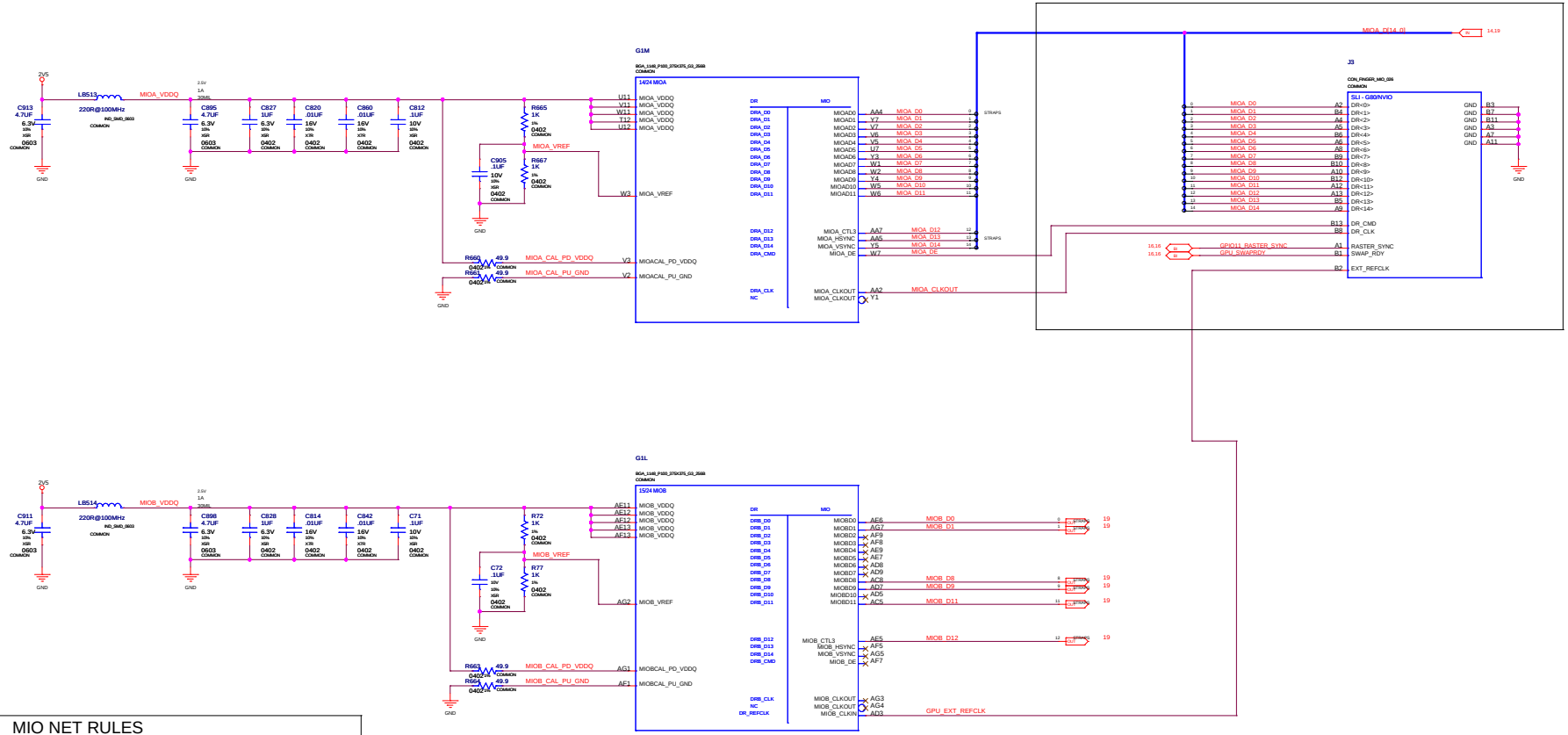
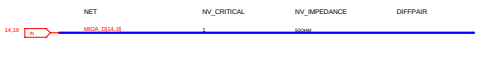
Page14: Multi-use IO(MIO) Interface

MIO Feature Connector



MIO NET RULES



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Multi-use IO(MIO) Interface

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Page15: Display Port (Analogix ANX9802/ANX9805)

* I2C keeper circuit removed

* ANX9805 support

pin 76 - GPIO3 to DP mode, from pin 13, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 74 - GPIO2, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 73 - CEC support via FET and pull-up, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 71 - SPDIF1 - tie to GND, input select 0/1 through internal register

pin 70 - SPDIF0 - support for Audio input, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 68 - NC - tie to GND

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display Port

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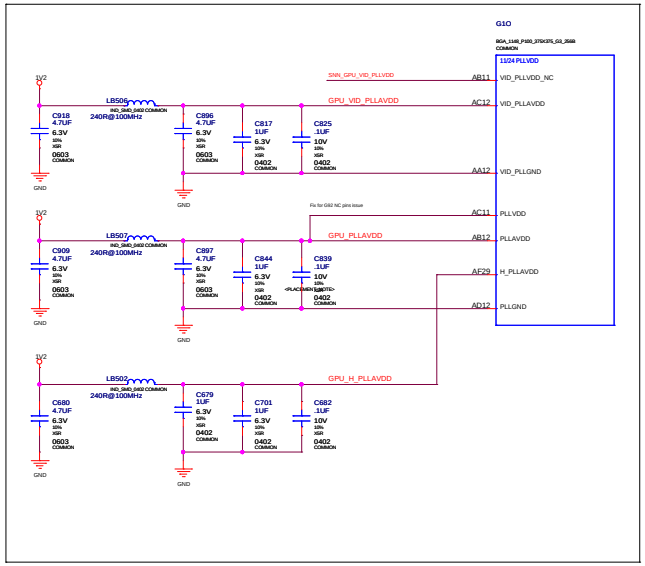
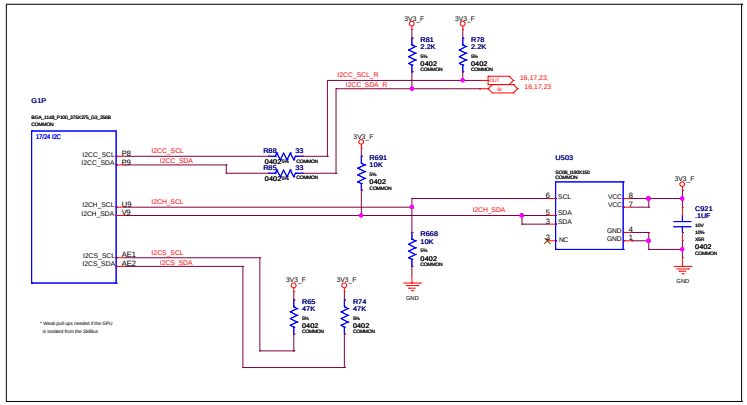
Page16: MISC: GPIO, I2C, BIOS, PLL, and XTAL

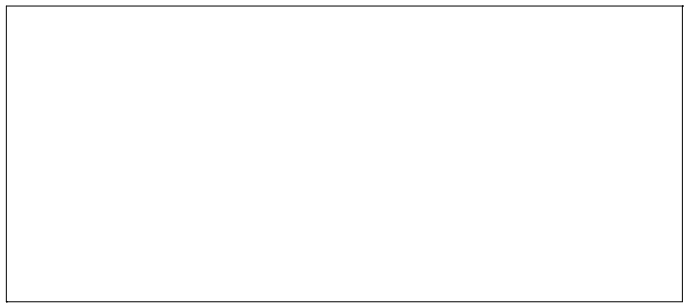
PLLVDD/VID_PLLVDD



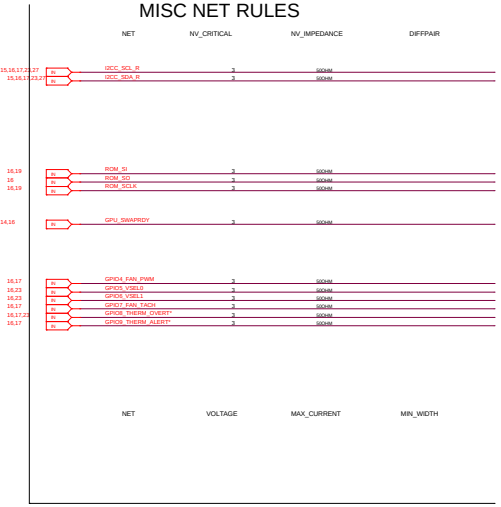
I2CC / I2CH(+ HDCP ROM) / I2CS



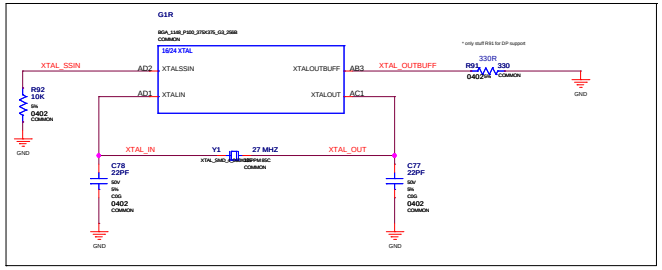
I2CS isolation for Hybrid Power



MISC NET RULES

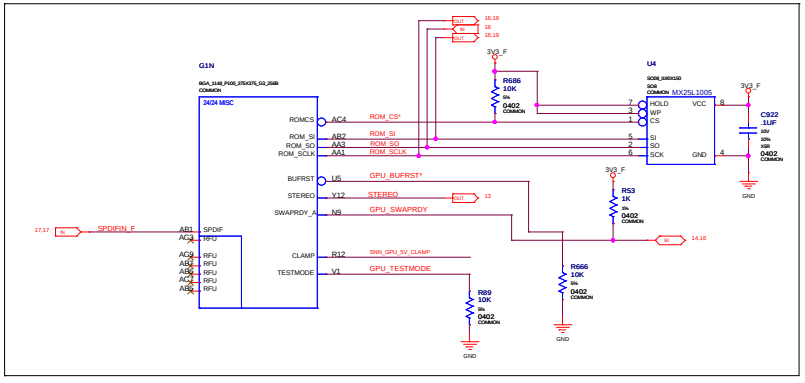


XTAL

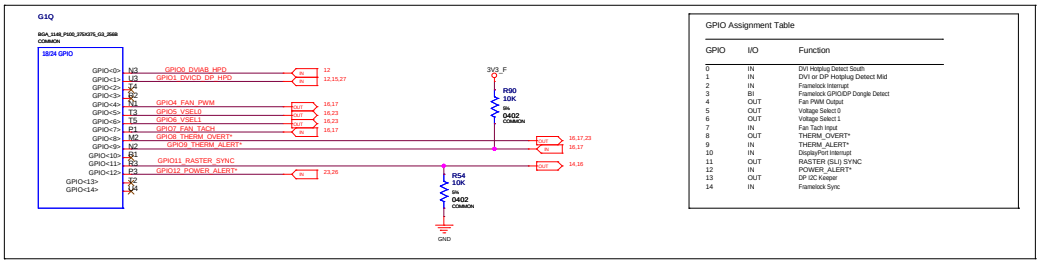


ROM / MISC

(BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)



GPIO



GPIO Assignment Table

GPIO	I/O	Function
0	IN	DVI Hotplug Detect South
1	IN	DVI or DP Hotplug Detect Mid
2	IN	Framelock Interrupt
3	BI	Framelock GPIO/DP Dongle Detect
4	OUT	Fan PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fan Tach Input
8	OUT	THERM_OVERT*
9	IN	THERM_ALERT*
10	IN	DisplayPort Interrupt
11	OUT	RASTER (SLI) SYNC
12	IN	POWER_ALERT*
13	OUT	DP I2C Keeper
14	IN	Framelock Sync

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO, I2C, BIOS, PLL, and XTAL

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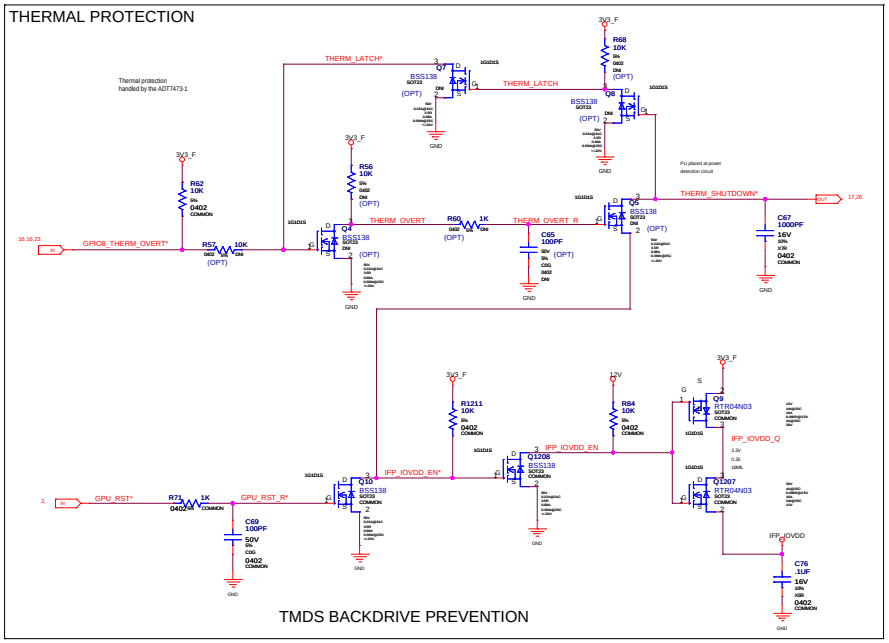
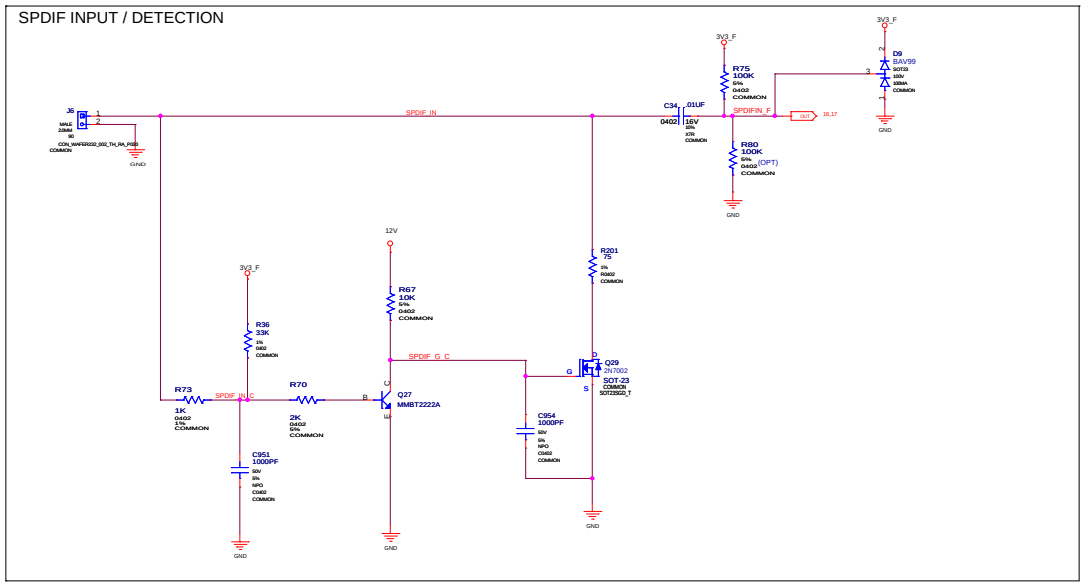
Page17: Thermal Control/Protection and SPDIF Input

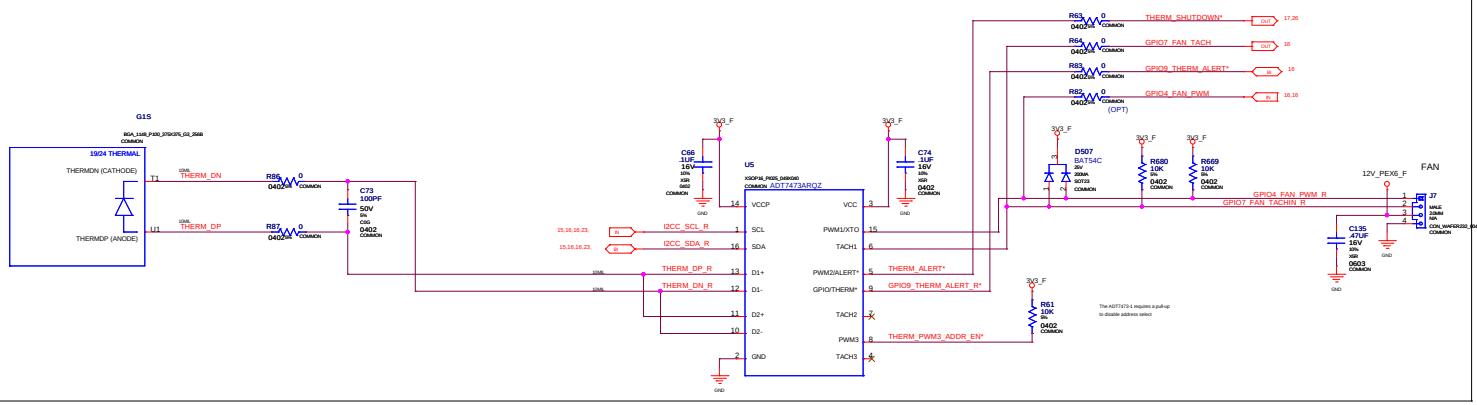
THERMAL PROTECTION



SPDIF INPUT / DETECTION



THERMAL CONTROL



The FAN connector needs to move as follows for mechanical / ID support:

* move -43mils in Y
* move +33mils in X

NET	IMPEDANCE	NV_CRITICAL_NET	MIN_LINE_WIDTH
SPDIFIN_F	SE/HIM		

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Control/Protection and SPDIF Input

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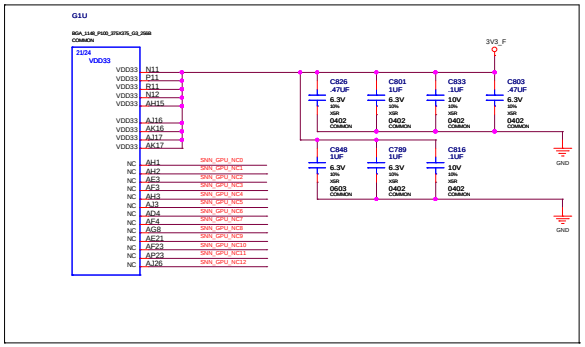
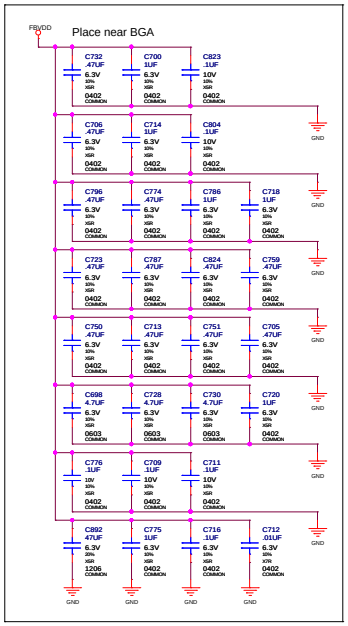
Page18: Power/GND and Decoupling

VDD33

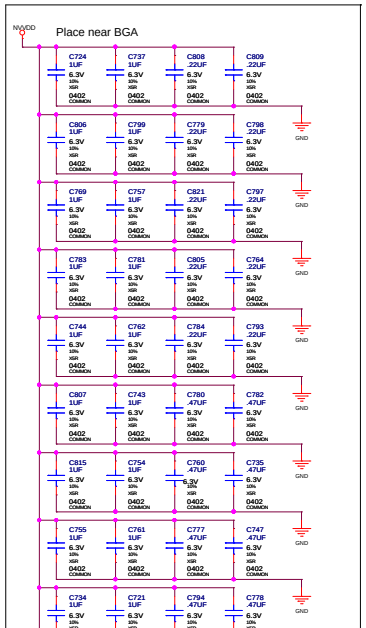


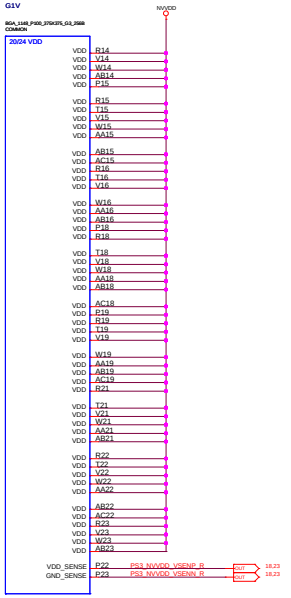
FBVTT

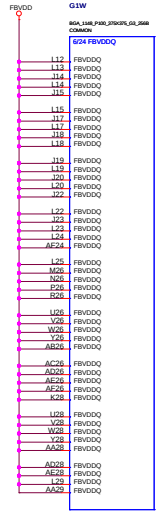
FBVDDQ

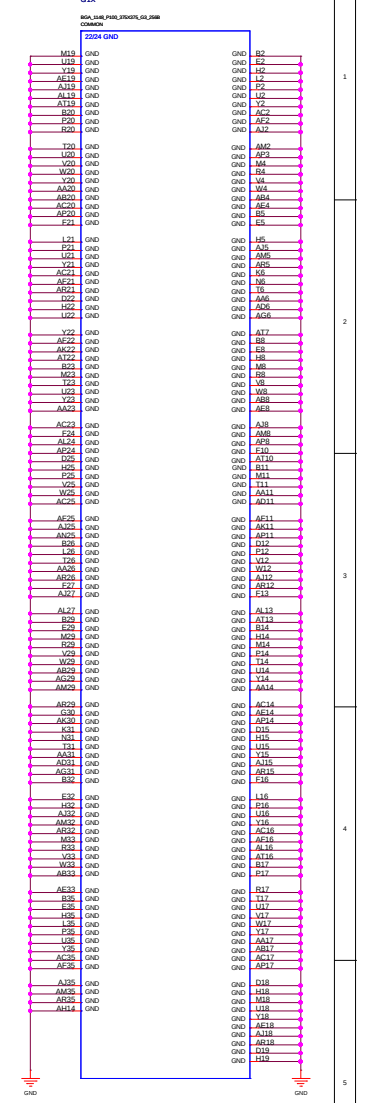


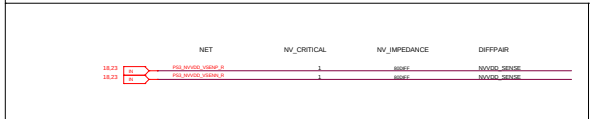
NVVDD











ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power/GND and Decoupling

Micro-Star International Co., LTD.

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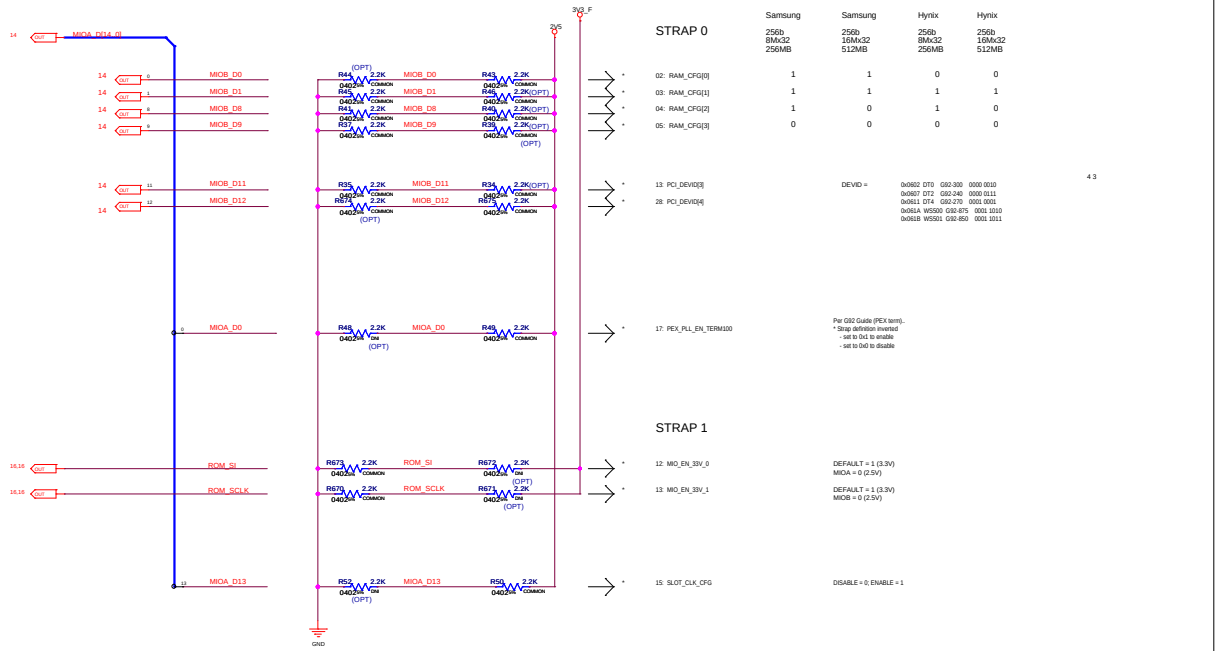
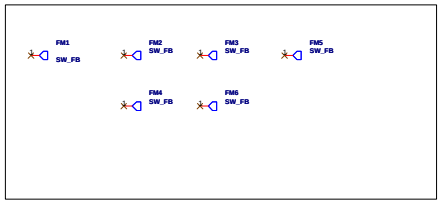
Page19: Configuration Straps and Mechanical

STRAPS

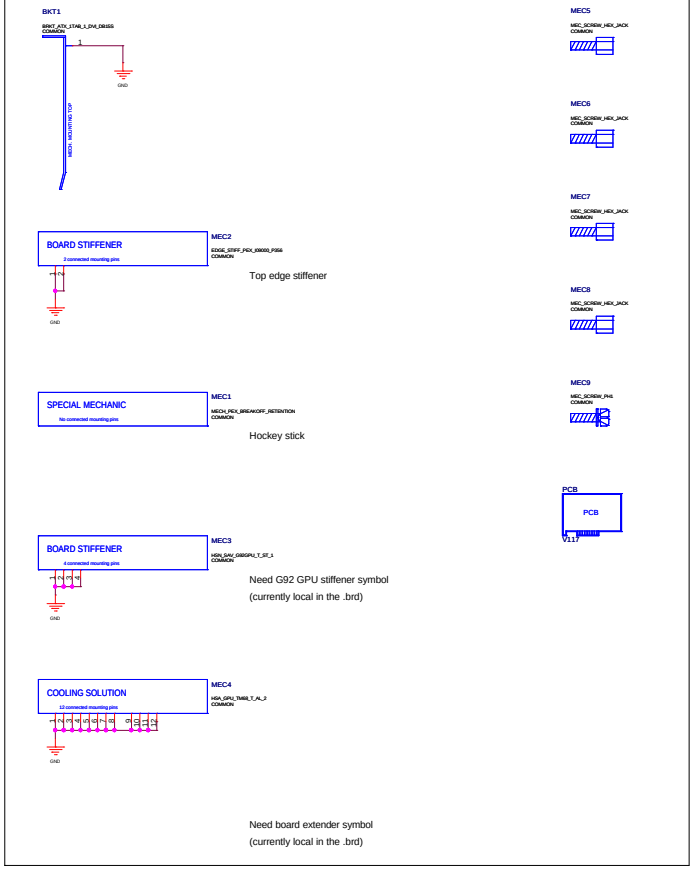


	Samsung	Samsung	Hynix	Hynix
STRAP 0	256b 8Mx32 256MB	256b 16Mx32 512MB	256b 8Mx32 256MB	256b 16Mx32 512MB
02: RAM_CFG[0]	1	1	0	0
03: RAM_CFG[1]	1	1	1	1
04: RAM_CFG[2]	1	0	1	0
05: RAM_CFG[3]	0	0	0	0

DEVID =			
0x0602	DT0	G92-300	0000 0010
0x0607	DT2	G92-240	0000 0111
0x0611	DT4	G92-270	0000 0001
0x061A	WS500	G92-875	0001 1010
0x061B	WS501	G92-850	0001 1011



MECHANICAL



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Configuration Straps and Mechanical

Micro-Star International Co., LTD.

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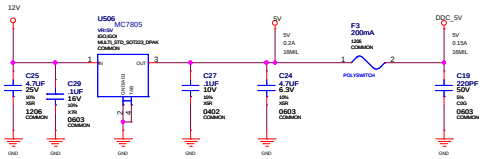
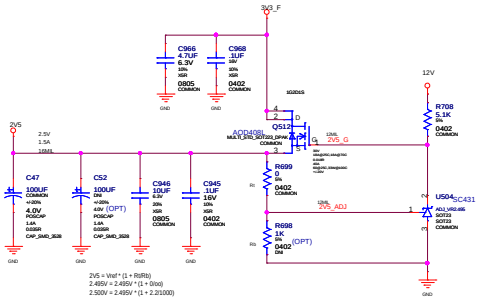
Page20: Power Supply: 5V, STEREO_5V, 2V5,

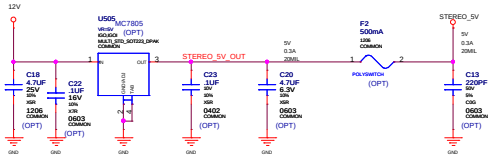
5V and DDC5V Supply



2V5 Supply



5V STEREO Supply



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 5V, STEREO_5V, 2V5, DP_PWR

Micro-Star International Co., LTD.

<Title>

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Custom	<Doc>	<RevCode>

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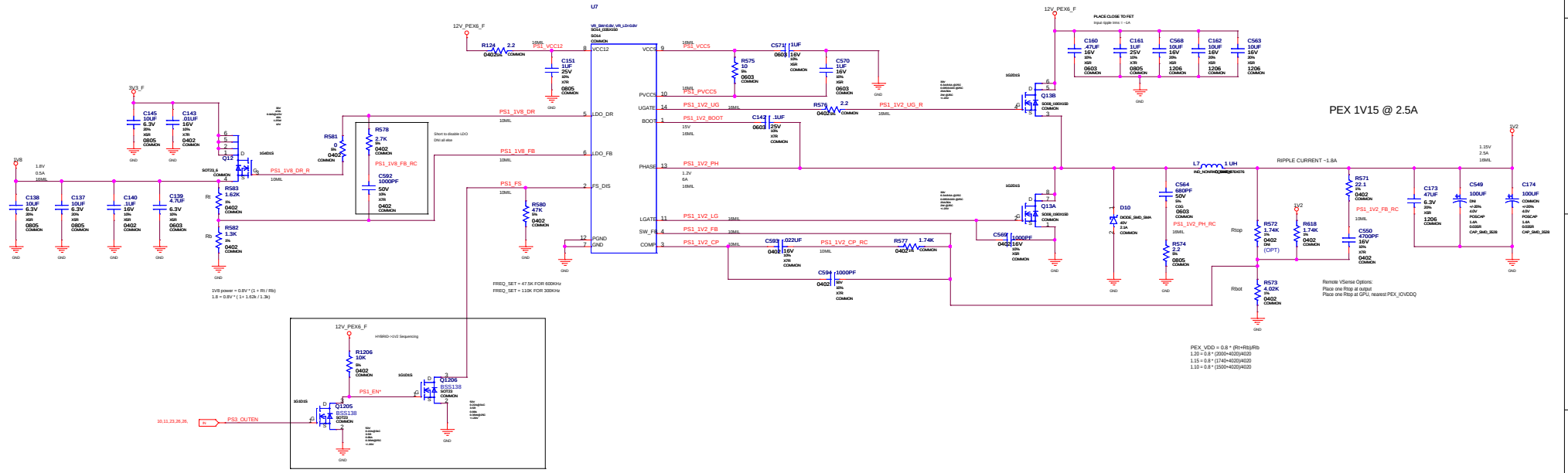
Page21: Power Supply: 1V2, 1V8



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 1V2, 1V8

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<Title>			
Size: Custom	Document Number: <Doc>	Rev: <RevCode>	
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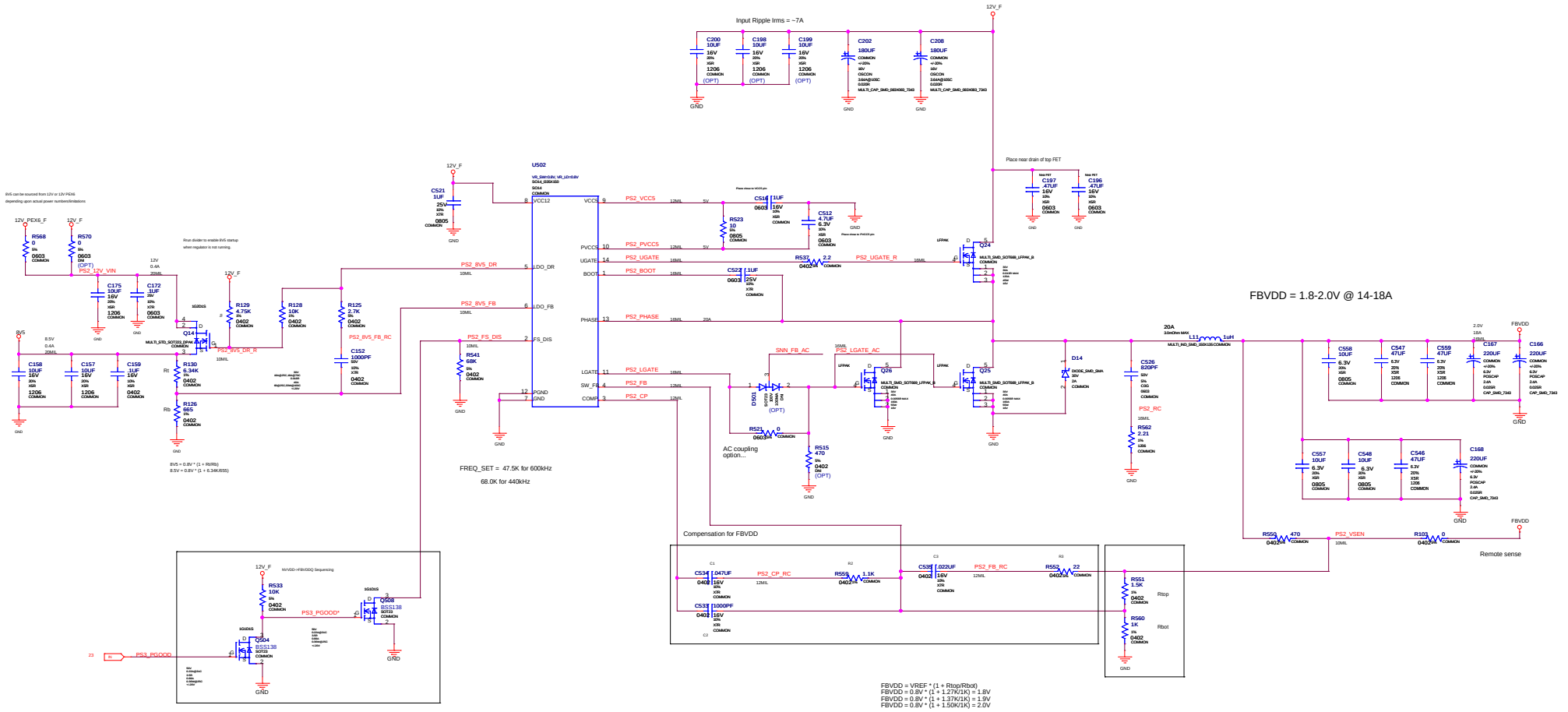
Page22: Combined FBVDD/VDDQ, 8V5



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: FBVDDQ, 8V5

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<Title>			
Size: Custom	Document Number: <Doc>	Rev: <RevCode>	
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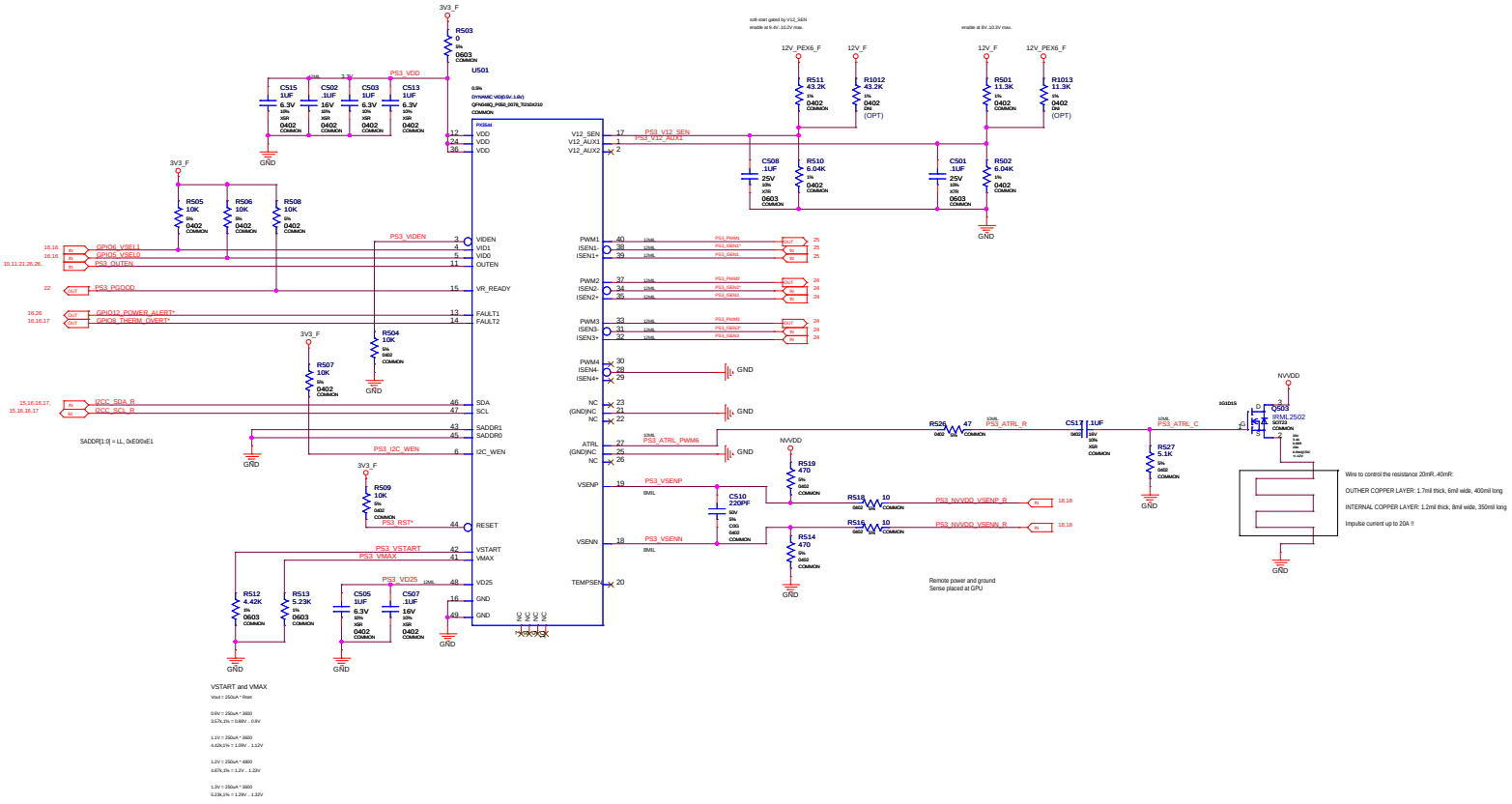
Page23: Power Supply: NVVDD Regulator



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Regulator

Micro-Star International Co., LTD.

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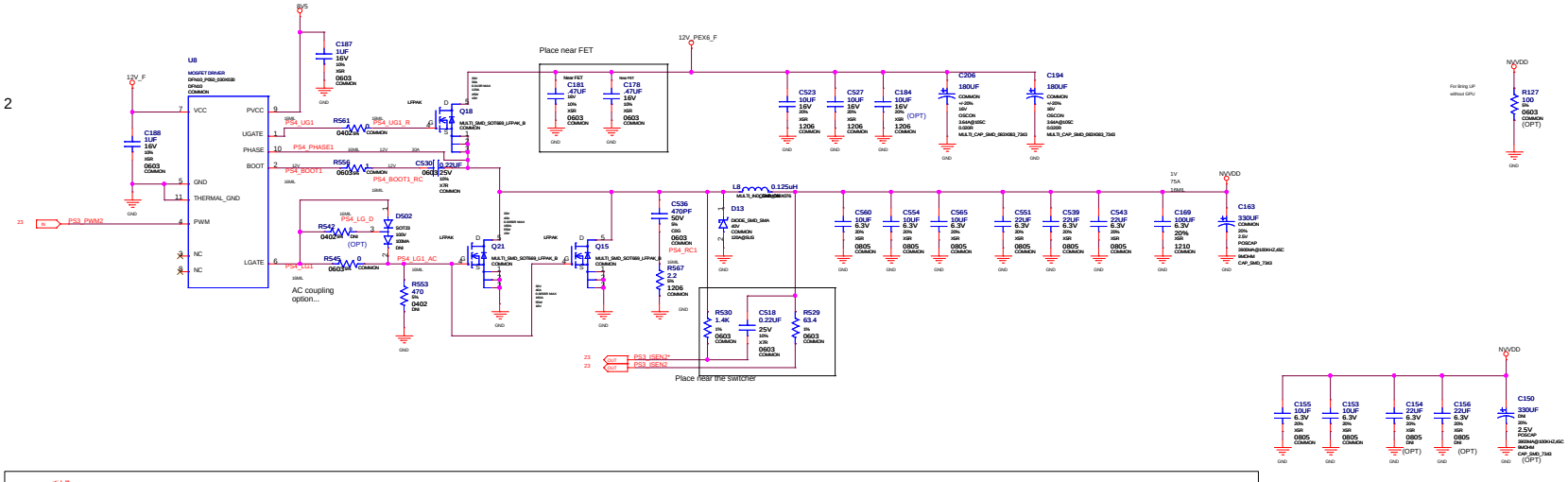
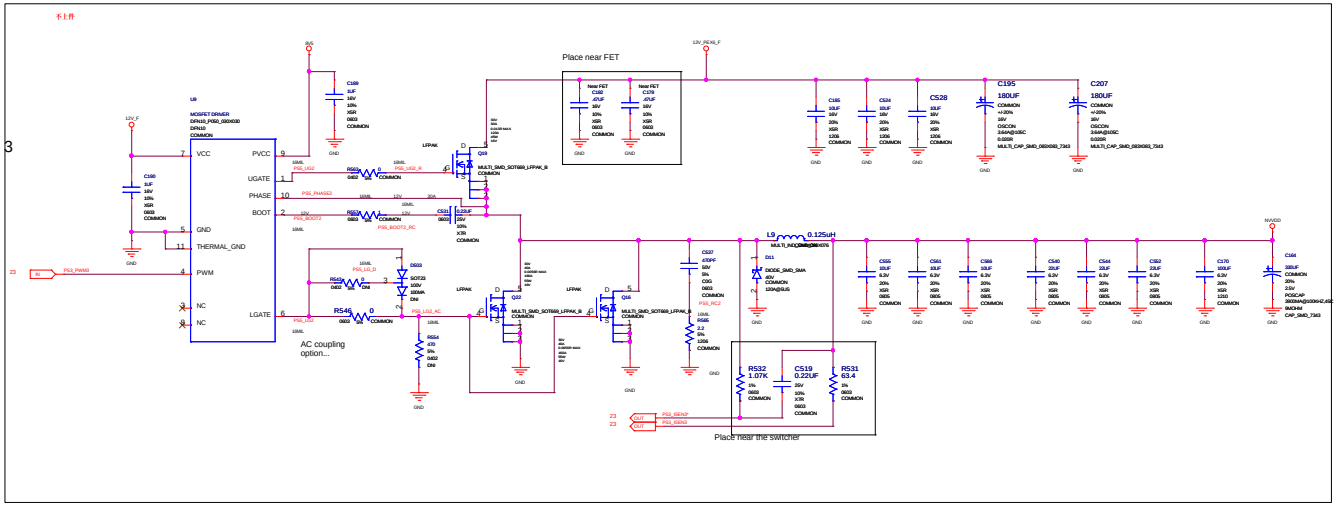
Page24: Power Supply: NVVDD Phase 2, 3

PHASE 2



PHASE 3



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 1 & 2

Micro-Star International Co., LTD.

<Title>

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Custom	<Doc>	<RevCode>

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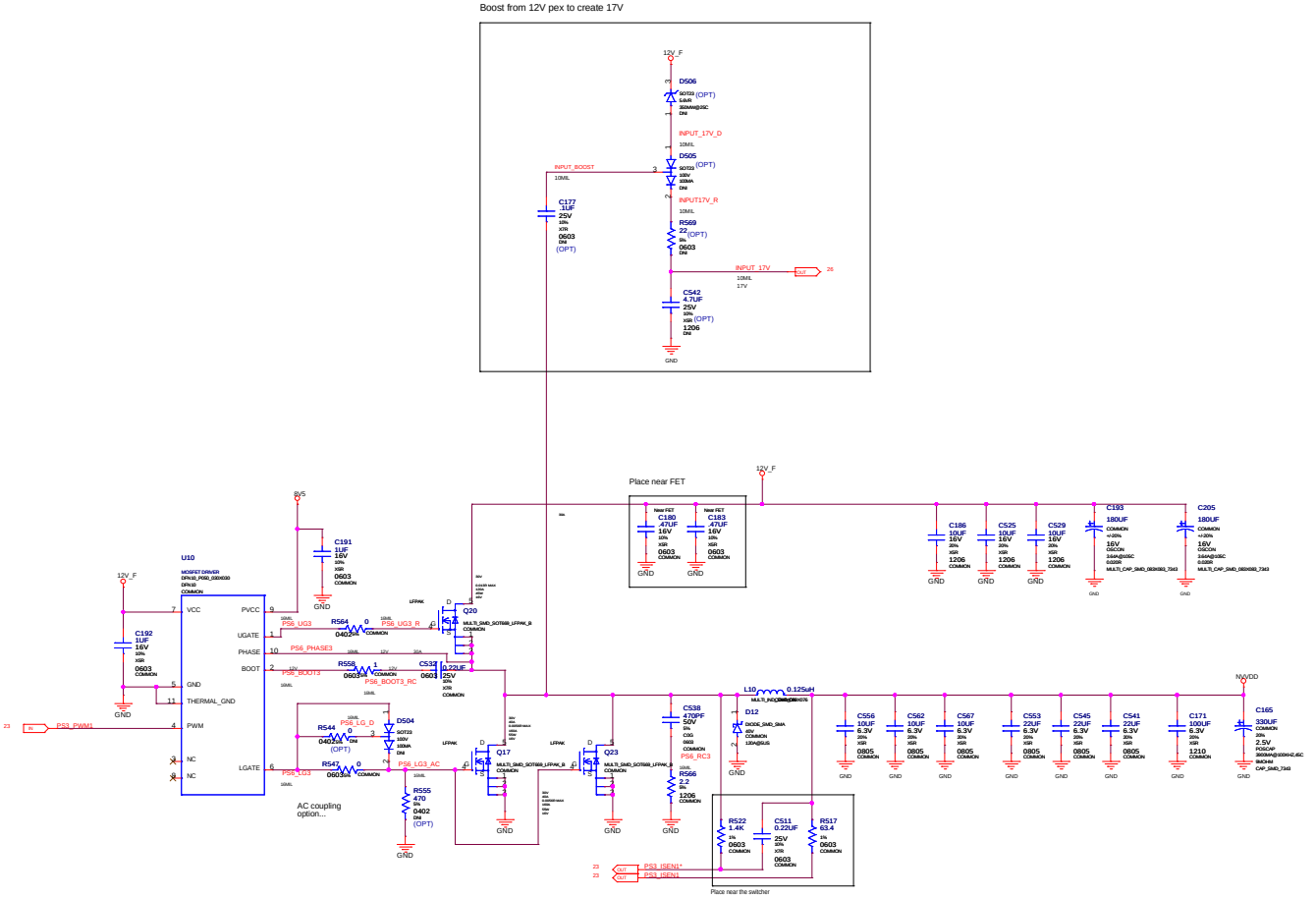
Page25: Power Supply: NVVDD Phase 1

PHASE 1



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 3

Micro-Star International Co., LTD.

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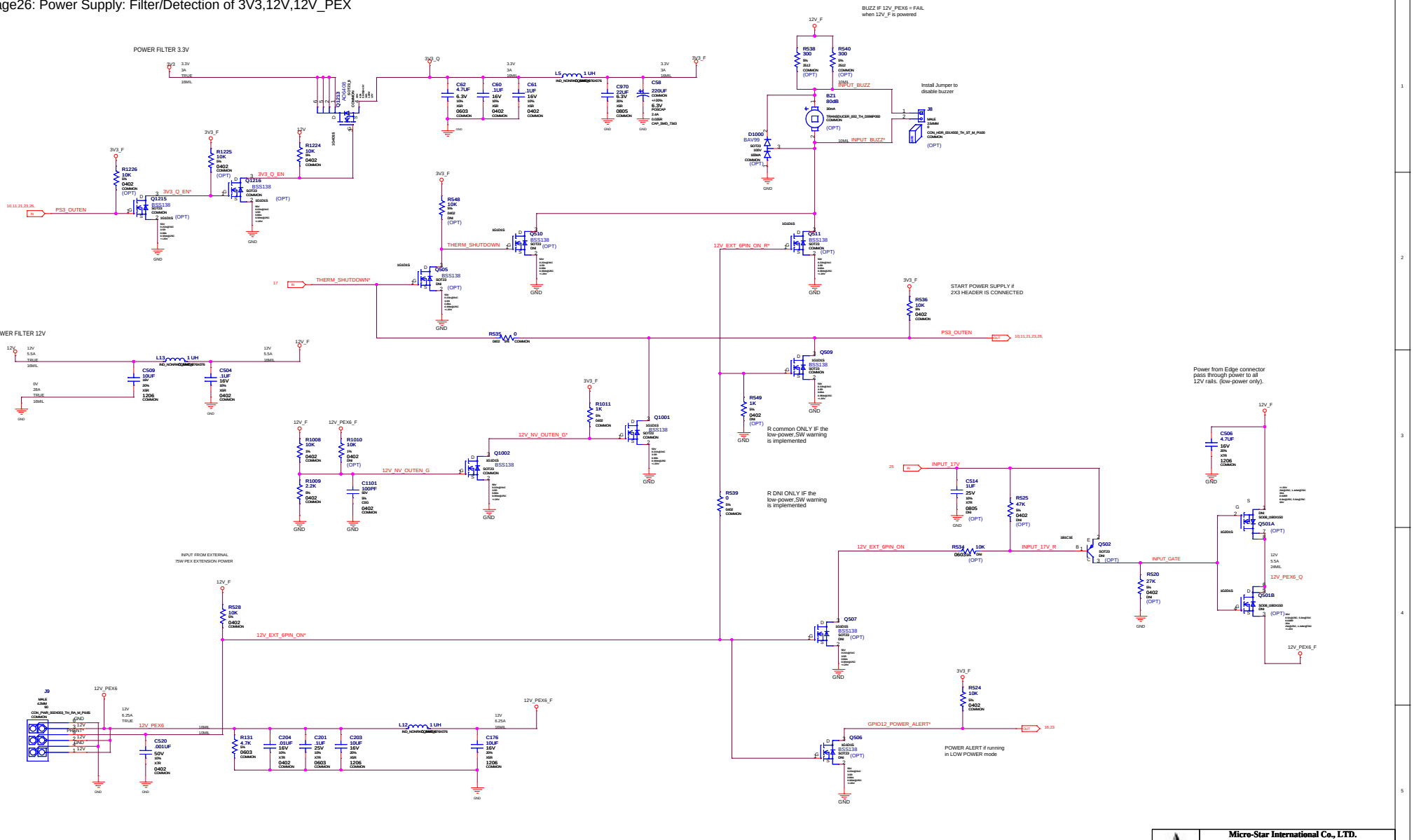
Page26: Power Supply: Filter/Detection of 3V3,12V,12V_PEX



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: Filter/Detection of 3V3, 12V, 12V_PEX6

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<Title>			
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Page27: Power Supply: Hybrid Power

Weak pull-ups needed for I2CS:

* if SMBus is isolated from the GPU
* if MB does not support SMBus
* if MB does not support 3V3AUX

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: Hybrid Power

Micro-Star International Co., LTD.

<Title>

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