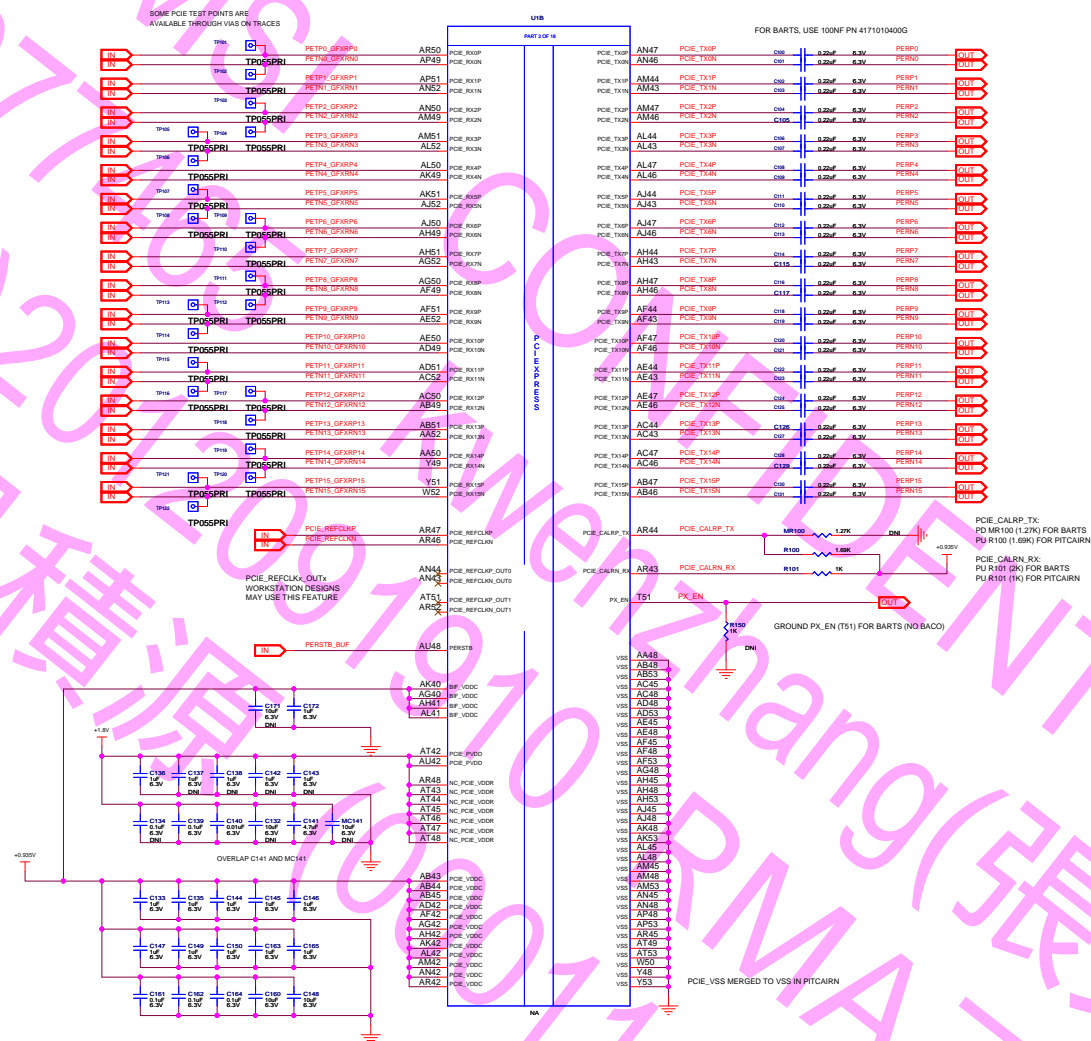
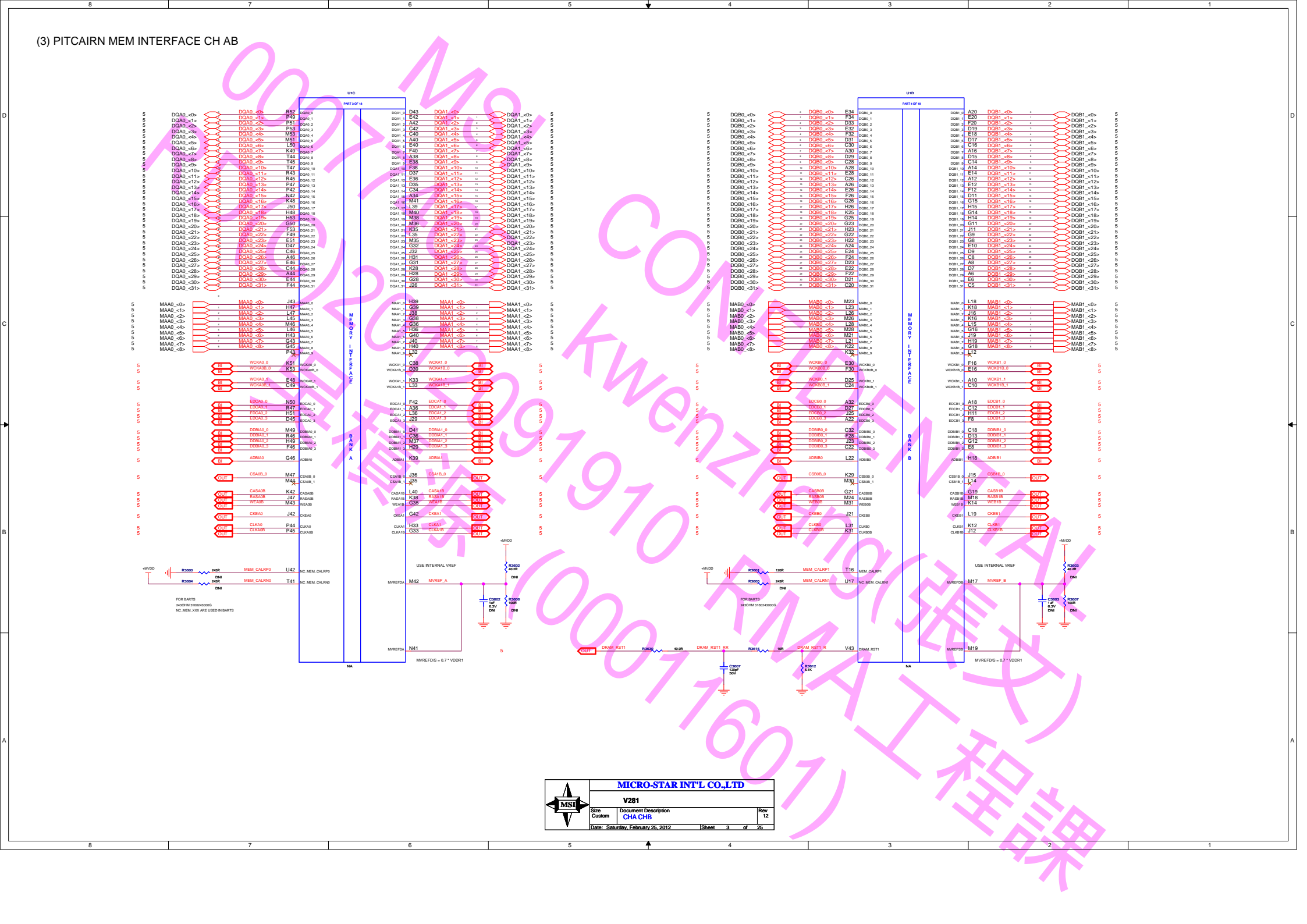


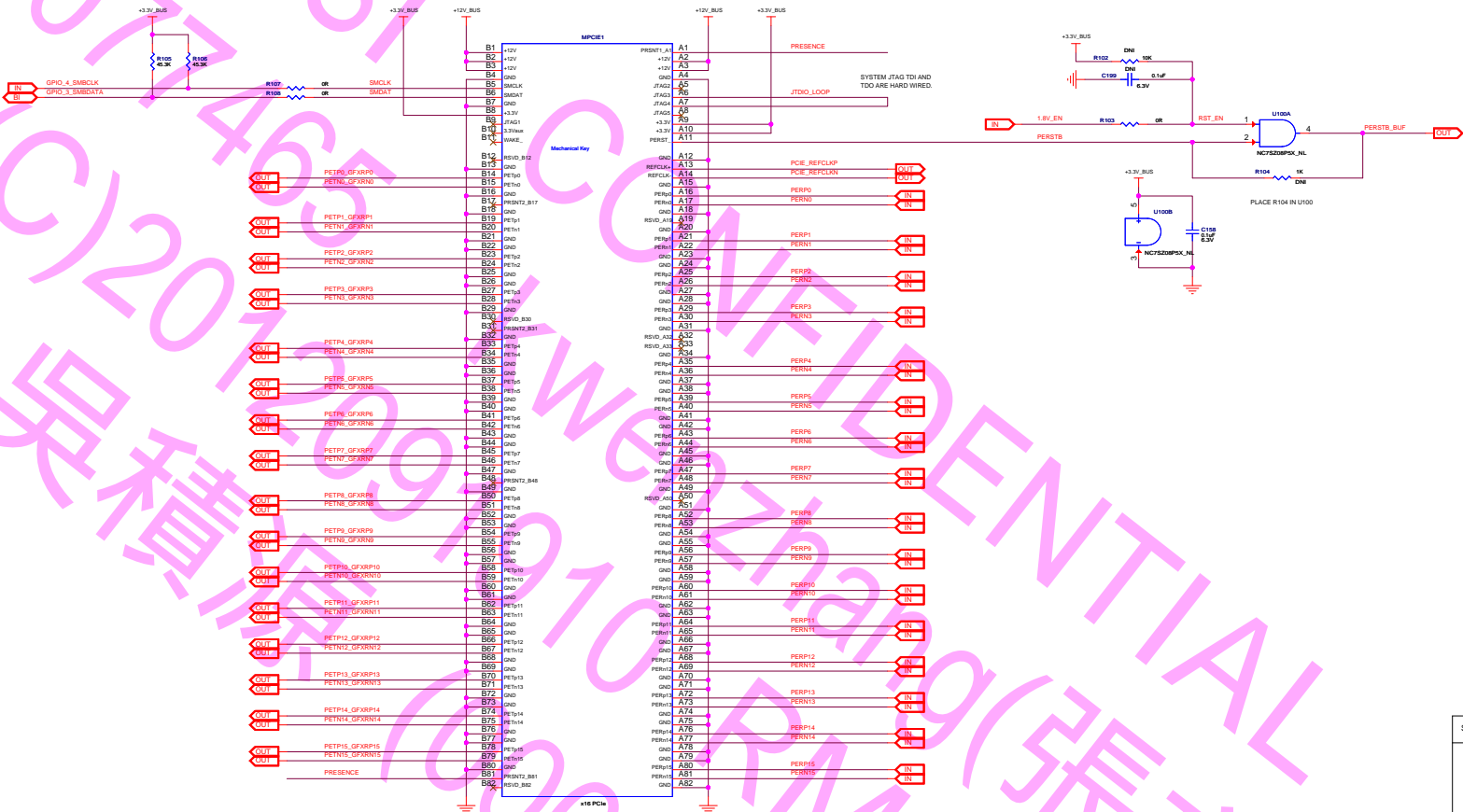
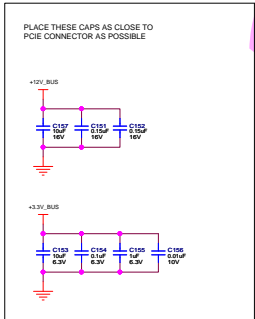
(2) PITCAIRN PCIE INTERFACE



(3) PITCAIRN MEM INTERFACE CH AB



(1) PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
b or #	ACTIVE LOW
BUG	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

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MIS-V281

Size Custom

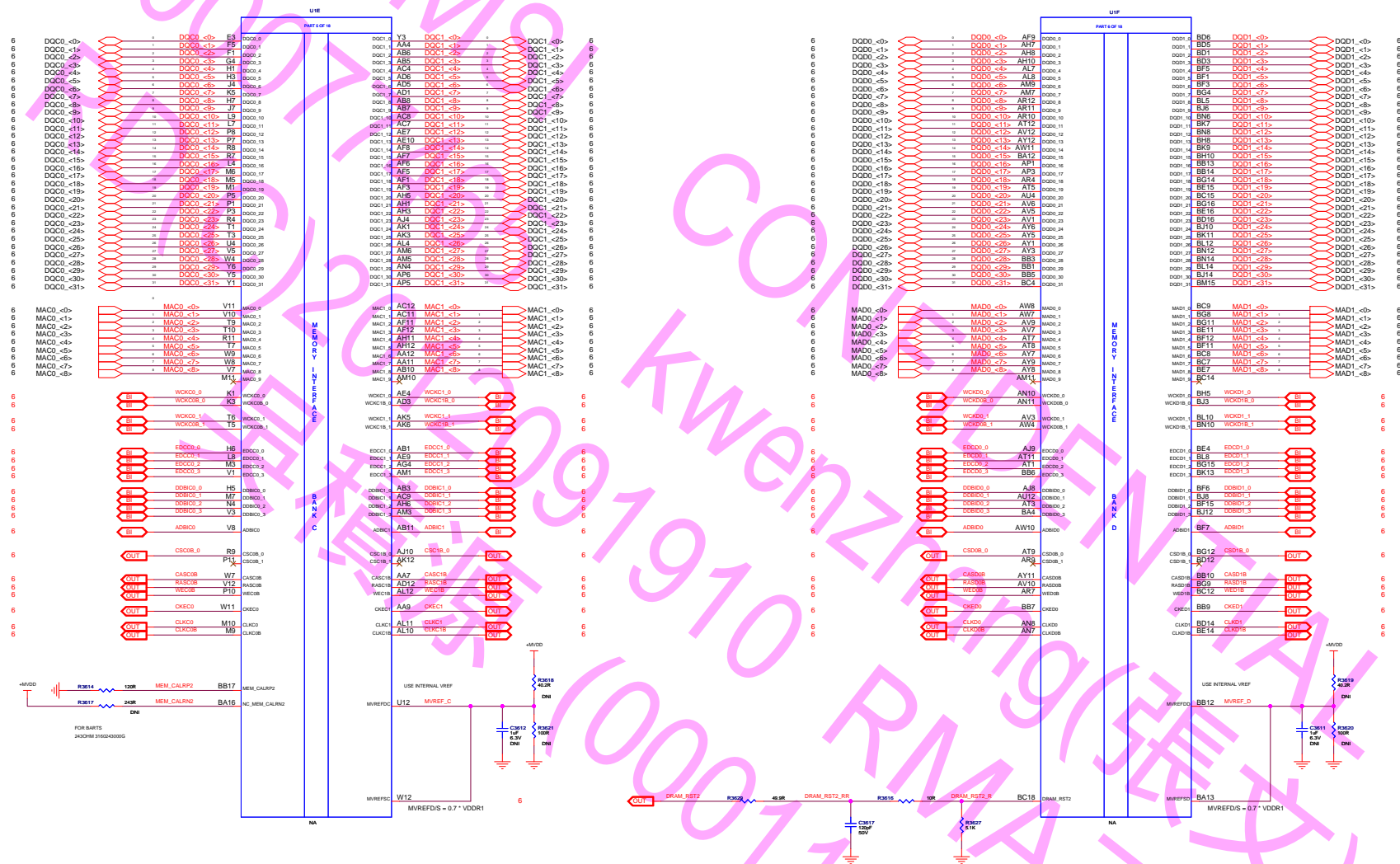
Document Description 01 PCI-EXPRESS

Rev 12

Date: Saturday, February 25, 2012

Sheet 1 of 25

(4) PITCAIRN MEM INTERFACE CH CD

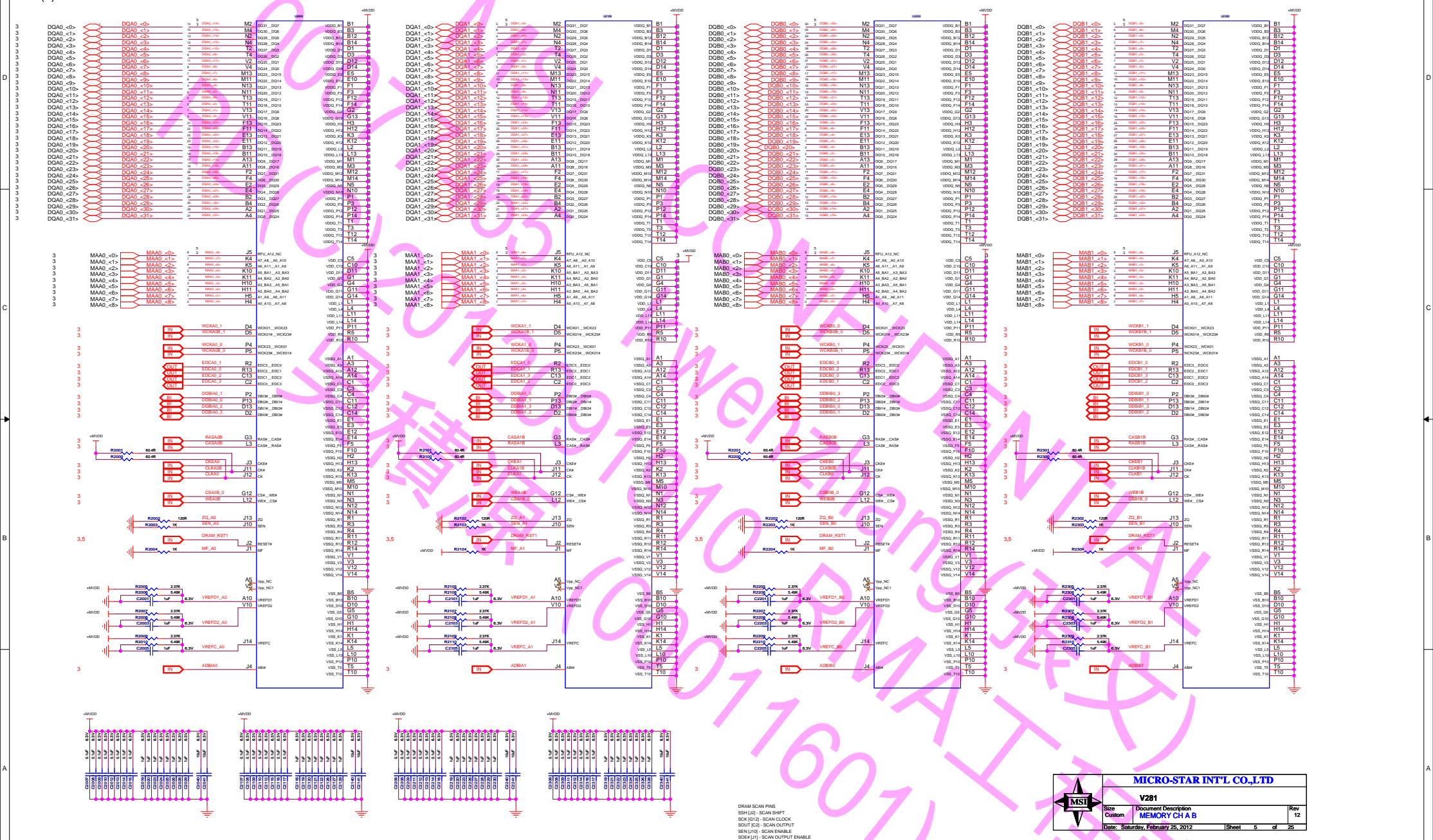


MICRO-STAR INT'L CO.,LTD

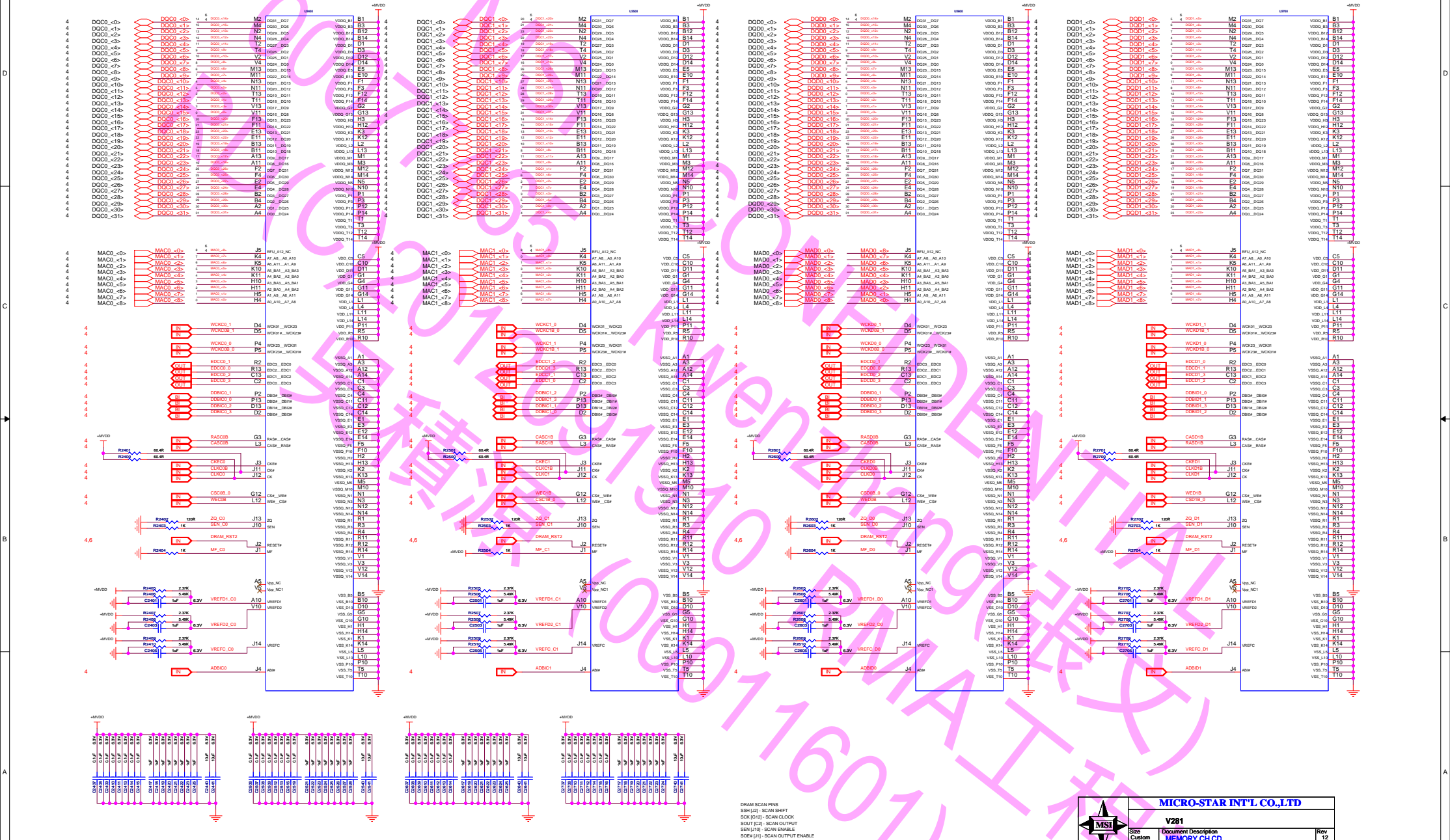
V281

Size Custom	Document Description MEM INTERFACE CH C D	Rev 12
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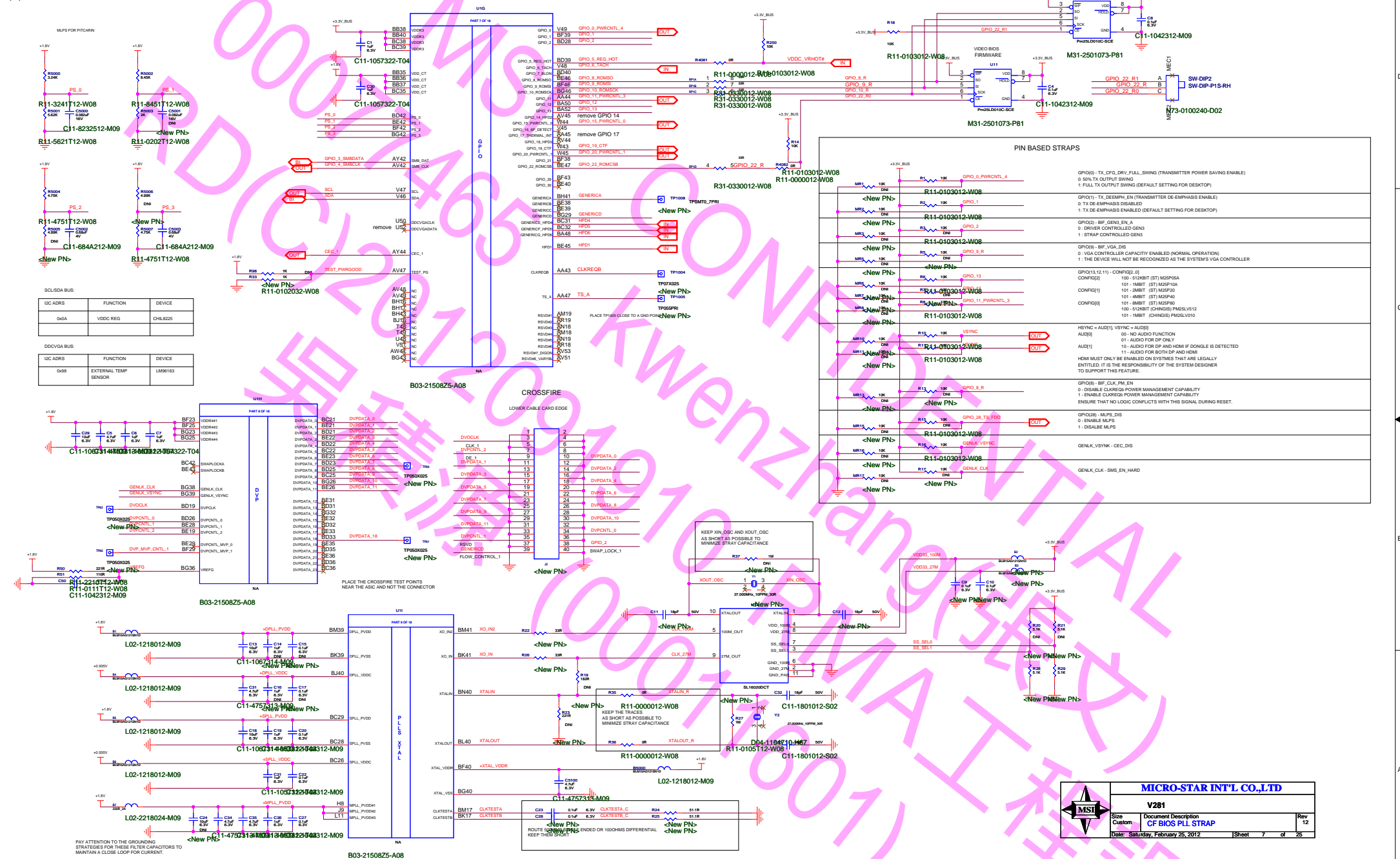
(5) GDDR5 MEMORY CH AB

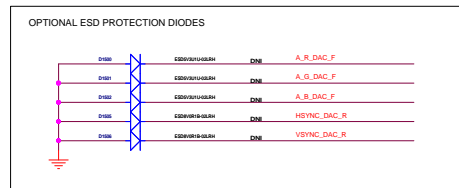


(6) GDDR5 MEMORY CH CD

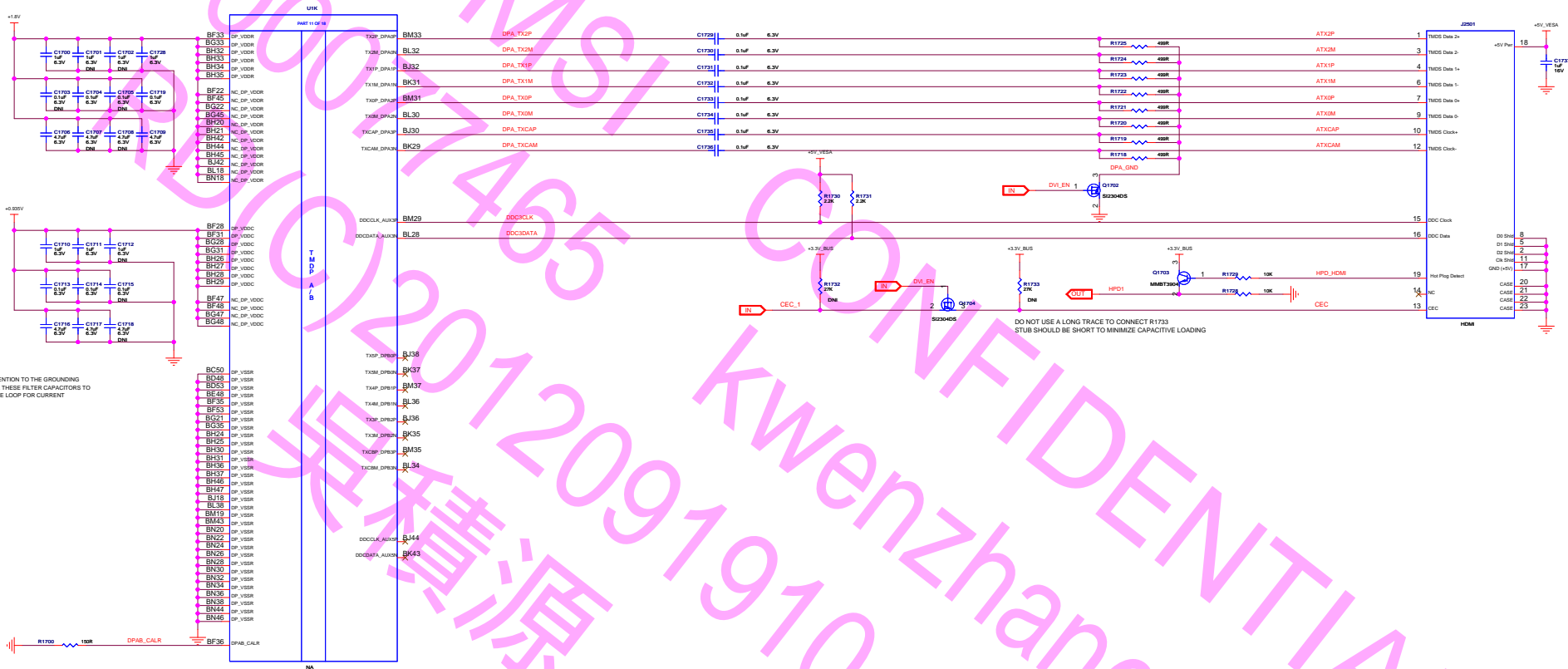


(7) PITCAIRN GPIO STRAP CF PLL XTAL

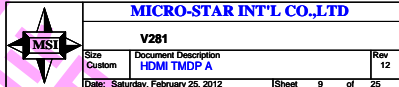
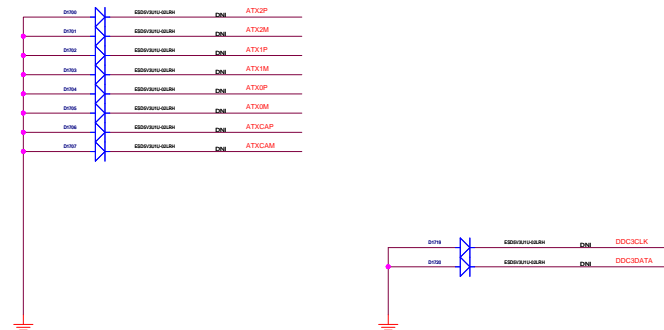


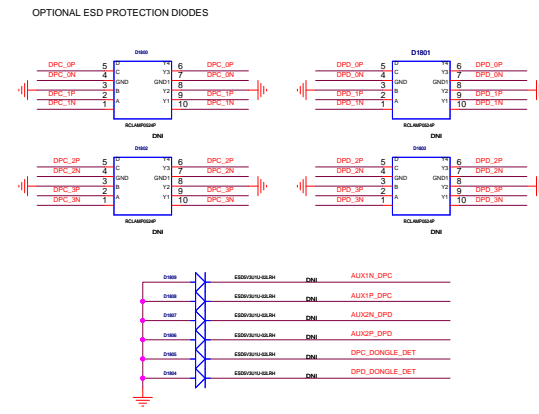
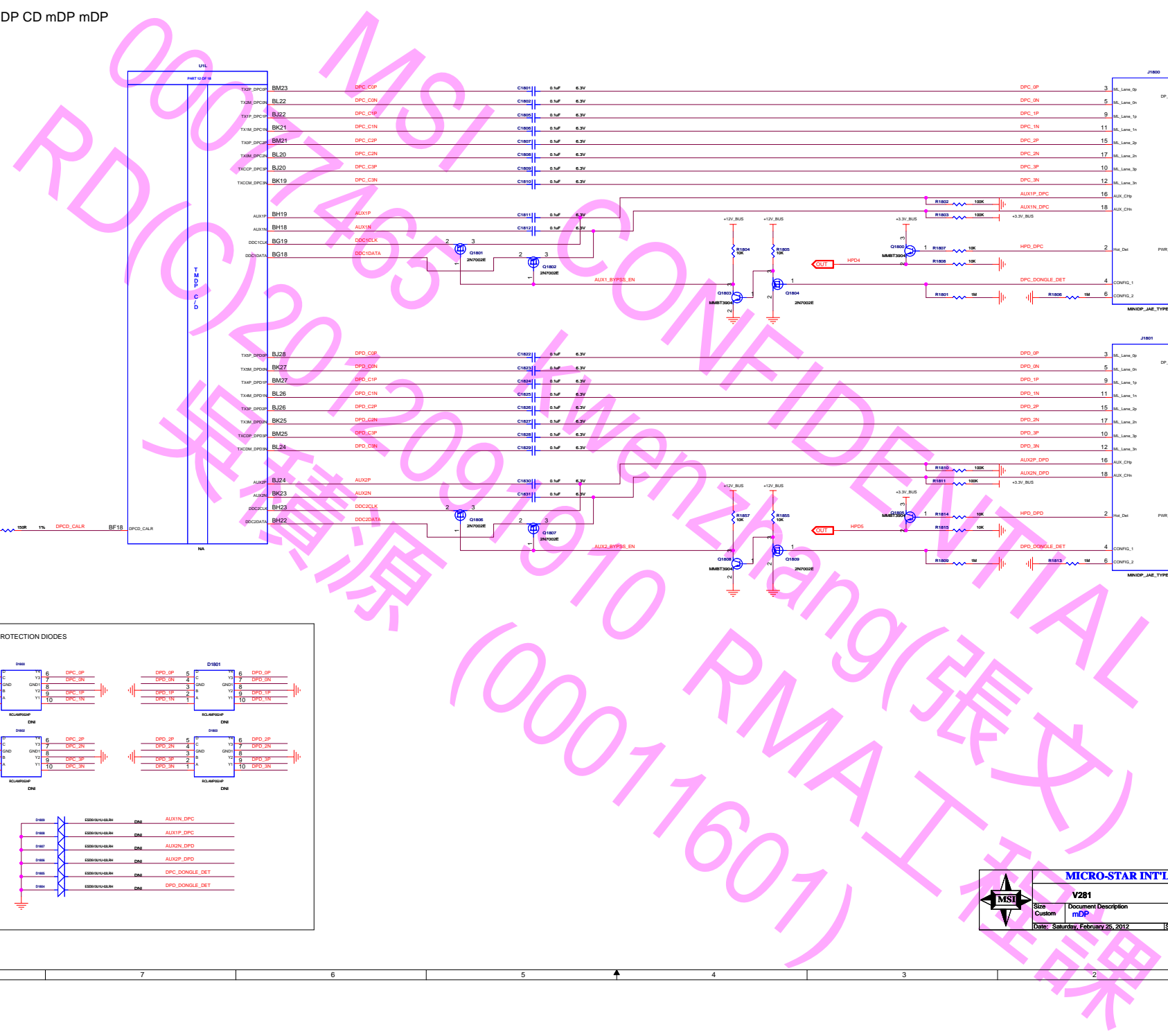


(9) PITCAIRN TMDP AB HDMI sDVI



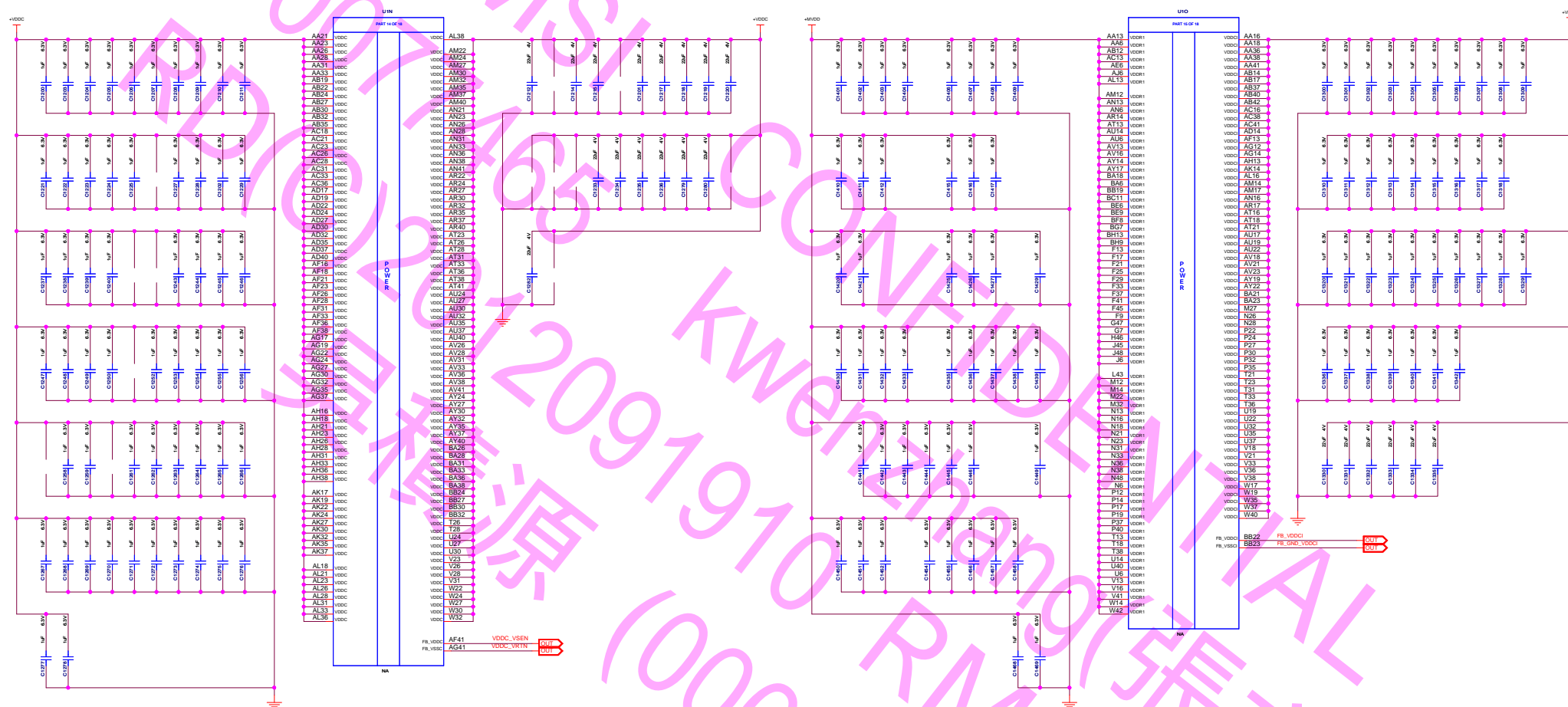
OPTIONAL ESD PROTECTION DIODE



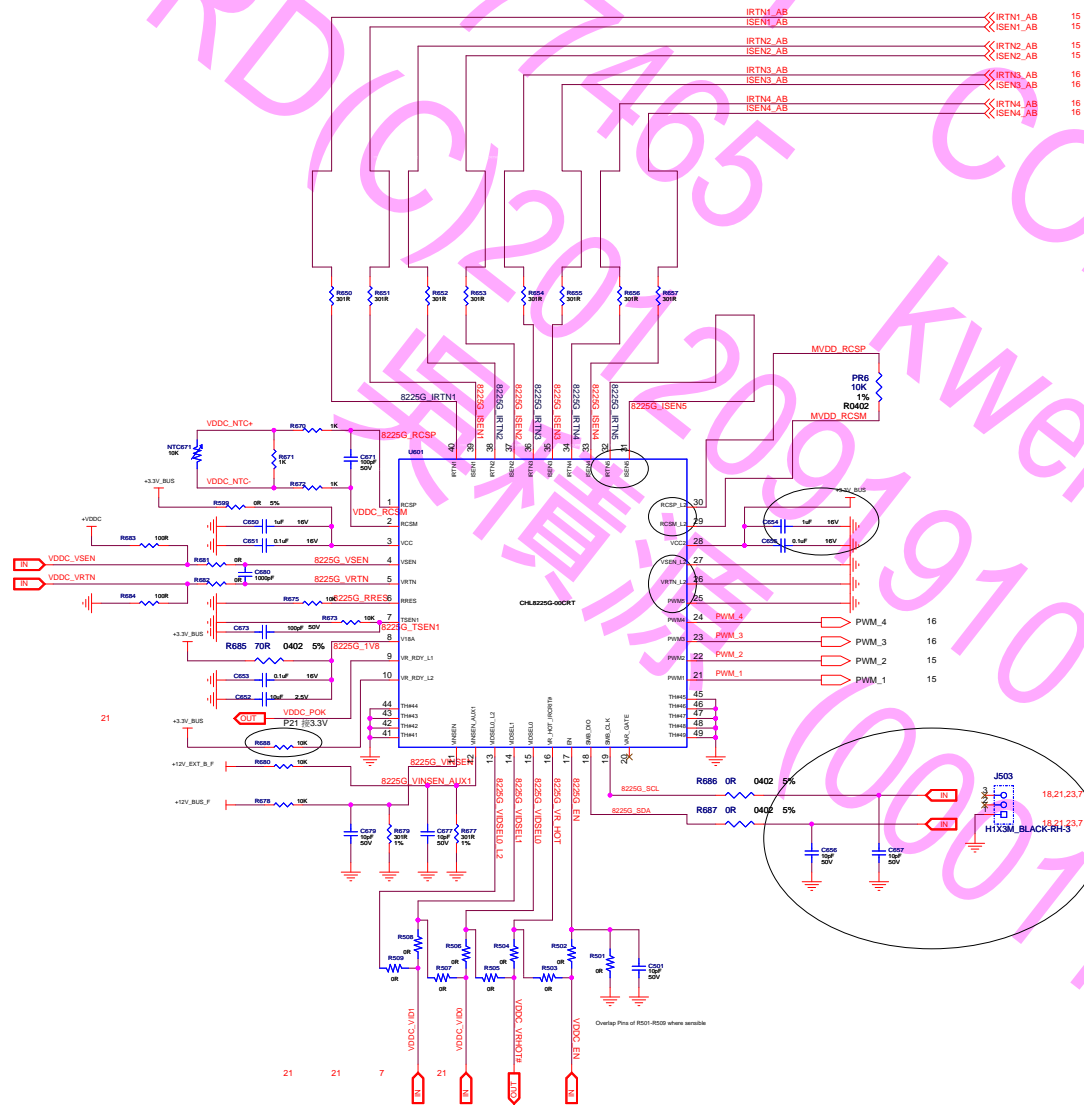




(12) PITCAIRN POWER

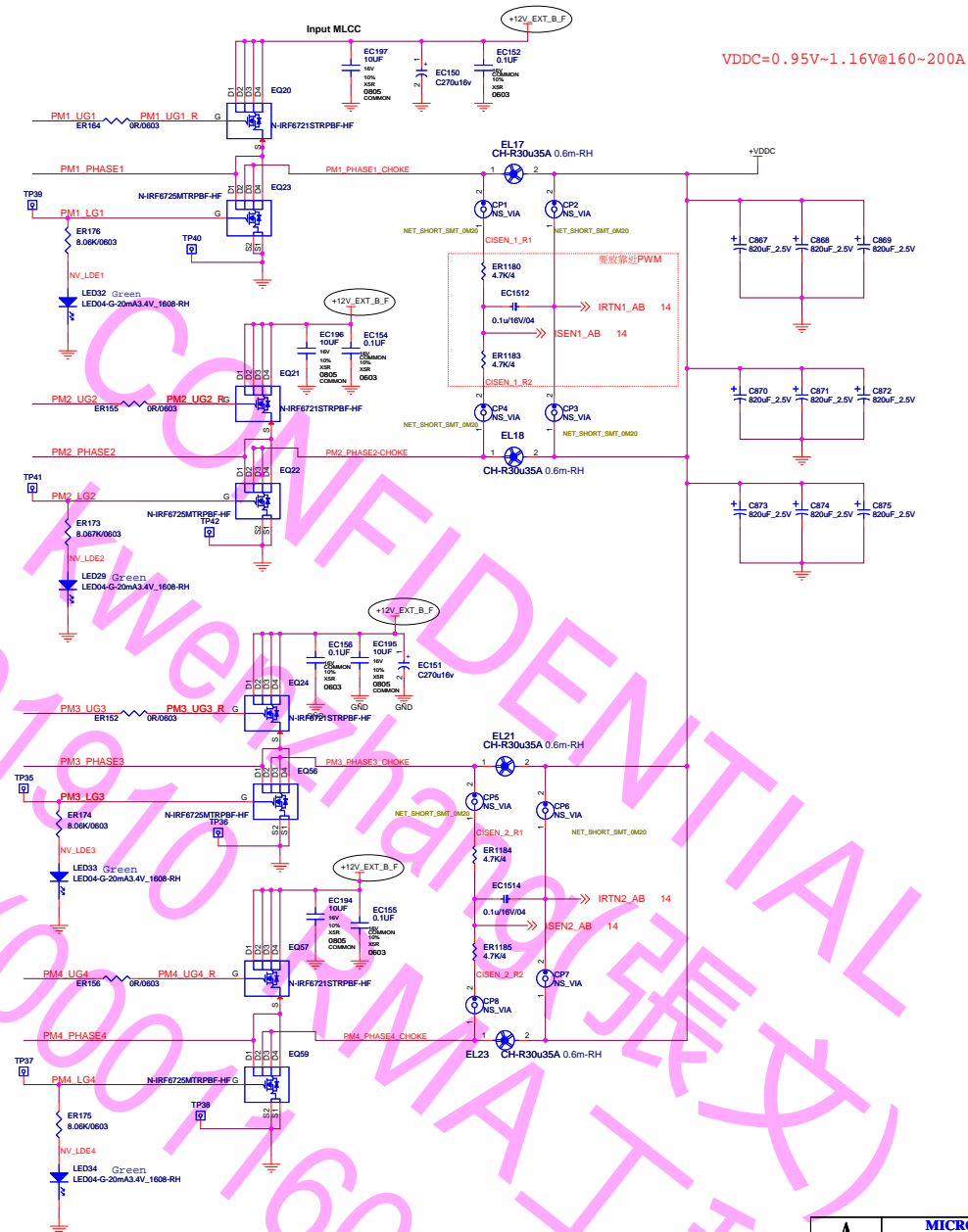
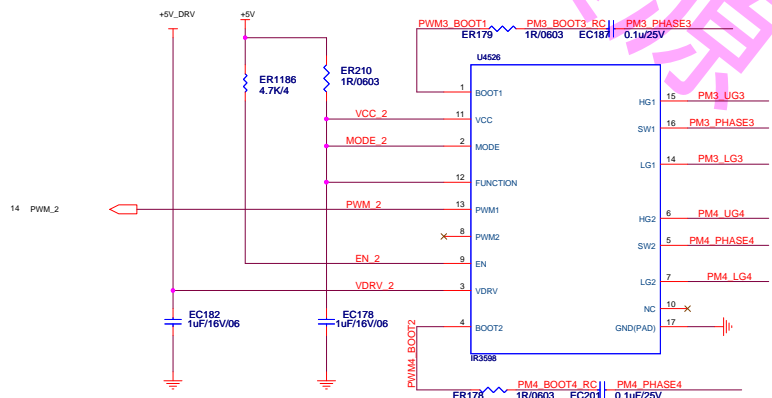
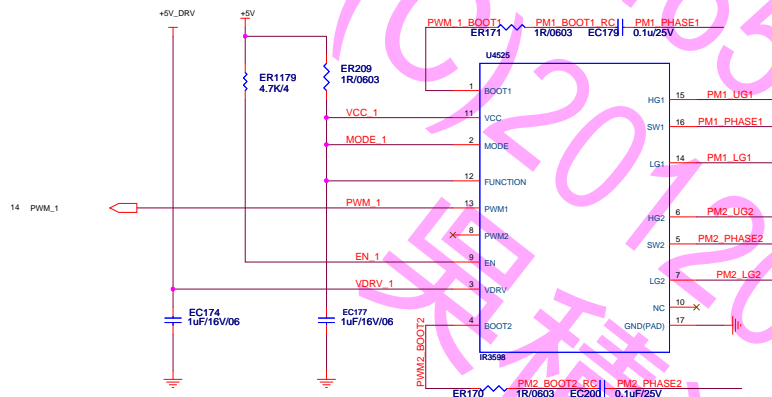
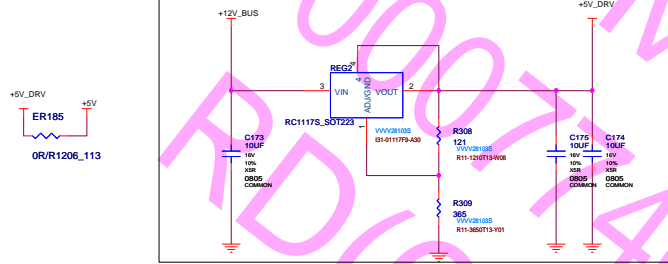


U1P		U1Q	
PART 16 OF 16		PART 17 OF 16	
A46	VS1	BA17	VS1
AA10	VS2	BA18	VS2
AA14	VS3	BA2	VS3
AA17	VS4	BA21	VS4
AA19	VS5	BA23	VS5
AA2	VS6	BA27	VS6
AA22	VS7	BA3	VS7
AA24	VS8	BA32	VS8
AA27	VS9	BA33	VS9
AA30	VS10	BA35	VS10
AA32	VS11	BA37	VS11
AA33	VS12	BA40	VS12
AA37	VS13	BA41	VS13
AA40	VS14	BB1	VS14
AA42	VS15	BB10	VS15
AA5	VS16	BB11	VS16
AB13	VS17	BB16	VS17
AB16	VS18	BB17	VS18
AB18	VS19	BB2	VS19
AB21	VS20	BB22	VS20
AB23	VS21	BB23	VS21
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AB33	VS25	BB35	VS25
AB36	VS26	BB40	VS26
AB38	VS27	BB41	VS27
AB41	VS28	BB8	VS28
AB5	VS29	BC16	VS29
AC10	VS30	BC19	VS30
AC14	VS31	BC2	VS31
AC17	VS32	BC23	VS32
AC19	VS33	BC30	VS33
AC2	VS34	BC33	VS34
AC22	VS35	BC35	VS35
AC24	VS36	BC8	VS36
AC27	VS37	BD15	VS37
AC30	VS38	BD16	VS38
AC32	VS39	BD20	VS39
AC37	VS40	BD33	VS40
AC40	VS41	BE12	VS41
AC42	VS42	BE10	VS42
AC5	VS43	BE16	VS43
AD16	VS44	BE20	VS44
AD18	VS45	BE23	VS45
AD21	VS46	BE28	VS46
AD23	VS47	BE31	VS47
AD25	VS48	BE33	VS48
AD28	VS49	BE35	VS49
AD31	VS50	BE40	VS50
AD33	VS51	BE41	VS51
AD36	VS52	BE8	VS52
AD38	VS53	BF12	VS53
AD41	VS54	BF10	VS54
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AE2	VS56	BF20	VS56
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AF30	VS65	BF12	VS65
AF32	VS66	BF10	VS66
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BA33	VS132	BF33	VS132
BA35	VS133	BF35	VS133
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BA40	VS135	BF41	VS135
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BF41	VS		



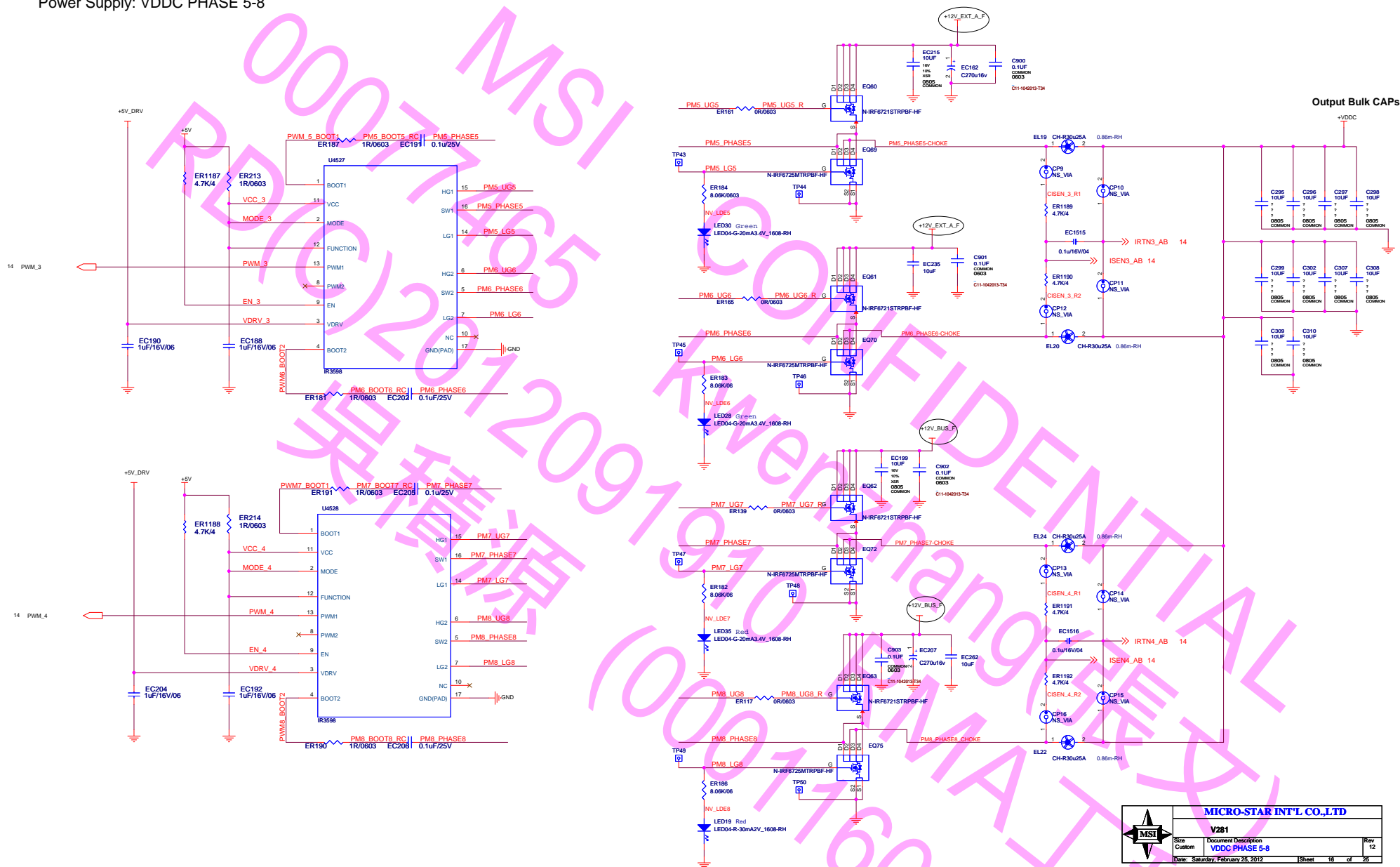
Power Supply: VDDC PHASE 1,~4

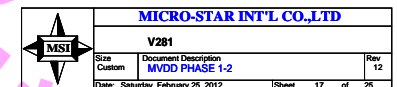
5V POWER SUPPLY FOR DRIVER

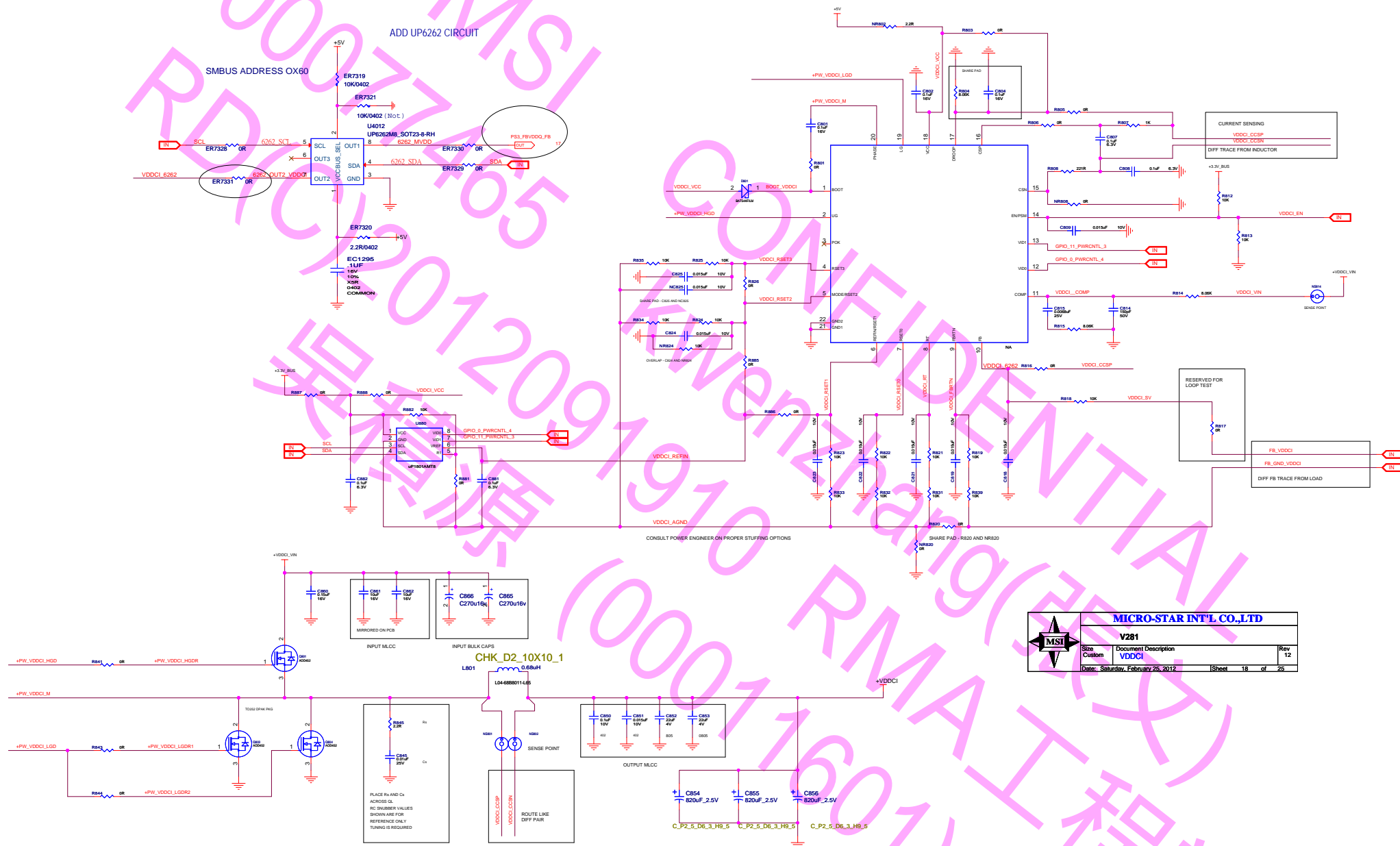


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Power Supply: VDDC PHASE 5-8







LAYOUT GUIDELINE

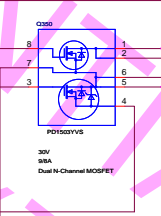
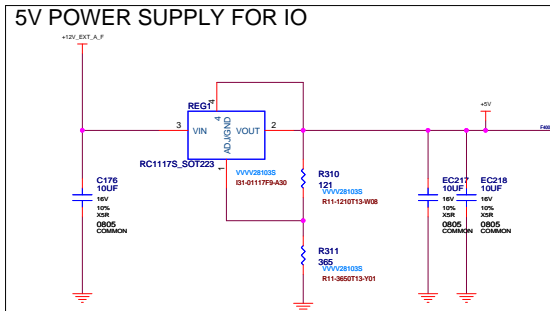
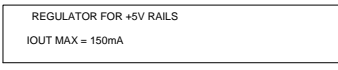
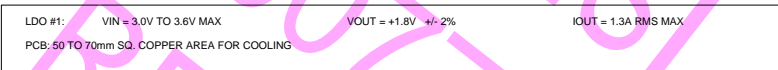
1. POSITION THE CONTROLLER (U703) SUCH THAT LGATE (PIN4) IS THE CLOSEST TO THE GATE OF THE MOSFETS. YOU CAN PLACE THE GATE RESISTORS R721 AND R722 NEXT TO THE GATE OF THE MOSFETS. MAKE THE GATE DRIVE TRACES (PIN, M5000, LG2HSD) AS SHORT AS POSSIBLE TO REDUCE THE TRACE INDUCTANCE.

2. PLACE THE BYPASS CAPACITORS FOR VCC (C703) AS WELL AS BOOST CAPS (C705) AS CLOSE TO THE CONTROLLER AS POSSIBLE.


3. VOLTAGE AMPLIFIER COMPENSATION NETWORK: PLACE R714 CLOSE TO THE PIN 7. PLACE THE REST OF THE COMPENSATION NETWORK (R716, R711, R712, R713, C711, C712 AND C713) CLOSE TO THE PINS 7 AND 6.

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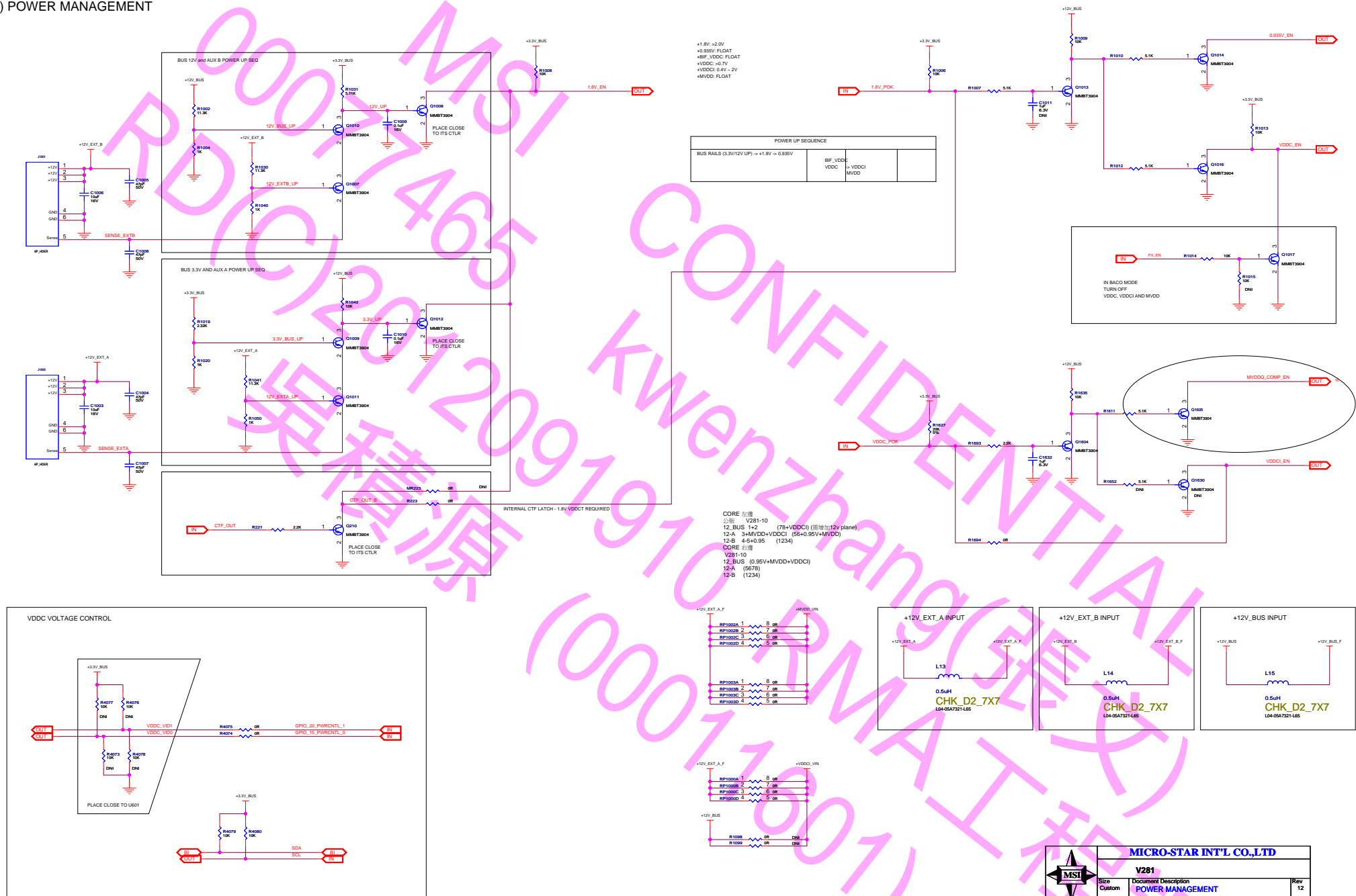
(17) SMALL RAIL REGULATOR



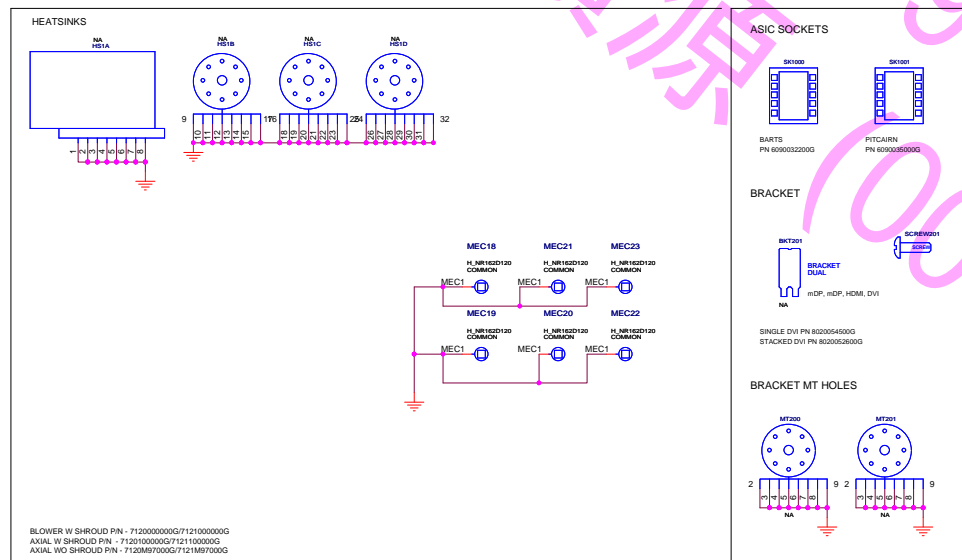
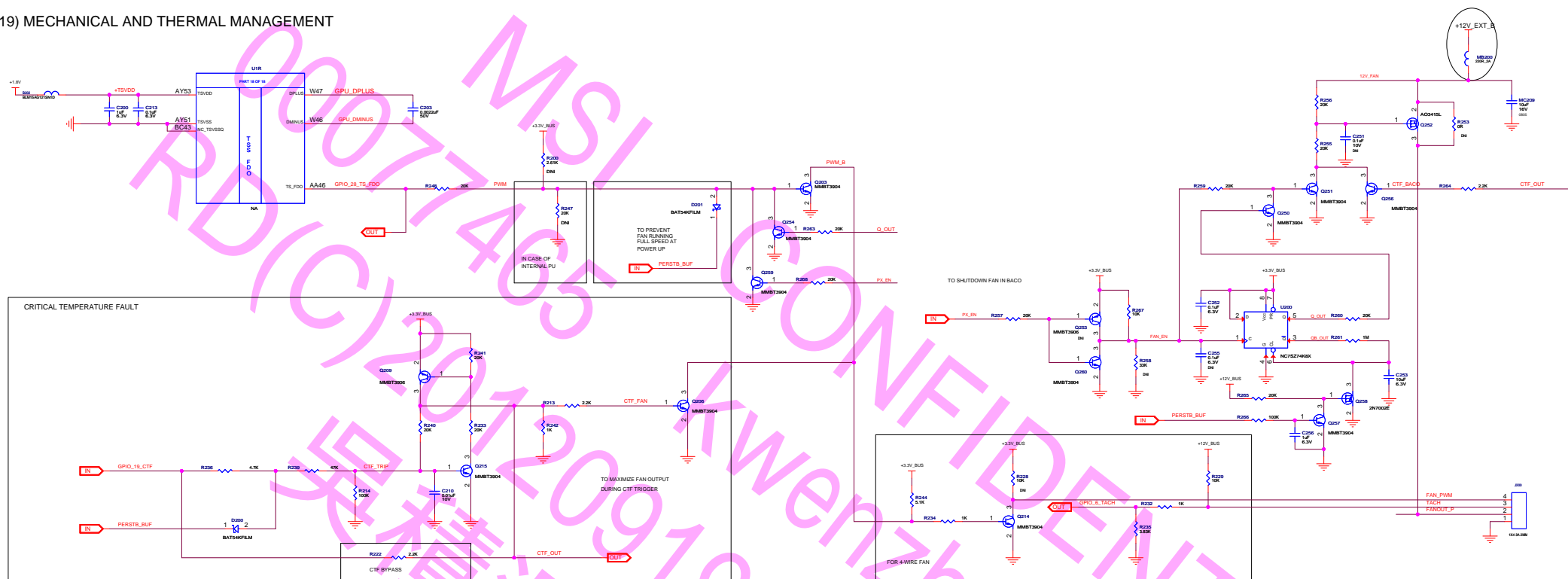
CONNECT ALL CONTROLLER RELATED GROUND ONLY AT C355


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(18) POWER MANAGEMENT



(19) MECHANICAL AND THERMAL MANAGEMENT



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AMD



TITLE: Pitcairn GDDR5 x32

DOCUMENT NUMBER: 105-C401xx-00

DATE: Wed Dec 21 19:16:58 2011

SHEET NUMBER: 22 OF 22

REV: <REV>

REVISION HISTORY

ENGINEER: <ENGINEER>

NOTES: NOTE


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Markham, ON L3T 7X6

SCH Rev	PCB Rev	Date	REVISION DESCRIPTION
	00A	11/08/2011	INITIAL DESIGN BASED ON CHAS FITCH/RYAN TRICAL LAYOUT
	00B	11/08/2011	LAYOUT INCREASE SPACING BETWEEN BGA AND JANE
	00C	12/11/2011	UPDATE FANBACK CIRCUITRY LAYOUT IMPROVE DISPLAY SEATING
	00	12/12/2011	ADD 750M SERVO ADDRESS 0-3 INPUT OPTION FOR 0.880V BGA ADD 0.80V-0.850V, RING, COUT
			REV: 1.2 更新MEM POWER 更新MEM SEQ VDDCI SEQ



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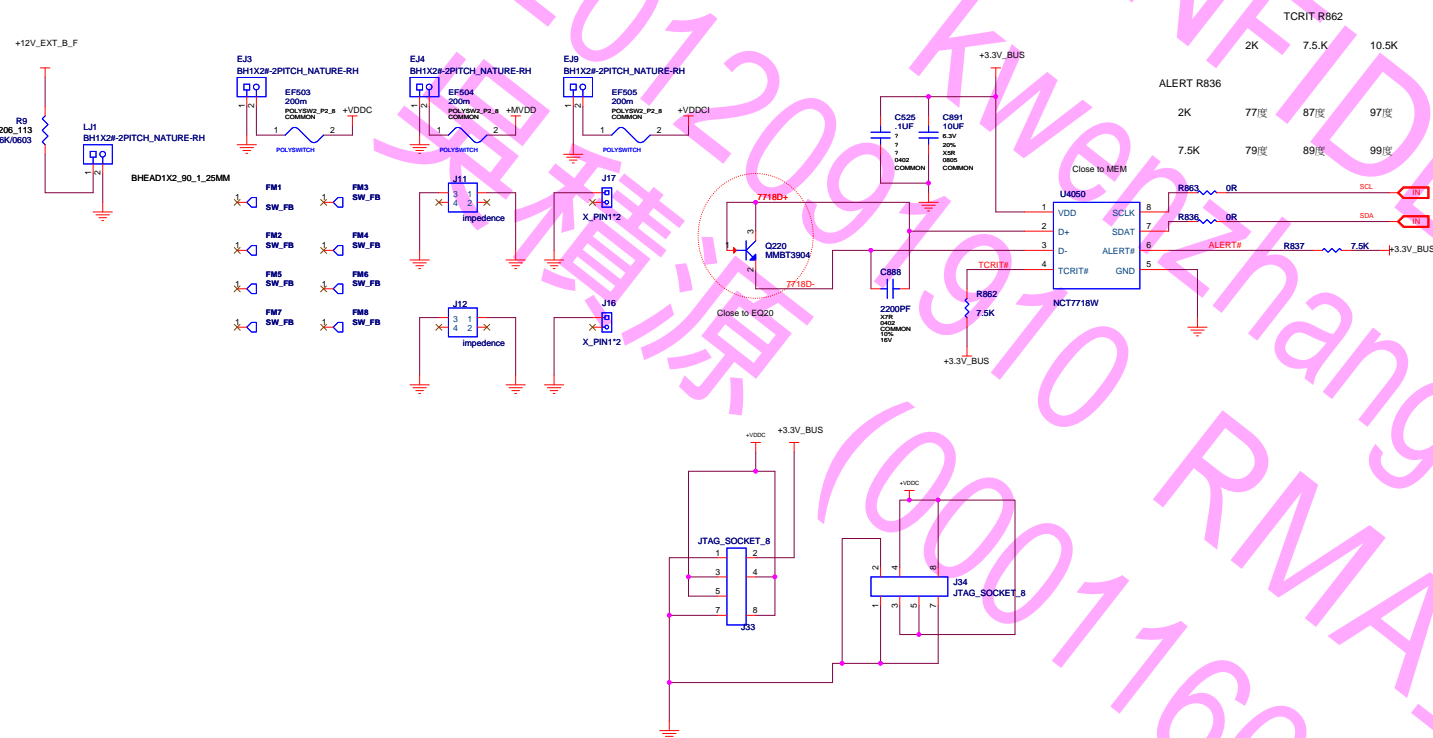
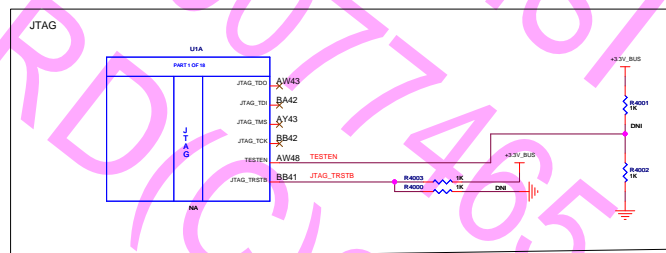
Document Description REVISION HISTORY


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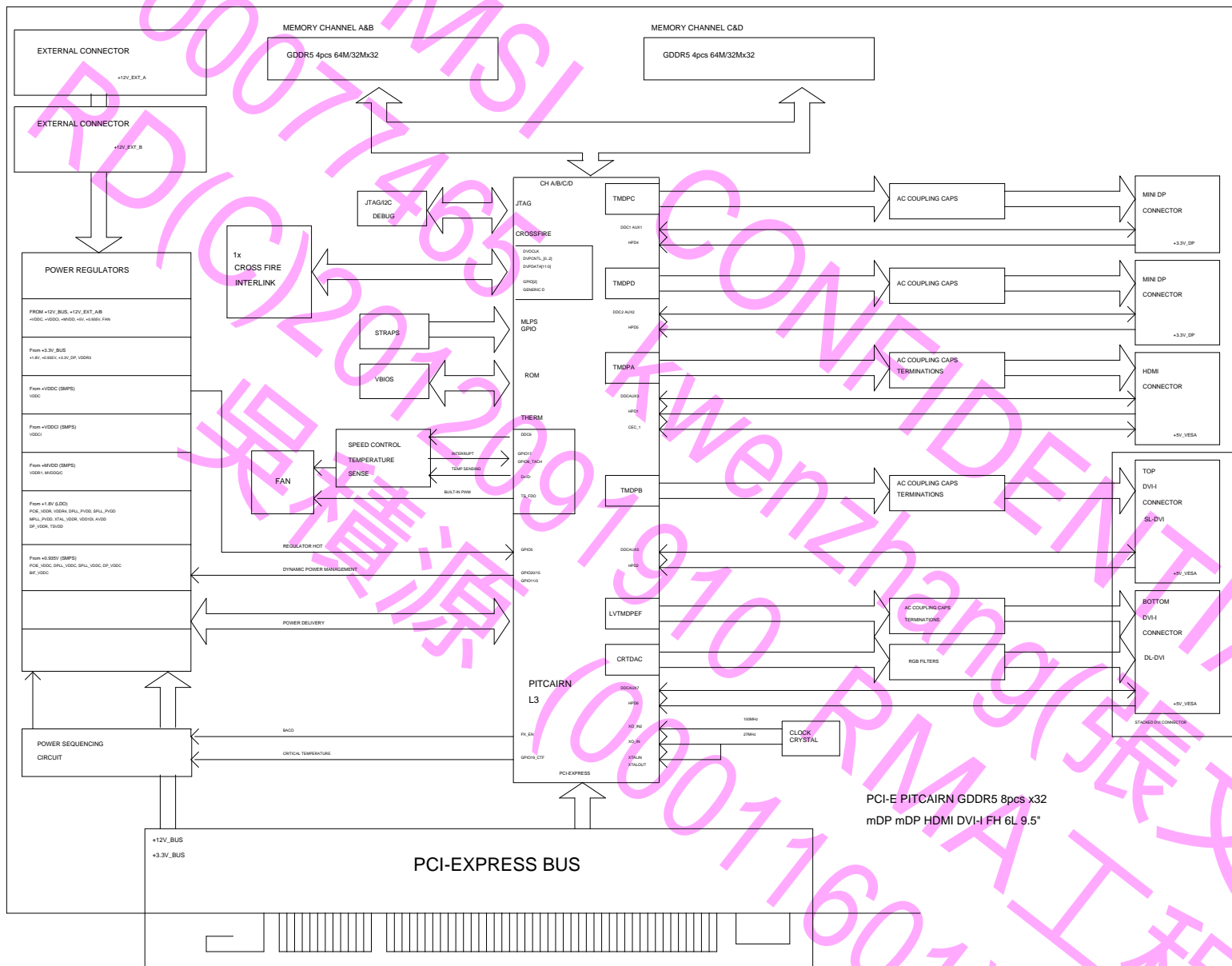
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(20) DEBUG CIRCUIT



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PCI-E PITCAIRN GDDR5 8pcs x32
mDP mDP HDMI DVI-I FH 6L 9.5"

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