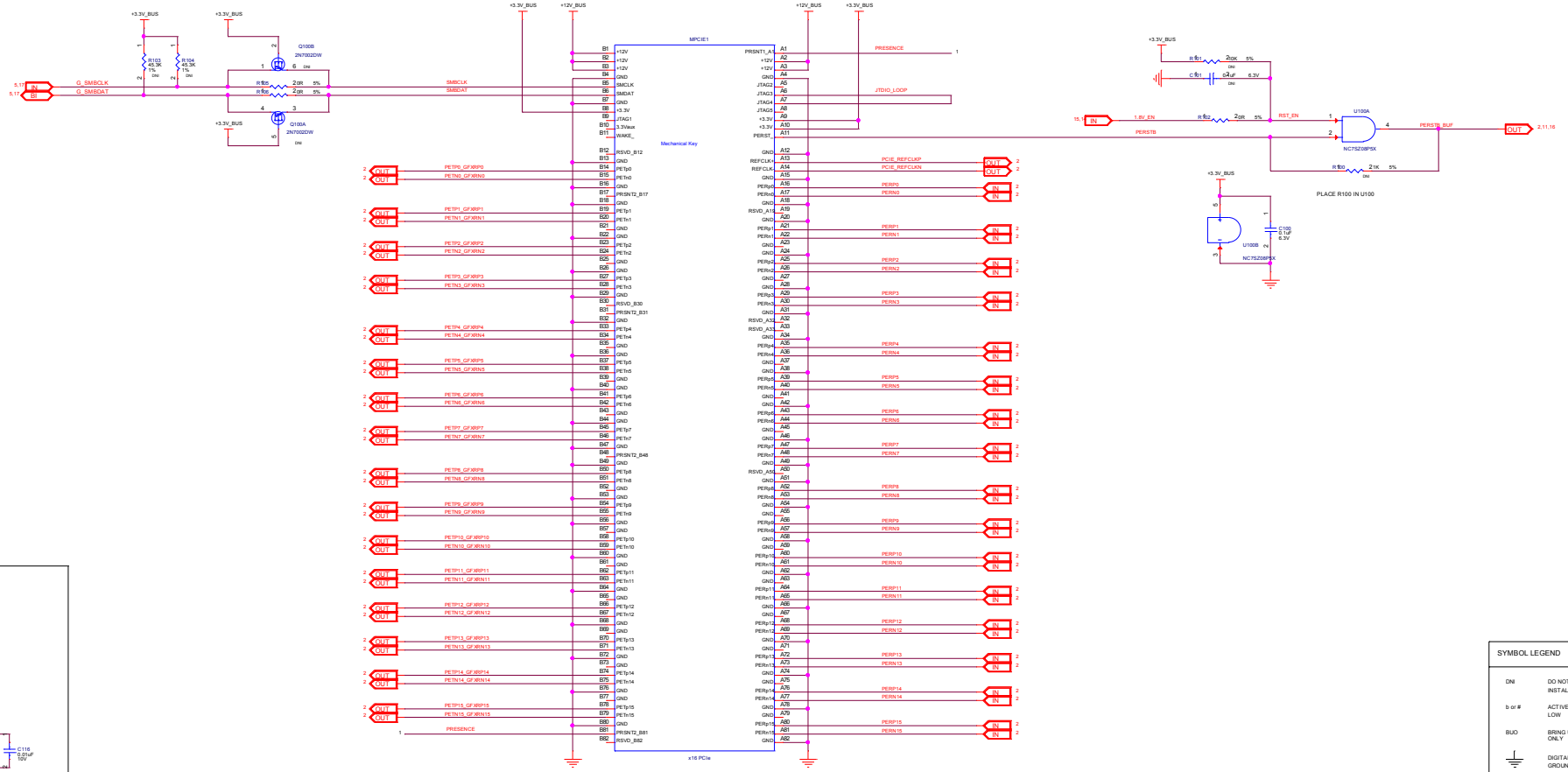
(1) PCI-EXPRESS EDGE CONNECTOR



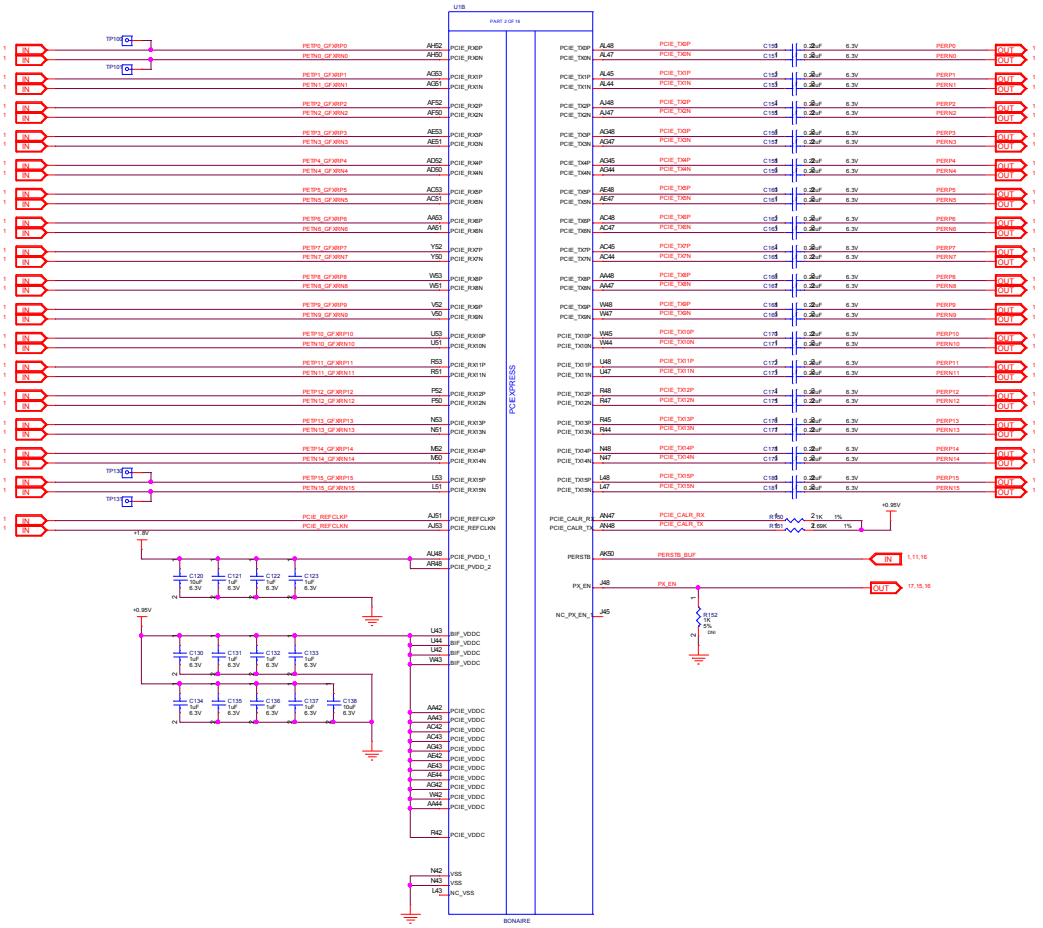
SYMBOL LEGEND

DNI	DO NOT INSTALL
b or #	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET:	PCI-EXPRESS EDGE CONNECTOR
DATE:	Thu Apr 23 05:56:02 2015
REV:	1.0
SHEET NUMBER:	1 OF 19
DOCUMENT NUMBER:	105_C913xx_00
NOTES:	NOTE
TITLE:	TOBAGO GDDR5 X32

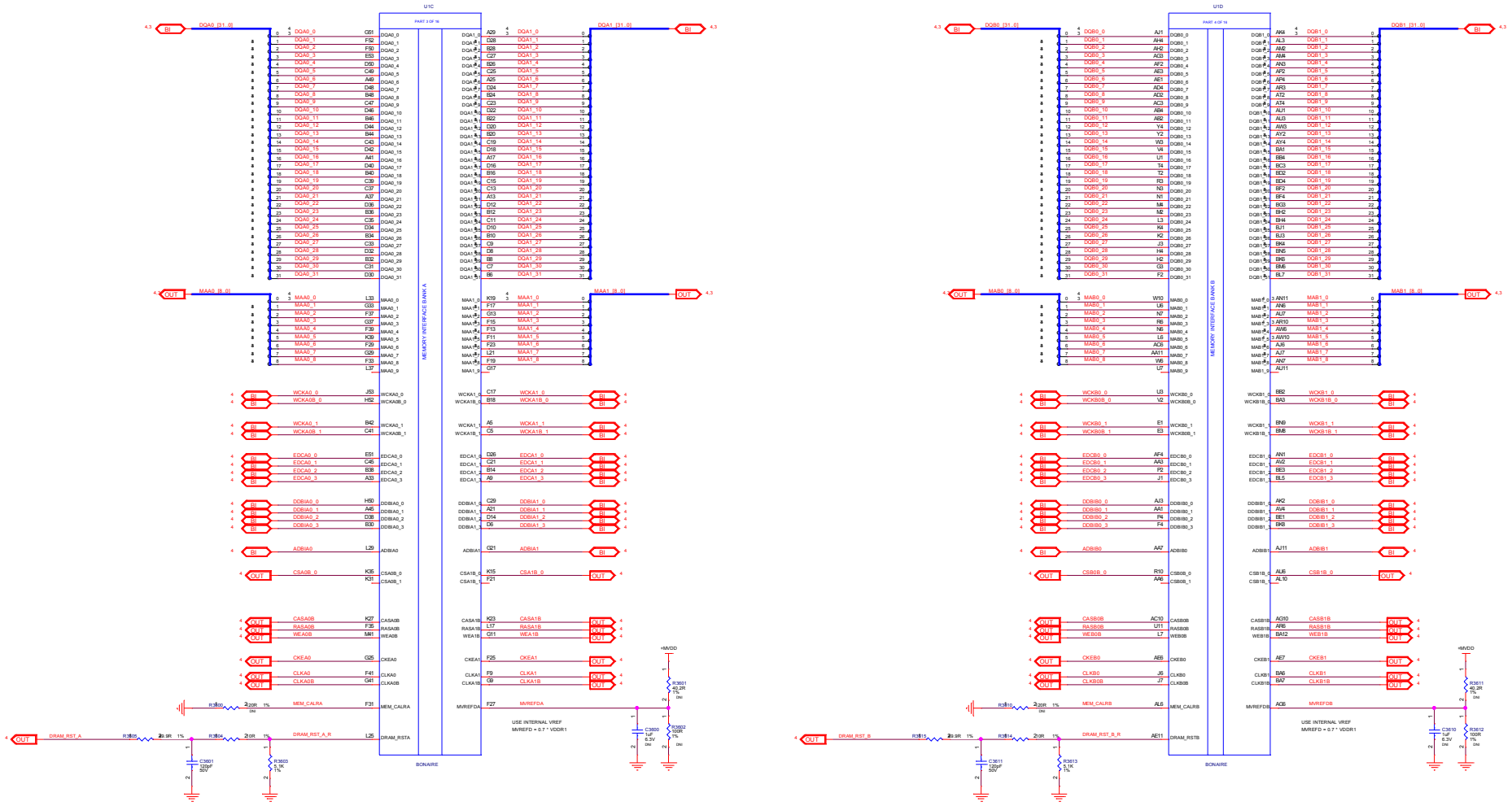
(2) TOBAGO PCIE INTERFACE



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: TOBAGO PCIE	
DATE: Thu Apr 23 05:54:17 2015	REV: 1.0
SHEET NUMBER: 2 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

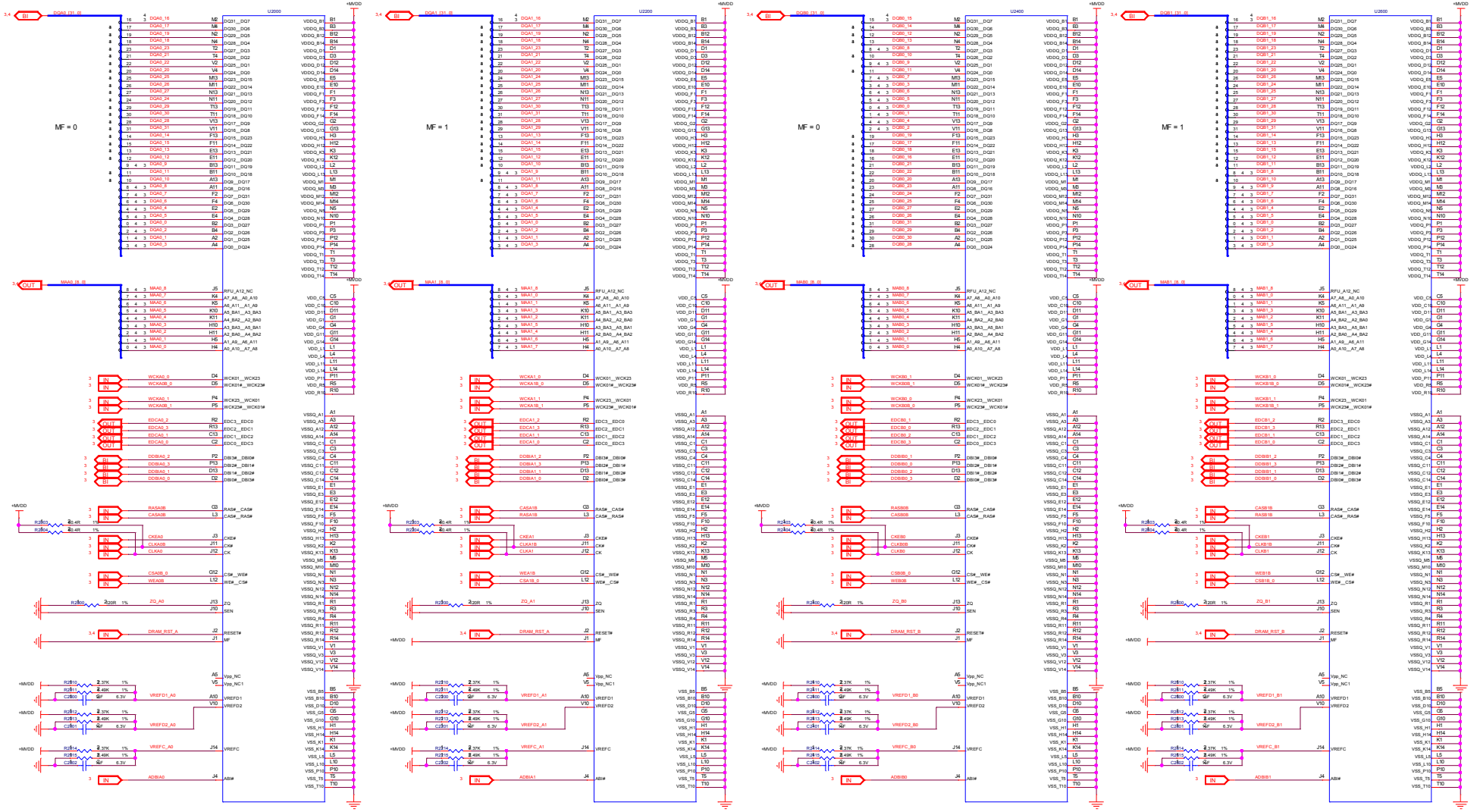
TITLE: TOBAGO GDDR5 X32

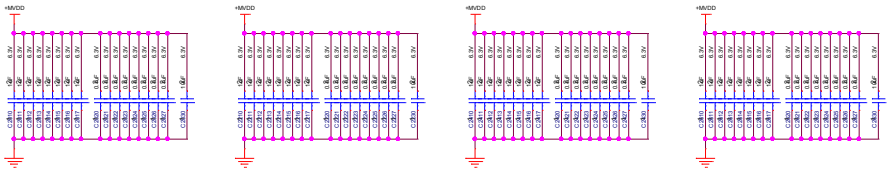
(3) TOBAGO MEMORY INTERFACE



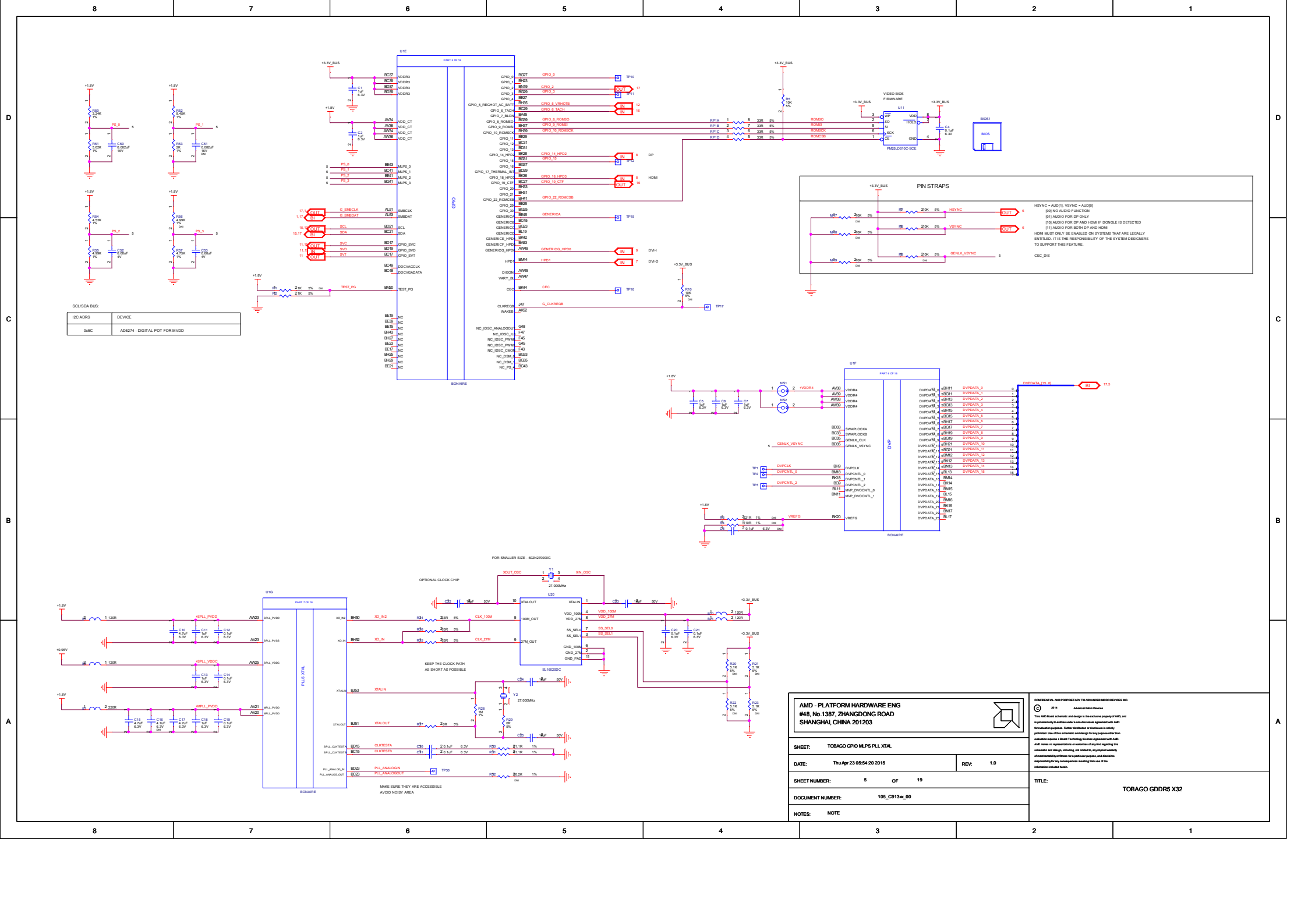
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: TOBAGO MEMORY	
DATE: Thu Apr 23 05:54:18 2015	REV: 1.0
SHEET NUMBER: 3 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	TITLE: TOBAGO GDDR5 X32

(4) GDDR5 CHAB x32

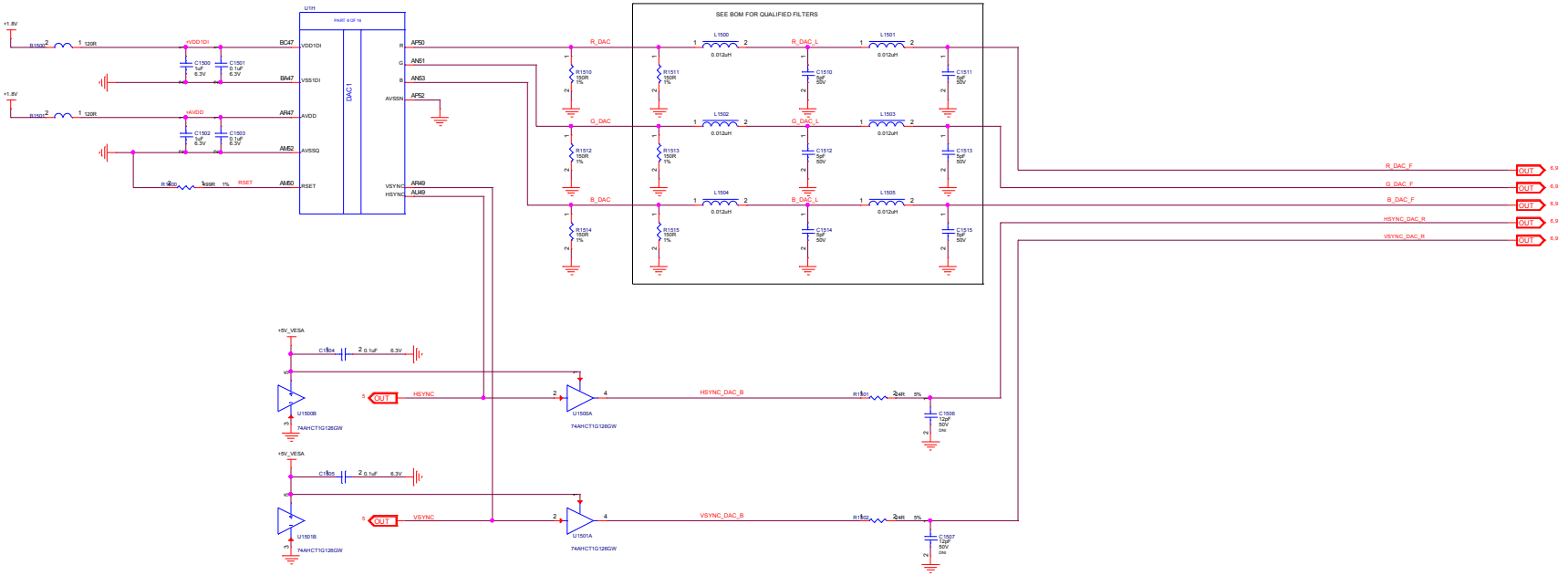


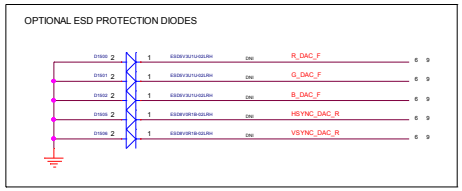


AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: GDDR5 x32 CHAB	
DATE: Thu Apr 23 05:54:19 2015	REV: 1.0
SHEET NUMBER: 4 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	TITLE: TOBAGO GDDR5 X32


SCL/SDA BUS:
I2C ADRS
DEVICE
0x5C
AD5274 - DIGITAL POT FOR MVDD
PIN STRAPS
HSYNC = AUD[1], VSYNC = AUD[0]
[00] NO AUDIO FUNCTION
[01] AUDIO FOR DP ONLY
[10] AUDIO FOR DP AND HDMI IF DONGLE IS DETECTED
[11] AUDIO FOR BOTH DP AND HDMI
HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNERS TO SUPPORT THIS FEATURE.
CEC_DIS
FOR SMALLER SIZE - 502N270000G
OPTIONAL CLOCK CHIP
KEEP THE CLOCK PATH AS SHORT AS POSSIBLE
MAKE SURE THEY ARE ACCESSIBLE AVOID NOISY AREA
AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203
SHEET: TOBAGO GPIO MLPS PLL XTAL
DATE: Thu Apr 23 05:54:20 2015
REV: 1.0
SHEET NUMBER: 5 OF 19
DOCUMENT NUMBER: 105_C913xx_00
NOTES: NOTE
TITLE: TOBAGO GDDR5 X32

(6) TOBAGO DAC

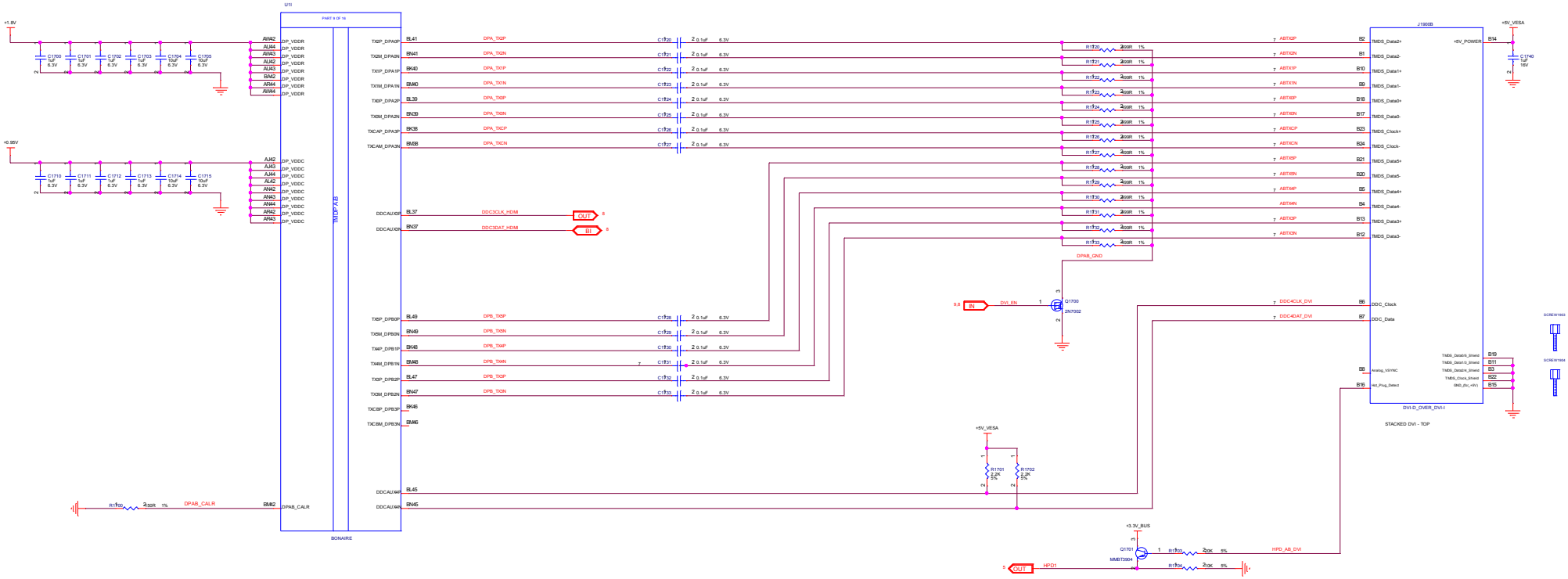


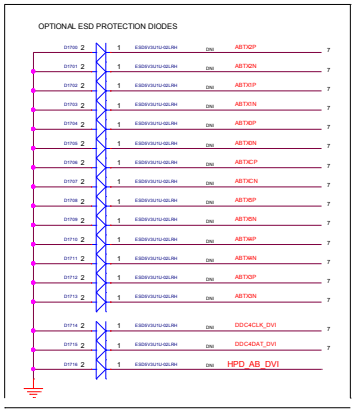


AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: TOBAGO DAC	
DATE: Thu Apr 23 05:54:20 2015	REV: 1.0
SHEET NUMBER: 6 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

TITLE: TOBAGO GDDR5 X32

(7) TOBAGO TMDPAB dDVI

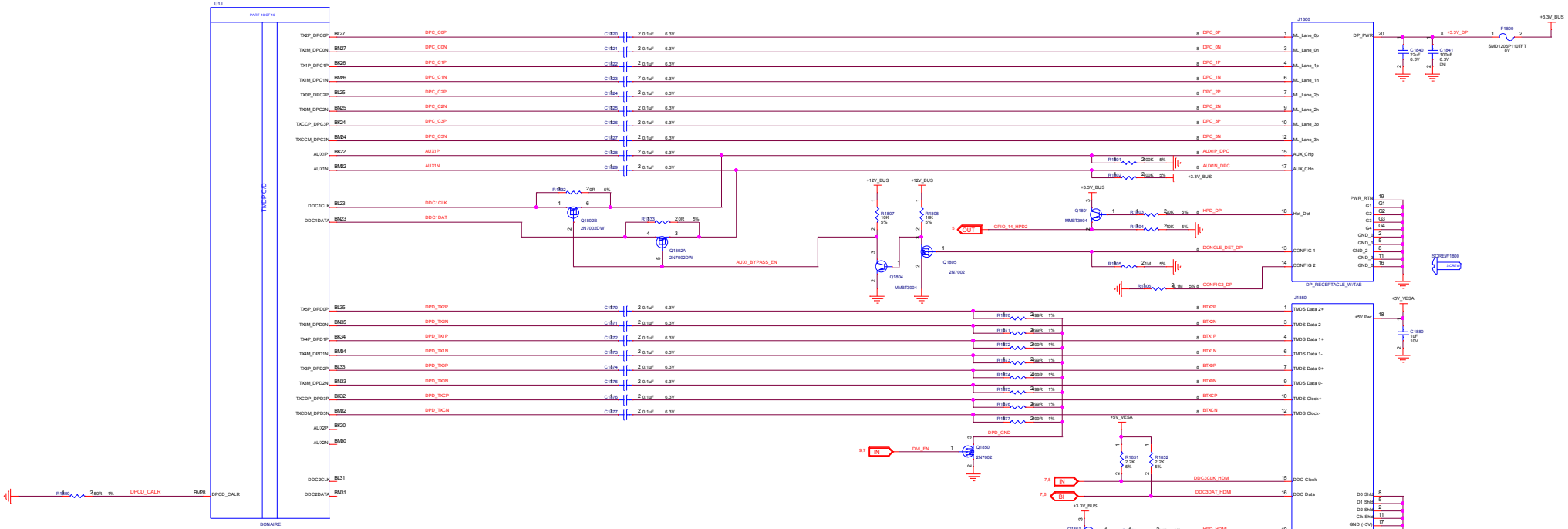


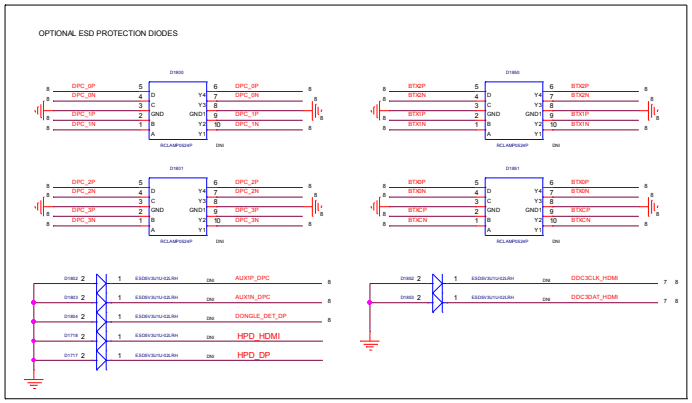


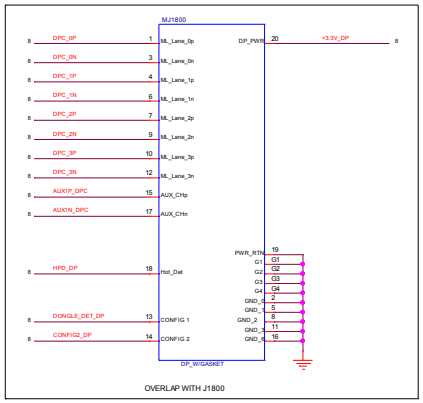
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: TOBAGO TMDPAB dDVI TOP	
DATE: Thu Apr 23 05:54:20 2015	REV: 1.0
SHEET NUMBER: 7 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

TITLE: TOBAGO GDDR5 X32

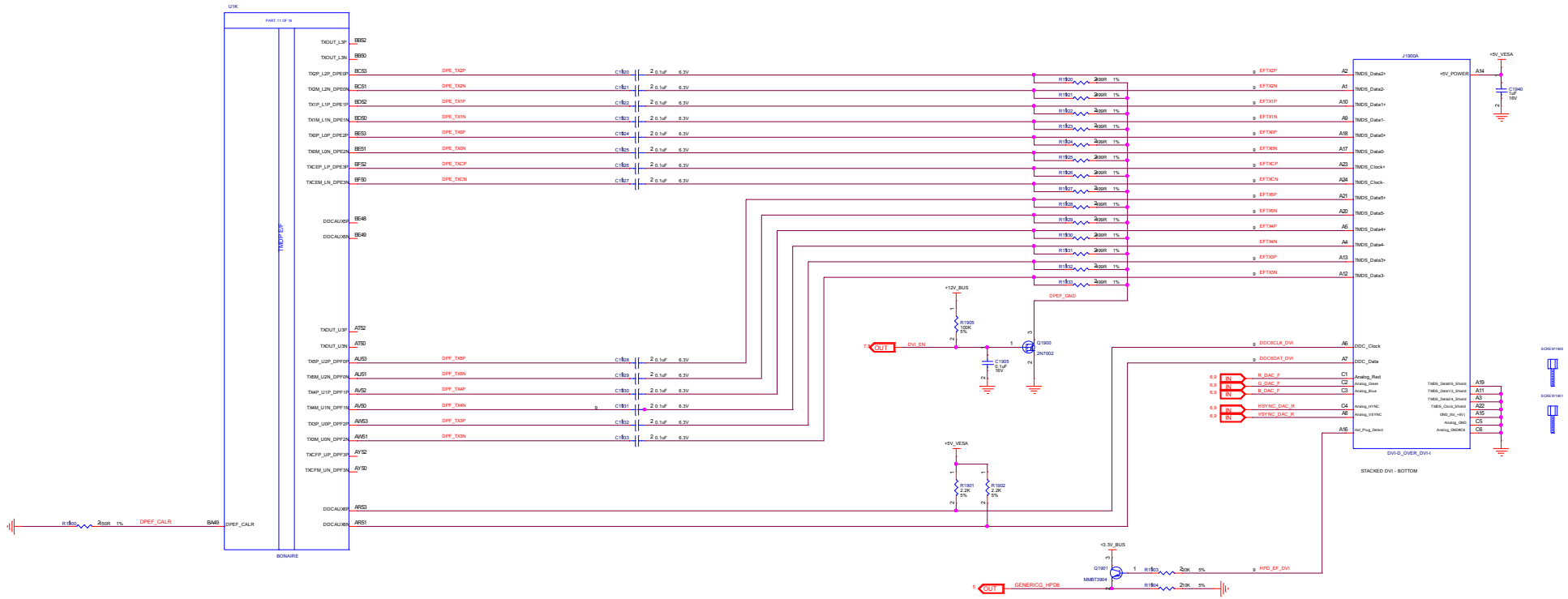
(8) TOBAGO TMDPCD DP HDMI

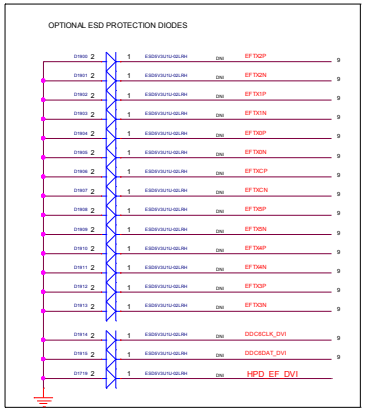


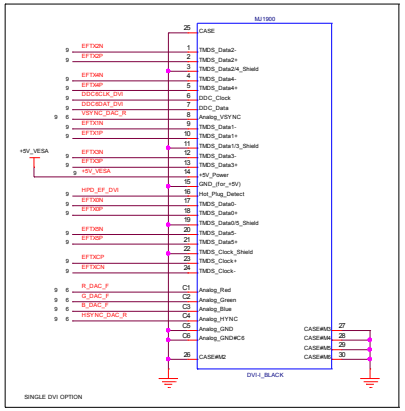


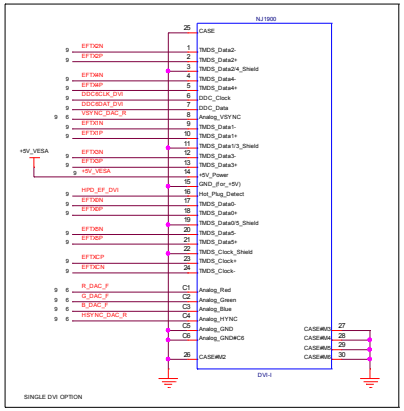


AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: TOBAGO TMDPCD DP HDMI	
DATE: Thu Apr 23 05:54:21 2015	REV: 1.0
SHEET NUMBER: 8 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	TITLE: TOBAGO GDDR5 X32





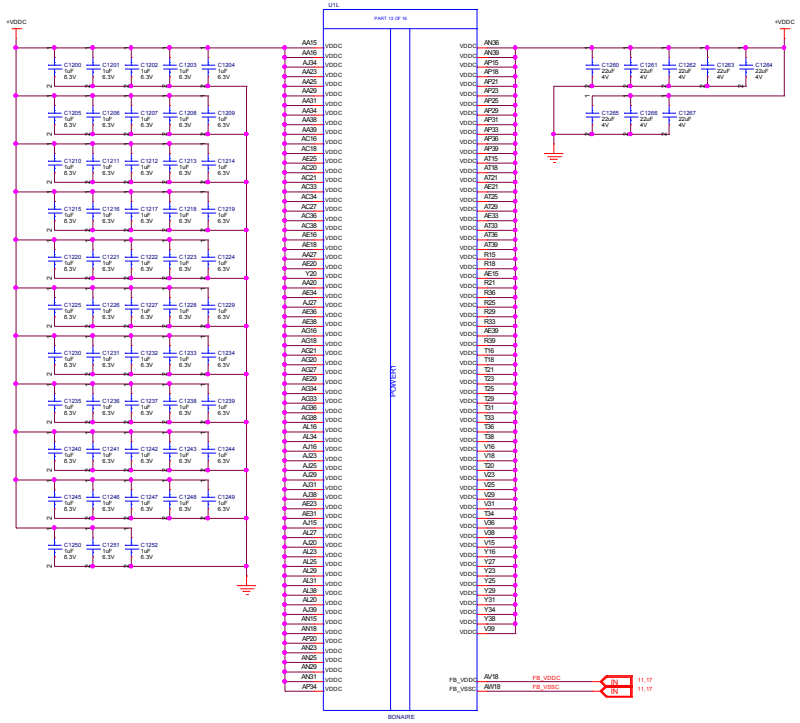


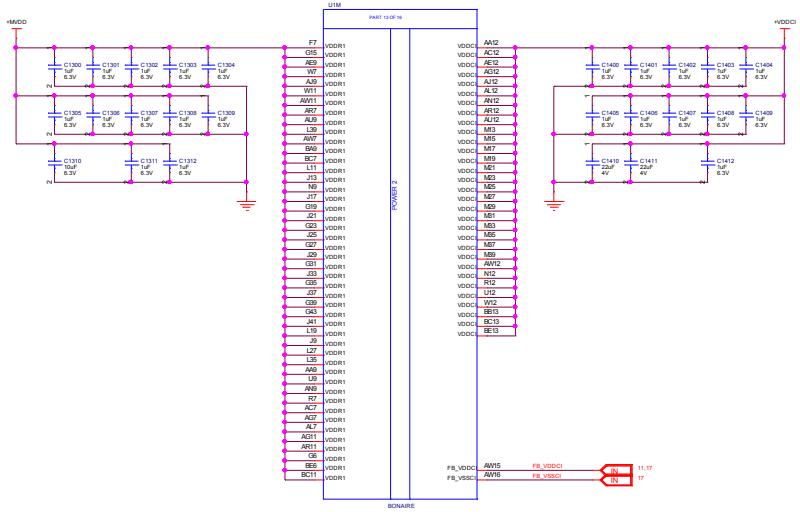


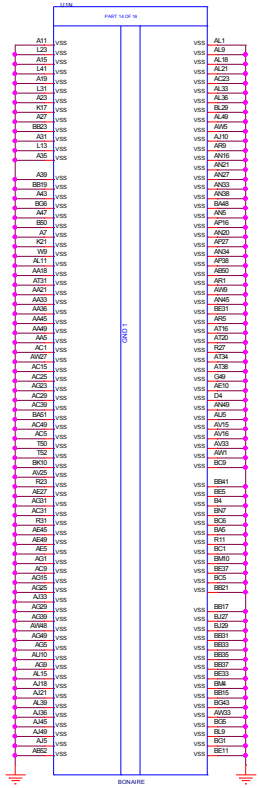
AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

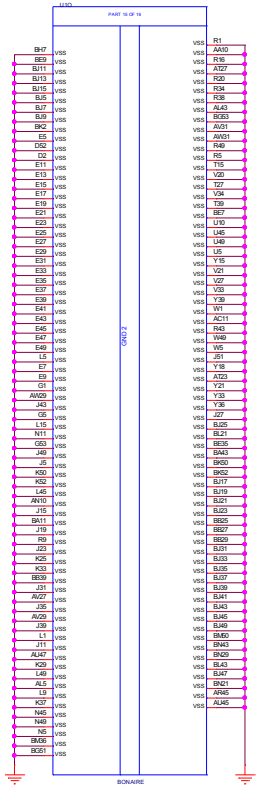
SHEET:	TOBAGO TMDPEF dDVI BOTTOM		
DATE:	Thu Apr 23 05:54:21 2015	REV:	1.0
SHEET NUMBER:	9 OF 19		
DOCUMENT NUMBER:	105_C913xx_00		
NOTES:	NOTE		

TITLE: TOBAGO GDDR5 X32

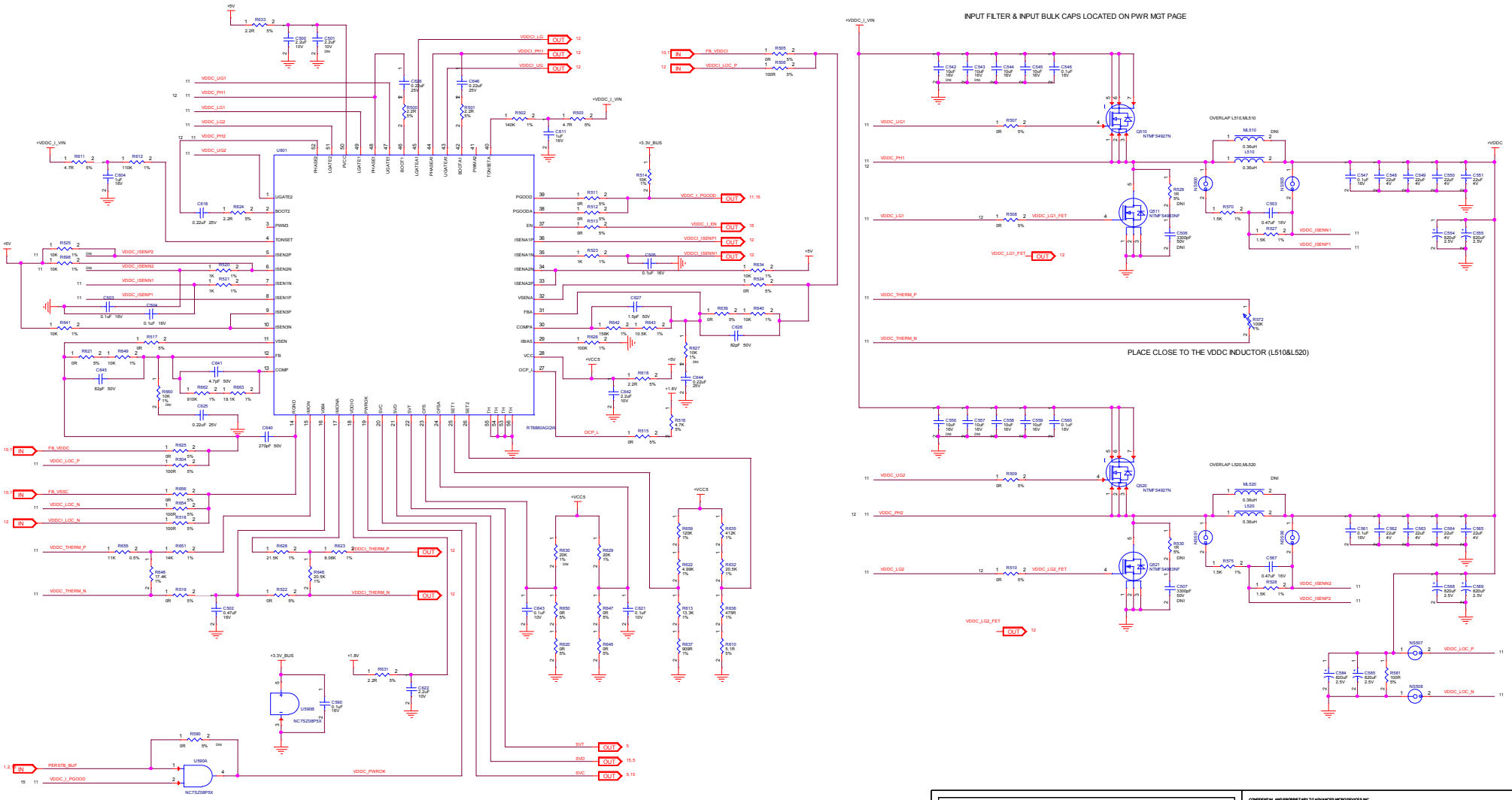






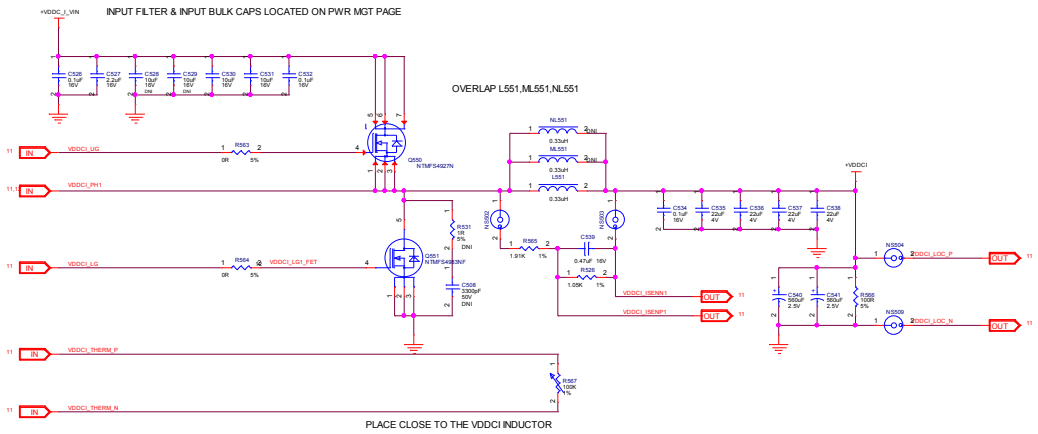


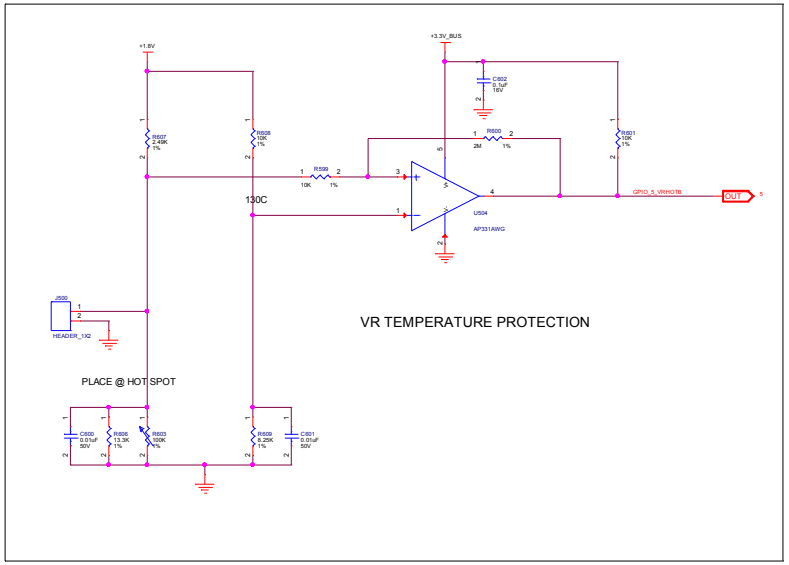
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: TOBAGO POWER GND	
DATE: Thu Apr 23 05:54:22 2015	REV: 1.0
SHEET NUMBER: 10 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	TITLE: TOBAGO GDDR5 X32



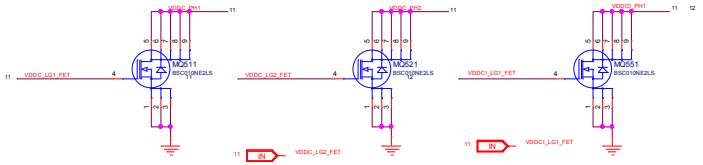
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: VDDC_VDDCI_I	
DATE: Thu Apr 23 05:54:23 2015	REV: 1.0
SHEET NUMBER: 11 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

TITLE: TOBAGO GDDR5 X32



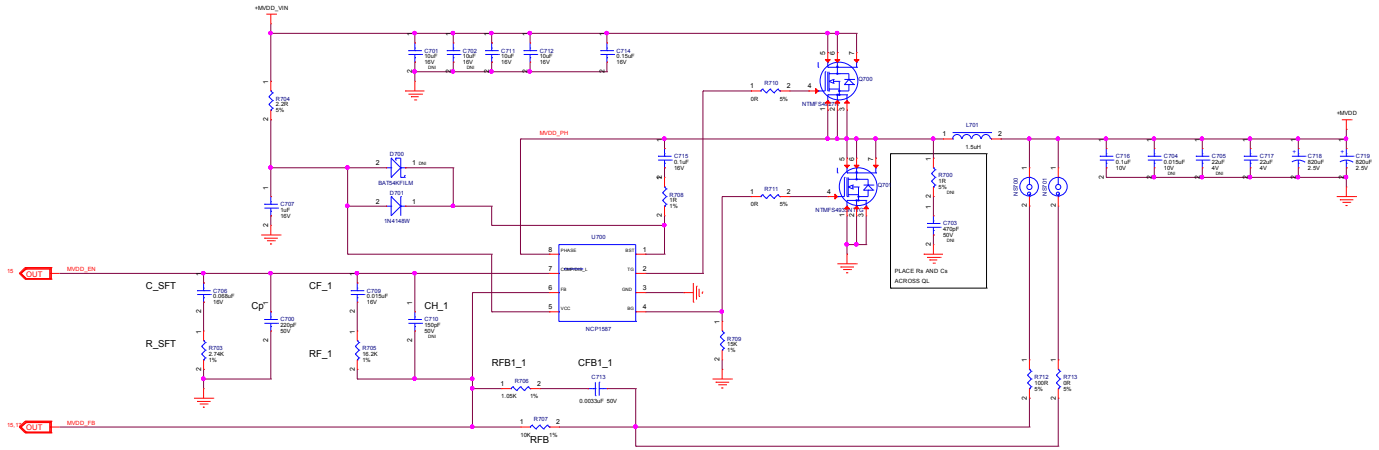


MQ5X1 PARTS ADDED FOR FOOTPRINT COMPATIBILITY WITH MULTIPLE VENDORS.
OVERLAP WITH RESPECTIVE Q5X1.



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: VDDC_VDDCI_II	
DATE: Thu Apr 23 05:54:23 2015	REV: 1.0
SHEET NUMBER: 12 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

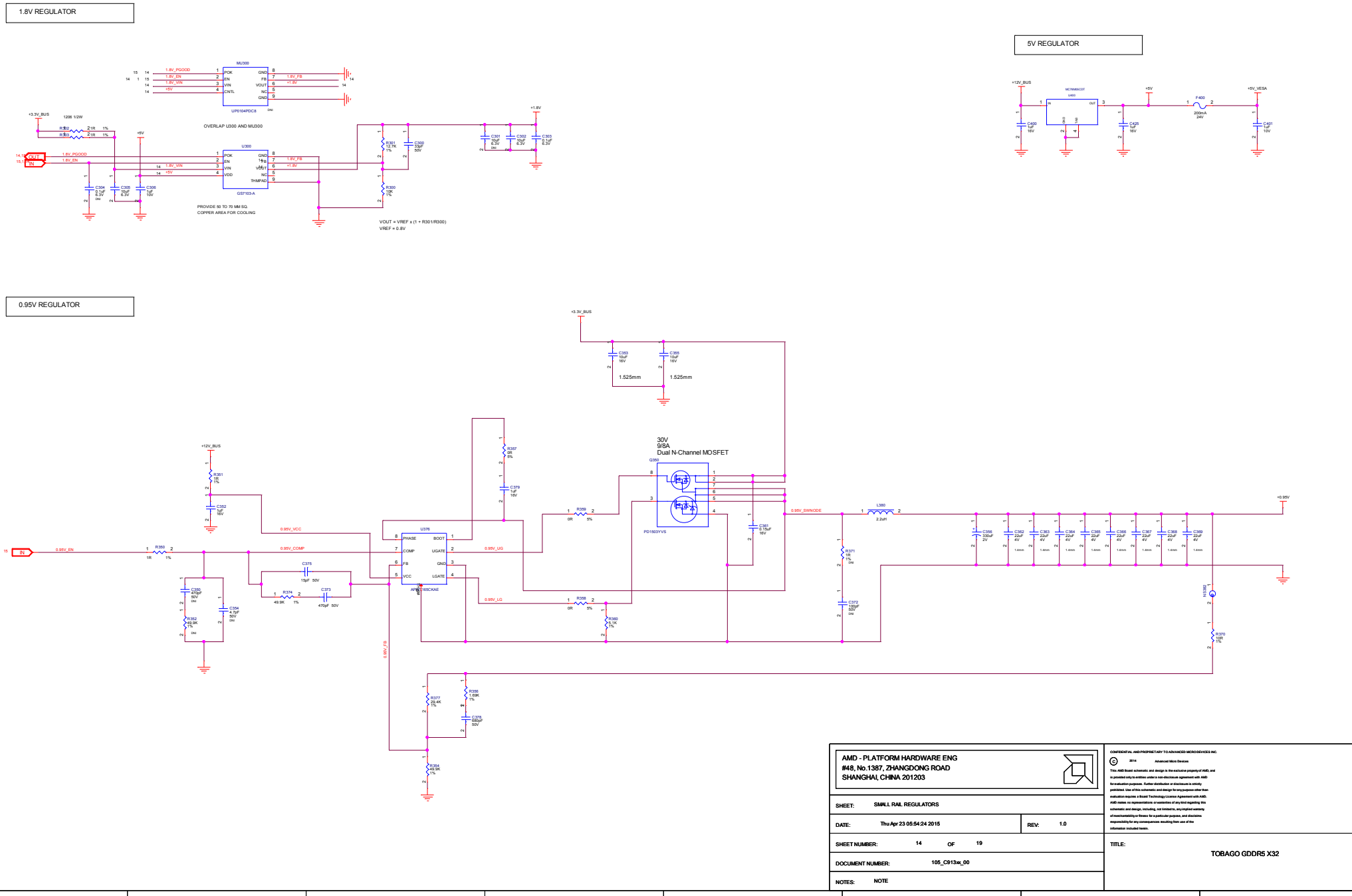
TITLE: TOBAGO GDDR5 X32

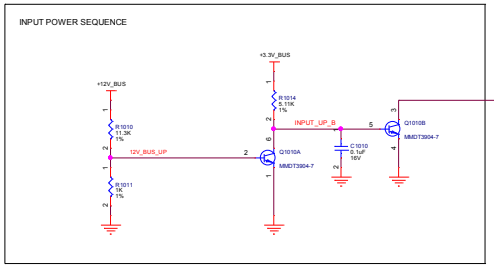


RFB2 is on BFoard Engineer's page.
Default value is 11.3k for 1.5V.
RFB2 = RFB*(Vref/(Vout-Vref))

AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: MVDD	
DATE: Thu Apr 23 05:54:24 2015	REV: 1.0
SHEET NUMBER: 13 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

TITLE: TOBAGO GDDR5 X32

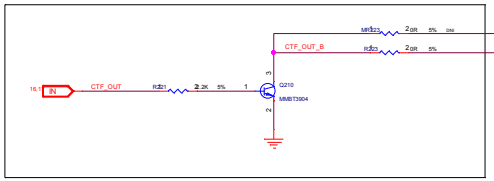

1.8V REGULATOR
5V REGULATOR
0.95V REGULATOR
OVERLAP U300 AND MU300
PROVIDE 50 TO 70 MM SQ.
COPPER AREA FOR COOLING
VOUT = VREF x (1 + R301/R300)
VREF = 0.8V
30V
9/8A
Dual N-Channel MOSFET
AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203
SHEET: SMALL RAIL REGULATORS
DATE: Thu Apr 23 05:54:24 2015
REV: 1.0
SHEET NUMBER: 14 OF 19
DOCUMENT NUMBER: 105_C913xx_00
NOTES: NOTE
TITLE: TOBAGO GDDR5 X32



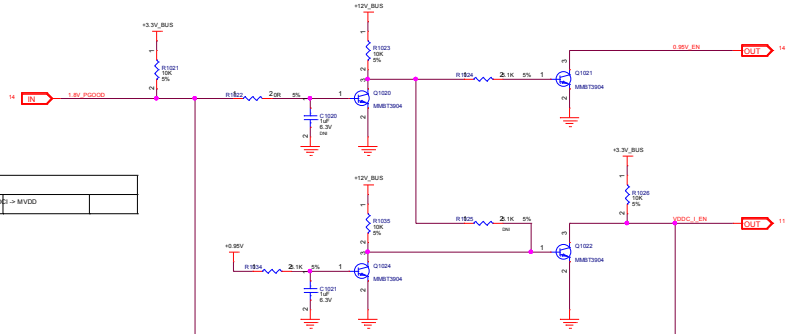
ENABLE THRESHOLD

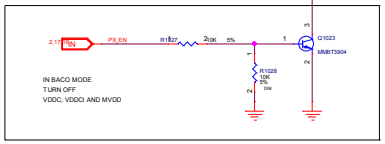
+1.8V: > 1.4V
+0.95V: FLOAT
+VDDC/+VDDCI: >2.0V
+MVDD: FLOAT

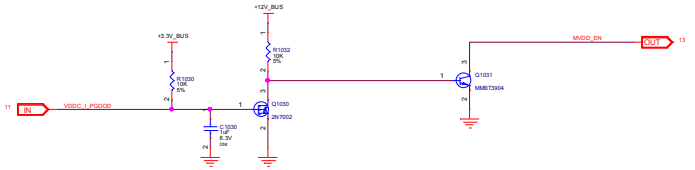
POWER UP SEQUENCE			
BUS RAILS (3.3V/12V UP) -> +1.8V -> 0.95V		-> VDDC/VDDCI -> MVDD	

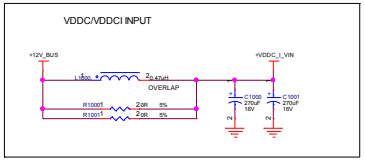


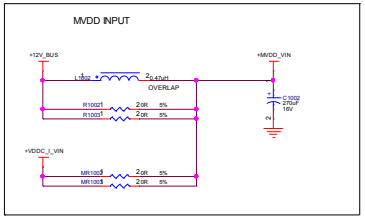
INTERNAL CTF LATCH - 1.8V VDDCT REQUIRED

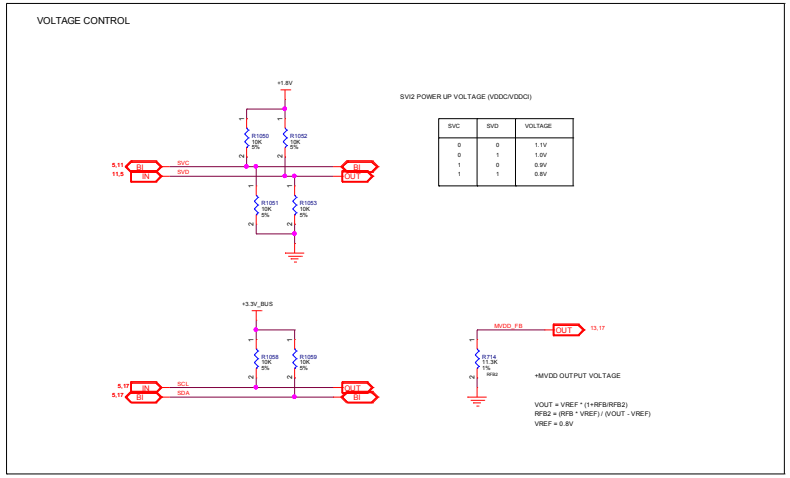








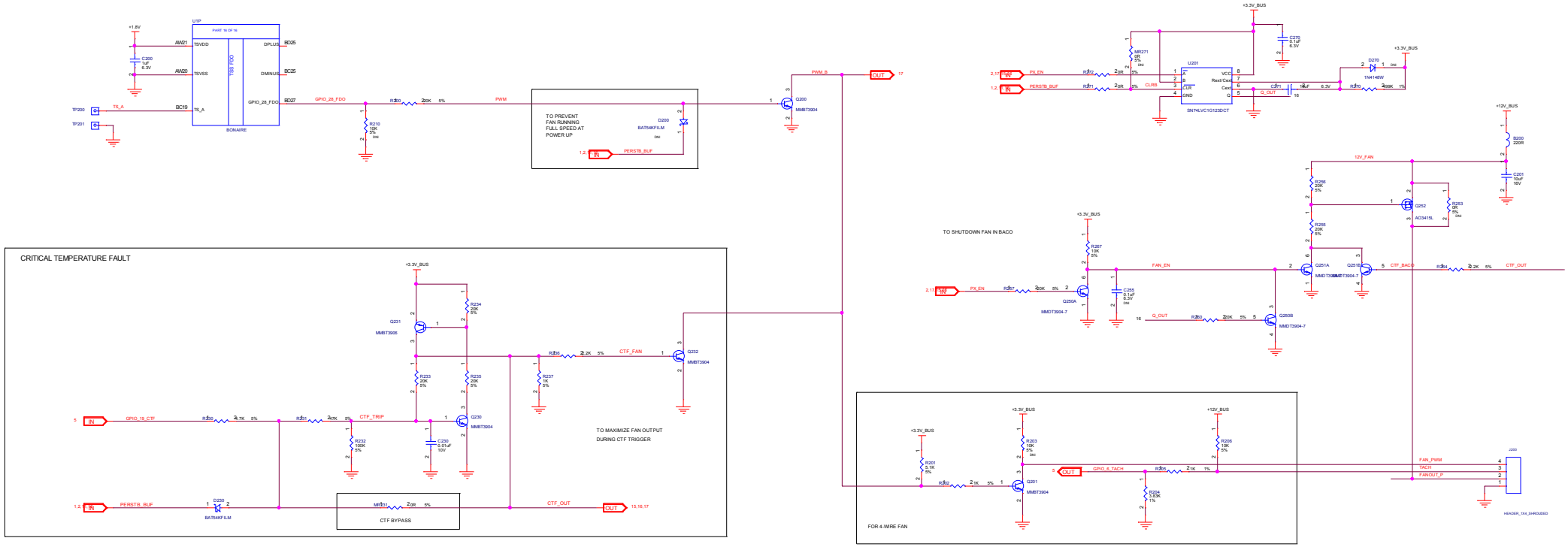


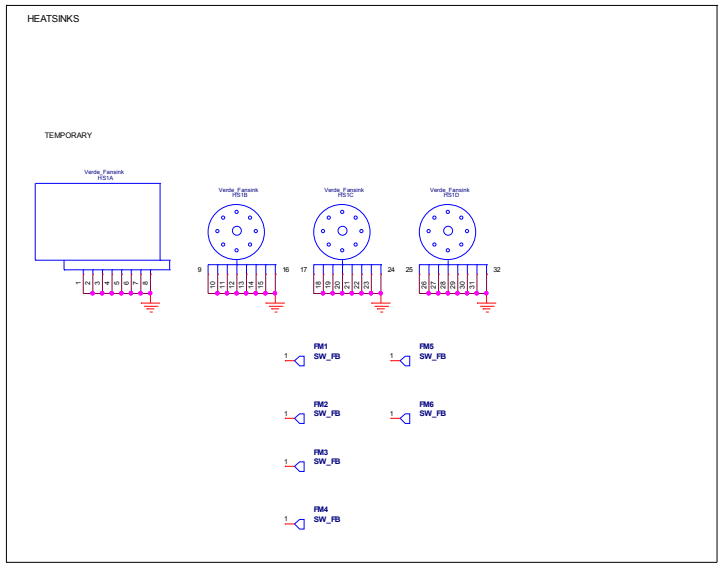


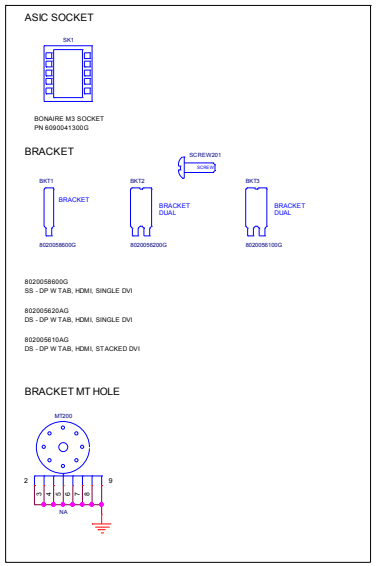
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: POWER MANAGEMENT	
DATE: Thu Apr 23 05:54:25 2015	REV: 1.0
SHEET NUMBER: 15 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

TITLE:

TOBAGO GDDR5 X32







TOP
Single end
Memory
48 ohm +/- 5 ohm
4.33 mils

TOP
Different
PCIE
85 ohm +/- 10 %
4.41 mils / 7.4 mils

L3
Different
TMDS
85 ohm +/- 10 %
4.61 mils / 7.2 mils

Bottom
Different
Memory clock
80 ohm +/- 10 %
4.33 mils / 6.3 mils

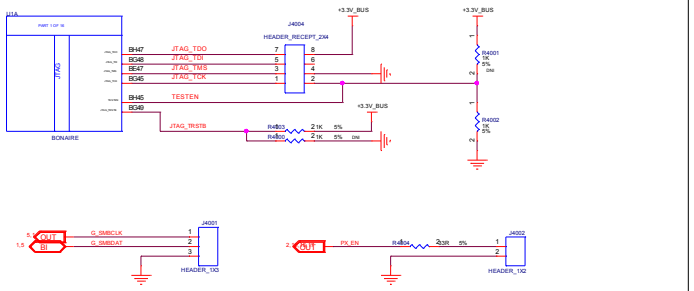
L3
Single end
Memory
48 ohm +/- 5 ohm
4.33 mils

Bottom
Single end
Memory
48 ohm +/- 5 ohm
4.33 mils

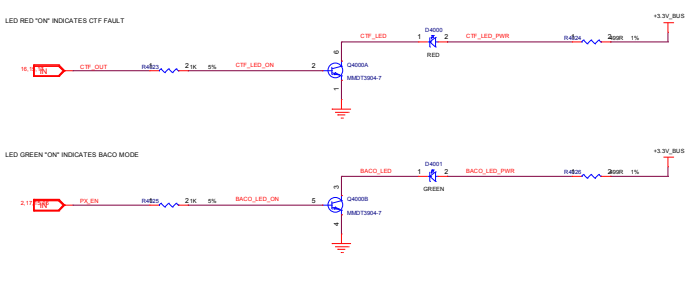
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: MECH AND THERM MANAGEMENT	
DATE: Thu Apr 23 05:54:25 2015	REV: 1.0
SHEET NUMBER: 16 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

TITLE: TOBAGO GDDR5 X32

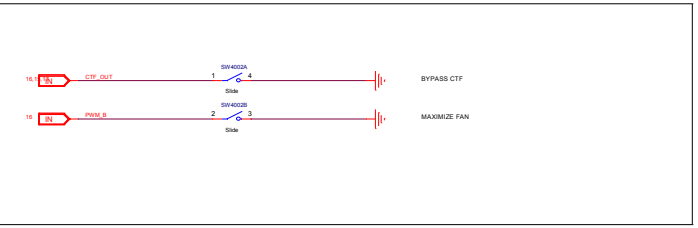
JTAG



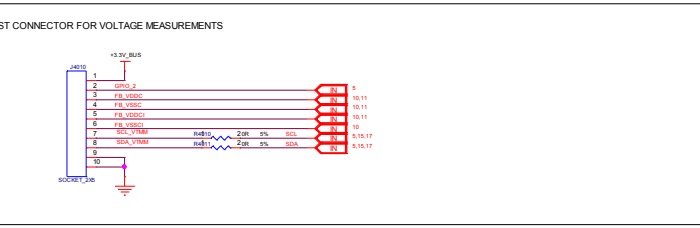
LED LIGHTS



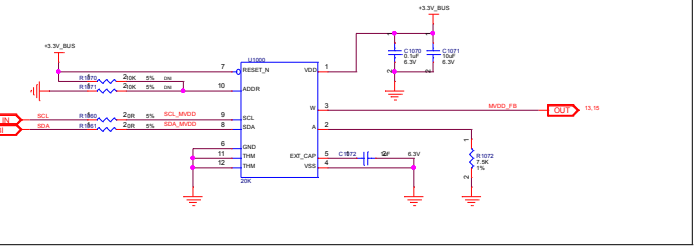
SWITCHES



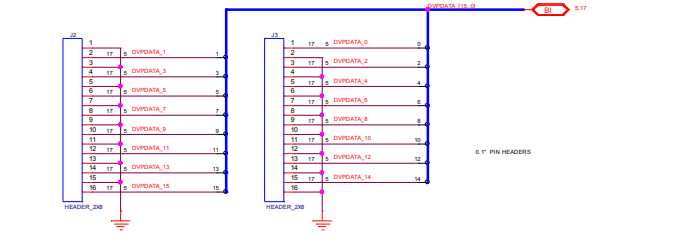
VTMM - TEST CONNECTOR FOR VOLTAGE MEASUREMENTS



DIGITAL POT

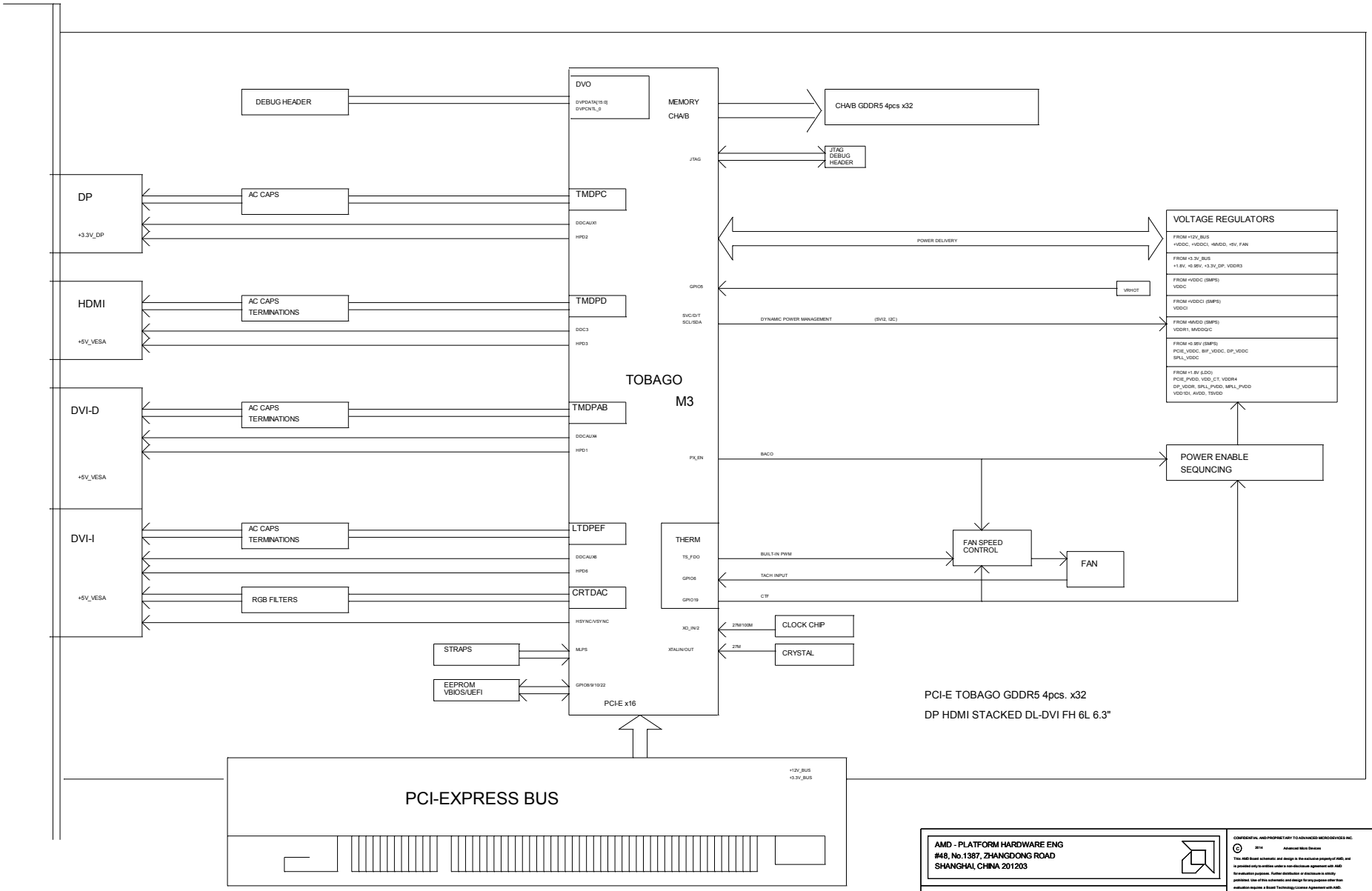


DEBUG BUS



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: DEBUG CIRCUITS	
DATE: Thu Apr 23 05:54:25 2015	REV: 1.0
SHEET NUMBER: 17 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

TITLE: TOBAGO GDDR5 X32



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: BLOCK DIAGRAM	
DATE: Thu Apr 23 05:54:26 2015	REV: 1.0
SHEET NUMBER: 18 OF 19	
DOCUMENT NUMBER: 105_C913xx_00	
NOTES: NOTE	

TITLE: TOBAGO GDDR5 X32

AMD

TITLE: TOBAGO GDDR5 X32

DOCUMENT NUMBER: 105_C913xx_00

DATE: Mon Jan 26 02:32:37 2015

SHEET NUMBER: 19 OF 19

REV: 1.0

REVISION HISTORY

ENGINEER: PEAK DONG

NOTES: NOTE

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
0	00A	09/19/2014	INITIAL DESIGN
1	00B	11/25/2014	CORRECTING VCCSTG->VCCS
2	00	1/23/2015	RELEASED TO 00