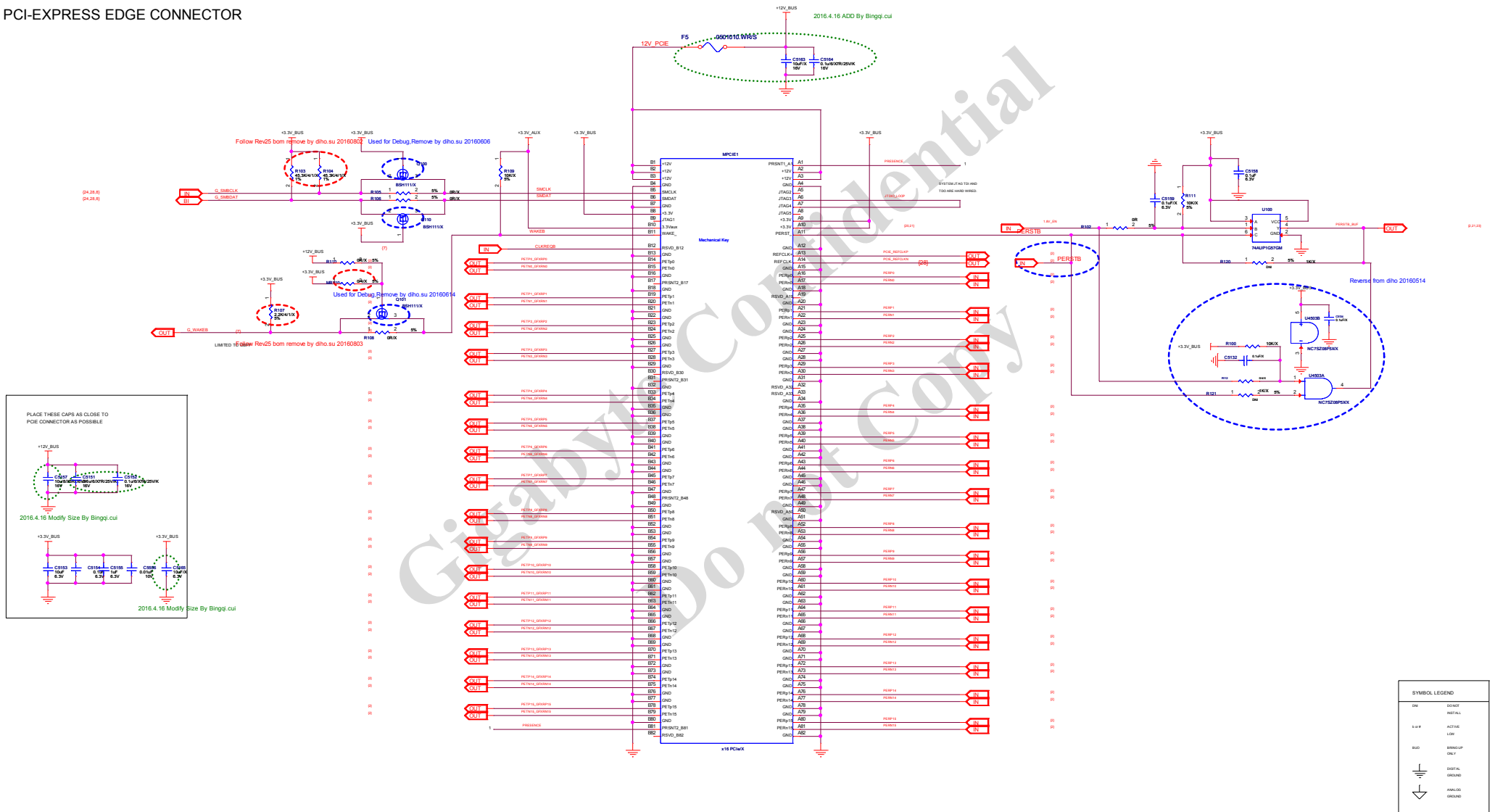
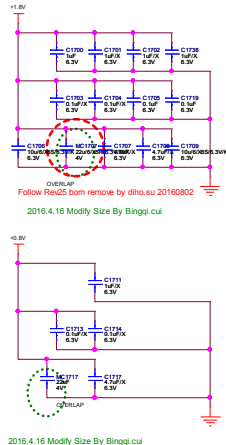


(1) PCI-EXPRESS EDGE CONNECTOR

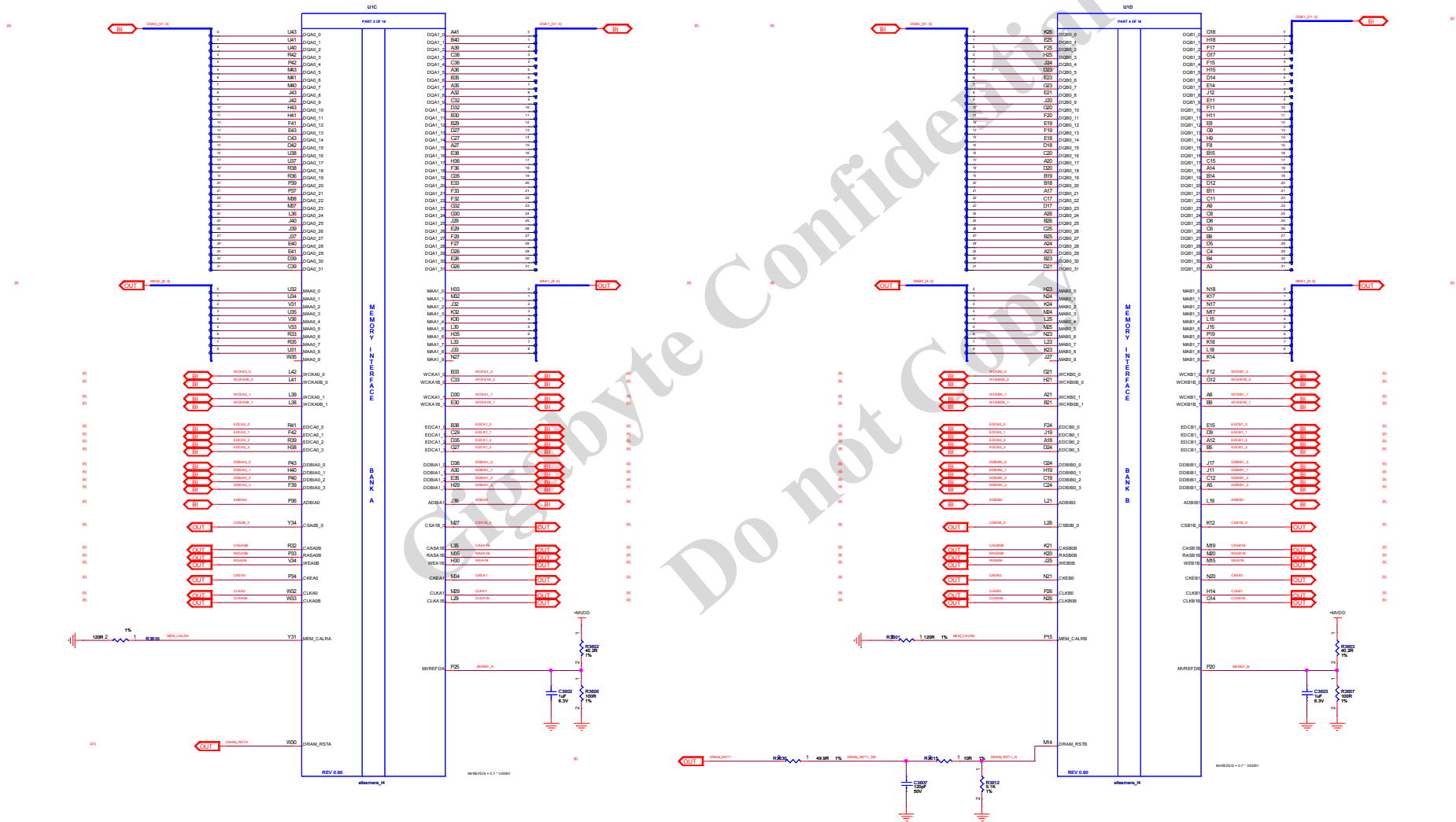


GIGABYTE			
Title PCI Express			
Size	Document Number		Rev
Custom	GV-RX580GAMING-8GD		1.0
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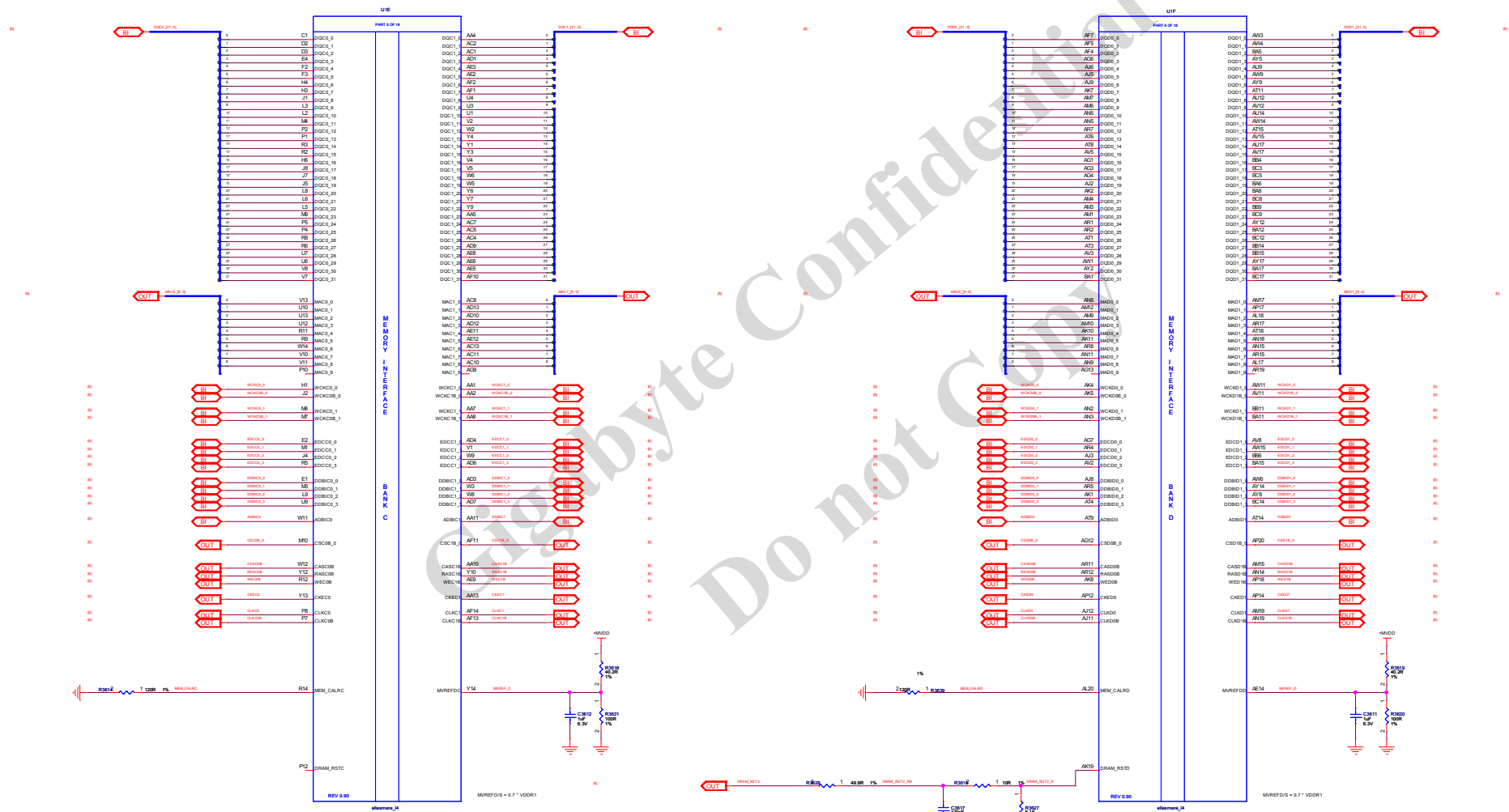
(2) ELLESMERE PCIE INTERFACE



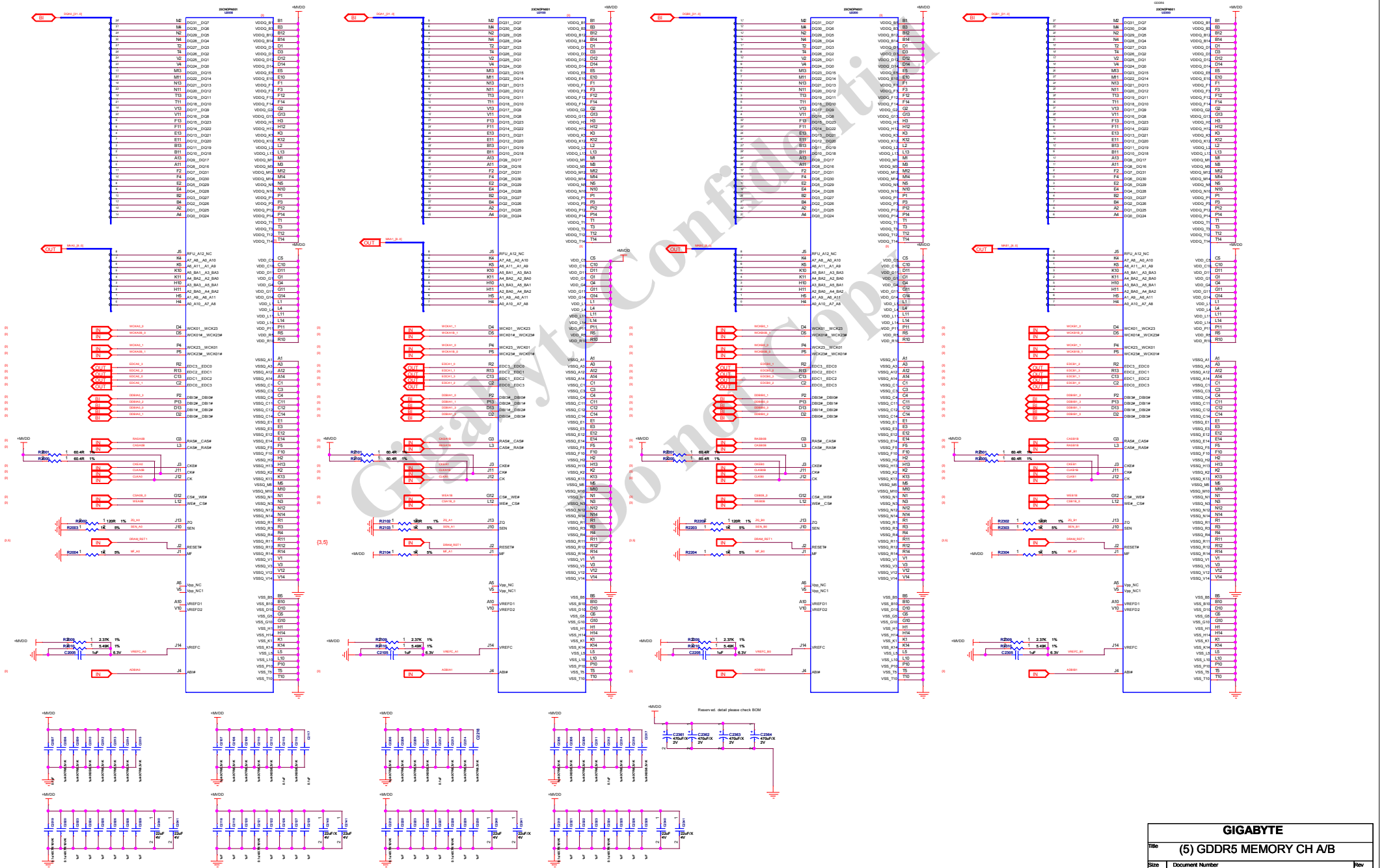
(3) ELLESMERE MEM INTERFACE CH A/B



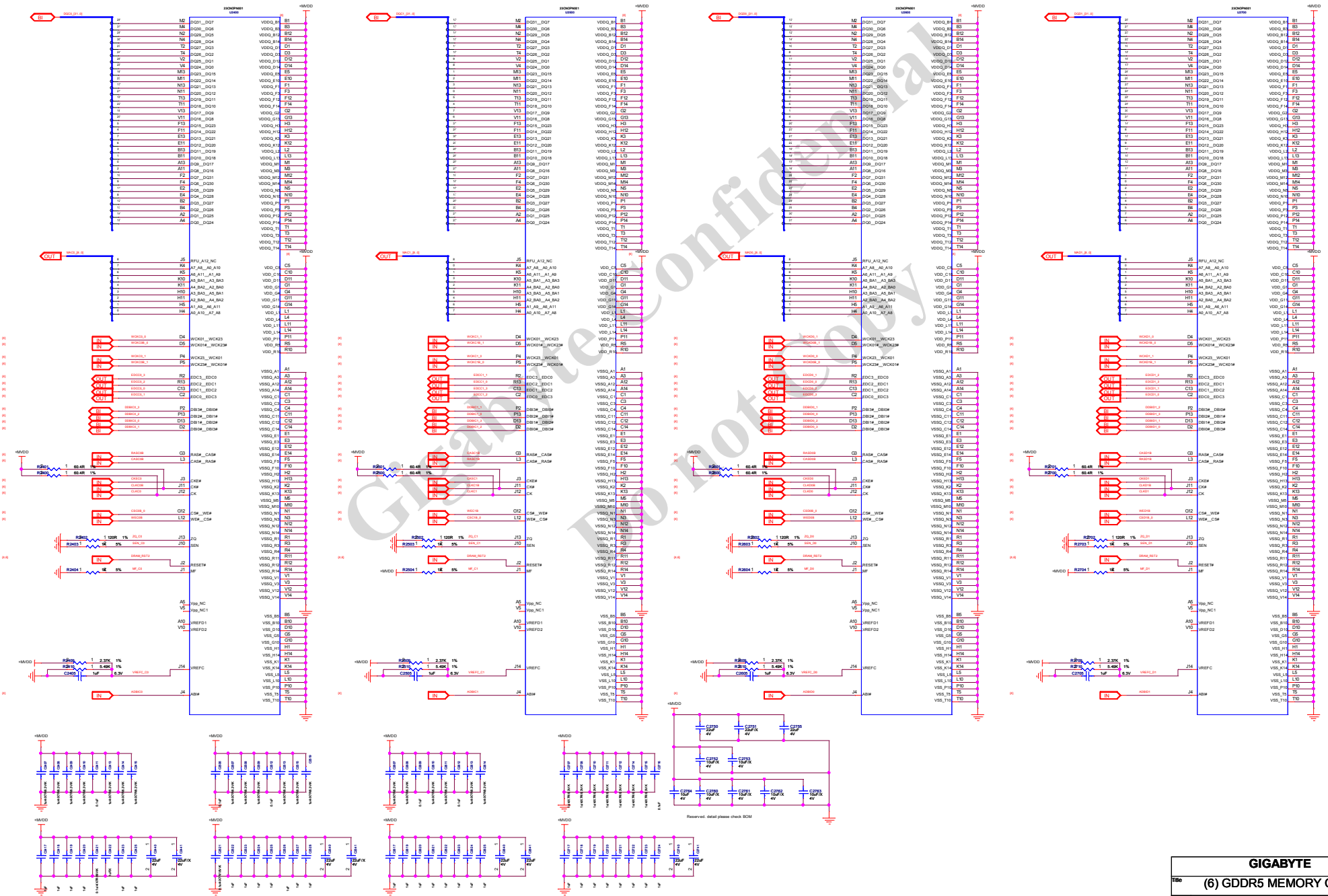
(4) ELLESMERE MEM INTERFACE CH C/D



(5) GDDR5 MEMORY CH A/B

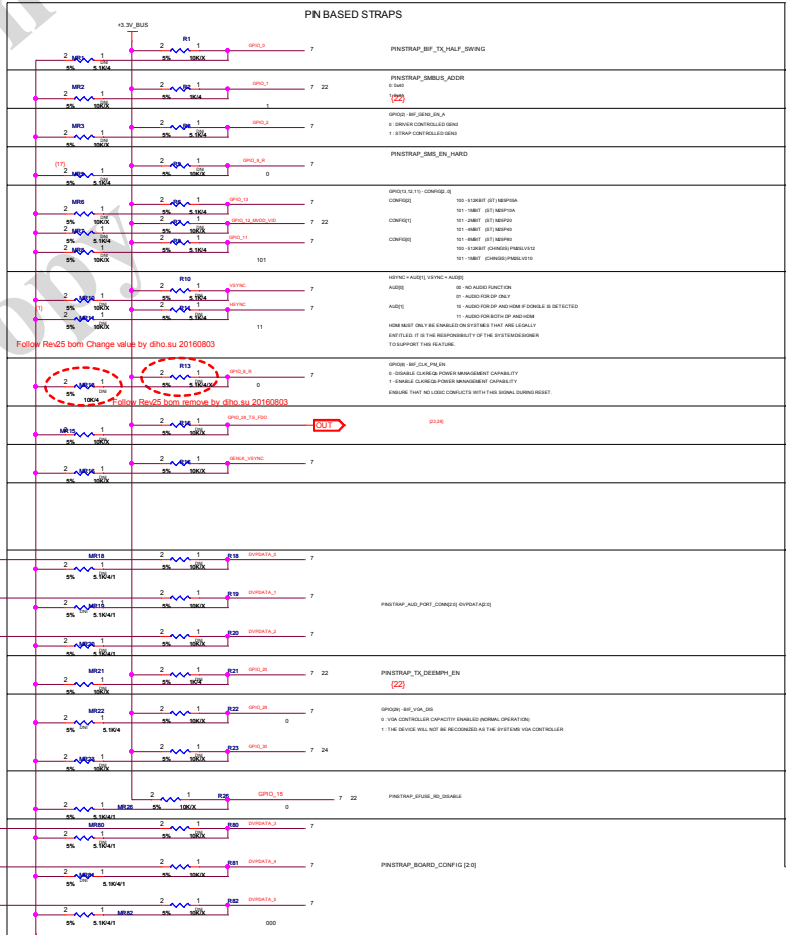
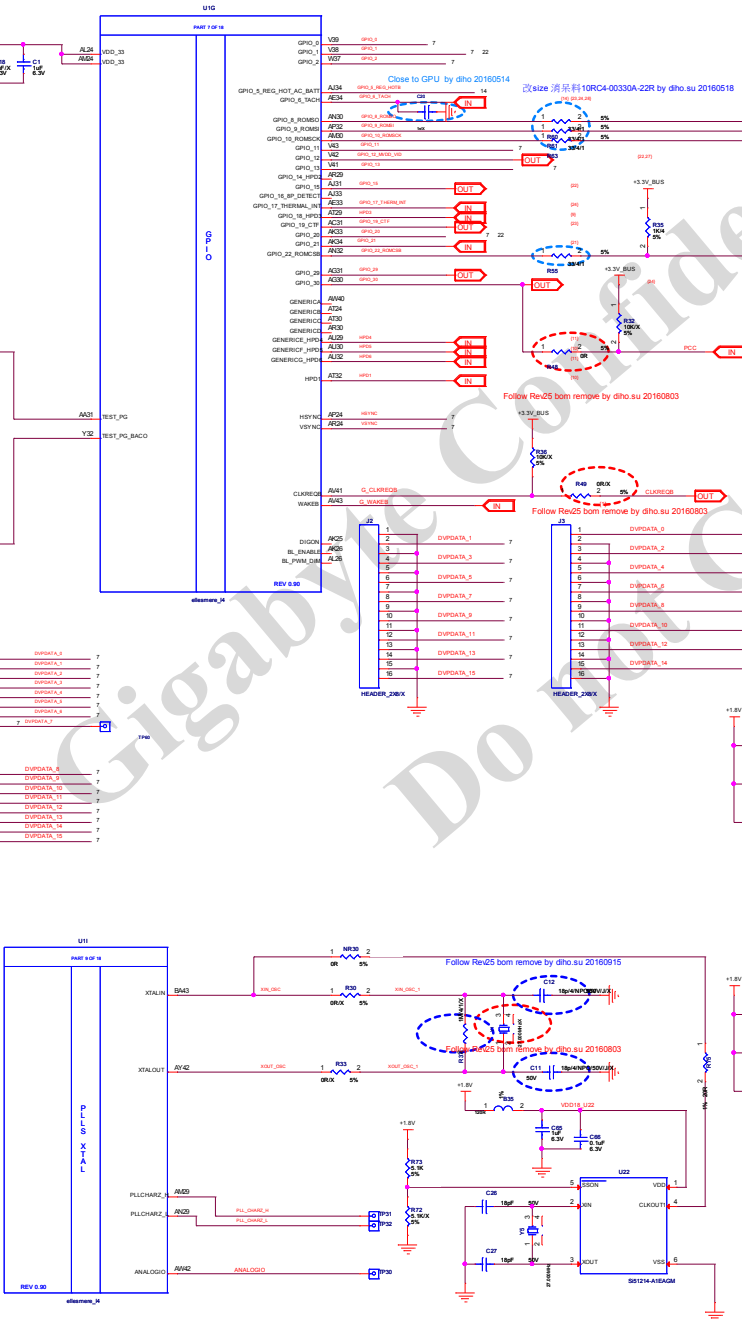
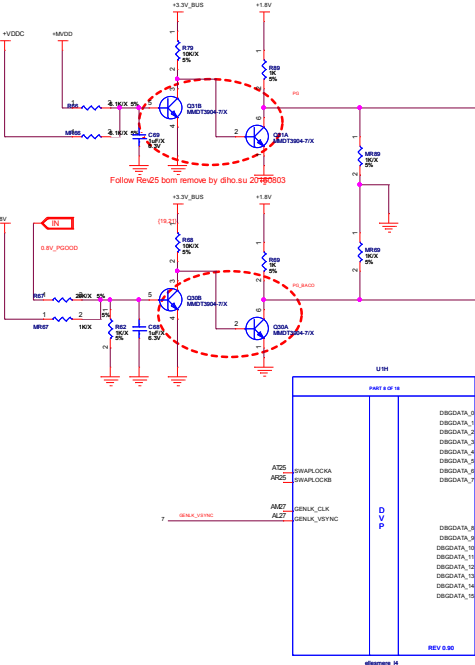


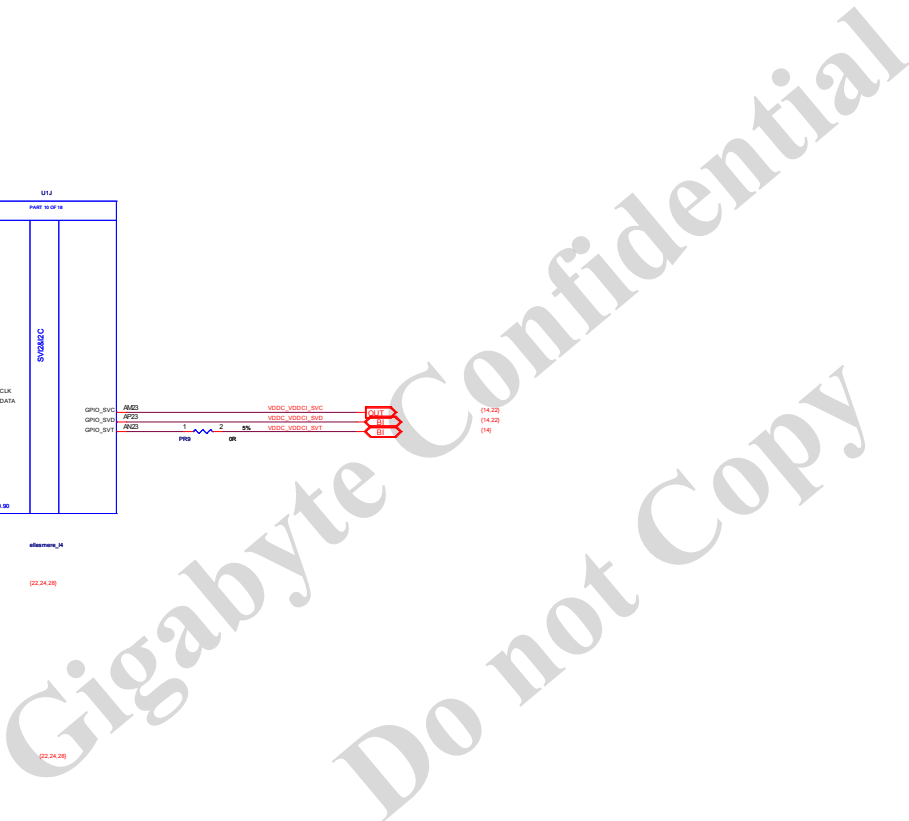
(6) GDDR5 MEMORY CH C/D



(7) ELLESMERE GPIO STRAP CF XTAL

SCUDBG BUS		
IO ADDRESS	FUNCTION	DEVICE
DDCVGA BUS		
IO ADDRESS	FUNCTION	DEVICE
0x00	EXT TEMP SENSOR	LM8003

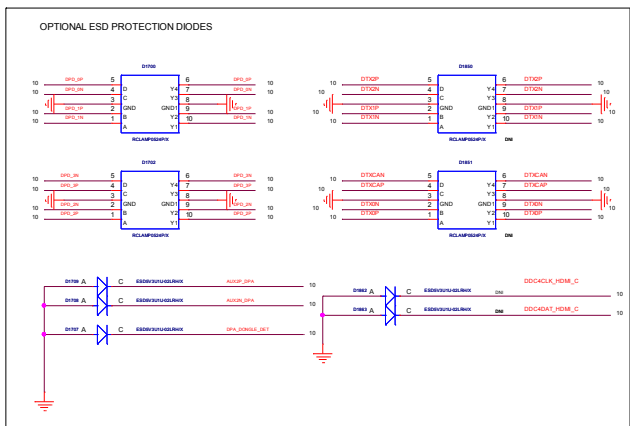
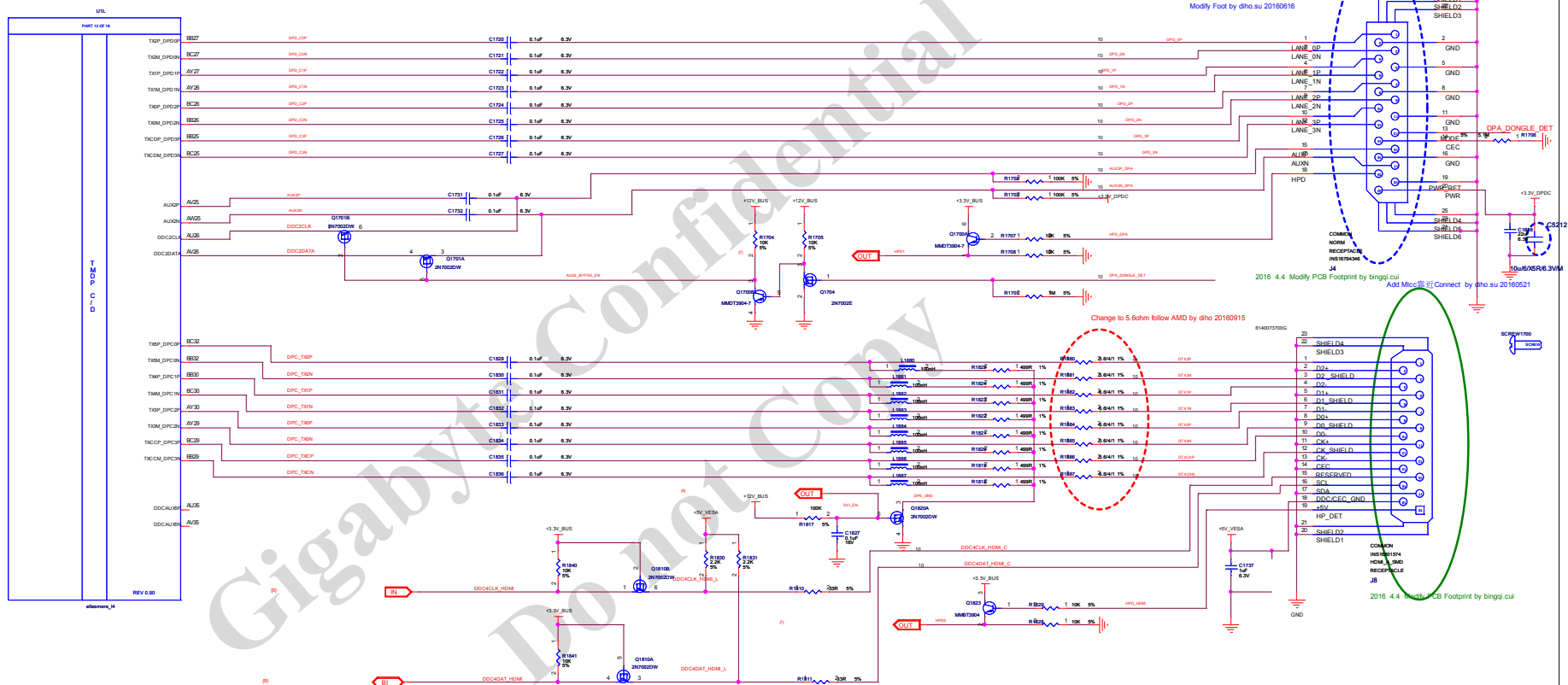


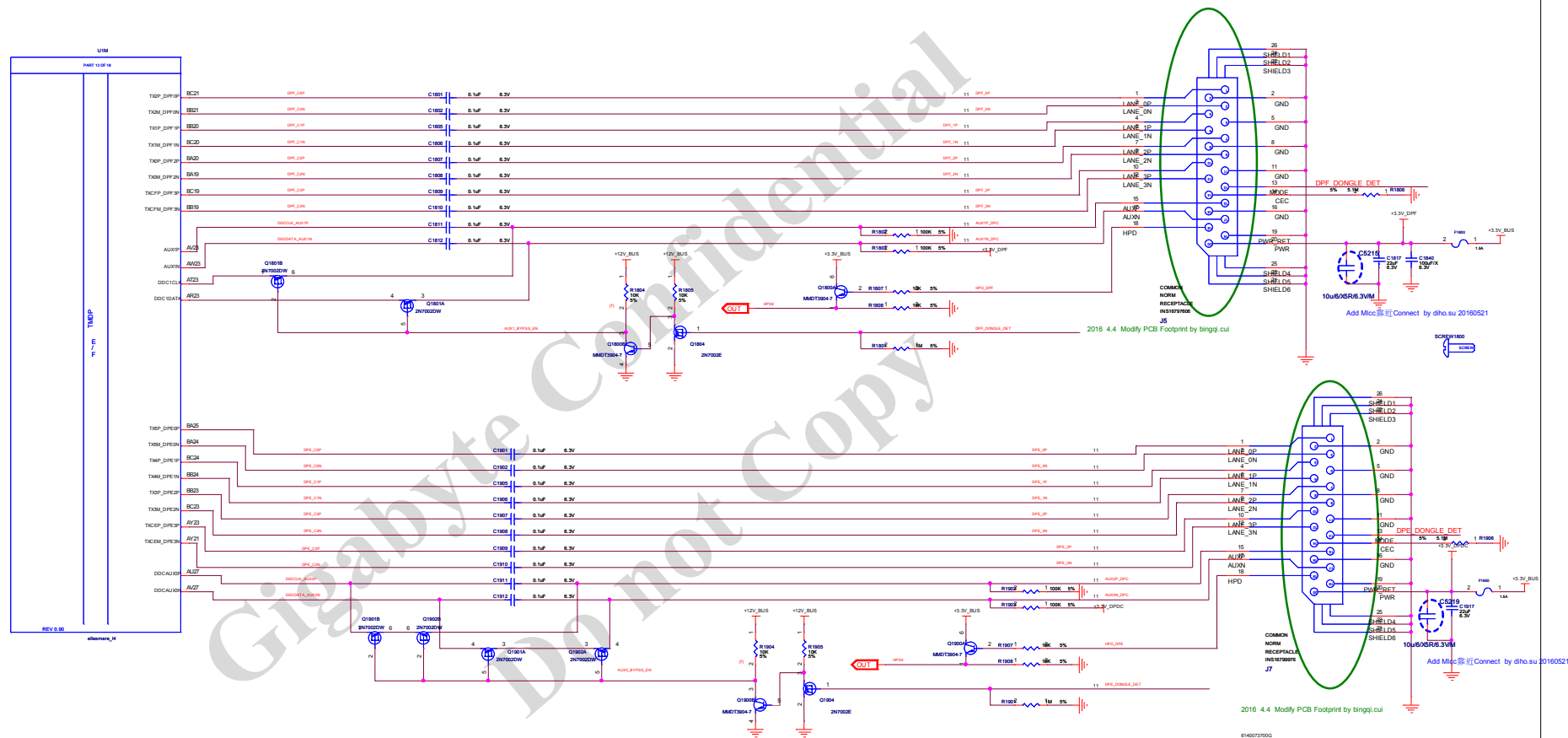
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GIGABYTE			
Title	ELLESMERE DAC1 LOCK		
Size	Document Number		Rev
Custom	GV-RX580GAMING-8GD		1.
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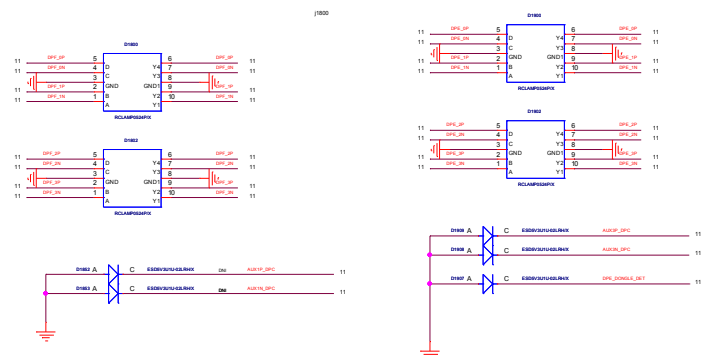
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GIGABYTE			
Title: ELLESMERE TMDP A/B			
Size Custom	Document Number GV-RX580GAMING-8GD		Rev 1.0
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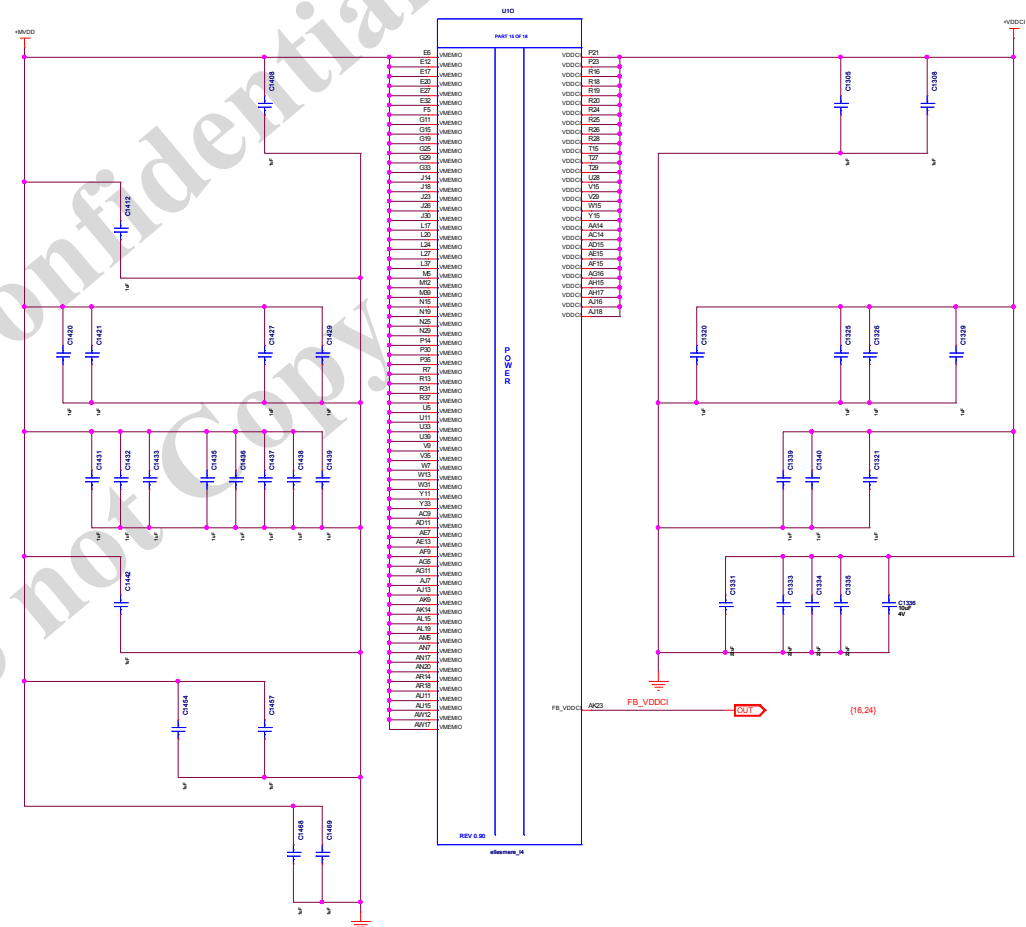
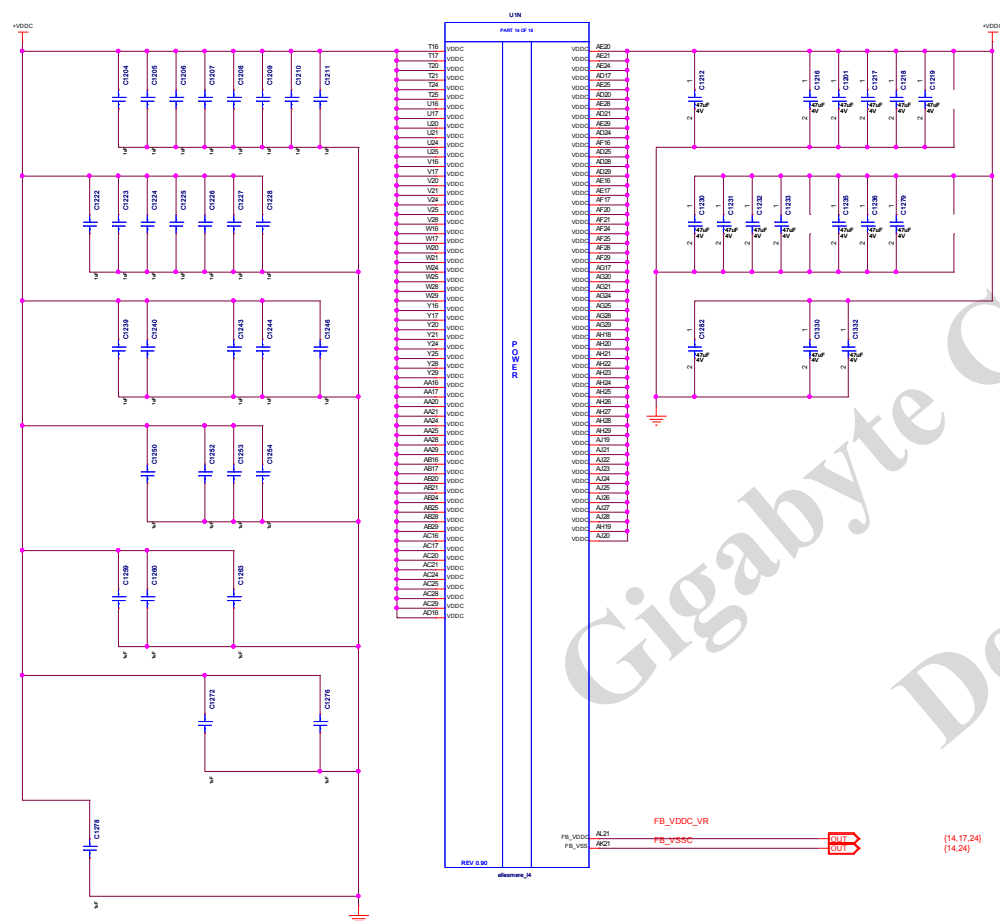


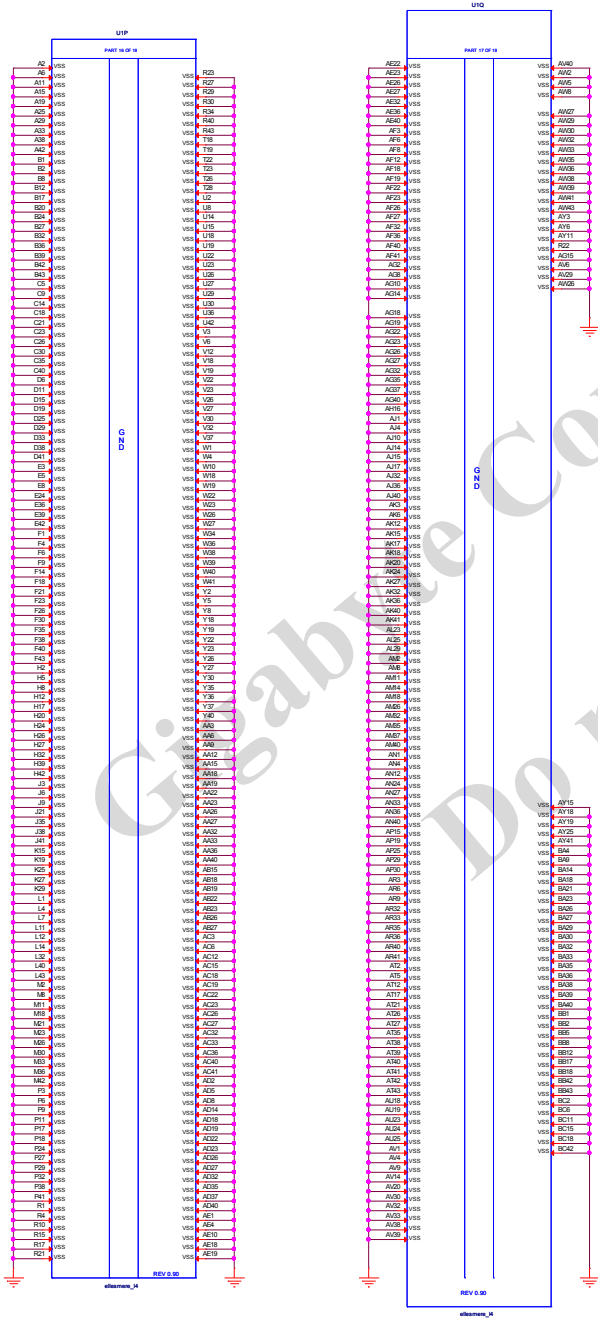
OPTIONAL ESD PROTECTION DIODES

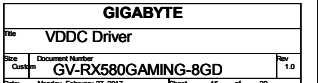


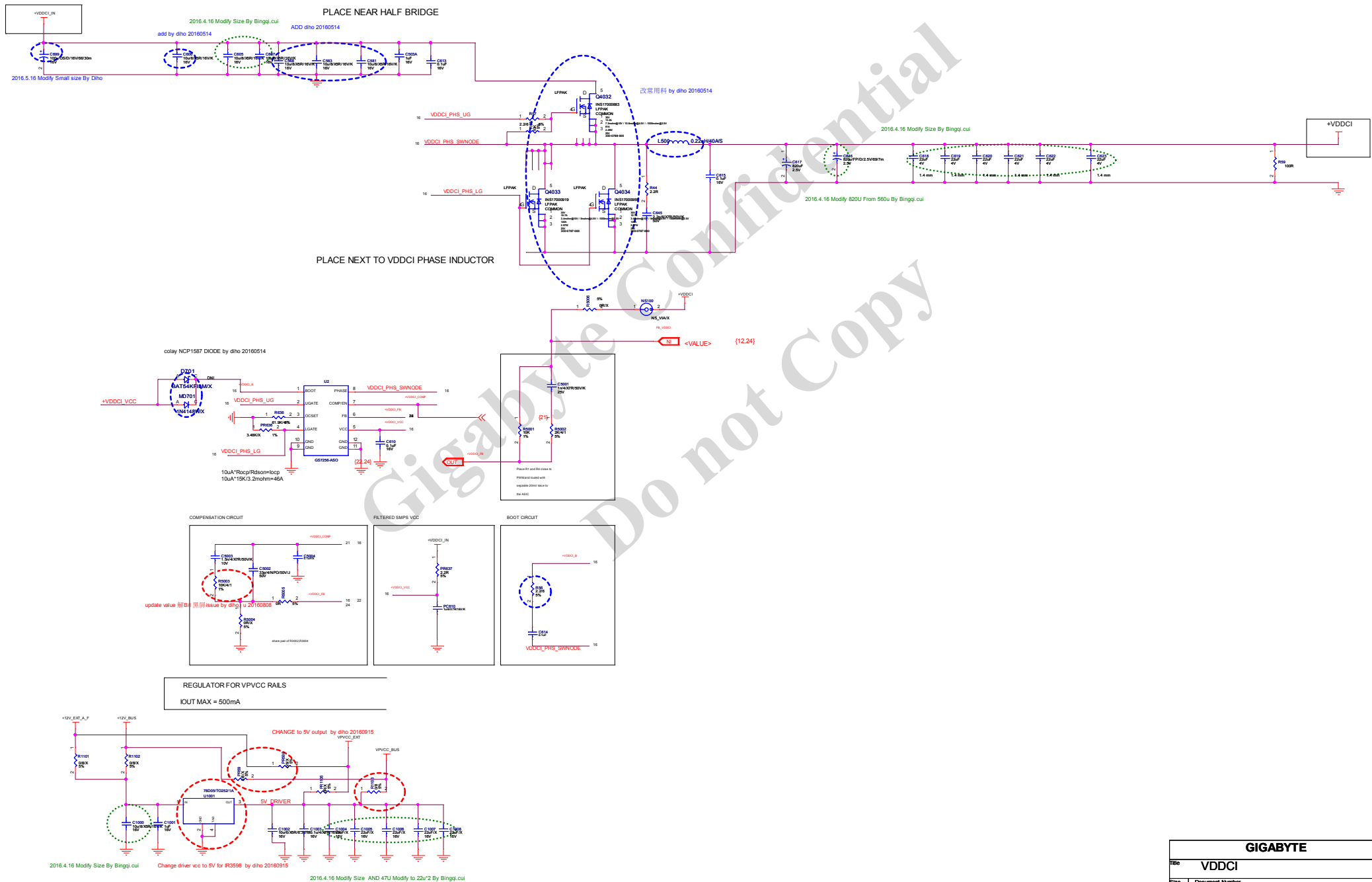
GIGABYTE			
Title ELLESMERE LVTMDP E/F			
Size	Document Number		Rev
Custom	GV-RX580GAMING-8GD		1.0
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(12) ELLESMERE POWER

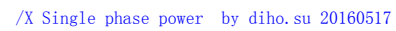


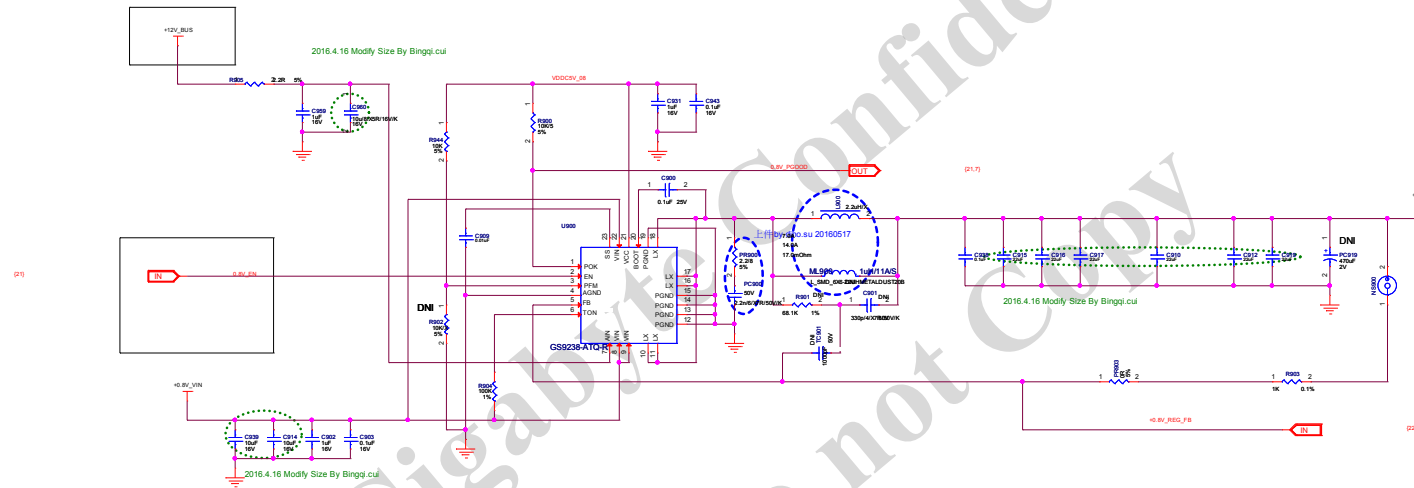






GIGABYTE			
File	VDDCI		
Size	Document Number	Rev	
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-2%

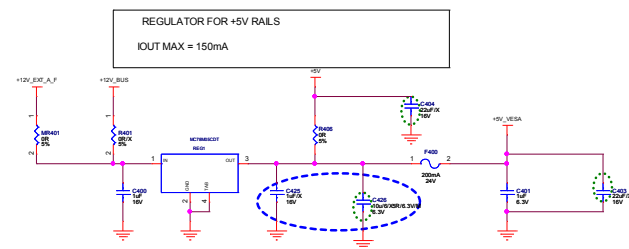
IOUT = 1.3A RMS MAX

The circuit diagram shows a current source with a feedback loop. The output current IOUT is 1.3A RMS MAX. The feedback loop is formed by a resistor network (R302, R301, R303) and a capacitor (C304). The feedback signal is compared to a reference voltage (VREF) at the inverting input of the op-amp. The output of the op-amp drives the current source. The feedback loop is highlighted with a green dashed circle. The feedback signal is also compared to a reference voltage (VREF) at the inverting input of the op-amp. The output of the op-amp drives the current source. The feedback loop is highlighted with a green dashed circle.

Modify size to 0603 save cost by dtho 20160315

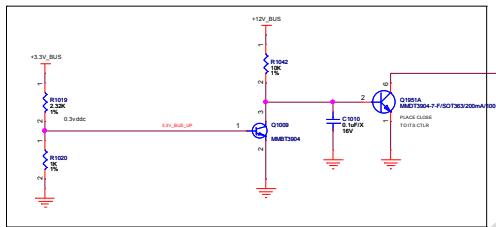
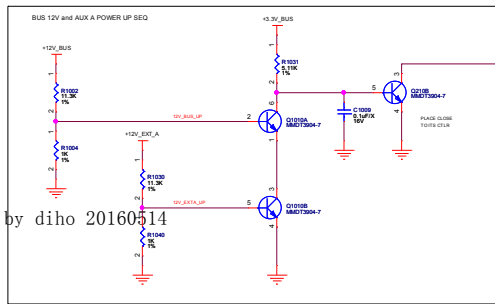
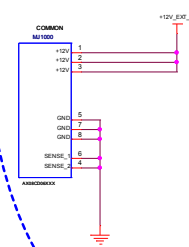
2016.4.16 Modify Size By Bingq.cui

VOUT = Vref x (1 + RS/R4)

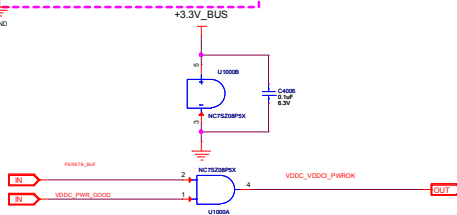
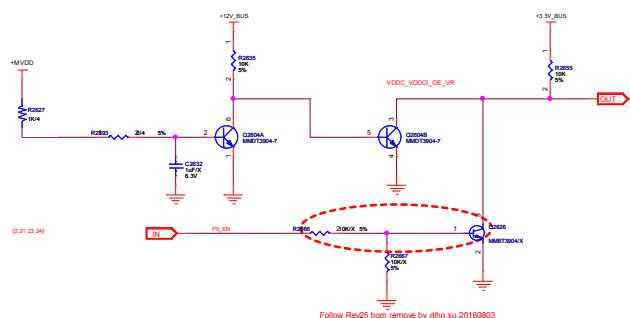
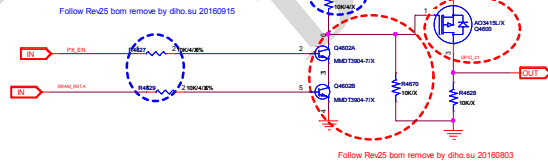
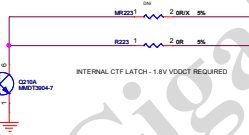
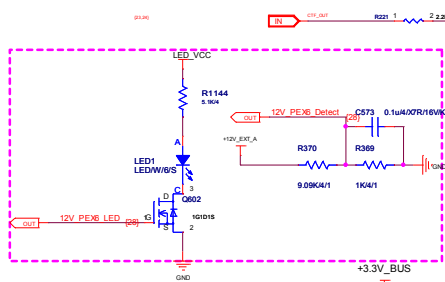
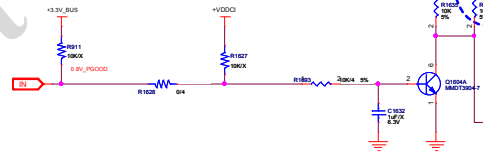
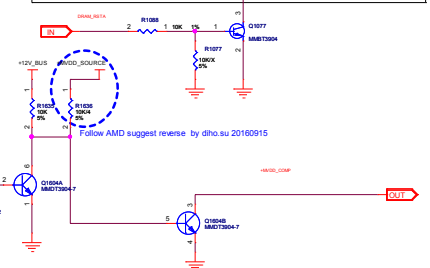
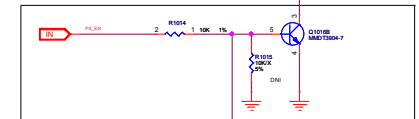
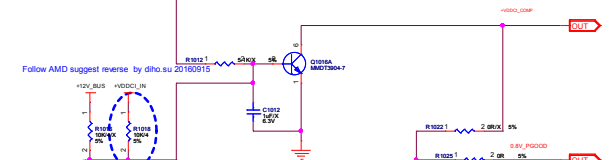
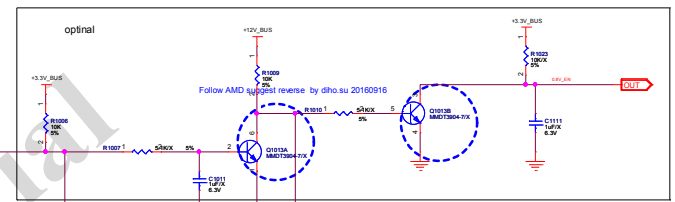
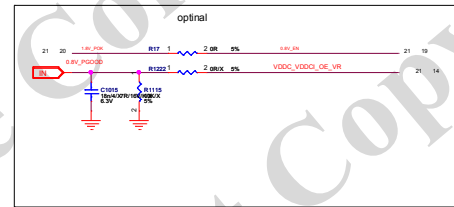


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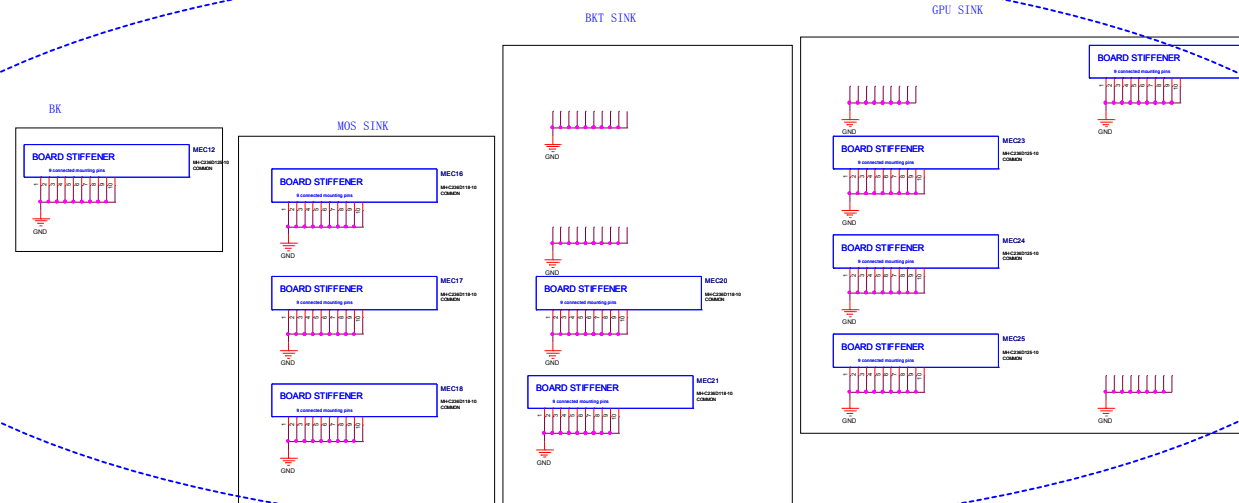
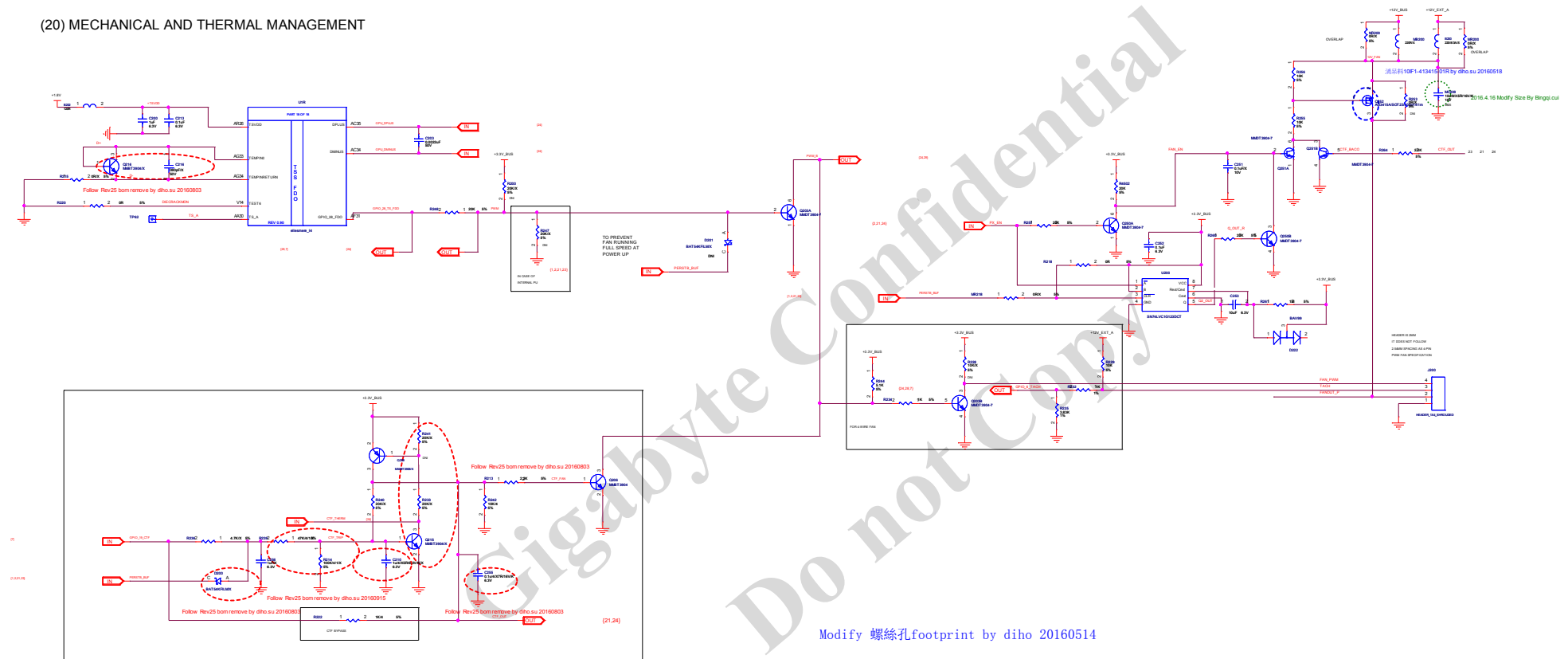
(19) POWER MANAGEMENT



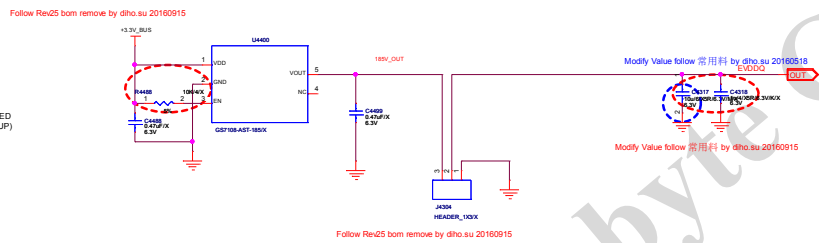
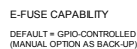
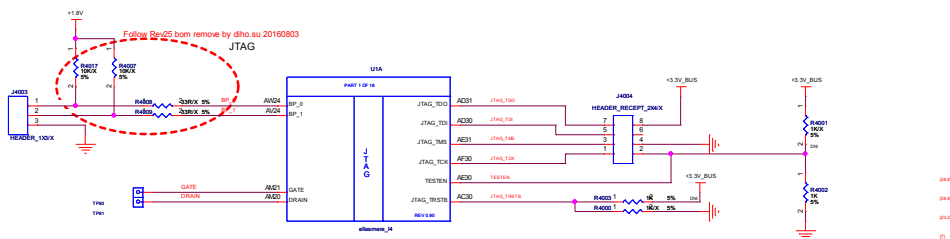
POWER UP SEQUENCE		
BUS ANAL (3.3V12V UP) → +1.8V → 0.930V	BP_VDDC VDDC → VDDC1 BVDD	



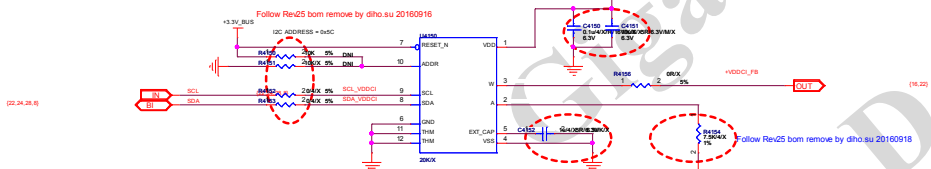
(20) MECHANICAL AND THERMAL MANAGEMENT



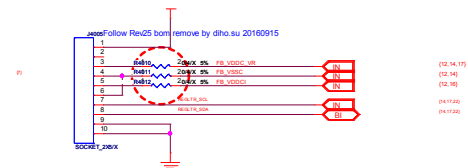
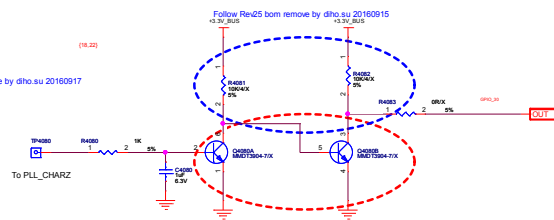
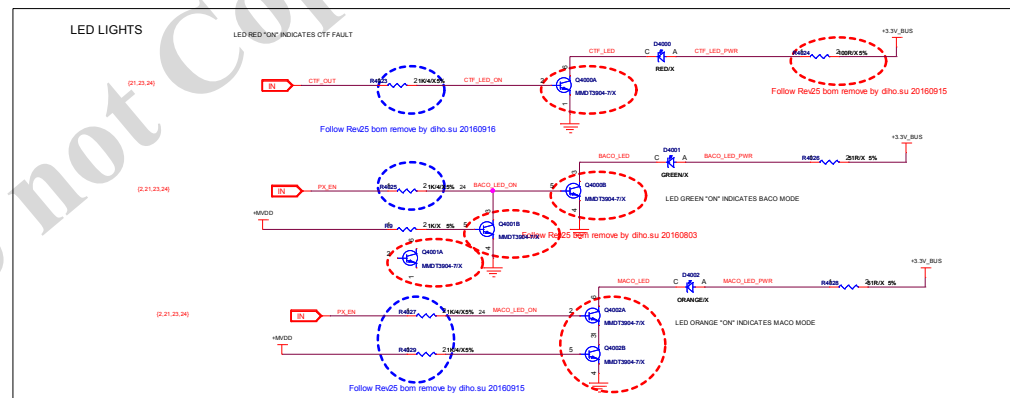
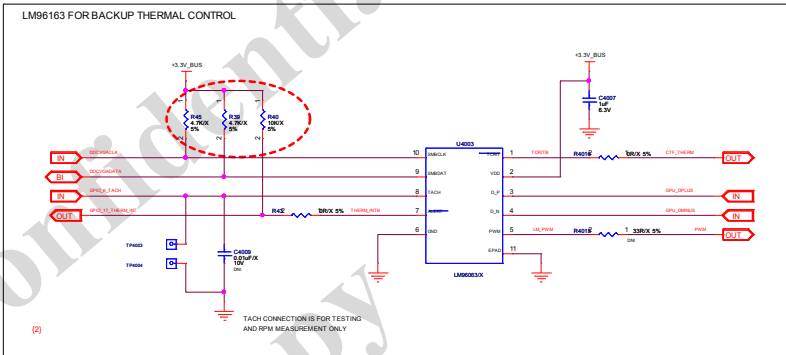
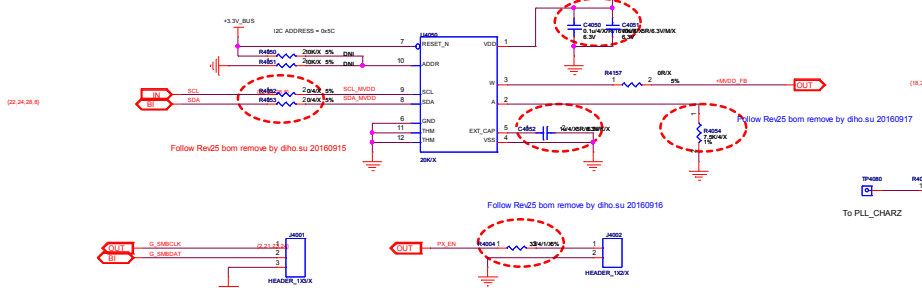
(21) DEBUG CIRCUITS



DIGITAL POTS

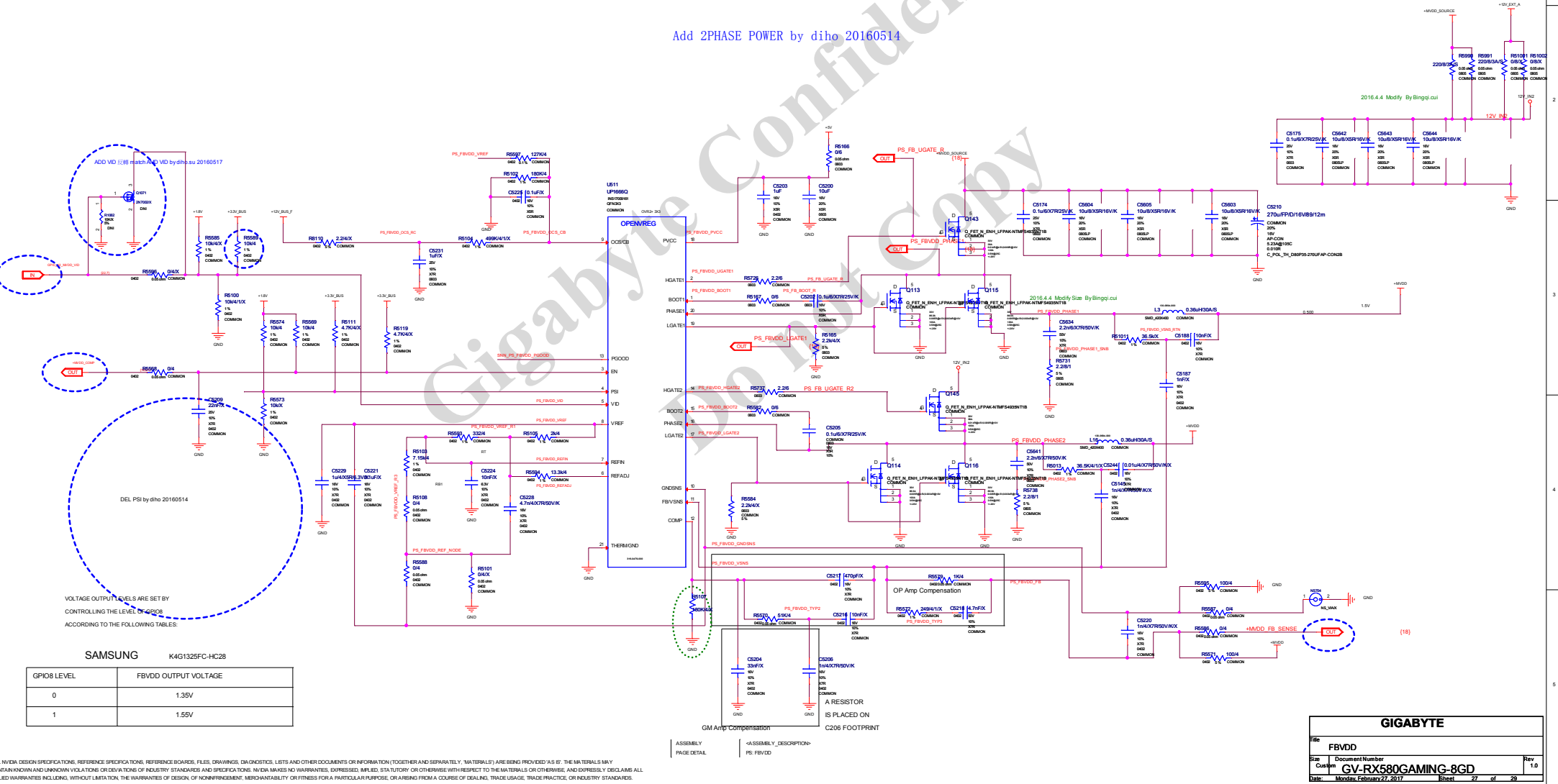


DIGITAL POTS



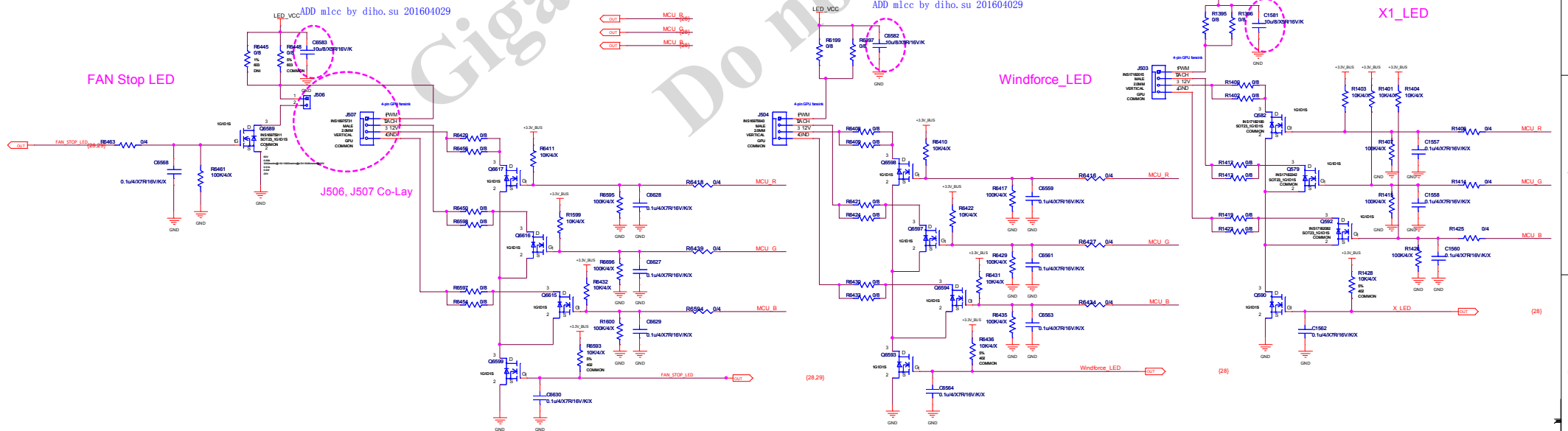
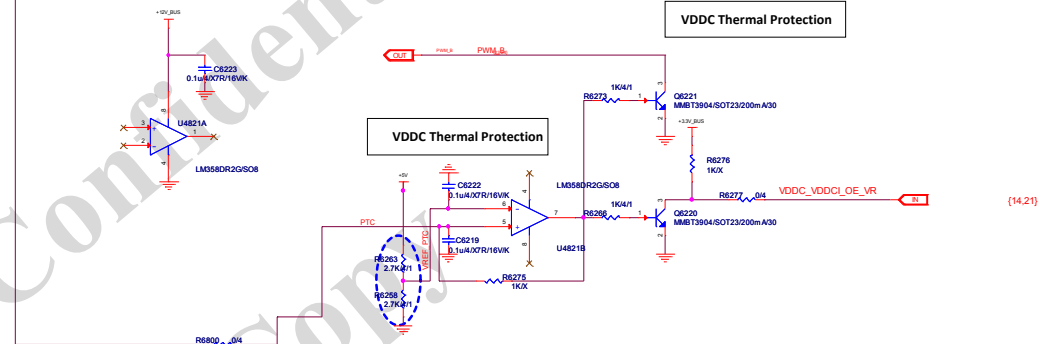
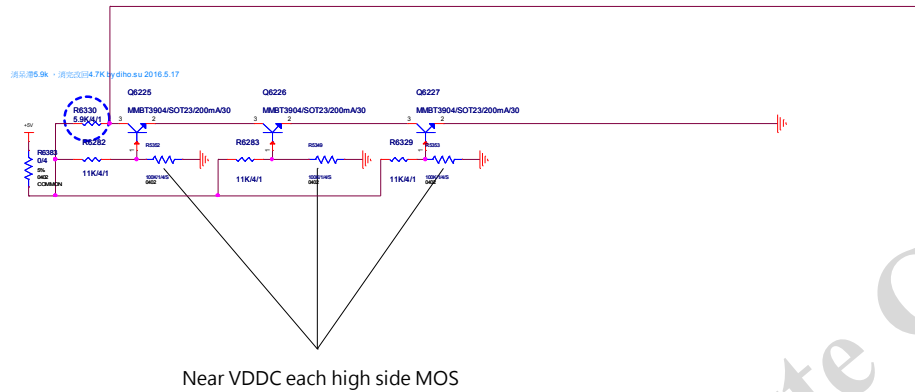
0	00A	000000	
1	00B	000000	1. Add SPI0 to SPI000 10000 2. Update SPI000 data response
2	00C	000000	PC000: - add serial resistor R1000 - R1007 - add pull-down resistor L1000 - L1007 Remove C400, C403, V0400, C410, C414, R400
3	00D	000000	Modify: G000 Design

GIGABYTE			
Title			
BLOCK DIAGRAM			
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Add MOS VRHOT CIRCUIT



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