P407-A01: G84M/G86M MXM-II
256/512MB 128-BIT GDDR2
LVDS, DVI-A, DVI-B, TV-OUT, VGA
SLI, HDMI, HDCP

Table of Contents

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10407-9998-200	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
1	SKU0001	600-10407-0001-200	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
2	SKU0002	600-10407-0002-200	G84M-600 450/400 512MB 128bit GDDR2 32Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
3	SKU0003	600-10407-0003-200	G84M-700 TBD/400 512MB 128bit GDDR2 32Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
4	SKU0004	600-10407-0004-200	G86M_770 500/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

P407 A00 to A01 change list:
There is no circuit change between A00 version and A01 version.
Only some components value been changed in A01 version, and add TTP support.

P407 A01 to A02 change list:
There is no circuit change between A00 version and A01 version.
Remove TTP support and change the thermal stiffner same as A00 used

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	Cover Page

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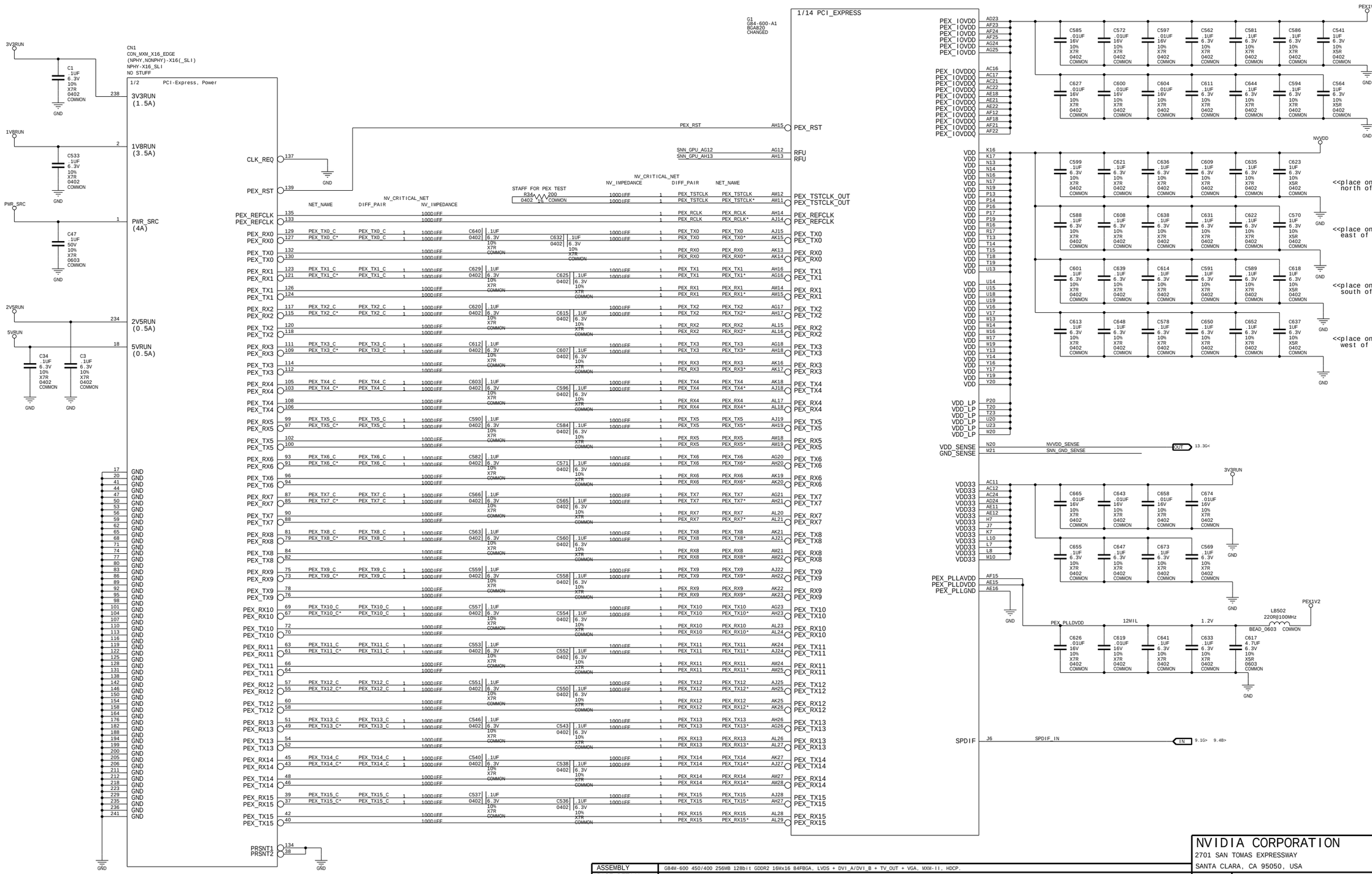
PAGE 2) MXM-II GOLDEN EDGE, PCI EXPRESS INTERFACE



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	PCI EXPRESS Interface

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PAGE 3) GPU MEMORY INTERFACE

NET	NV_IMPEDANCE	NV_CRITICAL_NET
FBA_RESET	50OHM	2
FBA_ODT_GPU	50OHM	2
FBC_RESET	50OHM	2
FBC_ODT_GPU	50OHM	2

G1
G84-600-A1
BGA820
CHANGED

2/14 FBA

FBADD0 FBADD1 FBADD2 FBADD3 FBADD4 FBADD5 FBADD6 FBADD7 FBADD8 FBADD9 FBADD10 FBADD11 FBADD12 FBADD13 FBADD14 FBADD15 FBADD16 FBADD17 FBADD18 FBADD19 FBADD20 FBADD21 FBADD22 FBADD23 FBADD24 FBADD25 FBADD26 FBADD27 FBADD28 FBADD29 FBADD30 FBADD31 FBADD32 FBADD33 FBADD34 FBADD35 FBADD36 FBADD37 FBADD38 FBADD39 FBADD40 FBADD41 FBADD42 FBADD43 FBADD44 FBADD45 FBADD46 FBADD47 FBADD48 FBADD49 FBADD50 FBADD51 FBADD52 FBADD53 FBADD54 FBADD55 FBADD56 FBADD57 FBADD58 FBADD59 FBADD60 FBADD61 FBADD62 FBADD63

FBADQM0 FBADQM1 FBADQM2 FBADQM3 FBADQM4 FBADQM5 FBADQM6 FBADQM7

FBADQS_WP0 FBADQS_WP1 FBADQS_WP2 FBADQS_WP3 FBADQS_WP4 FBADQS_WP5 FBADQS_WP6 FBADQS_WP7

FBADQS_RN0 FBADQS_RN1 FBADQS_RN2 FBADQS_RN3 FBADQS_RN4 FBADQS_RN5 FBADQS_RN6 FBADQS_RN7

FB_VREF1

FBVDD FBVDDQ GND

C642 C634 C548 C606 C605 — .1UF 6.3V 10% X7R 0402 COMMON
C576 C575 C593 C547 C587 — .1UF 6.3V 10% X7R 0402 COMMON
C645 C610 C545 C670 C602 — .1UF 6.3V 10% X7R 0402 COMMON
C654 C579 C616 C681 C583 — .1UF 6.3V 10% X7R 0402 COMMON
C598 C661 C574 C624 C573 — 1UF 6.3V 10% X5R 0402 COMMON

FBA_CMD0 FBA_CMD1 FBA_CMD2 FBA_CMD3 FBA_CMD4 FBA_CMD5 FBA_CMD6 FBA_CMD7 FBA_CMD8 FBA_CMD9 FBA_CMD10 FBA_CMD11 FBA_CMD12 FBA_CMD13 FBA_CMD14 FBA_CMD15 FBA_CMD16 FBA_CMD17 FBA_CMD18 FBA_CMD19 FBA_CMD20 FBA_CMD21 FBA_CMD22 FBA_CMD23 FBA_CMD24 FBA_CMD25 FBA_CMD26 FBA_CMD27 FBA_CMD28

FBA_CLK0 FBA_CLK0* FBA_CLK1 FBA_CLK1*

FBA_DEBUG

H_PLLAVDD FBA_PLLAVDD FBA_PLLGND

PLACE CLOSE TO BALLS
C568 470PF 16V 10% X7R 0402 COMMON
C577 .01UF 16V 10% X7R 0402 COMMON
C539 4.7UF 6.3V 10% X5R 0603 COMMON
LB501 BEAD_0603 COMMON 220R@100MHz
PEX1V2 12MIL 1.2V

NC1 NC2

R527 1K 1% 0402 NO STUFF
R529 1K 1% 0402 NO STUFF
C542 1UF 6.3V 10% X7R 0402 COMMON

ODT OPTION
FBA_RESET R535 0 0402 5% NO STUFF
FBA_ODT_GPU R537 0 0402 5% COMMON
FBA_ODT
FBC_RESET R545 0 0402 5% NO STUFF
FBC_ODT_GPU R547 0 0402 5% COMMON
FBC_ODT
PLACE THESE RESISTORS AT GPU SIDE

G1
G84-600-A1
BGA820
CHANGED

3/14 FBC

FBCD0 FBCD1 FBCD2 FBCD3 FBCD4 FBCD5 FBCD6 FBCD7 FBCD8 FBCD9 FBCD10 FBCD11 FBCD12 FBCD13 FBCD14 FBCD15 FBCD16 FBCD17 FBCD18 FBCD19 FBCD20 FBCD21 FBCD22 FBCD23 FBCD24 FBCD25 FBCD26 FBCD27 FBCD28 FBCD29 FBCD30 FBCD31 FBCD32 FBCD33 FBCD34 FBCD35 FBCD36 FBCD37 FBCD38 FBCD39 FBCD40 FBCD41 FBCD42 FBCD43 FBCD44 FBCD45 FBCD46 FBCD47 FBCD48 FBCD49 FBCD50 FBCD51 FBCD52 FBCD53 FBCD54 FBCD55 FBCD56 FBCD57 FBCD58 FBCD59 FBCD60 FBCD61 FBCD62 FBCD63

FBCDQM0 FBCDQM1 FBCDQM2 FBCDQM3 FBCDQM4 FBCDQM5 FBCDQM6 FBCDQM7

FBCDQS_WP0 FBCDQS_WP1 FBCDQS_WP2 FBCDQS_WP3 FBCDQS_WP4 FBCDQS_WP5 FBCDQS_WP6 FBCDQS_WP7

FBCDQS_RN0 FBCDQS_RN1 FBCDQS_RN2 FBCDQS_RN3 FBCDQS_RN4 FBCDQS_RN5 FBCDQS_RN6 FBCDQS_RN7

FB_VREF2

FBVTT — AA23 SNN_FBVTT_AA23; AB23 SNN_FBVTT_AB23; H16 SNN_FBVTT_H16; H17 SNN_FBVTT_H17; J10 SNN_FBVTT_J10; J23 SNN_FBVTT_J23; J24 SNN_FBVTT_J24; J9 SNN_FBVTT_J9; K11 SNN_FBVTT_K11; K12 SNN_FBVTT_K12; K21 SNN_FBVTT_K21; K22 SNN_FBVTT_K22; K24 SNN_FBVTT_K24; K9 SNN_FBVTT_K9; L23 SNN_FBVTT_L23; M23 SNN_FBVTT_M23; T25 SNN_FBVTT_T25; U25 SNN_FBVTT_U25

FBC_CMD0 FBC_CMD1 FBC_CMD2 FBC_CMD3 FBC_CMD4 FBC_CMD5 FBC_CMD6 FBC_CMD7 FBC_CMD8 FBC_CMD9 FBC_CMD10 FBC_CMD11 FBC_CMD12 FBC_CMD13 FBC_CMD14 FBC_CMD15 FBC_CMD16 FBC_CMD17 FBC_CMD18 FBC_CMD19 FBC_CMD20 FBC_CMD21 FBC_CMD22 FBC_CMD23 FBC_CMD24 FBC_CMD25 FBC_CMD26 FBC_CMD27 FBC_CMD28

FBC_CLK0 FBC_CLK0* FBC_CLK1 FBC_CLK1*

FBC_DEBUG

FBC_PLLVDD FBC_PLLAVDD FBC_PLLGND

PLACE CLOSE TO BALLS
C660 470PF 16V 10% X7R 0402 COMMON
C659 .01UF 16V 10% X7R 0402 COMMON
C646 4.7UF 6.3V 10% X5R 0603 COMMON
LB503 BEAD_0603 COMMON 220R@100MHz
PEX1V2 12MIL 1.2V

FBCAL_PD_VDDQ FBCAL_PU_GND FBCAL_TERM_GND
R539 40.2 1% 0402 COMMON
R541 40.2 1% 0402 COMMON
R534 40.2 1% 0402 NO STUFF

R533 1K 1% 0402 NO STUFF
R543 1K 1% 0402 NO STUFF
C561 .1UF 6.3V 10% X7R 0402 COMMON

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	Frame Buffer GPU Interface

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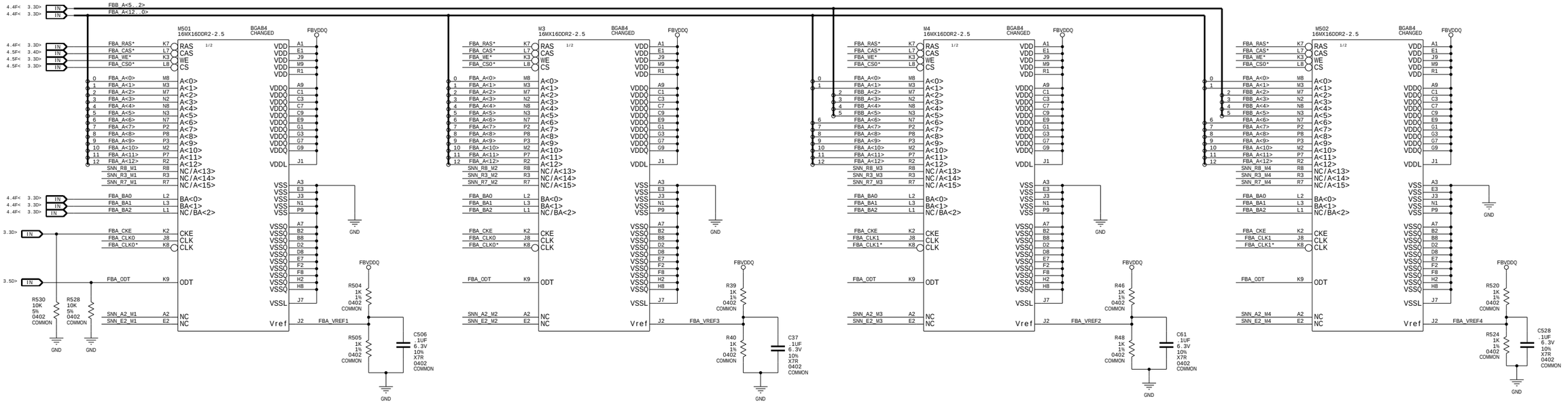
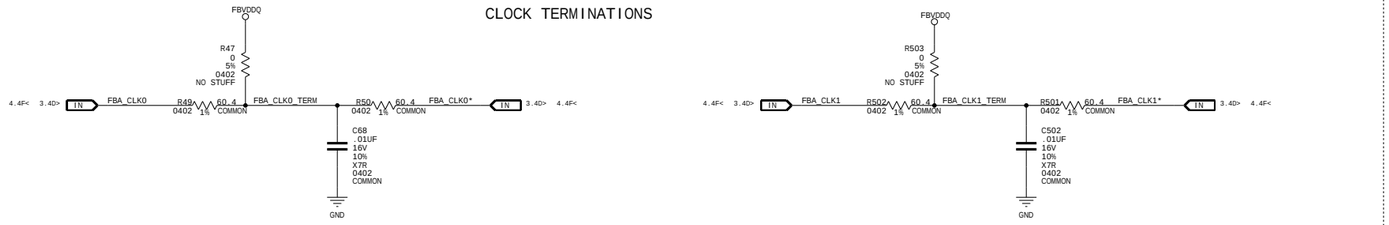
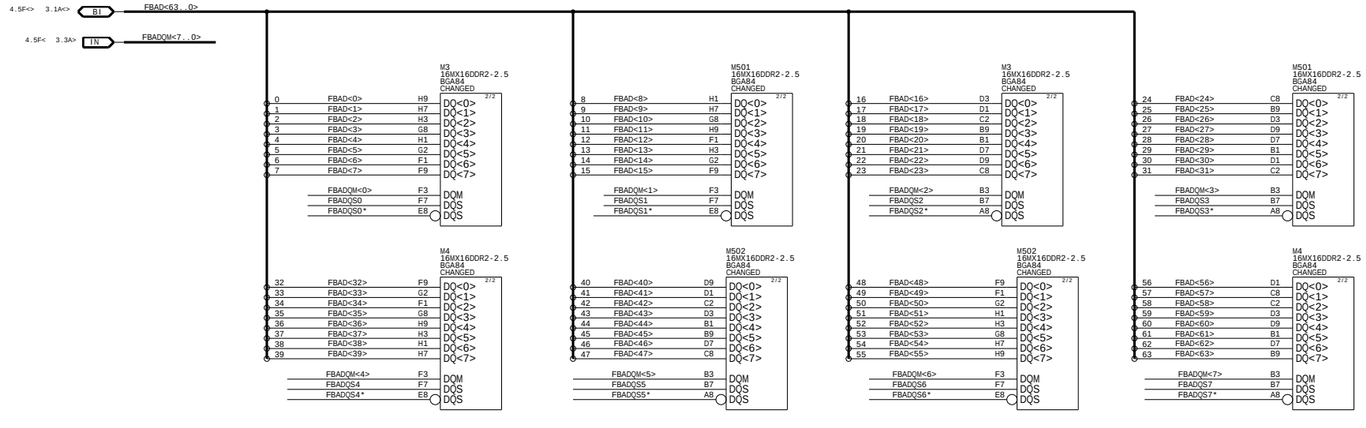
PAGE 4) MEMORY PARTITION A



CLOCK TERMINATIONS





NET		MIN_LINE_WIDTH	VOLTAGE
FBA_VREF1		16MIL	0.9V
FBA_VREF2		16MIL	0.9V
FBA_VREF3		16MIL	0.9V
FBA_VREF4		16MIL	0.9V

NET	DIFFPAIR	CRITICAL	IMPEDANCE
FBA_CLK0	FBA_CLK0	1	100DIFF
FBA_CLK0*	FBA_CLK0	1	100DIFF
FBA_CLK1	FBA_CLK1	1	100DIFF
FBA_CLK1*	FBA_CLK1	1	100DIFF
FBADQS0	FBADQS0	1	100DIFF
FBADQS0*	FBADQS0	1	100DIFF
FBADQS1	FBADQS1	1	100DIFF
FBADQS1*	FBADQS1	1	100DIFF
FBADQS2	FBADQS2	1	100DIFF
FBADQS2*	FBADQS2	1	100DIFF
FBADQS3	FBADQS3	1	100DIFF
FBADQS3*	FBADQS3	1	100DIFF
FBADQS4	FBADQS4	1	100DIFF
FBADQS4*	FBADQS4	1	100DIFF
FBADQS5	FBADQS5	1	100DIFF
FBADQS5*	FBADQS5	1	100DIFF
FBADQS6	FBADQS6	1	100DIFF
FBADQS6*	FBADQS6	1	100DIFF
FBADQS7	FBADQS7	1	100DIFF
FBADQS7*	FBADQS7	1	100DIFF
FBA_A<12..0>		2	56OHM
FBB_A<5..2>		2	56OHM
FBA_BA0		2	56OHM
FBA_BA1		2	56OHM
FBA_CKE		2	56OHM
FBA_BA2		2	56OHM
FBA_RAS*		2	56OHM
FBA_CAS*		2	56OHM
FBA_WE*		2	56OHM
FBA_CS0*		2	56OHM
FBA_CS1*		2	56OHM
FBAD<63..0>		2	50OHM
FBADQM<7..0>		2	50OHM
FBA_ODT		2	56OHM

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	Frame Buffer Partition A Memories

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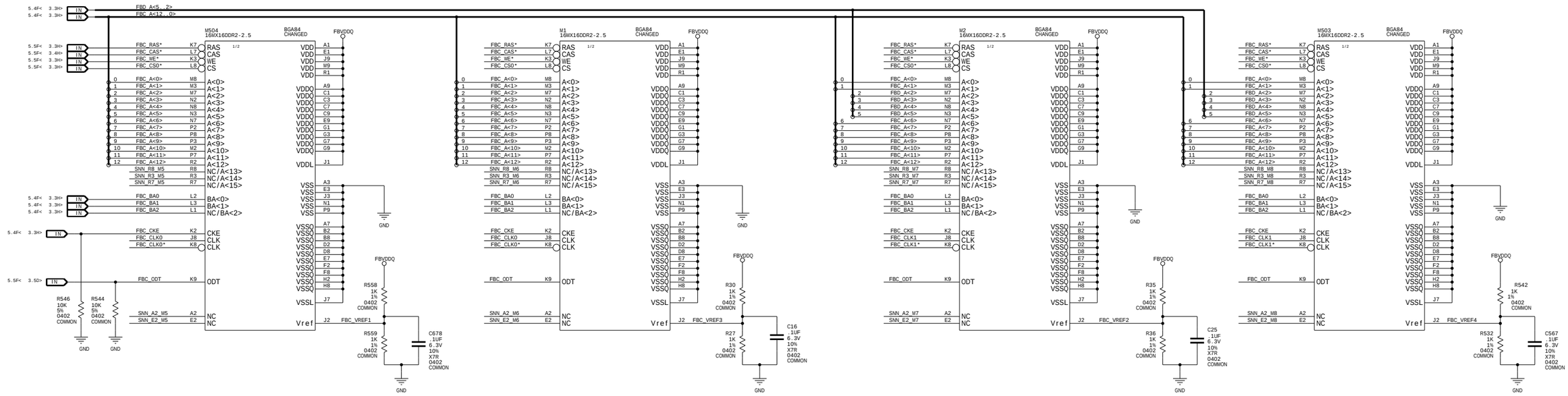
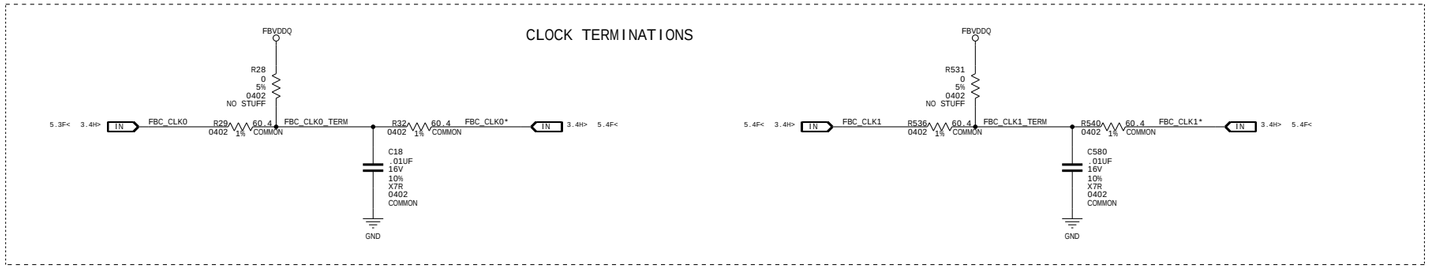
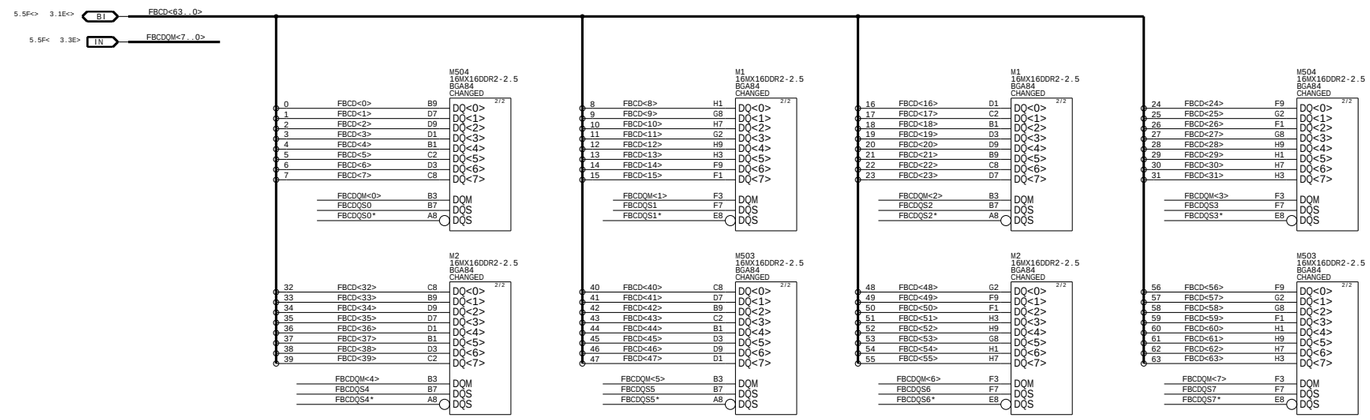
PAGE 5) MEMORY PARTITION C



CLOCK TERMINATIONS





NET	MIN_LINE_WIDTH	VOLTAGE
FBC_VREF1	16MIL	0.9V
FBC_VREF2	16MIL	0.9V
FBC_VREF3	16MIL	0.9V
FBC_VREF4	16MIL	0.9V

NET	DIFFPAIR	CRITICAL	IMPEDANCE
FBC_CLK0	FBC_CLK0	1	100DIFF
FBC_CLK0*	FBC_CLK0	1	100DIFF
FBC_CLK1	FBC_CLK1	1	100DIFF
FBC_CLK1*	FBC_CLK1	1	100DIFF
FBCDQS0	FBCDQS0	1	100DIFF
FBCDQS0*	FBCDQS0	1	100DIFF
FBCDQS1	FBCDQS1	1	100DIFF
FBCDQS1*	FBCDQS1	1	100DIFF
FBCDQS2	FBCDQS2	1	100DIFF
FBCDQS2*	FBCDQS2	1	100DIFF
FBCDQS3	FBCDQS3	1	100DIFF
FBCDQS3*	FBCDQS3	1	100DIFF
FBCDQS4	FBCDQS4	1	100DIFF
FBCDQS4*	FBCDQS4	1	100DIFF
FBCDQS5	FBCDQS5	1	100DIFF
FBCDQS5*	FBCDQS5	1	100DIFF
FBCDQS6	FBCDQS6	1	100DIFF
FBCDQS6*	FBCDQS6	1	100DIFF
FBCDQS7	FBCDQS7	1	100DIFF
FBCDQS7*	FBCDQS7	1	100DIFF

FBC_A<12..0>	2	56OHM
FBD_A<5..2>	2	56OHM
FBC_BA0	2	56OHM
FBC_BA1	2	56OHM
FBC_CKE	2	56OHM
FBC_BA2	2	56OHM
FBC_RAS*	2	56OHM
FBC_CAS*	2	56OHM
FBC_WE*	2	56OHM
FBC_CS0*	2	56OHM
FBC_CS1*	2	56OHM
FBCD<63..0>	2	50OHM
FBCDQM<7..0>	2	50OHM
FBC_ODT	2	56OHM

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	Frame Buffer Partition C Memories

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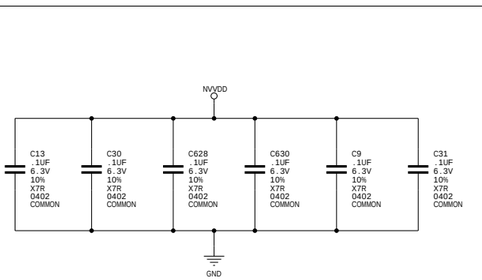
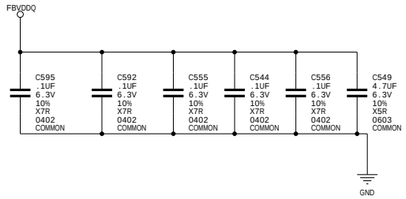
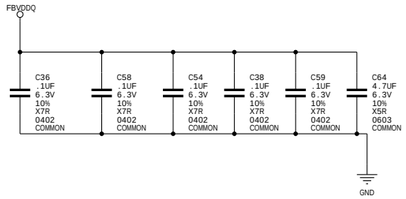
PAGE 6) MEMORY DECOUPLING CAPS

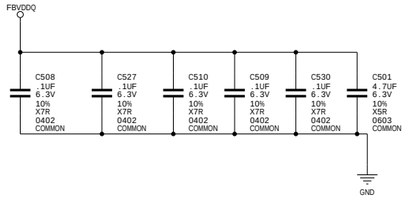
DECOUPLING CAPS FOR MEMORYS (PARTION A AND PARTION C)

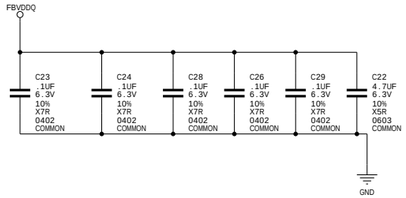


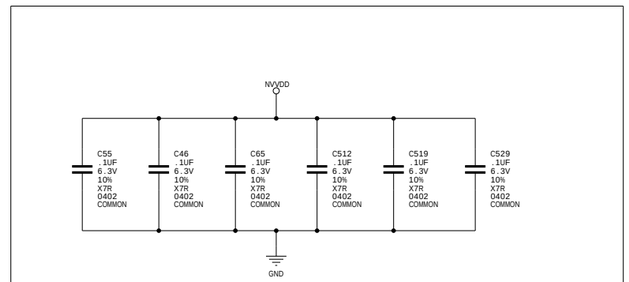
NVVDD TRANSITION CAP NEAR BY PARTION A



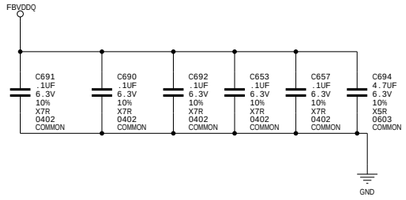


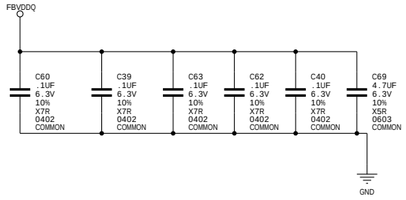


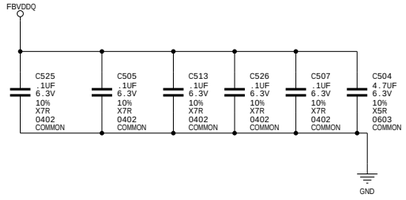


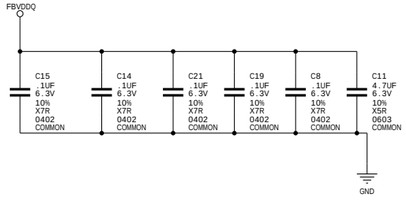


NVVDD TRANSITION CAP NEAR BY PARTION C









ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	Memory Decoupling Caps

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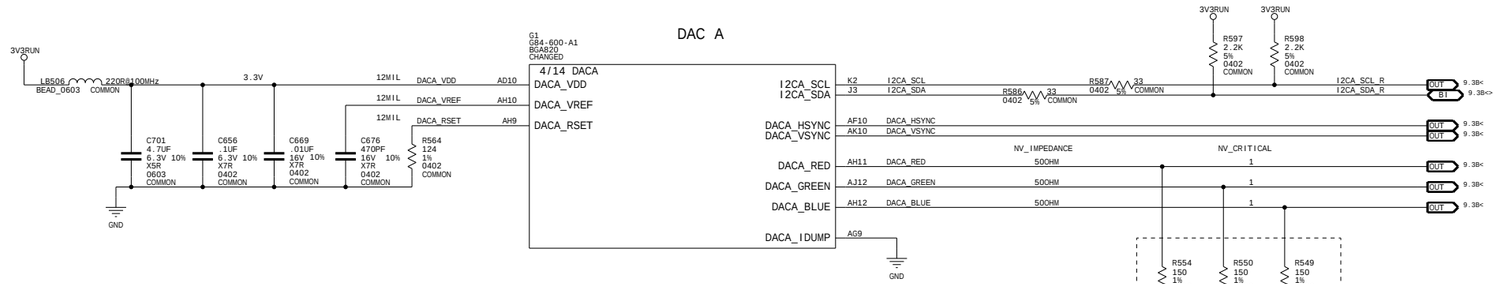
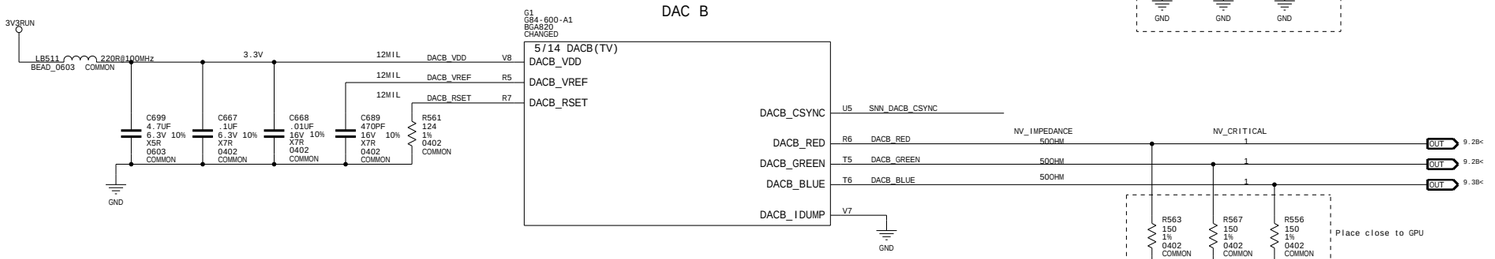
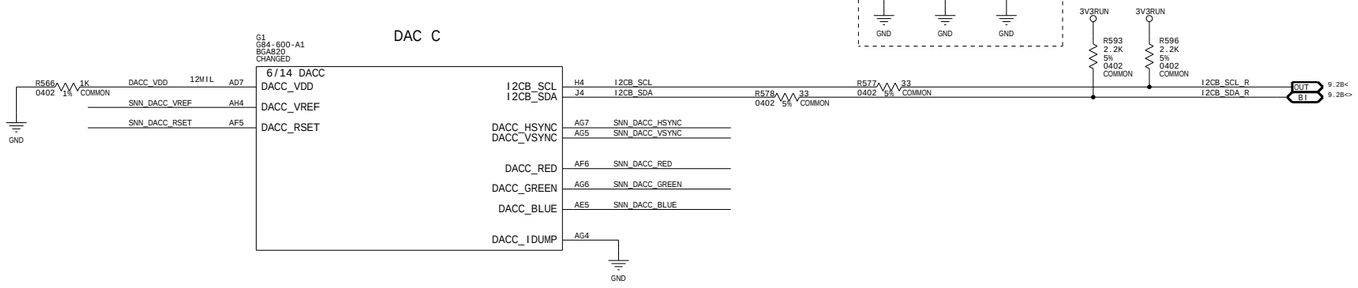
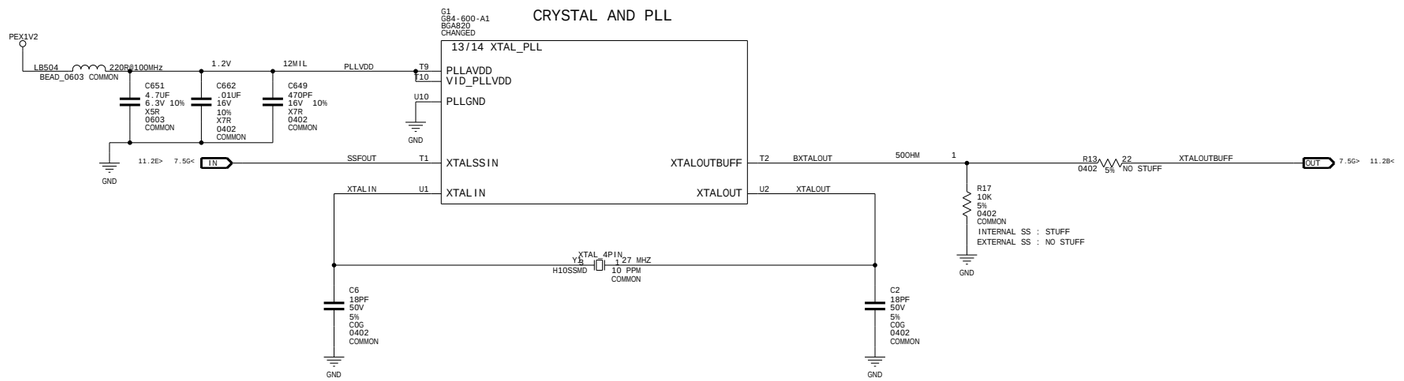
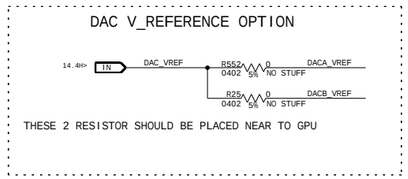
PAGE 7) DAC_A, DAC_B, DAC_C, PLL, CRYSTAL











NV_NET_NAME	NV_IMPEDANCE	NV_CRITICAL_NET
XTALOUT	500HM	1
XTALIN	500HM	1
XTALOUTBUFF	500HM	1
SSFOUT	500HM	1

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	DACs, Clock-Generation

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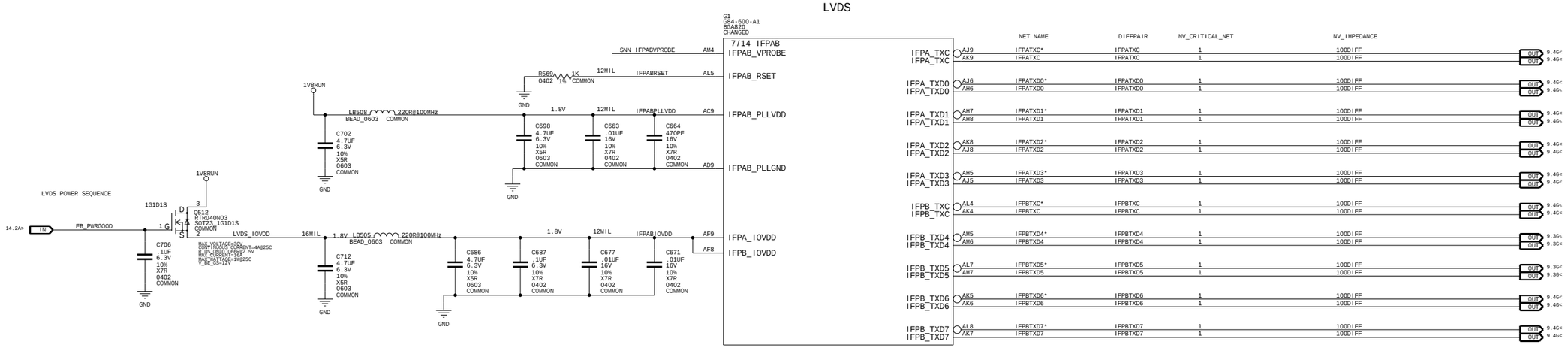
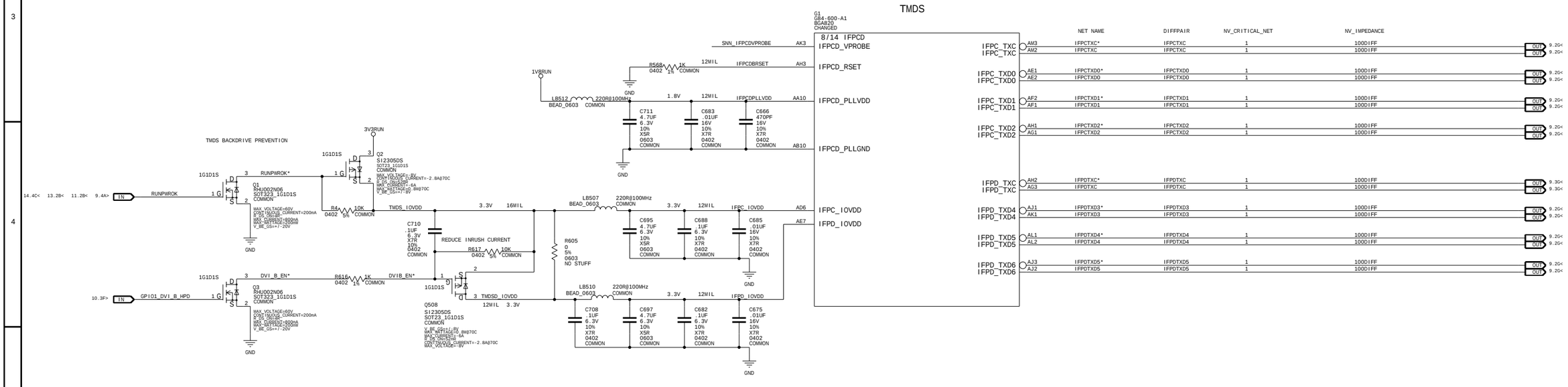
PAGE 8) LVDS(LINK A/B), TMDS(LINK C/D)

LVDS



TMDS



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	LVDS, TMDS GPU Interface

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PAGE 9) MXM CONNECTOR

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
3V3RUN	3.3V	12MIL	1.5A
1V8RUN	1.8V	12MIL	3.5A
2V5RUN	2.5V	12MIL	0.5A
5VRUN	5V	16MIL	0.5A
PWR_SRC	22V	16MIL	4A
GND	0V	12MIL	50A

SPDIF	50OHM	1	
SPDIF_IN	50OHM	1	

MXM CONNECTOR

CN1
CON_MXM_X16_EDGE
(N,NON)PHY(_X16,-HE)_SLI
NPHY-X16_SLI
NO STUFF

2/2 IO - LVDS,DVI,VGA,TV

10.3H<	OUT	DVI_A_HPD	217	DVI_A_HPD	
7.3G>	IN	I2CB_SCL_R	232	DDCB_SCLK	
7.3G<>	BI	I2CB_SDA_R	230	DDCB_SDATA	
10.3H<	OUT	DVI_B_HPD	193	DVI_B_HPD	
7.2F>	IN	DACB_GREEN	140	TV_Y / HDTV_Y	
7.2F>	IN	DACB_RED	136	TV_C / HDTV_Pr	
7.3F>	IN	DACB_BLUE	144	TV_CVBS / HDTV_Pb	
7.1F>	IN	DACA_VSYNC	153	VSYNC	
7.1F>	IN	DACA_HSYNC	151	HSYNC	
7.1F>	IN	DACA_RED	148	VGA_RED	
7.1F>	IN	DACA_GREEN	152	VGA_GRN	
7.2F>	IN	DACA_BLUE	156	VGA_BLU	
7.1F>	IN	I2CA_SCL_R	155	DDCA_SCLK	
7.1F<>	BI	I2CA_SDA_R	157	DDCA_SDATA	
10.3F>	IN	GPIO3_PPEN	224	LVDS_PPEN	
10.3F>	IN	GPIO4_BLEN	228	LVDS_BLEN	
10.3F>	IN	GPIO2_BL_PWM	226	LVDS_BL_BRGHT	
11.2B< 10.3F>	IN	I2CC_SCL_R	222	DDCC_SCLK	
11.2B<> 10.3F<>	BI	I2CC_SDA_R	220	DDCC_SDATA	
10.2A<>	BI	SMB_DAT	145	SMB_DAT	
10.2A<	OUT	SMB_CLK	147	SMB_CLK	
10.2F>	IN	THERM_ALERT*	149	THERM	
10.3F<	OUT	RUNPWROK_IN	16	RUNPWROK	
		GPIO_AC_BATT*	169	AC/BATT*	
2.5C< 9.1D>	OUT	SPDIF_IN		SPDIF	170

DVI-A

DVI_A_CLK	219	IFPCTXC*	8.3H>
DVI_A_CLK	221	IFPCTXC	8.3H>
DVI_A_TX0	237	IFPCTXD0*	8.3H>
DVI_A_TX0	239	IFPCTXD0	8.3H>
DVI_A_TX1	231	IFPCTXD1*	8.3H>
DVI_A_TX1	233	IFPCTXD1	8.3H>
DVI_A_TX2	225	IFPCTXD2*	8.4H>
DVI_A_TX2	227	IFPCTXD2	8.4H>

DVI-B / SLI

DVI_B_TX2	201	IFPDTXD5*	8.4H>
DVI_B_TX2	203	IFPDTXD5	8.4H>
DVI_B_TX1	207	IFPDTXD4*	8.4H>
DVI_B_TX1	209	IFPDTXD4	8.4H>
DVI_B_TX0	213	IFPDTXD3*	8.4H>
DVI_B_TX0	215	IFPDTXD3	8.4H>
DVI_B_CLK	189	IFPDTXC*	8.4H>
DVI_B_CLK	191	IFPDTXC	8.4H>
DR_RASTER_SYNC			
DR_SWAP_RDY			

DR_D0	185	SLI_D<0>	0
DR_D1	183	SLI_D<1>	1
DR_D2	181	SLI_D<2>	2
DR_D3	179	SLI_D<3>	3
DR_D4	177	SLI_D<4>	4
DR_D5	175	SLI_D<5>	5
DR_D6	173	SLI_D<6>	6
DR_D7	167	SLI_D<7>	7
DR_D8	165	SLI_D<8>	8
DR_D9	163	SLI_D<9>	9
DR_D10	161	SLI_D<10>	10
DR_D11	159	SLI_D<11>	11
DR_D12	187	SLI_D<12>	12
DR_D13	195	SLI_D<13>	13
DR_D14	197	SLI_D<14>	14
DR_CMD	143	SLI_DE	
DR_REFCLK	141	SLI_REFCLK	
DR_CLK	171	SLI_CLKOUT	

SLI_D<14..0> BI 12.1E<> 15.4B>

GND

LVDS_UTX0	186	IFPBTXD4	8.2H>
LVDS_UTX0	184	IFPBTXD4*	8.2H>
LVDS_UTX1	180	IFPBTXD5	8.2H>
LVDS_UTX1	178	IFPBTXD5*	8.2H>
LVDS_UTX2	174	IFPBTXD6	8.2H>
LVDS_UTX2	172	IFPBTXD6*	8.2H>
LVDS_UTX3	168	IFPBTXD7	8.2H>
LVDS_UTX3	166	IFPBTXD7*	8.2H>
LVDS_UCLK	162	IFPBTXC	8.2H>
LVDS_UCLK	160	IFPBTXC*	8.2H>
LVDS_LTX0	216	IFPATXD0	8.1H>
LVDS_LTX0	214	IFPATXD0*	8.1H>
LVDS_LTX1	210	IFPATXD1	8.1H>
LVDS_LTX1	208	IFPATXD1*	8.1H>
LVDS_LTX2	204	IFPATXD2	8.2H>
LVDS_LTX2	202	IFPATXD2*	8.2H>
LVDS_LTX3	198	IFPATXD3	8.2H>
LVDS_LTX3	196	IFPATXD3*	8.2H>
LVDS_LCLK	192	IFPATXC	8.1H>
LVDS_LCLK	190	IFPATXC*	8.1H>

2V5RUN 2V5RUN
R24 10K 5% 0402 COMMON
R18 10K 5% 0402 COMMON

R16 1K 0402 1% COMMON GPIO_SLI_SYNC BI 10.3F<>
R15 1K 0402 1% COMMON SLI_SWAP_OUT BI 11.4C<>

PLACE THESE COMPONENTS TO ISOLATE
2 TYPE SIGNALS AND BALANCE THE LOAD
OF THE DIFF PAIR

14.4C< 13.2B< 11.2B< 8.4A< OUT RUNPWROK R38 1K 0402 1% COMMON
C33 1000PF 50V 10% X7R 0402 COMMON GND

ESD Protection for MOSFET Gates

SPDIF_IN R565 49.9 0402 1% COMMON SPDIF

ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	MXM Connector. IO-Section

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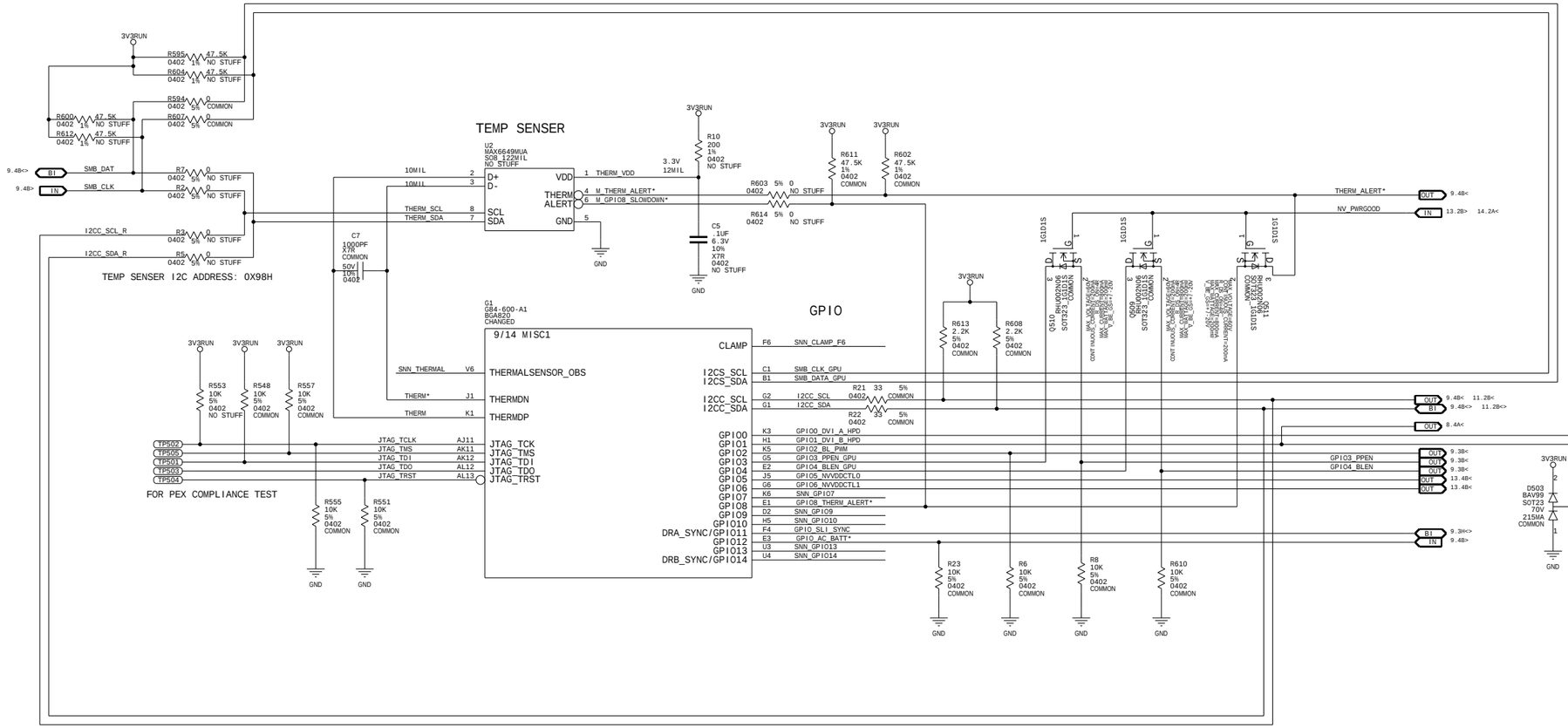
PAGE 10) GPIO, JTAG, TEMP SENSOR



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	GPIOs, JTAG, Thermal Senser

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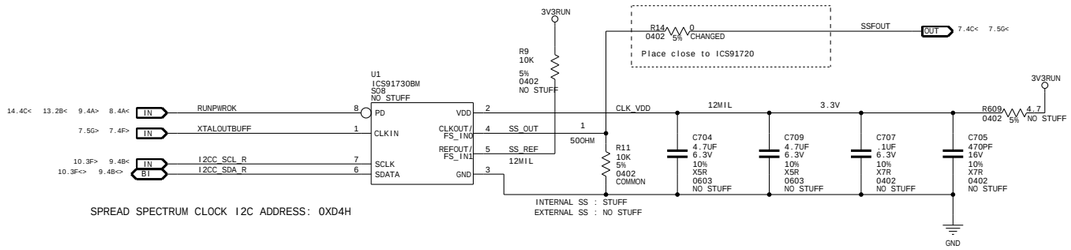
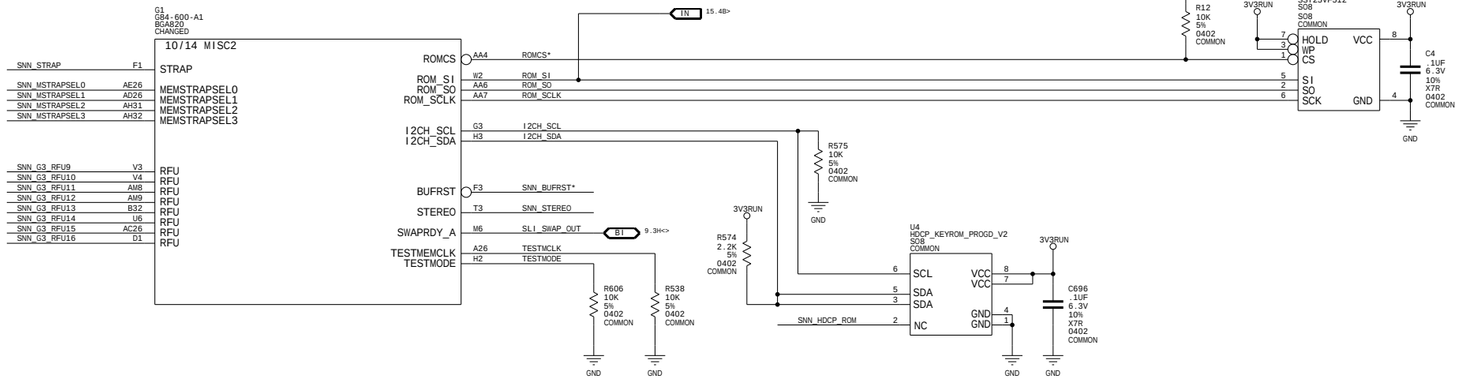
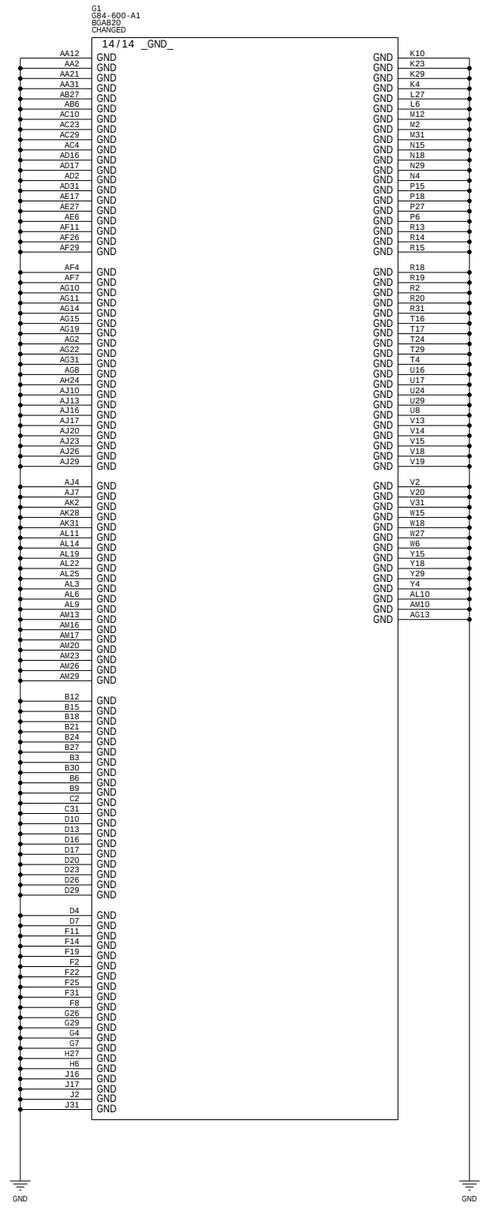
PAGE 11) SPREAD SPECTRUM, VBIOS, HDCP BIOS, GPU GND

SPREAD SPECTRUM



VBIOS AND HDCP ROM





ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	Spread Spectrum, VBIOS and HDCP ROM

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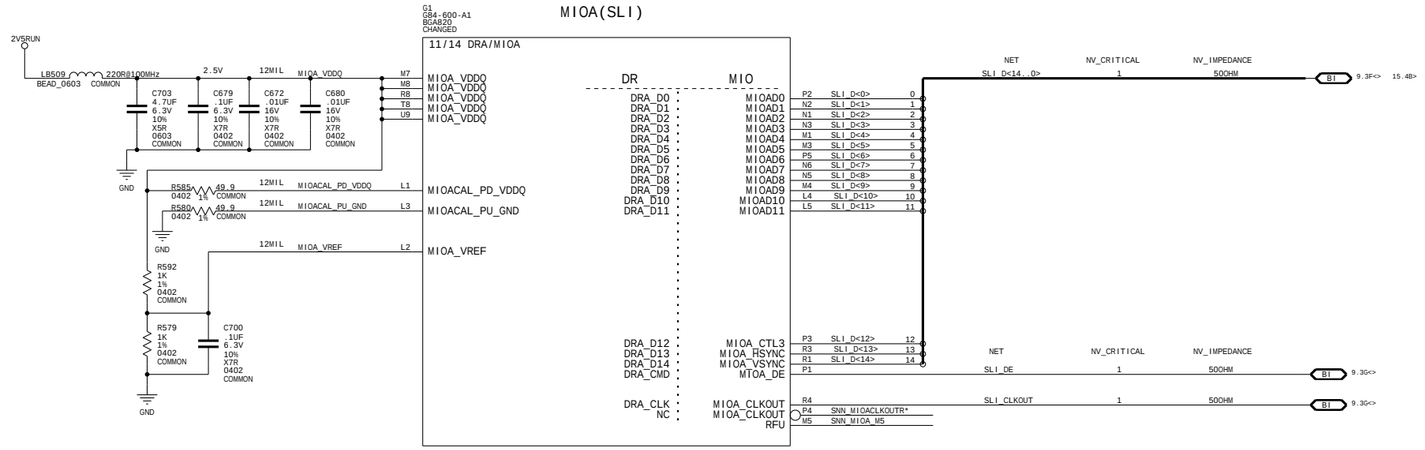
PAGE 12) MIOA(SLI), MIOB



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	MIOA(SLI), MIOB

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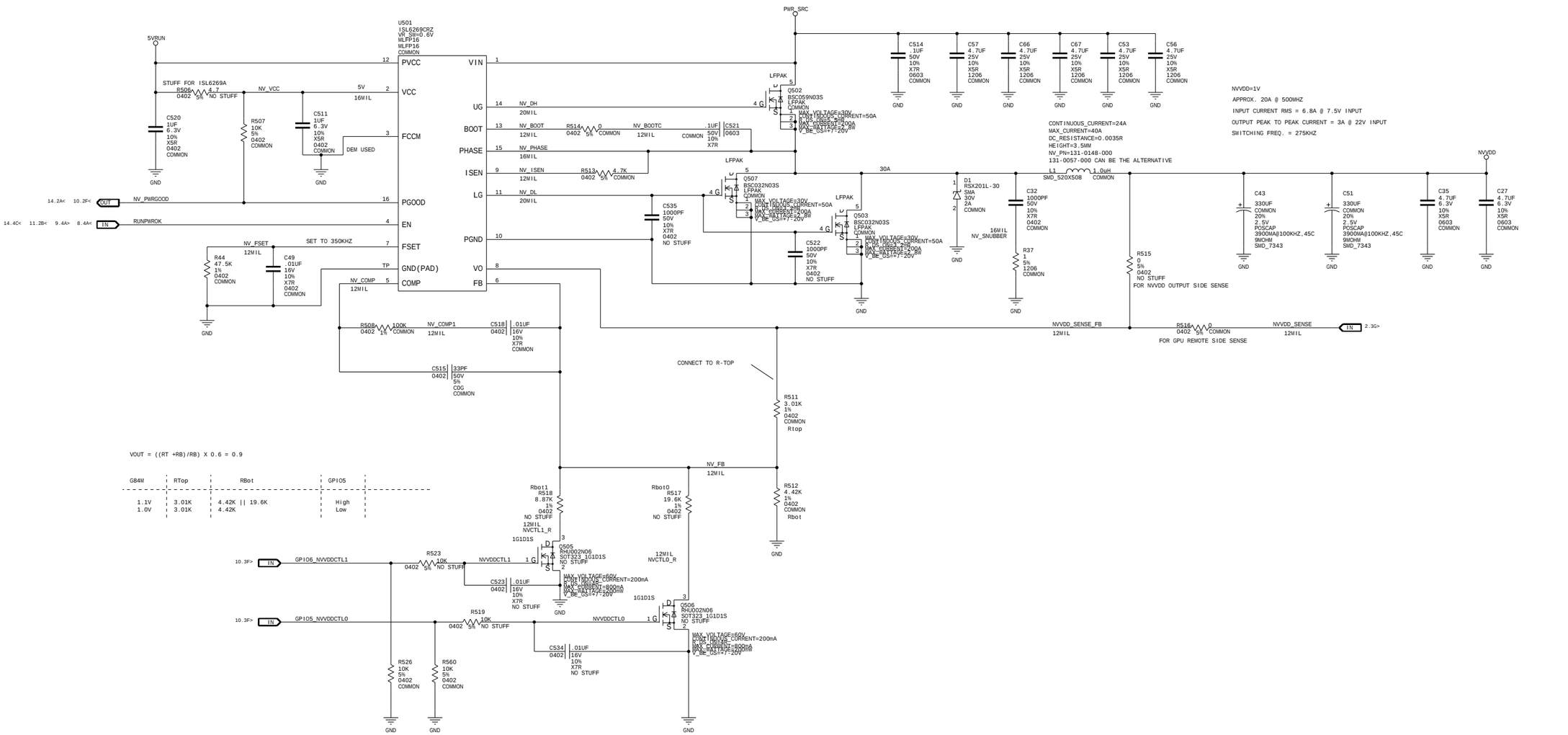
PAGE 13) NVVDD POWER SUPPLY

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
NVVDD	1V	12MIL	30A

NVVDD SWITCHER POWER SUPPLY



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	NVVDD Power Supply

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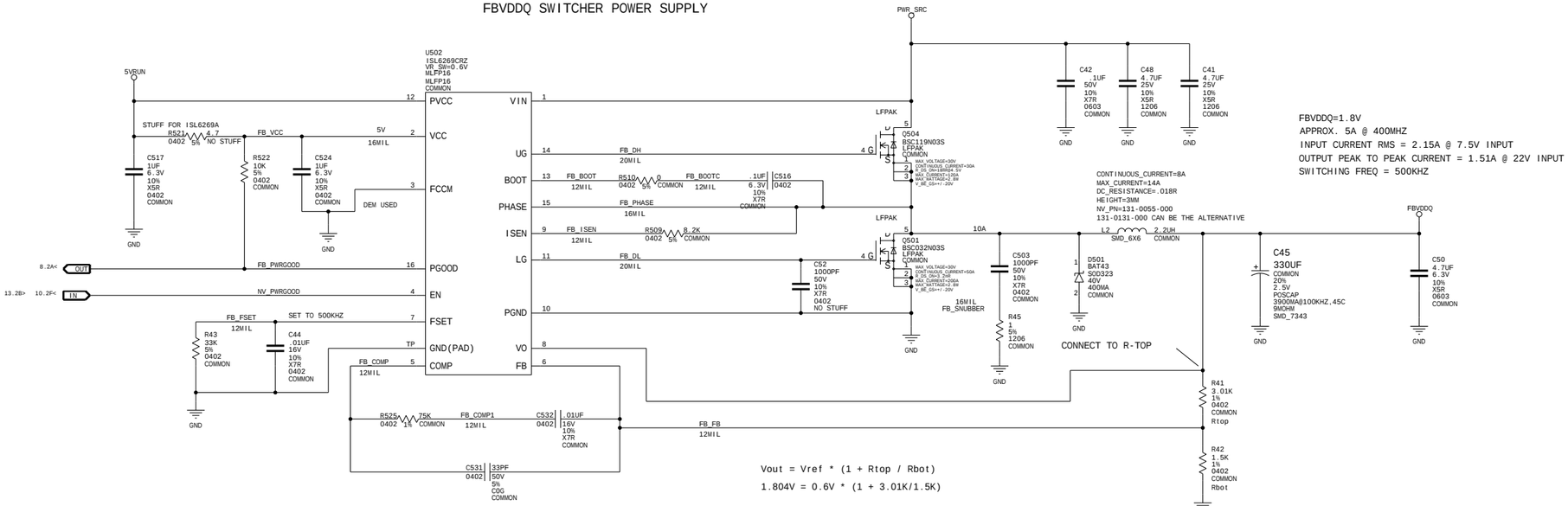
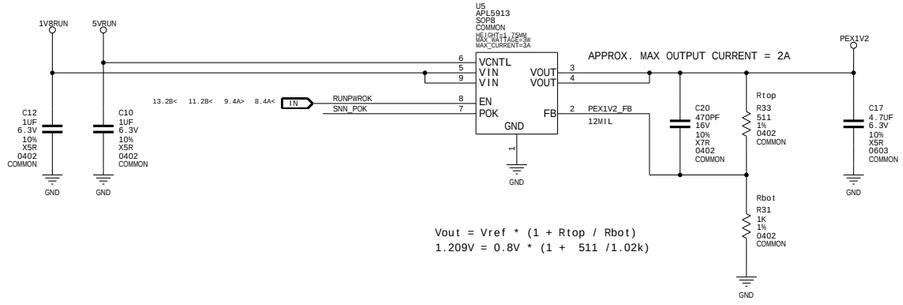
PAGE 14) FBVDDQ AND PEX1V2 POWER SUPPLY

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
PEX1V2 — PEX1V2	1.2V	12MIL	2A
FBVDDQ — FBVDDQ	1.8V	12MIL	10A

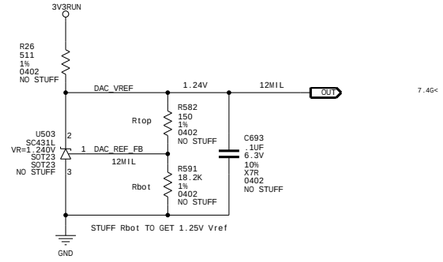
FBVDDQ SWITCHER POWER SUPPLY



PEX1V2 LINEAR SUPPLY



DAC V_REFERENCE SUPPLY



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	FBVDDQ, PEX1V2 and DAC_Vref Power Supply

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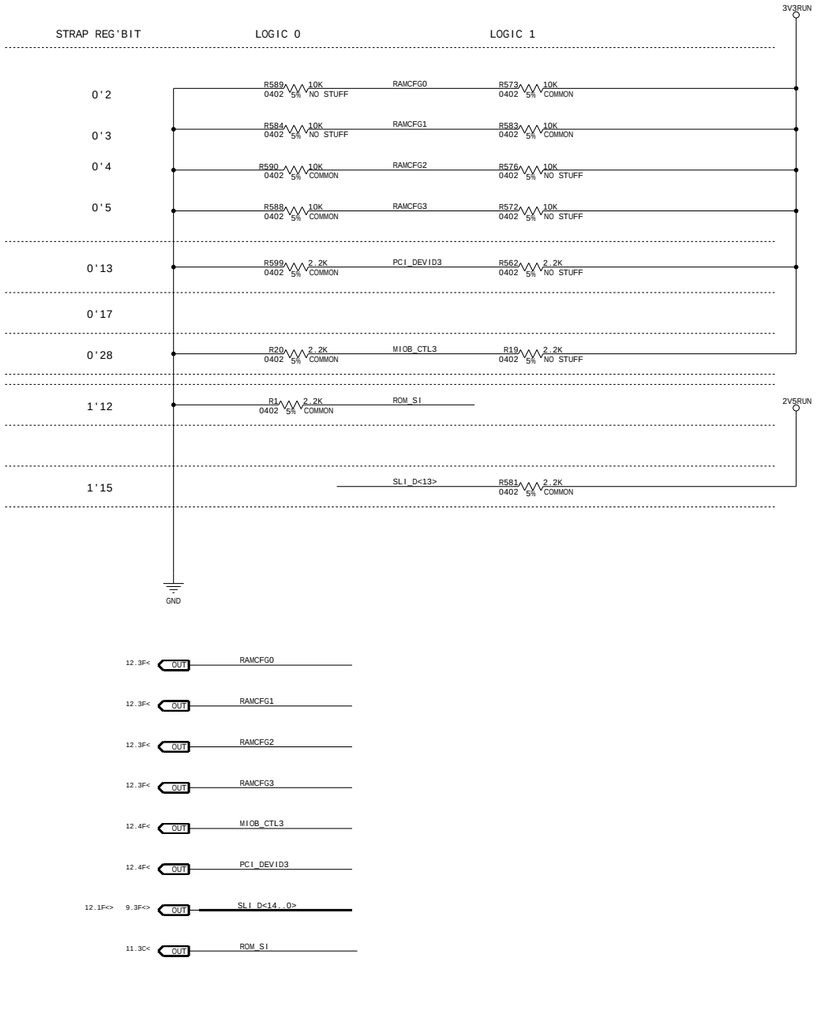
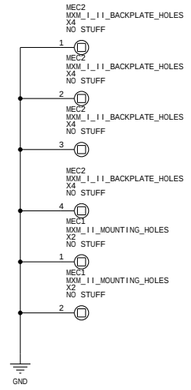
PAGE 15) STRAPS, MOUNTING HOLES



RAM_CFG_0	RAM_CFG[3:0]
RAM_CFG_1	MS_0000: 16Mx16 DDR2 128bit SDRAM, ELPIDA. MS_0001: 16Mx16 DDR2 128bit SDRAM, SAMSUNG, MICRON. MS_0010: 16Mx16 DDR2 128bit SDRAM. INFINEON. MS_0011: 16Mx16 DDR2 128bit SDRAM, HYNIX.
RAM_CFG_2	MS_0100: 32Mx16 DDR2 128bit SDRAM, ELPIDA. MS_0101: 32Mx16 DDR2 128bit SDRAM, SAMSUNG, MICRON. MS_0110: 32Mx16 DDR2 128bit SDRAM. INFINEON. MS_0111: 32Mx16 DDR2 128bit SDRAM, HYNIX.
RAM_CFG_3	
PCI_DEVID_3	MS_0: DEVICE ID = 0x0407, G84M-600. MS_1: DEVICE ID = 0x0408: G84M-700 MS_1: DEVICE ID = 0x0428: G86M-700
PEX_PLL_EN_TERM100	
PCI_DEVID_EXT	
MIOA_EN_3.3V	
MIOB_EN_3.3V	
SLOT CLOCK CONFIGURATION	



ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
PAGE DETAIL	STRAPS, MOUNTING HOLE

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Title: Basenet Report
Design: p407_a02
Date: Nov 30 11:00:17 2006

Base nets and synonyms for p407_lib.P407_A02(@p407_lib.p407_a02(sch_1))

Base Signal	Location([Zone][dir])
1V8RUN	9.1G
2V5RUN	9.1G
3V3RUN	9.1G
5VRUN	9.1G
BXTALOUT	7.4D
CLK_VDD	11.2C
DACA_BLUE	7.2F> 9.3B<
DACA_GREEN	7.1F> 9.3B<
DACA_HSYNC	7.1F> 9.3B<
DACA_RED	7.1F> 9.3B<
DACA_RSET	7.1C
DACA_VDD	7.1C
DACA_VREF	7.1C 7.4H
DACA_VSYNC	7.1F> 9.3B<
DACB_BLUE	7.3F> 9.3B<
DACB_GREEN	7.2F> 9.2B<
DACB_RED	7.2F> 9.2B<
DACB_RSET	7.2C
DACB_VDD	7.2C
DACB_VREF	7.2C 7.4H
DACC_VDD	7.3C
DAC_REF_FB	14.4G
DAC_VREF	7.4G< 14.4H>
DVIB_EN*	8.4B
DVI_A_HPD	9.2B> 10.3H<
DVI_B_EN*	8.4B
DVI_B_HPD	9.2B> 10.3H<
FBAD<0>	3.1A 4.4B
FBAD<63..0>	3.1A<> 4.4A<> 4.5F<>
FBAD<1>	3.1A 4.4B
FBAD<2>	3.1A 4.4B
FBAD<3>	3.1A 4.4B
FBAD<4>	3.1A 4.4B
FBAD<5>	3.1A 4.4B
FBAD<6>	3.1A 4.4B
FBAD<7>	3.1A 4.4B
FBAD<8>	3.1A 4.4C
FBAD<9>	3.1A 4.4C
FBAD<10>	3.1A 4.4C
FBAD<11>	3.1A 4.4C
FBAD<12>	3.1A 4.4C
FBAD<13>	3.1A 4.4C
FBAD<14>	3.1A 4.4C
FBAD<15>	3.1A 4.4C
FBAD<16>	3.1A 4.4D
FBAD<17>	3.2A 4.4D
FBAD<18>	3.2A 4.4D
FBAD<19>	3.2A 4.4D
FBAD<20>	3.2A 4.4D
FBAD<21>	3.2A 4.4D
FBAD<22>	3.2A 4.4D
FBAD<23>	3.2A 4.4D
FBAD<24>	3.2A 4.4D
FBAD<25>	3.2A 4.4D
FBAD<26>	3.2A 4.4D
FBAD<27>	3.2A 4.4D
FBAD<28>	3.2A 4.4D
FBAD<29>	3.2A 4.4D
FBAD<30>	3.2A 4.4D
FBAD<31>	3.2A 4.4D
FBAD<32>	3.2A 4.5B
FBAD<33>	3.2A 4.5B
FBAD<34>	3.2A 4.5B
FBAD<35>	3.2A 4.5B
FBAD<36>	3.2A 4.5B
FBAD<37>	3.2A 4.5B
FBAD<38>	3.2A 4.5B
FBAD<39>	3.2A 4.5B
FBAD<40>	3.2A 4.5C
FBAD<41>	3.2A 4.5C
FBAD<42>	3.2A 4.5C
FBAD<43>	3.2A 4.5C
FBAD<44>	3.2A 4.5C
FBAD<45>	3.2A 4.5C
FBAD<46>	3.2A 4.5C
FBAD<47>	3.3A 4.5C
FBAD<48>	3.3A 4.5D
FBAD<49>	3.3A 4.5D
FBAD<50>	3.3A 4.5D
FBAD<51>	3.3A 4.5D
FBAD<52>	3.3A 4.5D
FBAD<53>	3.3A 4.5D
FBAD<54>	3.3A 4.5D
FBAD<55>	3.3A 4.5D
FBAD<56>	3.3A 4.5D
FBAD<57>	3.3A 4.5D
FBAD<58>	3.3A 4.5D

FBAD<59>	3.3A 4.5D
FBAD<60>	3.3A 4.5D
FBAD<61>	3.3A 4.5D
FBAD<62>	3.3A 4.5D
FBAD<63>	3.3A 4.5D
FBADQM<0>	3.3A 4.4B
FBADQM<7..0>	3.3A> 4.4A< 4.5F<
FBADQM<1>	3.3A 4.4C
FBADQM<2>	3.3A 4.4D
FBADQM<3>	3.3A 4.4D
FBADQM<4>	3.3A 4.5B
FBADQM<5>	3.3A 4.5C
FBADQM<6>	3.3A 4.5D
FBADQM<7>	3.3A 4.5D
FBADQS0	3.3A<> 4.4B 4.4F<>
FBADQS0*	3.4A<> 4.4B 4.4F<>
FBADQS1	3.4A<> 4.4C 4.4F<>
FBADQS1*	3.4A<> 4.4C 4.4F<>
FBADQS2	3.4A<> 4.4D 4.4F<>
FBADQS2*	3.4A<> 4.4D 4.4F<>
FBADQS3	3.4A<> 4.4D 4.4F<>
FBADQS3*	3.4A<> 4.4D 4.4F<>
FBADQS4	3.4A<> 4.4F<> 4.5B
FBADQS4*	3.4A<> 4.4F<> 4.5B
FBADQS5	3.4A<> 4.4F<> 4.5C
FBADQS5*	3.4A<> 4.4F<> 4.5C
FBADQS6	3.4A<> 4.4F<> 4.5D
FBADQS6*	3.4A<> 4.4F<> 4.5D
FBADQS7	3.4A<> 4.4F<> 4.5D
FBADQS7*	3.4A<> 4.4F<> 4.5D
FBA_A<0>	3.3C 4.1A 4.1C 4.1E
	4.1G
FBA_A<12..0>	3.3D> 4.1A< 4.4F<
FBA_A<1>	3.3C 4.1A 4.1C 4.1E
	4.1G
FBA_A<2>	3.3C 4.1A 4.1C
FBA_A<3>	3.3C 4.1A 4.1C
FBA_A<4>	3.3C 4.1A 4.1C
FBA_A<5>	3.3C 4.1A 4.1C
FBA_A<6>	3.3C 4.1A 4.1C 4.1E
	4.1G
FBA_A<7>	3.3C 4.1A 4.1C 4.1E
	4.1G
FBA_A<8>	3.3C 4.1A 4.1C 4.1E
	4.1G
FBA_A<9>	3.3C 4.2A 4.2C 4.2E
	4.2G
FBA_A<10>	3.3C 4.2A 4.2C 4.2E
	4.2G
FBA_A<11>	3.3C 4.2A 4.2C 4.2E
	4.2G
FBA_A<12>	3.3C 4.2A 4.2C 4.2E
	4.2G
FBA_BA0	3.3D> 4.2A< 4.2C 4.2E
	4.2G 4.4F<
FBA_BA1	3.3D> 4.2A< 4.2C 4.2E
	4.2G 4.4F<
FBA_BA2	3.3D> 4.2A< 4.2C 4.2E
	4.2G 4.4F<
FBA_CAS*	3.4D> 4.1A< 4.1C 4.1E
	4.1G 4.5F<
FBA_CKE	3.3D> 4.2A< 4.2C 4.2E
	4.2G 4.4F<
FBA_CLK0	3.4D> 4.2A 4.2C 4.3A<
	4.4F<
FBA_CLK0*	3.4D> 4.2A 4.2C 4.3C<
	4.4F<
FBA_CLK0_TERM	4.3B
FBA_CLK1	3.4D> 4.2E 4.2G 4.3C<
	4.4F<
FBA_CLK1*	3.4D> 4.2E 4.2G 4.3E<
	4.4F<
FBA_CLK1_TERM	4.3D
FBA_CS0*	3.3D> 4.1A< 4.1C 4.1E
	4.1G 4.5F<
FBA_CS1*	4.5F<
FBA_ODT	3.5D> 4.2A< 4.2C 4.2E
	4.2G 4.5F<
FBA_ODT_GPU	3.1G> 3.4C 3.5C
FBA_PLLAVDD_GPU	3.4C
FBA_RAS*	3.3D> 4.1A< 4.1C 4.1E
	4.1G 4.4F<
FBA_RESET	3.1G> 3.3C 3.5C
FBA_VREF1	4.2B 4.3F<
FBA_VREF2	4.2F 4.3F<
FBA_VREF3	4.2D 4.3F<
FBA_VREF4	4.2H 4.3F<
FBA_WE*	3.3D> 4.1A< 4.1C 4.1E
	4.1G 4.5F<
FBB_A<2>	3.3C 4.1E 4.1G
FBB_A<5..2>	3.3D> 4.1A< 4.4F<
FBB_A<3>	3.3C 4.1E 4.1G
FBB_A<4>	3.3C 4.1E 4.1G
FBB_A<5>	3.3C 4.1E 4.1G
FBCAL_PD	3.4G
FBCAL_PU	3.4G

FBCAL_TERM	3.5G
FBCD<0>	3.1E 5.4B
FBCD<63..0>	3.1E<> 5.4A<> 5.5F<>
FBCD<1>	3.1E 5.4B
FBCD<2>	3.1E 5.4B
FBCD<3>	3.1E 5.4B
FBCD<4>	3.1E 5.4B
FBCD<5>	3.1E 5.4B
FBCD<6>	3.1E 5.4B
FBCD<7>	3.1E 5.4B
FBCD<8>	3.1E 5.4C
FBCD<9>	3.1E 5.4C
FBCD<10>	3.1E 5.4C
FBCD<11>	3.1E 5.4C
FBCD<12>	3.1E 5.4C
FBCD<13>	3.1E 5.4C
FBCD<14>	3.1E 5.4C
FBCD<15>	3.1E 5.4C
FBCD<16>	3.1E 5.4D
FBCD<17>	3.2E 5.4D
FBCD<18>	3.2E 5.4D
FBCD<19>	3.2E 5.4D
FBCD<20>	3.2E 5.4D
FBCD<21>	3.2E 5.4D
FBCD<22>	3.2E 5.4D
FBCD<23>	3.2E 5.4D
FBCD<24>	3.2E 5.4D
FBCD<25>	3.2E 5.4D
FBCD<26>	3.2E 5.4D
FBCD<27>	3.2E 5.4D
FBCD<28>	3.2E 5.4D
FBCD<29>	3.2E 5.4D
FBCD<30>	3.2E 5.4D
FBCD<31>	3.2E 5.4D
FBCD<32>	3.2E 5.5B
FBCD<33>	3.2E 5.5B
FBCD<34>	3.2E 5.5B
FBCD<35>	3.2E 5.5B
FBCD<36>	3.2E 5.5B
FBCD<37>	3.2E 5.5B
FBCD<38>	3.2E 5.5B
FBCD<39>	3.2E 5.5B
FBCD<40>	3.2E 5.5C
FBCD<41>	3.2E 5.5C
FBCD<42>	3.2E 5.5C
FBCD<43>	3.2E 5.5C
FBCD<44>	3.2E 5.5C
FBCD<45>	3.2E 5.5C
FBCD<46>	3.2E 5.5C
FBCD<47>	3.3E 5.5C
FBCD<48>	3.3E 5.5D
FBCD<49>	3.3E 5.5D
FBCD<50>	3.3E 5.5D
FBCD<51>	3.3E 5.5D
FBCD<52>	3.3E 5.5D
FBCD<53>	3.3E 5.5D
FBCD<54>	3.3E 5.5D
FBCD<55>	3.3E 5.5D
FBCD<56>	3.3E 5.5D
FBCD<57>	3.3E 5.5D
FBCD<58>	3.3E 5.5D
FBCD<59>	3.3E 5.5D
FBCD<60>	3.3E 5.5D
FBCD<61>	3.3E 5.5D
FBCD<62>	3.3E 5.5D
FBCD<63>	3.3E 5.5D
FBCDQM<0>	3.3E 5.4B
FBCDQM<7..0>	3.3E> 5.4A< 5.5F<
FBCDQM<1>	3.3E 5.4C
FBCDQM<2>	3.3E 5.4D
FBCDQM<3>	3.3E 5.4D
FBCDQM<4>	3.3E 5.5B
FBCDQM<5>	3.3E 5.5C
FBCDQM<6>	3.3E 5.5D
FBCDQM<7>	3.3E 5.5D
FBCDQS0	3.3E<> 5.4B 5.4F<>
FBCDQS0*	3.4E<> 5.4B 5.4F<>
FBCDQS1	3.4E<> 5.4C 5.4F<>
FBCDQS1*	3.4E<> 5.4C 5.4F<>
FBCDQS2	3.4E<> 5.4D 5.4F<>
FBCDQS2*	3.4E<> 5.4D 5.4F<>
FBCDQS3	3.4E<> 5.4D 5.4F<>
FBCDQS3*	3.4E<> 5.4D 5.4F<>
FBCDQS4	3.4E<> 5.4F<> 5.5B
FBCDQS4*	3.4E<> 5.4F<> 5.5B
FBCDQS5	3.4E<> 5.4F<> 5.5C
FBCDQS5*	3.4E<> 5.4F<> 5.5C
FBCDQS6	3.4E<> 5.4F<> 5.5D
FBCDQS6*	3.4E<> 5.4F<> 5.5D
FBCDQS7	3.4E<> 5.4F<> 5.5D
FBCDQS7*	3.4E<> 5.4F<> 5.5D
FBC_A<0>	3.3G 5.1A 5.1C 5.1E
	5.1G
FBC_A<12..0>	3.3H> 5.1A< 5.4F<
FBC_A<1>	3.3G 5.1A 5.1C 5.1E
	5.1G

FBC_A<2>	3.3G 5.1A 5.1C
FBC_A<3>	3.3G 5.1A 5.1C
FBC_A<4>	3.3G 5.1A 5.1C
FBC_A<5>	3.3G 5.1A 5.1C
FBC_A<6>	3.3G 5.1A 5.1C 5.1E
	5.1G
FBC_A<7>	3.3G 5.1A 5.1C 5.1E
	5.1G
FBC_A<8>	3.3G 5.1A 5.1C 5.1E
	5.1G
FBC_A<9>	3.3G 5.1A 5.1C 5.1E
	5.1G
FBC_A<10>	3.3G 5.1A 5.1C 5.1E
	5.1G
FBC_A<11>	3.3G 5.1A 5.1C 5.1E
	5.1G
FBC_A<12>	3.3G 5.2A 5.2C 5.2E
	5.2G
FBC_BA0	3.3H> 5.2A< 5.2C 5.2E
	5.2G 5.4F<
FBC_BA1	3.3H> 5.2A< 5.2C 5.2E
	5.2G 5.4F<
FBC_BA2	3.3H> 5.2A< 5.2C 5.2E
	5.2G 5.4F<
FBC_CAS*	3.4H> 5.1A< 5.1C 5.1E
	5.1G 5.5F<
FBC_CKE	3.3H> 5.2A< 5.2C 5.2E
	5.2G 5.4F<
FBC_CLK0	3.4H> 5.2A 5.2C 5.3A<
	5.3F<
FBC_CLK0*	3.4H> 5.2A 5.2C 5.3B<
	5.4F<
FBC_CLK0_TERM	5.3B
FBC_CLK1	3.4H> 5.2E 5.2G 5.3C<
	5.4F<
FBC_CLK1*	3.4H> 5.2E 5.2G 5.3E<
	5.4F<
FBC_CLK1_TERM	5.3D
FBC_CS0*	3.3H> 5.1A< 5.1C 5.1E
	5.1G 5.5F<
FBC_CS1*	5.5F<
FBC_ODT	3.5D> 5.2A< 5.2C 5.2E
	5.2G 5.5F<
FBC_ODT_GPU	3.1G> 3.4G 3.5C
FBC_PLLAVDD	3.4G
FBC_RAS*	3.3H> 5.1A< 5.1C 5.1E
	5.1G 5.5F<
FBC_RESET	3.1G> 3.3G 3.5C
FBC_VREF1	5.2B 5.3F<
FBC_VREF2	5.2F 5.3F<
FBC_VREF3	5.2D 5.3F<
FBC_VREF4	5.2H 5.3F<
FBC_WE*	3.3H> 5.1A< 5.1C 5.1E
	5.1G 5.5F<
FBD_A<2>	3.3G 5.1E 5.1G
FBD_A<5..2>	3.3H> 5.1A< 5.4F<
FBD_A<3>	3.3G 5.1E 5.1G
FBD_A<4>	3.3G 5.1E 5.1G
FBD_A<5>	3.3G 5.1E 5.1G
FBVDDQ	14.1G
FB_BOOT	14.2C
FB_BOOTC	14.2D
FB_COMP	14.3B
FB_COMP1	14.3C
FB_DH	14.2C
FB_DL	14.2C
FB_FB	14.3D
FB_FSET	14.2B
FB_ISEN	14.2C
FB_PHASE	14.2C
FB_PWRGOOD	8.2A< 14.2A>
FB_SNUBBER	14.2E
FB_VCC	14.2B
FB_VREF1	3.5A
FB_VREF2	3.5E
GPIO0_DVI_A_HPD	10.3D
GPIO1_DVI_B_HPD	8.4A< 10.3F>
GPIO2_BL_PWM	9.3B< 10.3F>
GPIO3_PPEN	9.3B< 10.3F>
GPIO3_PPEN_GPU	10.3D
GPIO4_BLEN	9.3B< 10.3F>
GPIO4_BLEN_GPU	10.3D
GPIO5_NVVDDCTL0	10.3F> 13.4B<
GPIO6_NVVDDCTL1	10.3F> 13.4B<
GPIO8_THERM_ALERT*	10.3D
GPIO_AC_BATT*	9.4B> 10.3F<
GPIO_SLI_SYNC	9.3H<> 10.3F<>
I2CA_SCL	7.1D
I2CA_SCL_R	7.1F> 9.3B<
I2CA_SDA	7.1D
I2CA_SDA_R	7.1F<> 9.3B<>
I2CB_SCL	7.3D
I2CB_SCL_R	7.3G> 9.2B<
I2CB_SDA	7.3D
I2CB_SDA_R	7.3G<> 9.2B<>
I2CC_SCL	10.3D

I2CC_SCL_R	9.4B< 10.3F> 11.2B<
I2CC_SDA	10.3D
I2CC_SDA_R	9.4B<> 10.3F<>
	11.2B<>
I2CH_SCL	11.4C
I2CH_SDA	11.4C
IFPABIOVDD	8.2D
IFPABPLLVDD	8.1D
IFPABRSET	8.1D
IFPATXC	8.1H> 9.4G<
IFPATXC*	8.1H> 9.4G<
IFPATXD0	8.1H> 9.4G<
IFPATXD0*	8.1H> 9.4G<
IFPATXD1	8.1H> 9.4G<
IFPATXD1*	8.1H> 9.4G<
IFPATXD2	8.2H> 9.4G<
IFPATXD2*	8.2H> 9.4G<
IFPATXD3	8.2H> 9.4G<
IFPATXD3*	8.2H> 9.4G<
IFPBTXC	8.2H> 9.4G<
IFPBTXC*	8.2H> 9.4G<
IFPBTXD4	8.2H> 9.3G<
IFPBTXD4*	8.2H> 9.3G<
IFPBTXD5	8.2H> 9.3G<
IFPBTXD5*	8.2H> 9.3G<
IFPBTXD6	8.2H> 9.4G<
IFPBTXD6*	8.2H> 9.4G<
IFPBTXD7	8.2H> 9.4G<
IFPBTXD7*	8.2H> 9.4G<
IFPCDBRSET	8.3D
IFPCDPLLVDD	8.3D
IFPCTXC	8.3H> 9.2G<
IFPCTXC*	8.3H> 9.2G<
IFPCTXD0	8.3H> 9.2G<
IFPCTXD0*	8.3H> 9.2G<
IFPCTXD1	8.3H> 9.2G<
IFPCTXD1*	8.3H> 9.2G<
IFPCTXD2	8.4H> 9.2G<
IFPCTXD2*	8.4H> 9.2G<
IFPC_IOVDD	8.4D
IFPDTXC	8.4H> 9.3G<
IFPDTXC*	8.4H> 9.3G<
IFPDTXD3	8.4H> 9.2G<
IFPDTXD3*	8.4H> 9.2G<
IFPDTXD4	8.4H> 9.2G<
IFPDTXD4*	8.4H> 9.2G<
IFPDTXD5	8.4H> 9.2G<
IFPDTXD5*	8.4H> 9.2G<
IFPD_IOVDD	8.4D
JTAG_TCLK	10.3B
JTAG_TDI	10.3B
JTAG_TDO	10.3B
JTAG_TMS	10.3B
JTAG_TRST	10.3B
LVDS_IOVDD	8.2B
MIOACAL_PD_VDDQ	12.2C
MIOACAL_PU_GND	12.2C
MIOA_VDDQ	12.1C
MIOA_VREF	12.2C
MIOB_CTL3	12.4F< 15.2C 15.4B>
M_GPIO8_SLOWDOWN*	10.2C
M_THERM_ALERT*	10.2C
NVCTLO_R	13.4D
NVCTL1_R	13.4D
NVVDD	13.1G
NVVDDCTL0	13.4D
NVVDDCTL1	13.4C
NVVDD_SENSE	2.3G> 13.3G<
NVVDD_SENSE_FB	13.3F
NV_BOOT	13.2C
NV_BOOTC	13.2D
NV_COMP	13.2C
NV_COMP1	13.3C
NV_DH	13.2C
NV_DL	13.2C
NV_FB	13.3D
NV_FSET	13.2B
NV_ISEN	13.2C
NV_PHASE	13.2C
NV_PWRGOOD	10.2F< 13.2B> 14.2A<
NV_SNUBBER	13.2F
NV_VCC	13.2B
PCI_DEVID3	12.4F< 15.2C 15.4B>
PEX1V2	14.1G
PEX1V2_FB	14.4D
PEX_PLLDVDD	2.4F
PEX_RCLK	2.2E
PEX_RCLK*	2.2E
PEX_RST	2.1D
PEX_RX0	2.2E
PEX_RX0*	2.2E
PEX_RX1	2.2E
PEX_RX1*	2.2E
PEX_RX2	2.2E
PEX_RX2*	2.2E
PEX_RX3	2.3E

PEX_RX3*	2.3E
PEX_RX4	2.3E
PEX_RX4*	2.3E
PEX_RX5	2.3E
PEX_RX5*	2.3E
PEX_RX6	2.3E
PEX_RX6*	2.3E
PEX_RX7	2.3E
PEX_RX7*	2.3E
PEX_RX8	2.4E
PEX_RX8*	2.4E
PEX_RX9	2.4E
PEX_RX9*	2.4E
PEX_RX10	2.4E
PEX_RX10*	2.4E
PEX_RX11	2.4E
PEX_RX11*	2.4E
PEX_RX12	2.4E
PEX_RX12*	2.4E
PEX_RX13	2.5E
PEX_RX13*	2.5E
PEX_RX14	2.5E
PEX_RX14*	2.5E
PEX_RX15	2.5E
PEX_RX15*	2.5E
PEX_TSTCLK	2.2E
PEX_TSTCLK*	2.2E
PEX_TX0	2.2E
PEX_TX0*	2.2E
PEX_TX0_C	2.2B
PEX_TX0_C*	2.2B
PEX_TX1	2.2E
PEX_TX1*	2.2E
PEX_TX1_C	2.2B
PEX_TX1_C*	2.2B
PEX_TX2	2.2E
PEX_TX2*	2.2E
PEX_TX2_C	2.2B
PEX_TX2_C*	2.2B
PEX_TX3	2.3E
PEX_TX3*	2.3E
PEX_TX3_C	2.3B
PEX_TX3_C*	2.3B
PEX_TX4	2.3E
PEX_TX4*	2.3E
PEX_TX4_C	2.3B
PEX_TX4_C*	2.3B
PEX_TX5	2.3E
PEX_TX5*	2.3E
PEX_TX5_C	2.3B
PEX_TX5_C*	2.3B
PEX_TX6	2.3E
PEX_TX6*	2.3E
PEX_TX6_C	2.3B
PEX_TX6_C*	2.3B
PEX_TX7	2.3E
PEX_TX7*	2.3E
PEX_TX7_C	2.3B
PEX_TX7_C*	2.3B
PEX_TX8	2.4E
PEX_TX8*	2.4E
PEX_TX8_C	2.4B
PEX_TX8_C*	2.4B
PEX_TX9	2.4E
PEX_TX9*	2.4E
PEX_TX9_C	2.4B
PEX_TX9_C*	2.4B
PEX_TX10	2.4E
PEX_TX10*	2.4E
PEX_TX10_C	2.4B
PEX_TX10_C*	2.4B
PEX_TX11	2.4E
PEX_TX11*	2.4E
PEX_TX11_C	2.4B
PEX_TX11_C*	2.4B
PEX_TX12	2.4E
PEX_TX12*	2.4E
PEX_TX12_C	2.4B
PEX_TX12_C*	2.4B
PEX_TX13	2.5E
PEX_TX13*	2.5E
PEX_TX13_C	2.5B
PEX_TX13_C*	2.5B
PEX_TX14	2.5E
PEX_TX14*	2.5E
PEX_TX14_C	2.5B
PEX_TX14_C*	2.5B
PEX_TX15	2.5E
PEX_TX15*	2.5E
PEX_TX15_C	2.5B
PEX_TX15_C*	2.5B
PLLVDD	7.4C
PWR_SRC	9.1G
RAMCFG0	12.3F< 15.1C 15.3B>
RAMCFG1	12.3F< 15.2C 15.4B>
RAMCFG2	12.3F< 15.2C 15.4B>

RAMCFG3	12.3F< 15.2C 15.4B>
ROMCS*	11.3C
ROM_SCLK	11.3C
ROM_SI	11.3C< 15.3C 15.4B>
ROM_SO	11.3C
RUNPWROK	8.4A< 9.4A> 11.2B<
	13.2B< 14.4C<
RUNPWROK*	8.4B
RUNPWROK_IN	9.4C
SLI_CLKOUT	9.3G<> 12.2F<>
SLI_D<0>	9.3E 12.1E
SLI_D<14..0>	9.3F<> 12.1F<> 15.4B>
SLI_D<1>	9.3E 12.1E
SLI_D<2>	9.3E 12.1E
SLI_D<3>	9.3E 12.1E
SLI_D<4>	9.3E 12.2E
SLI_D<5>	9.3E 12.2E
SLI_D<6>	9.3E 12.2E
SLI_D<7>	9.3E 12.2E
SLI_D<8>	9.3E 12.2E
SLI_D<9>	9.3E 12.2E
SLI_D<10>	9.3E 12.2E
SLI_D<11>	9.3E 12.2E
SLI_D<12>	9.3E 12.2E
SLI_D<13>	9.3E 12.2E 15.3C
SLI_D<14>	9.3E 12.2E
SLI_DE	9.3G<> 12.2F<>
SLI_REFCLK	9.3G<> 12.4F<>
SLI_SWAP_OUT	9.3H<> 11.4C<>
SMB_CLK	9.4B> 10.2A<
SMB_CLK_GPU	10.3D
SMB_DAT	9.4B<> 10.2A<>
SMB_DATA_GPU	10.3D
SNN_A2_M1	4.2A
SNN_A2_M2	4.2C
SNN_A2_M3	4.2E
SNN_A2_M4	4.2G
SNN_A2_M5	5.2A
SNN_A2_M6	5.2C
SNN_A2_M7	5.2E
SNN_A2_M8	5.2G
SNN_BUFRST*	11.4C
SNN_CLAMP_F6	10.3D
SNN_DACB_CSYNC	7.2D
SNN_DACC_BLUE	7.3D
SNN_DACC_GREEN	7.3D
SNN_DACC_HSYNC	7.3D
SNN_DACC_RED	7.3D
SNN_DACC_RSET	7.3C
SNN_DACC_VREF	7.3C
SNN_DACC_VSYNC	7.3D
SNN_E2_M1	4.2A
SNN_E2_M2	4.2C
SNN_E2_M3	4.2E
SNN_E2_M4	4.2G
SNN_E2_M5	5.2A
SNN_E2_M6	5.2C
SNN_E2_M7	5.2E
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ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
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ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
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ASSEMBLY	G84M-600 450/400 256MB 128bit GDDR2 16Mx16 84FBGA, LVDS + DVI_A/DVI_B + TV_OUT + VGA, MXM-II, HDCP.
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