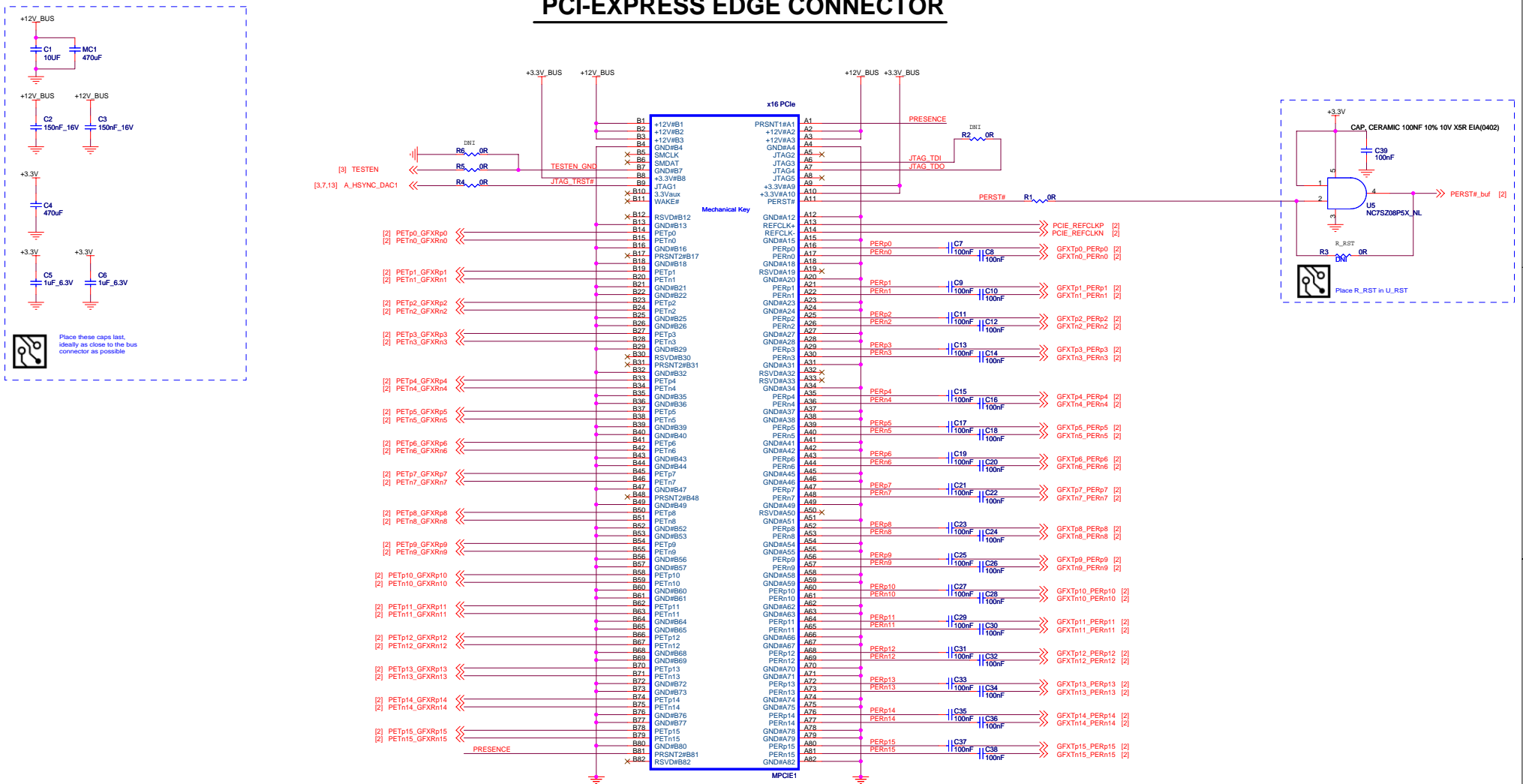


PCI-EXPRESS EDGE CONNECTOR

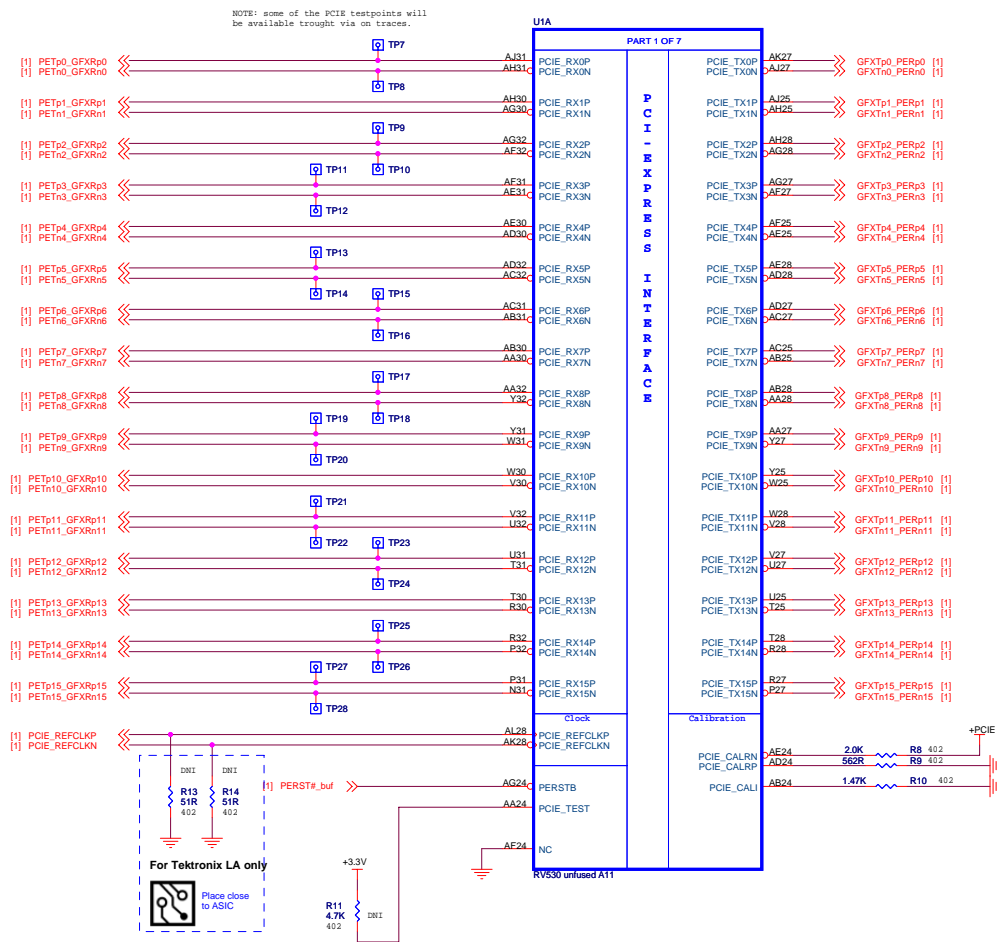


SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND



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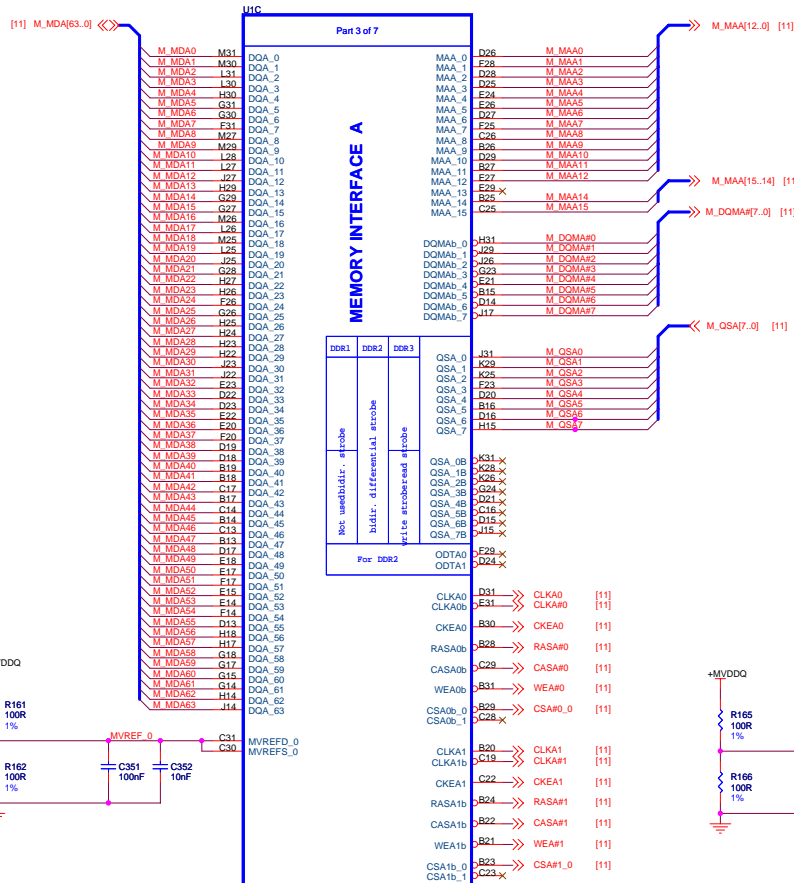


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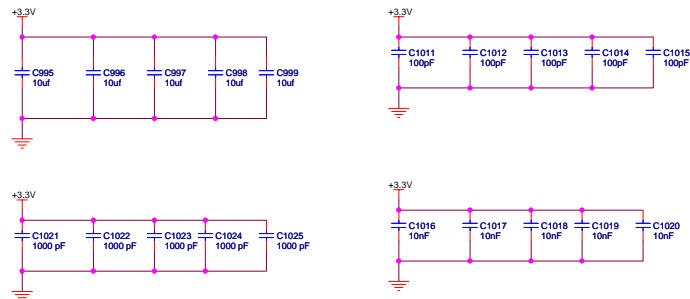
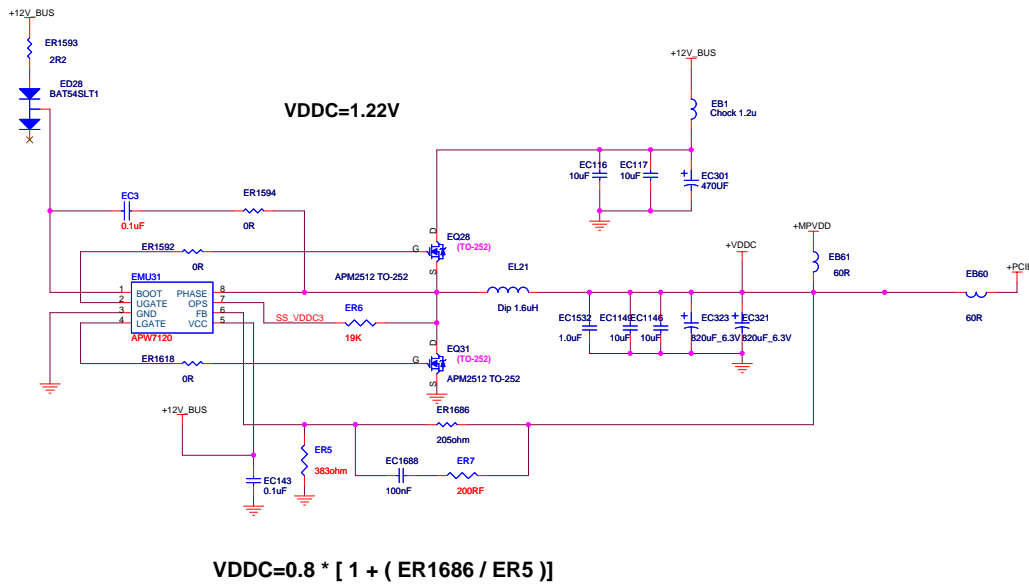
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RV530 MEMORY CHANNELS A and B

Channel A



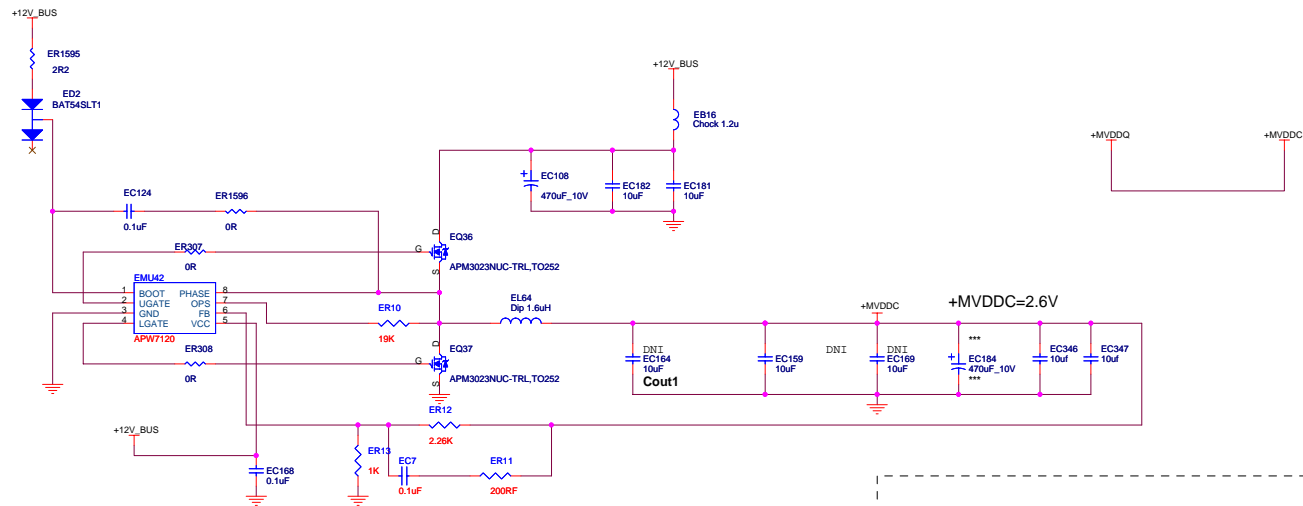
CORE REGULATOR +VDDC



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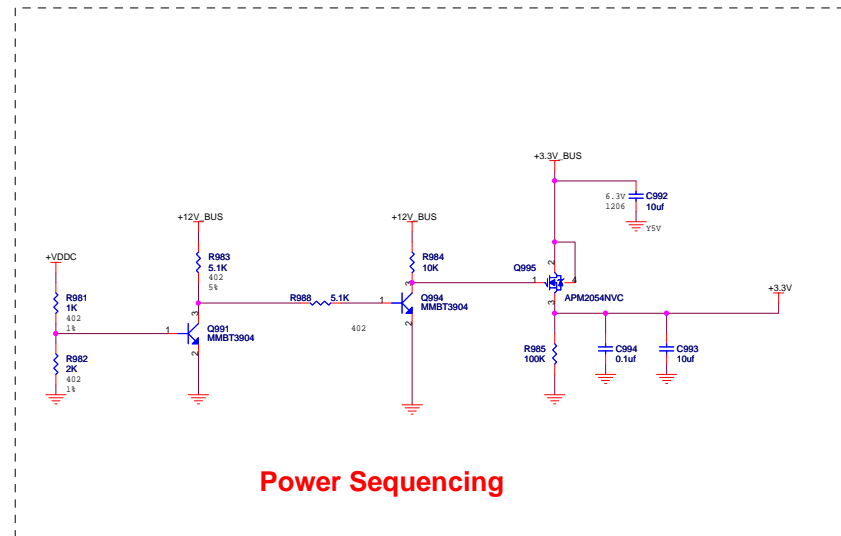
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$$MVDDC = 0.8 * [1 + (ER12 / ER13)]$$

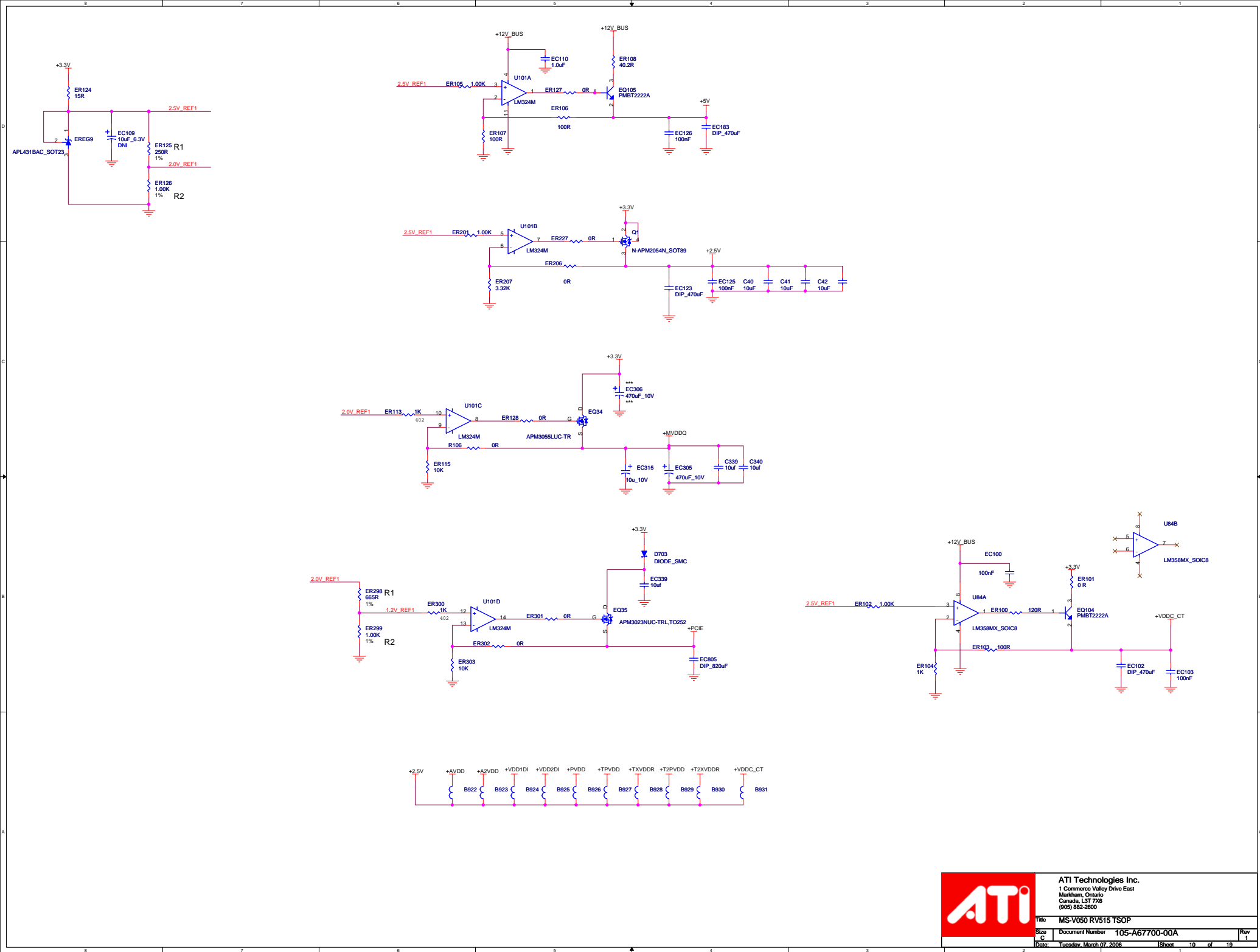
	ER12	ER13
2.6V	R11-2261T13-W08	R11-0102T23-R01



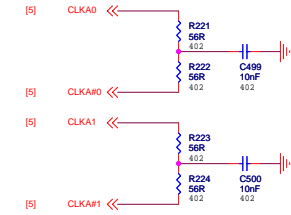
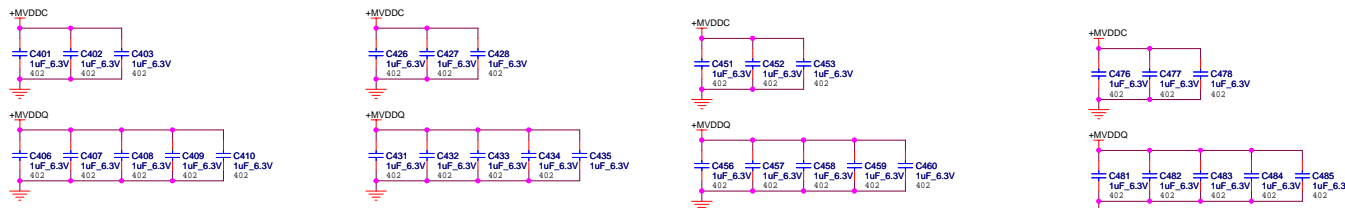
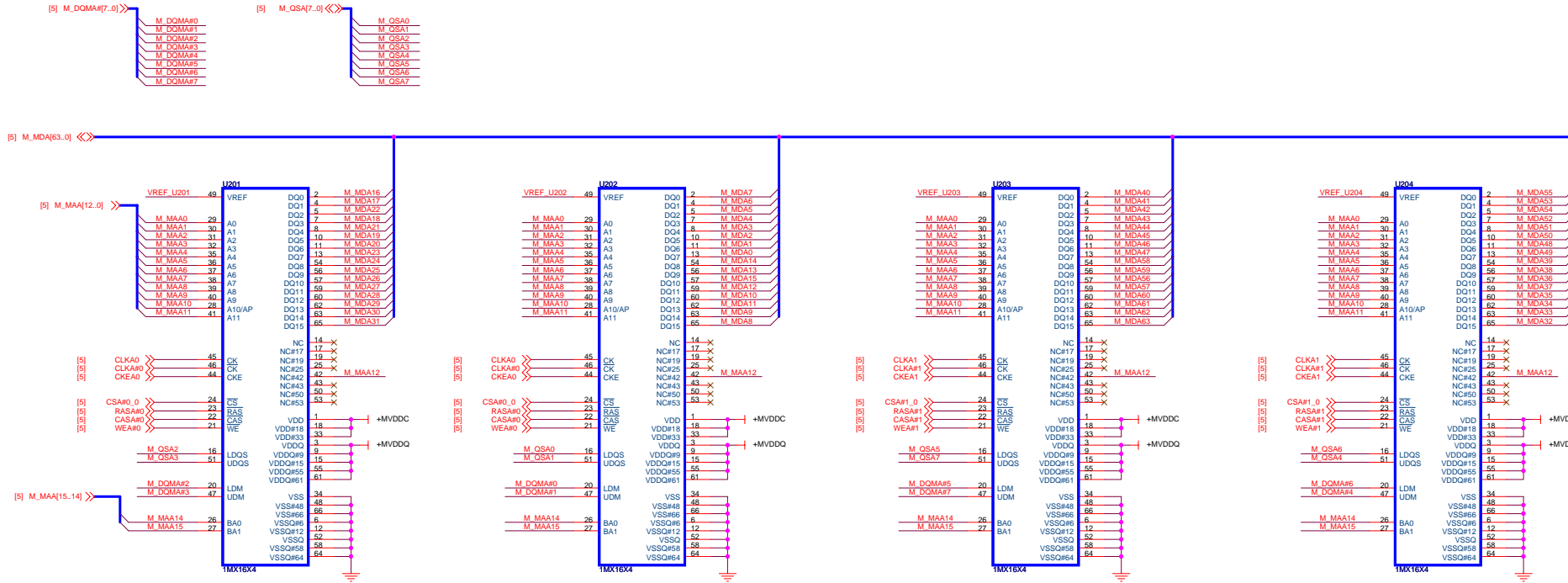
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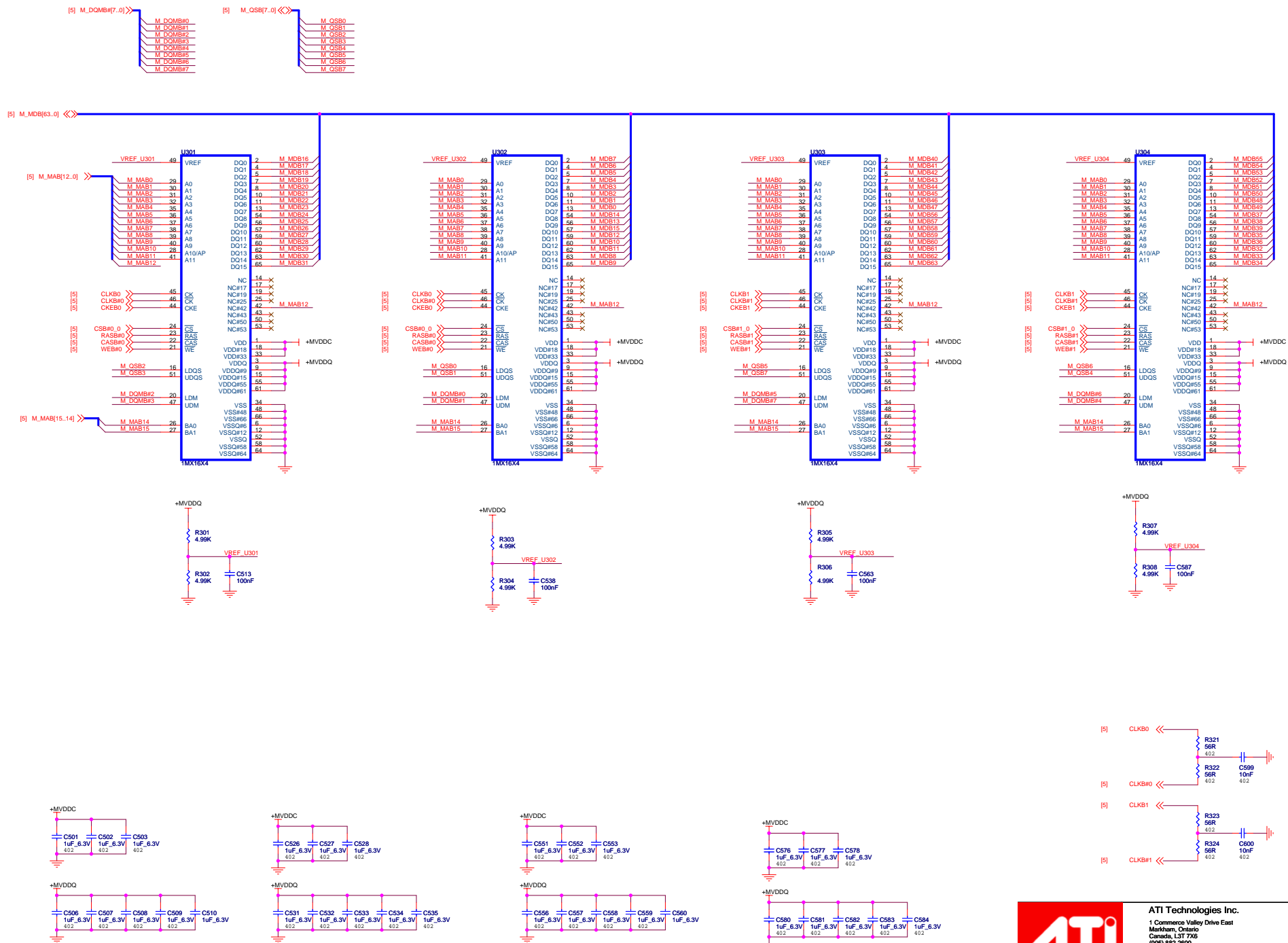
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CHANNEL A: RANK 0 128/256MB DDR1



CHANNEL B: RANK 0 128/256MB DDR1



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[3] A_R_DAC2
[3] A_G_DAC2
[3] A_B_DAC2

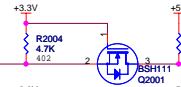
L2001 47nH
L2002 47nH
L2003 47nH
A_R_DAC2_M L2004 47nH
A_G_DAC2_M L2005 47nH
A_B_DAC2_M L2006 47nH

R2001 75R
R2002 75R
R2003 75R
C2004 3.3pF
C2005 3.3pF
C2006 3.3pF
C2001 8.0pF
C2002 8.0pF
C2003 8.0pF



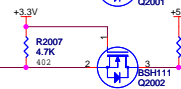
RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane

[3] CRT2DDCDA



R2006 33R 402 DDCDATA_DAC2_R

[3] CRT2DDCLK



R2009 33R 402 DDCCLK_DAC2_R

[3,7] A_HSYNC_DAC2



R2010 33R 402 A_HSYNC_DAC2_R

[3,7] A_VSYNC_DAC2



R2011 33R 402 A_VSYNC_DAC2_R



SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane



[3] HPD1

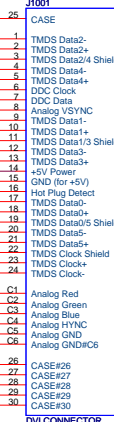
These resistors can be placed close to the ASIC so single net is needed



[3] TX2M
[3] TX2P
[3] TX4M
[3] TX4P
[3] TX1M
[3] TX1P
[3] TX3M
[3] TX3P
[3] TX0M
[3] TX0P
[3] TX5M
[3] TX5P
[3] TXCP
[3] TXCM

A_R_DAC3_F
A_G_DAC3_F
A_B_DAC3_F
A_HSYNC_DAC2_R

+5V_VESA2



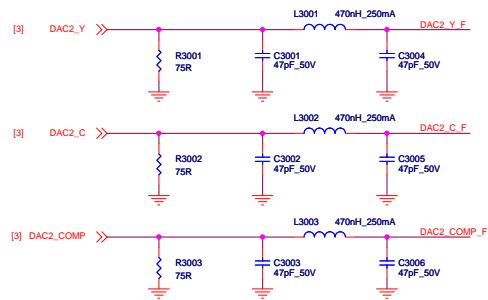
DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	Optional
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCD	SCD	Optional
9	N/C	+5V	+5V	+5V	Optional
Support	Mechanical Key	50mA min 1A max	50mA min 1A max	50mA min 1A max	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

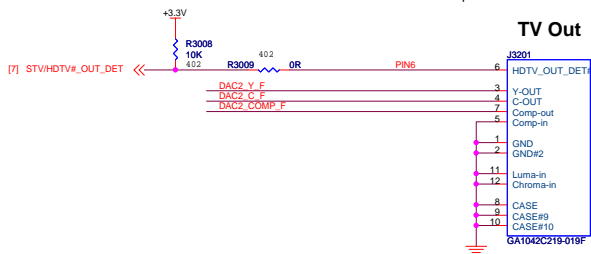


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Place near connector
OR leaves footprint for Ferrite
Beads if req'd for EMI



TV Out

The 7-pin MiniDIN footprint allows one of the two MiniDINs:

- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

7 pin N56-07F0021-F02

9 pin N56-09F0031-F02



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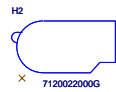
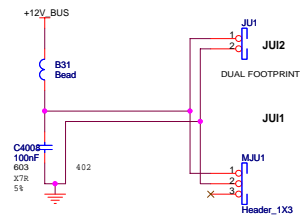
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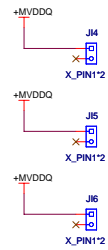
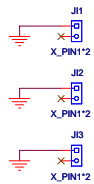
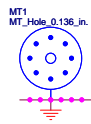
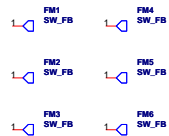
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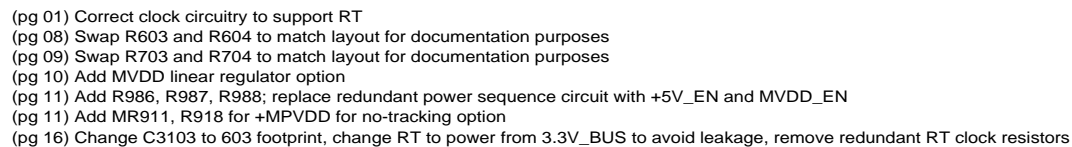
<Variant Name>

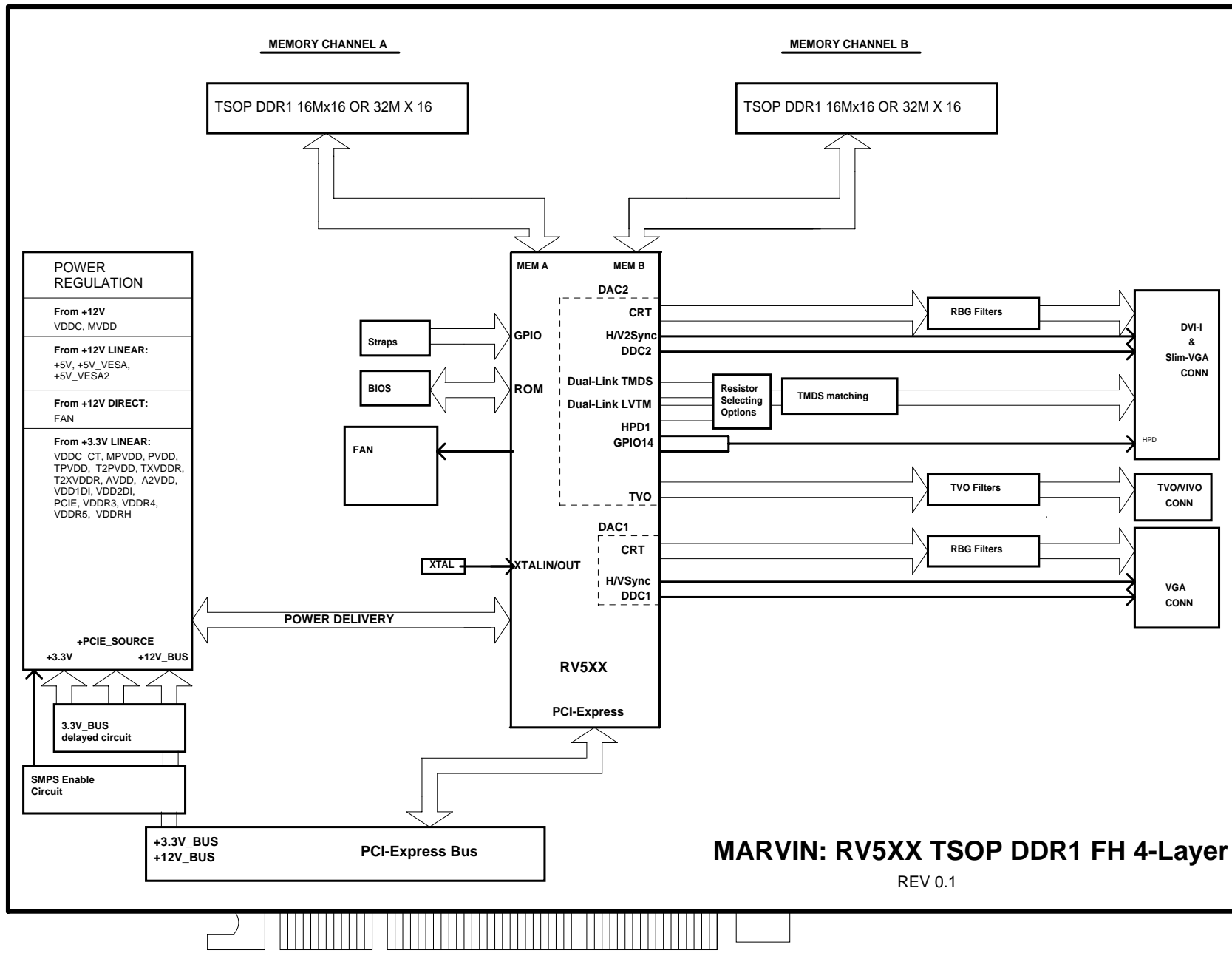


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Rev
1





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