P191-A02 DESIGN

REVISION HISTORY:

8/22/03: P191 was cloned from P193
8/22/03: Page(S) 4,5,7,8) - Changed Memory termination to FBVTT parrallel and added de-coupling caps.
8/26/03: Page(S) 22 - FBVDD(Q) power supply was changed from individual (HIP6012) switchers.
8/26/03: to a dual switcher (ISL6225) that generates FBVDD(Q) and FBVTT.
8/26/03: The Linear Sink/Source that generated FVBTT was also removed.
8/26/03: Page 21 - Added 10K pullup to NV_PGOOD
8/26/03: Page 6 - Added Low pass filter to GPU_VTT
8/27/03: Page 15 - Changed R562 to a 0603 to facilitate routing
8/29/03: Page 21 - Removed C765 and connected U510.12 to U510.17 (NV_SFTSTRT)
9/03/03: Page 21 - Added Schmoo two 10K (NO_STUFF) resistors for NVVDD Schmoo circuit.
9/04/03: Page 21 - Added Silent Running
9/04/08: X-Released
9/18/08: CLoned from P191-A00
9/18/03: Pages 2, 21 - Added two resistors for Droop Compensation
9/18/03: Page 12 - Removed Link-B from design
9/18/03: Page 22 - Added test point for FBVTT
10/23/03: Page 12 - Added CAP to IFPBIOVDD
10/23/03: Page 12 - Connected IFPBIOVDD to IFPAIOVDD

PAGE SUMMARY:

1. This page: Page summary, revision history and variant info table
2. AGP/PCI
3. FBA partition, FBVDDQ decoupling, FBDLLVDD decoupling
4. FBA0 qty 2 8Mx16 DDR1 memories,decoupling.
5. FBA1 qty 2 8Mx16 DDR1 memories,decoupling.
6. FBC partition, FBVTT, FBCAL
7. FBC0 qty 2 8Mx16 DDR1 memories,decoupling.
8. FBC1 qty 2 8Mx16 DDR1 memories,decoupling.
9. Ground, Thermal grounds and NCs.
10. DACA, DACB, DAC sync buffers, PLL, XTAL
11. DACA RGB and EMI filters, DB15 primary slim VGA connector
12. Internal TMDS Link A+B, Internal TMDS DVI-I connector
13. DACA RGB and EMI filters, DB15 primary slim VGA connector
14. Internal TMDS Link C, Internal TMDS DVI-I connector
15. NV36 VIP, NV36 DVOA
16. 7114 video capture
17. Mini Din Video In/Out Connector
18. 4-pin Video-In, 10-pin Video-In Connector
19. BIOS serial ROM, Temperature Sensor, PWM Fan Control.
20. Linear Regulators for A3V3, TMDSAB_PLLVDD, TMDSAB_IOVDD
21. NVVDD Switcher.
22. FBVDDQ Switcher
23. FBVDD Switcher
24. Strap Configurations

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	602-10191-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	600101910000200	602-10191-0000-200	NV36-U Gen 425/275 128MB 8Mx16 VGA+VO+DVI
2	600101910001200	602-10191-0001-200	NV36-U Gen 425/275 128MB 8Mx16 VGA+VIVO+DVI - VGA South - DVI-I North
3	600101910003200	602-10191-0003-200	NV36-U Gen 425/275 256MB 16Mx16 DVII+VIVO+DVII - ENGINEERING
4	600101910002200	602-10191-0002-200	NV36-U Gen 425/275 128MB 8Mx16 DVII+VO+VGA - VGA South - DVII North
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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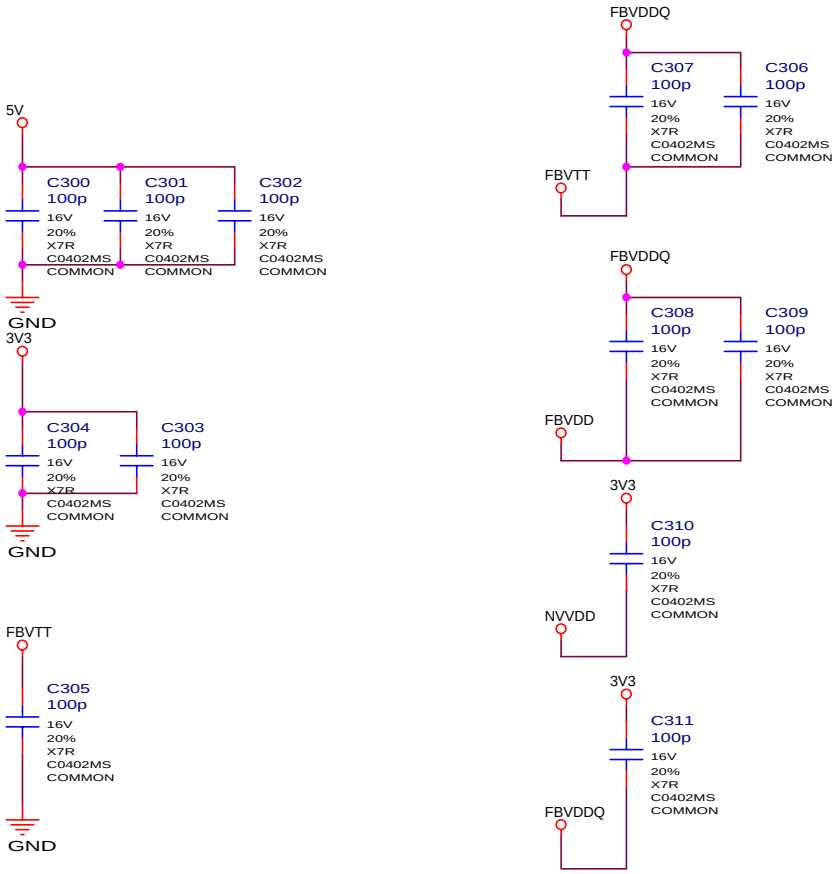

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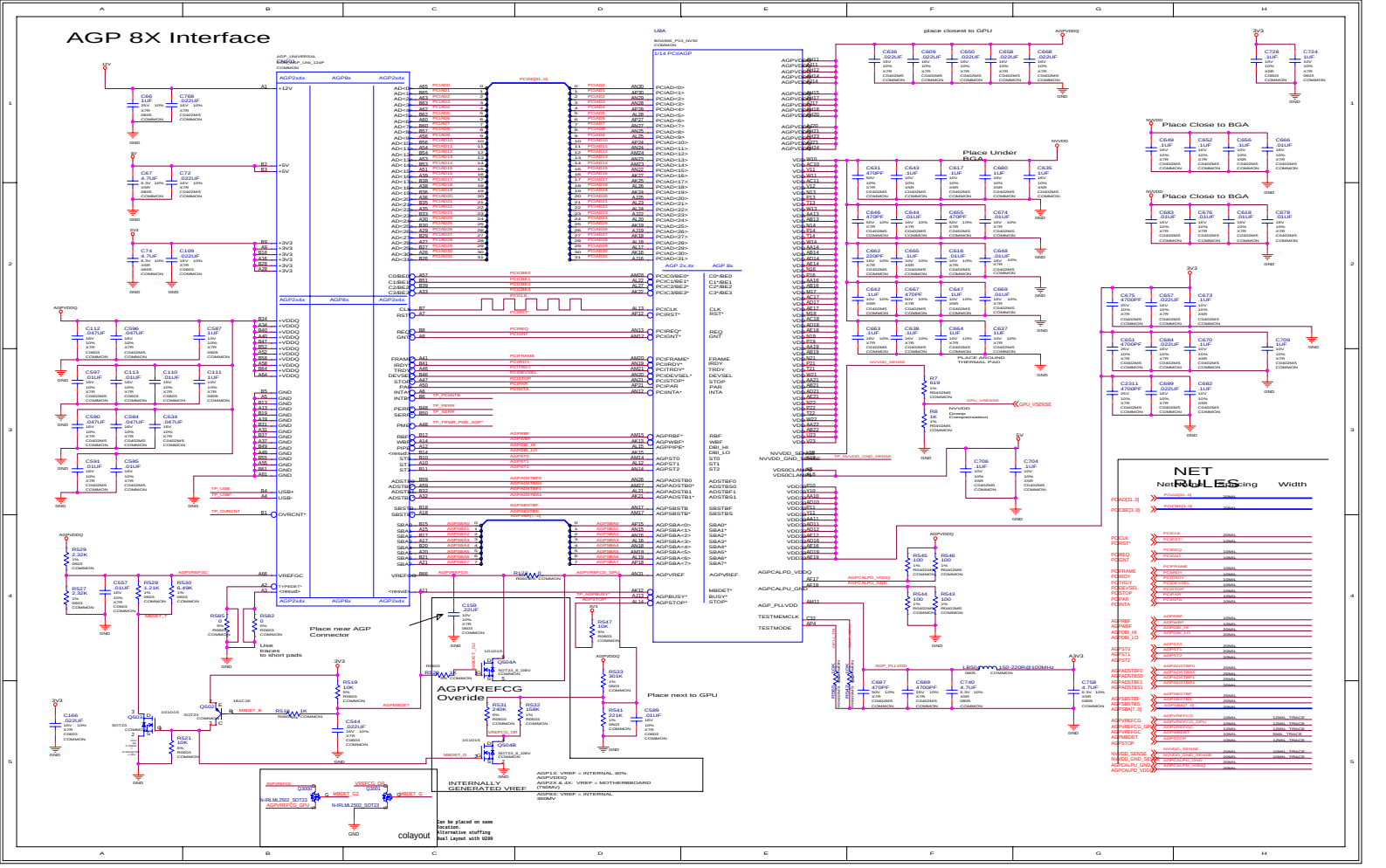
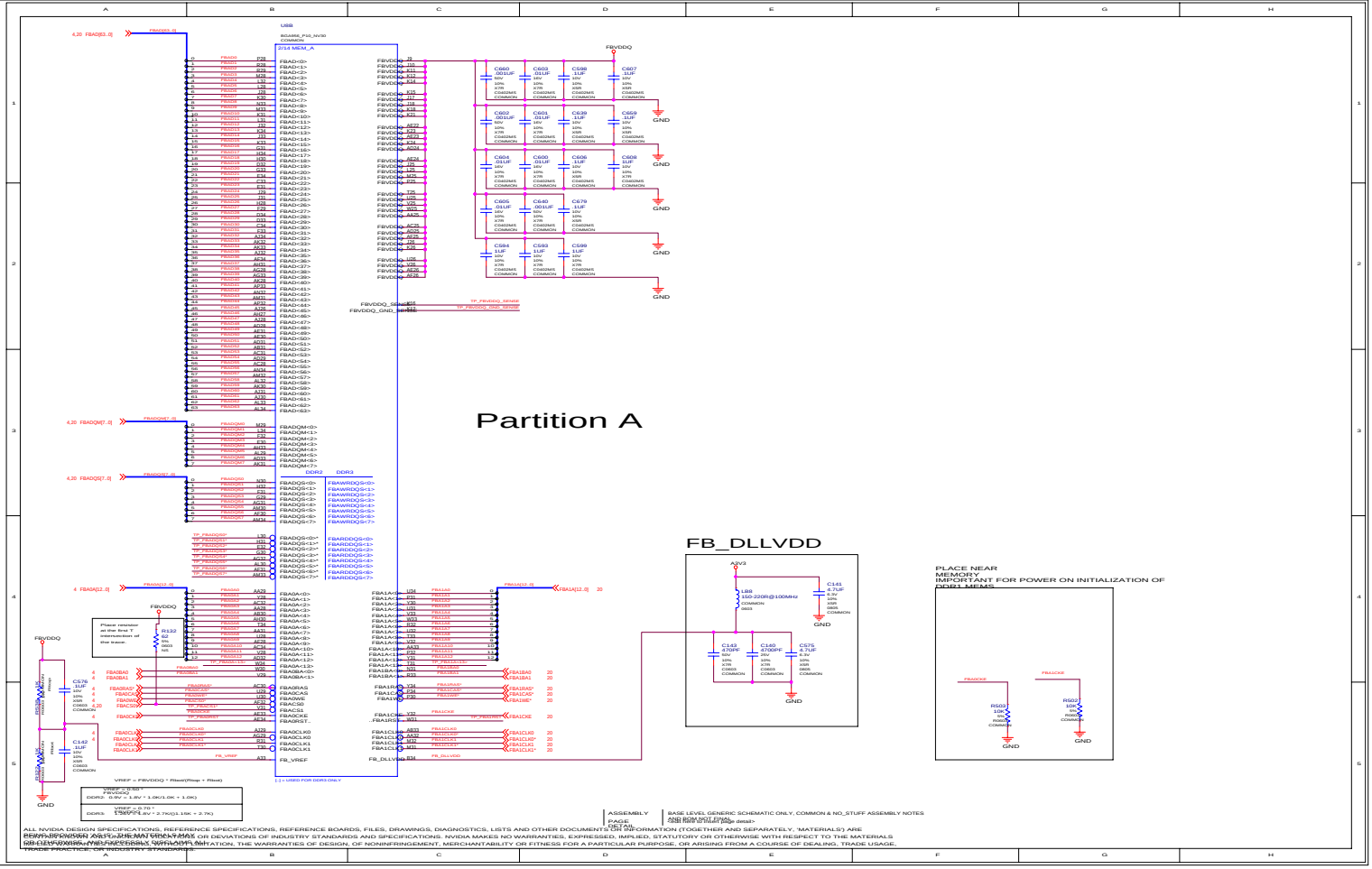
Size A	Document Number <Doc>	Rev <RevCo
Date: Monday, February 23, 2004	Sheet 1 of 1	


AGP 8X Interface
Place near AGP Connector
Use traces to short pads
Place next to GPU
Place under BGA
Place Close to BGA
Place Close to BGA
place closest to GPU
AGPVREFCG
Overide
INTERNALLY GENERATED VREF
colayout
NET
Net Physical Spacing
Width



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PAGE DETAIL: <Add BOM and Layer detail>

MEMORY 8(16)Mx16DDR Partition A , Bits 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

NET	Diffpair	NET_SPACING_RULE

TOP

BOTTOM

Clock Termination

FB_VREF

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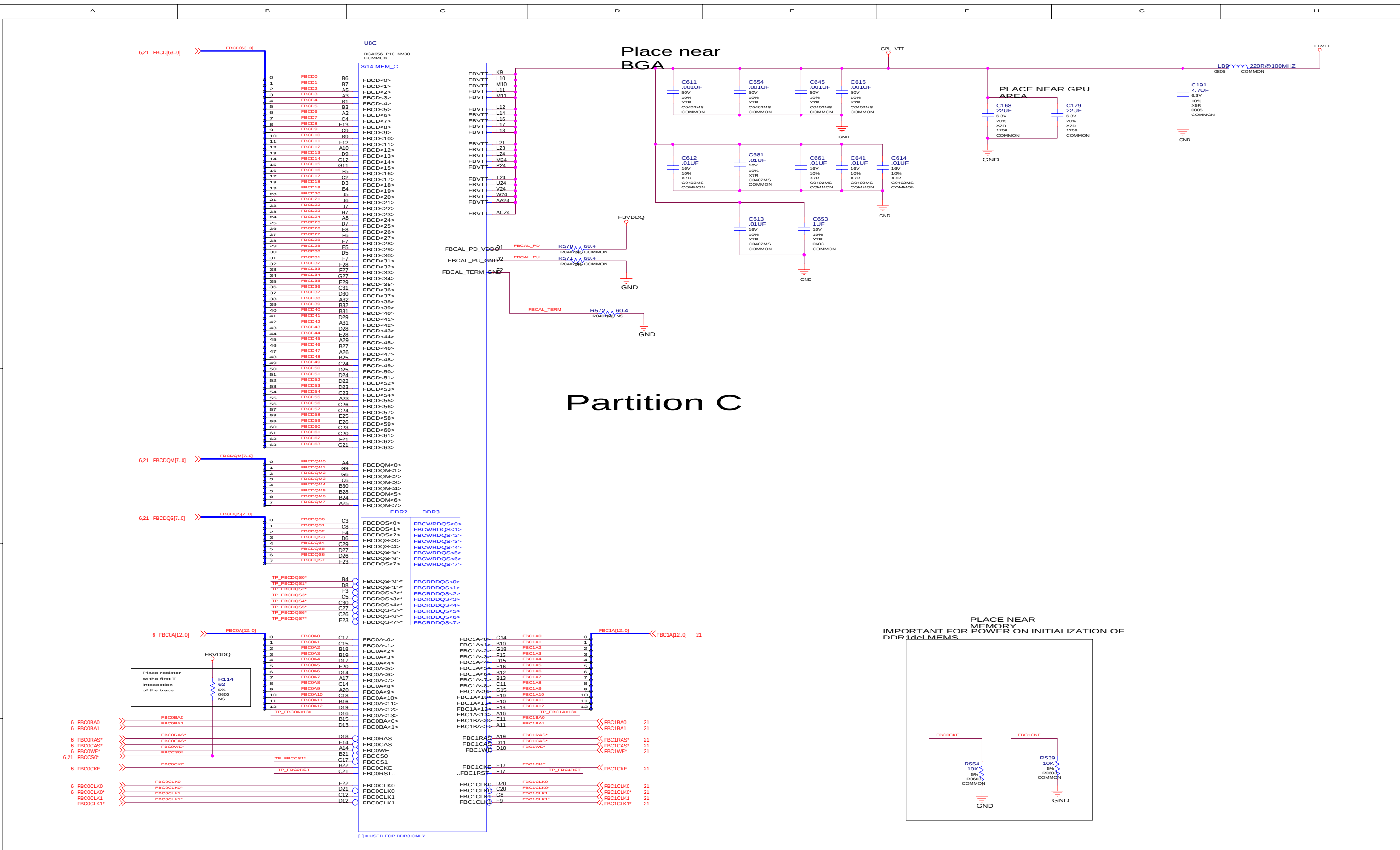
PAGE	<Add text to change page detail>
REVISION	



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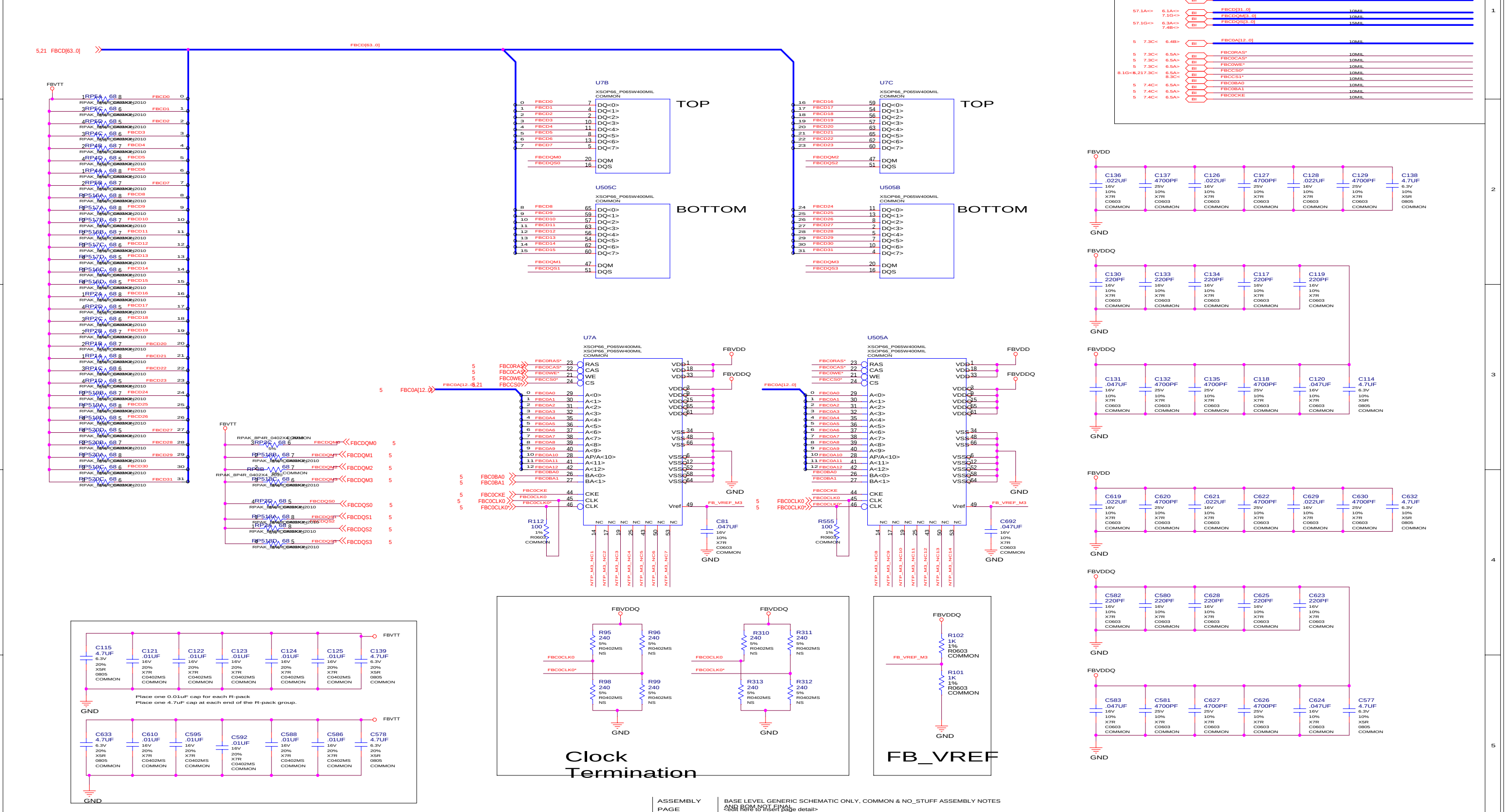
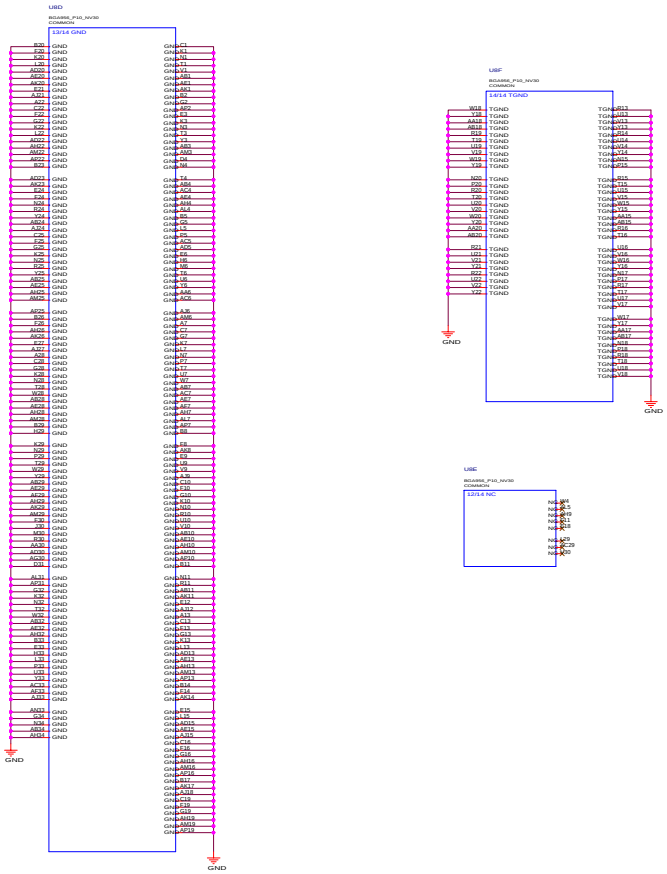
PAGE DETAIL | <edit here to insert page detail>

MEMORY 8(16)Mx16DDR Partition C , Bits 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!





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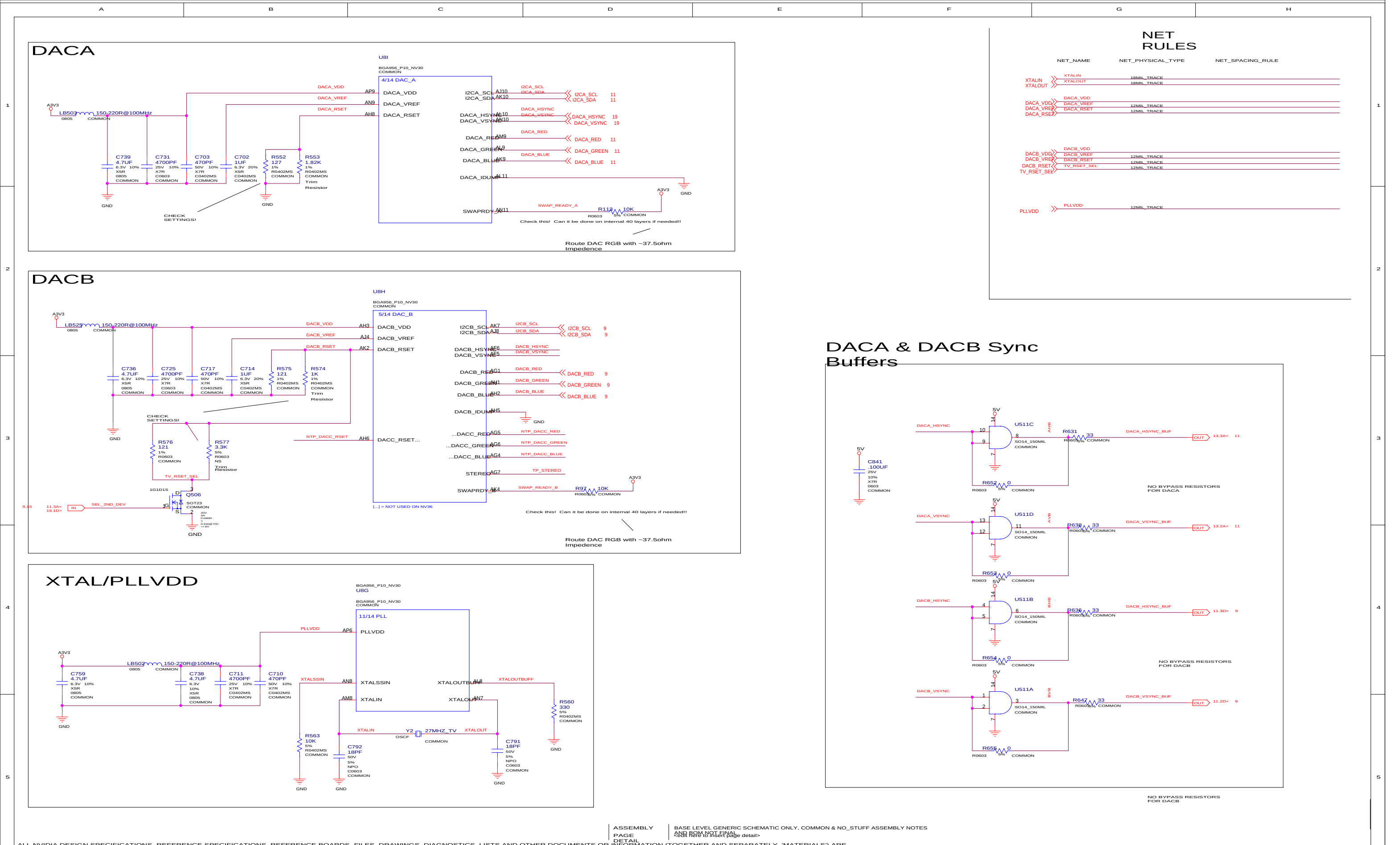
REVISION	<Revision Level>

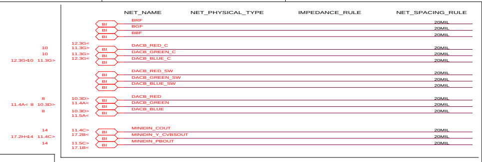


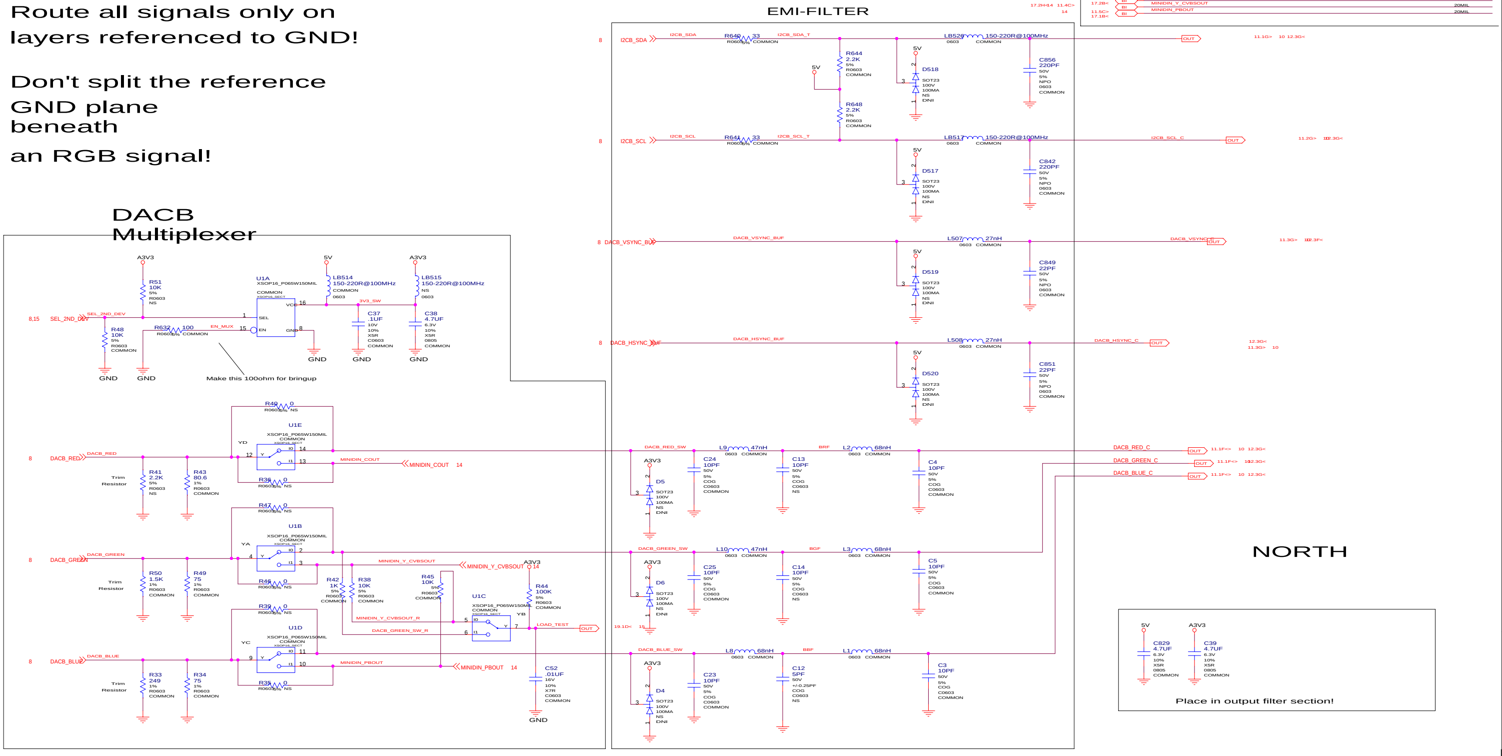
Secondary Display (DACB), Slim DB15

Place all filter components on the side nearest to the reference GND plane!

Route all signals only on layers referenced to GND!

Don't split the reference GND plane beneath an RGB signal!





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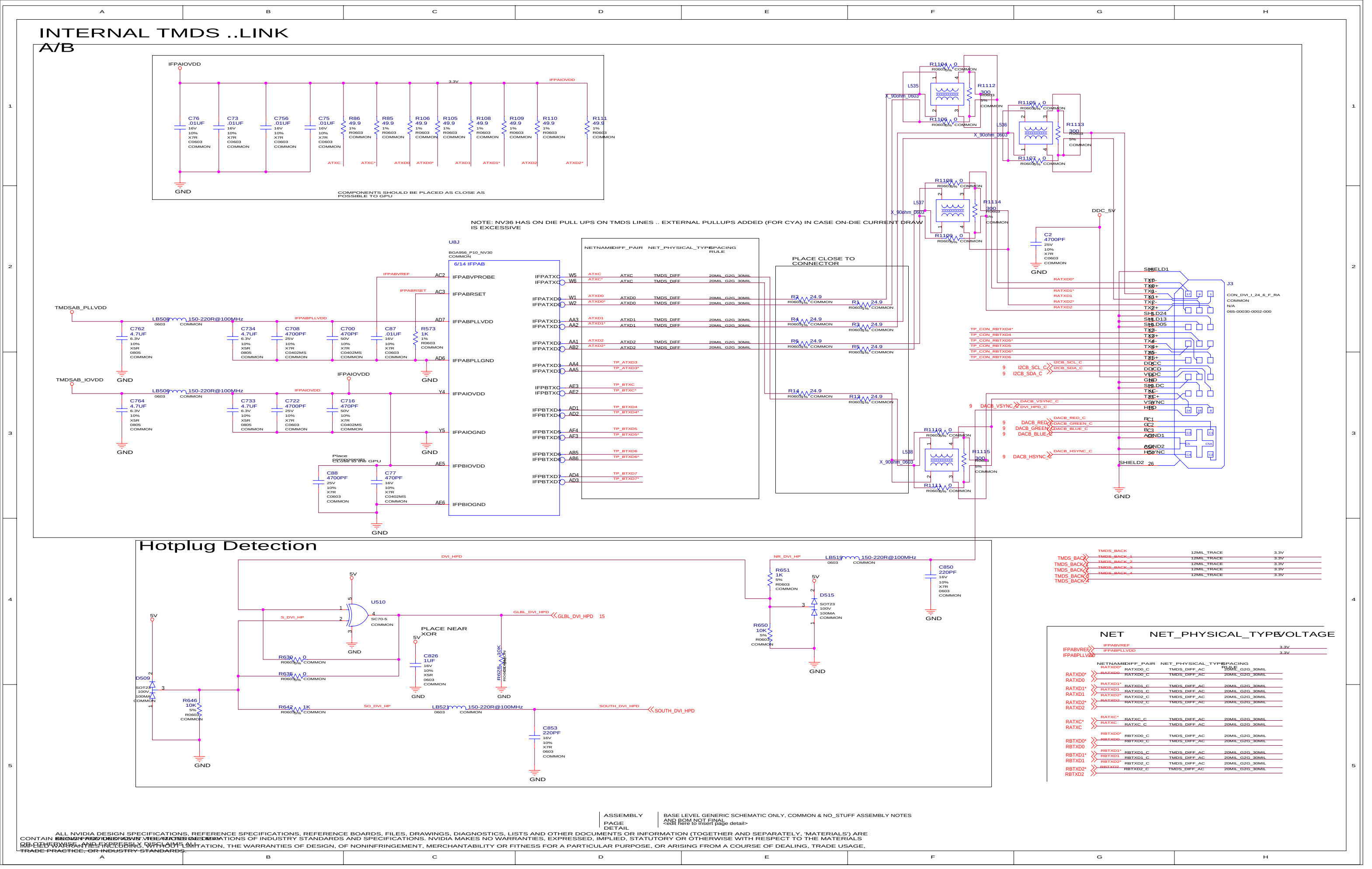
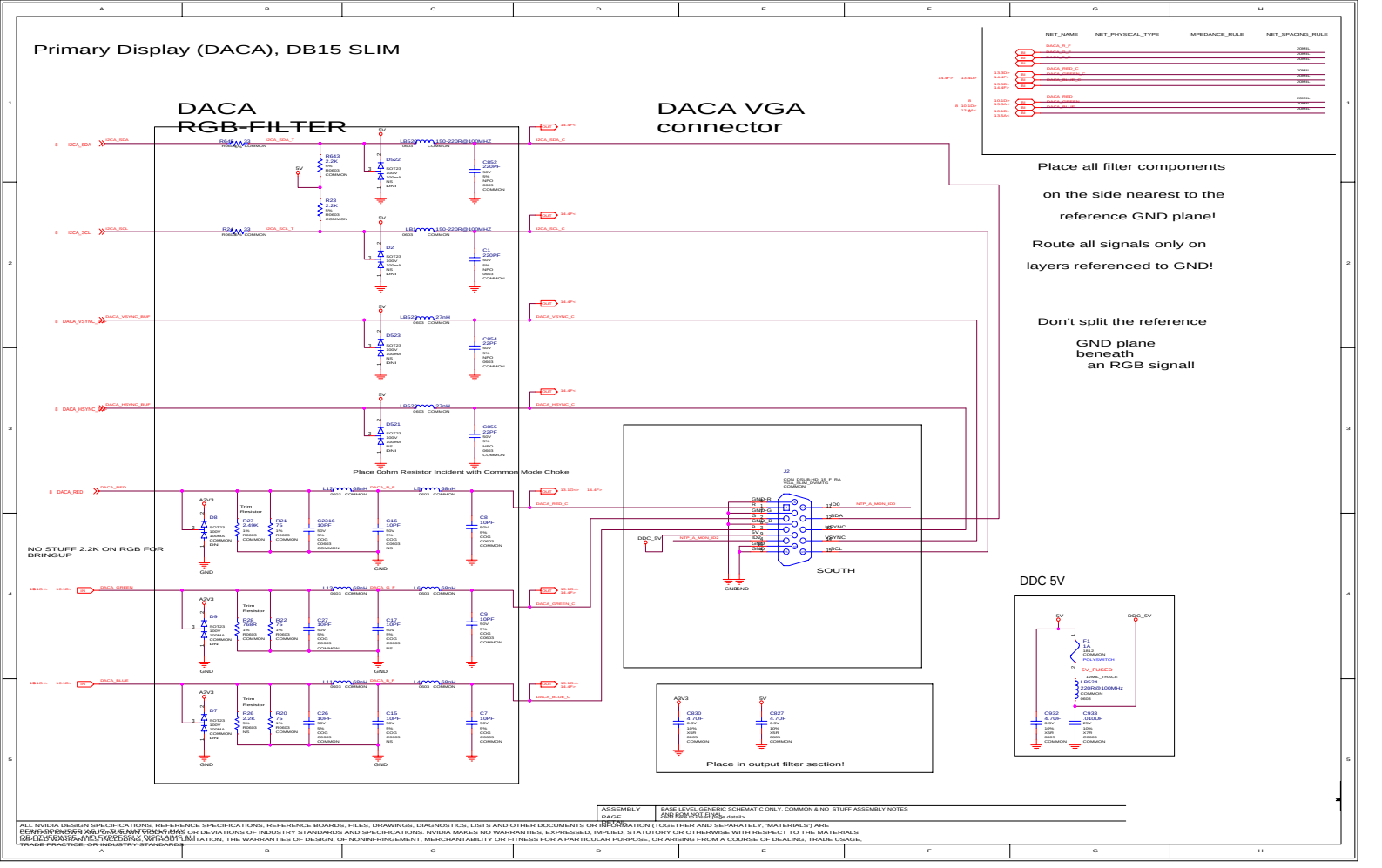


Primary Display (DACA), DB15 SLIM



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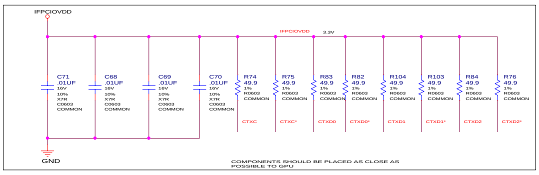
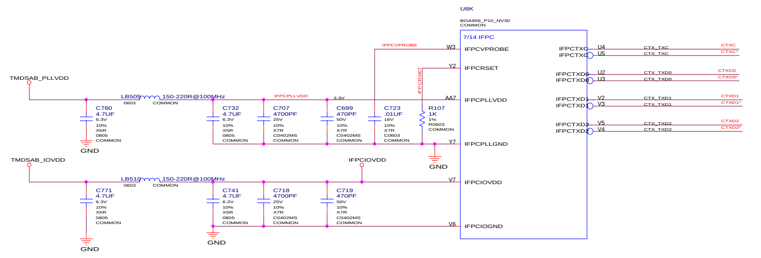


NET	NET_PHYSICAL_TYPE	VOLTAGE
DDC_5V	12MIL_TRACE	5V

NETNAME	DIFF_PAIR	NET_PHYSICAL_TYPE	SPACING RULE
RCTXD0*	RCTXD0_C	TMDS_DIFF_CC	20MIL_G2G_30MIL
RCTXD0	RCTXD0_C	TMDS_DIFF_CC	20MIL_G2G_30MIL
RCTXD1*	RCTXD1_C	TMDS_DIFF_CC	20MIL_G2G_30MIL
RCTXD1	RCTXD1_C	TMDS_DIFF_CC	20MIL_G2G_30MIL
RCTXD2*	RCTXD2_C	TMDS_DIFF_CC	20MIL_G2G_30MIL
RCTXD2	RCTXD2_C	TMDS_DIFF_CC	20MIL_G2G_30MIL
RCTXC*	RCTXC_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RCTXC	RCTXC_C	TMDS_DIFF_CC	20MIL_G2G_30MIL

INTERNAL TMDS LINK C



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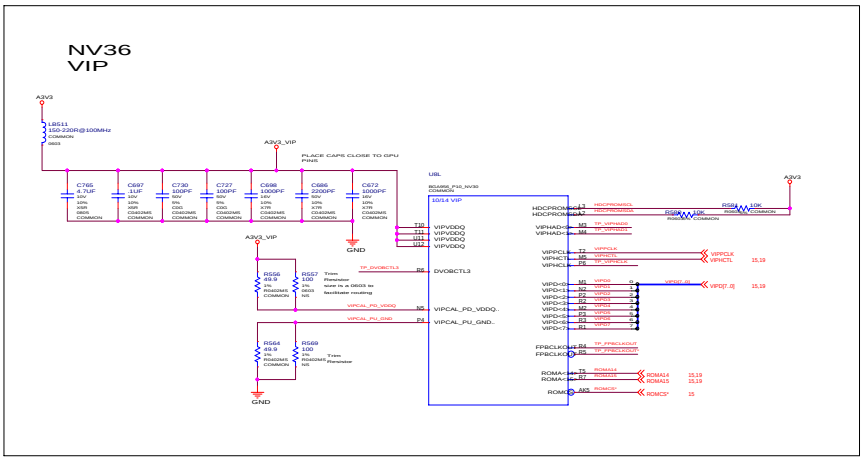

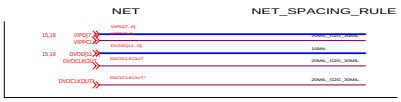

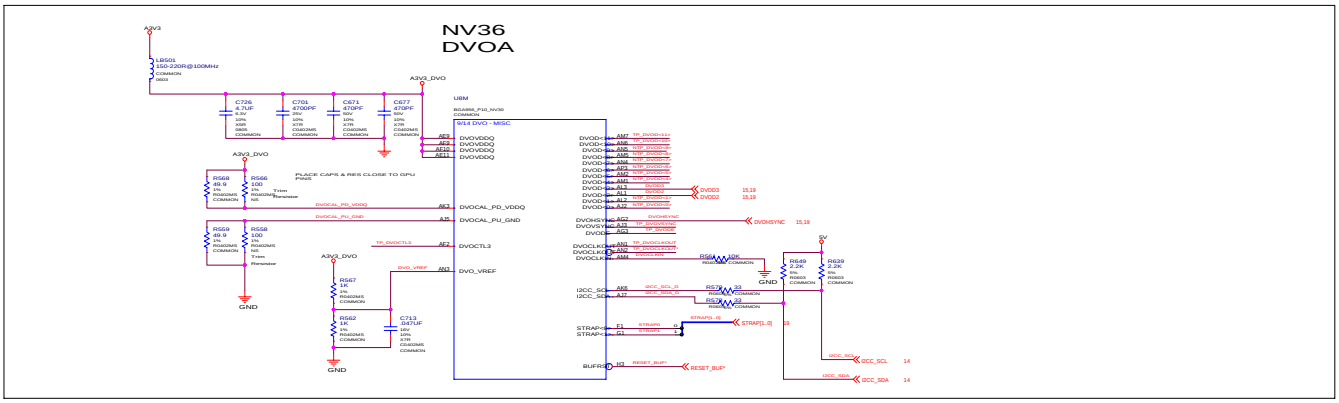

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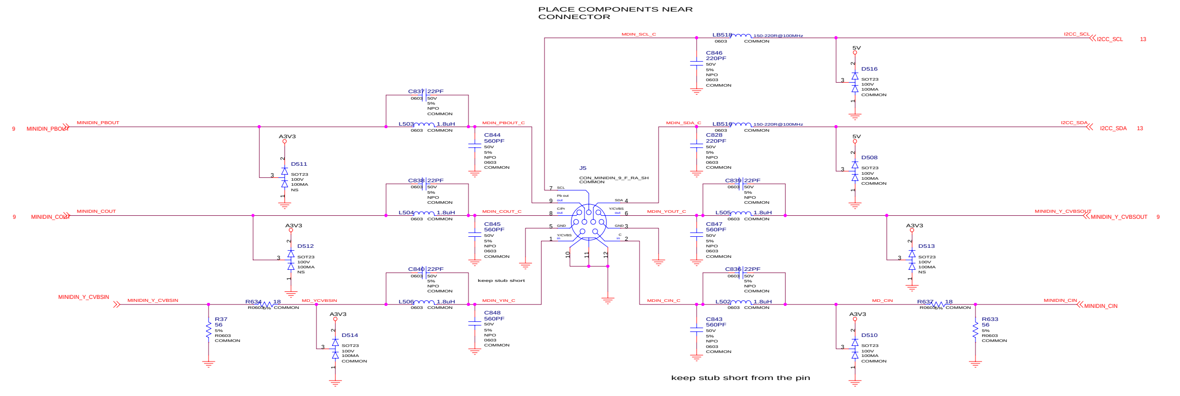
REVISION	<Revision Detail>

MiniDIN VIDEO IN/OUT CONNECTOR



NET_NAME	NET_PHYSICAL_TYPE	IMPEDANCE_RULE	NET_SPACING_RULE
MINIDIN_Y_CVBSIN			20MIL
MDIN_PBOUT_C			20MIL
MDIN_COUT_C			20MIL
MDIN_YIN_C			20MIL
MDIN_YOUT_C			20MIL
MDIN_CIN_C			20MIL
MINIDIN_CIN			20MIL
MD_PBOUT			20MIL
MD_COUT			20MIL
MD_YCVBSIN			20MIL
MD_CIN			20MIL
MD_YOUT			20MIL
7104_BLUE_CVBS			20MIL
7104_RED_COUT			20MIL
7104_GREEN_YOUT			20MIL

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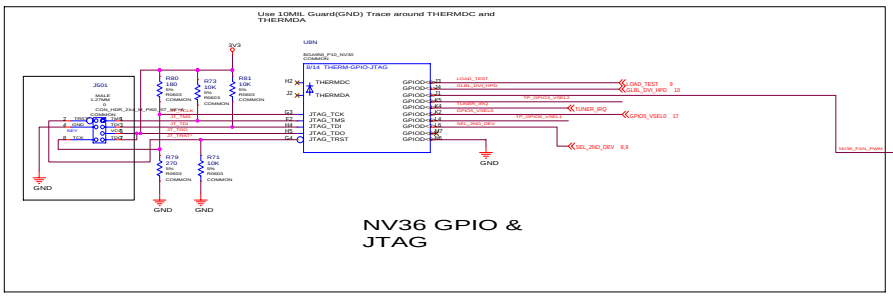
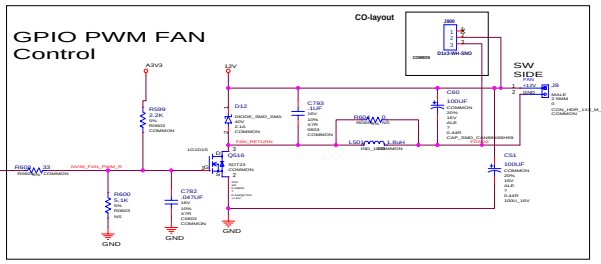
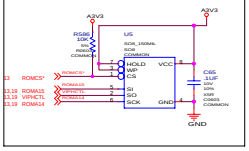
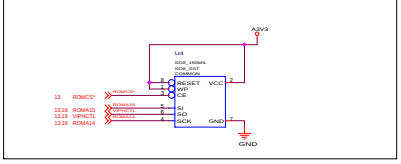




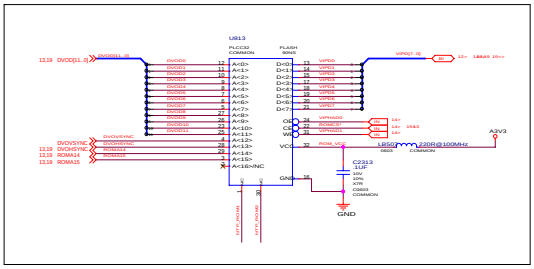
BIOS (serial)

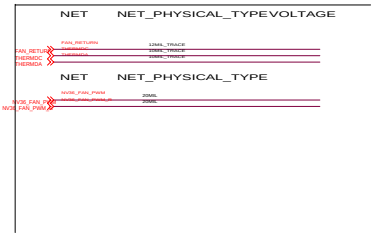


BIOS (serial alternative)



BIOS (parallel alternative)





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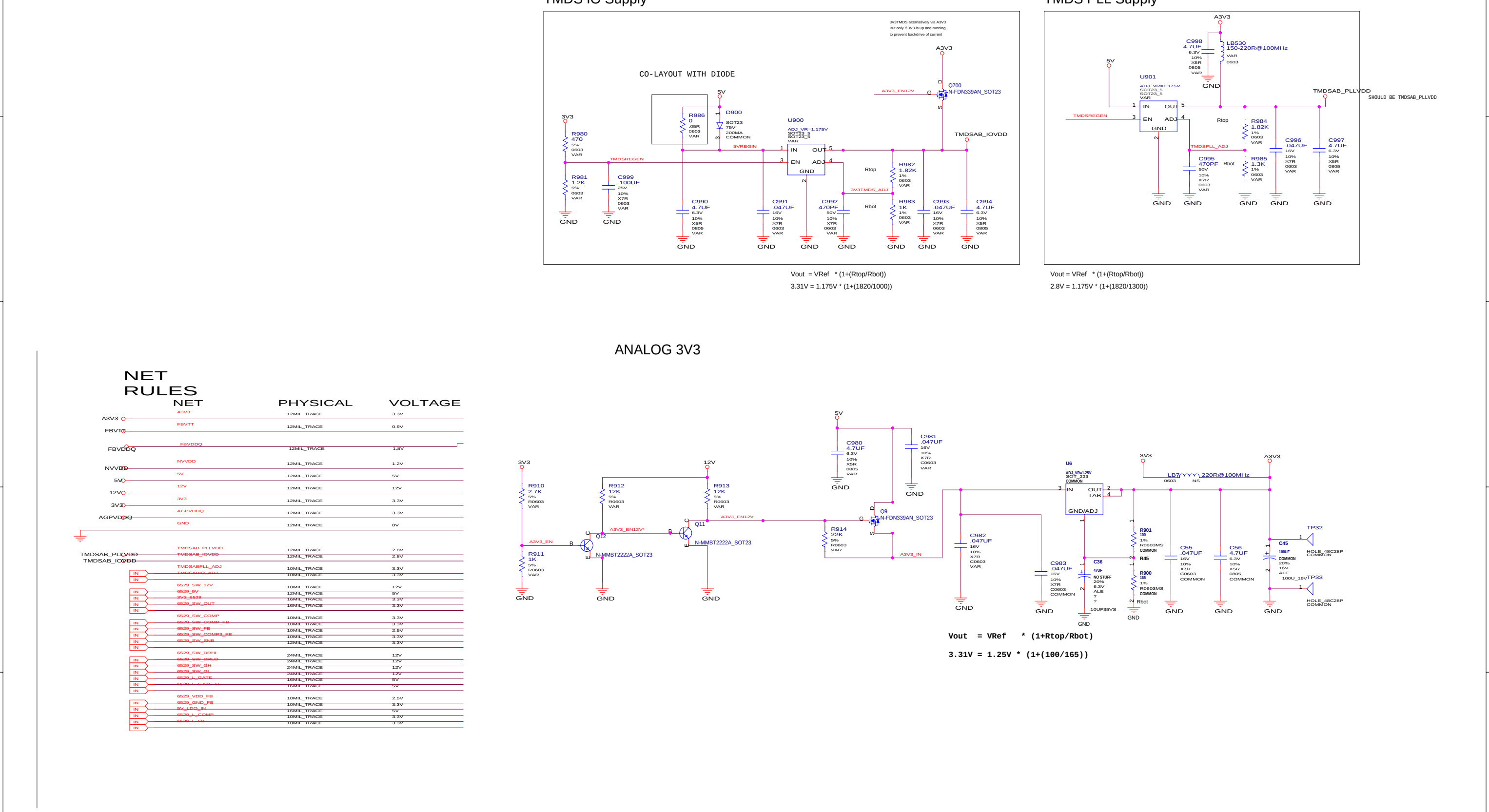
REVISION	ADD BOM OUTPUT FILES

Power Supply ... TMDS/A3V3



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PAGE DETAIL
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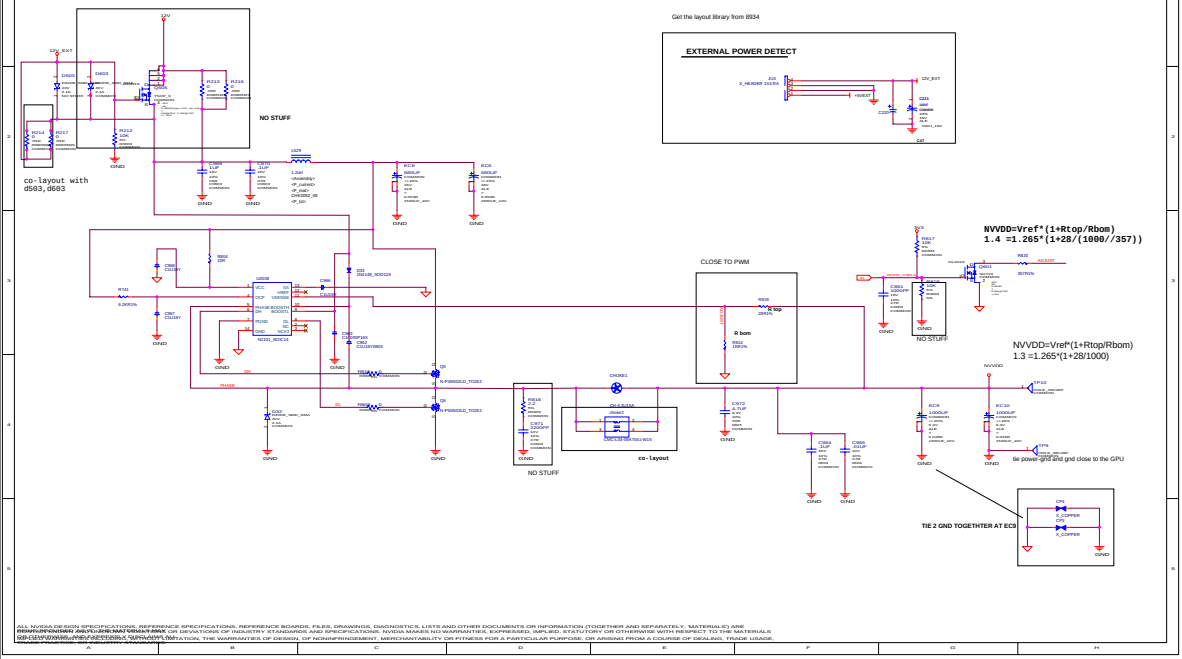
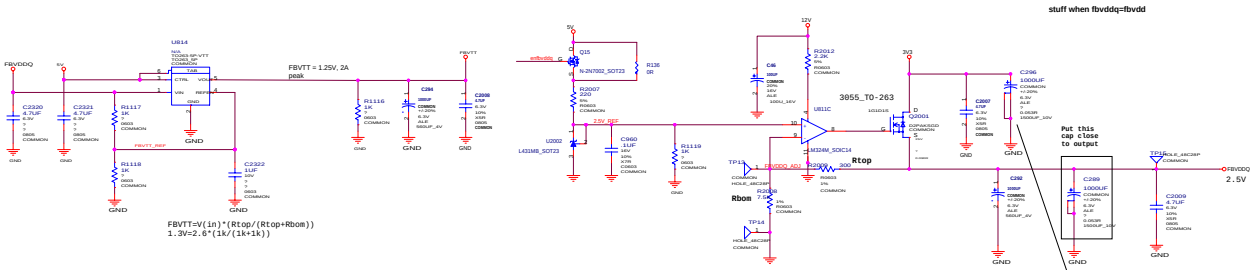
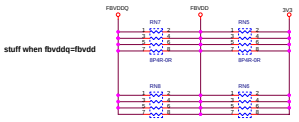


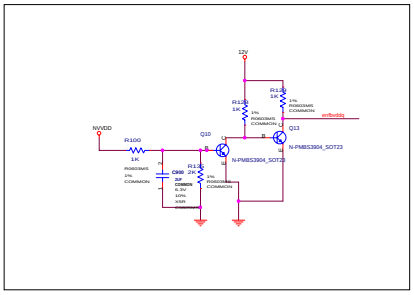
FBVDDQ



stuff when fbvddq=fbvdd



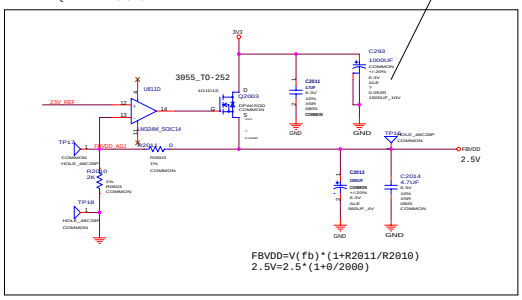
power sequence control



Put the two caps close,and the two mos drain close

FBVDD

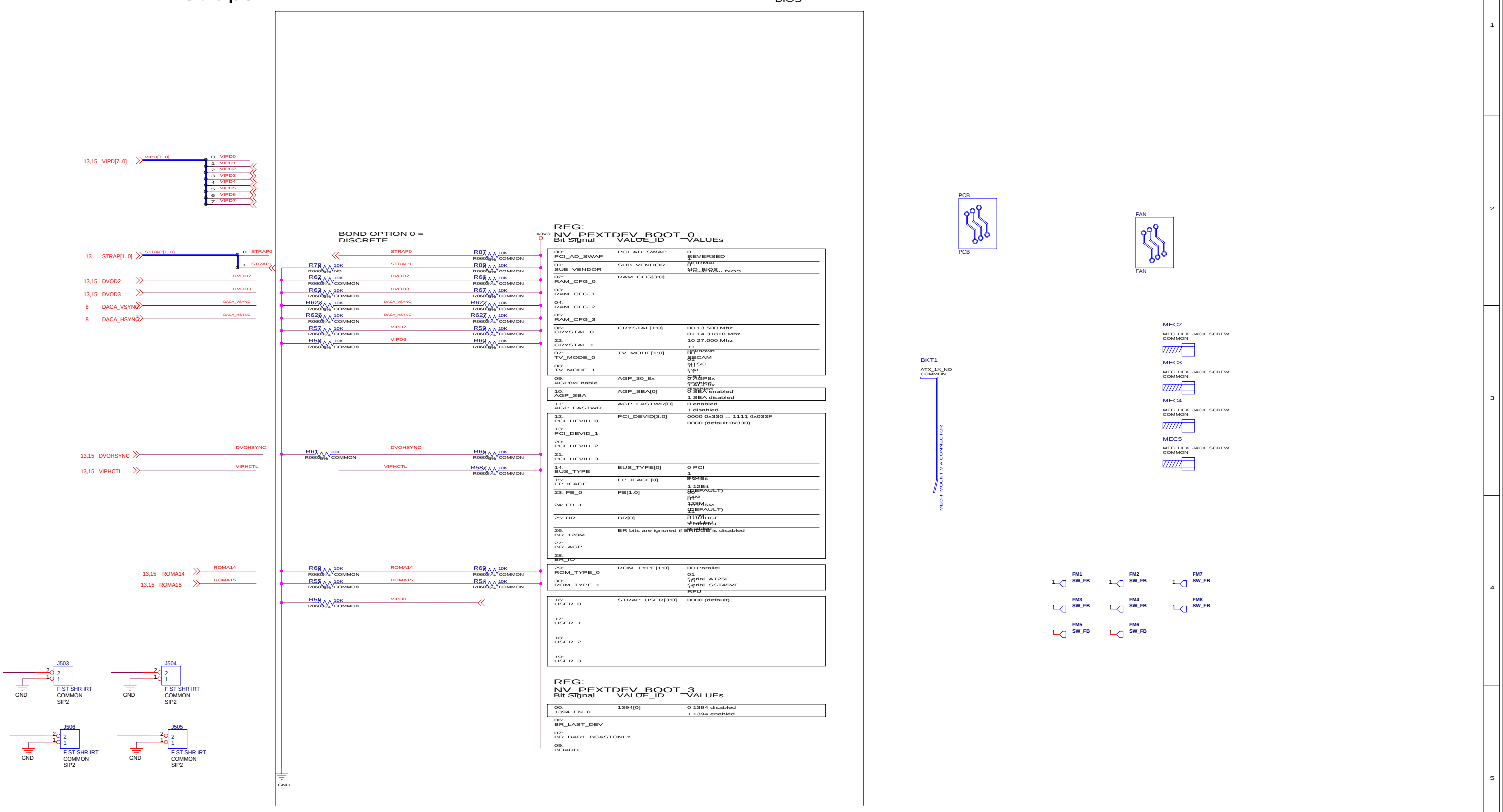
IF FBVDDQ=FBVDD NO STUFF



BIOS, Straps, Misc

Straps

Assembly:
BIOS



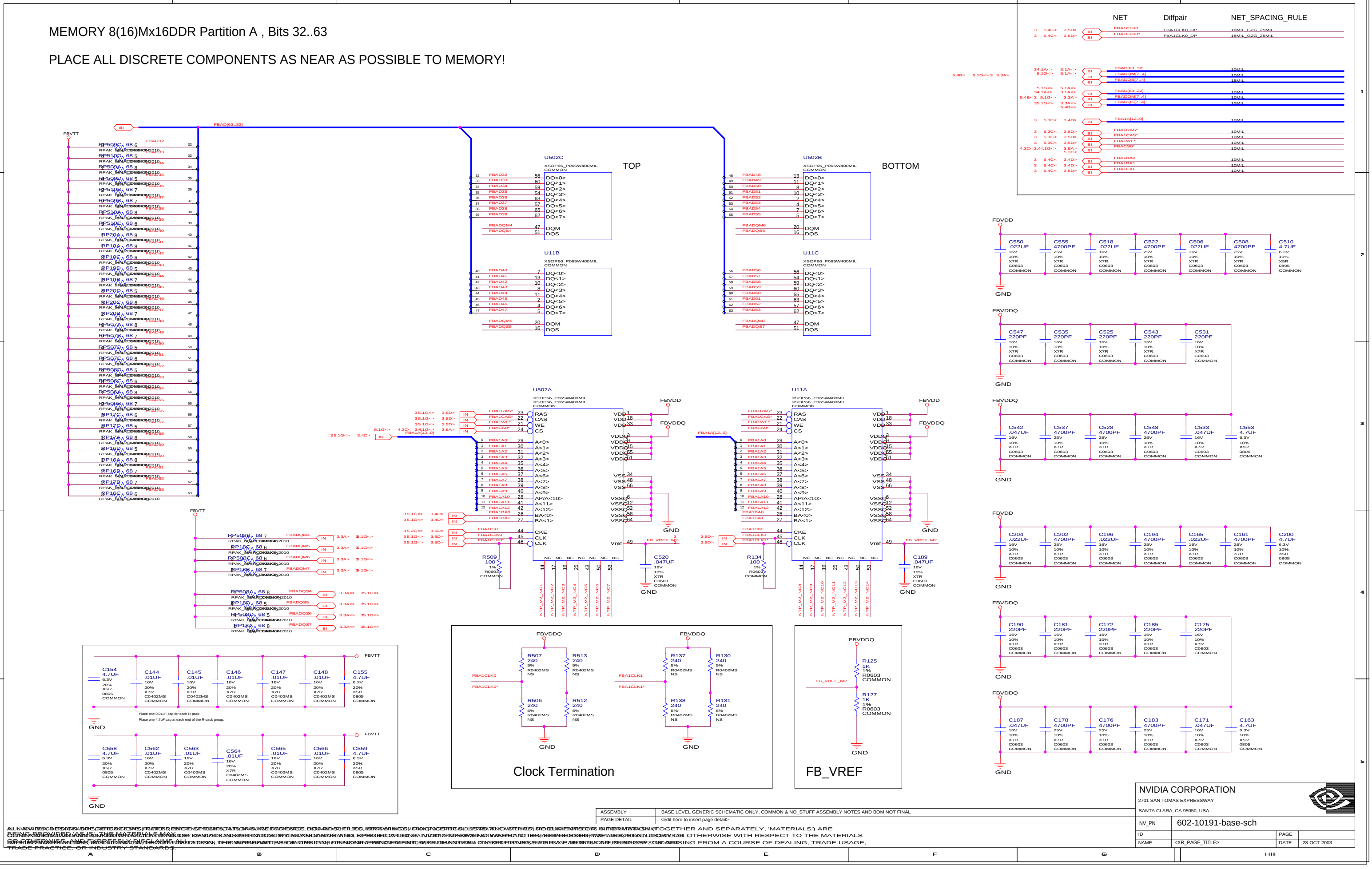
REG:
NV_PEXTDEV_BOOT_0

Bit Signal	VALUE_ID	VALUEs
00: PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED 1 NORMAL
01: SUB_VENDOR	SUB_VENDOR	0 NO_BIOS 1 read from BIOS
02: RAM_CFG_0 03: RAM_CFG_1 04: RAM_CFG_2 05: RAM_CFG_3	RAM_CFG[3:0]	
06: CRYSTAL_0 22: CRYSTAL_1	CRYSTAL[1:0]	00 13.500 Mhz 01 14.31818 Mhz 10 27.000 Mhz 11 unknown
07: TV_MODE_0 08: TV_MODE_1	TV_MODE[1:0]	00 SECAM 01 NTSC 10 PAL 11 CRT
09: AGP8xEnable	AGP_30_8x	0 AGP8x enabled 1 AGP8x disabled
10: AGP_SBA	AGP_SBA[0]	0 SBA enabled 1 SBA disabled
11: AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled
12: PCI_DEVID_0 13: PCI_DEVID_1 20: PCI_DEVID_2 21: PCI_DEVID_3	PCI_DEVID[3:0]	0000 0x330 ... 1111 0x033F 0000 (default 0x330)
14: BUS_TYPE	BUS_TYPE[0]	0 PCI 1 AGP
15: FP_IFACE	FP_IFACE[0]	0 24Bit 1 12Bit (DEFAULT)
23: FB_0 24: FB_1	FB[1:0]	00 64M 01 128M 10 256M (DEFAULT) 11 512M
25: BR	BR[0]	0 BRIDGE disabled 1 BRIDGE enabled
26: BR_128M 27: BR_AGP 28: BR_IO	BR bits are ignored if BRIDGE is disabled	
29: ROM_TYPE_0 30: ROM_TYPE_1	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F 10 Serial_SST45VF 11 RFU
16: USER_0 17: USER_1 18: USER_2 19: USER_3	STRAP_USER[3:0]	0000 (default)

REG:
NV_PEXTDEV_BOOT_3

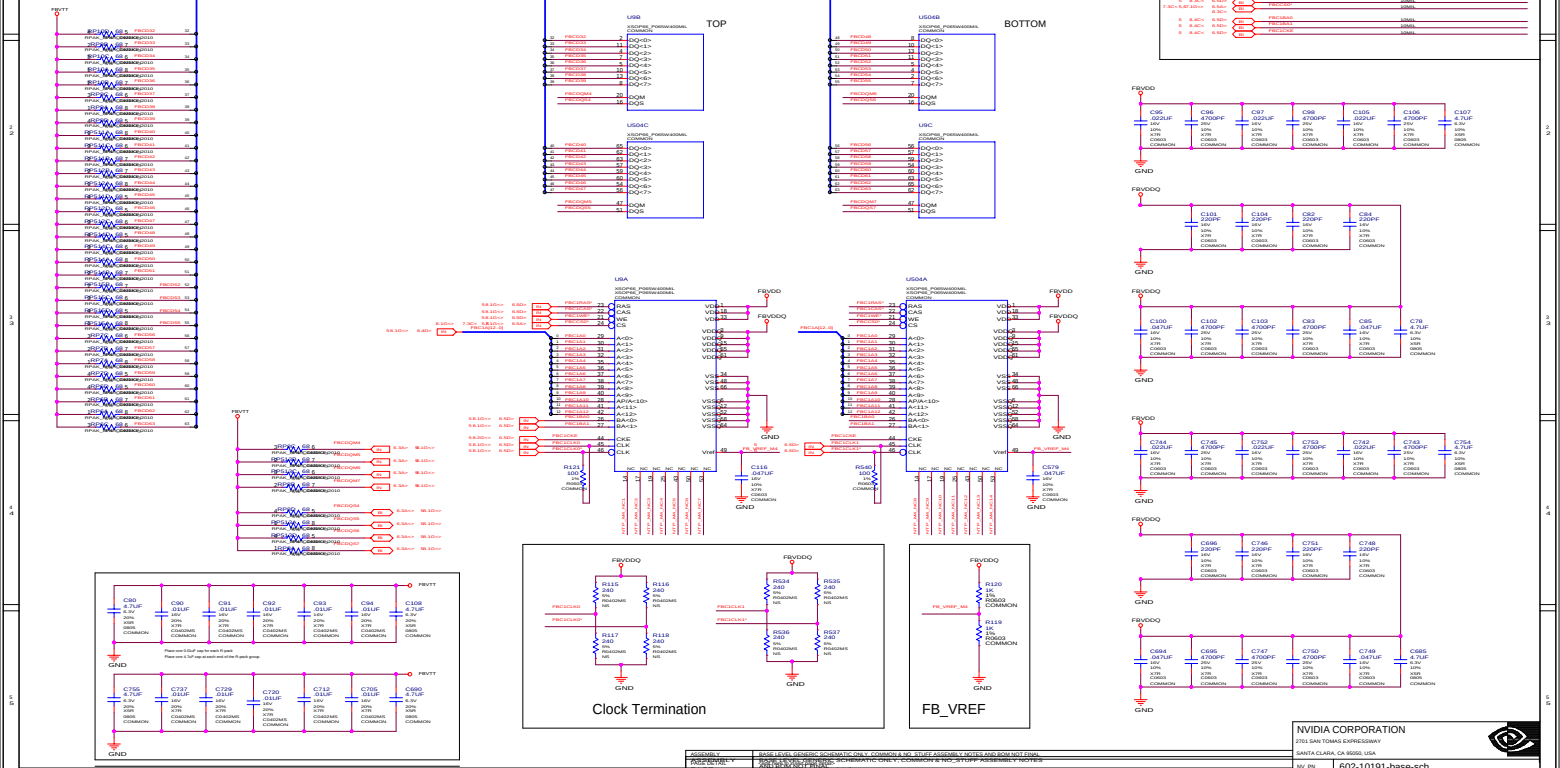
Bit Signal	VALUE_ID	VALUEs
00: 1394_EN_0	1394[0]	0 1394 disabled 1 1394 enabled
06: BR_LAST_DEV		
07: BR_BAR1_BCASTONLY		
09: BOARD		

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	<edit here to insert page detail>



MEMORY 8(16)Mx16DDR Partition C , Bits 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



Clock Termination

FB_VREF

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	<PAGE_TITLE>
PAGE	<PAGE_TITLE>

NVIDIA CORPORATION	
2701 SAN TOMAS EXPRESSWAY	
SANTA CLARA, CA 95050, USA	
NV_PN	602-10191-base-sch
ID	PAGE
NAME <XR_PAGE_TITLE>	DATE 28-OCT-2003