PCI-EXPRESS EDGE CONNECTOR

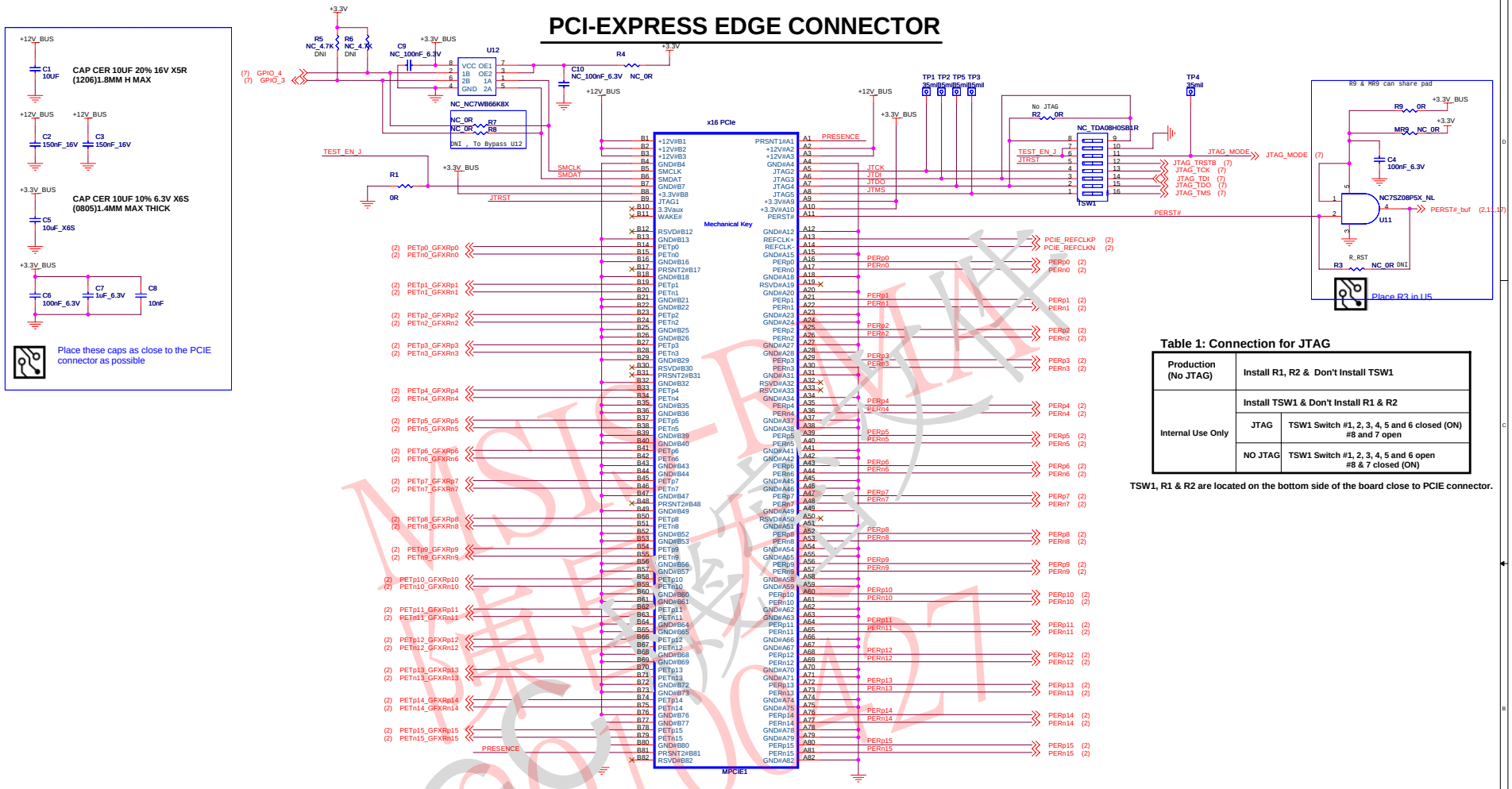

Table 1: Connection for JTAG

Production (No JTAG)	Install R1, R2 & Don't Install TSW1	
Internal Use Only	Install TSW1 & Don't Install R1 & R2	
	JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open
	NO JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

HD4870XG5-v10

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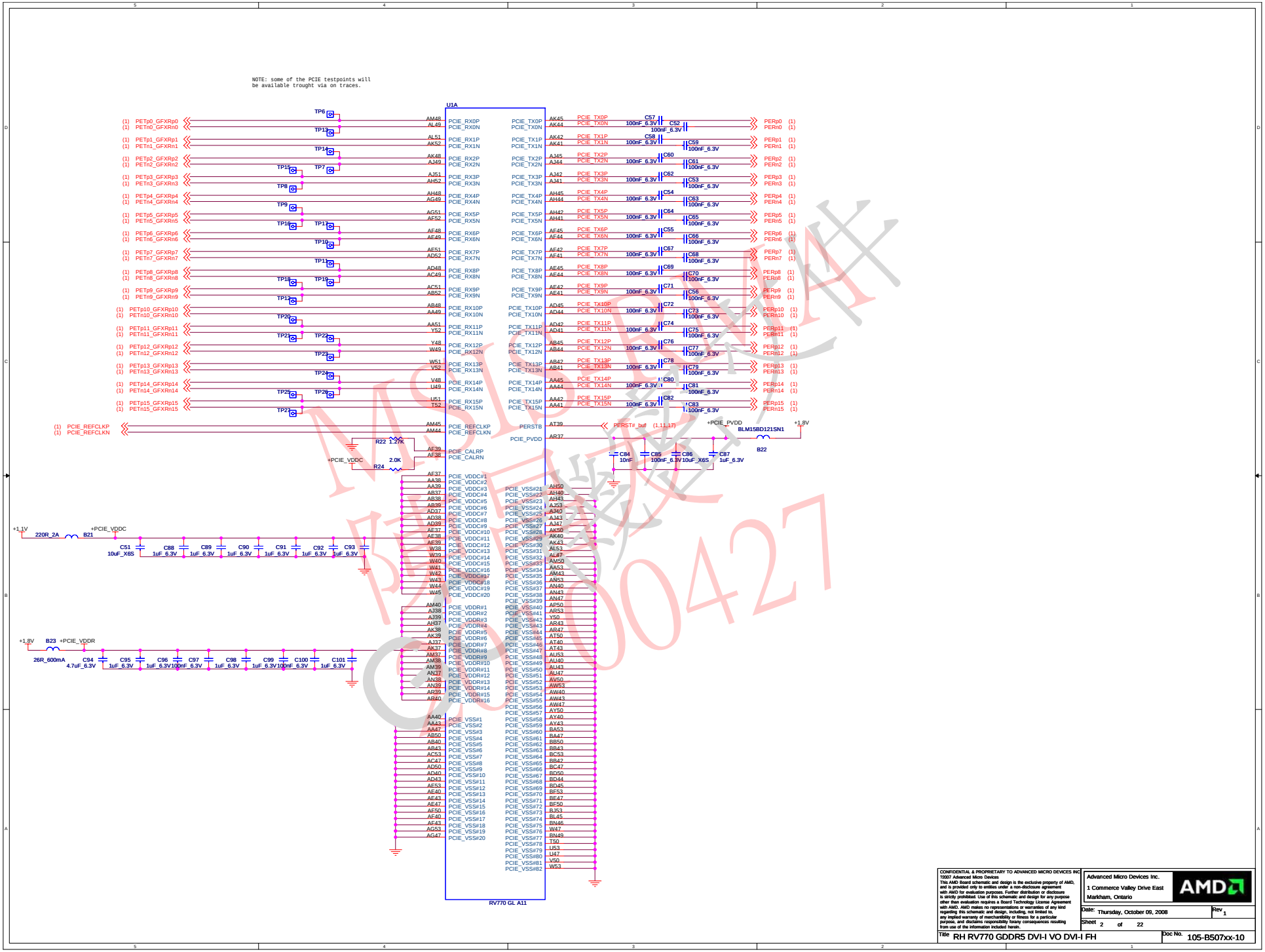

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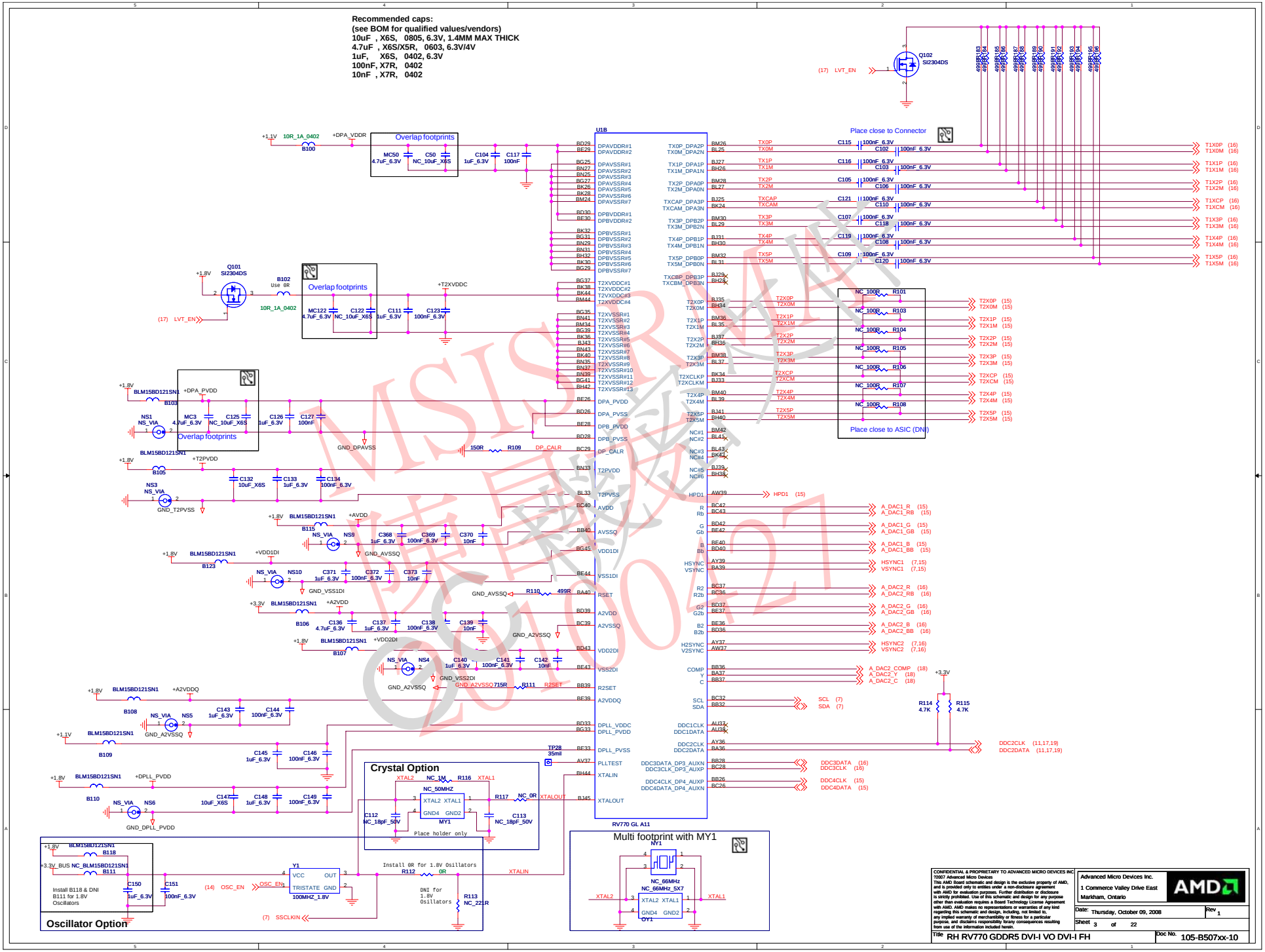

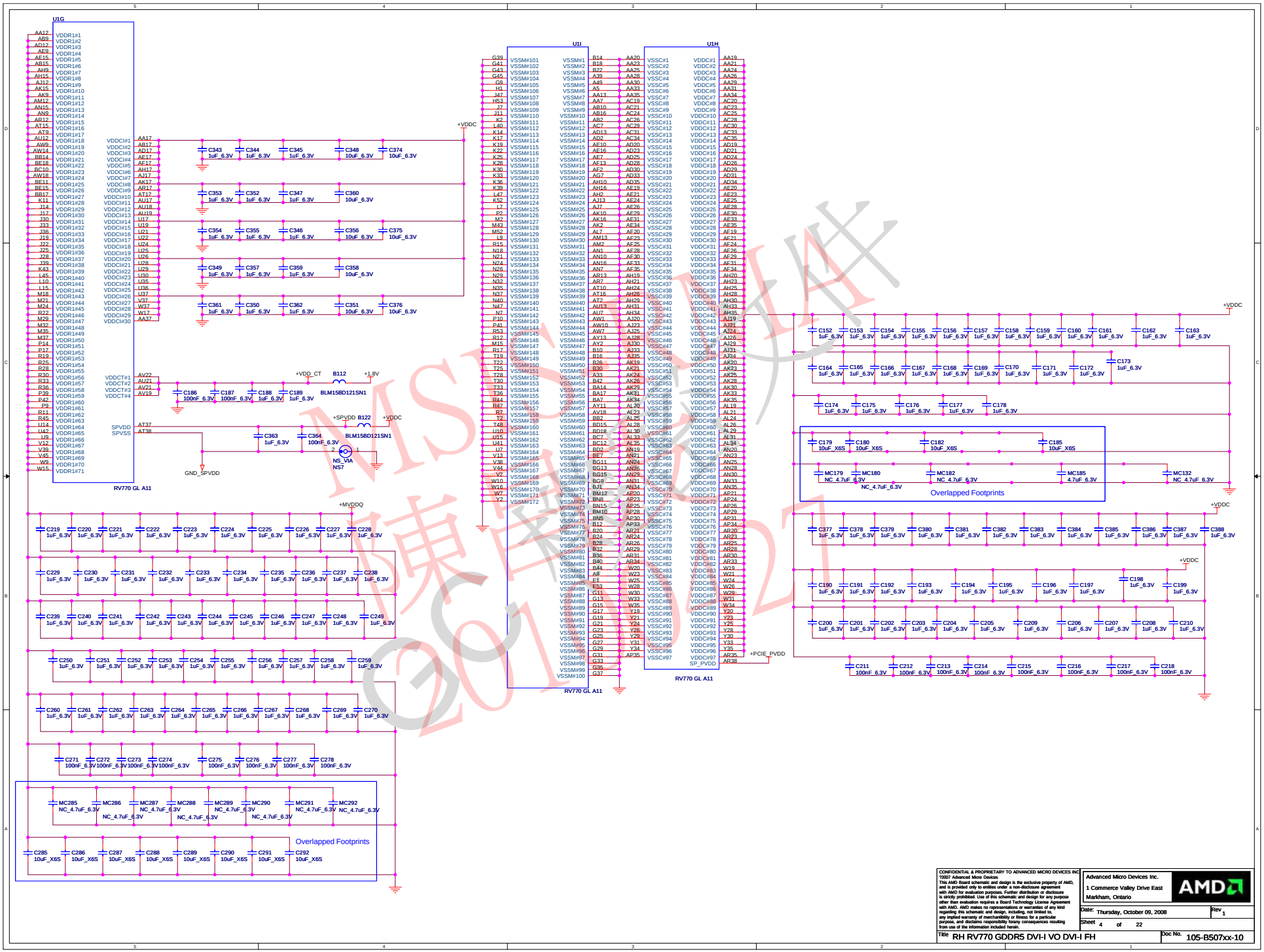

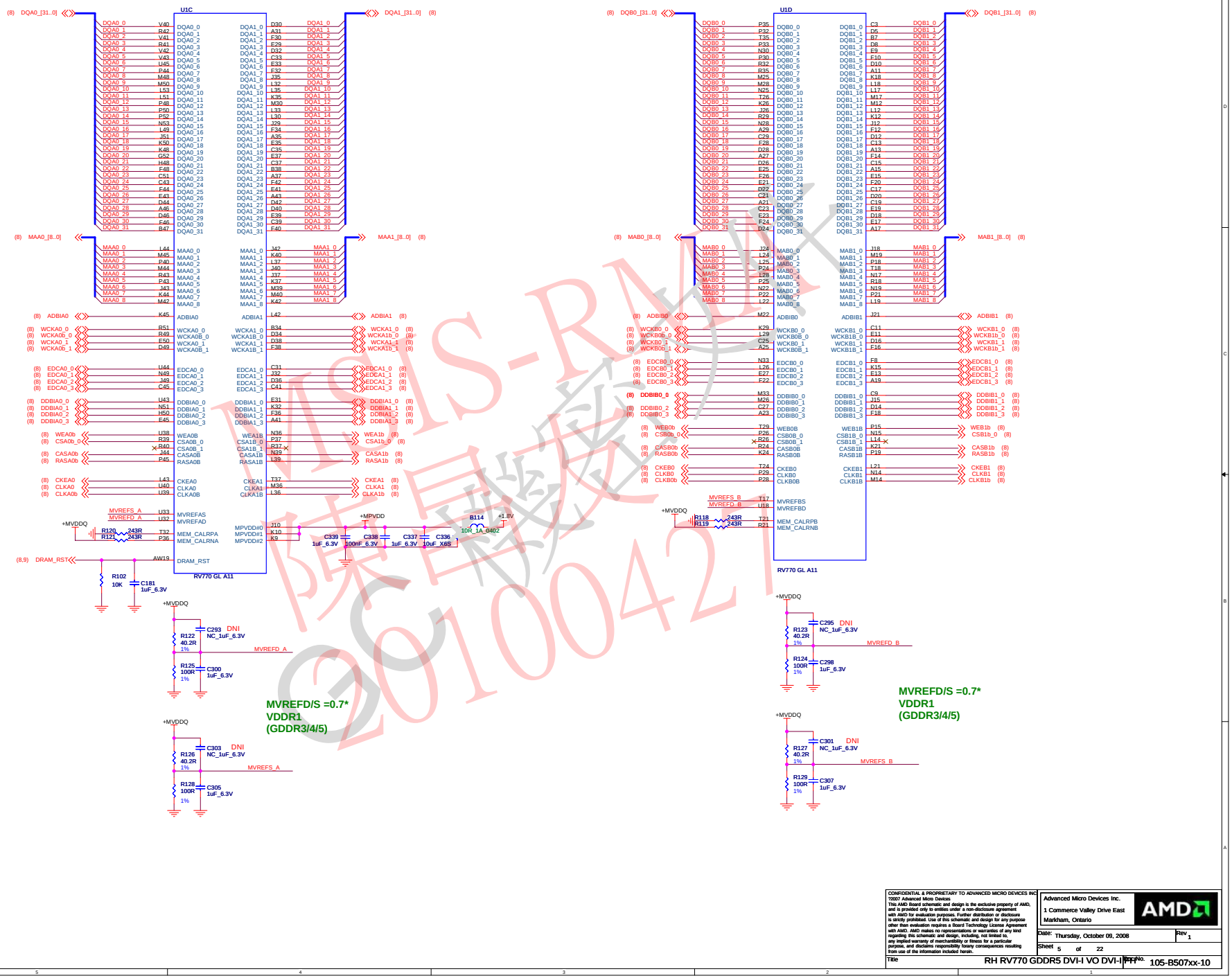

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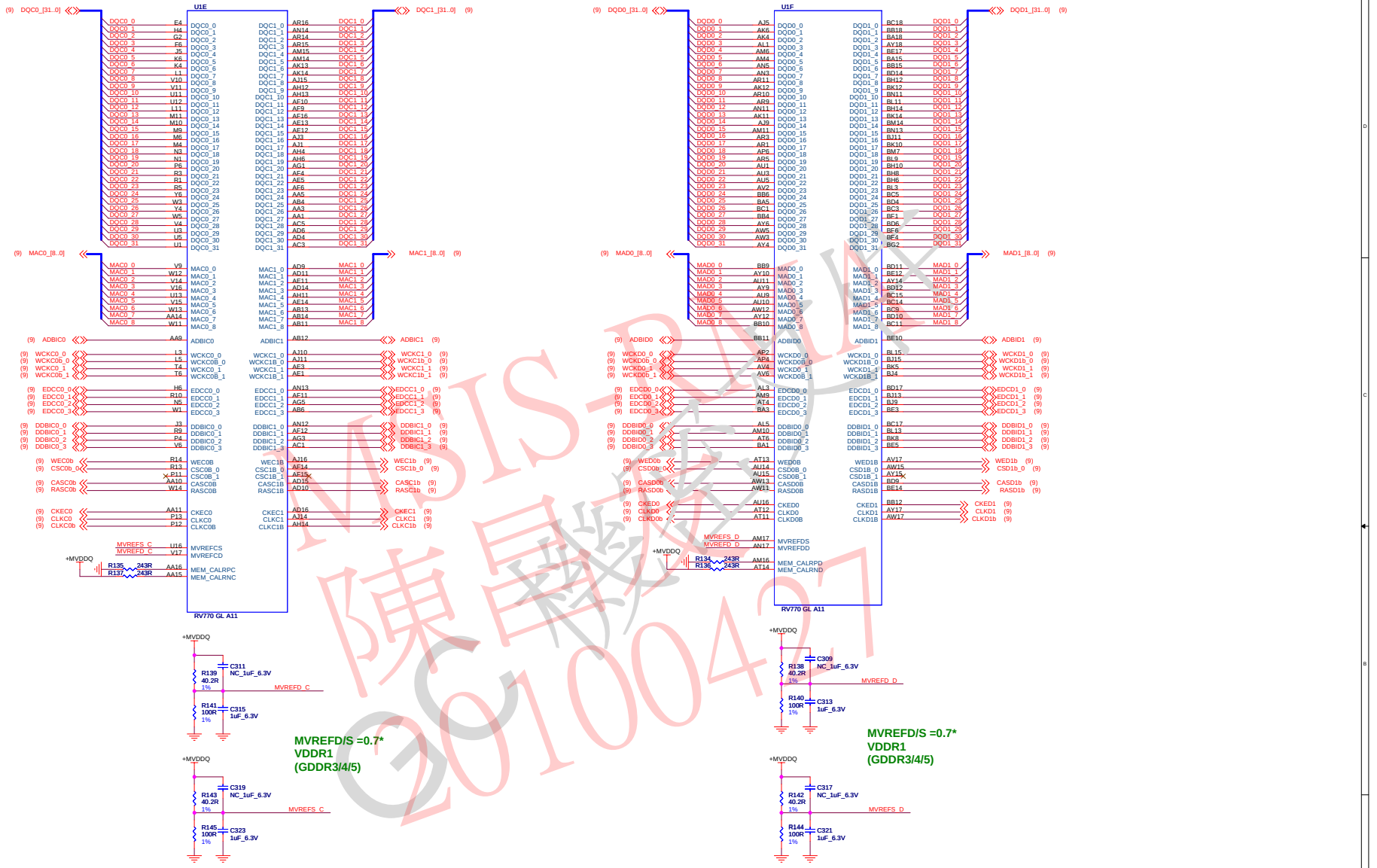

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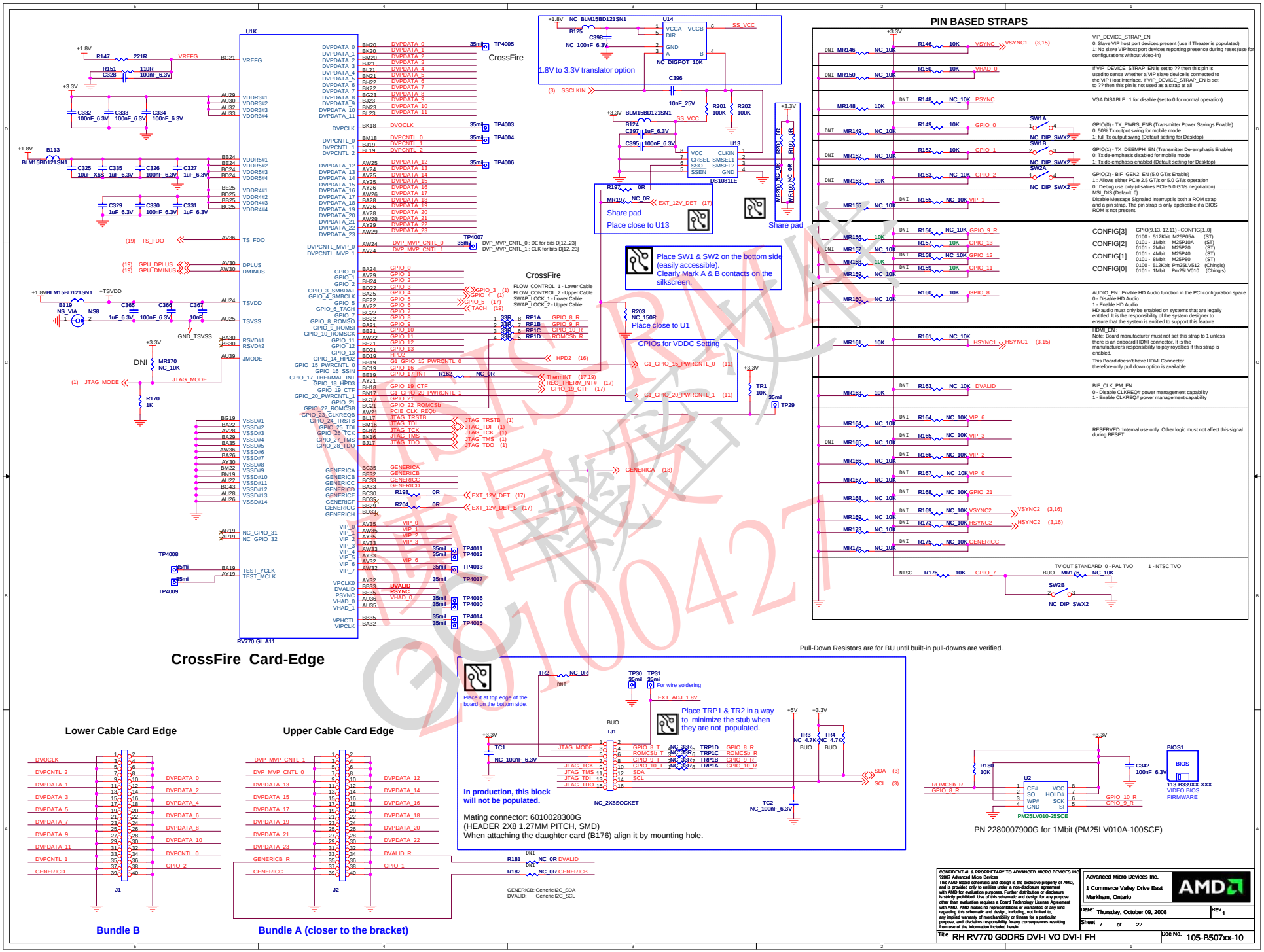

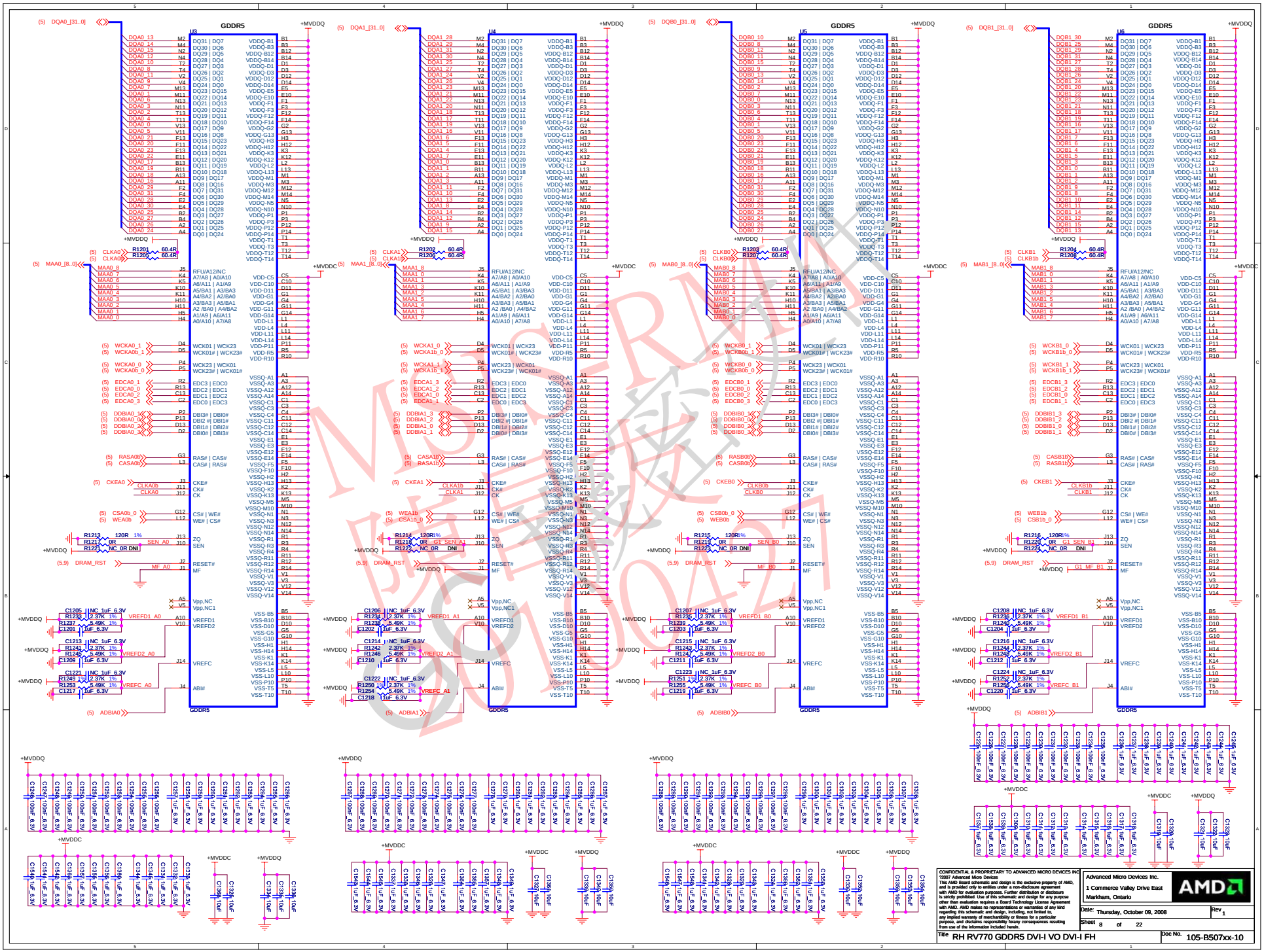

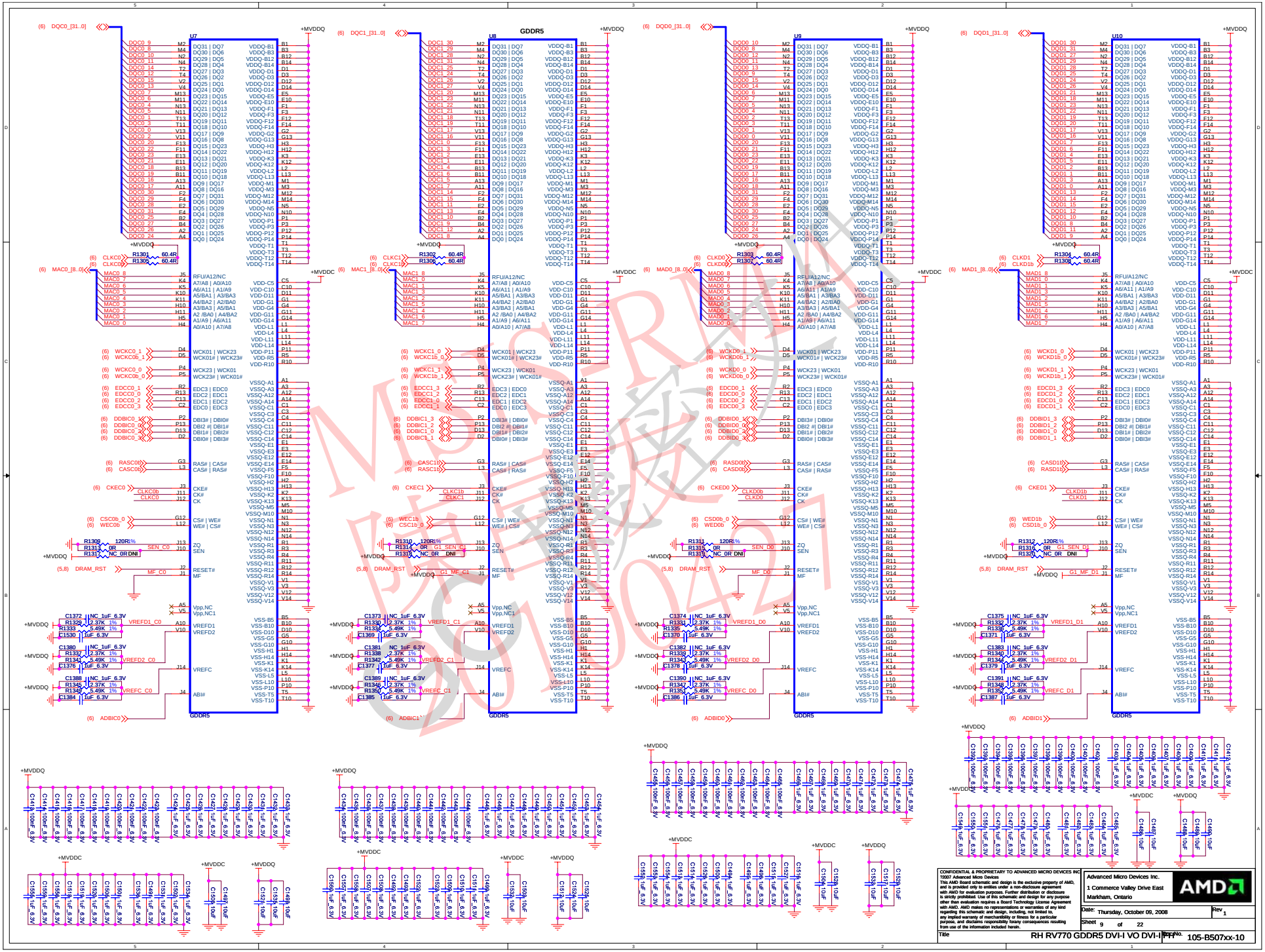

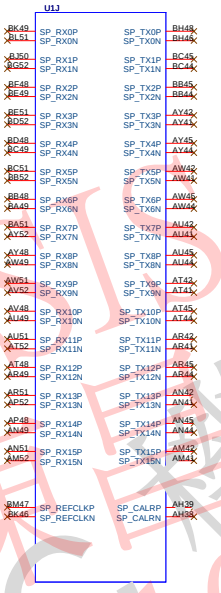

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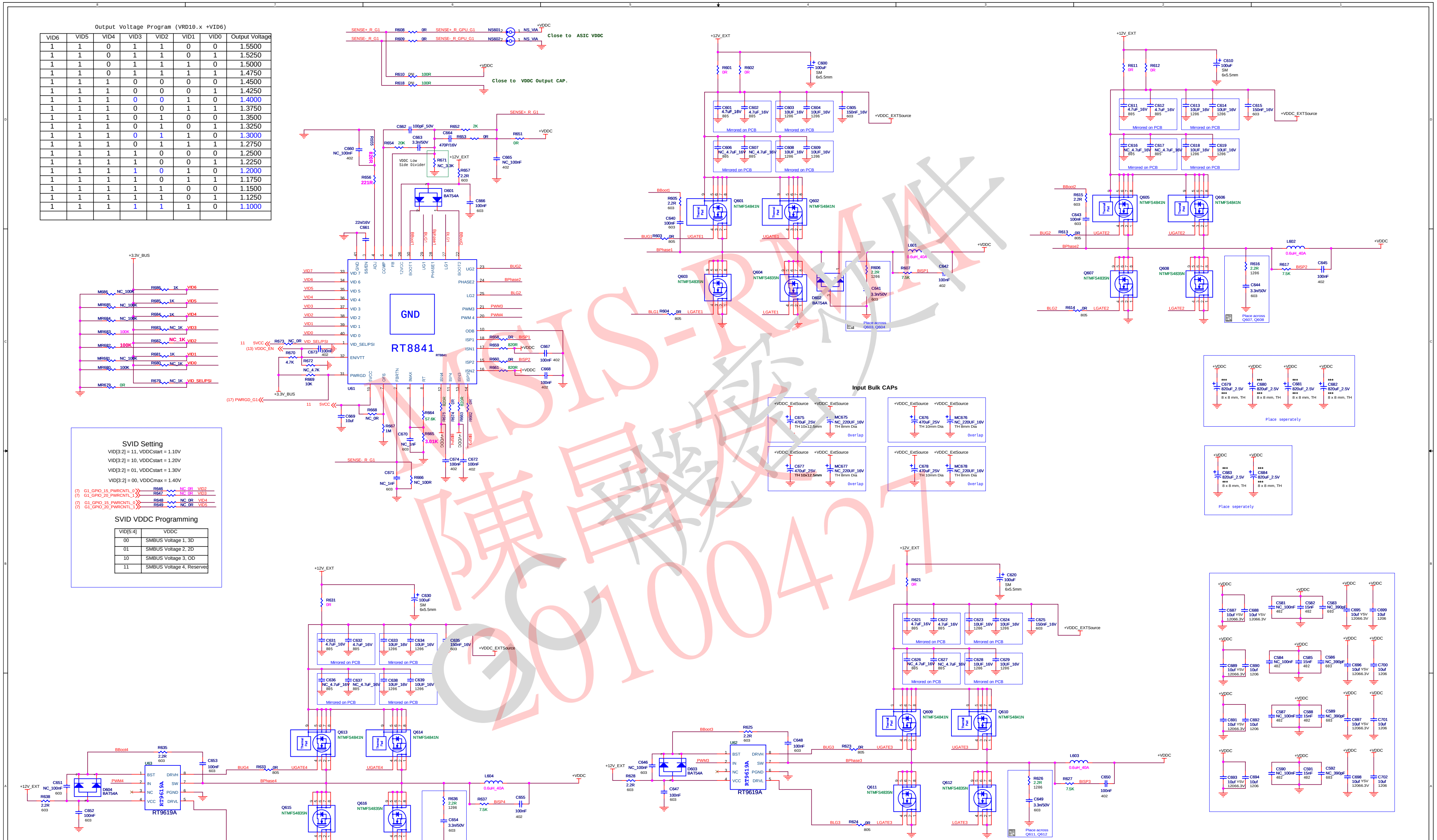

Output Voltage Program (VRD10.x +VID6)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output Voltage
1	1	0	1	1	0	0	1.5500
1	1	0	1	1	0	1	1.5250
1	1	0	1	1	1	0	1.5000
1	1	0	1	1	1	1	1.4750
1	1	1	0	0	0	0	1.4500
1	1	1	0	0	0	1	1.4250
1	1	1	0	0	1	0	1.4000
1	1	1	0	0	1	1	1.3750
1	1	1	0	1	0	0	1.3500
1	1	1	0	1	0	1	1.3250
1	1	1	0	1	1	0	1.3000
1	1	1	0	1	1	1	1.2750
1	1	1	1	0	0	0	1.2500
1	1	1	1	0	0	1	1.2250
1	1	1	1	0	1	0	1.2000
1	1	1	1	0	1	1	1.1750
1	1	1	1	1	0	0	1.1500
1	1	1	1	1	0	1	1.1250
1	1	1	1	1	1	0	1.1000

SVID Setting

VID[3:2] = 11, VDDCstart = 1.10V

VID[3:2] = 10, VDDCstart = 1.20V

VID[3:2] = 01, VDDCstart = 1.30V

VID[3:2] = 00, VDDCmax = 1.40V

(7) G1_GPIO_15_PWRCNTL_0 — R646 NC_0R VID2
(7) G1_GPIO_20_PWRCNTL_1 — R647 NC_0R VID3
(7) G1_GPIO_15_PWRCNTL_0 — R648 NC_0R VID4
(7) G1_GPIO_20_PWRCNTL_1 — R649 NC_0R VID5

SVID VDDC Programming

VID[5:4]	VDDC
00	SMBUS Voltage 1, 3D
01	SMBUS Voltage 2, 2D
10	SMBUS Voltage 3, OD
11	SMBUS Voltage 4, Reserved

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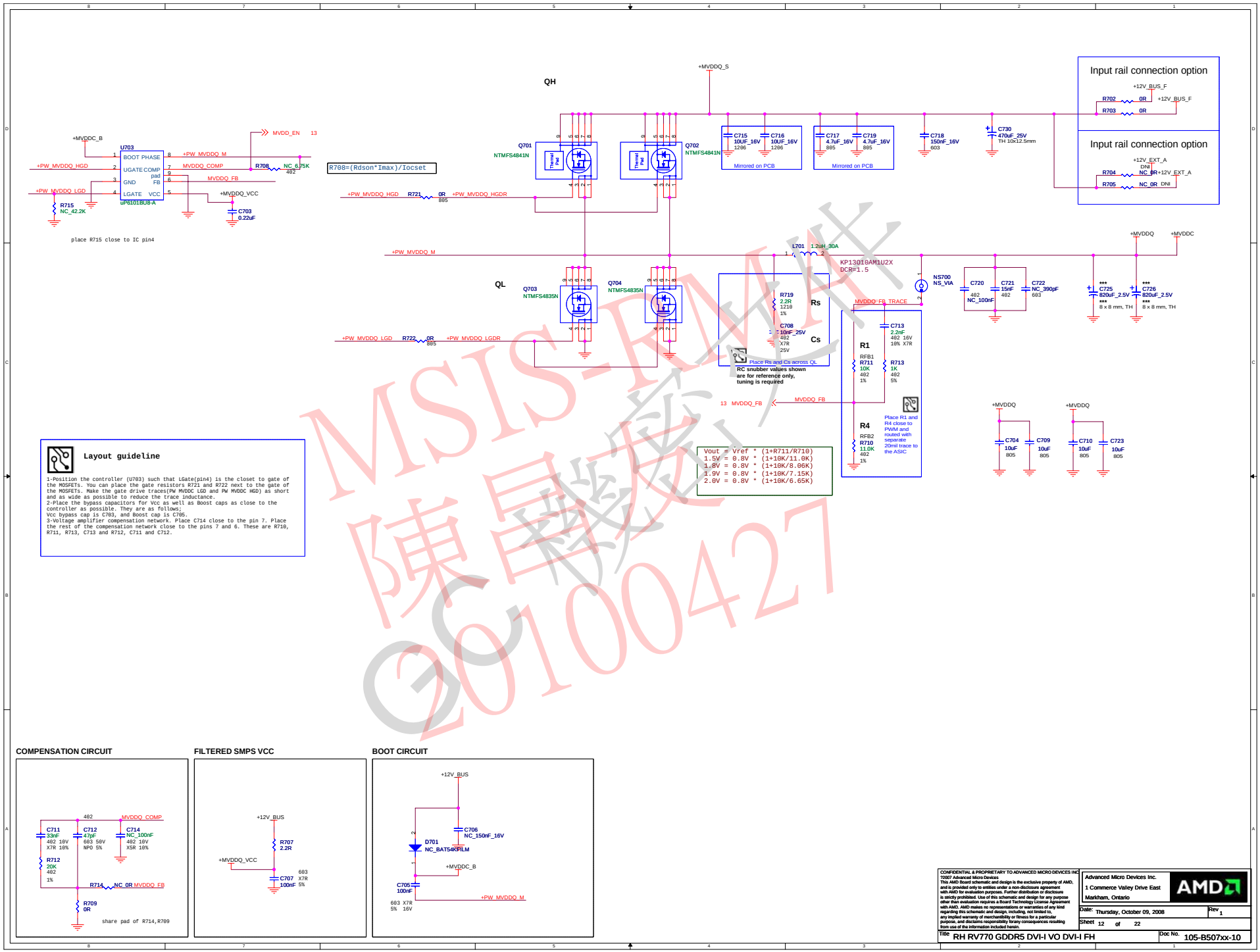

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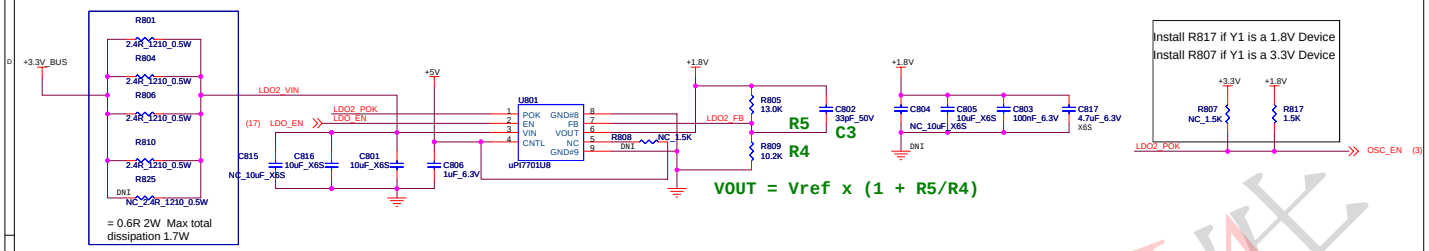
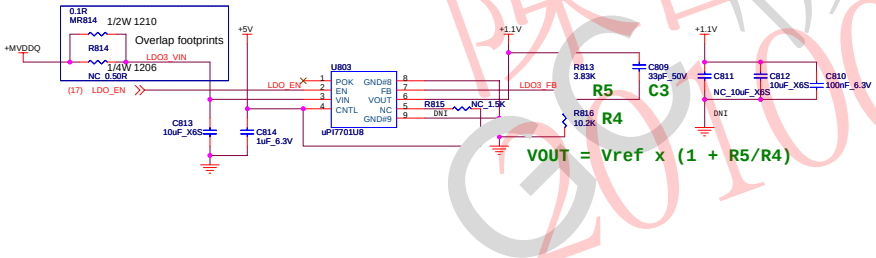
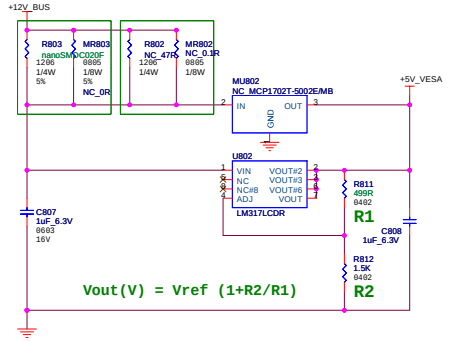
LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 1.7A (TBV) RMS MAX
PCB: Min 70mm sq. copper area for cooling

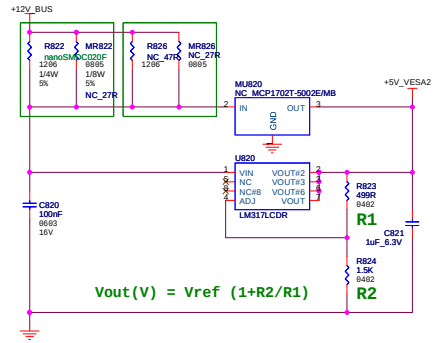


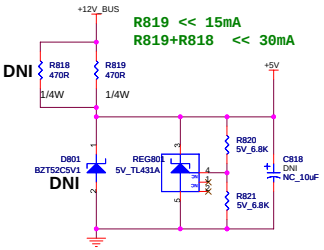
LDO #3: Vin = +1.50V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX
PCB: Min 70mm sq. copper area for cooling



Regulators for +5V, +5V_VESA and +5V_VESA2







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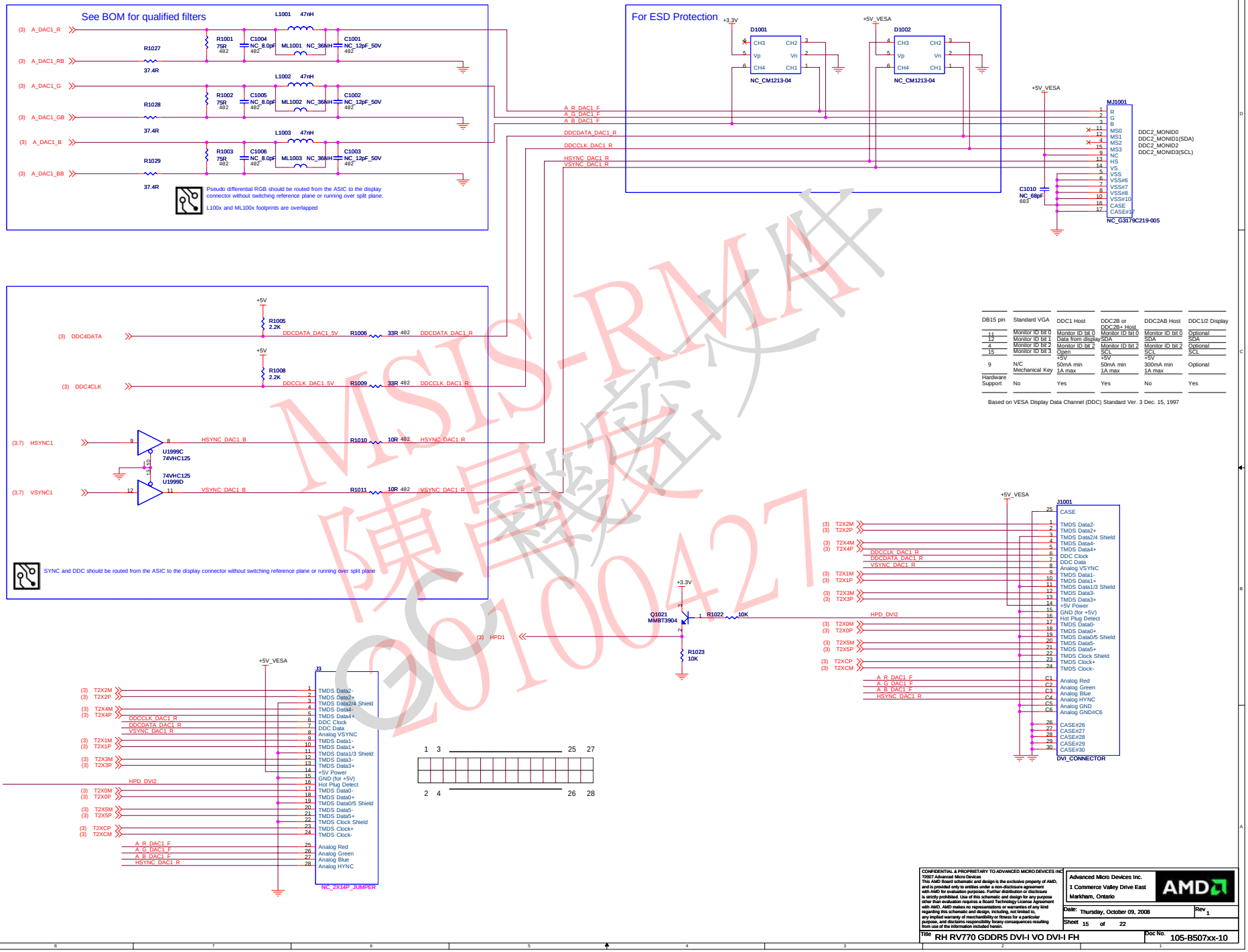

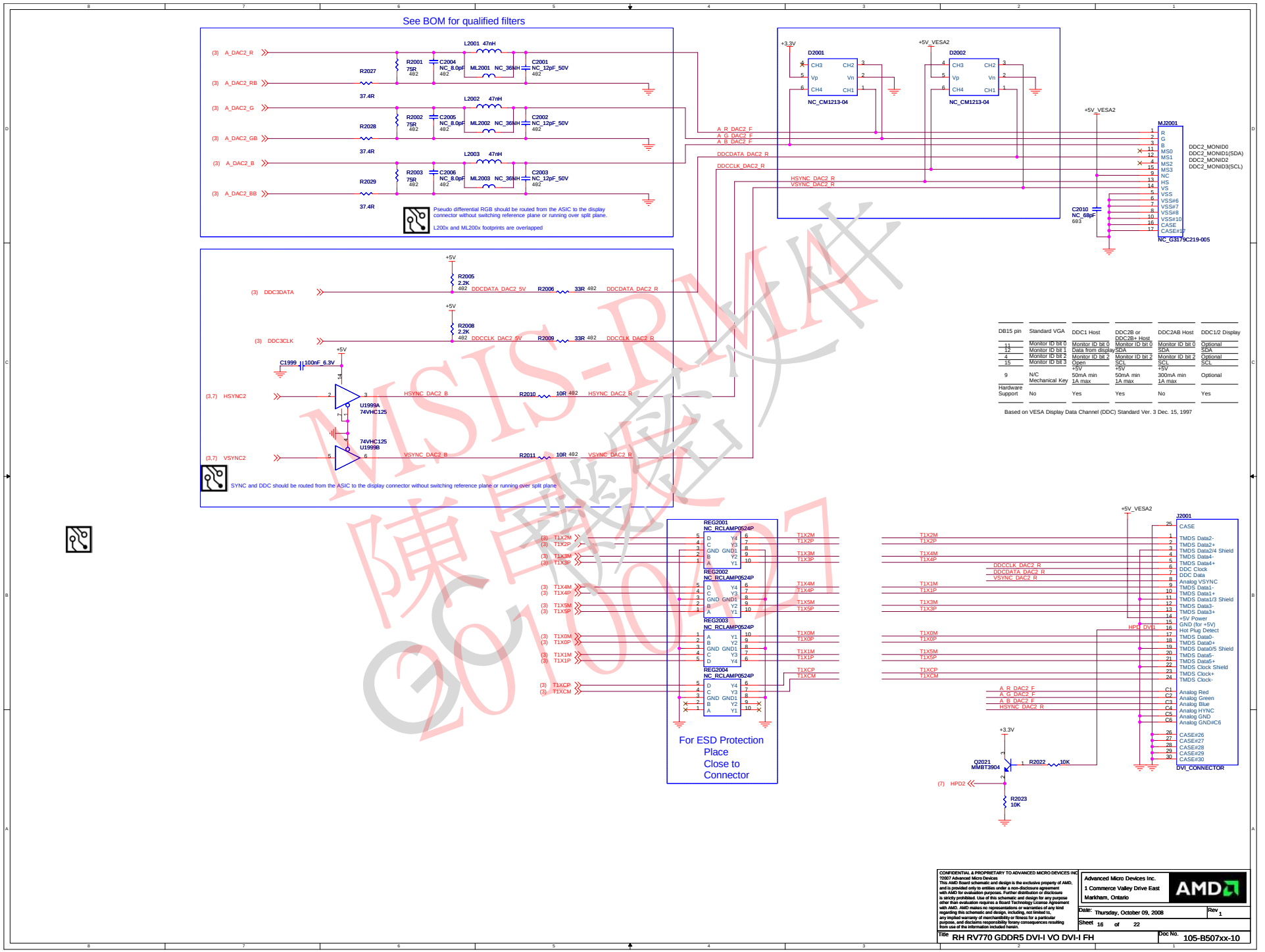

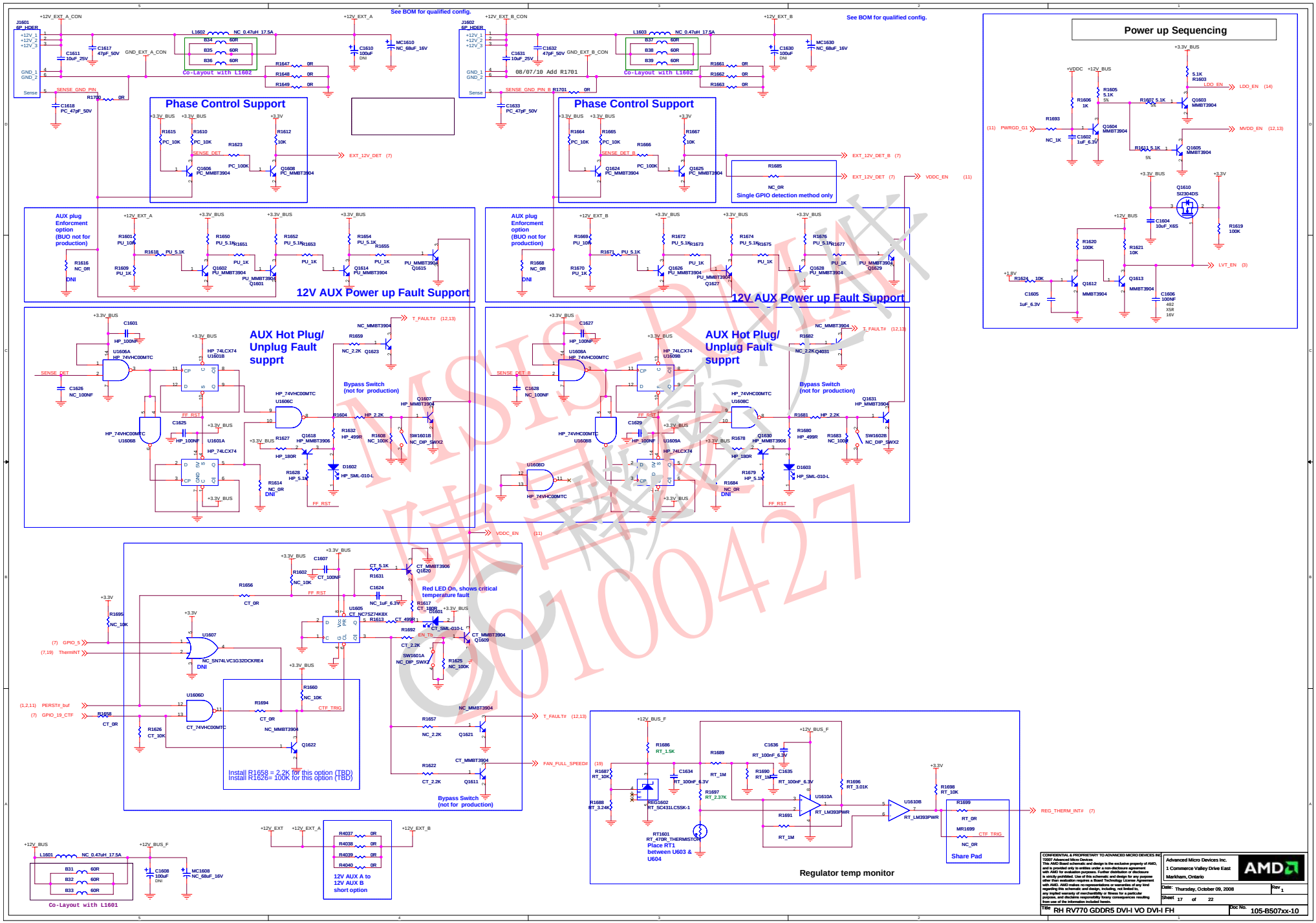

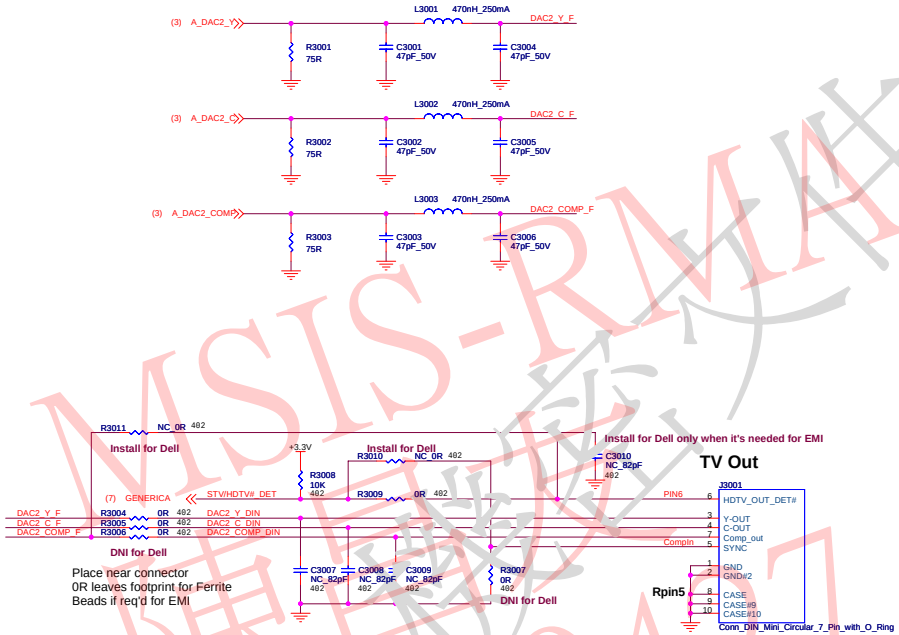

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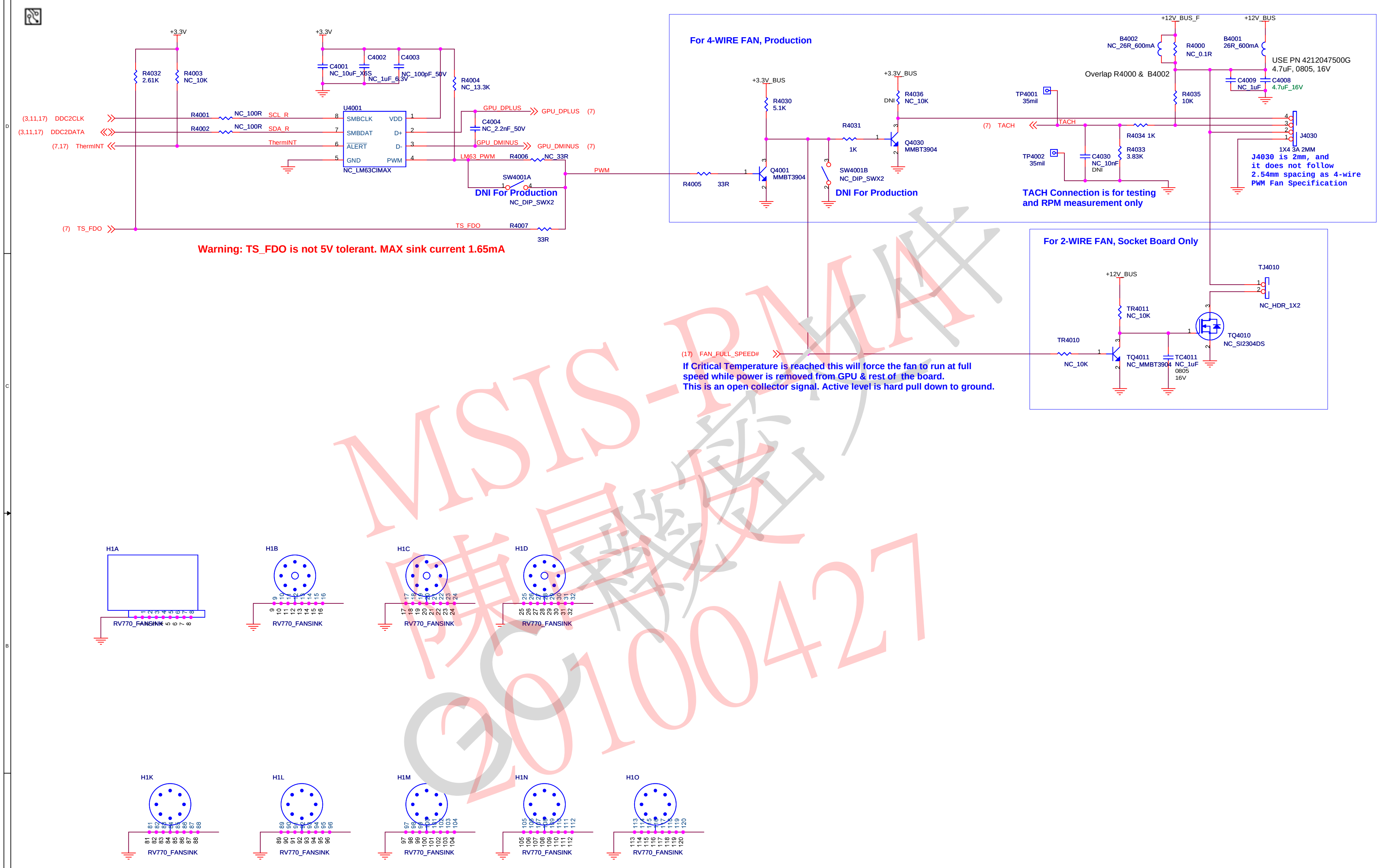

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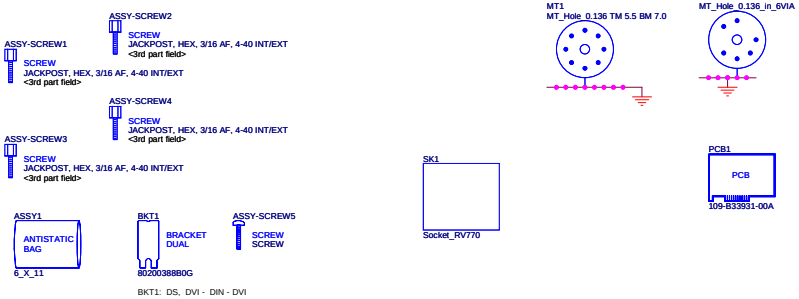

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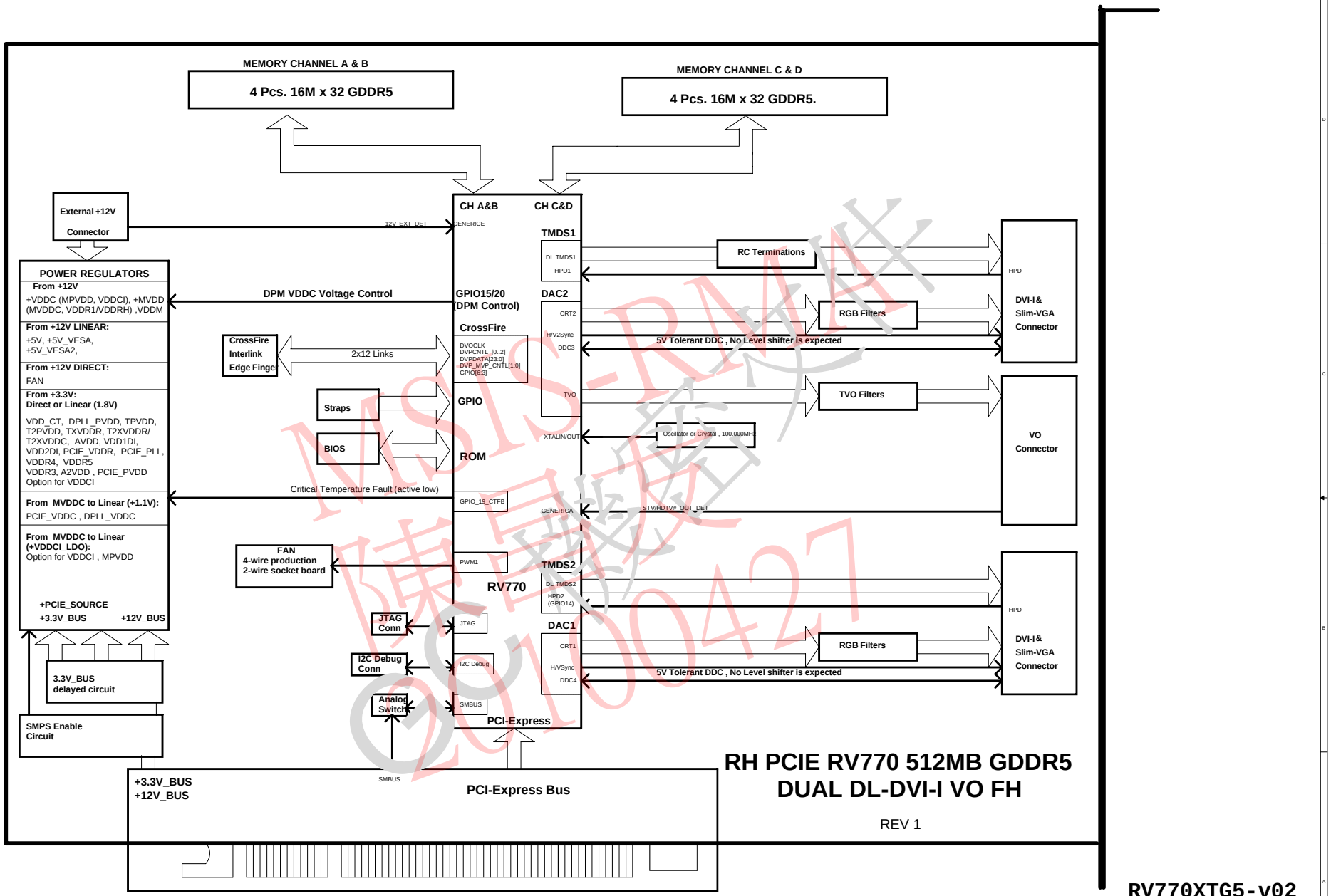
REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	08/01/04	Initial design for B507 based on B500 board with display chanaged to DVI VO- DVI
1	10	08/05/05	Based on B507-00 PCB with the following changes: 1. Spread Spectrum changed to MAXIM- pg.7 2. Add second 12V AUX power supply - pg.17 3. Add temperature monitor for VDDC regulator - pg.17 4. Add 12V_BUS & 12V_EXT input switch circuit - pg.17



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