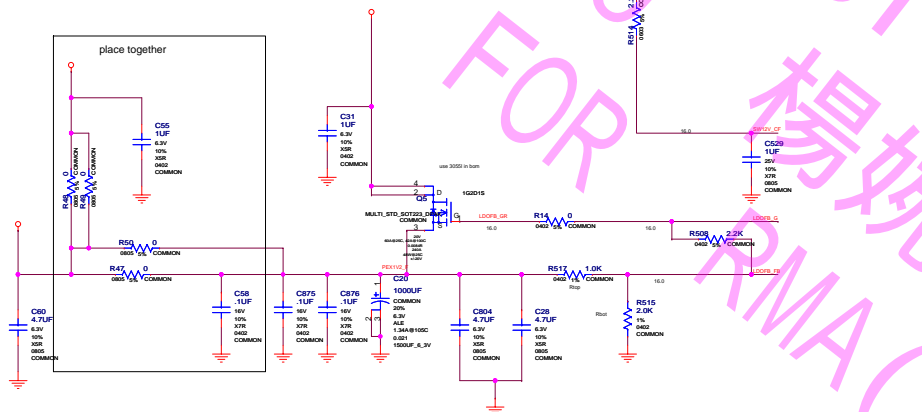
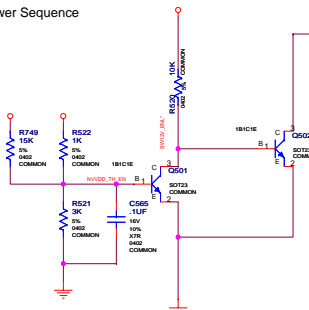


PowerSupplyIII: FBVDDQ, PEX1V2

$$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$$

$$1.227V = 0.8V * (1 + (1.65K/3.09K)) \text{ (ISL6549)}$$


Power down option
A3V3 Rtop 15K Rbot 10K
NVDD Rtop 1K Rbot 3K



RT9218

U101 RT9218B, V1.0, 8-PIN, 8-BIT, 50mA, 1.8V, 1.8V, 1.8V, 1.8V, 1.8V, 1.8V, 1.8V

SW12V_CF 11 VCC

LDOFB_G 5 LDO_DR

LDOFB_FB 9 LDO_FB

SW12VCF_1 6 NC

SW12VCF_2 7 NC

SW12VCF_3 8 NC

3 GND

PGOOD 10 SW1_PGOOD_M

PGOOD_M

UGATE 2 FB_LGM

BOOT 1 FB_BOOT

PHASE 14 FB_PHASE

OPS 13 SW12VCF_M

LGATE 4 FB_SG

SW_FB 12 FB_FB

R746 1K

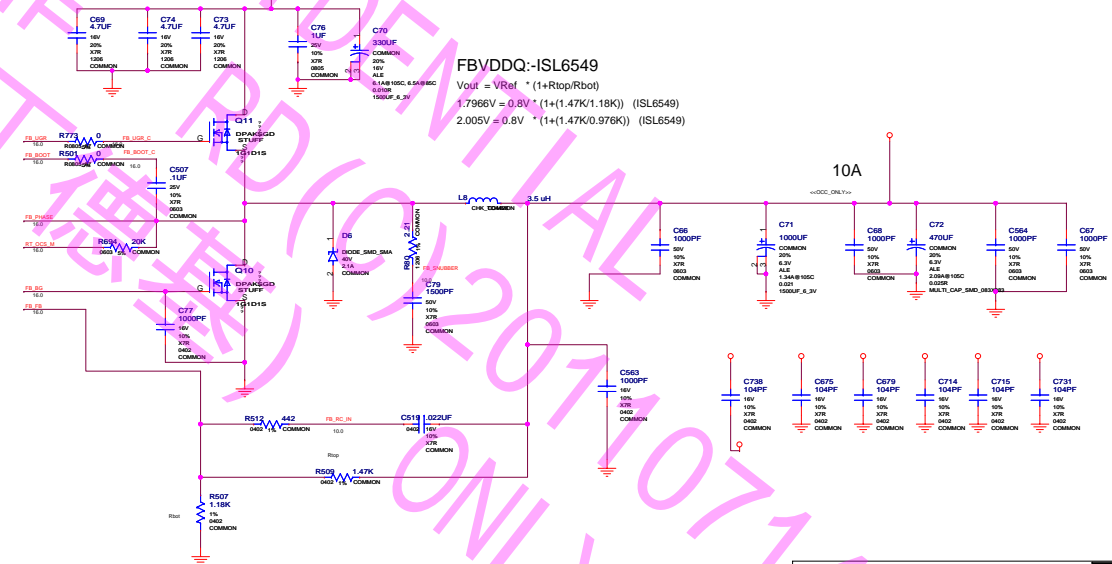
D15 RSX201L

Vout = VRef
1.8V = 0.8V
1.8V = 0.8V
2.003V = 0.8V

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

$$1.8V = 0.8V * (1 + (5k/4k)) \quad (RT9218)$$

$$1.8V = 0.8V * (1 + (200/160)) \quad (RT9218) \text{ Samsung MEM}$$

$$2.003V = 0.8V * (1 + (200/133)) \quad (RT9218) \text{ Infineon MEM default}$$
$$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$$
$$1.7966V = 0.8V * (1 + (1.47K/1.18K)) \quad (ISL6549)$$
$$2.005V = 0.8V * (1 + (1.47K/0.976K)) \quad (ISL6549)$$


Net Name	LINE_WIDTH	CURRENT	Voltage
FWD00	12MIL		1.8V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PowerSupply: FBVDDQ, PLLVDD

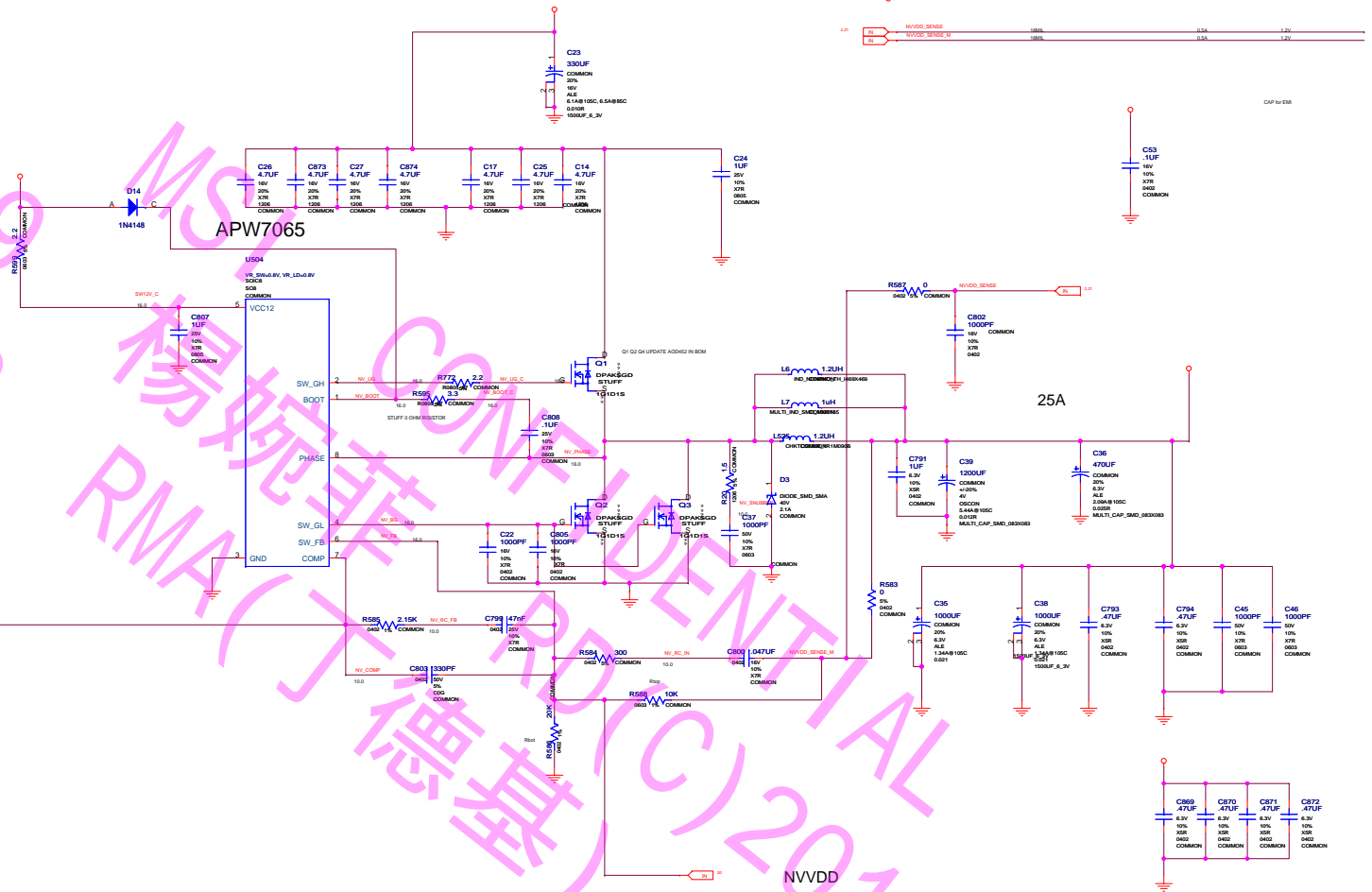
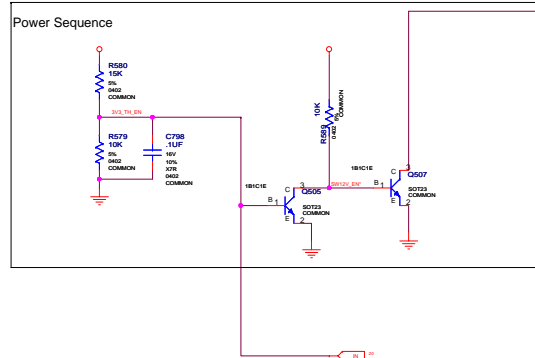
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PowerSupplyII: NVVDD




NVDD

$V_{out} = V_{Ref} * (1 + (R_{top}/R_{bot}))$

$1.1V = 0.8V * (1 + (1.54k/4.02k))$ (ISL6549)

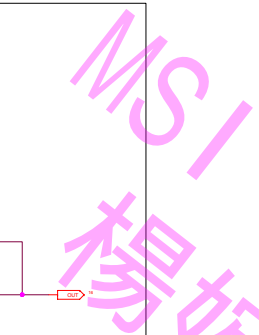
$1.2V = 0.8V * (1 + (1.54k/3.09k))$ (ISL6549)

$1.2V = 0.8V * (1 + (10k/20k))$ (APW7065)

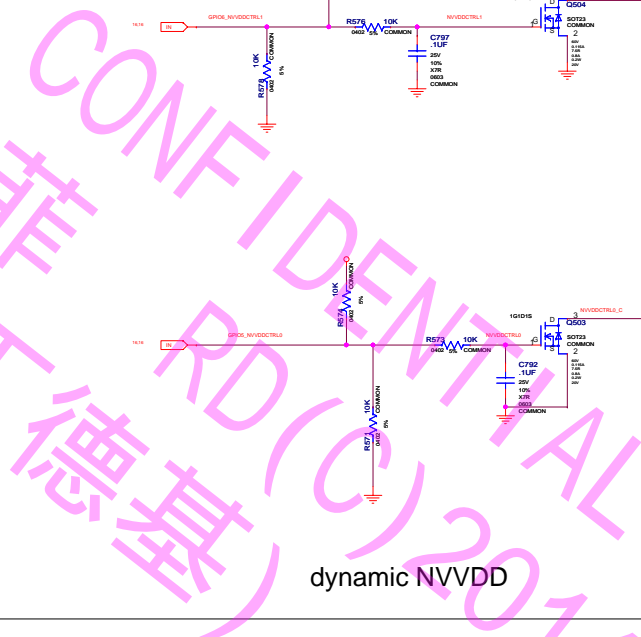
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Static and dynamic NVVDD



dynamic NVVDD



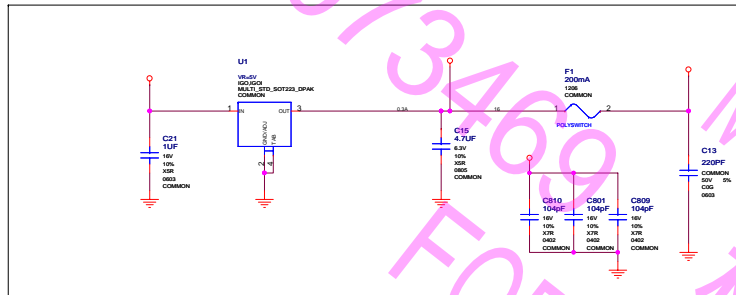
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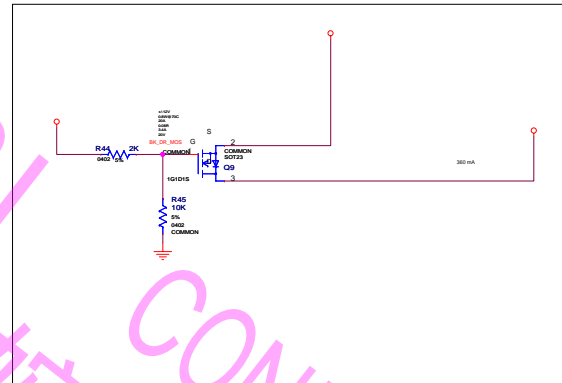
[illegible]

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DRG_BV	0.1A	12.0	5.00000V
AV50	1.5A	30.0	3.30000V
IPF46_VDD0	0.3A	16	3.30000V
GND		30.0	0.00000V
IPF_PU1VDD	0.3A	16	1.80000V

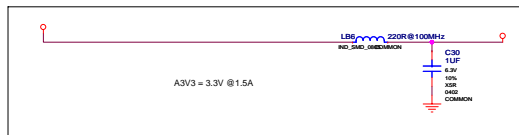
DDC 5V



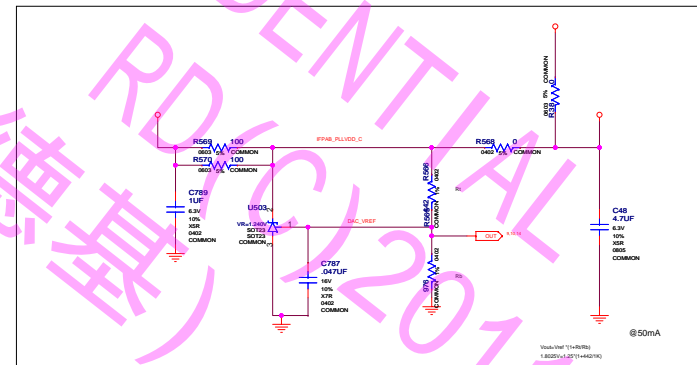
TMDS IO SUPPLY WITH BACKDRIVE PROTECTION



A3V3 Power Supply



IFP_PLL SUPPLY



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PAGE DETAIL	POWER SUPPLY: TMDS IOVDD,5V,A3V3

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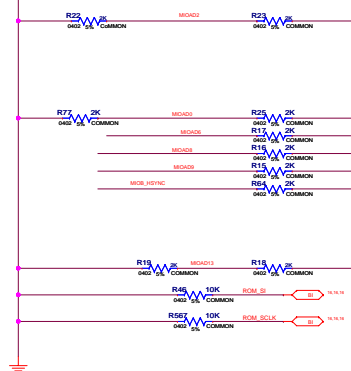
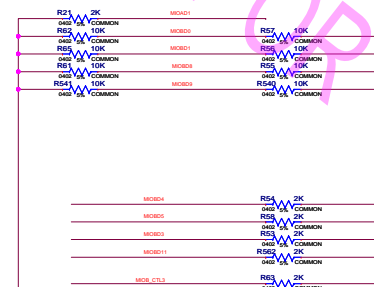
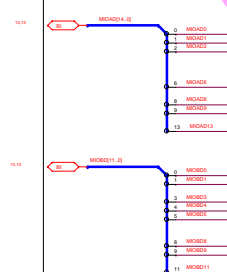
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Straps

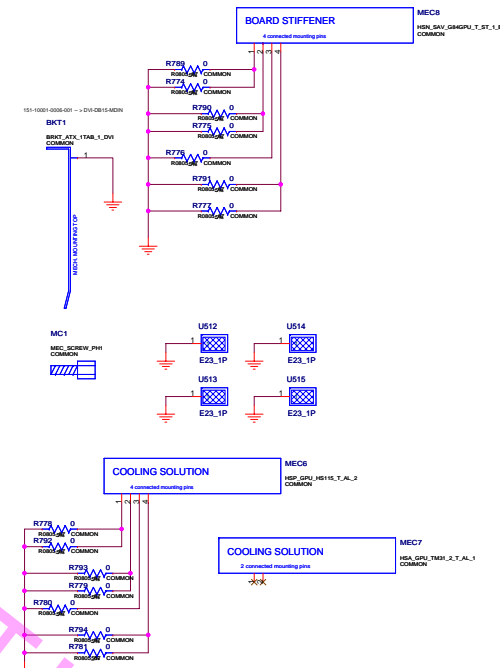
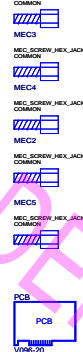


REG: NV_PEXTDEV_BOOT_0		
Bit Sign	VALUE_ID	VALUES
05: DV_WIDTH	GV_WIDTH	0x0000_0000
01: SUB_SELECTOR		0x0000_0000
04: RAM_CFG_0	RAM_VERSION	0x00_0000
03: RAM_CFG_1	RAM_CFG0_0	0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000
04: RAM_CFG_2		0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000
03: RAM_CFG_3		0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000
04: DEVSEL_0	CRPSTA	0x0000_0000 1x1x1x1x0000
02: TV_MODE_0	TV_MODE0_0	000_0000_0000 000_0000_0000 000_0000_0000 000_0000_0000 000_0000_0000 000_0000_0000 000_0000_0000 000_0000_0000
08: TV_MODE_1		1111_Reserved, 1
08: TVMODE02		1111_Reserved, 2
10: PDEV_DEV_0	PDEV_DEV0_0	0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000
11: PDEV_DEV_1		0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000
12: PDEV_DEV_2		0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000
13: PDEV_DEV_3		0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000
28: PDEV_DEV_EXT	PDEV_DEV0_Ext	0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000
14: FREQ0	Freq0_Reserved_0	0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000
15: FREQ1		0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000
16: FREQ2		0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000 0000_0000_0000_0000
22: ROM_TYPE_0	ROM_Type0_0	00_Persistent 01_Semi_Persistent 02_Volatile
23: ROM_TYPE_1		00_Persistent 01_Semi_Persistent 02_Volatile
24: USER_0	STRAP_USER0[0]	0000_Persistent
25: USER_1		0000_Persistent
26: USER_2		0000_Persistent
27: USER_3		0000_Persistent

17	PCK_ALL_EN_TERR100	0 (default - internal term only)	
18	30G0_PADQG_LUT_ADR[0]	0000-Createop 0001-Abuse 0010-Abuse NTWHS LLAMP 0011-Abuse NTWHS LLAMP 1000-Abuse NTWHS LLAMP 1001-Abuse NTWHS LLAMP 1010-Abuse NTWHS LLAMP 1011-Abuse NTWHS LLAMP 1100-Abuse NTWHS LLAMP 1101-Abuse NTWHS LLAMP 1110-Abuse NTWHS LLAMP 1111-Abuse NTWHS LLAMP	1001-Abuse NTWHS LLAMP 1010-Abuse NTWHS LLAMP 1011-Abuse NTWHS LLAMP 1100-Abuse NTWHS LLAMP 1101-Abuse NTWHS LLAMP 1110-Abuse NTWHS LLAMP 1111-Abuse NTWHS LLAMP
20	30G0_PADQG_LUT_ADR[2]		
21	30G0_PADQG_LUT_ADR[3]		

31: StrapControl0 per SW		
REG: NV_STRAP_1		
Bit Signal	VALUE_ID	VALUEs
15: Start Clock Configuration		0=Disable 1=Enable
12: MIO_EN_33V_0	MIOA_VDDQ Voltage	0=2.5V 1=3.3V
13: MIO_EN_33V_1	MIOB_VDDQ Voltage	0=2.5V 1=3.3V
16: PCI_JOBAR		0=Disable 1=Enable

MEC



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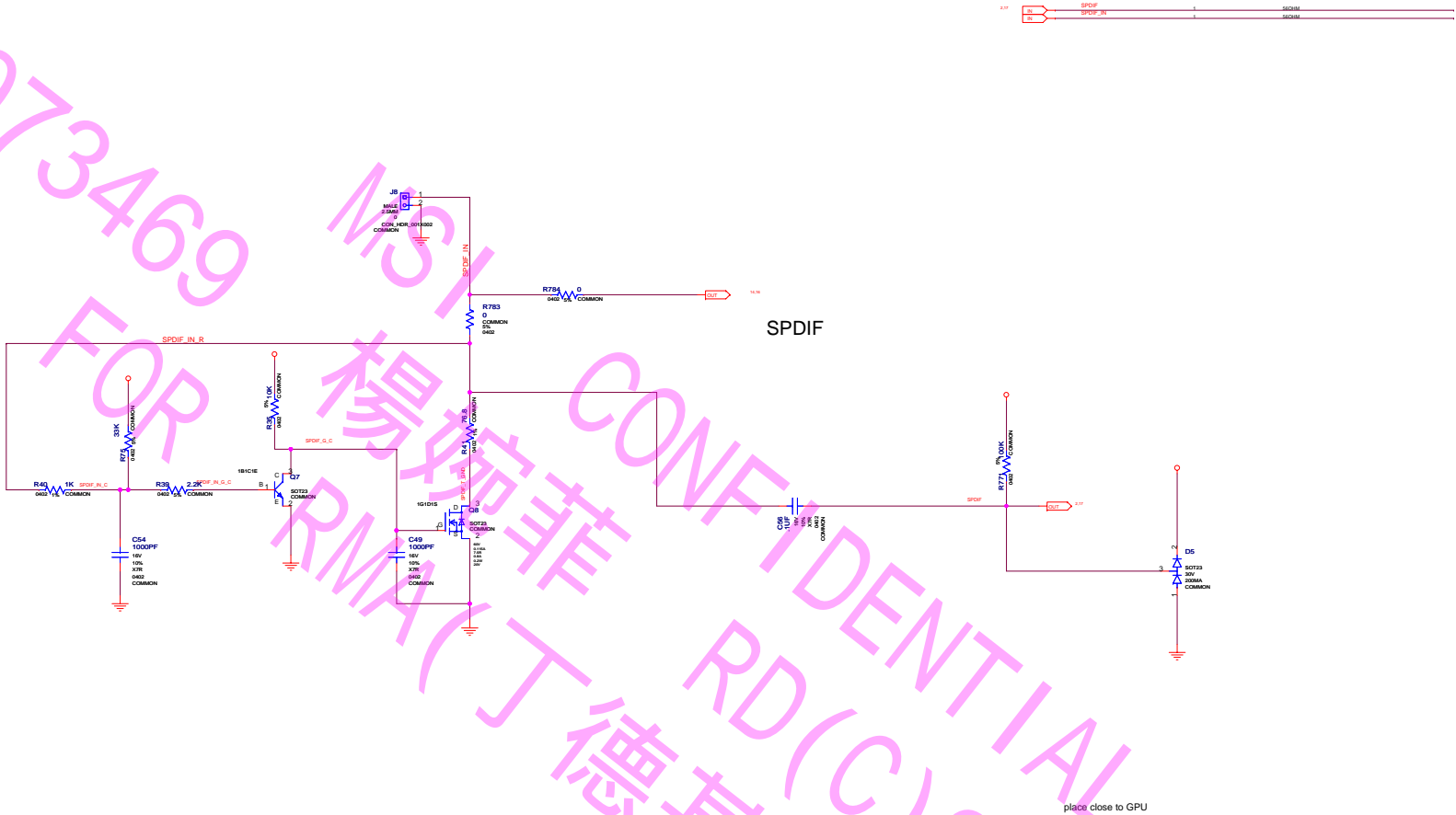
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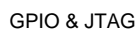
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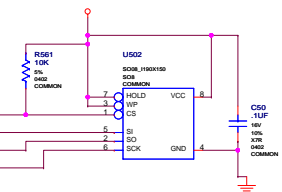
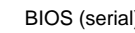
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PAGE DETAIL	SPDIF

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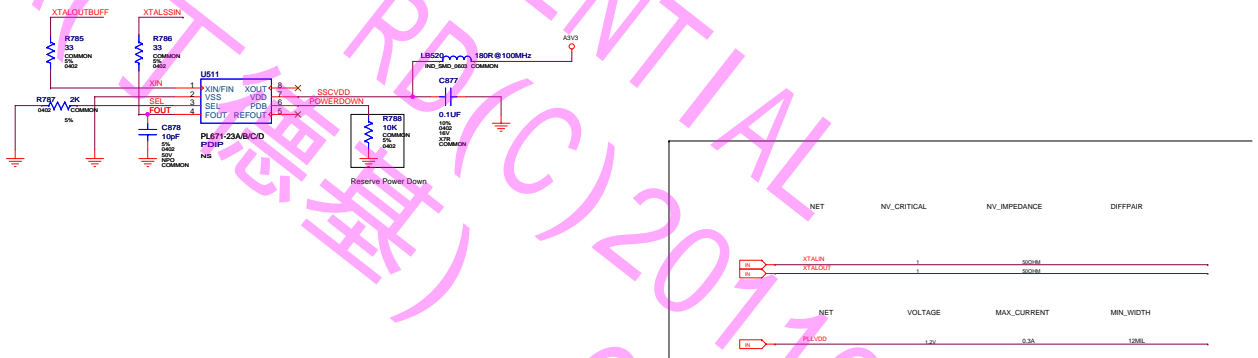
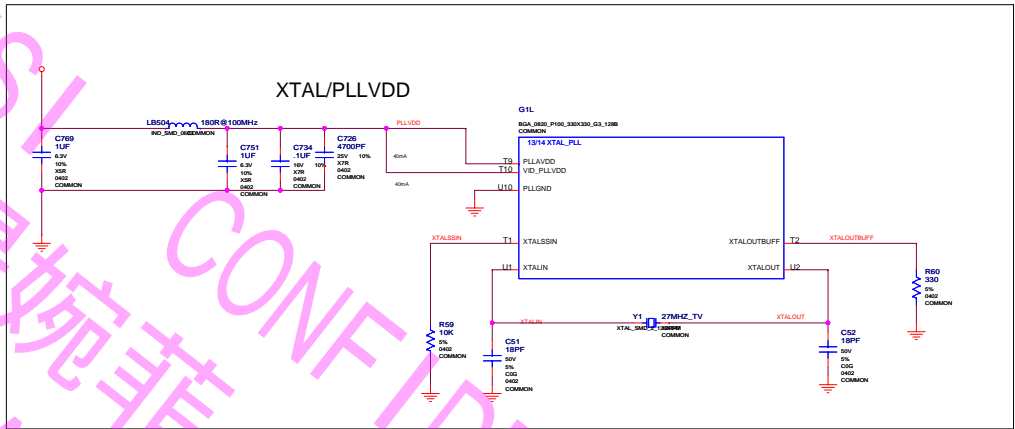
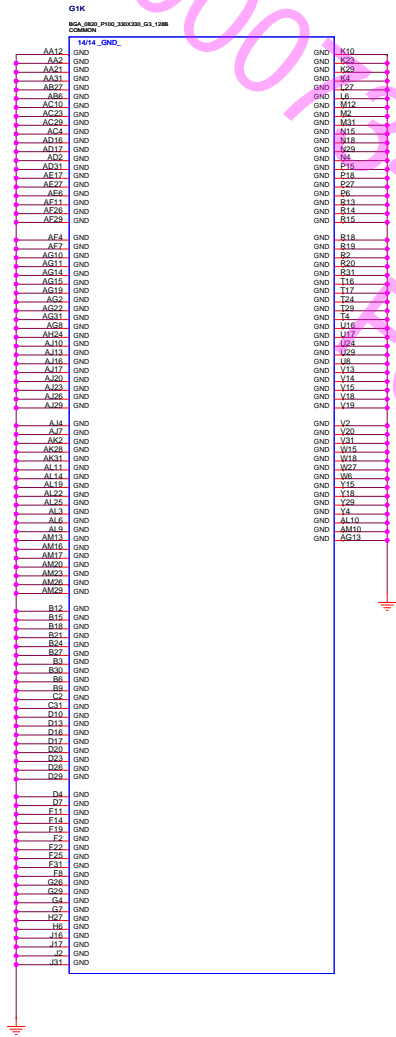


GPI0	IO	FUNCTION
0	IN	RESERVED

[illegible]

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GPU GND CONNECTION, XTAL



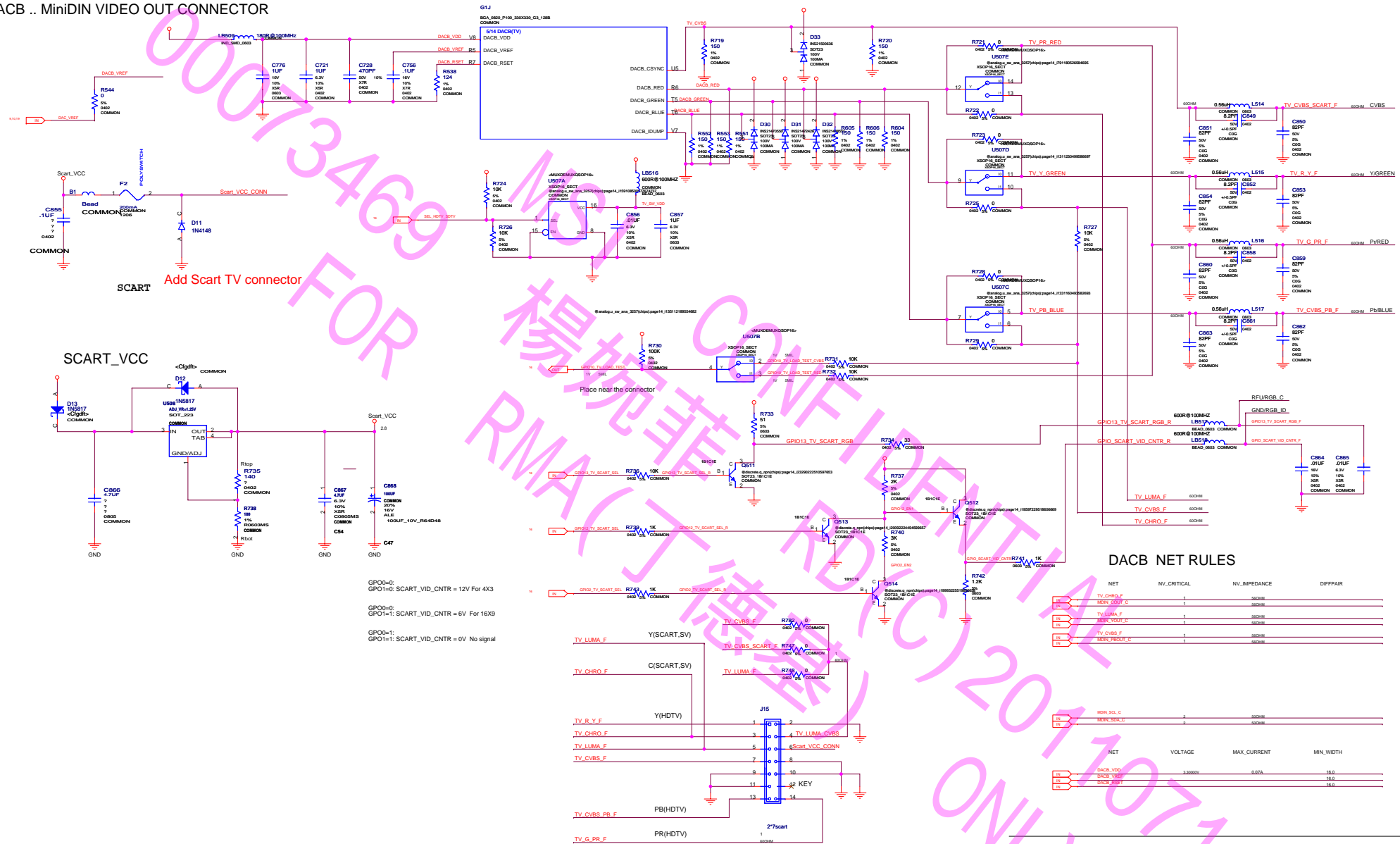
NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
XTALIN	1	50OHM	
XTALOUT	1	50OHM	
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
PLL VDD	1.2V	0.3A	12MIL

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PAGE DETAIL	GPU GND CONNECTION, XTAL

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DACB .. MiniDIN VIDEO OUT CONNECTOR

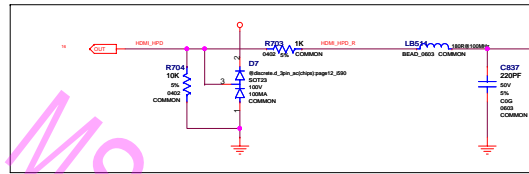


NET		NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
10	TV_CHIRUP_F	1	50OHM	
11	MORF_ROOT_C	1	50OHM	
12	TV_CHIRUP_F	1	50OHM	
13	MORF_ROOT_C	1	50OHM	
14	TV_CHIRUP_F	1	50OHM	
15	MORF_ROOT_C	1	50OHM	
16	MORF_ROOT_C	2	50OHM	
17	MORF_ROOT_C	2	50OHM	
18	MORF_ROOT_C	2	50OHM	
19	MORF_ROOT_C	2	50OHM	
20	MORF_ROOT_C	2	50OHM	
21	MORF_ROOT_C	2	50OHM	
22	MORF_ROOT_C	2	50OHM	
23	MORF_ROOT_C	2	50OHM	
24	MORF_ROOT_C	2	50OHM	
25	MORF_ROOT_C	2	50OHM	
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27	MORF_ROOT_C	2	50OHM	
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32	MORF_ROOT_C	2	50OHM	
33	MORF_ROOT_C	2	50OHM	
34	MORF_ROOT_C	2	50OHM	
35	MORF_ROOT_C	2	50OHM	
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95	MORF_ROOT_C	2	50OHM	
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INTERNAL TMD5 .. LINK C

Hotplug Detection

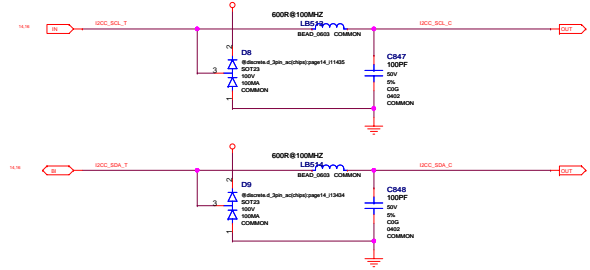
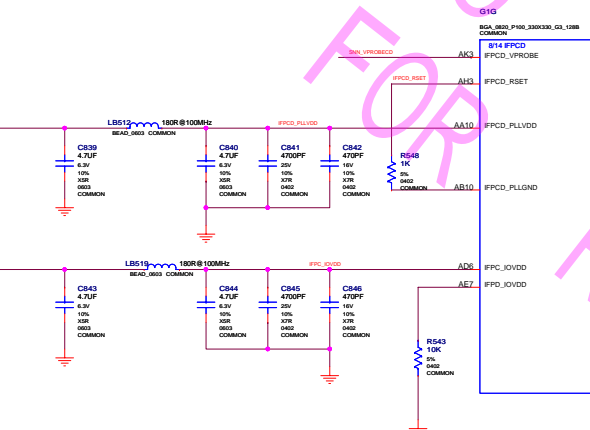
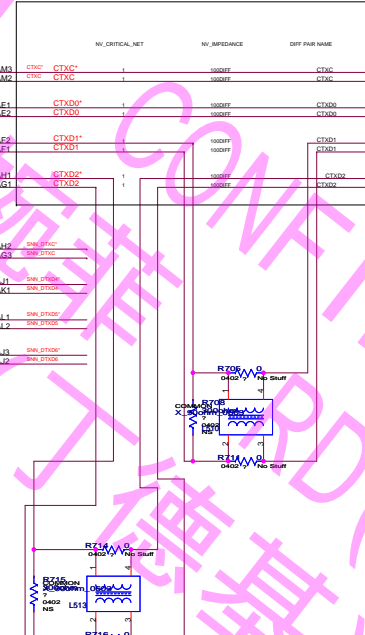
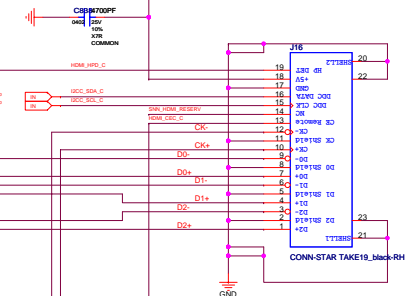


IFPAB NET RULES



NET RULES

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLVDD	3.3000V	0.04	16.0
IFPAB_PVDD	3.3000V	0	16.0
IFPAB_PVDD	3.3000V	0.15	16.0




CEC pullup and charging must be disconnected from HDMI connection when Power Down

ASSEMBLY	STATE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMD5 LINK C

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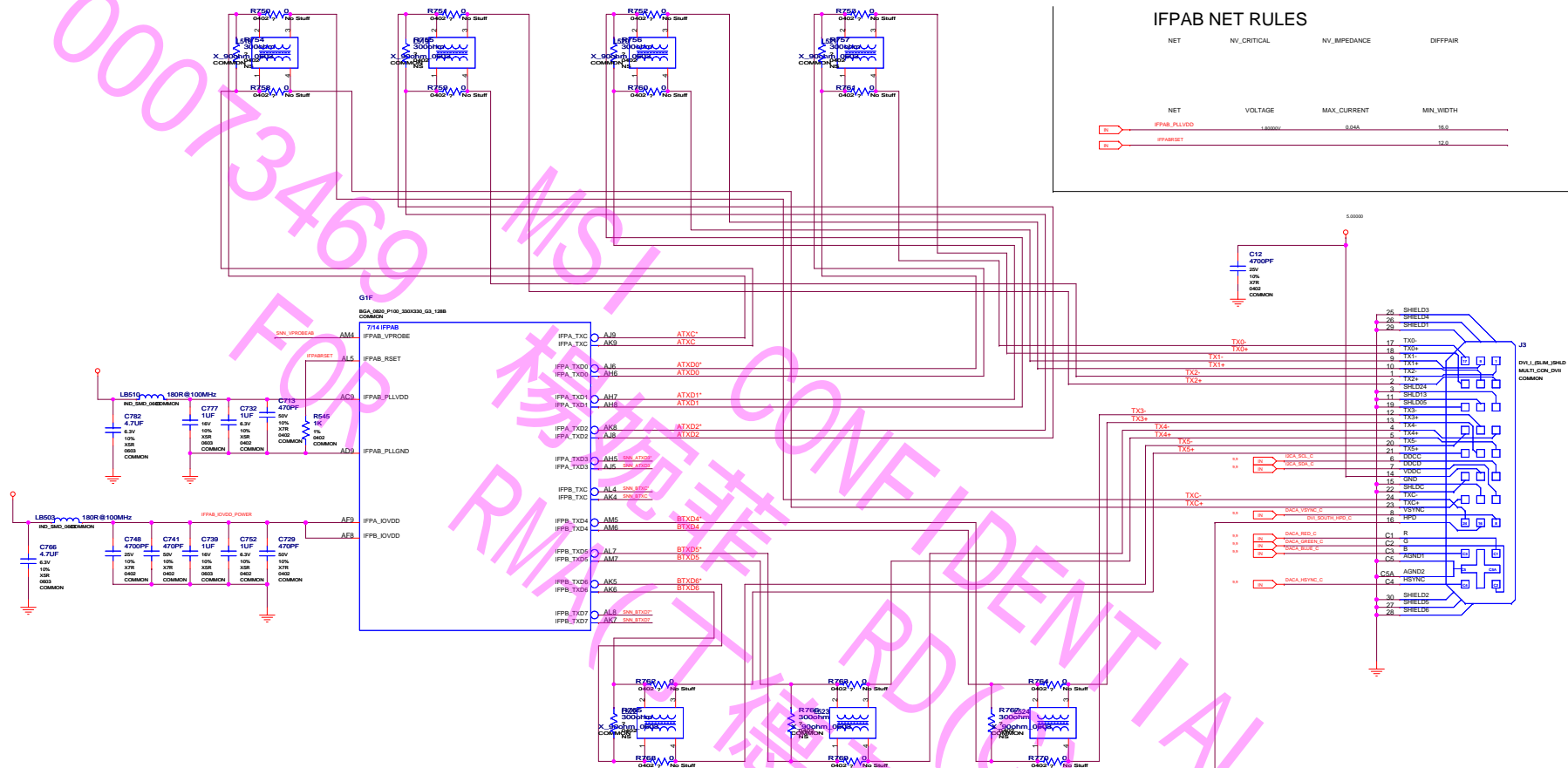
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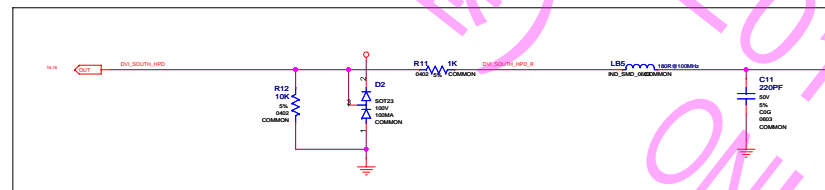
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IFPAB NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	FPAD_PLVDD	1.8000V	5000	18.0
IN	FPADRIET			12.0



Hotplug Detection



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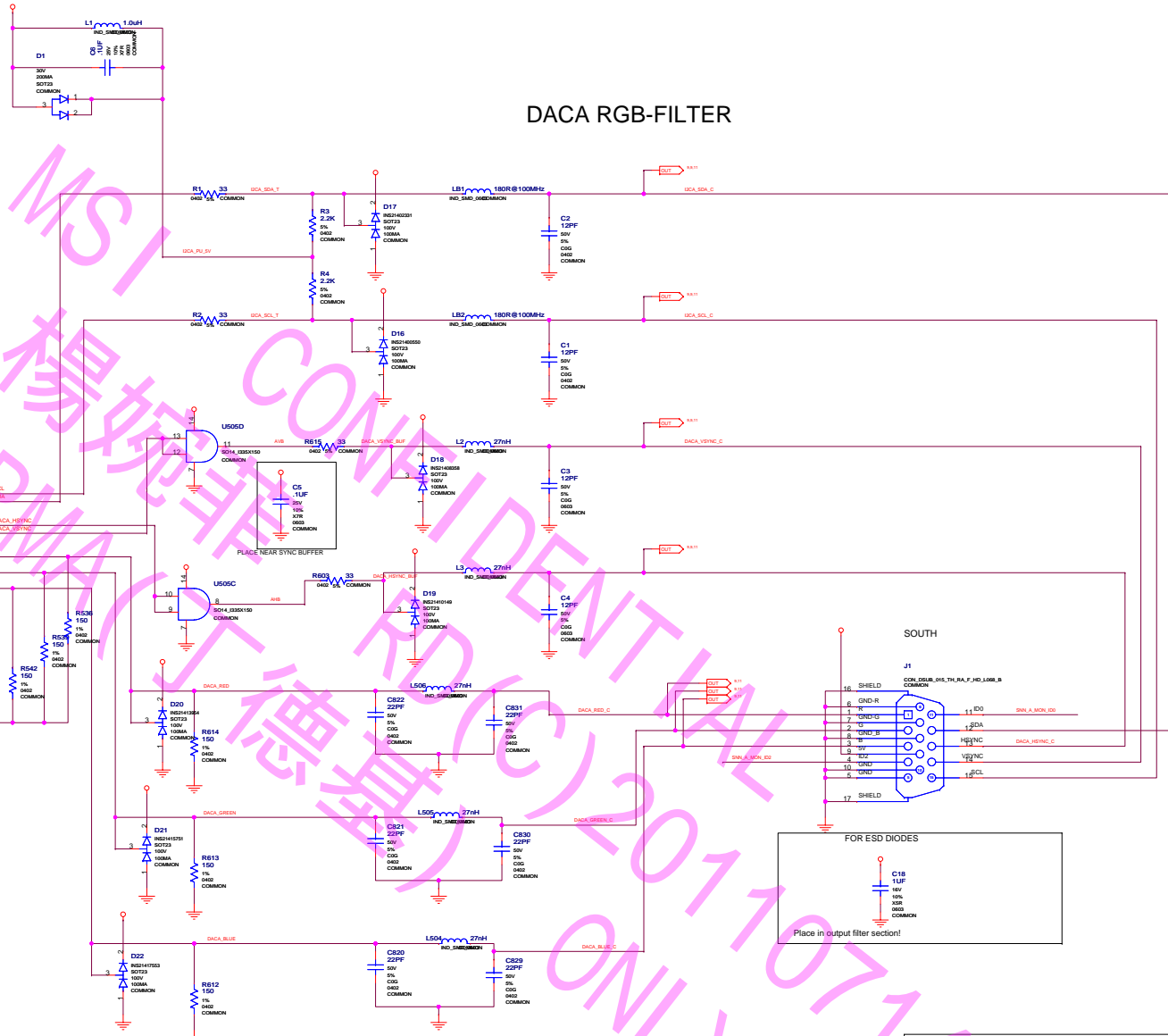
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Secondary Display (DACC), DB15

DACCC RGB-FILTER

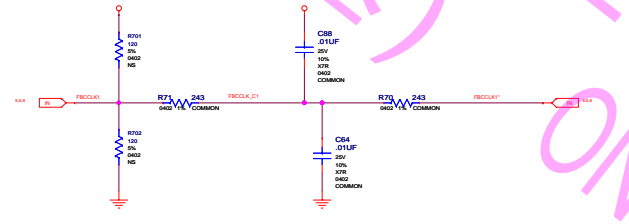
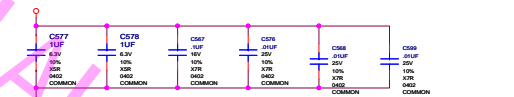
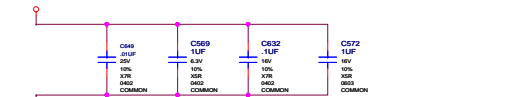
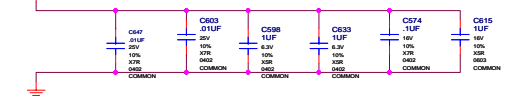
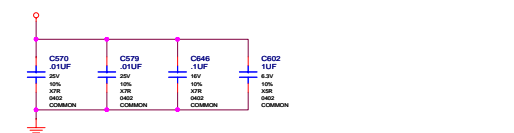
Primary Display (DACA), Slim DB15

DACA RGB-FILTER

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16Mx16 DDR2 MEMORIES, 2ND BANK 32_63

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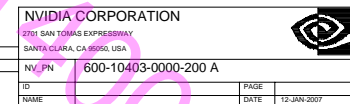


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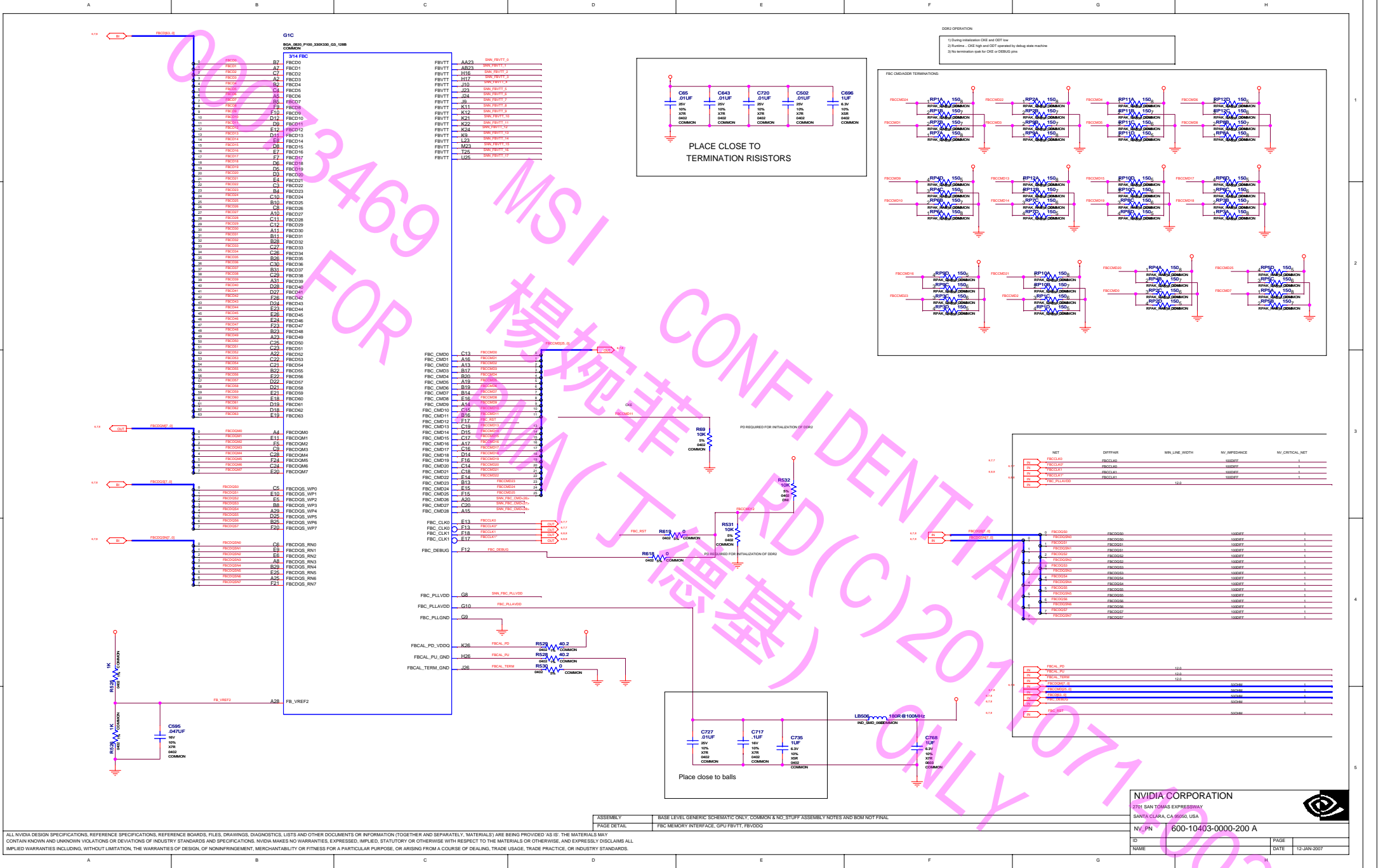
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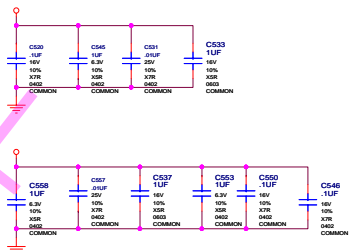
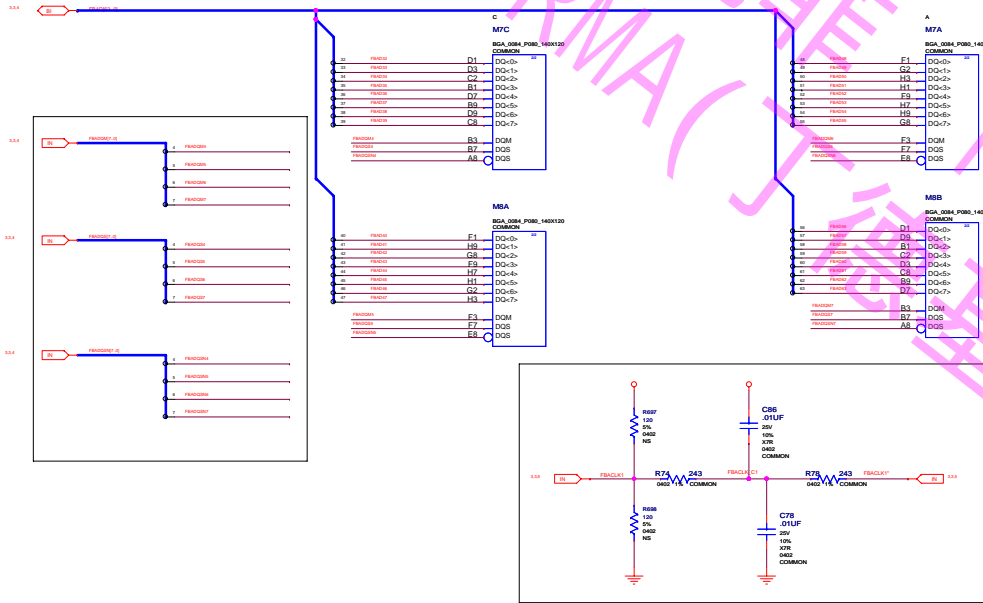
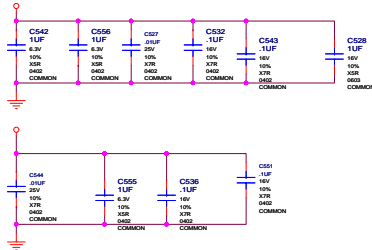
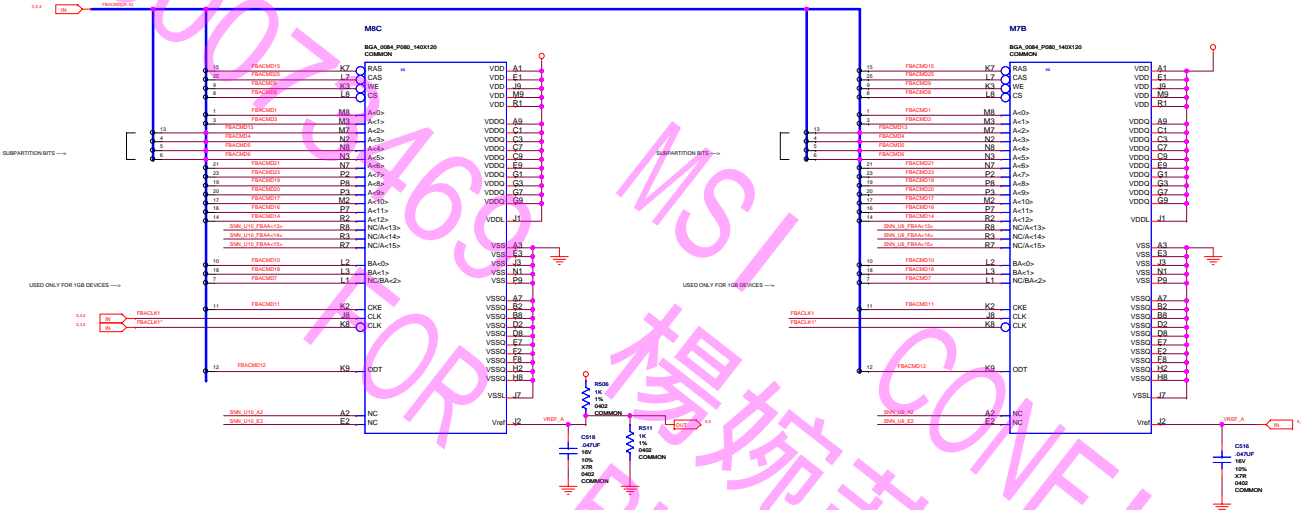
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PAGE DETAIL	FB MEMORY INTERFACE, CPU FBVTT, FBVDD

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FBA MEMORY 1st bank 32..63
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 10701 ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16GB GDDR5 MEMORIES, 1ST BANK 32..63

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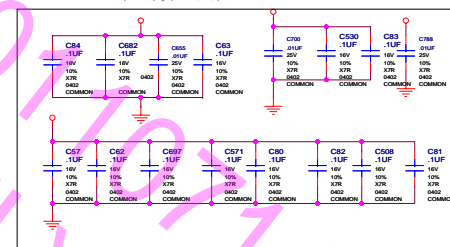
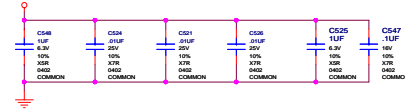
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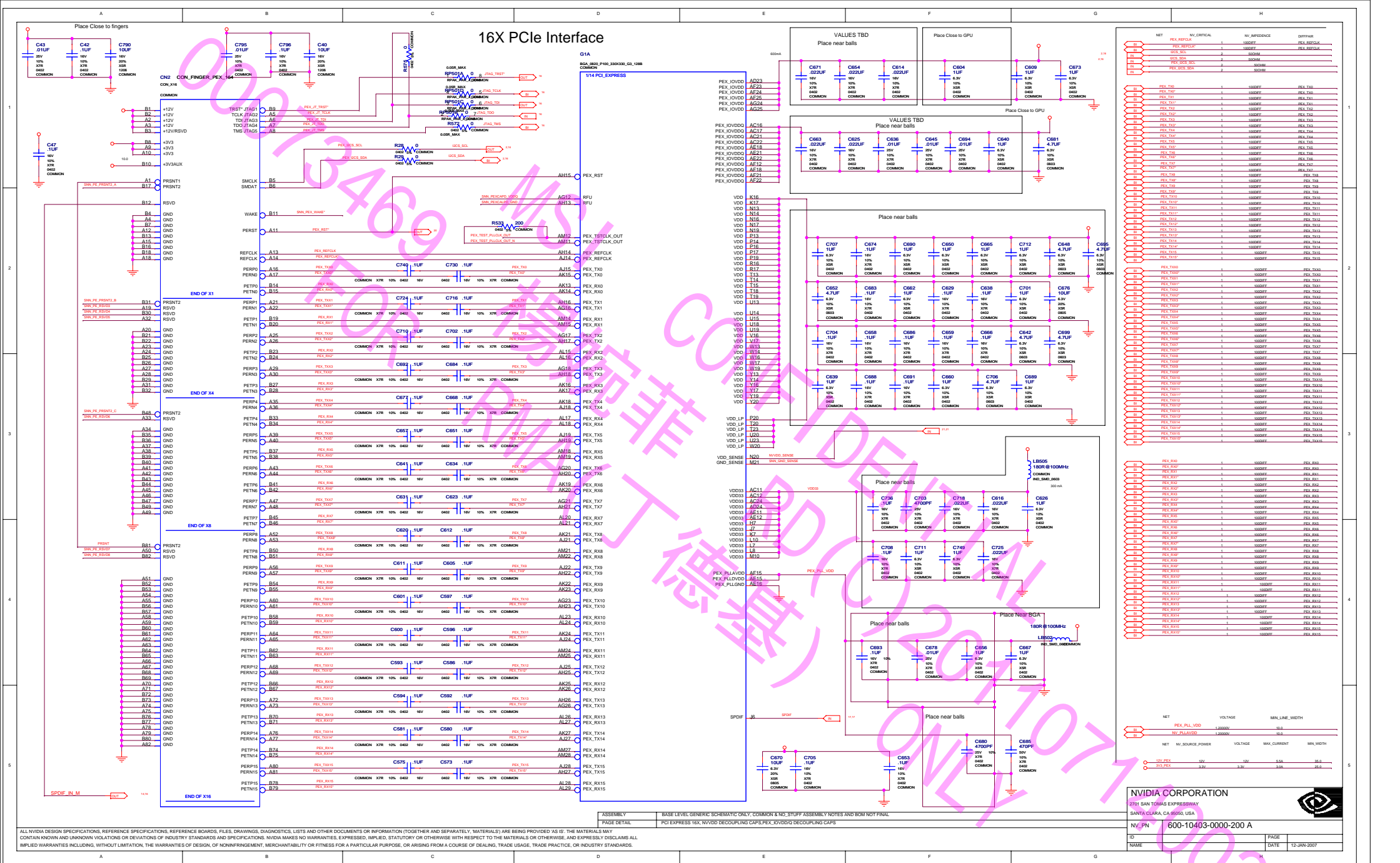
DATE

12-JAN-2007

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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P403-B00 DESIGN -- G84-200, 256 MB DDR2,DVI-I, VGA, HDTV

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REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10403-0000-200	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKUD020	600-10403-0020-200	P403 B00 G84-300 459/400MHz 256MB 16Mx16 BGA84 GDDR2 DVI-I DL+VGA+HDTV-Out
2	SKUD021	600-10403-0021-200	P403 B00 G84-200 459/400MHz 256MB 16Mx16 BGA84 GDDR2 DVI-I DL+VGA+HDTV-Out
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