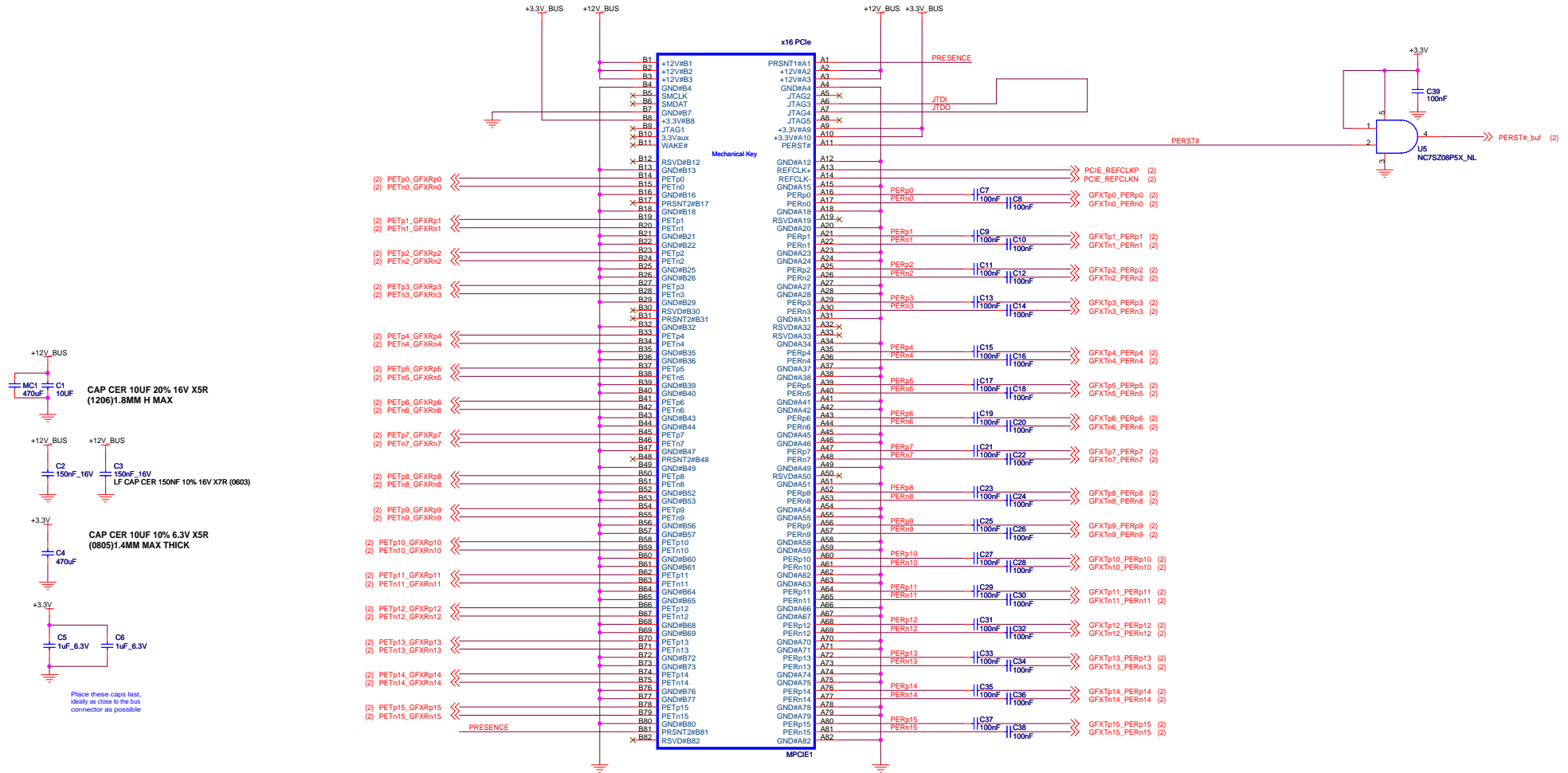


PCI-EXPRESS EDGE CONNECTOR

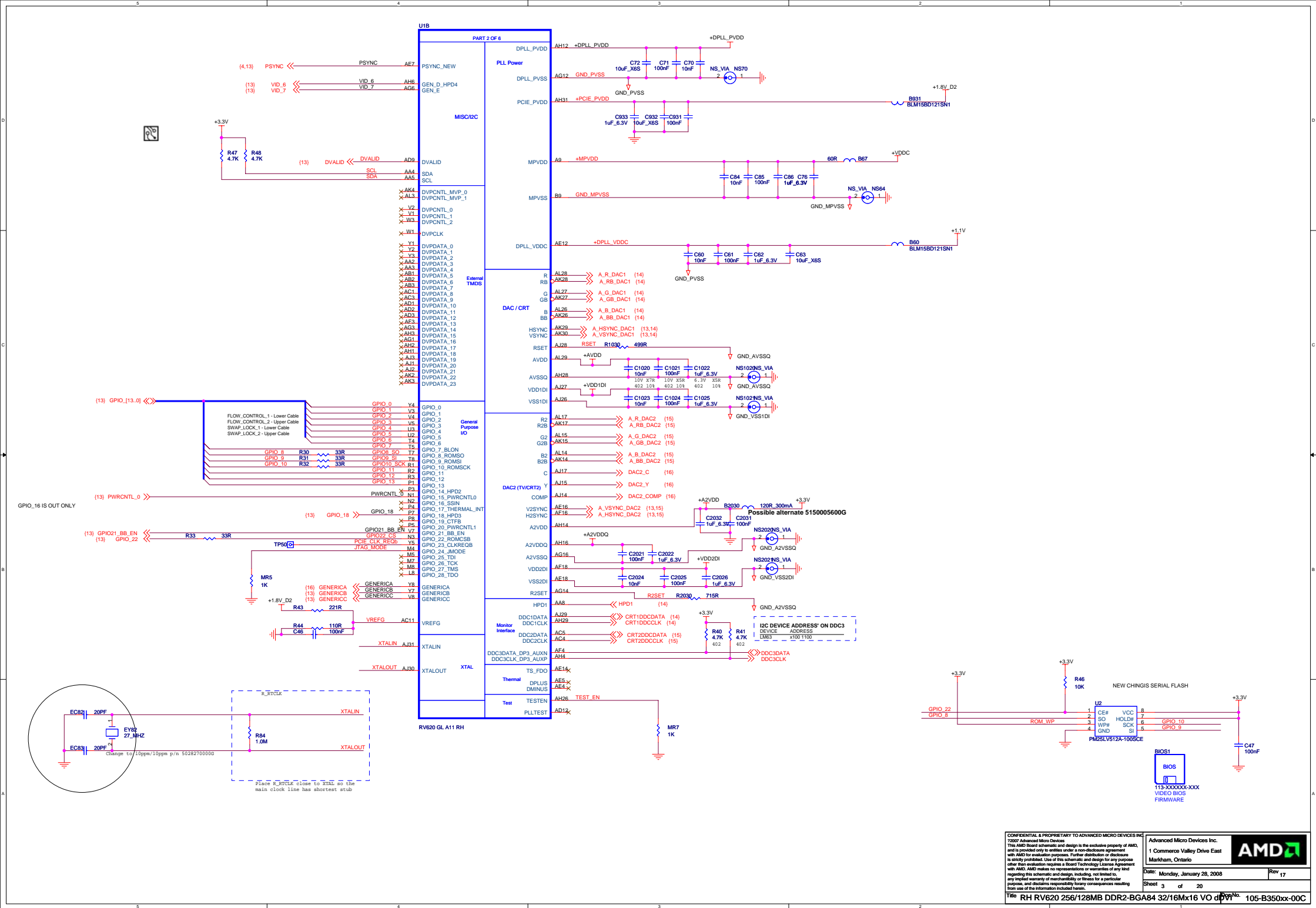


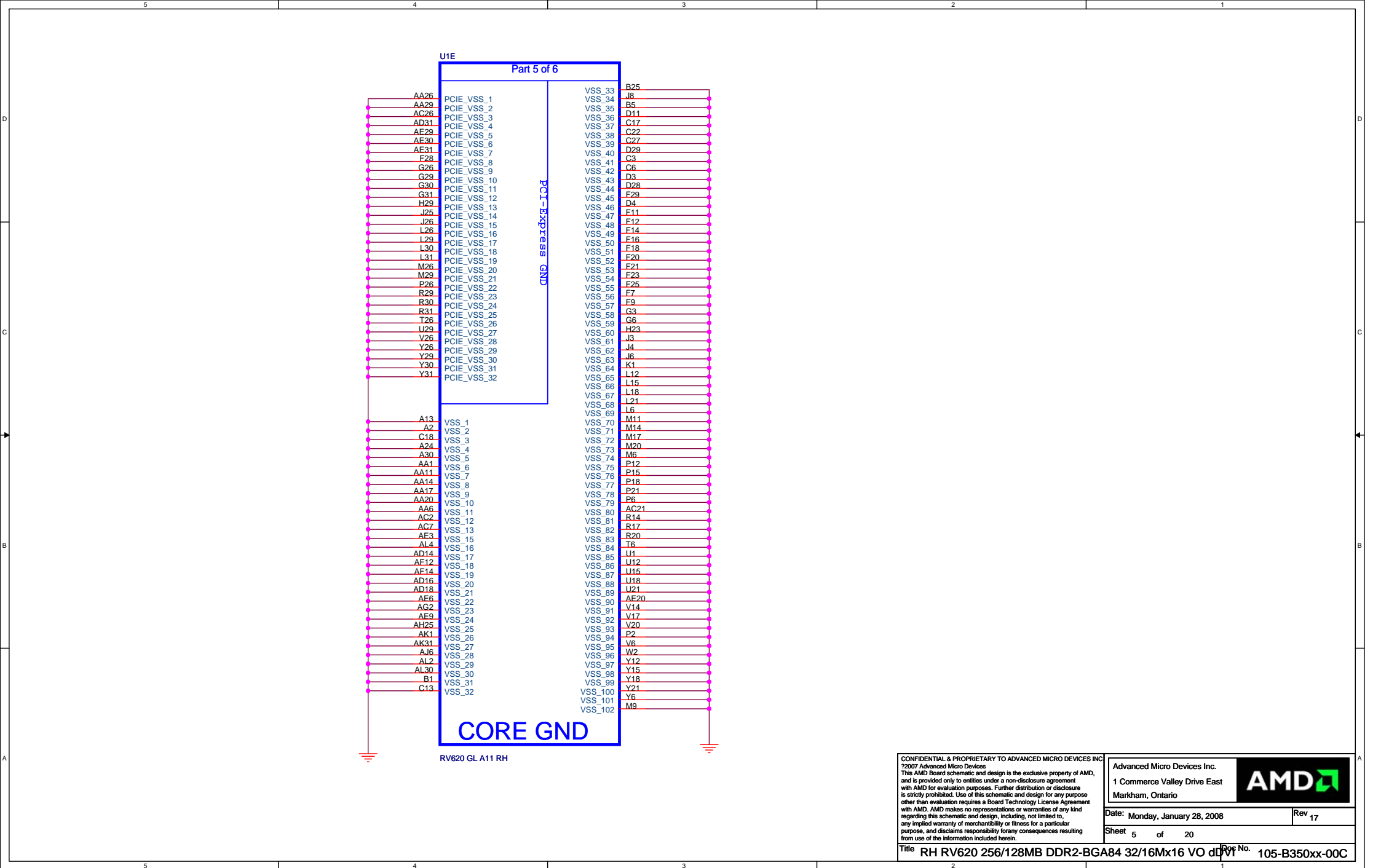
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

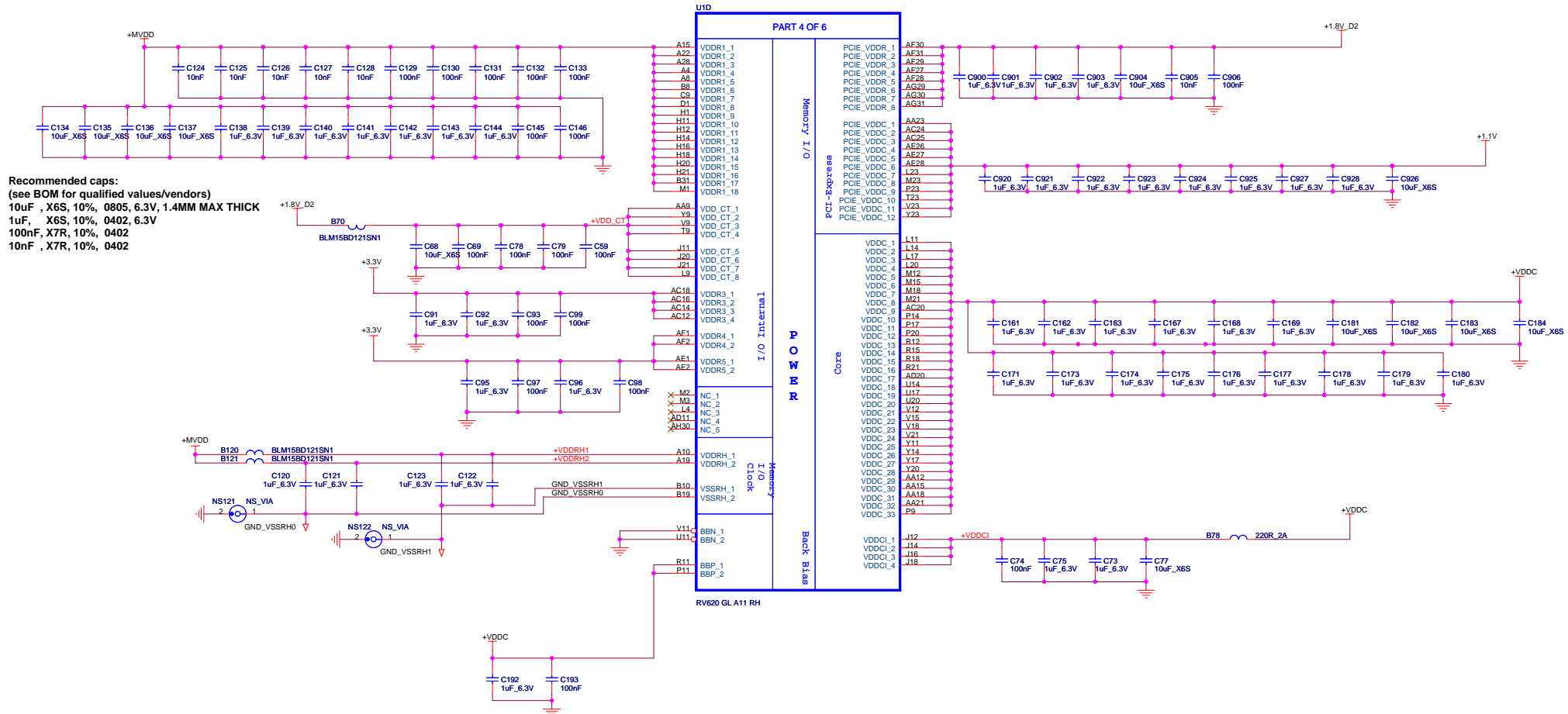
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Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF , X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402

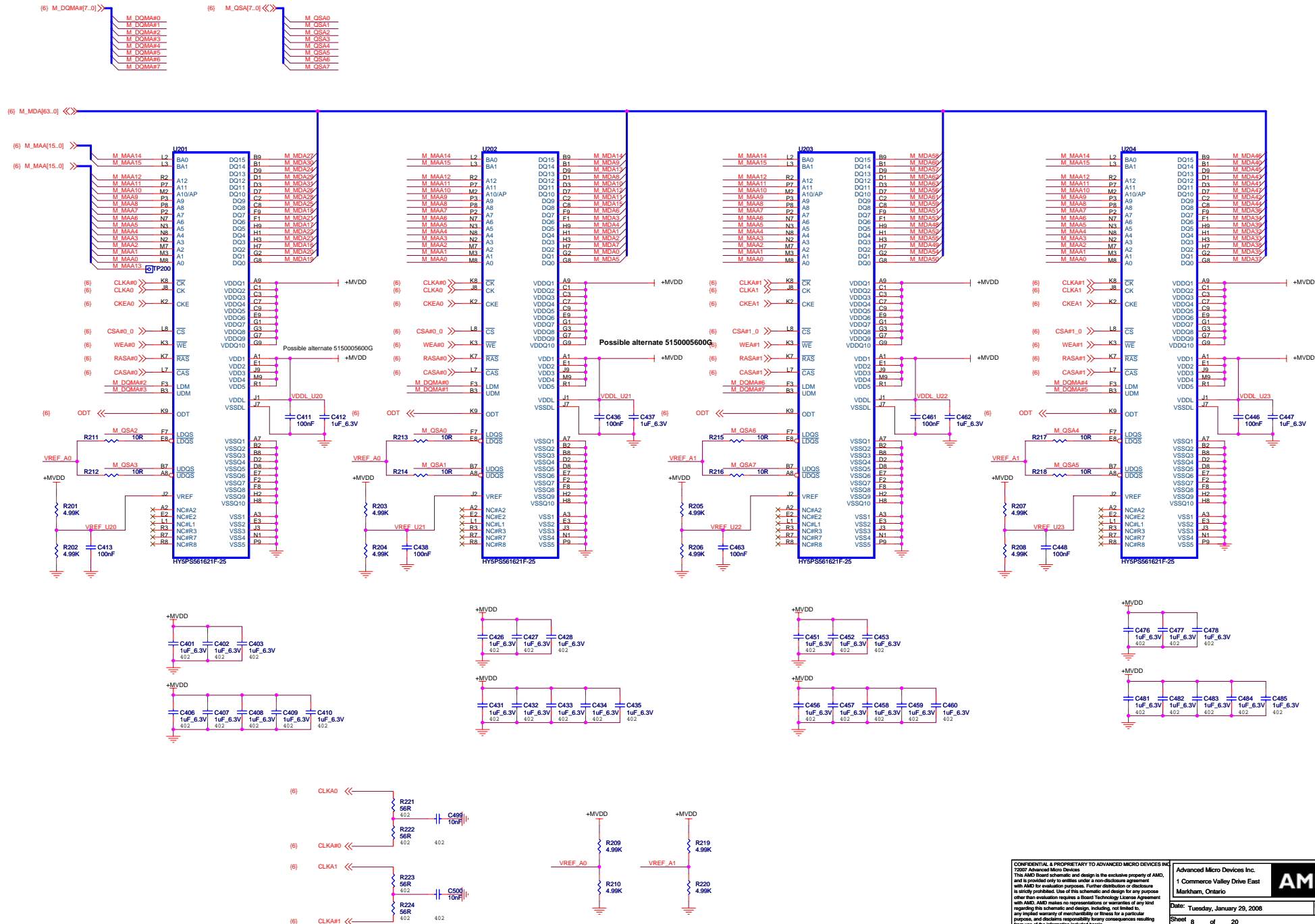
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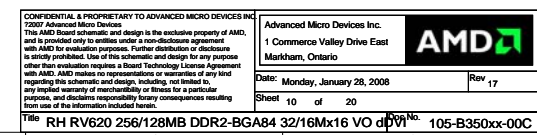
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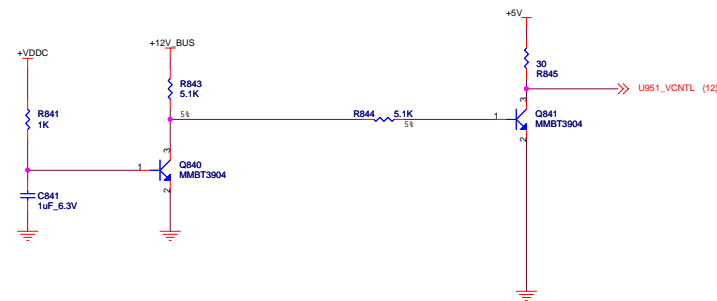
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CHANNEL A: RANK 0 128MB DDR2







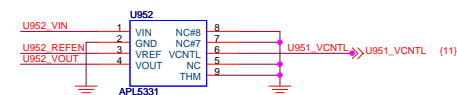
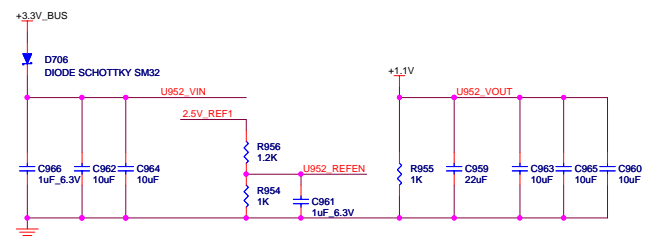
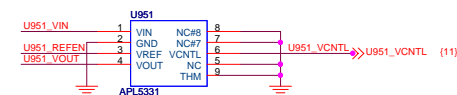
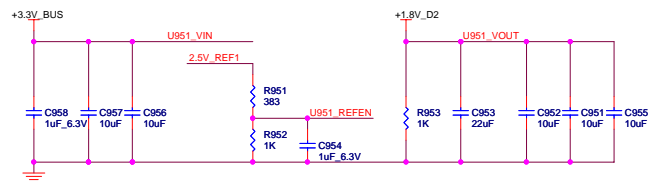
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Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO ddr



Shared Power Rails



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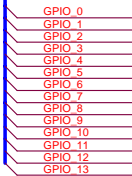
Rev

Title		RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dVFI		Doc No.		105-B350xx-00C	
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PSYNC
DVALID

RV610: (DEFAULT) MR70, R73, MR74, MR75 INSTALLED
RV620: MR70, MR73, MR74, MR75 MUST BE INSTALLED

(3) GPIO_13_0



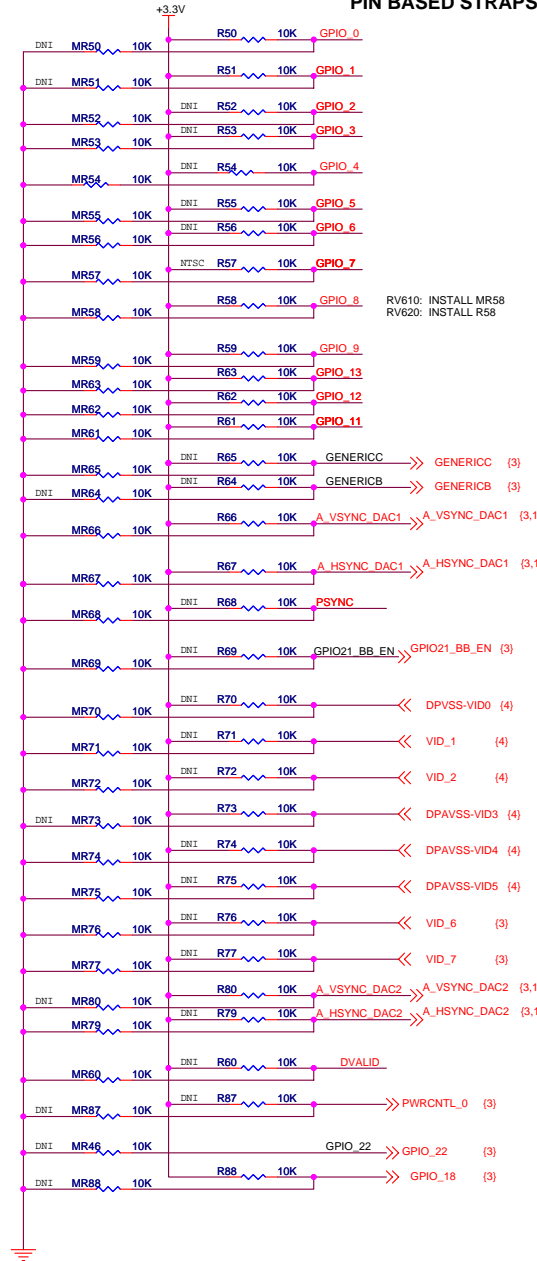
Overlap pads to save space
and to prevent assembly of
both resistors.

Layout



Ground High logic voltage
Signal

PIN BASED STRAPS




GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I 0 - 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	
GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	
GPIO(3,2) - ATI Internal Use Only - Reserved (Default: 00)	
GPIO(4) - DEBUG_ACCESS ATI Internal Use Only - Reserved (Default: 0)	
GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)	
GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)	
GPIO(7) - TV OUT STANDARD (Jumper position overwrite resistor settings) 0 - PAL TVO (Jumper is closed) 1 - NTSC TVO (Jumper is open)	
GPIO(8) - ATI Internal Use Only - Reserved (Default: 0)	
GPIO(9,13:11) - CONFIG(3..0) IF BIOS_ROM_EN=1 (default) (GPIO_22) tmel - AT25F512A (512 kbit) 01010 ST Microelectronics - M25P05A (512 kbit) 0100 M25P10A (1 Mbit) 0101 M25P20 (2 Mbit) 0101 Chingis (formerly PMC) - Pm25LV512 (512 kbit) 0100 Pm25LV010 (1 Mbit) 0101	
If BIOS_ROM_EN = 0, then Config(2:0) defines the primary memory aperture size (Config 3 = don't care). x000 128MB x001 256MB x010 64MB x011 32MB x100 512MB x101 1GB x110 2GB x111 4GB	
GENERICC, GENERICB - ATI Internal Use Only - Reserved (Default: 0)	
VSYNC - VIP_DEVICE_STRAP_EN 0: Slave VIP host port devices present (use if Theater is populated) 1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)	
HSYNC - ATI Internal Use Only - Reserved (Default: 0)	
PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)	
GPIO_21 - ATI Internal Use Only - Reserved (Default: 0)	
VID_0 - ATI Internal Use Only - Reserved (Default: 0)	
VID_1 - MSI_DIS (Default: 0)	
VID_2 - ATI Internal Use Only - Reserved (Default: 0)	
VID_3 - ATI Internal Use Only - Reserved (Default: 0)	
VID_4 - ATI Internal Use Only - Reserved (Default: 0)	
VID_5 - 64BAR_EN_A (Default: 0) Enable 64-bit BARs	
VID_6,7 - ATI Internal Use Only - Reserved (Default: 00)	
VSYNC - DDR2_VENDOR_SELECT ATI Board Feature I (see GPIO_18)	
HSYNC2 - ATI Internal Use Only - Reserved (Default: 0)	
BIF_CLK_PM_EN 0 - Disable CLKREQ# power management capability 1 - Enable CLKREQ# power management capability	
GPIO_15 - FOR FUTURE EXPANSION	
GPIO_22_ROMCSb - Enable external BIOS ROM device (Default 1)	
GPIO_18 - DDR2 MEM VENDOR [V2SYNC.GPIO_18] ATI Board Feature I QUIMONDA [0:0] HYNIX [0:1] SAMSUNG [1:0]	

Pull-Down Resistors are for BU until built-in pull-downs are verified.

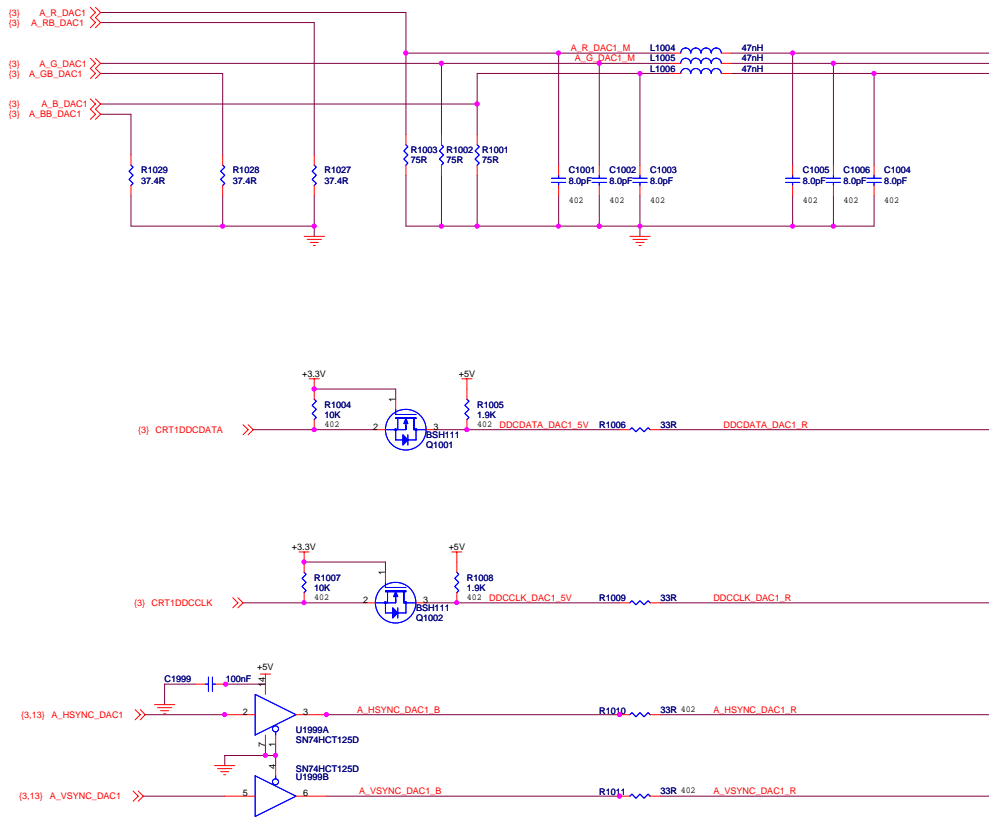
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Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO d11 No. 105-B350xx-00C

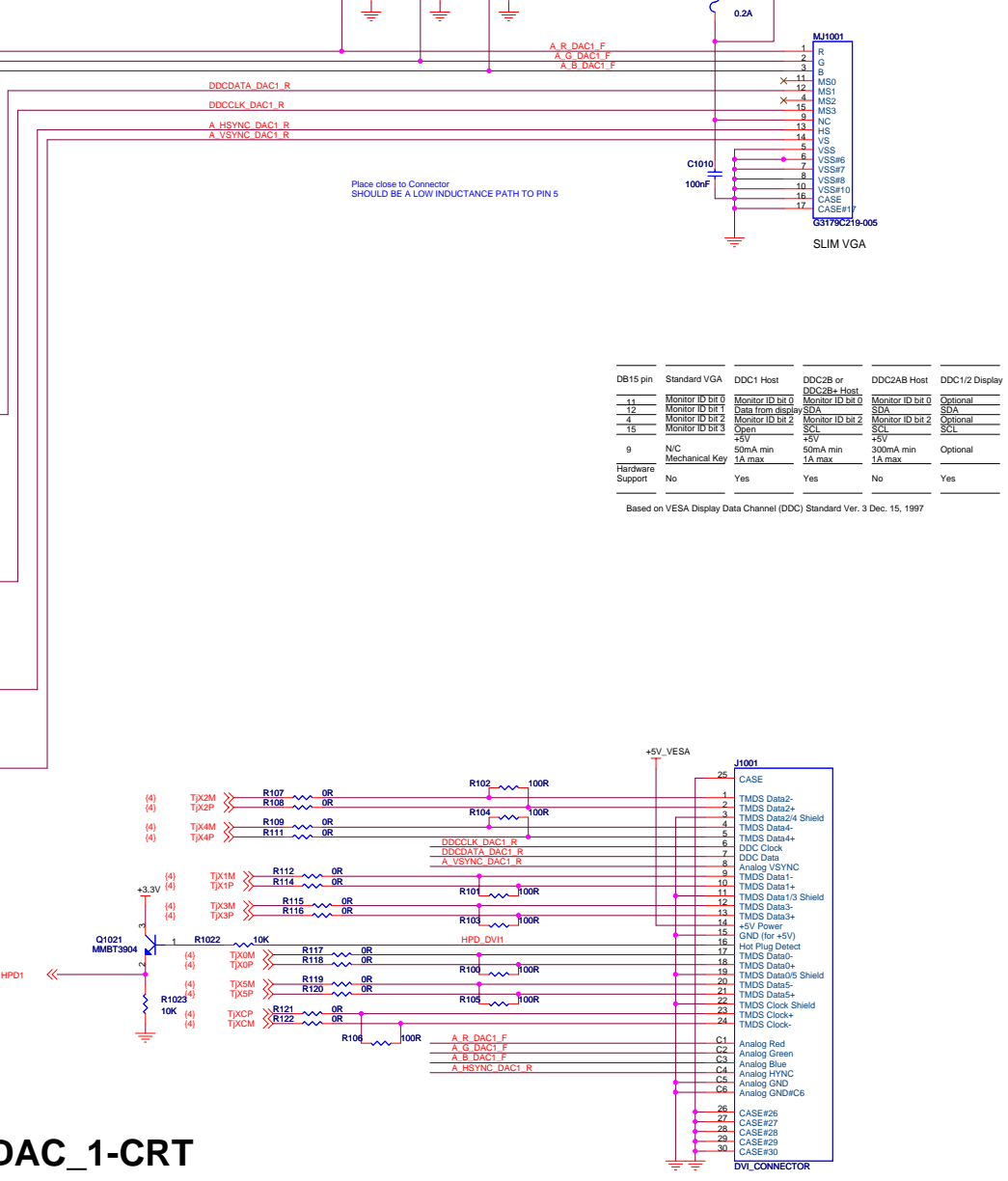
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Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)



SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane



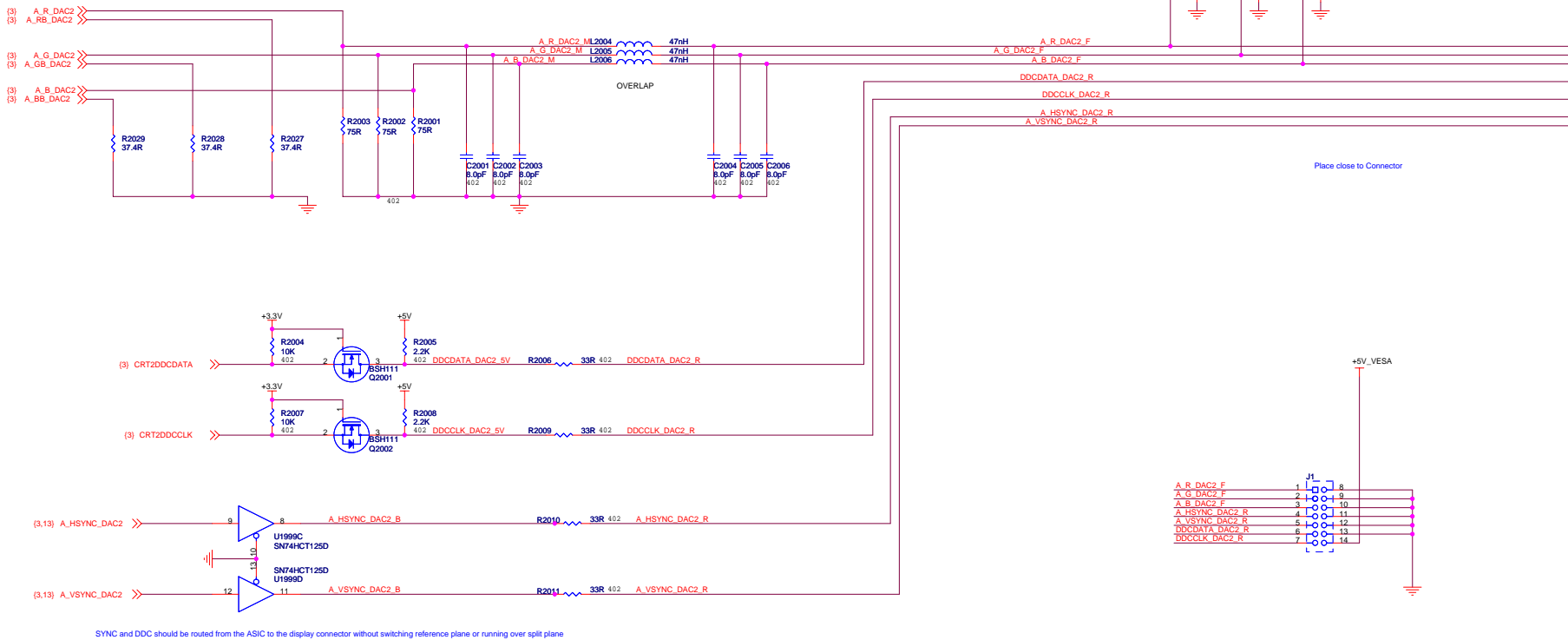
DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B Host	DDC2AB Host	DDC1/2 Display
14	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional	Optional
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional	Optional
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional	Optional
15	Monitor ID bit 3	Open	Open	Optional	Optional
9	N/C	50mA min	50mA min	300mA min	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

TMDS_2(Daul_Link) + DAC_1-CRT



Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane



TMDs_1(Single_Link) + DAC_2-CRT

Component (Y)
Component (Pr)
Component (Pb)

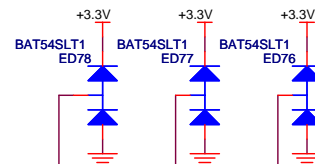
DAC2_Y_F
DAC2_C_F
DAC2_COMP_F
402
DAC2_Y_DIN
DAC2_C_DIN
DAC2_COMP_DIN

(3) GENERICA

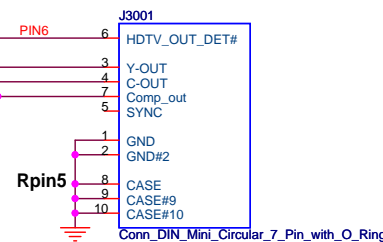
STV/HDTV#_DET

+3.3V
R3008
10K
402

R3009
0R
402




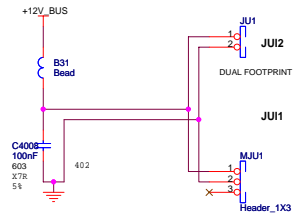
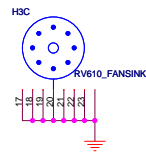
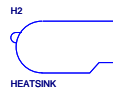
TV Out

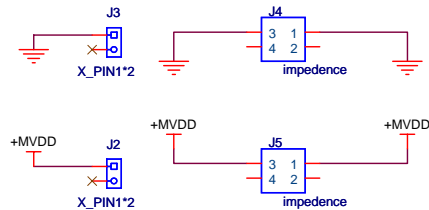
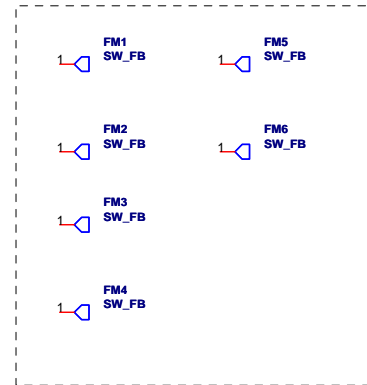
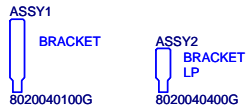


The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dLVT			







Title

RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

Schematic No.

105-B350xx-00C

Date:

Monday, January 28, 2008

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev

17

Sch
RevPCB
Rev

Date

REAL

REVISION DESCRIPTION

01 00A 2007.05.07 START NEW SCHEMATIC. DERIVED FROM B170 (RV610) SCHEMATIC.

02 00A 2007.05.17 p. 4 MR155/R155 FIX SHORT

03 00A 2007.05.17 RM R7, NR7, R5, MB60, MR45, R45, R890, R1248, R1247, R1242, R1243, C853, C863; ADD R2, B890, MR890, C846; CHANGE R1022, R1023;

04 00A 2007.05.22 REMOVE GND_TXVSSR, GND_PVSS; AG23 NOW NC - WAS SCHEM MISTAKE; ADD R858 FOR BUO; R858 CHANGE TO 1210;

05 00A 2007.05.24 CTF: ADD Q1252, R1254, R1255, R1256, R1258, Q1253, Q1254, CHANGE U1250 TO SINGLE FF; UPDATE BLOCK DIAGRAM.

06 00A 2007.05.25 LVTM: ADD R110, RM R109, MR109, R108, R107;

07 00A 2007.05.28 LVTM: ADD C118, RM C104; REMOVE MR85, MR86 FOR SIMPLIFICATION;

08 00A 2007.05.28 XTALIN/OUT: LAYOUT EASEMENT; REMOVE MR108 (R849 ALREADY THERE); LVTM: ADD C119 (LOWER COST OPTION); POWER SUPPLY: REMOVE R706, MR707, R606 & MR607;

09 00A 2007.05.29 REMOVAL OF +5V: ADD R861, MR861, R862, REG861, R869, R863, R867; REMOVE MU830, U830, C830. R833, R834, C831, R832, MR832, R831, MR831; CONNECT DDC TO 5V_VESA;

010 00A 2007.05.30 CHNG C858 TO 3.3VBUS; CONNECTION TO R845 CHNG; ADD R870, MR870, C867;

011 00A 2007.05.30 REMOVE R4033; REMOVE B201-204; ADD R30-33 [PLACE NEAR ASIC]; REMOVE R3004, R3005;

012 00A 2007.05.31 REMOVE C164-C166, C170, C172 PER SIMULATION RESULTS - THESE CAPS DO NOT IMPROVE DECOUPLING. RM TP860 (LAYOUT CONSTRAINTS. ALREADY ICT TP ON THAT NET);

013 00A 2007.05.31 RM R154-R157, MR154-157 -> FUNCTIONALITY TAKEN BY EXISTING STRAPS. LAYOUT USE PLACE OF M/R154-7; ADD R7; RM MR706, MR606, B889, R863; ADD D861;

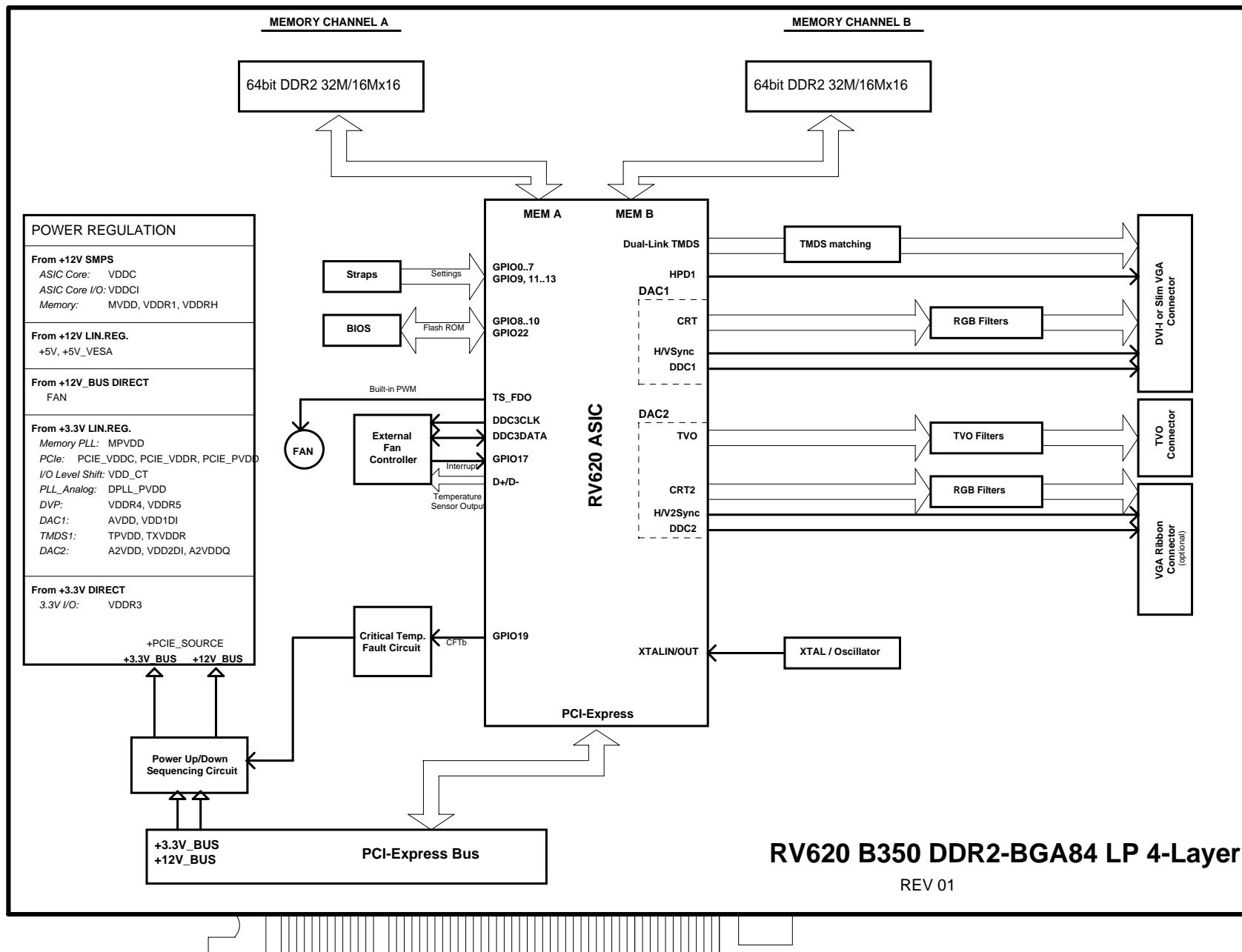
014 00A 2007.05.32 ADD SOCKET SK1

015 00A 2007.06.1 SK? CORRECTED TO SK1.

016 00B 2007.06.25 NO NETLIST CHANGES; - MOUNTING HOLES CHANGED TO 3.175mm;

017 00C 2007.10.01

- p. 1 - CONNECT B7 TO GND (SEE PA RV6XX H1)
- REMOVE R2. IT IS ALWAYS POPULATED, NO NEED TO ZERO OHM. THIS BOARD DOES NOT SUPPORT JTAG DEBUG;
- p. 11 - REMOVE R839. THIS CIRCUIT IS VERIFIED, THERE IS NO NEED TO BE ABLE TO DISCONNECT IT;
- p. 12 - REMOVE R870 - THIS OPTION NOT USED, VCNTRL MUST BE HIGHER THAN +3.3V;
- MR870 REMOVED - ALWAYS POPULATED, DO NOT NEED ZERO OHM RESISTOR OPTION;
- REMOVE R860 - WAS BRING UP ONLY OPTION;
- p. 17 - REPLACED FAN CIRCUIT WITH ONE THAT HAS FEEDBACK:
- ADD R4033, R4031, R4019, R4034, R4006, R4035, Q4004, R4035, Q40002. R4009, R4011, Q4003, R4012, R4013;



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