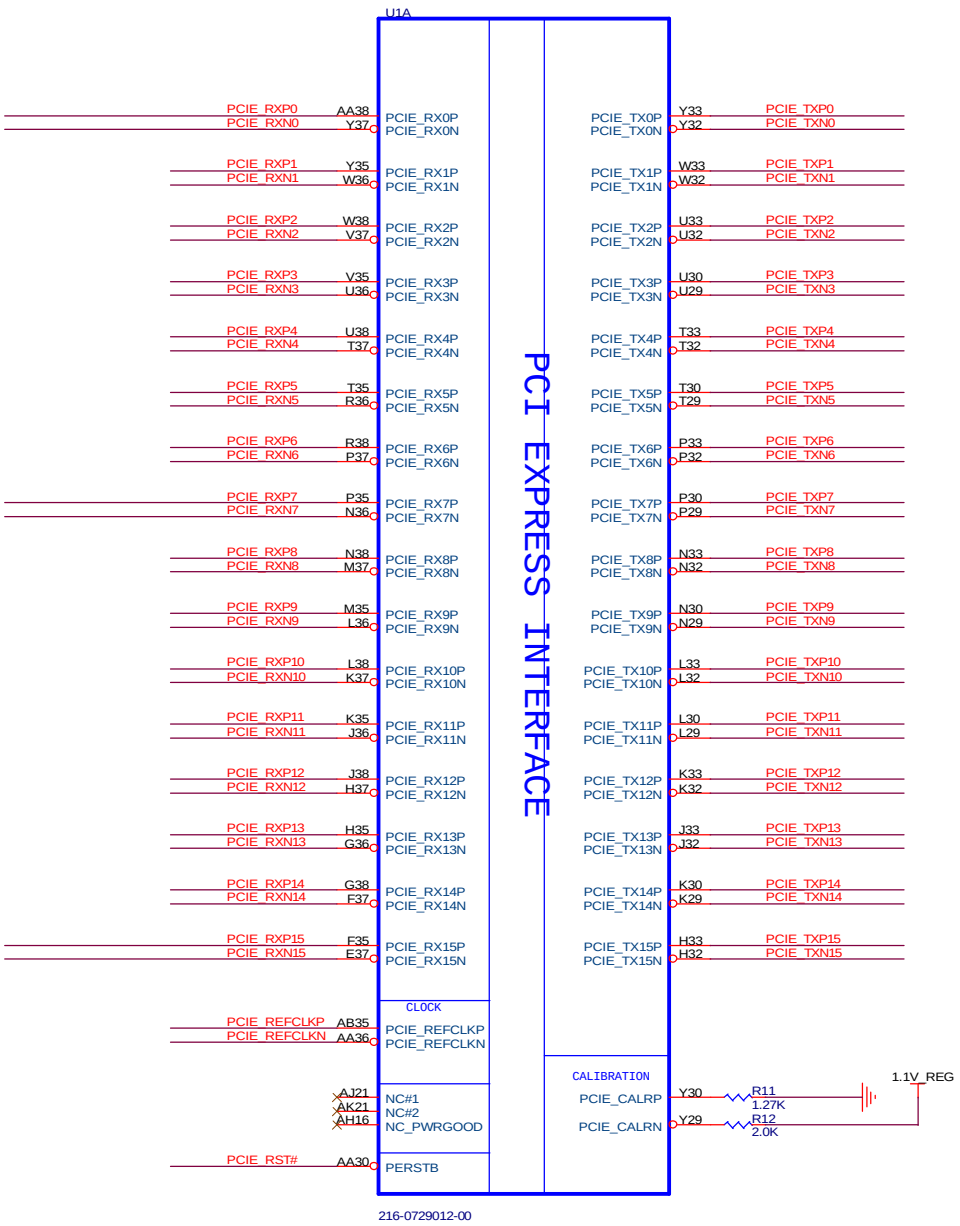

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M8X GDDR3

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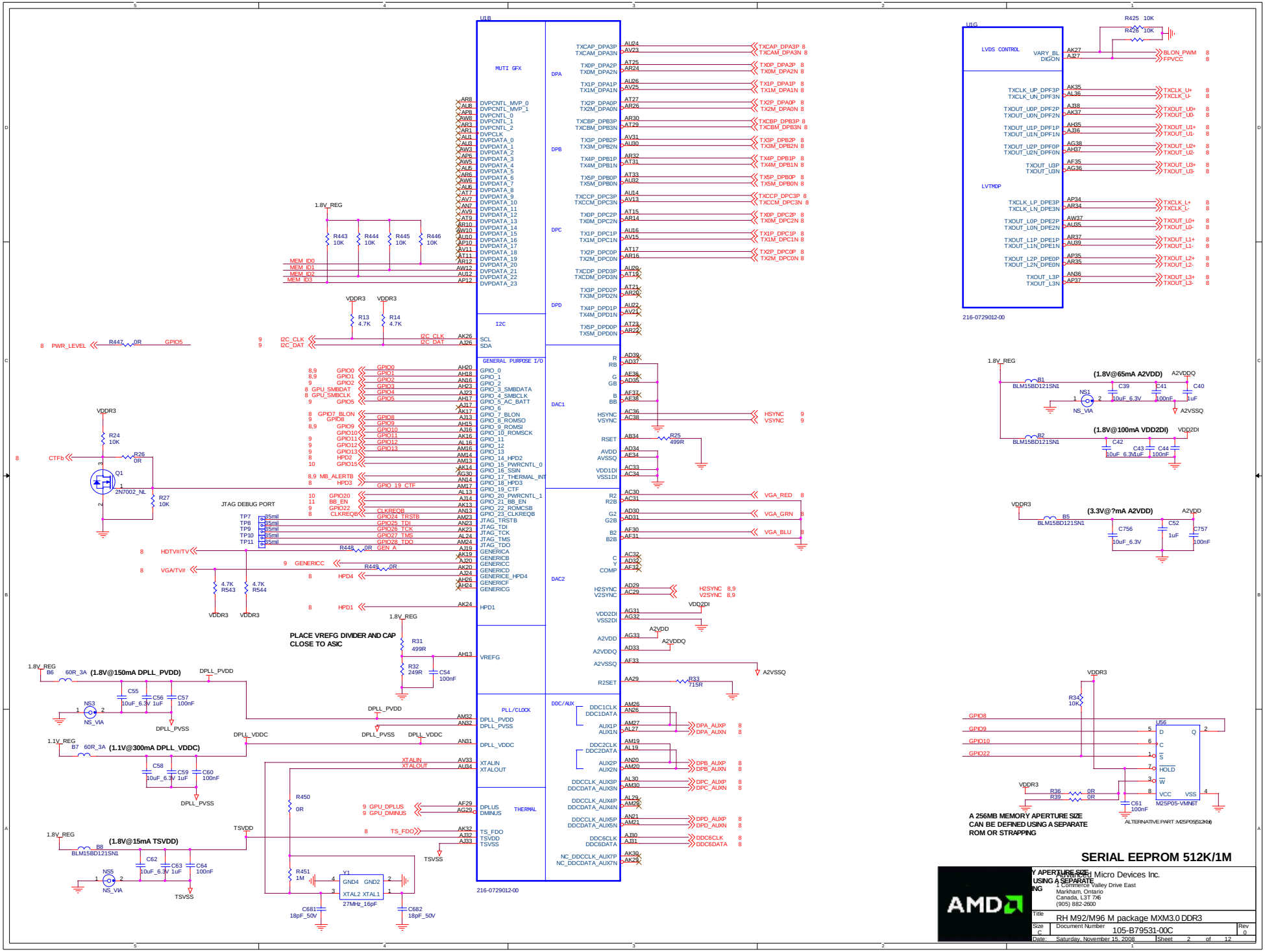
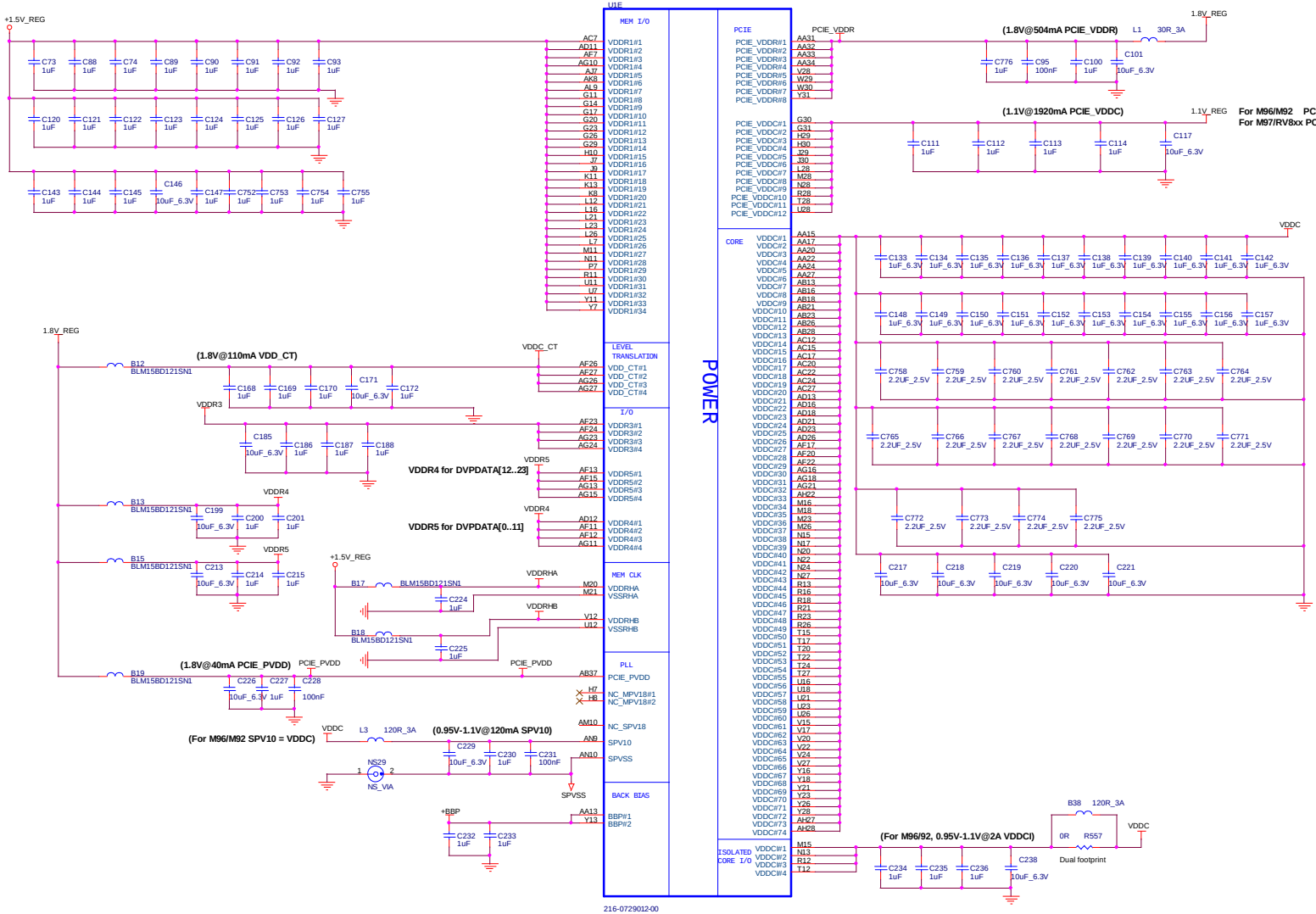
Title RH M92/M96 M package MXM3.0 DDR3

Doc No. 105-B79531-00C





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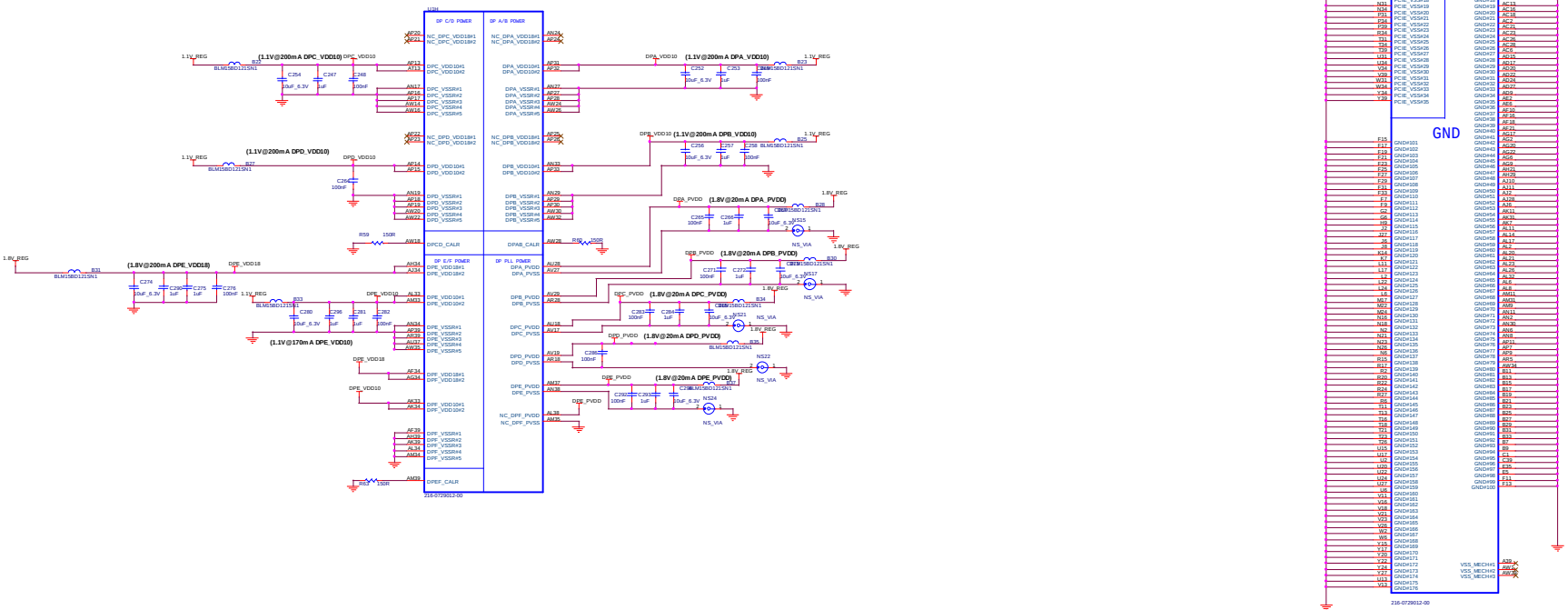
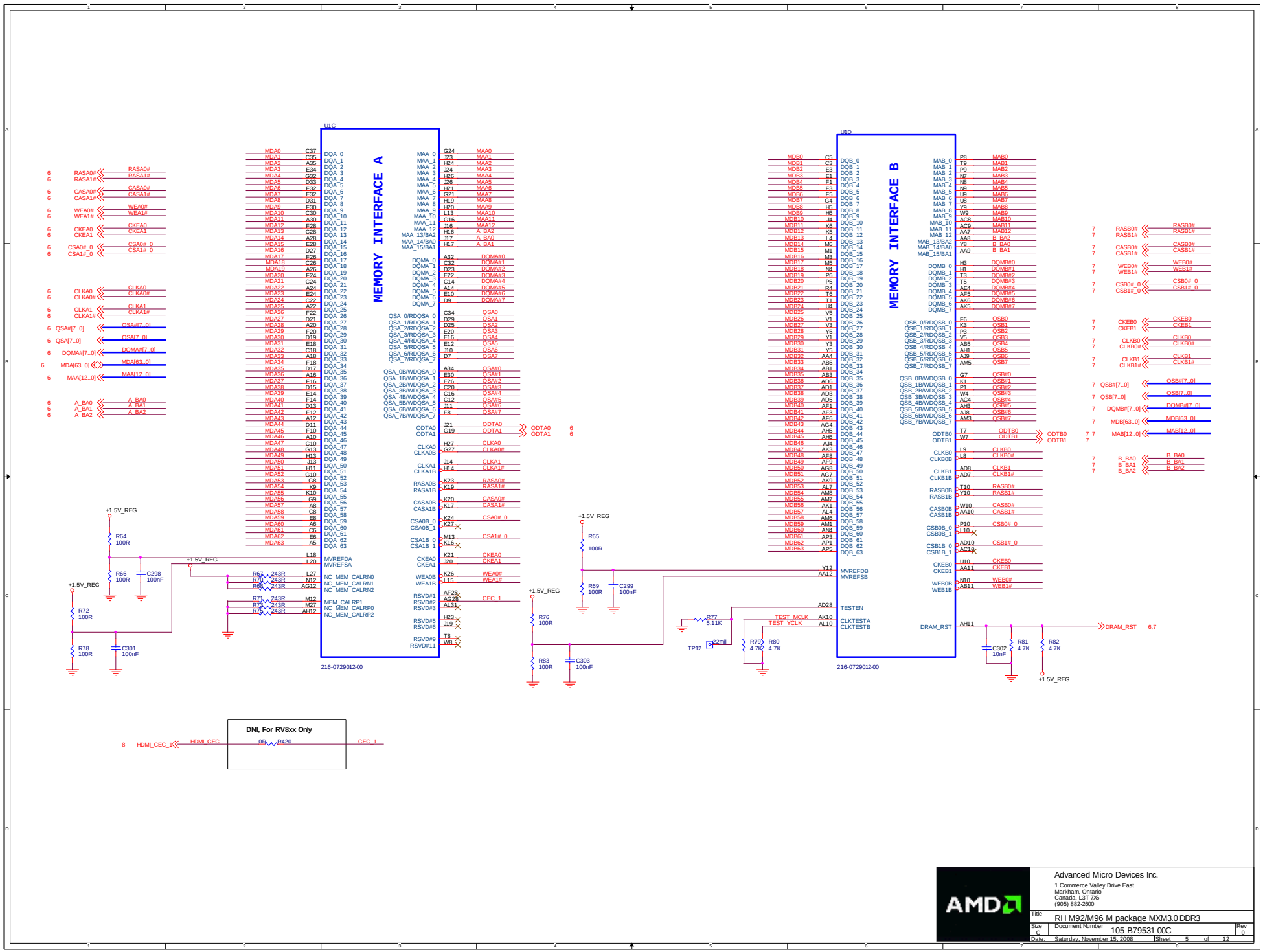
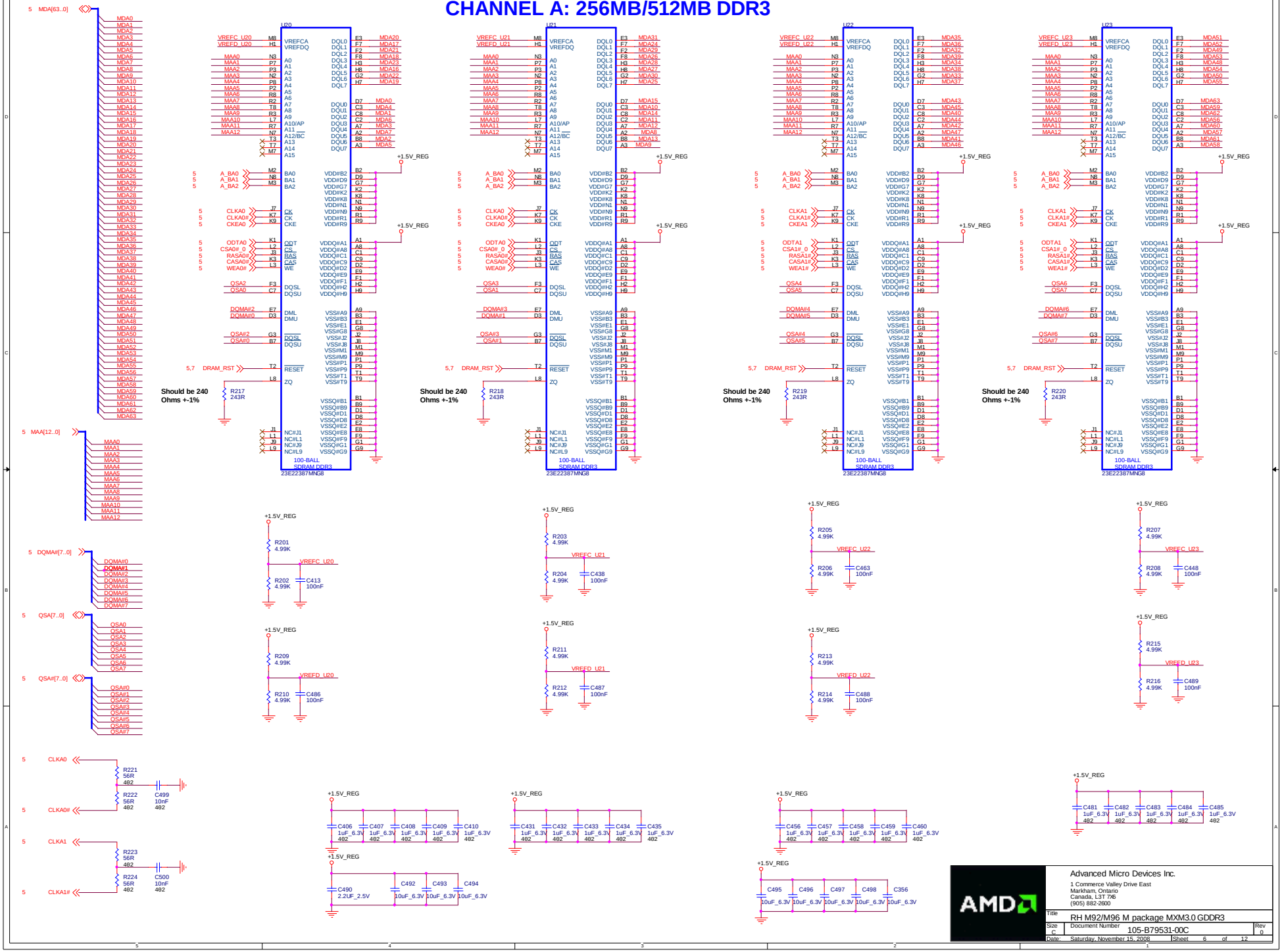
Title: RH M92/M96 M package MXM3.0 DDR3
Size: C | Document Number: 105-B79531-00C | Rev: 0
Date: Saturday, November 15, 2008 | Sheet 3 of 12





CHANNEL A: 256MB/512MB DDR3



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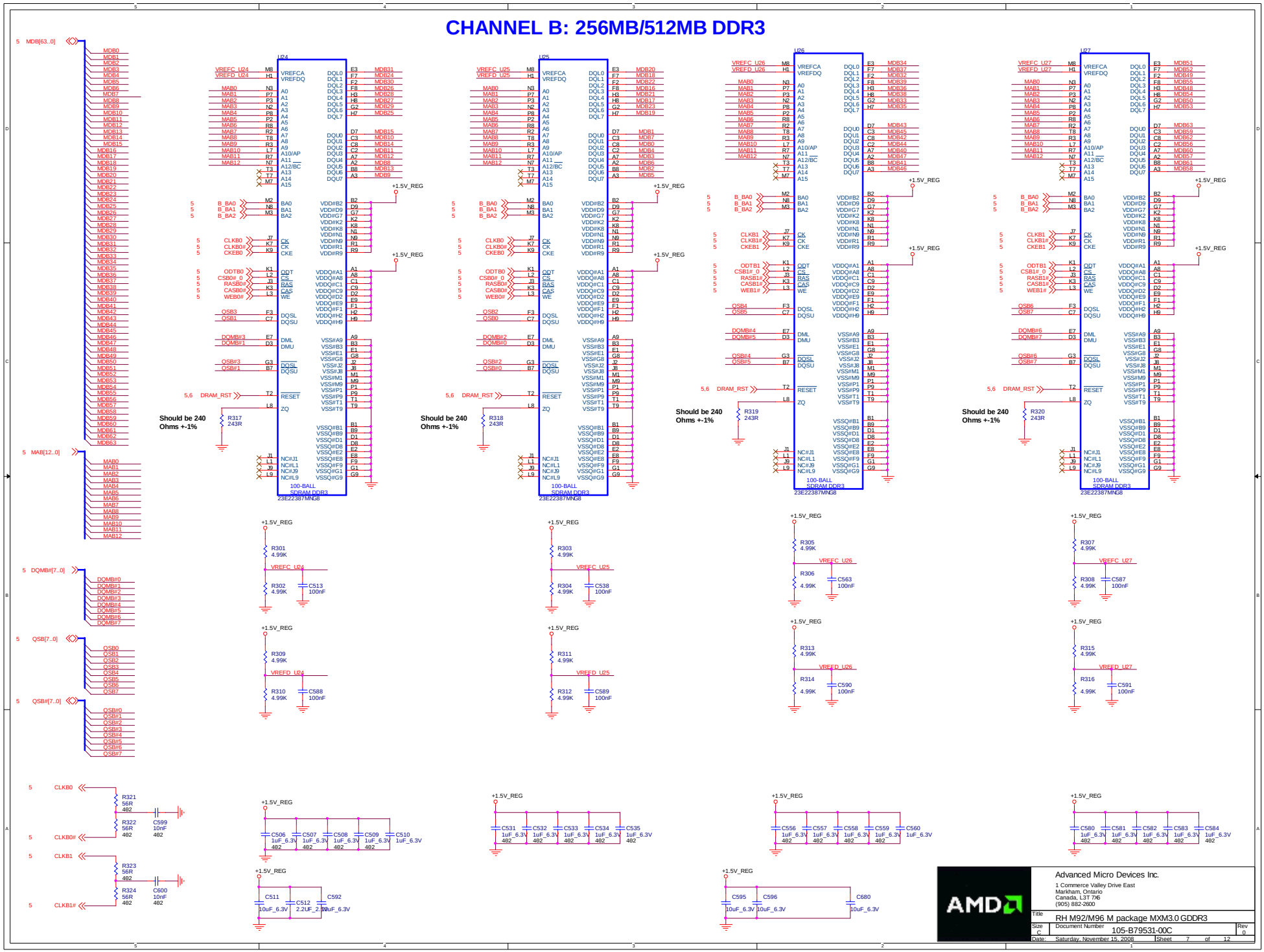
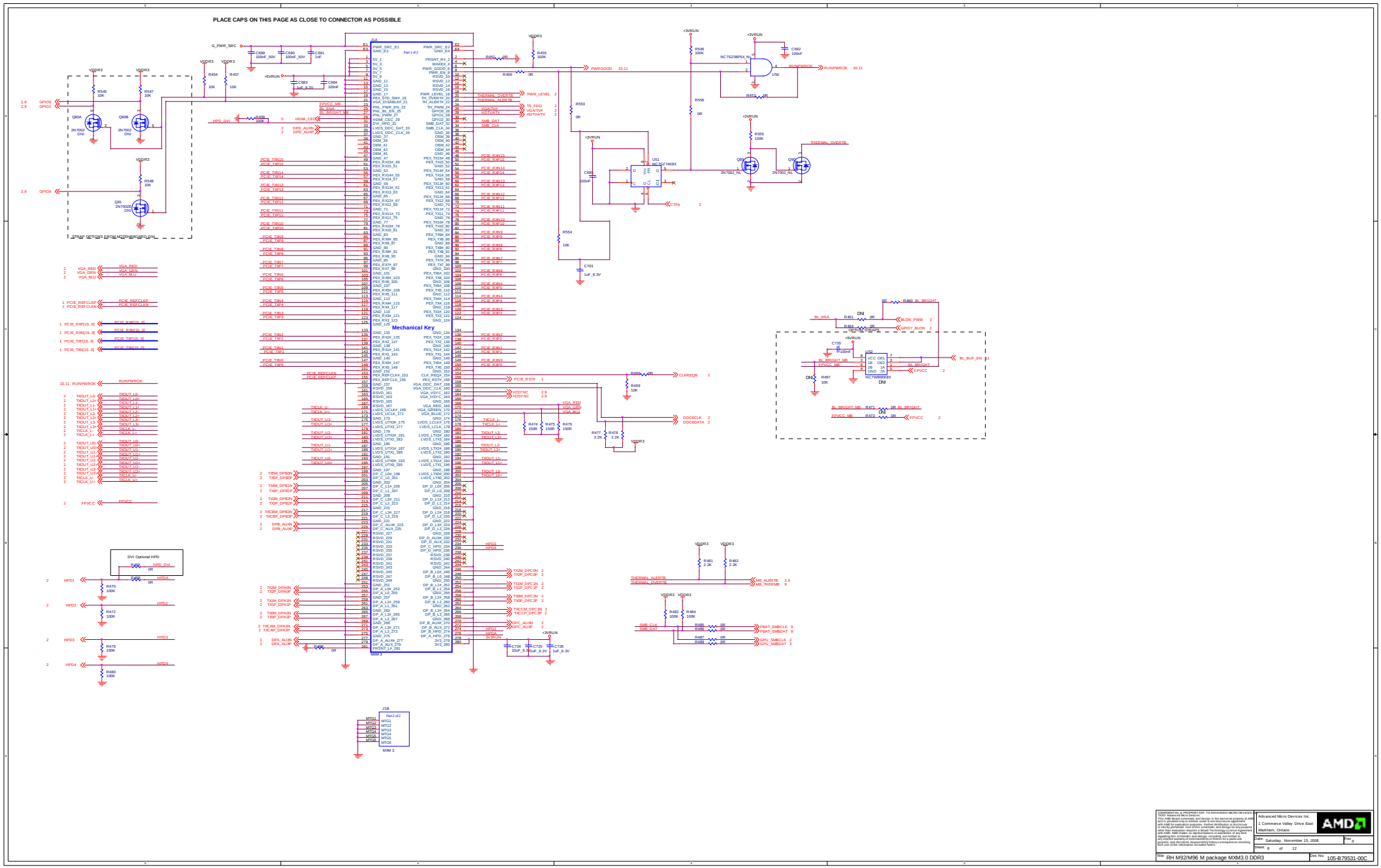
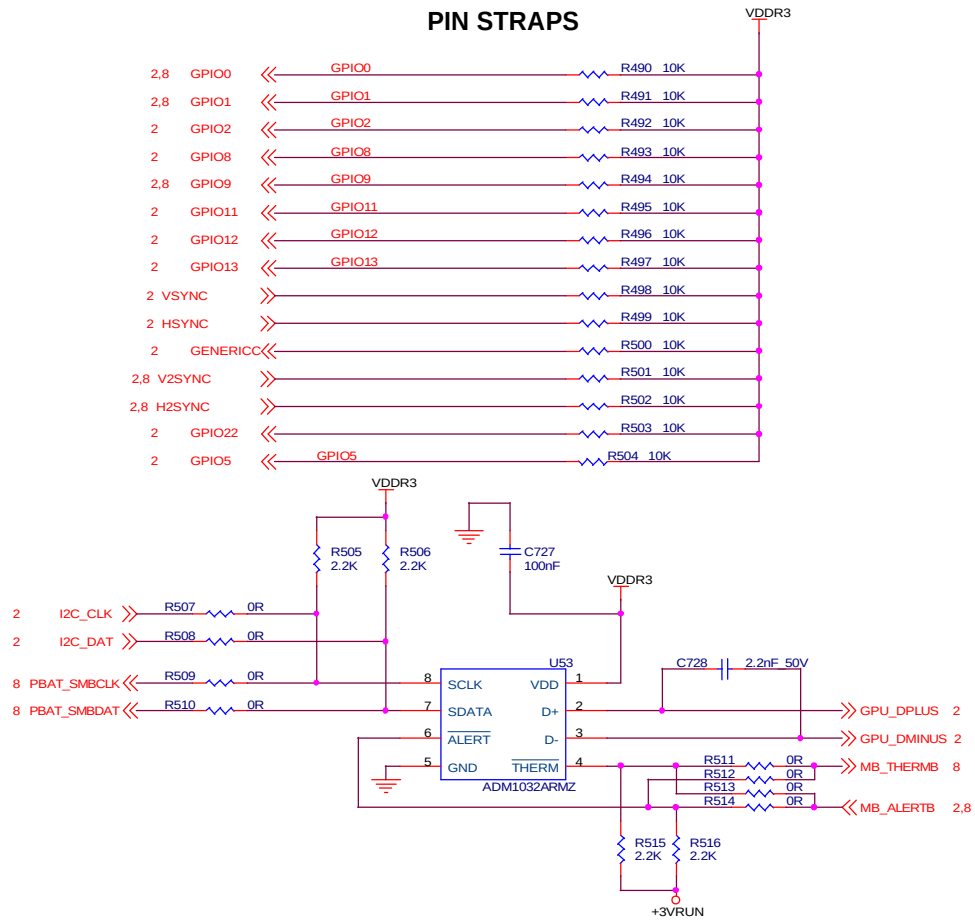
Title	RH M92/M96 M package MXM3.0 GDDR3	
Size: C	Document Number: 105-B79531-00C	Rev: 0
Date: Saturday, November 15, 2008	Sheet 6 of 12	







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSYNC	Audio functiuon present	1

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN

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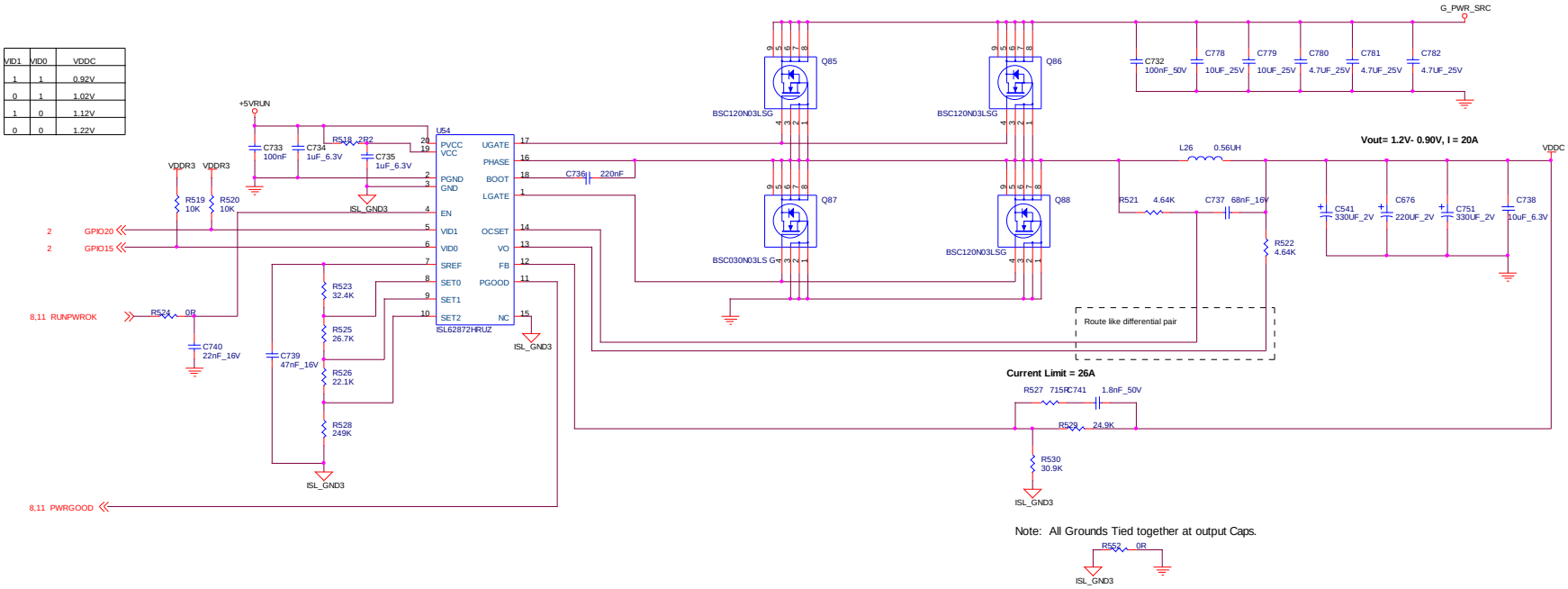
Title RH M92/M96 M package MXM3.0 DDR3 Doc No. 105-B79531-00C

VDDC REGULATOR 1.2V-0.9V @ 20A

VID1	VID0	VDDC
1	1	0.92V
0	1	1.02V
1	0	1.12V
0	0	1.22V



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Date: Saturday, November 15, 2008 Rev 1

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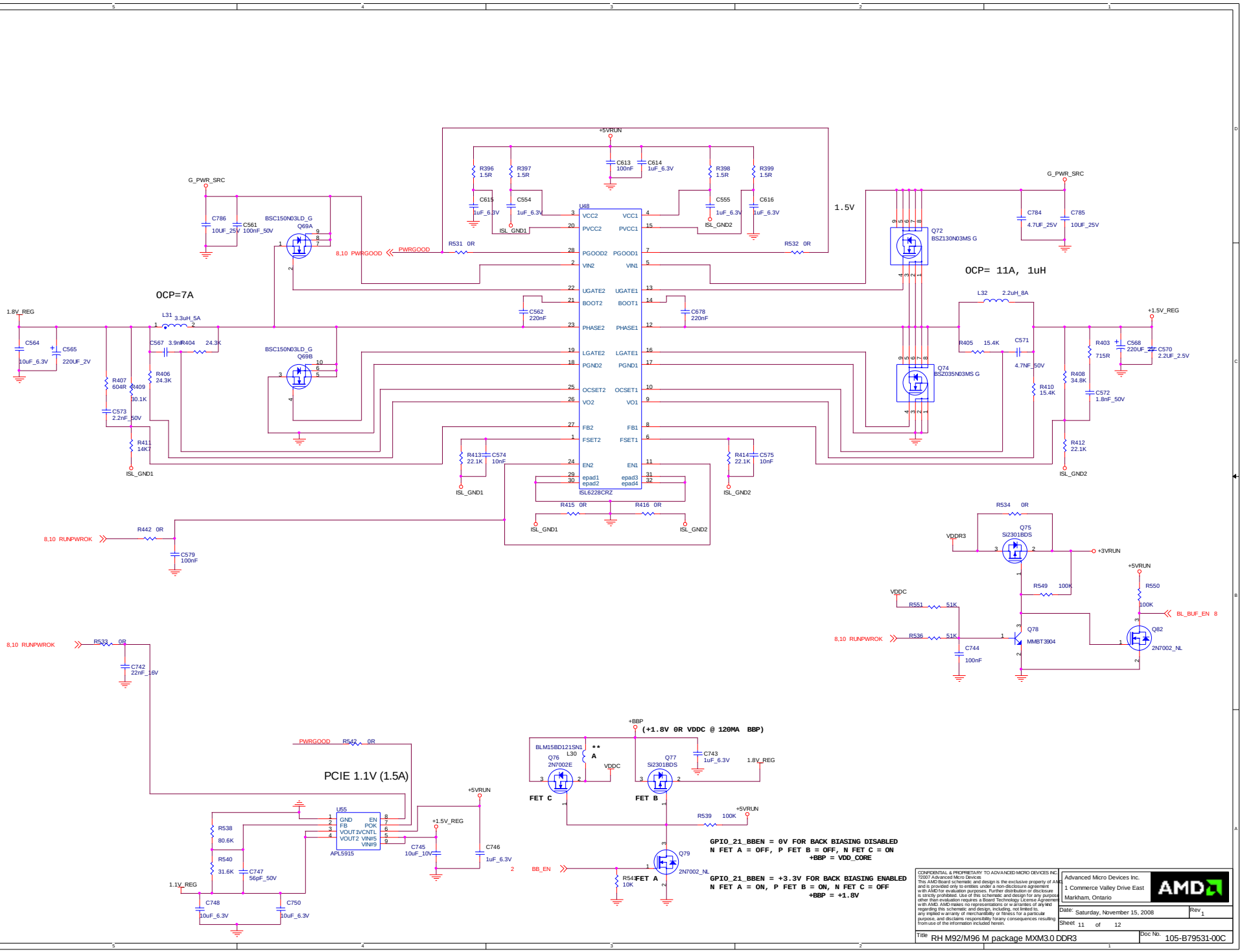
Title: RH M92/M96 M package MXM3.0 DDR3

Doc No. 105-B79531-00C



Title	Schematic No.	Date:
RH M92/M96 M package MXM3.0 DDR3	105-B79531-00C	**Saturday, November 15, 2008**

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00B	21/10/08	On base B795 rev.A
1	00C	06/11/08	