PG611 A00

12GB GDDR5X, 384b, 256Mx32
TALL DVI-D + DP + DP + HDMI/DP + DP

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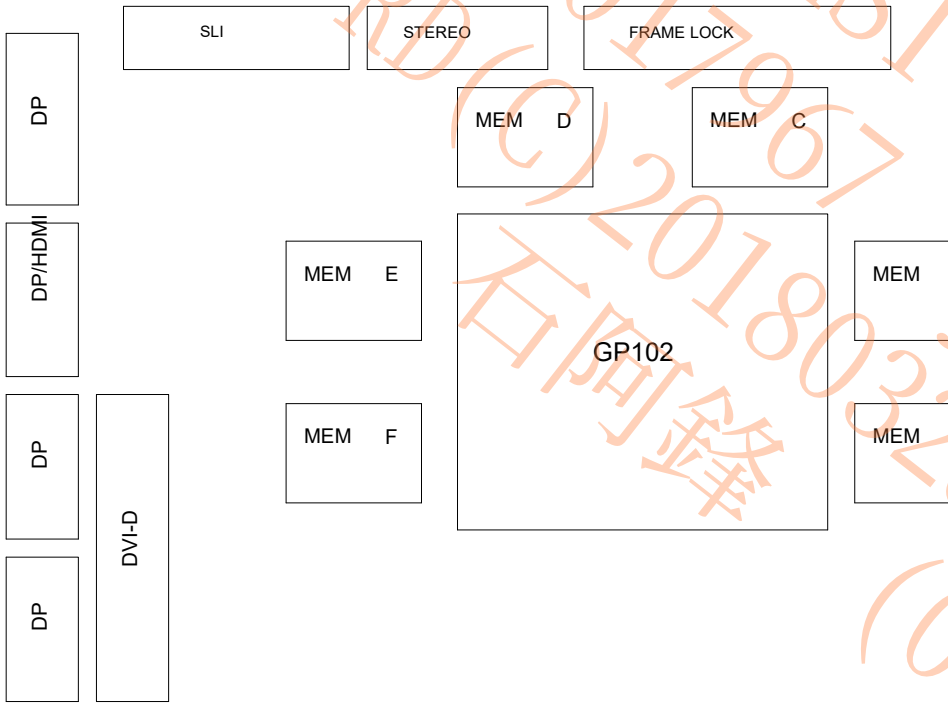

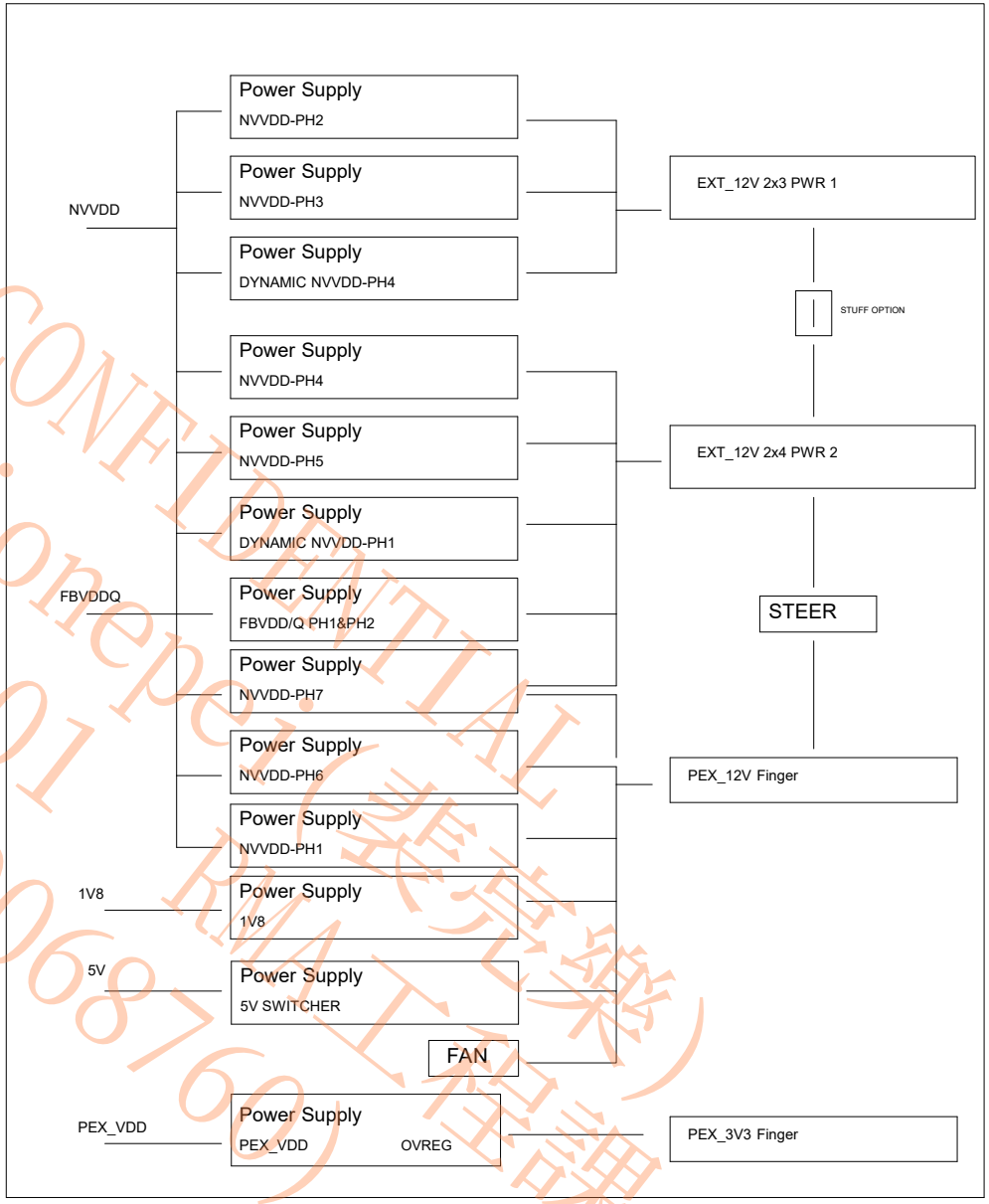

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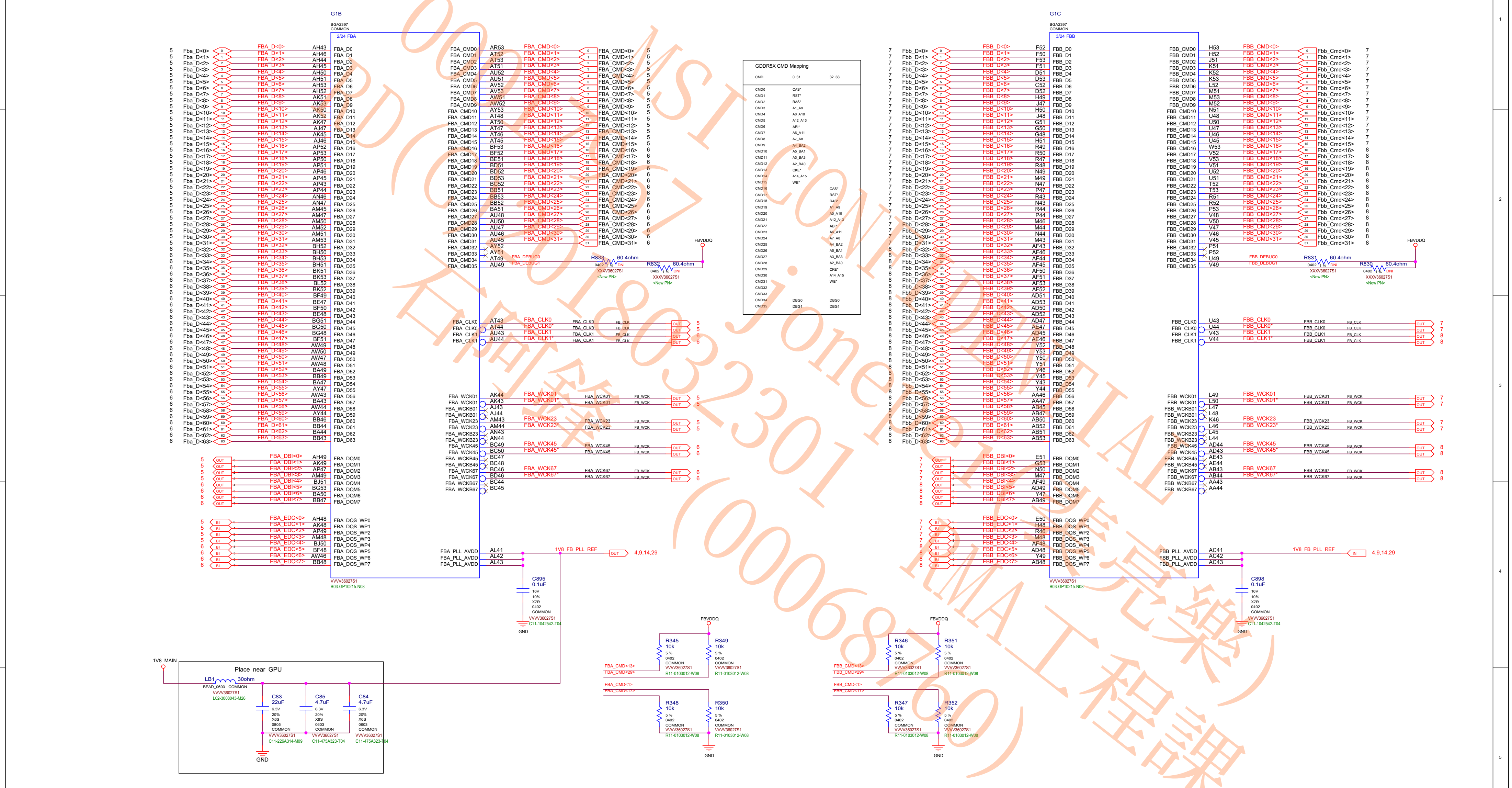
Page3: PCI Express

Page4: MEMORY: GPU Partition A/B



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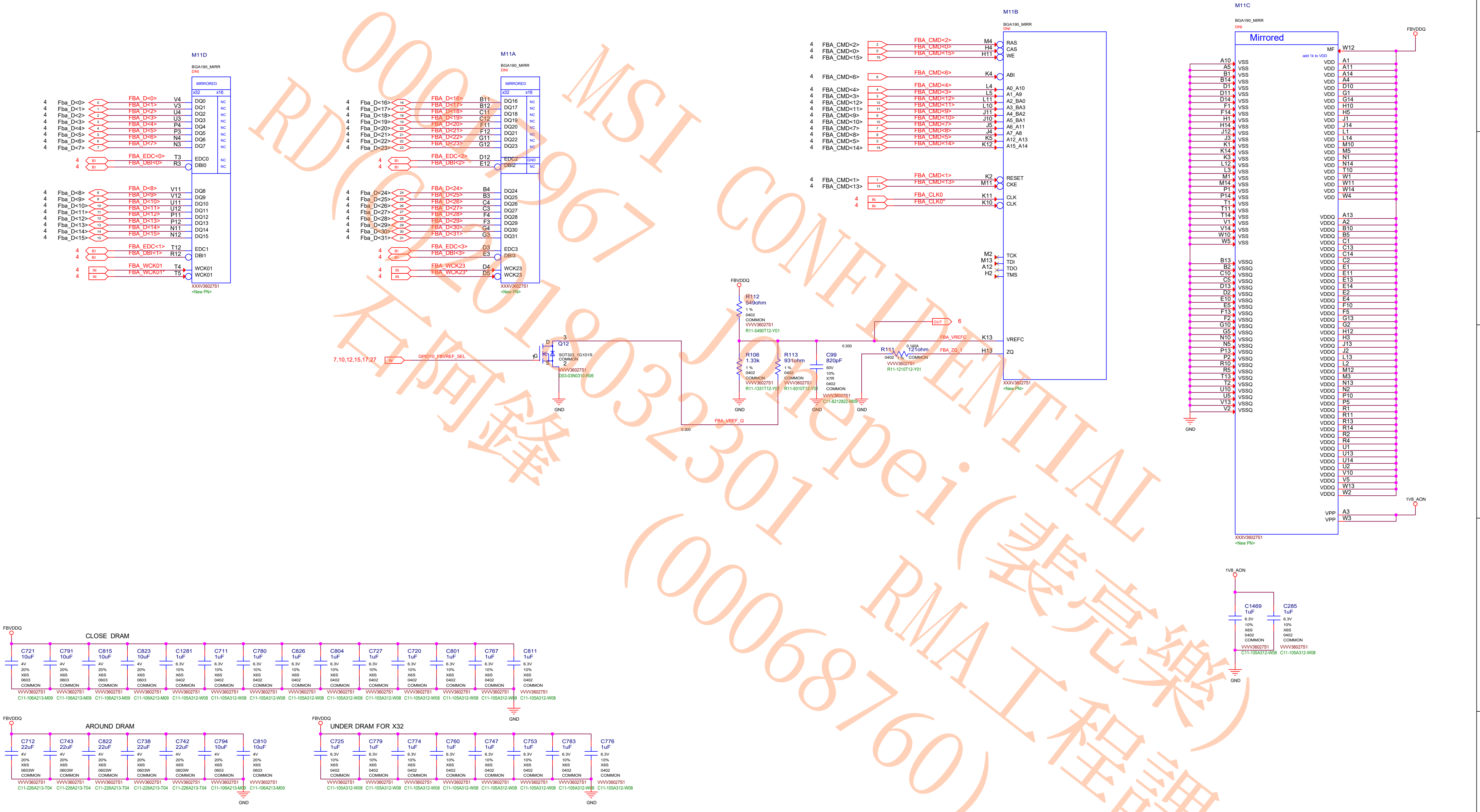

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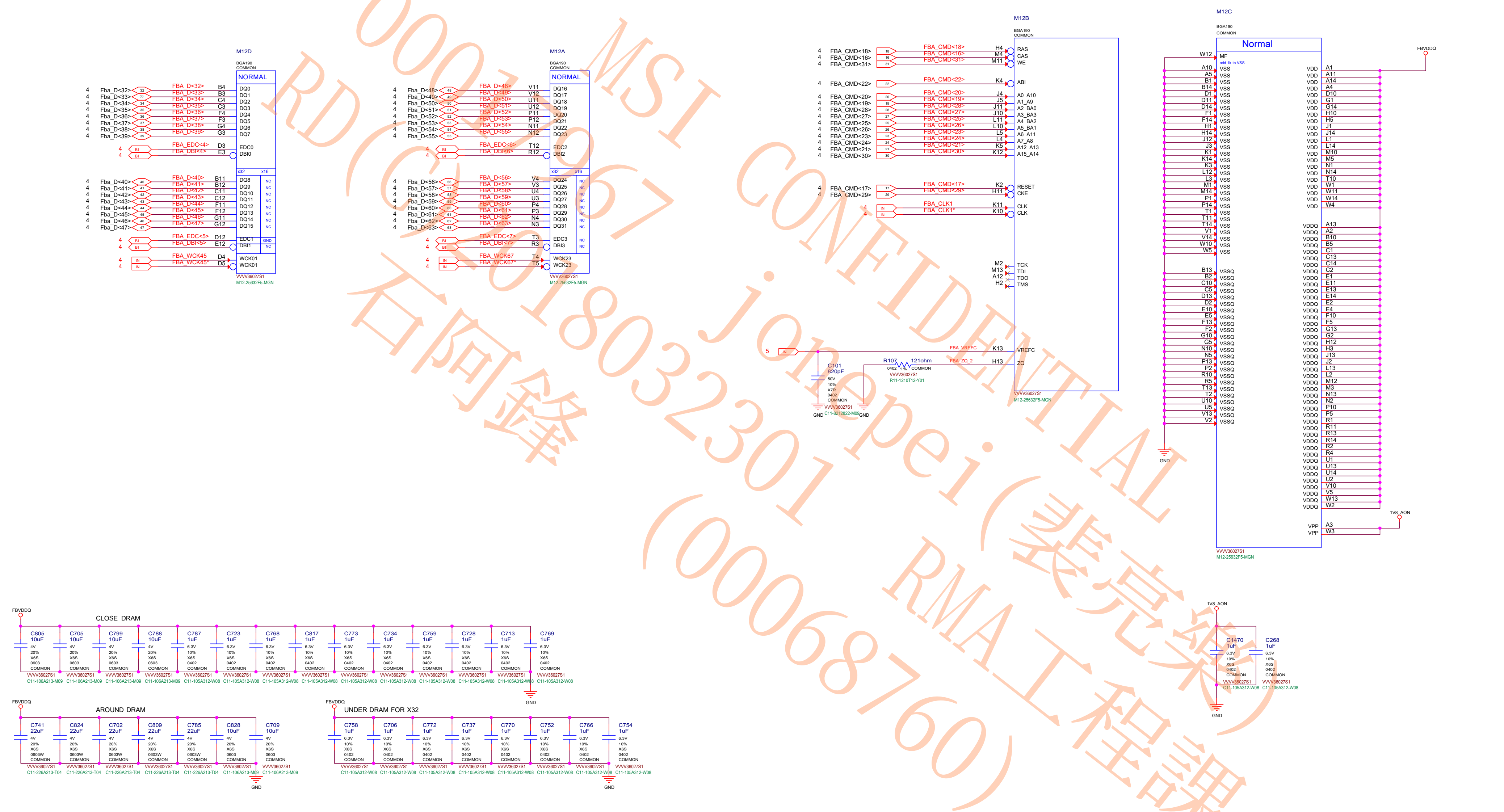
Page6: MEMORY: FBA Partition 63..32



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BGA190 COMMON
NORMAL
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
EDC0 DBI0
DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
EDC1 DBI1
WCK01 WCK01
M12-25632F5-MGN
M12A
BGA190 COMMON
NORMAL
DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23
EDC2 DBI2
DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31
EDC3 DBI3
WCK23 WCK23
M12-25632F5-MGN
M12B
BGA190 COMMON
RAS CAS WE
ABI
A0_A10 A1_A9 A2_BA0 A3_BA3 A4_BA2 A5_BA1 A6_A11 A7_A8 A12_A13 A15_A14
RESET CKE
CLK CLK
TCK TDI TDO TMS
VREFC
ZQ
FBA_VREFC
FBA_ZQ_2
C101 820pF
R107 121ohm
M12-25632F5-MGN
M12C
BGA190 COMMON
Normal
MF
VSS
VSSQ
VDD
VDDQ
VPP
FBVDDQ
1V8_AON
GND
M12-25632F5-MGN
CLOSE DRAM
AROUND DRAM
UNDER DRAM FOR X32
FBVDDQ
C805 10uF
C705 10uF
C799 10uF
C788 10uF
C787 1uF
C723 1uF
C768 1uF
C817 1uF
C773 1uF
C734 1uF
C759 1uF
C728 1uF
C713 1uF
C769 1uF
C741 22uF
C824 22uF
C702 22uF
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C766 1uF
C754 1uF
C1470 1uF
C268 1uF

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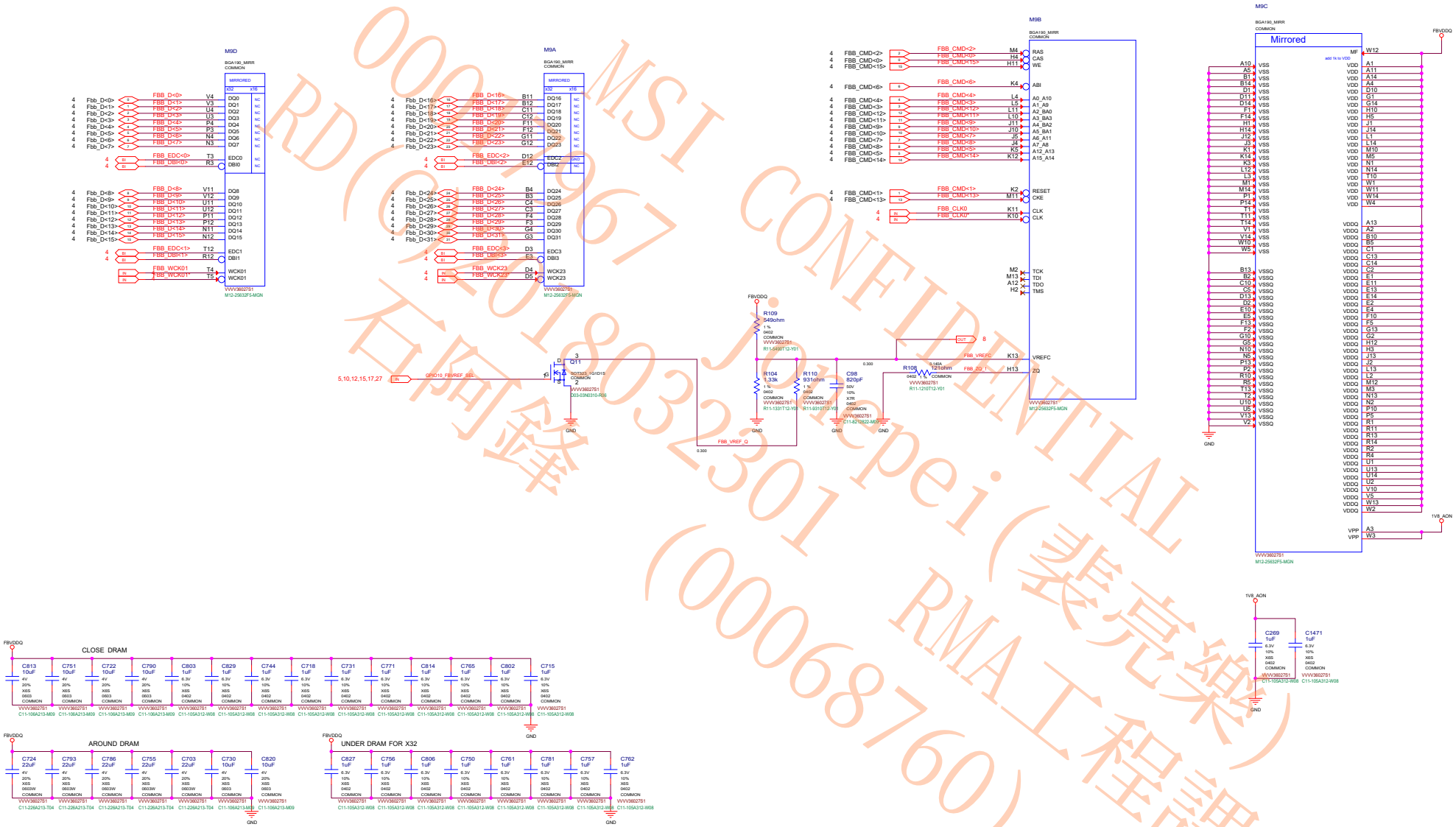

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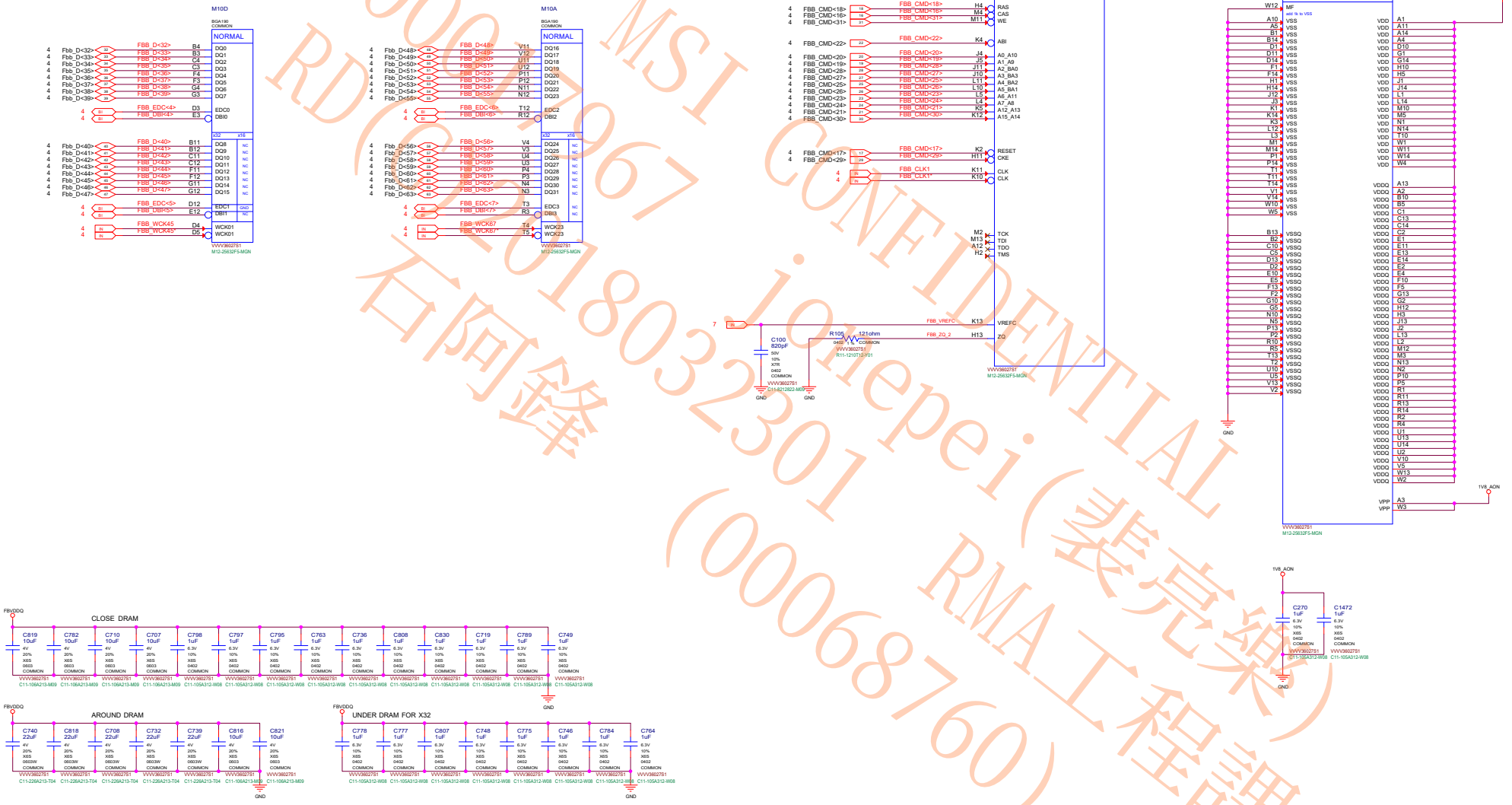

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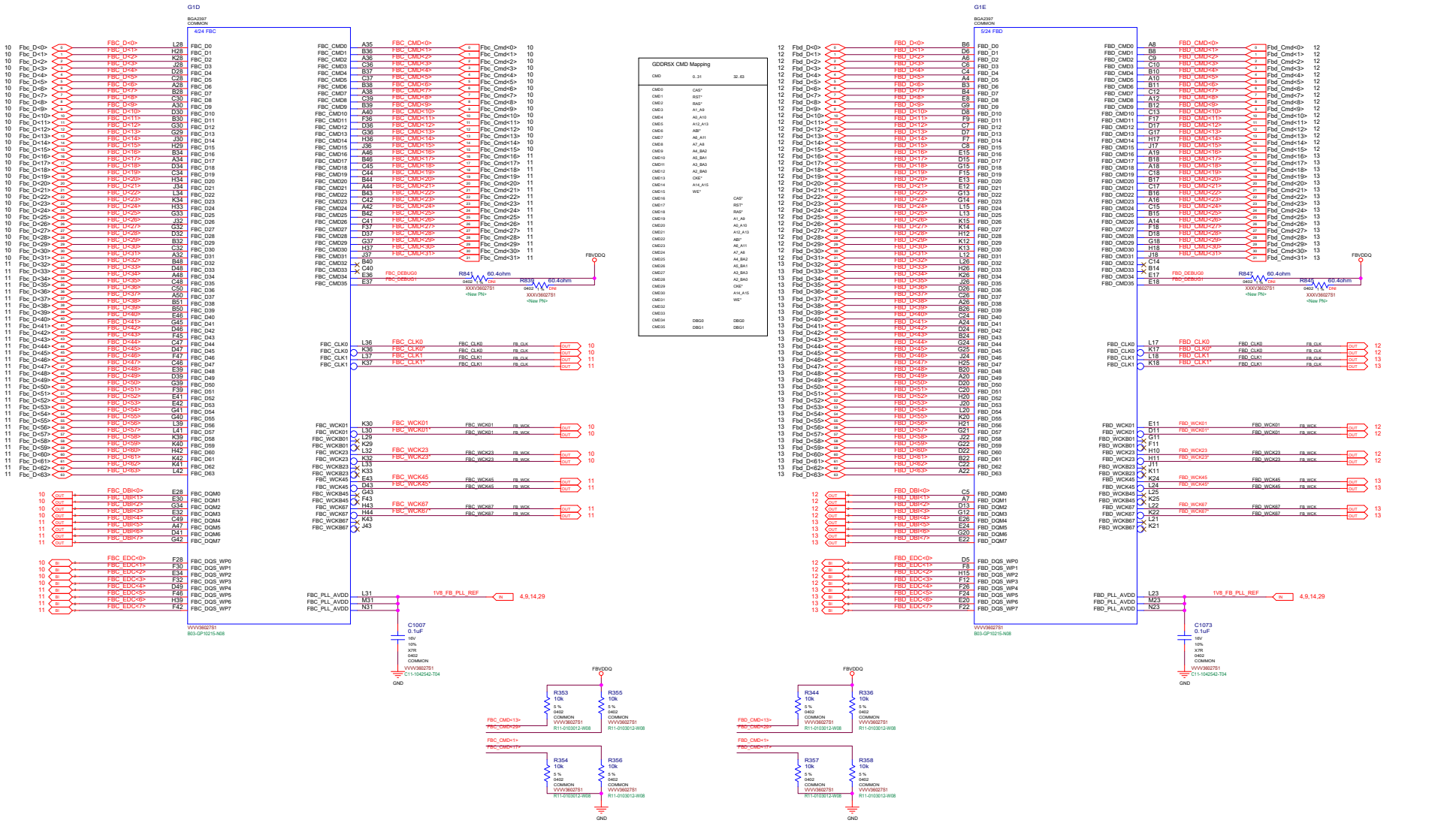
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BGA2307
COMMON
4/24 FBC
WVV3602781
BI3-GP102I5-N08
G1E
BGA2307
COMMON
5/24 FBD
WVV3602781
BI3-GP102I5-N08
GDDR5X CMD Mapping
FBVDDQ
GND
1V8_FB_PLL_REF
4,9,14,29
C1007
0.1uF
C1073
0.1uF
C11-1042542-T04
R353
R355
R354
R356
R344
R336
R357
R358
10k
R11-0103012-W08

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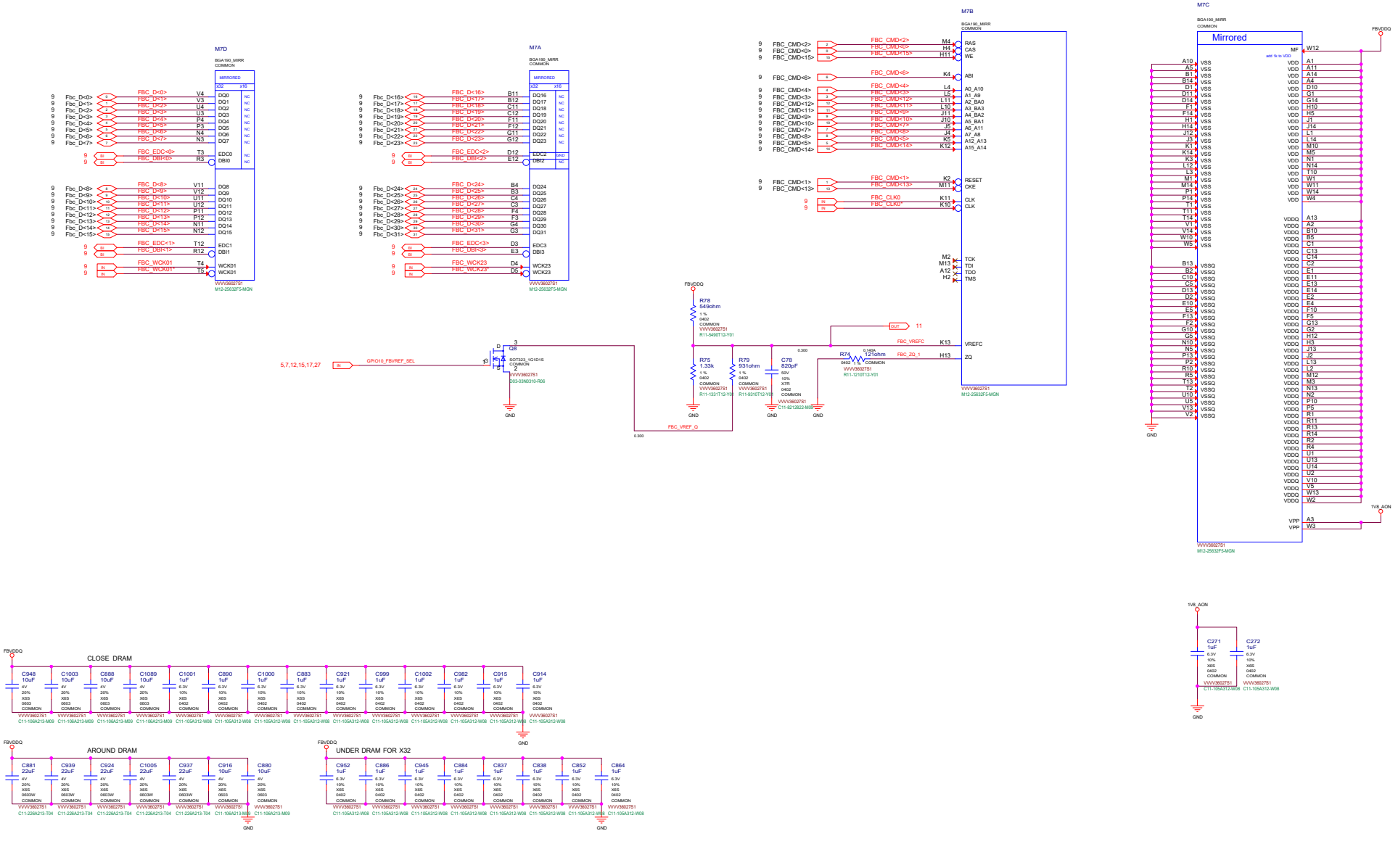

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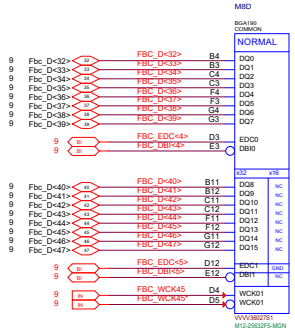

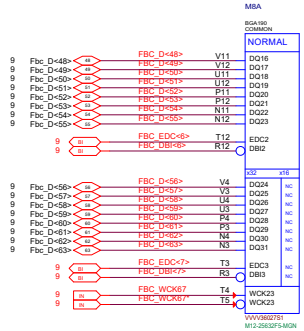

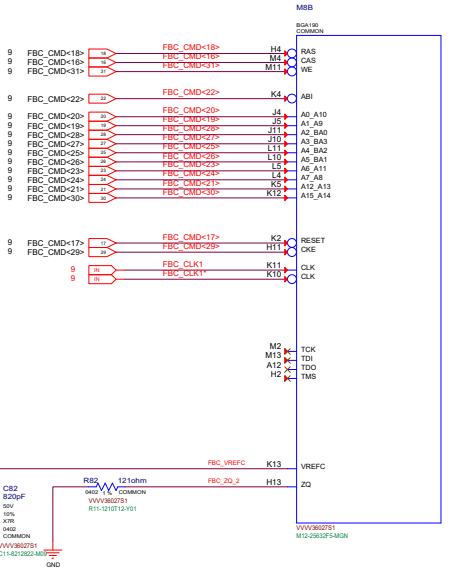

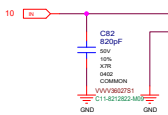

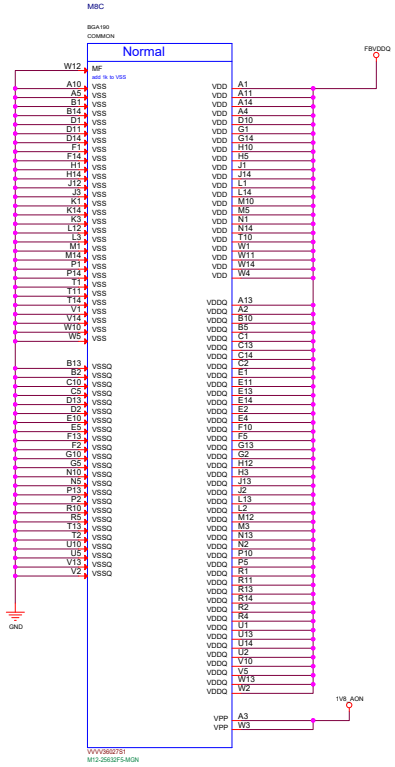

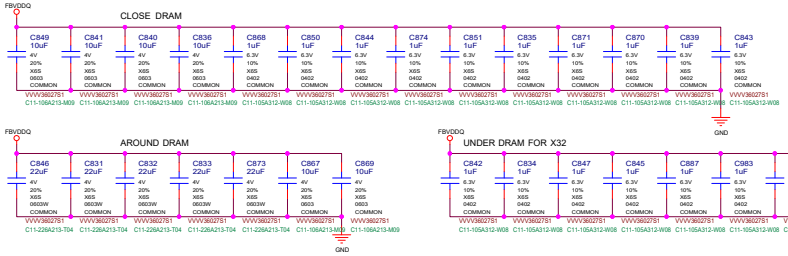

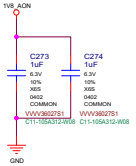

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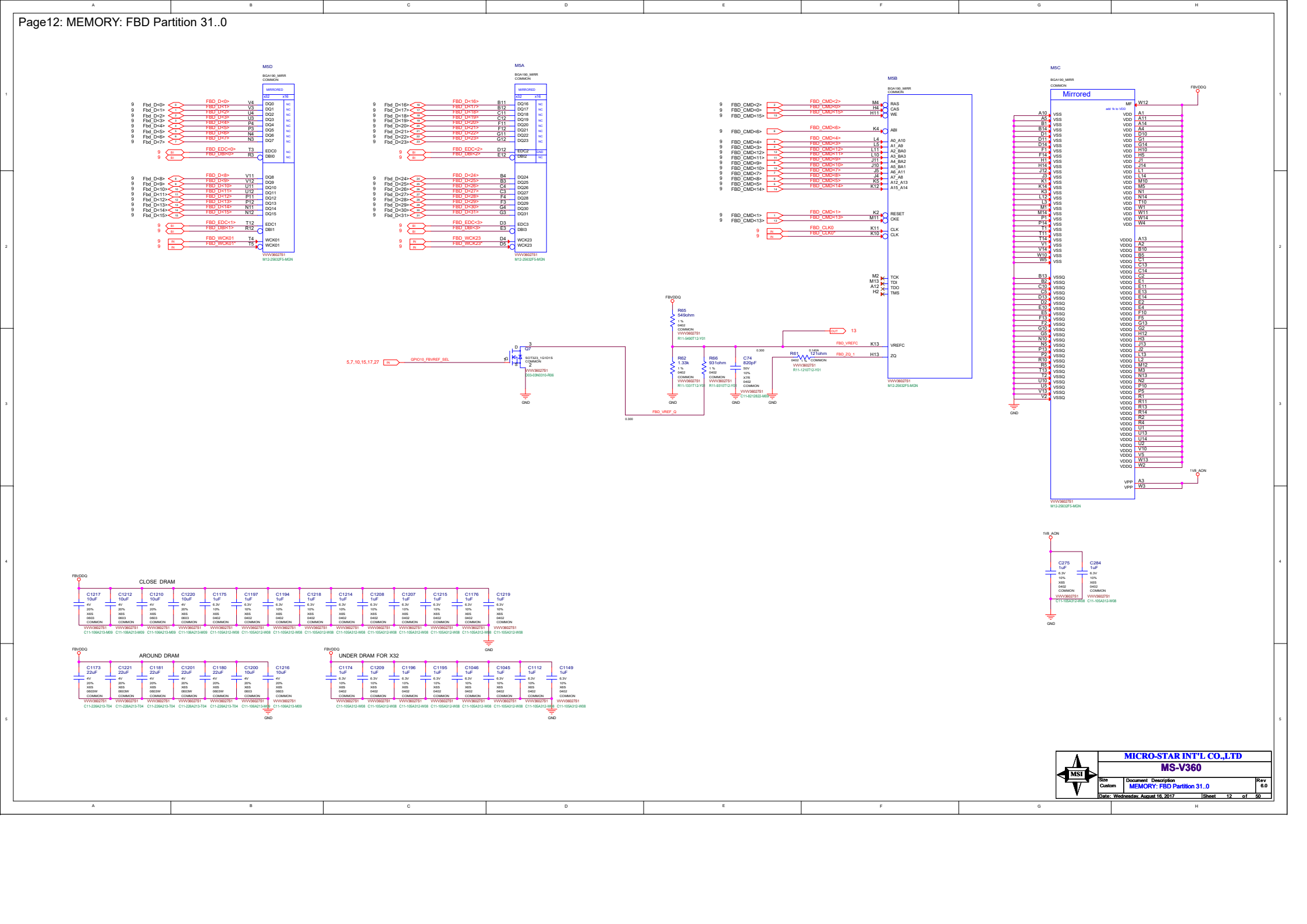

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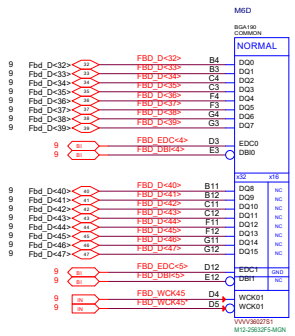

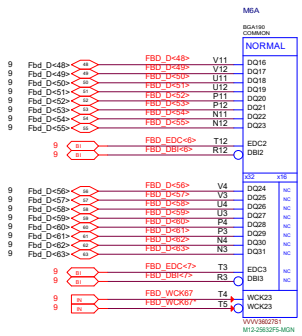

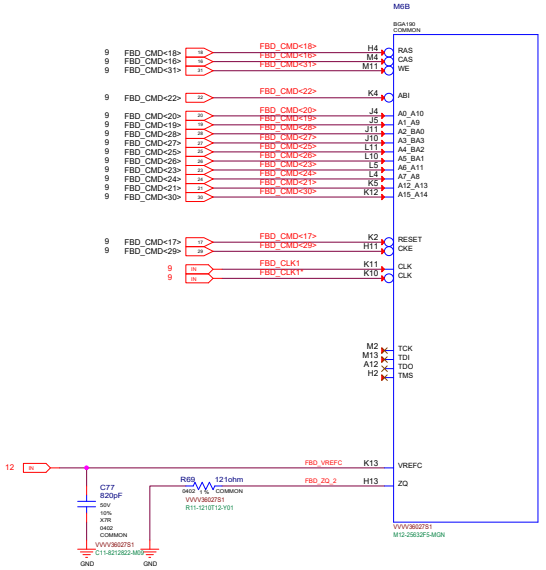

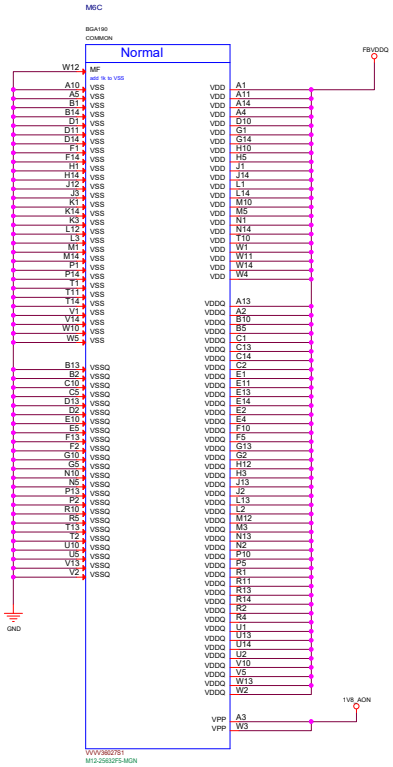

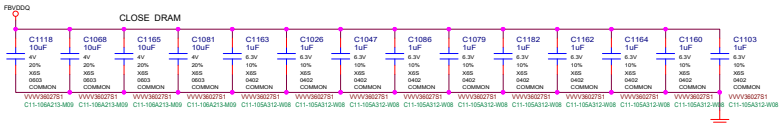

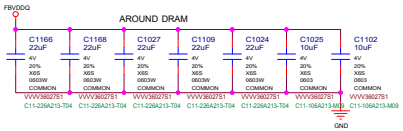

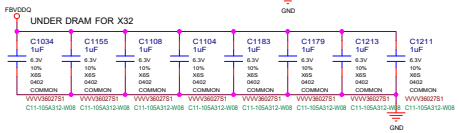

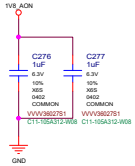

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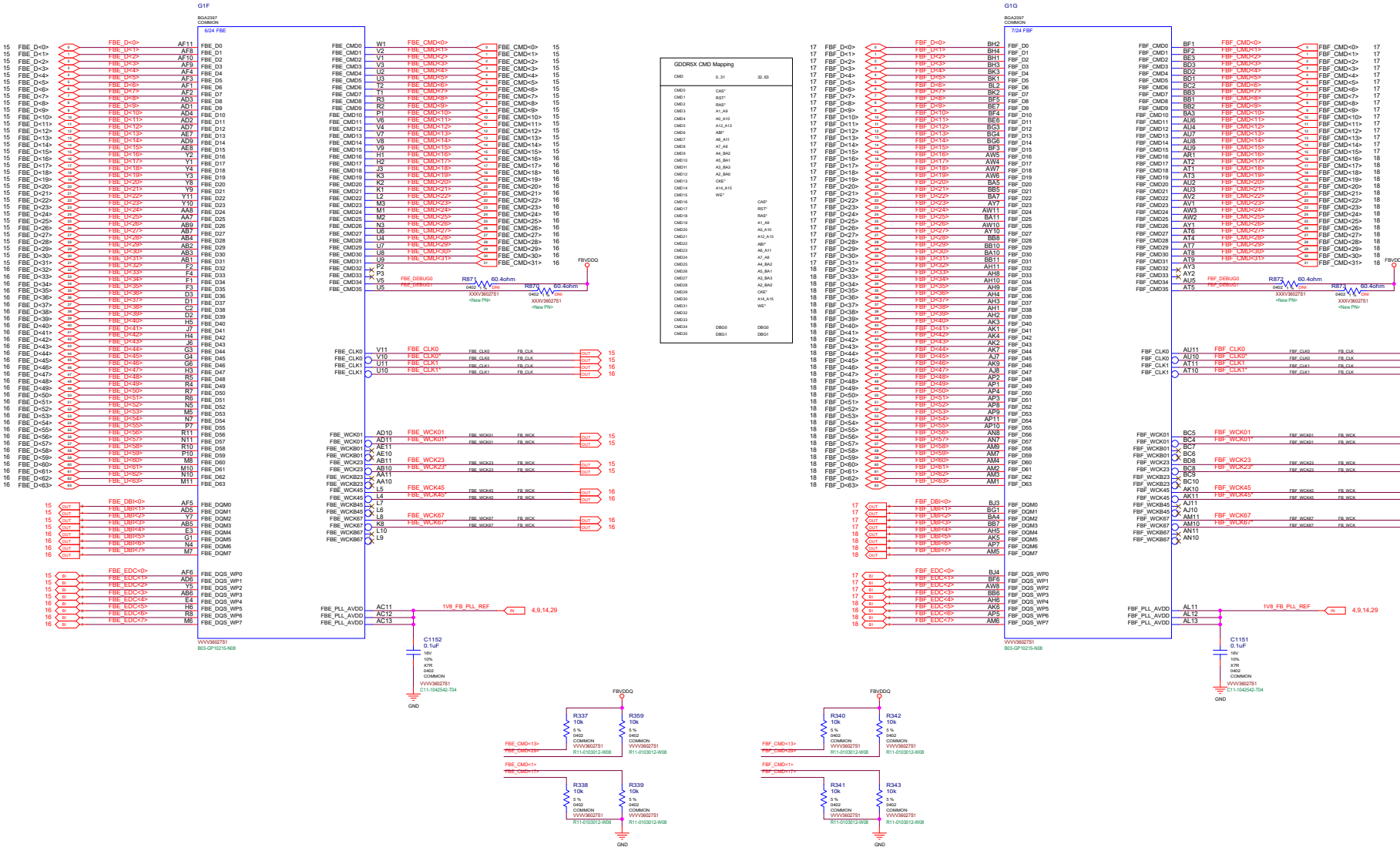

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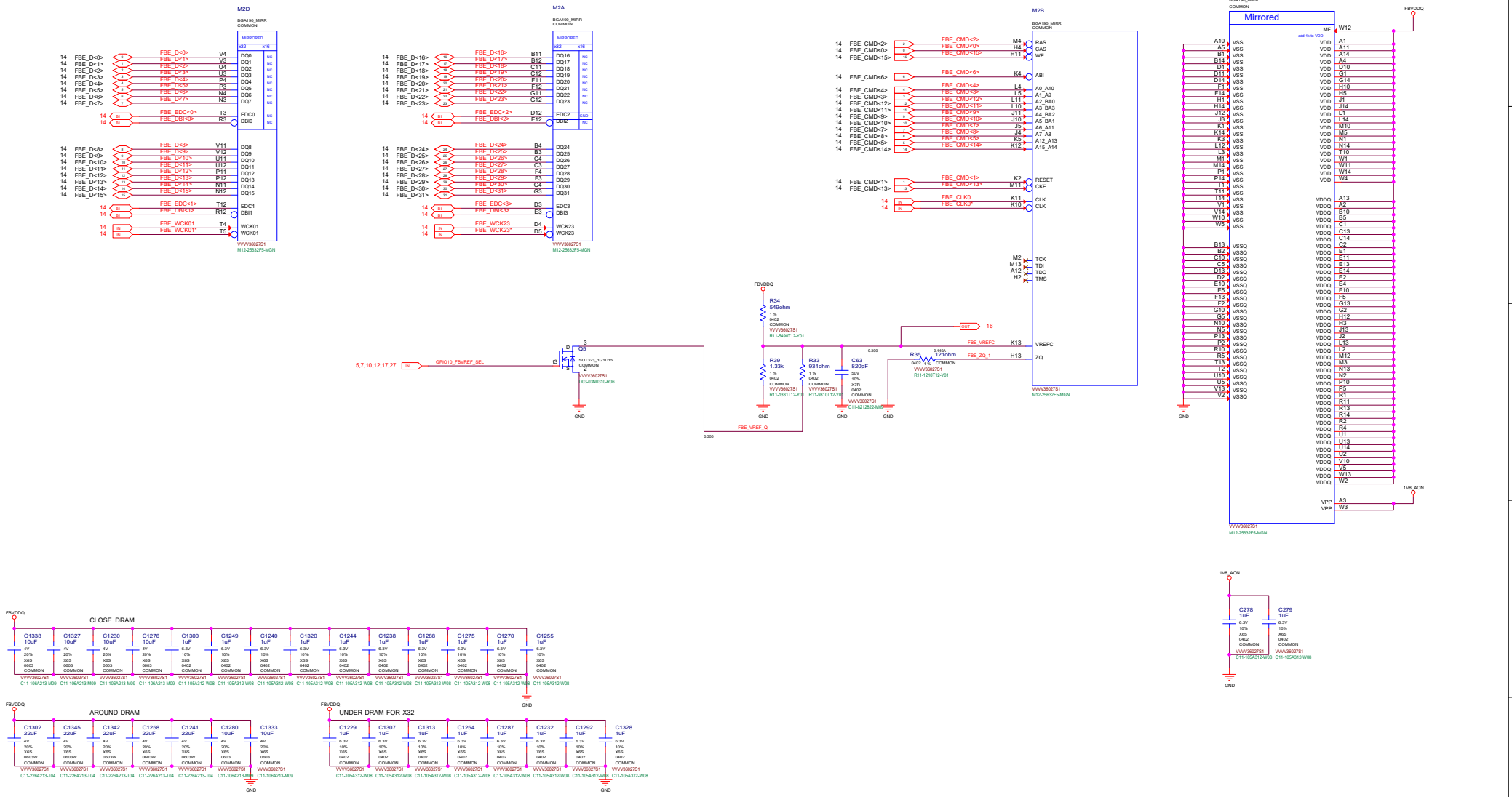

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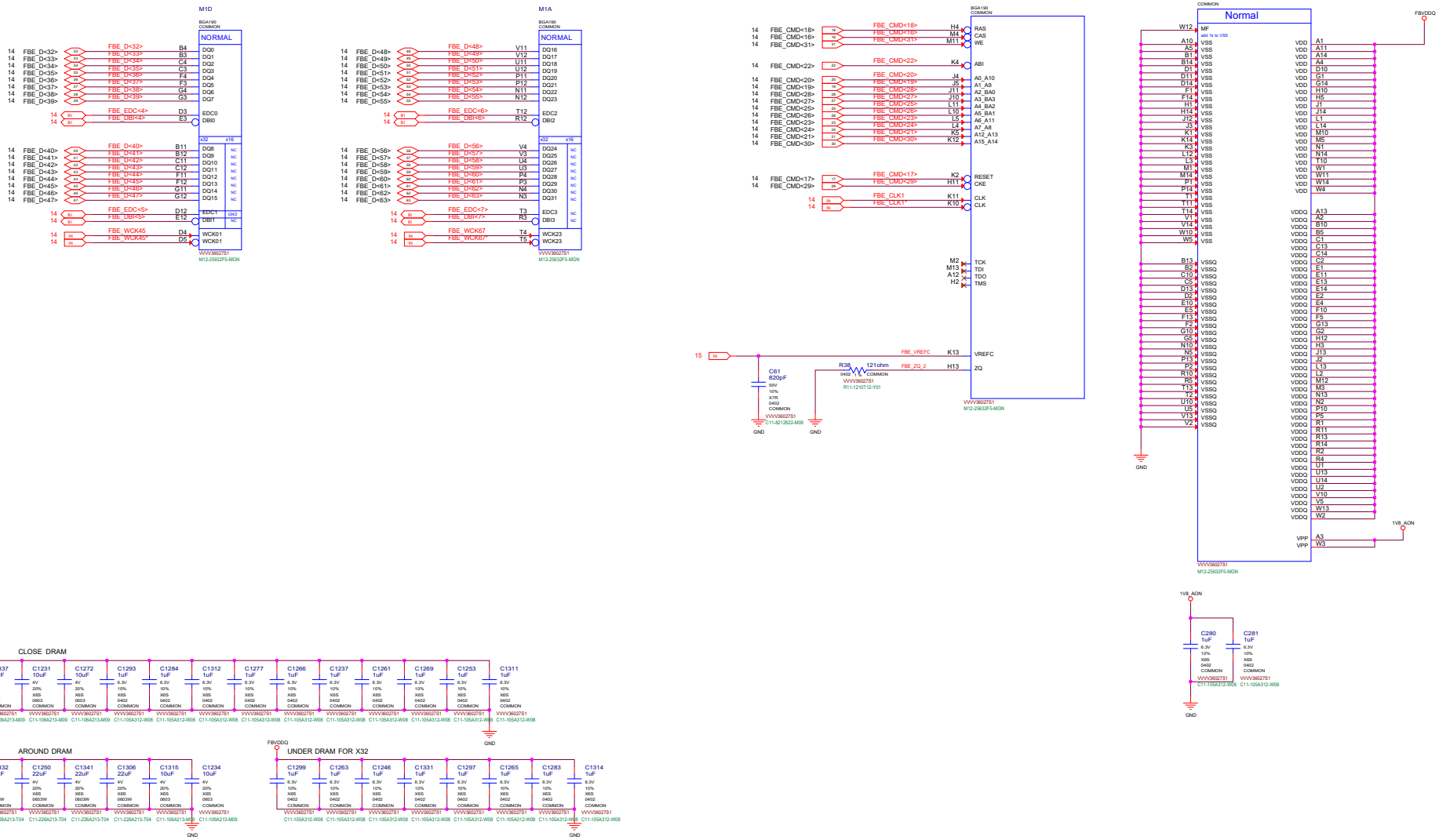

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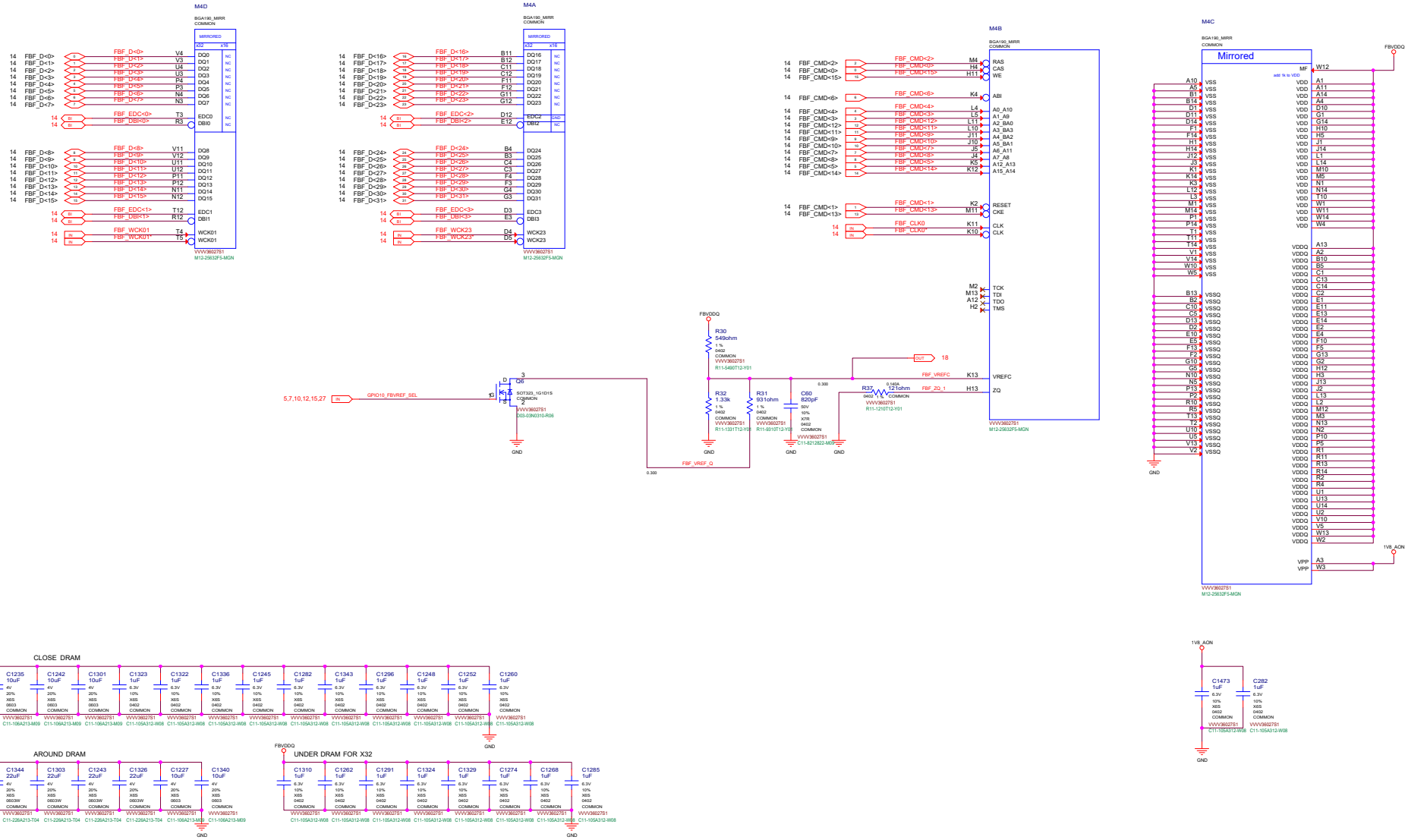

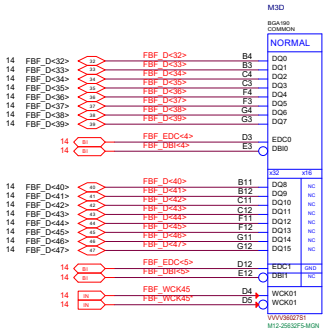

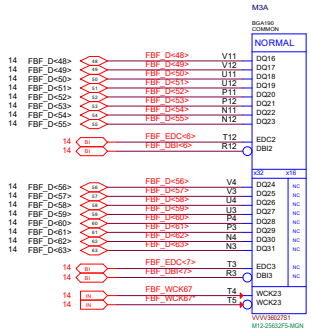

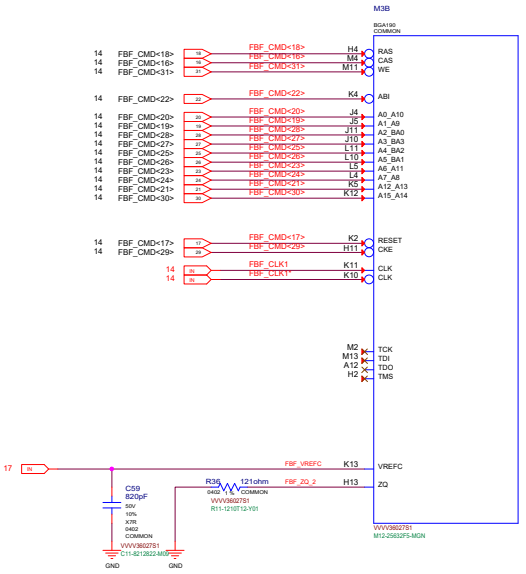

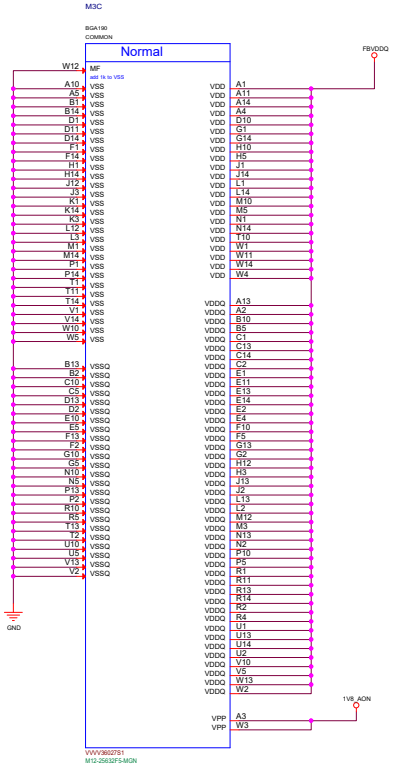

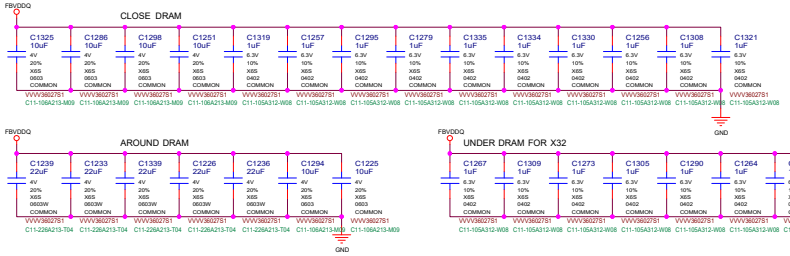

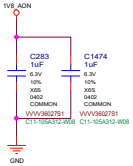

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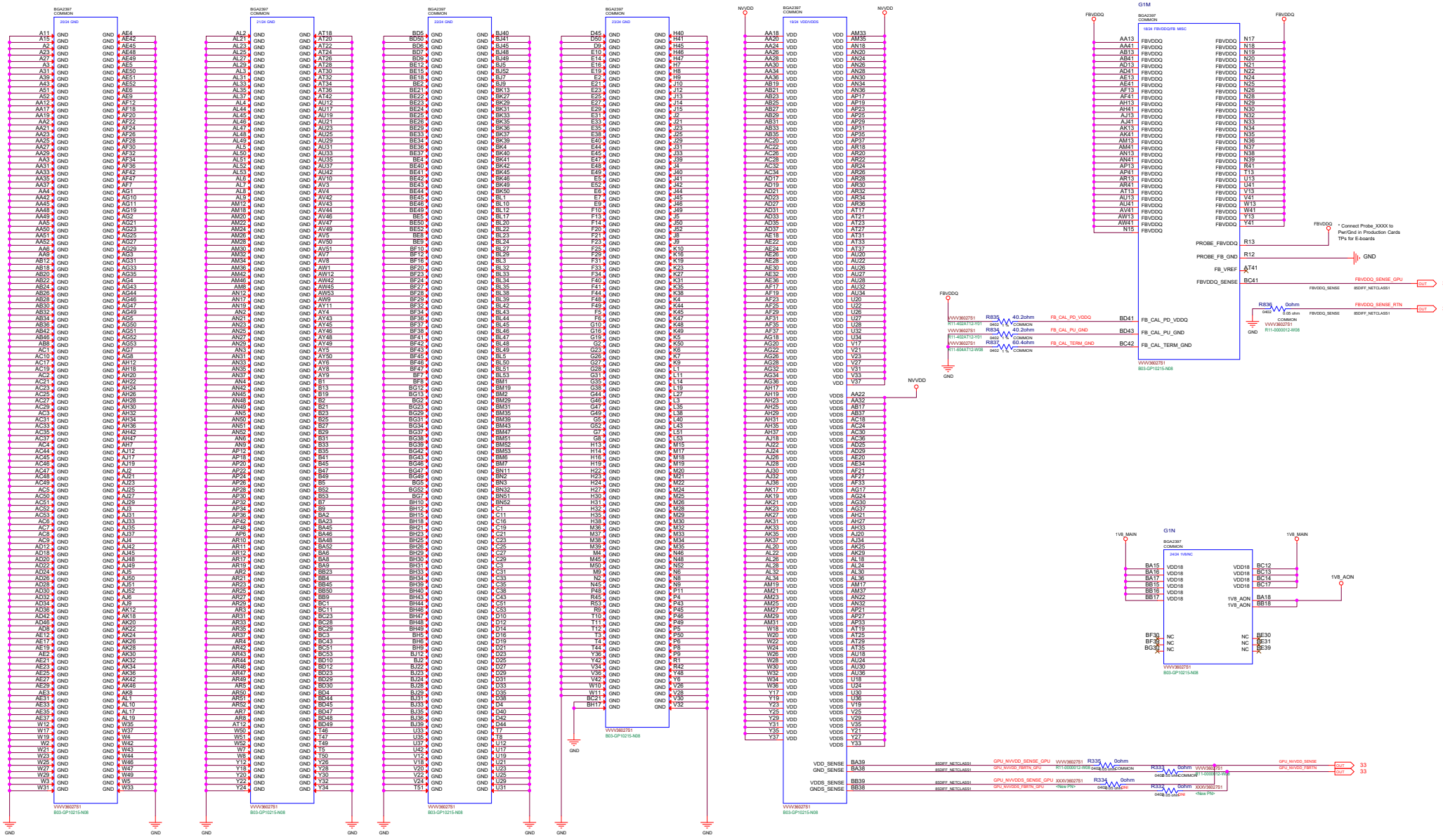

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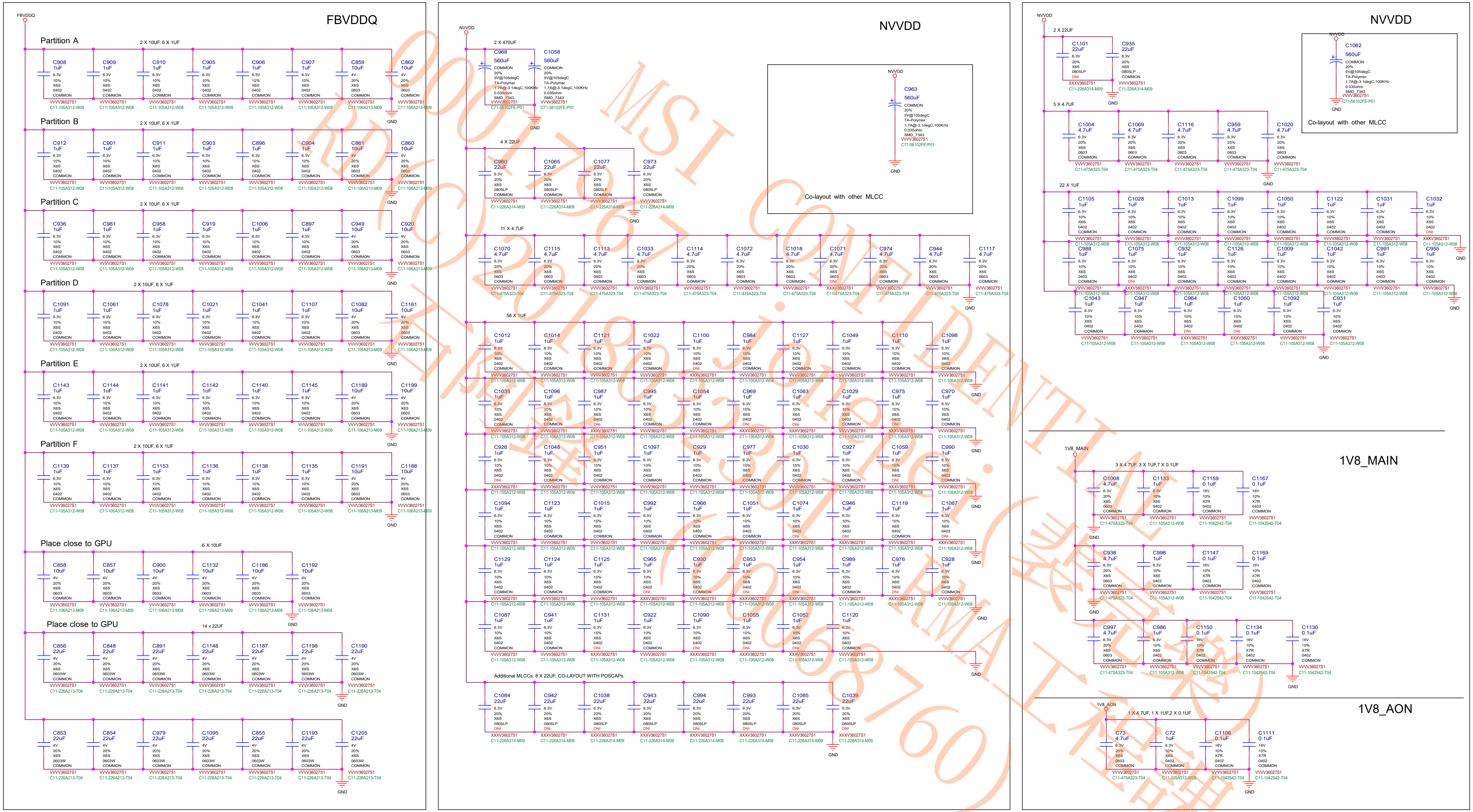
Page20: GPU Decoupling



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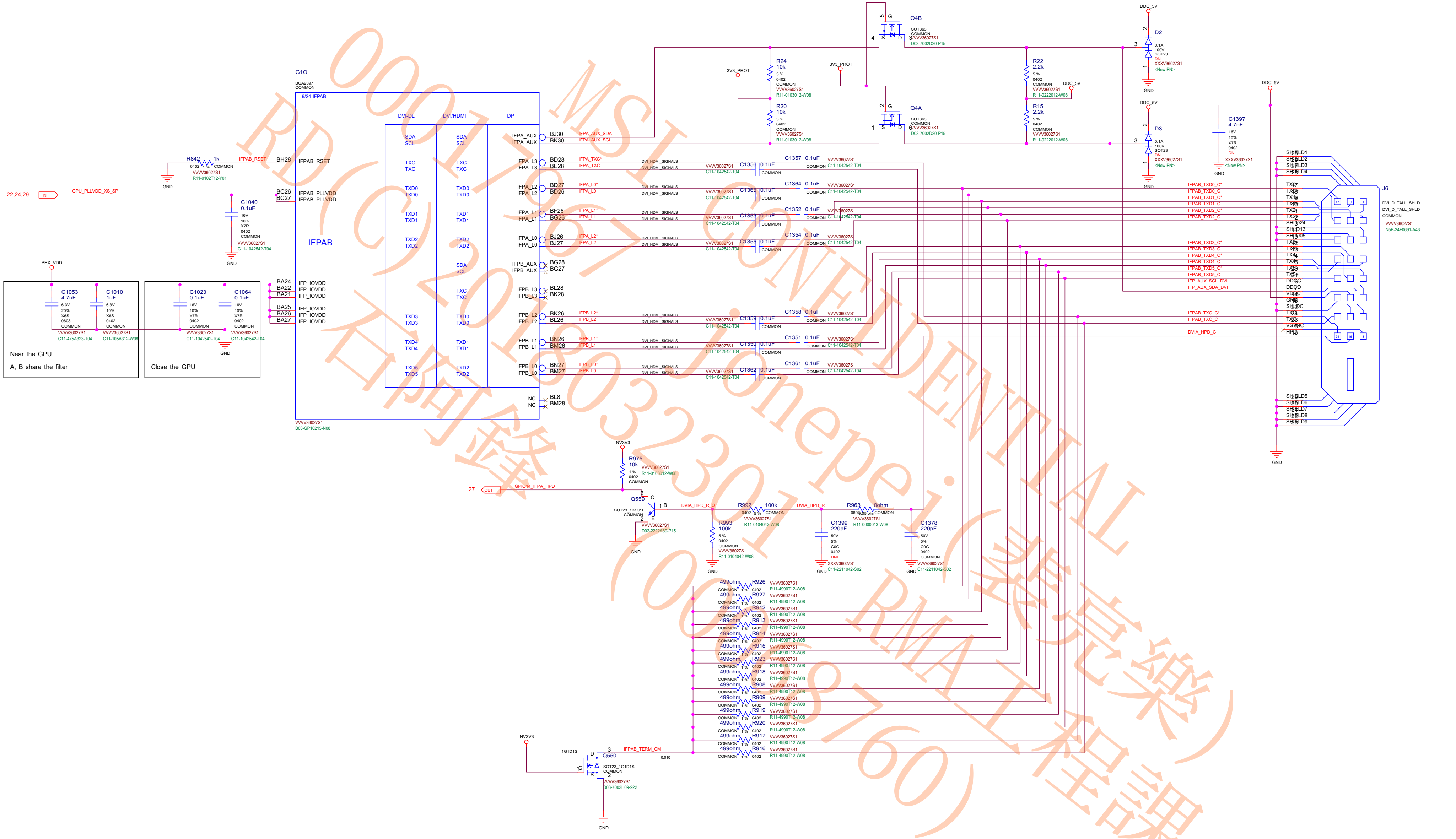

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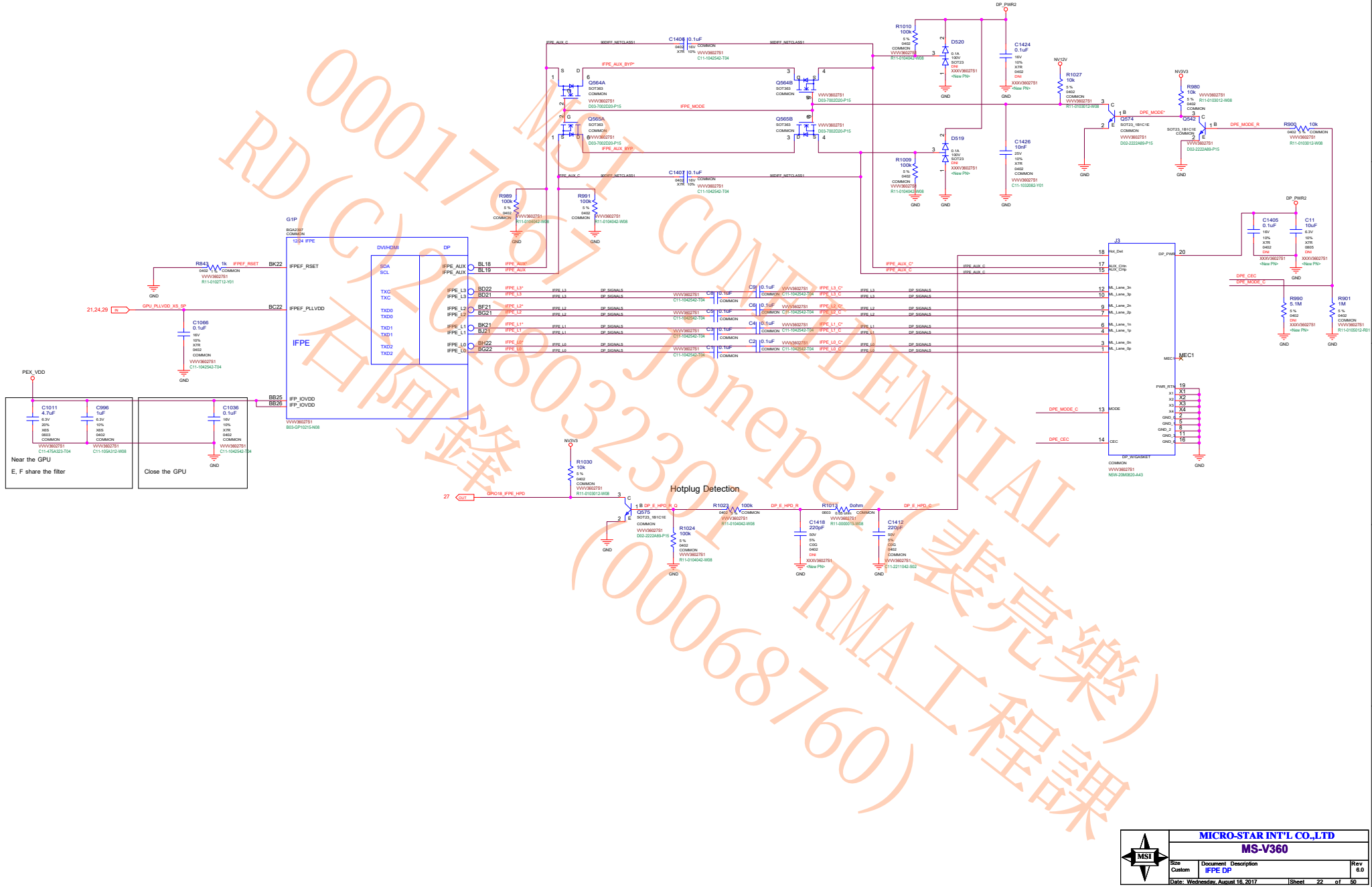
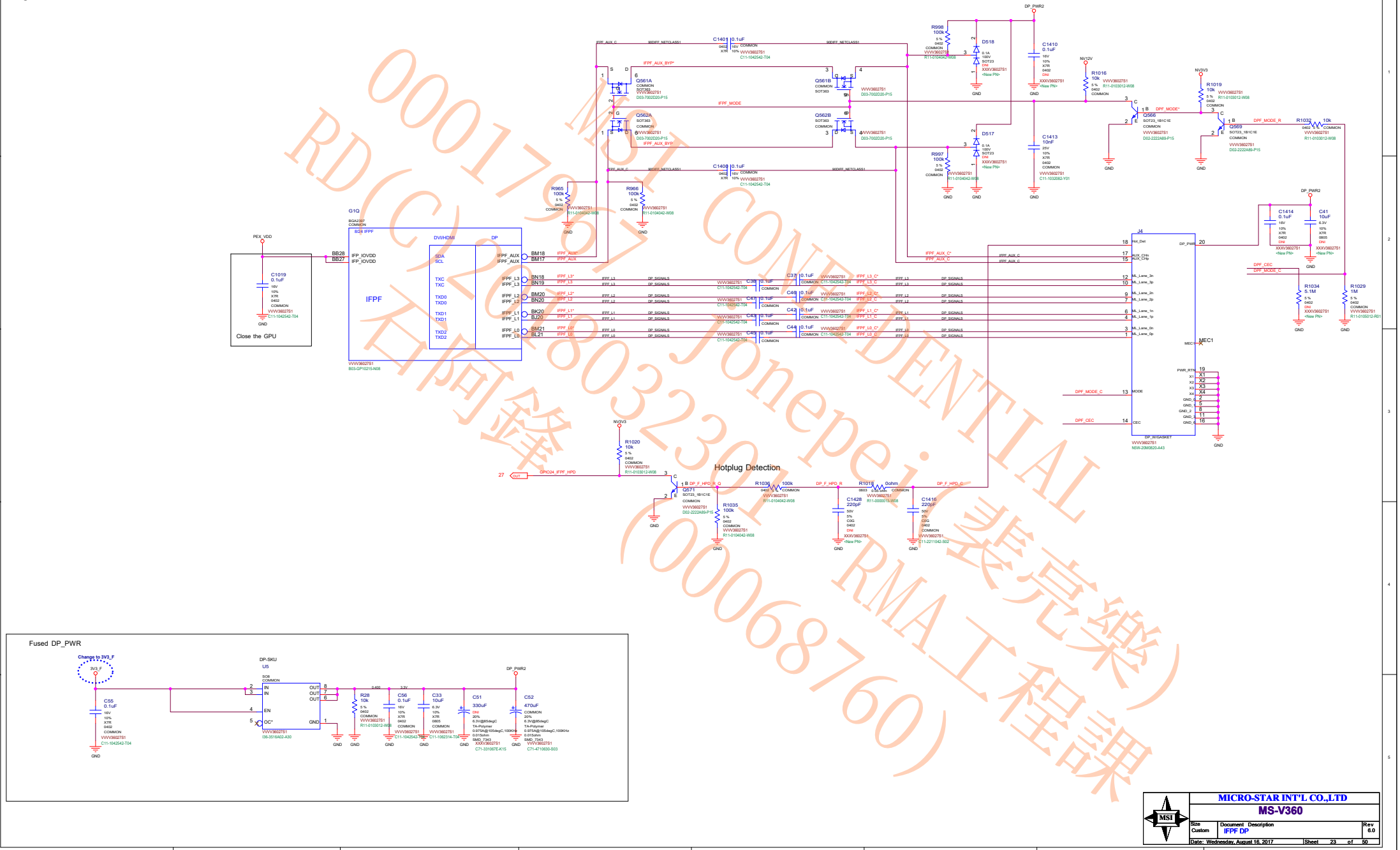
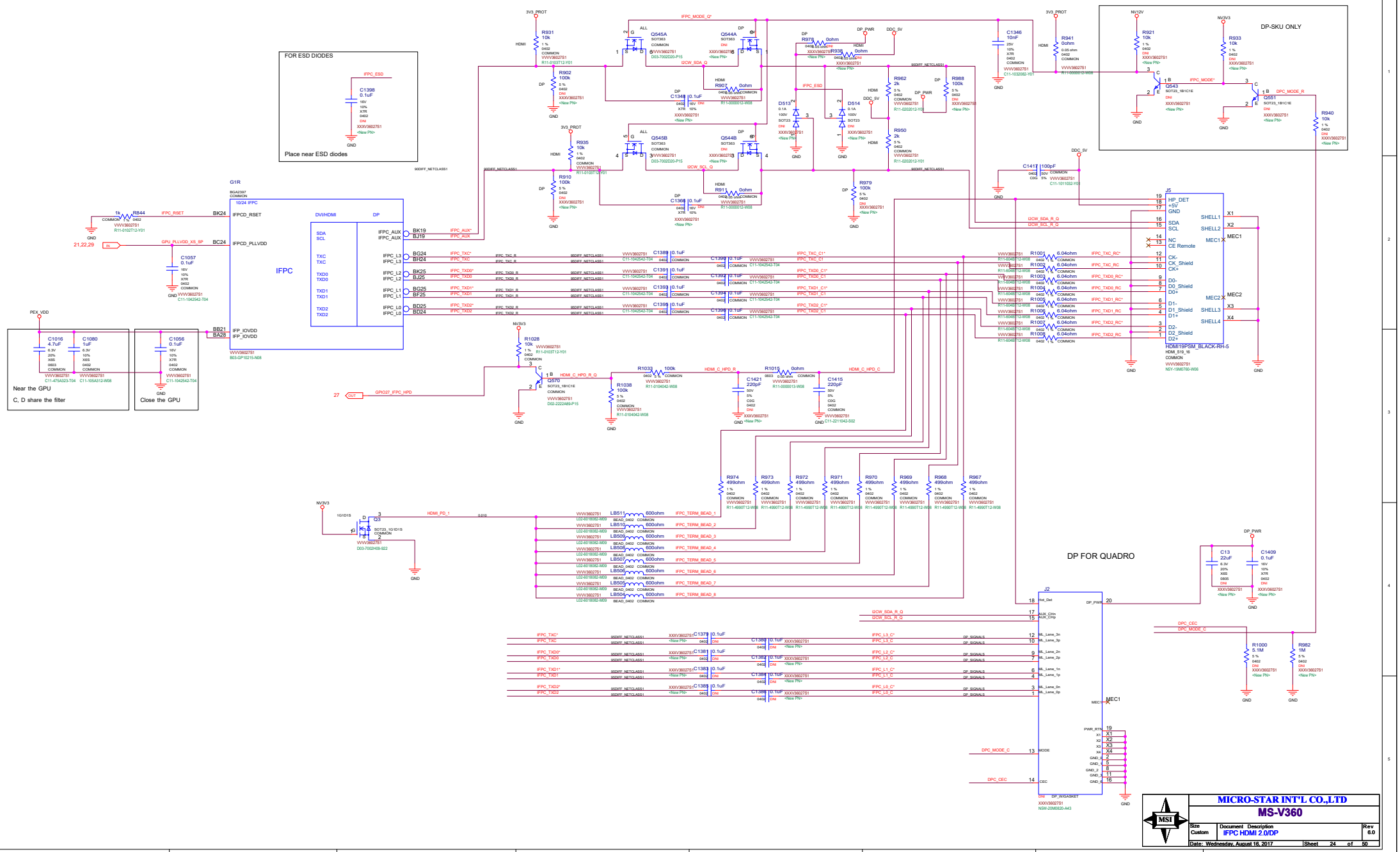
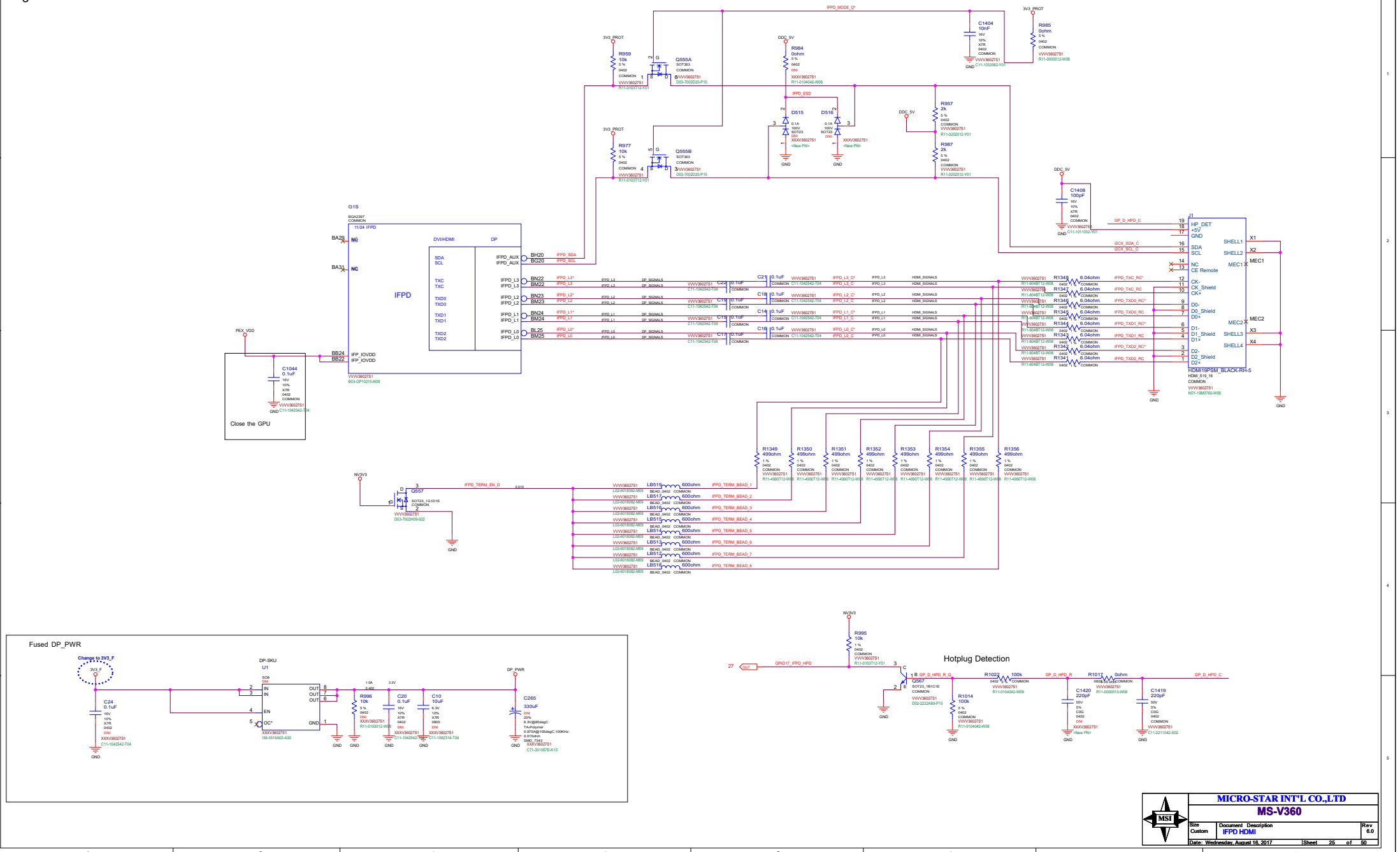




Page24: IFPC HDMI 2.0/DP



Page25: IFPD HDMI



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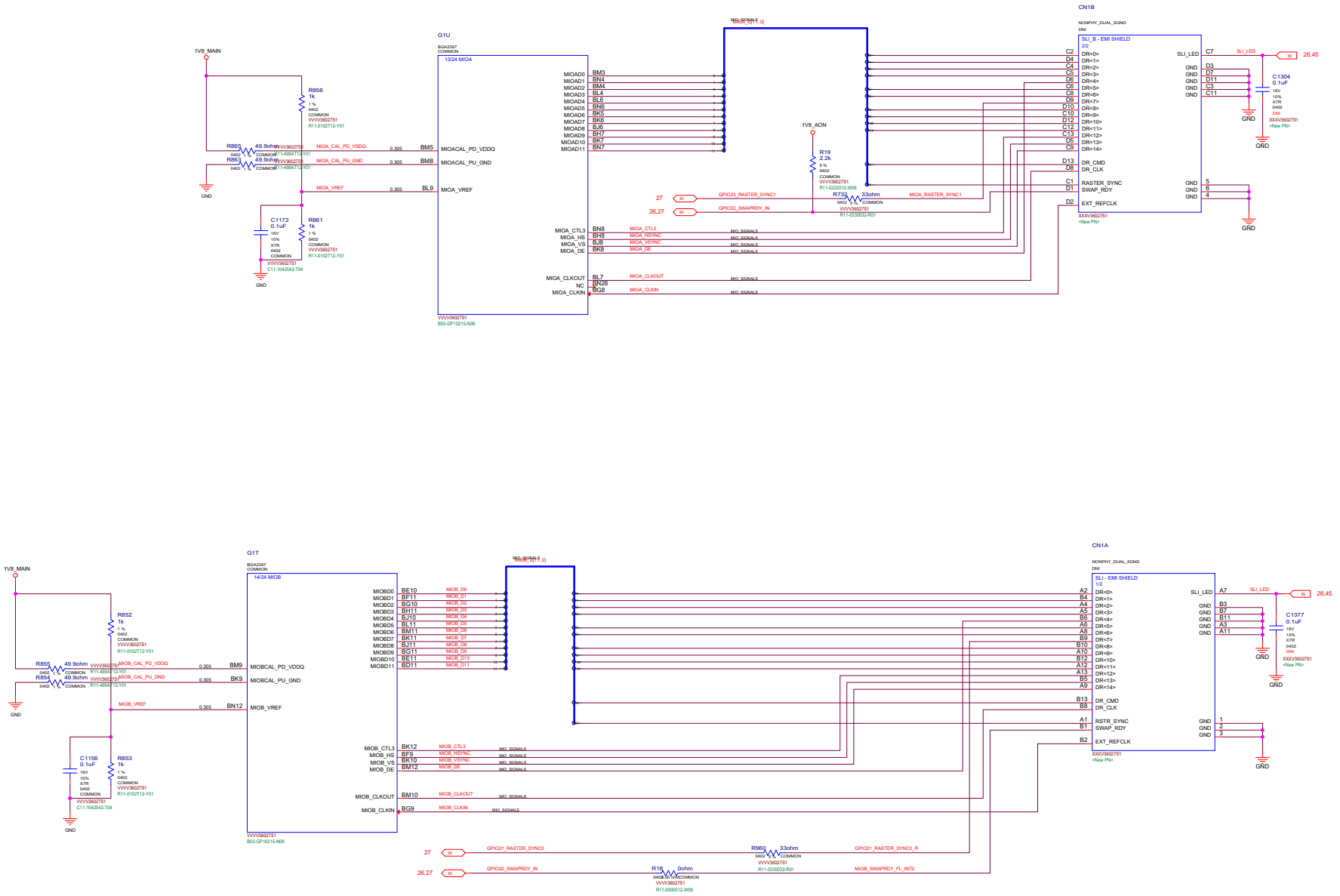
Page26: MIOA/B Interface



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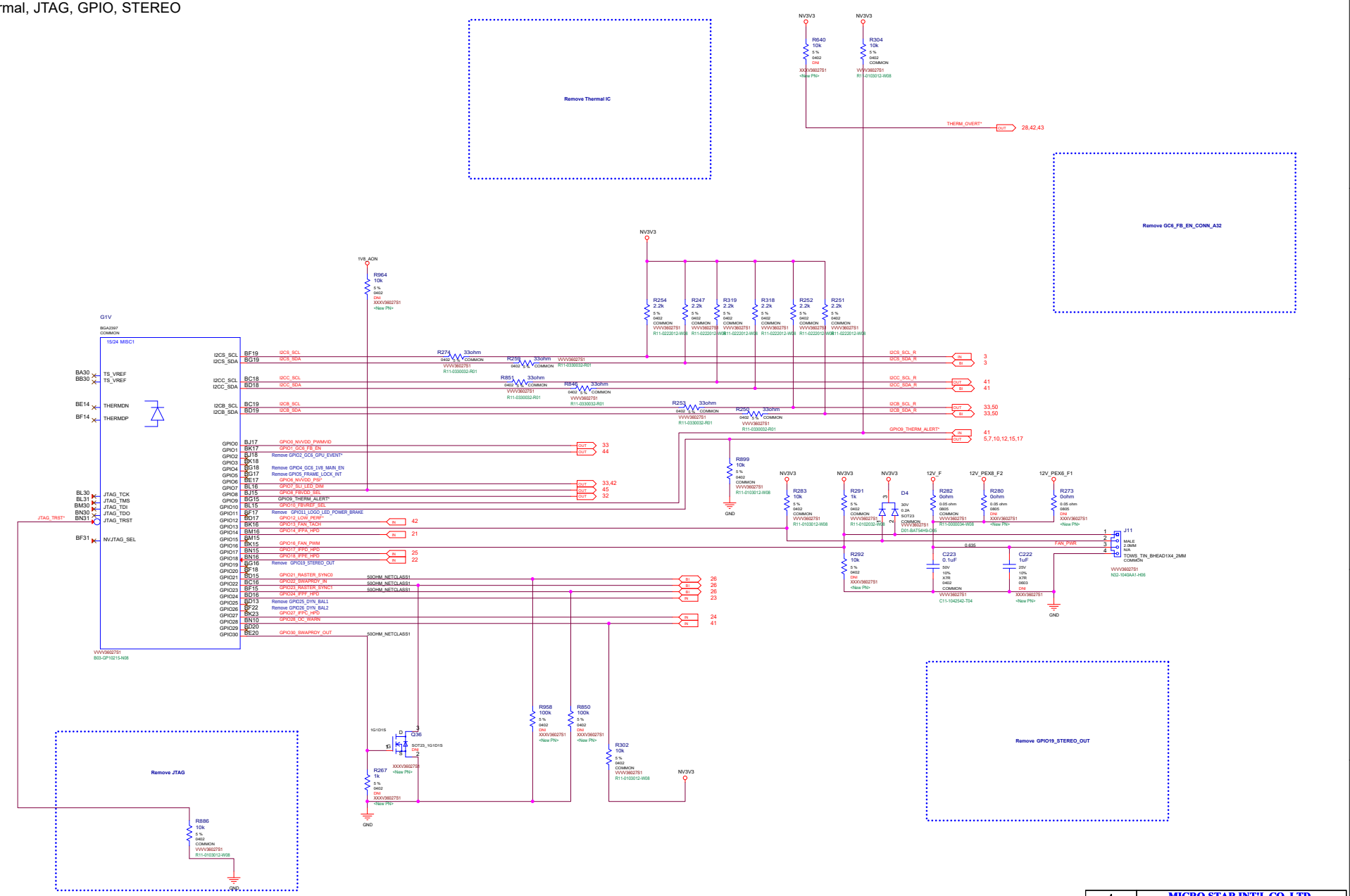
Page27: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: MISC1: Fan, Thermal, JTAG, GPIO, STEREO
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Page28: MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

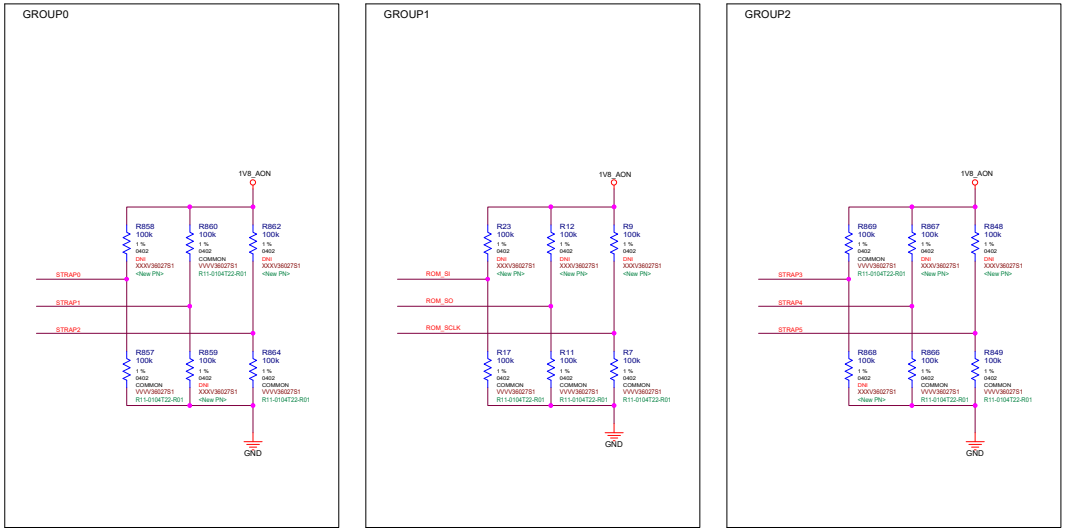
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

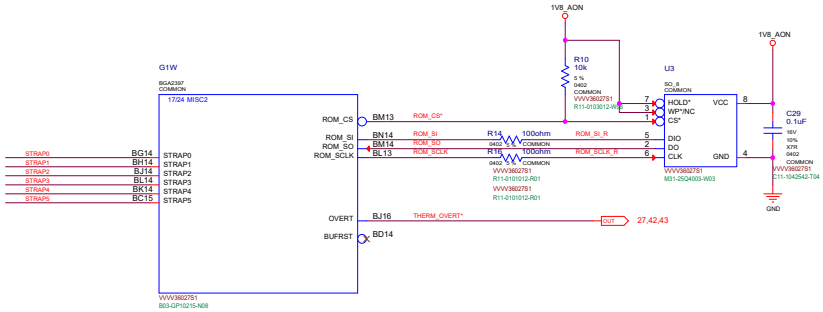
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





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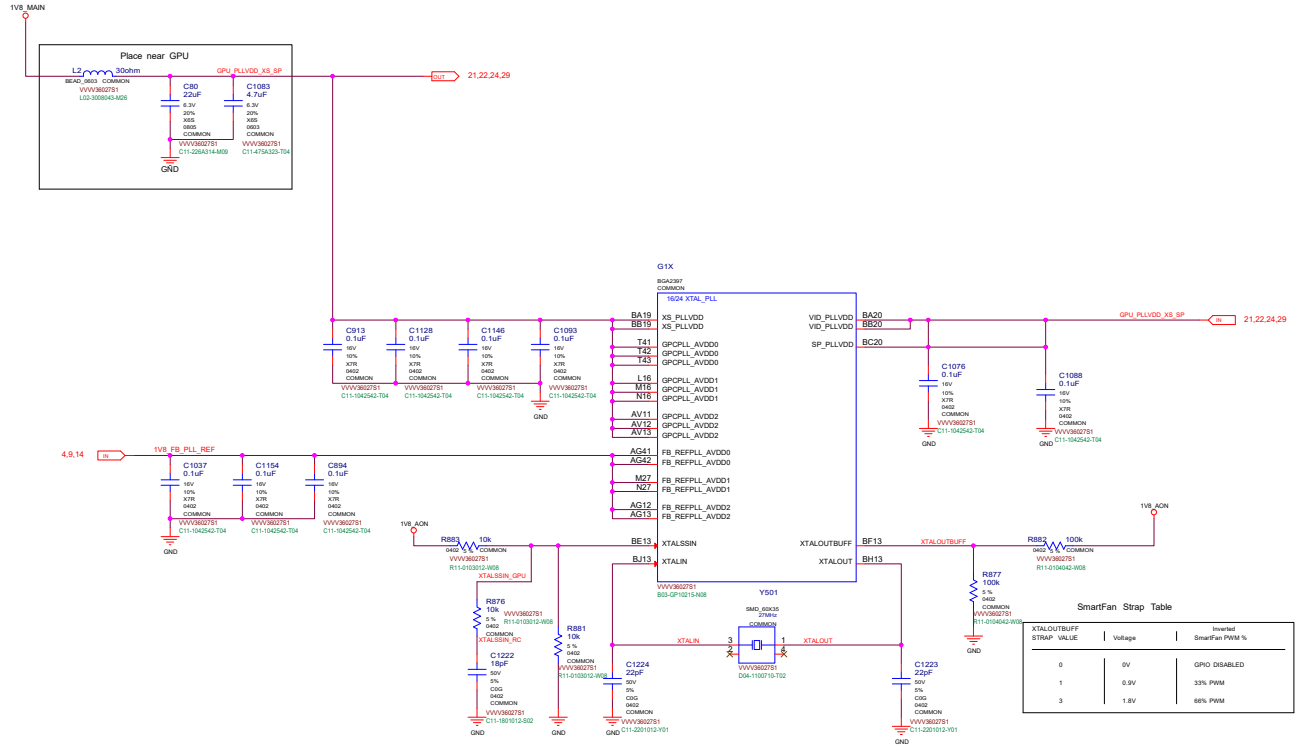

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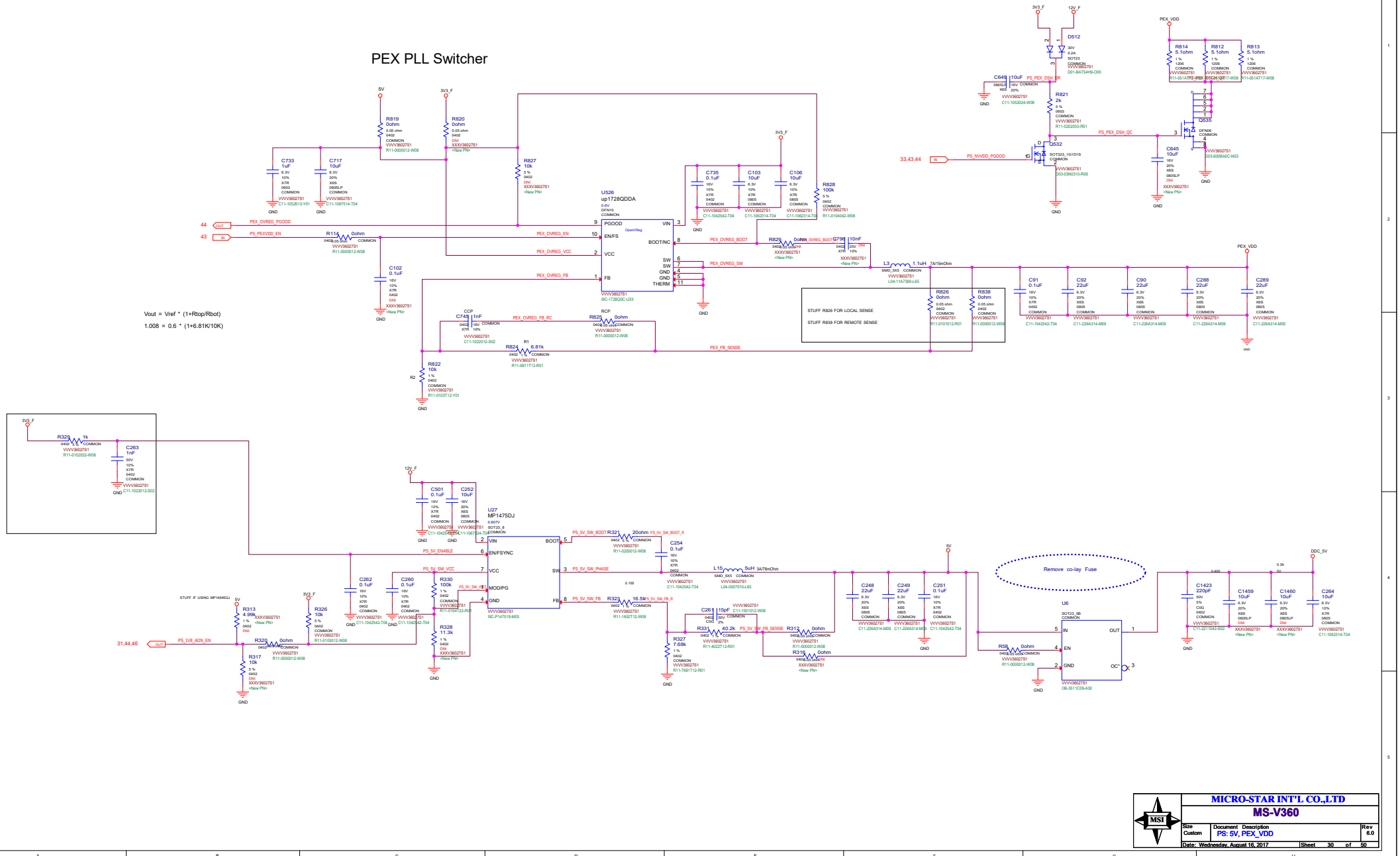
PEX PLL Switcher



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MS-V360		
Size: Custom	Document Description: PS: 5V, PEX_VDD	Rev: 6.0
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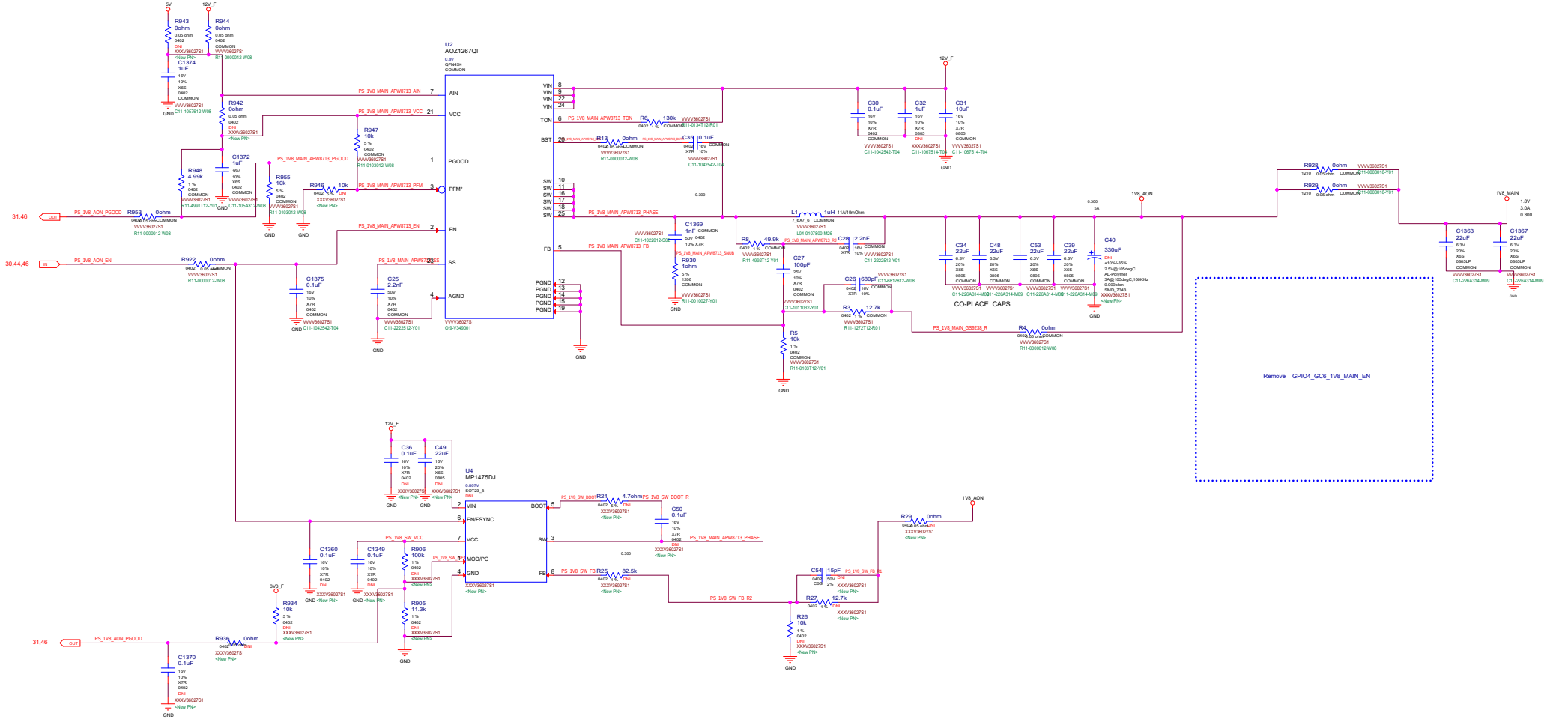
Page31: PS: 1V8 Rails



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Custom	PS: 1V8 Rails	6.0

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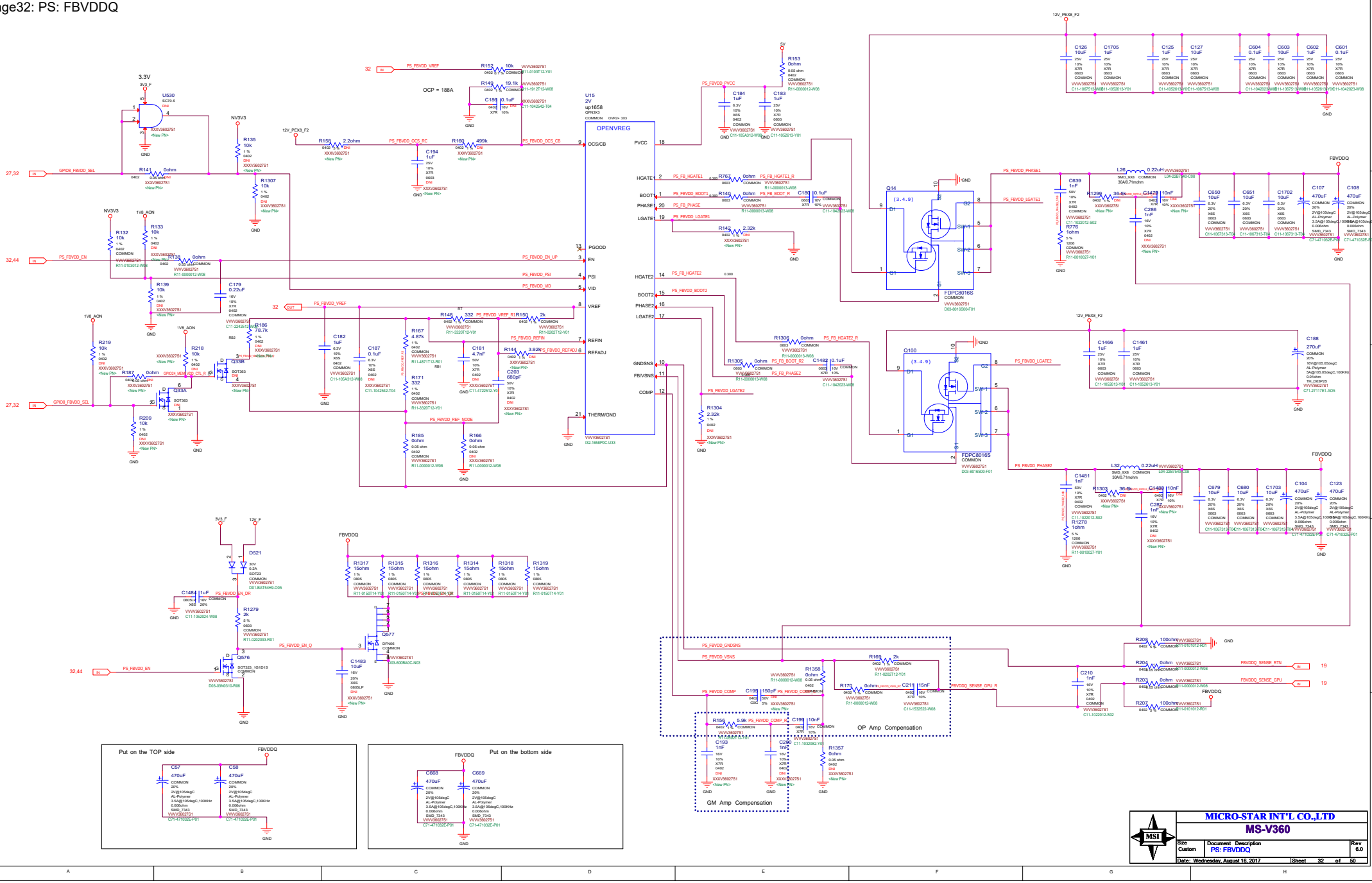
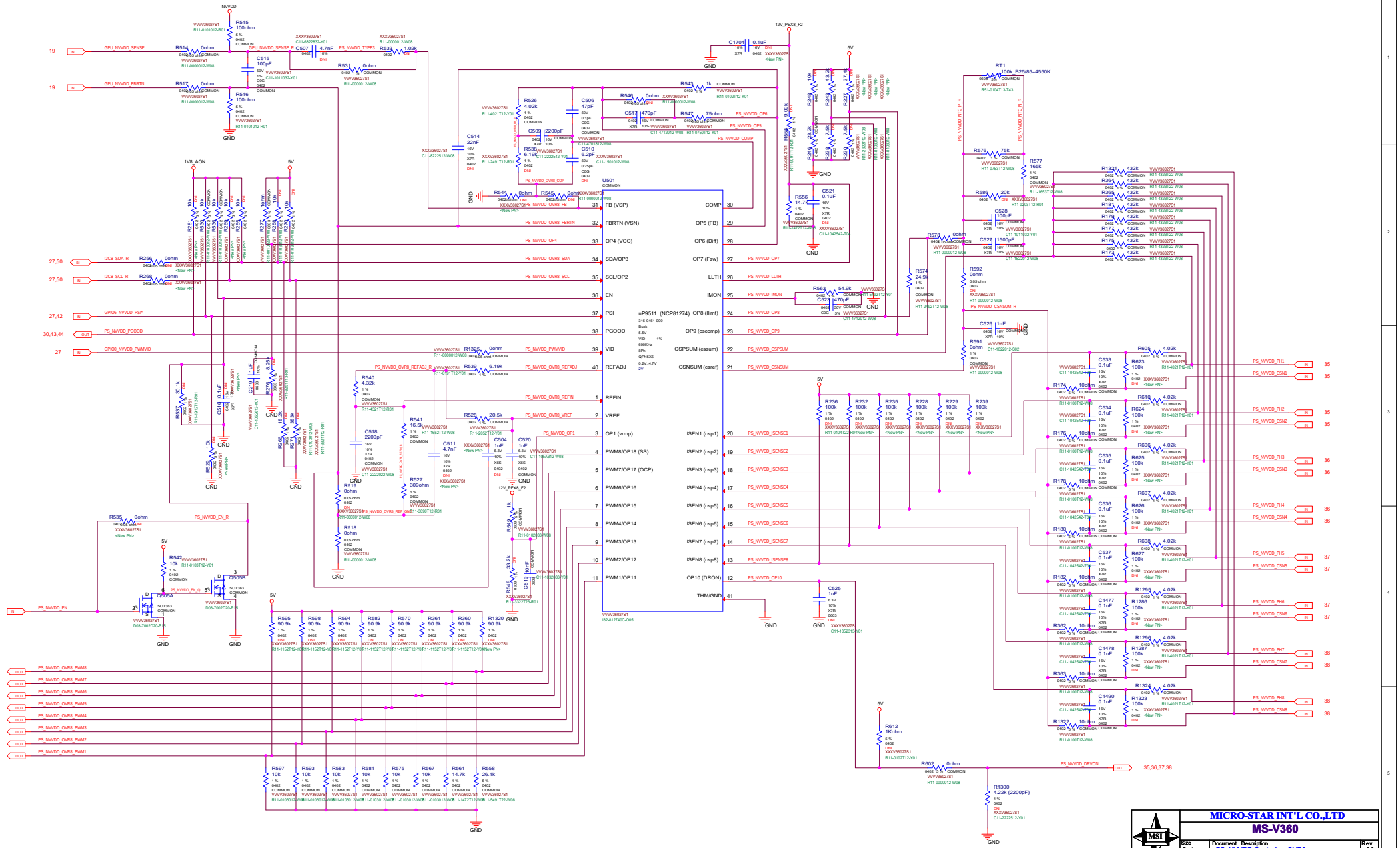
Page32: PS: FBVDDQ



Page33: PS: NVVDD Controller_OVR8



Page34: PS: NVVDD CONTROLLER_PWR-MODULE

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MS-V360	
Size: Custom	Document Description: PS: NVVDD CONTROLLER_PWR-MODULE
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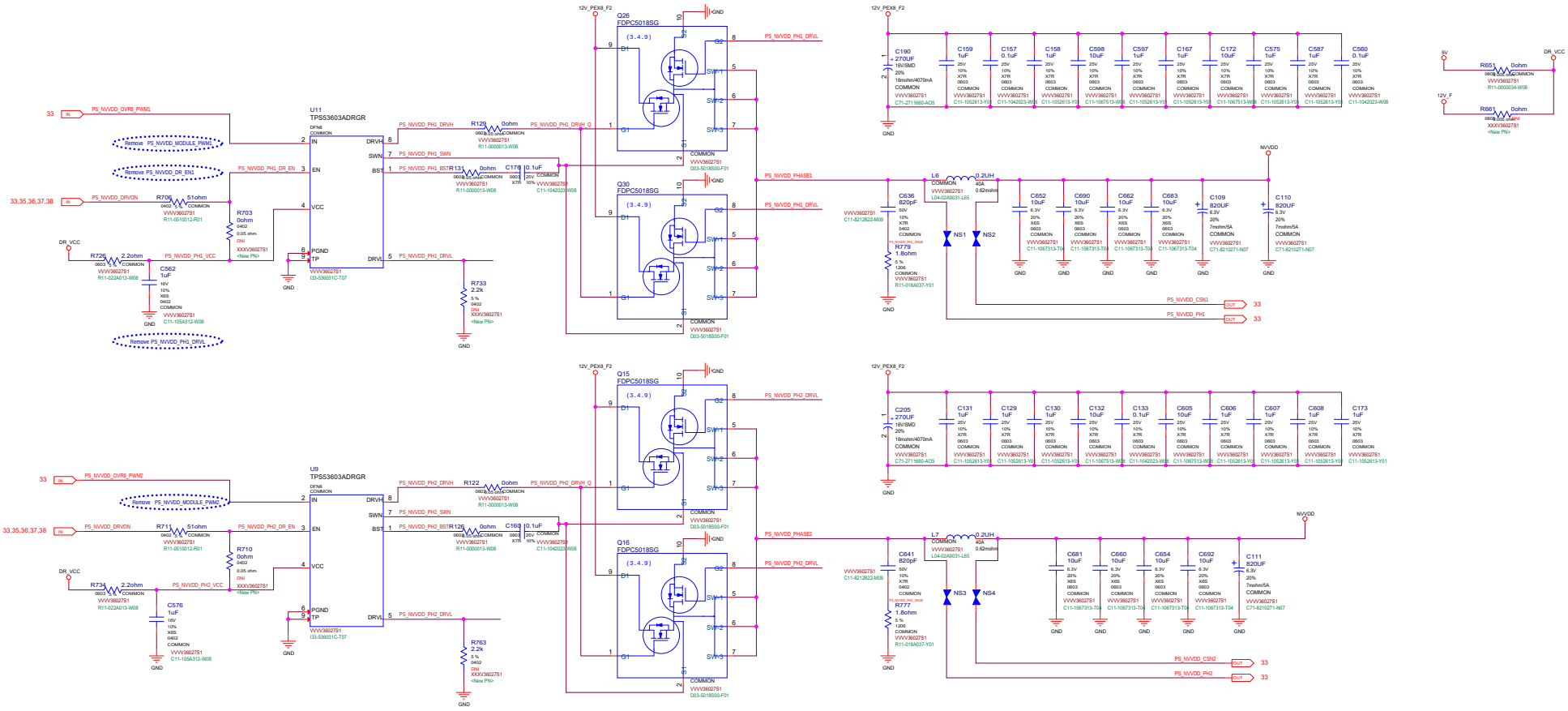

MICRO-STAR INT'L CO.,LTD			
MS-V360			
Size: Custom	Document Description: PS: NVVDD Phase 1,2		Rev: 6.0
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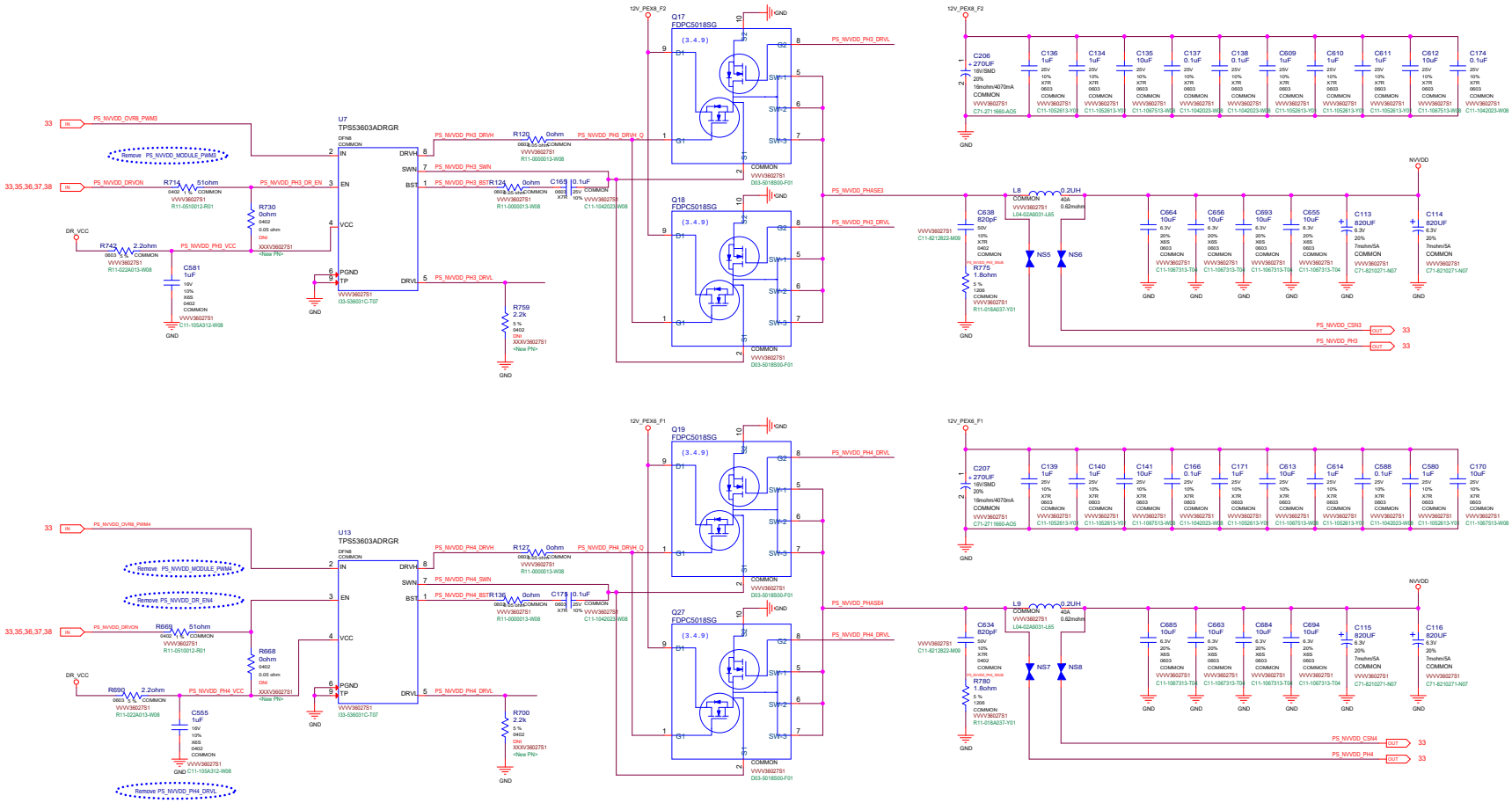
Page36: PS: NVVDD Phase 3,4



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Size: Custom
Document Description: PS: NVVDD Phase 3,4
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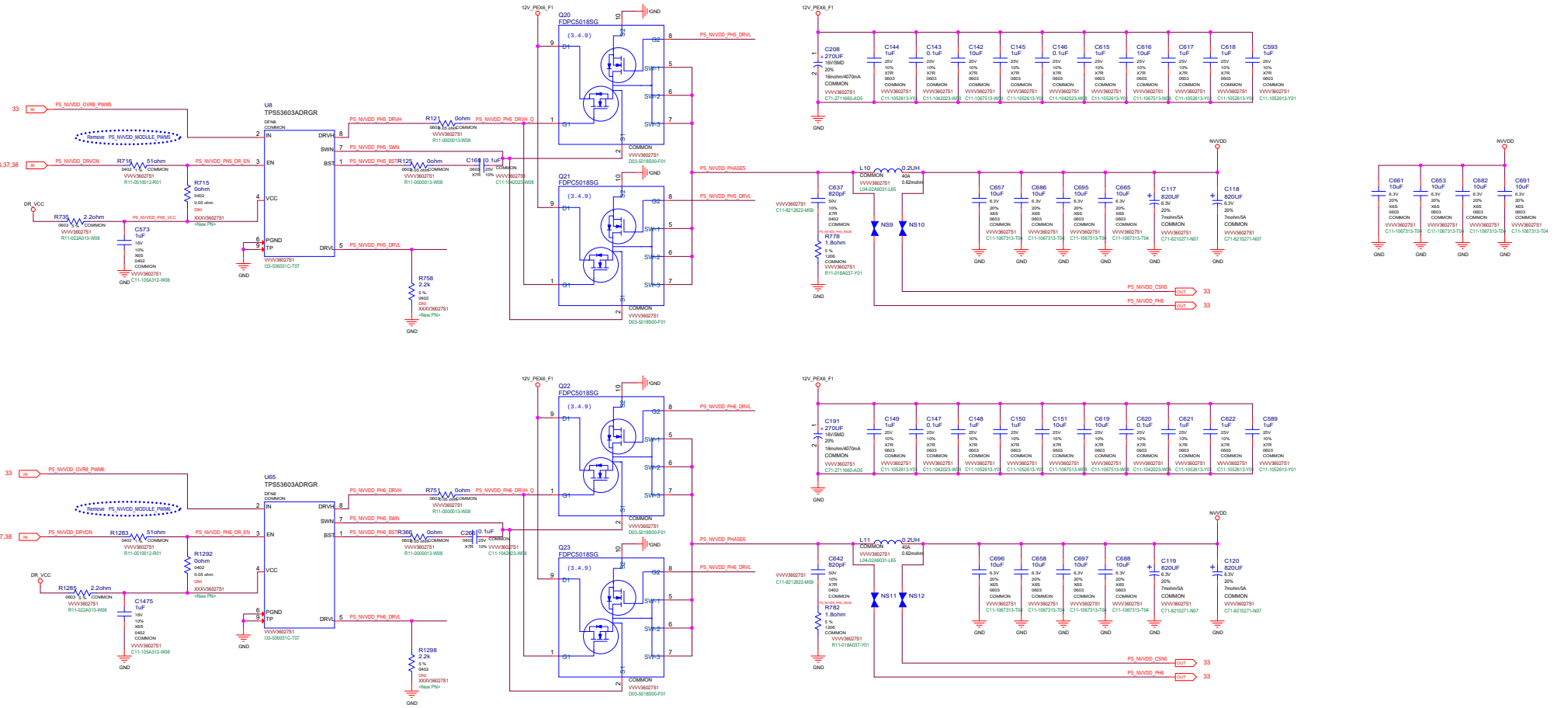
Page37: PS: NVVDD Phase 5,6



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Custom	PS: NVVDD Phase 5,6	6.0

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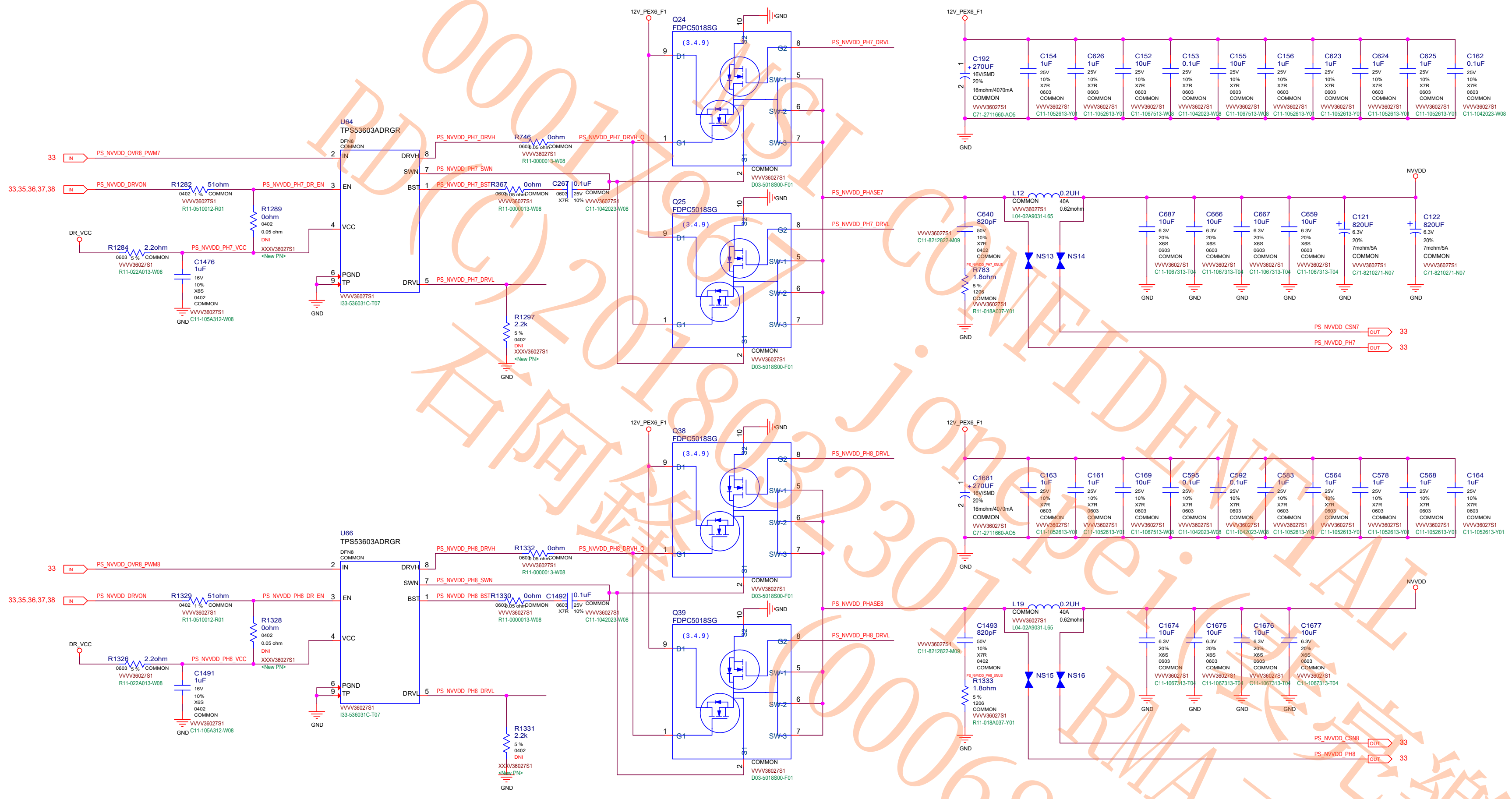
Page41: PS:NVVDD Phase 7,8



U64
TPS53603ADRGR
U66
TPS53603ADRGR
Q24
FDPC5018SG
Q25
FDPC5018SG
Q38
FDPC5018SG
Q39
FDPC5018SG
12V_PEX6_F1
PS_NVVDD_OVR8_PWM7
PS_NVVDD_OVR8_PWM8
PS_NVVDD_DRVON
PS_NVVDD_PH7_DR_EN
PS_NVVDD_PH8_DR_EN
PS_NVVDD_PH7_VCC
PS_NVVDD_PH8_VCC
PS_NVVDD_PH7_DRVH
PS_NVVDD_PH8_DRVH
PS_NVVDD_PH7_SWN
PS_NVVDD_PH8_SWN
PS_NVVDD_PH7_BST
PS_NVVDD_PH8_BST
PS_NVVDD_PH7_DRVL
PS_NVVDD_PH8_DRVL
PS_NVVDD_PHASE7
PS_NVVDD_PHASE8
PS_NVVDD_CSN7
PS_NVVDD_CSN8
PS_NVVDD_PH7
PS_NVVDD_PH8
NVVDD
DR_VCC
GND
L12 0.2UH
L19 0.2UH
NS13
NS14
NS15
NS16
C192 270UF
C1681 270UF
C121 820UF
C122 820UF

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Page39: PS: Dynamic Power Balance Phases

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Page40: PS: Dynamic Power Balance Logic

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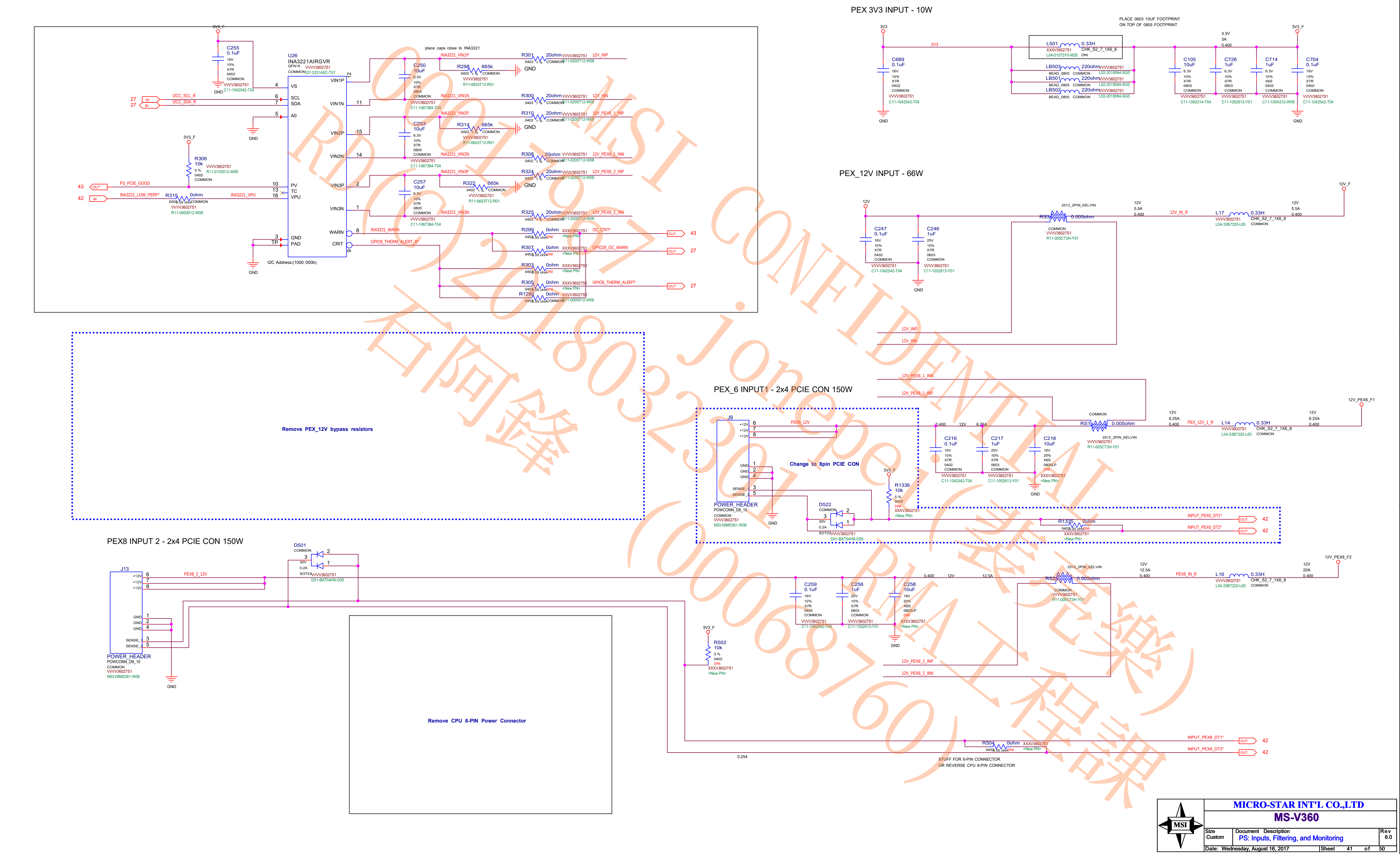
Page41: PS: Inputs, Filtering, and Monitoring



PEX 3V3 INPUT - 10W
PLACE 0603 10UF FOOTPRINT ON TOP OF 0805 FOOTPRINT
PEX_12V INPUT - 66W
PEX_6 INPUT1 - 2x4 PCIE CON 150W
PEX8 INPUT 2 - 2x4 PCIE CON 150W
U26
INA3221AIRGVR
place caps close to INA3221
I2C Address:(1000 000b)
Remove PEX_12V bypass resistors
Change to 8pin PCIE CON
Remove CPU 8-PIN Power Connector
STUFF FOR 6-PIN CONNECTOR OR REVERSE CPU 8-PIN CONNECTOR
J9
J13
POWER_HEADER
D501
D522
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Size Custom
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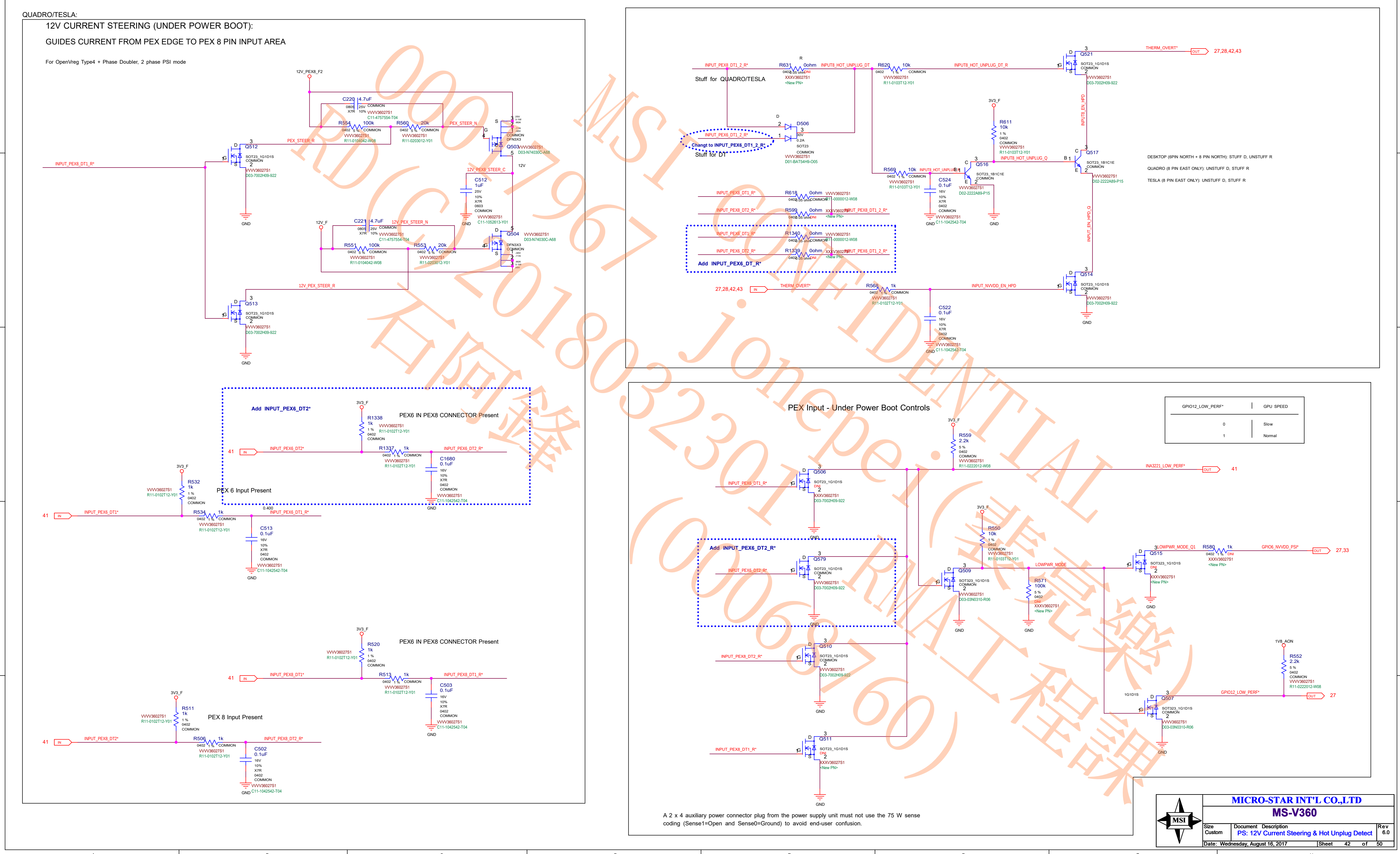
Page42: PS: 12V Current Steering & Hot Unplug Detect



QUADRO/TESLA:
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA
For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode
Stuff for QUADRO/TESLA
Change to INPUT_PEX6_DT1_2_R*
Stuff for DT
Add INPUT_PEX6_DT_R*
DESKTOP (6PIN NORTH + 8 PIN NORTH): STUFF D, UNSTUFF R
QUADRO (8 PIN EAST ONLY): UNSTUFF D, STUFF R
TESLA (8 PIN EAST ONLY): UNSTUFF D, STUFF R
Add INPUT_PEX6_DT2*
PEX6 IN PEX8 CONNECTOR Present
PEX 6 Input Present
PEX 8 Input Present
PEX Input - Under Power Boot Controls
Add INPUT_PEX6_DT2_R*
GPIO12_LOW_PERF*
GPU SPEED
0
Slow
1
Normal
A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.
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Size
Custom
Document Description
PS: 12V Current Steering & Hot Unplug Detect
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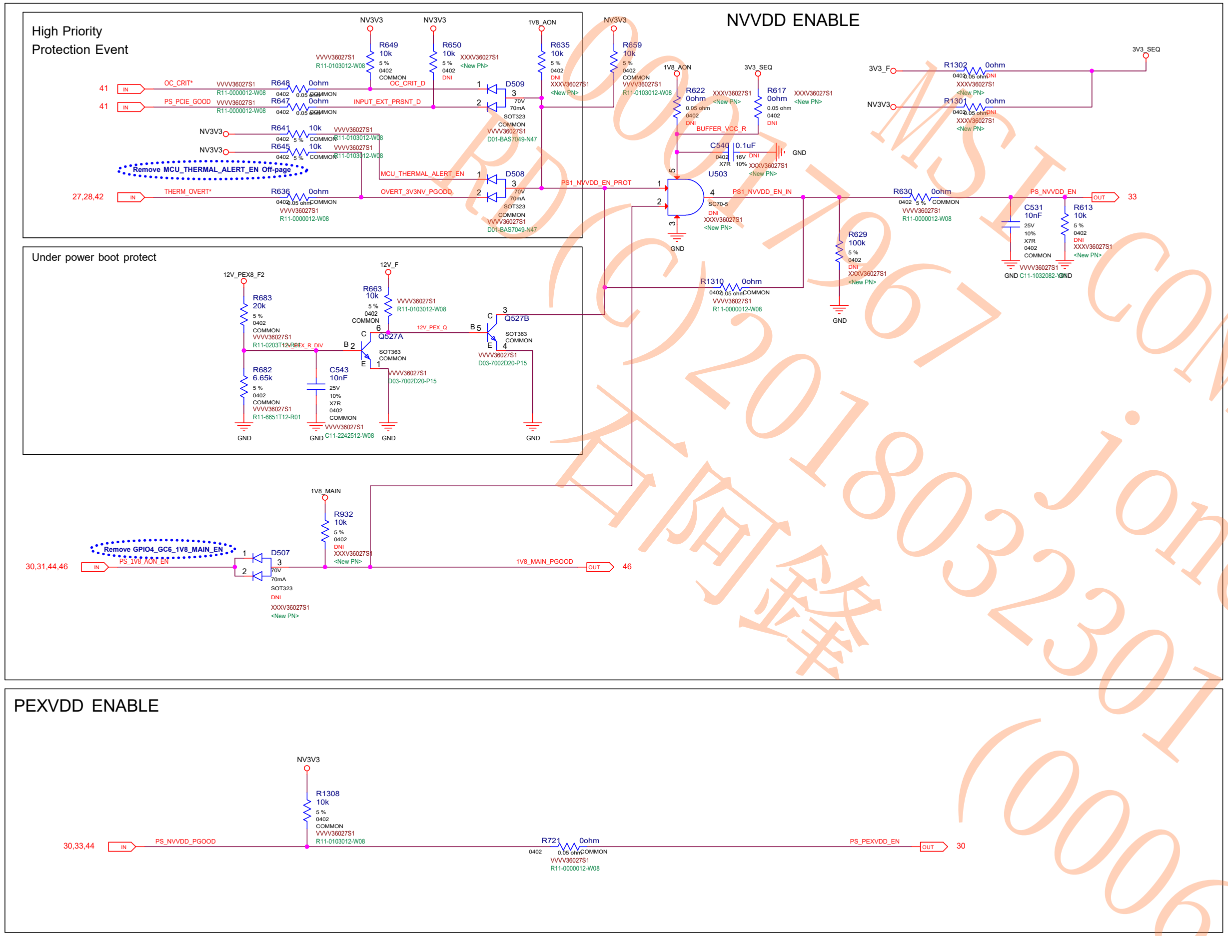
Page43: PS: NVVDD ENABLE



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Custom	PS: NVVDD ENABLE	6.0

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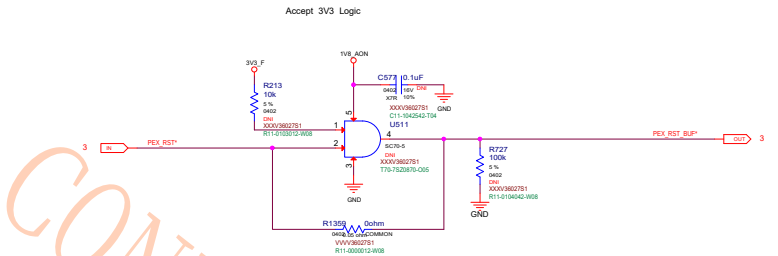
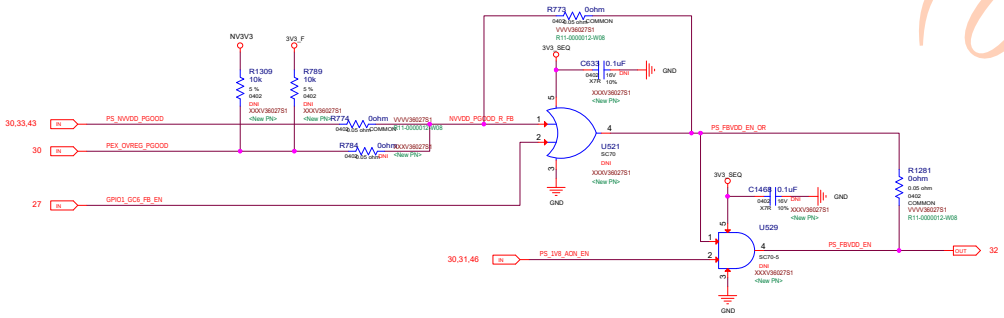
Remove PEX_CLKREQ*

Remove GPU_EVENT*

PEX_RST# LOGIC



FBVDD/Q ENABLE



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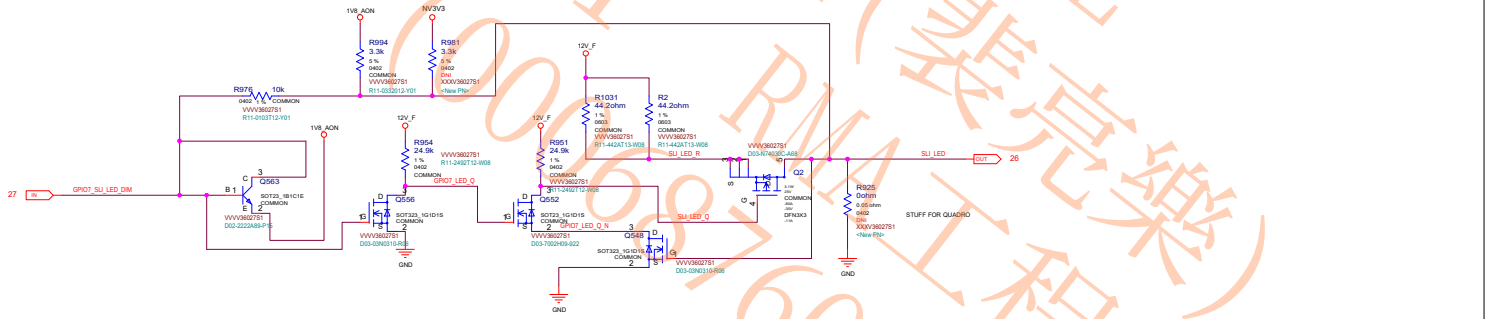
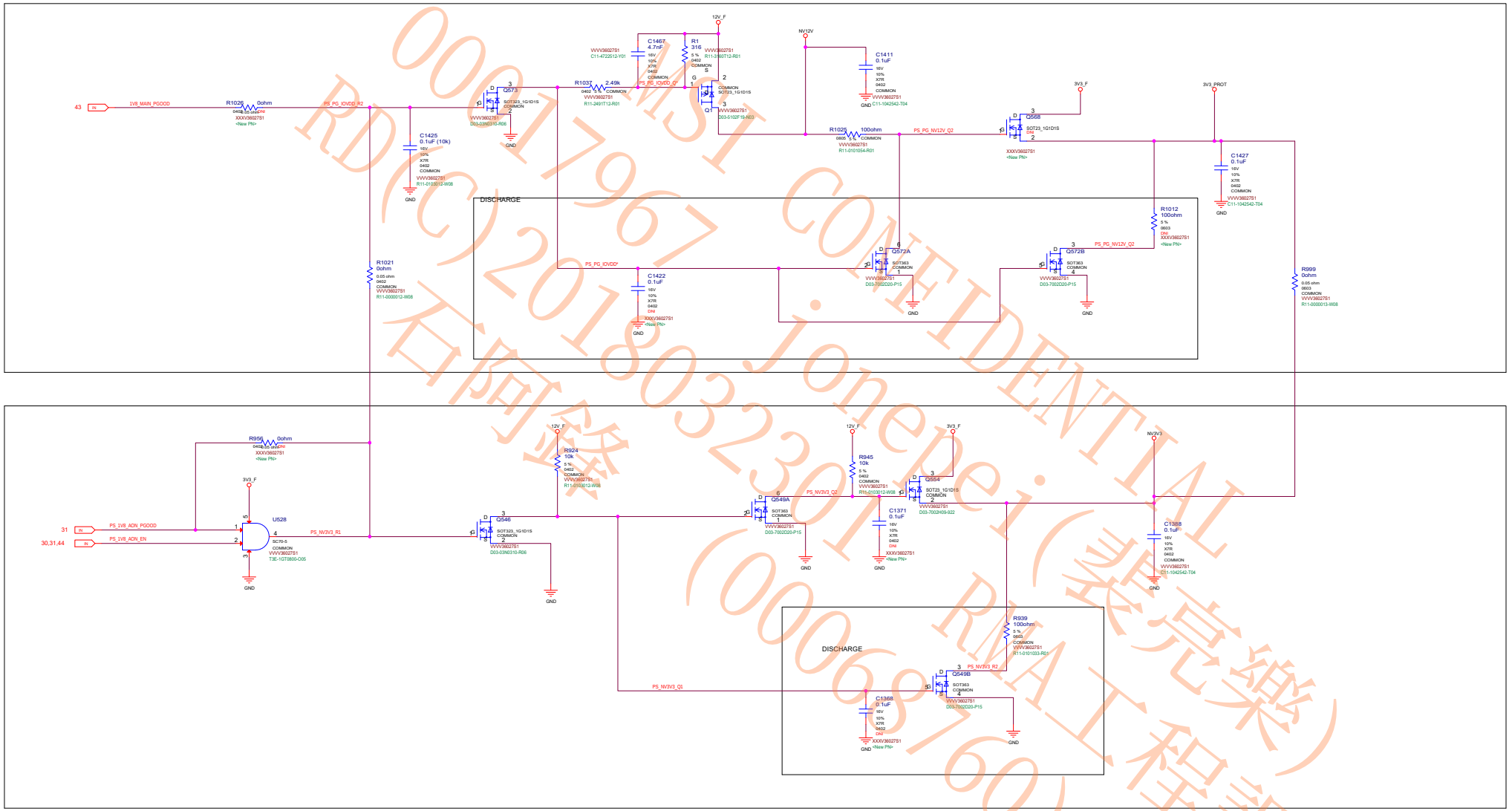
Remove LED HEADER(GEFORCE ONLY)

SLI LED (GEFORCE ONLY)





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Page47: MCU

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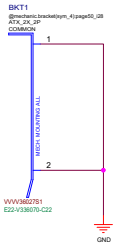
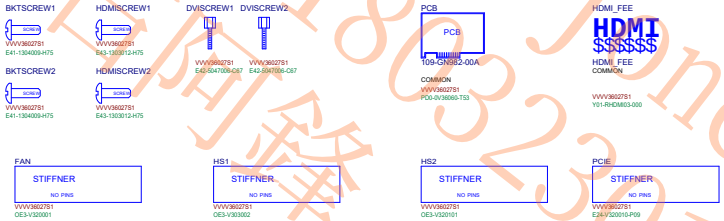
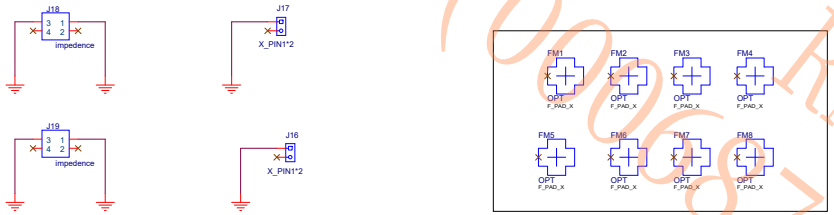
Brackets:

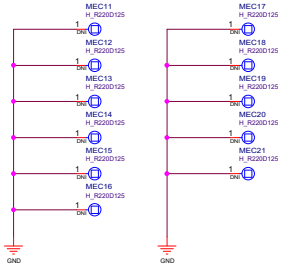


Screw

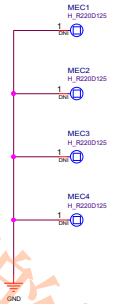




Mechanical Holes Symbol



GPU HOLES SYMBOL



MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: Mechanical: Bracket/Thermal Solution	Rev: 6.0
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Page49: VR THERMAL PROTECTION

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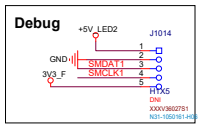
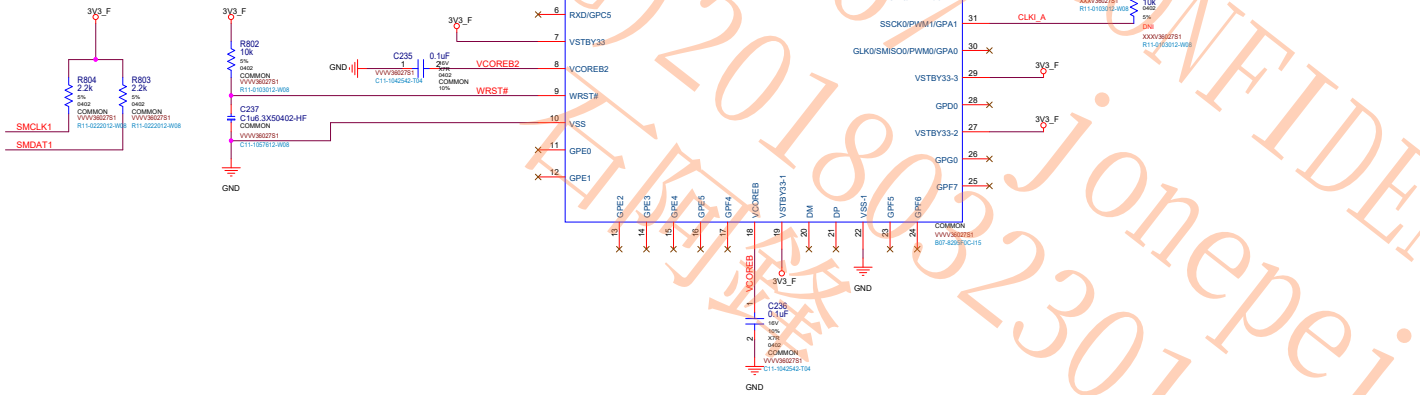
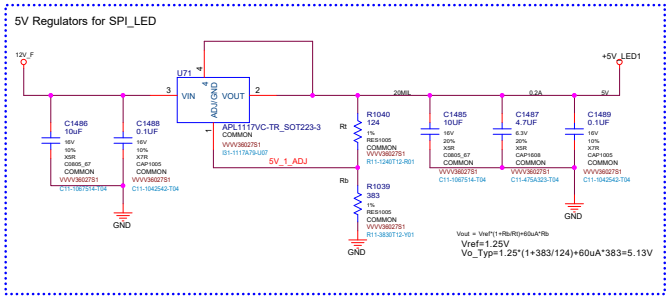
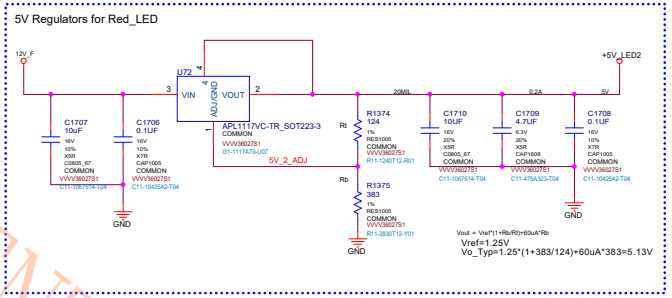
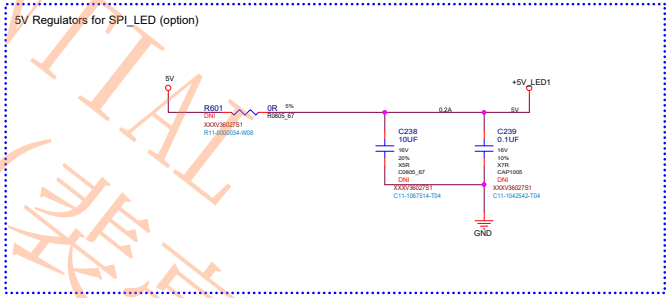
Page50: LED_CONTROLLER_ITE8295

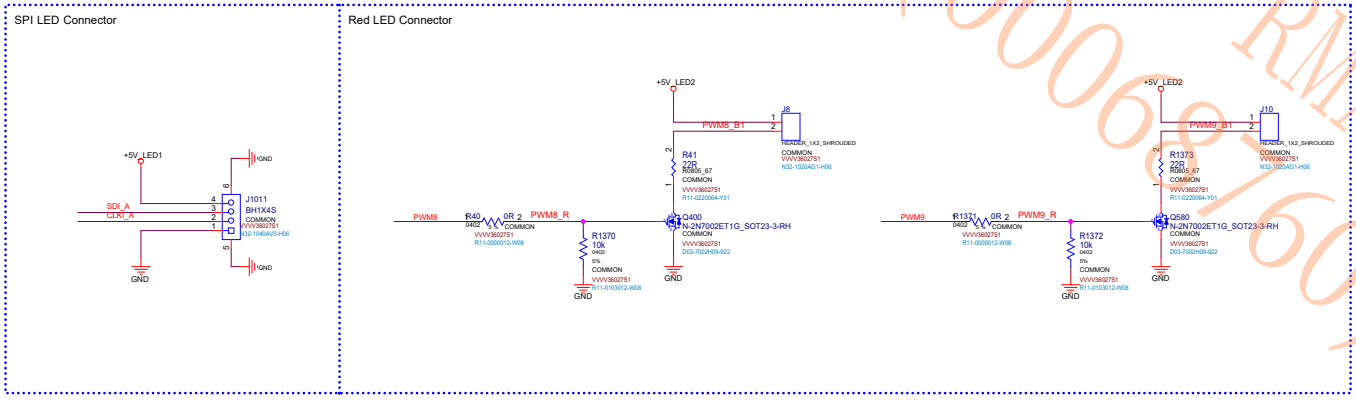












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