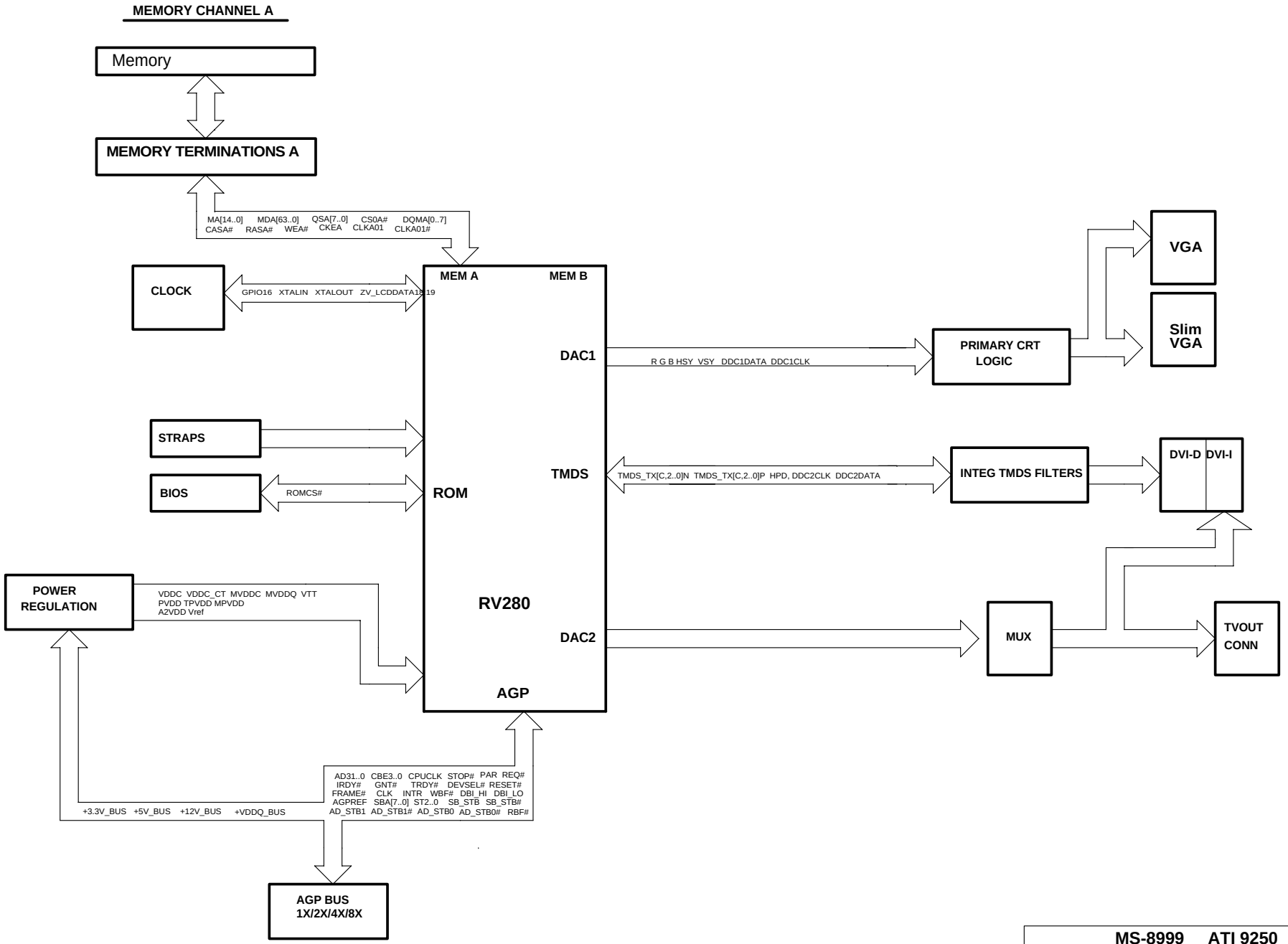


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|---|---|---|
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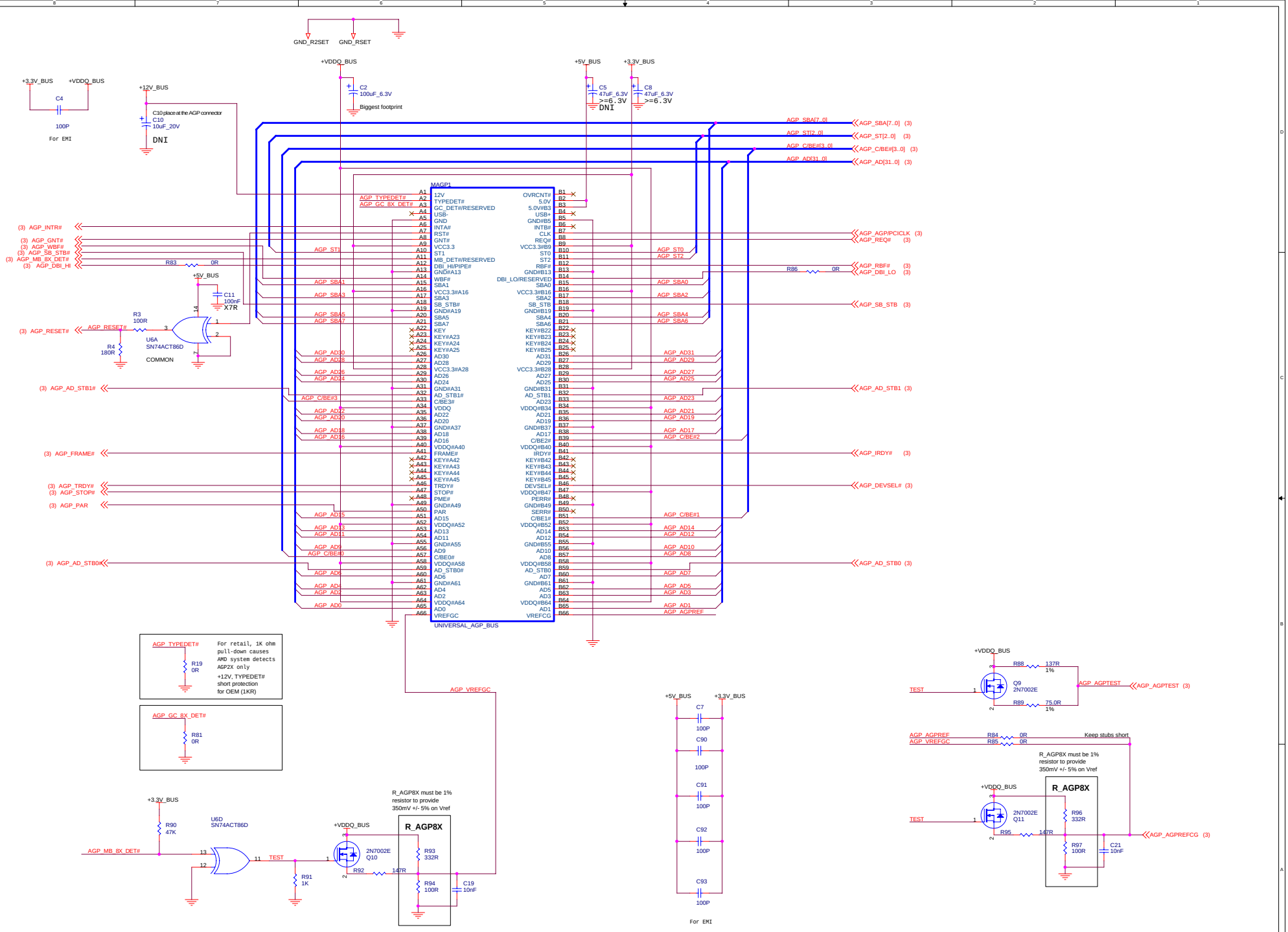
GND_R2SET
GND_RSET
+VDDQ_BUS
+5V_BUS
+3.3V_BUS
+12V_BUS
C2
100uF_6.3V
Biggest footprint
C5
47uF_6.3V
>=6.3V
DNI
C8
47uF_6.3V
>=6.3V
C4
100P
For EMI
C10 place at the AGP connector
C10
10uF_20V
DNI
MAGP1
12V
TYPEDET#
GC_DET#/RESERVED
USB-
GND
INTA#
RST#
GNT#
VCC3.3
ST1
MB_DET#/RESERVED
DBI_HI/PIPE#
GND#A13
WBF#
SBA1
VCC3.3#A16
SBA3
SB_STB#
GND#A19
SBA5
SBA7
KEY
KEY#A23
KEY#A24
KEY#A25
AD30
AD28
VCC3.3#A28
AD26
AD24
GND#A31
AD_STB1#
C/BE3#
VDDQ
AD22
AD20
GND#A37
AD18
AD16
VDDQ#A40
FRAME#
KEY#A42
KEY#A43
KEY#A44
KEY#A45
TRDY#
STOP#
PME#
GND#A49
PAR
AD15
VDDQ#A52
AD13
AD11
GND#A55
AD9
C/BE0#
VDDQ#A58
AD_STB0#
AD6
GND#A61
AD4
AD2
VDDQ#A64
AD0
VREFGC
OVRCNT#
5.0V
5.0V#B3
USB+
GND#B5
INT$#
CLK
REQ#
VCC3.3#B9
ST0
ST2
RBF#
GND#B13
DBI_LO/RESERVED
SBA0
VCC3.3#B16
SBA2
SB_STB
GND#B19
SBA4
SBA6
KEY#B22
KEY#B23
KEY#B24
KEY#B25
AD31
AD29
VCC3.3#B28
AD27
AD25
GND#B31
AD_STB1
AD23
VDDQ#B34
AD21
AD19
GND#B37
AD17
C/BE2#
VDDQ#B40
IRDY#
KEY#B42
KEY#B43
KEY#B44
KEY#B45
DEVSEL#
VDDQ#B47
PERR#
GND#B49
SERR#
C/BE1#
VDDQ#B52
AD14
AD12
GND#B55
AD10
AD8
VDDQ#B58
AD_STB0
AD7
GND#B61
AD5
AD3
VDDQ#B64
AD1
VREFCG
UNIVERSAL_AGP_BUS
AGP_SBA[7..0]
AGP_ST[2..0]
AGP_C/BE#[3..0]
AGP_AD[31..0]
(3) AGP_INTR#
(3) AGP_GNT#
(3) AGP_WBF#
(3) AGP_SB_STB#
(3) AGP_MB_8X_DET#
(3) AGP_DBI_HI
(3) AGP_RESET#
R83 0R
R86 0R
AGP_AGP/PCICLK (3)
AGP_REQ# (3)
AGP_RBF# (3)
AGP_DBI_LO (3)
AGP_SB_STB (3)
C11
100nF
X7R
R3
100R
R4
180R
U6A
SN74ACT86D
COMMON
(3) AGP_AD_STB1#
(3) AGP_FRAME#
(3) AGP_TRDY#
(3) AGP_STOP#
(3) AGP_PAR
(3) AGP_AD_STB0#
AGP_IRDY# (3)
AGP_DEVSEL# (3)
AGP_AD_STB1 (3)
AGP_AD_STB0 (3)
AGP_VREFGC
AGP_TYPEDET#
R19
0R
For retail, 1K ohm pull-down causes AMD system detects AGP2X only
+12V, TYPEDET# short protection for OEM (1KR)
AGP_GC_8X_DET#
R81
0R
UNIVERSAL VREFGC CIRCUIT (2X, 4X, 8X)
+3.3V_BUS
R90
47K
U6D
SN74ACT86D
AGP_MB_8X_DET#
TEST
R91
1K
+VDDQ_BUS
2N7002E
Q10
R92
147R
R_AGP8X must be 1% resistor to provide 350mV +/- 5% on Vref
R_AGP8X
R93
332R
R94
100R
C19
10nF
C7
C90
C91
C92
C93
100P
For EMI
R88
137R
1%
Q9
2N7002E
R89
75.0R
1%
AGP_AGPTEST
AGP_AGPTEST (3)
AGP_AGPREF
AGP_VREFGC
R84
R85
0R
Keep stubs short
R_AGP8X must be 1% resistor to provide 350mV +/- 5% on Vref
R_AGP8X
2N7002E
Q11
R95
147R
R96
332R
R97
100R
C21
10nF
AGP_AGPREFCG (3)
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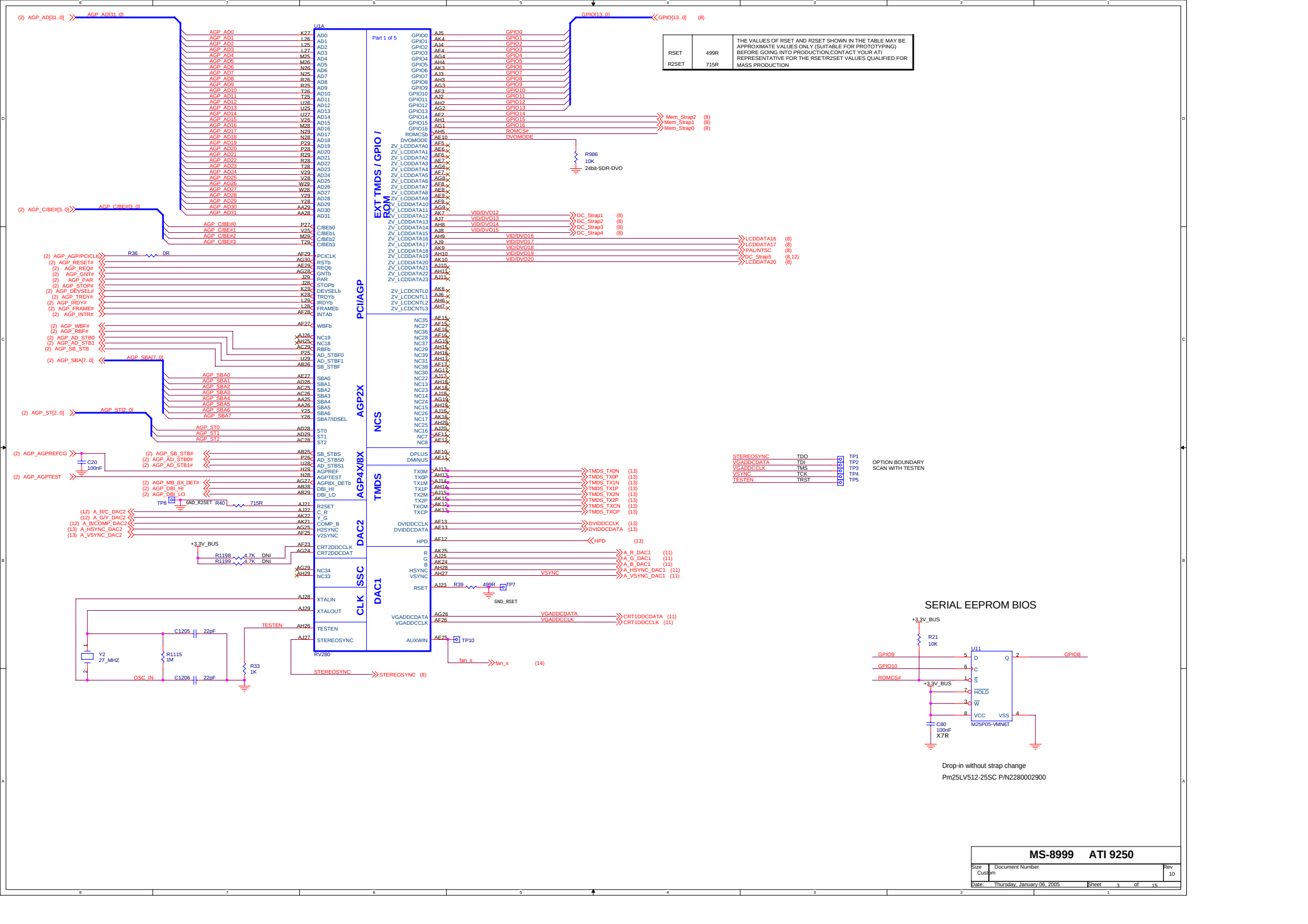
U1A
Part 1 of 5
PCI/AGP
AGP2X
AGP4X/8X
DAC2
SSC
CLK
DAC1
NCS
TMDS
EXT TMDS / GPIO / ROM
(2) AGP_AD[31..0]
AGP_AD[31..0]
(2) AGP_C/BE#[3..0]
AGP_C/BE#[3..0]
(2) AGP_SBA[7..0]
AGP_SBA[7..0]
(2) AGP_ST[2..0]
AGP_ST[2..0]
GPIO[13..0]
GPIO[13..0] (8)
R36 0R
R986 10K
24bit-SDR-DVO
Mem_Strap2 (8)
Mem_Strap1 (8)
Mem_Strap0 (8)
DC_Strap1 (8)
DC_Strap2 (8)
DC_Strap3 (8)
DC_Strap4 (8)
LCDDATA16 (8)
LCDDATA17 (8)
PALINTSC (8)
DC_Strap5 (8,12)
LCDDATA20 (8)
TMDS_TX0N (13)
TMDS_TX0P (13)
TMDS_TX1N (13)
TMDS_TX1P (13)
TMDS_TX2N (13)
TMDS_TX2P (13)
TMDS_TXCN (13)
TMDS_TXCP (13)
DVIDDCCLK (13)
DVIDDCDATA (13)
HPD (13)
A_R_DAC1 (11)
A_G_DAC1 (11)
A_B_DAC1 (11)
A_HSYNC_DAC1 (11)
A_VSYNC_DAC1 (11)
CRT1DDCDATA (11)
CRT1DDCCLK (11)
STEREOSYNC (8)
fan_s (14)
RSET 499R
R2SET 715R
THE VALUES OF RSET AND R2SET SHOWN IN THE TABLE MAY BE APPROXIMATE VALUES ONLY (SUITABLE FOR PROTOTYPING) BEFORE GOING INTO PRODUCTION,CONTACT YOUR ATI REPRESENTATIVE FOR THE RSET/R2SET VALUES QUALIFIED FOR MASS PRODUCTION
STEREOSYNC TDO TP1
VGADDCDATA TDI TP2
VGADDCCLK TMS TP3
VSYNC TCK TP4
TESTEN TRST TP5
OPTION BOUNDARY SCAN WITH TESTEN
SERIAL EEPROM BIOS
+3.3V_BUS
R21 10K
GPIO9
GPIO10
ROMCS#
GPIO8
U11
M25P05-VMN6T
C80 100nF X7R
Drop-in without strap change
Pm25LV512-25SC P/N2280002900
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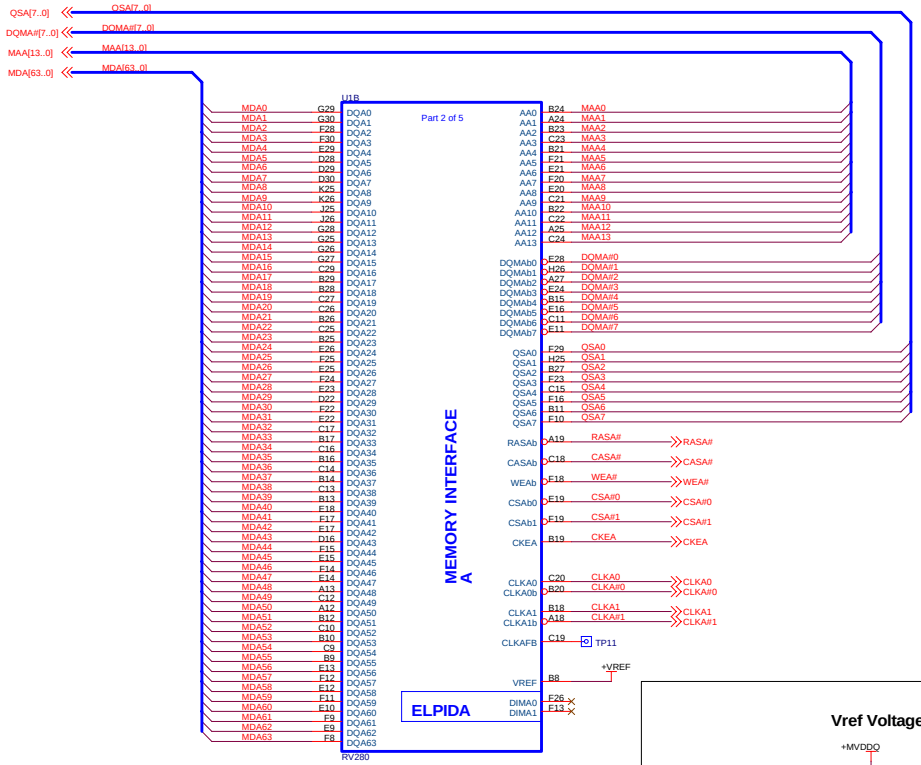
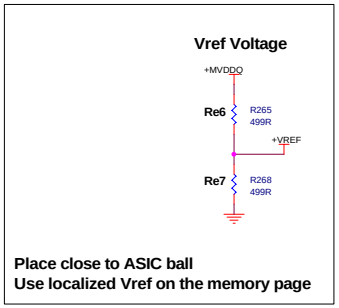
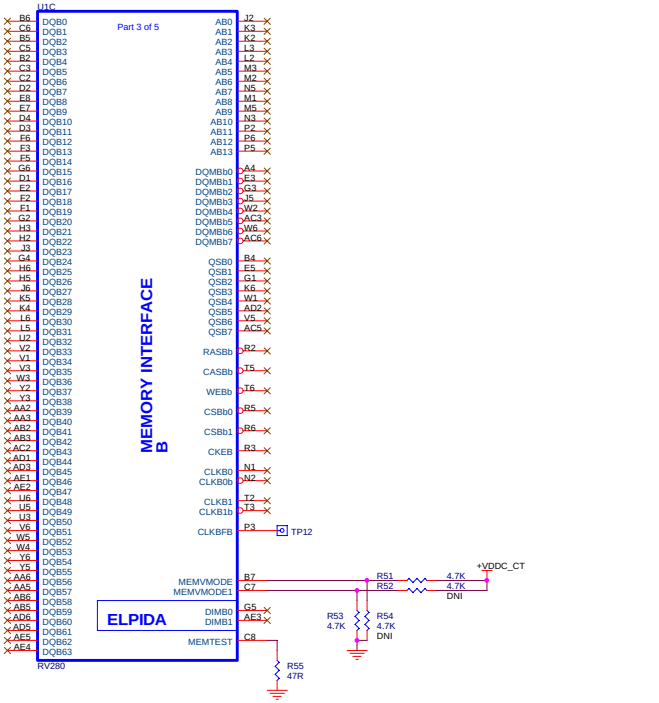
## MEMORY CHANNEL A

## MEMORY CHANNEL B




| MEMVMODE[1-0] | MEMORY IO VOLTAGE | |
|---|---|---|
| 0 1 | 2.5V (DDR) | Default |
| 1 0 | 1.8V (DDR) | |
| 1 1 | 3.3V (SDR) | |

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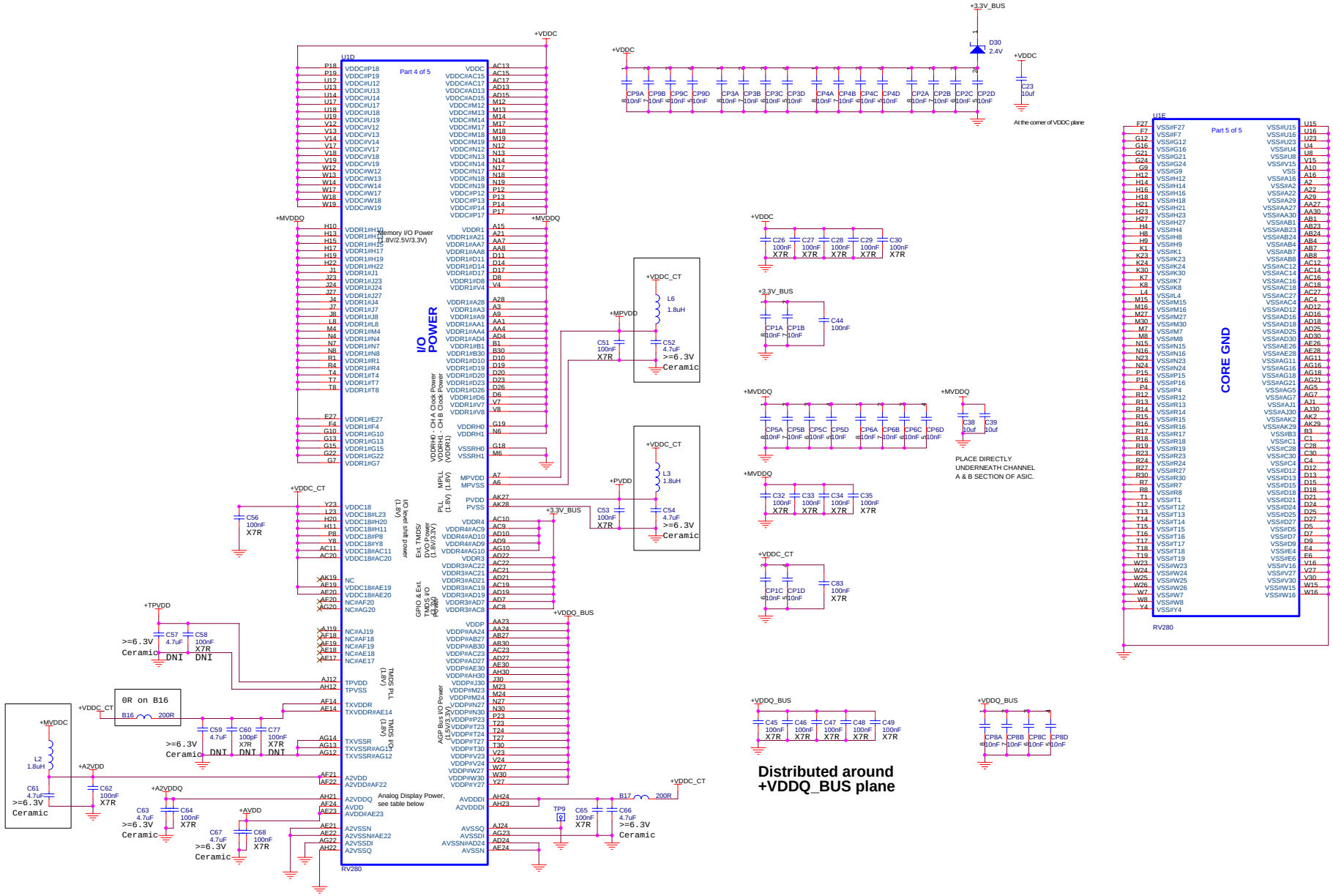


| Pin Names | +AVDD | Matching Ground | +A2VDD | Matching Ground | +A2VDDQ | Matching Ground | +AVDDDI +A2VDDDI | Matching Ground |
|---|---|---|---|---|---|---|---|---|
| Voltage | 1.8V | | 2.5V | | 1.8V | | 1.8V | |
| Usage | DAC1 VDD (80mA) | AVSSN (Noisy) | DAC2 VDD (120mA) | A2VSSN (Noisy) | DAC2 Band Gap Ref. | A2VSSQ (Quiet) | Digital Power for DAC1 and DAC2 | AVSSDI A2VSSDI (Digital) |
| | DAC1 Band Gap Ref. | AVSSQ (Quiet) | | | | | | |
| Board power and ground option(s) | AVDD sourced from VDDC_CT thru bead at least 15 mil trace and not longer than 1.5 inch. AVSSN and AVSSQ with single via to GND close to the pin. | | (1) A2VDD regulated source and A2VSSN return path routed with at least 15 mil trace and not longer than 1.5 inch. AVSSN with single via to GND at the regulator. (2) Sourced from VDD thru bead instead of the regulator | | Source from AVDD thru bead. A2VSSQ with sigle via to GND close to the pin. | | Source from VDDC_CT thru bead | |

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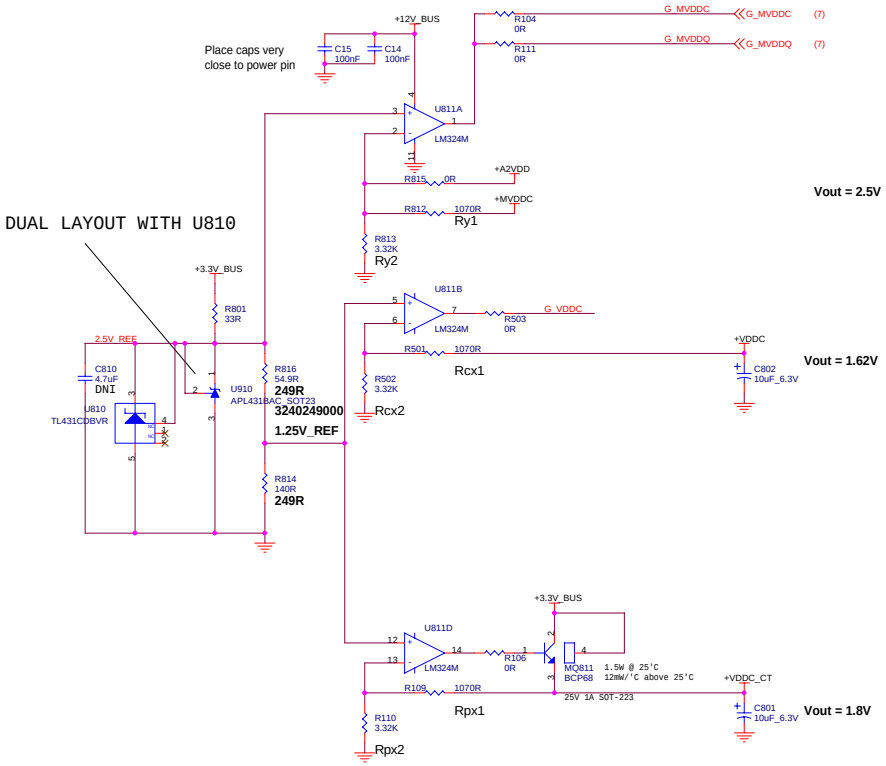



**Regulator for VDDC_CT (Core Transform) and AVDD/A2VDDQ/AVDDDI/A2VDDDI TXVDDR, LVDDRx, MPVDD**

**Vin = 3.3V AGP**
**Vout = 1.8V**
**Iout = 350mA + 100mA + 50mA = 500mA MAX**
**Iout = 600mA MAX (with PVDD/TPVDD)**

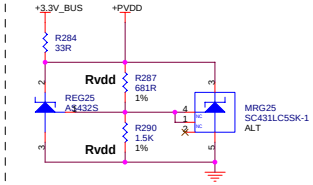
**Regulator for PVDD (Core PLLs) and optional TPVDD (TMDS PLLs)**

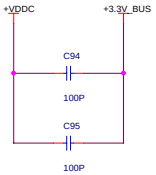
**Vin = 3.3V AGP**
**Vout = +1.8V**
**Iout = 25mA MAX (PVDD only)**
**Iout = 30mA MAX (PVDD + TPVDD)**

| | Rct1 | | Rct2 | | |
|---|---|---|---|---|---|
| 1.8V | 1K | 3240100100 603 | 422R | 3240422000 | 603 |
| 1.9V | | | 499R | 3240499000 | 603 |

The value of resistor were chosen to reduce failure rate caused by possible defective regulators, i.e., 33R are used instead of 47R or 51R for more start up current. (3.465V - 1.8V) / 33R = 50.5mA

805 package resistor are required for sufficient power rating (0.1W rating). (3.465V - 1.8V) * 50.5mA = 0.085W; therefore, smaller resistor value would require 1206 package



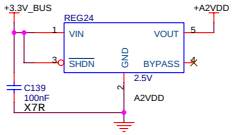




For EMI

**Regulator For A2VDD (2nd DACs)**

**Vin = +3.3V AGP**
**Vout = 2.5V**
**Iout = 150mA MAX**

A2VDD might not be needed if VDD can provide stable 2.5V




**TC1185**

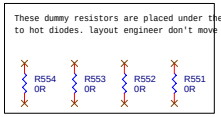
A2VDD and A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch. A2VSSN with signle via to GND at the regulator

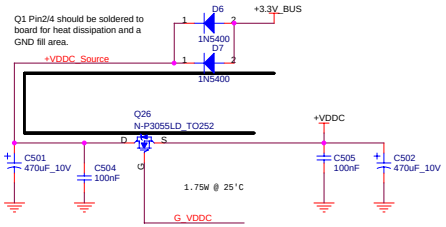
| | Range | Rpx1 | Rpx2 |
|---|---|---|---|
| 1.8V | 1.805V ~ 1.827V | 1K 3240100100 | 2.21K 3240221100 |
| | | | |

**Buffered Shount Regulator for VDDC**
**Vin = 3.3V**
**Vout = 1.62V or Adjustable**
**Iout = 3A MAX**

| +VDDC | Range | Rcx1 Rc1 | Rcx2 Rc2 |
|---|---|---|---|
| 1.62V | 1.619V ~ 1.635V | 1K 3240100100 | 3.32K 3240332100 |
| | | | |

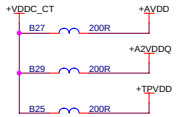
These dummy resistors are placed under the diodes to avoid PCB heat damage due to hot diodes. layout engineer don't move these components' position




**AVDD/A2VDDQ (1st DAC & 2nd DAC Band Gap)**

**TPVDD**

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**Buffered Shunt Regulator for MVDDQ & VDDR1**
**Vin = 3.3V AGP**
**Vout = 2.5V**
**Iout = 1200mA MAX**
**Iout = 1000mA Est. MAX**

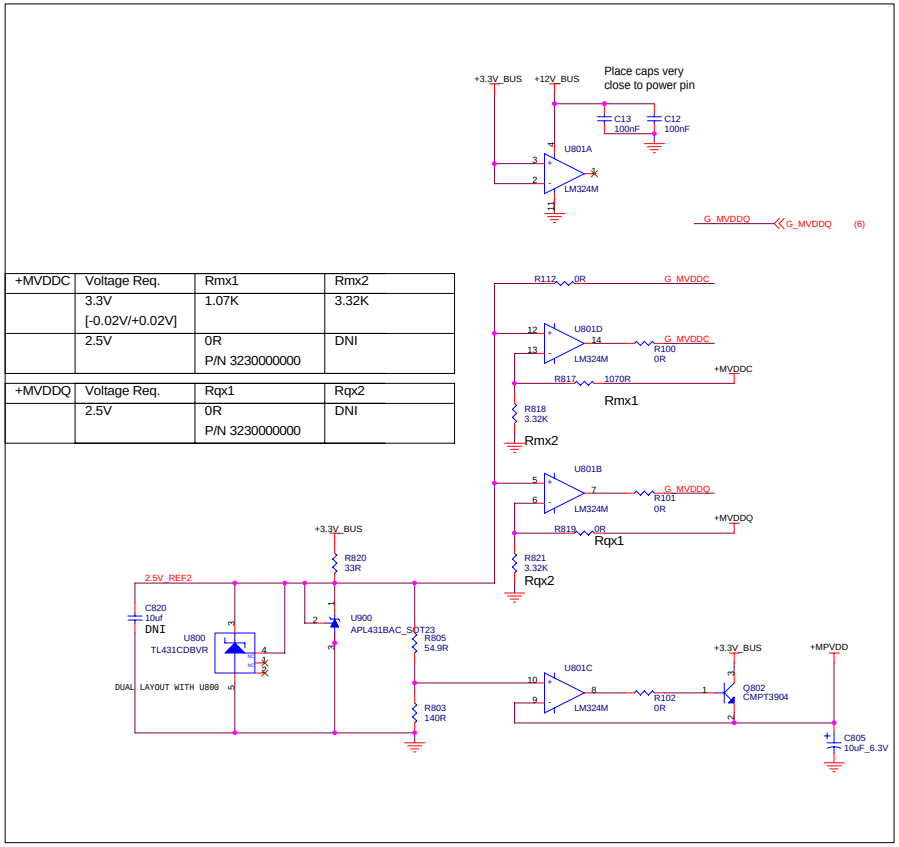
| Type | Voltage Req. | Rq1 | Rq2 |
|---|---|---|---|
| Elpida | 1.8V [-0.09V/+0.18V] | 681R 3240681000 | 1.5K 3230015200 |
| | 2.5V | 1K 3240100100 | 1K 3240100100 |
| | 2.6V | 4.75K 3240475100 | 4.32K 3240432100 |

**Buffered Shount Regulator for MVDDC**
**Vin = 5V**
**Vout = 3.3V**
**Iout = 1.4A MAX**

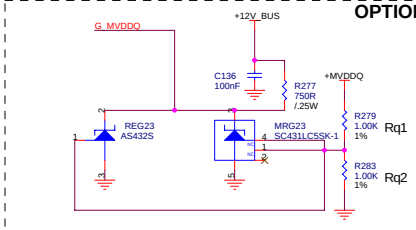
| | Voltage Req. | Rm1 | Rm2 |
|---|---|---|---|
| Hynix | 3.22V [-0.04V/+0.04V] | 4.32K P/N 3240432100 | 2.74K P/N 3240274100 |
| | 3.34V [-0.04V/+0.04V] | 4.32K P/N 3240432100 | 2.55K P/N 3240255100 |
| | 3.45V [-0.04V/+0.04V] | 4.32K P/N 3240432100 | 2.43K P/N 3250243100 |
| Sumsung | 2.56V [-0.03V/+0.03V] | 2.55K P/N 3240255100 | 2.43K P/N 3250243100 |

| +MVDDC | Voltage Req. | Rmx1 | Rmx2 |
|---|---|---|---|
| | 3.3V [-0.02V/+0.02V] | 1.07K | 3.32K |
| | 2.5V | 0R P/N 3230000000 | DNI |

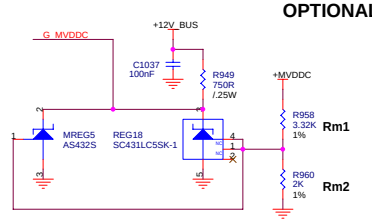
| +MVDDQ | Voltage Req. | Rqx1 | Rqx2 |
|---|---|---|---|
| | 2.5V | 0R P/N 3230000000 | DNI |

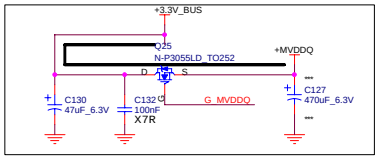



**OPTIONAL**



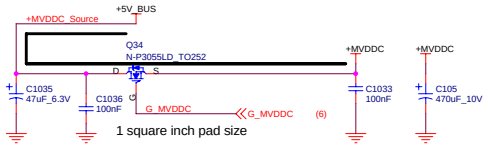

**OPTIONAL**

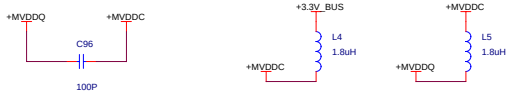



no stuff

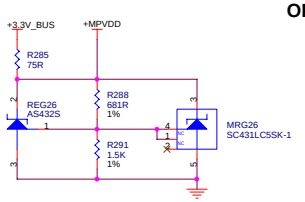
Q34 Pin2/4 should be soldered to board for heat dissipation and a GND fill area.




**Buffered Shunt Regulator for MPVDD**
**Vin = 3.3V**
**Vout = 1.8V**
**Iout = 10mA MAX**

**OPTIONAL**

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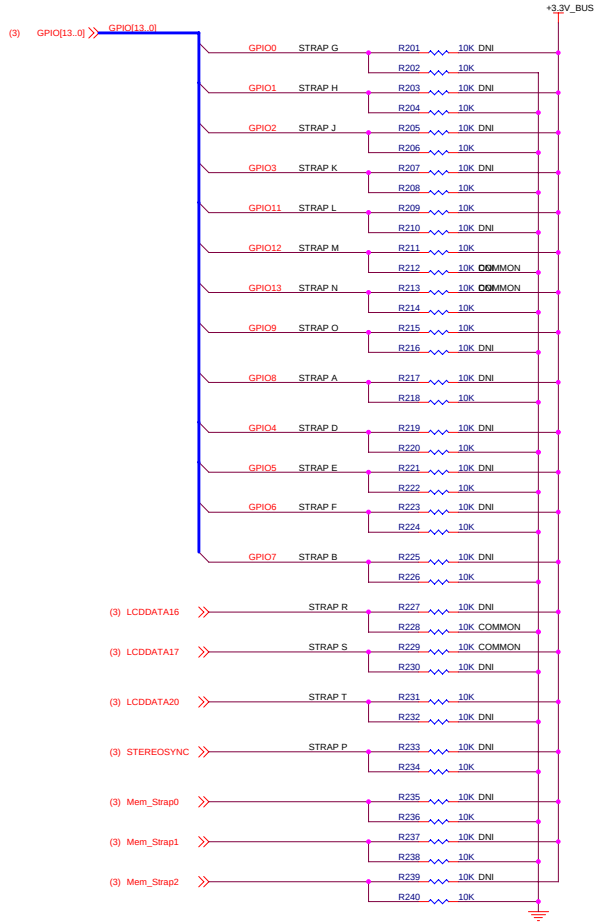
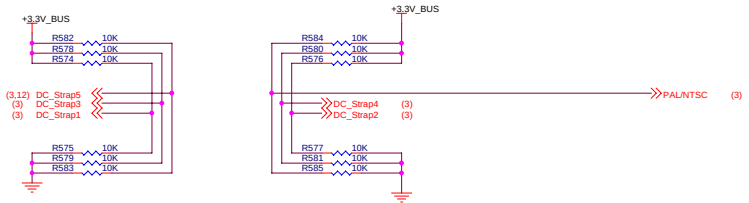



# OPTION STRAPS

| STRAPS | PIN | DESCRIPTION | DEFAULT |
|---|---|---|---|
| AGPFBSKEW(1:0) | GPIO(1:0) | AGP 1x clock feedback phase adjustment wrt refclk(cpuclk)<br>**00 - refclk slightly earlier then feedback**<br>01 - refclk 1 tap earlier then feedback<br>10 - refclk 1 tap later then feedback<br>11 - refclk 2 taps earlier then feedback clock | 00<br>(internal pull-down) |
| X1CLK_SKWE(1:0) | GPIO(3:2) | Clock phase adjustment between x1 clk and x2clk<br>**00 - 0 tap delay**<br>01 - 1 tap delay<br>10 - 2 taps delay<br>11 - 3 taps delay | 00<br>(internal pull-down) |
| ROMIDCFG(3:0) | GPIO(9,13:11) | If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type<br>0000 - No ROM, CHG_ID=0<br>0001 - No ROM, CHG_ID=1<br>0100 - reserved<br>0110 - reserved<br>1000 - Parallel ROM, chip IDis from ROM<br>1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM<br>1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM<br>**1011 - Serial M25P05/10 ROM (ST), chip IDis from ROM**<br>1100 - Reserved<br>1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM | 1100 |
| ID_DISABLE | GPIO(8) | **0 - Normal operation**<br>1 - Shuts the chip down by not responding to any config cycles<br>In a system with two graphics chips, one on the motherboard,<br>the other on add-in card, the strap can be used to disable one of the two throught a jumper. | 0<br>(internal pull-down) |
| BUSCFG(2:0) | GPIO(6:4) | Controls bus type, CLK PLL select, and IDSEL<br>**000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16**<br>000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16<br>001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17<br>001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17<br>010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16<br>010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16<br>011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17<br>011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17<br>100 - PCI 66MHz, PLL clk<br>101 - PCI 33MHz, 3.3v, REF clk<br>110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16<br>110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16<br>111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17<br>111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17<br>Note that for AGP configurations GPIO(4) acts as the IDSEL strap.<br>For PCI it acts as the PLL bypass (33 or 66MHz) strap. | 000<br>(internal pull-down) |
| VGA_DISABLE | GPIO(7) | **0 - VGA controller capability enabled.**<br>1 - The device will not be recognized as the systemis VGA controller. | 0 |
| MULTIFUNC(1:0) | LCDDATA(17:16) | Multi-function device select<br>00 - single function device.<br>01 - two function device. No AGP in either function<br>**10 - two function device. AGP only in function 0**<br>11 - two function device. AGP in both functions<br>If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function.<br>See AGP function table below for detail on AGP ability claims. | 10 |
| VIP_DEVICE | LCDDATA(20)<br>STRAP T | Indicates if any slave VIP host devices drove this in low during reset.<br>**0 - Slave VIP host port devices present**<br>1 - No slave VIP host port devices reporting presence during reset | 0 |

| STRAP P | INTERRUPT |
|---|---|
| LOW | **ENABLED (DEFAULT)** |
| HIGH | DISABLED |

## Daughter Card Straps




| STRAPS | PIN | DESCRIPTION |
|---|---|---|
| DC_STRAP1 | LCDDATA12 | Internal TMDS Enabled<br>**0 - Disabled**<br>1 - Enabled |
| DC_STRAP2 | LCDDATA13 | Video Capture Enabled<br>**0 - Disabled**<br>1 - Enabled |
| DC_STRAP4 DC_STRAP5 | LCDDATA15 LCDDATA19<br>0 0<br>0 1<br>1 0<br>1 1 | DAC2 Configuration<br>DAC2 Off<br>DAC2 On as CRT<br>DAC2 On as TVOUT<br>DAC2 On as TVOUT and CRT |
| DC_STRAP6 | LCDDATA18 | TVO Standard Default (Resistor pull-up and switch short to GND)<br>0 - PAL (on board resistor pull-down and switch closed)<br>1 -NTSC (on board resistor pull-up) |

**MS-8999 ATI 9250**

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|---|---|---|
| Custom | | 10 |

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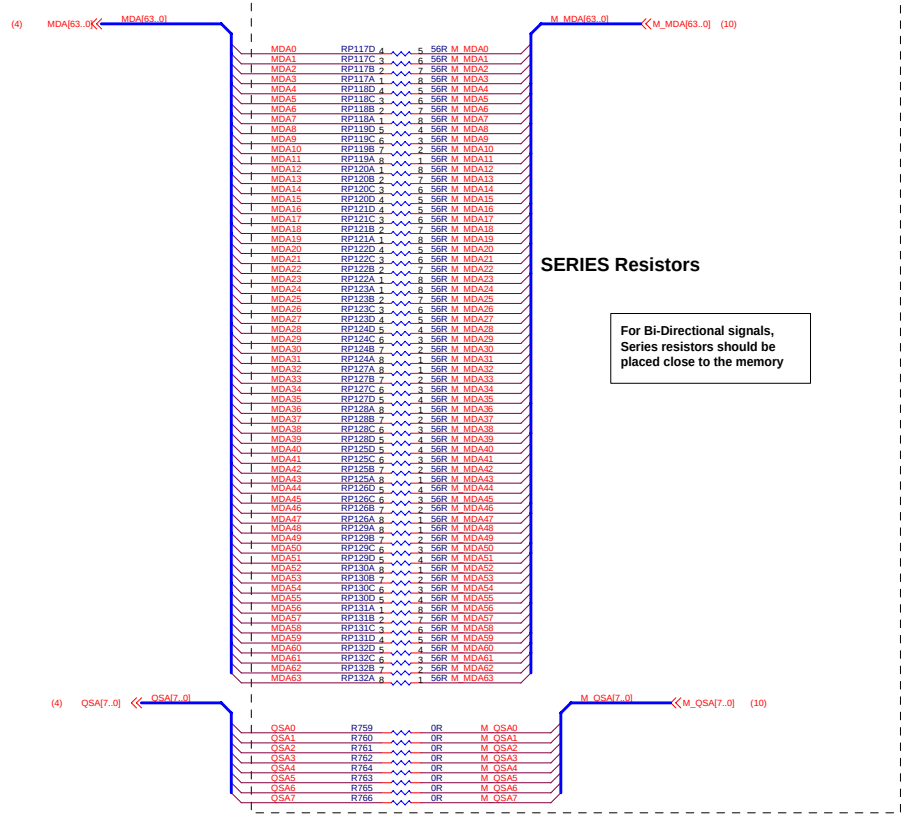
**TERMINATION FOR MEMORY CHANNEL A**




**SERIES Resistors**

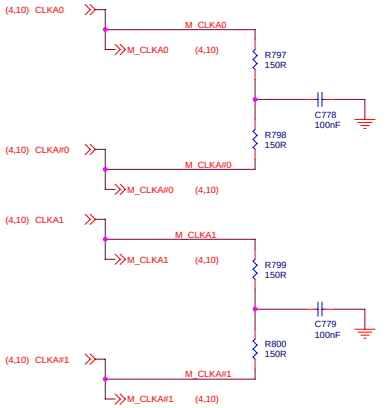
**For Bi-Directional signals, Series resistors should be placed close to the memory**

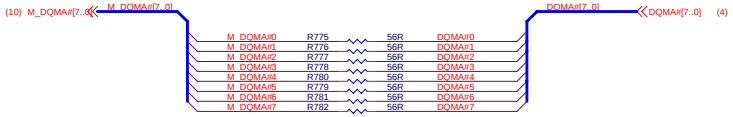
**Proper Termination of QSA?**

# CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory




**For Uni-Directional signals, Series resistors should be placed close to the ASIC**

**MS-8999 ATI 9250**

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|---|---|---|
| Custom | | 10 |

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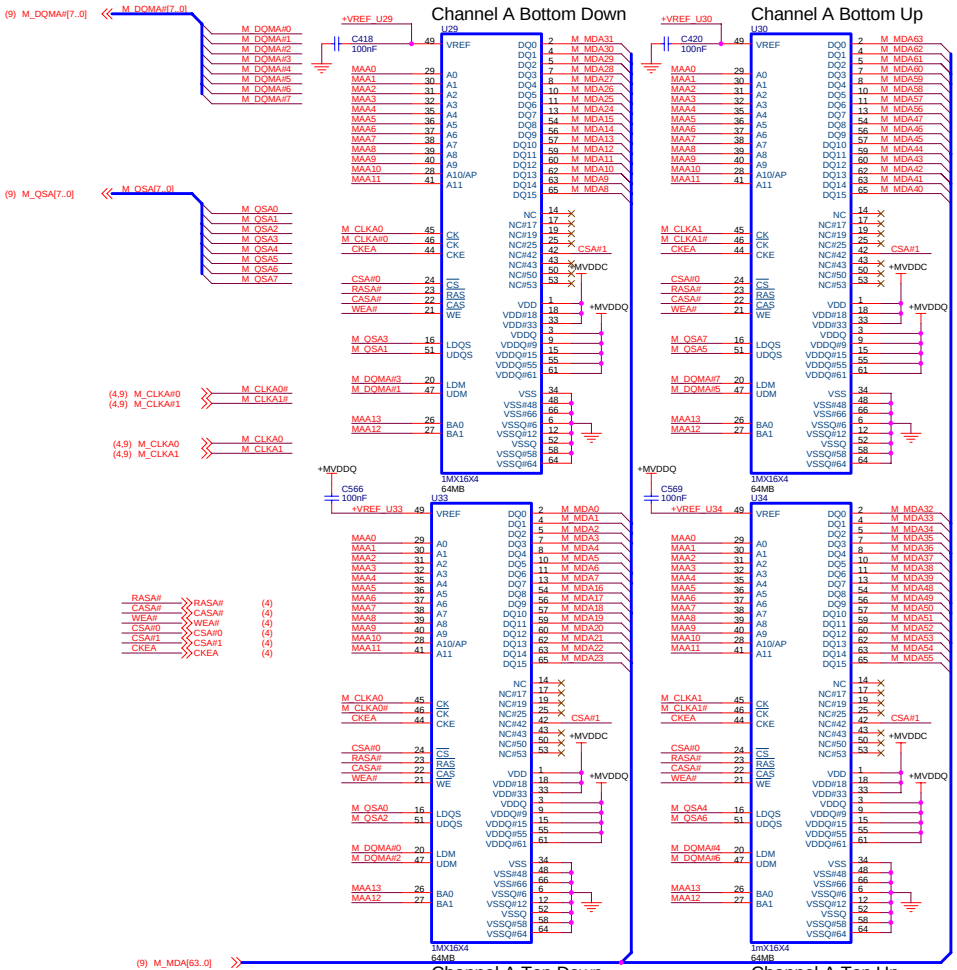
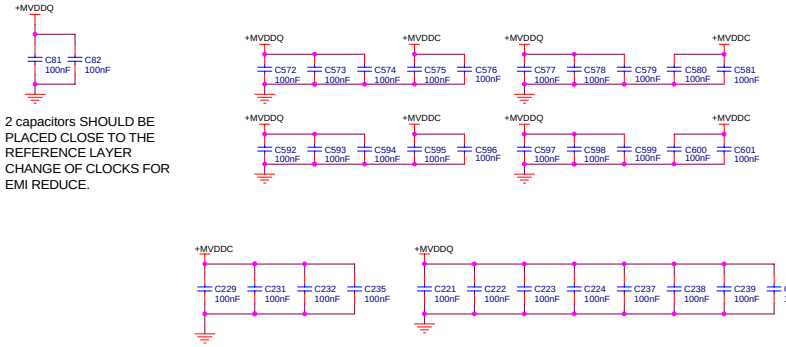



Put 1 1uF cap per power pin of memory




2 capacitors SHOULD BE PLACED CLOSE TO THE REFERENCE LAYER CHANGE OF CLOCKS FOR EMI REDUCE.

Part number for 8Mx16: 2354274204 (Samsung)

DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

**MS-8999 ATI 9250**

| Size | Document Number | Rev |
|---|---|---|
| C | | 10 |

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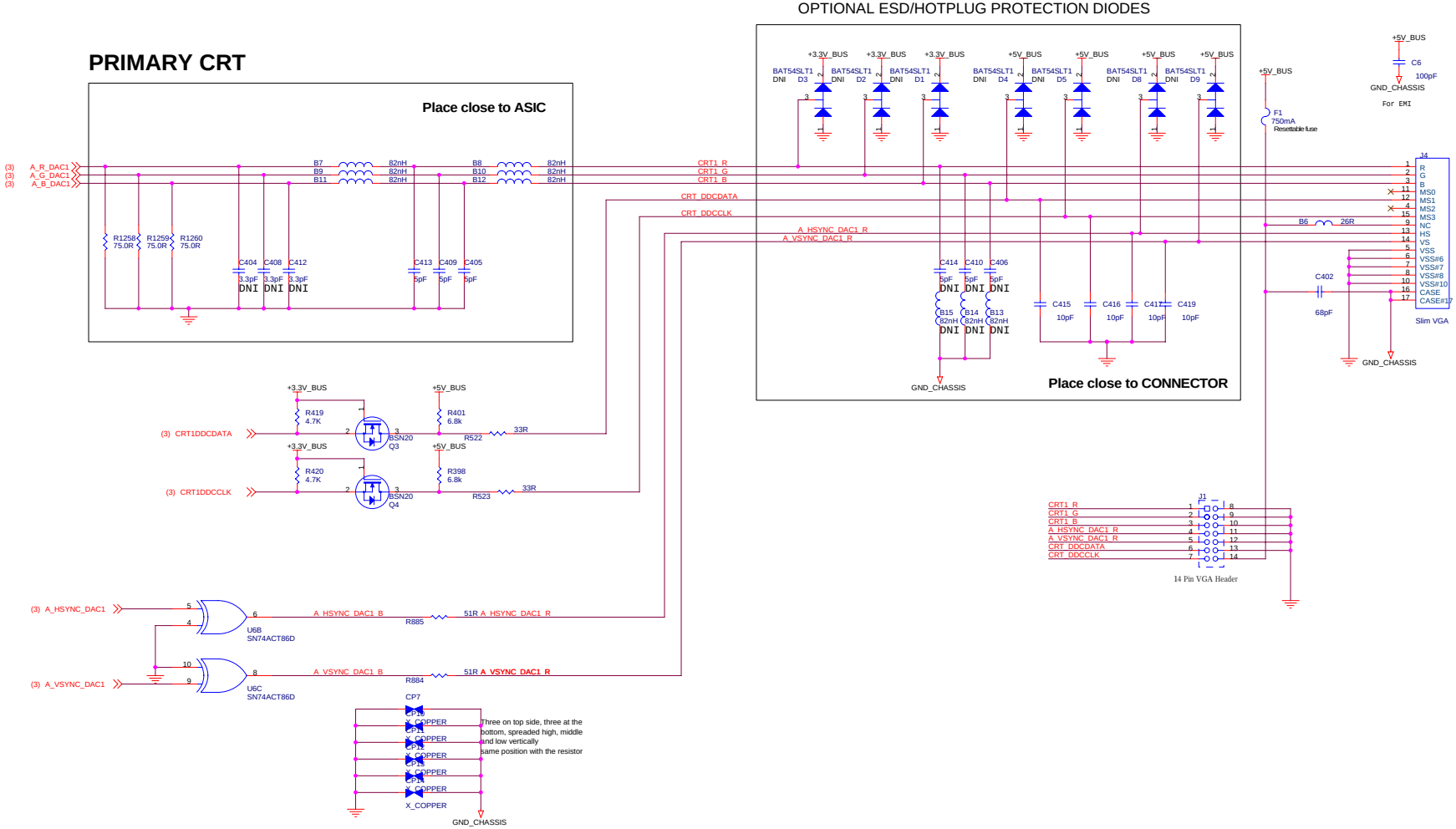
# PRIMARY CRT




| | | |
|---|---|---|
| **MS-8999 ATI 9250** | | |
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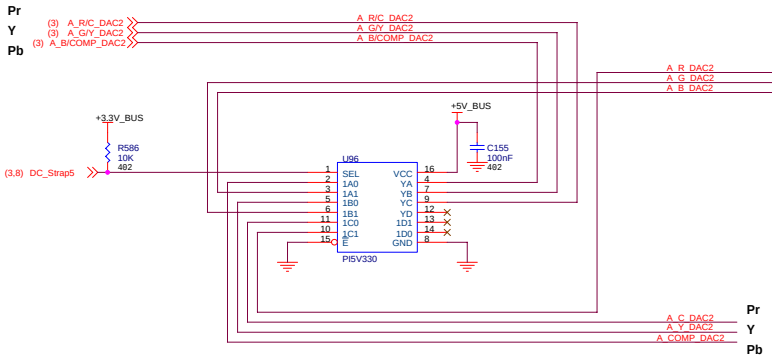
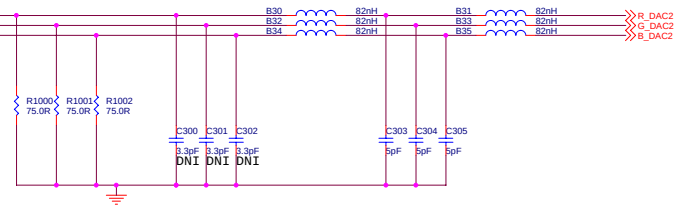
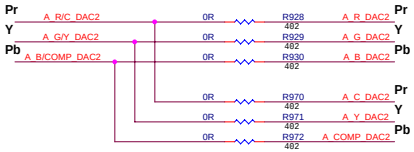
Place close to ASIC



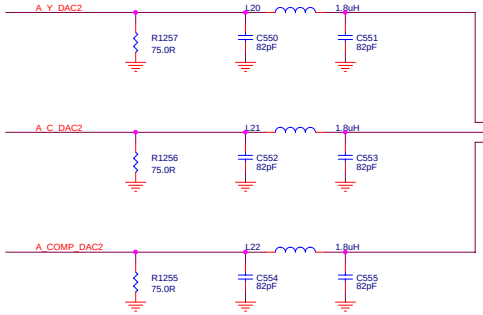

Place close to ASIC




MUX BYPASS



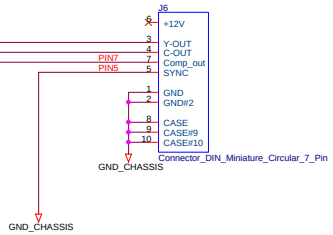

**Place Resistors close to ASIC.**




Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI



**TV Out (SVHS)**




| MS-8999 ATI 9250 | | |
|---|---|---|
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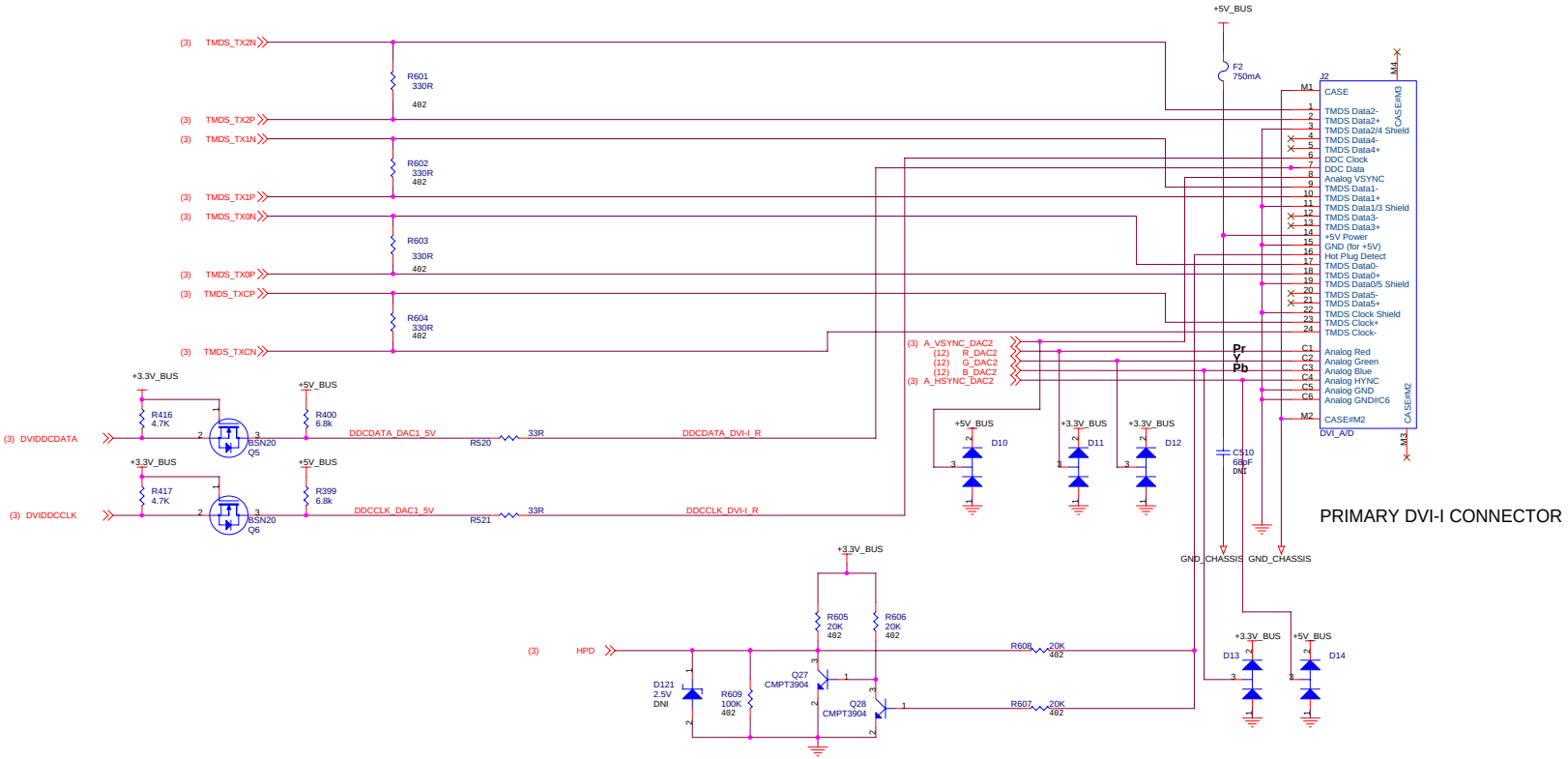
| Date: Thursday, January 06, 2005 | Sheet 12 of 15 | |




PRIMARY DVI-I CONNECTOR

| | | |
|---|---|---|
| **MS-8999 ATI 9250** | | |
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CRT SCREWS

ASSY1

SCREW
JACKSCREW
ASSY

ASSY2

SCREW
JACKSCREW
ASSY

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM4 SW_FB
FM5 SW_FB
FM6 SW_FB
FM7 SW_FB
FM8 SW_FB

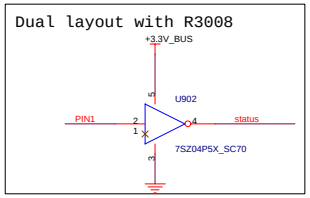
CABLE
D-Sub Cable
D-sub Cable

STD COMMON SCREW-1
MEC_SCREW
STD COMMON SCREW-2
MEC_SCREW
STD COMMON SCREW-3
MEC_SCREW
STD COMMON SCREW-4
MEC_SCREW

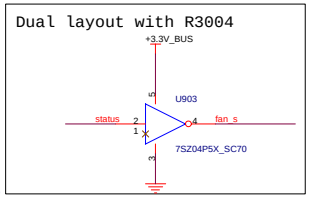
## Heatsink

MH101
HEATSINK

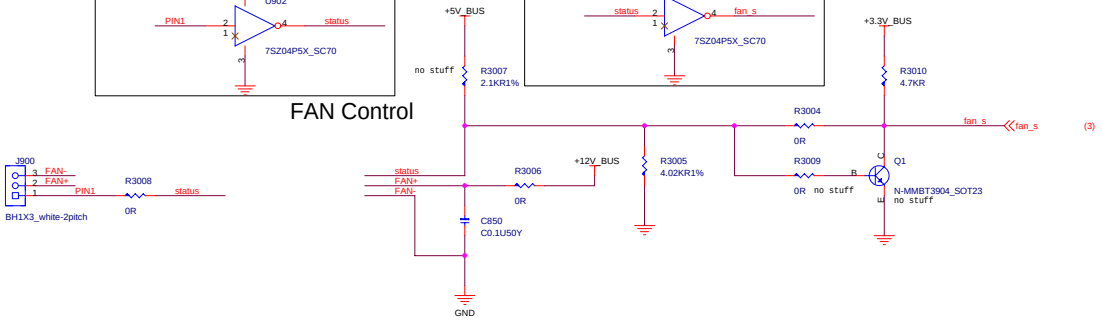
Dual layout with R3008




Dual layout with R3004




FAN Control




| | | |
|---|---|---|
| **MS-8999 ATI 9250** | | |
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<Variant Name>

| Title | Schematic No. | Date: |
|---|---|---|
| RV280 LP AGP8x 128MB 16Mx16 DDR | 105-A165XX-00 | **Thursday, January 06, 2005** |

# REVISION HISTORY

Rev 10

| Sch Rev | | Date | REVISION DESCRIPTION |
|---|---|---|---|
| 0 | 00A | 03/25/03 | Based on 105-A062xx-00 schematic<br>(pg2) Add pull-up on CS# for flashrom<br>(pg5) Replace swiching VDDC regulator with Op-Amp regulator circuit<br>(pg5) Add Op-Amp regulator circuit for low-cost design<br>(pg6) Add Op-Amp regulator circuit for low-cost design<br>(pg6) Remove C317 Thru-hole Alum. Cap for MVDDC<br>(pg6) Add +3.3V_BUS directly to +MVDDC option<br>(pg11) Modify VO connector filter chassis ground connections |
| | | 04/01/03 | (pg5) Replace VDDC 470uF with thru-hole<br>(pg6) Add thru-hole 470uF on +MVDDC for option |
| | | 04/10/03 | (pg6) Remove C1, C17 and C1034 |
| 1 | 00B | 05/14/03 | (pg5) Remove Q811 and Q814<br>(pg6) Add C805 10uF tant. cap on +MPVDD<br>(pg6) Add R112 to bypass opamp for +MVDDC<br>(pg6) Remove diodes (D10 and D11) and resistors (R111, R1261, R1262, R1263 and R1264) for +MVDDC<br>(pg5, 6) Add R104 to drive +MVDDC from alternate shunt reference<br>(pg7) Add jumper J1 for PAL TVO default<br>(Layout) Add silscreen for switch and jumper<br>(Layout) Correct MiniDIN J6 footprint<br>(Layout) Correct diode clearance for manufacturing request<br>(Layout) Move sticker location |
| 2 | 00 | 05/30/03 | (pg9) Replace a 2-pin with a 3-pin jumper for NTSC/PAL section.<br>(pg5) Add R812, R813 and R815 for +MVDDC voltage adjustment<br>(Layout) Change footprint of P/N4238010600 |