P361 A00 Base Design

P361-A00, G92, 8Mx32/16Mx32 GDDR3
HDMI, D-SUB, DVI

Table of Contents:

REV HISTORY (BASE ON V154 40)

2009/10/30
1. Remove TV-out circuit P13
2. Add HDMI circuit P13
3. Add D-SUBcircuit P11
4. Remove DVI circuit(J3) P12

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VAR	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10361-base-000	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0051	600-10361-0051-000	P361 G92-280B1 1024MB GDDR3 16Mx32 DVI-I+DVI-I
2	SKU0050	600-10361-0050-000	P361 G92-289B1 512MB GDDR3 16Mx32 DVI-I+DVI-I
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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PAGE DETAIL	Overview

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ID		PAGE	
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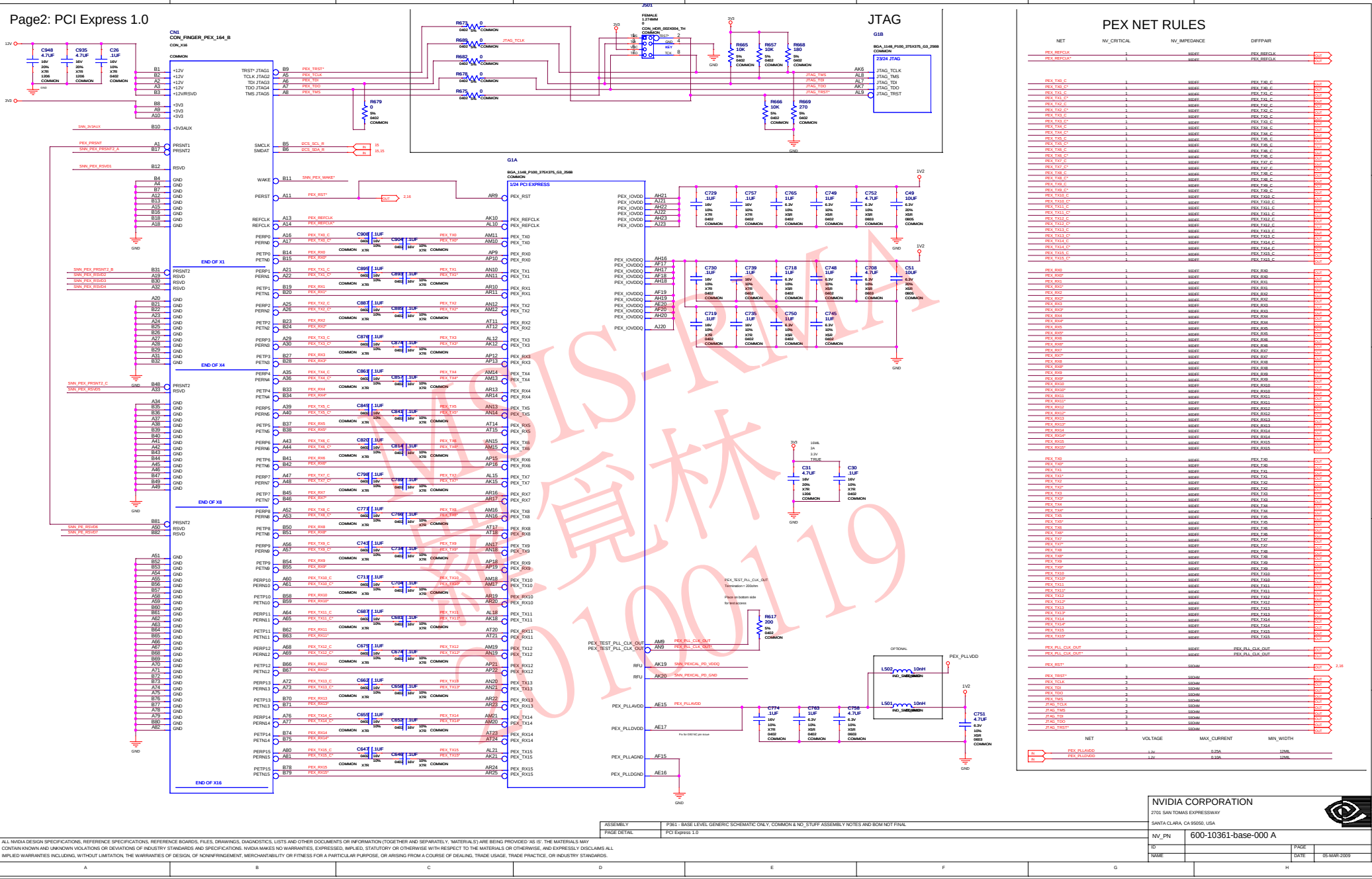

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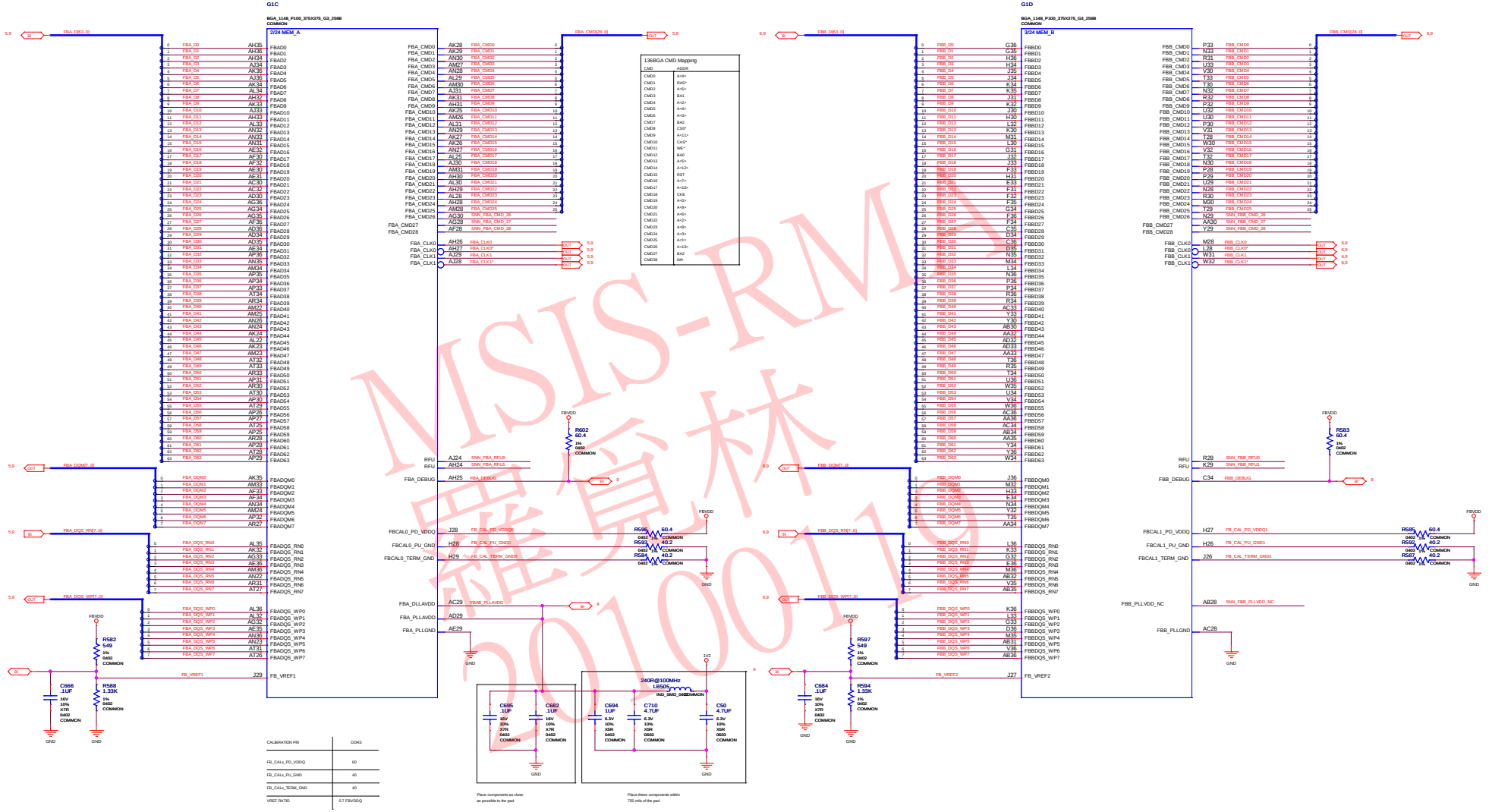
Page3: MEMORY: GPU Partition A/B



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PAGE DETAIL	MEMORY: GPU Partition A/B

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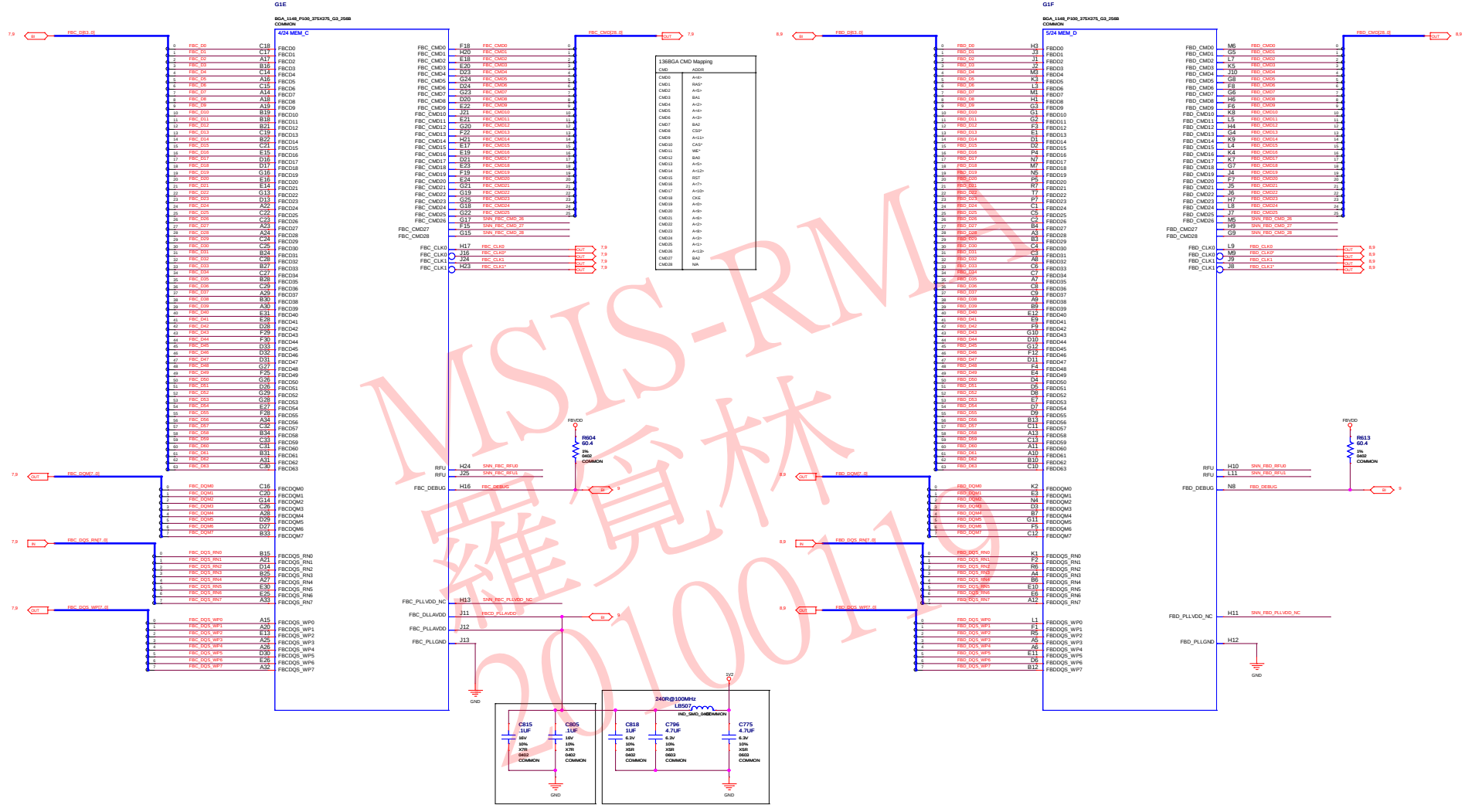
ID		PAGE	
NAME		DATE	05-MAR-2009

Page4: MEMORY: GPU Partition C/D



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PAGE DETAIL	MEMORY: GPU Partition C/D

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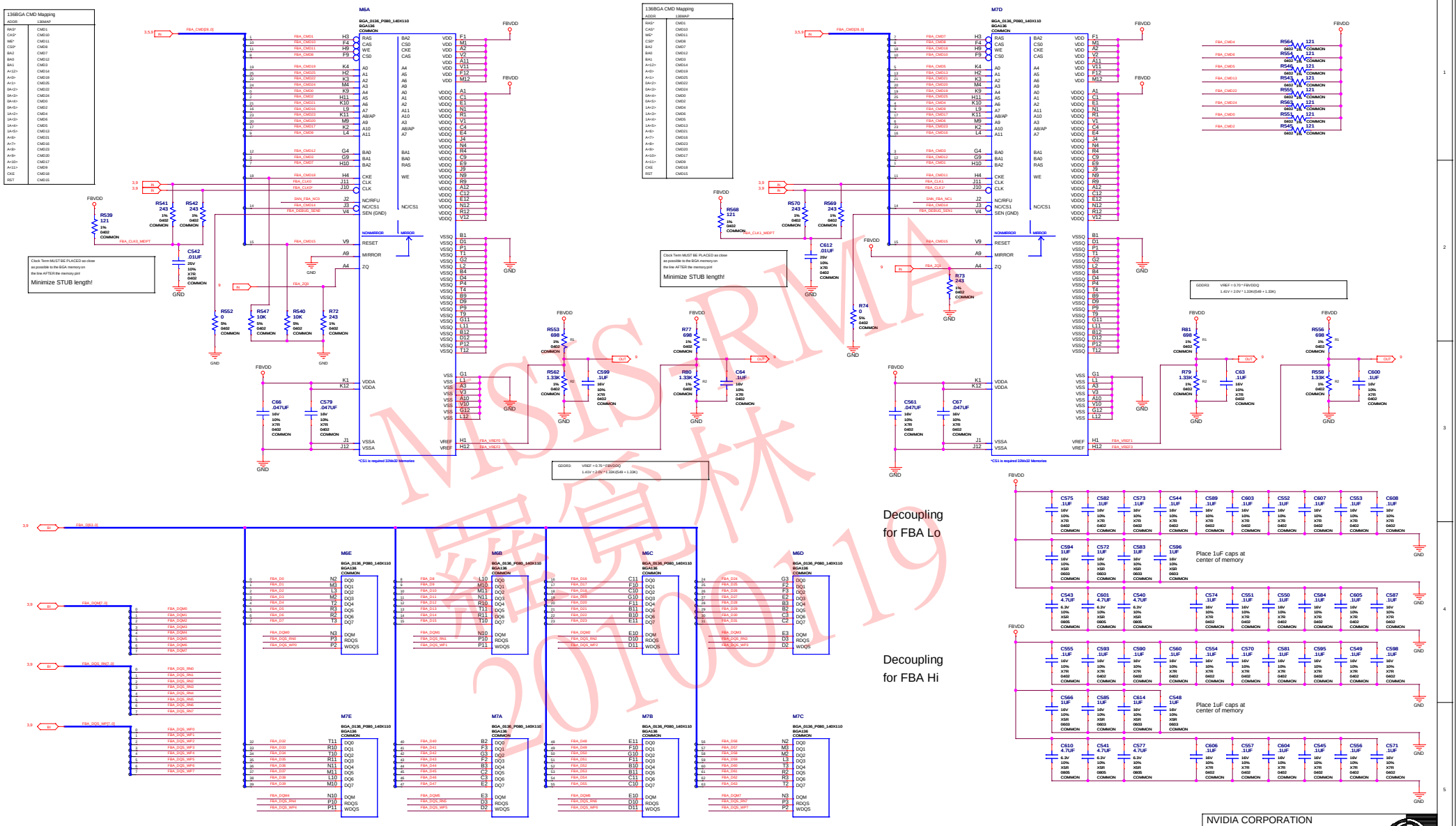
ID		PAGE	
NAME		DATE	05-MAR-2009

Page5: FBA Partition



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NAME	
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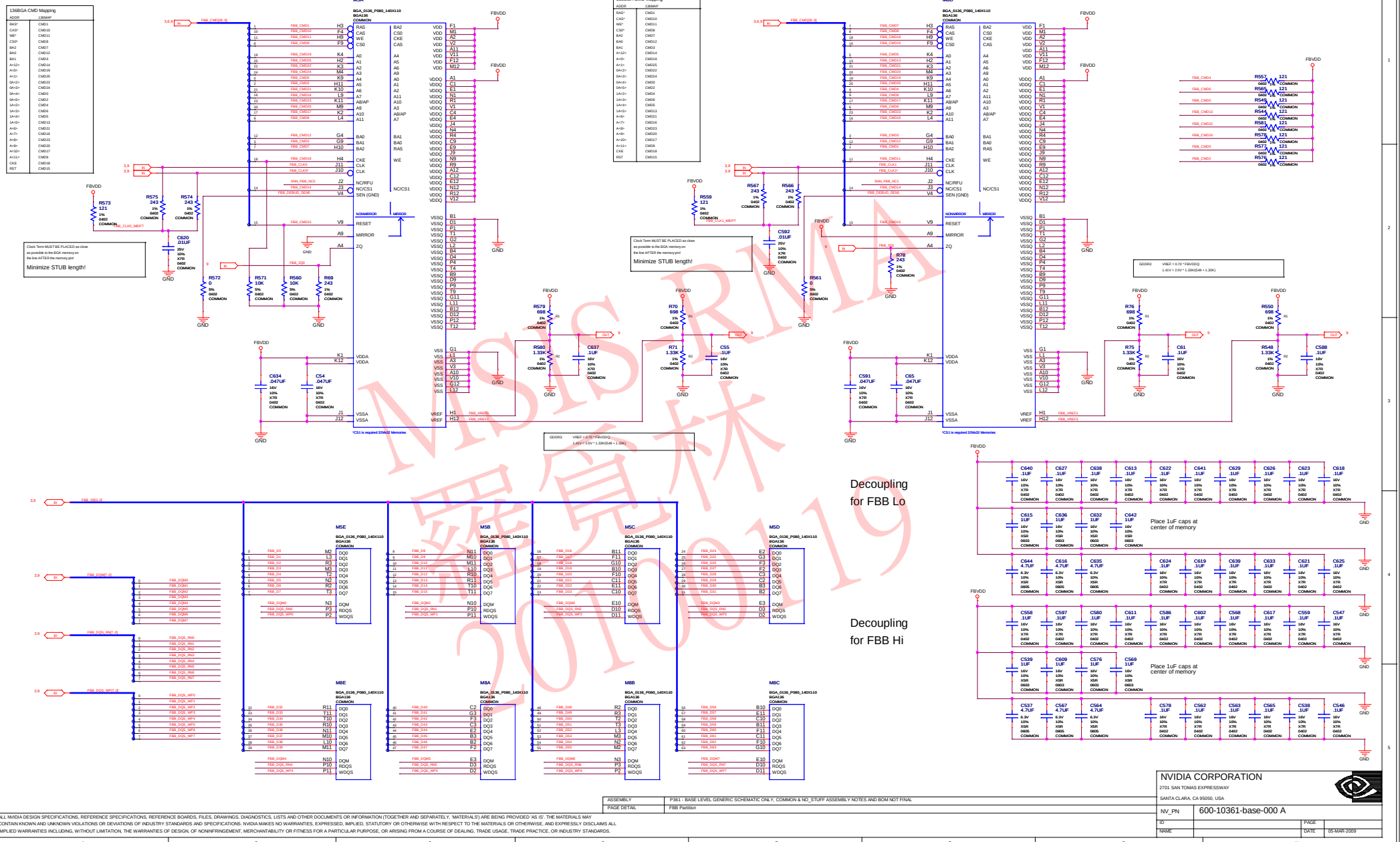
Page6: FBB Partition



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PAGE DETAIL	FBB Partition

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PAGE	
NAME	
DATE	05-MAR-2009

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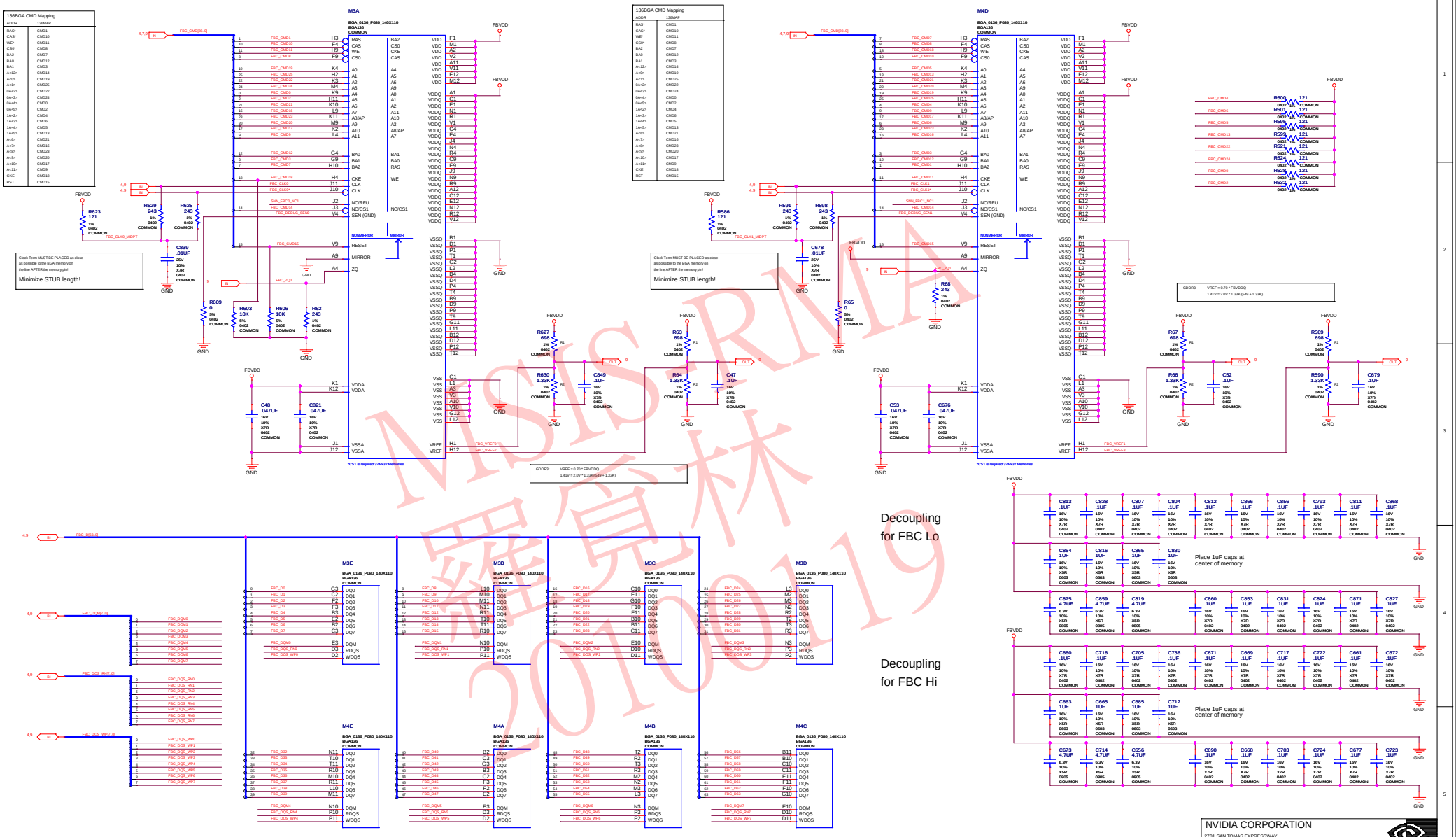
Page7: FBC Partition



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PAGE DETAIL	FBC Partition

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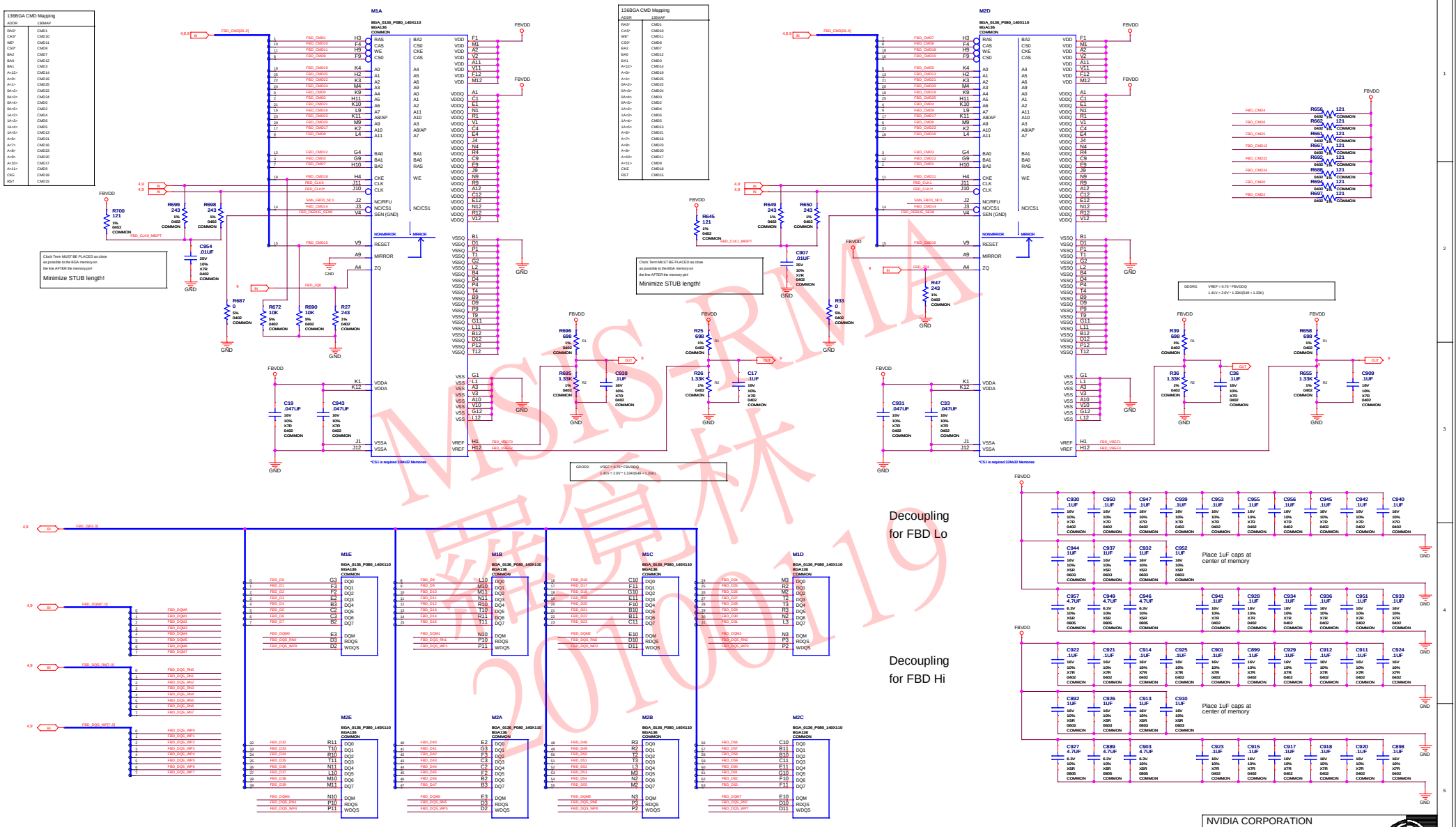
ID		PAGE	
NAME		DATE	05-MAR-2009

Page8: FBD Partition



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PAGE DETAIL	FBD Partition

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NAME		DATE	05-MAR-2009

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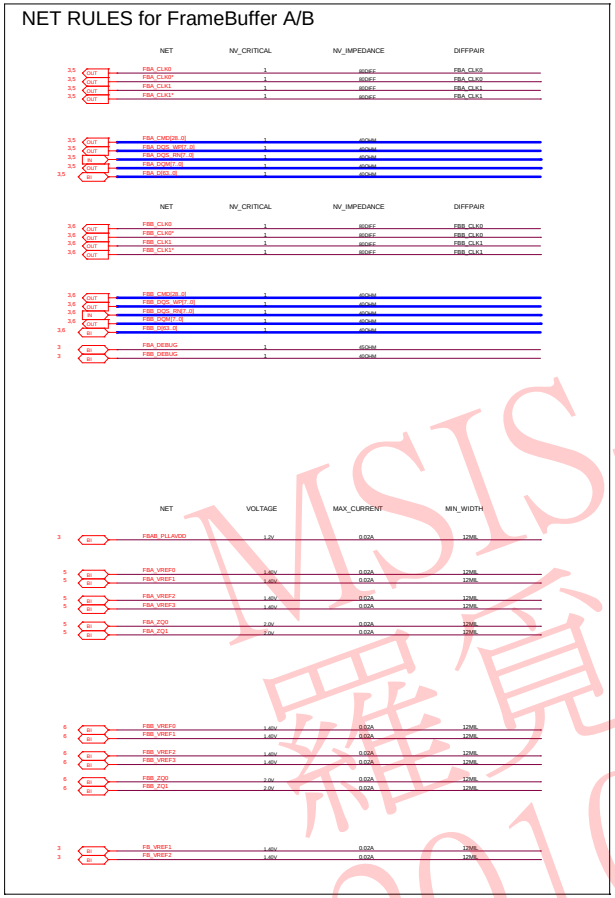
Page9: FrameBuffer Net Rules

NET RULES for FrameBuffer A/B



NET RULES for FrameBuffer C/D

Note: FB traces on top and bottom layers are routed with 45ohm impedance for increasing spacing.

Internal FB traces are routed with 40ohm impedance.

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PAGE DETAIL	FrameBuffer Net Rules

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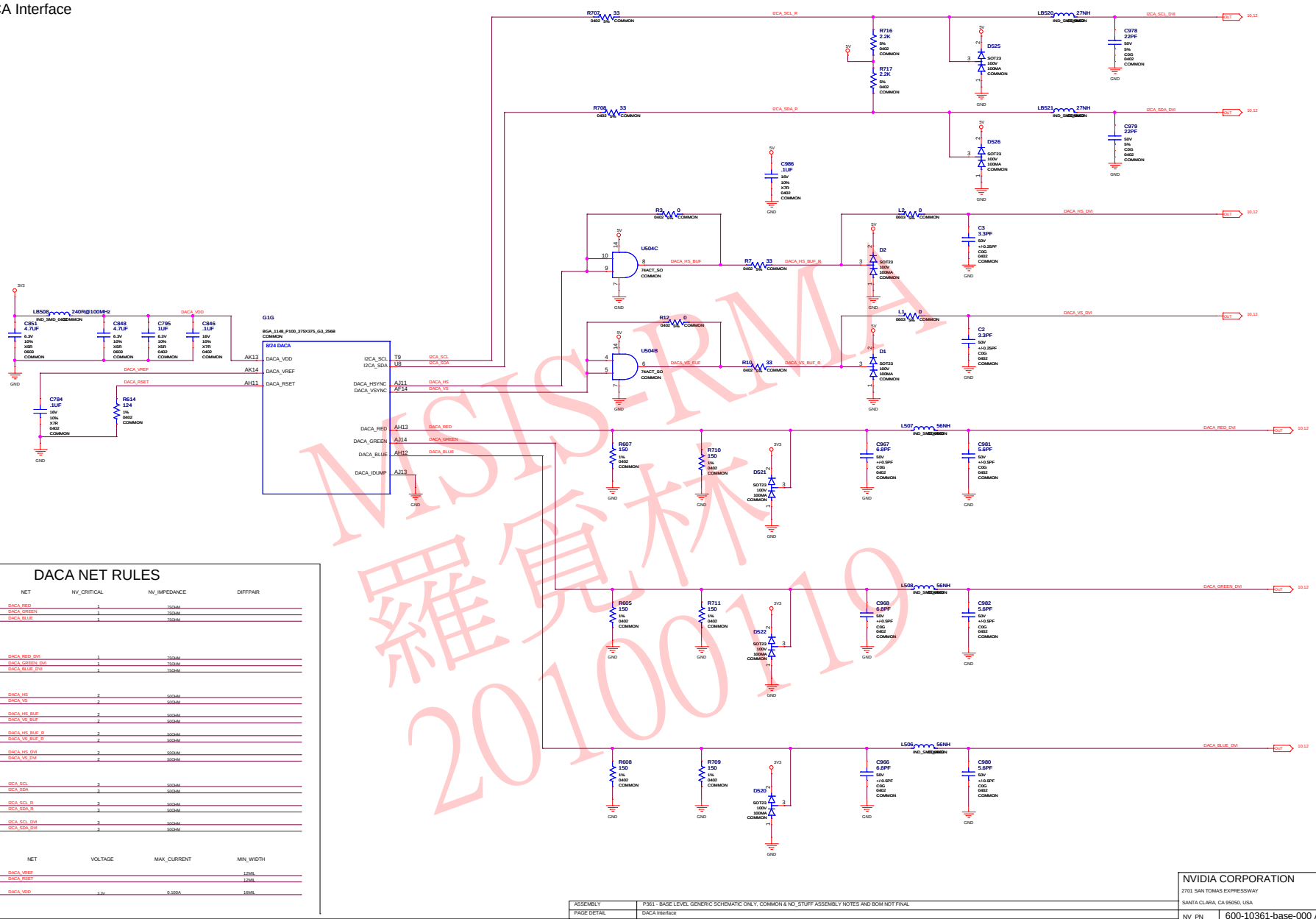
ID		PAGE	
NAME		DATE	05-MAR-2009

Page10: DACA Interface



DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACA_RED	1	75OHM	
DACA_GREEN	1	75OHM	
DACA_BLUE	1	75OHM	
DACA_RED_DVI	1	75OHM	
DACA_GREEN_DVI	1	75OHM	
DACA_BLUE_DVI	1	75OHM	
DACA_HS	2	50OHM	
DACA_VS	2	50OHM	
DACA_HS_BUF	2	50OHM	
DACA_VS_BUF	2	50OHM	
DACA_HS_BUF_R	2	50OHM	
DACA_VS_BUF_R	2	50OHM	
DACA_HS_DVI	2	50OHM	
DACA_VS_DVI	2	50OHM	
I2CA_SCL	3	50OHM	
I2CA_SDA	3	50OHM	
I2CA_SCL_R	3	50OHM	
I2CA_SDA_R	3	50OHM	
I2CA_SCL_DVI	3	50OHM	
I2CA_SDA_DVI	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACA_VREF			12MIL
DACA_RSET			12MIL
DACA_VDD	3.3V	0.100A	16MIL

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PAGE DETAIL	DACA Interface

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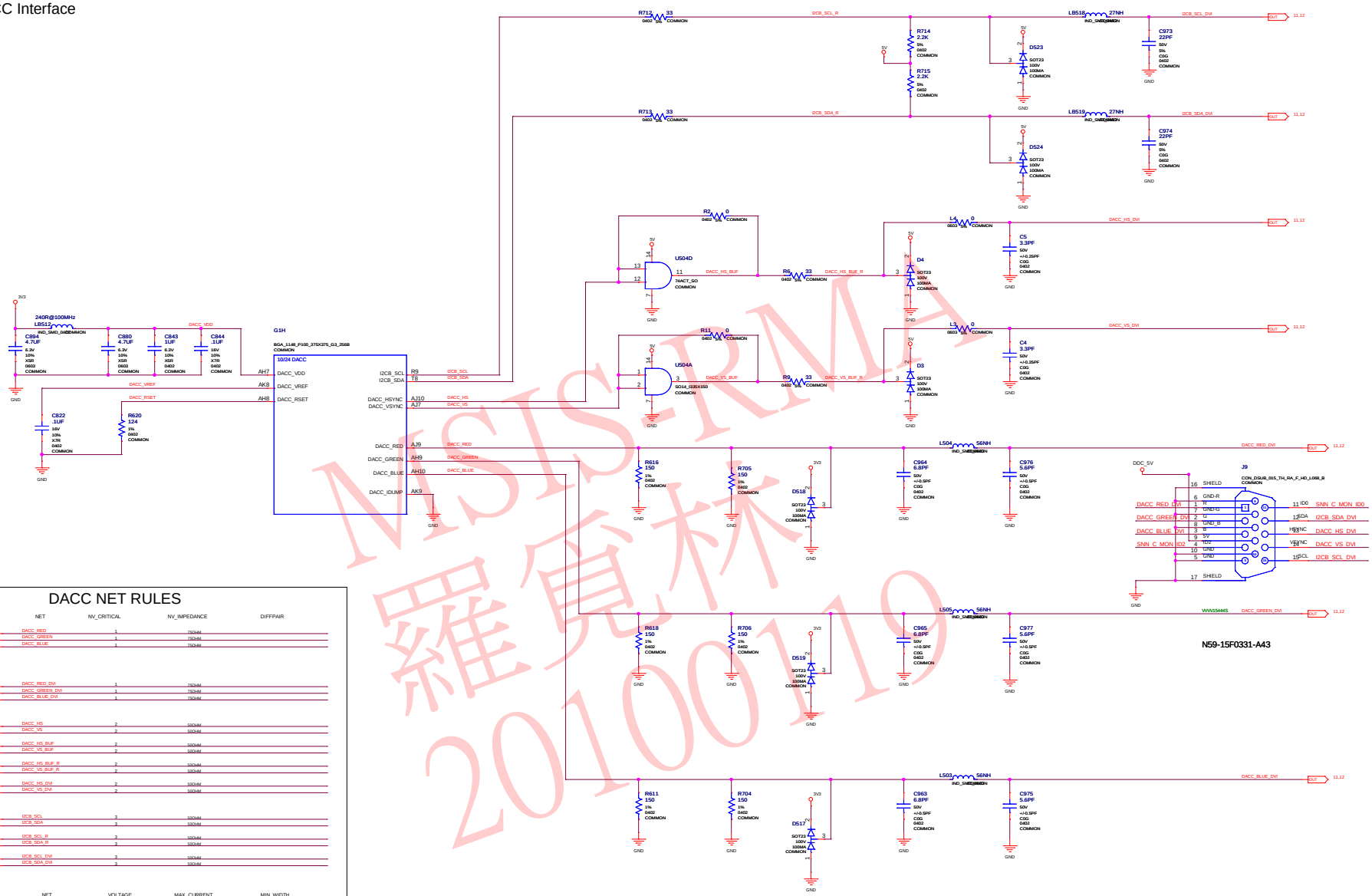
NAME	
PAGE	
DATE	05-MAR-2009

Page11: DACC Interface



DACC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACC_RED	1	75OHM	
DACC_GREEN	1	75OHM	
DACC_BLUE	1	75OHM	
DACC_RED_DVI	1	75OHM	
DACC_GREEN_DVI	1	75OHM	
DACC_BLUE_DVI	1	75OHM	
DACC_HS	2	50OHM	
DACC_VS	2	50OHM	
DACC_HS_BUF	2	50OHM	
DACC_VS_BUF	2	50OHM	
DACC_HS_BUF_R	2	50OHM	
DACC_VS_BUF_R	2	50OHM	
DACC_HS_DVI	2	50OHM	
DACC_VS_DVI	2	50OHM	
I2CB_SCL	3	50OHM	
I2CB_SDA	3	50OHM	
I2CB_SCL_R	3	50OHM	
I2CB_SDA_R	3	50OHM	
I2CB_SCL_DVI	3	50OHM	
I2CB_SDA_DVI	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACC_VREF			12MIL
DACC_RSET			12MIL
DACC_VDD	3.3V	0.300A	16MIL

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PAGE DETAIL	DACC Interface

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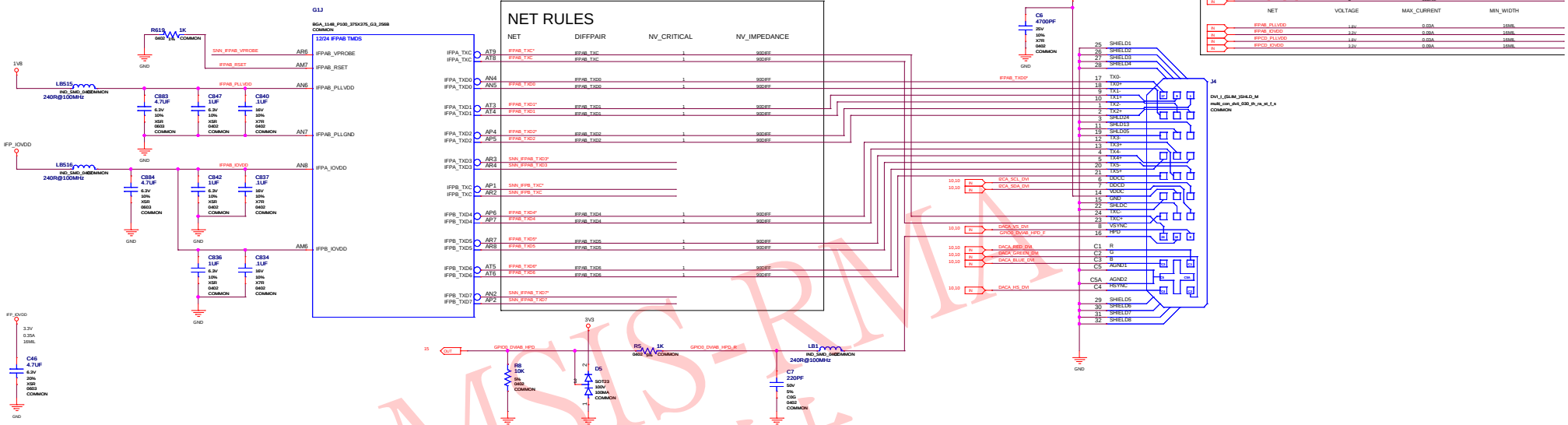
PAGE	
DATE	05-MAR-2009

Page12: IFP A/B and C/D Interface



IFPABCD NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RSET			12MIL
IFPCD_RSET			12MIL
GPIO0_DVAB_HPD_F	3	90OHM	
GPIO0_DVAB_HPD_R	3	90OHM	
GPIO1_DVCD_HPD_F	3	90OHM	
GPIO1_DVCD_HPD_R	3	90OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLLVDD	1.8V	0.03A	16MIL
IFPAB_IOVDD	3.3V	0.09A	16MIL
IFPCD_PLLVDD	1.8V	0.03A	16MIL
IFPCD_IOVDD	3.3V	0.09A	16MIL

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PAGE DETAIL	IFP A/B and C/D Interface

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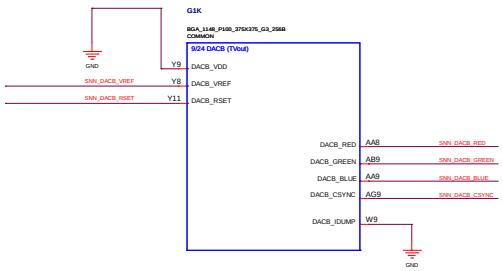
ID		PAGE	
NAME		DATE	05-MAR-2009

Page13: DACB Interface



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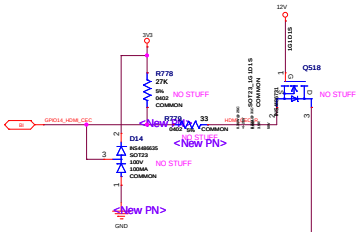
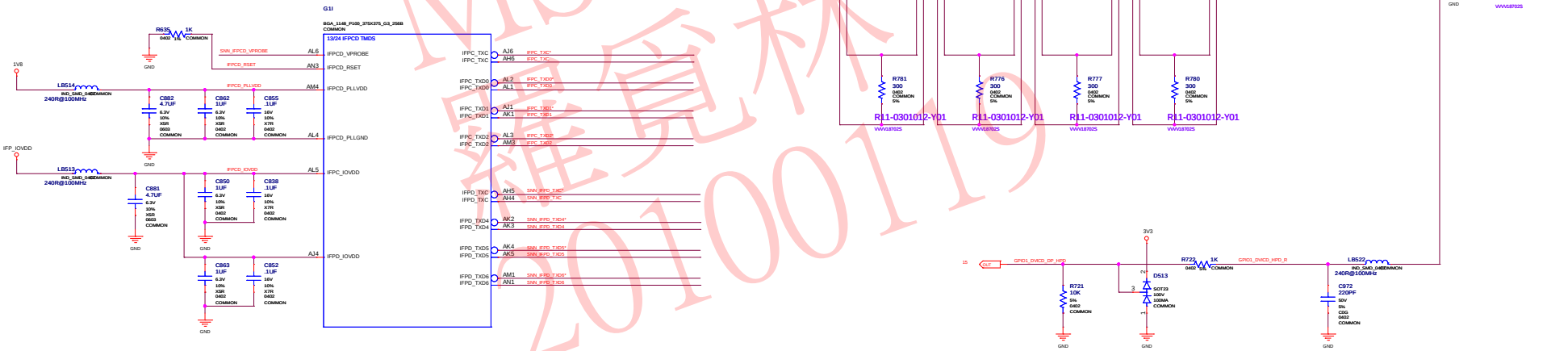


LINK C:
HDMI CEC USE GPIO 14
HPD GPIO 1



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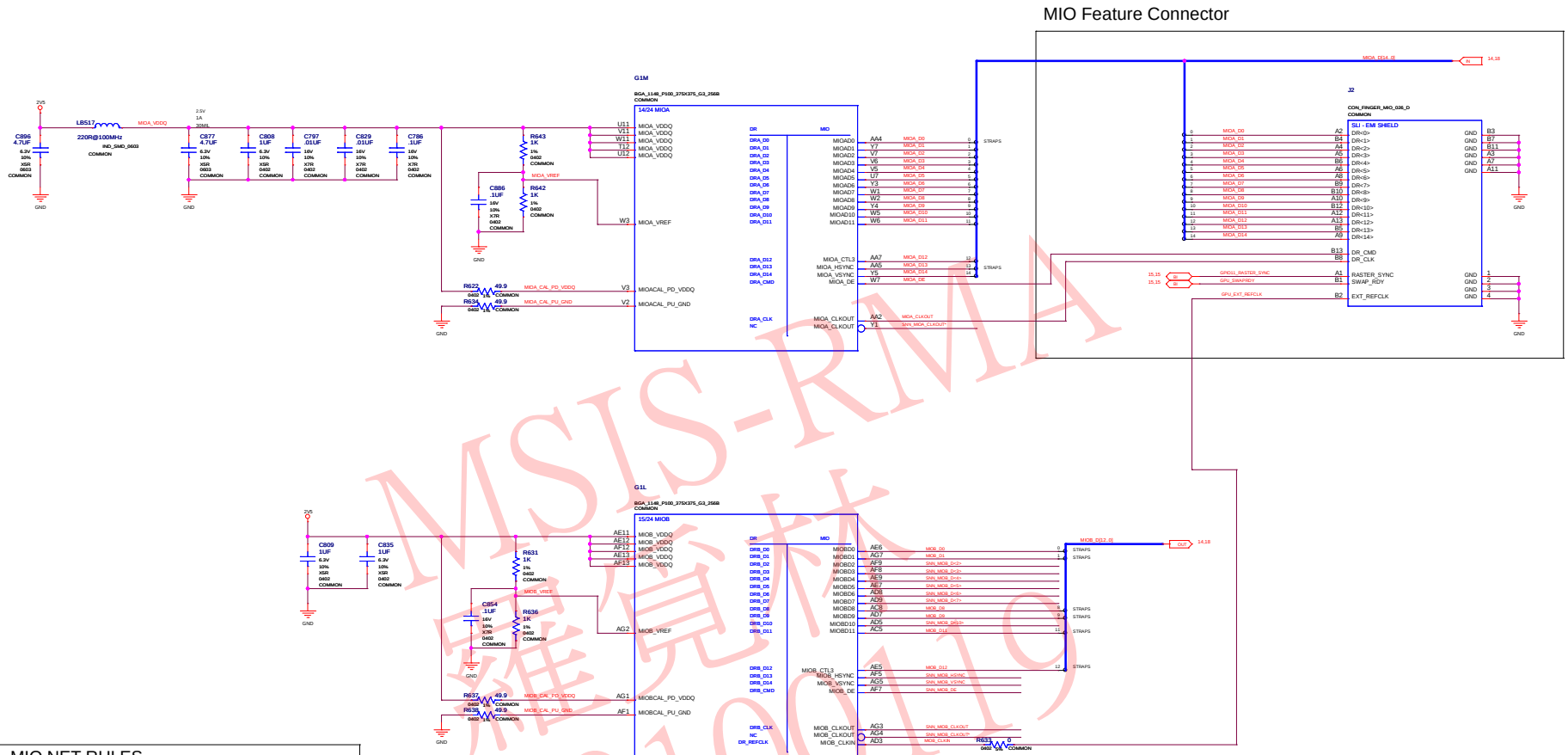
NV_PN	600-10361-base-000 A
ID	
NAME	
PAGE	
DATE	05-MAR-2009

Page14: Multi-use IO(MIO) Interface



MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
MIOA_DI14..0]	1	60OHM	
MIOA_CLKOUT	1	60OHM	
MIOA_DE	1	60OHM	
MIOB_DI12..0]	1	60OHM	
MIOB_CLKIN	1	60OHM	
GPU_EXT_REFCLK	1	60OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	1.35V		12MIL
MIOACAL_PD_VDDQ			12MIL
MIOACAL_PU_GND			12MIL
MIOB_VREF	1.35V		12MIL
MIOBCAL_PD_VDDQ			12MIL
MIOBCAL_PU_GND			12MIL

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ASSEMBLY	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Multi-use IO(MIO) Interface

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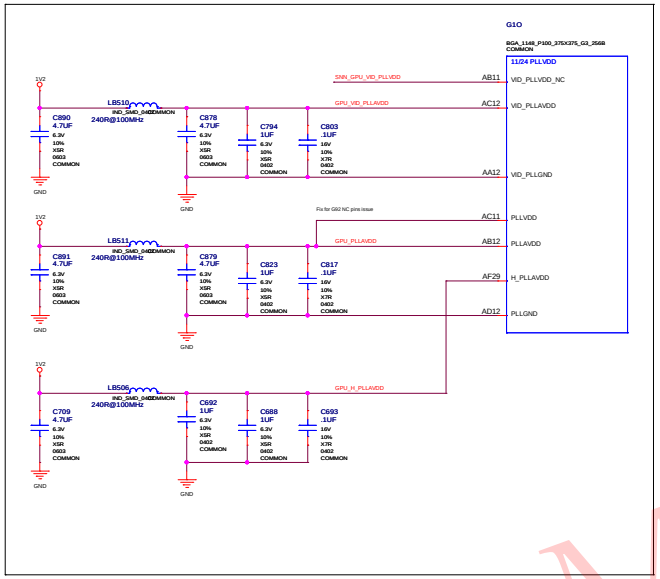
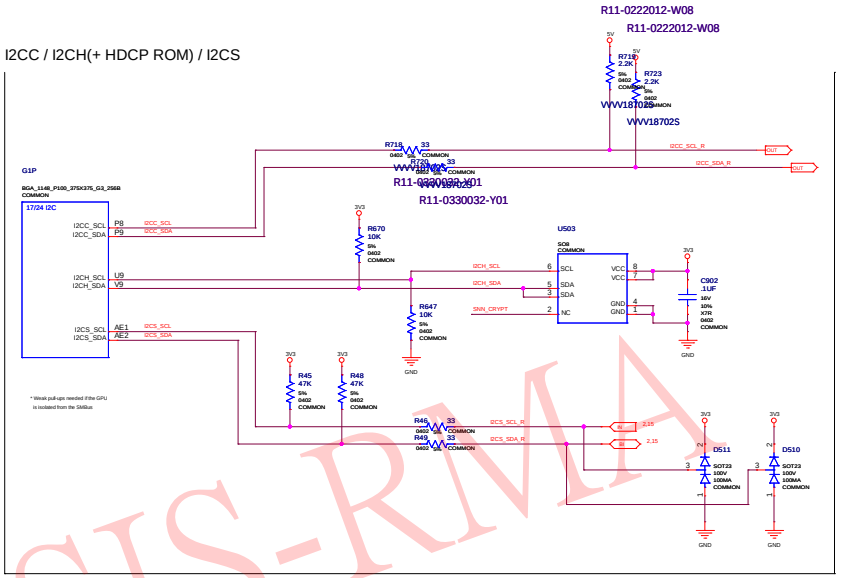
ID		PAGE	
NAME		DATE	05-MAR-2009

Page15: MISC: GPIO, I2C, BIOS, PLL, and XTAL

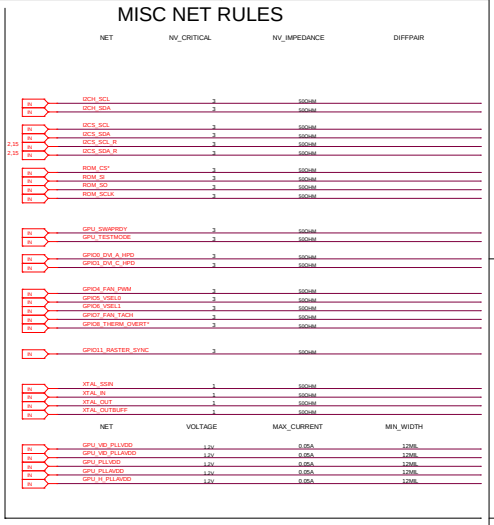
PLLVDD/VID_PLLVDD



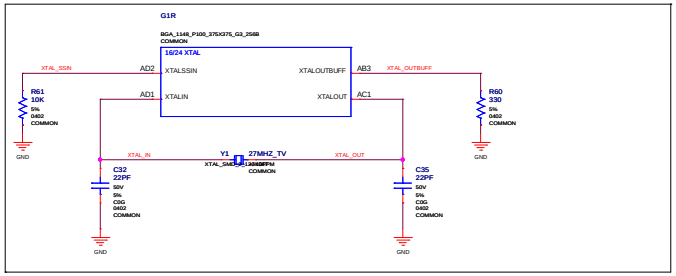
I2CC / I2CH(+ HDCP ROM) / I2CS



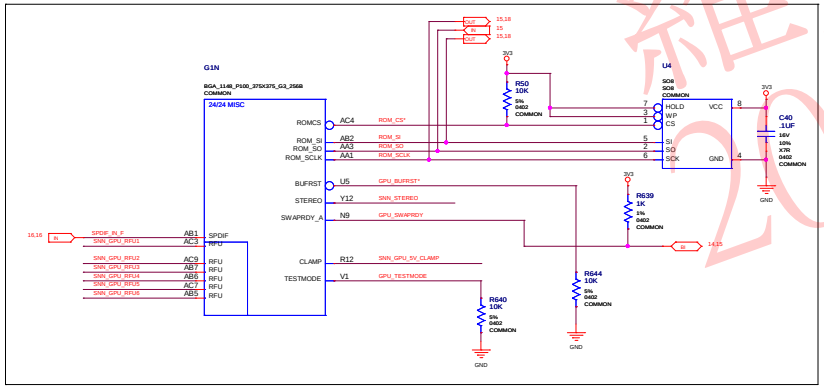
MISC NET RULES



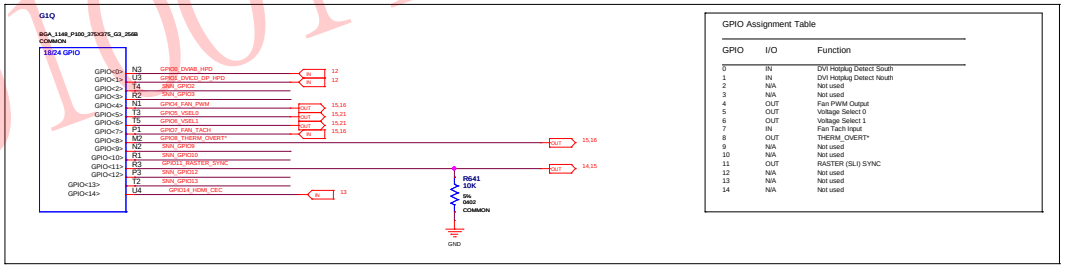
XTAL



ROM / MISC (BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)



GPIO



GPIO Assignment Table

GPIO	I/O	Function
0	IN	DVI Hotplug Detect South
1	IN	DVI Hotplug Detect Nouth
2	N/A	Not used
3	N/A	Not used
4	OUT	Fan PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fan Tach Input
8	OUT	THERM_OVERT*
9	N/A	Not used
10	N/A	Not used
11	OUT	RASTER (SLI) SYNC
12	N/A	Not used
13	N/A	Not used
14	N/A	Not used

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ASSEMBLY	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO, I2C, BIOS, PLL, and XTAL

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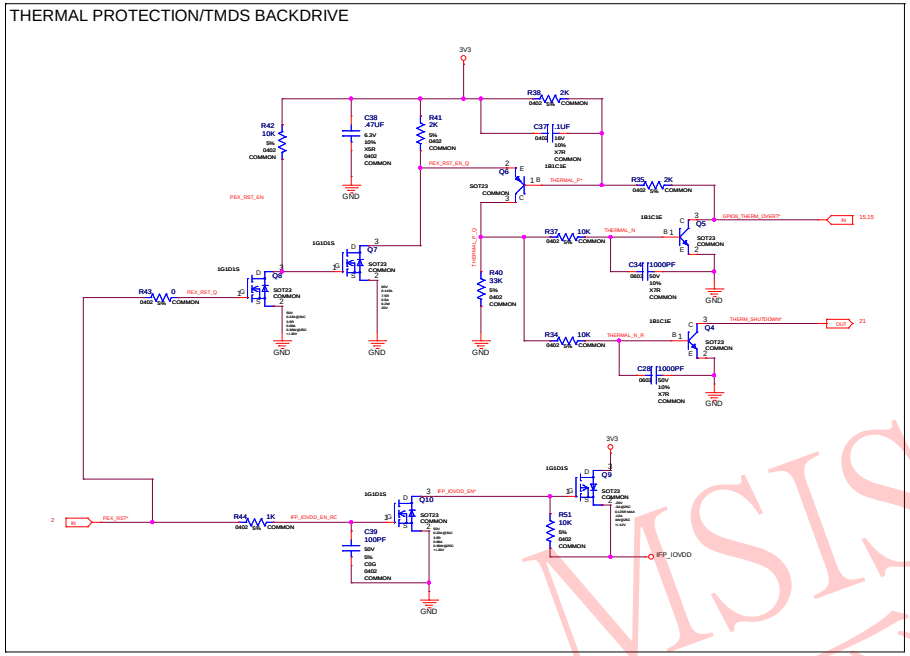
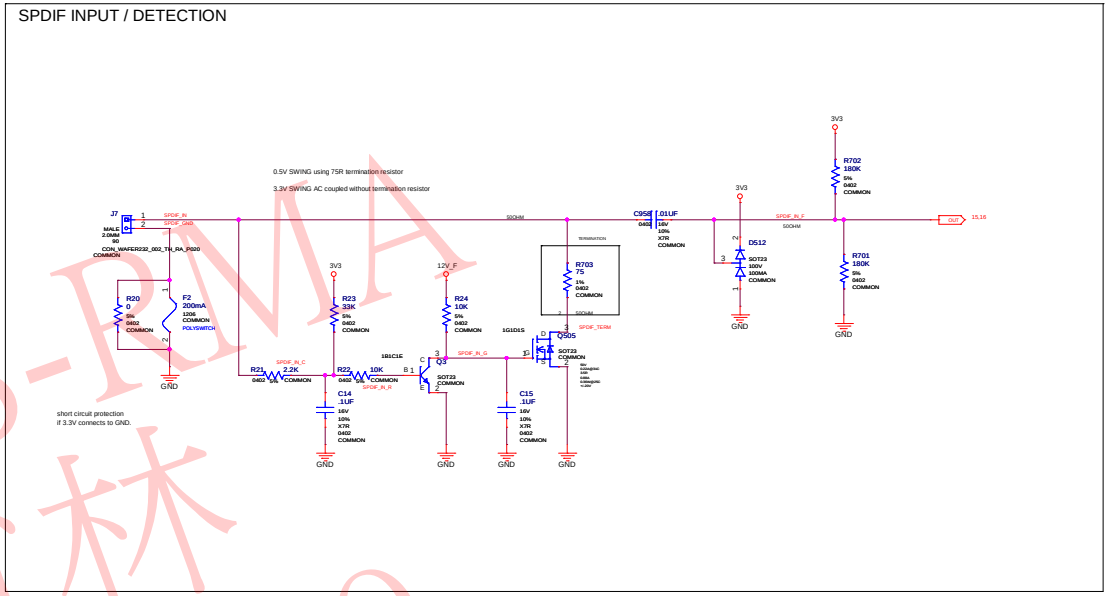
ID	
NAME	
PAGE	
DATE	05-MAR-2009

Page16: Thermal Control/Protection and SPDIF Input

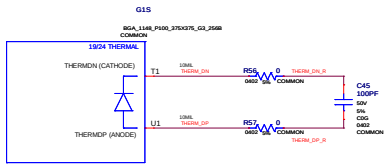
THERMAL PROTECTION/TMDS BACKDRIVE

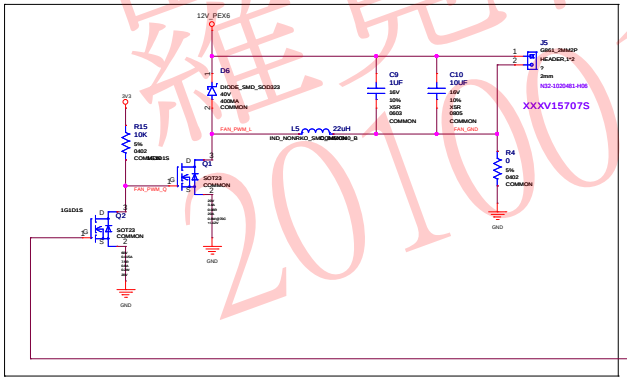


SPDIF INPUT / DETECTION

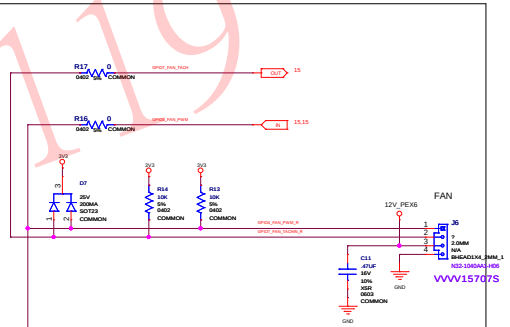


THERMAL DIODE





2-pin fan option



NET	IMPEDANCE	NV_CRITICAL_NET	MIN_LINE_WIDTH
SPDIF_IN	50OHM	1	
SPDIF_IN_C	50OHM	1	
SPDIF_IN_R	50OHM	1	
SPDIF_IN_G	50OHM	1	
SPDIFIN_TERM	50OHM	1	
SPDIF_IN_F	50OHM	1	

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PAGE DETAIL	Thermal Control/Protection and SPDIF Input

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ID		PAGE	
NAME		DATE	05-MAR-2009

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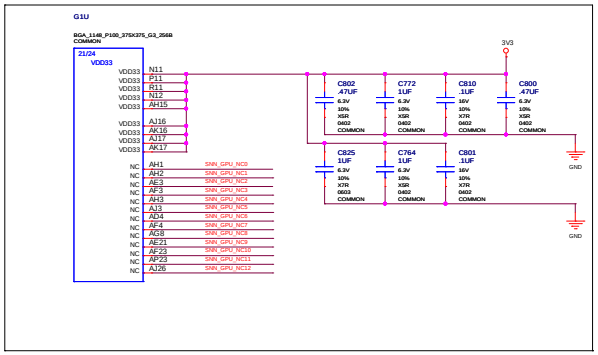
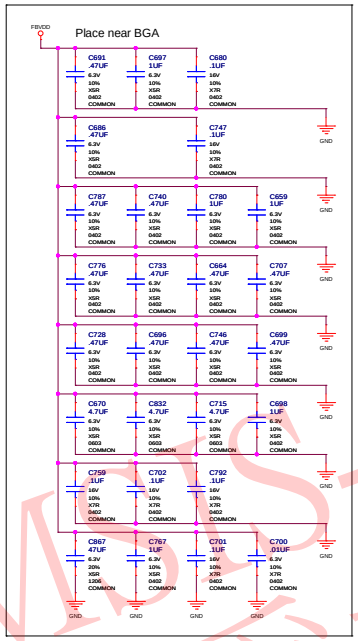
Page17: Power/GND and Decoupling

VDD33

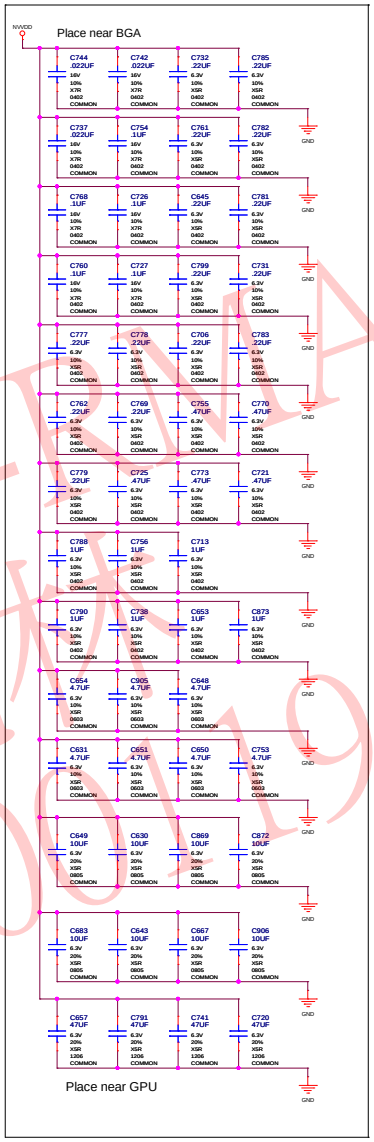


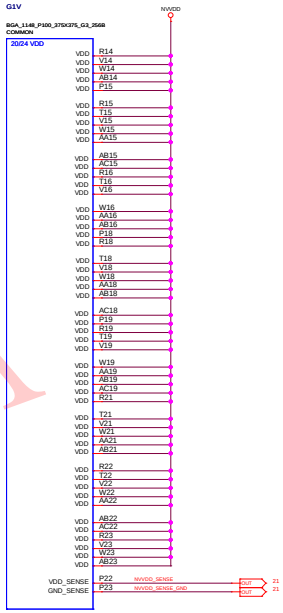
FBVTT

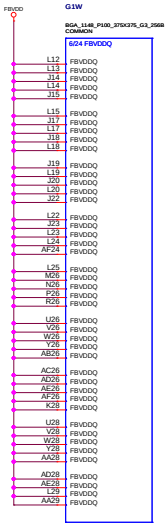
FBVDDQ

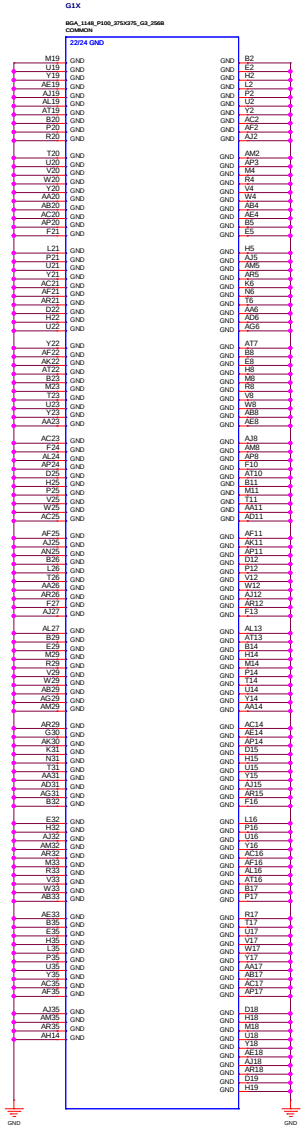


NVVDD









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ASSEMBLY	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power/GND and Decoupling

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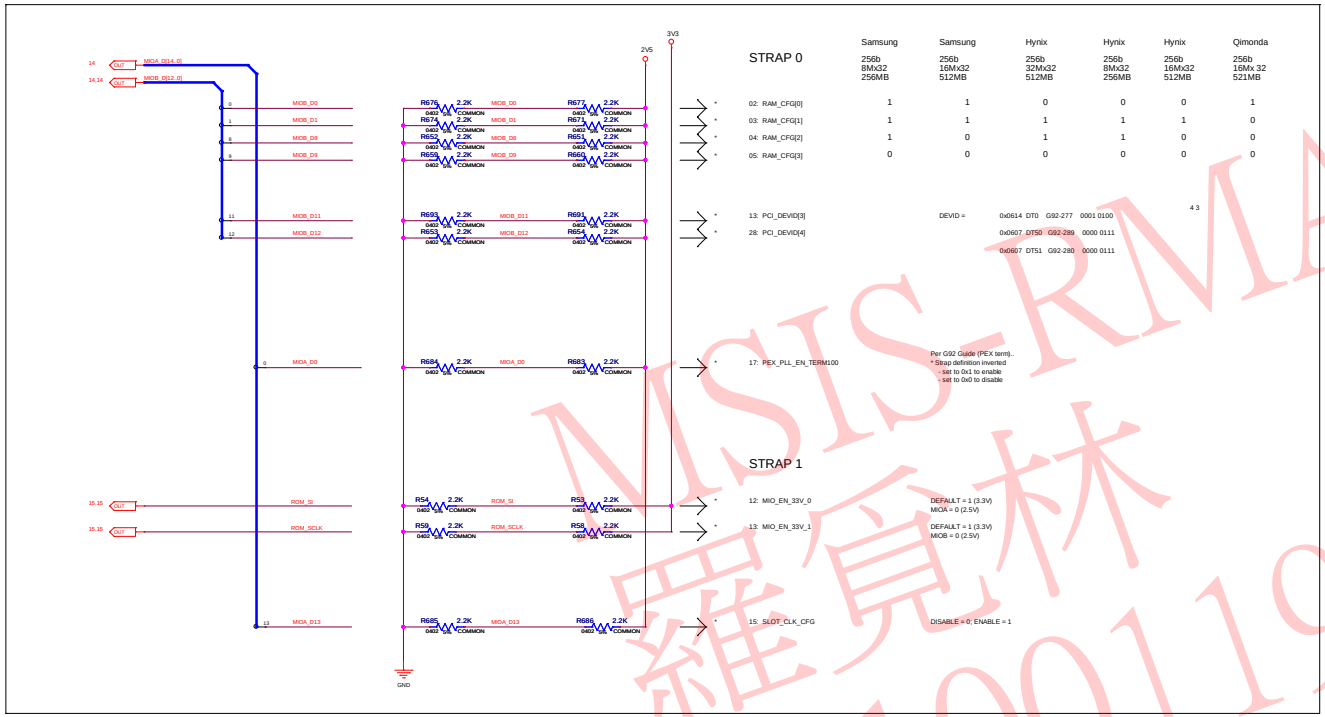
NV_PN	600-10361-base-000 A		
ID		PAGE	
NAME		DATE	05-MAR-2009

Page18: Configuration Straps and Mechanical

STRAPS



STRAP 0

	Samsung 256b 8Mx32 256MB	Samsung 256b 16Mx32 512MB	Hynix 256b 32Mx32 512MB	Hynix 256b 8Mx32 256MB	Hynix 256b 16Mx32 512MB	Qimonda 256b 16Mx 32 521MB
02: RAM_CFG[0]	1	1	0	0	0	1
03: RAM_CFG[1]	1	1	1	1	1	0
04: RAM_CFG[2]	1	0	1	1	0	0
05: RAM_CFG[3]	0	0	0	0	0	0

13: PCI_DEVID[3] — DEVID = 0x0614 DT0 G92-277 0001 0100 (4 3)
28: PCI_DEVID[4] — 0x0607 DT50 G92-289 0000 0111; 0x0607 DT51 G92-280 0000 0111

Per G92 Guide (PEX term)..
* Strap definition inverted
- set to 0x1 to enable
- set to 0x0 to disable

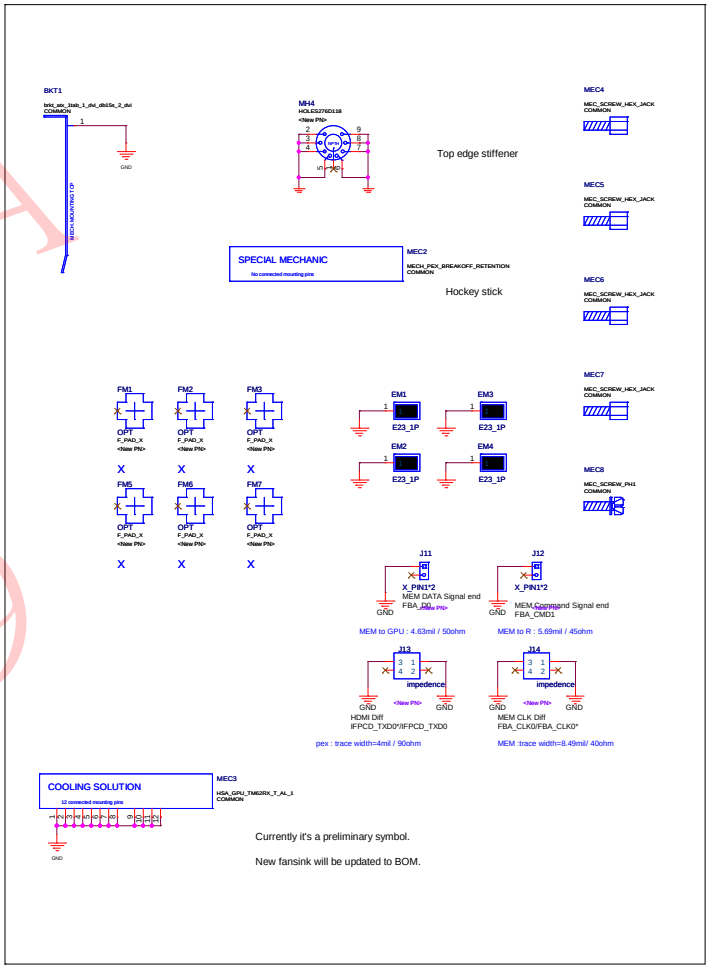
17: PEX_PLL_EN_TERM100

STRAP 1

12: MIO_EN_33V_0 — DEFAULT = 1 (3.3V) MOA = 0 (2.5V)
13: MIO_EN_33V_1 — DEFAULT = 1 (3.3V) MIOB = 0 (2.5V)

15: SLOT_CLK_CFG — DISABLE = 0; ENABLE = 1

MECHANICAL



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PAGE DETAIL	Configuration Straps and Mechanical

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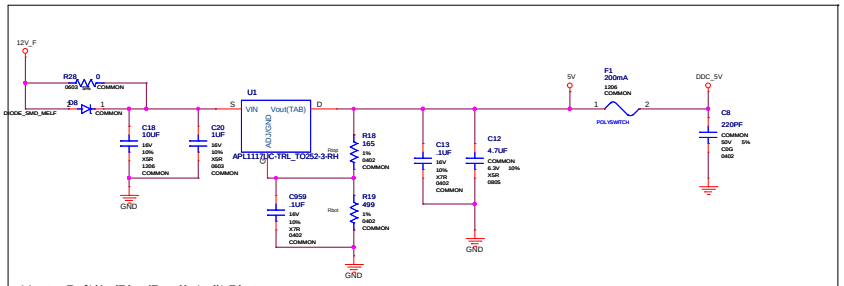
NV_PN	600-10361-base-000 A		
ID		PAGE	
NAME		DATE	05-MAR-2009

Page 19:Power Supply: 5V, 5V_DDC, 1v8, 2V5,PEX_PLLVDD Option

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	DDC_5V	0.1A	12MIL	5V
5V	5V	0.15A	12MIL	5V
PEX_PLLVDD	PEX_PLLVDD	0.12A	12MIL	1.1V
1V8	1V8	0.12A	12MIL	1.8V
2V5	2V5	0.8A	12MIL	2.5V

5V REGULATOR

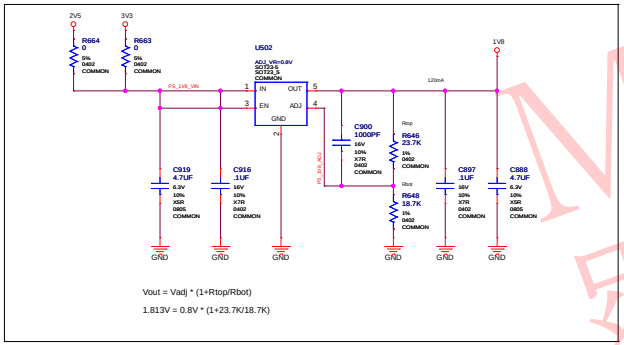
5V DDC



Vout = Ref*(1+(Rbot/Rtop))+Iadj* Rbot

5.06V = 1.25*(1+(499/165))+60uA* 499

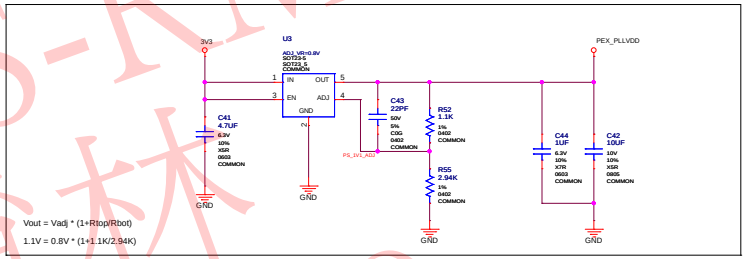
IFP PLL Supply 1.8V



Vout = Vadj * (1+Rtop/Rbot)

1.813V = 0.8V * (1+23.7K/18.7K)

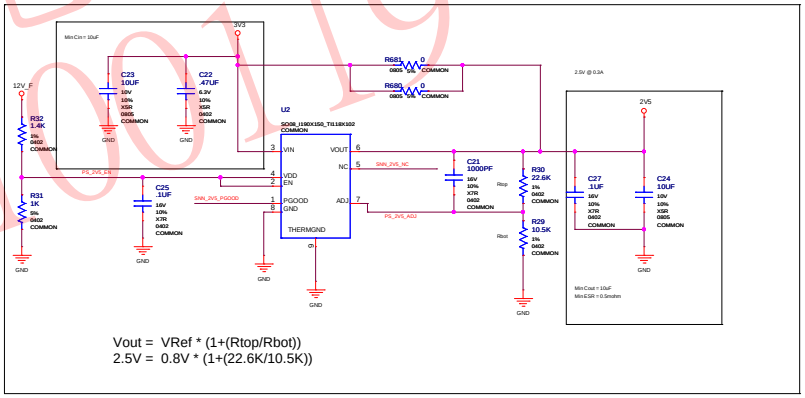
PEX_PLLVDD Optional



Vout = Vadj * (1+Rtop/Rbot)

1.1V = 0.8V * (1+1.1K/2.94K)

MIO_VDD 2.5V



Vout = VRef * (1+(Rtop/Rbot))

2.5V = 0.8V * (1+(22.6K/10.5K))

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ASSEMBLY	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 5V, STEREO_5V, 2V5, DP_PWR

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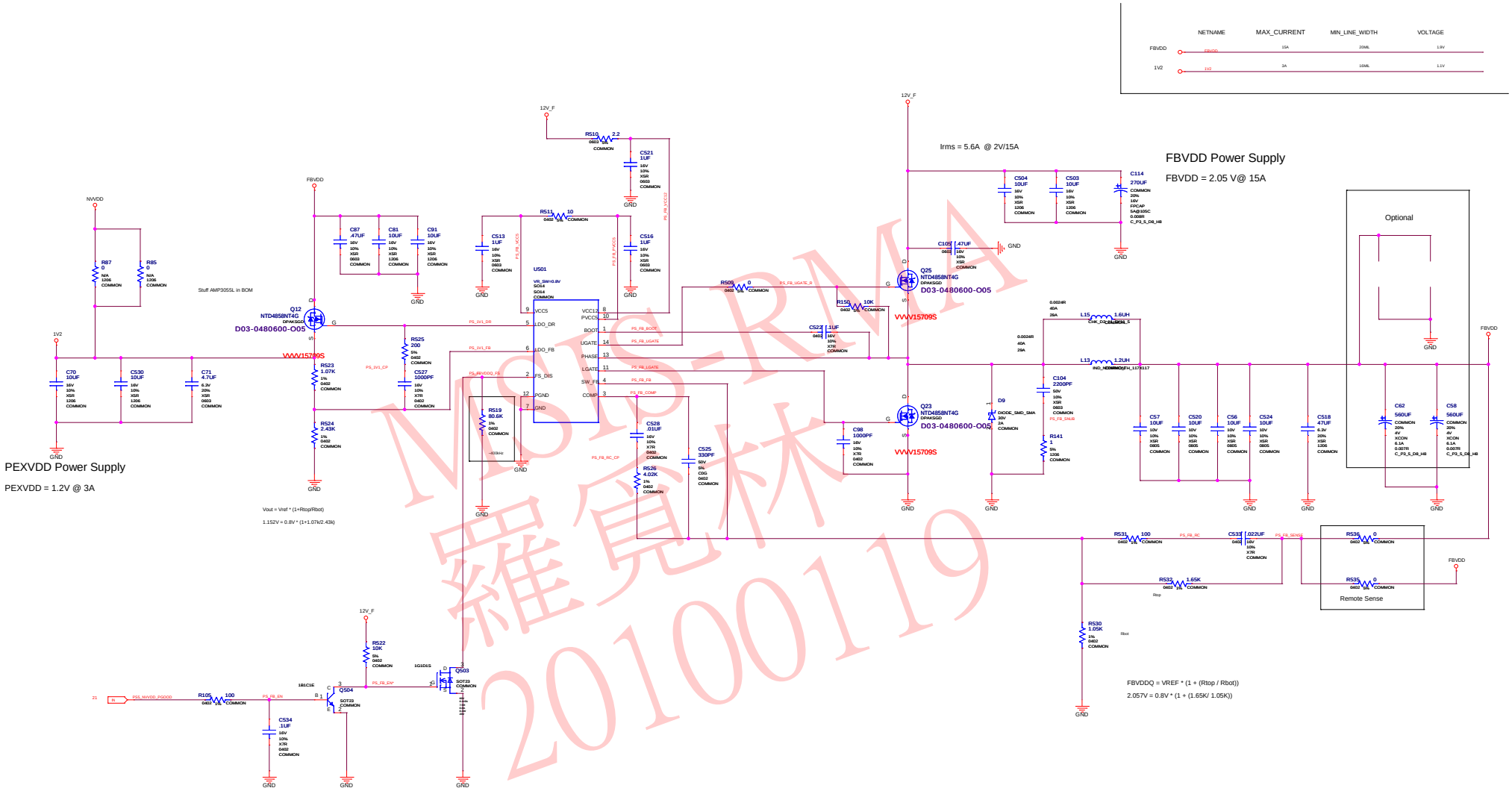
ID		PAGE	
NAME		DATE	05-MAR-2009

Page20:POWER SUPPLY: FBVDD,PEX_VDD



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PAGE DETAIL	Power Supply: FBVDD, PEXVDD

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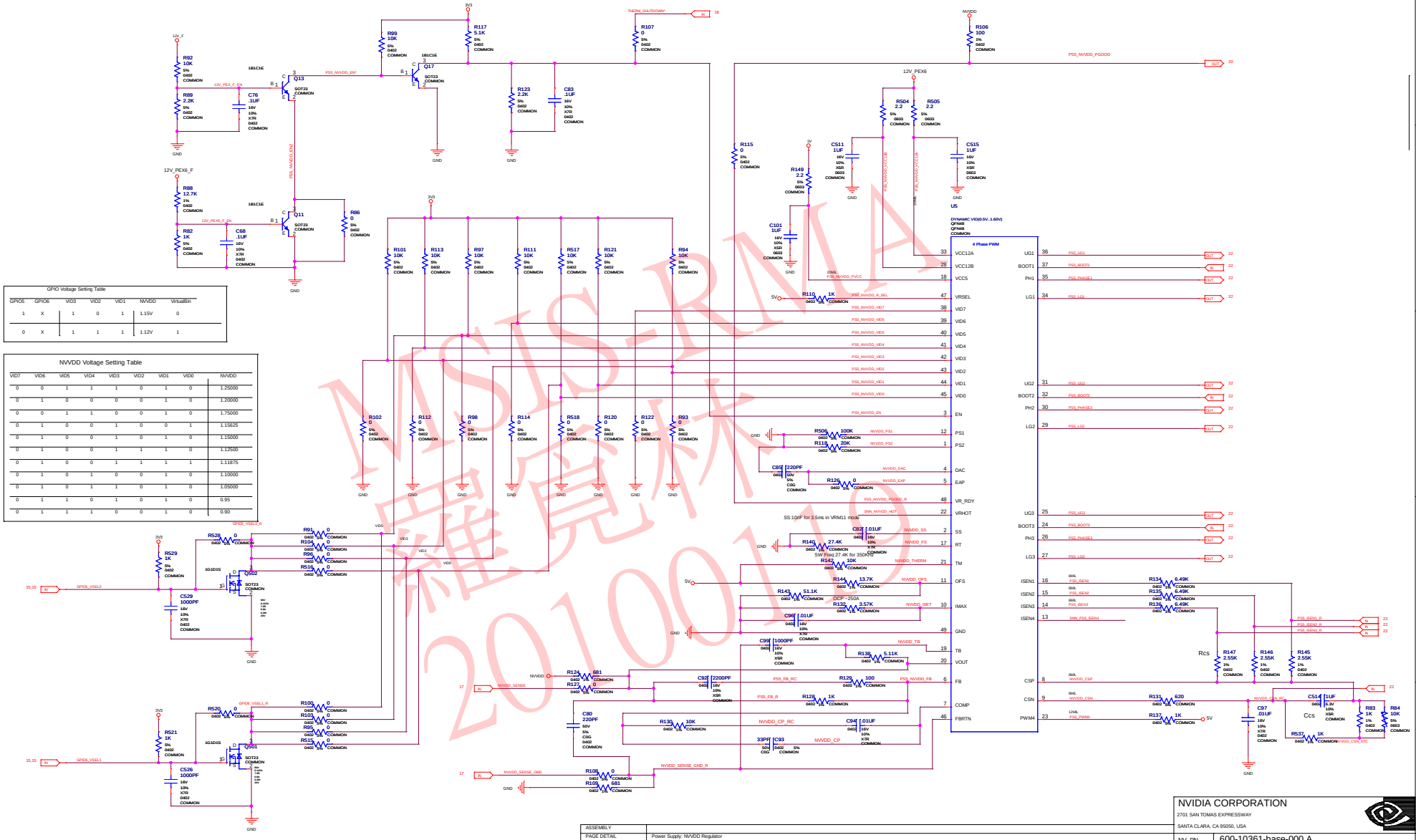
ID	
PAGE	
NAME	
DATE	05-MAR-2009

Page21: Power Supply: NVVDD Regulator



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ASSEMBLY	
PAGE DETAIL	Power Supply: NVVDD Regulator

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Page22: Power Supply: NVVDD Mosfet

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ASSEMBLY	
PAGE DETAIL	Power Supply: NVVDD Mosfet

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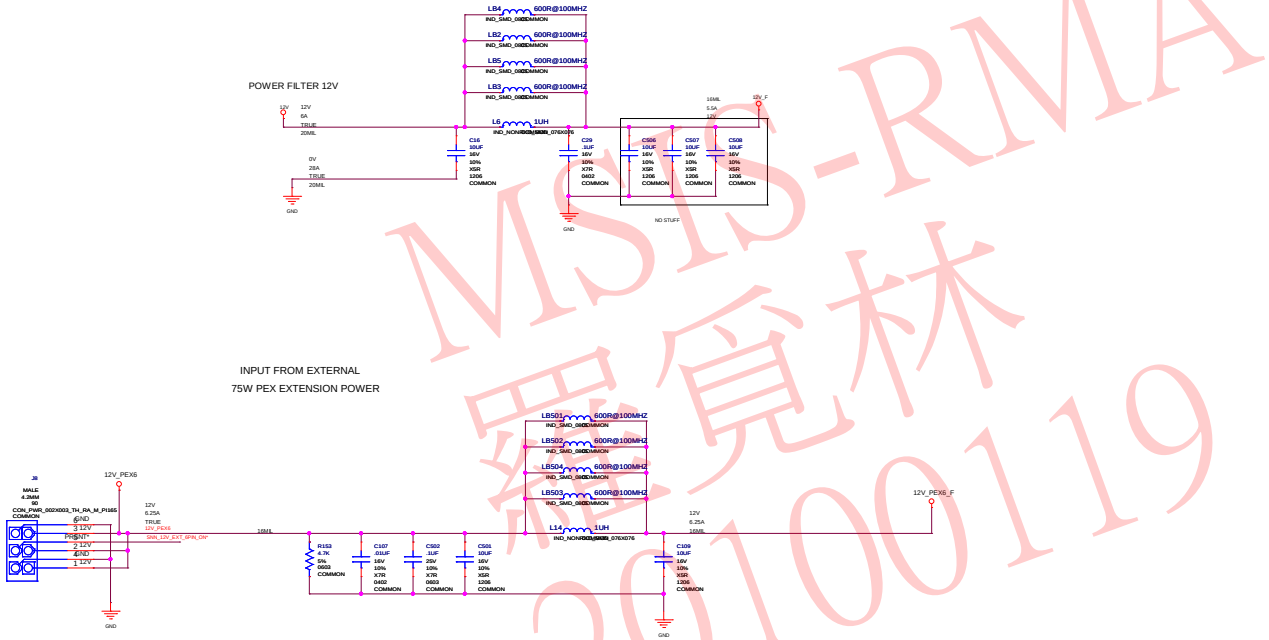
Page23: Power Supply: Filter of 12V,12V_PEX6,3V3



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ASSEMBLY	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: Filter of 3V3, 12V, 12V_PEX6

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