

PG180-A03

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

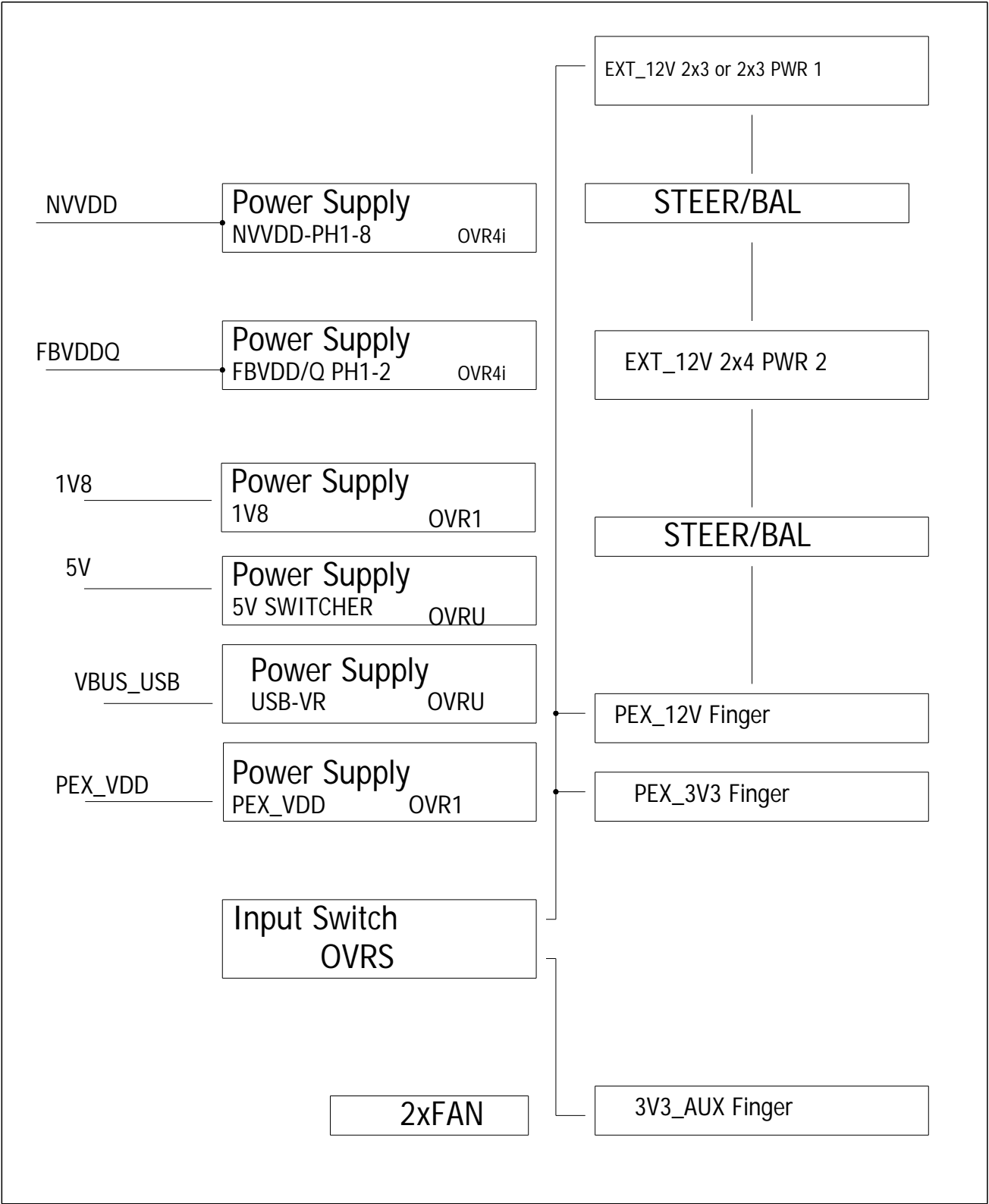
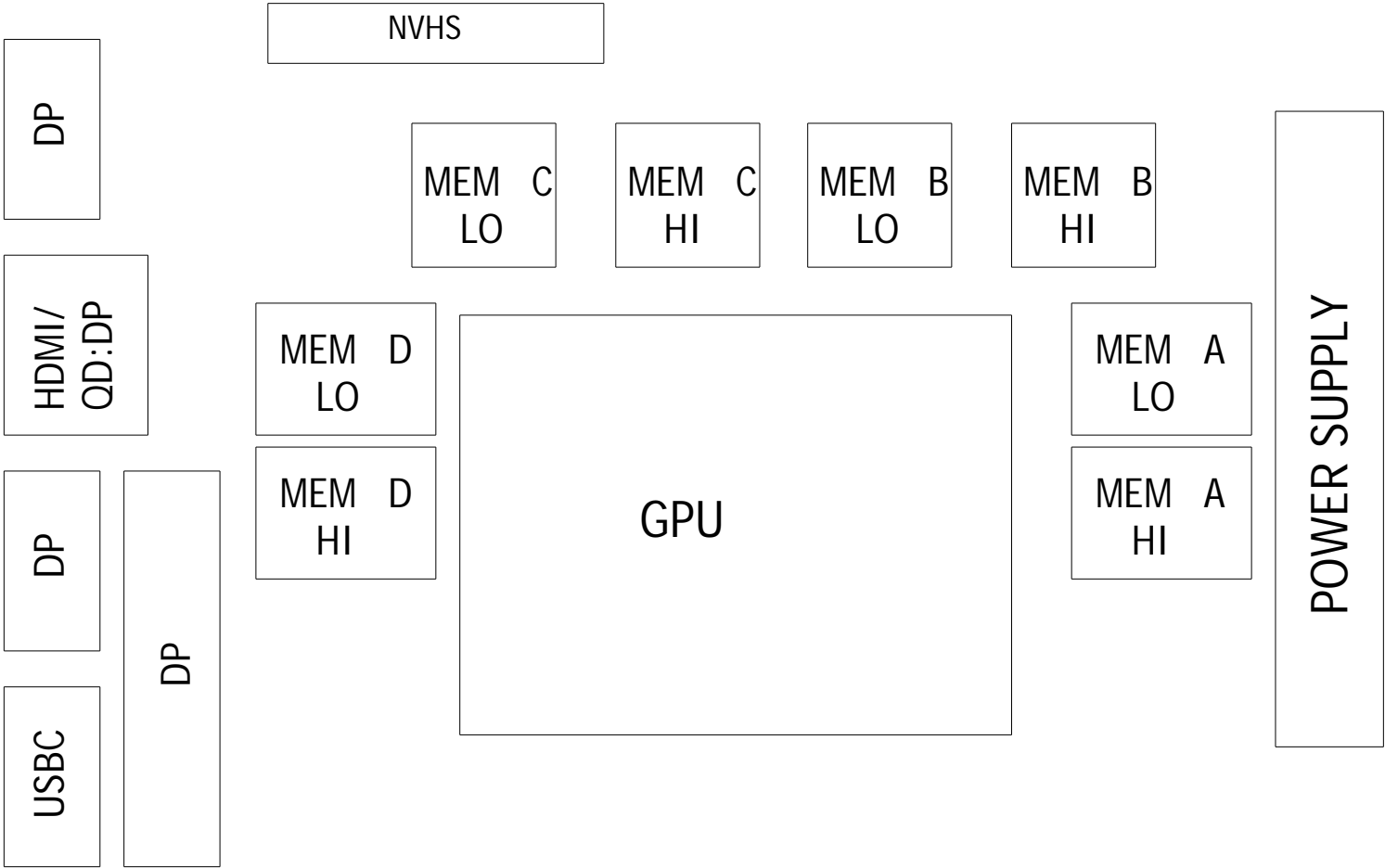
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Page2: Block Diagram

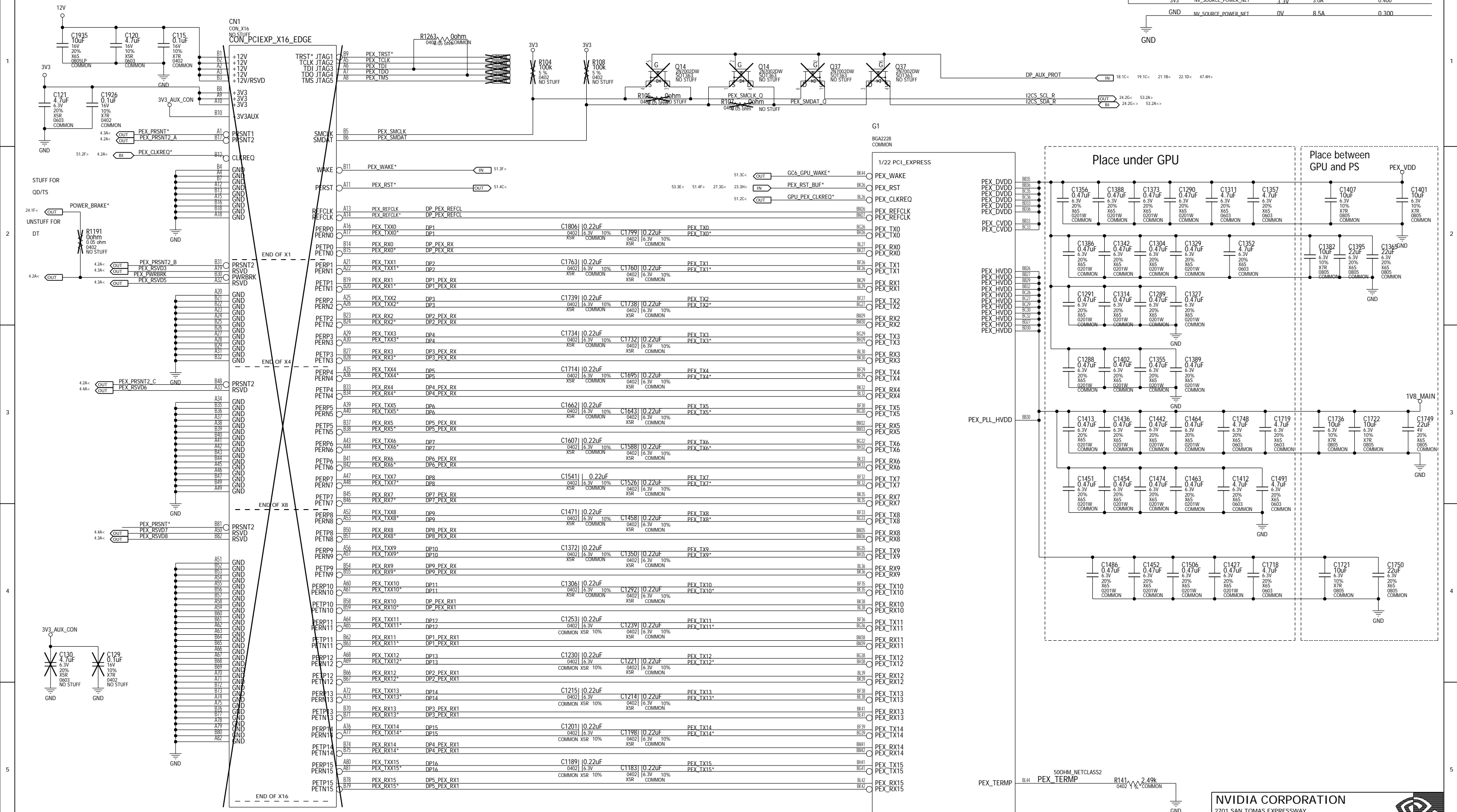


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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	Block Diagram


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Page3: PCI Express

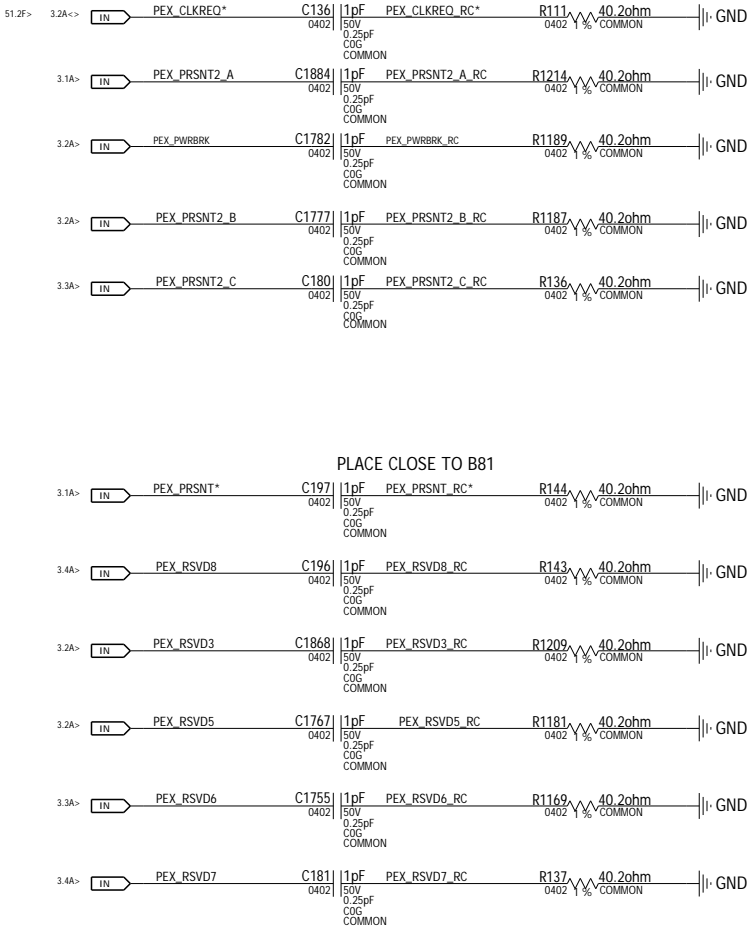


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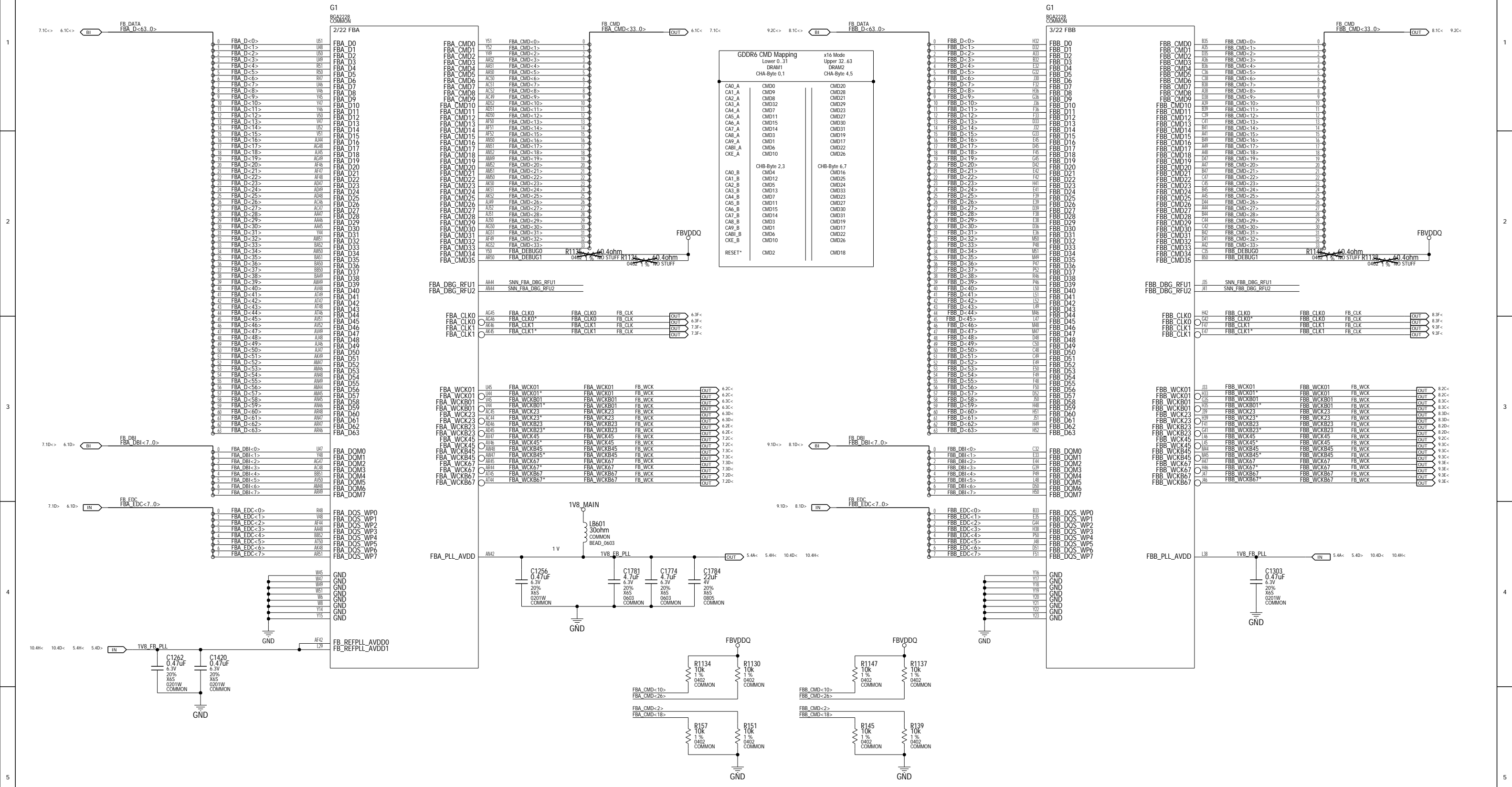
ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PCI Express

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Page4: PCI Termination

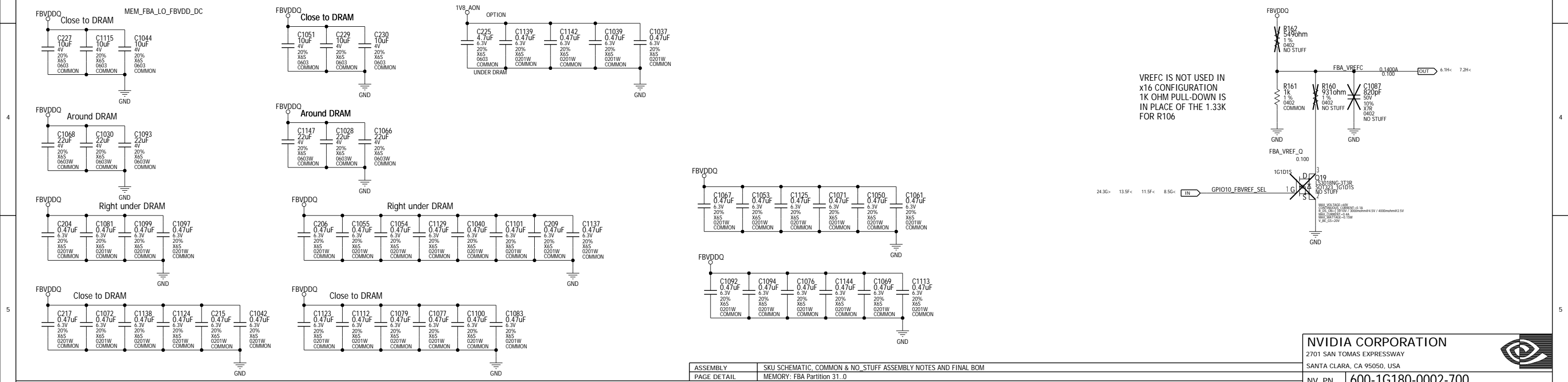
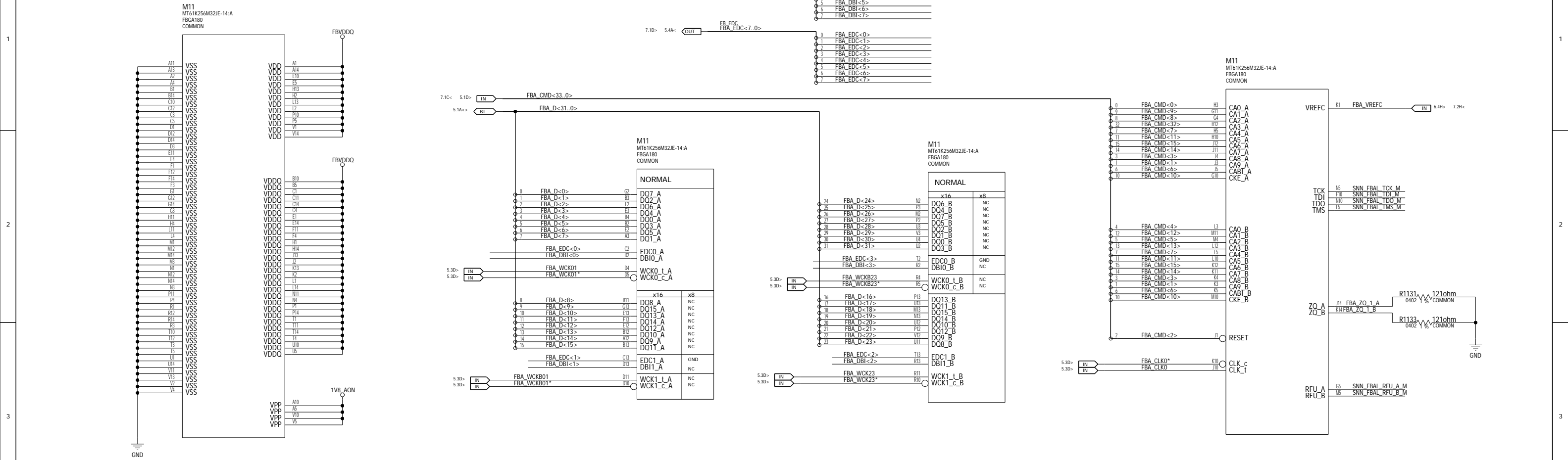


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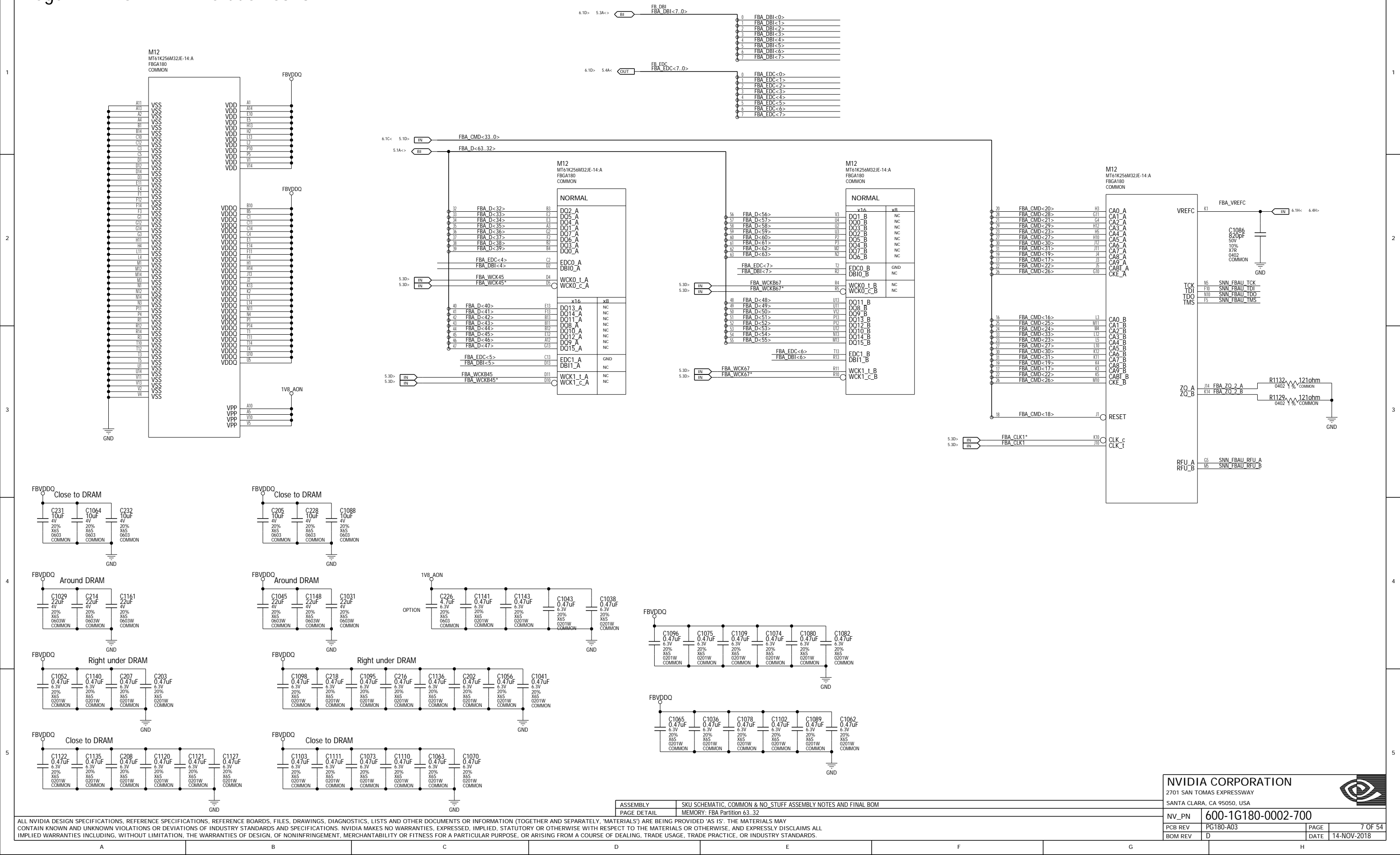


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Page6: MEMORY: FBA Partition 31..0



Page7: MEMORY: FBA Partition 63..32



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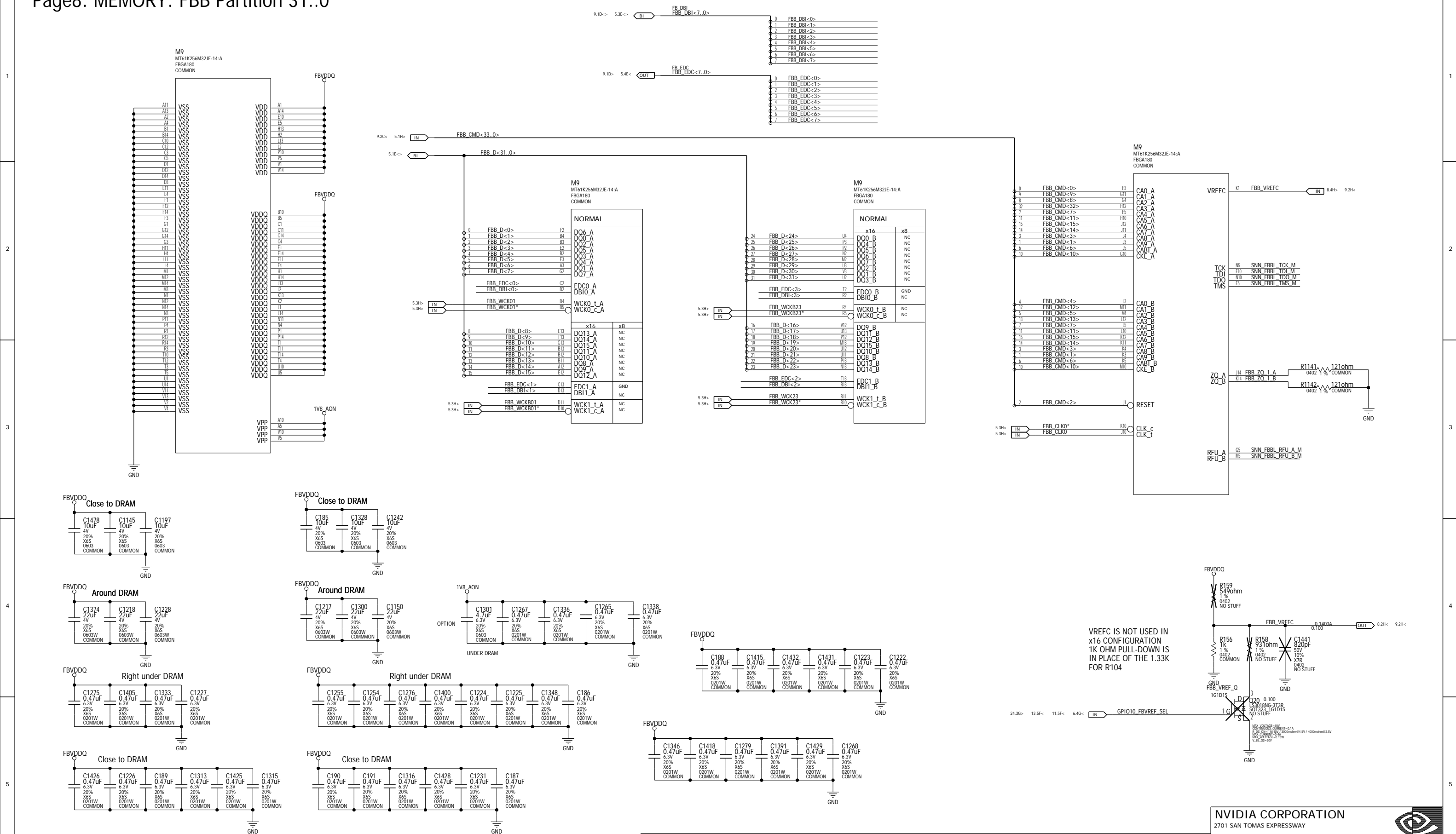
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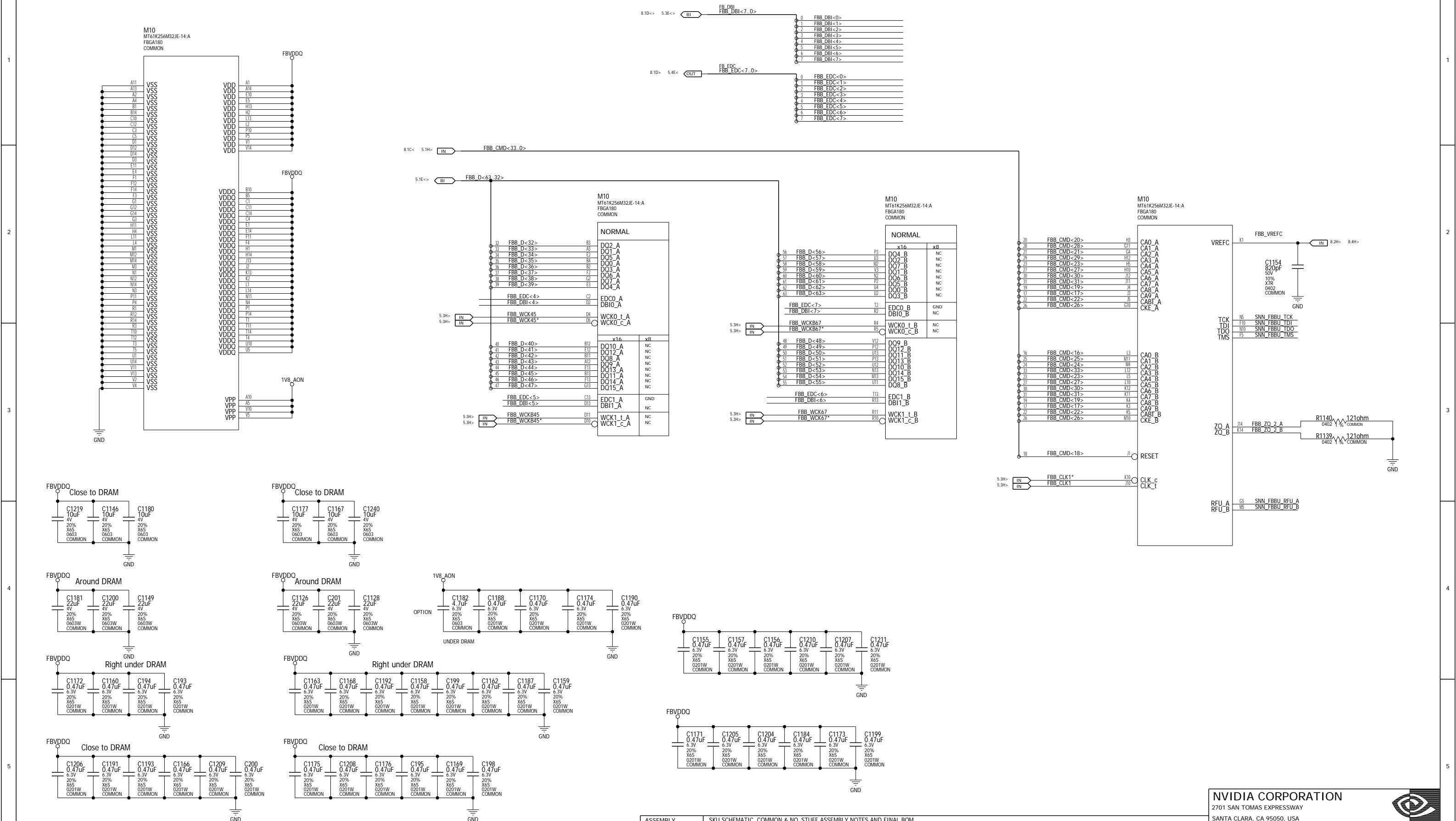


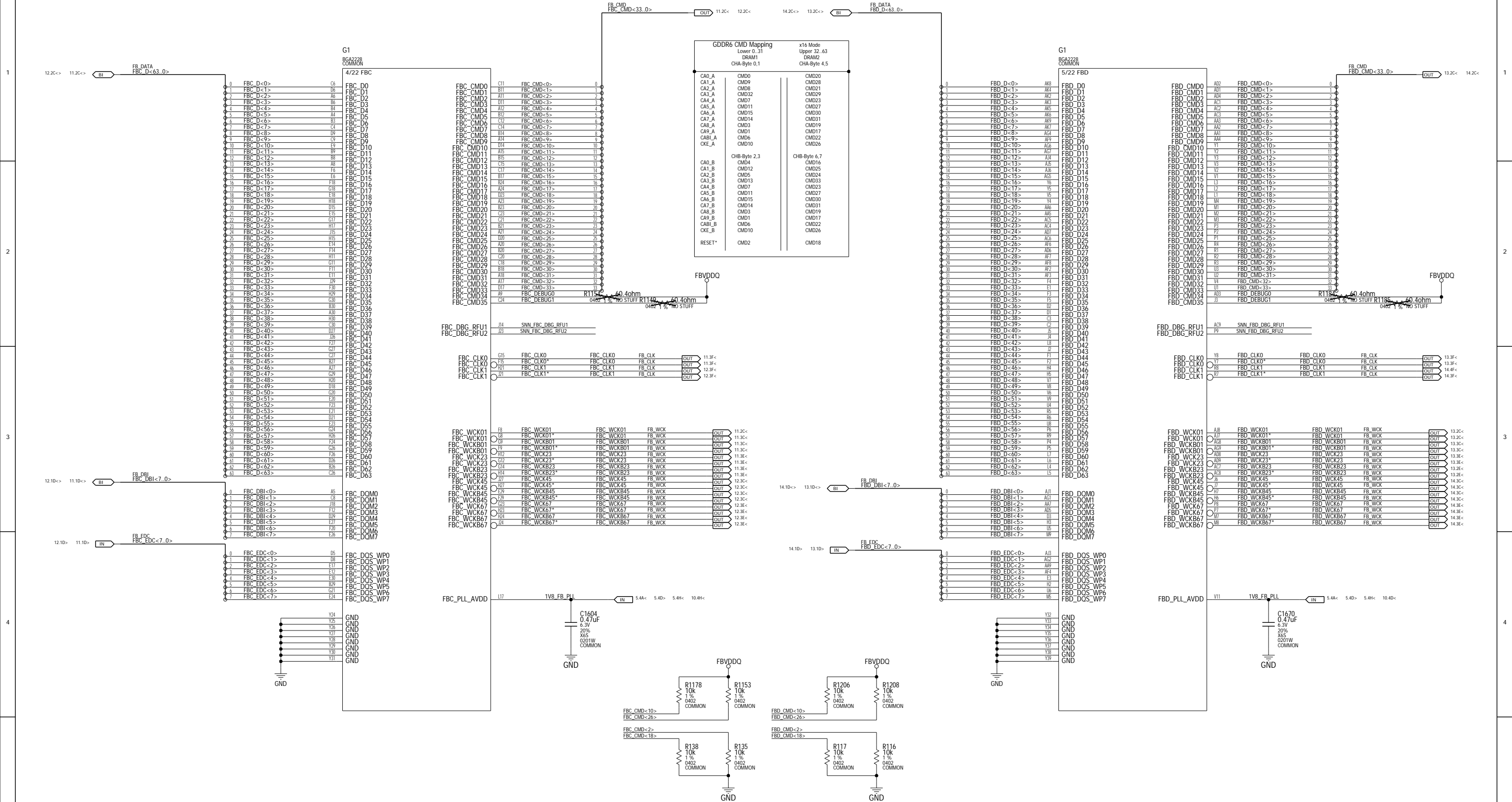
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PAGE DETAIL	MEMORY: FBB Partition 31..0

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Page9: MEMORY: FBB Partition 63..32





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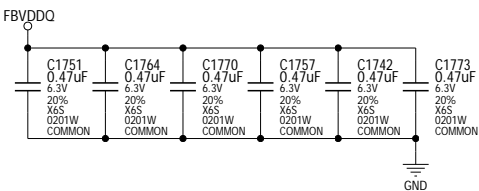
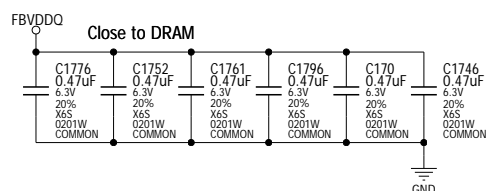
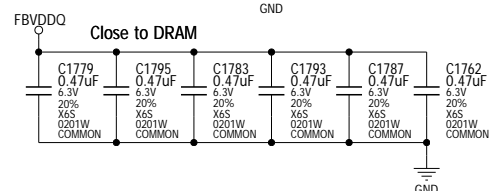
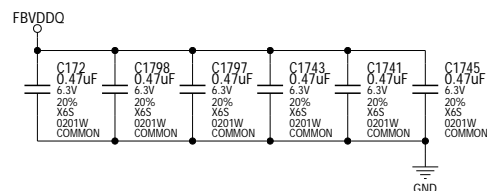
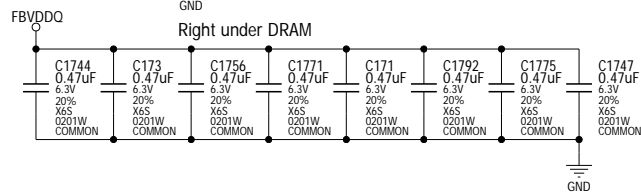
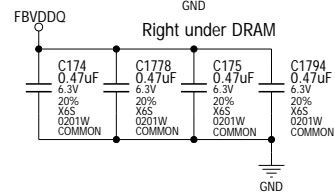
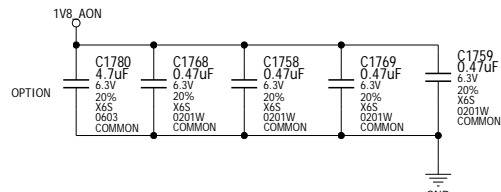
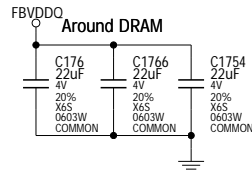
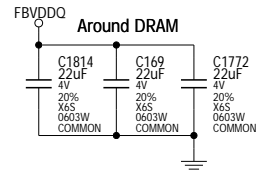
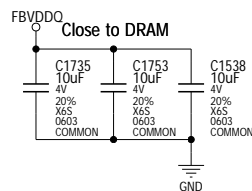
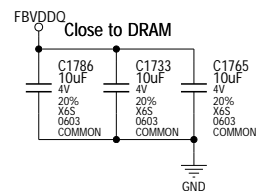
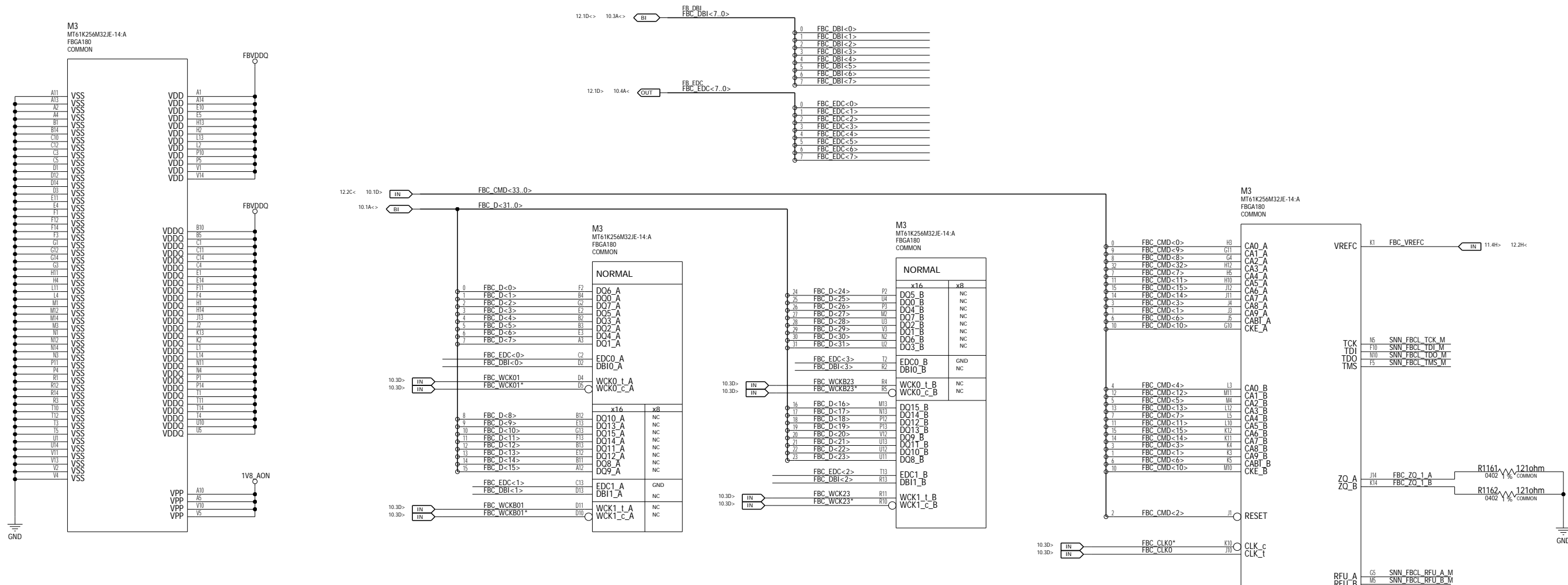
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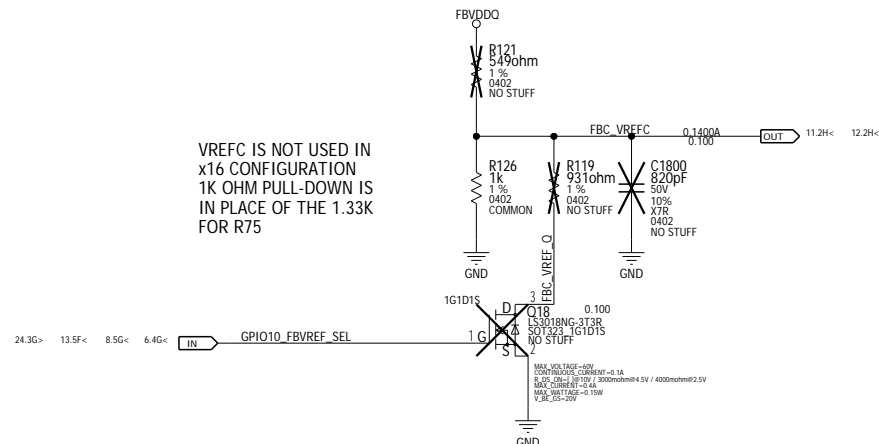
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PAGE DETAIL	MEMORY: GPU Partition C/D



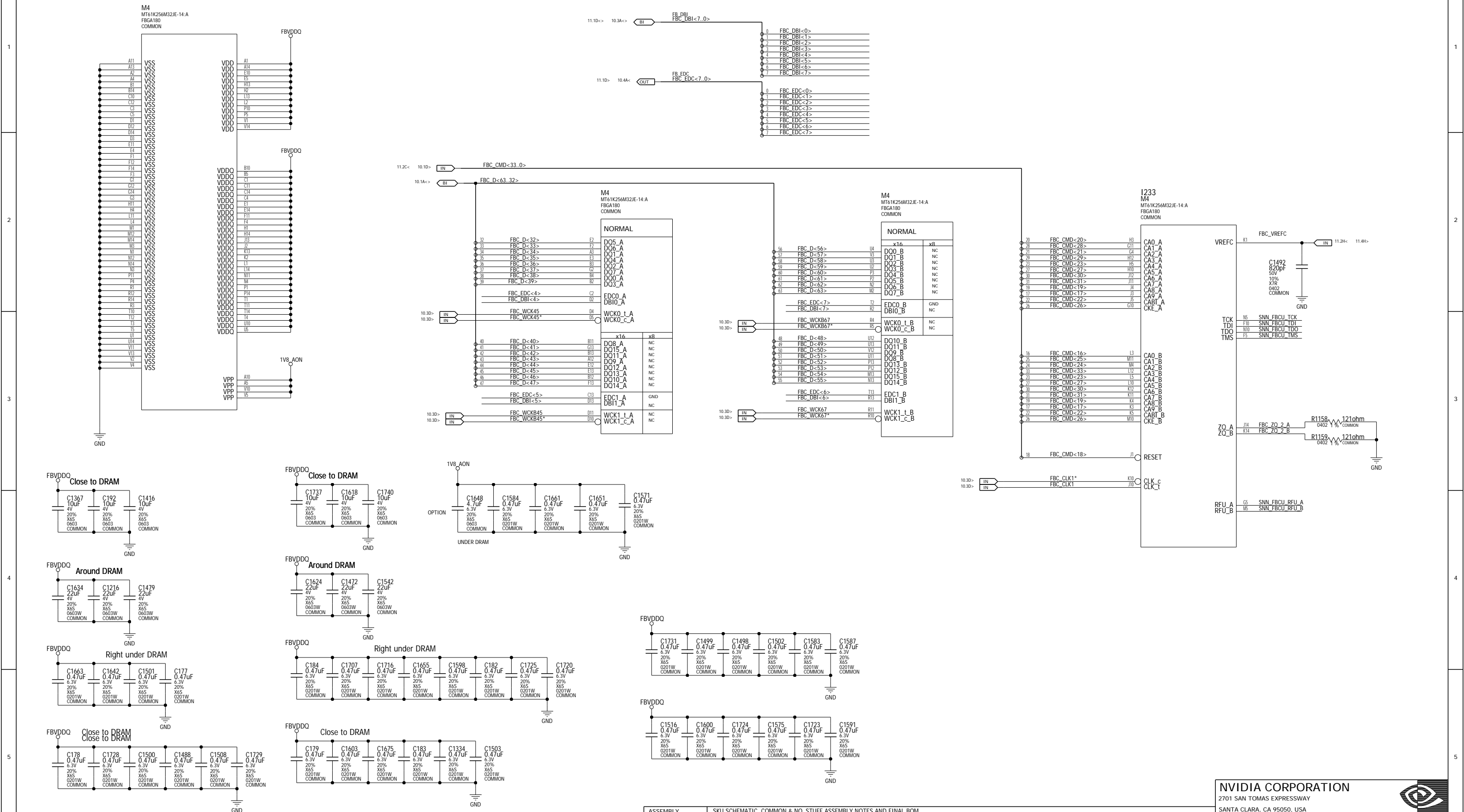
VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R75



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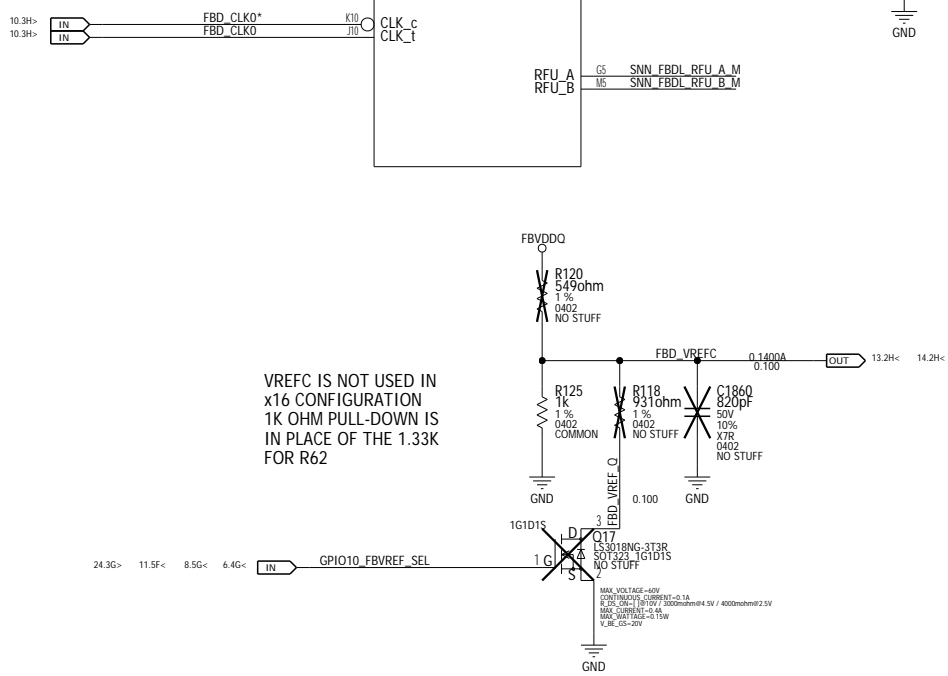
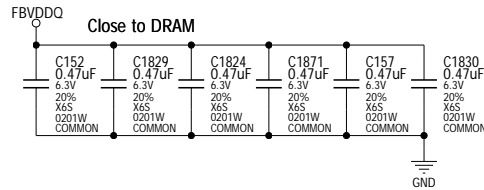
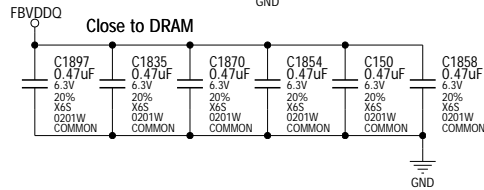
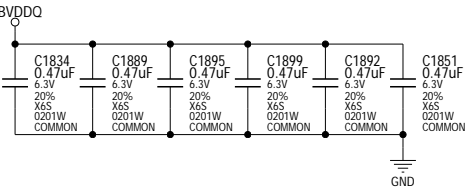
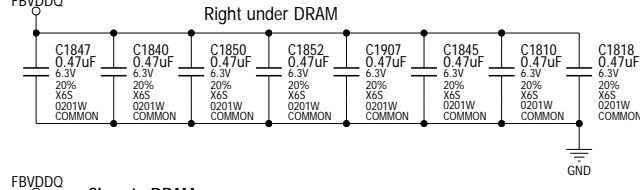
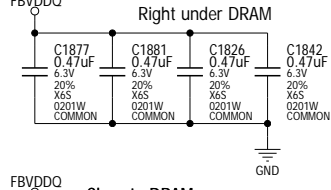
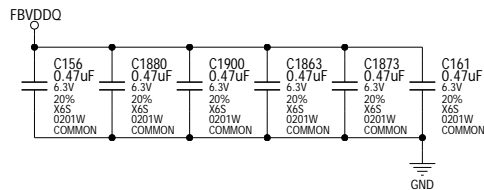
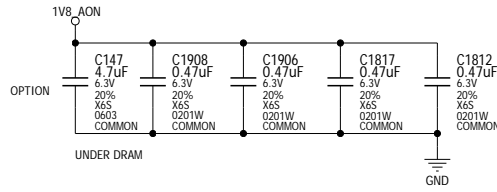
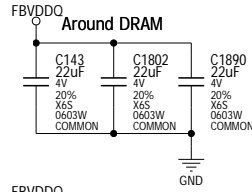
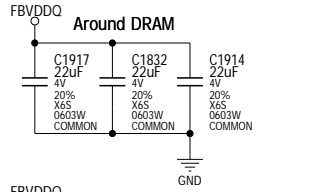
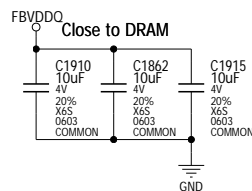
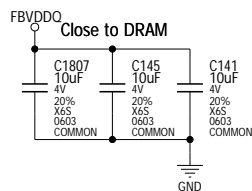
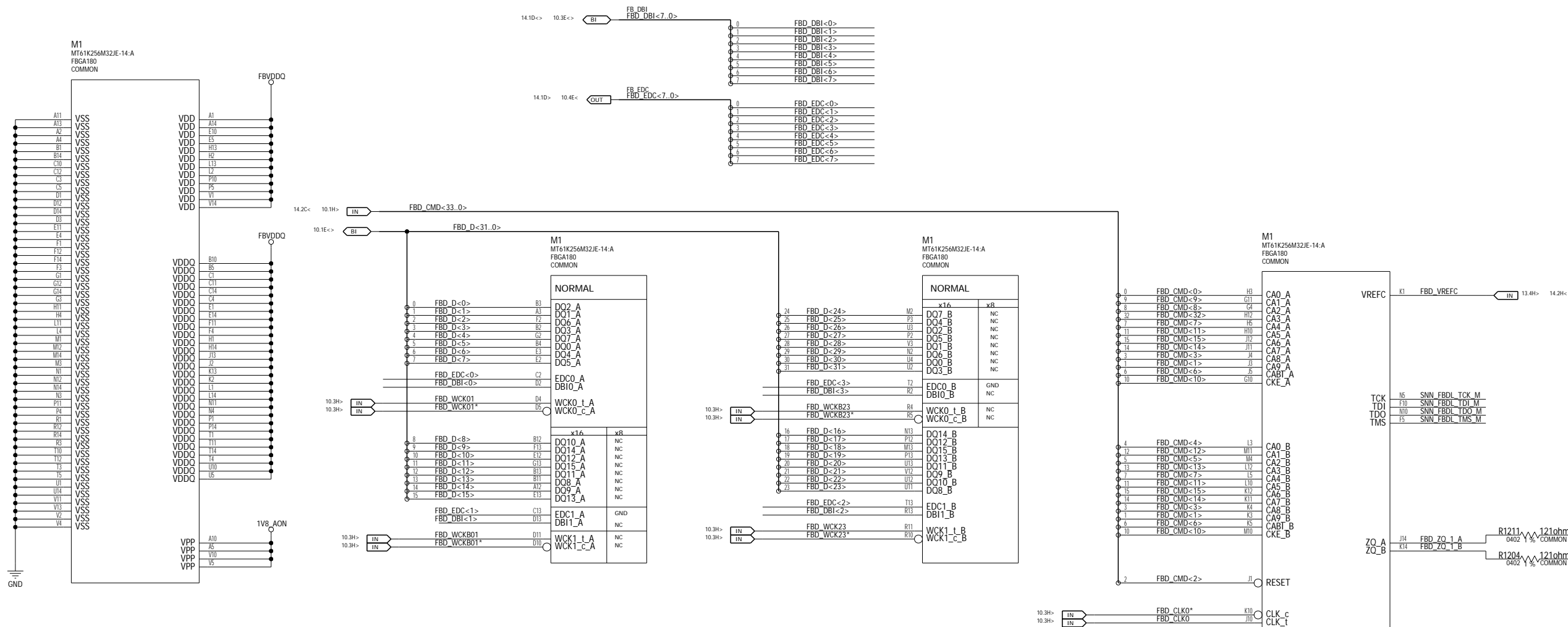
Page12: MEMORY: FBC Partition 63..32



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PAGE DETAIL	MEMORY: FBC Partition 63..32

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VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R62

ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	MEMORY: FBD Partition 31..0

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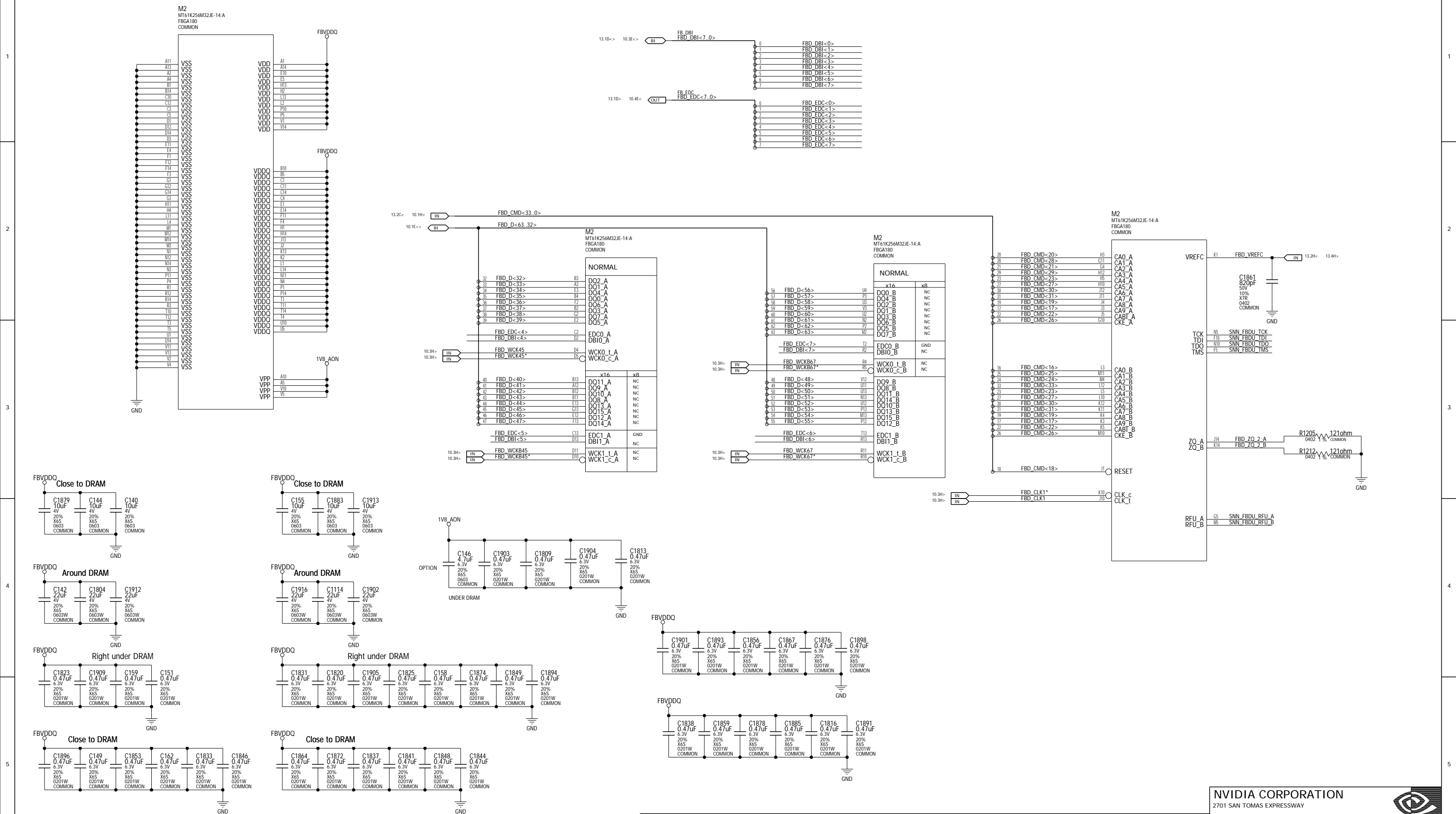
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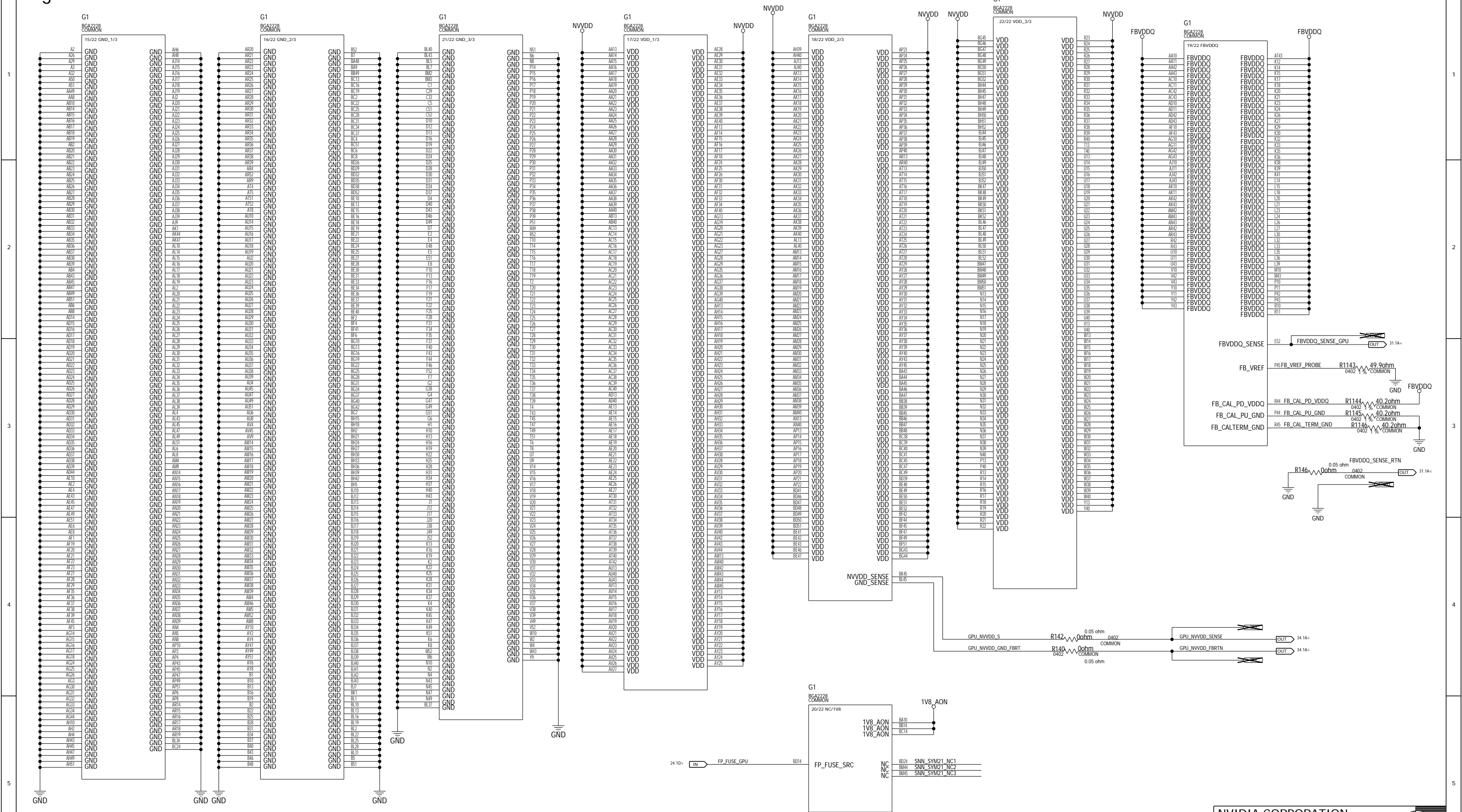
Page14: MEMORY: FBD Partition 63..32

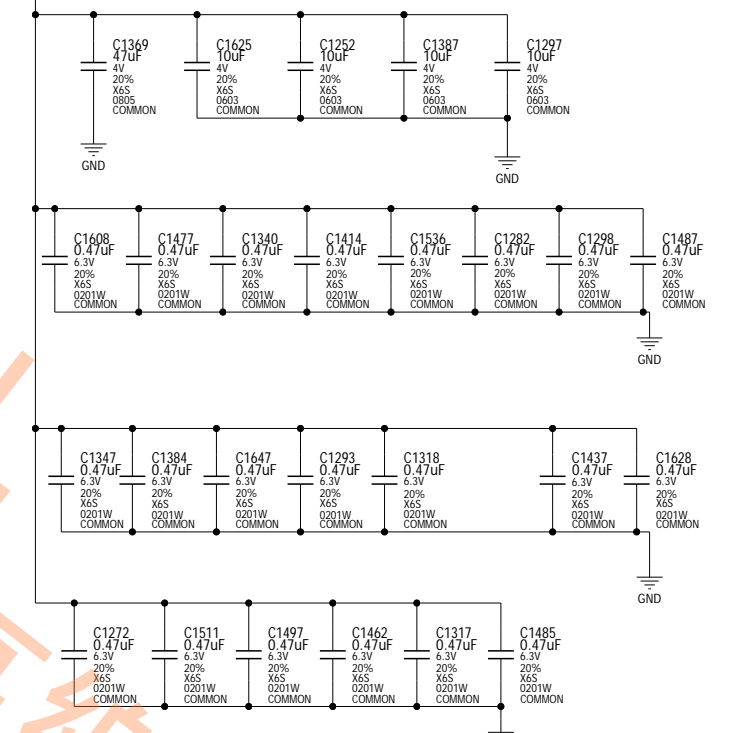


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PAGE DETAIL	MEMORY: FBD Partition 63..32

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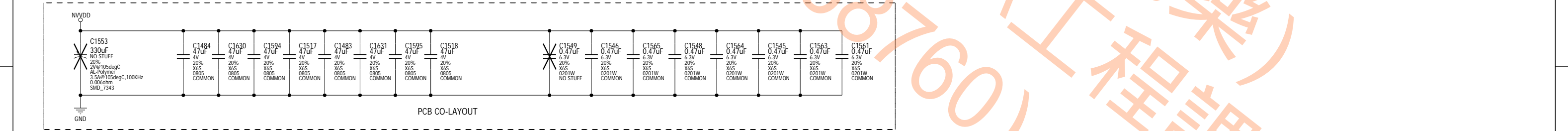
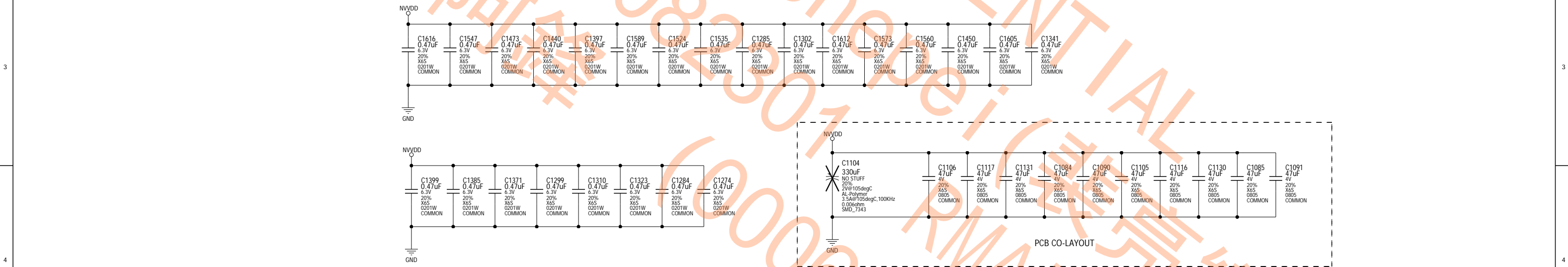
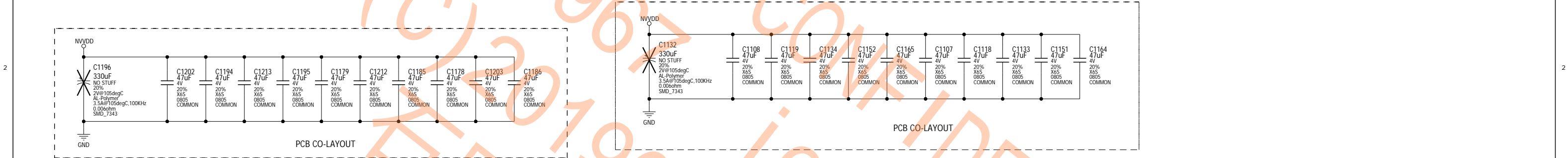
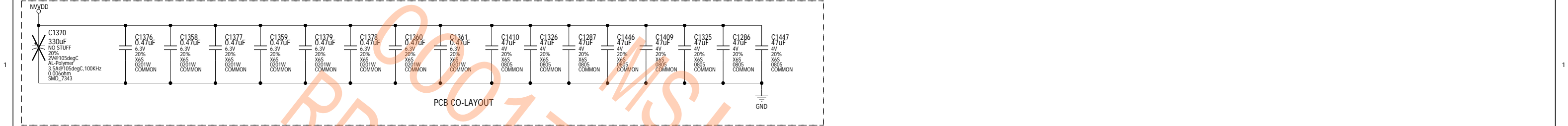
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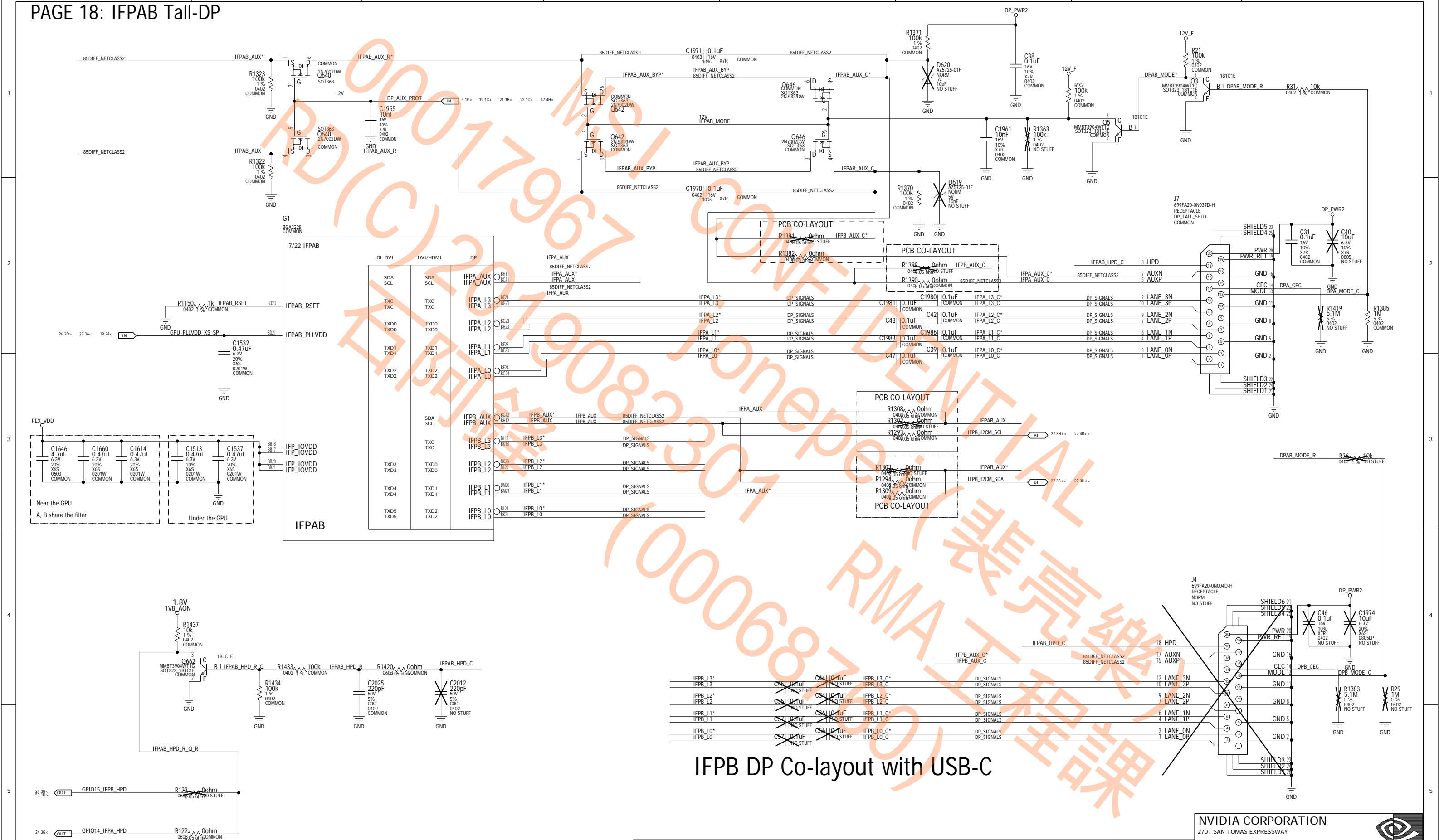


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Page17: GPU Decoupling




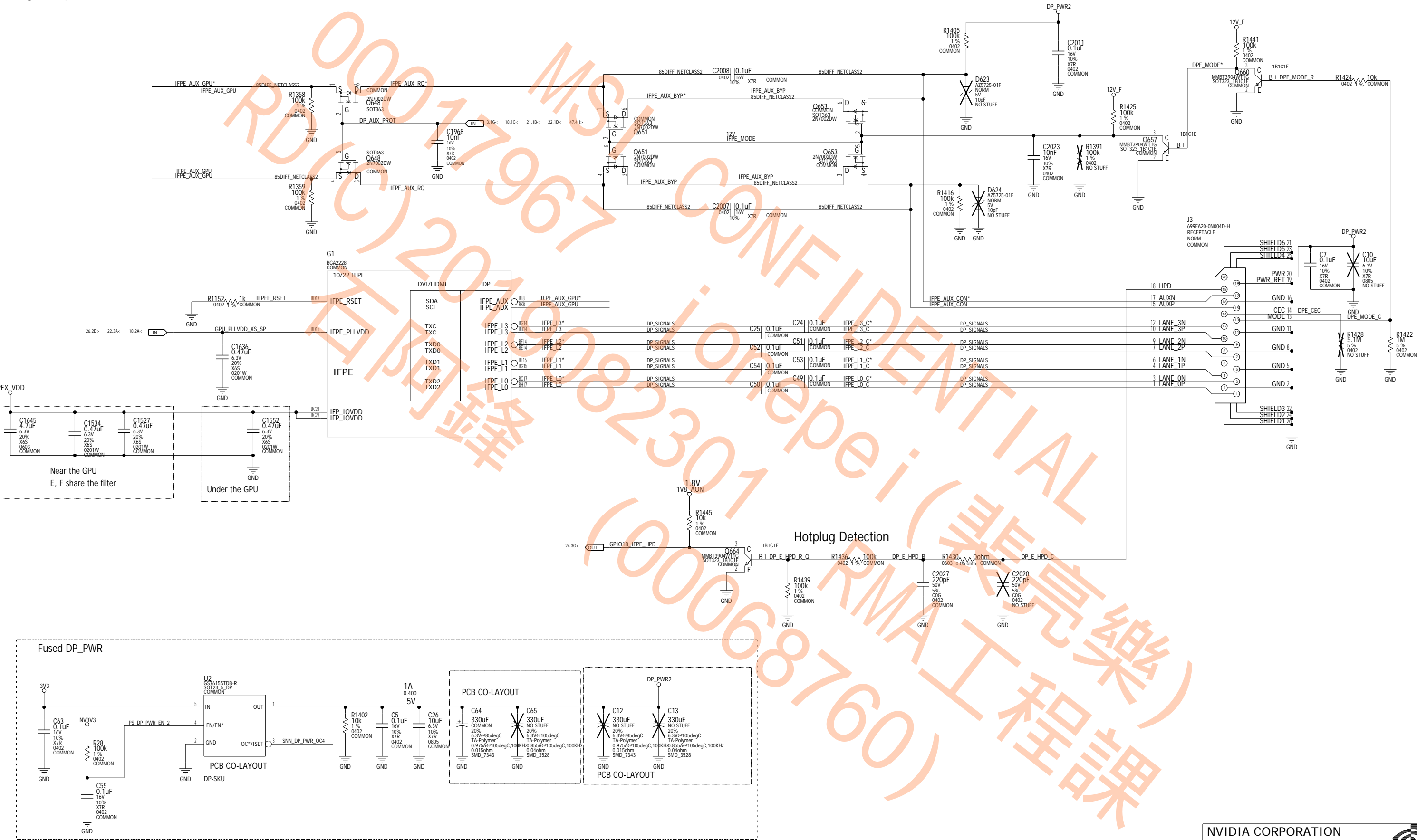
PAGE 18: IFPAB Tall-DP



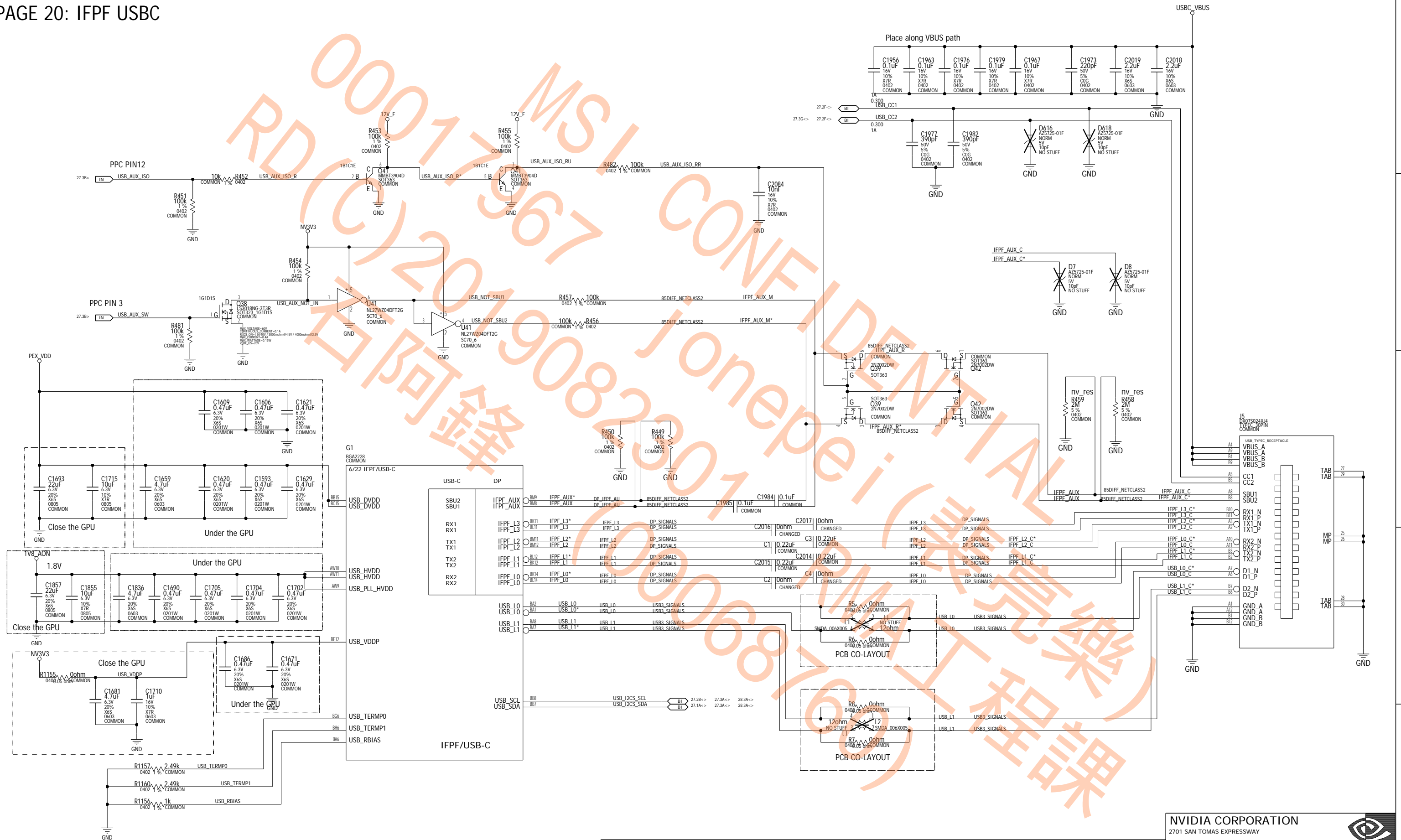
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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	IFPAB TALL-DP

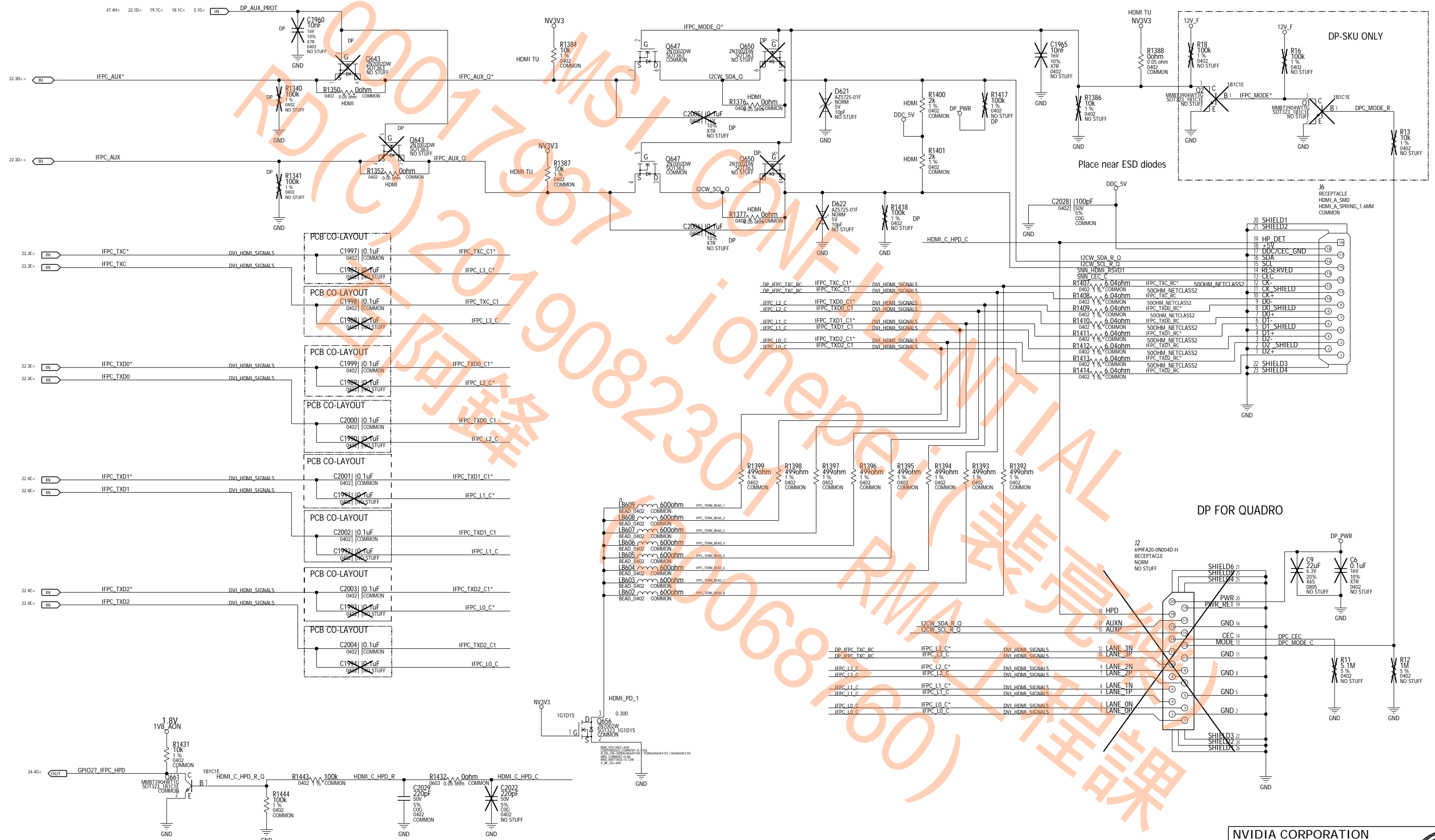
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
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PAGE 21:IFPC HDMI 2.0/DP



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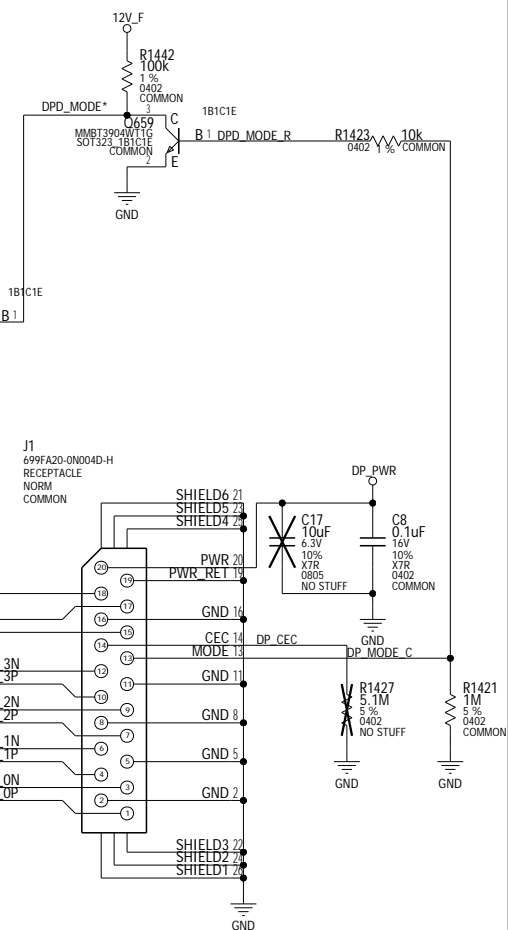
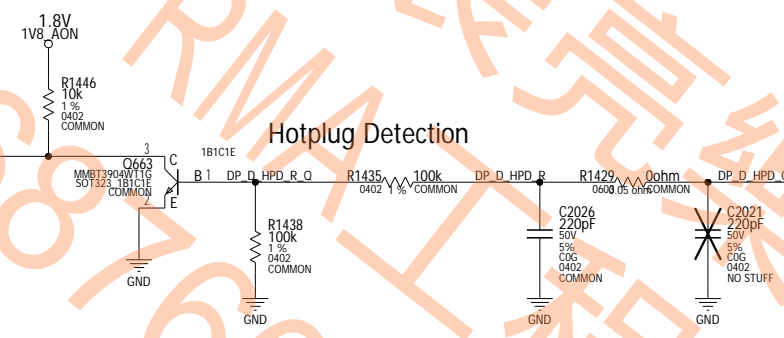
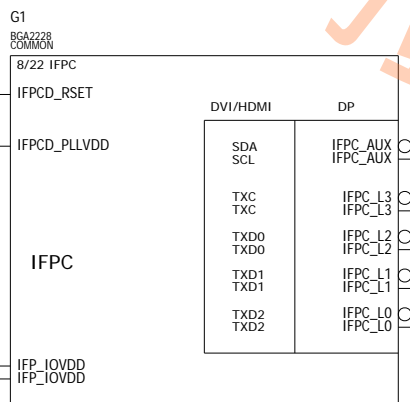
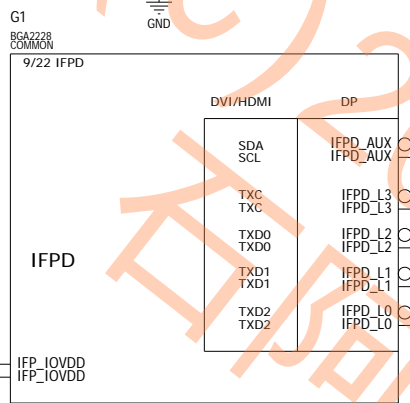
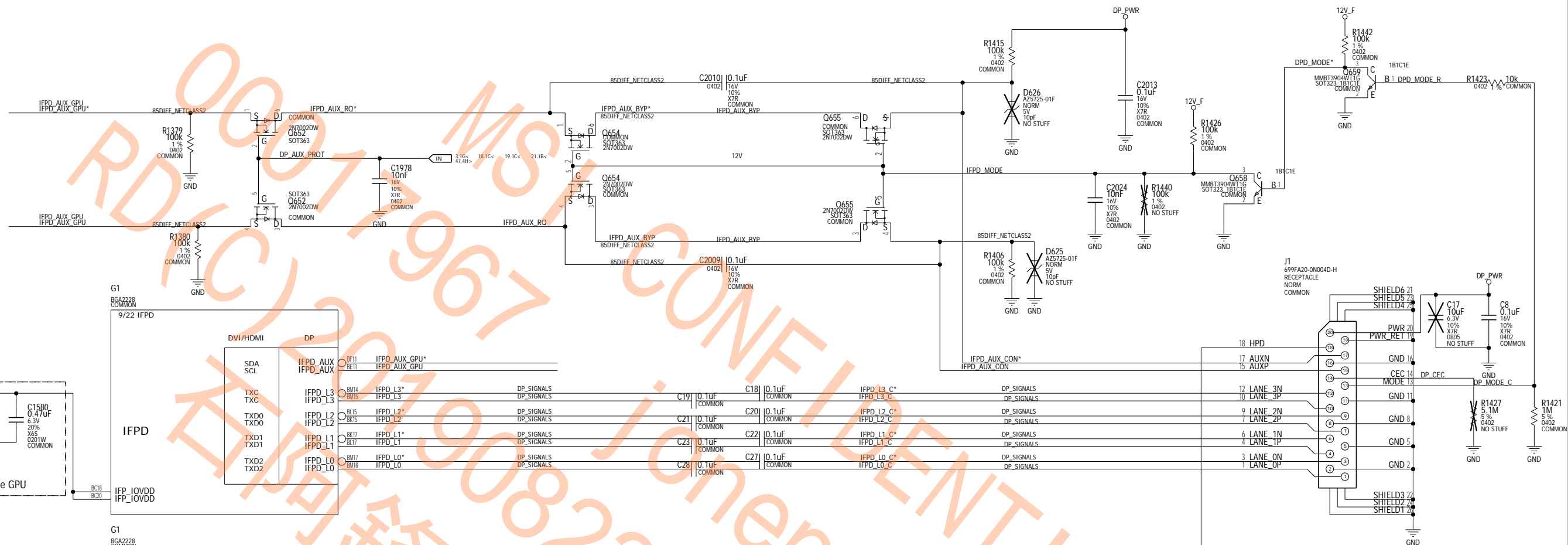
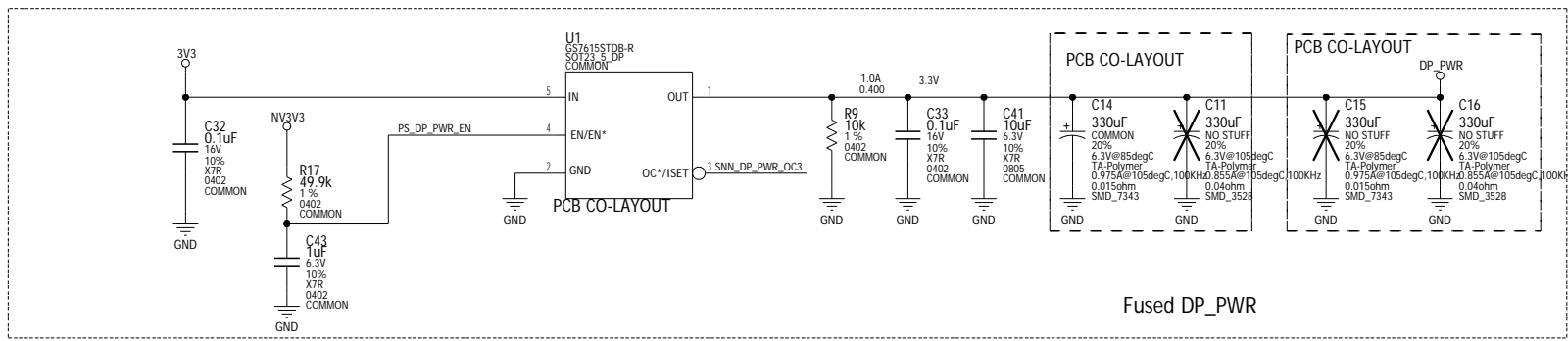
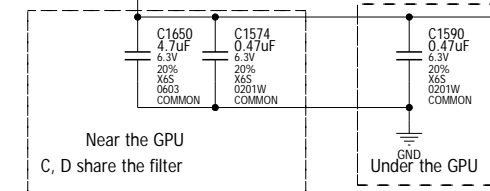
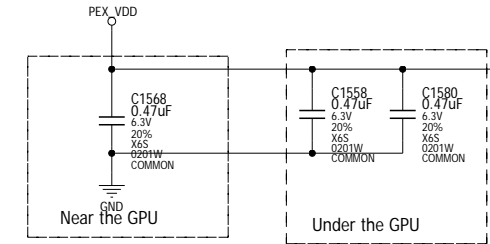
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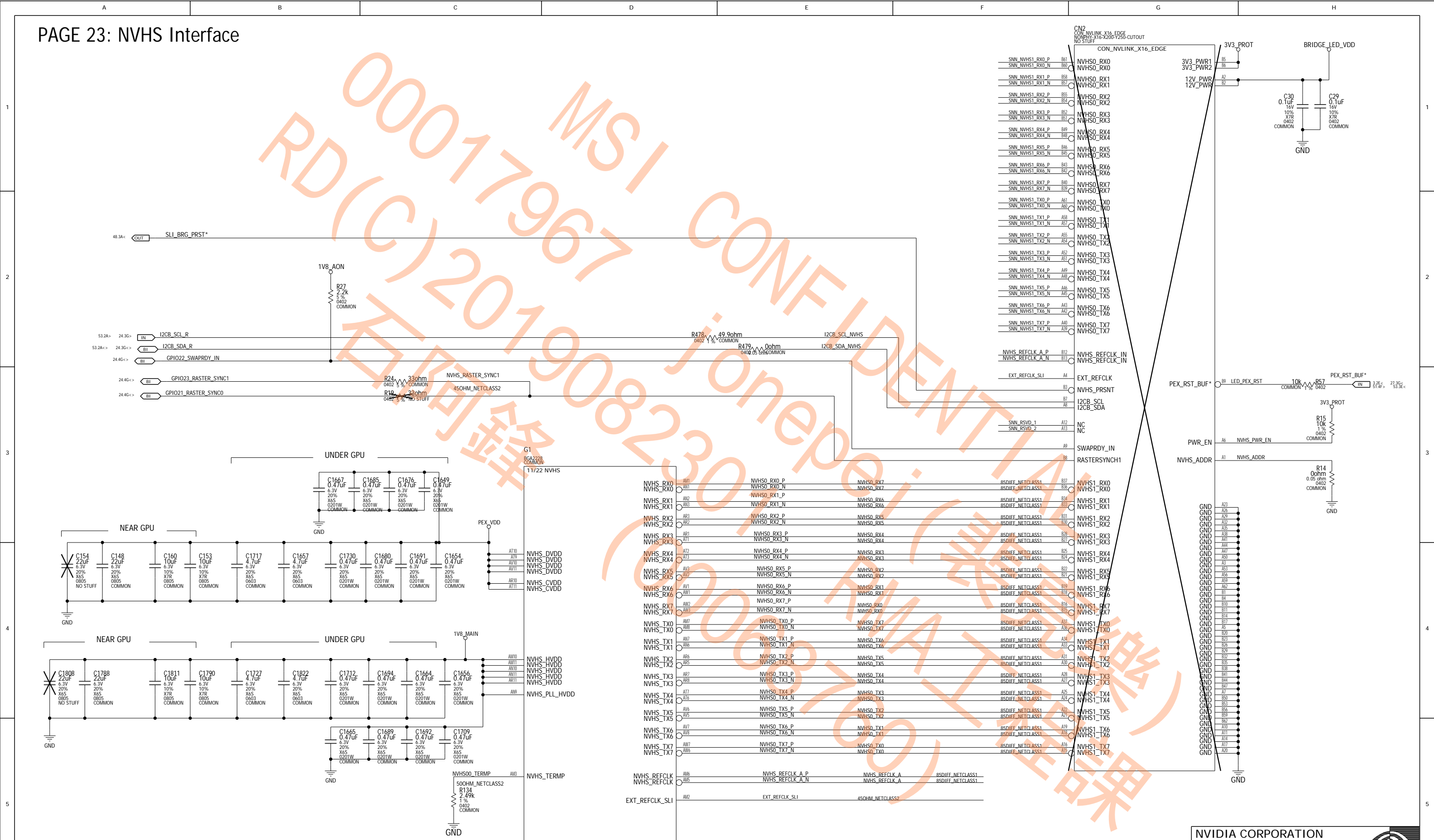
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PAGE 23: NVHS Interface



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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	NVHS INTERFACE

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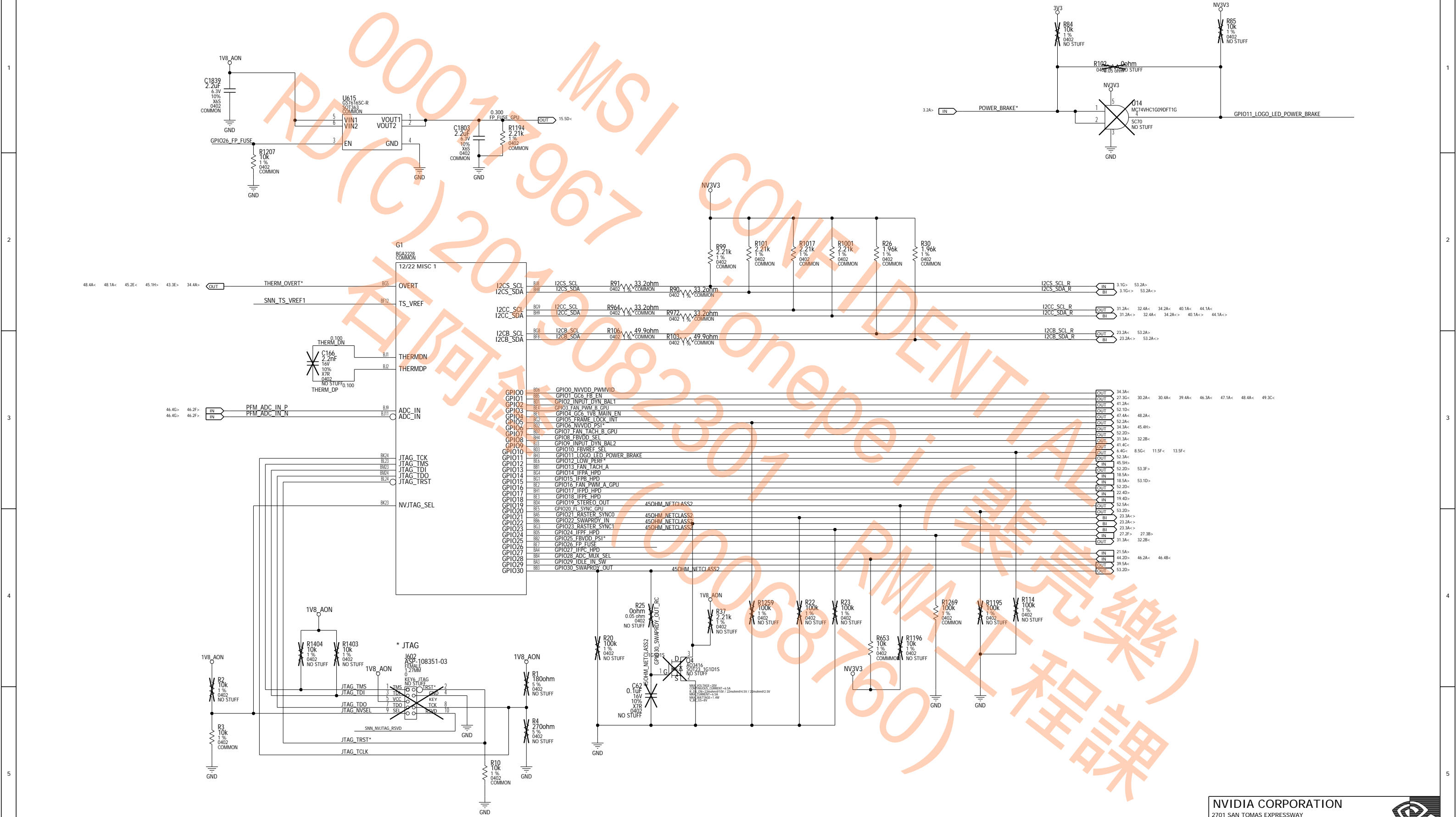
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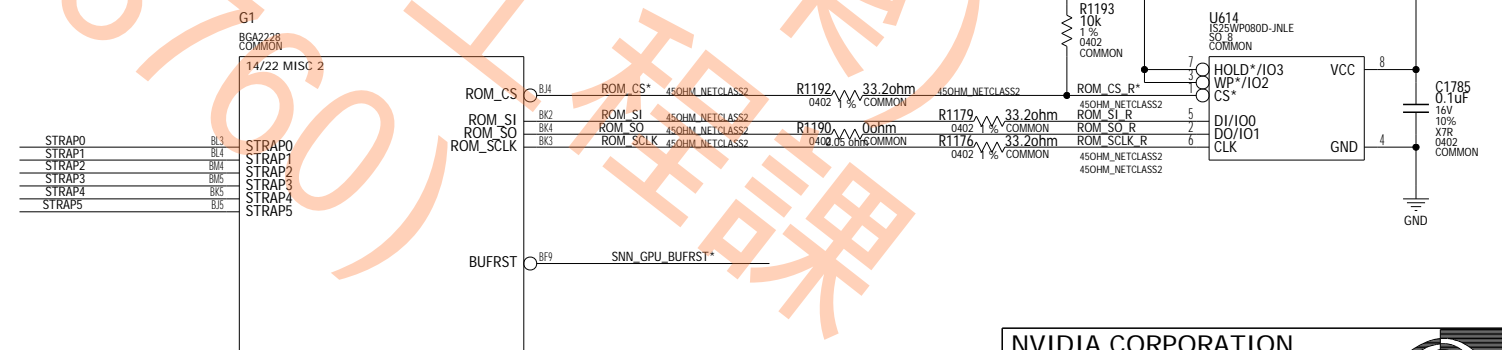
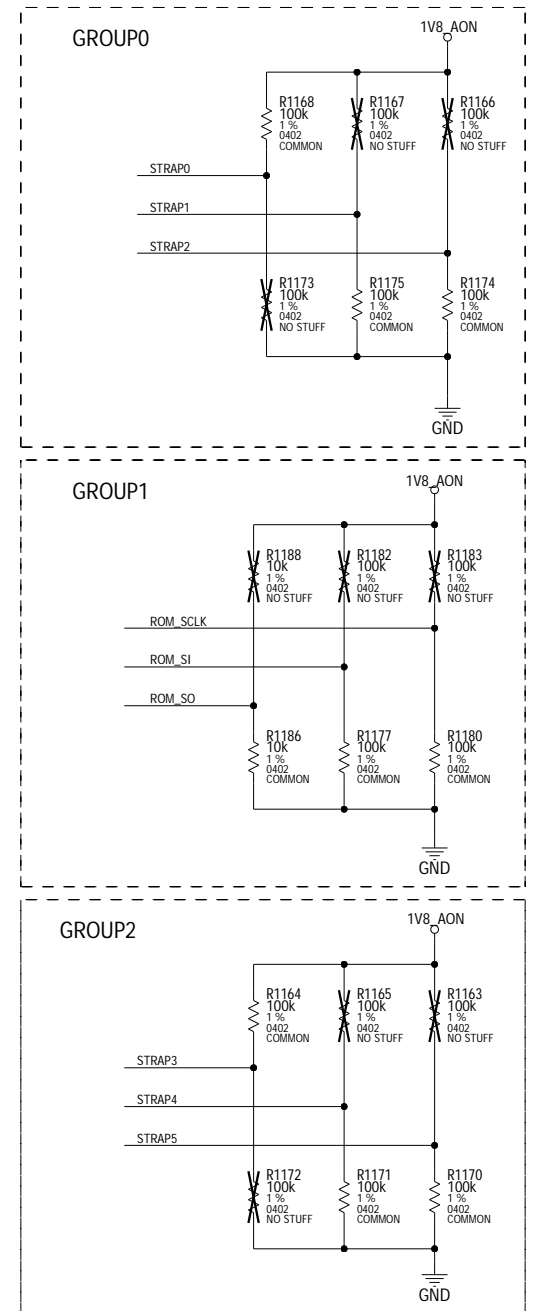
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

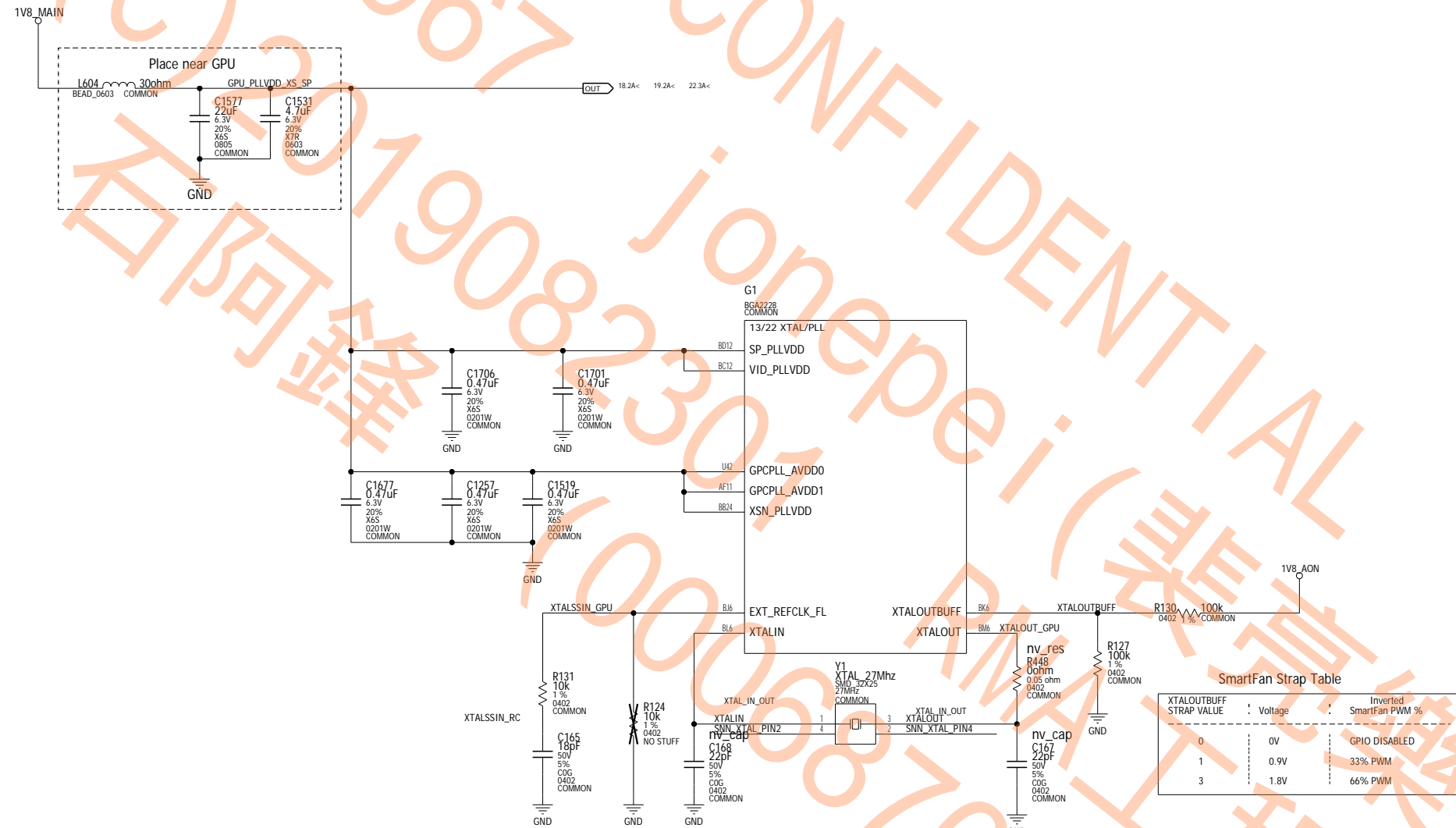
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		
L	L	L	00000	RAMCFG TBD	DEFAULT
L	L	H	00001	RAMCFG TBD	
L	H	L	00010	RAMCFG TBD	
L	H	H	00011	RAMCFG TBD	
H	H	L	00110	RAMCFG TBD	
H	H	H	00111	RAMCFG TBD	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

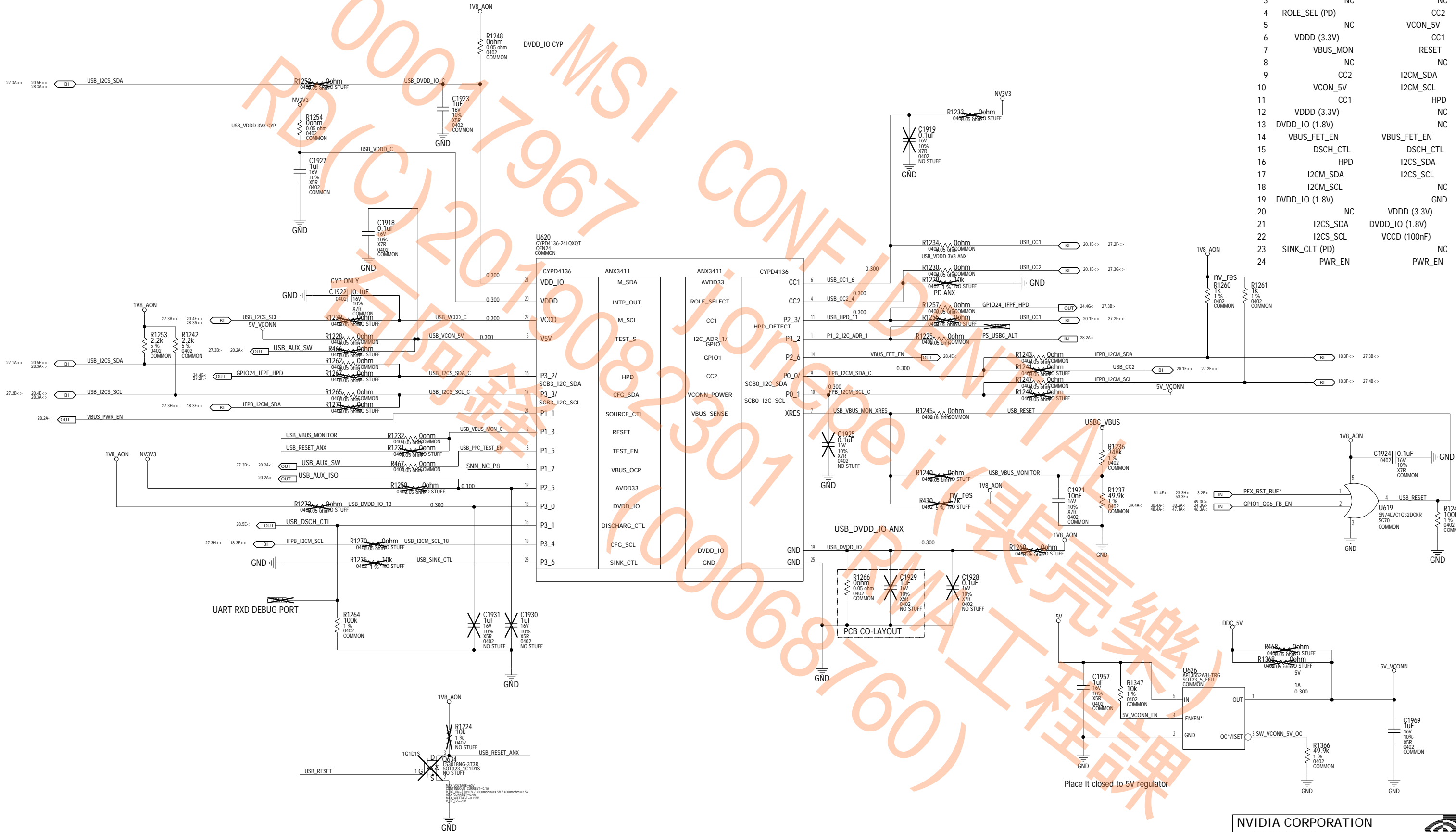
RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	1:SMB_ALT_ADDR ENABLE
M	L	H	1	1	0	1	0:SMB_ALT_ADDR DISABLE
M	L	L	1	1	0	0	1:DEVID_SEL REBRAND
L	H	M	1	0	1	1	0:DEVID_SEL ORIGNAL
L	M	H	1	0	1	0	1:PCIE_CFG LOW POWER
L	M	L	1	0	0	1	0:PCIE_CFG HIGH POWER
L	L	M	1	0	0	0	1:VGA_DEVICE ENABLE
H	H	H	0	1	1	1	0:VGA_DEVICE DISABLE
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	



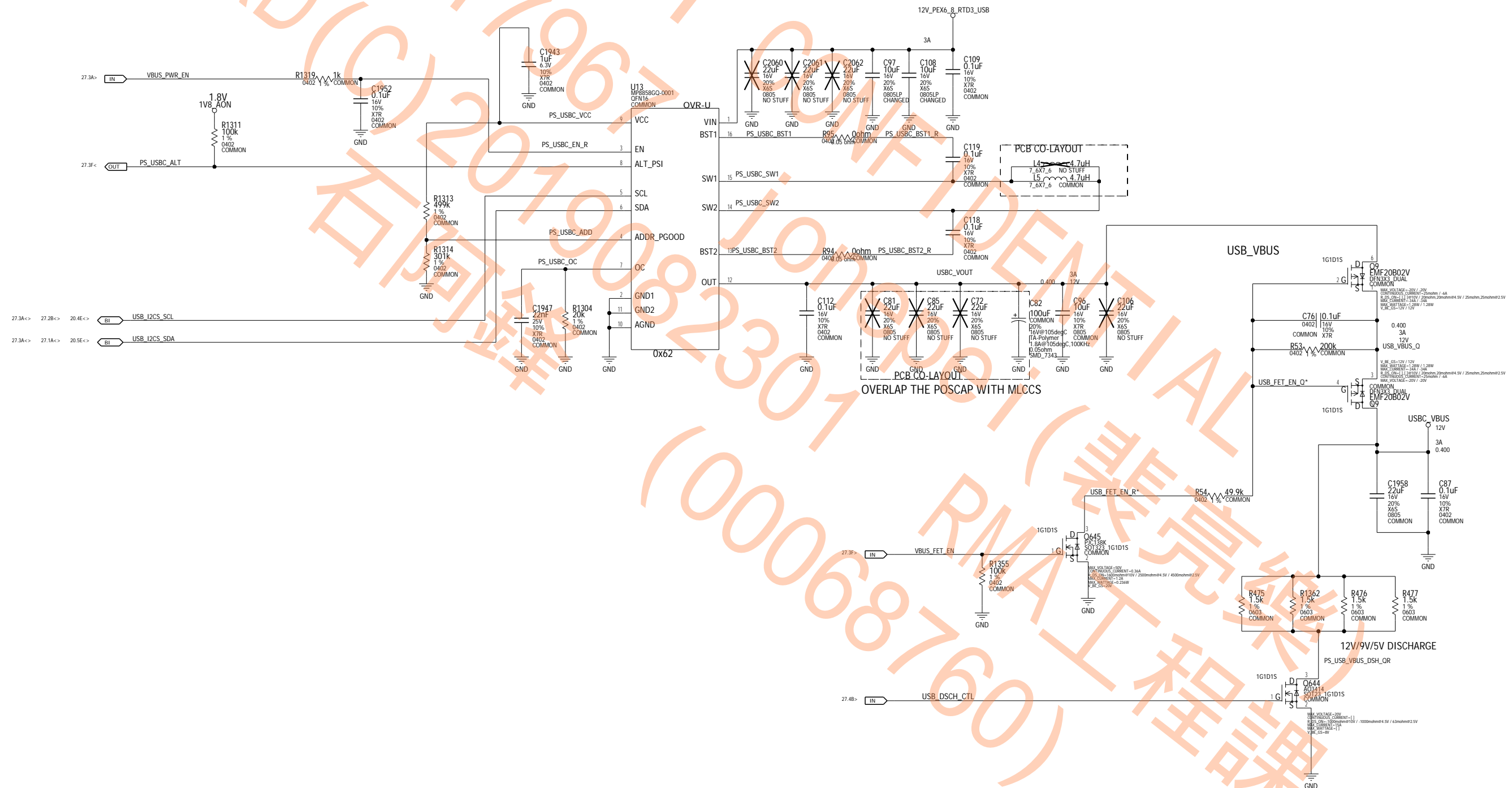


XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	0.9V	33% PWM
3	1.8V	66% PWM



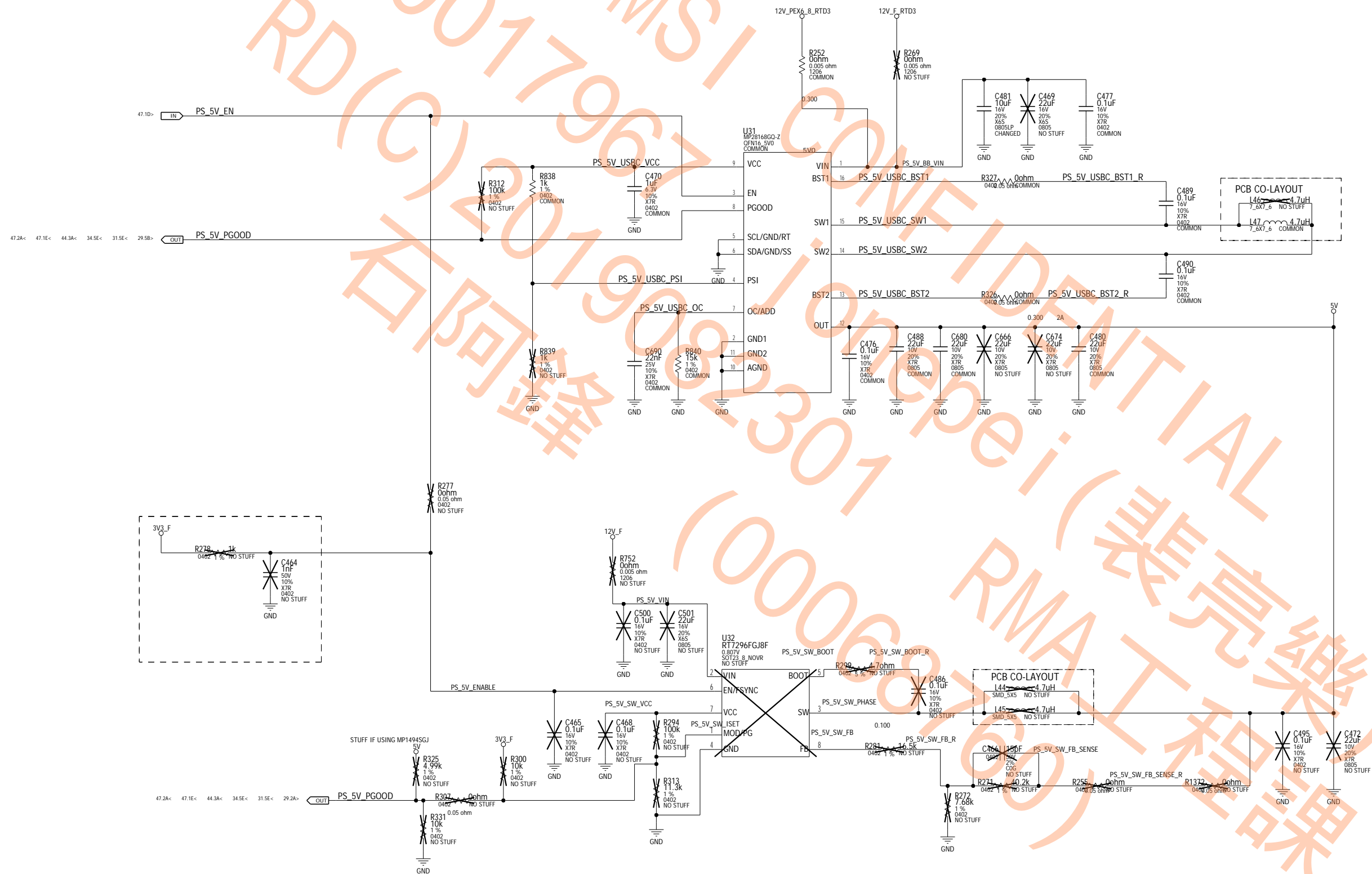
PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN

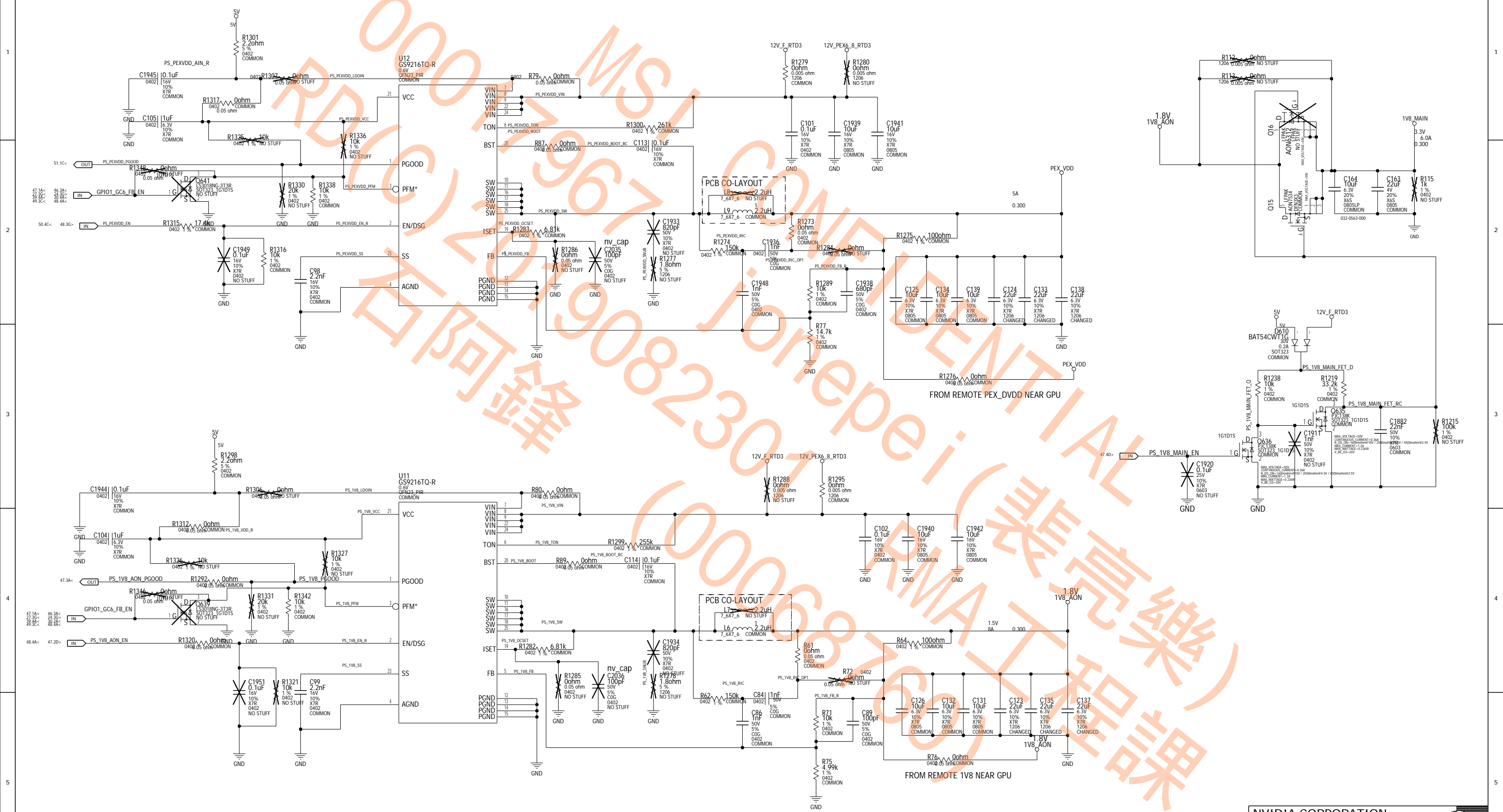
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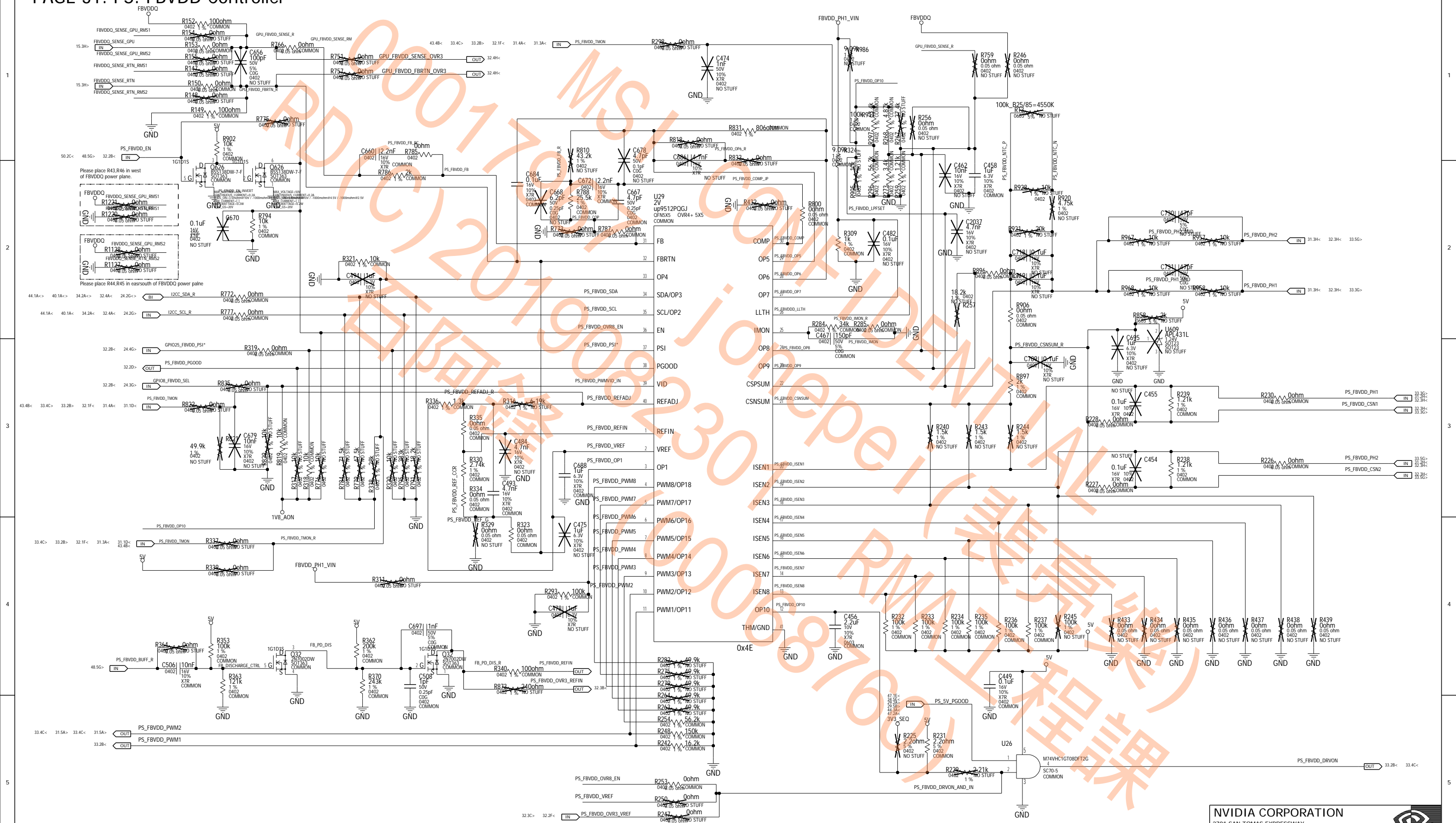
ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PS: USB VR

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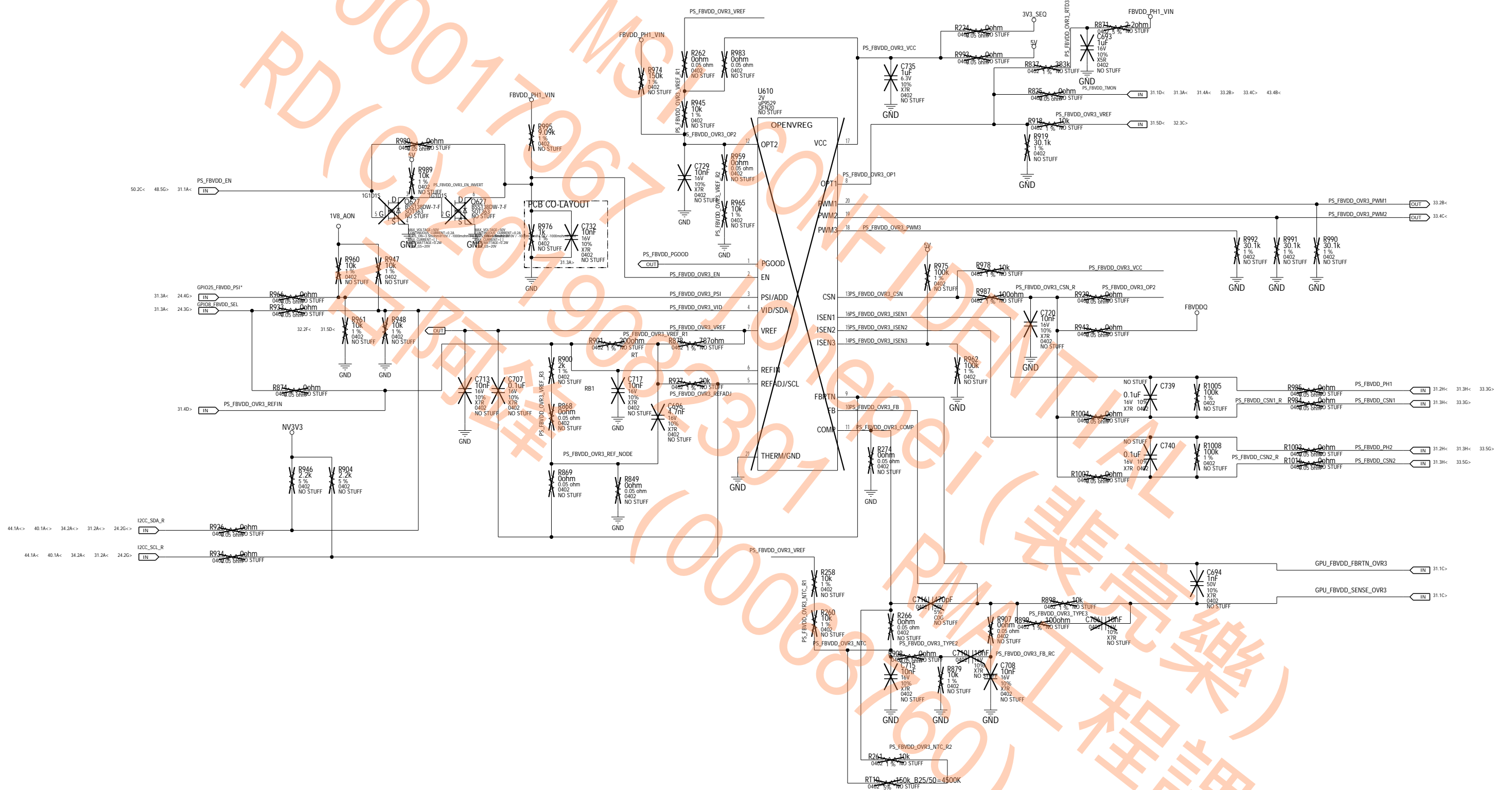
PAGE 31: PS: FBVDD Controller



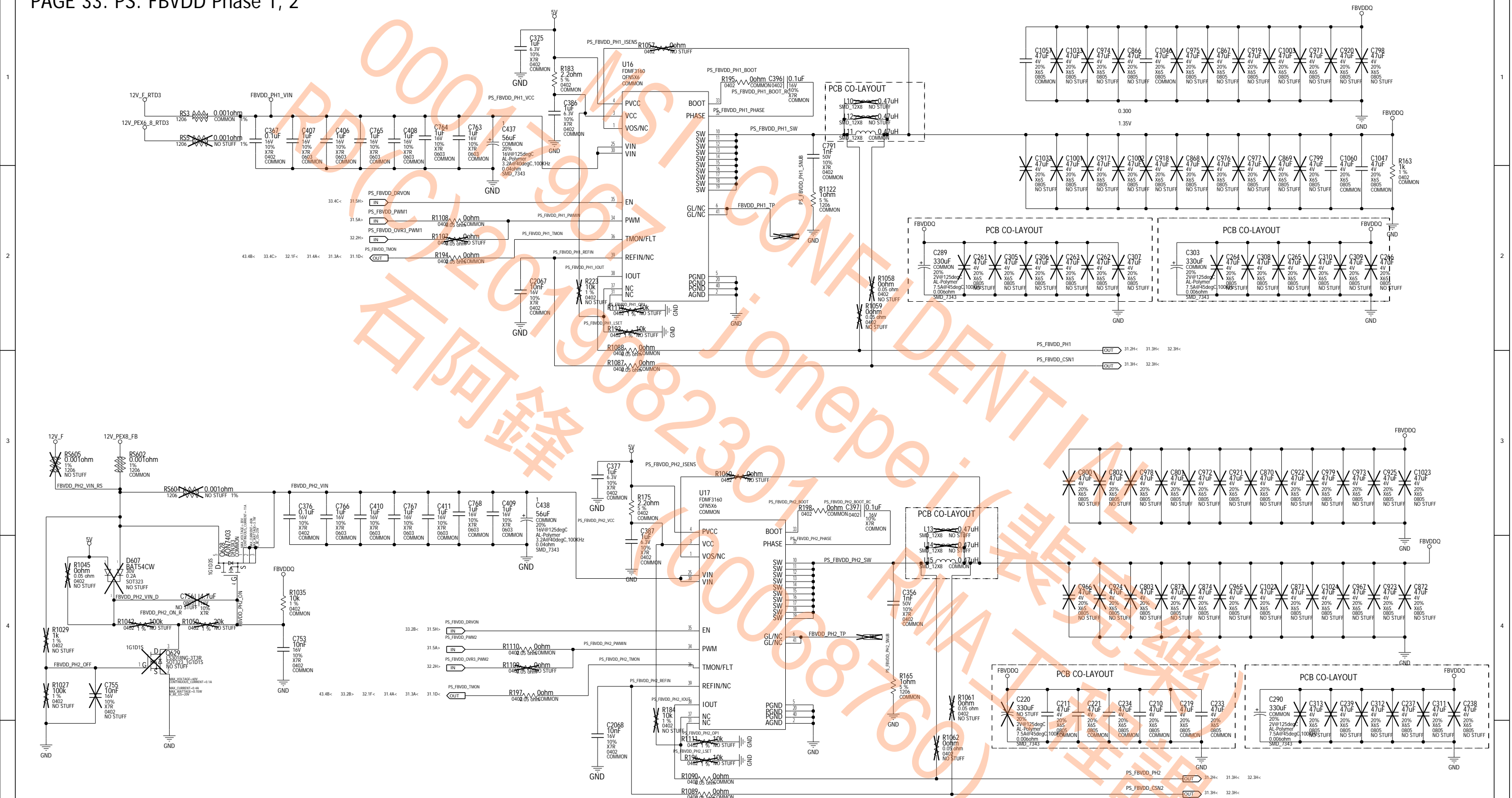
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PAGE DETAIL	PS: FBVDD CONTROLLER

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PAGE 33: PS: FBVDD Phase 1, 2



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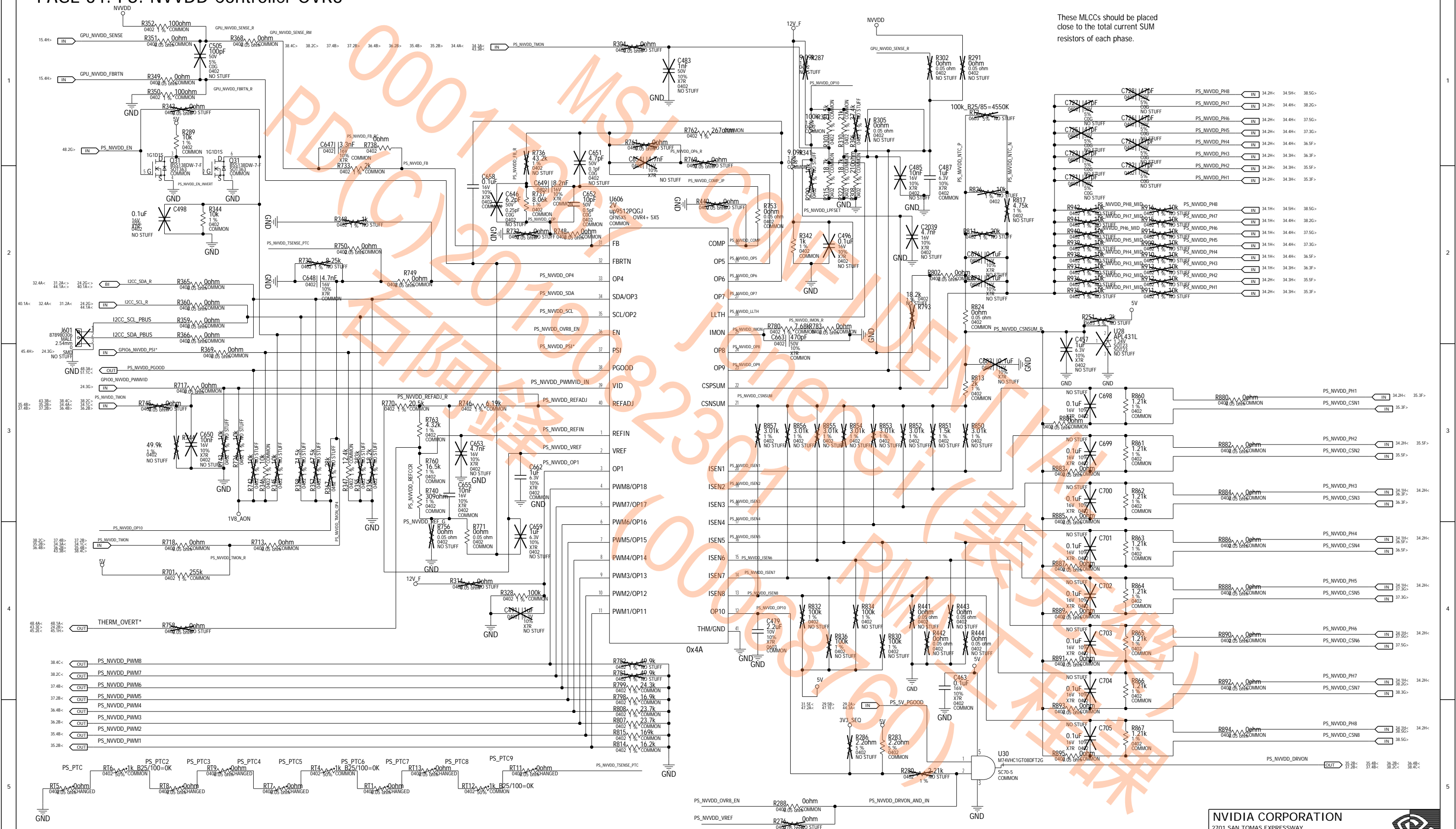
NV_PN	600-1G180-0002-700
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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PS: FBVDD PHASE 1, 2

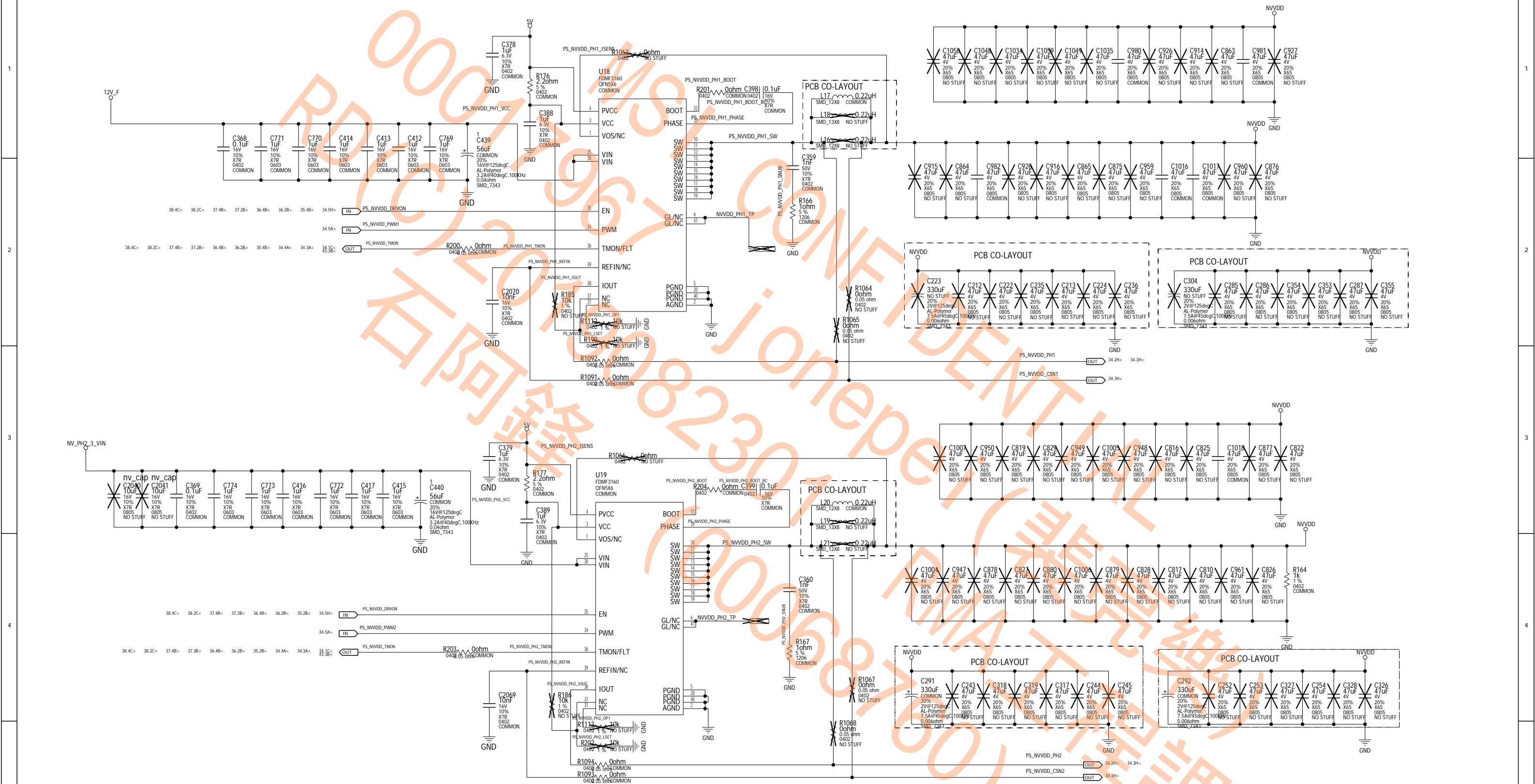
PAGE 34: PS: NVVDD Controller OVR8

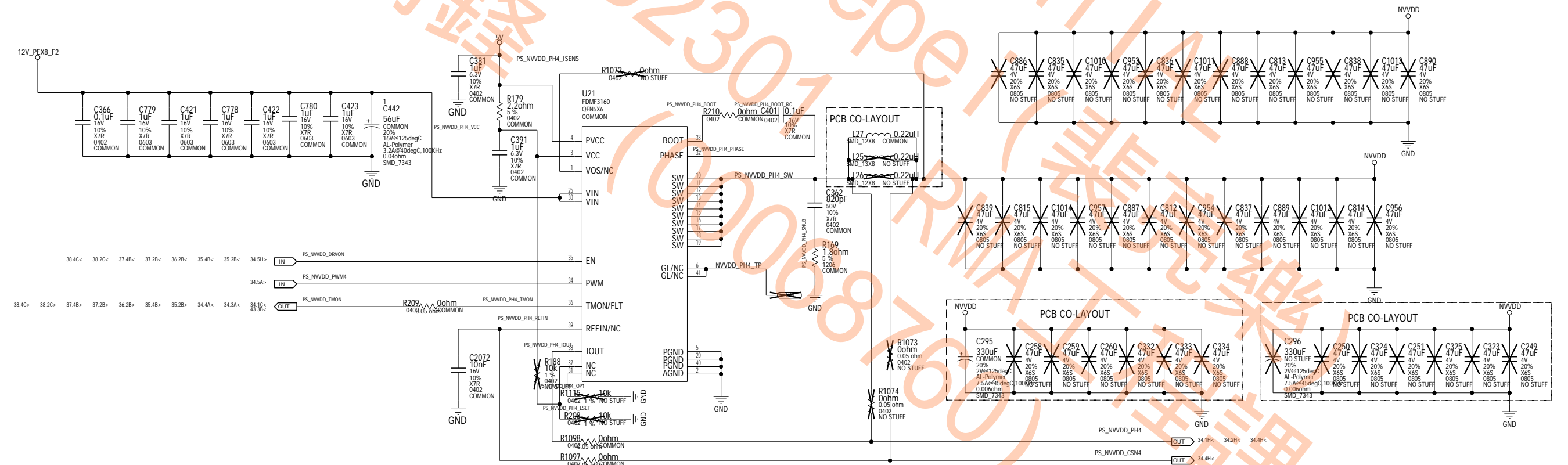
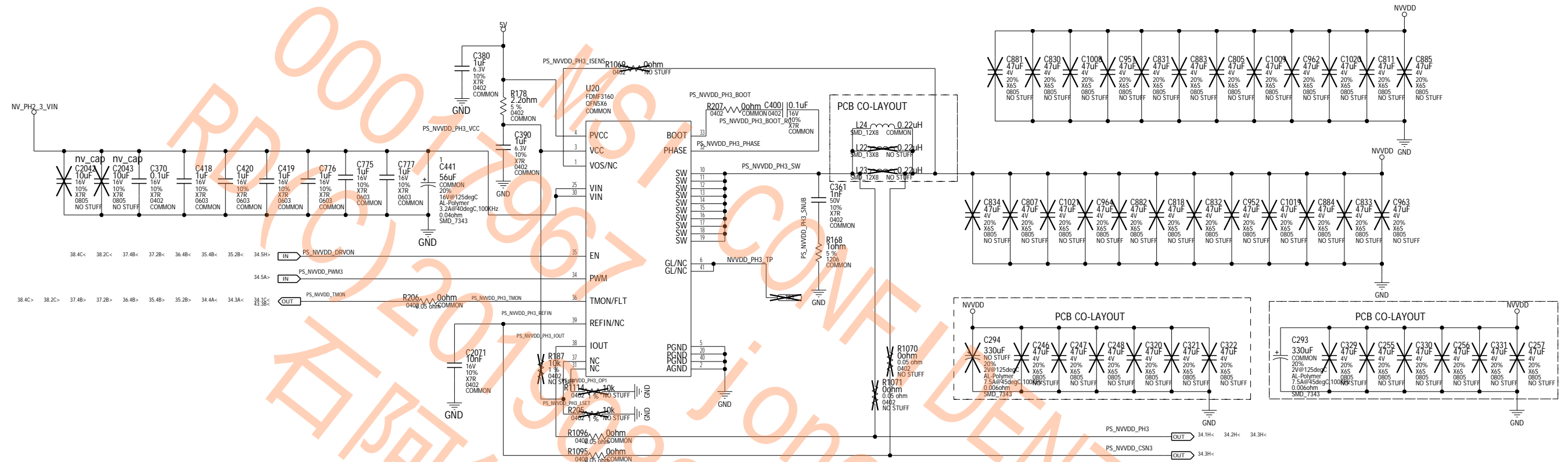


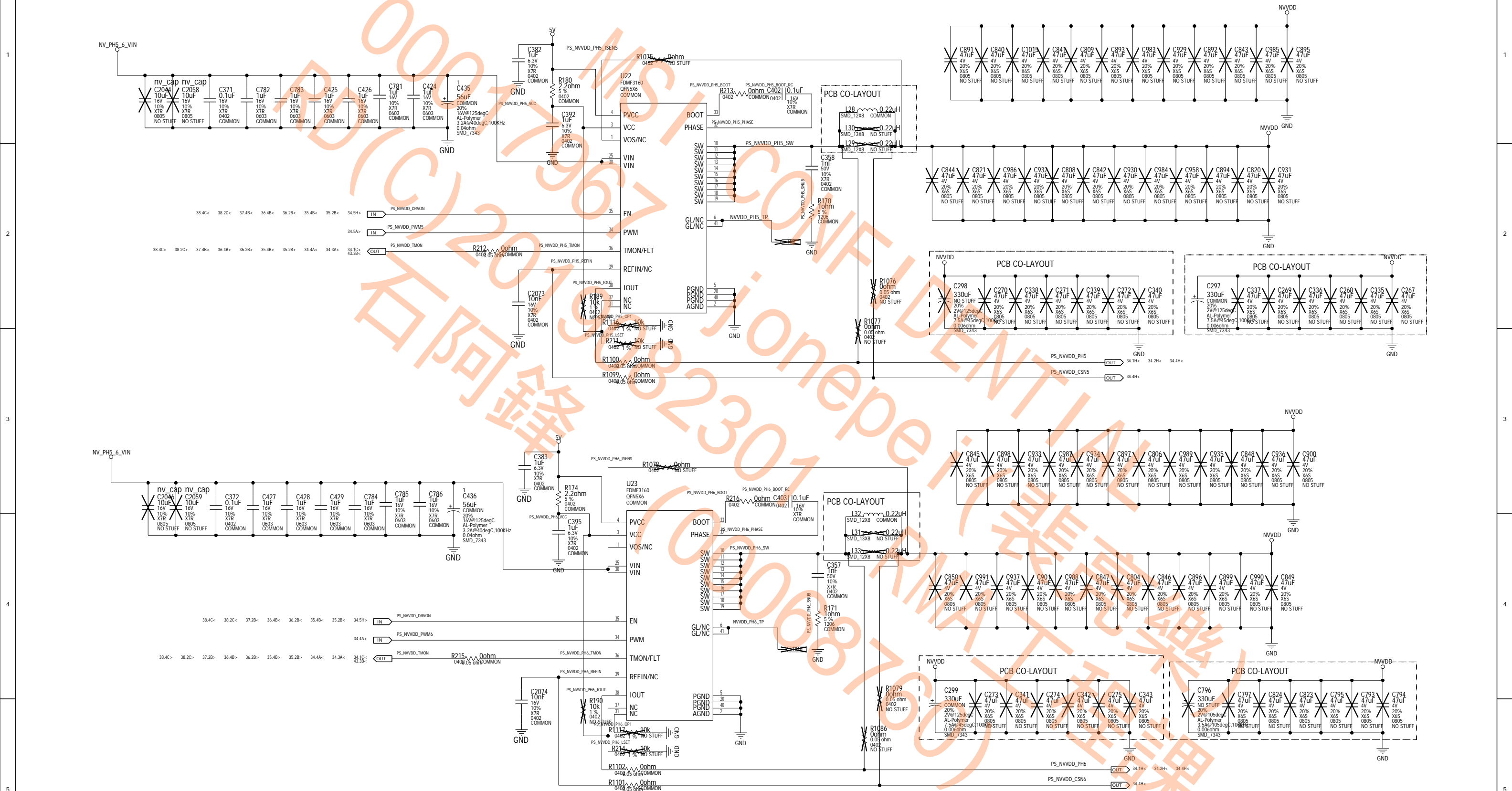
These MLCCs should be placed close to the total current SUM resistors of each phase.

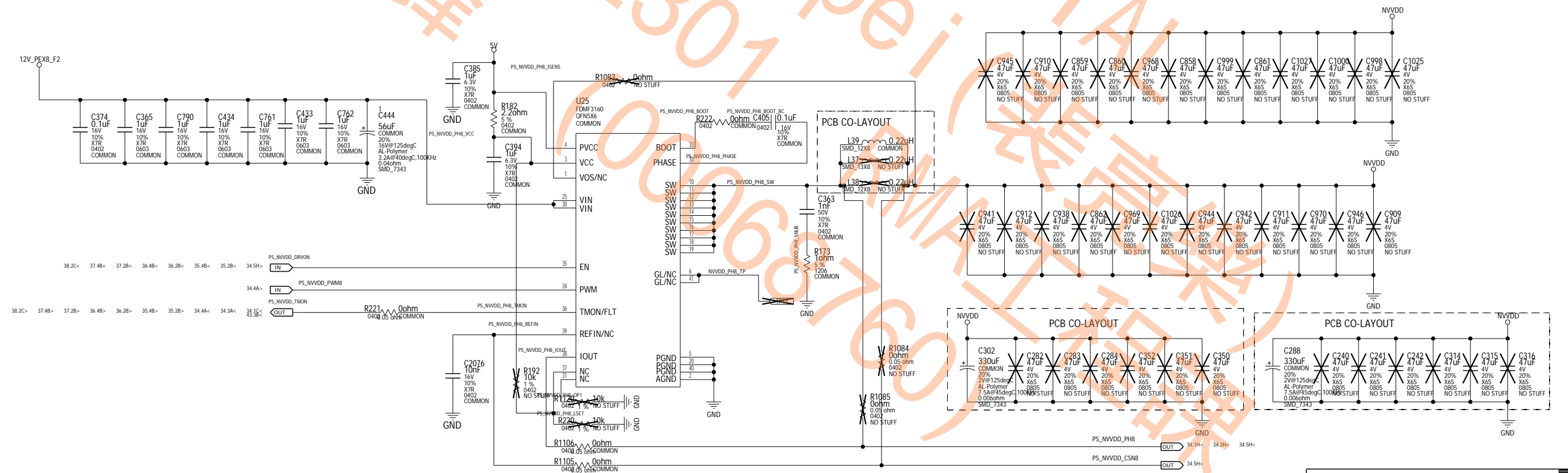
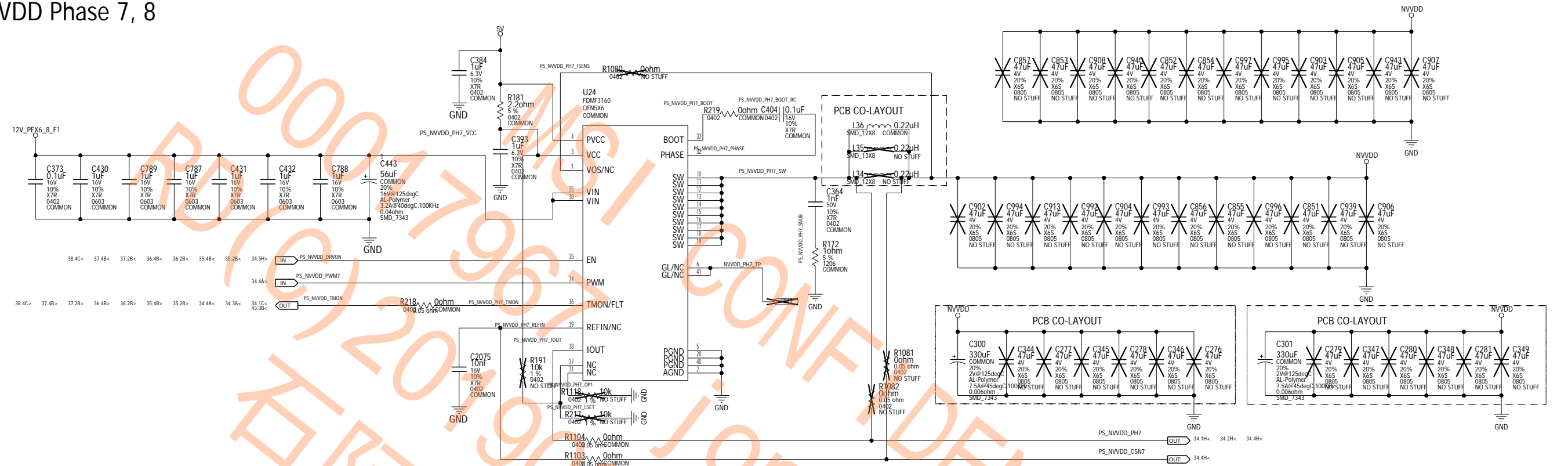
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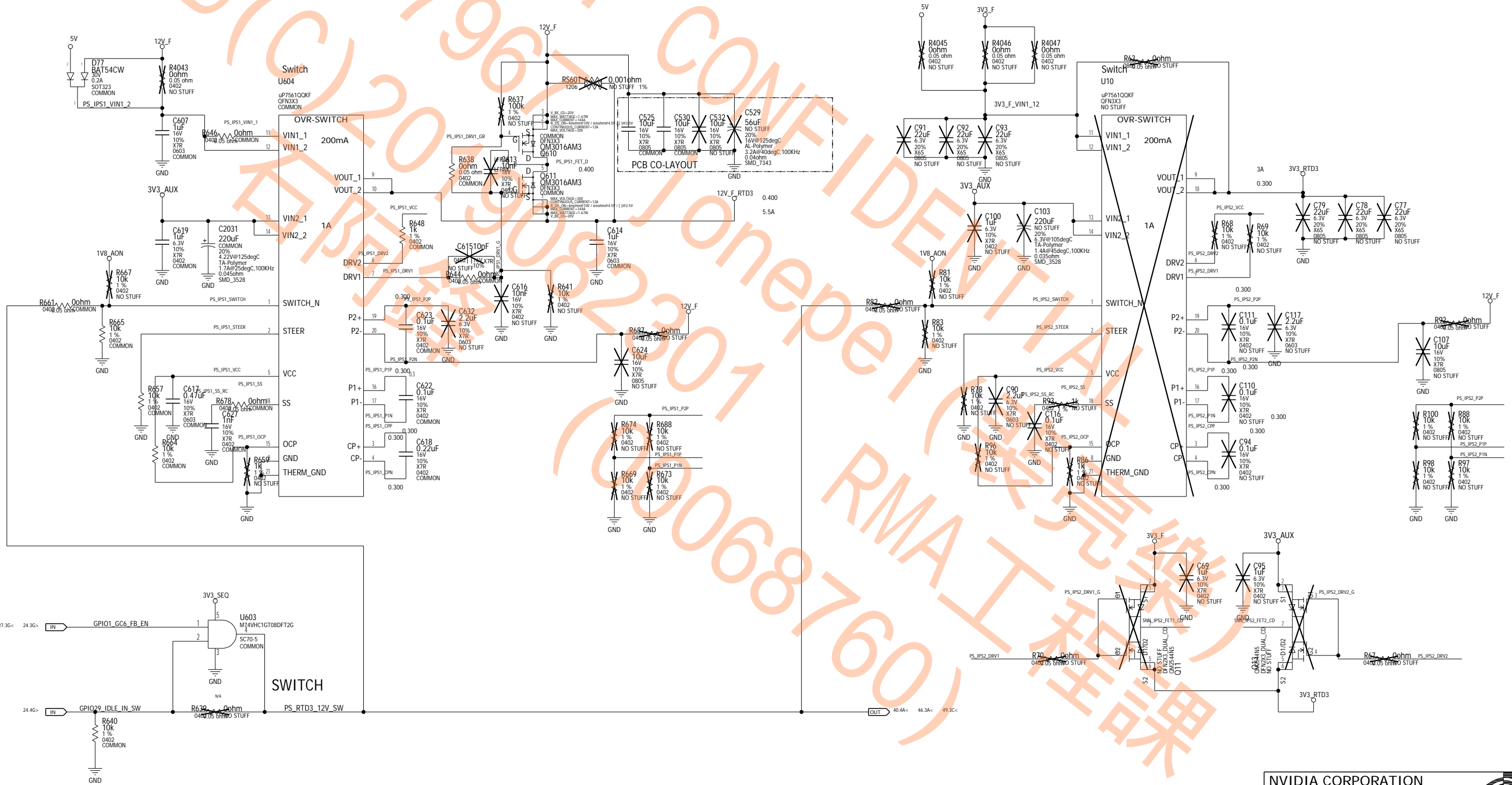
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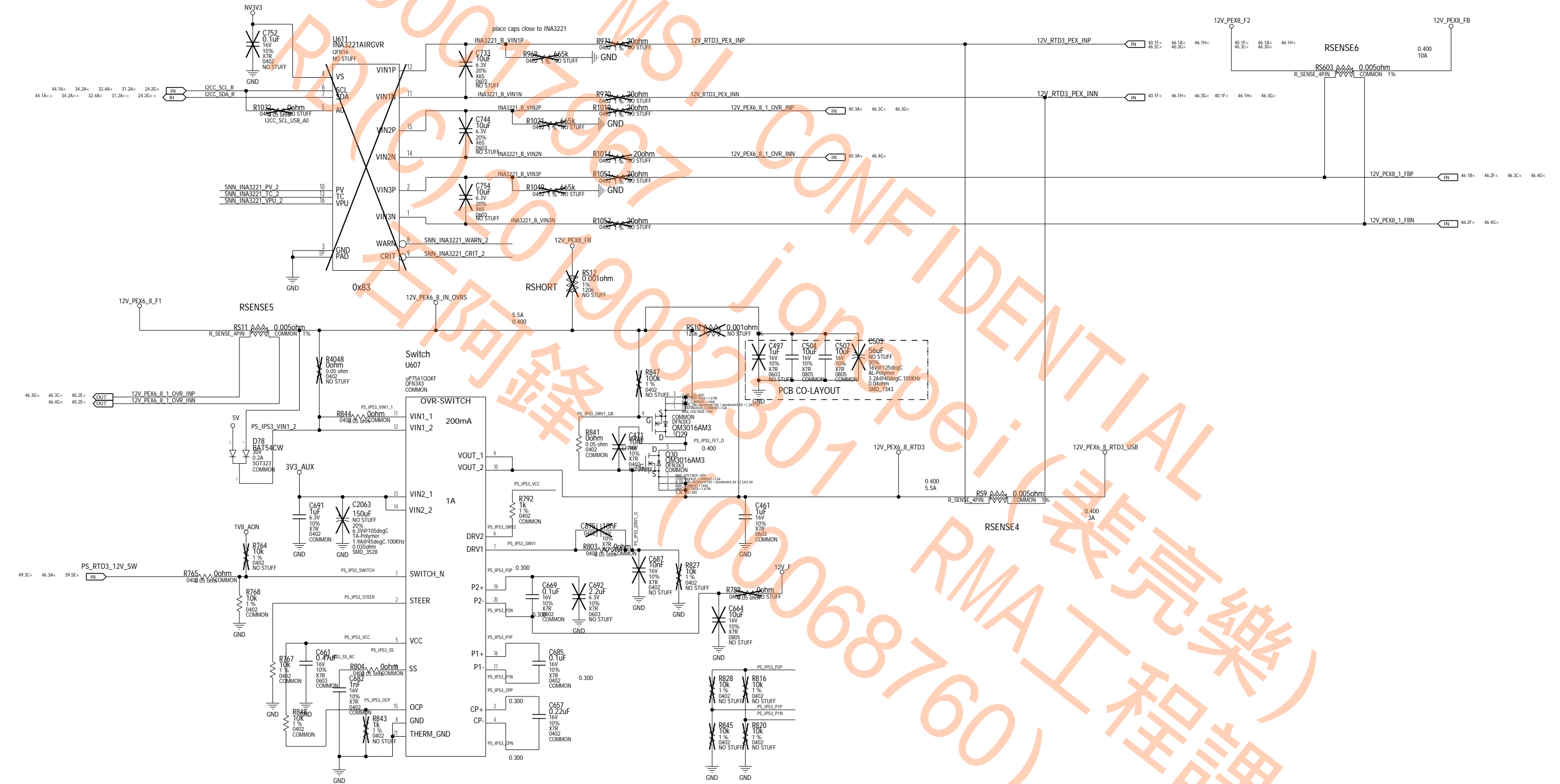
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AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

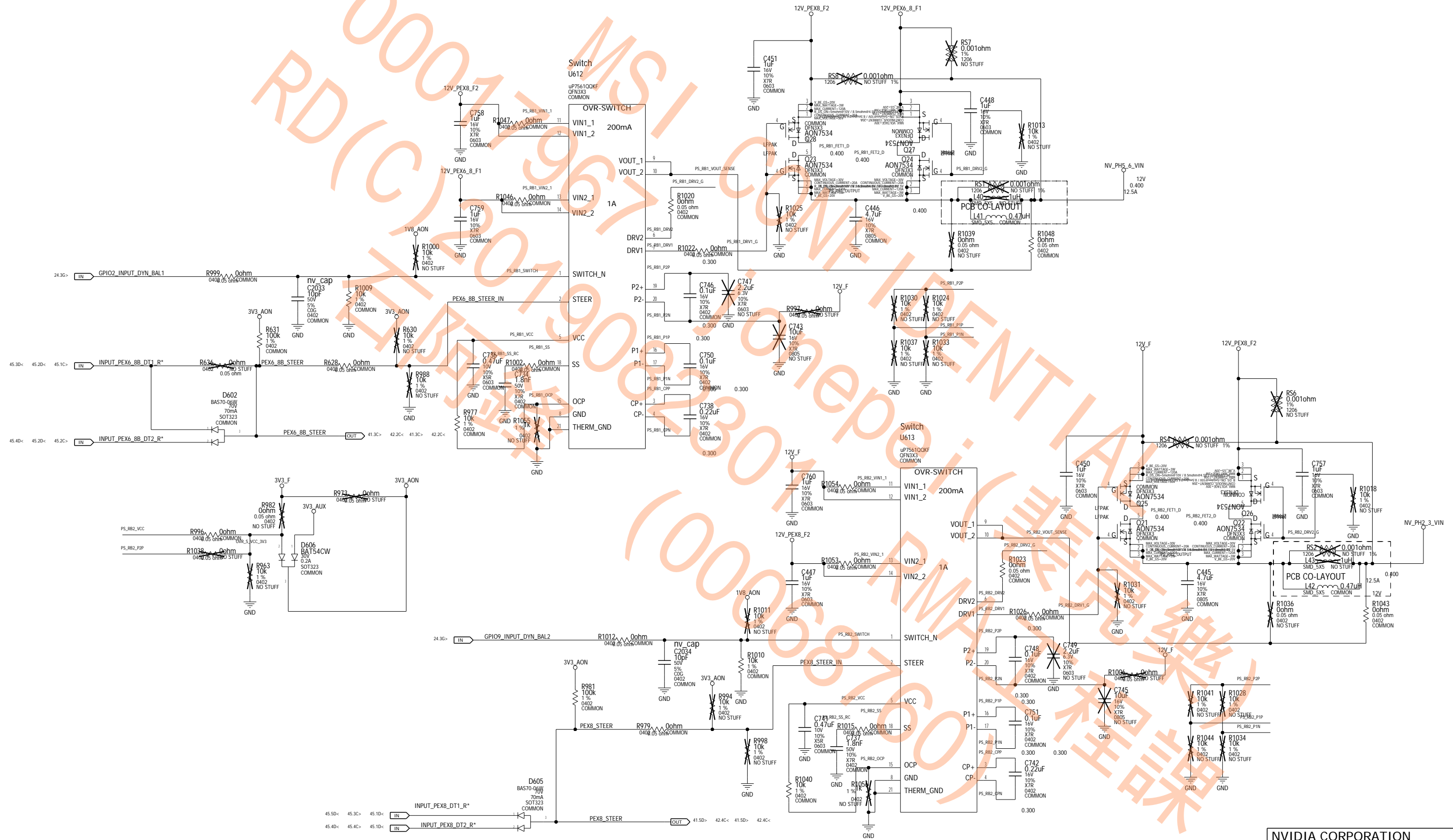


PAGE 40: PS: INPUT SWITCH RTD3 USB

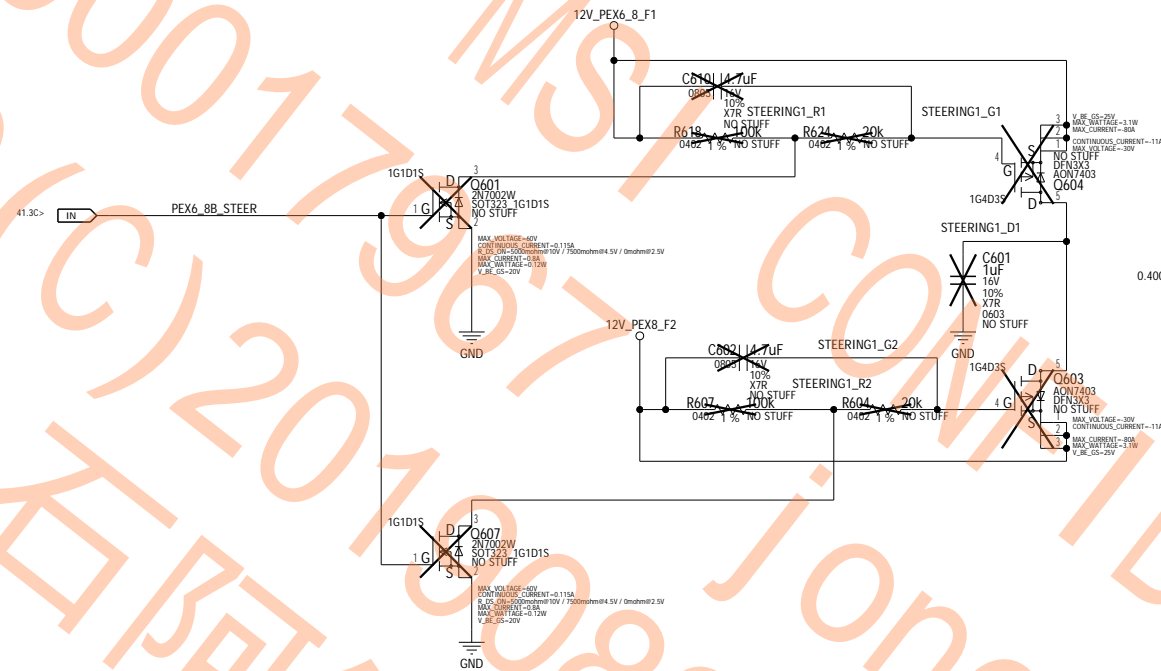


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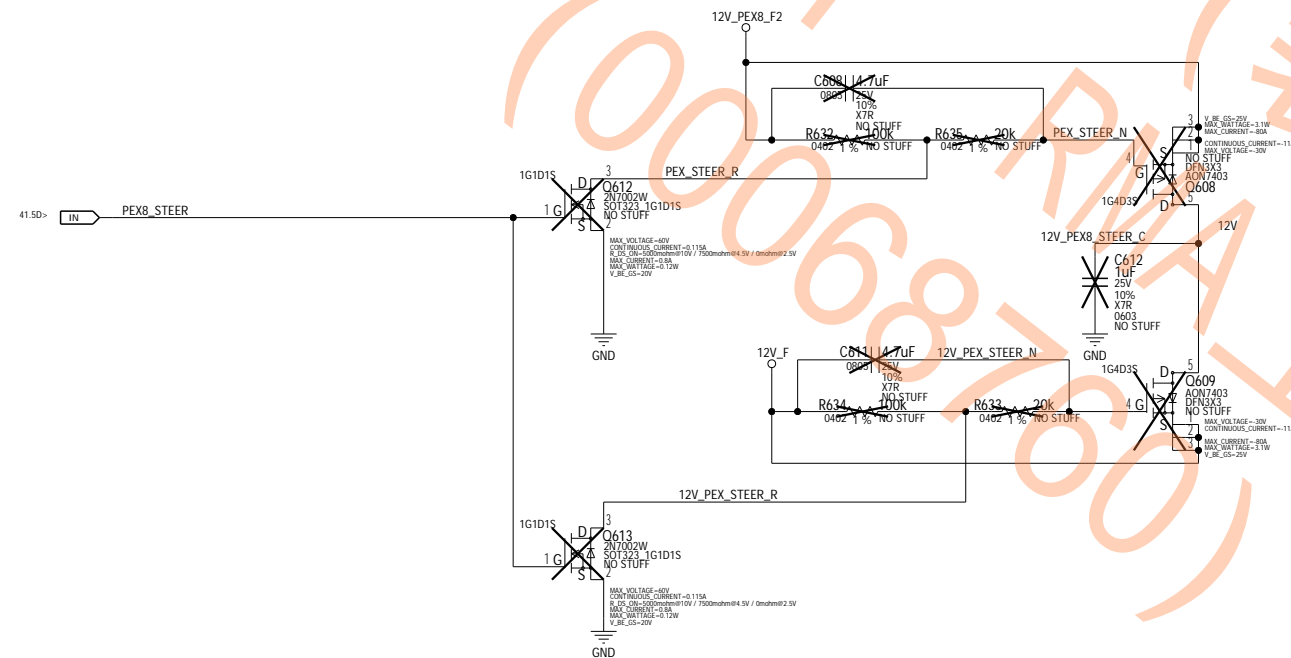
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12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

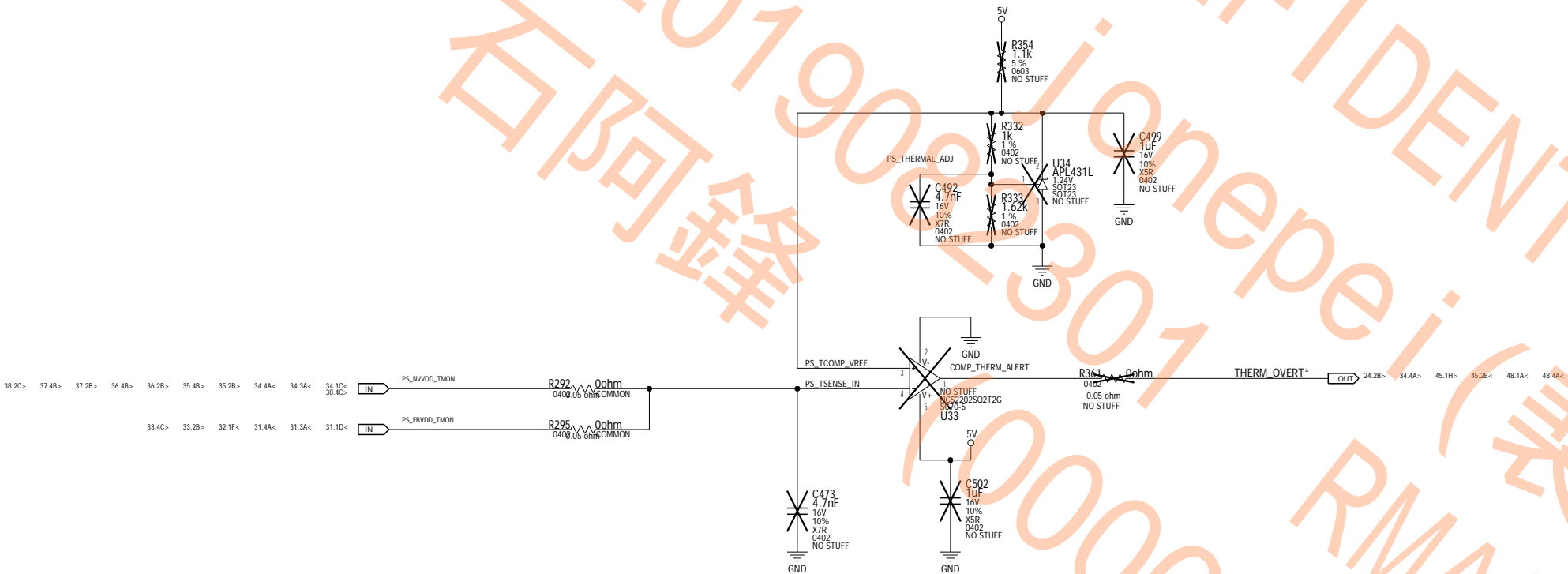


12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

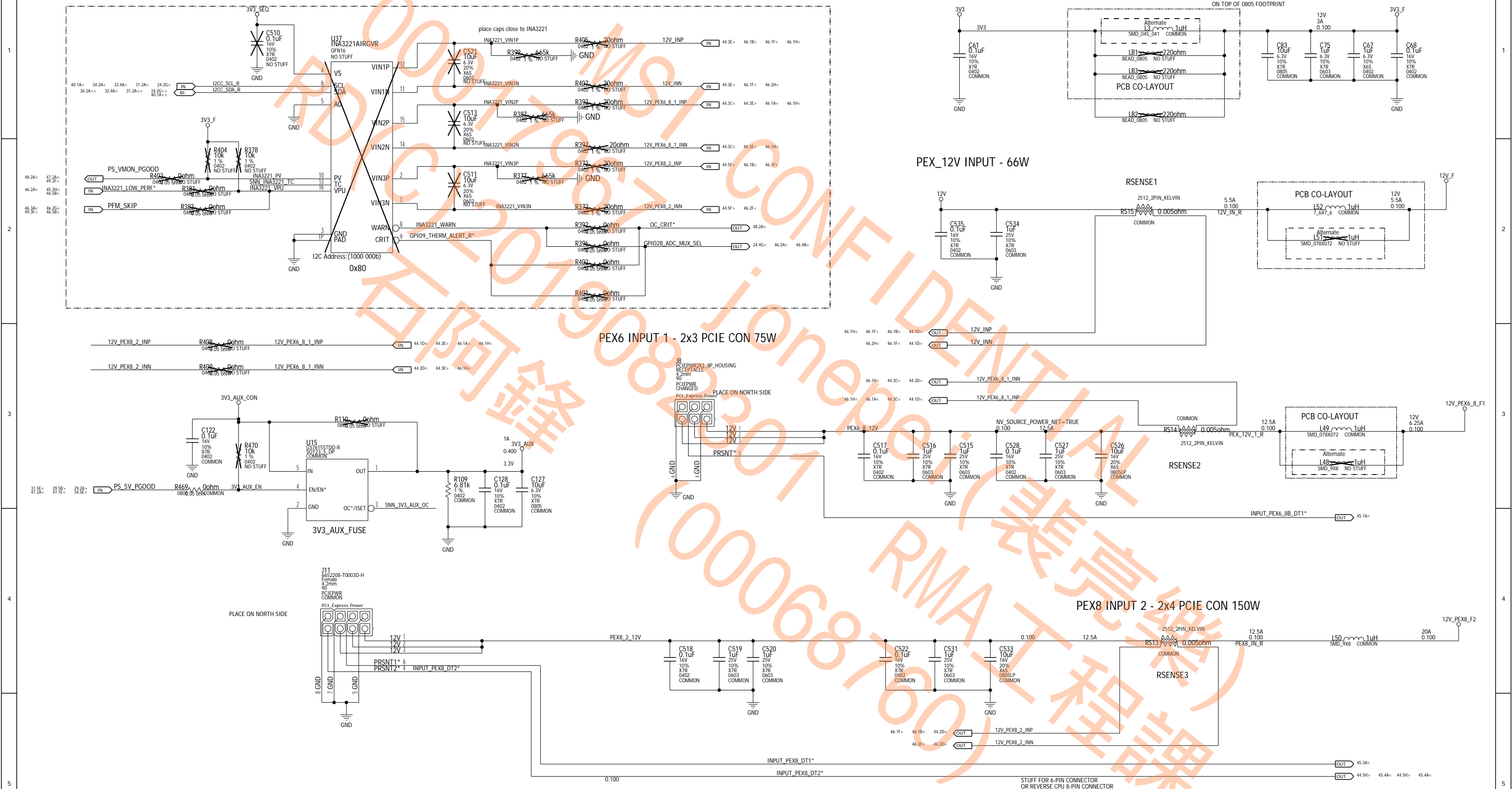



ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PS: 12V CURRENT STEERING

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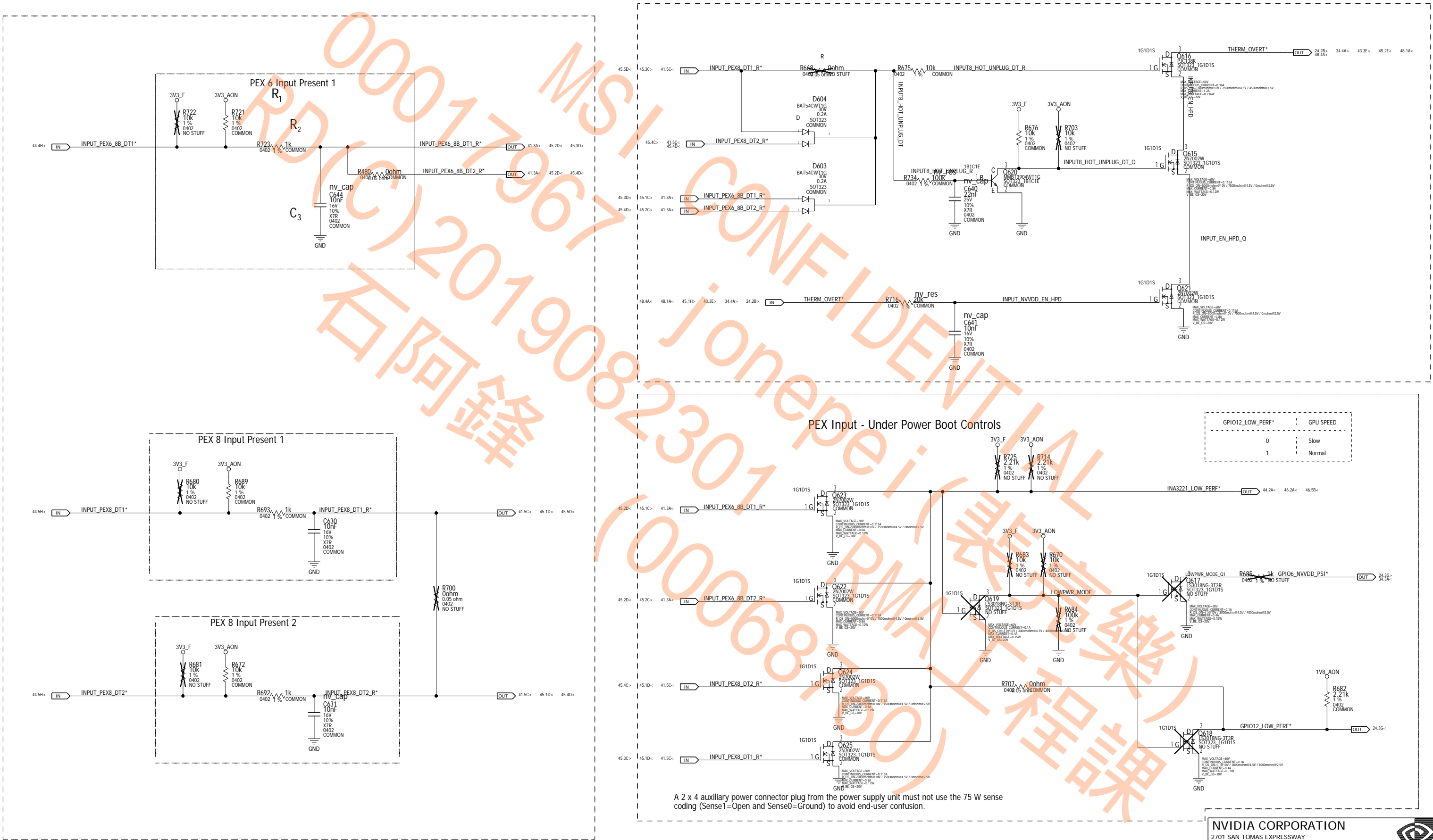
PAGE 44: PS: Inputs, Filtering, and Monitoring



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PAGE 45: PS: Current Steering, Hot Unplug Detect



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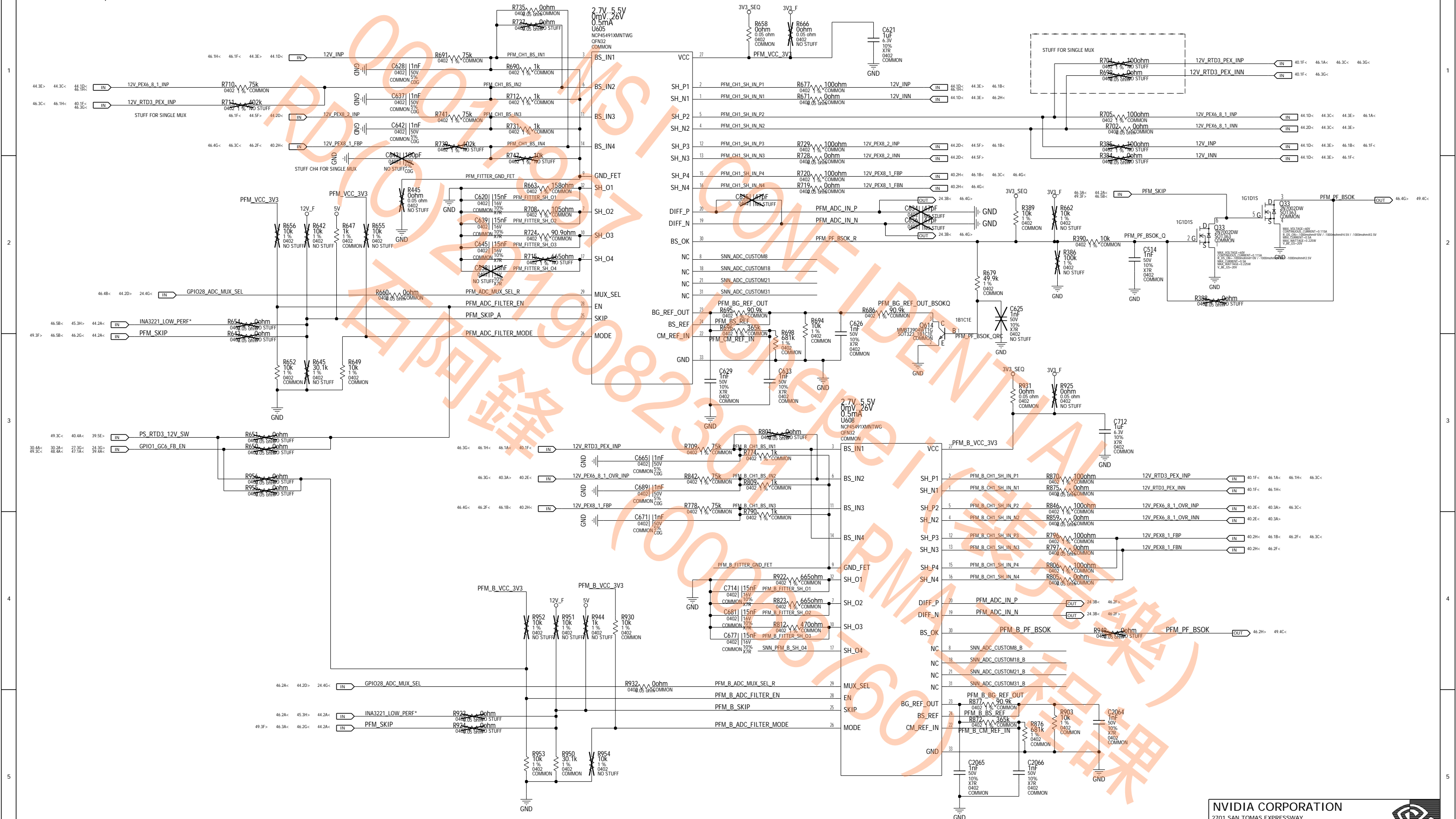
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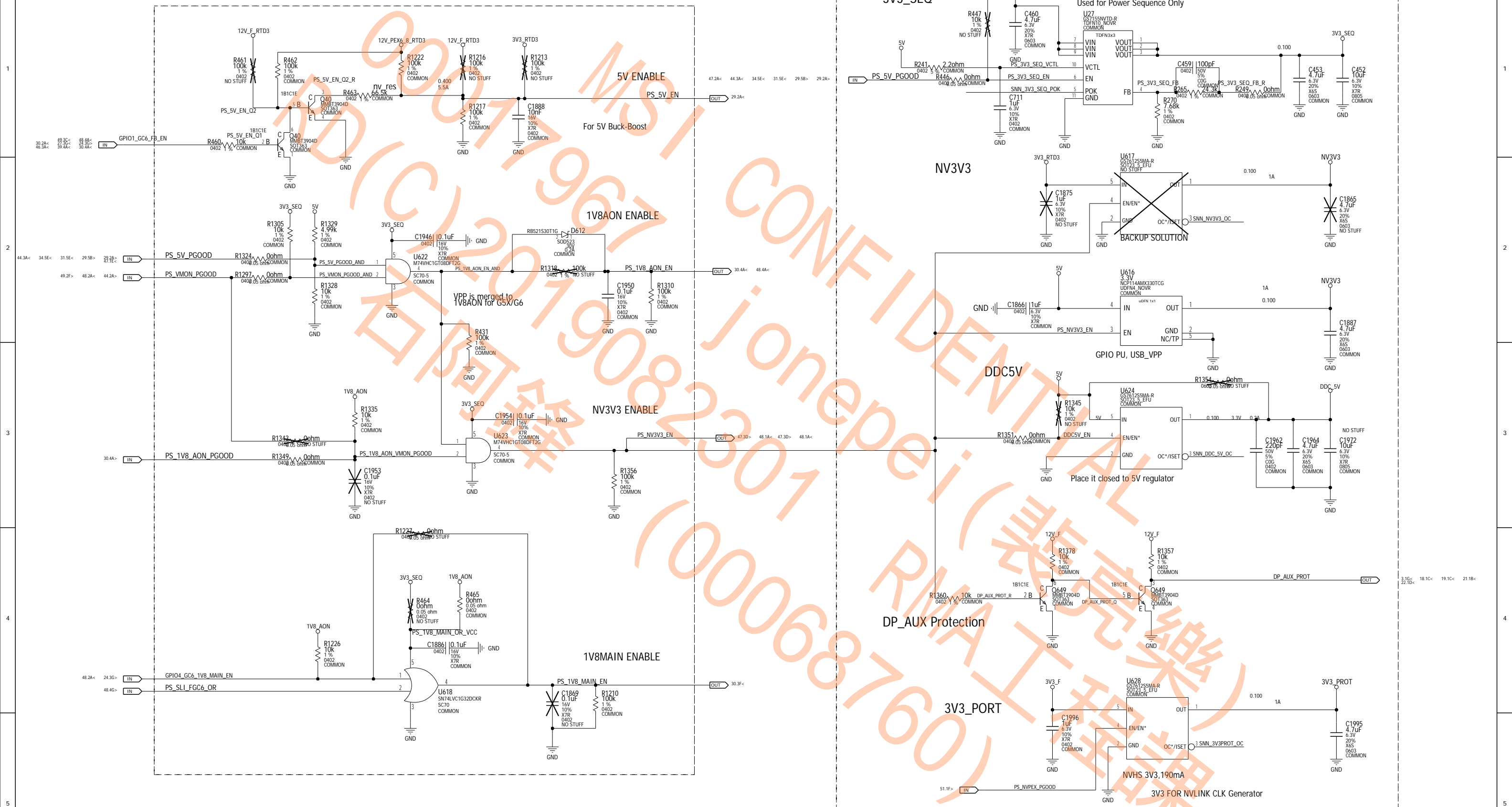
PAGE46; PS: Pre-Filter

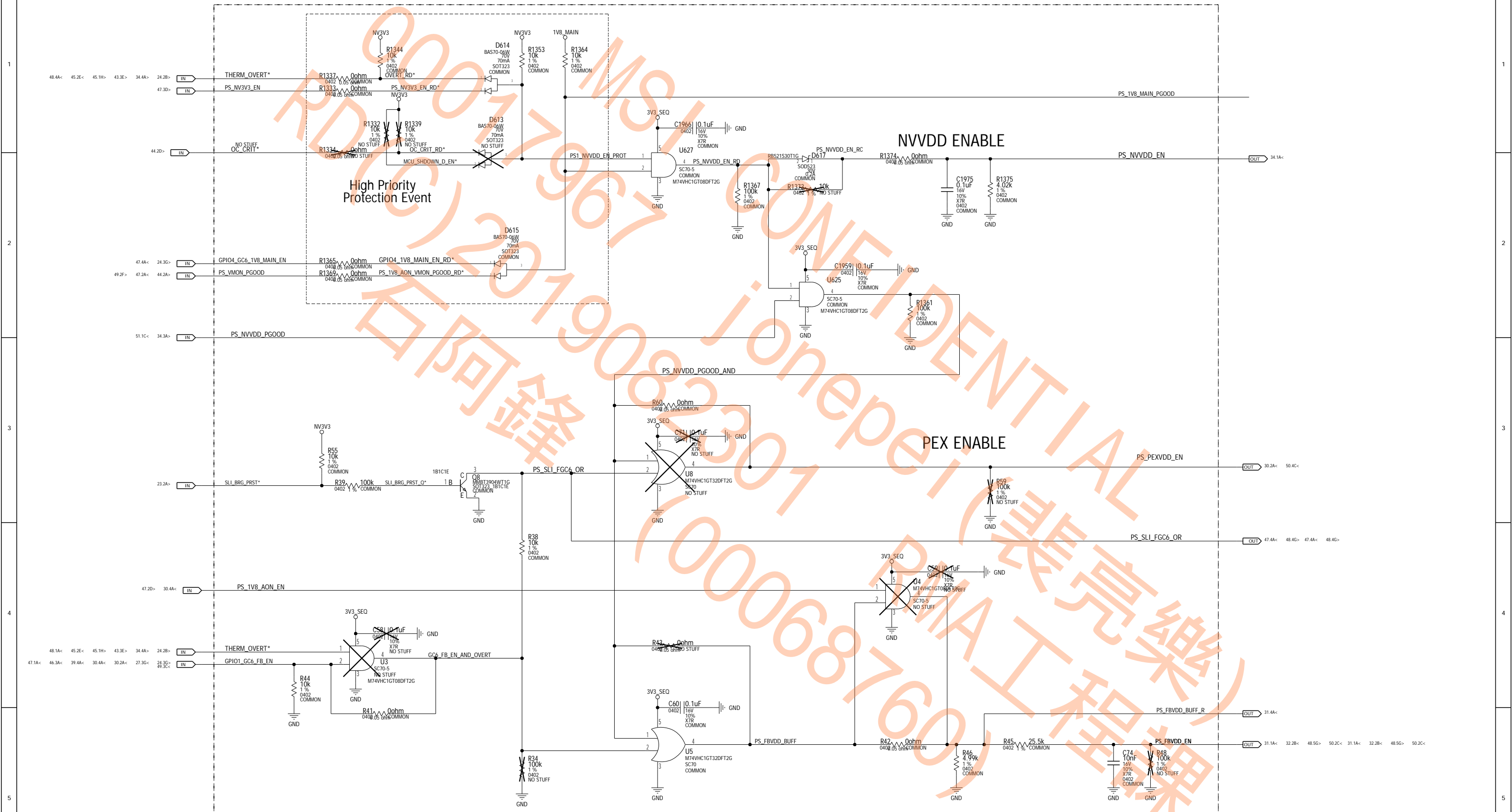


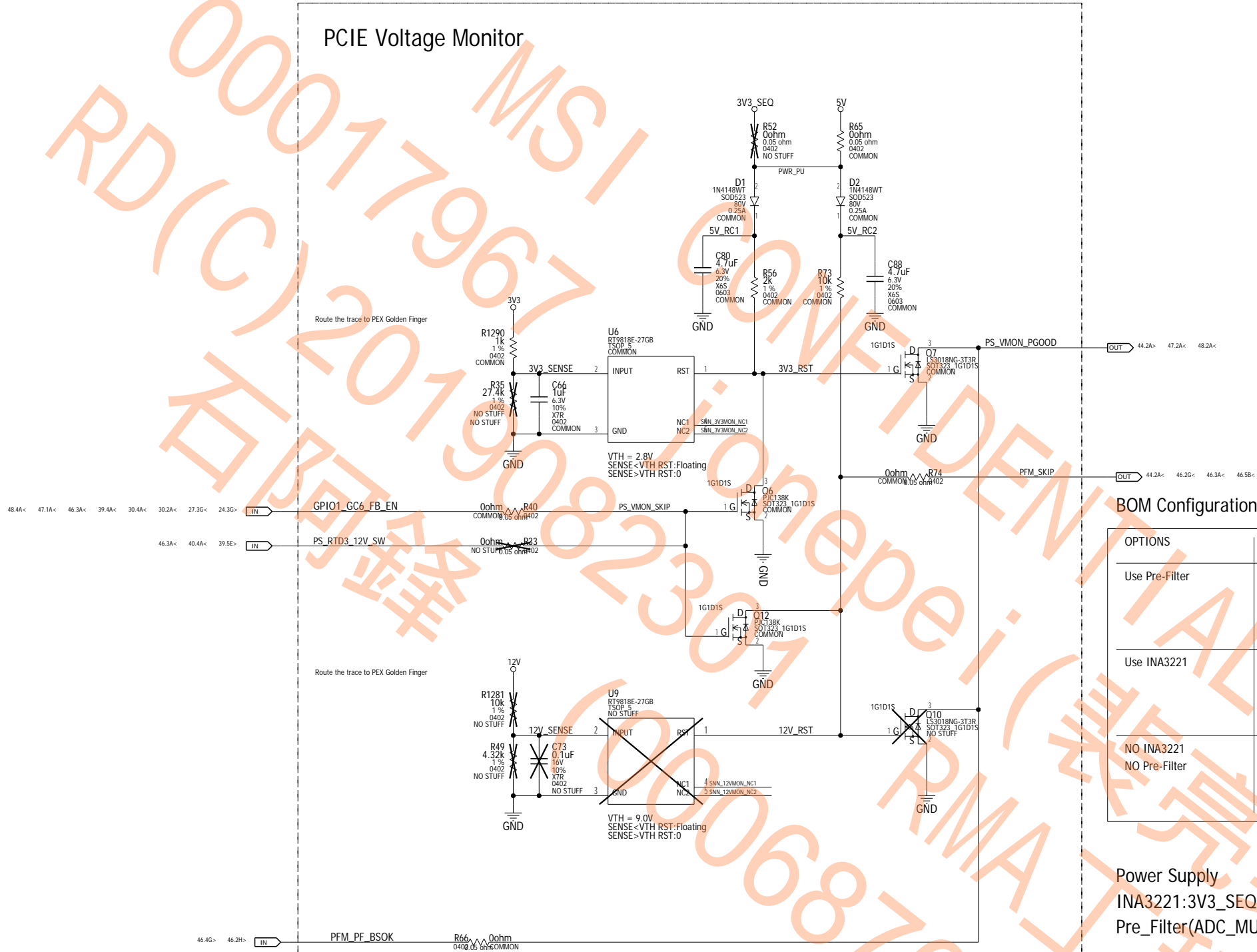
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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PS: PRE-FILTER

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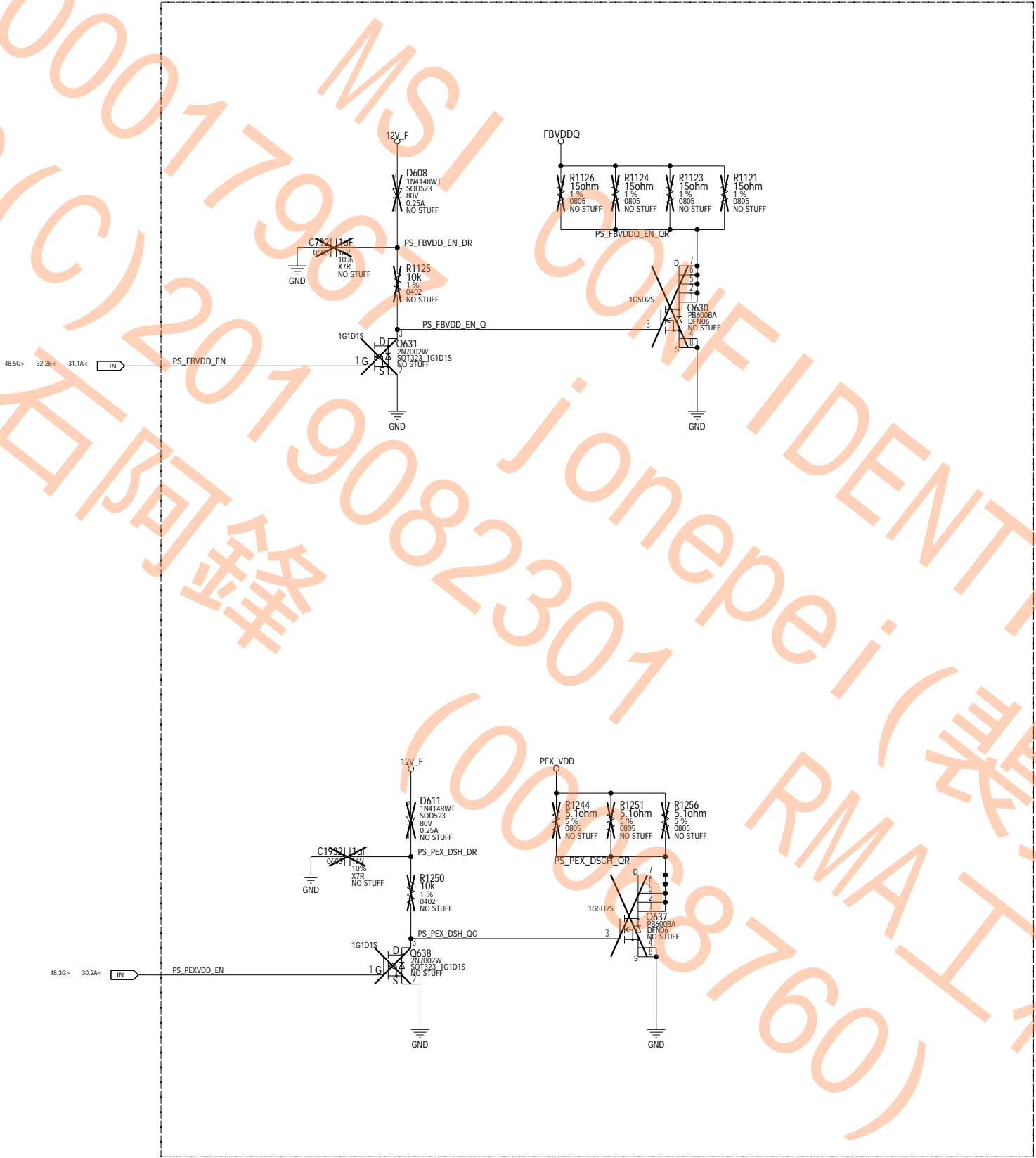
BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply
INA3221:3V3_SEQ
Pre_Filter(ADC_MUX):3V3(PEX)

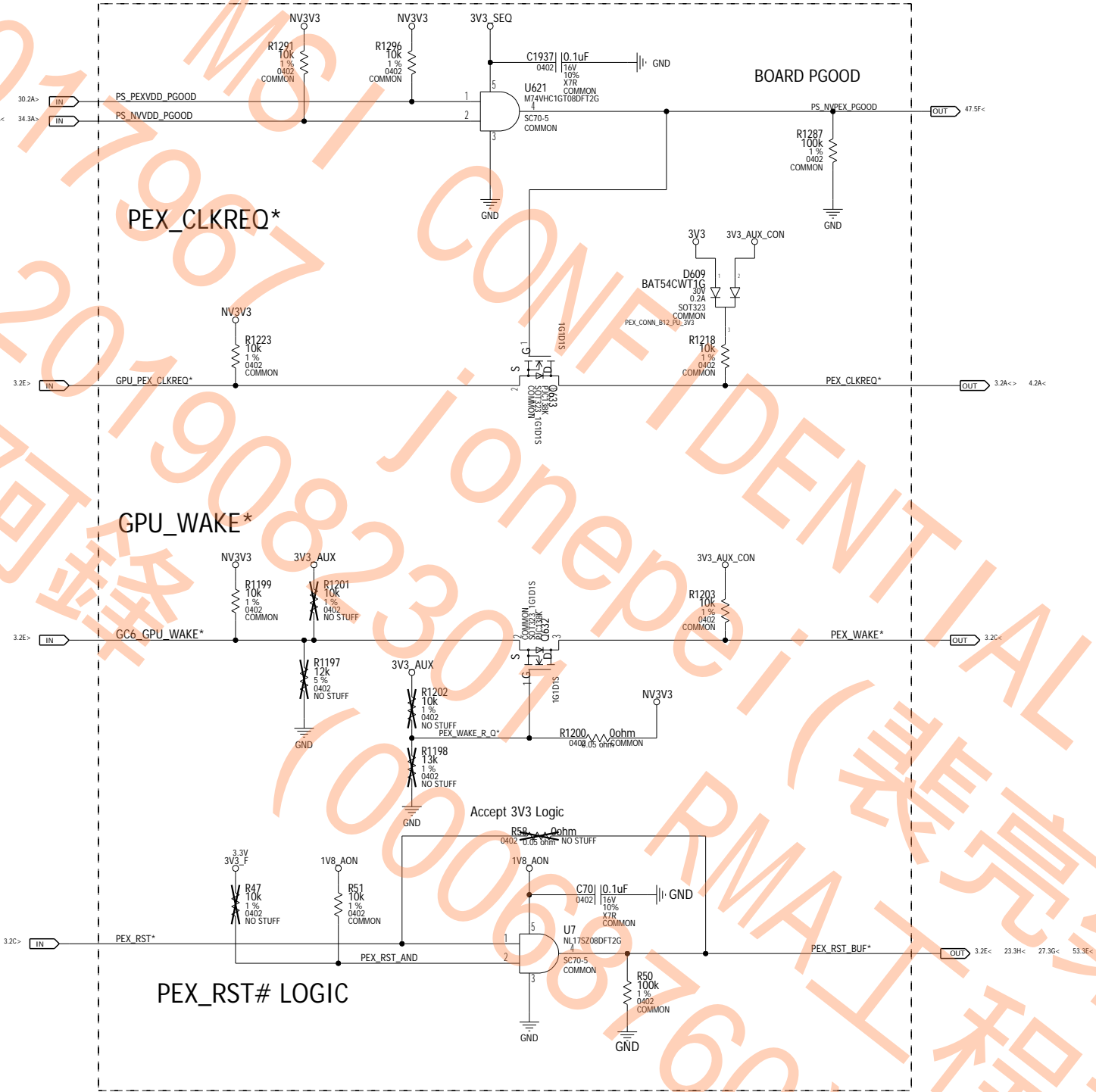
Dual Pre-Filter case:
Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOX	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RT3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW



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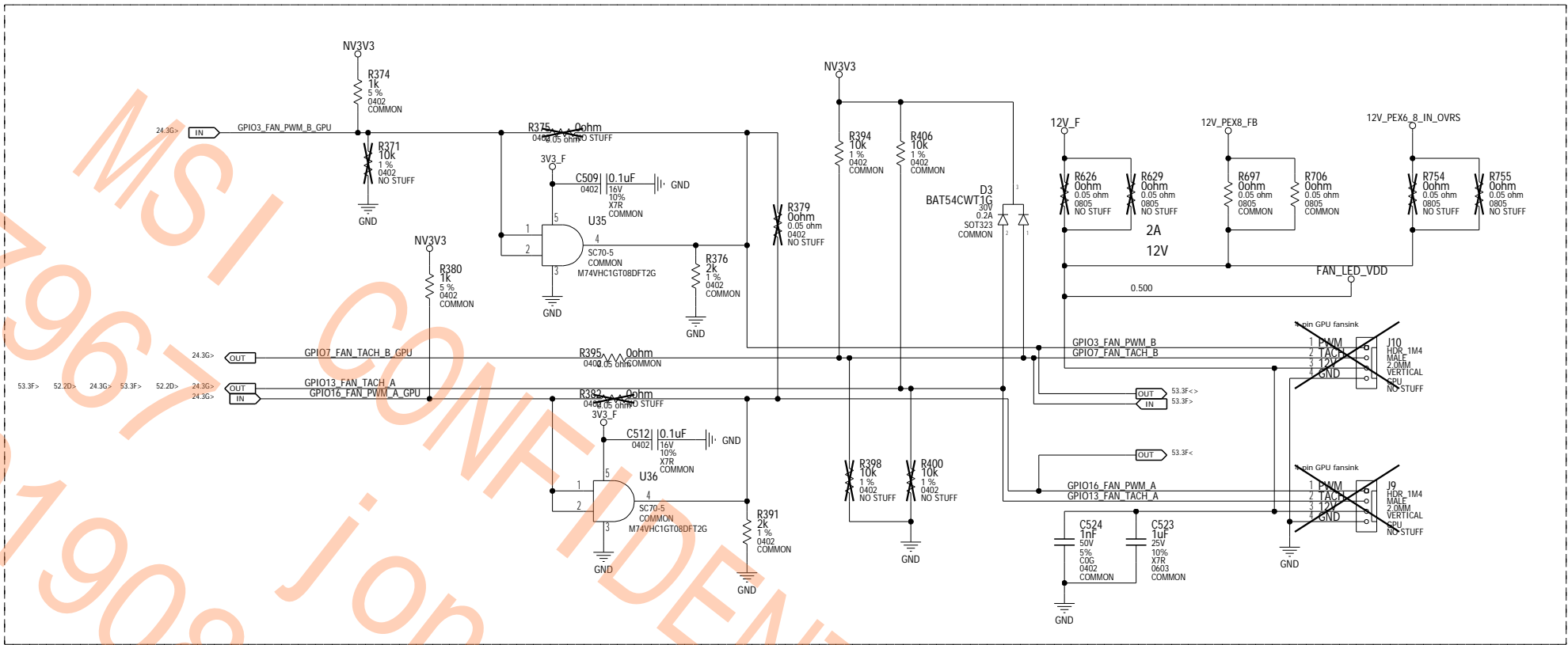
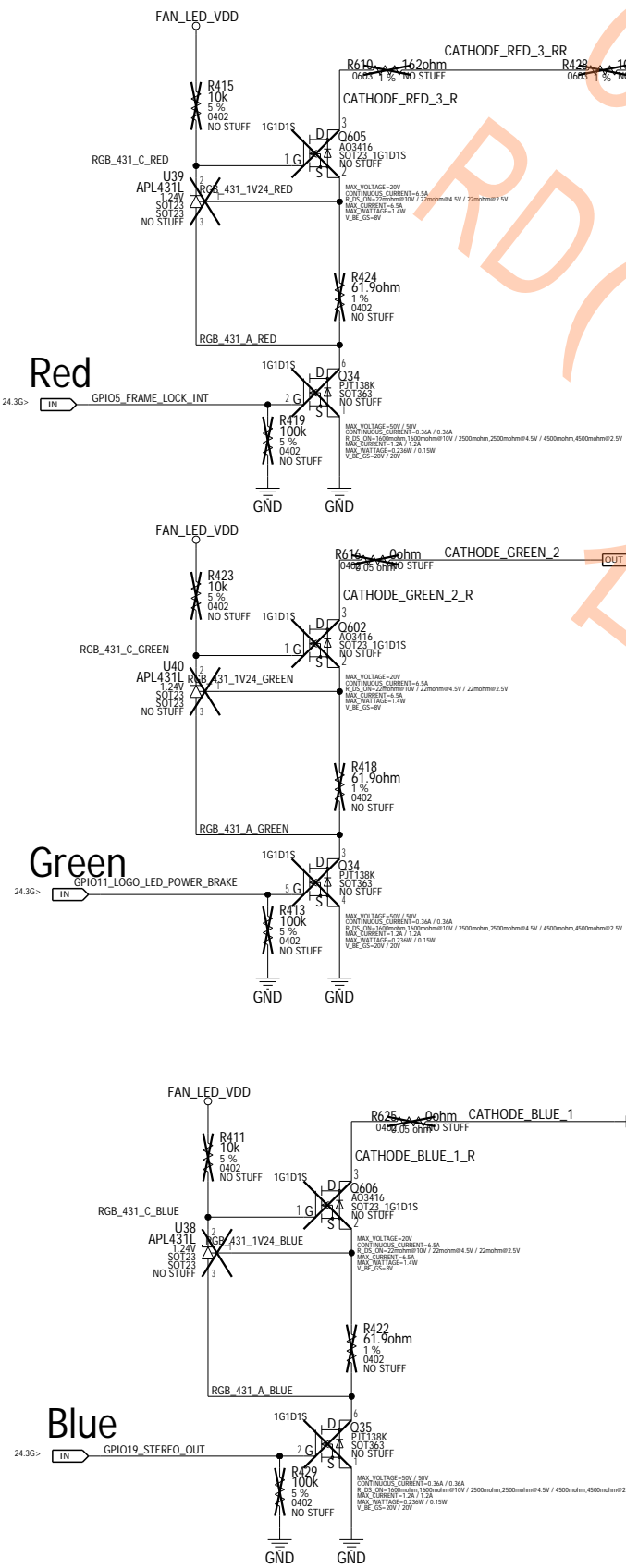
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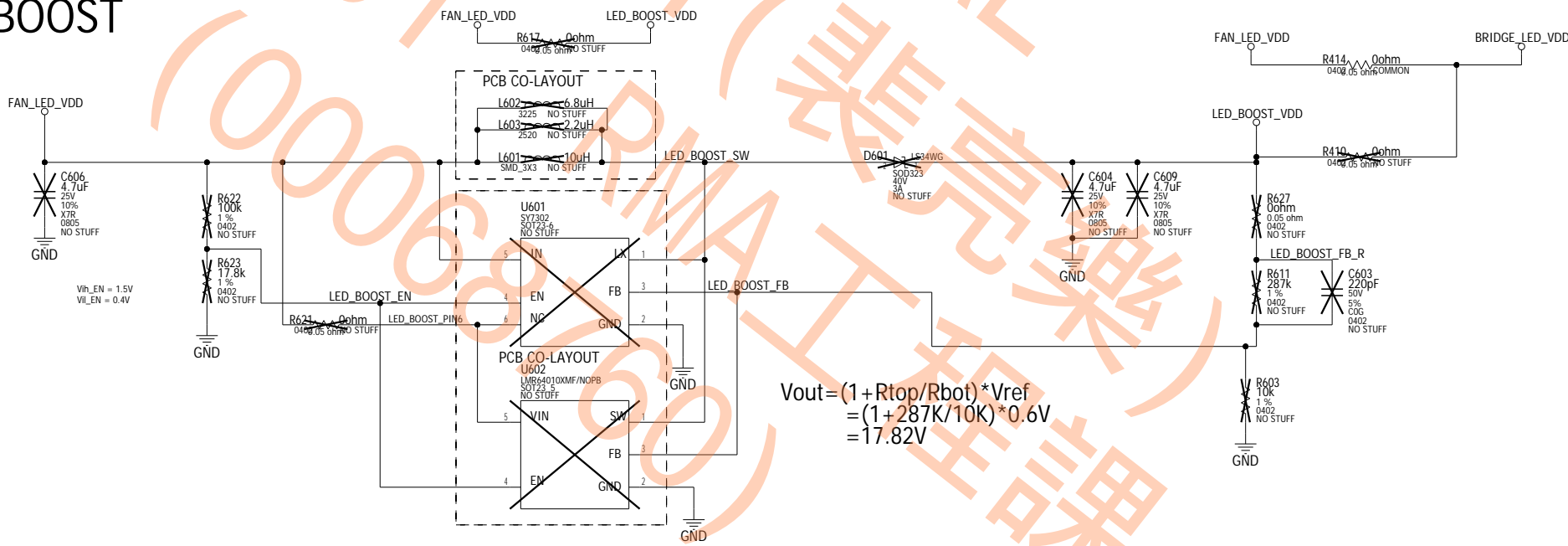
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PAGE 52: LED & FAN HEADERS



LED BOOST



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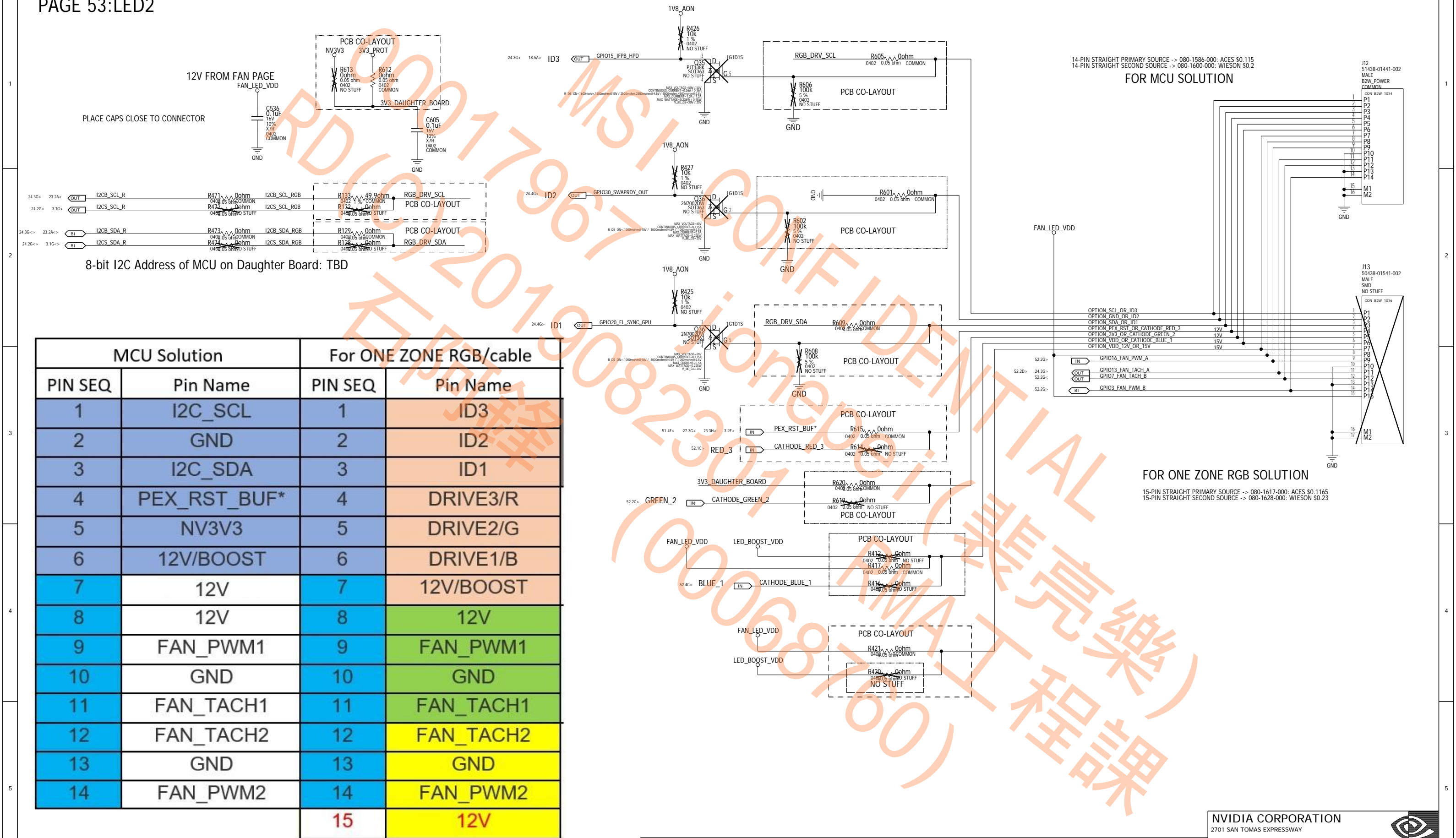
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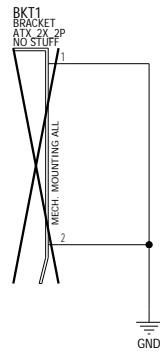
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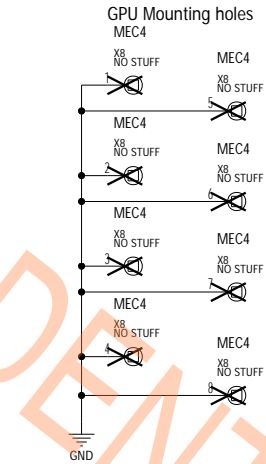
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Brackets:

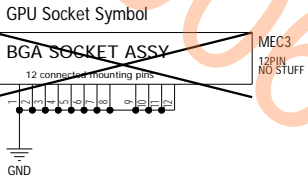
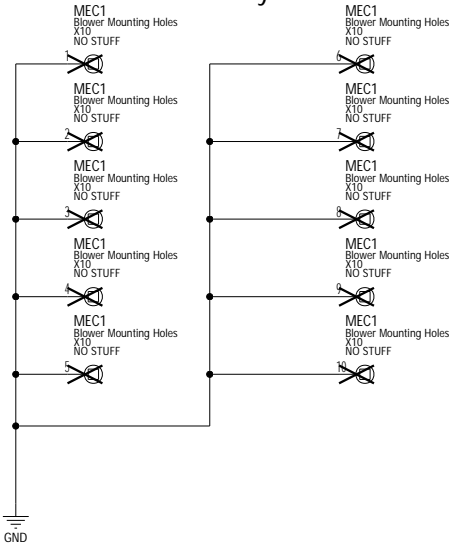


Bracket Screw



STIFFENER

Mechanical Holes Symbol



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