

PG210 B00

GP107 128b GDDR5, 75W , PCB 5.7"
DVI-D_DL (DP + DP) + HDMI (DP) + DP

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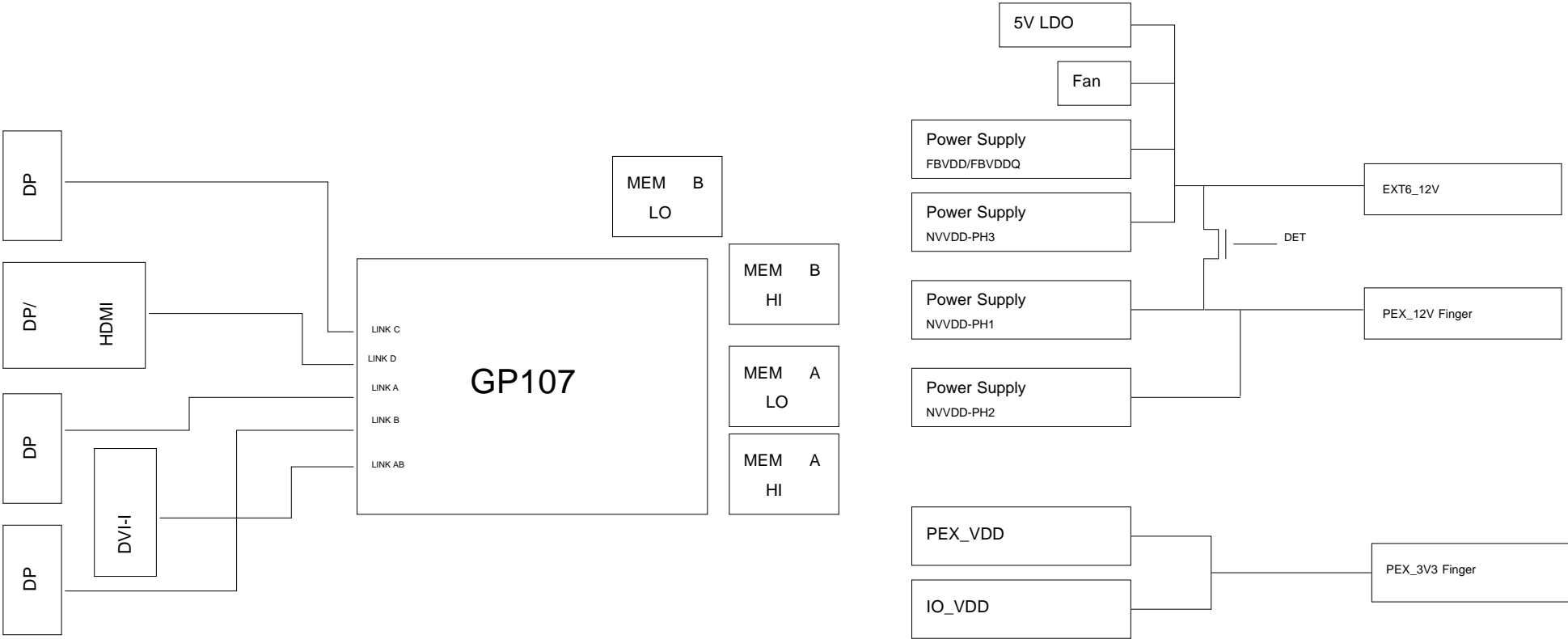
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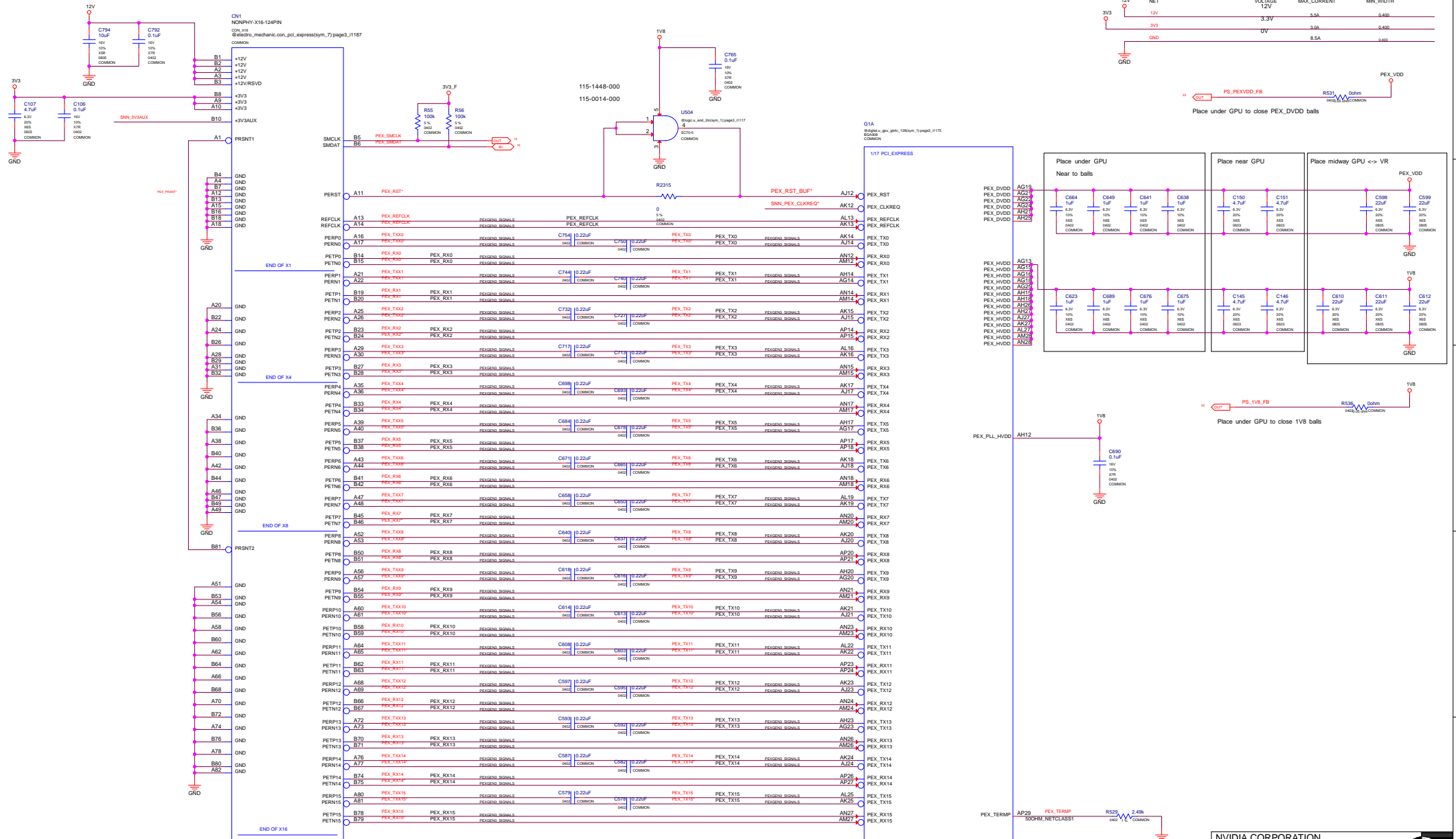
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Block Diagram




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PCI Express



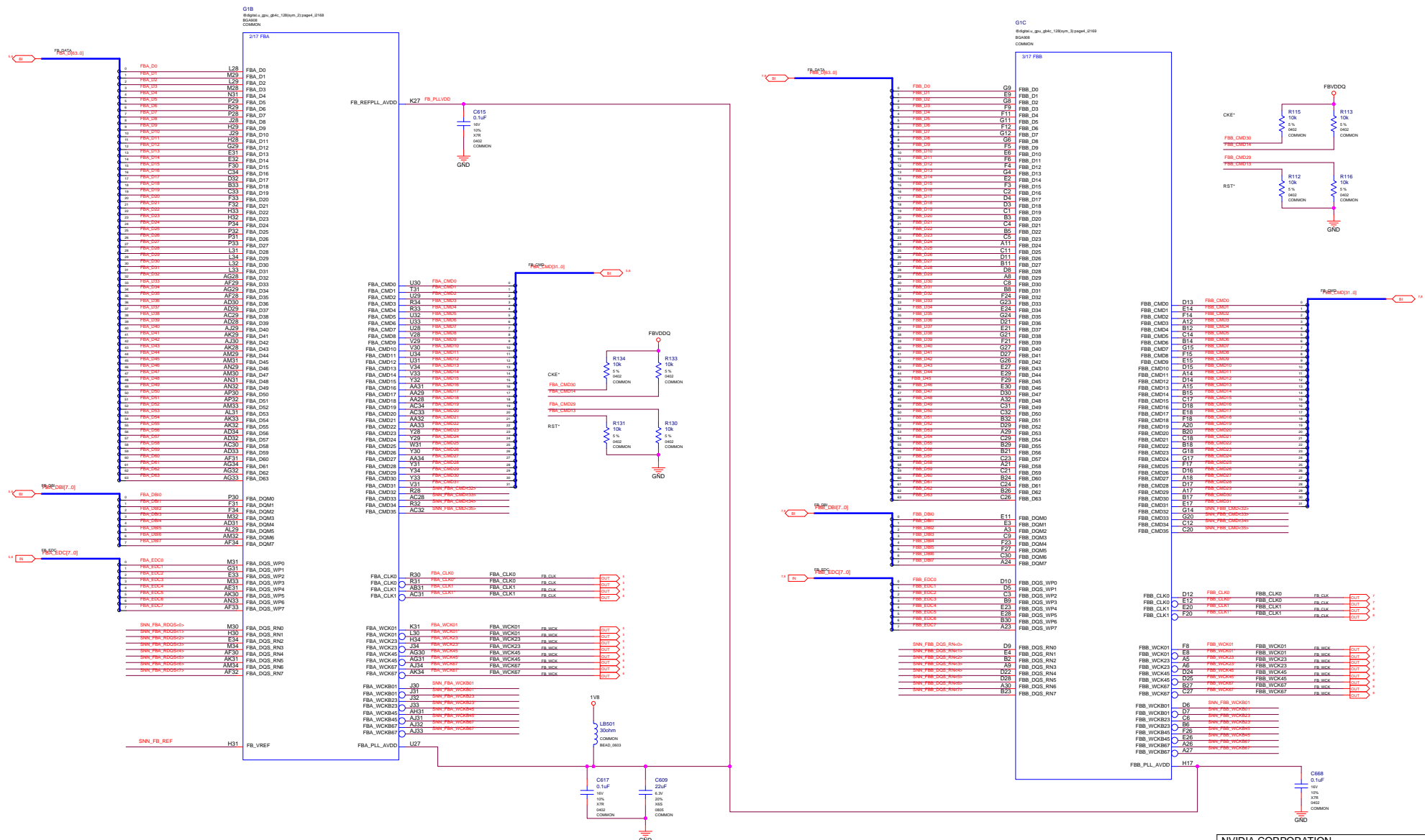
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MEMORY: GPU Partition A/B



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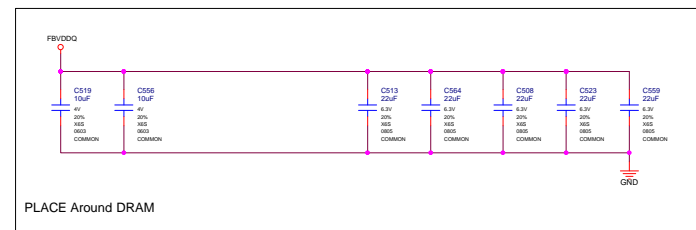
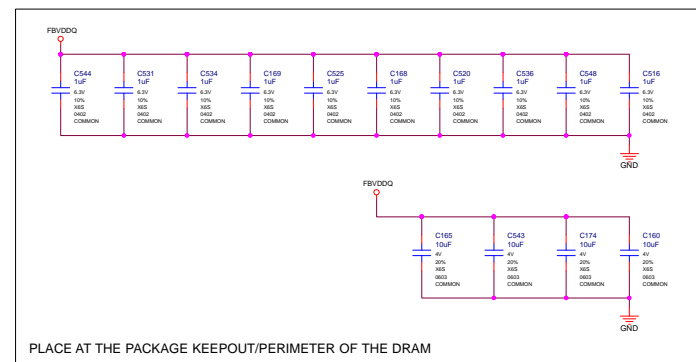
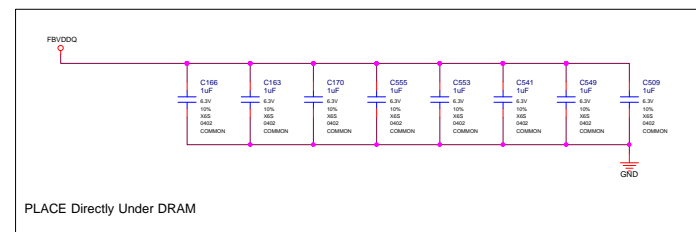
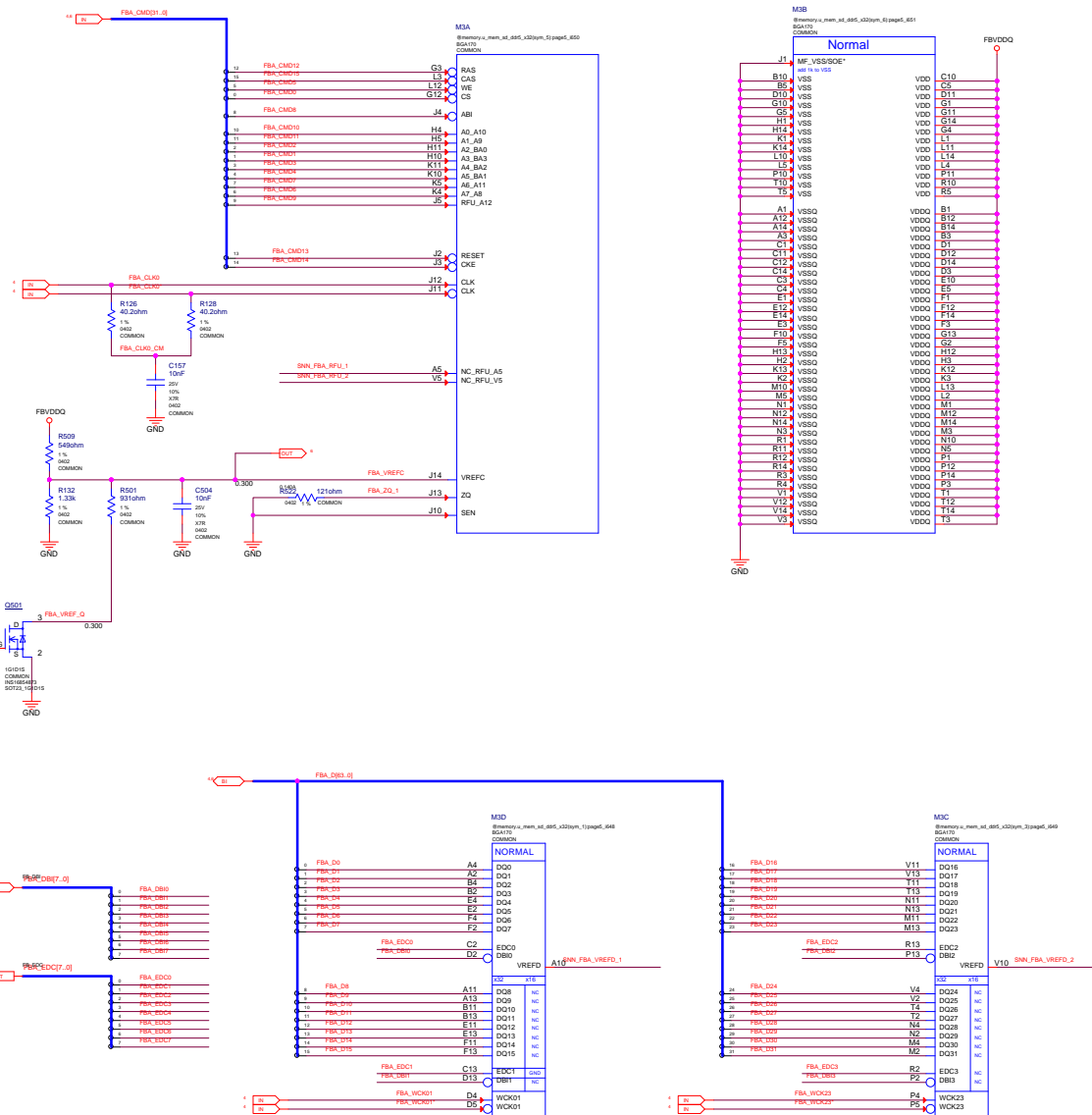
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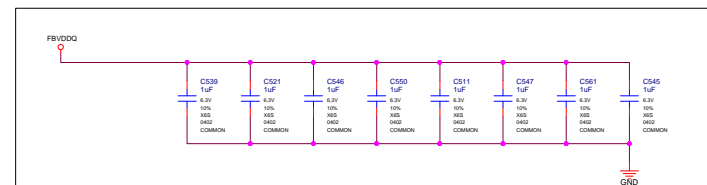
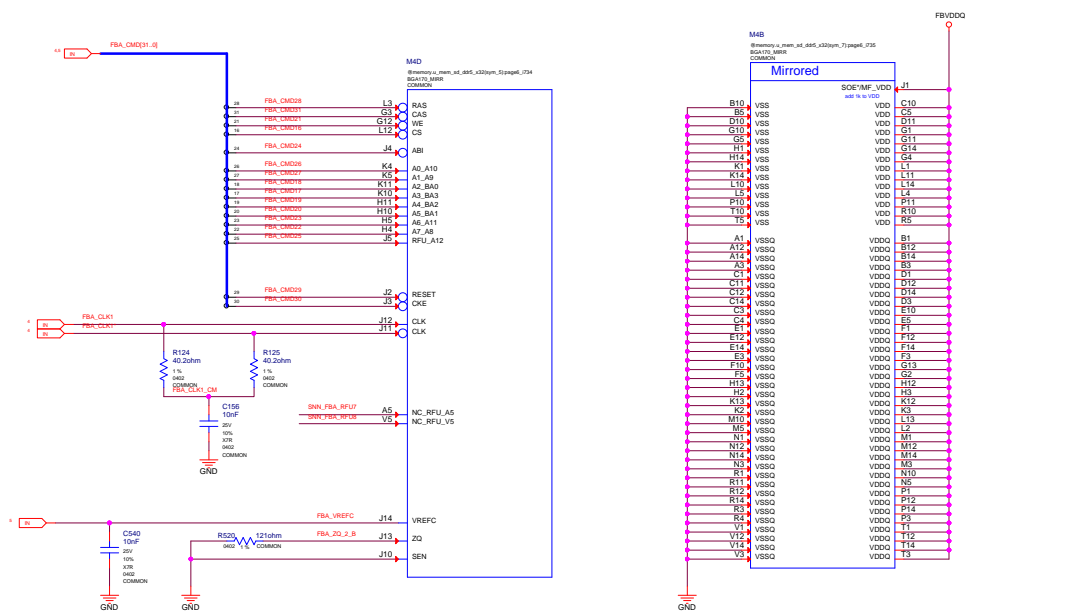
MEMORY: FBA Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3..BA3	
CMD2	A2..BA2	
CMD3	A4..BA2	
CMD4	A5..BA1	
CMD5	WE*	
CMD6	A7..A8	
CMD7	AE..A11	
CMD8	AB*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A9	
CMD12	RA*	
CMD13	RE*	
CMD14	CK*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3..BA3
CMD18		A2..BA2
CMD19		A4..BA2
CMD20		A5..BA1
CMD21		WE*
CMD22		A7..A8
CMD23		AE..A11
CMD24		AB*
CMD25		A12..RFU
CMD26		A0..A10
CMD27		A1..A9
CMD28		RA*
CMD29		RE*
CMD30		CK*
CMD31		CAS*

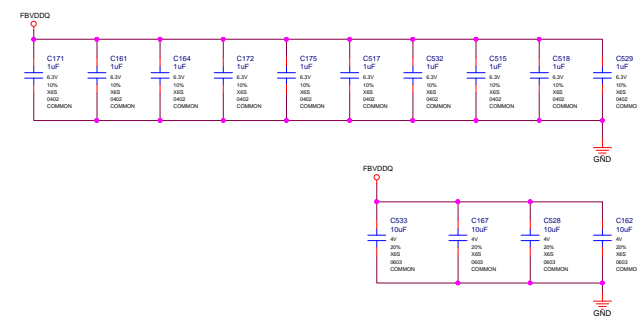


MEMORY: FBA Partition 63..32

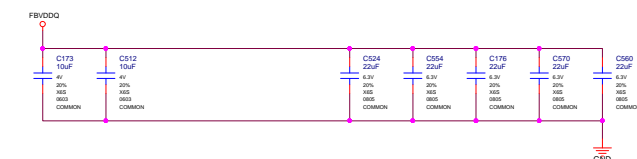
CMD	0..31	32..63
CMD0	CS*	
CMD1	A3..BA3	
CMD2	A2..BA2	
CMD3	A4..BA2	
CMD4	A5..BA1	
CMD5	WE*	
CMD6		
CMD7	AE..A11	
CMD8	AB*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A0	
CMD12	RAS*	
CMD13	RS1*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		
CMD17		CS*
CMD18	A3..BA3	
CMD19	A2..BA2	
CMD20	A5..BA1	
CMD21	WE*	
CMD22	A7..A8	
CMD23	AE..A11	
CMD24	AB*	
CMD25	A12..RFU	
CMD26	A0..A10	
CMD27	A1..A0	
CMD28	RAS*	
CMD29	RS1*	
CMD30	CKE*	
CMD31	CAS*	



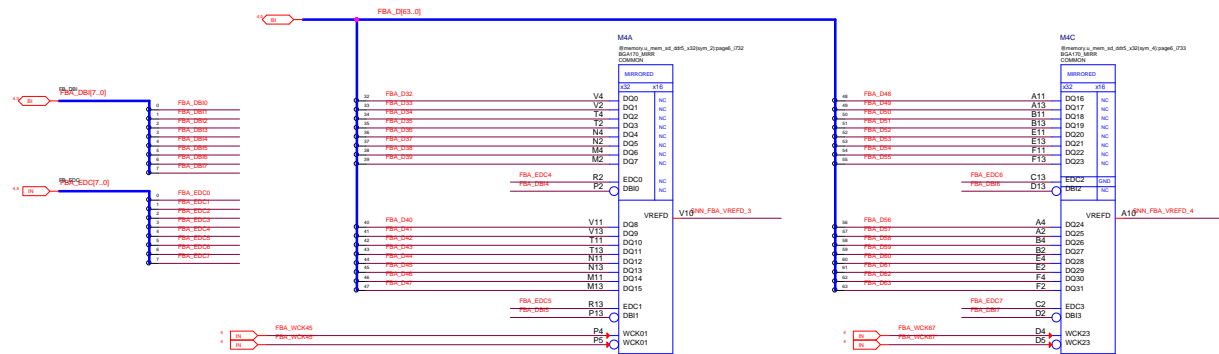
PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM

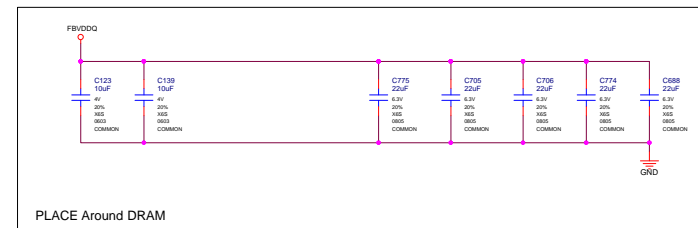
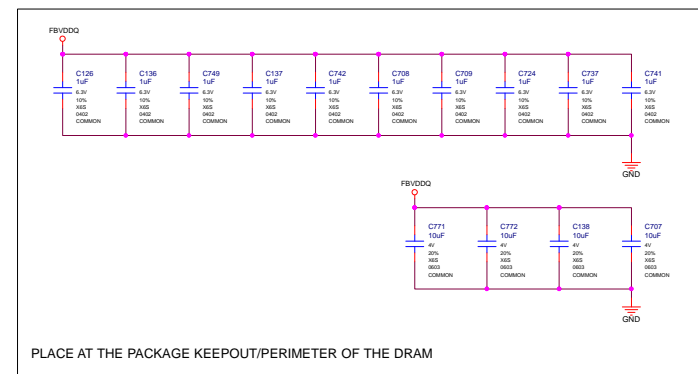
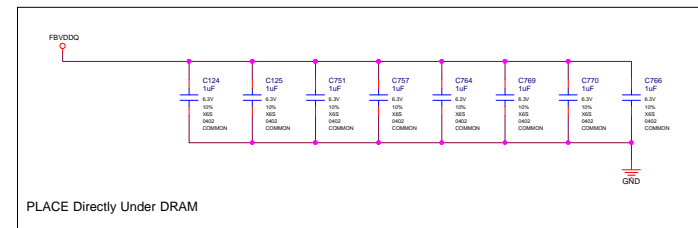
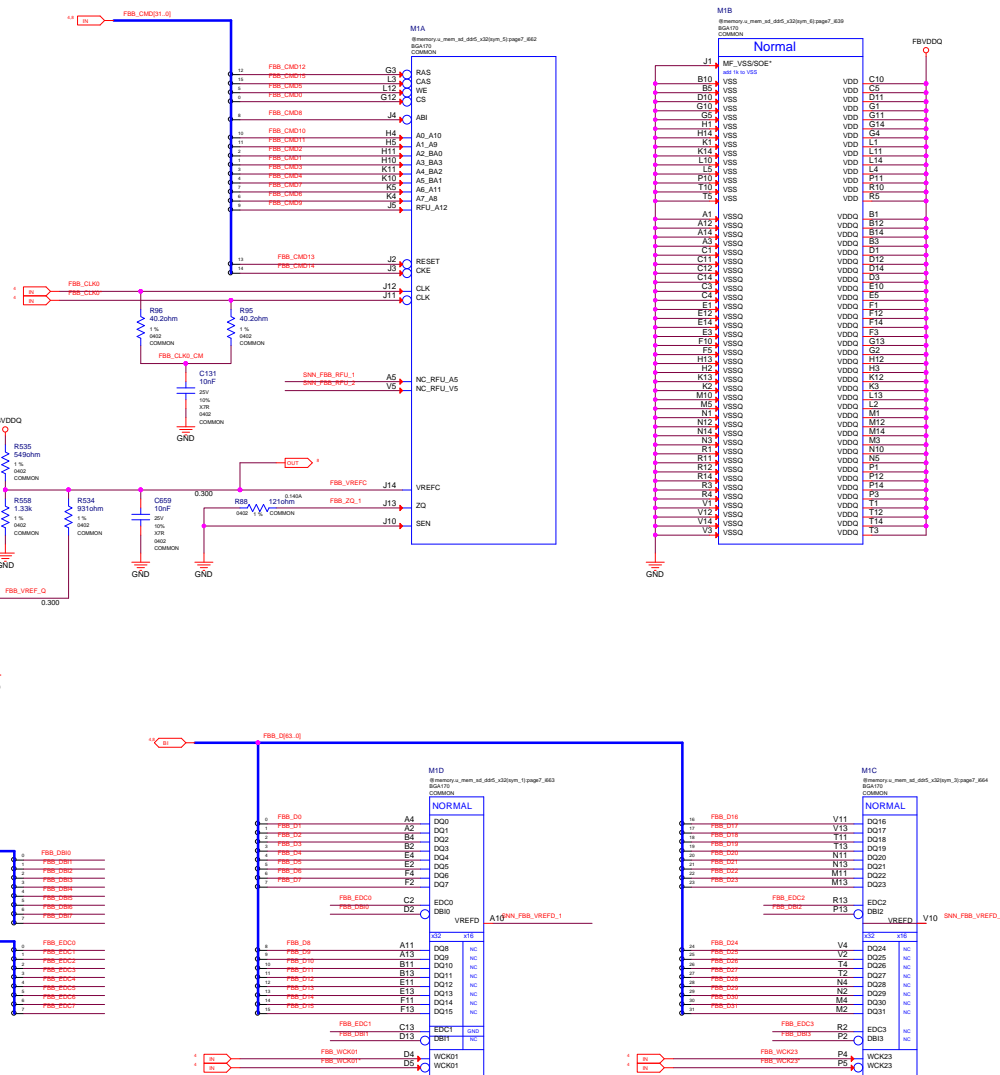


PLACE Around DRAM



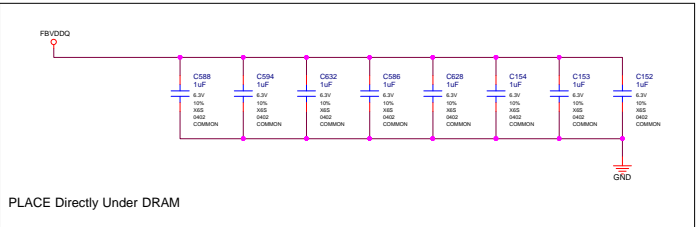
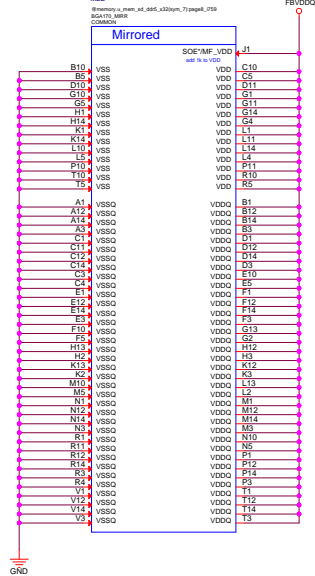
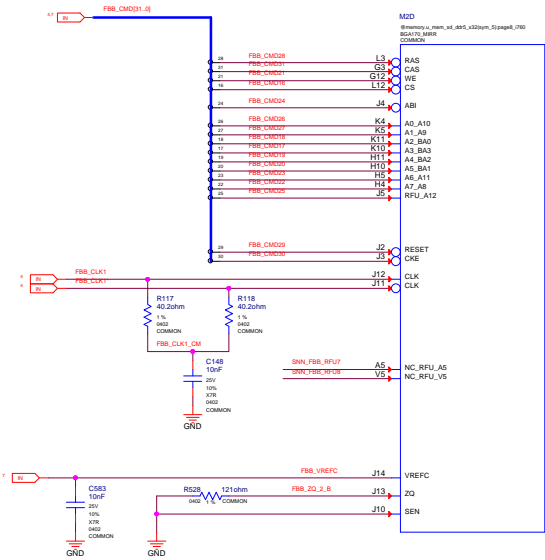
MEMORY: FBB Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3..BA3	
CMD2	A2..BA0	
CMD3	A4..BA2	
CMD4	A5..BA1	
CMD5	WE*	
CMD6	A7..A8	
CMD7	AB..A11	
CMD8	AB*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A9	
CMD12	RA3*	
CMD13	RB1*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17	A3..BA3	
CMD18	A2..BA0	
CMD19	A4..BA2	
CMD20	A5..BA1	
CMD21	WE*	
CMD22	A7..A8	
CMD23	AB..A11	
CMD24	AB*	
CMD25	A12..RFU	
CMD26	A0..A10	
CMD27	A1..A9	
CMD28	RA3*	
CMD29	RB1*	
CMD30	CKE*	
CMD31	CAS*	

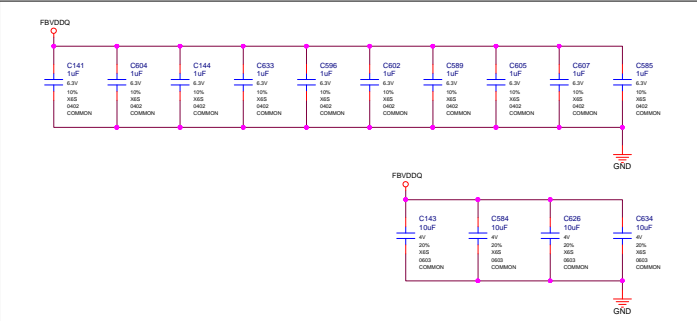


MEMORY: FBB Partition 63..32

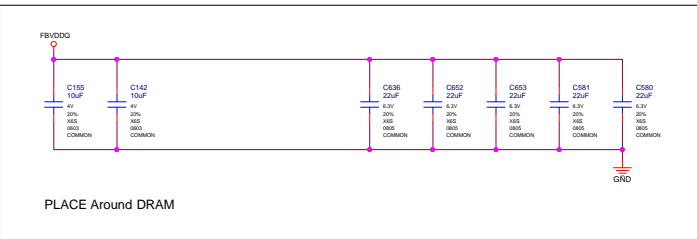
CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA2	
CMD3	A4_BA2	
CMD4	A0_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	AL_A11	
CMD8	AB*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A8	
CMD12	RAS*	
CMD13	RST*	
CMD14	CHE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA2
CMD19		A4_BA2
CMD20		A0_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		AL_A11
CMD24		AB*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A8
CMD28		RAS*
CMD29		RST*
CMD30		CHE*
CMD31		CAS*



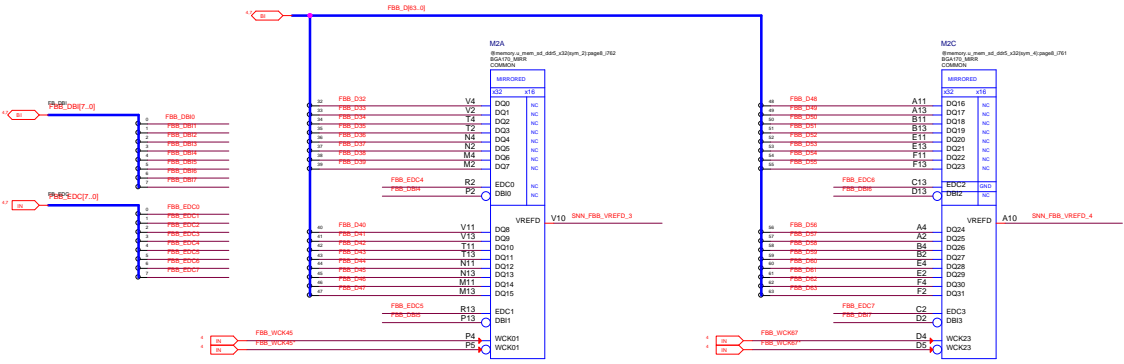
PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM



PLACE Around DRAM



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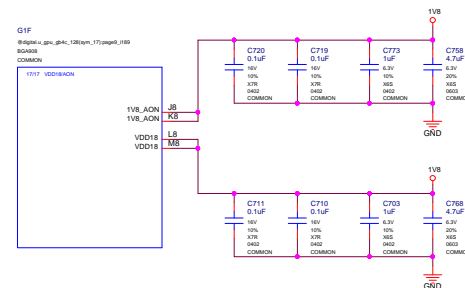
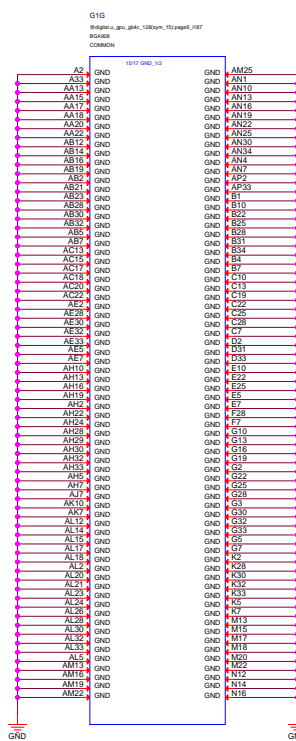
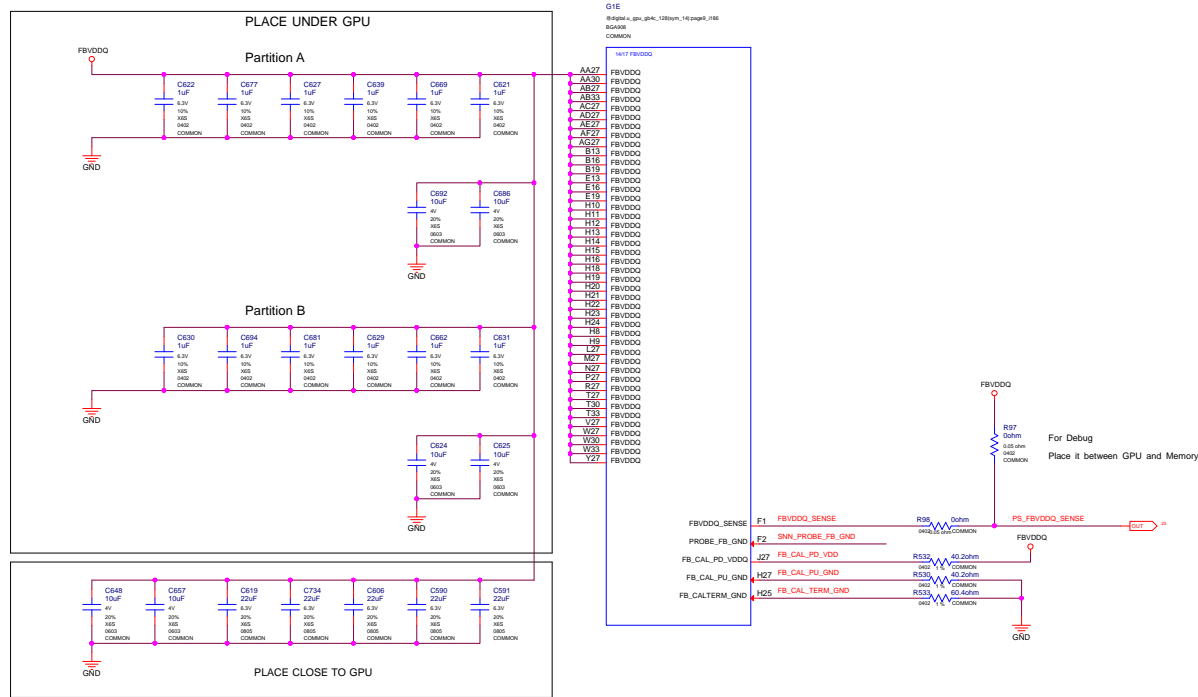
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB[63:32]

GPU FBVDDQ & 1V8 Decoupling



ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	GPU FBVDDQ & 1V8 Decoupling

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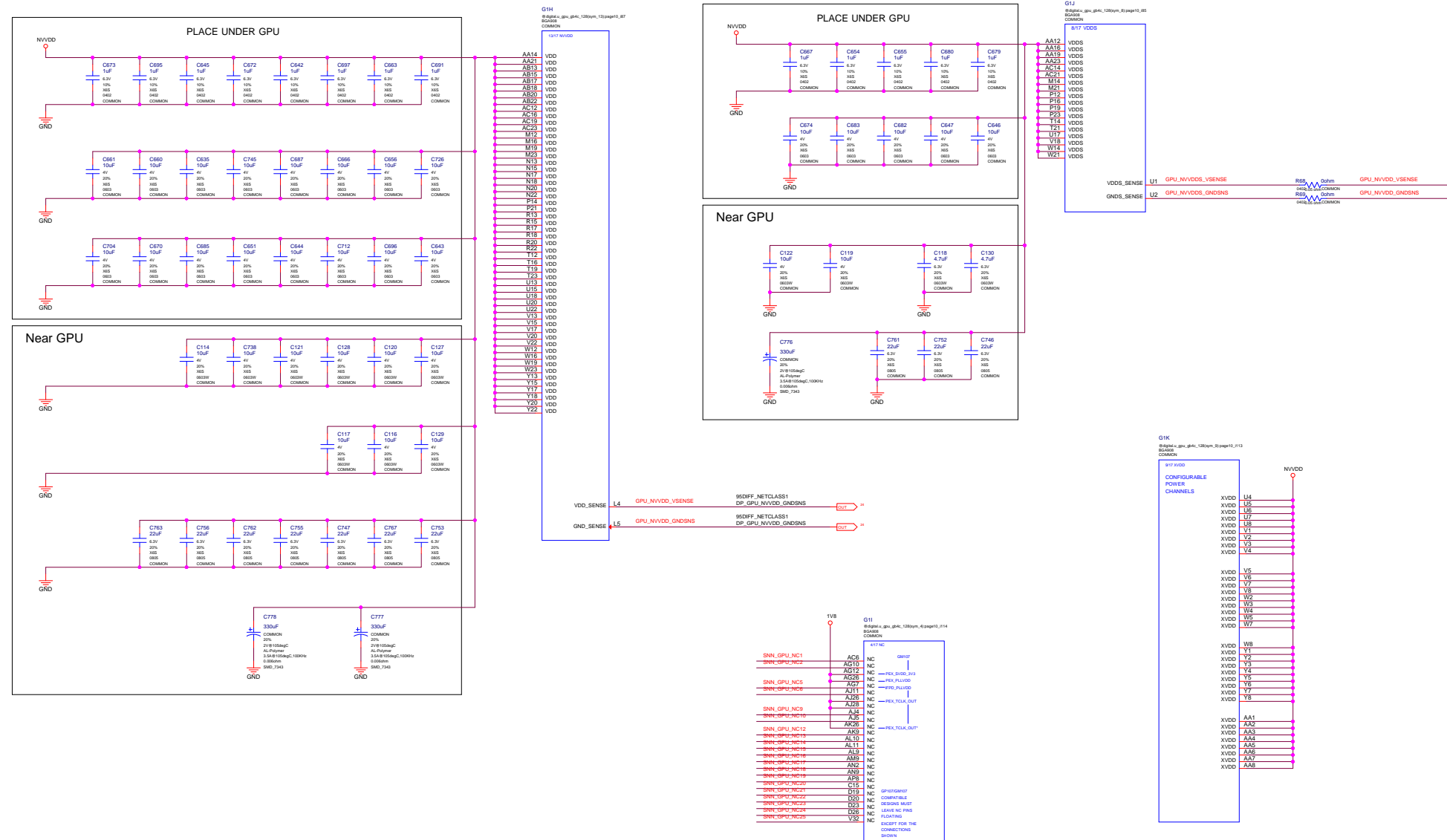
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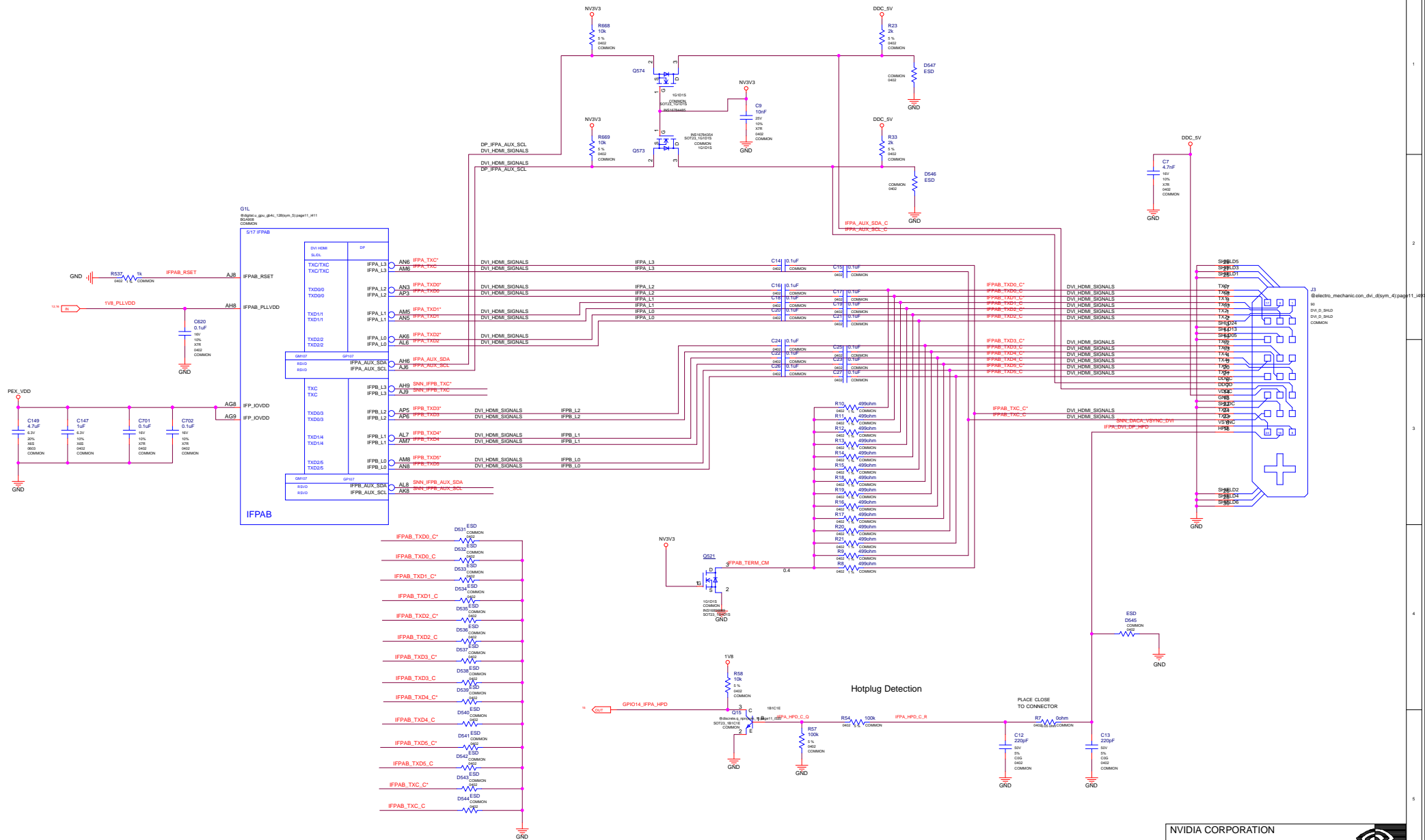
GPU NVVDD & NVVDDS Decoupling



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IFPAB DVI-DL



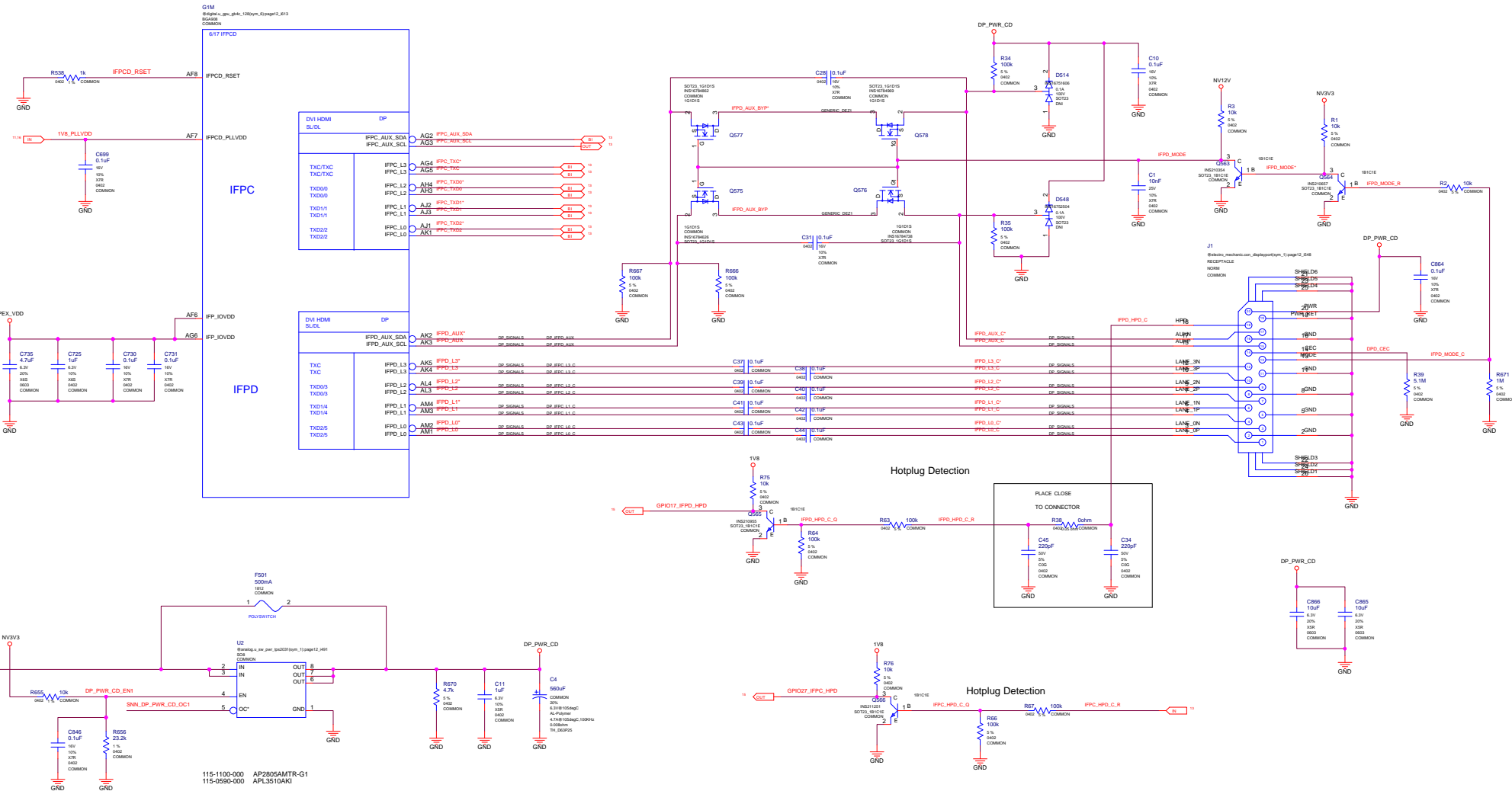
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PAGE DETAIL	IFPAB DVI-DL

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IFPD DP

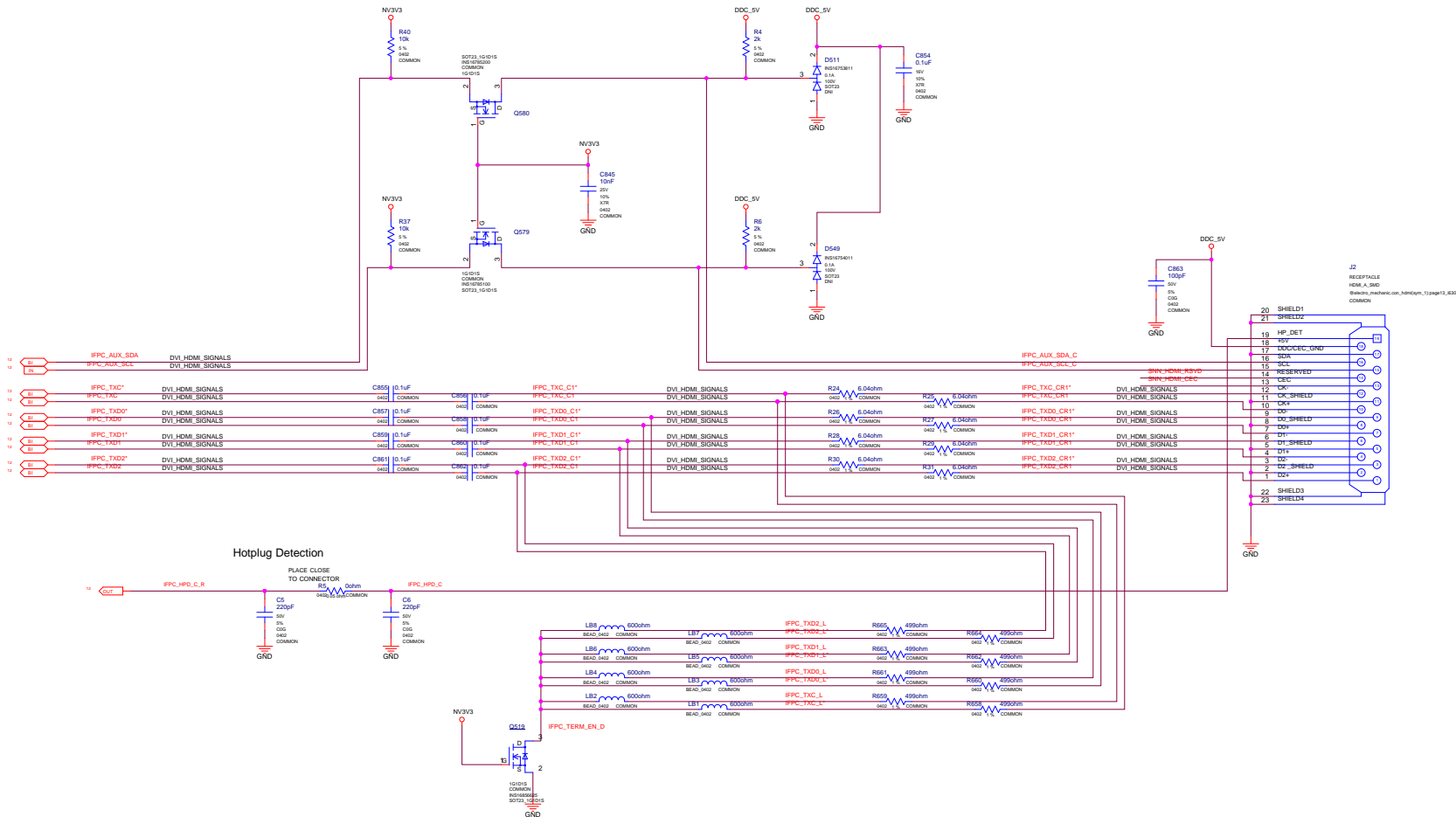


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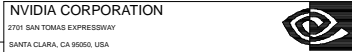
ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	IFPD DP

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IFPC HDMI

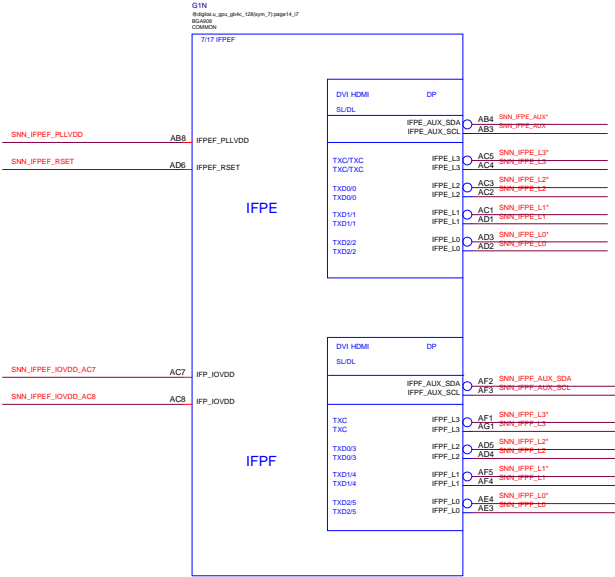


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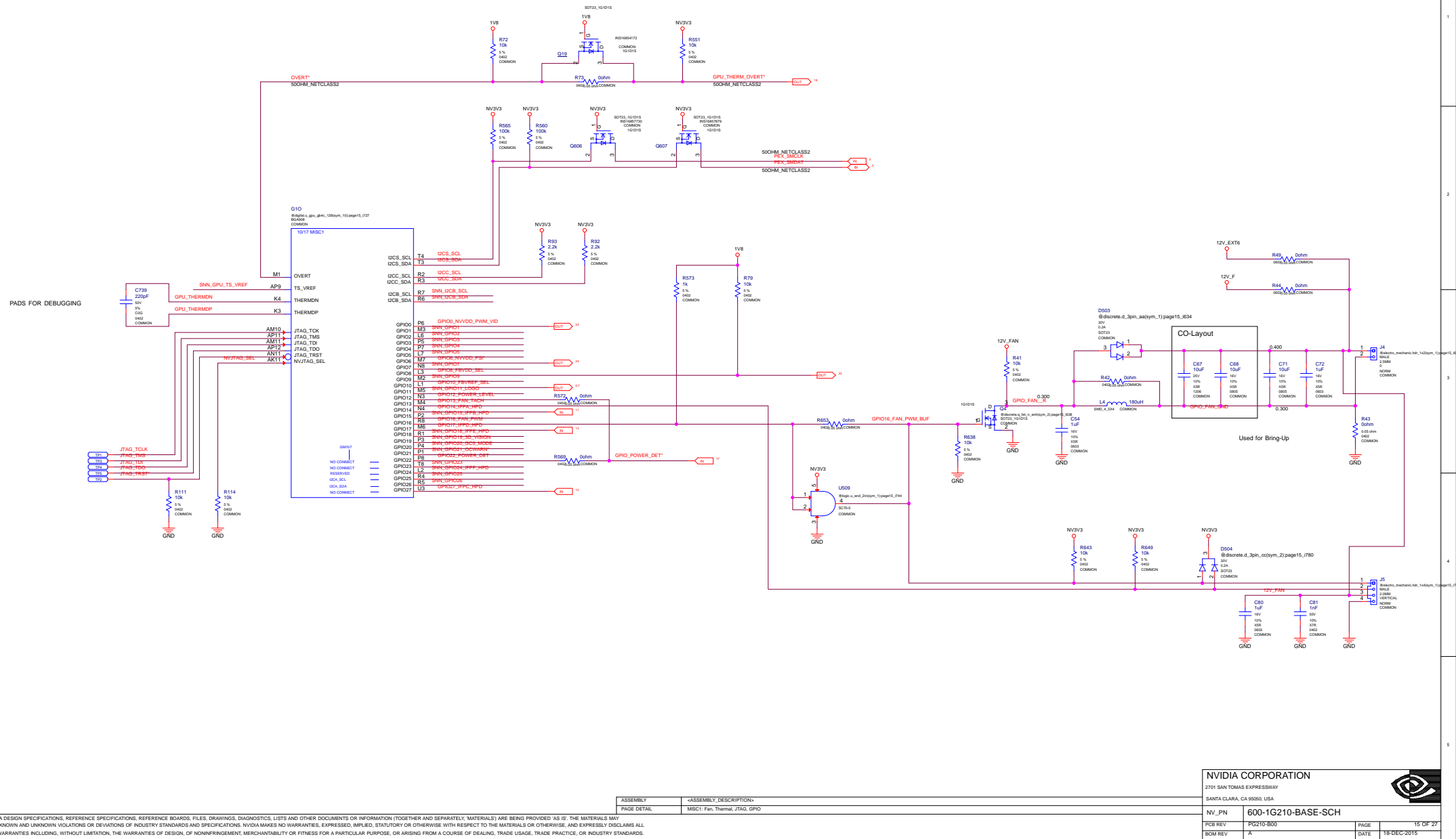
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MISC1: GPIO, Fan, Thermal, JTAG



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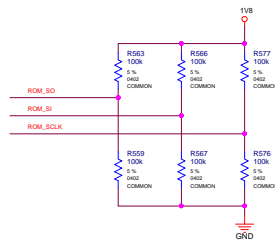
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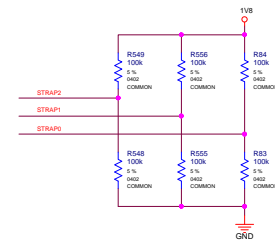
ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GP

MISC2: ROM, XTAL, Straps

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L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

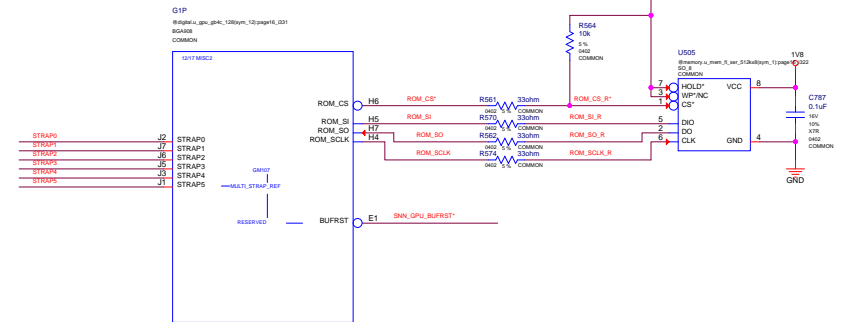
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

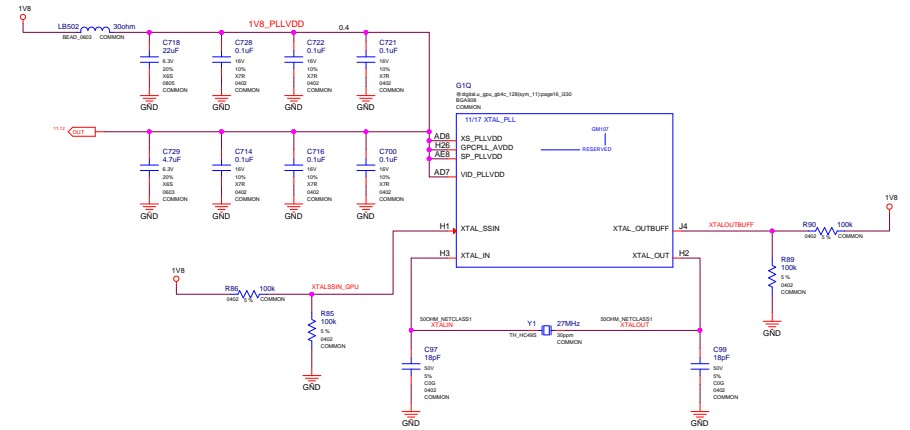
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```



Smart Fan

XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



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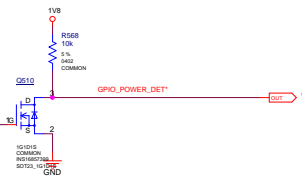
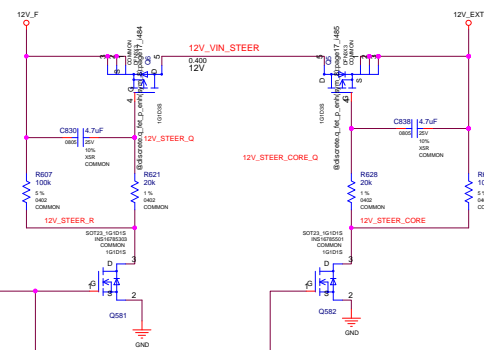
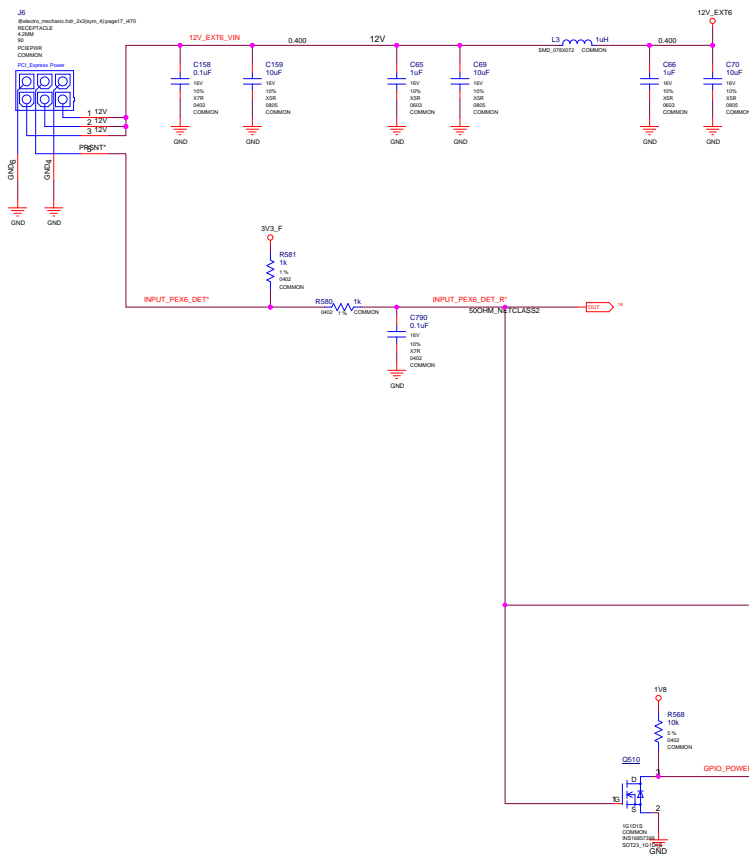
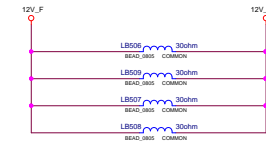
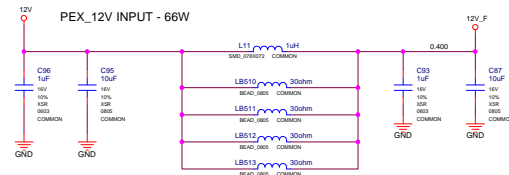
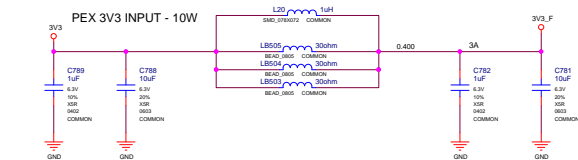


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ASSEMBLY	«ASSEMBLY_DESCRIPTION
PAGE DETAIL	MISC2: ROM, XTAL, Straps

Power Inputs and Filtering



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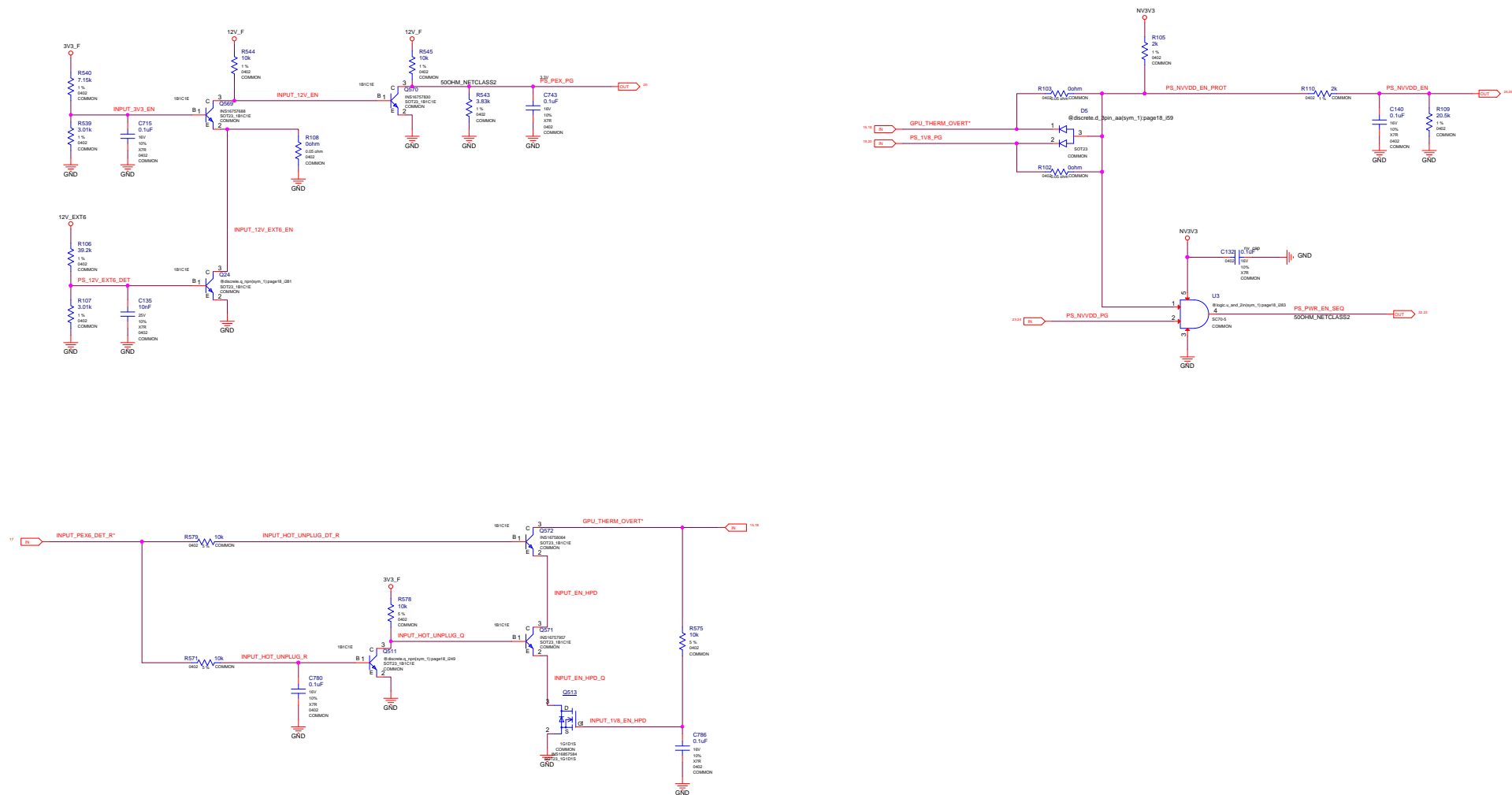
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Power sequence



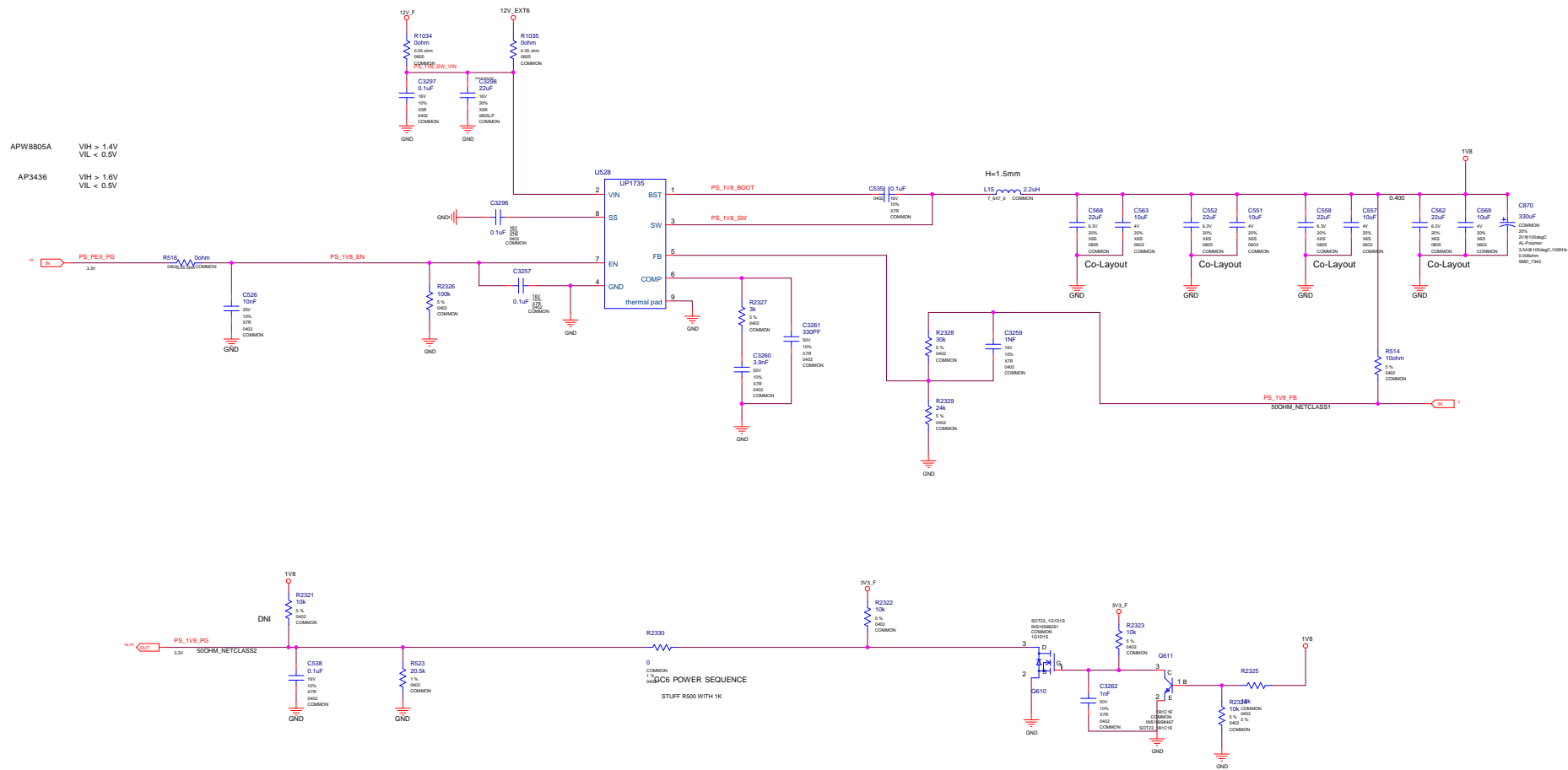
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ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	Power Sequence

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PS I: 1V8



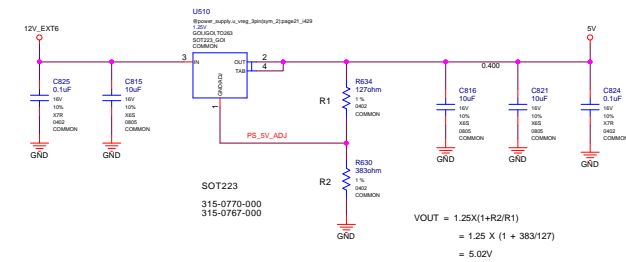
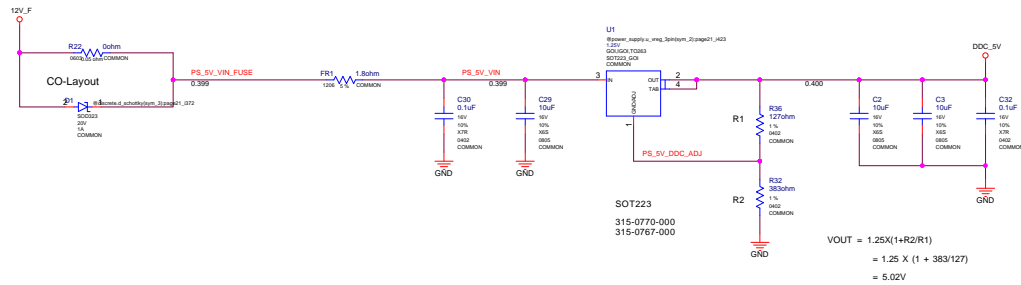
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PSt 1V8

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PSII:5V & 12V_FAN



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PSII: 5V & 12V_FAN

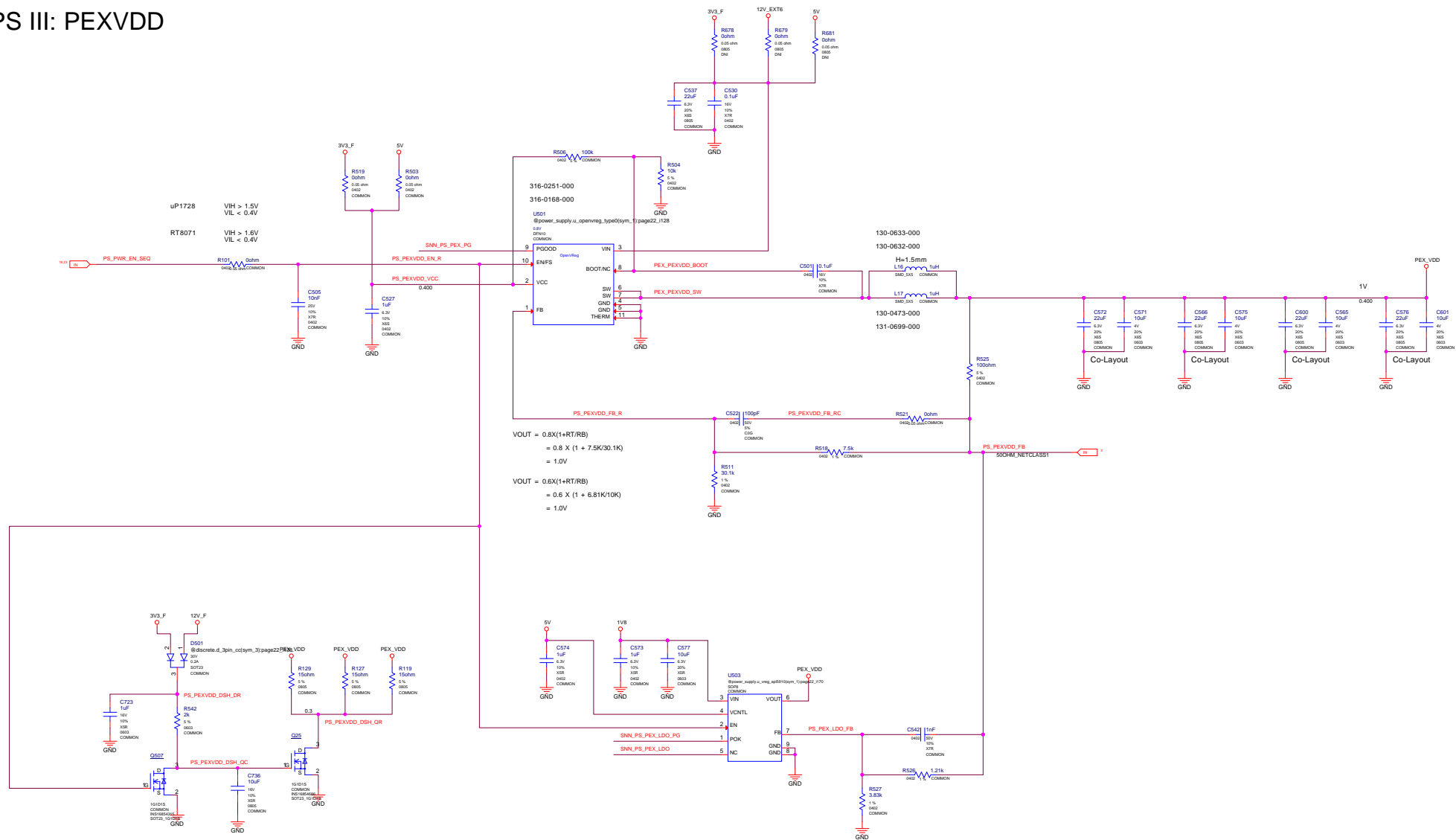
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PS III: PEXVDD



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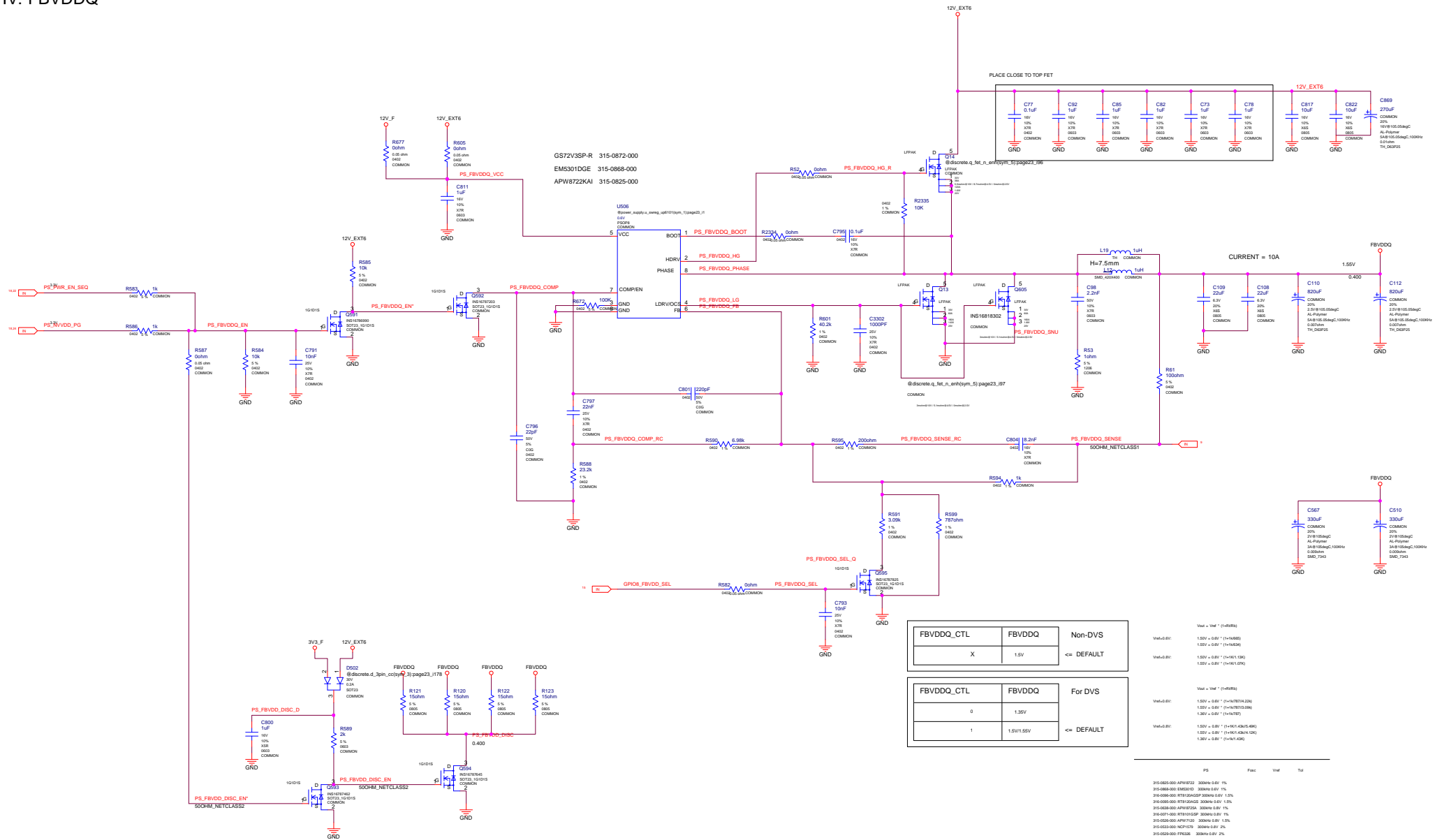
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PS IV: FBVDDQ



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ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	PS IV: FBVDDQ

FBVDDQ_CTL	FBVDDQ	Non-DVS
X	1.5V	
		<= DEFAULT

FBVDDQ_CTL	FBVDDQ	For DVS
0	1.35V	
1	1.5V/1.55V	
		<= DEFAULT

	$V_{\text{out}} = V_{\text{in}} * (1 + R1/R2)$
$V_{\text{out}} = 0.5V$	$0.50V = 0.5V * (1 + R1/R2)$ $1.55V = 0.5V * (1 + R1/R2)$
$V_{\text{out}} = 0.8V$	$0.50V = 0.8V * (1 + R1/R2)$ $1.55V = 0.8V * (1 + R1/R2)$
	$V_{\text{out}} = V_{\text{in}} * (1 + R1/R2)$
$V_{\text{out}} = 0.5V$	$0.50V = 0.5V * (1 + R1/R2/2.2k)$ $0.50V = 0.5V * (1 + R1/R2/3.3k)$ $1.36V = 0.5V * (1 + R1/R2)$
$V_{\text{out}} = 0.8V$	$0.50V = 0.8V * (1 + R1/R2/5.6k)$ $1.55V = 0.8V * (1 + R1/R2/3.3k)$ $1.36V = 0.8V * (1 + R1/R2)$

PS	Fosc	Vref
----	------	------

215-0825-000: APW8722	300kHz 0.8V 1%
215-0868-000: EM5201D	300kHz 0.8V 1%
216-0096-000: RT8120AGSP	300kHz 0.6V
216-0095-000: RT8120AGS	300kHz 0.6V
215-0638-000: APW8725A	300kHz 0.8V 1%
216-0071-000: RT8101GSP	300kHz 0.8V 1%
215-0526-000: APW7120	300kHz 0.8V 1%
215-0523-000: NCP1579	300kHz 0.8V 2%
215-0529-000: FR6326	300kHz 0.8V 2%

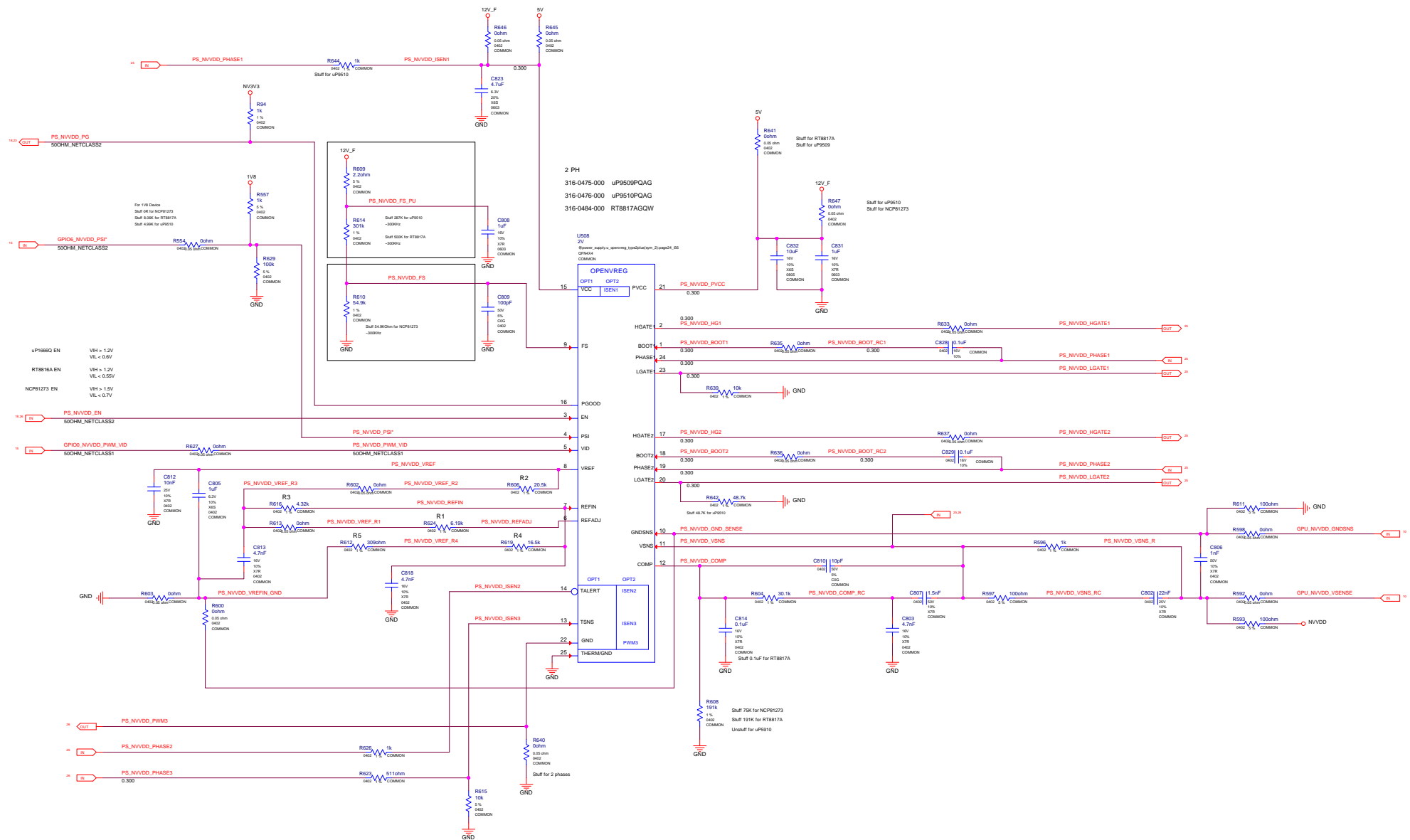
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PS V: NVVDD OVR2+1



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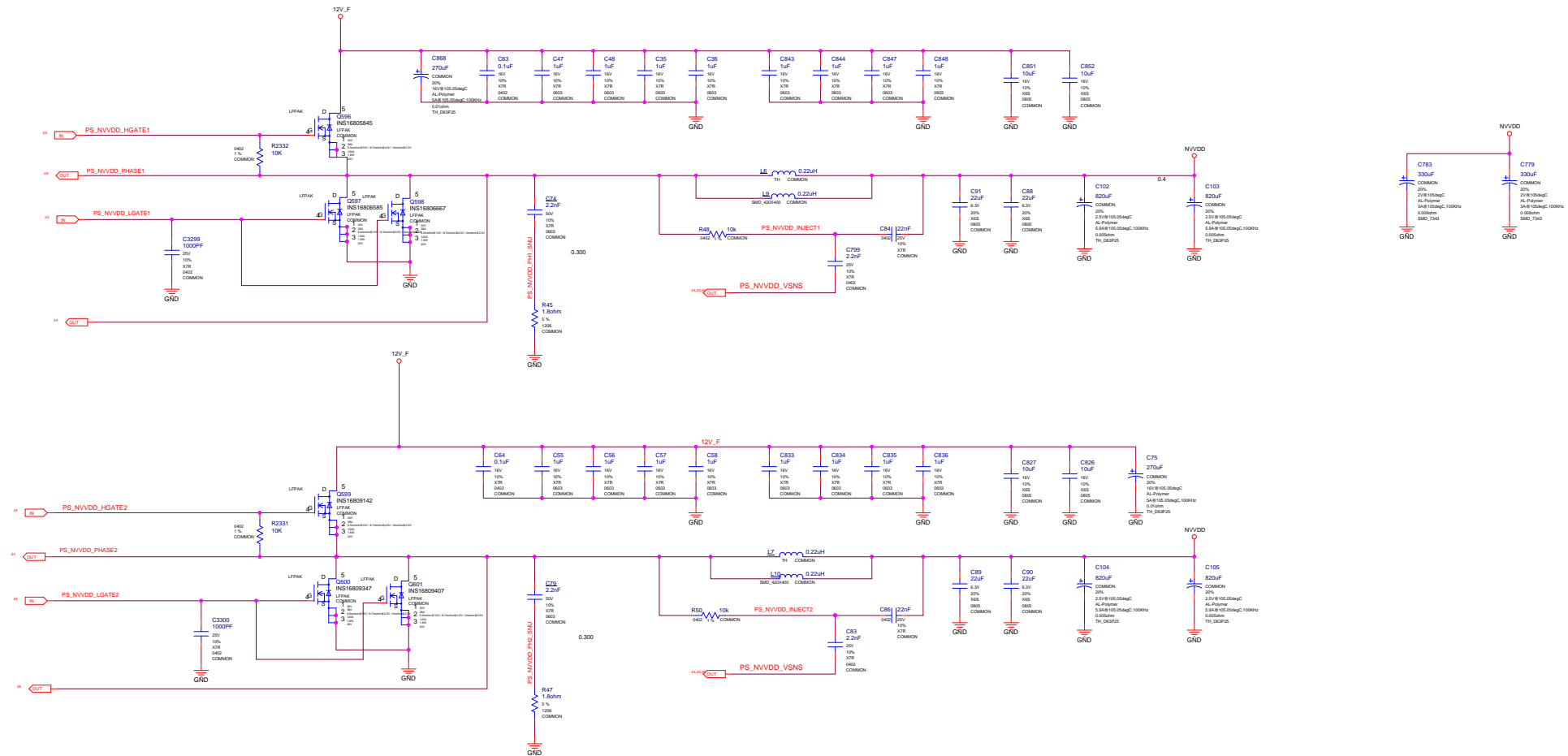



NV_PN	600-1G210-BASE-SCH		
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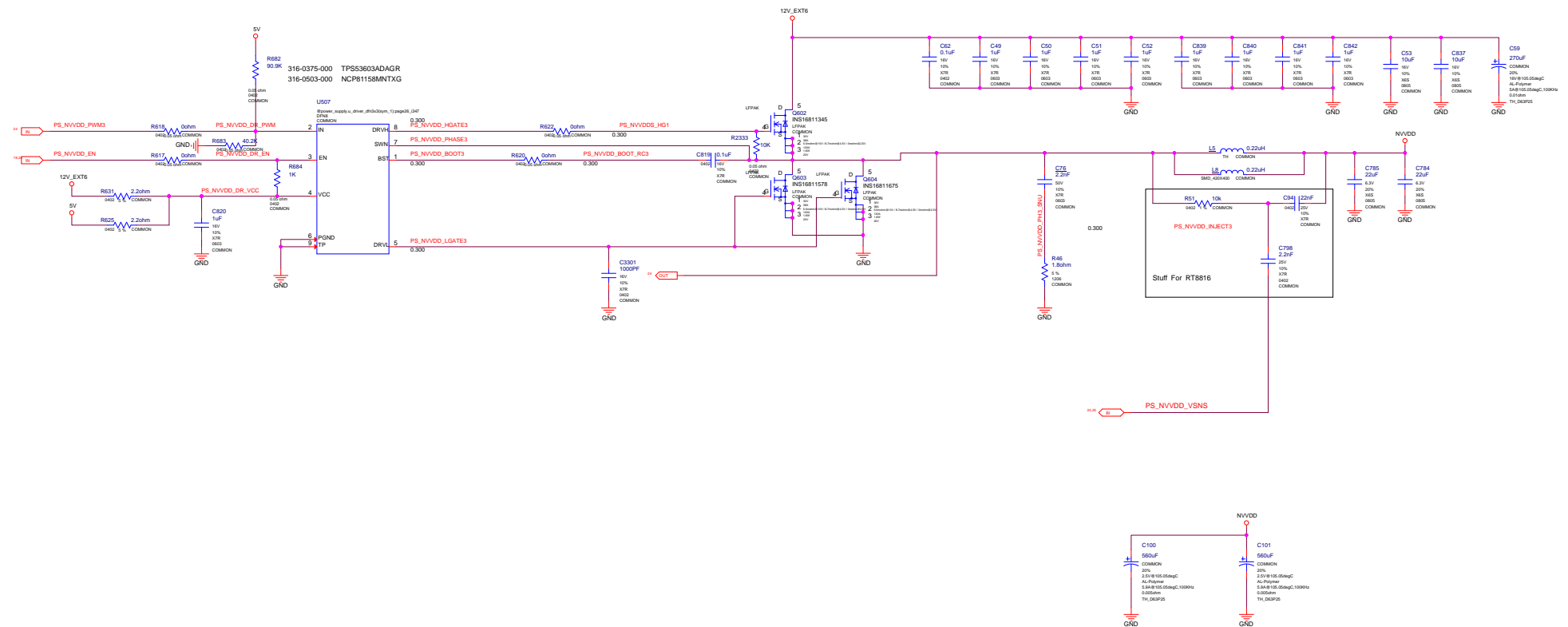
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS V: NVVDD OVR2+1

PS V: NVVDD Phase 1,2



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ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	PS V: NVVDD Phase 3

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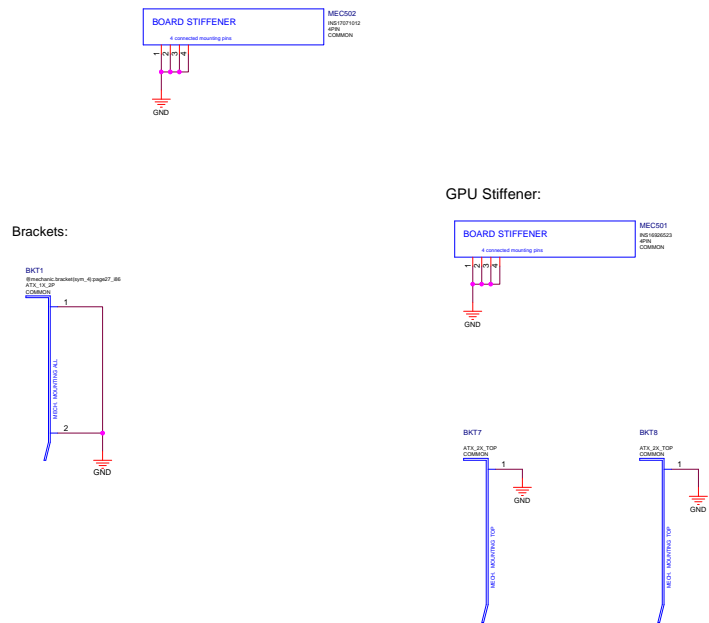
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


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Mechanical: Bracket/Thermal Solution



ASSEMBLY		-ASSEMBLY DESCRIPTION-		SANTA CLARA, CA 95050, USA	
PAGE DETAIL		MECH Bracket/Thermal			
MAY DISCLOSES ALL Y STANDARDS.				NV_PN 600-1G210-BASE-SCH	
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