NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X

PCI DEVICE ID 0X0=0X200 FOR NV20.

NVVDD SET TO: 1.67V FOR -H CHIP
FBVDD SET TO: 3.47V
FBVDDQ SET TO: 2.59V

HISTORY REVISION:

X00: Based on P50-A06
- See change list in 149- file.
- Set FBVDDQ=2.59V

P50-A07-X01:

- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

P50-A08:

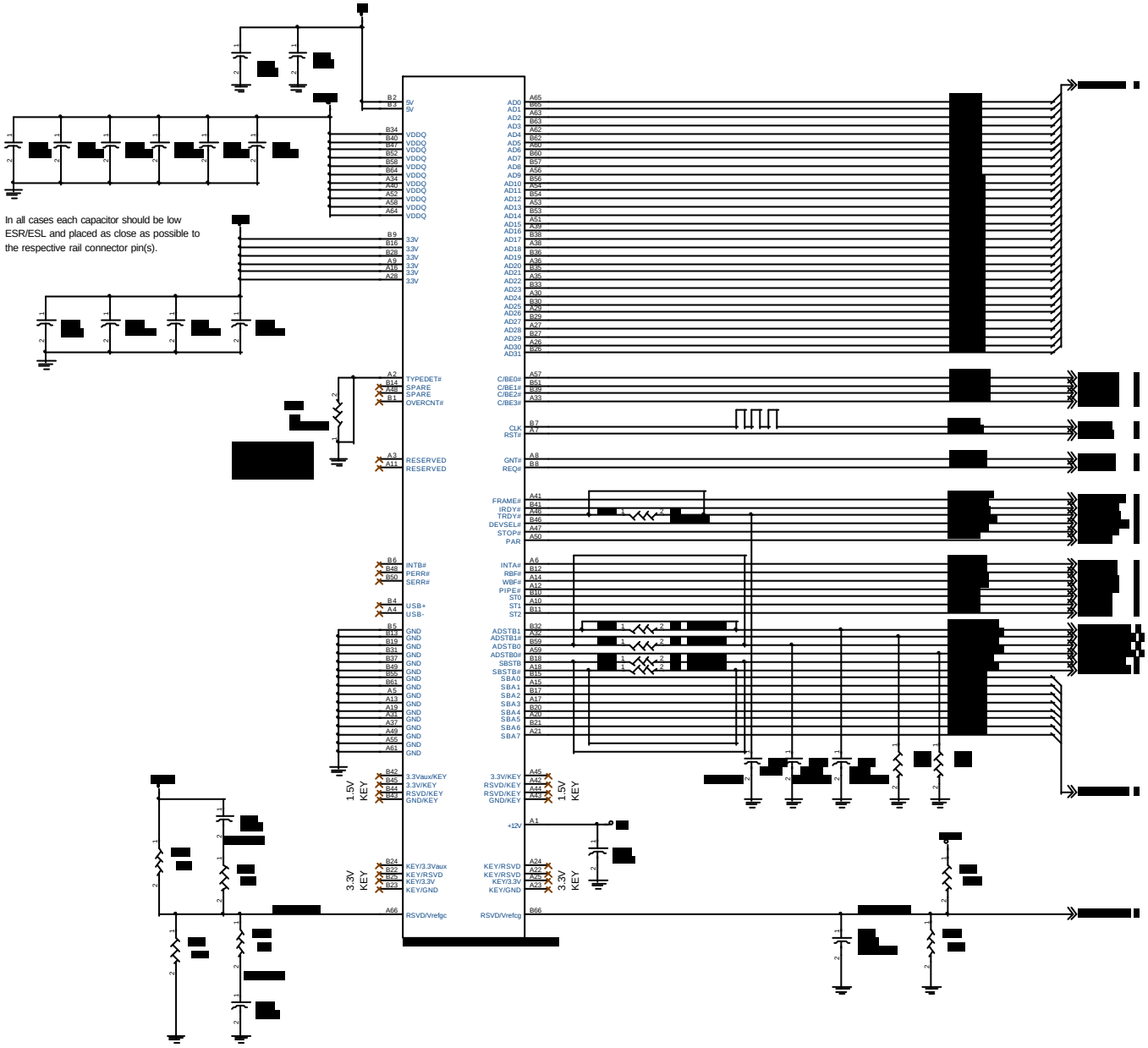
X04: - Delay PLL_VDD to come up after NVVDD.
X05: - Added 1UF accross R257.
X06: - Removed X04-5 above, added a switcher generated PLL delay option.
- SSENA cap for 2nd SW changed to 1UF.
- A05 Si, NVVDD=1.52V

P50-A09:

X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.
X03: - Added option to pull up power good to 12V

ECO1235: - Changed R841 PU to 10K (from 4.7K)

ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction. Replaced C303,306,309 with 75ohm and no stuffed R208-210.



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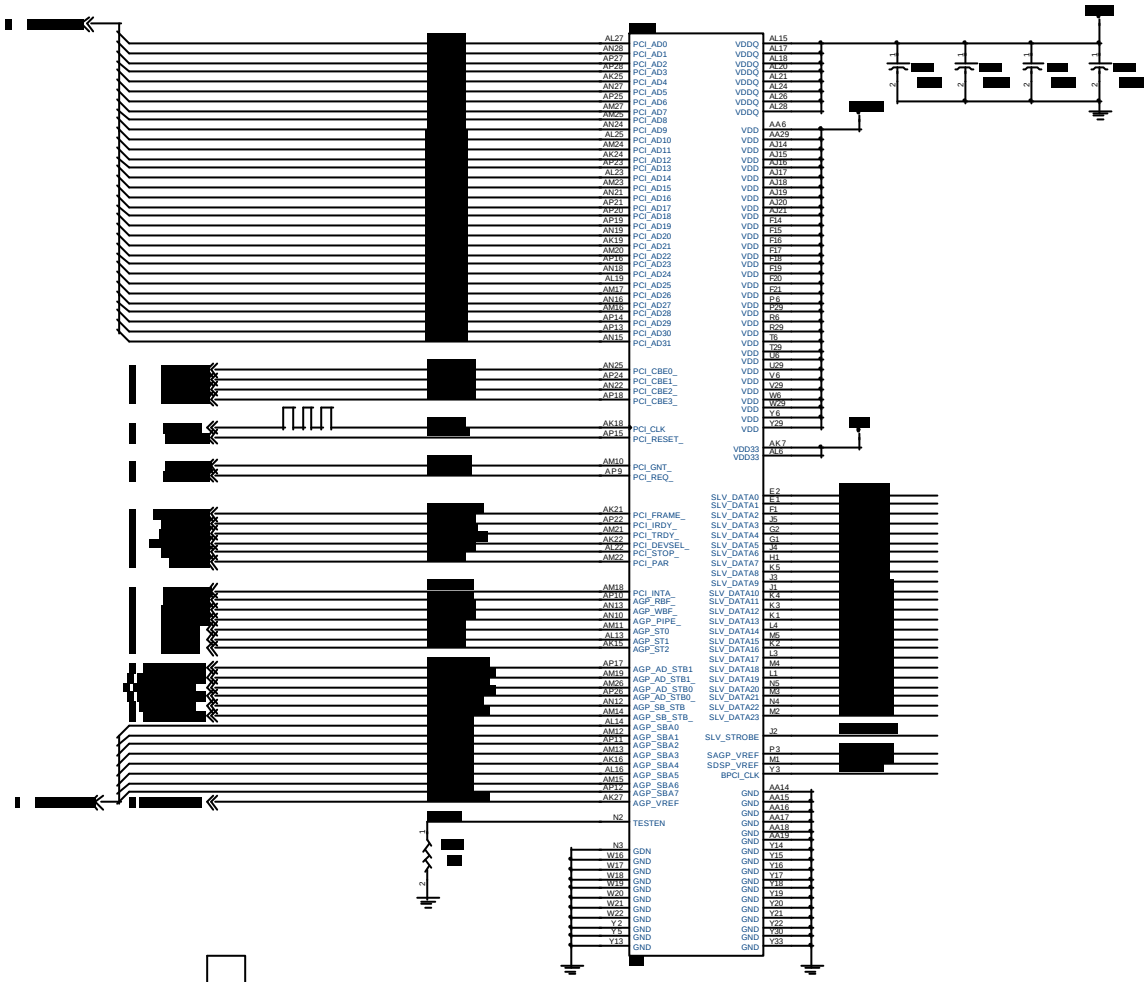
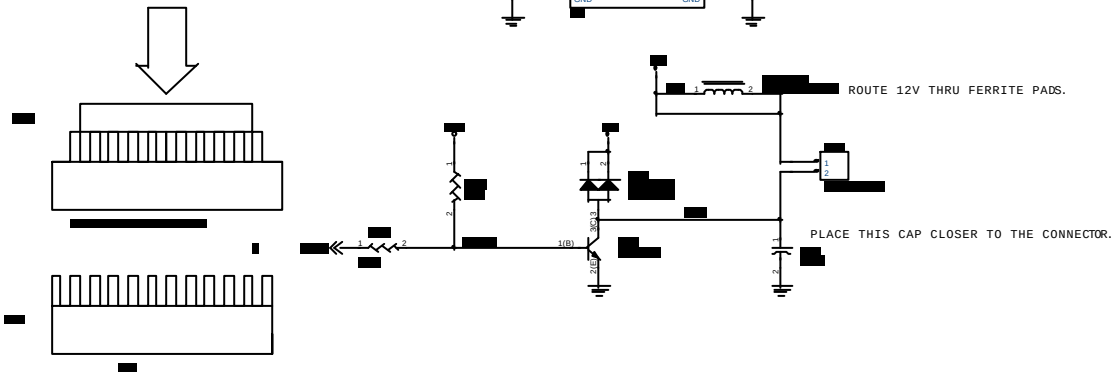
BUS I/O	





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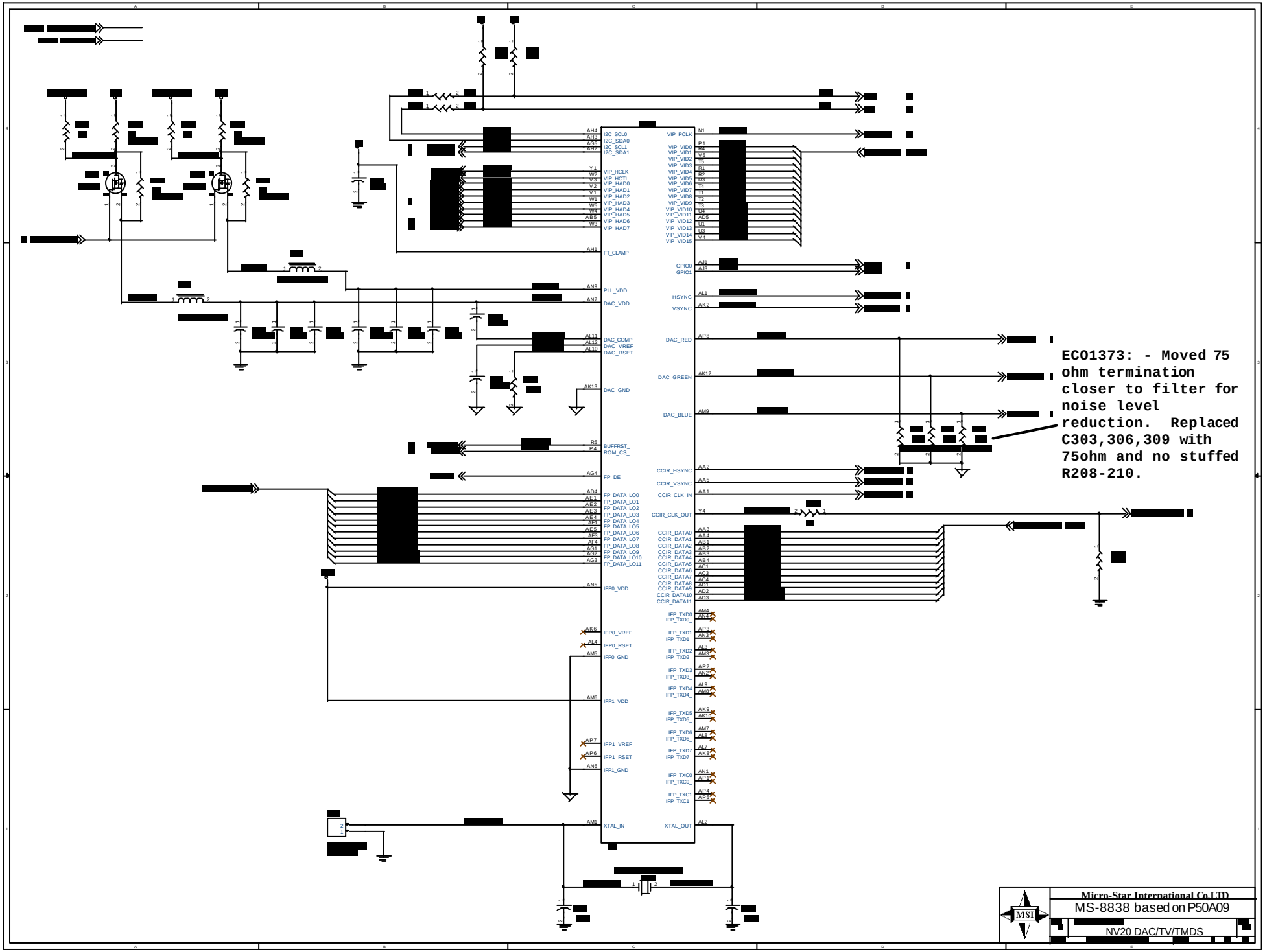
NV20 HOST	



ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction. Replaced C303,306,309 with 75ohm and no stuffed R208-210.

Use thick (non-impedance controlled) traces on XTALIN/OUT

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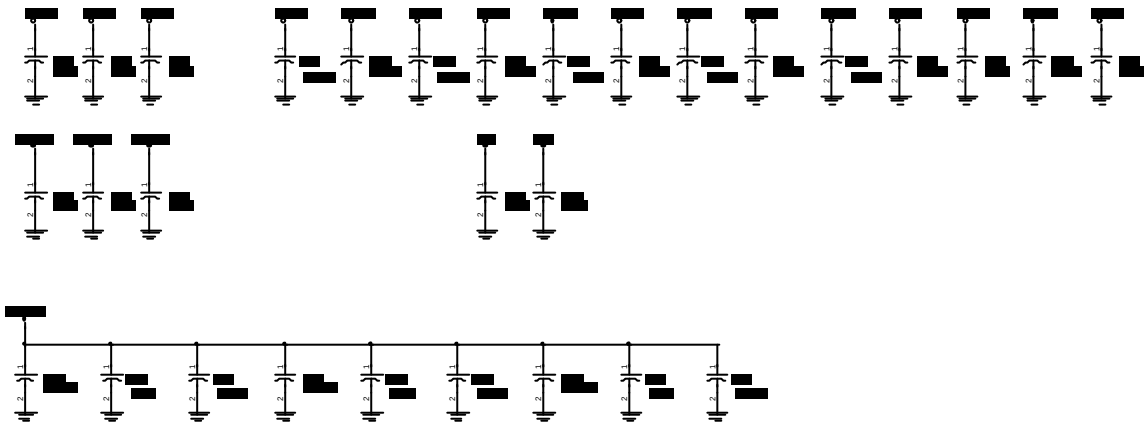
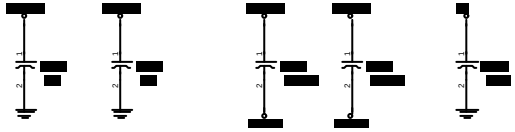
NV20 DAC/TV/TMDS



For EMI Solution



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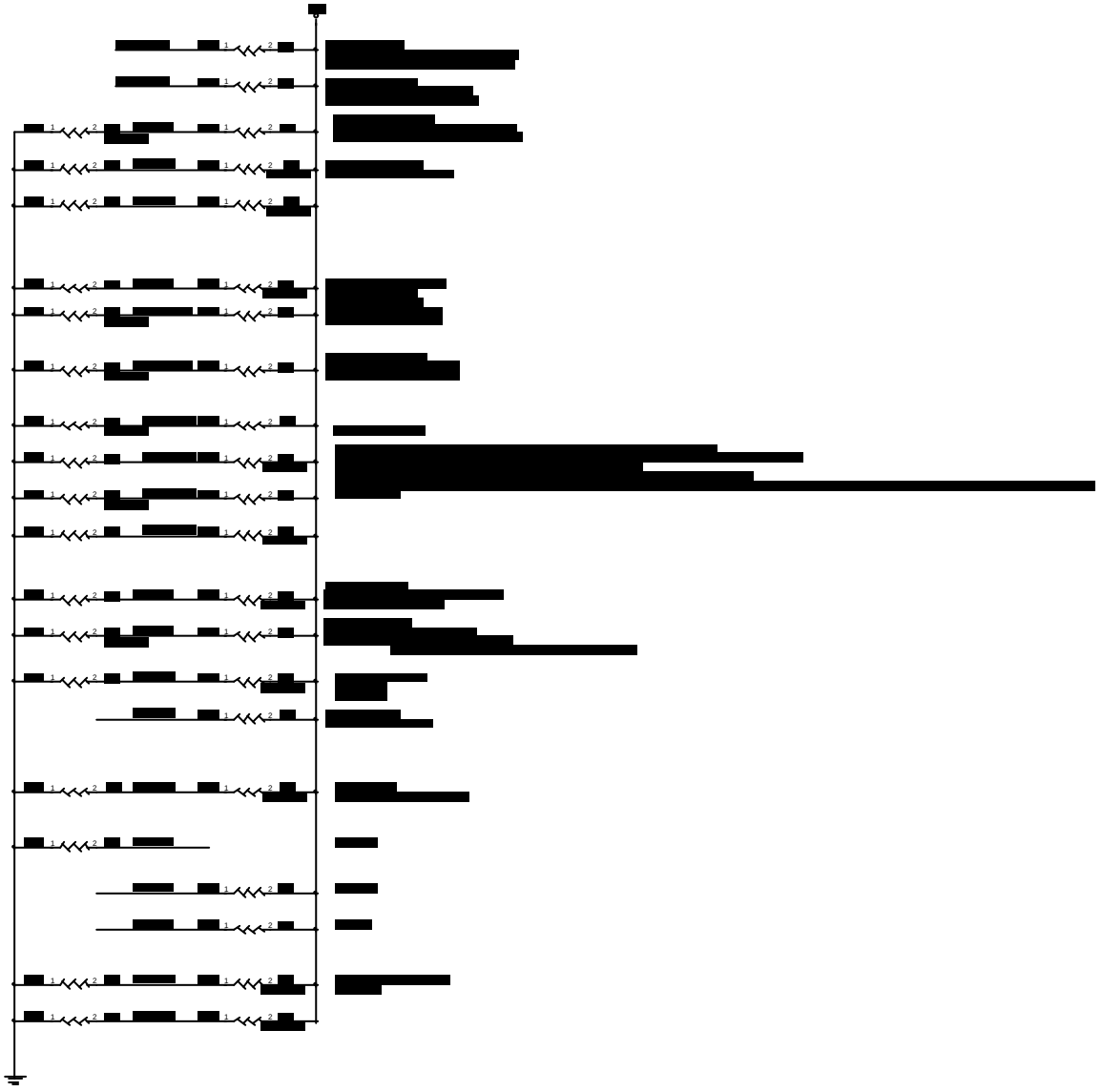
NV20 DECOUPLING



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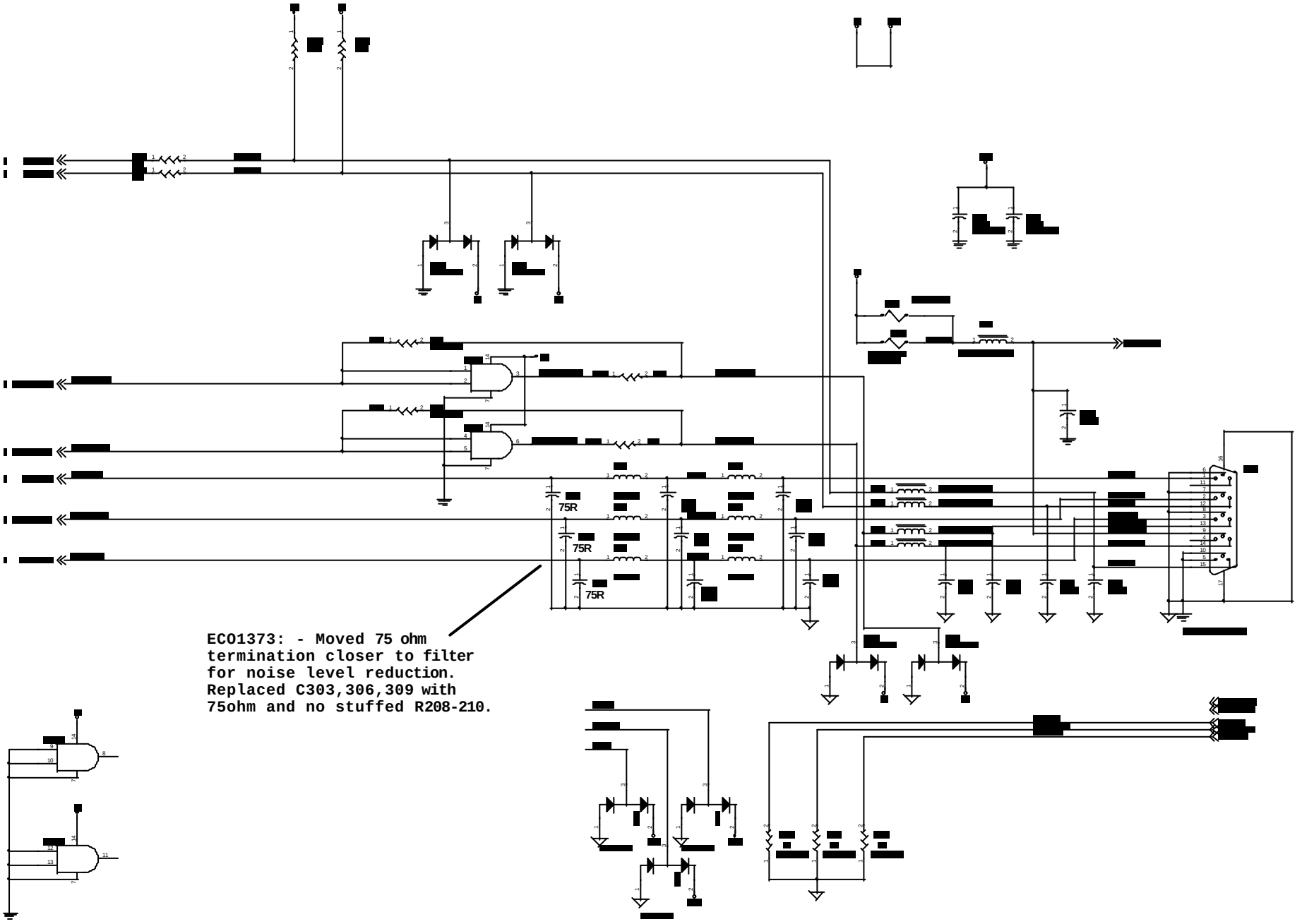
NV20 HOST STRAPS



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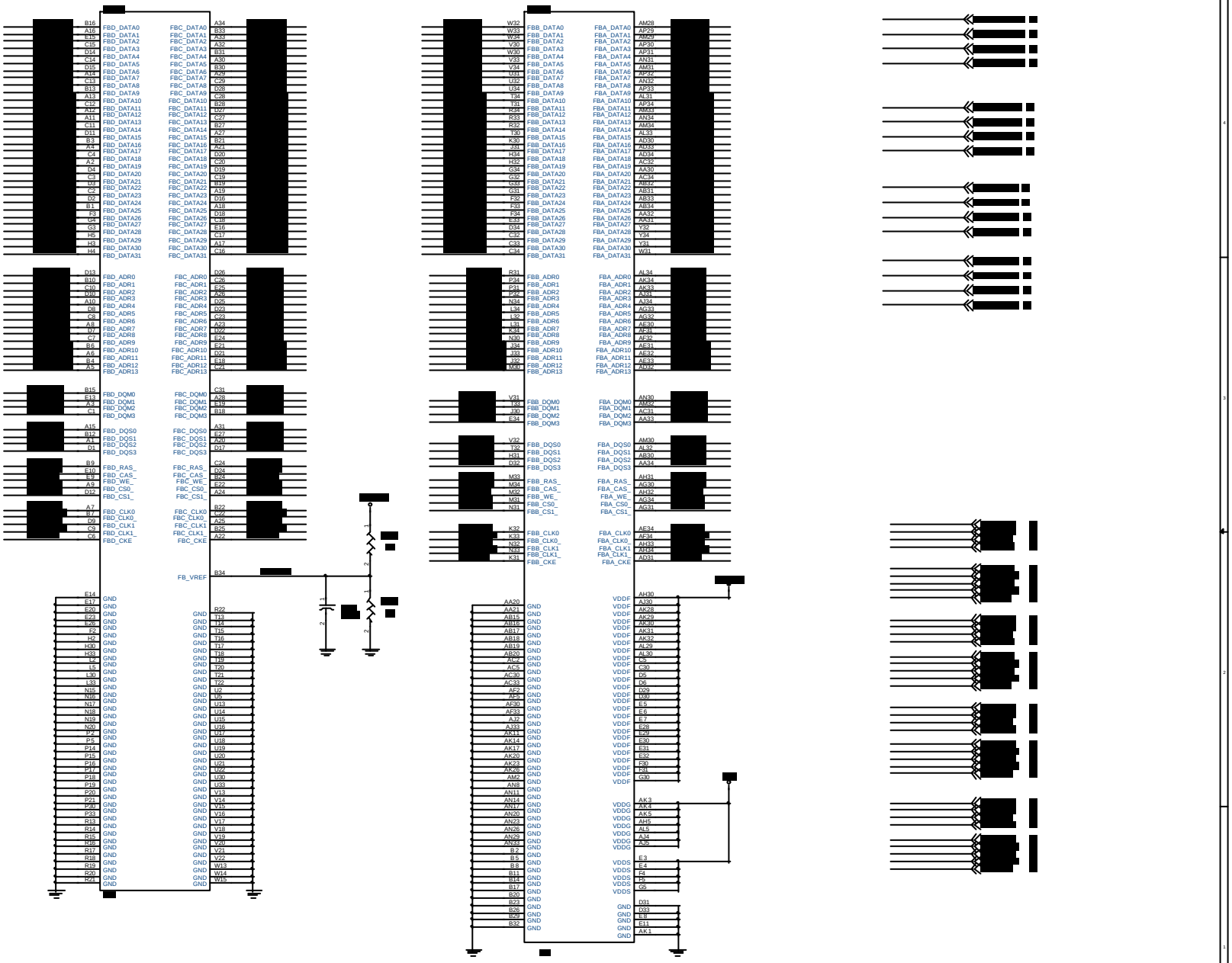
Micro-Star International Co.LTD
MS-8838 based on P50A09
DAC I/O



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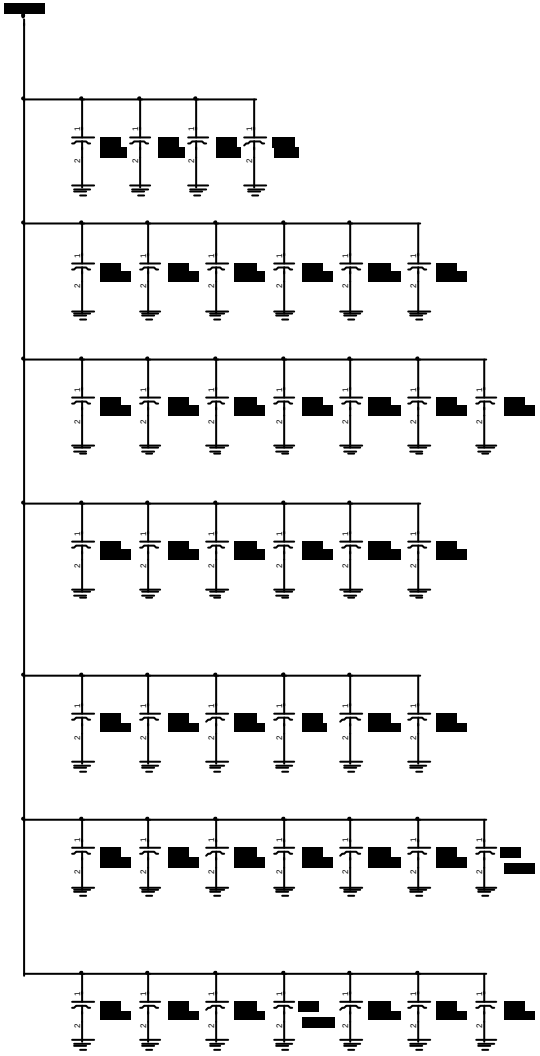
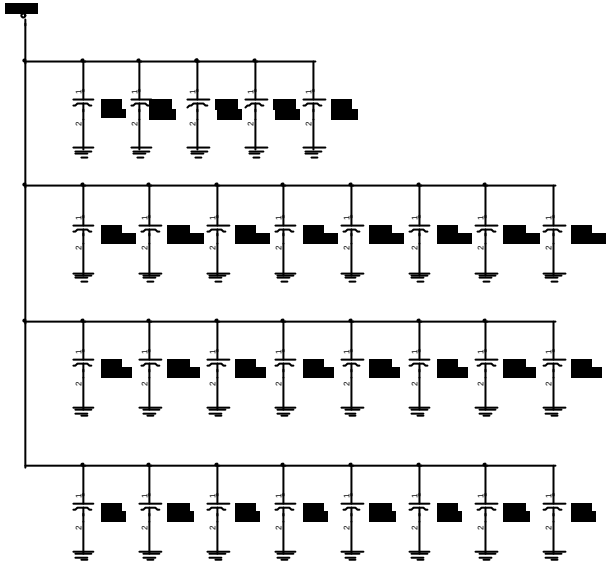
MS-8838 based on P50A09	
NV20 FBA/B/C/D	





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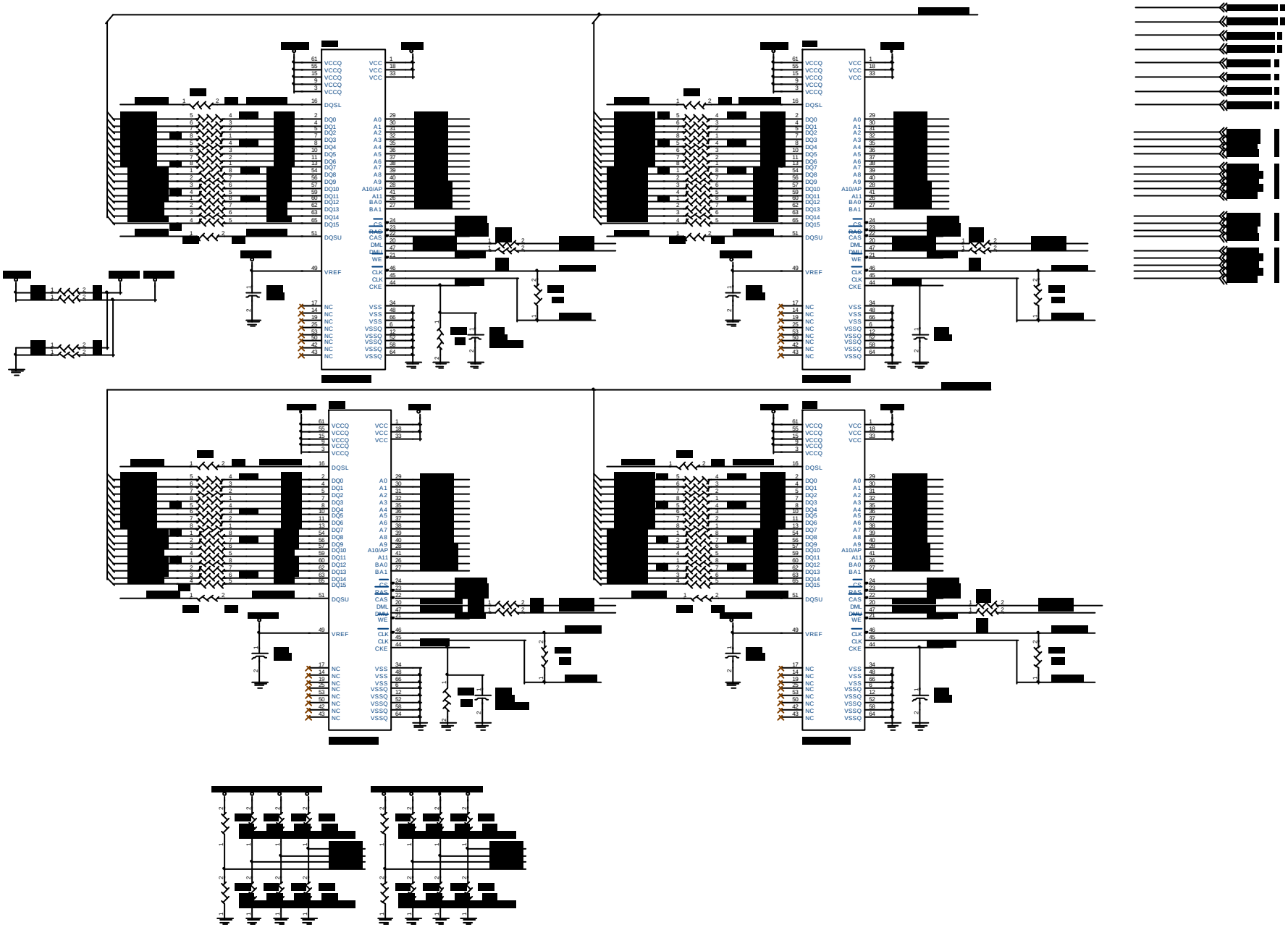
FB DECOUPLING 4MX16 SDRAM



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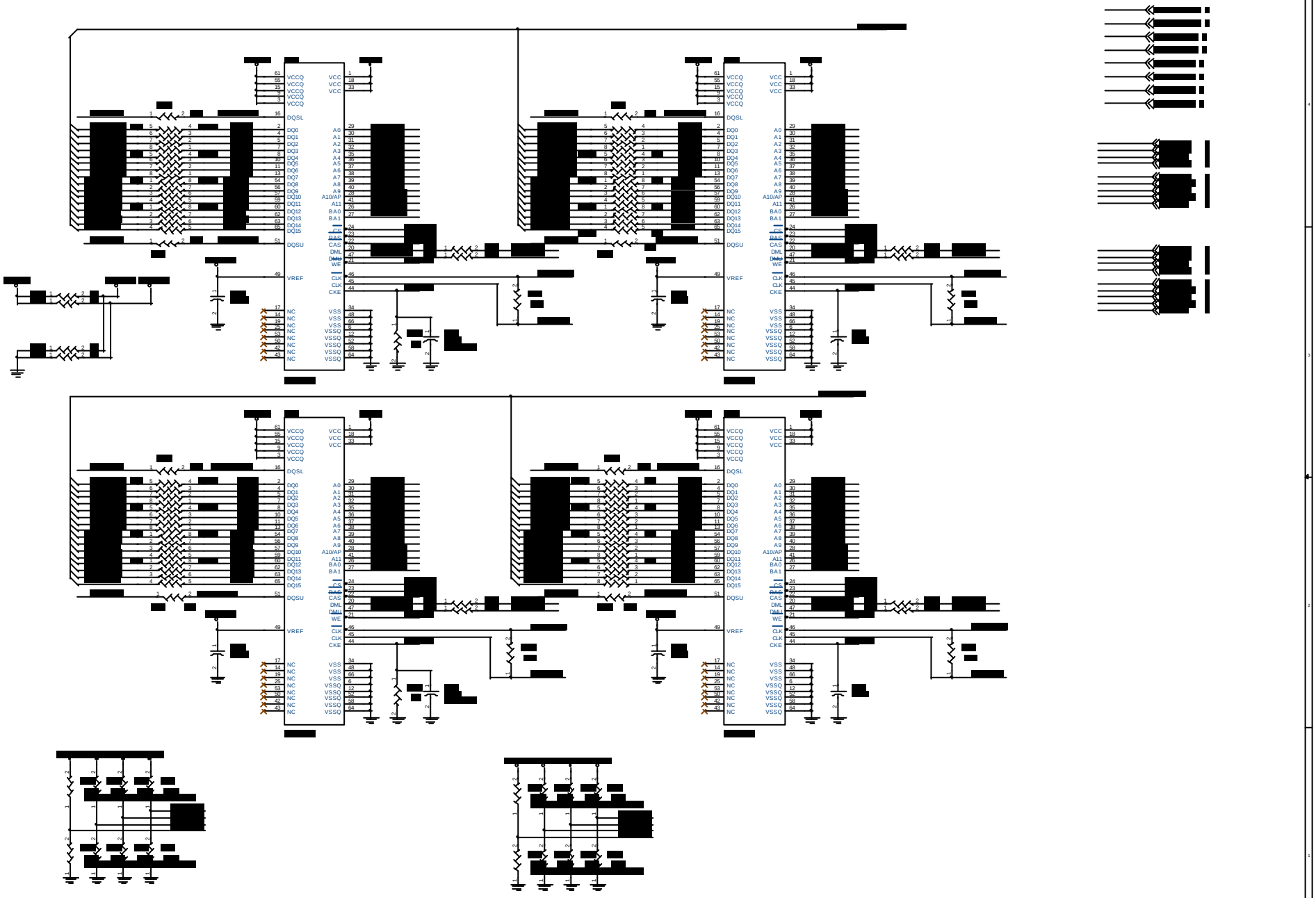
FBA/B DDR 4MX16 SDRAM	



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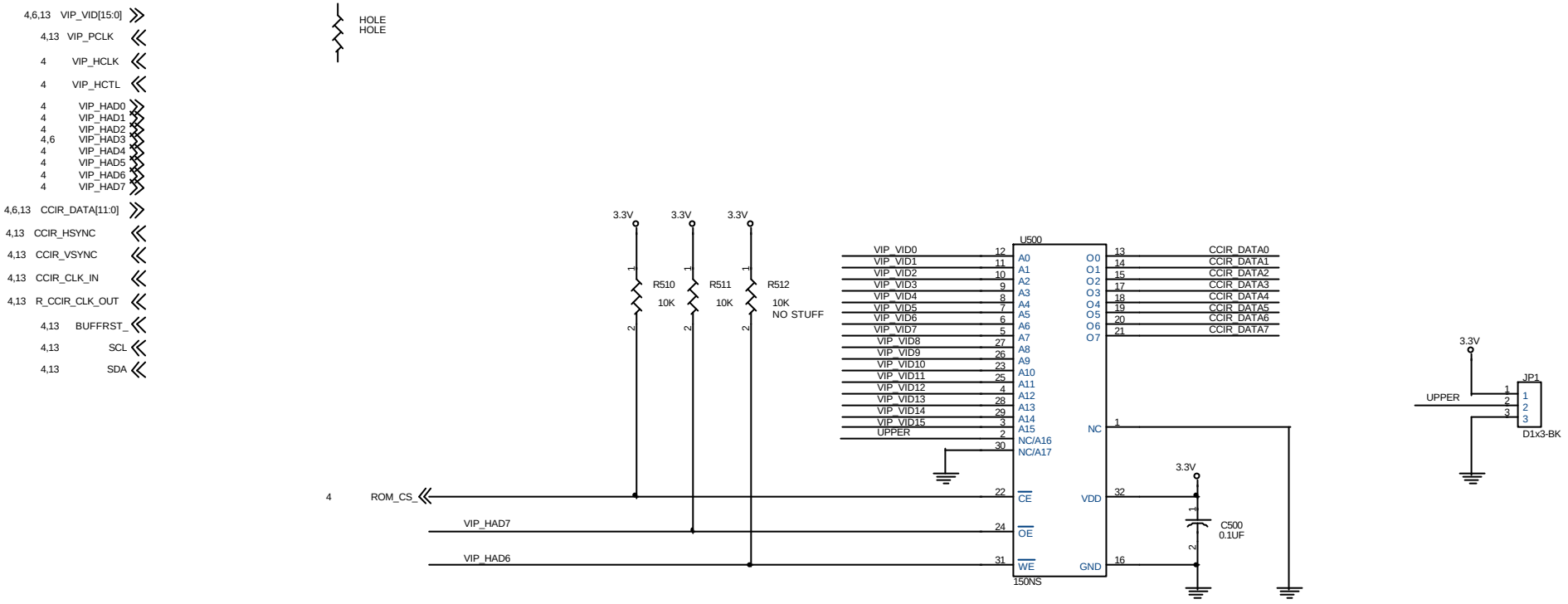
FBC/D DDR 4MX16 SDRAM



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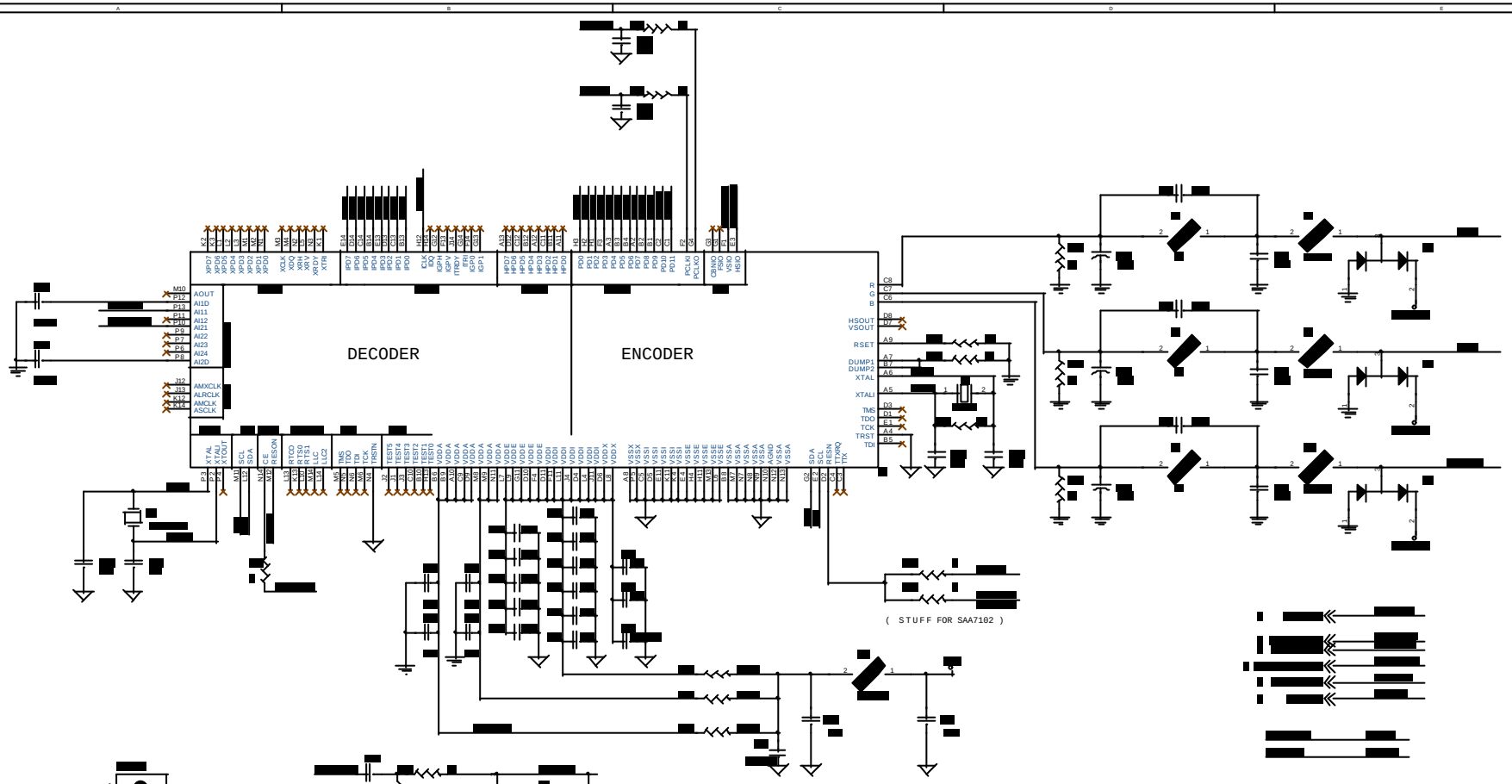
Size: B	Document Number: ROM VIP & VIDEO IF	Rev: 1.0
Date: Tuesday, July 17, 2001	Sheet 12 of 14	



1.EXTAL,EXTALI,DXTAL AND DXTALI
NETS SHOULD BE 10 mils width.

R98 and R99 closer to J1

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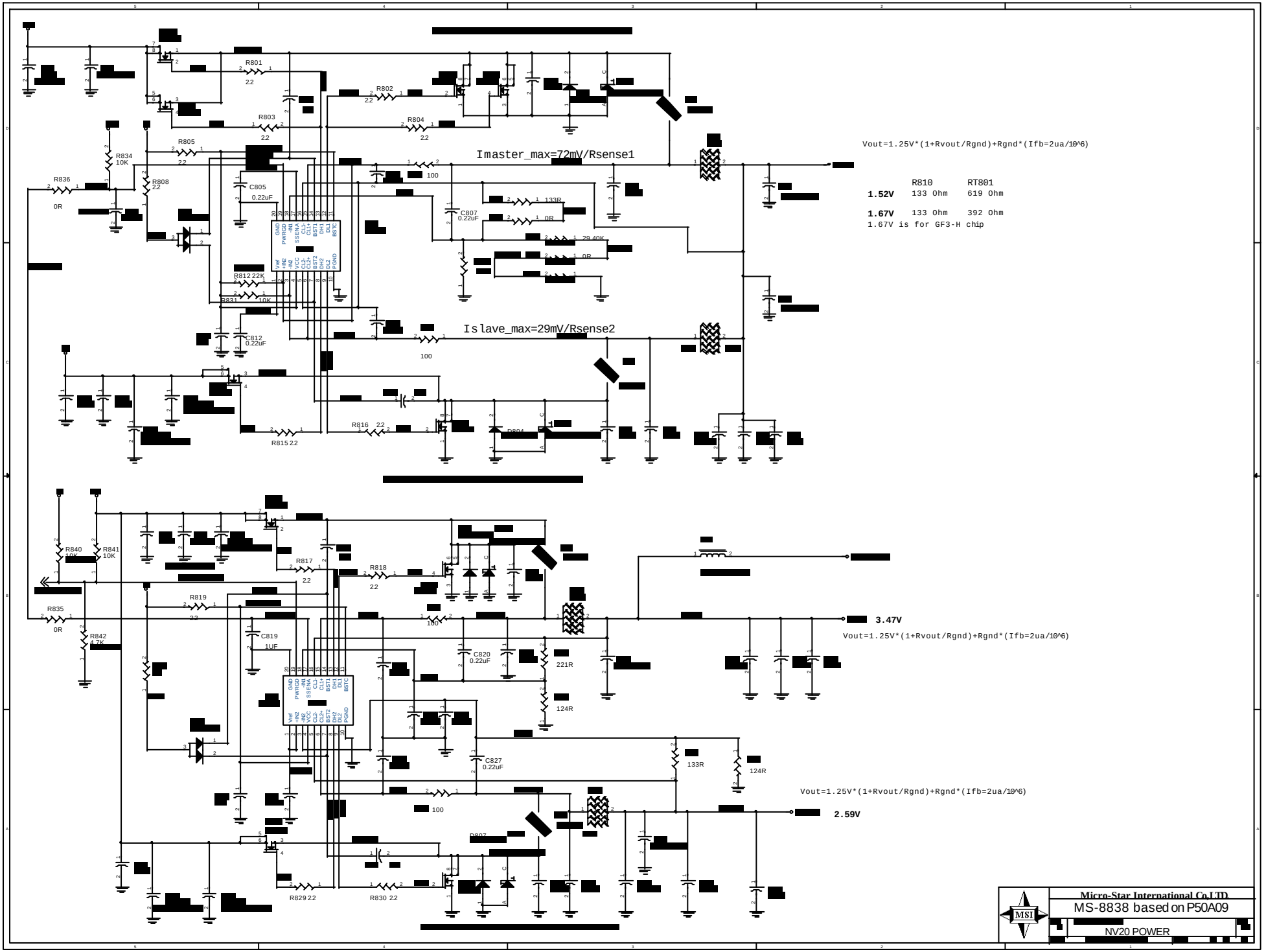
VIDEO CODEC



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NV20 POWER