28-P152, DUAL DAC/TMDS, 128MB 4MX32 BGA DDR, VIVO, GOGGLES, AGP8X

28-P152: Based on P83-A02

Replaced NV25 with NV28.
Use AGP8X section, DVO and DVOB series terminations from P151.
Corrected GPU partition E (some power and gnd pins were missing.)
Removed DVO power regulators from P-ROM page.
Changed Serial Rom power pin to 3.3V
Removed parallel ROM and added SST45VF010 as an alternate.
Updated compensation circuit for SC2602.
Added HIP6012CB as an NVVDD alternate switcher to SC2602.
Added a PU on ROMCS and deleted PUs on WP and HOLD.
Rearragned PS sheets; they look too busy.
Added ISL6225 memory PS.
Added SST45VF strap support
Removed bypass resistors for CLC input rail filters (3.3V and 12V)
Added SC2672--ALT to ISL6225

Changes Made After Design Review:

Added PD on DVOBCLK_IN
Removed C14-C17--left over from P151.
Replaced 3 pin RGB integrated filters with 0603 inductors.
Added an X element near svideo.
Added PD on GPIO1 (for VGA SKU).
Fixed Power Good error:
- Renamed PWRGD_MEM & PWRGD_SC1102 to NVVDD_PWRGD.
- Renamed PWRGD_SC1175 to FB_PWRGD
Incorporated some feedbacks from PS Vendors (more to come):
- Deleted PU duplication (R1269)
- Merged PVCC and SC_BST to become SW12V
- Deleted D615.
-Removed SC2672.
-Used CAPS_SMD_7343H38_1812 in place of SMD_SANYO_CAP footprint for C1662, C1645 and C1653.
-Corrected L814 symbol error.
- Added RGB stub breaker resistors near long VGA filters.
- Added 0.22uF 0603 pkg to AGPVREFCG, tracking NV18 bringup.
-Deleted C1617 and C1618--no room.
-Changed C1622 to 0603 pkg.
-Isolated Gate drive Resistors (R1032, R1033) to the FET--Each chip has its own gate drive resistors for better routing.
-Added ISL6525 as an alternate to HIP6012. There are only 2 pins different.

Second Design Review:

1-Removed mutichip straps STRAP_MULTICHIP_AGP_DEV--Deleted R982 and R983
2-Removed mutichip straps STRAP_MULTICHIP_IO_DEV--Deleted R984 and R985
3-Consolidated 1uF caps: Changed C22, C23, C706, C1242 and C1639 to 0603 (from 0805).
4-Consolidated 33R resistors: Changed R1000, R1107 and R1108 to 0402 pkg (from 0603).
5-Provided the ability to disable AGP PWR GOOD: Added 0R R1306.
6-Clamped GPIO1 to 3.3V: Changed FCCDDCPWRVGA on D611.2 and D600.2 to 3.3VD1
7-Removed PU R1294 from Serial ROM WP pin and connected to 3.3V directly.
8-Set RAM_CFG to 0100b for 4Mx32 DDR DQS per byte.
9-Merged CAPS_SMD_7343H38_1812 with CAPS_SMD_8_0-10_0_SANYO to become caps_smd_ale-d80d100_D7343_1812 footprint (C1658, C1263 and C1268 don't need to support 1812). This change would allow us to use ceramic caps for NVVDD, FBVDD and VTT rails.
10-Changed NVVDD_PWGD inverting input to the comparator to be referenced at 1.3V from 12V rail (moved R1268.1 to 12V).
11-Merged netname FBVDDQ with FBVDD to become FBVDD. Historically we connected these 2 nets together and Orcad chose FBVDD.

"FAB STOP" CHANGES TO TRACK P151 Bringup:

1- Corrected Q901 PCB Footprint.
2- Changed AGPCALPD pullup resistors to VDDQ for pad calibration to 56.2R 1%.
3- Changed AGPCALPU pulldown resistors to GND for pad calibration to 49.9R 1%.

Revision A01:

1- Added AGP VREFCG Circuit.
2- Added common mode chokes on RGB signals for both DACs.
3- Updated AGP Constraints based on NV28 pkg measurement.
4- Made Common Mode filters available to long VGA.

Revision A02:

1- Added circuit to fix AGP current violation.

CHANGES AFTER X-RELEASE:

ECO6753: Populate R1348 (was NO_STUFF)
ECO6784: Adjusted RSET Values: R927=105R; R207=110R
ECO6989: Incorporated changes to pass EMI prescan.
Updated various properties and added some more notes.
ECO7119: Incorporated changes to pass EMI final scan.

ECO7152: P-RELEASE.

ECO7284: Corrected PN discrepancies (R1310, C1680-C1683, C1677-C1679).

COMMON -- ALL
NO_STUFF - NOT STUFFED
PRI_VGA - Primary VGA Support
PRI_DVI - Primary DVI-D (Digital) Support
PRI_DVI_I - Primary DVI-I - (Digital & Analog) Support
SEC_DVI_I - Secondary DVI-I (Digital & Analog) Support
PRI_PROT - Primary DVI-VGA protection diodes.
SEC_PROT - Secondary DVI-I protection diodes
MEM128 - 128MB EXTENDED MEMORY

STEREO - USED FOR STEREO GOGGLES
STEREOSYNC1 - USED FOR STEREO GOGGLES
STEREOSYNC2 - USED FOR STEREO GOGGLES
STEREOSYNCS - USED FOR STEREO SYNC BUFFERS
SAA8 - PHILIPS ENCODER/DECODER SAA7108
SAA2 - PHILIPS ENCODER SAA7102
CX - CONEXENT ENCODER CX25871

PS Switchers:

SC1565 - USED TO REGULATE 3.3VL FROM 3.3V - LINEAR
ISL6225 - USED TO REGULATE FBVDD and VTT from 12V.
SC1102/ISL6525CB - USED TO REGULATE NVVDD FROM 3.3V - SWITCHER

VGA-TV-DVI - Used for Primary VGA / TV / Secondary DVI
VGA-DVI - Used for Primary VGA / Secodary DVI only
VGA-TV - Used for Primary VGA / TV
VGA - Used for Primary VGA only
DVI-TV-DVI - Used for Primary DVI / TV / Secondary DVI
DVI-DVI - Used for Primary DVI / Secondary DVI Only
DVI-TV - Used for Primary DVI / TV
DVI - Used for Secondary DVI
PASSIVE_HS - Used for Passive heat sink
FAN_HS - Used for Fan heat Sink
SOCKET - PARTS REMOVED WHEN USING A SOCKET

0. TOP PAGE

140-10152-0000-A02
602-10152-0000-A02

NV28, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

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NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

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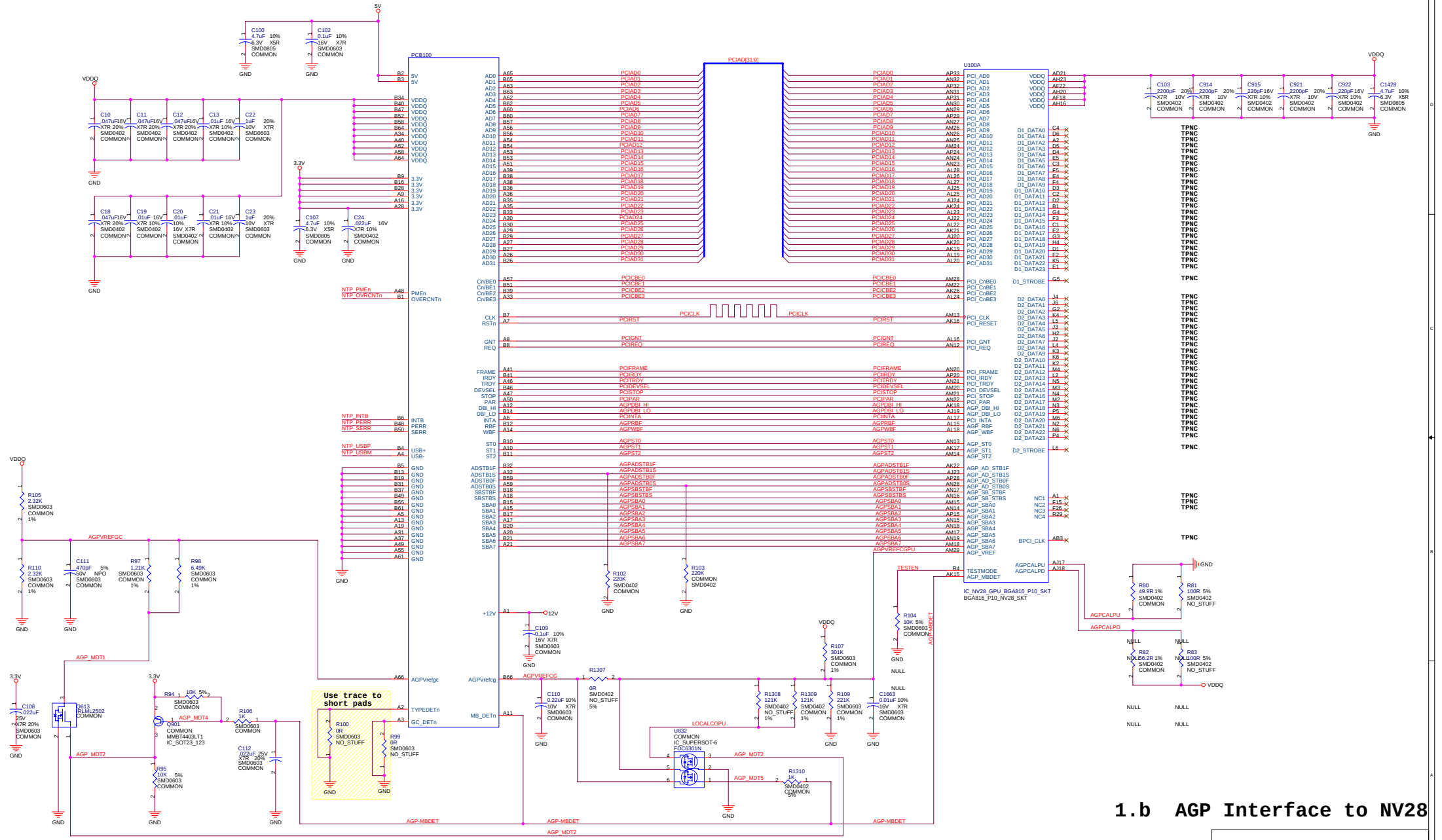
Saturday, December 07, 2002

Scale

Sheet 1 of 23



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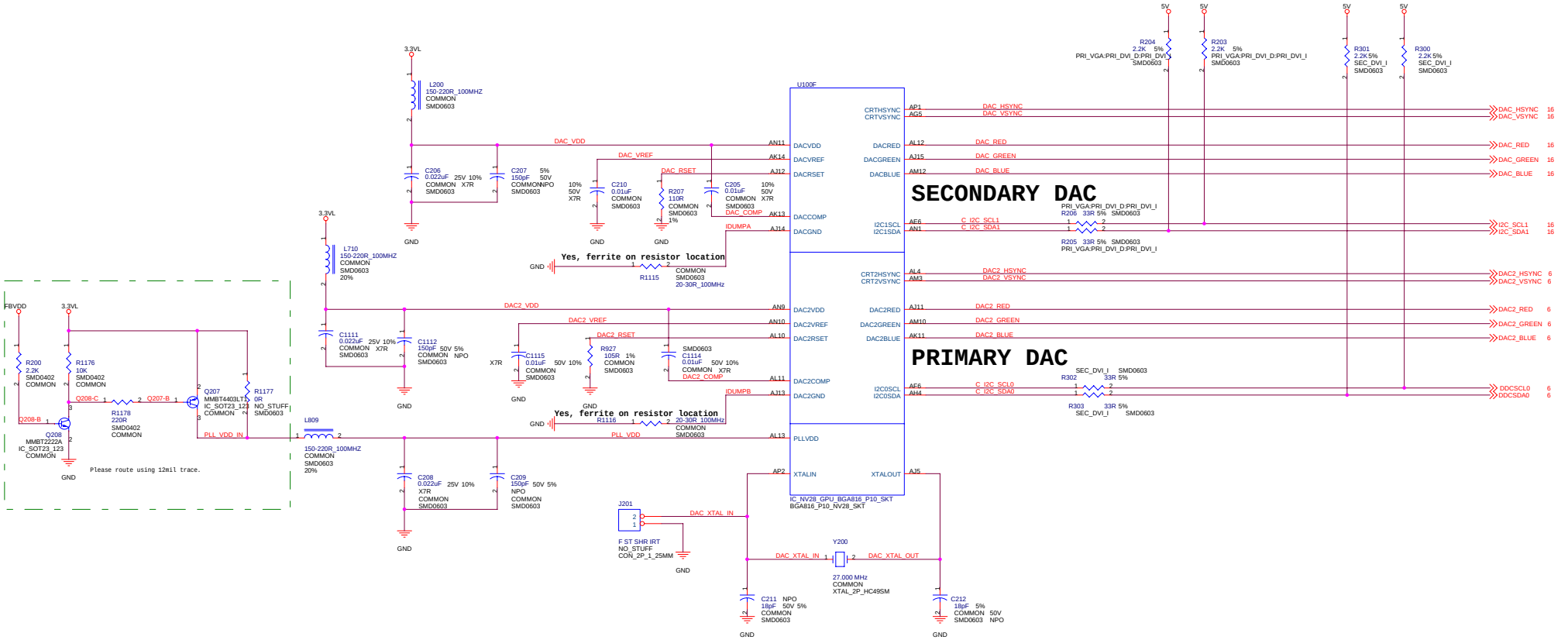

2.2 NV DAC/PLL/I2C

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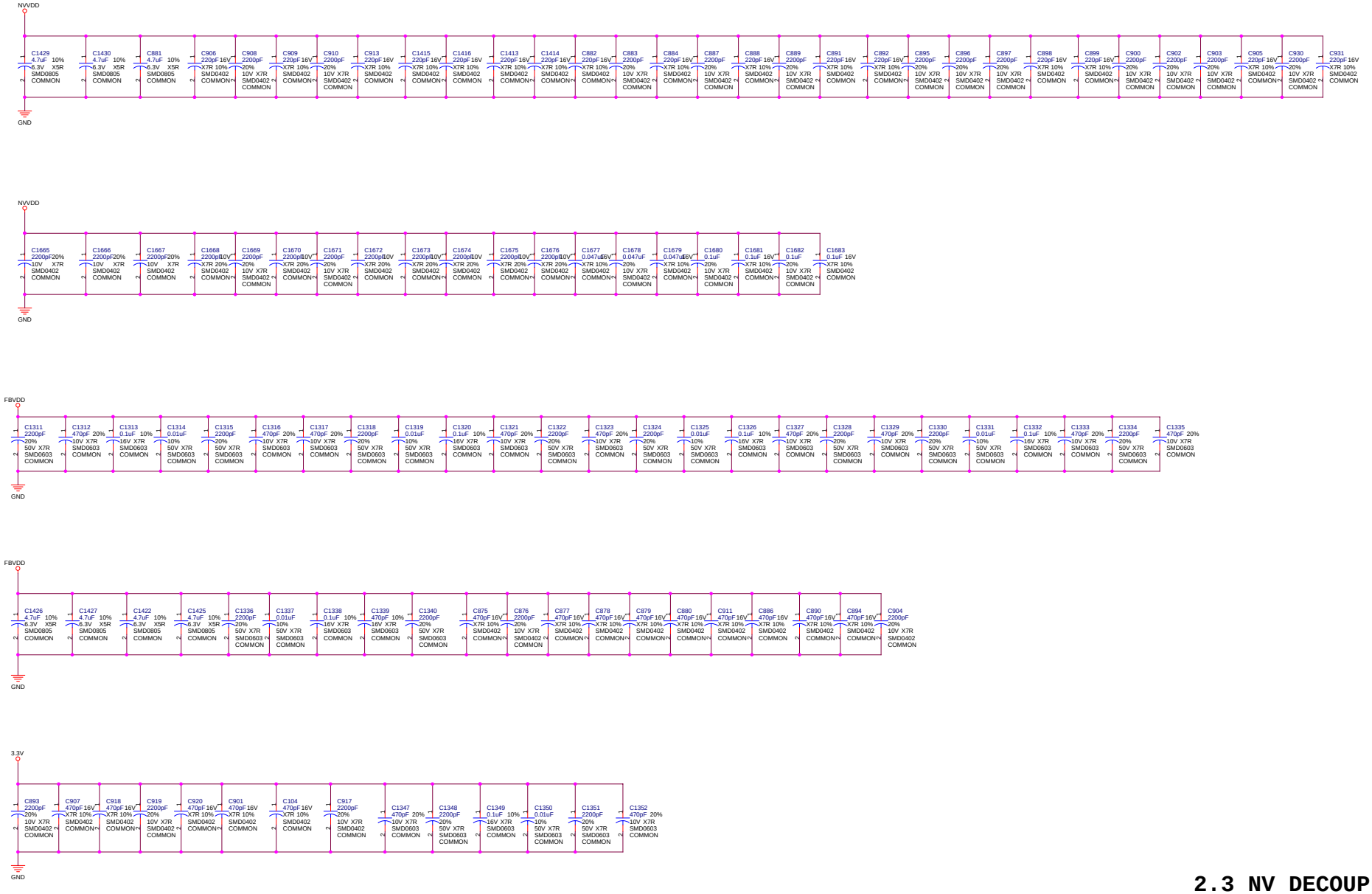
Date:	Saturday, December 07, 2002
Sheet	3 of 23



2.3 NV DECOUPLING

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Title	MS-8905-00A	
Size: Custom	Document Number: <Doc>	Rev: <RevCode>
Date: Saturday, December 07, 2002	Sheet 4 of 23	

STRAP_MULTICHIP_AGP_DEV

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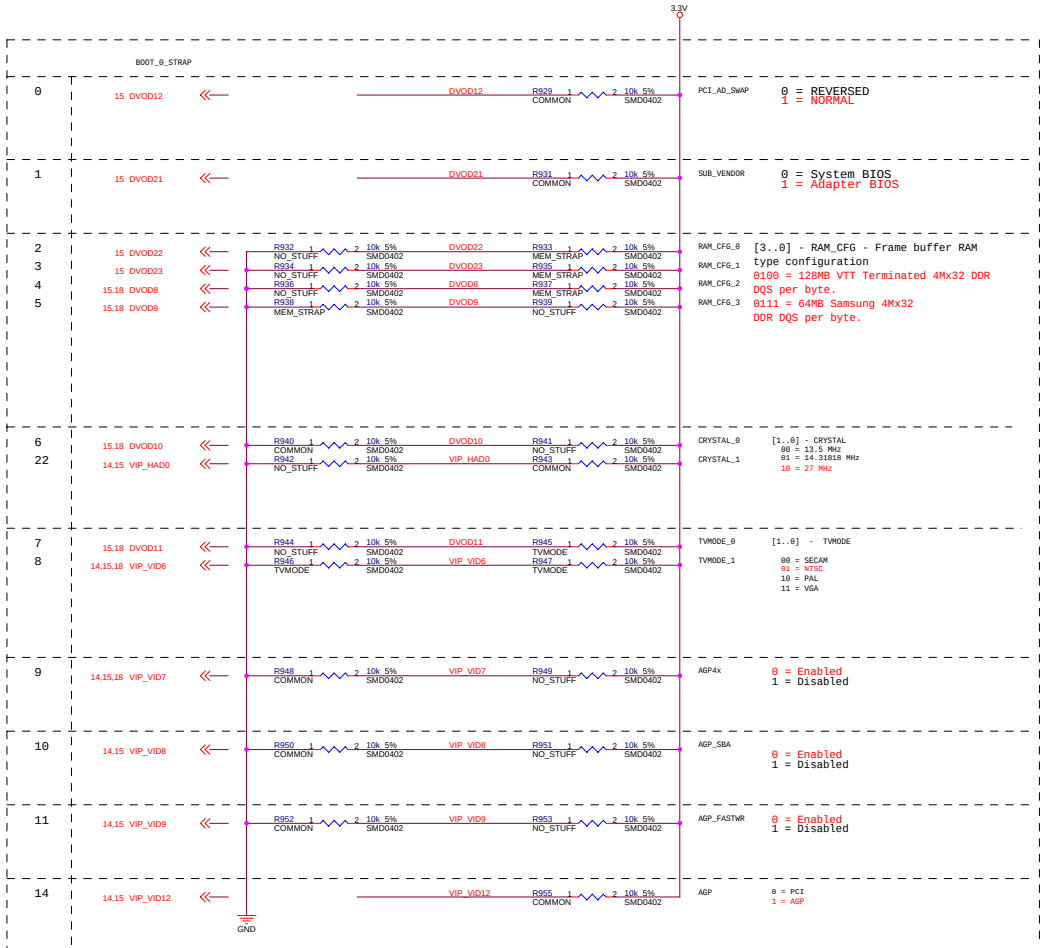
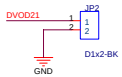
15 DVOBD[23:0] DVOBD[23:0]
14,15,18 VIP_VID[15:0] VIP_VID[15:0]





3.0 NV STRAP

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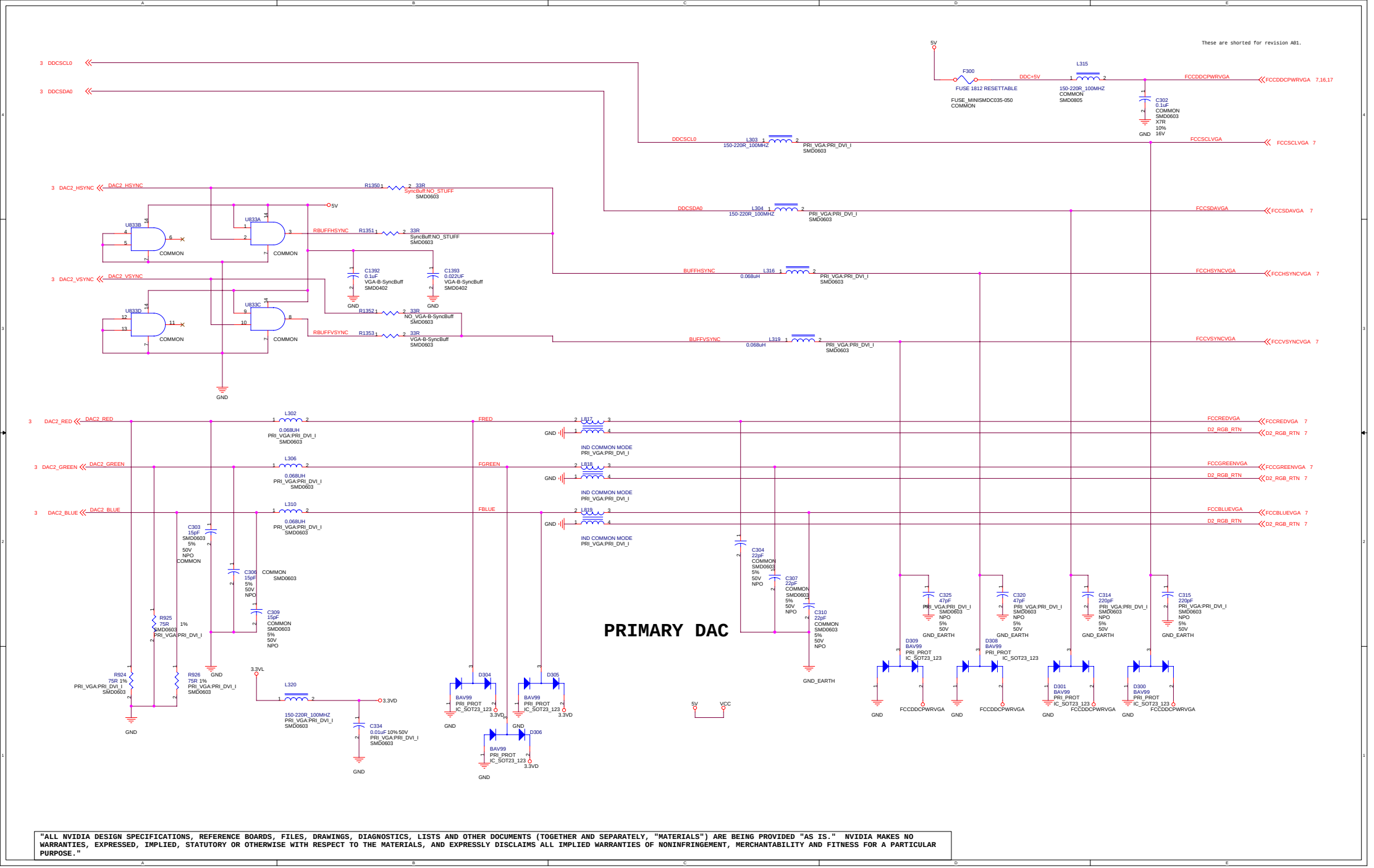
Date:	Saturday, December 07, 2002	Sheet 5 of 23



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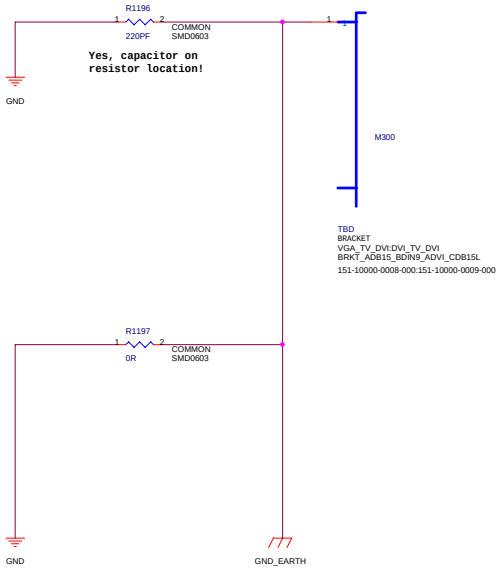
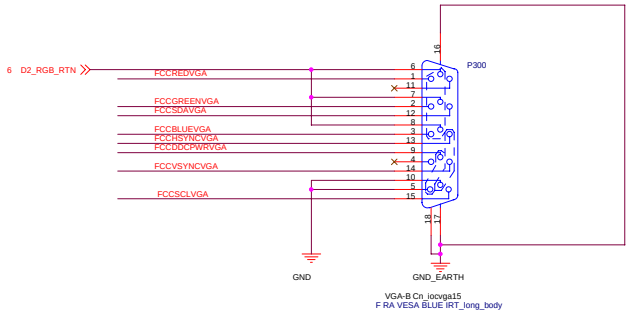
3.1 DACB-I2C0--Pri

Components to connect
digital and chassis GND.



VGA-TV-DVI - Used for Primary VGA / TV / Secondary DVI

DVI-TV-DVI - Used for Primary DVI / TV / Secondary DVI



PRIMARY DAC-LONG VGA

THIS CONNECTOR IS
PLACED ON THE NORTH
SIDE OF THE BOARD

3.2 VGA CON, BRACKET

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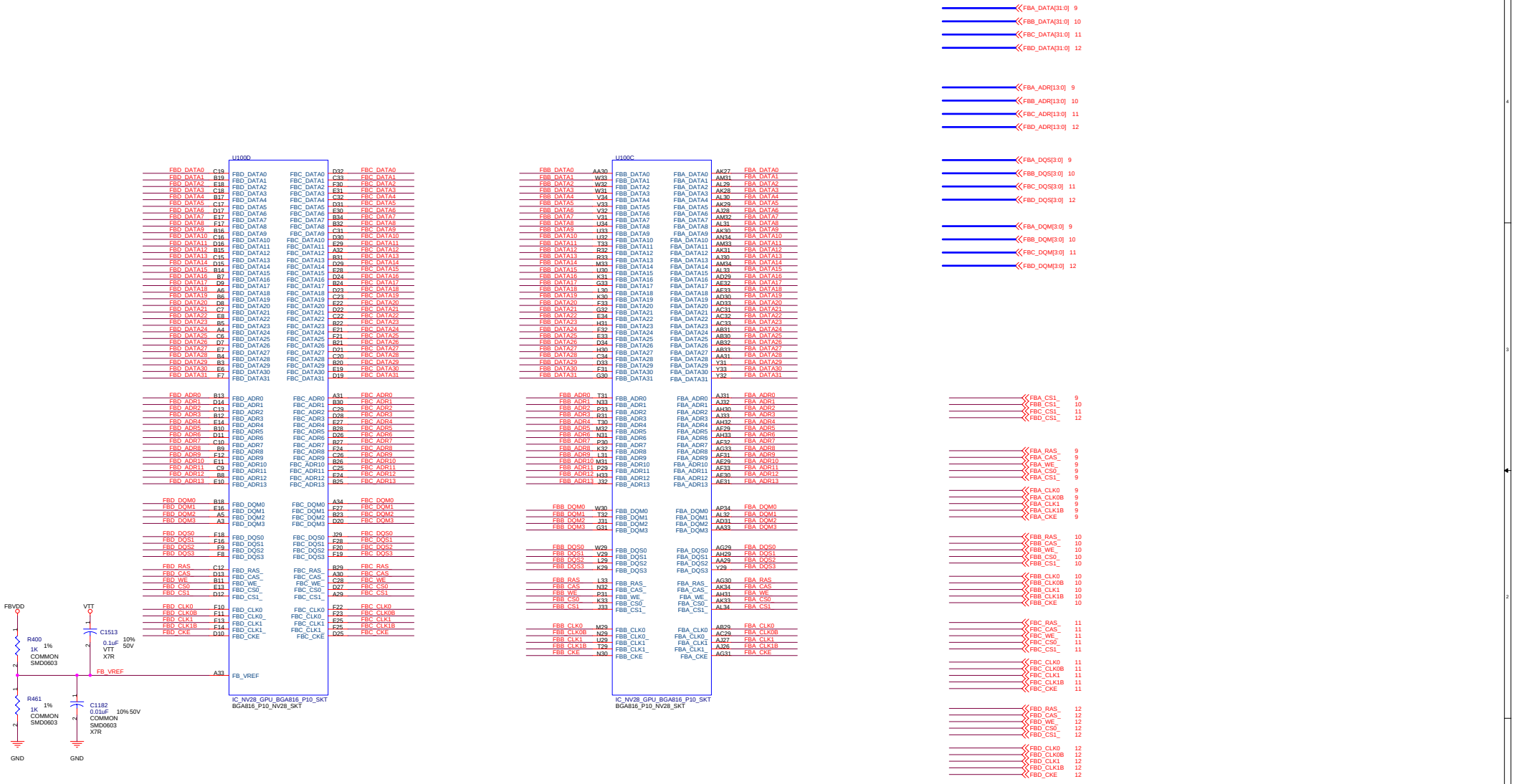
Date: Saturday, December 07, 2002	Sheet 7 of 23	



4.1 NV FBA/B/C/D

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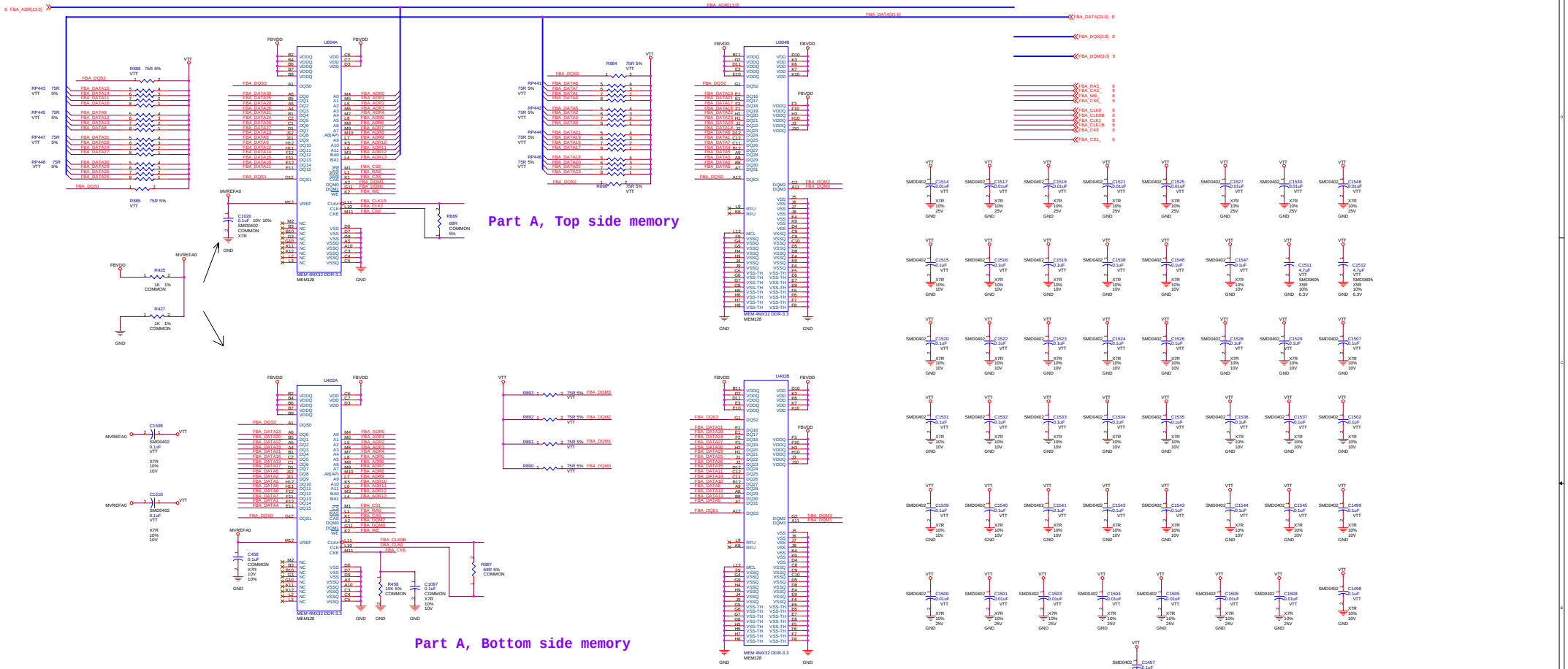
Date:	Saturday, December 07, 2002
Sheet	8 of 23



4.2 FBA DDR 4MX32 SDRAM

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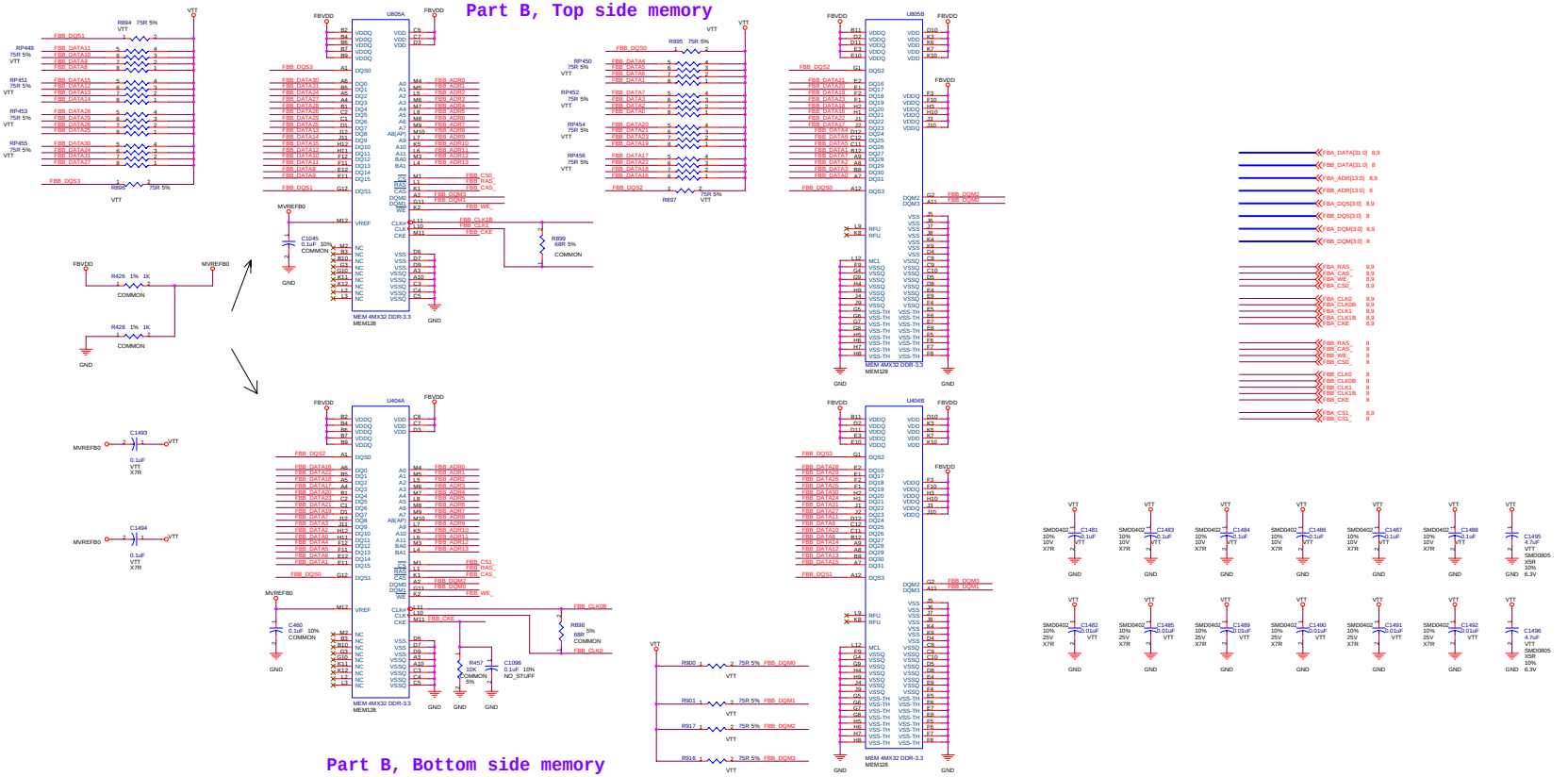

4.3 FBB DDR 4MX32 SDRAM

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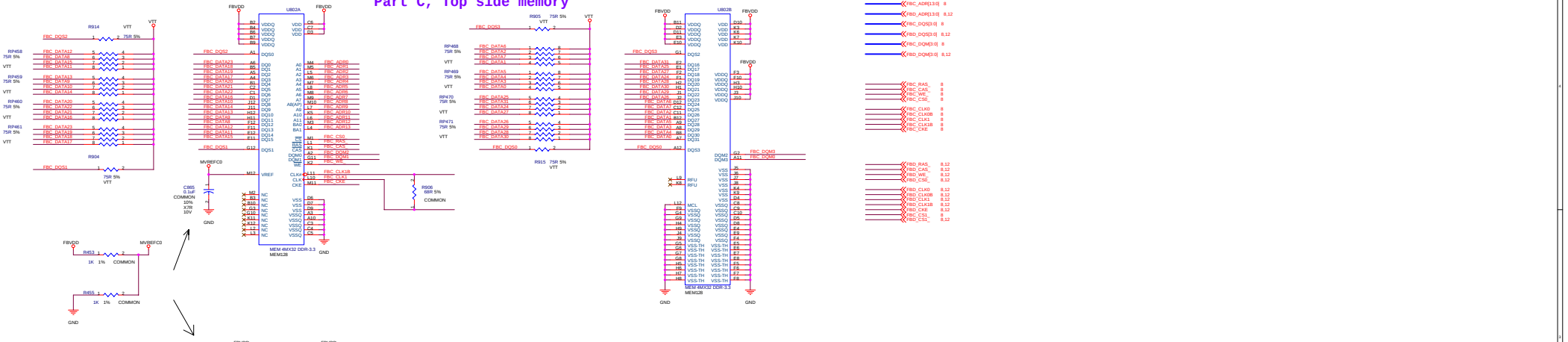
Date: Saturday, December 07, 2002	Sheet 19 of 23		

Part C, Top side memory



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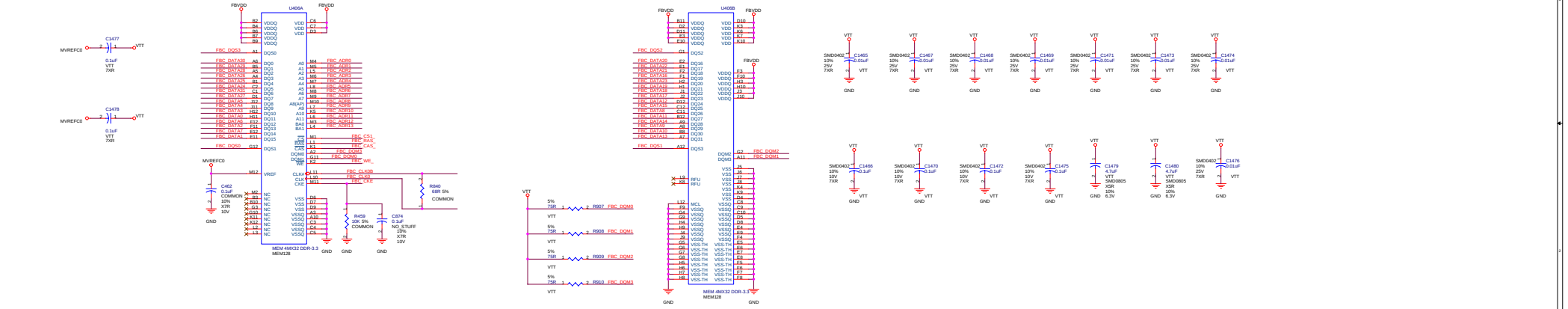

4.4 FBC DDR 4MX32 SDRAM

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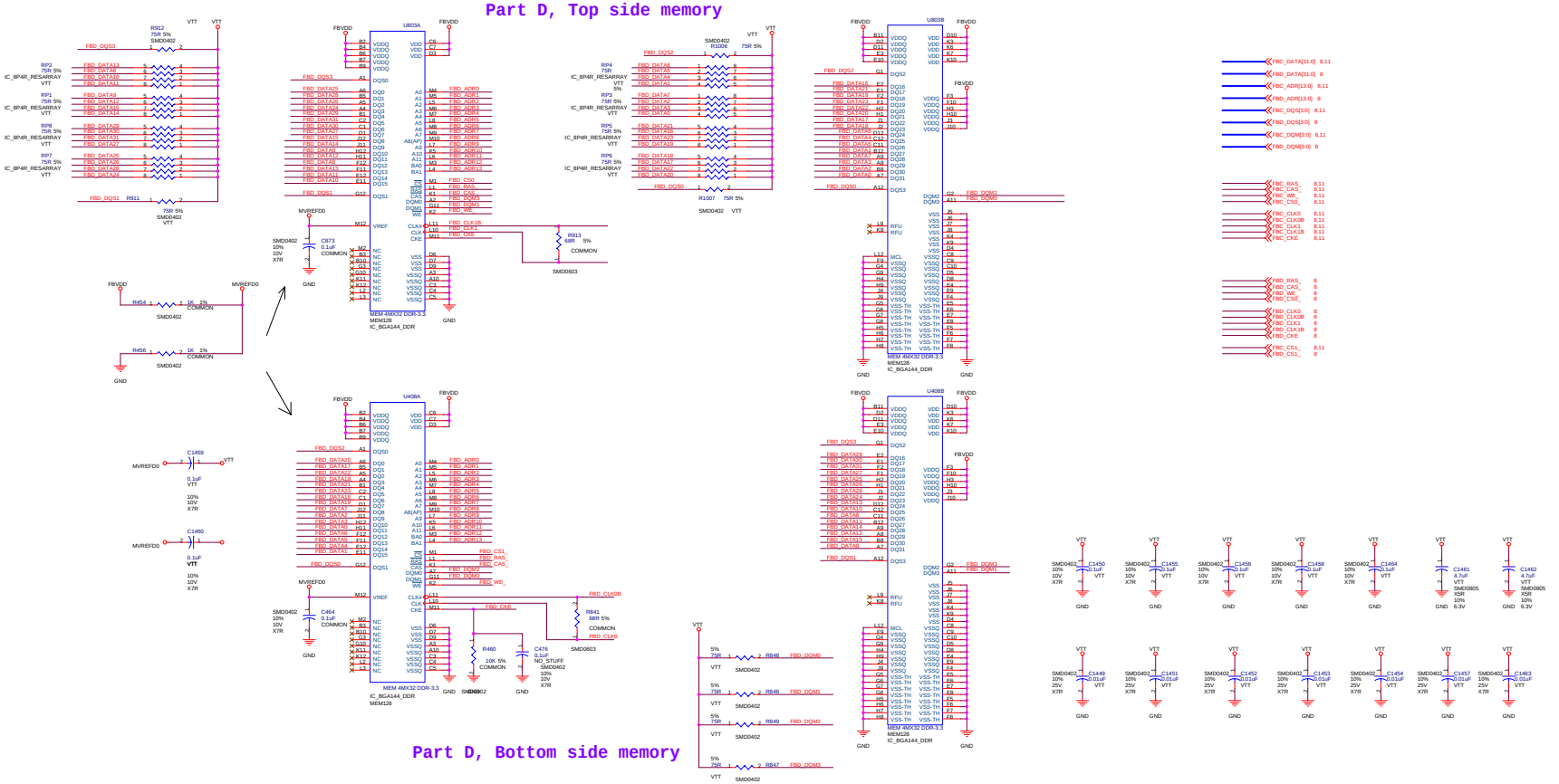
Date: Saturday, December 07, 2002	Sheet 11 of 23		



4.5 FBD DDR 4MX32 SDRAM

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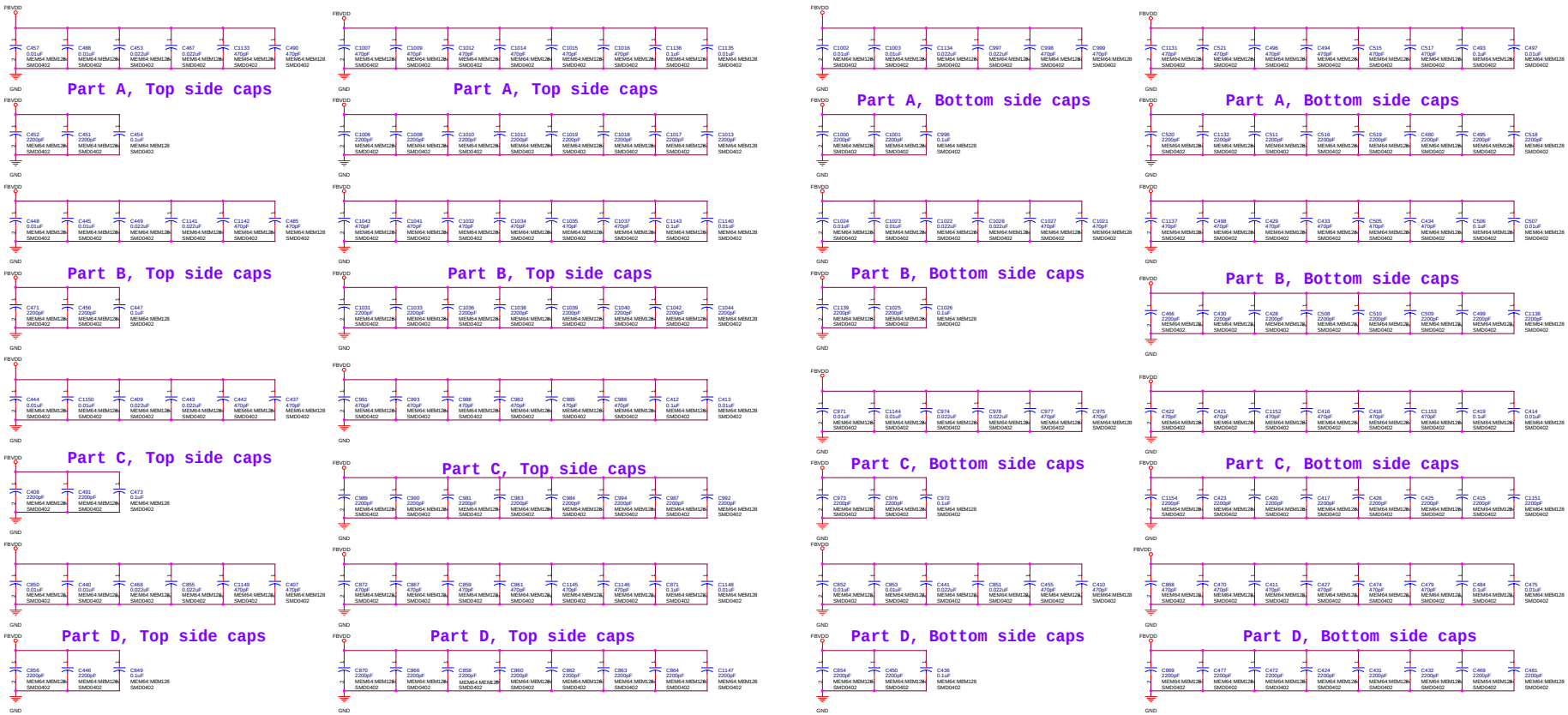

4.6 BGA MEMORY DECOUPLING

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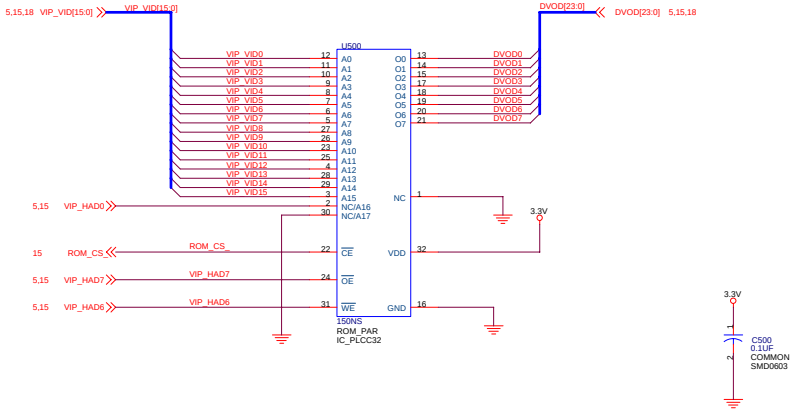

5.2 S-ROM

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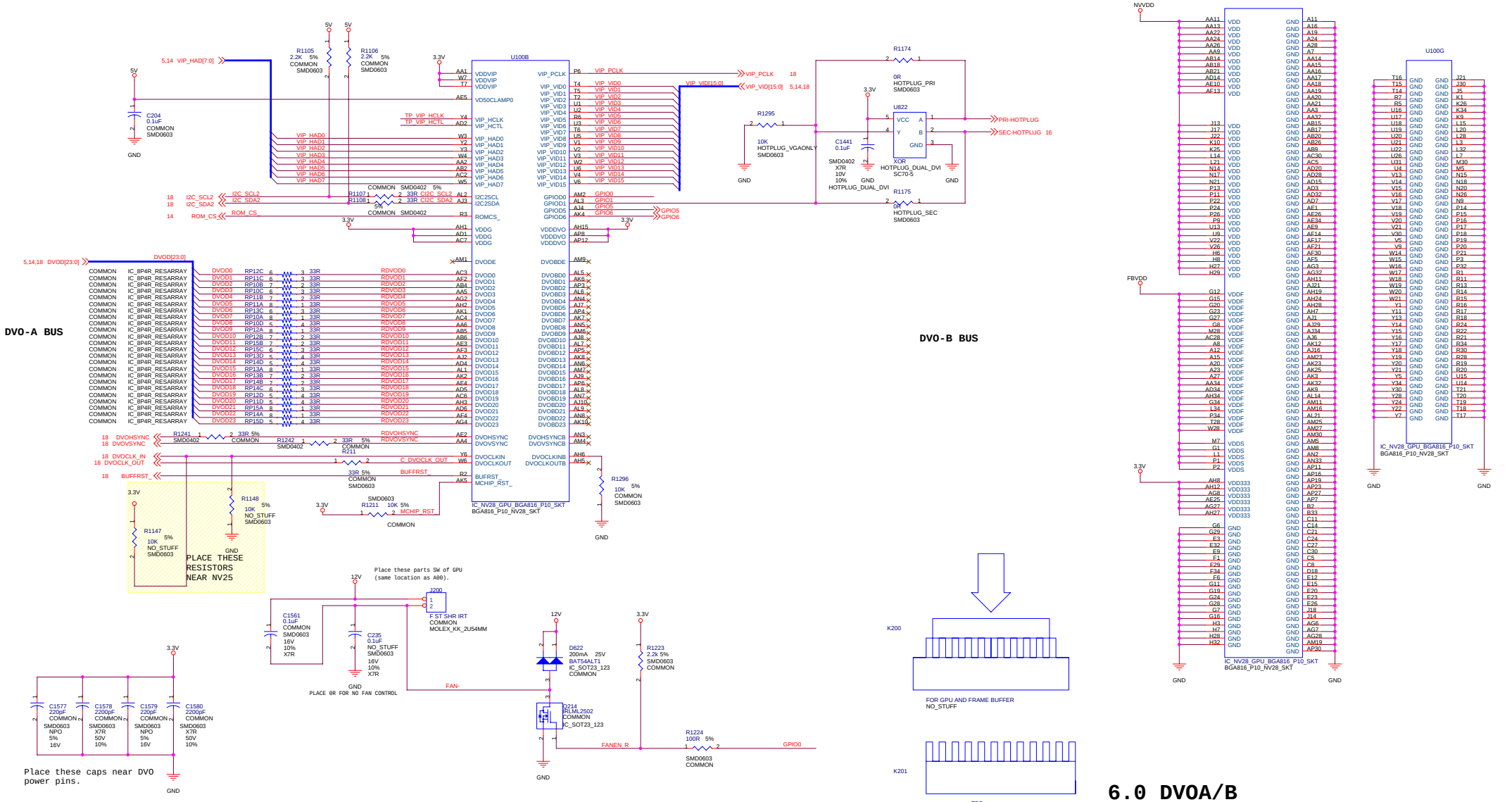

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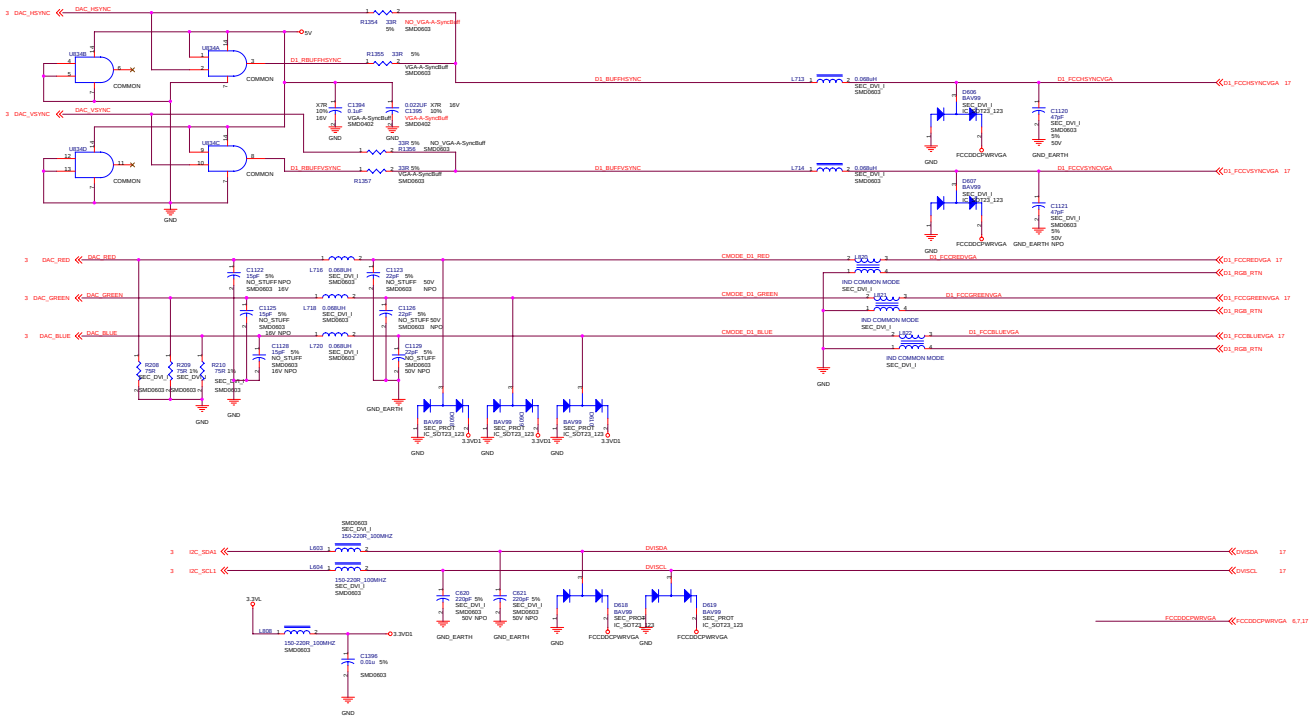
Sheet	15 of 23



SECONDARY DAC

6.4 DVOB/DACA I/O SEC

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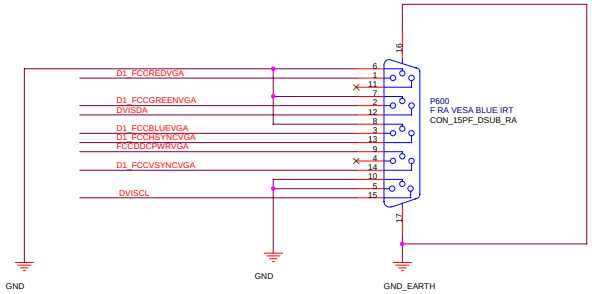
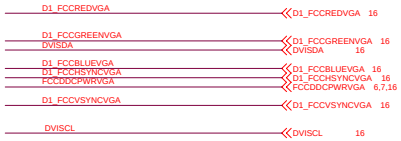
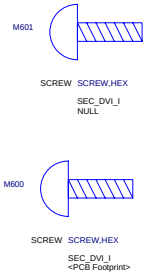


SECONDARY DAC





6.5 DVOB/DACA CONNECTOR

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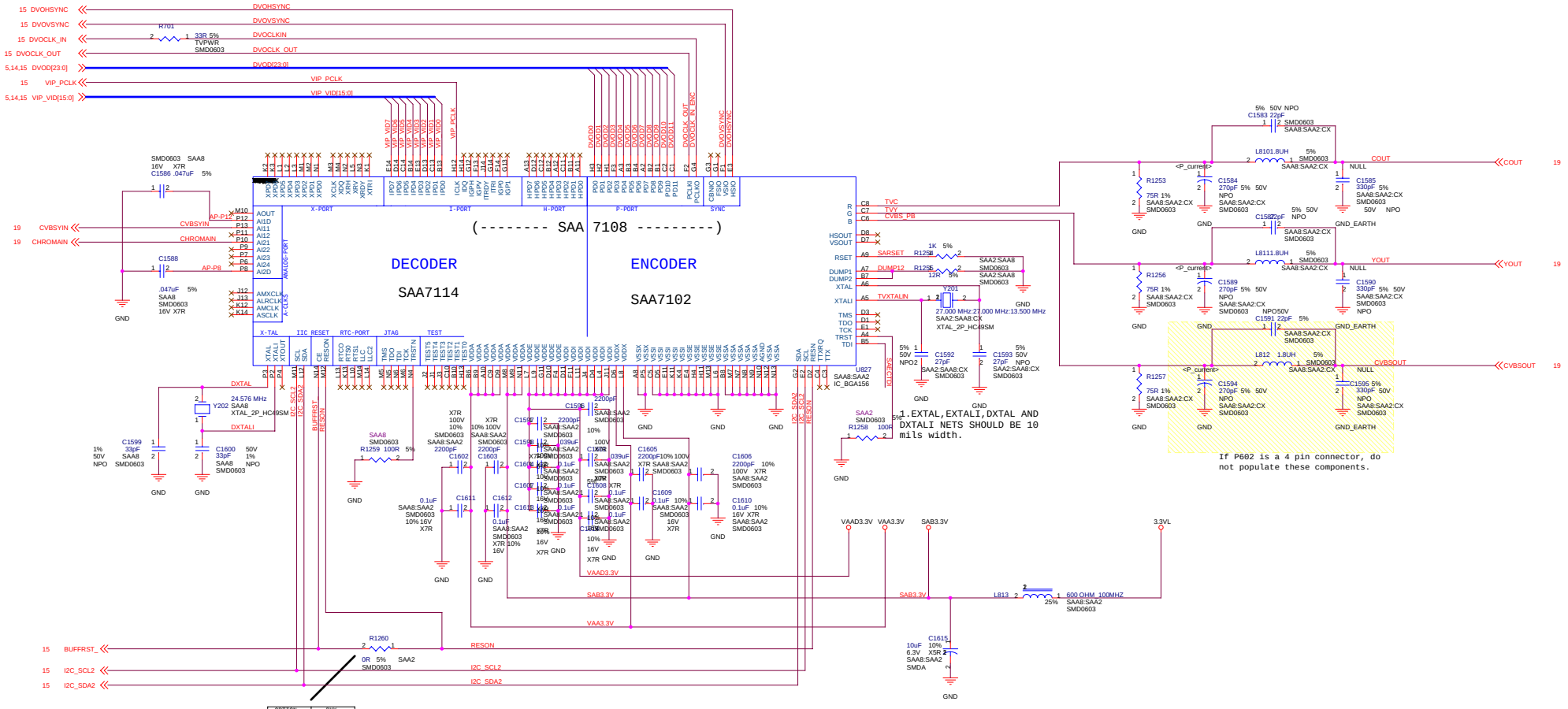
Date: Saturday, December 07, 2002	Sheet 17 of 23	



7.2 TV-PH CODEC

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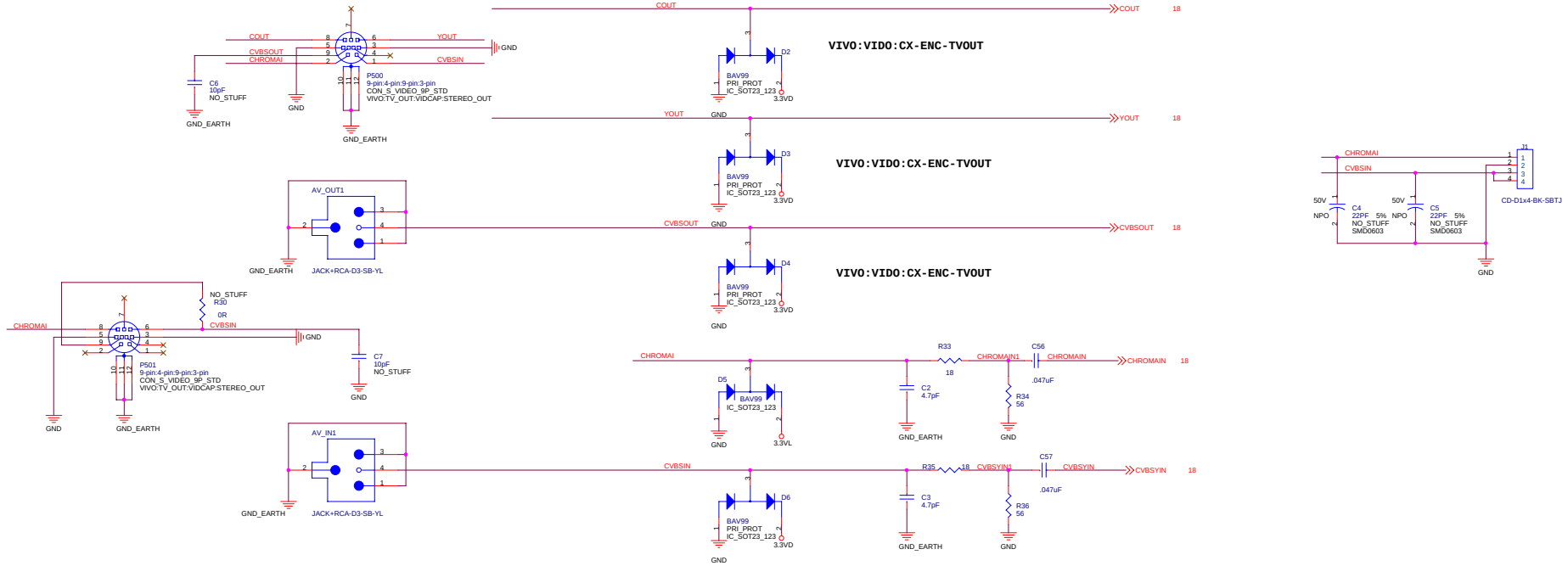
Rev	<RevCode>
Date:	Saturday, December 07, 2002
Sheet	18 of 23



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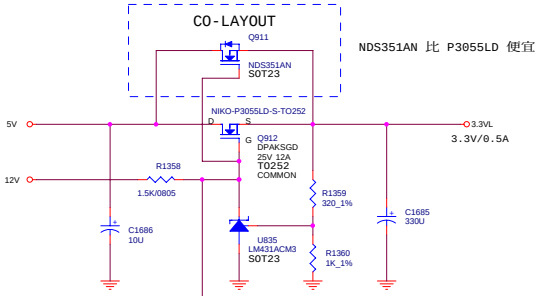
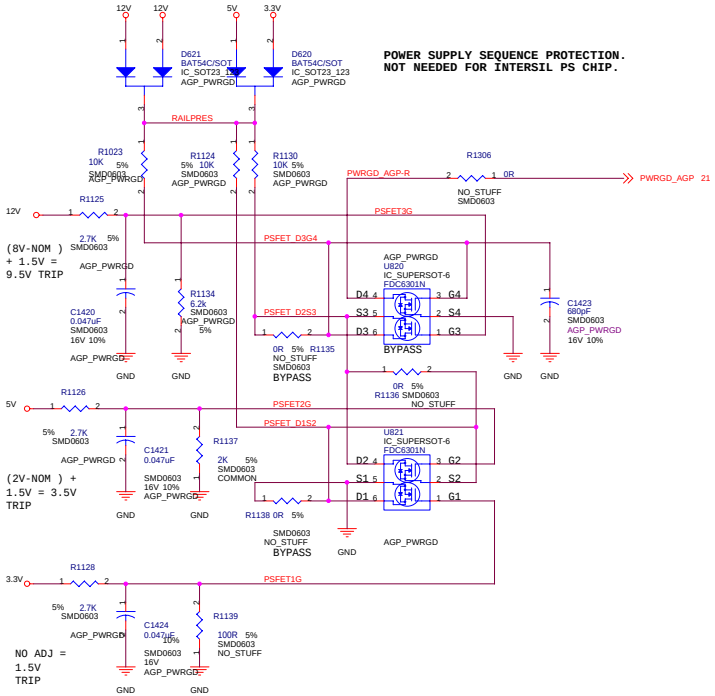
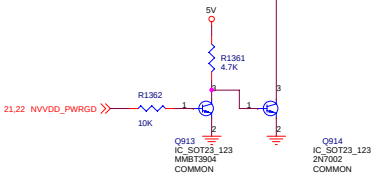
Size	Document Number Custom<Doc>		Rev <RevCode>
Date:	Saturday, December 07, 2002	Sheet 19 of 23	

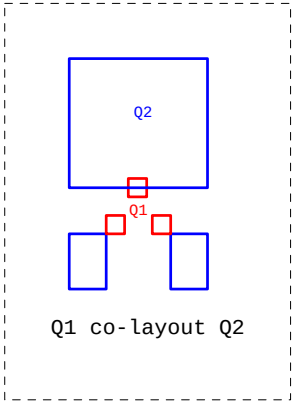
Regulated 3.3V

5V TO 3.3V/0.5A POWER CKT









5.a Power Sequence / 3.3VL Pwr.

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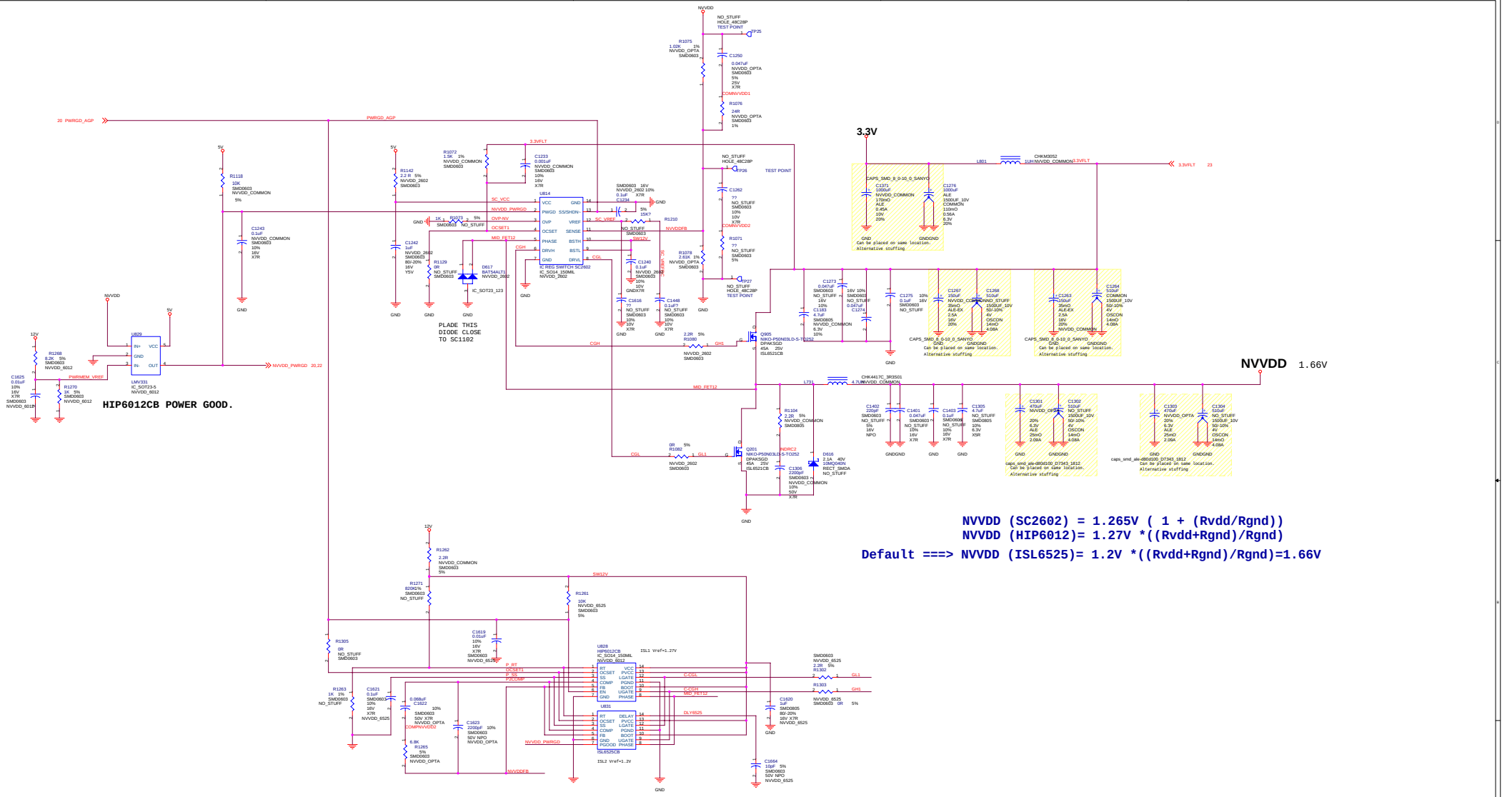
Size	Document Number	Rev
Custom	<Doc>	<RevCode>
Date: Saturday, December 07, 2002	Sheet 20 of 23	



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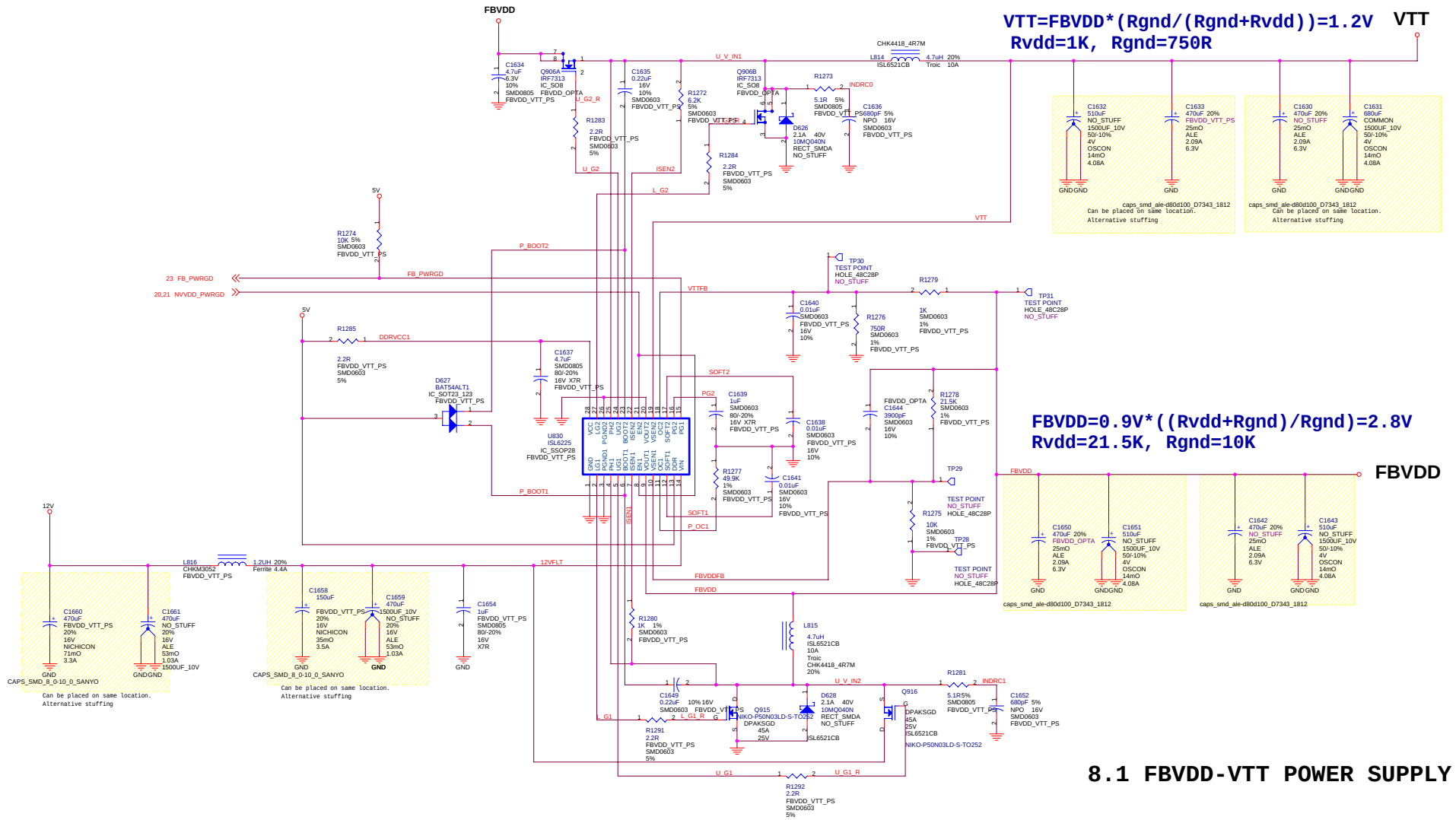
Size D	Document Number <Doc>		Rev <RevCode>
Date: Saturday, December 07, 2002	Sheet 21 of 23		



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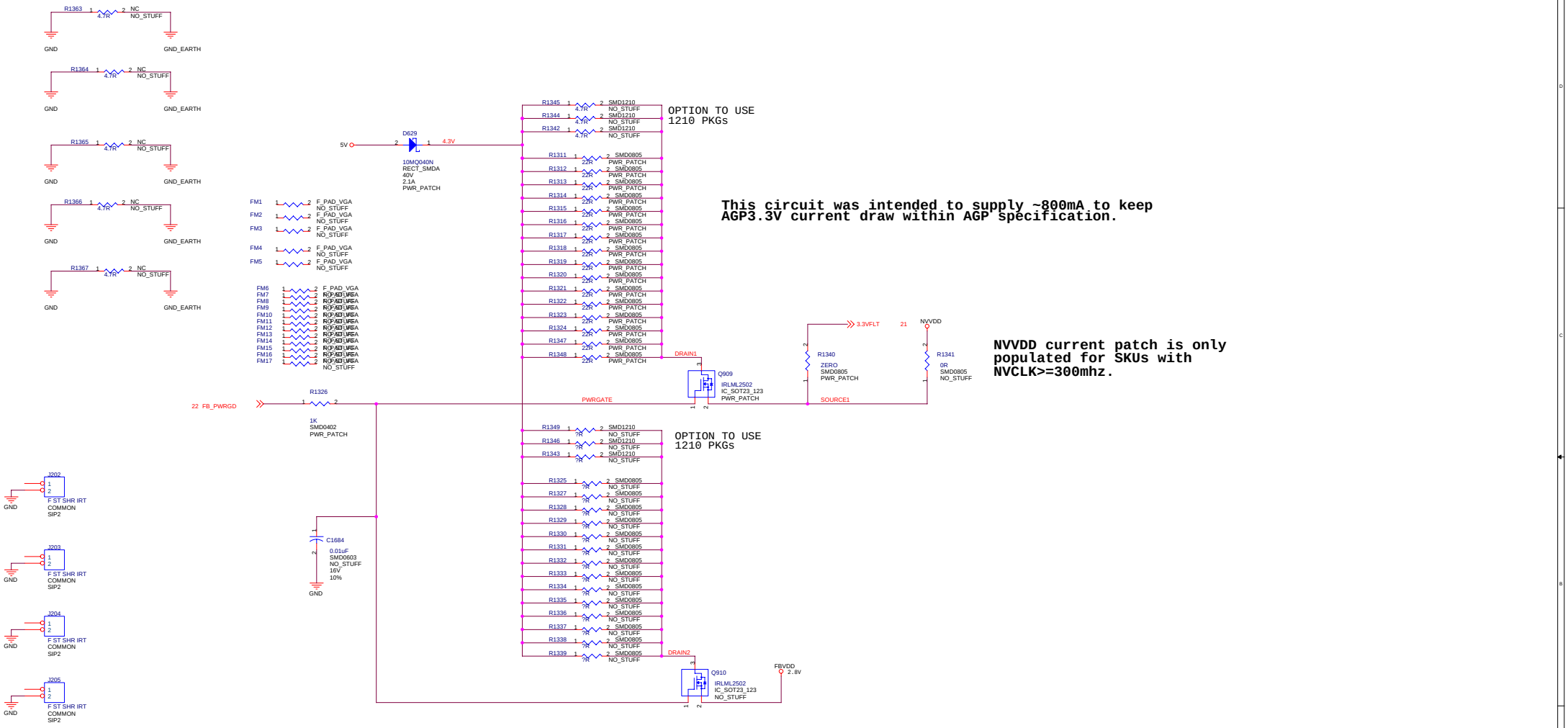
Title: MS-8905-00A
Size: Custom | Document Number: <Doc> | Rev: <RevCode>
Date: Saturday, December 07, 2002 | Sheet 22 of 23



8.4 CURRENT PATCH

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Title	MS-8905-00A	
Size: Custom	Document Number: <Doc>	Rev: <RevCode>
Date: Saturday, December 07, 2002	Sheet 23 of 23	