P1071: GF108, 1024MB x16 DDR3, DVI+HDMI+VGA

V230-8.0

1.Base on V230-4.0 to modify
2.Page 4：Remove FBB and add TERMINATION OPTION FOR 8 LOAD CMD LINE
3.Page 5：Change to Memory 1st Bank 0..31
4.Page 6：Change to Memory 1st Bank 32..63
5.Page 7：Del som Memory Decoupling
6.Page 12：Co-lay Hi-C cap for GT440
7.Page 14：Change Fan control circuit

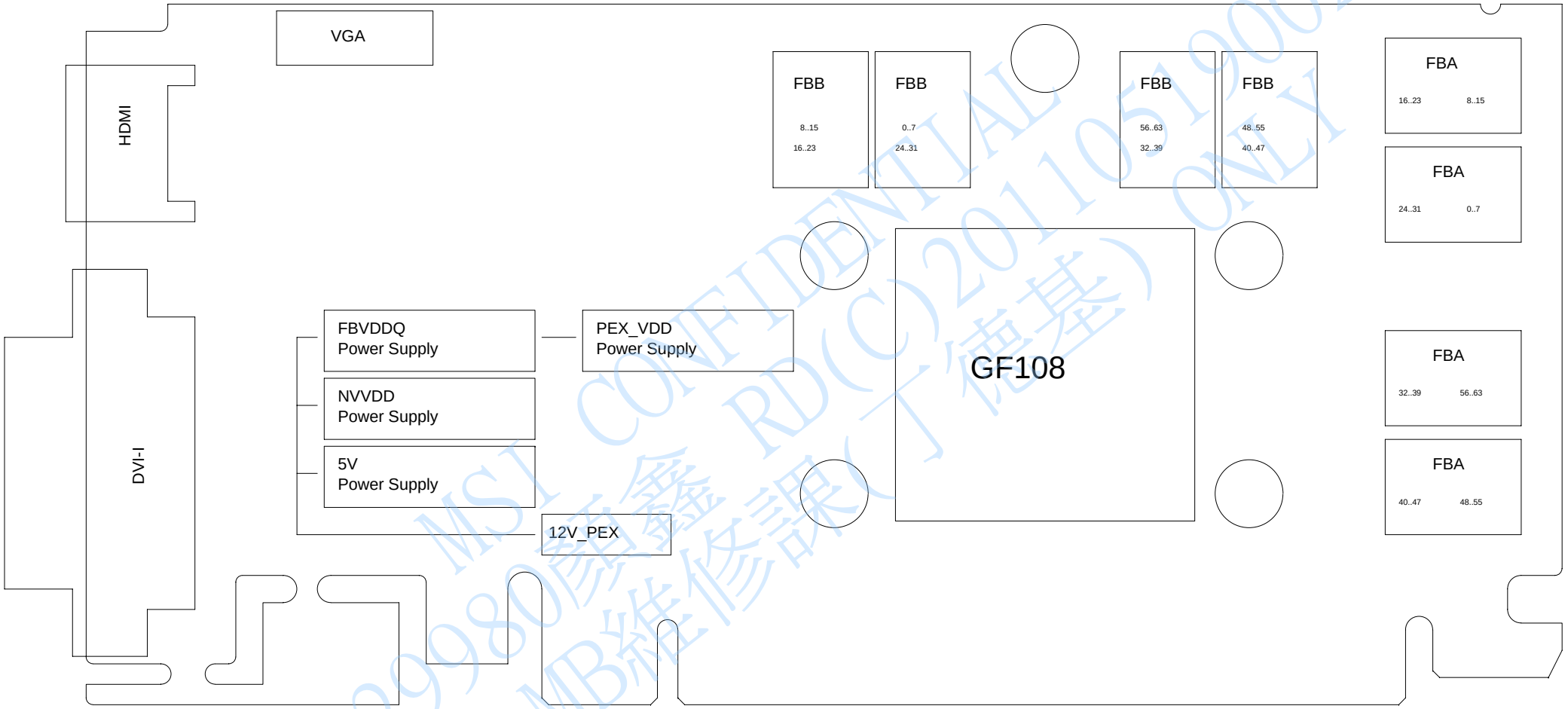
SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11071-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-11071-0001-100	GF108-300-A1 625/1250/900MHz 1024MB/128bit DDR3, DVI-DL+HDMI+VGA
2	SKU0002	600-11071-0002-100	GF108-200-A1 650/1300/900MHz 1024MB/128bit DDR3, DVI-DL+HDMI+VGA
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

MICRO-STAR INT'L CO.,LTD
MS-V230

Size: Custom | Document Description: Overview | Rev: 8.0

Date: Friday, April 08, 2011 | Sheet 1 of 20

Block Diagram



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V230	
Size: Custom	Document Description: Board Block Diagram	Rev: 8.0
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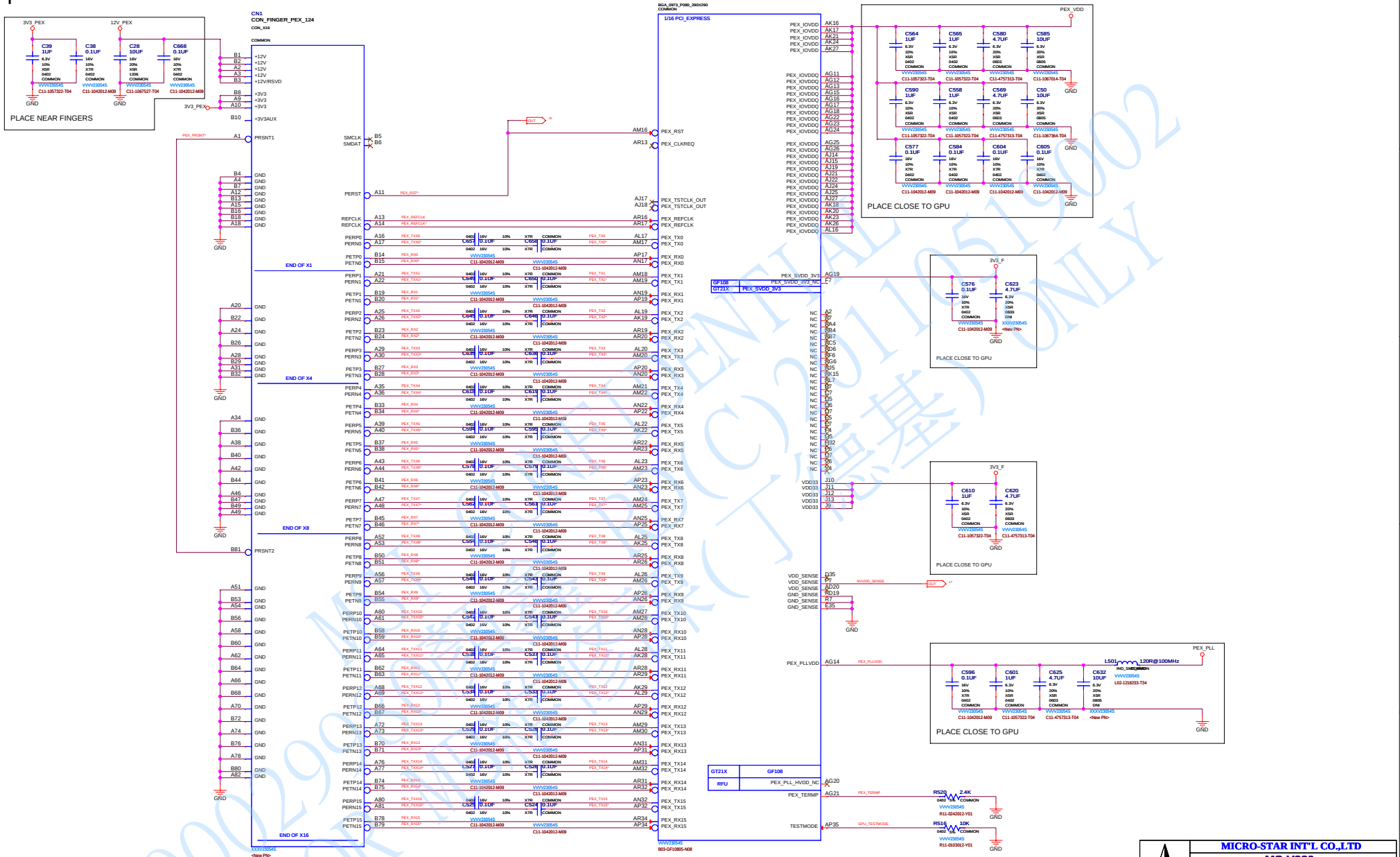
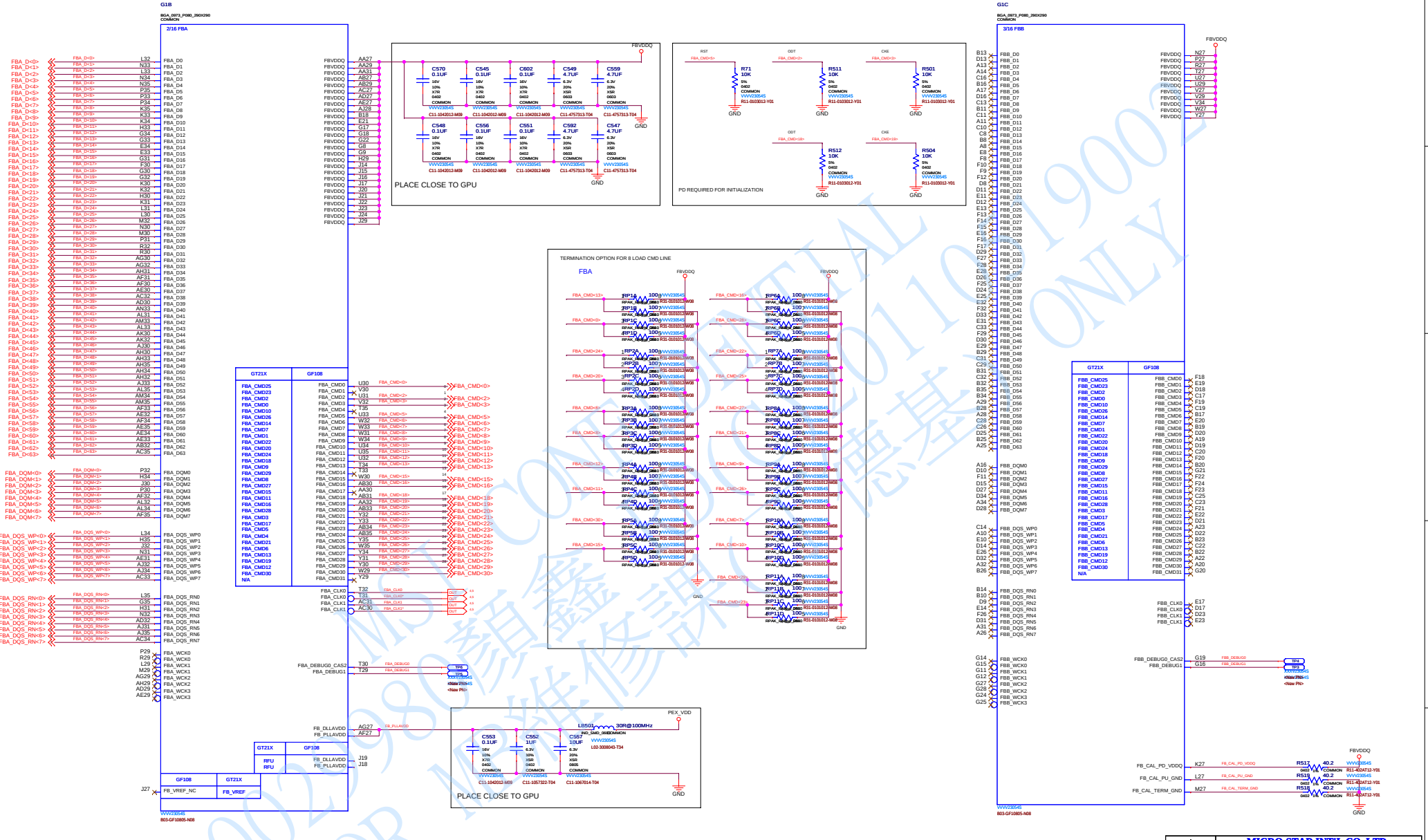
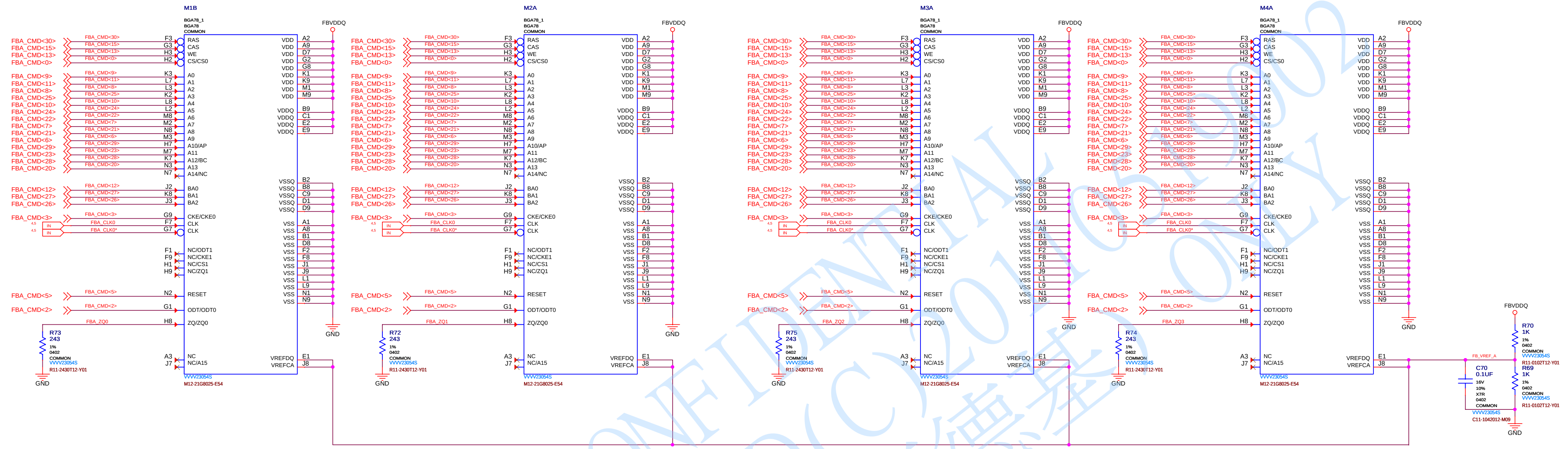
PCI Express Interface

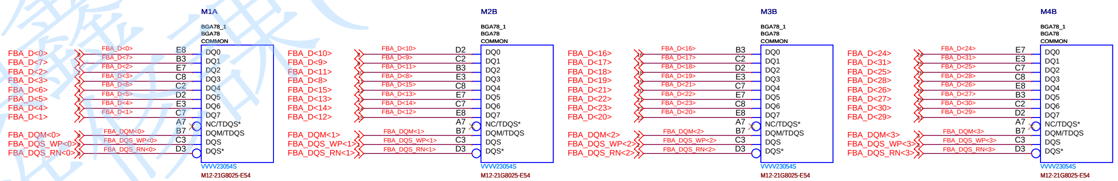


GPU Frame Buffer



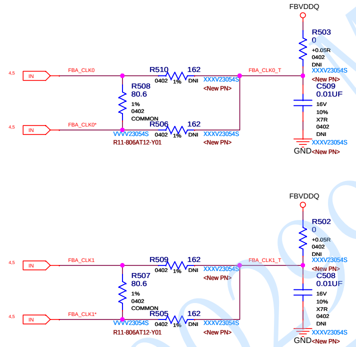
Memory 1st Bank 0..31





CMD Mapping

CMD	<0..31>	<32..63>
CMD0	CS0*	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4		
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14		
CMD15	CAS*	CAS*
CMD16		CS0*
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
CMD31		



CLK Termination

MICRO-STAR INT'L CO.,LTD

MS-V230

Size	Document Description	Rev
Custom	Memory 1st Bank 0..31	8.0

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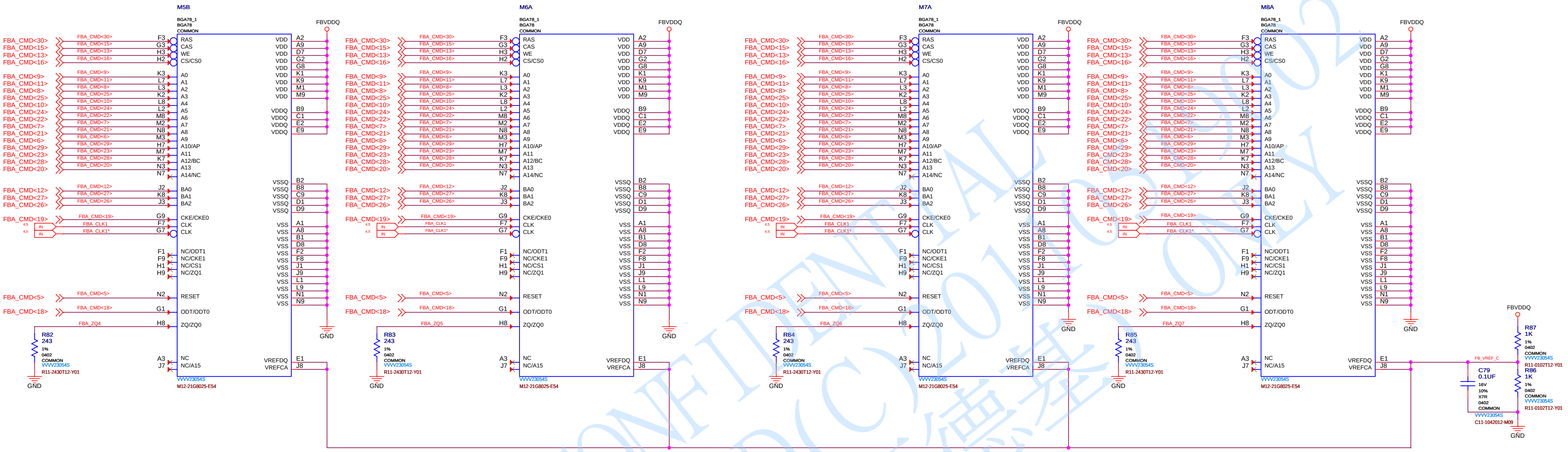
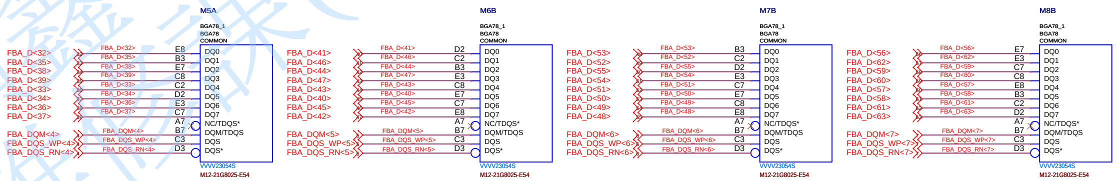
Memory 1st Bank 32..63





CMD Mapping

CMD	<0..31>	<32..63>
CMD0	CS0*	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4		
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14		
CMD15	CAS*	CAS*
CMD16		CS0*
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
CMD31		

CLK Termination

MICRO-STAR INT'L CO.,LTD

MS-V230

Size	Document Description	Rev
Custom	Memory 1st Bank 32..63	8.0

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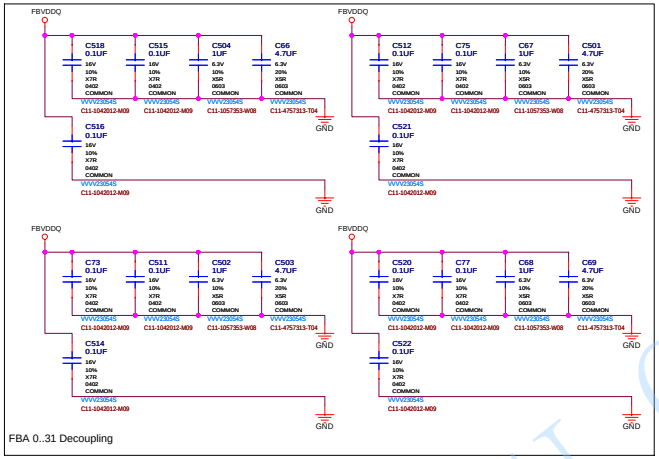
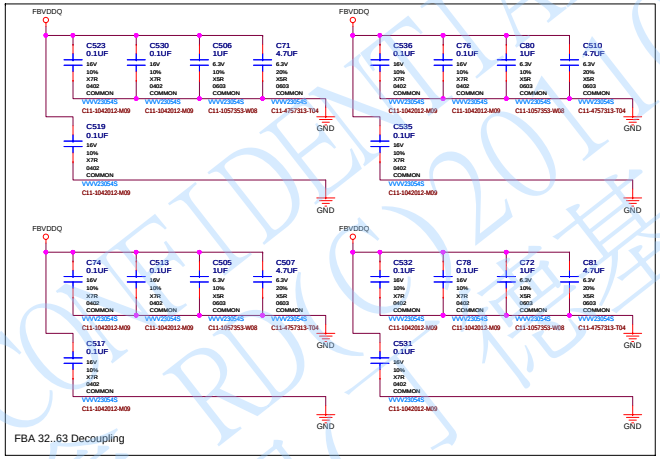
Memory Decoupling



FBA 0..31 Decoupling



FBA 32..63 Decoupling

MICRO-STAR INT'L CO.,LTD		
MS-V230		
Size: Custom	Document Description: Memory Decoupling	Rev: 8.0
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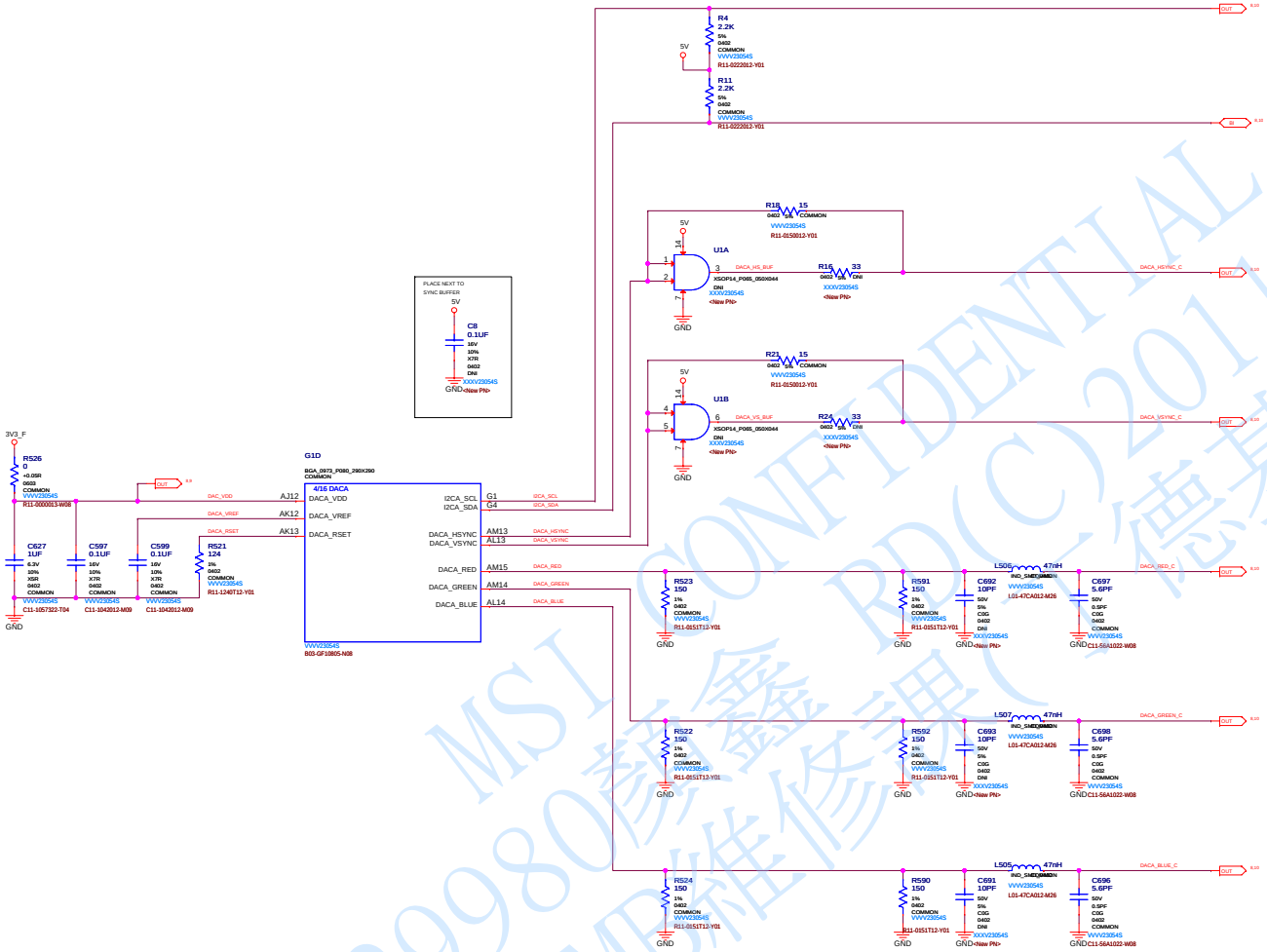
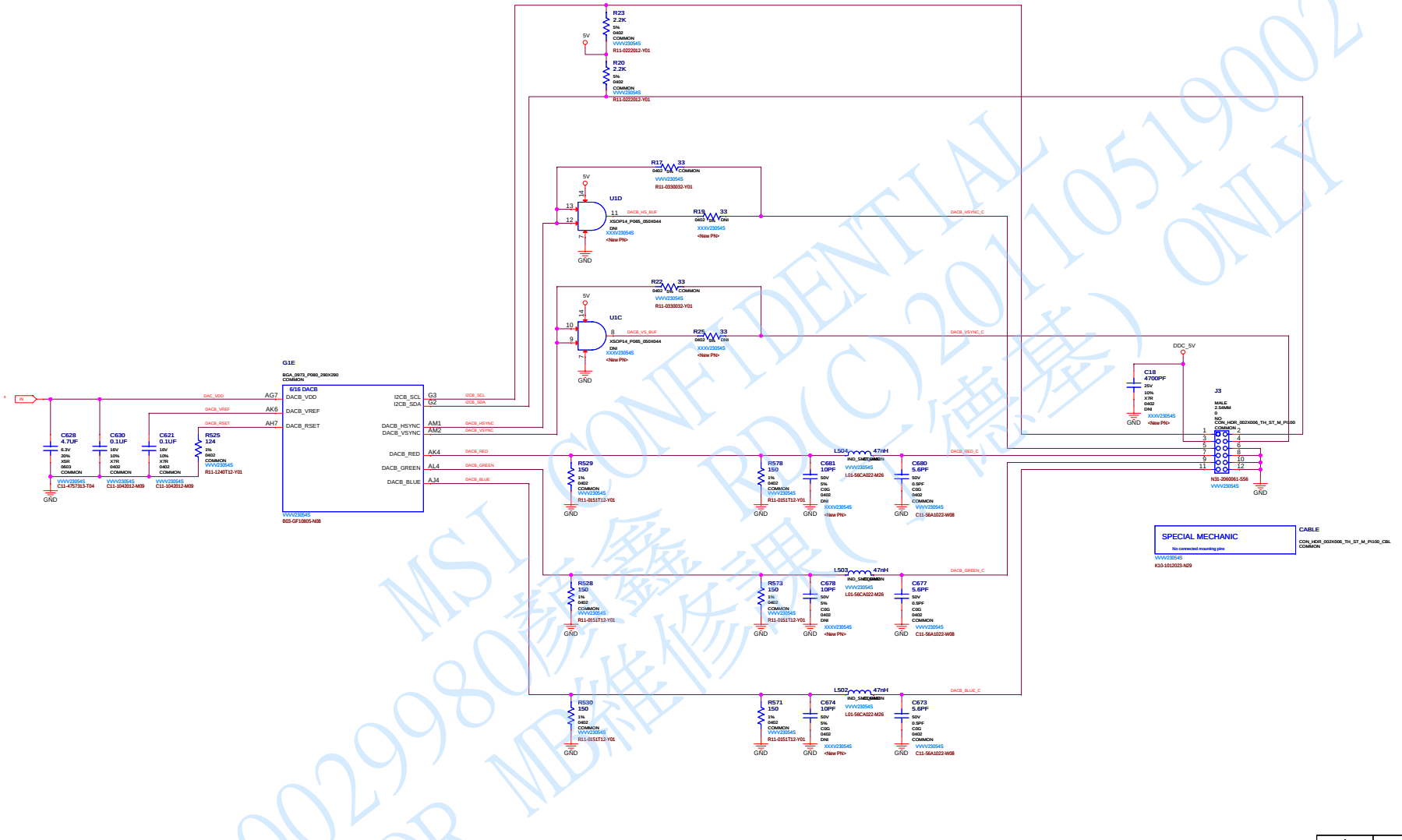
DACA VGA



MICRO-STAR INT'L CO.,LTD		
MS-V230		
Size: Custom	Document Description: DACA VGA	Rev: 8.0
Date: Friday, April 08, 2011	Sheet 8 of 20	

DACB VGA Header



MICRO-STAR INT'L CO.,LTD			
MS-V230			
Size: Custom	Document Description: DACB VGA Header		Rev: 8.0
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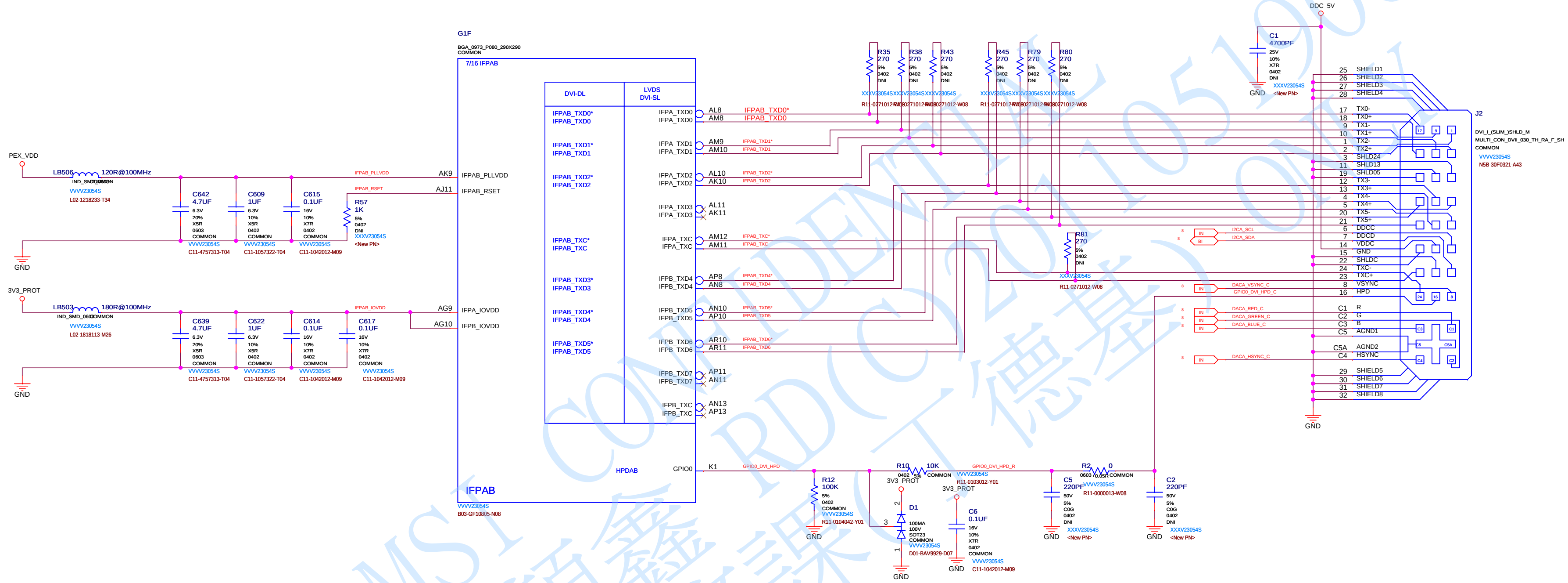
TMDS Interface



MICRO-STAR INT'L CO.,LTD

MS-V230

Size	Document Description	Rev
Custom	TMDS Interface	8.0

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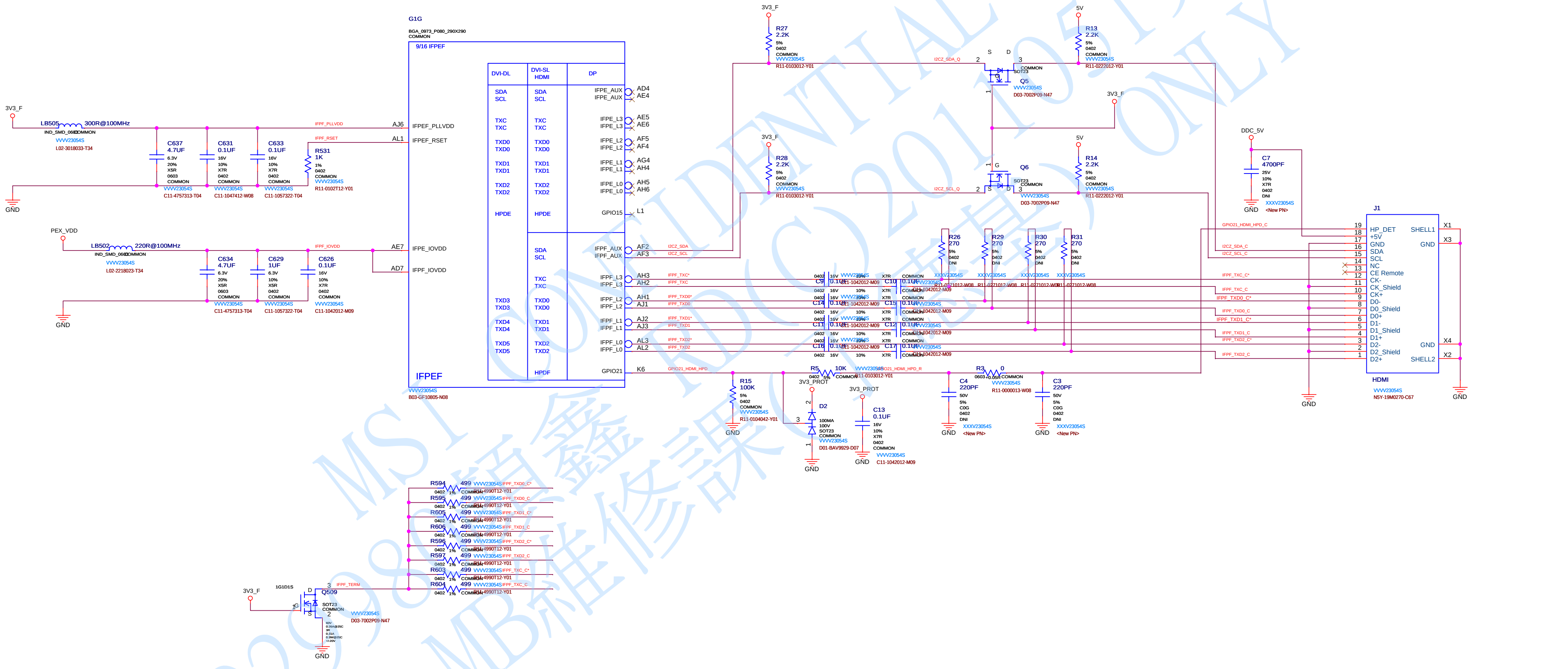
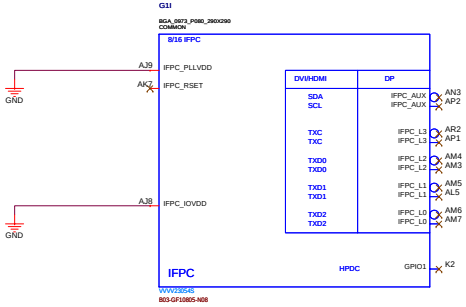
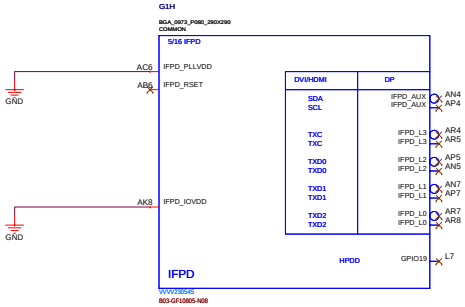
HDMI Interface

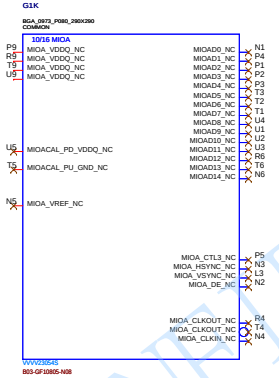


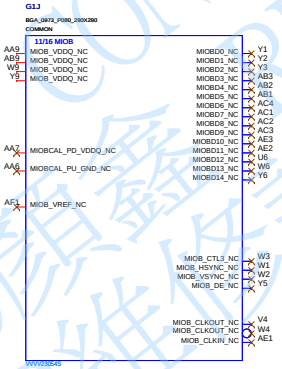
MICRO-STAR INT'L CO.,LTD			
MS-V230			
Size: Custom	Document Description: HDMI Interface		Rev: 8.0
Date: Friday, April 08, 2011		Sheet 11 of 20	

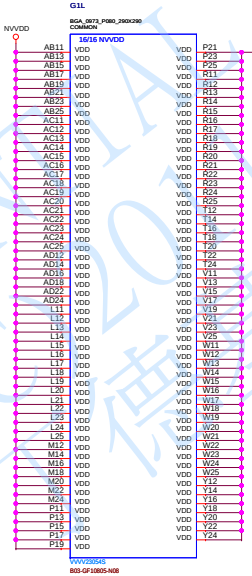
Unused Interfaces, NVVDD Decoupling

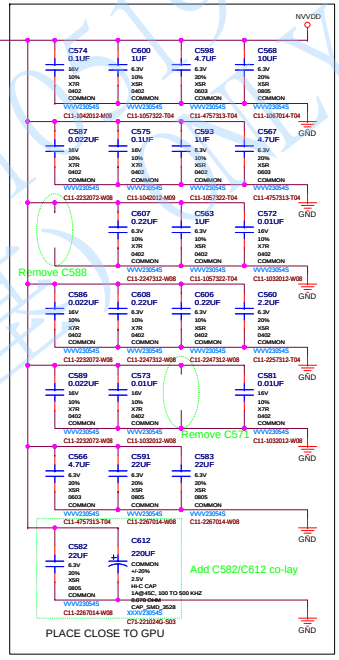


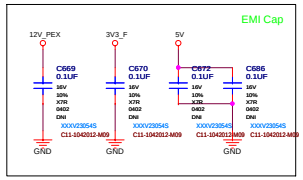


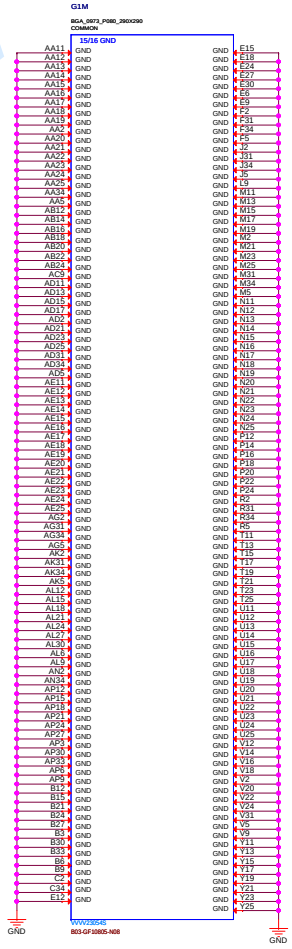












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Size: Custom	Document Description: Unused Interfaces, NVVDD Decoupling	Rev: 8.0
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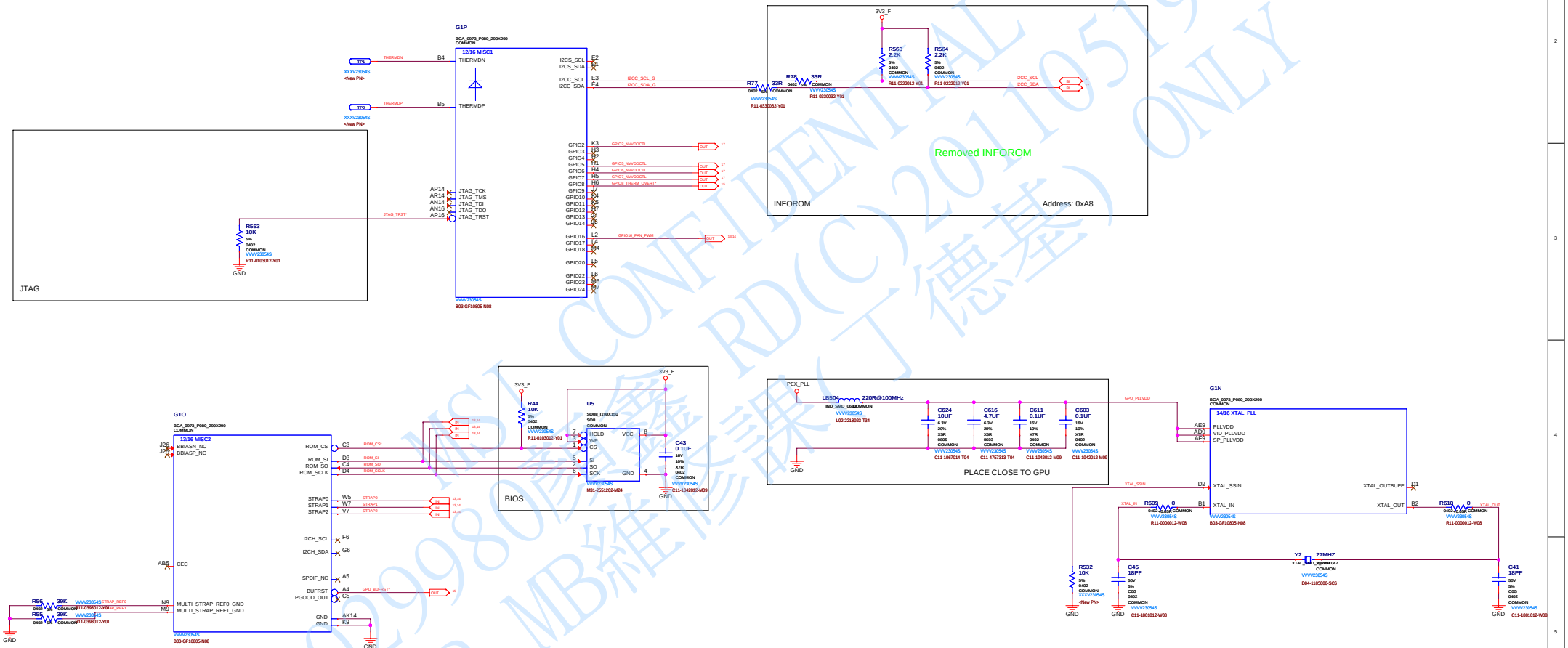
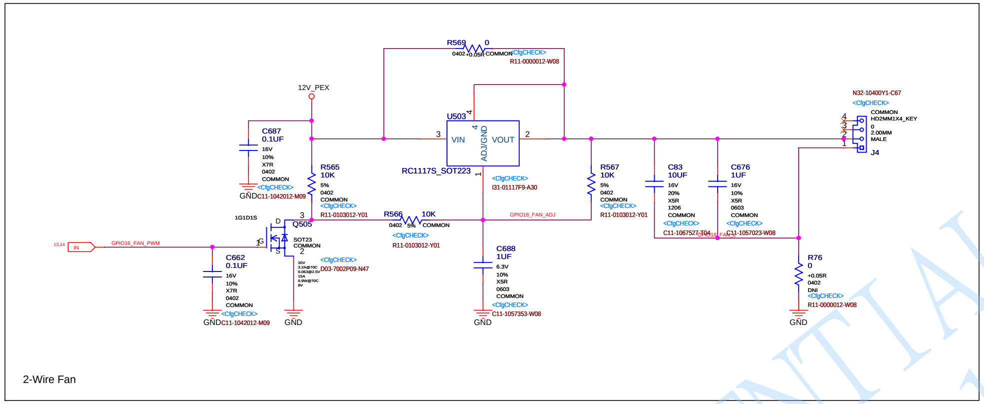
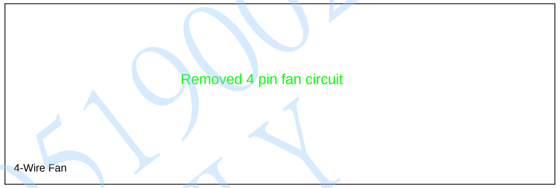
XTAL, ROM, JTAG, Misc

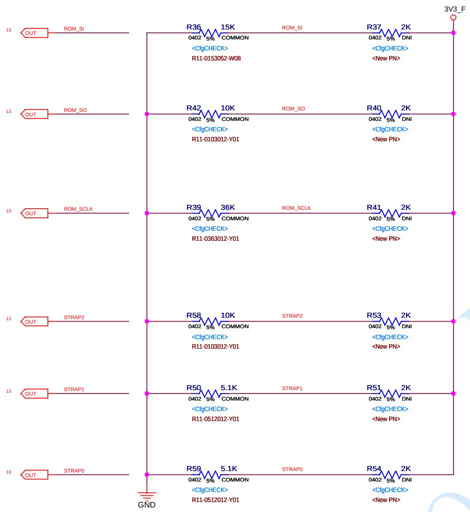


MICRO-STAR INT'L CO.,LTD	
MS-V230	
Size: Custom	Document Description: XTAL, ROM, JTAG, Misc
Rev: 8.0	
Date: Friday, April 08, 2011	Sheet 13 of 20

Straps, Thermal, Mechanical





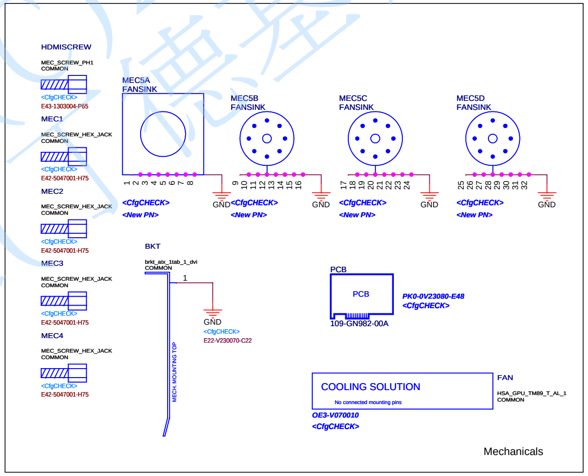


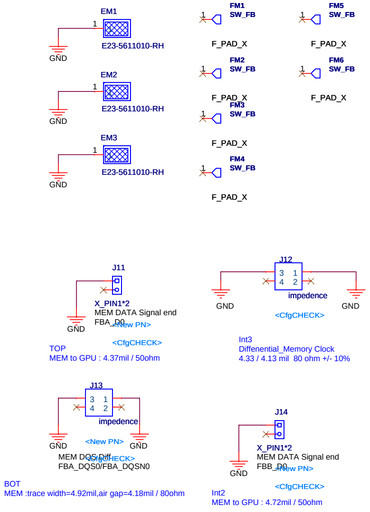
GF108 Straps

Bit	Signal	Values			
03:	RAMCFG[3]	0000			
		0001	Micron		
02:	RAMCFG[2]	0010	Hynix		
		0011	Samsung		
01:	RAMCFG[1]	0100			
		0101			
00:	RAMCFG[0]	0110			
		0111			
03:	XCLK_417	0	Disable		
		1	Enable		
02:	FB[0]	0	Default		
01:	SMB_ALT_ADDR	0	0x9E		
		1	0x9C		
00:	VGA_DEVICE	0	Disable		
		1	Enable		
03:	PCI_DEVID_EXT	0	GF108-300-A1		
		0	GF108-200-A1		
02:	SUB_VENDOR	0	No BIOS		
		1	BIOS		
01:	SLOT_CLK_CFG	0	Disable		
		1	Enable		
00:	PEX_PLL_EN_TERM100	0	Disable		
		1	Enable		
03:	PCI_DEVID[3]	0001	GF108-300-A1		
		0010	GF108-200-A1		
02:	PCI_DEVID[2]				
01:	PCI_DEVID[1]				
00:	PCI_DEVID[0]				
03:	3GIO_PADCFG_LUT_ADR[3]	0000	DSKTOP_DEFAULT	1000	DSKTOP_HTHRS
		0001	MOBILE_DEFAULT	1001	MOBILE_HTHRS_NAMP
02:	3GIO_PADCFG_LUT_ADR[2]	0010	MOBILE_NTHRS_LLAMP	1010	MOBLIE_HTHRS_LLAMP
		0011	MOBILE_NTHRS_LAMP	1011	MOBILE_HTHRS_LAMP
01:	3GIO_PADCFG_LUT_ADR[1]	0100	MOBILE_NTHRS_HAMP	1100	MOBILE_HTHRS_HAMP
		0101	MOBILE_NTHRS_HHAMP	1101	MOBILE_HTHRS_HHAMP
00:	3GIO_PADCFG_LUT_ADR[0]	0110	MOBILE_NTHRS_HHHAMP	1110	MOBILE_HTHRS_HHHAMP
		0111	MOBILE_NTHRS_HHHHAMP	1111	MOBILE_HTHRS_HHHHAMP
03:	USER[3]	0000	Default		
02:	USER[2]				
01:	USER[1]				
00:	USER[0]				

Multilevel Straps

5K to GND	0000
10K to GND	0001
15K to GND	0010
20K to GND	0011
25K to GND	0100
30K to GND	0101
35K to GND	0110
45K to GND	0111
5K to VCC	1000
10K to VCC	1001
15K to VCC	1010
20K to VCC	1011
25K to VCC	1100
30K to VCC	1101
35K to VCC	1110
45K to VCC	1111





MICRO-STAR INT'L CO.,LTD			
MS-V230			
Size: Custom	Document Description: Straps, Thermal, Mechanical		Rev: 8.0
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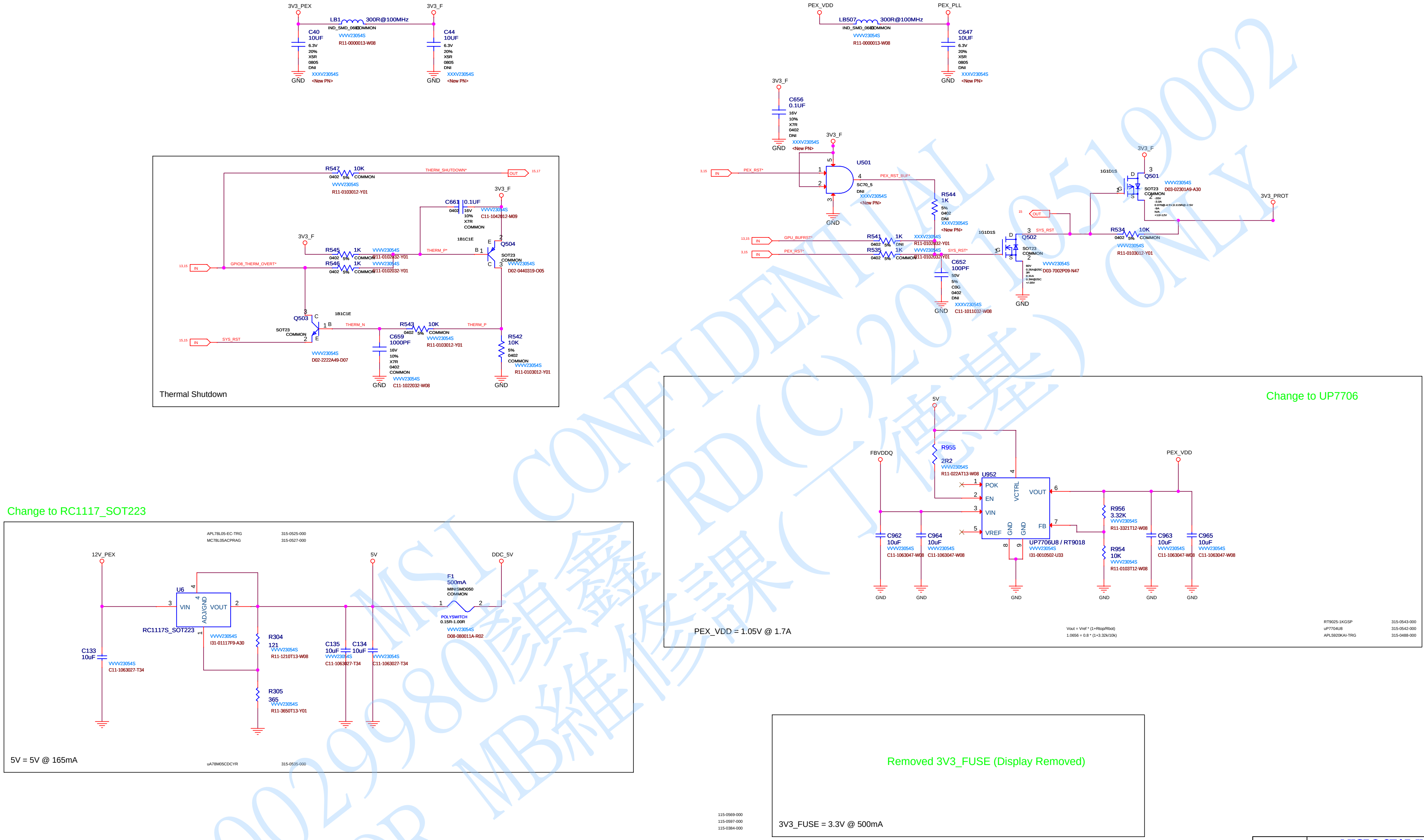
Power Supply I: Misc Power, Thermal Shutdown



MICRO-STAR INT'L CO.,LTD

MS-V230

Size	Document Description	Rev
Custom	Power Supply I: Misc Power, Thermal Shutdown	8.0

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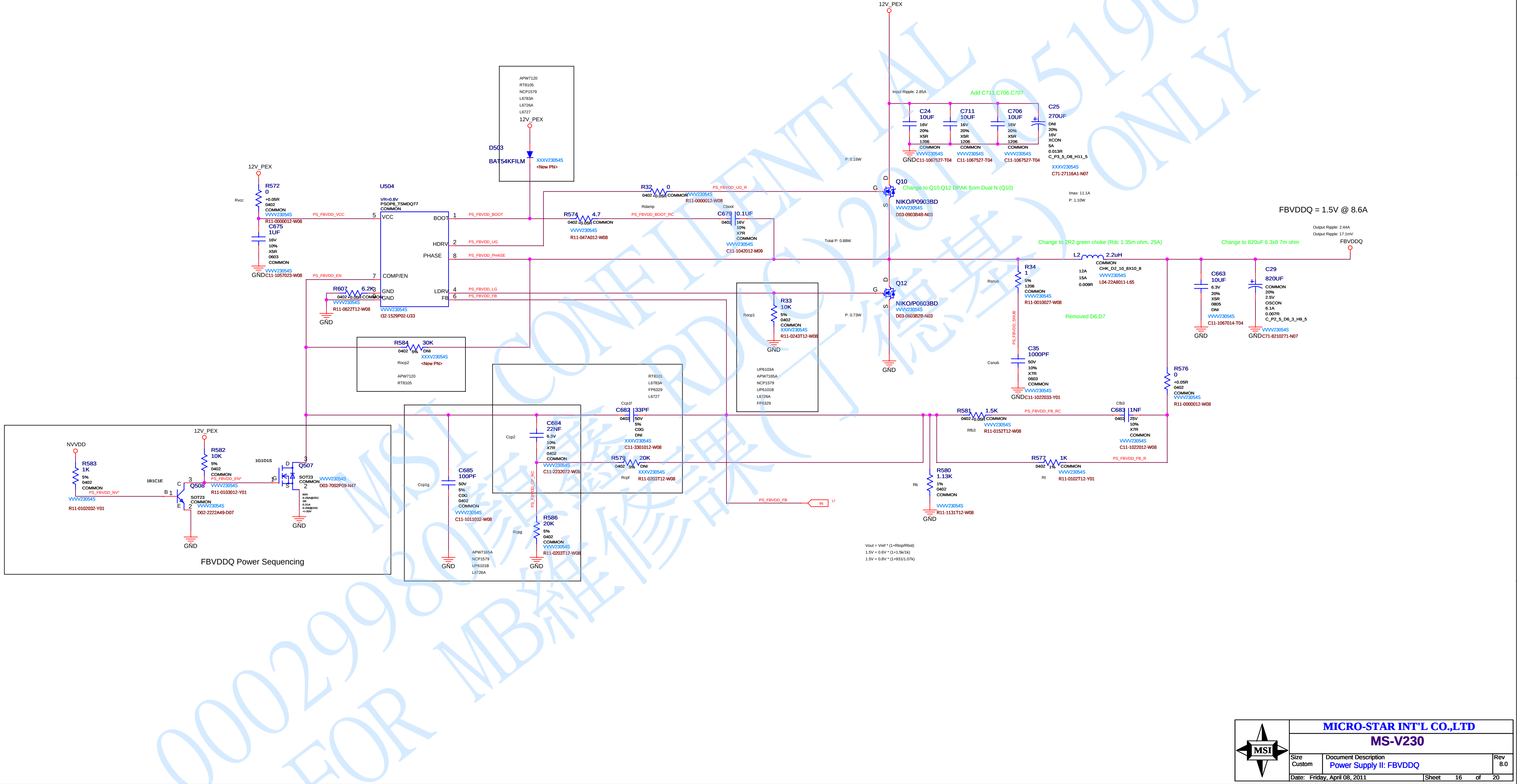
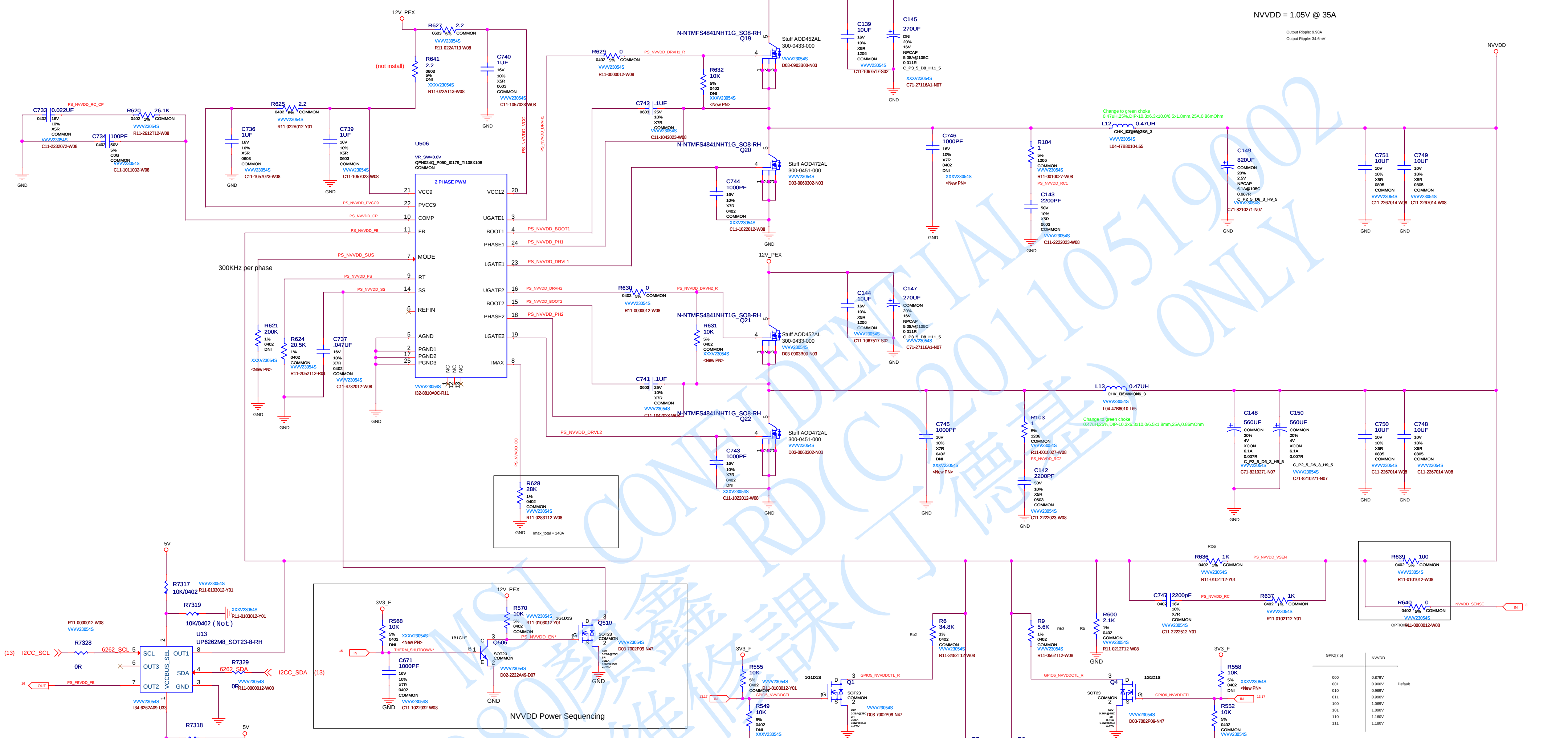
Power Supply II: FBVDDQ



Power Supply III: NVVDD

Irms = 7.2A @ 1V/38A/Two phase

NVVDD = 1.05V @ 35A



NVVDD Power Sequencing

GPIO[2,7:5]	NVVDD
0000	0.870V
0001	0.885V
0010	0.900V
0011	0.915V
0100	0.930V
0101	0.945V
0110	0.960V
0111	0.975V
1000	0.990V
1001	1.005V
1010	1.020V
1011	1.035V
1100	1.050V
1101	1.065V
1110	1.080V
1111	1.095V

Vref=0.6V; Rt=1.15k; Rb=2.55k; Rb2=47.5k; Rb3=23.7k; Rb4=11.5k; Rb5=5.76k
Vref=0.8V; Rt=931; Rb=10.7k; Rb2=48.7k; Rb3=24.3k; Rb4=12.4k; Rb5=6.19k

GPIO[7:5]	NVVDD	
000	0.879V	
001	0.900V	Default
010	0.969V	
011	0.990V	
100	1.069V	
101	1.090V	
110	1.160V	
111	1.180V	

PS	Fosc	Vref
UP6103A	300kHz	0.6V
APW7120	300kHz	0.8V
APW7165A	300kHz	0.8V
RT8105	300kHz	0.8V
NCP1579	275kHz	0.8V
RT8101	300kHz	0.8V
UP6101B	300kHz	0.8V
L6783A	300kHz	0.8V
L6726A	270kHz	0.8V
FP6329	300kHz	0.6V
L6727	300kHz	0.8V

MICRO-STAR INT'L CO.,LTD
MS-V230

Size	Document Description	Rev
Custom	Power Supply III: NVVDD	8.0

Date: Friday, April 08, 2011 | Sheet 17 of 20

Title: Basenet Report
Design: p1071_a01
Date: Mar 31 14:19:50 2010

Base nets and synonyms for
p1071_a01_lib.P1071_A01(@p1071_a01_lib.p
1071_a01(sch_1))

Base Signal	Location([Zone][dir])
3V3_F	15.1G
3V3_PEX	17.2H
3V3_PROT	15.1G
5V	15.1G
12V_PEX	17.2H
DACA_BLUE	8.1G< 8.4C
DACA_BLUE_C	8.1G> 8.5F> 10.3F<
DACA_GREEN	8.1G< 8.3C
DACA_GREEN_C	8.1G> 8.4F> 10.3F<
DACA_HSYNC	8.1G< 8.3C
DACA_HSYNC_C	8.1G> 8.2F> 10.3F<
DACA_HS_BUF	8.1G< 8.2D
DACA_RED	8.1G< 8.3C
DACA_RED_C	8.1G> 8.3F> 10.3F<
DACA_RSET	8.1G< 8.3B
DACA_VREF	8.1G< 8.3B
DACA_VSYNC	8.1G< 8.3C
DACA_VSYNC_C	8.1G> 8.3F> 10.3F<
DACA_VS_BUF	8.1G< 8.3D
DACB_BLUE	9.1G< 9.4C
DACB_BLUE_C	9.1G< 9.5E
DACB_GREEN	9.1G< 9.3C
DACB_GREEN_C	9.1G< 9.4E
DACB_HSYNC	9.1G< 9.3C
DACB_HSYNC_C	9.1G< 9.2E
DACB_HS_BUF	9.1G< 9.2D
DACB_RED	9.1G< 9.3C
DACB_RED_C	9.1G< 9.3E
DACB_RSET	9.1G< 9.3B
DACB_VREF	9.1G< 9.3B
DACB_VSYNC	9.1G< 9.3C
DACB_VSYNC_C	9.1G< 9.3E
DACB_VS_BUF	9.1G< 9.3D
DAC_VDD	8.1G> 8.3B> 9.3A<
DDC_5V	15.1G
DP_MODE	11.2F
DP_MODE*	11.2G
DP_MODE_C	11.4H
FBA_CLK0	4.1G> 4.4C> 5.2A<
	5.2C< 5.4B<
FBA_CLK0*	4.1G> 4.4C> 5.2A<
	5.2C< 5.4B<
FBA_CLK0_T	5.1G< 5.4B
FBA_CLK1	4.1G> 4.4C> 5.2E<
	5.2F< 5.5B<
FBA_CLK1*	4.1G> 4.4C> 5.2E<
	5.2F< 5.5B<
FBA_CLK1_T	5.1G< 5.5B
FBA_CMD<0>	4.3C 5.1A 5.1C
FBA_CMD<30..0>	4.1G> 4.3D> 5.1A<
FBA_CMD<2>	4.3C 4.3C 5.3A 5.3C
FBA_CMD<3>	4.3C 4.3D 5.2A 5.2C
FBA_CMD<5>	4.3C 4.4D 5.3A 5.3C
	5.3E 5.3F
FBA_CMD<6>	4.3C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<7>	4.3C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<8>	4.3C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<9>	4.3C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<10>	4.3C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<11>	4.3C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<12>	4.3C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<13>	4.3C 5.1A 5.1C 5.1E
	5.1F
FBA_CMD<15>	4.3C 5.1A 5.1C 5.1E
	5.1F
FBA_CMD<16>	4.3C 5.1E 5.1F
FBA_CMD<18>	4.3C 4.3C 5.3E 5.3F
FBA_CMD<19>	4.3C 4.3D 5.2E 5.2F
FBA_CMD<20>	4.3C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<21>	4.3C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<22>	4.4C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<23>	4.4C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<24>	4.4C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<25>	4.4C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<26>	4.4C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<27>	4.4C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<28>	4.4C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<29>	4.4C 5.2A 5.2C 5.2E
	5.2F
FBA_CMD<30>	4.4C 5.1A 5.1C 5.1E
	5.1F
FBA_D<0>	4.1A 5.4D
FBA_D<63..0>	4.1A<> 4.1G<> 5.4C<>
FBA_D<1>	4.1A 5.4D
FBA_D<2>	4.1A 5.4D
FBA_D<3>	4.1A 5.4D
FBA_D<4>	4.1A 5.4D
FBA_D<5>	4.1A 5.4D
FBA_D<6>	4.1A 5.4D
FBA_D<7>	4.1A 5.4D
FBA_D<8>	4.1A 5.5D
FBA_D<9>	4.1A 5.5D
FBA_D<10>	4.1A 5.5D
FBA_D<11>	4.1A 5.5D
FBA_D<12>	4.1A 5.5D
FBA_D<13>	4.1A 5.5D
FBA_D<14>	4.2A 5.5D
FBA_D<15>	4.2A 5.5D
FBA_D<16>	4.2A 5.4E
FBA_D<17>	4.2A 5.4E
FBA_D<18>	4.2A 5.4E
FBA_D<19>	4.2A 5.4E
FBA_D<20>	4.2A 5.4E
FBA_D<21>	4.2A 5.4E
FBA_D<22>	4.2A 5.4E
FBA_D<23>	4.2A 5.4E
FBA_D<24>	4.2A 5.5E
FBA_D<25>	4.2A 5.5E
FBA_D<26>	4.2A 5.5E
FBA_D<27>	4.2A 5.5E
FBA_D<28>	4.2A 5.5E
FBA_D<29>	4.2A 5.5E
FBA_D<30>	4.2A 5.5E
FBA_D<31>	4.2A 5.5E
FBA_D<32>	4.2A 5.4F
FBA_D<33>	4.2A 5.4F
FBA_D<34>	4.2A 5.4F
FBA_D<35>	4.2A 5.4F
FBA_D<36>	4.2A 5.4F
FBA_D<37>	4.2A 5.4F
FBA_D<38>	4.2A 5.4F
FBA_D<39>	4.2A 5.4F
FBA_D<40>	4.2A 5.5F
FBA_D<41>	4.2A 5.5F
FBA_D<42>	4.2A 5.5F
FBA_D<43>	4.2A 5.5F
FBA_D<44>	4.3A 5.5F
FBA_D<45>	4.3A 5.5F
FBA_D<46>	4.3A 5.5F
FBA_D<47>	4.3A 5.5F
FBA_D<48>	4.3A 5.4G
FBA_D<49>	4.3A 5.4G
FBA_D<50>	4.3A 5.4G
FBA_D<51>	4.3A 5.4G
FBA_D<52>	4.3A 5.4G
FBA_D<53>	4.3A 5.4G
FBA_D<54>	4.3A 5.4G
FBA_D<55>	4.3A 5.4G
FBA_D<56>	4.3A 5.5G
FBA_D<57>	4.3A 5.5G
FBA_D<58>	4.3A 5.5G
FBA_D<59>	4.3A 5.5G
FBA_D<60>	4.3A 5.5G
FBA_D<61>	4.3A 5.5G
FBA_D<62>	4.3A 5.5G
FBA_D<63>	4.3A 5.5G
FBA_DEBUG0	4.1G< 4.4C
FBA_DEBUG1	4.2G< 4.4C
FBA_DQM<0>	4.3A 5.4D
FBA_DQM<7..0>	4.1G> 4.3A> 5.4C<
FBA_DQM<1>	4.3A 5.5D
FBA_DQM<2>	4.3A 5.4E
FBA_DQM<3>	4.3A 5.5E
FBA_DQM<4>	4.3A 5.4F
FBA_DQM<5>	4.3A 5.5F
FBA_DQM<6>	4.3A 5.4G
FBA_DQM<7>	4.3A 5.5G
FBA_DQS_RN<0>	4.4A 5.4D 7.1G
FBA_DQS_RN<7..0>	4.4A<> 5.4C<> 7.1G<>
FBA_DQS_RN<1>	4.4A 5.5D 7.1G
FBA_DQS_RN<2>	4.4A 5.4E 7.1G
FBA_DQS_RN<3>	4.4A 5.5E 7.1G
FBA_DQS_RN<4>	4.4A 5.4F 7.1G
FBA_DQS_RN<5>	4.4A 5.5F 7.1G
FBA_DQS_RN<6>	4.4A 5.4G 7.1G
FBA_DQS_RN<7>	4.4A 5.5G 7.1G
FBA_DQS_WP<0>	4.4A 5.4D 7.1G
FBA_DQS_WP<7..0>	4.4A<> 5.4C<> 7.1G<>
FBA_DQS_WP<1>	4.4A 5.5D 7.1G
FBA_DQS_WP<2>	4.4A 5.4E 7.1G
FBA_DQS_WP<3>	4.4A 5.5E 7.1G
FBA_DQS_WP<4>	4.4A 5.4F 7.1G
FBA_DQS_WP<5>	4.4A 5.5F 7.1G
FBA_DQS_WP<6>	4.4A 5.4G 7.1G
FBA_DQS_WP<7>	4.4A 5.5G 7.1G
FBA_VREF	5.1G< 5.3H
FBA_ZQ0	5.1G< 5.3A
FBA_ZQ1	5.1G< 5.3C
FBA_ZQ2	5.1G< 5.3E
FBA_ZQ3	5.1G< 5.3F
FBB_CLK0	4.1G> 4.4G> 6.2A<
	6.2C< 6.4B<
FBB_CLK0*	4.1G> 4.4G> 6.2A<
	6.2C< 6.4B<
FBB_CLK0_T	6.1G< 6.4B
FBB_CLK1	4.1G> 4.4G> 6.2E<
	6.2F< 6.5B<
FBB_CLK1*	4.1G> 4.4G> 6.2E<
	6.2F< 6.5B<
FBB_CLK1_T	6.1G< 6.5B
FBB_CMD<0>	4.3G 6.1A 6.1C
FBB_CMD<30..0>	4.1G> 4.3H> 6.1A<
FBB_CMD<2>	4.3G 4.3G 6.3A 6.3C
FBB_CMD<3>	4.3G 4.3H 6.2A 6.2C
FBB_CMD<5>	4.3G 4.4H 6.3A 6.3C
	6.3E 6.3F
FBB_CMD<6>	4.3G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<7>	4.3G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<8>	4.3G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<9>	4.3G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<10>	4.3G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<11>	4.3G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<12>	4.3G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<13>	4.3G 6.1A 6.1C 6.1E
	6.1F
FBB_CMD<15>	4.3G 6.1A 6.1C 6.1E
	6.1F
FBB_CMD<16>	4.3G 6.1E 6.1F
FBB_CMD<18>	4.3G 4.3G 6.3E 6.3F
FBB_CMD<19>	4.3G 4.3H 6.2E 6.2F
FBB_CMD<20>	4.3G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<21>	4.3G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<22>	4.3G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<23>	4.4G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<24>	4.4G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<25>	4.4G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<26>	4.4G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<27>	4.4G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<28>	4.4G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<29>	4.4G 6.2A 6.2C 6.2E
	6.2F
FBB_CMD<30>	4.4G 6.1A 6.1C 6.1E
	6.1F
FBB_D<0>	4.1E 6.4D
FBB_D<63..0>	4.1E<> 4.1G<> 6.4C<>
FBB_D<1>	4.1E 6.4D
FBB_D<2>	4.1E 6.4D
FBB_D<3>	4.1E 6.4D
FBB_D<4>	4.1E 6.4D
FBB_D<5>	4.1E 6.4D
FBB_D<6>	4.1E 6.4D
FBB_D<7>	4.1E 6.4D
FBB_D<8>	4.1E 6.5D
FBB_D<9>	4.1E 6.5D
FBB_D<10>	4.1E 6.5D
FBB_D<11>	4.1E 6.5D
FBB_D<12>	4.1E 6.5D
FBB_D<13>	4.1E 6.5D
FBB_D<14>	4.1E 6.5D
FBB_D<15>	4.2E 6.5D
FBB_D<16>	4.2E 6.4E
FBB_D<17>	4.2E 6.4E
FBB_D<18>	4.2E 6.4E
FBB_D<19>	4.2E 6.4E
FBB_D<20>	4.2E 6.4E
FBB_D<21>	4.2E 6.4E
FBB_D<22>	4.2E 6.4E
FBB_D<23>	4.2E 6.4E
FBB_D<24>	4.2E 6.5E
FBB_D<25>	4.2E 6.5E
FBB_D<26>	4.2E 6.5E
FBB_D<27>	4.2E 6.5E
FBB_D<28>	4.2E 6.5E
FBB_D<29>	4.2E 6.5E
FBB_D<30>	4.2E 6.5E
FBB_D<31>	4.2E 6.5E
FBB_D<32>	4.2E 6.4F
FBB_D<33>	4.2E 6.4F
FBB_D<34>	4.2E 6.4F
FBB_D<35>	4.2E 6.4F
FBB_D<36>	4.2E 6.4F
FBB_D<37>	4.2E 6.4F
FBB_D<38>	4.2E 6.4F
FBB_D<39>	4.2E 6.4F
FBB_D<40>	4.2E 6.5F
FBB_D<41>	4.2E 6.5F
FBB_D<42>	4.2E 6.5F
FBB_D<43>	4.2E 6.5F
FBB_D<44>	4.2E 6.5F
FBB_D<45>	4.3E 6.5F
FBB_D<46>	4.3E 6.5F
FBB_D<47>	4.3E 6.5F
FBB_D<48>	4.3E 6.4G
FBB_D<49>	4.3E 6.4G
FBB_D<50>	4.3E 6.4G
FBB_D<51>	4.3E 6.4G
FBB_D<52>	4.3E 6.4G
FBB_D<53>	4.3E 6.4G
FBB_D<54>	4.3E 6.4G
FBB_D<55>	4.3E 6.4G
FBB_D<56>	4.3E 6.5G
FBB_D<57>	4.3E 6.5G
FBB_D<58>	4.3E 6.5G
FBB_D<59>	4.3E 6.5G
FBB_D<60>	4.3E 6.5G
FBB_D<61>	4.3E 6.5G
FBB_D<62>	4.3E 6.5G
FBB_D<63>	4.3E 6.5G
FBB_DEBUG0	4.2G< 4.4G
FBB_DEBUG1	4.2G< 4.4G
FBB_DQM<0>	4.3E 6.4D
FBB_DQM<7..0>	4.1G> 4.3E> 6.4C<
FBB_DQM<1>	4.3E 6.5D
FBB_DQM<2>	4.3E 6.4E
FBB_DQM<3>	4.3E 6.5E
FBB_DQM<4>	4.3E 6.4F
FBB_DQM<5>	4.3E 6.5F
FBB_DQM<6>	4.3E 6.4G
FBB_DQM<7>	4.3E 6.5G
FBB_DQS_RN<0>	4.4E 6.4D 7.1G
FBB_DQS_RN<7..0>	4.4E<> 6.4C<> 7.1G<>
FBB_DQS_RN<1>	4.4E 6.5D 7.1G
FBB_DQS_RN<2>	4.4E 6.4E 7.1G
FBB_DQS_RN<3>	4.4E 6.5E 7.1G
FBB_DQS_RN<4>	4.4E 6.4F 7.2G
FBB_DQS_RN<5>	4.4E 6.5F 7.2G
FBB_DQS_RN<6>	4.4E 6.4G 7.2G
FBB_DQS_RN<7>	4.4E 6.5G 7.2G
FBB_DQS_WP<0>	4.4E 6.4D 7.1G
FBB_DQS_WP<7..0>	4.4E<> 6.4C<> 7.1G<>
FBB_DQS_WP<1>	4.4E 6.5D 7.1G
FBB_DQS_WP<2>	4.4E 6.4E 7.1G
FBB_DQS_WP<3>	4.4E 6.5E 7.1G
FBB_DQS_WP<4>	4.4E 6.4F 7.2G
FBB_DQS_WP<5>	4.4E 6.5F 7.2G
FBB_DQS_WP<6>	4.4E 6.4G 7.2G
FBB_DQS_WP<7>	4.4E 6.5G 7.2G
FBB_VREF0	6.1G< 6.3D
FBB_VREF1	6.1G< 6.3H
FBB_ZQ0	6.1G< 6.3A
FBB_ZQ1	6.1G< 6.3C
FBB_ZQ2	6.1G< 6.3E
FBB_ZQ3	6.1G< 6.3F
FBVDDQ	16.1G
FB_CAL_PD_VDDQ	4.1G< 4.5G
FB_CAL_PU_GND	4.1G< 4.5G
FB_CAL_TERM_GND	4.1G< 4.5G
FB_PLLAVDD	4.2G< 4.5C
GPIO0_DVI_HPD	10.1G< 10.4D
GPIO0_DVI_HPD_C	10.1G< 10.3F
GPIO0_DVI_HPD_R	10.1G< 10.4E
GPIO2_NVVDDCTL	13.2D> 17.1G< 17.5G<
GPIO2_NVVDDCTL_R	17.2G< 17.5F
GPIO4_FAN_TACH	13.2D< 13.2G< 14.2F>
GPIO5_NVVDDCTL	13.2D> 17.1G< 17.4D<
GPIO5_NVVDDCTL_R	17.1G< 17.4E
GPIO6_NVVDDCTL	13.2D> 17.1G< 17.4G<
GPIO6_NVVDDCTL_R	17.1G< 17.4F
GPIO7_NVVDDCTL	13.2D> 17.1G< 17.5D<
GPIO7_NVVDDCTL_R	17.1G< 17.5E
GPIO8_THERM_OVERT*	13.2D> 15.1G< 15.2B<
GPIO16_FAN_ADJ	14.1G< 14.2C
GPIO16_FAN_C	14.1G< 14.2E
GPIO16_FAN_D	14.2D
GPIO16_FAN_L	14.1G< 14.2E
GPIO16_FAN_PWM	13.2D> 13.2G> 14.2B<
	14.2F<
GPIO16_FAN_Q	14.1G< 14.2C
GPIO21_HDMI_HPD	11.2G< 11.4D
GPIO21_HDMI_HPD_C	11.2G< 11.3G
GPIO21_HDMI_HPD_R	11.2G< 11.4E
GPU_BUFRST*	13.4D> 15.1G< 15.3E<
GPU_PLLVDD	13.2G< 13.4B
GPU_TESTMODE	3.1G< 3.5F
I2CA_SCL	8.1F> 8.1G> 10.3F<
I2CA_SDA	8.1G<> 8.2F<> 10.3F<>
I2CB_SCL	9.1G< 9.3C
I2CB_SDA	9.1G< 9.3C
I2CC_SCL	13.1D 13.1G<
I2CC_SCL_R	13.1F 13.1G<
I2CC_SDA	13.1D 13.1G<
I2CC_SDA_R	13.1F 13.1G<
I2CZ_SCL	11.1G< 11.3D
I2CZ_SCL_C	11.1G< 11.3G
I2CZ_SCL_Q	11.3F
I2CZ_SDA	11.1G< 11.3D
I2CZ_SDA_C	11.1G< 11.3G
I2CZ_SDA_Q	11.2F
IFPAB_IOVDD	10.2G< 10.3C
IFPAB_PLLVDD	10.1G< 10.2C
IFPAB_RSET	10.1G< 10.2C
IFPAB_TXC	10.1G< 10.3D
IFPAB_TXC*	10.1G< 10.3D
IFPAB_TXD0	10.1G< 10.2D
IFPAB_TXD0*	10.1G< 10.2D
IFPAB_TXD1	10.1G< 10.2D
IFPAB_TXD1*	10.1G< 10.2D
IFPAB_TXD2	10.1G< 10.2D
IFPAB_TXD2*	10.1G< 10.2D
IFPAB_TXD4	10.1G< 10.3D
IFPAB_TXD4*	10.1G< 10.3D
IFPAB_TXD5	10.1G< 10.3D
IFPAB_TXD5*	10.1G< 10.3D
IFPAB_TXD6	10.1G< 10.3D
IFPAB_TXD6*	10.1G< 10.3D
IFPF_IOVDD	11.2G< 11.3C
IFPF_PLLVDD	11.2C 11.2G<
IFPF_RSET	11.2G< 11.3C
IFPF_TERM	11.2G< 11.5C
IFPF_TXC	11.1G< 11.3D
IFPF_TXC*	11.1G< 11.3D
IFPF_TXC_C	11.1G< 11.3G 11.5D
IFPF_TXC_C*	11.1G< 11.3G 11.5D
IFPF_TXD0	11.1G< 11.3D
IFPF_TXD0*	11.1G< 11.3D
IFPF_TXD0_C	11.1G< 11.3G 11.4D
IFPF_TXD0_C*	11.1G< 11.3G 11.4D
IFPF_TXD1	11.1G< 11.3D
IFPF_TXD1*	11.1G< 11.3D
IFPF_TXD1_C	11.1G< 11.3G 11.4D
IFPF_TXD1_C*	11.1G< 11.3G 11.4D
IFPF_TXD2	11.1G< 11.3D
IFPF_TXD2*	11.1G< 11.3D
IFPF_TXD2_C	11.1G< 11.4D 11.4G
IFPF_TXD2_C*	11.1G< 11.3G 11.4D
IROM_VCC	13.1F 13.1G<
JTAG_TCK	13.1G< 13.2C
JTAG_TDI	13.1G< 13.2C
JTAG_TDO	13.1G< 13.2C
JTAG_TMS	13.1G< 13.2C
JTAG_TRST*	13.1G< 13.2C
NVVDD	17.2H
NVVDD_SENSE	3.4F> 17.1G< 17.4H<
PEX_PLL	15.1G
PEX_PLLVDD	3.1G< 3.4F
PEX_PRSNT*	3.1B 3.1G<
PEX_REFCLK	3.2C 3.5A<
PEX_REFCLK*	3.2C 3.5A<
PEX_RST*	3.1D> 15.1G< 15.2E<
	15.3E<
PEX_RST_BUF*	15.1G< 15.2F
PEX_RX0	3.2C 3.4A<
PEX_RX0*	3.2C 3.4A<
PEX_RX1	3.2C 3.4A<
PEX_RX1*	3.2C 3.4A<
PEX_RX2	3.2C 3.4A<
PEX_RX2*	3.3C 3.4A<
PEX_RX3	3.3C 3.4A<
PEX_RX3*	3.3C 3.4A<
PEX_RX4	3.3C 3.4A<
PEX_RX4*	3.3C 3.4A<
PEX_RX5	3.3C 3.5A<
PEX_RX5*	3.3C 3.5A<
PEX_RX6	3.3C 3.5A<
PEX_RX6*	3.3C 3.5A<
PEX_RX7	3.3C 3.5A<
PEX_RX7*	3.4C 3.5A<
PEX_RX8	3.4C 3.5A<
PEX_RX8*	3.4C 3.5A<
PEX_RX9	3.4C 3.5A<
PEX_RX9*	3.4C 3.5A<
PEX_RX10	3.4C 3.5A<
PEX_RX10*	3.4C 3.5A<
PEX_RX11	3.4C 3.5A<
PEX_RX11*	3.4C 3.5A<
PEX_RX12	3.4C 3.5A<
PEX_RX12*	3.5A< 3.5C
PEX_RX13	3.5A< 3.5C
PEX_RX13*	3.5A< 3.5C
PEX_RX14	3.5A< 3.5C
PEX_RX14*	3.5A< 3.5C
PEX_RX15	3.5A< 3.5C
PEX_RX15*	3.5A< 3.5C
PEX_TERMP	3.1G< 3.5F
PEX_TX0	3.2A< 3.2D
PEX_TX0*	3.2A< 3.2D
PEX_TX1	3.2A< 3.2D
PEX_TX1*	3.2A< 3.2D
PEX_TX2	3.2A< 3.2D
PEX_TX2*	3.2A< 3.2D
PEX_TX3	3.2A< 3.3D
PEX_TX3*	3.2A< 3.3D
PEX_TX4	3.2A< 3.3D
PEX_TX4*	3.2A< 3.3D
PEX_TX5	3.2A< 3.3D
PEX_TX5*	3.2A< 3.3D
PEX_TX6	3.2A< 3.3D
PEX_TX6*	3.2A< 3.3D
PEX_TX7	3.2A< 3.3D
PEX_TX7*	3.2A< 3.3D
PEX_TX8	3.3A< 3.4D
PEX_TX8*	3.3A< 3.4D
PEX_TX9	3.3A< 3.4D
PEX_TX9*	3.3A< 3.4D
PEX_TX10	3.3A< 3.4D
PEX_TX10*	3.3A< 3.4D
PEX_TX11	3.3A< 3.4D
PEX_TX11*	3.3A< 3.4D
PEX_TX12	3.3A< 3.4D
PEX_TX12*	3.3A< 3.4D
PEX_TX13	3.3A< 3.5D
PEX_TX13*	3.3A< 3.5D
PEX_TX14	3.3A< 3.5D
PEX_TX14*	3.3A< 3.5D
PEX_TX15	3.3A< 3.5D
PEX_TX15*	3.3A< 3.5D
PEX_TXX0	3.2C 3.3A<
PEX_TXX0*	3.2C 3.3A<
PEX_TXX1	3.2C 3.3A<
PEX_TXX1*	3.2C 3.3A<
PEX_TXX2	3.2C 3.3A<
PEX_TXX2*	3.2C 3.3A<
PEX_TXX3	3.3A< 3.3C
PEX_TXX3*	3.3A< 3.3C
PEX_TXX4	3.3A< 3.3C
PEX_TXX4*	3.3A< 3.3C
PEX_TXX5	3.3A< 3.3C
PEX_TXX5*	3.3A< 3.3C
PEX_TXX6	3.3A< 3.3C
PEX_TXX6*	3.3C 3.4A<
PEX_TXX7	3.3C 3.4A<
PEX_TXX7*	3.3C 3.4A<
PEX_TXX8	3.4A< 3.4C
PEX_TXX8*	3.4A< 3.4C
PEX_TXX9	3.4A< 3.4C
PEX_TXX9*	3.4A< 3.4C
PEX_TXX10	3.4A< 3.4C
PEX_TXX10*	3.4A< 3.4C
PEX_TXX11	3.4A< 3.4C
PEX_TXX11*	3.4A< 3.4C
PEX_TXX12	3.4A< 3.4C
PEX_TXX12*	3.4A< 3.4C
PEX_TXX13	3.4A< 3.5C
PEX_TXX13*	3.4A< 3.5C
PEX_TXX14	3.4A< 3.5C
PEX_TXX14*	3.4A< 3.5C
PEX_TXX15	3.4A< 3.5C
PEX_TXX15*	3.4A< 3.5C
PEX_VDD	15.1G
PS_5V_BACKDRIVE	15.1G< 15.4B
PS_5V_PROT	15.1G< 15.4B
PS_FBVDD_BOOT	16.1G< 16.2C
PS_FBVDD_BOOT_RC	16.1G< 16.2D
PS_FBVDD_CP_RC	16.1G< 16.4C
PS_FBVDD_EN	16.1G< 16.3B
PS_FBVDD_EN*	16.1G< 16.4B
PS_FBVDD_FB	16.1G< 16.3C
PS_FBVDD_FB_R	16.4F
PS_FBVDD_FB_RC	16.1G< 16.3F
PS_FBVDD_LG	16.1G< 16.3C
PS_FBVDD_NV*	16.4A
PS_FBVDD_PHASE	16.1G< 16.3C
PS_FBVDD_SNUB	16.1G< 16.3F
PS_FBVDD_UG	16.1G< 16.3C
PS_FBVDD_UG_R	16.1G< 16.2D
PS_FBVDD_VCC	16.1G< 16.2B
PS_NVVDD_BOOT	17.1G< 17.2C
PS_NVVDD_BOOT_RC	17.1G< 17.2D
PS_NVVDD_CP_RC	17.1G< 17.4C
PS_NVVDD_EN	17.1G< 17.3B
PS_NVVDD_EN*	17.1G< 17.4B
PS_NVVDD_FB	17.1G< 17.3C
PS_NVVDD_FB_RC	17.1G< 17.3F
PS_NVVDD_LG	17.1G< 17.3C
PS_NVVDD_PHASE	17.1G< 17.3C
PS_NVVDD_SNUB	17.1G< 17.3F
PS_NVVDD_UG	17.1G< 17.3C
PS_NVVDD_UG_R	17.1G< 17.2D
PS_NVVDD_VCC	17.1G< 17.2B
PS_NVVDD_VSEN	17.1G< 17.4G
PS_PEXVDD_CNTL	15.1G< 15.4E
PS_PEXVDD_FB	15.1G< 15.4F
ROM_CS*	13.2G< 13.3D
ROM_SCLK	13.2G< 13.3D< 14.4B>
	14.4C
ROM_SI	13.2G< 13.3D< 14.3B>
	14.3C
ROM_SO	13.2G< 13.3D< 14.3B>
	14.3C
SNN_3V3FUSE_OC	15.5E
SNN_3V3_AUX	3.1B
SNN_BBIASN	13.3C
SNN_BBIASP	13.3C
SNN_CEC	13.3C
SNN_DP_CEC	11.4H
SNN_FBA0_A1	5.3A
SNN_FBA0_A11	5.3A
SNN_FBA0_J2	5.3A
SNN_FBA0_J10	5.3A
SNN_FBA0_L2	5.3A
SNN_FBA0_L10	5.3A
SNN_FBA0_M8	5.2A
SNN_FBA0_T1	5.3A
SNN_FBA0_T8	5.2A
SNN_FBA0_T11	5.3A
SNN_FBA1_A1	5.3C
SNN_FBA1_A11	5.3C
SNN_FBA1_J2	5.3C
SNN_FBA1_J10	5.3C
SNN_FBA1_L2	5.3C
SNN_FBA1_L10	5.3C
SNN_FBA1_M8	5.2C
SNN_FBA1_T1	5.3C
SNN_FBA1_T8	5.2C
SNN_FBA1_T11	5.3C
SNN_FBA2_A1	5.3E
SNN_FBA2_A11	5.3E
SNN_FBA2_J2	5.3E
SNN_FBA2_J10	5.3E
SNN_FBA2_L2	5.3E
SNN_FBA2_L10	5.3E
SNN_FBA2_M8	5.2E
SNN_FBA2_T1	5.3E
SNN_FBA2_T8	5.2E
SNN_FBA2_T11	5.3E
SNN_FBA3_A1	5.3F
SNN_FBA3_A11	5.3F
SNN_FBA3_J2	5.3F
SNN_FBA3_J10	5.3F
SNN_FBA3_L2	5.3F
SNN_FBA3_L10	5.3F
SNN_FBA3_M8	5.2F
SNN_FBA3_T1	5.3F
SNN_FBA3_T8	5.2F
SNN_FBA3_T11	5.3F
SNN_FBA_CMD1	4.3C
SNN_FBA_CMD4	4.3C
SNN_FBA_CMD14	4.3C
SNN_FBA_CMD17	4.3C
SNN_FBA_CMD31	4.4C
SNN_FBA_WCK0	4.4A
SNN_FBA_WCK1	4.4A
SNN_FBA_WCK2	4.4A
SNN_FBA_WCK3	4.4A
SNN_FBA_WCKN0	4.4A
SNN_FBA_WCKN1	4.4A
SNN_FBA_WCKN2	4.4A
SNN_FBA_WCKN3	4.4A
SNN_FBB0_A1	6.3A
SNN_FBB0_A11	6.3A
SNN_FBB0_J2	6.3A
SNN_FBB0_J10	6.3A
SNN_FBB0_L2	6.3A
SNN_FBB0_L10	6.3A
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SNN_FBB0_T1	6.3A
SNN_FBB0_T8	6.2A
SNN_FBB0_T11	6.3A
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SNN_FBB1_A11	6.3C
SNN_FBB1_J2	6.3C
SNN_FBB1_J10	6.3C
SNN_FBB1_L2	6.3C
SNN_FBB1_L10	6.3C
SNN_FBB1_M8	6.2C
SNN_FBB1_T1	6.3C
SNN_FBB1_T8	6.2C
SNN_FBB1_T11	6.3C
SNN_FBB2_A1	6.3E
SNN_FBB2_A11	6.3E
SNN_FBB2_J2	6.3E
SNN_FBB2_J10	6.3E
SNN_FBB2_L2	6.3E
SNN_FBB2_L10	6.3E
SNN_FBB2_M8	6.2E
SNN_FBB2_T1	6.3E
SNN_FBB2_T8	6.2E
SNN_FBB2_T11	6.3E
SNN_FBB3_A1	6.3F
SNN_FBB3_A11	6.3F
SNN_FBB3_J2	6.3F
SNN_FBB3_J10	6.3F
SNN_FBB3_L2	6.3F
SNN_FBB3_L10	6.3F
SNN_FBB3_M8	6.2F
SNN_FBB3_T1	6.3F
SNN_FBB3_T8	6.2F
SNN_FBB3_T11	6.3F
SNN_FBB_CMD1	4.3G
SNN_FBB_CMD4	4.3G
SNN_FBB_CMD14	4.3G
SNN_FBB_CMD17	4.3G

MSI

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SNN_FBB_CMD31 4.4G
SNN_FBB_WCK0 4.4E
SNN_FBB_WCK1 4.4E
SNN_FBB_WCK2 4.4E
SNN_FBB_WCK3 4.4E
SNN_FBB_WCKN0 4.4E
SNN_FBB_WCKN1 4.4E
SNN_FBB_WCKN2 4.4E
SNN_FBB_WCKN3 4.4E
SNN_FB_DLLAVDD 4.5C
SNN_FB_PLLAVDD 4.5C
SNN_FB_VREF 4.5A
SNN_GPIO1 12.3B
SNN_GPIO3 13.2D
SNN_GPIO9 13.2D
SNN_GPIO10 13.2D
SNN_GPIO11 13.2D
SNN_GPIO12 13.2D
SNN_GPIO13 13.2D
SNN_GPIO14 13.2D
SNN_GPIO15 11.3D
SNN_GPIO17 13.2D
SNN_GPIO18 13.2D
SNN_GPIO19 12.4B
SNN_GPIO20 13.2D
SNN_GPIO22 13.2D
SNN_GPIO23 13.2D
SNN_GPIO24 13.2D
SNN_GPU_A2 3.2F
SNN_GPU_A7 3.2F
SNN_GPU_AA4 3.2F
SNN_GPU_AB4 3.2F
SNN_GPU_AB7 3.3F
SNN_GPU_AC5 3.3F
SNN_GPU_AD6 3.3F
SNN_GPU_AF6 3.3F
SNN_GPU_AG6 3.3F
SNN_GPU_AJ5 3.3F
SNN_GPU_AK15 3.3F
SNN_GPU_AL7 3.3F
SNN_GPU_B7 3.3F
SNN_GPU_C7 3.3F
SNN_GPU_D5 3.3F
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SNN_GPU_F4 3.3F
SNN_GPU_G5 3.3F
SNN_GPU_H32 3.3F
SNN_GPU_P6 3.3F
SNN_GPU_U7 3.3F
SNN_GPU_V6 3.3F
SNN_GPU_Y4 3.3F
SNN_HDMI_CEC 11.3G
SNN_HDMI_RSVD 11.3G
SNN_I2CH_SCL 13.3D
SNN_I2CH_SDA 13.3D
SNN_I2CS_SCL 13.1D
SNN_I2CS_SDA 13.1D
SNN_IFPA_TXD3 10.3D
SNN_IFPA_TXD3* 10.2D
SNN_IFPB_TXC 10.3D
SNN_IFPB_TXC* 10.3D
SNN_IFPB_TXD7 10.3D
SNN_IFPB_TXD7* 10.3D
SNN_IFPC_AUX 12.2B
SNN_IFPC_AUX* 12.2B
SNN_IFPC_L0 12.3B
SNN_IFPC_L0* 12.3B
SNN_IFPC_L1 12.2B
SNN_IFPC_L1* 12.2B
SNN_IFPC_L2 12.2B
SNN_IFPC_L2* 12.2B
SNN_IFPC_L3 12.2B
SNN_IFPC_L3* 12.2B
SNN_IFPC_RSET 12.2A
SNN_IFPD_AUX 12.4B
SNN_IFPD_AUX* 12.4B
SNN_IFPD_L0 12.4B
SNN_IFPD_L0* 12.4B
SNN_IFPD_L1 12.4B
SNN_IFPD_L1* 12.4B
SNN_IFPD_L2 12.4B
SNN_IFPD_L2* 12.4B
SNN_IFPD_L3 12.4B
SNN_IFPD_L3* 12.4B
SNN_IFPD_RSET 12.4A
SNN_IFPE_AUX 11.2D
SNN_IFPE_AUX* 11.2D
SNN_IFPE_L0 11.3D
SNN_IFPE_L0* 11.3D
SNN_IFPE_L1 11.3D
SNN_IFPE_L1* 11.3D
SNN_IFPE_L2 11.3D
SNN_IFPE_L2* 11.3D
SNN_IFPE_L3 11.2D
SNN_IFPE_L3* 11.2D
SNN_MIOACAL_PD_VDD 12.2C
Q
SNN_MIOACAL_PU_GND 12.2C

SNN_MIOAD0 12.2D
SNN_MIOAD1 12.2D
SNN_MIOAD2 12.2D
SNN_MIOAD3 12.2D
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SNN_MIOAD5 12.2D
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SNN_MIOAD7 12.2D
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SNN_MIOAD10 12.2D
SNN_MIOAD11 12.2D
SNN_MIOAD12 12.2D
SNN_MIOAD13 12.2D
SNN_MIOAD14 12.2D
SNN_MIOA_CLKIN 12.3D
SNN_MIOA_CLKOUT 12.3D
SNN_MIOA_CLKOUT* 12.3D
SNN_MIOA_CTL3 12.3D
SNN_MIOA_DE 12.3D
SNN_MIOA_HSYNC 12.3D
SNN_MIOA_VDDQ_P9 12.2C
SNN_MIOA_VDDQ_R9 12.2C
SNN_MIOA_VDDQ_T9 12.2C
SNN_MIOA_VDDQ_U9 12.2C
SNN_MIOA_VREF 12.2C
SNN_MIOA_VSYNC 12.3D
SNN_MIOBCAL_PD_VDD 12.4C
Q
SNN_MIOBCAL_PU_GND 12.4C
SNN_MIOBD0 12.3D
SNN_MIOBD1 12.3D
SNN_MIOBD2 12.4D
SNN_MIOBD3 12.4D
SNN_MIOBD4 12.4D
SNN_MIOBD5 12.4D
SNN_MIOBD6 12.4D
SNN_MIOBD7 12.4D
SNN_MIOBD8 12.4D
SNN_MIOBD9 12.4D
SNN_MIOBD10 12.4D
SNN_MIOBD11 12.4D
SNN_MIOBD12 12.4D
SNN_MIOBD13 12.4D
SNN_MIOBD14 12.4D
SNN_MIOB_CLKIN 12.5D
SNN_MIOB_CLKOUT 12.4D
SNN_MIOB_CLKOUT* 12.4D
SNN_MIOB_CTL3 12.4D
SNN_MIOB_DE 12.4D
SNN_MIOB_HSYNC 12.4D
SNN_MIOB_VDDQ_AA9 12.3C
SNN_MIOB_VDDQ_AB9 12.3C
SNN_MIOB_VDDQ_W9 12.4C
SNN_MIOB_VDDQ_Y9 12.4C
SNN_MIOB_VREF 12.4C
SNN_MIOB_VSYNC 12.4D
SNN_NVVDD_SENSE_1 3.4F
SNN_NVVDD_SENSE_3 3.4F
SNN_PEX_CLKREQ* 3.1D
SNN_PEX_PLL_HVDD 3.5F
SNN_PEX_TSTCLK_OUT 3.2D
SNN_PEX_TSTCLK_OUT 3.2D
*
SNN_PGOOD_OUT 13.4D
SNN_PS_PEXVDD_NC 15.4E
SNN_PS_PEXVDD_POK 15.4E
SNN_SMCLK 3.1C
SNN_SMDAT 3.1C
SNN_SPDIF 13.4D
SNN_SVDD_3V3 3.2F
SNN_XTAL_OUTBUFF 13.5D
STRAP0 13.2G< 13.3D> 14.4C>
14.5B>
STRAP1 13.2G< 13.3D> 14.4B>
14.4C
STRAP2 13.2G< 13.3D> 14.4B>
14.4C
STRAP_REF0 13.1G< 13.4C
STRAP_REF1 13.1G< 13.4C
SYS_RST 15.1G< 15.3B< 15.3F>
SYS_RST* 15.1G< 15.3F
THERMDN 13.1C 13.1G<
THERMDP 13.1G< 13.2C
THERM_N 15.1G< 15.3C
THERM_P 15.1G< 15.3C
THERM_P* 15.1G< 15.2C
THERM_SHUTDOWN* 15.1G> 15.2D> 17.4A<
XTAL_IN 13.1G< 13.5B
XTAL_OUT 13.1G< 13.5D
XTAL_SSIN 13.1G< 13.5B

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Date: Mar 31 14:19:50 2010

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C13	[11.4E]
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C20	[15.4C]
C21	[17.3F]
C22	[17.1F]
C23	[15.4B]
C24	[16.2E]
C25	[17.2E]
C26	[17.1F]
C27	[17.1E]
C28	[3.1B]
C29	[16.3G]
C30	[16.3H]
C31	[17.3H]
C32	[17.3H]
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C37	[15.4E]
C38	[3.1A]
C39	[3.1A]
C40	[15.1B]
C41	[13.5D]
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C43	[13.3E]
C44	[15.1C]
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C46	[15.4G]
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C68	[7.3C]
C69	[7.3C]
C70	[5.4H]
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C78	[7.3C]
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C85	[11.3E]
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C536	[7.3E]
C537	[3.4D]
C538	[3.4D]
C539	[7.3D]
C540	[7.3E]
C541	[3.4D]
C542	[3.4D]
C543	[3.4D]
C544	[3.4D]
C545	[4.1C]
C546	[3.4D]
C547	[4.1D]
C548	[4.1C]
C549	[4.1D]
C550	[7.3D]
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C552	[4.5D]
C553	[4.5C]
C554	[3.4D]
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C556	[4.1C]
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Size	Document Description	Rev
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