

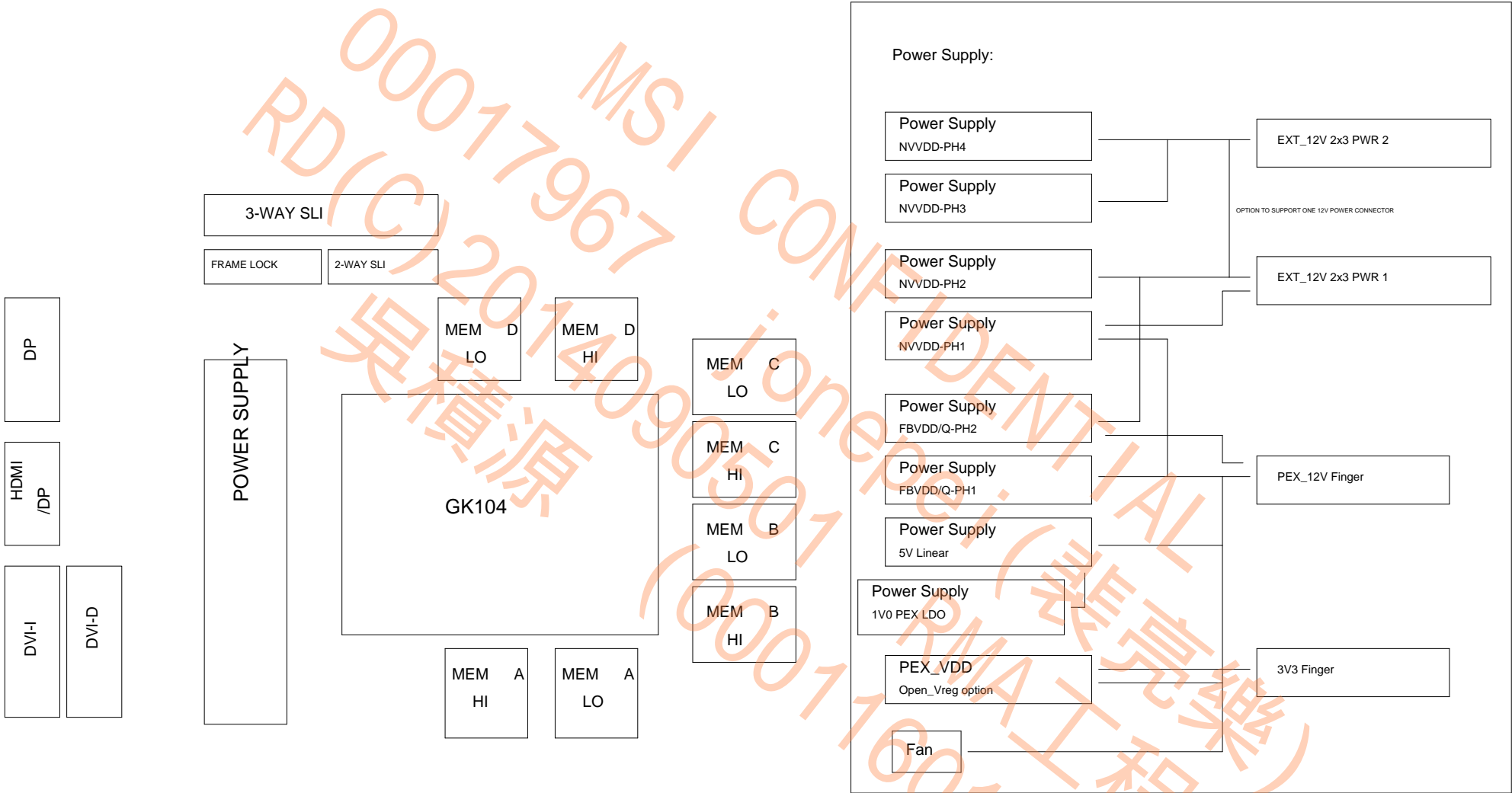
# P2004

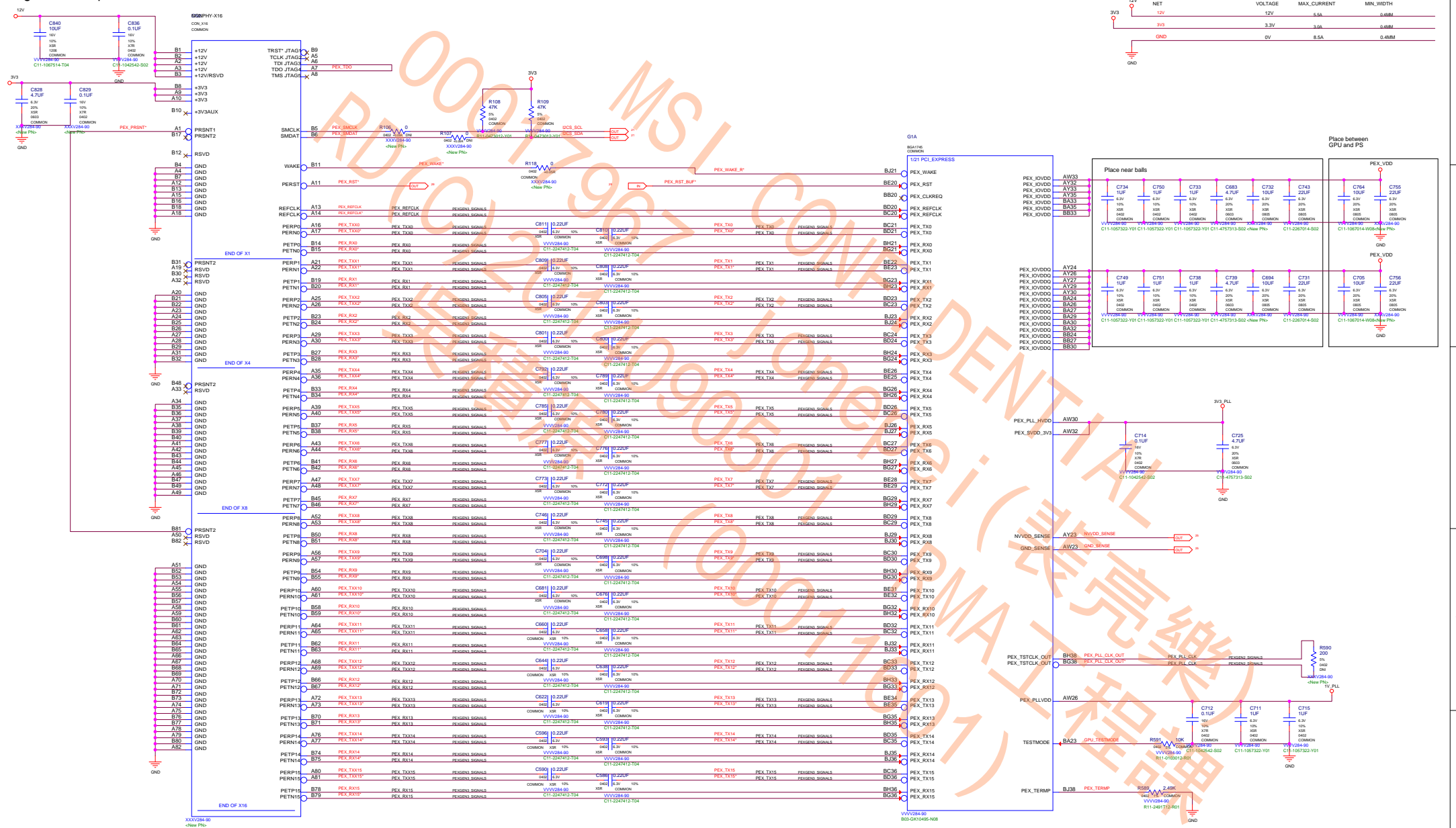
4/2GB GDDR5, 256/192b, 128Mx16/64Mx32  
DVI-I+DVI-D (stacked) + HDMI/DP + DP

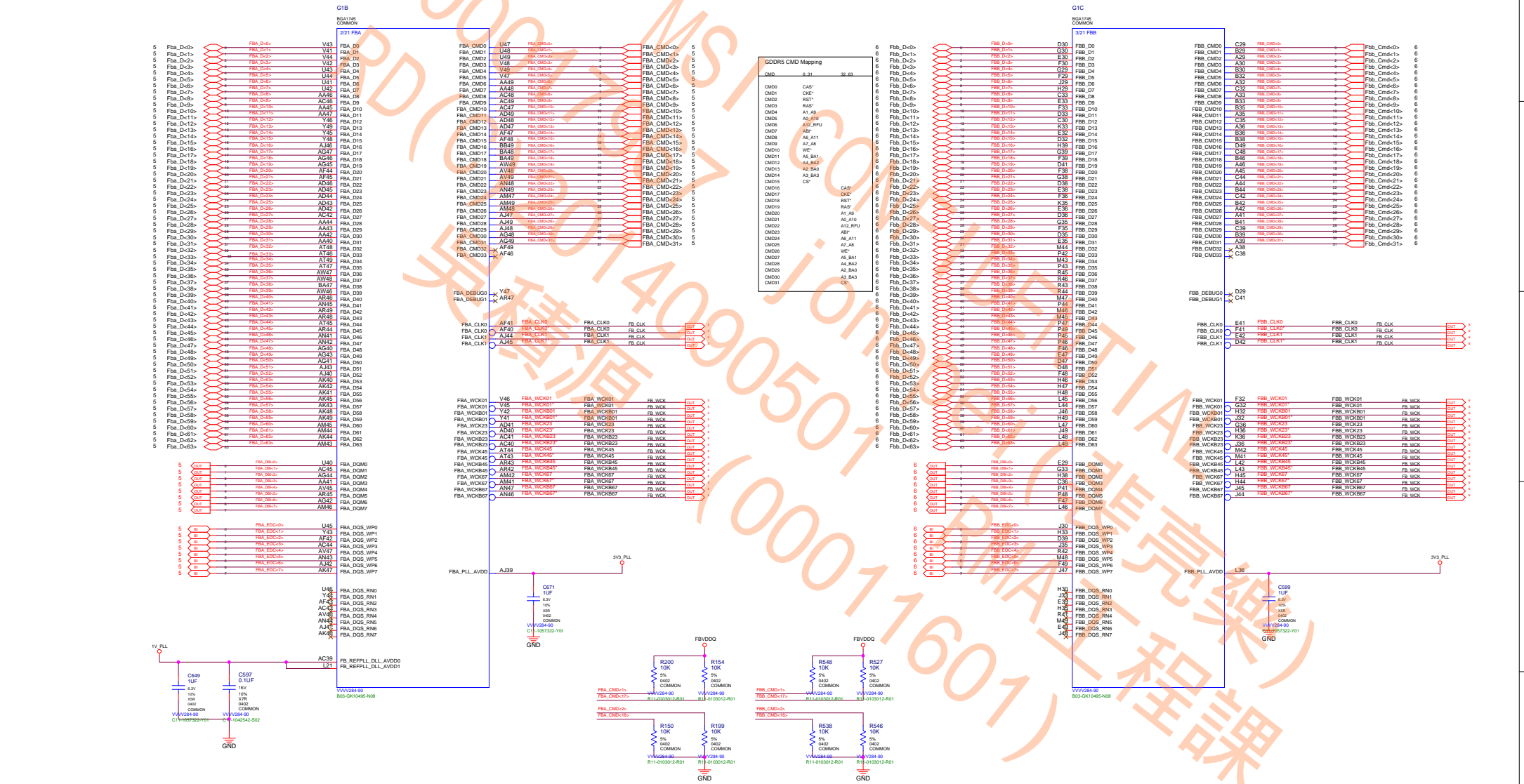
## TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	GPU FB_AB
5	MEM FB_A
6	MEM FB_B
7	MEM FB_AB PWR
8	GPU FB_CD
9	MEM FB_C
10	MEM FB_D
11	MEM FB_CD PWR
12	GPU PWR and GND
13	GPU Decoupling
14	DACA Interface
15	IFPAB DVI-I-DL
16	IFPEF DVI-D-DL
17	IFPC HDMI/DP
18	IFPD DP
19	MIOA/B Interface and Frame Lock
20	Stereo Connector
21	MISC1: Fan, Thermal, JTAG, GPIO
22	MISC2: ROM, XTAL, Straps
23	PS: 5V, PEX_VDD
24	PS: FBVDD/Q
25	PS: NVVDD Controller

Page	Description
26	PS: NVVDD PHASE 1 & 3
27	PS: NVVDD PHASES 2 & 4
28	PS: Inputs, Filtering, and Monitoring
29	PS: Thermal Shutdown & Lighted SLI DRIVER
30	PS: 12V Current Steering
31	MECH
	<b>Change List</b>
	Base on P2004 sku 10 designkit to modify
13	Removed POSCAPs
15	Removed stack DVI , change to one slot DVI-I,add ESD
16	Removed stack DVI , IFPE add mDP
17	Removed DP co-layout
18	Change to mDP from DP
19	Removed co-layout resistor one PIN to minimize MIO BUS stubs
20	Removed Stereo Connector circuit
21	Removed Fan startup ASM and Backup option vs. "smart" fan circuit
23	Removed PEXVDD1 and PEX Pwm circuit,change 5V to 1117 from 78m05
24	Change PWM to single phase solution
28	Change input power to 8-pin from 6-pin*2
29	Change SLI LED circuit
30	Removed PEX6-2 input DT and FBVDDQ PSI circuit

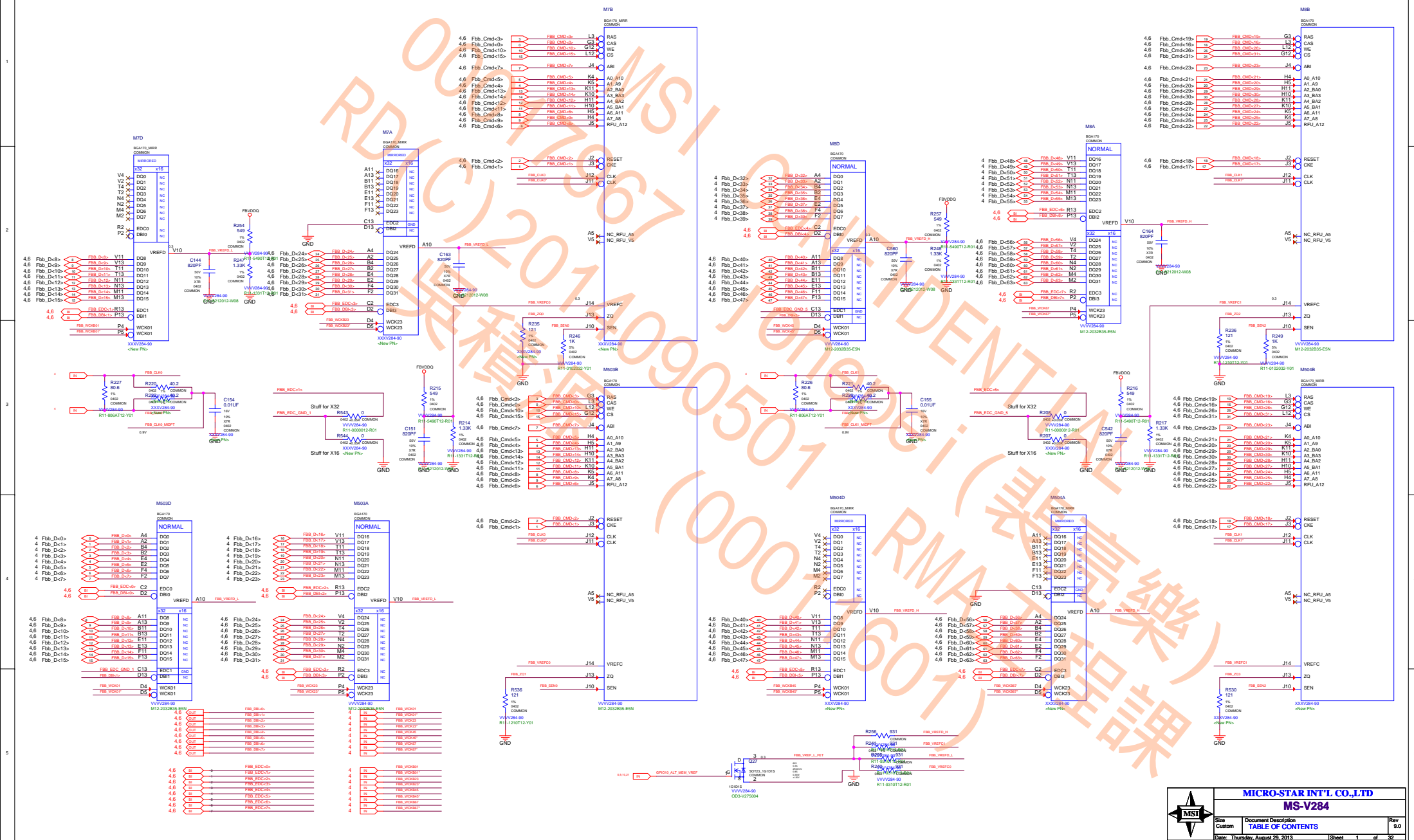


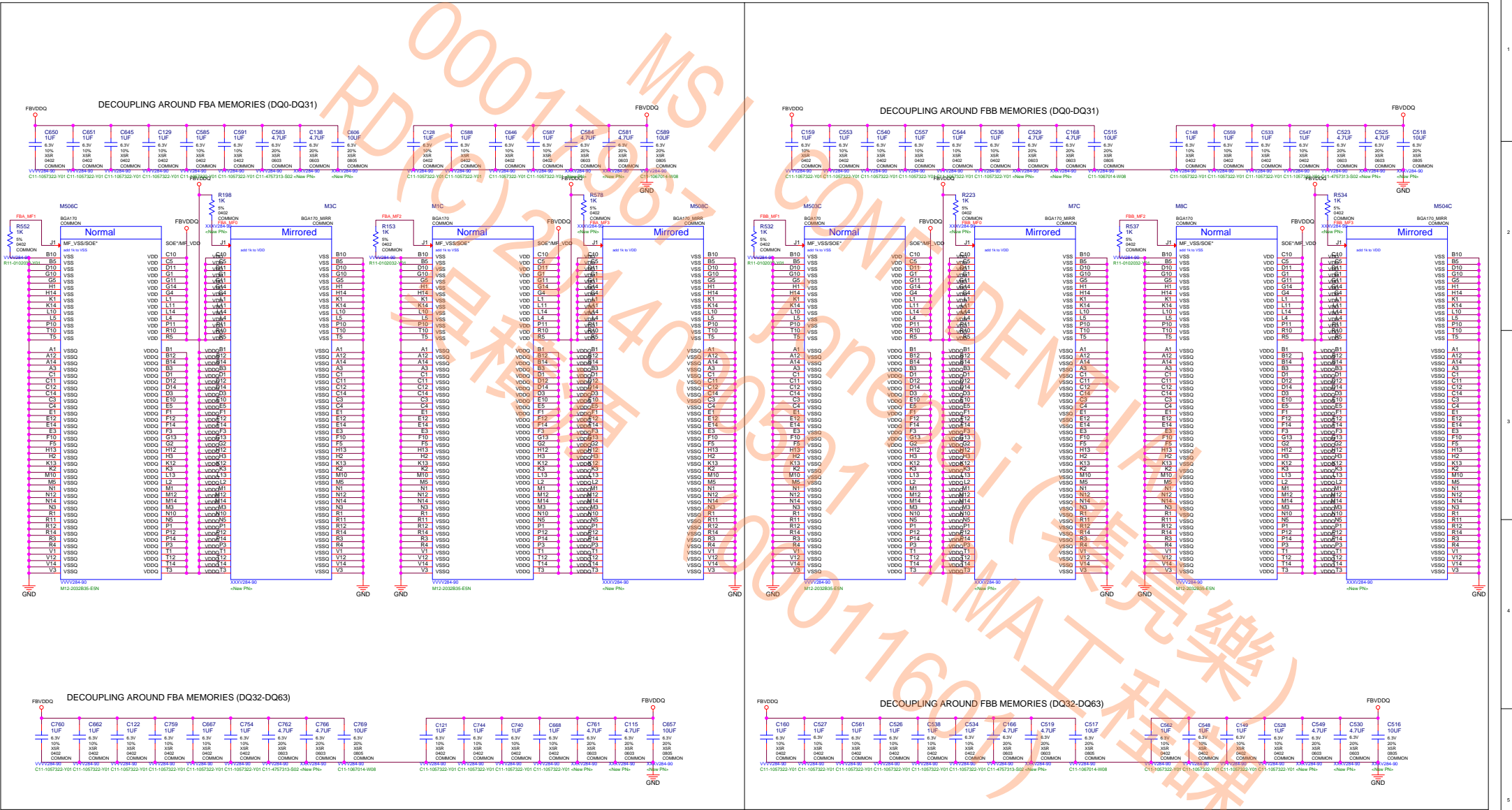


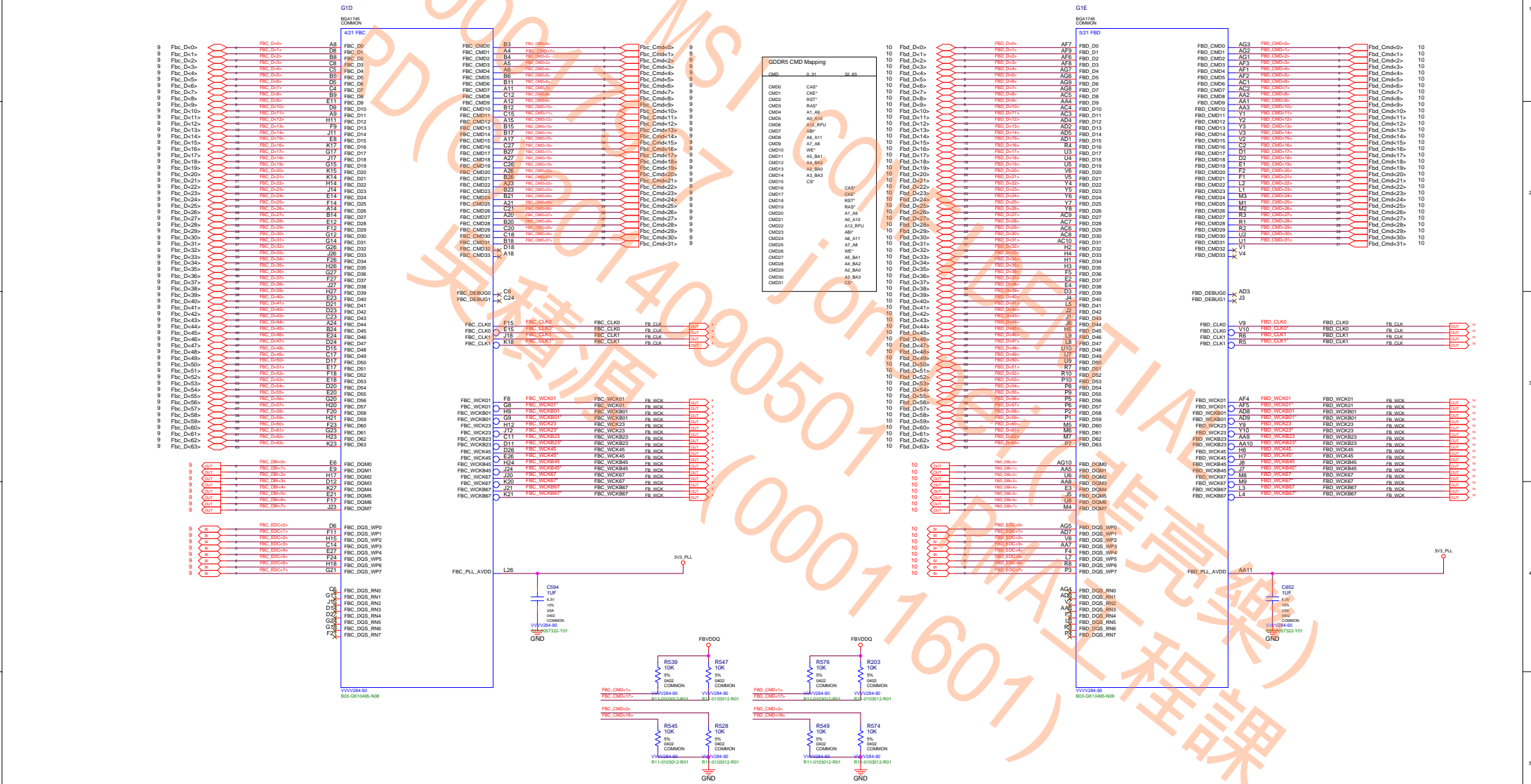








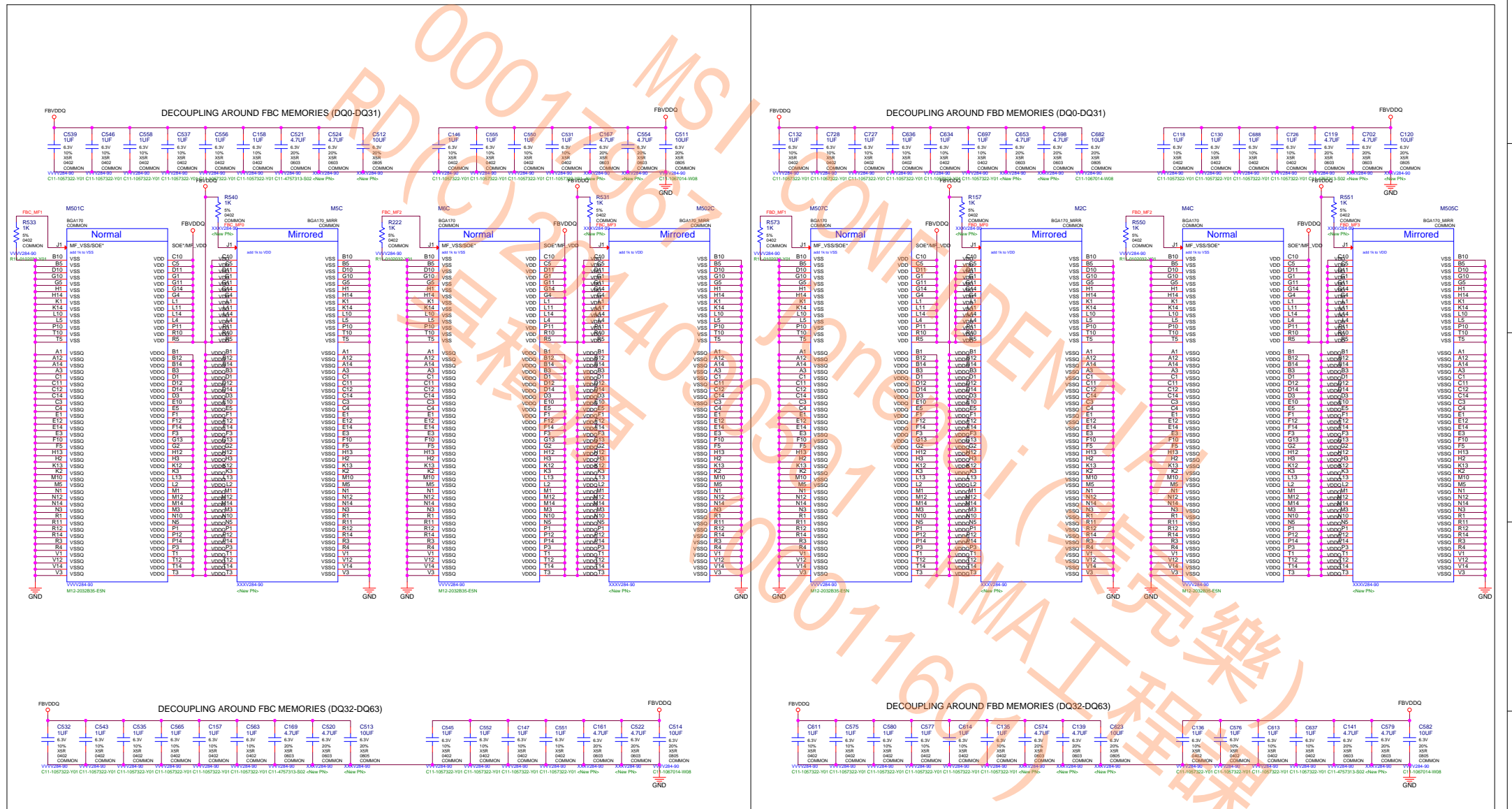




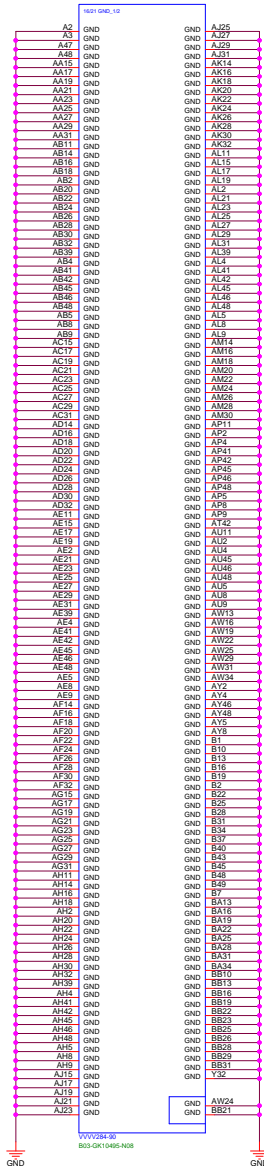




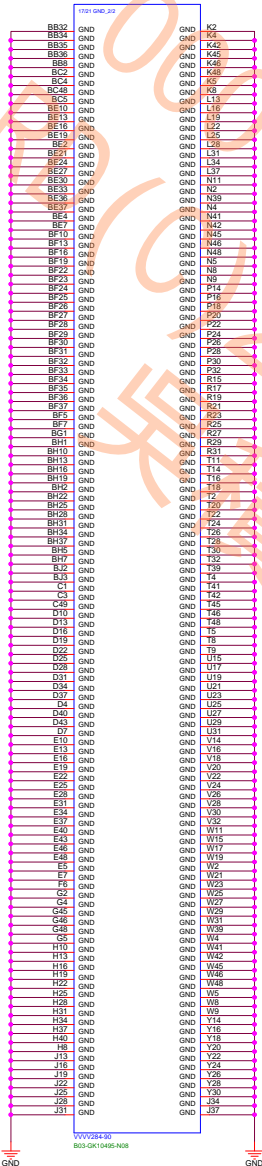




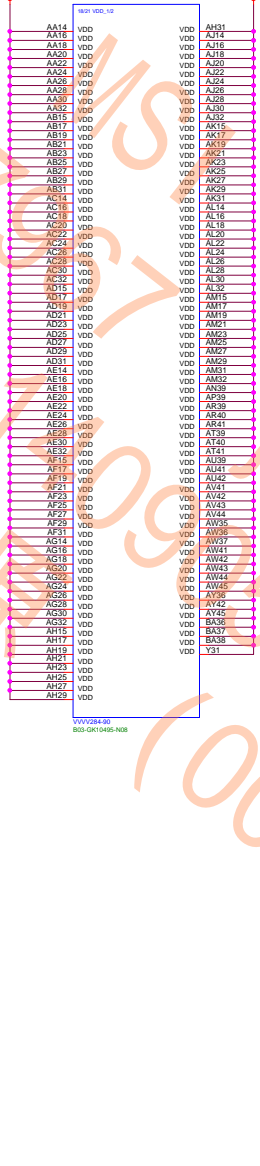
G1F



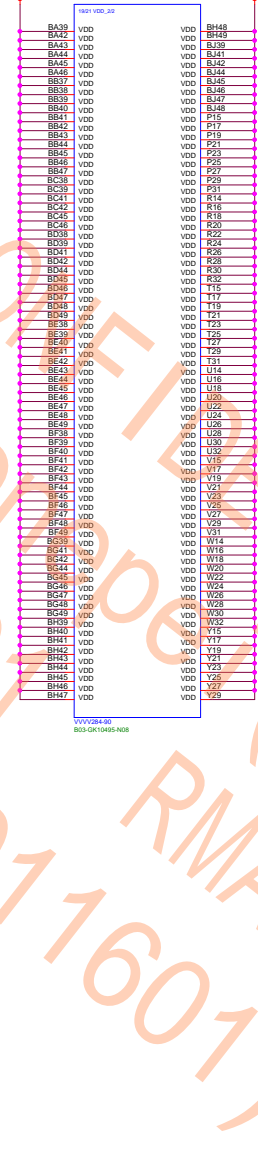
G1G



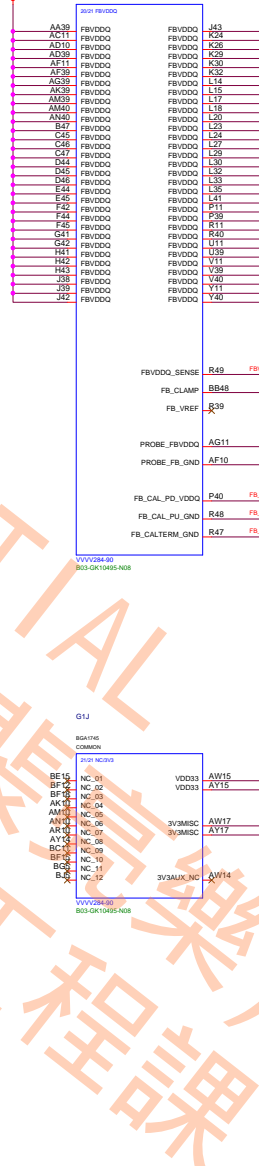
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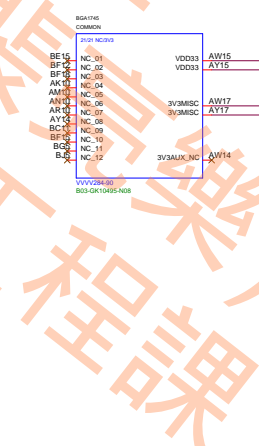
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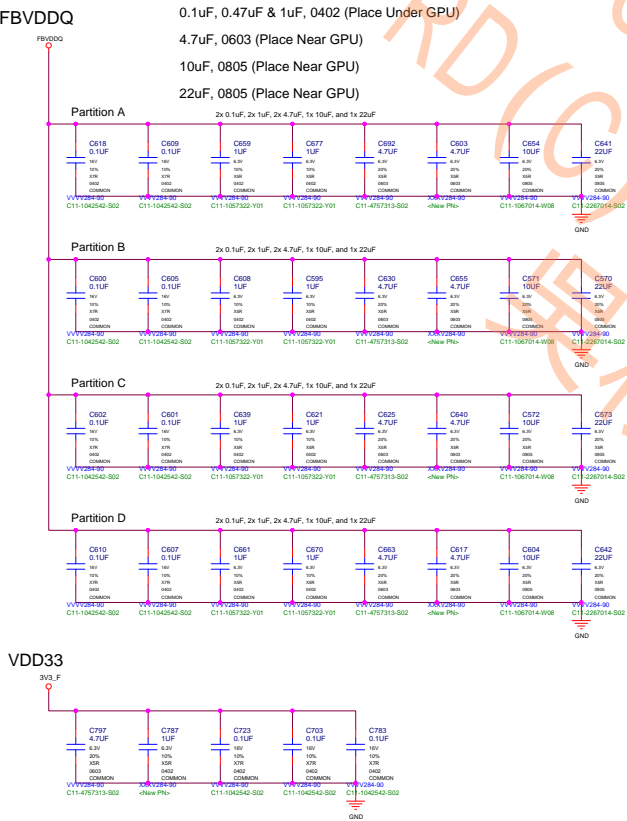
G1K



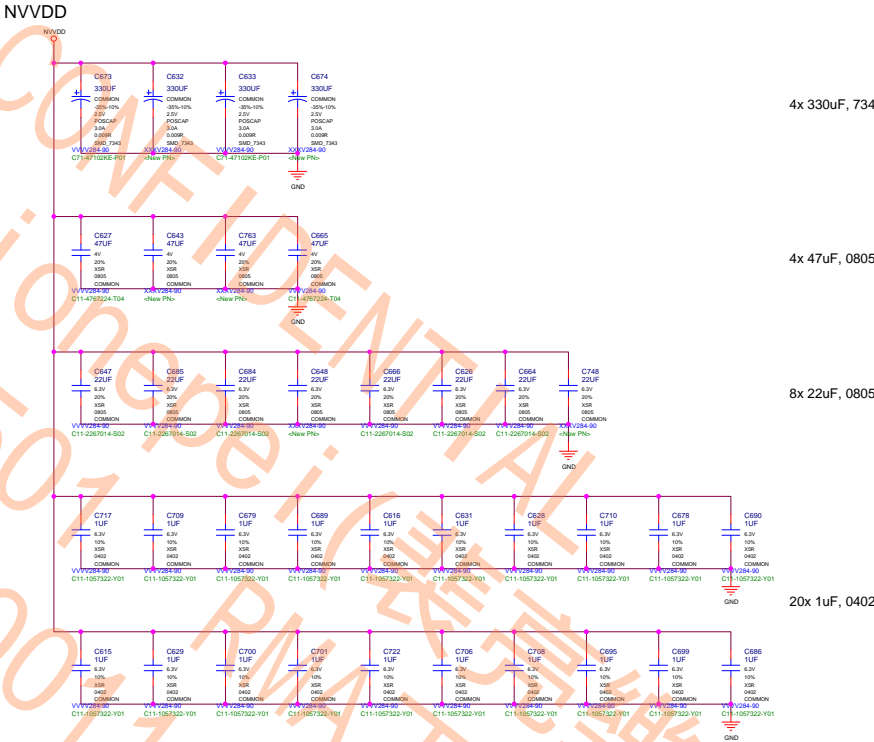
G1J



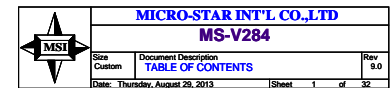
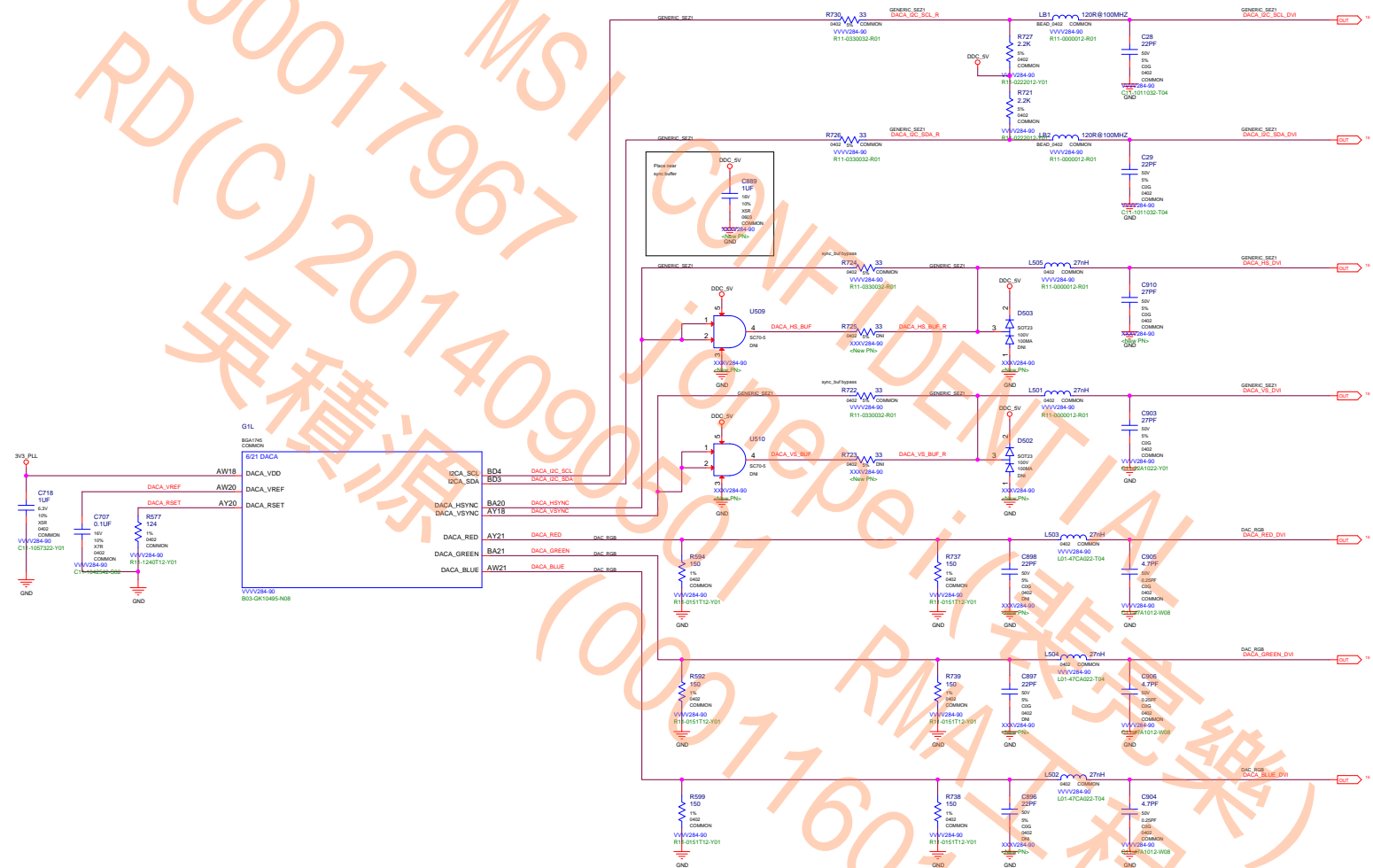
Based on GB2-X GDDR5 FBVDDQ Decap Guideline



NVVDD Decoupling caps. Place under GPU.

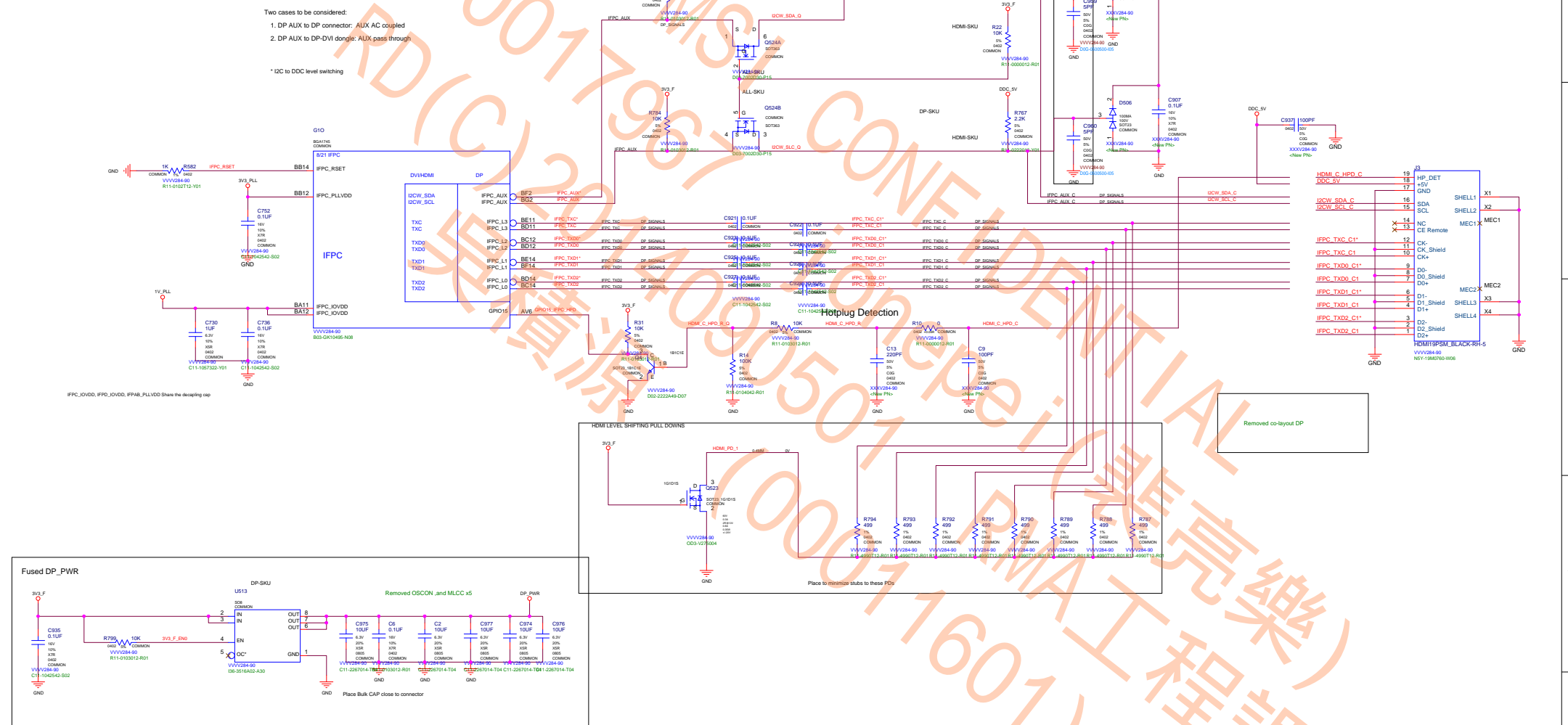




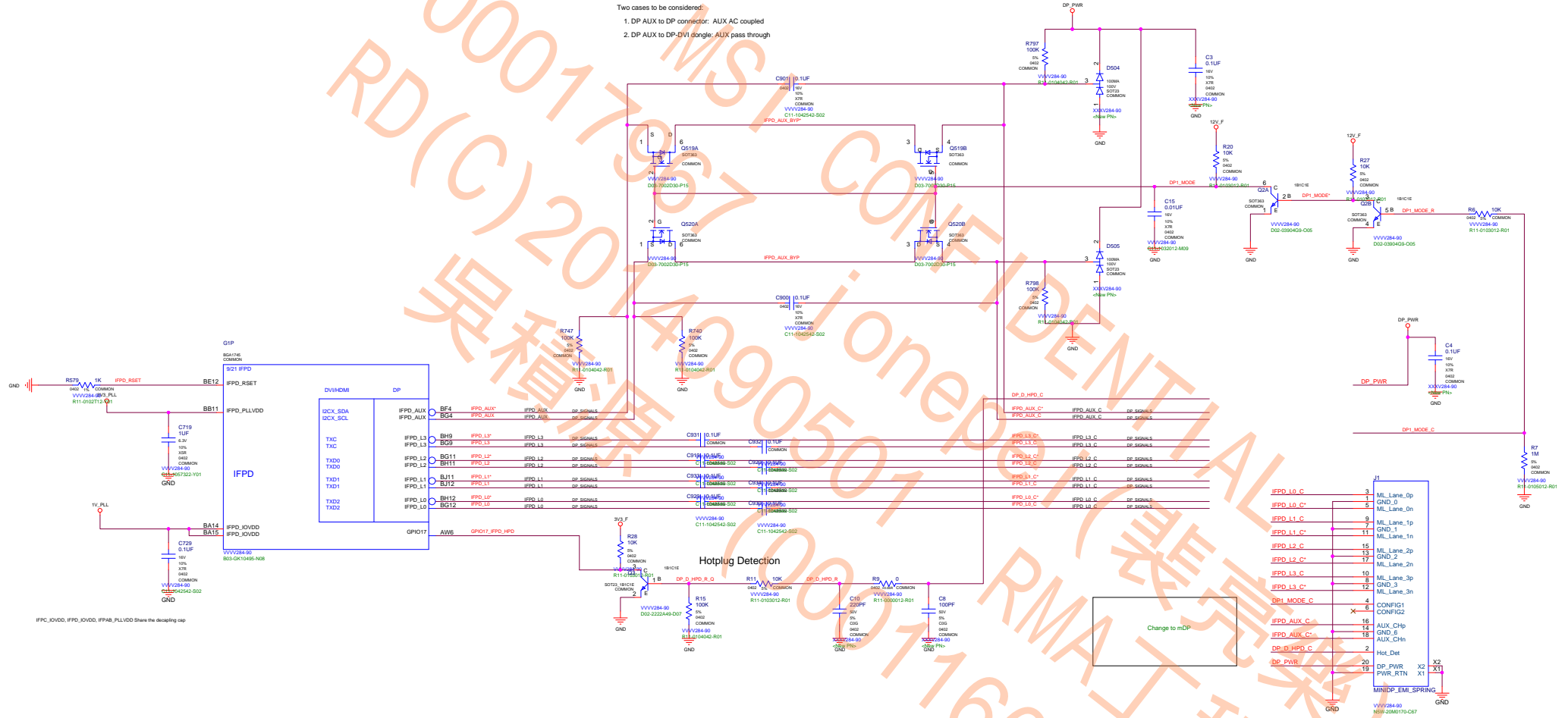








1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-V284</b>		
	Size Custom	Document Description <b>TABLE OF CONTENTS</b>	Rev 9.0
	Date: Thursday, August 29, 2013		Sheet 1 of 32





Removed \* Co-layout resistor one PIN to minimize MIO BUS stub



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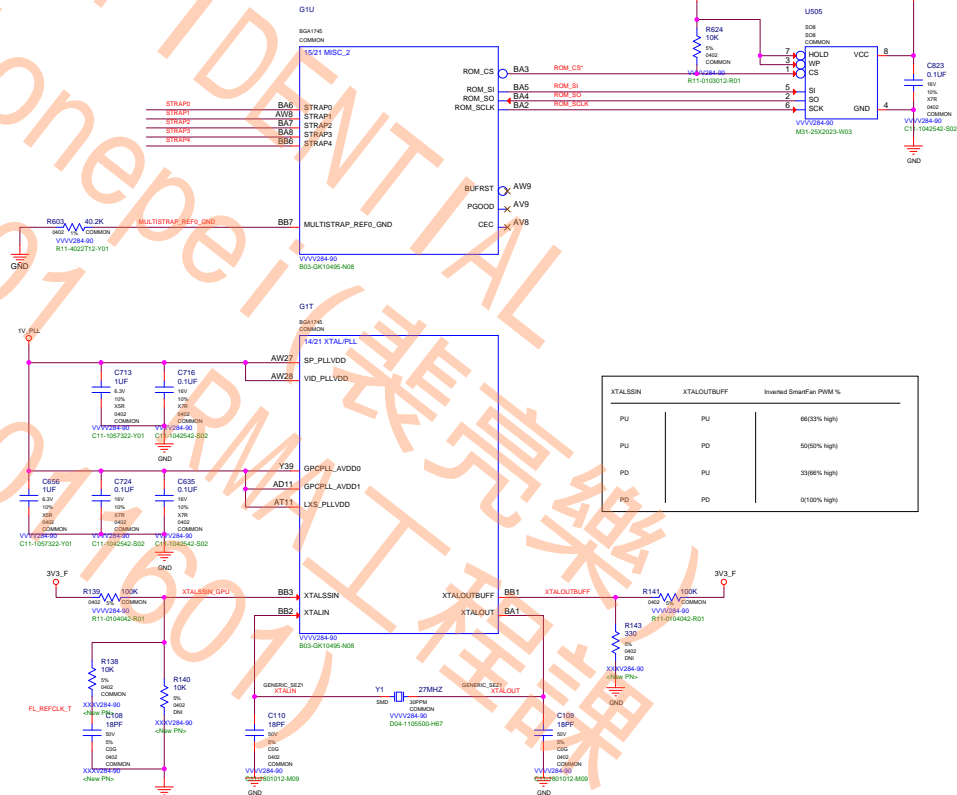
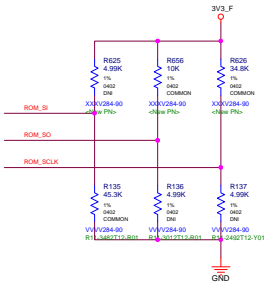
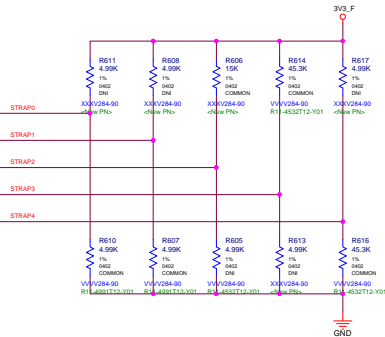


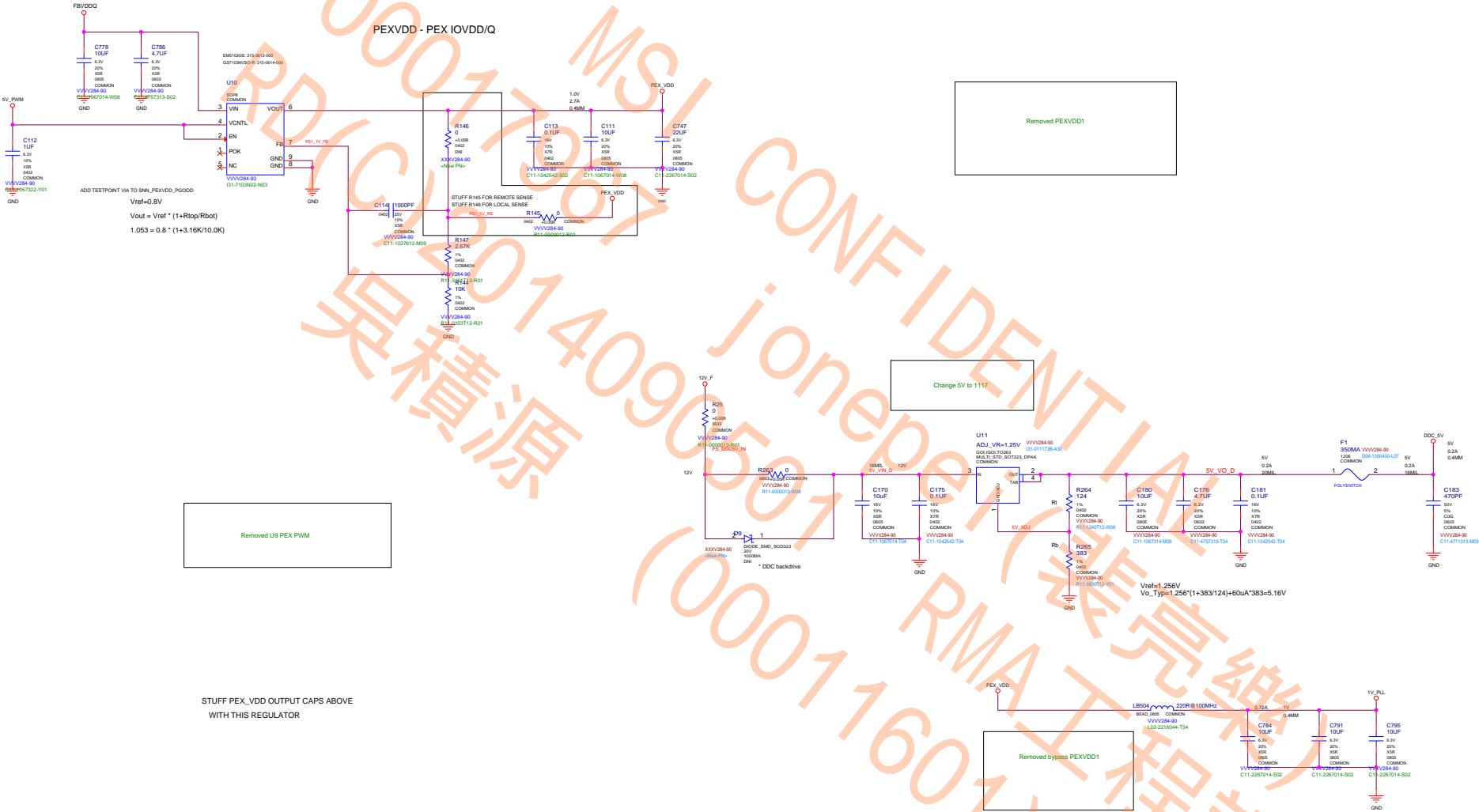
STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	1001 - (0x1189)*	10K PU -325 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		
ROM_SI	RAMCFG[0]*	0*	
	RAMCFG[1]*	1*	64Mx32 256-bit Hynix for SML5 primary memory 35K PD*
	RAMCFG[2]*	1*	
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	30k PD*
	FB[0]_APERTURE_SIZE*	1* For 128MB*	
	FB[1]_APERTURE_SIZE*	0* For 128MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0* DISABLE*	
	PCI_DEVID_EXT[5]*	0* For 0x1189*	25K PD*
	SUB_VENDOR*	1* Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0* For 0x1189*	

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0] Config Width	Vendor
0000	Reserved
0001	32Mx32 256-bit Elpida
0010	32Mx32 256-bit Hynix
0011	32Mx32 256-bit Samsung
0100	Reserved
0101	64Mx32 256-bit Elpida
0110	64Mx32 256-bit Hynix
0111	64Mx32 256-bit Samsung

	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	45.3K 1% TO GND



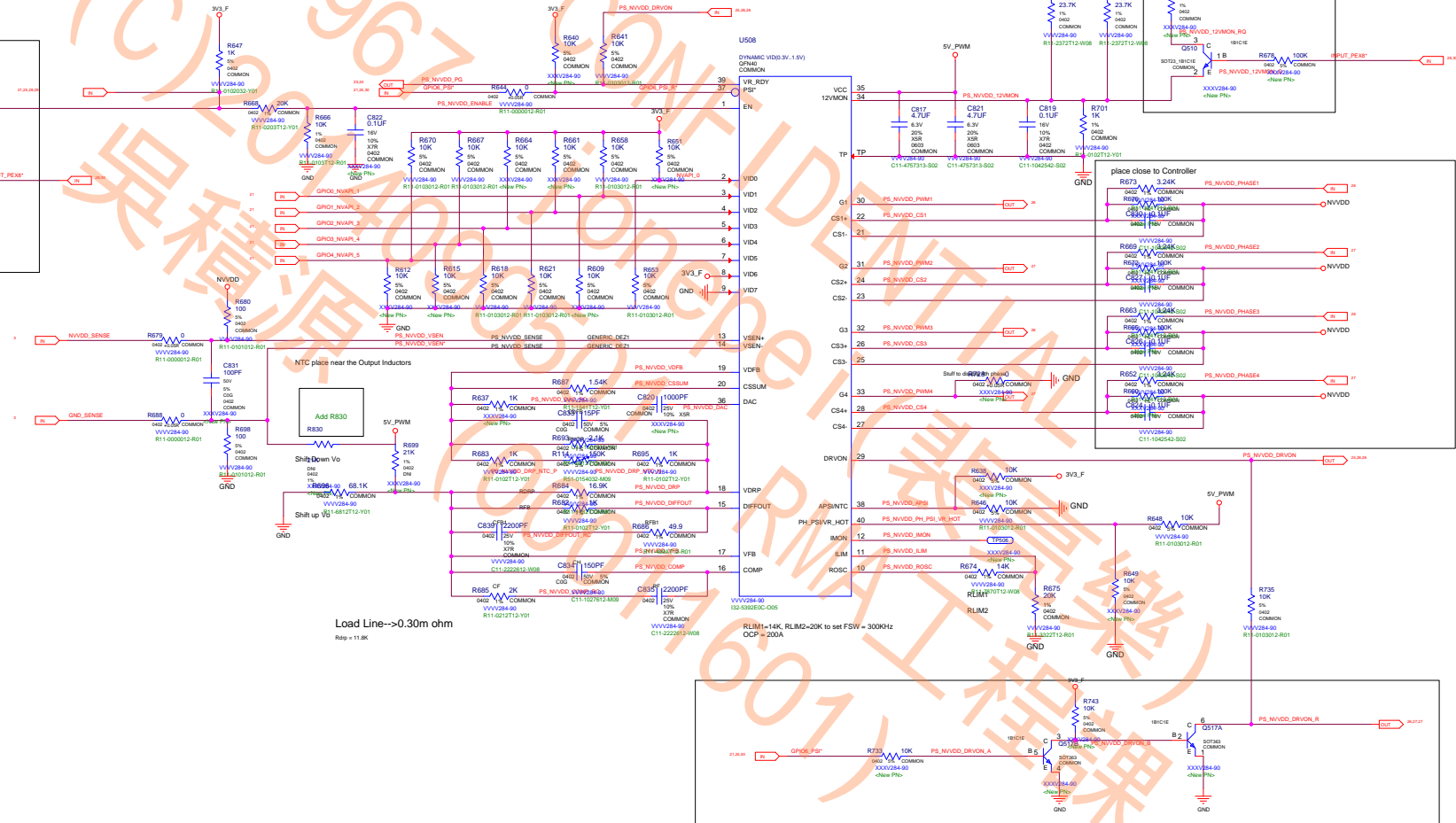
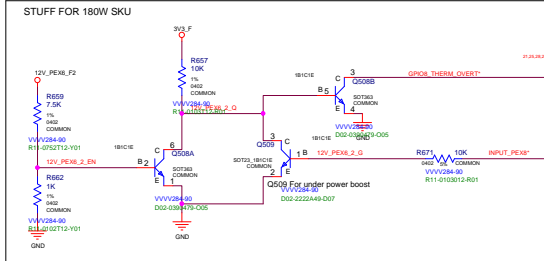




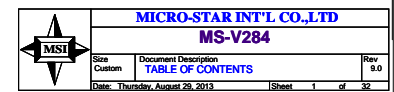


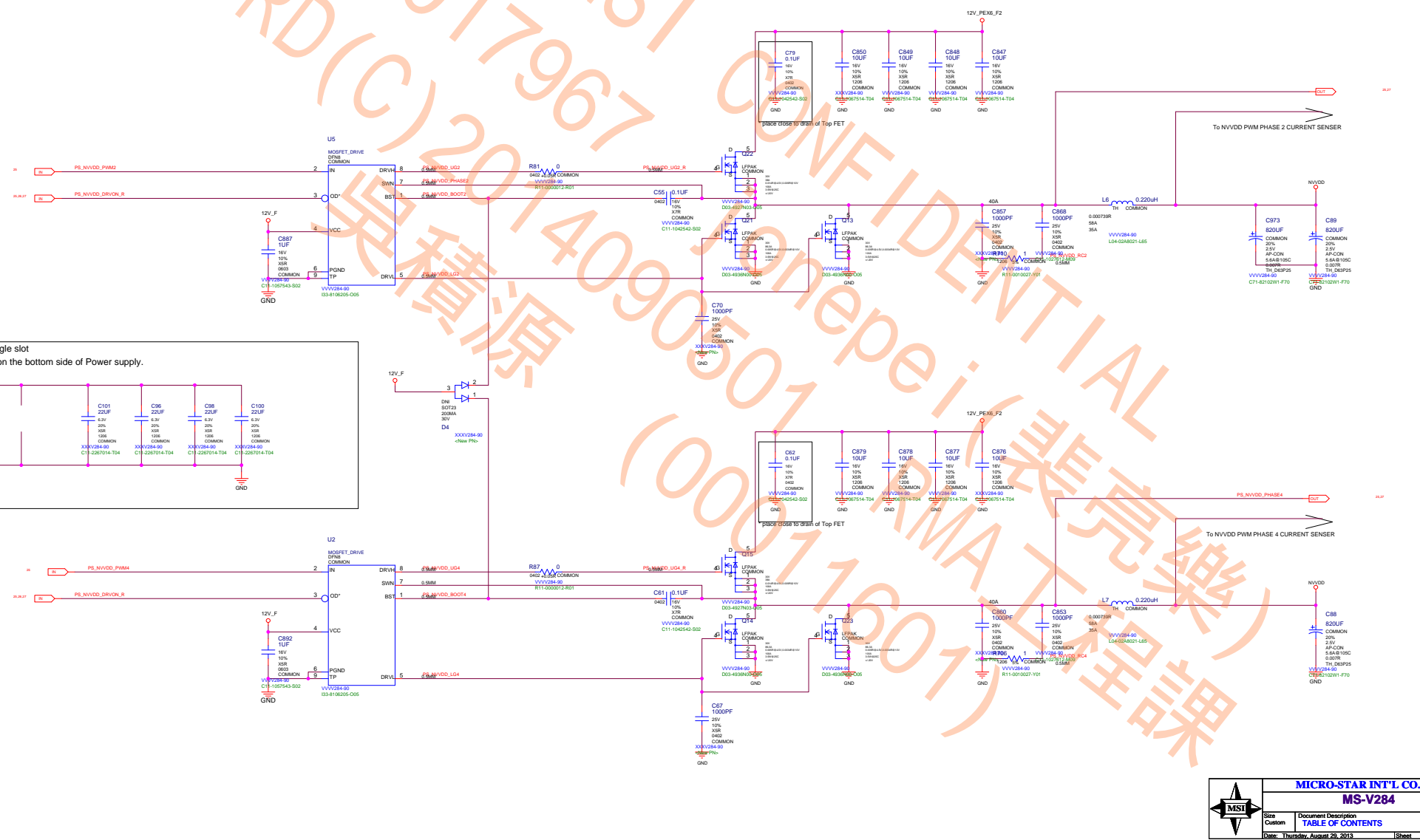
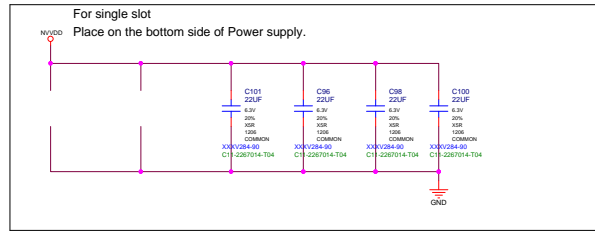
GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

GPIO8\_THERM\_OVERT\*(EN): Combine 3V3\_F and 12V\_PEX\_F2  
Voltage Monitor:USE NCP5392P to Monitor 12V\_F and 12V\_PEX\_F1



Size Custom	Document Description <b>TABLE OF CONTENTS</b>	Rev 9
Date: Thursday, August 29, 2013	Sheet 1 of 32	





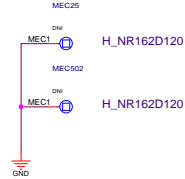
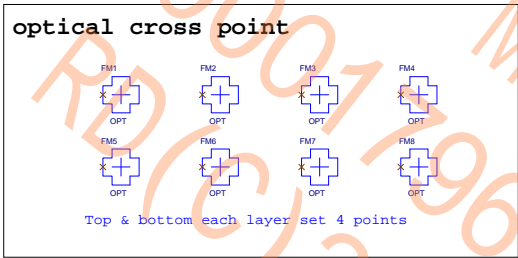
MICRO-STAR INT'L CO.,LTD			
MS-V284			
Size	Custom	Document Description	Rev
TABLE OF CONTENTS			9.0
Date:	Thursday, August 29, 2013	Sheet	1 of 32



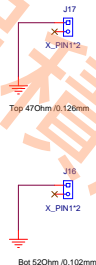
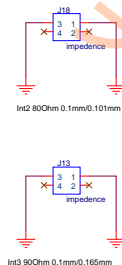








Brackets:



GPU Stiffener:



MOUNTING HOLES FOR HS:

