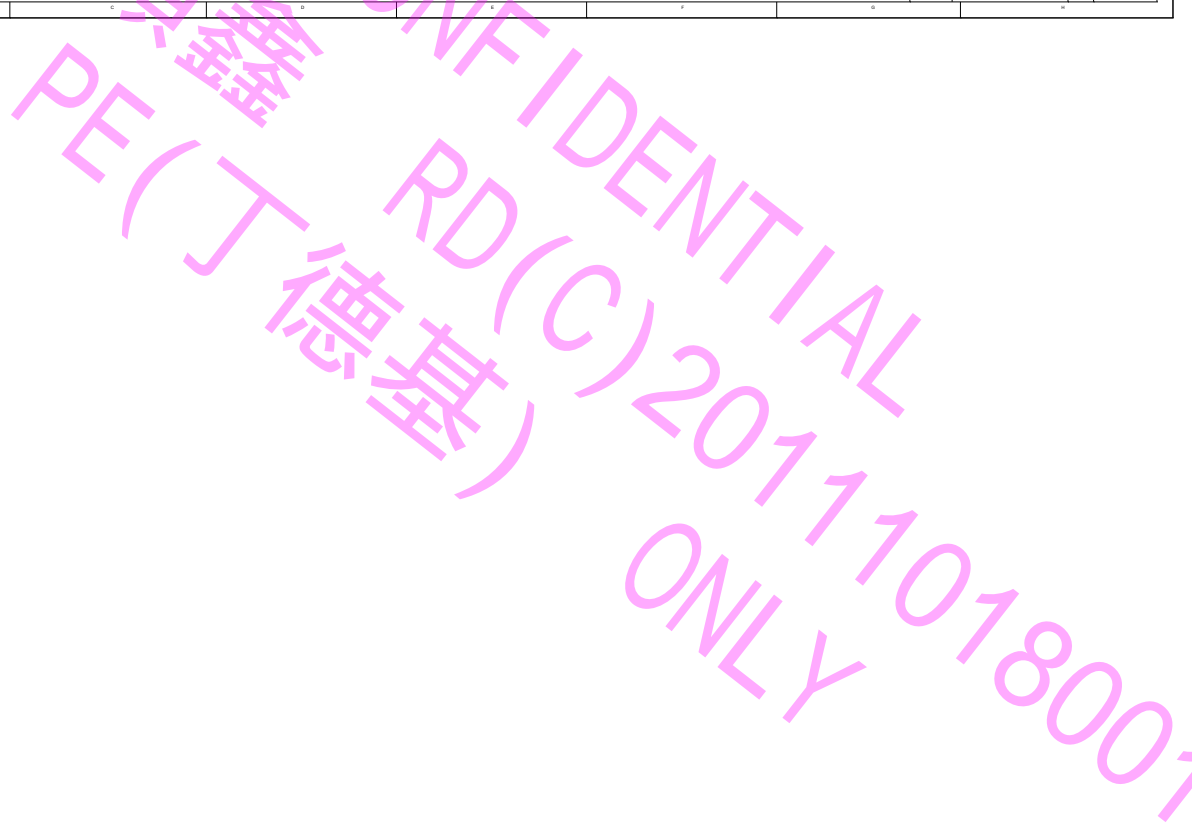
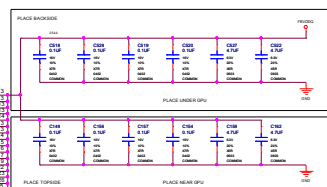
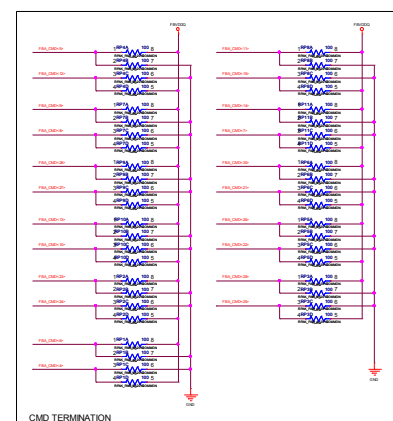
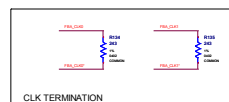
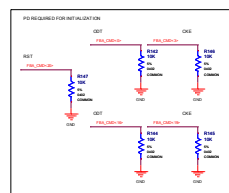
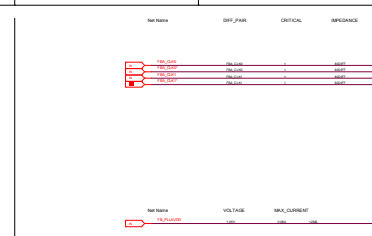





Timing diagram showing the relationship between PEK1\_PRESENT and PEK1\_PLUGGED\_EOP2 signals. PEK1\_PRESENT is a square wave with four pulses. PEK1\_PLUGGED\_EOP2 is a single pulse that occurs during the first PEK1\_PRESENT pulse.

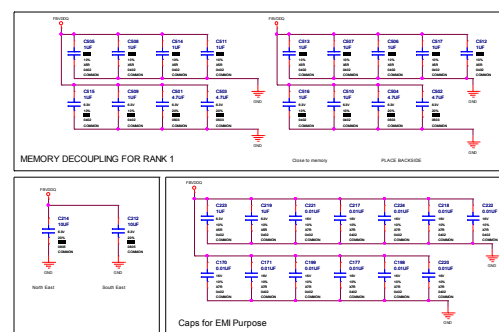
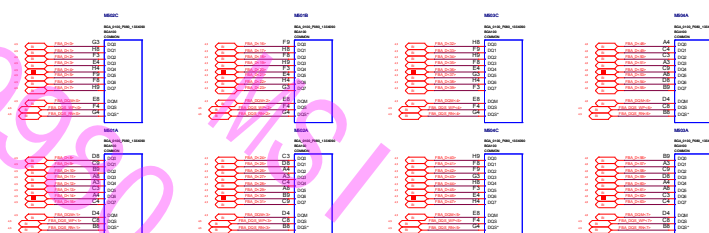
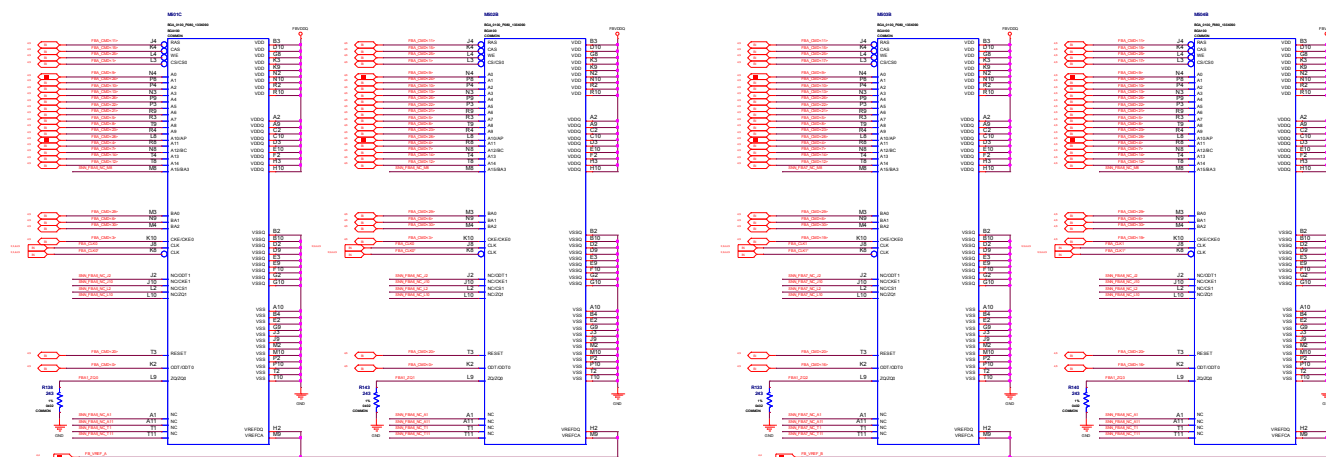



[illegible][illegible]

<b>NVIDIA CORPORATION</b> 3701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA					
NV_P/N		600-11310-BASE-100			
FOUR SIX V		FPGAS/1		PAGE	
ROMREV V		A		DATE	
				08 DEC 2010	



### DDR3 Memories Rank 1



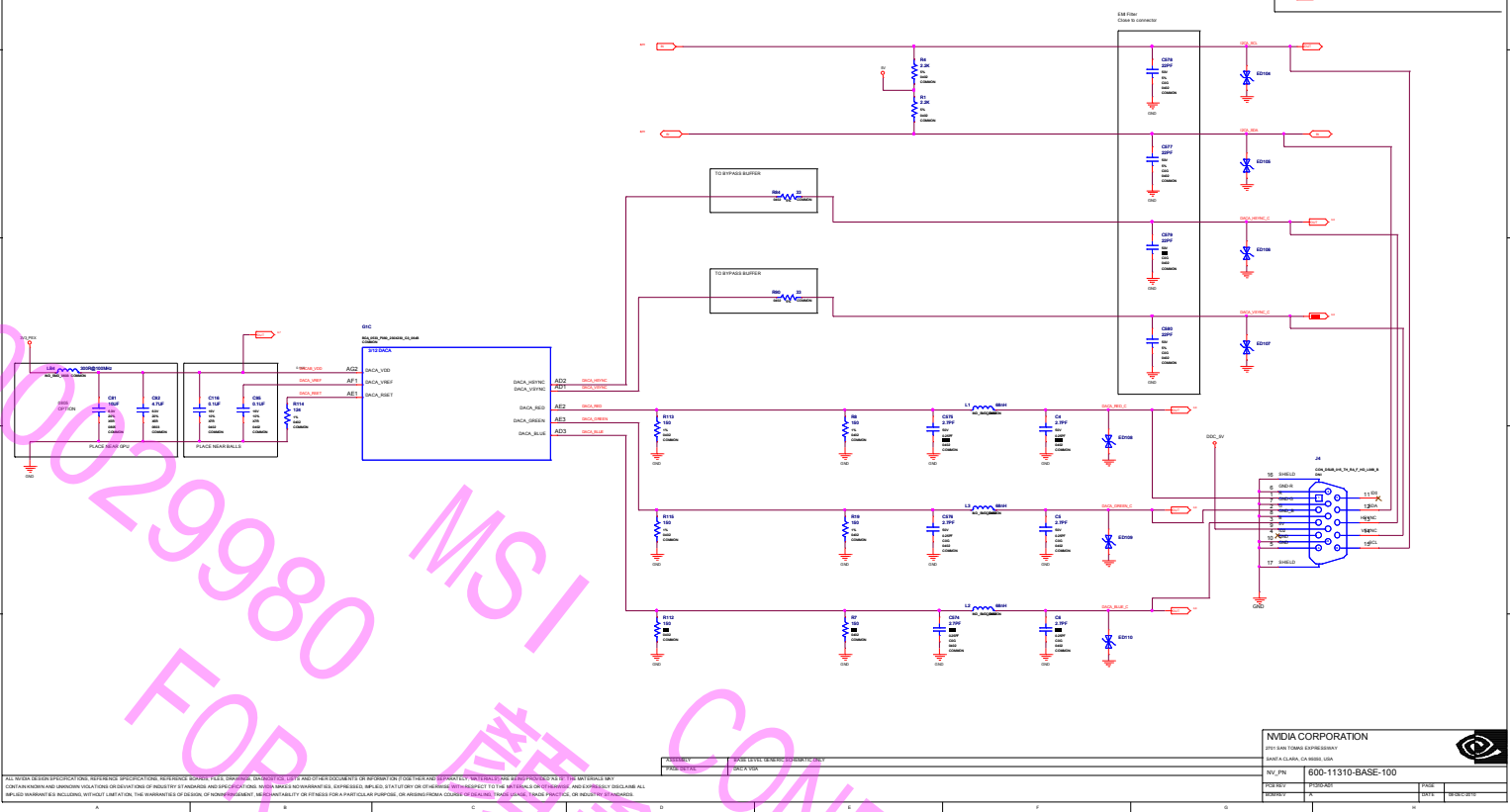
NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN		600-11310-BASE-100	
PCB REV	PCB DATE	PAGE	
REV 0.0	0	DATE	02/25/2005


## DAC A VGA

	Net Name	Critical	Max Delay
1	GPIO_WREN	1	0.000ns
2	GPIO_OENBANK	1	0.000ns
3	GPIO_READ	1	0.000ns
4	GPIO_READ_2	1	0.000ns
5	GPIO_OENBANK_2	1	0.000ns
6	GPIO_READ_3	1	0.000ns
7	GPIO_READING	1	0.000ns
8	GPIO_READING	1	0.000ns
9	GPIO_READING	1	0.000ns
10	GPIO_READING	1	0.000ns
11	GPIO_READING_2	1	0.000ns
12	GPIO_READING_3	1	0.000ns

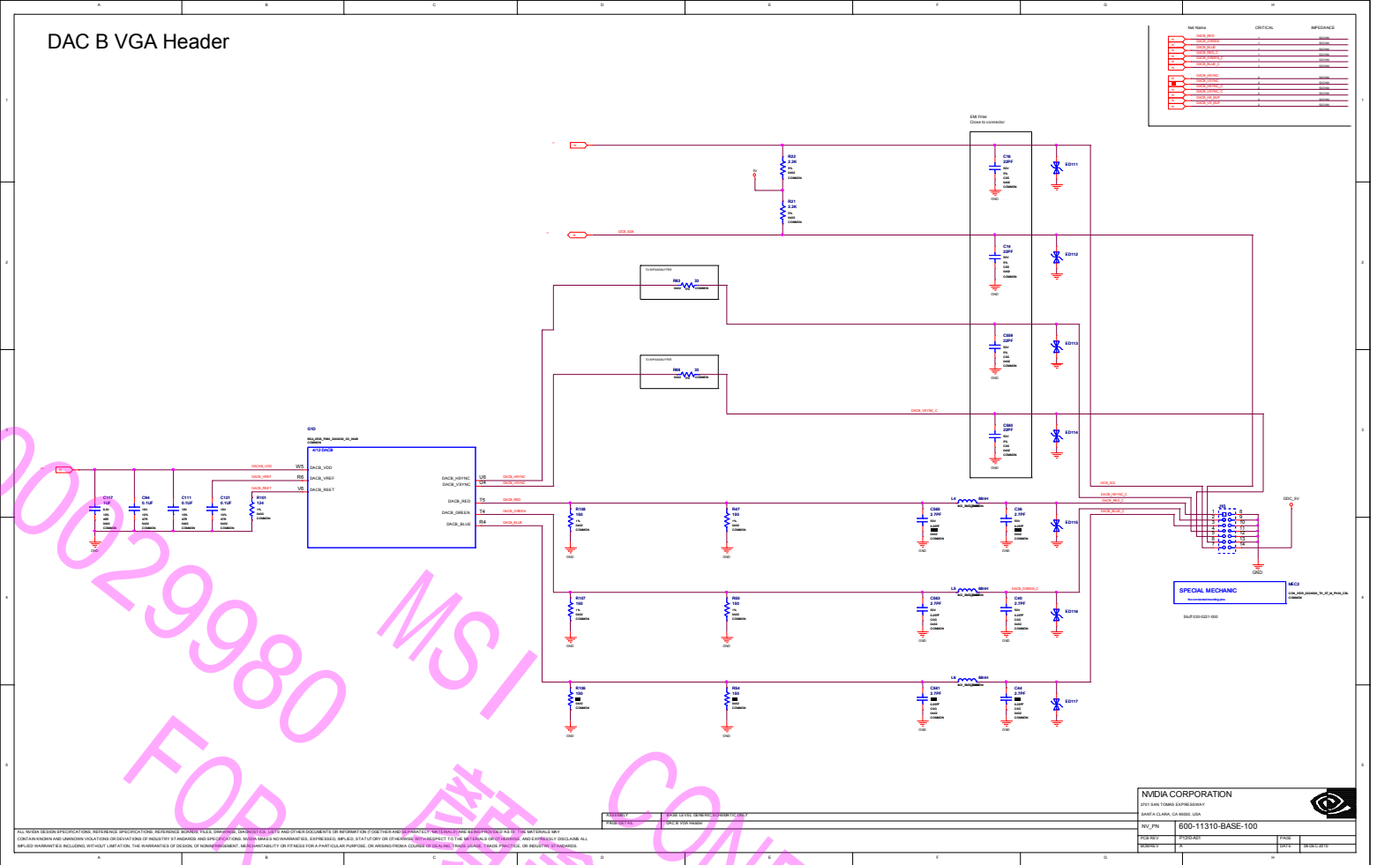
  

	Net Name	Min Width	Max Current
1	GPIOA_VDD	1.00V	0.00A



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NV_PN	600-11310-BASE-100		
FOR REV	P100-AD1	PAGE	
DATE REV	A	DATE	08/04/2010

## DAC B VGA Header







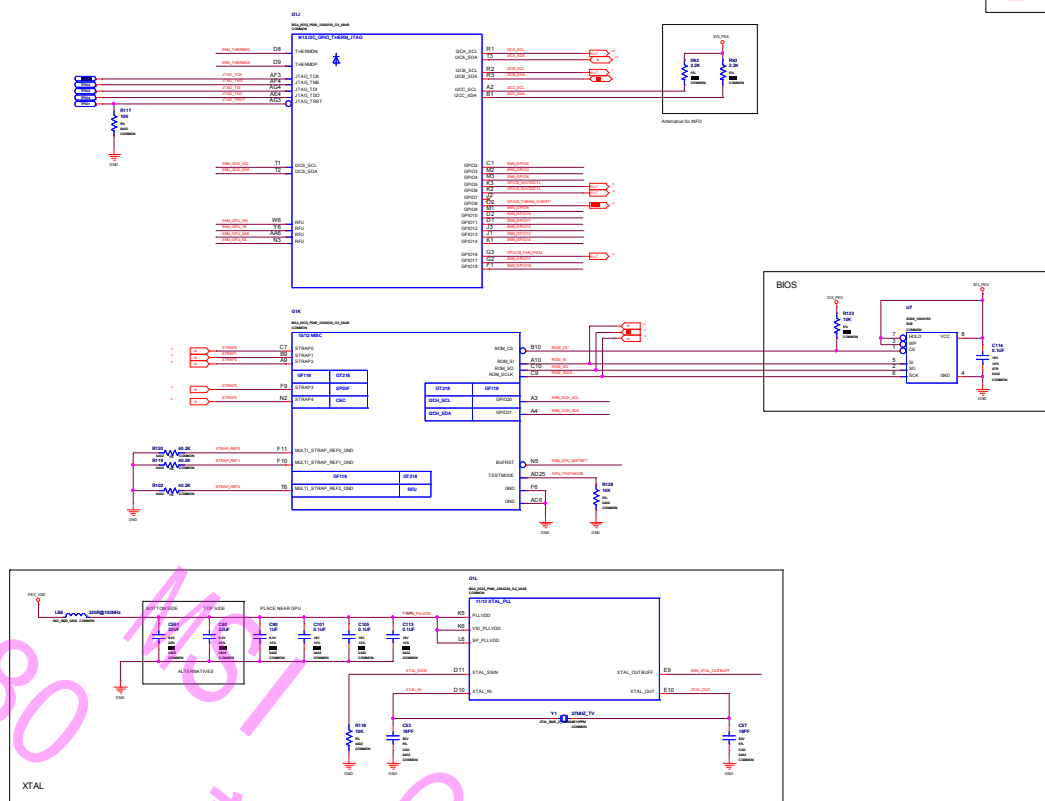





NetName		DIF_PAIR	CRITICAL	IMPEDANCE
10	IC1A_OUT	20n	1	100pF
10	IC1A_IN	20n	1	100pF

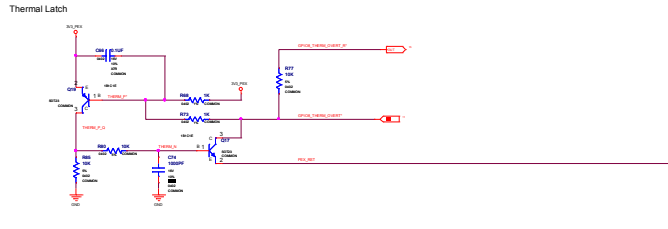
NetName		VOLTAGE	MAX_CURRENT
10	OPAMP_POWER	1.8V	100mA
10	IC1A_V		100mA



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NV_PIN	<b>600-11310-BASE-100</b>	
PCH_REV	PCH_REV	PAGE
BIOS_REV	BIOS_REV	BIOS_REV

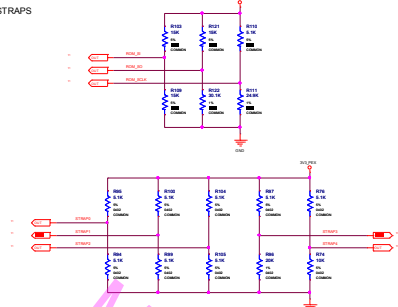
										<b>NVIDIA CORPORATION</b> <small>2005 LAKE TOWN DRIVE SANTA CLARA, CA 95051, USA</small>			
										<b>600-11310-BASE-100</b>			
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Thermal Protection, Protected 3V3, Straps, Fan



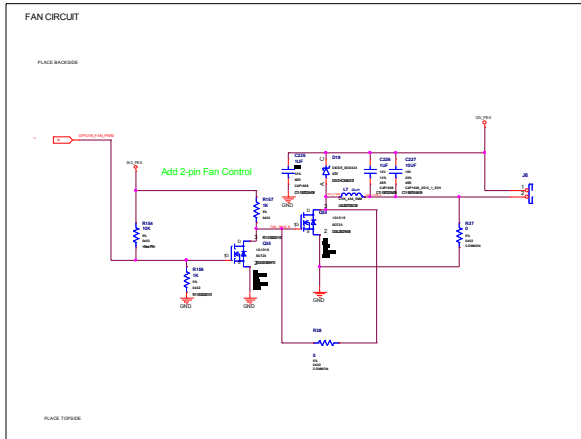
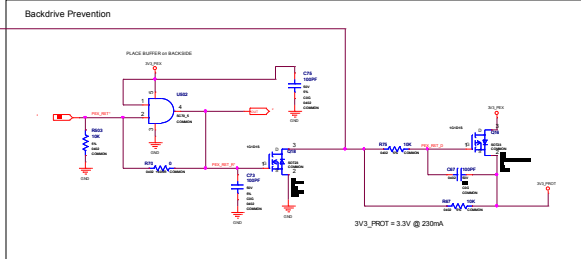
STRAPS

Strap	PIN	Level
0	PD 5A	
1	PD 10A	
2	PD 15A	
3	PD 20A	
4	PD 25A	
5	PD 30A	
6	PD 35A	
7	PD 40A	
8	PU 5A	
9	PU 10A	
A	PU 15A	
B	PU 20A	
C	PU 25A	
D	PU 30A	
E	PU 35A	
F	PU 40A	



STRAP PIN MODE TABLE

	PIN NAME	MULTILEVEL IN (S)	BINARY PRODUCTION	BINARY SRINGUP
GF19	STRAP0	USER[0]	RAMCFG0	3G0_PACCFG_LUT_ADR0
	STRAP1	3G0_PACCFG_ADR[0]	RAMCFG1	3G0_PACCFG_LUT_ADR1
	STRAP2	PO_DEV[0]	RAMCFG2	3G0_PACCFG_LUT_ADR2
	STRAP3	SOE[0]	TBD	TBD
GF19	STRAP4	RESERVED/RESERVED/POE_MAX_SPEED/DP_PLL_VDD33V	TBD	TBD
	ROM_SCLK	POE_VEN[4] SUB_VEND[0] SCLK_PU_LUT_TERM	POE_DEV[0]	3G0_PACCFG_LUT_ADR3
	ROM_S0	RAMCFG[0]	POE_DEV[EXT]	SUB_VEND[0]
	ROM_S0	XCLK_417_FBS_BAR_SIZE 8MB_ALT_ADDR_VGA_DEVICE	XCLK_417	XCLK_277
GF19	ROM_S0	POE[1] POE[0] SUB_VEND[0] SCLK_PU_LUT_TERM	TBD	TBD



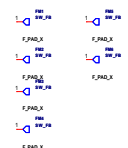
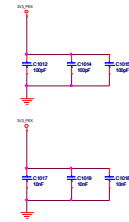
NVIDIA CORPORATION

600-11310-BASE-100

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NVIDIA CORPORATION  
200 LAW STREET, SANTA CLARA, CA 95051, USA

MODEL: 600-11310-BASE-100

DATE: 10/18/2011

REVISION: 1.0

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<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
<b>NV_PN</b>		<b>600-11310-BASE-100</b>	
<b>PCB REV</b>	<b>P100-AD1</b>	<b>PAGE</b>	
<b>BOARD V</b>	<b>A</b>	<b>DATE</b>	<b>08/03/2010</b>

