

G94-P545-A01 - GDDR3, DVI /VGA + DVI /VGA + HDTV/SDTV-Out

SKU	VARI ANT	NVPN	ASSEMBLY
8	BASE	600-10545-base-100	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU9100	600-10545-9100-100	G94-400 650MHz/1000MHz 512MB 16Mx32 BGA136 GDDR3, DVI -I -DL+DVI -I -DL+HDTV-Out (Bring Up SKU)
2	SKU0000	600-10545-0000-100	G94-400 650MHz/1000MHz 512MB 16Mx32 BGA136 GDDR3, DVI -I -DL+DVI -I -DL+HDTV-Out
3	SKU0010	600-10545-0010-100	G94-300 500MHz/800MHz 512MB 16Mx32 BGA136 GDDR3, DVI -I -DL+DVI -I -DL+HDTV-Out
4	SKU0020	600-10545-0020-100	G94-200 500MHz/800MHz 384MB 16Mx32 BGA136 GDDR3, DVI -I -DL+DVI -I -DL+HDTV-Out
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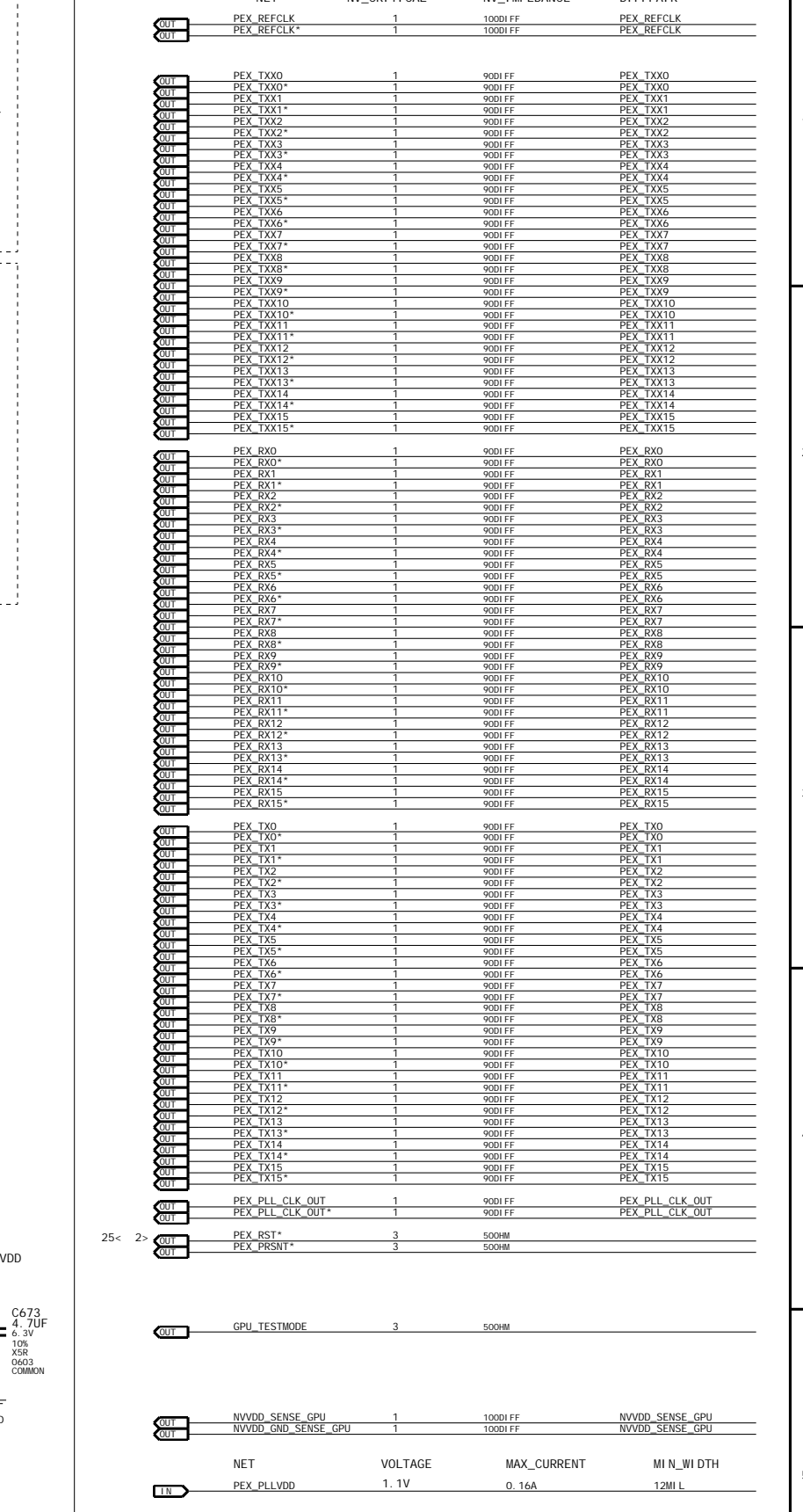
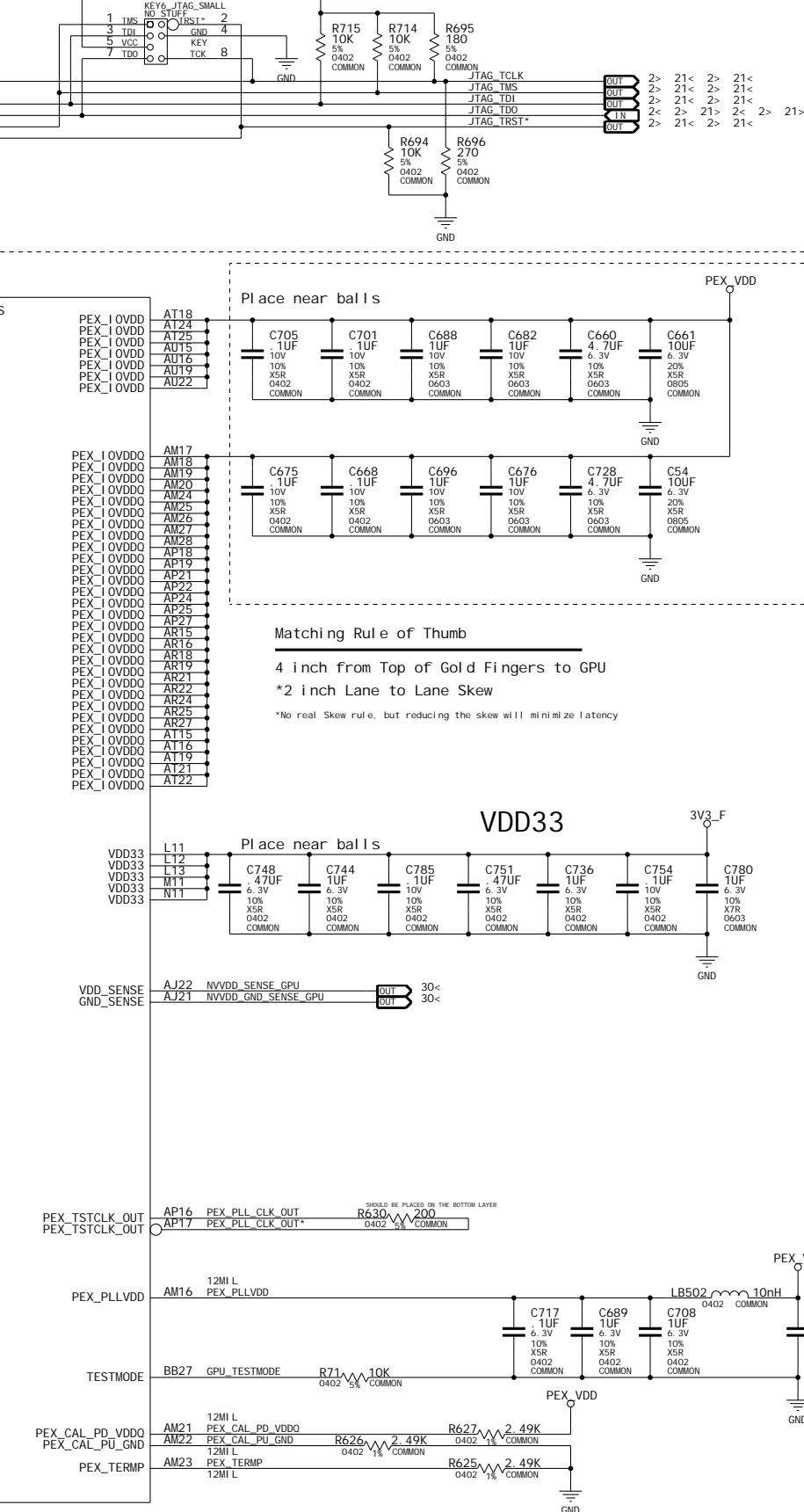
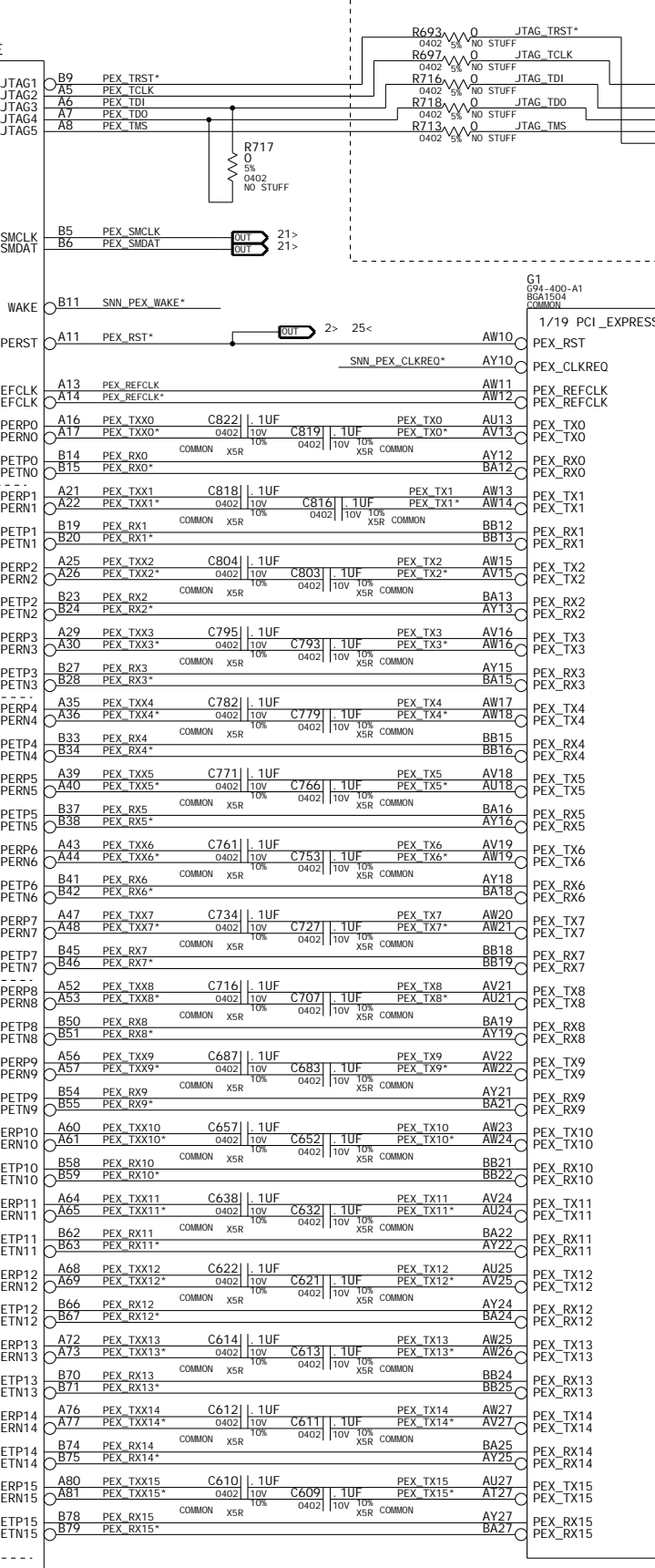
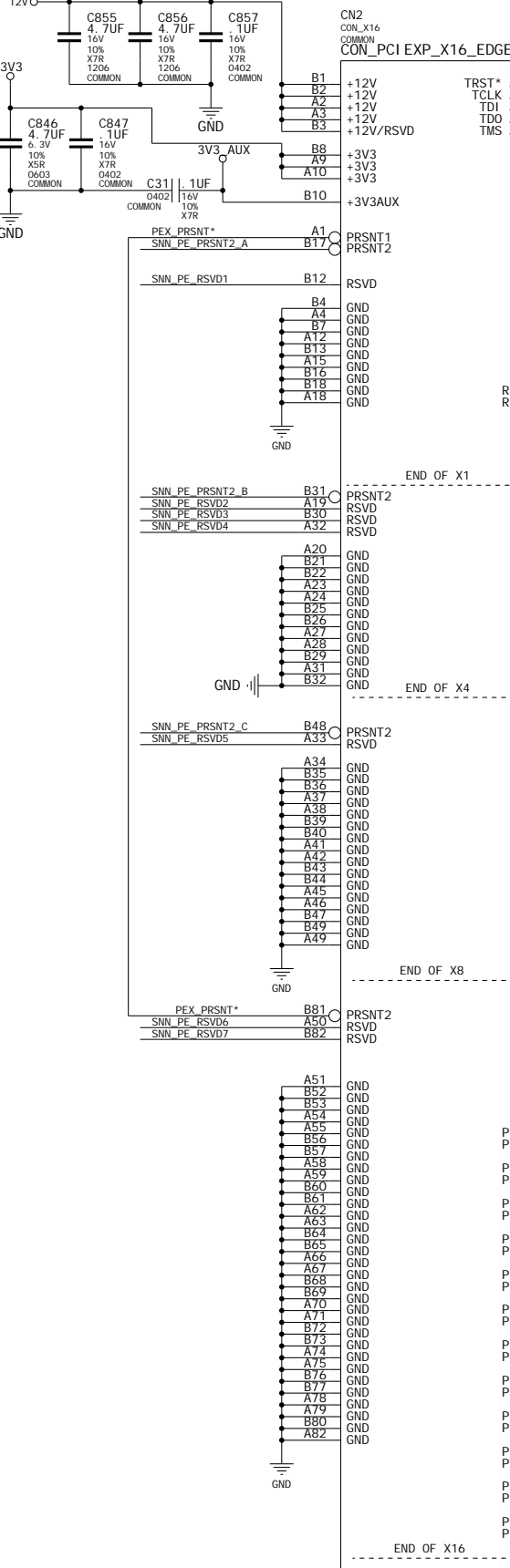
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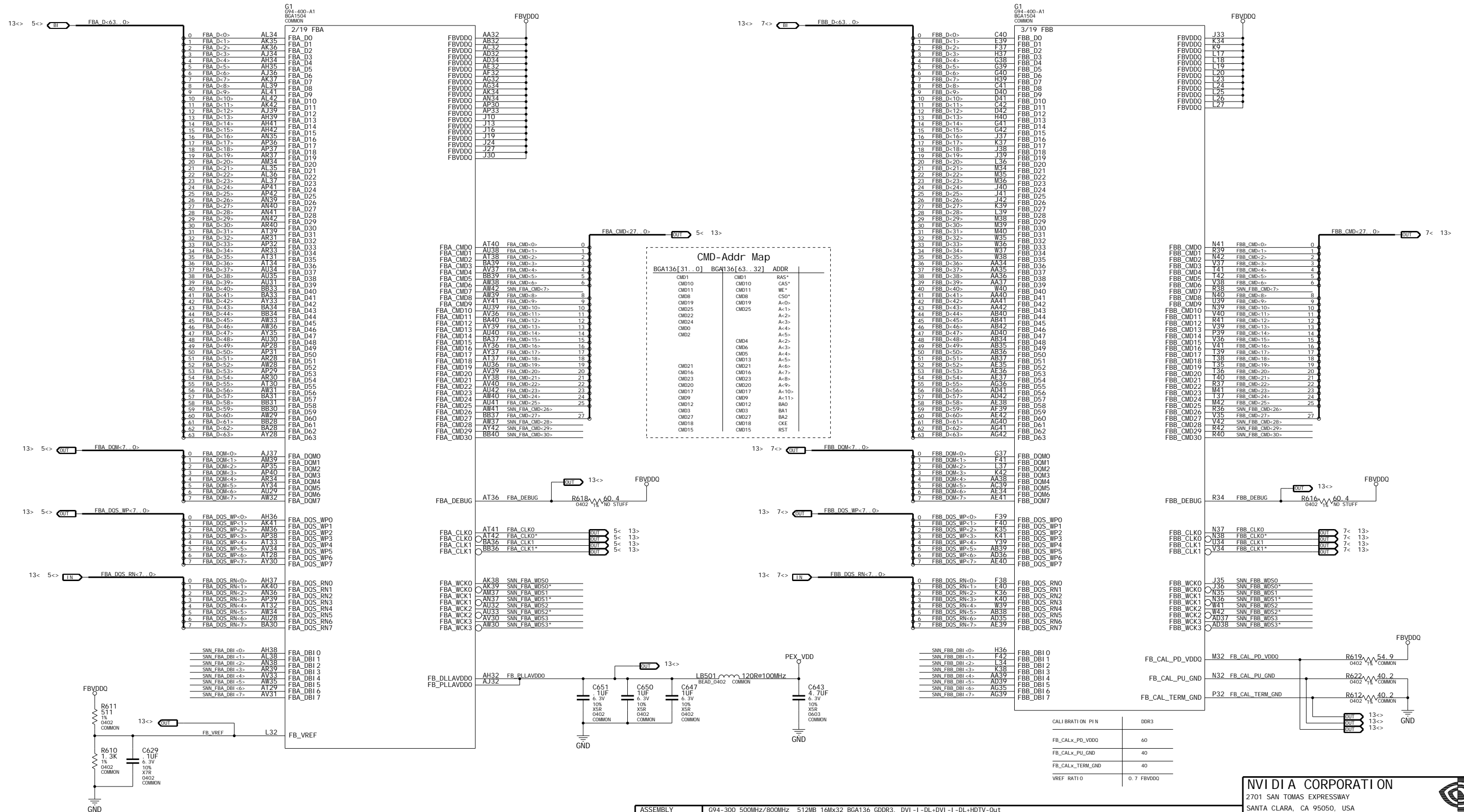
Page 32: Thermal , Mechanical , and Bracket

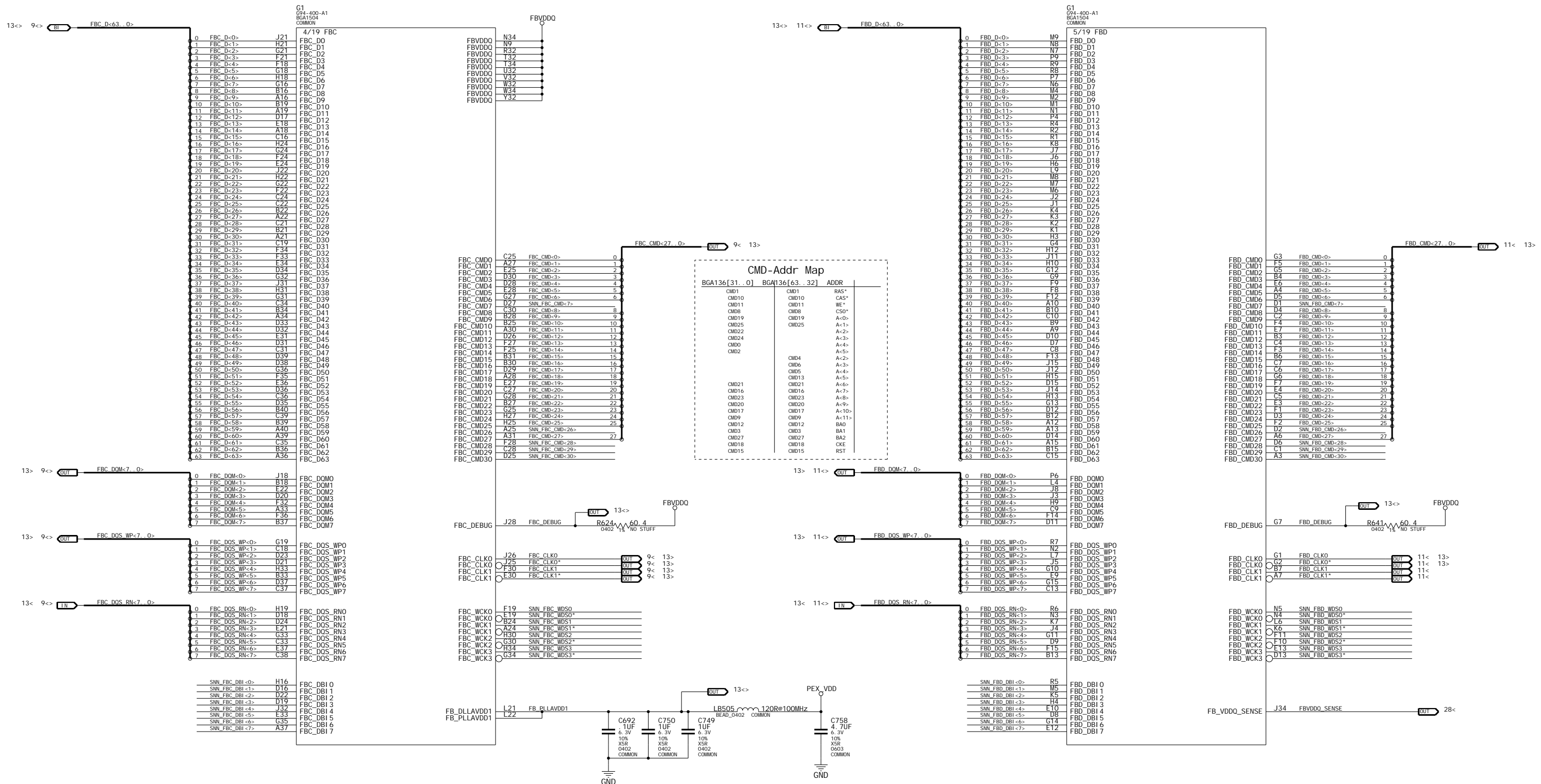
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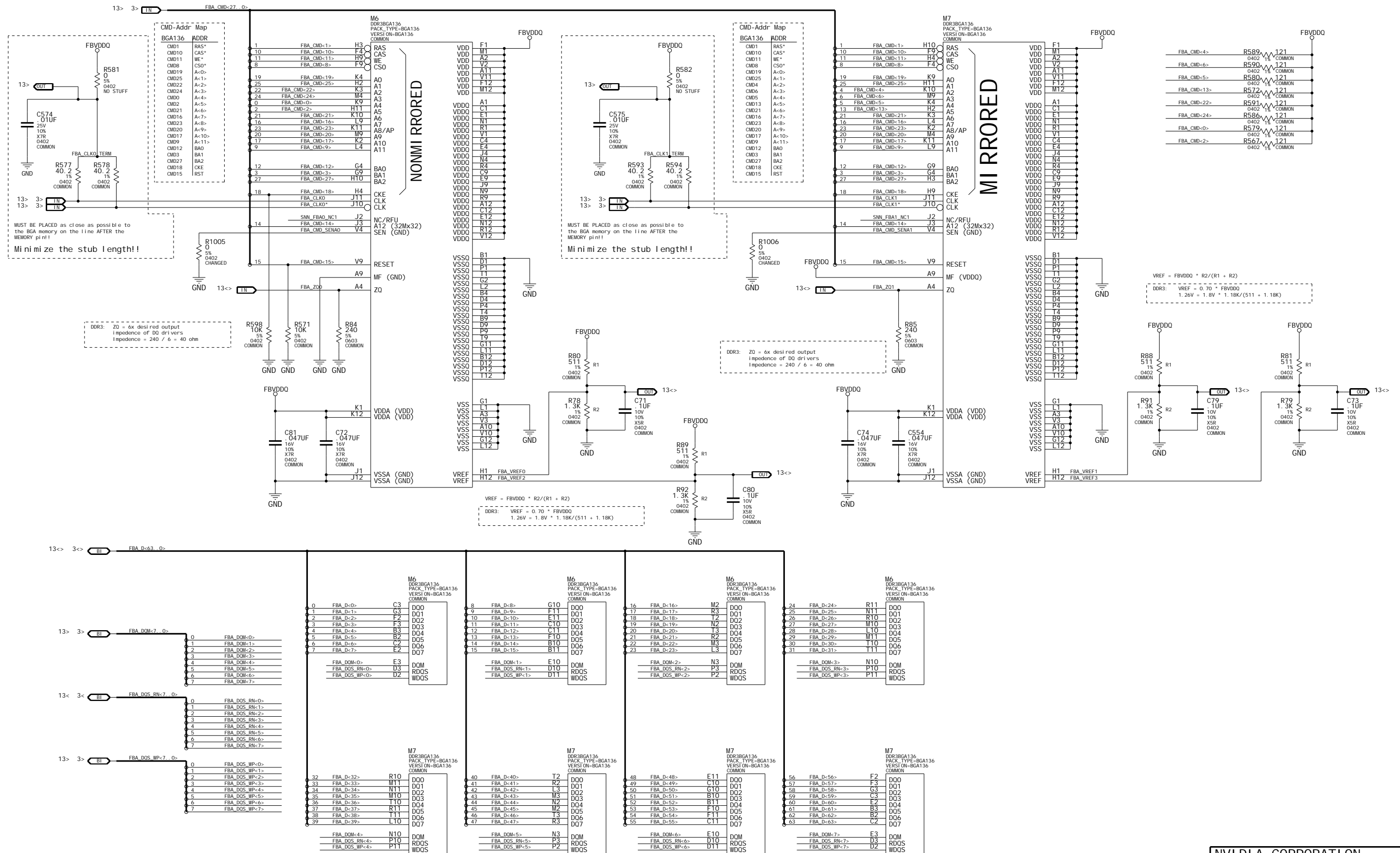
Page2: PCI Express



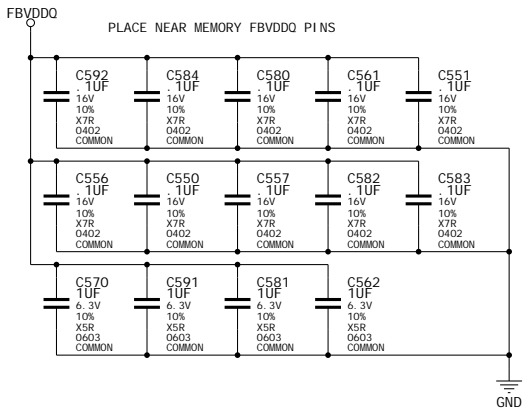




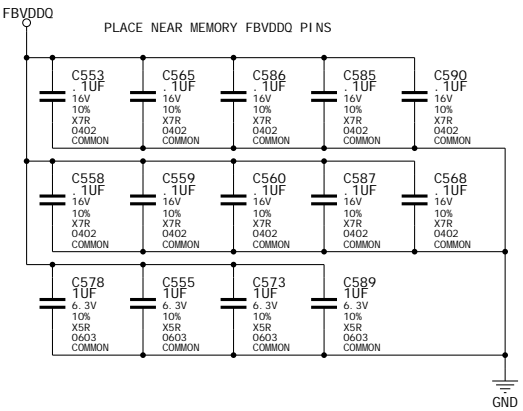
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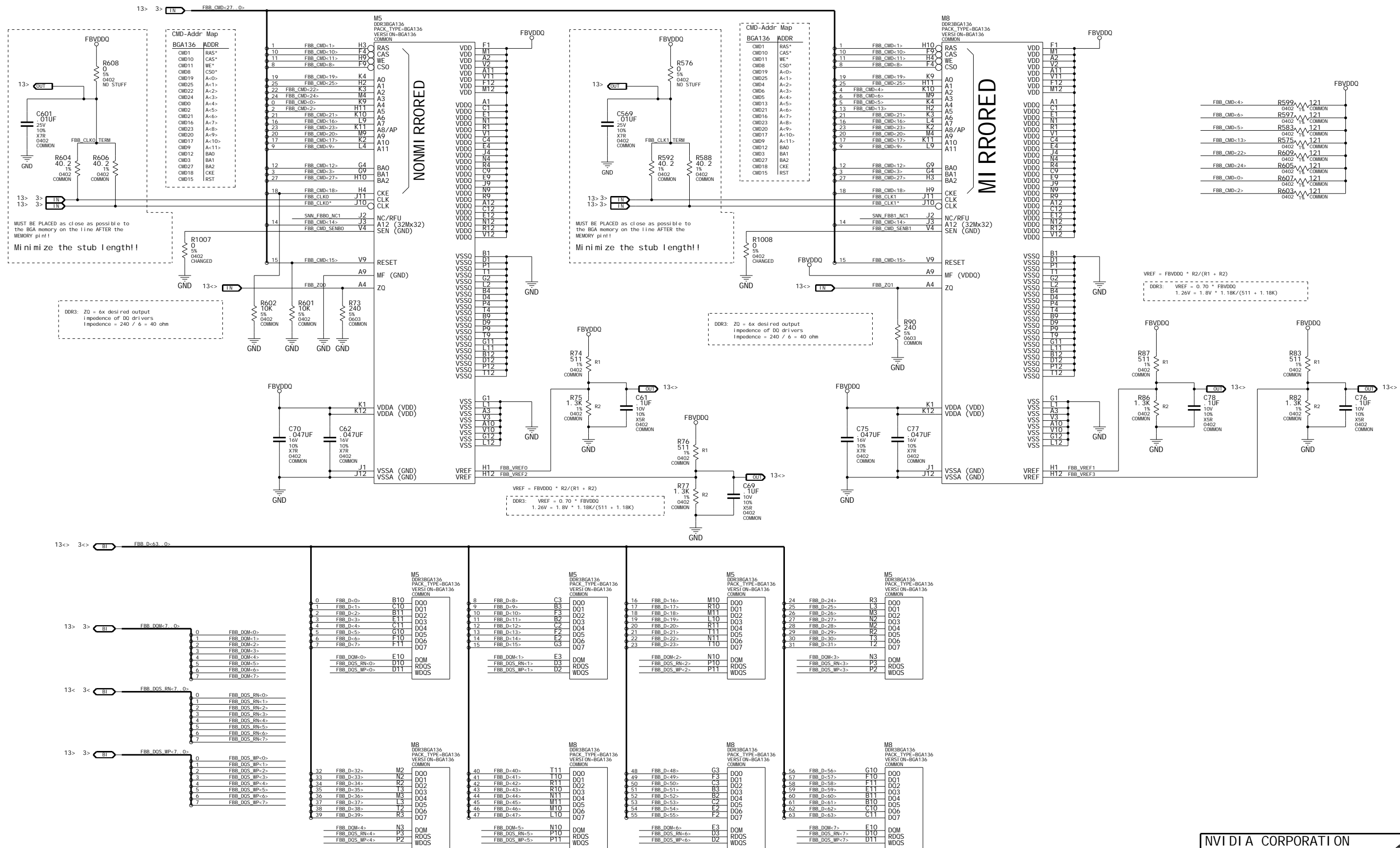


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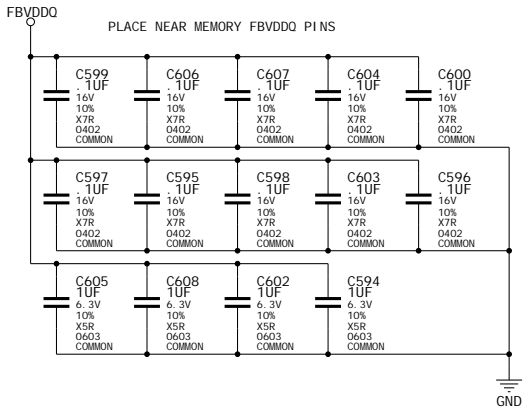


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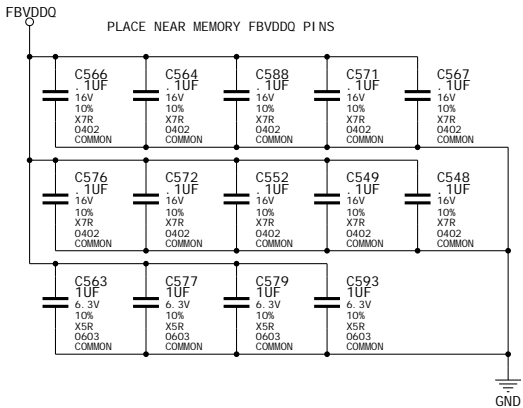


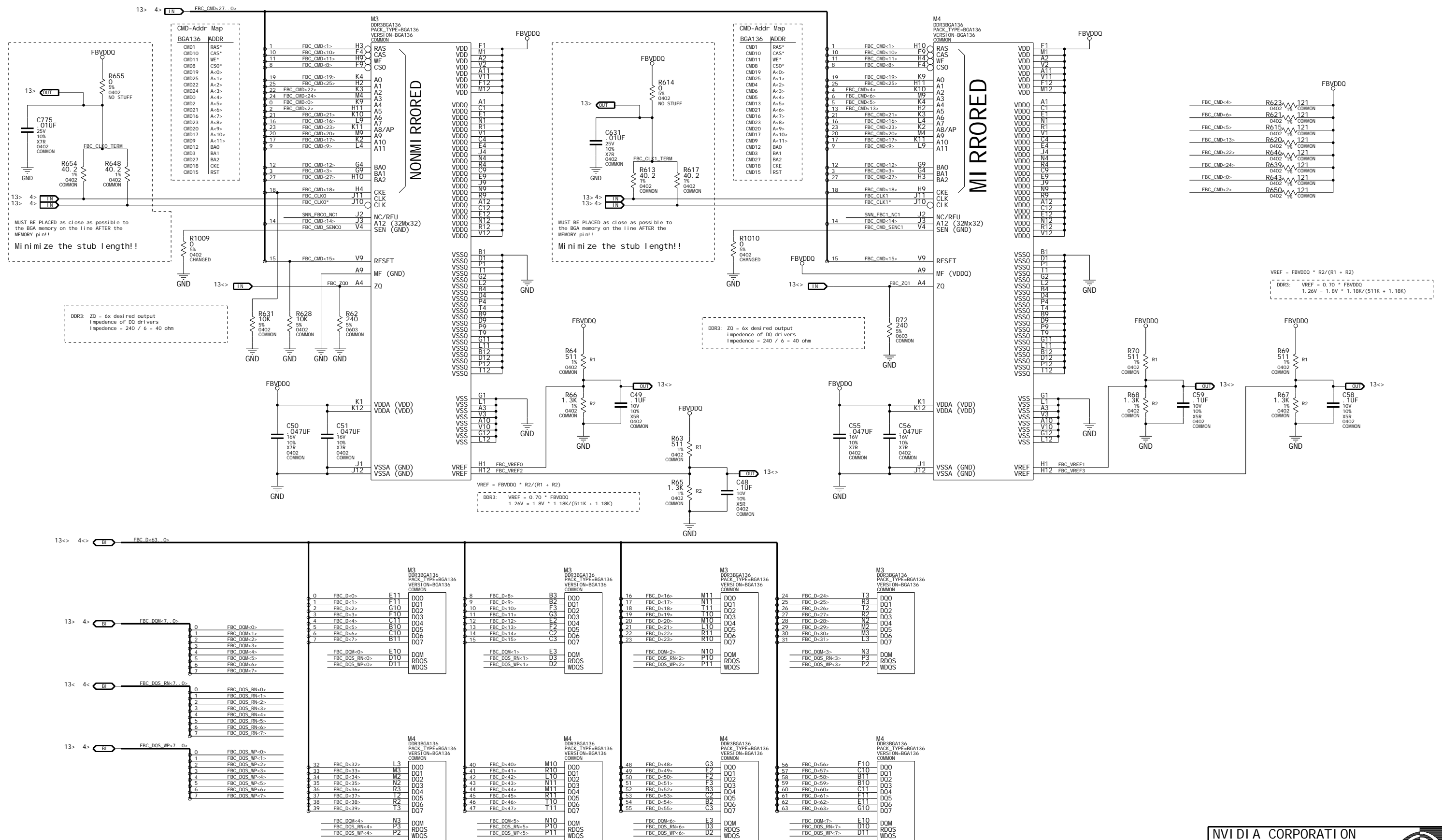


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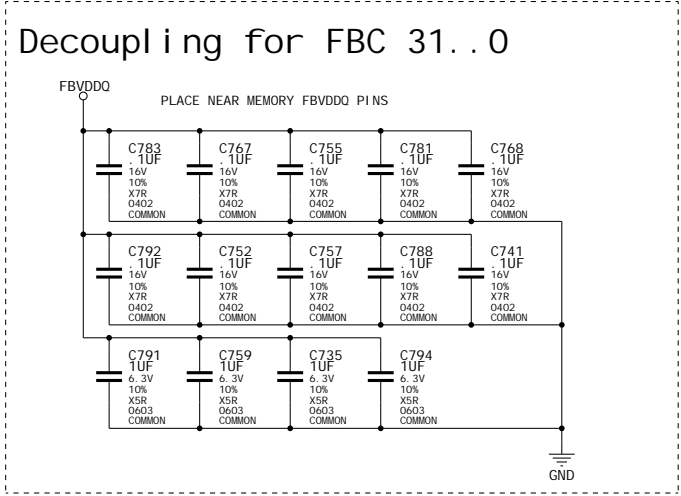


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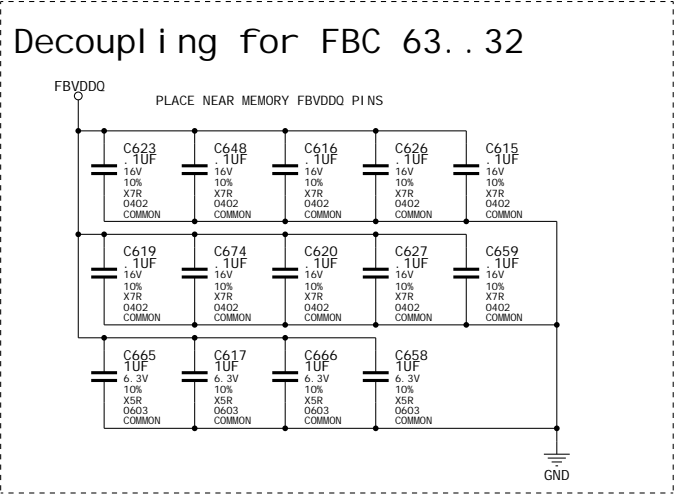


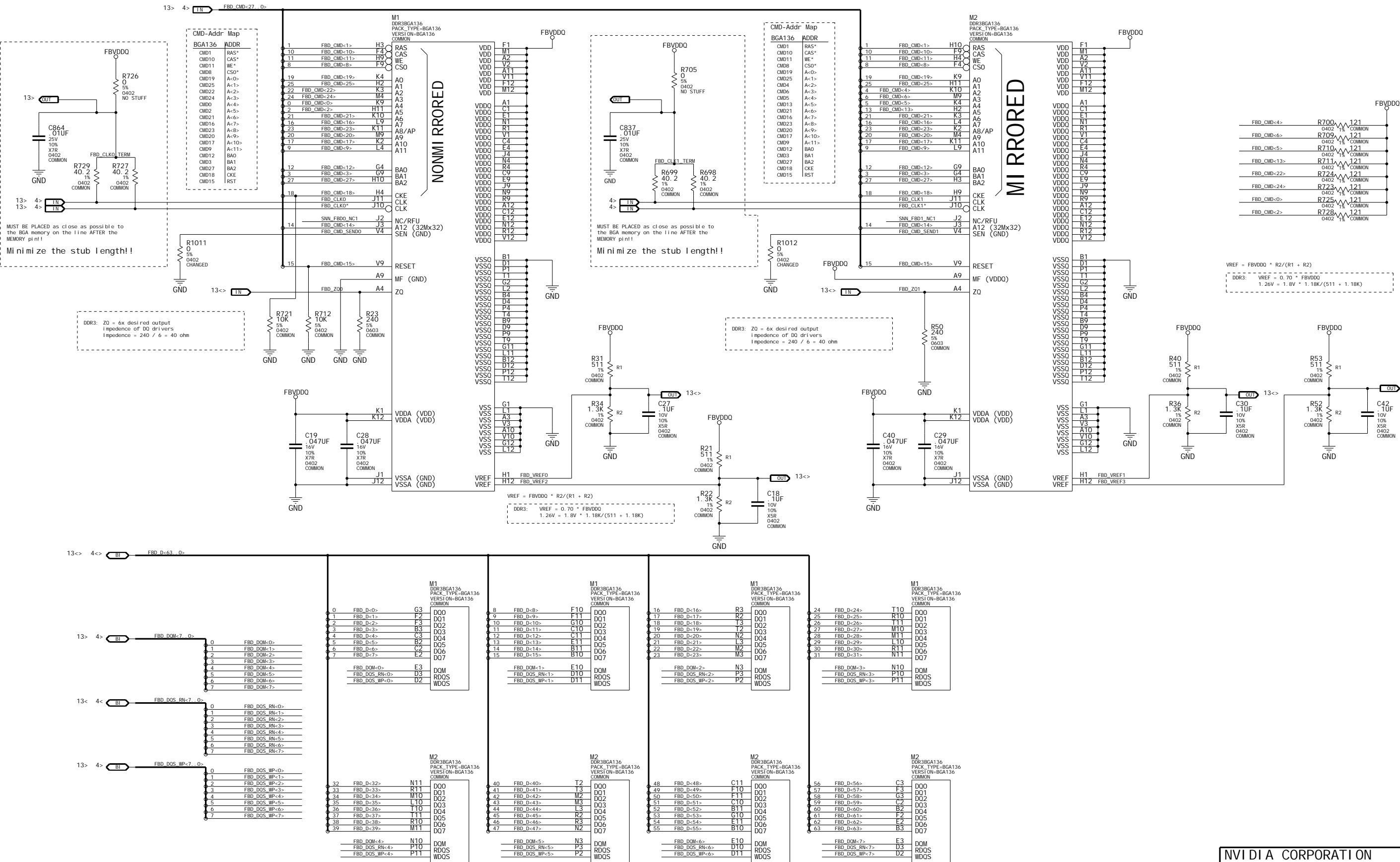


Decoupling for FBC 31..0



Decoupling for FBC 63..32





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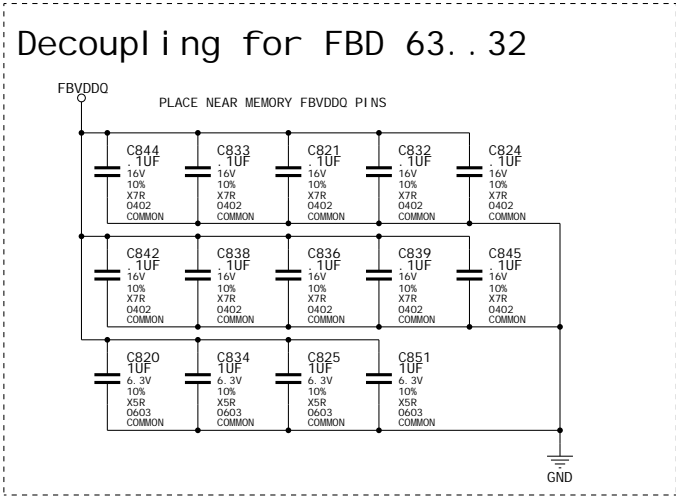
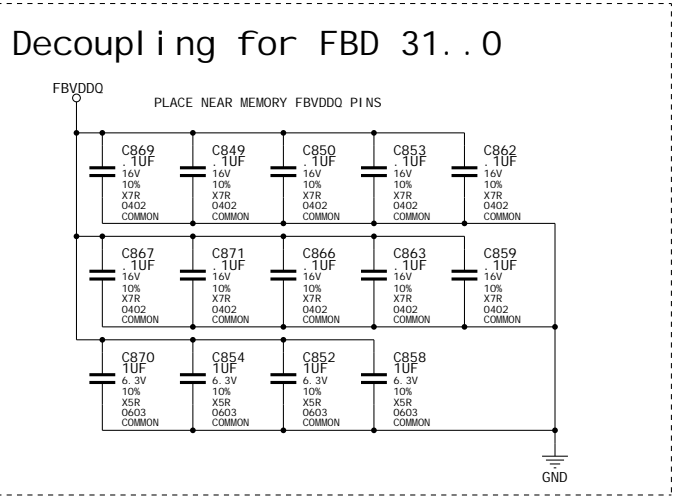
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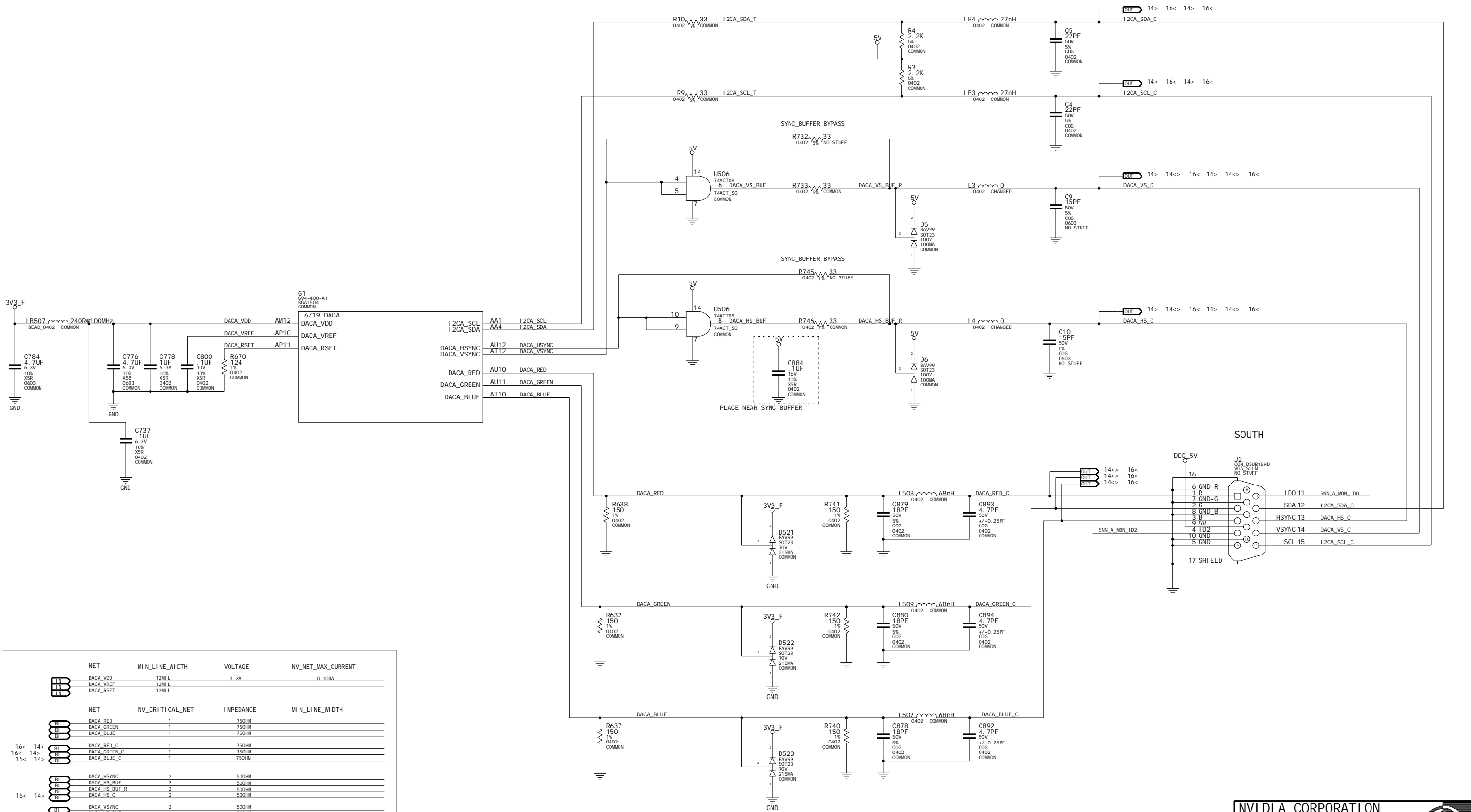
ASSEMBLY	G94-300 500MHz/800MHz 512MB 16Mx32 BGA136 GDDR3, DVI -I -DL+DVI -I -DL+HDTV-Out
PAGE DETAIL	FBD Part i on



NET RULES for FBA and FBB				
NET		NV_CRI TI CAL_NET	IMPEDANCE	DI FFPAI R
5< 3>	OUT	FBA_CLK0	1	80DI FF FBA_CLK0
	OUT	FBA_CLK0*	1	80DI FF FBA_CLK0
	OUT	FBA_CLK0_TERM	1	40OHM
5< 3>	OUT	FBA_CLK1	1	80DI FF FBA_CLK1
	OUT	FBA_CLK1*	1	80DI FF FBA_CLK1
	OUT	FBA_CLK1_TERM	1	40OHM
NET		NV_CRI TI CAL_NET	IMPEDANCE	
5< 3>	OUT	FBA_CMD<27..0>	1	40OHM
	OUT	FBA_DQS_WP<7..0>	1	40OHM
	OUT	FBA_DQS_RN<7..0>	1	40OHM
5<> 3<	IN	FBA_DQS_RN<7..0>	1	40OHM
5<> 3>	OUT	FBA_DQM<7..0>	1	40OHM
	BI	FBA_D<63..0>	1	40OHM
NET		NV_CRI TI CAL_NET	IMPEDANCE	DI FFPAI R
7< 3>	OUT	FBB_CLK0	1	80DI FF FBB_CLK0
	OUT	FBB_CLK0*	1	80DI FF FBB_CLK0
	OUT	FBB_CLK0_TERM	1	40OHM
7< 3>	OUT	FBB_CLK1	1	80DI FF FBB_CLK1
	OUT	FBB_CLK1*	1	80DI FF FBB_CLK1
	OUT	FBB_CLK1_TERM	1	40OHM
13> 7>	OUT	FBB_CLK1	1	80DI FF FBB_CLK1
	OUT	FBB_CLK1*	1	80DI FF FBB_CLK1
	OUT	FBB_CLK1_TERM	1	40OHM
NET		NV_CRI TI CAL_NET	IMPEDANCE	
7< 3>	OUT	FBB_CMD<27..0>	1	40OHM
	OUT	FBB_DQS_WP<7..0>	1	40OHM
	OUT	FBB_DQS_RN<7..0>	1	40OHM
7<> 3<	IN	FBB_DQS_RN<7..0>	1	40OHM
7<> 3>	OUT	FBB_DQM<7..0>	1	40OHM
	BI	FBB_D<63..0>	1	40OHM
NET		MI N_LI NE_WI DTH	VOLTAGE	NV_NET_MAX_CURRENT
3>	BI	FB_PLLAVDD0	12MI L	1.1V
	BI	FB_VREF	12MI L	1.26V
3>	BI	FB_VREF	12MI L	1.26V
	BI	FB_VREF	12MI L	1.26V
5>	BI	FBA_VREF0	12MI L	1.26V
	BI	FBA_VREF1	12MI L	1.26V
5>	BI	FBA_VREF2	12MI L	1.26V
	BI	FBA_VREF3	12MI L	1.26V
5<	BI	FBA_Z00	12MI L	1.26V
	BI	FBA_Z01	12MI L	1.26V
7>	BI	FBB_VREF0	12MI L	1.26V
	BI	FBB_VREF1	12MI L	1.26V
7>	BI	FBB_VREF2	12MI L	1.26V
	BI	FBB_VREF3	12MI L	1.26V
7<	BI	FBB_Z00	12MI L	1.26V
	BI	FBB_Z01	12MI L	1.26V

NET RULES for FBC and FBD				
NET		NV_CRI TI CAL_NET	IMPEDANCE	DI FFPAI R
9< 4>	OUT	FBC_CLK0	1	80DI FF FBC_CLK0
	OUT	FBC_CLK0*	1	80DI FF FBC_CLK0
	OUT	FBC_CLK0_TERM	1	40OHM
9< 4>	OUT	FBC_CLK1	1	80DI FF FBC_CLK1
	OUT	FBC_CLK1*	1	80DI FF FBC_CLK1
	OUT	FBC_CLK1_TERM	1	40OHM
NET		NV_CRI TI CAL_NET	IMPEDANCE	
9< 4>	OUT	FBC_CMD<27..0>	1	40OHM
	OUT	FBC_DQS_WP<7..0>	1	40OHM
	OUT	FBC_DQS_RN<7..0>	1	40OHM
9<> 4<	IN	FBC_DQS_RN<7..0>	1	40OHM
9<> 4>	OUT	FBC_DQM<7..0>	1	40OHM
	BI	FBC_D<63..0>	1	40OHM
NET		NV_CRI TI CAL_NET	IMPEDANCE	DI FFPAI R
11< 4>	OUT	FBD_CLK0	1	80DI FF FBD_CLK0
	OUT	FBD_CLK0*	1	80DI FF FBD_CLK0
	OUT	FBD_CLK0_TERM	1	40OHM
13> 7<	OUT	FBD_CLK1	1	80DI FF FBD_CLK1
	OUT	FBD_CLK1*	1	80DI FF FBD_CLK1
	OUT	FBD_CLK1_TERM	1	40OHM
13> 7>	OUT	FBD_CLK1	1	80DI FF FBD_CLK1
	OUT	FBD_CLK1*	1	80DI FF FBD_CLK1
	OUT	FBD_CLK1_TERM	1	40OHM
NET		NV_CRI TI CAL_NET	IMPEDANCE	
11< 4>	OUT	FBD_CMD<27..0>	1	40OHM
	OUT	FBD_DQS_WP<7..0>	1	40OHM
	OUT	FBD_DQS_RN<7..0>	1	40OHM
11<> 4<	IN	FBD_DQS_RN<7..0>	1	40OHM
11<> 4>	OUT	FBD_DQM<7..0>	1	40OHM
	BI	FBD_D<63..0>	1	40OHM
NET		MI N_LI NE_WI DTH	VOLTAGE	NV_NET_MAX_CURRENT
4>	BI	FB_PLLAVDD1	12MI L	1.1V
	BI	FB_VREF	12MI L	1.26V
9>	BI	FBC_VREF0	12MI L	1.26V
	BI	FBC_VREF1	12MI L	1.26V
9>	BI	FBC_VREF2	12MI L	1.26V
	BI	FBC_VREF3	12MI L	1.26V
9<	BI	FBC_Z00	12MI L	1.26V
	BI	FBC_Z01	12MI L	1.26V
11>	BI	FBD_VREF0	12MI L	1.26V
	BI	FBD_VREF1	12MI L	1.26V
11>	BI	FBD_VREF2	12MI L	1.26V
	BI	FBD_VREF3	12MI L	1.26V
11<	BI	FBD_Z00	12MI L	1.26V
	BI	FBD_Z01	12MI L	1.26V

DACA RGB-FILTER



NET	MI N_LI NE_WI DTH	VOLTAGE	NV_NET_MAX_CURRENT
1N	DACA_VDD	12M L	3.3V
1N	DACA_VREF	12M L	0.100A
1N	DACA_RSET	12M L	

NET	NV_NI TRI CAL_NET	IMPEDANCE	MI N_LI NE_WI DTH
BI	DACA_RED	1	75OHM
BI	DACA_GREEN	1	75OHM
BI	DACA_BLUE	1	75OHM
16< 14>	DACA_RED_C	1	75OHM
16< 14>	DACA_GREEN_C	1	75OHM
16< 14>	DACA_BLUE_C	1	75OHM
BI	DACA_HSYNC	2	50OHM
BI	DACA_HS_BUF	2	50OHM
BI	DACA_HS_BUF_R	2	50OHM
BI	DACA_HS_C	2	50OHM
BI	DACA_VSYNC	2	50OHM
BI	DACA_VS_BUF	2	50OHM
BI	DACA_VS_BUF_R	2	50OHM
BI	DACA_VS_C	2	50OHM

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ASSEMBLY

G94-300 500MHz/800MHz 512MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out

PAGE DETAIL

DACA Interface

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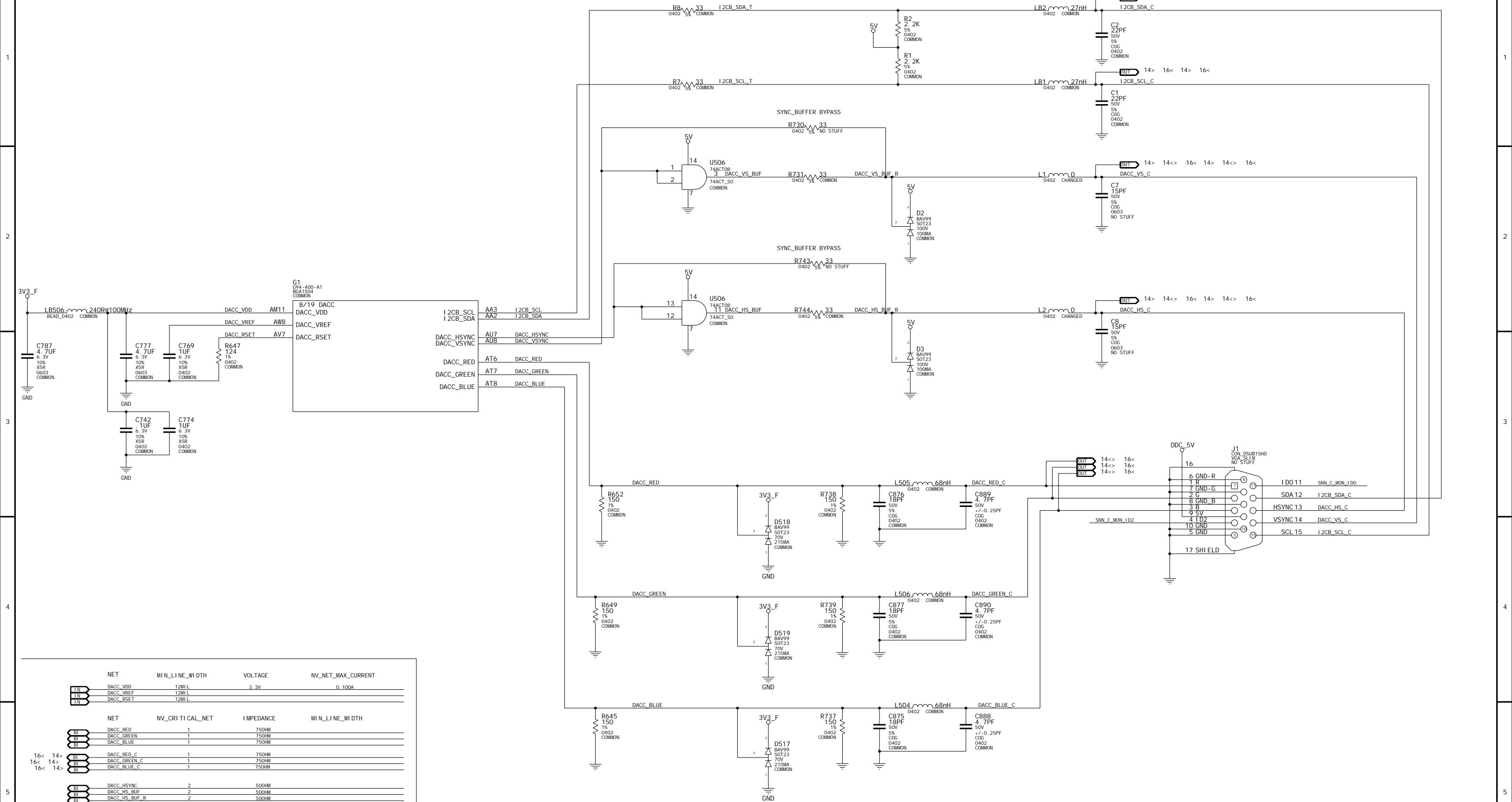
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DACC RGB-FILTER



NET	MIN_LENGTH	VOLTAGE	NV_NET_MAX_CURRENT
DACC_VDD	12MIL	3.3V	0.100A
DACC_VREF	12MIL		
DACC_VSET	12MIL		

NET	NV_CRTICAL_NET	IMPEDANCE	MIN_LENGTH
DACC_RED	1	750HM	
DACC_GREEN	1	750HM	
DACC_BLUE	1	750HM	
DACC_RED_C	1	750HM	
DACC_GREEN_C	1	750HM	
DACC_BLUE_C	1	750HM	

DACC_HSYNC	2	500HM	
DACC_HS_BUF	2	500HM	
DACC_HS_BUF_R	2	500HM	
DACC_HS_C	2	500HM	
DACC_VSYNC	2	500HM	
DACC_VS_BUF	2	500HM	
DACC_VS_BUF_R	2	500HM	
DACC_VS_C	2	500HM	

ASSEMBLY	G94-300 500MHz/800MHz 512MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
PAGE DETAIL	DACC Interface

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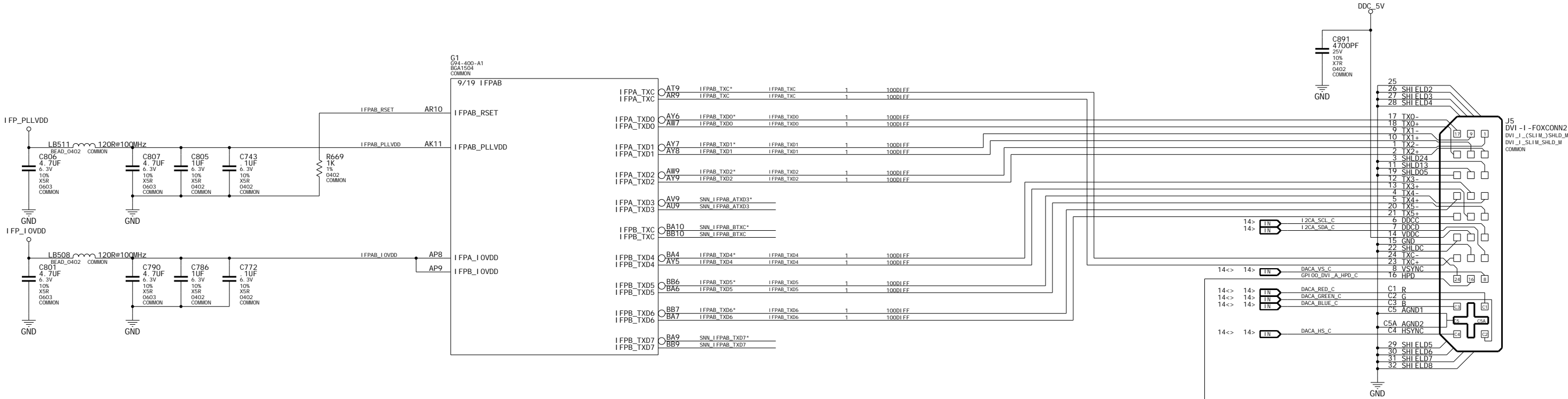
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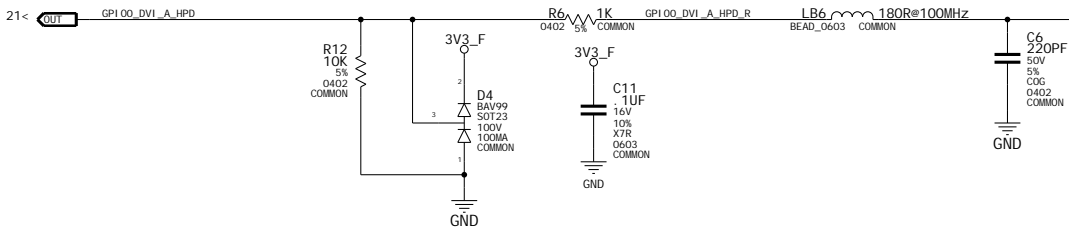
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	NET	MIN_LENGTH	VOLTAGE	NV_NET_MAX_CURRENT
BI	IFPAB_PLLVDD	12MIL	1.8V	0.035A
BI	IFPAB_I0VDD	12MIL	3.3V	0.145A
BI	IFPAB_RSET	12MIL		



DVI AB Hotplug Detection



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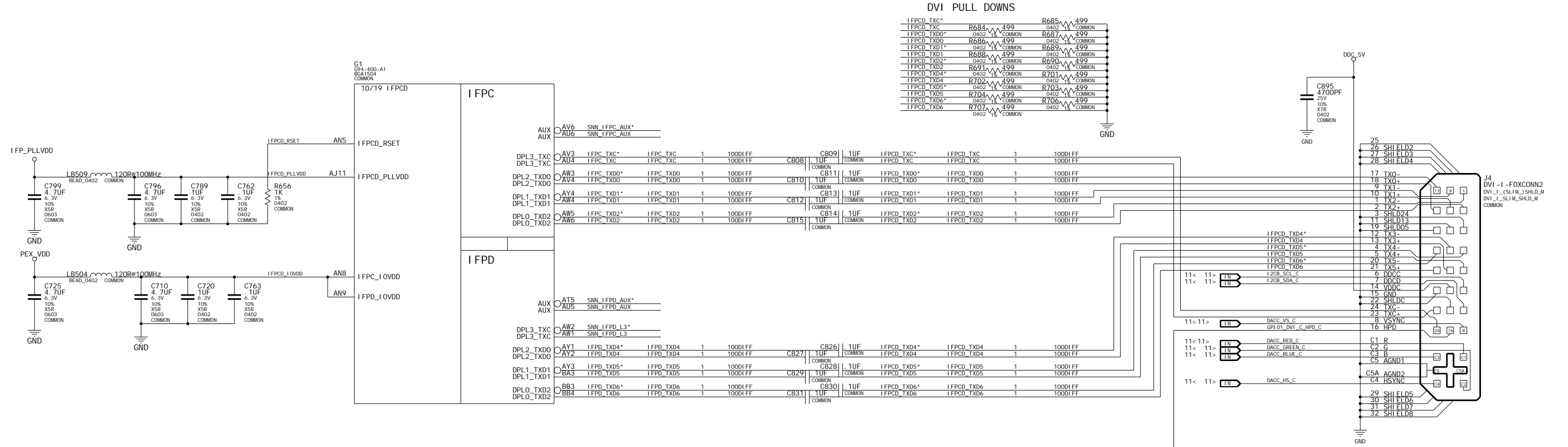


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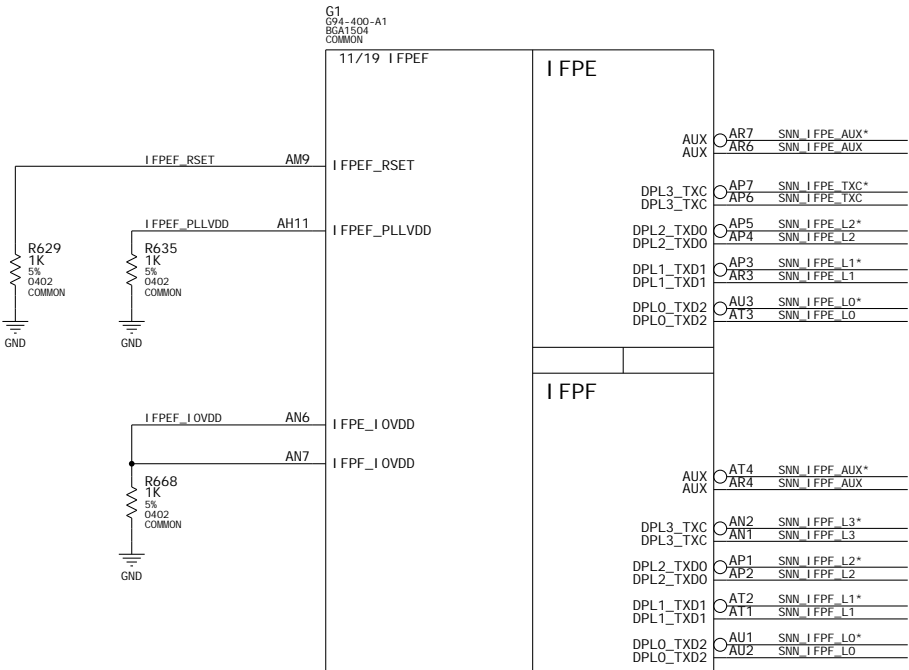
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NET	MIN_LENGTH	VOLTAGE	MAX_CURRENT
IFPCD_PLLVDD	12MIL	1.8V	0.035A
IFPCD_I0VDD	12MIL	1.1V	0.800A
IFPCD_RSET	12MIL		



Page18: I FP E/F Interface -- Unused



NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
I FPEF_PLLVDD	12MIL		
I FPEF_LOVDD	12MIL		
I FPEF_RSET	12MIL		

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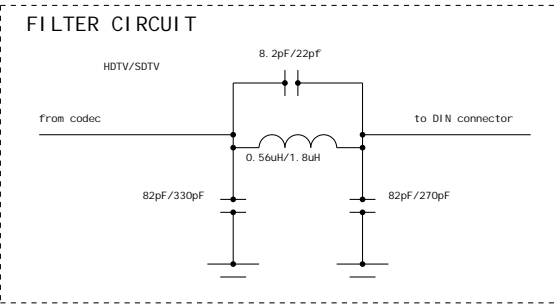
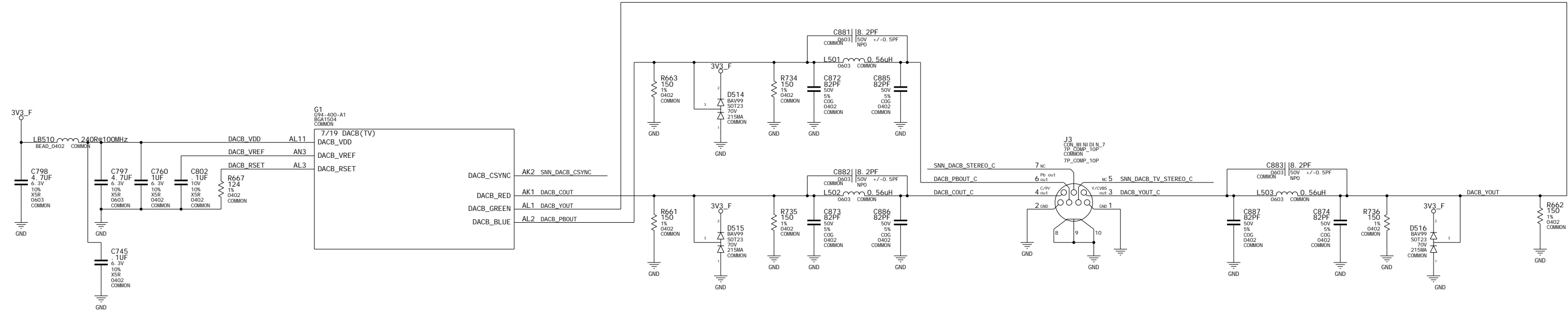
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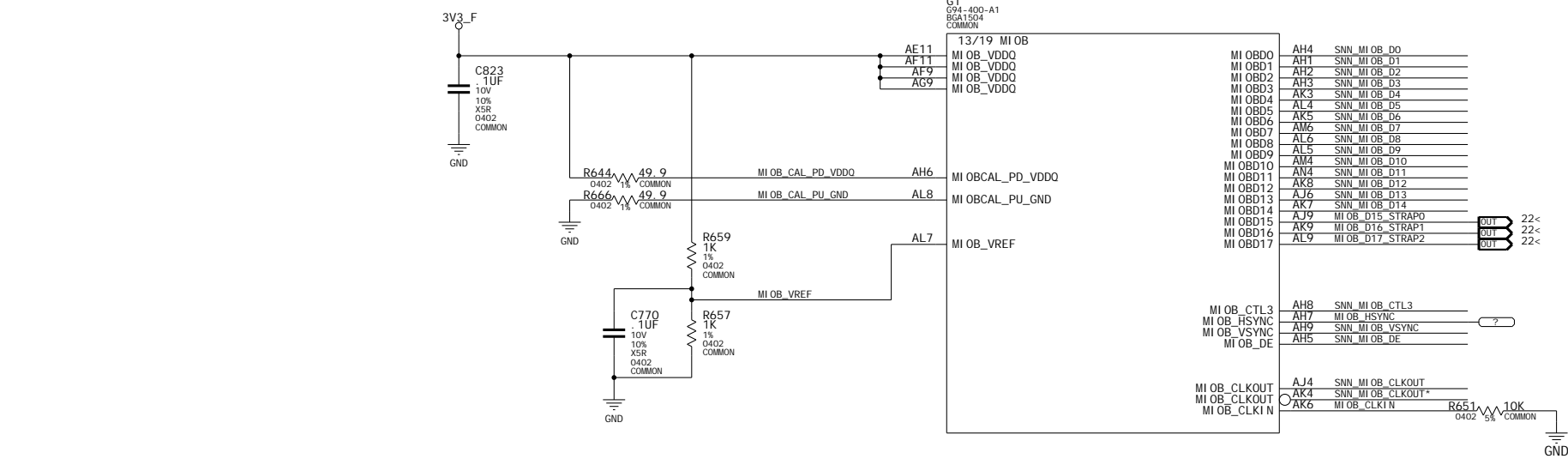
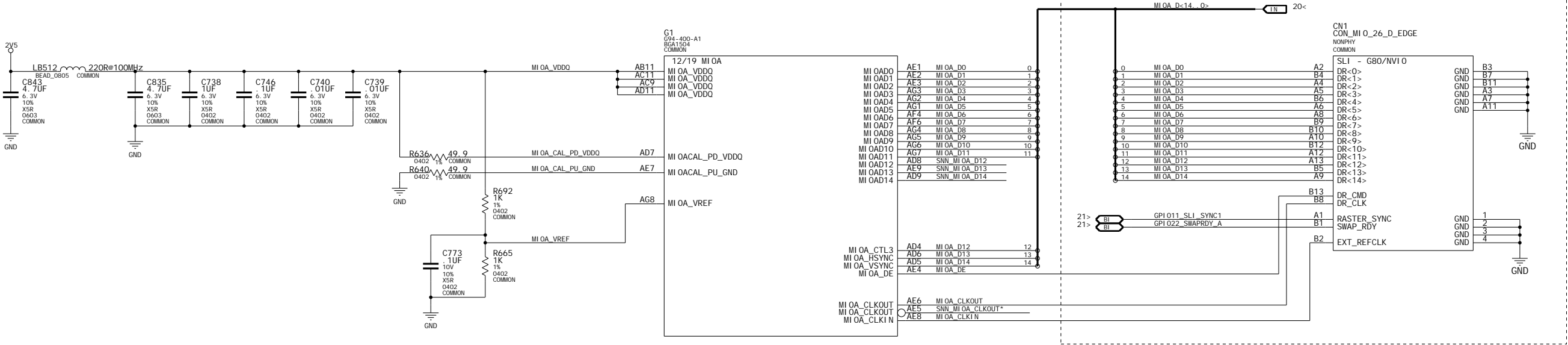
ASSEMBLY	G94-300 500MHz/800MHz 512MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
PAGE DETAIL	I FP E/F Interface -- Unused

NET		NET	NV_CRI TI CAL_NET	IMPEDANCE
<div>1N</div>	DACB_COUT	1	75OHM	
	DACB_COUT_C	1	75OHM	
<div>1N</div>	DACB_YOUT	1	75OHM	
	DACB_YOUT_C	1	75OHM	
<div>1N</div>	DACB_PBOUT	1	75OHM	
	DACB_PBOUT_C	1	75OHM	

NET		MIN_LI NE_WI DTH	VOLTAGE	NV_NET_MAX_CURRENT
19<	DACB_VREF	12MI L	3.3V	0.100A
19<	DACB_VREF	12MI L		
	DACB_RSET	12MI L		



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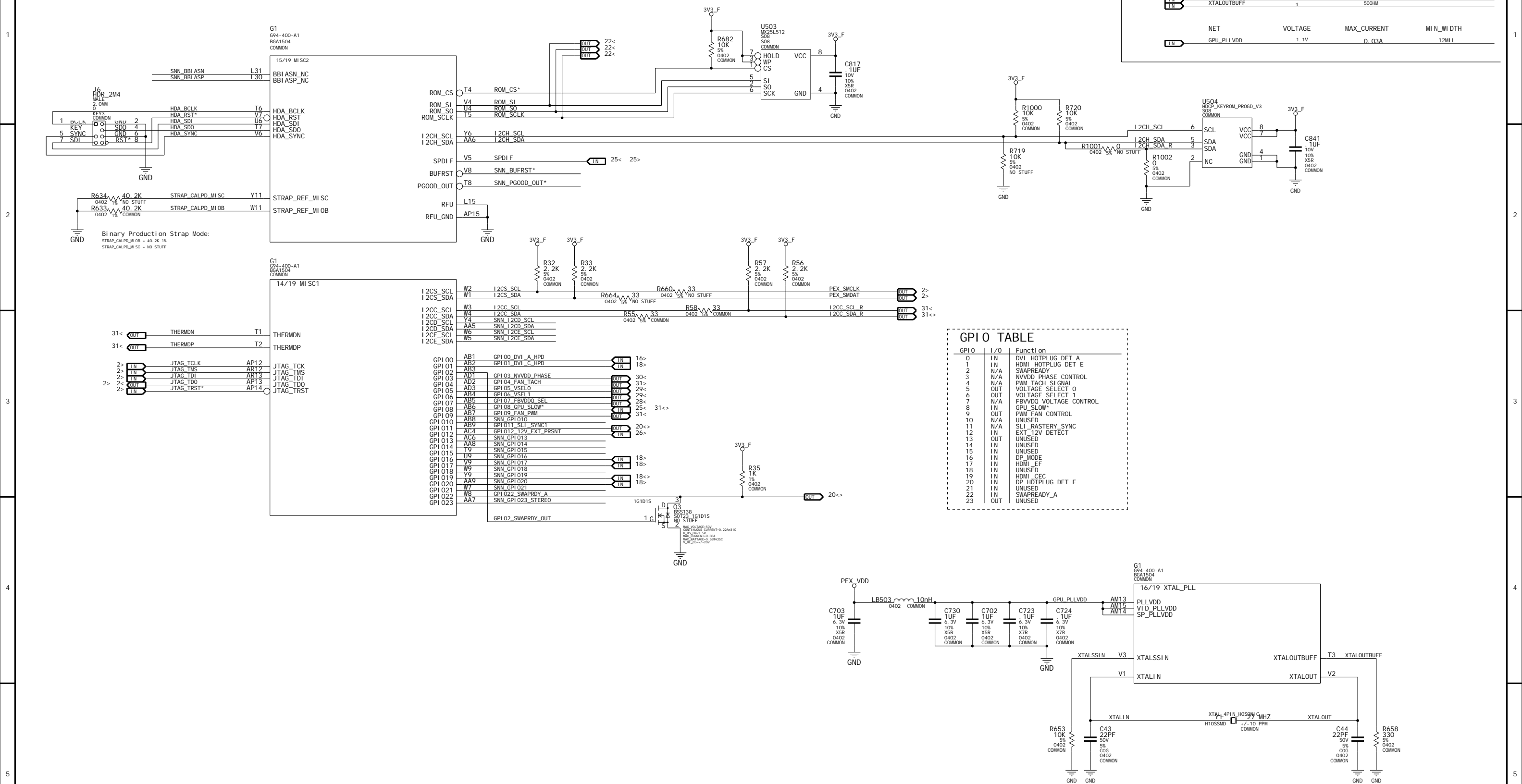
NET	NV_CRI TI CAL_NET	I MPEDANCE	DI FFPAI R
20< 1N	MI 0A D<14_ 0>	1	500H
1N	MI 0A CLKI N	1	500H
1N	MI 0A CLKOUT	1	500H
1N	MI 0A DE	1	500H

NET	MI N_LI NE_WI DTH	VOLTAGE	NV_NET_MAX_CURRENT
1N	MI 0A VDDQ	16M L	2.5V
1N	MI 0A VREF	12M L	1.65V
1N	MI 0A CAL_PD_VDDQ	12M L	2.5V
1N	MI 0A CAL_PD_GND	12M L	0.0V

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NV_PN	600-10545-0010-100 J		
ID	p545_a01	PAGE	20 OF 32
NAME	apatel	DATE	11-DEC-2007

Page21: MI SC: GPI O, I 2C, ROM, HDCP, and XTAL

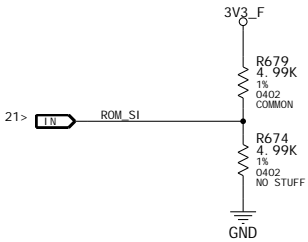


ASSEMBLY	G94-300 500MHz/800MHz 512MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
PAGE DETAIL	MI SC: GPIO, I2C, ROM, HDCP, and XTAL

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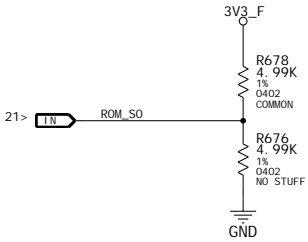
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NV_PN	600-10545-0010-100 J		
ID	p545_a01	PAGE	21 OF 32
NAME	apatel	DATE	11-DEC-2007

Page22: Strap Confi gurati on

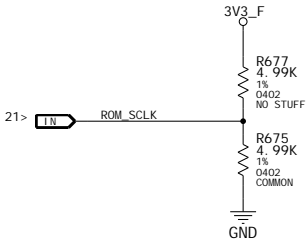


STRAP PIN	STRAP NAME
ROM_SI	PCI_DEVI D_EXT

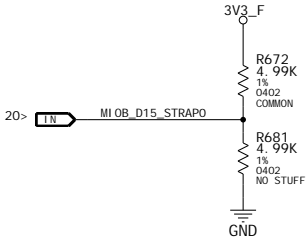
3V3	GND
5K	1 0



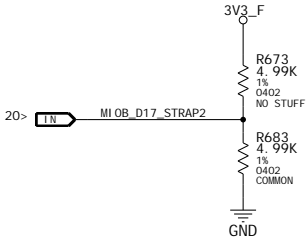
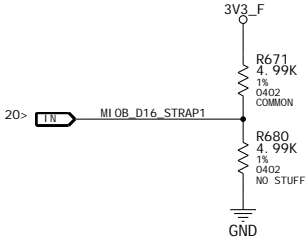
STRAP PIN	STRAP NAME
ROM_SO	SLOT_CLK_CFG



STRAP PIN	STRAP NAME
ROM_SCLK	PCI_DEVI D[3]



STRAP PIN	STRAP NAME				
STRAP0	RAMCFG0				
		* RAMCFG[2:0]			
STRAP PIN	STRAP NAME	256MB (8Mx32)	512MB (16Mx32)	1024MB (32Mx32)	
		101 --- 256-bit Qimonda	001 --- 256-bit Qimonda	101 --- 256-bit Hynix	
		110 --- 256-bit Hynix	010 --- 256-bit Hynix	110 --- 256-bit Hynix	
		111 --- 256-bit Samsung	011 --- 256-bit Samsung	111 --- 256-bit Samsung	
		* VBIOS will be defined on a per SKU basis.			



STRAP PIN	STRAP NAME
STRAP2	RAMCFG2

G1		G94-400-A1
BGA1504		COMMON
19/19 NC	NC	
SNN_NC<1>	AC34	NC
SNN_NC<2>	AC36	NC
SNN_NC<3>	AC37	NC
SNN_NC<4>	AC7	NC
SNN_NC<5>	AF34	NC
SNN_NC<6>	AF36	NC
SNN_NC<7>	AF37	NC
SNN_NC<8>	AF7	NC
SNN_NC<9>	AG37	NC
SNN_NC<10>	AG38	NC
SNN_NC<11>	AH40	NC
SNN_NC<12>	AJ7	NC
SNN_NC<13>	AK32	NC
SNN_NC<14>	AL32	NC
SNN_NC<15>	AL40	NC
SNN_NC<16>	AM29	NC
SNN_NC<17>	AM30	NC
SNN_NC<18>	AM31	NC
SNN_NC<19>	AM32	NC
SNN_NC<20>	AM7	NC
SNN_NC<21>	AP34	NC
SNN_NC<22>	AR36	NC
SNN_NC<23>	AT11	NC
SNN_NC<24>	AT113	NC
SNN_NC<25>	AT35	NC
SNN_NC<26>	AU14	NC
SNN_NC<27>	AU17	NC
SNN_NC<28>	AU20	NC
SNN_NC<29>	AU23	NC
SNN_NC<30>	AU26	NC
SNN_NC<31>	AV10	NC
SNN_NC<32>	AV12	NC
SNN_NC<33>	AV28	NC
SNN_NC<34>	AY31	NC
SNN_NC<35>	C12	NC
SNN_NC<36>	E15	NC
SNN_NC<37>	E16	NC
SNN_NC<38>	F16	NC
SNN_NC<39>	F17	NC
SNN_NC<40>	F20	NC
SNN_NC<41>	F23	NC
SNN_NC<42>	F31	NC
SNN_NC<43>	G17	NC
SNN_NC<44>	G20	NC
SNN_NC<45>	G23	NC
SNN_NC<46>	G26	NC
SNN_NC<47>	G29	NC
SNN_NC<48>	G8	NC
SNN_NC<49>	H28	NC
SNN_NC<50>	J17	NC
SNN_NC<51>	J17	NC
SNN_NC<52>	J20	NC
SNN_NC<53>	J23	NC
SNN_NC<54>	J29	NC
SNN_NC<55>	J9	NC
SNN_NC<56>	L14	NC
SNN_NC<57>	L16	NC
SNN_NC<58>	L28	NC
SNN_NC<59>	L29	NC
SNN_NC<60>	M3	NC
SNN_NC<61>	M37	NC
SNN_NC<62>	P11	NC
SNN_NC<63>	P34	NC
SNN_NC<64>	P36	NC
SNN_NC<65>	R11	NC
SNN_NC<66>	R3	NC
SNN_NC<67>	R35	NC
SNN_NC<68>	T11	NC
SNN_NC<69>	U11	NC
SNN_NC<70>	U36	NC
SNN_NC<71>	Y7	NC
SNN_NC<72>	Y34	NC
SNN_NC<73>	Y36	NC
SNN_NC<74>	Y37	NC
SNN_NC<75>	Y7	NC

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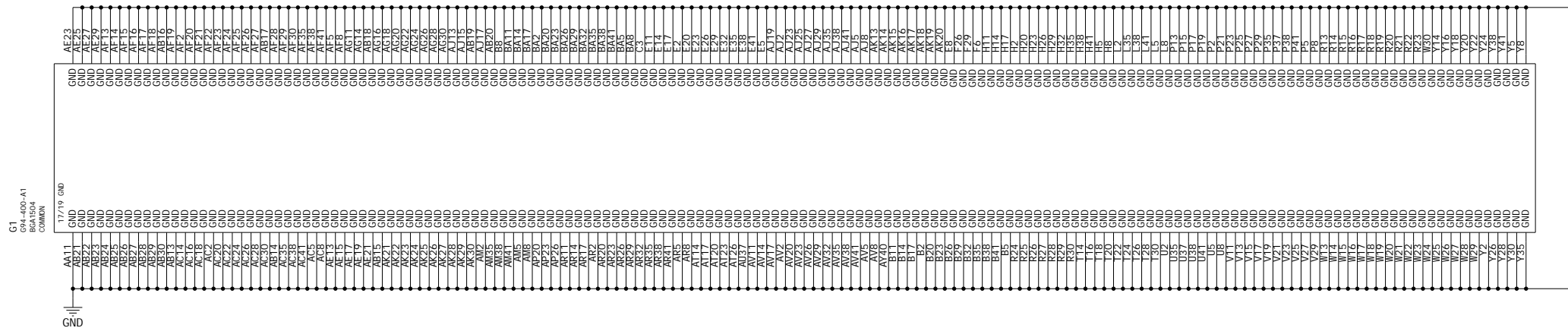
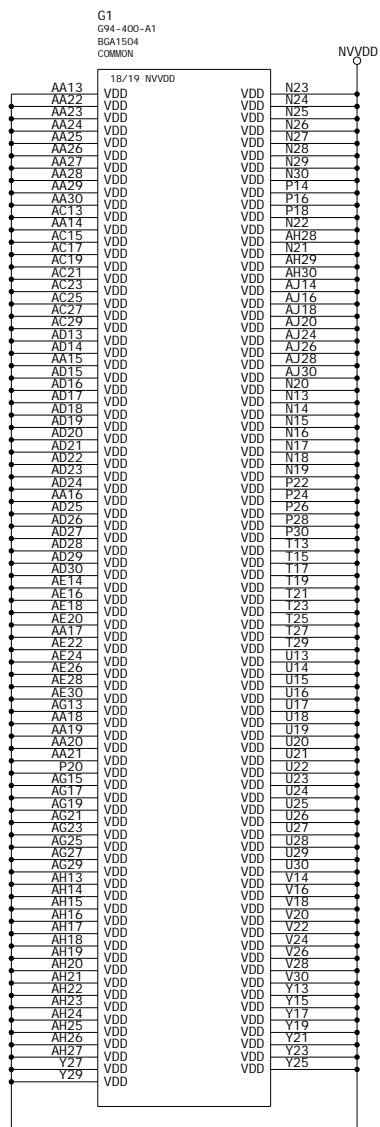


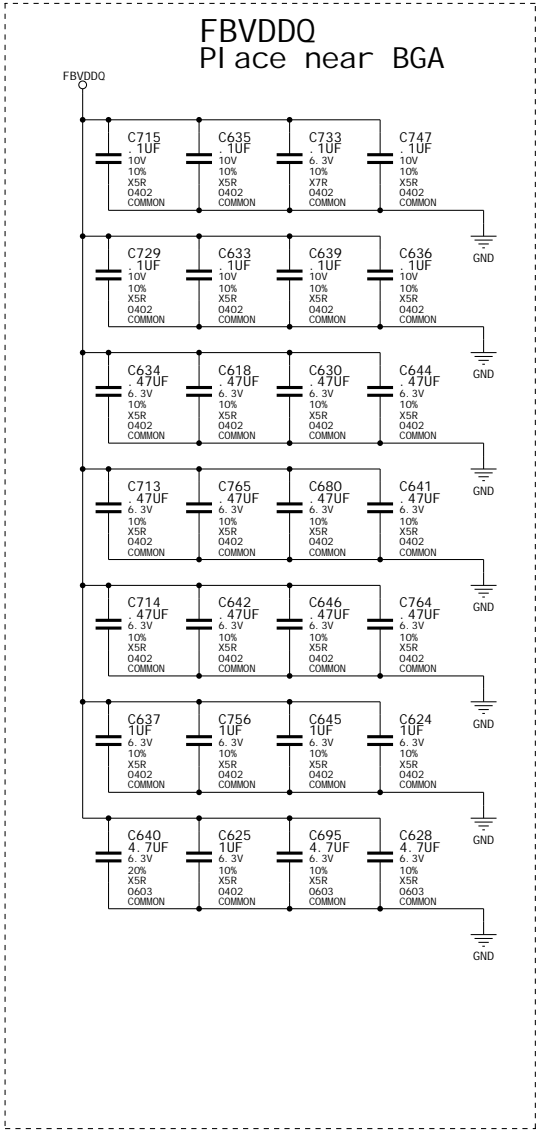
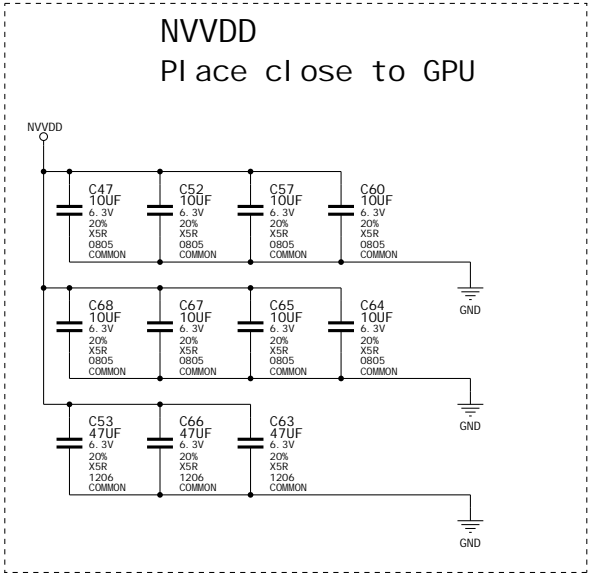
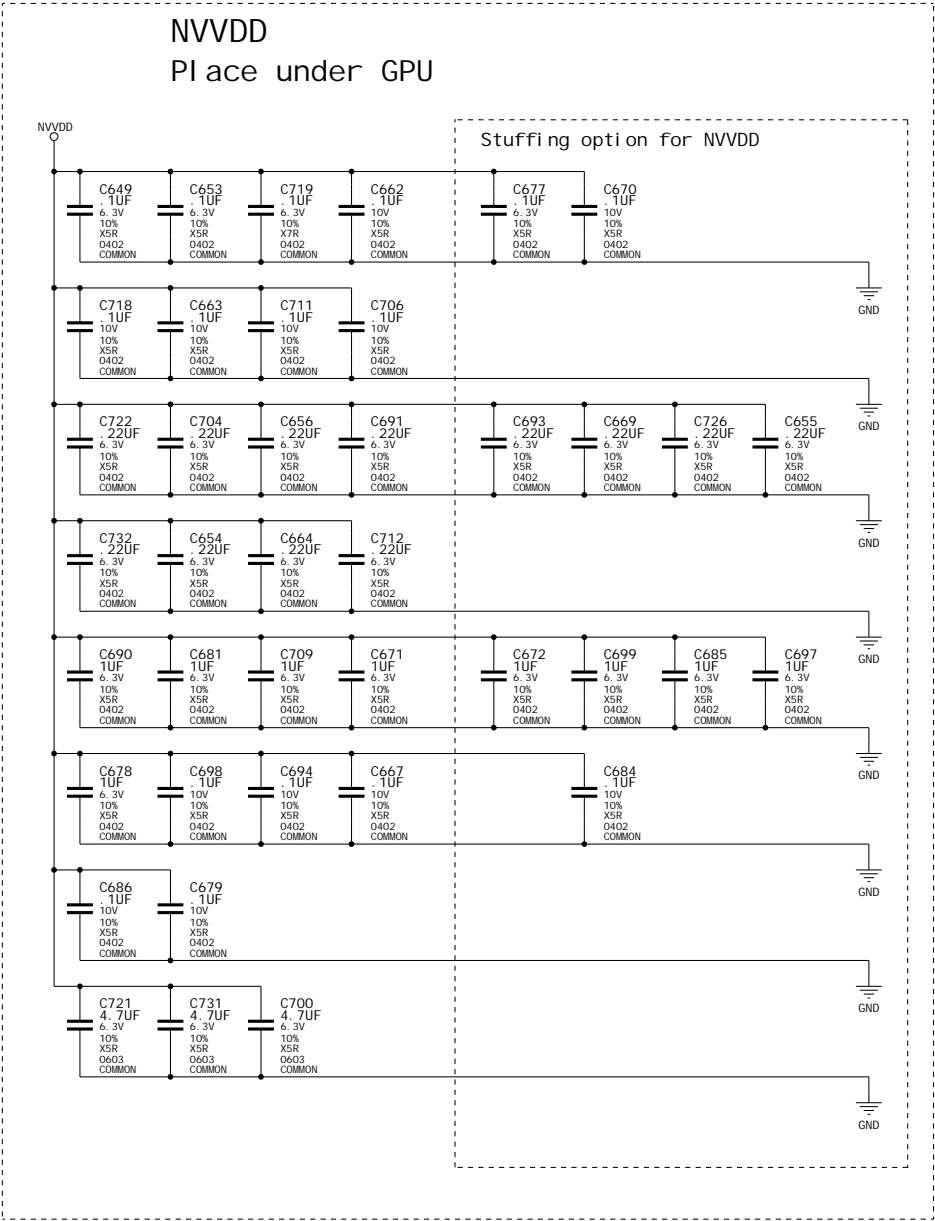
NV_PN 600-10545-0010-100 J

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NAME apatel DATE 11-DEC-2007

Page23: PWR and GND Signal s





12V_EXT

R1013
6.8K
5%
0402
COMMON

12V_F

R1015
10K
5%
0402
COMMON

1G1D15

01002
BSS138
SOT23
COMMON

1G

NVDD_EN_PWR_O

1G1D15

01003
BSS138
SOT23
COMMON

1G1D15

1G

NVDD_EN_PWR_I

R1014
1K
5%
0402
COMMON

GND

GND

PU placed at power detection circuit

Thermal Protection

[illegible]

SPDIF Input

The schematic diagram illustrates a SPDIF Input circuit. It features two OPA2830 op-amp buffers (U1, U2) configured as voltage followers. The input signal (SPDIF_IN) is connected to the non-inverting input of U1. The output of U1 is connected to the non-inverting input of U2. The output of U2 is connected to the SPDIF_OUT pin. The circuit includes a 5V power supply and a 3V3_F input. A 1N4148 diode (D8) is connected between the SPDIF_IN and the output of U1. A 3V3_F Schottky diode (D7) is connected between the SPDIF_OUT and the output of U2. Various passive components, including resistors (R13-R29) and capacitors (C13-C17), are used for signal conditioning and timing. The circuit is designed to interface a SPDIF signal with a microcontroller.

Components:

- U1, U2: OPA2830, 508 COMMON
- D8: 1N4148, COMMON
- D7: 3V3_F, 100V, 100MA, COMMON
- R13: 10K, 1%, 0402 COMMON
- R14: 6.2K, 5%, 0402 COMMON
- R15: 1K, 1%, 0402 COMMON
- R16: 330, 5%, 0402 COMMON
- R17: 330, 5%, 0402 COMMON
- R18: 1K, 1%, 0402 COMMON
- R19: 1.5K, 1%, 0402 COMMON
- R20: 10K, 5%, 0402 NO STUFF
- R21: 15K, 1%, 0402 NO STUFF
- R22: 1K, 1%, 0402 COMMON
- R23: 1K, 1%, 0402 COMMON
- R24: 15K, 1%, 0402 NO STUFF
- R25: 1K, 1%, 0402 COMMON
- R26: 75, 5%, 0805 COMMON
- R27: 15K, 1%, 0402 NO STUFF
- R28: 1K, 1%, 0402 COMMON
- R29: 75, 5%, 0805 NO STUFF
- C13: 0.01uF, 10%, 16V, X7R, COMMON
- C14: 0.01uF, 10%, 16V, X7R, COMMON
- C15: 1uF, 10%, 6.3V, XSR, 0402 COMMON
- C16: 1uF, 10%, 16V, XSR, 0402 COMMON
- C17: 0.1uF, 10%, 16V, X7R, 0402 COMMON

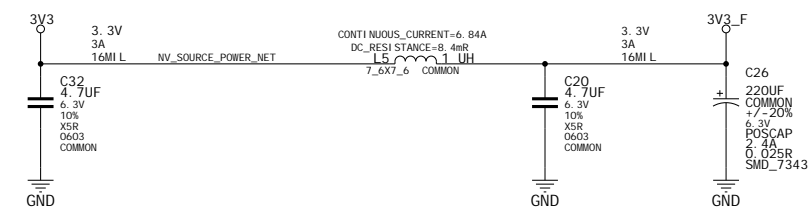
Connections:

- SPDIF_IN to U1 V+
- U1 V- to GND
- U1 V+ to U2 V+
- U2 V- to GND
- U2 V+ to SPDIF_OUT
- 5V to R13, R14, R15, R20, R21, R27
- 3V3_F to D7
- D7 to D8
- D8 to U1 V+
- U1 V+ to R16
- R16 to D8
- D8 to U1 V+
- U1 V+ to R17
- R17 to D8
- D8 to U1 V+
- U1 V+ to R18
- R18 to D8
- D8 to U1 V+
- U1 V+ to R19
- R19 to D8
- D8 to U1 V+
- U1 V+ to R20
- R20 to D8
- D8 to U1 V+
- U1 V+ to R21
- R21 to D8
- D8 to U1 V+
- U1 V+ to R22
- R22 to D8
- D8 to U1 V+
- U1 V+ to R23
- R23 to D8
- D8 to U1 V+
- U1 V+ to R24
- R24 to D8
- D8 to U1 V+
- U1 V+ to R25
- R25 to D8
- D8 to U1 V+
- U1 V+ to R26
- R26 to D8
- D8 to U1 V+
- U1 V+ to R27
- R27 to D8
- D8 to U1 V+
- U1 V+ to R28
- R28 to D8
- D8 to U1 V+
- U1 V+ to R29
- R29 to D8
- D8 to U1 V+

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V_EXT	12V	6.25A	16MIL
12V	12V	5.5A	16MIL
GND	0V	28A	16MIL

3V3 Power Supply Filter

3V3_F = 3.3V @ 2.5A



12V Power Supply Filter

12V_F = 12V @ 5.5A

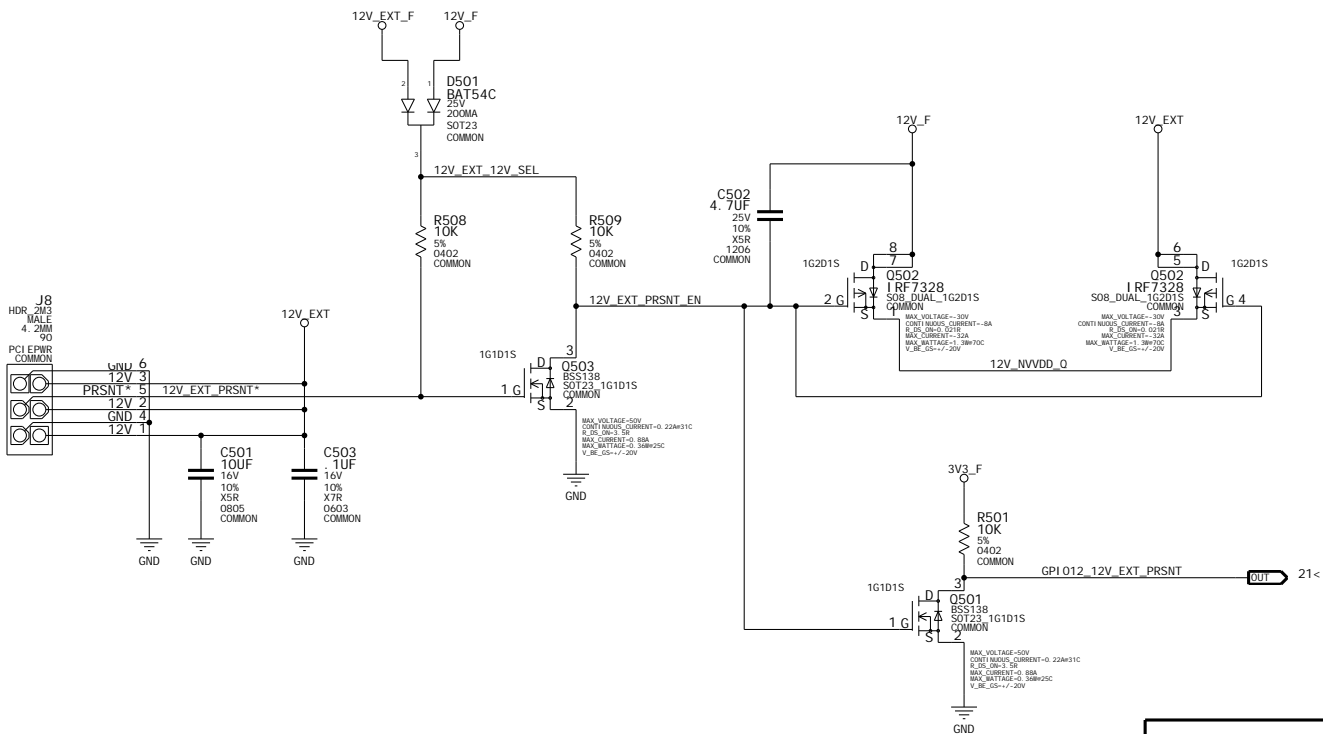


12V_EXT Power Supply Filter

12V_EXT_F = 12V @ 6.25A



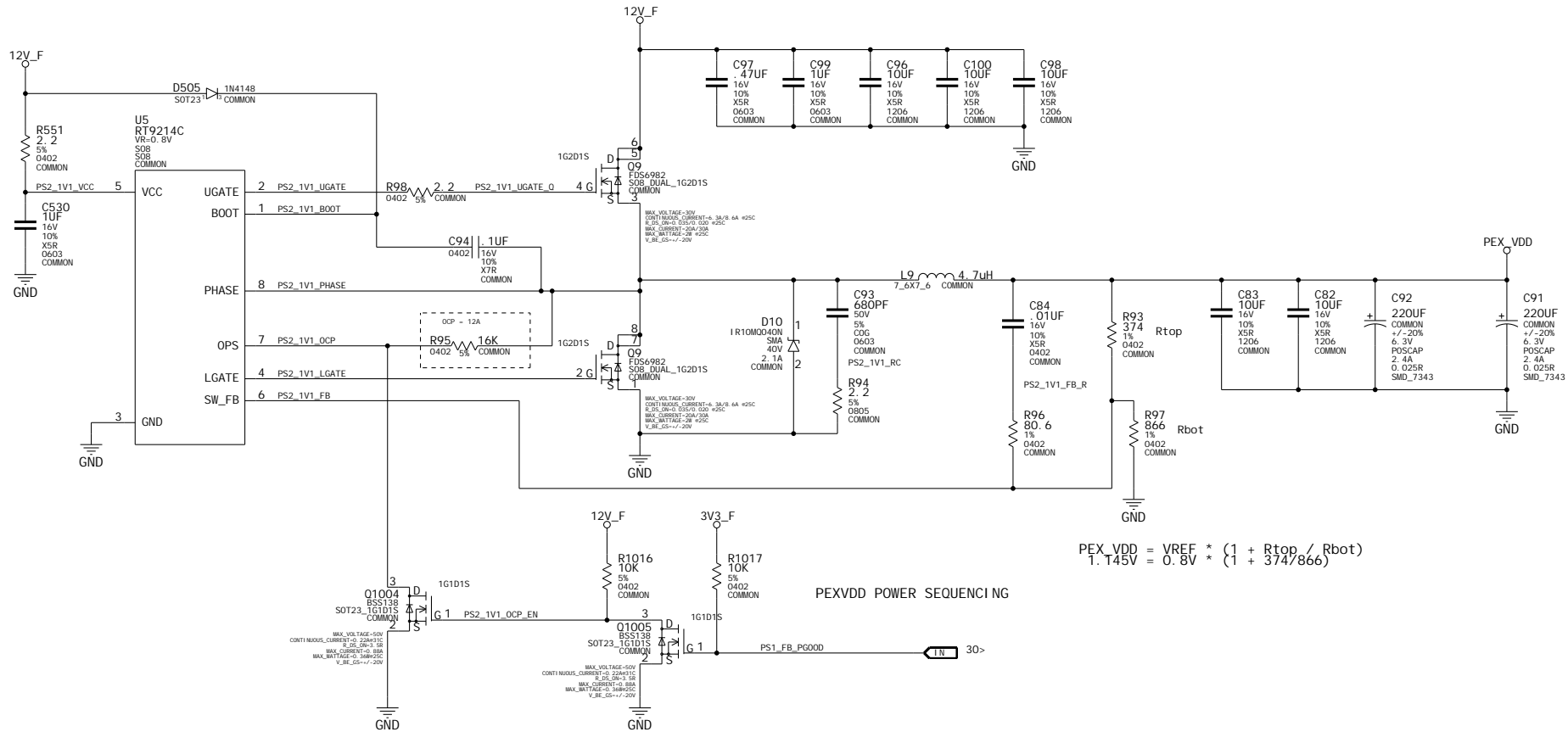
INPUT POWER SELECTION for NVVDD



	GPI012
EMERGENCY MODE (12V_EXT present)	0
150W POWER MODE (12V_EXT NOT present)	1

PEX_VDD Power Supply

PEX_VDD = 1.1V @ 3A

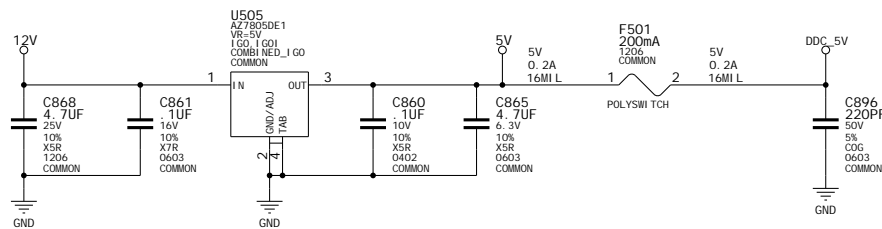


$$\frac{\text{PEX_VDD}}{1.145\text{V}} = \frac{\text{VREF}}{0.8\text{V}} * \left(1 + \frac{\text{Rtop}}{374/866}\right)$$

5V and DDC_5V Power Supply

DDC_5V = 5V @ 200mA

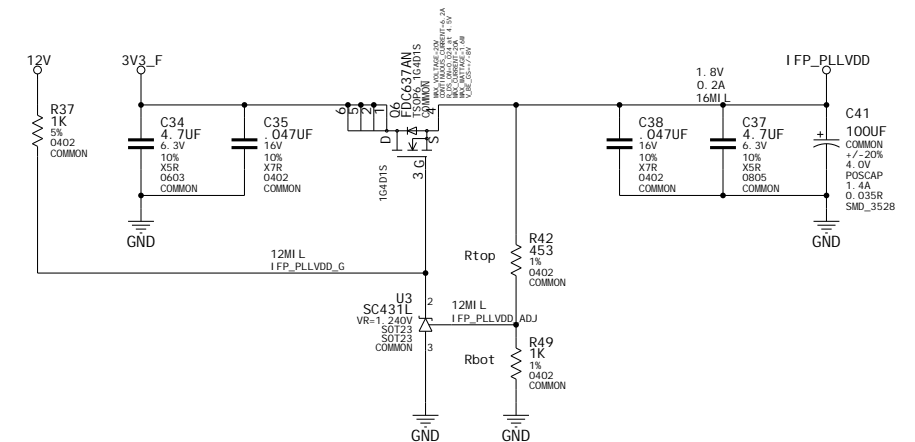
LAYOUT NOTE: ADD MIN 200MM^2 COPPER AROUND THIS DPAK FOR HEAT DISSIPATION



NET		MI_N_LI_NE_WDTH	VOLTAGE	NV_NET_MAX_CURRENT
PEX_VDD	PEX_VDD	16mI L	1.1V	3A
(N)	PS2_1V1_UGATE	16mI L		
(N)	PS2_1V1_UGATE_Q	16mI L		
(N)	PS2_1V1_BOOT	16mI L		
(N)	PS2_1V1_PHASE	16mI L		3A
(N)	PS2_1V1_OCP	16mI L		
(N)	PS2_1V1_UGATE	16mI L		
(N)	PS2_1V1_FB	16mI L		
(N)	PS2_1V1_FB_R	16mI L		
(N)	PS2_1V1_RC	16mI L		
(N)	PS2_1V1_VCC	16mI L		

IFP_PLLVDD Power Supply

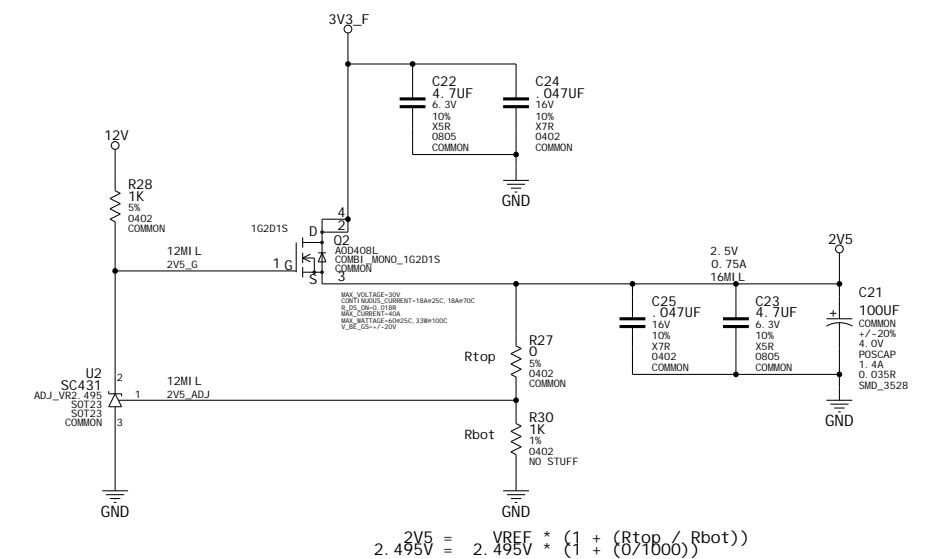
IFP_PLLVDD = 1.8V @ 200mA



$$I_{FP_PLLVD D} = V_{REF} * (1 + (R_{top} / R_{bot}))$$

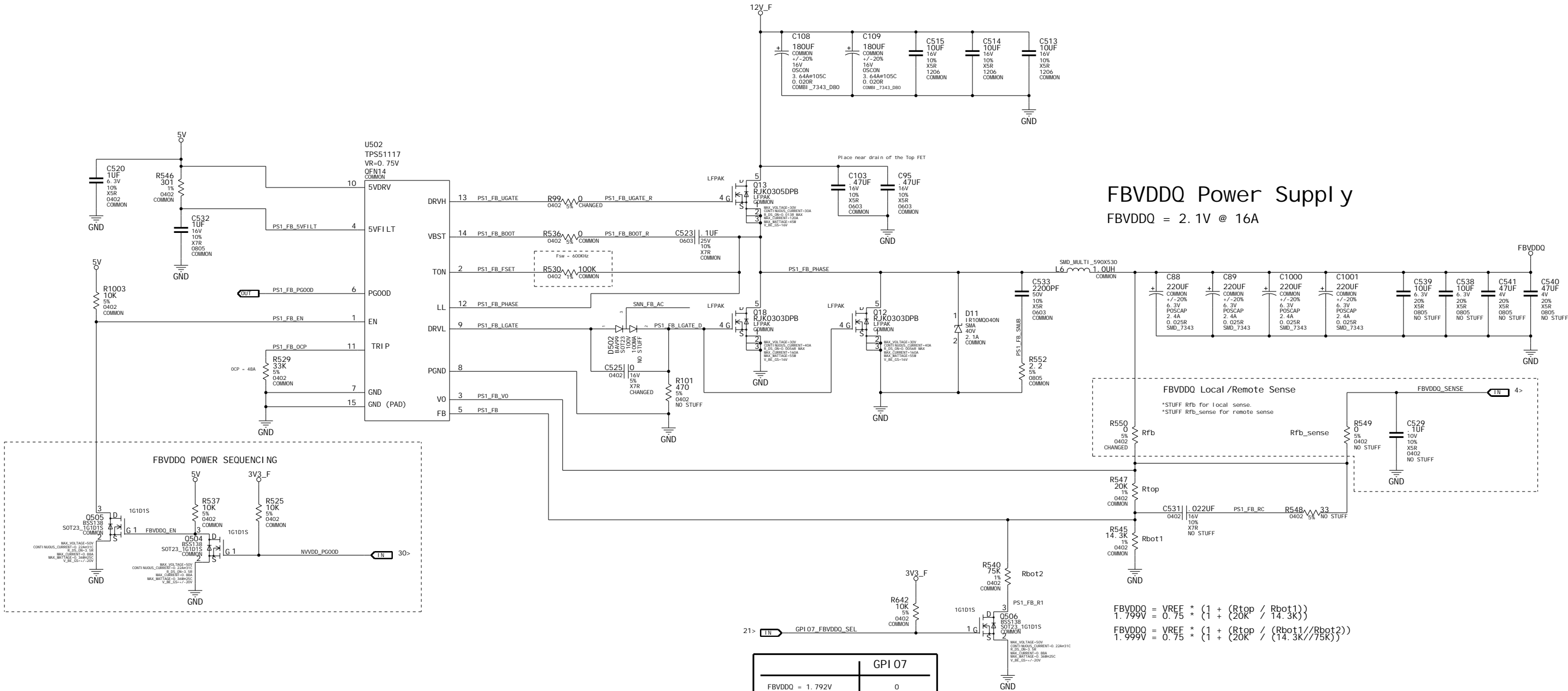
$$1.801V = 1.24V * (1 + (453/1000))$$

2V5 Power Supply

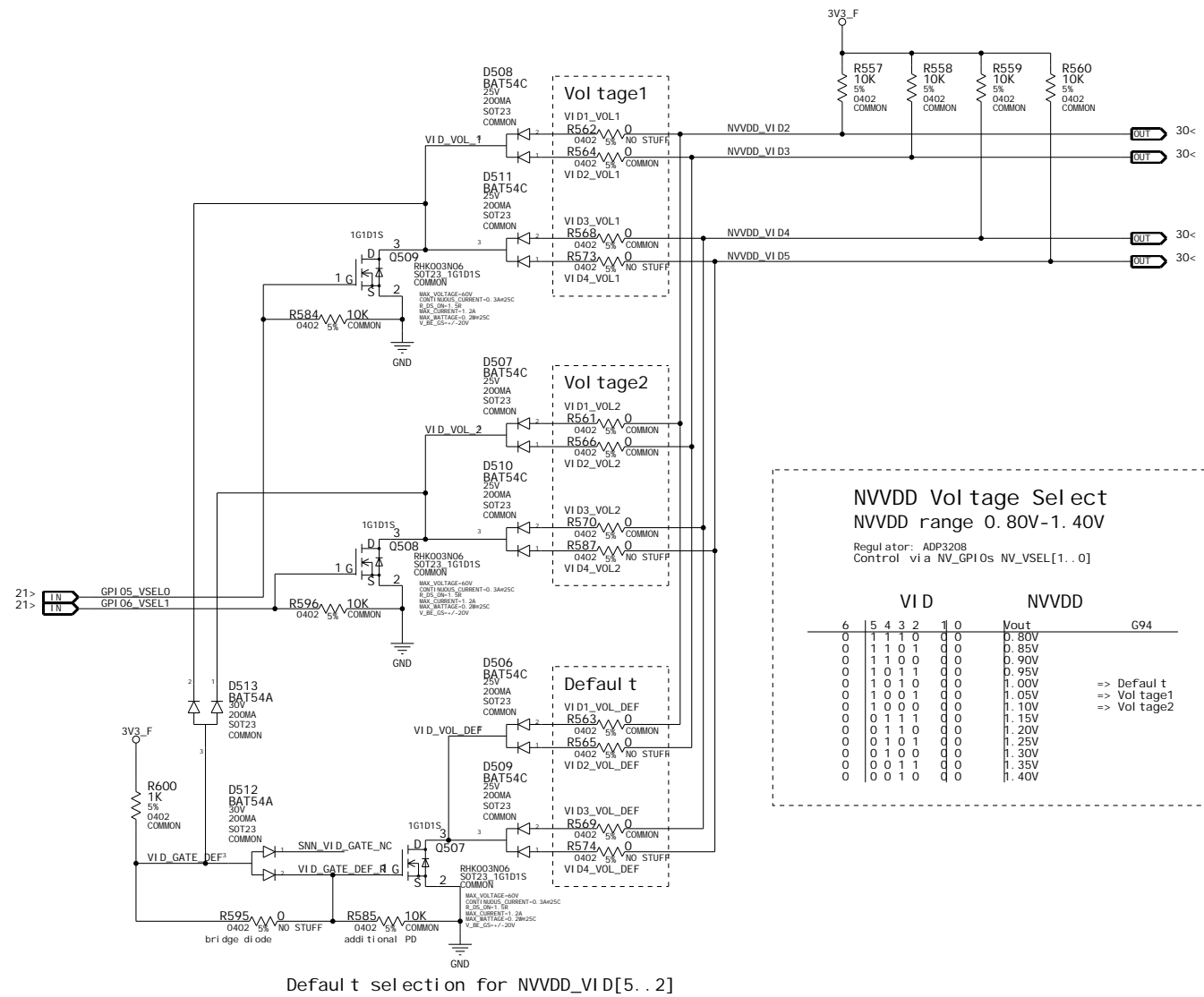
$$2V5 = 2.5V @ 750mA$$


$$2.495V = 2.495V * (1 + (R_{top}/R_{bot}))$$

	NET	MIN_LENGTH	VOLTAGE	NV_NET_MAX_CURRENT
28<	FBVDDQ	20MIL	2.1V	16A
28<	PS1_FB_BOOT	20MIL		
28<	PS1_FB_BOOT	20MIL		
28<	PS1_FB_UGATE	20MIL		
28<	PS1_FB_UGATE_R	20MIL		
28<	PS1_FB_PHASE	20MIL		16A
28<	PS1_FB_LGATE	20MIL		
28<	PS1_FB_LGATE_D	20MIL		
28<	PS1_FB_FSET	20MIL		
28<	PS1_FB_FSET	20MIL		
28<	PS1_FB_COMP	20MIL		
28<	PS1_FB_COMP1	20MIL		
28<	PS1_FB_SNUB	20MIL		
28<	PS1_FB_FSET	20MIL		
28<	PS1_FB_5VFILT	20MIL		
28<	PS1_FB	20MIL		
28<	PS1_VO	20MIL		
28<	PVCC5	20MIL		
28<	VCC5	20MIL		
28<	FBVDDQ_FS_D15	12MIL		
28<	FBVDDQ_EN	12MIL		



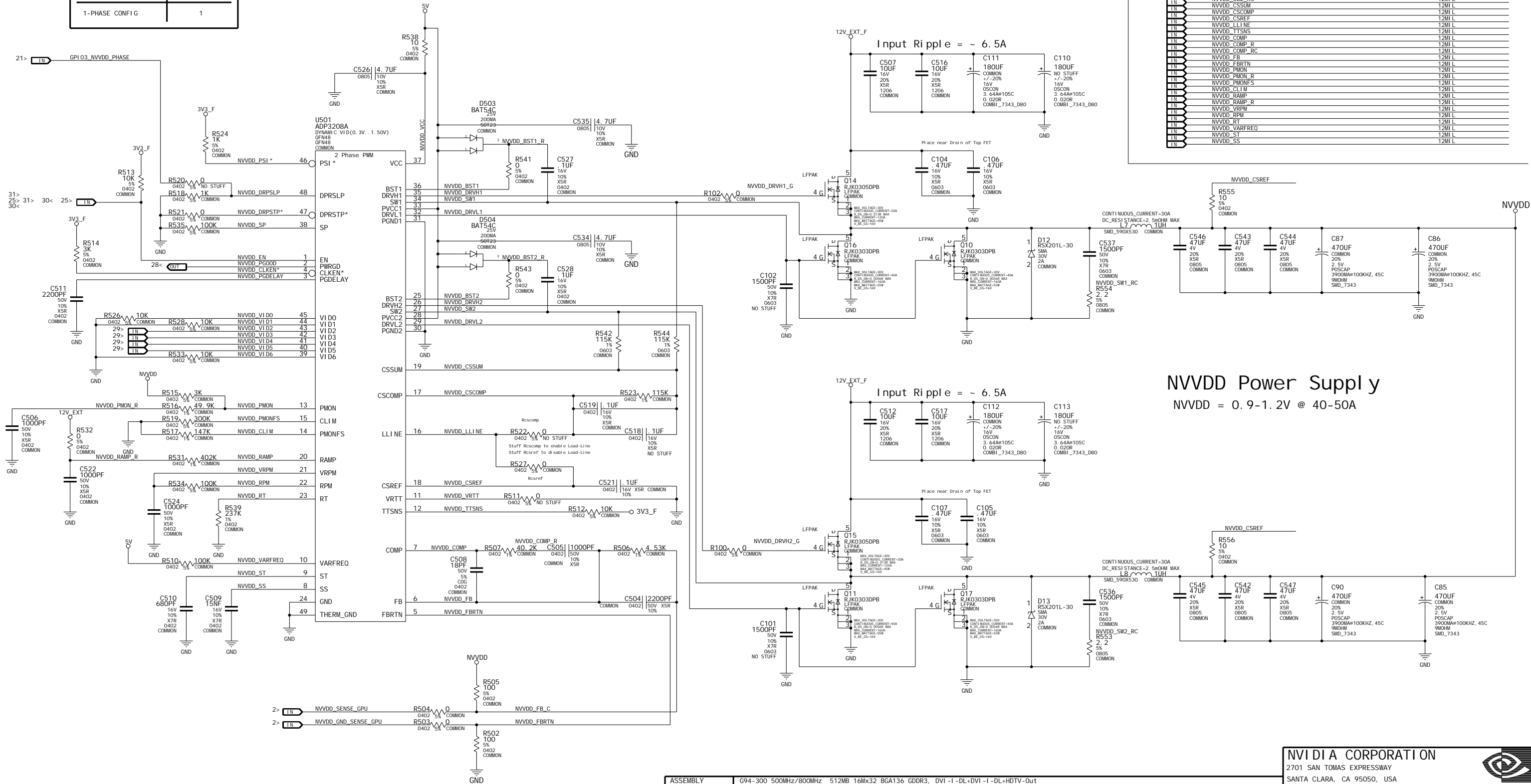
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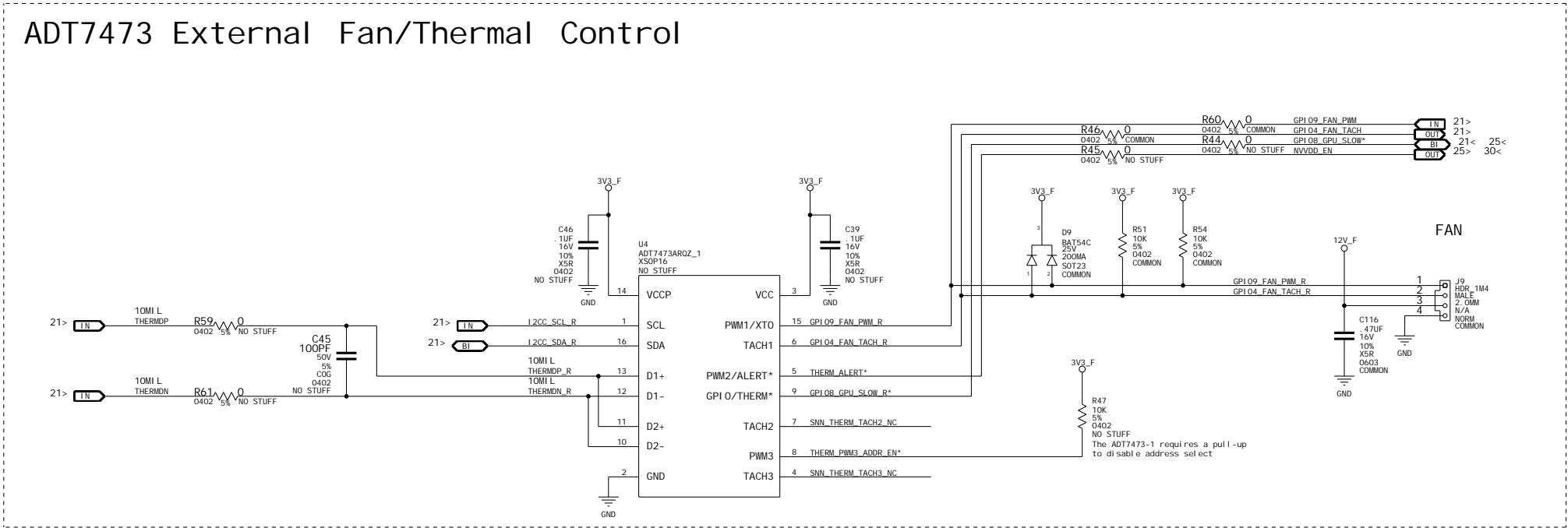
VID						NVVDD	
6	5	4	3	2	1	0	Vout
0	1	1	0	0	0	0	0.80V
0	1	1	0	1	0	0	0.85V
0	1	1	0	1	1	0	0.90V
0	1	1	0	1	1	1	0.95V
0	1	1	1	0	0	0	0.90V
0	1	1	1	0	1	0	1.05V
0	1	0	0	1	0	0	1.10V
0	1	0	0	1	1	0	1.15V
0	0	1	1	0	0	0	1.20V
0	0	1	1	0	1	0	1.25V
0	0	1	0	1	0	0	1.30V
0	0	1	0	1	1	0	1.35V
0	0	0	1	0	0	0	1.40V

GPI O3

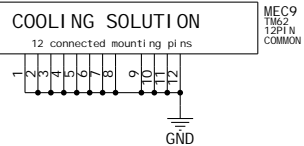
2-PHASE CONFIG	0
1-PHASE CONFIG	1



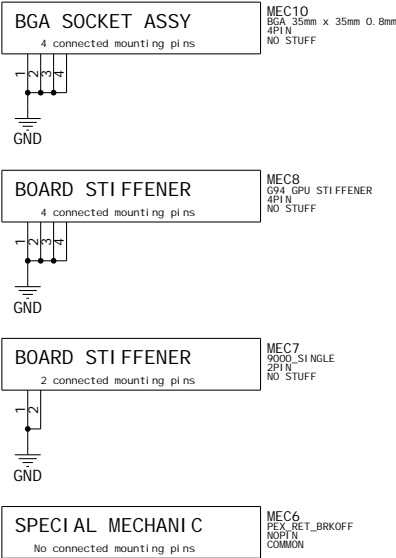
ADT7473 External Fan/Thermal Control



Thermal



Mechani cal



Bracket

