PCI-EXPRESS EDGE CONNECTOR

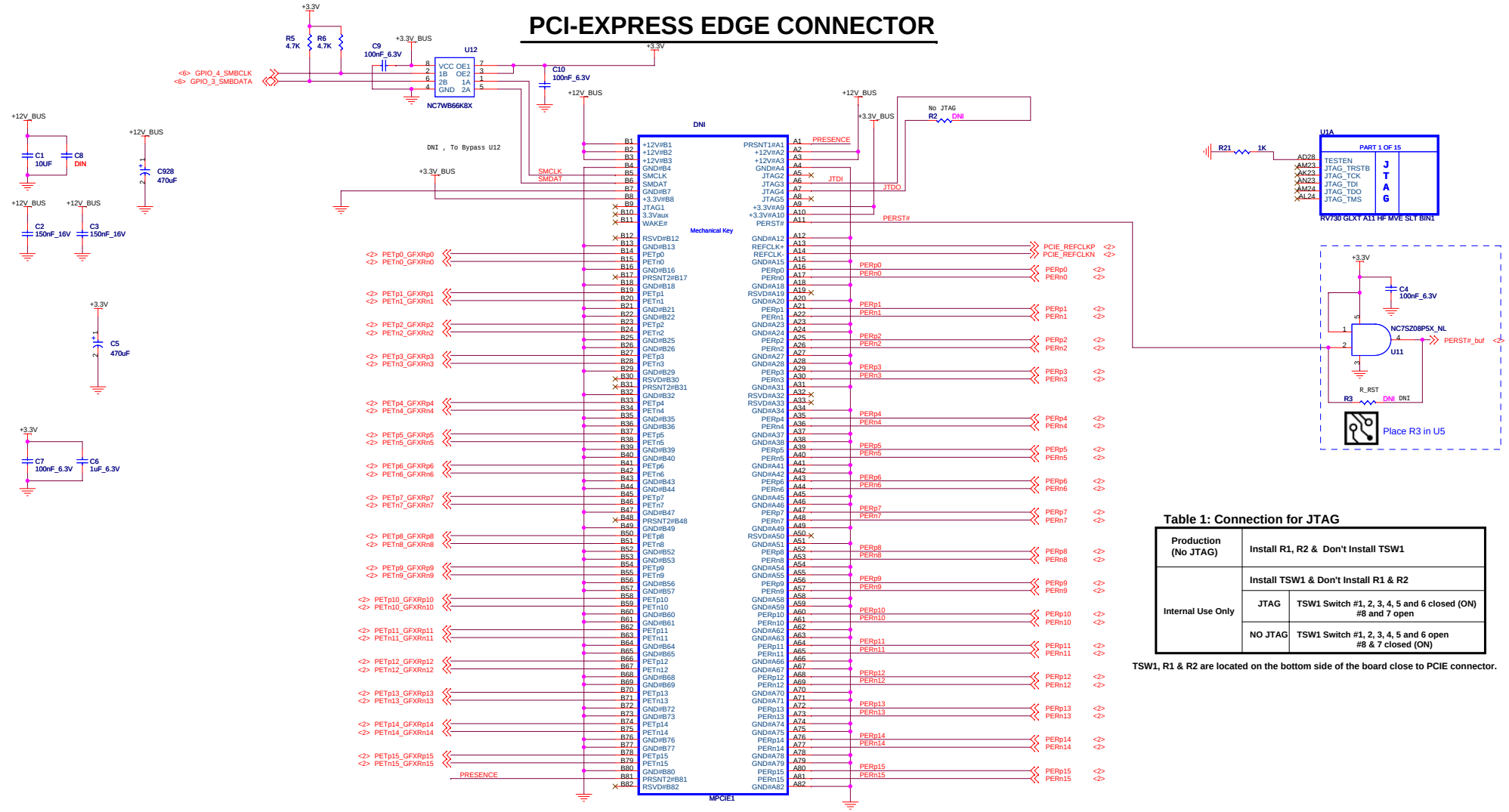

Table 1: Connection for JTAG

Production (No JTAG)	**Install R1, R2 & Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R1 & R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)**

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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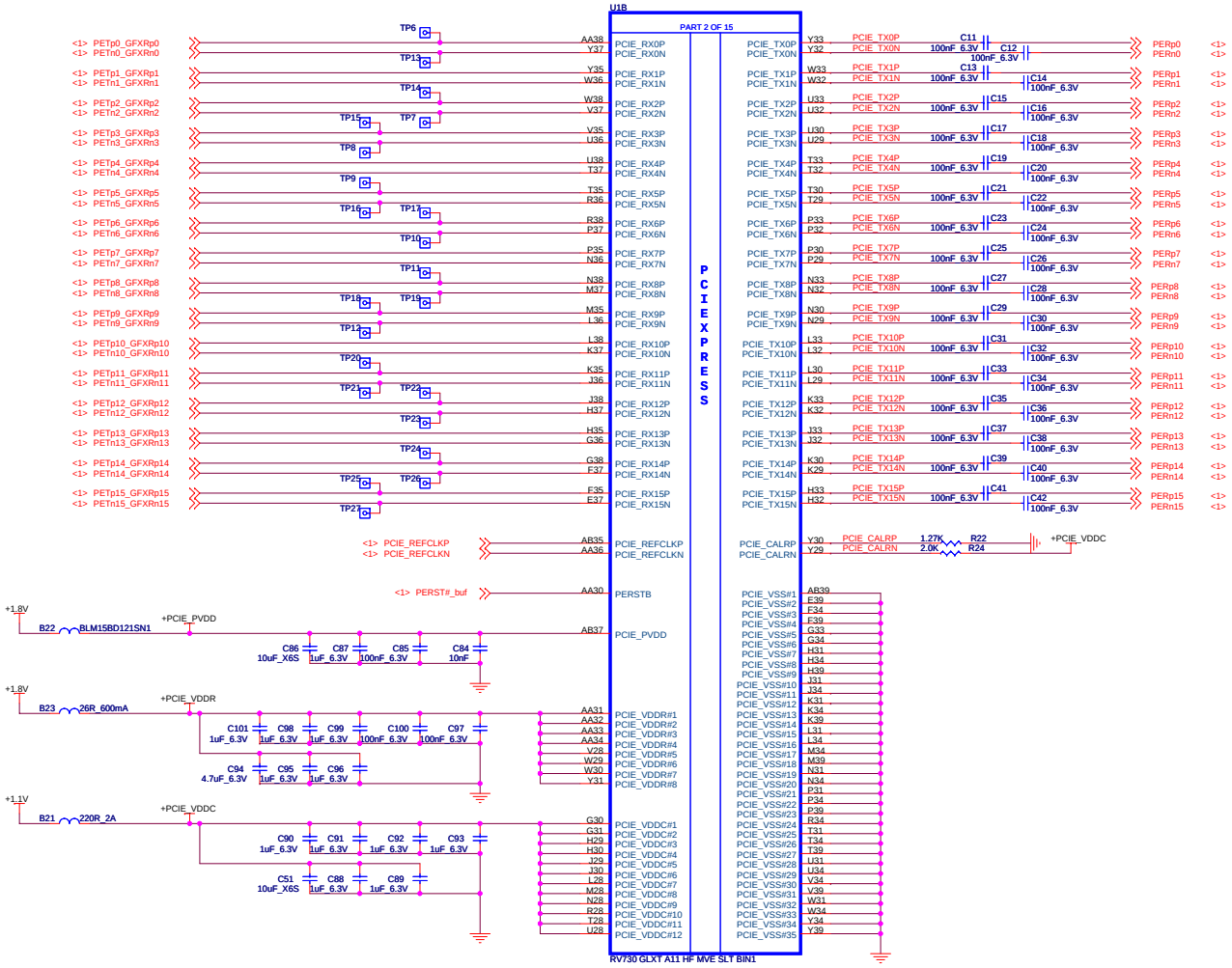
(2) RV730 PCIE Interface

NOTE: some of the PCIE testpoints will be available trought via on traces.



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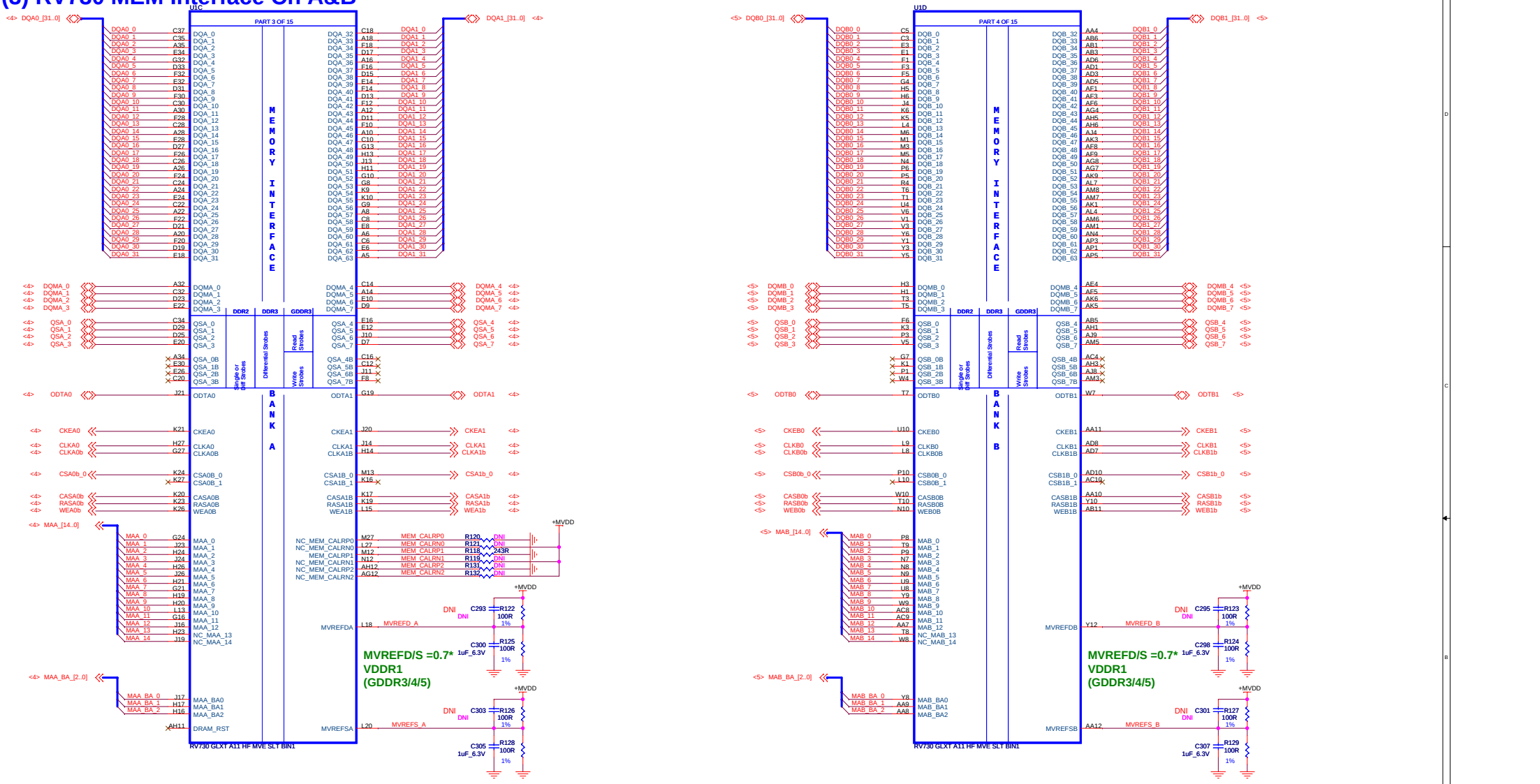
(3) RV730 MEM Interface Ch A&B



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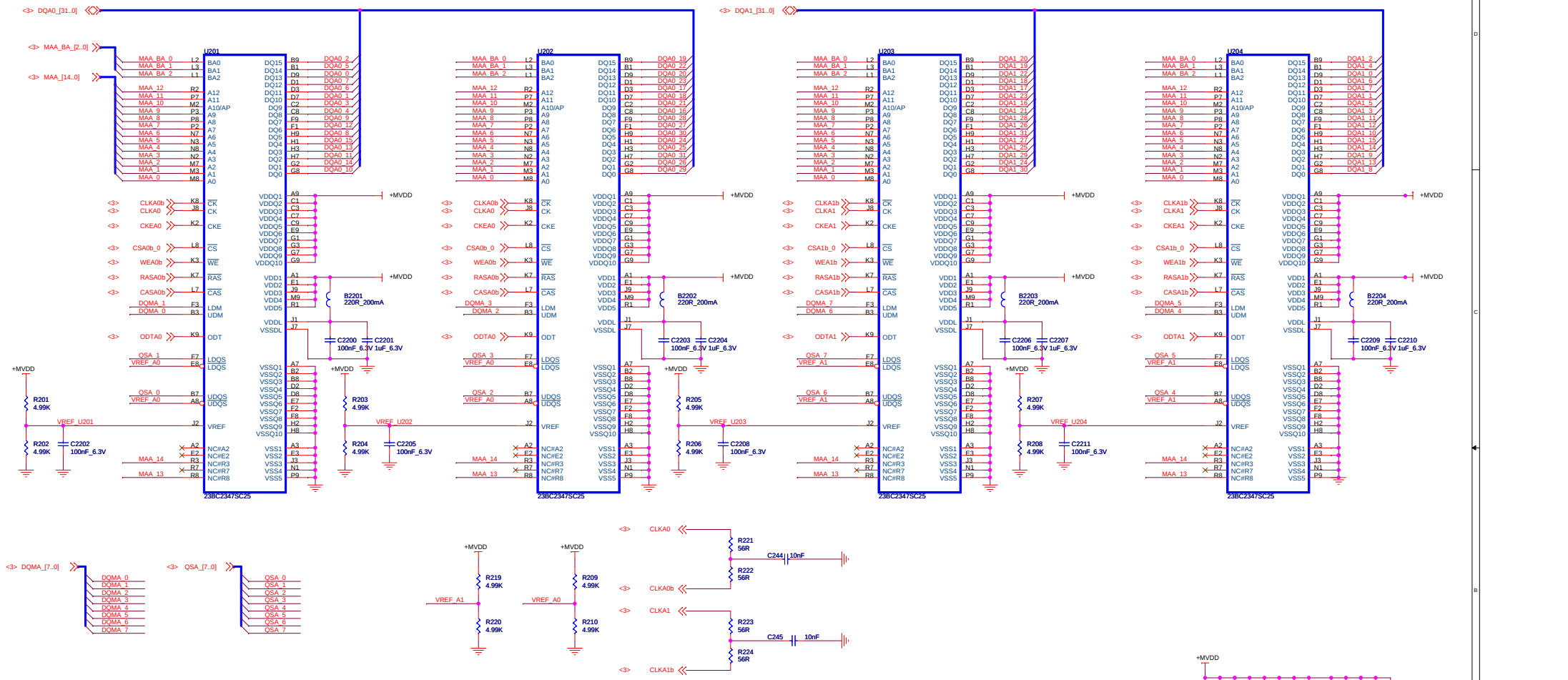
(4) DDR2 Ch A

CHANNEL A: 128MB/256MB DDR2



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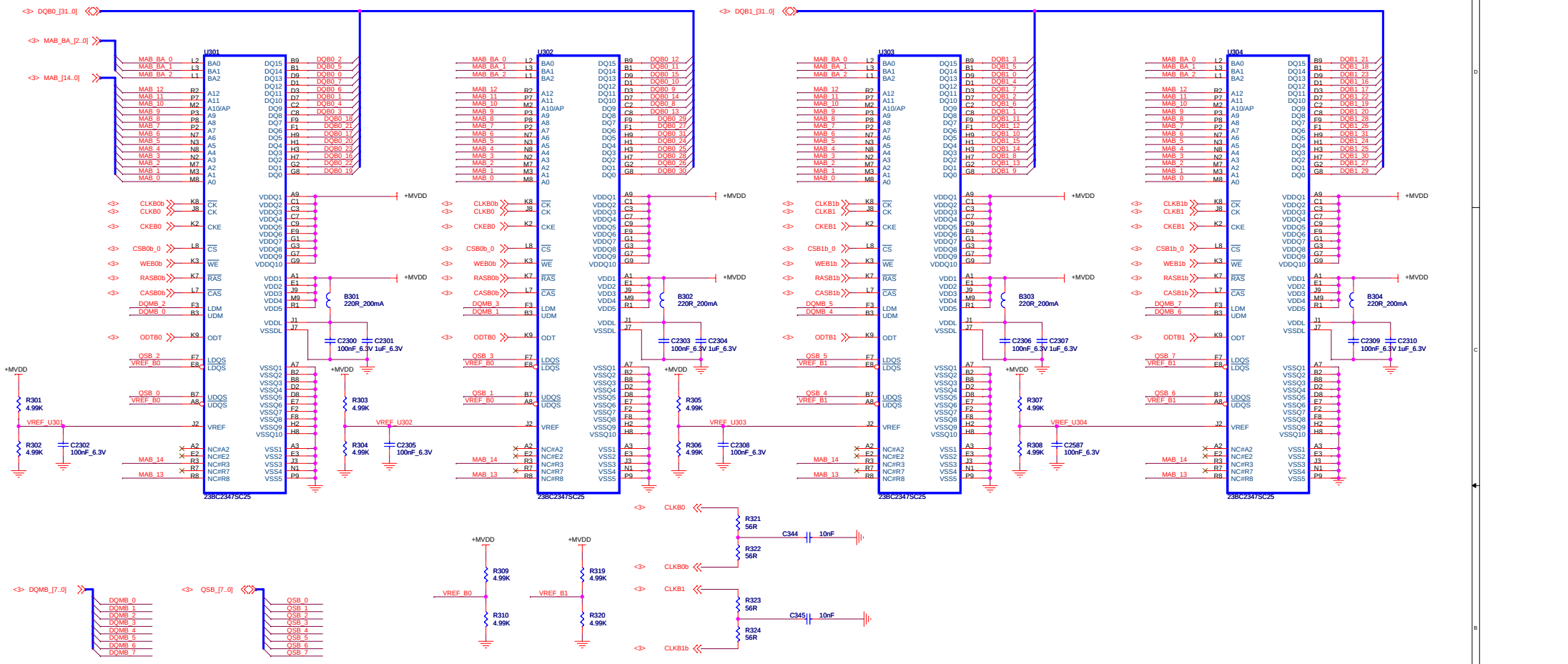
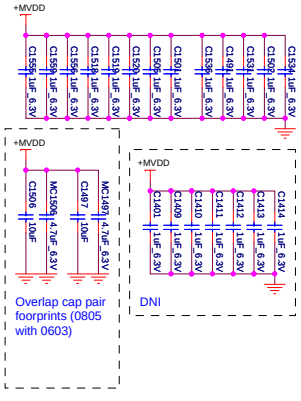
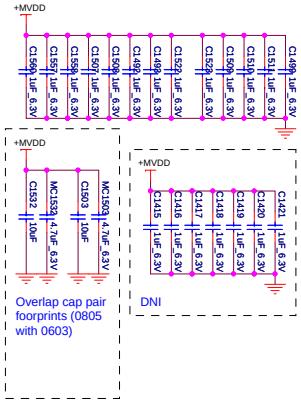
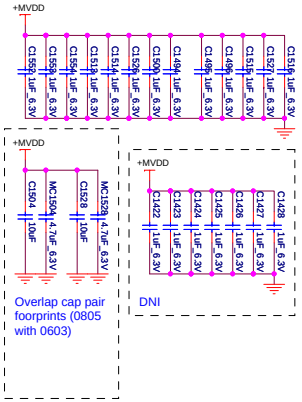
(5) DDR2 Ch B

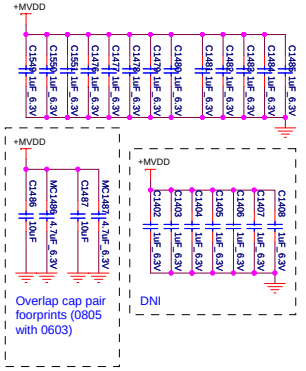
CHANNEL B: 128MB/256MB DDR2











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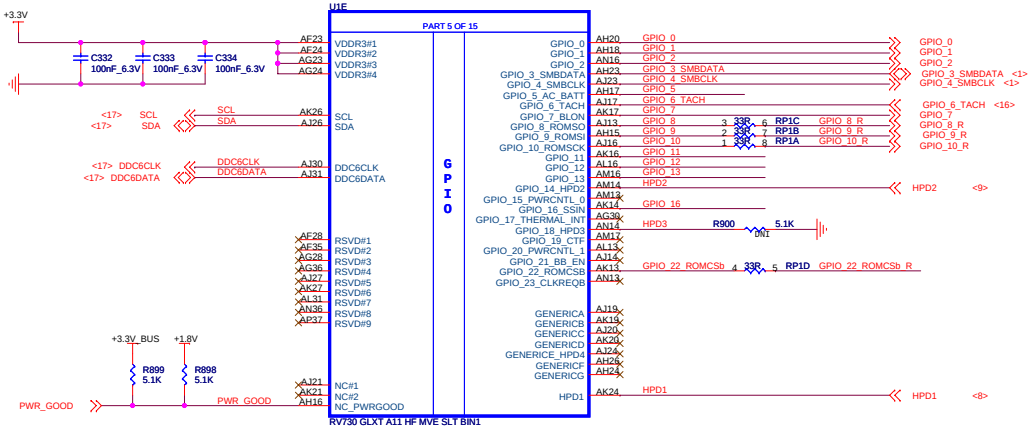
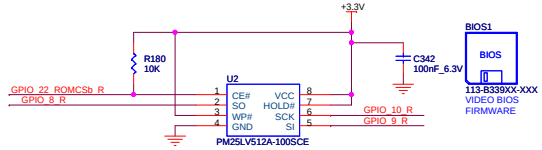
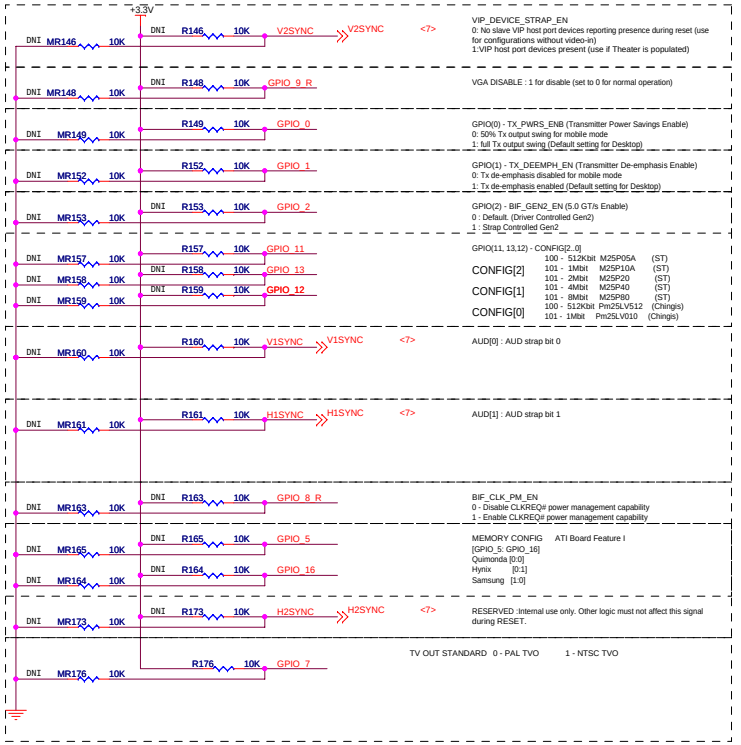
(06) RV730 GPIOs Strap CF XTAL

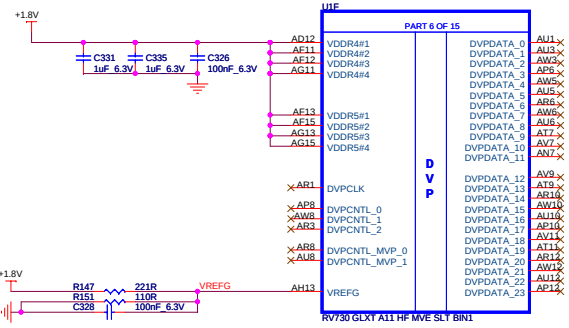


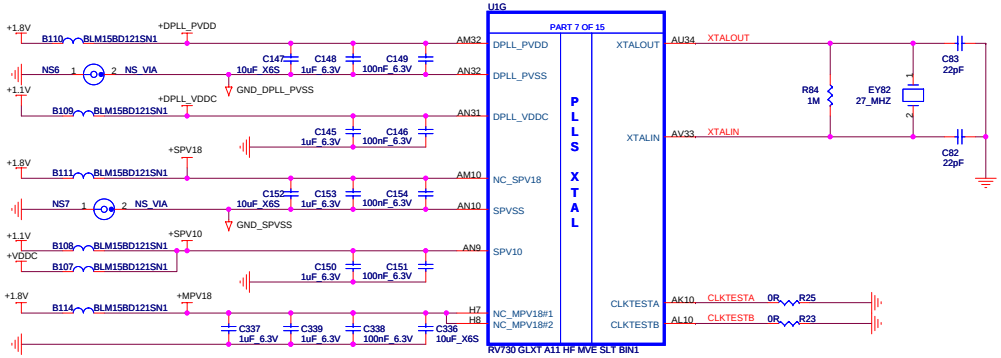


PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

PIN BASED STRAPS







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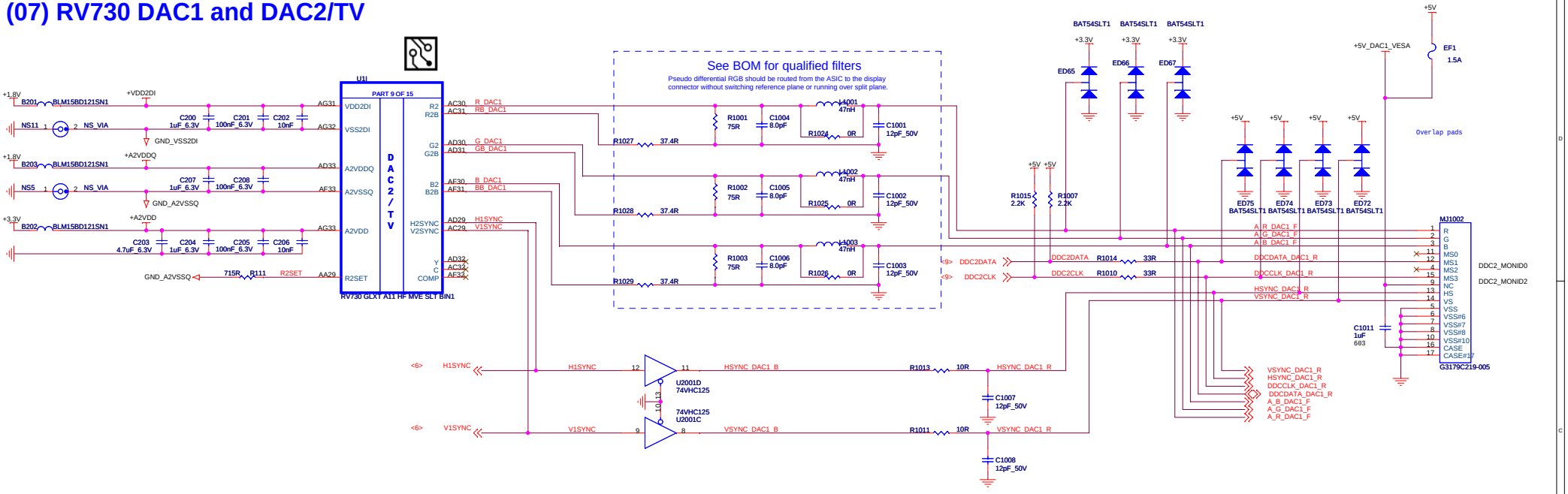
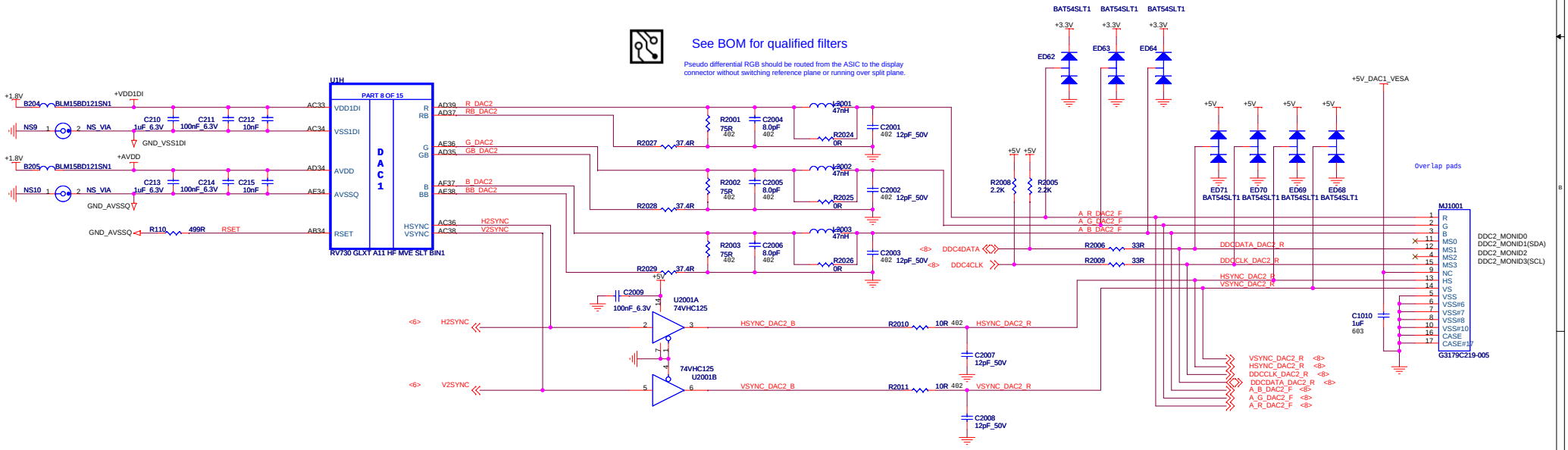
(07) RV730 DAC1 and DAC2/TV





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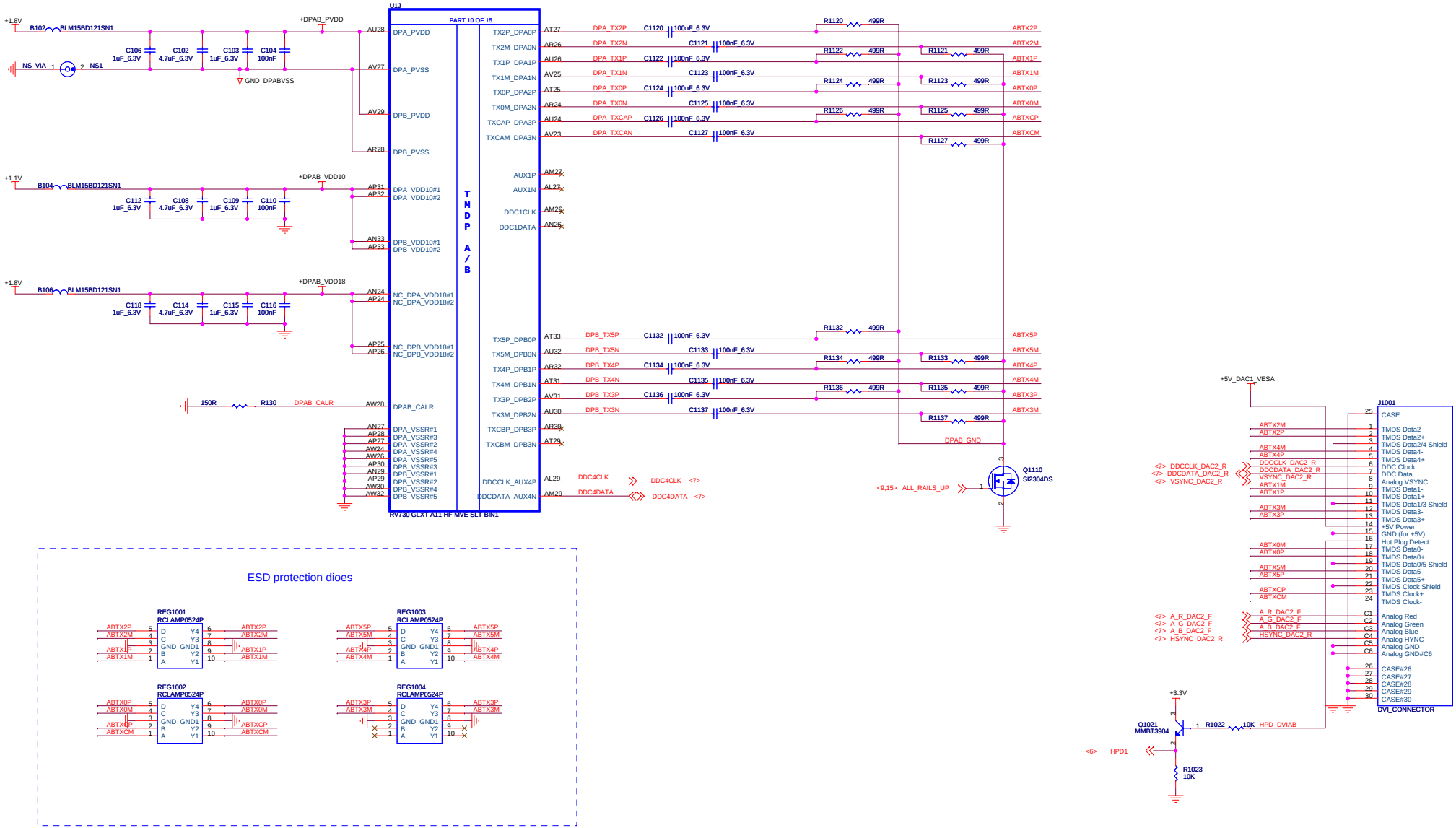
(08) RV730 TMDS A&B



ESD protection dioes

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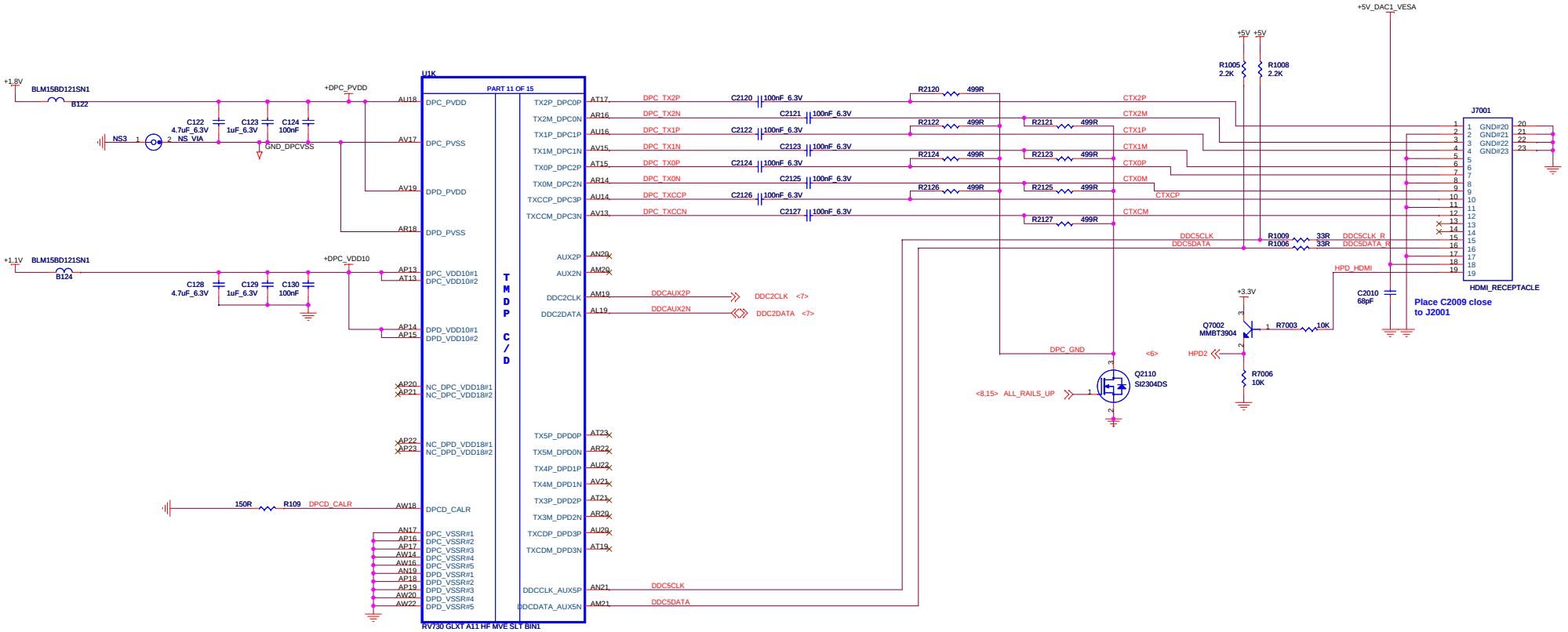
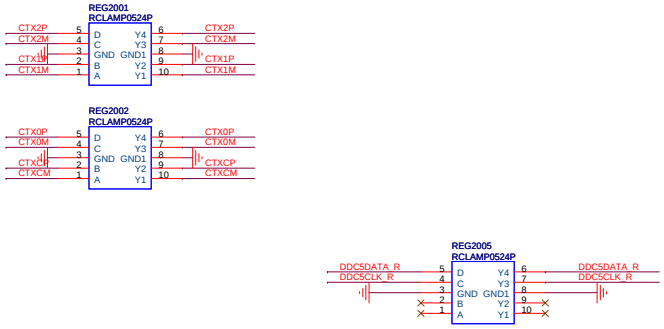
(09) RV730 HDMI and DisplayPort on C&D



ESD protection dioes



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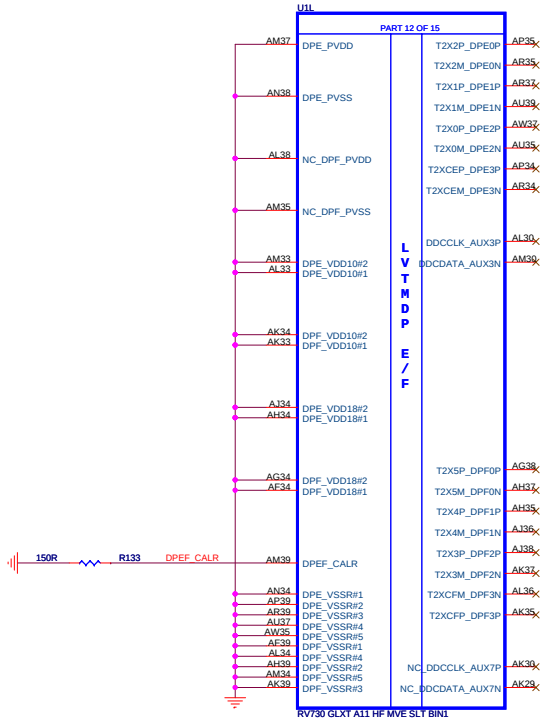
(10) No Connect E&F



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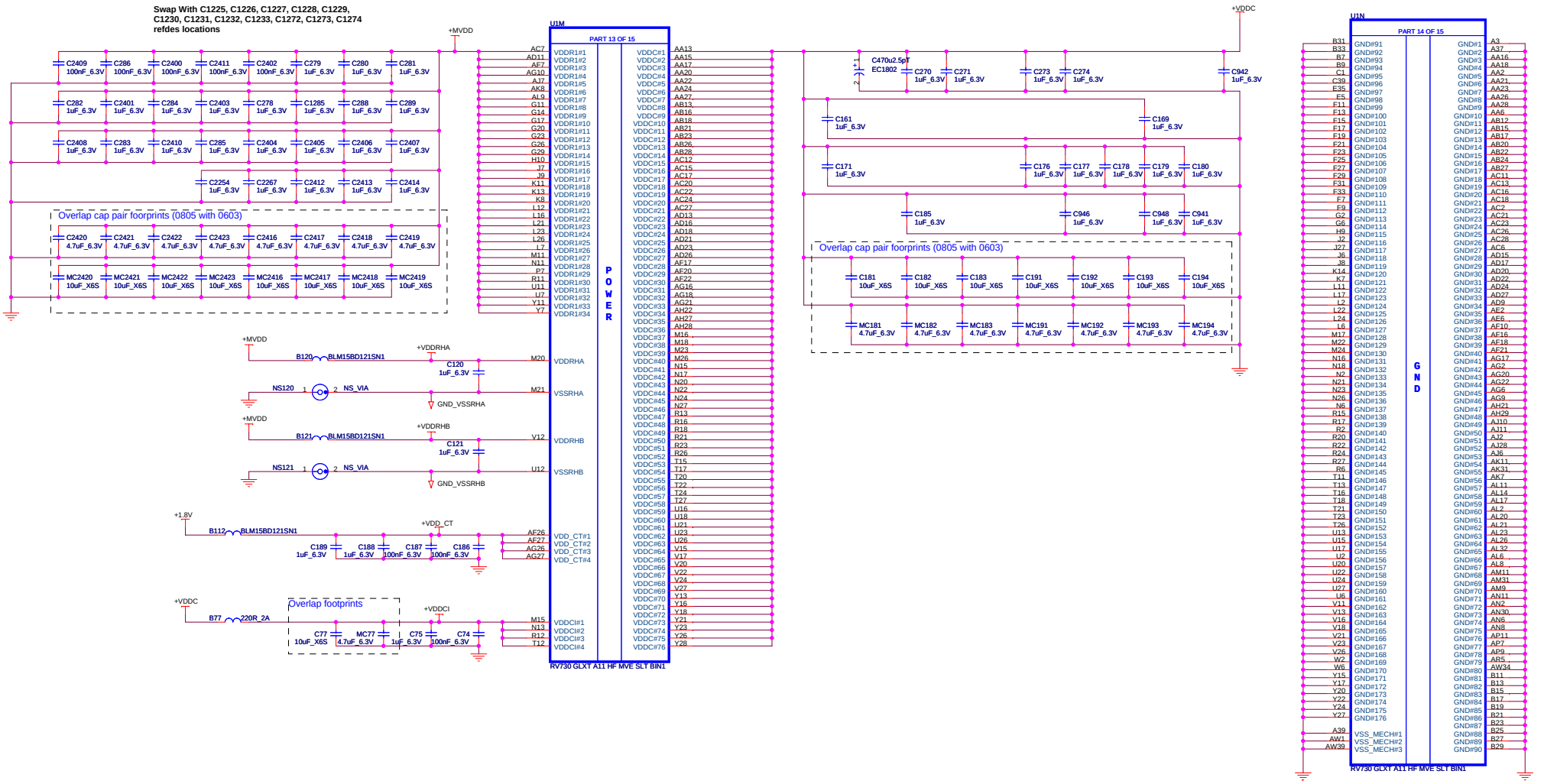
(11) RV730 Power & GND



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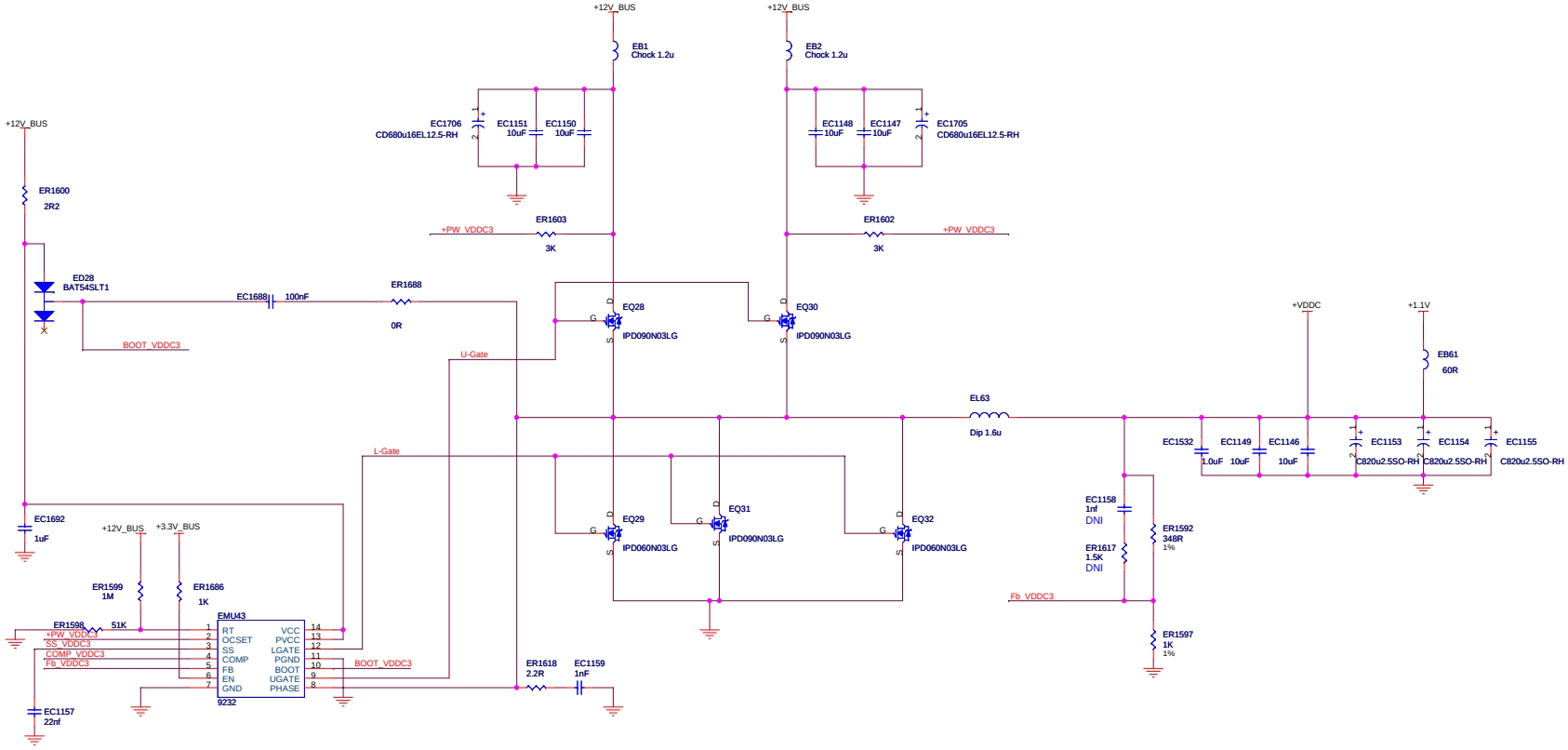
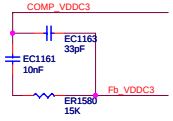
(12) VDDC

CORE REGULATOR VDDC



+VDDC=0.8*(1+(ER1592 / ER1597))

Compensation Circuit



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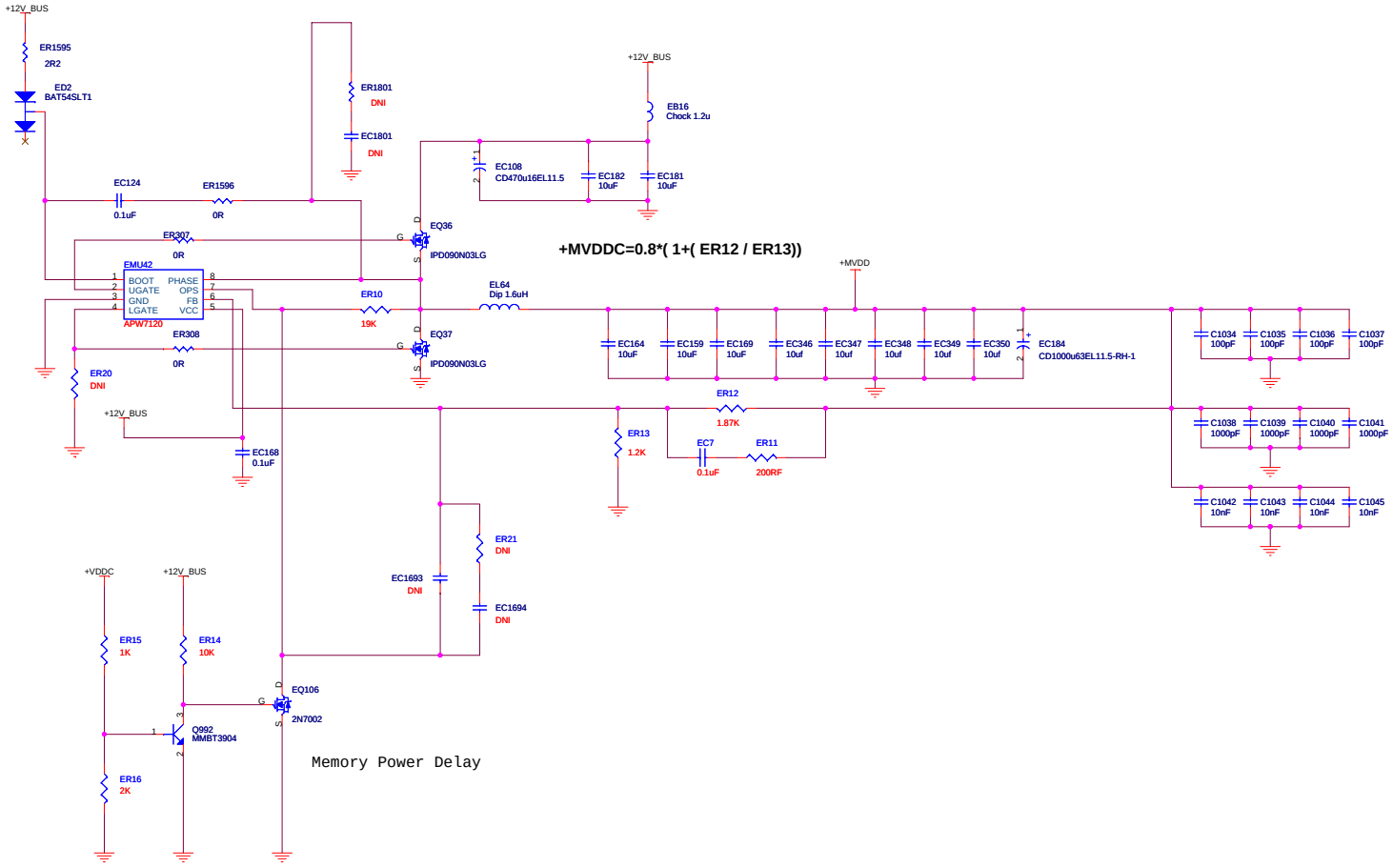
(13) MVDD



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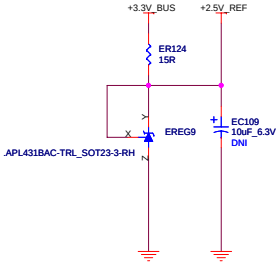
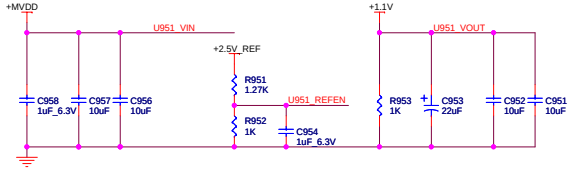
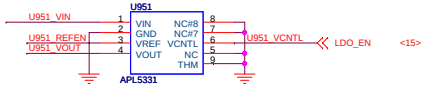
(14) Linear Regulators

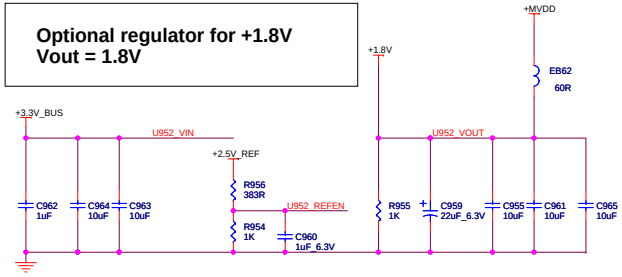


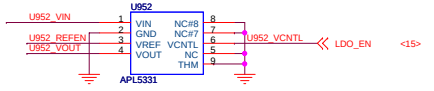
Optional regulator for +1.1V
Vout = 1.1V

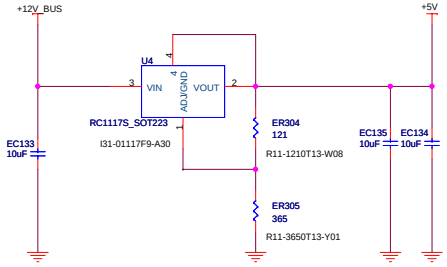




Optional regulator for +1.8V
Vout = 1.8V







Vout=1.25V* [1+(ER305/ER304)]

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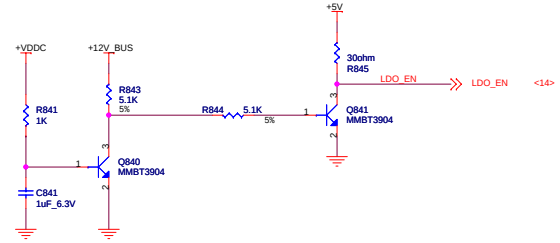
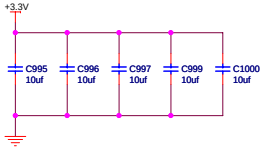
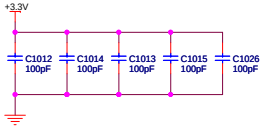
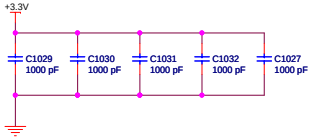
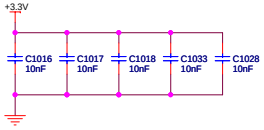
(15) Power Management

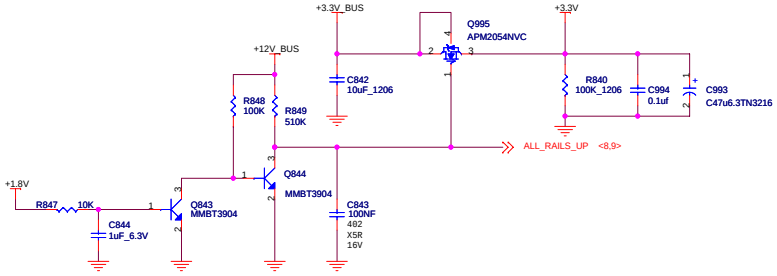












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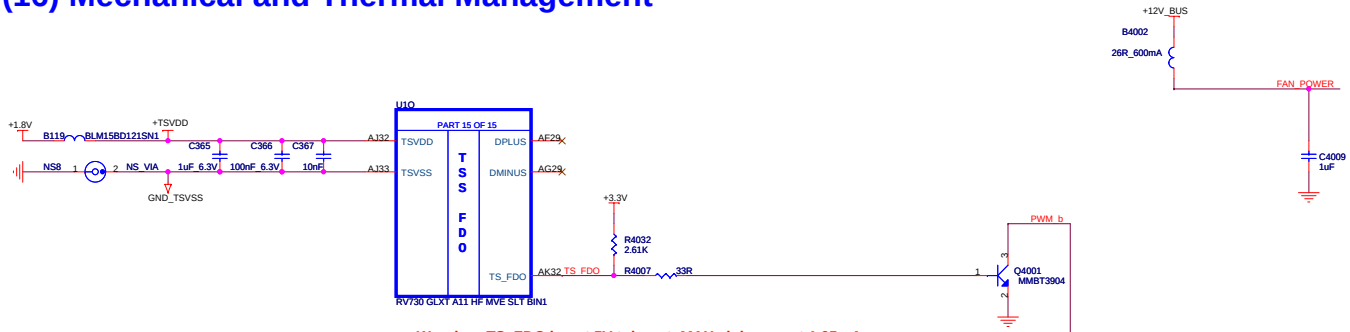
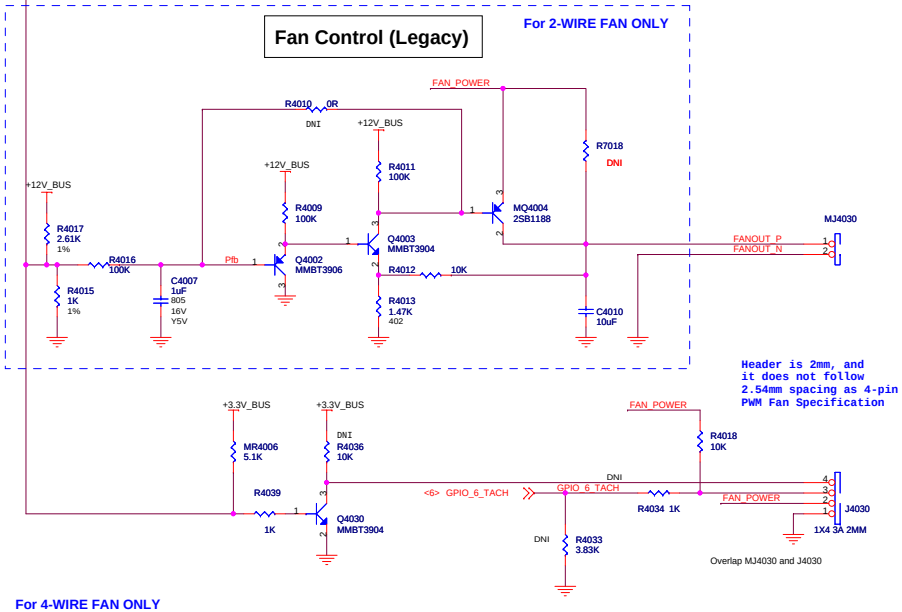
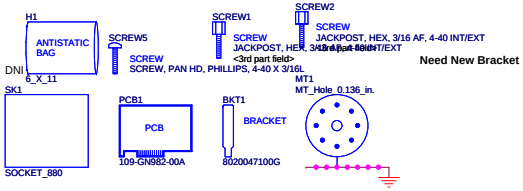
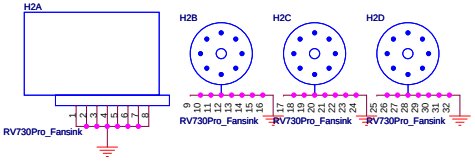
(16) Mechanical and Thermal Management



Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA







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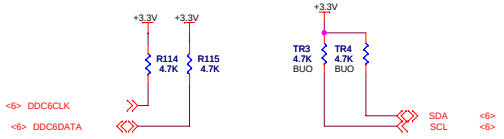
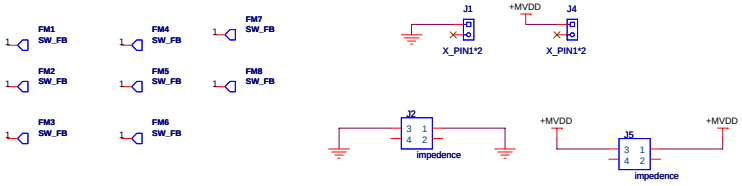
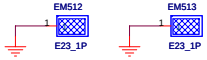
(17) Debug Circuits







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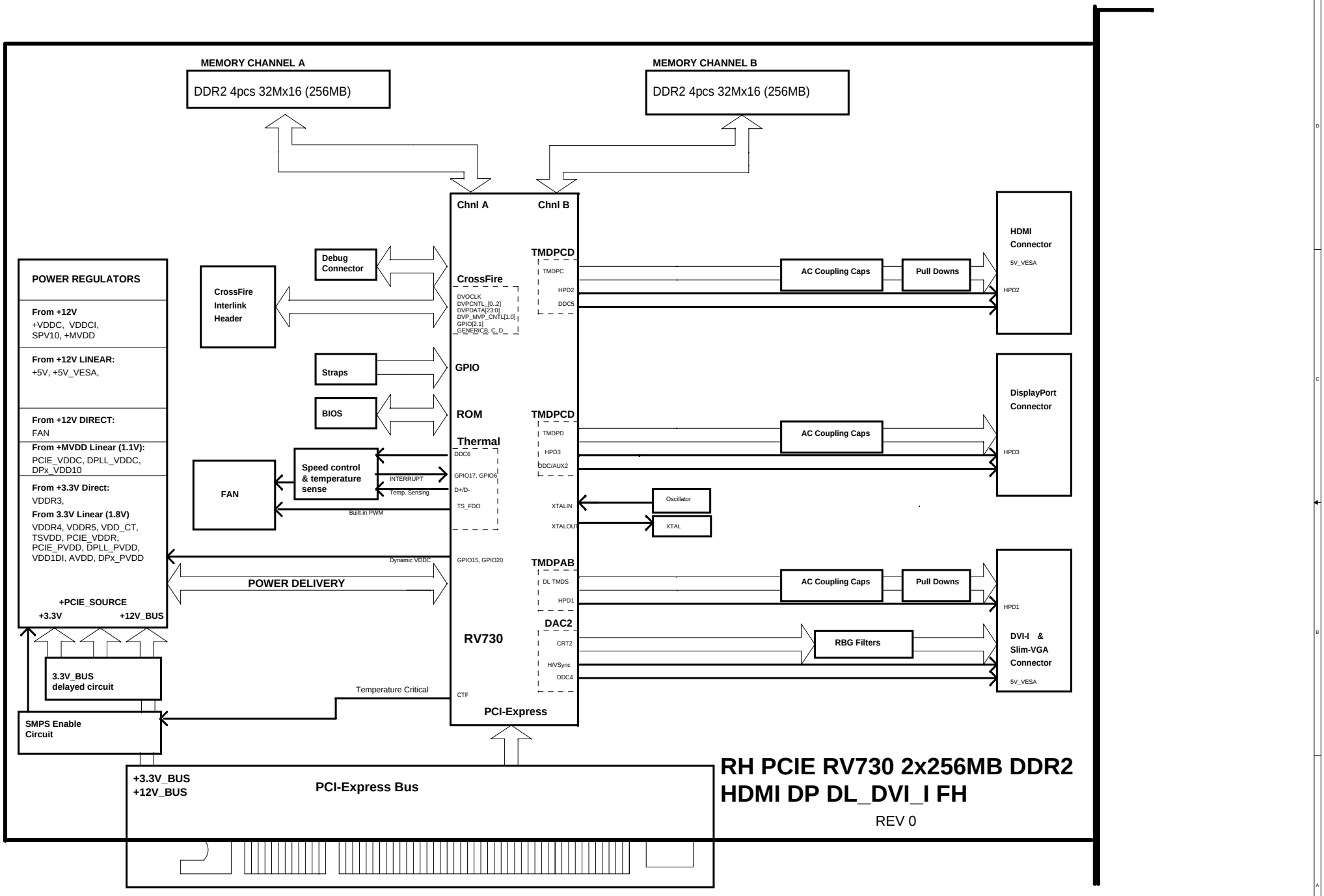

RH PCIE RV730 2x256MB DDR2
HDMI DP DL_DVI_I FH

REV 0

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

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RH RV730 512MB DDR2 DL-DVI DP HDMI FH 6'	105-B665xx-00A	Saturday, July 26, 2008

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	08/04/01	Initial design for RV730 GDDR3