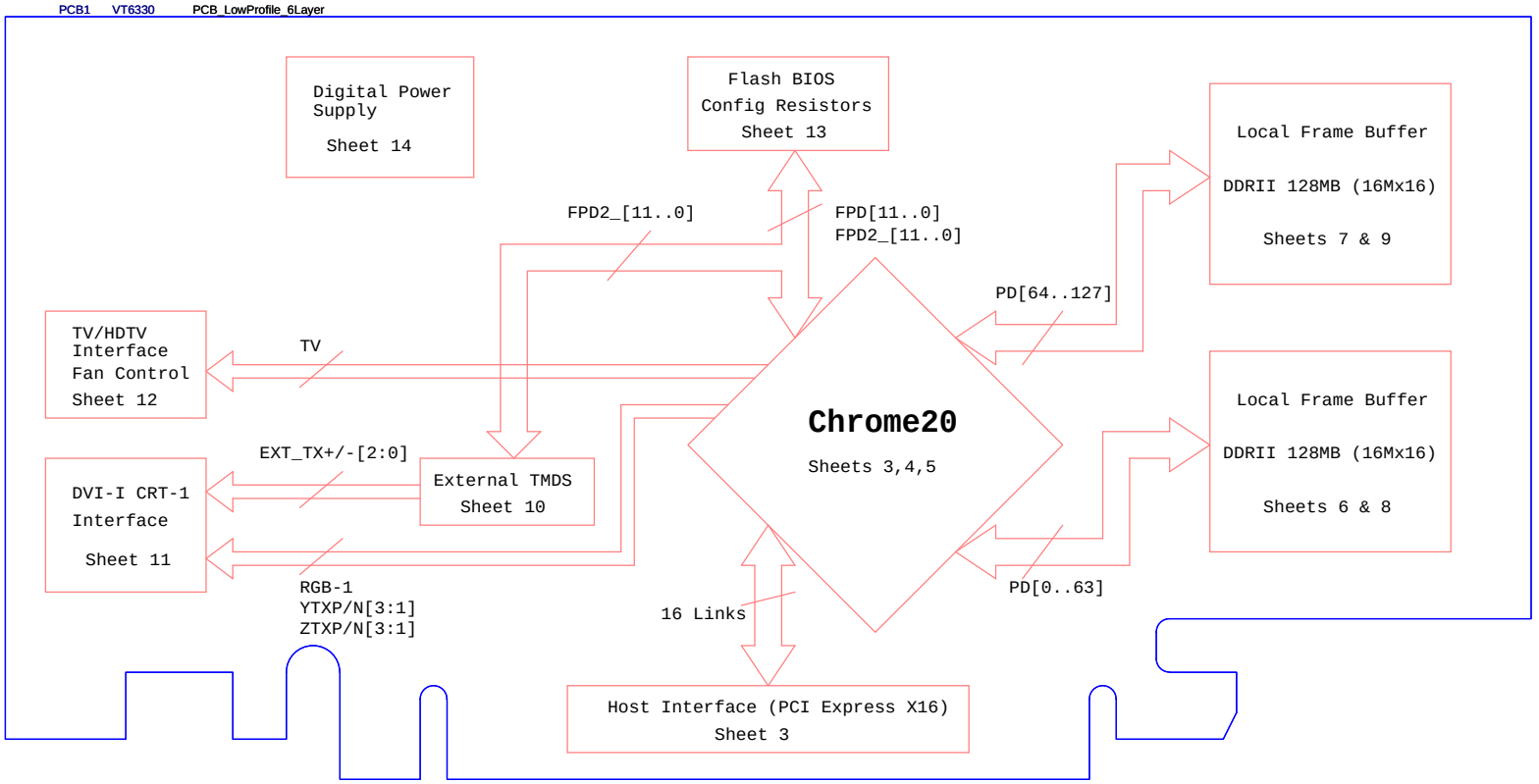
Chrome20 "LOW PROFILE" DESKTOP

Pins	Assignment
GPIO0	*DVI Hot Plug Detect*
GPIO1	*Analog Mux Select*
GPIO2	*TMDS Power Down*
SPDAT/CLK1	*DDC CRT1/DVI1*
SPDAT/CLK2	*DDC CRT2* *I2C Ext TMDS*
SPDAT3	*CTL3 Ext TMDS*

PCB No: VT6330B



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Title: **Block Diagram**

Size: B | Document Number: **VT6330 Chrome20 Low Profile** | Rev: 1B

Date: Wednesday, April 19, 2006 | Sheet 1 of 14

REV	DESCRIPTION OF CHANGE	DATE
0A	Schematic created	01/16/06
A	Added LDO for Internal TMDS/LVDS U20. Changed the formulas for power supply (resistors) Release to Rev A PCB	02/07/06
0B	Unscrambled TV analog mux signals U12 (AYR to Y, AVB to TV_COMP_Pr and ACG to C_Pb) Added resistors R8, R9 to U20 for adjustable regulator option Changed U19 (+5V Regulator) from AMS1117-50 to 7805 Changed U13-U16 from NC7S08 to NC7ST08	02/27/06
1B	Changed DVI Hotplug CN5 pin 14 to GPIO0 from GPIO2 Changed I2C Pullups R105, R106, R142, R143 from 1.2K to 4.7K Changed VMEM compensation circuit values R221 (39 Ohms), C364 (0.1uF), C365 (3300 pF) Do Not Populate R61 and R254 (remove external Eclk option) Added 2 x 100uF C106, C107 to VCORE and 2 x 100uF C108, C109 to VMEM Changed VMEM to 2.0V R226 = 1.54K and VTT to 1.0V R223 = 1.5K Changed R139 from DNP to Stuff for SPDAT3 to CTL3 Changed L6 to 1uH from 0.54uH Added 0 Ohm R6 option for 3.3V connected to TMDS_VCC if External TMDS not used. Changed C289,C290,C309,C310 from 220pF to 22pF for Hsync and VSync Remove R1 and short TVGND to GND Changed R84,R86,R88,R90,R92,R94,R96,R98 from 0402 size to 0603 size Added Bridge Resistors R10,R11,R12,R13 across TMDS differential signals	03/03/06

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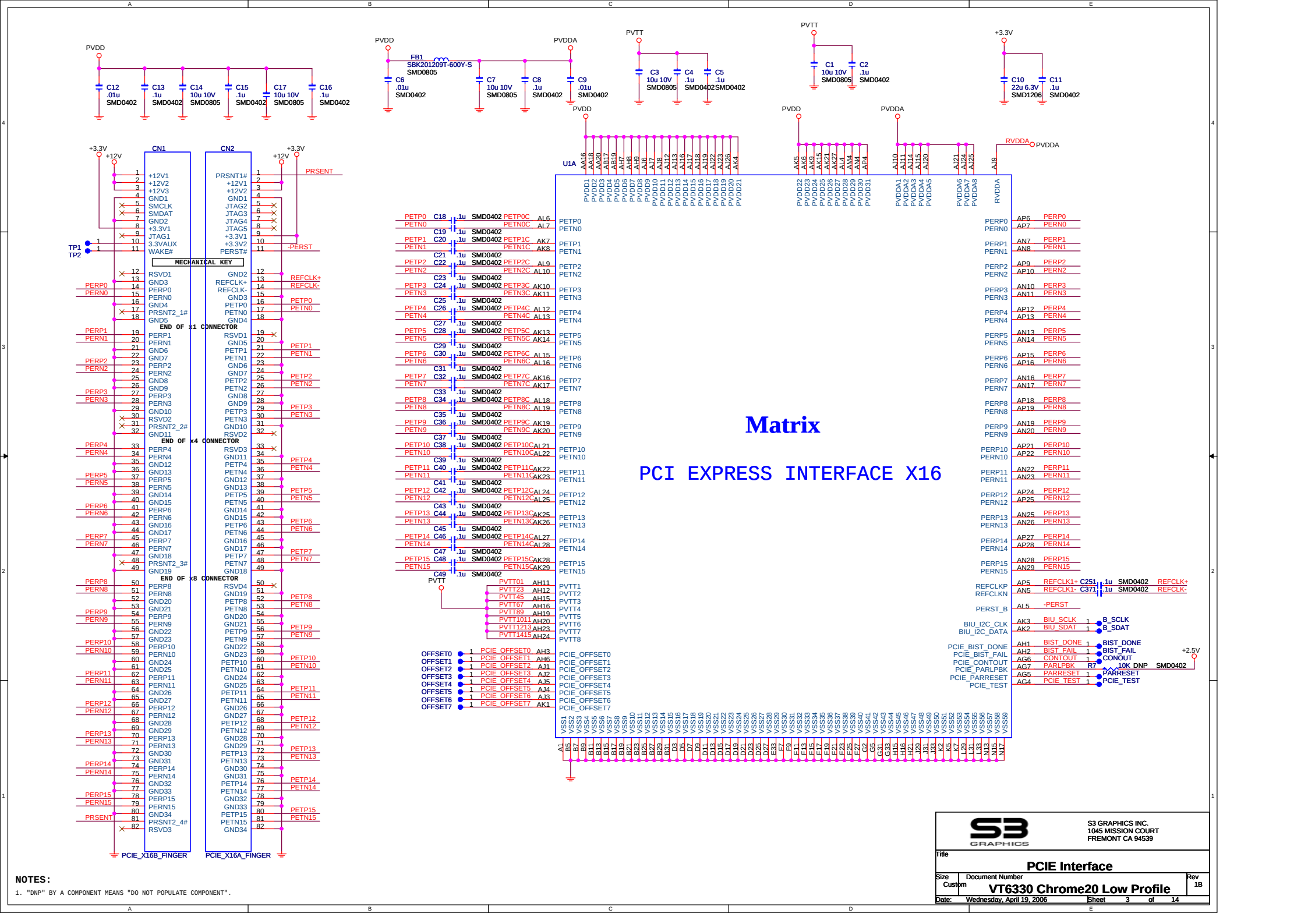
Title

Design Change History

Size	Document Number	Rev
A	VT6330 Chrome20 Low Profile	1B

Date: Wednesday, April 19, 2006 Sheet 2 of 14


Matrix
PCI EXPRESS INTERFACE X16
PCIE_X16B_FINGER
PCIE_X16A_FINGER
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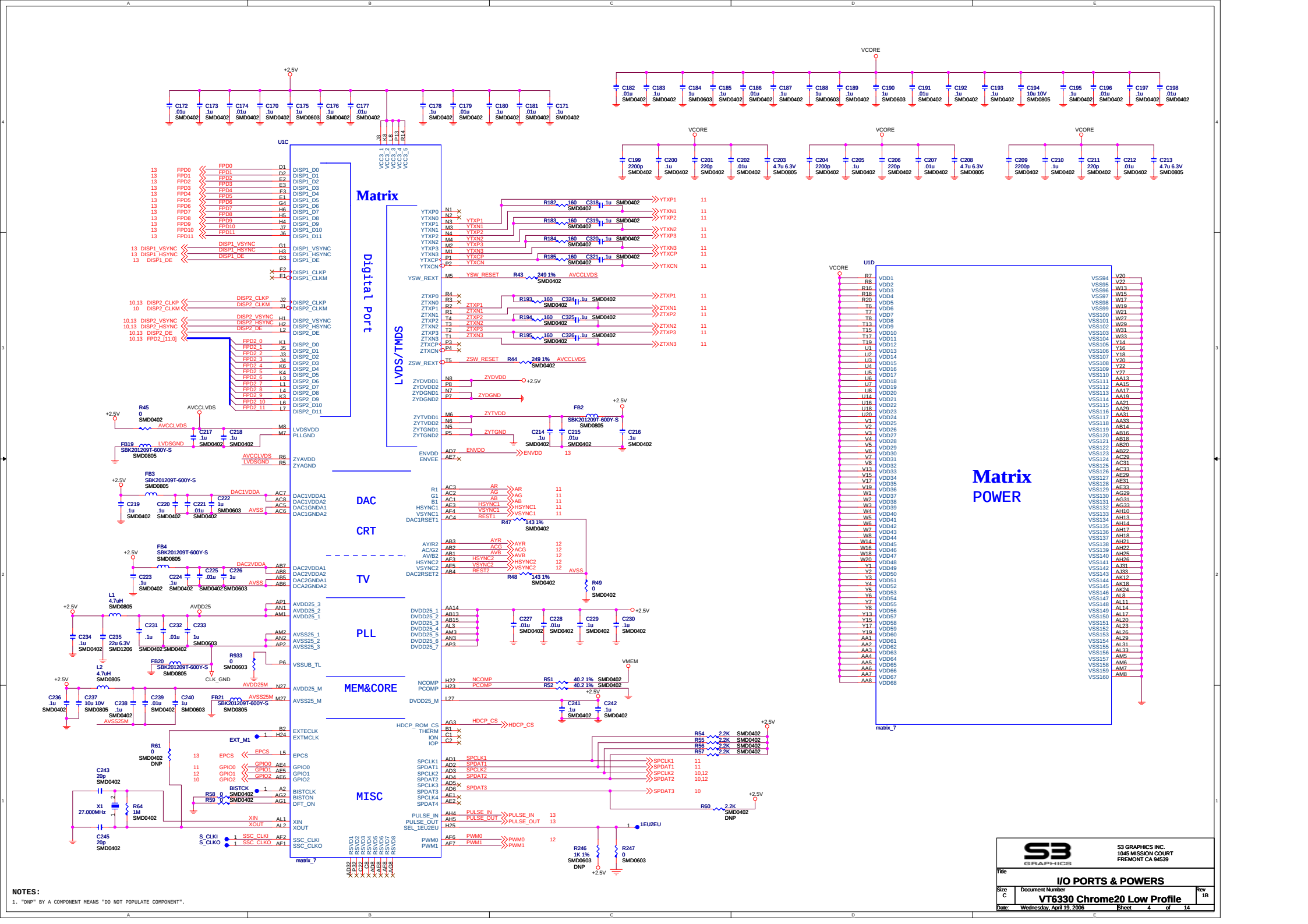
PCIE Interface
VT6330 Chrome20 Low Profile
Wednesday, April 19, 2006
NOTES:
1. "DNP" BY A COMPONENT MEANS "DO NOT POPULATE COMPONENT".


Matrix
Digital Port
LVDS/TMDS
DAC
CRT
TV
PLL
MEM&CORE
MISC
Matrix
POWER
U1C
U1D
matrix_7
matrix_7
VCORE
+2.5V
VMEM
1EU2EU
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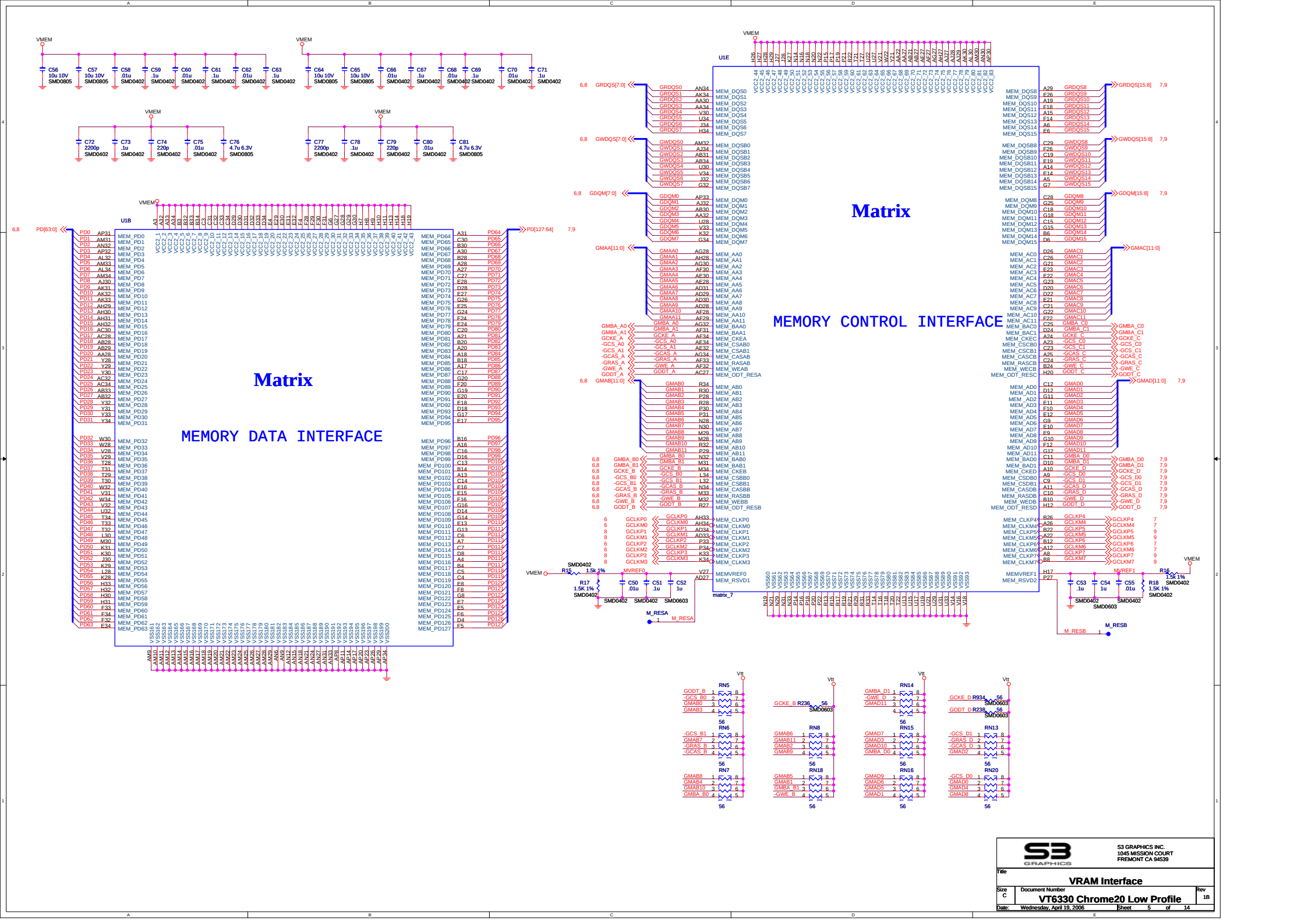
I/O PORTS & POWERS
VT6330 Chrome20 Low Profile
Wednesday, April 19, 2006
NOTES:
1. "DNP" BY A COMPONENT MEANS "DO NOT POPULATE COMPONENT".


Matrix
MEMORY DATA INTERFACE
Matrix
MEMORY CONTROL INTERFACE
U1B
U1E
matrix_7
VMEM
C56 10u 10V SMD0805
C57 10u 10V SMD0805
C58 .01u SMD0402
C59 .1u SMD0402
C60 .01u SMD0402
C61 .1u SMD0402
C62 .01u SMD0402
C63 .1u SMD0402
C64 10u 10V SMD0805
C65 10u 10V SMD0805
C66 .01u SMD0402
C67 .1u SMD0402
C68 .01u SMD0402
C69 .1u SMD0402
C70 .01u SMD0402
C71 .1u SMD0402
C72 2200p SMD0402
C73 .1u SMD0402
C74 220p SMD0402
C75 .01u SMD0402
C76 4.7u 6.3V SMD0805
C77 2200p SMD0402
C78 .1u SMD0402
C79 220p SMD0402
C80 .01u SMD0402
C81 4.7u 6.3V SMD0805
PD[63:0]
PD[127:64]
MEM_PD0
MEM_PD1
MEM_PD2
MEM_PD3
MEM_PD4
MEM_PD5
MEM_PD6
MEM_PD7
MEM_PD8
MEM_PD9
MEM_PD10
MEM_PD11
MEM_PD12
MEM_PD13
MEM_PD14
MEM_PD15
MEM_PD16
MEM_PD17
MEM_PD18
MEM_PD19
MEM_PD20
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MEM_PD98
MEM_PD99
MEM_PD100
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MEM_PD118
MEM_PD119
MEM_PD120
MEM_PD121
MEM_PD122
MEM_PD123
MEM_PD124
MEM_PD125
MEM_PD126
MEM_PD127
GRDQS[7:0]
GWDQS[7:0]
GDQM[7:0]
GMAA[11:0]
GMBA[11:0]
GRDQS[15:8]
GWDQS[15:8]
GDQM[15:8]
GMAC[11:0]
GMAD[11:0]
GMBA_A0
GMBA_A1
GCKE_A
-GCS_A0
-GCS_A1
-GCAS_A
-GRAS_A
-GWE_A
GODT_A
GMBA_B0
GMBA_B1
GCKE_B
-GCS_B0
-GCS_B1
-GCAS_B
-GRAS_B
-GWE_B
GODT_B
GMBA_C0
GMBA_C1
GCKE_C
-GCS_C0
-GCS_C1
-GCAS_C
-GRAS_C
-GWE_C
GODT_C
GMBA_D0
GMBA_D1
GCKE_D
-GCS_D0
-GCS_D1
-GCAS_D
-GRAS_D
-GWE_D
GODT_D
GCLKP0
GCLKM0
GCLKP1
GCLKM1
GCLKP2
GCLKM2
GCLKP3
GCLKM3
GCLKP4
GCLKM4
GCLKP5
GCLKM5
GCLKP6
GCLKM6
GCLKP7
GCLKM7
MVREF0
MVREF1
M_RESA
M_RESB
R15 1.5K 1%
R16 1.5K 1%
R17 1.5K 1%
R18 1.5K 1%
RN5
RN6
RN7
RN8
RN13
RN14
RN15
RN16
RN18
RN20
R934 56
R236 56
R238 56
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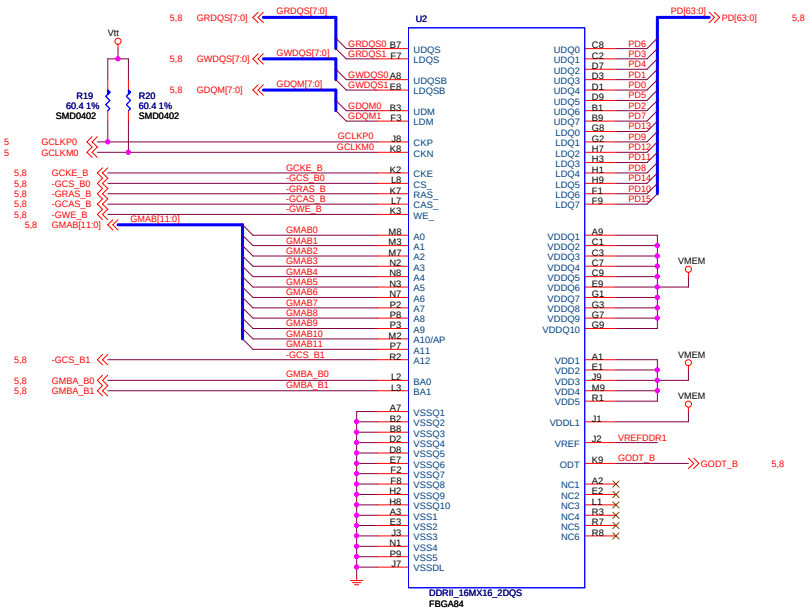
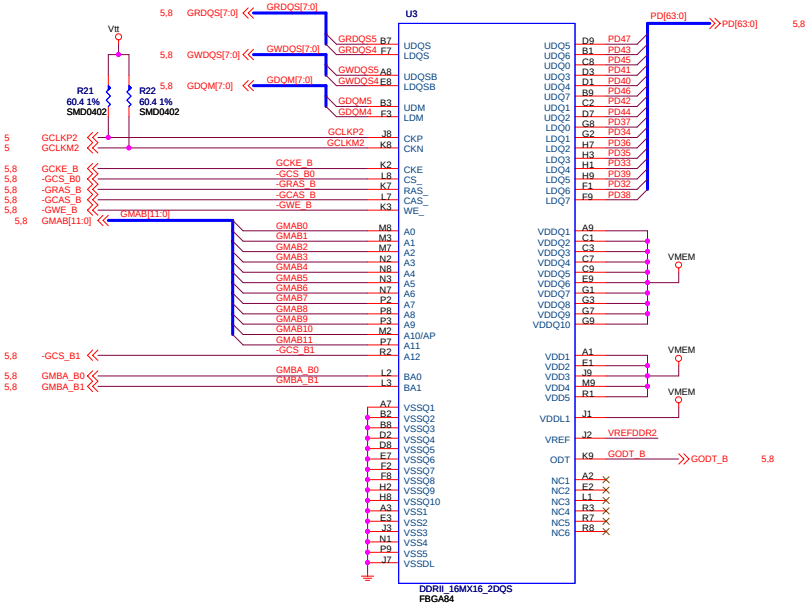
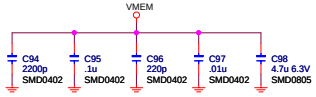
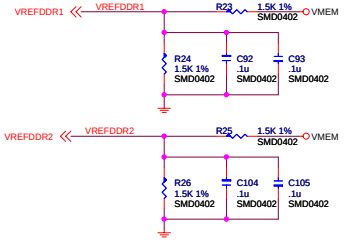
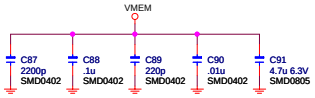
Title
VRAM Interface
Size C
Document Number
VT6330 Chrome20 Low Profile
Rev 1B
Date: Wednesday, April 19, 2006
Sheet 5 of 14











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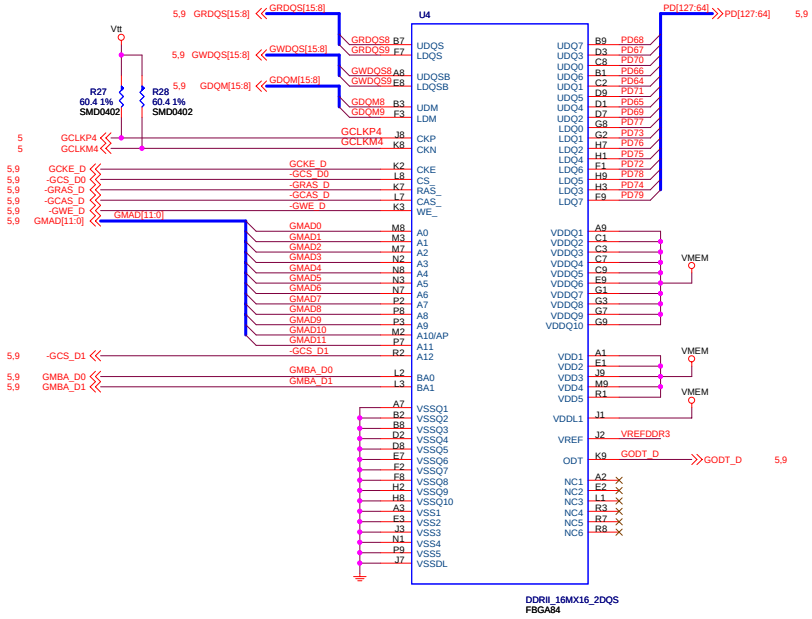
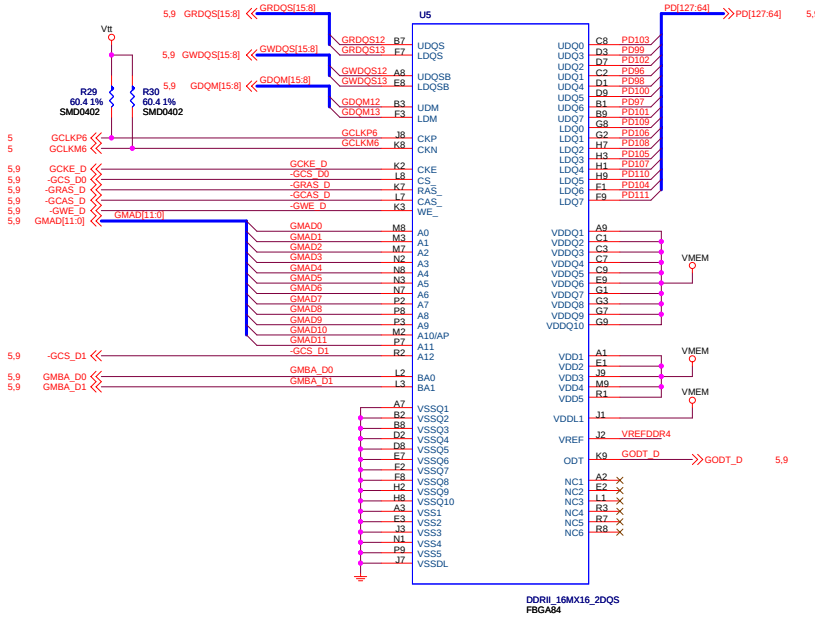
FREMONT CA 94539

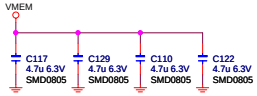
Title: 1st 32-BIT DDRII 16Mx16

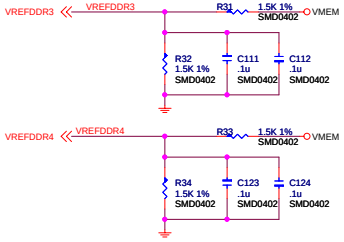
Size: C | Document Number: VT6330 Chrome20 Low Profile | Rev: 1B

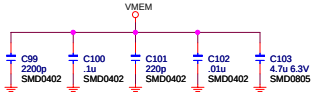
Date: Wednesday, April 19, 2006 | Sheet 6 of 14











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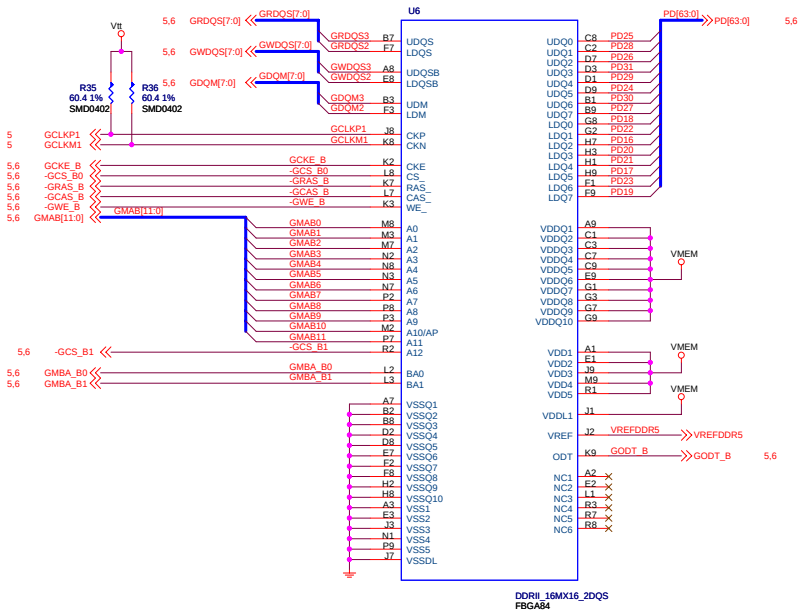
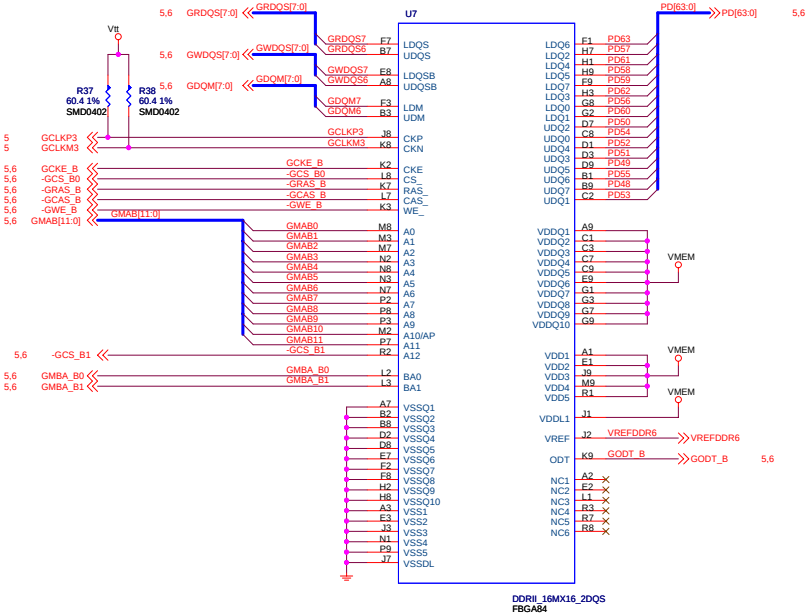
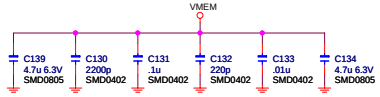
Title: 2nd 32-BIT DDRII 16Mx16

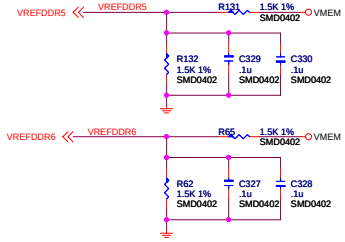
Size	Document Number	Rev
C	VT6330 Chrome20 Low Profile	1B

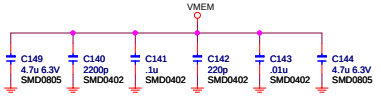
Date: Wednesday, April 19, 2006 Sheet 7 of 14











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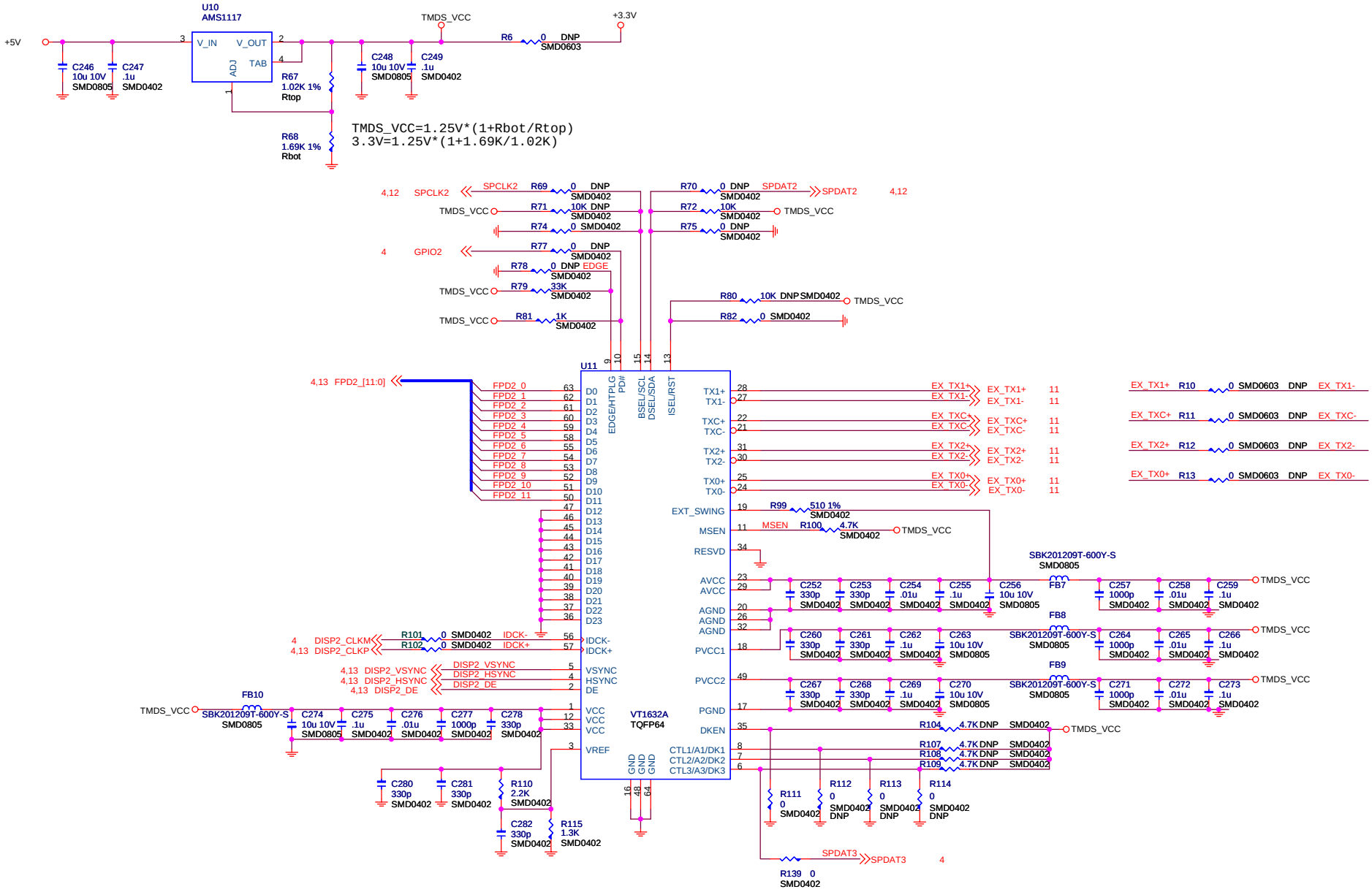
FREMONT CA 94539

Title: 3rd 32-BIT DDRII 16Mx16

Size: C | Document Number: VT6330 Chrome20 Low Profile | Rev: 1B

Date: Wednesday, April 19, 2006 | Sheet 8 of 14



NOTES:

1. "DNP" BY A COMPONENT MEANS "DO NOT POPULATE COMPONENT".

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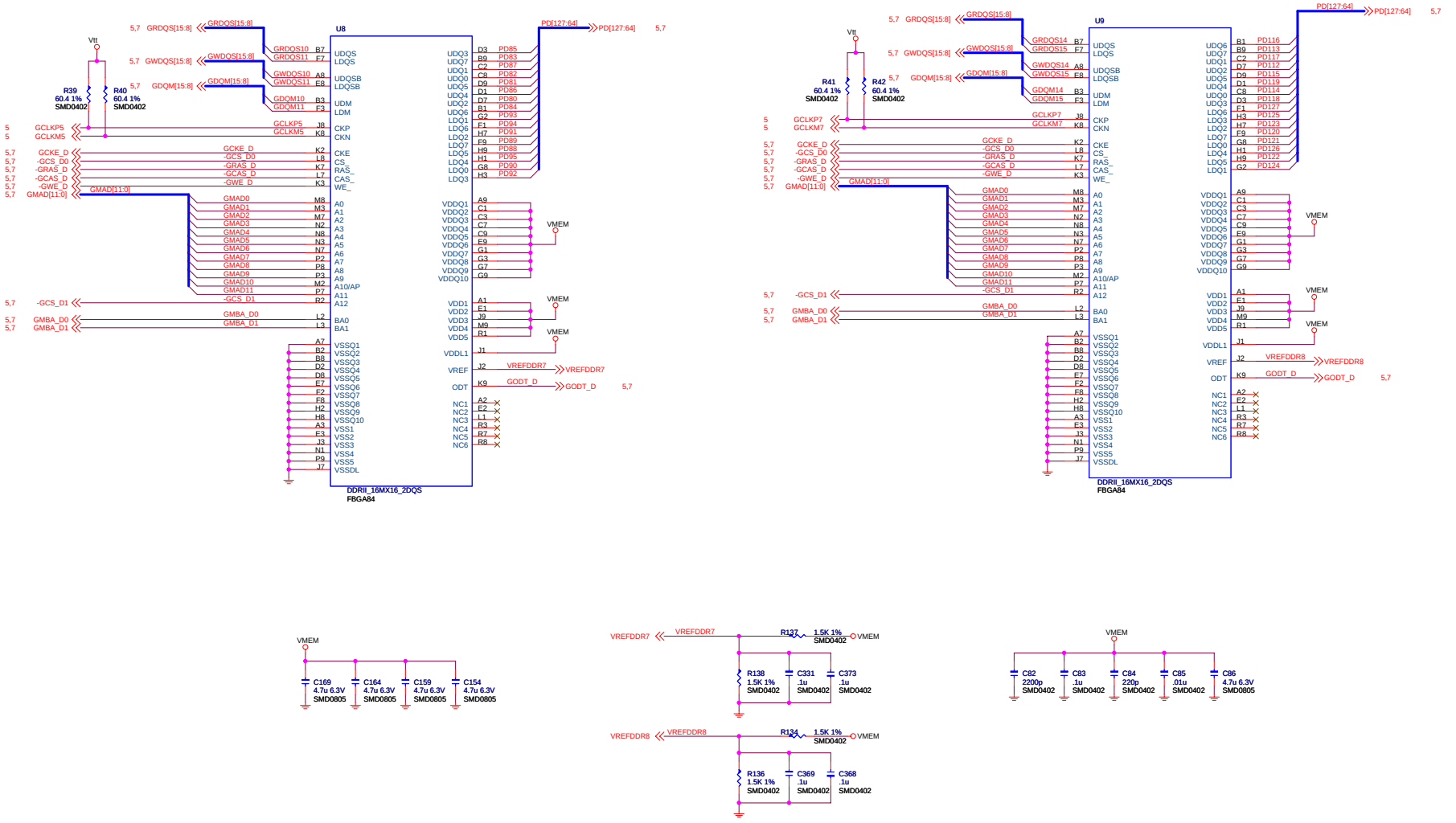
Title: **EXTERNAL TMDS**

Size: B | Document Number: **VT6330 Chrome20 Low Profile** | Rev: 1B

Date: Wednesday, April 19, 2006 | Sheet 10 of 14



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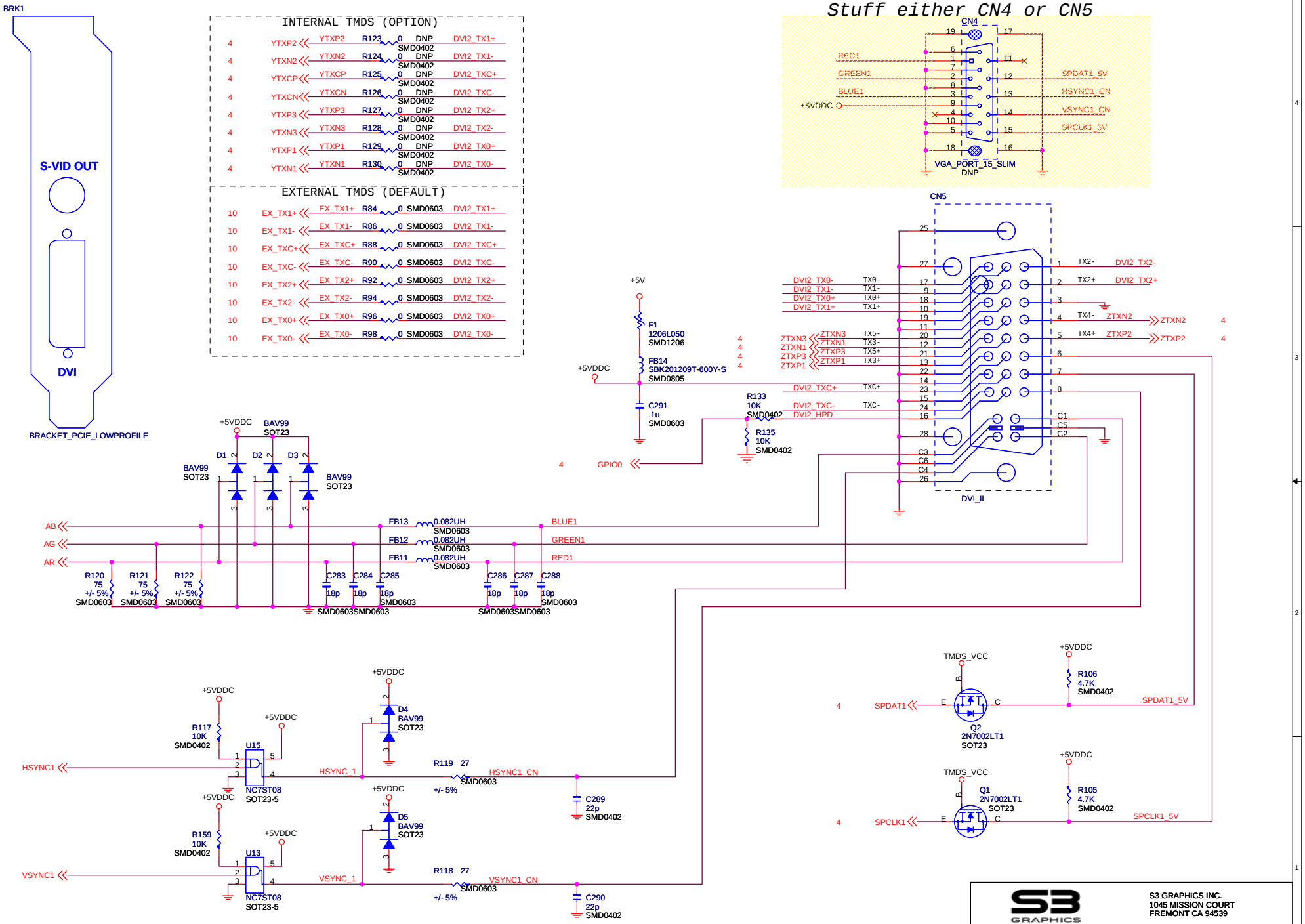
Title: 4th 32-BIT DDRII 16Mx16

Size: C | Document Number: VT6330 Chrome20 Low Profile | Rev: 1B

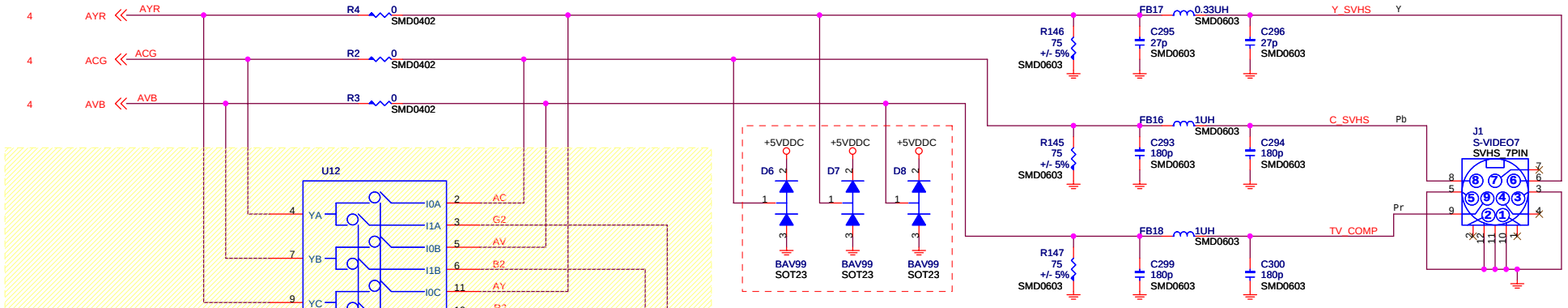
Date: Wednesday, April 19, 2006 | Sheet 9 of 14



NOTES:

1. "DNP" BY A COMPONENT MEANS "DO NOT POPULATE COMPONENT".

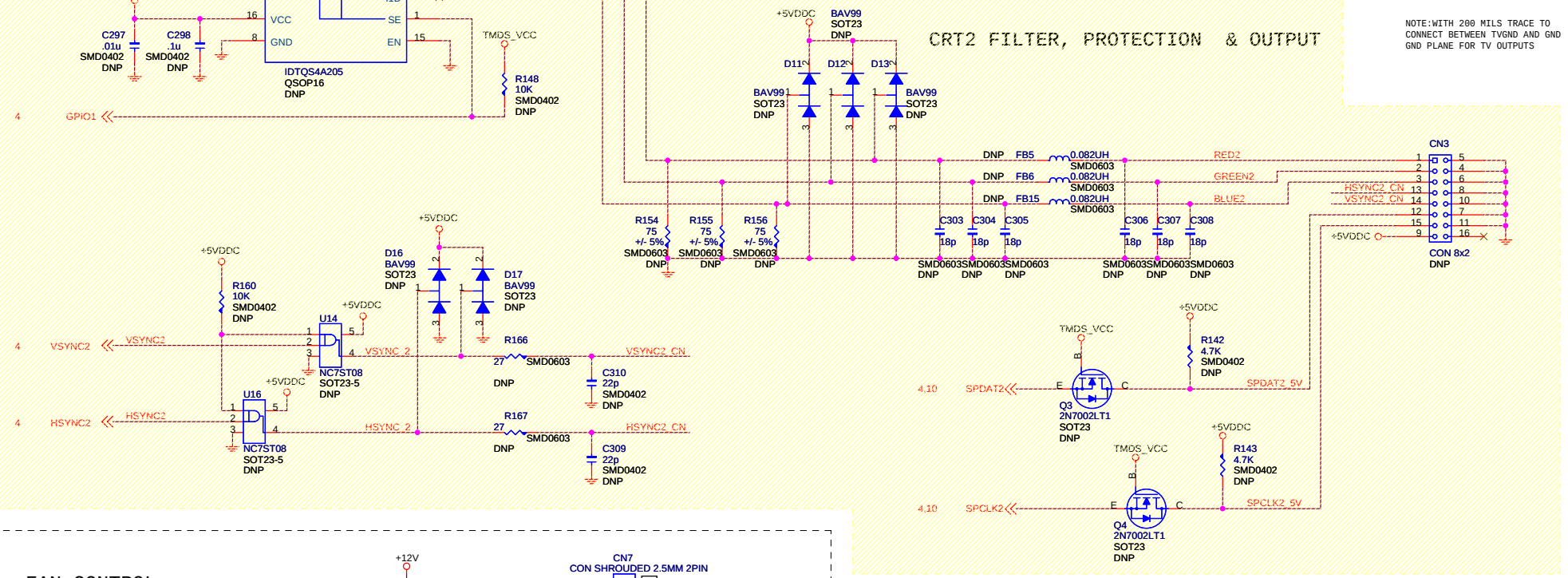
TV FILTER, PROTECTION & OUTPUT



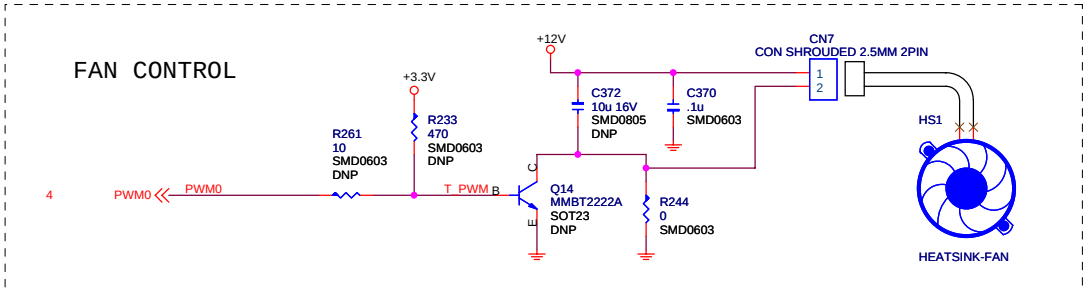
OPTIONAL COMPONENTS FOR CRT2 OUTPUT

NOTE:WITH 200 MILS TRACE TO CONNECT BETWEEN TVGND AND GND GND PLANE FOR TV OUTPUTS

CRT2 FILTER, PROTECTION & OUTPUT



FAN CONTROL



NOTES:

1. "DNP" BY A COMPONENT MEANS "DO NOT POPULATE COMPONENT".

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FREMONT CA 94539

Title: **TV / CRT2 / HDTV PORT & FAN CONTROL**

Size	Document Number	Rev
B	VT6330 Chrome20 Low Profile	1B

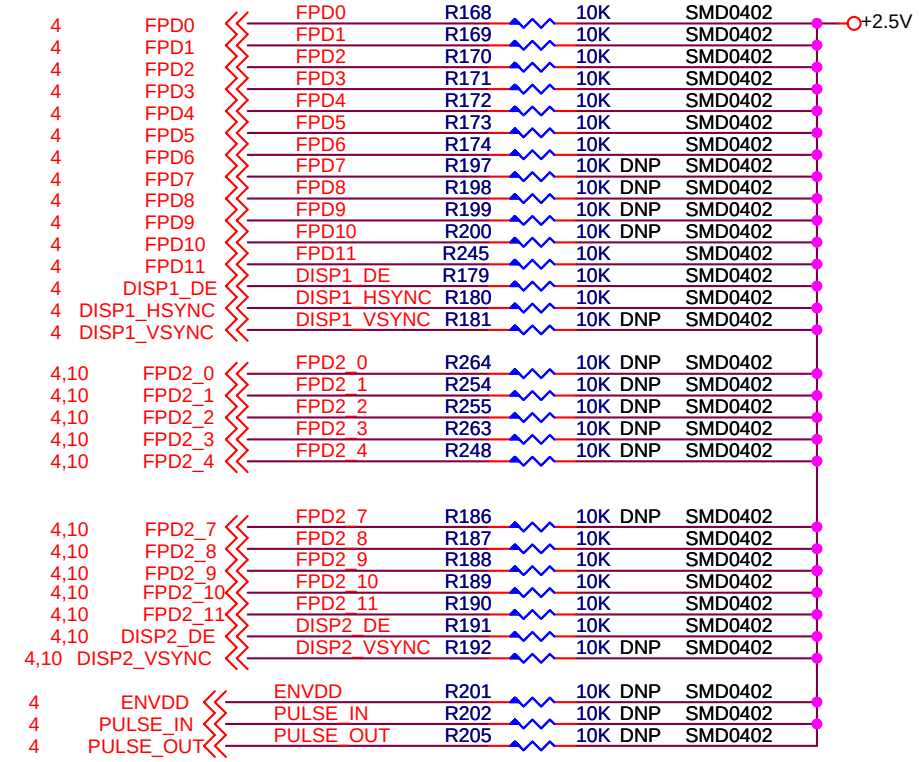
Date: Wednesday, April 19, 2006 Sheet 12 of 14

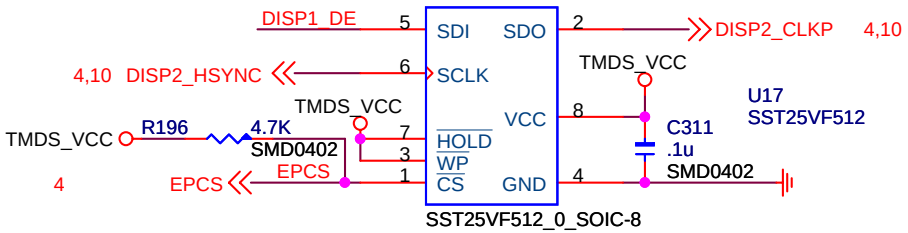
Strapping pins

REGISTER	SIGNAL	FUNCTION	VALUE	STUFF	RESISTOR
		PCIE LO NOT SUPPORTED	"0"	YES	
CR36_0	FPD0	PCIE LO SUPPORTED (DEFAULT)	"1"		R168
		PCIE L1 NOT SUPPORT	"0"	YES	
CR36_1	FPD1	PCIE L1 SUPPORTED (DEFAULT)	"1"		R169
		PCIE SCRAMBLE (DEFAULT)	"0"	YES	
CR36_2	FPD2	PCIE SCRAMBLE DISABLE	"1"		R170
		PCIE MSI_EN DISABLE (DEFAULT)	"0"	YES	
CR36_3	FPD3	PCIE MSI_EN ENABLE	"1"		R171
		PCIE NOT COMMON CLOCK	"0"	YES	
CR36_4	FPD4	PCIE COMMON CLOCK (DEFAULT)	"1"		R172
		USE PCIE INTERNAL PCLK (DEFAULT)	"0"	YES	
CR36_5	FPD5	USE PCIE EXTERNAL PCLK	"1"		R173
		PCIE 32-BIT ADDRESS MODE	"0"	YES	
CR36_6	FPD6	PCIE 64-BIT ADDRESS MODE	"1"		R174
		256K byte ROM size	"0"		
CR36_7	FPD7	64K byte ROM size	"1"	NO	R197
CR37_0	FPD8	ROM TYPE BIT-3..0] CR37[3..0] 000 SST SST39VF512 (PARALLEL 512kBIT) 001 LPC ROM, SST49LF080A 100 ATMEL 25F1024 (SERIAL 1MBIT) 101 ST MICRO 25P10 (SERIAL 1MBIT) 110 ST MICRO 25P05 (SERIAL 512kBIT) 111 SST SST25VF512 (SERIAL 512kBIT) OTHERS RESERVED	"0"		
			"1"	NO	R198
CR37_1	FPD9		"0"		
			"1"	NO	R199
CR37_2	FPD10		"0"		
			"1"	NO	R200
CR37_3	FPD11	ROM CLK is PCLK/32	"0"	YES	
		ROM CLK is PCLK/16	"1"		R245
		X16 PCI EXPRESS LINK WIDTH (DEFAULT)	"0"	YES	
CR37_4	DISP1_DE	X8 PCI EXPRESS LINK WIDTH	"1"		R179
CR37_5	DISP1_HSYNC	MEMORY SPEED BITS[2..0] CR68[3]CR37[6..5] 000 RESERVED 100 RESERVED 001 RESERVED 101 400MHz 010 300MHz 110 500MHz 011 350MHz 111 RESERVED	"0"	YES	
			"1"		R180
CR37_6	DISP1_VSYNC		"0"		
			"1"	NO	R181
CR68_3	FPD2_4		"0"		
			"1"	NO	R248
		HYNIX	"0"		
CR6F_7	ENVDD	SAMSUNG	"1"	NO	R201
		USE EXTERNAL MCLK/MCLK90 ON EXTMCLK/SPDAT2	"0"		
CR37_7	FPD2_0	USE INTERNAL MCLK/MCLK90 (DEFAULT)	"1"	NO	R264
		USE EXTERNAL ECLK ON EXTECLK	"0"		
CR68_0	FPD2_1	USE INTERNAL ECLK (DEFAULT)	"1"	NO	R254
		USE EXTERNAL DCLK1 ON XIN	"0"		
CR68_1	FPD2_2	USE INTERNAL DCLK1 (DEFAULT)	"1"	NO	R255
		USE EXTERNAL DCLK2 ON SPDAT4	"0"		
CR68_2	FPD2_3	USE INTERNAL DCLK2 (DEFAULT)	"1"	NO	R263
		CRYSTAL CONNECTED TO XIN, XOUT (DEFAULT)	"0"	YES	
CR68_7	FPD2_8	OSCILLATOR CONNECTED TO XIN	"1"		R187
		1 RANK POPULATED	"0"		
CR68_6	FPD2_7	2 RANKS	"1"	NO	R186
CR6F_0	FPD2_9	POPULATED 000 DDR2 16Mx16 100 DDR1 16Mx16 001 DDR3 8Mx32 101 DDR1 8Mx32 010 DDR2 32Mx16 110 DDR1 8Mx16 011 DDR3 16Mx32 111 DDR1 4Mx32	"0"	YES	
			"1"		R188
CR6F_1	FPD2_10		"0"	YES	R189
			"1"		
CR6F_2	FPD2_11		"0"	YES	
			"1"		R190
CR6F_3	DISP2_DE	00 0 FB 01 32-BIT MEMORY BUS WIDTH 10 128-BIT MEMORY BUS WIDTH 11 64-BIT MEMORY BUS	"0"	YES	
			"1"		R191
CR6F_5	DISP2_VSYNC	WIDTH(DEFAULT)	"0"		
			"1"	NO	R192
		FB MEMORY SIZE = 256M (DEFAULT)	"0"	NO	
CRCF1_6	PULSE_IN	FB MEMORY SIZE = 512M	"1"		R202
		BIGENDIAN DISABLE (DEFAULT)	"0"	NO	
CRCF1_7	PULSE_OUT	BIGENDIAN ENABLE	"1"		R205

NOTES:

1. "DNP" BY A COMPONENT MEANS "DO NOT POPULATE COMPONENT".





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1045 MISSION COURT
FREMONT CA 94539

Title

VGA BIOS EEPROM & Config Setting

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A	VT6330 Chrome20 Low Profile	1B

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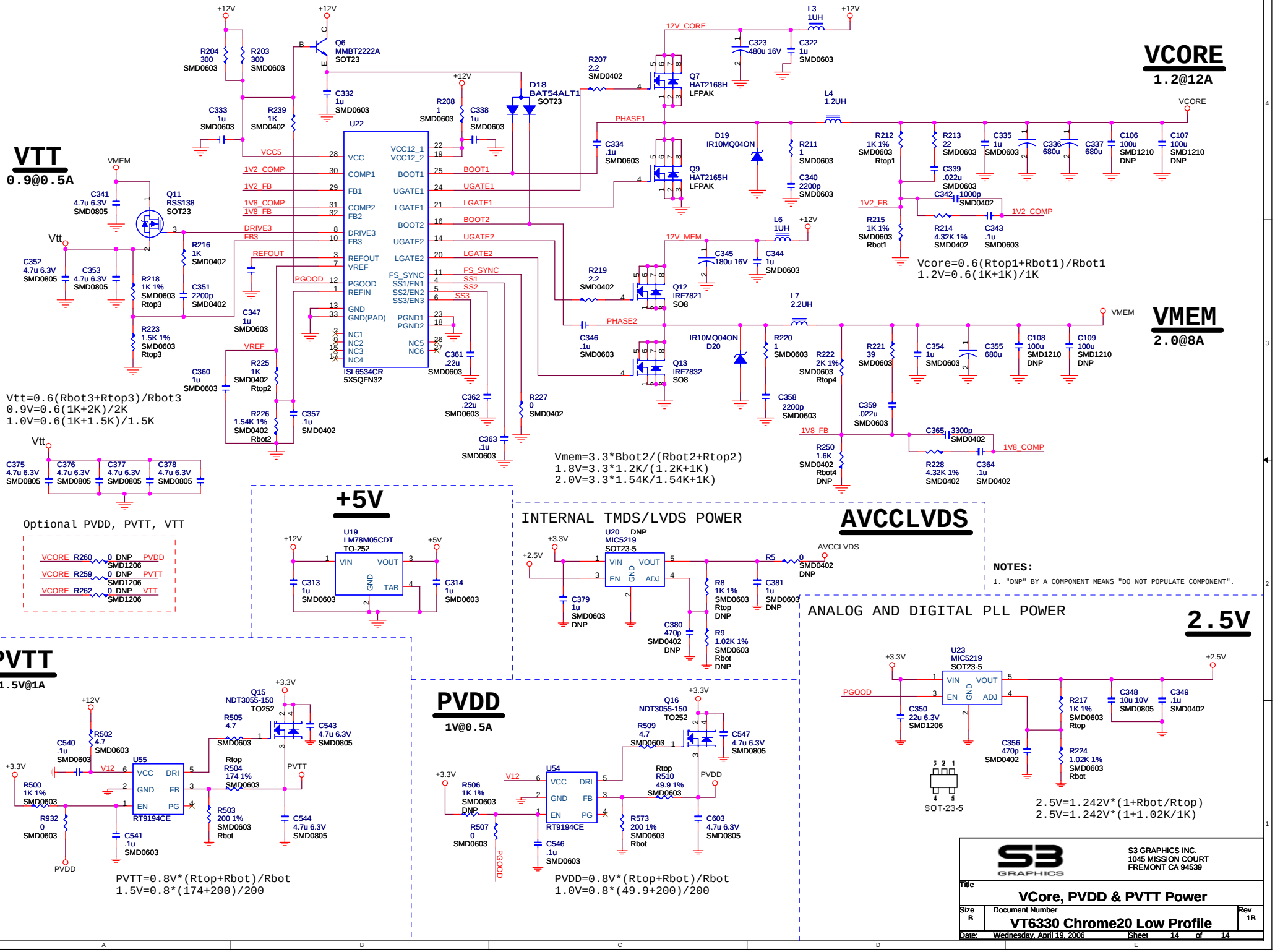
VCORE
1.2@12A
VMEM
2.0@8A
VTT
0.9@0.5A
+5V
AVCCLVDS
2.5V
PVTT
1.5V@1A
PVDD
1V@0.5A
INTERNAL TMDS/LVDS POWER
ANALOG AND DIGITAL PLL POWER
U22
ISL6534CR
5X5QFN32
Vcore=0.6(Rtop1+Rbot1)/Rbot1
1.2V=0.6(1K+1K)/1K
Vtt=0.6(Rbot3+Rtop3)/Rbot3
0.9V=0.6(1K+2K)/2K
1.0V=0.6(1K+1.5K)/1.5K
Vmem=3.3*Bbot2/(Rbot2+Rtop2)
1.8V=3.3*1.2K/(1.2K+1K)
2.0V=3.3*1.54K/1.54K+1K)
Optional PVDD, PVTT, VTT
PVTT=0.8V*(Rtop+Rbot)/Rbot
1.5V=0.8*(174+200)/200
PVDD=0.8V*(Rtop+Rbot)/Rbot
1.0V=0.8*(49.9+200)/200
2.5V=1.242V*(1+Rbot/Rtop)
2.5V=1.242V*(1+1.02K/1K)
NOTES:
1. "DNP" BY A COMPONENT MEANS "DO NOT POPULATE COMPONENT".
S3 GRAPHICS INC.
1045 MISSION COURT
FREMONT CA 94539
Title
VCore, PVDD & PVTT Power
Size B
Document Number
VT6330 Chrome20 Low Profile
Rev 1B
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