電子類元件 零件承認書文件 CHECK LIST

零件廠商：VISHAY(代理商 Weikeng) 品名規格：POWERSTAGE SiC632ACD-T1-GE3 VIS

技嘉料號：10IFD-500632-01R

項次	文件項目
Data Sheet 檢核項目	
1	DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2**
8	零件樣品 20PCS(Chipset 等高單價，至少 1PCS)
9	**電子零件承認基本調查表。註 3**
10	以上資料電子檔為 PDF 檔，且是同 1 個 File
GSCM 綠色產品管理系統-物料管制文件檢核清單	
物料管制文件 1	GSCM 綠色產品管理系統：零件照片
物料管制文件 2	GSCM 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4**
物料管制文件 3	GSCM 綠色產品管理系統：Data Sheet
GSCM 綠色產品管理系統-MCD 表格	
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
其他文件 (僅適用電阻、電容類之系列元件)	
附件 1	危害物質測試報告 Test Report of Hazardous Substances。**註 5**
附件 2	元件調查表 Component Composition Table

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等

※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)

2.1. 基本需符合 JEDEC 規範

2.2. Ambient Temp. (Reflow Temp endurace): >225℃, 70 sec. 零件塑膠材質需 PA9T(含)等級以上

2.3. PASTE IN HOLE 零件塑膠材質需 PA9T(含)等級以上

※ **3. 電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G*,11T***

非 IC 類：10C*,11C*,10L*,11L*,10X*,11X*,10R*,11B*

※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”

※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

電子零件承認基本調查表

一、原物料規格/來源

項次	部位名稱/規格	材　質	原物料來源產地
1	Bonding wire	Metal	Korea
2	Copper Clip	Metal	Korea
3	Die	Wafer	Taiwan
5	Die attach	ADHESIVES	USA
6	External plating	Metal materials plating layer	Singapore
7	Lead frame	Metal	Japan
8	Mold Compound	Epoxy resin	Malaysia
9	Solder paste	ADHESIVES	USA

二、晶圓廠(非 IC 類免填)

項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	Vanguard	台灣	8”	>80%	Outsource

三、封裝廠(IC 類)；成品之生產製造工廠(非 IC 類)

項次	工廠名稱	生產產地	投產比率(%)	自有/外包
1	Vishay Siliconix TW	TW	>80%	Outsource

四、產能

總產能(月/PCS)	可供技嘉產能(月/PCS)
10M/M	5/M

※ 1. IC 類之晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 2. 非 IC 類零件之成品生產製造工廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 3. 以上資訊欄位若有不足，可自行增加行數

威健實業股份有限公司

樣 品 承 認 書

日　　期　：　07. 1. 2018

廠　　牌　：　VISHAY

料　　號　：　10IFD-500632-01R

廠　　商　：　威健實業股份有限公司

地　　址　：　台北市內湖路一段308號11樓 T:(02)2659 0202 F:(02)2658 8338

業務代表　：　徐欣瑜

客戶名稱　：　技嘉科技股份有限公司

廠商料號　：　SIC632ACD-T1-GE3

結　　論　：

- ☐ 初審認可,進行測試
- ☐ 廠商認可依樣交貨
- ☐ 依備註條改後,直接認可
- ☐ 依備註條改後,重新送樣
- ☐ 不予承認,列入禁用
- ☐ 其他:

備　　註：

經　　理	主　　管	經　　辦

50 A VRPower® Integrated Power Stage

DESCRIPTION

The SiC632 and SiC632A are integrated power stage solutions optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's proprietary 5 mm x 5 mm MLP package, SiC632 and SiC632A enables voltage regulator designs to deliver up to 50 A continuous current per phase.

The internal power MOSFETs utilizes Vishay's state-of-the-art Gen IV TrenchFET technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC632 and SiC632A incorporate an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, a thermal warning (THWn) that alerts the system of excessive junction temperature, and zero current detection to improve light load efficiency. The drivers are also compatible with a wide range of PWM controllers and supports tri-state PWM, 3.3 V (SiC632A) / 5 V (SiC632) PWM logic.

FEATURES

RoHS COMPLIANT HALOGEN FREE

- Thermally enhanced PowerPAK® MLP55-31L package
- Vishay's Gen IV MOSFET technology and a low side MOSFET with integrated Schottky diode
- Delivers up to 50 A continuous current
- High efficiency performance
- High frequency operation up to 1.5 MHz
- Power MOSFETs optimized for 19 V input stage
- 3.3 V (SiC632A) / 5 V (SiC632) PWM logic with tri-state and hold-off
- Zero current detect control for light load efficiency improvement
- Low PWM propagation delay (< 20 ns)
- Faster disable
- Thermal monitor flag
- Under voltage lockout for V_{CIN}
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Multi-phase VRDs for computing, graphics card and memory
- Intel IMVP-8 VRPower delivery
  - V_{CORE}, $V_{GRAPHICS}$, $V_{SYSTEM\ AGENT}$ Skylake, Kabylake platforms
  - V_{CCGI} for Apollo Lake platforms
- Up to 24 V rail input DC/DC VR modules

TYPICAL APPLICATION DIAGRAM

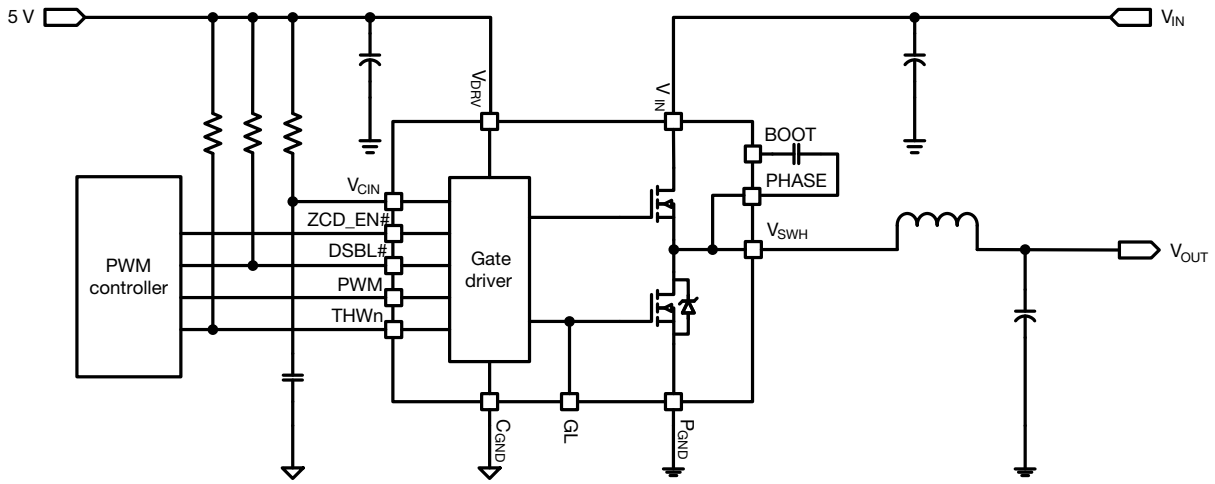


Fig. 1 - SiC632 and SiC632A Typical Application Diagram

PINOUT CONFIGURATION

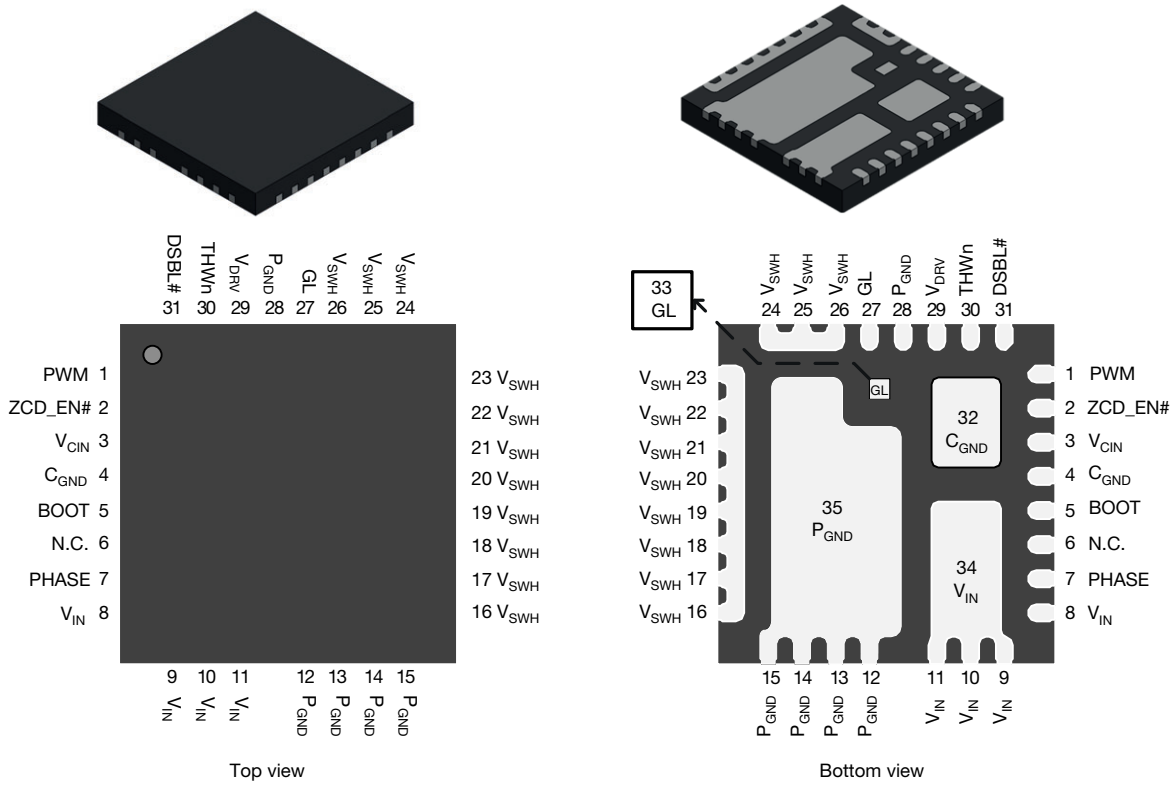
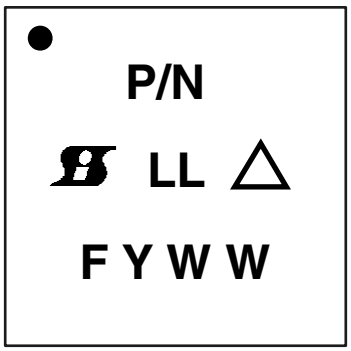


Fig. 2 - SiC632 and SiC632A Pin Configuration

PIN CONFIGURATION		
PIN NUMBER	**NAME**	**FUNCTION**
1	PWM	PWM input logic
2	ZCD_EN#	ZCD control. Active low
3	V_{CIN}	Supply voltage for internal logic circuitry
4, 32	C_{GND}	Signal ground
5	BOOT	High side driver bootstrap voltage
6	N.C.	Not connected internally, can be left floating or connected to ground
7	PHASE	Return path of high side gate driver
8 to 11, 34	V_{IN}	Power stage input voltage. Drain of high side MOSFET
12 to 15, 28, 35	P_{GND}	Power ground
16 to 26	V_{SWH}	Phase node of the power stage
27, 33	GL	Low side MOSFET gate signal
29	V_{DRV}	Supply voltage for internal gate driver
30	THWn	Thermal warning open drain output
31	DSBL#	Disable pin. Active low

ORDERING INFORMATION			
PART NUMBER	**PACKAGE**	**MARKING CODE**	**OPTION**
SiC632CD-T1-GE3	PowerPAK MLP55-31L	SiC632	5 V PWM optimized
SiC632ACD-T1-GE3	PowerPAK MLP55-31L	SiC632A	3.3 V PWM optimized
SiC632DB / SiC632ADB	Reference board		

PART MARKING INFORMATION



●	=	Pin 1 Indicator
P/N	=	Part Number Code
	=	Siliconix Logo
△	=	ESD Symbol
F	=	Assembly Factory Code
Y	=	Year Code
WW	=	Week Code
LL	=	Lot Code

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL PARAMETER	CONDITIONS	LIMIT	UNIT
Input voltage	V_{IN}	-0.3 to +28	V
Control logic supply voltage	V_{CIN}	-0.3 to +7	
Drive supply voltage	V_{DRV}	-0.3 to +7	
Switch node (DC voltage)	V_{SWH}	-0.3 to +28	
Switch node (AC voltage) (1)		-7 to +33	
BOOT voltage (DC voltage)	V_{BOOT}	35	
BOOT voltage (AC voltage) (2)		40	
BOOT to PHASE (DC voltage)	$V_{BOOT-PHASE}$	-0.3 to +7	
BOOT to PHASE (AC voltage) (3)		-0.3 to +8	
All logic inputs and outputs (PWM, DSBL#, and THWn)		-0.3 to V_{CIN} + 0.3	
Max. operating junction temperature	T_J	150	°C
Ambient temperature	T_A	-40 to +125	
Storage temperature	T_{stg}	-65 to +150	
Electrostatic discharge protection	Human body model, JESD22-A114	3000	V
	Charged device model, JESD22-C101	1000	

Notes

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

(1) The specification values indicated “AC” is V_{SWH} to P_{GND} -8 V (< 20 ns, 10 µJ), min. and 33 V (< 50 ns), max.
(2) The specification value indicates “AC voltage” is V_{BOOT} to P_{GND}, 40 V (< 50 ns) max.
(3) The specification value indicates “AC voltage” is V_{BOOT} to V_{PHASE}, 8 V (< 20 ns) max.

RECOMMENDED OPERATING RANGE

ELECTRICAL PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
Input voltage (V_{IN})	4.5	-	24	V
Drive supply voltage (V_{DRV})	4.5	5	5.5	
Control logic supply voltage (V_{CIN})	4.5	5	5.5	
BOOT to PHASE ($V_{BOOT-PHASE}$, DC voltage)	4	4.5	5.5	
Thermal resistance from junction to ambient	-	10.6	-	°C/W
Thermal resistance from junction to case	-	1.6	-	

ELECTRICAL SPECIFICATIONS

(DSBL# = ZCD_EN# = 5 V, V_{IN} = 12 V, V_{DRV} and V_{CIN} = 5 V, T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
POWER SUPPLY						
Control logic supply current	I_{VCIN}	$V_{DSBL\#}$ = 0 V, no switching, V_{PWM} = FLOAT	-	10	-	µA
		$V_{DSBL\#}$ = 5 V, no switching, V_{PWM} = FLOAT	-	300	-	
		$V_{DSBL\#}$ = 5 V, f_S = 300 kHz, D = 0.1	-	525	-	
Drive supply current	I_{VDRV}	f_S = 300 kHz, D = 0.1	-	10	15	mA
		f_S = 1 MHz, D = 0.1	-	35	-	
		$V_{DSBL\#}$ = 0 V, no switching	-	15	-	µA
		$V_{DSBL\#}$ = 5 V, no switching	-	55	-	
BOOTSTRAP SUPPLY						
Bootstrap diode forward voltage	V_F	I_F = 2 mA			0.4	V
PWM CONTROL INPUT (SiC632)						
Rising threshold	$V_{TH\_PWM\_R}$		3.4	3.8	4.2	V
Falling threshold	$V_{TH\_PWM\_F}$		0.72	0.9	1.1	
Tri-state voltage	V_{TRI}	V_{PWM} = FLOAT	-	2.3	-	
Tri-state rising threshold	$V_{TRI\_TH\_R}$		0.9	1.15	1.38	
Tri-state falling threshold	$V_{TRI\_TH\_F}$		3	3.3	3.6	
Tri-state rising threshold hysteresis	$V_{HYS\_TRI\_R}$		-	225	-	mV
Tri-state falling threshold hysteresis	$V_{HYS\_TRI\_F}$		-	325	-	
PWM input current	I_{PWM}	V_{PWM} = 5 V	-	-	350	µA
		V_{PWM} = 0 V	-	-	-350	
PWM CONTROL INPUT (SiC632A)						
Rising threshold	$V_{TH\_PWM\_R}$		2.2	2.45	2.7	V
Falling threshold	$V_{TH\_PWM\_F}$		0.72	0.9	1.1	
Tri-state Voltage	V_{TRI}	V_{PWM} = FLOAT	-	1.8	-	
Tri-state rising threshold	$V_{TRI\_TH\_R}$		0.9	1.15	1.38	
Tri-state falling threshold	$V_{TRI\_TH\_F}$		1.95	2.2	2.45	
Tri-state rising threshold hysteresis	$V_{HYS\_TRI\_R}$		-	250	-	mV
Tri-state falling threshold hysteresis	$V_{HYS\_TRI\_F}$		-	300	-	
PWM input current	I_{PWM}	V_{PWM} = 3.3 V	-	-	225	µA
		V_{PWM} = 0 V	-	-	-225	
TIMING SPECIFICATIONS						
Tri-state to GH/GL rising propagation delay	$t_{PD\_TRI\_R}$	No load, see fig. 4	-	30	-	ns
Tri-state hold-off time	t_{TSHO}		-	130	-	
GH - turn off propagation delay	$t_{PD\_OFF\_GH}$		-	15	-	
GH - turn on propagation delay (dead time rising)	$t_{PD\_ON\_GH}$		-	10	-	
GL - turn off propagation delay	$t_{PD\_OFF\_GL}$		-	13	-	
GL - turn on propagation delay (dead time falling)	$t_{PD\_ON\_GL}$		-	10	-	
DSBL# Lo to GH/GL falling propagation delay	$t_{PD\_DSBL\#\_F}$	Fig. 5	-	15	-	
PWM minimum on-Time	$t_{PWM\_ON\_MIN}$		30	-	-	

ELECTRICAL SPECIFICATIONS
(DSBL# = ZCD_EN# = 5 V, V_{IN} = 12 V, V_{DRV} and V_{CIN} = 5 V, T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
DSBL# ZCD_EN# INPUT						
DSBL# logic input voltage	$V_{IH\_DSBL\#}$	Input logic high	2	-	-	V
	$V_{IL\_DSBL\#}$	Input logic low	-	-	0.8	
ZCD_EN# logic input voltage	$V_{IH\_ZCD\_EN\#}$	Input logic high	2	-	-	
	$V_{IL\_ZCD\_EN\#}$	Input logic low	-	-	0.8	
PROTECTION						
Under voltage lockout	V_{UVLO}	V_{CIN} rising, on threshold	-	3.7	4.1	V
		V_{CIN} falling, off threshold	2.7	3.1	-	
Under voltage lockout hysteresis	V_{UVLO_HYST}		-	575	-	mV
THWn flag set (2)	T_{THWn_SET}		-	160	-	°C
THWn flag clear (2)	T_{THWn_CLEAR}		-	135	-	
THWn flag hysteresis (2)	T_{THWn_HYST}		-	25	-	
THWn output low	V_{OL_THWn}	I_{THWn} = 2 mA	-	0.02	-	V

Notes

(1) Typical limits are established by characterization and are not production tested

(2) Guaranteed by design

DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{PWM\_TH\_R}$ the low side is turned OFF and the high side is turned ON. When PWM input is driven below $V_{PWM\_TH\_F}$ the high side is turned OFF and the low side is turned ON. For tri-state logic, the PWM input operates as previously stated for driving the MOSFETs when PWM is logic high and logic low. However, there is a third state that is entered as the PWM output of tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC632 and SiC632A to pull the PWM input into the tri-state region (see definition of PWM logic and Tri-State, fig. 4). If the PWM input stays in this region for the Tri-state Hold-Off Period, tTSHO, both high side and low side MOSFETs are turned OFF. The function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC632A incorporates PWM voltage thresholds that are compatible with 3.3 V logic and the SiC632 thresholds are compatible with 5 V logic.

Disable (DSBL#)

In the low state, the DSBL# pin shuts down the driver IC and disables both high side and low side MOSFETs. In this state, standby current is minimized. If DSBL# is left unconnected, an internal pull-down resistor will pull the pin to C_{GND} and shut down the IC.

Diode Emulation Mode (ZCD_EN#)

When ZCD_EN# pin is driven below $V_{IL\_ZCD\_EN\#}$. diode emulation mode is enabled. If the PWM signal switches below $V_{TH\_PWM\_F}$ then the LS MOSFET is under control of the ZCD (zero crossing detect) comparator. If, after the internal blanking delay, the inductor current becomes less than or = 0 the low side is turned OFF. Light load efficiency is improved by avoiding discharge of output capacitors. If both high side and low side MOSFETs are required to be turned off, regardless of inductor current, the PWM input should be tri-stated.

Thermal Shutdown Warning (THWn)

The THWn pin is an open drain signal that flags the presence of excessive junction temperature. Connect with a maximum of 20 kΩ, to V_{CIN}. An internal temperature sensor detects the junction temperature. The temperature threshold is 160 °C. When this junction temperature is exceeded the THWn flag is set. When the junction temperature drops below 135 °C the device will clear the THWn signal. The SiC632 and SiC632A do not stop operation when the flag is set. The decision to shutdown must be made by an external thermal control function.

Voltage Input (V_{IN})

This is the power input to the drain of the high side power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The switch node, V_{SWH}, is the circuit power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter. The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20 kΩ resistor is connected between GH (the high side gate) and PHASE to provide a discharge path for the HS MOSFET in the event that V_{CIN} goes to zero while V_{IN} is still applied.

Ground Connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (signal ground). The layout of the printed circuit board should be such that the inductance separating C_{GND} and P_{GND} is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V

Control and Drive Supply Voltage Input (V_{DRV}, V_{CIN})

V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

Bootstrap Circuit (BOOT)

The internal bootstrap diode and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

Shoot-Through Protection and Adaptive Dead Time

The SiC632 and SiC632A have an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high side and low side MOSFETs are not turned ON at the same time. The adaptive dead time control operates as follows. The high side and low side gate voltages are monitored to prevent the MOSFET turning ON from tuning ON until the other MOSFET's gate voltage is sufficiently low (< 1 V). Built in delays also ensure that one power MOSFET is completely OFF, before the other can be turned ON. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high side and low side MOSFET gates low until the supply voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC632, SiC632A also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20 kΩ resistor is connected between GH (the high side gate) and PHASE to provide a discharge path for the HS MOSFET.

FUNCTIONAL BLOCK DIAGRAM

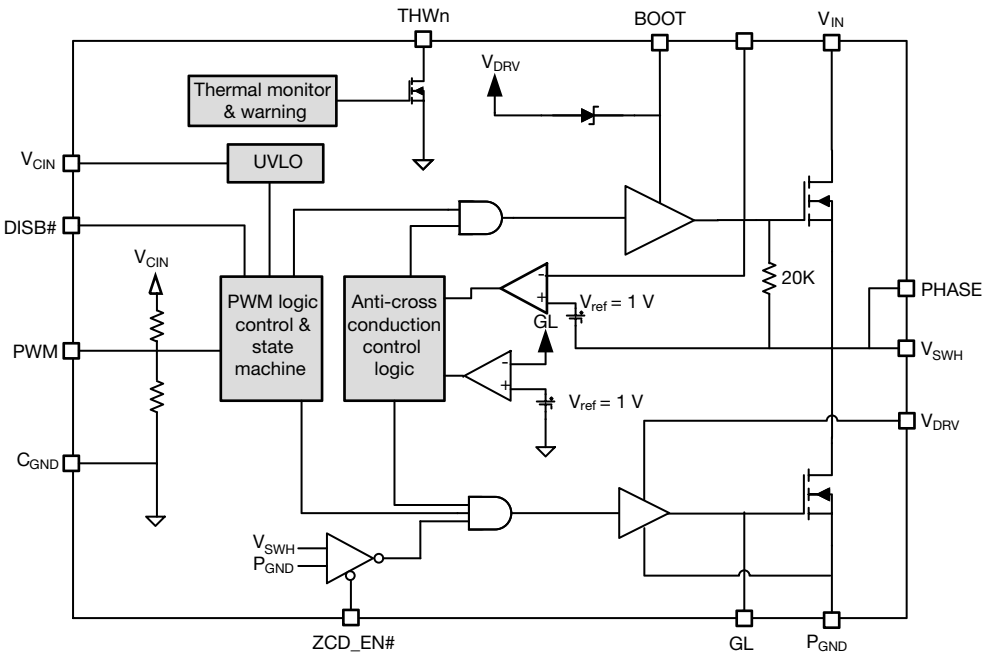


Fig. 3 - SiC632 and SiC632A Functional Block Diagram

DEVICE TRUTH TABLE				
DSBL#	**ZCD_EN#**	**PWM**	**GH**	**GL**
Open	X	X	L	L
L	X	X	L	L
H	L	L	L	H, I_L > 0 A L, I_L < 0 A
H	L	H	H	L
H	L	Tri-state	L	L
H	H	L	L	H
H	H	H	H	L
H	H	Tri-state	L	L

PWM TIMING DIAGRAM

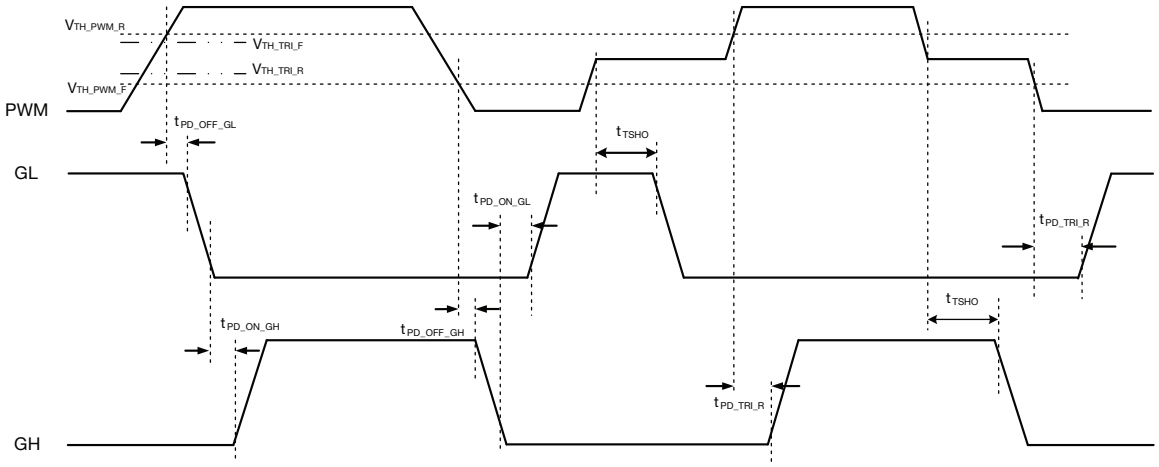


Fig. 4 - Definition of PWM Logic and Tri-state

DSBL# PROPAGATION DELAY

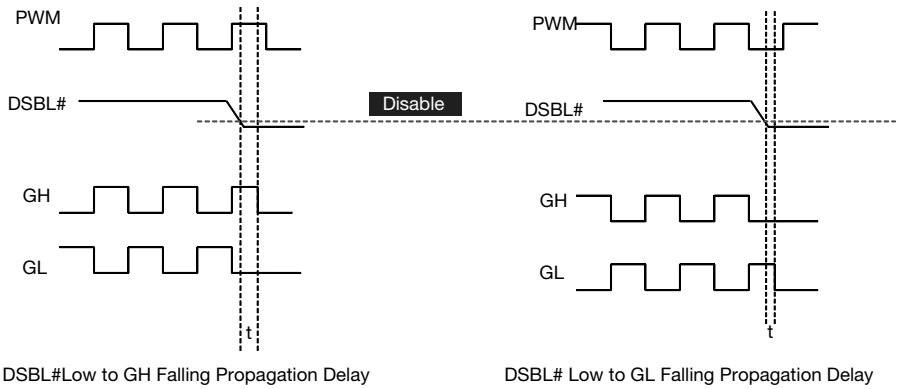


Fig. 5 - DSBL# Falling Propagation Delay

ELECTRICAL CHARACTERISTICS

Test condition: V_{IN} = 13 V, DSBL# = V_{DRV} = V_{CIN} = 5 V, ZCD_EN# = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH (DCR = 0.32 mΩ), T_A = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC632 and SiC632A losses only unless otherwise stated)

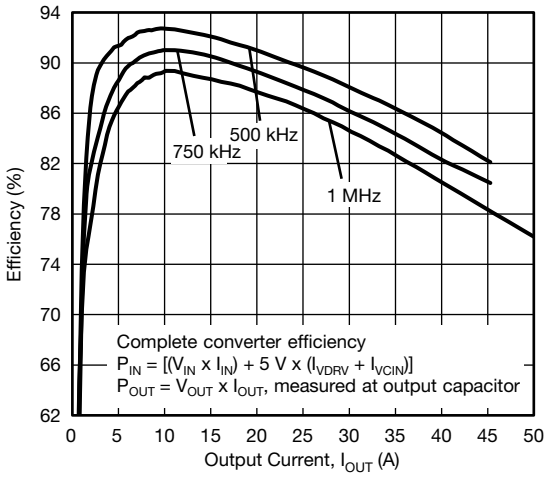


Fig. 6 - Efficiency vs. Output Current (V_{IN} = 12.6 V)

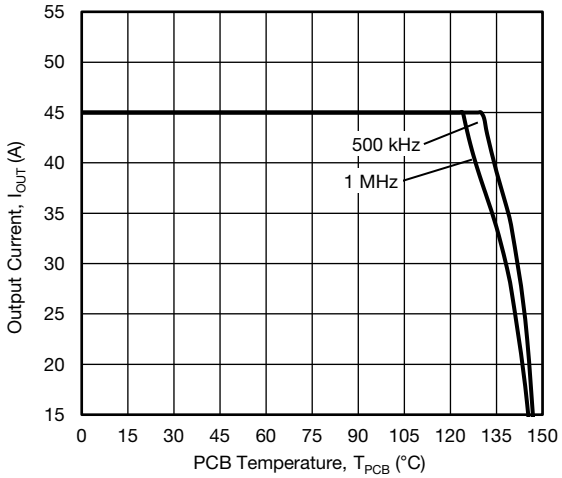


Fig. 9 - Safe Operating Area

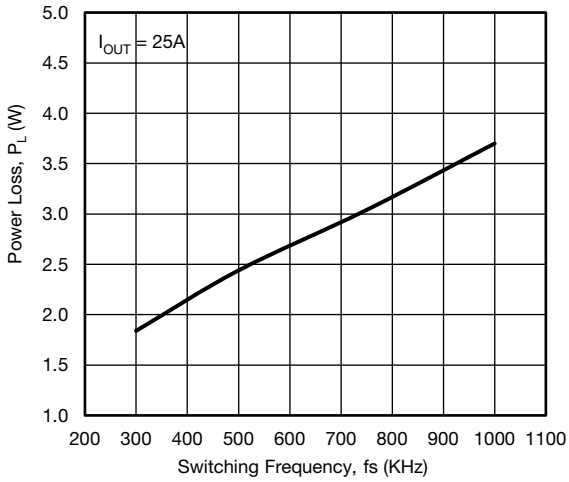


Fig. 7 - Power Loss vs. Switching Frequency (V_{IN} = 12.6 V)

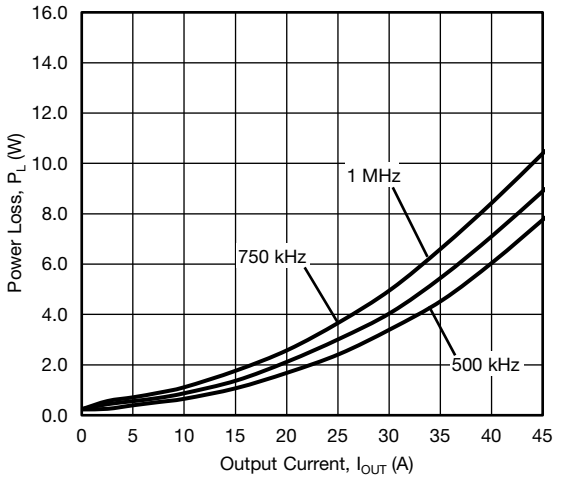


Fig. 10 - Power Loss vs. Output Current (V_{IN} = 12.6 V)

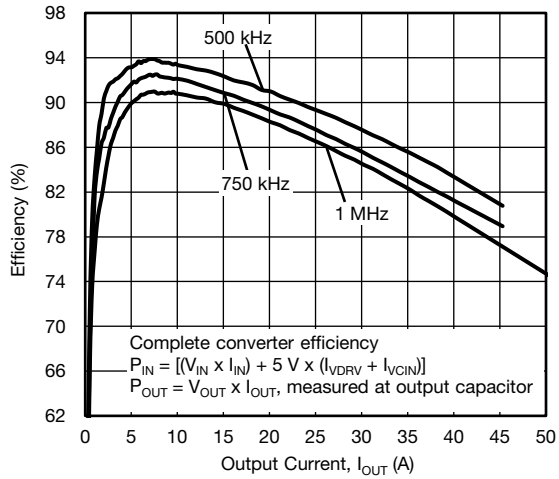


Fig. 8 - Efficiency vs. Output Current (V_{IN} = 9 V)

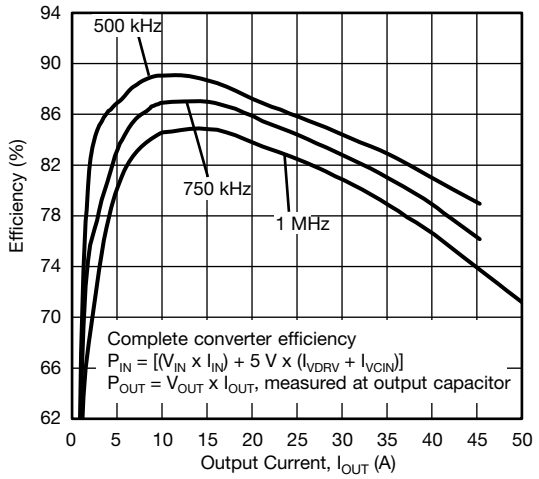


Fig. 11 - Efficiency vs. Output Current (V_{IN} = 19 V)

ELECTRICAL CHARACTERISTICS

Test condition: V_{IN} = 13 V, DSBL# = V_{DRV} = V_{CIN} = 5 V, ZCD_EN# = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH (DCR = 0.32 mΩ), T_A = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC632 and SiC632A losses only unless otherwise stated)

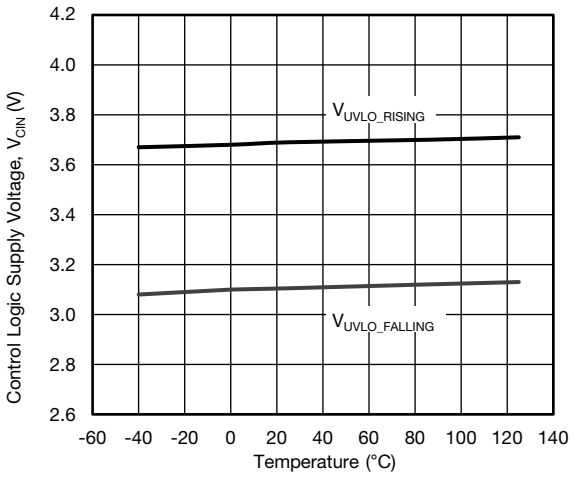


Fig. 12 - UVLO Threshold vs. Temperature

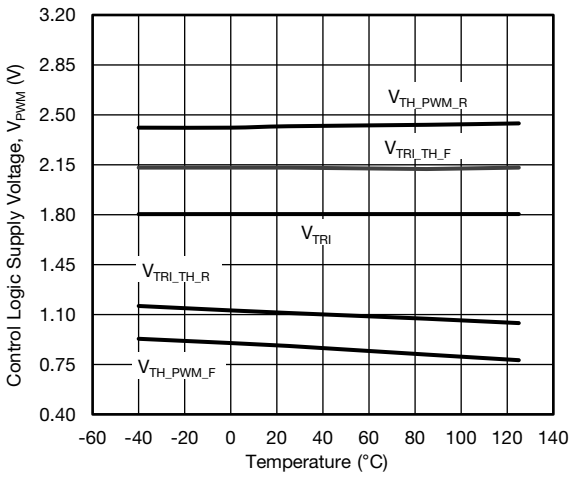


Fig. 13 - PWM Threshold vs. Temperature (SiC632A)

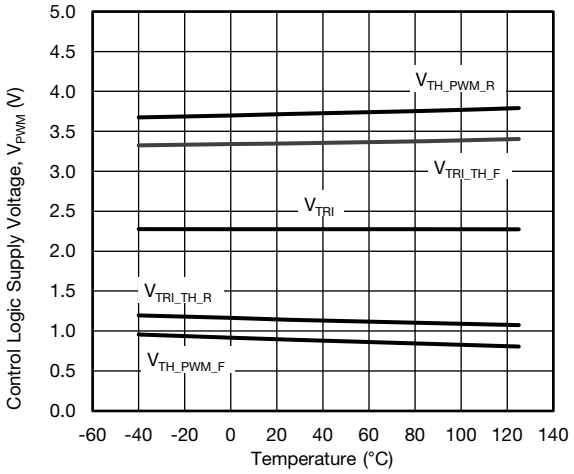


Fig. 14 - PWM Threshold vs. Temperature (SiC632)

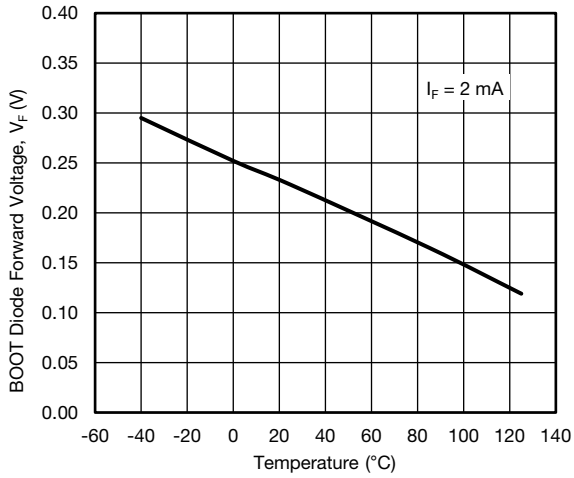


Fig. 15 - Boot Diode Forward Voltage vs. Temperature

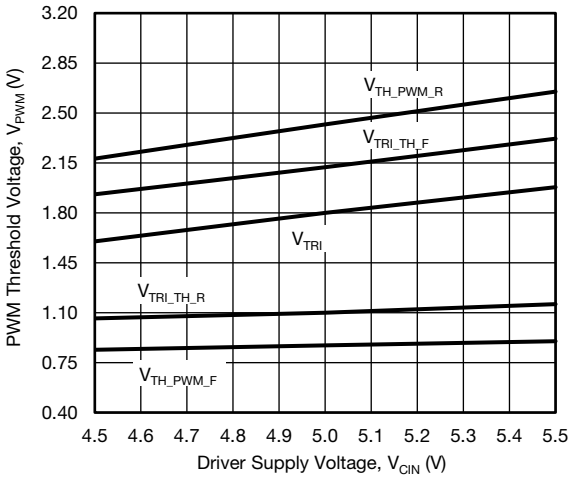


Fig. 16 - PWM Threshold vs. Driver Supply Voltage (SiC632A)

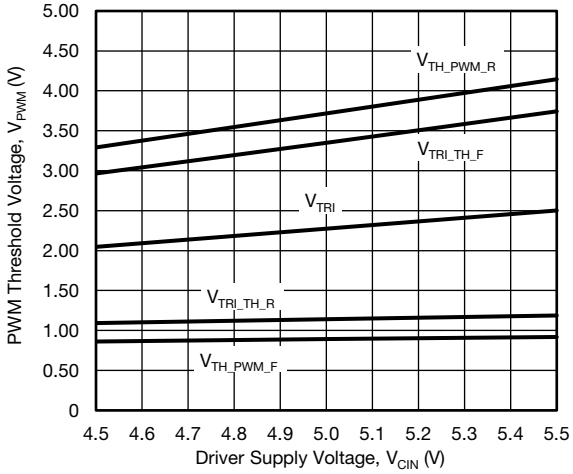


Fig. 17 - PWM Threshold vs. Driver Supply Voltage (SiC632)

ELECTRICAL CHARACTERISTICS

Test condition: V_{IN} = 13 V, DSBL# = V_{DRV} = V_{CIN} = 5 V, ZCD_EN# = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH (DCR = 0.32 mΩ), T_A = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC632 and SiC632A losses only unless otherwise stated)

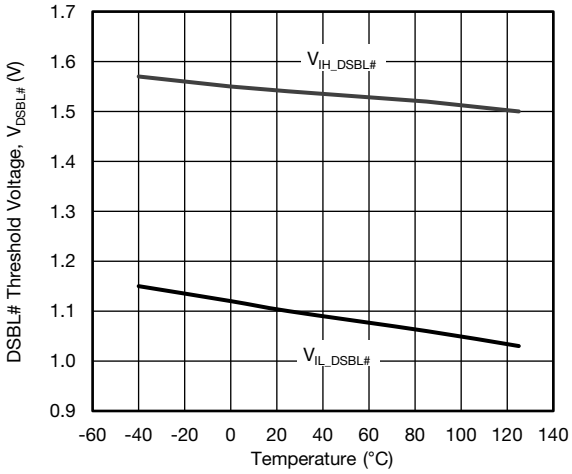


Fig. 18 - DSBL# Threshold vs. Temperature

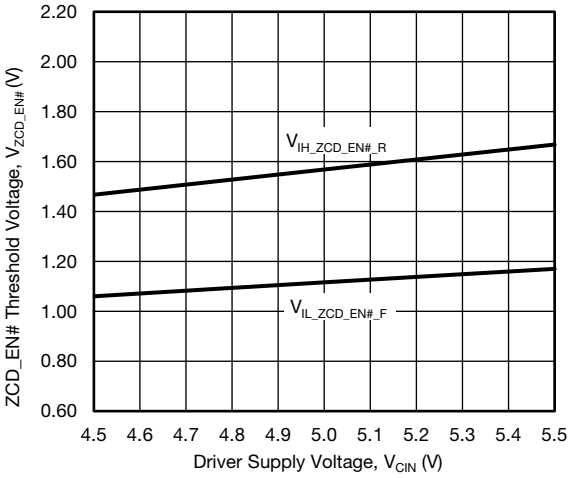


Fig. 21 - ZCD_EN# Threshold vs. Driver Supply Voltage

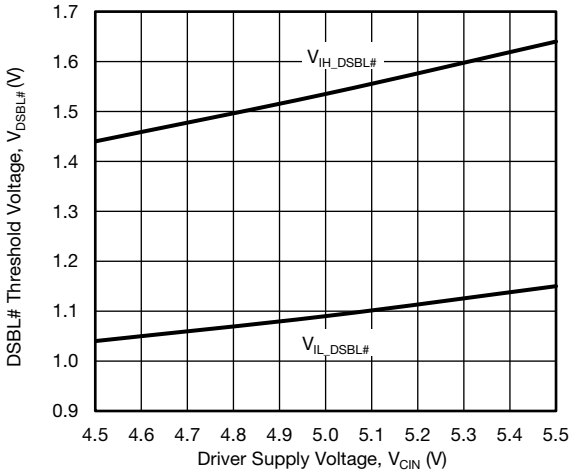


Fig. 19 - DSBL# vs. Driver Input Voltage

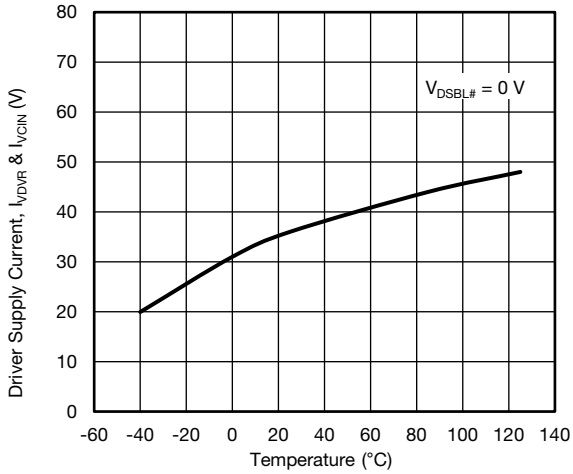


Fig. 22 - Driver Shutdown Current vs. Temperature

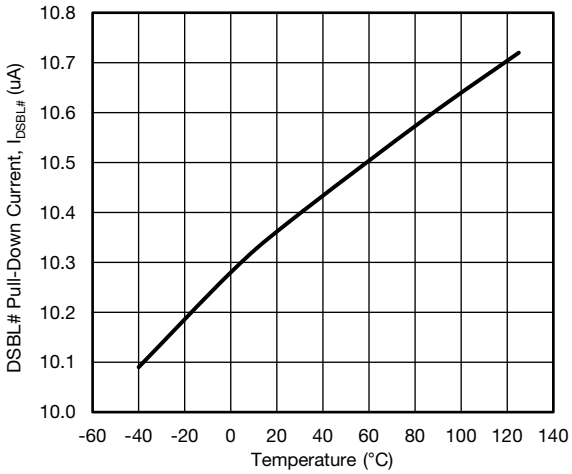


Fig. 20 - DSBL# Pull-Down Current vs. Temperature

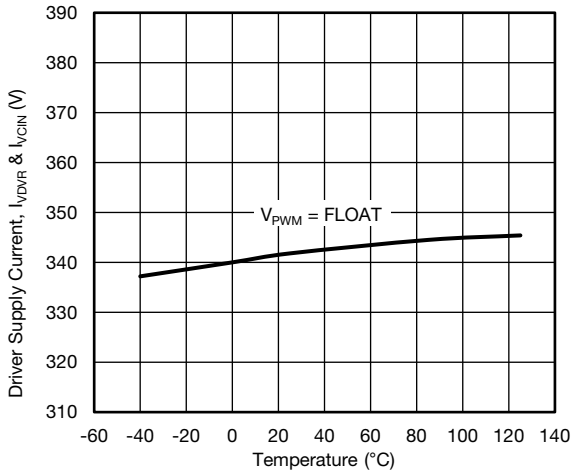
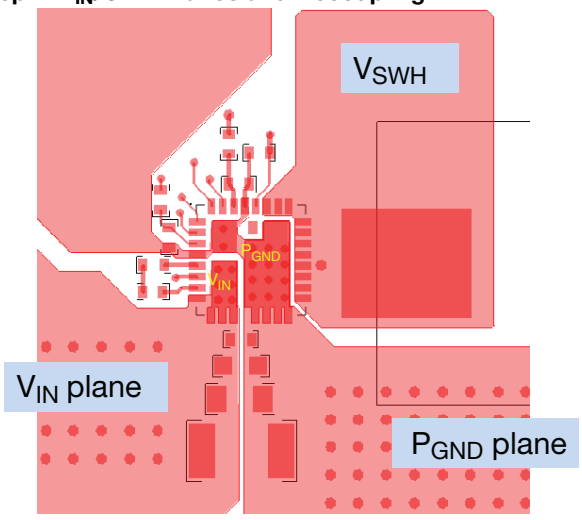


Fig. 23 - Driver Supply Current vs. Temperature

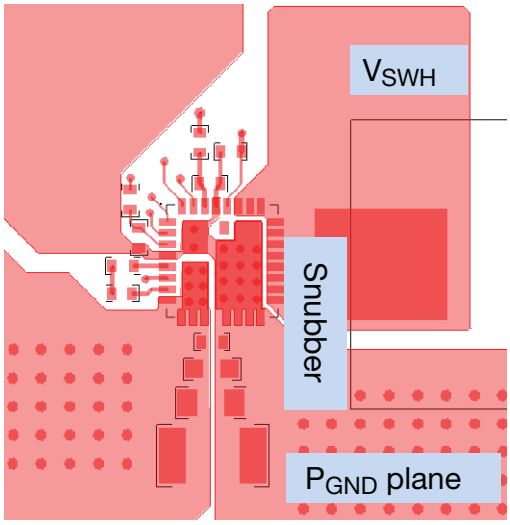
PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN}/GND Planes and Decoupling



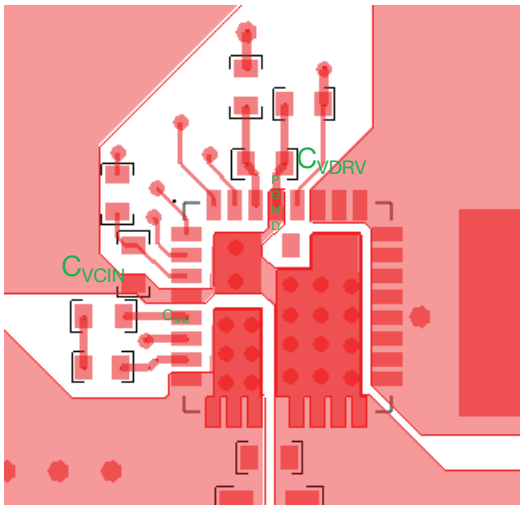
1. Layout V_{IN} and P_{GND} planes as shown above
2. Ceramic capacitors should be placed right between V_{IN} and P_{GND}, and very close to the device for best decoupling effect
3. Difference values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210, 0805, 0603 and 0402
4. Smaller capacitance value, closer to device V_{IN} pin(s) - better high frequency noise absorbing

Step 2: V_{SWH} Plane



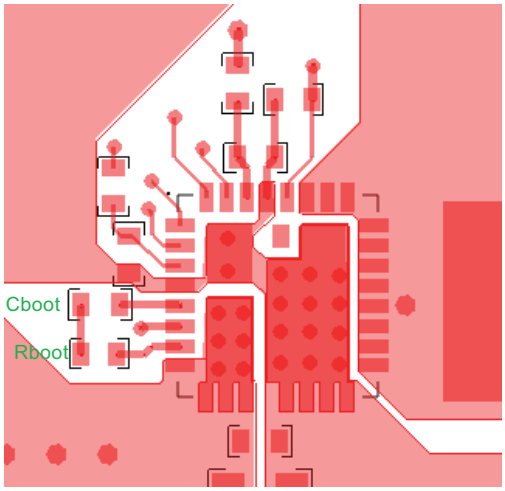
1. Connect output inductor to DrMOS with large plane to lower the resistance
2. If any snubber network is required, place the components as shown above and the network can be placed at bottom

Step 3: V_{CIN}/V_{DRV} Input Filter



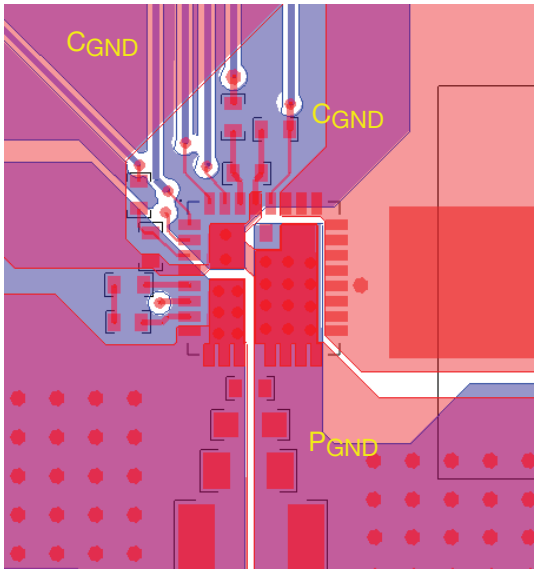
1. The V_{CIN}/V_{DRV} input filter ceramic cap should be placed very close to IC. It is recommended to connect two caps separately.
2. C_{VCIN} cap should be placed between pin 3 and pin 4 (C_{GND} of driver IC) to achieve best noise filtering.
3. C_{VDRV} cap should be placed between pin 28 (P_{GND} of driver IC) and pin 29 to provide maximum instantaneous driver current for low side MOSFET during switching cycle
4. For connecting C_{VCIN} analog ground, it is recommended to use large plane to reduce parasitic inductance.

Step 4: BOOT Resistor and Capacitor Placement



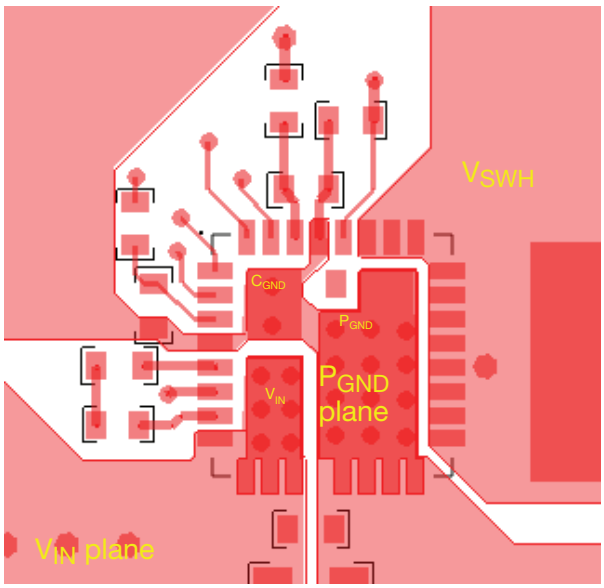
1. These components need to be placed very close to IC, right between PHASE (pin 7) and BOOT (pin 5).
2. To reduce parasitic inductance, chip size 0402 can be used.

Step 5: Signal Routing



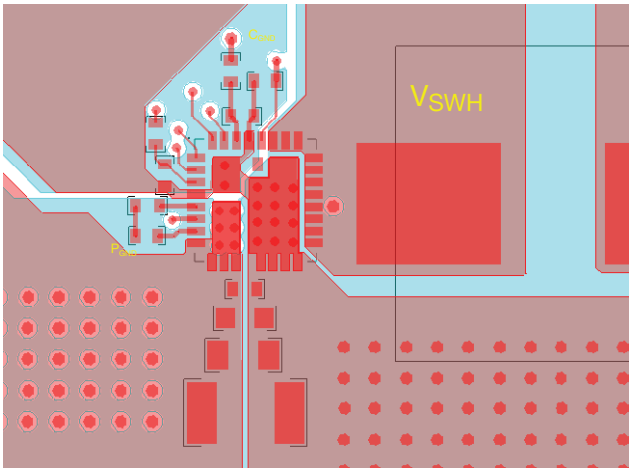
1. Route the PWM / ZCD_EN# / DSBL# / THWn signal traces out of the top left corner next DrMOS pin 1.
2. PWM signal is very important signal, both signal and return traces need to pay special attention of not letting this trace cross any power nodes on any layer.
3. It is best to “shield” traces form power switching nodes, e.g. V_{SWH}, to improve signal integrity.
4. GL (pin 27) has been connected with GL pad internally and does not need to connect externally.

Step 6: Adding Thermal Relief Vias



1. Thermal relief vias can be added on the V_{IN} and P_{GND} pads to utilize inner layers for high current and thermal dissipation.
2. To achieve better thermal performance, additional vias can be put on V_{IN} plane and P_{GND} plane.
3. V_{SWH} pad is a noise source and not recommended to put vias on this plane.
4. 8 mil drill for pads and 10 mils drill for plane can be the optional via size. Vias on pad may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline.

Step 7: Ground Connection



1. It is recommended to make single connection between C_{GND} and P_{GND} and this connection can be done on top layer.
2. It is recommended to make the whole inner 1 layer (next to top layer) ground plane and separate them into C_{GND} and P_{GND} plane.
3. These ground planes provide shielding between noise source on top layer and signal trace on bottom layer.

Multi-Phases VRPower PCB Layout

Following is an example for 6 phase layout. As can be seen, all the VRPower stages are lined in X-direction compactly with decoupling caps next to them. The inductors are placed as close as possible to the SiC632 and SiC632A to minimize the PCB copper loss. Vias are applied on all PADs (V_{IN}, P_{GND}, C_{GND}) of the SiC632 and SiC632A to ensure that both electrical and thermal performance are excellent. Large copper planes are used for all the high current loops, such as V_{IN}, V_{SWH}, V_{OUT} and P_{GND}. These copper planes are duplicated in other layers to minimize the inductance and resistance. All the control signals are routed from the SiC632 and SiC632A to a controller placed to the north of the power stage through inner layers to avoid the overlap of high current loops. This achieves a compact design with the output from the inductors feeding a load located to the south of the design as shown in the figure.

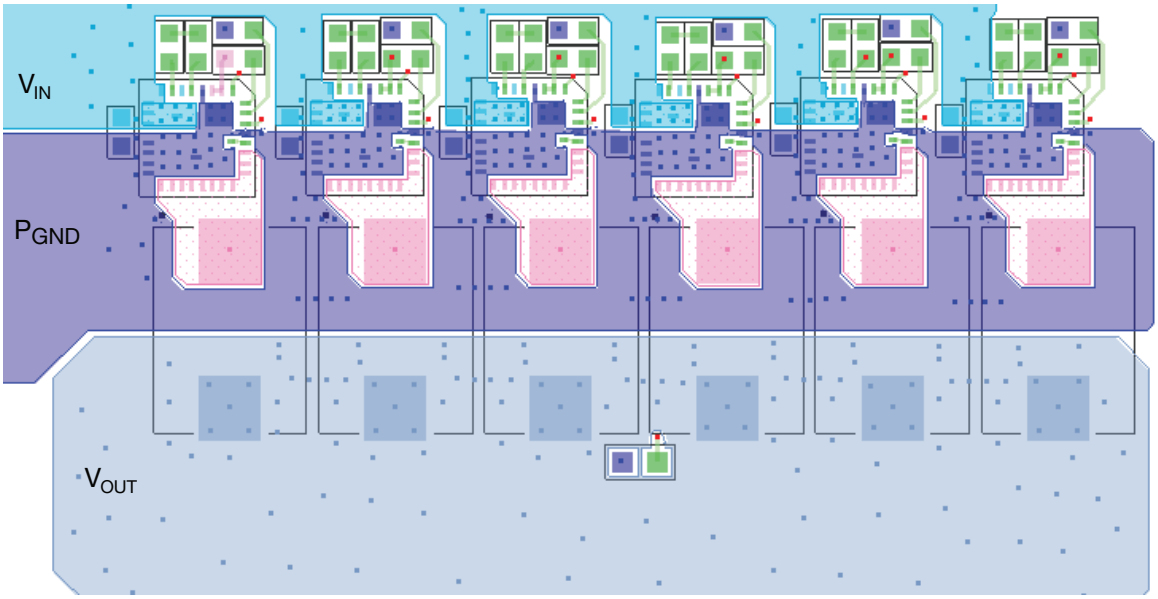


Fig. 24 - Multi - Phase VRPower Layout Top View

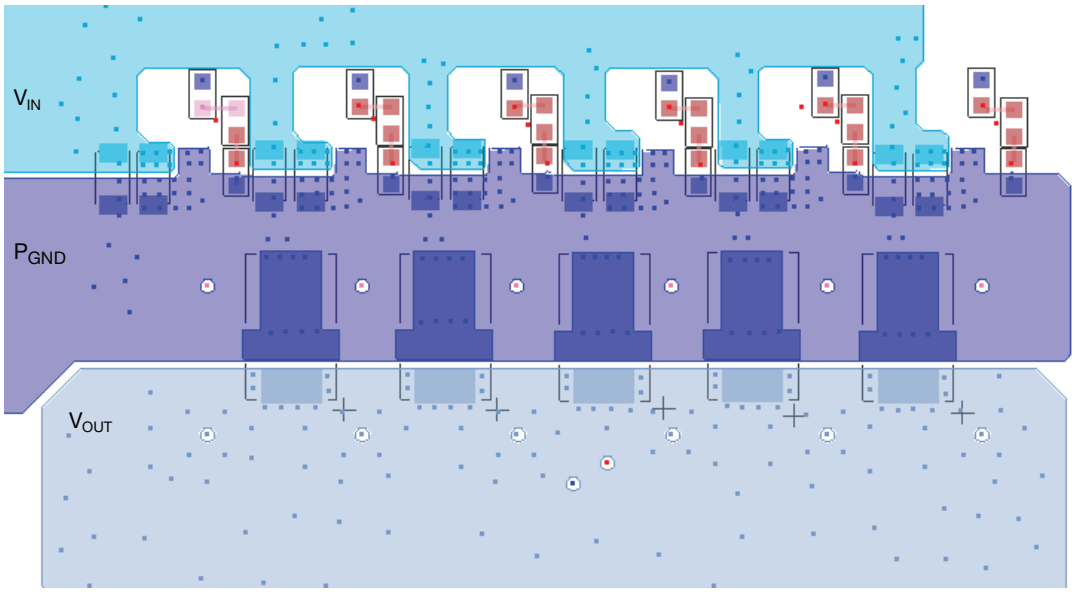
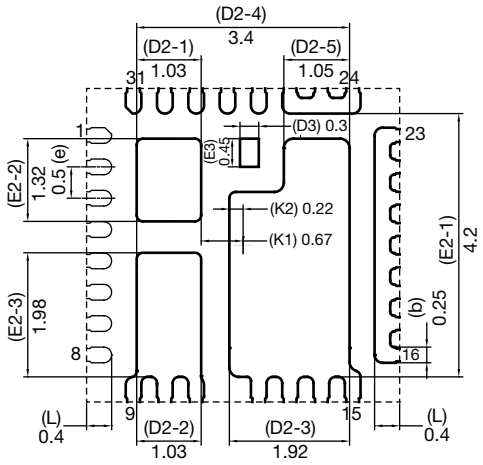


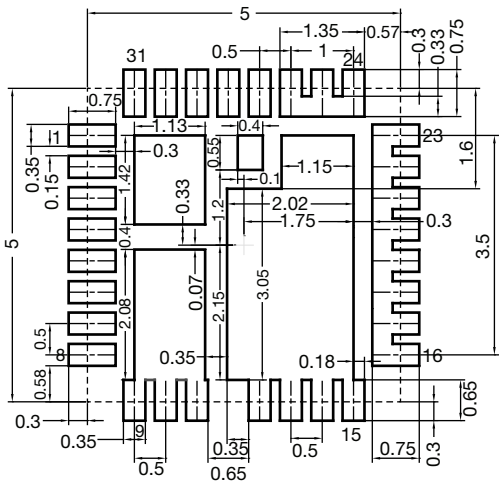
Fig. 25 - Multi - Phase VRPower Layout Bottom View

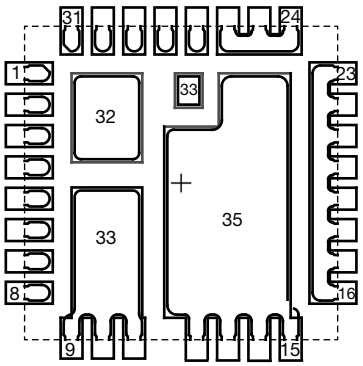
RECOMMENDED LAND PATTERN POWERPAK MLP55-31L

Package outline top view, transparent



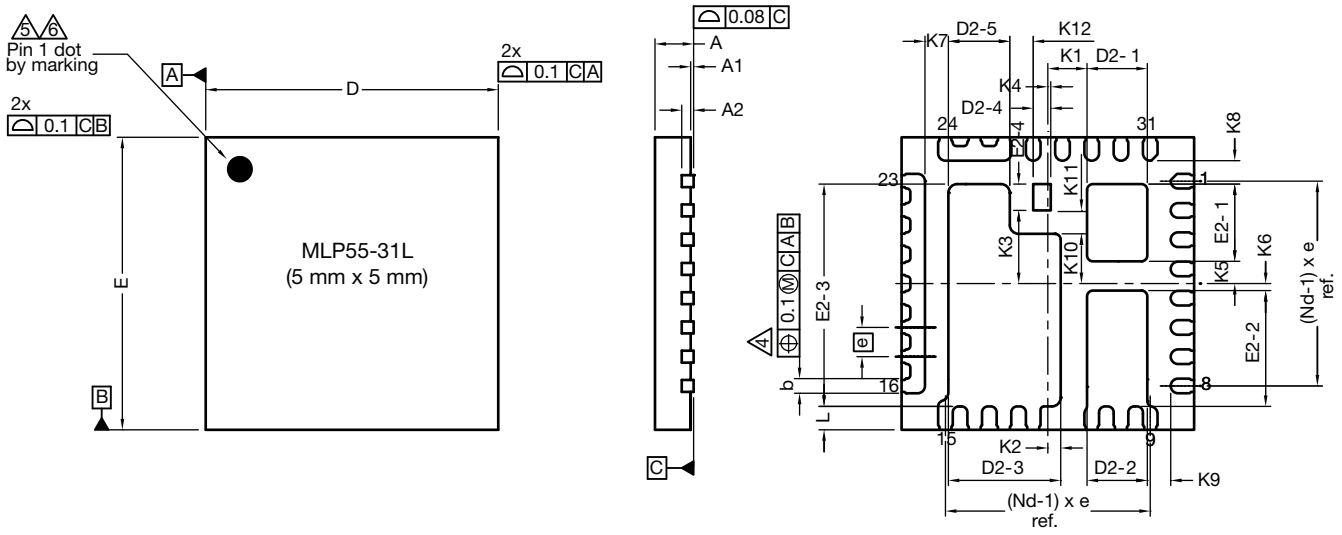
Land pattern for MLP55-31L





All dimensions in millimeters

PACKAGE OUTLINE DRAWING MLP55-31L



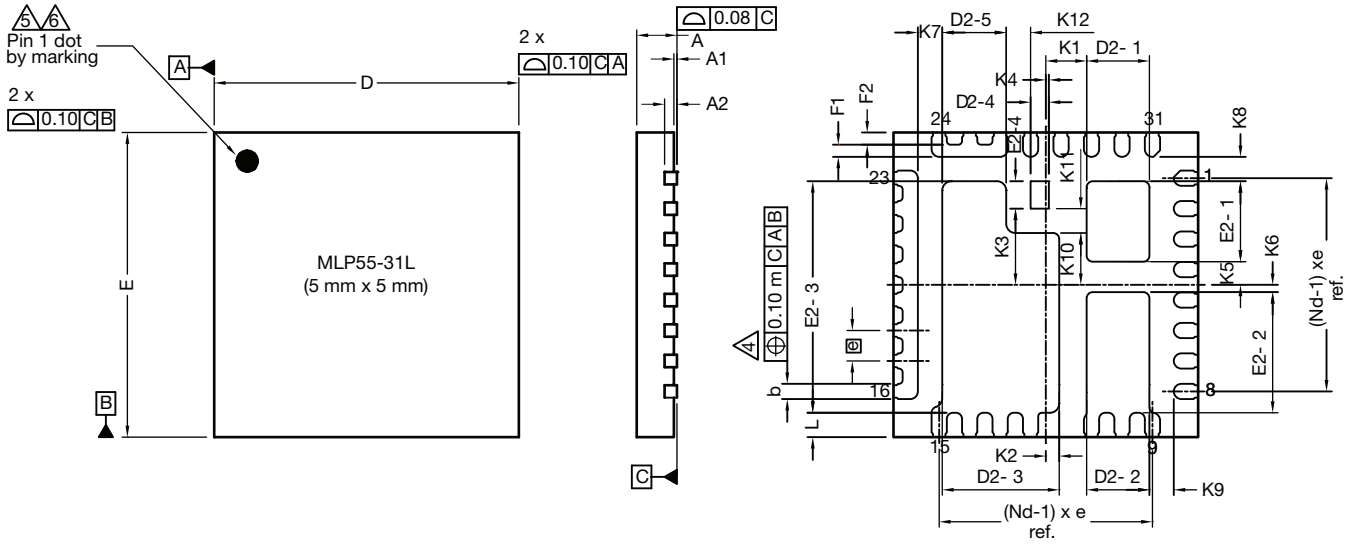
Top view Side view Bottom view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b (4)	0.20	0.25	0.30	0.008	0.010	0.012
D		5.00 BSC			0.196 BSC	
e		0.50 BSC			0.019 BSC	
E		5.00 BSC			0.196 BSC	
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)		32			32	
Nd (3)		8			8	
Ne (3)		8			8	
D2-1	0.98	1.03	1.08	0.039	0.041	0.043
D2-2	0.98	1.03	1.08	0.039	0.041	0.043
D2-3	1.87	1.92	1.97	0.074	0.076	0.078
D2-4		0.30 BSC			0.012 BSC	
D2-5	1.00	1.05	1.10	0.039	0.041	0.043
E2-1	1.27	1.32	1.37	0.050	0.052	0.054
E2-2	1.93	1.98	2.03	0.076	0.078	0.080
E2-3	3.75	3.80	3.82	0.148	0.150	0.152
E2-4		0.45 BSC			0.018 BSC	
K1		0.67 BSC			0.026 BSC	
K2		0.22 BSC			0.008 BSC	
K3		1.25 BSC			0.049 BSC	

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
K4		0.05 BSC			0.002 BSC	
K5		0.38 BSC			0.015 BSC	
K6		0.12 BSC			0.005 BSC	
K7		0.40 BSC			0.016 BSC	
K8		0.40 BSC			0.016 BSC	
K9		0.40 BSC			0.016 BSC	
K10		0.85 BSC			0.033 BSC	
K11		0.40 BSC			0.016 BSC	
K12		0.40 BSC			0.016 BSC	

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62992.

PowerPAK® MLP55-31L Case Outline



Top view Side view Bottom view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b (4)	0.20	0.25	0.30	0.008	0.010	0.012
D	4.90	5.00	5.10	0.193	0.196	0.200
e		0.50 BSC			0.019 BSC	
E	4.90	5.00	5.10	0.193	0.196	0.200
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)		32			32	
Nd (3)		8			8	
Ne (3)		8			8	
D2-1	0.98	1.03	1.08	0.039	0.041	0.043
D2-2	0.98	1.03	1.08	0.039	0.041	0.043
D2-3	1.87	1.92	1.97	0.074	0.076	0.078
D2-4		0.30 BSC			0.012 BSC	
D2-5	1.00	1.05	1.10	0.039	0.041	0.043
E2-1	1.27	1.32	1.37	0.050	0.052	0.054
E2-2	1.93	1.98	2.03	0.076	0.078	0.080
E2-3	3.75	3.80	3.82	0.148	0.150	0.152
E2-4		0.45 BSC			0.018 BSC	
F1		0.20 BSC			0.008 BSC	
F2		0.20 BSC			0.008 BSC	
K1		0.67 BSC			0.026 BSC	
K2		0.22 BSC			0.008 BSC	
K3		1.25 BSC			0.049 BSC	
K4		0.05 BSC			0.002 BSC	
K5		0.38 BSC			0.015 BSC	
K6		0.12 BSC			0.005 BSC	

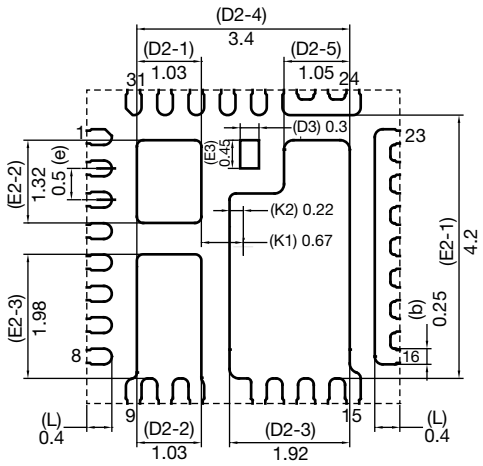
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
K7		0.40 BSC			0.016 BSC	
K8		0.40 BSC			0.016 BSC	
K9		0.40 BSC			0.016 BSC	
K10		0.85 BSC			0.033 BSC	
K11		0.40 BSC			0.016 BSC	
K12		0.40 BSC			0.016 BSC	
ECN: T16-0644-Rev. E, 24-Oct-16 DWG: 6025						

Notes

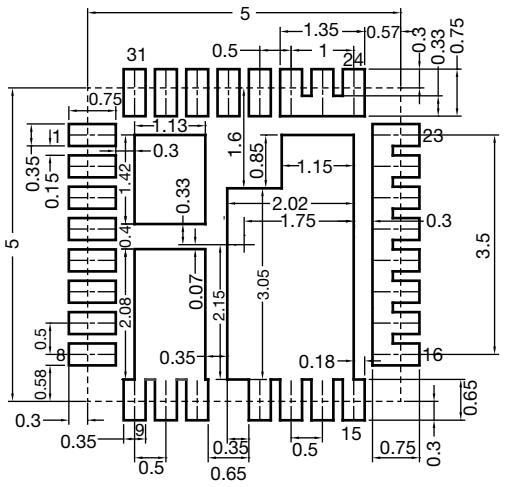
1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. N is the number of terminals,
   Nd is the number of terminals in X-direction, and
   Ne is the number of terminals in Y-direction
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals

Recommended Land Pattern
PowerPAK® MLP55-31L for SiC620, SiC620A

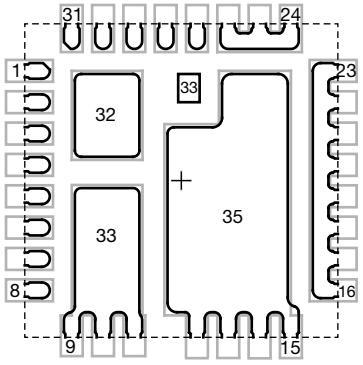
Top side transparent view
(not bottom view)



Land pattern for MLP55-31L



All dimensions in millimeters



Component for MLP55-31L

Land pattern for MLP55-31L

VRPower® Integrated Power Stage Solution

By Ron Vinsant

VRPower® products are integrated power stage solutions optimized for high-performance synchronous buck applications. These devices offer high power conversion efficiency and high power density with low electrical parasitics due to both excellent silicon (MOSFETs and drivers) and packaging design techniques. The devices are available in Vishay's proprietary 4.5 mm by 3.5 mm package for 30 A applications, and the industry-standard 5 mm by 5 mm thermally enhanced MLP package for 60 A applications.

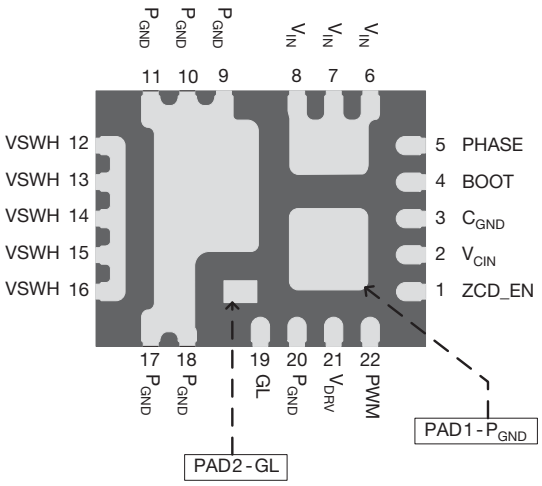


Fig. 1 - 3.5 mm by 4.5 mm package

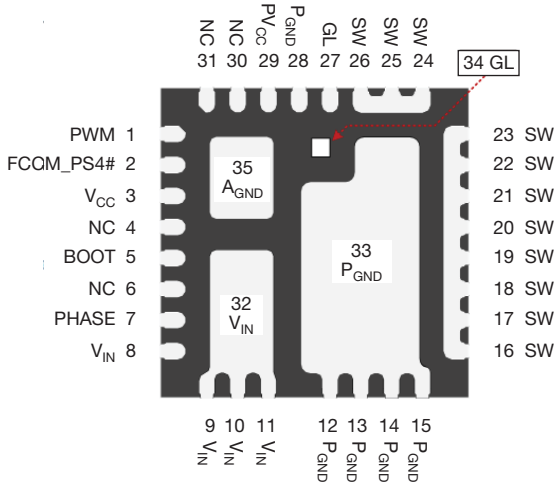


Fig. 2 - 5 mm by 5 mm package

VRPower devices are primarily intended for use in applications with 12 V inputs and < 2 V outputs. The power devices - MOSFETs - are asymmetrical to match the expected duty ratios in the intended operating range. The internal drivers are then matched to the MOSFETs to maximize efficiency.

This application document is meant to be used as a guide to the performance possibilities of some of the most popular Vishay VRPower products. We will cover efficiency and power loss over the operating frequency range of 400 kHz to 1 MHz. The 3.5 mm by 4.5 mm, 30 A device (SiC530) will be covered first, followed by the 5 mm by 5 mm, 60 A device (SiC620). Future application documents will cover EMC, boot resistor, capacitor, and thermal issues, and how they are affected by layout.

The "rated current" of a VRPower device is not an indicator of its performance under steady-state conditions. While it can be misleading, it is intended to be a guide for those applications where there are transient operating conditions requiring high peak currents, such as processors.

APPLICATION NOTE

VRPower® Integrated Power Stage Solution

SiC530: 3.5 mm by 4.5 mm, 30 A

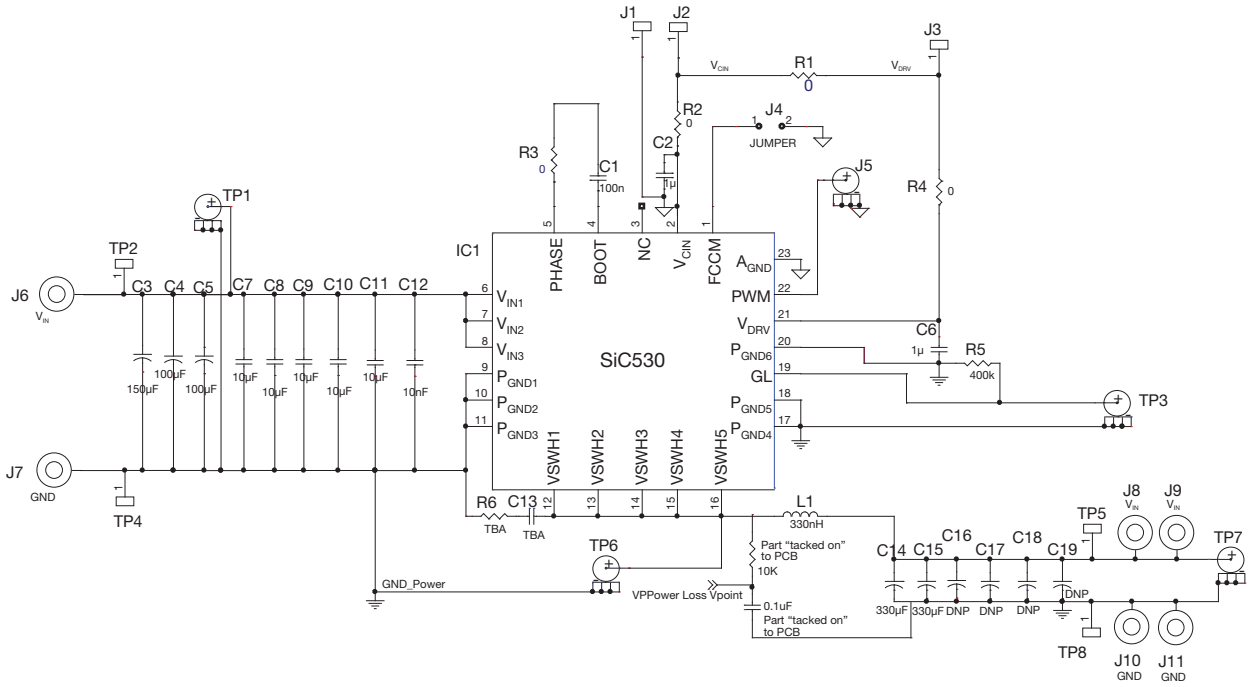


Fig. 3 - SiC530: 3.5 mm by 4.5 mm test board schematic

EFFICIENCY, POWER LOSS, AND OPERATING FREQUENCY

The SiC530 is normally used over a frequency operating range of 500 kHz to 1 MHz. The graph below shows efficiency and bias power requirements over that operating range.

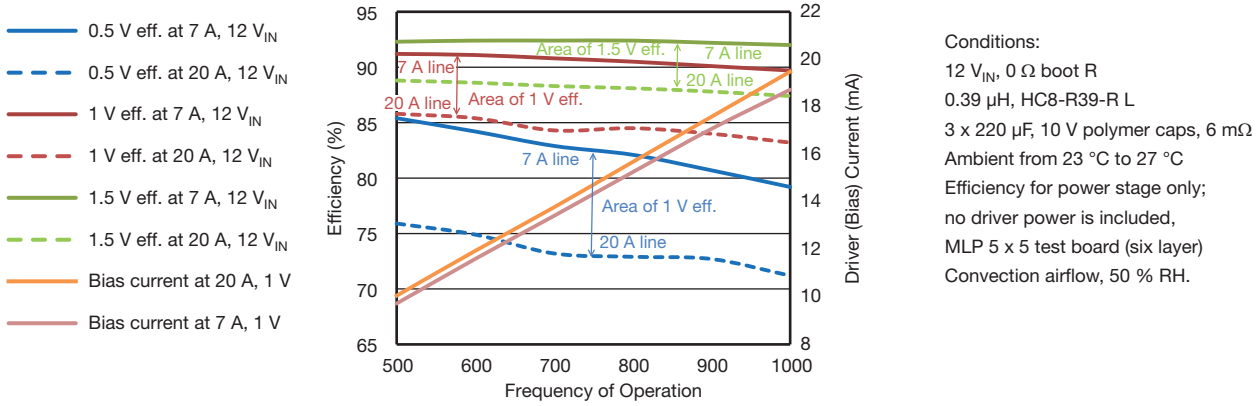


Fig. 4 - Area of efficiency from peak efficiency point (7 A) to max. current (20 A) for three different operating points: 0.5 V, 1 V, and 1.5 V outputs with 5 V MOSFET drive bias currents

Although the SiC530 is rated at 25 A, our testing was limited to 20 A for Fig. 4 due to our PCB construction being only six layers. Since the PCB supplies much of the heatsinking for the SiC530, its thermal properties are critical.

We are often asked about the expected performance of a SiC530. It is a difficult question to answer in general, and even more difficult to answer with any precision. It is instructive, however, to look at some typical examples that are in common use. One such example is shown below in Fig. 5.

VRPower® Integrated Power Stage Solution

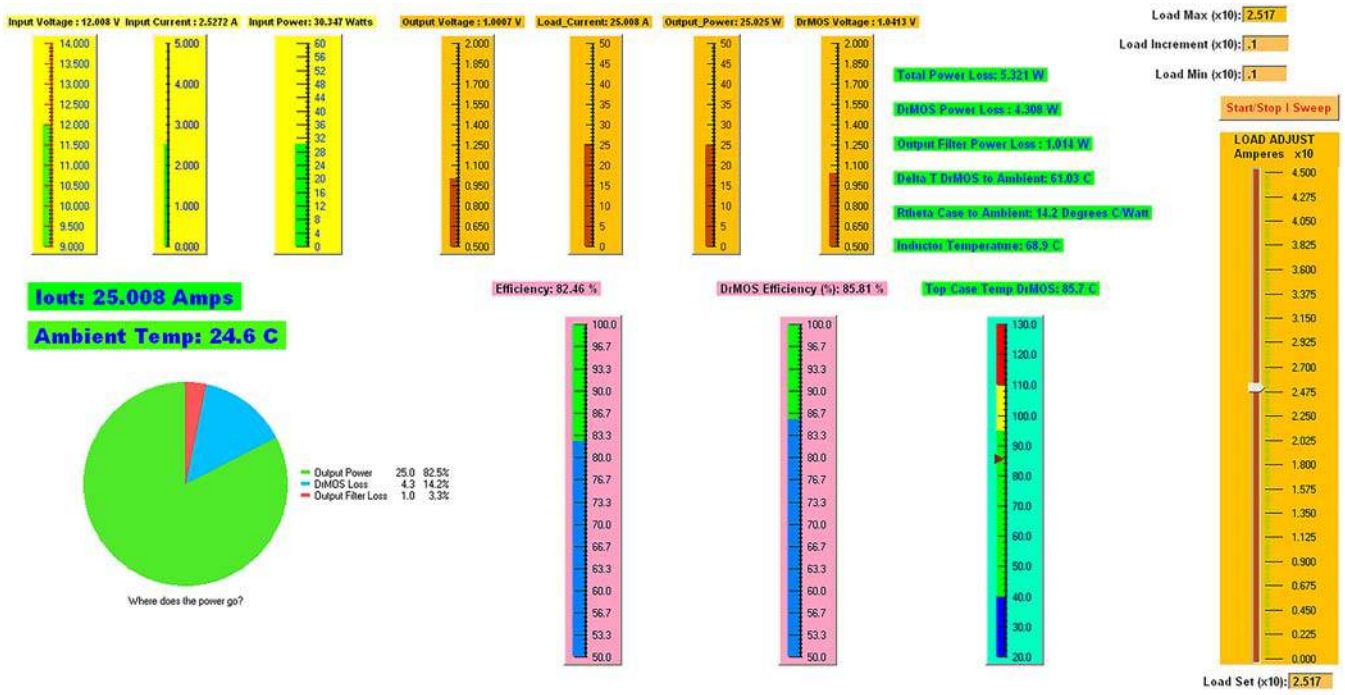
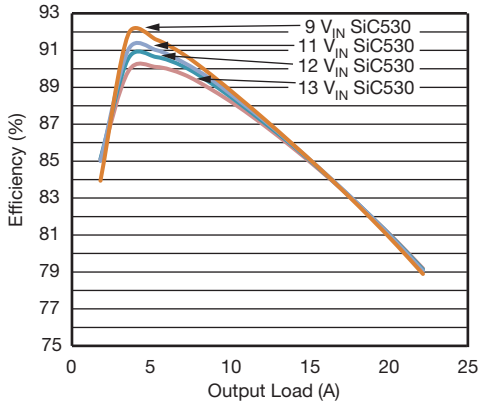


Fig. 5 - "Dashboard" example of the typical performance of a SiC530 with a 1 V output at 500 kHz

In Fig. 5 we can observe some of the expected operating temperatures of key components and their corresponding power losses when using a SiC530 in a 12 V_{IN}, 1 V_{OUT}, 500 kHz application at 25 A.

The term "filter loss" refers to the combination of the filter cap losses and inductor losses. These losses are typically dominated by the inductor.

In Fig. 6 below we can see efficiency at higher frequency operation.



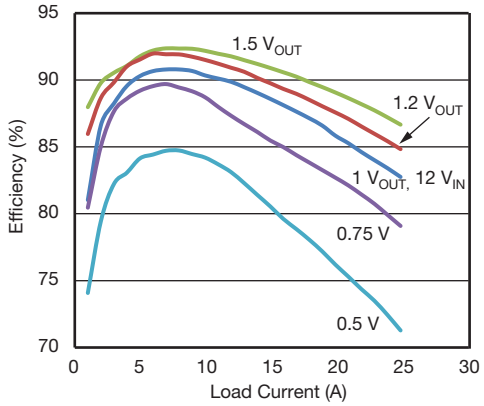
Conditions:
Ambient: 23 °C to 28 °C
0.9 V_{OUT}, 800 kHz
0.22 µH, 3.9 mΩ DCR
(custom)
100 µF x 5R, 1206 caps (13 µA)
220 µF POSCAPS (4)
Single-phase, 0 Ω boot R
SiC530 temp (on top) 65.3 °C at 20 A with 13 V_{IN}
SiC530 efficiency only; does not
include all bias power for board
and controller

Fig. 6 - SiC530 800 kHz, 0.9 V_{OUT} single-phase efficiency vs. load for different V_{IN}

APPLICATION NOTE

VRPower® Integrated Power Stage Solution

In Fig. 7 below we show operation at 500 kHz.



Conditions: 12 V_{IN}, 0 Ω boot R
Inductor: Coiltronics, HC-R39-R, 0.39 µH,
1.55 mΩ DCR
3 x 220 µF, 10 V, polymer cap, 6 mΩ ESR
Ambient: 23 °C to 27 °C
Efficiency for power stage only; no driver power
Convection airflow, 50 % RH
Six-layer PCB

Fig. 7 - Efficiency of SiC530 at 500 kHz for 12 V_{IN} with 0.5 V to 1.5 V output voltage vs. load current

APPLICATION NOTE

VRPower® Integrated Power Stage Solution

SiC620: 5 mm by 5 mm, 60 A

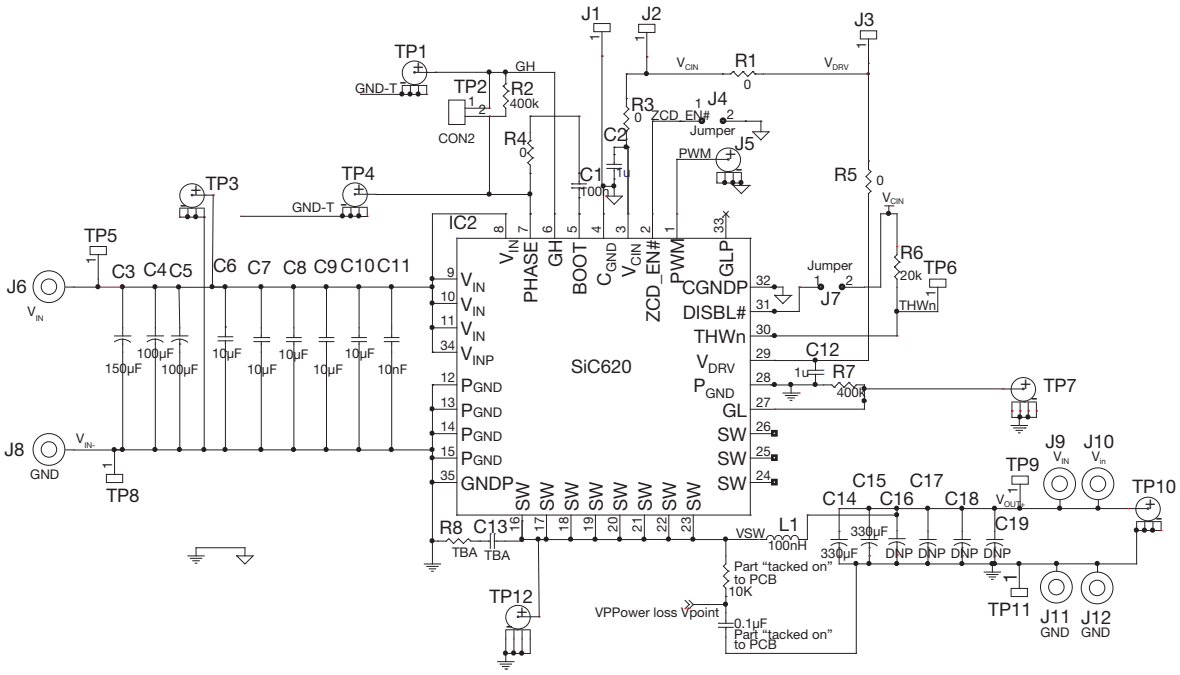
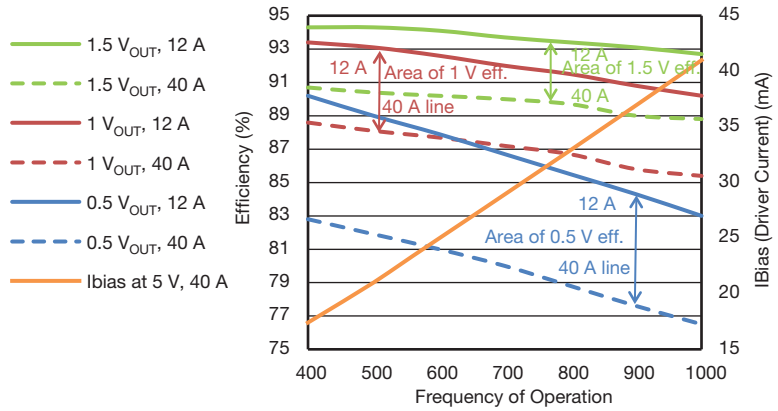


Fig. 8 - SiC620: 5 mm by 5 mm test board schematic

EFFICIENCY, POWER LOSS, AND OPERATING FREQUENCY

The SiC620 is normally used over a frequency operating range of 400 kHz to 1 MHz. The graph below shows efficiency and bias power requirements over that operating range.



Conditions: 12 V_{IN}, 0 Ω boot R
Inductor: Coiltronics, HC8-R39-R, 0.39 µH, 1.55 mΩ DCR
3 x 220 µF, 10 V, polymer cap, 6 mΩ ESR
Ambient: 23 °C to 27 °C
Efficiency for power stage only; no driver power
Convection airflow, 50 % RH
Six-layer PCB

Fig. 9 - Area of efficiency from peak efficiency point (12 A) to max. current (40 A) for three different operating points: 0.5 V, 1 V, and 1.5 V outputs with 5 V MOSFET drive bias currents

APPLICATION NOTE

VRPower® Integrated Power Stage Solution

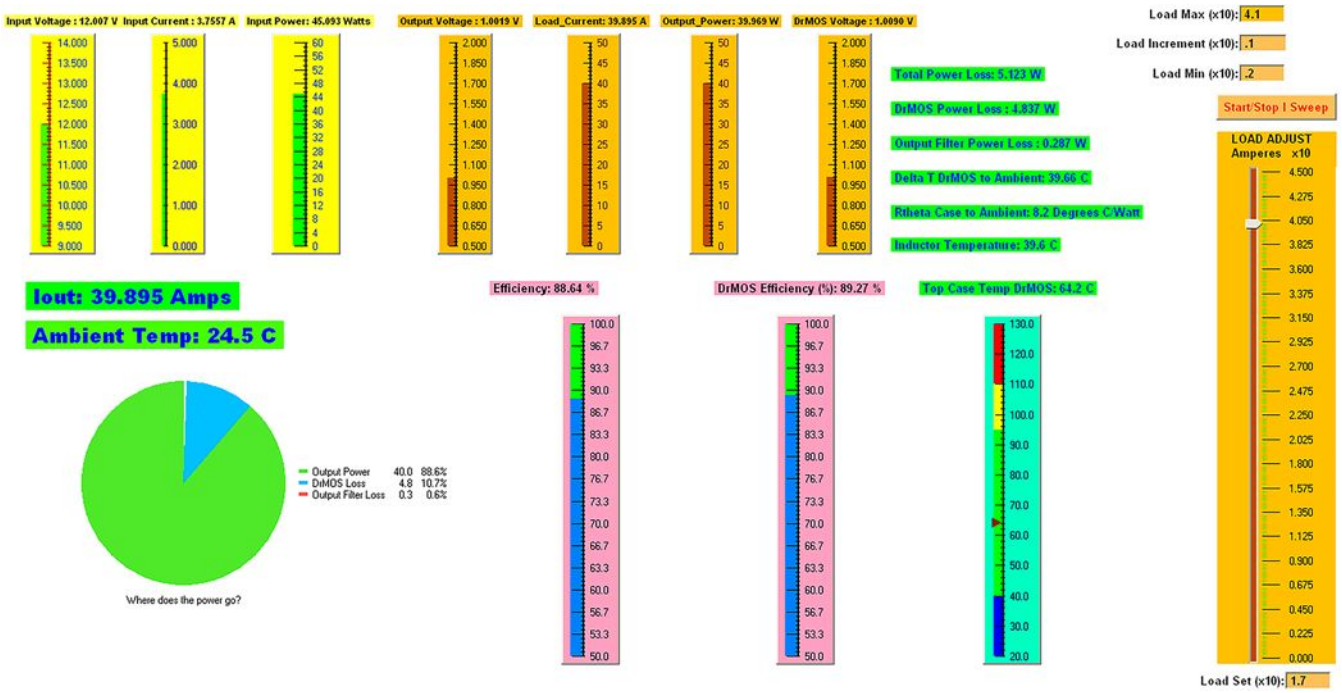
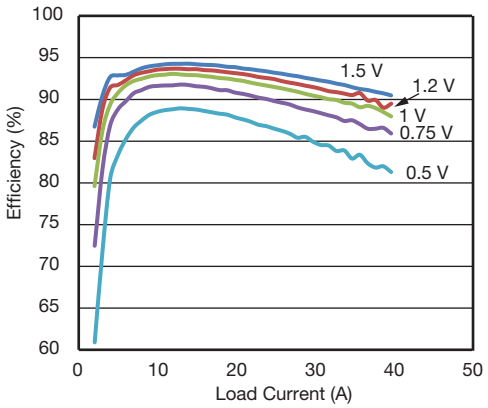


Fig. 10 - "Dashboard" example of the typical performance of the SiC620 with a 40 A, 1 V output at 412 kHz

In Fig. 10 we can observe some of the expected operating temperatures of key components and their corresponding power losses when using an SiC620 in a 12 V_{IN}, 1 V_{OUT}, 412 kHz application at 40 A. Unlike the SiC530 tests, the SiC620 tests were run with some airflow, as this would be the normal environment in higher-power applications.

The term "filter loss" is the combination of the filter cap losses and inductor losses. These losses are typically dominated by the inductor; output filter capacitors are a very small loss term in most applications.

In Fig. 11 below we show operation at 500 kHz.



Conditions:
12 V_{IN}, 0 Ω boot R, 500 kHz
0.25 µH, 744309025 Wurth
3 x 220 µF, 10 V, polymer caps, 6 mΩ
Ambient: 23 °C to 27 °C
Efficiency for power stage only;
no driver power is included
MLP 5 x 5 test board (six-layer)
Convection airflow, 50 % RH

Fig. 11 - Efficiency of SiC620 at 500 kHz for 12 V_{IN} with 0.5 V to 1.5 V output voltage vs. load current

APPLICATION NOTE

VRPower® Integrated Power Stage Solution

ISSUES RELATED TO ALL VRPower PRODUCTS

Inductor Power Loss

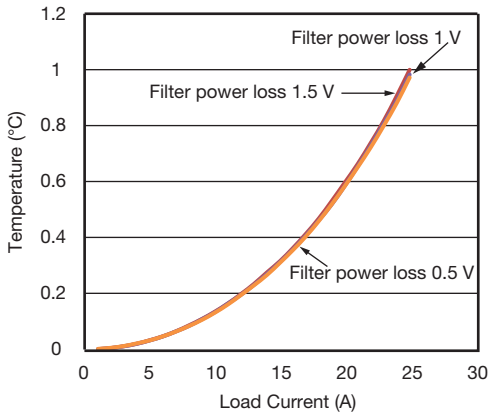


Fig. 12 - Output filter power loss for three different operating points (0.5 V, 1 V, and 1.5 V) for an SiC530

This shows that in general, the power loss in the filter (L1 and C14 through C19, referring to Fig. 3) is dominated by the DC loss term and not AC (magnetic core) losses. This would leave one to believe that the temperature of the inductor would only change due to load and not V_{OUT}.

This is not true, however. The inductor temperature does change with V_{OUT}, as we can see below.

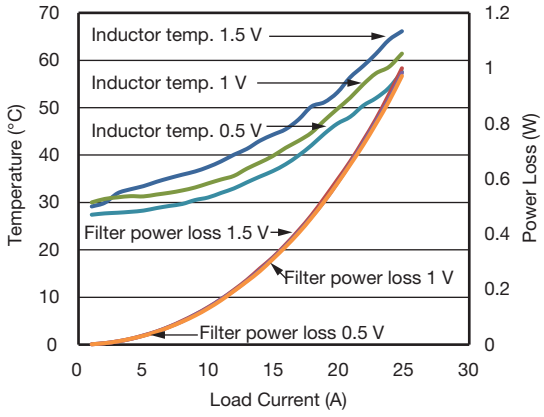


Fig. 13 - Output filter power loss and temperature for three different operating points - 0.5 V, 1 V, and 1.5 V

If a good electrical layout is achieved, the inductor is always placed as close as possible to the V_{SW} pins of the SiC530 to minimize inductance in the path, which causes ringing that places added stress on the device.

APPLICATION NOTE

VRPower® Integrated Power Stage Solution

Here is an example PCB layout showing how close the two components should be.

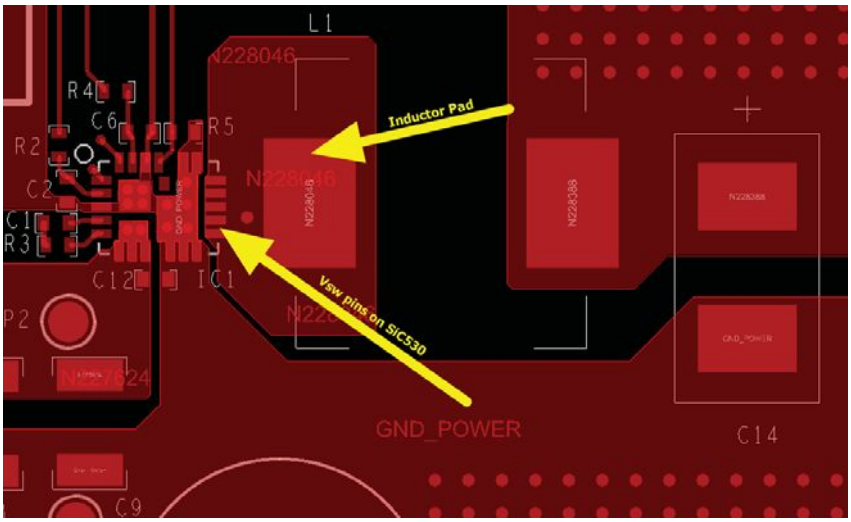


Fig. 14 - SiC530 evaluation board layout showing the close proximity of an inductor to the SiC530

Being close to the switching device allows the inductor to absorb heat from the SiC530; in other words it is a heatsink, and thus is very important to the thermal design of the regulator. If the inductor is placed in airflow it will help keep temperatures down. Keeping other PCB-mounted components out of the airflow path passing the inductor is always helpful.

Below, we can observe that losses, and therefore temperature rise, in the SiC530 are not linearly proportional to V_{OUT} for any specific load point.

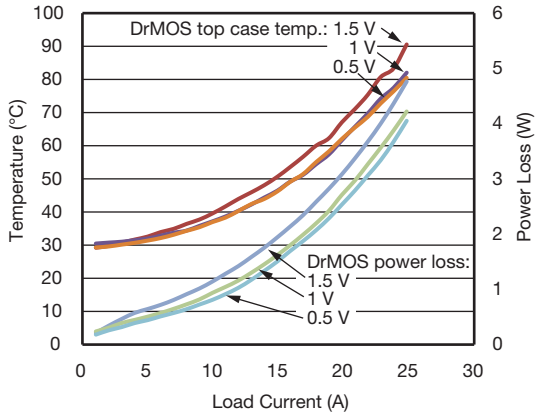


Fig. 15 - SiC530 power loss and top case temperature

This non-linearity shows that while a 1.5 V, 25 A output might not meet required design goals due to temperature rise, at 1 V such a design might be acceptable due to the lower operating temperature of the SiC530.

Please note we are using the same inductor for all outputs for this test. In a typical system design the inductor value would change depending on load specifications such as ripple and transient response. Since the peak value of current in the inductor is one of the parameters that determines switching loss in the high-side MOSFET, results might be different for lower voltages with smaller-value inductors.

VRPower® Integrated Power Stage Solution

Inductor Core Loss

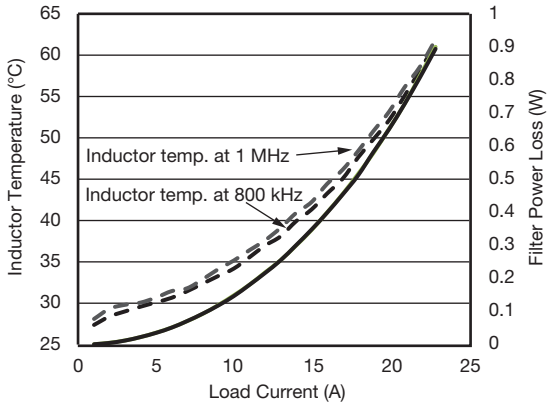
It is often stated that increasing the switching frequency is not prudent as it will increase magnetic losses. If the value of the inductor does not change and the frequency increases, core losses actually go down, not up, as the delta B (flux swing) in the inductor is less.

A typical model for core loss is shown below:

$PL = 492 \times B^{2.22} f^{1.32}$ for Magnetics Inc. high-flux 60 µ core material,

where PL is power loss, B is one half the peak-to-peak flux swing, and f is frequency. Note that the exponent for B is much greater than for f.

Below is an example (note there is little to no change in power loss in the inductor).



Circuit and conditions:
13 V_{IN}, 0.9 V_{OUT}, 0 Ω boot R
800 kHz and 1 MHz
0.22 µH, 8 mm x 8 mm
3 x 220 µF, 10 V, polymer cap,
6 mΩ ESR
Ambient: 23 °C to 27 °C
Power stage only; no driver power
CCM driver power is
SiC530 800K
15.3 mA at 5 V = 76.5 mW
SiC530 1 MHz
18.9 mA at 5 V = 94.5 mW

Fig. 16 - Inductor loss and temperature at two operating frequencies with the same inductor in an SiC530

The additional change in temperature of the inductor is, as we have shown above, due to the increased switching losses in the SiC530, and not inductor loss.

VRPower® Integrated Power Stage Solution

Inductor Saturation

In some VRPower applications, space is critical and the largest component is most often the inductor. Due to its large size, it is the first component to be addressed in solving any space issues.

As the size of the inductor decreases, its ability to store energy decreases. This is dependent on a number of factors, such as magnetic material and operating temperature. If the saturation level of the inductor is exceeded, the currents in the VRPower MOSFETs will increase and cause additional power loss in the VRPower device.

Observing the current in the inductor with a current probe is a useful way of determining if the inductor is heading into saturation.

Below is an example of the normal operation of two inductors of the same type.

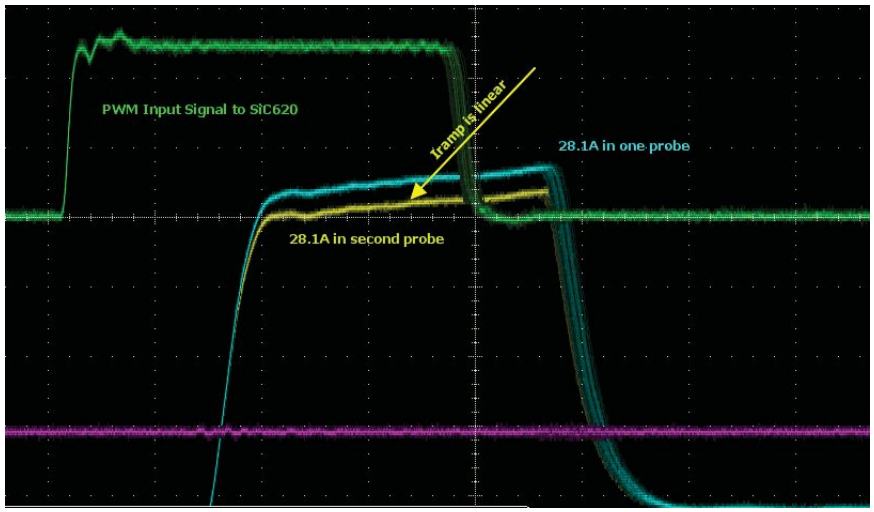


Fig. 17 - Normal inductor operation; linear current ramp

With only a small increment in current from 28.1 A to 30.27 A, we can see the current ramp becoming non-linear.

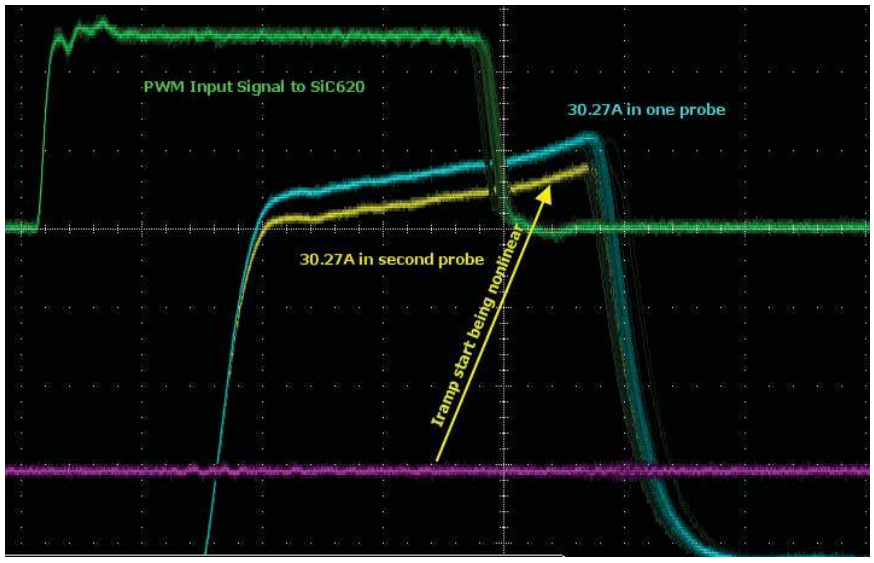


Fig. 18 - Border-line inductor operation; current ramp becoming non-linear

VRPower® Integrated Power Stage Solution

With yet another small increment from 30.27 A to 32.2 A, we see a very large increase in peak current.

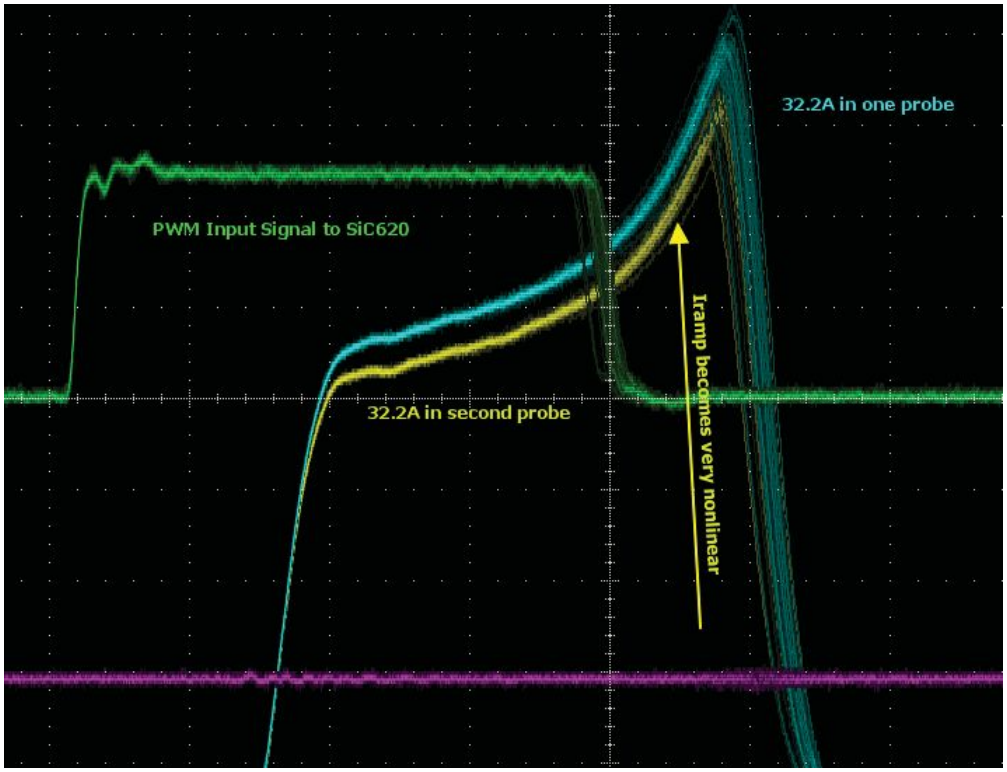


Fig. 19 - Saturated inductor operation; current ramp very non-linear

The peak current increases both conduction losses and switching losses in the high-side MOSFETs of the VRPower device. Operation in this region should be avoided due to increased stresses on the MOSFETs.

If the control system utilizes DCR current sensing, there is also the issue of inaccuracy of the current sense value due to the non-linearity of the value of L.

Another question that frequently arises is the effect of varying L on efficiency and power loss. There are many variables involved, such as PCB layout, physical and electrical size of the inductor, input voltage, boot resistor value, etc.

In Fig. 20 below, we show an example of what might be expected in a typical application for the SiC620. We use three different inductors. One is a 220 nH device with a “standard” height of 6 mm from Vishay; the second is a competitor’s 6 mm inductor, also of 220 nH; and an 8 mm, 300 nH inductor from Vishay. For any specific operating point, a large value of L results in a lower peak current decreasing the switching loss in the upper MOSFET and increasing efficiency. In addition, a larger physical size of L will result in additional heatsinking, further increasing efficiency and lowering operating temperatures. However, this increase in L will lower the ability of the control loop to respond to transient events.

VRPower® Integrated Power Stage Solution

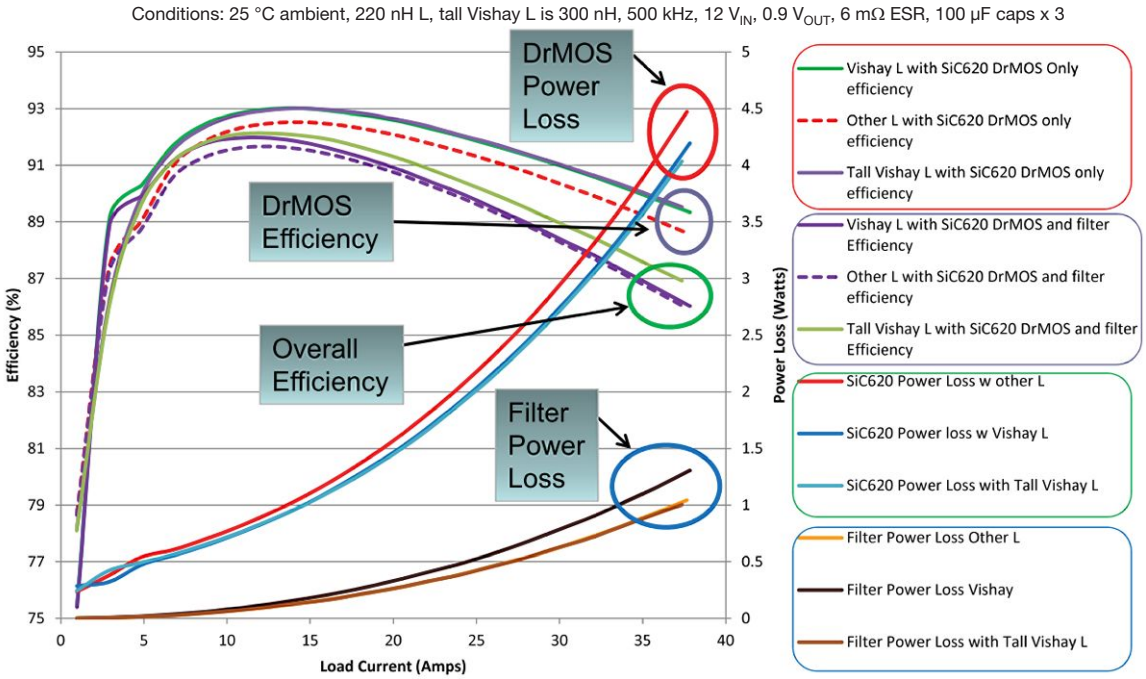
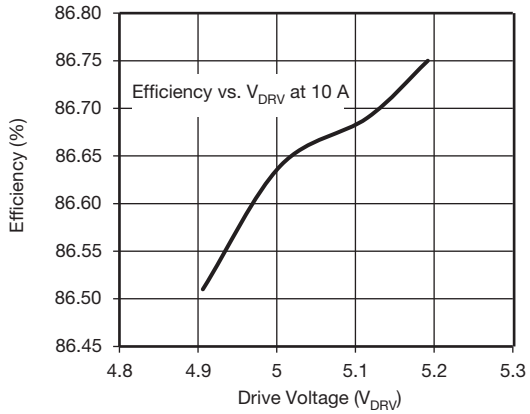


Fig. 20 - Efficiency and power losses vs. load current for the SiC620 with different inductors

A design tool for inductor selection can be found here: www.vishay.com/inductors/calculator/calculator/

V_{DRV} Supply Voltage (MOSFET Gate Voltage)

VRPower devices use a 5 V drive for MOSFET enhancement. Varying this voltage over a small range will not substantially affect the efficiency of the devices. Fig. 21 below shows the effects on efficiency with changes in drive voltage.



Circuit and conditions:
13 V_{IN}, 0.9 V_{OUT}, 1.006 MHz
0.22 µH, 1 mΩ DCR L
3 x 220 µF, 10 V, polymer cap,
6 mΩ ESR
Ambient: 26 °C
Power stage only; no driver power
CCM driver power is
27.6 mA at 5 V = 138 mW
MLP 5 x 5 Test Board

Fig. 21 - Effect on efficiency due to drive voltage on SiC631 (3.5 mm x 4.5 mm)

Although these devices have a UVLO, it is prudent to design the system so that when in operation the VRPower device has a minimum value of 4.5 V for V_{DRV}.

APPLICATION NOTE

VRPower® Integrated Power Stage Solution

V_{CIN} Supply Voltage (Driver V_{CC} Voltage)

It is important that the supply voltage rail for the driver and the controller generating the PWM signal be the same. This requirement is due to the tri-state inputs on the PWM signal to the VRPower device.

Below is a simplified schematic of a VRPower device being driven by a system regulator.

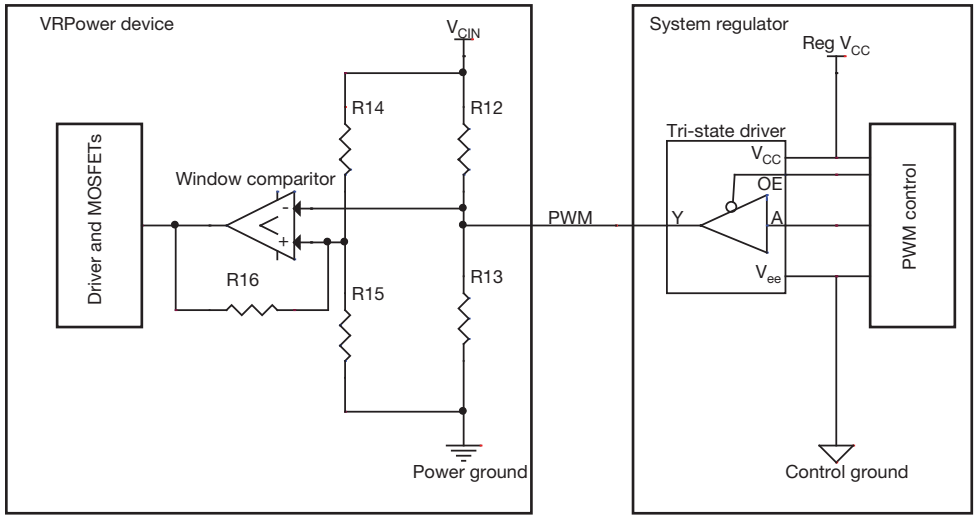


Fig. 22 - Simplified schematic of a VRPower device driven by a system regulator with separate grounds and supply rails

As V_{CIN} changes in magnitude, the threshold of the window comparator sensing the signal from the system regulator tri-state driver will change. If the system regulator's supply rail, Reg V_{CC}, is active before the VRPower device's V_{CIN}, then there can be a region of operation as V_{CIN} rises where the device can have false triggering of the drivers and MOSFETs, leading to erratic behavior and possible device failure.

To a lesser extent this is also true of the ground paths. In order to reduce noise on the PWM signal, it is best not to have the grounds tied as shown in Fig. 22 above, but to tie both power rails and grounds of the system regulator and VRPower device together, as shown below.

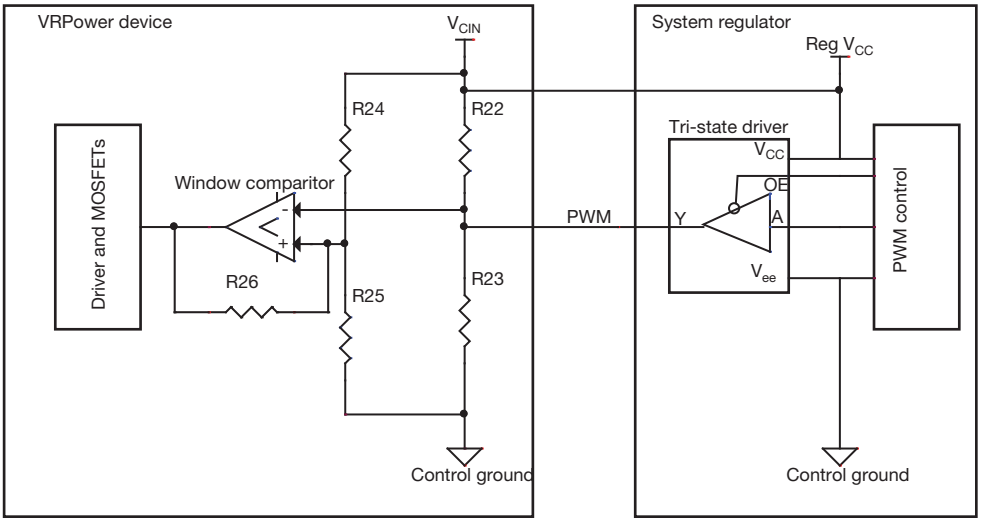


Fig. 23 - Simplified schematic of a VRPower device driven by a system regulator with properly tied grounds and supply rails

VRPower® Integrated Power Stage Solution

Minimum on Time

At higher frequencies like 1 MHz and large input-voltage-to-output-voltage ratios, the parameter of minimum on time, $t_{PWM\_ON\_MIN}$, may be of concern. Since the ratio of V_{IN} to V_{OUT} when in continuous conduction mode is set by the ratio of the high-side MOSFET on time to the off time,

Time on = V_{OUT}/V_{IN} x 1 period; e.g. 0.5 V/12 = 0.0417 or a 4.17 % on time in 1 µs. This equates to 41.7 ns, which is less than the specified minimum PWM input of 50 ns.

Also consider this parameter on transient response. At load release, the PWM should be at as narrow a width as possible, or perhaps not be generated at all. When simulations are being run, this non-linearity must be considered.

CONCLUSIONS

1. Use the peak current rating as a “pulse” rating; not as a steady-state operating current specification.
2. The inductor is an important contributor to thermal, as well as electrical, design.
3. Do place the inductor close to the VRPower device in the PCB layout.
4. V_{OUT} has a large effect on operating temperature. Higher currents might be possible for applications where the operating temperature is the same, but since output voltage is lower, power loss is less, and therefore output current can be higher.
5. When selecting an inductor, be sure to assess the saturation parameters to minimize thermal and electrical stress on the VRPower device.
6. MOSFET drive voltage has little effect on overall efficiency, but should not drop below 4.5 V.
7. The control system and the VRPower device should be supplied from the same V_{CC} rail.
8. The control system ground should be tied to the analog ground of the VRPower device, not the power ground.
9. Take into account the minimum PWM input pulse when considering operating frequency in your design.

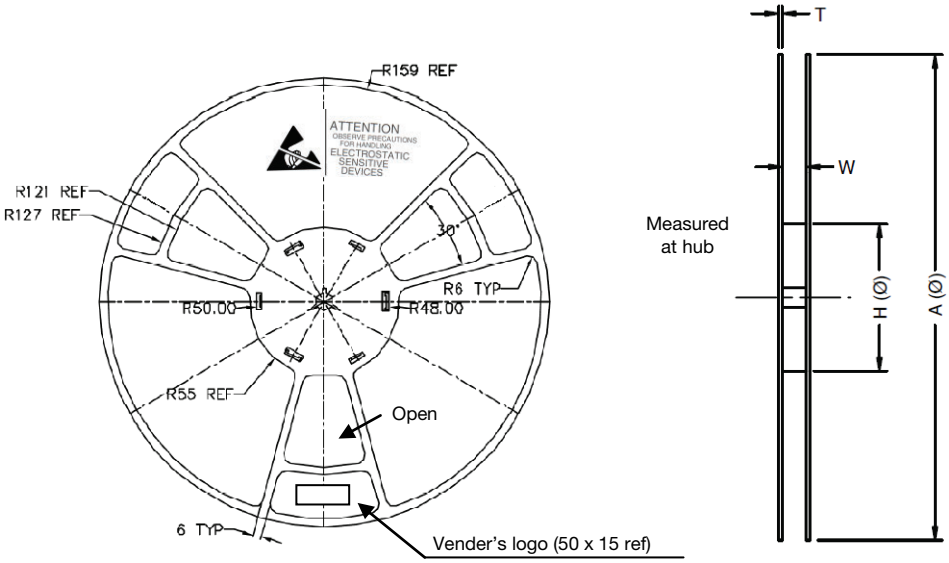
ENVIRONMENTAL AND PACKAGE TESTING DATA FOR POWERPAK® MLP55					
STRESS	**SAMPLE SIZE**	**DEVICE HRS./CYC**	**CONDITION**	**TOTAL FAILS**	**FAIL PERCENTAGE**
Bond Integrity	82	41 000	200 °C + N2	0	0.00
HAST	246	24 600	130 °C, 85 % RH	0	0.00
Pressure Pot	246	23 616	121°C, 15 PSIG	0	0.00
Solder Dunk	164	492	260 °C, 10 s	0	0.00
Temp. Cycle	246	246 000	-65 °C to +150 °C	0	0.00

ACCELERATED OPERATING LIFE TEST RESULT	
Sample Size	2459
Equivalent Device Hours	278 826 325
Failure Rate in FIT	4.454

Failure Rate in FIT is calculated according to JEDEC® Standard JESD85, *Methods for Calculating Failure Rates in Units of FITs,* based on accelerated high temperature operating life test results by using an apparent activation energy of 0.7 eV. The junction temperature of the device at use is assumed to be 55 °C. A constant failure rate distribution is assumed. The upper confidence bound of the failure rate is 60 %.

Reel

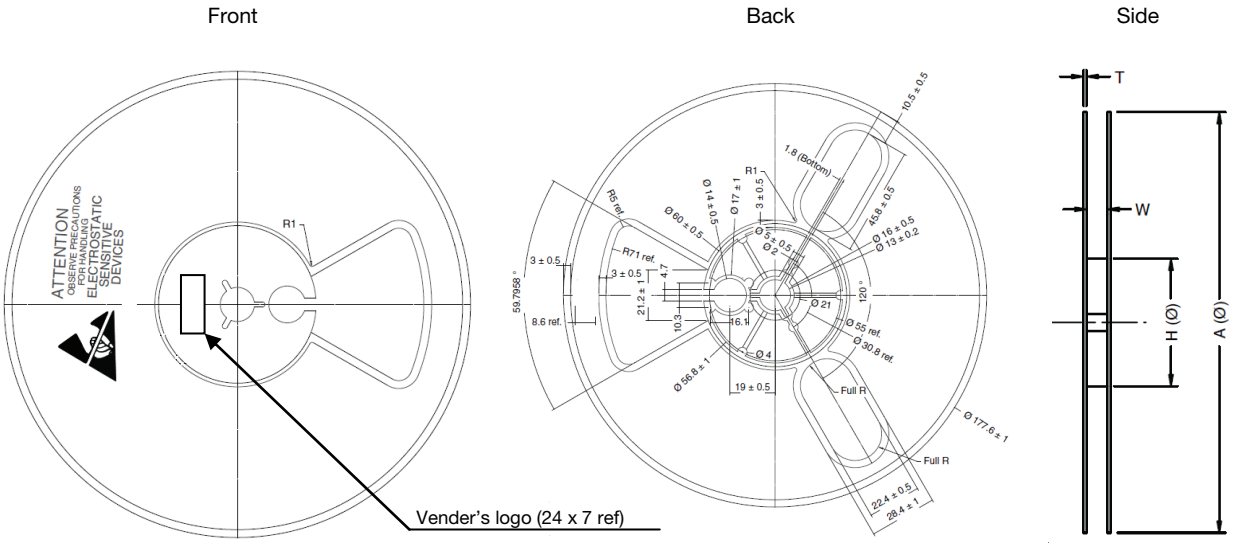
330 mm Reel (Lock Reel)



Notes
1. Material: antistatic or conductor plastic
2. All dimensions in mm
3. ESD-surface resistivity -10^4 Ω to 10^{11} Ω
4. Color: black

VER	APPLICATION		A	W	TAPE WIDTH	H	T
- 1	SOIC-14/16 TO-251 (Short Lead) TO-252/TO-252 (Reverse Lead) PLCC-20 TSSOP-8/14/16/20/28 SSOP-24 SOIC-16 (W)	PowerPAK MLF 9 x 9 PowerPAK MLP 6 x 6 MLF 8 x 8 PowerPAK 8 x 8L PowerPAK 8 x 8 MLP77	330 ± 2	16.4 +2.0 -0	16	100 ± 1	2.5 ± 0.5
- 2	SOIC-8 (N), SOIC-8 (N) epad MSOP-8/10 PowerPAK® SO-8 PowerPAK 1212 PowerPAK 1212-8W MICRO FOOT® MLP33-5, MLP33-8, MLP33-10 QFN (4 x 4)/(3 x 3)/DFN-10 (3 x 3)/ MLP44-16L MLP65-18/20L	PolarPAK® MLP55 PowerPAIR® 6 x 5 PowerPAIR 6 x 3 J PowerPAIR SO-8L PolarPAK1215 PowerPAIR 6 x 3.7 PowerPAK SO-8L MLP4.5 x 3.5-22L PKSO8DCWL	330 ± 2	12.4 +2.0 -0	12	100 ± 1	2.5 ± 0.5
- 4	SOT-23/143 SC70 MICRO FOOT	TSOP-6, 1206-8 ChipFET PowerPAK SC70, PowerPAK SC75	330 ± 2	8.4 +1.5 -0	8.4	100 ± 1	2.5 ± 0.5
- 5	SOIC-20W/24W D^2PAK SSOP-28 QSOP-36	PowerPAK MLF 10 x 10	330 ± 2	24.4 +2.0 -0	24	100 ± 1	2.5 ± 0.5
- 8	KGD		330 ± 2	16.4 +2.0 -0	16	130 ± 1	2.5 ± 0.5

178 mm Reel (Complete Reel)

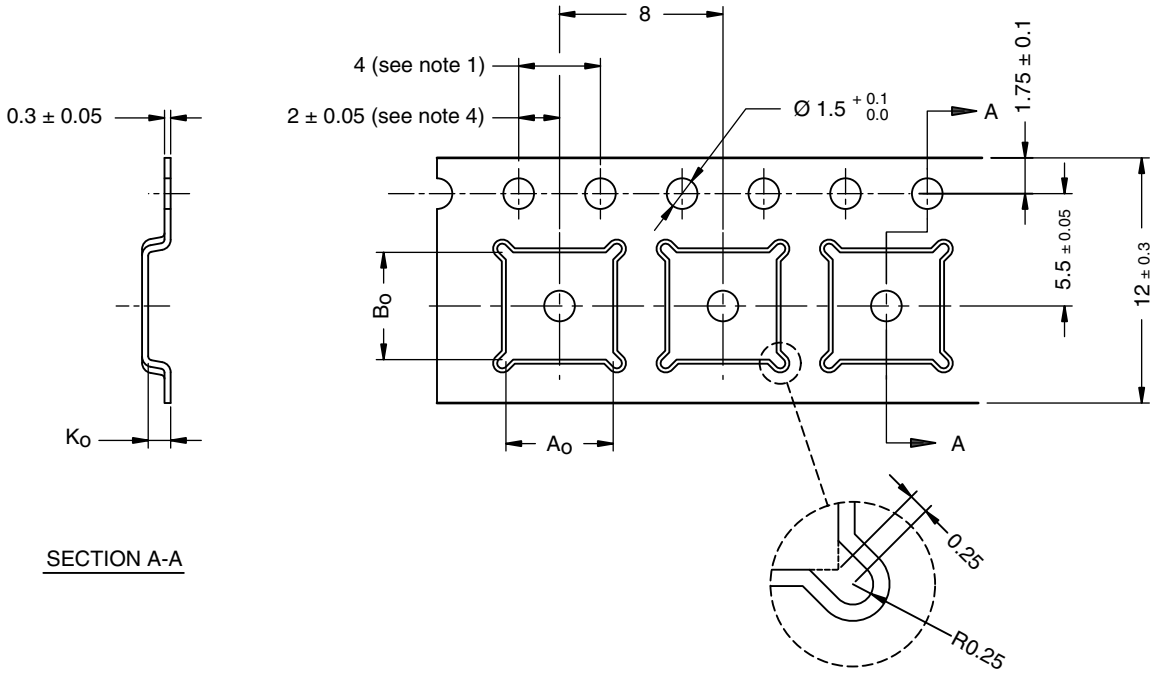


Notes
1. Material: antistatic or conductor plastic
2. All dimensions in mm
3. ESD-surface resistivity -10^4 Ω to 10^{11} Ω
4. Color: black

VER	APPLICATION		A	W	TAPE WIDTH	H	T
- 3	SOT-23/143 TSOP-5/6/SC70JW-8L 1206-8 ChipFET® SC70/SC75A/SC89 MICRO FOOT SC-89 (SOT-666) SOT23-5, 6 KGD WCSP PowerPAK 0806 PowerPAK SC70	PowerPAK SC75 MiniQFN PowerPAK MLP22-5 PowerPAK ChipFET PowerPAK SC75-6L (PIC) PowerPAK TSC75-6L (PIC) TDFN4 1.2 x 1.6, TDFN8 2 x 2 Thin PowerPAK SC-70 Thin PowerPAK SC-75 µDFN-6L 1 x 1 µDFN-4L 1 x 1	178 ± 2	8.4 +1.5 -0	8.4	62 ± 2	1.5 ± 0.5
- 7	MICRO FOOT PowerPAK 2 x 5	KGD	178 ± 2	12.4 +2.0 -0	12	55 ± 2	1.6 ± 0.25

ECN: E17-0619-Rev. BU, 25-Dec-17
DWG: 93-5211-X

Carrier Tape for MLP55



Version	A_O	B_O	K_O
- 1	5.25 ± 0.1	5.25 ± 0.1	1.10 ± 0.1

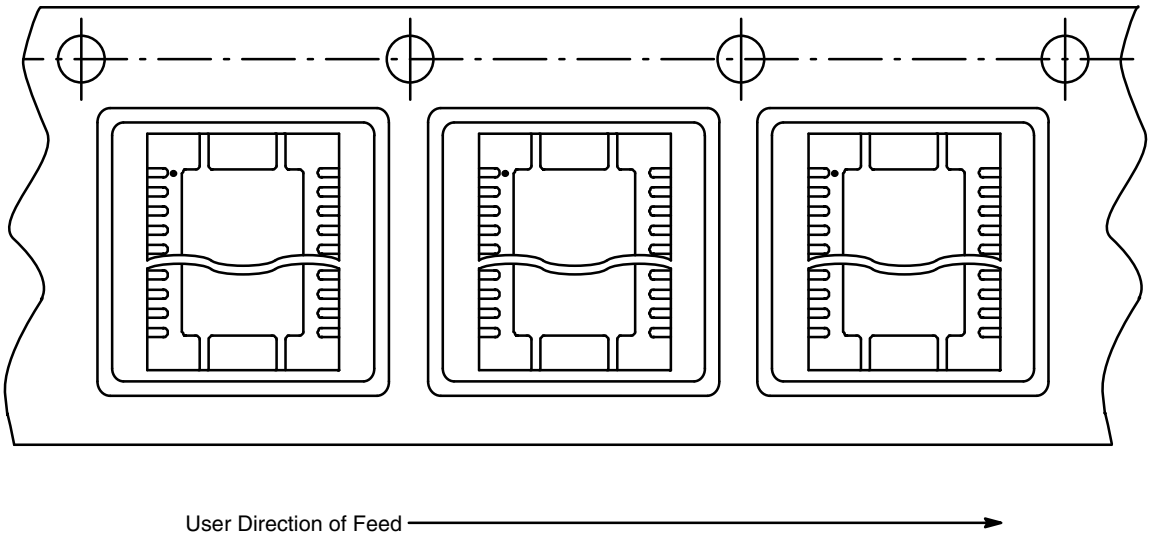
Notes

1. 10 sprocket hole pitch cumulative tolerance ± 0.2 mm.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: black conductive polycarbonate.
4. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
5. All sizes in mm unless specified.

T15-0464-Rev. E, 07-Sep-15
DWG: 93-5260-X

Device Orientation for PowerPAK® MLP65, PowerPAK® MLP55, PowerPAK® MLP55 Double Cooling

DEVICE ORIENTATION	
PACKAGE	**METHOD**
MLP65-20L	T1
MLP55	T1
MLP55 double cooling	T1



Revision control of this drawing is maintained through Document Control, Pack Specification-PACK-0007-19

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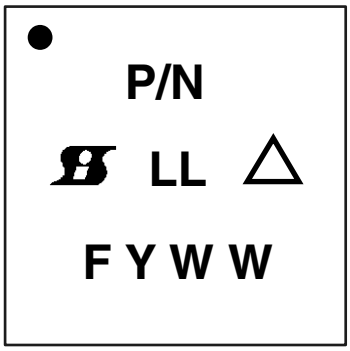
PowerPAK® MLP4535
PowerPAK® MLP55
PowerPAK® MLP66
PowerPAK® MLP77



●	=	Pin 1 Indicator	
P/N	=	Part Number Code	
	=	Siliconix Logo	
△	=	ESD Symbol	
F	=	Assembly Factory Coden	T:TAIWAN assembly
Y	=	Year Code	W:大陸封裝廠
WW	=	Week Code	G:菲律賓封裝廠
LL	=	Lot Code	

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.