

G94-P545-A01 - GDDR3, DVI/VGA + DVI/VGA + HDTV/SDTV-Out

REV	VARIANT	NVPIN	ASSEMBLY
8	BASE	600-10545-5860-100	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10545-9100-100	G94-400 600MHz/1000MHz 512MB 18MAJ2 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out (Bring Up SKU)
2	SKU0000	600-10545-6000-100	G94-400 600MHz/1000MHz 512MB 18MAJ2 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out
3	SKU0010	600-10545-6010-100	G94-300 600MHz/800MHz 512MB 18MAJ2 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out
4	SKU020	600-10545-6020-100	G94-200 600MHz/800MHz 384MB 18MAJ2 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out
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V127-0A Base on P545


- 1.PAGE18: ADD Display port circuit
- 2.PAGE21: ADD GPIO circuit
- 3.PAGE 21: change SPDIF circuit
- 4.PAGE 27: remove PEX\_VDD power switch circuit
- 5.PAGE 27: remove IFP\_PLLVDD/2V5 power switch circuit cahnge APL5713 and APL5910 circuit
- 6.PAGE 28: remove FBVDDQ power switch circuit change APW7067N power circuit
- 7.PAGE 29: remove NVVDD VID circuit
- 8.PAGE 30: change NNVDD POWER APW7088 circuit
- 9.PAGE 16/17 : ADD EMI bridge R
- 10.PAGE 17 CO-LAYOUT HDIM CONNECT
- 11.PAGE 15 remove J1 D\_SUB SLIM CONNECT

V135-0A Base on V127-0A and P545

- 1.Add Page 33,34,35,36 for extend MEM
- 2.Page 3,4 FBCMD7 connect to CS1

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PAGE DETAIL	Overview



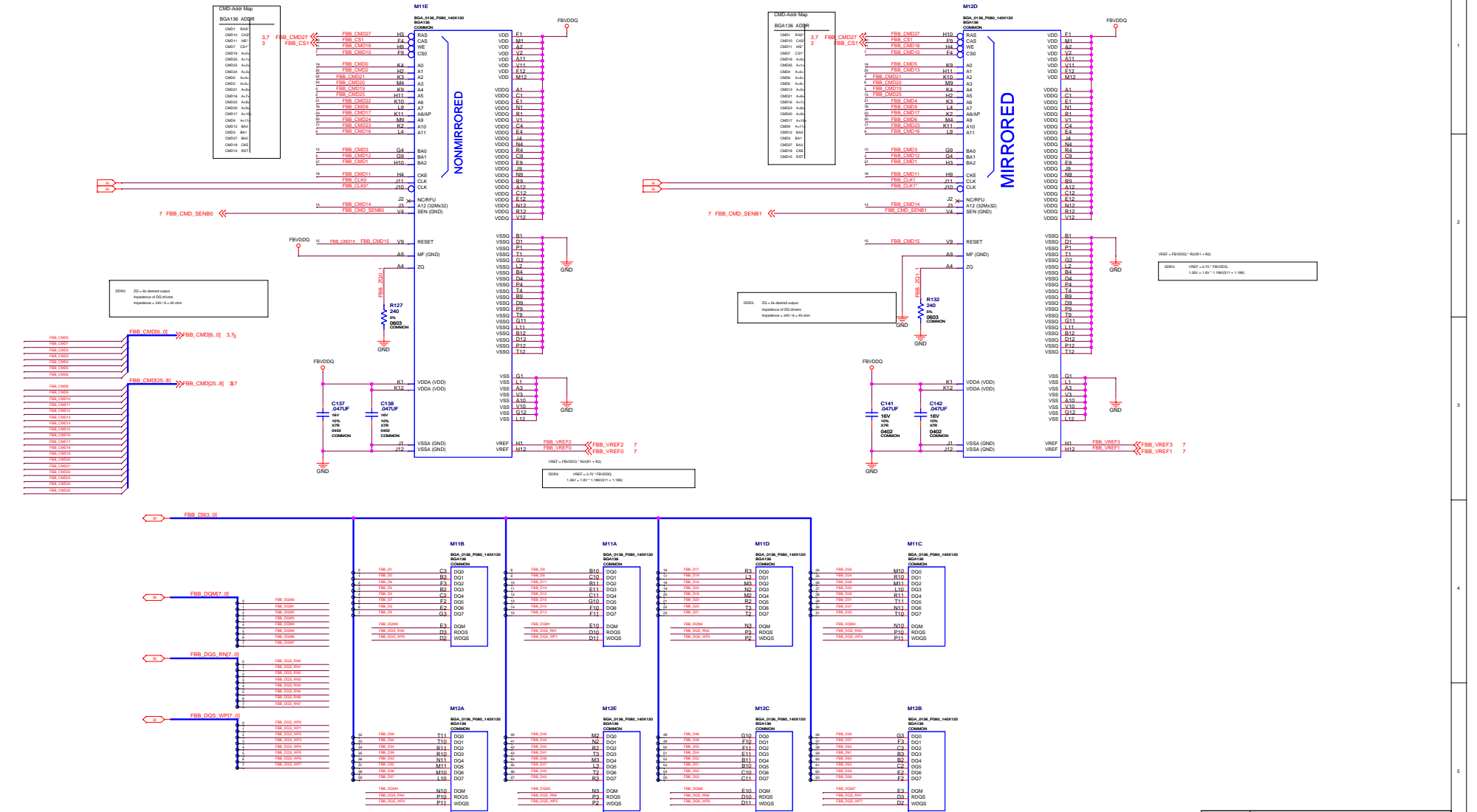
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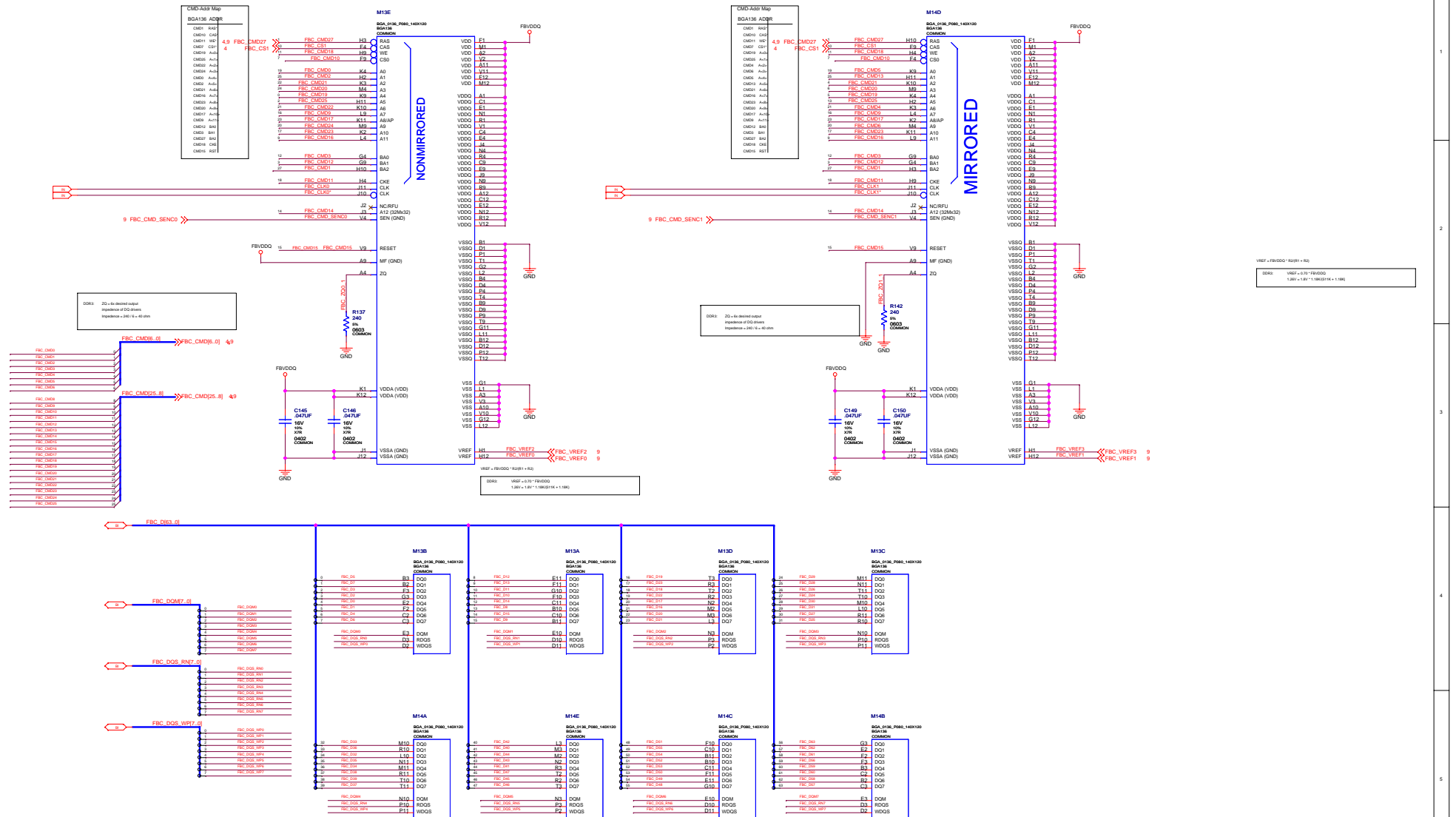
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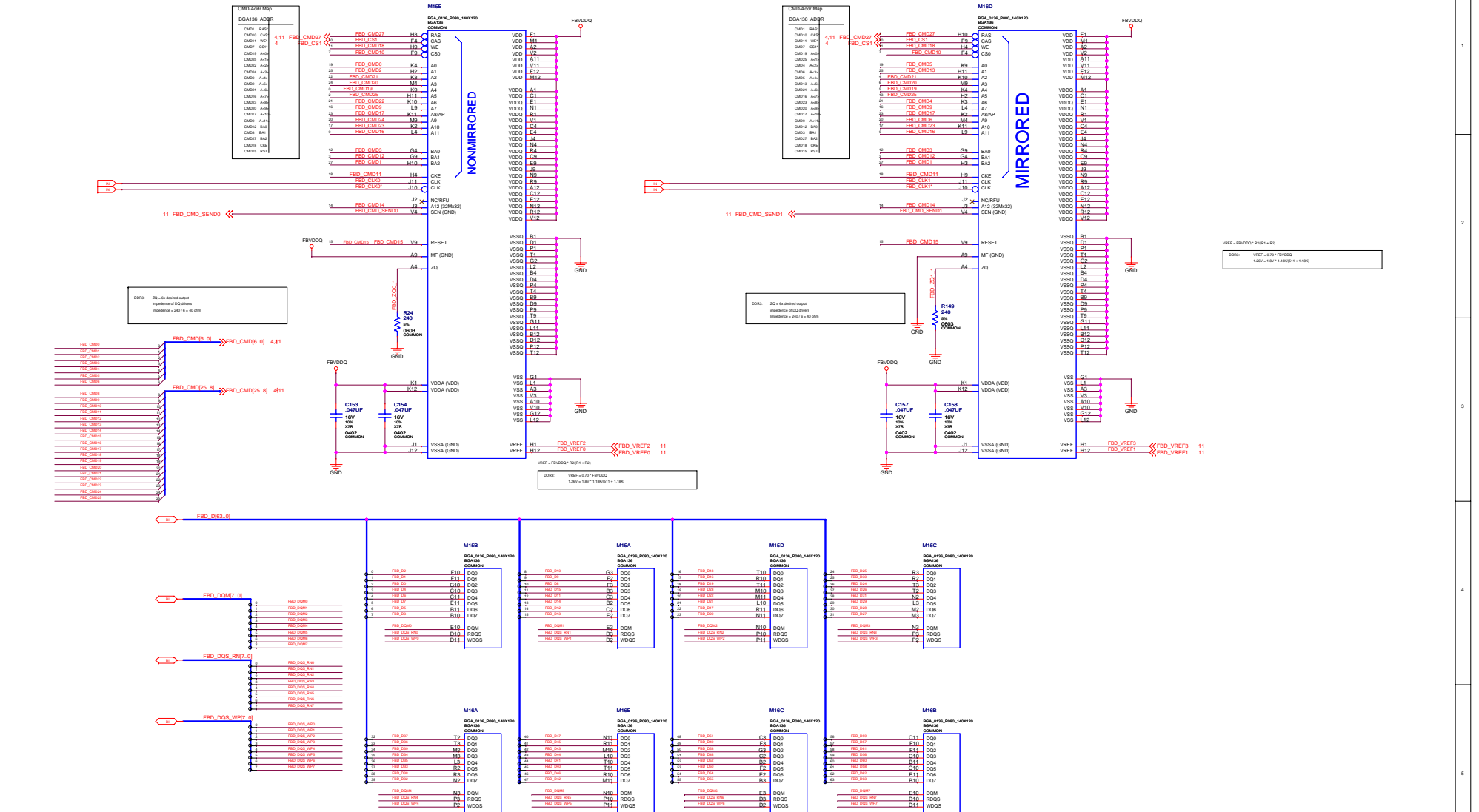
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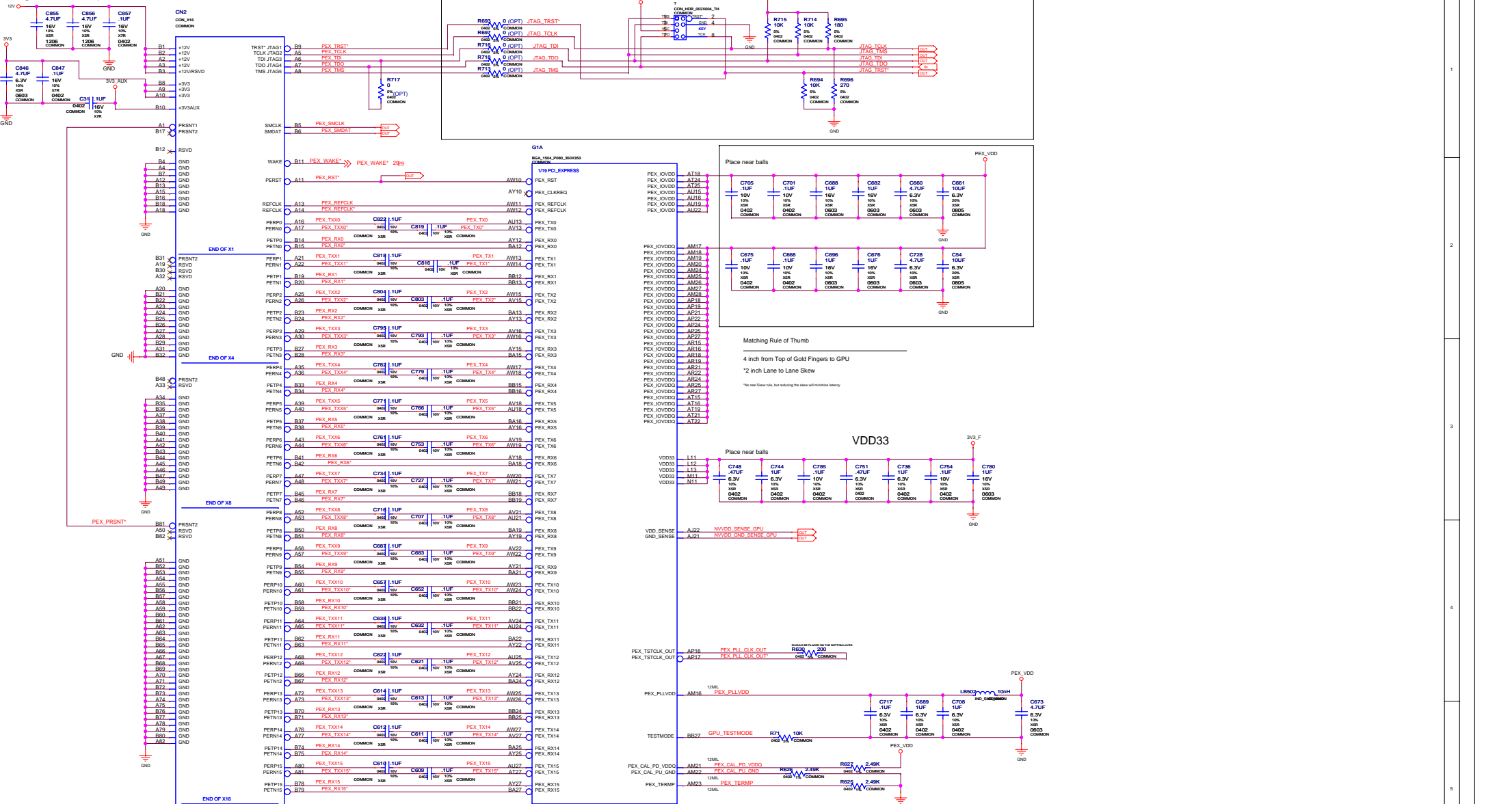
ASSEMBLY	PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC Partition

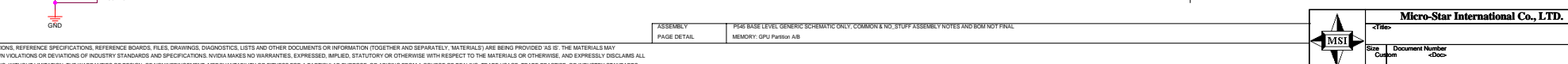


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CALIBRATION PIN	DDR3
FB_CALx_PO_VDDQ	60
FB_CALx_PU_GND	40
FB_CALx_TERM_GND	40
VREF RATIO	0.7 FB/VDDQ



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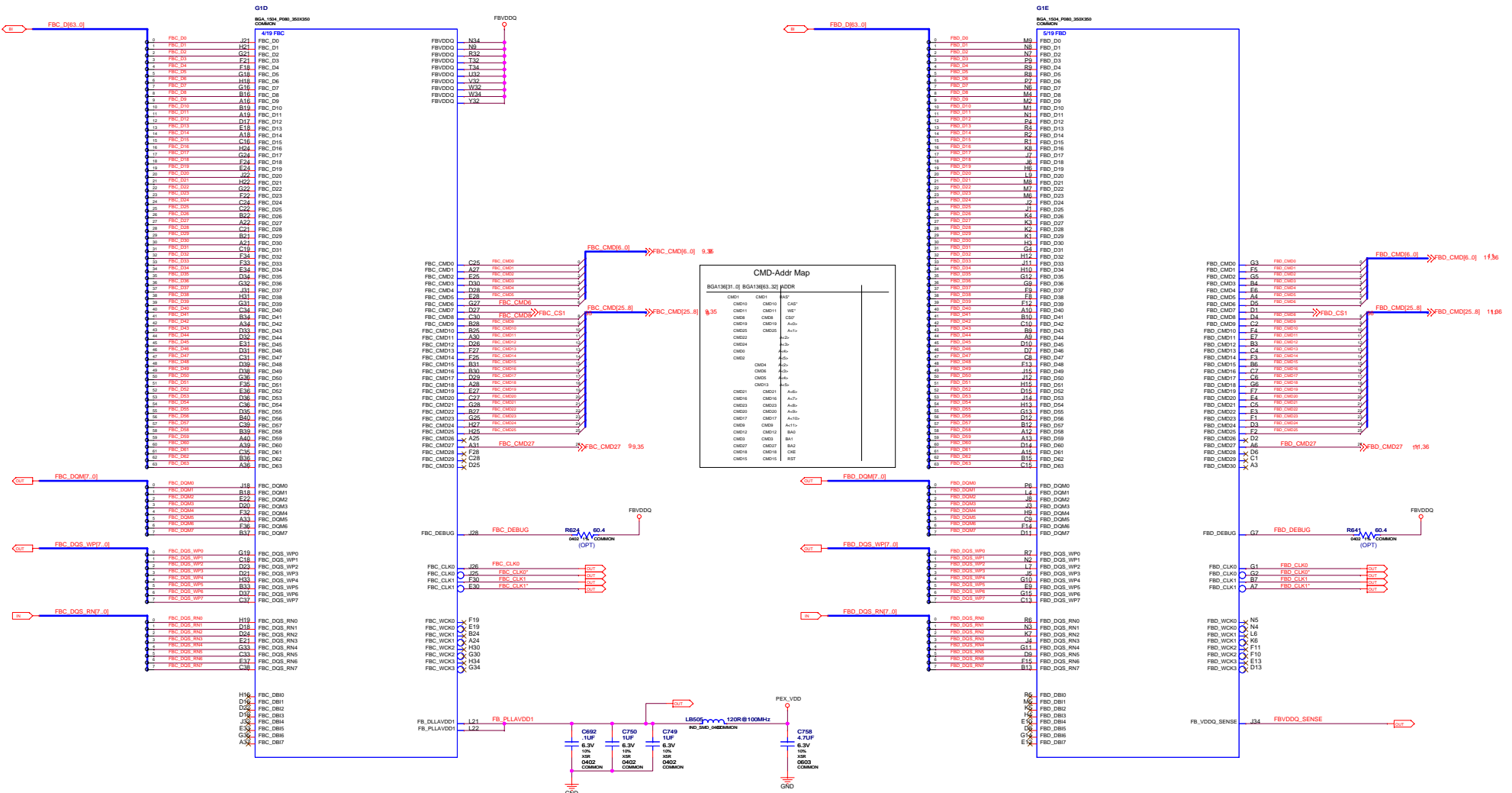
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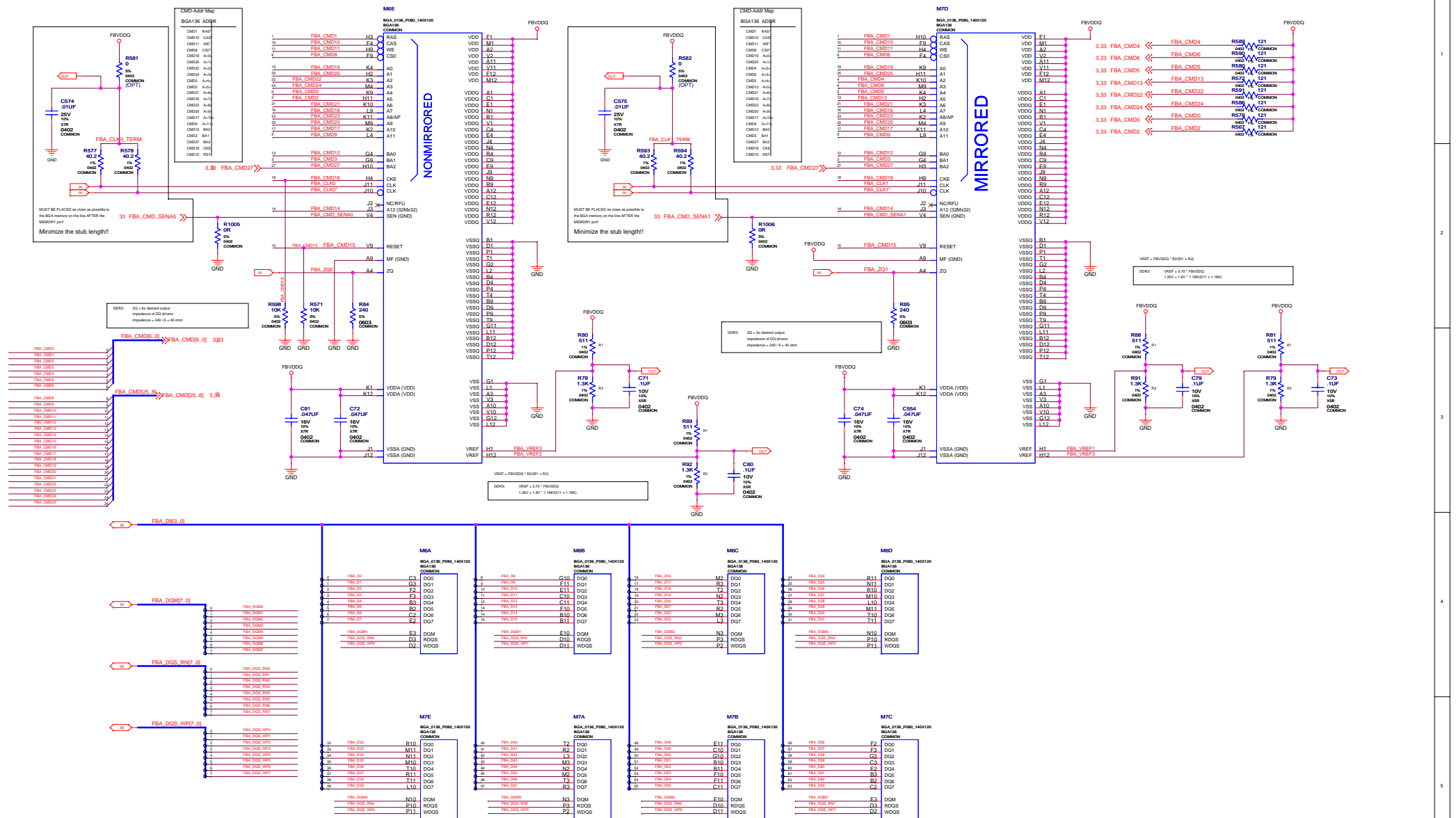
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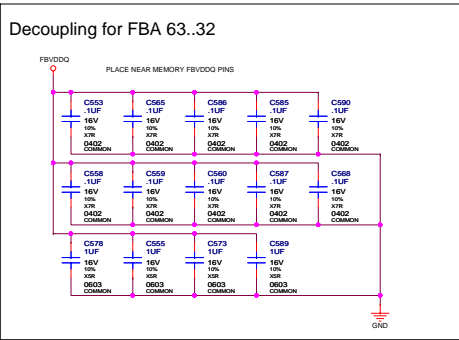
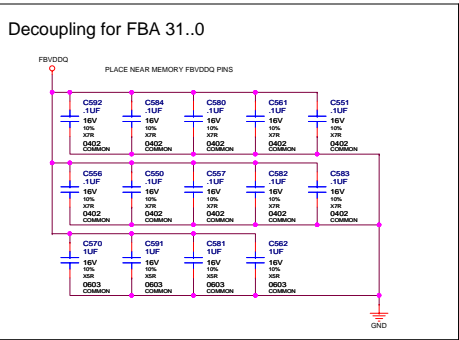




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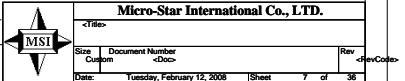
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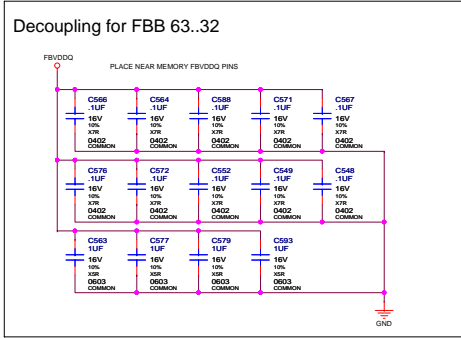
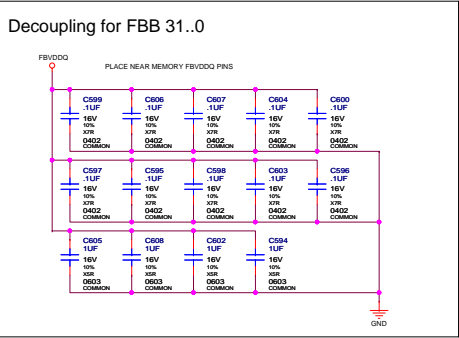
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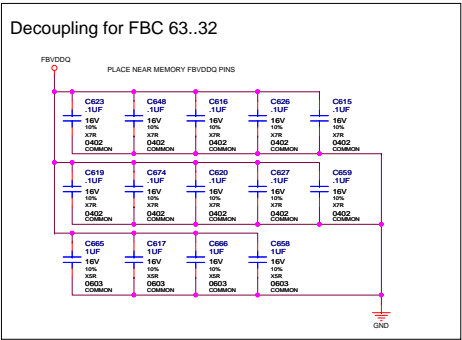
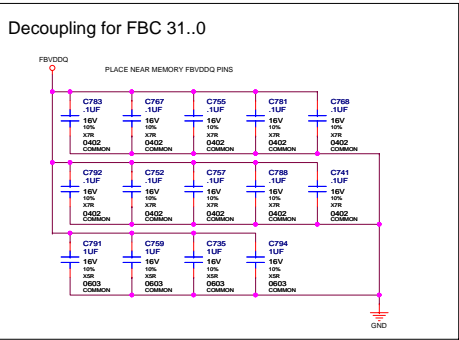
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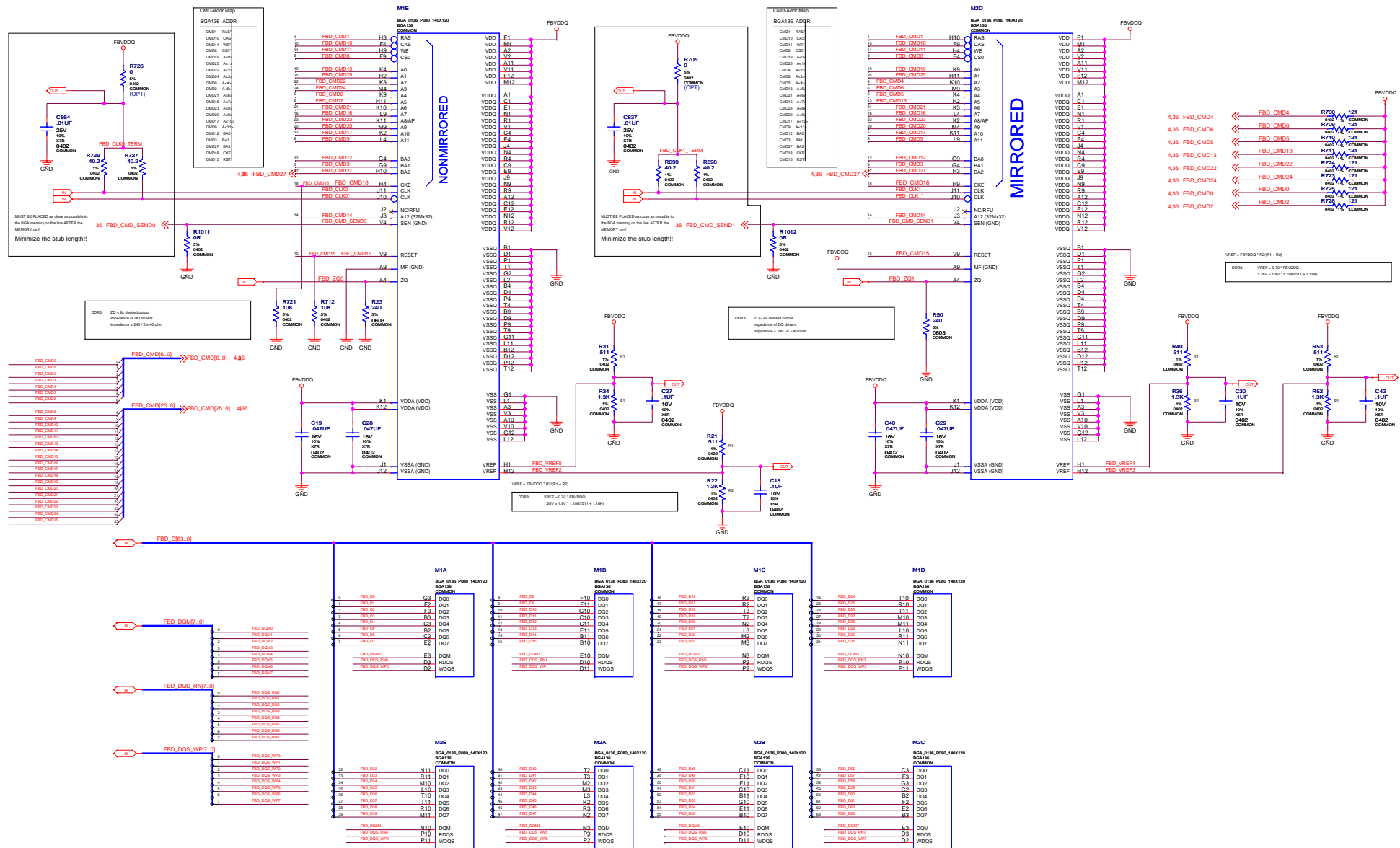
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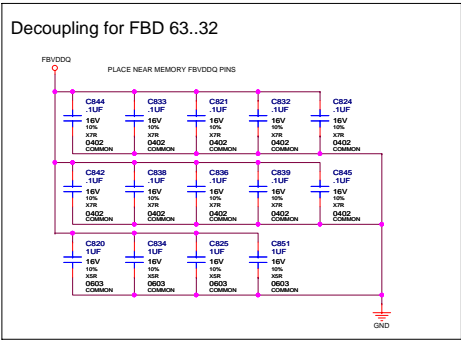
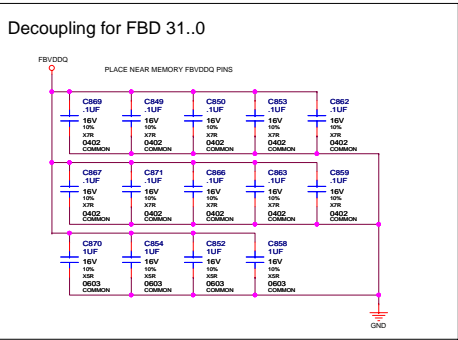
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PER BOARD LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO 3YUPP ASSEMBLY NOTES AND NOT FOR FINAL  
FBC Partition Decoupling



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ASSEMBLY  
PAGE DETAIL

PER BOARD LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO 3V3UPF ASSEMBLY NOTES AND BOARD NOT FINAL

FBD Partition Decoupling



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Document Number <Doc>  
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Rev <Rev Code>



NET		NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
OUT	FBA_CLK0	1	NOFF	FBA_CLK0
OUT	FBA_CLK0*	1	NOFF	FBA_CLK0
OUT	FBA_CLK0_TERM	1	NOBM	
OUT	FBA_CLK1	1	NOFF	FBA_CLK1
OUT	FBA_CLK1*	1	NOFF	FBA_CLK1
OUT	FBA_CLK1_TERM	1	NOBM	

NET	NV_CRITICAL_NET	IMPEDANCE
OUT	FBA_DG5_W9P7_0	1
IN	FBA_DG5_W9P7_0	1
OUT	FBA_DG4P7_0	1
IN	FBA_DG3_0	1

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
OUT FBB_CLK0	1	50OH	FBB_CLK0
OUT FBB_CLK0*	1	50OH	FBB_CLK0
OUT FBB_CLK0_TERM	1	60OH	
OUT FBB_CLK1	1	50OH	FBB_CLK1
OUT FBB_CLK1*	1	50OH	FBB_CLK1
OUT FBB_CLK1_TERM	1	60OH	

	NET	NV_CRITICAL_NET	IMPEDANCE
OUT	FBS_Q05_W0P7_0	1	400M
IN	FBS_Q05_W0P7_0	1	400M
OUT	FBS_Q06P7_0	1	400M
IN	FBS_Q06P7_0	1	400M

	NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
65	FB_PILA000	120%	1.1V	0.00A
66	FB_VREF	120%	1.80V	0.00A
67	FBA_VREF0	120%	1.80V	0.00A
68	FBA_VREF1	120%	1.80V	0.00A
69	FBA_VREF2	120%	1.80V	0.00A
70	FBA_VREF3	120%	1.80V	0.00A
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309	FBA_VREF242	120%	1.80V	0.00A

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
OUT1 → FRC_CLK0	1	NOFF	FRC_CLK0
OUT2 → FRC_CLK0?	1	NOFF	FRC_CLK0
OUT3 → FRC_CLK0_TERM	1	NOIR	
OUT4 → FRC_CLK1	1	NOFF	FRC_CLK1
OUT5 → FRC_CLK1?	1	NOFF	FRC_CLK1
OUT6 → FRC_CLK1_TERM	1	NOIR	

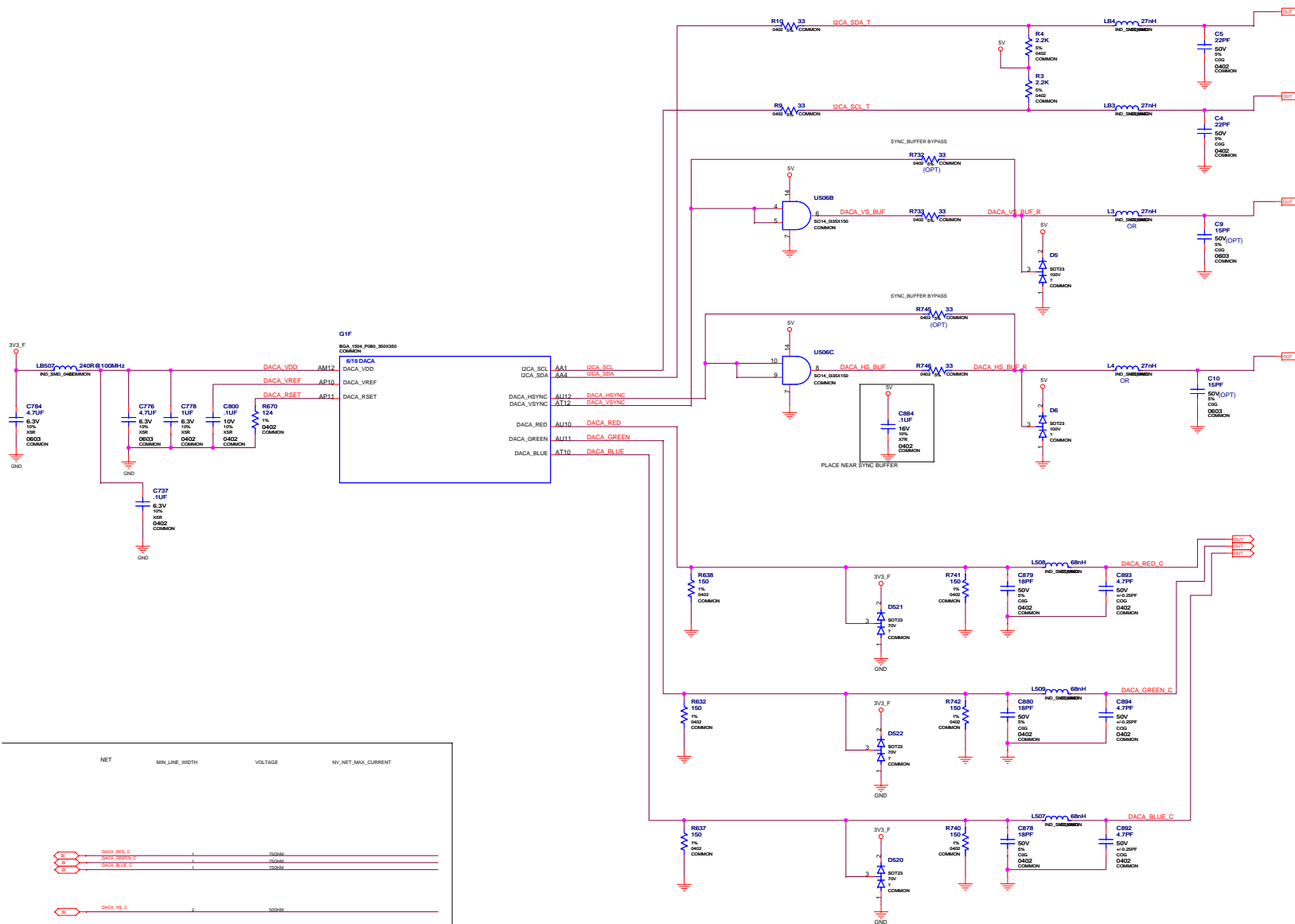
NET	NV_CRITICAL_NET	IMPEDANCE
OUT	FBC_DQ5_WN7_0	1
IN	FBC_DQ5_WN7_0	1
OUT	FBC_DQ67_0	1
IN	FBC_DQ67_0	1
OUT	FBC_DQ83_0	1
IN	FBC_DQ83_0	1

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
OUT1 FBD_CLK0	1	NOFF	FBD_CLK0
OUT2 FBD_CLK0*	1	NOFF	FBD_CLK0
OUT3 FBD_CLK0_TERM	1	GOHM	
OUT1 FBD_CLK1	1	NOFF	FBD_CLK1
OUT2 FBD_CLK1*	1	NOFF	FBD_CLK1
OUT3 FBD_CLK1_TERM	1	GOHM	

NET	NV_CRITICAL_NET	IMPEDANCE
QUT	F8C_DQS_WRPY[0]	1
QUT	F8C_DQS_WRPY[0]	400m
QUT	F8C_DQS_WRPY[0]	1
QUT	F8C_DQS_WRPY[0]	400m
QUT	F8C_DQS_WRPY[0]	1
QUT	F8C_DQS_WRPY[0]	400m
QUT	F8C_DQS_WRPY[0]	1
QUT	F8C_DQS_WRPY[0]	400m

	NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
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10	FPC_Z00	12MIL	1.80V	0.025
10	FPC_Z01	12MIL	1.80V	0.025
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10	FPC_VREF1	12MIL	1.80V	0.025
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10	FPC_VREF3	12MIL	1.80V	0.025
10	FPC_Z00	12MIL	1.80V	0.025
10	FPC_Z01	12MIL	1.80V	0.025

## DACA RGB-FILTER



NET	MIN_LINE_WIDTH	VOLTAGE	IV_NET_MAX_CURRENT
G	DIGITAL_VDD_1C	1	7500mA
B	DIGITAL_VDD_1C	1	7500mA
D	DIGITAL_VDD_1C	1	7500mA
E	DIGITAL_VDD_1C	1	7500mA
B	DIGITAL_VDD_1C	2	5000mA
E	DIGITAL_VDD_1C	2	5000mA

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ASSEMBLY	PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA Interface



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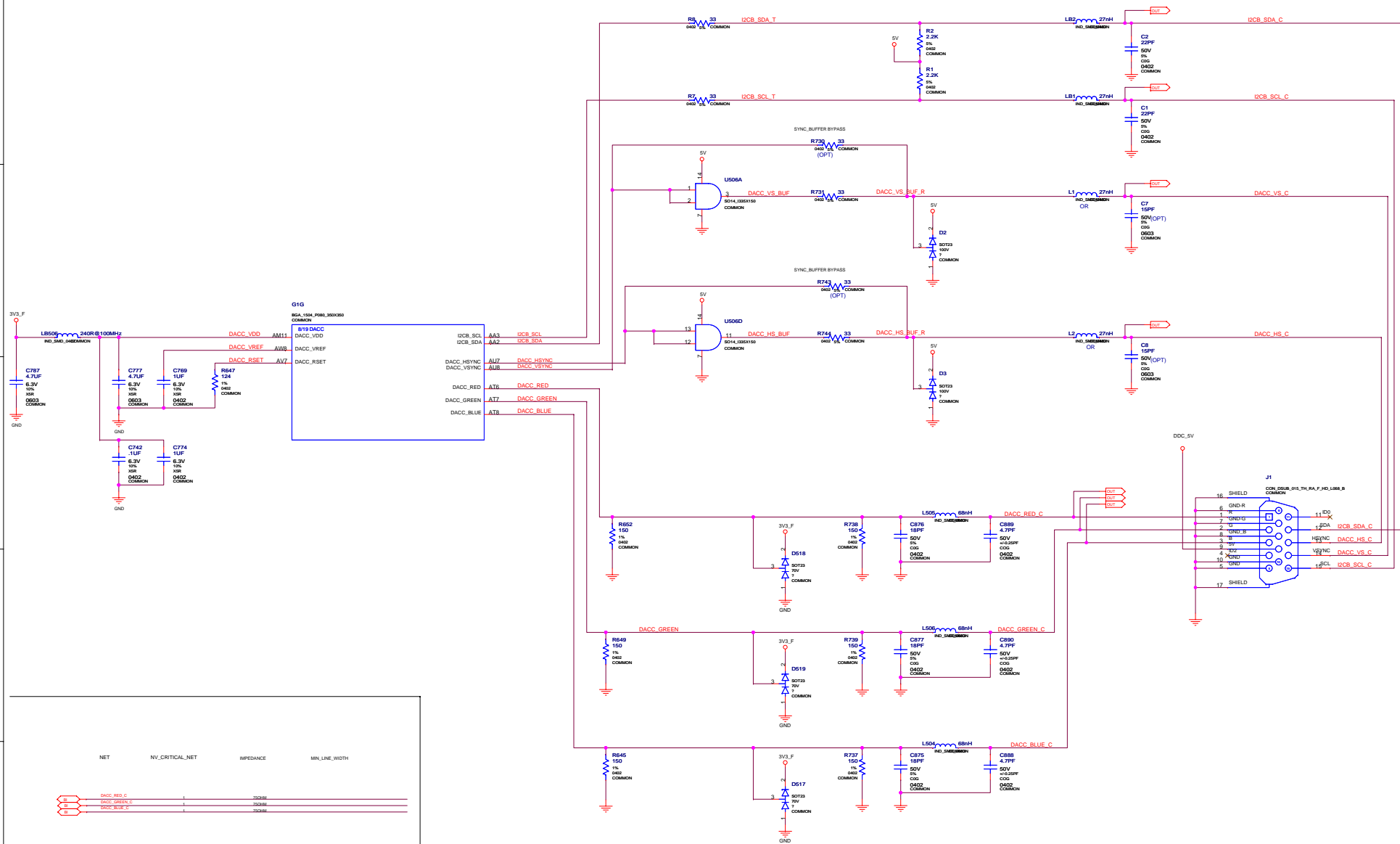
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Rev	Rev Codes
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38	
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# DACC RGB-FILTER



	NET	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
	DAC0_RED_C	1	0000H	
B	DAC0_GREEN_C	1	0000H	
B	DAC0_BLUE_C	1	0000H	
	DAC0_HS_C	2	0000H	
	DAC0_VS_C	2	0000H	

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PAGE DETAIL	DACC Interface



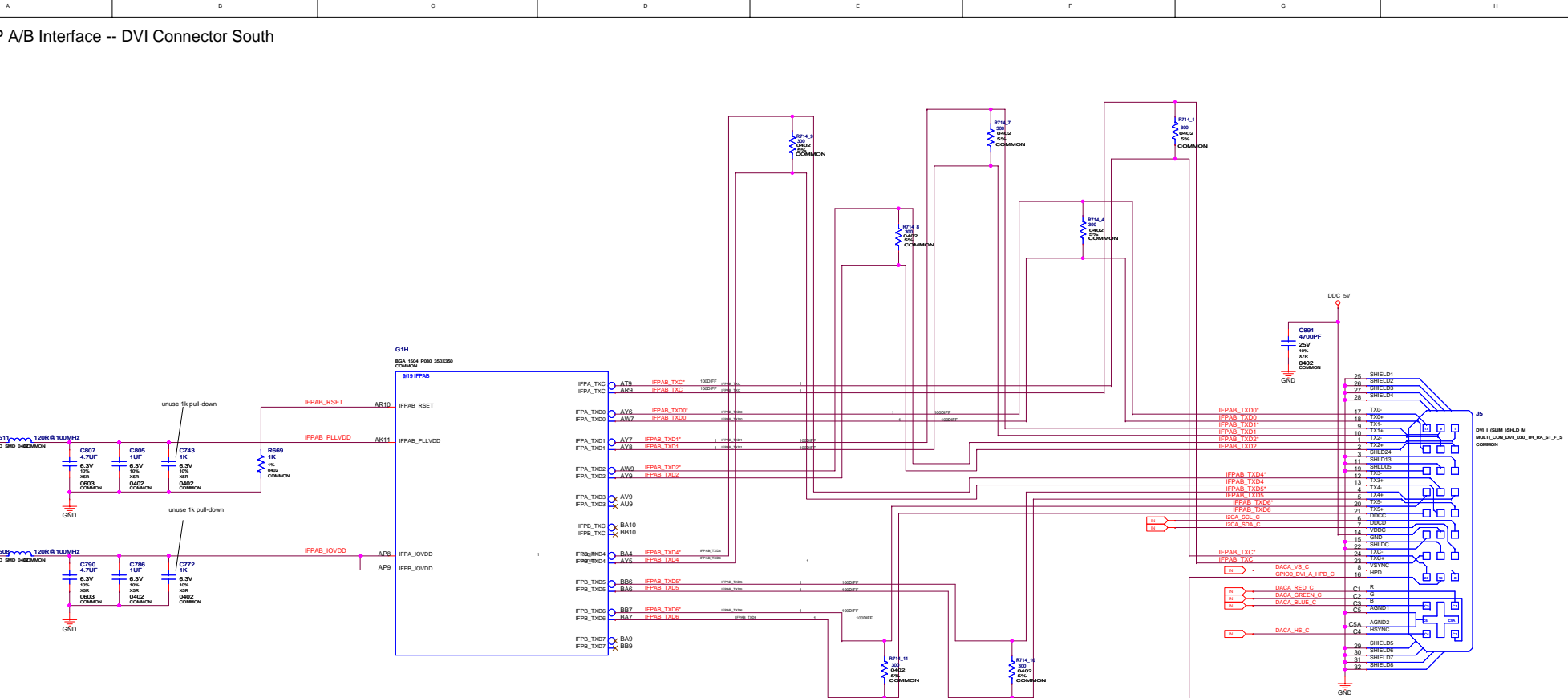
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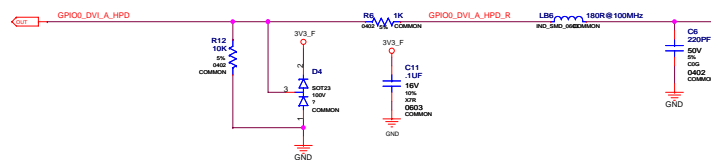


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## DVIAB Hotplug Detection



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PAGE DETAIL	IFP A/B Interface -- DVI Connector South



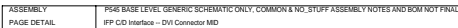
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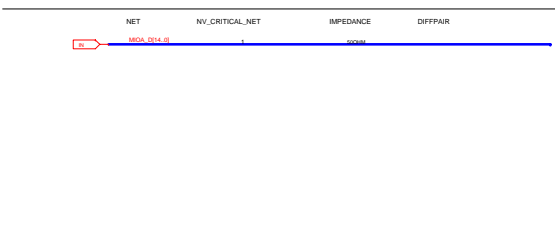
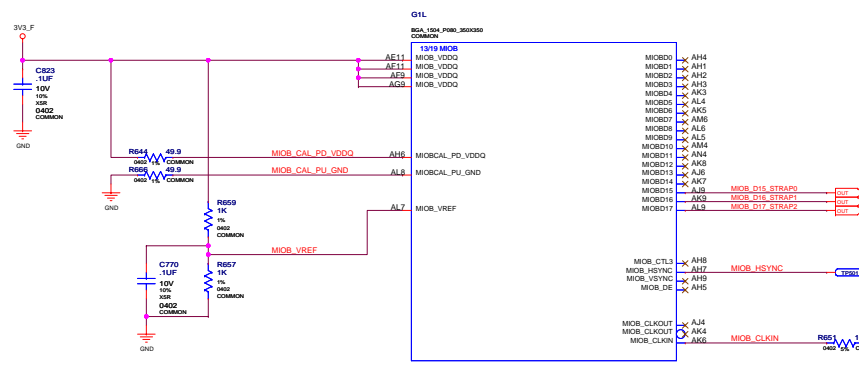
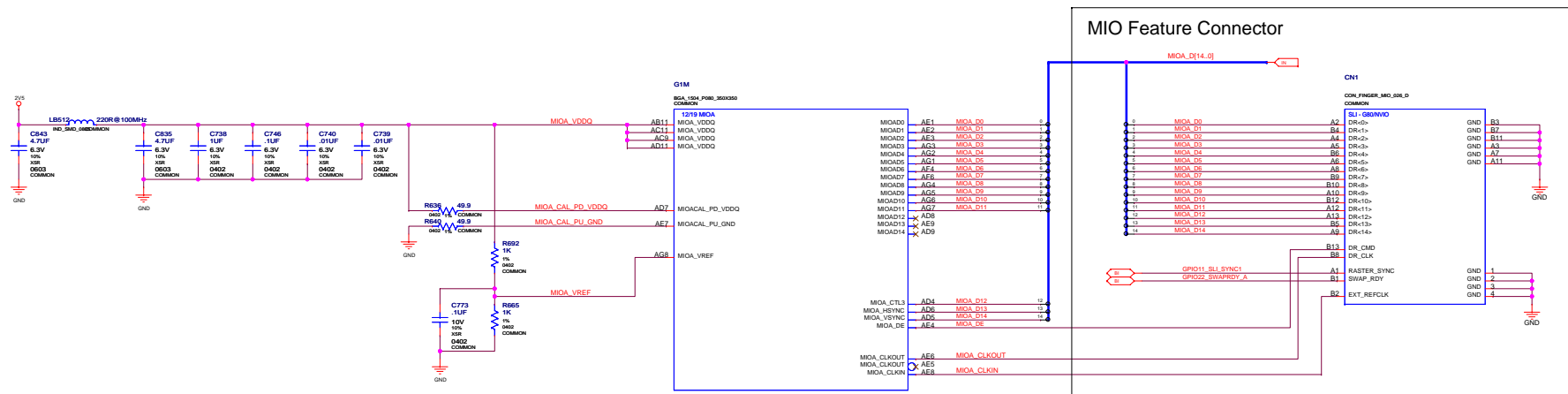
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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIO A/B Interface



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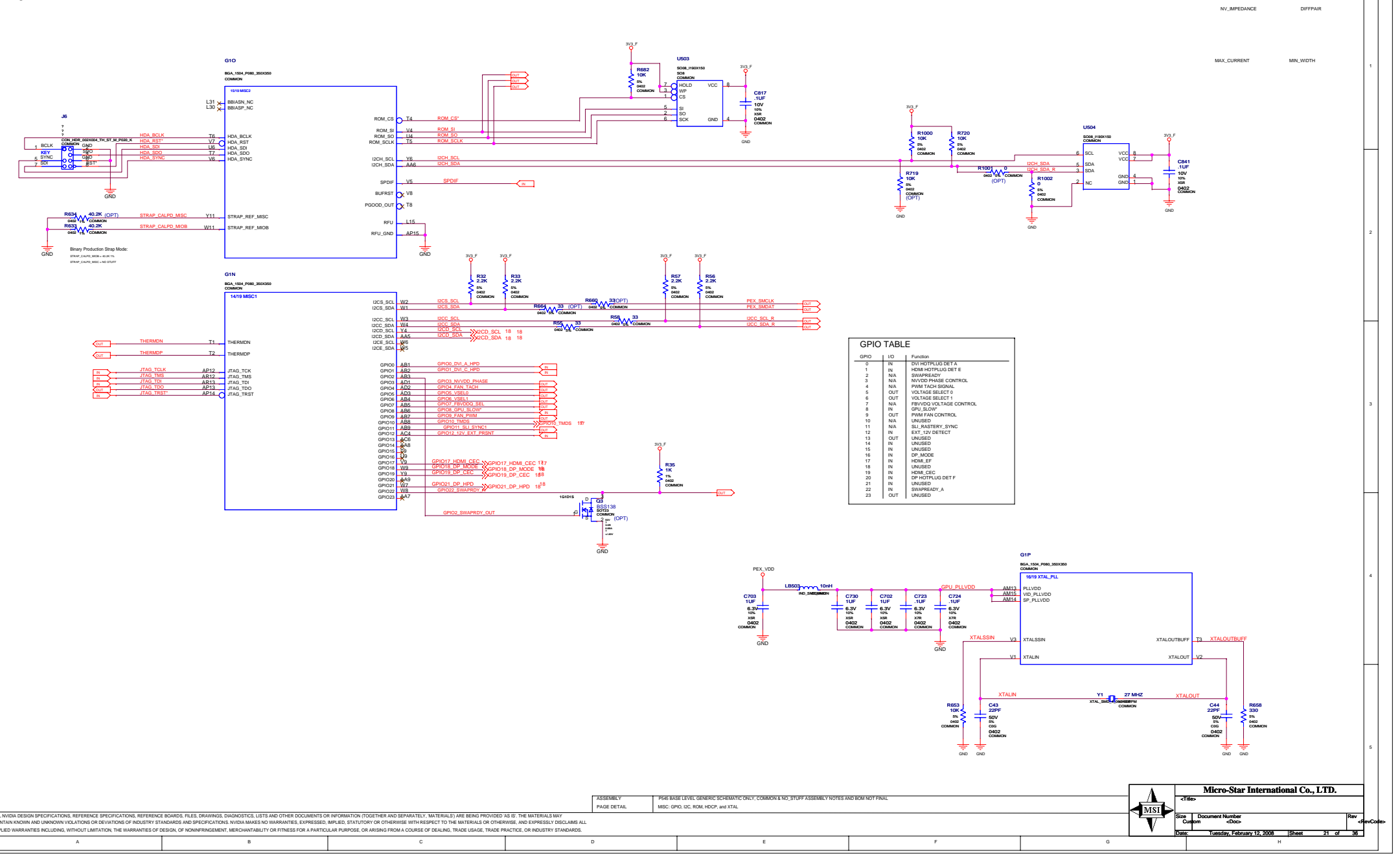
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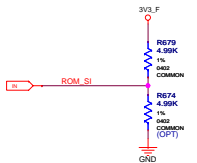




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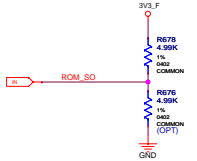
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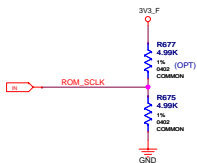


STRAP PIN	STRAP NAME	
ROM_SI	PCI_DEVID_EXT	

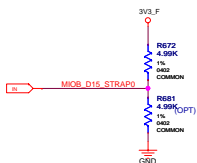
3V3	GND
5K	1   0



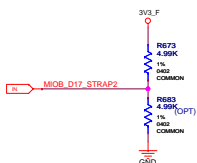
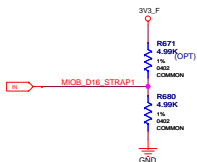
STRAP PIN	STRAP NAME	
ROM_SO	SLOT_CLK_CFG	



STRAP PIN	STRAP NAME	
ROM_SCLK	PCI_DEVID[3]	



STRAP PIN	STRAP NAME	
STRAP0	RAMCFG0	
STRAP1	RAMCFG1	
STRAP2	RAMCFG2	



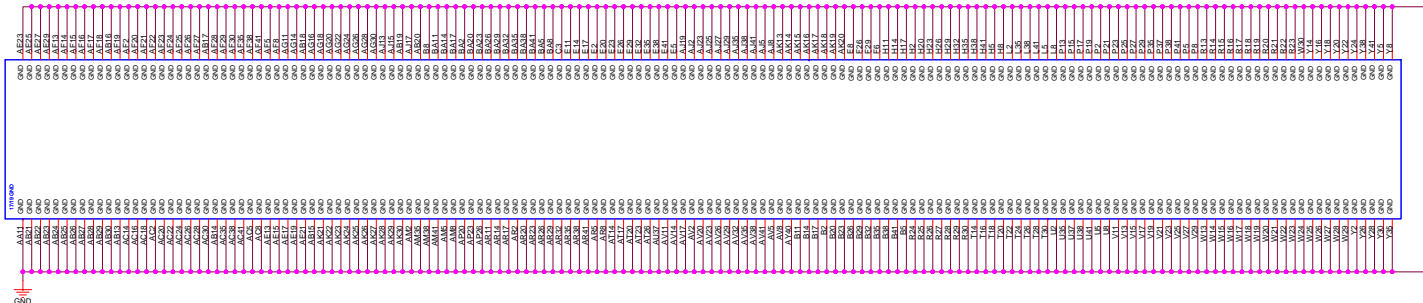
MSI_150A_P160_350035	COMMON
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ACM4	NC
ACM5	NC
ACM6	NC
AF34	NC
AF35	NC
AF36	NC
AF37	NC
AG34	NC
AG35	NC
AG36	NC
AG37	NC
AL34	NC
AL35	NC
AL36	NC
AM34	NC
AM35	NC
AM36	NC
AM37	NC
AP34	NC
AP35	NC
AT34	NC
AT35	NC
AU34	NC
AU35	NC
AU36	NC
AV34	NC
AV35	NC
AV36	NC
AV37	NC
ED34	NC
ED35	NC
ED36	NC
ED37	NC
FG34	NC
FG35	NC
FG36	NC
FG37	NC
GI34	NC
GI35	NC
GI36	NC
GI37	NC
HO34	NC
HO35	NC
HO36	NC
HO37	NC
LI34	NC
LI35	NC
LI36	NC
LI37	NC
MI34	NC
MI35	NC
MI36	NC
MI37	NC
PI34	NC
PI35	NC
PI36	NC
PI37	NC
TI34	NC
TI35	NC
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UI36	NC
UI37	NC
VI34	NC
VI35	NC
VI36	NC
VI37	NC

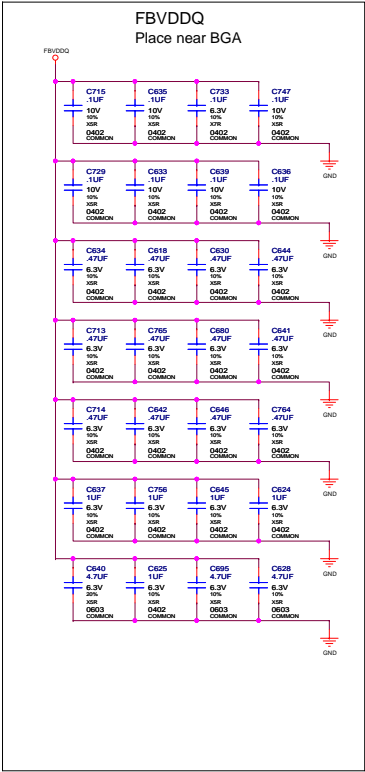
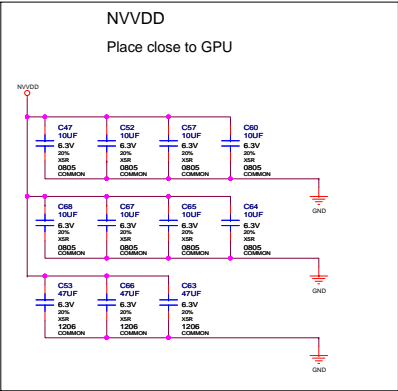
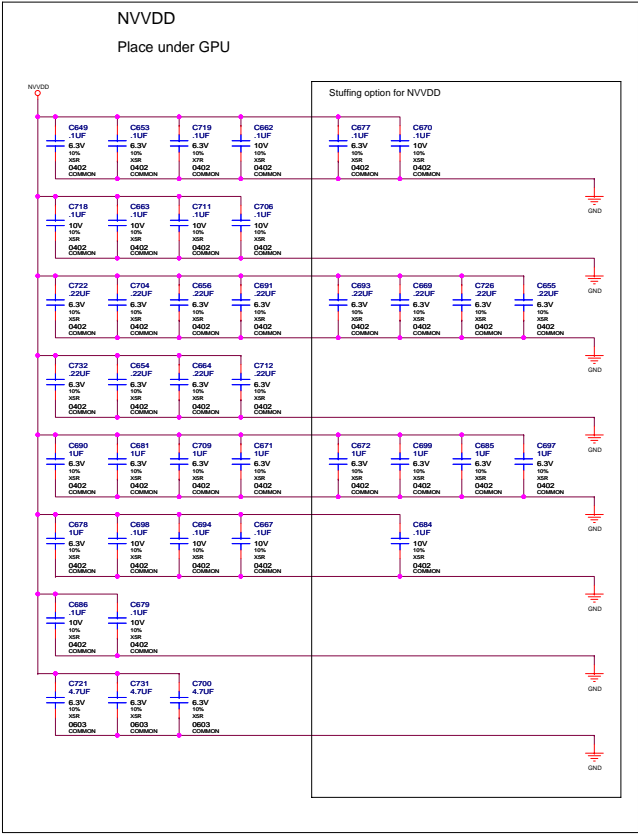
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ASSEMBLY	PER BOARD LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO 3Y/5Y ASSEMBLY NOTES AND BOARD NOT FINAL
PAGE DETAIL	Strap Configuration



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Date:	Tuesday, February 12, 2008	Sheet	22 of 38





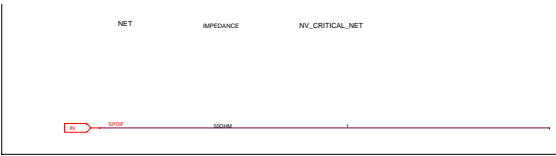
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ASSEMBLY PAGE DETAIL PCB LAYER LEVEL: GENERIC SCHEMATIC ONLY; COMMON & NO. 3(CPU) ASSEMBLY NOTES AND BOARD FINAL NVVDD and FBVDDQ Decoupling

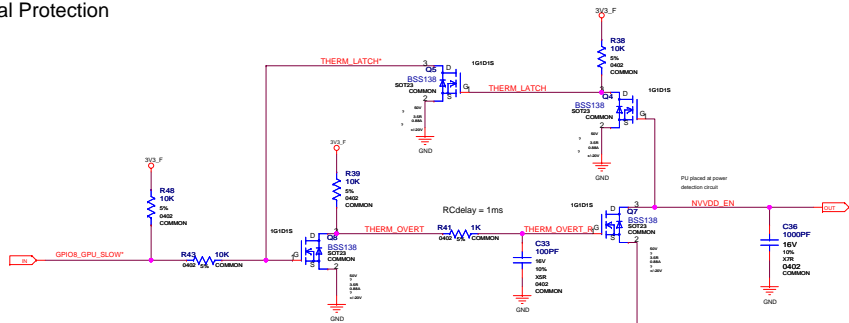


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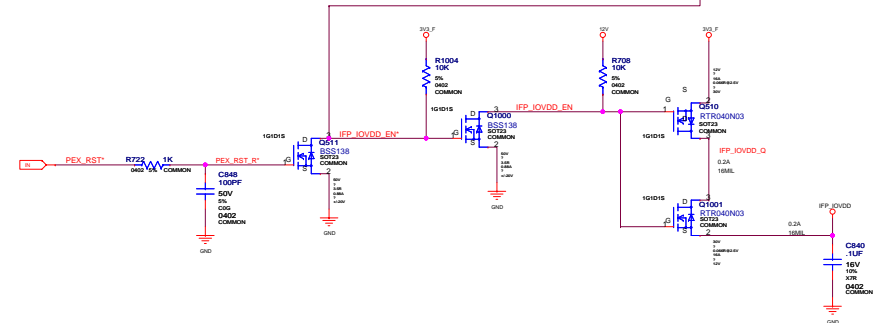


## Thermal Protection

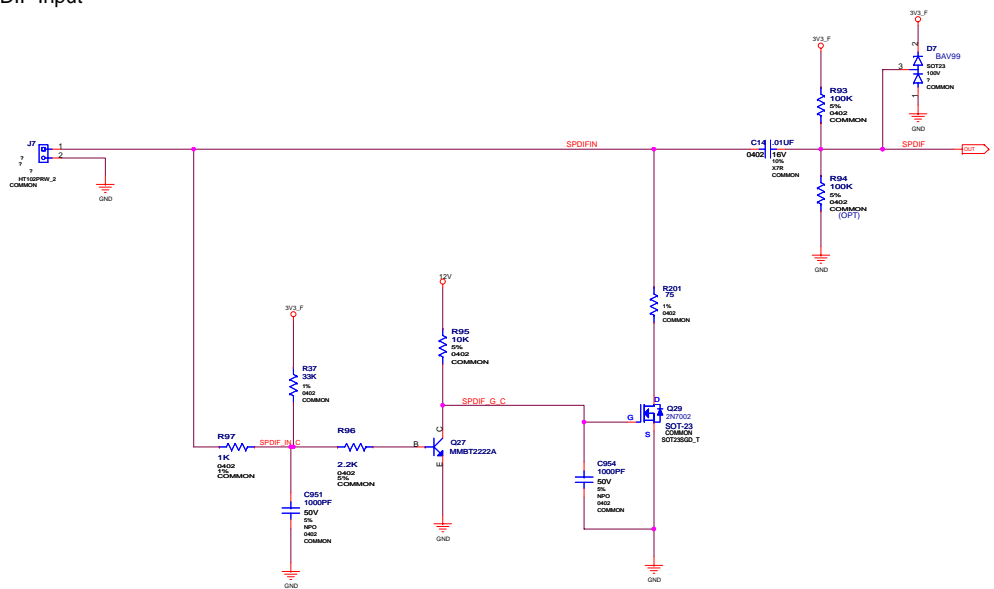


## IFP\_IOVDD Backdrive Prevention

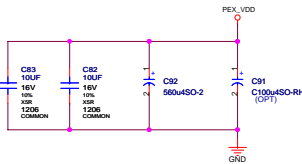
#### Stuffing possibilities for thermal control and protection:



## SPDIF Input



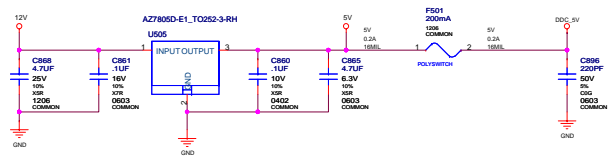




## 5V and DDC\_5V Power Supply

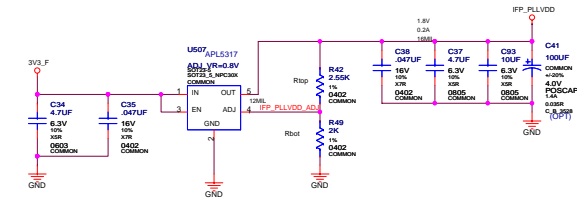
DDC\_5V = 5V @ 200mA

**LAYOUT NOTE:** ADD MIN 200MM<sup>2</sup> COPPER AROUND THIS DPAK FOR HEAT DISSIPATION



## IFP\_PLLVDD Power Supply

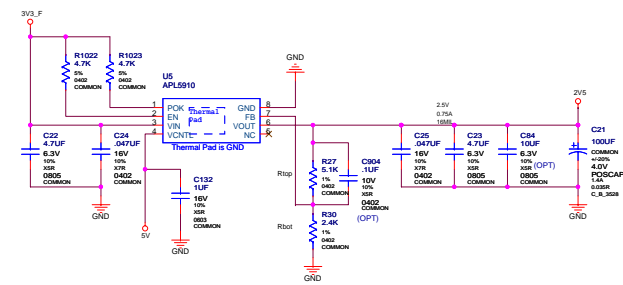
IFP\_PLLVDD = 1.8V @ 200mA



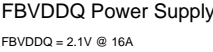
$$\text{IFP\_PLLVD D} = \text{VREF} * (1 + (\text{Rtop} / \text{Rbot}))$$

$$1.82\text{V} = 0.8\text{V} * (1 + (2.5\text{K}/2\text{K}))$$

## 2V5 Power Supply

$$2V5 = 2.5V @ 750mA$$


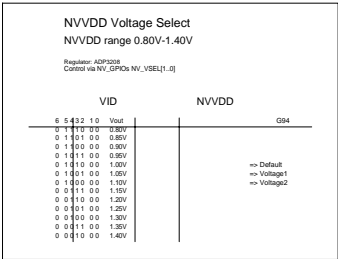
$$2V5 = V_{REF} * (1 + (R_{top} / R_{bot}))$$
$$2.5V = 0.8V * (1 + (5.1K/2.4K))$$

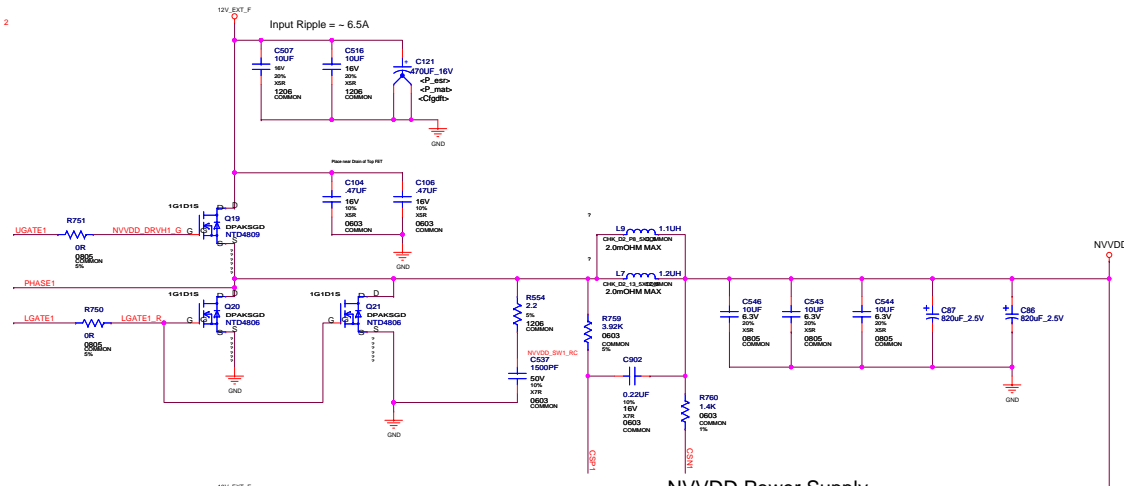


	GPIO7
FBVDDQ = 1.792V	0
FBVDDQ = 1.999V	1

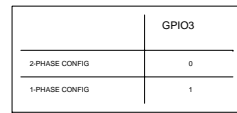
$$\begin{aligned} \text{FBVDDQ} &= \text{VREF} * (1 + (\text{Rtop} / \text{Rbot1})) \\ 1.82\text{V} &= 0.8 * (1 + (2.55\text{K} / 2\text{K})) \\ \text{FBVDDQ} &= \text{VREF} * (1 + (\text{Rtop} / (\text{Rbot1} // \text{Rbot2}))) \\ 2.02\text{V} &= 0.8 * (1 + (2.55\text{K} / (2\text{K} // 10\text{K}))) \\ \text{FBVDD} &= 0.8\text{V} * (1 + (1.3\text{K} / (1.1\text{K} // 10\text{K})) = 1.84\text{V} \\ \text{FBVDD} &= 0.8\text{V} * (1 + 1.3\text{K} / 1.1\text{K}) = 1.745\text{V} \end{aligned}$$







### NVVDD Power Supply

[illegible]

	GPIQ3
2-PHASE CONFIG	0
1-PHASE CONFIG	1

ASSEMBLY	PS46 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS V: NVVDD Power Supply



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The schematic diagram illustrates the electrical connections for the ADMP3074 module. It features three main sections: I2C, THERM, and FAN.

- I2C Section:** The module's I2C pins (SCL, SDA, D+, D-) are connected to a 10kΩ pull-up resistor (R46) and a 100pF capacitor (C46) to VCC. The I2C address pin (A0) is connected to a 10kΩ pull-up resistor (R47) to VCC.
- THERM Section:** The module's THERM pins (THERMOP, THERMON, THERMID) are connected to a 10kΩ pull-up resistor (R48) and a 100pF capacitor (C48) to VCC. The THERMID pin is also connected to a 10kΩ pull-up resistor (R49) to VCC.
- FAN Section:** The module's FAN pins (FANP, FANM, FANS) are connected to a 10kΩ pull-up resistor (R50) and a 100pF capacitor (C50) to VCC. The FANM pin is also connected to a 10kΩ pull-up resistor (R51) to VCC.

The module is powered by a 3.3V supply (VCC) and ground (GND). The module's pins are labeled with their respective functions and pin numbers.

ASSEMBLY	PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Diode and Fan Control



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Date:	Tuesday, February 12, 2008	Sheet	31	of	36
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Rev. 04/2010

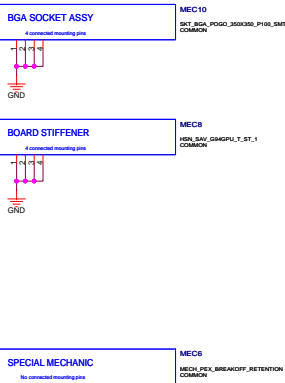
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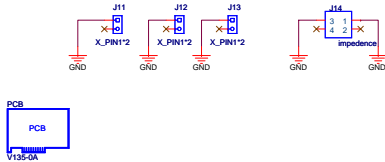
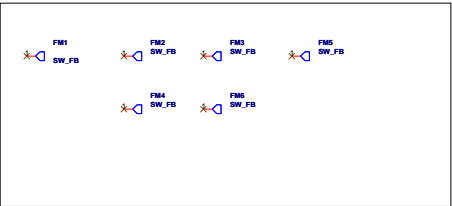
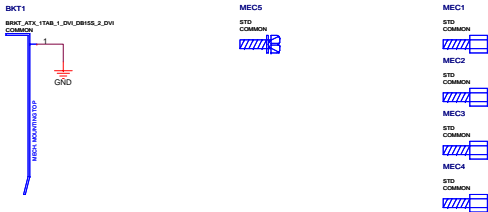
Thermal



Mechanical



Bracket



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ASSEMBLY  
PAGE DETAIL  
PCB/BOARD LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO 3D/CAD ASSEMBLY NOTES AND NOT FOR FINAL  
Thermal, Mechanical, and Bracket

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Size Custom	Document Number <Doc>
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