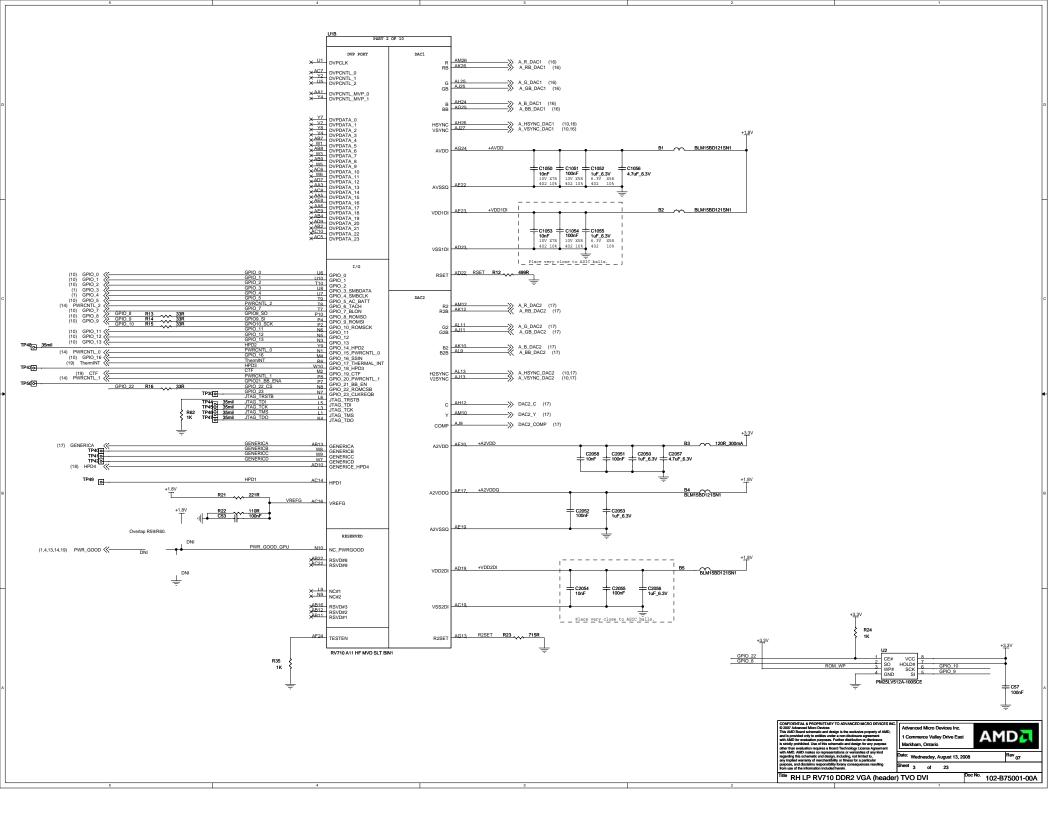


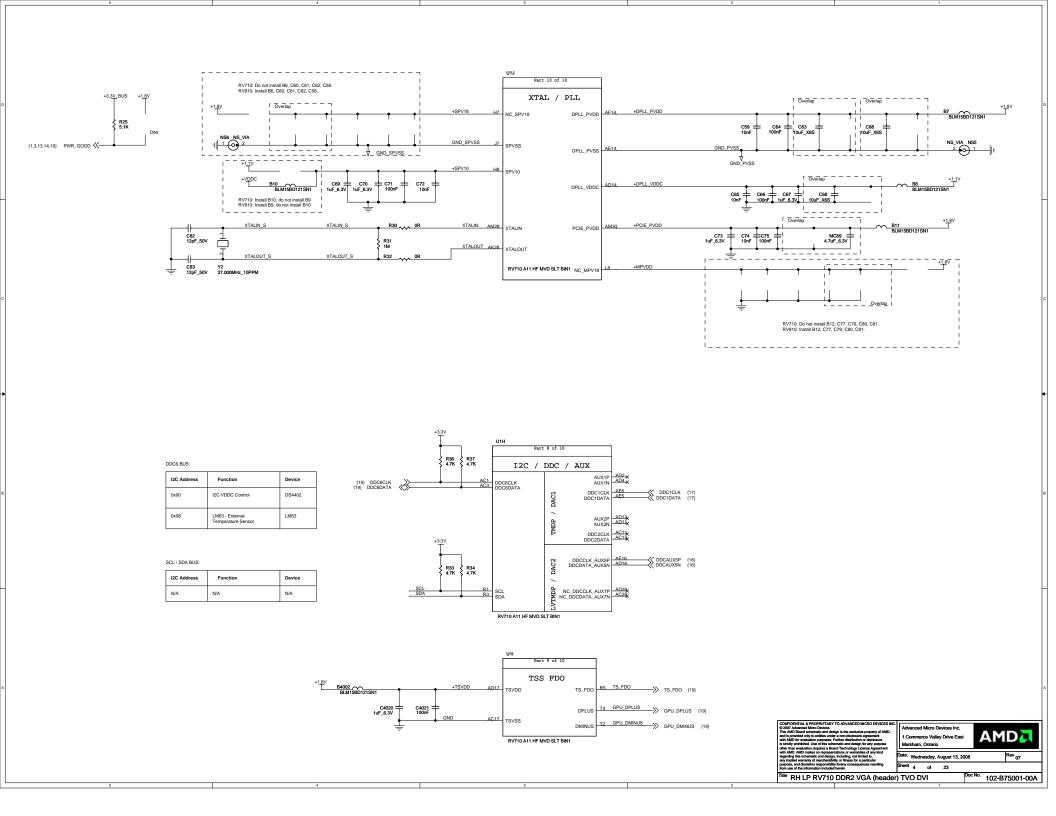
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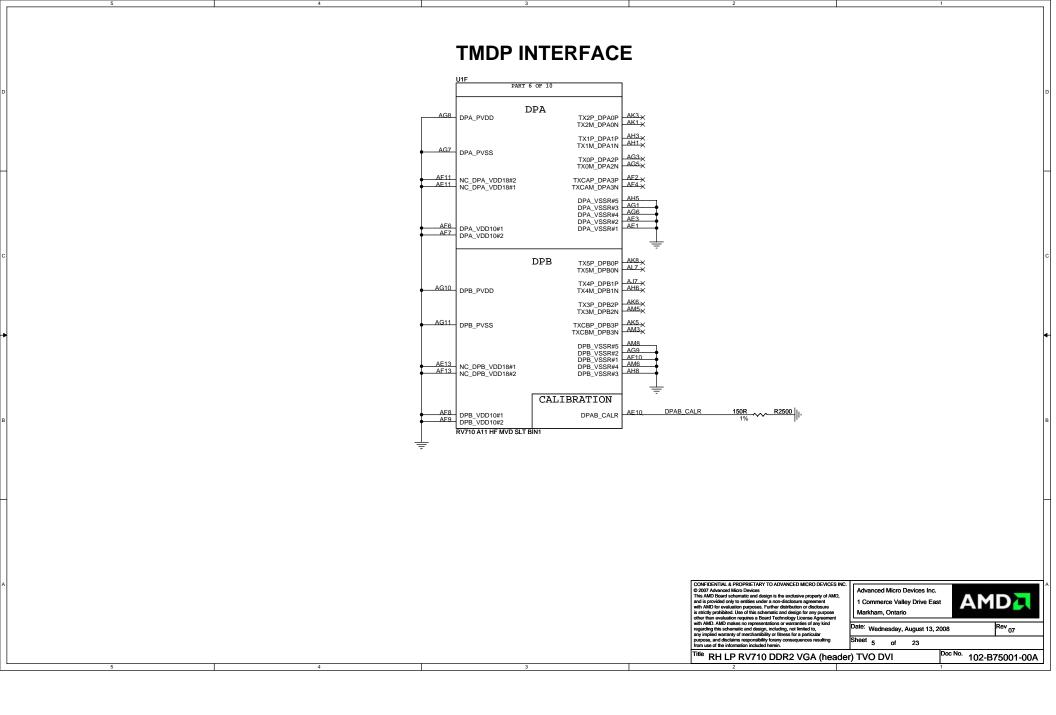
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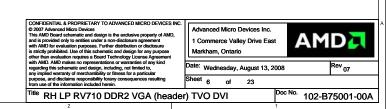
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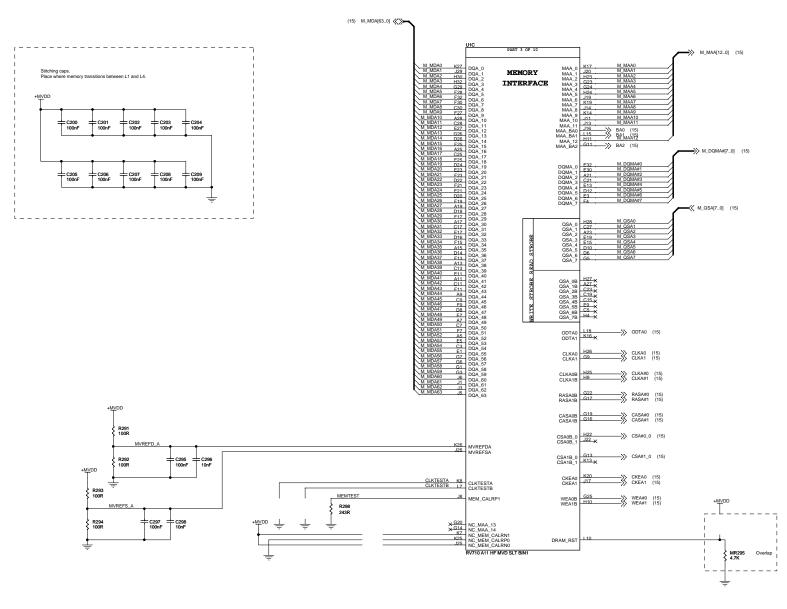




#### LVTMDP INTERFACE U1G Part 7 of 10 DPF RSVD#6 RSVD#4 AK24 AJ23 AG19 NC\_DPF\_PVDD T2X5P\_DPF0P AL 23 T2X5M\_DPF0N AK22 T2X5P (18) T2X5M (18) T2X4P\_DPF1P AH22 T2X4M\_DPF1N AJ21 NC\_DPF\_PVSS T2X4P (18) T2X4M (18) T2X3P (18) T2X3M (18) T2X3P\_DPF2P AL21 T2X3M\_DPF2N AK20 AG17 DPF\_VDD18#2 DPF\_VDD18#1 T2XCFP\_DPF3P AH20x T2XCFM\_DPF3N AJ19x DPF\_VSSR#4 DPF\_VSSR#5 DPF\_VSSR#2 DPF\_VSSR#1 DPF\_VSSR#3 AM20 DPF\_VDD10#2 DPF\_VDD10#1 DPE RSVD#7 Al 19 RSVD#5 AK18 T2X2P\_DPE0P AH18 T2X2M\_DPE0N AJ17 T2X2P (18) T2X2M (18) +1.8V T2X1P\_DPE1P AL17 T2X1M\_DPE1N AK16 B1500 \_\_\_\_ BLM15BD121SN1 DPE\_PVDD AG18 DPE\_PVDD T2X1P (18) T2X1M (18) C1501 1uF\_6.3V C1500 4.7uF\_6.3V C1509= C1502 T2X0P\_DPE2P AH16\_ T2X0M\_DPE2N AJ15\_ 1uF\_6.3V T2X0P (18) T2X0M (18) AF19 DPE\_PVSS T2XCEP\_DPE3P AL15 T2XCEM\_DPE3N AK14 T2XCEP (18) T2XCEM (18) +<u>1.8</u>V DPE\_VSSR#3 DPE\_VSSR#2 DPE\_VSSR#1 DPE\_VSSR#1 DPE\_VSSR#4 AG16 DPE\_VDD18#2 DPE\_VDD18#1 B1501 \_\_\_\_ BLM15BD121SN1 +DPE\_VDD18 C1504 1uF\_6.3V C1505 C1503 C1510= 4.7uF\_6.3V 1uF\_6.3V AM18 DPE\_VSSR#5 +1<u>.1</u>V CALIBRATION AG21 DPE\_VDD10#2 DPE\_VDD10#1 150R ~ R1500 B1502 ~ 30R\_1A +DPE\_VDD10 AF17 DPEF\_CALR DPEF CALR RV710 A11 HF MVD SLT BIN1 C1511 C1506 C1508 100nF C1507 1uF\_6.3V 4.7uF\_6.3V 1uF\_6.3V



## **MEMORY INTERFACE**

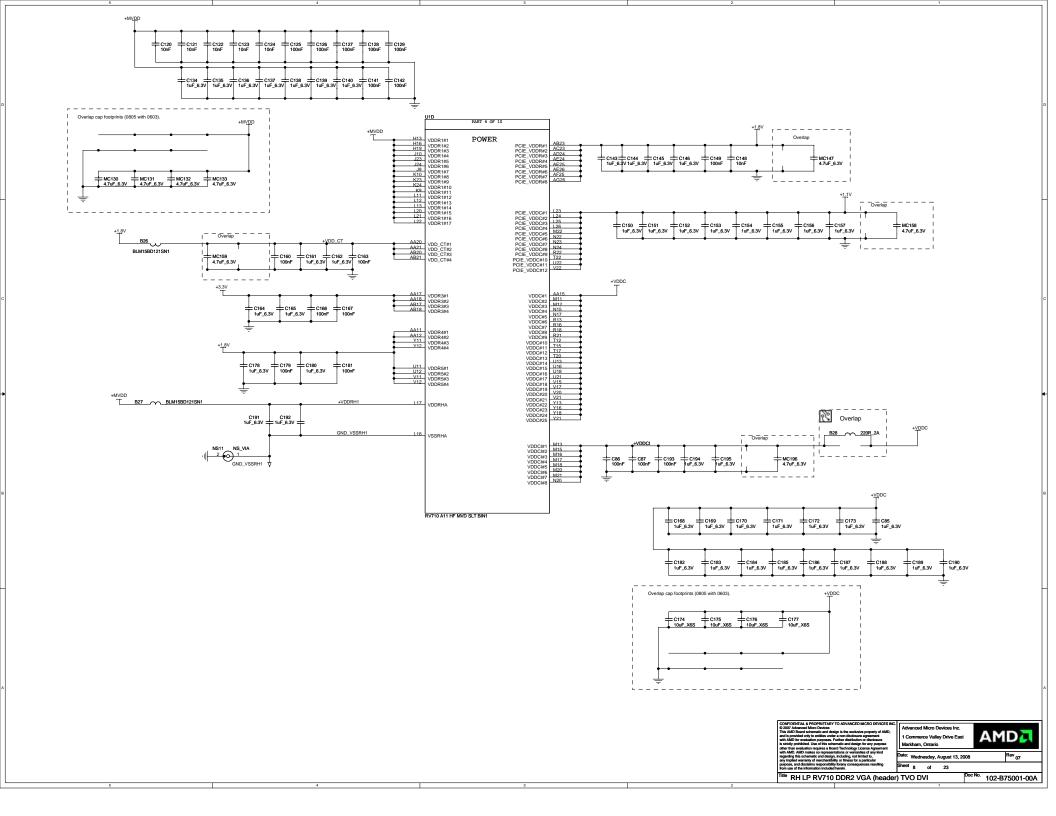


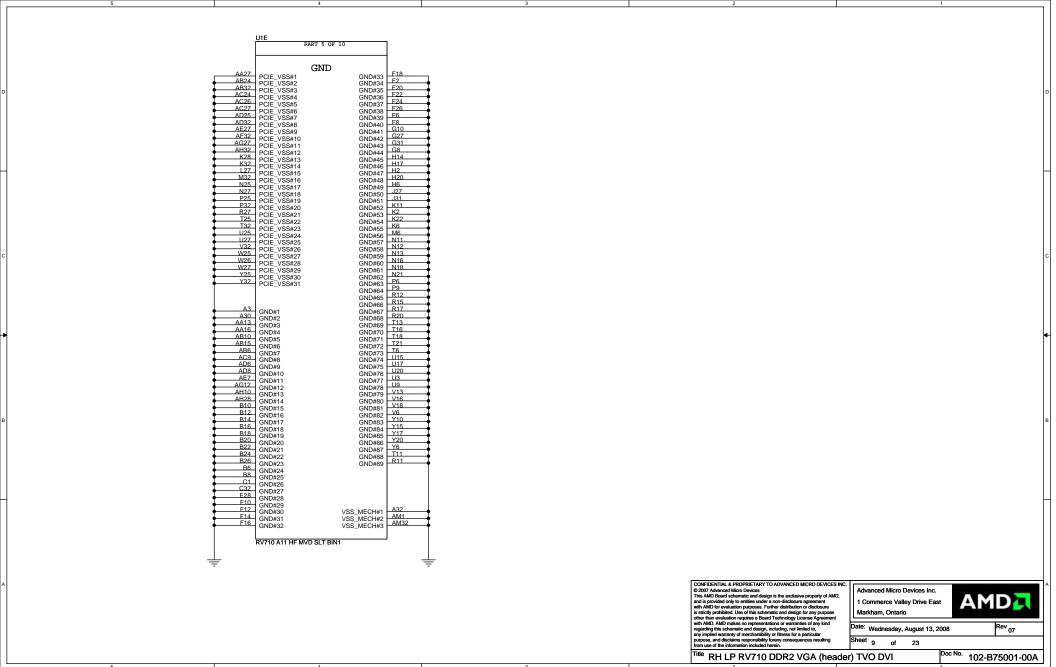
DIVIDER RESISTORS	DDR2	
MVREF TO 1.8V	100R	
MVREF TO GND	100R	



**AMD** 

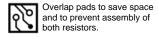
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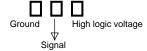


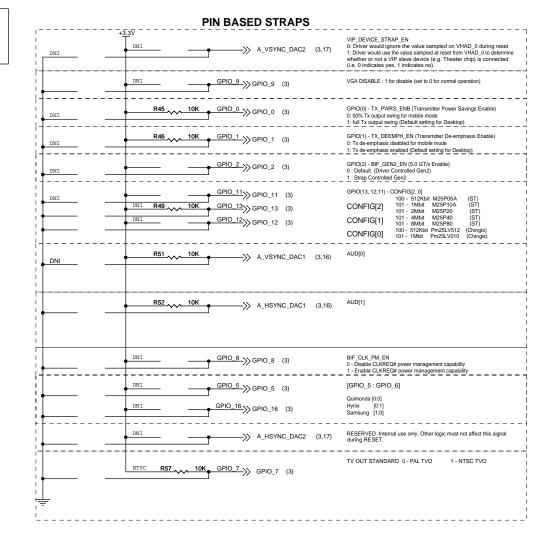
### **PIN BASED STRAPS**

Pull-Down Resistors are for BU until built-in pull-downs are verified.



Layout



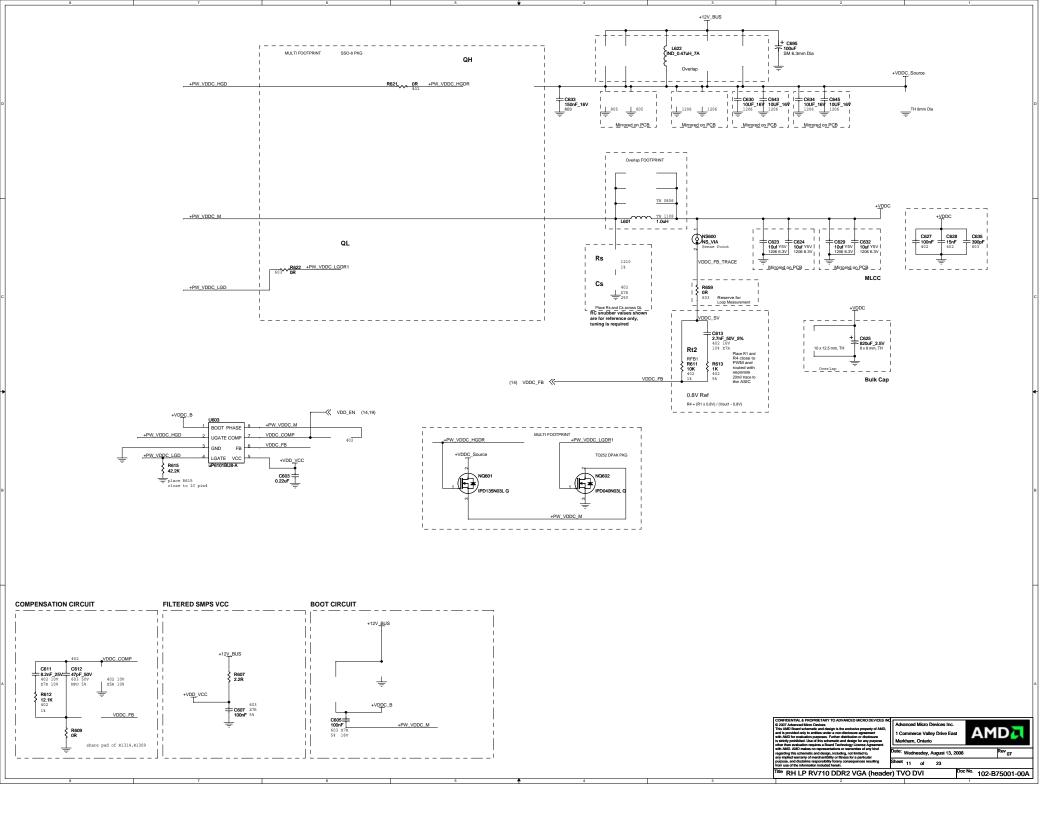


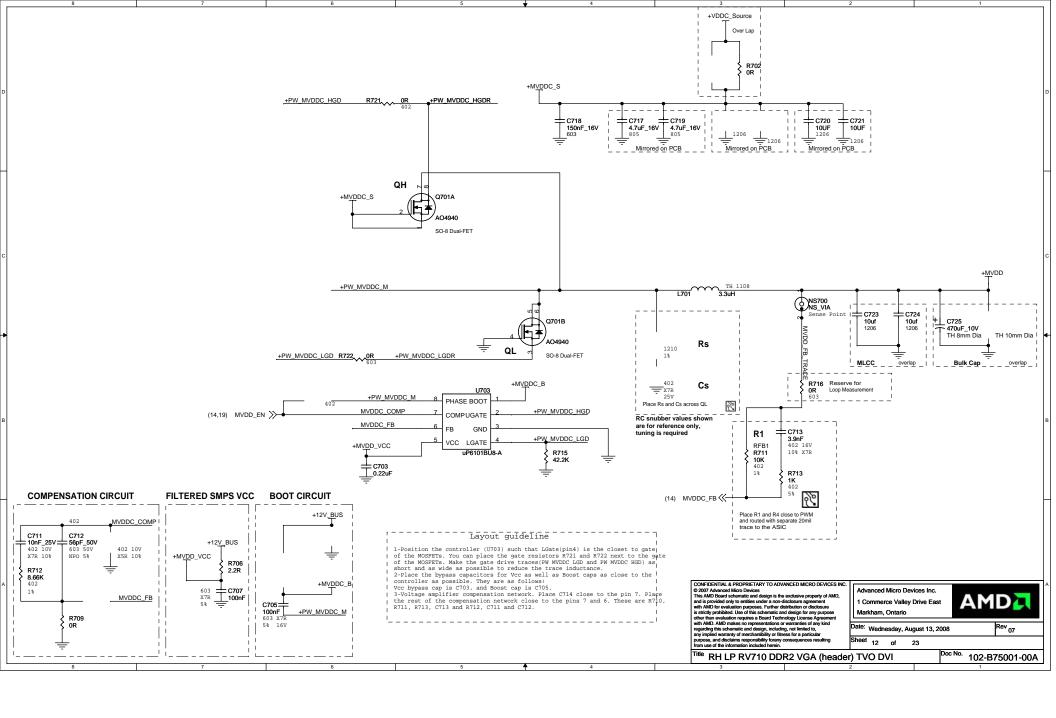
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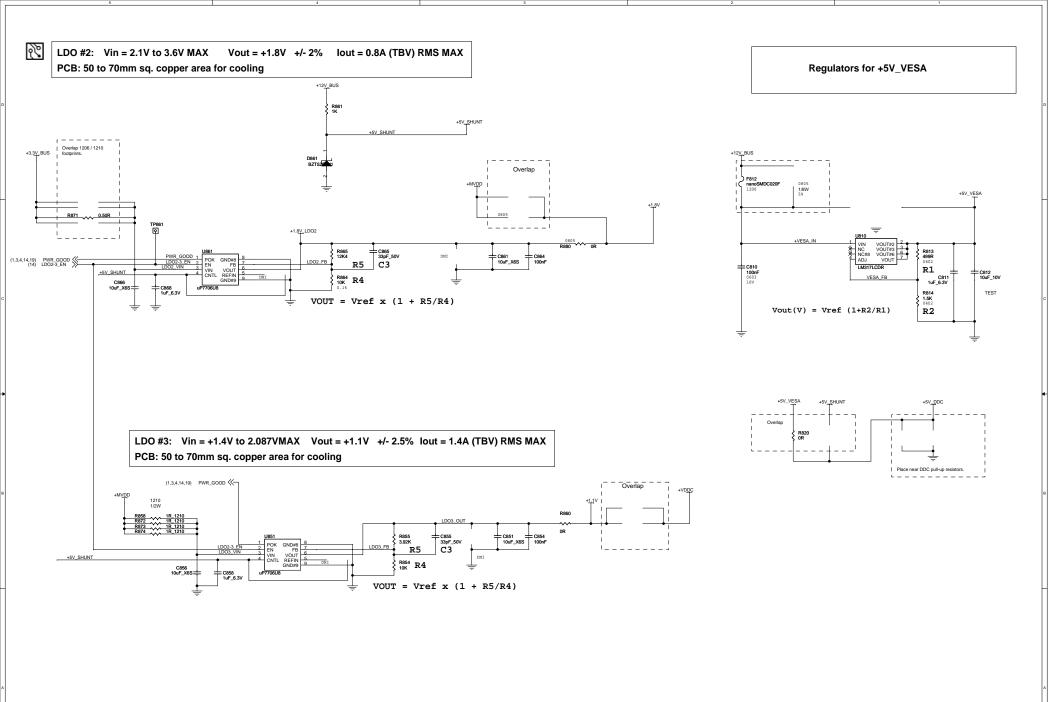
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Title RH LP RV710 DDR2 VGA (header) TVO DVI

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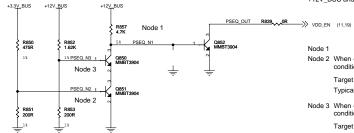






#### Power up/down Sequencing

Power Sequence Circuit to ensure SMPS\_EN is released after +12V\_BUS and +3.3V\_BUS are both in regulation.



Node 1

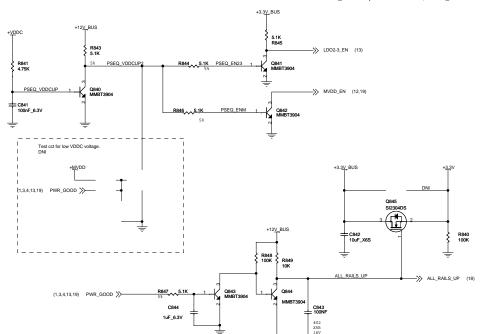
Node 2 When +3.3V\_BUS gets close to regulation, one of the two conditions of releasing SMPS\_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)
Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS\_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)
Typical trigger when +12V ramps above 10V (1.1V)

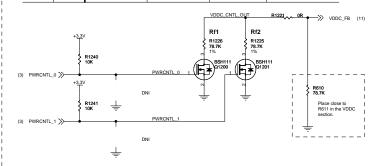
When +12V\_BUS ramps above min Vbe, SMPS\_EN will be held low



### Power Play

VDDC Voltage Settings Using GPIOs

		Output Voltage (V)					
PWRCNTL_1	PWRCNTL_0		Rf1=	Rf1=			
GPIO_20	GPIO_15	Rf2=	Rf2=	Rf2=			
0	0						
0	1						
1	0						
1	1	1 0	1		Power-up Default		



#### MVDD Voltage Settings Using GPIOs

PWRCNTL_2 GPIO_6	Rf1= Rf2=		Rf1= Rf2=	Rf1= Rf2=	
0					
1	1	0	1		Power-up Default



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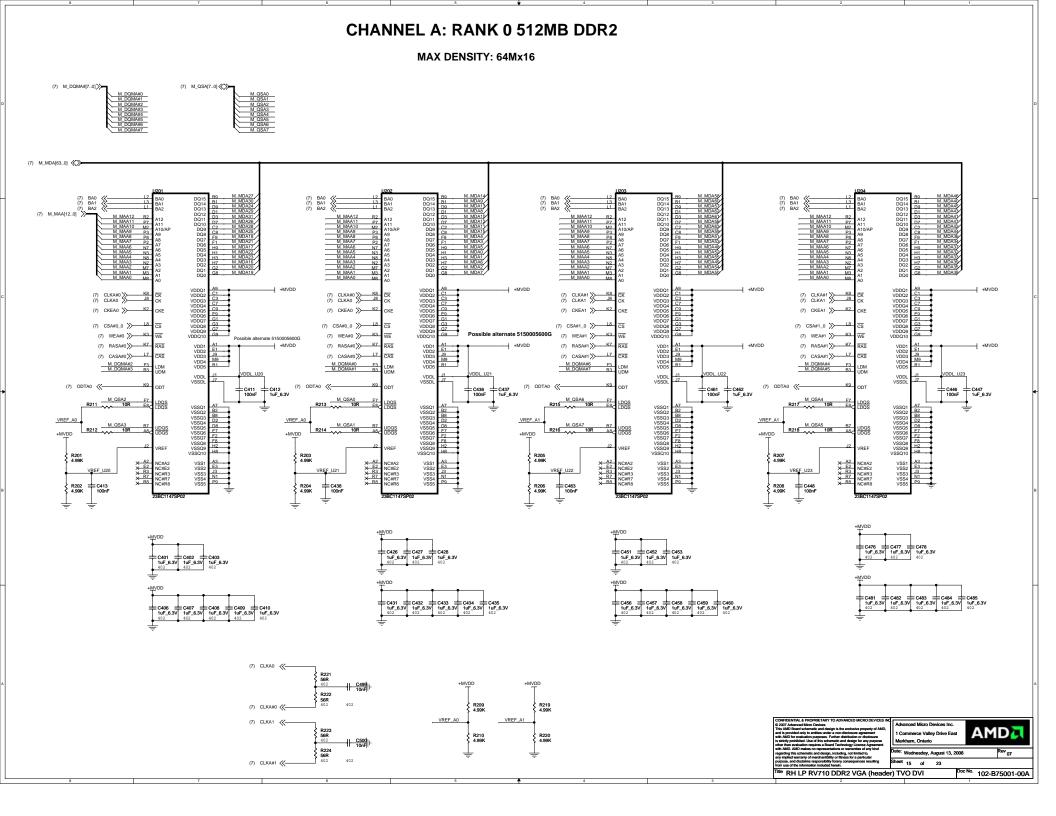
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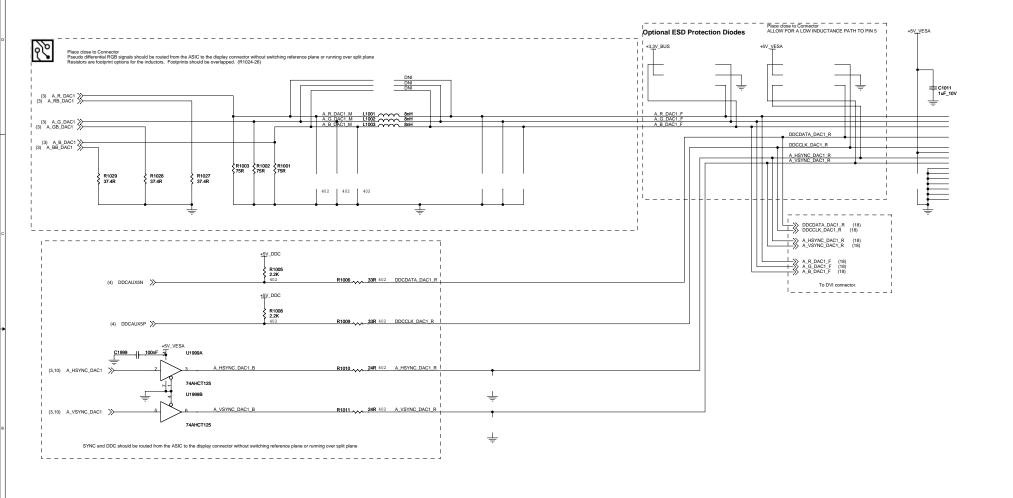
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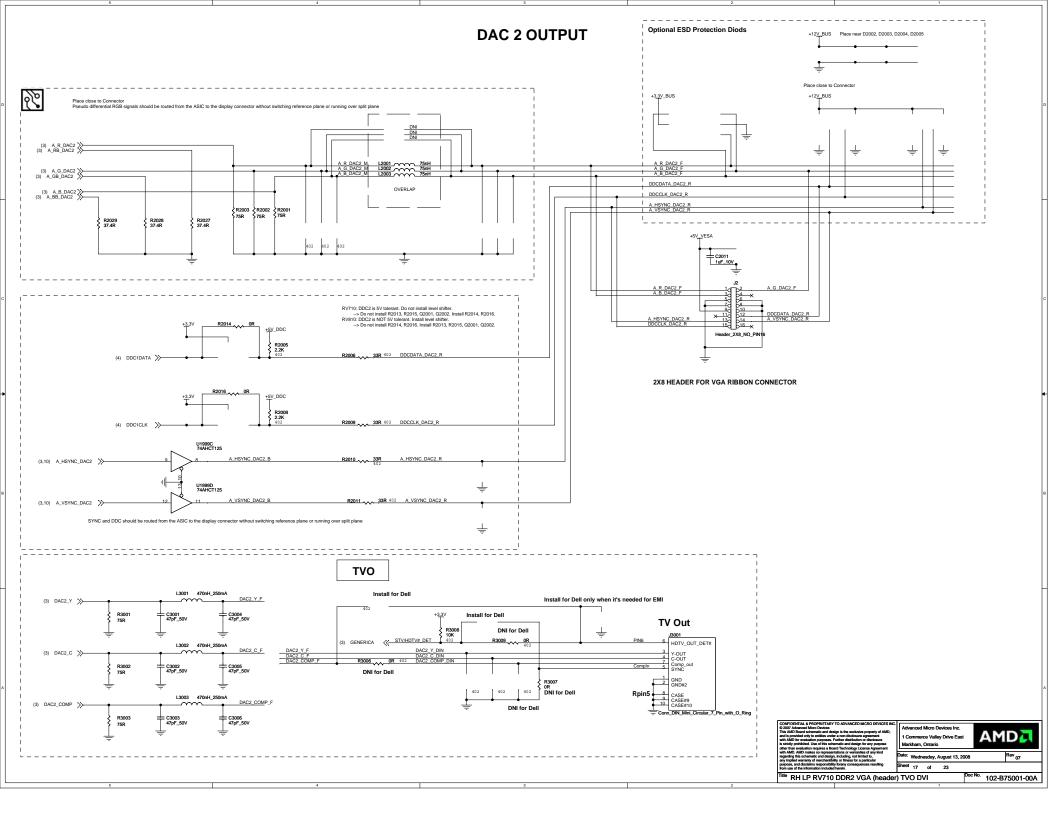
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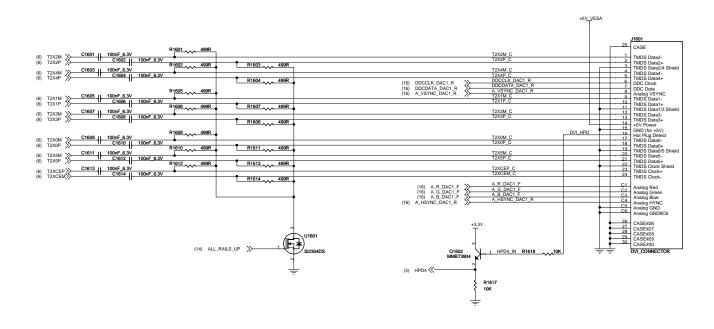
# **DAC 1 OUTPUT**







# **DPE / DPF OUTPUT**



Optional ESD protection diodes					
T2X2P C T2X2M C T2X1P C 1	DNI	T2X2P C T2X2M C -  1 T2X1P C T2X1M C	T2X5P C T2X5M C T2X4P C	DNI	12X5P C 12X5M C   I  12X4P C 12X4M C
TZXOP C TZXOM C TZXCEP C 'II	DNI	T2XOP C T2XOM C T2XCEP C T2XCEM C	T2X3M_C T2X3P_C	DNI	TZXSM C TZXSP C



