31P141, NV31, 4(8,16)Mx16, 64(128,256)MB, VIDEO IN/OUT, DVI-I, VGA

Page Overview

HISTORY:

A00

X00: INITIAL VERSION

X01: First Review
- Replaced series resistors in sync lines with 33ohms
- Moved clamping diodes next to GPU
- Added parallel caps to EMI filter DACB
- Removed not needed strap on SAA7114
- Connected RESET and WP of SST ROM to ROMVCC
- Added parallel ROM and Strapps
- Added FBVDD regulator
- Added STEREO glasses circuit
- Removed Decoupling CAPs on VIP VDD, covered by Caps on page 2
- Added ROM_VCC for cleaner planes
- Changed used TMDS lines of IFPA and IFPB to TP from NTP
- Changed Resistor for AGP Vref circuit to 158k

X02: Final Review
- Added clock termination resistors
- Added net name for FBCALxxx
- Added cap on filter input for FB_DLLVDD, DACA_VDD & DACB_VDD
- Changed netnames for SAA7114 NTPs to NTP_xxx
- Added 1uF cap parallel to fan connector
- Changed all xxCALxx resistors to 50 Ohms
- Changed all FBxDQS*<x> to NTP_FBxDQS*<x> with NO_TEST property

602-10141-0000-000 Base Schematic

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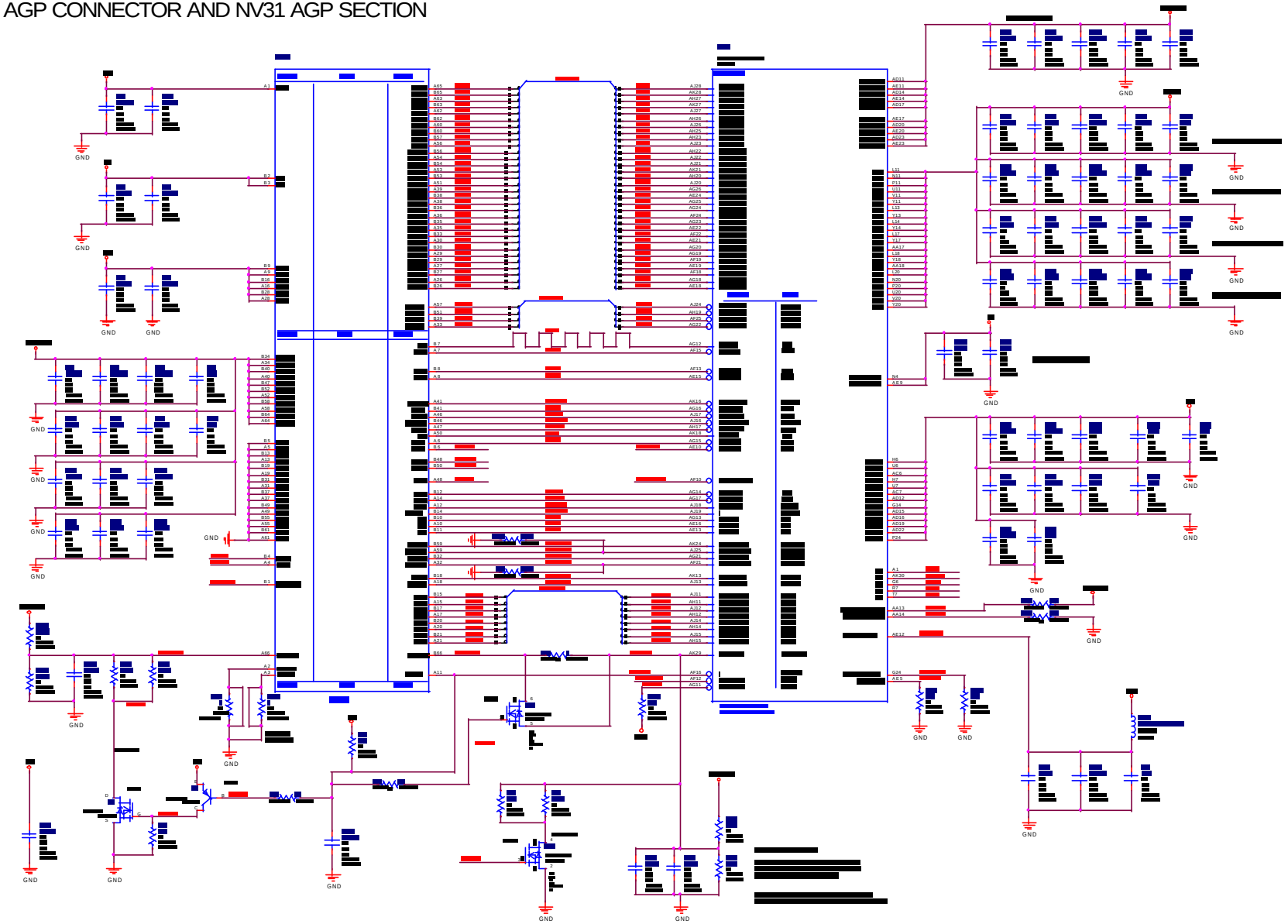
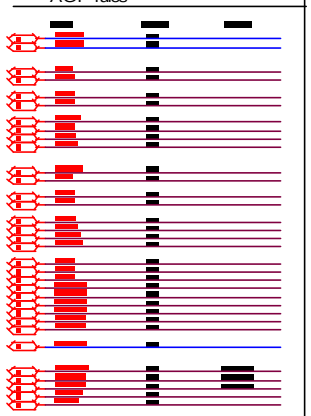
Size: Custom | Document Number | Rev: 00A
TOP PAGE
Date: Wednesday, January 29, 2003 | Sheet of

AGP CONNECTOR AND NV31 AGP SECTION



AGP rules



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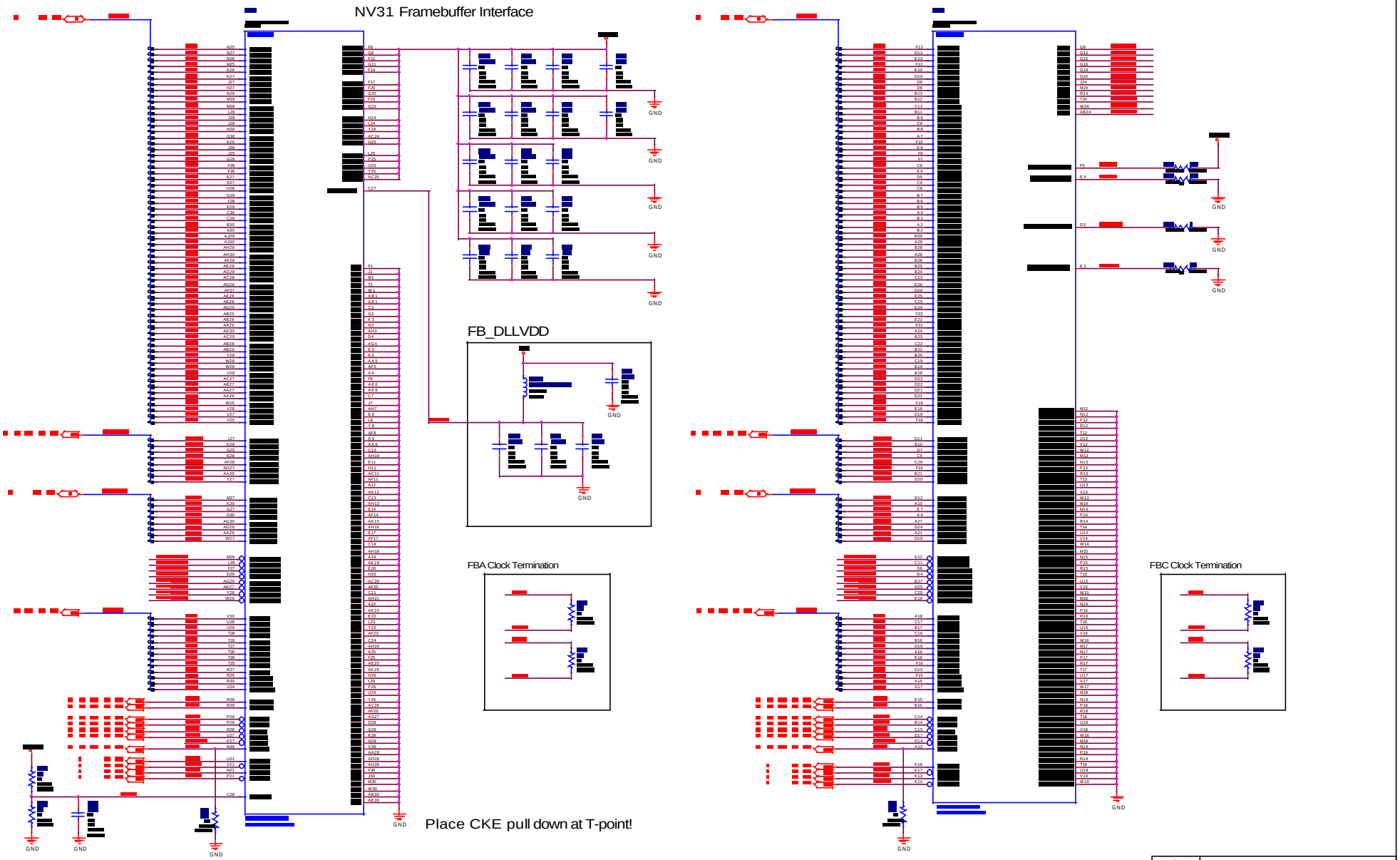
Size: Custom	Document Number: AGP CONNECTOR AND NV31 AGP SECTION	Rev: 00A
Date: Wednesday, January 29, 2003	Sheet of	



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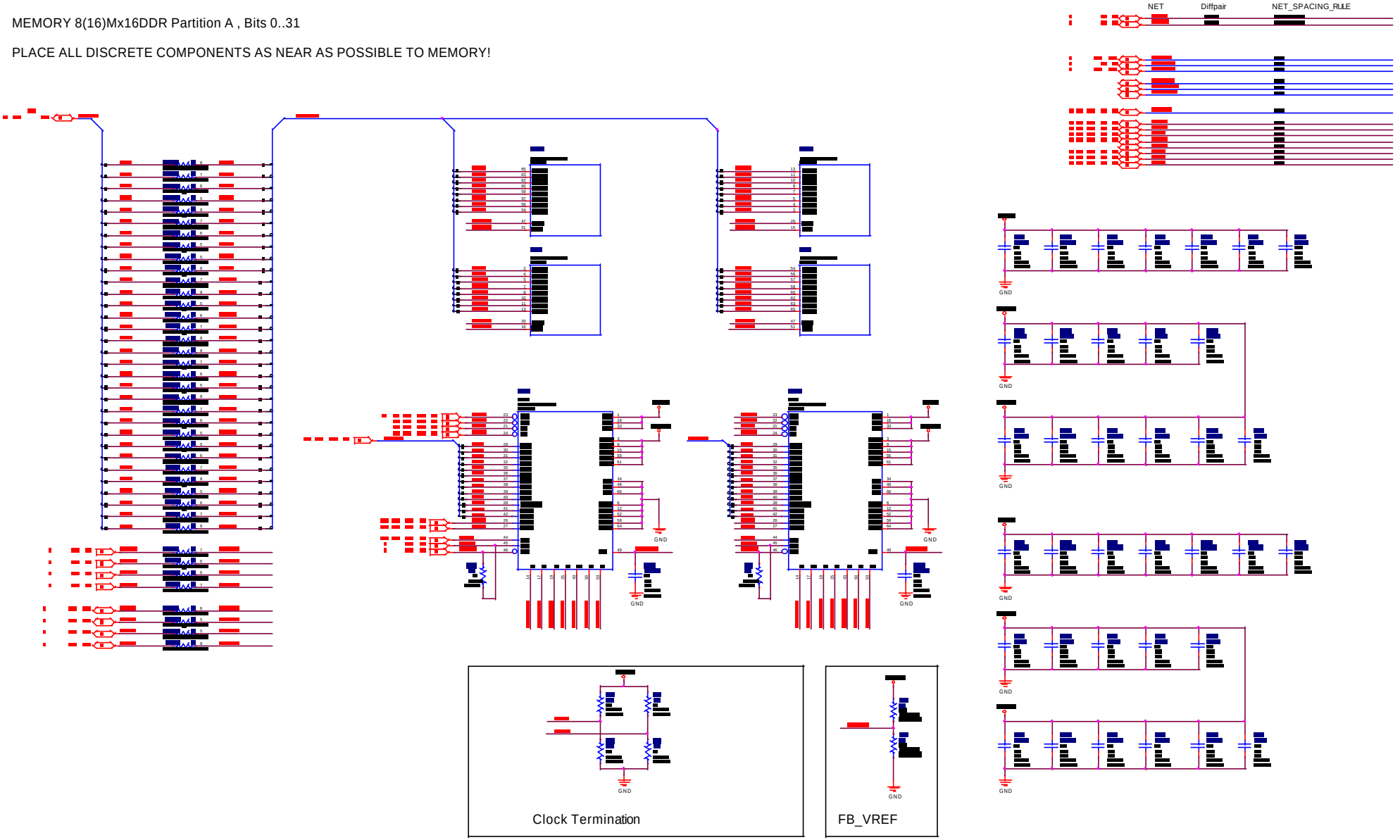
Size: Custom | Document Number: NV31 Framebuffer Interface | Rev: 00A

Date: Wednesday, January 29, 2003 | Sheet of

MEMORY 8(16)Mx16DDR Partition A , Bits 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



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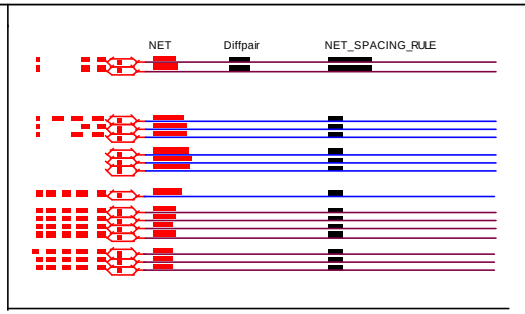
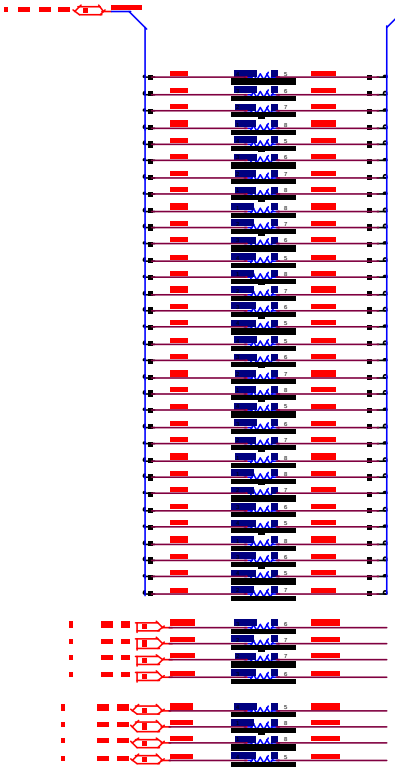
Size: Custom | Document Number: MEMORY 8(16)Mx16DDR Partition A , Bits 0..31 | Rev: 0.0A

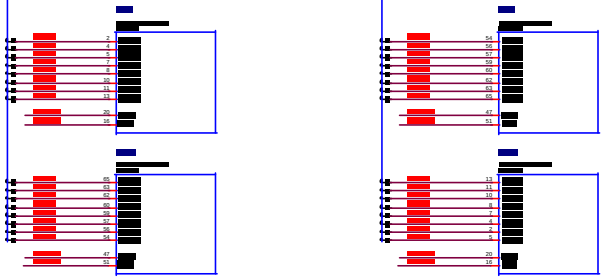
Date: Wednesday, January 29, 2003 | Sheet of

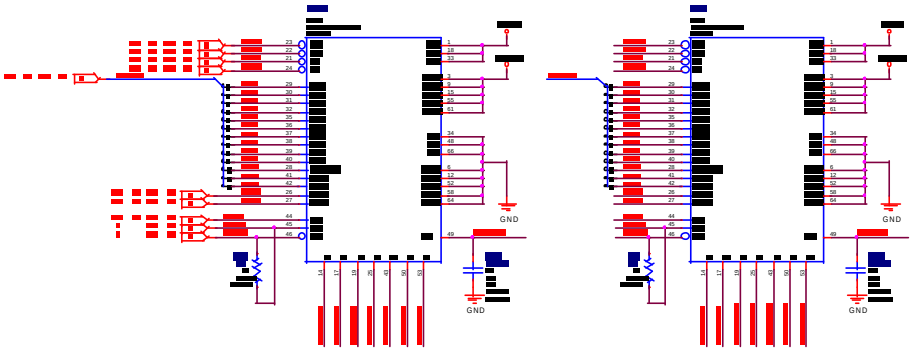
MEMORY 8(16)Mx16DDR Partition A , Bits 32..63

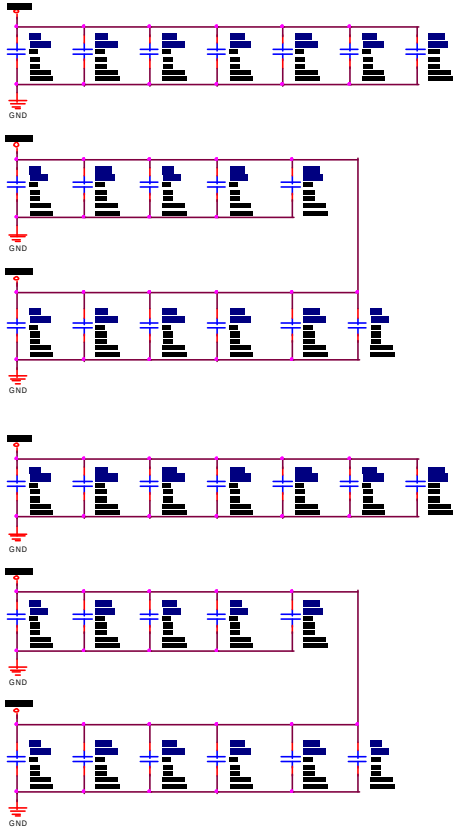
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

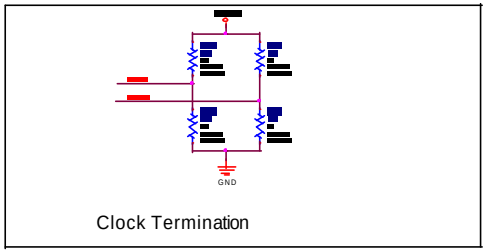


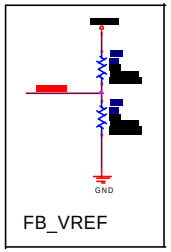












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Date: Wednesday, January 29, 2003 | Sheet of

MEMORY 8(16)Mx16DDR Partition C , Bits 0..31

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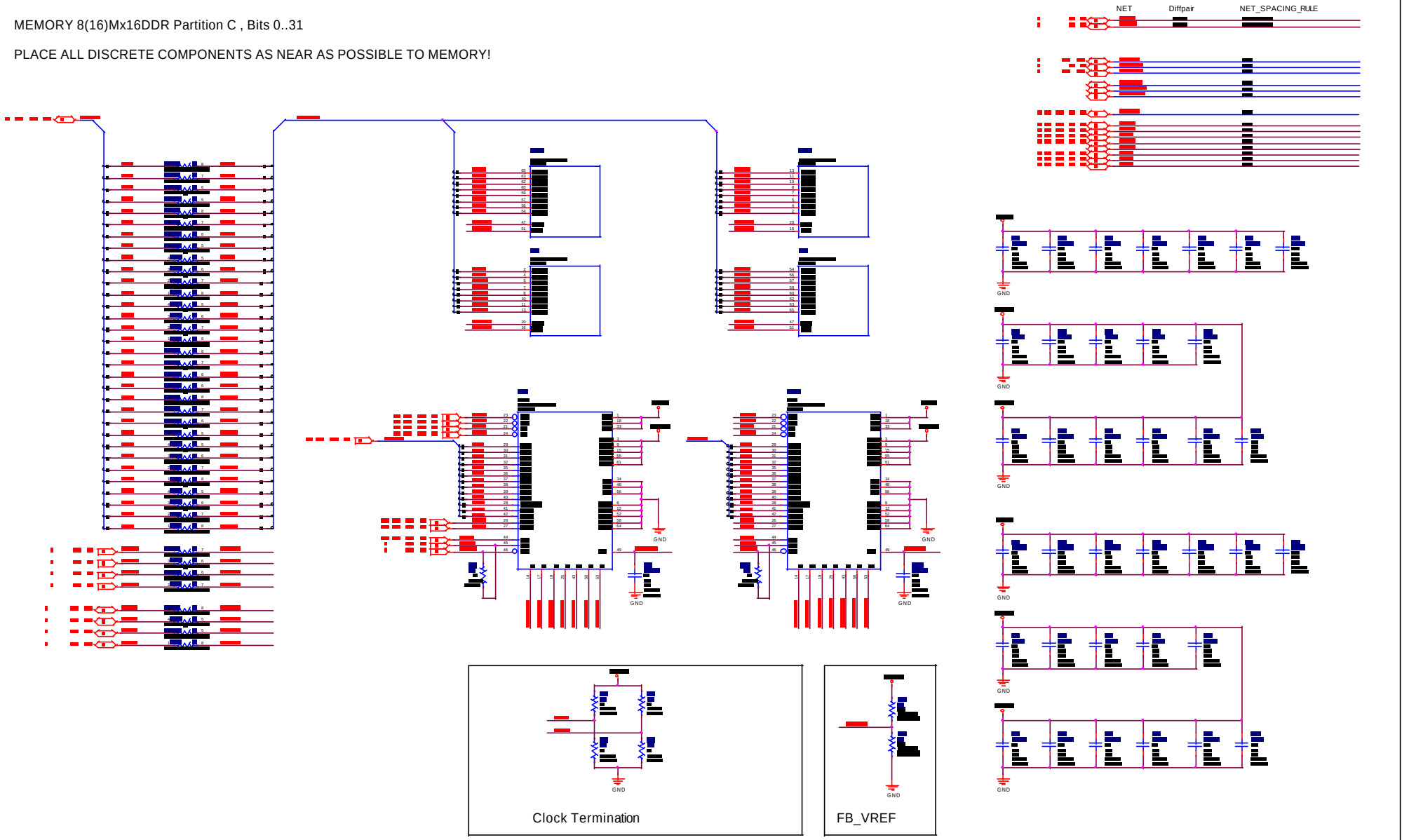

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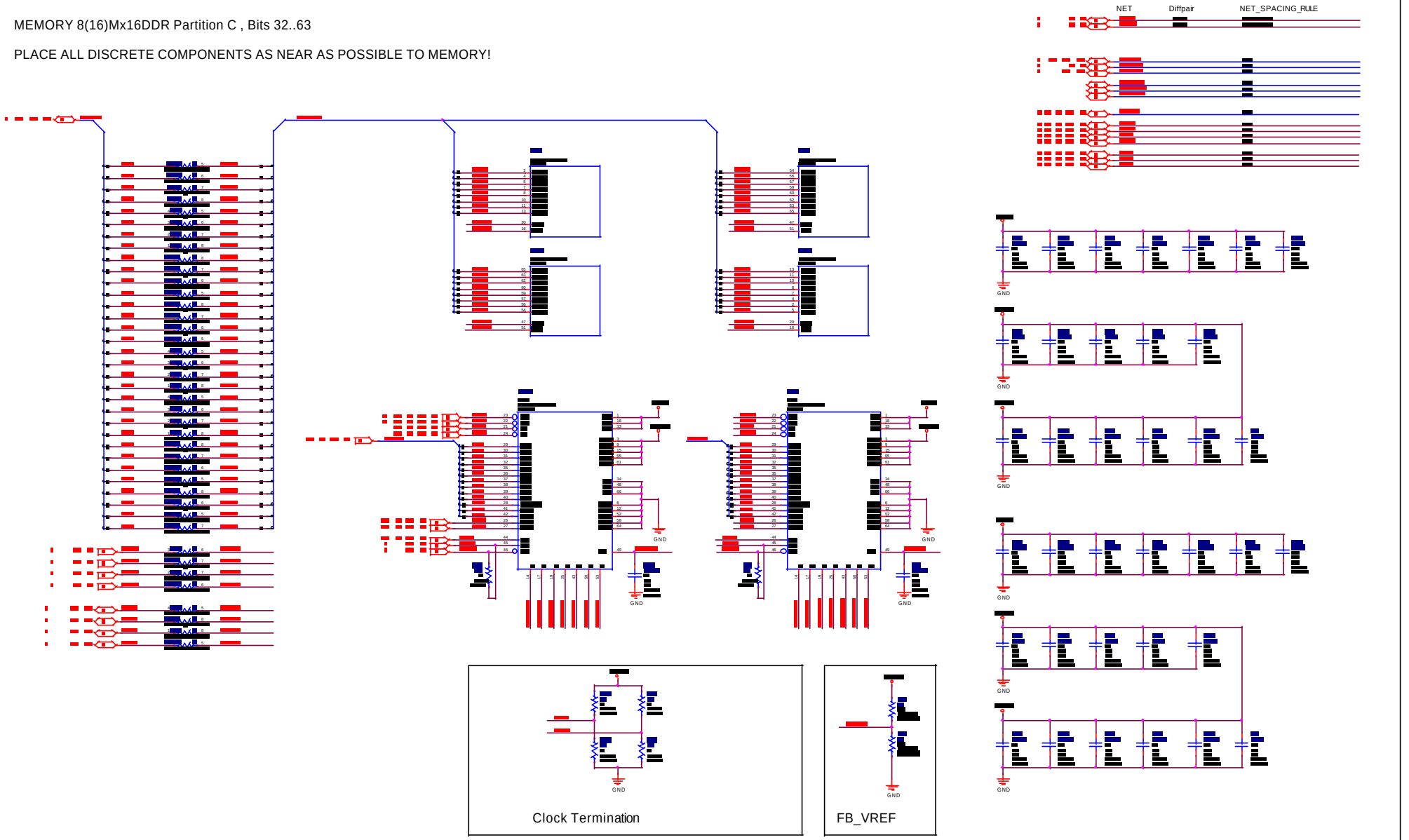
MS-8912 base on P141 modify

Size: Custom | Document Number: MEMORY 8(16)Mx16DDR Partition C , Bits 0..31 | Rev: 00A

Date: Wednesday, January 29, 2003 | Sheet of

MEMORY 8(16)Mx16DDR Partition C , Bits 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



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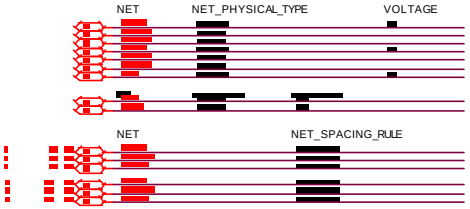
MS-8912 base on P141 modify

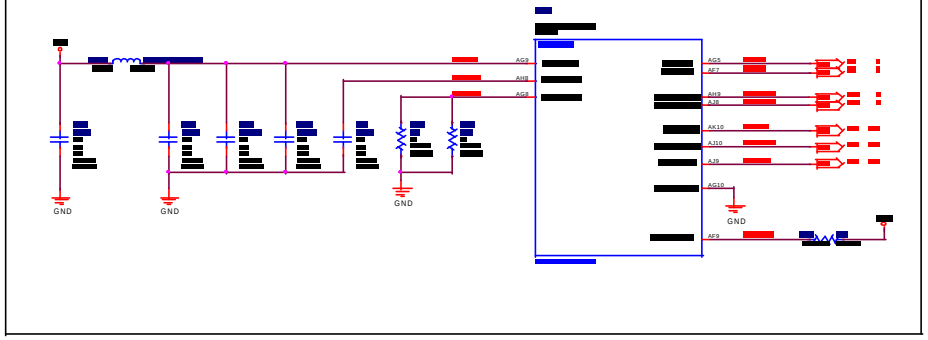
Size: Custom | Document Number: MEMORY 8(16)Mx16DDR Partition C , Bits 32..63 | Rev: 00A

Date: Wednesday, January 29, 2003 | Sheet of

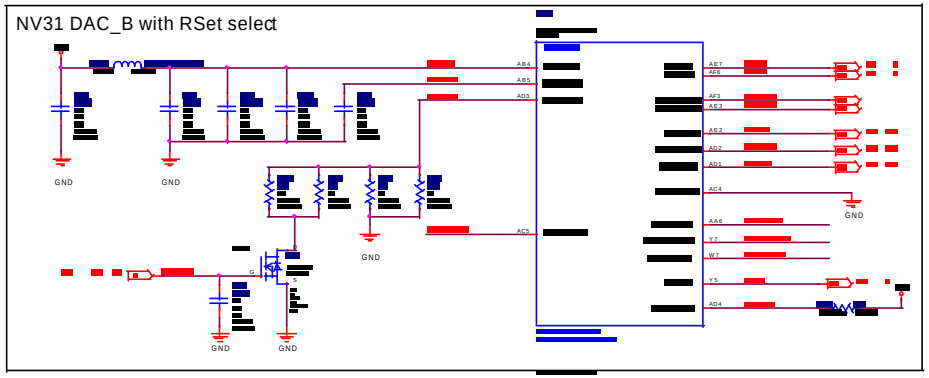
NV31 DAC_A, DAC_B, PLL, SYNC Buffer



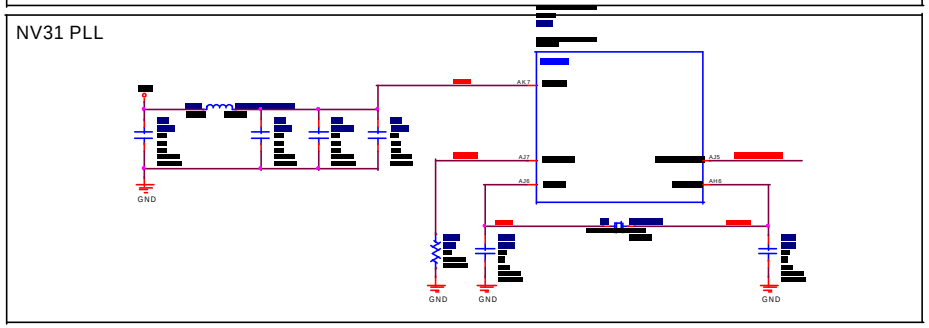
NV31 DAC_A



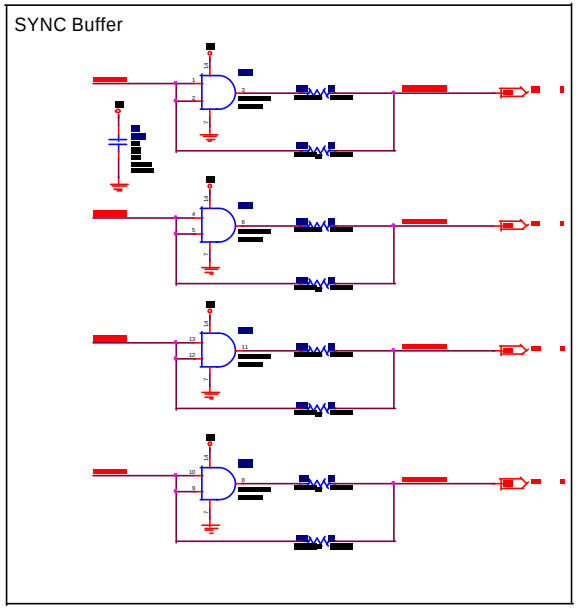
NV31 DAC_B with RSet select



NV31 PLL



SYNC Buffer



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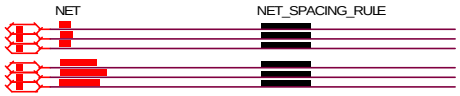
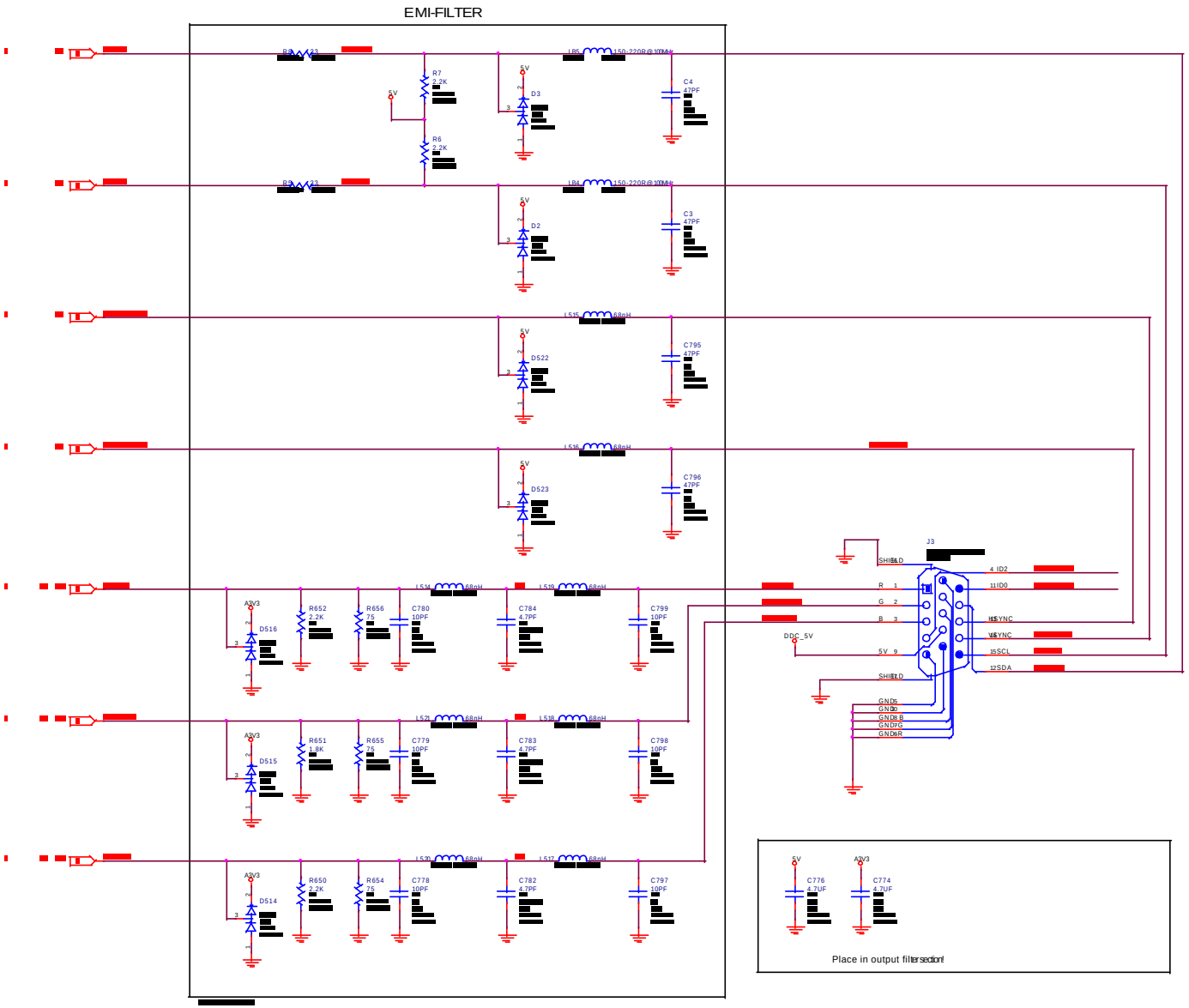
Size: Custom	Document Number: NV31 DAC_A, DAC_B, PLL, SYNC Buffer		Rev: 00A
Date: Wednesday, January 29, 2003	Sheet	of	

Primary Display (DACA), DB15 only!





Place all filter components on the side nearest to the reference GND plane!

Route all signals only on layers referenced to GND!

Don't split the reference GND plane beneath a RGB signal!

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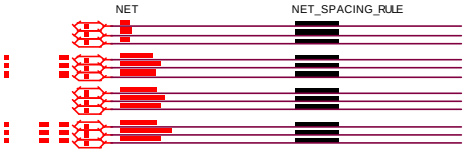
MS-8912 base on P141 modify		
Size: C	Document Number: Primary Display (DACA), DB15 only!	Rev: 00A
Date: Wednesday, January 29, 2003	Sheet of	

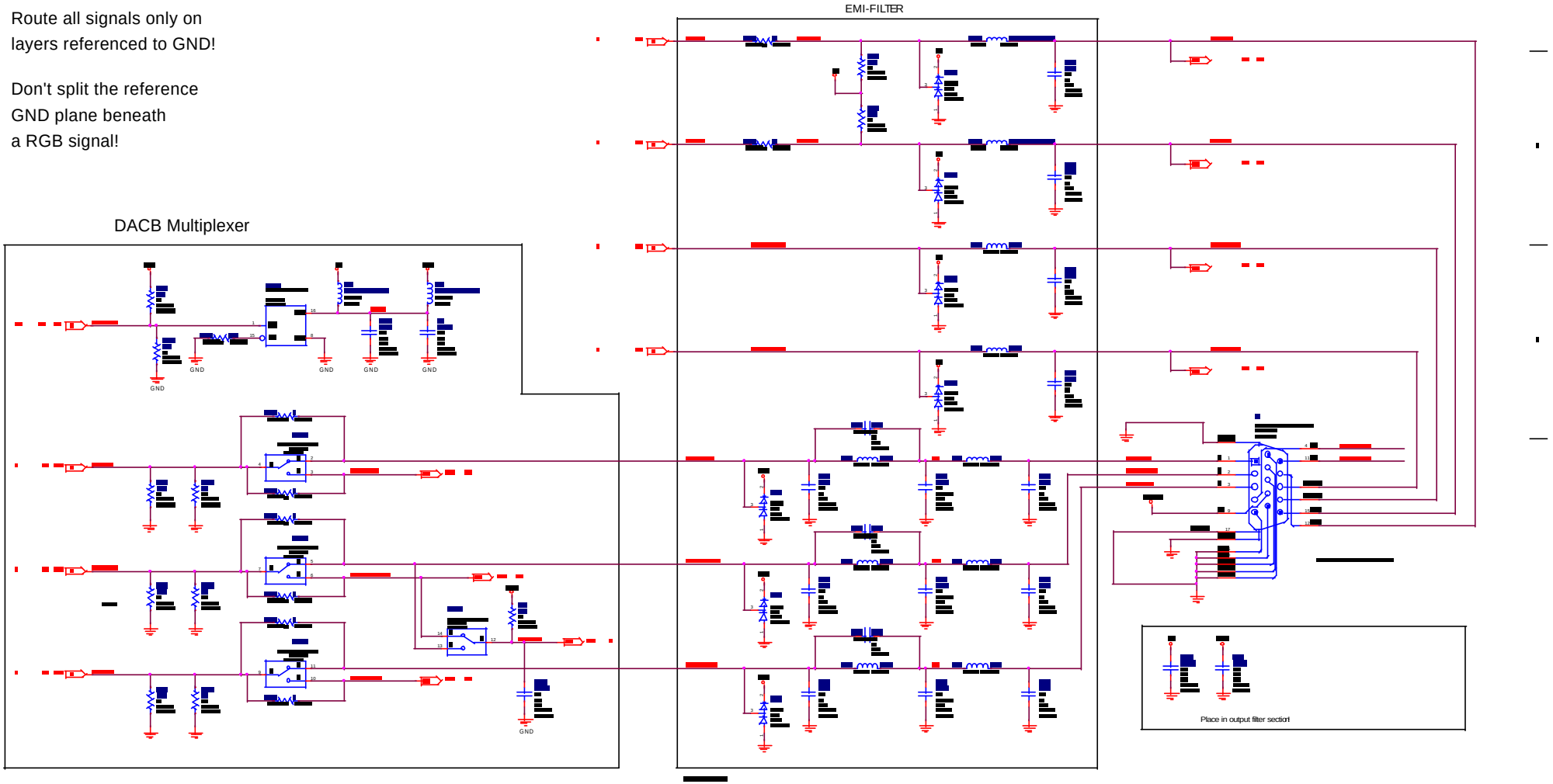
Secondary Display (DACB), long DB15 optional DVI-I

Place all filter components on the side nearest to the reference GND plane!

Route all signals only on layers referenced to GND!

Don't split the reference GND plane beneath a RGB signal!





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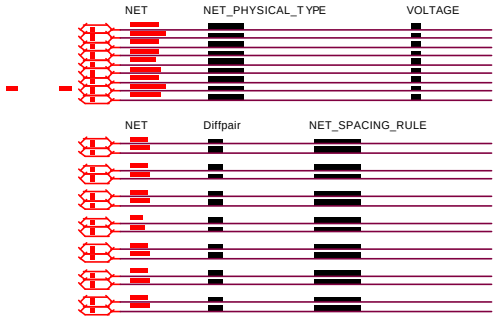
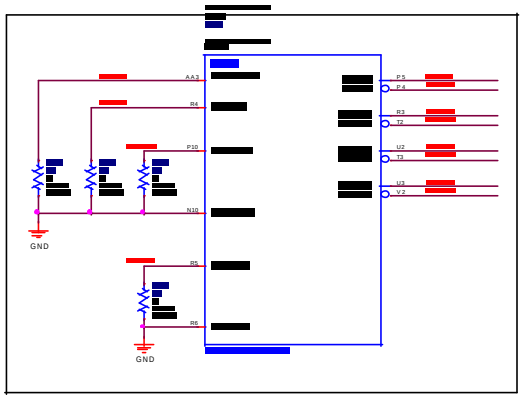
Size: Custom | Document Number: Secondary Display (DACB), long DB15 optional DVI-I | Rev: 00A

Date: Wednesday, January 29, 2003 | Sheet of

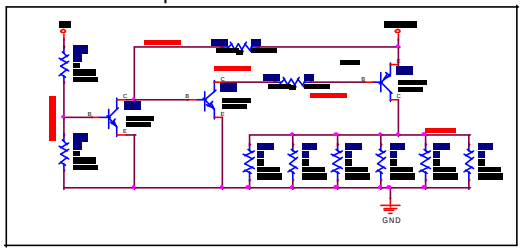
INTERNAL DUAL LINK TMDS POWER AND DECOUPLING



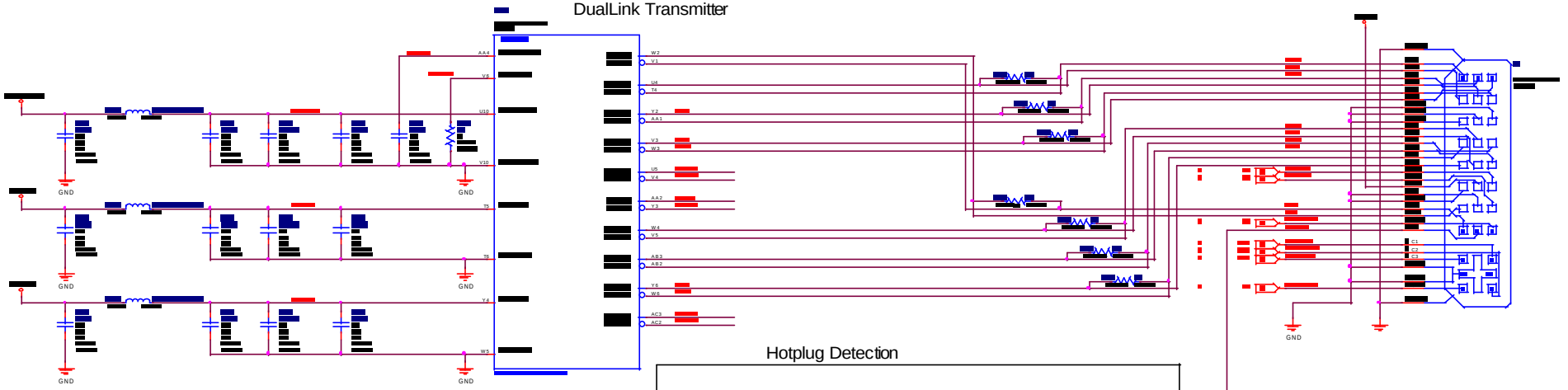
Unused Transmitter



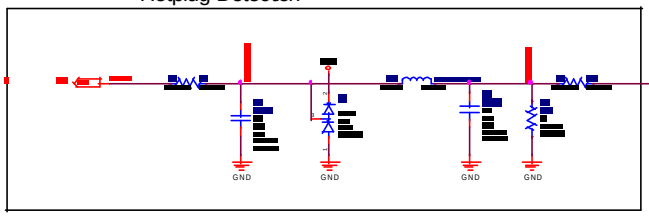
TMDS backdrive prevention

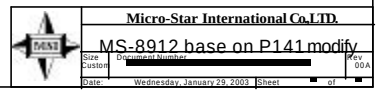


DualLink Transmitter

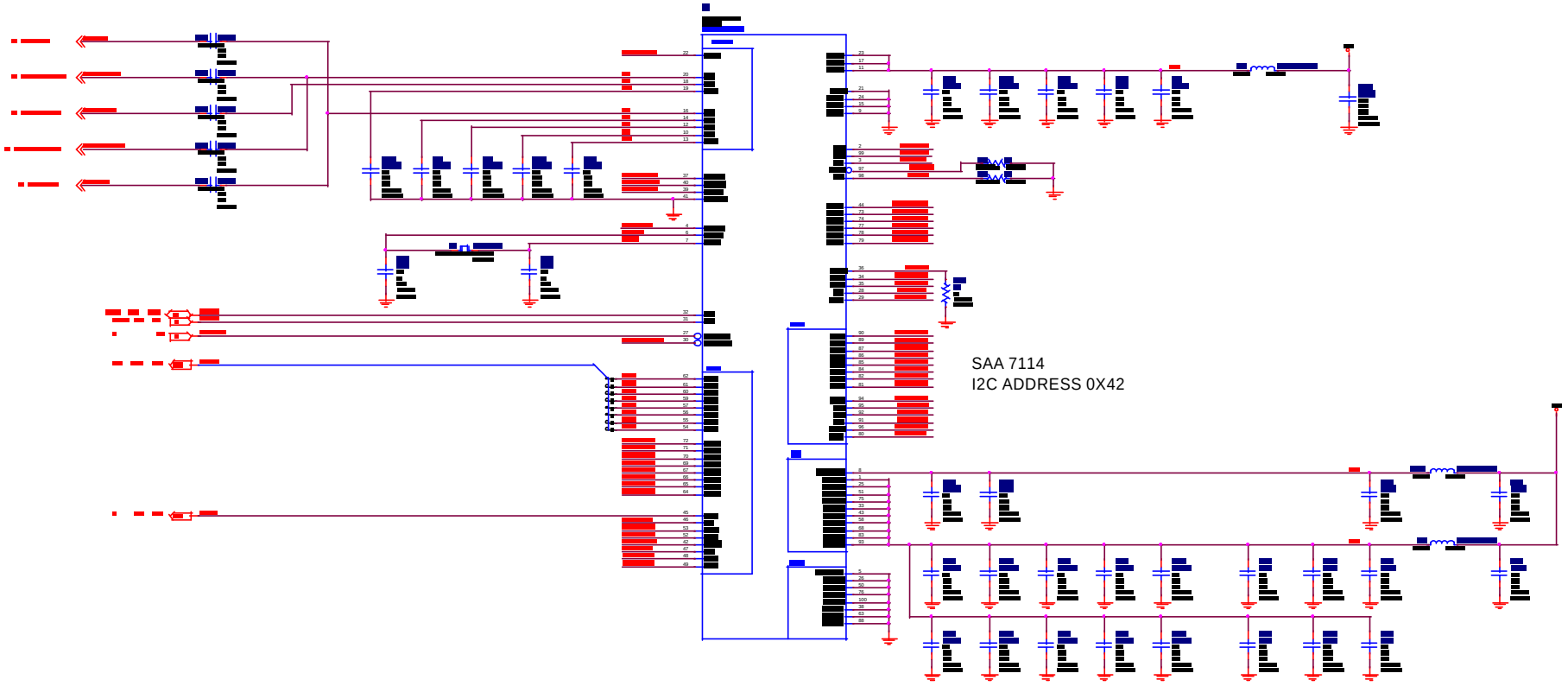


Hotplug Detection





VIDEO CAPTURE



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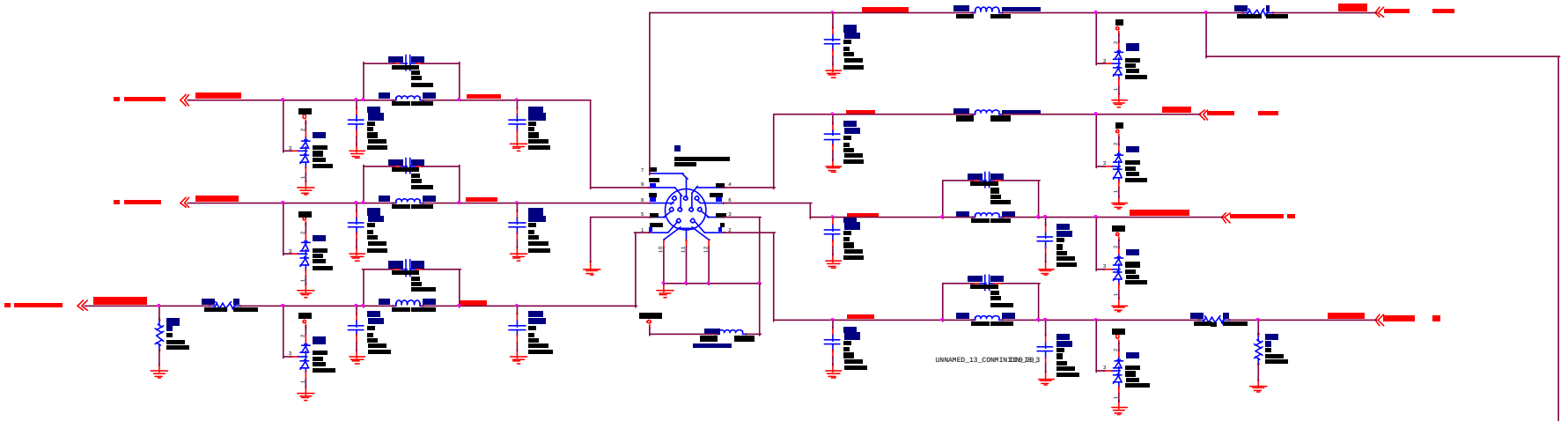
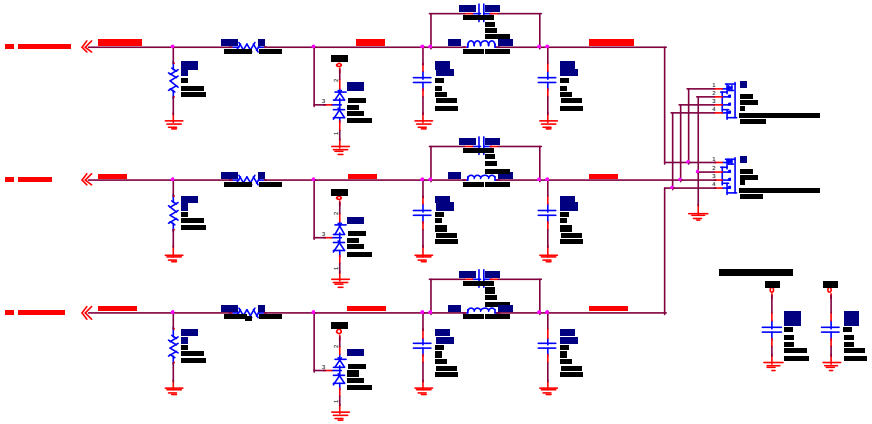
Size: Custom	Document Number: VIDEO CAPTURE	Rev: 00A
Date: Wednesday, January 29, 2003	Sheet ■ of ■	

MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES

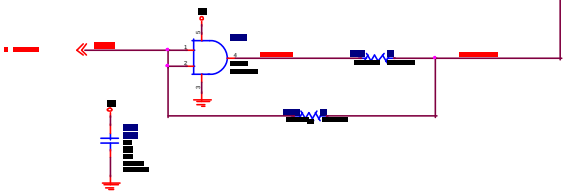


INTERNAL VIDEO IN CONNECTOR



STEREO GLASSES BUFFER

Place close to MiniDIN connector!



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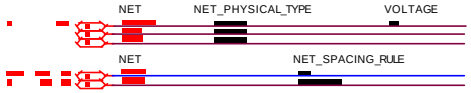
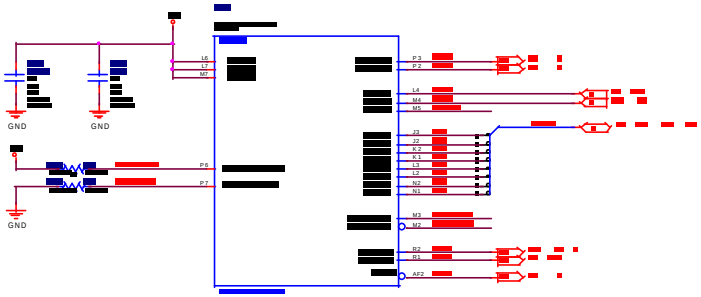
MS-8912 base on P141 modify		
Size: Custom	Document Number: MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES	Rev: 00A
Date: Wednesday, January 29, 2003	Sheet of	

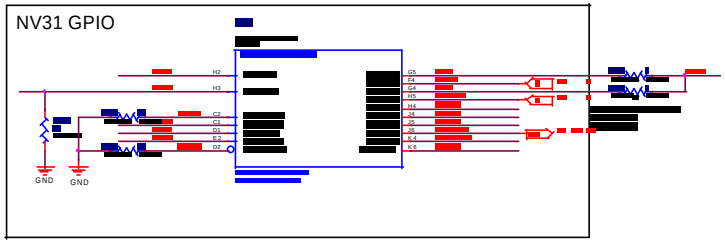
NV31 DVO, VIP AND GPIO SECTION, FAN CONTROL AND TEMP SENSOR



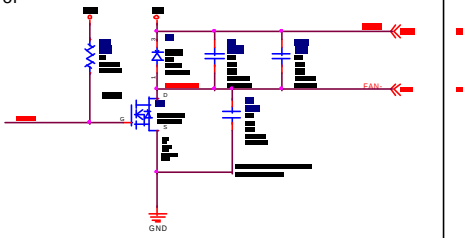
NV31 VIP



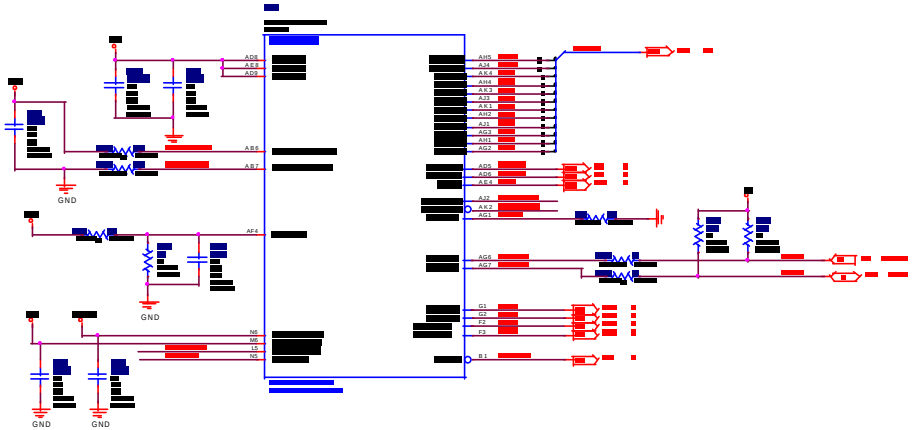
NV31 GPIO



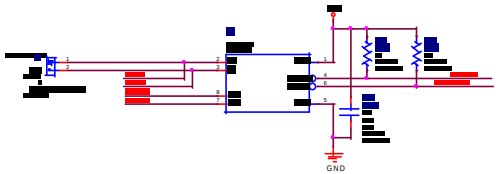
FAN Control



NV31 DVO



TEMP Sensor



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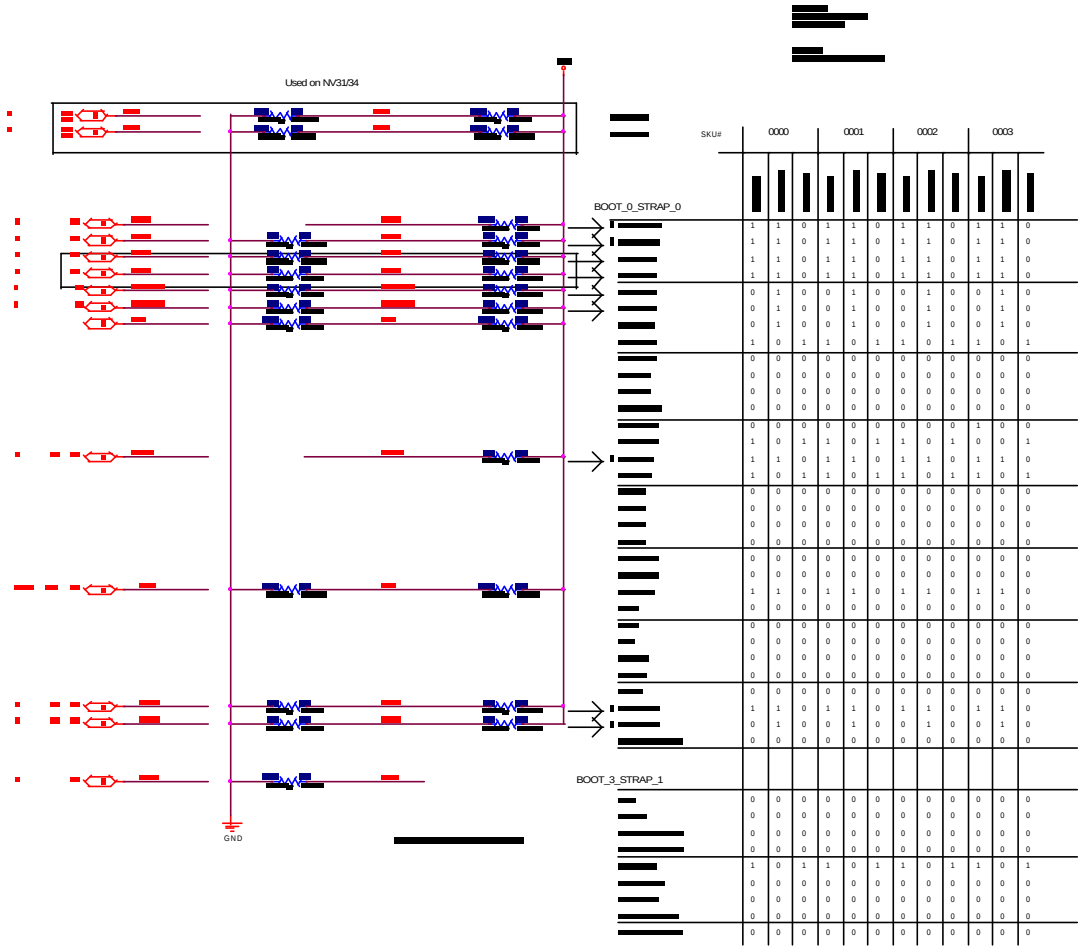
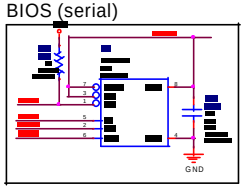
MS-8912 base on P141 modify	
Size: Custom	Document Number:
Rev: 0A	
Date: Wednesday, January 29, 2008	Sheet of

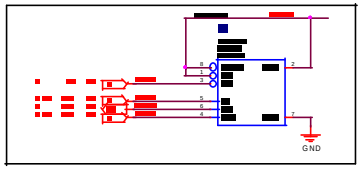
NV31 BIOS STRAPPING



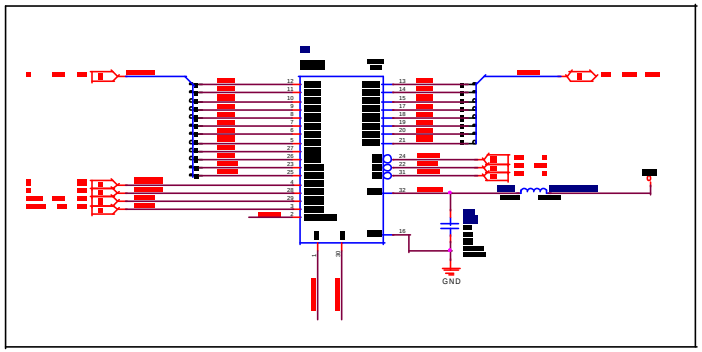
BIOS (serial)



BIOS (serial alternative)

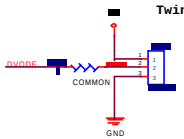


BIOS (parallel alternative)



NV Register Description	NV Address	BIOS Address	Data SKU#0000-0002	Data SKU#0003
BOOT_0_STRAP_0 0x00101000			0x2040E08F	0x2040C08F
BOOT_1_STRAP_0_ANDMASK 0x00101004		0x58	0x6040407F	0x6040407F
BOOT_2_STRAP_0_ORMASK 0x00101008		0x5C	0x00008080	0x00008080
BOOT_3_STRAP_1 0x0010100C			0x00000010	0x00000010
BOOT_4_STRAP_1_ANDMASK 0x00101010		0x60	0x00000000	0x00000000
BOOT_5_STRAP_1_ORMASK 0x00101014		0x64	0x00000010	0x00000010

Twin BIOS



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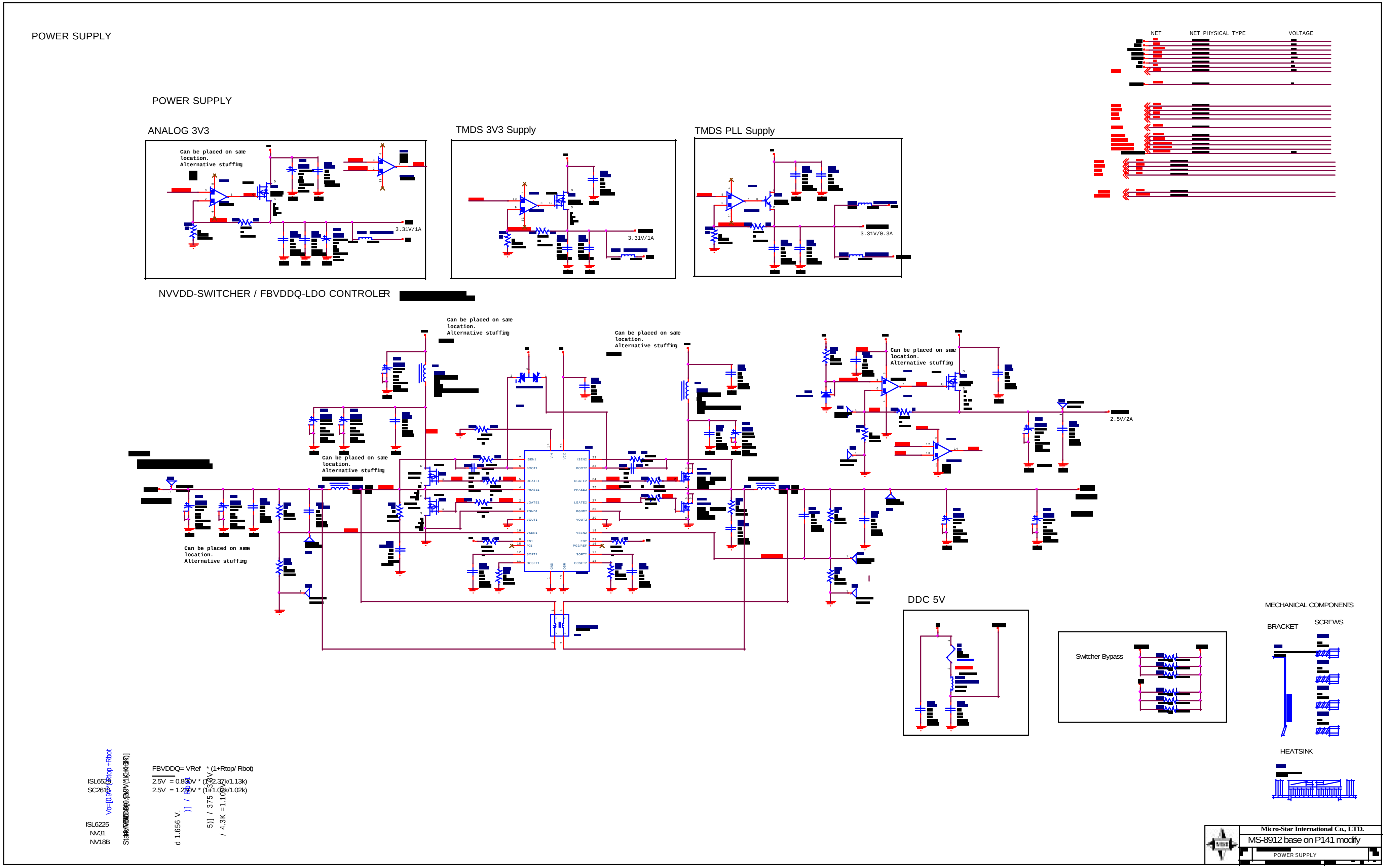
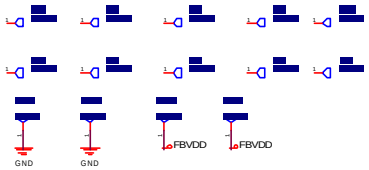
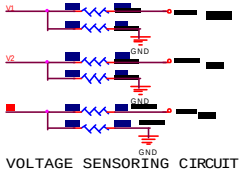
Size: Custom | Document Number: NV31 BIOS STRAPPING | Rev: 00A

Date: Wednesday, January 29, 2003 | Sheet of

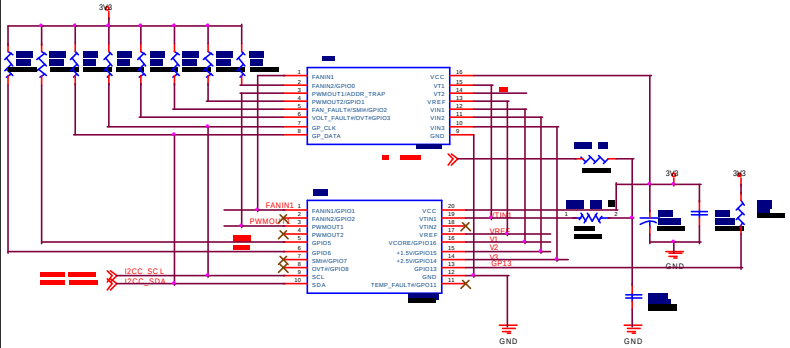

POWER SUPPLY
POWER SUPPLY
ANALOG 3V3
TMDS 3V3 Supply
TMDS PLL Supply
Can be placed on same location. Alternative stuffing
3.31V/1A
3.31V/0.3A
NVVDD-SWITCHER / FBVDDQ-LDO CONTROLER
2.5V/2A
NET
NET_PHYSICAL_TYPE
VOLTAGE
DDC 5V
Switcher Bypass
MECHANICAL COMPONENTS
BRACKET
SCREWS
HEATSINK
FBVDDQ= VRef * (1+Rtop/ Rbot)
2.5V = 0.8V * (1+2.37k/1.13k)
2.5V = 1.25V * (1+1.02k/1.02k)
ISL6225
NV31
NV18B
Micro-Star International Co., LTD.
MS-8912 base on P141 modify
POWER SUPPLY

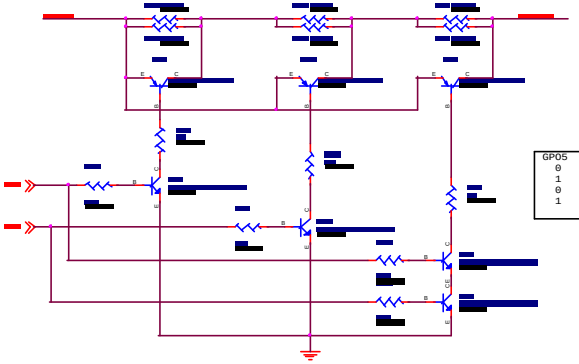
H/W Monitor Funtion





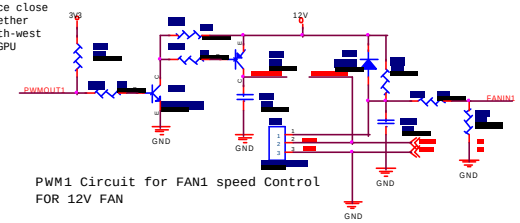
VOLTAGE SENSORING CIRCUIT





GPO5	GPO6	Q1	Q2	Q3	Vout
0	0	off	off	off	9V
1	0	on	off	off	10V
0	1	off	on	off	11V
1	1	on	on	on	12V

Place close
together
south-west
of GPU



PWM1 Circuit for FAN1 speed Control
FOR 12V FAN

TEMPERATURE SENSORING CIRCUIT

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MS-8912 base on P141 modify	
Size: Custom	Document Number: H/W Monitor Function
Rev: 0.0A	
Date: Wednesday, January 28, 2009	Sheet: of