

PG150-C04

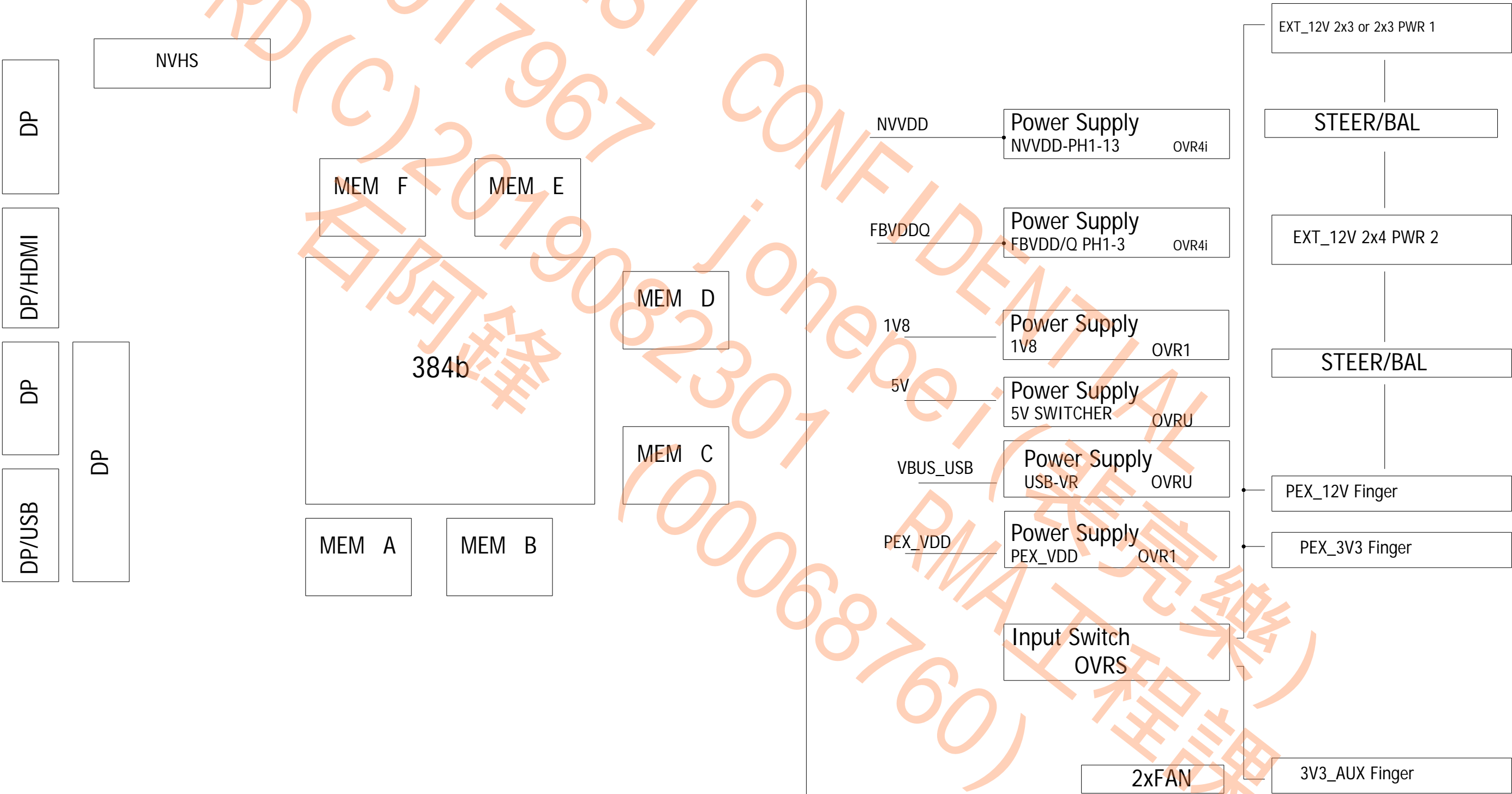
384b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

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Block Diagram



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PCI Express



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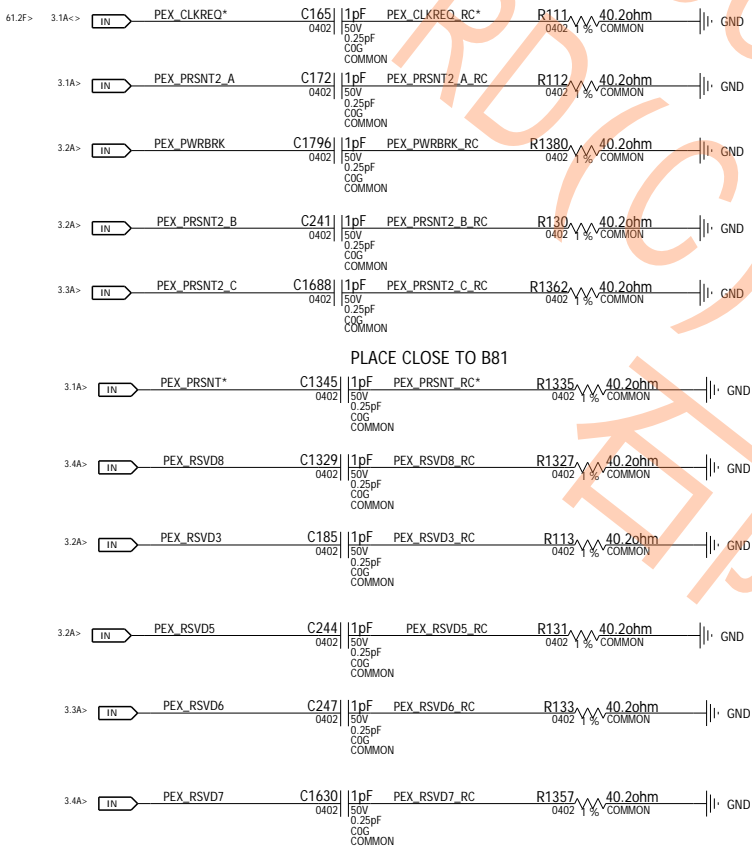
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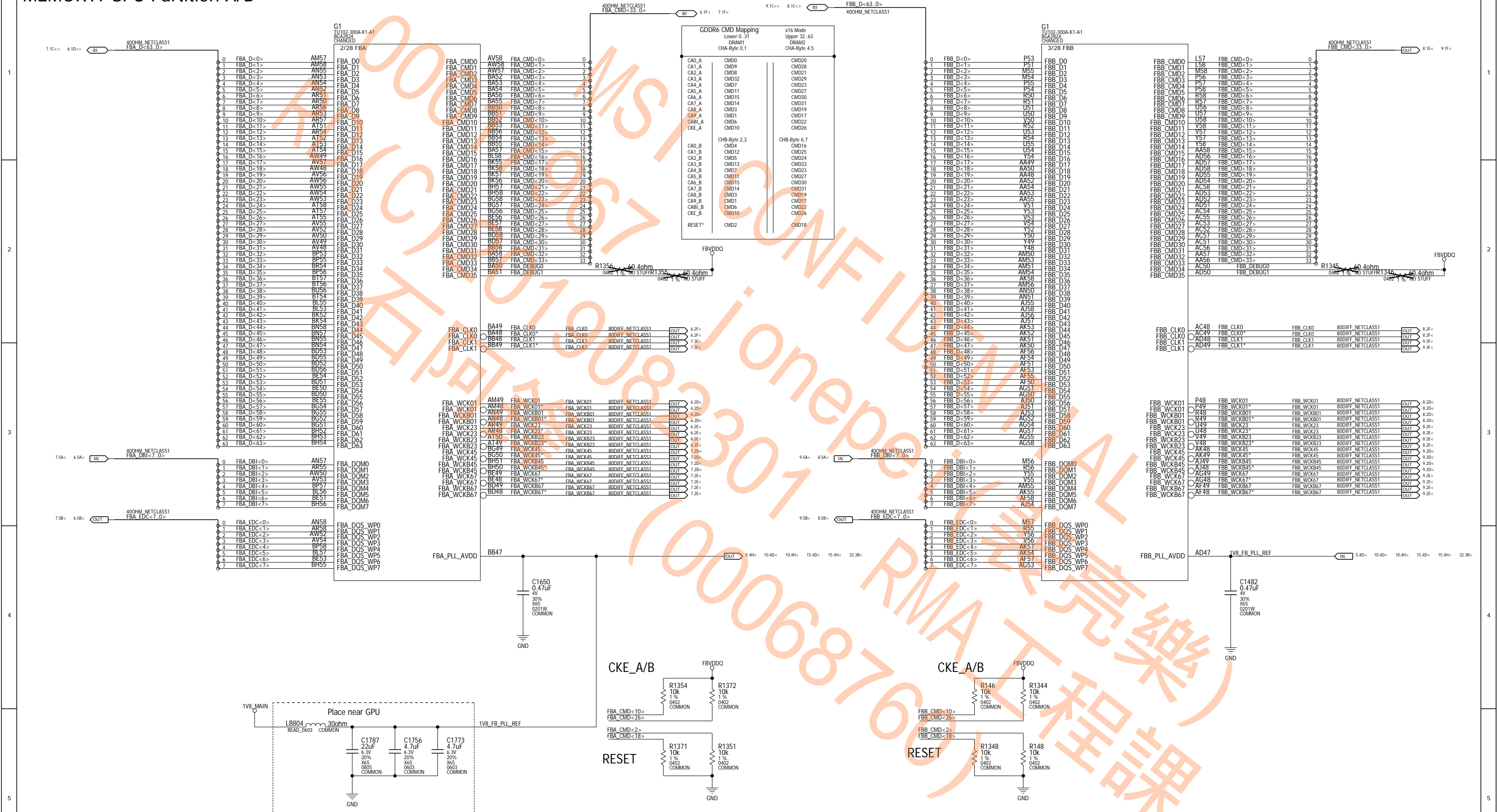
ASSEMBLY	SKU32
PAGE DETAIL	PCI EXPRESS

PCI TERM

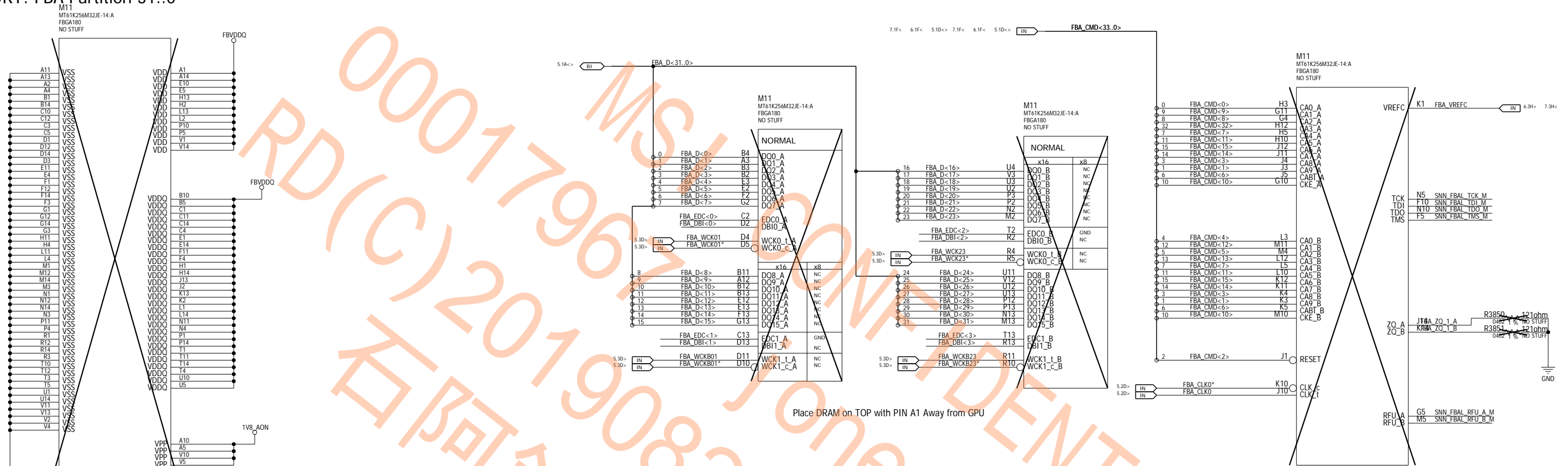


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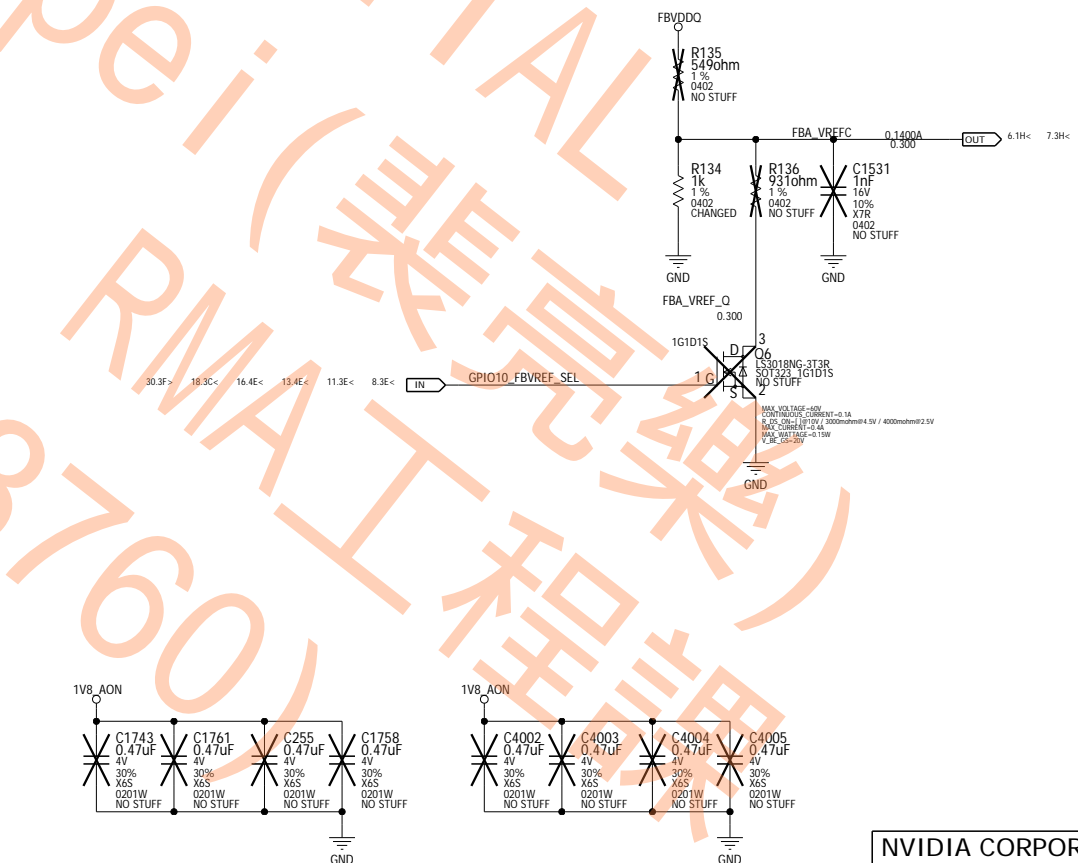
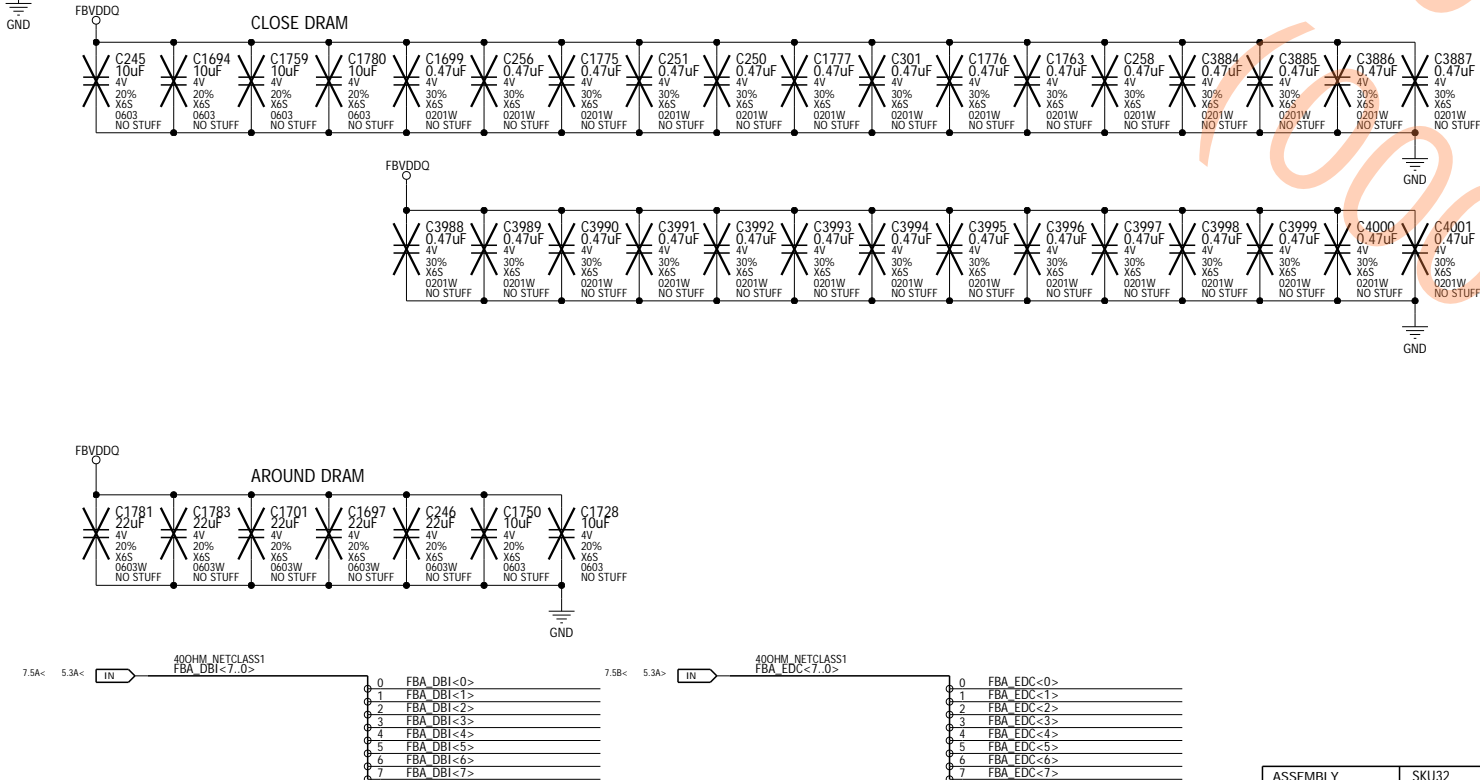
MEMORY: GPU Partition A/B




MEMORY: FBA Partition 31..0



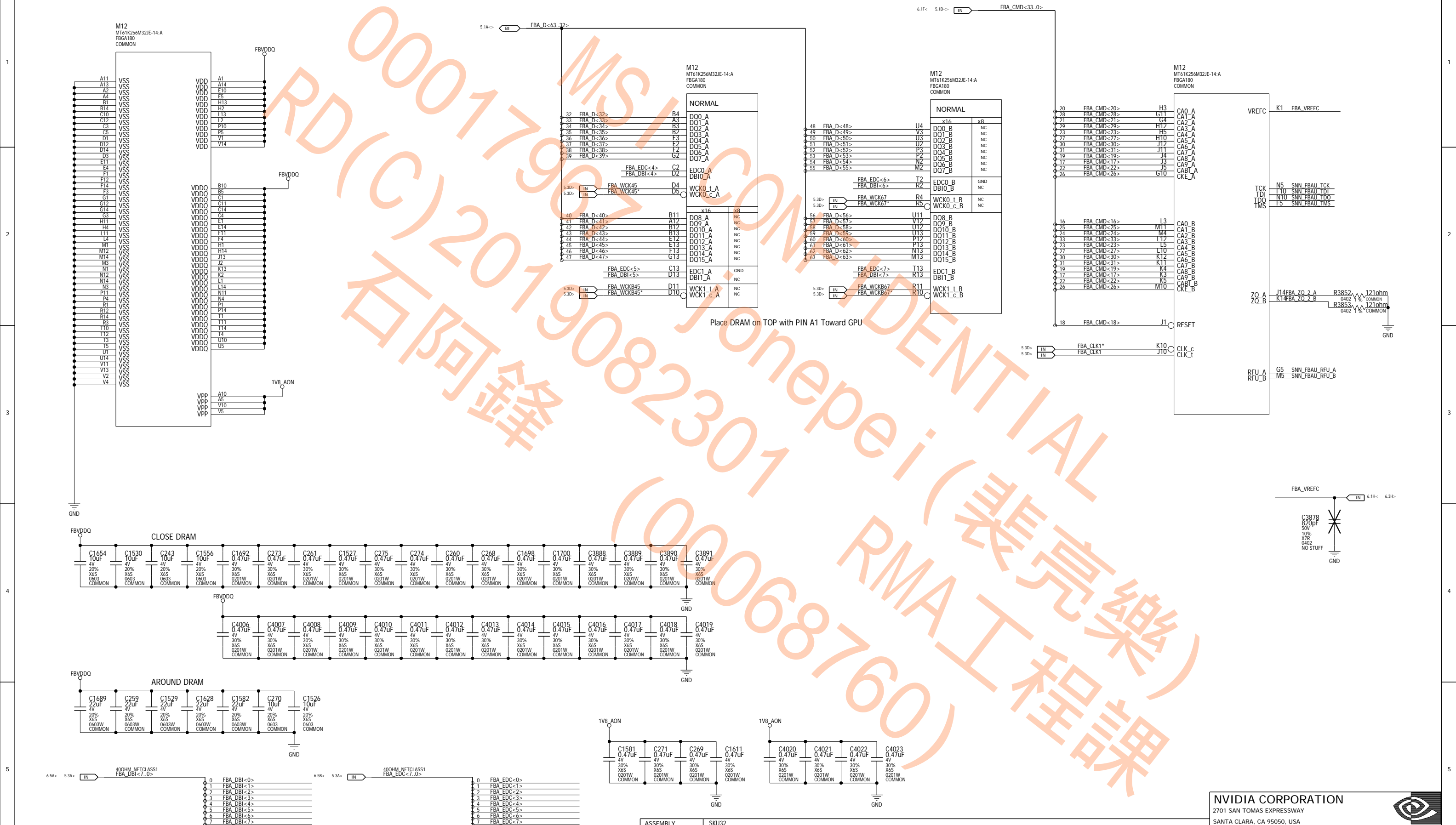
Place DRAM on TOP with PIN A1 Away from GPU



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Nv_PN PCB REV BOM REV	600-1G150-0032-404 PG150-C04 F	PAGE DATE	6 OF 66 14-NOV-2018


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MEMORY: FBA Partition 63..32

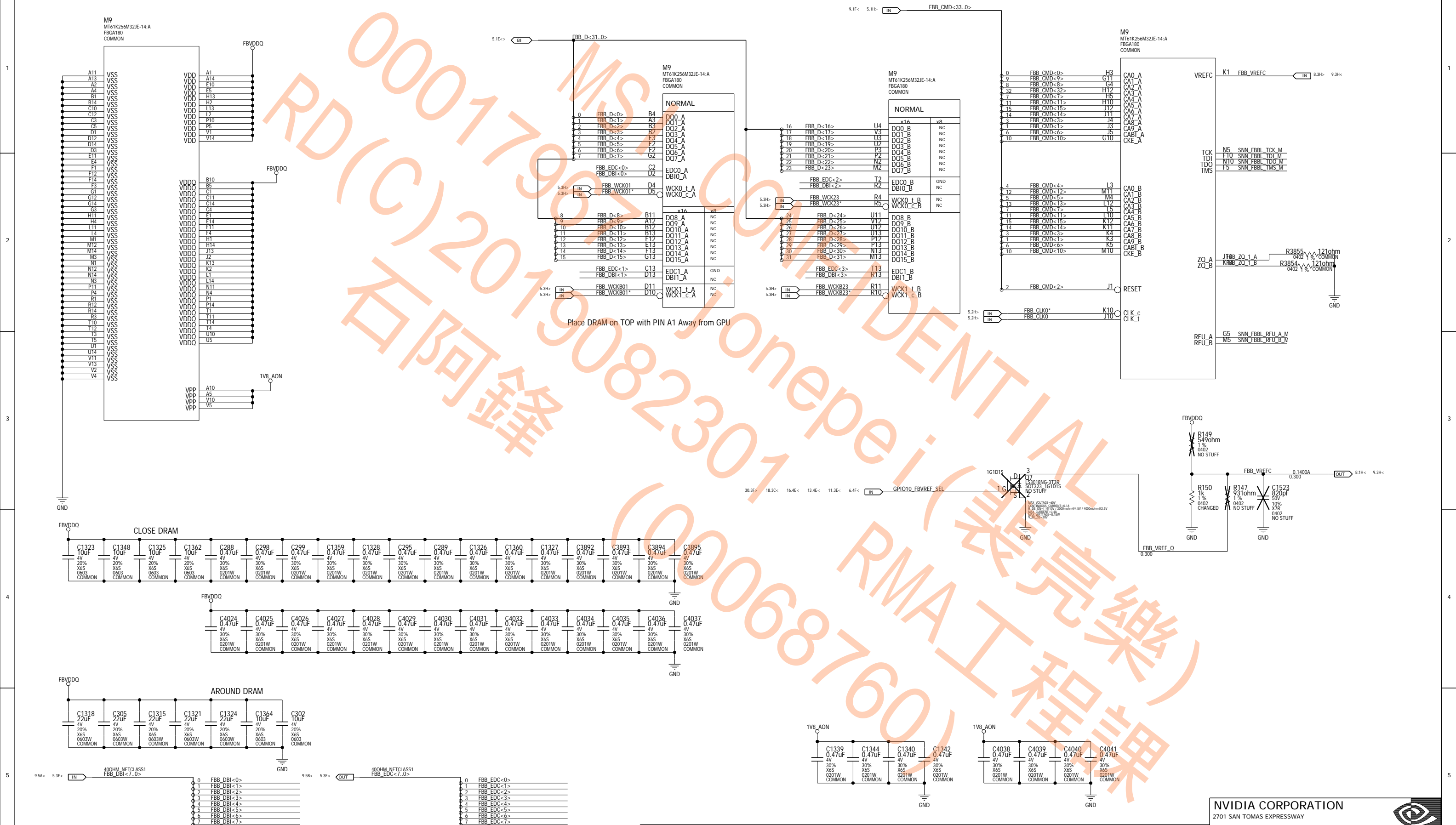


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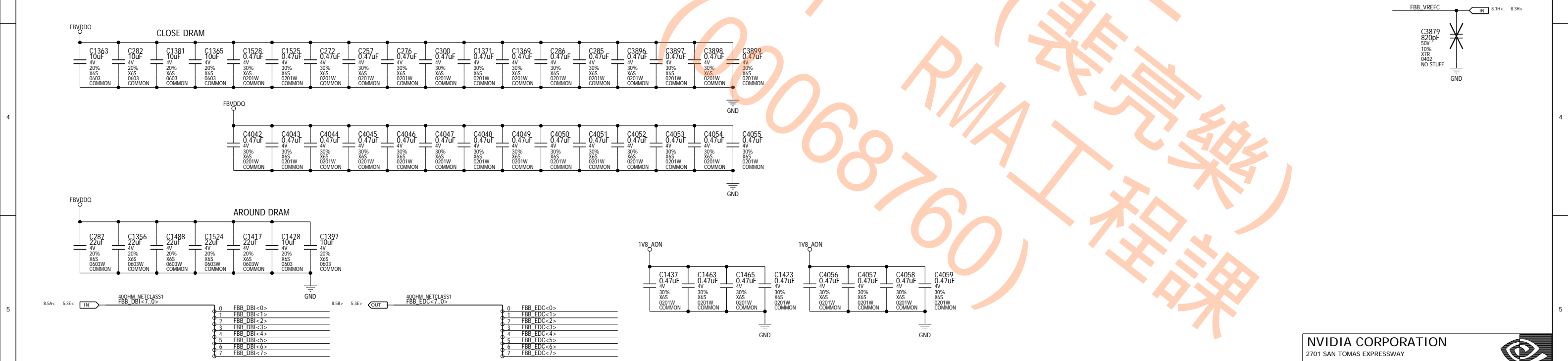
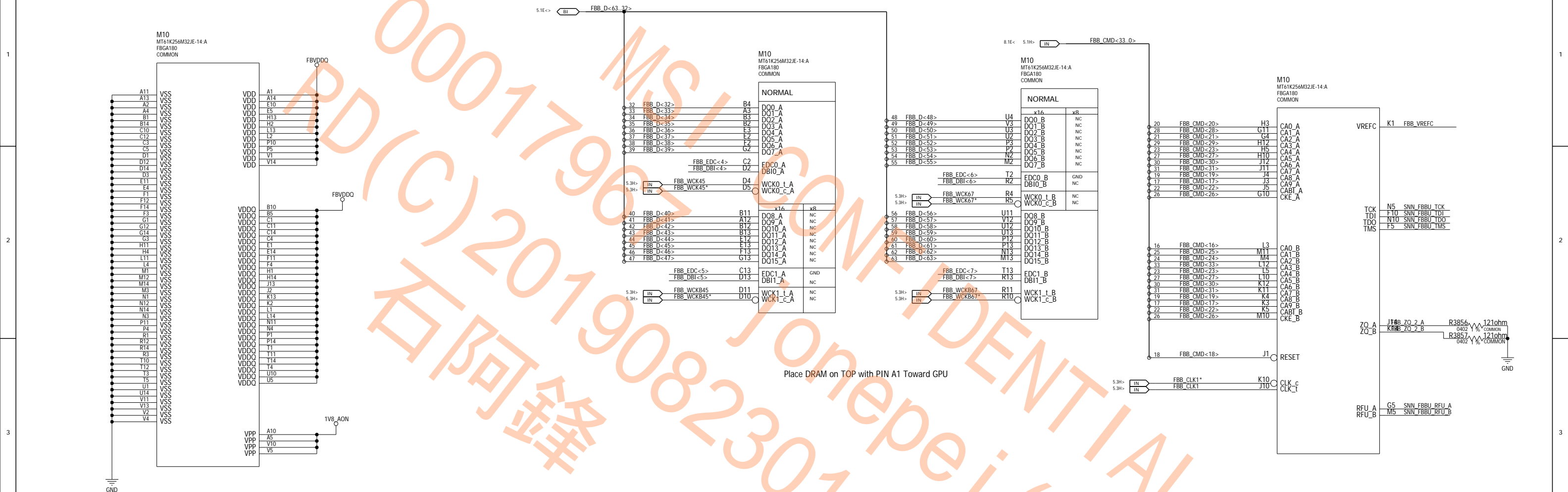
ASSEMBLY	SKU32
PAGE DETAIL	MEMORY: FBA PARTITION[63:32]

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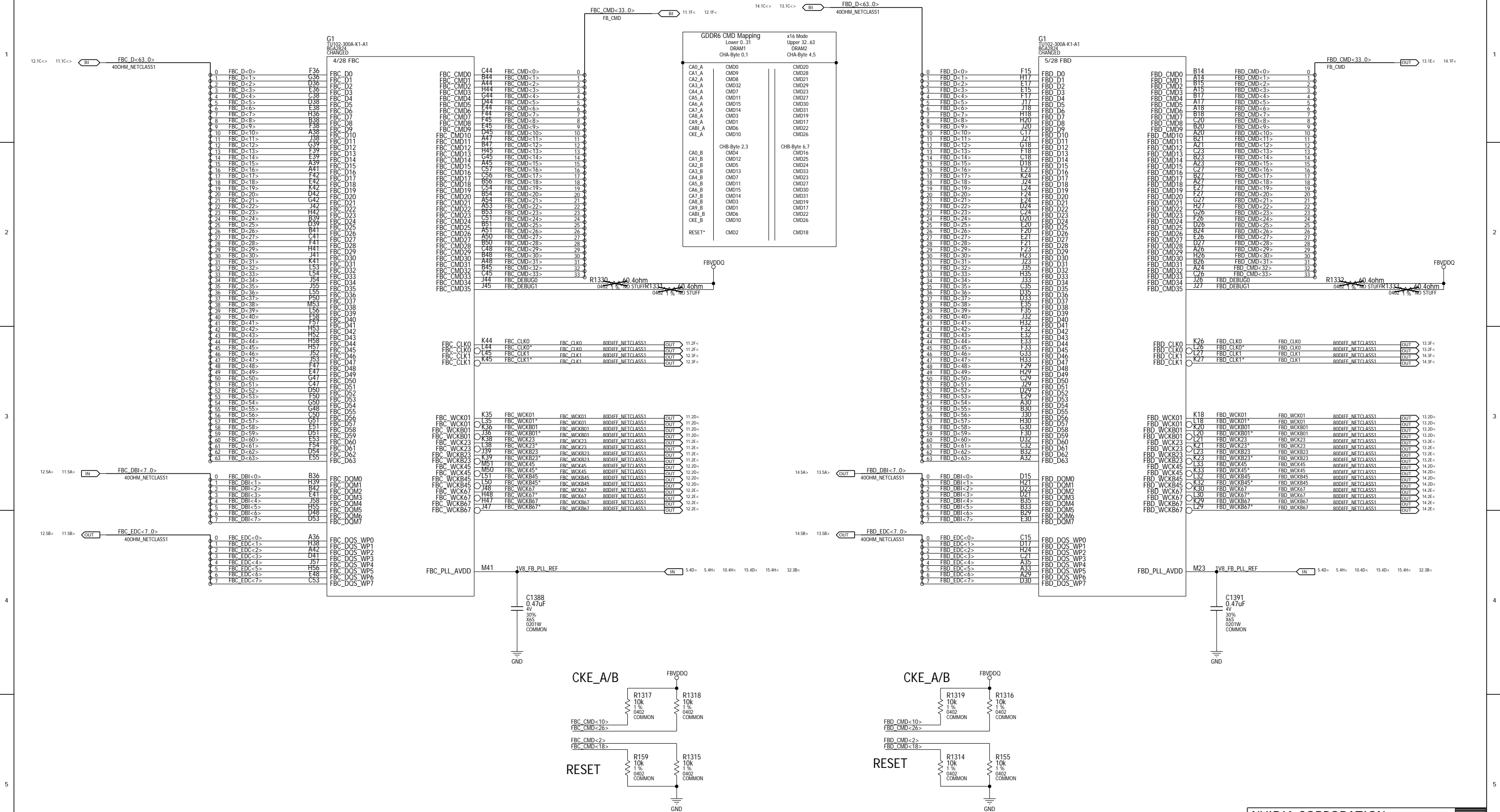
MEMORY: FBB Partition 31..0



MEMORY: FBB Partition 63..32



MEMORY: GPU Partition C/D



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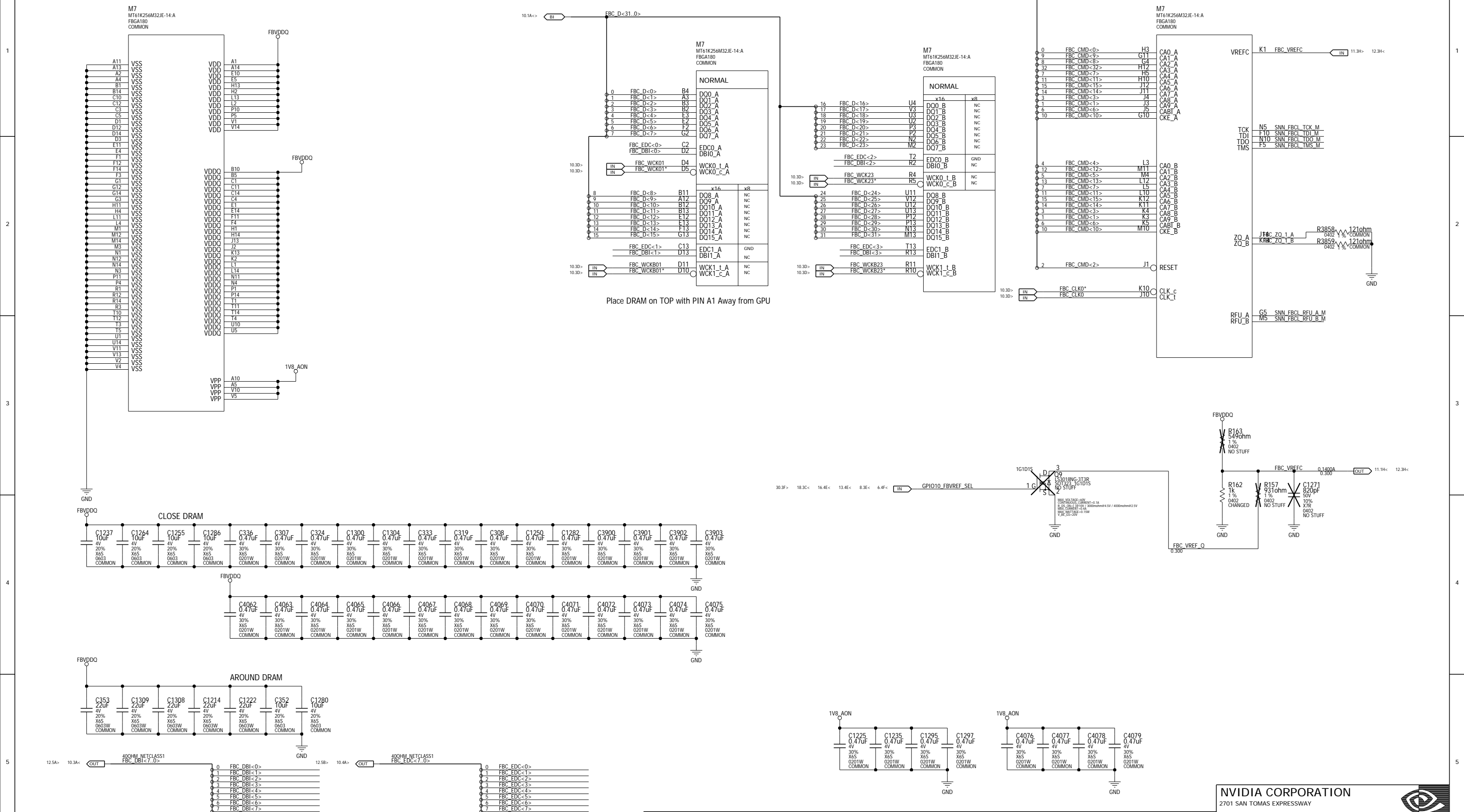
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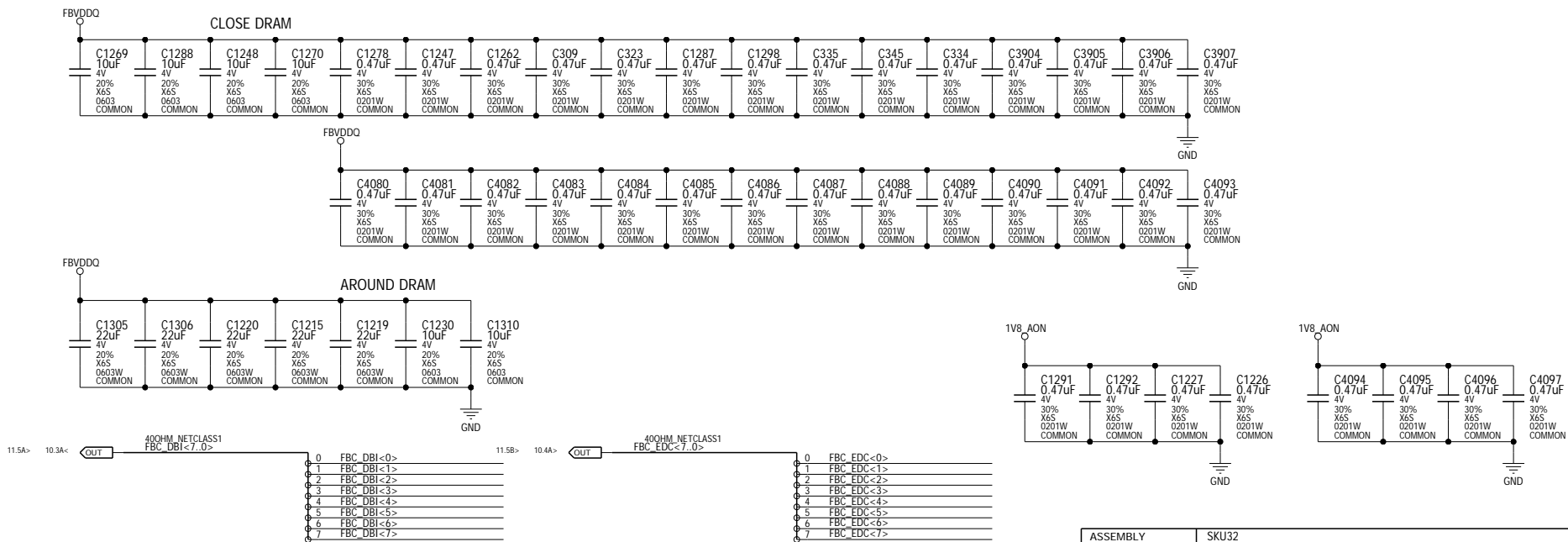
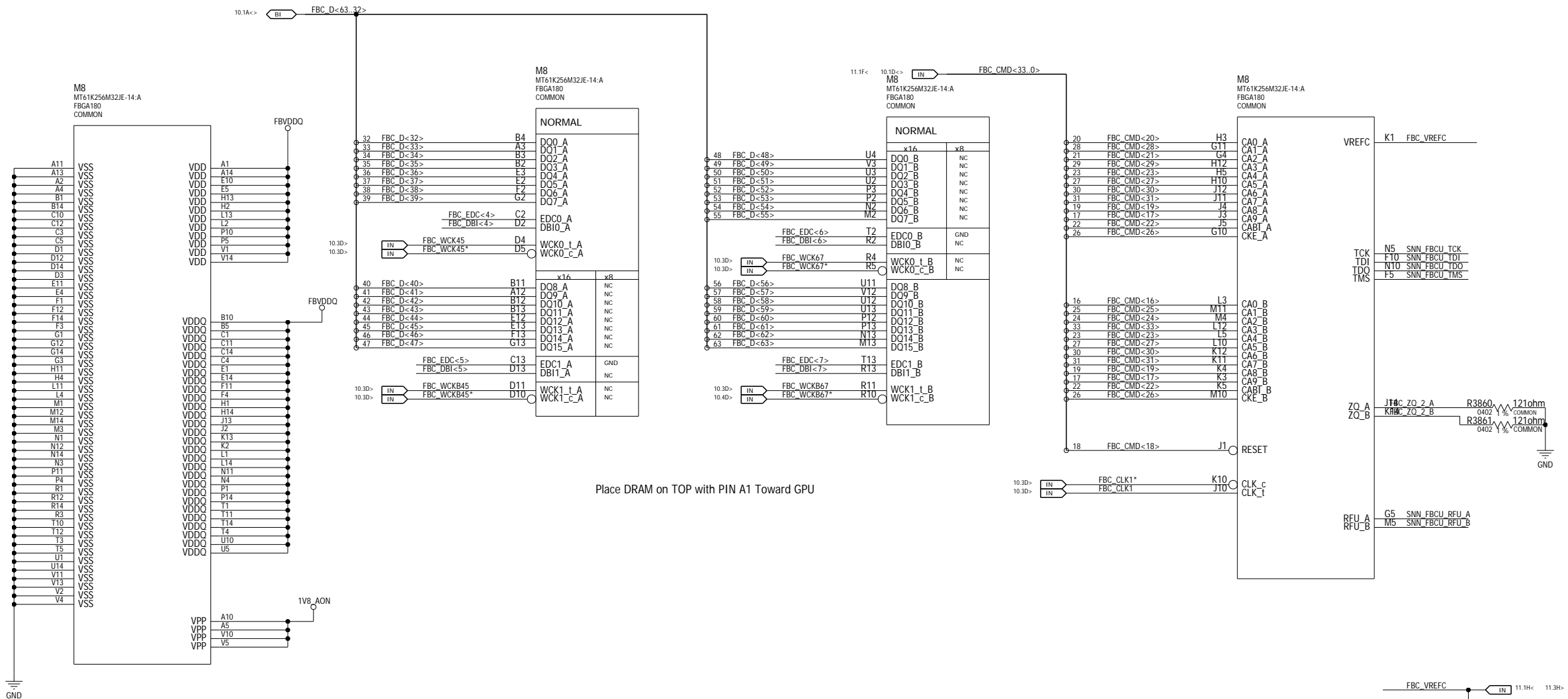
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MEMORY: FBC Partition 31..0



MEMORY: FBC Partition 63..32



ASSEMBLY	SKU32
PAGE DETAIL	MEMORY: FBC PARTITION[63:32]

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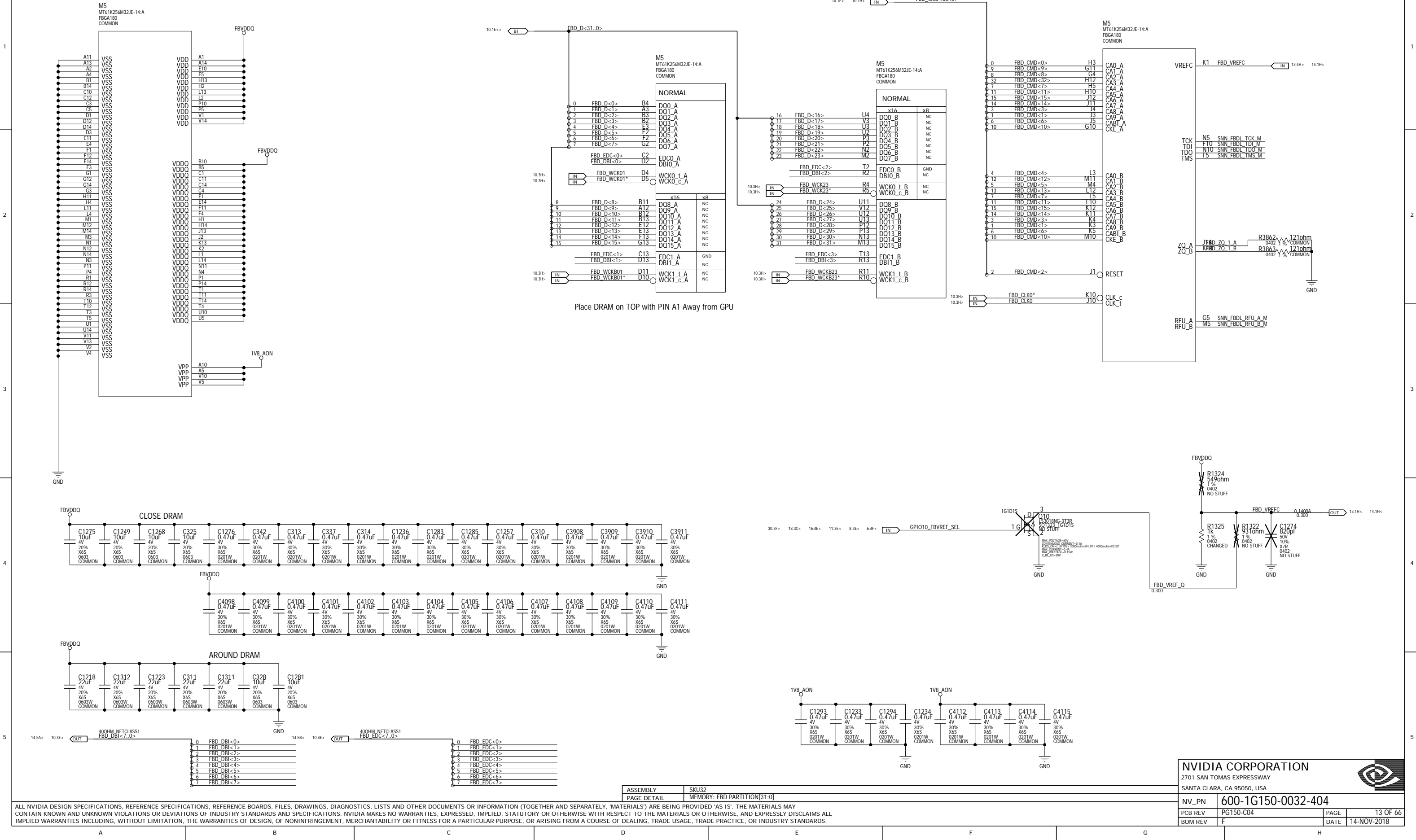
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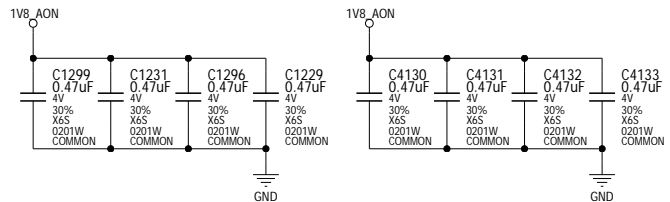
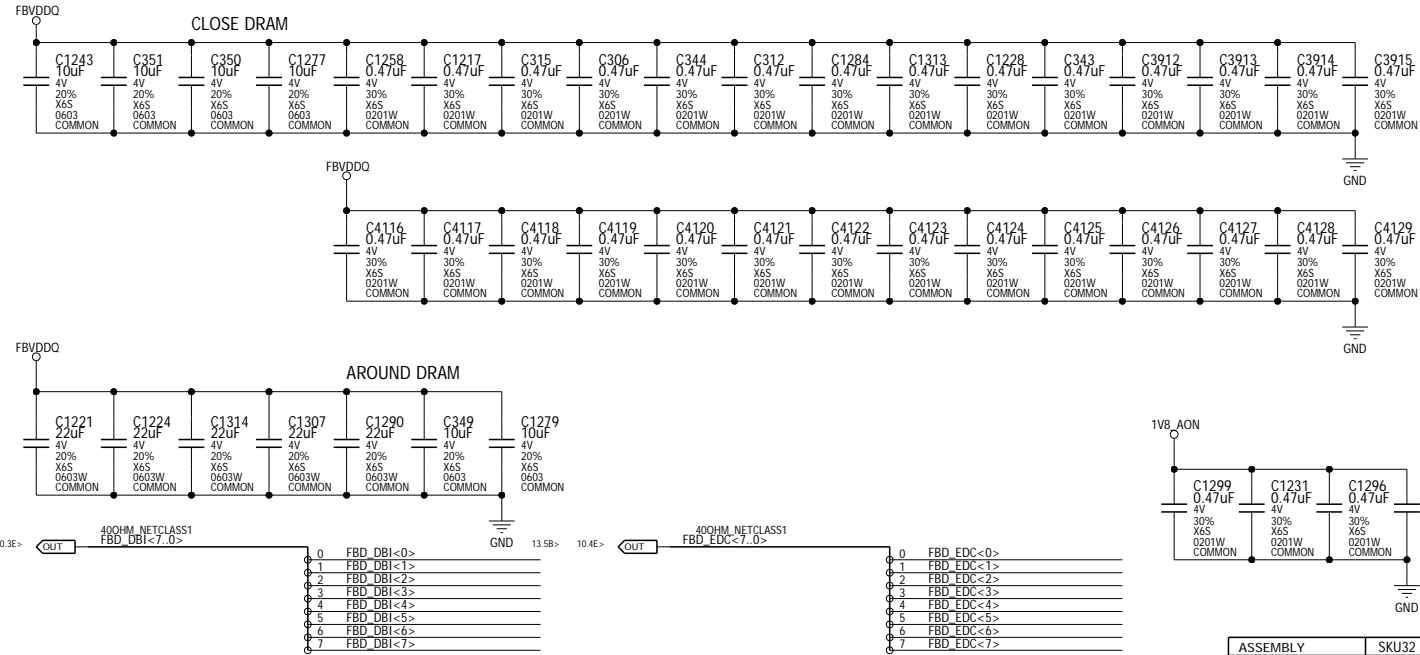
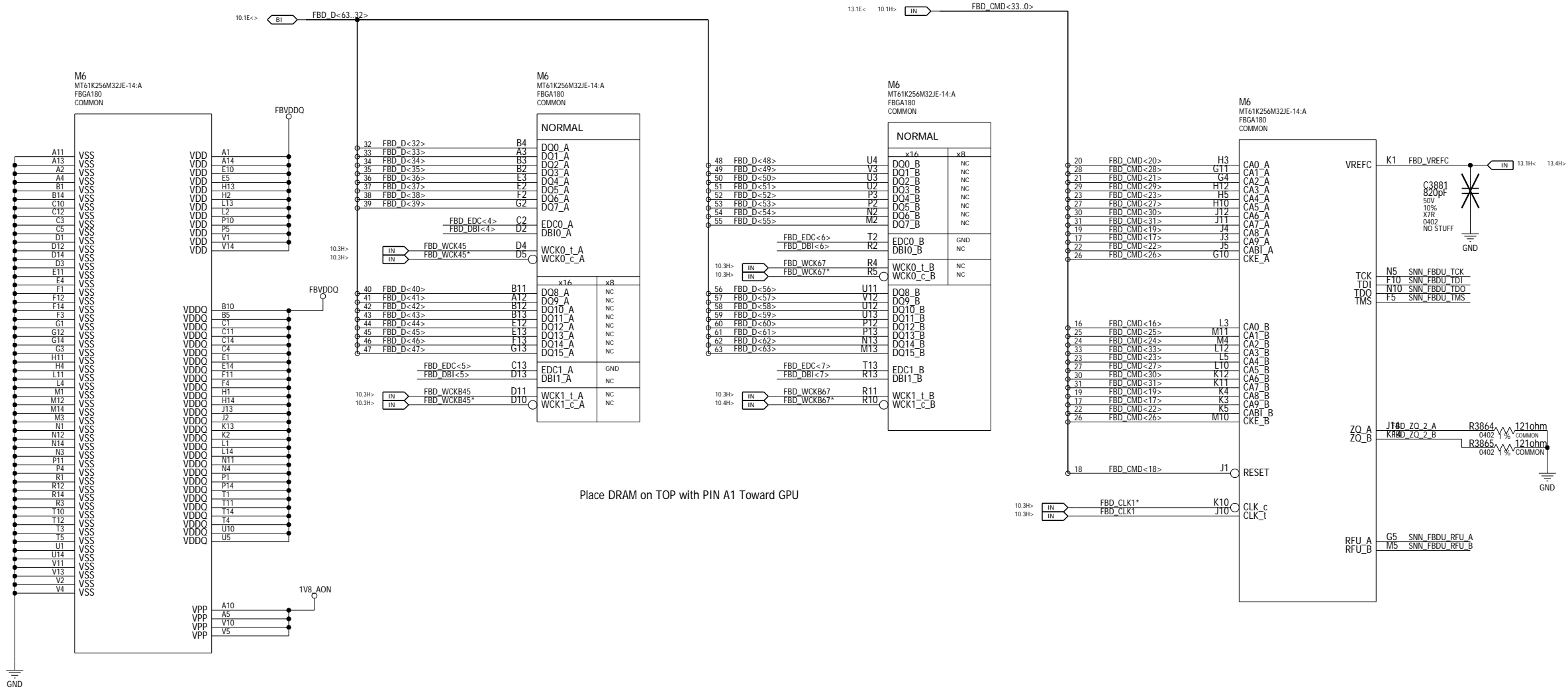
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MEMORY: FBD Partition 31..0



MEMORY: FBD Partition 63..32



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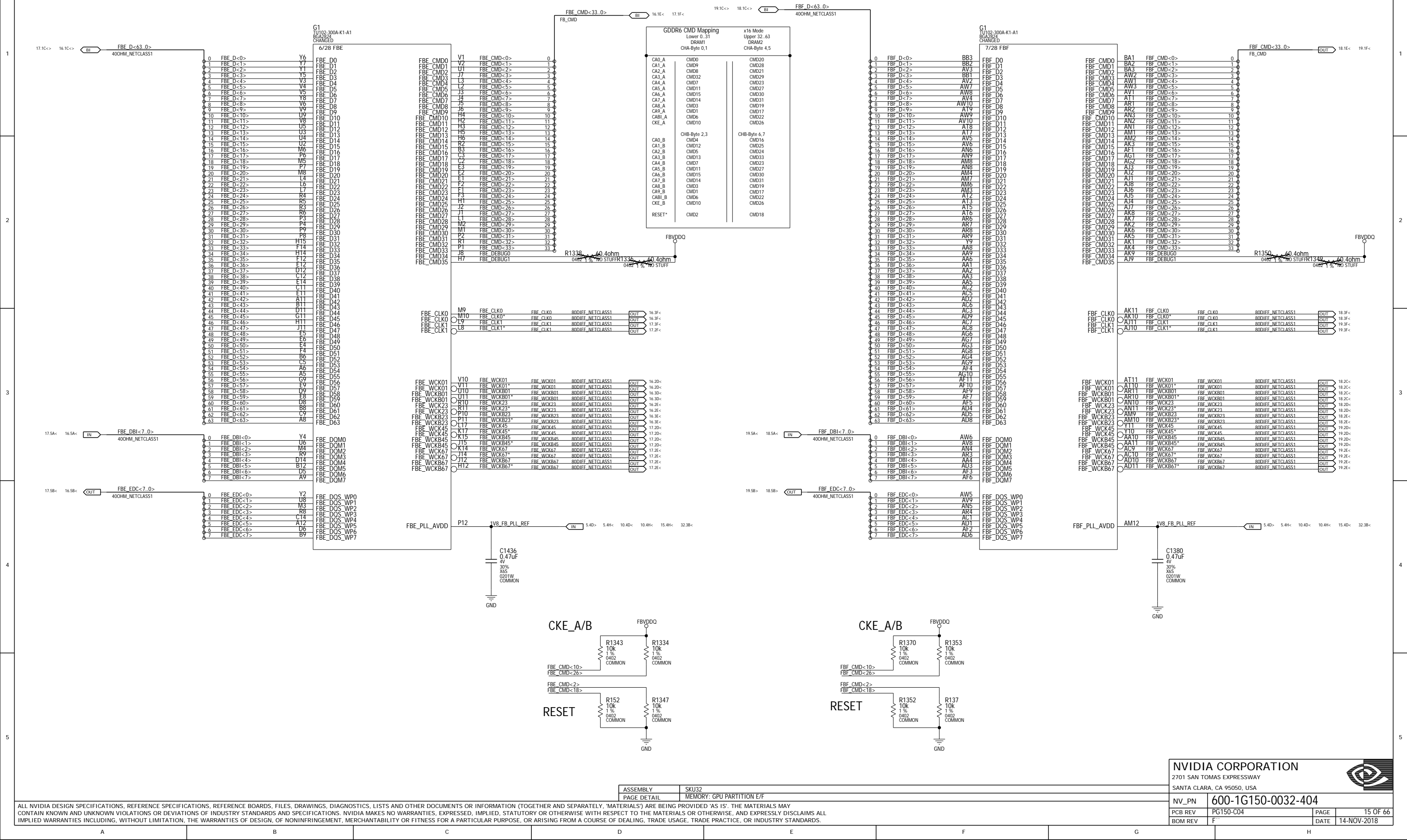
14-NOV-2018

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ASSEMBLY	SKU32
PAGE DETAIL	MEMORY: FBD PARTITION[63:32]

MEMORY: GPU Partition E/F



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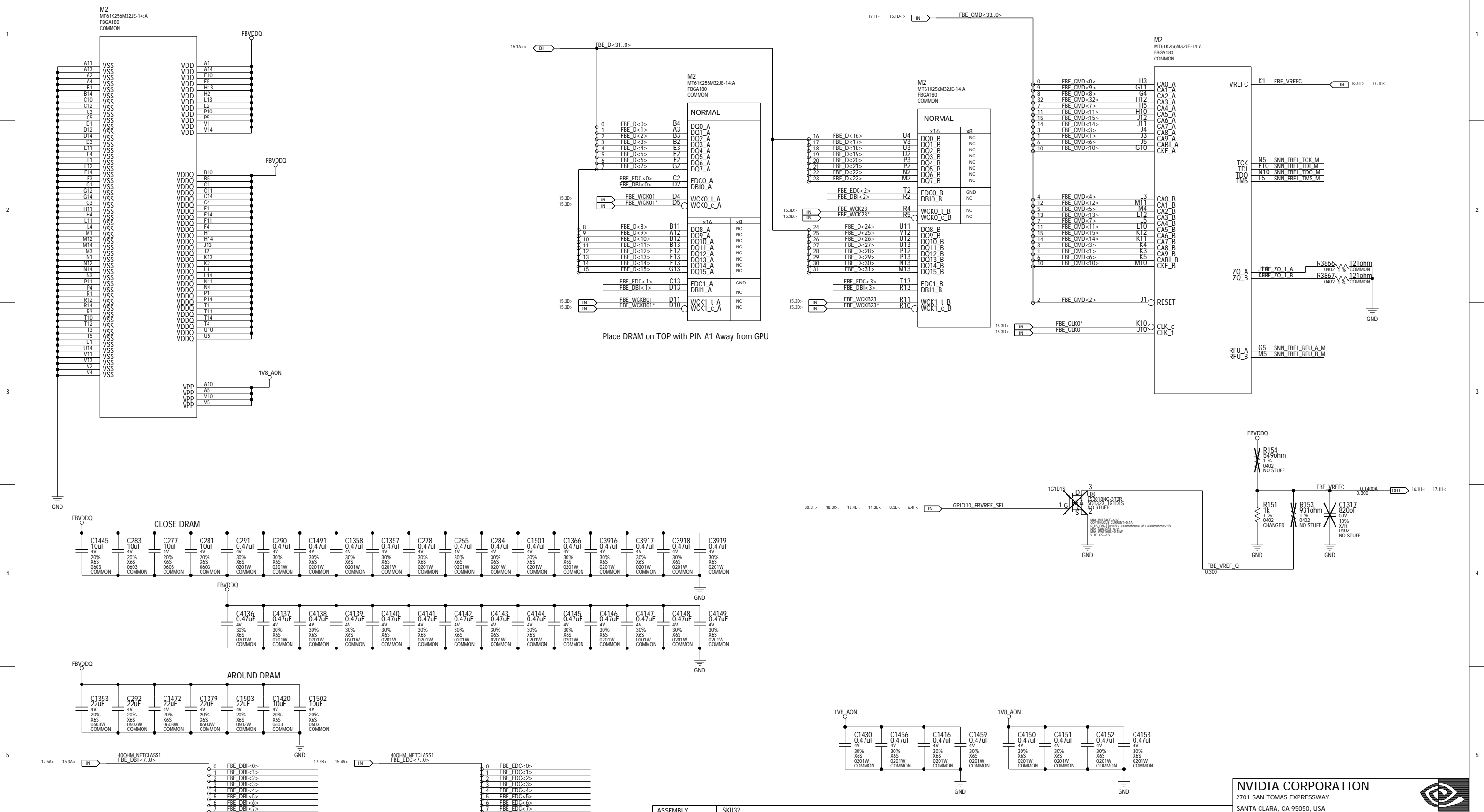
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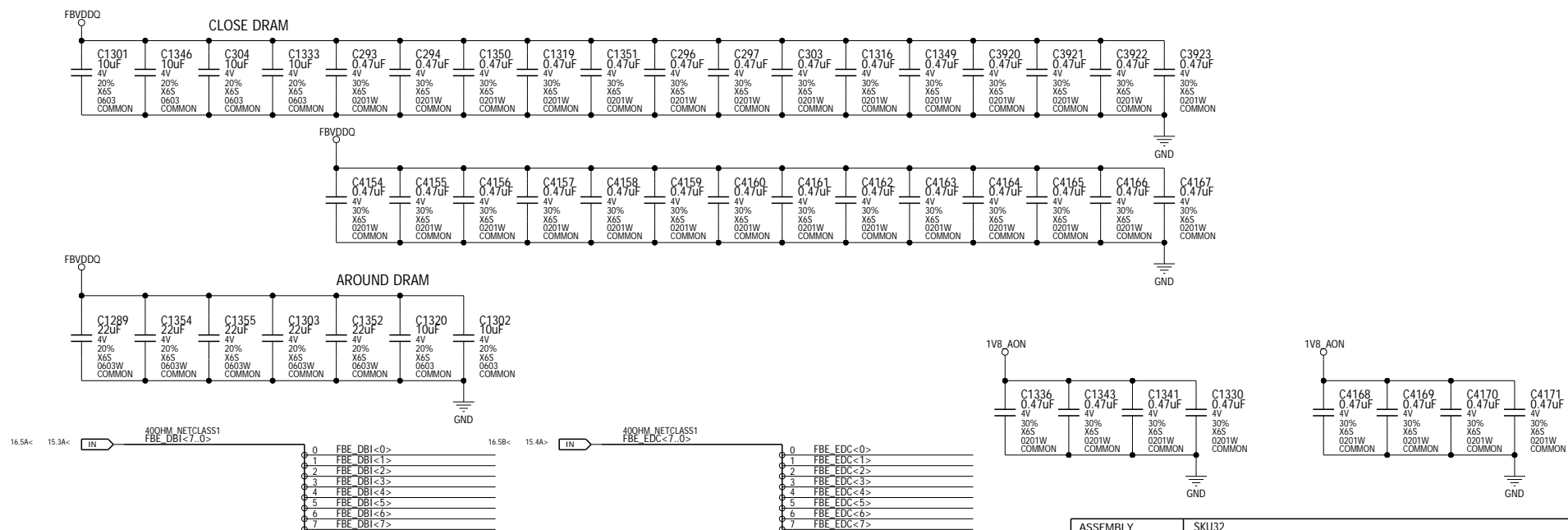
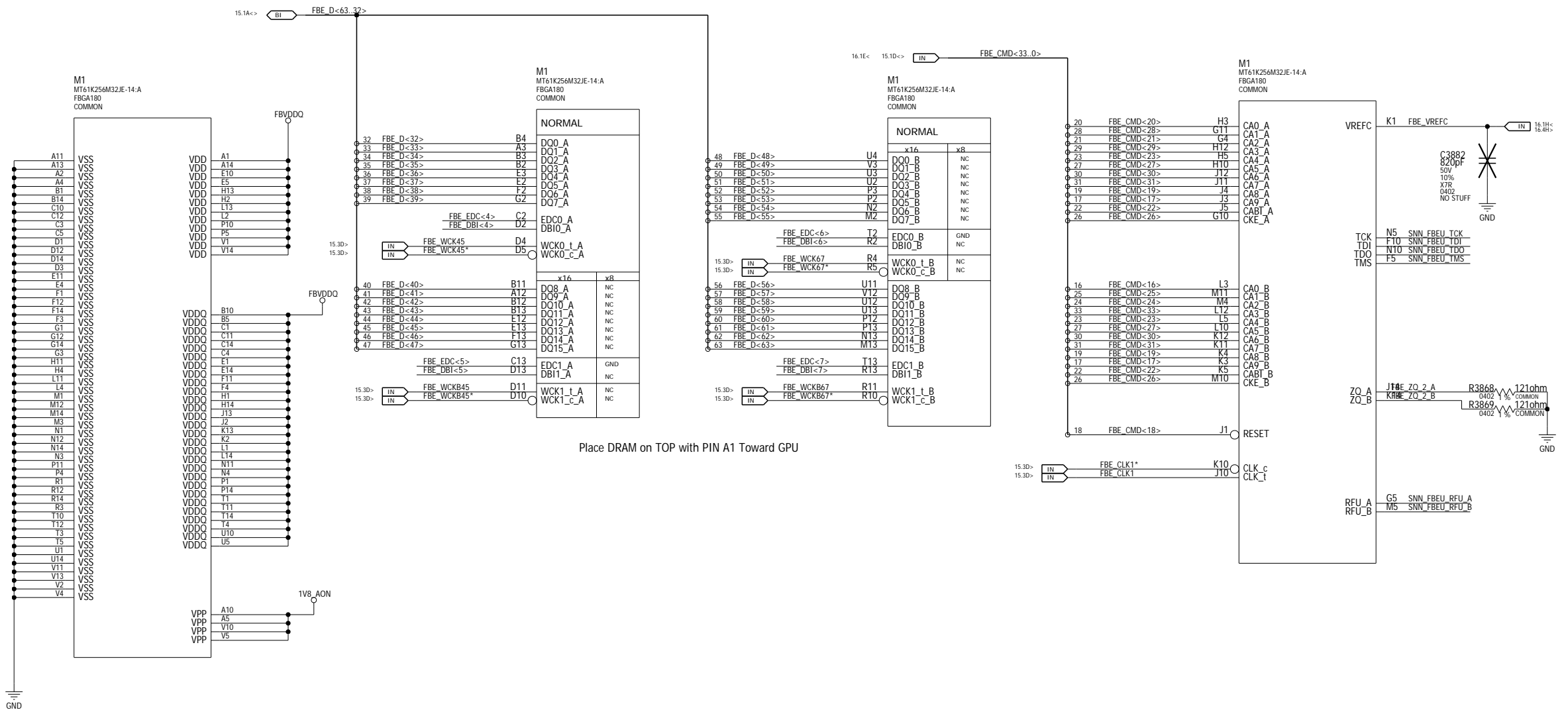
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MEMORY: FBE Partition 31..0



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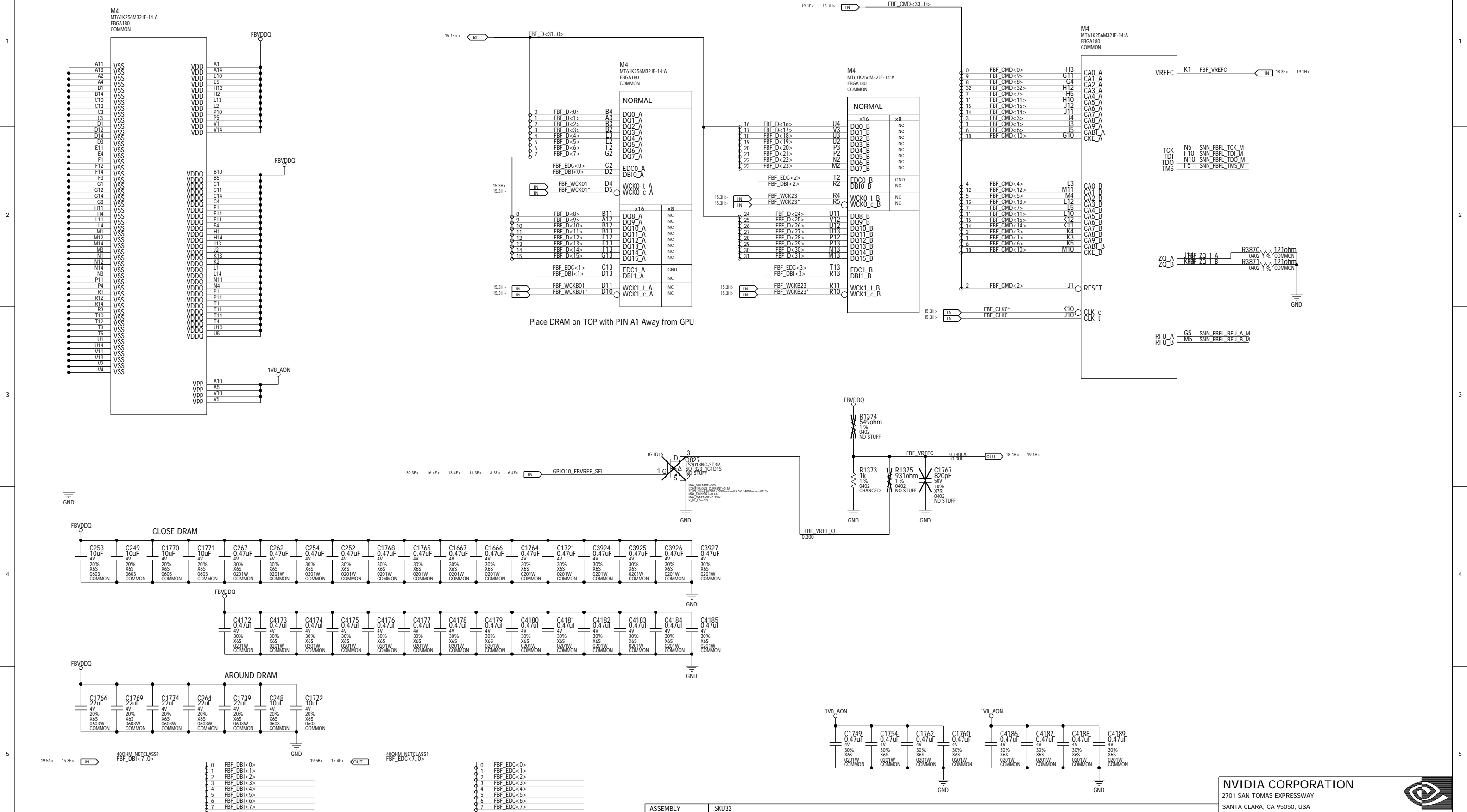
MEMORY: FBE Partition 63..32



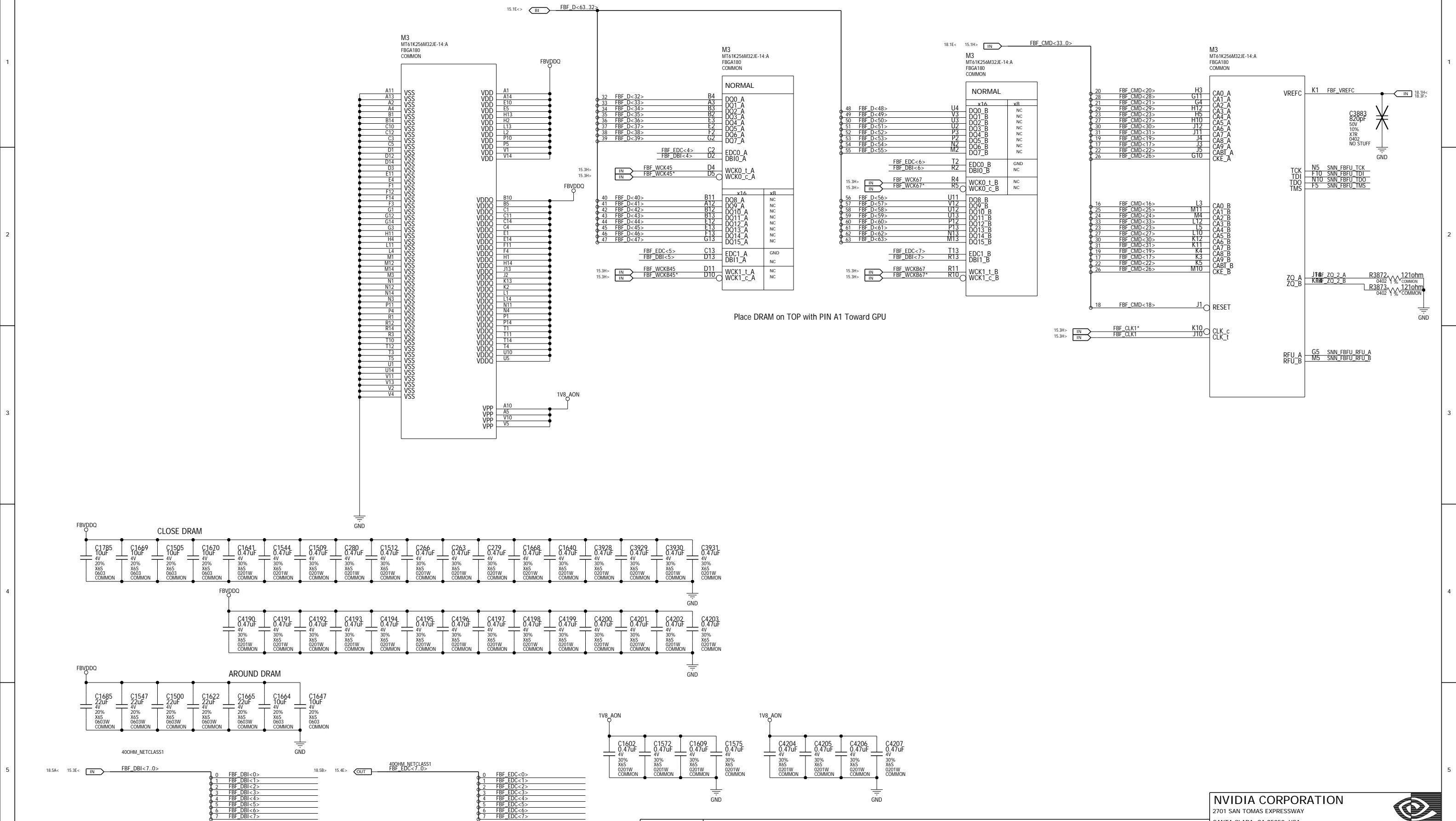
ASSEMBLY	SKU32
PAGE DETAIL	MEMORY: FBE PARTITION[63:32]

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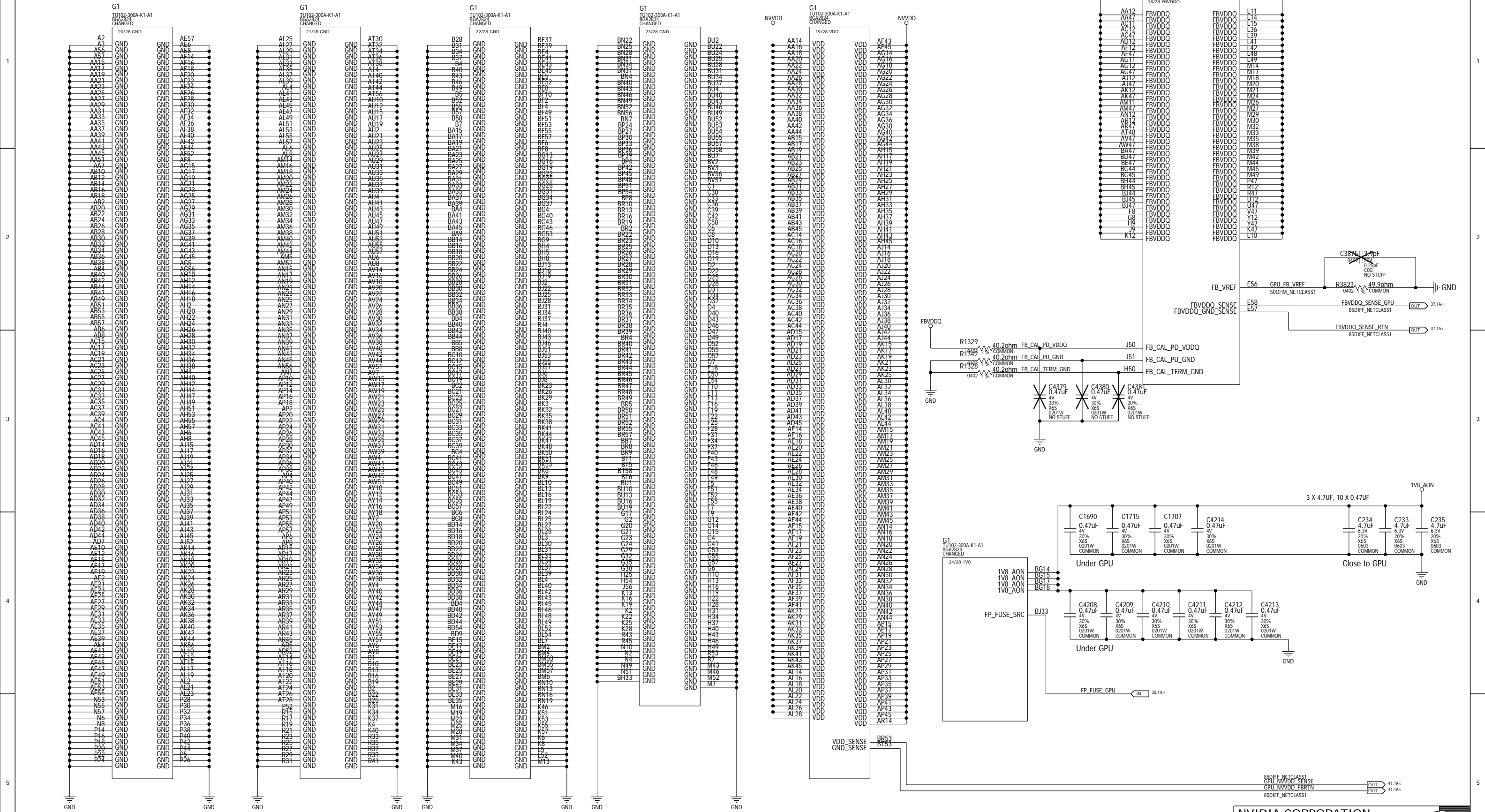
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MEMORY: FBF Partition 63..32

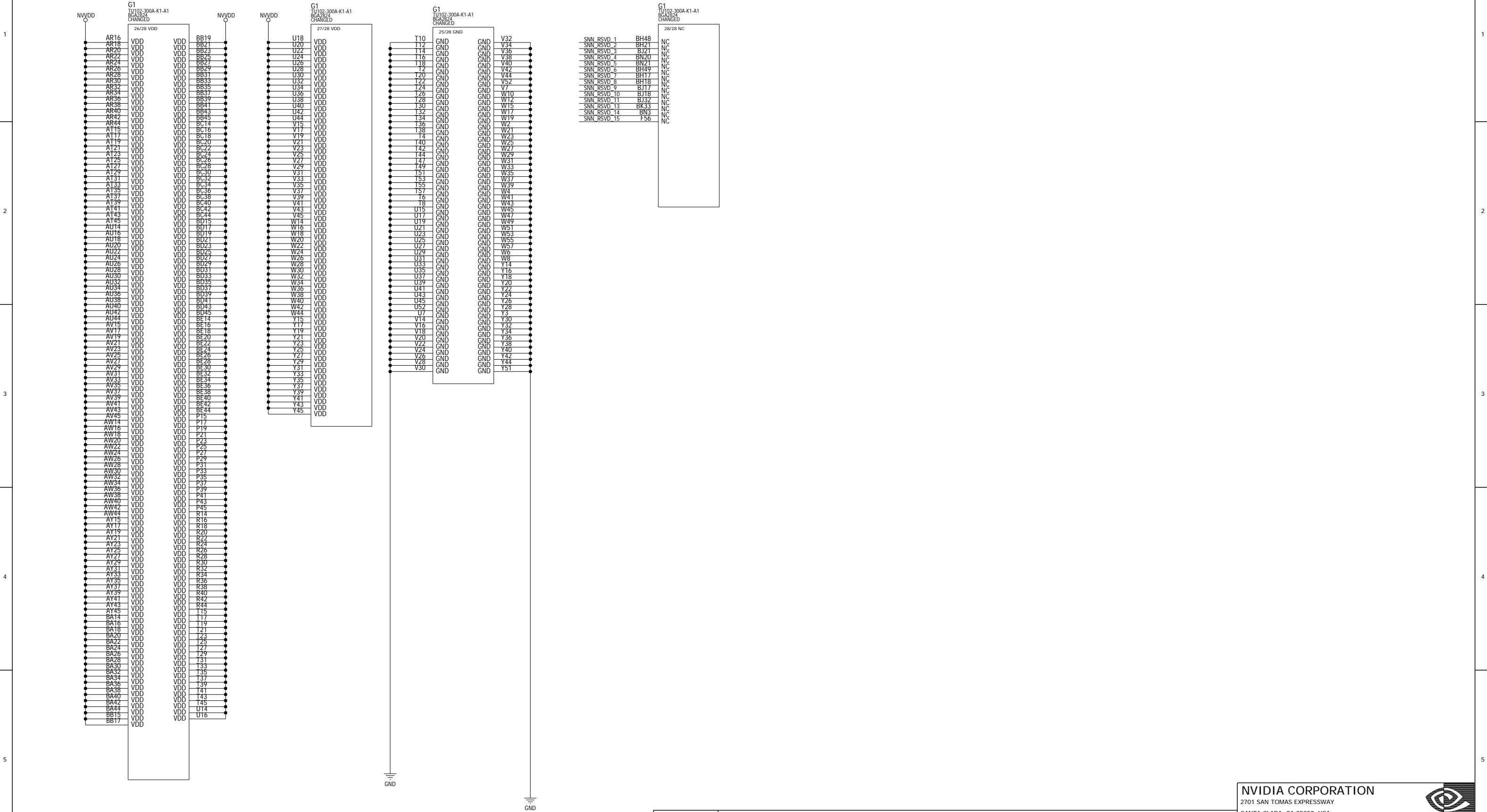


GPU PWR and GND



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GPU PWR GND NCs



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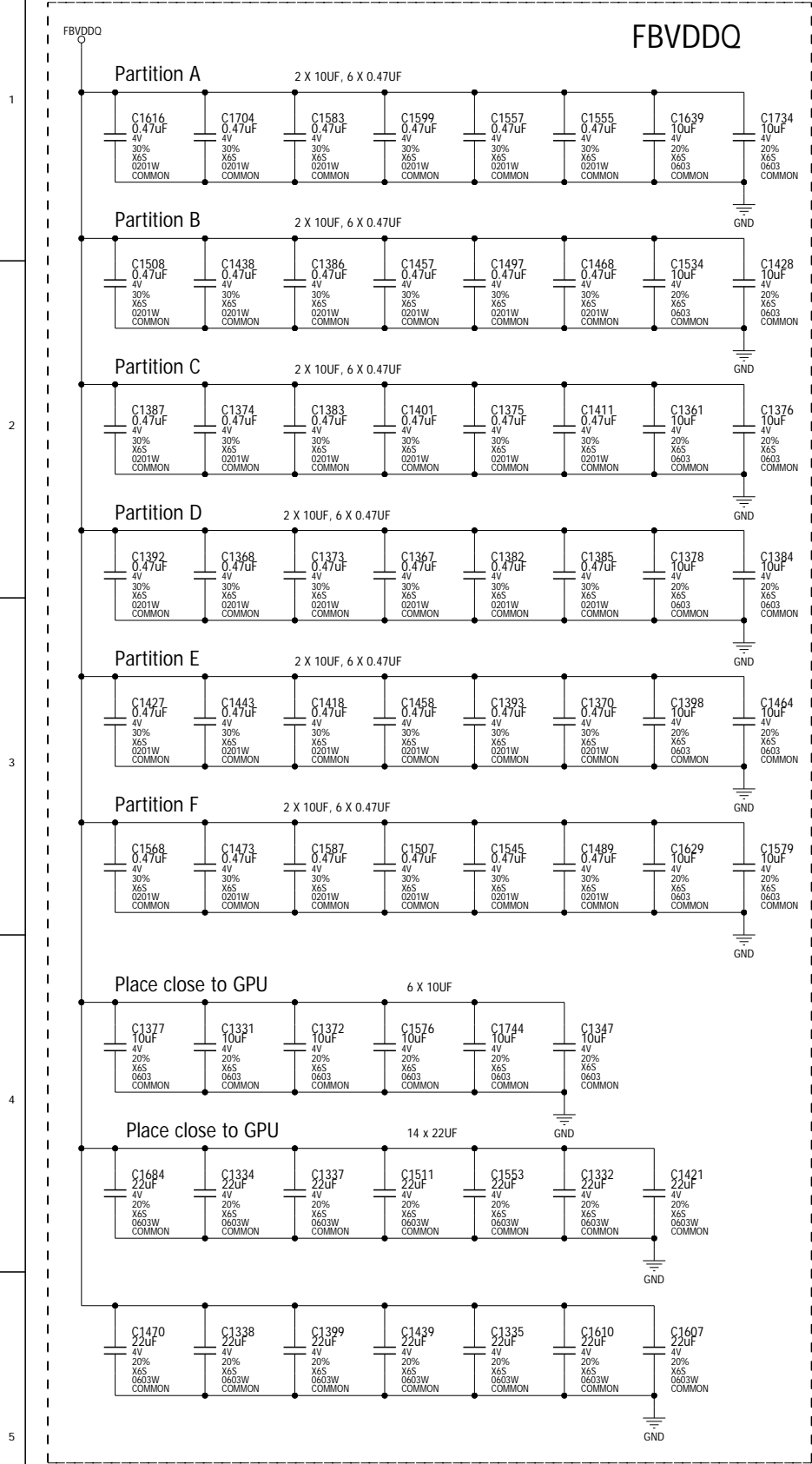
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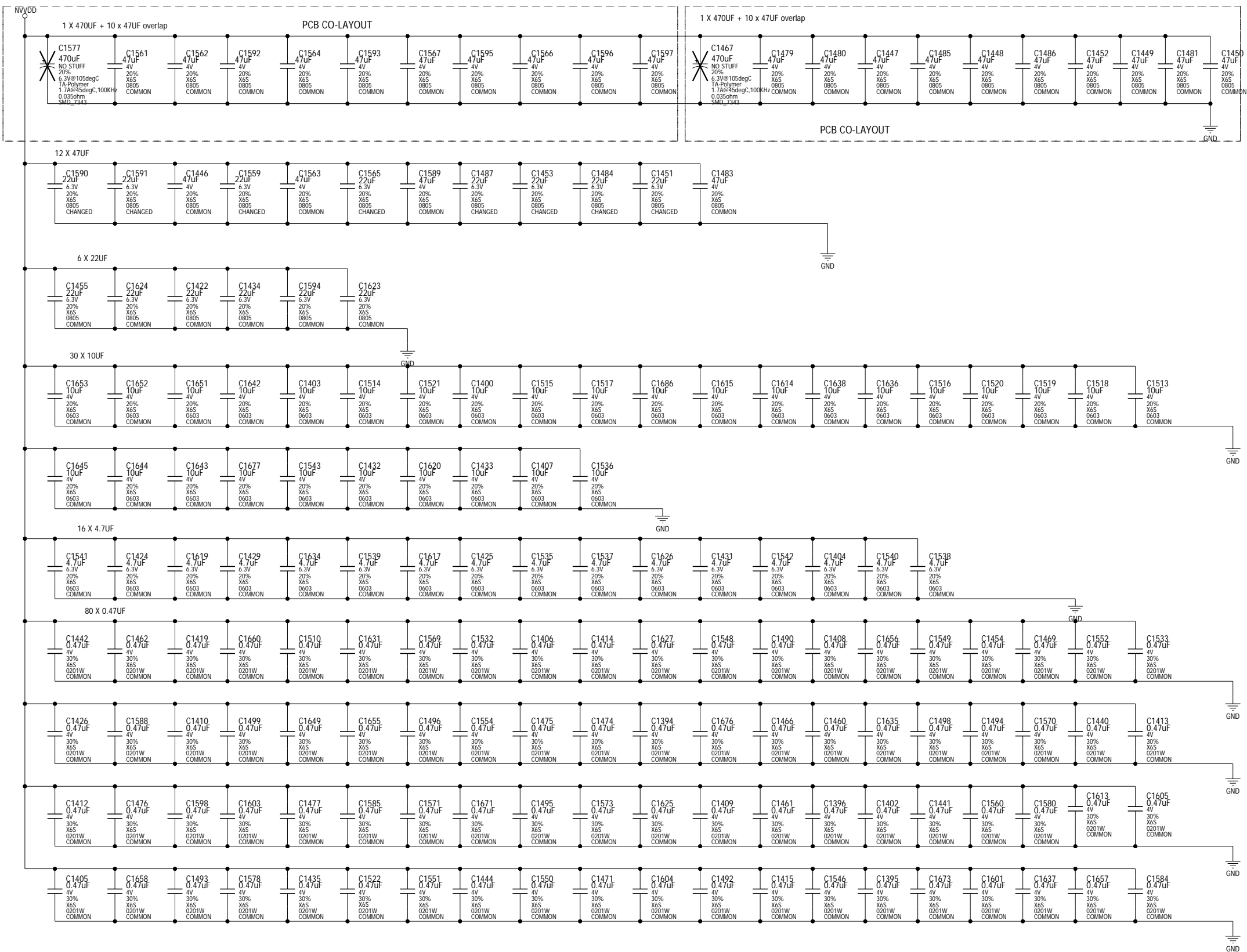
DATE

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GPU Decoupling



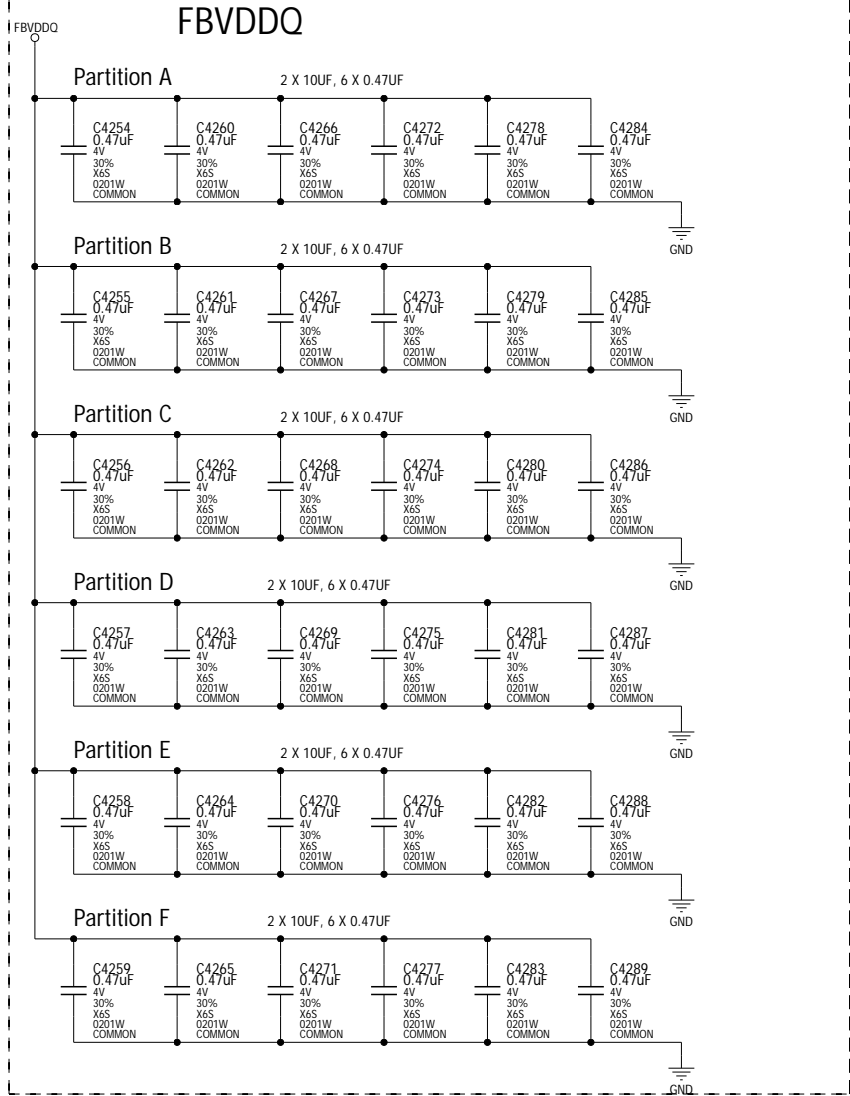
NVVD



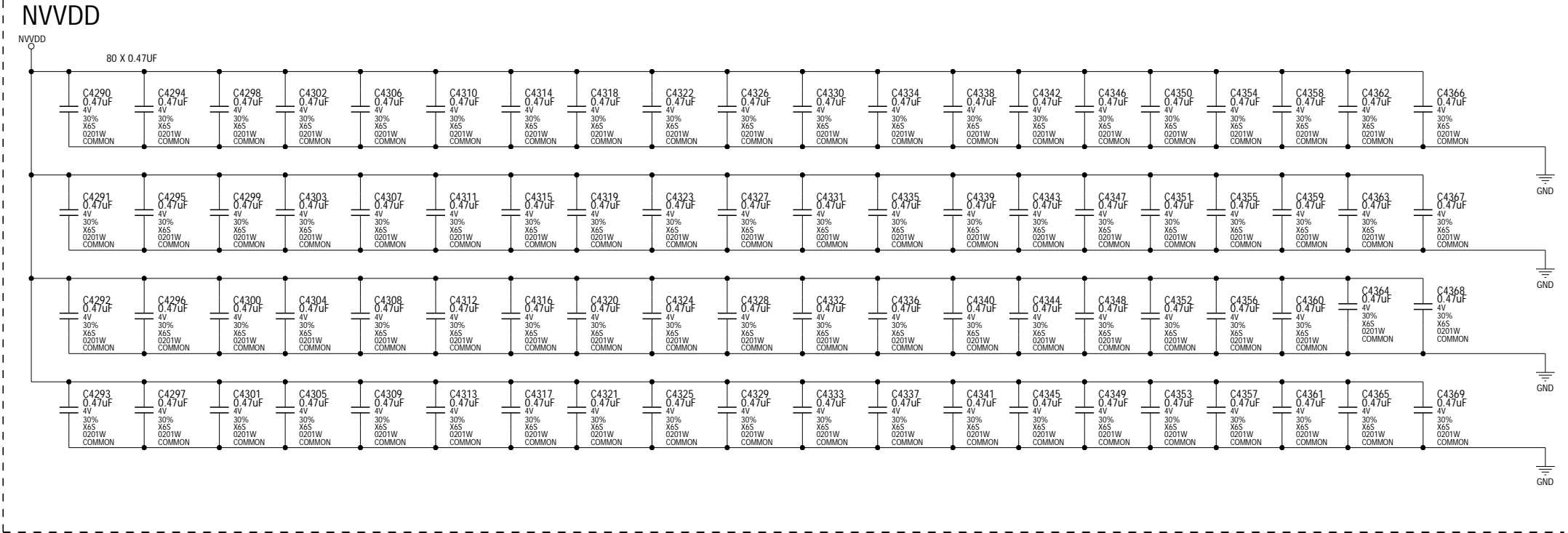
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GPU Decoupling

FBVDDQ



NVVD



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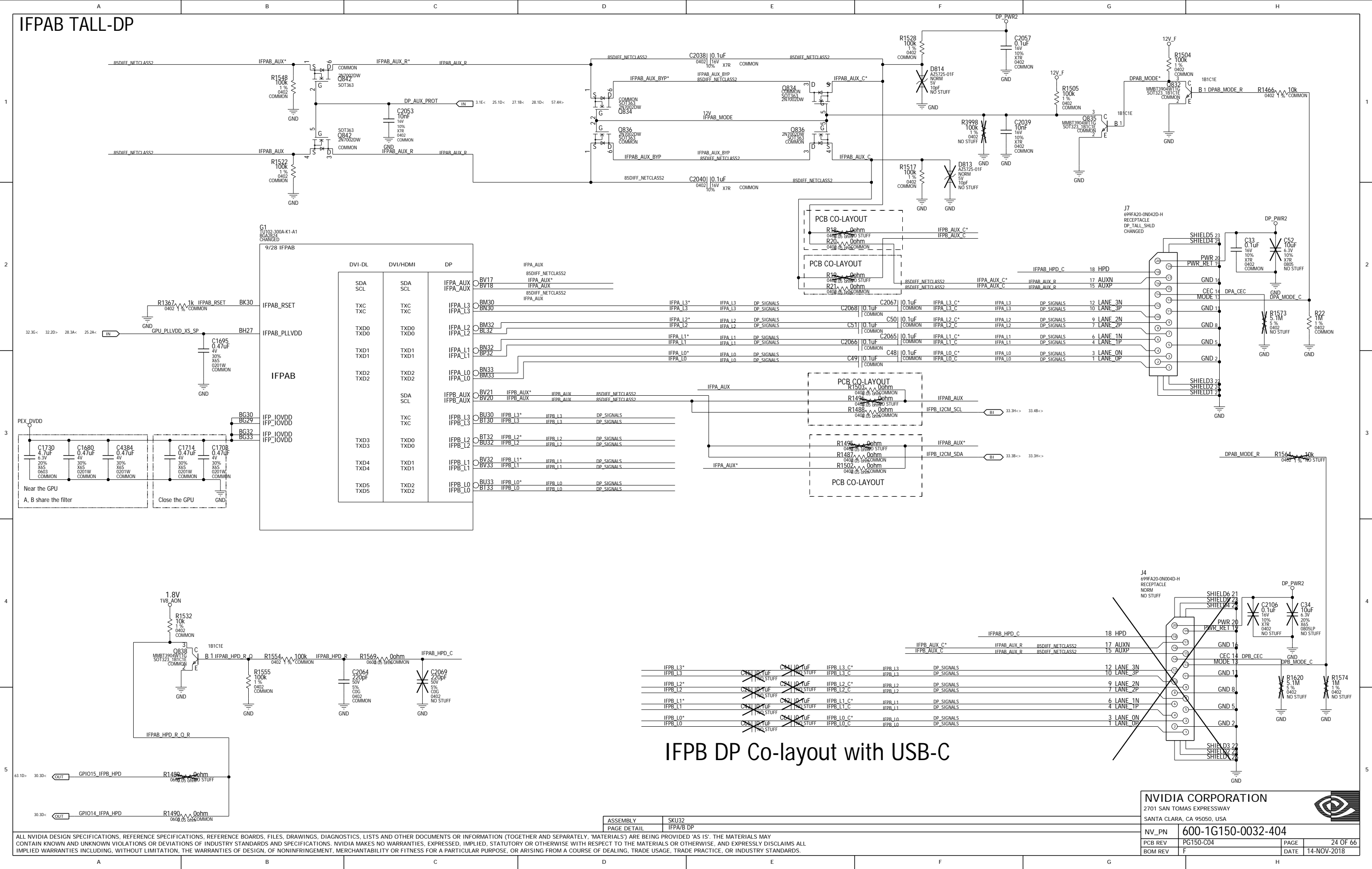
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IFPAB TALL-DP

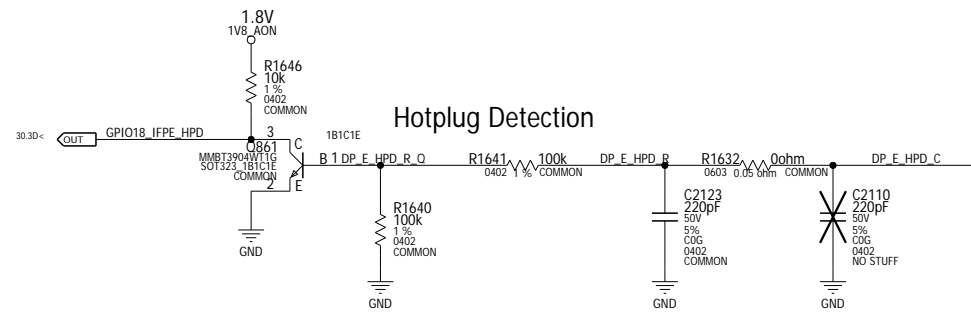
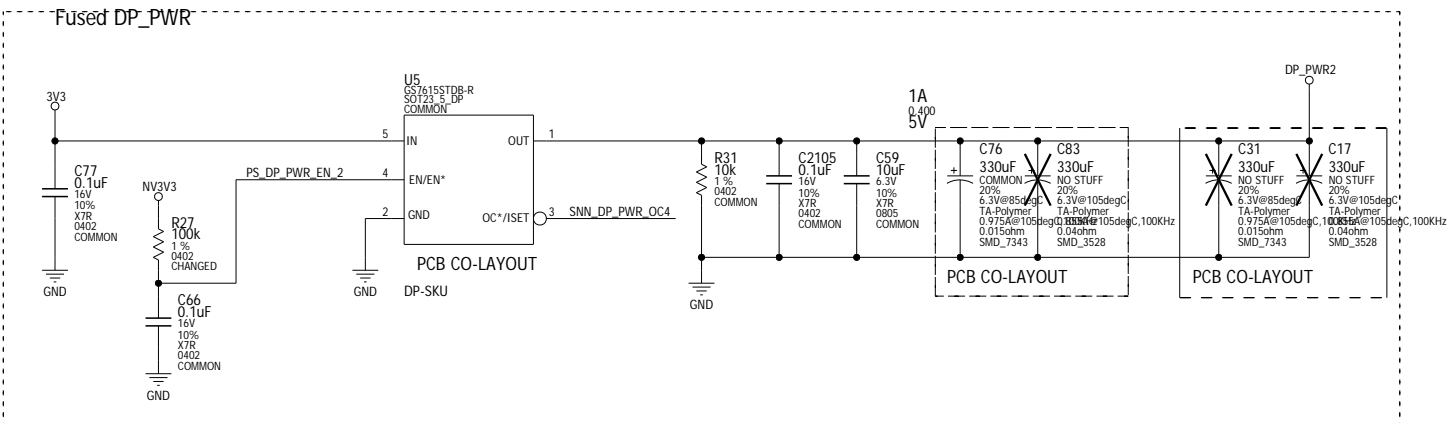
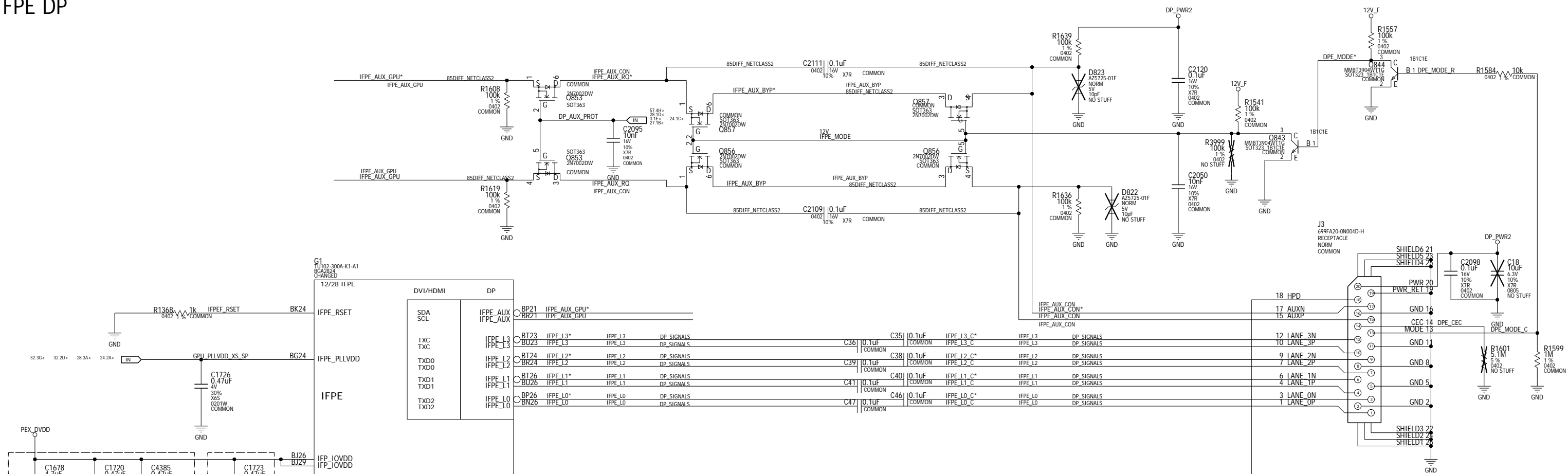


IFPB DP Co-layout with USB-C

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ASSEMBLY	SKU32
PAGE DETAIL	IFPA/B DP

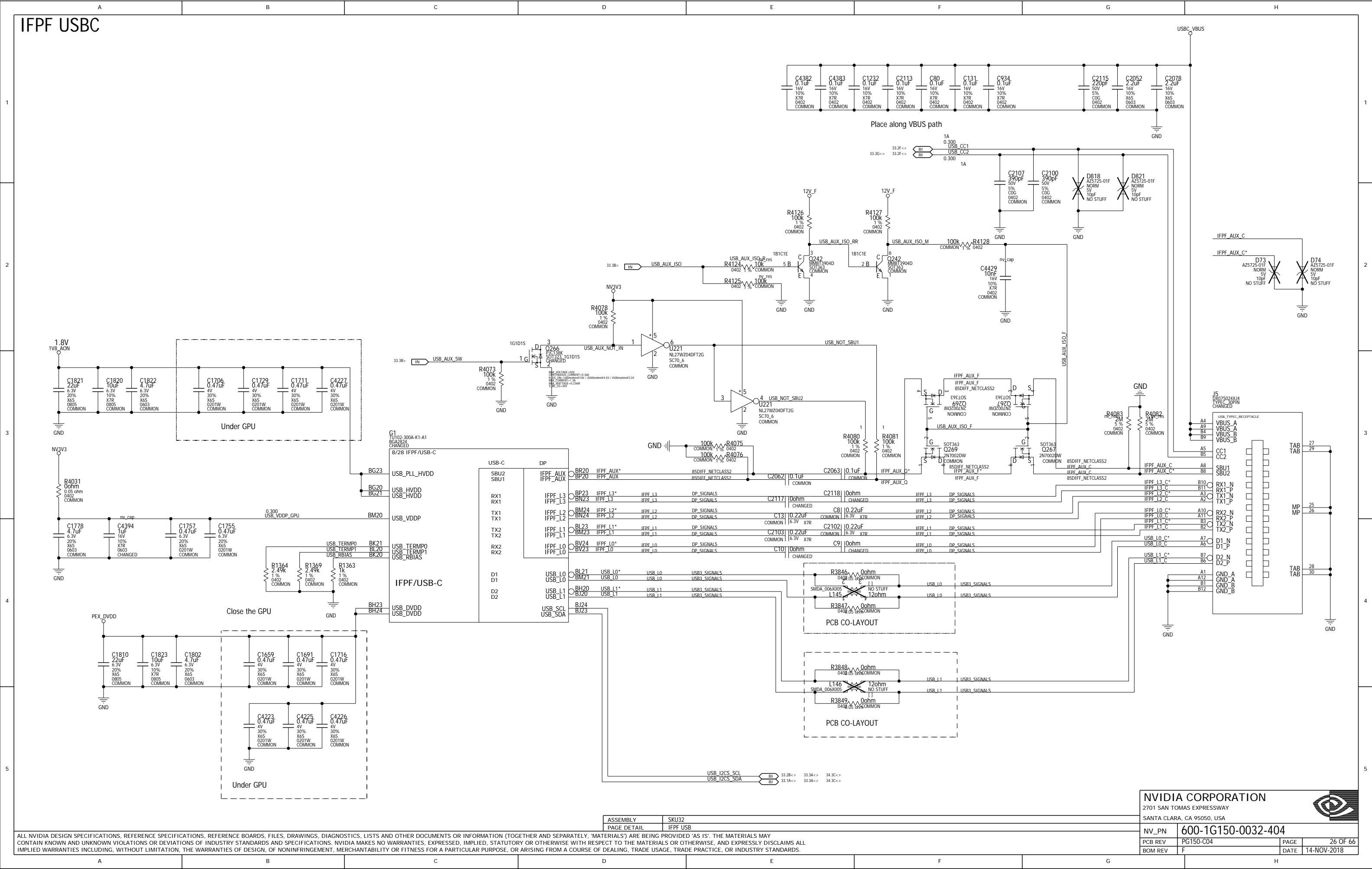
IFPE DP




ASSEMBLY	SKU32
PAGE DETAIL	IFPE DP

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IFPF USBC

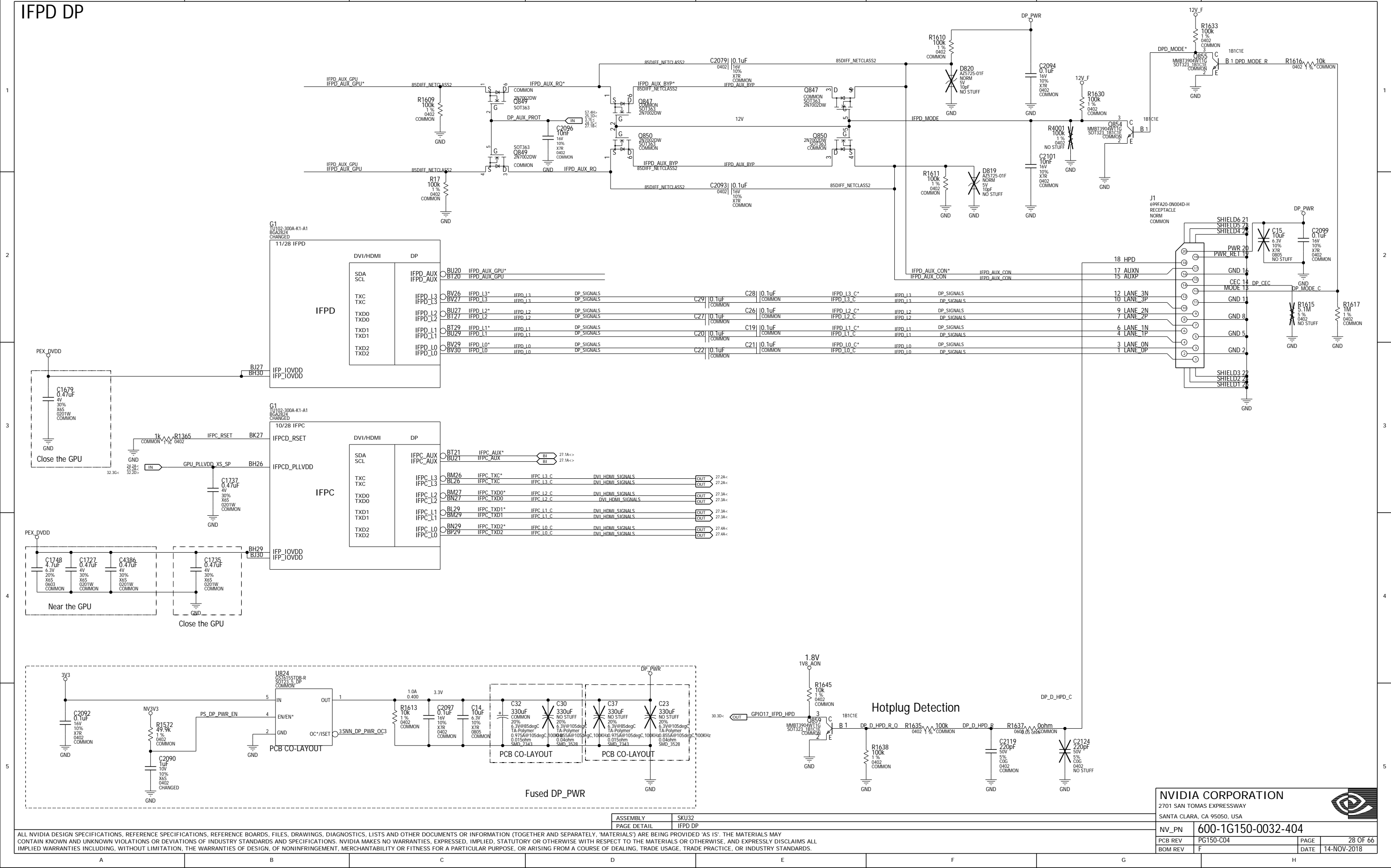


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IFPD DP



NVHS Interface and FRAME LOCK



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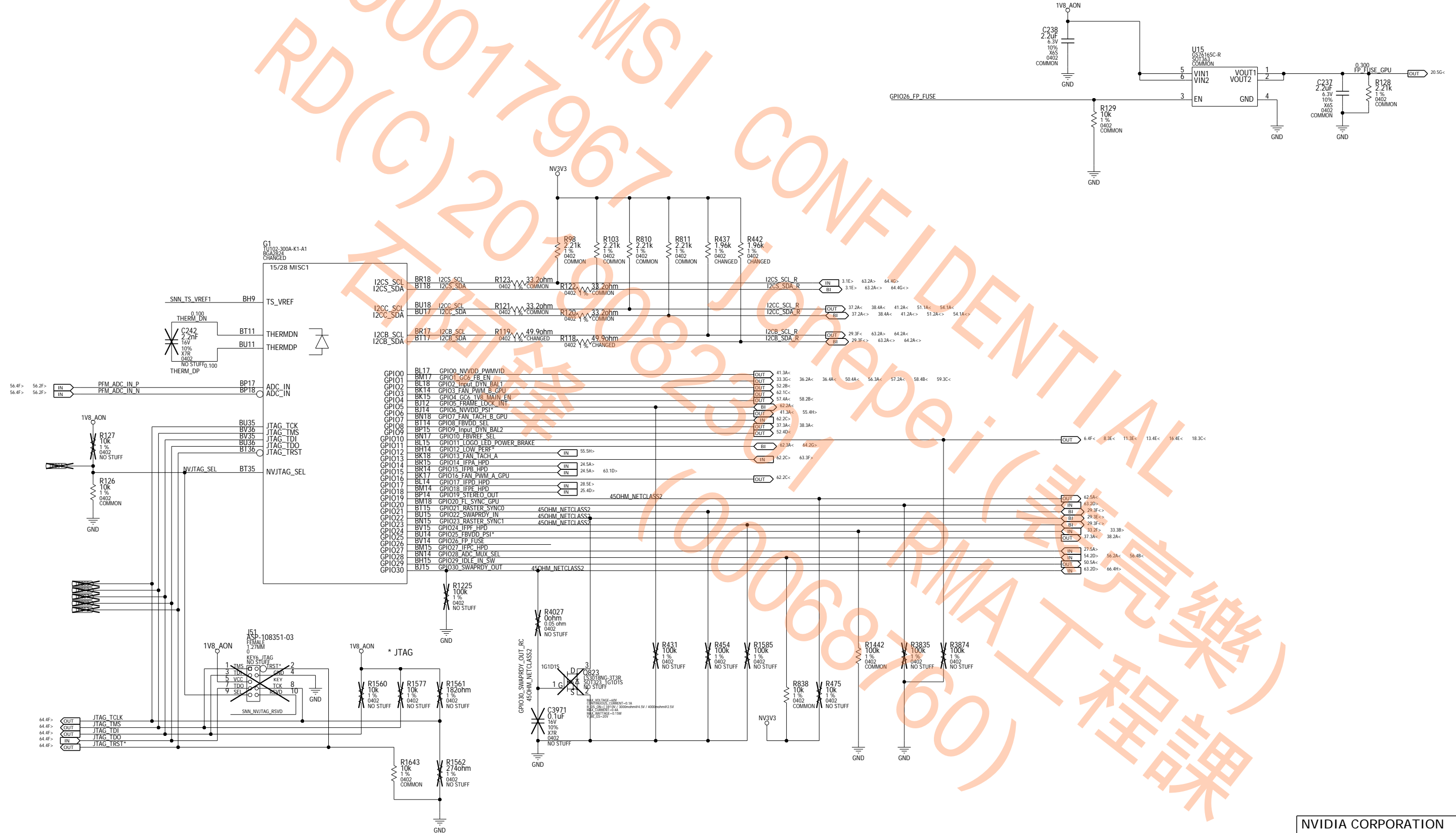


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MISC1: Fan, Thermal, JTAG, GPIO, STEREO



ASSEMBLY	SKU32
PAGE DETAIL	MISC: THERMAL, JTAG, GPIO, STEREO

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MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	K4Z80325BC-HC14
L	L	H	00001	MT61K256M32JE-14:A
L	H	L	00010	H56C8H24MJR-S2C
L	H	H	00011	K4Z80325BC-HC16
H	L	L	00100	K4Z80325BC-HC16
H	L	H	00101	H56C8H24MJR-S4C
H	H	L	00110	K4ZAF325BM-HC14
H	H	H	00111	K4ZAF325BM-HC14
L	L	M	01000	K4Z80325BC-HC14
L	M	L	01001	H56C8H24MJR-S2C

DEFAULT

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	
L	L	L	XXX1	FS_OVERT ENABLE
L	L	H	XXX0	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

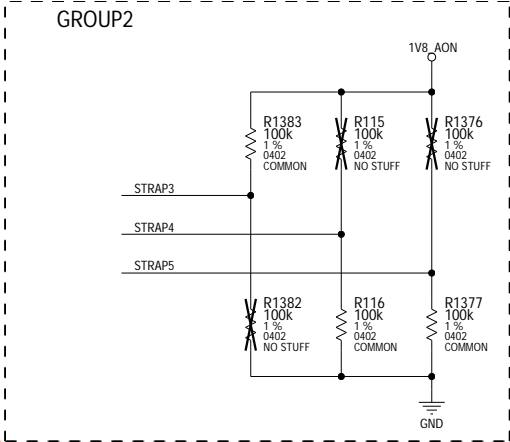
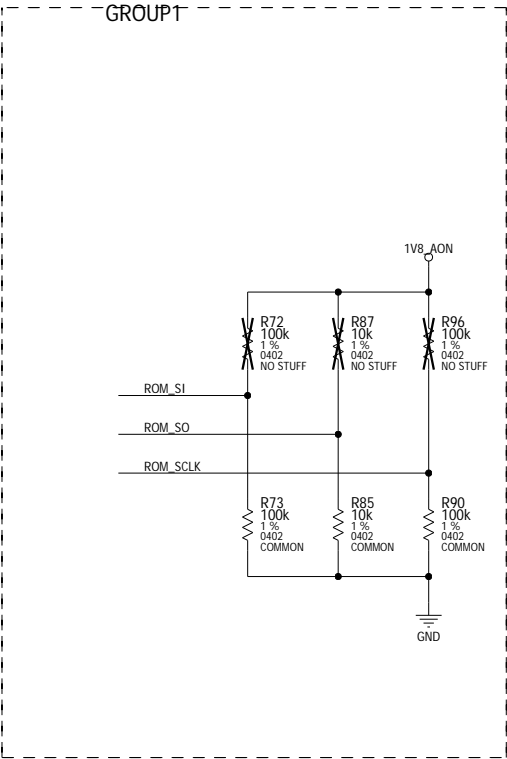
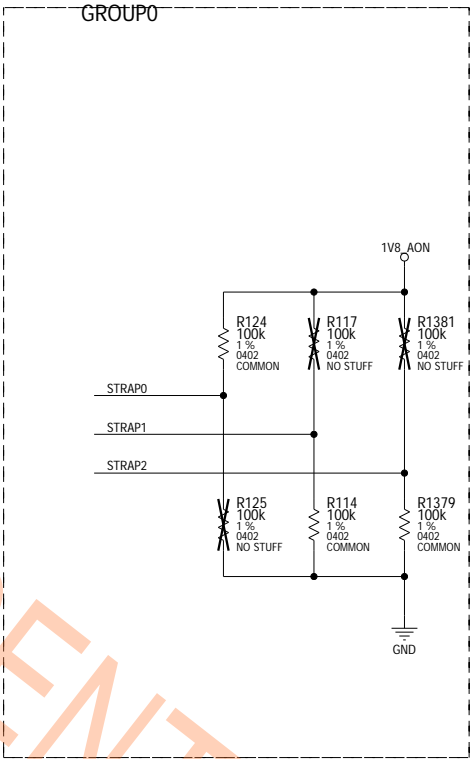
SKU 200

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



G1
TU102-300A-K1-A1
0402 10K
CHANGED

17/28 MISC2

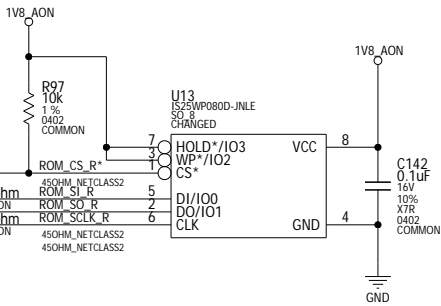
STRAP0	BK11	STRAP0
STRAP1	BL11	STRAP1
STRAP2	BM11	STRAP2
STRAP3	BM12	STRAP3
STRAP4	BK12	STRAP4
STRAP5	BL12	STRAP5

ROM_CS
ROM_SI
ROM_SO
ROM_SCLK

BR12 ROM_CS* 450HM_NETCLASS2
BP11 ROM_SI 450HM_NETCLASS2
BP12 ROM_SO 450HM_NETCLASS2
R99 33.2ohm 450HM_NETCLASS2
R81 0ohm 450HM_NETCLASS2
R82 33.2ohm 450HM_NETCLASS2
R86 33.2ohm 450HM_NETCLASS2

OVERT
BUFRST

BN11 THERM OVERT*
BN12 SNN_GPU_BUFRST*



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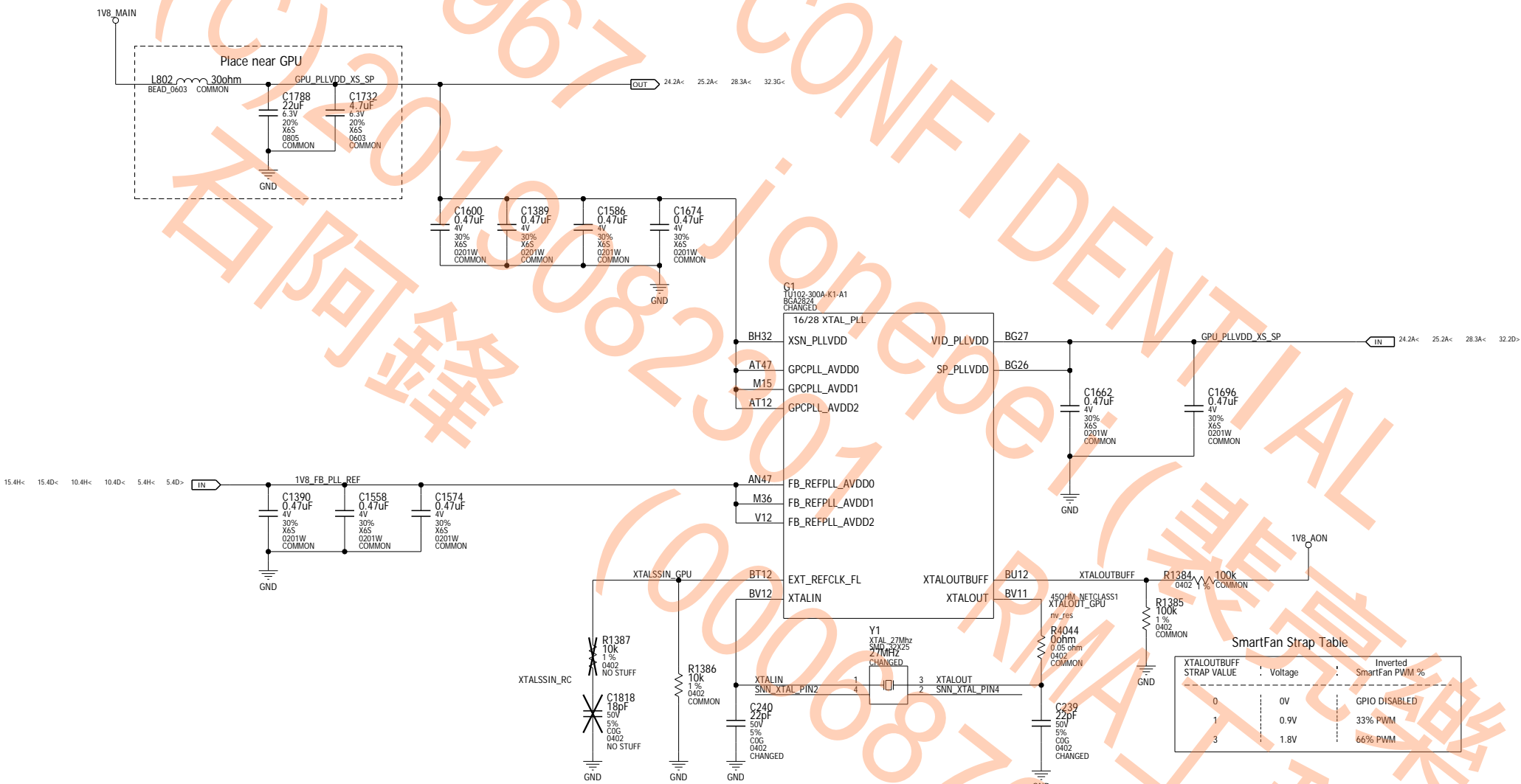
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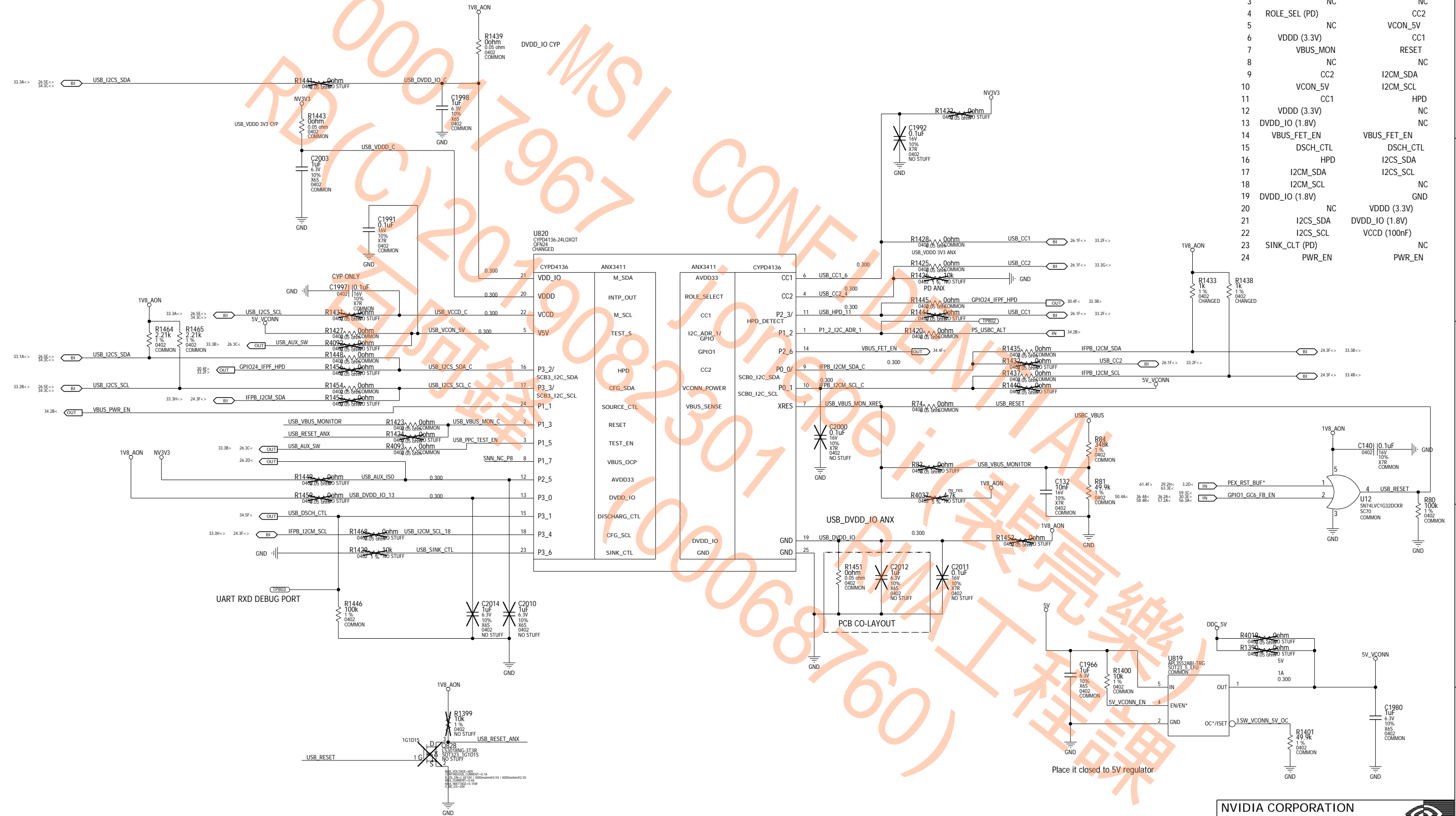
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MISC2: XTAL. PLL



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MISC: USB PPC



PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN

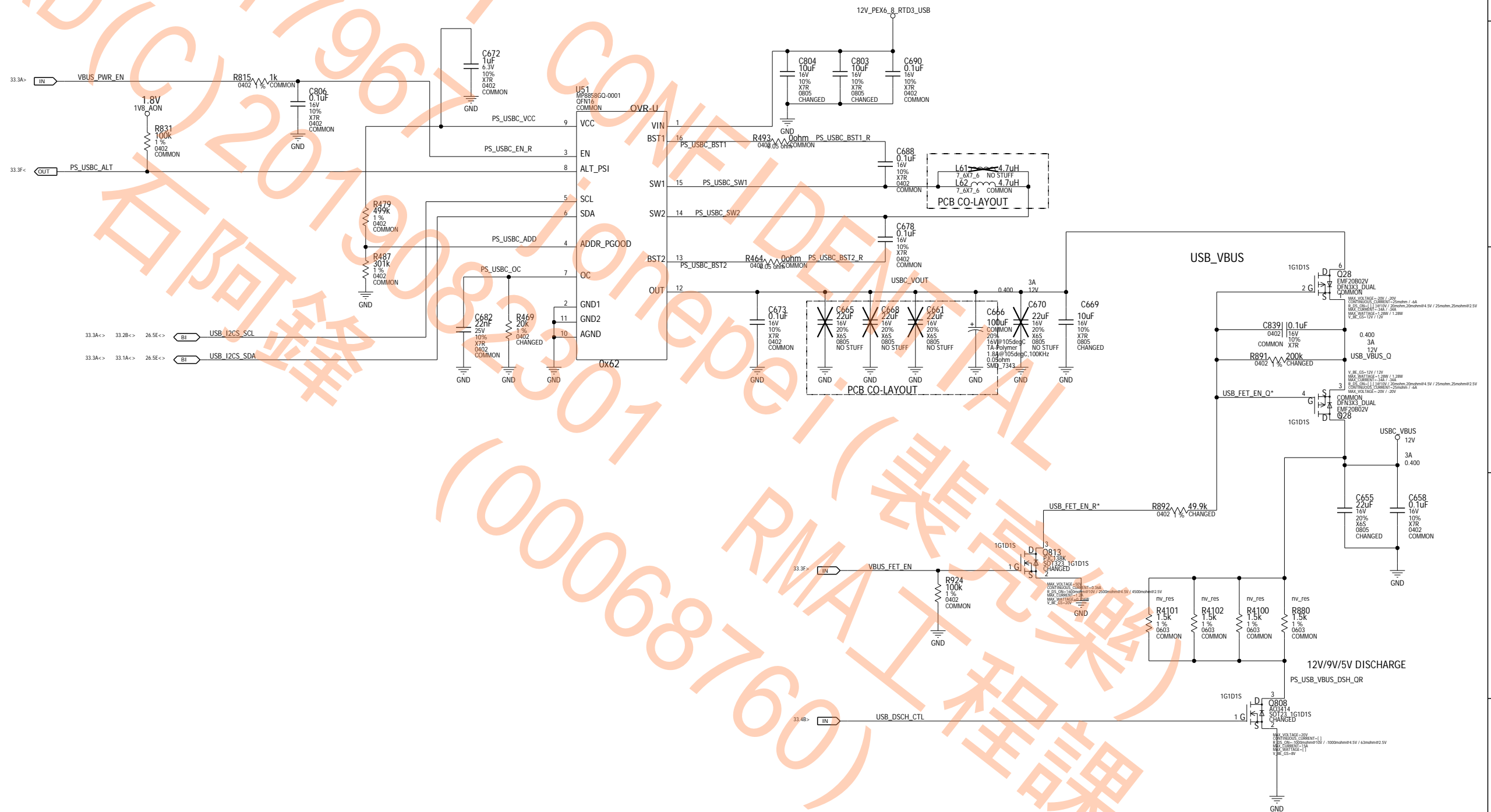
ASSEMBLY	SKU32
PAGE DETAIL	MISC: USB PPC

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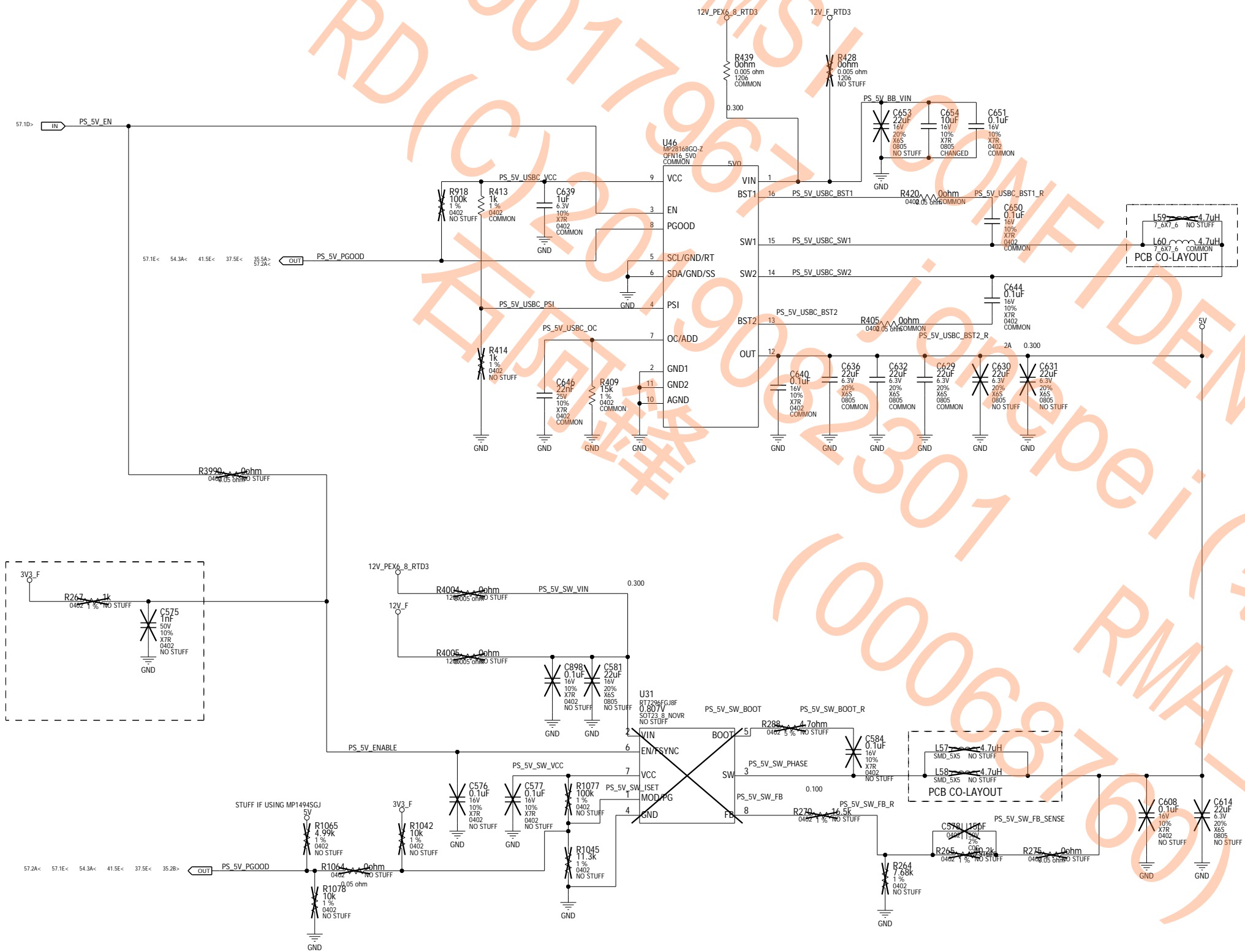
PS: USB VR



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PS: 5V, 5V_BACKUP



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ASSEMBLY	SKU32
PAGE DETAIL	PS: 5V

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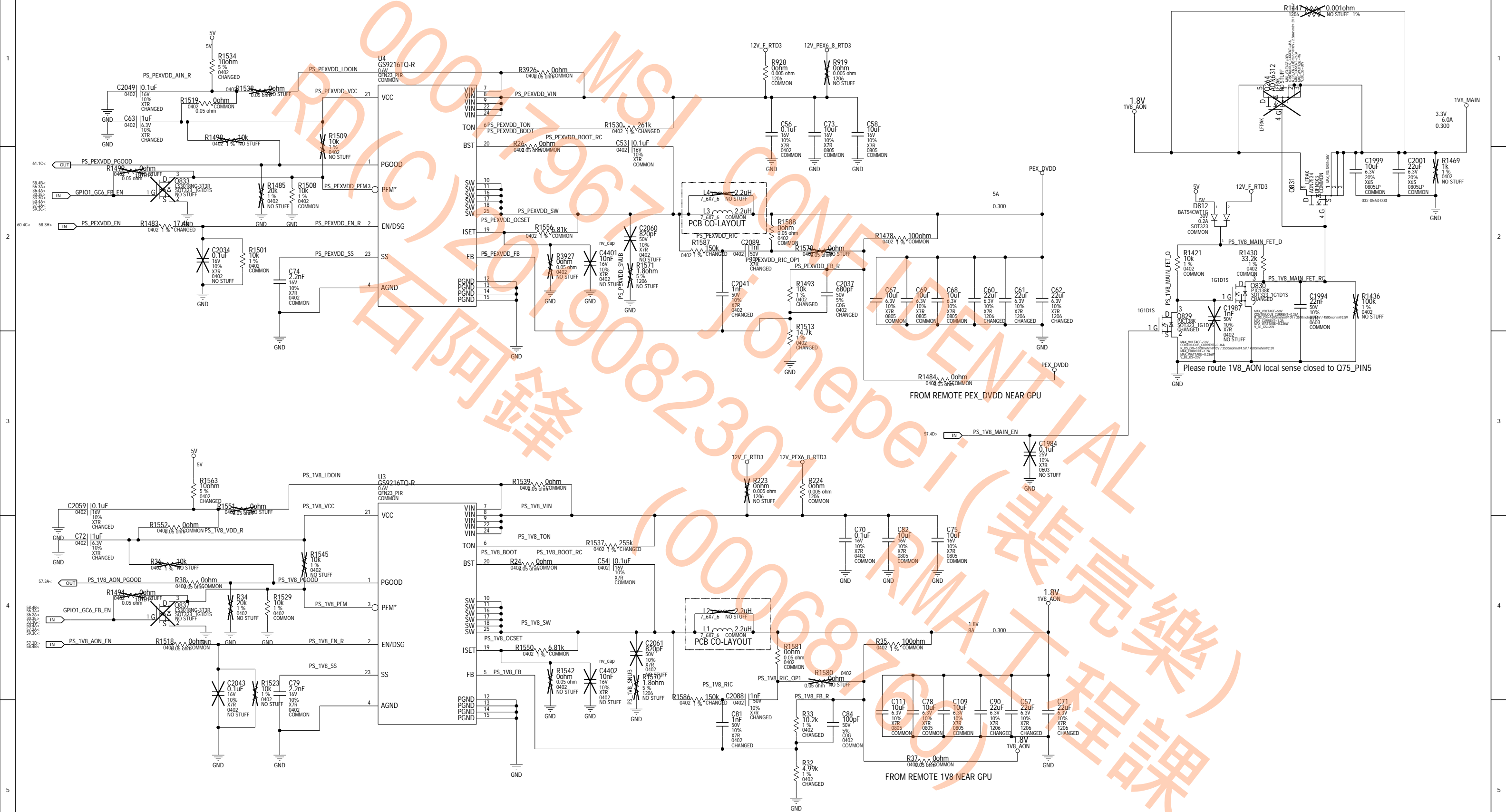
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PS: PEXVDD 1V8 Rail



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ASSEMBLY	SKU32
PAGE DETAIL	PS: PEXVDD 1V8 Ra

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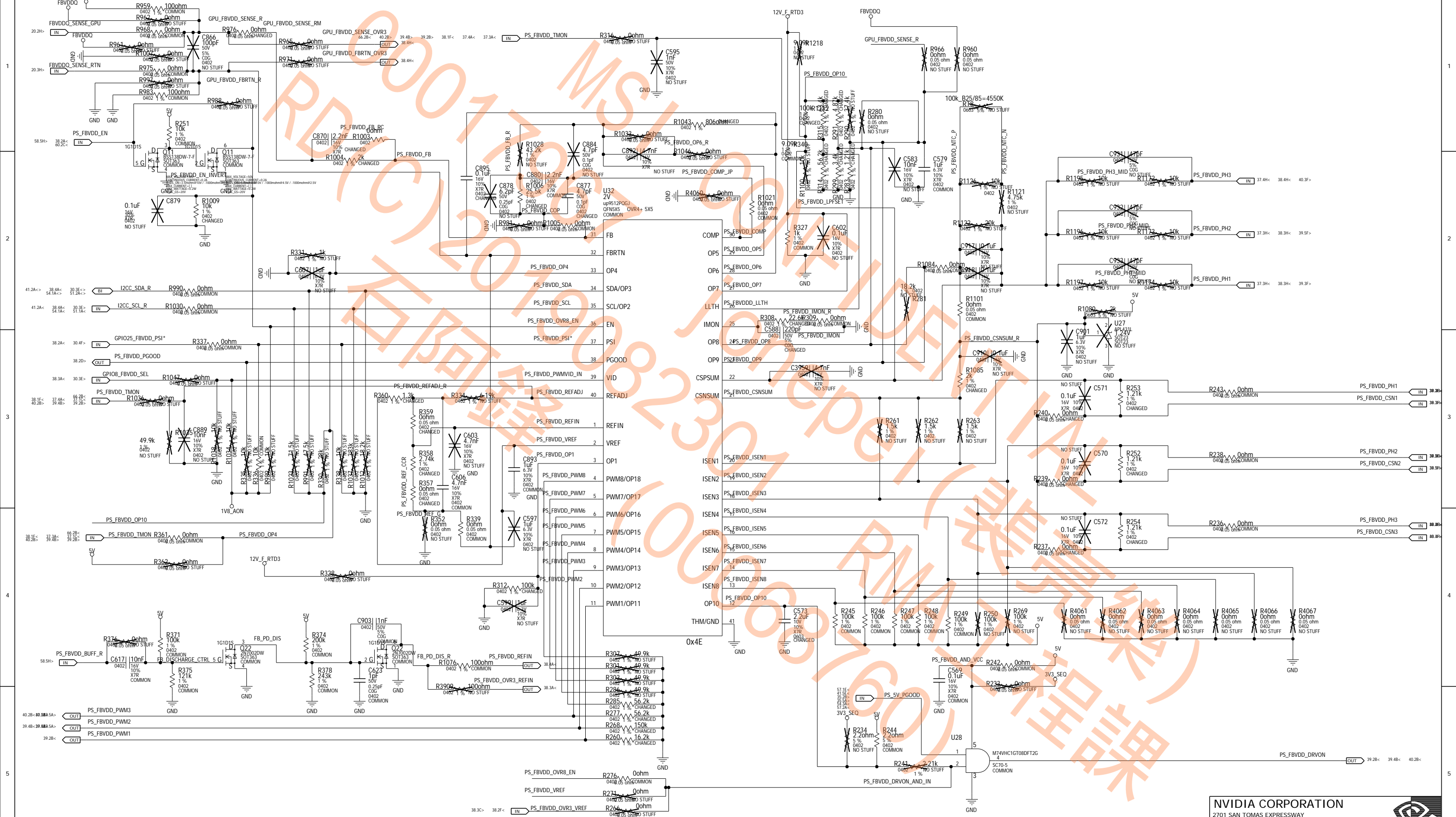
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PS: FBVDD Controller



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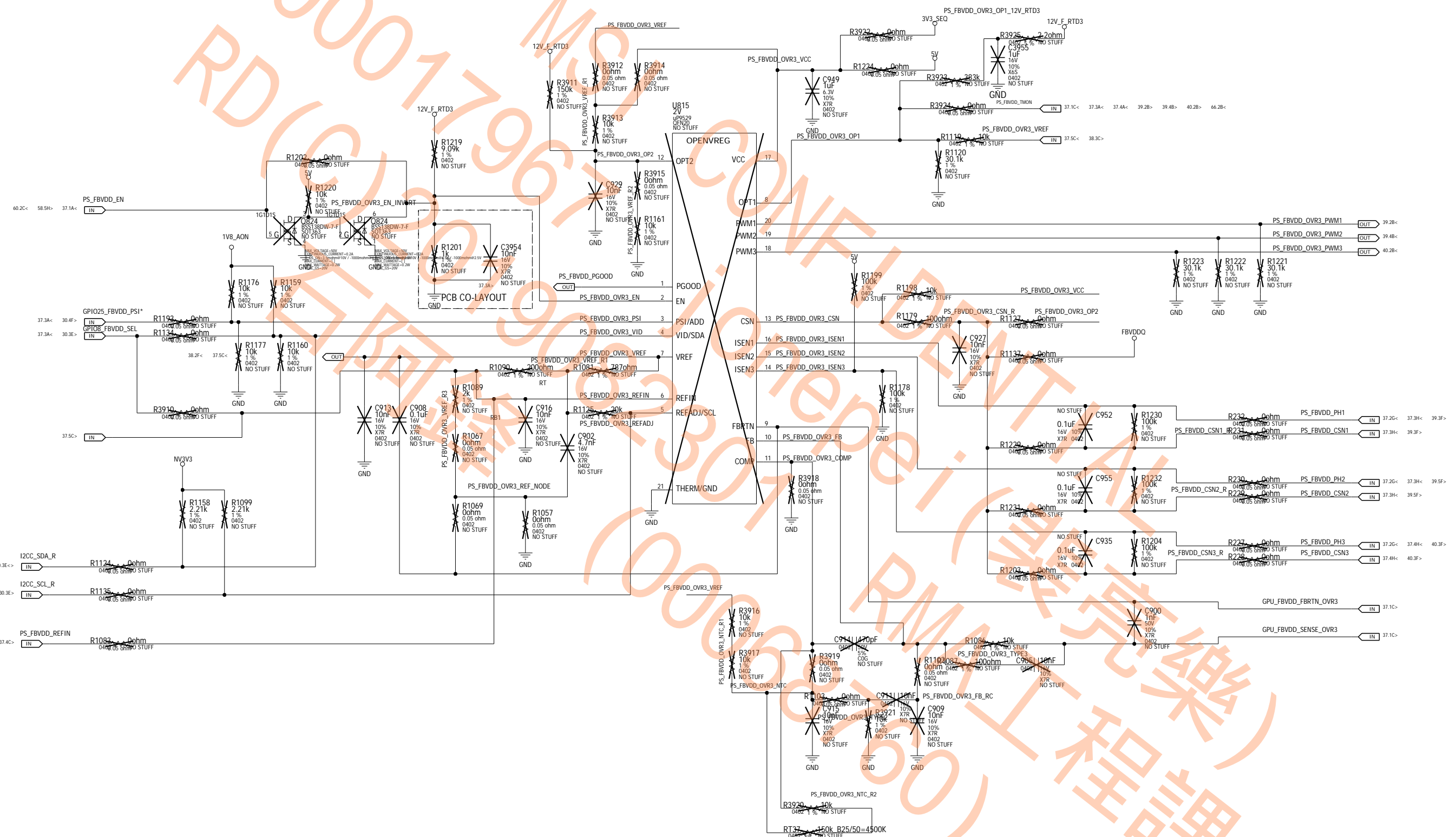
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ASSEMBLY	SKU32
PAGE DETAIL	PS: FBVDD Controller

PS: FBVDD Controller OVR3



ASSEMBLY	SKU32
PAGE DETAIL	PS: FBVDD Controller OVR3

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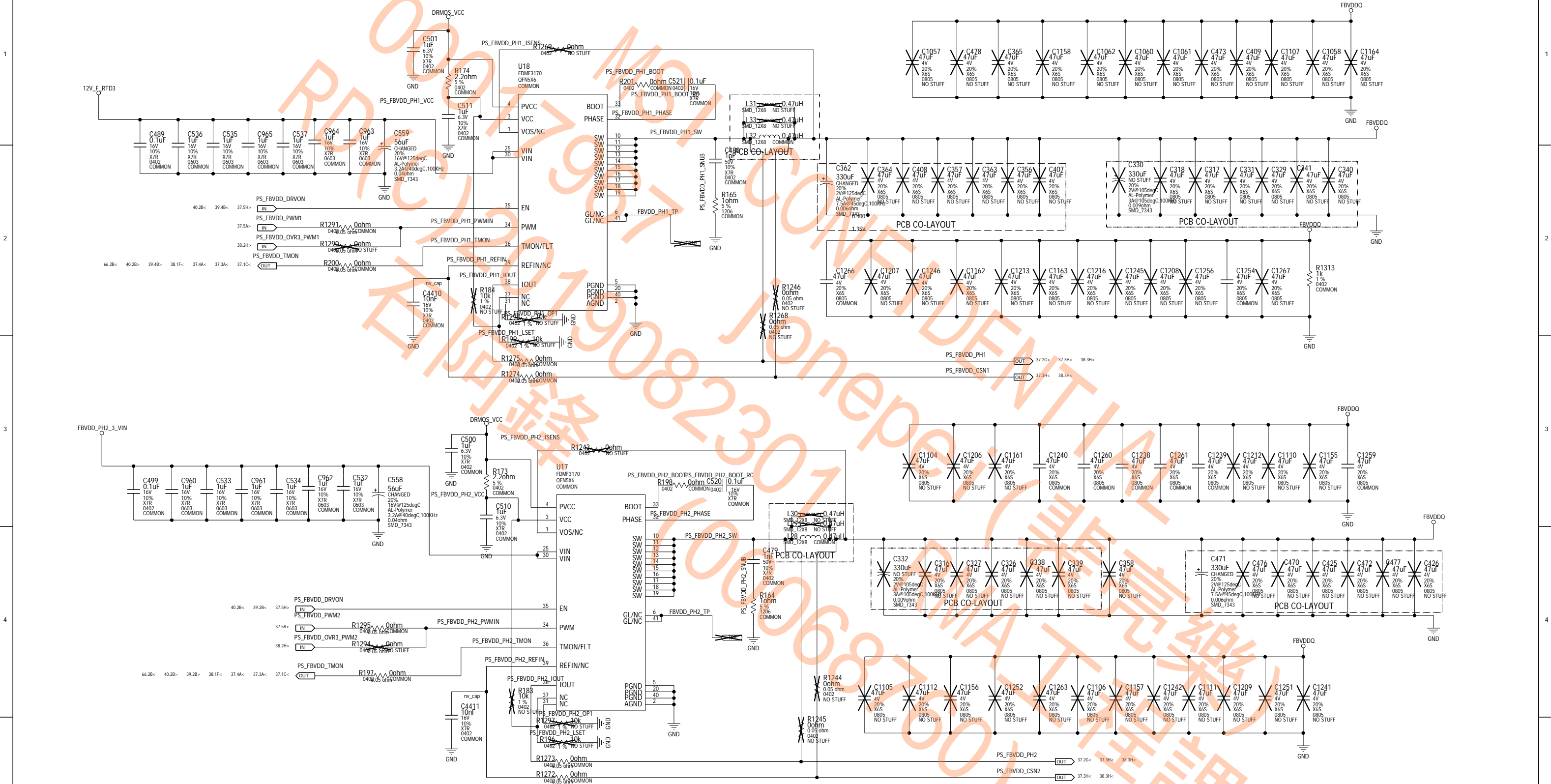
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PS: FBVDD PH1, 2



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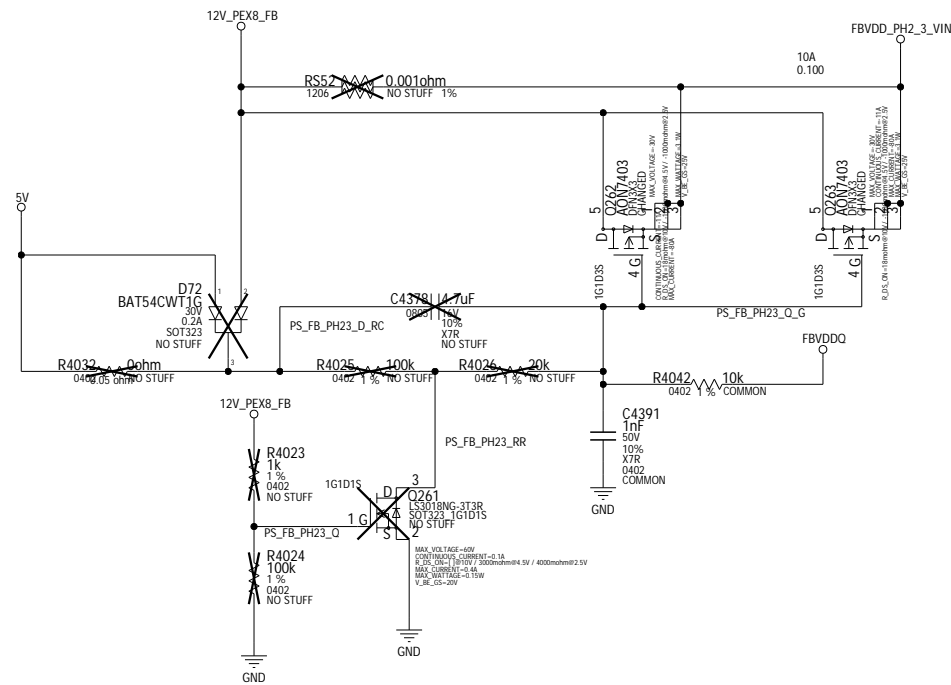
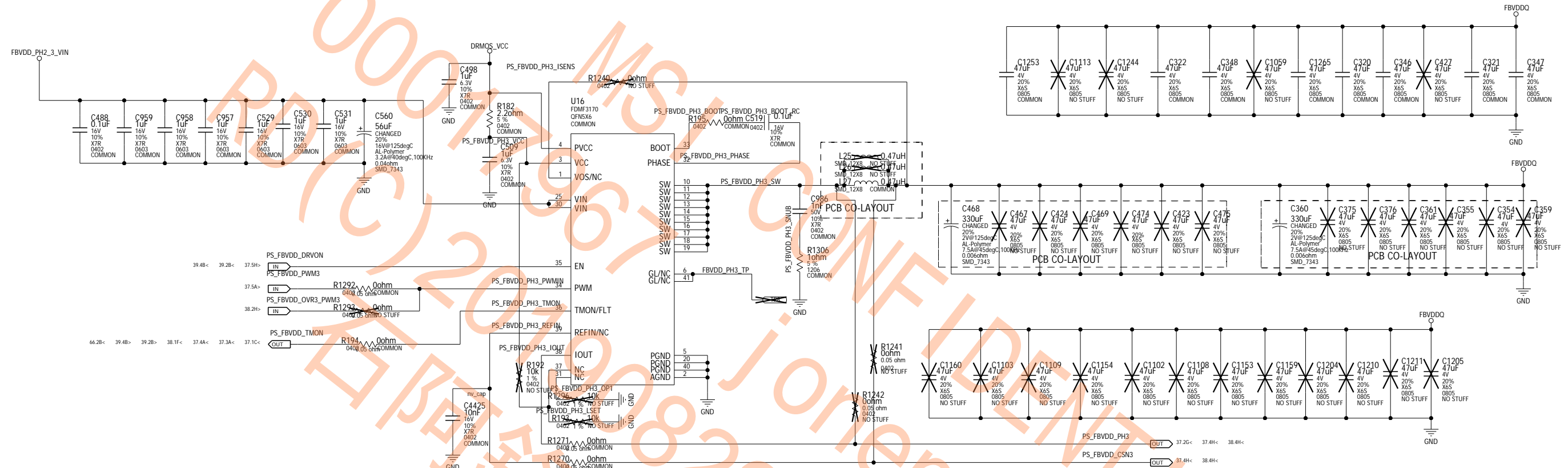
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ASSEMBLY	SKU32
PAGE DETAIL	PS: FBVDD Phase 1, 2

PS: FBVDD PH3



ASSEMBLY	SKU32
PAGE DETAIL	PS: FBVDD Phase 3

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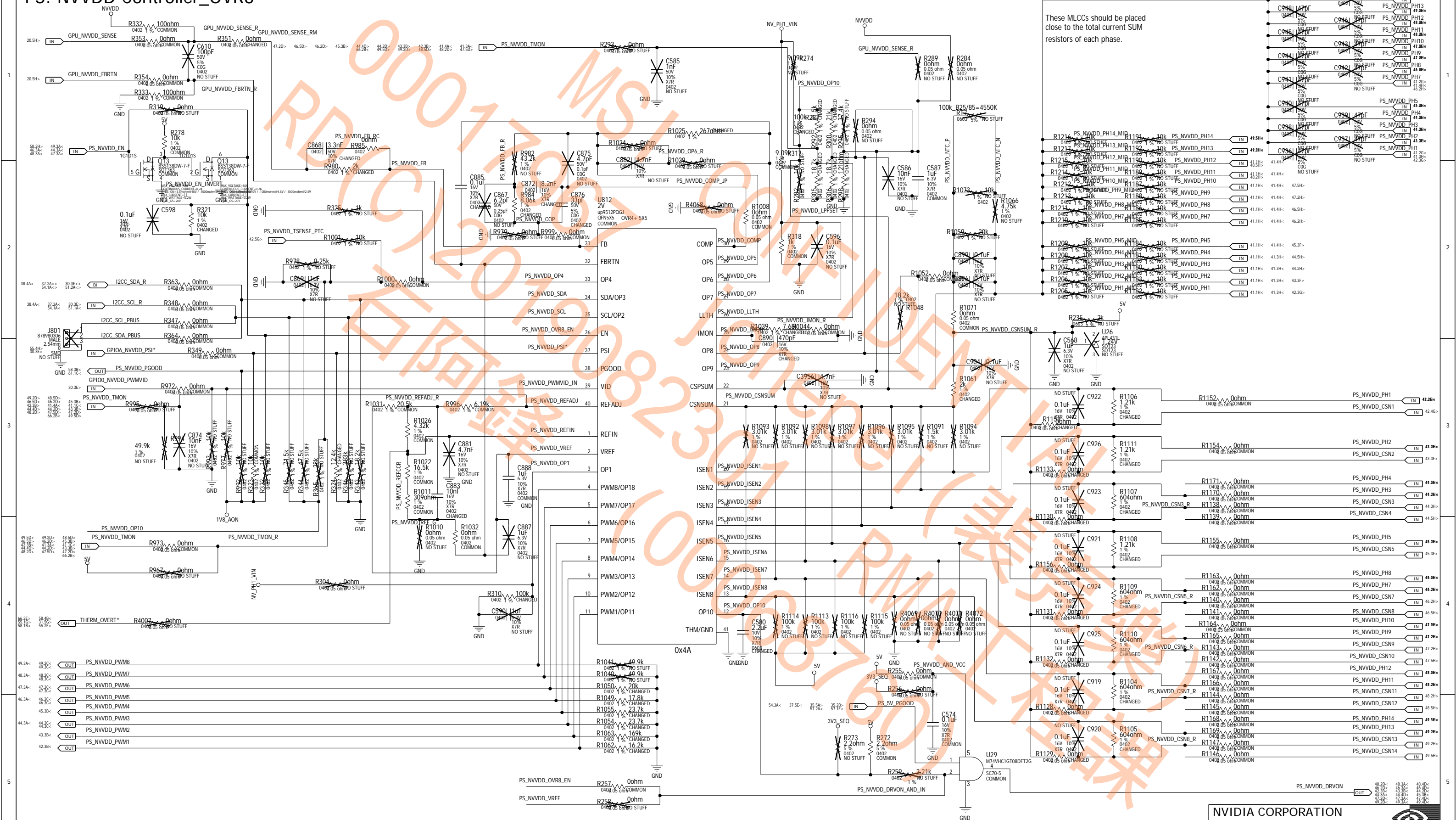
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PS: NVVDD Controller_OVR8



These MLCCs should be placed close to the total current SUM resistors of each phase.

ASSEMBLY	SKU32
PAGE DETAIL	PS: NVVDD Controller_OVR8

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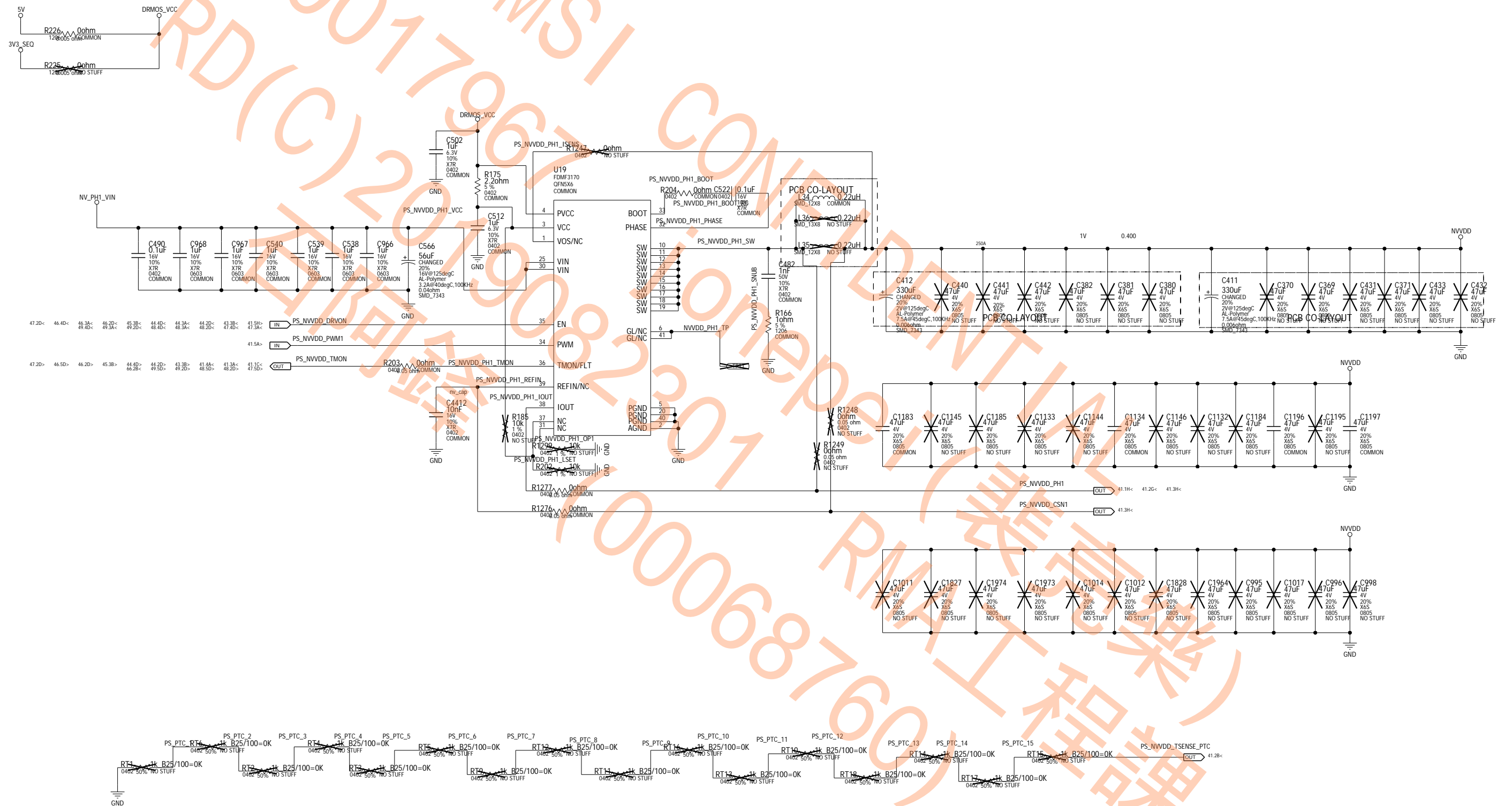
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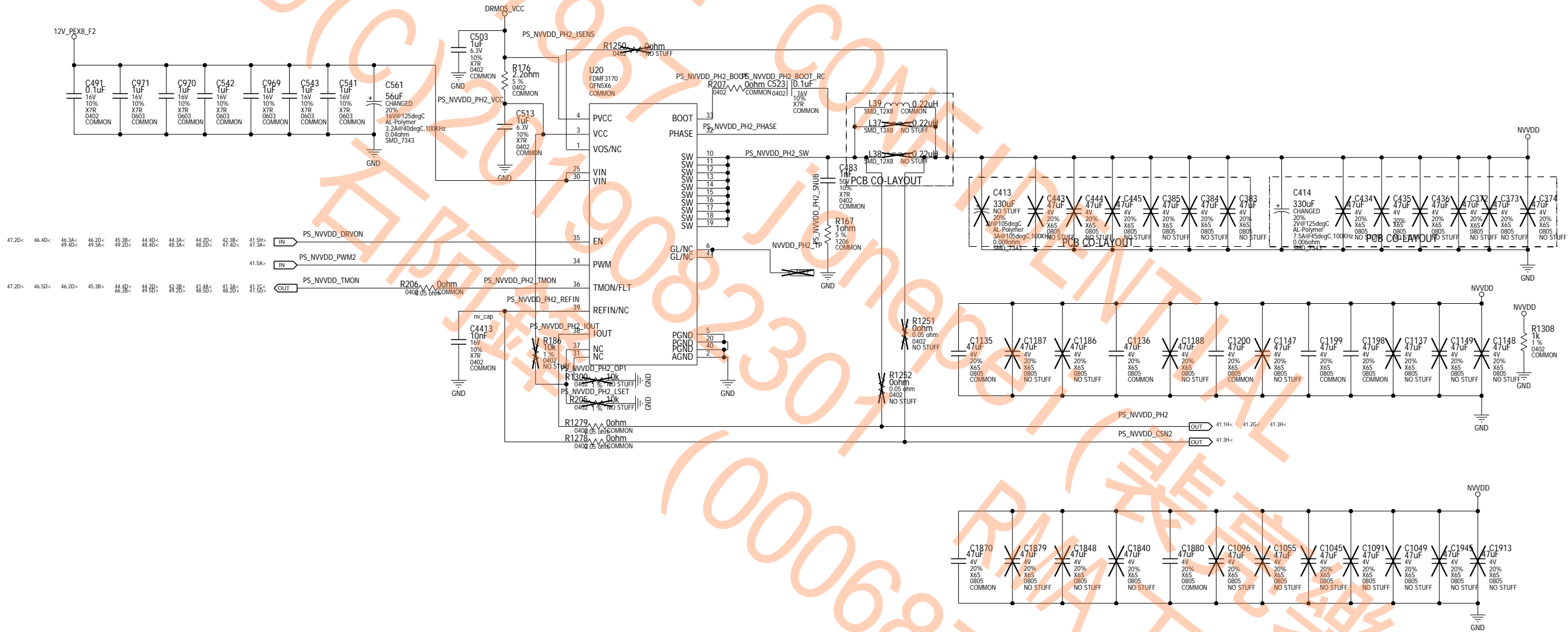
PS: NVVDD Phase 1



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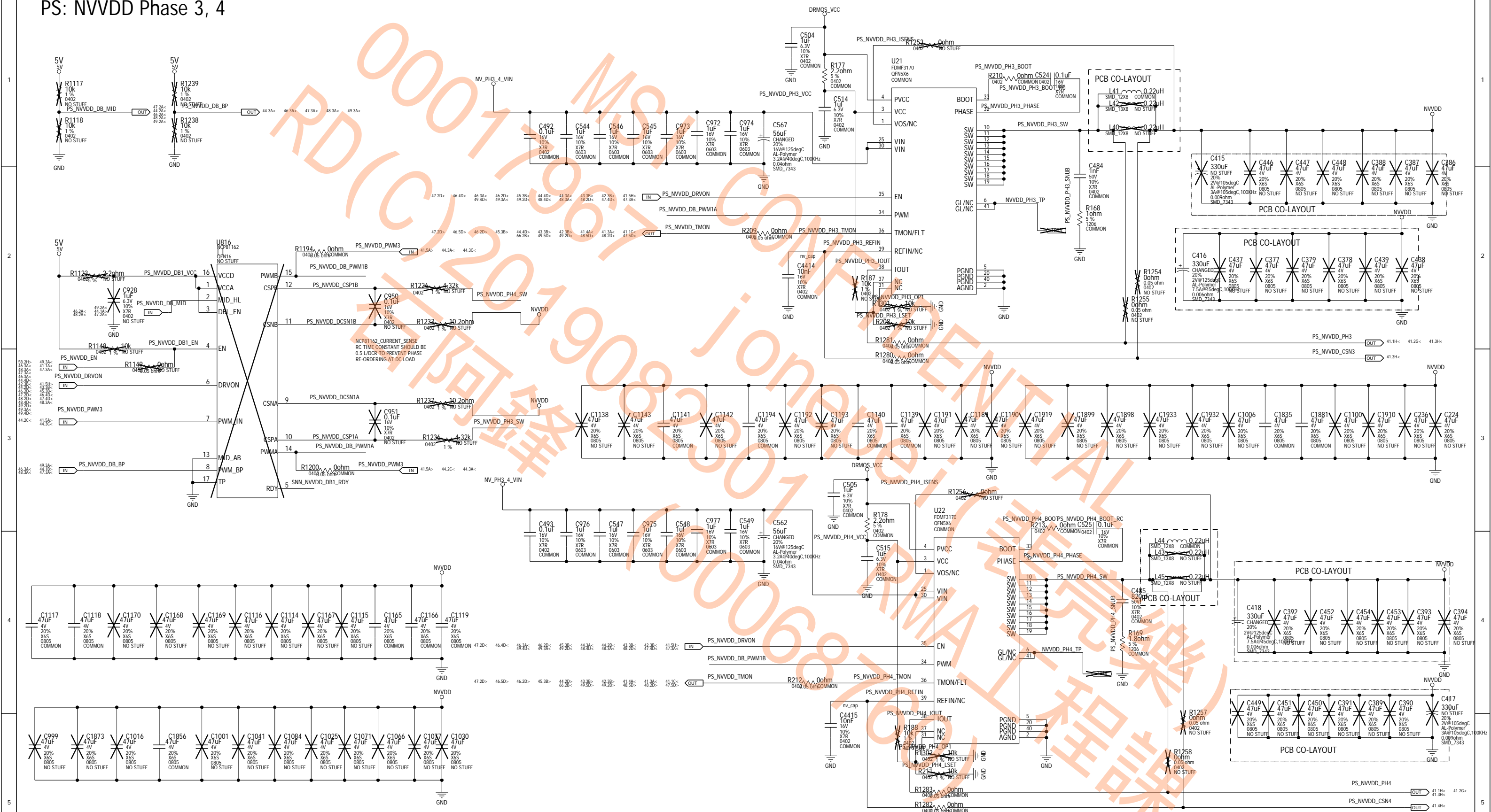
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PS: NVVDD Phase 2



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PS: NVVDD Phase 3, 4



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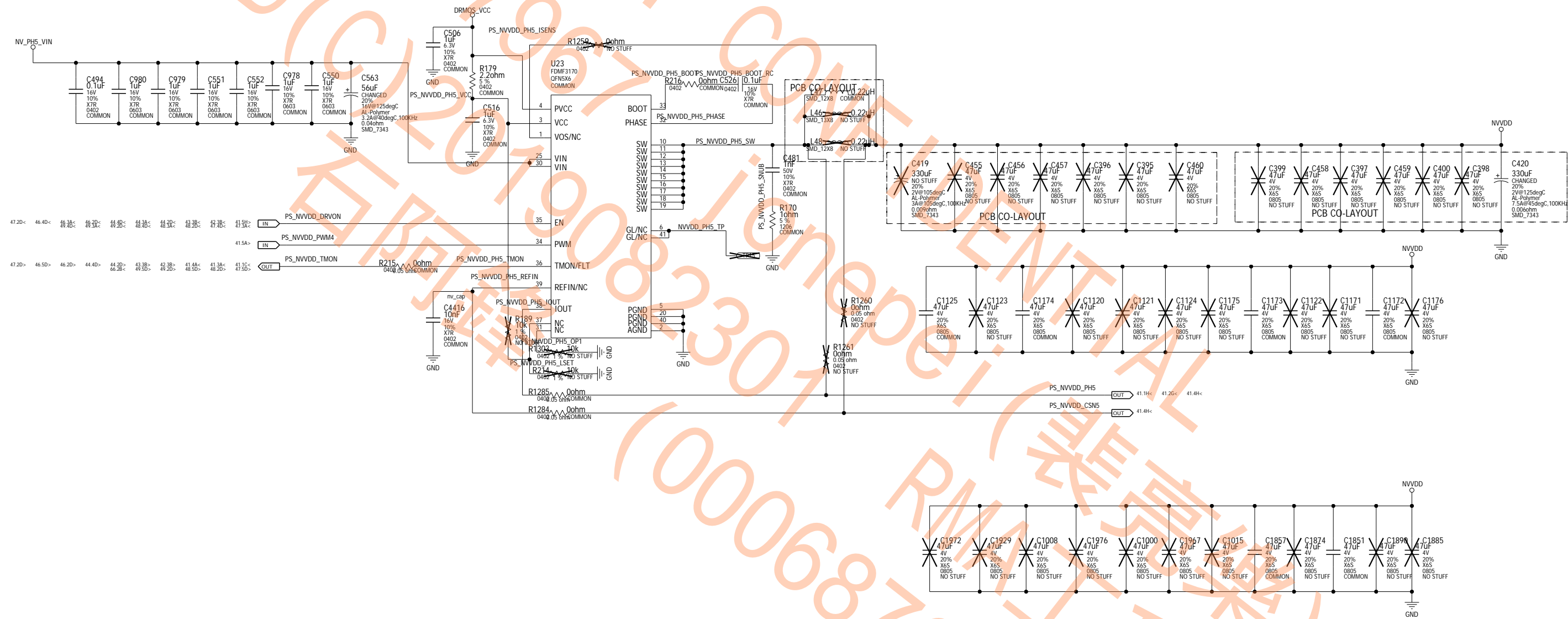


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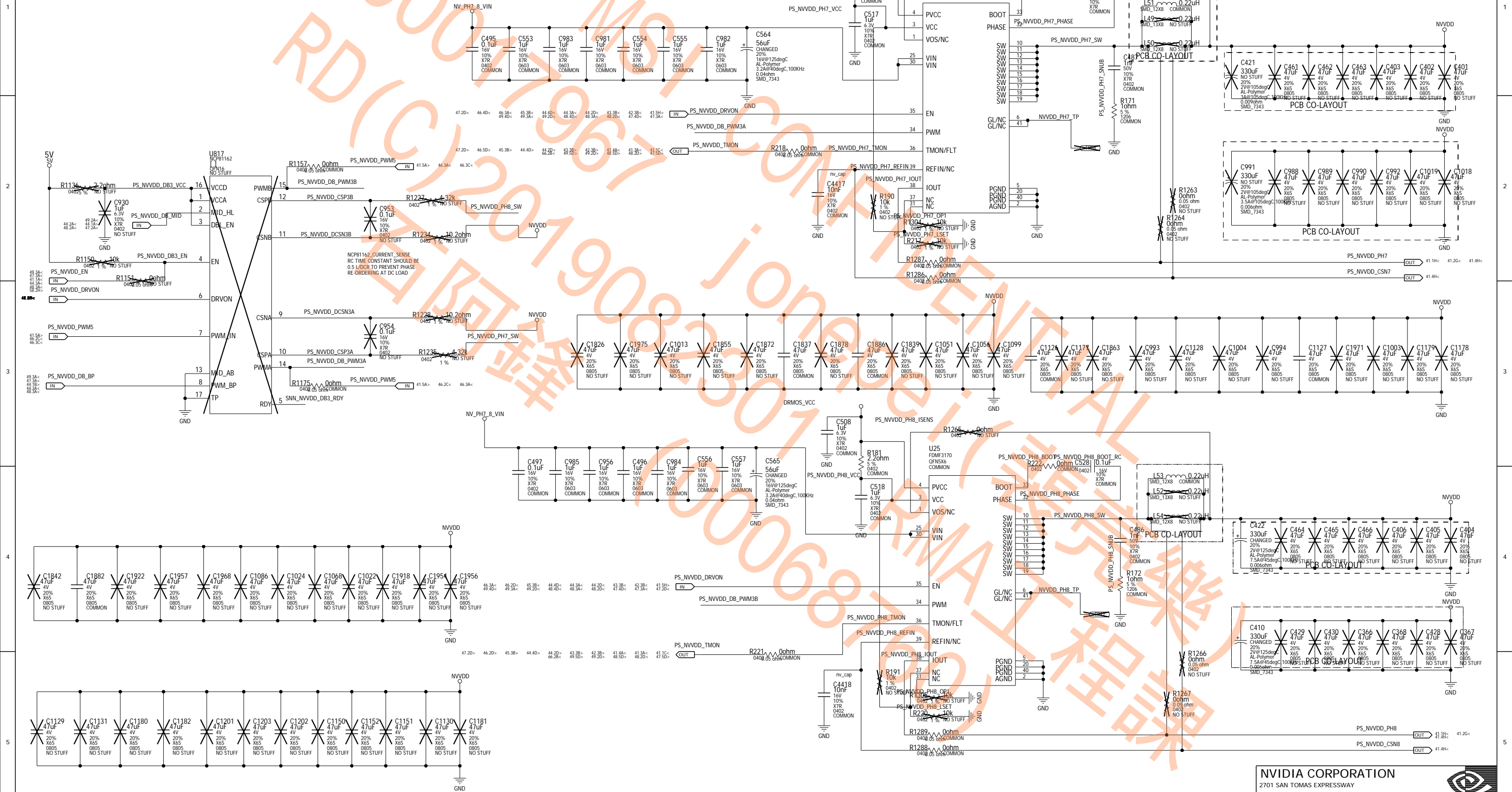
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PS: NVVDD Phase 5



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PS:NVVDD Phase 7, 8



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PS: NVVDD PH 9,10

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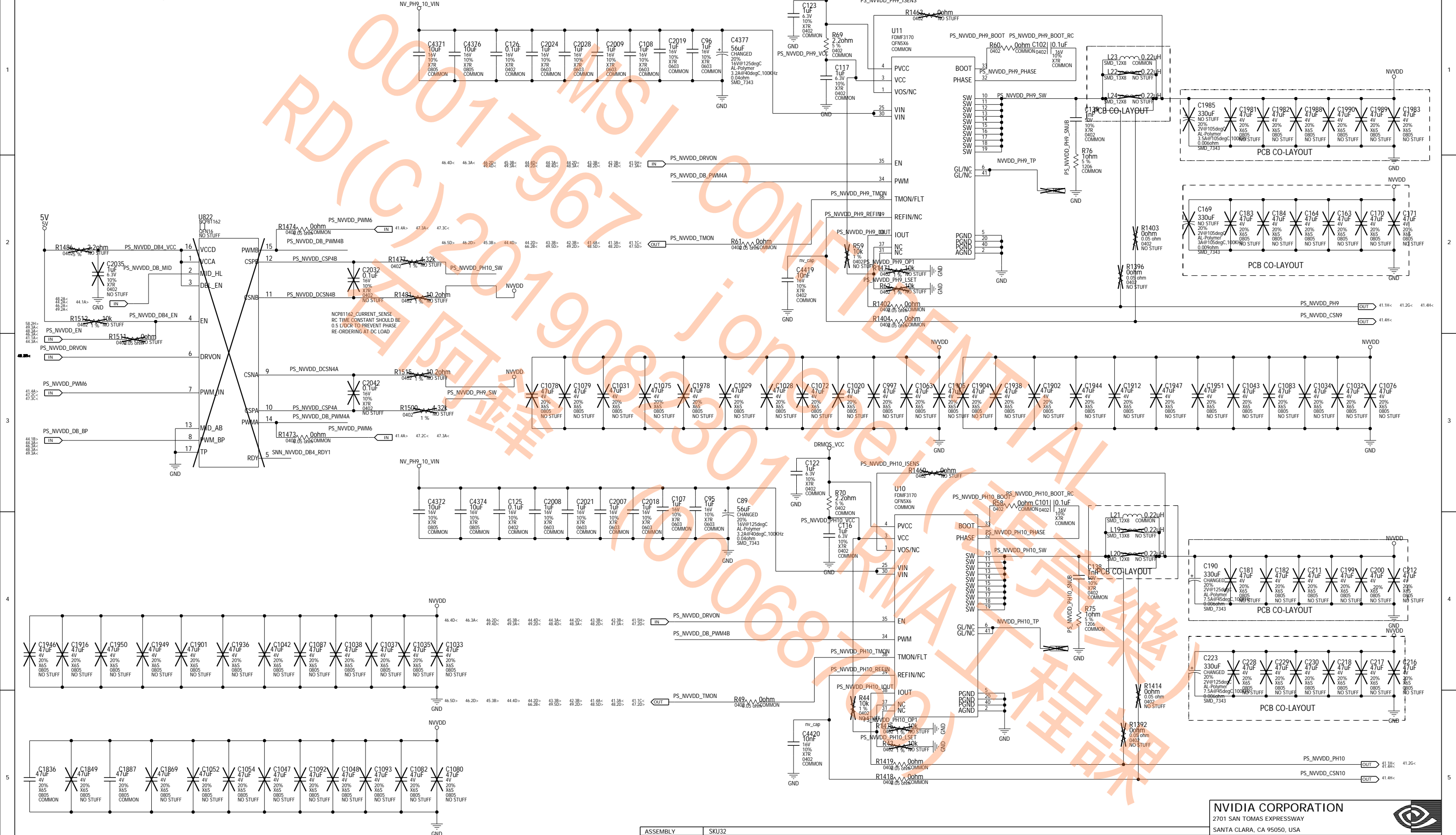
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PS: NVVDD PH 11,12

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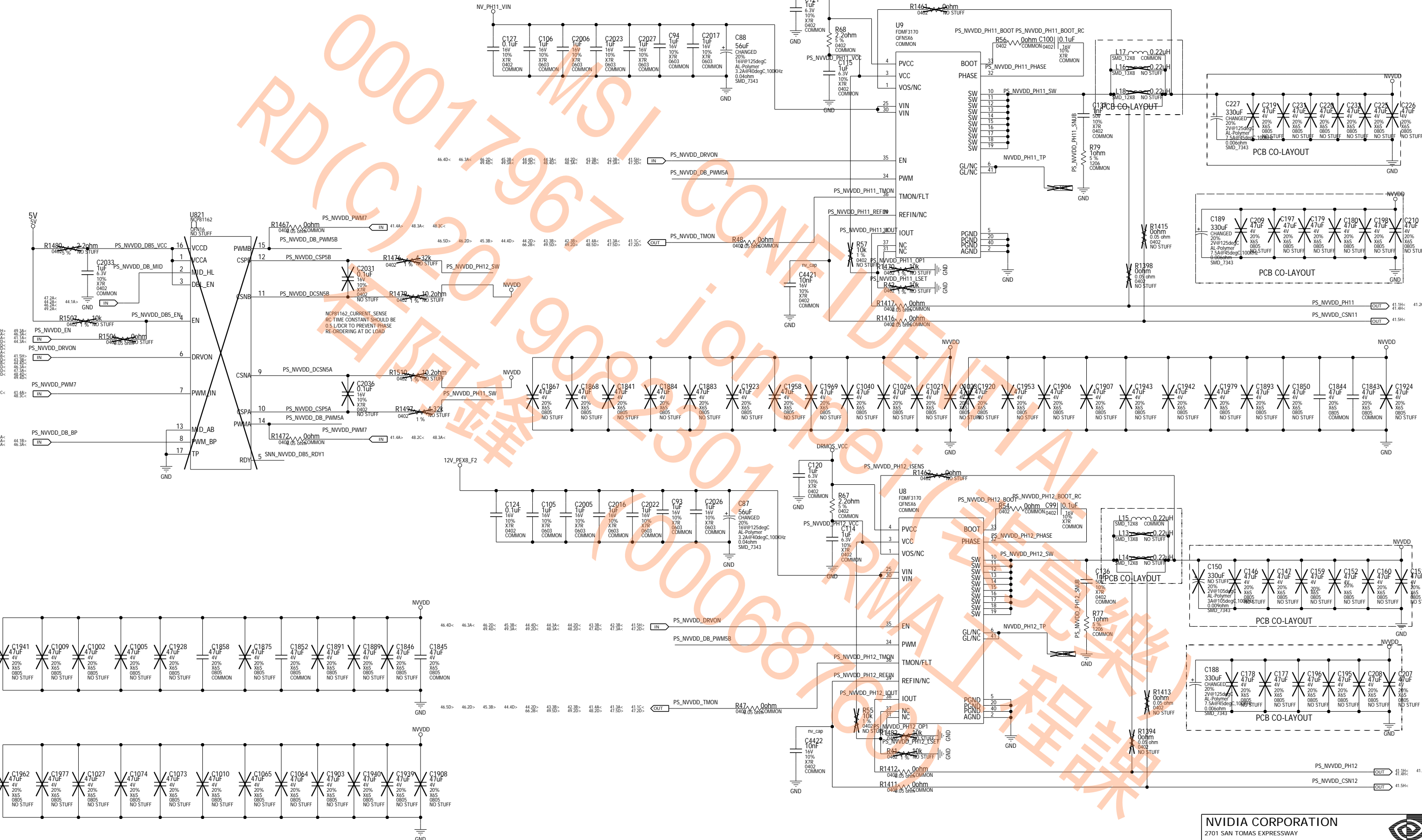
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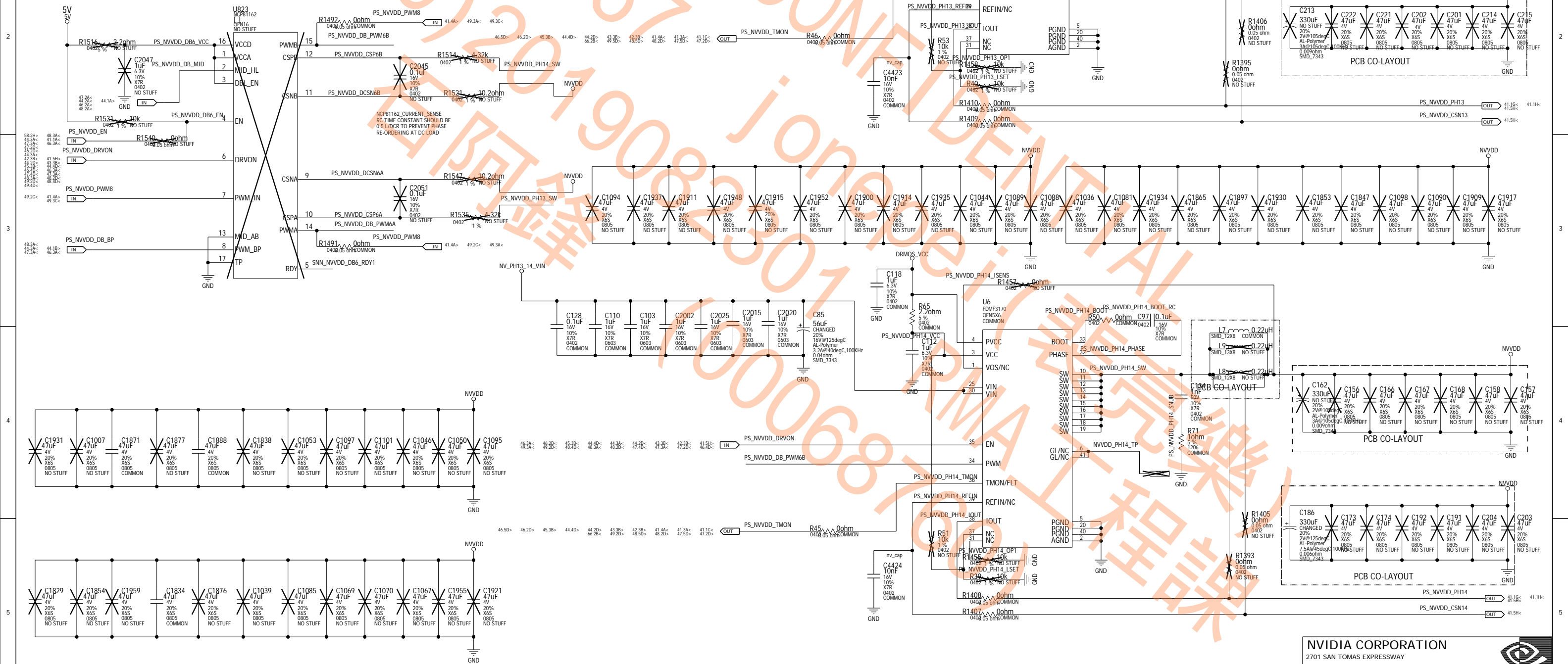


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ASSEMBLY	SKU32
PAGE DETAIL	PS: NVVDD Phase 11, 12

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PS: NVVDD PH 13,14



ASSEMBLY	SKU32
PAGE DETAIL	PS: NVVDD Phase 13, 14

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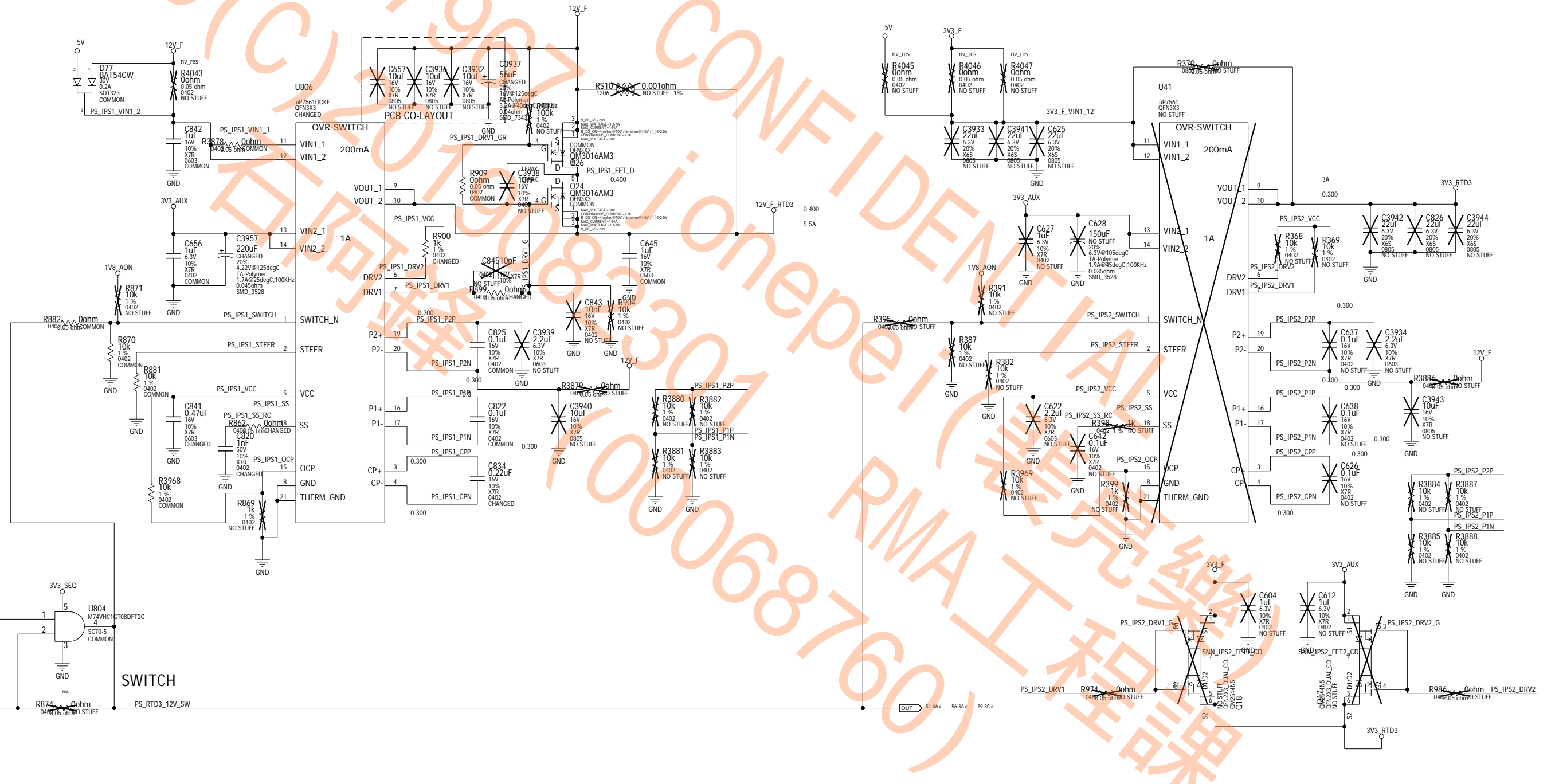
PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPI01	GPI029	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



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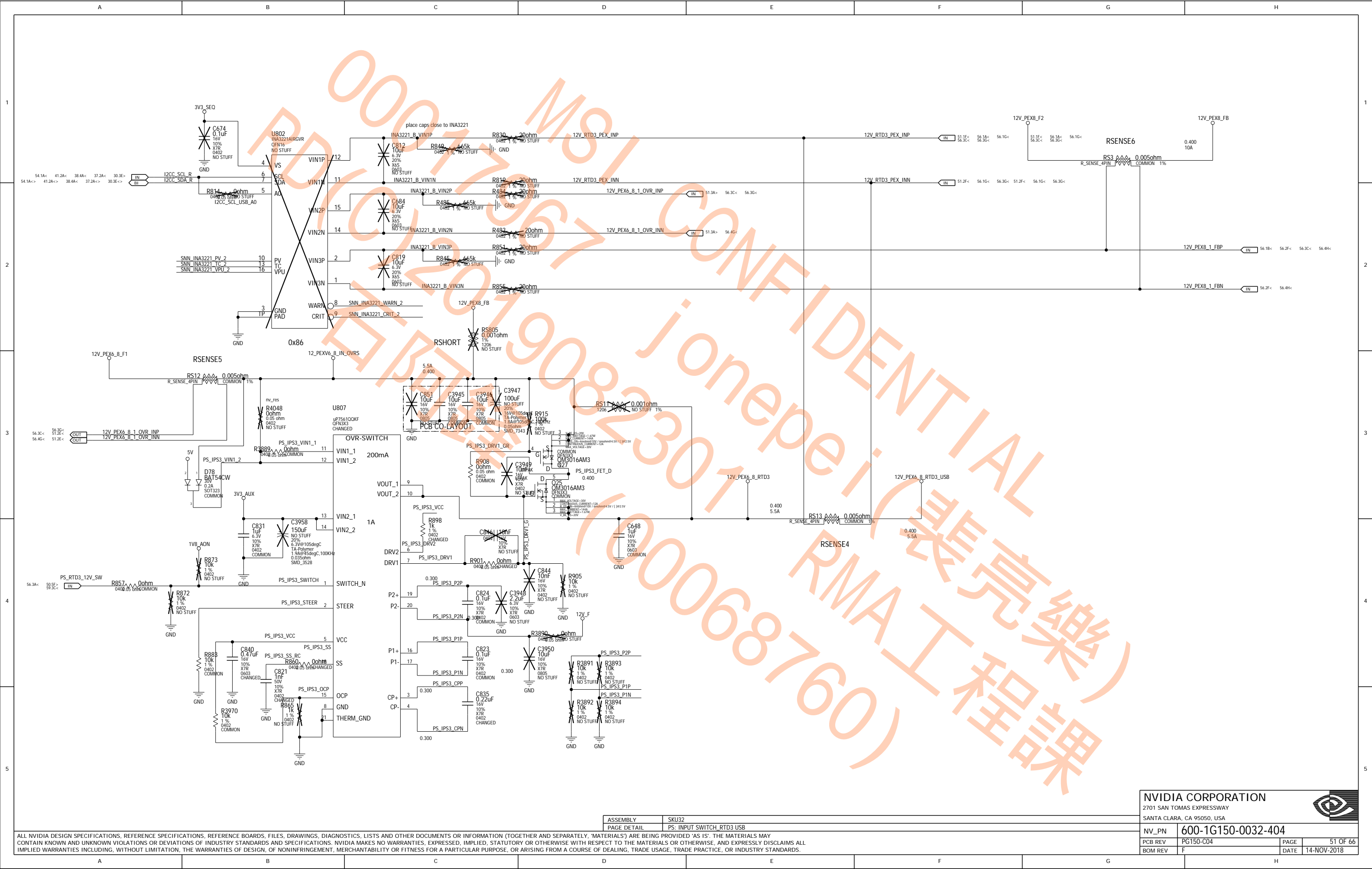
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PCB REV	PG150-C04
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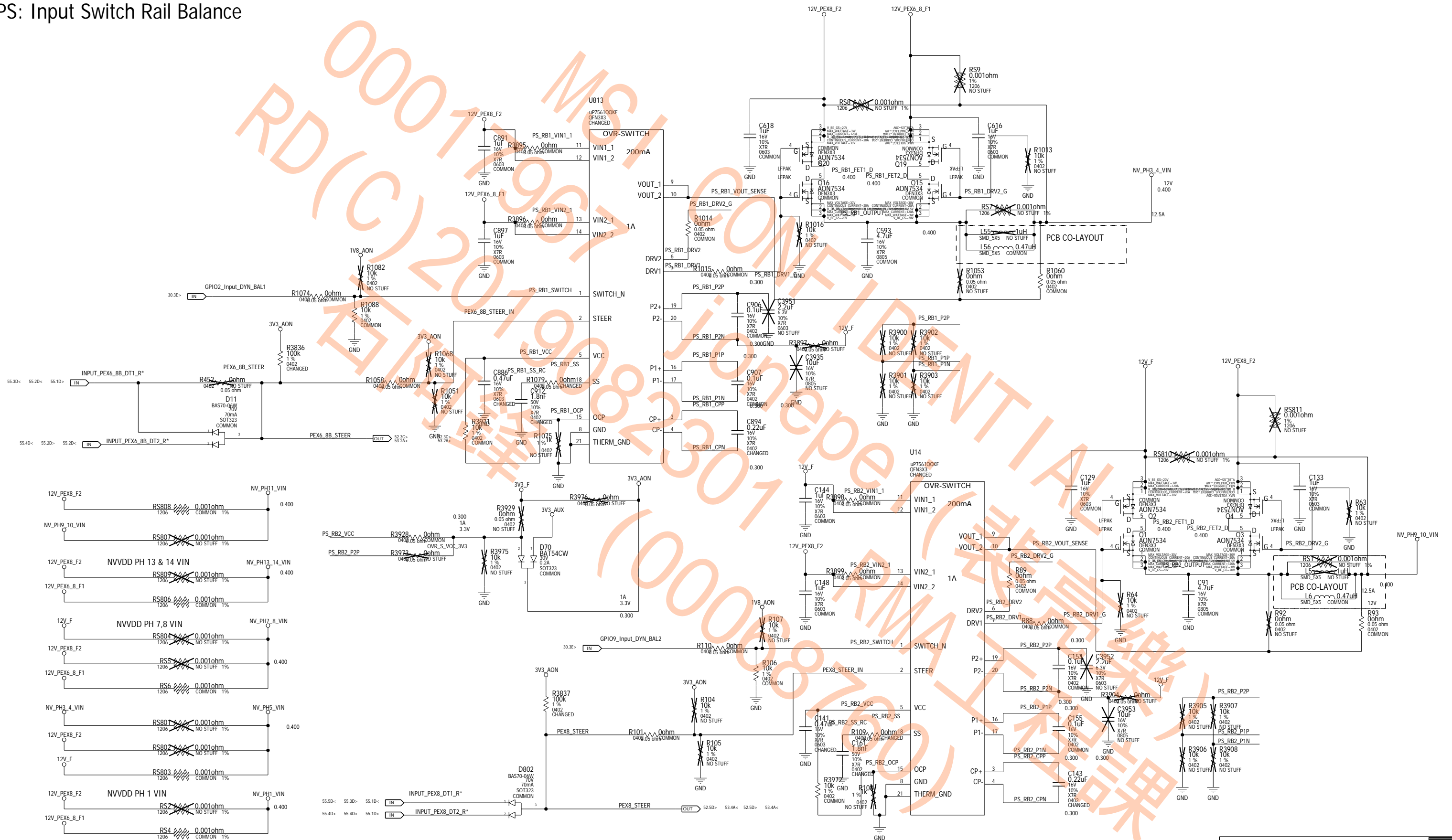
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PS: Input Switch Rail Balance



ASSEMBLY	SKU32
PAGE DETAIL	PS: INPUT SWITCH RAIL BALANCE

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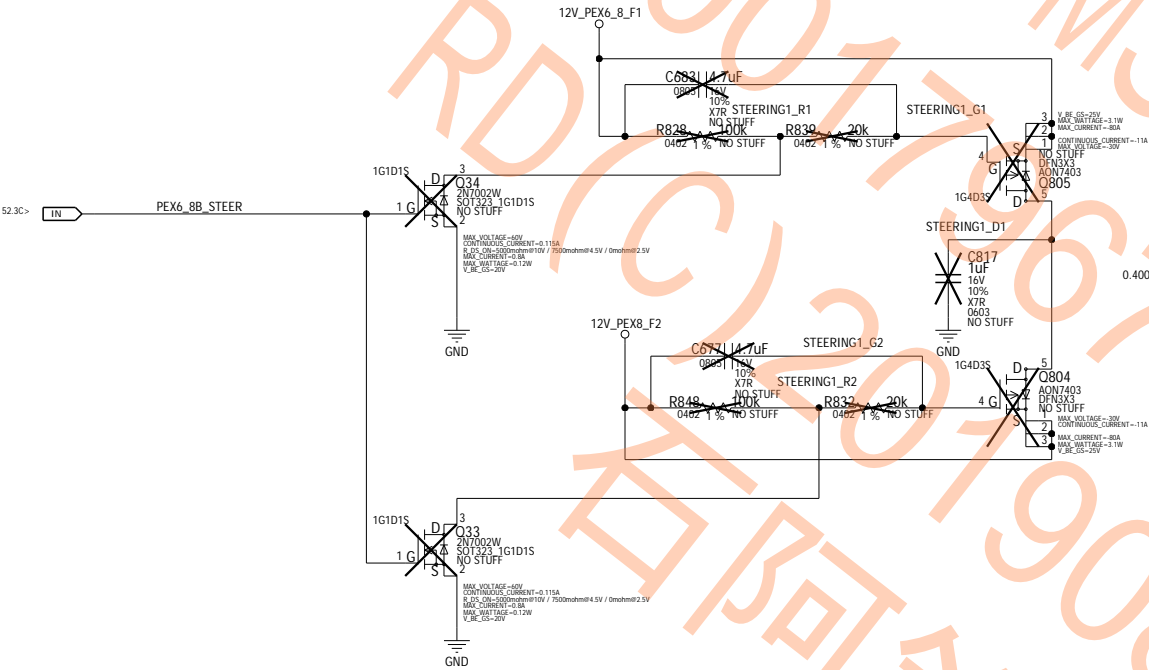
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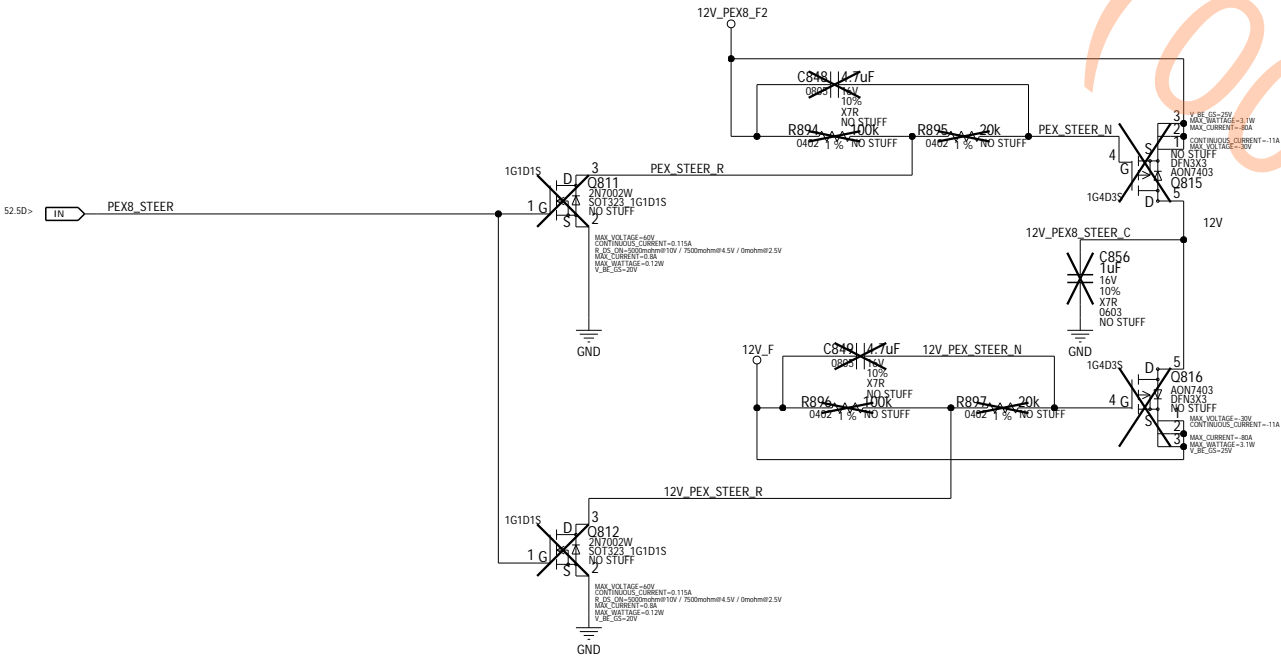
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12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



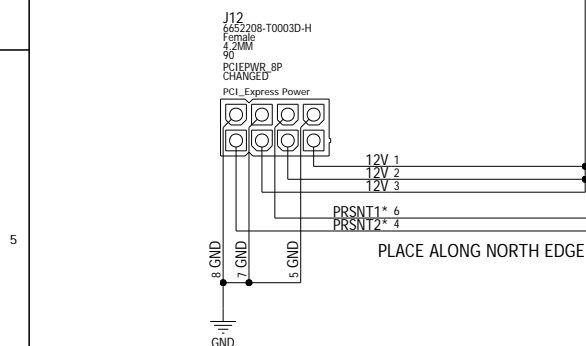
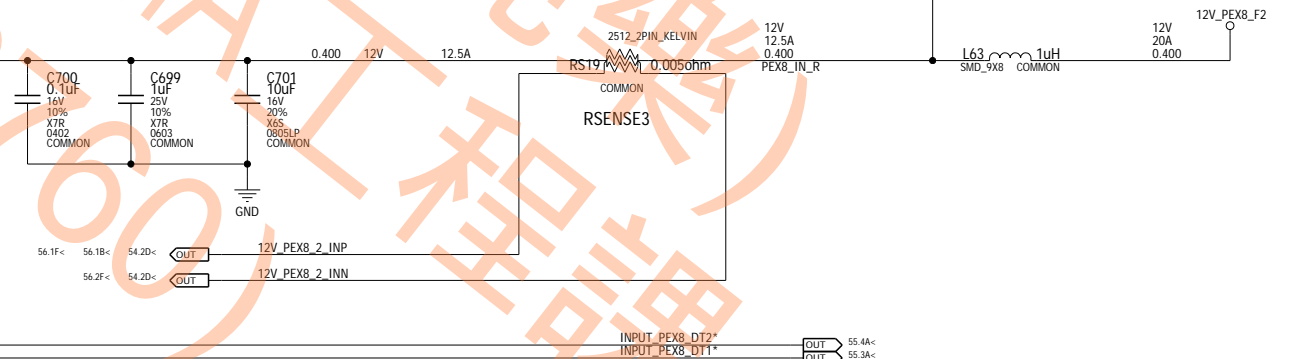
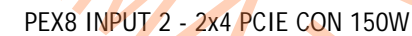
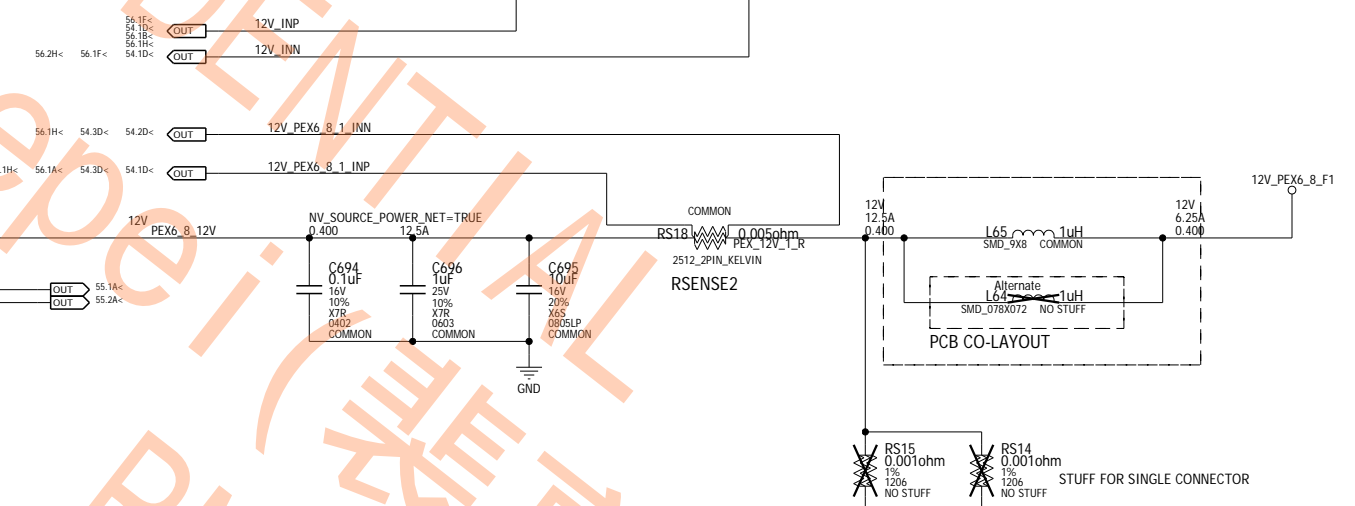
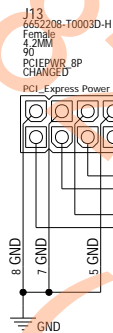
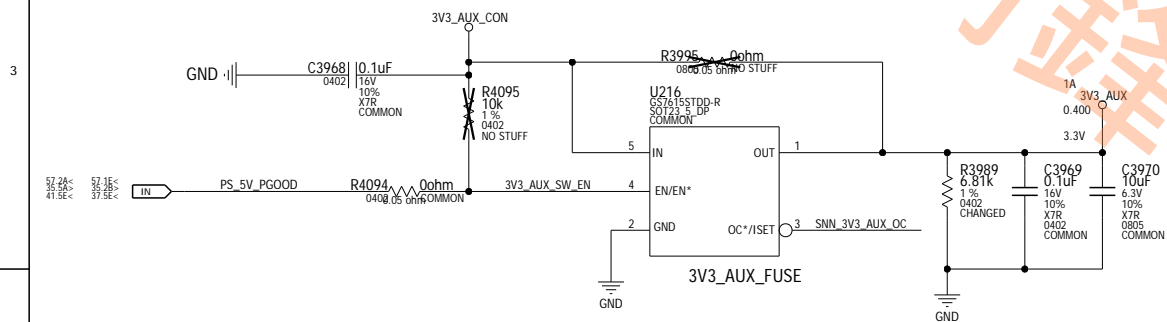
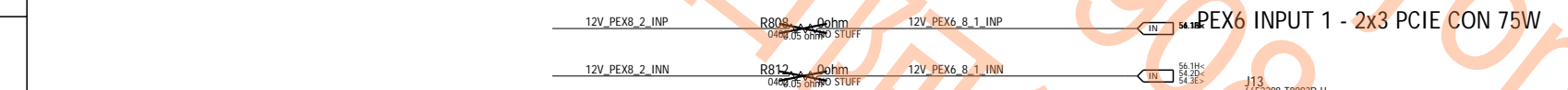
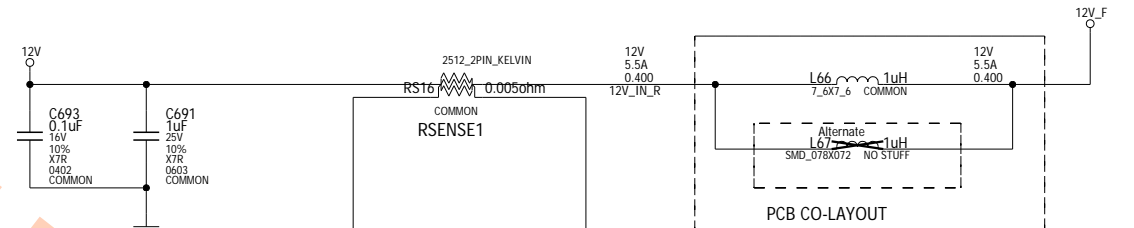
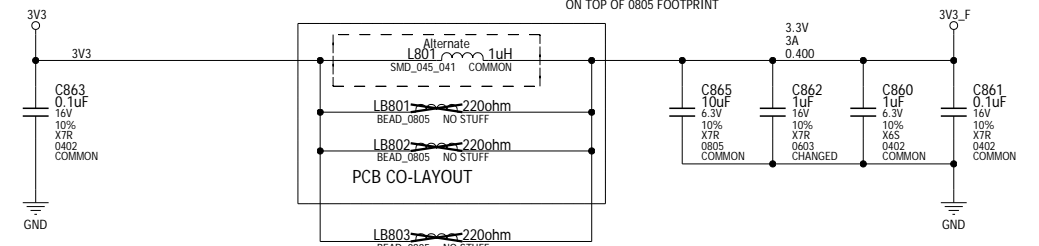
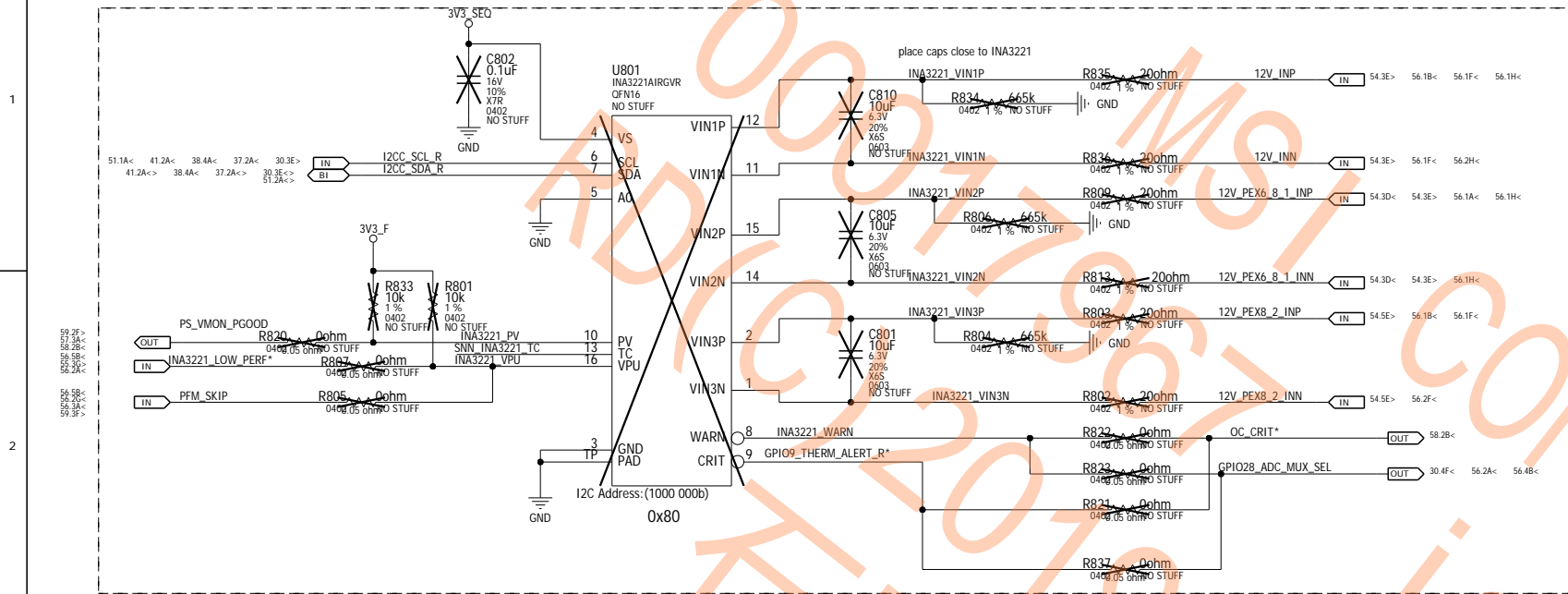
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



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PS: Inputs, Filtering, and Monitoring



ASSEMBLY	SKU32
PAGE DETAIL	PS: Input, filtering, and Monitoring

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PCB REV
BOM REV

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PS: 12V Current Steering & Hot Unplug Detect

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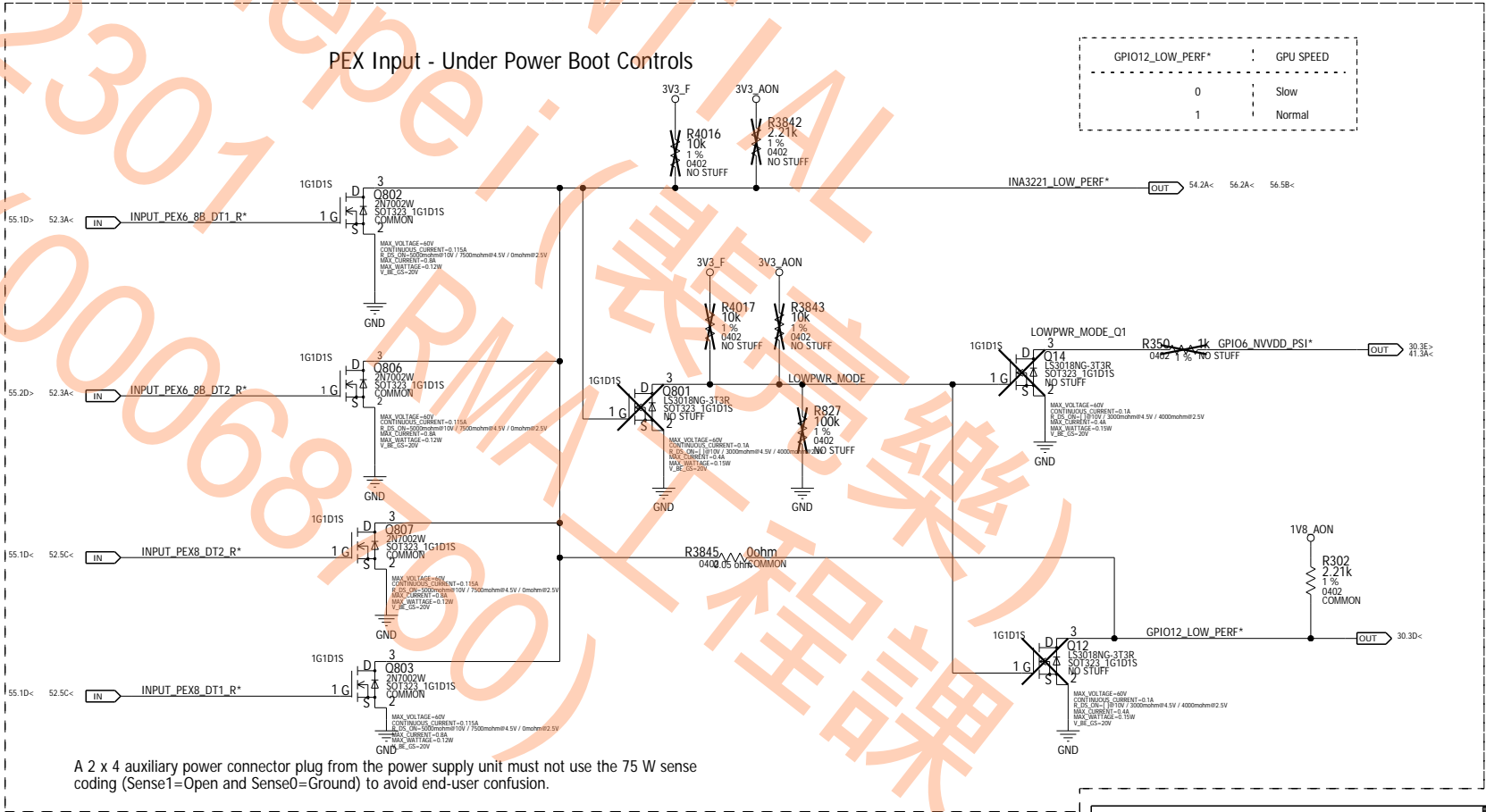
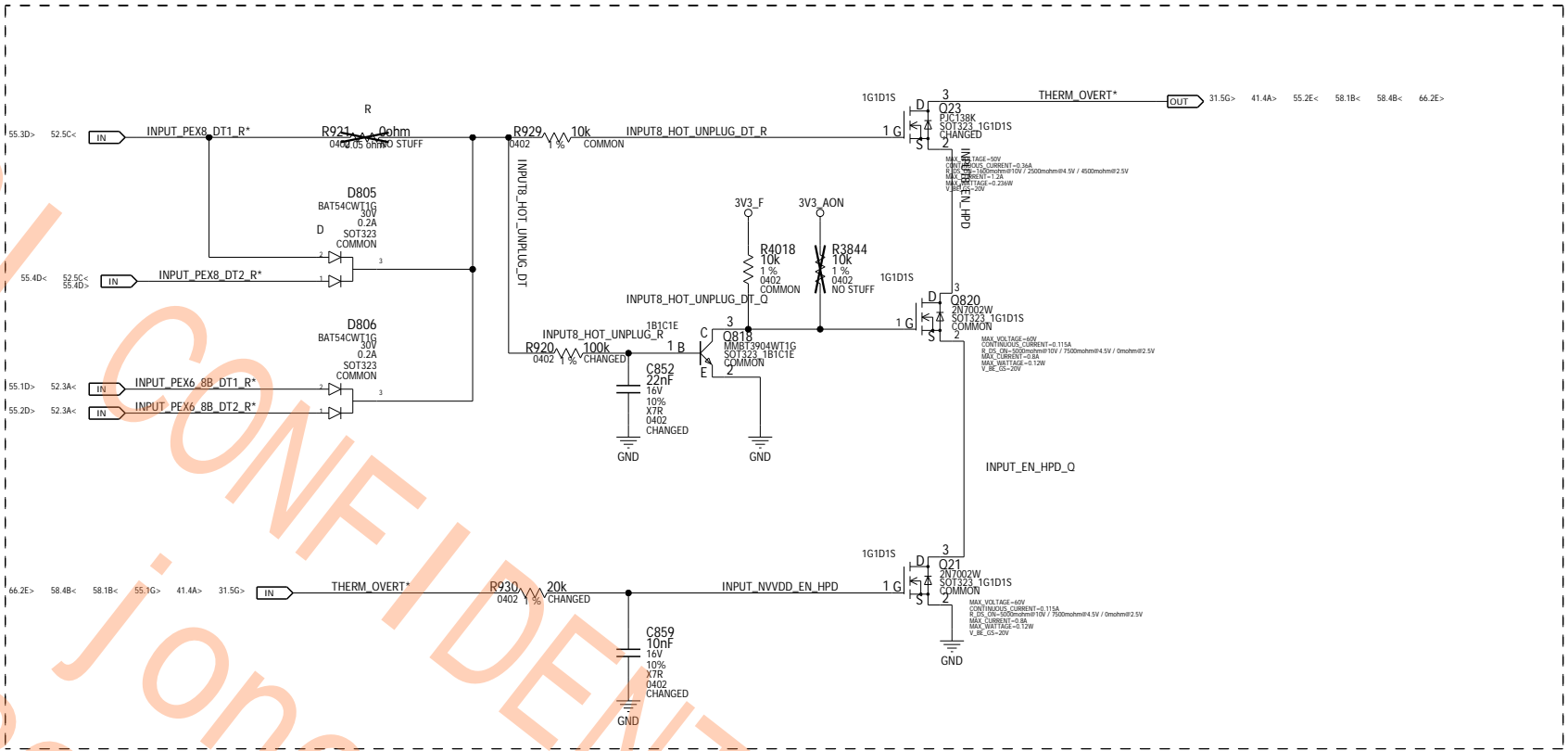
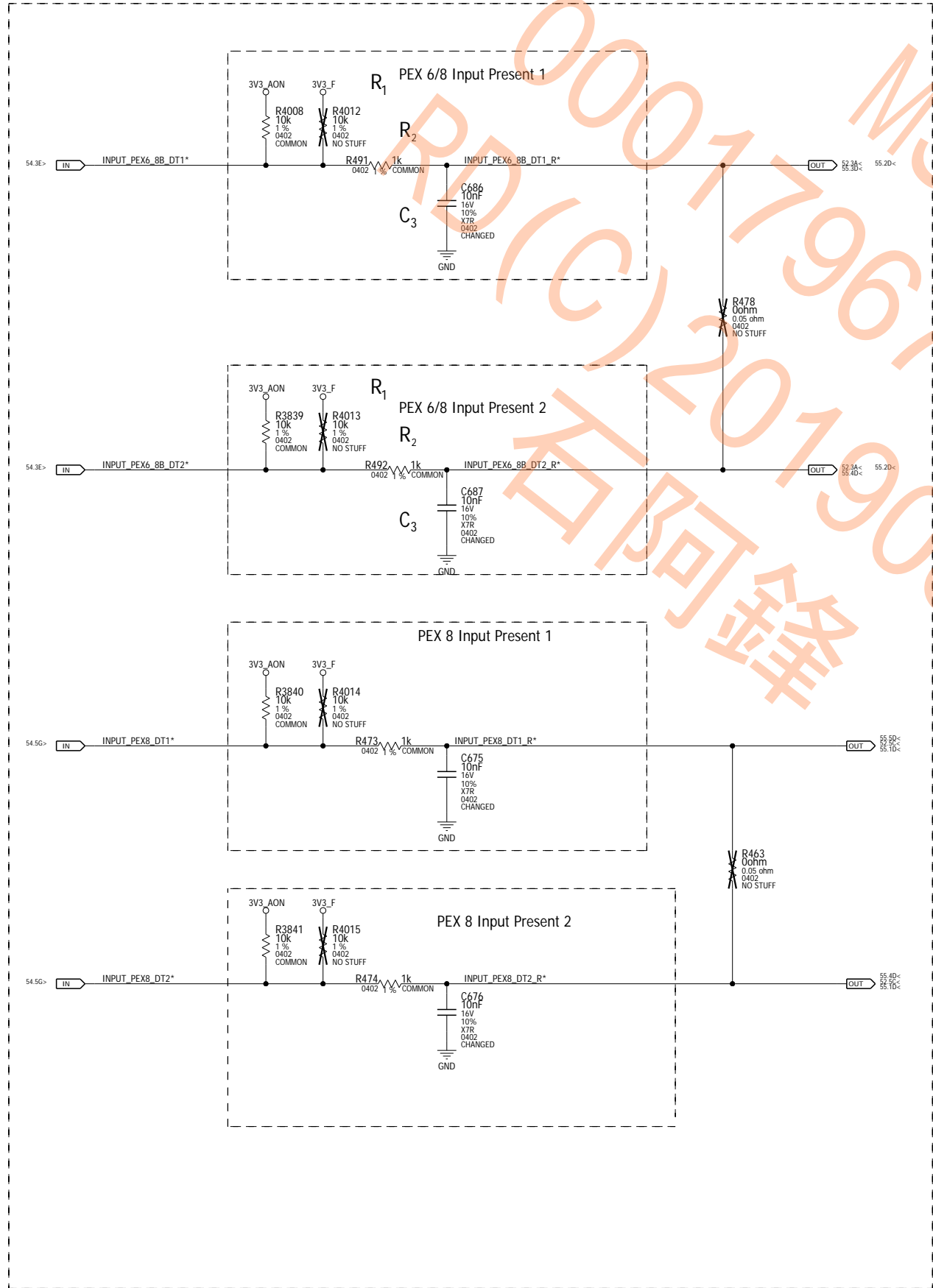
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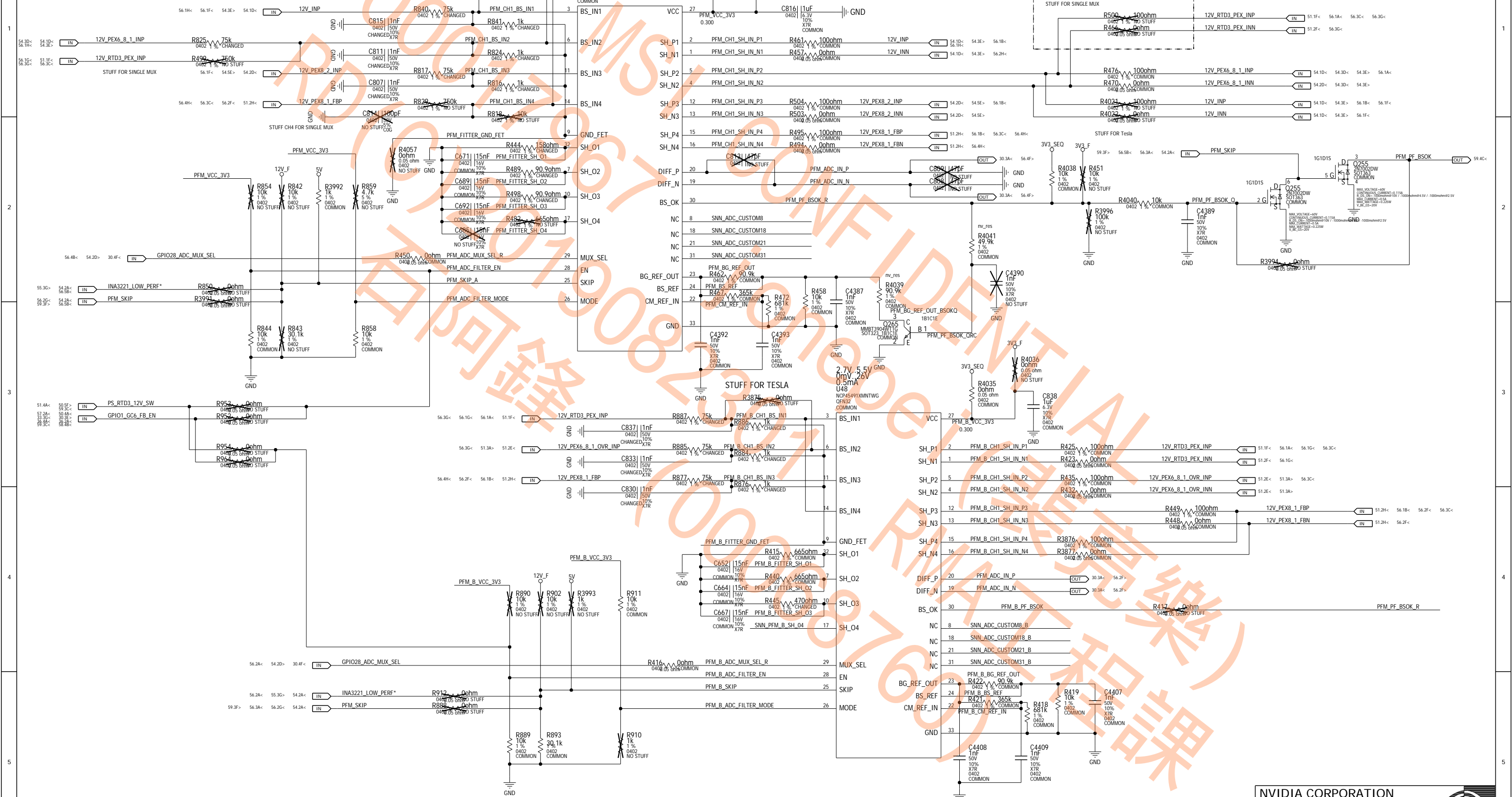
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A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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PS: Pre-Filter



ASSEMBLY	SKU32
PAGE DETAIL	PS: Pre

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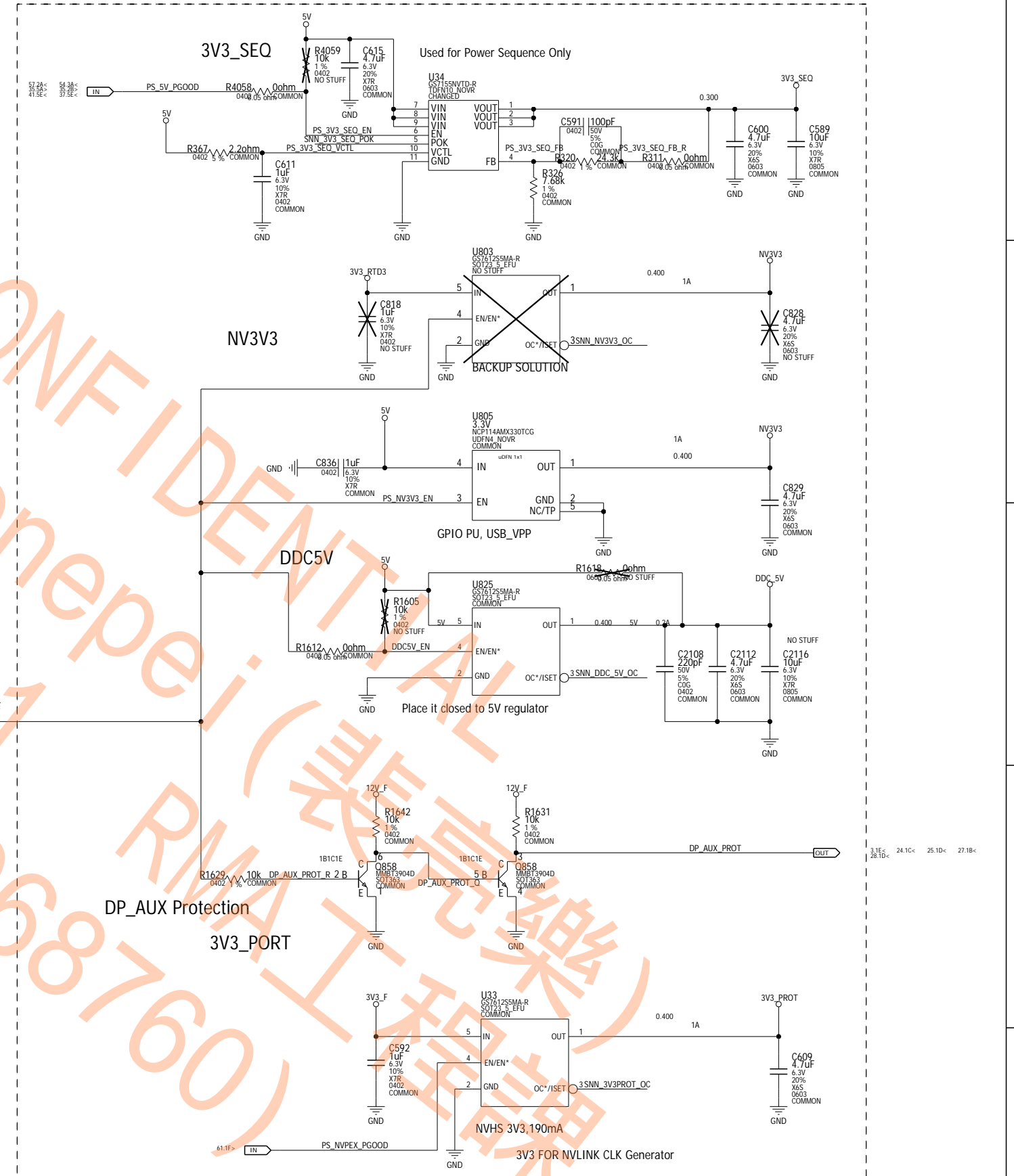
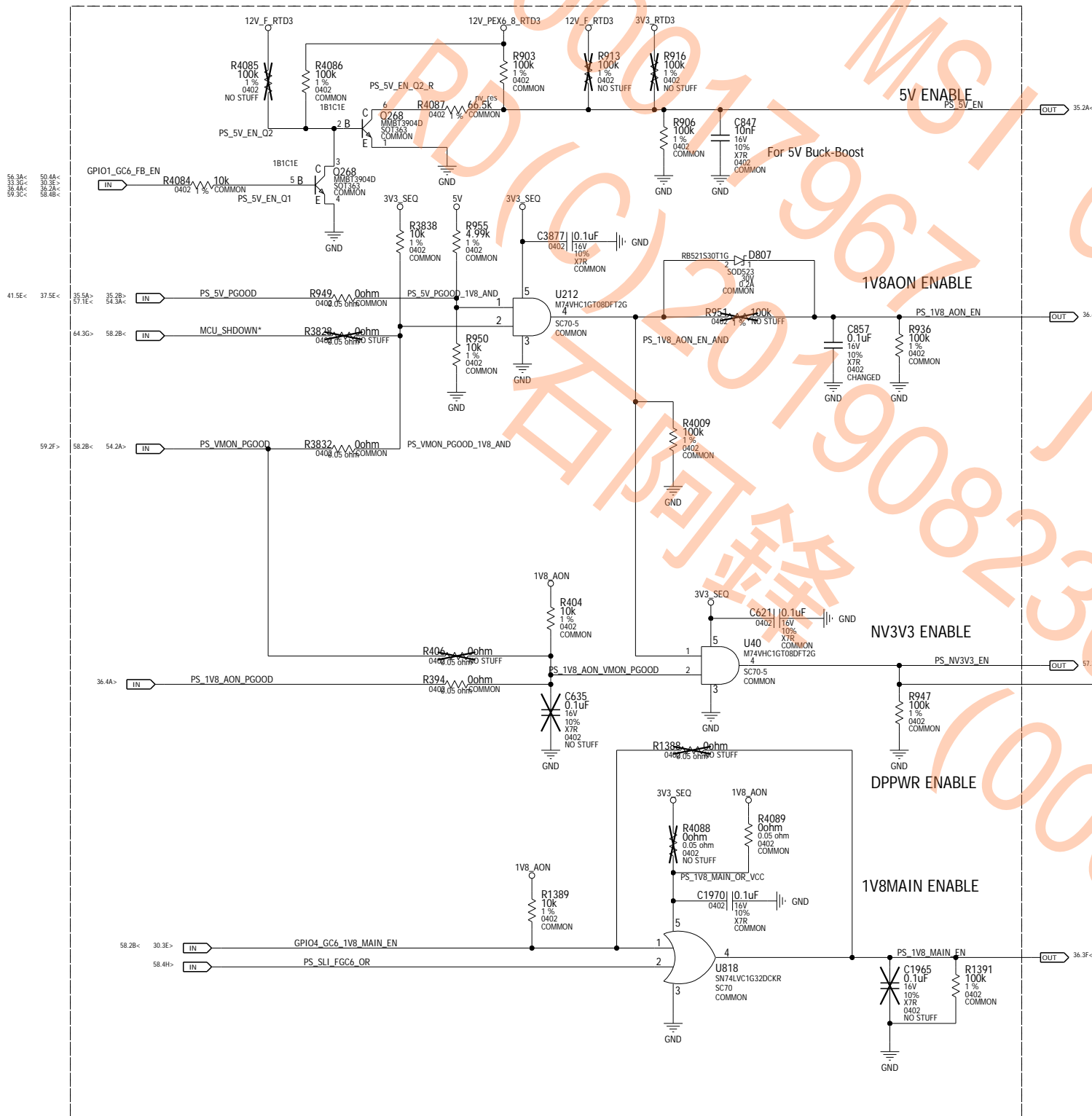
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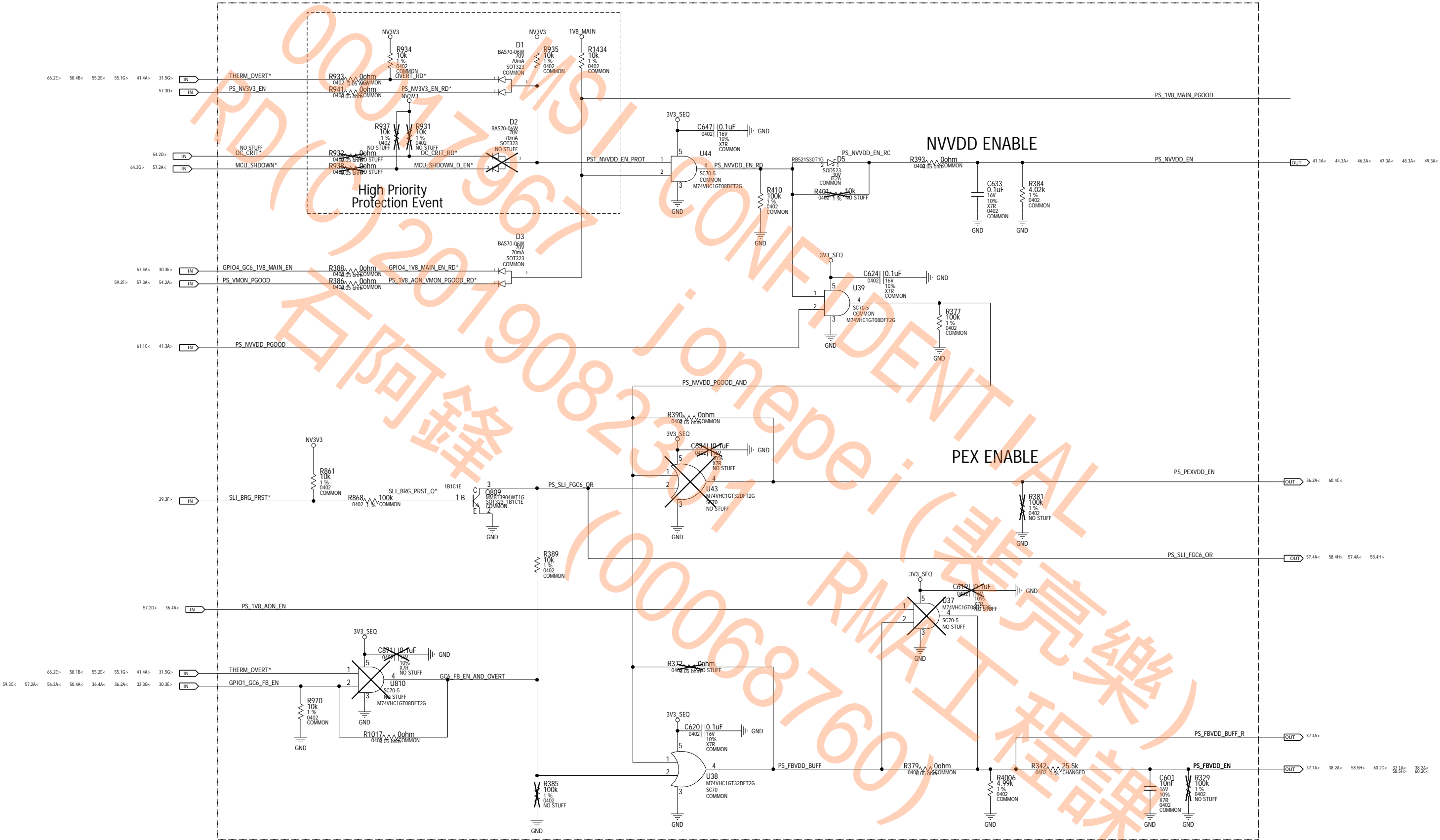
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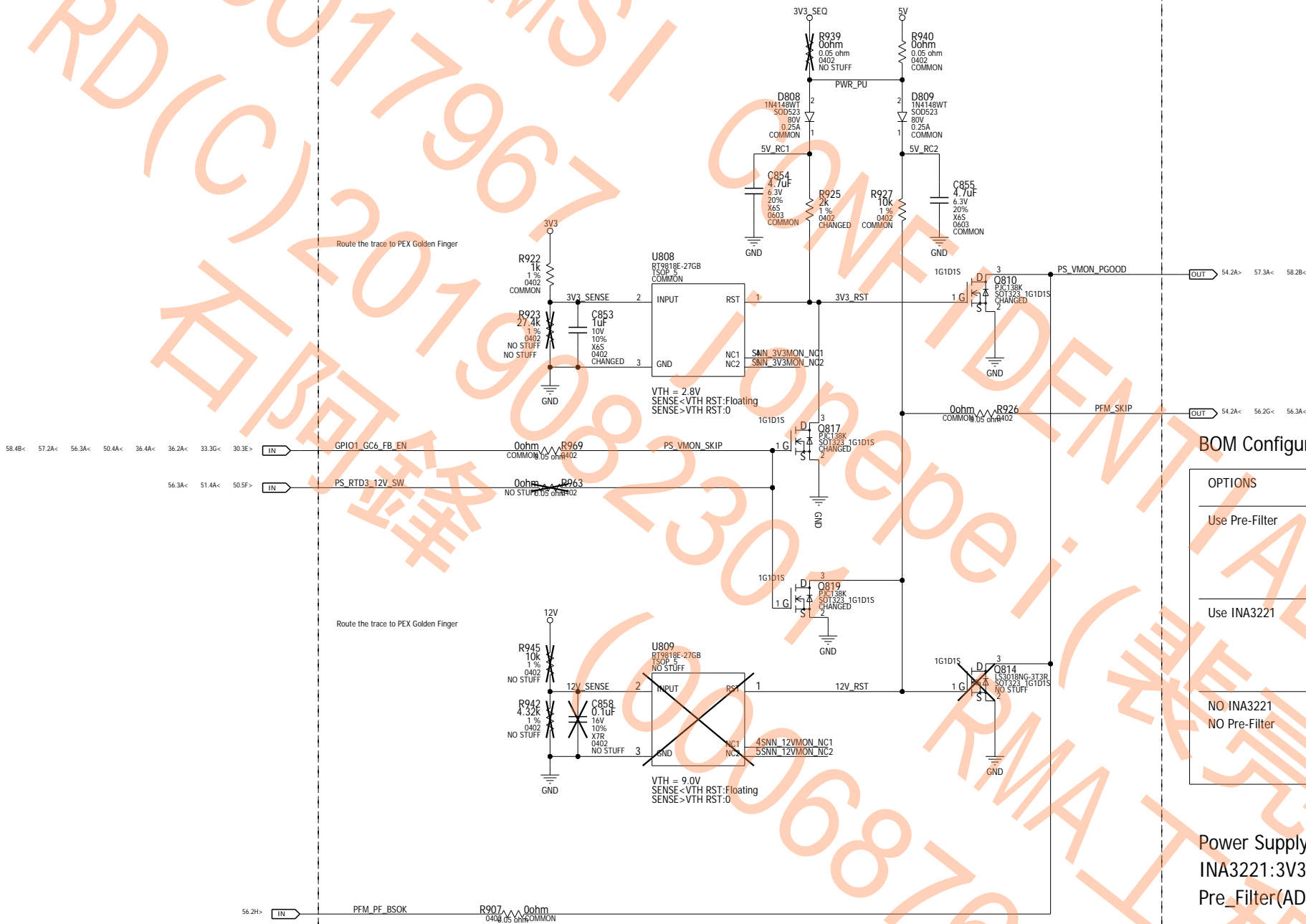
SEQUENCE:NV,PEX,FB ENABLE



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SEQUENCE:PCIE Voltage Monitor

PCIE Voltage Monitor



BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply
INA3221:3V3_SEQ
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:
Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

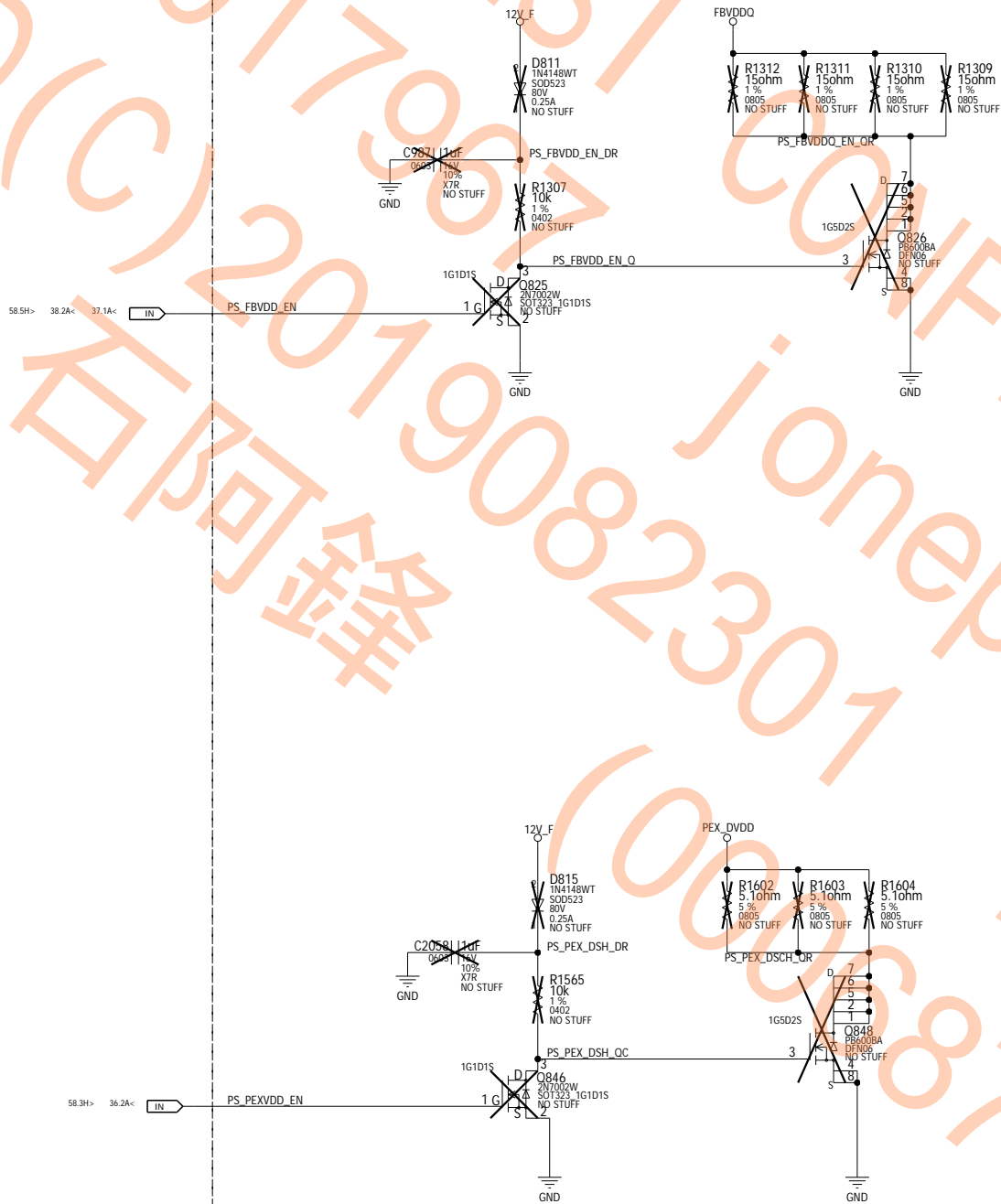
Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

ASSEMBLY	SKU32
PAGE DETAIL	Sequence: PCIE Voltage Monitor

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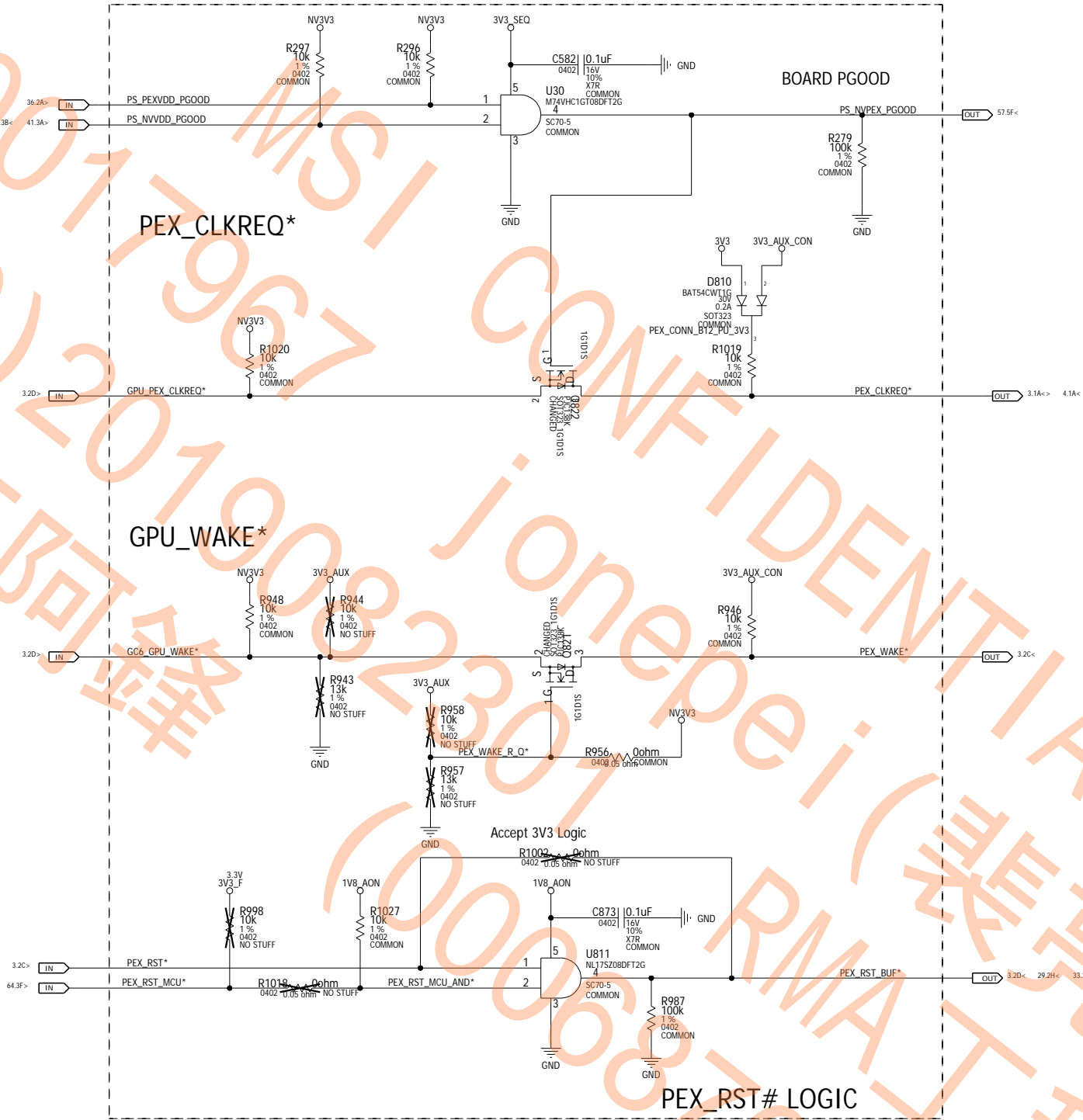
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BOM REV	F	DATE	14-NOV-2018

SEQUENCE: Discharge



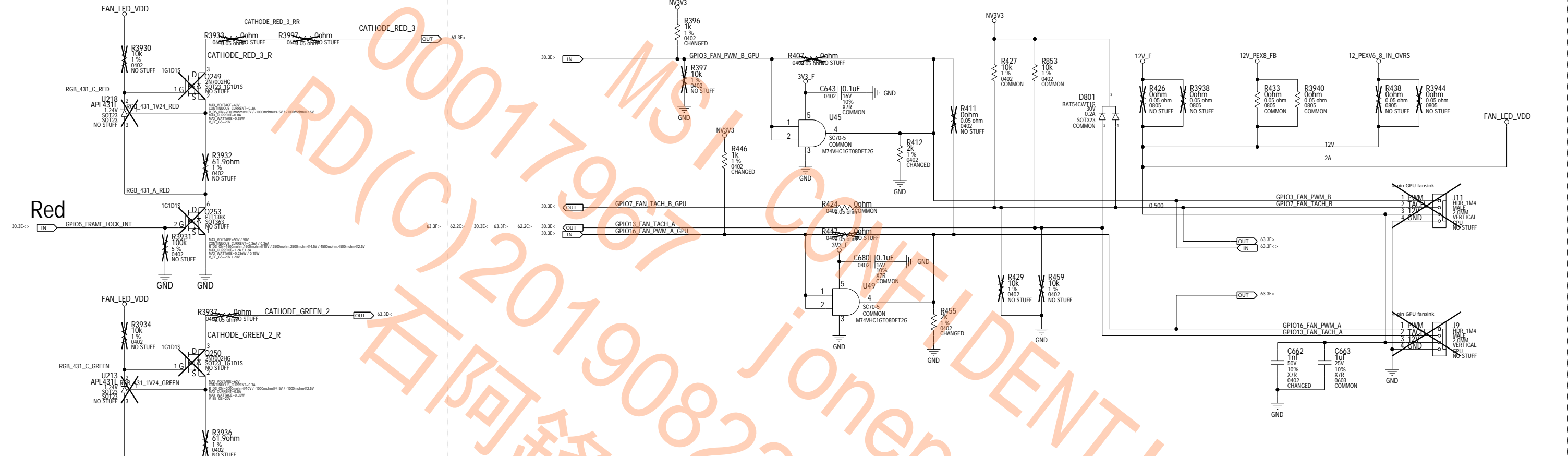
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SEQUENCE:MISC

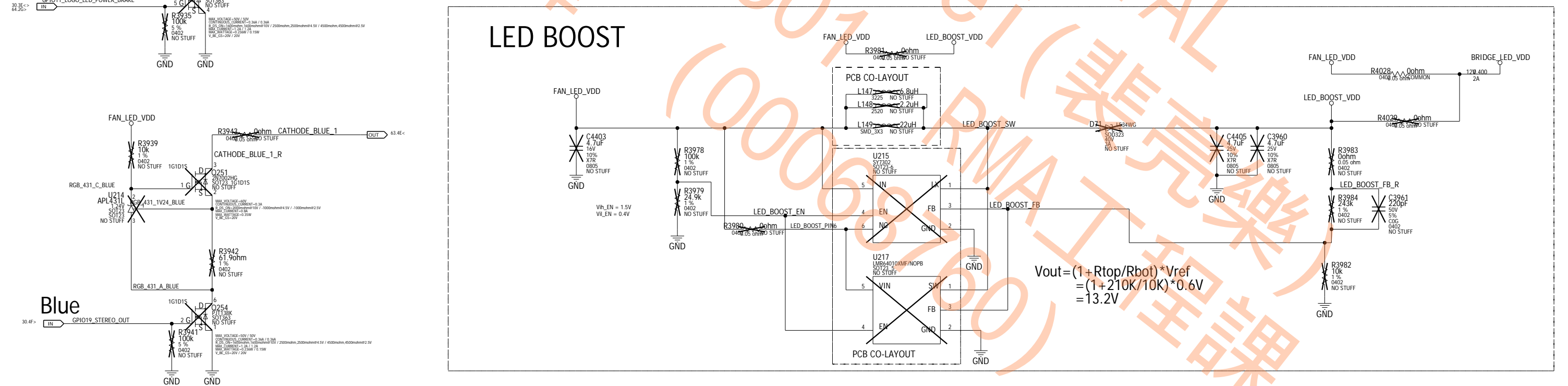



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MISC: FAN & LED1



LED BOOST



NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN		600-1G150-0032-404		
PCB REV	PG150-C04	PAGE	62 OF 66	
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MISC: LED2

1

2

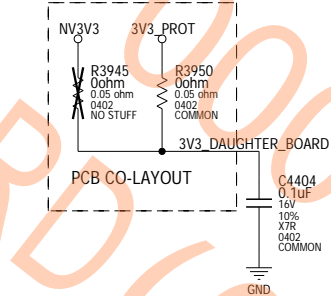
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4

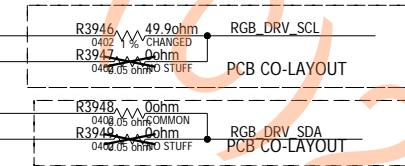
5

12V FROM FAN PAGE
FAN_LED_VDD

PLACE CAPS CLOSE TO CONNECTOR

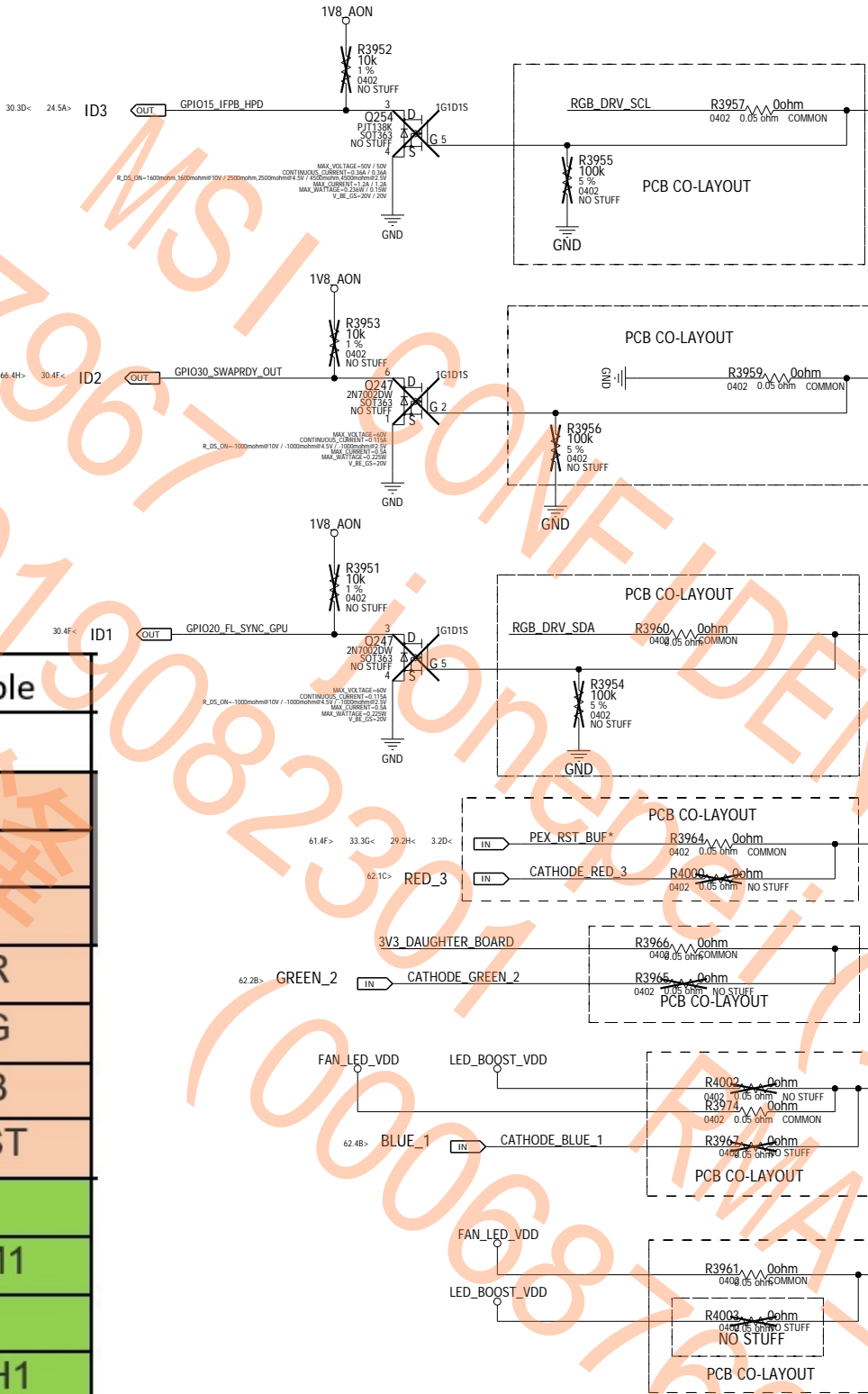


STUFF I2CB RESISTORS



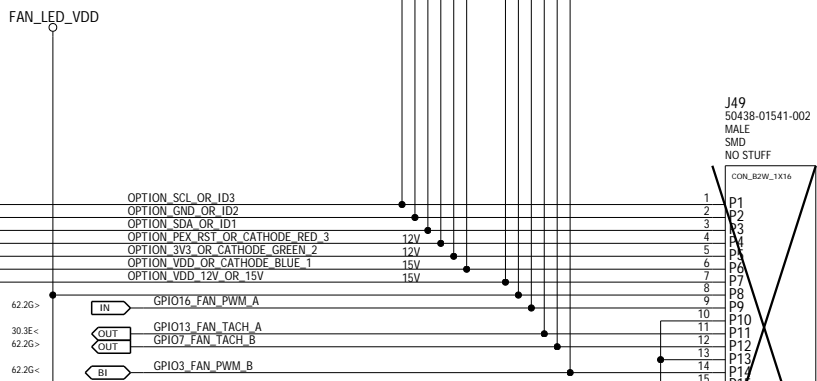
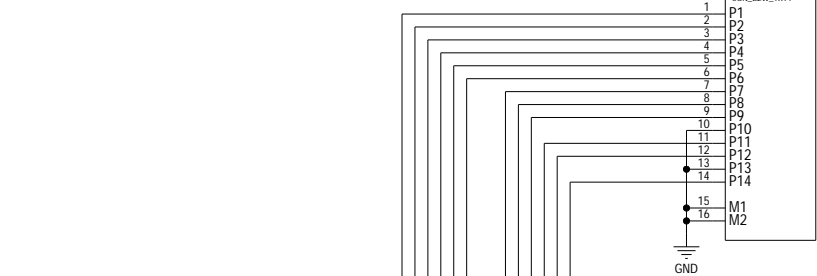
8-bit I2C Address of MCU on Daughter Board: 0x92

MCU Solution		For ONE ZONE RGB/cable	
PIN SEQ	Pin Name	PIN SEQ	Pin Name
1	I2C_SCL	1	ID3
2	GND	2	ID2
3	I2C_SDA	3	ID1
4	PEX_RST_BUF*	4	DRIVE3/R
5	NV3V3	5	DRIVE2/G
6	12V/BOOST	6	DRIVE1/B
7	12V	7	12V/BOOST
8	12V	8	12V
9	FAN_PWM1	9	FAN_PWM1
10	GND	10	GND
11	FAN_TACH1	11	FAN_TACH1
12	FAN_TACH2	12	FAN_TACH2
13	GND	13	GND
14	FAN_PWM2	14	FAN_PWM2
		15	12V



14-PIN STRAIGHT PRIMARY SOURCE -> 080-1586-000: ACES \$0.115
14-PIN STRAIGHT SECOND SOURCE -> 080-1600-000: WIESON \$0.2

FOR MCU SOLUTION



FOR ONE ZONE RGB SOLUTION

15-PIN STRAIGHT PRIMARY SOURCE -> 080-1617-000: ACES \$0.1165
15-PIN STRAIGHT SECOND SOURCE -> 080-1628-000: WIESON \$0.23

NVIDIA CORPORATION

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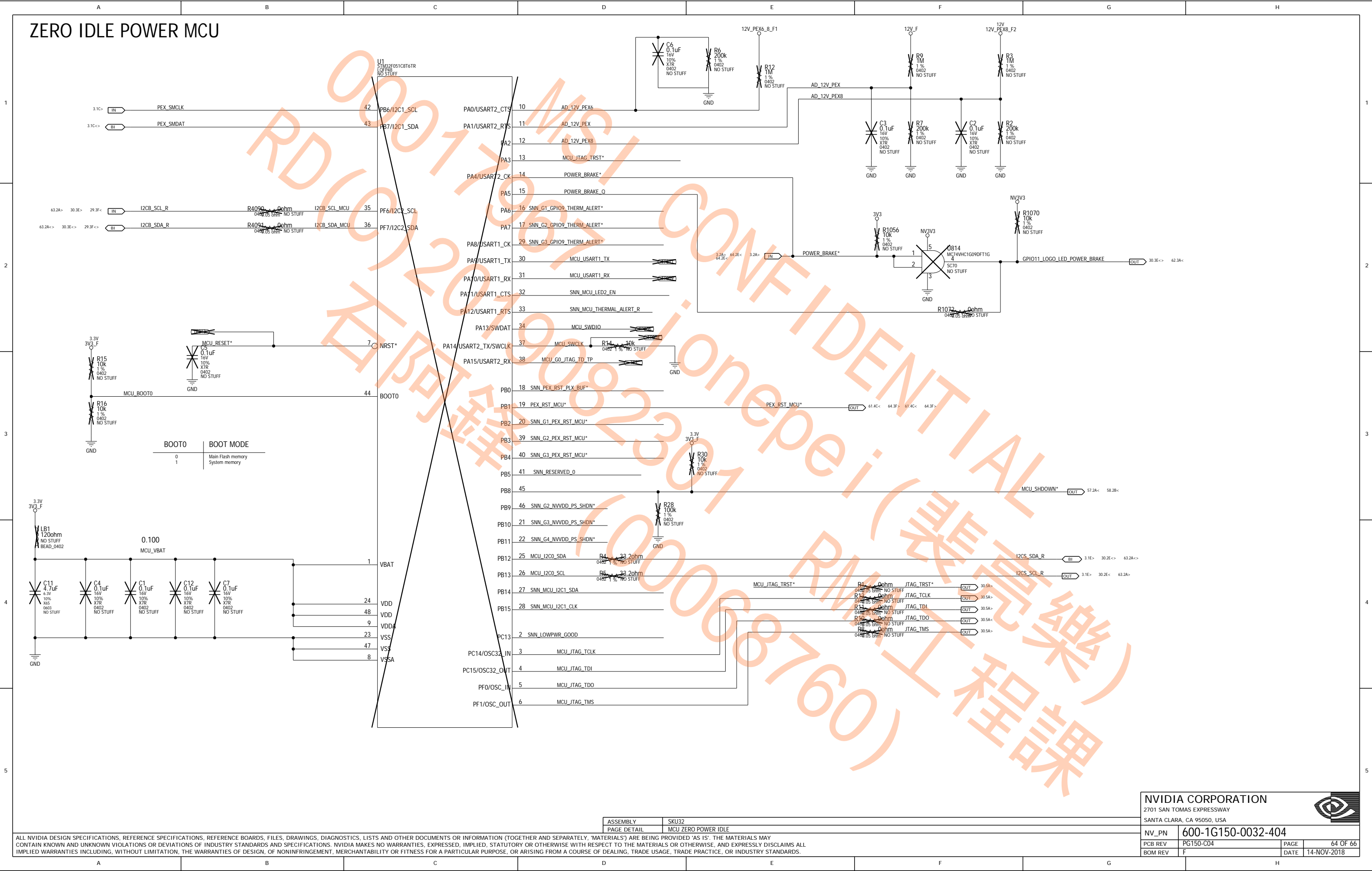
BOM REV F

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DATE 14-NOV-2018

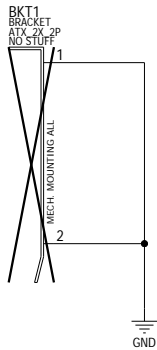
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ZERO IDLE POWER MCU

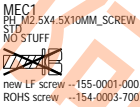


Mechanical: Bracket/Thermal Solution

Brackets:



Bracket Screw



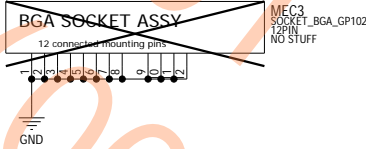
Back Cover



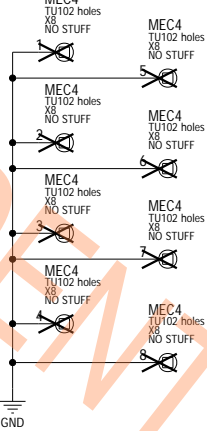
GPU Stiffner back side



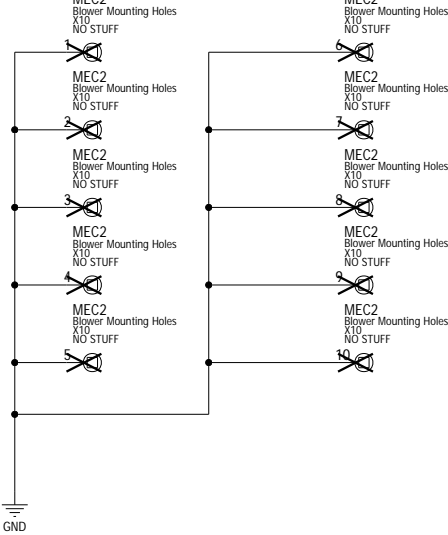
GPU Socket Symbol



GPU Mounting holes

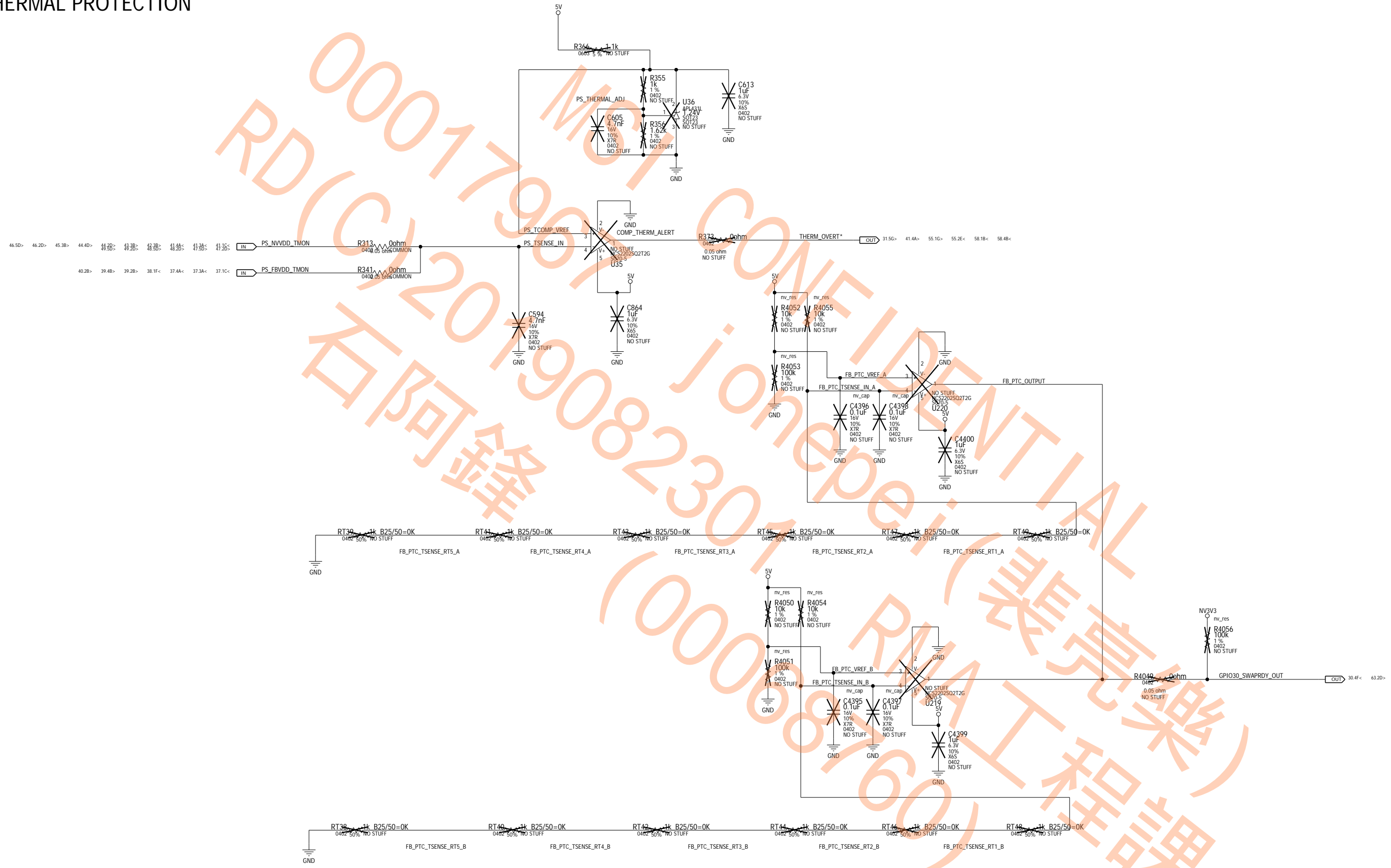


Mechanical Holes Symbol



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VR THERMAL PROTECTION



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