

1

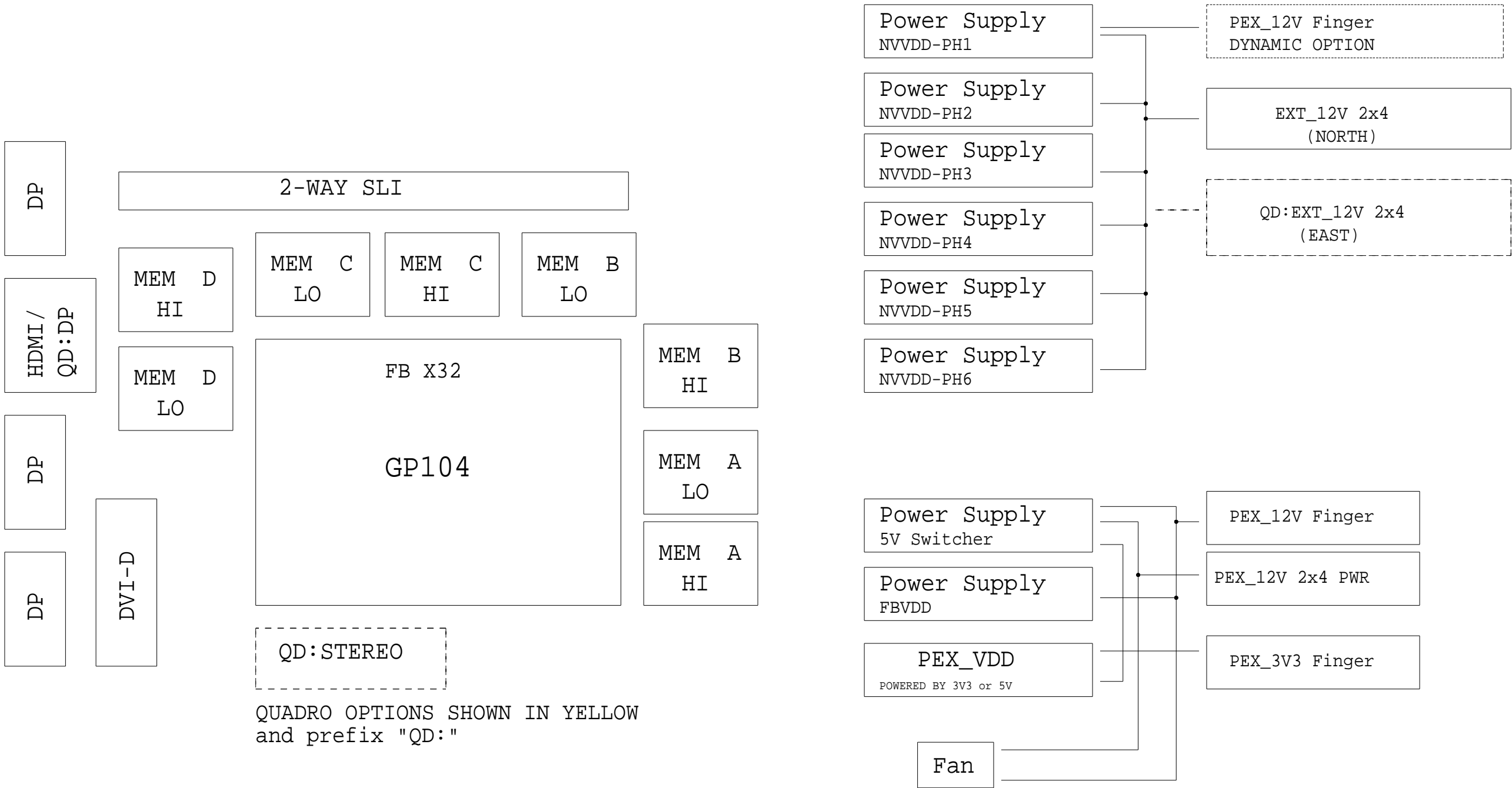
1

2

3234

4

5



QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

12V

PLACE 0603 4.7uF FOOTPRINT
ON TOP OF 0805 FOOTPRINT

Part	Value	Footprint	Notes
C43	4.7uF	16V	X5R 0603 NO STUFF
C1079	4.7uF	16V	X5R 0603 NO STUFF
C44	4.7uF	16V	X5R 0805 COMMON
C1078	4.7uF	16V	X5R 0805LP COMMON

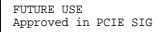


Figure 10 shows the PCB layout for the PEX VDD supply, divided into three sections: "Place under GPU", "Place between GPU and PS", and "Place under GPU".

Place under GPU:

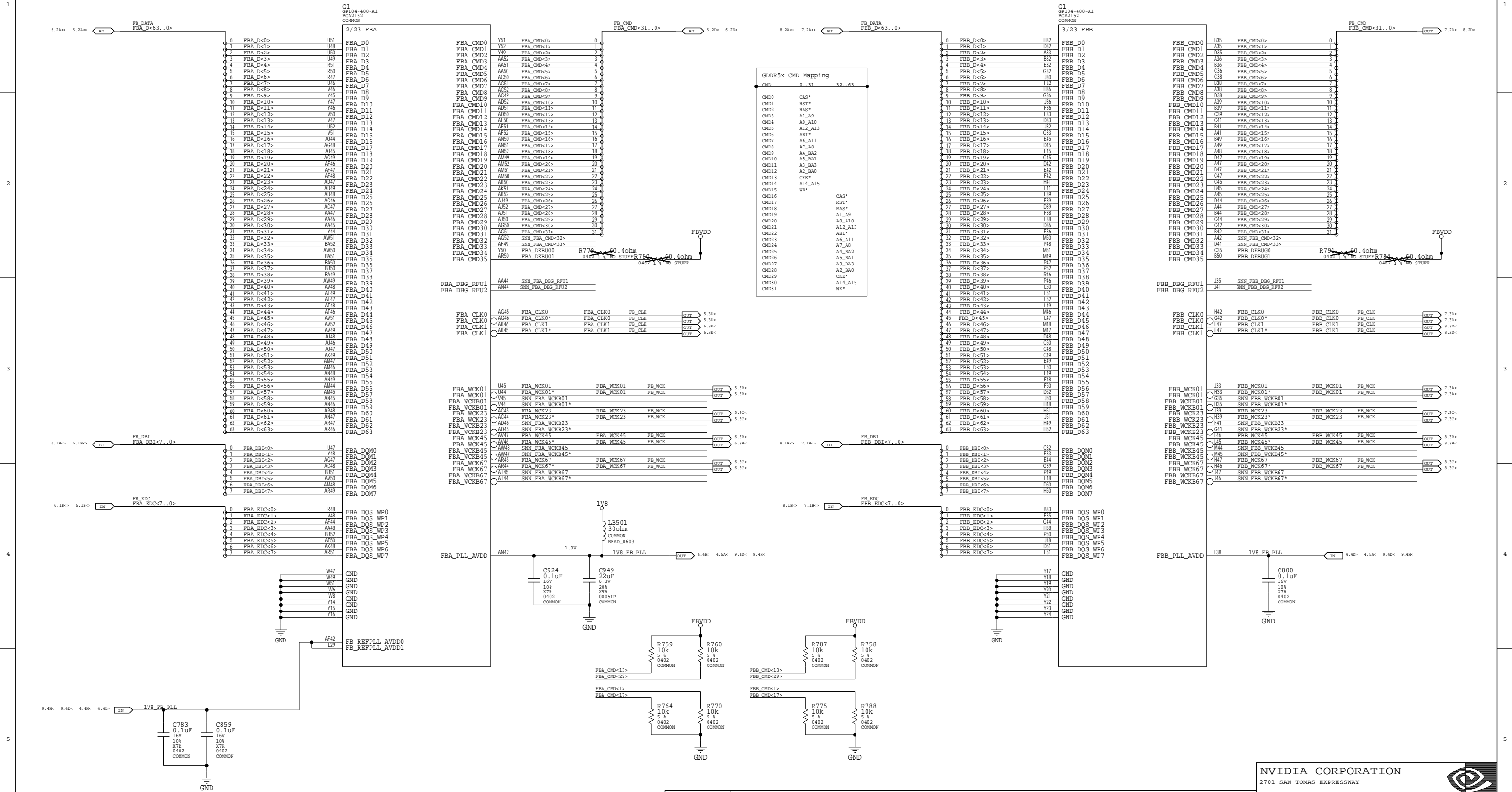
- C822 1uF, 6.3V, 10%, XSR, 0402 COMMON
- C841 1uF, 6.3V, 10%, XSR, 0402 COMMON
- C817 1uF, 6.3V, 10%, XSR, 0402 COMMON
- C832 1uF, 6.3V, 10%, XSR, 0402 COMMON
- C754 4.7uF, 6.3V, 20%, XSR, 0603 COMMON
- C112 4.7uF, 6.3V, 20%, XSR, 0603 COMMON
- C106 10uF, 6.3V, 20%, XSR, 0805LP COMMON
- C748 22uF, 6.3V, 20%, XSR, 0805LP COMMON

Place between GPU and PS:

- C957 1uF, 6.3V, 10%, XSR, 0402 COMMON
- C880 1uF, 6.3V, 10%, XSR, 0402 COMMON
- C966 1uF, 6.3V, 10%, XSR, 0402 COMMON
- C867 1uF, 6.3V, 10%, XSR, 0402 COMMON
- C979 4.7uF, 6.3V, 20%, XSR, 0603 COMMON
- C845 4.7uF, 6.3V, 20%, XSR, 0603 COMMON
- C1029 10uF, 6.3V, 20%, XSR, 0805LP COMMON
- C1028 10uF, 6.3V, 20%, XSR, 0805LP COMMON
- C1021 22uF, 6.3V, 20%, XSR, 0805LP COMMON

The layout also shows a PEX VDD pin connected to a 1V8 voltage source and a GND connection.

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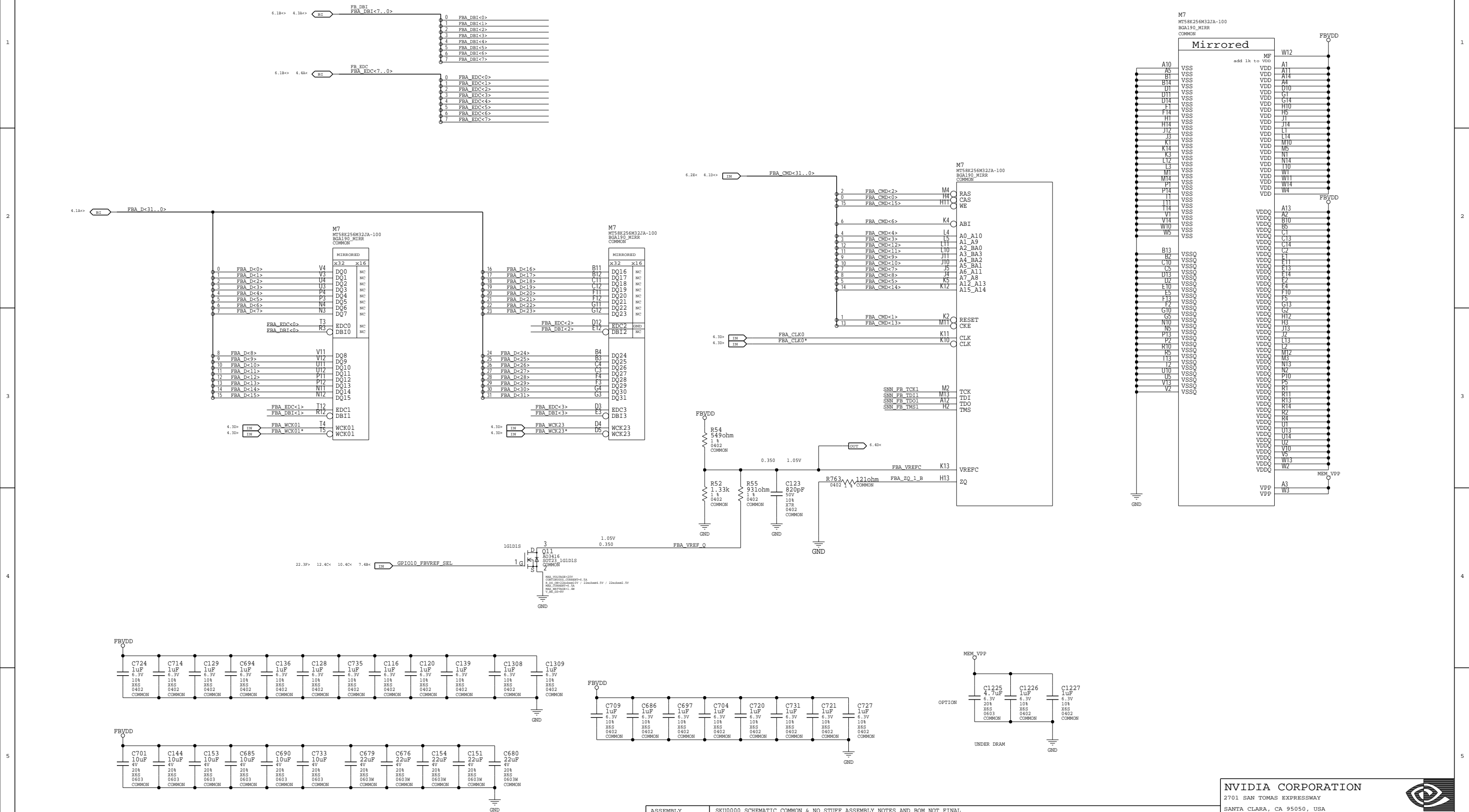
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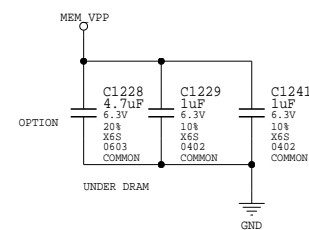
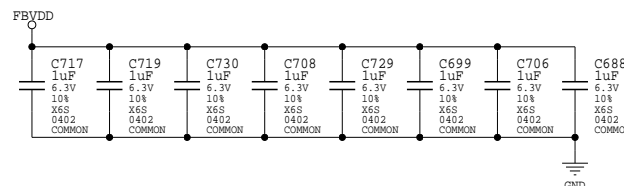
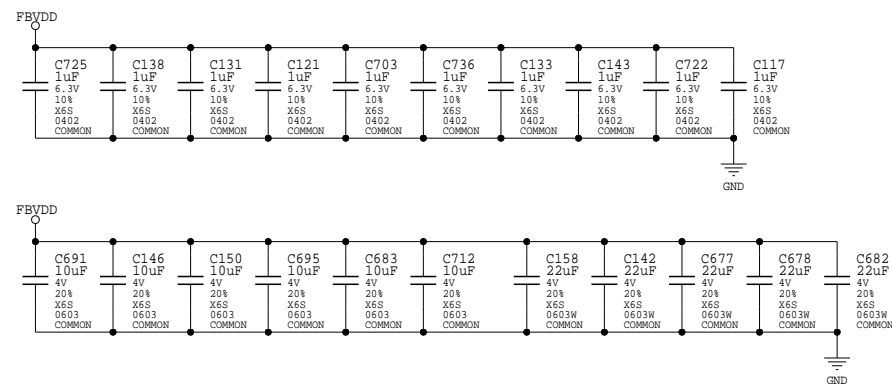
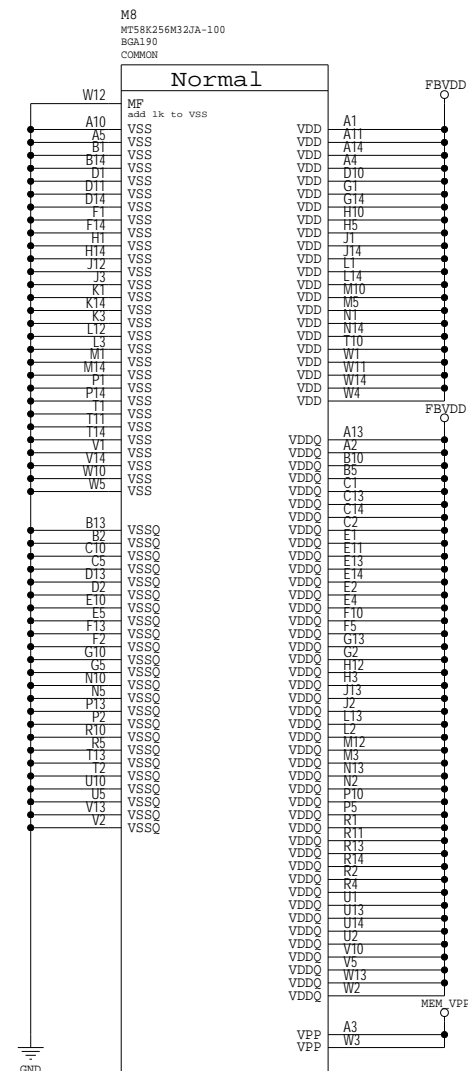
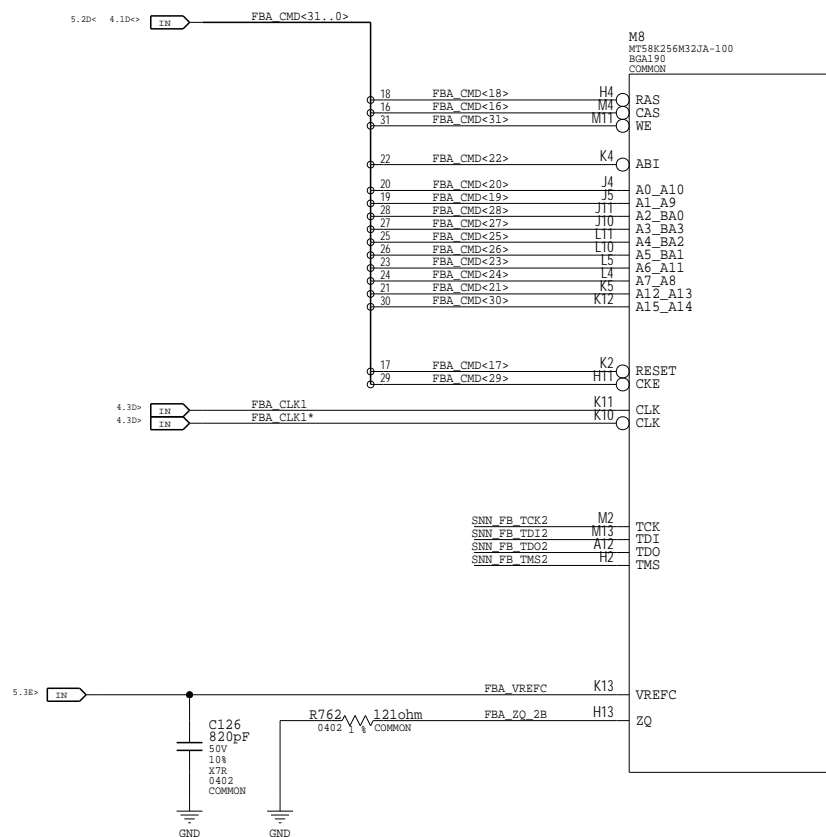
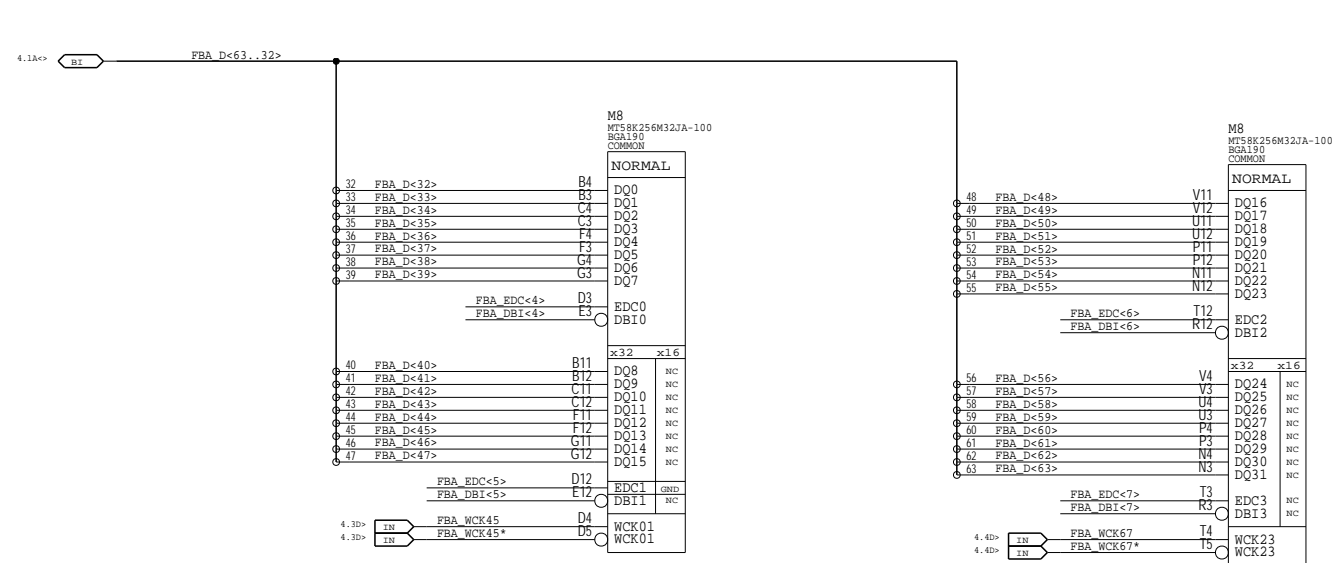
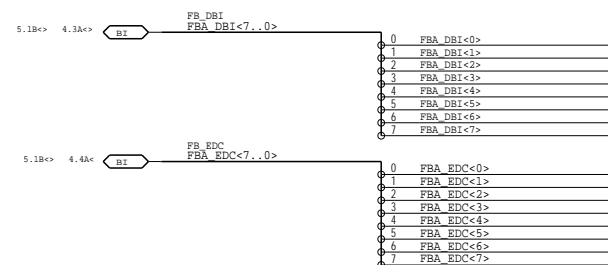
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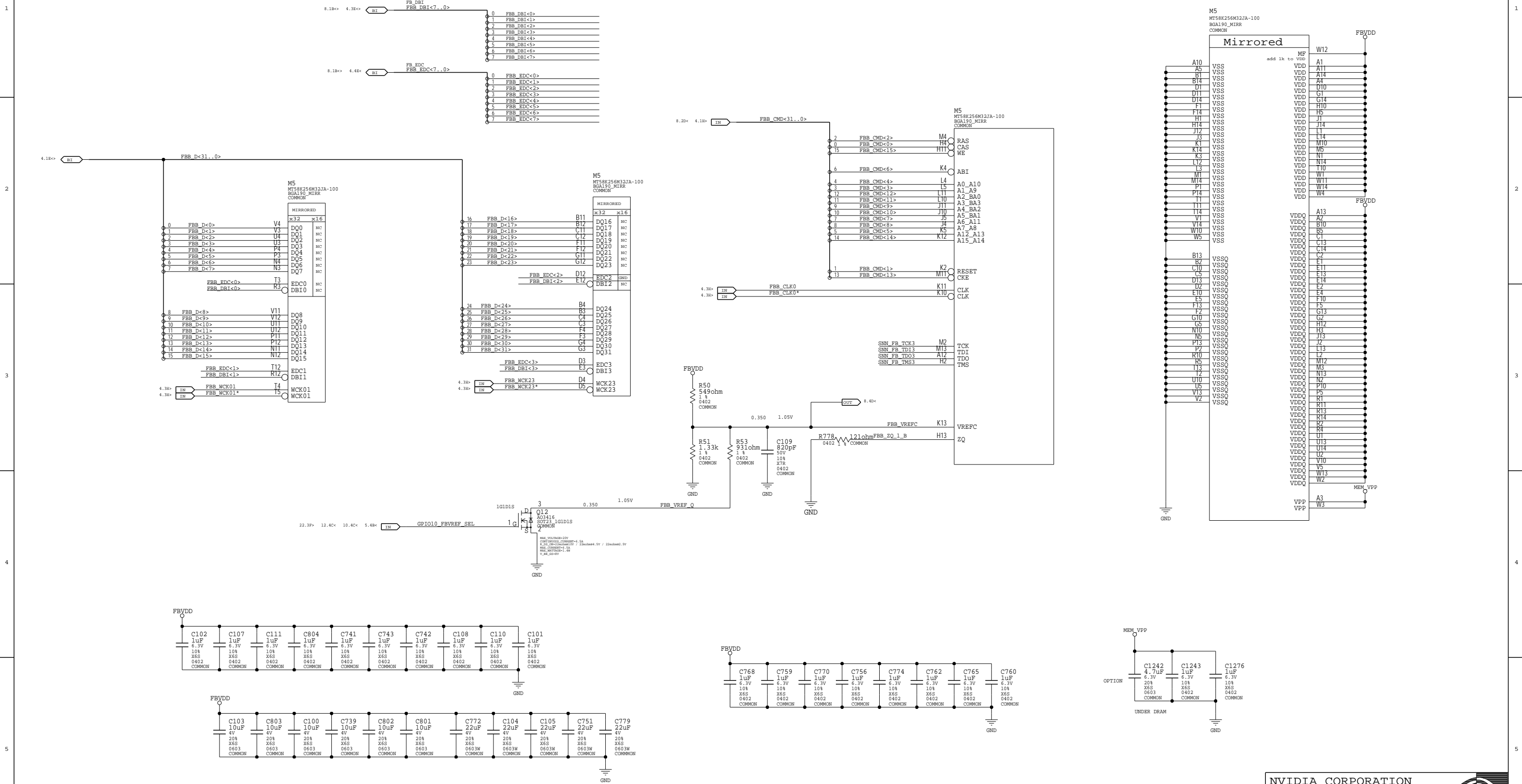
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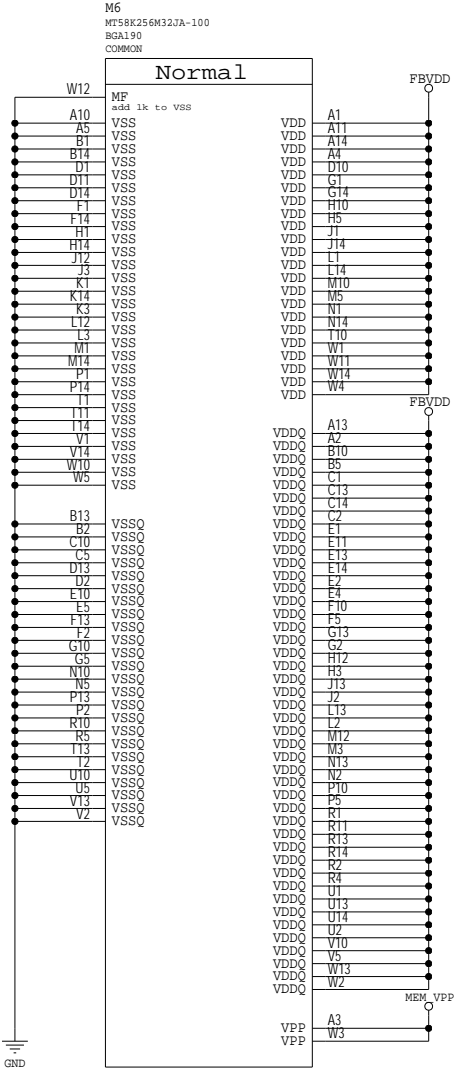
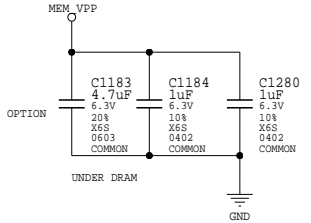
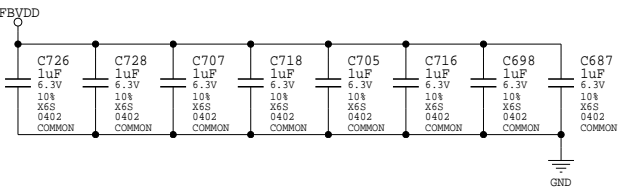
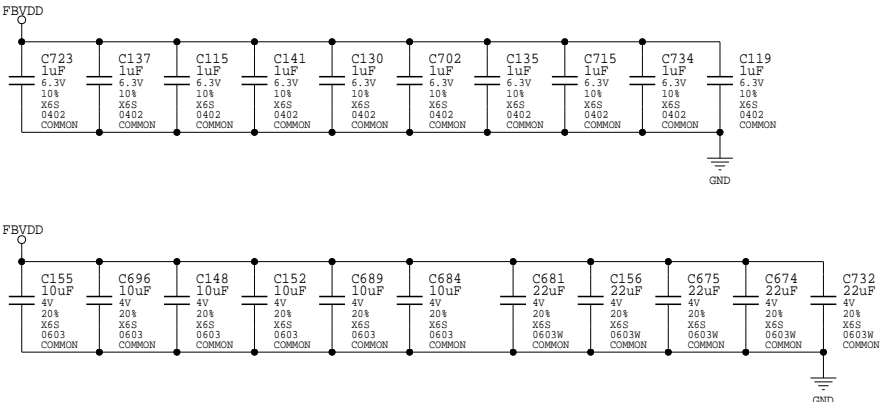
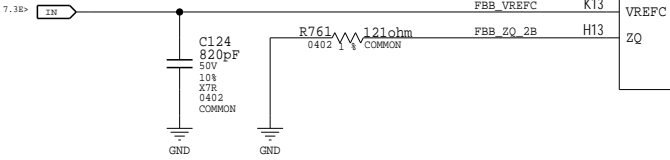
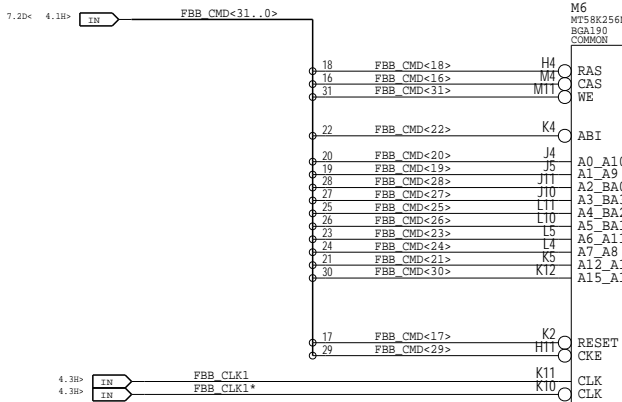
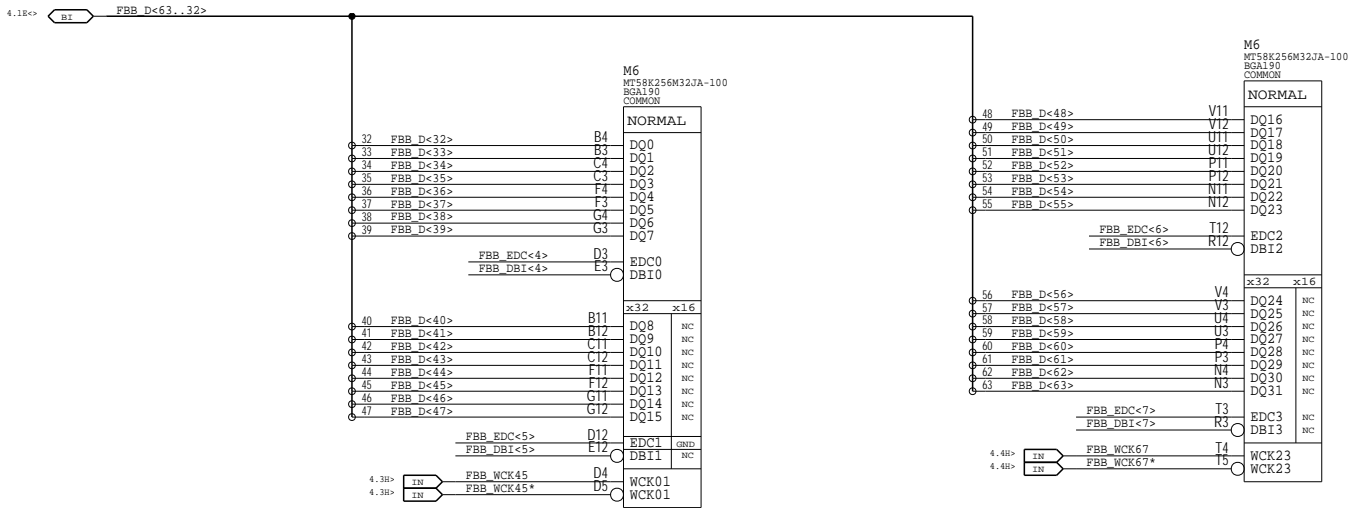
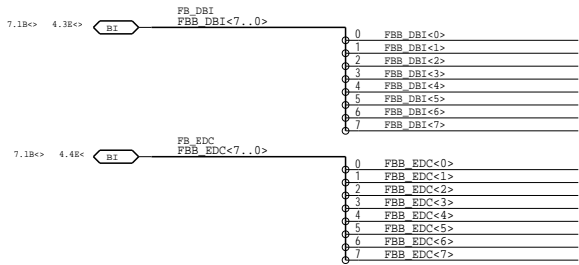


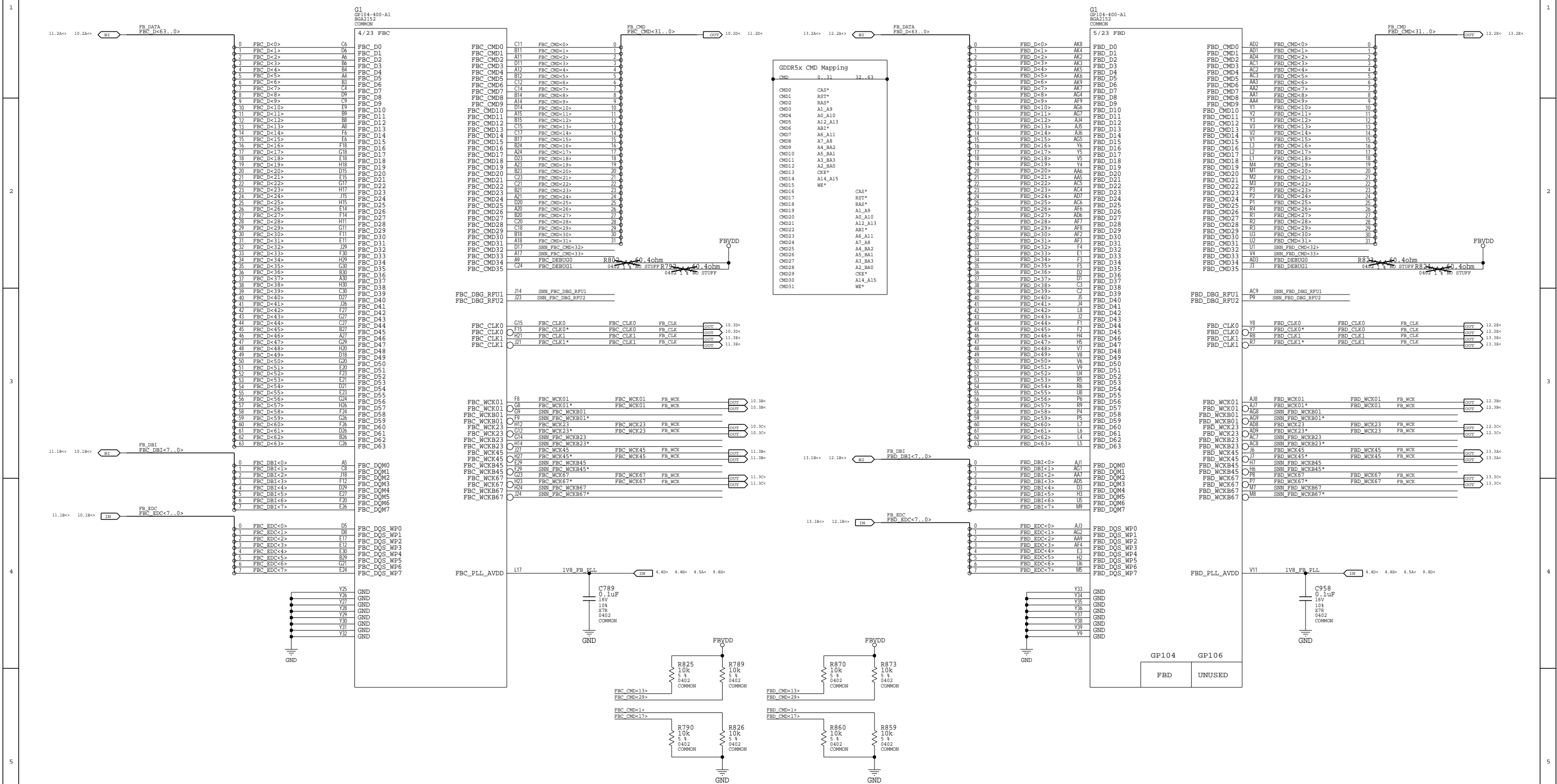
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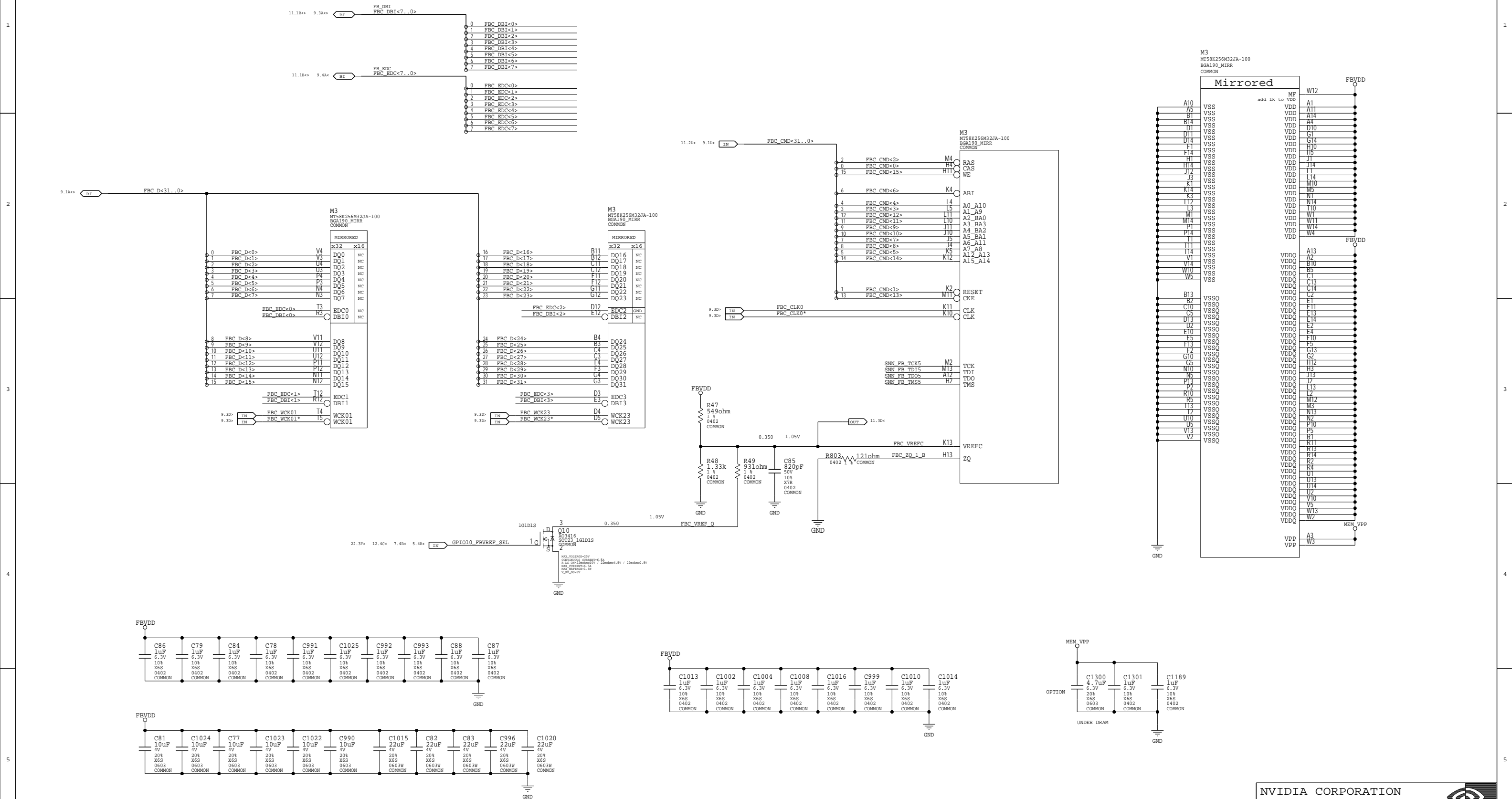
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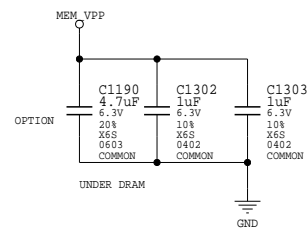
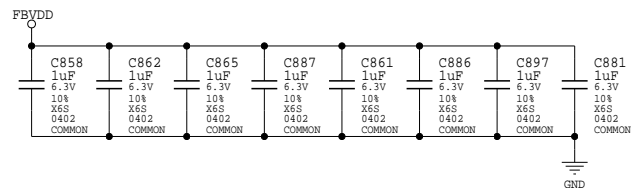
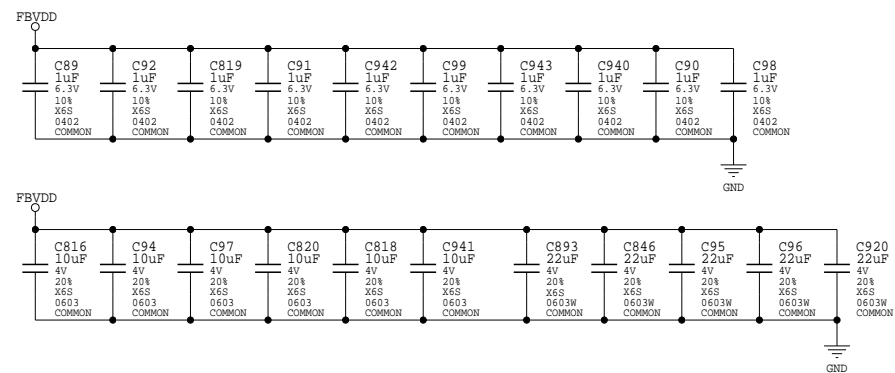
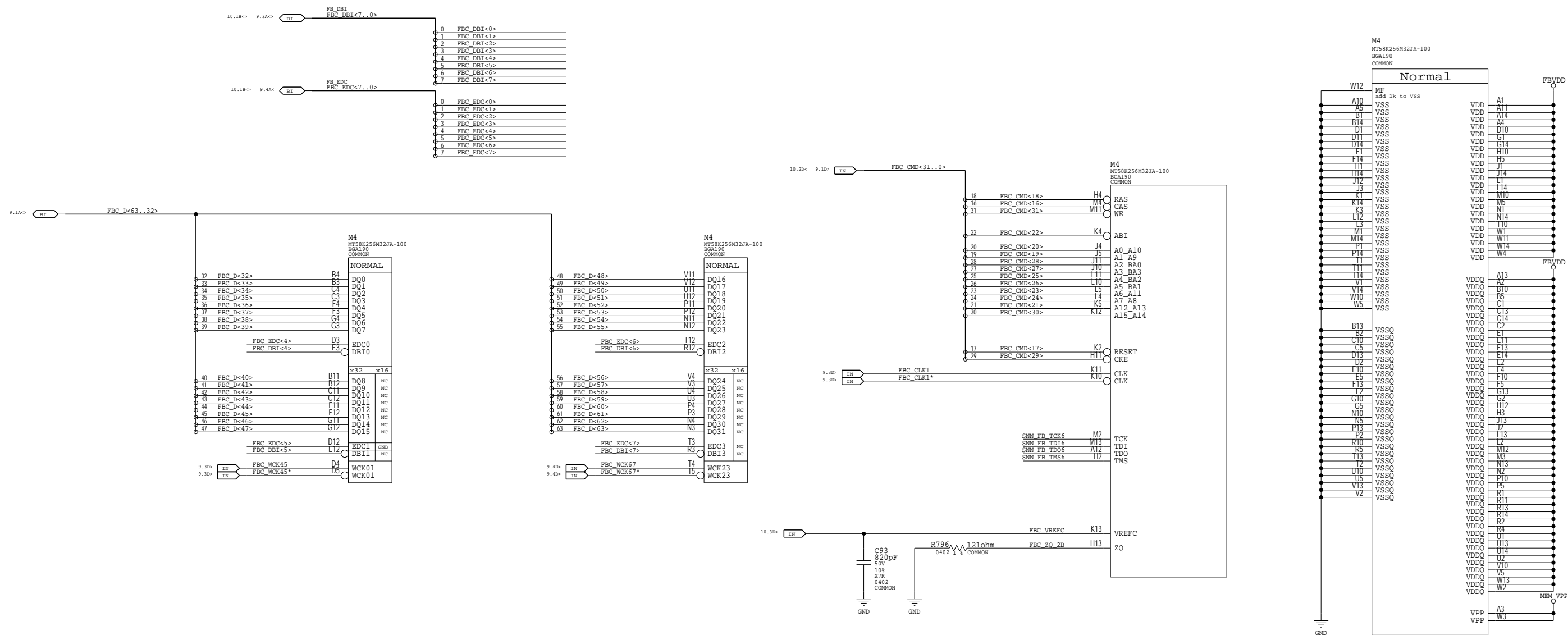


Page10: MEMORY: FBC Partition 31..0

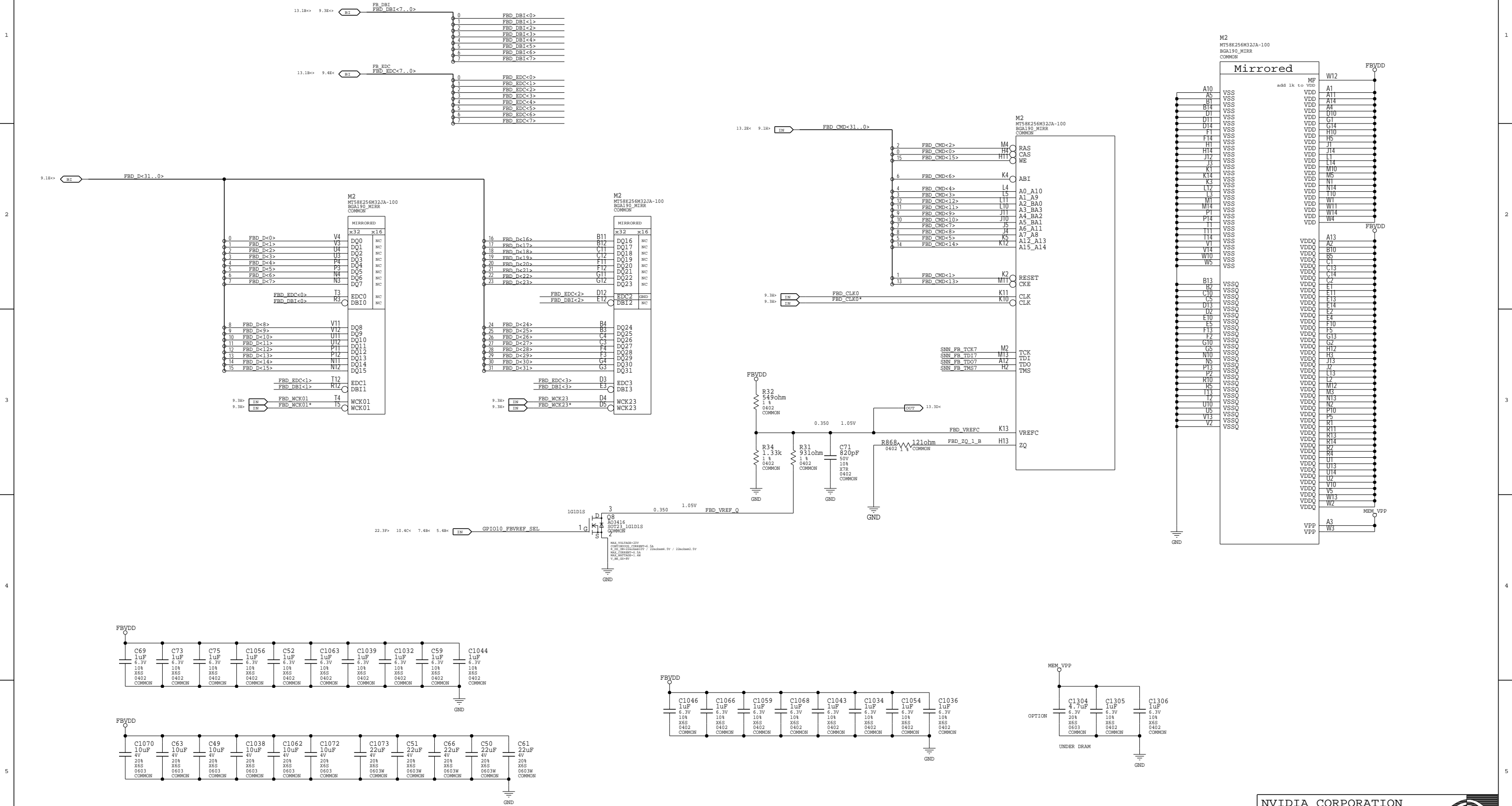


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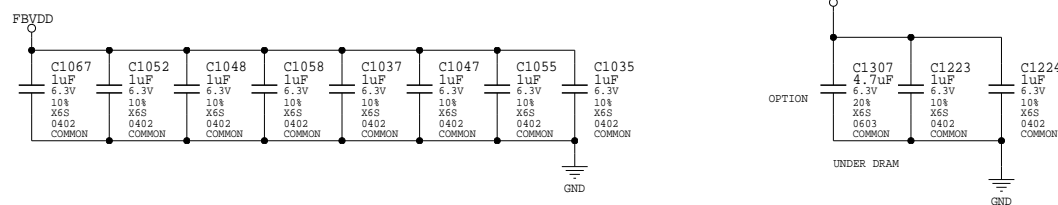
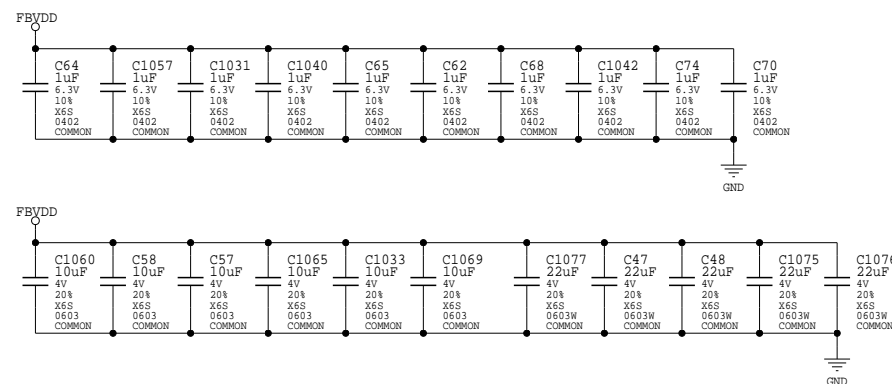
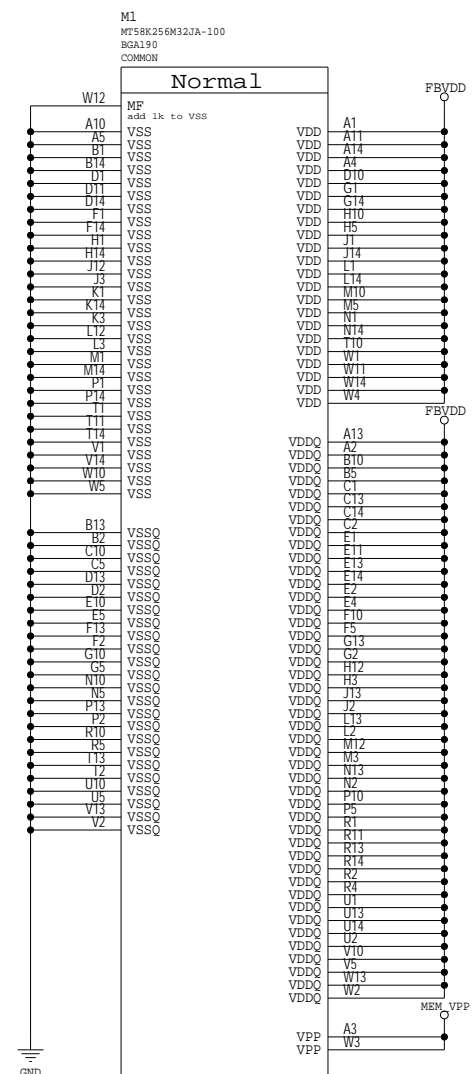
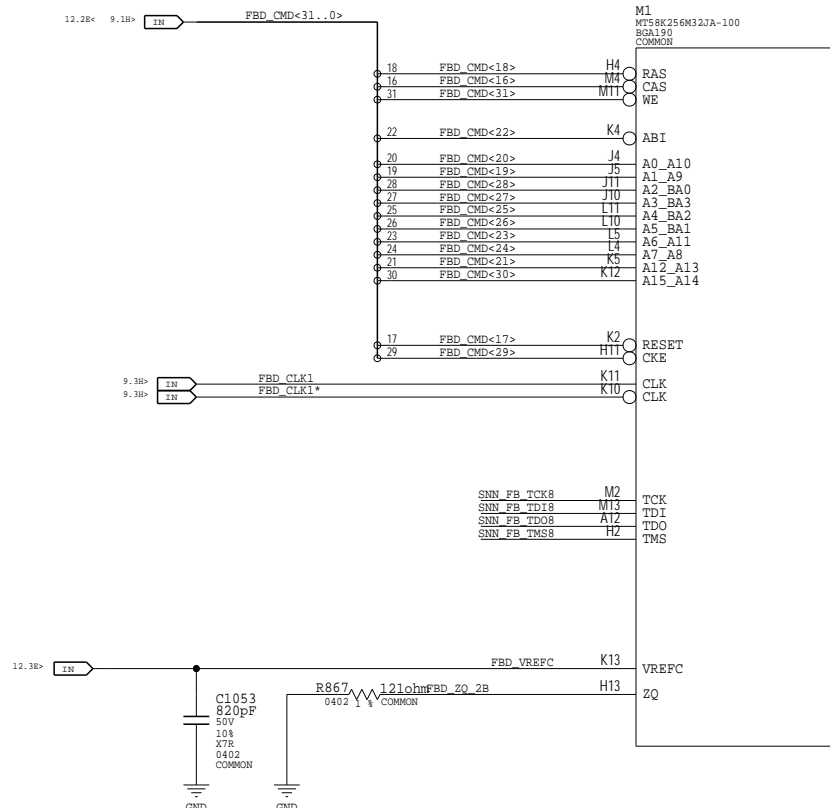
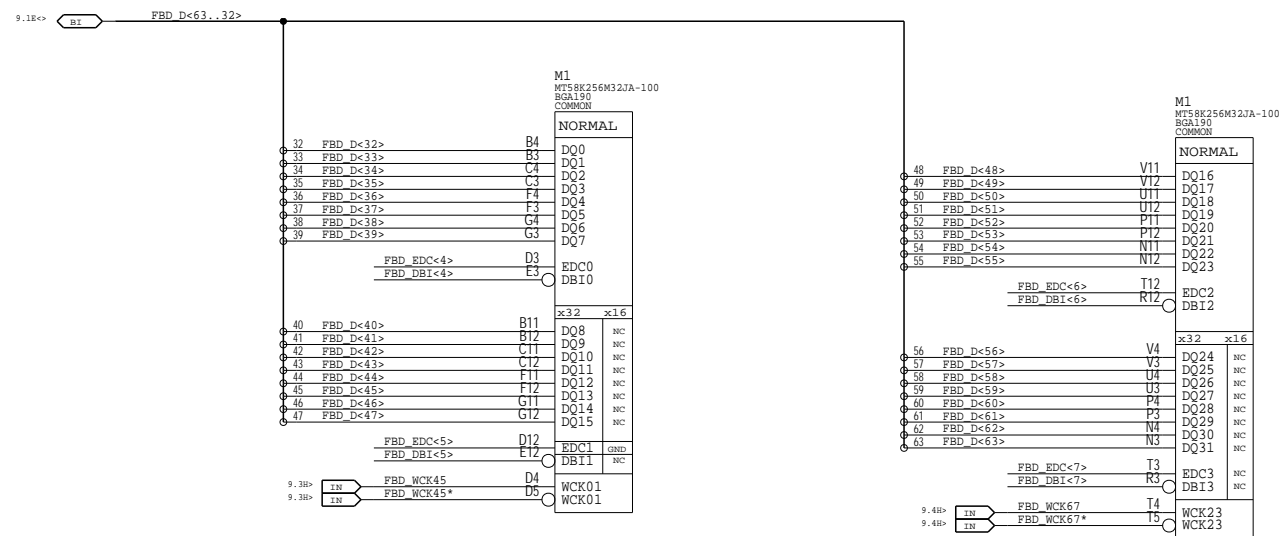
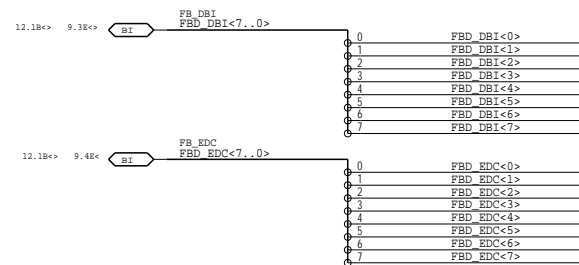
Page11: MEMORY: FBC Partition 63..32



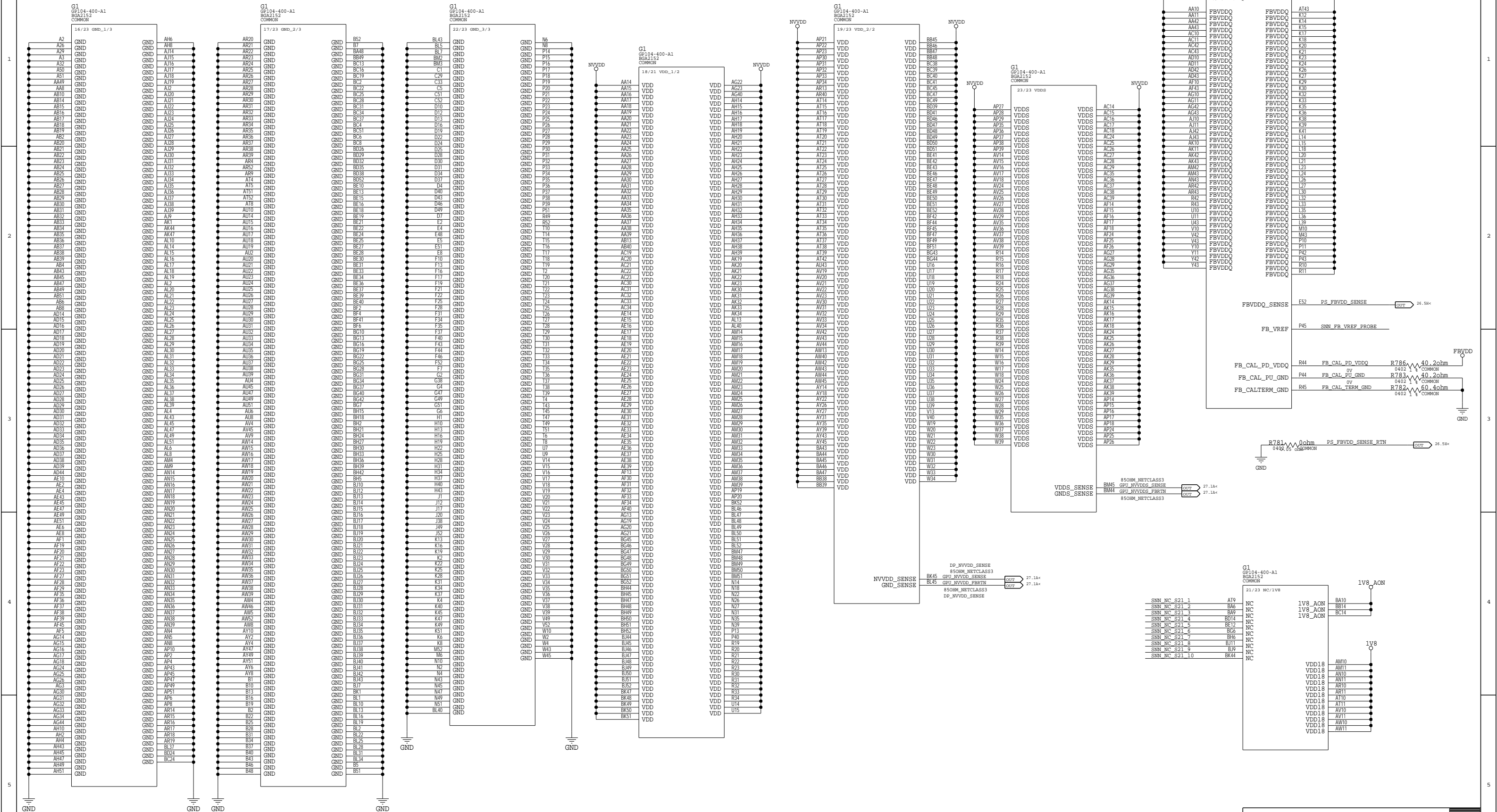
Page12: MEMORY: FBD Partition 31..0



Page13: MEMORY: FBD Partition 63..32

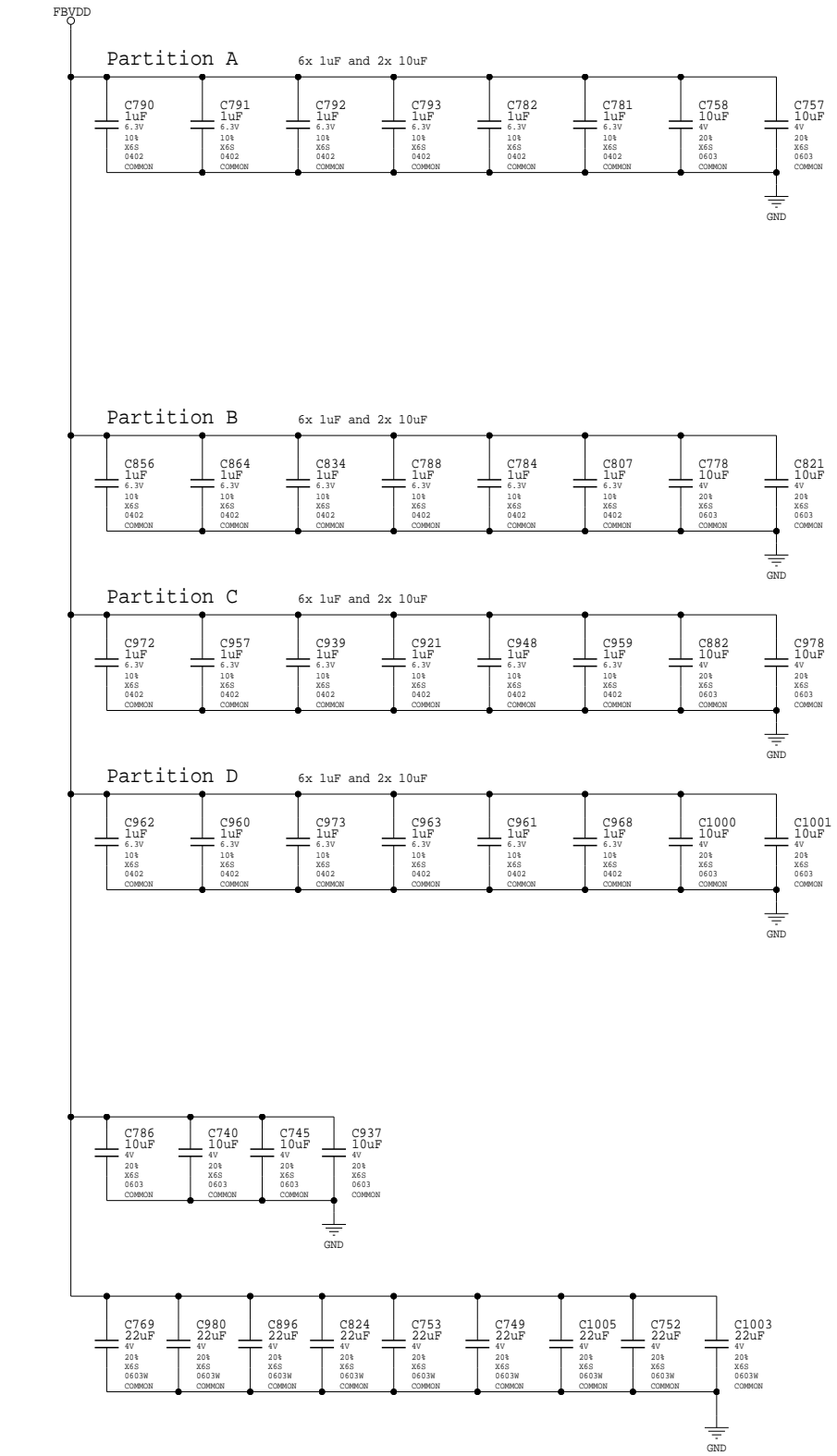


Page14: GPU PWR and GND

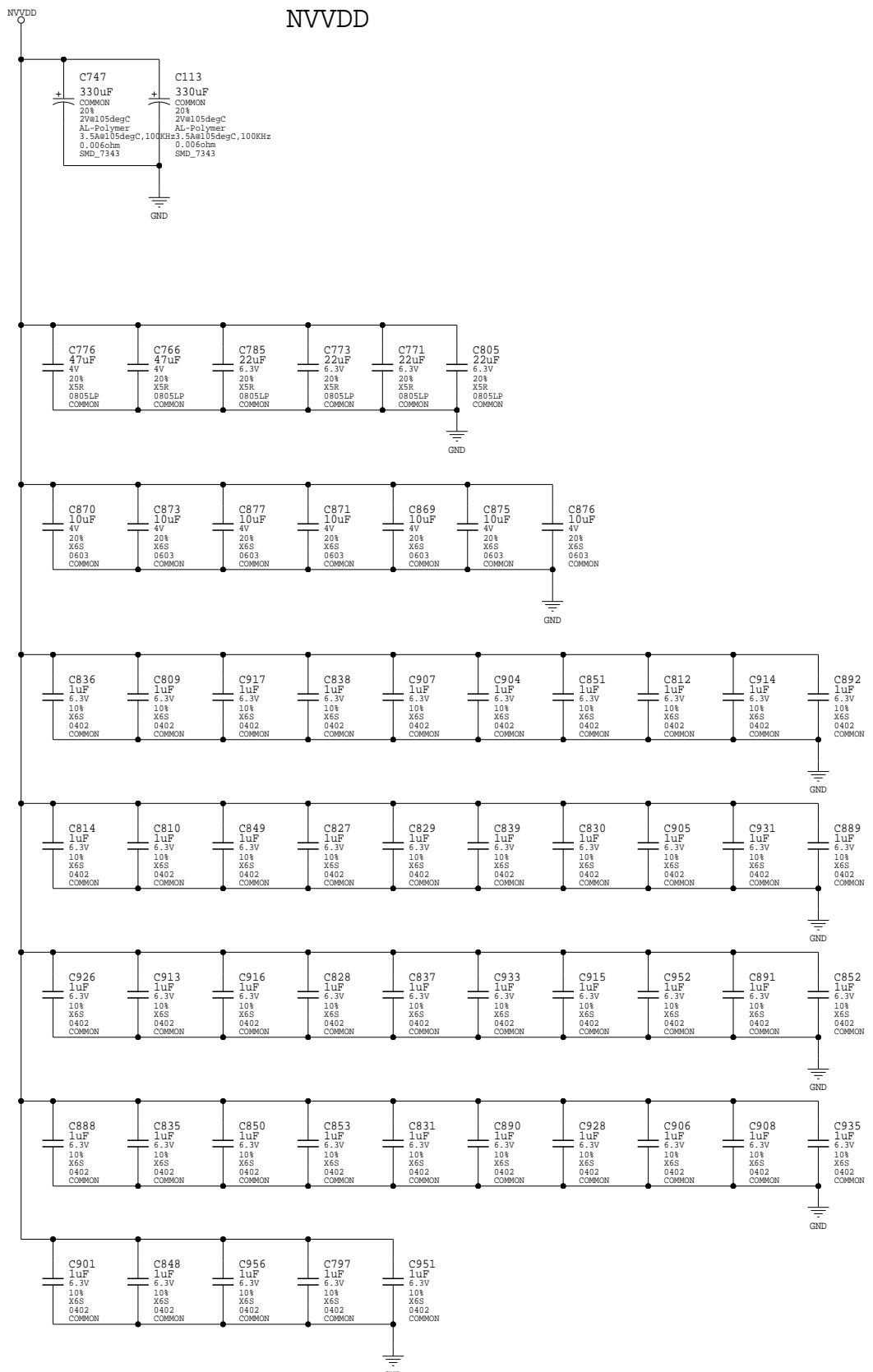


Page15: GPU Decoupling

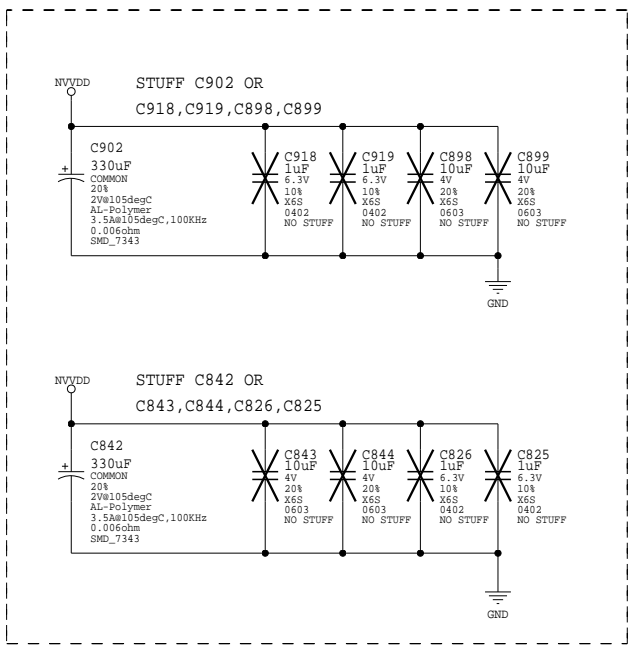
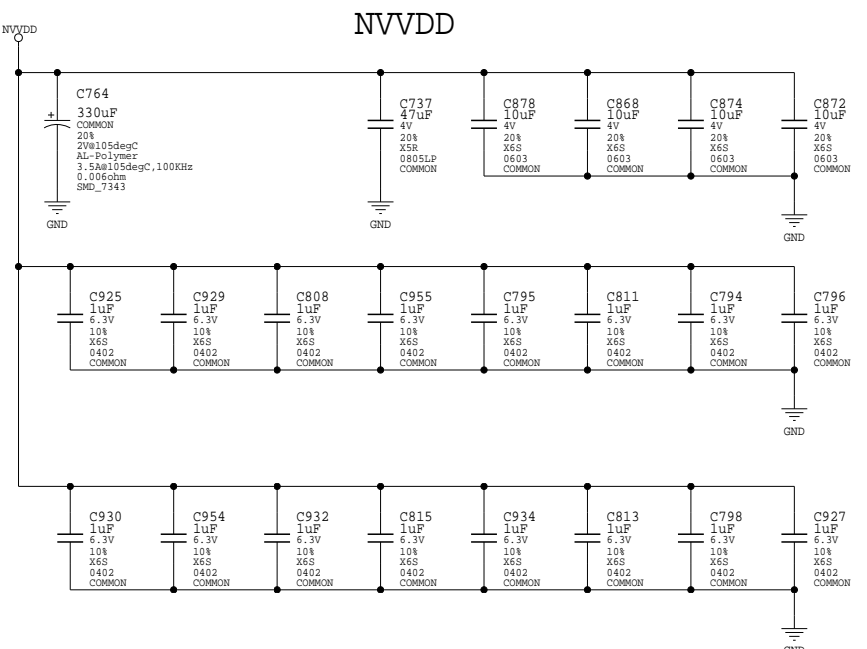
FBVDD



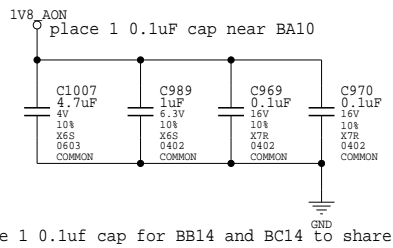
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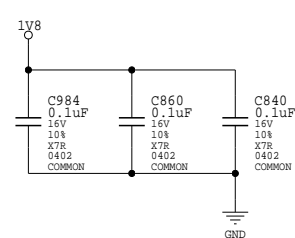
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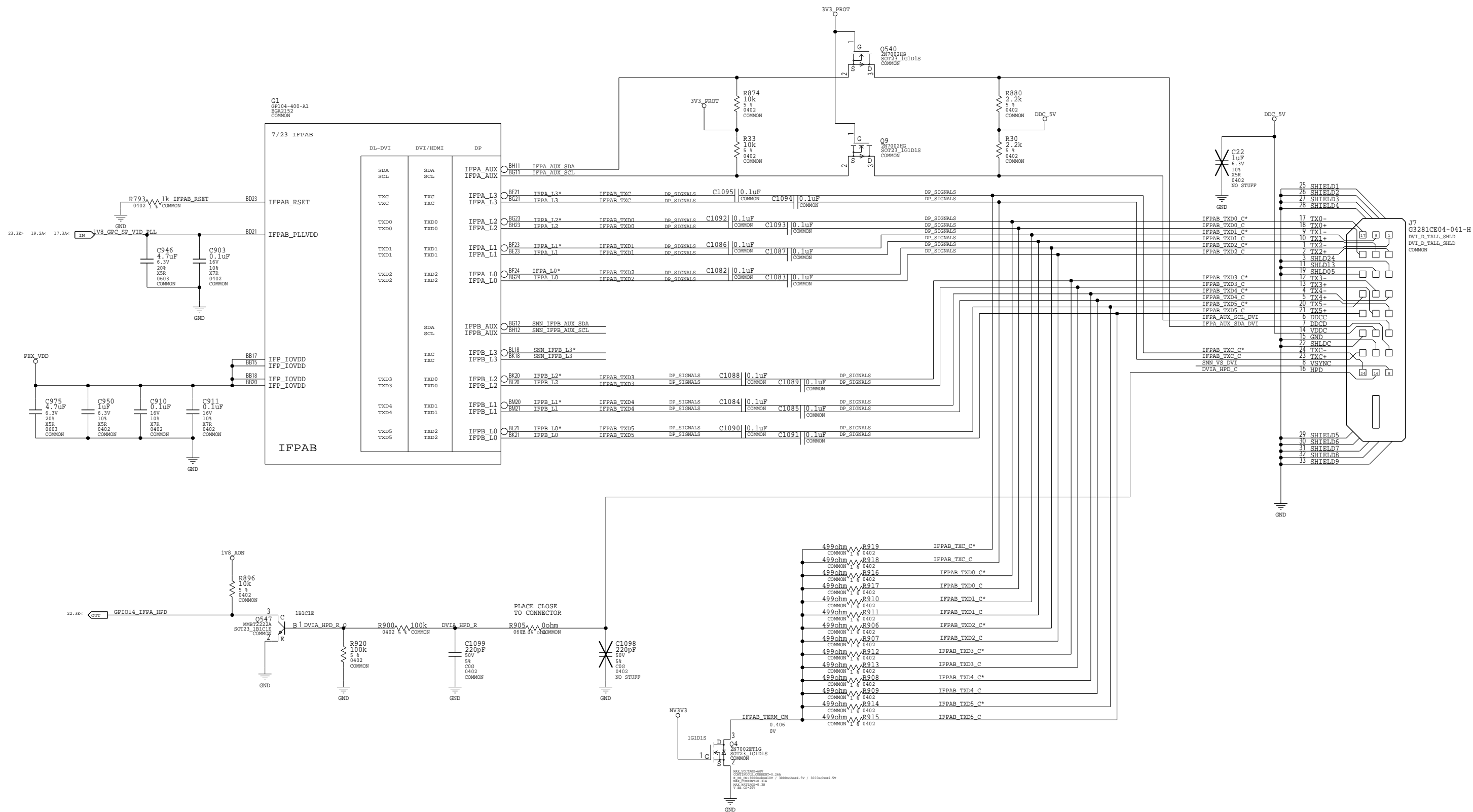
1V8_AON



VDD18



Page16: IFPAB DVI-D-DL



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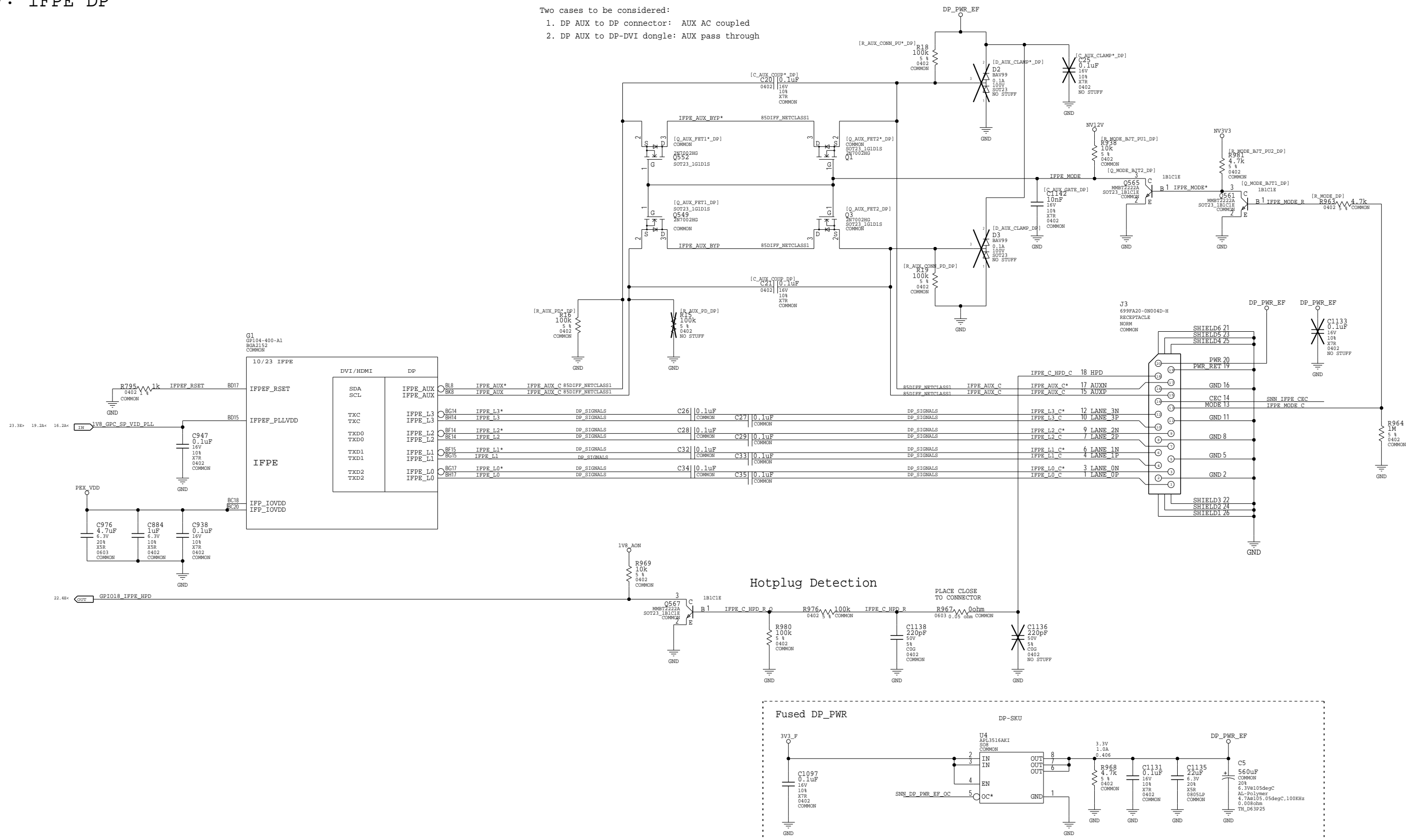
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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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PAGE DETAIL	IFPE DP

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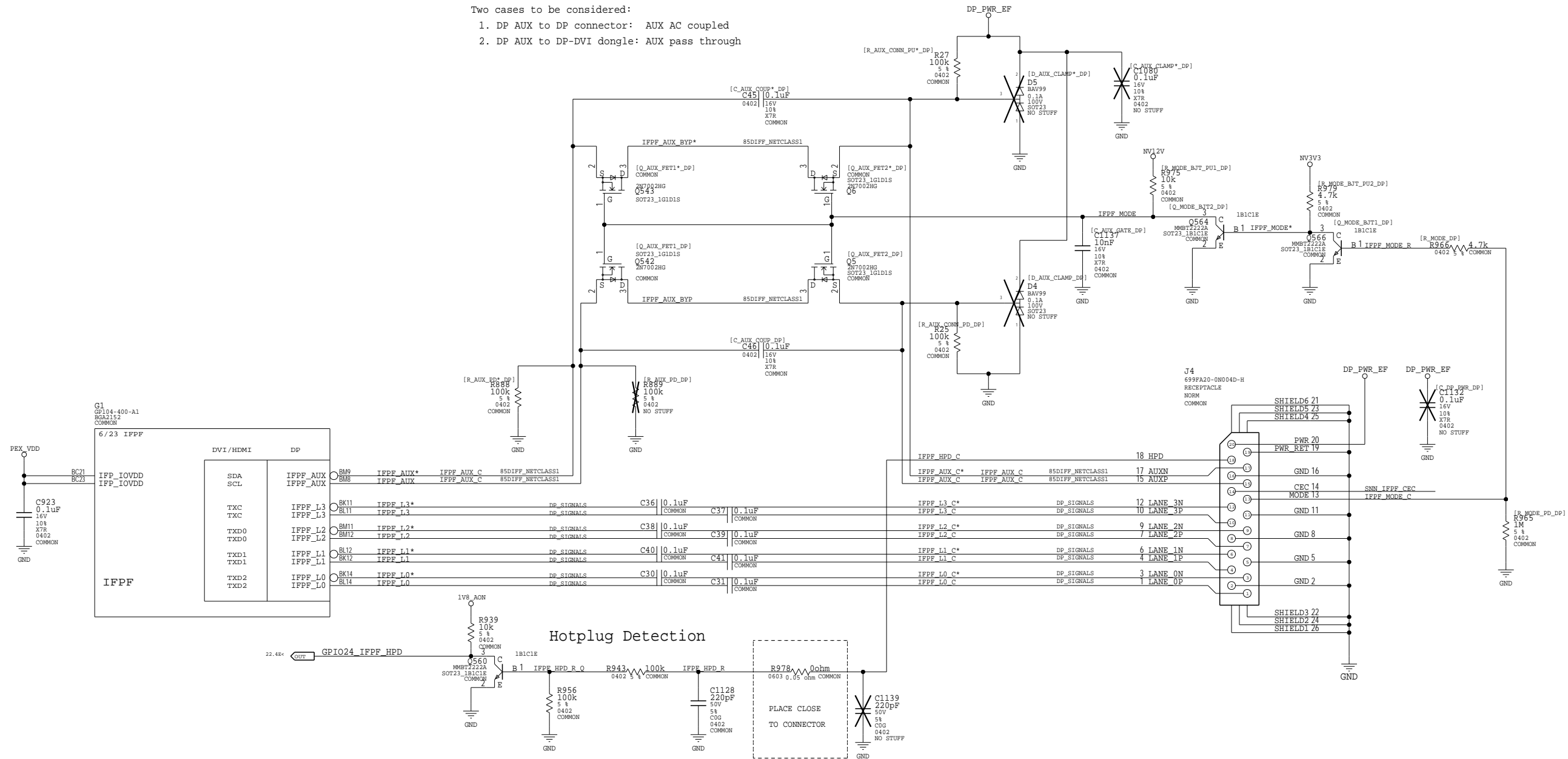
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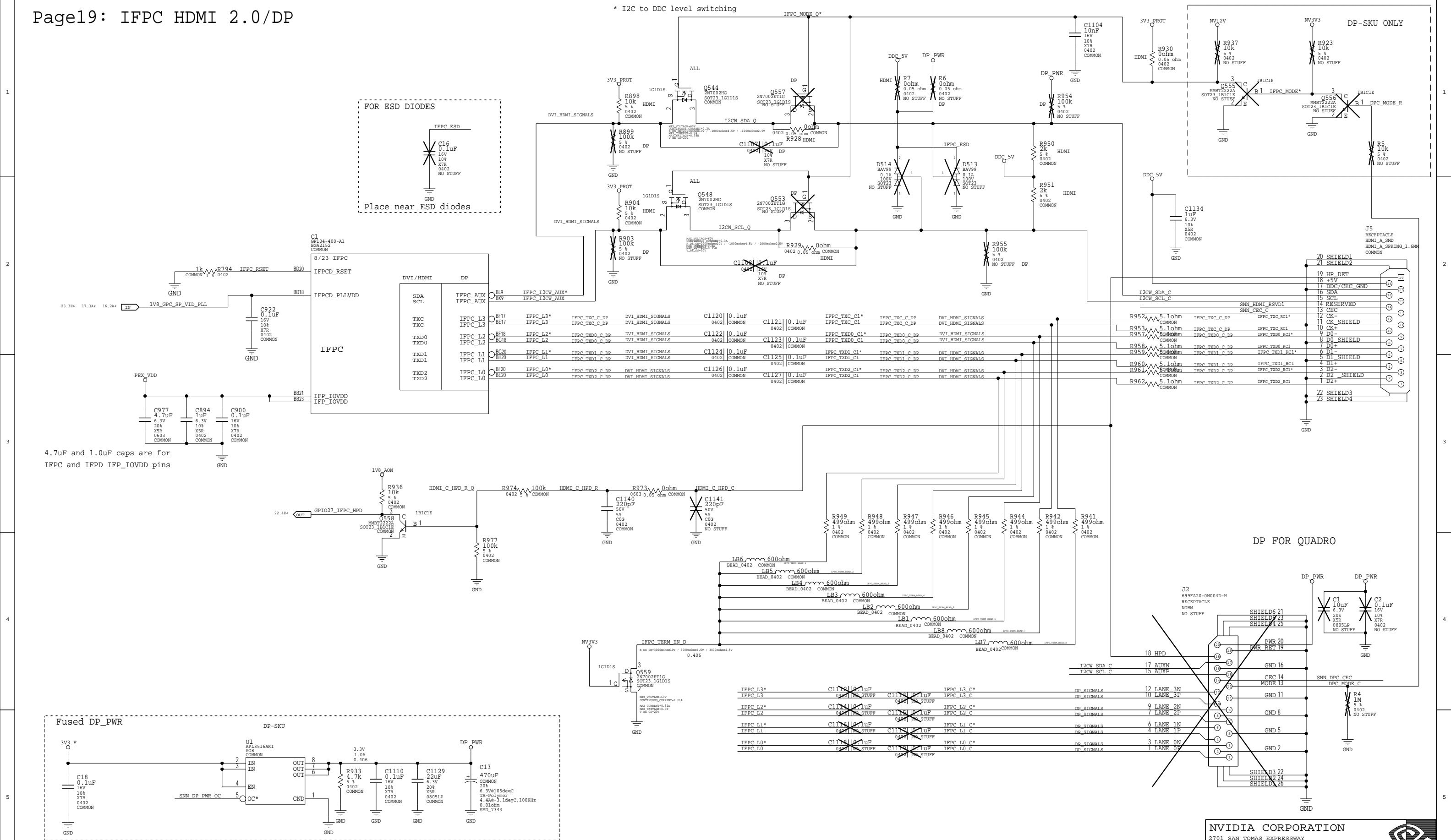
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Two cases to be considered:


1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through





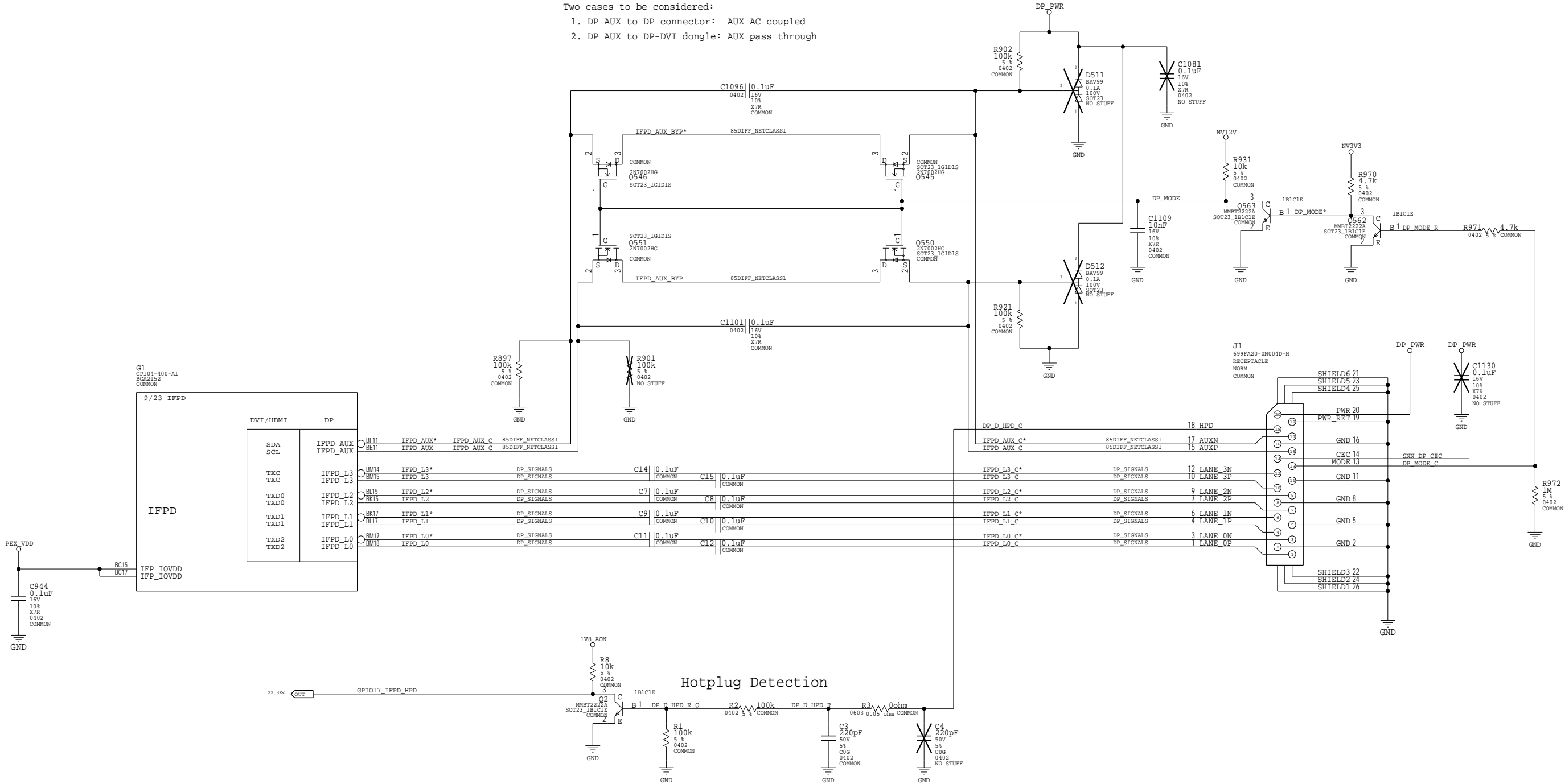
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PAGE DETAIL	IFPC HDMI 2.0/DP

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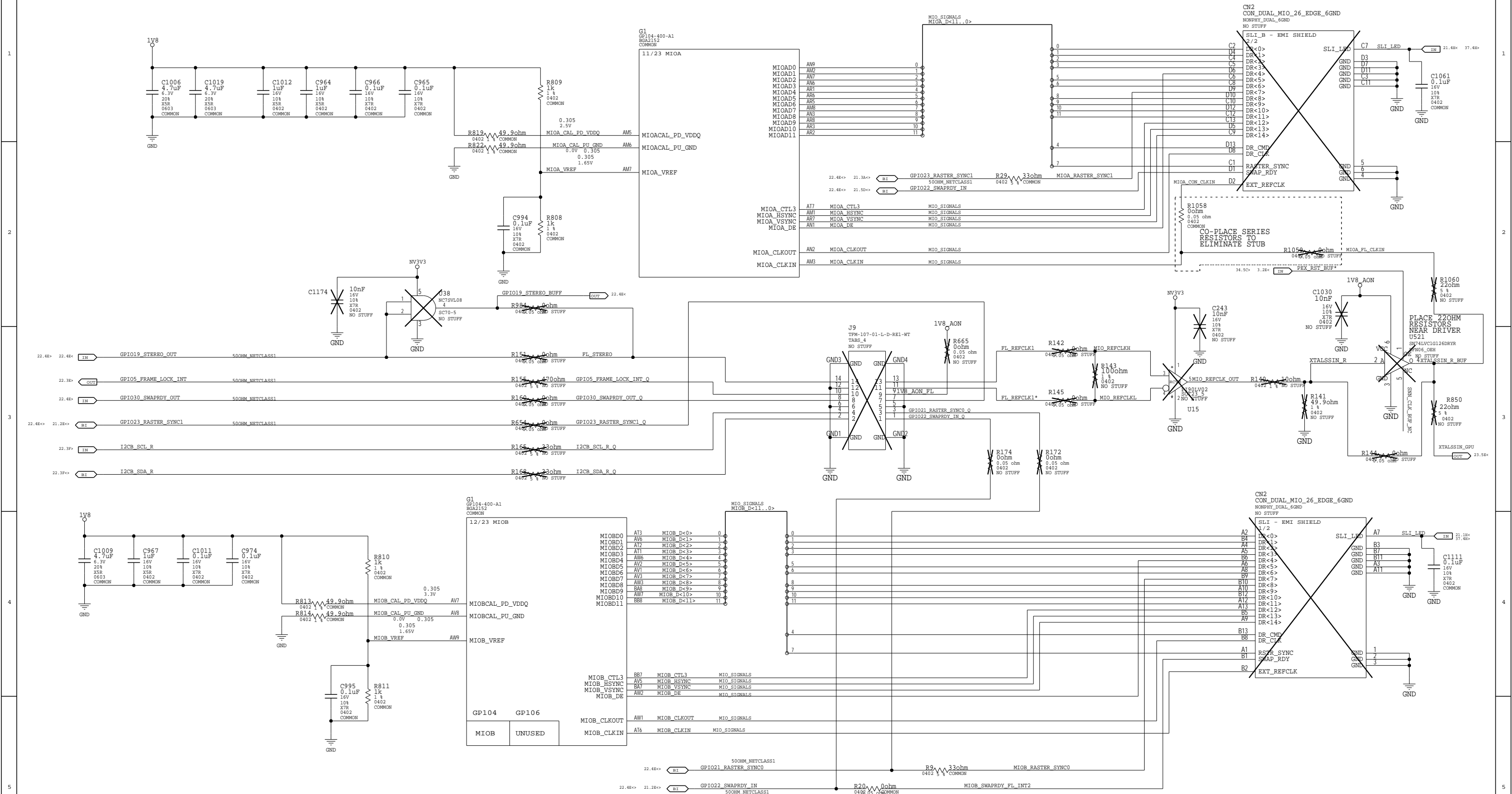
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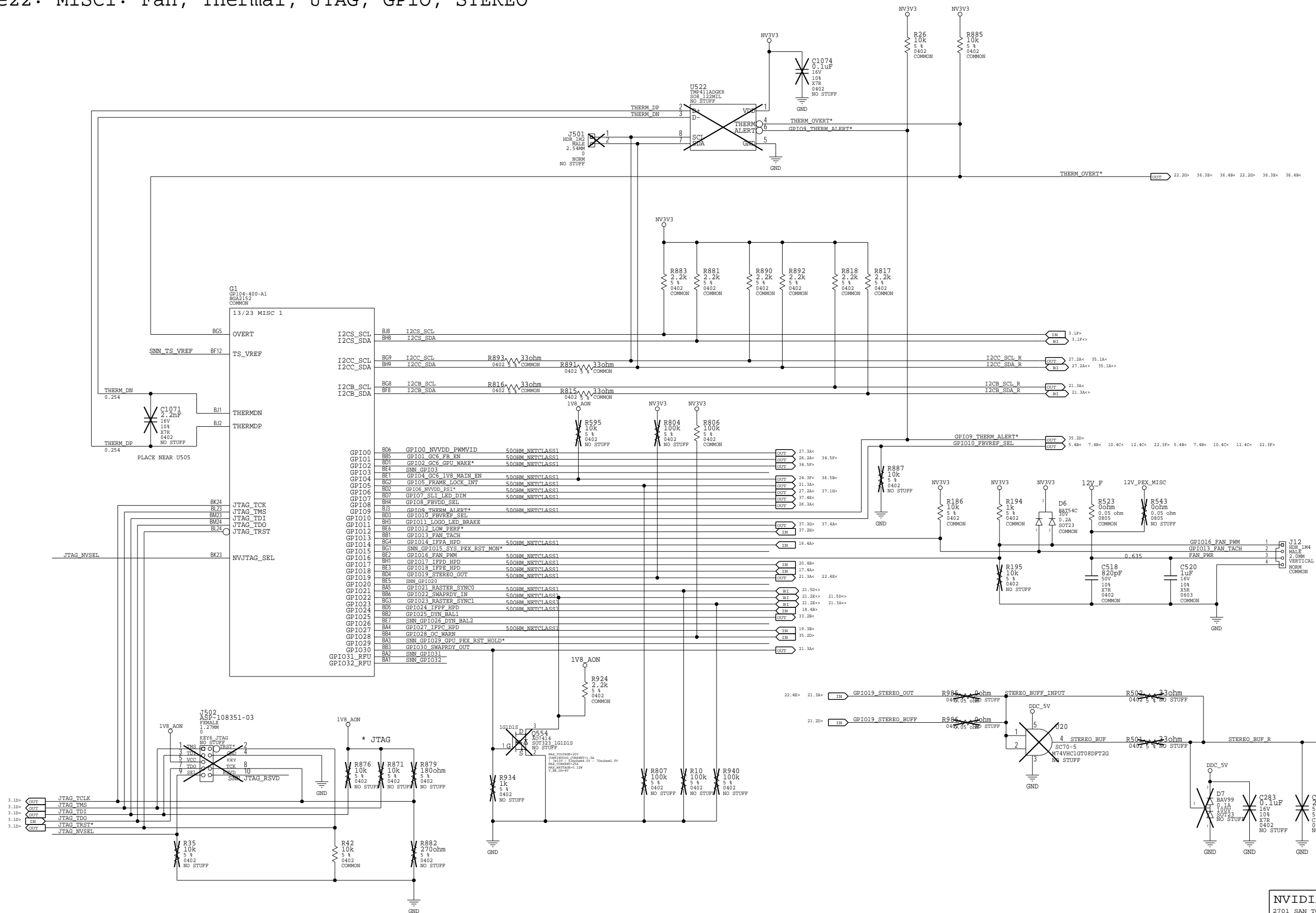



- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



Page21: MIOA/B Interface and FRAME LOCK





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Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		
L	L	L	00000		
L	H	L	00010		
L	H	H	00011		
H	H	L	00110		
H	H	H	00111		
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE	
L	L	L	1111	DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110		
L	H	L	1101		
L	H	H	1100		
H	L	L	1011		
H	L	H	1010		
H	H	L	1001		
H	H	H	1000		
L	L	M	0111		
L	M	L	0110		
L	M	H	0101		
L	H	M	0100		
H	L	M	0011		
H	M	L	0010		
H	M	H	0001		
H	H	M	0000		

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

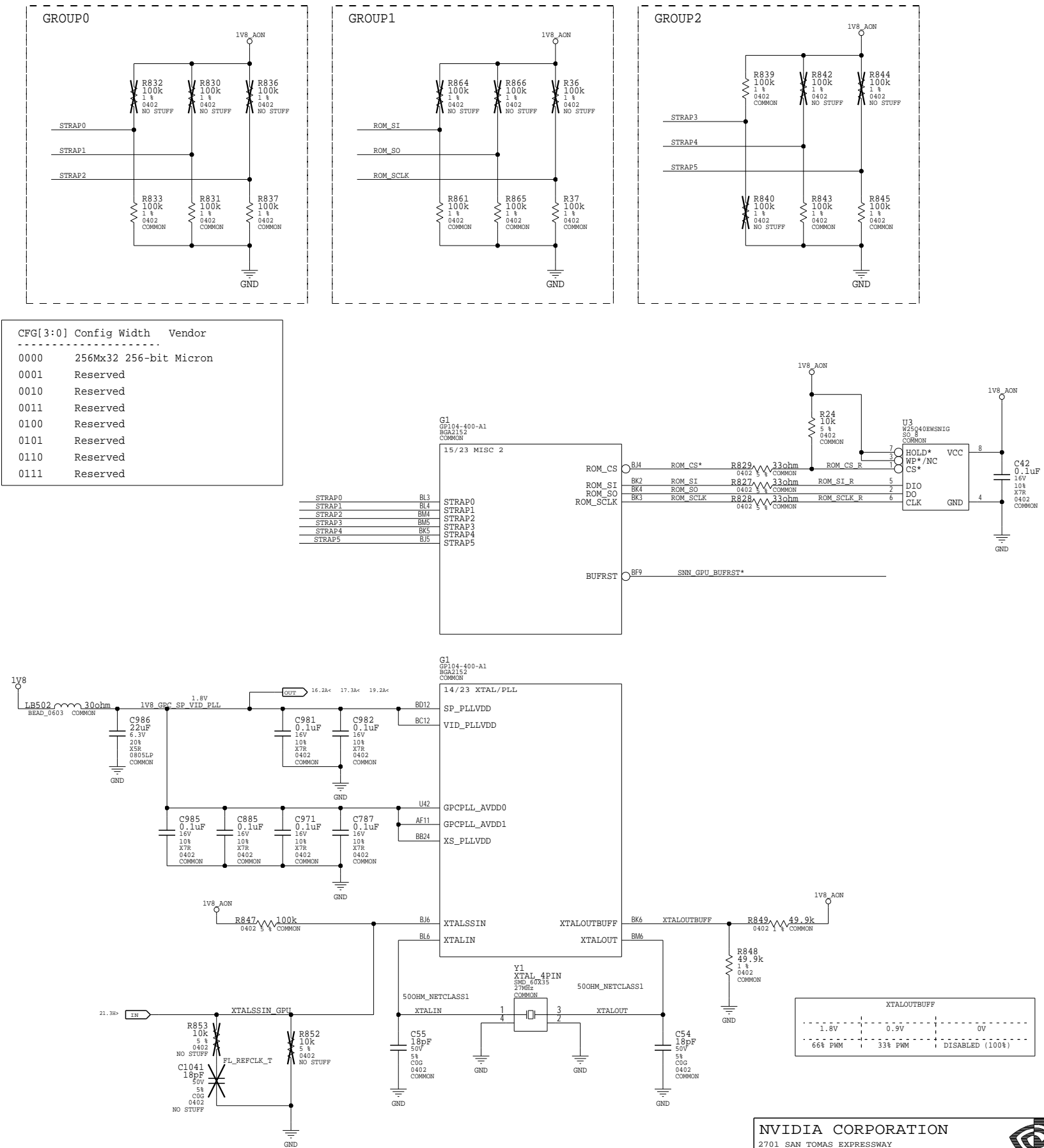
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

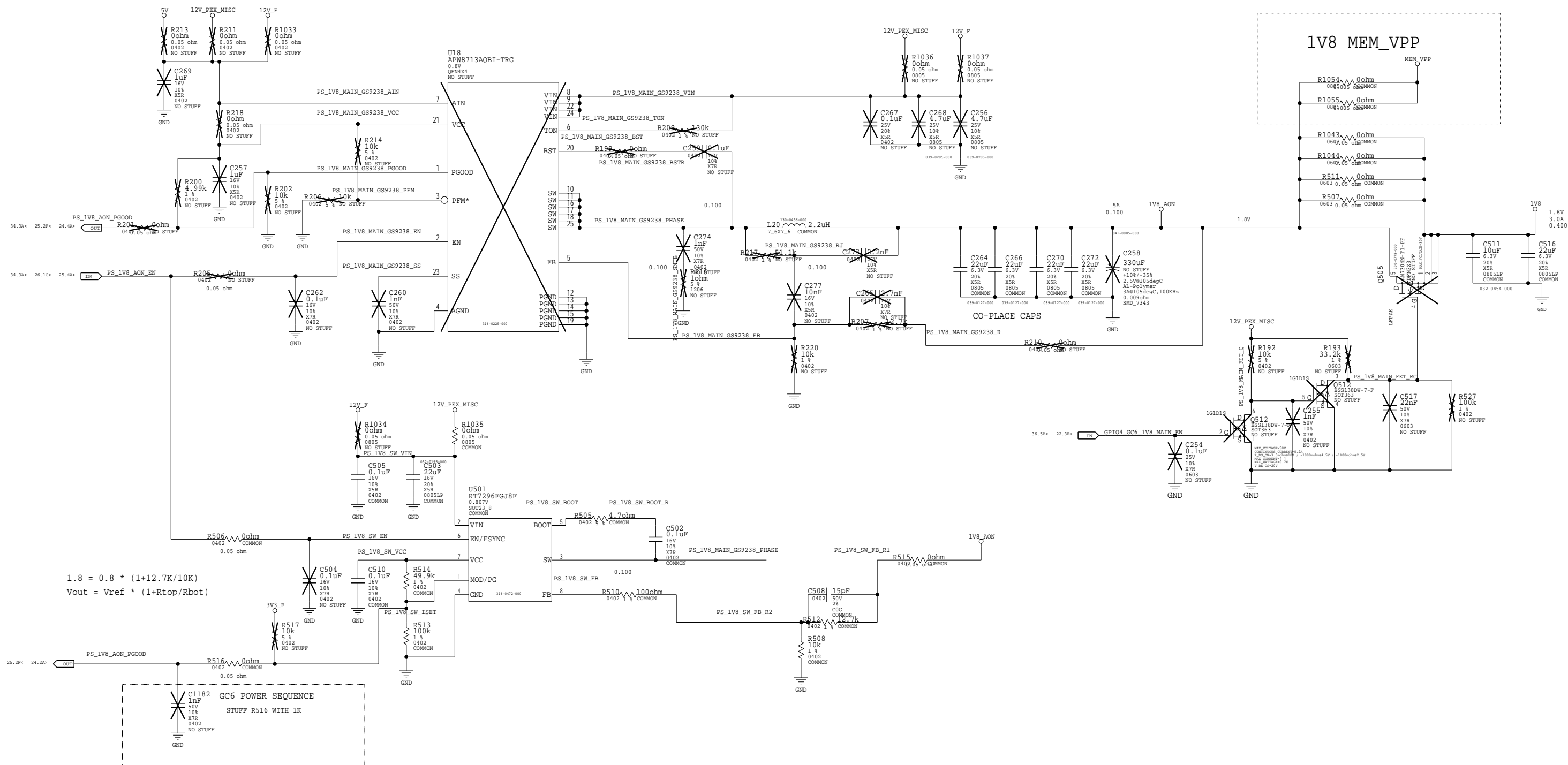
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





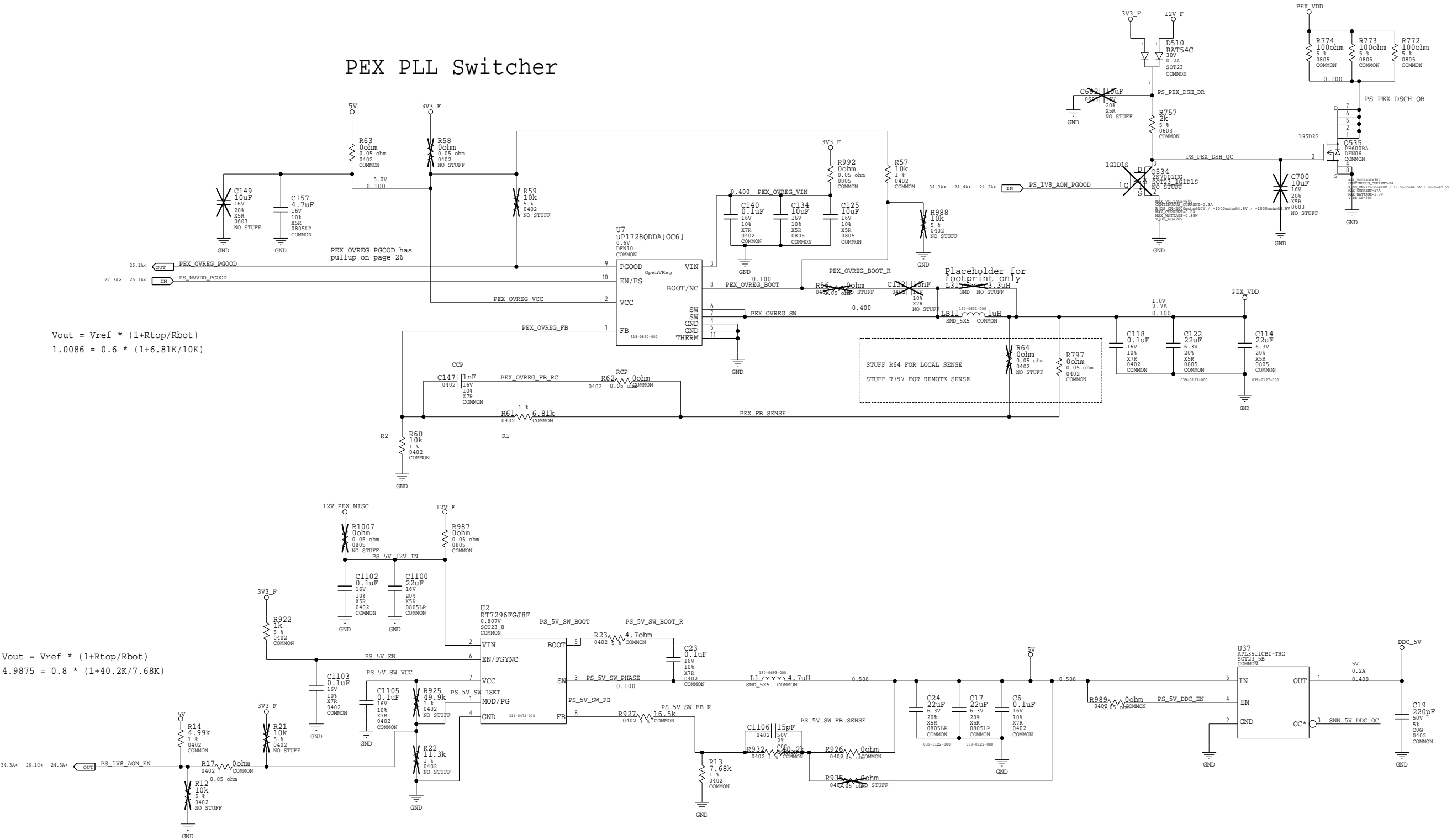
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PEX PLL Switcher

$$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$$
$$1.0086 = 0.6 * (1 + 6.81K/10K)$$

$$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$$
$$4.9875 = 0.8 * (1 + 40.2K/7.68K)$$



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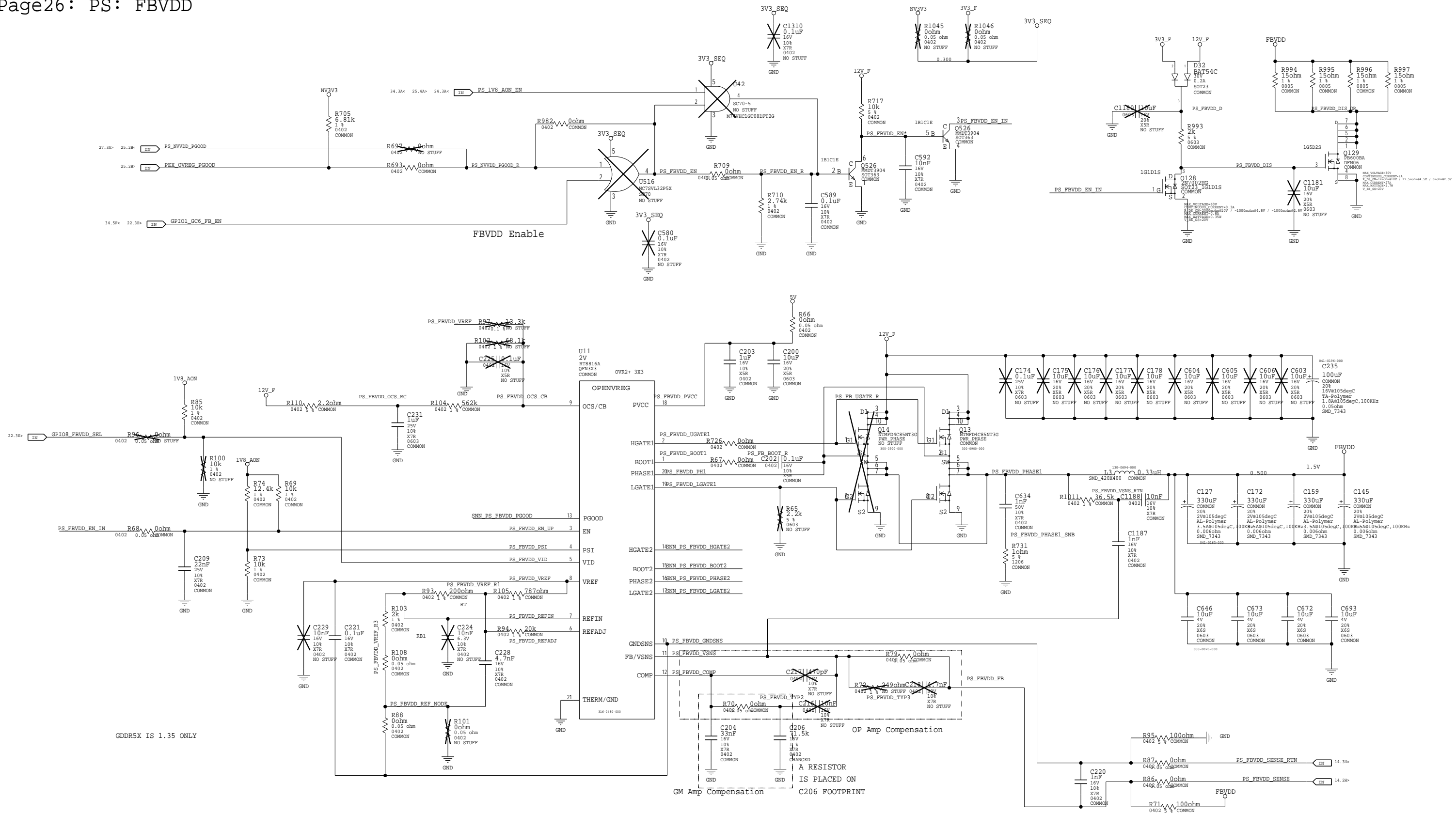
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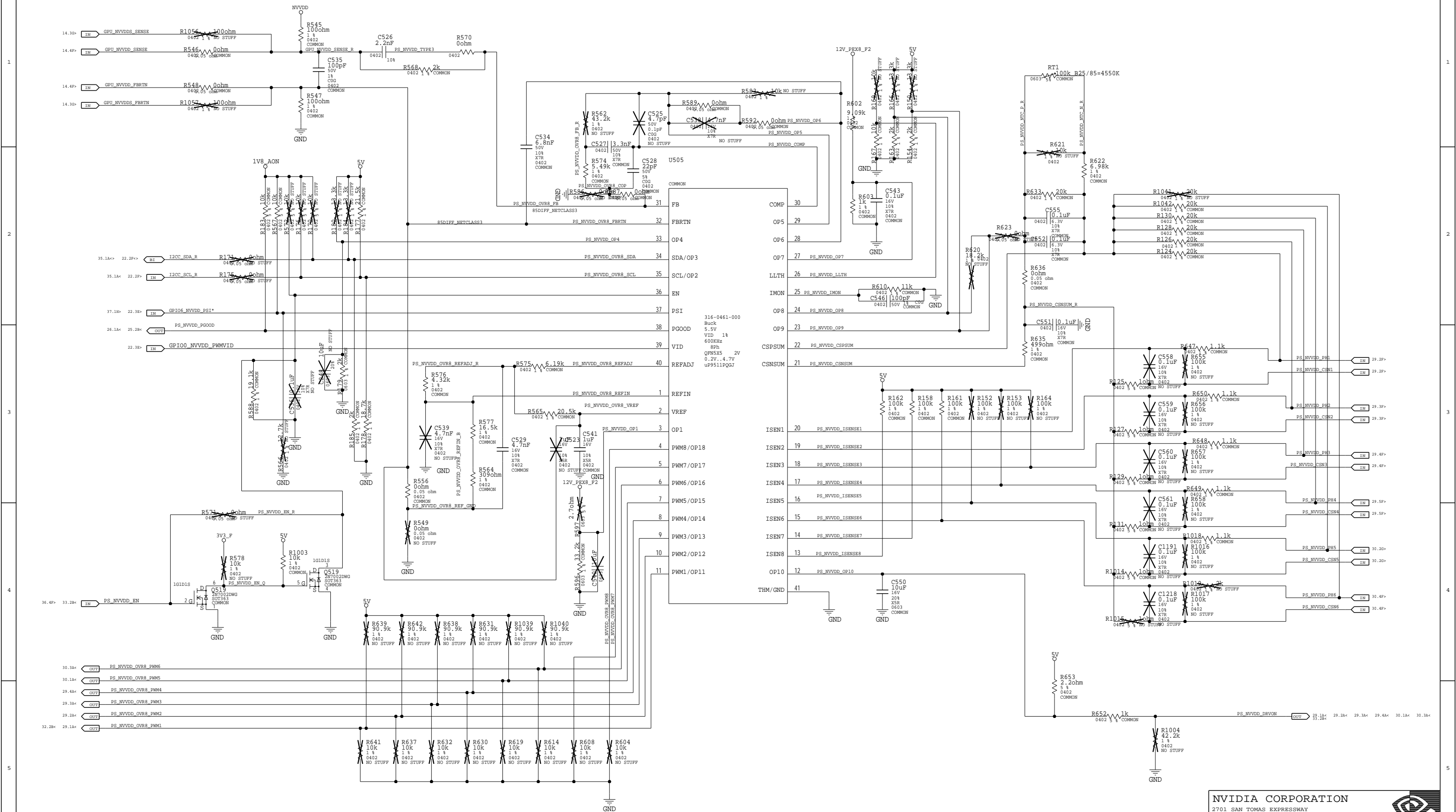
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Page27: PS: NVVDD_OVR8



ASSEMBLY	SKU0000 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD_OVR8

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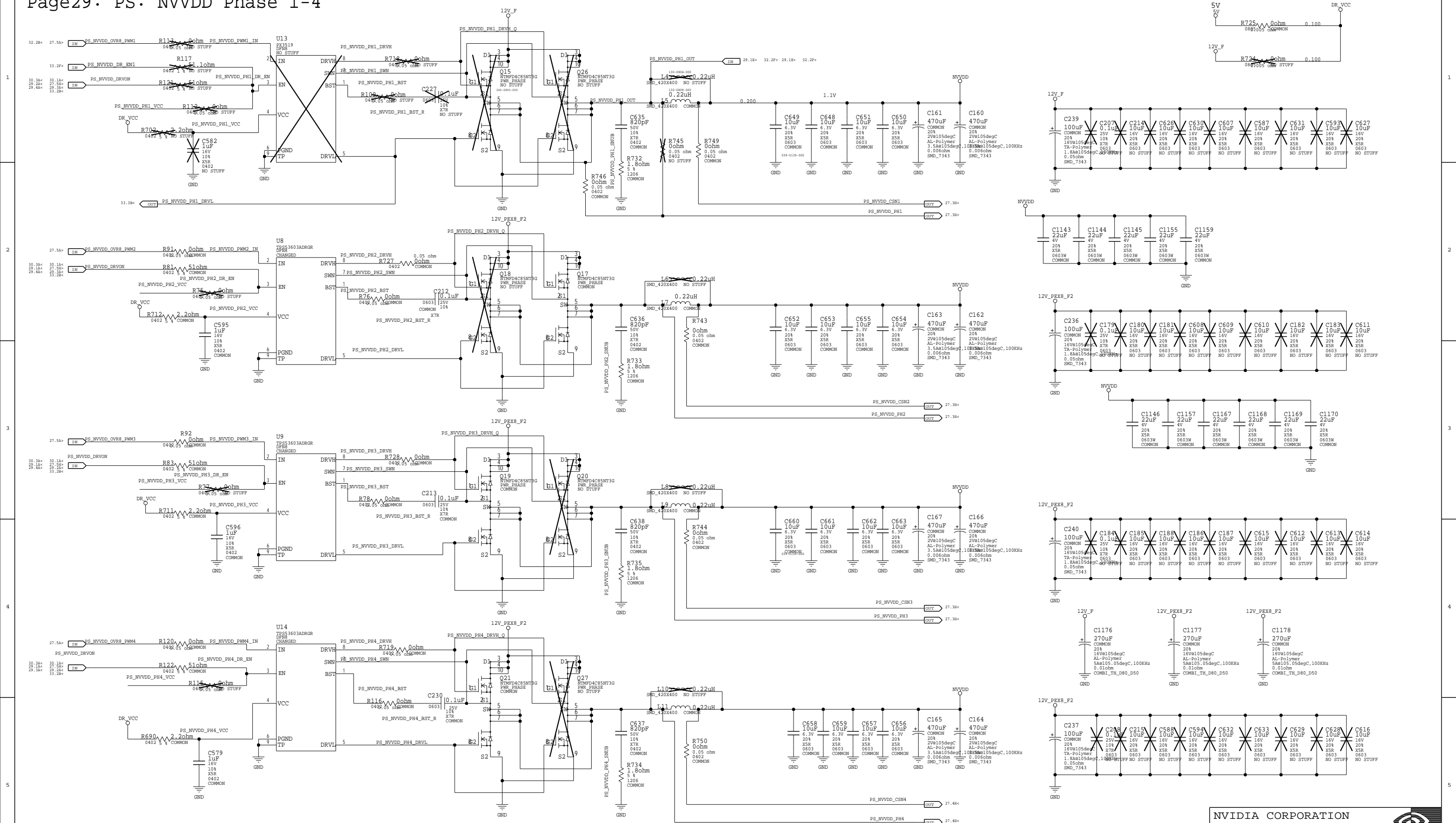
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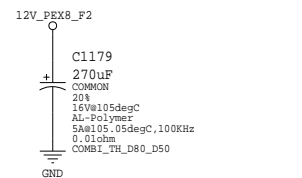
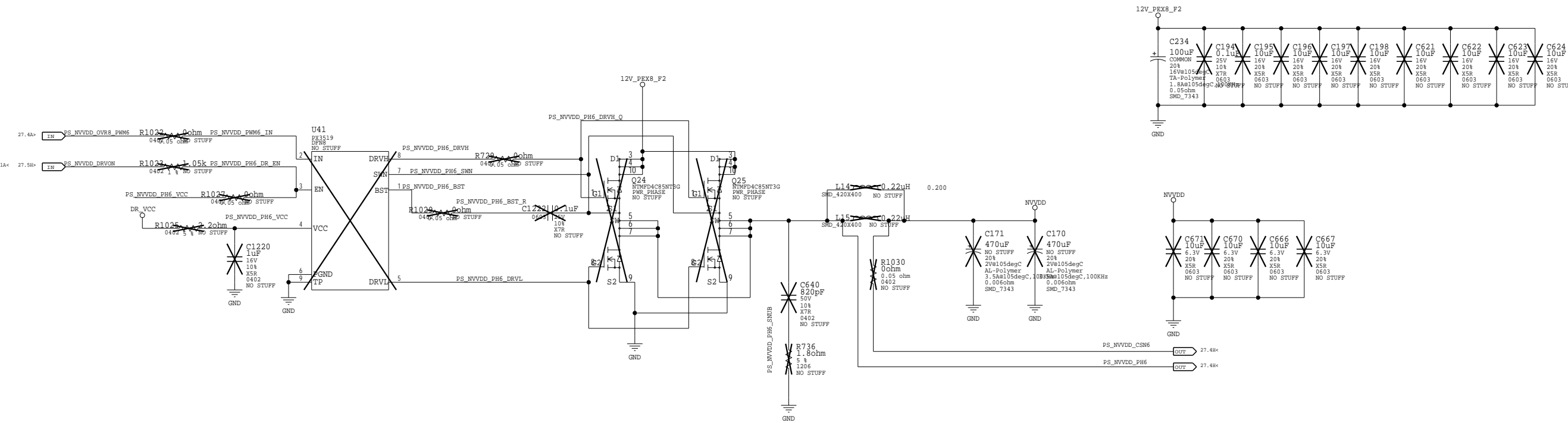
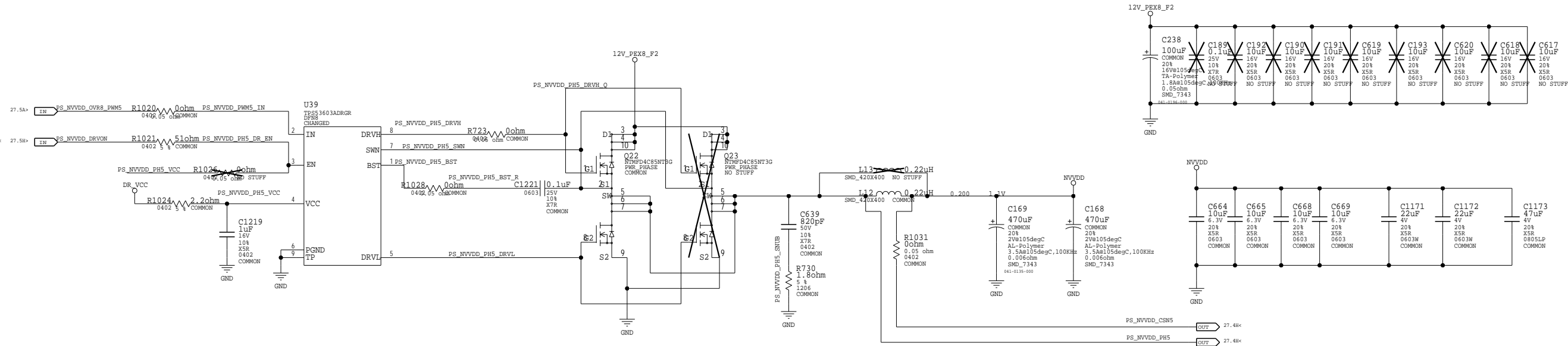
PAGE	27 OF 38
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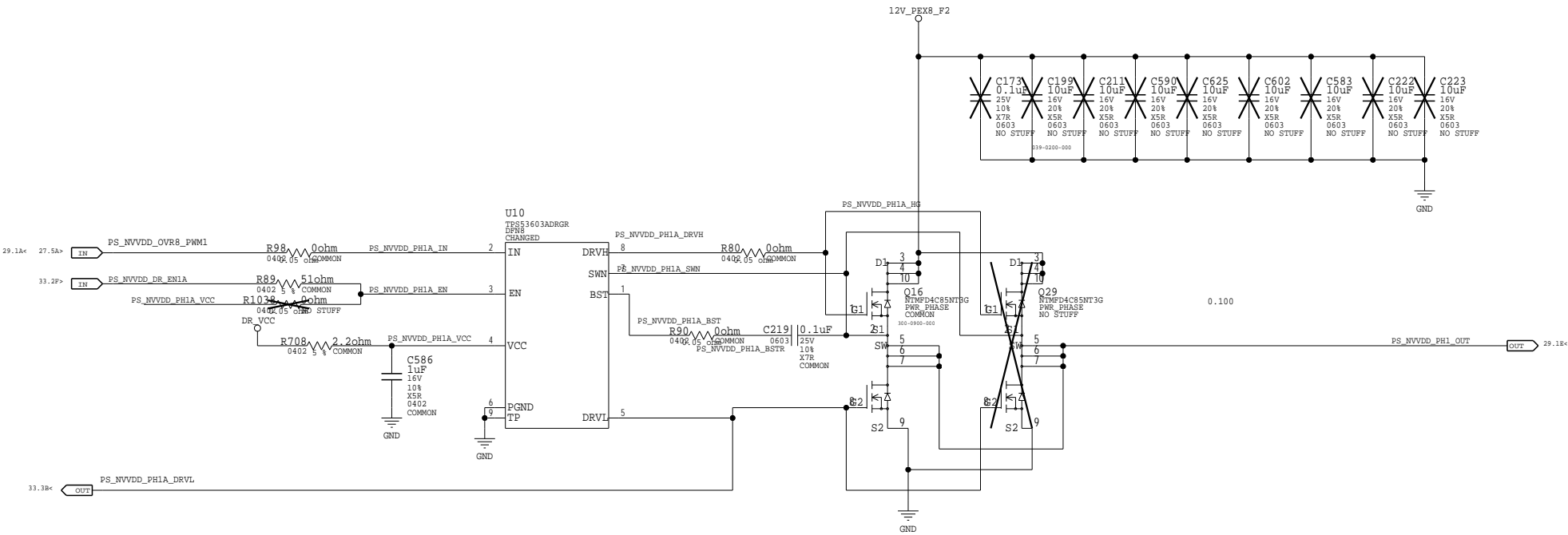


Page29: PS: NVVDD Phase 1-4





Page32: PS: Dynamic Power Balance Phases



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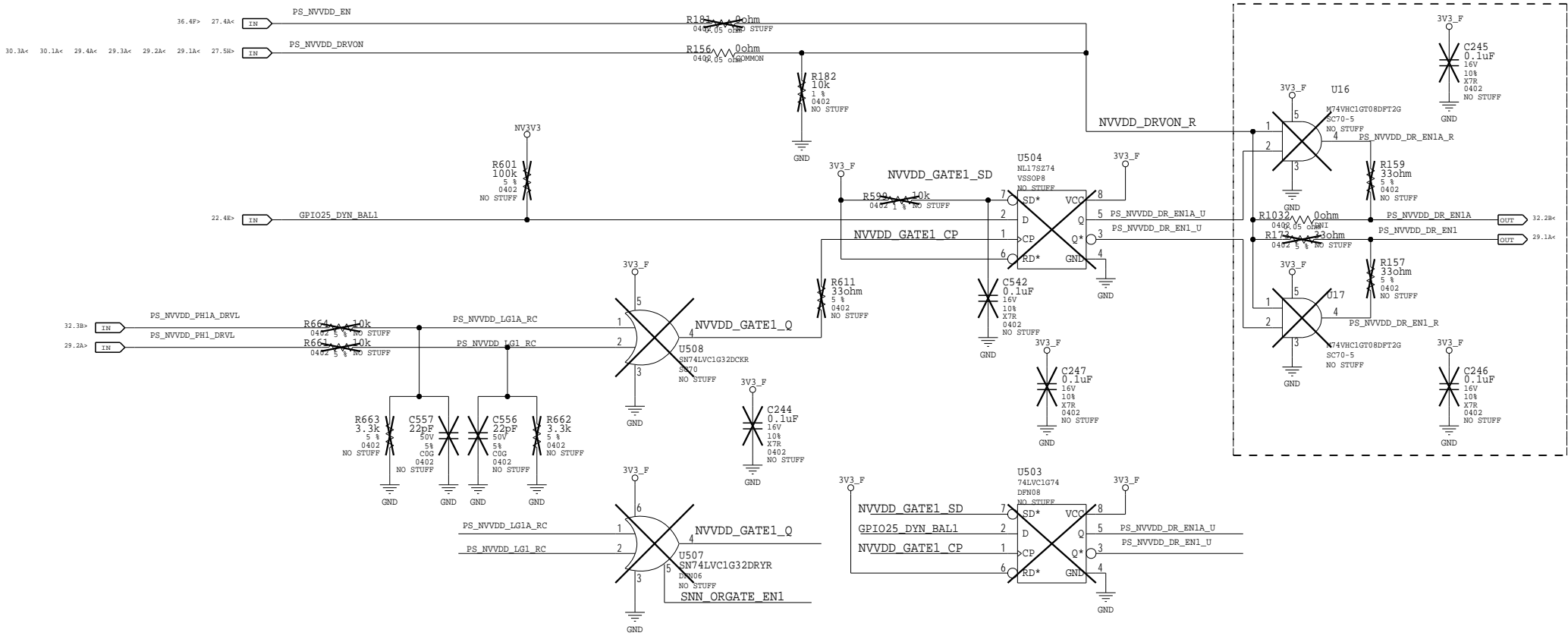
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Page33: PS: Dynamic Power Balance Logic



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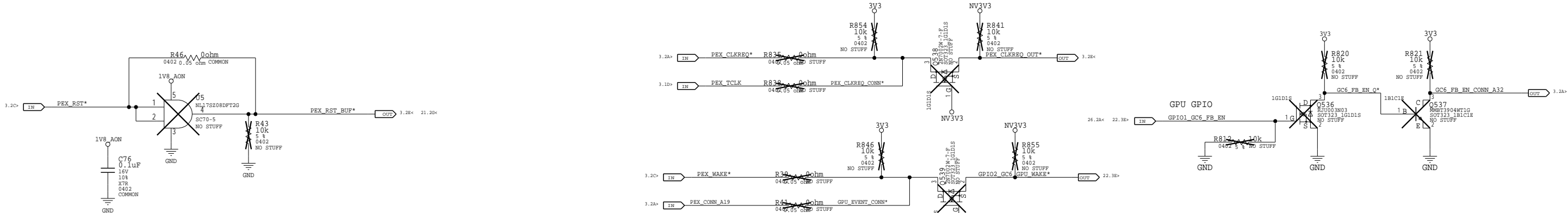
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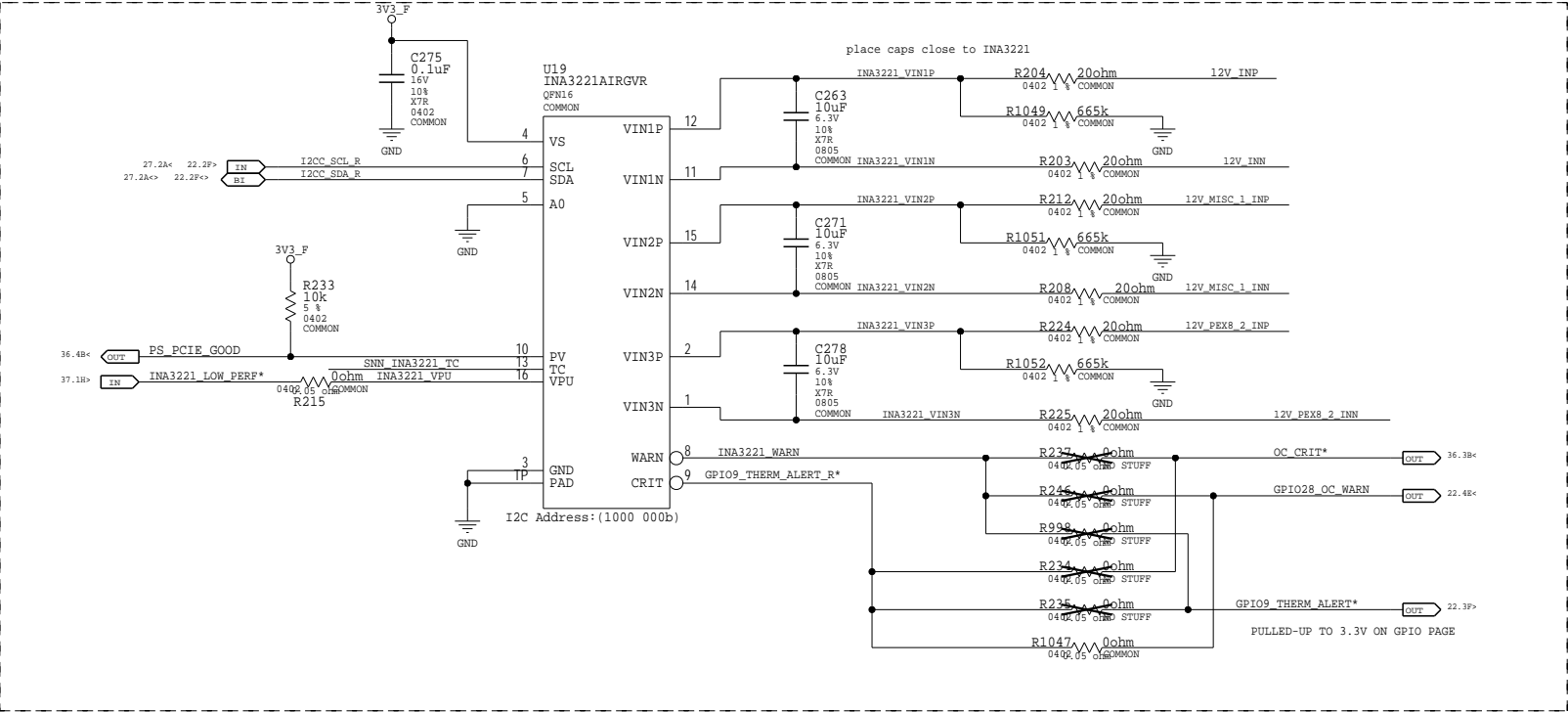
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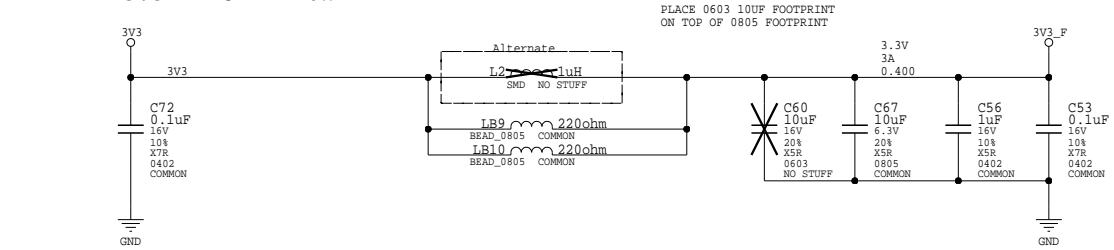
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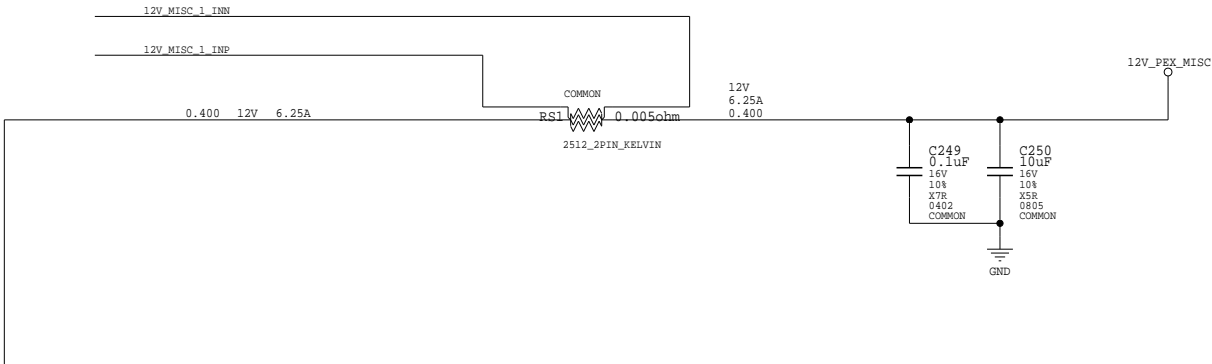
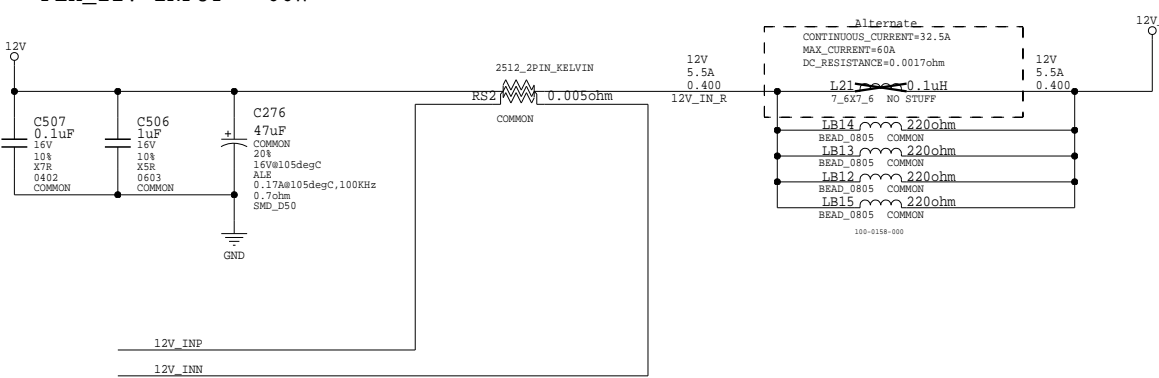
Page35: PS: Inputs, Filtering, and Monitoring



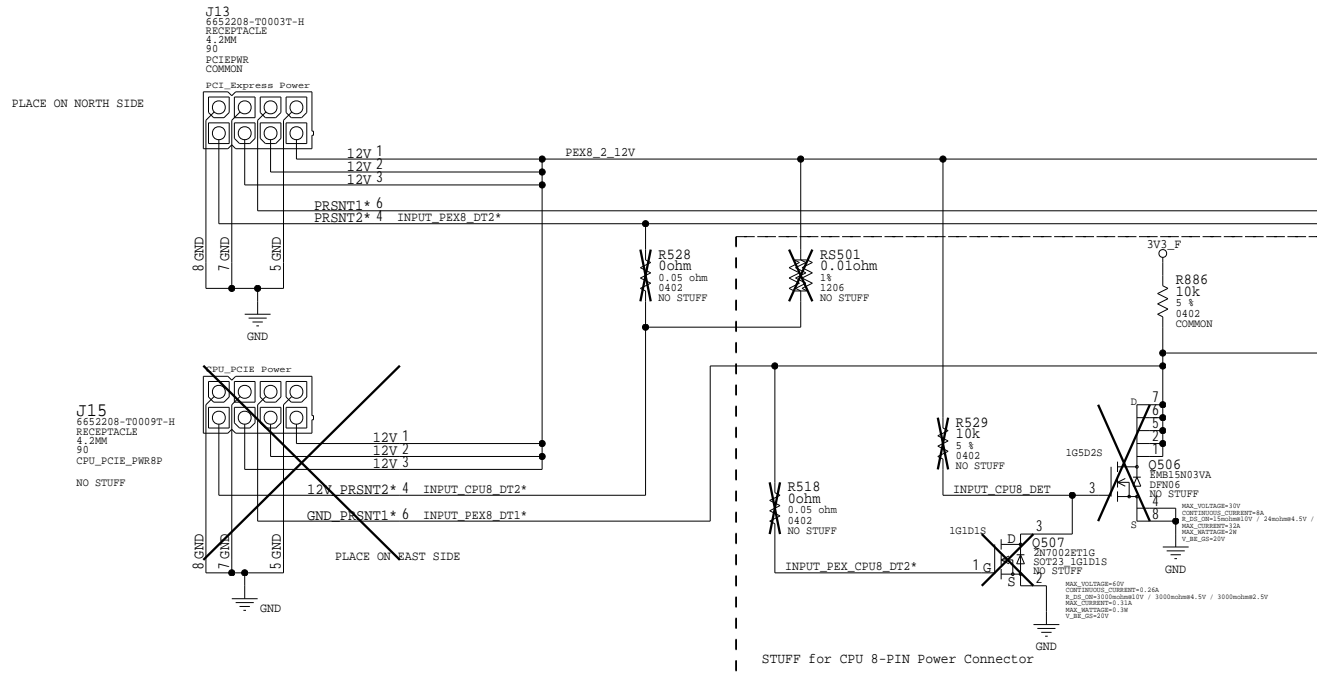
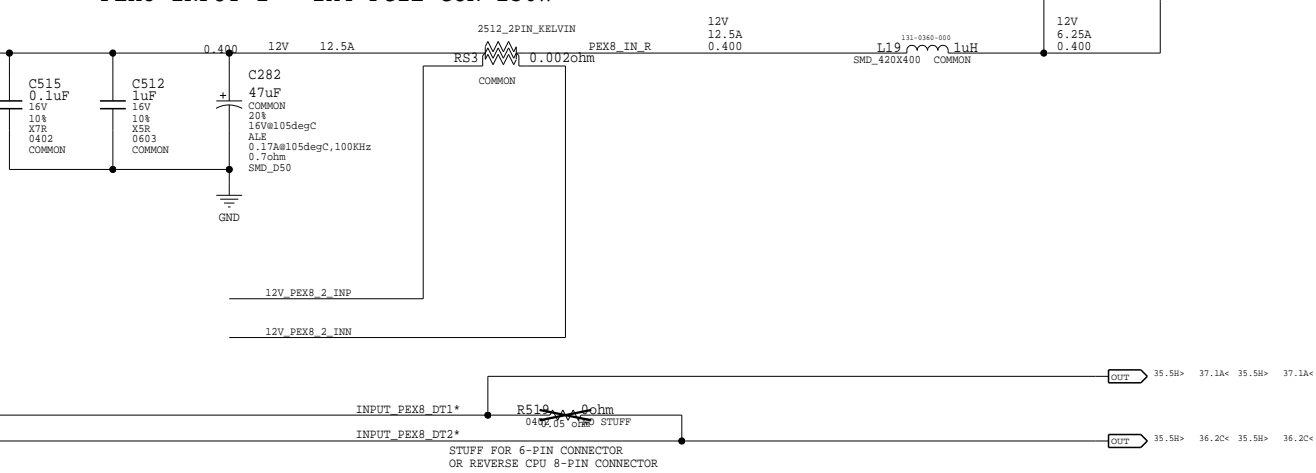
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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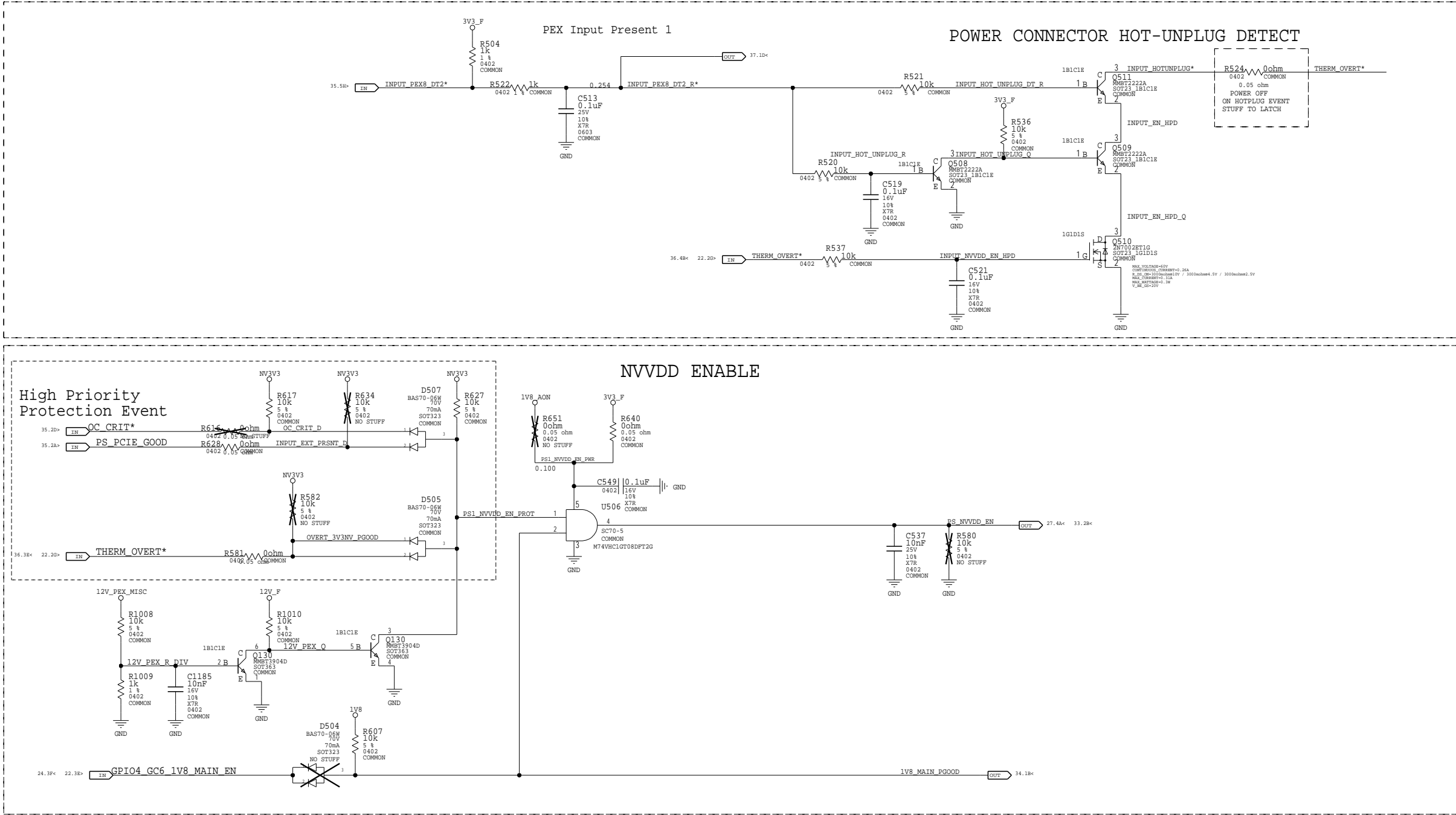
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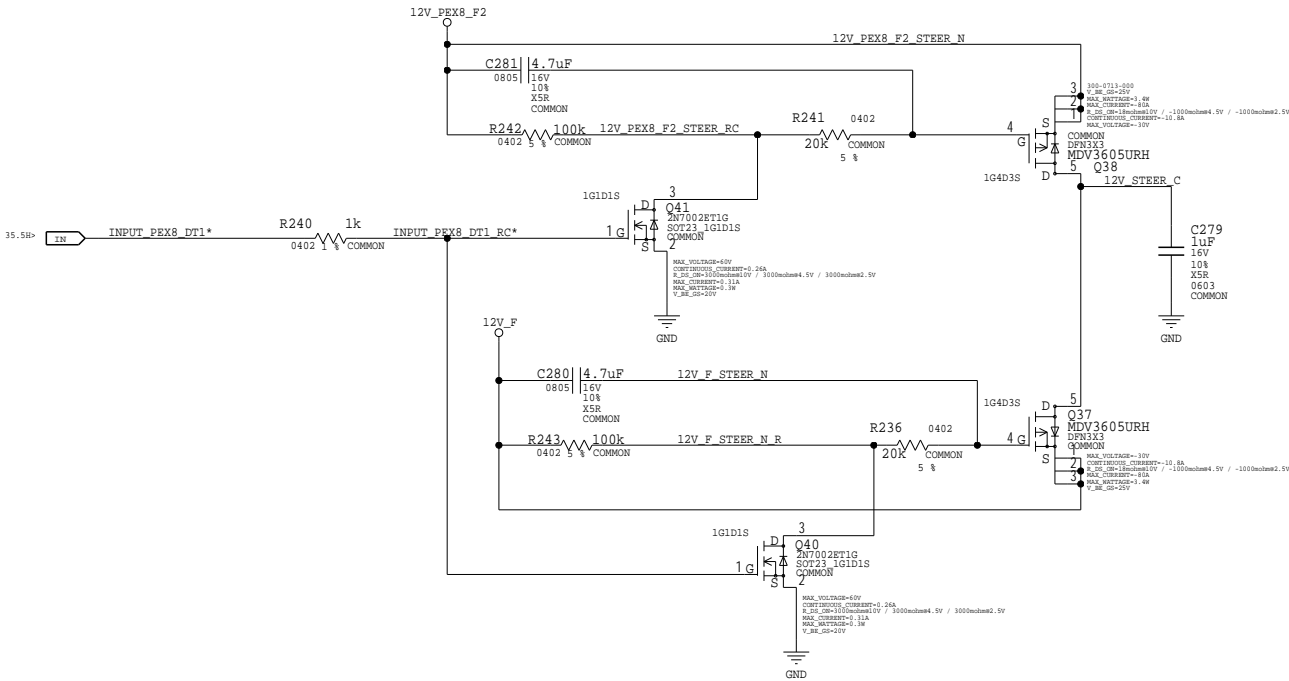
BOM REV K

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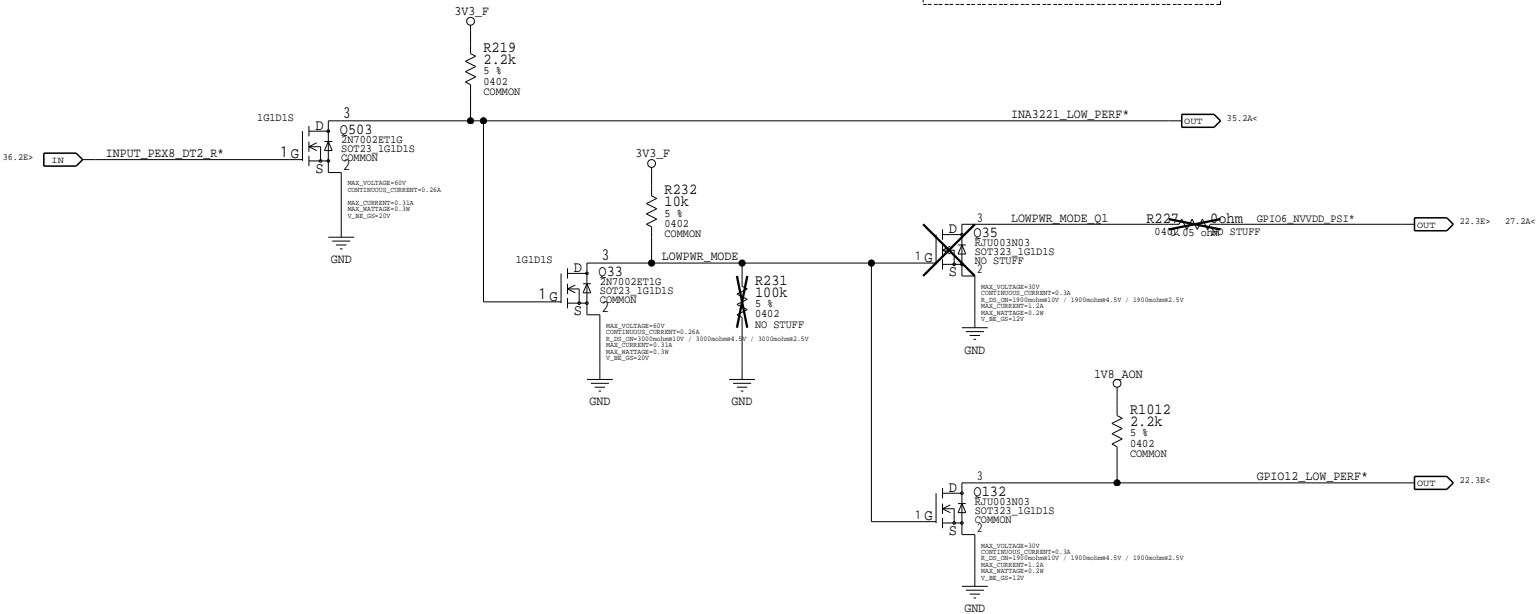
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PEX Input - 12V Current Steering FETs

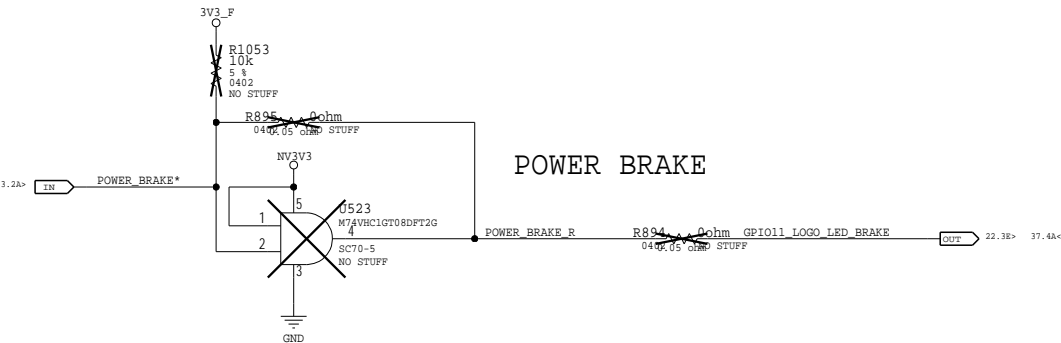


PEX Input - Power Level/PSI* Control



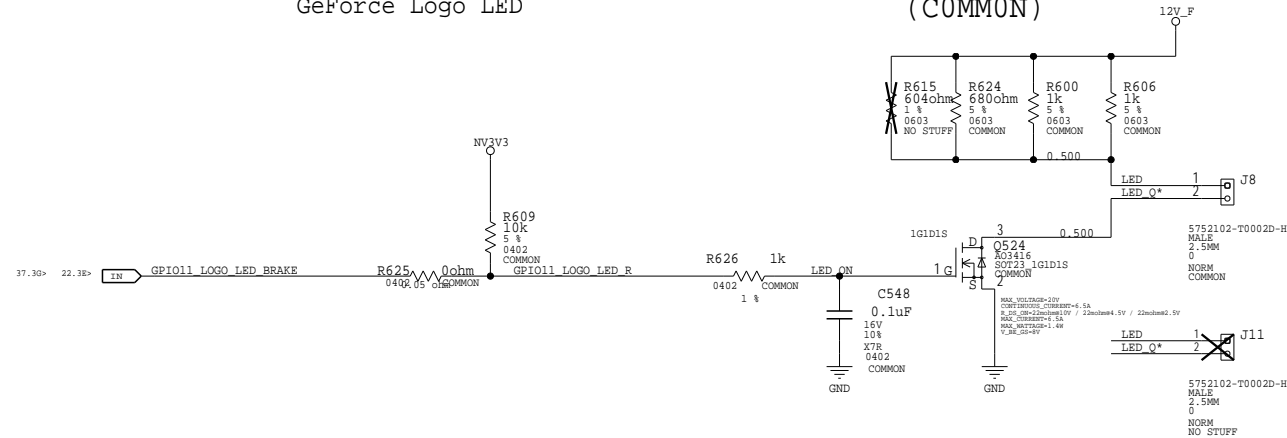
GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

POWER BRAKE

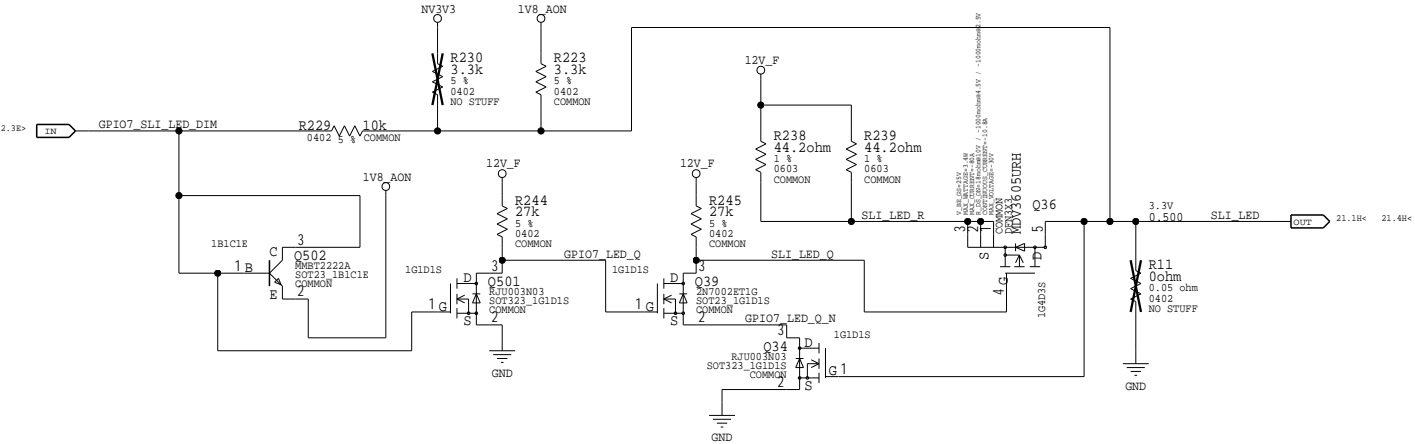


GeForce Logo LED

LED HEADER (COMMON)



SLI LED (GEFORCE ONLY)



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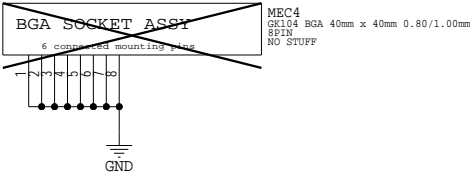
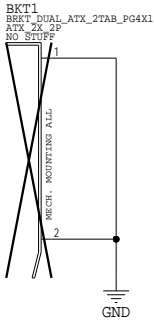
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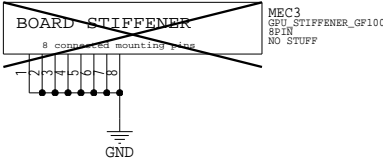
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Brackets:



GPU Stiffner



Mechanical Holes Symbol

