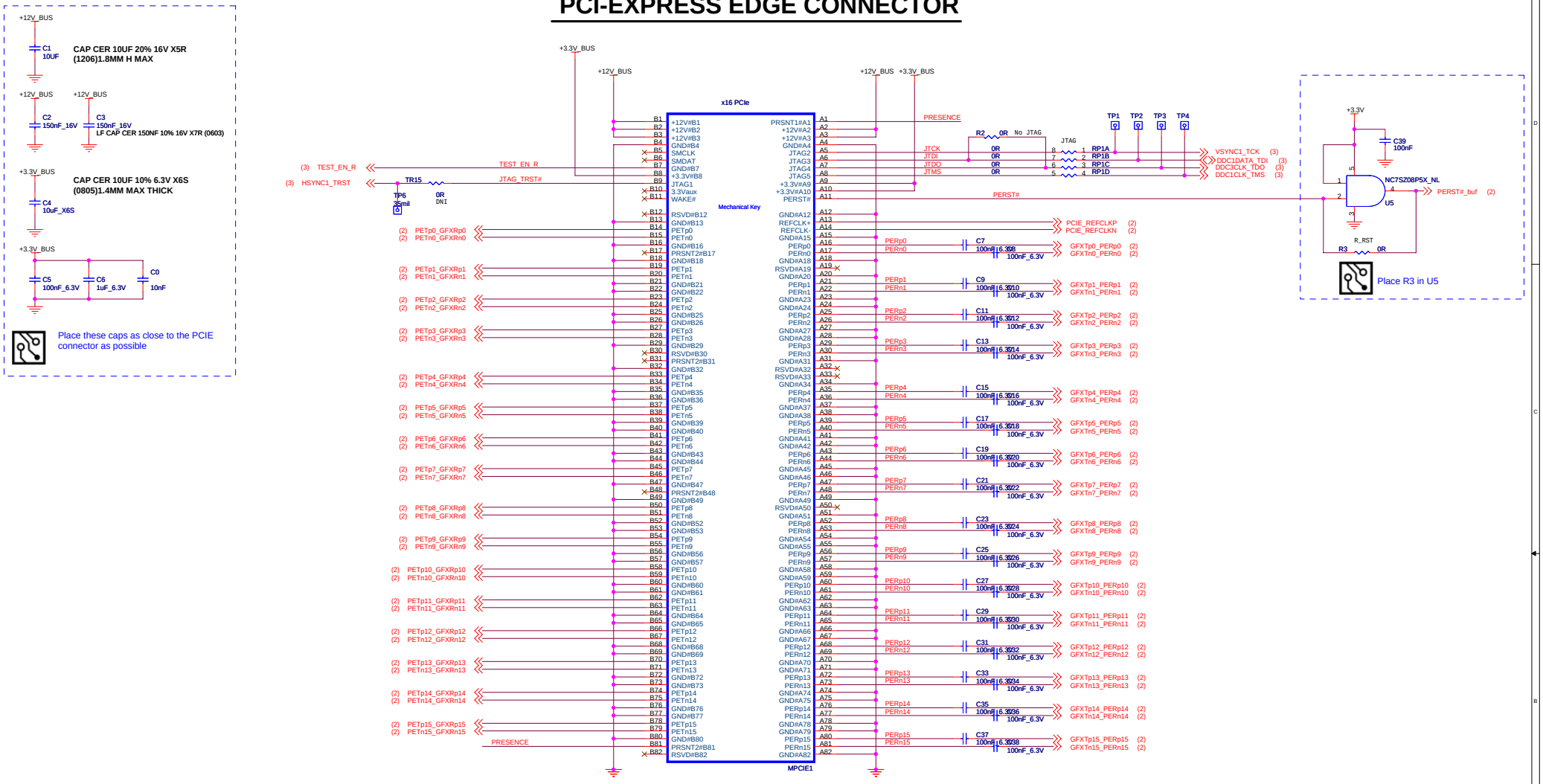
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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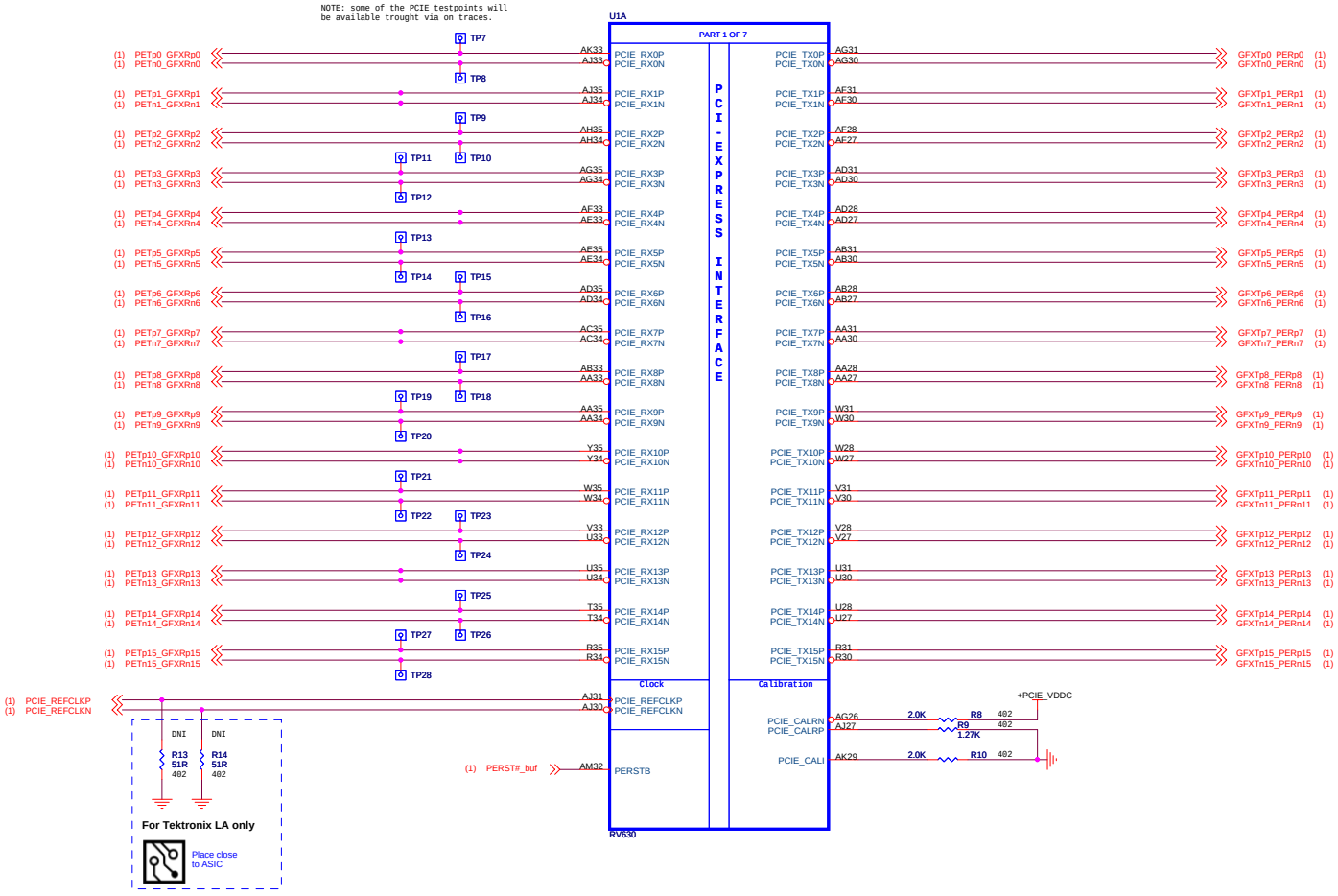
Title	RV630 GDDR3 - PCI-E Edge Connector		
Size C	Document Number 105-B148xx-00D		Rev 3
Date: Wednesday, May 09, 2007		Sheet 1 of 21	



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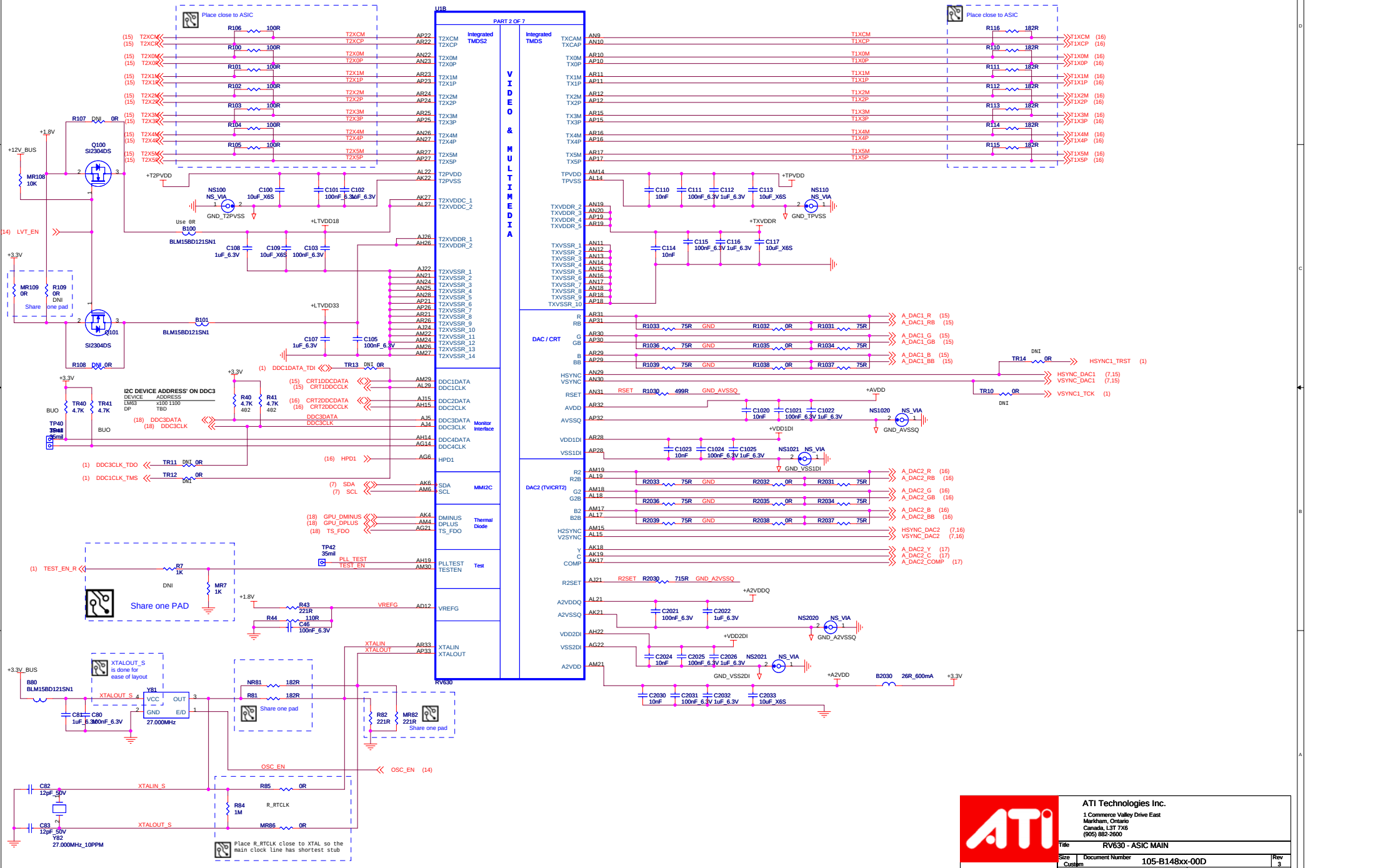
Title	RV630 GDDR3 - ASIC PCIE_Interface	
Size C	Document Number 105-B148xx-00D	Rev 3
Date: Wednesday, May 09, 2007	Sheet 2 of 21	

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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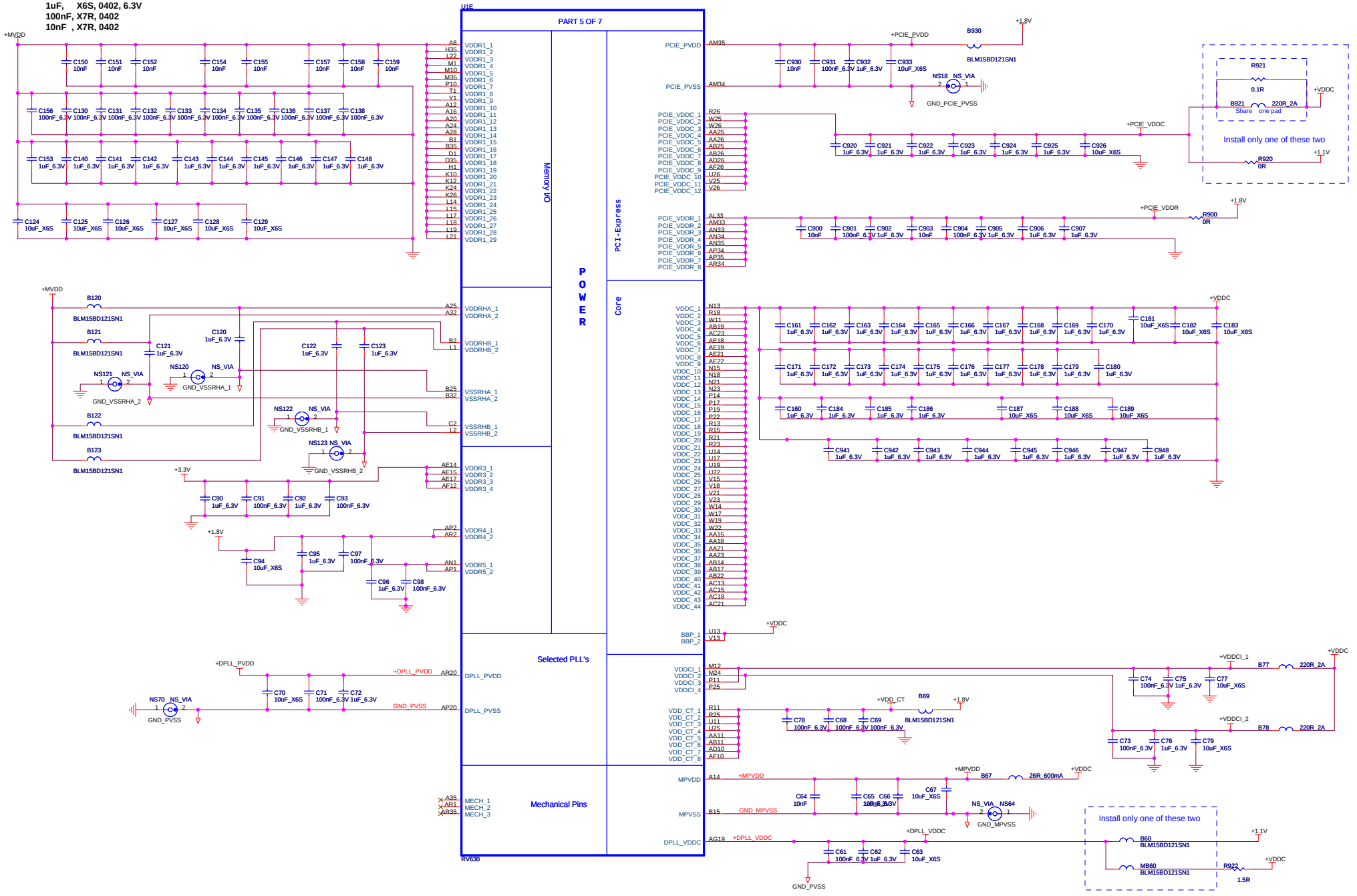
Title	RV630 - ASIC MAIN		
Size: Custom	Document Number: 105-B148xx-00D		Rev: 3
Date: Wednesday, May 09, 2007	Sheet 3 of 21		

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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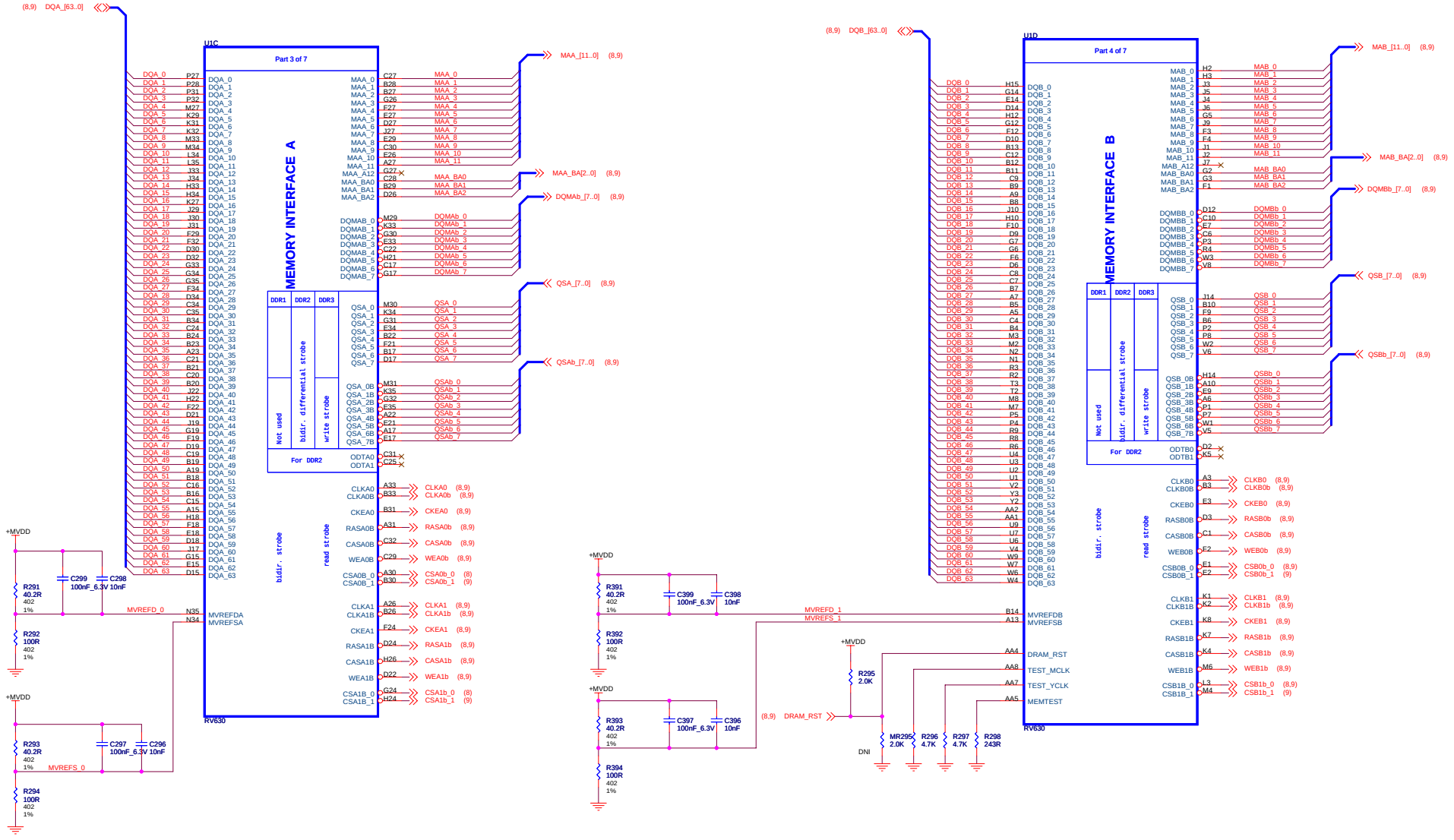
Title	RV630 GDDR3 - ASIC Power		
Size C	Document Number 105-B148xx-00D		Rev 3
Date: Wednesday, May 09, 2007	Sheet 4 of 21		



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Title	RV630 GDDR3 - ASIC Memory Interface (Channel A & B)		
Size C	Document Number 105-B148xx-00D		Rev 3
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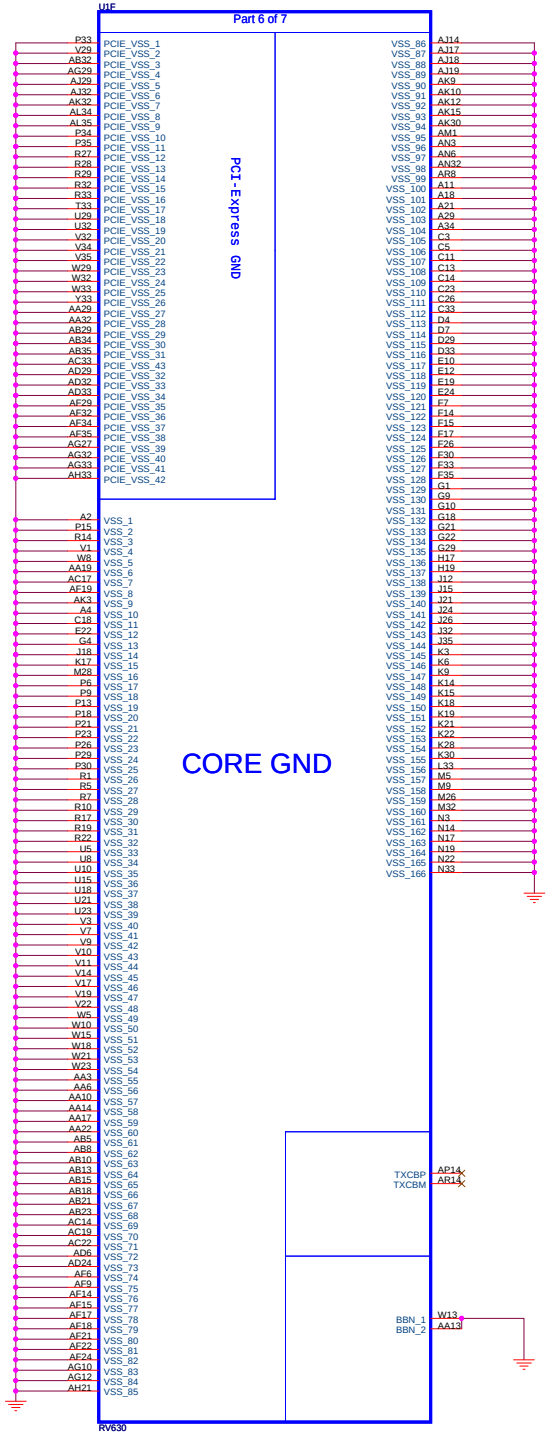

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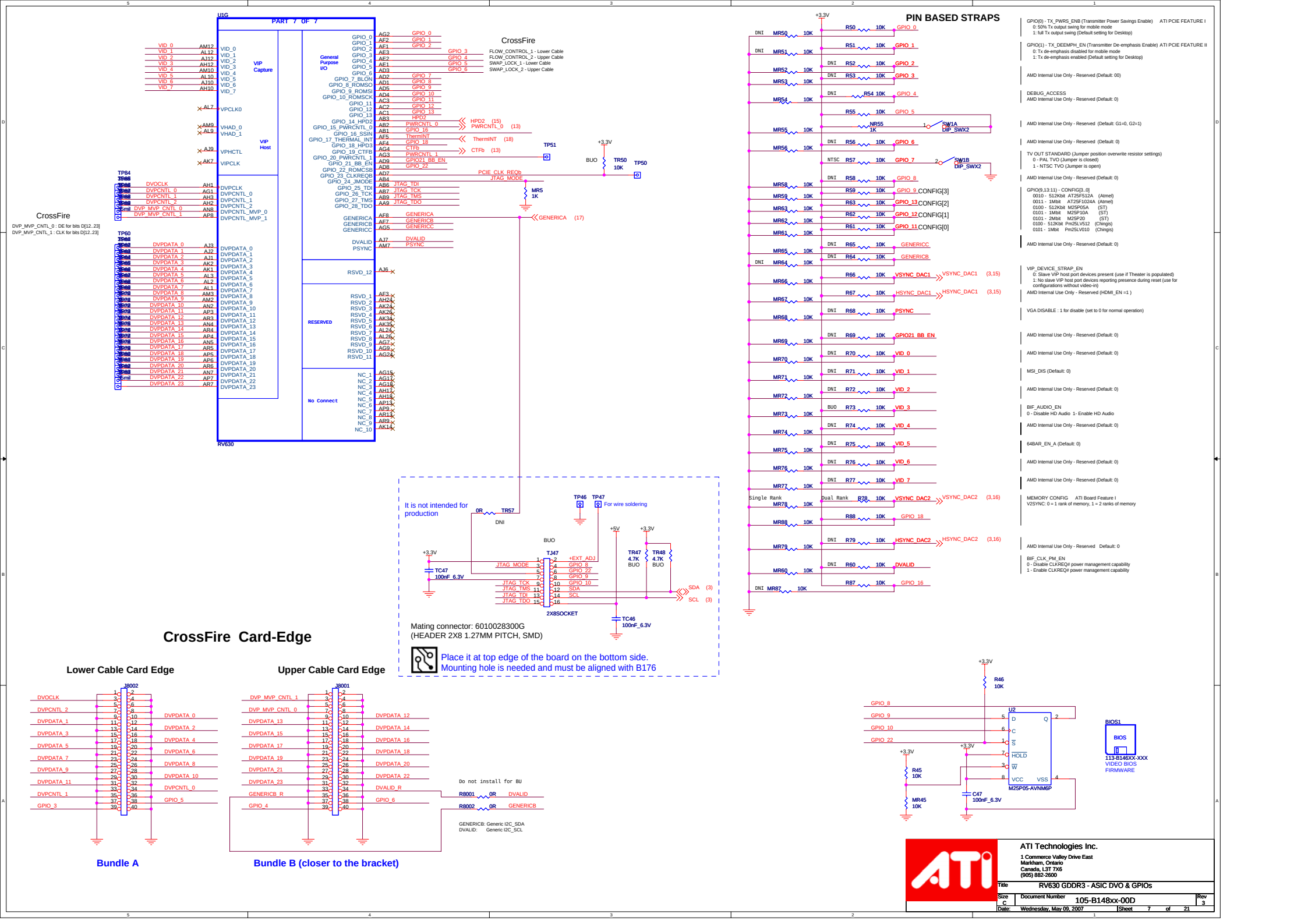
Title	RV630 GDDR3 - ASIC Grounds	
Size: C	Document Number: 105-B148xx-00D	Rev: 3
Date: Wednesday, May 09, 2007	Sheet 6 of 21	


U1G
PART 7 OF 7
RV630
VIP Capture
VIP Host
CrossFire
General Purpose I/O
RESERVED
No Connect
PIN BASED STRAPS
CrossFire Card-Edge
Lower Cable Card Edge
Upper Cable Card Edge
Bundle A
Bundle B (closer to the bracket)
It is not intended for production
For wire soldering
Mating connector: 6010028300G
(HEADER 2X8 1.27MM PITCH, SMD)
Place it at top edge of the board on the bottom side.
Mounting hole is needed and must be aligned with B176
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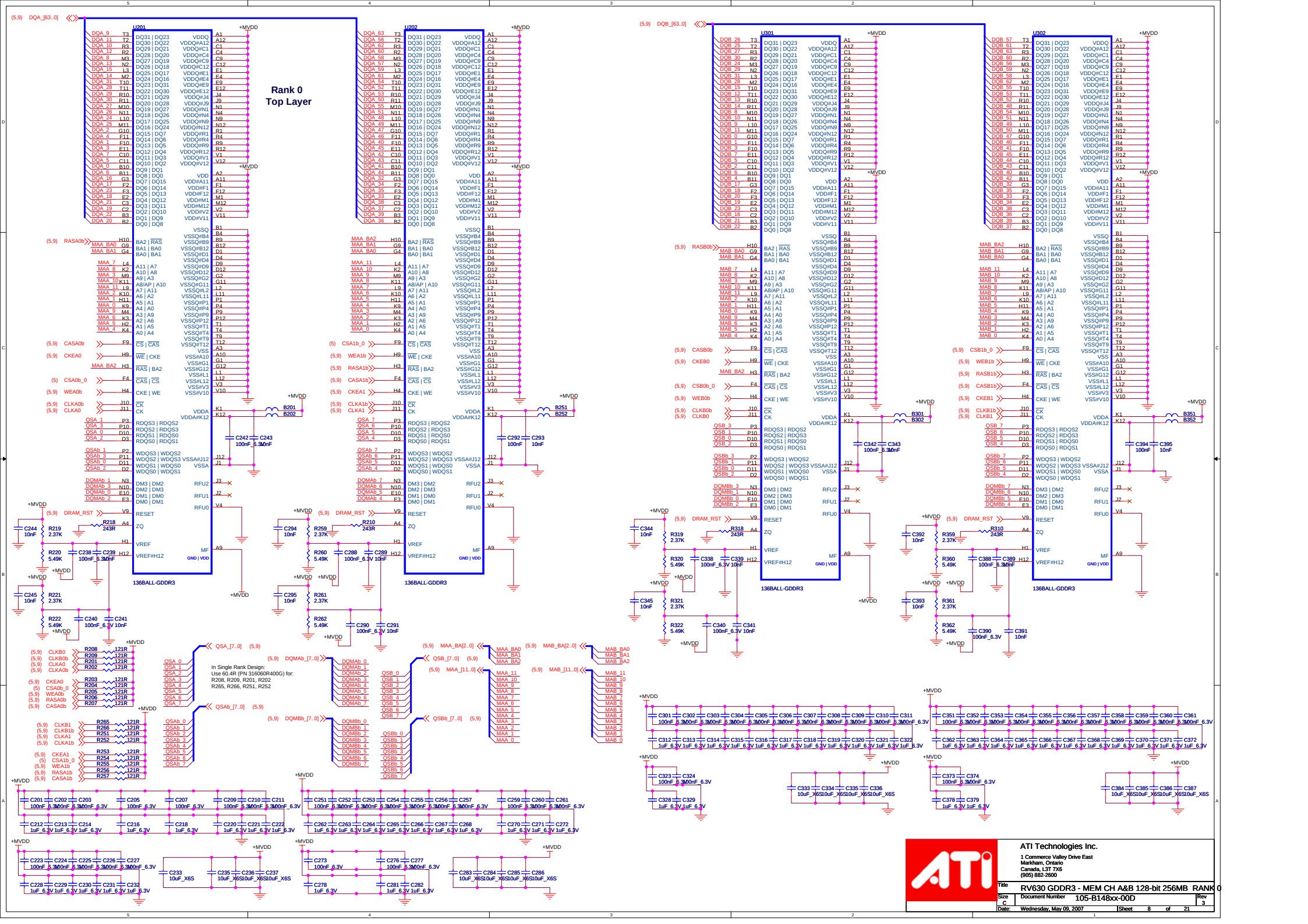
RV630 GDDR3 - ASIC DVO & GPIOs
105-B148xx-00D
Wednesday, May 09, 2007


Rank 0
Top Layer
U201
U202
U301
U302
136BALL-GDDR3
In Single Rank Design:
Use 60.4R (PN 316060R400G) for:
R208, R209, R201, R202
R265, R266, R251, R252
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(905) 882-2600
Title
RV630 GDDR3 - MEM CH A&B 128-bit 256MB RANK 0
Size
C
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8
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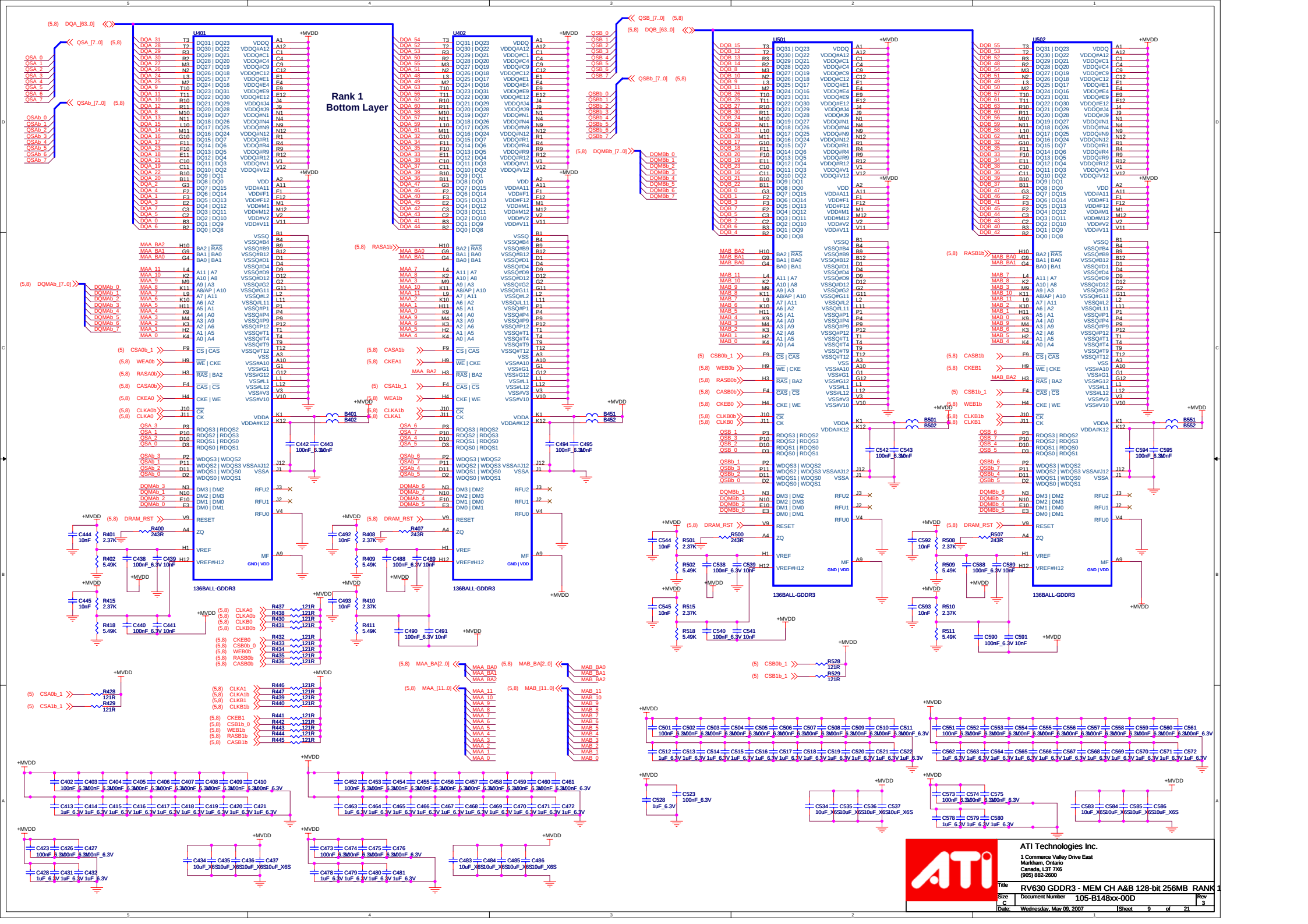

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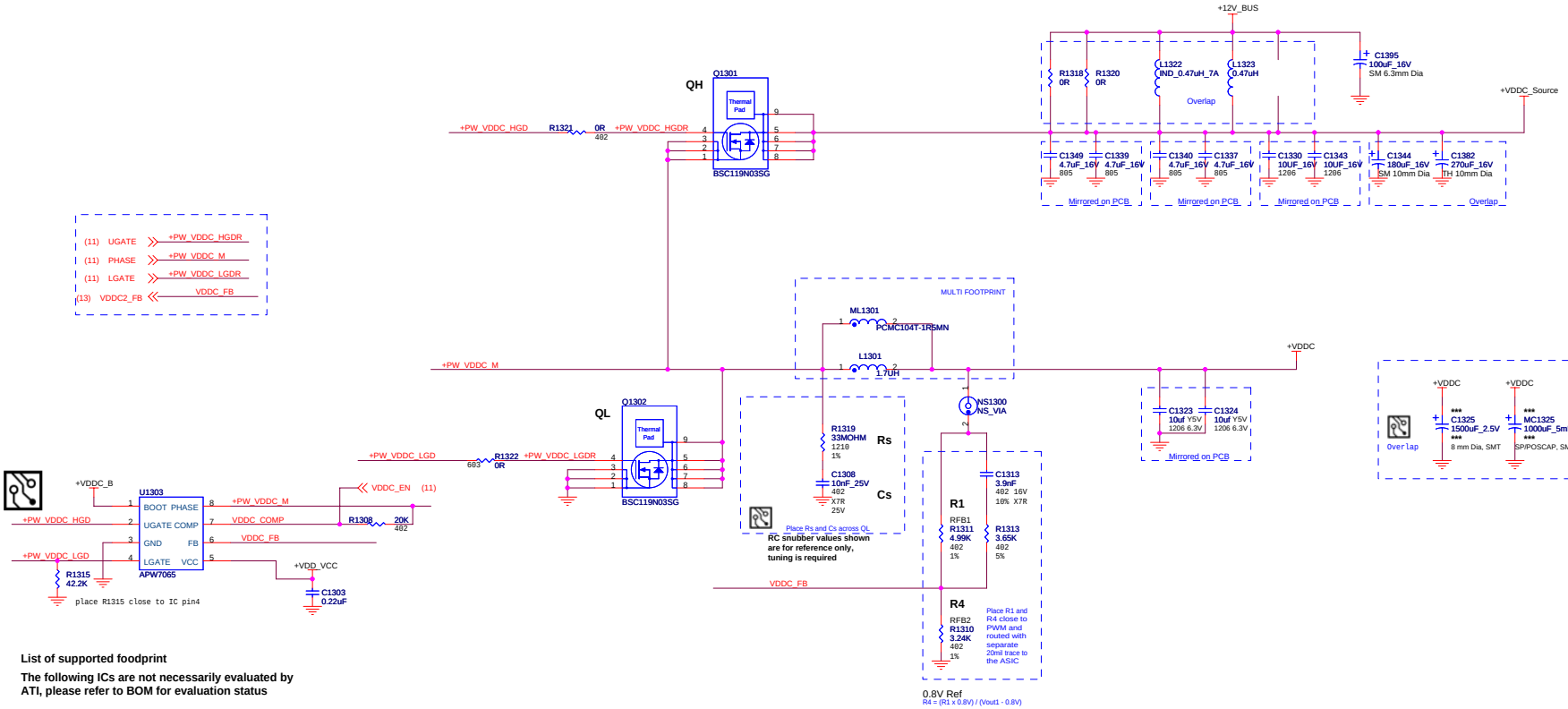
Title	RV630 GDDR3 - MEM CH A&B 128-bit 256MB RANK 1		
Size C	Document Number 105-B148xx-00D	Rev 3	
Date: Wednesday, May 09, 2007	Sheet 9 of 21		



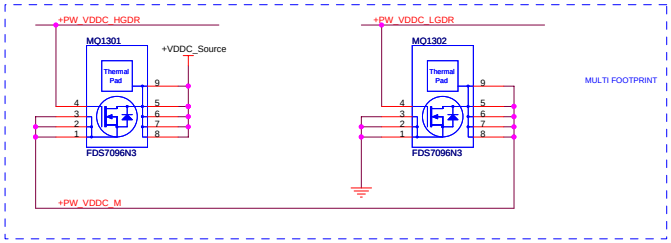
List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7120/APW7065 (12V)
CAT CAT7583 (12V)
INTERSIL ISL6545
NEXSEM NX2114/2307
RICHTEK RT9214/RT8101
OnSemi ON1582
uPI UP6101 (No Ext_Vref in)

Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



SMPS02- Regulator for VDDC

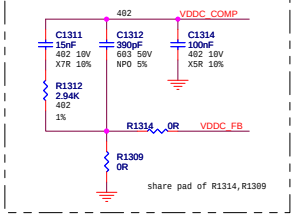
Vout = 0.9V ~ 1.1V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G

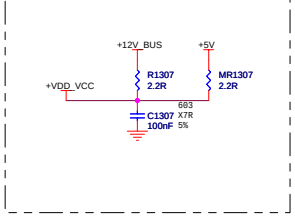
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

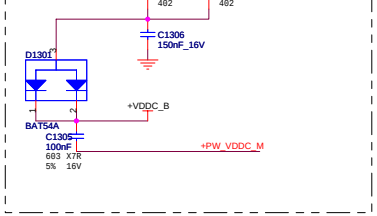
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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Title	RV630 GDDR3 - VDDC SMPS 01	
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Information on Compatable Controller Parts

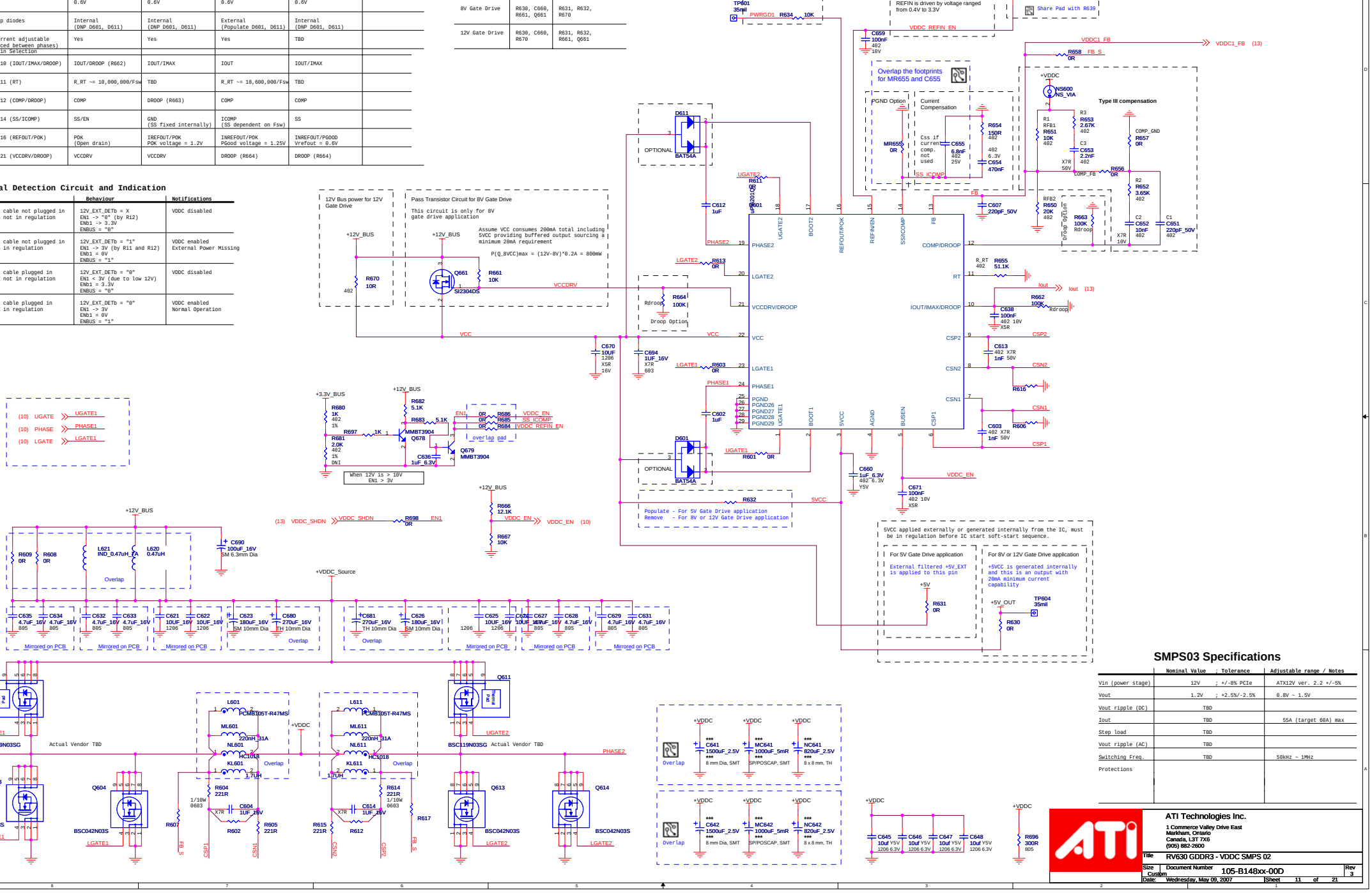
	PWM IC #1	PWM IC #2	PWM IC #3	PWM IC #4	
Gate drive voltage	5V, 8V, 12V	5V, 8V, 12V	5V only	12V only	
Vref	0.6V	0.6V	0.6V	0.6V	
Bootstrap diodes	Internal (DNP D601, D611)	Internal (DNP D601, D611)	External (Populate D601, D611)	Internal (DNP D601, D611)	
Phase current adjustable (unbalanced between phases)	Yes	Yes	Yes	TBD	
Option Pin Selection					
Pin 10 (IOUT/IMAX/DROOP)	IOUT/DROOP (R662)	IOUT/IMAX	IOUT	IOUT/IMAX	
Pin 11 (RT)	R_RT ~= 10,000,000/Fsw	TBD	R_RT ~= 18,600,000/Fsw	TBD	
Pin 12 (COMP/DROOP)	COMP	DROOP (R663)	COMP	COMP	
Pin 14 (SS/ICOMP)	SS/EN	GND (SS fixed internally)	ICOMP (SS dependent on Fsw)	SS	
Pin 16 (REFOUT/POK)	POK (Open drain)	IREFOUT/POK POK voltage = 1.2V	INREFOUT/POK PGood voltage = 1.25V	INREFOUT/PGOOD Vrefout = 0.6V	
Pin 21 (VCCDRV/DROOP)	VCCDRV	VCCDRV	DROOP (R664)	DROOP (R664)	

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661

External Detection Circuit and Indication

Cases	Behaviour	Notifications
External cable not plugged in +12V_BUS not in regulation	12V_EXT_DETb = X EN1 -> "0" (by Ri2) ENb1 -> 3.3V ENBUS = "0"	VDDC disabled
External cable not plugged in +12V_BUS in regulation	12V_EXT_DETb = "1" EN1 -> 3V (by Ri1 and R12) ENb1 = 0V ENBUS = "1"	VDDC enabled External Power Missing
External cable plugged in +12V_XXX not in regulation	12V_EXT_DETb = "0" EN1 < 3V (due to low 12V) ENb1 = 3.3V ENBUS = "0"	VDDC disabled
External cable plugged in +12V_XXX in regulation	12V_EXT_DETb = "0" EN1 -> 3V ENb1 = 0V ENBUS = "1"	VDDC enabled Normal Operation



SMPS03 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	1.2V ; +2.5%/-2.5%	0.8V ~ 1.5V
Vout ripple (DC)	TBD	
Iout	TBD	55A (target 60A) max
Step load	TBD	
Vout ripple (AC)	TBD	
Switching Freq.	TBD	50kHz ~ 1MHz
Protections		

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Title	RV630 GDDR3 - VDDC SMPS 02	
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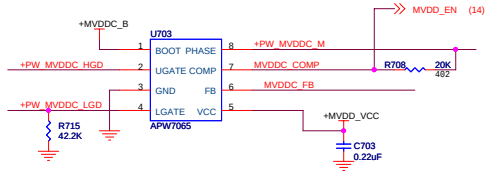
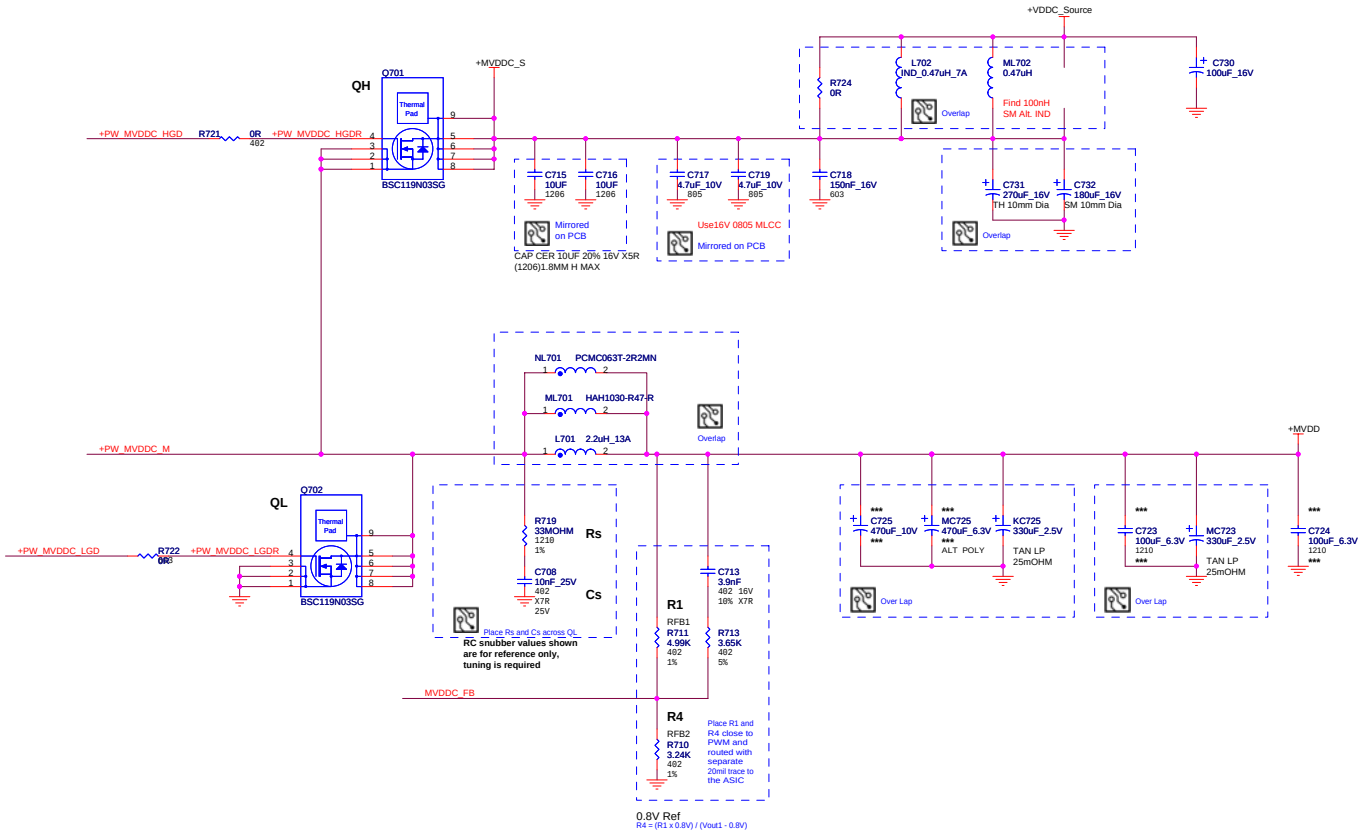
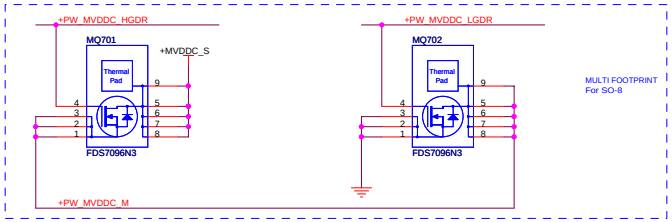


List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

- **ANPEC APW7120/APW7065 (12V)**
- **CAT CAT7583 (12V)**
- **INTERSIL ISL6545**
- **NEXSEM NX2114/2307**
- **RICHTEK RT9214/RT8101**
- **OnSemi ON1582**
- **uPI UP6101 (No Ext_Vref in)**
- **uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**





SMPS02- Regulator for MVDD

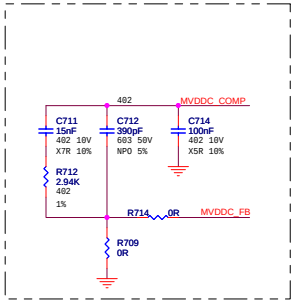
Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G

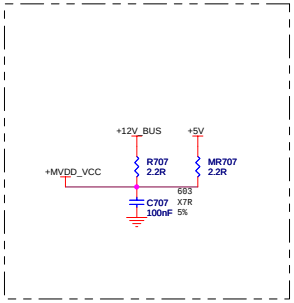
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

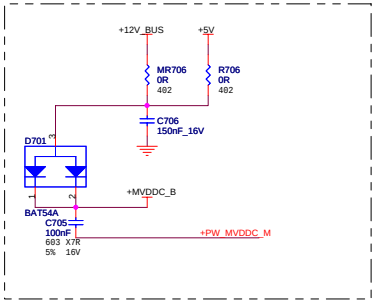
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

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Title: RV630 GDDR3 - MVDD SMPS 01

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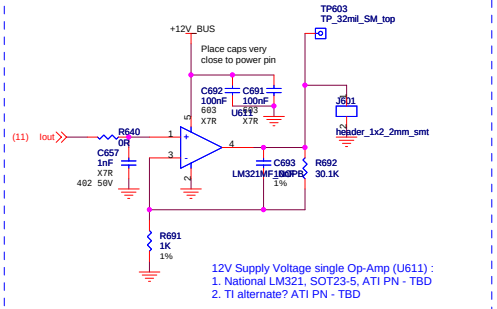
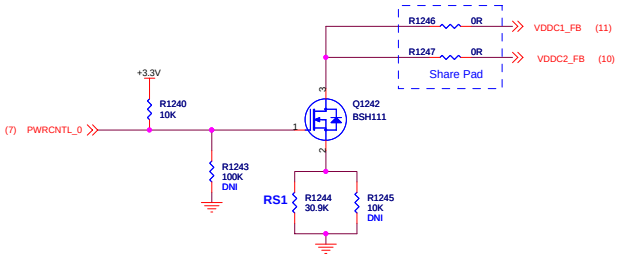
Buffered VDDC Output Current Monitoring



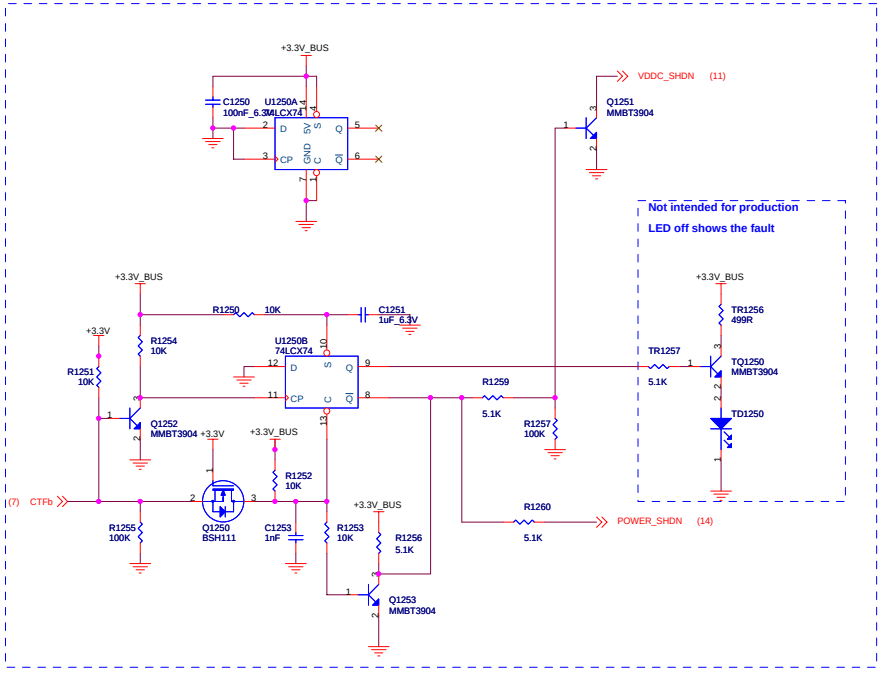
12V Supply Voltage single Op-Amp (U611) :
1. National LM321, SOT23-5, ATI PN - TBD
2. TI alternate? ATI PN - TBD

132-
For Testing purposes only



SMPS03- Regulator for VDDC
Vout = .9V ~ 1.2V

	VDDC	RS1	PWRCNTL_0
0.6V Ref	.9V	N/A	LOW
	1.0V	59.0K 1% ATI # 3160590200G	HIGH
	1.1V	30.9K 1% ATI # 3160309200G	HIGH
	1.2V	20.0K 1% ATI # 3160200200G	HIGH



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Title	RV630 GDDR3 - Power Management	
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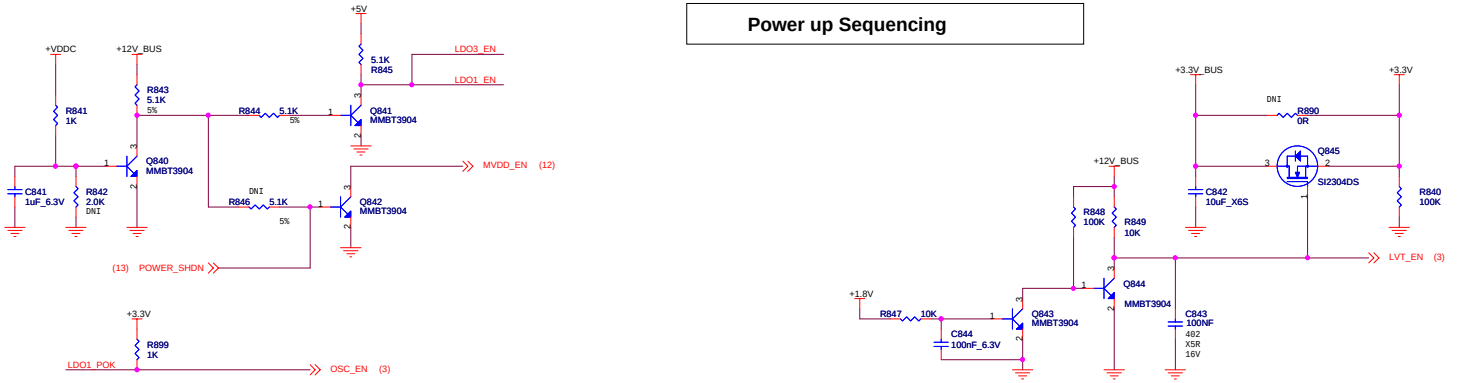
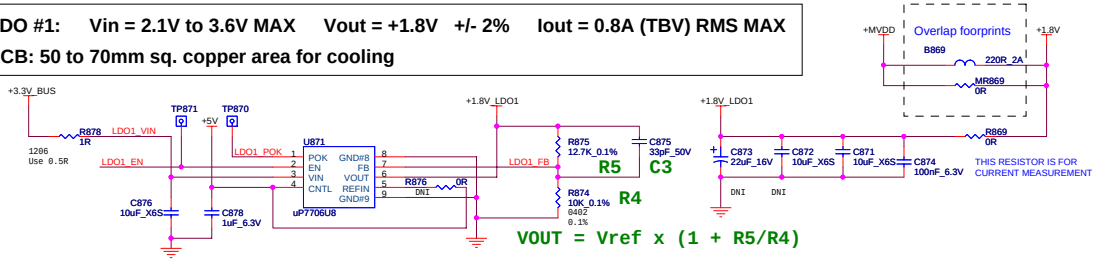
Power up Sequencing



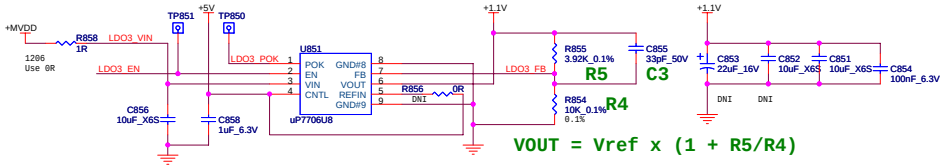
LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

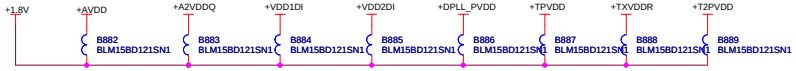


LDO #3: Vin = +1.45V to 2.1VMAX Vout = +1.1V +/- 2% Iout = 1.1A (TBV) RMS MAX

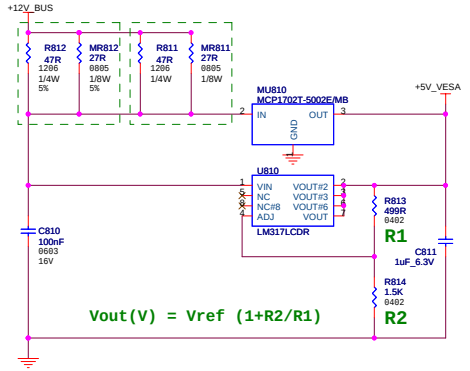
PCB: 50 to 70mm sq. copper area for cooling

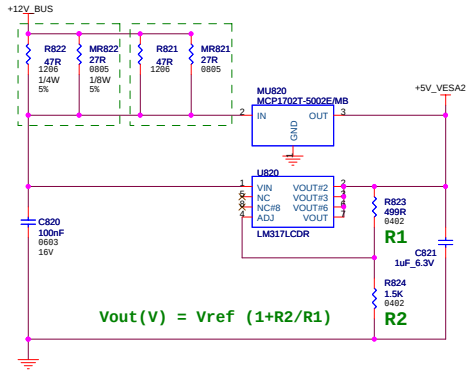


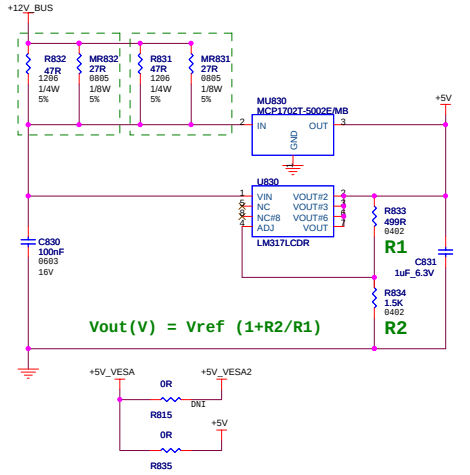
Shared Power Rails



Regulators for +5V, +5V_VESA and +5V_VESA2







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Title	RV630 GDDR3 - Linear Regulators	
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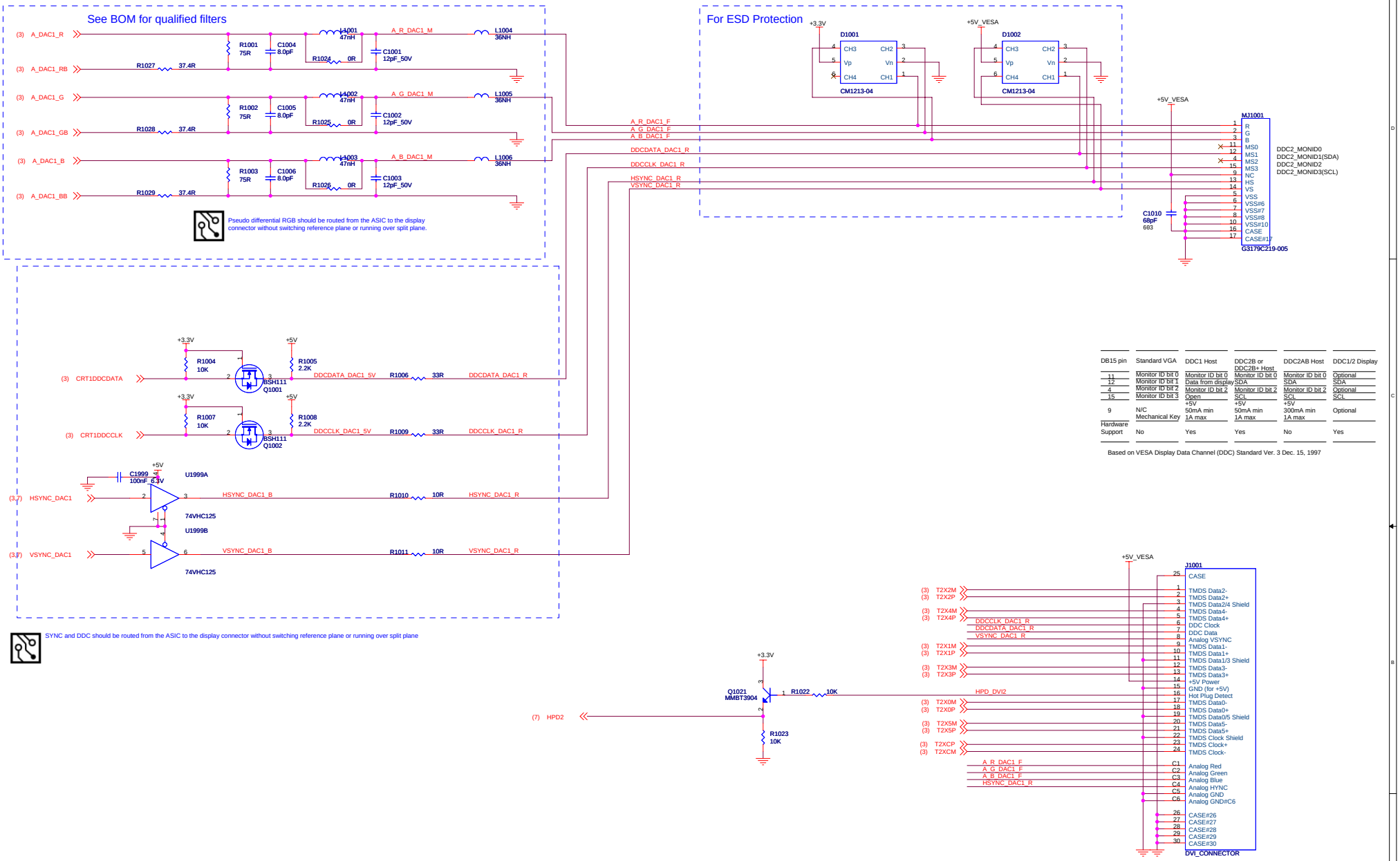

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

Title	RV630 GDDR3- DAC1&TMDS2
Size	Custom
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See BOM for qualified filters

(3) A_DAC2_R — R2001 75R 402 — C2004 8.0pF 402 — L2001 47nH — R2024 0R — C2001 12pF_50V — A_R_DAC2_M — L2004 36NH

(3) A_DAC2_RB — R2027 37.4R

(3) A_DAC2_G — R2002 75R 402 — C2005 8.0pF 402 — L2002 47nH — R2025 0R — C2002 12pF_50V — A_G_DAC2_M — L2005 36NH

(3) A_DAC2_GB — R2028 37.4R

(3) A_DAC2_B — R2003 75R 402 — C2006 8.0pF 402 — L2003 47nH — R2026 0R — C2003 12pF_50V — A_B_DAC2_M — L2006 36NH

(3) A_DAC2_BB — R2029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

+3.3V — D2001 CM1213-04 — +5V_VESA2 — D2002 CM1213-04

For ESD Protection

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R

+5V_VESA2 — C2010 68pF 603 — MJ2001 G3179C219-005

MJ2001: R, G, B, MS0, MS1, MS2, MS3, NC, HS, VS, VSS, VSS#6, VSS#7, VSS#8, VSS#10, CASE, CASE#17

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

(3) CRT2DDCDATA — +3.3V — R2004 10K — +5V — R2005 2.2K 402 — Q2001 BSH111 — DDCDATA_DAC2_5V — R2006 33R 402 — DDCDATA_DAC2_R

(3) CRT2DDCCLK — +3.3V — R2007 10K — +5V — R2008 2.2K 402 — Q2002 BSH111 — DDCCLK_DAC2_5V — R2009 33R 402 — DDCCLK_DAC2_R

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

U1999C — (3,7) HSYNC_DAC2 — 74VHC125 — HSYNC_DAC2_B — R2010 10R 402 — HSYNC_DAC2_R

U1999D — (3,7) VSYNC_DAC2 — 74VHC125 — VSYNC_DAC2_B — R2011 10R 402 — VSYNC_DAC2_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

+3.3V — Q2021 MMBT3904 — R2022 10K — HPD_DVI1 — (3) HPD1 — R2023 10K

+5V_VESA2 — J2001 DVI_CONNECTOR

(3) T1X2M	R2017 0R	1	TMDS Data2-
(3) T1X2P	R2018 0R	2	TMDS Data2+
		3	TMDS Data2/4 Shield
(3) T1X4M		4	TMDS Data4-
(3) T1X4P		5	TMDS Data4+
DDCCLK_DAC2_R		6	DDC Clock
DDCDATA_DAC2_R		7	DDC Data
VSYNC_DAC2_R		8	Analog VSYNC
(3) T1X1M	R2015 0R	9	TMDS Data1-
(3) T1X1P	R2016 0R	10	TMDS Data1+
		11	TMDS Data1/3 Shield
(3) T1X3M		12	TMDS Data3-
(3) T1X3P		13	TMDS Data3+
		14	+5V Power
		15	GND (for +5V)
HPD_DVI1		16	Hot Plug Detect
(3) T1X0M	R2013 0R	17	TMDS Data0-
(3) T1X0P	R2014 0R	18	TMDS Data0+
		19	TMDS Data0/5 Shield
(3) T1X5M		20	TMDS Data5-
(3) T1X5P		21	TMDS Data5+
		22	TMDS Clock Shield
(3) T1XCP	R2019 0R	23	TMDS Clock+
(3) T1XCM	R2020 0R	24	TMDS Clock-
A_R_DAC2_F		C1	Analog Red
A_G_DAC2_F		C2	Analog Green
A_B_DAC2_F		C3	Analog Blue
HSYNC_DAC2_R		C4	Analog HYNC
		C5	Analog GND
		C6	Analog GND#C6
		25	CASE
		26	CASE#26
		27	CASE#27
		28	CASE#28
		29	CASE#29
		30	CASE#30

+5V_VESA2 — B2012 220R — R2012 4.7K DNI — C2012 100pF_50V

55mA current limited for +5V rail

Place C2012 close to J2001

NJ2001 LONG_TYPE-2_HDMI

(3) T1X2P	1	GND#20	20
	2	GND#21	21
(3) T1X2M	3	GND#22	22
(3) T1X1P	4	GND#23	23
(3) T1X1M	5		
(3) T1X0P	6		
(3) T1X0M	7		
(3) T1XCP	8		
(3) T1XCM	9		
DDCCLK_DAC2_R	10		
DDCDATA_DAC2_R	11		
HPD_DVI1	12		
	13		
	14		
	15		
	16		
	17		
	18		
	19		

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Title: RV630 GDDR3-DAC2/TMDS1
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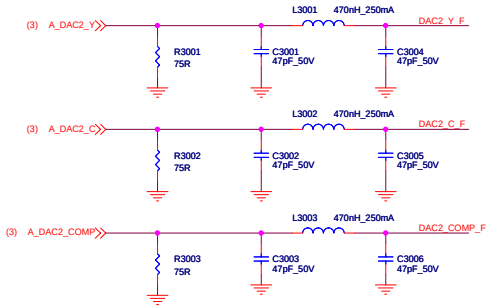
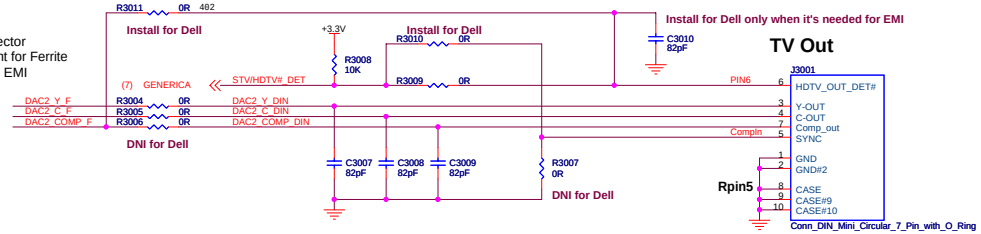


Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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Title	RV630 GDDR3 - TVO	
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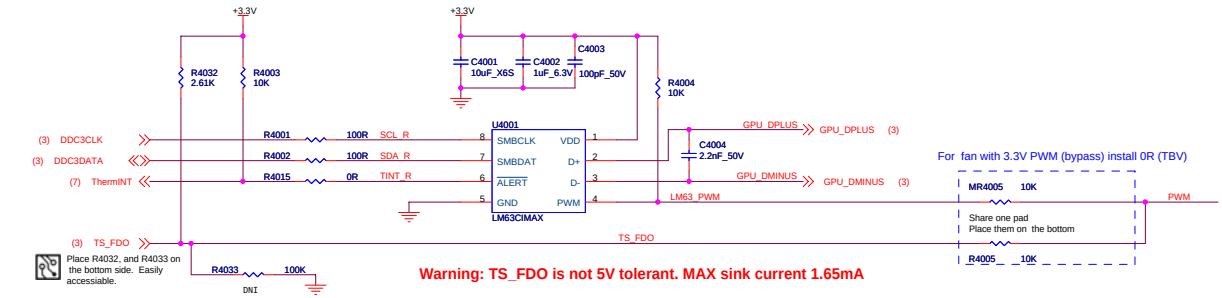
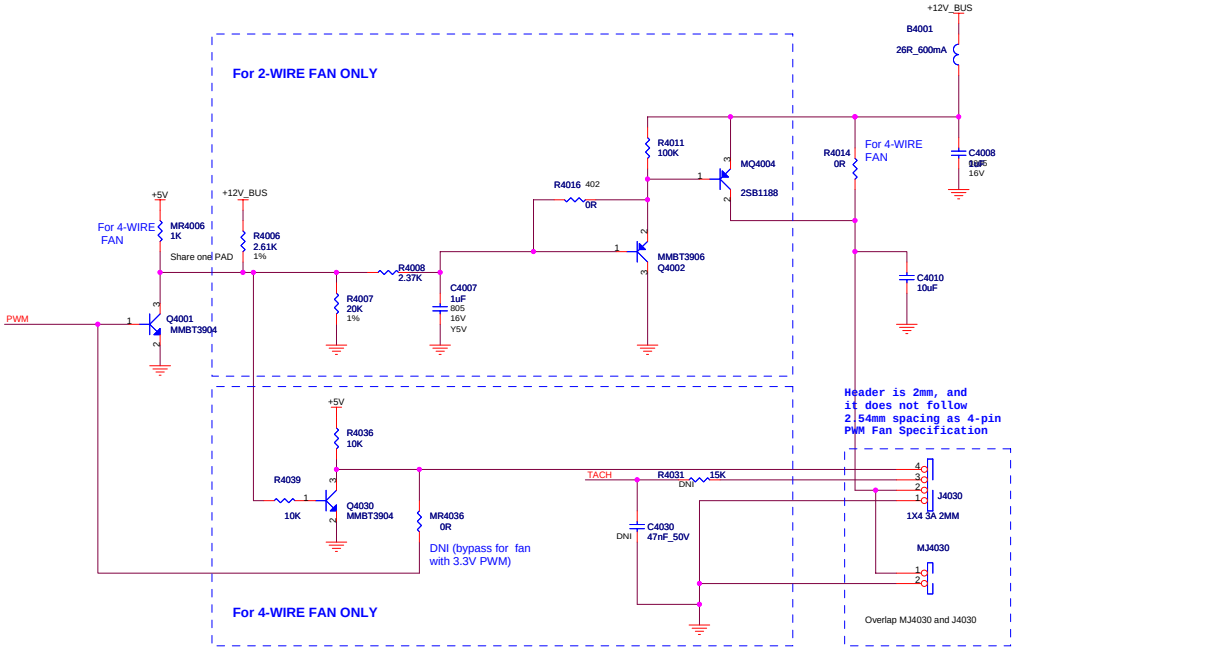
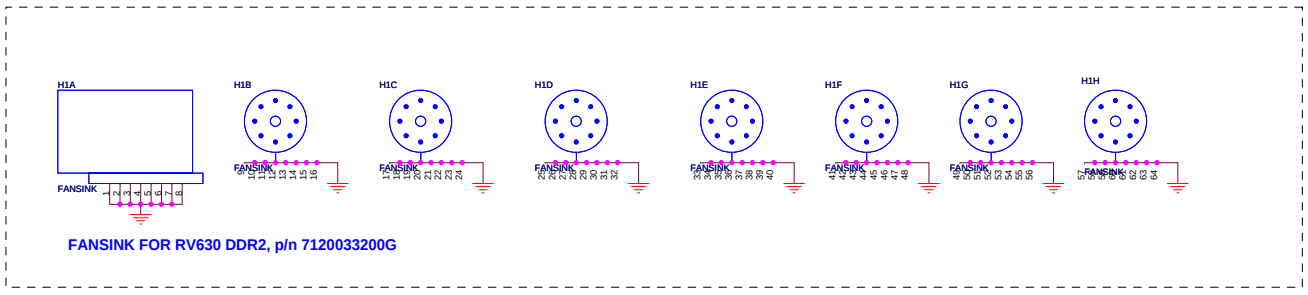
LM63 is for BU only, until built-in fan controller is verified.



Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA





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Title	RV630 GDDR3- Thermal Management		
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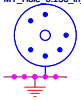
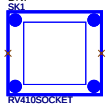
DVI/DVI SCREWS with top tab

MT2
MT_Hole_0.136_in_6VIA



DNI
SK1



RV410SOCKET

PCB1

109-B14831-00C

BKT1

80200386B0G

<Variant Name>

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Title	RV630 GDDR3- Mechanical	
Size: C	Document Number: 105-B148xx-00D	Rev: 3
Date: Wednesday, May 09, 2007	Sheet 19 of 21	

<variant Name>

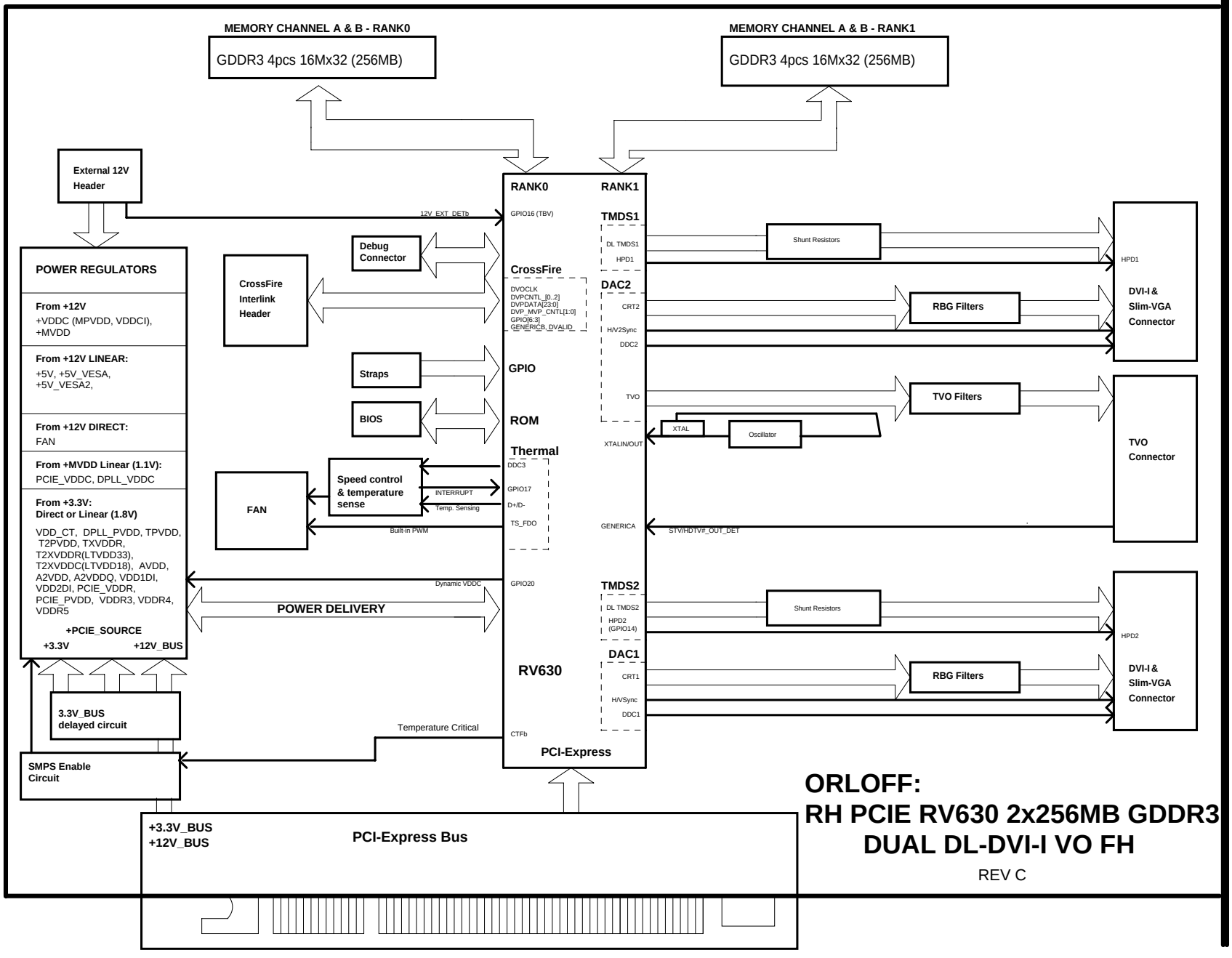
Title	Schematic No.	Date:
RH PCIE RV630 2x256MB GDDR3 DUAL DL-DVI-I VIVO FH	105-B148xx-00D	Saturday, May 05, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.

Rev 3

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/02/06	Initial design for RV630 GDDR3
1	00B	04/09/07	Added pull down MR5 on JTAG_MODE (pg 7) Connected C239, C241, C289, C291, C339, C341, C389, C391 to GND instead of MVDD (MTAG recommendation) (pg 8/9) Added C244, C245, C292, C293, C344, C345, C394, C395, C444, C445, C492, C493, C544, C545, C592, C593 for noise reduction (pg 8/9) Removed duplicated footprints R723 and B703 on MVDD power supply (pg 12) I2C block removed (pg 13) / Off page connection for MVDDC_FB removed (pg 12) Label changed from LDO2_POK to LDO1_POK (pg 14) HDMI connector (dual footprint for DVI and HDMI) NJ2001 added (pg 16) R2013~R2020 added for TMDS lines (pg 16) C4010 added for ripple reduction when using 2-wire fan (pg 18) Component PN changed to match updated BOM (no footprint changes) (Layout) Q842 moved close to MVDD SMPS block (Layout) Move MVDD caps close to DRAM
2	00C	04/13/07	(Layout) Enlarged VDDC plane
3	00D	05/04/07	(Layout) Update. No Schematic changes.



ORLOFF:
RH PCIE RV630 2x256MB GDDR3
DUAL DL-DVI-I VO FH

REV C

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Title	RV630 GDDR3 - BLOCK DIAGRAM	
Size: C	Document Number: 105-B148xx-00D	Rev: 3
Date: Saturday, May 05, 2007	Sheet 21 of 21	