



TU106-400A GPU

NPN-09110-001_v01 | July 2018

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New Product Notice

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Gigabyte Desktop 2018-08-15 00:13:35

New Product Notice

NPN-09110-001_v01

New Product Introduction

This NPN specifies the following new NVIDIA® TU106-400A GPU. This GPU is offered in the GB4B-256 (2228-ball BGA, 37.5 mm × 37.5 mm) package only.

Notification

August 2018

Planned Implementation

Now

Product Information

These new products represent the high-end of the Enthusiast consumer desktop GPU segment. They are based on the new NVIDIA Turing graphics architecture and will be manufactured using qualified suppliers per our approved suppliers’ list and are RoHS and Halogen-free compliant.

Key Specifications:

	TU106-400A
Chip	TU106-400A-A1
Device ID	0x1F07
Memory interface	256-bit GDDR6
Package	GB4B-256

Impact of Change and Recommended Action

NVIDIA is committed to providing our customers with quality products that push the edge of technology and at the same time enable product segmentation. To help guarantee a rapid time-to-market launch and smooth and uninterrupted product supply, NVIDIA strongly recommends that customers qualify these GPUs as soon as possible.

Forecasted Key Milestones

TU106-400A-A1: OS

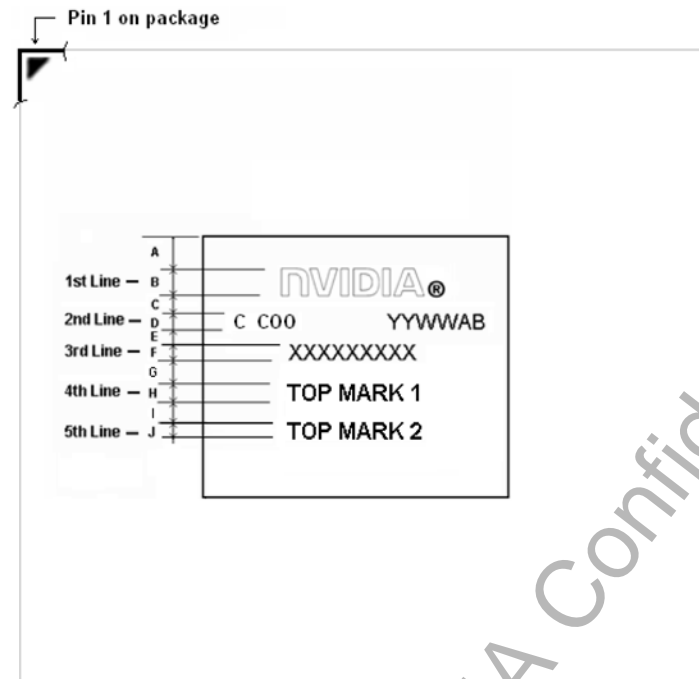
August 2, 2018

TU106-400A-A1: Production

August 31, 2018

Product Marking and Traceability

TU106-400A Markings



Pin 1: Location of Pin 1 in upper left when reading the marking.

Line 1: Company Name

Line 2: Assembly information: plant identifier (C) and country of origin (COO):

- C = Plant identifier: A (ASE), B (Amkor K5), K (Amkor K4), R (ATT - Amkor Tech), S (SPIL), T (TSMC).

- COO = Country of origin: Taiwan for ASE, ATT, SPIL and TSMC, and Korea for Amkor K4 and Amkor K5.

- YYWW = Assembly date code
- AB = Mask revision

Line 3: Assembly lot number (XXXXXXXX).

The first character identifies the wafer Fab location:

- P = TSMC Fab 14

Line 4: Product Part Number, for example: XXXXX-XX-XX

Line 5: <BLANK>

Products Affected/Ordering Codes

Product	NVIDIA Part Number ¹	Marketing Part Number for P.O.	Comments
TU106-400A	TU106-400A-A1	TU106-400A-A1	37.5 mm × 37.5 mm 2228-ball BGA (GB4B-256)

Note:

¹ The NVIDIA part number is provided in this document as a reference for product shipping and handling at factory. This part number is NVIDIA confidential.

Revision History

Version	Date	Authors	Description of Change
01	July 24, 2018	QL, DR	Initial release

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TU106 Graphics Processing Unit

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Data Sheet

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DOCUMENT CHANGE HISTORY

DS-09129-001_v01

Version	Date	Authors	Description of Change
01	August 7, 2018	RT, DR	Initial Release

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1 INTRODUCTION

Overview

The Graphics Processing Unit (GPU) covered in this data sheet is designed using a new architecture to bring a new level of performance to visual graphics and computing software applications. This GPU fully integrates hardware acceleration for both graphics and computing code, enabling hardware acceleration of a wider class of software applications than ever before.

The NVIDIA® TU106 GPU is fabricated using TSMC 12FFB process technology to provide maximum performance. The TU106 GPU supports GDDR6 memories.

Features and Technologies

The TU106 GPU supports the following features and technologies:

- ▶ Direct3D 12 and Shader Model 7.0
- ▶ OpenGL 4.5
- ▶ Vulkan 1.0
- ▶ NVIDIA® PhysX™ (Ageia PhysX) technology
- ▶ NVIDIA® CUDA® technology

Memory Support

The TU106 GPU supports a 256-bit frame buffer memory interface using GDDR6 memories.

Display

Key display features include:

- ▶ Four display pipelines for quad independent display
- ▶ Pipeline pixel depth 12 bits per each color
- ▶ HDMI version: 2.0b
 - Full backwards compatibility with HDMI 1.x
- ▶ DisplayPort (DP) version: 1.4a
 - Max resolution 7680 x 4320 at 60Hz (DSC)
- ▶ DVI D: Dual-link resolution of 2560 x 1600 x 24 bpp at 60 Hz refresh rate
- ▶ USB-C VirtualLink

Digital Audio

Digital audio features include:

- ▶ Support for HD Audio over PCI Express
- ▶ Data rates of 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz, 176 KHz, and 192 KHz with HDMI. Only 48 KHz supported over DP.
- ▶ Word sizes of 16-bit, 20-bit, and 24-bit

Video

The TU106 GPU introduces a new video engine, which is backward compatible with the video engine in earlier GPUs. The following video formats are supported:

► Decode

- H264 (MPEG4 AVC)
- H265 (HEVC)
- VP8/VP9
- MVC
- MV-HEVC
- MPEG2
- MPEG4 ASP
- VC1

► Encode

- H264 (MPEG4 AVC)
- H265 (HEVC)
- MVC
- MV-HEVC

A full range of resolutions are supported including 2160p, 1080p, 1080i, 720p, 480p, and 480i. The TU106 GPU provides hardware acceleration for the computationally intensive parts of video processing. The TU106 video processor provides improved video playback speeds via faster decode and transcode.

PCI Express 3.0

The TU106 GPU supports PCI Express 3.0 with 16 lanes of PCIe traffic for a peak bandwidth (counting both directions) of up to 16 gigabytes (GBps) per second.

GPIOs

The GPIO interface allows for basic control of devices on the graphics card.

Power Management Technologies

The TU106 GPU employs enhanced power management to achieve very low GPU power consumption. The following features are supported:

- ▶ ASLM and ASPM power management
- ▶ PLLs on lower voltage rails
- ▶ Dynamic memory termination
- ▶ Adaptive clocking
- ▶ Adaptive Power States

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2 SIGNAL DESCRIPTIONS

The signal description section contains definitions grouped under the following functions:

- ▶ Conventions
- ▶ PCI Express Interface
- ▶ Frame Buffer Memory Interface
- ▶ ROM Access Signals
- ▶ Digital Display Interface
- ▶ USB-C Display Interface
- ▶ I2C Interface
- ▶ Clock Reference Signals
- ▶ Power Rail Signals
- ▶ Test Signals
- ▶ Miscellaneous



Note: For detailed functionality and usage please refer to the D18 Hardware Design Guide (DG-08781-001).

Conventions

The following conventions are used to describe the signals for the TU106 GPU:

- Signal names listed in the ballout are written in bold *sans serif* font to distinguish them from other text. Single-ended active low signals are identified by an underscore and the letter “n” (**_N**) after the signal. For example, **PEX_TX1_N** indicates an active low signal. Signal names that do not appear in the ballout, but that are used for alternate interfaces are written in *sans serif* font without bold.
- Vendor signals appear as are standard for the vendor data sheets. For instance, $\overline{\text{CAS}}$ represents the active low Column Address Strobe signal in the frame buffer memory interface.
- I/O Type
The signal I/O state is represented as a code to indicate the operational characteristics of the signal. Table 2.1 lists the I/O codes used in the signal description tables.

Table 2.1 I/O Codes for Signal Descriptions

I/O Code	Meaning
I	Input signal
I/O	Input/output signal
O	Output signal
P, GND	Power/ground
B	Bidirectional signal
Z	Tri-state output
AB	Analog bidirectional signal
AI	Analog Input signal
AO	Analog Output signal

PCI Express Interface

The PCI Express Interface signals are given in Table 2.2.

Table 2.2 PCI Express Interface

Signal	I/O	Description
PEX_RX[15:0] PEX_RX[15:0]_N	I	PCI Express Receive Data Bus This is the high-speed unidirectional differential input data bus. The raw data rate is 2.5 Gbps per differential pair for PCI Express 1.1, 5.0 Gbps for PCI Express 2.0, 8.0 Gbps for PCI Express 3.0, including the symbol overhead for an embedded clock.

Table 2.2 PCI Express Interface

Signal	I/O	Description
PEX_TX[15:0] PEX_TX[15:0]_N	O	<p>PCI Express Transmit Data Bus</p> <p>This is the high-speed unidirectional differential output data bus. The raw data rate is 2.5 Gbps per differential pair for PCI Express 1.1, 5.0 Gbps for PCI Express 2.0, 8.0 Gbps for PCI Express 3.0, including the symbol overhead for an embedded clock.</p>
PEX_REFCLK PEX_REFCLK_N	I	<p>PCI Express Reference Clock</p> <p>The reference clock is a differential low-jitter input the GPU uses for its internal timing purposes. This input clock may be spread spectrum. Refer to the latest PCI Express specification for details on the reference clock spread spectrum.</p>
PEX_RST_N	I	<p>PCI Express Reset</p> <p>The PEX_RST_N signal indicates when the power supply is within its specified voltage tolerance and is stable. It goes inactive after a delay time from the power rails, achieving specified tolerance and power up. Refer to the latest PCI Express specification for details on the PCI Express reset.</p>
PEX_TERM_P	AB	<p>PCI Express Input/Output Termination Calibration</p> <p>The PEX_TERM_P signal provides the reference for the internal calibration of the PCI Express input/output termination. Use a pull-down to GND that is the same value as the desired termination.</p>
PEX_CLKREQ_N	O	<p>PCI Express Clock Request</p> <p>This active low signal is driven to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data.</p>
PEX_WAKE_N	I/O	<p>PCI Express Wake Request</p> <p>This active low signal is driven to request that the PCI Express interfaces wakes up from a lower power state.</p>

Frame Buffer Memory Interface

The TU106 frame buffer memory interface supports GDDR6 memories. Each memory partition has its own set of command signals. To see how the frame buffer control signals map to the memory command signals, refer to the D18 Hardware Design Guide (DG-08781-001).

Table 2.3 and Table 2.4 describes the data and clock signals for each memory partition.

Table 2.3 Frame Buffer Command Interface for GDDR6

Signal	I/O	Description
FBx_CMD[35:0] (x = A,B,C,D)	O	Command Address Bus Inversion (CABI_n) Used to reduce power consumption on the command Address bus.
	O	Reset (RESET_n) Asynchronous DRAM reset signal
	O	Memory Clock Enable (CKE_n) Enables the clock receivers for the target RAM.
	O	Command Address Inputs (CA[9:0]) The CA inputs receive DDR Command and Address inputs

Table 2.4 Frame Buffer Interface

Signal	I/O	Description
FBx_CLK[1:0] FBx_CLK[1:0]_N (x=A,B,C,D)	O	Memory Clock Signals These are separate sets of clock signals for each memory partition. For a further reduction in loading, there are two sets of clocks per partition. Each partition has two clock pairs that control either the most significant 32 bits or the least significant 32 bits per partition. The active low CA signals switch on the falling clock edge. The active high CA signals switch on the rising clock edge. The memory clock signals are as follows: FBx_CLK0 and FBx_CLK0_N → FBx_D[31:0] FBx_CLK1 and FBx_CLK1_N → FBx_D[63:32] x= A,B,C,D
FBx_D[63:0] (x=A,B,C,D)	I/O	Memory Data Bus These signals connect to data signals of the memory device for each 64-bit partition.

Table 2.4 Frame Buffer Interface

Signal	I/O	Description
FBx_DQM[7:0] (x=A,B,C,D)	I/O	Data Bus Inversion (DBI) FBx_DQM[7:0] signals are connected to DBI[7:0] signals of the memory. Used to reduce power consumption and VDD noise of the DRAM.
FBx_DQS_WP[7:0] (x=A,B,C,D)	I	Error Detection Code (EDC) FBx_DQS_WP[7:0] signals are connected to the EDC[7:0] signals of the memory. The CRC data is communicated on these signals
FBx_WCK01 FBx_WCK01_N FBx_WCK23 FBx_WCK23_N FBx_WCK45 FBx_WCK45_N FBx_WCK67 FBx_WCK67_N (x=A,B,C,D)	O	Reference for read and write data.
FBx_WCKB01 FBx_WCKB01_N FBx_WCKB23 FBx_WCKB23_N FBx_WCKB45 FBx_WCKB45_N FBx_WCKB67 FBx_WCKB67_N (x=A,B,C,D)	O	Reference for read and write data.
FB_CAL_PD_VDDQ FB_CAL_PU_GND	AO	Calibration Pull-Down/Pull-Up When the frame buffer bus operates in high-speed source-synchronous mode, several signals require dynamic calibration. Other slower signals are calibrated once on power-up. FB_CAL_PD_VDDQ and FB_CAL_PU_GND are used to compute the drive strength of the frame buffer pads. FB_CAL_PD_VDDQ connects to FBVDDQ and is pulled up through a precision resistor. FB_CAL_PU_GND is pulled down to GND through a precision resistor.

Table 2.4 Frame Buffer Interface

Signal	I/O	Description
FB_CAL_TERM_GND	AO	Termination Calibration Signal When the frame buffer bus operates in high-speed source-synchronous mode, it may use internal termination provided by the GPU. This signal provides the calibration for the internal termination. It should be tied to GND through a precision resistor that is the same value as the desired termination.
FB_VREF	I	Frame Buffer Voltage Reference Sets switching threshold for inputs on the frame buffer when the frame buffer input pads are set to input mode.
FBVDDQ_SENSE	AO	Frame Buffer Power Rail Sense Signal

ROM Access Signals

Table 2.5 Serial ROM Access Signals

Signal	I/O	Description
ROM_SCLK	O	Serial ROM Clock ROM_SCLK supplies the clock signal for accessing serial ROM data.
ROM_CS_N	O	Chip Select.
ROM_SI	O	Serial Output ROM_SI supplies the data signal to the SROM_SI serial ROM signal.
ROM_SO	I	Serial Input ROM_SO accepts the data signal input from SROM_SO of the serial ROM as input.

Digital Display Interface

The TU106 GPU enables Links A, B, C, D, E, and F to support DisplayPort. Links can also be configured to support DVI and HDMI.

Table 2.6 Digital Display Interface Signals, Links A & B

Signal	I/O	Description
IFPA_AUX_SCL/ IFPA_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link A)
IFPA_L0/IFPA_L0_N	O	DisplayPort Main Link Lane 0 (Link A)
IFPA_L1/IFPA_L1_N	O	DisplayPort Main Link Lane 1 (Link A)
IFPA_L2/IFPA_L2_N	O	DisplayPort Main Link Lane 2 (Link A)
IFPA_L3/IFPA_L3_N	O	DisplayPort Main Link Lane 3 (Link A)
IFPB_AUX_SCL IFPB_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link B)
IFPB_L0/IFPB_L0_N	O	DisplayPort Main Link Lane 0 (Link B)
IFPB_L1/IFPB_L1_N	O	DisplayPort Main Link Lane 1 (Link B)
IFPB_L2/IFPB_L2_N	O	DisplayPort Main Link Lane 2 (Link B)
IFPB_L3/IFPB_L3_N	O	DisplayPort Main Link Lane 3 (Link B)
IFPAB_RSET	I/O	Set Reference Current Generate a reference current through connecting an external resistor to this signal.

Table 2.7 Digital Display Interface Signals, Links C, D, E, and F

Signal	I/O	Description
IFPC_AUX_SCL / IFPC_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link C)
IFPC_L0/IFPC_L0_N	O	DisplayPort Main Link Lane 0 (Link C)
IFPC_L1/IFPC_L1_N	O	DisplayPort Main Link Lane 1 (Link C)
IFPC_L2/IFPC_L2_N	O	DisplayPort Main Link Lane 2 (Link C)
IFPC_L3/IFPC_L3_N	O	DisplayPort Main Link Lane 3 (Link C)
IFPCD_RSET	I/O	Set Reference Current Generates a reference current through connecting an external resistor to this signal
IFPD_AUX_SCL/ IFPD_AUX_SDA_N	I/O	DisplayPort Auxiliary Channel (Link D)
IFPD_L0/IFPD_L0_N	O	DisplayPort Main Link Lane 0 (Link D)
IFPD_L1/IFPD_L1_N	O	DisplayPort Main Link Lane 1 (Link D)

Table 2.7 Digital Display Interface Signals, Links C, D, E, and F

Signal	I/O	Description
IFPD_L2/IFPD_L2_N	O	DisplayPort Main Link Lane 2 (Link D)
IFPD_L3/IFPD_L3_N	O	DisplayPort Main Link Lane 3 (Link D)
IFPE_AUX_SCL/ IFPE_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link E)
IFPE_L0/IFPE_L0_N	O	DisplayPort Main Link Lane 0 (Link E)
IFPE_L1/IFPE_L1_N	O	DisplayPort Main Link Lane 1 (Link E)
IFPE_L2/IFPE_L2_N	O	DisplayPort Main Link Lane 2 (Link E)
IFPE_L3/IFPE_L3_N	O	DisplayPort Main Link Lane 3 (Link E)
IFPE_RSET	I/O	Set Reference Current Generates a reference current through connecting an external resistor to this signal
IFPF_AUX_SCL/ IFPF_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link F)
IFPF_L0/IFPF_L0_N	O	DisplayPort Main Link Lane 0 (Link F);
IFPF_L1/IFPF_L1_N	O	DisplayPort Main Link Lane 1 (Link F)
IFPF_L2/IFPF_L2_N	O	DisplayPort Main Link Lane 2 (Link F)
IFPF_L3/IFPF_L3_N	O	DisplayPort Main Link Lane 3 (Link F)

USB-C Display Interface

Link F and IFPB_AUX support USB-C, as described in Table 2.8.

Table 2.8 USB Interface Signals

Signal	I/O	Description
IFPF_AUX_SCL/ IFPF_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane/USB-C Sideband signals SBU1/SBU2
IFPB_AUX_SCL/ IFPB_AUX_SDA_N	I/O	Master I2C to USB-C PPC
IFPF_L0/IFPF_L0_N	O	USB3 RX+ / USB3 RX- Note: This signal pad is used as USB3 RX+ / USB3 RX- for USB-C interface
IFPF_L1/IFPF_L1_N	O	USB3 TX+ / USB3 TX- Note: This signal pad is used as USB3 TX+ / USB3 TX- for USB-C interface
IFPF_L2/IFPF_L2_N	O	USB3 TX+ / USB3 TX- Note: This signal pad is used as USB3 TX+ / USB3 TX- for USB-C interface
IFPF_L3/IFPF_L3_N	O	USB3 RX+ / USB3 RX- Note: This signal pad is used as USB3 RX+ / USB3 RX- for USB-C interface

Table 2.8 USB Interface Signals

Signal	I/O	Description
USB_L0/USB_LO_N	O	USB3 TX+ or USB2+/USB3 TX- or USB2- Note: This signal pad is used as USB3 TX+/USB3 TX- for USB-C interface
USB_L1/USB_L1_N	O	USB3 RX+ or USB2+/USB3 RX- or USB2- Note: This signal pad is used as USB3 RX+/USB3 RX- for USB-C interface
USB_RBIAS	AI	USB Reference Resistor
USB_SCL	I/O	Slave I2C Clock interface for controlling integrated DP/USB cross-connect
USB_SDA	I/O	Slave I2C Data interface for controlling integrated DP/USB cross-connect
USB_TERMPO	AI	USB PLL Reference Resistor 0
USB_TERMPP1	AI	USB PLL Reference Resistor 1

I2C Interface

Table 2.9 I2C Interface Signals

Signal	I/O	Description
I2CB_SCL I2CB_SDA	I/O	If not used for any external Bus, this bus may be used for embedded devices.
I2CC_SCL I2CC_SDA	I/O	Restricted to embedded devices such as voltage regulators and power monitors.
I2CS_SCL I2CS_SDA	I/O	Slave I2C-Compatible Bus Signal.

Clock Reference Signals

Table 2.10 Clock Reference Signals

Signal	I/O	Description
XTAL_IN	I	A series resonant crystal is connected between these two points to provide the reference clock for the internal clock synthesizers. Alternately, an external LVTTTL clock oscillator output may be driven in XTAL_IN, leaving XTAL_OUT unconnected.
XTAL_OUT	O	
XTAL_OUTBUFF	O	XTAL_OUTBUFF is a buffered version of the XTAL_IN/XTAL_OUT.

Power Rail Signals

IFP Power Rail Signals

Table 2.11 IFP Power Rail Signals

Signal	I/O	Description
IFP_IOVDD	P	1.0V supply for integrated Digital Display I/O Power Rails for all IFP links.
IFPAB_PLLVDD	P	1.8V supply for integrated Digital Display PLL Power Rails for the IFP-A and IFP-B links.
IFPCD_PLLVDD	P	1.8V supply for Integrated Digital Display PLL Power Rails for the IFP-C and IFP-D links.
IFPE_PLLVDD	P	1.8V supply for Integrated Digital Display PLL Power Rails for the IFP-E link.

PEX Power Rail Signals

Table 2.12 PEX Power Rail Signals

Signal	I/O	Description
PEX_CVDD / PEX_DVDD	P	1.0V supply for PCIe interface/PLL digital power rail
PEX_HVDD	P	1.8V supply for PCIe interface/PLL analog power rail
PEX_PLL_HVDD	P	1.8V supply for the PEX PLL

Frame Buffer Power Rail Signals

Table 2.13 FrameBuffer Power Rail Signals

Signal	I/O	Description
FB_REFPLL_AVDDx (x=0,1)	P	1.8V supply for Frame Buffer Digital Power Rails
FBVDDQ	P	Frame Buffer Power Rail
FBVDDQ_SENSE	O	Frame Buffer Power Rail Sense Signal
FBx_PLL_AVDD (x=A,B,C,D)	P	1.8V supply for Frame Buffer PLL Analog Power Rails

General Power Rail Signals

Table 2.14 General Power Rail Signals

Signal	I/O	Description
GPCPLL_AVDDx (x=0,1)	P	1.8V supply for Analog Power Rails for GPCs
SP_PLLVDD	P	1.8V supply for Core Clock PLL Analog Power Rail
VDD	P	Core Power Rail. Connect to NVVDD power supply.
1V8_AON	P	1.8V Always On Power Rail
VID_PLLVDD	P	1.8V supply for Video Pixel Clock PLL Analog power rail
XS_PLLVDD	P	1.8V supply for Core PLL Analog rail

USB Power Rail Signals

Table 2.15 USB Power Rail Signals

Signal	I/O	Description
USB_DVDD	P	USB 1.0V Core Power Rail
USB_HVDD	P	USB 1.8V Voltage Power Rail
USB_PLL_HVDD	P	USB 1.8V PLL Power Rail
USB_VDDP	P	USB 3.3V Analog Supply



Note: For detailed functionality and usage please refer to the D18 Hardware Design Guide (DG-08781-001).

Test Signals

Table 2.16 Test Signals

Signals	I/O	Description
JTAG_TCK JTAG_TDI JTAG_TDO JTAG_TMS	I I Z I	JTAG Test Signals
NVJTAG_SEL	I	JTAG Select

Miscellaneous

Table 2.17 Miscellaneous Signals

Signal	I/O	Description
STRAP[5:0]	I	Strap Signals
THERMDP THERMDN	I O	Thermal Monitor Signals Leave floating and unconnected.
ADC_IN / ADC_IN_N	I	External current sense for power monitoring
GPIO [30:0]	I	General Purpose I/O
BUFRST_N	O	Behaves as a buffered copy of the system PEX_RST* signal in all operating modes when 1V8 is present . Tri-state when 1V8 is not present .
FP_FUSE_SRC	I	TBD

3 ELECTRICAL SPECIFICATIONS

This section provides absolute maximum ratings and operating conditions for the TU106 GPU.

For more information about the core graphics voltage (NVVDD), frame buffer clock frequency (MCLK), and core clock frequency (GPCCLK) values and electrical and thermal design guidelines for this product, refer to the Product Specification.

The frame buffer memory clock, MCLK, is defined as an actual clock output (not as a data rate). The NVIDIA® GPU Boost™ technology manages the clocks dynamically.

Table 3.1 lists the absolute maximum ratings of the power rails.

Table 3.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max. ¹	Units	Notes
FBVDDQ	Frame buffer power rail	-0.3	1.98	V	
FBx_PLL_AVDD (x=A,B,C,D)	Frame buffer PLL analog power rail	-0.3	1.854	V	
GPCPLL_AVDD0 GPCPLL_AVDD1	Core PLL Analog Rails	-0.3	1.854	V	
IFP_IOVDD	Integrated Digital Display I/O power rails	-0.3	1.1	V	
IFPAB_PLLVDD	Integrated Digital Display PLL power rails	-0.3	1.854	V	
IFPCD_PLLVDD	Integrated Digital Display PLL power rails	-0.3	1.854	V	

Table 3.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max. ¹	Units	Notes
IFPE_PLLVDD	Integrated Digital Display PLL power rails	-0.3	1.854	V	
PEX_DVDD/ PEX_CVDD	PCIe interface/PLL digital power rail	-0.3	1.1	V	
PEX_HVDD	PCIe interface/PLL analog power rail	-0.3	1.854	V	
PEX_PLL_HVDD	PCIe interface PLL supply power rail	-0.3	1.854	V	
SP_PLLVDD	Core clock PLL analog power rail	-0.3	1.854	V	
USB_VDDP	USB analog supply	-0.3	3.63	V	
USB_DVDD	USB analog supply	-0.3	1.1	V	
USB_HVDD	USB analog supply	-0.3	1.854	V	
USB_PLL_HVDD	USB analog PLL supply	-0.3	1.854	V	
VDD	Core (NVVDD) power rail	-0.3	TBD	V	
1V8_AON	1.8 V power rail	-0.3	1.854	V	
VID_PLLVDD	Thermal controller and Video pixel clock PLL analog power rail	-0.3	1.854	V	
XS_PLLVDD	Core PLL Analog Rails	-0.3	1.854	V	
T _j	Die junction temperature	Refer to the Product Specification		°C	

Notes:

1. Stress greater than those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



Note: Voltage settings may vary with the reference design; please refer to the specific reference design to get the required values.

Table 3.2 lists the operating conditions of the clock and power rail signals.

Table 3.2 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max. ¹	Units	Notes
FBVDDQ	Frame buffer power rail		1.35		V	Note 2
FBx_PLL_AVDD (x=A,B,C,D)	Frame buffer PLL analog power rail	1.746	1.800	1.854	V	
GPCPLL_AVDD0 GPCPLL_AVDD1	Core PLL Analog Rails	1.746	1.800	1.854	V	
IFP_IOVDD	Integrated Digital Display I/O power rails	0.97	1.00	1.03	V	
IFPAB_PLLVDD	Integrated Digital Display PLL power rails	1.746	1.800	1.854	V	
IFPCD_PLLVDD	Integrated Digital Display PLL power rails	1.746	1.800	1.854	V	
IFPE_PLLVDD	Integrated Digital Display PLL power rails	1.746	1.800	1.854	V	
PEX_DVDD/ PEX_CVDD	PCIe interface/PLL digital power rail	0.97	1.00	1.03	V	
PEX_HVDD	PCIe interface/PLL analog power rail	1.746	1.800	1.854	V	
PEX_PLL_HVDD	PCIe interface PLL supply power rail	1.746	1.800	1.854	V	
SP_PLLVDD	Core clock PLL analog power rail	1.746	1.800	1.854	V	
USB_VDDP	USB analog supply	3.135	3.3	3.456	V	
USB_DVDD	USB analog supply	0.97	1.0	1.03	V	
USB_HVDD	USB analog supply	1.746	1.800	1.854	V	
USB_PLL_HVDD	USB analog PLL supply	1.746	1.800	1.854	V	
VDD	Core (NVVDD) power rail	NVVDD-2.5%	NVVDD	NVVDD+2.5%	V	
1V8_AON	1.8 V power rail	1.746	1.800	1.854	V	
VID_PLLVDD	Thermal controller and Video pixel clock PLL analog power rail	1.746	1.800	1.854	V	
XS_PLLVDD	Core PLL Analog Rails	1.746	1.800	1.854	V	
T _j	Die junction temperature	0	Refer to the Product Specification		°C	See Note 3.

Notes:

1 This specification defines the goals for the DC supply at **VDD**. Short pulses due to switching noise on **VDD** may exceed this limit.

2 Min/Typ/Max/ should meet memory vendor spec which can vary.

3 T_j is the maximum die temperature at which the GPU can operate at its maximum clock frequencies, as defined in the NVIDIA Product Specification.

Table 3.3 GPIO Electrical Specifications

Voh,Vih/min	Voh,Vih/max	Vol,Vil/min	Vol,Vil/max	Vi_mid max	Vi_mid min
1.50V	1.854V	0V	0.3V	1.3V	0.5V

Jane Li NVIDIA Confidential
Gigabyte Desktop 2018-08-15 19:04:49

4 MASTER SIGNAL LIST

This chapter contains the master signal list for the TU106 GPU.

Table 4.1 Master Signal List

Master Signal List for TU106 GPU					
IOB Key: B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z= Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		Reset & Initial Value Key: Z= Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
I2C					
I2CB_SCL	O			+1.8V_AON	
I2CB_SDA	B			+1.8V_AON	
I2CC_SCL	O			+1.8V_AON	
I2CC_SDA	B			+1.8V_AON	
I2CS_SCL	O			+1.8V_AON	
I2CS_SDA	B			+1.8V_AON	
IFP					
IFPA_L0_N	O				
IFPA_L0	O				
IFPA_L1_N	O				
IFPA_L1	O				
IFPA_L2_N	O				
IFPA_L2	O				
IFPA_L3_N	O				
IFPA_L3	O				
IFPB_L0_N	O				

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Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
IFPB_L0	O				
IFPB_L1_N	O				
IFPB_L1	O				
IFPB_L2_N	O				
IFPB_L2	O				
IFPB_L3_N	O				
IFPB_L3	O				
IFPC_L0_N	O				
IFPC_L0	O				
IFPC_L1_N	O				
IFPC_L1	O				
IFPC_L2_N	O				
IFPC_L2	O				
IFPC_L3_N	O				
IFPC_L3	O				
IFPD_L0_N	O				
IFPD_L0	O				
IFPD_L1_N	O				
IFPD_L1	O				
IFPD_L2_N	O				
IFPD_L2	O				
IFPD_L3_N	O				
IFPD_L3	O				
IFPE_L0_N	O				
IFPE_L0	O				
IFPE_L1_N	O				
IFPE_L1	O				
IFPE_L2_N	O				
IFPE_L2	O				
IFPE_L3_N	O				
IFPE_L3	O				
IFPF_L0_N	O				
IFPF_L0	O				
IFPF_L1_N	O				
IFPF_L1	O				
IFPF_L2_N	O				
IFPF_L2	O				
IFPF_L3_N	O				
IFPF_L3	O				

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Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
IFPAB_RSET	AI				
IFPCD_RSET	AI				
IFPE_RSET	AI				
IFPA_AUX_SCL	O				
IFPA_AUX_SDA_N	B				
IFPB_AUX_SCL	O				
IFPB_AUX_SDA_N	B				
IFPC_AUX_SCL	O				
IFPC_AUX_SDA_N	B				
IFPD_AUX_SCL	O				
IFPD_AUX_SDA_N	B				
IFPE_AUX_SCL	O				
IFPE_AUX_SDA_N	B				
IFPF_AUX_SCL	O				
IFPF_AUX_SDA_N	B				
IFPAB_PLLVDD	P				
IFP_IOVDD	P				
IFPCD_PLLVDD	P				
IFPE_PLLVDD	P				
IFPE_PLLVDD	P				
Frame Buffer A					
FBA_D[63:0]	B			FBVDDQ	
FBA_DQM[7:0]	B			FBVDDQ	
FBA_DQS_WP[7:0]	I			FBVDDQ	
FBA_WCK01	O			FBVDDQ	
FBA_WCK01_N	O			FBVDDQ	
FBA_WCKB01	O			FBVDDQ	
FBA_WCKB01_N	O			FBVDDQ	
FBA_WCK23	O			FBVDDQ	
FBA_WCK23_N	O			FBVDDQ	
FBA_WCKB23	O			FBVDDQ	
FBA_WCKB23_N	O			FBVDDQ	
FBA_WCK45	O			FBVDDQ	
FBA_WCK45_N	O			FBVDDQ	
FBA_WCKB45	O			FBVDDQ	
FBA_WCKB45_N	O			FBVDDQ	
FBA_WCK67	O			FBVDDQ	
FBA_WCK67_N	O			FBVDDQ	
FBA_WCKB67	O			FBVDDQ	

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Master Signal List for TU106 GPU					
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Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
FBA_WCKB67_N	O			FBVDDQ	
FBA_CMD[35:0]	O			FBVDDQ	
FBA_CLK0	O			FBVDDQ	
FBA_CLK0_N	O			FBVDDQ	
FBA_CLK1	O			FBVDDQ	
FBA_CLK1_N	O			FBVDDQ	
Frame Buffer B					
FBB_D[63:0]	B			FBVDDQ	
FBB_DQM[7:0]	B			FBVDDQ	
FBB_DQS_WP[7:0]	I			FBVDDQ	
FBB_WCK01	O			FBVDDQ	
FBB_WCK01_N	O			FBVDDQ	
FBB_WCKB01	O			FBVDDQ	
FBB_WCKB01_N	O			FBVDDQ	
FBB_WCK23	O			FBVDDQ	
FBB_WCK23_N	O			FBVDDQ	
FBB_WCKB23	O			FBVDDQ	
FBB_WCKB23_N	O			FBVDDQ	
FBB_WCK45	O			FBVDDQ	
FBB_WCK45_N	O			FBVDDQ	
FBB_WCKB45	O			FBVDDQ	
FBB_WCKB45_N	O			FBVDDQ	
FBB_WCK67	O			FBVDDQ	
FBB_WCK67_N	O			FBVDDQ	
FBB_WCKB67	O			FBVDDQ	
FBB_WCKB67_N	O			FBVDDQ	
FBB_CMD[35:0]	O			FBVDDQ	
FBB_CLK0	O			FBVDDQ	
FBB_CLK0_N	O			FBVDDQ	
FBB_CLK1	O			FBVDDQ	
FBB_CLK1_N	O			FBVDDQ	
Frame Buffer C					
FBC_D[63:0]	B			FBVDDQ	
FBC_DQM[7:0]	B			FBVDDQ	
FBC_DQS_WP[7:0]	I			FBVDDQ	
FBC_WCK01	O			FBVDDQ	
FBC_WCK01_N	O			FBVDDQ	
FBC_WCKB01	O			FBVDDQ	
FBC_WCKB01_N	O			FBVDDQ	

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Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
FBC_WCK23	O			FBVDDQ	
FBC_WCK23_N	O			FBVDDQ	
FBC_WCKB23	O			FBVDDQ	
FBC_WCKB23_N	O			FBVDDQ	
FBC_WCK45	O			FBVDDQ	
FBC_WCK45_N	O			FBVDDQ	
FBC_WCKB45	O			FBVDDQ	
FBC_WCKB45_N	O			FBVDDQ	
FBC_WCK67	O			FBVDDQ	
FBC_WCK67_N	O			FBVDDQ	
FBC_WCKB67	O			FBVDDQ	
FBC_WCKB67_N	O			FBVDDQ	
FBC_CMD[35:0]	O			FBVDDQ	
FBC_CLK0	O			FBVDDQ	
FBC_CLK0_N	O			FBVDDQ	
FBC_CLK1	O			FBVDDQ	
FBC_CLK1_N	O			FBVDDQ	
Frame Buffer D					
FBD_D[63:0]	B			FBVDDQ	
FBD_DQM[7:0]	B			FBVDDQ	
FBD_DQS_WP[7:0]	I			FBVDDQ	
FBD_WCK01	O			FBVDDQ	
FBD_WCK01_N	O			FBVDDQ	
FBD_WCKB01	O			FBVDDQ	
FBD_WCKB01_N	O			FBVDDQ	
FBD_WCK23	O			FBVDDQ	
FBD_WCK23_N	O			FBVDDQ	
FBD_WCKB23	O			FBVDDQ	
FBD_WCKB23_N	O			FBVDDQ	
FBD_WCK45	O			FBVDDQ	
FBD_WCK45_N	O			FBVDDQ	
FBD_WCKB45	O			FBVDDQ	
FBD_WCKB45_N	O			FBVDDQ	
FBD_WCK67	O			FBVDDQ	
FBD_WCK67_N	O			FBVDDQ	
FBD_WCKB67	O			FBVDDQ	
FBD_WCKB67_N	O			FBVDDQ	
FBD_CMD[35:0]	O			FBVDDQ	
FBD_CLK0	O			FBVDDQ	

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Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
FBD_CLK0_N	O			FBVDDQ	
FBD_CLK1	O			FBVDDQ	
FBD_CLK1_N	O			FBVDDQ	
Mem Miscellaneous Signals					
FB_CAL_VDDQ	AI			FBVDDQ	
FB_CAL_GND	AI			FBVDDQ	
FB_CAL_TERM	AI			FBVDDQ	
FBVDDQ	P				
FB_VREF	AI			FBVDDQ	
FBVDDQ_SENSE	AO				
PCI Express					
PEX_RX[15:0]	I				
PEX_RX[15:0]_N	I				
PEX_TX[15:0]	O				
PEX_TX[15:0]_N	O				
PEX_REFCLK	I				
PEX_REFCLK_N	I				
PEX_CLKREQ_N	O			+1.8V_AON	
PEX_RST_N	I			+1.8V_AON	
PEX_HVDD	P				
PEX_DVDD	P				
PEX_PLL_HVDD	P				
PEX_DVDD	P				
PEX_WAKE_N	O				
JTAG Interface					
JTAG_TMS	I			+1.8V_AON	
JTAG_TCK	I			+1.8V_AON	
JTAG_TRST_N	I			+1.8V_AON	
JTAG_TDI	I			+1.8V_AON	
JTAG_TDO	O			+1.8V_AON	
NVJTAG_SEL	I			+1.8V_AON	
Other Clocks					
ROM_CS_N	O			+1.8V_AON	
ROM_SCLK	B			+1.8V_AON	
ROM_SI	B			+1.8V_AON	
ROM_SO	B			+1.8V_AON	
XTAL_OUTBUFF	O			+1.8V_AON	
EXT_REFCLK_FL	I			+1.8V_AON	
XTAL_IN	AI			+1.8V_AON	

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Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
XTAL_OUT	AO			+1.8V_AON	
GPIO					
GPIO0	B			+1.8V_AON	
GPIO1	B			+1.8V_AON	
GPIO2	B			+1.8V_AON	
GPIO3	B			+1.8V_AON	
GPIO4	B			+1.8V_AON	
GPIO5	B			+1.8V_AON	
GPIO6	B			+1.8V_AON	
GPIO7	B			+1.8V_AON	
GPIO8	B			+1.8V_AON	
GPIO9	B			+1.8V_AON	
GPIO10	B			+1.8V_AON	
GPIO11	B			+1.8V_AON	
GPIO12	B			+1.8V_AON	
GPIO13	B			+1.8V_AON	
GPIO14	B			+1.8V_AON	
GPIO15	B			+1.8V_AON	
GPIO16	B			+1.8V_AON	
GPIO17	B			+1.8V_AON	
GPIO18	B			+1.8V_AON	
GPIO19	B			+1.8V_AON	
GPIO20	B			+1.8V_AON	
GPIO21	B			+1.8V_AON	
GPIO22	B			+1.8V_AON	
GPIO23	B			+1.8V_AON	
GPIO24	B			+1.8V_AON	
GPIO25	B			+1.8V_AON	
GPIO26	B			+1.8V_AON	
GPIO27	B			+1.8V_AON	
GPIO28	B			+1.8V_AON	
GPIO29	B			+1.8V_AON	
GPIO30	B			+1.8V_AON	
System Interfaces					
BUFRST_N	O			+1.8V_AON	
STRAP0	I			+1.8V_AON	
STRAP1	I			+1.8V_AON	
STRAP2	I			+1.8V_AON	
STRAP3	I			+1.8V_AON	

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Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
STRAP4	I			+1.8V_AON	
STRAP5	I			+1.8V_AON	
OVERT	B			+1.8V_AON	
THERMDP	AO				
THERMDN	AO				
TS_VREF	AI				
GND_SENSE	AO				
VDD_SENSE	AO				
ADC_IN	AI				
ADC_IN_N	AI				
Power Direct Drills - IO voltage Rails & Core Voltages					
VDD	P				
GND	P				
1V8_AON	P			+1.8V_AON	
PLLs					
XS_PLLVDD	P				
FB_REFPLL_AVDD0	P				
FB_REFPLL_AVDD1	P				
VID_PLLVDD	P				
SP_PLLVDD	P				
XS_PLLVDD	P				
GPCPLL_AVDD0	P				
GPCPLL_AVDD1	P				
FBA_PLL_AVDD	P				
FBB_PLL_AVDD	P				
FBC_PLL_AVDD	P				
FBD_PLL_AVDD	P				
USB					
USB_DVDD	P				
USB_HVDD	P				
USB_L0	O				
USB_L0_N	O				
USB_L1	O				
USB_L1_N	O				
USB_PLL_HVDD	P				
USB_RBIAS	AI				
USB_SCL	O				
USB_SDA	B				
USB_TERMPO	AI				

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Signal Name	IOB	Reset Value	Initial Value	Drive	Notes
USB_TERM1	AI				
USB_VDDP	P				

5 PACKAGE DESCRIPTIONS

Mechanical Specifications

This section provides the following mechanical specifications and characteristics for the TU106 GPU.

Figure 5.1 shows the package specifications for the TU106 GPU in a 37.5 mm x 37.5 mm FCBGA package with 2228 balls. [Table 5.1](#) provides the package measurements.

GB4B-256 37.5 mm x 37.5 mm Package Specification



Note: Drawings are not to scale.

Figure 5.1 shows the GB4B-256 package.

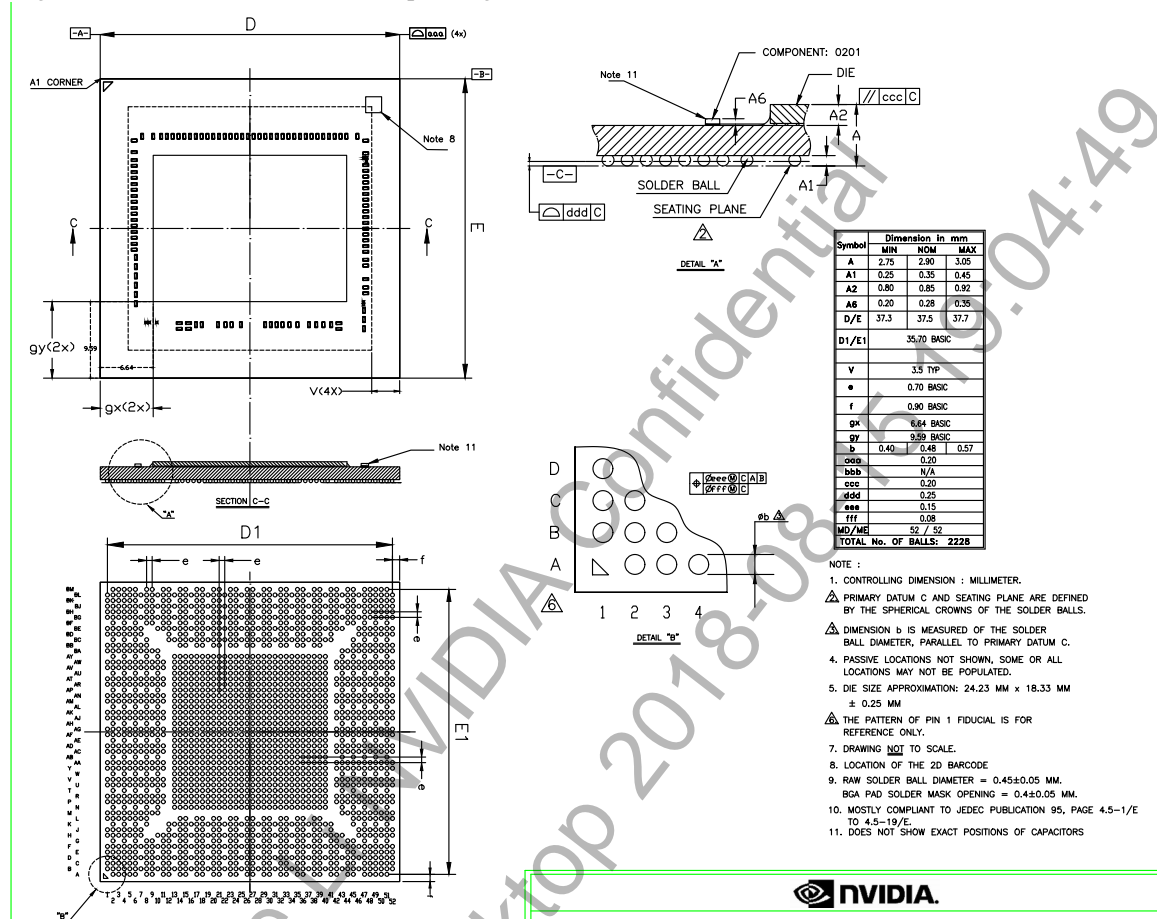


Figure 5.1 GB4B-256 37.5 mm x 37.5 mm Package Specification

Mechanical and Environmental Specifications

Table 5.1 describes the mechanical characteristics for the packages.

Table 5.1 Mechanical Characteristics

Symbol	Parameter	Min.	Nominal	Max.	Units	Notes
P_{cont}	Maximum allowable pressure during PCA, system assembly and operation.	-	≤ 60	≤ 80 (die edge)	psi	1
T_{pkg}	Maximum allowable package temperature during device operation	-	-	$\leq TBD$	$^{\circ}C$	2
T_{reflow}	Maximum package temperature during surface mount to printed circuit board	Refer to NVIDIA specifications 630-0011-001				
ϵ_{max}	Maximum allowable strain during PCA, system assembly or operation			≤ 500	μ strains	3

Notes:

- 1) This specification is based on the following conditions:
 - a. This specification is based on solder ball deformation and die chips and cracks. Additional requirements may be needed to meet the thermal performance and/or long term reliability as to specific application,
 - b. When a compliant thermal interface is used between die and heat sink, the bond line thickness must have less than 20% in variation.
 - c. The pressure should be measured on the top of the die surface by an instrument equipped pressure sensors. See details in "GPU Load Distribution Measurement Application Note".
 - d. Nominal pressure is the total force divided by the die surface area. Since the pressure may have variations across the whole surfaces. The following additional requirement is applied:
 - i. The pressure has to be measured from the top of the die surface with a grid resolution of $1 \times 1 \text{mm}^2$ for the pressure sensor.
 - e. Both nominal and maximum pressure requirement must be met.
- 2) Maximum package temperature allowed. It includes device case and/or junction temperature.
- 3) Strain measurement shall follow IPC-9704, particularly on following items:
 - a. The strain shall be measured on the top side of PCB close to the four corners of the package. A rigid PCB is assumed.
 - b. For generic application, the max. allowable strain must be no more than 500μ strains for a board thickness from 1.0 to 3.2mm. A separate requirement may be specified and the qualification test should be performed if
 - i. A sensitive PCB laminate and build up structure is used where the pad cratering occurs at a PCB strain of 500μ strains or below.
 - ii. A weak surface finish of PCB is used where cracked solder joint has been observed at a PCB strain of 500μ strains or below.
 - iii. The strain rate is too high ($.5000 \mu$ strains/second) during the PCA operations.
 - c. For PCB thickness less than 1,0mm, the max. allowable strain shall follow IPC 9704.

Table 5.2 contains information regarding environmental specifications and conditions.

Table 5.2 Environmental Specifications

Specifications	Conditions
Storage temperature	-40 °C to 125 °C
Operating humidity	5% to 90% RH
Storage humidity	5% to 95% RH

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6 BALL INFORMATION

The TU106 GPU uses the GB4B-256 package. The GB4B-256 ball list and ball map are included in this chapter.

GB4B-256 Ball List (Sorted by Ball Name)

Table 6.1 GB4B-256 Ball List

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
1V8_AON	BA10	FBA_CMD26	AJ49	FBA_D28	AA47
1V8_AON	BB14	FBA_CMD27	AJ52	FBA_D29	AA46
1V8_AON	BC14	FBA_CMD28	AJ51	FBA_D3	U49
ADC_IN	BJ9	FBA_CMD29	AJ50	FBA_D30	AA45
ADC_IN*	BJ11	FBA_CMD3	AA52	FBA_D31	Y44
BUFRST*	BF9	FBA_CMD30	AG50	FBA_D32	AW51
EXT_REFCLK_FL	BJ6	FBA_CMD31	AG51	FBA_D33	BA52
EXT_REFCLK_SLI	AM2	FBA_CMD32	AF49	FBA_D34	AW50
FB_CAL_PD_VDDQ	R44	FBA_CMD33	AG52	FBA_D35	BA51
FB_CAL_PU_GND	P44	FBA_CMD34	Y50	FBA_D36	BA50
FB_CAL_TERM_GND	R45	FBA_CMD35	AR50	FBA_D37	BB50
FB_REFPLL_AVDD0	AF42	FBA_CMD4	AA51	FBA_D38	BA49
FB_REFPLL_AVDD1	L29	FBA_CMD5	AA50	FBA_D39	AW49
FB_VREF	P45	FBA_CMD6	AC50	FBA_D4	R51
FBA_CLK0	AG45	FBA_CMD7	AC51	FBA_D40	AV48
FBA_CLK0*	AG46	FBA_CMD8	AC52	FBA_D41	AT49
FBA_CLK1	AK46	FBA_CMD9	AC49	FBA_D42	AT47
FBA_CLK1*	AK45	FBA_D0	U51	FBA_D43	AT48
FBA_CMD0	Y51	FBA_D1	U48	FBA_D44	AT46
FBA_CMD1	Y52	FBA_D10	Y47	FBA_D45	AV51
FBA_CMD10	AD52	FBA_D11	Y46	FBA_D46	AV52
FBA_CMD11	AD51	FBA_D12	V50	FBA_D47	AV49
FBA_CMD12	AD50	FBA_D13	V47	FBA_D48	AJ48
FBA_CMD13	AF50	FBA_D14	U52	FBA_D49	AJ46
FBA_CMD14	AF51	FBA_D15	V51	FBA_D5	R50
FBA_CMD15	AF52	FBA_D16	AJ44	FBA_D50	AJ47
FBA_CMD16	AN50	FBA_D17	AG48	FBA_D51	AK49
FBA_CMD17	AN51	FBA_D18	AJ45	FBA_D52	AM47
FBA_CMD18	AN52	FBA_D19	AG49	FBA_D53	AM46
FBA_CMD19	AM49	FBA_D2	U50	FBA_D54	AN48
FBA_CMD2	Y49	FBA_D20	AF46	FBA_D55	AN49
FBA_CMD20	AM52	FBA_D21	AF47	FBA_D56	AM44
FBA_CMD21	AM51	FBA_D22	AF48	FBA_D57	AM45
FBA_CMD22	AM50	FBA_D23	AD47	FBA_D58	AN45
FBA_CMD23	AK50	FBA_D24	AD49	FBA_D59	AN46
FBA_CMD24	AK51	FBA_D25	AD48	FBA_D6	R47
FBA_CMD25	AK52	FBA_D26	AC46	FBA_D60	AR48
		FBA_D27	AC47	FBA_D61	AN47

Ball Name	Ball #
FBA_D62	AR47
FBA_D63	AR46
FBA_D7	U46
FBA_D8	V46
FBA_D9	Y45
FBA_DBG_RFU1	AA44
FBA_DBG_RFU2	AN44
FBA_DQM0	U47
FBA_DQM1	Y48
FBA_DQM2	AG47
FBA_DQM3	AC48
FBA_DQM4	BB51
FBA_DQM5	AV50
FBA_DQM6	AM48
FBA_DQM7	AR49
FBA_DQS_WP0	R48
FBA_DQS_WP1	V48
FBA_DQS_WP2	AF44
FBA_DQS_WP3	AA48
FBA_DQS_WP4	BB52
FBA_DQS_WP5	AT50
FBA_DQS_WP6	AK48
FBA_DQS_WP7	AR51
FBA_PLL_AVDD	AN42
FBA_WCK01	U45
FBA_WCK01*	U44
FBA_WCK23	AC45
FBA_WCK23*	AC44
FBA_WCK45	AV47
FBA_WCK45*	AV46
FBA_WCK67	AR45
FBA_WCK67*	AR44
FBA_WCKB01	V45
FBA_WCKB01*	V44
FBA_WCKB23	AD46
FBA_WCKB23*	AD45
FBA_WCKB45	AW48
FBA_WCKB45*	AW47
FBA_WCKB67	AT45
FBA_WCKB67*	AT44
FBB_CLK0	H42

Ball Name	Ball #
FBB_CLK0*	G42
FBB_CLK1	F47
FBB_CLK1*	E47
FBB_CMD0	B35
FBB_CMD1	A35
FBB_CMD10	A39
FBB_CMD11	B39
FBB_CMD12	C39
FBB_CMD13	C41
FBB_CMD14	B41
FBB_CMD15	A41
FBB_CMD16	B49
FBB_CMD17	A49
FBB_CMD18	A48
FBB_CMD19	D47
FBB_CMD2	D35
FBB_CMD20	A47
FBB_CMD21	B47
FBB_CMD22	C47
FBB_CMD23	C45
FBB_CMD24	B45
FBB_CMD25	A45
FBB_CMD26	D44
FBB_CMD27	A44
FBB_CMD28	B44
FBB_CMD29	C44
FBB_CMD3	A36
FBB_CMD30	C42
FBB_CMD31	B42
FBB_CMD32	D41
FBB_CMD33	A42
FBB_CMD34	C35
FBB_CMD35	B50
FBB_CMD4	B36
FBB_CMD5	C36
FBB_CMD6	C38
FBB_CMD7	B38
FBB_CMD8	A38
FBB_CMD9	D38
FBB_D0	H32
FBB_D1	D32

Ball Name	Ball #
FBB_D10	J36
FBB_D11	F36
FBB_D12	F33
FBB_D13	D33
FBB_D14	J32
FBB_D15	G33
FBB_D16	E45
FBB_D17	D45
FBB_D18	F45
FBB_D19	G45
FBB_D2	A33
FBB_D20	D42
FBB_D21	E42
FBB_D22	F42
FBB_D23	H41
FBB_D24	E41
FBB_D25	F39
FBB_D26	E39
FBB_D27	D39
FBB_D28	F38
FBB_D29	E38
FBB_D3	B32
FBB_D30	D36
FBB_D31	E36
FBB_D32	M50
FBB_D33	P48
FBB_D34	M51
FBB_D35	M49
FBB_D36	P47
FBB_D37	P52
FBB_D38	R46
FBB_D39	P46
FBB_D4	E32
FBB_D40	L50
FBB_D41	L51
FBB_D42	L52
FBB_D43	L49
FBB_D44	M46
FBB_D45	L47
FBB_D46	M48
FBB_D47	M47

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
FBB_D48	D48	FBB_WCK01*	H33	FBC_CMD29	C18
FBB_D49	C50	FBB_WCK23	J39	FBC_CMD3	D11
FBB_D5	G32	FBB_WCK23*	H39	FBC_CMD30	B18
FBB_D50	C48	FBB_WCK45	L46	FBC_CMD31	A18
FBB_D51	C49	FBB_WCK45*	L45	FBC_CMD32	A17
FBB_D52	E49	FBB_WCK67	H47	FBC_CMD33	D17
FBB_D53	E50	FBB_WCK67*	H46	FBC_CMD34	A9
FBB_D54	F49	FBB_WCKB01	G35	FBC_CMD35	C24
FBB_D55	F48	FBB_WCKB01*	H35	FBC_CMD4	A12
FBB_D56	F50	FBB_WCKB23	F41	FBC_CMD5	B12
FBB_D57	D52	FBB_WCKB23*	G41	FBC_CMD6	C12
FBB_D58	J50	FBB_WCKB45	M44	FBC_CMD7	C14
FBB_D59	H48	FBB_WCKB45*	M45	FBC_CMD8	B14
FBB_D6	J30	FBB_WCKB67	J47	FBC_CMD9	A14
FBB_D60	H51	FBB_WCKB67*	J46	FBC_D0	C6
FBB_D61	J51	FBC_CLK0	G15	FBC_D1	D6
FBB_D62	H49	FBC_CLK0*	F15	FBC_D10	E9
FBB_D63	H52	FBC_CLK1	H21	FBC_D11	B9
FBB_D7	F32	FBC_CLK1*	J21	FBC_D12	B8
FBB_D8	H36	FBC_CMD0	C11	FBC_D13	A8
FBB_D9	G36	FBC_CMD1	B11	FBC_D14	F6
FBB_DBG_RFU1	J35	FBC_CMD10	D14	FBC_D15	E6
FBB_DBG_RFU2	J41	FBC_CMD11	A15	FBC_D16	F18
FBB_DQM0	C32	FBC_CMD12	B15	FBC_D17	G18
FBB_DQM1	E33	FBC_CMD13	C15	FBC_D18	E18
FBB_DQM2	E44	FBC_CMD14	C17	FBC_D19	H18
FBB_DQM3	G39	FBC_CMD15	B17	FBC_D2	A6
FBB_DQM4	P49	FBC_CMD16	B24	FBC_D20	D15
FBB_DQM5	L48	FBC_CMD17	A24	FBC_D21	E15
FBB_DQM6	D50	FBC_CMD18	D23	FBC_D22	G17
FBB_DQM7	H50	FBC_CMD19	A23	FBC_D23	H17
FBB_DQS_WP0	B33	FBC_CMD2	A11	FBC_D24	J15
FBB_DQS_WP1	E35	FBC_CMD20	B23	FBC_D25	H15
FBB_DQS_WP2	G44	FBC_CMD21	C23	FBC_D26	E14
FBB_DQS_WP3	H38	FBC_CMD22	C21	FBC_D27	F14
FBB_DQS_WP4	P50	FBC_CMD23	B21	FBC_D28	H11
FBB_DQS_WP5	J48	FBC_CMD24	A21	FBC_D29	G11
FBB_DQS_WP6	D51	FBC_CMD25	D20	FBC_D3	B6
FBB_DQS_WP7	F51	FBC_CMD26	A20	FBC_D30	F11
FBB_PLL_AVDD	L38	FBC_CMD27	B20	FBC_D31	E11
FBB_WCK01	J33	FBC_CMD28	C20	FBC_D32	J29

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
FBC_D33	F30	FBC_DQM2	J18	FBD_CMD14	V2
FBC_D34	H29	FBC_DQM3	F12	FBD_CMD15	V1
FBC_D35	G30	FBC_DQM4	D29	FBD_CMD16	L3
FBC_D36	B30	FBC_DQM5	E27	FBD_CMD17	L2
FBC_D37	A30	FBC_DQM6	F20	FBD_CMD18	L1
FBC_D38	H30	FBC_DQM7	E26	FBD_CMD19	M4
FBC_D39	C30	FBC_DQS_WP0	D5	FBD_CMD2	AD4
FBC_D4	B4	FBC_DQS_WP1	D8	FBD_CMD20	M1
FBC_D40	D27	FBC_DQS_WP2	E17	FBD_CMD21	M2
FBC_D41	J26	FBC_DQS_WP3	E12	FBD_CMD22	M3
FBC_D42	F27	FBC_DQS_WP4	E30	FBD_CMD23	P3
FBC_D43	G27	FBC_DQS_WP5	B29	FBD_CMD24	P2
FBC_D44	C27	FBC_DQS_WP6	G21	FBD_CMD25	P1
FBC_D45	B27	FBC_DQS_WP7	E24	FBD_CMD26	R4
FBC_D46	A27	FBC_PLL_AVDD	L17	FBD_CMD27	R1
FBC_D47	G29	FBC_WCK01	F8	FBD_CMD28	R2
FBC_D48	H20	FBC_WCK01*	G8	FBD_CMD29	R3
FBC_D49	D18	FBC_WCK23	H12	FBD_CMD3	AC1
FBC_D5	A4	FBC_WCK23*	G12	FBD_CMD30	U3
FBC_D50	G20	FBC_WCK45	J27	FBD_CMD31	U2
FBC_D51	E20	FBC_WCK45*	H27	FBD_CMD32	V4
FBC_D52	F23	FBC_WCK67	G23	FBD_CMD33	U1
FBC_D53	E21	FBC_WCK67*	H23	FBD_CMD34	AD3
FBC_D54	D21	FBC_WCKB01	G9	FBD_CMD35	J3
FBC_D55	E23	FBC_WCKB01*	F9	FBD_CMD4	AC2
FBC_D56	G24	FBC_WCKB23	G14	FBD_CMD5	AC3
FBC_D57	H26	FBC_WCKB23*	H14	FBD_CMD6	AA3
FBC_D58	F24	FBC_WCKB45	E29	FBD_CMD7	AA2
FBC_D59	G26	FBC_WCKB45*	F29	FBD_CMD8	AA1
FBC_D6	B3	FBC_WCKB67	H24	FBD_CMD9	AA4
FBC_D60	F26	FBC_WCKB67*	J24	FBD_D0	AK8
FBC_D61	D26	FBD_CLK0	Y8	FBD_D1	AK4
FBC_D62	B26	FBD_CLK0*	Y7	FBD_D10	AG6
FBC_D63	C26	FBD_CLK1	R8	FBD_D11	AG7
FBC_D7	C4	FBD_CLK1*	R7	FBD_D12	AJ4
FBC_D8	D9	FBD_CMD0	AD2	FBD_D13	AJ5
FBC_D9	C9	FBD_CMD1	AD1	FBD_D14	AJ6
FBC_DBG_RFU1	J14	FBD_CMD10	Y1	FBD_D15	AG5
FBC_DBG_RFU2	J23	FBD_CMD11	Y2	FBD_D16	Y6
FBC_DQM0	A5	FBD_CMD12	Y3	FBD_D17	Y5
FBC_DQM1	C8	FBD_CMD13	V3	FBD_D18	V5

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
FBD_D19	Y4	FBD_D56	P6	FBD_WCKB23	AC7
FBD_D2	AK2	FBD_D57	R9	FBD_WCKB23*	AC8
FBD_D20	AA6	FBD_D58	P4	FBD_WCKB45	H7
FBD_D21	AA5	FBD_D59	P5	FBD_WCKB45*	H6
FBD_D22	AC5	FBD_D6	AK9	FBD_WCKB67	M7
FBD_D23	AC4	FBD_D60	L7	FBD_WCKB67*	M8
FBD_D24	AD7	FBD_D61	L6	FBVDDQ	AA10
FBD_D25	AC6	FBD_D62	L4	FBVDDQ	AA11
FBD_D26	AF6	FBD_D63	L5	FBVDDQ	AA42
FBD_D27	AD6	FBD_D7	AK7	FBVDDQ	AA43
FBD_D28	AF7	FBD_D8	AG4	FBVDDQ	AC10
FBD_D29	AF8	FBD_D9	AF9	FBVDDQ	AC11
FBD_D3	AK3	FBD_DBG_RFU1	AC9	FBVDDQ	AC42
FBD_D30	AF2	FBD_DBG_RFU2	P9	FBVDDQ	AC43
FBD_D31	AF3	FBD_DQM0	AJ1	FBVDDQ	AD10
FBD_D32	F4	FBD_DQM1	AG1	FBVDDQ	AD11
FBD_D33	E1	FBD_DQM2	AA7	FBVDDQ	AD42
FBD_D34	F3	FBD_DQM3	AD5	FBVDDQ	AD43
FBD_D35	F5	FBD_DQM4	D3	FBVDDQ	AF10
FBD_D36	D2	FBD_DQM5	H3	FBVDDQ	AF43
FBD_D37	D1	FBD_DQM6	U5	FBVDDQ	AG10
FBD_D38	C3	FBD_DQM7	M9	FBVDDQ	AG11
FBD_D39	C2	FBD_DQS_WP0	AJ3	FBVDDQ	AG42
FBD_D4	AK5	FBD_DQS_WP1	AG2	FBVDDQ	AG43
FBD_D40	J5	FBD_DQS_WP2	AA9	FBVDDQ	AJ10
FBD_D41	J4	FBD_DQS_WP3	AF4	FBVDDQ	AJ11
FBD_D42	L8	FBD_DQS_WP4	E3	FBVDDQ	AJ42
FBD_D43	J2	FBD_DQS_WP5	H2	FBVDDQ	AJ43
FBD_D44	F1	FBD_DQS_WP6	U6	FBVDDQ	AK10
FBD_D45	F2	FBD_DQS_WP7	M5	FBVDDQ	AK11
FBD_D46	H4	FBD_PLL_AVDD	V11	FBVDDQ	AK42
FBD_D47	H5	FBD_WCK01	AJ8	FBVDDQ	AK43
FBD_D48	V7	FBD_WCK01*	AJ7	FBVDDQ	AM42
FBD_D49	V8	FBD_WCK23	AD8	FBVDDQ	AM43
FBD_D5	AK6	FBD_WCK23*	AD9	FBVDDQ	AN43
FBD_D50	V6	FBD_WCK45	J6	FBVDDQ	AR42
FBD_D51	V9	FBD_WCK45*	J7	FBVDDQ	AR43
FBD_D52	U4	FBD_WCK67	P8	FBVDDQ	AT43
FBD_D53	R5	FBD_WCK67*	P7	FBVDDQ	K12
FBD_D54	R6	FBD_WCKB01	AG8	FBVDDQ	K14
FBD_D55	U8	FBD_WCKB01*	AG9	FBVDDQ	K15

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
FBVDDQ	K17	FBVDDQ	R43	GND	AB31
FBVDDQ	K18	FBVDDQ	U10	GND	AB32
FBVDDQ	K20	FBVDDQ	U11	GND	AB33
FBVDDQ	K21	FBVDDQ	U43	GND	AB34
FBVDDQ	K23	FBVDDQ	V10	GND	AB35
FBVDDQ	K24	FBVDDQ	V42	GND	AB36
FBVDDQ	K26	FBVDDQ	V43	GND	AB37
FBVDDQ	K27	FBVDDQ	Y10	GND	AB38
FBVDDQ	K29	FBVDDQ	Y11	GND	AB39
FBVDDQ	K30	FBVDDQ	Y42	GND	AB4
FBVDDQ	K32	FBVDDQ	Y43	GND	AB43
FBVDDQ	K33	FBVDDQ_SENSE	E52	GND	AB45
FBVDDQ	K35	FP_FUSE_SRC	BD14	GND	AB47
FBVDDQ	K36	GND	A2	GND	AB49
FBVDDQ	K38	GND	A26	GND	AB51
FBVDDQ	K39	GND	A29	GND	AB6
FBVDDQ	K41	GND	A3	GND	AB8
FBVDDQ	L14	GND	A32	GND	AD14
FBVDDQ	L15	GND	A50	GND	AD15
FBVDDQ	L18	GND	A51	GND	AD16
FBVDDQ	L20	GND	AA49	GND	AD17
FBVDDQ	L21	GND	AA8	GND	AD18
FBVDDQ	L23	GND	AB10	GND	AD19
FBVDDQ	L24	GND	AB14	GND	AD20
FBVDDQ	L26	GND	AB15	GND	AD21
FBVDDQ	L27	GND	AB16	GND	AD22
FBVDDQ	L30	GND	AB17	GND	AD23
FBVDDQ	L32	GND	AB18	GND	AD24
FBVDDQ	L33	GND	AB19	GND	AD25
FBVDDQ	L35	GND	AB2	GND	AD26
FBVDDQ	L36	GND	AB20	GND	AD27
FBVDDQ	L39	GND	AB21	GND	AD28
FBVDDQ	M10	GND	AB22	GND	AD29
FBVDDQ	M43	GND	AB23	GND	AD30
FBVDDQ	P10	GND	AB24	GND	AD31
FBVDDQ	P11	GND	AB25	GND	AD32
FBVDDQ	P42	GND	AB26	GND	AD33
FBVDDQ	P43	GND	AB27	GND	AD34
FBVDDQ	R10	GND	AB28	GND	AD35
FBVDDQ	R11	GND	AB29	GND	AD36
FBVDDQ	R42	GND	AB30	GND	AD37

Ball Name	Ball #
GND	AD38
GND	AD39
GND	AD44
GND	AE10
GND	AE2
GND	AE4
GND	AE43
GND	AE45
GND	AE47
GND	AE49
GND	AE51
GND	AE6
GND	AE8
GND	AF1
GND	AF19
GND	AF20
GND	AF21
GND	AF22
GND	AF23
GND	AF27
GND	AF28
GND	AF29
GND	AF35
GND	AF36
GND	AF37
GND	AF38
GND	AF39
GND	AF45
GND	AF5
GND	AG14
GND	AG15
GND	AG16
GND	AG17
GND	AG18
GND	AG24
GND	AG25
GND	AG26
GND	AG3
GND	AG30
GND	AG31
GND	AG32

Ball Name	Ball #
GND	AG33
GND	AG34
GND	AG44
GND	AH10
GND	AH2
GND	AH4
GND	AH43
GND	AH45
GND	AH47
GND	AH49
GND	AH51
GND	AH6
GND	AH8
GND	AJ14
GND	AJ15
GND	AJ16
GND	AJ17
GND	AJ18
GND	AJ19
GND	AJ2
GND	AJ20
GND	AJ21
GND	AJ22
GND	AJ23
GND	AJ24
GND	AJ25
GND	AJ26
GND	AJ27
GND	AJ28
GND	AJ29
GND	AJ30
GND	AJ31
GND	AJ32
GND	AJ33
GND	AJ34
GND	AJ35
GND	AJ36
GND	AJ37
GND	AJ38
GND	AJ39
GND	AJ9

Ball Name	Ball #
GND	AK1
GND	AK44
GND	AK47
GND	AL10
GND	AL14
GND	AL15
GND	AL16
GND	AL17
GND	AL18
GND	AL19
GND	AL2
GND	AL20
GND	AL21
GND	AL22
GND	AL23
GND	AL24
GND	AL25
GND	AL26
GND	AL27
GND	AL28
GND	AL29
GND	AL30
GND	AL31
GND	AL32
GND	AL33
GND	AL34
GND	AL35
GND	AL36
GND	AL37
GND	AL38
GND	AL39
GND	AL4
GND	AL43
GND	AL45
GND	AL47
GND	AL49
GND	AL51
GND	AL6
GND	AL8
GND	AM4
GND	AM9

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
GND	AN14	GND	AR16	GND	AU21
GND	AN15	GND	AR17	GND	AU22
GND	AN16	GND	AR18	GND	AU23
GND	AN17	GND	AR19	GND	AU24
GND	AN18	GND	AR20	GND	AU25
GND	AN19	GND	AR21	GND	AU26
GND	AN20	GND	AR22	GND	AU27
GND	AN21	GND	AR23	GND	AU28
GND	AN22	GND	AR24	GND	AU29
GND	AN23	GND	AR25	GND	AU30
GND	AN24	GND	AR26	GND	AU31
GND	AN25	GND	AR27	GND	AU32
GND	AN26	GND	AR28	GND	AU33
GND	AN27	GND	AR29	GND	AU34
GND	AN28	GND	AR30	GND	AU35
GND	AN29	GND	AR31	GND	AU36
GND	AN30	GND	AR32	GND	AU37
GND	AN31	GND	AR33	GND	AU38
GND	AN32	GND	AR34	GND	AU39
GND	AN33	GND	AR35	GND	AU4
GND	AN34	GND	AR36	GND	AU45
GND	AN35	GND	AR37	GND	AU47
GND	AN36	GND	AR38	GND	AU49
GND	AN37	GND	AR39	GND	AU51
GND	AN38	GND	AR4	GND	AU6
GND	AN39	GND	AR52	GND	AU8
GND	AN4	GND	AR9	GND	AV4
GND	AN5	GND	AT4	GND	AV45
GND	AN8	GND	AT5	GND	AV9
GND	AP10	GND	AT51	GND	AW14
GND	AP2	GND	AT52	GND	AW15
GND	AP4	GND	AT8	GND	AW16
GND	AP43	GND	AU10	GND	AW17
GND	AP45	GND	AU14	GND	AW18
GND	AP47	GND	AU15	GND	AW19
GND	AP49	GND	AU16	GND	AW20
GND	AP51	GND	AU17	GND	AW21
GND	AP6	GND	AU18	GND	AW22
GND	AP8	GND	AU19	GND	AW23
GND	AR14	GND	AU2	GND	AW24
GND	AR15	GND	AU20	GND	AW25

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
GND	AW26	GND	B46	GND	BE30
GND	AW27	GND	B48	GND	BE31
GND	AW28	GND	B5	GND	BE33
GND	AW29	GND	B51	GND	BE34
GND	AW30	GND	B52	GND	BE36
GND	AW31	GND	B7	GND	BE37
GND	AW32	GND	BA48	GND	BE39
GND	AW33	GND	BA9	GND	BE40
GND	AW34	GND	BB49	GND	BF2
GND	AW35	GND	BC13	GND	BF4
GND	AW36	GND	BC16	GND	BF41
GND	AW37	GND	BC19	GND	BF6
GND	AW38	GND	BC2	GND	BG10
GND	AW39	GND	BC22	GND	BG13
GND	AW4	GND	BC25	GND	BG16
GND	AW46	GND	BC28	GND	BG19
GND	AW5	GND	BC31	GND	BG22
GND	AW52	GND	BC34	GND	BG25
GND	AW8	GND	BC37	GND	BG28
GND	AY10	GND	BC4	GND	BG31
GND	AY2	GND	BC51	GND	BG34
GND	AY4	GND	BC6	GND	BG37
GND	AY47	GND	BC8	GND	BG40
GND	AY49	GND	BD26	GND	BG42
GND	AY51	GND	BD29	GND	BG7
GND	AY6	GND	BD32	GND	BH15
GND	AY8	GND	BD35	GND	BH18
GND	B1	GND	BD38	GND	BH2
GND	B10	GND	BD52	GND	BH21
GND	B13	GND	BE10	GND	BH24
GND	B16	GND	BE13	GND	BH27
GND	B19	GND	BE15	GND	BH30
GND	B2	GND	BE16	GND	BH33
GND	B22	GND	BE18	GND	BH36
GND	B25	GND	BE19	GND	BH39
GND	B28	GND	BE21	GND	BH42
GND	B31	GND	BE22	GND	BH5
GND	B34	GND	BE24	GND	BJ10
GND	B37	GND	BE25	GND	BJ12
GND	B40	GND	BE27	GND	BJ13
GND	B43	GND	BE28	GND	BJ14

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
GND	BJ15	GND	BL34	GND	F16
GND	BJ16	GND	BL37	GND	F17
GND	BJ17	GND	BL40	GND	F19
GND	BJ18	GND	BL43	GND	F21
GND	BJ19	GND	BL5	GND	F22
GND	BJ20	GND	BL7	GND	F25
GND	BJ21	GND	BM2	GND	F28
GND	BJ22	GND	BM3	GND	F31
GND	BJ23	GND	C1	GND	F34
GND	BJ24	GND	C29	GND	F35
GND	BJ25	GND	C33	GND	F37
GND	BJ26	GND	C5	GND	F40
GND	BJ27	GND	C51	GND	F43
GND	BJ28	GND	C52	GND	F44
GND	BJ29	GND	D10	GND	F46
GND	BJ30	GND	D12	GND	F52
GND	BJ31	GND	D13	GND	F7
GND	BJ32	GND	D16	GND	G2
GND	BJ33	GND	D19	GND	G38
GND	BJ34	GND	D22	GND	G4
GND	BJ35	GND	D24	GND	G47
GND	BJ36	GND	D25	GND	G49
GND	BJ37	GND	D28	GND	G51
GND	BJ38	GND	D30	GND	G6
GND	BJ39	GND	D31	GND	H1
GND	BJ40	GND	D34	GND	H10
GND	BJ41	GND	D37	GND	H13
GND	BJ42	GND	D4	GND	H16
GND	BJ43	GND	D40	GND	H19
GND	BJ7	GND	D43	GND	H22
GND	BK1	GND	D46	GND	H25
GND	BL1	GND	D49	GND	H28
GND	BL10	GND	D7	GND	H31
GND	BL13	GND	E2	GND	H34
GND	BL16	GND	E4	GND	H37
GND	BL19	GND	E48	GND	H40
GND	BL2	GND	E5	GND	H43
GND	BL22	GND	E51	GND	J1
GND	BL25	GND	E8	GND	J12
GND	BL28	GND	F10	GND	J17
GND	BL31	GND	F13	GND	J20

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
GND	J38	GND	P22	GND	T32
GND	J49	GND	P23	GND	T33
GND	J52	GND	P24	GND	T34
GND	K13	GND	P25	GND	T35
GND	K16	GND	P26	GND	T36
GND	K19	GND	P27	GND	T37
GND	K2	GND	P28	GND	T38
GND	K22	GND	P29	GND	T39
GND	K25	GND	P30	GND	T4
GND	K28	GND	P31	GND	T43
GND	K31	GND	P32	GND	T45
GND	K34	GND	P33	GND	T47
GND	K37	GND	P34	GND	T49
GND	K4	GND	P35	GND	T51
GND	K40	GND	P36	GND	T6
GND	K45	GND	P37	GND	T8
GND	K47	GND	P38	GND	U7
GND	K49	GND	P39	GND	U9
GND	K51	GND	P51	GND	V14
GND	K6	GND	R49	GND	V15
GND	K8	GND	R52	GND	V16
GND	M52	GND	T10	GND	V17
GND	M6	GND	T14	GND	V18
GND	N10	GND	T15	GND	V19
GND	N2	GND	T16	GND	V20
GND	N4	GND	T17	GND	V21
GND	N43	GND	T18	GND	V22
GND	N45	GND	T19	GND	V23
GND	N47	GND	T2	GND	V24
GND	N49	GND	T20	GND	V25
GND	N51	GND	T21	GND	V26
GND	N6	GND	T22	GND	V27
GND	N8	GND	T23	GND	V28
GND	P14	GND	T24	GND	V29
GND	P15	GND	T25	GND	V30
GND	P16	GND	T26	GND	V31
GND	P17	GND	T27	GND	V32
GND	P18	GND	T28	GND	V33
GND	P19	GND	T29	GND	V34
GND	P20	GND	T30	GND	V35
GND	P21	GND	T31	GND	V36

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
GND	V37	GND	Y9	I2CS_SDA	BH8
GND	V38	GND	BC24	IFP_IOVDD	BB17
GND	V39	GND_SENSE	BL45	IFP_IOVDD	BC23
GND	V49	GPCPLL_AVDD0	U42	IFP_IOVDD	BB18
GND	V52	GPCPLL_AVDD1	AF11	IFP_IOVDD	BB20
GND	W10	GPIO0	BD6	IFP_IOVDD	BB21
GND	W2	GPIO1	BB5	IFP_IOVDD	BB23
GND	W4	GPIO10	BD3	IFP_IOVDD	BC17
GND	W43	GPIO11	BH3	IFP_IOVDD	BC18
GND	W45	GPIO12	BE6	IFP_IOVDD	BC20
GND	W47	GPIO13	BB1	IFP_IOVDD	BC21
GND	W49	GPIO14	BG4	IFPA_AUX_SCL	BG11
GND	W51	GPIO15	BG1	IFPA_AUX_SDA*	BH11
GND	W6	GPIO16	BE2	IFPA_L0	BG24
GND	W8	GPIO17	BH1	IFPA_L0*	BF24
GND	Y14	GPIO18	BE3	IFPA_L1	BE23
GND	Y15	GPIO19	BD4	IFPA_L1*	BF23
GND	Y16	GPIO2	BD1	IFPA_L2	BH23
GND	Y17	GPIO20	BE5	IFPA_L2*	BG23
GND	Y18	GPIO21	BA5	IFPA_L3	BG21
GND	Y19	GPIO22	BB6	IFPA_L3*	BF21
GND	Y20	GPIO23	BG3	IFPAB_PLLVDD	BD21
GND	Y21	GPIO24	BD5	IFPAB_RSET	BD23
GND	Y22	GPIO25	BB2	IFPB_AUX_SCL	BH12
GND	Y23	GPIO26	BE7	IFPB_AUX_SDA*	BG12
GND	Y24	GPIO27	BA4	IFPB_L0	BK21
GND	Y25	GPIO28	BB4	IFPB_L0*	BL21
GND	Y26	GPIO29	BA3	IFPB_L1	BM21
GND	Y27	GPIO3	BE4	IFPB_L1*	BM20
GND	Y28	GPIO30	BB3	IFPB_L2	BL20
GND	Y29	GPIO4	BE1	IFPB_L2*	BK20
GND	Y30	GPIO5	BG2	IFPB_L3	BK18
GND	Y31	GPIO6	BD2	IFPB_L3*	BL18
GND	Y32	GPIO7	BD7	IFPC_AUX_SCL	BK9
GND	Y33	GPIO8	BH4	IFPC_AUX_SDA*	BL9
GND	Y34	GPIO9	BJ3	IFPC_L0	BE20
GND	Y35	I2CB_SCL	BG8	IFPC_L0*	BF20
GND	Y36	I2CB_SDA	BF8	IFPC_L1	BH20
GND	Y37	I2CC_SCL	BG9	IFPC_L1*	BG20
GND	Y38	I2CC_SDA	BH9	IFPC_L2	BG18
GND	Y39	I2CS_SCL	BJ8	IFPC_L2*	BF18

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
IFPC_L3	BE17	NC	BD24	NC	AT7
IFPC_L3*	BF17	NC	BM44	NC	AT6
IFPCD_PLLVDD	BD18	NC	AR10	NC	AV6
IFPCD_RSET	BD20	NC	AT11	NC	AV5
IFPD_AUX_SCL	BE11	NC	AT10	NC	AV7
IFPD_AUX_SDA*	BF11	NC	AT9	NC	AV8
IFPD_L0	BM18	NC	AV10	NC	AW7
IFPD_L0*	BM17	NC	AV11	NC	AW6
IFPD_L1	BL17	NC	AM10	NVJTAG_SEL	BK23
IFPD_L1*	BK17	NC	AM11	OVERT	BG5
IFPD_L2	BK15	NC	AN10	PEX_CLKREQ*	BL26
IFPD_L2*	BL15	NC	AN11	PEX_CVDD	BB33
IFPD_L3	BM15	NC	AR11	PEX_CVDD	BC33
IFPD_L3*	BM14	NC	AN9	PEX_DVDD	BB35
IFPE_AUX_SCL	BK8	NC	AM6	PEX_DVDD	BB36
IFPE_AUX_SDA*	BL8	NC	AM5	PEX_DVDD	BC35
IFPE_L0	BH17	NC	AM3	PEX_DVDD	BC36
IFPE_L0*	BG17	NC	AM1	PEX_DVDD	BD33
IFPE_L1	BG15	NC	AN1	PEX_DVDD	BD36
IFPE_L1*	BF15	NC	AN2	PEX_HVDD	BB26
IFPE_L2	BE14	NC	AN3	PEX_HVDD	BB27
IFPE_L2*	BF14	NC	AR3	PEX_HVDD	BB29
IFPE_L3	BH14	NC	AR2	PEX_HVDD	BB32
IFPE_L3*	BG14	NC	AR1	PEX_HVDD	BC26
IFPE_PLLVDD	BD15	NC	AT1	PEX_HVDD	BC27
IFPE_RSET	BD17	NC	AT2	PEX_HVDD	BC29
IFPF_AUX_SCL	BM8	NC	AT3	PEX_HVDD	BC30
IFPF_AUX_SDA*	BM9	NC	AV3	PEX_HVDD	BC32
IFPF_L0	BL14	NC	AV2	PEX_HVDD	BD27
IFPF_L0*	BK14	NC	AV1	PEX_HVDD	BD30
IFPF_L1	BK12	NC	AW1	PEX_PLL_HVDD	BB30
IFPF_L1*	BL12	NC	AW2	PEX_REFCLK	BM26
IFPF_L2	BM12	NC	AW3	PEX_REFCLK*	BM27
IFPF_L2*	BM11	NC	AM7	PEX_RST*	BK26
IFPF_L3	BL11	NC	AM8	PEX_RX0	BL27
IFPF_L3*	BK11	NC	AN7	PEX_RX0*	BK27
JTAG_TCK	BK24	NC	AN6	PEX_RX1	BK29
JTAG_TDI	BM23	NC	AR6	PEX_RX1*	BL29
JTAG_TDO	BM24	NC	AR5	PEX_RX10	BK38
JTAG_TMS	BL23	NC	AR7	PEX_RX10*	BL38
JTAG_TRST*	BL24	NC	AR8	PEX_RX11	BM38

Ball Name	Ball #
PEX_RX11*	BM39
PEX_RX12	BL39
PEX_RX12*	BK39
PEX_RX13	BK41
PEX_RX13*	BL41
PEX_RX14	BM41
PEX_RX14*	BM42
PEX_RX15	BL42
PEX_RX15*	BK42
PEX_RX2	BM29
PEX_RX2*	BM30
PEX_RX3	BL30
PEX_RX3*	BK30
PEX_RX4	BK32
PEX_RX4*	BL32
PEX_RX5	BM32
PEX_RX5*	BM33
PEX_RX6	BL33
PEX_RX6*	BK33
PEX_RX7	BK35
PEX_RX7*	BL35
PEX_RX8	BM35
PEX_RX8*	BM36
PEX_RX9	BL36
PEX_RX9*	BK36
PEX_TERMPP	BL44
PEX_TX0	BG26
PEX_TX0*	BH26
PEX_TX1	BF26
PEX_TX1*	BE26
PEX_TX10	BF35
PEX_TX10*	BE35
PEX_TX11	BF36
PEX_TX11*	BG36
PEX_TX12	BG38
PEX_TX12*	BH38
PEX_TX13	BF38
PEX_TX13*	BE38
PEX_TX14	BF39
PEX_TX14*	BG39
PEX_TX15	BH41

Ball Name	Ball #
PEX_TX15*	BG41
PEX_TX2	BF27
PEX_TX2*	BG27
PEX_TX3	BG29
PEX_TX3*	BH29
PEX_TX4	BF29
PEX_TX4*	BE29
PEX_TX5	BF30
PEX_TX5*	BG30
PEX_TX6	BG32
PEX_TX6*	BH32
PEX_TX7	BF32
PEX_TX7*	BE32
PEX_TX8	BF33
PEX_TX8*	BG33
PEX_TX9	BG35
PEX_TX9*	BH35
PEX_WAKE*	BK44
ROM_CS*	BJ4
ROM_SCLK	BK3
ROM_SI	BK2
ROM_SO	BK4
SP_PLLVDD	BD12
STRAP0	BL3
STRAP1	BL4
STRAP2	BM4
STRAP3	BM5
STRAP4	BK5
STRAP5	BJ5
THERMDN	BJ1
THERMDP	BJ2
TS_VREF	BF12
USB_DVDD	BB15
USB_DVDD	BC15
USB_HVDD	AW10
USB_HVDD	AW11
USB_L0	BA2
USB_L0*	BA1
USB_L1	BA8
USB_L1*	BA7
USB_PLL_HVDD	AW9

Ball Name	Ball #
USB_RBIA5	BA6
USB_SCL	BB8
USB_SDA	BB7
USB_TERMPO	BG6
USB_TERMPP	BH6
USB_VDDP	BE12
VDD	AA13
VDD	AA14
VDD	AA15
VDD	AA16
VDD	AA17
VDD	AA18
VDD	AA19
VDD	AA20
VDD	AA21
VDD	AA22
VDD	AA23
VDD	AA24
VDD	AA25
VDD	AA26
VDD	AA27
VDD	AA28
VDD	AA29
VDD	AA30
VDD	AA31
VDD	AA32
VDD	AA33
VDD	AA34
VDD	AA35
VDD	AA36
VDD	AA37
VDD	AA38
VDD	AA39
VDD	AA40
VDD	AB13
VDD	AB40
VDD	AC13
VDD	AC14
VDD	AC15
VDD	AC16
VDD	AC17

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
VDD	AC18	VDD	AE29	VDD	AG40
VDD	AC19	VDD	AE30	VDD	AH13
VDD	AC20	VDD	AE31	VDD	AH14
VDD	AC21	VDD	AE32	VDD	AH15
VDD	AC22	VDD	AE33	VDD	AH16
VDD	AC23	VDD	AE34	VDD	AH17
VDD	AC24	VDD	AE35	VDD	AH18
VDD	AC25	VDD	AE36	VDD	AH19
VDD	AC26	VDD	AE37	VDD	AH20
VDD	AC27	VDD	AE38	VDD	AH21
VDD	AC28	VDD	AE39	VDD	AH22
VDD	AC29	VDD	AE40	VDD	AH23
VDD	AC30	VDD	AF13	VDD	AH24
VDD	AC31	VDD	AF14	VDD	AH25
VDD	AC32	VDD	AF15	VDD	AH26
VDD	AC33	VDD	AF16	VDD	AH27
VDD	AC34	VDD	AF17	VDD	AH28
VDD	AC35	VDD	AF18	VDD	AH29
VDD	AC36	VDD	AF24	VDD	AH30
VDD	AC37	VDD	AF25	VDD	AH31
VDD	AC38	VDD	AF26	VDD	AH32
VDD	AC39	VDD	AF30	VDD	AH33
VDD	AC40	VDD	AF31	VDD	AH34
VDD	AD13	VDD	AF32	VDD	AH35
VDD	AD40	VDD	AF33	VDD	AH36
VDD	AE13	VDD	AF34	VDD	AH37
VDD	AE14	VDD	AF40	VDD	AH38
VDD	AE15	VDD	AG13	VDD	AH39
VDD	AE16	VDD	AG19	VDD	AH40
VDD	AE17	VDD	AG20	VDD	AJ13
VDD	AE18	VDD	AG21	VDD	AJ40
VDD	AE19	VDD	AG22	VDD	AK13
VDD	AE20	VDD	AG23	VDD	AK14
VDD	AE21	VDD	AG27	VDD	AK15
VDD	AE22	VDD	AG28	VDD	AK16
VDD	AE23	VDD	AG29	VDD	AK17
VDD	AE24	VDD	AG35	VDD	AK18
VDD	AE25	VDD	AG36	VDD	AK19
VDD	AE26	VDD	AG37	VDD	AK20
VDD	AE27	VDD	AG38	VDD	AK21
VDD	AE28	VDD	AG39	VDD	AK22

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
VDD	AK23	VDD	AM34	VDD	AT15
VDD	AK24	VDD	AM35	VDD	AT16
VDD	AK25	VDD	AM36	VDD	AT17
VDD	AK26	VDD	AM37	VDD	AT18
VDD	AK27	VDD	AM38	VDD	AT19
VDD	AK28	VDD	AM39	VDD	AT20
VDD	AK29	VDD	AM40	VDD	AT21
VDD	AK30	VDD	AN13	VDD	AT22
VDD	AK31	VDD	AN40	VDD	AT23
VDD	AK32	VDD	AP13	VDD	AT24
VDD	AK33	VDD	AP14	VDD	AT25
VDD	AK34	VDD	AP15	VDD	AT26
VDD	AK35	VDD	AP16	VDD	AT27
VDD	AK36	VDD	AP17	VDD	AT28
VDD	AK37	VDD	AP18	VDD	AT29
VDD	AK38	VDD	AP19	VDD	AT30
VDD	AK39	VDD	AP20	VDD	AT31
VDD	AK40	VDD	AP21	VDD	AT32
VDD	AL13	VDD	AP22	VDD	AT33
VDD	AL40	VDD	AP23	VDD	AT34
VDD	AM13	VDD	AP24	VDD	AT35
VDD	AM14	VDD	AP25	VDD	AT36
VDD	AM15	VDD	AP26	VDD	AT37
VDD	AM16	VDD	AP27	VDD	AT38
VDD	AM17	VDD	AP28	VDD	AT39
VDD	AM18	VDD	AP29	VDD	AT40
VDD	AM19	VDD	AP30	VDD	AT42
VDD	AM20	VDD	AP31	VDD	AU13
VDD	AM21	VDD	AP32	VDD	AU40
VDD	AM22	VDD	AP33	VDD	AU43
VDD	AM23	VDD	AP34	VDD	AV13
VDD	AM24	VDD	AP35	VDD	AV14
VDD	AM25	VDD	AP36	VDD	AV15
VDD	AM26	VDD	AP37	VDD	AV16
VDD	AM27	VDD	AP38	VDD	AV17
VDD	AM28	VDD	AP39	VDD	AV18
VDD	AM29	VDD	AP40	VDD	AV19
VDD	AM30	VDD	AR13	VDD	AV20
VDD	AM31	VDD	AR40	VDD	AV21
VDD	AM32	VDD	AT13	VDD	AV22
VDD	AM33	VDD	AT14	VDD	AV23

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
VDD	AV24	VDD	AY28	VDD	BE41
VDD	AV25	VDD	AY29	VDD	BE42
VDD	AV26	VDD	AY30	VDD	BE43
VDD	AV27	VDD	AY31	VDD	BE46
VDD	AV28	VDD	AY32	VDD	BE47
VDD	AV29	VDD	AY33	VDD	BE48
VDD	AV30	VDD	AY34	VDD	BE49
VDD	AV31	VDD	AY35	VDD	BE50
VDD	AV32	VDD	AY36	VDD	BE51
VDD	AV33	VDD	AY37	VDD	BE52
VDD	AV34	VDD	AY38	VDD	BF42
VDD	AV35	VDD	AY39	VDD	BF44
VDD	AV36	VDD	AY40	VDD	BF45
VDD	AV37	VDD	AY43	VDD	BF47
VDD	AV38	VDD	AY45	VDD	BF49
VDD	AV39	VDD	BA43	VDD	BF51
VDD	AV40	VDD	BA44	VDD	BG43
VDD	AV42	VDD	BA45	VDD	BG44
VDD	AV43	VDD	BA46	VDD	BG45
VDD	AV44	VDD	BA47	VDD	BG46
VDD	AW13	VDD	BB38	VDD	BG47
VDD	AW40	VDD	BB39	VDD	BG48
VDD	AW42	VDD	BB45	VDD	BG49
VDD	AW43	VDD	BB46	VDD	BG50
VDD	AW44	VDD	BB47	VDD	BG51
VDD	AW45	VDD	BB48	VDD	BG52
VDD	AY13	VDD	BC38	VDD	BH44
VDD	AY14	VDD	BC39	VDD	BH45
VDD	AY15	VDD	BC40	VDD	BH47
VDD	AY16	VDD	BC41	VDD	BH48
VDD	AY17	VDD	BC45	VDD	BH49
VDD	AY18	VDD	BC47	VDD	BH50
VDD	AY19	VDD	BC49	VDD	BH51
VDD	AY20	VDD	BD39	VDD	BH52
VDD	AY21	VDD	BD41	VDD	BJ44
VDD	AY22	VDD	BD46	VDD	BJ45
VDD	AY23	VDD	BD47	VDD	BJ46
VDD	AY24	VDD	BD48	VDD	BJ47
VDD	AY25	VDD	BD49	VDD	BJ48
VDD	AY26	VDD	BD50	VDD	BJ49
VDD	AY27	VDD	BD51	VDD	BJ50

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
VDD	BJ51	VDD	N34	VDD	U15
VDD	BJ52	VDD	N35	VDD	U16
VDD	BK47	VDD	N36	VDD	U17
VDD	BK48	VDD	N37	VDD	U18
VDD	BK49	VDD	N38	VDD	U19
VDD	BK50	VDD	N39	VDD	U20
VDD	BK51	VDD	N40	VDD	U21
VDD	BK52	VDD	P13	VDD	U22
VDD	BL46	VDD	P40	VDD	U23
VDD	BL47	VDD	R13	VDD	U24
VDD	BL48	VDD	R14	VDD	U25
VDD	BL49	VDD	R15	VDD	U26
VDD	BL50	VDD	R16	VDD	U27
VDD	BL51	VDD	R17	VDD	U28
VDD	BL52	VDD	R18	VDD	U29
VDD	BM47	VDD	R19	VDD	U30
VDD	BM48	VDD	R20	VDD	U31
VDD	BM49	VDD	R21	VDD	U32
VDD	BM50	VDD	R22	VDD	U33
VDD	BM51	VDD	R23	VDD	U34
VDD	N13	VDD	R24	VDD	U35
VDD	N14	VDD	R25	VDD	U36
VDD	N15	VDD	R26	VDD	U37
VDD	N16	VDD	R27	VDD	U38
VDD	N17	VDD	R28	VDD	U39
VDD	N18	VDD	R29	VDD	U40
VDD	N19	VDD	R30	VDD	V13
VDD	N20	VDD	R31	VDD	V40
VDD	N21	VDD	R32	VDD	W13
VDD	N22	VDD	R33	VDD	W14
VDD	N23	VDD	R34	VDD	W15
VDD	N24	VDD	R35	VDD	W16
VDD	N25	VDD	R36	VDD	W17
VDD	N26	VDD	R37	VDD	W18
VDD	N27	VDD	R38	VDD	W19
VDD	N28	VDD	R39	VDD	W20
VDD	N29	VDD	R40	VDD	W21
VDD	N30	VDD	T13	VDD	W22
VDD	N31	VDD	T40	VDD	W23
VDD	N32	VDD	U13	VDD	W24
VDD	N33	VDD	U14	VDD	W25

Ball Name	Ball #
VDD	W26
VDD	W27
VDD	W28
VDD	W29
VDD	W30
VDD	W31
VDD	W32
VDD	W33
VDD	W34
VDD	W35
VDD	W36

Ball Name	Ball #
VDD	W37
VDD	W38
VDD	W39
VDD	W40
VDD	Y13
VDD	Y40
VDD_SENSE	BK45
VID_PLLVDD	BC12
XSN_PLLVDD	BB24
XTAL_IN	BL6
XTAL_OUT	BM6

Ball Name	Ball #
XTAL_OUTBUFF	BK6

23	24	25	26	27	28	29	30
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