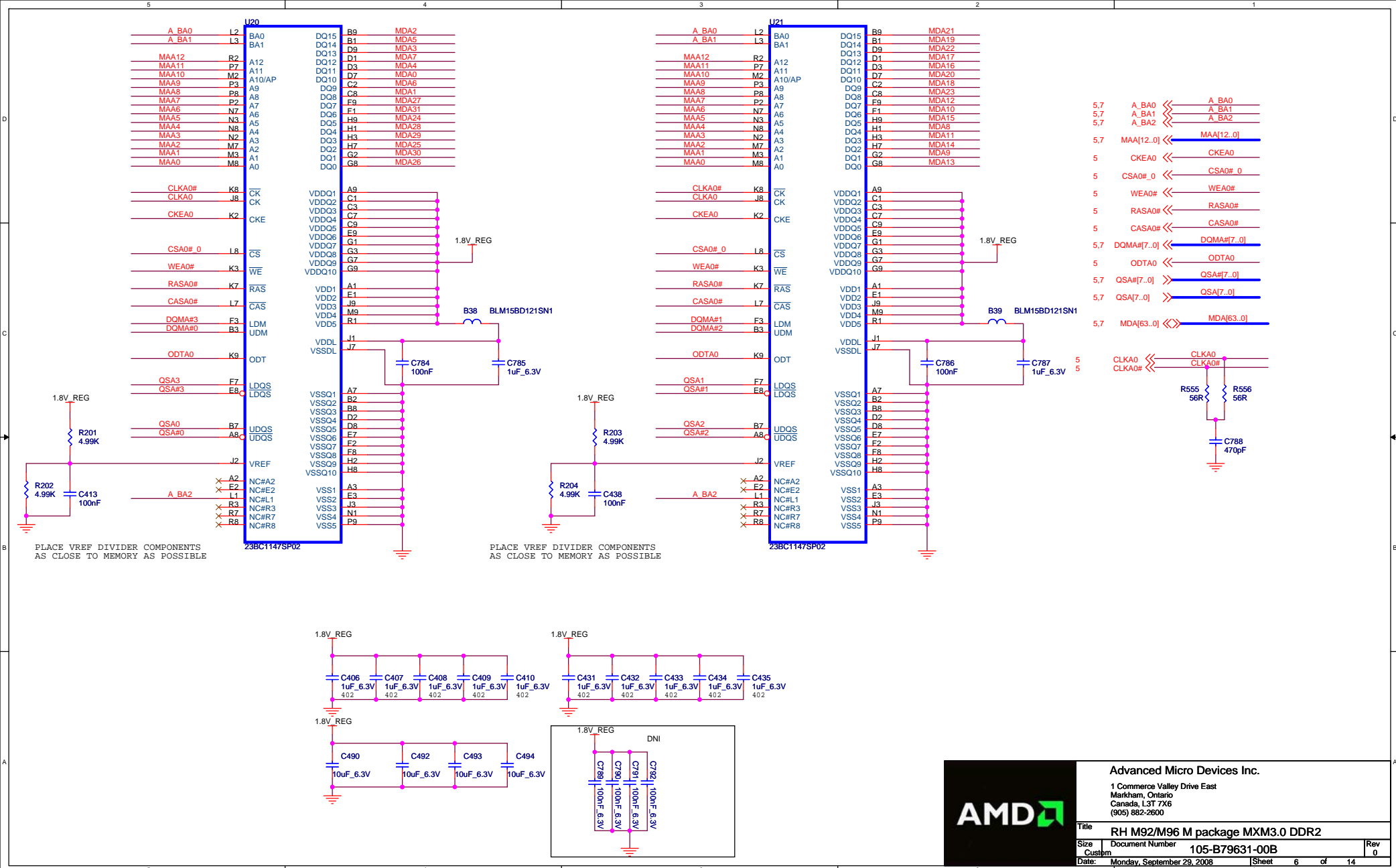
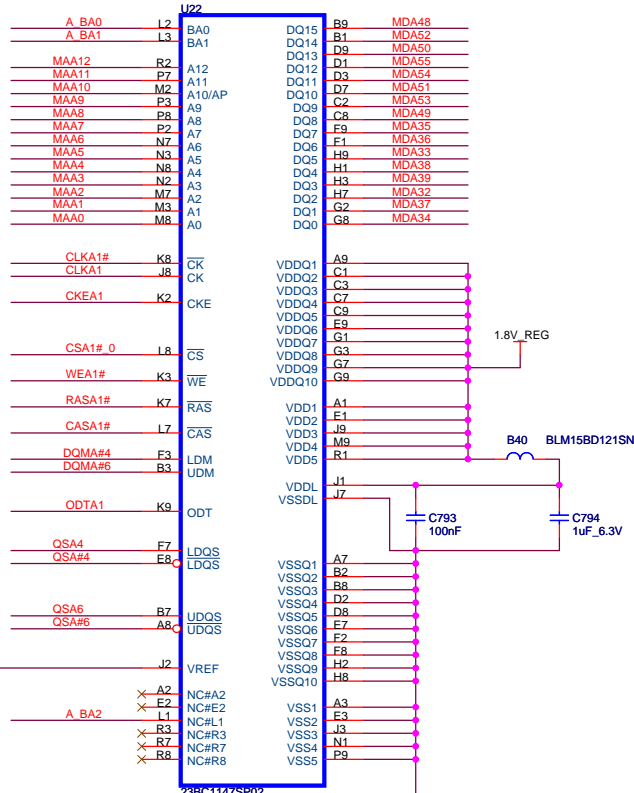


216-0729012-00

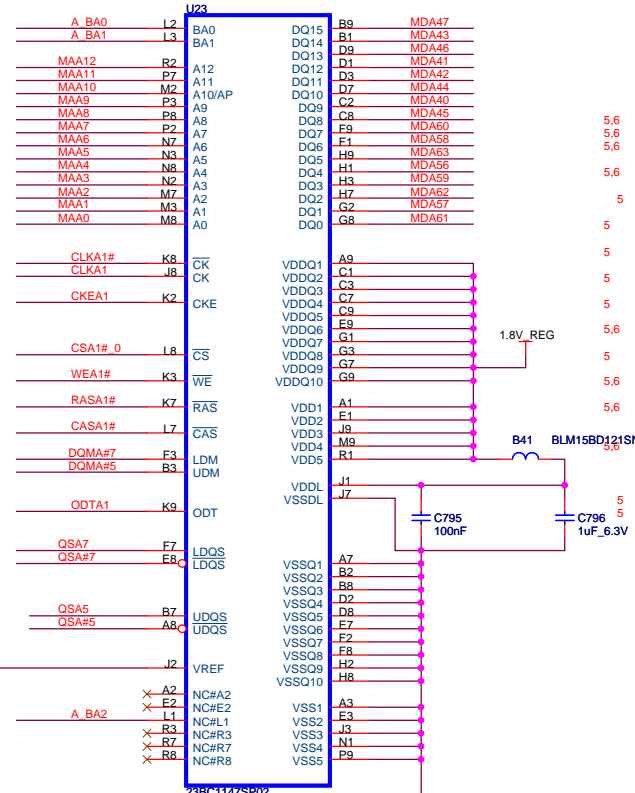




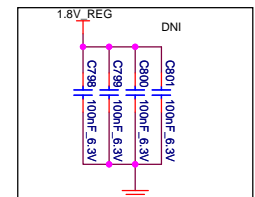
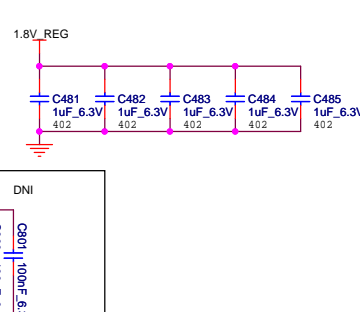
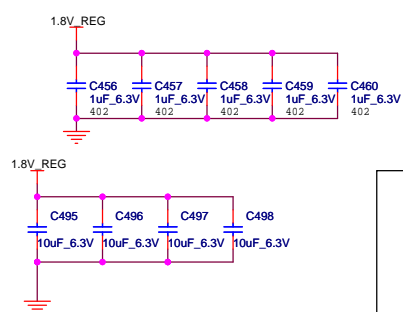
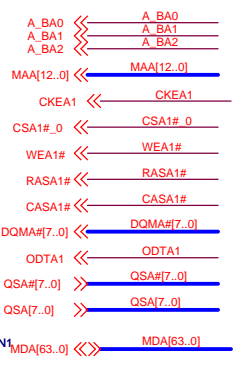




PLACE VREF DIVIDER COMPONENTS  
AS CLOSE TO MEMORY AS POSSIBLE

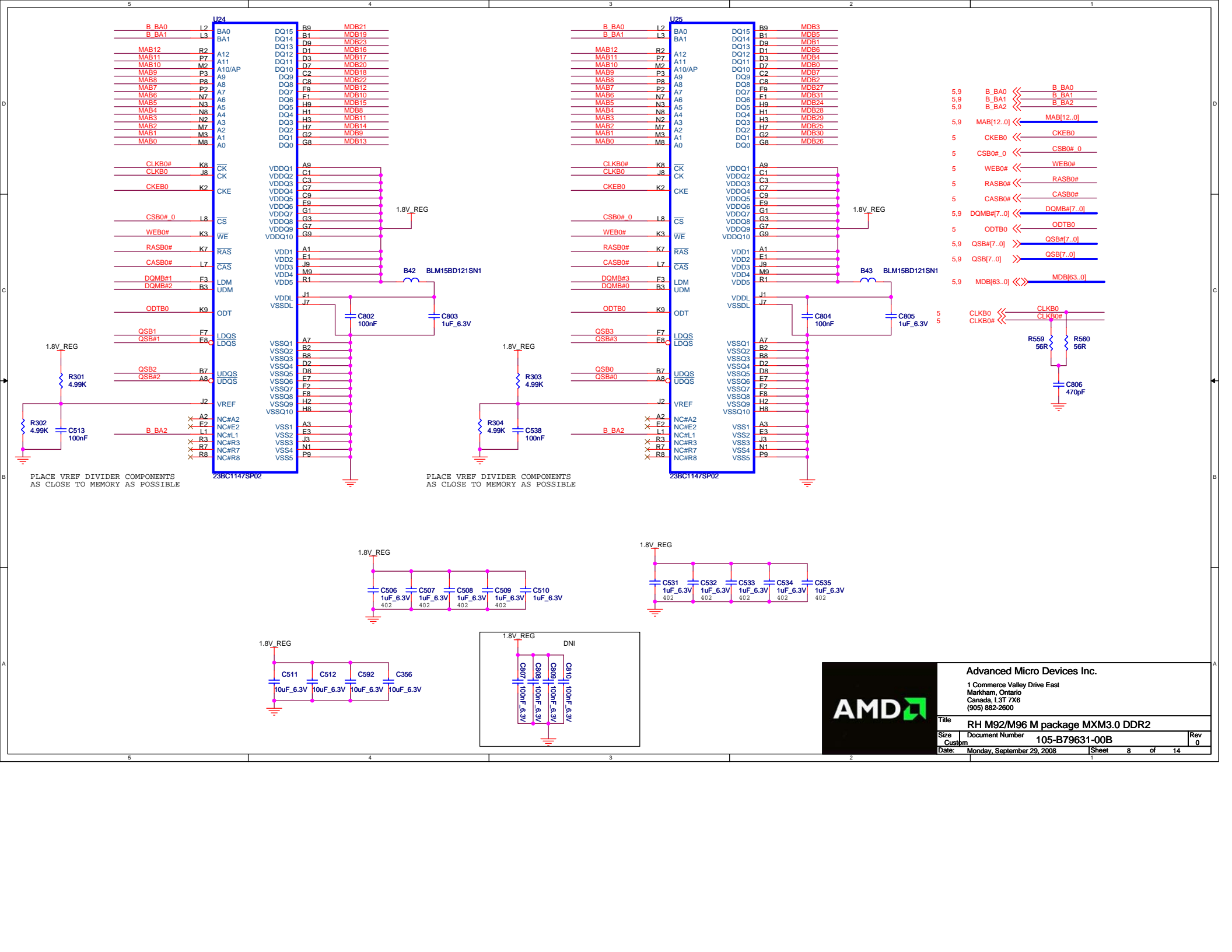


PLACE VREF DIVIDER COMPONENTS  
AS CLOSE TO MEMORY AS POSSIBLE

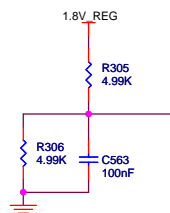
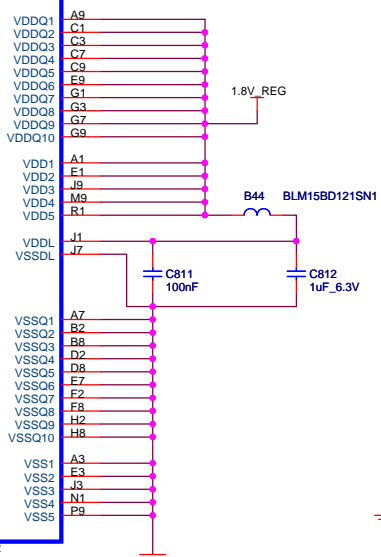
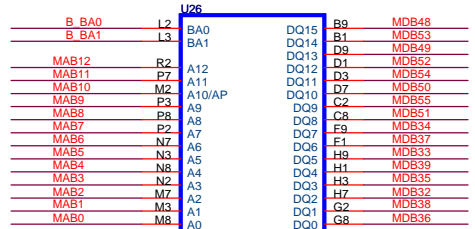


Advanced Micro Devices Inc.  
1 Commerce Valley Drive East  
Markham, Ontario  
Canada, L3T 7X6  
(905) 882-2600

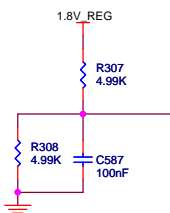
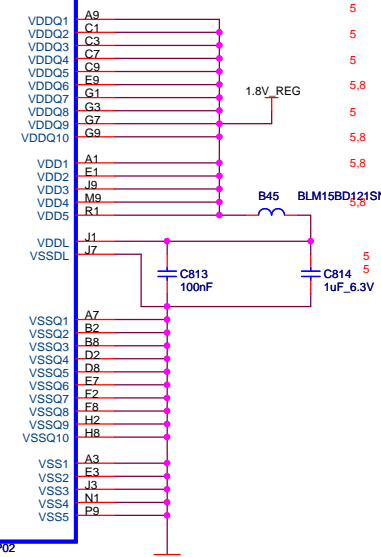
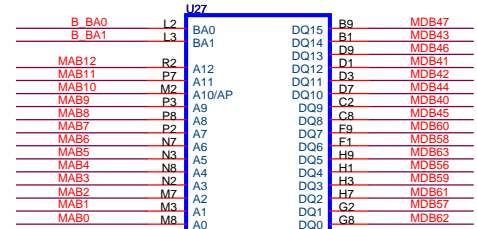
Title	RH M92/M96 M package MXM3.0 DDR2		
Size	Document Number	105-B79631-00B	Rev
Custom			0
Date:	Monday, September 29, 2008	Sheet	7 of 14



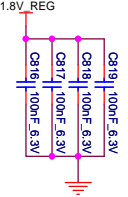
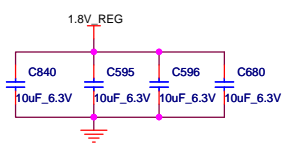
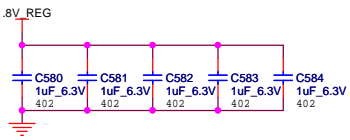
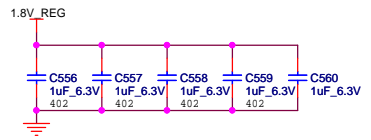
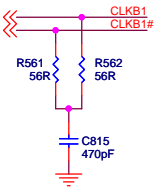
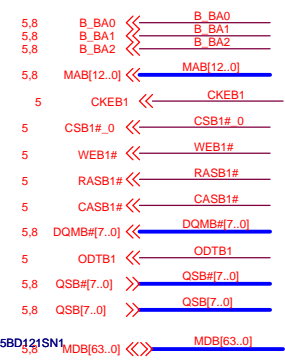




PLACE VREF DIVIDER COMPONENTS  
AS CLOSE TO MEMORY AS POSSIBLE



PLACE VREF DIVIDER COMPONENTS  
AS CLOSE TO MEMORY AS POSSIBLE

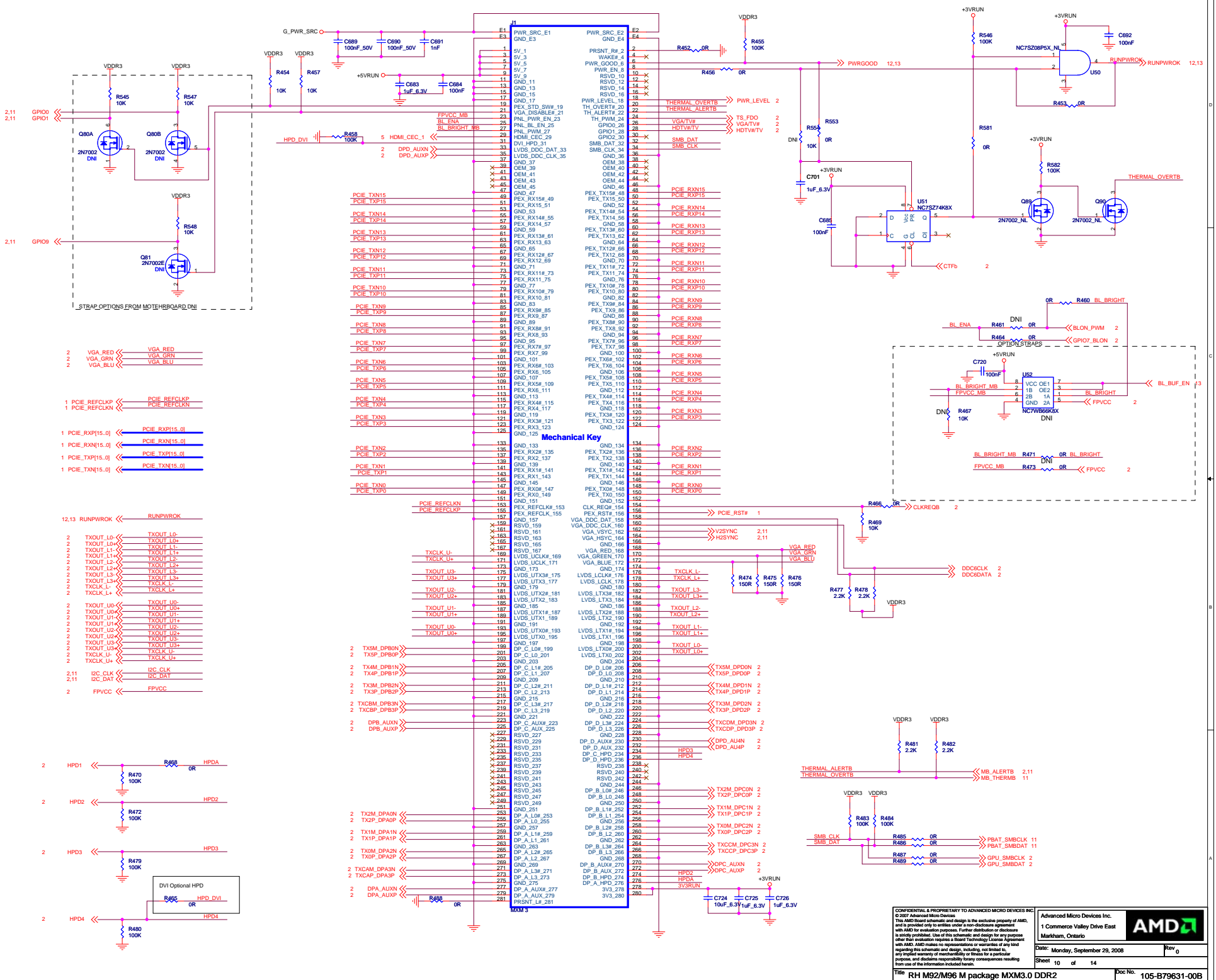





**Advanced Micro Devices Inc.**  
1 Commerce Valley Drive East  
Markham, Ontario  
Canada, L3T 7X6  
(905) 882-2600

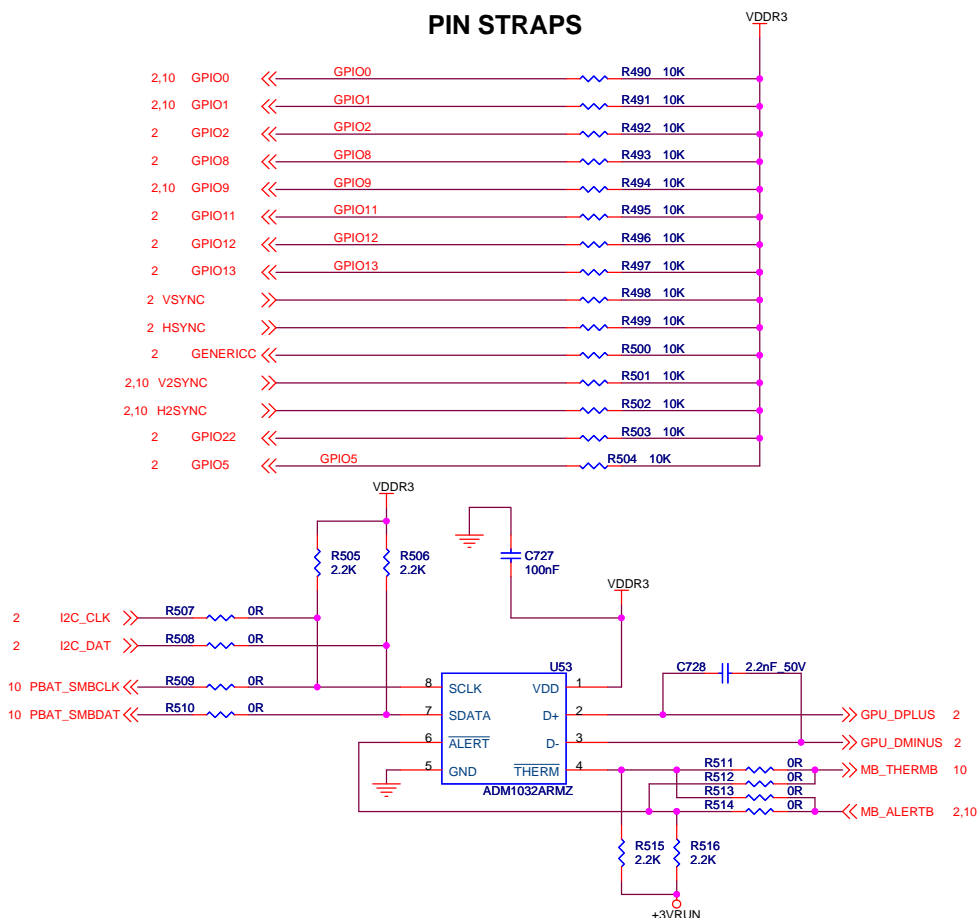
Title		RH M92/M96 M package MXM3.0 DDR2	
Size	Document Number	105-B79631-00B	
Custom			Rev 0
Date:	Monday, September 29, 2008	Sheet	9 of 14

PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE



CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC. © 2007 Advanced Micro Devices, Inc. The AMD RD880 schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for the purpose of evaluating, developing, designing or testing a third party product. This document and its contents are confidential and proprietary to AMD. AMD makes no representations or warranties of any kind regarding the accuracy, completeness, or reliability of the information contained herein. AMD makes no representations or warranties of any kind regarding the accuracy, completeness, or reliability of the information contained herein. AMD makes no representations or warranties of any kind regarding the accuracy, completeness, or reliability of the information contained herein.		Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario L3R 9V5 	
Date: <u>Monday, September 29, 2008</u>		Rev <u>0</u>	
Sheet <u>10</u> of <u>14</u>			
Title <u>RH M92/M96 M package MXM3.0 DDR2</u>		Doc No. <u>105-879631-00B</u>	

## PIN STRAPS



## CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1 = INSTALL 10K RESISTOR  
X = DESIGN DEPENDANT  
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSNC	Audio function present	1

## AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO_28_TDO	GPIO21_BB_EN

CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
© 2007 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

Advanced Micro Devices Inc.  
1 Commerce Valley Drive East  
Markham, Ontario

Date: Monday, September 29, 2008  
Sheet 11 of 14

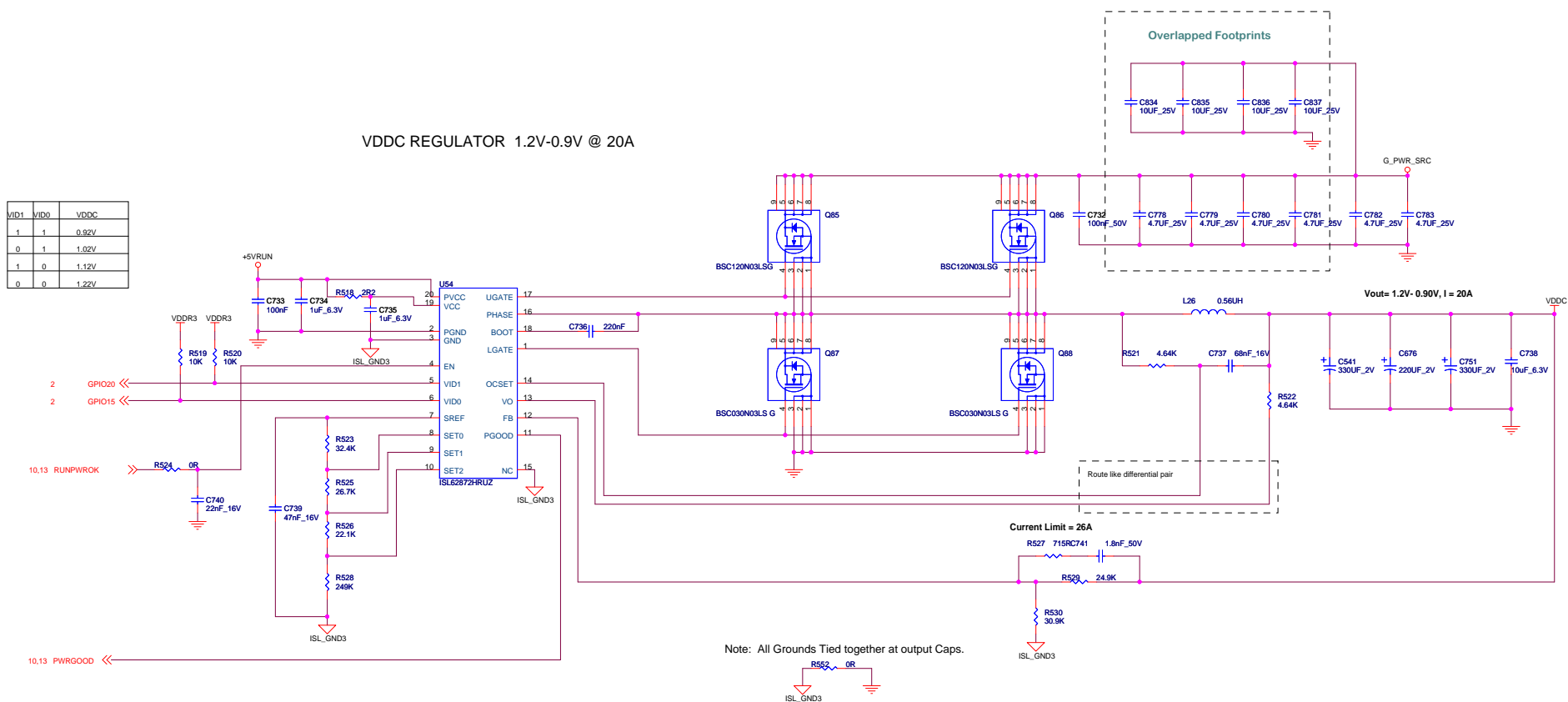
Rev 1

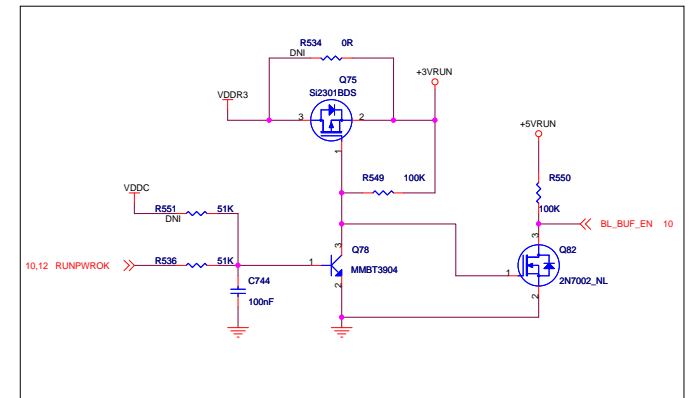
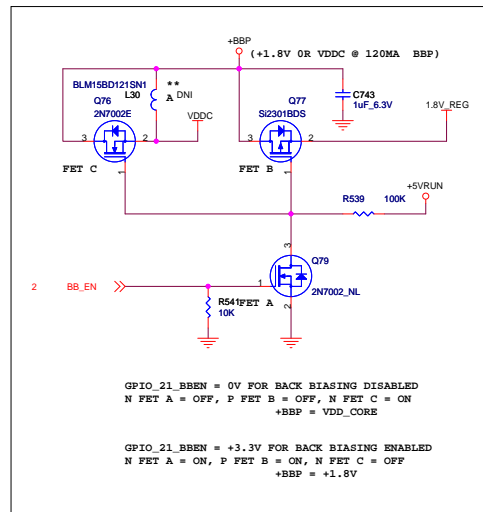
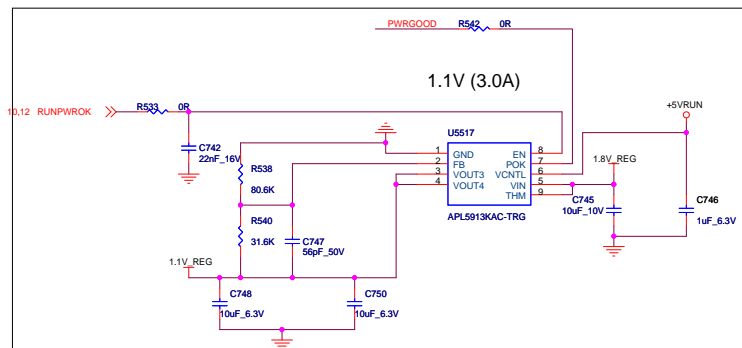
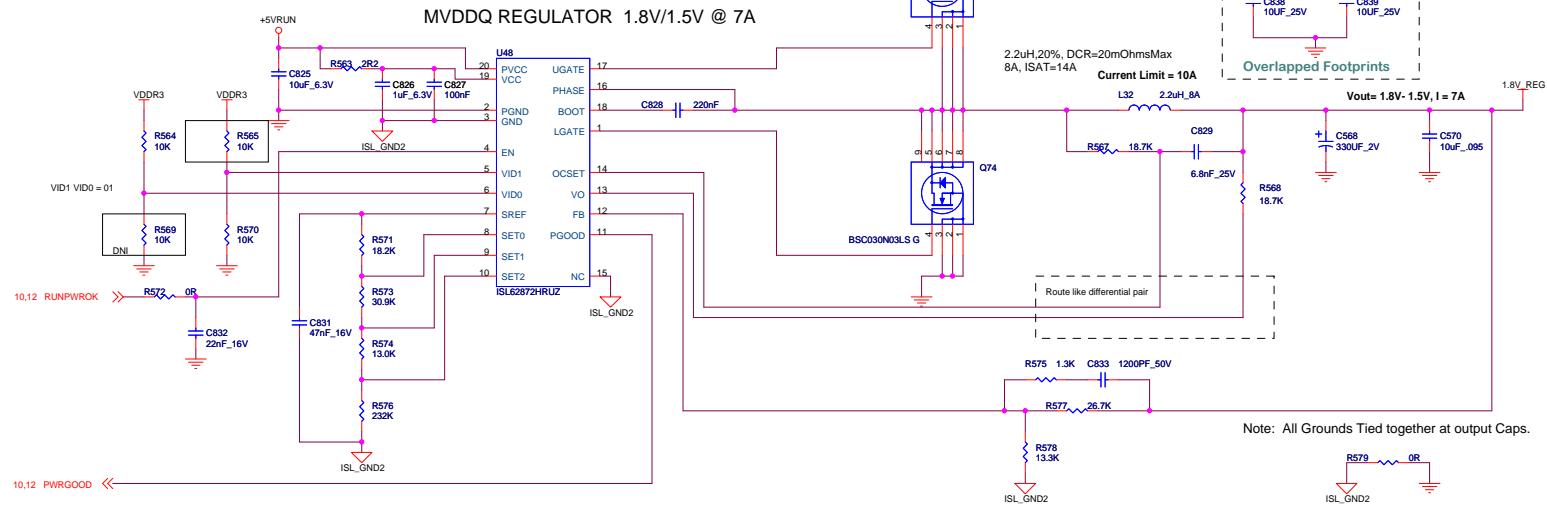
Title RH M92/M96 M package MXM3.0 DDR2

Doc No. 105-B79631-00B

VID1	VID0	VDDC
1	1	0.92V
0	1	1.02V
1	0	1.12V
0	0	1.22V

# VDDC REGULATOR 1.2V-0.9V @ 20A





<div>AMD</div>			Title		Schematic No.	Date:
			RH M92/M96 M package MXM3.0 DDR2		105-B79631-00B	Monday, September 29, 2008
			REVISION HISTORY		NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.	
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION			
0	00A	22/08/08	On base B735			
0	00B	10/09/08	CFT circuit Swap AUX5 and added AUX4 for DPD added Bead to VDDCI			