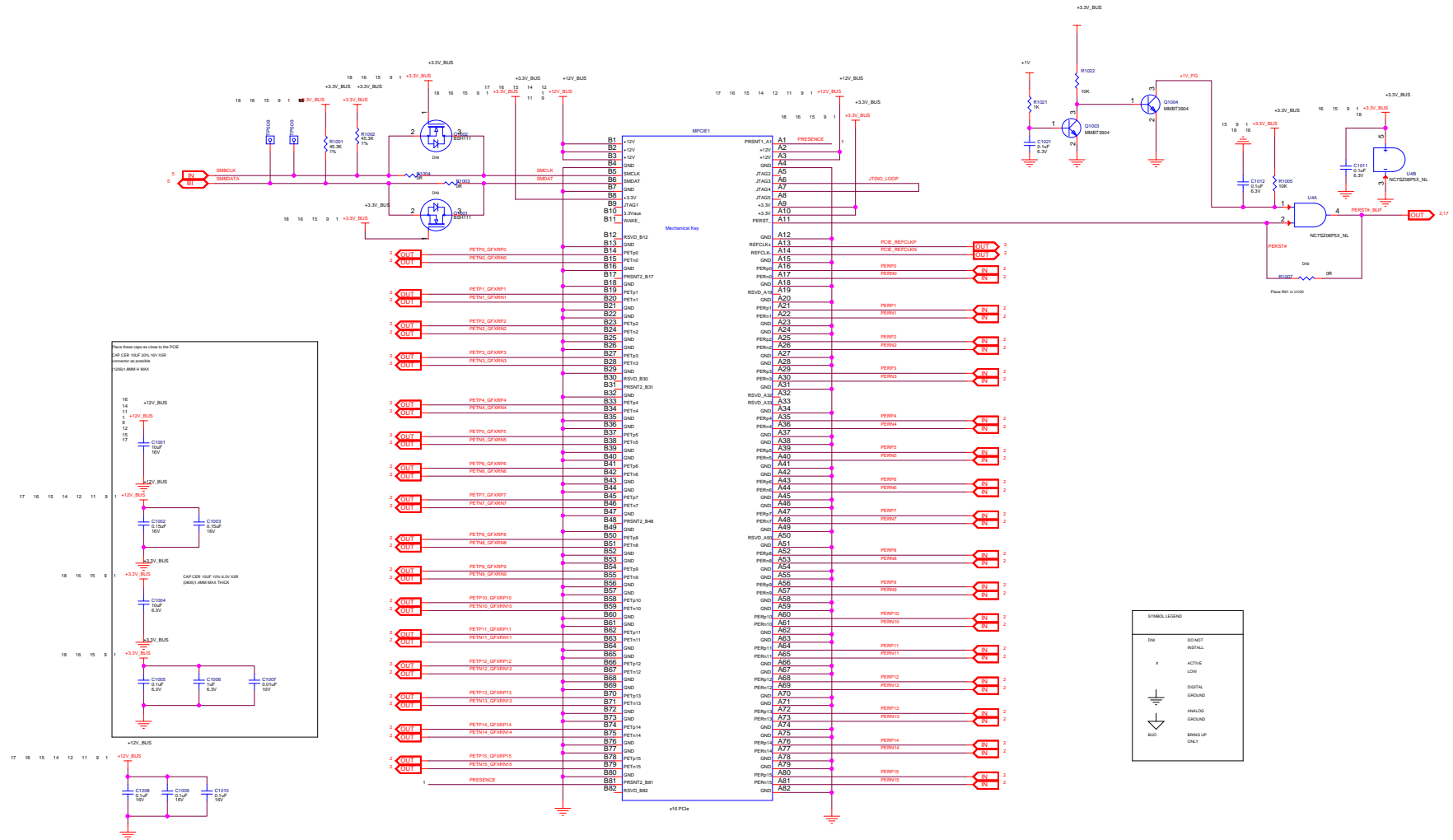


PCI-EXPRESS EDGE CONNECTOR



AMD - PLATFORM HARDWARE ENG
#48, No. 1387, ZHANGJIANG ROAD
SHANGHAI, CHINA 201203

SHEET: PCI-E Edge Connector

DATE: Tue Aug 20 06:26:30 201

SHEET NUMBER: 1 OF 20

DOCUMENT NUMBER: 105-C750xx-00A

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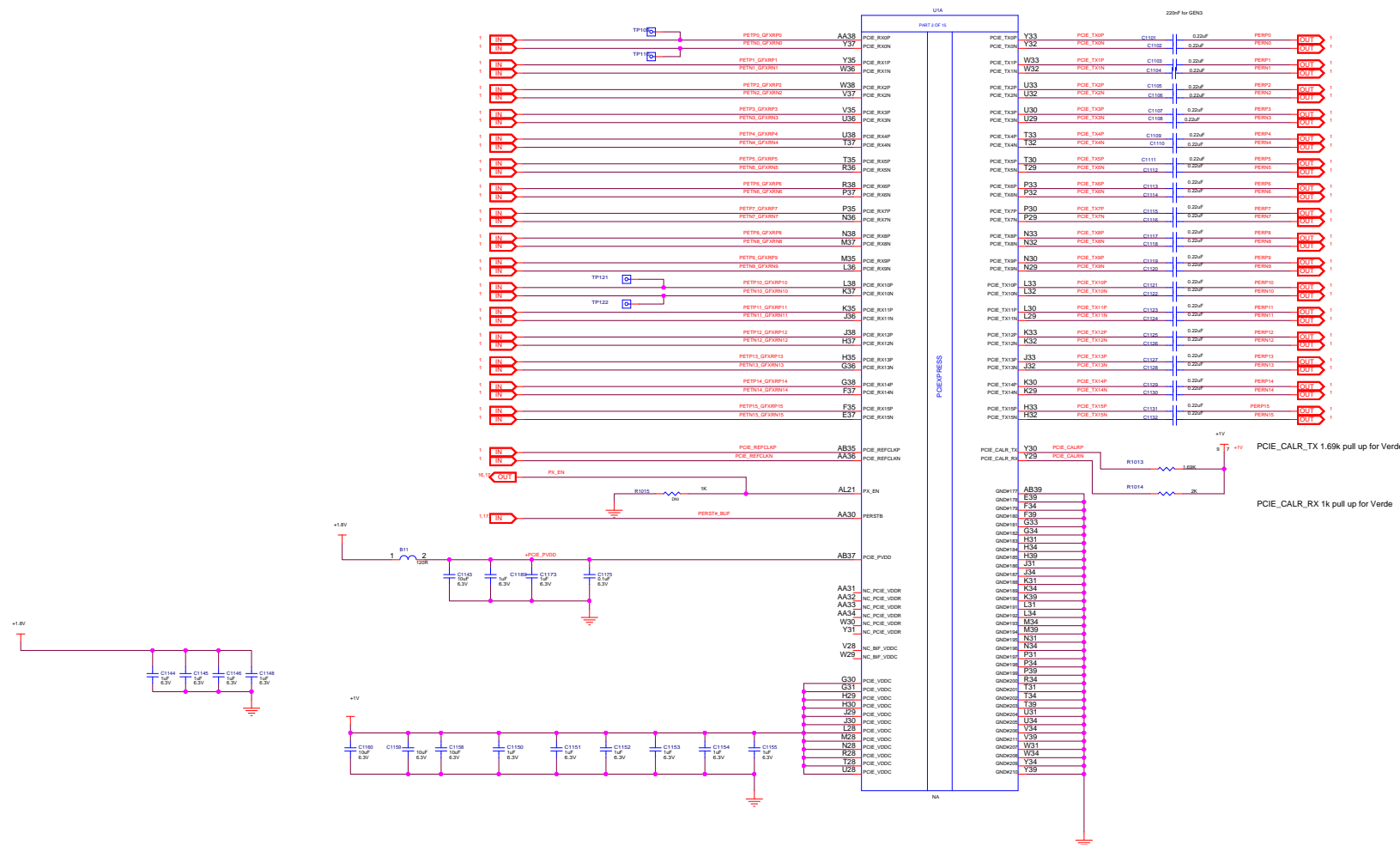
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TITLE:

PRO GDDR5 64Mx32 dDVI-I+HDMI/DP+DP/VGA

Cape_Verde PCIe Interface

NOTE: Some of the PCIe testpoints will be available through vias on traces.



PCIE_CALR_TX 1.69k pull up for Verde

PCIE_CALR_RX 1k pull up for Verde

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SHEET: Cape Verde PCIe Interface

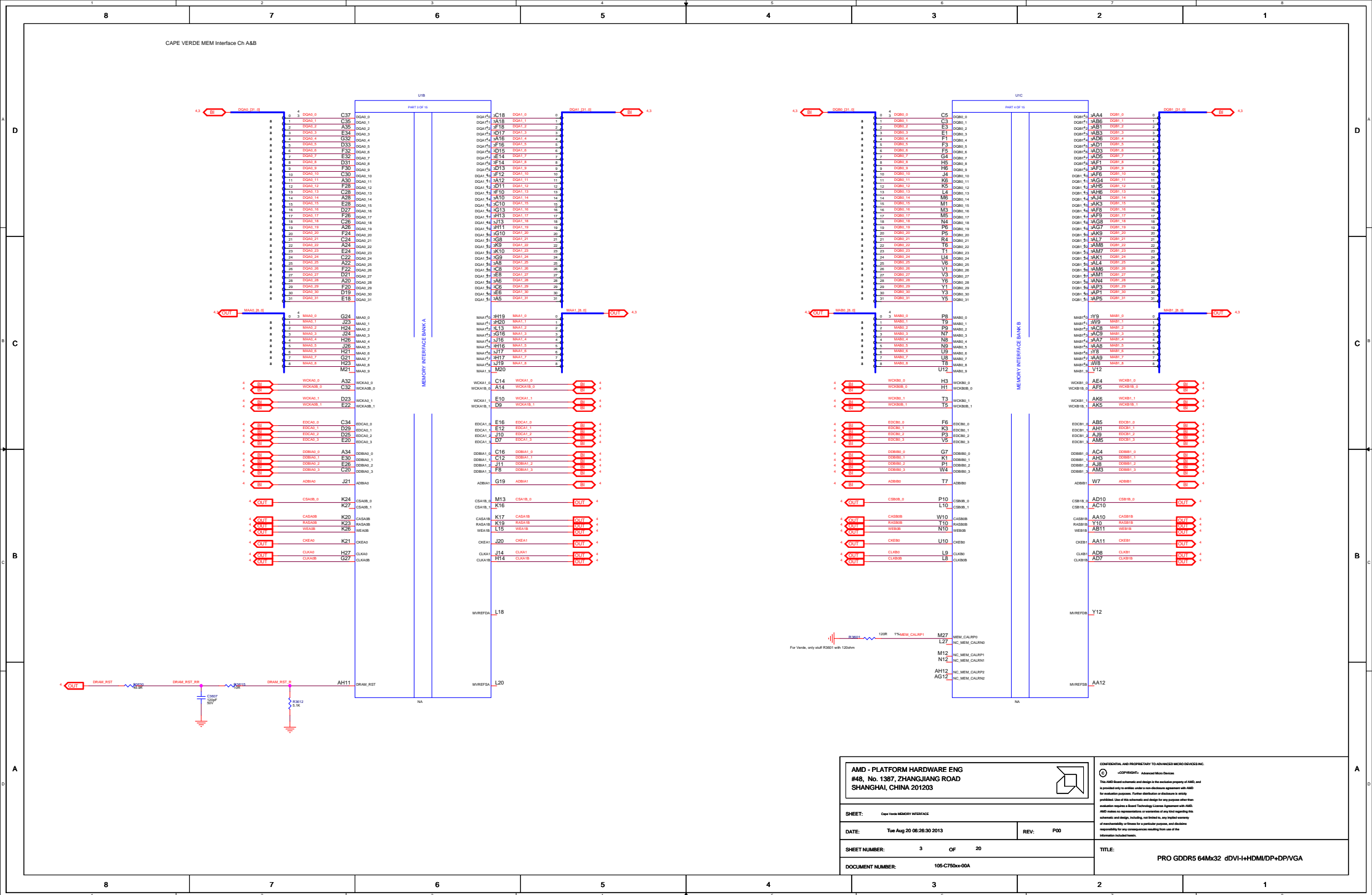
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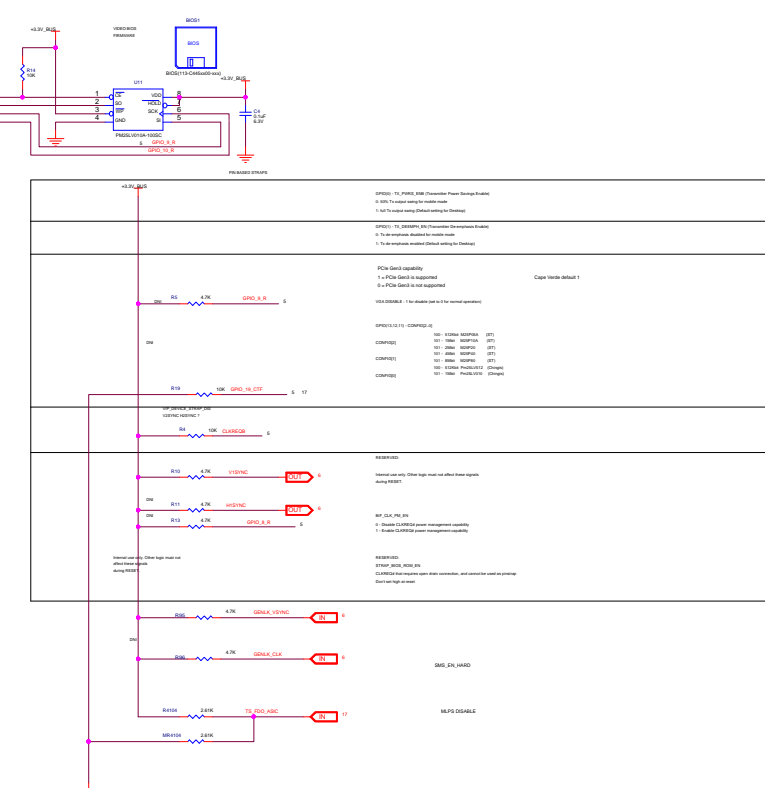
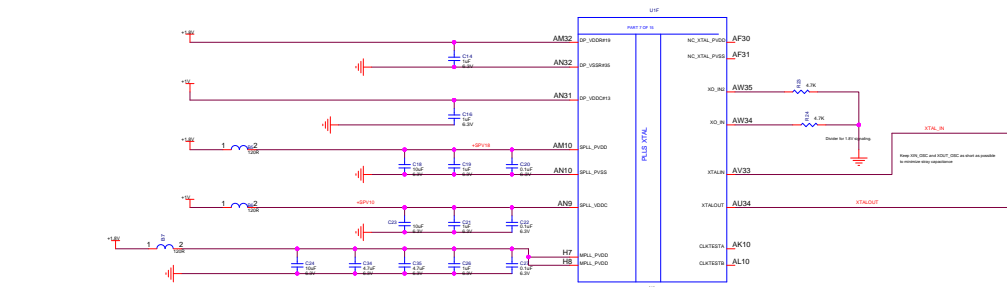
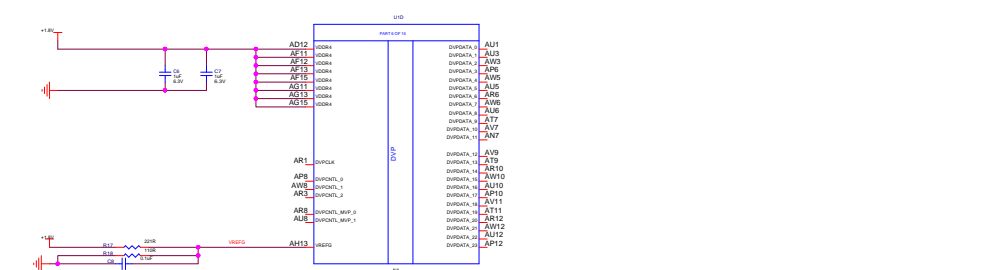
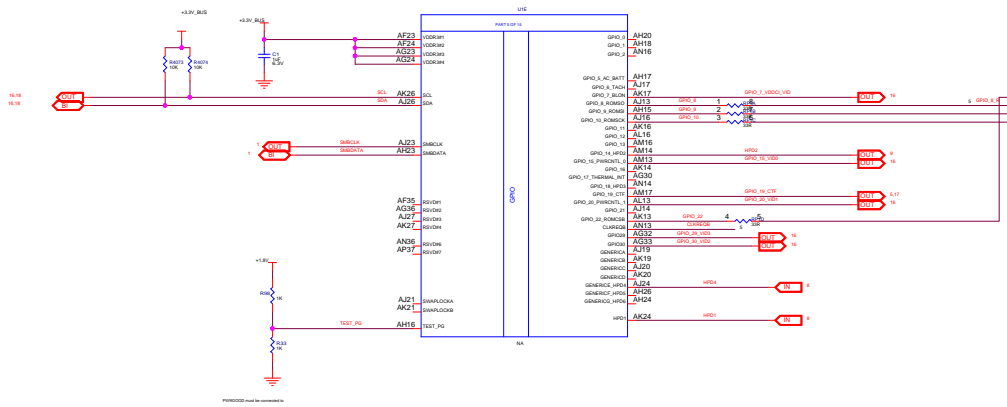
REV: P00


SHEET NUMBER: 2 OF 20

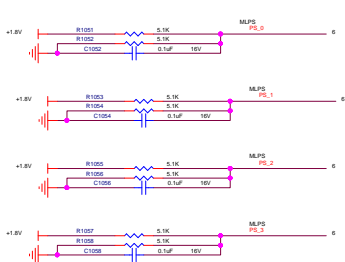
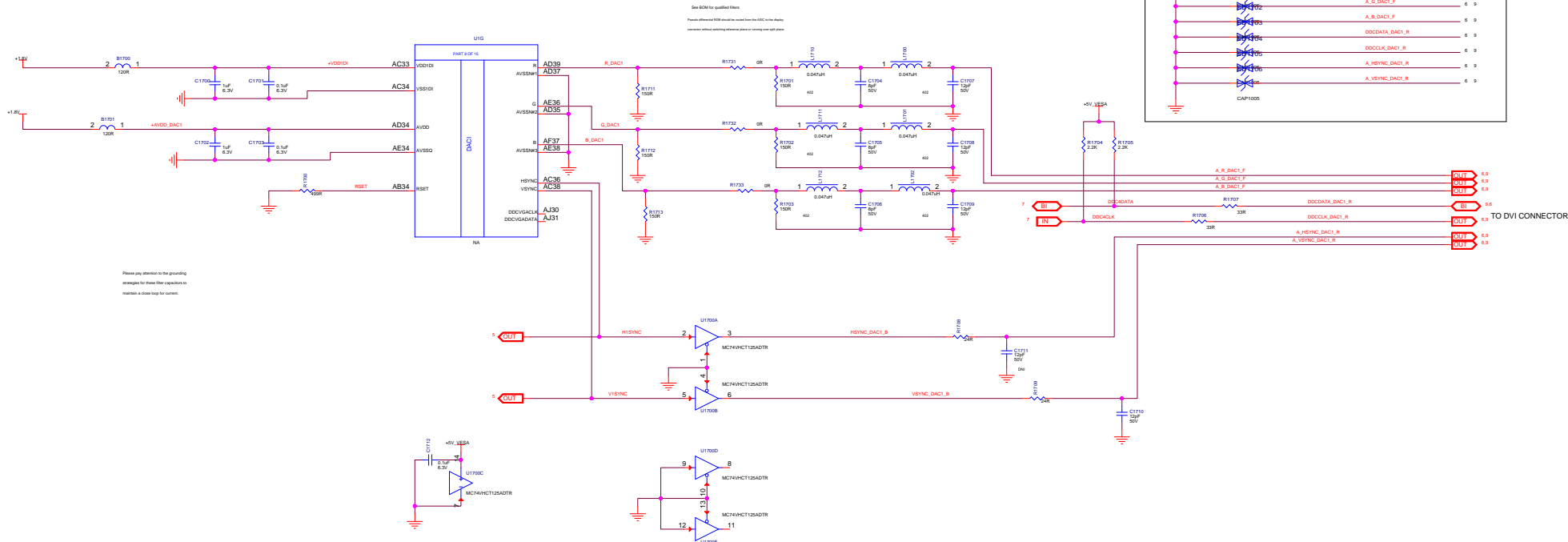
TITLE: PRO GDDR5 64Mx32 dDVI-I+HDMI/DP+DP/VGA

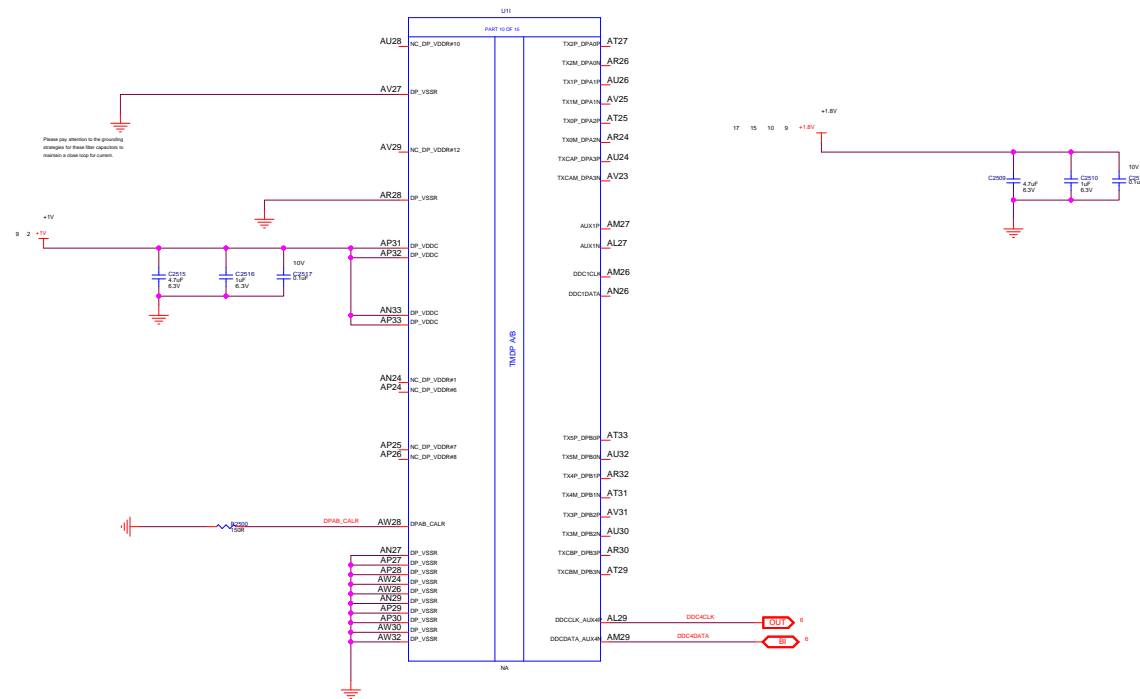
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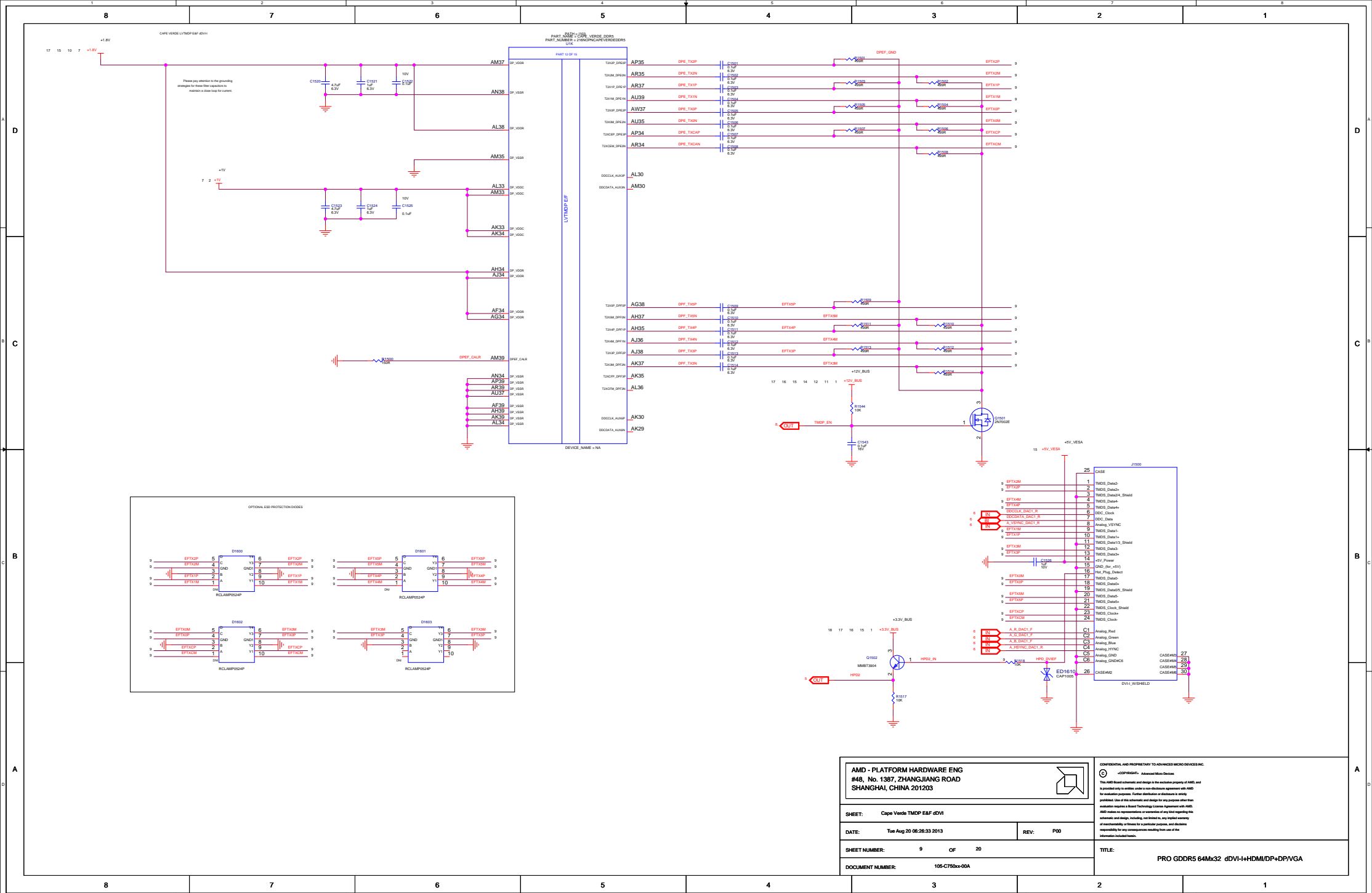


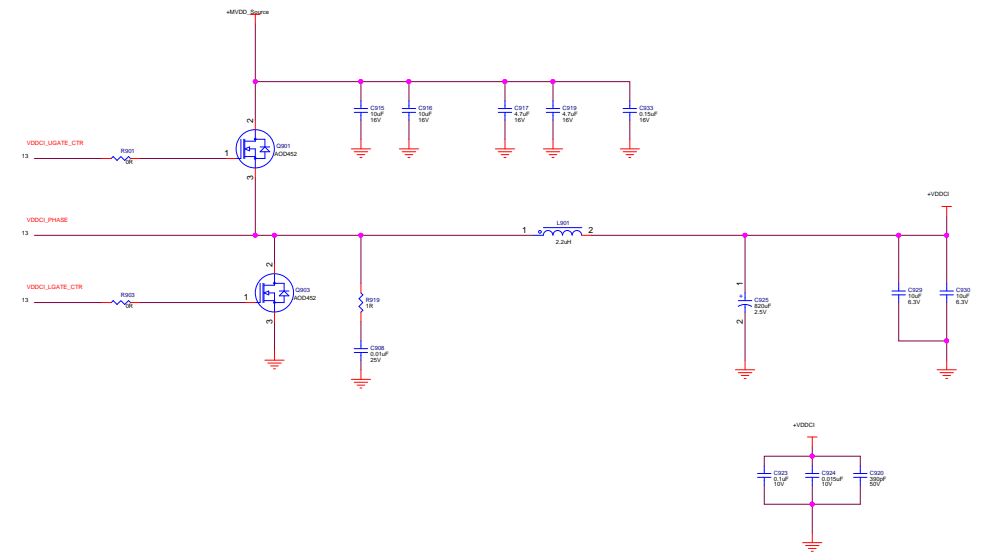
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SHEET: Cap Item 0000 0000 00 00		DATE: Tue Aug 20 06:26:32 2013		REV: P00	
SHEET NUMBER: 5 OF 30		TITLE: PRO GDDR5 64Mb/32 dVt/4+HDMI/DP+DP/IVA			
DOCUMENT NUMBER: 105-C7000v-00A					
NOTE: 0000					





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<p>SHEET: Cape Verde TMDP AR unused</p>	<p>REV: P00</p>	
<p>DATE: Tue Aug 20 06:26:32 2013</p>	<p>TITLE: PRO GDDR5 64Mx32 dDVI-I+HDMI/DP+DP/AGRA</p>	
<p>SHEET NUMBER: 7 OF 20</p>		
<p>DOCUMENT NUMBER: 105-C750xx-00A</p>		





VDDCI

REV: P00

OF 20

105-C750xx-00A

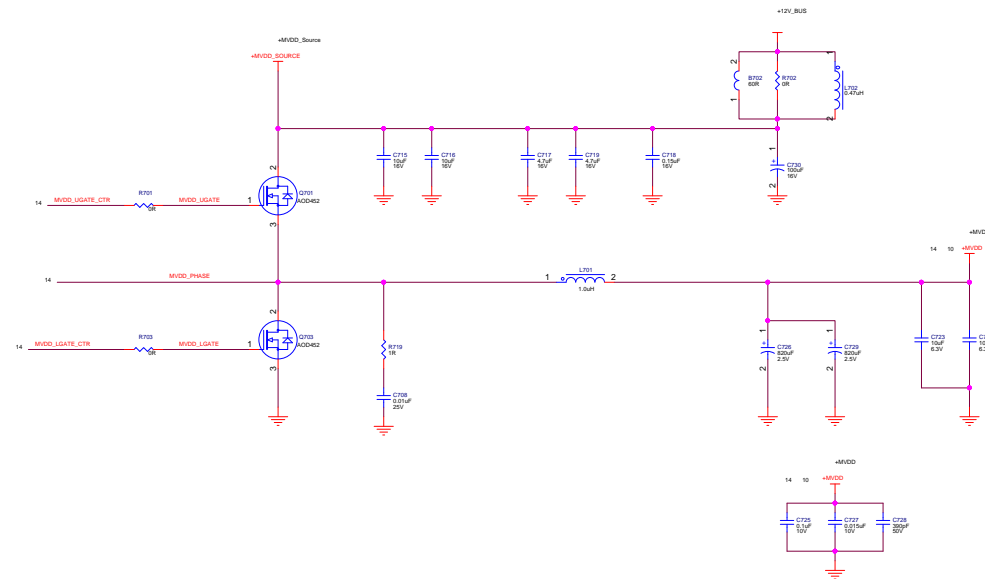
3

3

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PRO GDDR5 64Mx32 dDVI-I+HDMI/DP+DP/VGA

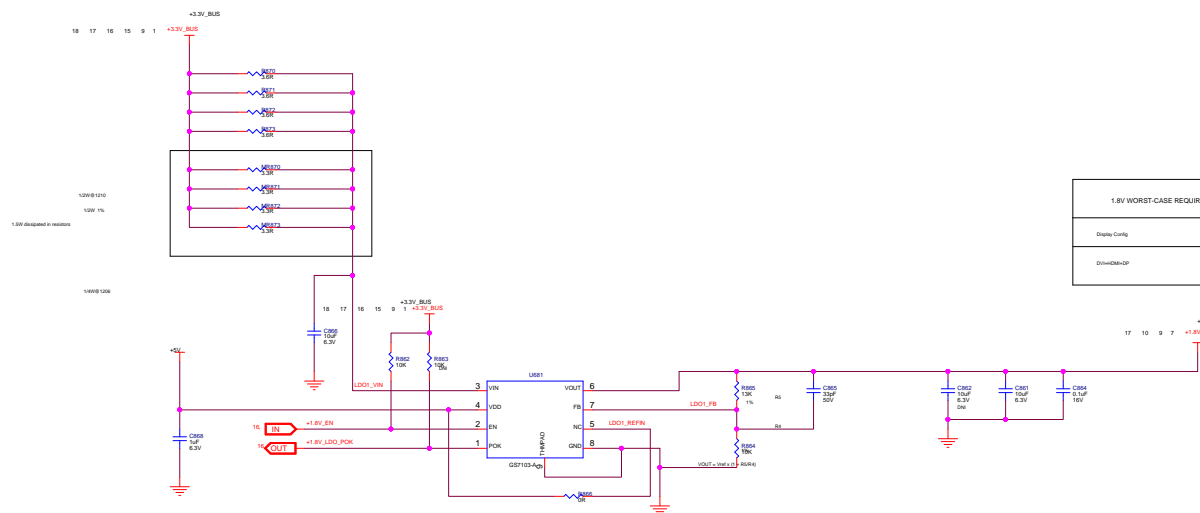


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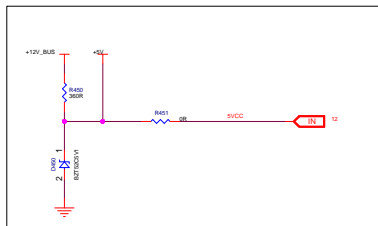
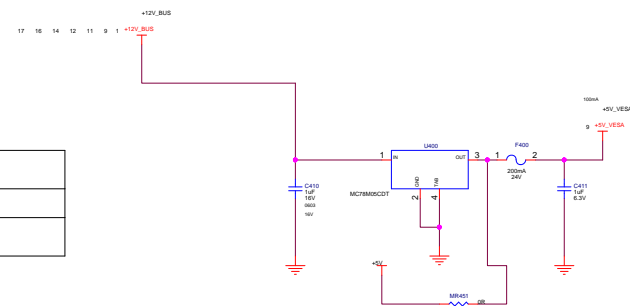
Linear Regulators

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TbV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

Regulators for +5V, +5V_VESA and +5V_VESA2



1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DP+DP-@EP	1380mA



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SHEET: Linear Regulators

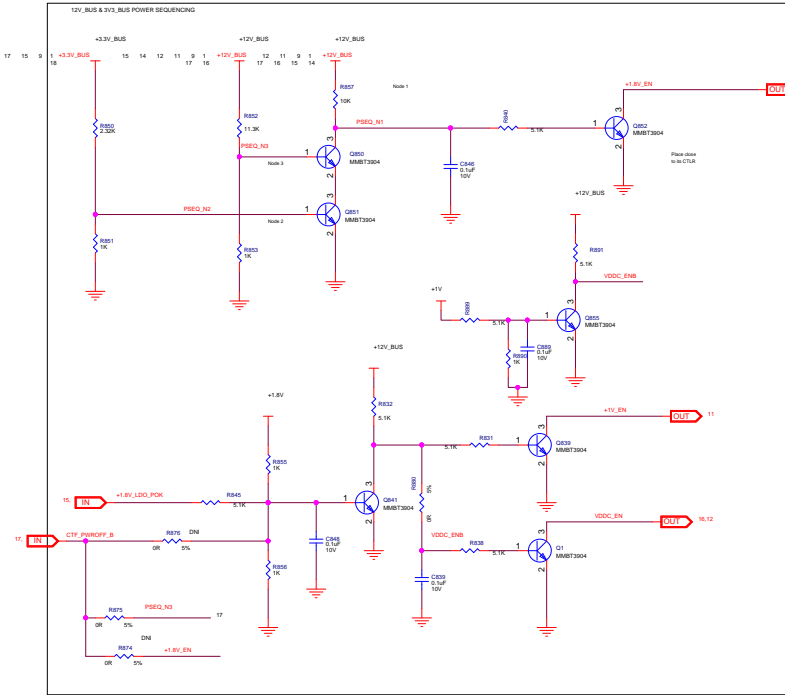
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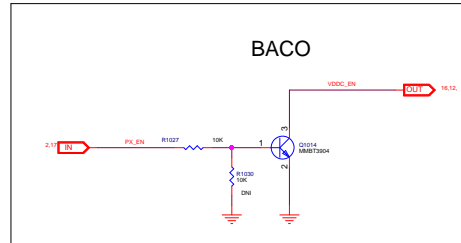
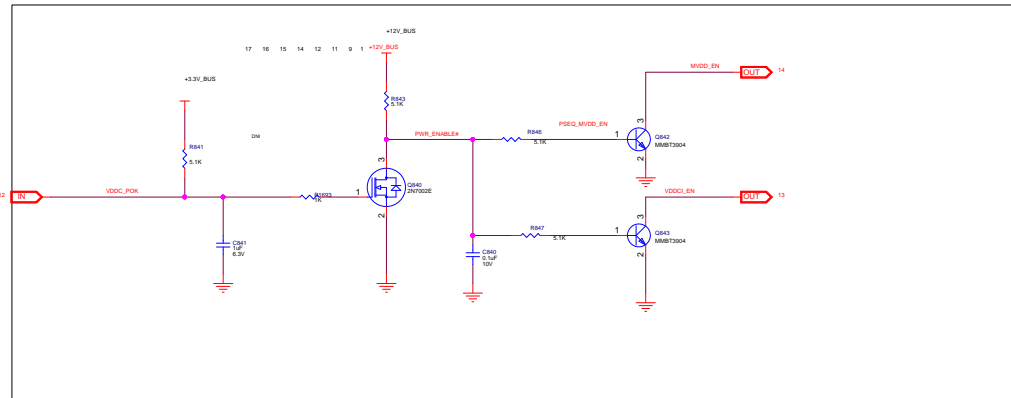
SHEET NUMBER: 15 OF 20

TITLE: PRO GDDR5 64Mx32 dDVI-I+HDMI/DP+DP/VGA

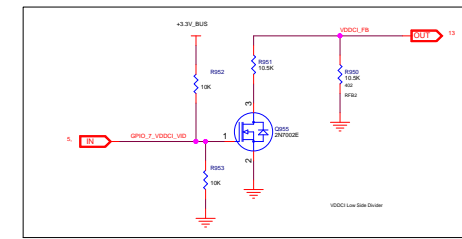
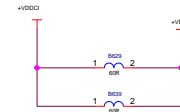
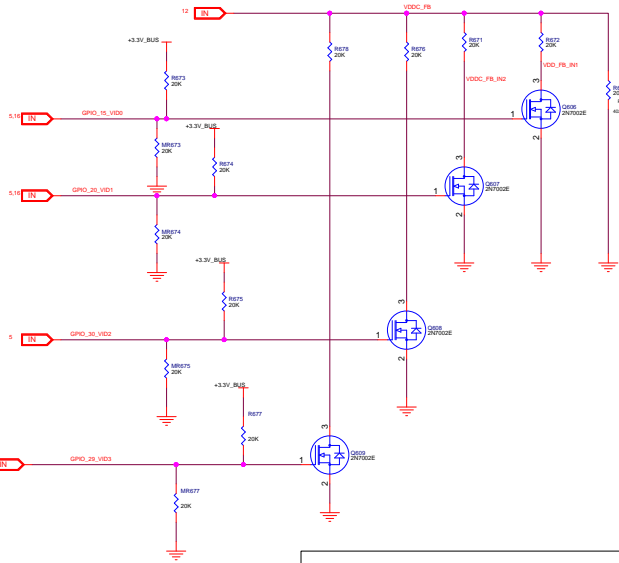
Power Management - Power Gating and Dynamic Voltage Control



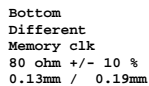
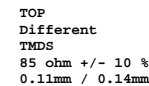
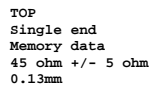
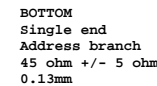
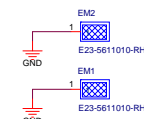
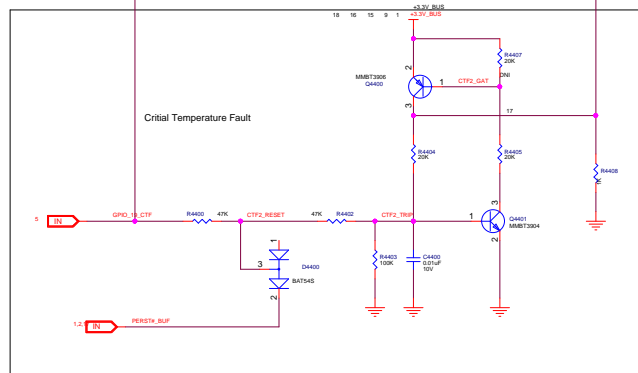
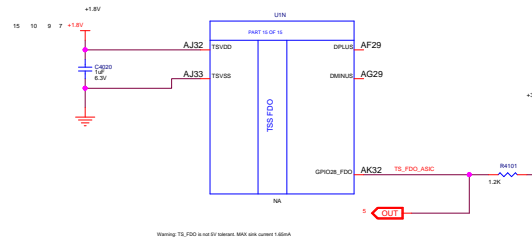
POWER SEQUENCING CIRCUIT



VDDC Low Side Divider






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SHEET: PWR MGMT & SEQ		REV: P00	
DATE: Tue Aug 20 08:26:36 2013		REV: P00	
SHEET NUMBER: 16 OF 20		TITLE: PRO GDDR5 64Mx32 dVLI-I+HDMI/DP+DP/VGA	
DOCUMENT NUMBER: 105-C750xx-00A			




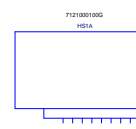
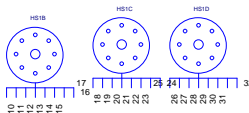
Socket	8000034000G	
Bracket	80000015A0G	VGA DP DVI
Bracket	80000013C0G	DP DP DVI
Bracket	8000001000G	VGA HDMI DVI
	8000001800G	DP HDMI DVI
Fanrail	7121000100G 7120000100G 7120100100G	For 75W board

Part 012 Components

<p>ASSY-SCREW020</p>  <p>70200001000G</p>	<p>ASSY-SCREW0201</p>  <p>70200000000G</p>	<p>ASSY-SCREW0202</p>  <p>70200001700G</p>
--	---	---

Braced Connections

<p>MF200</p>  <p>1 8</p> <p>80200011000G 80200011000G 80200011000G</p>	<p>80200011000G (B1)</p> <p>BRACKET</p>	<p>80200011800G (B2)</p> <p>BRACKET</p>	<p>80200011500G (B3)</p> <p>BRACKET</p>	<p>80200011600G (B4)</p> <p>BRACKET</p>
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SHANGHAI, CHINA 201203

SHEET: Mech/Thermal Management	
DATE: Tue Aug 20 06:26:35 2013	REV: P00
SHEET NUMBER: 17 OF 20	
DOCUMENT NUMBER: 105-C750xx-00A	

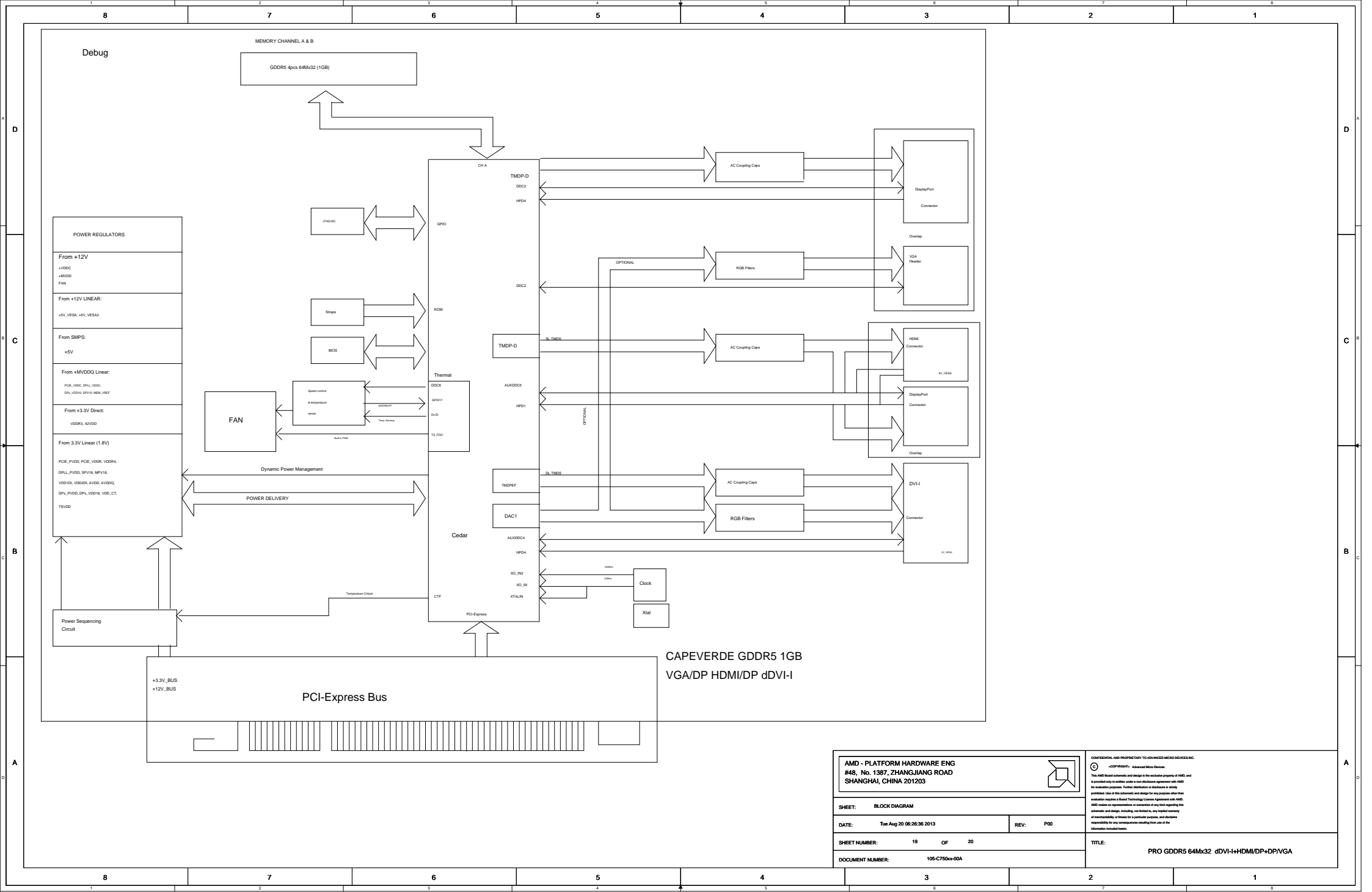
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TITLE: PRO GDDR5 64Mx32 dDVI-I+HDMI/DP+DP/VGA

Figure 1: JTAG pin connections for the AD9288. The diagram shows the JTAG pinout of the AD9288 (left) and the corresponding connections to the AD9288 (right). The AD9288 has pins for TESTEN, JTAG_TMS, JTAG_TCK, JTAG_TDI, JTAG_TDO, and JTAG_TMS. The AD9288 has pins for TESTEN, JTAG_TMS, JTAG_TCK, JTAG_TDI, JTAG_TDO, and JTAG_TMS. The connections are: TESTEN to AD9288 TESTEN, JTAG_TMS to AD9288 JTAG_TMS, JTAG_TCK to AD9288 JTAG_TCK, JTAG_TDI to AD9288 JTAG_TDI, JTAG_TDO to AD9288 JTAG_TDO, and JTAG_TMS to AD9288 JTAG_TMS. The diagram also shows the connection of the JTAG_TMS pin to the AD9288 JTAG_TMS pin.



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SHEET: BLOCK DIAGRAM			TITLE: PRO GDDR5 64Mx32 dVI-I+HDMI/DP+DP/VGA		
DATE: Tue Aug 20 08:26:36 2013			REV: P00		
SHEET NUMBER: 19 OF 20					
DOCUMENT NUMBER: 105-C750xx-00A					

