1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0001231154	ENGINEERING RELEASED	2011-09-06

J2 MLB - DVT OK2FAB

LAST_MODIFIED=Tue Sep 6 17:35:11 2011

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table of Contents	MIKE	NA
2	2	BLOCK DIAGRAM: SYSTEM	J2DEV	N/A
3	4	BOM TABLES	MIKE	N/A
4	6	AP: MAIN	MIKE	N/A
5	7	AP: I/Os	JOE	N/A
6	8	AP: NAND	MIKE	N/A
7	9	AP: TV,DP,MIPI	JOE	01/13/2011
8	10	AP: DDR	MIKE	N/A
9	11	AP: POWER	MIKE	N/A
10	12	AP: MISC & ALIASES	ALEX	N/A
11	13	AP: VIDEO BUFFER,BB USB MUXES	CHOPIN	12/10/2010
12	14	NAND	MIKE	N/A
13	16	DDR 0 AND 1	MIKE	06/21/2010
14	17	DDR 2 AND 3	MIKE	06/21/2010
15	21	MLB ALIASES/CONNECTIONS	ALEX	09/30/2010
16	22	VIDEO: EDP CONNECTOR	JOE	01/19/2011
17	30	GRAPE: GROUNDHOG,CONN,BOOST	RAMSIN	12/17/2010
18	31	GRAPE: Z1, Z2	RAMSIN	12/17/2010
19	36	AUDIO: L63B CODEC	KAVITHA	02/03/2011
20	37	AUDIO: SPEAKER AMP	KAVITHA	02/03/2011
21	38	AUDIO: HEADPHONE OUT	KAVITHA	02/03/2011
22	42	AUDIO: DETECT/MIC BIAS	KAVITHA	02/03/2011
23	43	AUDIO: HP/MIC FILTERS	KAVITHA	02/03/2011
24	54	CONNECTOR: SENSOR	MARK	01/11/2011
25	55	SENSOR PANEL FILTERS 1	MARK	01/11/2011
26	56	SENSOR PANEL FILTERS 2	MARK	01/11/2011
27	57	IO FLEX: DOCK COMPONENTS	JOE	01/19/2011
28	58	DISPLAY PORT MISC	JOE	01/19/2011
29	59	IO FLEX: B2B CONNECTOR	JOE	01/19/2011
30	60	CONNECTOR: X26	JOE	01/19/2011
31	61	WLAN BB & POWER	X26_WIFI_MIKE_BT	09/01/2011
32	62	WLAN 2.4GHZ AND ANT	X26_WIFI_MIKE_BT	09/01/2011
33	63	WLAN 5GHZ AND TEST POINTS	X26_WIFI_MIKE_BT	09/01/2011
34	75	POWER: BATTERY CONNECTOR	MADHAVI	01/13/2011
35	80	POWER ALIASES	MADHAVI	01/13/2011
36	81	POWER: AMELIA PMU	MADHAVI	01/13/2011
37	82	POWER: AMELIA PMU	MLB	01/14/2011
38	83	POWER: AMELIA VSS	MADHAVI	01/13/2011
39	90	DEBUG AND MISC	ALEX	10/04/2010
40	93	FCT/ICT TEST/BRACKETS	ALEX	10/04/2010
41	150	CONSTRAINTS: MLB RULES	MIKE	01/21/2011
42	151	CONSTRAINTS: LOW SPEED BUS	MIKE	01/21/2011
43	152	CONSTRAINTS: DISPLAY/AUDIO	MIKE	01/21/2011
44	153	CONSTRAINTS: DDR/FMI	MIKE	01/21/2011
45	154	CONSTRAINTS: POWER / GND	MIKE	01/21/2011
46	155	CONSTRAINTS: DEBUG	MIKE	01/21/2011
47	156	FUNC TEST POINTS	MIKE	01/21/2011
48	157	FUNC TEST POINTS	MIKE	01/21/2011

DRAWING
DRAWING
MLB

Schematic / PCB #'s

H4G

DUAL-CORE ARM CORTEX-A9 W/ SMP 950 MHZ

GPU
QUAD-CORE IMG SGX543-MP2

AUDIO
AE2
ARM A5 CPU

Z2
CSA 31

Z1
CSA 31

GROUNDHOG
CSA 30

LPDDR2
1 GBYTE
4X32-BIT
400MHZ/800MB/S

DISPLAY/
TOUCH PANEL
RESOLUTION: 2048X1536
BACKLIGHT

PMU
AMELIA
I2C 8'H78
CSA 81,82

BATTERY
CSA 75

HALL EFF
BUTTON FLEX

PROX SENSOR
I2C 8'H58
SENSOR PANEL

COMPASS
I2C 8'H1C
SENSOR PANEL

GYRO
I2C 8'HD0
SENSOR PANEL

ACCELEROMETER
I2C 8'H32
SENSOR PANEL

ALS
I2C 8'H72
VGA FLEX

NAND FLASH
PPN1.0
CSA 14

NAND FLASH
PPN1.0
CSA 14

SPI1
EDP
UART5
DWI
I2C0
I2C1
I2C2
FMI0 FMI1
FMI2 FMI3

ISP_I2C1
MIPI1C
ISP_I2C0
MIPI0C
HSIC1_1
UART3
UART6
HSIC0_1
UART1
SPI2
USB2.0
UART0
DISPLAYPORT
VIDEO DAC
I2S2
I2S0
I2S3

FF CAMERA
VGA FLEX

REAR CAMERA
VA5/8 FLEX

MIMO
WIFI/BT
BT_I2S
CSA 61-64

WIFI ANT 1

WIFI/BT ANT 2

X26
CELLULAR/GPS
HSIC1
USART
IPC
CSA 60

PRIMARY CELLULAR ANT

DIVERSITY CELLULAR ANT

GPS ANT

30-PIN
DOCK
CSA 57

AMP

AUDIO CODEC
L63B
VSP
ASP
XSP
LINEOUT
I2C 8'H94
CSA 36

AMP

AMP

SPEAKER

MIC

MUX
US/CHINA
I2C 8'H76

EXT MIC

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD
32GB_PROD
64GB_PROD
128GB_PROD

DEVELOPMENT_JTAG
DEVELOPMENT_JTAG_TAP
JTAG_DAP

SPEAKER
INTERNAL_MIC

NAND_IO_1V8
NAND_IO=3V3

SNOTE
DEV
MLB
J2

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE
AUDIO	SPEAKER,INTERNAL_MIC

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR 639-2352 (J1 16G)	EEEE_DNKT	CRITICAL	EEEE_J1_16G
825-7691	1	EEEE FOR 639-2058 (J1 32G)	EEEE_DM2N	CRITICAL	EEEE_J1_32G
825-7691	1	EEEE FOR 639-2059 (J1 64G)	EEEE_DM2P	CRITICAL	EEEE_J1_64G
825-7691	1	EEEE FOR 639-2353 (J2 16G)	EEEE_DNKV	CRITICAL	EEEE_J2_16G
825-7691	1	EEEE FOR 639-1572 (J2 32G)	EEEE_DHWV	CRITICAL	EEEE_J2_32G
825-7691	1	EEEE FOR 639-1871 (J2 64G)	EEEE_DKQL	CRITICAL	EEEE_J2_64G
825-7691	1	EEEE FOR 639-1870 (J2 128G)	EEEE_DKQK	CRITICAL	EEEE_J2_128G
825-7691	1	EEEE FOR 639-2844 (J2A 16G)	EEEE_DRJQ	CRITICAL	EEEE_J2A_16G
825-7691	1	EEEE FOR 639-2826 (J2A 32G)	EEEE_DRF6	CRITICAL	EEEE_J2A_32G
825-7691	1	EEEE FOR 639-2827 (J2A 64G)	EEEE_DRF5	CRITICAL	EEEE_J2A_64G

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-2105	1	FENCE,NAND,TOP,MLB,J2	PD_FENCE_NAND	CRITICAL	
806-1857	1	FENCE,LARGE,TOP,MLB,J2	PD_FENCE_LARGE	CRITICAL	
806-2349	1	FENCE,SMALLER,TOP,MLB,J2	PD_FENCE_SMALL	CRITICAL	
806-1860	1	FENCE,1,BTM,MLB,J2	PD_FENCE_BTM1	CRITICAL	
806-1865	1	FENCE,2,BTM,MLB,J2	PD_FENCE_BTM2	CRITICAL	
806-2352	1	FENCE,SMALLER,BTM,MLB,J2	PD_FENCE_BTM3	CRITICAL	

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8773	1	SCH,MLB,J2	SCH1	CRITICAL	?
820-2996	1	PCBF,MLB,J2	PCB1	CRITICAL	?
085-3058	1	DEV BOM,MLB,J2	DEV1		?

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0533	1	IC,SOC,H4G,FCBGA1225	U0600	CRITICAL	?

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0561	1	IC,PMU,AMELIA,D1974AB	U8100	CRITICAL	?

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0579	2	SDRAM,LPDDR2,512MB,SAMSUNG 46NM	U1600,U1700	CRITICAL	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0580	333S0579		U1600,U1700	LPDDR2,HYNIX 44NM
333S0581	333S0579		U1600,U1700	LPDDR2,ELPIDA 45NM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0781	1	HYNIX 26NM PPN1.0 16GB	U1400	CRITICAL	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0804	335S0781	16GB_PROD	U1400	TOSHIBA 24NM PPN1.0

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0781	2	HYNIX 26NM PPN1.0 16GB	U1400,U1410	CRITICAL	32GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0804	335S0781	32GB_PROD	U1400,U1410	TOSHIBA 24NM PPN1.0

64GB FLASH CONFIGURATIONS

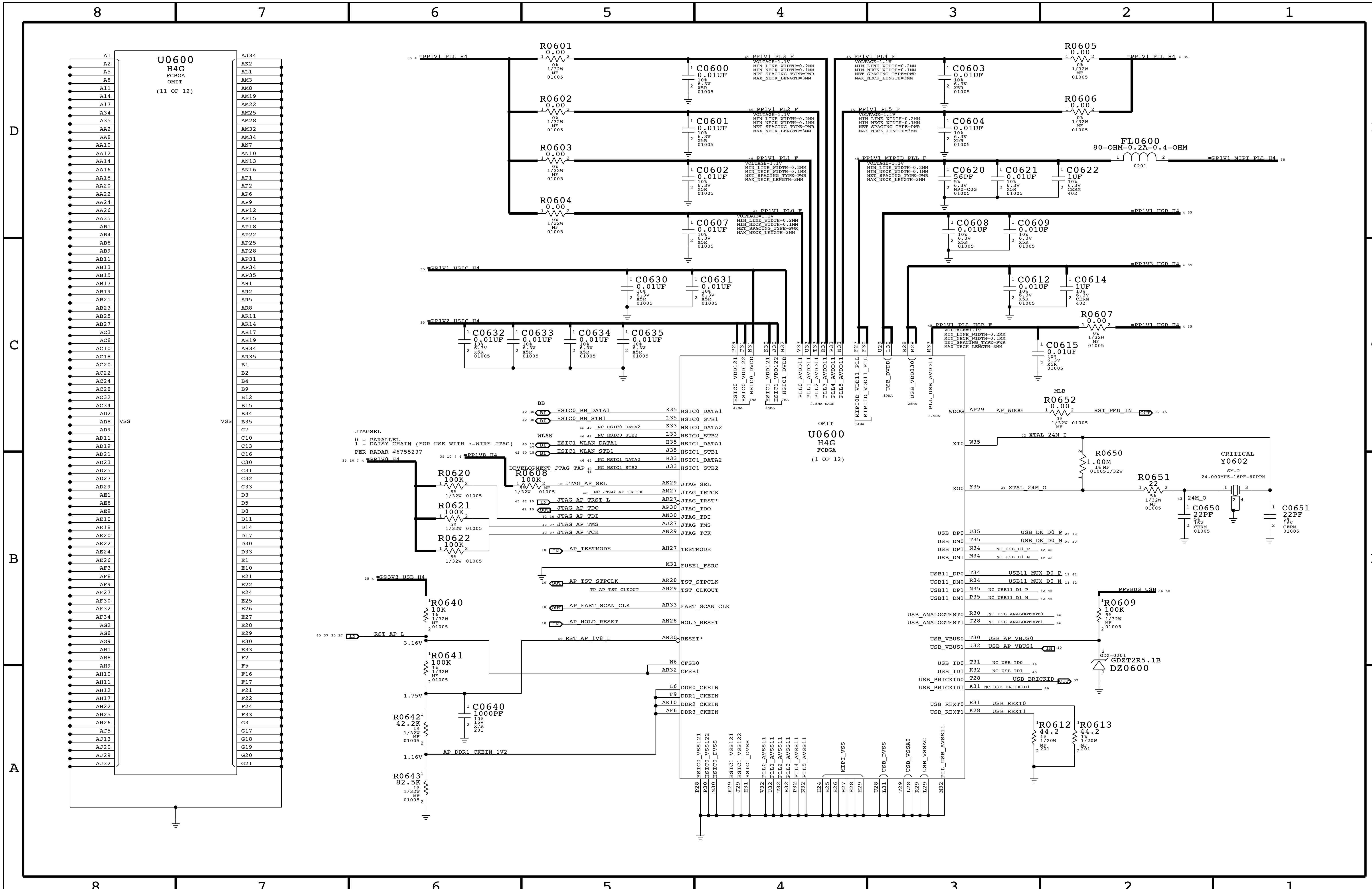
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0782	2	HYNIX 26NM PPN1.0 32GB	U1400,U1410	CRITICAL	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0805	335S0782	64GB_PROD	U1400,U1410	TOSHIBA 24NM PPN1.0

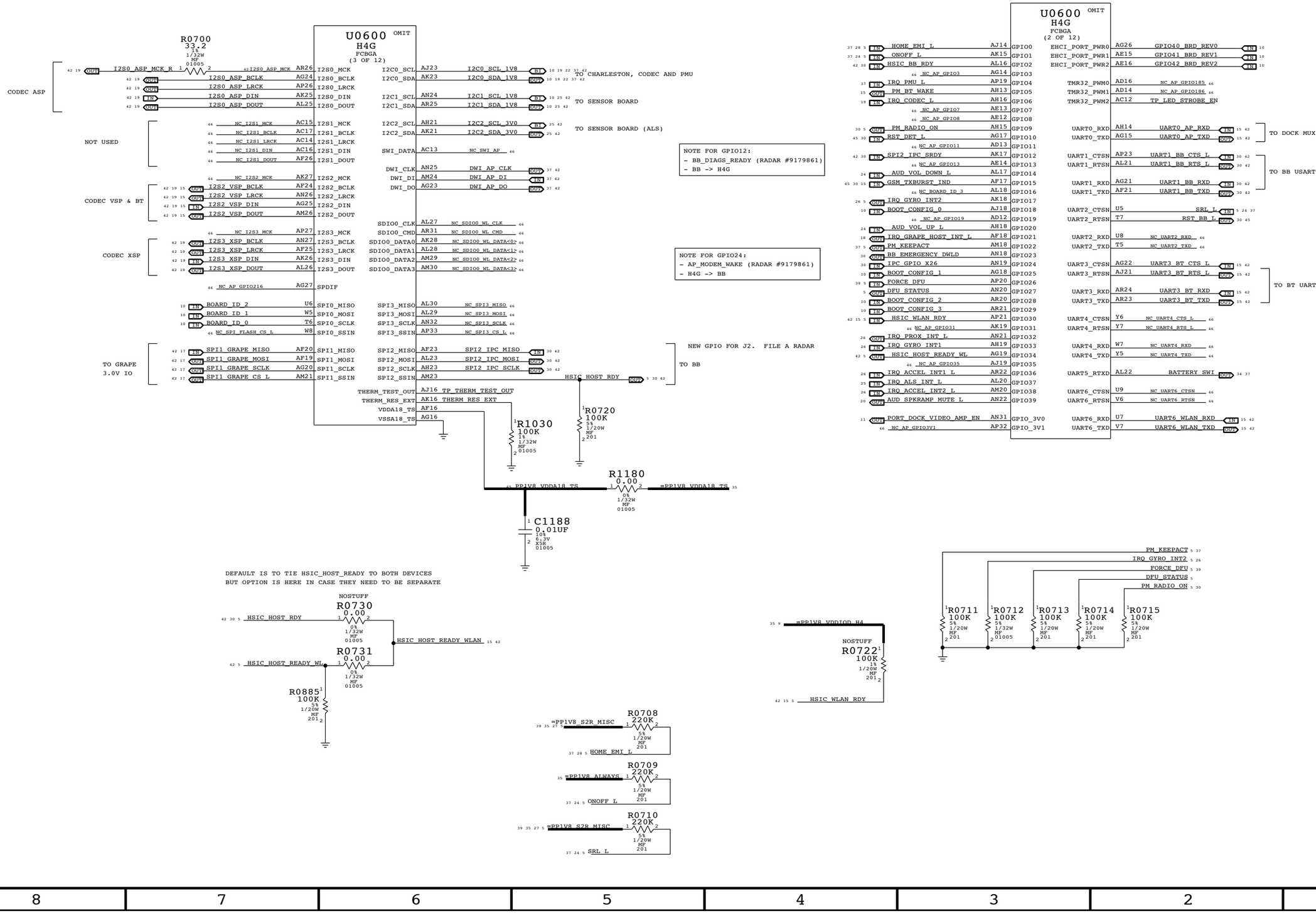
128GB FLASH CONFIGURATIONS

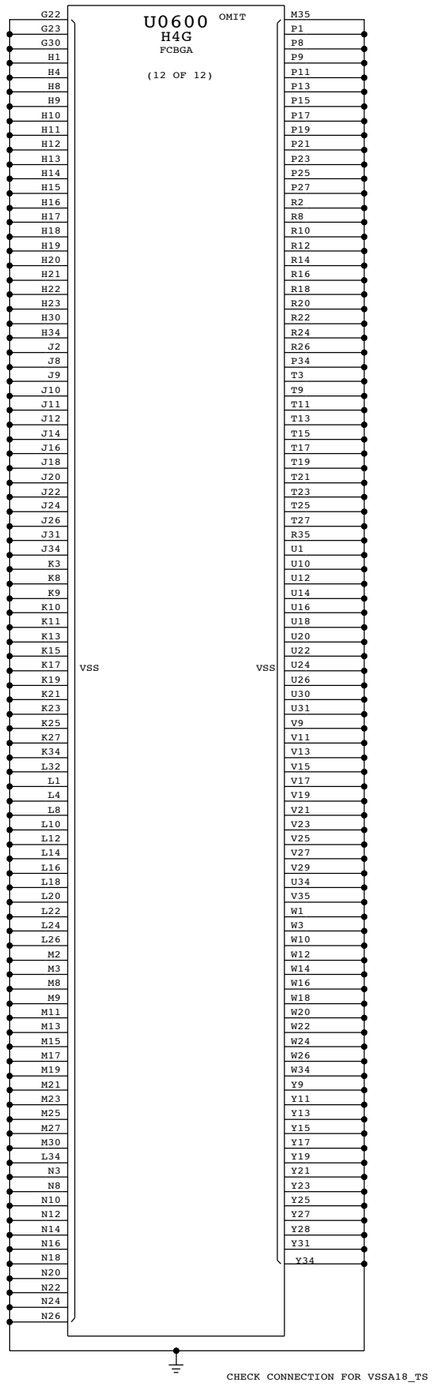
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0814	2	HYNIX 26NM PPN1.0 64GB	U1400,U1410	CRITICAL	128GB_PROD

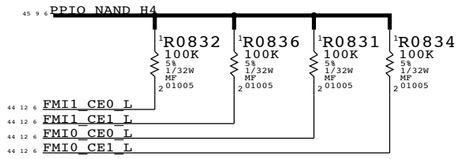
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0806	335S0814	128GB_PROD	U1400,U1410	TOSHIBA 24NM PPN1.0

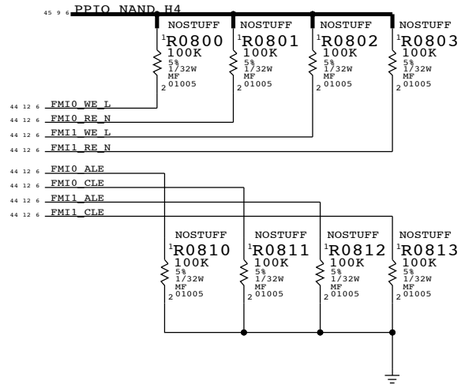


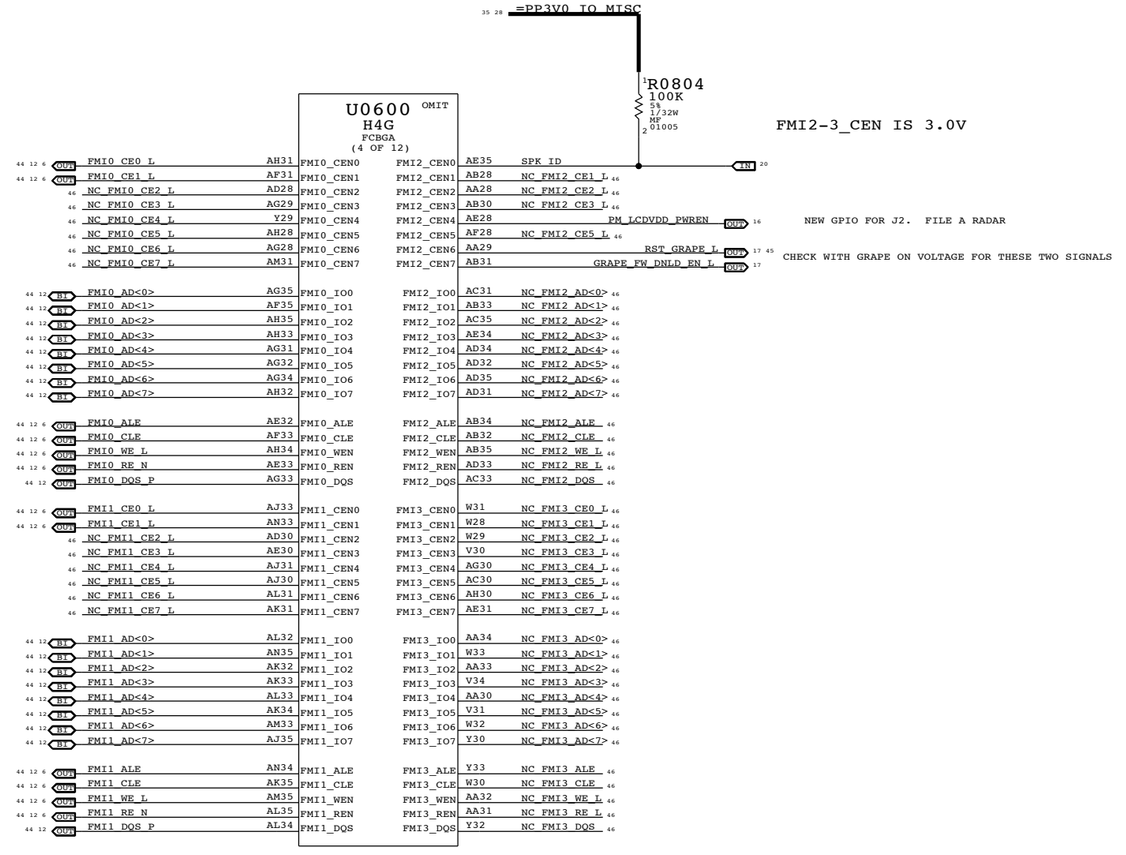
U0600
H4G
FCBGA
OMIT
(11 OF 12)
VSS
R0601
R0602
R0603
R0604
R0605
R0606
R0607
C0600
C0601
C0602
C0603
C0604
C0607
C0608
C0609
C0612
C0614
C0615
C0620
C0621
C0622
C0630
C0631
C0632
C0633
C0634
C0635
FL0600
80-OHM-0.2A-0.4-OHM
=PP1V1_PLL_H4
=PP1V1_MIPI_PLL_H4
=PP1V1_USB_H4
=PP3V3_USB_H4
=PP1V1_HSIC_H4
=PP1V2_HSIC_H4
PP1V1_PLL_USB_F
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3MM
BB
WLAN
HSIC0_BB_DATA1
HSIC0_BB_STB1
HSIC1_WLAN_DATA1
HSIC1_WLAN_STB1
JTAGSEL
0 = PARALLEL
1 = DAISY CHAIN (FOR USE WITH 5-WIRE JTAG)
PER RADAR #6755237
DEVELOPMENT JTAG_TAP
R0608
R0620
R0621
R0622
JTAG_AP_SEL
JTAG_AP_TRST_L
JTAG_AP_TDO
JTAG_AP_TDI
JTAG_AP_TMS
JTAG_AP_TCK
AP_TESTMODE
AP_TST_STPCLK
TP_AP_TST_CLKOUT
AP_FAST_SCAN_CLK
AP_HOLD_RESET
RST_AP_L
RST_AP_1V8_L
AP_DDR1_CKEIN_1V2
R0640
R0641
R0642
R0643
C0640
=PP3V3_USB_H4
OMIT
U0600
H4G
FCBGA
(1 OF 12)
MLB
R0652
AP_WDOG
RST_PMU_IN
XTAL_24M_I
XTAL_24M_O
R0650
R0651
CRITICAL
Y0602
24.000MHZ-16PF-60PPM
C0650
C0651
USB_DK_D0_P
USB_DK_D0_N
USB11_MUX_D0_P
USB11_MUX_D0_N
PPVBUS_USB
R0609
USB_AP_VBUS0
USB_AP_VBUS1
USB_BRICKID
USB_REXT0
USB_REXT1
GDZT2R5.1B
DZ0600
R0612
R0613


U0600 OMIT
H4G
FCBGA
(3 OF 12)
CODEC ASP
I2S0_ASP_MCK_R
I2S0_ASP_MCK
I2S0_ASP_BCLK
I2S0_ASP_LRCK
I2S0_ASP_DIN
I2S0_ASP_DOUT
R0700 33.2 1% 1/32W MF 01005
NOT USED
CODEC VSP & BT
I2S2_VSP_BCLK
I2S2_VSP_LRCK
I2S2_VSP_DIN
I2S2_VSP_DOUT
CODEC XSP
I2S3_XSP_BCLK
I2S3_XSP_LRCK
I2S3_XSP_DIN
I2S3_XSP_DOUT
SPDIF
BOARD_ID_2
BOARD_ID_1
BOARD_ID_0
TO GRAPE 3.0V IO
SPI1_GRAPE_MISO
SPI1_GRAPE_MOSI
SPI1_GRAPE_SCLK
SPI1_GRAPE_CS_L
TO CHARLESTON, CODEC AND PMU
TO SENSOR BOARD
TO SENSOR BOARD (ALS)
NOTE FOR GPIO12:
- BB_DIAGS_READY (RADAR #9179861)
- BB -> H4G
NOTE FOR GPIO24:
- AP_MODEM_WAKE (RADAR #9179861)
- H4G -> BB
NEW GPIO FOR J2. FILE A RADAR
TO BB
HSIC_HOST_RDY
R0720 100K 5% 1/20W MF 201
R1030 100K 1% 1/32W MF 01005
R1180 0.00 0% 1/32W MF 01005
C1188 0.01UF 10% 6.3V X5R 01005
DEFAULT IS TO TIE HSIC_HOST_READY TO BOTH DEVICES
BUT OPTION IS HERE IN CASE THEY NEED TO BE SEPARATE
NOSTUFF
R0730 0.00 0% 1/32W MF 01005
R0731 0.00 0% 1/32W MF 01005
HSIC_HOST_RDY
HSIC_HOST_READY_WL
HSIC_HOST_READY_WLAN
R0885 100K 5% 1/20W MF 201
R0708 220K 5% 1/20W MF 201
R0709 220K 5% 1/20W MF 201
R0710 220K 5% 1/20W MF 201
=PP1V8_S2R_MISC
=PP1V8_ALWAYS
HOME_EMI_L
ONOFF_L
SRL_L
U0600 OMIT
H4G
FCBGA
(2 OF 12)
HOME_EMI_L
ONOFF_L
HSIC_BB_RDY
IRQ_PMU_L
PM_BT_WAKE
IRQ_CODEC_L
PM_RADIO_ON
RST_DET_L
SPI2_IPC_SRDY
AUD_VOL_DOWN_L
GSM_TXBURST_IND
IRQ_GYRO_INT2
BOOT_CONFIG_0
AUD_VOL_UP_L
IRQ_GRAPE_HOST_INT_L
PM_KEEPACT
BB_EMERGENCY_DWLD
IPC_GPIO_X26
BOOT_CONFIG_1
FORCE_DFU
DFU_STATUS
BOOT_CONFIG_2
BOOT_CONFIG_3
HSIC_WLAN_RDY
IRQ_PROX_INT_L
IRQ_GYRO_INT1
HSIC_HOST_READY_WL
IRQ_ACCEL_INT1_L
IRQ_ALS_INT_L
IRQ_ACCEL_INT2_L
AUD_SPKRAMP_MUTE_L
PORT_DOCK_VIDEO_AMP_EN
TMR32_PWM0
TMR32_PWM1
TMR32_PWM2
UART0_RXD
UART0_TXD
UART1_CTSN
UART1_RTSN
UART1_RXD
UART1_TXD
UART2_CTSN
UART2_RTSN
UART2_RXD
UART2_TXD
UART3_CTSN
UART3_RTSN
UART3_RXD
UART3_TXD
UART4_CTSN
UART4_RTSN
UART4_RXD
UART4_TXD
UART5_RTXD
UART6_CTSN
UART6_RTSN
UART6_RXD
UART6_TXD
TO DOCK MUX
TO BB USART
TO BT UART
=PP1V8_VDDIOD_H4
R0722 100K 1% 1/20W MF 201
HSIC_WLAN_RDY
PM_KEEPACT
IRQ_GYRO_INT2
FORCE_DFU
DFU_STATUS
PM_RADIO_ON
R0711 100K 5% 1/20W MF 201
R0712 100K 5% 1/32W MF 01005
R0713 100K 5% 1/20W MF 201
R0714 100K 5% 1/20W MF 201
R0715 100K 5% 1/20W MF 201


U0600 OMIT
H4G
FCBGA
(12 OF 12)
VSS
VSS
CHECK CONNECTION FOR VSSA18_TS


PPIO_NAND_H4
R0832 100K
R0836 100K
R0831 100K
R0834 100K
FMI1_CE0_L
FMI1_CE1_L
FMI0_CE0_L
FMI0_CE1_L


PPIO_NAND_H4
NOSTUFF
R0800 100K
R0801 100K
R0802 100K
R0803 100K
FMI0_WE_L
FMI0_RE_N
FMI1_WE_L
FMI1_RE_N
FMI0_ALE
FMI0_CLE
FMI1_ALE
FMI1_CLE
R0810 100K
R0811 100K
R0812 100K
R0813 100K


=PP3V0_IO_MISC
R0804 100K
FMI2-3_CEN IS 3.0V
U0600 OMIT
H4G
FCBGA
(4 OF 12)
FMI0_CE0_L
FMI0_CE1_L
NC_FMI0_CE2_L
NC_FMI0_CE3_L
NC_FMI0_CE4_L
NC_FMI0_CE5_L
NC_FMI0_CE6_L
NC_FMI0_CE7_L
FMI0_AD<0>
FMI0_AD<1>
FMI0_AD<2>
FMI0_AD<3>
FMI0_AD<4>
FMI0_AD<5>
FMI0_AD<6>
FMI0_AD<7>
FMI0_ALE
FMI0_CLE
FMI0_WE_L
FMI0_RE_N
FMI0_DQS_P
FMI1_CE0_L
FMI1_CE1_L
NC_FMI1_CE2_L
NC_FMI1_CE3_L
NC_FMI1_CE4_L
NC_FMI1_CE5_L
NC_FMI1_CE6_L
NC_FMI1_CE7_L
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FMI1_AD<3>
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FMI1_AD<6>
FMI1_AD<7>
FMI1_ALE
FMI1_CLE
FMI1_WE_L
FMI1_RE_N
FMI1_DQS_P
FMI0_CEN0
FMI0_CEN1
FMI0_CEN2
FMI0_CEN3
FMI0_CEN4
FMI0_CEN5
FMI0_CEN6
FMI0_CEN7
FMI0_IO0
FMI0_IO1
FMI0_IO2
FMI0_IO3
FMI0_IO4
FMI0_IO5
FMI0_IO6
FMI0_IO7
FMI0_ALE
FMI0_CLE
FMI0_WEN
FMI0_REN
FMI0_DQS
FMI1_CEN0
FMI1_CEN1
FMI1_CEN2
FMI1_CEN3
FMI1_CEN4
FMI1_CEN5
FMI1_CEN6
FMI1_CEN7
FMI1_IO0
FMI1_IO1
FMI1_IO2
FMI1_IO3
FMI1_IO4
FMI1_IO5
FMI1_IO6
FMI1_IO7
FMI1_ALE
FMI1_CLE
FMI1_WEN
FMI1_REN
FMI1_DQS
FMI2_CEN0
FMI2_CEN1
FMI2_CEN2
FMI2_CEN3
FMI2_CEN4
FMI2_CEN5
FMI2_CEN6
FMI2_CEN7
FMI2_IO0
FMI2_IO1
FMI2_IO2
FMI2_IO3
FMI2_IO4
FMI2_IO5
FMI2_IO6
FMI2_IO7
FMI2_ALE
FMI2_CLE
FMI2_WEN
FMI2_REN
FMI2_DQS
FMI3_CEN0
FMI3_CEN1
FMI3_CEN2
FMI3_CEN3
FMI3_CEN4
FMI3_CEN5
FMI3_CEN6
FMI3_CEN7
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FMI3_IO1
FMI3_IO2
FMI3_IO3
FMI3_IO4
FMI3_IO5
FMI3_IO6
FMI3_IO7
FMI3_ALE
FMI3_CLE
FMI3_WEN
FMI3_REN
FMI3_DQS
SPK_ID
NC_FMI2_CE1_L
NC_FMI2_CE2_L
NC_FMI2_CE3_L
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NC_FMI2_CE5_L
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NC_FMI2_RE_L
NC_FMI2_DQS
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NC_FMI3_CE1_L
NC_FMI3_CE2_L
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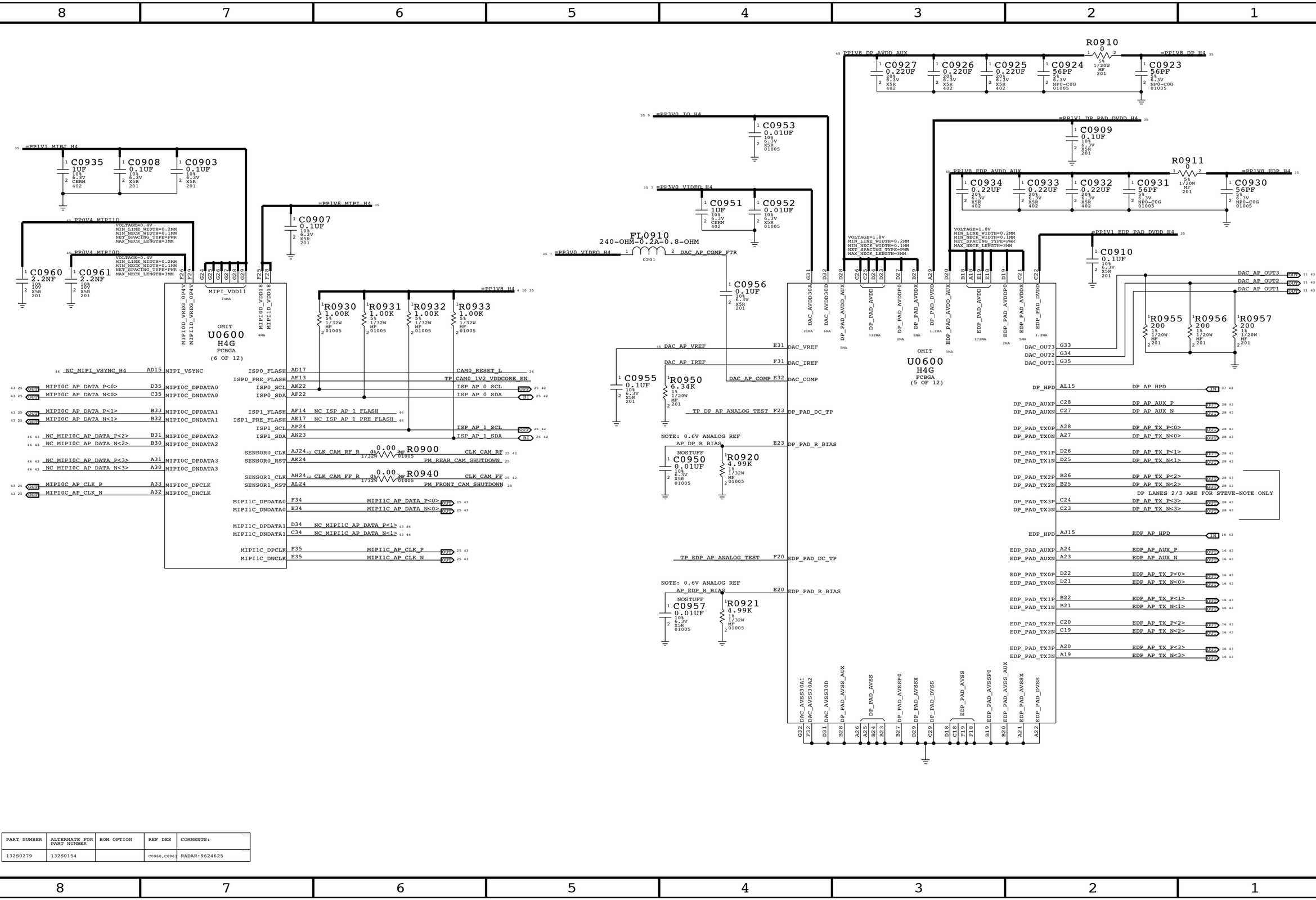
NEW GPIO FOR J2. FILE A RADAR
CHECK WITH GRAPE ON VOLTAGE FOR THESE TWO SIGNALS



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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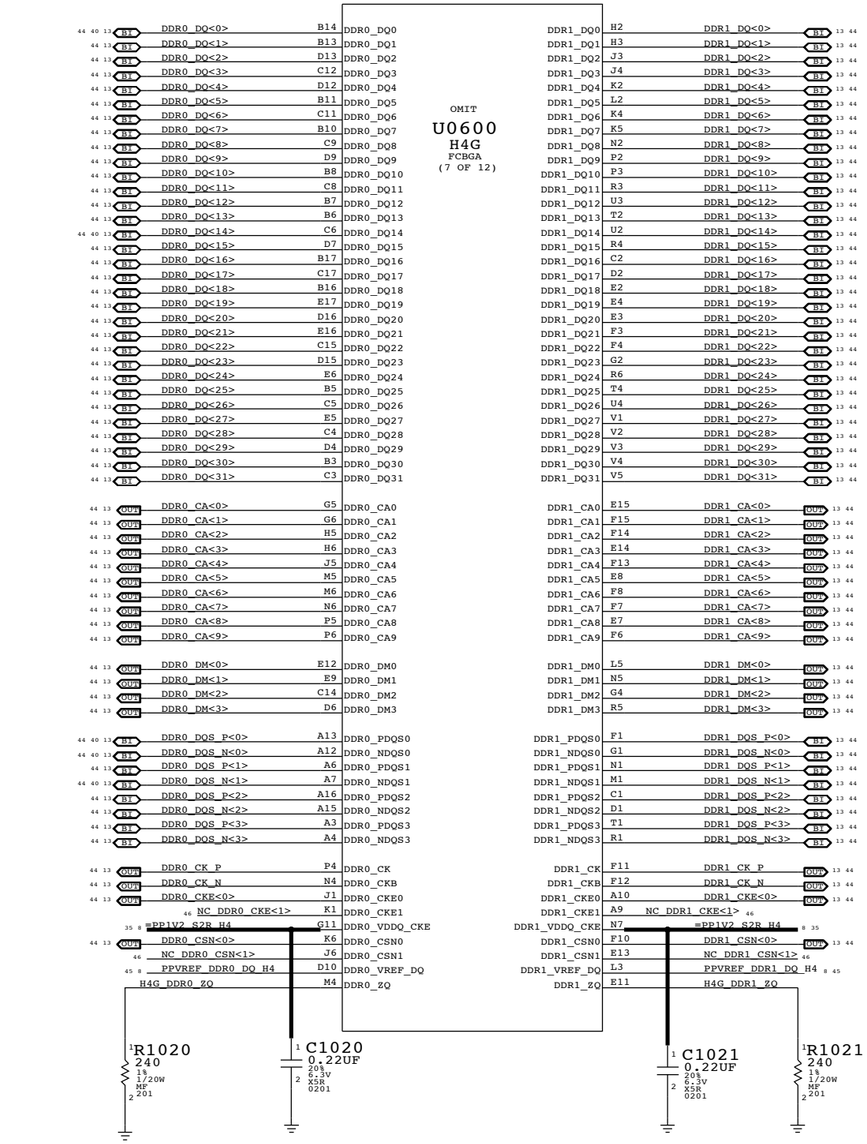
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FCBGA
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DDR0_CKB
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DDR0_CKE1
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DDR0_CSN1
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DDR0_ZQ
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MF
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C1020
0.22UF
20%
4.3V
X5R
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20%
4.3V
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0201
R1021
240
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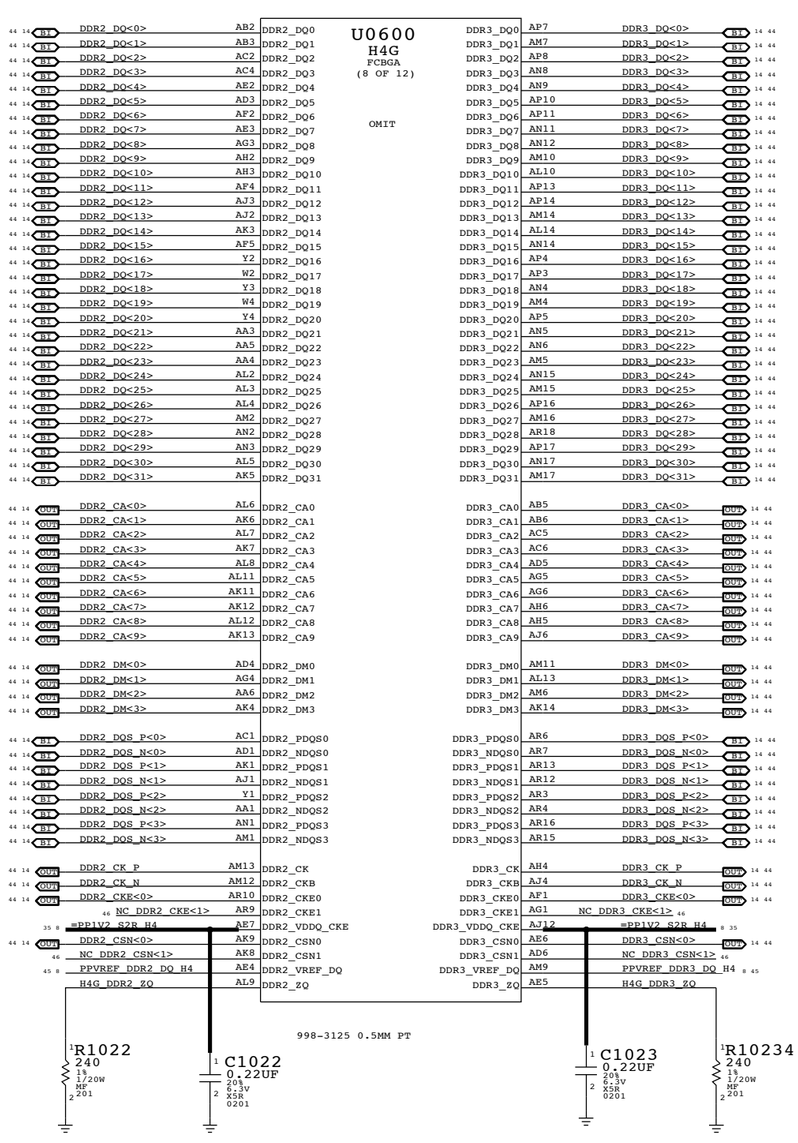
1/20W
MF
201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1/20W
MF
201
C1022
0.22UF
20%
4.3V
X5R
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20%
4.3V
X5R
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1%
1/20W
MF
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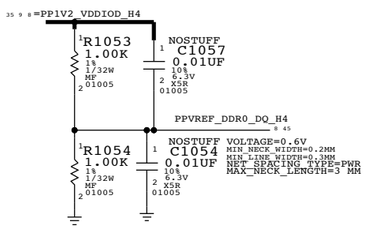
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1/32W
MF
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NOSTUFF
C1057
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10%
6.3V
X5R
01005
PPVREF_DDR0_DQ_H4
R1054
1.00K
1%
1/32W
MF
01005
NOSTUFF
C1054
0.01UF
10%
6.3V
X5R
01005
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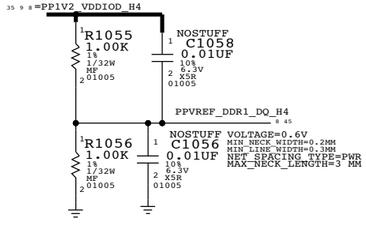
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM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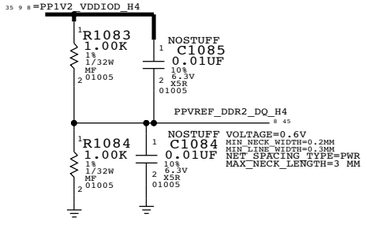
10%
6.3V
X5R
01005
PPVREF_DDR1_DQ_H4
R1056
1.00K
1%
1/32W
MF
01005
NOSTUFF
C1056
0.01UF
10%
6.3V
X5R
01005
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM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1/32W
MF
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NOSTUFF
C1085
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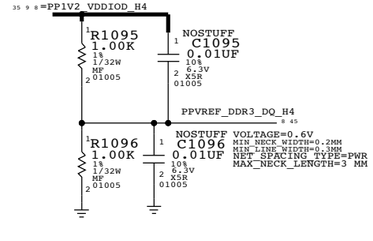
10%
6.3V
X5R
01005
PPVREF_DDR2_DQ_H4
R1084
1.00K
1%
1/32W
MF
01005
NOSTUFF
C1084
0.01UF
10%
6.3V
X5R
01005
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM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C1095
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10%
6.3V
X5R
01005
PPVREF_DDR3_DQ_H4
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1%
1/32W
MF
01005
NOSTUFF
C1096
0.01UF
10%
6.3V
X5R
01005
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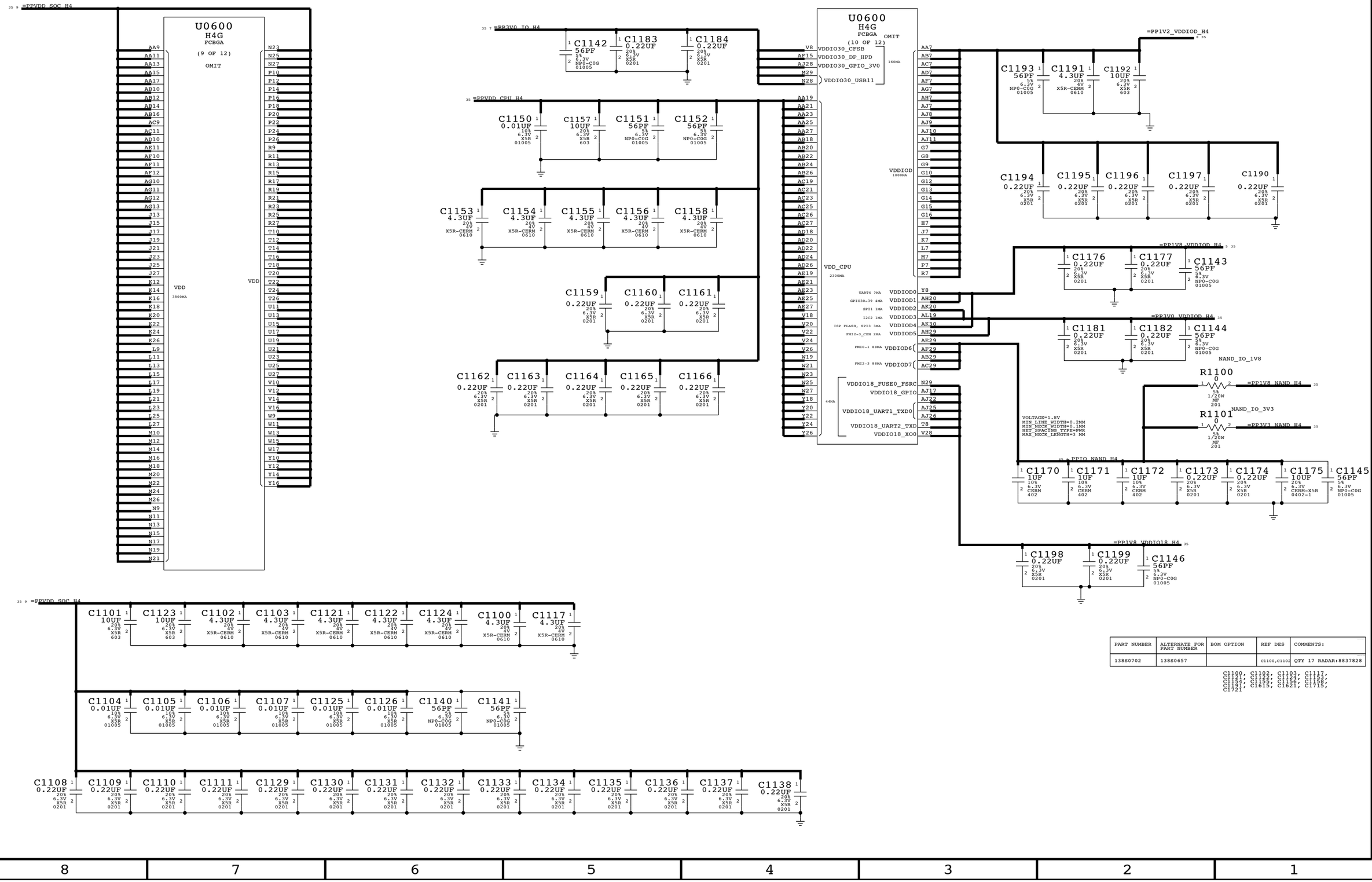
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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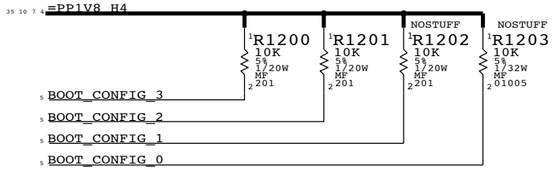
C1100; C1102; C1103; C1117; C1121; C1122; C1124; C1153; C1154; C1155; C1156; C1158; C1191; C1615; C1621; C1715; C1721;

BOOT CONFIG ID

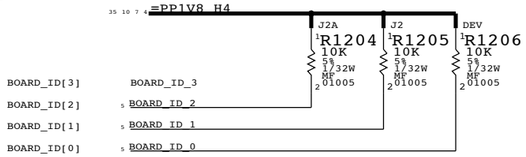


BOOT_CONFIG[3-0]	
1100	FMI0/1 2/2 CS
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS WITH TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID

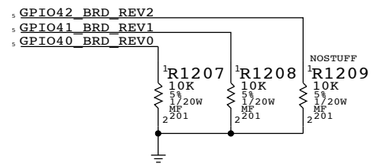


BOARD_ID[3-0]	
0000	J1 AP
0001	J1 DEV
0010	J2 AP
0011	J2 DEV
0100	J2A AP
0101	J2A DEV

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION



BRD_REV[2-0]	
000	PROTO 0
001	PROTO 1 LOCAL
010	PROTO 1 CHINA
011	PROTO 2
100	EVT

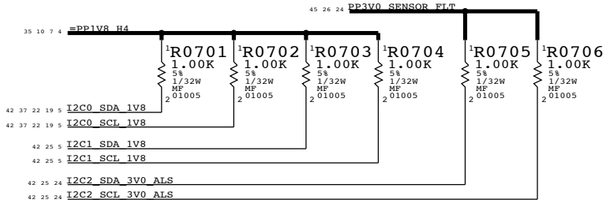
S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

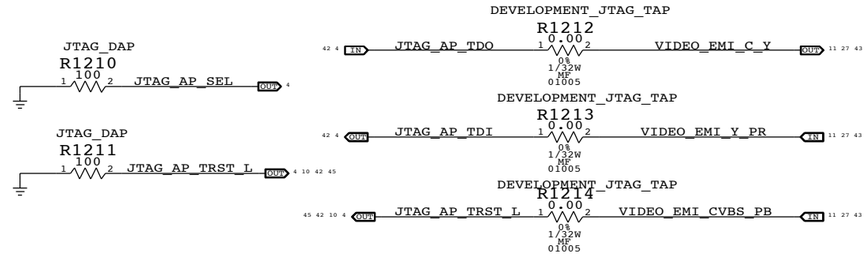
FOR REFERENCE

	BOOT_CONFIG[3:0]	
	0000	SPI0
	0001	SPI1
	0010	SPI0 W/TEST
	0011	SPI1 W/TEST
	0100	FMI0 2CS
	0101	FMI0 4CS
	0110	FMI0 4CS W/TEST
	0111	RESERVED
	1000	FMI1 2 CS
	1001	FMI1 4 CS
	1010	FMI1 4CS W/TEST
CURRENT SETTING ->	1100	FMI0/1 2/2 CS
	1101	FMI0/1 4/4 CS
	1110	FMI0/1 4/4 CS W/TEST
	1111	RESERVED

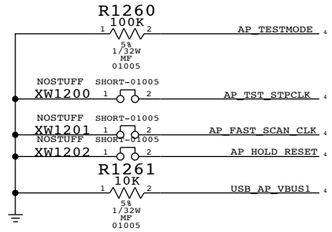
I2C PULL-UPS

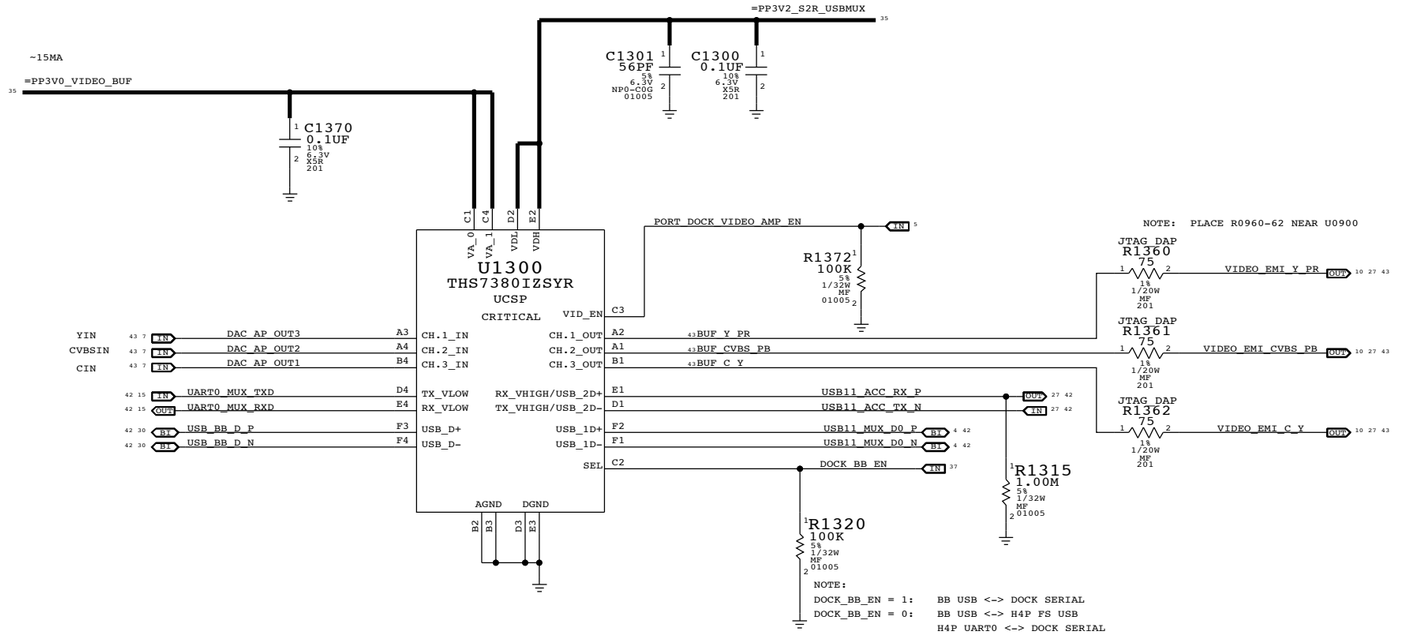


JTAG

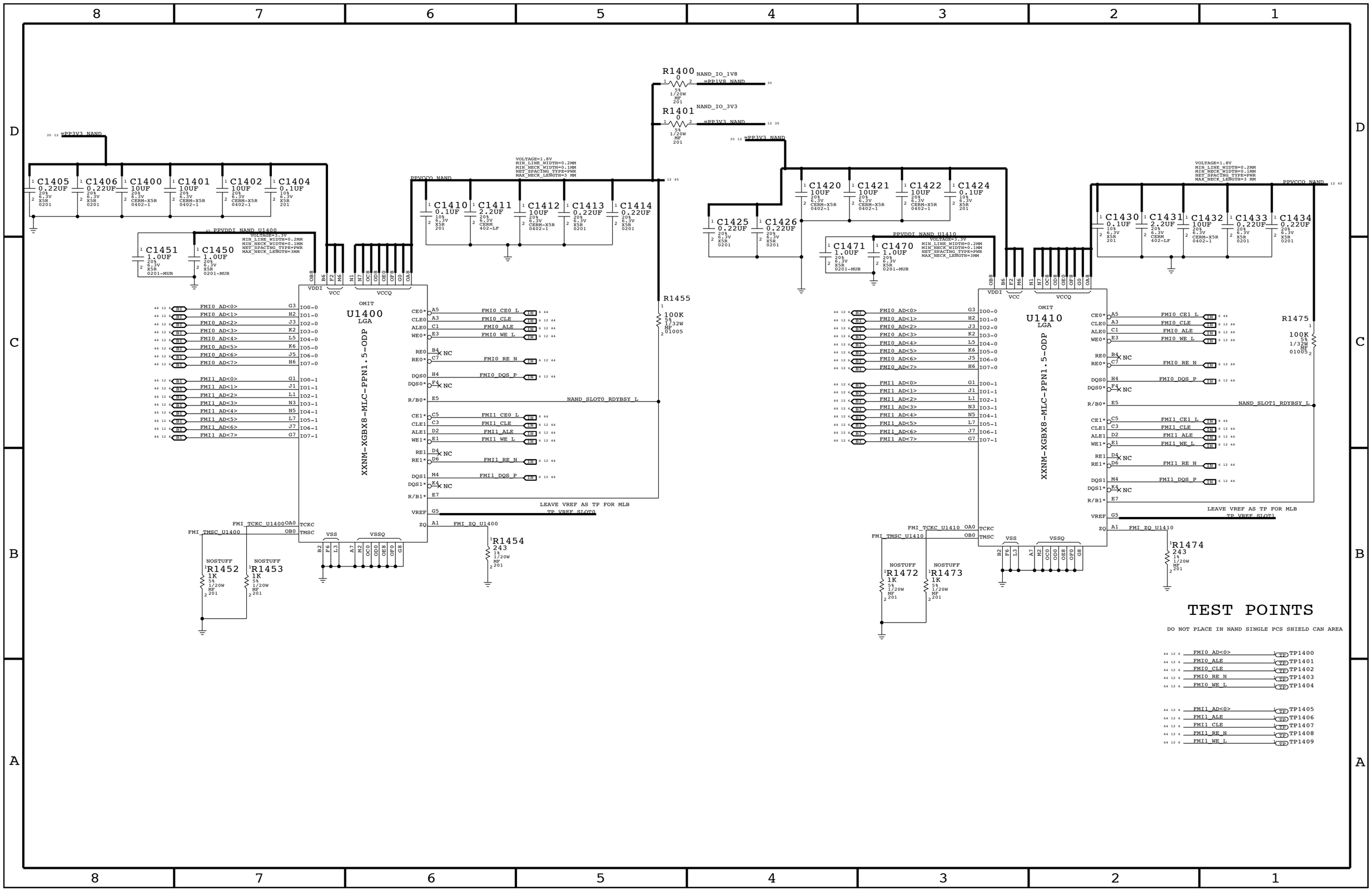


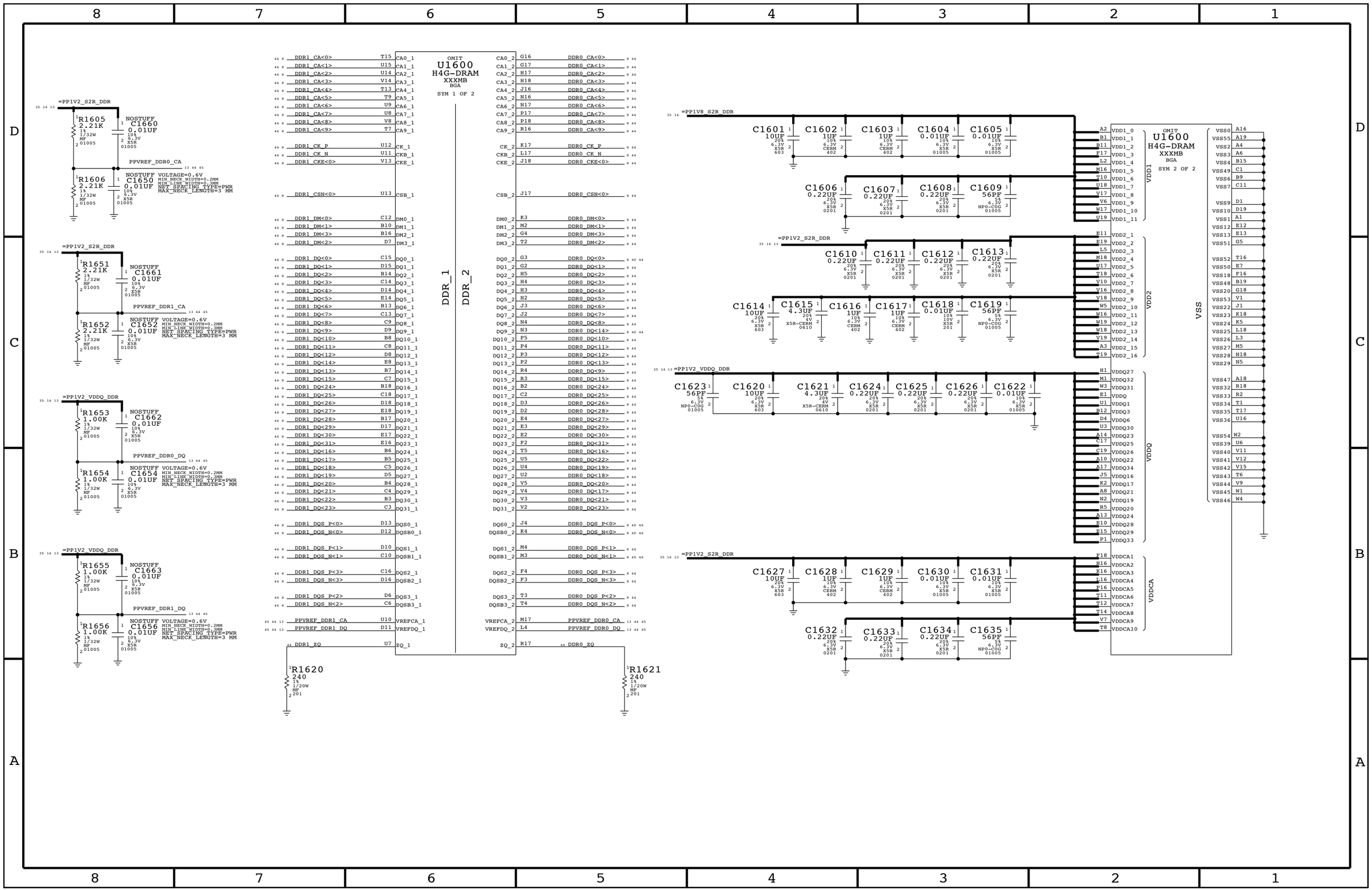
2-WIRE DAP	SCAN DUMP	PRODUCTION
DEVELOPMENT_JTAG	DEVELOPMENT_JTAG	JTAG_DAP
JTAG_DAP	DEVELOPMENT_JTAG_TAP	





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0539	343S0520		U1300	RADAR:9009078


R1400 0 NAND_IO_1V8 =PP1V8_NAND
R1401 0 NAND_IO_3V3 =PP3V3_NAND
=PP3V3_NAND
PPVCCQ_NAND
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
C1405 0.22UF
C1406 0.22UF
C1400 10UF
C1401 10UF
C1402 10UF
C1404 0.1UF
C1410 0.1UF
C1411 2.2UF
C1412 10UF
C1413 0.22UF
C1414 0.22UF
C1420 10UF
C1421 10UF
C1422 10UF
C1424 0.1UF
C1425 0.22UF
C1426 0.22UF
C1430 0.1UF
C1431 2.2UF
C1432 10UF
C1433 0.22UF
C1434 0.22UF
C1450 1.0UF
C1451 1.0UF
C1470 1.0UF
C1471 1.0UF
PPVDDI_NAND_U1400
PPVDDI_NAND_U1410
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3MM
U1400 LGA XXNM-XGBX8-MLC-PPN1.5-ODP
U1410 LGA XXNM-XGBX8-MLC-PPN1.5-ODP
OMIT
VDDI
VCC
VCCQ
FMI0_AD<0> FMI0_AD<1> FMI0_AD<2> FMI0_AD<3> FMI0_AD<4> FMI0_AD<5> FMI0_AD<6> FMI0_AD<7>
FMI1_AD<0> FMI1_AD<1> FMI1_AD<2> FMI1_AD<3> FMI1_AD<4> FMI1_AD<5> FMI1_AD<6> FMI1_AD<7>
IO0-0 IO1-0 IO2-0 IO3-0 IO4-0 IO5-0 IO6-0 IO7-0
IO0-1 IO1-1 IO2-1 IO3-1 IO4-1 IO5-1 IO6-1 IO7-1
CE0* CLE0 ALE0 WE0* RE0 RE0* DQS0 DQS0* R/B0*
CE1* CLE1 ALE1 WE1* RE1 RE1* DQS1 DQS1* R/B1*
FMI0_CE0_L FMI0_CLE FMI0_ALE FMI0_WE_L FMI0_RE_N FMI0_DQS_P
FMI1_CE0_L FMI1_CLE FMI1_ALE FMI1_WE_L FMI1_RE_N FMI1_DQS_P
NAND_SLOT0_RDYBSY_L
NAND_SLOT1_RDYBSY_L
VREF ZQ
LEAVE VREF AS TP FOR MLB
TP_VREF_SLOT0
TP_VREF_SLOT1
FMI_ZQ_U1400
FMI_ZQ_U1410
FMI_TCKC_U1400 FMI_TMSC_U1400
FMI_TCKC_U1410 FMI_TMSC_U1410
TCKC TMSC
VSS VSSQ
R1455 100K 5% 1/32W MF 01005
R1475 100K 5% 1/32W MF 01005
R1452 1K 5% 1/20W MF 201
R1453 1K 5% 1/20W MF 201
R1454 243 1% 1/20W MF 201
R1472 1K 5% 1/20W MF 201
R1473 1K 5% 1/20W MF 201
R1474 243 1% 1/20W MF 201
NOSTUFF
TEST POINTS
DO NOT PLACE IN NAND SINGLE PCS SHIELD CAN AREA
TP1400 FMI0_AD<0>
TP1401 FMI0_ALE
TP1402 FMI0_CLE
TP1403 FMI0_RE_N
TP1404 FMI0_WE_L
TP1405 FMI1_AD<0>
TP1406 FMI1_ALE
TP1407 FMI1_CLE
TP1408 FMI1_RE_N
TP1409 FMI1_WE_L


U1600
H4G-DRAM
XXXMB
BGA
SYM 1 OF 2
OMIT
DDR_1
DDR_2
U1600
H4G-DRAM
XXXMB
BGA
SYM 2 OF 2
OMIT
VDD1
VDD2
VDDQ
VDDCA
VSS
=PP1V2_S2R_DDR
=PP1V8_S2R_DDR
=PP1V2_VDDQ_DDR
PPVREF_DDR0_CA
PPVREF_DDR1_CA
PPVREF_DDR0_DQ
PPVREF_DDR1_DQ
NOSTUFF
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
R1605 2.21K
R1606 2.21K
R1651 2.21K
R1652 2.21K
R1653 1.00K
R1654 1.00K
R1655 1.00K
R1656 1.00K
R1620 240
R1621 240
C1601 10UF
C1602 1UF
C1603 1UF
C1604 0.01UF
C1605 0.01UF
C1606 0.22UF
C1607 0.22UF
C1608 0.22UF
C1609 56PF
C1610 0.22UF
C1611 0.22UF
C1612 0.22UF
C1613 0.22UF
C1614 10UF
C1615 4.3UF
C1616 1UF
C1617 1UF
C1618 0.01UF
C1619 56PF
C1623 56PF
C1620 10UF
C1621 4.3UF
C1624 0.22UF
C1625 0.22UF
C1626 0.22UF
C1622 0.01UF
C1627 10UF
C1628 1UF
C1629 1UF
C1630 0.01UF
C1631 0.01UF
C1632 0.22UF
C1633 0.22UF
C1634 0.22UF
C1635 56PF


=PP1V2_S2R_DDR
R1705 2.21K 1% 1/32W MF 01005
C1760 0.01UF 10% 6.3V X5R 01005
NOSTUFF
PPVREF_DDR2_CA
R1706 2.21K 1% 1/32W MF 01005
C1750 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.3MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM
=PP1V2_S2R_DDR
R1751 2.21K 1% 1/32W MF 01005
C1761 0.01UF 10% 6.3V X5R 01005
NOSTUFF
PPVREF_DDR3_CA
R1752 2.21K 1% 1/32W MF 01005
C1752 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.3MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM
=PP1V2_VDDQ_DDR
R1753 1.00K 1% 1/32W MF 01005
C1762 0.01UF 10% 6.3V X5R 01005
NOSTUFF
PPVREF_DDR2_DQ
R1754 1.00K 1% 1/32W MF 01005
C1754 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.3MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM
=PP1V2_VDDQ_DDR
R1755 1.00K 1% 1/32W MF 01005
C1763 0.01UF 10% 6.3V X5R 01005
NOSTUFF
PPVREF_DDR3_DQ
R1756 1.00K 1% 1/32W MF 01005
C1756 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.3MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM
OMIT
U1700
H4G-DRAM
XXXMB
BGA
SYM 1 OF 2
DDR_1
DDR_2
DDR3_CA<0> T15 CA0_1
DDR3_CA<1> U15 CA1_1
DDR3_CA<2> U14 CA2_1
DDR3_CA<3> V14 CA3_1
DDR3_CA<4> T13 CA4_1
DDR3_CA<5> T9 CA5_1
DDR3_CA<6> U9 CA6_1
DDR3_CA<7> U8 CA7_1
DDR3_CA<8> V8 CA8_1
DDR3_CA<9> T7 CA9_1
DDR3_CK_P U12 CK_1
DDR3_CK_N U11 CKB_1
DDR3_CKE<0> V13 CKE_1
DDR3_CSN<0> U13 CSB_1
DDR3_DM<0> C12 DM0_1
DDR3_DM<1> B10 DM1_1
DDR3_DM<3> B16 DM2_1
DDR3_DM<2> D7 DM3_1
DDR3_DQ<0> C15 DQ0_1
DDR3_DQ<1> D15 DQ1_1
DDR3_DQ<2> B14 DQ2_1
DDR3_DQ<3> C14 DQ3_1
DDR3_DQ<4> D14 DQ4_1
DDR3_DQ<5> E14 DQ5_1
DDR3_DQ<6> B13 DQ6_1
DDR3_DQ<7> C13 DQ7_1
DDR3_DQ<8> C9 DQ8_1
DDR3_DQ<9> D9 DQ9_1
DDR3_DQ<10> B8 DQ10_1
DDR3_DQ<11> C8 DQ11_1
DDR3_DQ<12> D8 DQ12_1
DDR3_DQ<13> E8 DQ13_1
DDR3_DQ<14> B7 DQ14_1
DDR3_DQ<15> C7 DQ15_1
DDR3_DQ<24> B18 DQ16_1
DDR3_DQ<25> C18 DQ17_1
DDR3_DQ<26> D18 DQ18_1
DDR3_DQ<27> E18 DQ19_1
DDR3_DQ<28> B17 DQ20_1
DDR3_DQ<29> D17 DQ21_1
DDR3_DQ<30> E17 DQ22_1
DDR3_DQ<31> E16 DQ23_1
DDR3_DQ<16> B6 DQ24_1
DDR3_DQ<17> B5 DQ25_1
DDR3_DQ<18> C5 DQ26_1
DDR3_DQ<19> D5 DQ27_1
DDR3_DQ<20> B4 DQ28_1
DDR3_DQ<21> C4 DQ29_1
DDR3_DQ<22> B3 DQ30_1
DDR3_DQ<23> C3 DQ31_1
DDR3_DQS_P<0> D13 DQS0_1
DDR3_DQS_N<0> D12 DQSB0_1
DDR3_DQS_P<1> D10 DQS1_1
DDR3_DQS_N<1> C10 DQSB1_1
DDR3_DQS_P<3> C16 DQS2_1
DDR3_DQS_N<3> D16 DQSB2_1
DDR3_DQS_P<2> D6 DQS3_1
DDR3_DQS_N<2> C6 DQSB3_1
PPVREF_DDR3_CA U10 VREFCA_1
PPVREF_DDR3_DQ D11 VREFDQ_1
DDR3_ZQ U7 ZQ_1
CA0_2 G16 DDR2_CA<0>
CA1_2 G17 DDR2_CA<1>
CA2_2 H17 DDR2_CA<2>
CA3_2 H18 DDR2_CA<3>
CA4_2 J16 DDR2_CA<4>
CA5_2 N16 DDR2_CA<5>
CA6_2 N17 DDR2_CA<6>
CA7_2 P17 DDR2_CA<7>
CA8_2 P18 DDR2_CA<8>
CA9_2 R16 DDR2_CA<9>
CK_2 K17 DDR2_CK_P
CKB_2 L17 DDR2_CK_N
CKE_2 J18 DDR2_CKE<0>
CSB_2 J17 DDR2_CSN<0>
DM0_2 K3 DDR2_DM<0>
DM1_2 M2 DDR2_DM<1>
DM2_2 G4 DDR2_DM<3>
DM3_2 T2 DDR2_DM<2>
DQ0_2 G3 DDR2_DQ<0>
DQ1_2 G2 DDR2_DQ<1>
DQ2_2 H5 DDR2_DQ<2>
DQ3_2 H4 DDR2_DQ<3>
DQ4_2 H3 DDR2_DQ<4>
DQ5_2 H2 DDR2_DQ<5>
DQ6_2 J3 DDR2_DQ<6>
DQ7_2 J2 DDR2_DQ<7>
DQ8_2 N4 DDR2_DQ<8>
DQ9_2 N3 DDR2_DQ<15>
DQ10_2 P5 DDR2_DQ<10>
DQ11_2 P4 DDR2_DQ<11>
DQ12_2 P3 DDR2_DQ<12>
DQ13_2 P2 DDR2_DQ<13>
DQ14_2 R4 DDR2_DQ<14>
DQ15_2 R3 DDR2_DQ<9>
DQ16_2 B2 DDR2_DQ<24>
DQ17_2 C2 DDR2_DQ<25>
DQ18_2 D3 DDR2_DQ<26>
DQ19_2 D2 DDR2_DQ<27>
DQ20_2 E4 DDR2_DQ<30>
DQ21_2 E3 DDR2_DQ<29>
DQ22_2 E2 DDR2_DQ<28>
DQ23_2 F2 DDR2_DQ<31>
DQ24_2 T5 DDR2_DQ<16>
DQ25_2 U5 DDR2_DQ<20>
DQ26_2 U4 DDR2_DQ<18>
DQ27_2 U2 DDR2_DQ<19>
DQ28_2 V5 DDR2_DQ<23>
DQ29_2 V4 DDR2_DQ<21>
DQ30_2 V3 DDR2_DQ<22>
DQ31_2 V2 DDR2_DQ<17>
DQS0_2 J4 DDR2_DQS_P<0>
DQSB0_2 K4 DDR2_DQS_N<0>
DQS1_2 M4 DDR2_DQS_P<1>
DQSB1_2 M3 DDR2_DQS_N<1>
DQS2_2 F4 DDR2_DQS_P<3>
DQSB2_2 F3 DDR2_DQS_N<3>
DQS3_2 T3 DDR2_DQS_P<2>
DQSB3_2 T4 DDR2_DQS_N<2>
VREFCA_2 M17 PPVREF_DDR2_CA
VREFDQ_2 L4 PPVREF_DDR2_DQ
ZQ_2 R17 DDR2_ZQ
R1720 240 1% 1/20W MF 201
R1721 240 1% 1/20W MF 201
=PP1V8_S2R_DDR
C1701 10UF 20% 6.3V X5R 603
C1702 1UF 10% 6.3V CERM 402
C1703 1UF 10% 6.3V CERM 402
C1704 0.01UF 10% 6.3V X5R 01005
C1705 0.01UF 10% 6.3V X5R 01005
C1706 0.22UF 20% 6.3V X5R 0201
C1707 0.22UF 20% 6.3V X5R 0201
C1708 0.22UF 20% 6.3V X5R 0201
C1709 56PF 5% 6.3V NPO-C0G 01005
=PP1V2_S2R_DDR
C1710 0.22UF 20% 6.3V X5R 0201
C1711 0.22UF 20% 6.3V X5R 0201
C1712 0.22UF 20% 6.3V X5R 0201
C1713 0.22UF 20% 6.3V X5R 0201
C1714 10UF 20% 6.3V X5R 603
C1715 4.3UF 20% 4V X5R-CERM 0610
C1716 1UF 10% 6.3V CERM 402
C1717 1UF 10% 6.3V CERM 402
C1718 0.01UF 10% 6.3V X5R 201
C1719 56PF 5% 6.3V NPO-C0G 01005
=PP1V2_VDDQ_DDR
C1723 56PF 5% 6.3V NPO-C0G 01005
C1720 10UF 20% 6.3V X5R 603
C1721 4.3UF 20% 4V X5R-CERM 0610
C1724 0.22UF 20% 6.3V X5R 0201
C1725 0.22UF 20% 6.3V X5R 0201
C1726 0.22UF 20% 6.3V X5R 0201
C1722 0.01UF 10% 6.3V X5R 01005
=PP1V2_S2R_DDR
C1727 10UF 20% 6.3V X5R 603
C1728 1UF 10% 6.3V CERM 402
C1729 1UF 10% 6.3V CERM 402
C1730 0.01UF 10% 6.3V X5R 01005
C1731 0.01UF 10% 6.3V X5R 01005
C1732 0.22UF 20% 6.3V X5R 0201
C1733 0.22UF 20% 6.3V X5R 0201
C1734 0.22UF 20% 6.3V X5R 0201
C1735 56PF 5% 6.3V NPO-C0G 01005
OMIT
U1700
H4G-DRAM
XXXMB
BGA
SYM 2 OF 2
VDD1
VDD2
VDDQ
VDDCA
VSS
A2 VDD1_0
B1 VDD1_1
B11 VDD1_2
F17 VDD1_3
L2 VDD1_4
M16 VDD1_5
T10 VDD1_6
U18 VDD1_7
V17 VDD1_8
V6 VDD1_9
W17 VDD1_10
U19 VDD1_11
E11 VDD2_1
E19 VDD2_2
L5 VDD2_3
M18 VDD2_4
U17 VDD2_5
T18 VDD2_6
V10 VDD2_7
V16 VDD2_8
V18 VDD2_9
W5 VDD2_10
W16 VDD2_11
W19 VDD2_12
W18 VDD2_13
V19 VDD2_14
A3 VDD2_15
T19 VDD2_16
H1 VDDQ27
M1 VDDQ32
W3 VDDQ31
E1 VDDQ
U1 VDDQ1
B12 VDDQ3
D4 VDDQ6
U3 VDDQ30
A14 VDDQ23
C17 VDDQ25
C19 VDDQ26
A10 VDDQ22
A17 VDDQ34
J5 VDDQ16
K2 VDDQ17
A8 VDDQ21
N2 VDDQ19
R5 VDDQ20
A13 VDDQ24
E10 VDDQ28
E15 VDDQ29
P1 VDDQ33
F18 VDDCA1
H16 VDDCA2
K16 VDDCA3
L16 VDDCA4
P16 VDDCA5
T11 VDDCA6
T12 VDDCA7
T14 VDDCA8
V7 VDDCA9
T8 VDDCA10
VSS0 A16
VSS55 A19
VSS2 A4
VSS3 A6
VSS4 B15
VSS49 C1
VSS6 B9
VSS7 C11
VSS9 D1
VSS10 D19
VSS1 A1
VSS12 E12
VSS13 E13
VSS51 G5
VSS52 T16
VSS50 E7
VSS18 F16
VSS48 B19
VSS20 G18
VSS53 V1
VSS22 J1
VSS23 K18
VSS24 K5
VSS25 L18
VSS26 L3
VSS27 M5
VSS28 N18
VSS29 N5
VSS47 A18
VSS32 R18
VSS33 R2
VSS34 T1
VSS35 T17
VSS36 U16
VSS54 W2
VSS39 U6
VSS40 V11
VSS41 V12
VSS42 V15
VSS43 T6
VSS44 V9
VSS45 W1
VSS46 W4

WIFI ALIASES

42 40 4	HSIC1_WLAN_DATA1	MAKE_BASE=TRUE	HSIC_DATA_4330	31 33
42 40 4	HSIC1_WLAN_STB1	MAKE_BASE=TRUE	HSIC_STROBE_4330	31 33
42 5	HSIC_HOST_READY_WLAN	MAKE_BASE=TRUE	WLAN_GPIO1	31 33
42 5	HSIC_WLAN_RDY	MAKE_BASE=TRUE	HSIC_DEVICE_READY	31
45 37	RST_WLAN_L	MAKE_BASE=TRUE	WLAN_ENABLE	31 33
37	PM_WLAN_HOST_WAKE	MAKE_BASE=TRUE	WLAN_GPIO0	31 33
45 37	RST_BT_L	MAKE_BASE=TRUE	BT_RESET_N	31 33
37	PM_BT_HOST_WAKE	MAKE_BASE=TRUE	BT_HOST_WAKE	31 33
5	PM_BT_WAKE	MAKE_BASE=TRUE	BT_WAKE	31 33
42 5	UART3_BT_RXD	MAKE_BASE=TRUE	BT_UART_TXD	31 33
42 5	UART3_BT_TXD	MAKE_BASE=TRUE	BT_UART_RXD	31 33
42 5	UART3_BT_CTS_L	MAKE_BASE=TRUE	BT_UART_RTS_N	31 33
42 5	UART3_BT_RTS_L	MAKE_BASE=TRUE	BT_UART_CTS_N	31 33
42 37	CLK_32K_WLAN	MAKE_BASE=TRUE	CLK32K	32 33
42 19 5	I2S2_VSP_BCLK	MAKE_BASE=TRUE	BT_PCM_CLK	31
42 19 5	I2S2_VSP_DOUT	MAKE_BASE=TRUE	BT_PCM_DIN	31
42 19 5	I2S2_VSP_DIN	MAKE_BASE=TRUE	BT_PCM_DOUT	31
42 19 5	I2S2_VSP_LRCK	MAKE_BASE=TRUE	BT_PCM_SYNC	31
42 5	UART6_WLAN_RXD	MAKE_BASE=TRUE	WLAN_GPIO4	31 33
42 5	UART6_WLAN_TXD	MAKE_BASE=TRUE	WLAN_GPIO3	31 33

UART ALIASES

42 5	UART0_AP_RXD	MAKE_BASE=TRUE	UART0_MUX_RXD	11 42
42 5	UART0_AP_TXD	MAKE_BASE=TRUE	UART0_MUX_TXD	11 42

OBSOLETE ALIASES

	NC_EXT_SMPS_REQ	MAKE_BASE=TRUE	EXT_SMPS_REQ	
	NC_EXT_PWM_REQ	MAKE_BASE=TRUE	EXT_PWM_REQ	
	NC_BT_GPIO5	MAKE_BASE=TRUE	BT_GPIO5	31
	TP_WLAN_GPIO5	MAKE_BASE=TRUE	WLAN_GPIO5	31
45 30 5	GSM_TXBURST_IND	MAKE_BASE=TRUE	LED_DRIVE_GSMB	

NEED TO DOUBLE CHECK IF WE NEED THIS IN IPAD, OR IF THIS MIGHT BE A PHONE SPECIFIC ISSUE

EDP CONNECTOR

SIA413DJ

MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS(ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0903	376S0796		Q2200	RADAR:8379470
155S0667	155S0583			RADAR:8616060, RADAR: 9015335

CRITICAL
Q2200
SIA413DJ
SC70-6L

=PP3V3_LCD
C2240 82PF 5% 25V CERM 0201
C2241 82PF 5% 25V CERM 0201
NOSTUFF R2210 10K 1% 1/20W MF 201
R2203 39K 1% 1/20W MF 201
NOSTUFF R2211 10K 1% 1/20W MF 201
R2204 21.5K 1% 1/20W MF 201
R2250 0 5% 1/20W MF 201
C2204 0.015UF 10% 6.3V X5R 0201
LCDVDD_PWREN_L
LCDVDD_PWREN_L_R
PM_LCDVDD_PWREN
Q2201 2N7002TXG SOT-523-3
R2205 100K 1% 1/20W MF 201

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
PP3V3_S0_LCD_FERR
C2203 0.1UF 10% 6.3V X5R 201
C2202 1UF 10% 6.3V CERM 402
R2290 47K 5% 1/20W MF 201
C2230 82PF 5% 25V CERM 0201

CRITICAL
L2201
FERR-120-OHM-1.5A
0402B
C2232 82PF 5% 25V CERM 0201
C2206 1000PF 10% 16V X7R 201

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
PP3V3_LCDVDD_SW_F

PP3V3_S0_LCD_FERR
R2240 100K 1% 1/32W MF 01005

EDP_AP_AUX_N → C2250 0.1UF 201 6.3V 10% X5R → EDP_EMI_AUX_N → TCM0605-1 → EDP_AUX_CONN_N
EDP_AP_AUX_P → C2251 0.1UF 201 6.3V 10% X5R → EDP_EMI_AUX_P → 90-OHM-50MA L2242 → EDP_AUX_CONN_P
R2241 100K 1% 1/32W MF 01005

EDP_AP_TX_N<0> → C2242 0.1UF → EDP_EMI_TX_N<0> → EDP_DATA_CONN_N<0>
EDP_AP_TX_P<0> → C2243 0.1UF → EDP_EMI_TX_P<0> → EDP_DATA_CONN_P<0>
TCM0606-4SM 12-OHM-100MA-8.5GHZ L2212

EDP_AP_TX_N<1> → C2244 0.1UF → EDP_EMI_TX_N<1> → EDP_DATA_CONN_N<1>
EDP_AP_TX_P<1> → C2245 0.1UF → EDP_EMI_TX_P<1> → EDP_DATA_CONN_P<1>
TCM0606-4SM 12-OHM-100MA-8.5GHZ L2222

EDP_AP_TX_N<2> → C2246 0.1UF → EDP_EMI_TX_N<2> → EDP_DATA_CONN_N<2>
EDP_AP_TX_P<2> → C2247 0.1UF → EDP_EMI_TX_P<2> → EDP_DATA_CONN_P<2>
TCM0606-4SM 12-OHM-100MA-8.5GHZ L2232

EDP_AP_TX_N<3> → C2248 0.1UF → EDP_EMI_TX_N<3> → EDP_DATA_CONN_N<3>
EDP_AP_TX_P<3> → C2249 0.1UF → EDP_EMI_TX_P<3> → EDP_DATA_CONN_P<3>
TCM0606-4SM 12-OHM-100MA-8.5GHZ L2202

518S0827
CRITICAL
J2200
502250-8051
F-RT-SM

EDP_AP_HPD → R2242 100K 1% 1/32W MF 01005

EDP_AUX_CONN_P
EDP_AUX_CONN_N
EDP_DATA_CONN_N<0>
EDP_DATA_CONN_P<0>
EDP_DATA_CONN_N<1>
EDP_DATA_CONN_P<1>
EDP_DATA_CONN_N<2>
EDP_DATA_CONN_P<2>
EDP_DATA_CONN_N<3>
EDP_DATA_CONN_P<3>
NC, NCX

LED_IO_5_B, LED_IO_3_B, LED_IO_1_B, LED_IO_6_A, LED_IO_4_A, LED_IO_2_A
LED_IO_6_B, LED_IO_4_B, LED_IO_2_B, LED_IO_5_A, LED_IO_3_A, LED_IO_1_A

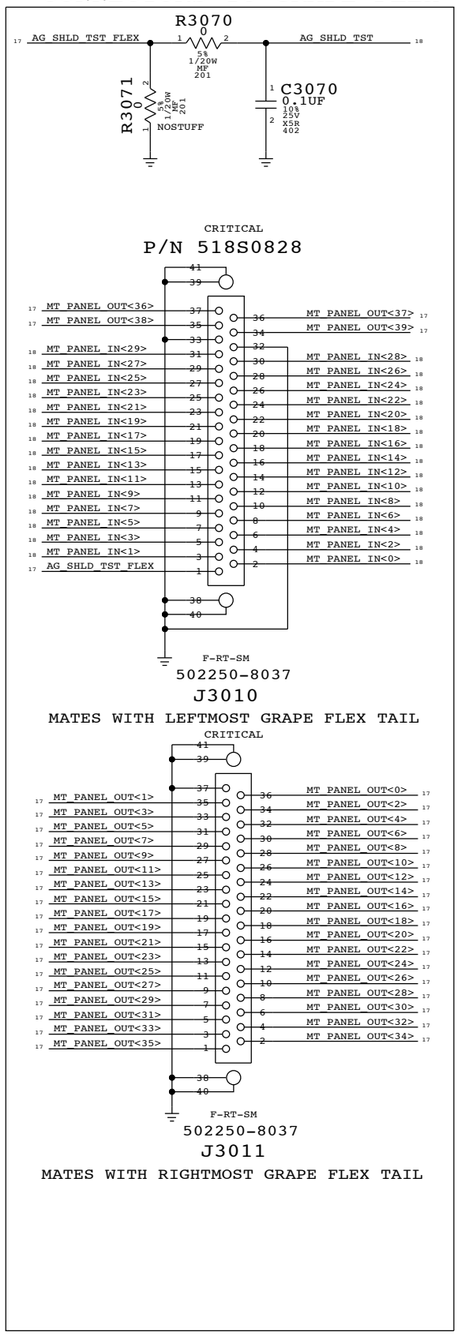
R2280 1.00M 01005 EDP_DATA_CONN_N<0>
R2281 1.00M 01005 EDP_DATA_CONN_P<0>
R2282 1.00M 01005 EDP_DATA_CONN_N<1>
R2283 1.00M 01005 EDP_DATA_CONN_P<1>
R2284 1.00M 01005 EDP_DATA_CONN_N<2>
R2285 1.00M 01005 EDP_DATA_CONN_P<2>
R2286 1.00M 01005 EDP_DATA_CONN_N<3>
R2287 1.00M 01005 EDP_DATA_CONN_P<3>

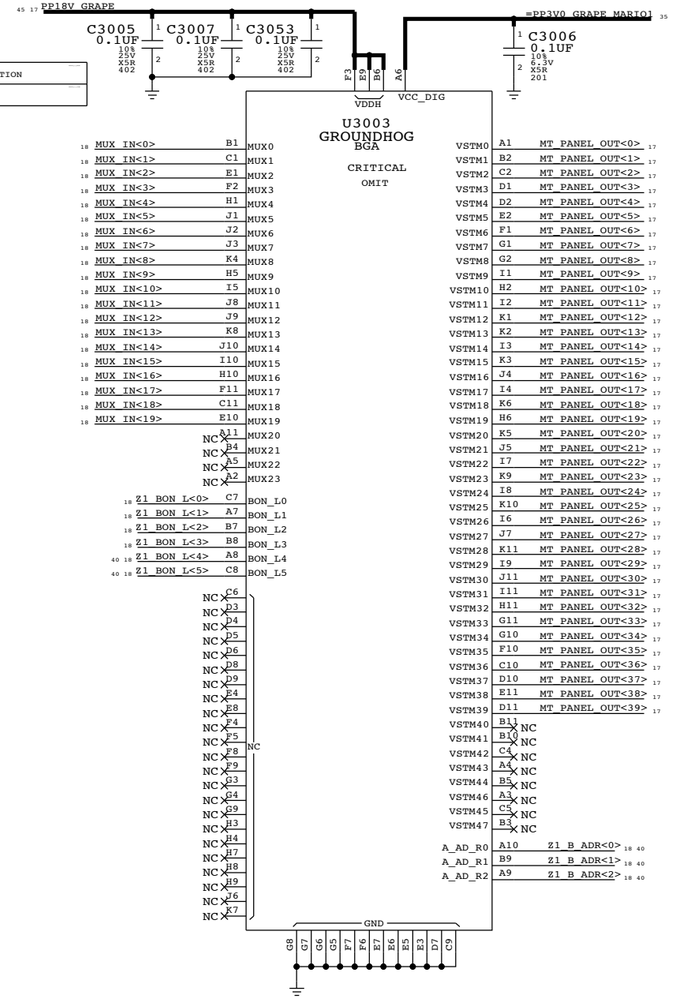
CRITICAL
L2210
FERR-240-OHM-25%-300MA
0402
=PPLED_REG_B → PPLED_BACK_REG_B
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
C2253 100PF 5% 50V CERM 402
C2270 820PF 10% 50V CERM 402

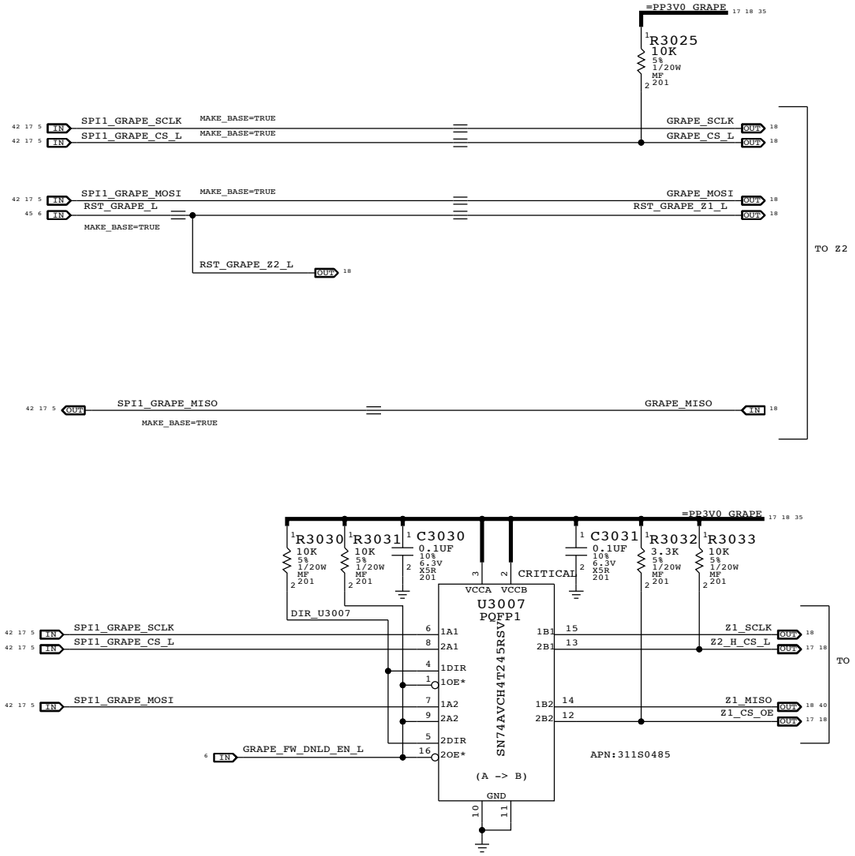
CRITICAL
L2200
FERR-240-OHM-25%-300MA
0402
=PPLED_REG_A → PPLED_BACK_REG_A
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
C2233 100PF 5% 50V CERM 402
C2220 820PF 10% 50V CERM 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

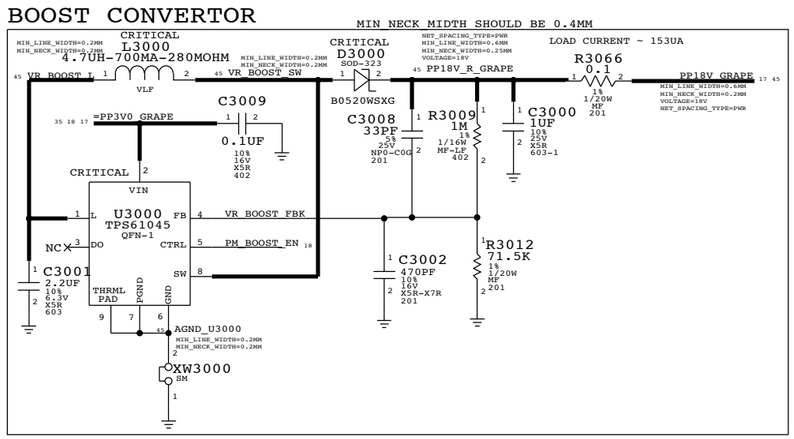
CONNECTORS TO GRAPE FLEX

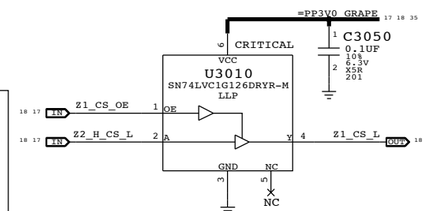


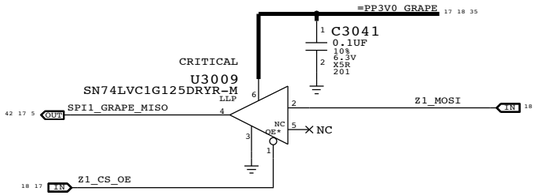




BOOST CONVERTOR







PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

ZEPHYR 1+ ASIC

=PP3V0_GRAPE_Z1 35

R3101 4.7 5% 1/20W MF 201

C3102 0.1UF 10% 6.3V X5R 201

C3104 2.2UF 20% 4V X5R 402

C3103 0.1UF 10% 6.3V X5R 201

C3101 2.2UF 20% 4V X5R 402

Z1_1V8_OUT 45 18

=PP3V0_GRAPE 17 18 35

R3155 100K 5% 1/20W MF 201

G6 G7 G8 K8 K10 C10 C5 C9 B6

VDDANA VDDDIG CRITICAL VDDIO V18

U3100
BCM5973
BGA

MT_PANEL_IN<0>	H2	IN0	
MT_PANEL_IN<1>	G2	IN1	
MT_PANEL_IN<2>	D7	IN2	
MT_PANEL_IN<3>	C1	IN3	
MT_PANEL_IN<4>	F1	IN4	
MT_PANEL_IN<5>	J1	IN5	
MT_PANEL_IN<6>	D2	IN6	
MT_PANEL_IN<7>	D1	IN7	
MT_PANEL_IN<8>	K7	IN8	
MT_PANEL_IN<9>	H1	IN9	
MT_PANEL_IN<10>	E1	IN10	
MT_PANEL_IN<11>	E2	IN11	
MT_PANEL_IN<12>	J2	IN12	
MT_PANEL_IN<13>	G1	IN13	
MT_PANEL_IN<14>	F2	IN14	
MT_PANEL_IN<15>	J7	IN15	
MT_PANEL_IN<16>	K2	IN16	
MT_PANEL_IN<17>	N4	IN17	
MT_PANEL_IN<18>	M5	IN18	
MT_PANEL_IN<19>	N5	IN19	
MT_PANEL_IN<20>	M6	IN20	
MT_PANEL_IN<21>	N3	IN21	
MT_PANEL_IN<22>	M3	IN22	
MT_PANEL_IN<23>	L1	IN23	
MT_PANEL_IN<24>	K1	IN24	
MT_PANEL_IN<25>	L2	IN25	
MT_PANEL_IN<26>	N6	IN26	
MT_PANEL_IN<27>	M2	IN27	
MT_PANEL_IN<28>	M4	IN28	
MT_PANEL_IN<29>	M1	IN29	
MUX_IN<0>	N2	IN30	
MUX_IN<1>	N1	IN31	
MUX_IN<2>	N13	IN32	
MUX_IN<3>	N12	IN33	
MUX_IN<4>	M10	IN34	
MUX_IN<5>	M13	IN35	
MUX_IN<6>	N8	IN36	
MUX_IN<7>	M12	IN37	
MUX_IN<8>	K13	IN38	
MUX_IN<9>	L13	IN39	
MUX_IN<10>	L12	IN40	
MUX_IN<11>	M11	IN41	
MUX_IN<12>	N11	IN42	
MUX_IN<13>	M8	IN43	
MUX_IN<14>	N9	IN44	
MUX_IN<15>	M9	IN45	
MUX_IN<16>	N10	IN46	
MUX_IN<17>	K12	IN47	
MUX_IN<18>	J13	IN48	
MUX_IN<19>	F12	IN49	
NC	C13	IN50	
NC	C12	IN51	
NC	B12	IN52	
NC	E13	IN53	
NC	B13	IN54	
NC	N7	IN55	
NC	B13	IN56	
NC	B12	IN57	
NC	H12	IN58	
NC	F13	IN59	
NC	C13	IN60	
NC	E7	IN61	
NC	M7	IN62	
NC	G12	IN63	

SCLK	A11	Z1_SCLK	IN 17 18
CS*	B10	Z1_CS_L	IN 17
MISO	B9	Z1_MISO	IN 17 18 40
MOSI	B8	Z1_MOSI	OUT 17 18
GO	A8	Z1_GO	18
DONE	B7	Z1_DONE	18
PCLK	A12	Z1_PCLK	18
STMOUT	A10		
STMIN	A13	Z1_STMIN	
B_ADR0	A5	Z1_B_ADR<0>	17 40
B_ADR1	B5	Z1_B_ADR<1>	17 40
B_ADR2	A6	Z1_B_ADR<2>	17 40
BON_L0	A2	Z1_BON_L<0>	17
BON_L1	A1	Z1_BON_L<1>	17
BON_L2	A3	Z1_BON_L<2>	17
BON_L3	A4	Z1_BON_L<3>	17
BON_L4	B4	Z1_BON_L<4>	17 40
BON_L5	B3	Z1_BON_L<5>	17 40
TM	A9	U3100_TM	
RESET*	A7	RST_GRAPE_Z1_L	17

R3181 100 1% 1/32W MF 01005

GNDANA GNDDIG GNDIO

B1 B2 B12 B13 C2 C3 C6 C7 C8 C11 C12 D3 D11 F7 H7 E3 E4 E5 L6 L7 L8 L9 L10 L11 C4 B11

ARM9 MCU (Z2 BASED)

45 Z2_VDDCORE

VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR

C3111 10UF 20% 6.3V CERM-X5R 0402-1

C3109 0.1UF 10% 6.3V X5R 201

VDDANA AND VDDCORE ARE EACH GENERATED WITHIN Z2 AND BYPASSED OUTSIDE

45 Z2_VDDANA

VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR

C3112 2.2UF 20% 4V X5R 402

C3110 0.1UF 10% 6.3V X5R 201

=PP3V0_GRAPE_Z2 35

C3105 0.1UF 10% 6.3V X5R 201

C3107 4.7UF 20% 6.3V X5R-CERM1 402

VOLTAGE=1.8V NET_SPACING_TYPE=PWR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

45 Z2_3V3_1V8_IN

C3108 0.1UF 10% 6.3V X5R 201

C3106 0.1UF 10% 6.3V X5R 201

C3191 10UF 20% 6.3V CERM-X5R 0402-1

C3192 10UF 20% 6.3V CERM-X5R 0402-1

R3190 1.00 1% 1/20W MF 201

Z1_1V8_OUT 18 45

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM VOLTAGE=1.8V NET_SPACING_TYPE=PWR

MIN_NECK_WIDTH SHOULD BE 0.4MM

D2 F1 G8 H2 J5 E2 E3

VDDANA VDDCORE VDDIO VDDLDO

CRITICAL
U3101
BCM5974CKFBGH
FBGA

NC	A9	IN0_0	
NC	B9	IN0_1	
NC	A7	IN1_0	
NC	A8	IN1_1	
NC	B8	IN2_0	
NC	C8	IN2_1	
NC	B7	IN3_0	
NC	C7	IN3_1	
NC	A6	IN4_0	
NC	B6	IN4_1	
NC	C6	IN5_0	
NC	C5	IN5_1	
NC	B5	IN6_0	
NC	A5	IN6_1	
NC	A4	IN7_0	
NC	B4	IN7_1	
NC	A3	IN8_0	
NC	B3	IN8_1	
NC	C2	IN9_0	
NC	B2	IN9_1	
NC	B2	IN10_0	
NC	C1	IN10_1	
NC	B1	IN11_0	
NC	A1	IN11_1	
NC	E6	ARMTAPMD*	
	F6	BOOT_CFG0	
	D3	BOOT_CFG1	
NC	C5	FLOO	
NC	E5	LFOO	
NC	G7	EXTFLLIN	

B_ADR0	F9		
B_ADR1	F8	Z1_PCLK	18
B_ADR2	G9		
BON_L0	J8	Z1_CS_OE_R	
BON_L1	H9	NC_BON_L1	46
BON_L2	J9	AG_SHLD_TST	17
BON_L3	H7	NC_BON_L3	46
BON_L4	J7		
BON_L5	H5	NC_BON_L5	46
GPIO0	J2	IRQ_GRAPE_HOST_INT_L	OUT 5
GPIO1	J3	PM_BOOST_EN	OUT 17
GPIO2	H4	Z1_GO	18
GPIO3	J6	Z1_DONE	18
GPIO4	G3	GRAPE_CS_L	IN 17
GPIO5	F3	GRAPE_MOSI	IN 17
GPIO6	F4	GRAPE_MISO	OUT 17
GPIO7	H6	GRAPE_SCLK	IN 17
JTAG_TCK	G6	TP_U3101_TCK	
JTAG_TDI	E8	TP_U3101_TDI	
JTAG_TDO	E9	TP_U3101_TDO	
JTAG_TMS	F7	TP_U3101_TMS	
H_CS*	H1	Z2_H_CS_L	IN 17
H_SCLK	J1	Z1_SCLK	IN 17 18
H_SDI	H3	Z1_MISO	IN 17 18 40
H_SDO	J4	Z1_MOSI	OUT 17 18
A_CS*	F1	Z2_A_CS_L	
A_SCLK	G1	TP_Z2_A_SCLK	
A_SDI	F2	TP_Z2_A_SDI	
A_SDO	G4	TP_Z2_A_SDO	
TM0	E7	TP_U3101_TM0	
TM1	D4	U3101_TM1	
CLKIN	E5	HOST_REFCLK	CLK_32K_PMU IN 17 42
CLKOUT	E4	NC	MAKE_BASE=TRUE
RESET*	D5	RST_GRAPE_Z2_L	IN 17

R3120 0 5% 1/20W MF 201

Z1_CS_OE IN 17

R3160 100K 5% 1/20W MF 201

=PP3V0_GRAPE 17 18 35

R3107 100K 5% 1/20W MF 201

R3180 100 1% 1/32W MF 01005

INTERNAL PU

GND

C3 C4 D6 D7 D8 C9 D9 G2 D1 H8

R3173 0 5% 1/20W MF 201

35 18 17 =PP3V0_GRAPE

R3171 0

BOOT_CFG0_R

BOOT_CFG1_R

CFG1	CFG0	MODE
0	0	DEPENDENT 1
0	1	DEPENDENT 2
1	0	AUTONOMOUS
1	1	SLAVE

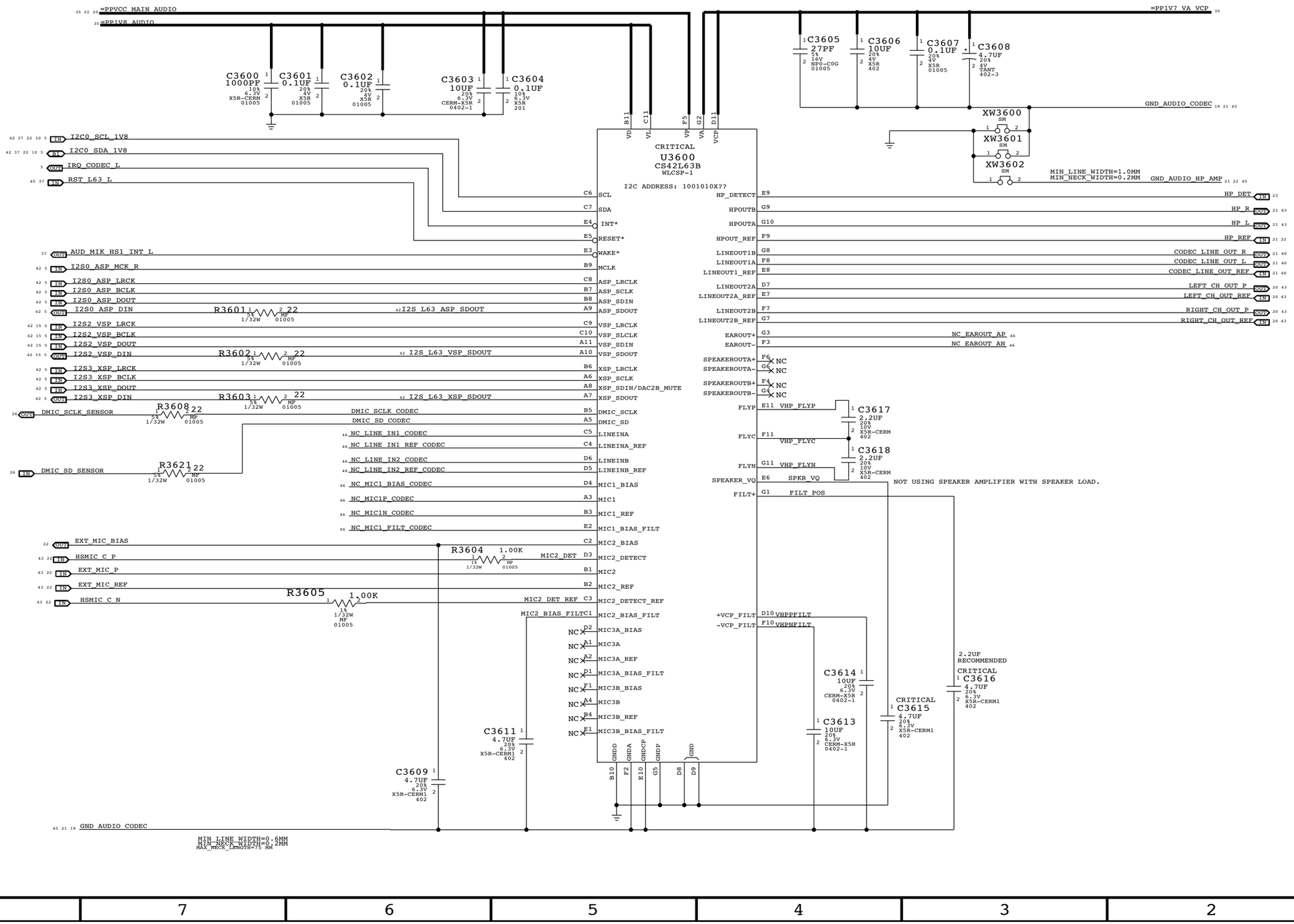
K48 USES DEPENDENT 2 MODE

Z2 - PRODUCT STRAP OPTIONS

BON_L5	BON_L4	BON_L3	MODE
LOW	X	X	K48
FLOAT	FLOAT	FLOAT	K94
FLOAT	LOW	FLOAT	J2
ALL OTHER STRAPS			CRITICAL ERROR
DEFAULT			J2

L63B AUDIO CODEC

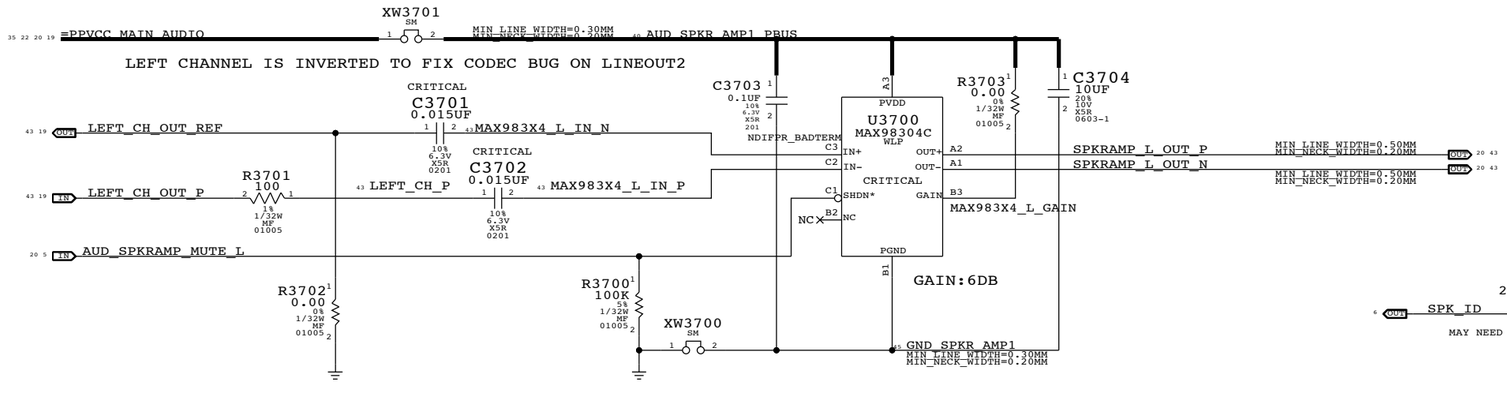
APN:338S0940



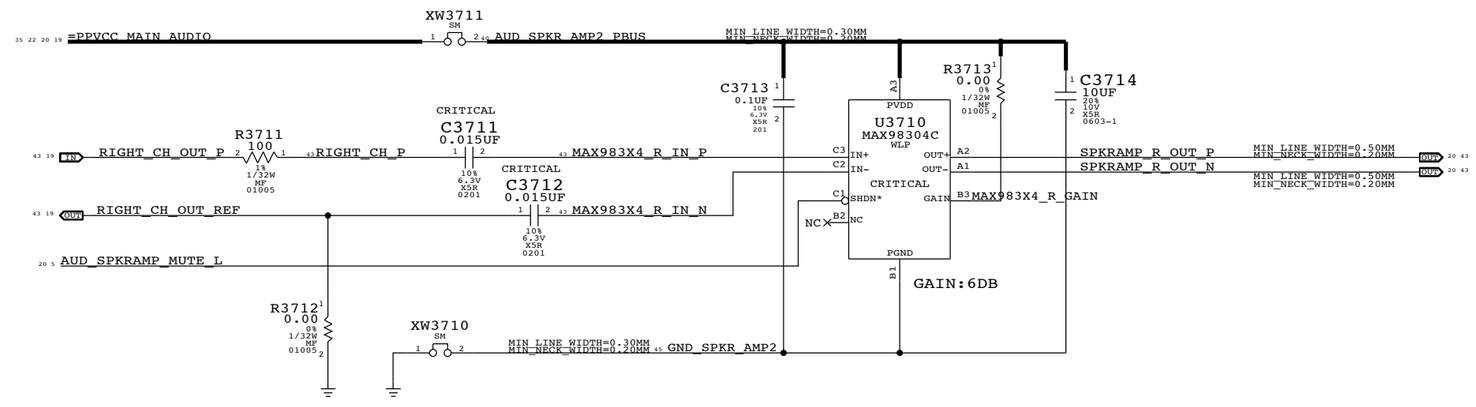
SPEAKER AMPLIFIER

APN:353S3317)
TURN ON TIME: 3.5MS
75HZ +/- XXX% TURN ON DELAY: ?MS

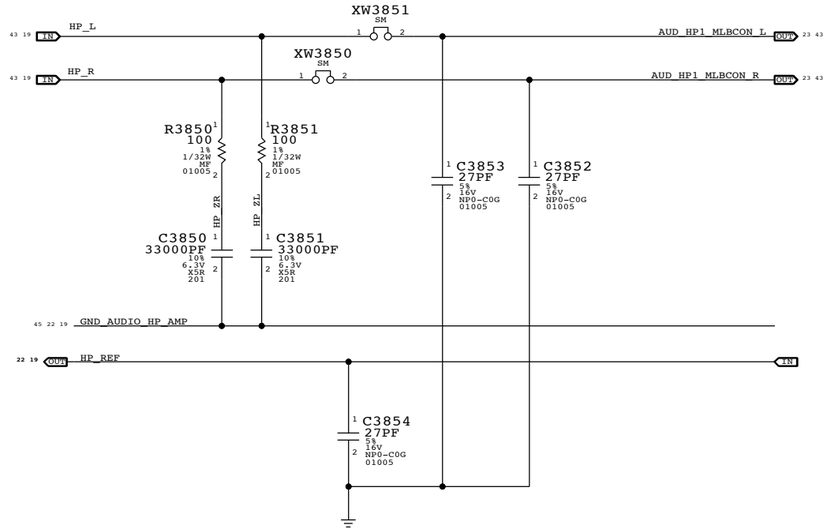
GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC



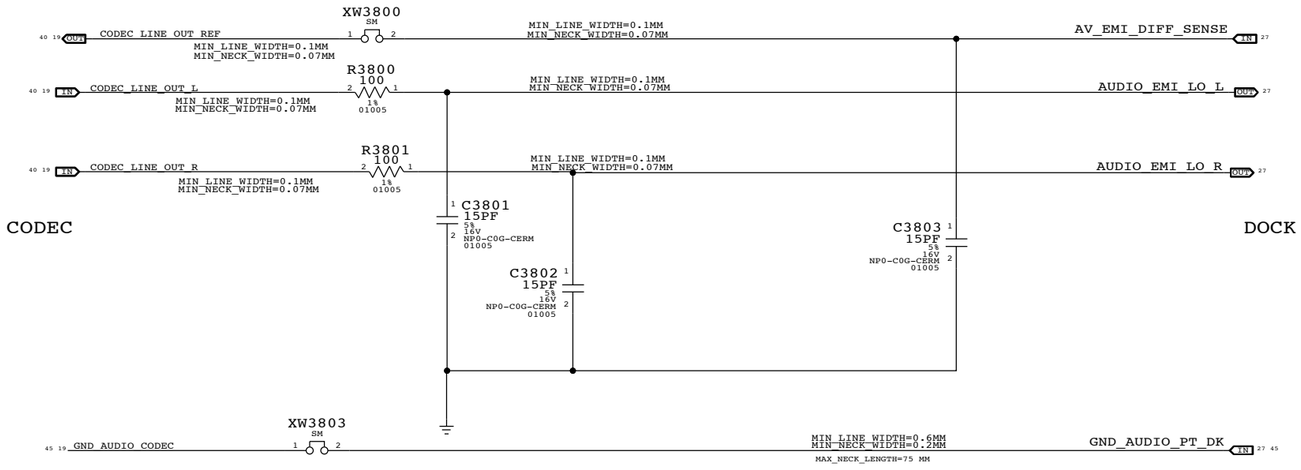
L63 LINEOUT2A IS CONNECTED TO U3700
L63 LINEOUT2B IS CONNECTED TO U3710



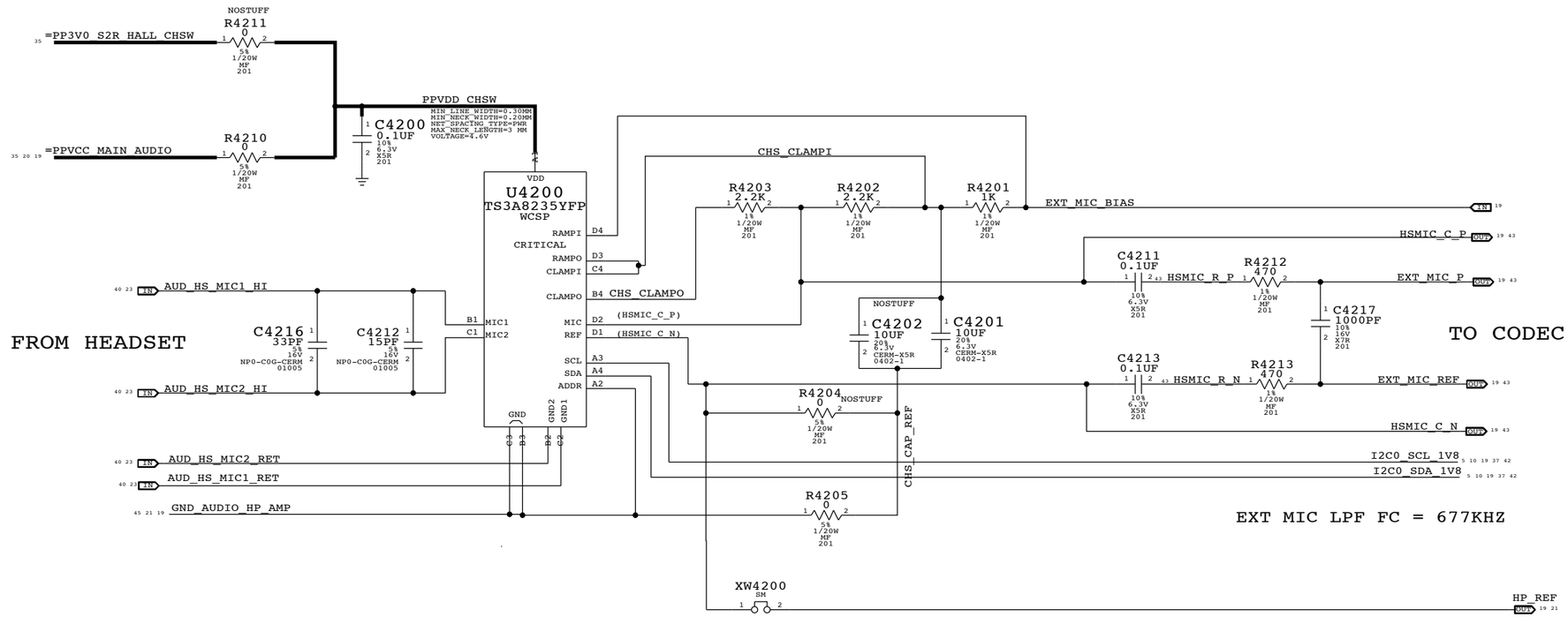
HEADPHONE OUTPUT ZOBEL NETWORK



DOCK LINE OUTPUT

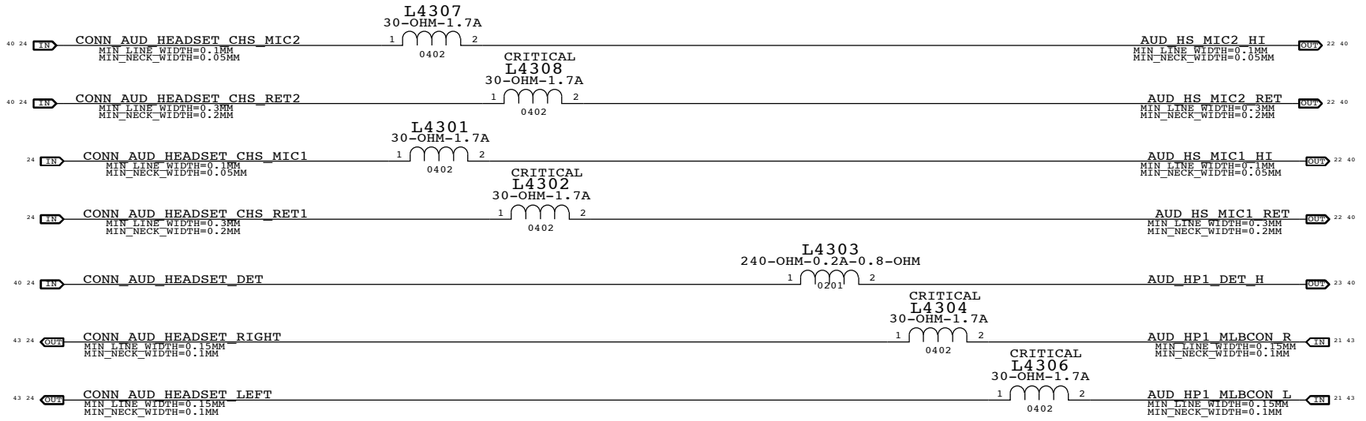


EXTERNAL (HEADSET) MIC INPUT CIRCUITRY

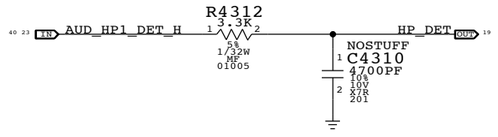


HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29

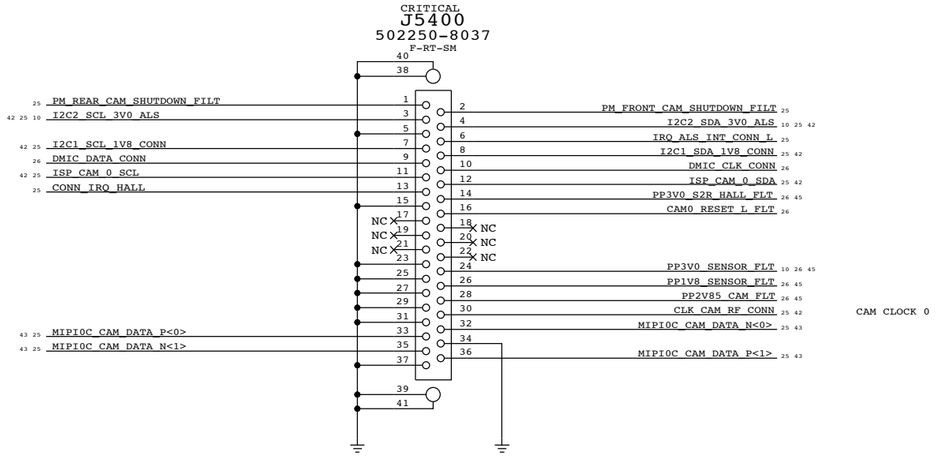
PLACE ALL COMPONENTS NEAR J5401



HEADSET JACK INSERTION DETECT

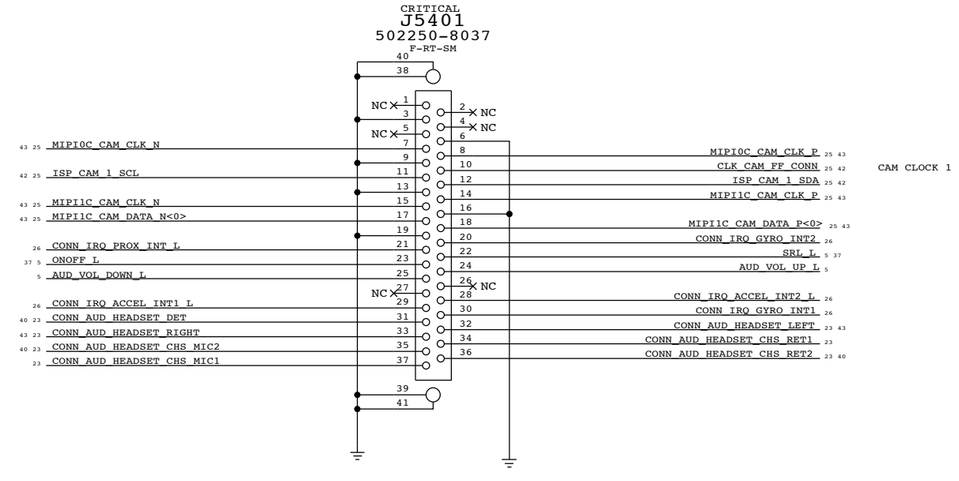


APN: 518S0828

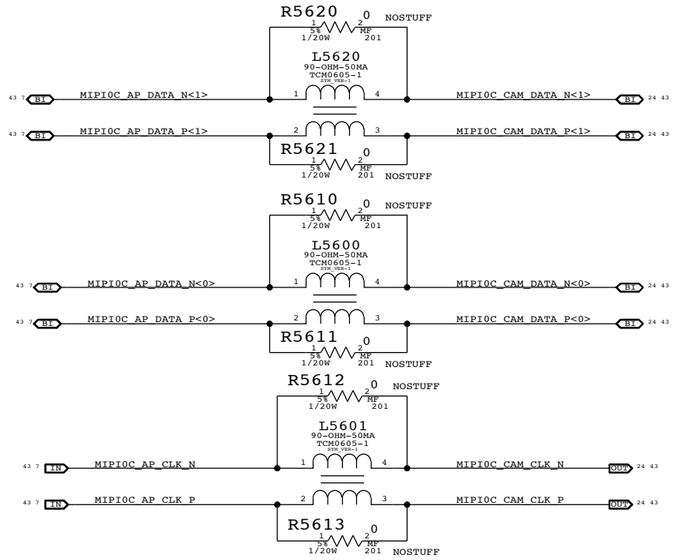


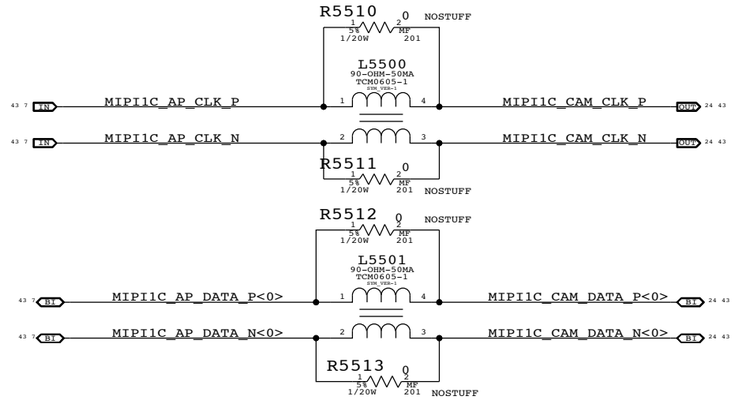
CAM CLOCK 0

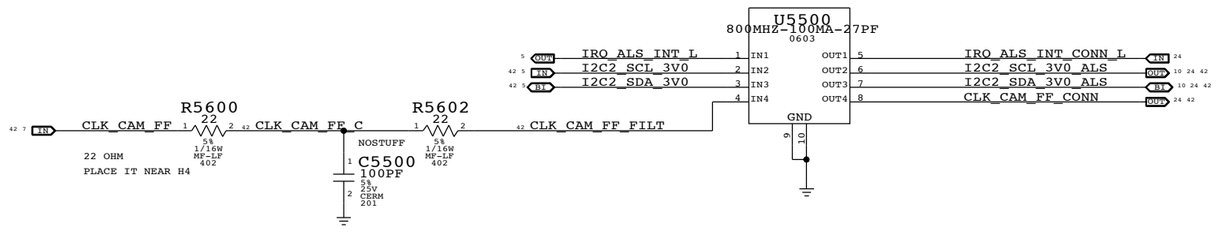
APN: 518S0828

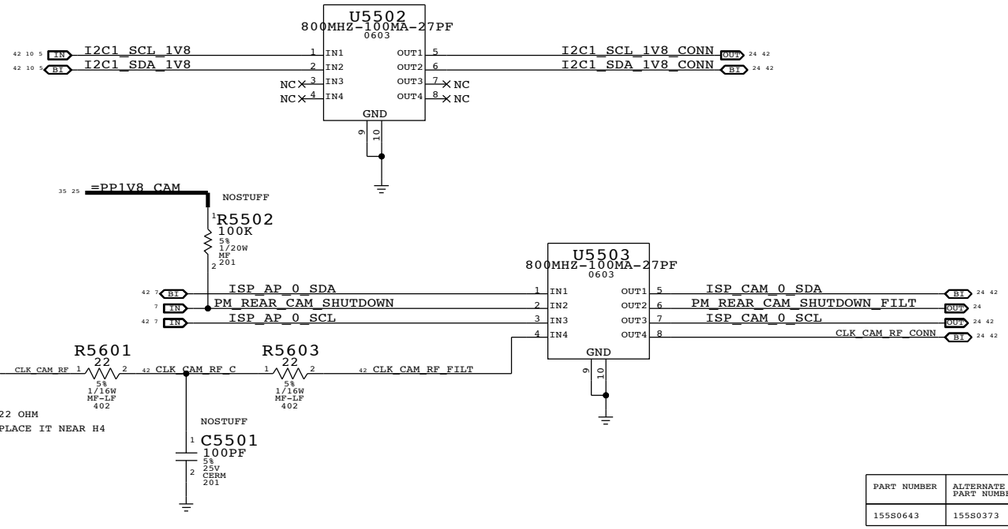


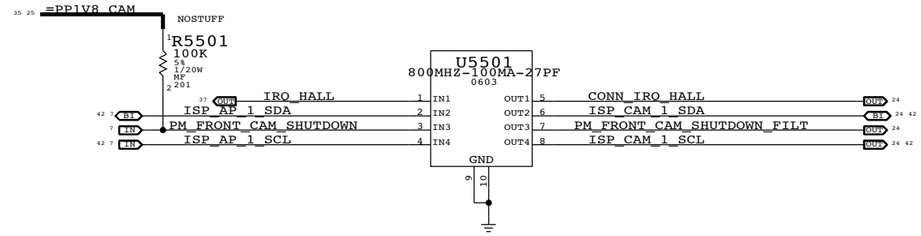
CAM CLOCK 1



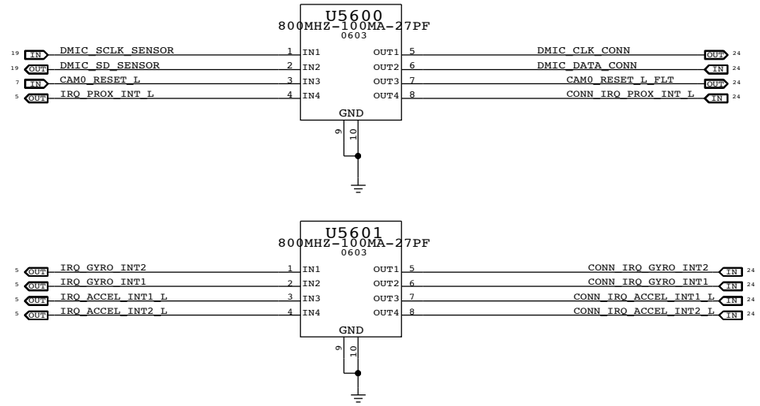


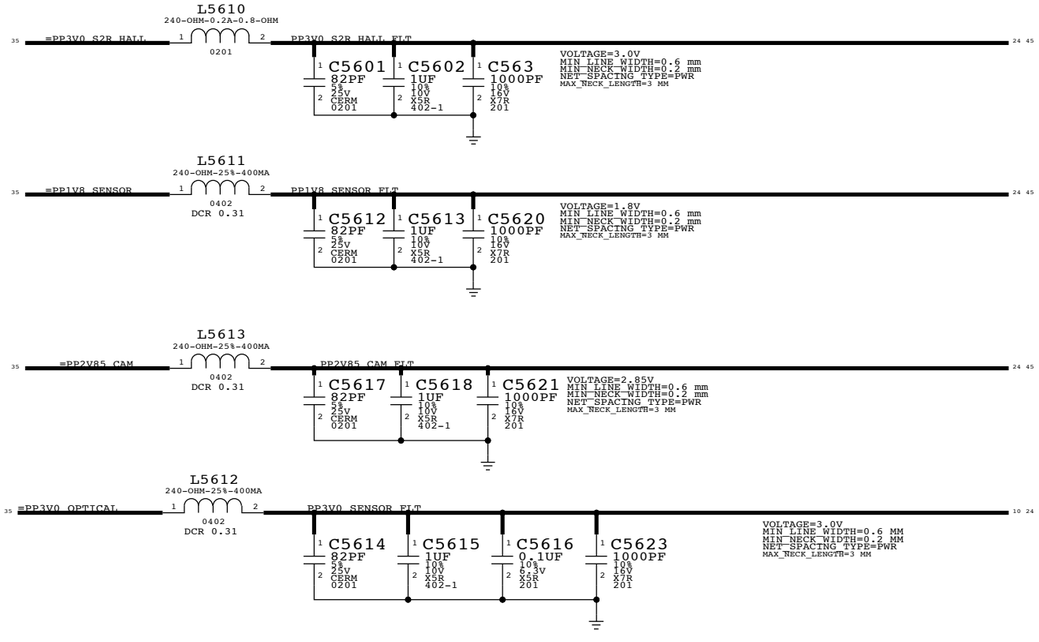


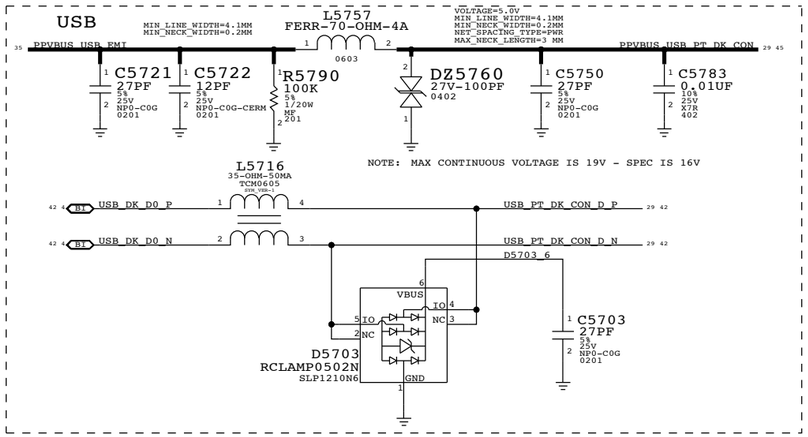


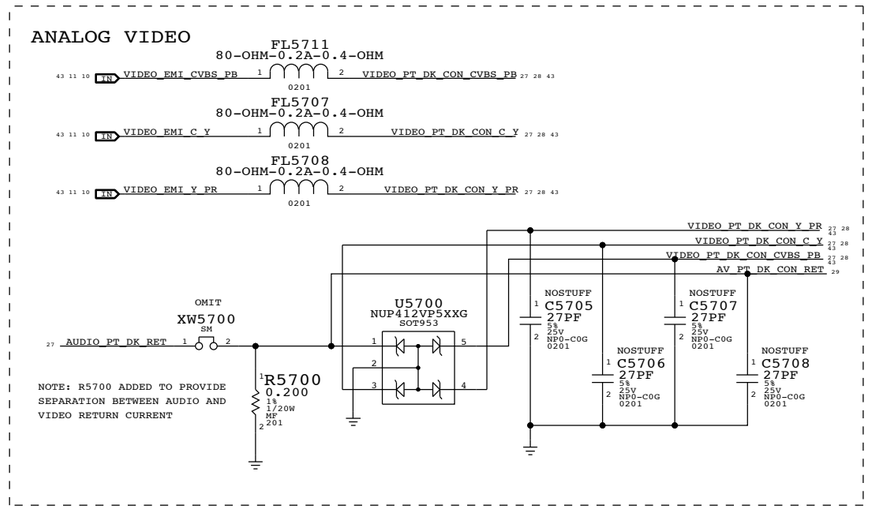


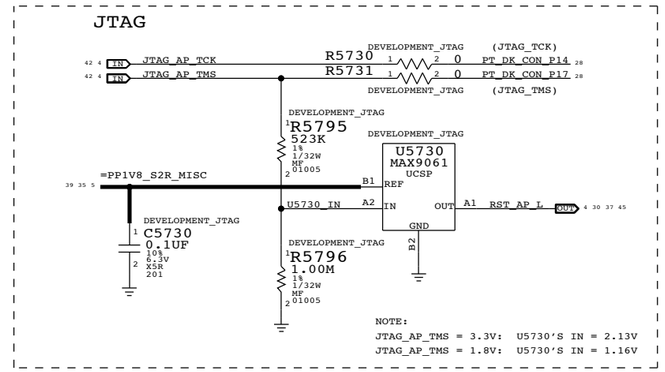
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15580643	15580373	?	U5502,U5503,U5500,U5501,U5600,U5601	RADAR:8376668

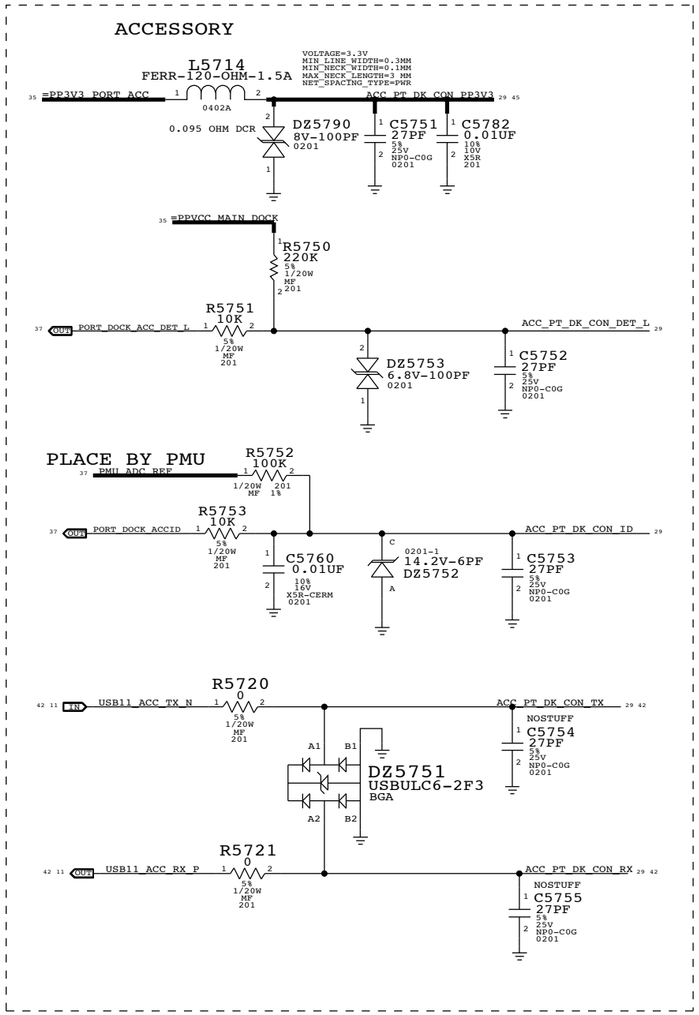

U5600
800MHZ-100MA-27PF
0603
DMIC_SCLK_SENSOR
DMIC_SD_SENSOR
CAM0_RESET_L
IRQ_PROX_INT_L
DMIC_CLK_CONN
DMIC_DATA_CONN
CAM0_RESET_L_FLT
CONN_IRQ_PROX_INT_L
GND
U5601
800MHZ-100MA-27PF
0603
IRQ_GYRO_INT2
IRQ_GYRO_INT1
IRQ_ACCEL_INT1_L
IRQ_ACCEL_INT2_L
CONN_IRQ_GYRO_INT2
CONN_IRQ_GYRO_INT1
CONN_IRQ_ACCEL_INT1_L
CONN_IRQ_ACCEL_INT2_L
GND

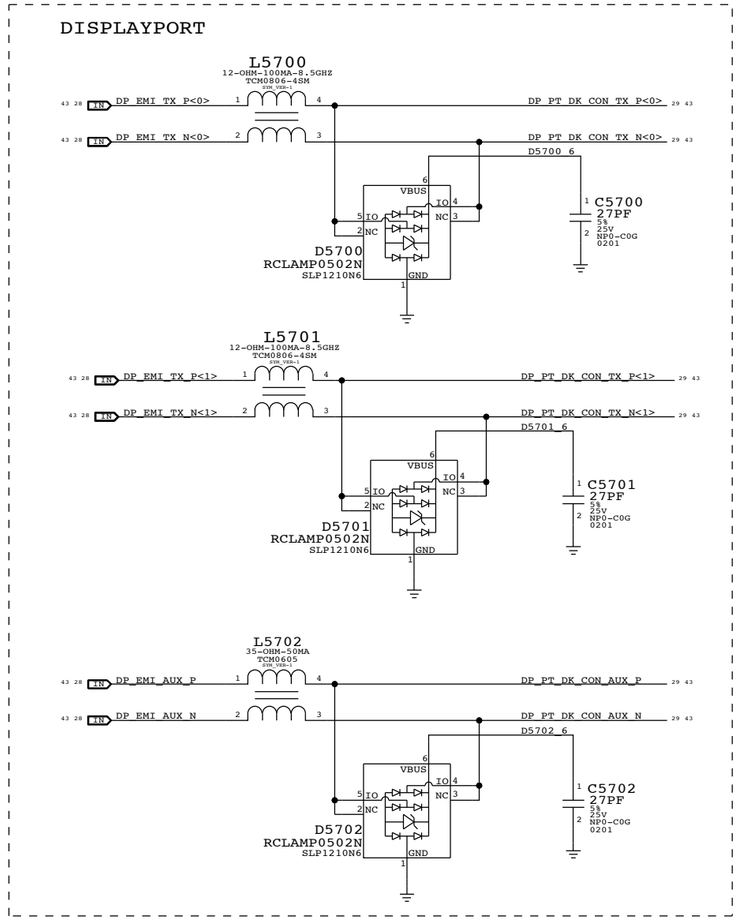

L5610
240-OHM-0.2A-0.8-OHM
0201
=PP3V0_S2R_HALL
PP3V0_S2R_HALL_FLT
C5601
82PF
5%
25V
C0G
0201
C5602
1UF
10%
10V
X5R
402-1
C563
1000PF
10%
16V
X7R
201
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
L5611
240-OHM-25%-400MA
0402
DCR 0.31
=PP1V8_SENSOR
PP1V8_SENSOR_FLT
C5612
82PF
5%
25V
C0G
0201
C5613
1UF
10%
10V
X5R
402-1
C5620
1000PF
10%
16V
X7R
201
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
L5613
240-OHM-25%-400MA
0402
DCR 0.31
=PP2V85_CAM
PP2V85_CAM_FLT
C5617
82PF
5%
25V
C0G
0201
C5618
1UF
10%
10V
X5R
402-1
C5621
1000PF
10%
16V
X7R
201
VOLTAGE=2.85V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
L5612
240-OHM-25%-400MA
0402
DCR 0.31
=PP3V0_OPTICAL
PP3V0_SENSOR_FLT
C5614
82PF
5%
25V
C0G
0201
C5615
1UF
10%
10V
X5R
402-1
C5616
0.1UF
10%
6.3V
X5R
201
C5623
1000PF
10%
16V
X7R
201
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

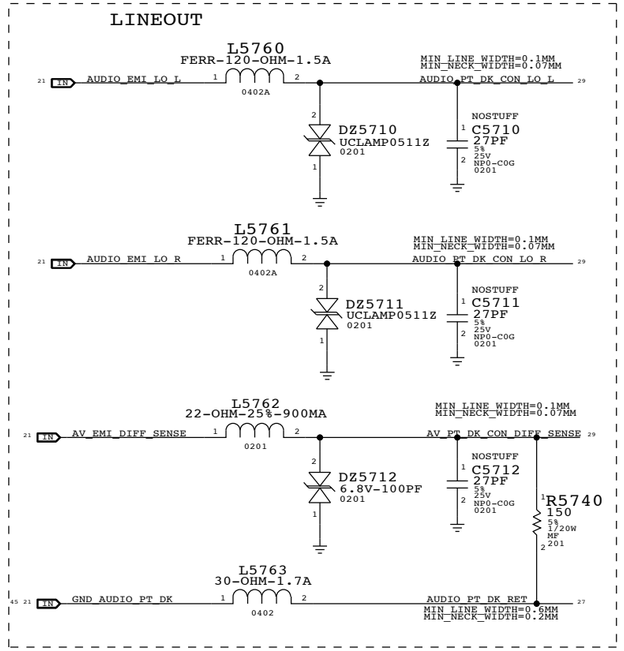


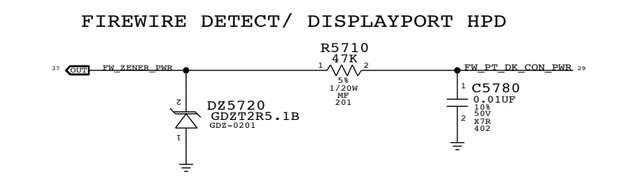






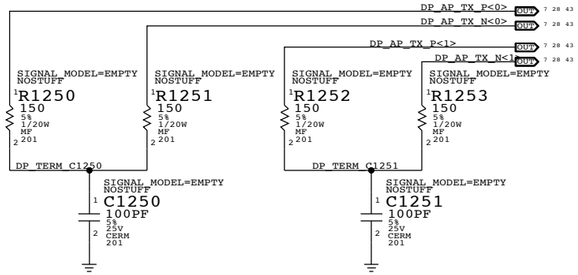




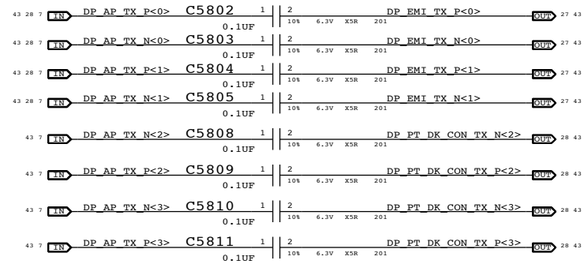


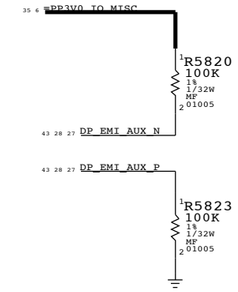
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0090	377S0081		DZ5751	RADAR:8972666
377S0111	377S0099		DZ5710,DZ5711	RADAR:8849707
377S0107	377S0066		D5700,D5701,D5702,D5703	RADAR:8947642
155S0625	155S0559		L5700,L5701	RADAR:8423156
377S0116	377S0108		DZ5760	RADAR:8370432
155S0725	155S0276		FL5699, FL5707, FL5708, FL5711	QTY 4 RADAR:9625553
155S0513	155S0320		L5762	RADAR:9625601

PLACEMENT NOTE: NEAR U0600

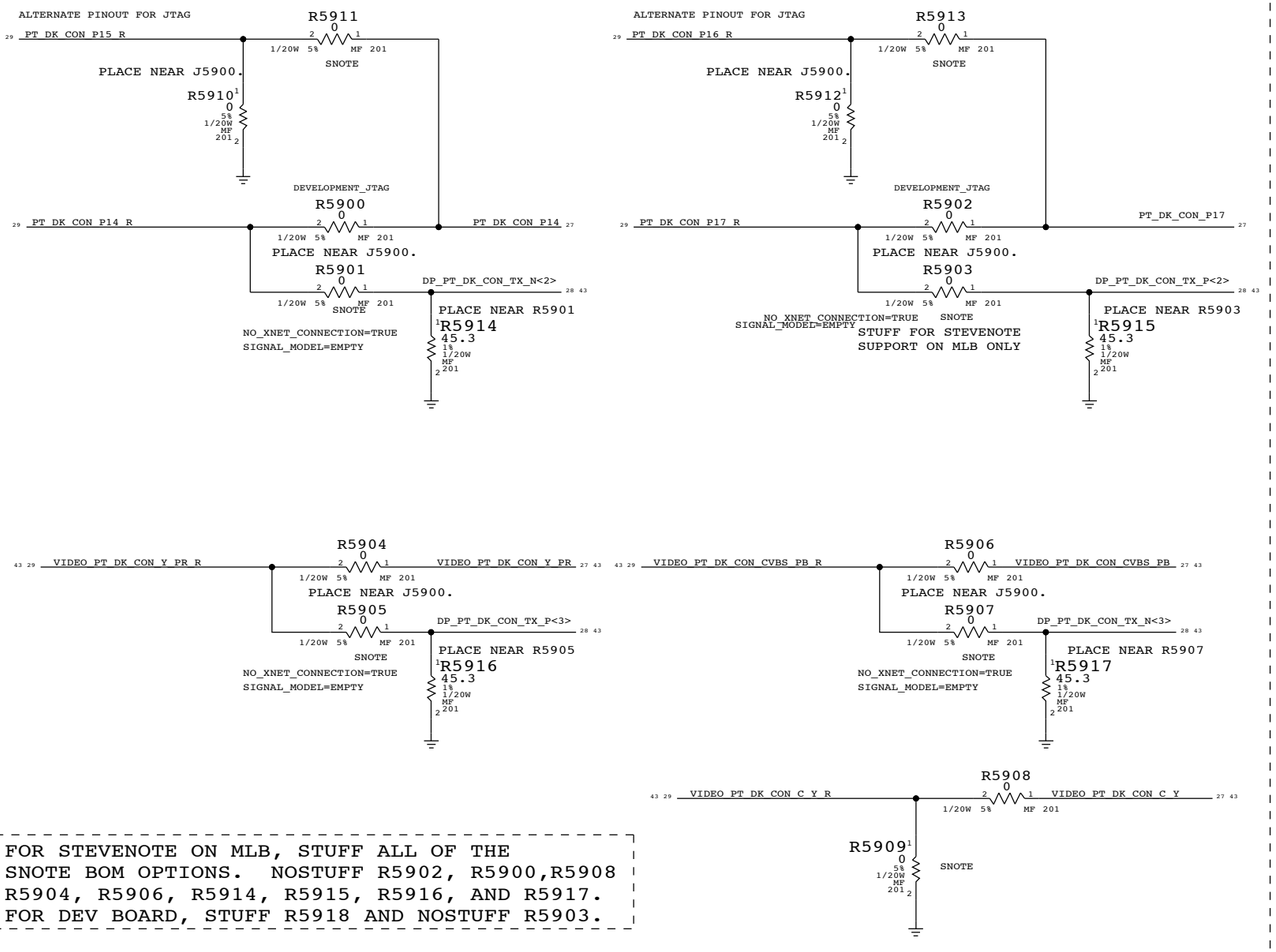


DISPLAYPORT AC COUPLING

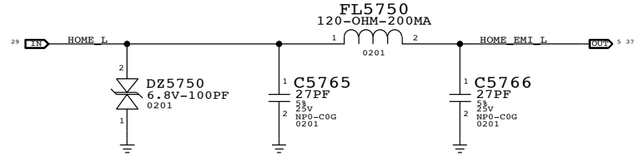


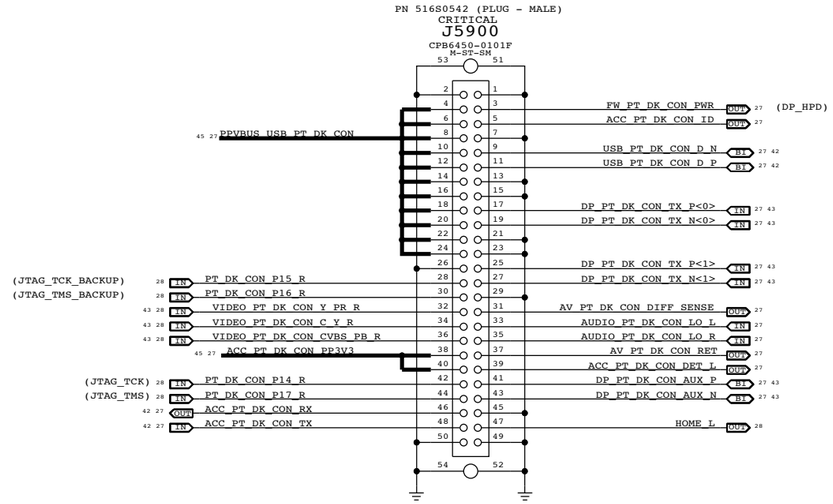


STUFFING OPTIONS FOR DP LANES 2, 3 FOR STEVENOTE.



FOR STEVENOTE ON MLB, STUFF ALL OF THE SNOTE BOM OPTIONS. NOSTUFF R5902, R5900,R5908 R5904, R5906, R5914, R5915, R5916, AND R5917. FOR DEV BOARD, STUFF R5918 AND NOSTUFF R5903.




PN 516S0542 (PLUG - MALE)
CRITICAL
J5900
CPB6450-0101F
M-ST-SM
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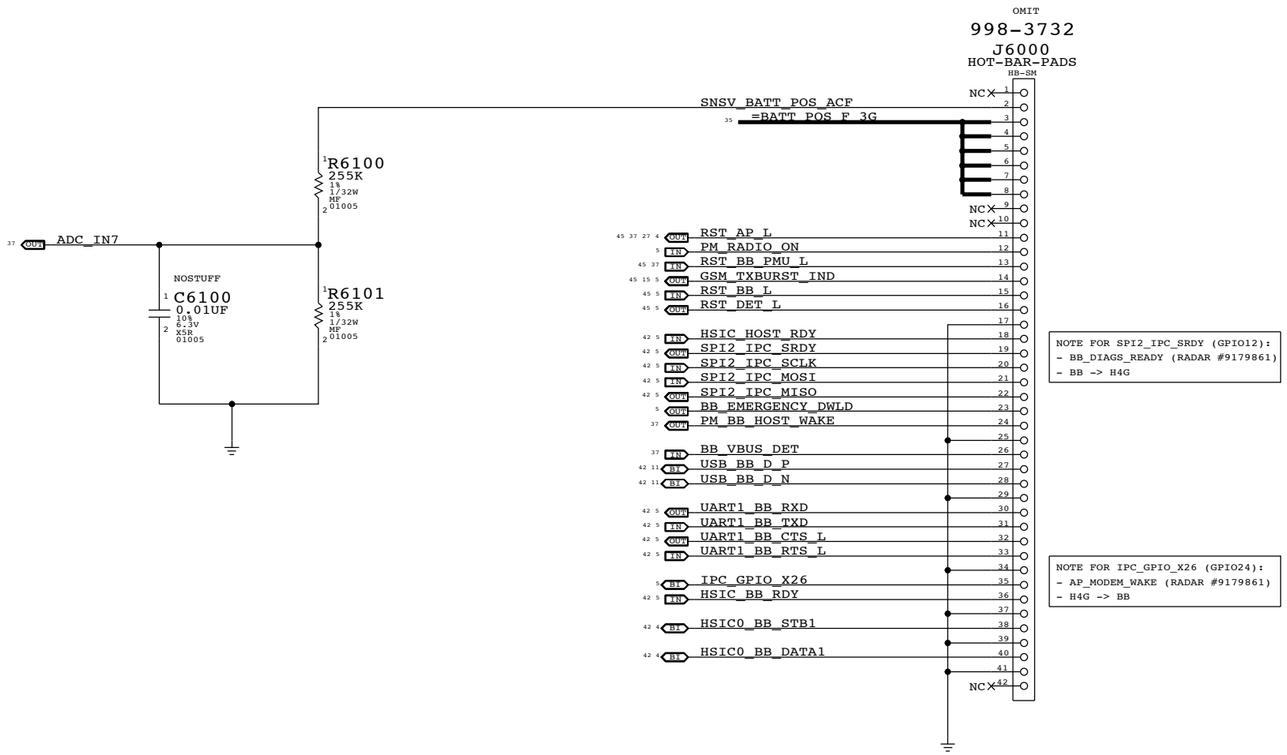
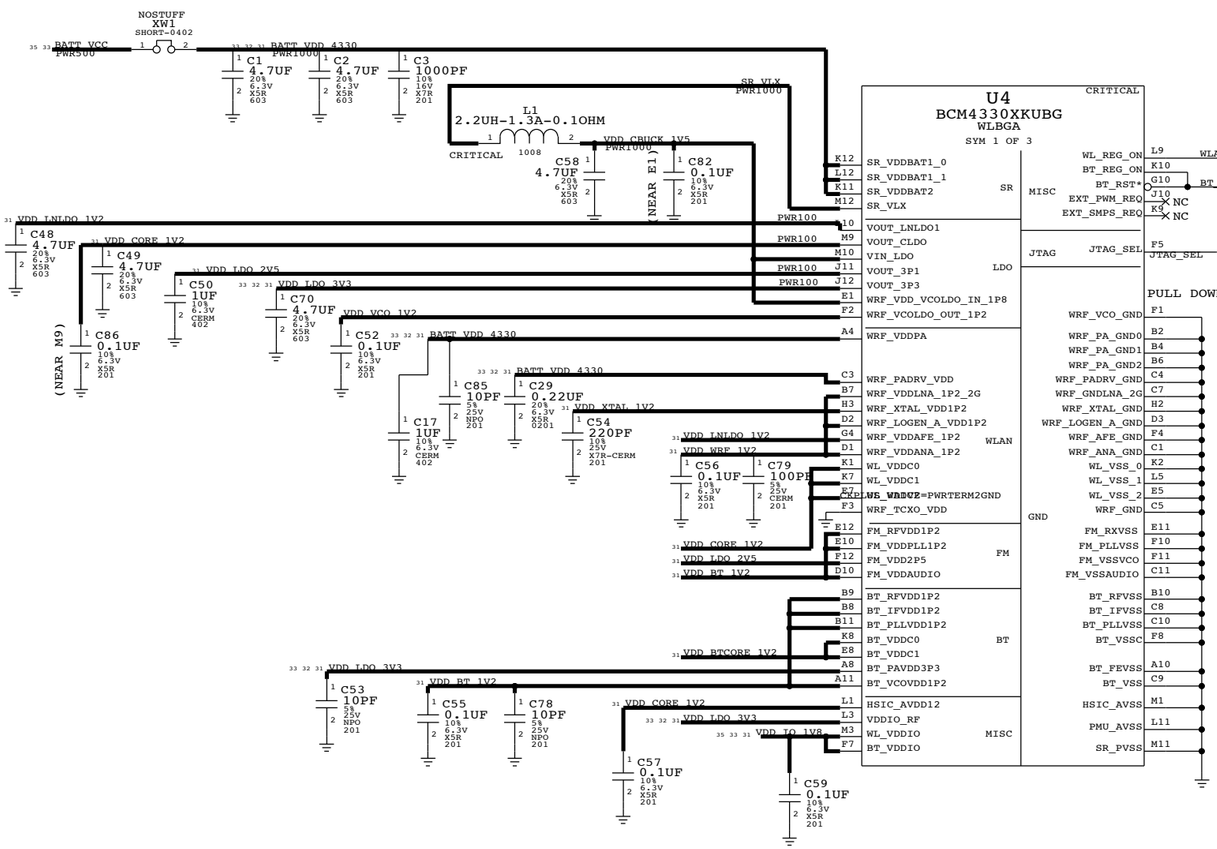
54
52
45 27 PPVBUS_USB_PT_DK_CON
(JTAG_TCK_BACKUP) 28 IN PT_DK_CON_P15_R
(JTAG_TMS_BACKUP) 28 IN PT_DK_CON_P16_R
43 28 IN VIDEO_PT_DK_CON_Y_PR_R
43 28 IN VIDEO_PT_DK_CON_C_Y_R
43 28 IN VIDEO_PT_DK_CON_CVBS_PB_R
45 27 ACC_PT_DK_CON_PP3V3
(JTAG_TCK) 28 IN PT_DK_CON_P14_R
(JTAG_TMS) 28 IN PT_DK_CON_P17_R
42 27 OUT ACC_PT_DK_CON_RX
42 27 IN ACC_PT_DK_CON_TX
FW_PT_DK_CON_PWR OUT 27 (DP_HPD)
ACC_PT_DK_CON_ID OUT 27
USB_PT_DK_CON_D_N BI 27 42
USB_PT_DK_CON_D_P BI 27 42
DP_PT_DK_CON_TX_P<0> IN 27 43
DP_PT_DK_CON_TX_N<0> IN 27 43
DP_PT_DK_CON_TX_P<1> IN 27 43
DP_PT_DK_CON_TX_N<1> IN 27 43
AV_PT_DK_CON_DIFF_SENSE OUT 27
AUDIO_PT_DK_CON_LO_L IN 27
AUDIO_PT_DK_CON_LO_R IN 27
AV_PT_DK_CON_RET OUT 27
ACC_PT_DK_CON_DET_L OUT 27
DP_PT_DK_CON_AUX_P BI 27 43
DP_PT_DK_CON_AUX_N BI 27 43
HOME_L OUT 28

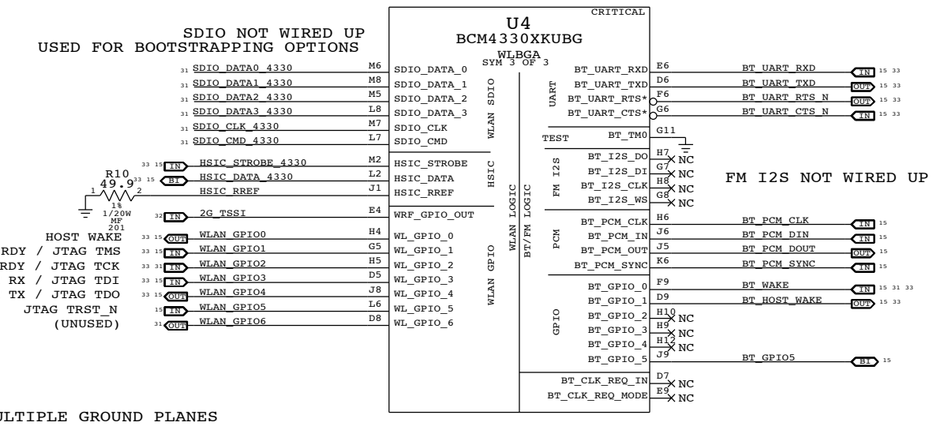
X26 CELLULAR/GPS CONNECTOR



WLAN/BT POWER



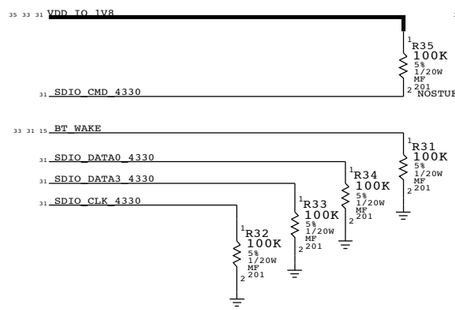
WLAN/BT BASEBAND



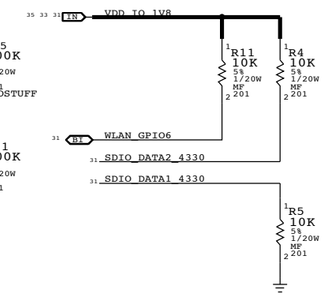
BOOTSTRAPPING OPTIONS

GPIO6	SDIO_DATA2	SDIO_DATA1	MODE	DEF.ARM STATE
0	X	X	SDIO	RESET
1	0	X	GSPI	RESET
1	1	0	HSIC	RUNNING
1	1	1	BOOTLOADERLESS HSIC	RUNNING

PULL-UP/DOWN RESISTORS



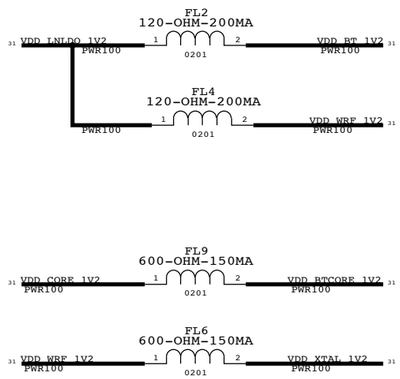
BOOTSTRAP RESISTORS



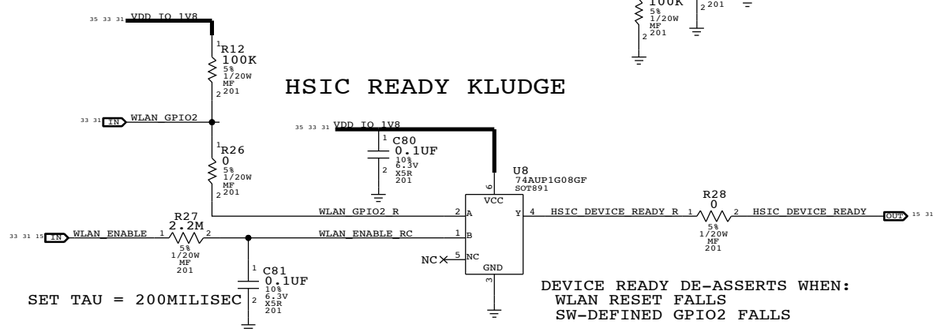
ALTERNATE PARTS AVAILABLE:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0548	311S0398	ANDGATE_TI	U8	TI
155S0657	155S0537	FERRITE_TY	FL2,FL4	TAIYO YUDEN
155S0337	155S0444	FERRITE_TDK	FL6,FL9	TDK

SUPPLY FILTERING



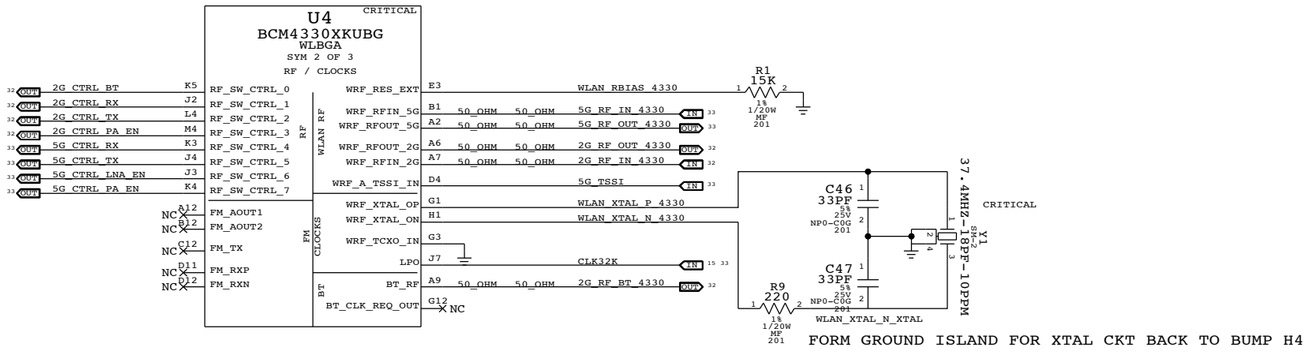
HSIC READY KLUDGE



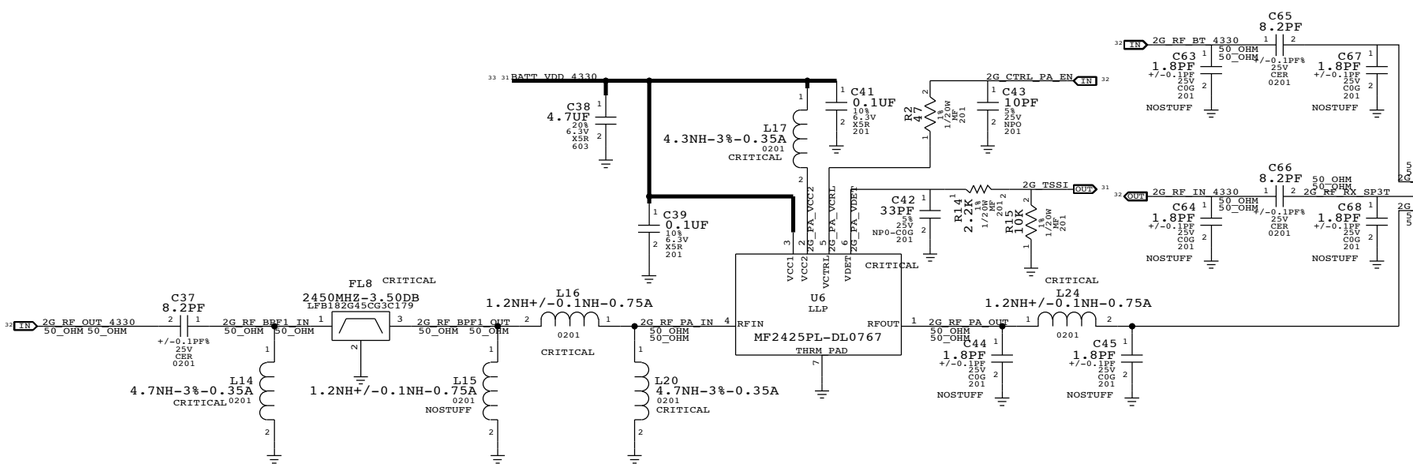
WLAN TRANSCEIVER

RF I/O PLAN

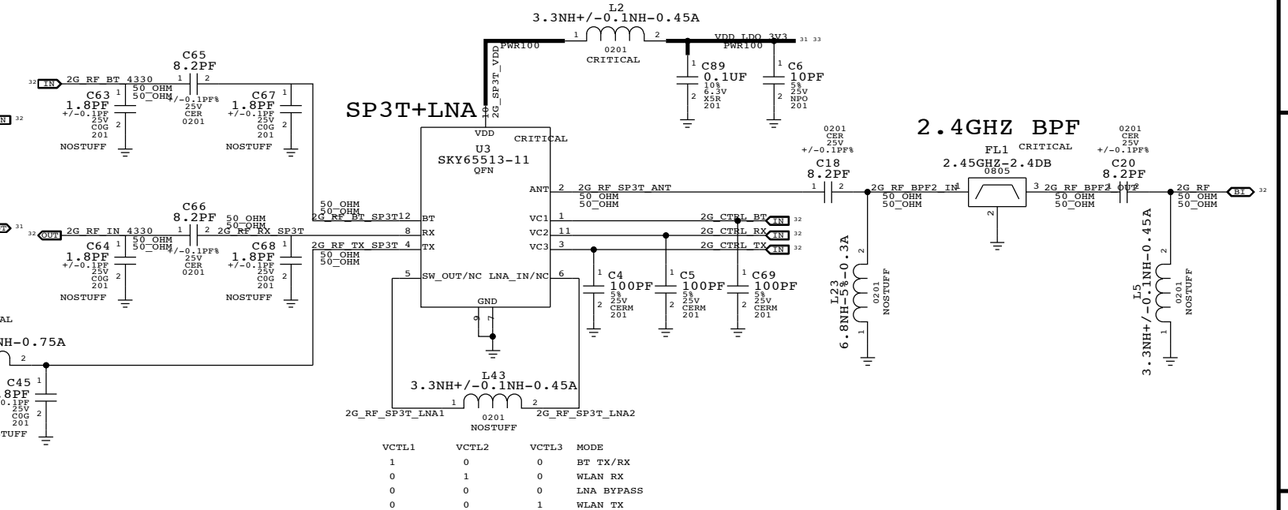
RF_SW_CTRL_0: 2G_CTRL_BT
RF_SW_CTRL_1: 2G_CTRL_RX
RF_SW_CTRL_2: 2G_CTRL_TX
RF_SW_CTRL_3: 2G_CTRL_PA_EN
RF_SW_CTRL_4: 5G_CTRL_RX
RF_SW_CTRL_5: 5G_CTRL_TX
RF_SW_CTRL_6: 5G_CTRL_LNA_EN
RF_SW_CTRL_7: 5G_CTRL_PA_EN



2.4GHZ TX

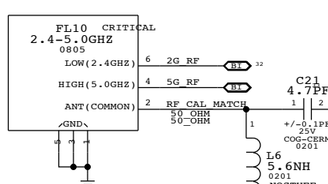


2.4GHZ RX + T/R SWITCH

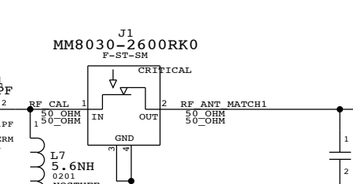


VCTL1	VCTL2	VCTL3	MODE
1	0	0	BT TX/RX
0	1	0	WLAN RX
0	0	0	LNA BYPASS
0	0	1	WLAN TX

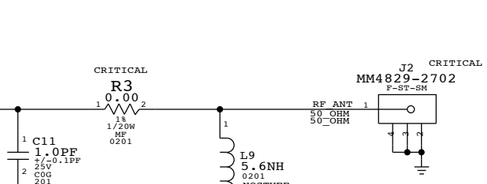
2.4GHZ/5GHZ DIPLEXER



CONDUCTED TEST PORT



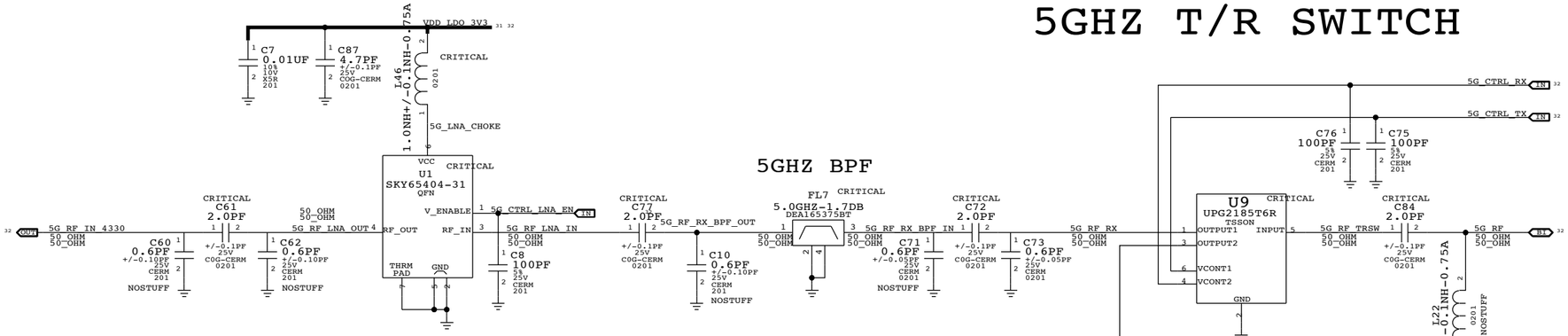
ANTENNA CONNECTOR



5GHZ FRONT-END CONTROL

VCRL1	VCTL2	PA_EN	LNA_EN	MODE
1	0	0	1	RX SUPERBYPASS MODE -- 26DB GAIN STEP
0	1	0	1	RX
1	0	1	0	TX

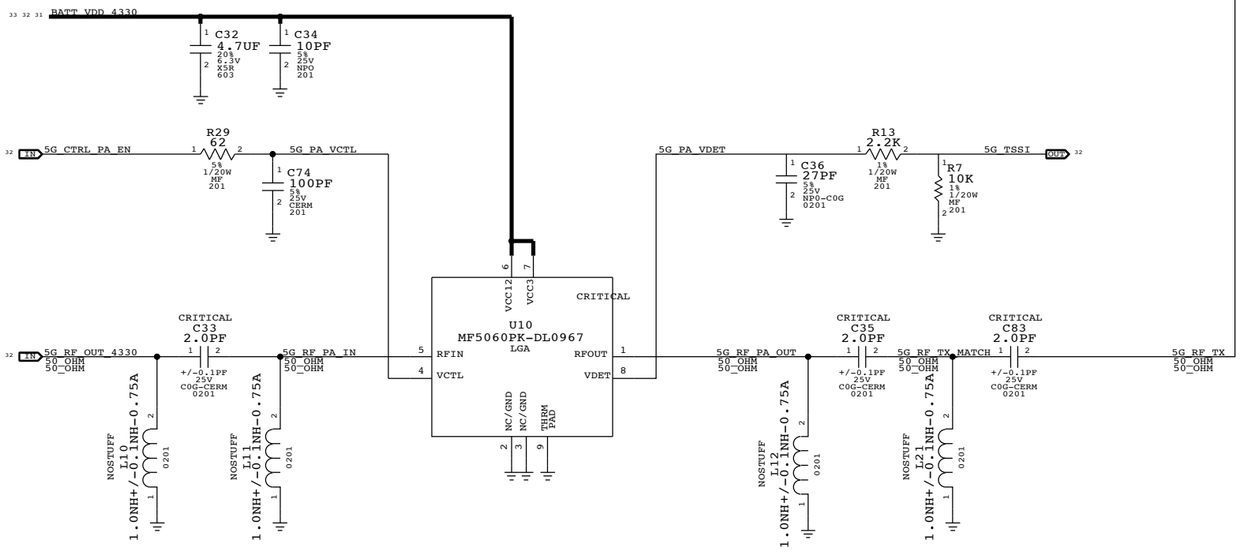
5GHZ LNA



5GHZ BPF

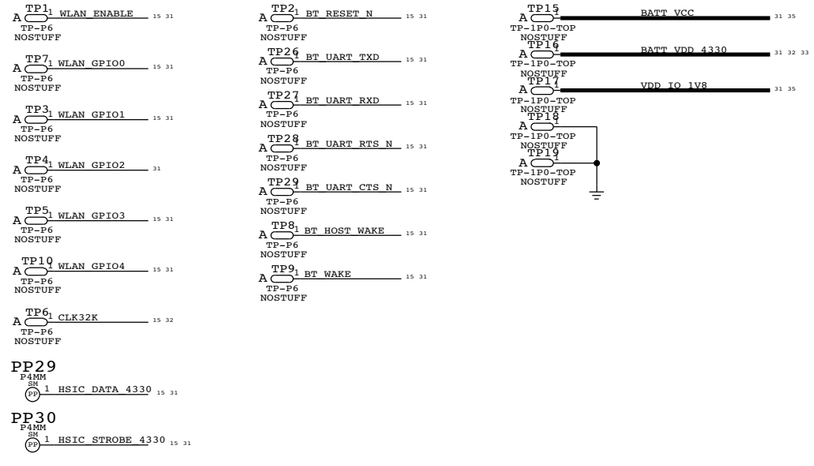
5GHZ T/R SWITCH

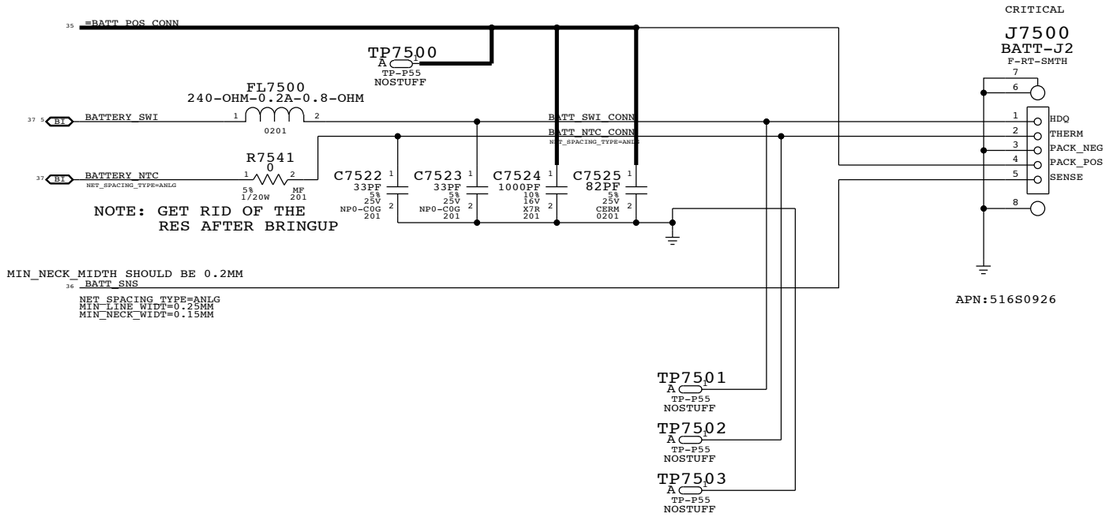
5GHZ PA



TEST POINTS

TEST AND PROBE POINTS




35 =BATT_POS_CONN
TP7500
A
TP-P55
NOSTUFF
FL7500
240-OHM-0.2A-0.8-OHM
0201
37 6 BT BATTERY_SWI
BATT_SWI_CONN
BATT_NTC_CONN
NET_SPACING_TYPE=ANLG
R7541
0
5%
1/20W
MF
201
37 BT BATTERY_NTC
NET_SPACING_TYPE=ANLG
C7522
33PF
5%
25V
NP0-C0G
201
C7523
33PF
5%
25V
NP0-C0G
201
C7524
1000PF
10%
16V
X7R
201
C7525
82PF
5%
25V
CERM
0201
NOTE: GET RID OF THE
RES AFTER BRINGUP
MIN_NECK_MIDTH SHOULD BE 0.2MM
36 BATT_SNS
NET_SPACING_TYPE=ANLG
MIN_LINE_WIDT=0.25MM
MIN_NECK_WIDT=0.15MM
CRITICAL
J7500
BATT-J2
F-RT-SMTH
7
6
1 HDQ
2 THERM
3 PACK_NEG
4 PACK_POS
5 SENSE
8
APN:516S0926
TP7501
A
TP-P55
NOSTUFF
TP7502
A
TP-P55
NOSTUFF
TP7503
A
TP-P55
NOSTUFF

POWER CONN / ALIAS

LDO RAILS

PROGRAMMABLE ON/OFF

LDO1

PP3V0_GRAPE (45 36)
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_GRAPE (17 18)
→ =PP3V0_GRAPE_MARIO1 (17)
→ =PP3V0_GRAPE_Z1 (18)
→ =PP3V0_GRAPE_Z2 (18)

LDO2

PP1V7_VA_VCP (45 40 36)
MAKE_BASE=TRUE
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V7_VA_VCP (19)

LDO3

PP3V0_VIDEO (45 36)
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_VIDEO_H4 (7)

LDO4

PP3V0_OPTICAL (45 36)
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_OPTICAL (26)

LDO5

PP3V2_LDO5 (45 36)
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V2_LDO5

LDO6

PP3V3_ACC (45 36)
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V3_PORT_ACC (27)

LDO7

PP3V0_VIDEO_BUF (45 36)
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_VIDEO_BUF (11)

LDO8

PP3V2_S2R_USBMUX (45 36)
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V2_S2R_USBMUX (11)

LDO9

PP3V0_IO (45 36)
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_IO_MISC (6 28)
→ =PP3V0_IO_H4 (7 9)
→ =PP3V0_VDDIOD_H4 (9)

LDO10

PP3V0_S2R_HALL (45 36)
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_S2R_HALL (26)
→ =PP3V0_S2R_HALL_CHSW (22)

LDO11

PP2V85_CAM (45 36)
MAKE_BASE=TRUE
VOLTAGE=2.85V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP2V85_CAM (26)

LDO12

PP1V1 (45 36)
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V1_PLL_H4 (4)
→ =PP1V1_MIPI_H4 (7)
→ =PP1V1_DP_PAD_DVDD_H4 (7)
→ =PP1V1_USB_H4 (4)
→ =PP1V1_HSIC_H4 (4)
→ =PP1V1_MIPI_PLL_H4 (4)
→ =PP1V1_EDP_PAD_DVDD_H4 (7)

PP1V8_ALWAYS (45 36)
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_ALWAYS (5)

BUCK RAILS

BUCK0

PP1V25_CPU (45 36)
MAKE_BASE=TRUE
VOLTAGE=1.25V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPVDD_CPU_H4 (9)

BUCK2

PP1V2_SOC (45 36)
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPVDD_SOC_H4 (9)

BUCK3

PP1V8_S2R (45 36)
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_S2R_MISC (5 27 39)
→ VDD_IO_1V8 (31 33)
→ =PP1V8_S2R_DDR (13 14)

CPU1V8_SW (BUCK3)

PP1V8 (36 45)
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_CAM (25)
→ =PP1V8_SENSOR (26)
→ =PP1V8_DP_H4 (7)
→ =PP1V8_AUDIO (19)
→ =PP1V8_H4 (4 7 10)
→ =PP1V8_NAND_H4 (9)
→ =PP1V8_MIPI_H4 (7)
→ =PP1V8_NAND (12)
→ =PP1V8_VDDIO18_H4 (9)
→ =PP1V8_EDP_H4 (7)
→ =PP1V8_VDDIOD_H4 (5 9)
→ =PP1V8_VDDA18_TS (5)

WDIG_SW (BUCK3)

PP1V8_GRAPE (45 36)
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_GRAPE

BUCK4

PP1V2_S2R (45 36)
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V2_S2R_H4 (8)
→ =PP1V2_S2R_DDR (13 14)

BUCK4_SW

PP1V2 (45 36)
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V2_VDDIOD_H4 (8 9)
→ =PP1V2_HSIC_H4 (4)
→ =PP1V2_VDDQ_DDR (13 14)

BUCK5

PP3V3_OUT (45 36)
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3MM
→ =PP3V3_NAND (12)
→ =PP3V3_USB_H4 (4)
→ =PP3V3_NAND_H4 (9)
→ =PP3V3_LCD (16)

VOUT_LED_A

PPLED_OUT_A (45 37)
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPLED_REG_A (16)

VOUT_LED_B

PPLED_OUT_B (45 37)
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPLED_REG_B (16)

CHARGER MAIN

PPVCC_MAIN (45 37 36)
MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPVCC_MAIN_LED (37)
→ =PPVCC_MAIN_AUDIO (19 20 22)
→ =PPVCC_MAIN_DOCK (27)

BATTERY

PPBATT_VCC (45 39 36)
MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.20 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =BATT_POS_F_3G (30)
→ =BATT_POS_CONN (34)
→ BATT_VCC (31 33) USED BY WIFI_BT

USB POWER INPUT

PPVBUS_USB_EMI (27)
→ PPVBUS_USB_DCIN (36 45)
MAKE_BASE=TRUE

LCM_BOOST

PP5V25_VLCM2 (45 37)
MAKE_BASE=TRUE
VOLTAGE=5.25V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP5V25_GRAPE_VDDH

GND
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.15MM
NET_SPACING_TYPE=GND
MAX_NECK_LENGTH=5 MM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0392	197S0299	?	Y8138	RADAR:8788152
152S1452	152S1292	?	L8128	RADAR:8376462

ALTERNATE FOUNDRY

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

USB REVERSE VOLTAGE PROTECTION

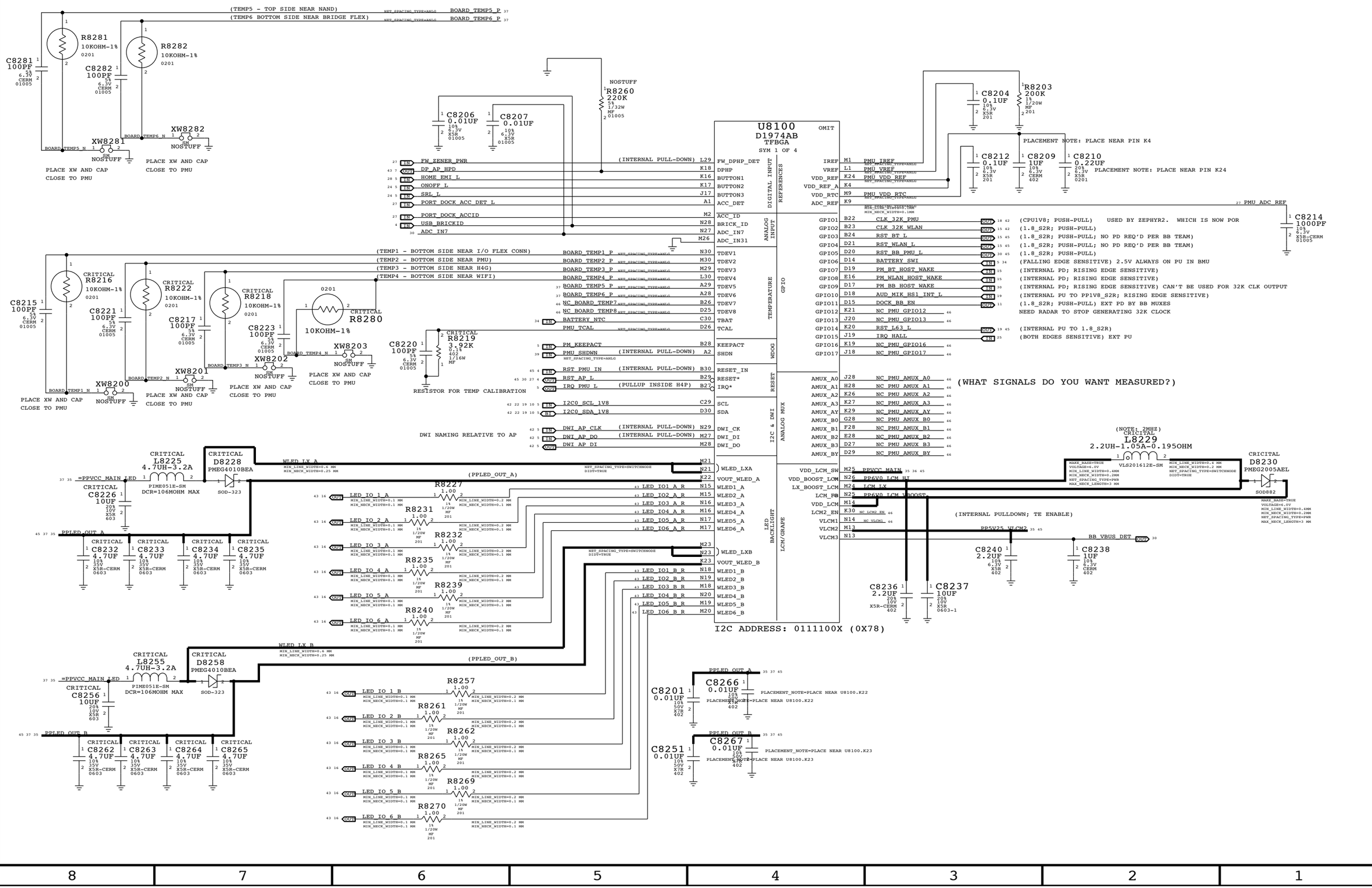
NOTE: FOR NO BATTERY SITUATION

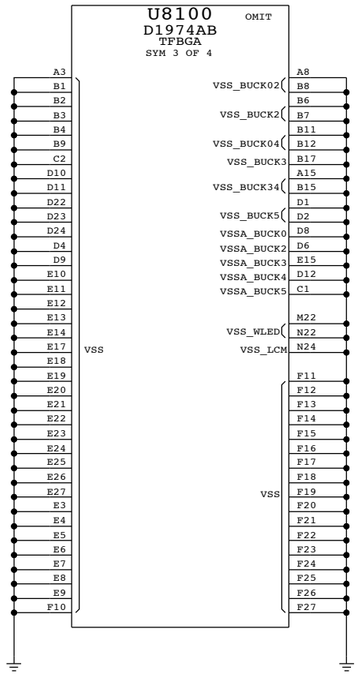
VCC_MAIN BYPASS
TOTAL CAPS = ~400UF
(DISTRIBUTED AND NO DE-RATING)
(PLACE ONE 10UF CAP AT EACH VDD INPUT)

NOTE: CONCERNED ABOUT ESR > 20MOHM
NOTE: CHANGE SOME 1UF TO 4.7UF

LDO BYPASS

ADDITIONAL DISTRIBUTED 25UF (NO DE-RATING)
ADDITIONAL DISTRIBUTED 30UF (NO DE-RATING)
ADDITIONAL DISTRIBUTED 14UF (NO DE-RATING)
ADDITIONAL DISTRIBUTED 47UF (NO DE-RATING)


(TEMP5 - TOP SIDE NEAR NAND)
(TEMP6 BOTTOM SIDE NEAR BRIDGE FLEX)
BOARD_TEMP5_P
BOARD_TEMP6_P
R8281 10KOHM-1% 0201
R8282 10KOHM-1% 0201
C8281 100PF 5% 6.3V CERM 01005
C8282 100PF 5% 6.3V CERM 01005
XW8281 NOSTUFF
XW8282 NOSTUFF
PLACE XW AND CAP CLOSE TO PMU
C8206 0.01UF 10% 6.3V X5R 01005
C8207 0.01UF 10% 6.3V X5R 01005
R8260 220K 5% 1/32W MF 01005
NOSTUFF
U8100 D1974AB TFBGA SYM 1 OF 4 OMIT
FW_DPHP_DET L29
DPHP K18
BUTTON1 K16
BUTTON2 K17
BUTTON3 J17
ACC_DET A1
ACC_ID M2
BRICK_ID N28
ADC_IN7 N27
ADC_IN31 M26
TDEV1 N30
TDEV2 M30
TDEV3 M29
TDEV4 L30
TDEV5 A29
TDEV6 A28
TDEV7 B26
TDEV8 D25
TBAT C30
TCAL D26
KEEPACT B28
SHDN A2
RESET_IN B30
RESET* B29
IRQ* B27
SCL C29
SDA D30
DWI_CK N29
DWI_DI M27
DWI_DO M28
WLED_LXA M21
WLED_LXA N21
VOUT_WLED_A K22
WLED1_A N15
WLED2_A M15
WLED3_A N16
WLED4_A M16
WLED5_A N17
WLED6_A M17
WLED_LXB M23
WLED_LXB N23
VOUT_WLED_B K23
WLED1_B N18
WLED2_B N19
WLED3_B M18
WLED4_B N20
WLED5_B M19
WLED6_B M20
DIGITAL INPUT
REFERENCES
ANALOG INPUT
TEMPERATURE
GPIO
WDOG
RESET
I2C & DWI
ANALOG MUX
LED BACKLIGHT
LCM/GRAPE
I2C ADDRESS: 0111100X (0X78)
C8204 0.1UF 10% 6.3V X5R 201
R8203 200K 1% 1/20W MF 201
PLACEMENT NOTE: PLACE NEAR PIN K4
C8212 0.1UF 10% 6.3V X5R 201
C8209 1UF 10% 6.3V CERM 402
C8210 0.22UF 20% 6.3V X5R 0201 PLACEMENT NOTE: PLACE NEAR PIN K24
C8214 1000PF 10% 6.3V X5R-CERM 01005
PMU_ADC_REF
GPIO1 B22 CLK_32K_PMU (CPU1V8; PUSH-PULL) USED BY ZEPHYR2. WHICH IS NOW POR
GPIO2 B23 CLK_32K_WLAN (1.8_S2R; PUSH-PULL)
GPIO3 B24 RST_BT_L (1.8_S2R; PUSH-PULL; NO PD REQ'D PER BB TEAM)
GPIO4 D21 RST_WLAN_L (1.8_S2R; PUSH-PULL; NO PD REQ'D PER BB TEAM)
GPIO5 D20 RST_BB_PMU_L (1.8_S2R; PUSH-PULL)
GPIO6 D14 BATTERY_SWI (FALLING EDGE SENSITIVE) 2.5V ALWAYS ON PU IN BMU
GPIO7 D19 PM_BT_HOST_WAKE (INTERNAL PD; RISING EDGE SENSITIVE)
GPIO8 E16 PM_WLAN_HOST_WAKE (INTERNAL PD; RISING EDGE SENSITIVE)
GPIO9 D17 PM_BB_HOST_WAKE (INTERNAL PD; RISING EDGE SENSITIVE) CAN'T BE USED FOR 32K CLK OUTPUT
GPIO10 D18 AUD_MIK_HS1_INT_L (INTERNAL PU TO PP1V8_S2R; RISING EDGE SENSITIVE)
GPIO11 D15 DOCK_BB_EN (1.8_S2R; PUSH-PULL) EXT PD BY BB MUXES
GPIO12 K21 NC_PMU_GPIO12 NEED RADAR TO STOP GENERATING 32K CLOCK
GPIO13 J20 NC_PMU_GPIO13
GPIO14 K20 RST_L63_L (INTERNAL PU TO 1.8_S2R)
GPIO15 J19 IRQ_HALL (BOTH EDGES SENSITIVE) EXT PU
GPIO16 K19 NC_PMU_GPIO16
GPIO17 J18 NC_PMU_GPIO17
AMUX_A0 J28 NC_PMU_AMUX_A0
AMUX_A1 H28 NC_PMU_AMUX_A1
AMUX_A2 K26 NC_PMU_AMUX_A2
AMUX_A3 K27 NC_PMU_AMUX_A3
AMUX_AY K29 NC_PMU_AMUX_AY
AMUX_B0 G28 NC_PMU_AMUX_B0
AMUX_B1 F28 NC_PMU_AMUX_B1
AMUX_B2 E28 NC_PMU_AMUX_B2
AMUX_B3 D27 NC_PMU_AMUX_B3
AMUX_BY D29 NC_PMU_AMUX_BY
(WHAT SIGNALS DO YOU WANT MEASURED?)
VDD_LCM_SW M25 PPVCC_MAIN
VDD_BOOST_LCM N26 PP6V0_LCM_BT
LX_BOOST_LCM M24 LCM_LX
LCM_FB N25 PP6V0_LCM_VBOOST
VDD_LCM M14
LCM2_EN K30 NC_LCM2_EN
VLCM1 N14 NC_VLCM1
VLCM2 M13
VLCM3 N13
(INTERNAL PULLDOWN; TE ENABLE)
PP5V25_WLCM2
BB_VBUS_DET
C8240 2.2UF 20% 6.3V X5R 402
C8238 1UF 10% 6.3V CERM 402
C8236 2.2UF 20% 10V X5R-CERM 402
C8237 10UF 20% 10V X5R 0603-1
(NOTE: 2MHZ)
CRICITAL L8229 2.2UH-1.05A-0.195OHM
VLS201612E-SM
CRICITAL D8230 PMEG2005AEL SOD882
CRITICAL R8216 10KOHM-1% 0201
CRITICAL R8222 10KOHM-1% 0201
CRITICAL R8218 10KOHM-1% 0201
0201 CRITICAL R8280 10KOHM-1%
C8215 100PF 5% 6.3V CERM 01005
C8221 100PF 5% 6.3V CERM 01005
C8217 100PF 5% 6.3V CERM 01005
C8223 100PF 5% 6.3V CERM 01005
XW8200 NOSTUFF
XW8201 NOSTUFF
XW8202 NOSTUFF
XW8203 NOSTUFF
PLACE XW AND CAP CLOSE TO PMU
(TEMP1 - BOTTOM SIDE NEAR I/O FLEX CONN)
(TEMP2 - BOTTOM SIDE NEAR PMU)
(TEMP3 - BOTTOM SIDE NEAR H4G)
(TEMP4 - BOTTOM SIDE NEAR WIFI)
BOARD_TEMP1_P
BOARD_TEMP2_P
BOARD_TEMP3_P
BOARD_TEMP4_P
BOARD_TEMP5_P
BOARD_TEMP6_P
NC_BOARD_TEMP7
NC_BOARD_TEMP8
BATTERY_NTC
PMU_TCAL
C8220 100PF 5% 6.3V CERM 01005
CRITICAL R8219 3.92K 0.1% 402 1/16W MF
RESISTOR FOR TEMP CALIBRATION
PM_KEEPACT
PMU_SHDWN (INTERNAL PULL-DOWN)
RST_PMU_IN (INTERNAL PULL-DOWN)
RST_AP_L
IRQ_PMU_L (PULLUP INSIDE H4P)
I2C0_SCL_1V8
I2C0_SDA_1V8
DWI NAMING RELATIVE TO AP
DWI_AP_CLK (INTERNAL PULL-DOWN)
DWI_AP_DO (INTERNAL PULL-DOWN)
DWI_AP_DI
CRITICAL L8225 4.7UH-3.2A PIME051E-SM DCR=106MOHM MAX
CRITICAL D8228 PMEG4010BEA SOD-323
=PPVCC_MAIN_LED
CRITICAL C8226 10UF 20% 10V X5R 603
PPLED_OUT_A
CRITICAL C8232 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8233 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8234 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8235 4.7UF 10% 35V X5R-CERM 0603
WLED_LX_A
(PPLED_OUT_A)
R8227 1.00 1% 1/20W MF 201
R8231 1.00 1% 1/20W MF 201
R8232 1.00 1% 1/20W MF 201
R8235 1.00 1% 1/20W MF 201
R8239 1.00 1% 1/20W MF 201
R8240 1.00 1% 1/20W MF 201
LED_IO_1_A
LED_IO_2_A
LED_IO_3_A
LED_IO_4_A
LED_IO_5_A
LED_IO_6_A
LED_IO1_A_R
LED_IO2_A_R
LED_IO3_A_R
LED_IO4_A_R
LED_IO5_A_R
LED_IO6_A_R
CRITICAL L8255 4.7UH-3.2A PIME051E-SM DCR=106MOHM MAX
CRITICAL D8258 PMEG4010BEA SOD-323
=PPVCC_MAIN_LED
CRITICAL C8256 10UF 20% 10V X5R 603
PPLED_OUT_B
CRITICAL C8262 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8263 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8264 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8265 4.7UF 10% 35V X5R-CERM 0603
WLED_LX_B
(PPLED_OUT_B)
R8257 1.00 1% 1/20W MF 201
R8261 1.00 1% 1/20W MF 201
R8262 1.00 1% 1/20W MF 201
R8265 1.00 1% 1/20W MF 201
R8269 1.00 1% 1/20W MF 201
R8270 1.00 1% 1/20W MF 201
LED_IO_1_B
LED_IO_2_B
LED_IO_3_B
LED_IO_4_B
LED_IO_5_B
LED_IO_6_B
LED_IO1_B_R
LED_IO2_B_R
LED_IO3_B_R
LED_IO4_B_R
LED_IO5_B_R
LED_IO6_B_R
C8201 0.01UF 10% 50V X7R 402
C8266 0.01UF 10% 50V X7R 402
C8251 0.01UF 10% 50V X7R 402
C8267 0.01UF 10% 50V X7R 402
PLACEMENT_NOTE=PLACE NEAR U8100.K22
PLACEMENT_NOTE=PLACE NEAR U8100.K23


U8100
D1974AB
TFBGA
SYM 3 OF 4
OMIT
A3
B1
B2
B3
B4
B9
C2
D10
D11
D22
D23
D24
D4
D9
E10
E11
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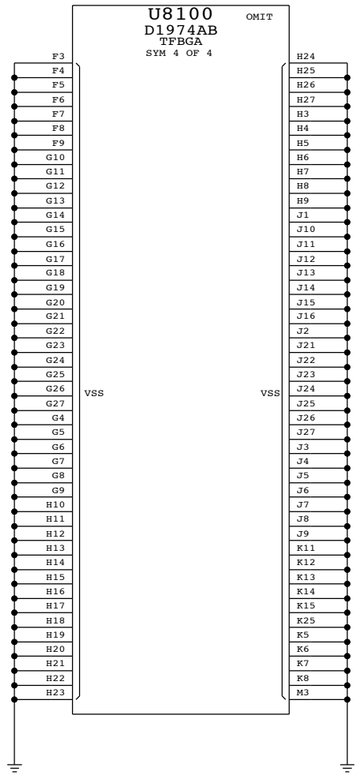
E26
E27
E3
E4
E5
E6
E7
E8
E9
F10
VSS
A8
VSS_BUCK02
B8
B6
VSS_BUCK2
B7
B11
VSS_BUCK04
B12
VSS_BUCK3
B17
A15
VSS_BUCK34
B15
D1
VSS_BUCK5
D2
VSSA_BUCK0
D8
VSSA_BUCK2
D6
VSSA_BUCK3
E15
VSSA_BUCK4
D12
VSSA_BUCK5
C1
M22
VSS_WLED
N22
VSS_LCM
N24
F11
F12
F13
F14
F15
F16
F17
F18
VSS
F19
F20
F21
F22
F23
F24
F25
F26
F27


U8100
D1974AB
TFBGA
SYM 4 OF 4
OMIT
F3
F4
F5
F6
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F9
G10
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H23
VSS
H24
H25
H26
H27
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H6
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H8
H9
J1
J10
J11
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J4
J5
J6
J7
J8
J9
K11
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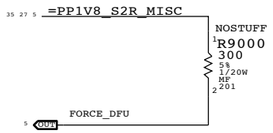
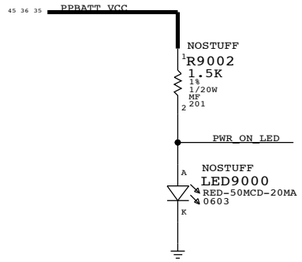
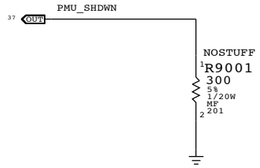
K14
K15
K25
K5
K6
K7
K8
M3
VSS

DEBUG RESET ACCESS

PLACE OUTSIDE OF CAN







PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

FID9300 FID 0P5SM1P0SQ-NSP
FID9301 FID 0P5SM1P0SQ-NSP
FID9302 FID 0P5SM1P0SQ-NSP
FID9303 FID 0P5SM1P0SQ-NSP
FID9304 FID 0P5SM1P0SQ-NSP
FID9305 FID 0P5SM1P0SQ-NSP

SL9300 TH-NSP SL-1.1X0.4-1.4X0.7
SL9301 TH-NSP SL-1.1X0.4-1.4X0.7
SL9302 TH-NSP SL-1.1X0.4-1.4X0.7
SL9304 TH-NSP SL-1.1X0.4-1.4X0.7
SL9305 TH-NSP SL-1.1X0.4-1.4X0.7
SL9306 TH-NSP SL-1.1X0.4-1.4X0.7
SL9310 TH-NSP SL-1.1X0.4-1.4X0.7
SL9312 TH-NSP SL-1.1X0.4-1.4X0.7
SL9313 TH-NSP SL-1.1X0.4-1.4X0.7
SL9314 TH-NSP SL-1.1X0.4-1.4X0.7
SL9315 TH-NSP SL-1.1X0.4-1.4X0.7
SL9316 TH-NSP SL-1.1X0.4-1.4X0.7

PROBE POINTS

PP0 P4MM SM	CODEC_LINE_OUT_REF	19 21
PP1 P4MM SM	CODEC_LINE_OUT_R	19 21
PP2 P4MM SM	AUD_SPKR_AMP2_PBUS	20
PP3 P4MM SM	AUD_SPKR_AMP1_PBUS	20
PP4 P4MM SM	CODEC_LINE_OUT_L	19 21
PP5 P4MM SM	DDR0_DQS_P<0>	8 13 44
PP6 P4MM SM	DDR0_DQ<0>	8 13 44
PP7 P4MM SM	DDR0_DQS_N<0>	8 13 44
PP8 P4MM SM	DDR0_DQS_N<1>	8 13 44
PP9 P4MM SM	DDR0_DQ<14>	8 13 44
PP10 P4MM SM	HSIC1_WLAN_DATA1	4 15 42
PP11 P4MM SM	HSIC1_WLAN_STB1	4 15 42
PP12 P4MM SM	Z1_BON_L<5>	17 18
PP13 P4MM SM	Z1_B_ADR<2>	17 18
PP14 P4MM SM	Z1_B_ADR<1>	17 18
PP15 P4MM SM	Z1_B_ADR<0>	17 18
PP16 P4MM SM	Z1_MISO	17 18
PP17 P4MM SM	Z1_BON_L<4>	17 18
PP18 P4MM SM	PP1V7_VA_VCP	35 36 45
PP19 P4MM SM	CONN_AUD_HEADSET_CHS_RET2	23 24
PP20 P4MM SM	CONN_AUD_HEADSET_CHS_MIC2	23 24
PP21 P4MM SM	CONN_AUD_HEADSET_DET	23 24
PP22 P4MM SM	AUD_HP1_DET_H	23
PP23 P4MM SM	AUD_HS_MIC2_RET	22 23
PP24 P4MM SM	AUD_HS_MIC1_HI	22 23
PP25 P4MM SM	AUD_HS_MIC1_RET	22 23
PP26 P4MM SM	AUD_HS_MIC2_HI	22 23

MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA06-06	MM	16.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES
45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL1,ISL12	Y	0.110 MM	0.060 MM	3.0 MM		
45_OHM_SE	ISL5,ISL8	Y	0.077 MM	0.060 MM	3.0 MM		
45_OHM_SE	ISL3	Y	0.055 MM	0.050 MM	3.0 MM		
45_OHM_SE	*	N	0.055 MM	0.050 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL1,ISL12	Y	0.088 MM	0.050 MM	3.0 MM		
50_OHM_SE	ISL3	Y	0.050 MM	0.050 MM	3.0 MM		
50_OHM_SE	ISL5,ISL8	Y	0.062 MM	0.050 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES
90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM		0.110 MM	0.110 MM
90_OHM_DIFF	ISL3	Y	0.051 MM	0.051 MM	=STANDARD	0.120 MM	0.120 MM
90_OHM_DIFF	ISL5,ISL8	Y	0.072 MM	0.075 MM	=STANDARD	0.120 MM	0.120 MM

MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM
LED	*	Y	0.2 MM	0.10MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.100 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.057 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.086 MM	?
2:1_SPACING	*	0.114 MM	?
2.5:1_SPACING	*	0.143 MM	?
3:1_SPACING	*	0.171 MM	?
4:1_SPACING	*	0.228 MM	?
5:1_SPACING	*	0.285 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP,BOTTOM	0.2 MM	1000

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

POWER

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PWR	*	Y	0.6MM	0.25 MM	10.0 MM		
GND_PH	*	Y	0.6MM	0.075 MM	10.0 MM		

MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING
LED	*	*	3:1_SPACING

Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I63	CLK_50S	CLK	CLK_32K_PMU	18 37
I162	CLK_50S	CLK	CLK_32K_WLAN	15 37
I81	CLK_50S	CLK	CLK_32K_GPS	
I88	CLK_50S	CLK	CLK_CAM_FF	7 25
I89	CLK_50S	CLK	CLK_CAM_FF_FILT	25
I95	SE_50S	0P2MM_SPACING	CLK_CAM_FF_CONN	24 25
I96	CLK_50S	CLK	CLK_CAM_RF	7 25
I94	CLK_50S	CLK	CLK_CAM_RF_FILT	25
I225	CLK_50S	CLK	CLK_CAM_RF_CONN	24 25
I135	CLK_50S	CLK	I2S0_ASP_MCK	5
I133	CLK_50S	CLK	I2S0_ASP_MCK_R	5 19
I157	CLK_50S	CLK	CLK_CAM_FF_R	7
I158	CLK_50S	CLK	CLK_CAM_RF_R	7
I235	CLK_50S	CLK	CLK_CAM_FF_C	25
I235	CLK_50S	CLK	CLK_CAM_RF_C	25

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	3:1_SPACING
UART	UART	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I231	UART_50S	UART	UART0_AP_RXD	5 15
I230	UART_50S	UART	UART0_AP_TXD	5 15
I174	UART_50S	UART	UART0_MUX_RXD	11 15
I175	UART_50S	UART	UART0_MUX_TXD	11 15
I176	UART_50S	UART	UART1_BB_CTS_L	5 30
I178	UART_50S	UART	UART1_BB_RTS_L	5 30
I177	UART_50S	UART	UART1_BB_TXD	5 30
I179	UART_50S	UART	UART1_BB_RXD	5 30
I170	UART_50S	UART	UART3_BT_CTS_L	5 15
I167	UART_50S	UART	UART3_BT_RTS_L	5 15
I171	UART_50S	UART	UART3_BT_RXD	5 15
I169	UART_50S	UART	UART3_BT_TXD	5 15
I232	UART_50S	UART	UART6_WLAN_RXD	5 15
I233	UART_50S	UART	UART6_WLAN_TXD	5 15

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I183	SPI_50S	SPI	SPI1_GRAPE_MISO	5 17
I184	SPI_50S	SPI	SPI1_GRAPE_MOSI	5 17
I185	SPI_50S	SPI	SPI1_GRAPE_SCLK	5 17
I186	SPI_50S	SPI	SPI1_GRAPE_CS_L	5 17
I187	SPI_50S	SPI	SPI2_IPC_MISO	5 30
I188	SPI_50S	SPI	SPI2_IPC_MOSI	5 30
I189	SPI_50S	SPI	SPI2_IPC_SCLK	5 30
I190	SPI_50S	SPI	SPI2_IPC_SRDY	5 30

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I152		DWI	DWI_AP_CLK	5 37
I153		DWI	DWI_AP_DI	5 37
I154		DWI	DWI_AP_DO	5 37

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I16		JTAG	JTAG_AP_TCK	4 27
I15		JTAG	JTAG_AP_TMS	4 27
I14		JTAG	JTAG_AP_TDI	4 10
I13		JTAG	JTAG_AP_TDO	4 10
I20		RST	JTAG_AP_TRST_L	4 10 45

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I1	I2C_50S	I2C	I2C1_SDA_1V8	5 10 25
I2	I2C_50S	I2C	I2C1_SCL_1V8	5 10 25
I3	I2C_50S	I2C	I2C0_SDA_1V8	5 10 19 22 37
I4	I2C_50S	I2C	I2C0_SCL_1V8	5 10 19 22 37
I61	I2C_50S	I2C	I2C2_SDA_3V0	5 25
I62	I2C_50S	I2C	I2C2_SCL_3V0	5 25
I98	I2C_50S	I2C	ISP_AP_0_SCL	7 25
I99	I2C_50S	I2C	ISP_AP_0_SDA	7 25
I100	I2C_50S	I2C	ISP_AP_1_SCL	7 25
I101	I2C_50S	I2C	ISP_AP_1_SDA	7 25
I102	I2C_50S	I2C	I2C2_SCL_3V0_ALS	10 24 25
I103	I2C_50S	I2C	I2C2_SDA_3V0_ALS	10 24 25
I220	I2C_50S	I2C	I2C1_SCL_1V8_CONN	24 25
I221	I2C_50S	I2C	I2C1_SDA_1V8_CONN	24 25
I123	I2C_50S	I2C	ISP_CAM_1_SCL	24 25
I125	I2C_50S	I2C	ISP_CAM_1_SDA	24 25
I220	I2C_50S	I2C	ISP_CAM_0_SCL	24 25
I224	I2C_50S	I2C	ISP_CAM_0_SDA	24 25

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I92		CRYSTAL	XTAL_24M_I	4
I90		CRYSTAL	XTAL_24M_O	4
I93		CRYSTAL	24M_O	4
I230		CRYSTAL	PMU_XTAL	36
I231		CRYSTAL	PMU_EXTAL	36

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I140	I2S_50S	I2S	I2S0_ASP_BCLK	5 19
I145	I2S_50S	I2S	I2S0_ASP_LRCK	5 19
I142	I2S_50S	I2S	I2S0_ASP_DIN	5 19
I141	I2S_50S	I2S	I2S0_ASP_DOUT	5 19
I159	I2S_50S	I2S	I2S_L63_ASP_SDOUT	19
I146	I2S_50S	I2S	I2S2_VSP_BCLK	5 15 19
I148	I2S_50S	I2S	I2S2_VSP_LRCK	5 15 19
I147	I2S_50S	I2S	I2S2_VSP_DIN	5 15 19
I156	I2S_50S	I2S	I2S2_VSP_DOUT	5 15 19
I160	I2S_50S	I2S	I2S_L63_VSP_SDOUT	19
I143	I2S_50S	I2S	I2S3_XSP_BCLK	5 19
I144	I2S_50S	I2S	I2S3_XSP_LRCK	5 19
I136	I2S_50S	I2S	I2S3_XSP_DIN	5 19
I155	I2S_50S	I2S	I2S3_XSP_DOUT	5 19
I161	I2S_50S	I2S	I2S_L63_XSP_SDOUT	19

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I5	USB_90D	USB	USB_DK_D0_P	4 27
I6	USB_90D	USB	USB_DK_D0_N	4 27
I7	USB_90D	USB	USB_DK_CON_D0_P	
I8	USB_90D	USB	USB_DK_CON_D0_N	
I82	USB_90D	USB	USB_BB_D_P	11 30
I83	USB_90D	USB	USB_BB_D_N	11 30
I84	USB_90D	USB	USB11_MUX_D0_P	4 11
I85	USB_90D	USB	USB11_MUX_D0_N	4 11
I129	USB_90D	USB	USB11_ACC_TX_N	11 27
I127	USB_90D	USB	USB11_ACC_RX_P	11 27
I171	USB_90D	USB	ACC_PT_DK_CON_TX	27 29
I172	USB_90D	USB	ACC_PT_DK_CON_RX	27 29
I208	USB_90D	USB	EXTRA_USB_D1_N	
I206	USB_90D	USB	EXTRA_USB_D1_P	
I205	USB_90D	USB	NC_USB11_D1_N	4 46
I207	USB_90D	USB	NC_USB11_D1_P	4 46
I208	USB_90D	USB	NC_USB_D1_N	4 46
I209	USB_90D	USB	NC_USB_D1_P	4 46
I210	USB_90D	USB	TP_WLAN_USB_DN	
I211	USB_90D	USB	TP_WLAN_USB_DP	
I212	USB_90D	USB	USB_GPIO_DM	
I214	USB_90D	USB	USB_GPIO_DM_CONN	
I213	USB_90D	USB	USB_GPIO_DP	
I215	USB_90D	USB	USB_GPIO_DP_CONN	
I216	USB_90D	USB	USB_PT_DK_CON_D_N	27 29
I217	USB_90D	USB	USB_PT_DK_CON_D_P	27 29
I218	USB_90D	USB	USB_UART_DM	
I219	USB_90D	USB	USB_UART_DM_CONN	
I222	USB_90D	USB	USB_UART_DP	
I221	USB_90D	USB	USB_UART_DP_CONN	
I223	USB_90D	USB	EXTRA_USB11_D1_N	
I224	USB_90D	USB	EXTRA_USB11_D1_P	

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I191	HSIC	HSIC_BB	HSIC0_BB_DATA1	4 30
I192	HSIC	HSIC_BB	HSIC0_BB_STB1	4 30
I193	HSIC	HSIC_WLAN	HSIC1_WLAN_DATA1	4 15 40
I192	HSIC	HSIC_WLAN	HSIC1_WLAN_STB1	4 15 40
I195	HSIC	HSIC	HSIC_BB_RDY	5 30
I196	HSIC	HSIC	HSIC_HOST_RDY	5 30
I197	HSIC	HSIC	HSIC_HOST_READY_WL	5
I198	HSIC	HSIC	HSIC_HOST_READY_WLAN	5 15
I199	HSIC	HSIC	HSIC_WLAN_RDY	5 15
I200	HSIC	HSIC	NC_HSIC0_DATA2	4 46
I201	HSIC	HSIC	NC_HSIC0_STB2	4 46
I202	HSIC	HSIC	NC_HSIC1_DATA2	4 46
I203	HSIC	HSIC	NC_HSIC1_STB2	4 46

ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P213	VID_50S	ANALOG_VIDEO	DAC_AP_OUT1 7 11
P214	VID_50S	ANALOG_VIDEO	DAC_AP_OUT2 7 11
P215	VID_50S	ANALOG_VIDEO	DAC_AP_OUT3 7 11
P232	VID_50S	ANALOG_VIDEO	BUF_C_Y 11
P233	VID_50S	ANALOG_VIDEO	BUF_CVBS_PB 11
P231	VID_50S	ANALOG_VIDEO	BUF_Y_PR 11
P219	VID_50S	ANALOG_VIDEO	VIDEO_EMI_CVBS_PB 10 11 27
P220	VID_50S	ANALOG_VIDEO	VIDEO_EMI_C_Y 10 11 27
P221	VID_50S	ANALOG_VIDEO	VIDEO_EMI_Y_PR 10 11 27
P222	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_CVBS_PB 27 28
P224	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_C_Y 27 28
P223	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_Y_PR 27 28
P526	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_CVBS_PB_R 28 29
P527	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_C_Y_R 28 29
P528	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_Y_PR_R 28 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P335	MIPI_90D	MIPI0C	MIPI0C_AP_CLK_P 7 25
P336	MIPI_90D	MIPI0C	MIPI0C_AP_CLK_N 7 25
P338	MIPI_90D	MIPI0C	MIPI0C_CAM_CLK_P 24 25
P339	MIPI_90D	MIPI0C	MIPI0C_CAM_CLK_N 24 25
P331	MIPI_90D	MIPI0C	MIPI0C_AP_DATA_P<0> 7 25
P330	MIPI_90D	MIPI0C	MIPI0C_AP_DATA_N<0> 7 25
P332	MIPI_90D	MIPI0C	MIPI0C_AP_DATA_N<1> 7 25
P333	MIPI_90D	MIPI0C	NC_MIPI0C_AP_DATA_N<2> 7 46
P334	MIPI_90D	MIPI0C	NC_MIPI0C_AP_DATA_N<3> 7 46
P327	MIPI_90D	MIPI0C	MIPI0C_AP_DATA_P<1> 7 25
P326	MIPI_90D	MIPI0C	NC_MIPI0C_AP_DATA_P<2> 7 46
P325	MIPI_90D	MIPI0C	NC_MIPI0C_AP_DATA_P<3> 7 46
P516	CAM_100DVA3	CAM	MIPI0C_CAM_DATA_N<0> 24 25
P518	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_N<1> 24 25
P521	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_N<2>
P520	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_N<3>
P517	CAM_100DVA3	CAM	MIPI0C_CAM_DATA_P<0> 24 25
P522	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_P<1> 24 25
P523	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_P<2>
P524	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_P<3>
P340	MIPI_90D	MIPI0C	MIPI0C_CAM_CLK_DEBUG_N
P341	MIPI_90D	MIPI0C	MIPI0C_CAM_CLK_DEBUG_P
P342	MIPI_90D	MIPI0C	MIPI0C_CAM_D0_DEBUG_N
P343	MIPI_90D	MIPI0C	MIPI0C_CAM_D0_DEBUG_P
P344	MIPI_90D	MIPI0C	MIPI0C_CAM_D1_DEBUG_N
P345	MIPI_90D	MIPI0C	MIPI0C_CAM_D1_DEBUG_P
P346	MIPI_90D	MIPI0C	MIPI0C_CAM_D2_DEBUG_N
P347	MIPI_90D	MIPI0C	MIPI0C_CAM_D2_DEBUG_P
P348	MIPI_90D	MIPI0C	MIPI0C_CAM_D3_DEBUG_N
P349	MIPI_90D	MIPI0C	MIPI0C_CAM_D3_DEBUG_P
P354	MIPI_90D	MIPI1C	MIPI1C_AP_DATA_P<0> 7 25
P356	MIPI_90D	MIPI1C	MIPI1C_AP_DATA_N<0> 7 25
P535	MIPI_90D	MIPI1C	NC_MIPI1C_AP_DATA_P<1> 7 46
P534	MIPI_90D	MIPI1C	NC_MIPI1C_AP_DATA_N<1> 7 46
P357	MIPI_90D	MIPI1C	MIPI1C_AP_CLK_P 7 25
P358	MIPI_90D	MIPI1C	MIPI1C_AP_CLK_N 7 25
P355	CAM_100DVGA	CAM	MIPI1C_CAM_DATA_P<0> 24 25
P353	CAM_100DVGA	CAM	MIPI1C_CAM_DATA_N<0> 24 25
P360	MIPI_90D	MIPI1C	MIPI1C_CAM_CLK_P 24 25
P359	MIPI_90D	MIPI1C	MIPI1C_CAM_CLK_N 24 25
P410	MIPI_90D	MIPI1C	MIPI1C_CAM_CLK_DEBUG_N
P411	MIPI_90D	MIPI1C	MIPI1C_CAM_CLK_DEBUG_P
P412	MIPI_90D	MIPI1C	MIPI1C_CAM_D0_DEBUG_N
P413	MIPI_90D	MIPI1C	MIPI1C_CAM_D0_DEBUG_P

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_90D	*	90_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P410	DP_90D	DP	DP_AP_AUX_N 7 28
P411	DP_90D	DP	DP_AP_AUX_P 7 28
P418	DP_50S	DP	DP_AP_HPD 7 37
P419	DP_90D	DP	DP_AP_TX_N<0> 7 28
P420	DP_90D	DP	DP_AP_TX_N<1> 7 28
P422	DP_90D	DP	DP_AP_TX_P<0> 7 28
P421	DP_90D	DP	DP_AP_TX_P<1> 7 28
P423	DP_90D	DP	DP_EMI_AUX_N 27 28 43
P424	DP_90D	DP	DP_EMI_AUX_P 27 28 43
P425	DP_90D	DP	DP_EMI_TX_N<0> 27 28
P427	DP_90D	DP	DP_EMI_TX_N<1> 27 28
P426	DP_90D	DP	DP_EMI_TX_P<0> 27 28
P428	DP_90D	DP	DP_EMI_TX_P<1> 27 28
P429	DP_90D	DP	DP_PT_DK_CON_AUX_N 27 29 43
P430	DP_90D	DP	DP_PT_DK_CON_AUX_P 27 29 43
P431	DP_90D	DP	DP_PT_DK_CON_TX_N<0> 27 29
P432	DP_90D	DP	DP_PT_DK_CON_TX_N<1> 27 29
P433	DP_90D	DP	DP_PT_DK_CON_TX_P<0> 27 29
P434	DP_90D	DP	DP_PT_DK_CON_TX_P<1> 27 29
P466	DP_90D	DP	DP_AP_TX_N<2> 7 28
P467	DP_90D	DP	DP_AP_TX_N<3> 7 28
P469	DP_90D	DP	DP_AP_TX_P<2> 7 28
P468	DP_90D	DP	DP_AP_TX_P<3> 7 28
P470	DP_90D	DP	DP_EMI_AUX_N 27 28 43
P471	DP_90D	DP	DP_EMI_AUX_P 27 28 43
P472	DP_90D	DP	DP_EMI_TX_N<2>
P473	DP_90D	DP	DP_EMI_TX_N<3>
P474	DP_90D	DP	DP_EMI_TX_P<2>
P475	DP_90D	DP	DP_EMI_TX_P<3>
P476	DP_90D	DP	DP_PT_DK_CON_AUX_N 27 29 43
P477	DP_90D	DP	DP_PT_DK_CON_AUX_P 27 29 43
P478	DP_90D	DP	DP_PT_DK_CON_TX_N<2> 28
P479	DP_90D	DP	DP_PT_DK_CON_TX_N<3> 28
P480	DP_90D	DP	DP_PT_DK_CON_TX_P<2> 28
P481	DP_90D	DP	DP_PT_DK_CON_TX_P<3> 28

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LED	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P482	LED	LEDA	LED_IO1_A_R 37
P484	LED	LEDB	LED_IO1_B_R 37
P483	LED	LEDA	LED_IO2_A_R 37
P485	LED	LEDB	LED_IO2_B_R 37
P487	LED	LEDA	LED_IO3_A_R 37
P486	LED	LEDB	LED_IO3_B_R 37
P489	LED	LEDA	LED_IO4_A_R 37
P488	LED	LEDB	LED_IO4_B_R 37
P490	LED	LEDA	LED_IO5_A_R 37
P491	LED	LEDB	LED_IO5_B_R 37
P492	LED	LEDA	LED_IO6_A_R 37
P493	LED	LEDB	LED_IO6_B_R 37
P494	LED	LEDA	LED_IO_1_A 16 37
P495	LED	LEDB	LED_IO_1_B 16 37
P496	LED	LEDA	LED_IO_2_A 16 37
P497	LED	LEDB	LED_IO_2_B 16 37
P498	LED	LEDA	LED_IO_3_A 16 37
P499	LED	LEDB	LED_IO_3_B 16 37
P500	LED	LEDA	LED_IO_4_A 16 37
P501	LED	LEDB	LED_IO_4_B 16 37
P502	LED	LEDA	LED_IO_5_A 16 37
P503	LED	LEDB	LED_IO_5_B 16 37
P504	LED	LEDA	LED_IO_6_A 16 37
P505	LED	LEDB	LED_IO_6_B 16 37

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P435	EDP_90D	EDP	EDP_AP_AUX_N 7 16
P436	EDP_90D	EDP	EDP_AP_AUX_P 7 16
P437	EDP_50S	EDP	EDP_AP_HPD 7 16
P439	EDP_90D	EDP	EDP_AP_TX_N<0> 7 16
P438	EDP_90D	EDP	EDP_AP_TX_N<1> 7 16
P440	EDP_90D	EDP	EDP_AP_TX_N<2> 7 16
P442	EDP_90D	EDP	EDP_AP_TX_N<3> 7 16
P443	EDP_90D	EDP	EDP_AP_TX_P<0> 7 16
P444	EDP_90D	EDP	EDP_AP_TX_P<1> 7 16
P441	EDP_90D	EDP	EDP_AP_TX_P<2> 7 16
P445	EDP_90D	EDP	EDP_AP_TX_P<3> 7 16
P447	EDP_90D	EDP	EDP_AUX_CONN_N 16
P446	EDP_90D	EDP	EDP_AUX_CONN_P 16
P449	EDP_90D	EDP	EDP_DATA_CONN_N<0> 16
P448	EDP_90D	EDP	EDP_DATA_CONN_N<1> 16
P450	EDP_90D	EDP	EDP_DATA_CONN_N<2> 16
P451	EDP_90D	EDP	EDP_DATA_CONN_N<3> 16
P452	EDP_90D	EDP	EDP_DATA_CONN_P<0> 16
P454	EDP_90D	EDP	EDP_DATA_CONN_P<1> 16
P453	EDP_90D	EDP	EDP_DATA_CONN_P<2> 16
P455	EDP_90D	EDP	EDP_DATA_CONN_P<3> 16
P457	EDP_90D	EDP	EDP_EMI_AUX_N 16
P456	EDP_90D	EDP	EDP_EMI_AUX_P 16
P458	EDP_90D	EDP	EDP_EMI_TX_N<0> 16
P460	EDP_90D	EDP	EDP_EMI_TX_N<1> 16
P459	EDP_90D	EDP	EDP_EMI_TX_N<2> 16
P462	EDP_90D	EDP	EDP_EMI_TX_N<3> 16
P461	EDP_90D	EDP	EDP_EMI_TX_P<0> 16
P463	EDP_90D	EDP	EDP_EMI_TX_P<1> 16
P464	EDP_90D	EDP	EDP_EMI_TX_P<2> 16
P465	EDP_90D	EDP	EDP_EMI_TX_P<3> 16

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P509	AUDIO	AUDIO	LEFT_CH_OUT_P 19 20
P507	AUDIO	AUDIO	LEFT_CH_OUT_REF 19 20
P508	AUDIO	AUDIO	LEFT_CH_P 20
P511	AUDIO	AUDIO	MAX983X4_L_IN_N 20
P510	AUDIO	AUDIO	MAX983X4_L_IN_P 20
P531	AUDIO	AUDIO	SPKRAMP_L_OUT_N 20
P530	AUDIO	AUDIO	SPKRAMP_L_OUT_P 20
P513	AUDIO	AUDIO	RIGHT_CH_OUT_REF 19 20
P514	AUDIO	AUDIO	RIGHT_CH_OUT_P 19 20
P529	AUDIO	AUDIO	RIGHT_CH_P 20
P515	AUDIO	AUDIO	MAX983X4_R_IN_P 20
P519	AUDIO	AUDIO	MAX983X4_R_IN_N 20
P532	AUDIO	AUDIO	SPKRAMP_R_OUT_N 20
P533	AUDIO	AUDIO	SPKRAMP_R_OUT_P 20
P536	AUDIO	AUDIO	EXT_MIC_P 19 22
P537	AUDIO	AUDIO	EXT_MIC_REF 19 22
P538	AUDIO	AUDIO	HSMIC_C_P 19 22
P539	AUDIO	AUDIO	HSMIC_C_N 19 22
P540	AUDIO	AUDIO	HSMIC_R_P 22
P541	AUDIO	AUDIO	HSMIC_R_N 22
P542	AUDIO	AUDIO	AUD_HP1_MLBCON_R 21 23
P543	AUDIO	AUDIO	AUD_HP1_MLBCON_L 21 23
P544	AUDIO	AUDIO	CONN_AUD_HEADSET_RIGHT 23 24
P546	AUDIO	AUDIO	CONN_AUD_HEADSET_LEFT 23 24
P547	AUDIO	AUDIO	HP_R 19 21
P548	AUDIO	AUDIO	HP_L 19 21

DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	90_OHM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1223	DDR_50S	DDR	DDR0_CA<9..0>	8 13
1222	DDR_50S	DDR	DDR0_DM<3..0>	8 13
1222	DDR_90D	DDR	DDR0_CK_P	8 13
1222	DDR_90D	DDR	DDR0_CK_N	8 13
1222	DDR_50S	DDR	DDR0_CKE<1..0>	8 13
1224	DDR_50S	DDR	DDR0_CSN<2..0>	8 13
1223	DDR_50S	DDR	DDR0_ZQ	13
1231	DDR_50S	DDR0	DDR0_DQ<7..0>	8 13 40
1225	DDR_50S	DDR0	DDR0_DQS_P<0>	8 13 40
1233	DDR_50S	DDR0	DDR0_DQS_N<0>	8 13 40
1232	DDR_50S	DDR1	DDR0_DQ<15..8>	8 13 40
1237	DDR_50S	DDR1	DDR0_DQS_P<1>	8 13
1235	DDR_50S	DDR1	DDR0_DQS_N<1>	8 13 40
1234	DDR_50S	DDR2	DDR0_DQ<23..16>	8 13
1230	DDR_50S	DDR2	DDR0_DQS_P<2>	8 13
1237	DDR_50S	DDR2	DDR0_DQS_N<2>	8 13
1238	DDR_50S	DDR3	DDR0_DQ<31..24>	8 13
1239	DDR_50S	DDR3	DDR0_DQS_P<3>	8 13
1240	DDR_50S	DDR3	DDR0_DQS_N<3>	8 13
1201	DDR_50S	DDR	DDR1_CA<9..0>	8 13
1207	DDR_50S	DDR	DDR1_DM<3..0>	8 13
1201	DDR_90D	DDR	DDR1_CK_P	8 13
1205	DDR_90D	DDR	DDR1_CK_N	8 13
1205	DDR_50S	DDR	DDR1_CKE<1..0>	8 13
1205	DDR_50S	DDR	DDR1_CSN<2..0>	8 13
1205	DDR_50S	DDR	DDR1_ZQ	13
1210	DDR_50S	DDR0	DDR1_DQ<7..0>	8 13
1208	DDR_50S	DDR0	DDR1_DQS_P<0>	8 13
1211	DDR_50S	DDR0	DDR1_DQS_N<0>	8 13
1219	DDR_50S	DDR1	DDR1_DQ<15..8>	8 13
1213	DDR_50S	DDR1	DDR1_DQS_P<1>	8 13
1216	DDR_50S	DDR1	DDR1_DQS_N<1>	8 13
1214	DDR_50S	DDR2	DDR1_DQ<23..16>	8 13
1215	DDR_50S	DDR2	DDR1_DQS_P<2>	8 13
1217	DDR_50S	DDR2	DDR1_DQS_N<2>	8 13
1218	DDR_50S	DDR3	DDR1_DQ<31..24>	8 13
1215	DDR_50S	DDR3	DDR1_DQS_P<3>	8 13
1220	DDR_50S	DDR3	DDR1_DQS_N<3>	8 13
1183	DDR_50S	DDR	DDR2_CA<9..0>	8 14
1187	DDR_50S	DDR	DDR2_DM<3..0>	8 14
1183	DDR_90D	DDR	DDR2_CK_P	8 14
1183	DDR_90D	DDR	DDR2_CK_N	8 14
1188	DDR_50S	DDR	DDR2_CKE<1..0>	8 14
1184	DDR_50S	DDR	DDR2_CSN<2..0>	8 14
1188	DDR_50S	DDR	DDR2_ZQ	14
1190	DDR_50S	DDR0	DDR2_DQ<7..0>	8 14
1188	DDR_50S	DDR0	DDR2_DQS_P<0>	8 14
1191	DDR_50S	DDR0	DDR2_DQS_N<0>	8 14
1192	DDR_50S	DDR1	DDR2_DQ<15..8>	8 14
1193	DDR_50S	DDR1	DDR2_DQS_P<1>	8 14
1195	DDR_50S	DDR1	DDR2_DQS_N<1>	8 14
1194	DDR_50S	DDR2	DDR2_DQ<23..16>	8 14
1196	DDR_50S	DDR2	DDR2_DQS_P<2>	8 14
1197	DDR_50S	DDR2	DDR2_DQS_N<2>	8 14
1198	DDR_50S	DDR3	DDR2_DQ<31..24>	8 14
1199	DDR_50S	DDR3	DDR2_DQS_P<3>	8 14
1200	DDR_50S	DDR3	DDR2_DQS_N<3>	8 14
138	DDR_50S	DDR	DDR3_CA<9..0>	8 14
142	DDR_50S	DDR	DDR3_DM<3..0>	8 14
141	DDR_90D	DDR	DDR3_CK_P	8 14
144	DDR_90D	DDR	DDR3_CK_N	8 14
142	DDR_50S	DDR	DDR3_CKE<1..0>	8 14
147	DDR_50S	DDR	DDR3_CSN<2..0>	8 14
148	DDR_50S	DDR	DDR3_ZQ	14
137	DDR_50S	DDR0	DDR3_DQ<7..0>	8 14
1170	DDR_50S	DDR0	DDR3_DQS_P<0>	8 14
1171	DDR_50S	DDR0	DDR3_DQS_N<0>	8 14
1172	DDR_50S	DDR1	DDR3_DQ<15..8>	8 14
1173	DDR_50S	DDR1	DDR3_DQS_P<1>	8 14
1174	DDR_50S	DDR1	DDR3_DQS_N<1>	8 14
1172	DDR_50S	DDR2	DDR3_DQ<23..16>	8 14
1176	DDR_50S	DDR2	DDR3_DQS_P<2>	8 14
1177	DDR_50S	DDR2	DDR3_DQS_N<2>	8 14
1178	DDR_50S	DDR3	DDR3_DQ<31..24>	8 14
1179	DDR_50S	DDR3	DDR3_DQS_P<3>	8 14
1180	DDR_50S	DDR3	DDR3_DQS_N<3>	8 14

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
168	NAND_50S	NAND0	FMI0_AD<0>	6 12
169	NAND_50S	NAND0	FMI0_AD<1>	6 12
170	NAND_50S	NAND0	FMI0_AD<2>	6 12
171	NAND_50S	NAND0	FMI0_AD<3>	6 12
172	NAND_50S	NAND0	FMI0_AD<4>	6 12
173	NAND_50S	NAND0	FMI0_AD<5>	6 12
174	NAND_50S	NAND0	FMI0_AD<6>	6 12
175	NAND_50S	NAND0	FMI0_AD<7>	6 12
176	NAND_50S	NAND0	FMI0_ALE	6 12
177	NAND_50S	NAND0	FMI0_CE0_L	6 12
178	NAND_50S	NAND0	FMI0_CE1_L	6 12
1120	NAND_50S	NAND0	FMI0_CE2_L	
112	NAND_50S	NAND0	FMI0_CE3_L	
1122	NAND_50S	NAND0	FMI0_CE4_L	
112	NAND_50S	NAND0	FMI0_CE5_L	
1124	NAND_50S	NAND0	FMI0_CE6_L	
1125	NAND_50S	NAND0	FMI0_CE7_L	
1126	NAND_50S	NAND0	FMI0_CLE	6 12
1127	NAND_50S	NAND0	FMI0_DQS_N	
1128	NAND_50S	NAND0	FMI0_DQS_P	6 12
1129	NAND_50S	NAND0	FMI0_RB0_L	
1130	NAND_50S	NAND0	FMI0_RB1_L	
1131	NAND_50S	NAND0	FMI0_RE_N	6 12
1132	NAND_50S	NAND0	FMI0_RE_P	
1133	NAND_50S	NAND0	FMI0_WE_L	6 12
1134	NAND_50S	NAND0	FMI0_WP_L	
1135	NAND_50S	NAND1	FMI1_AD<0>	6 12
1136	NAND_50S	NAND1	FMI1_AD<1>	6 12
113	NAND_50S	NAND1	FMI1_AD<2>	6 12
1138	NAND_50S	NAND1	FMI1_AD<3>	6 12
1139	NAND_50S	NAND1	FMI1_AD<4>	6 12
1140	NAND_50S	NAND1	FMI1_AD<5>	6 12
1143	NAND_50S	NAND1	FMI1_AD<6>	6 12
1145	NAND_50S	NAND1	FMI1_AD<7>	6 12
1144	NAND_50S	NAND1	FMI1_ALE	6 12 44
1146	NAND_50S	NAND1	FMI1_CE0_L	6 12
1147	NAND_50S	NAND1	FMI1_CE1_L	6 12
1148	NAND_50S	NAND1	FMI1_CE2_L	
1149	NAND_50S	NAND1	FMI1_CE3_L	
1150	NAND_50S	NAND1	FMI1_CE4_L	
1151	NAND_50S	NAND1	FMI1_CE5_L	
1152	NAND_50S	NAND1	FMI1_CE6_L	
1153	NAND_50S	NAND1	FMI1_CE7_L	
1155	NAND_50S	NAND1	FMI1_CLE	6 12 44
1154	NAND_50S	NAND1	FMI1_DQS_N	
1156	NAND_50S	NAND1	FMI1_DQS_P	6 12
1158	NAND_50S	NAND1	FMI1_RB0_L	
1157	NAND_50S	NAND1	FMI1_RB1_L	
1159	NAND_50S	NAND1	FMI1_RE_N	6 12
1159	NAND_50S	NAND1	FMI1_RE_P	
1160	NAND_50S	NAND1	FMI1_WE_L	6 12 44
1159	NAND_50S	NAND1	FMI1_WP_L	44
1161	NAND_50S	NAND1	FMI1_CLE	6 12 44
1162	NAND_50S	NAND1	FMI1_ALE	6 12 44
1163	NAND_50S	NAND1	FMI1_RE_L	
1164	NAND_50S	NAND1	FMI1_WE_L	6 12 44
1165	NAND_50S	NAND1	FMI1_WP_L	44

NAND DEV

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
149	NAND_50S	NAND0	SLOT0_FMI0_AD<0>
150	NAND_50S	NAND0	SLOT0_FMI0_AD<1>
151	NAND_50S	NAND0	SLOT0_FMI0_AD<2>
152	NAND_50S	NAND0	SLOT0_FMI0_AD<3>
153	NAND_50S	NAND0	SLOT0_FMI0_AD<4>
154	NAND_50S	NAND0	SLOT0_FMI0_AD<5>
155	NAND_50S	NAND0	SLOT0_FMI0_AD<6>
156	NAND_50S	NAND0	SLOT0_FMI0_AD<7>
157	NAND_50S	NAND0	SLOT0_FMI0_ALE
158	NAND_50S	NAND0	SLOT0_FMI0_CE0_L
159	NAND_50S	NAND0	SLOT0_FMI0_CE1_L
160	NAND_50S	NAND0	SLOT0_FMI0_CLE
162	NAND_50S	NAND0	SLOT0_FMI0_DQS_P
161	NAND_50S	NAND0	SLOT0_FMI0_RE_N
163	NAND_50S	NAND0	SLOT0_FMI0_WE_L
164	NAND_50S	NAND1	SLOT0_FMI1_AD<0>
165	NAND_50S	NAND1	SLOT0_FMI1_AD<1>
167	NAND_50S	NAND1	SLOT0_FMI1_AD<2>
166	NAND_50S	NAND1	SLOT0_FMI1_AD<3>
179	NAND_50S	NAND1	SLOT0_FMI1_AD<4>
180	NAND_50S	NAND1	SLOT0_FMI1_AD<5>
181	NAND_50S	NAND1	SLOT0_FMI1_AD<6>
183	NAND_50S	NAND1	SLOT0_FMI1_AD<7>
182	NAND_50S	NAND1	SLOT0_FMI1_ALE
184	NAND_50S	NAND1	SLOT0_FMI1_CE0_L
185	NAND_50S	NAND1	SLOT0_FMI1_CE1_L
186	NAND_50S	NAND1	SLOT0_FMI1_CLE
187	NAND_50S	NAND1	SLOT0_FMI1_DQS_P
188	NAND_50S	NAND1	SLOT0_FMI1_RE_N
189	NAND_50S	NAND1	SLOT0_FMI1_WE_L
190	NAND_50S	NAND0	SLOT1_FMI0_AD<0>
191	NAND_50S	NAND0	SLOT1_FMI0_AD<1>
193	NAND_50S	NAND0	SLOT1_FMI0_AD<2>
192	NAND_50S	NAND0	SLOT1_FMI0_AD<3>
194	NAND_50S	NAND0	SLOT1_FMI0_AD<4>
195	NAND_50S	NAND0	SLOT1_FMI0_AD<5>
196	NAND_50S	NAND0	SLOT1_FMI0_AD<6>
197	NAND_50S	NAND0	SLOT1_FMI0_AD<7>
198	NAND_50S	NAND0	SLOT1_FMI0_ALE
199	NAND_50S	NAND0	SLOT1_FMI0_CE0_L
1100	NAND_50S	NAND0	SLOT1_FMI0_CE1_L
1101	NAND_50S	NAND0	SLOT1_FMI0_CLE
1102	NAND_50S	NAND0	SLOT1_FMI0_DQS_P
1104	NAND_50S	NAND0	SLOT1_FMI0_RE_N
1103	NAND_50S	NAND0	SLOT1_FMI0_WE_L
1105	NAND_50S	NAND1	SLOT1_FMI1_AD<0>
1106	NAND_50S	NAND1	SLOT1_FMI1_AD<1>
1107	NAND_50S	NAND1	SLOT1_FMI1_AD<2>
1108	NAND_50S	NAND1	SLOT1_FMI1_AD<3>
1109	NAND_50S	NAND1	SLOT1_FMI1_AD<4>
1110	NAND_50S	NAND1	SLOT1_FMI1_AD<5>
111	NAND_50S	NAND1	SLOT1_FMI1_AD<6>
1112	NAND_50S	NAND1	SLOT1_FMI1_AD<7>
1113	NAND_50S	NAND1	SLOT1_FMI1_ALE
1114	NAND_50S	NAND1	SLOT1_FMI1_CE0_L
1115	NAND_50S	NAND1	SLOT1_FMI1_CE1_L
1116	NAND_50S	NAND1	SLOT1_FMI1_CLE
1117	NAND_50S	NAND1	SLOT1_FMI1_DQS_P
1118	NAND_50S	NAND1	SLOT1_FMI1_RE_N
1119	NAND_50S	NAND1	SLOT1_FMI1_WE_L

DDR VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1166		PWR	PPVREF_DDR0_CA	13 45
1167		PWR	PPVREF_DDR0_DQ	13 45
1168		PWR	PPVREF_DDR1_CA	13 45
1169		PWR	PPVREF_DDR1_DQ	13 45

PWR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PWR	*	PWR_PMU

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PWR	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P224 3.3V	PP_PWR	PWR	ACC_PT_DK_CON_PP3V3 27 29
B1	PP_PWR	PWR	BUCK0_FB 36
B2	PP_PWR	PWR	BUCK0_LXL 36
B3	PP_PWR	PWR	BUCK0_LXM 36
B4	PP_PWR	PWR	BUCK2_FB 36
B5	PP_PWR	PWR	BUCK2_LXL 36
B6	PP_PWR	PWR	BUCK2_LXM 36
B7	PP_PWR	PWR	BUCK2_LXR 36
B8	PP_PWR	PWR	BUCK3_FB 36
B9	PP_PWR	PWR	BUCK3_LXL 36
B12	PP_PWR	PWR	BUCK3_LXM 36
B11	PP_PWR	PWR	BUCK4_FB 36
B10	PP_PWR	PWR	BUCK4_LXL 36
B13	PP_PWR	PWR	BUCK4_LXM 36
B15	PP_PWR	PWR	BUCK5_FB 36
B14	PP_PWR	PWR	BUCK5_LX 36
B16 0.4V	PP_PWR	PWR	PP0V4_MIPI0D 7
B17 0.4V	PP_PWR	PWR	PP0V4_MIPI1D 7
B11 1.1V	PP_PWR	PWR	PP1V1 35 36
B19 1.2V	PP_PWR	PWR	PP1V2 35 36
B20 1.1V	PP_PWR	PWR	PP1V8 35 36
B21 1.1V	PP_PWR	PWR	PP1V1_MIPID_PLL_F 4
B23 1.1V	PP_PWR	PWR	PP1V1_PL0_F 4
B22 1.1V	PP_PWR	PWR	PP1V1_PL1_F 4
B24 1.1V	PP_PWR	PWR	PP1V1_PL2_F 4
B25 1.1V	PP_PWR	PWR	PP1V1_PL3_F 4
B26 1.1V	PP_PWR	PWR	PP1V1_PL4_F 4
B28 1.1V	PP_PWR	PWR	PP1V1_PL5_F 4
B27 1.1V	PP_PWR	PWR	PP1V1_PLL_USB_F 4
B29 1.25V	PP_PWR	PWR	PP1V25_CPU 35 36
B30 1.2V	PP_PWR	PWR	PP1V2_S2R 35 36
B31 1.2V	PP_PWR	PWR	PP1V2_SOC 35 36
B32 1.7V	PP_PWR	PWR	PP1V7_VA_VCP 35 36 40
B33 1.8V	PP_PWR	PWR	PP1V8_ALWAYS 35 36
B34 1.8V	PP_PWR	PWR	PP1V8_DP_AVDD_AUX 7
B35 1.8V	PP_PWR	PWR	PP1V8_EDP_AVDD_AUX 7
B36 1.8V	PP_PWR	PWR	PP1V8_GRAPE 35 36
B37 1.8V	PP_PWR	PWR	PP1V8_S2R 35 36
B38 1.8V	PP_PWR	PWR	PP1V8_SENSOR_FLT 24 26
B39 1.8V	PP_PWR	PWR	PP1V8_VDDA18_TS 5
B40 2.85V	PP_PWR	PWR	PP2V85_CAM 35 36
B41 2.85V	PP_PWR	PWR	PP2V85_CAM_FLT 24 26
B42 3.0V	PP_PWR	PWR	PP3V0_GRAPE 35 36
B43 3.0V	PP_PWR	PWR	PP3V0_IO 35 36
B44 3.0V	PP_PWR	PWR	PP3V0_OPTICAL 35 36
B45 3.0V	PP_PWR	PWR	PP3V0_S2R_HALL 35 36
B46 3.0V	PP_PWR	PWR	PP3V0_S2R_HALL_FLT 24 26
B47 3.0V	PP_PWR	PWR	PP3V0_SENSOR_FLT 10 24 26
B49 3.0V	PP_PWR	PWR	PP3V0_VIDEO 35 36
B51 3.0V	PP_PWR	PWR	PP3V0_VIDEO_BUF 35 36
B50 3.2V	PP_PWR	PWR	PP3V2_LDO5 35 36
B53 3.2V	PP_PWR	PWR	PP3V2_S2R_USBMUX 35 36
B52 3.3V	PP_PWR	PWR	PP3V3_ACC 35 36
B54 3.3V	PP_PWR	PWR	PP3V3_LCDVDD_SW_F 16
B55 3.3V	PP_PWR	PWR	PP3V3_OUT 35 36
B56 3.3V	PP_PWR	PWR	PP3V3_S0_LCD_FERR 16
B57 5.25V	PP_PWR	PWR	PP5V25_VLCM2 35 37
B58 6.0V	PP_PWR	PWR	PP6V0_LCM_HI 37
B59 6.0V	PP_PWR	PWR	PP6V0_LCM_VBOOST 37
B60 4.2V	PWR500	PWR	PPBATT_VCC 35 36 39
B61 1.8V	PP_PWR	PWR	PPIO_NAND_H4 6 9
B62 20.4V	PP_PWR	PWR	PPLED_BACK_REG_A 16
B63 20.4V	PP_PWR	PWR	PPLED_BACK_REG_B 16
B64 20.4V	PP_PWR	PWR	PPLED_OUT_A 35 37
B65 20.4V	PP_PWR	PWR	PPLED_OUT_B 35 37
B66 6.0V	PP_PWR	PWR	PPVBUS_PROT 36
B67 6.0V	PP_PWR	PWR	PPVBUS_USB 4 36
B68 6.0V	PP_PWR	PWR	PPVBUS_USB_DCIN 35 36
B69 5.0V	PP_PWR	PWR	PPVBUS_USB_PT_DK_CON 27 29
B70 1.8V	PP_PWR	PWR	PPVCCO_NAND 12
B71 4.7V	PP_PWR	PWR	PPVCC_MAIN 35 36 37
B72 0.6V	PP_PWR	PWR	PPVREF_DDR0_CA 13 44
B73 0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ 13 44
B74 0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ_H4 8
B76 0.6V	PP_PWR	PWR	PPVREF_DDR1_CA 13 44
B75 0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ 13 44
B77 0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ_H4 8
B78 0.6V	PP_PWR	PWR	PPVREF_DDR2_CA 14
B79 0.6V	PP_PWR	PWR	PPVREF_DDR2_DQ 14
B87 0.6V	PP_PWR	PWR	PPVREF_DDR2_DQ_H4 8
B80 0.6V	PP_PWR	PWR	PPVREF_DDR3_CA 14
B81 0.6V	PP_PWR	PWR	PPVREF_DDR3_DQ 14
B82 0.6V	PP_PWR	PWR	PPVREF_DDR3_DQ_H4 8
P219 4.6V	PP_PWR	PWR	BATT_POS_RC 36
B84 18V	PP_PWR	PWR	PP18V_GRAPE 17
B85 18V	PP_PWR	PWR	PP18V_R_GRAPE 17
P220	PP_PWR	PWR	DAC_AP_VREF 7
P221 3.3V	PP_PWR	PWR	PPVDDI_NAND_U1400 12
P222	PP_PWR	PWR	VR_BOOST_SW 17
P223	PP_PWR	PWR	VR_BOOST_L 17
P226 3.0V	PP_PWR	PWR	MT_3V3_INT 18 45

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P255 3.0V	PP_PWR	PWR	MT_3V3_INT 18 45
P256 1.8V	PP_PWR	PWR	Z1_1V8_OUT 18
P257 1.8V	PP_PWR	PWR	Z2_VDDCORE 18
P258 1.8V	PP_PWR	PWR	Z2_VDDANA 18
P259 1.8V	PP_PWR	PWR	Z2_3V3_1V8_IN 18

GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND_PH	*	GND

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B192	GND	GND		GND
B200	GND	GND	VOLTAGE=0V	GND_AUDIO_CODEC 19 21
B201	GND	GND	VOLTAGE=0V	GND_AUDIO_HP_AMP 19 21 22
B202	GND	GND	VOLTAGE=0V	GND_AUDIO_PT_DK 21 27
B203	GND	GND	VOLTAGE=0V	GND_SPKR_AMP1 20
B204	GND	GND	VOLTAGE=0V	GND_SPKR_AMP2 20
B205	GND	GND	VOLTAGE=0V	GND_PMU
B206	GND	GND		AGND
P217	GND	GND		AGND_U3000 17

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
B163		RST	BB_TRST_L
B164		RST	DBG_RST
B176		RST	DEBUG_RST_L
B171		RST	GSM_TXBURST_IND 5 15 30
B160		RST	JTAG_AP_TRST_L 4 10 42
B170		RST	RST_AP_1V8_L 4
B166		RST	RST_AP_L 4 27 30 37
B172		RST	RST_BB_L 5 30
B174		RST	RST_BB_PMU_L 30 37
B173		RST	RST_BT_L 15 37
B175		RST	RST_DET_L 5 30
B176		GRAPE	RST_GRAPE_L 6 17
B177		RST	RST_L63_L 19 37
B178		RST	RST_PMU_IN 4 37
B179		RST	RST_WLAN_L 15 37
B181		RST	SIMCRD_RST
B183		RST	TP_WLAN_TRST_L
B180		RST	UD881_RST
B182		RST	UD882_RST
B184		RST	

SNS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SNS	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_90D	*	90_OHM_DIFF

E58	NC_HSIC0_DATA2	NO_TEST=TRUE	4 42
E59	NC_HSIC0_STB2	NO_TEST=TRUE	4 42
E60	NC_HSIC1_DATA2	NO_TEST=TRUE	4 42
E61	NC_HSIC1_STB2	NO_TEST=TRUE	4 42
E62	NC_JTAG_AP_TRTCK	NO_TEST=TRUE	4
E64	NC_USB_D1_P	NO_TEST=TRUE	4 42
E65	NC_USB_D1_N	NO_TEST=TRUE	4 42
E66	NC_USB11_D1_P	NO_TEST=TRUE	4 42
E67	NC_USB11_D1_N	NO_TEST=TRUE	4 42
E68	NC_USB_ANALOGTEST0	NO_TEST=TRUE	4
E69	NC_USB_ANALOGTEST1	NO_TEST=TRUE	4
E60	NC_USB_ID0	NO_TEST=TRUE	4
E61	NC_USB_ID1	NO_TEST=TRUE	4
E62	NC_USB_BRICKID1	NO_TEST=TRUE	4
E63	NC_I2S1_MCK	NO_TEST=TRUE	5
E64	NC_I2S1_BCLK	NO_TEST=TRUE	5
E65	NC_I2S1_LRCK	NO_TEST=TRUE	5
E66	NC_I2S1_DIN	NO_TEST=TRUE	5
E67	NC_I2S1_DOUT	NO_TEST=TRUE	5
E68	NC_I2S2_MCK	NO_TEST=TRUE	5
E69	NC_I2S3_MCK	NO_TEST=TRUE	5
E70	NC_AP_GPIO216	NO_TEST=TRUE	5
E71	NC_SPI_FLASH_CS_L	NO_TEST=TRUE	5
E72	NC_SWI_AP	NO_TEST=TRUE	5
E73	NC_SDIO0_WL_CLK	NO_TEST=TRUE	5
E74	NC_SDIO0_WL_CMD	NO_TEST=TRUE	5
E75	NC_SDIO0_WL_DATA<0>	NO_TEST=TRUE	5
E76	NC_SDIO0_WL_DATA<1>	NO_TEST=TRUE	5
E77	NC_SDIO0_WL_DATA<2>	NO_TEST=TRUE	5
E78	NC_SDIO0_WL_DATA<3>	NO_TEST=TRUE	5
E81	NC_SPI3_MISO	NO_TEST=TRUE	5
E83	NC_SPI3_MOSI	NO_TEST=TRUE	5
E82	NC_SPI3_SCLK	NO_TEST=TRUE	5
E85	NC_SPI3_CS_L	NO_TEST=TRUE	5
E90	NC_AP_GPIO3	NO_TEST=TRUE	5
E92	NC_AP_GPIO7	NO_TEST=TRUE	5
E93	NC_AP_GPIO8	NO_TEST=TRUE	5
E94	NC_AP_GPIO11	NO_TEST=TRUE	5
E95	NC_AP_GPIO13	NO_TEST=TRUE	5
E96	NC_BOARD_ID_3	NO_TEST=TRUE	5
E98	NC_AP_GPIO19	NO_TEST=TRUE	5
E97	NC_AP_GPIO31	NO_TEST=TRUE	5
E99	NC_AP_GPIO35	NO_TEST=TRUE	5
E99	NC_AP_GPIO3V1	NO_TEST=TRUE	5
E101	NC_AP_GPIO185	NO_TEST=TRUE	5
E100	NC_AP_GPIO186	NO_TEST=TRUE	5
E102	NC_UART2_RXD	NO_TEST=TRUE	5
E104	NC_UART2_TXD	NO_TEST=TRUE	5
E107	NC_UART4_CTS_L	NO_TEST=TRUE	5
E106	NC_UART4_RTS_L	NO_TEST=TRUE	5
E105	NC_UART4_RXD	NO_TEST=TRUE	5
E108	NC_UART4_TXD	NO_TEST=TRUE	5
E110	NC_UART6_CTSN	NO_TEST=TRUE	5
E109	NC_UART6_RTSN	NO_TEST=TRUE	5

E111	NC_FMI0_CE2_L	NO_TEST=TRUE	6
E113	NC_FMI0_CE3_L	NO_TEST=TRUE	6
E114	NC_FMI0_CE4_L	NO_TEST=TRUE	6
E127	NC_FMI0_CE5_L	NO_TEST=TRUE	6
E128	NC_FMI0_CE6_L	NO_TEST=TRUE	6
E127	NC_FMI0_CE7_L	NO_TEST=TRUE	6
E124	NC_FMI1_CE2_L	NO_TEST=TRUE	6
E123	NC_FMI1_CE3_L	NO_TEST=TRUE	6
E122	NC_FMI1_CE4_L	NO_TEST=TRUE	6
E125	NC_FMI1_CE5_L	NO_TEST=TRUE	6
E121	NC_FMI1_CE6_L	NO_TEST=TRUE	6
E119	NC_FMI1_CE7_L	NO_TEST=TRUE	6
E133	NC_FMI2_CE1_L	NO_TEST=TRUE	6
E132	NC_FMI2_CE2_L	NO_TEST=TRUE	6
E131	NC_FMI2_CE3_L	NO_TEST=TRUE	6
E132	NC_FMI2_CE5_L	NO_TEST=TRUE	6
E135	NC_FMI2_AD<0>	NO_TEST=TRUE	6
E136	NC_FMI2_AD<1>	NO_TEST=TRUE	6
E139	NC_FMI2_AD<2>	NO_TEST=TRUE	6
E138	NC_FMI2_AD<3>	NO_TEST=TRUE	6
E137	NC_FMI2_AD<4>	NO_TEST=TRUE	6
E140	NC_FMI2_AD<5>	NO_TEST=TRUE	6
E141	NC_FMI2_AD<6>	NO_TEST=TRUE	6
E144	NC_FMI2_AD<7>	NO_TEST=TRUE	6
E144	NC_FMI2_ALE	NO_TEST=TRUE	6
E145	NC_FMI2_CLE	NO_TEST=TRUE	6
E143	NC_FMI2_WE_L	NO_TEST=TRUE	6
E146	NC_FMI2_RE_L	NO_TEST=TRUE	6
E147	NC_FMI2_DQS	NO_TEST=TRUE	6
E155	NC_FMI3_CE0_L	NO_TEST=TRUE	6
E153	NC_FMI3_CE1_L	NO_TEST=TRUE	6
E159	NC_FMI3_CE2_L	NO_TEST=TRUE	6
E157	NC_FMI3_CE3_L	NO_TEST=TRUE	6
E155	NC_FMI3_CE4_L	NO_TEST=TRUE	6
E154	NC_FMI3_CE5_L	NO_TEST=TRUE	6
E153	NC_FMI3_CE6_L	NO_TEST=TRUE	6
E152	NC_FMI3_CE7_L	NO_TEST=TRUE	6
E161	NC_FMI3_AD<0>	NO_TEST=TRUE	6
E160	NC_FMI3_AD<1>	NO_TEST=TRUE	6
E158	NC_FMI3_AD<2>	NO_TEST=TRUE	6
E162	NC_FMI3_AD<3>	NO_TEST=TRUE	6
E164	NC_FMI3_AD<4>	NO_TEST=TRUE	6
E163	NC_FMI3_AD<5>	NO_TEST=TRUE	6
E166	NC_FMI3_AD<6>	NO_TEST=TRUE	6
E165	NC_FMI3_AD<7>	NO_TEST=TRUE	6
E172	NC_FMI3_ALE	NO_TEST=TRUE	6
E169	NC_FMI3_CLE	NO_TEST=TRUE	6
E168	NC_FMI3_WE_L	NO_TEST=TRUE	6
E171	NC_FMI3_RE_L	NO_TEST=TRUE	6
E170	NC_FMI3_DQS	NO_TEST=TRUE	6
E174	NC_MIPI_VSYNC_H4	NO_TEST=TRUE	7
E177	NC_MIPI0C_AP_DATA_P<2>	NO_TEST=TRUE	7 43
E176	NC_MIPI0C_AP_DATA_N<2>	NO_TEST=TRUE	7 43
E179	NC_MIPI0C_AP_DATA_P<3>	NO_TEST=TRUE	7 43
E180	NC_MIPI0C_AP_DATA_N<3>	NO_TEST=TRUE	7 43
E181	NC_MIPI1C_AP_DATA_P<1>	NO_TEST=TRUE	7 43
E183	NC_MIPI1C_AP_DATA_N<1>	NO_TEST=TRUE	7 43
E183	NC_ISP_AP_1_FLASH	NO_TEST=TRUE	7
E182	NC_ISP_AP_1_PRE_FLASH	NO_TEST=TRUE	7

E189	NC_DDR0_CKE<1>	NO_TEST=TRUE	8
E191	NC_DDR1_CKE<1>	NO_TEST=TRUE	8
E190	NC_DDR2_CKE<1>	NO_TEST=TRUE	8
E192	NC_DDR3_CKE<1>	NO_TEST=TRUE	8
E196	NC_DDR0_CSN<1>	NO_TEST=TRUE	8
E195	NC_DDR1_CSN<1>	NO_TEST=TRUE	8
E193	NC_DDR2_CSN<1>	NO_TEST=TRUE	8
E200	NC_DDR3_CSN<1>	NO_TEST=TRUE	8
E205	NC_PMU_VBUCK0_SW0_G	NO_TEST=TRUE	36
E204	NC_PMU_VBUCK0_SW0_S	NO_TEST=TRUE	36
E226	NC_VBUS_A_OV_L	NO_TEST=TRUE	36
E497	NC_BOARD_TEMP7	NO_TEST=TRUE	37
E498	NC_BOARD_TEMP8	NO_TEST=TRUE	37
E210	NC_PMU_GPIO12	NO_TEST=TRUE	37
E212	NC_PMU_GPIO13	NO_TEST=TRUE	37
E213	NC_PMU_GPIO16	NO_TEST=TRUE	37
E213	NC_PMU_GPIO17	NO_TEST=TRUE	37
E216	NC_PMU_AMUX_A0	NO_TEST=TRUE	37
E218	NC_PMU_AMUX_A1	NO_TEST=TRUE	37
E217	NC_PMU_AMUX_A2	NO_TEST=TRUE	37
E220	NC_PMU_AMUX_A3	NO_TEST=TRUE	37
E219	NC_PMU_AMUX_AY	NO_TEST=TRUE	37
E223	NC_PMU_AMUX_B0	NO_TEST=TRUE	37
E222	NC_PMU_AMUX_B1	NO_TEST=TRUE	37
E221	NC_PMU_AMUX_B2	NO_TEST=TRUE	37
E222	NC_PMU_AMUX_B3	NO_TEST=TRUE	37
E225	NC_PMU_AMUX_BY	NO_TEST=TRUE	37

NET_SPACING_TYPE=ANLG

E232	NC_BON_L1	NO_TEST=TRUE	18
E233	NC_BON_L3	NO_TEST=TRUE	18
E232	NC_BON_L5	NO_TEST=TRUE	18
E240	NC_EAROUT_AP	NO_TEST=TRUE	19
E241	NC_EAROUT_AN	NO_TEST=TRUE	19
E233	NC_LINE_IN1_CODEC	NO_TEST=TRUE	19
E233	NC_LINE_IN1_REF_CODEC	NO_TEST=TRUE	19
E234	NC_LINE_IN2_CODEC	NO_TEST=TRUE	19
E233	NC_LINE_IN2_REF_CODEC	NO_TEST=TRUE	19
E235	NC_MIC1_BIAS_CODEC	NO_TEST=TRUE	19
E237	NC_MIC1P_CODEC	NO_TEST=TRUE	19
E236	NC_MIC1N_CODEC	NO_TEST=TRUE	19
E238	NC_MIC1_FILT_CODEC	NO_TEST=TRUE	19
E240	NC_D5703_6	NO_TEST=TRUE	
E243	NC_D5700_6	NO_TEST=TRUE	
E242	NC_D5701_6	NO_TEST=TRUE	
E243	NC_D5702_6	NO_TEST=TRUE	
E244	NC_LCM2_EN	NO_TEST=TRUE	37
E245	NC_VLCM1	NO_TEST=TRUE	37

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