


V035-00A DESIGN BASE ON P216-A01 DESIGN

PAGE SUMMARY:

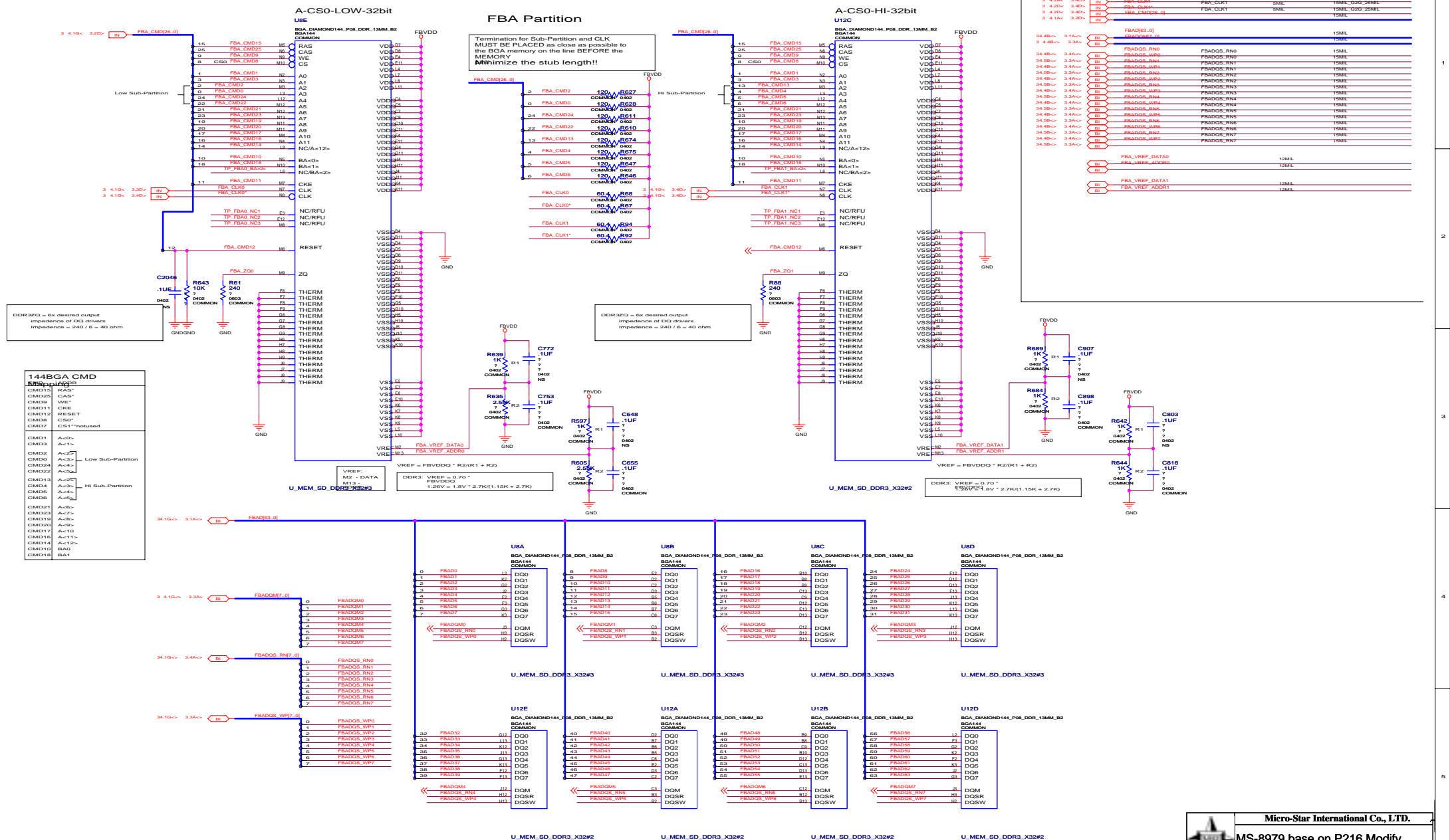
Schmatic From 8970-11A Modify
BOM From 8970-020 Modify

PAGE SUMMARY:

PAGE15.add Scart_VCC
PAGE19.ADD Linear Power for Scart_Vcc
PAGE20.ADD mos/diode/cap for nvvdd and fbvddq

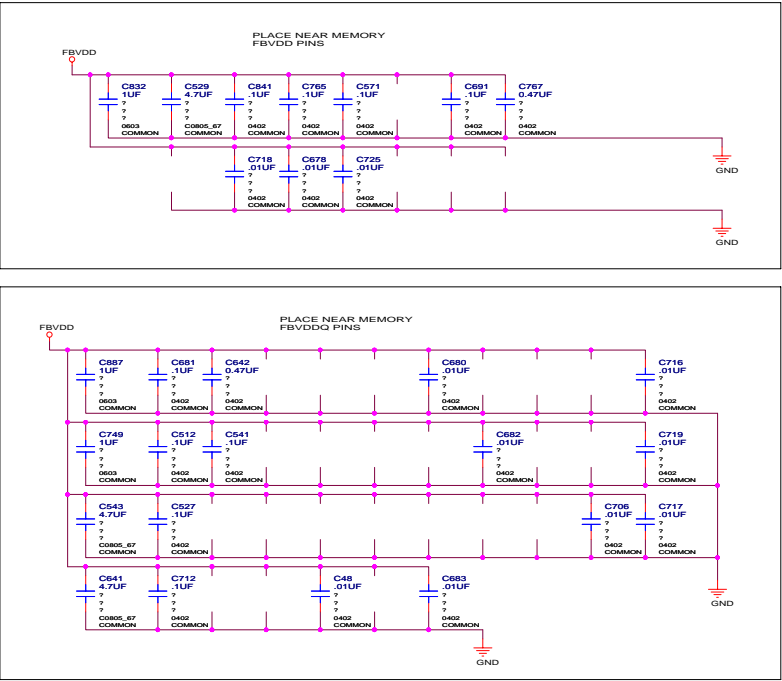
	Micro-Star International Co., LTD.		
	MS-8979 base on P216 Modify		
	Doc	Document Number	Rev
	Custom		00A
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5 FrameBuffer: Partition A 8Mx32 BGA144 DDR3

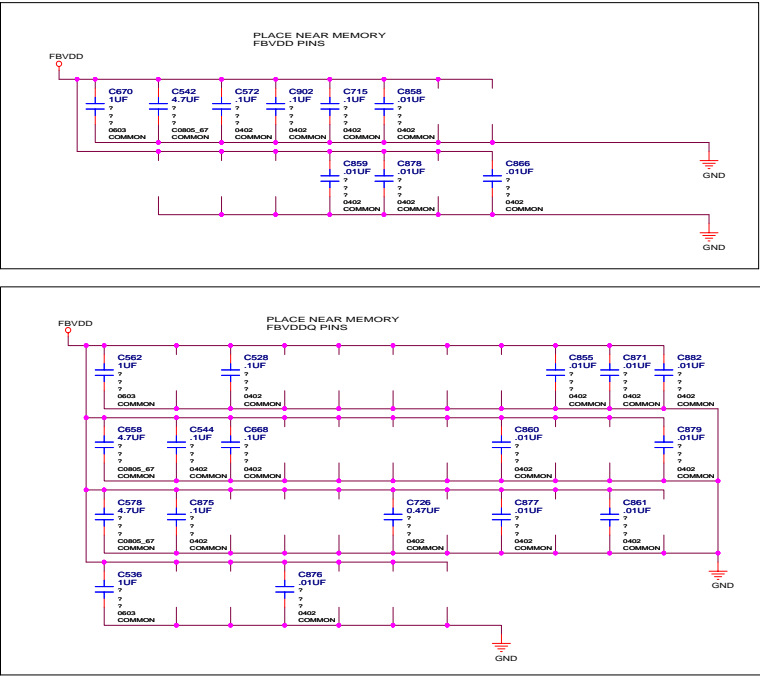


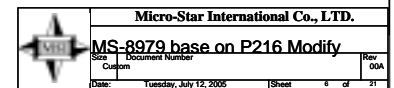
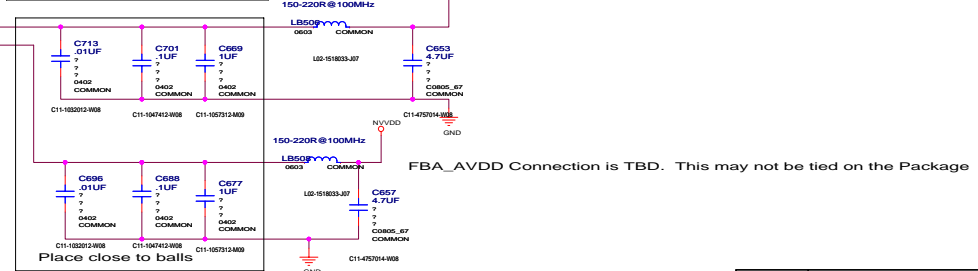
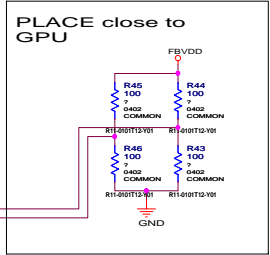
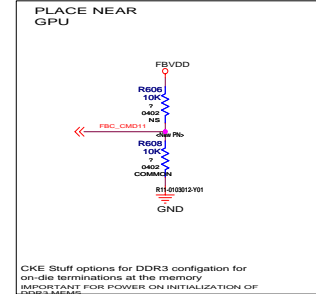
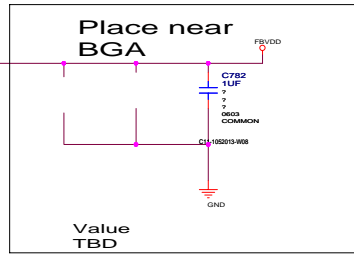
FRAME BUFFER: PARTITION A
DECOUPLING

Decoupling for FBA 0..31

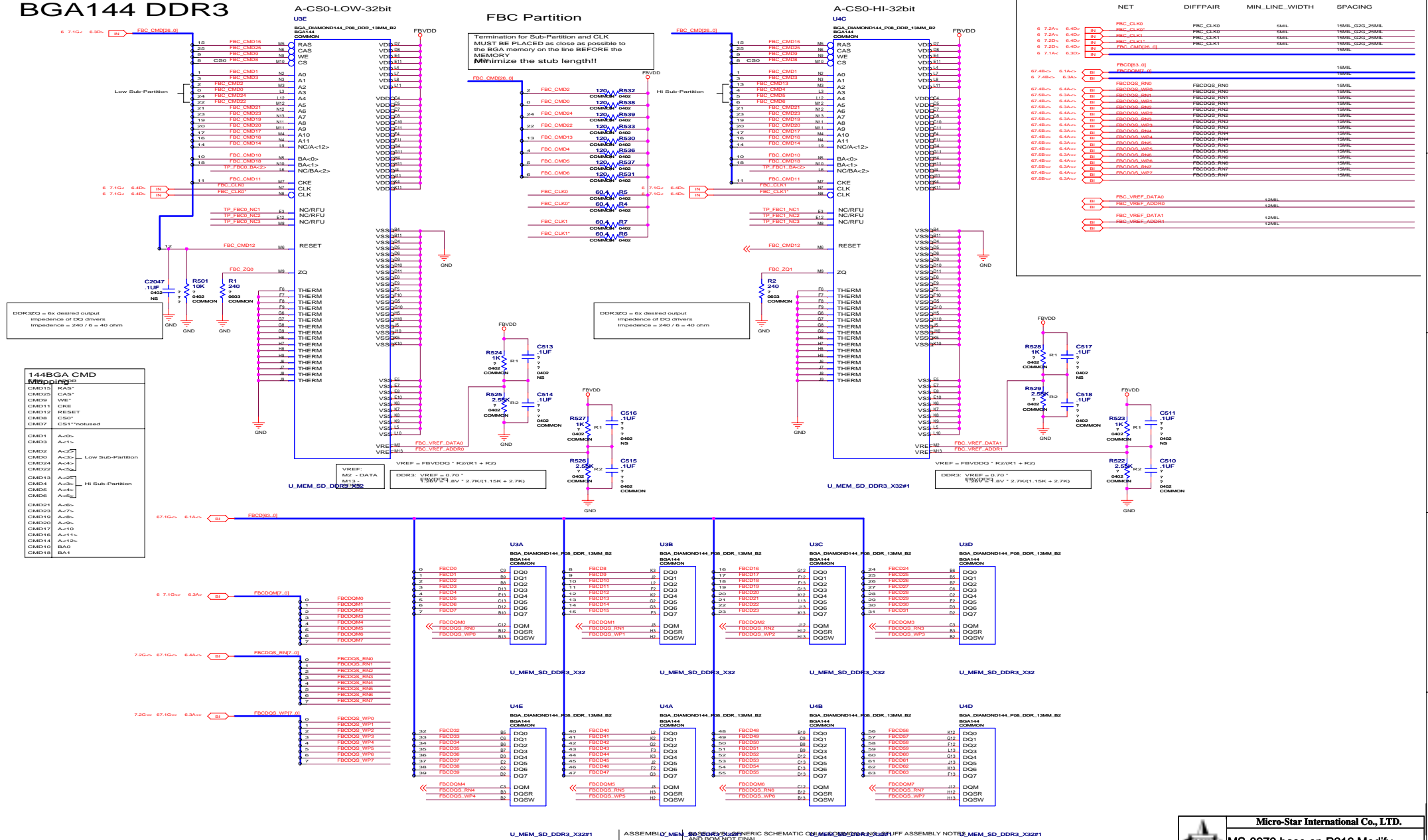


Decoupling for FBA 32..63



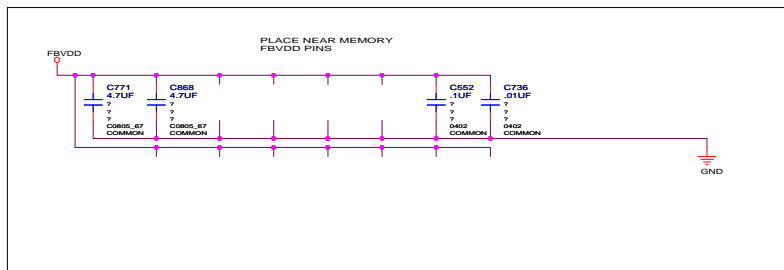


FRAMEBUFFER: PARTITION C 8Mx32
BGA144 DDR3

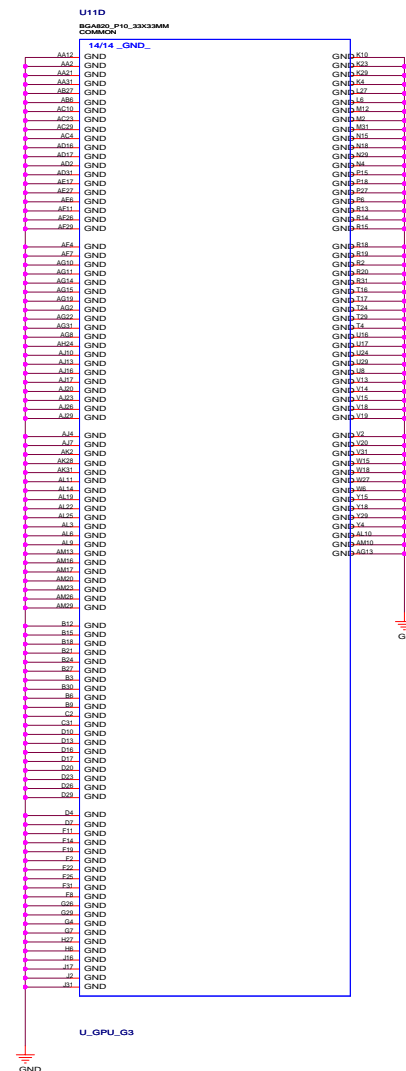
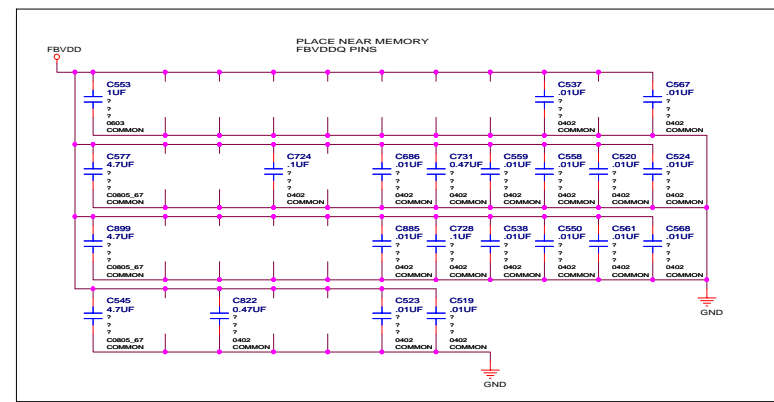
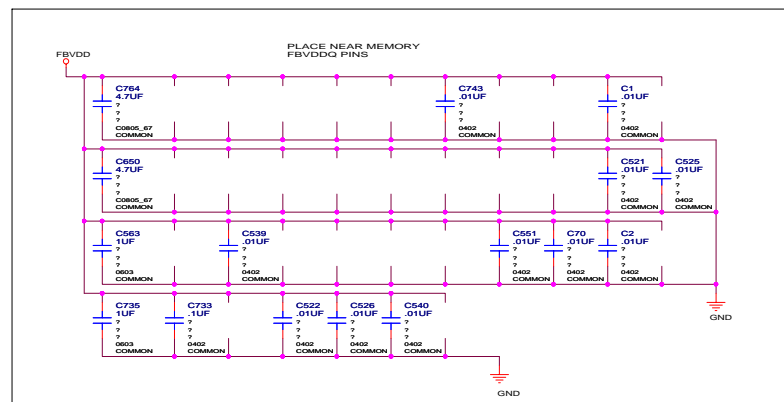
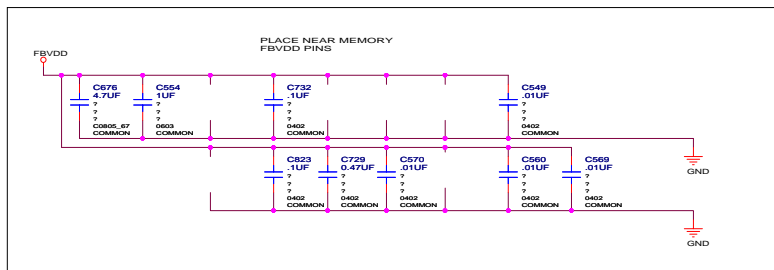


FRAMEBUFFER: PARTITION C DECOUPLING

Decoupling for FBC 0..31



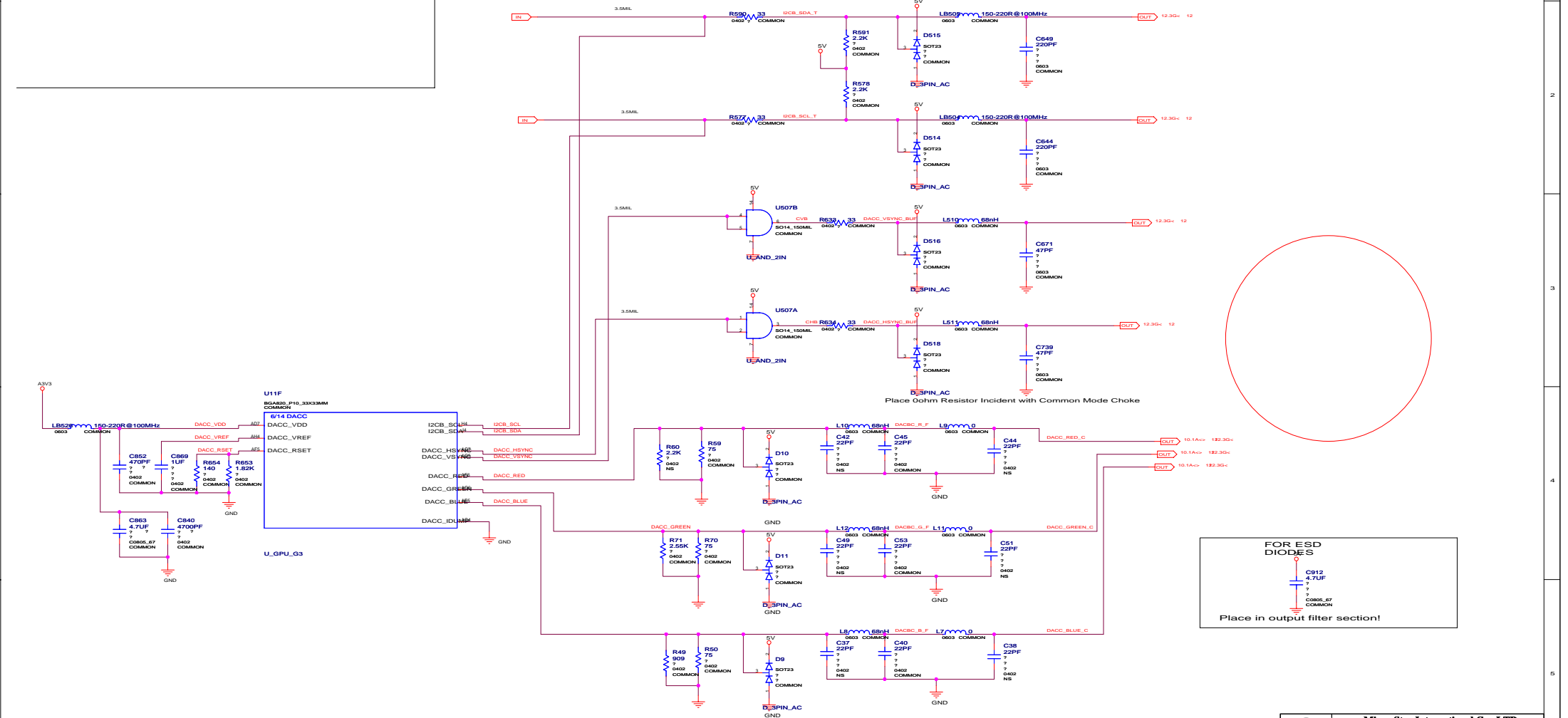
Decoupling for FBC 32..63



	NET_NAME	NET_SPACING_RULE	IMPEDANCE	MIN_LINE_WIDTH
	DACC_VDD			12MIL
BI	DACC_VREF			12MIL
BI	DACC_RSET			12MIL
BI	DACC_GREEN	20MIL	U111 AFB R59 1.37.50 ohm 2 %	
BI	DACC_BLUE	20MIL	U111 AFB R59 1.37.50 ohm 2 %	
BI	DACC_R_F	20MIL	L10 2.1 1.75.00 ohm 2 %	
BI	DACC_R_F	20MIL	L12 2.1 1.75.00 ohm 2 %	
BI	DACC_R_F	20MIL	L8 1.7 1.75.00 ohm 2 %	
12.3G+	DACC_RED_C	20MIL	L9 2.1 1.75.00 ohm 2 %	
10.1G+	DACC_GREEN_C	20MIL	L11 2.1 1.75.00 ohm 2 %	
10.4G+	DACC_BLUE_C	20MIL	L7 2.1 1.75.00 ohm 2 %	

Secondary Display
(DACC), To DVI-I

DACC
RGB-FILTER



INTERNAL TMDS .. LINK A & B

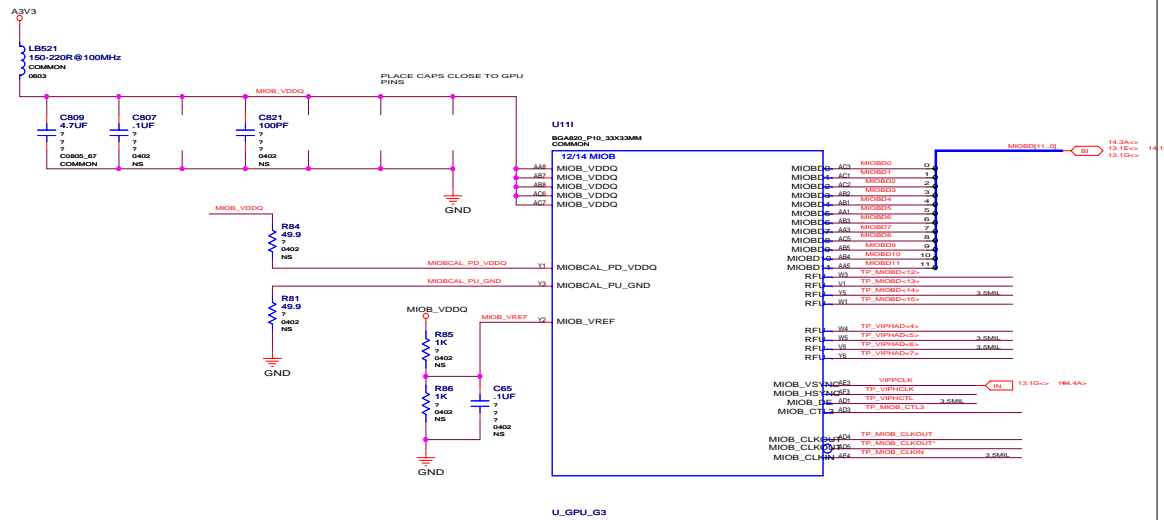
INTERNAL TMDS .. LINK A & B



et name change from 5v_ENBL* to EN_FBVDD*

	NETNAME	MIN_LINE_WIDTH	VOLTAGE
TMD5_PL1VDD	TMD5_PL1VDD	12MIL	3.3V
	IFPAB_PL1VDD	12MIL	3.3V
TMD5_I0VDD	TMD5_I0VDD	12MIL	3.3V
	IFPAB_I0VDD	12MIL	3.3V
	IFPABRESET	12MIL	
	TMD5_I0BACK	12MIL	

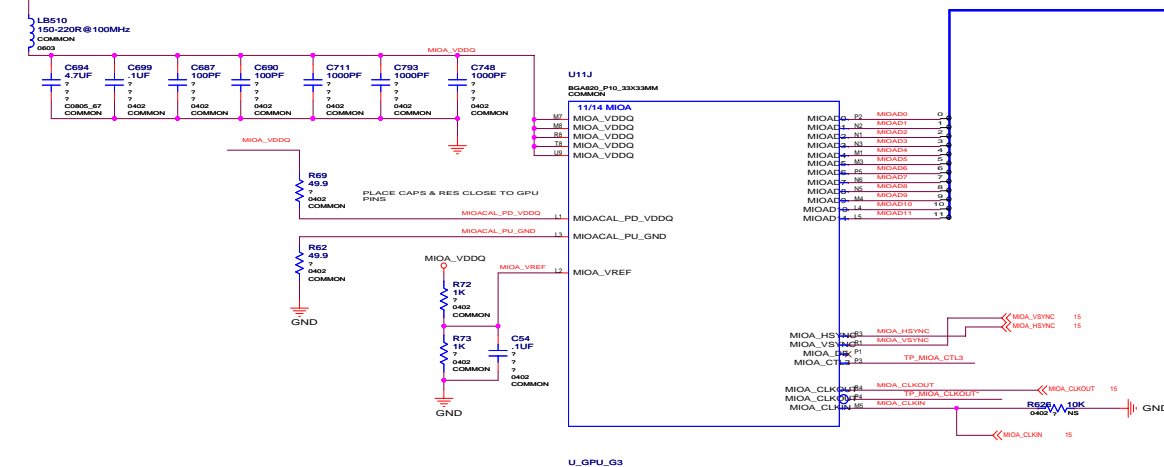
G3 VIP/MIOB



NETNAME	MIN_LINE_WIDTH	SPACING RULE
MIOB_VDDQ	12MIL	12MIL
MIOB_VREF	12MIL	12MIL
MIOA_VDDQ	12MIL	12MIL
MIOA_VREF	12MIL	12MIL

G3 MIOA

Change input power from MIOA_2V5 to A3V3




Feature Connector

Remove feature connector

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (INCLUDING BUT NOT LIMITED TO: BOM, SPC, TEST PLANS, AND OTHER DOCUMENTS) ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO: THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

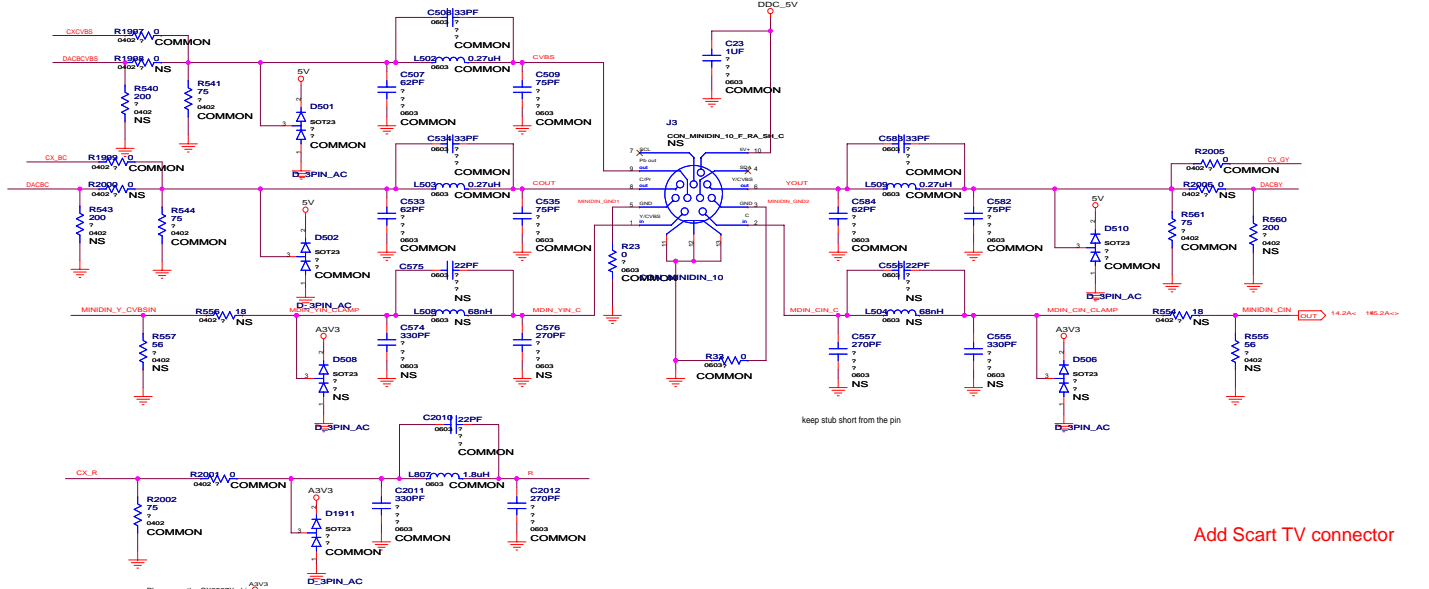
G		H	
NETNAME	MIN_LINE_WIDTH		
VDDA	12MIL		
VDDX	12MIL		
VDDC	12MIL		



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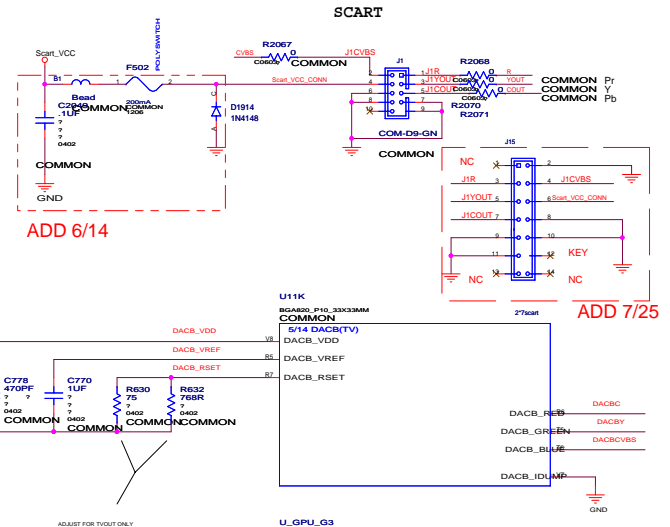
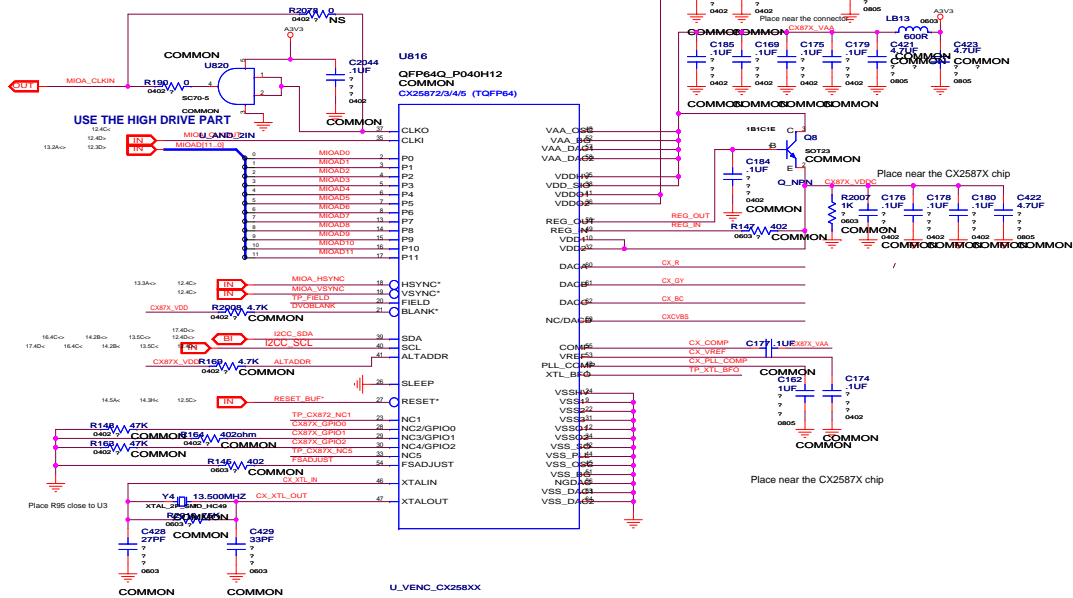
DACB .. MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES


NET_NAME	MIN_LINE_WIDTH	IMPEDANCE	NET_SPACING_RULE
OUT1 DABC_C_OUT		U11.86, R544.1, 37.50 ohm @ 5%	20MIL
OUT1 DABC_VIBE_OUT		U11.75, R561.1, 37.50 ohm @ 5%	20MIL
OUT1 DABC_PB_OUT		U11.75, R561.1, 37.50 ohm @ 5%	20MIL
OUT1		U11.75, R561.1, 37.50 ohm @ 5%	20MIL
MDIN_PBOUT_C			20MIL
MDIN_GND_C			20MIL
MDIN_VIB_C			20MIL
MDIN_VIB_CLAMP			20MIL
MDIN_VIB_C			20MIL
MDIN_VIB_CLAMP			20MIL
MDIN_CIN_C			20MIL
MDIN_CIN			20MIL
MDIN_CIN_CLAMP			20MIL
DABC_VDD	128MIL		
DABC_VREF	128MIL		
DABC_RESET	128MIL		

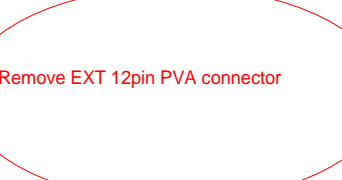


Add Scart TV connector


Add Scart TV chip CX25874/5



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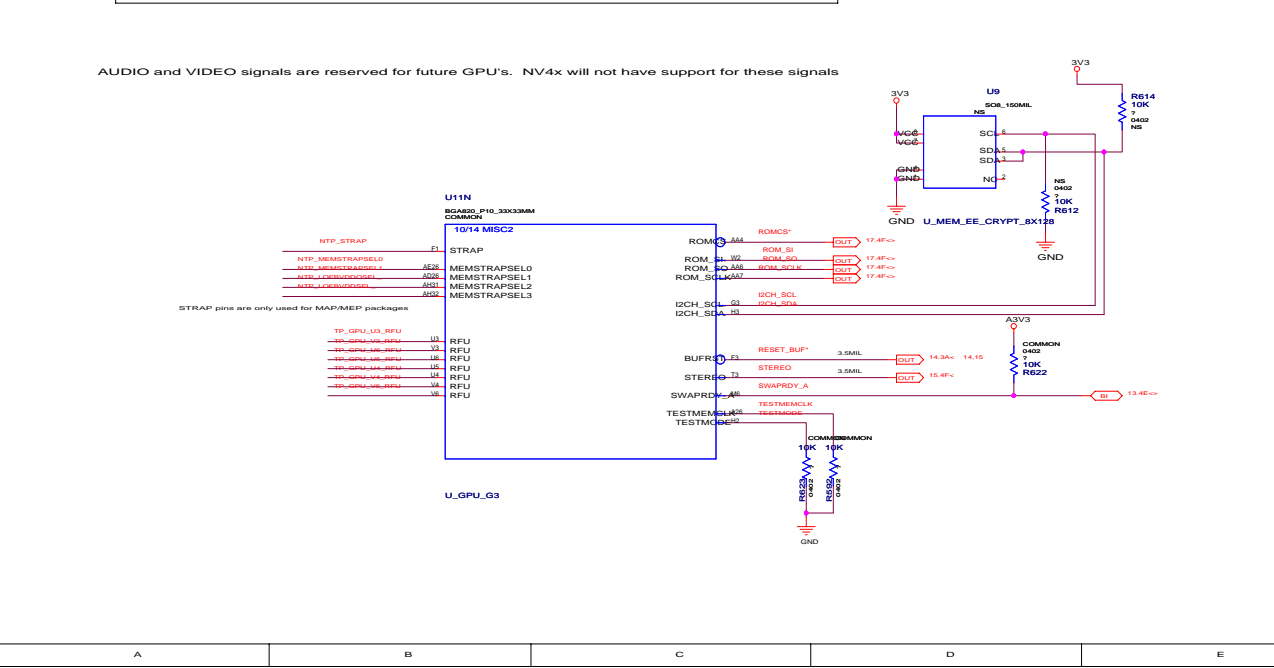
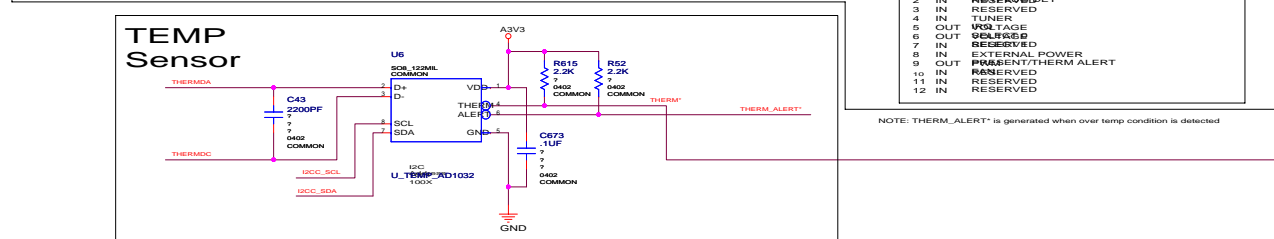
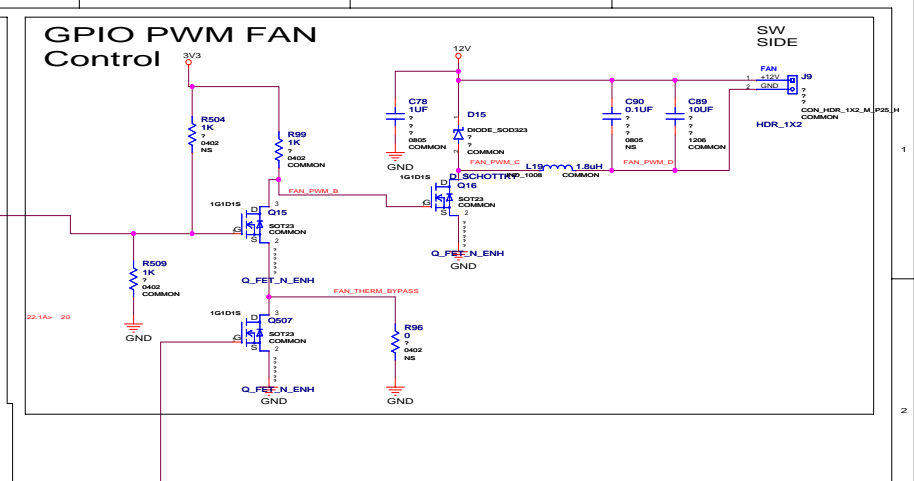
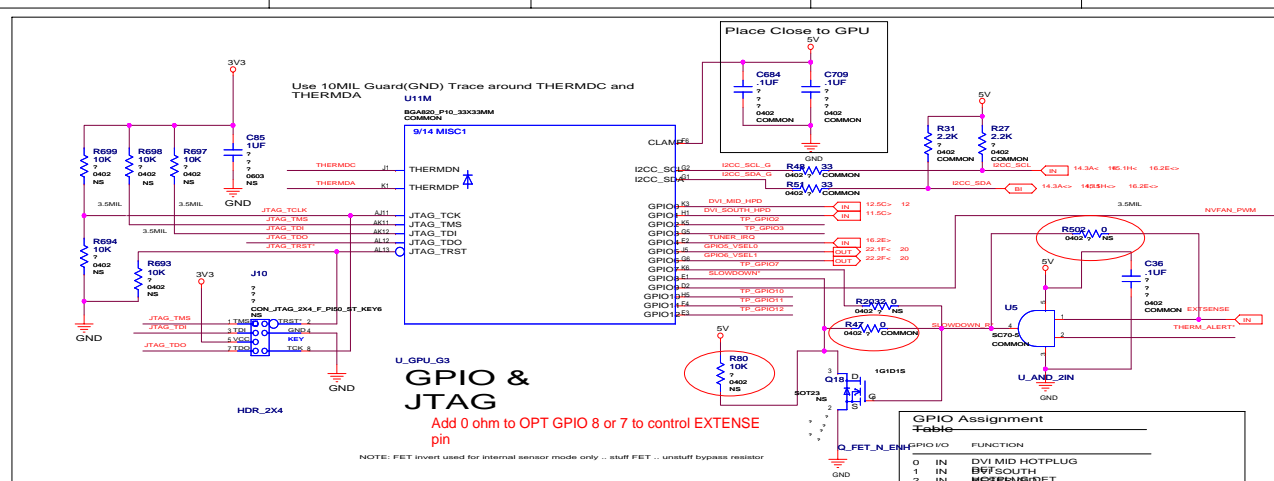
A large red oval graphic that frames the text "Remove EXT 12pin PVA connector".

Remove EXT 12pin PVA connector

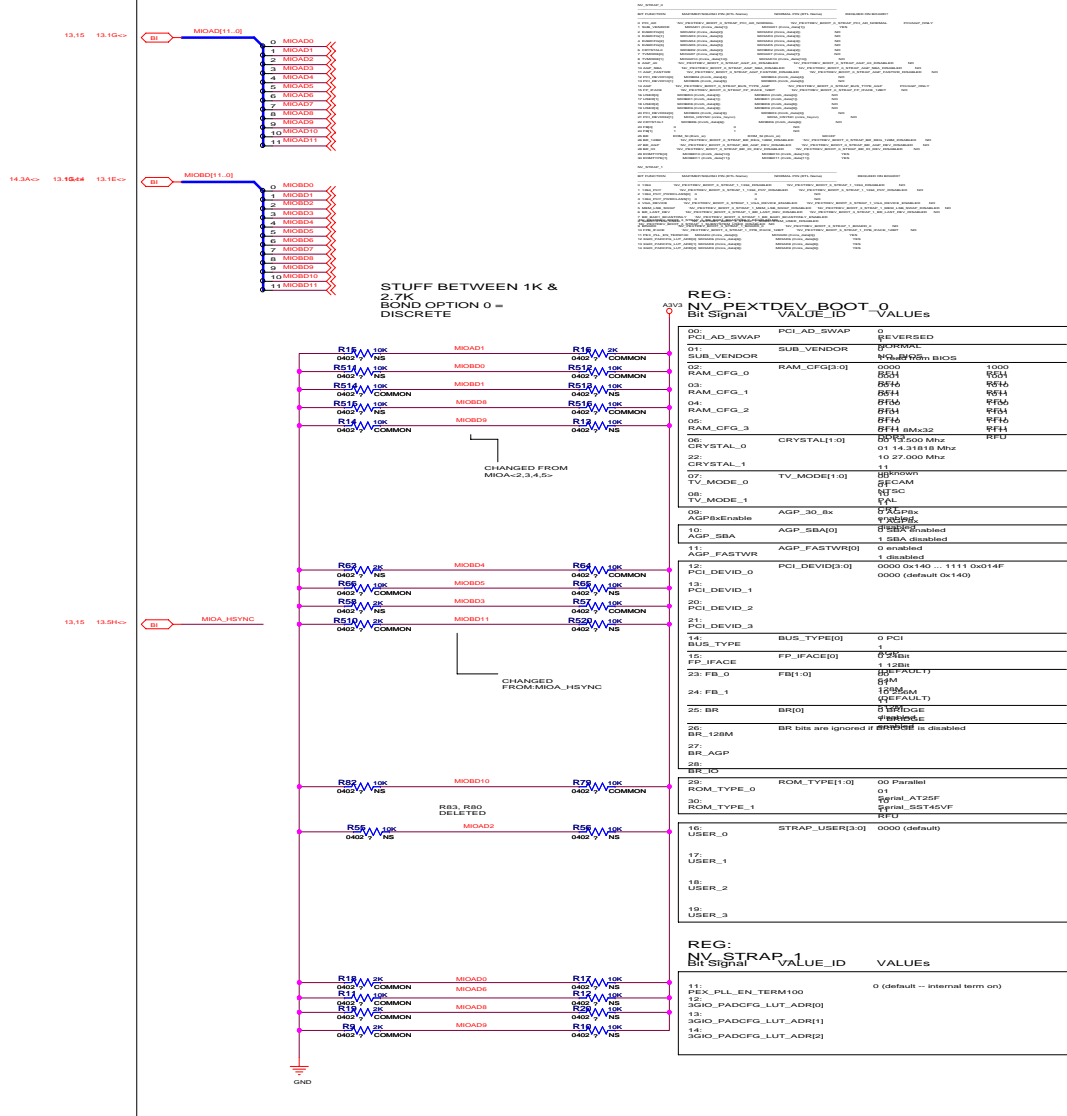


DEL EXT 4-PIN CONNECTOR

[illegible]



Assembly:
BIOS



REG: NV_PEXTDEV_BOOT_0

Bit Signal

VALUE_ID

VALUES

00: PCI_AD_SWAP

PCI_AD_SWAP

0 REVERSED

01: SUB_VENDOR

SUB_VENDOR

00000000

02: RAM_CFG_0

RAM_CFG[2:0]

00000000 RAM0

03: RAM_CFG_1

RAM_CFG_1

00000000 RAM1

04: RAM_CFG_2

RAM_CFG_2

00000000 RAM2

05: RAM_CFG_3

RAM_CFG_3

00000000 RAM3

06: CRYSTAL_0

CRYSTAL[1:0]

00000000 00000000 Mhz

22: CRYSTAL_1

CRYSTAL_1

01 1.31618 Mhz

07: TV_MODE_0

TV_MODE[1:0]

00000000 10.27.000 Mhz

08: TV_MODE_1

TV_MODE_1

00000000 11.11.000 Mhz

09: AGP8xEnable

AGP_30_8x

0 AGP8x ENABLE

10: AGP_SBA

AGP_SBA[0]

0 SBA enabled

11: AGP_FASTWR

AGP_FASTWR[0]

0 enabled

12: PCI_DEVID_0

PCI_DEVID[3:0]

0000 0x140F 0000 (default 0x140)

13: PCI_DEVID_1

PCI_DEVID_1

14: PCI_DEVID_2

PCI_DEVID_2

21: PCI_DEVID_3

PCI_DEVID_3

15: BUS_TYPE

BUS_TYPE[0]

0 PCI

16: IFACE

IFACE[0]

0 PCI

23: FB_0

FB[1:0]

00000000 00000000

24: FB_1

FB_1

00000000 00000000

25: BR

BR[0]

0 BR0

26: BR_128M

BR

BR bits are ignored if BR[0] is disabled

27: BR_AGP

BR_AGP

28: BR_ID

BR_ID

00 Parallel

29: ROM_TYPE_0

ROM_TYPE[1:0]

01 Parallel

30: ROM_TYPE_1

ROM_TYPE_1

01 Parallel

31: ROM_TYPE_2

ROM_TYPE_2

01 Parallel

32: ROM_TYPE_3

ROM_TYPE_3

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33: ROM_TYPE_4

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34: ROM_TYPE_5

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35: ROM_TYPE_6

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01 Parallel

210: ROM_TYPE_181

ROM_TYPE_181

01 Parallel

211: ROM_TYPE_182

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212: ROM_TYPE_183

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213: ROM_TYPE_184

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214: ROM_TYPE_185

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220: ROM_TYPE_191

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221: ROM_TYPE_192

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227: ROM_TYPE_198

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229: ROM_TYPE_200

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230: ROM_TYPE_201

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231: ROM_TYPE_202

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232: ROM_TYPE_203

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235: ROM_TYPE_206

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236: ROM_TYPE_207

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237: ROM_TYPE_208

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238: ROM_TYPE_209

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239: ROM_TYPE_210

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240: ROM_TYPE_211

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241: ROM_TYPE_212

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242: ROM_TYPE_213

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243: ROM_TYPE_214

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255: ROM_TYPE_226

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256: ROM_TYPE_227

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257: ROM_TYPE_228

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259: ROM_TYPE_230

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261: ROM_TYPE_232

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262: ROM_TYPE_233

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263: ROM_TYPE_234

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264: ROM_TYPE_235

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269: ROM_TYPE_240

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293: ROM_TYPE_264

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299: ROM_TYPE_270

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300: ROM_TYPE_271

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367: ROM_TYPE_338

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368: ROM_TYPE_339

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369: ROM_TYPE_340

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370: ROM_TYPE_341

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371: ROM_TYPE_342

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372: ROM_TYPE_343

ROM_TYPE_343

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373: ROM_TYPE_344

ROM_TYPE_344

01 Parallel

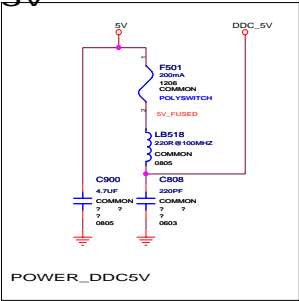
374: ROM_TYPE_345

ROM_TYPE_345

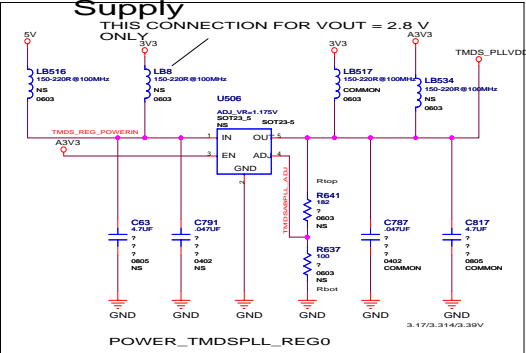
01 Parallel

375: ROM

Power Supply ...
TMD5/A3V3/FBVDD
DDC
5V



TMD5 AB/CD PLL
Supply



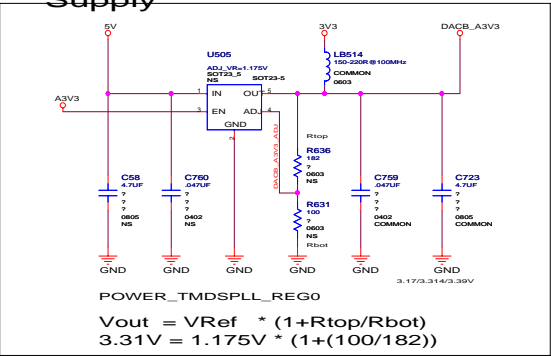
$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$
 $3.31V = 1.175V * (1 + (100/182))$

MIOA_VDDQ



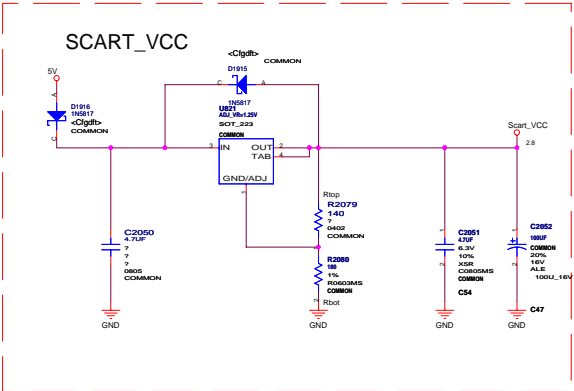
NETNAME	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	12MIL	5V
3V3	12MIL	3.3V
5V	12MIL	5V
TMD5AB/CD PLL	12MIL	3.3V
TMD5_PLLVDD	12MIL	3.3V
12V	30MIL	12V
MIOA_2V5	12MIL	2.5V
GND	30MIL	0V
DACB_A3V3_ADJ	10MIL	3.3V
DACB_A3V3	12MIL	3.3V

DACB
Supply



$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$
 $3.31V = 1.175V * (1 + (100/182))$

SCART_VCC



ADD 6/14

ISL6549 for Nvidia NV4x Graphic card power ckt

A

1.21V/1.68A(ambient)

B

C

D

D

ADD 6/16

NVVD & PEX1V2

Change all power(NVVD,FBVD/Q,A3V3,5V & ADD EXT PWR)

$$NVVD = VREF(0.8) \times (1 + R_V/R_B)$$

GPIO6_VSEL1	GPIO5_VSEL0	NVVD
0	0	1.1V
0	1	1.2V(DEFAULT)
1	0	1.3V
1	1	1.4V

1.35V(Fix)/24A(ambient)

Add External Power Connector

ADD 7/25

ADD 6/21

5V & A3V3

FBVD

$$FBVD = VREF(1.265) \times (1 + R_V/R_B)$$

PWR current share for FBVD (OPT)

2.04V/9.08A(ambient)

OPT(if power rail not enough),default NS

