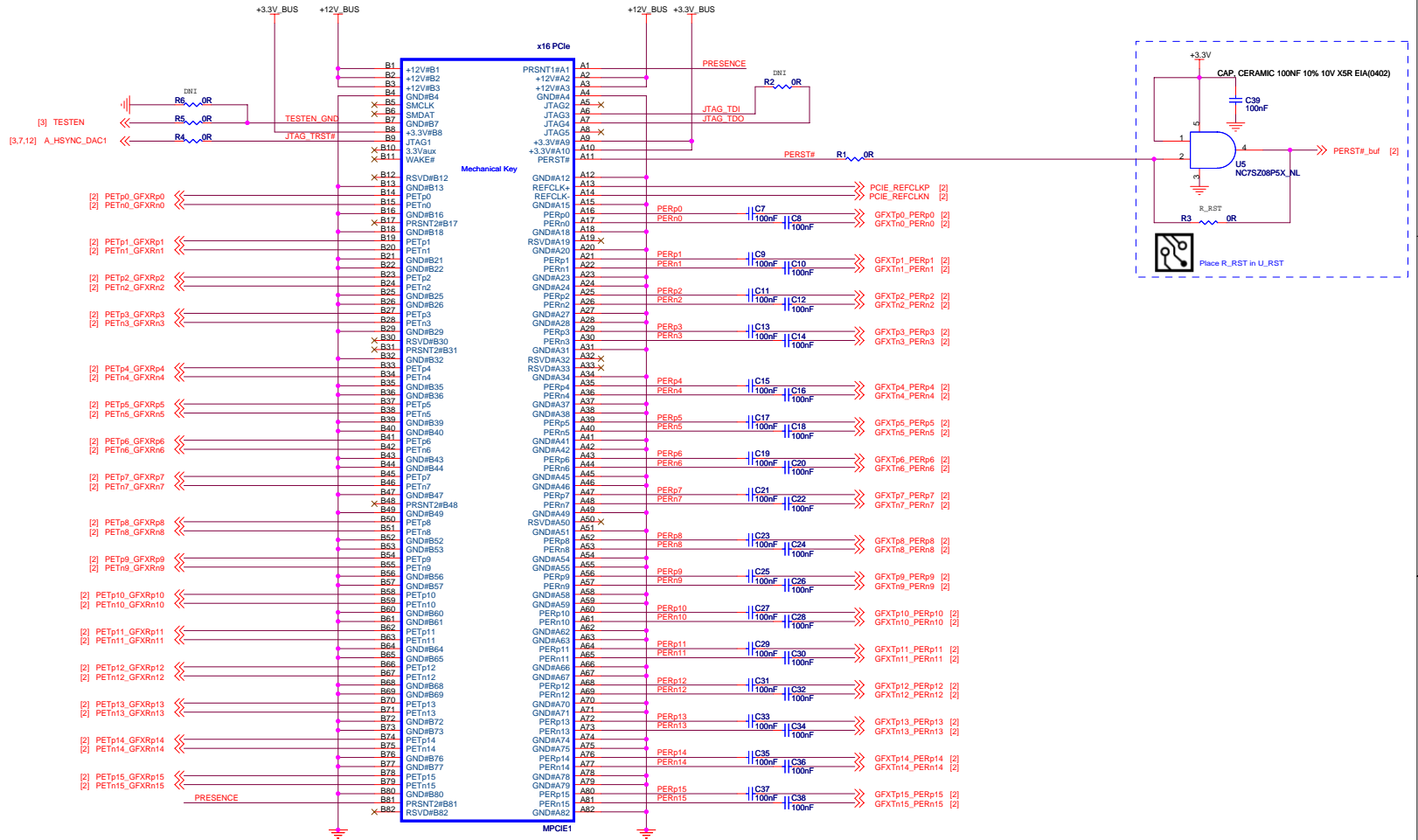
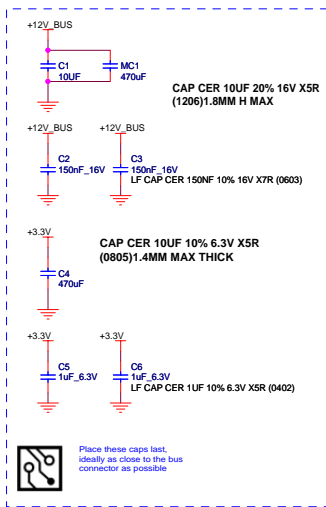


PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

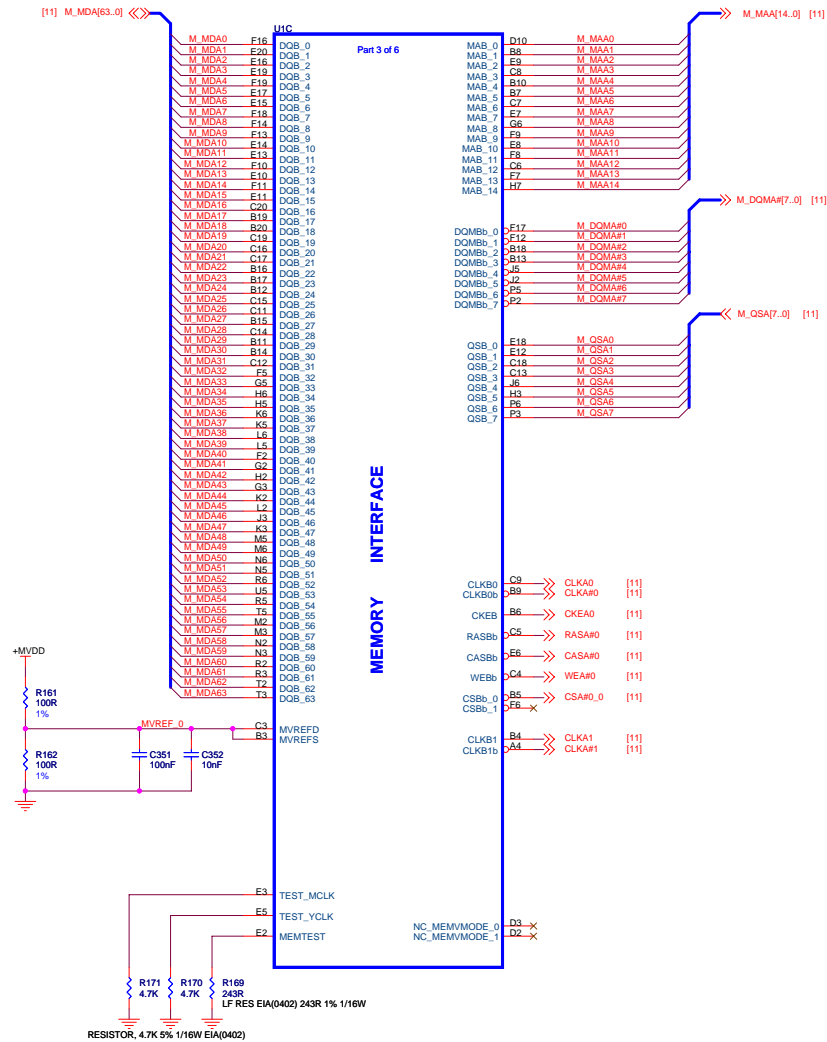


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Channel A

Register control is from Registers named CHANNEL B although this ASIC package only has 1 channel



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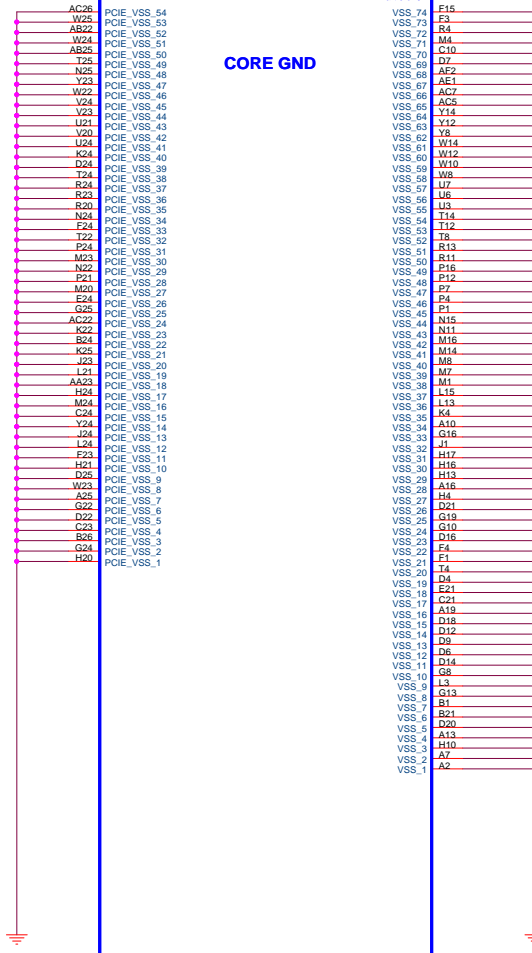
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JHE

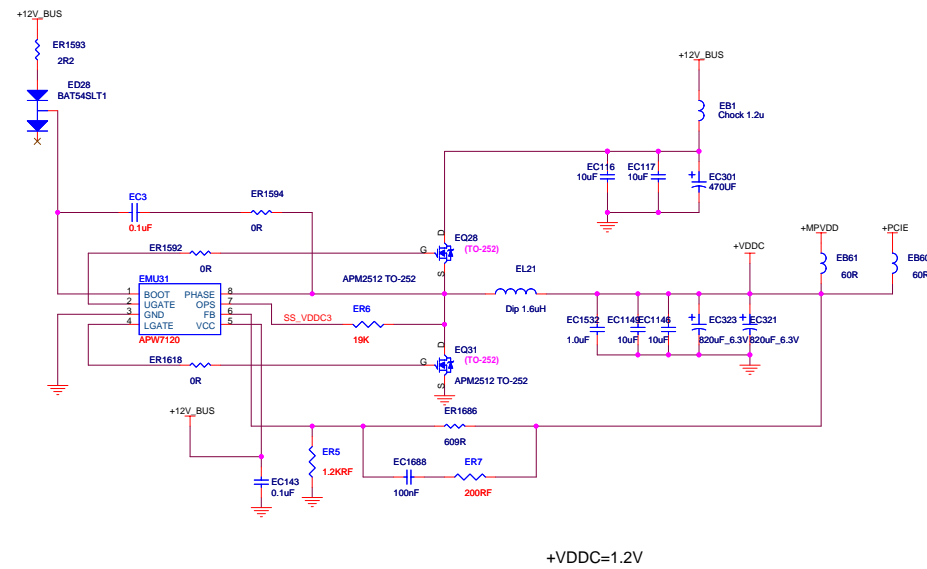
Part 5 of 6

CORE GND



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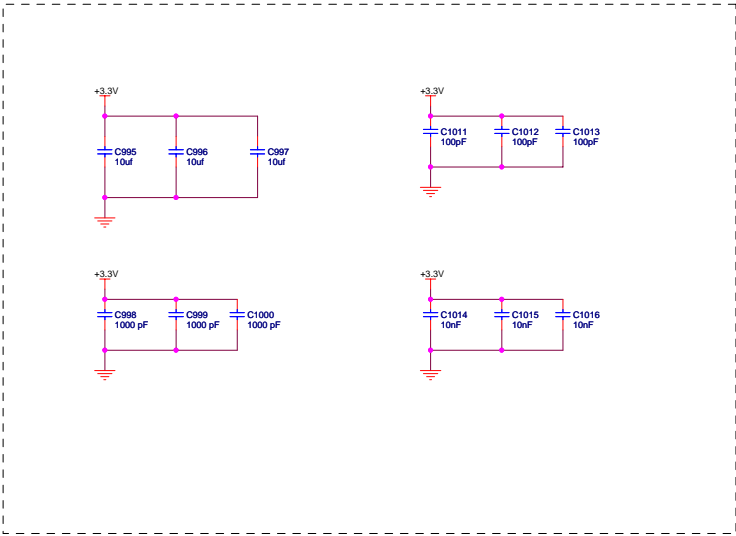
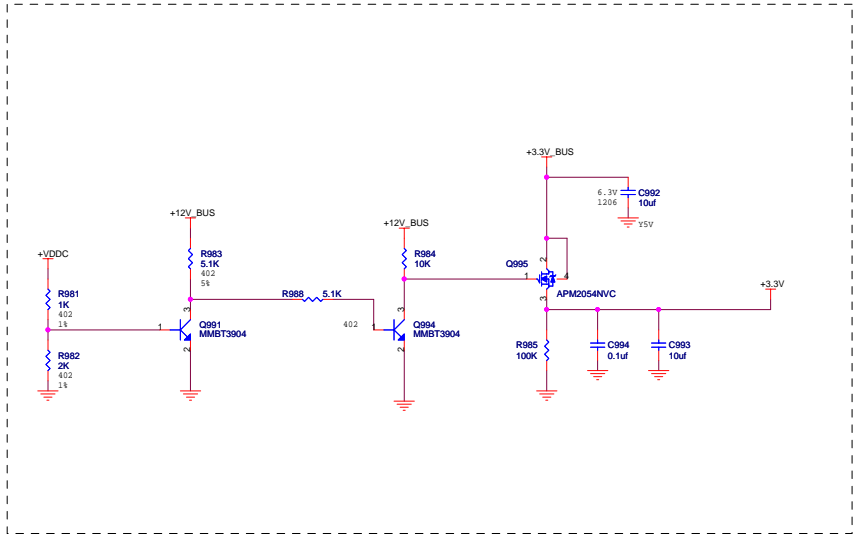
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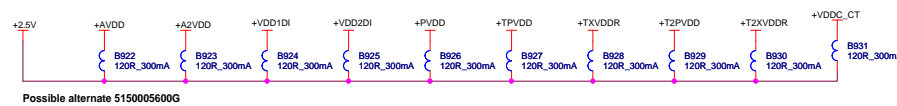
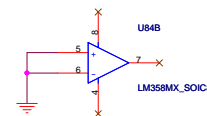
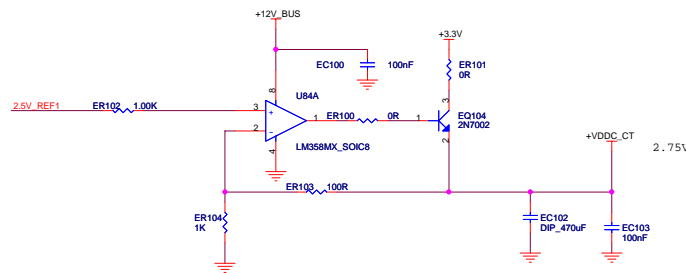
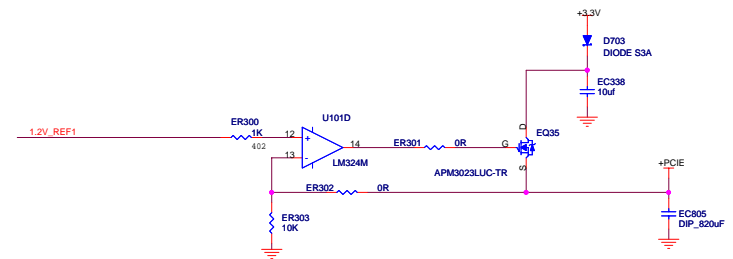
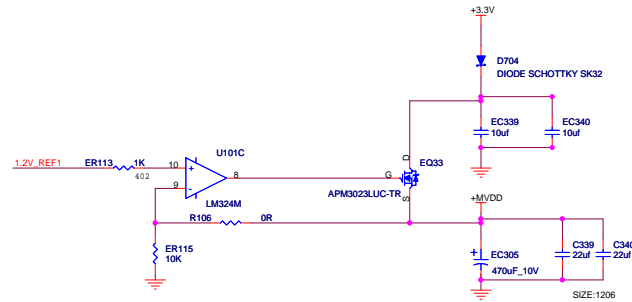
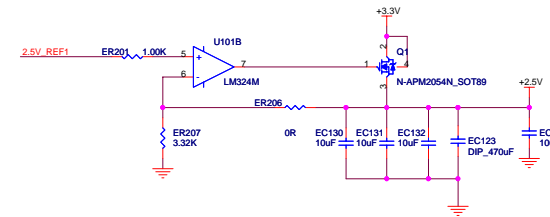
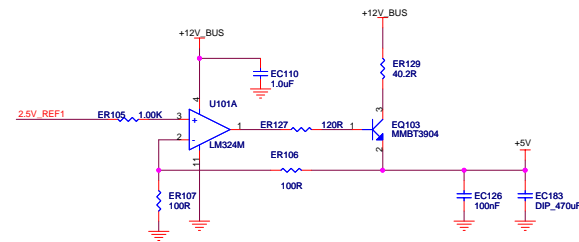
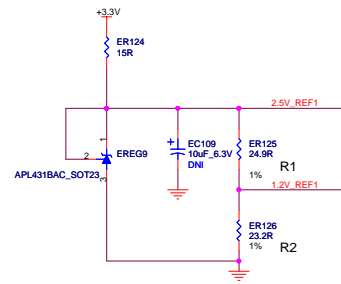


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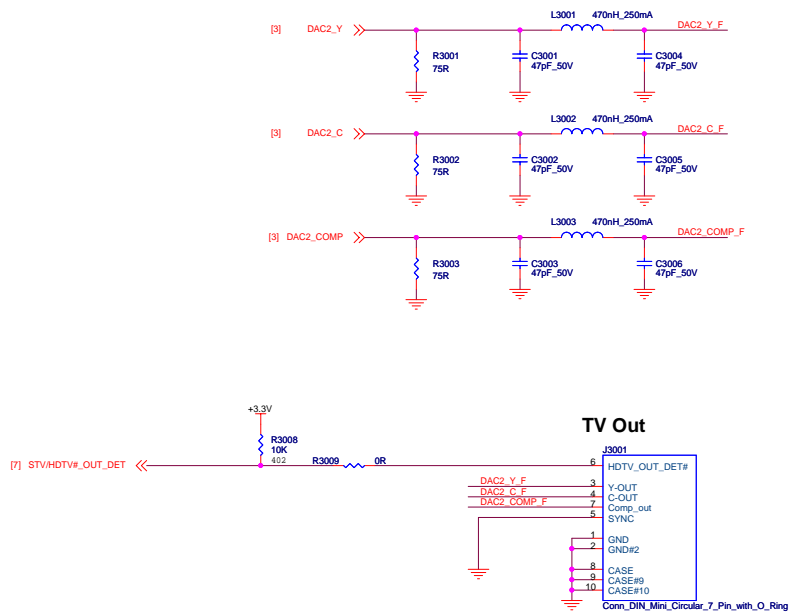
power
sequence





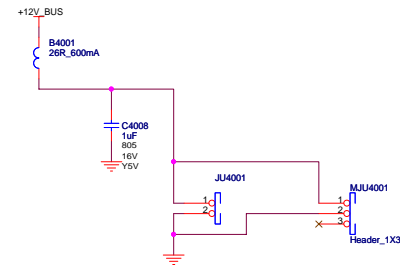
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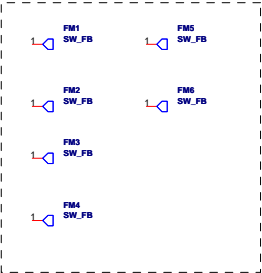
DVI/VGA SCREWS

ASSY-SCREW1

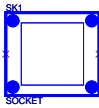
SCREW
JACKSCREW
ASSY
7020000800

ASSY-SCREW2

SCREW
JACKSCREW
ASSY
7020000800



DNI



PCB DESIGN NOTE:
ASIC REQUIREMENTS
FOR THIS SOCKET:
1. USE ALTERNATE ASIC DECAL
WITH SQUARE VIA PADS.
2. SOCKET & ASIC PADS
REQUIRED GOLD PLATING.
SEE SPEC. FOR DETAILS.



<Variant Name>



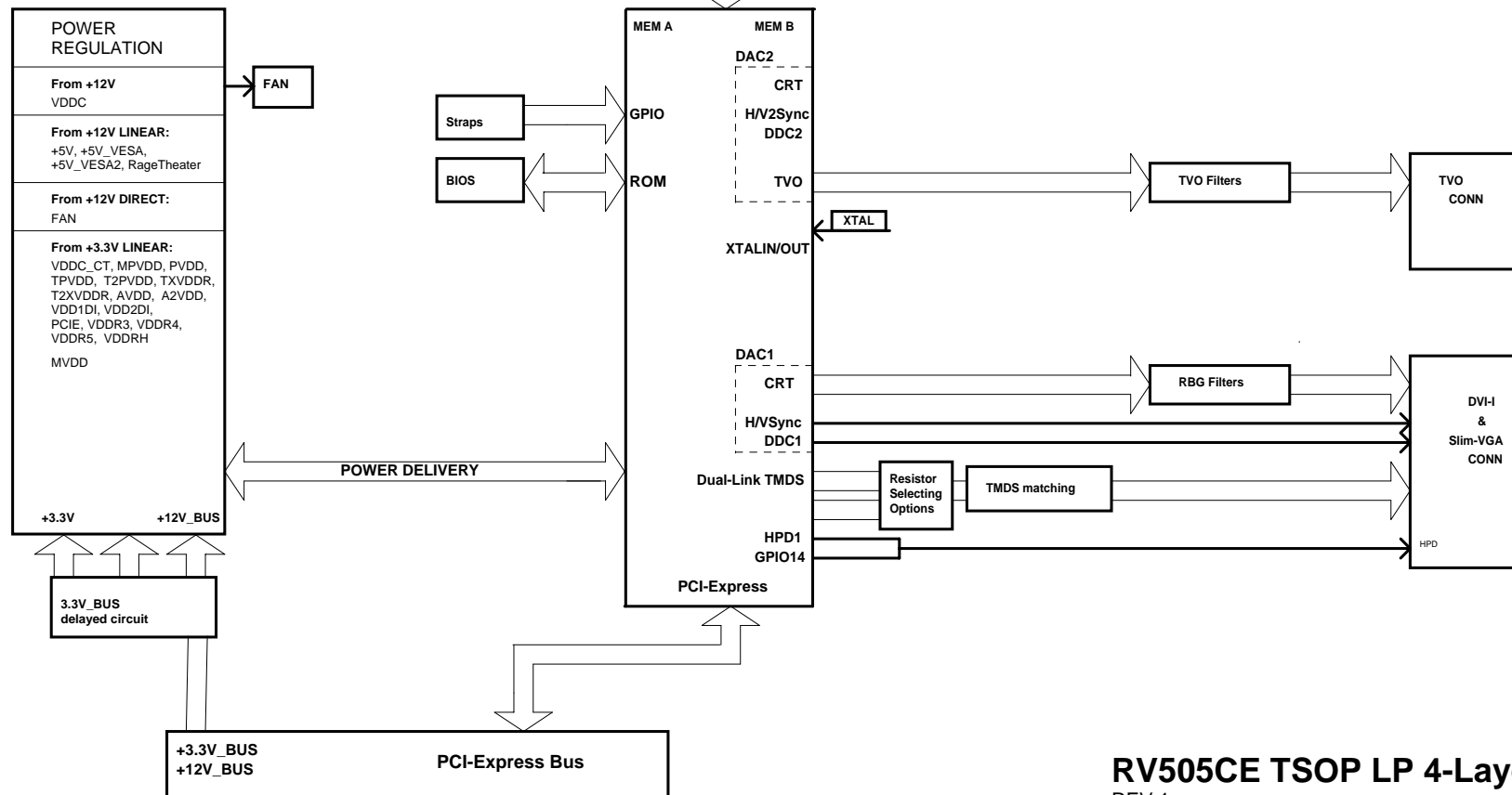
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RV505CE

MEMORY CHANNEL A

DDR2 16M/32Mx16




RV505CE TSOP LP 4-Layer
REV 1



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REVISION HISTORY							Rev 0	
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION					
0	00A	12/5/2005	LP design based on LP A857. Changed memory using latest interface from A676-10 Design. Changed memory Bank Addressing, for RV505 CE compliance Remove TMD52 and Dual Link Support. This avoids Shunt resistors for muxing TMD5 transmitters.					



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