

# P361 A00 Base Design

P361-A00, G92, 8Mx32/16Mx32 GDDR3  
DVI-I-DL, DVI-I-DL

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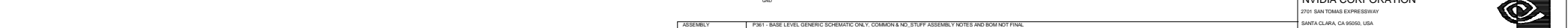
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MSIS-RMA  
羅覓林  
20091215

REV	VARIANT	NUPN	ASSEMBLY
0	BASE	600-10361-base-000	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU001	600-10361-0001-000	P361 G92-280B1 1024MB GDDR3 16Mx32 DVI-I+DVI-I
2	SKU002	600-10361-0002-000	P361 G92-280B1 512MB GDDR3 16Mx32 DVI-I+DVI-I
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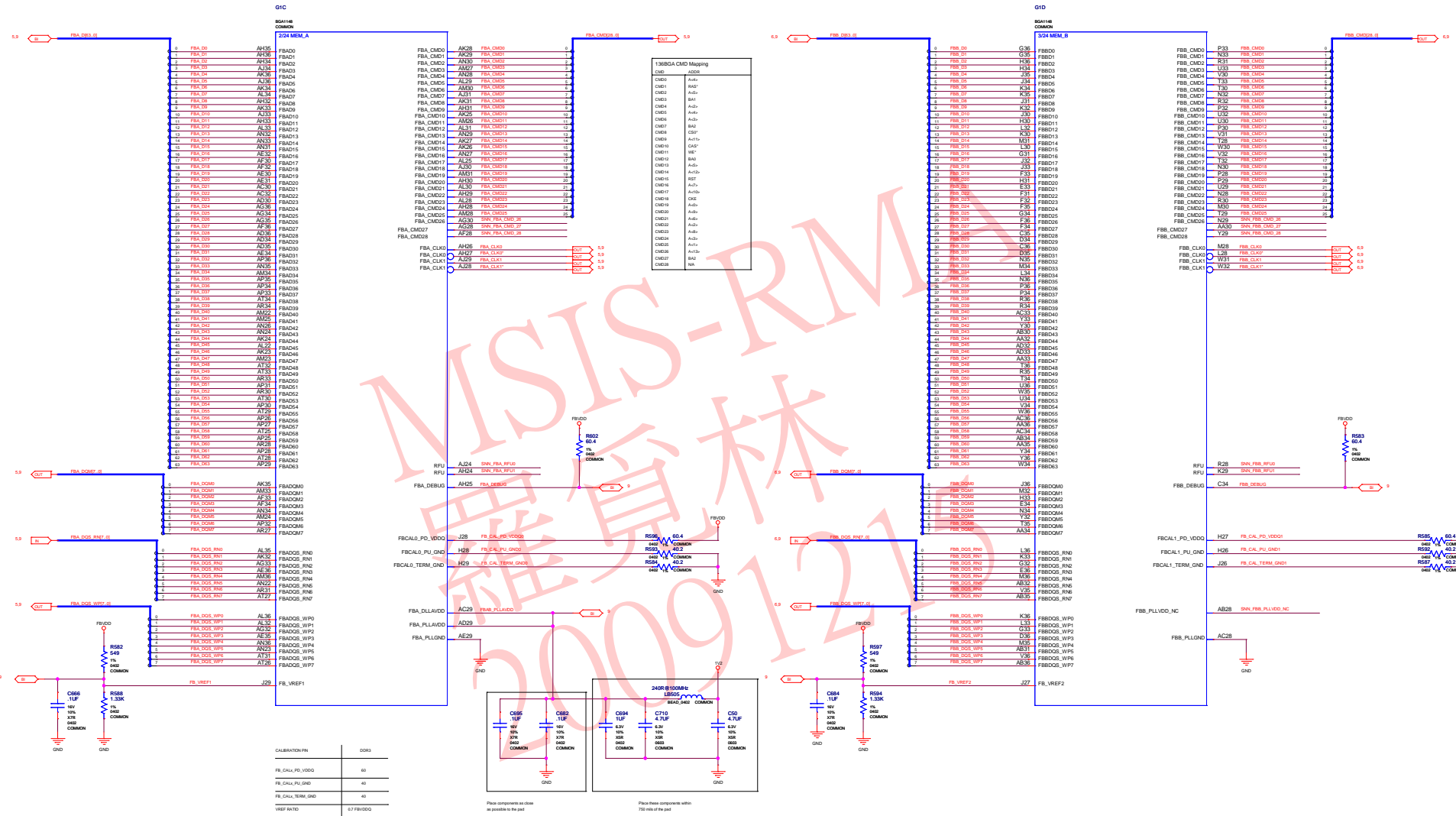
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PAGE DETAIL	PCI Express 1.0



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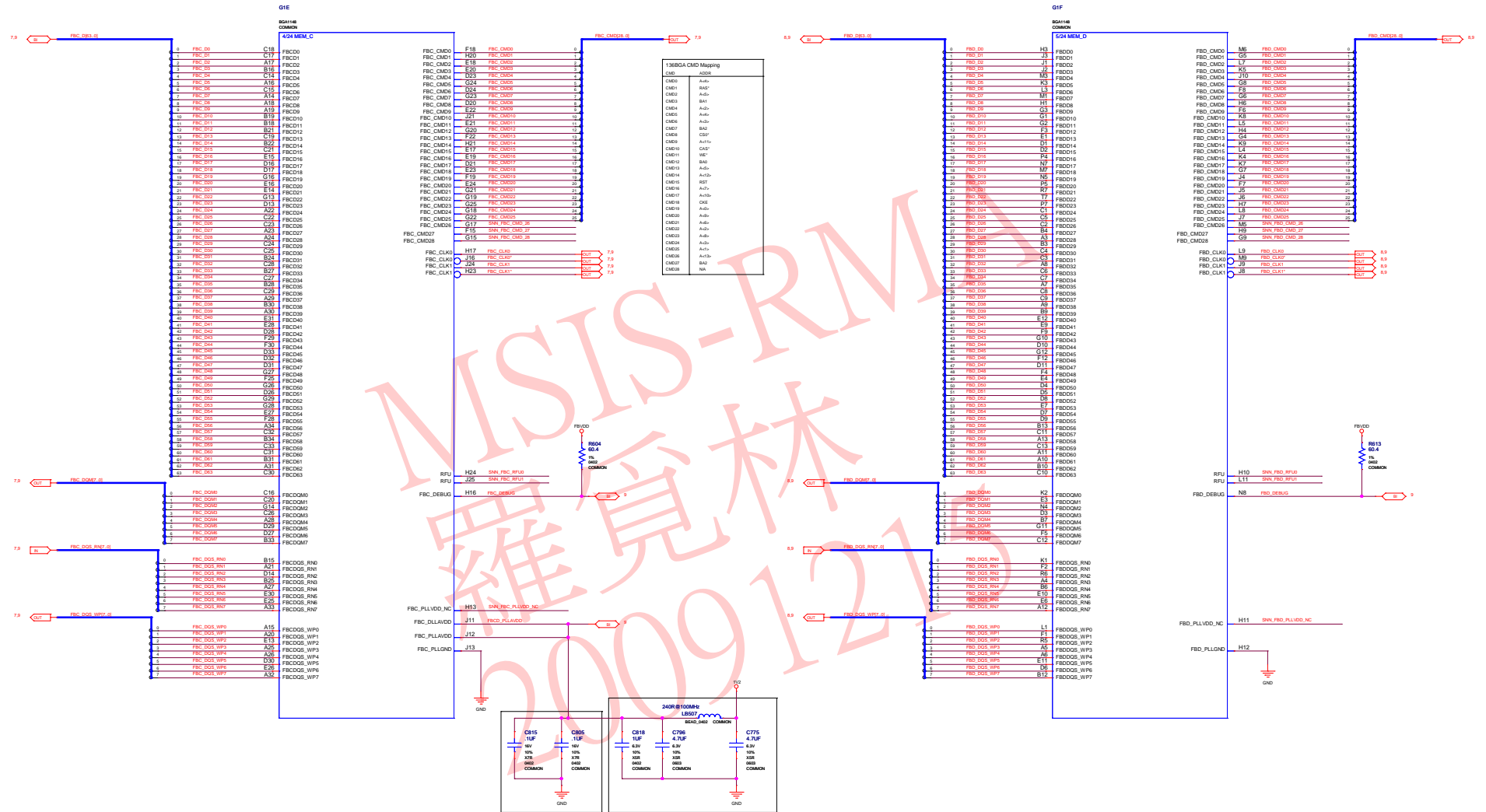
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PAGE DETAIL: MEMORY: GPU Partition A/B

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Place components as close

Place these components within  
750 mils of the pad

ASSEMBLY	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: GPU Partition C/D

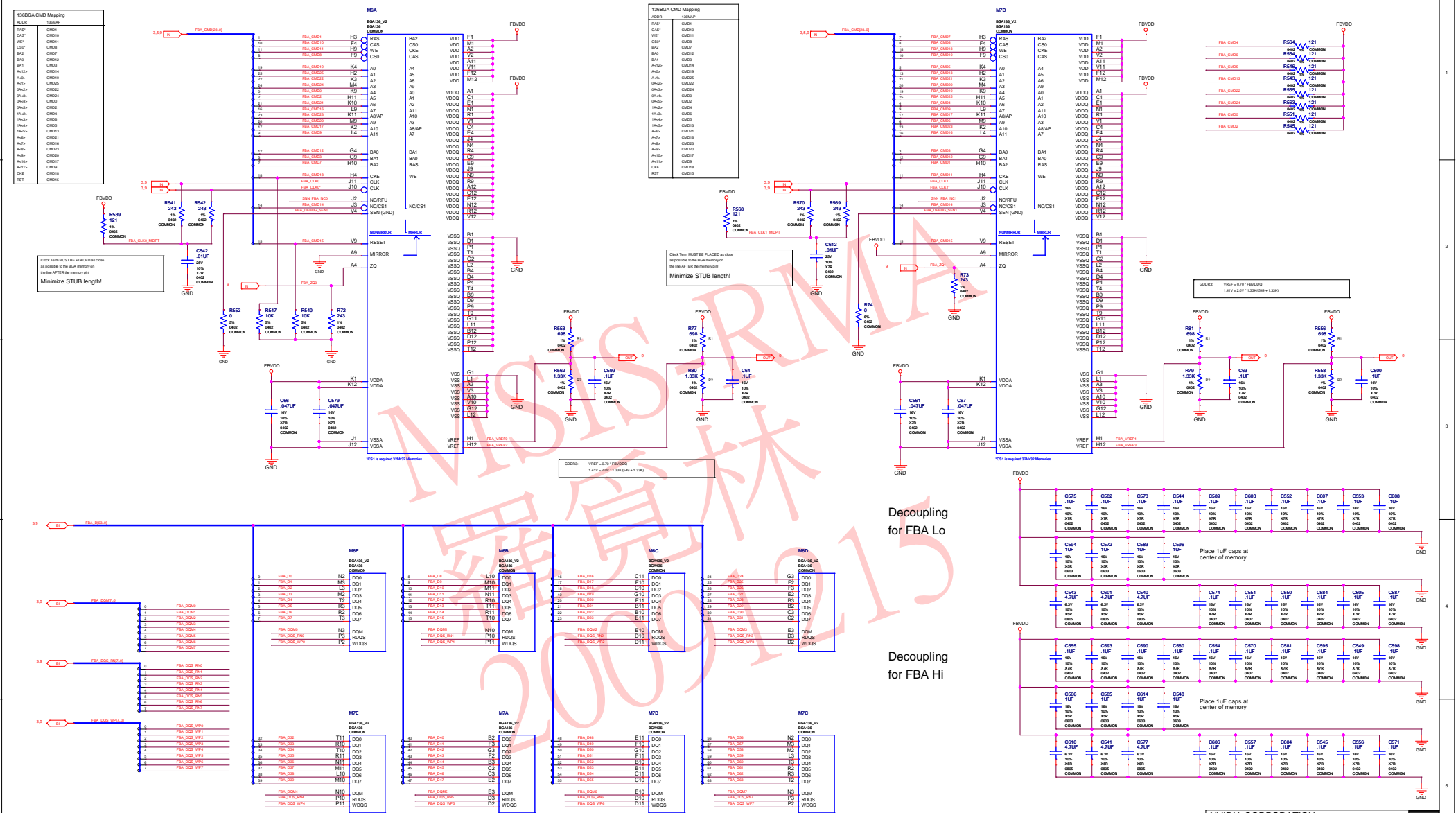
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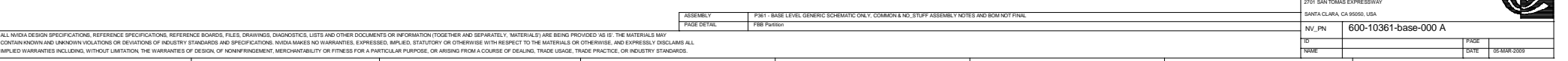
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138BGA CMD Mapping	138MAP
BA0P	CM01
BA0F	CM10
BA0E	CM11
BA0D	CM04
BA0C	CM07
BA0B	CM02
BA0A	CM03
Au0A	CM04
Au0B	CM05
Au0C	CM06
Au0D	CM07
Au0E	CM08
Au0F	CM09
Au0G	CM10
Au0H	CM11
Au0I	CM12
Au0J	CM13
Au0K	CM14
Au0L	CM15
Au0M	CM16
Au0N	CM17
Au0O	CM18
BA0P	CM01
BA0F	CM10

138BGA CMD Mapping	138MAP
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Au0B	CM05
Au0C	CM06
Au0D	CM07
Au0E	CM08
Au0F	CM09
Au0G	CM10
Au0H	CM11
Au0I	CM12
Au0J	CM13
Au0K	CM14
Au0L	CM15
Au0M	CM16
Au0N	CM17
Au0O	CM18
BA0P	CM01
BA0F	CM10

Close Term MUST BE PLACED as close as possible to the BGA memory pin  
Minimize STUB length!

Close Term MUST BE PLACED as close as possible to the BGA memory pin  
Minimize STUB length!

C31 is required 25000 Mhz

C31 is required 25000 Mhz

Decoupling for FBD Lo

Decoupling for FBD Hi

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FBD Partition

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## NET RULES for FrameBuffer A/B

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
3.5	OUT → FBA_CLK0	1	NOFF	FBA_CLK0
3.5	OUT → FBA_CLK0*	1	NOFF	FBA_CLK0
3.5	OUT → FBA_CLK1	1	NOFF	FBA_CLK1
3.5	OUT → FBA_CLK1*	1	NOFF	FBA_CLK1

Port	Signal	Direction	Device
3.5	FBA_CMC08_05	1	ACQM
3.5	FBA_C05_WF07_05	1	ACQM
3.5	FBA_C05_RN07_05	1	ACQM
3.5	FBA_C0M07_05	1	ACQM
3.5	FBA_C003_05	1	ACQM

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
3.6	OUT → FBS_CLK0	1	ROFF	FBS_CLK0
3.6	OUT → FBS_CLK0*	1	ROFF	FBS_CLK0
3.6	OUT → FBS_CLK1	1	ROFF	FBS_CLK1
3.6	OUT → FBS_CLK1*	1	ROFF	FBS_CLK1

Signal	Direction	Component	Frequency
3.6	OUT	F8B_D0D06_0	1
3.6	OUT	F8B_D0D_0007_0	1
3.6	OUT	F8B_D0D_0007_0	1
3.6	IN	F8B_D0D_0007_0	1
3.6	OUT	F8B_D0D07_0	1
3.6	IN	F8B_D0D_0	1
3	IN	F8A_DEBUG	1
3	IN	F8B_DEBUG	1

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH		
3	5V	FMSB_PLLA/CO	1.2V	0.02A	120MIL

Symbol	Parameter	Value	Unit	Min	Max
5	FBA_VREF0	1.60V	0.02%	120mV	
	FBA_VREF1	1.60V	0.02%	120mV	
5	FBA_VREF2	1.60V	0.02%	120mV	
	FBA_VREF3	1.60V	0.02%	120mV	

S	Bi	FSB_201	201	0.02A	0.02B
S	Bi		201	0.02A	0.02B

6	BI	FBS_VREF0	1.65V	0.02%	1250K
6	BI	FBS_VREF1	1.65V	0.02%	1250K
6	BI	FBS_VREF2	1.65V	0.02%	1250K
6	BI	FBS_VREF3	1.65V	0.02%	1250K

6	Id	F8B_Z01	2.0V	0.02s	128Hz
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3	B1	FD_VREF1	1.40V	0.02A	120mW
	B1	FD_VREF2	1.40V	0.02A	120mW

Note: FB traces on top and bottom layers are routed with 45ohm impedance for increasing spacing.  
Internal FB traces are routed with 40ohm impedance.

## NET RULES for FrameBuffer C/D

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
4.7	OUT → FBC_CLK0	1	NODEF	FBC_CLK0
4.7	OUT → FBC_CLK0*	1	NODEF	FBC_CLK0
4.7	OUT → FBC_CLK1	1	NODEF	FBC_CLK1
4.7	OUT → FBC_CLK1*	1	NODEF	FBC_CLK1

4.7	OUT	FBC DMS2R.G	1	000M
4.7	OUT	FBC D25.WP7.G	1	000M
4.7	IN	FBC D25.WP7.G	1	000M
4.7	OUT	FBC D2M7.G	1	000M
4.7	IN	FBC D2M7.G	1	000M

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
4.8	OUT FWD_CLK0	1	800FF	FWD_CLK0
4.8	OUT FWD_CLK0*	1	800FF	FWD_CLK0
4.8	OUT FWD_CLK1	1	800FF	FWD_CLK1
4.8	OUT FWD_CLK1*	1	800FF	FWD_CLK1

Signal	Pin	Function	Level
OUT	FB0-00020A-B	1	400mV
OUT	FB0-00040B-B	1	400mV
IN	FB0-0001-B	1	400mV
OUT	FB0-0007-B	1	400mV
IN	FB0-000A-B	1	400mV
IN	FB0-000B-B	1	400mV
IN	FB0-000C-B	1	400mV
IN	FB0-000D-B	1	400mV

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FPCD_PILA00	1.2V	0.02A	12MIL

7	IN	FBC_VREF0	1.40V	0.02A	128Hz
7	IN	FBC_VREF1	1.40V	0.02A	128Hz
7	IN	FBC_VREF2	1.40V	0.02A	128Hz
7	IN	FBC_VREF3	1.40V	0.02A	128Hz

Item	Value	Unit	Value	Unit
1	200	200	0.020	0.020
2	200	200	0.020	0.020

Pin	Symbol	Function	Level	Current	Power
1	FB	FB0_VREF	1.60V	0.02A	32mW
2	FB	FB0_VREF1	1.60V	0.02A	32mW
3	FB	FB0_VREF2	1.60V	0.02A	32mW
4	FB	FB0_VREF3	1.60V	0.02A	32mW

1. **Introduction**



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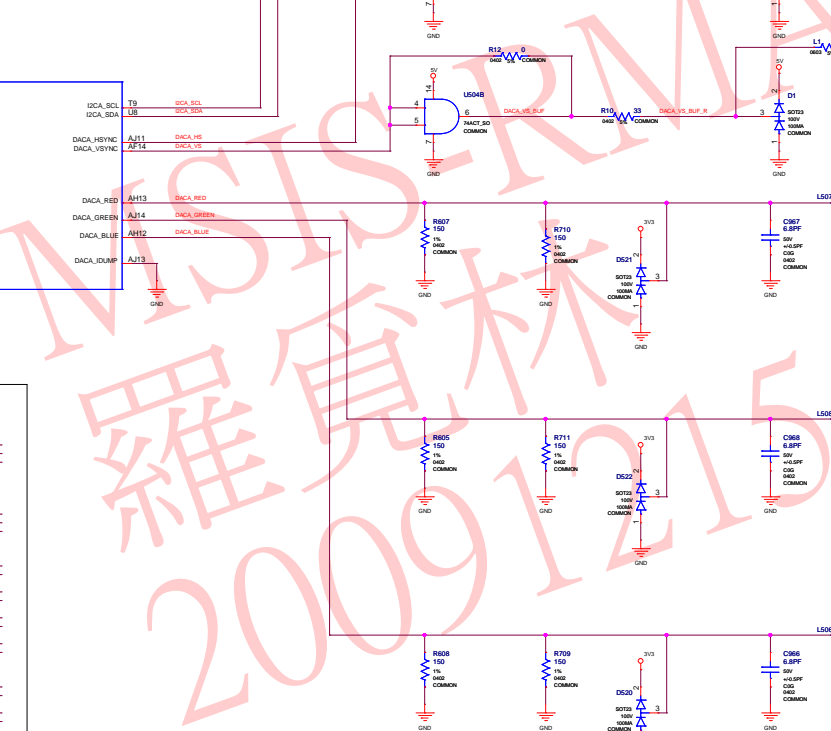
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DACA NET RULES

NET		NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
R	DACA_RED	1	75OHM	
R	DACA_GREEN	1	75OHM	
R	DACA_BLUE	1	75OHM	
10.12	DACA_RED_DV	1	75OHM	
10.12	DACA_GREEN_DV	1	75OHM	
10.12	DACA_BLUE_DV	1	75OHM	
R	DACA_HS	2	50OHM	
R	DACA_VS	2	50OHM	
R	DACA_HS_BUF	2	50OHM	
R	DACA_VS_BUF	2	50OHM	
R	DACA_HS_BUF_B	2	50OHM	
R	DACA_VS_BUF_B	2	50OHM	
10.12	DACA_HS_DV	2	50OHM	
10.12	DACA_VS_DV	2	50OHM	
R	DACA_SCL	3	50OHM	
R	DACA_SDA	3	50OHM	
R	DACA_SCL_B	3	50OHM	
R	DACA_SDA_B	3	50OHM	
10.12	DACA_SCL_DV	3	50OHM	
10.12	DACA_SDA_DV	3	50OHM	
NET		VOLTAGE	MAX_CURRENT	MIN_WIDTH
R	DACA_VREF	3.3V	1.00A	198ML
R	DACA_VREF	3.3V	1.00A	198ML
R	DACA_VREF	3.3V	1.00A	198ML

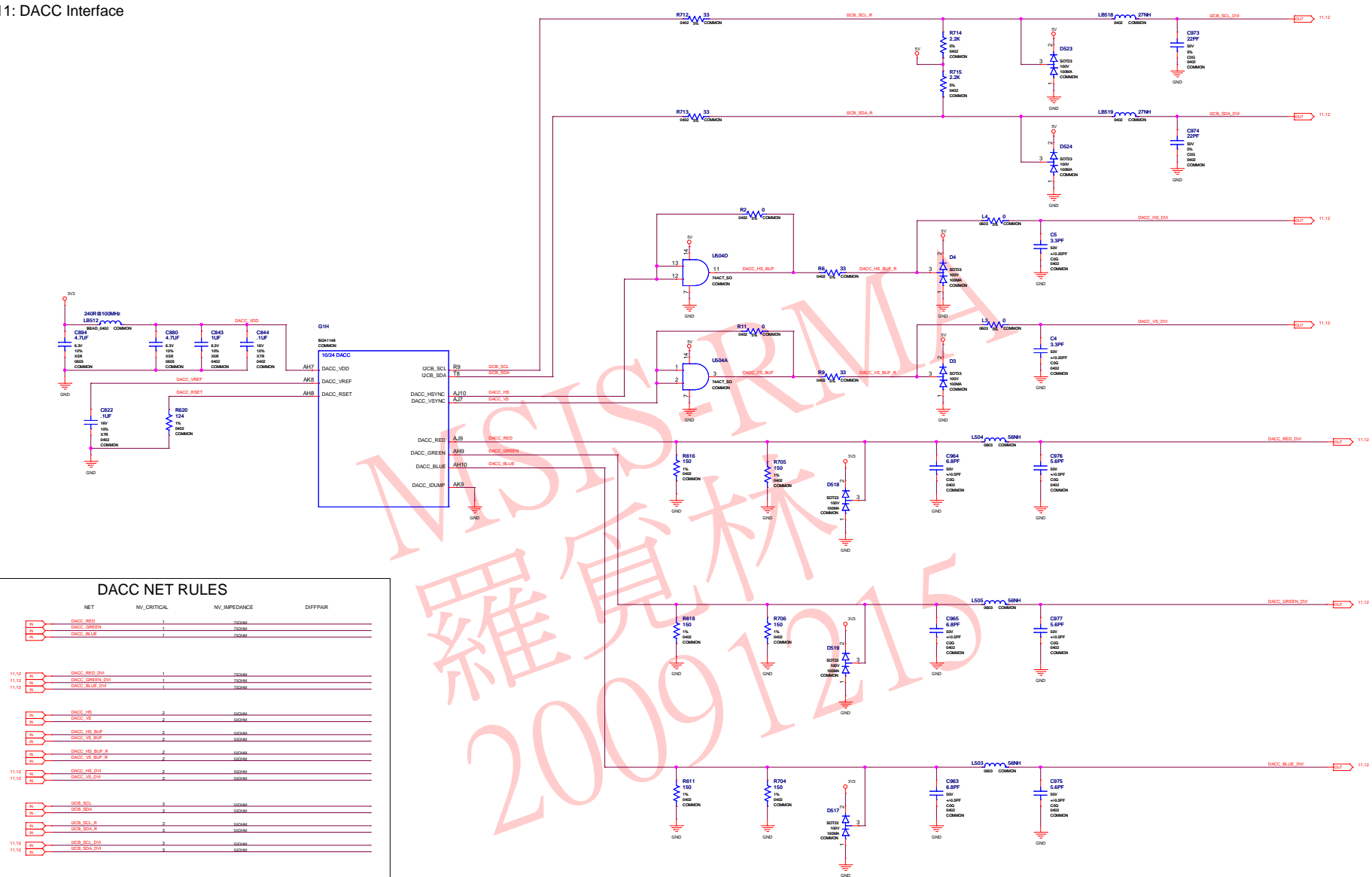


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PAGE DETAIL	DACA Interface

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## DACC NET RULES

	NET	NV_CRITICAL	NV_IMPEDIANCE	DIFF_PAIR
B	DACC_RED	1	100Ω	
B	DACC_GREEN	1	100Ω	
B	DACC_BLUE	1	100Ω	
11,12	DACC_RED_DN	1	100Ω	
11,12	DACC_GREEN_DN	1	100Ω	
11,12	DACC_BLUE_DN	1	100Ω	
B	DACC_HS	2	100Ω	
B	DACC_LS	2	100Ω	
B	DACC_HS_BUF	2	100Ω	
B	DACC_LS_BUF	2	100Ω	
B	DACC_HS_BUF_P	2	100Ω	
B	DACC_LS_BUF_P	2	100Ω	
11,12	DACC_HS_DN	2	100Ω	
11,12	DACC_LS_DN	2	100Ω	
B	DCB_SCL	3	100Ω	
B	DCB_SDA	3	100Ω	
B	DCB_SCL_P	3	100Ω	
B	DCB_SDA_P	3	100Ω	
11,12	DCB_SCL_DN	3	100Ω	
11,12	DCB_SDA_DN	3	100Ω	
	NET	VOLTAGE	MAX_CURRENT	MIN_LENGTH
B	DACC_AREF			1200L
B	DACC_RESET			1200L
B	DACC_D0	3.3V	0.100A	1000L

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PAGE DETAIL	DACC Interface

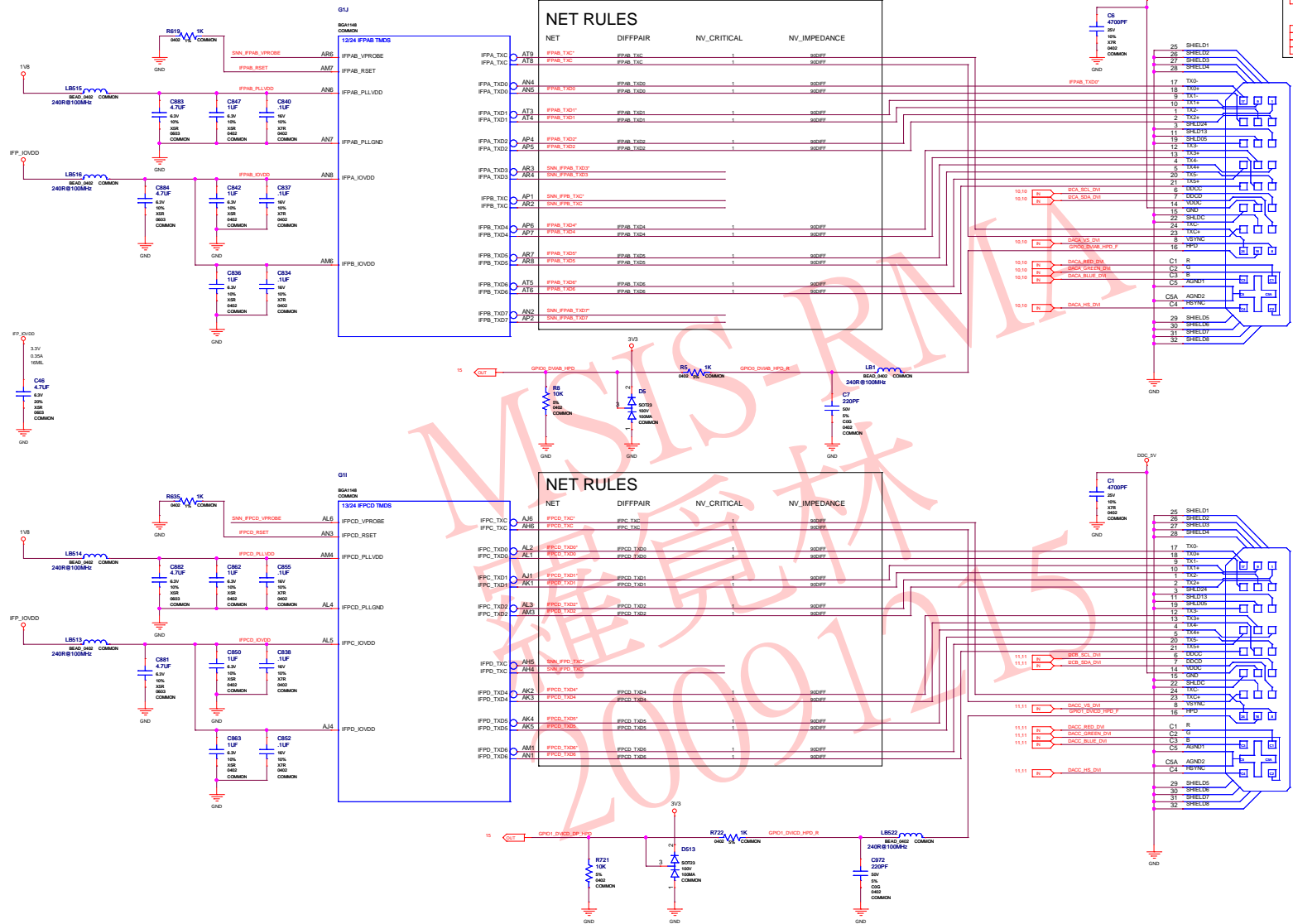
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## IFPABCD NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RESET			120Ω
IFPAB_RESET			120Ω
IFPAB_DIN0_VPD_0	3	50ΩCM	
IFPAB_DIN0_VPD_0	3	50ΩCM	
IFPAB_DIN0_VPD_0	3	50ΩCM	
IFPAB_DIN0_VPD_0	3	50ΩCM	
IFPAB_DIN0_VPD_0	3	50ΩCM	
IFPAB_DIN0_VPD_0	3	50ΩCM	
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLVDD0	1.6V	0.05A	100MIL
IFPAB_VDD0	3.3V	0.05A	100MIL
IFPAB_PLVDD0	1.6V	0.05A	100MIL
IFPAB_VDD0	3.3V	0.05A	100MIL

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# NET RULES

NET	DIFFPAIR	NV_CRITICAL	NV_IMPACTANCE
FFCD_T1C1	FFCD_T1C2	1	300F
FFCD_T1C2	FFCD_T1C3	1	300F
FFCD_T1C3	FFCD_T1C4	1	300F
FFCD_T1C4	FFCD_T1C5	1	300F
FFCD_T1C5	FFCD_T1C6	1	300F
FFCD_T1C6	FFCD_T1C7	1	300F
FFCD_T1C7	FFCD_T1C8	1	300F
FFCD_T1C8	FFCD_T1C9	1	300F
FFCD_T1C9	FFCD_T1C10	1	300F
FFCD_T1C10	FFCD_T1C11	1	300F
FFCD_T1C11	FFCD_T1C12	1	300F
FFCD_T1C12	FFCD_T1C13	1	300F
FFCD_T1C13	FFCD_T1C14	1	300F
FFCD_T1C14	FFCD_T1C15	1	300F
FFCD_T1C15	FFCD_T1C16	1	300F
FFCD_T1C16	FFCD_T1C17	1	300F
FFCD_T1C17	FFCD_T1C18	1	300F
FFCD_T1C18	FFCD_T1C19	1	300F
FFCD_T1C19	FFCD_T1C20	1	300F
FFCD_T1C20	FFCD_T1C21	1	300F
FFCD_T1C21	FFCD_T1C22	1	300F
FFCD_T1C22	FFCD_T1C23	1	300F
FFCD_T1C23	FFCD_T1C24	1	300F
FFCD_T1C24	FFCD_T1C25	1	300F
FFCD_T1C25	FFCD_T1C26	1	300F
FFCD_T1C26	FFCD_T1C27	1	300F
FFCD_T1C27	FFCD_T1C28	1	300F
FFCD_T1C28	FFCD_T1C29	1	300F
FFCD_T1C29	FFCD_T1C30	1	300F
FFCD_T1C30	FFCD_T1C31	1	300F
FFCD_T1C31	FFCD_T1C32	1	300F
FFCD_T1C32	FFCD_T1C33	1	300F
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FFCD_T1C35	FFCD_T1C36	1	300F
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FFCD_T1C39	FFCD_T1C40	1	300F
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FFCD_T1C44	FFCD_T1C45	1	300F
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FFCD_T1C276	FFCD_T1C277	1	300F
FFCD_T1C277	FFCD_T1C278	1	300F
FFCD_T1C278	FFCD_T1C279	1	300F
FFCD_T1C279	FFCD_T1C280	1	300F

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DB(1), COLUMN, DBA(2), IN
DB(1), COLUMN, DBA(2), IN
COMMON

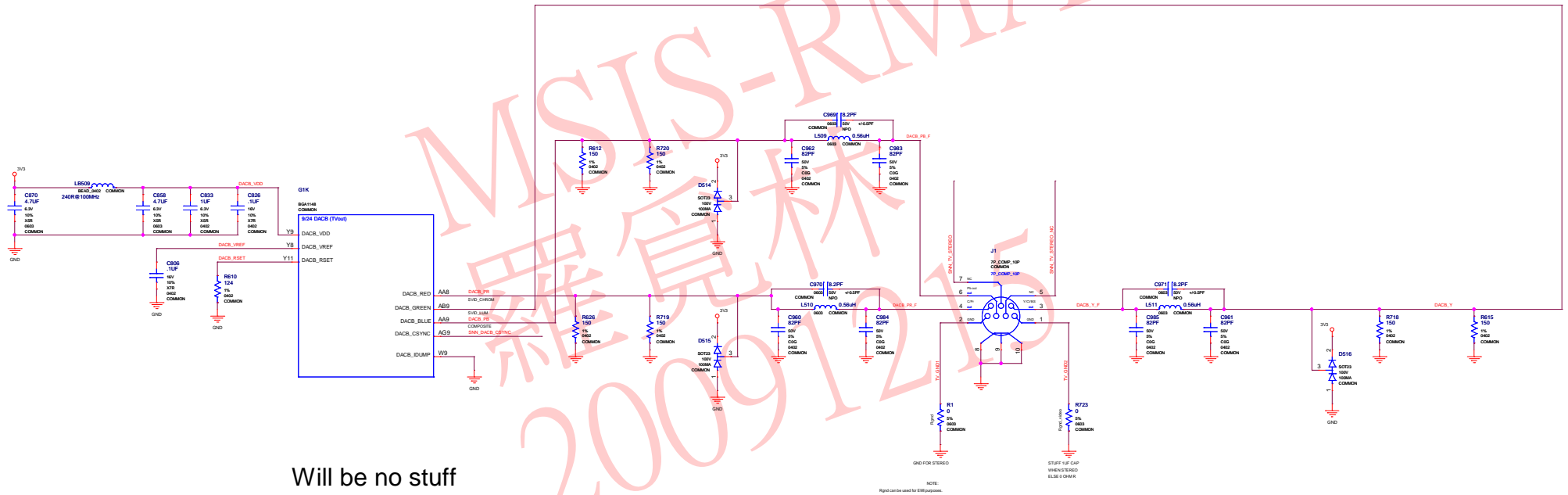
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## DACB,STEREO, FL NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
8a	DACS_PB	1	750Ω	
8b	DACS_Y	1	750Ω	
8c	DACS_PB	1	750Ω	
9a	DACS_PB_P	1	750Ω	
9b	DACS_Y_P	1	750Ω	
9c	DACS_PB_P	1	750Ω	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
16	TV_GND1	0.0V		12MIL
70	TV_GND2	0V		12MIL
16	DACB_VDD	3.3V	0.2A	12MIL
91	DACB_VREF			12MIL
80	DACB_RESET			12MIL



Will be no stuff

NOTE:  
Rgnd can be used for EIM purposes

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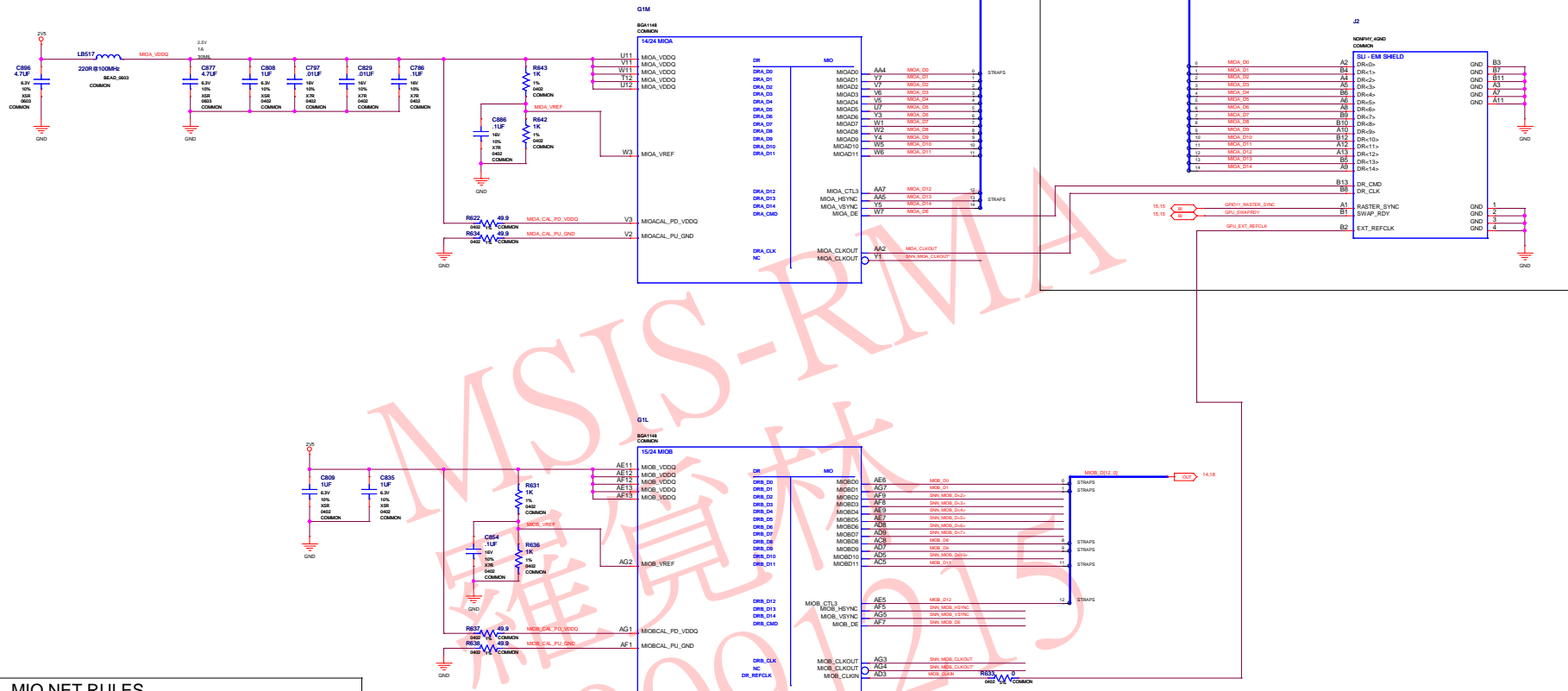
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## MIO Feature Connector



## MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
MIOA_MIOA_05	1	100OHM	
MIOA_MIOA_06	1	100OHM	
MIOA_MIOA_07	1	100OHM	
MIOB_MIOB_05	1	100OHM	
MIOB_MIOB_06	1	100OHM	
MIOB_MIOB_07	1	100OHM	
MIOB_MIOB_08	1	100OHM	
MIOB_MIOB_09	1	100OHM	
MIOB_MIOB_10	1	100OHM	
MIOB_MIOB_11	1	100OHM	
MIOB_MIOB_12	1	100OHM	
MIOB_MIOB_13	1	100OHM	
MIOB_MIOB_14	1	100OHM	
MIOB_MIOB_15	1	100OHM	
MIOB_MIOB_16	1	100OHM	
MIOB_MIOB_17	1	100OHM	
MIOB_MIOB_18	1	100OHM	
MIOB_MIOB_19	1	100OHM	
MIOB_MIOB_20	1	100OHM	
MIOB_MIOB_21	1	100OHM	
MIOB_MIOB_22	1	100OHM	
MIOB_MIOB_23	1	100OHM	
MIOB_MIOB_24	1	100OHM	
MIOB_MIOB_25	1	100OHM	
MIOB_MIOB_26	1	100OHM	
MIOB_MIOB_27	1	100OHM	
MIOB_MIOB_28	1	100OHM	
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MIOB_MIOB_31	1	100OHM	
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MIOB_MIOB_100	1	100OHM	

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ASSEMBLY: P081 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL  
PAGE DETAIL: Multi-use (MIO) Interface

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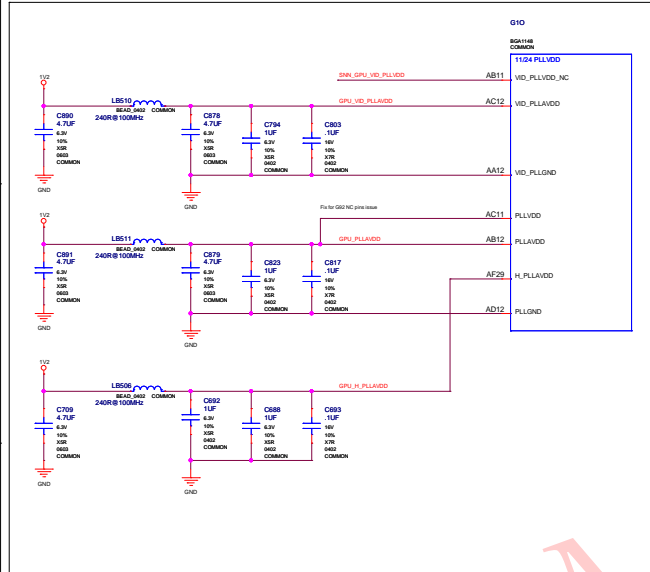


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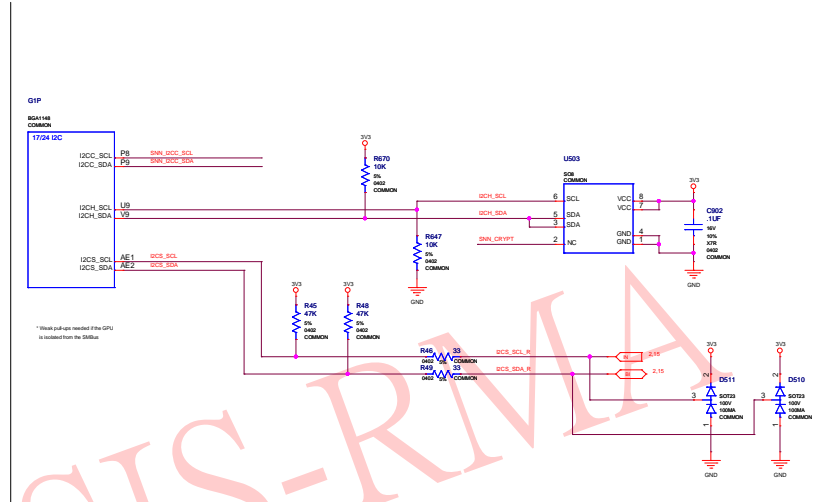
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## PLLVD/VID\_PLLVD



## I2CC / I2CH(+ HDCP ROM) / I2CS



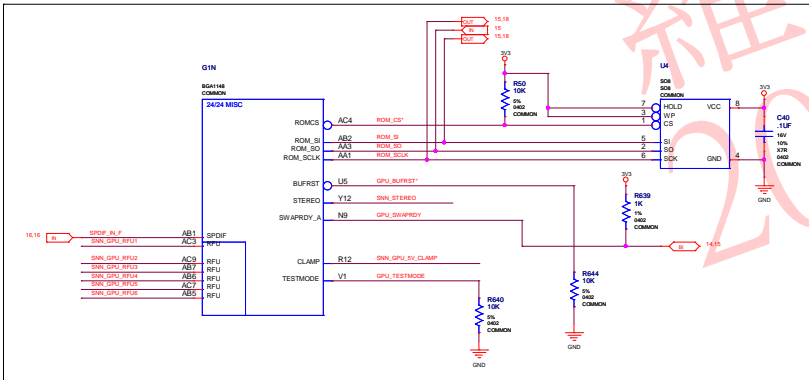
## MISC NET RULES

NET NV\_CRITICAL NV\_IMPEDANCE DIFFPAIR

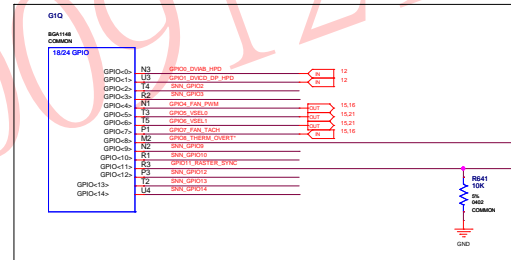
	18	DOCH_SCL	3	DOCHN	
	18	DOCH_SDA	3	DOCHN	
	18	I2CS_SCL	3	DOCHN	
	18	I2CS_SCL_N	3	DOCHN	
	18	I2CS_SDA_N	3	DOCHN	
15,15	18	DOCH_SCL_N	3	DOCHN	
	18	DOCH_SDA_N	3	DOCHN	
15,15	18	ROM_CS*	3	DOCHN	
	18	ROM_SE	3	DOCHN	
15	18	ROM_SD	3	DOCHN	
15,15	18	ROM_SCLK	3	DOCHN	
14,15	18	GPU_BURST/ GPU_TESTMODE	3	DOCHN	
	18	GPICD_DVLA_HPD	3	DOCHN	
	18	GPICD_DVLA_C_HPD	3	DOCHN	
15,15	18	GPICD_FAN_PWM	3	DOCHN	
15,21	18	GPICD_VSEL1	3	DOCHN	
15,21	18	GPICD_VSEL2	3	DOCHN	
15,15	18	GPICD_FAN_TACH	3	DOCHN	
15,15	18	GPICD_THERM_OVER*	3	DOCHN	
14,15	18	GPICD1_MASTER_SYNC	3	DOCHN	
	18	XTAL_SDN	1	DOCHN	
	18	XTAL_N	1	DOCHN	
	18	XTAL_OUT1	1	DOCHN	
	18	XTAL_OUTBUFF	1	DOCHN	
		NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
	18	GPU_VB_PLLVD	1.2V	0.05A	120uM
	18	GPU_VB_PLLVD	1.2V	0.05A	120uM
	18	GPU_VB_PLLVD	1.2V	0.05A	120uM
	18	GPU_VB_PLLVD	1.2V	0.05A	120uM
	18	GPU_VB_PLLVD	1.2V	0.05A	120uM

## ROM / MISC

(BURST/STEREO/SWAPRDY/CLAMP/TESTMODE)

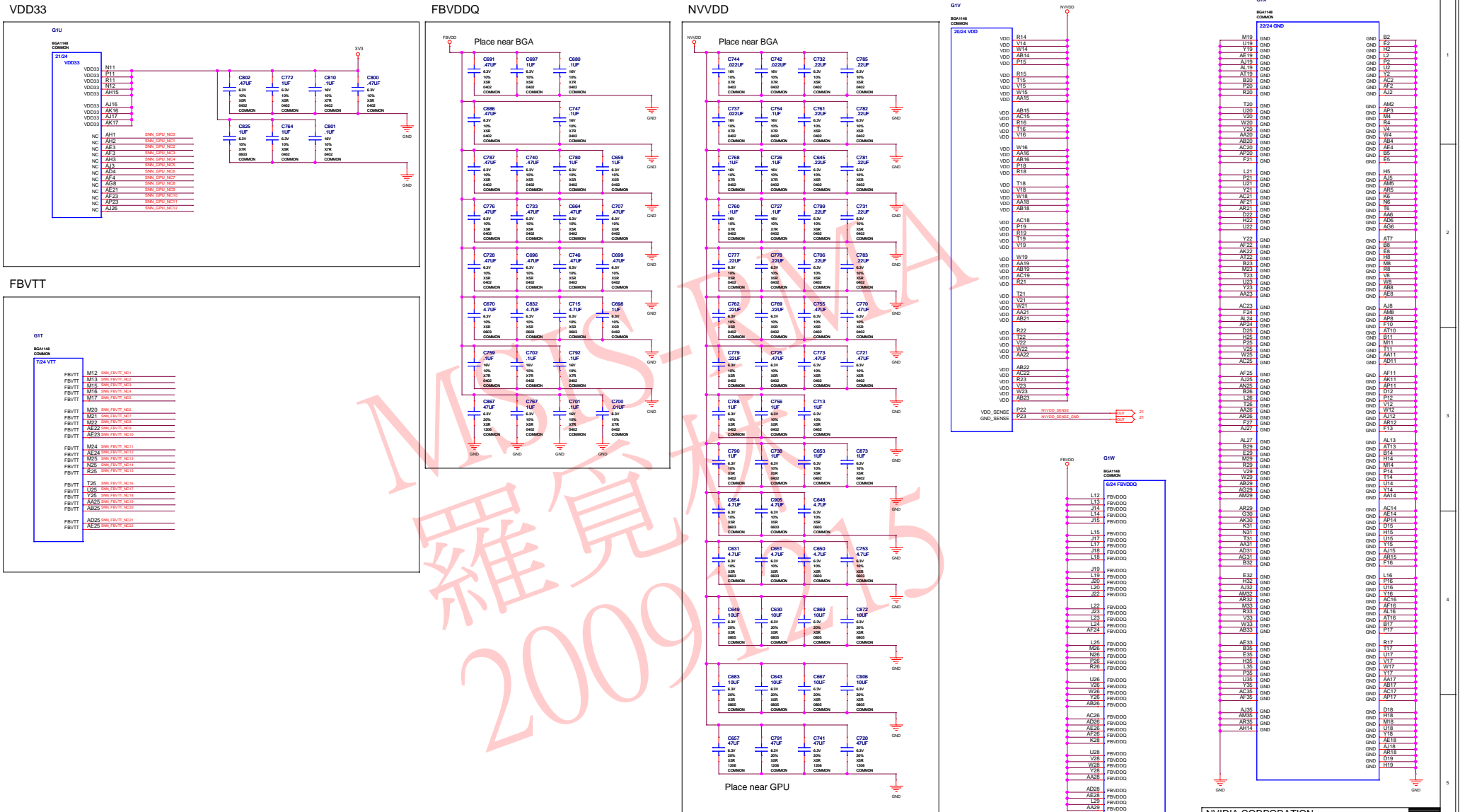


## GPIO

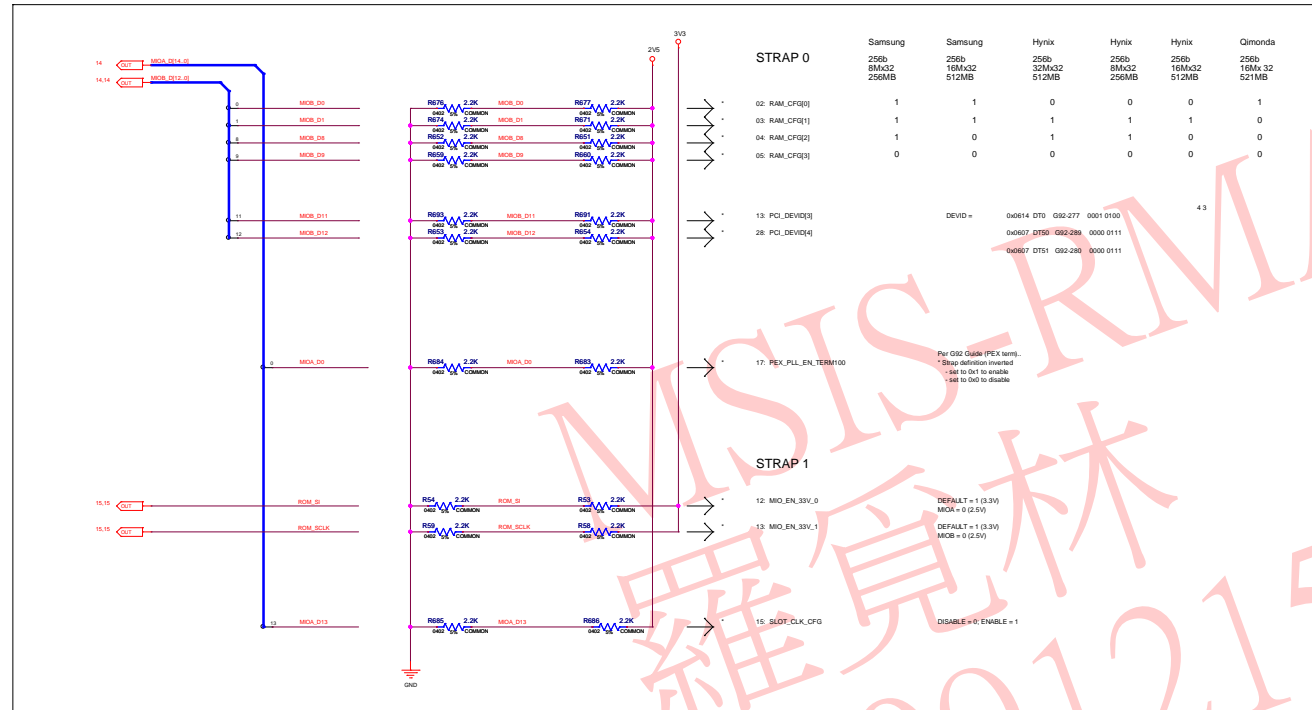




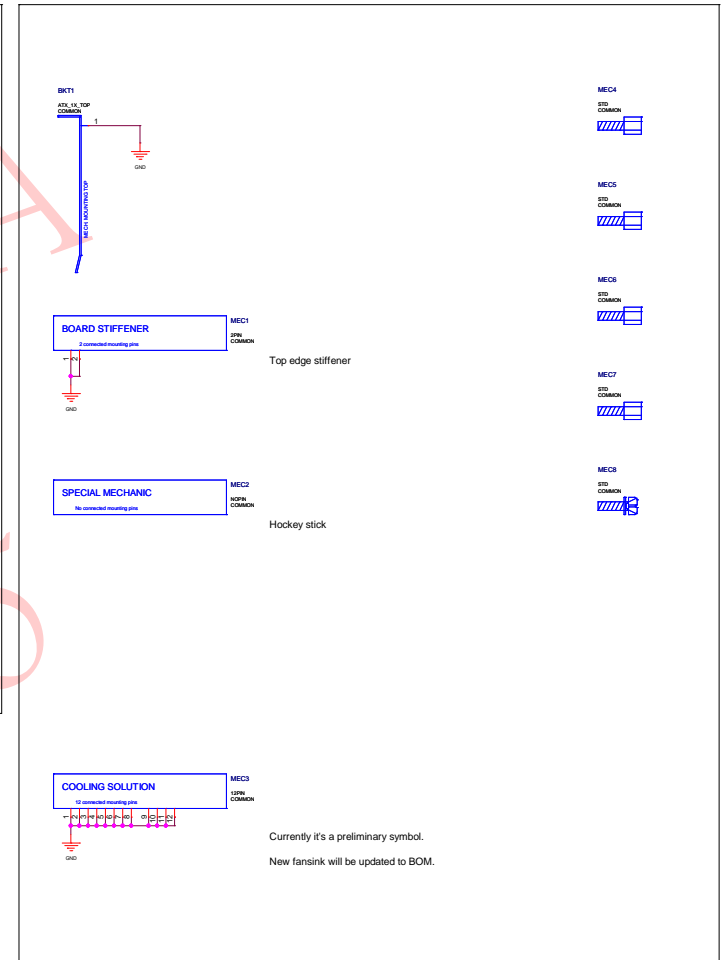




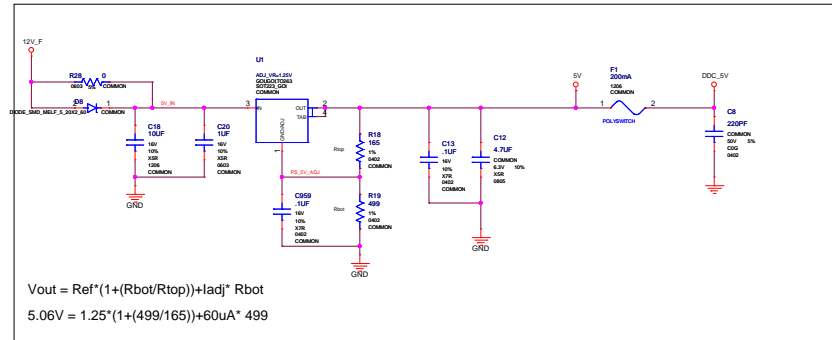
## STRAPS



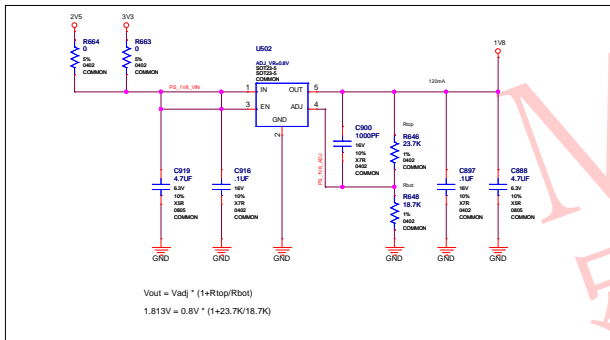
## MECHANICAL



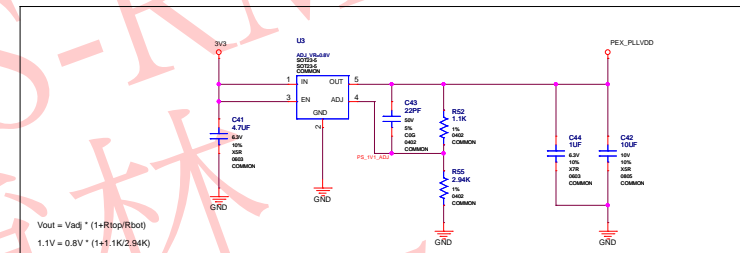
## 5V REGULATOR



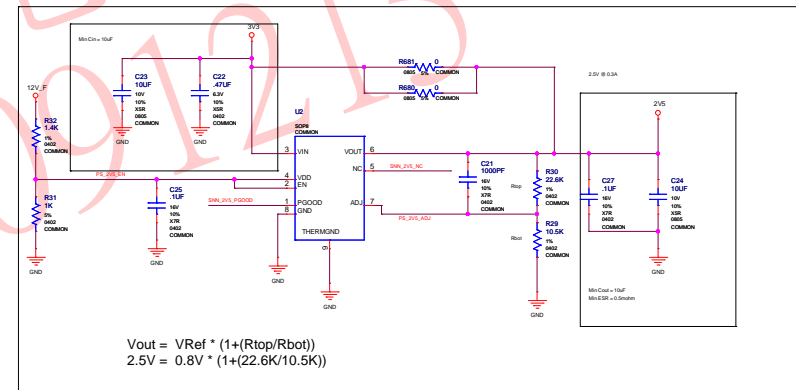
## 5V DDC



### PEX\_PLLVDD Optional

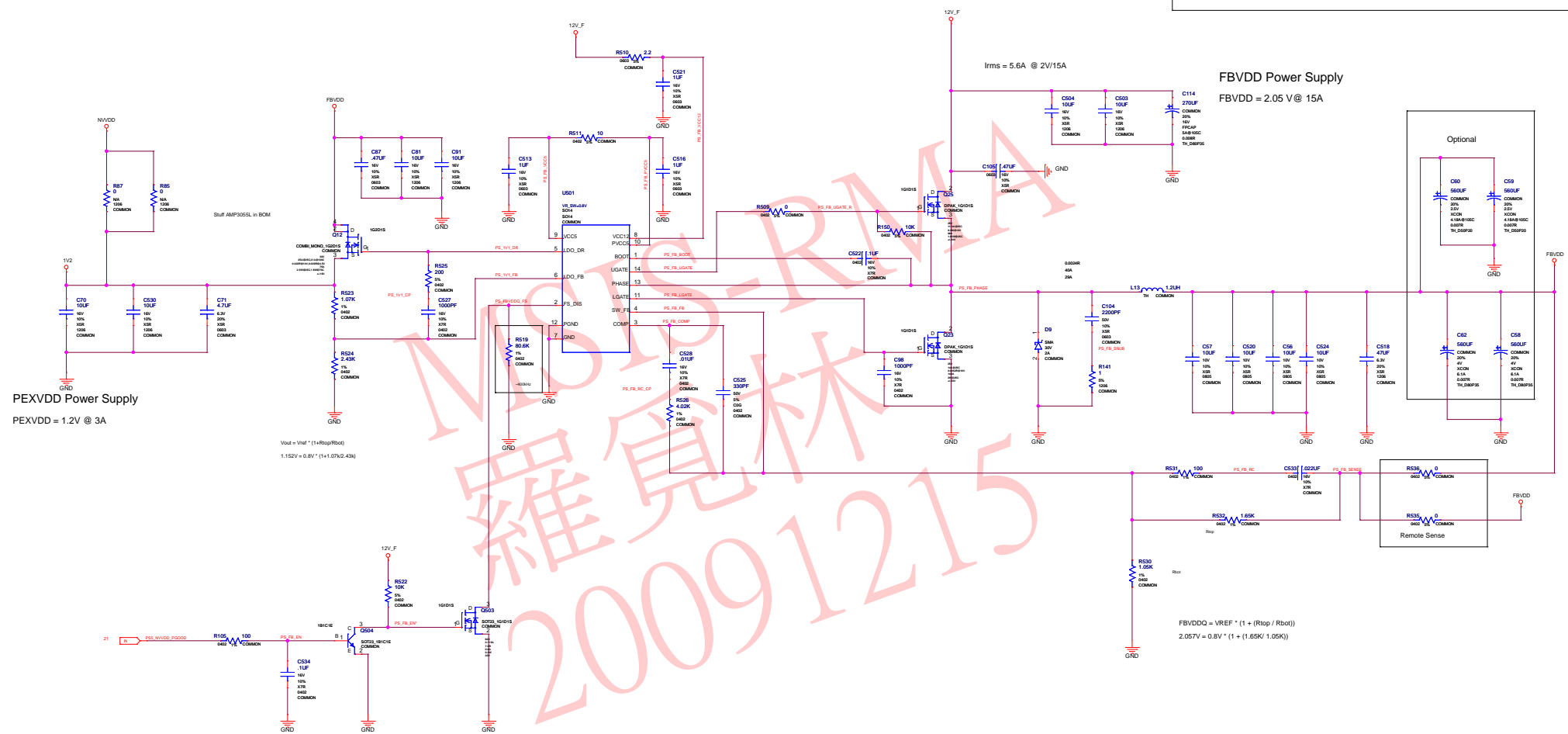


MIO\_VDD 2.5V



NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	0.14	138L	5V
5V	0.154	138L	5V
PEX_PLVDD	0.164	138L	1.0V
TVDD	0.164	138L	1.8V
2V5	0.84	138L	2.5V





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ASSEMBLY	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: FBVDD, PEXVDD

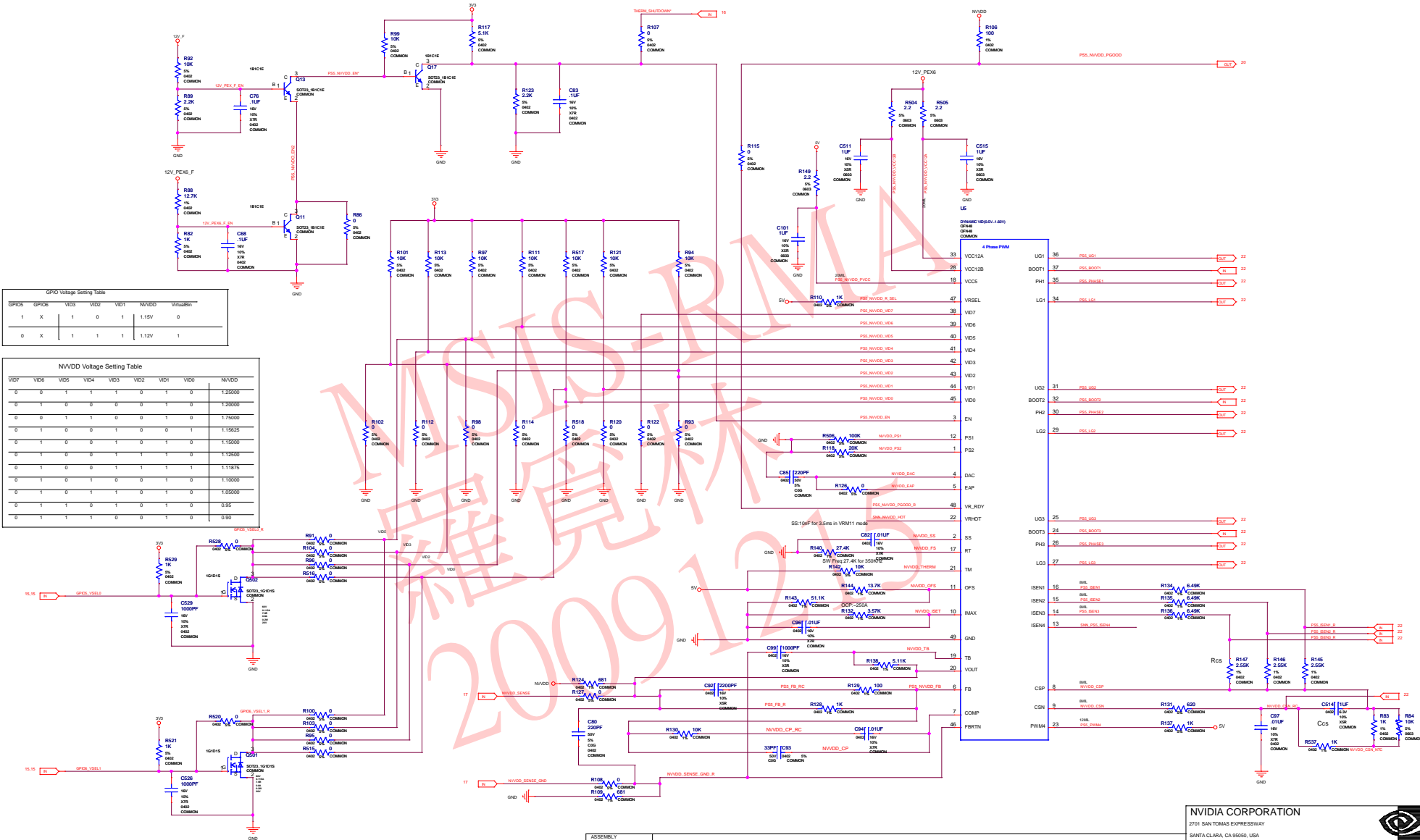
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GPVDD Voltage Setting Table						
GPVDD	GPVDD	VDD1	VDD2	VDD1	NVDD	VDD1
1	X	1	0	1	1.15V	0
0	X	1	1	1	1.12V	1

NVVDD Voltage Setting Table									
VDD1	VDD2	VDD3	VDD4	VDD5	VDD6	VDD7	VDD8	VDD9	NVDD
0	0	1	1	1	0	1	0	1	1.35000
0	1	0	0	0	0	0	1	0	1.20000
0	0	1	1	1	0	0	1	0	1.75000
0	1	0	0	1	1	0	0	1	1.15625
0	1	0	0	1	0	1	1	0	1.15000
0	1	0	0	1	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1	1.11875
0	1	0	1	1	0	1	1	0	1.10000
0	1	0	1	1	0	1	1	0	1.05000
0	1	1	0	1	0	1	0	1	0.95
0	1	1	1	0	0	1	0	1	0.90

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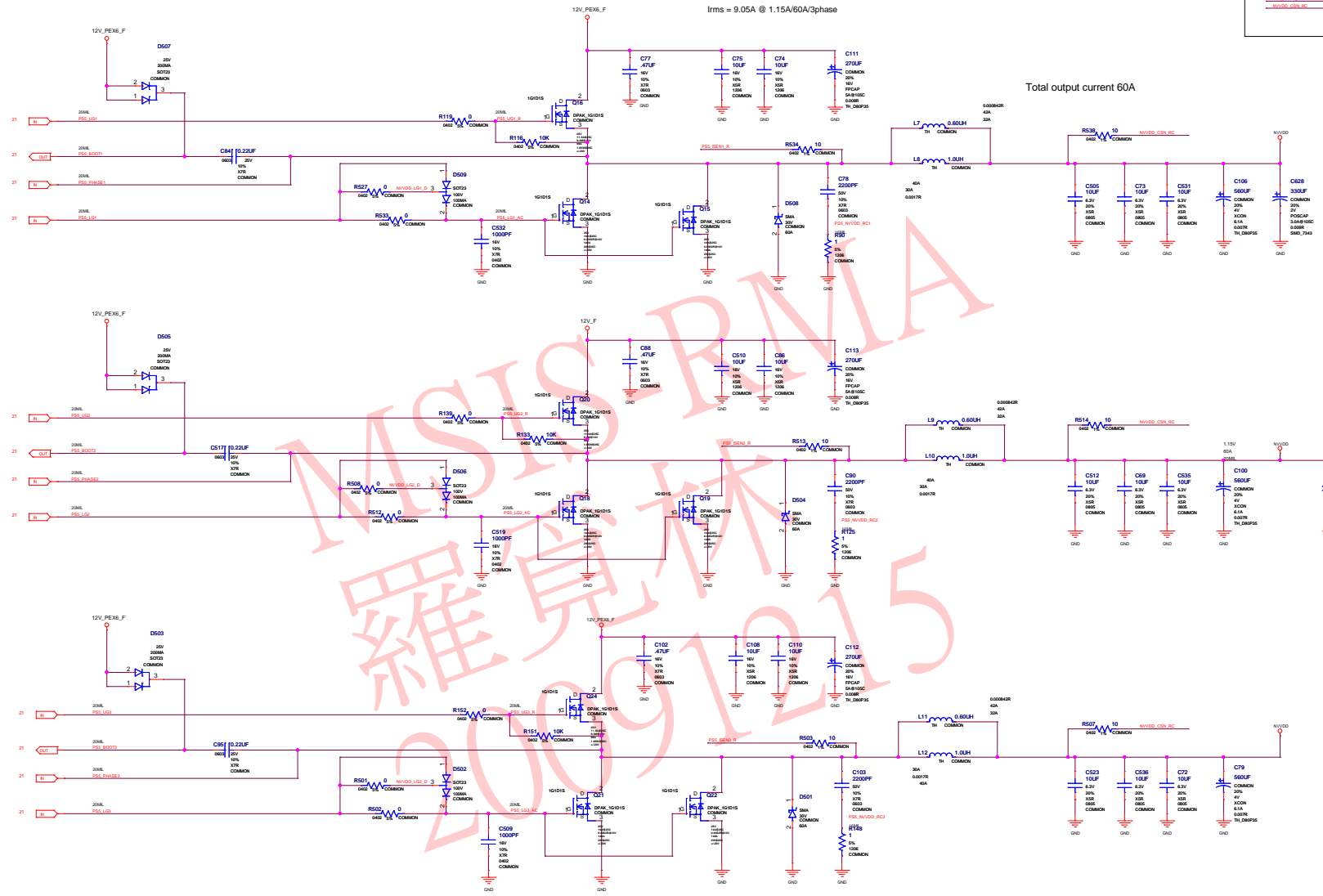
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PSL_BEN_R	0	COMMON	TH	COMMON	0.0004R	4A	3A
PSL_BEN_R	0	COMMON	TH	COMMON	0.0004R	4A	3A
PSL_BEN_R	0	COMMON	TH	COMMON	0.0004R	4A	3A
PSL_BEN_R	0	COMMON	TH	COMMON	0.0004R	4A	3A

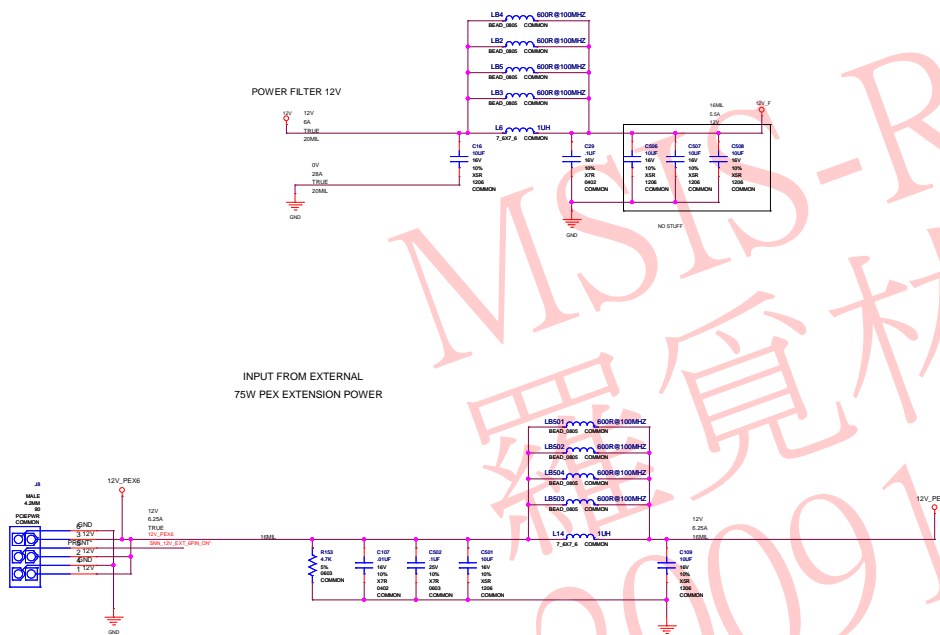
Total output current 60A

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ASSEMBLY	Power Supply: NVVDD Mosfet
PAGE DETAIL	

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ASSEMBLY	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: Filter of 3V3, 12V, 12V_PEX6

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