

P392-B01 Board

P392-B01, G92, 16Mx32 GDDR3 (1200MHz),  
DVI -I -DL, DVI -I -DL, HDTVout, 3Way SLI

Table of Contents:

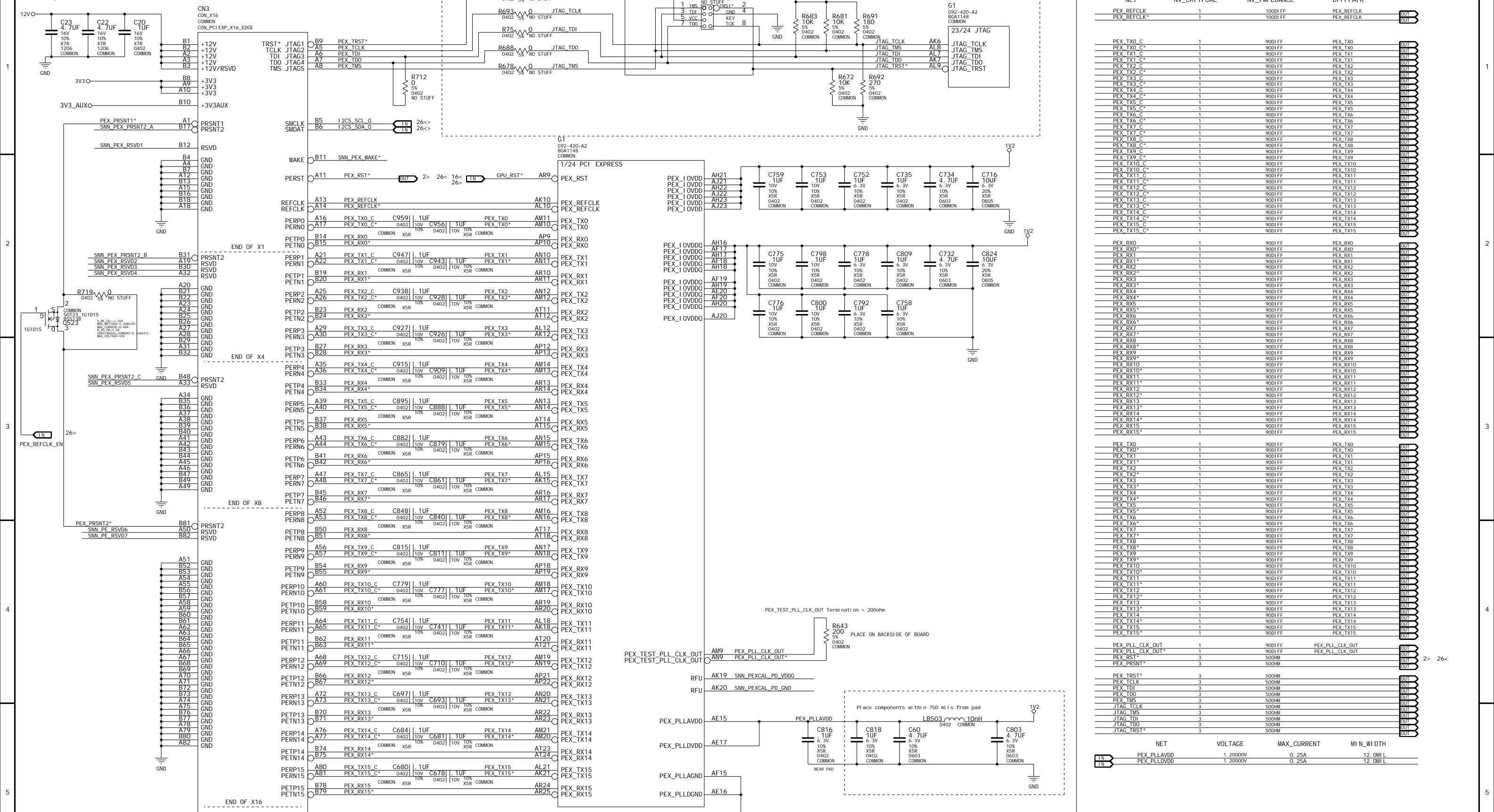
Page 1: Overview  
Page 2: PCI Express 1.0  
Page 3: MEMORY: GPU Partition A/B  
Page 4: MEMORY: GPU Partition C/D  
Page 5: FBA Partition  
Page 6: FBB Partition  
Page 7: FBC Partition  
Page 8: FBD Partition  
Page 9: FrameBuffer Net Rules  
Page 10: DACA Interface  
Page 11: DACC Interface  
Page 12: IFP A/B and C/D Interface  
Page 13: DACB HDTV Interface  
Page 14: Multi-use IO(MIO) Interface  
Page 15: MISC: GPIO, I2C, BIOS, PLL, and XTAL  
Page 16: SPDIF, Thermal Control & TMDS Backdrive Protection  
Page 17: Configuration Straps and Mechanical  
Page 18: Power/GND and Decoupling  
Page 19: Power Supply: 5V, 2V5  
Page 20: Power Supply: 1V2, 1V8  
Page 21: Power Supply: FBVDD, FBVDDQ, 8V5  
Page 22: Power Supply: NVVDD Regulator  
Page 23: Power Supply: NVVDD Phase 1, 2  
Page 24: Power Supply: NVVDD Phase 3, 4  
Page 25: Power Supply: Filter/Detection 12V & 12V\_PEX  
Page 26: Power Supply: Filter/Isolation of 3V3 & Hybrid

REVISION HISTORY:

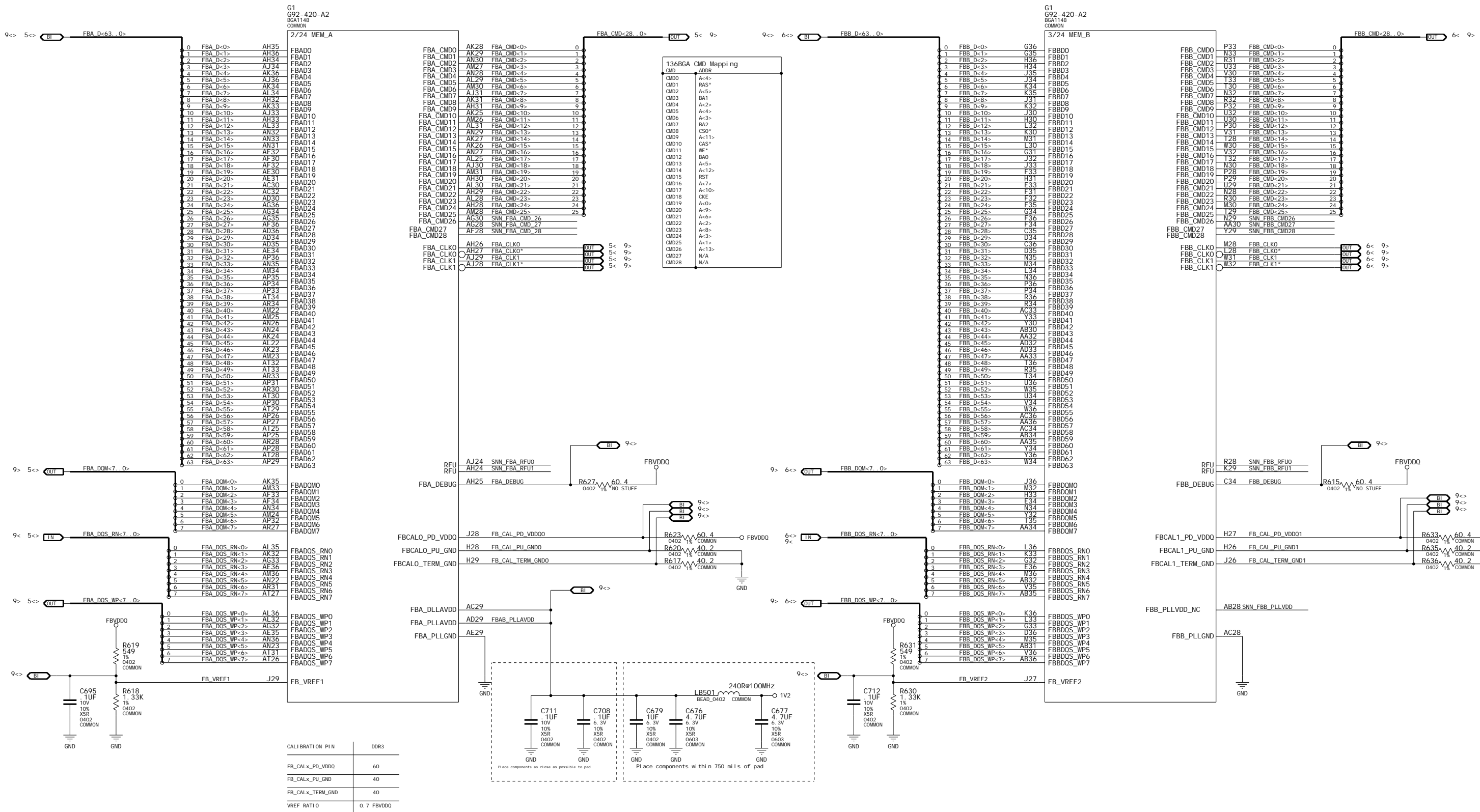
A	Dev Release.
B	X-Release.

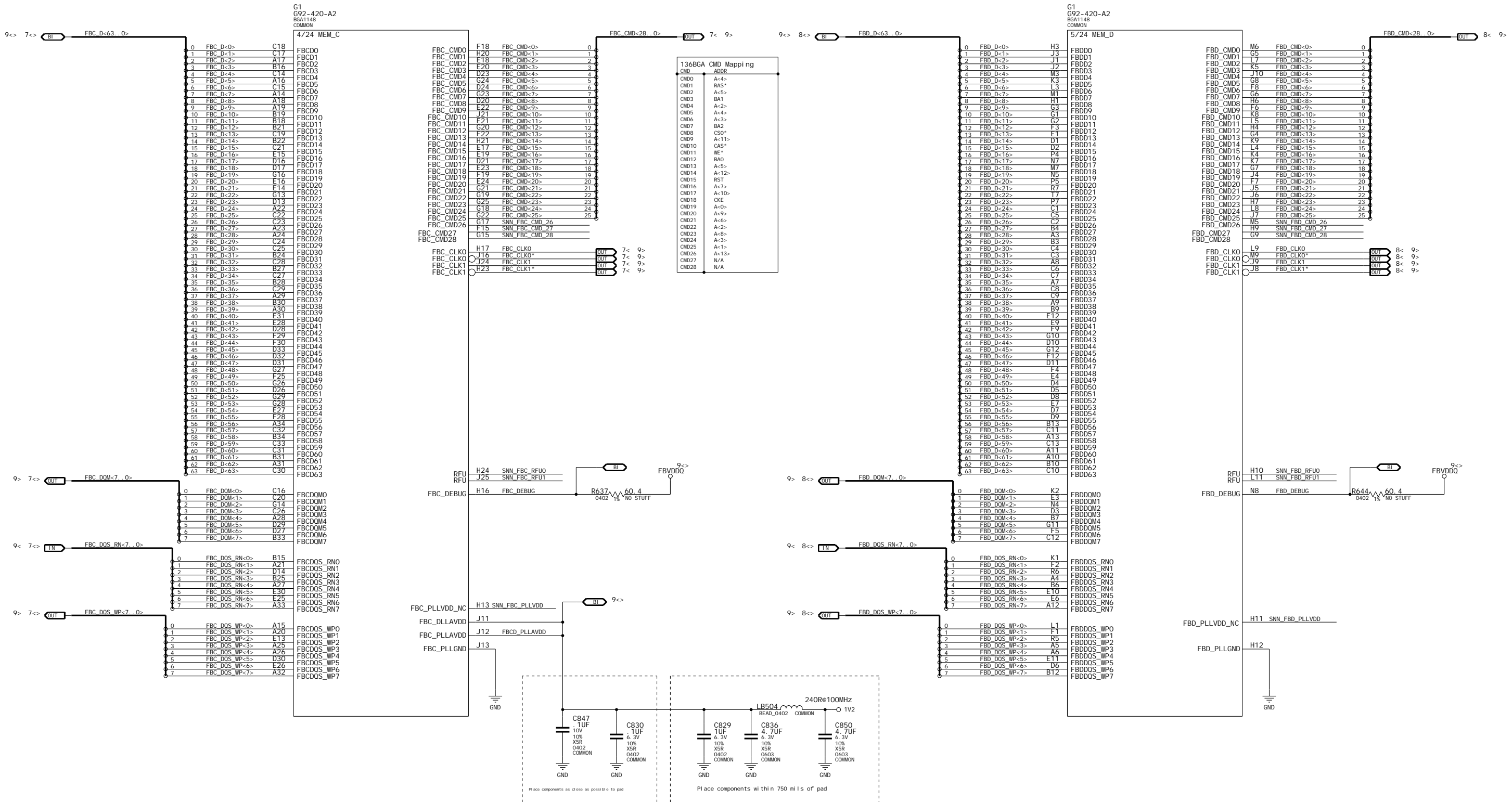
SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10392-base-200	P392 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10392-0001-200	P392 - SKU1
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

## Page2: PCI Express 1.0

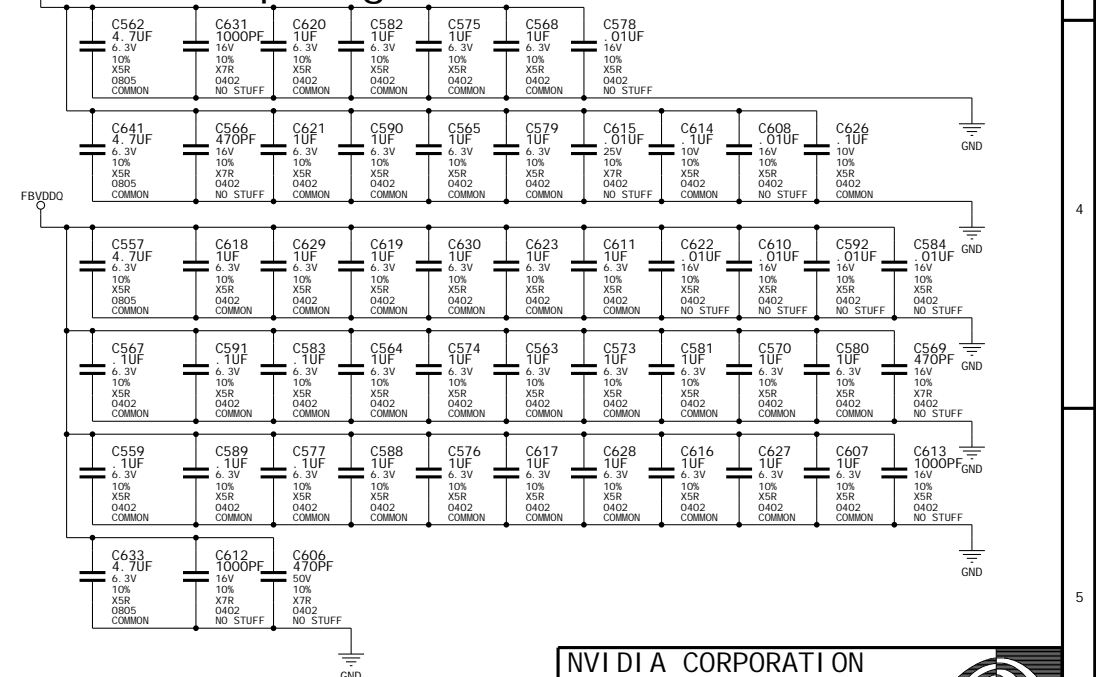
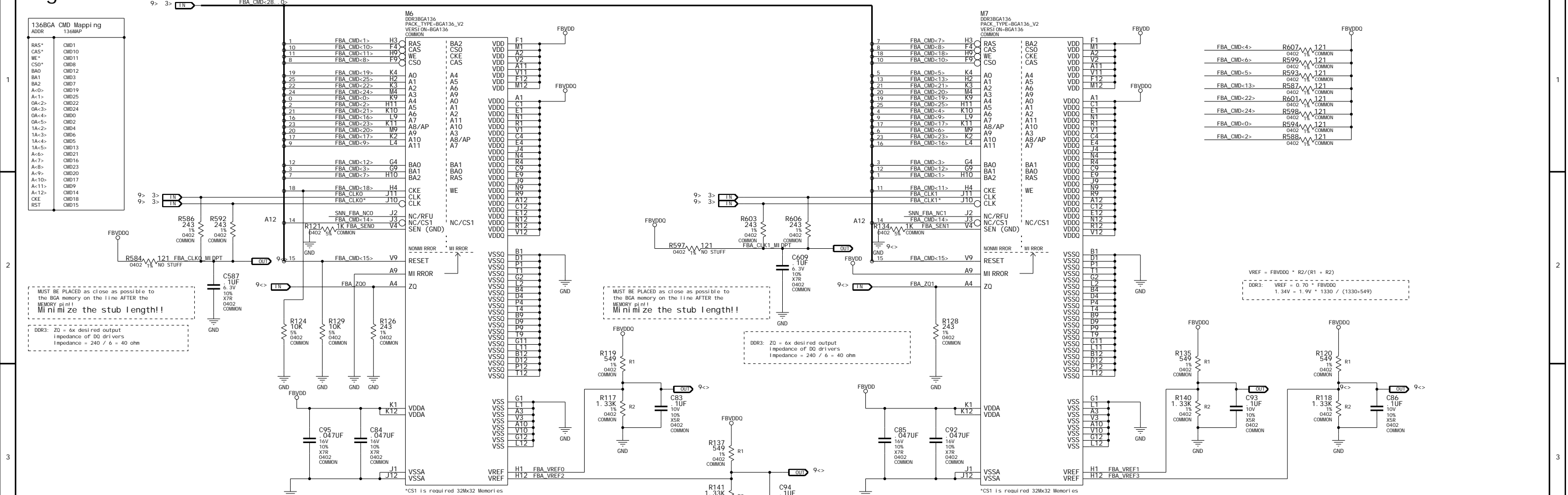


PEX NET RULES				
NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FPAI R	
PEX_REFCLK	1	100DI FF	PEX_REFCLK	OUT
PEX_REFCLK*	1	100DI FF	PEX_REFCLK	OUT
PEX_TX0_C	1	90DI FF	PEX_TX0	OUT
PEX_TX0_C*	1	90DI FF	PEX_TX0	OUT
PEX_TX1_C	1	90DI FF	PEX_TX1	OUT
PEX_TX1_C*	1	90DI FF	PEX_TX1	OUT
PEX_TX2_C	1	90DI FF	PEX_TX2	OUT
PEX_TX2_C*	1	90DI FF	PEX_TX2	OUT
PEX_TX3_C	1	90DI FF	PEX_TX3	OUT
PEX_TX3_C*	1	90DI FF	PEX_TX3	OUT
PEX_TX4_C	1	90DI FF	PEX_TX4	OUT
PEX_TX4_C*	1	90DI FF	PEX_TX4	OUT
PEX_TX5_C	1	90DI FF	PEX_TX5	OUT
PEX_TX5_C*	1	90DI FF	PEX_TX5	OUT
PEX_TX6_C	1	90DI FF	PEX_TX6	OUT
PEX_TX6_C*	1	90DI FF	PEX_TX6	OUT
PEX_TX7_C	1	90DI FF	PEX_TX7	OUT
PEX_TX7_C*	1	90DI FF	PEX_TX7	OUT
PEX_TX8_C	1	90DI FF	PEX_TX8	OUT
PEX_TX8_C*	1	90DI FF	PEX_TX8	OUT
PEX_TX9_C	1	90DI FF	PEX_TX9	OUT
PEX_TX9_C*	1	90DI FF	PEX_TX9	OUT
PEX_TX10_C	1	90DI FF	PEX_TX10	OUT
PEX_TX10_C*	1	90DI FF	PEX_TX10	OUT
PEX_TX11_C	1	90DI FF	PEX_TX11	OUT
PEX_TX11_C*	1	90DI FF	PEX_TX11	OUT
PEX_TX12_C	1	90DI FF	PEX_TX12	OUT
PEX_TX12_C*	1	90DI FF	PEX_TX12	OUT
PEX_TX13_C	1	90DI FF	PEX_TX13	OUT
PEX_TX13_C*	1	90DI FF	PEX_TX13	OUT
PEX_TX14_C	1	90DI FF	PEX_TX14	OUT
PEX_TX14_C*	1	90DI FF	PEX_TX14	OUT
PEX_TX15_C	1	90DI FF	PEX_TX15	OUT
PEX_TX15_C*	1	90DI FF	PEX_TX15	OUT
PEX_RX0	1	90DI FF	PEX_RX0	OUT
PEX_RX0*	1	90DI FF	PEX_RX0	OUT
PEX_RX1	1	90DI FF	PEX_RX1	OUT
PEX_RX1*	1	90DI FF	PEX_RX1	OUT
PEX_RX2	1	90DI FF	PEX_RX2	OUT
PEX_RX2*	1	90DI FF	PEX_RX2	OUT
PEX_RX3	1	90DI FF	PEX_RX3	OUT
PEX_RX3*	1	90DI FF	PEX_RX3	OUT
PEX_RX4	1	90DI FF	PEX_RX4	OUT
PEX_RX4*	1	90DI FF	PEX_RX4	OUT
PEX_RX5	1	90DI FF	PEX_RX5	OUT
PEX_RX5*	1	90DI FF	PEX_RX5	OUT
PEX_RX6	1	90DI FF	PEX_RX6	OUT
PEX_RX6*	1	90DI FF	PEX_RX6	OUT
PEX_RX7	1	90DI FF	PEX_RX7	OUT
PEX_RX7*	1	90DI FF	PEX_RX7	OUT
PEX_RX8	1	90DI FF	PEX_RX8	OUT
PEX_RX8*	1	90DI FF	PEX_RX8	OUT
PEX_RX9	1	90DI FF	PEX_RX9	OUT
PEX_RX9*	1	90DI FF	PEX_RX9	OUT
PEX_RX10	1	90DI FF	PEX_RX10	OUT
PEX_RX10*	1	90DI FF	PEX_RX10	OUT
PEX_RX11	1	90DI FF	PEX_RX11	OUT
PEX_RX11*	1	90DI FF	PEX_RX11	OUT
PEX_RX12	1	90DI FF	PEX_RX12	OUT
PEX_RX12*	1	90DI FF	PEX_RX12	OUT
PEX_RX13	1	90DI FF	PEX_RX13	OUT
PEX_RX13*	1	90DI FF	PEX_RX13	OUT
PEX_RX14	1	90DI FF	PEX_RX14	OUT
PEX_RX14*	1	90DI FF	PEX_RX14	OUT
PEX_RX15	1	90DI FF	PEX_RX15	OUT
PEX_RX15*	1	90DI FF	PEX_RX15	OUT
PEX_TX0	1	90DI FF	PEX_TX0	OUT
PEX_TX0*	1	90DI FF	PEX_TX0	OUT
PEX_TX1	1	90DI FF	PEX_TX1	OUT
PEX_TX1*	1	90DI FF	PEX_TX1	OUT
PEX_TX2	1	90DI FF	PEX_TX2	OUT
PEX_TX2*	1	90DI FF	PEX_TX2	OUT
PEX_TX3	1	90DI FF	PEX_TX3	OUT
PEX_TX3*	1	90DI FF	PEX_TX3	OUT
PEX_TX4	1	90DI FF	PEX_TX4	OUT
PEX_TX4*	1	90DI FF	PEX_TX4	OUT
PEX_TX5	1	90DI FF	PEX_TX5	OUT
PEX_TX5*	1	90DI FF	PEX_TX5	OUT
PEX_TX6	1	90DI FF	PEX_TX6	OUT
PEX_TX6*	1	90DI FF	PEX_TX6	OUT
PEX_TX7	1	90DI FF	PEX_TX7	OUT
PEX_TX7*	1	90DI FF	PEX_TX7	OUT
PEX_TX8	1	90DI FF	PEX_TX8	OUT
PEX_TX8*	1	90DI FF	PEX_TX8	OUT
PEX_TX9	1	90DI FF	PEX_TX9	OUT
PEX_TX9*	1	90DI FF	PEX_TX9	OUT
PEX_TX10	1	90DI FF	PEX_TX10	OUT
PEX_TX10*	1	90DI FF	PEX_TX10	OUT
PEX_TX11	1	90DI FF	PEX_TX11	OUT
PEX_TX11*	1	90DI FF	PEX_TX11	OUT
PEX_TX12	1	90DI FF	PEX_TX12	OUT
PEX_TX12*	1	90DI FF	PEX_TX12	OUT
PEX_TX13	1	90DI FF	PEX_TX13	OUT
PEX_TX13*	1	90DI FF	PEX_TX13	OUT
PEX_TX14	1	90DI FF	PEX_TX14	OUT
PEX_TX14*	1	90DI FF	PEX_TX14	OUT
PEX_TX15	1	90DI FF	PEX_TX15	OUT
PEX_TX15*	1	90DI FF	PEX_TX15	OUT
PEX_PLL_CLK_OUT	1	90DI FF	PEX_PLL_CLK_OUT	OUT
PEX_PLL_CLK_OUT*	1	90DI FF	PEX_PLL_CLK_OUT	OUT
PEX_RST*	3	500HM		OUT
PEX_PRESNT*	3	500HM		OUT
PEX_TRST*	3	500HM		OUT
PEX_TCLK	3	500HM		OUT
PEX_TDI	3	500HM		OUT
PEX_TDO	3	500HM		OUT
PEX_TMS	3	500HM		OUT
JTAG_TCLK	3	500HM		OUT
JTAG_TMS	3	500HM		OUT
JTAG_TDI	3	500HM		OUT
JTAG_TDO	3	500HM		OUT
JTAG_TRST*	3	500HM		OUT





## Page5: FBA Partiti on



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY



NV_PN	600-10392-0001-200 A
-------	----------------------

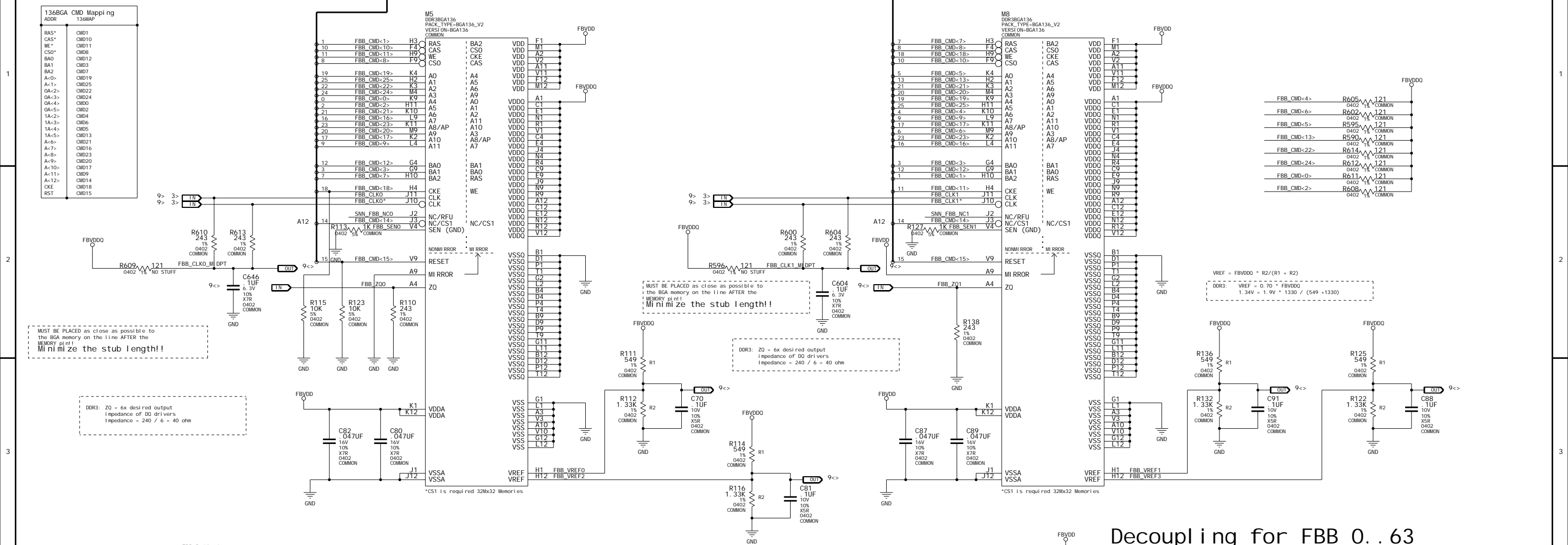
ID	design	PAGE	5 OF 26
----	--------	------	---------

NAME	etal	DATE	17-JAN-2008
------	------	------	-------------

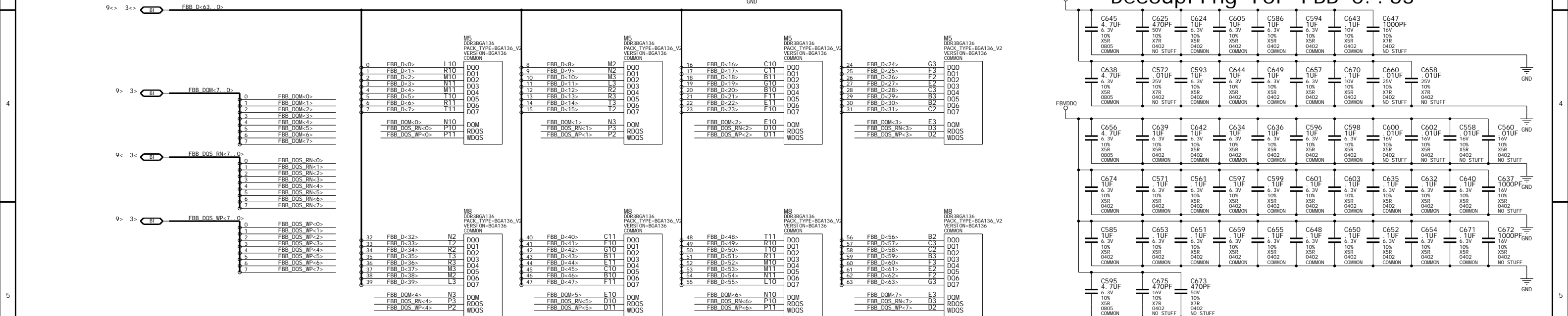
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	P392 - SKU1
PAGE DETAIL	FBA Partit ion

## Page6: FBB Parti ti on



## Decoupling for FBB 0..63



ASSEMBLY	P392 - SKU1
PAGE DETAIL	FBB Partit ion

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA

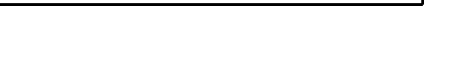
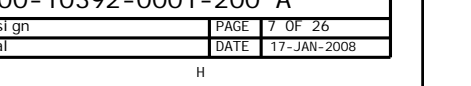
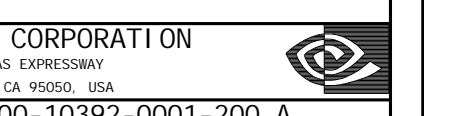
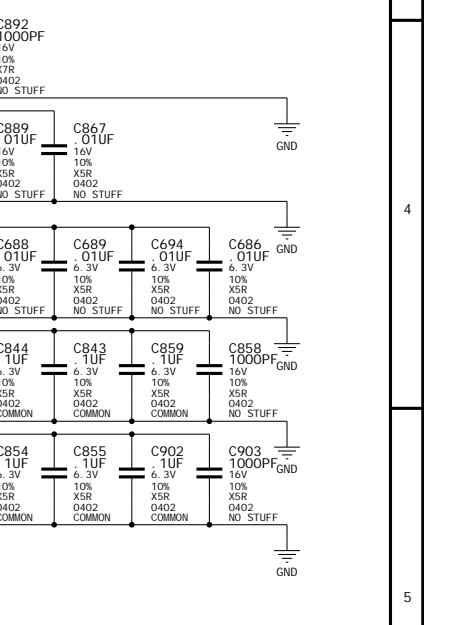
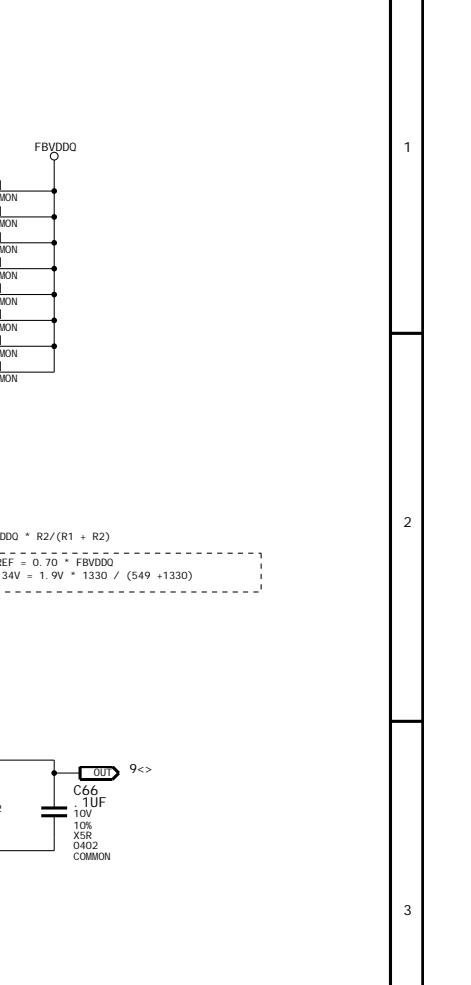
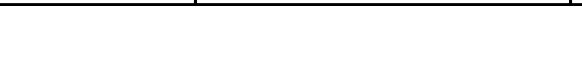
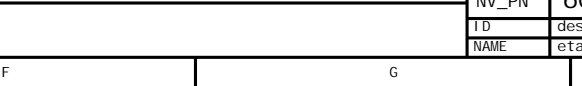
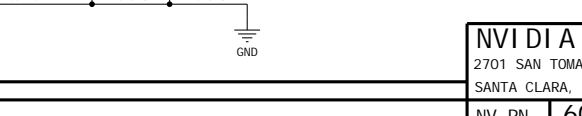
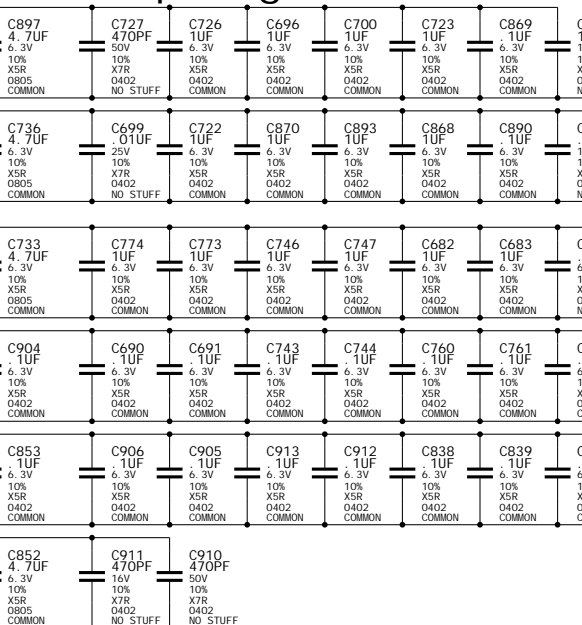
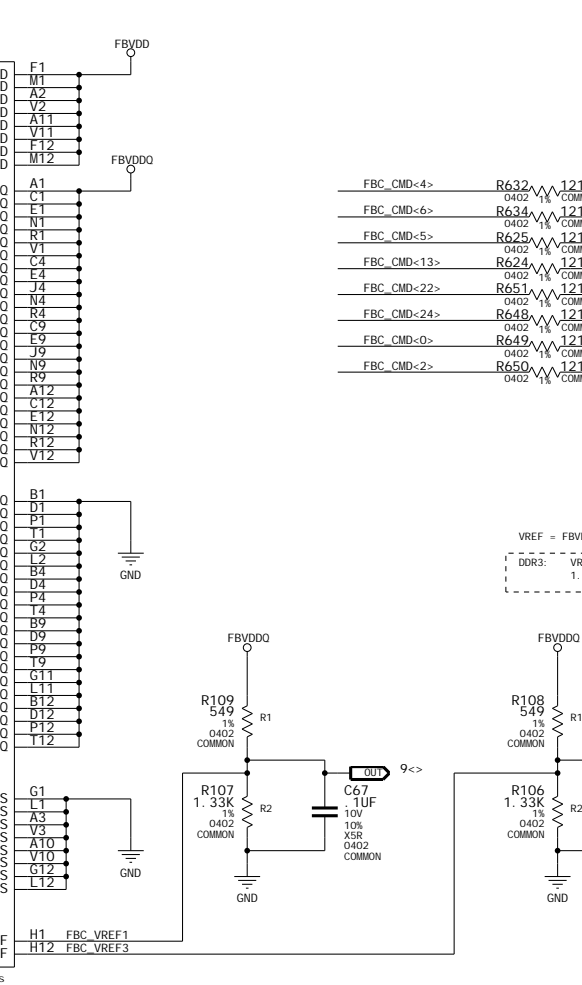
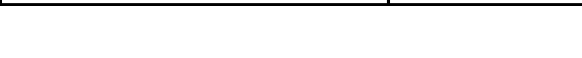
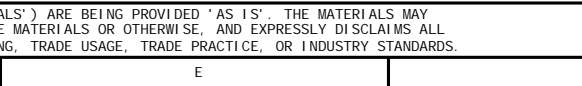
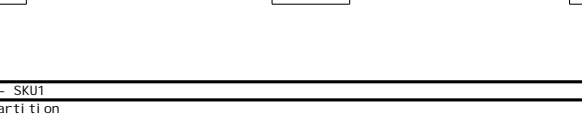
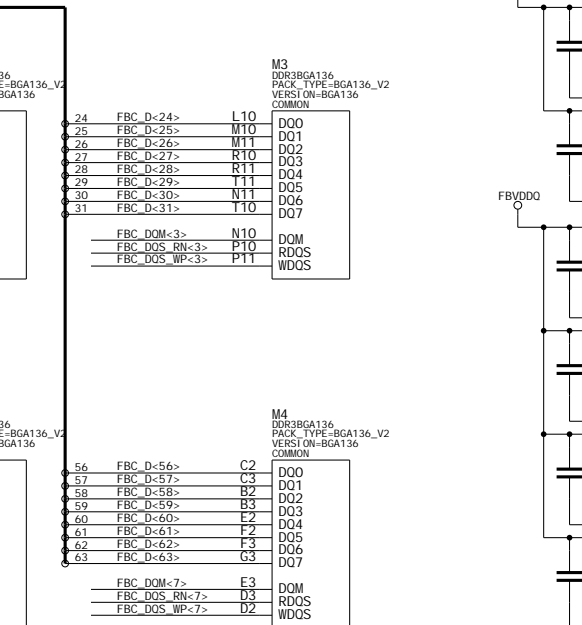
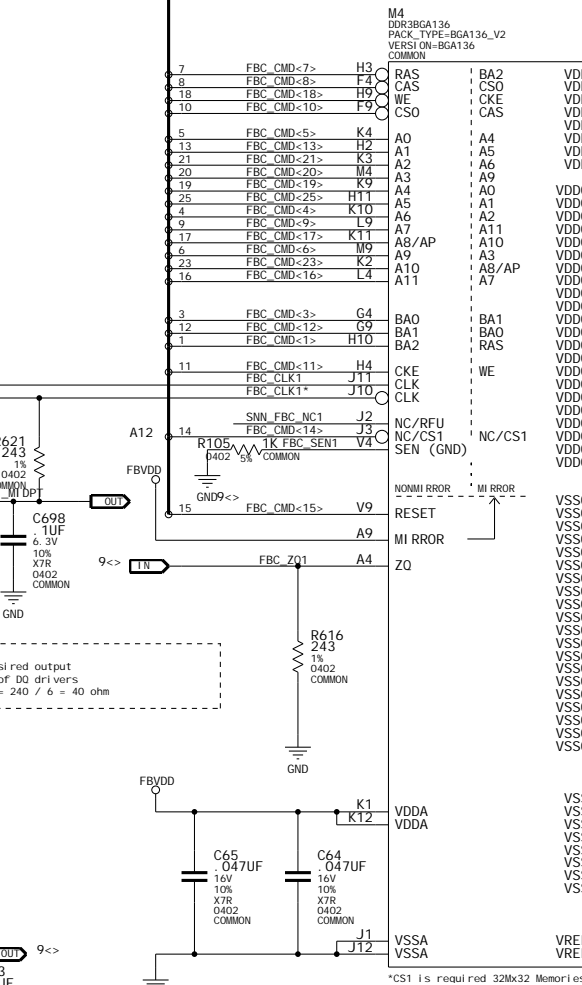
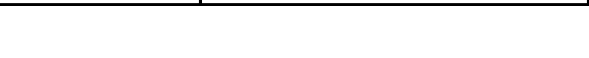
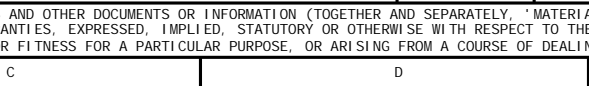
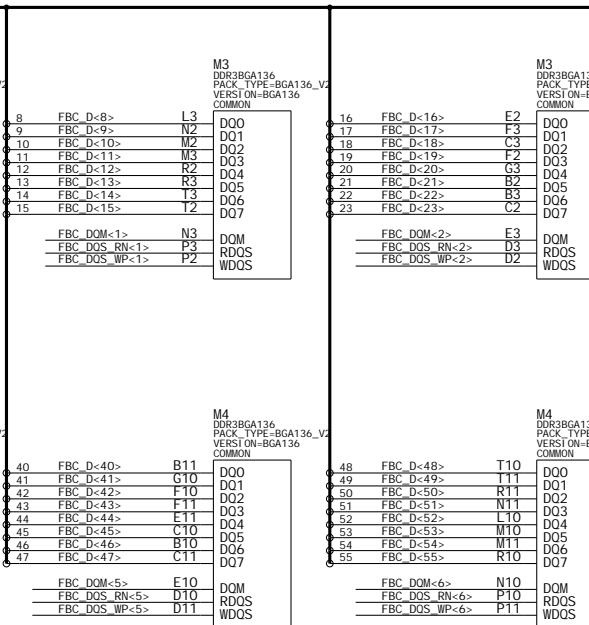
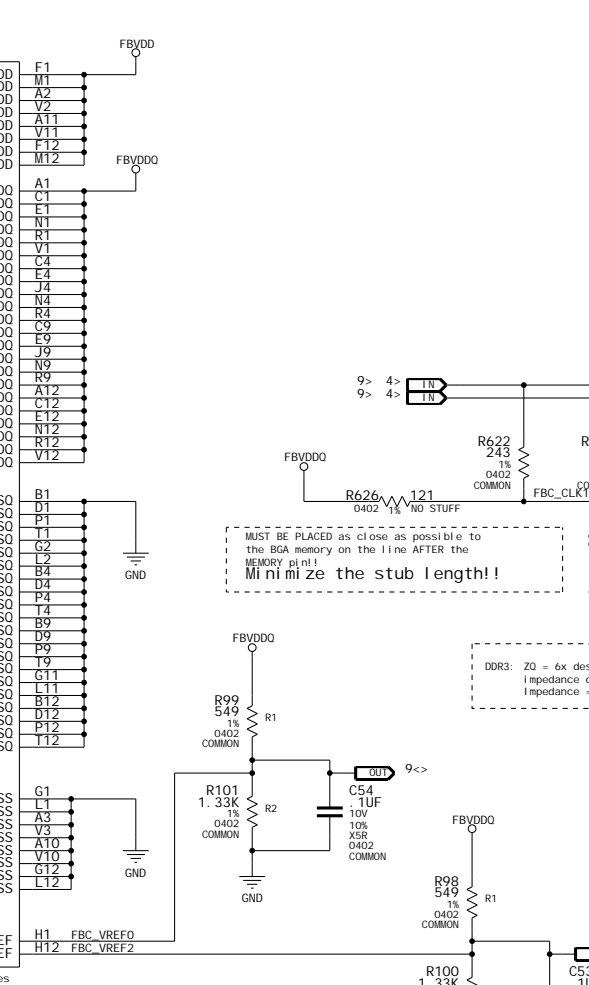
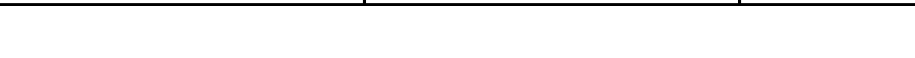
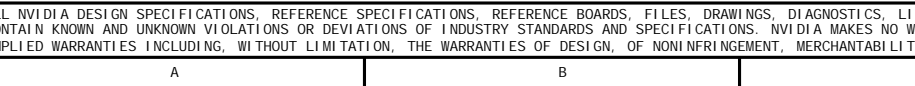
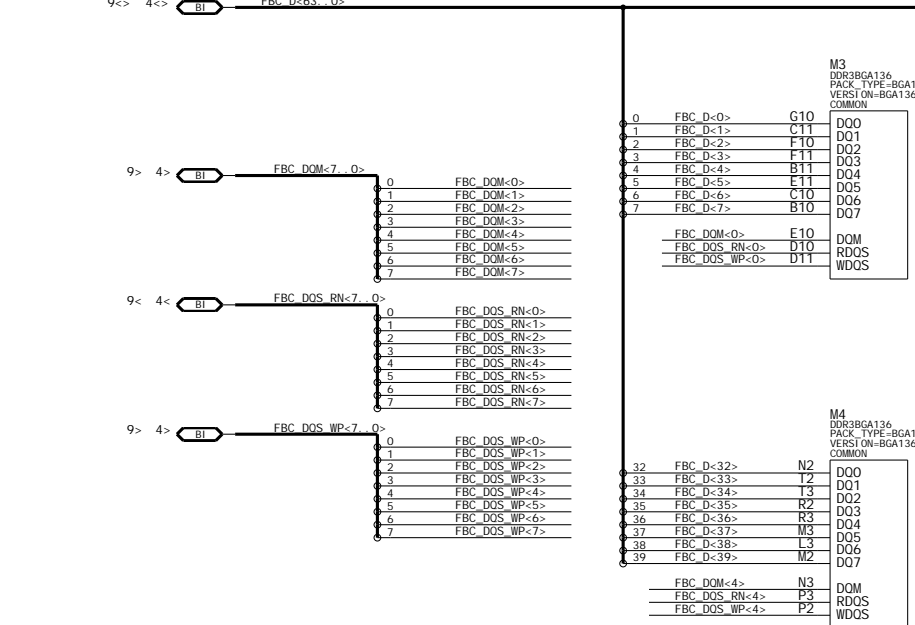
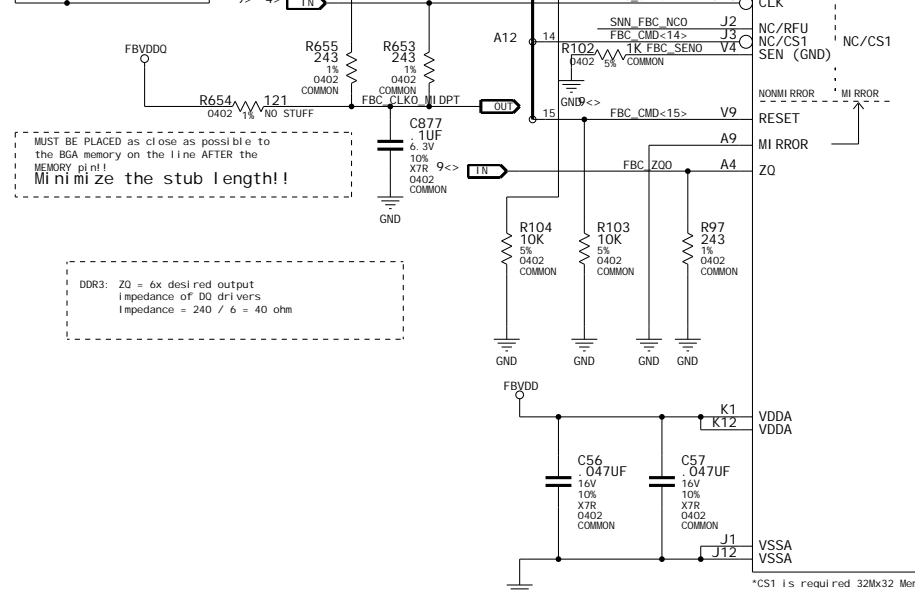
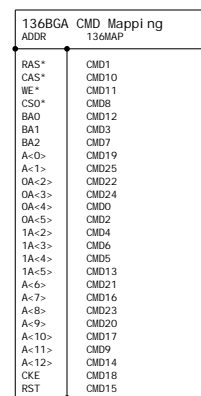


NV_PN	600-10392-0001-200 A
-------	----------------------

ID	design	PAGE	6 OF 26
----	--------	------	---------

NAME	etal	DATE	17-JAN-2008
------	------	------	-------------

## Page7: FBC Parti ti on



## Decoupling for FBC 0..63

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV PN	600-10392-0001-200 A
-------	----------------------

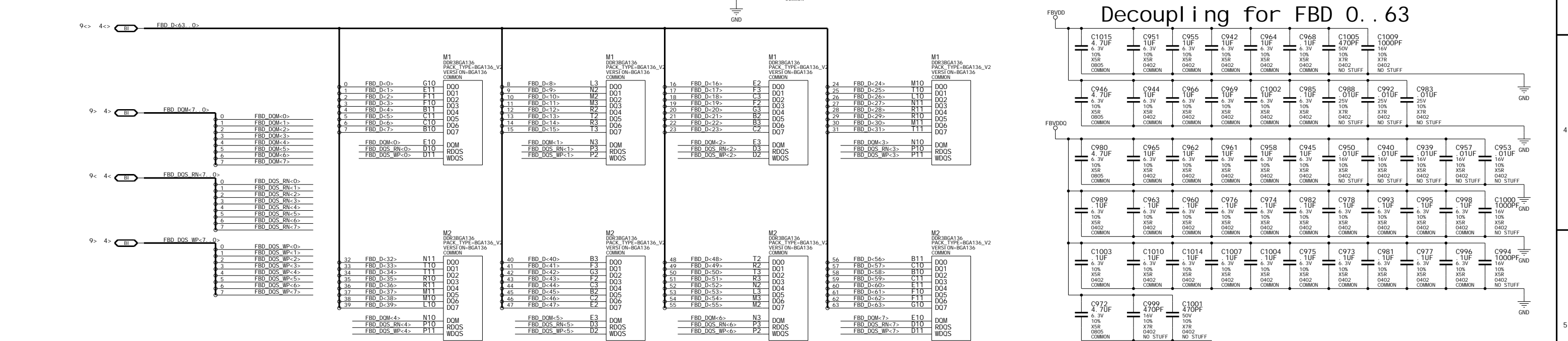
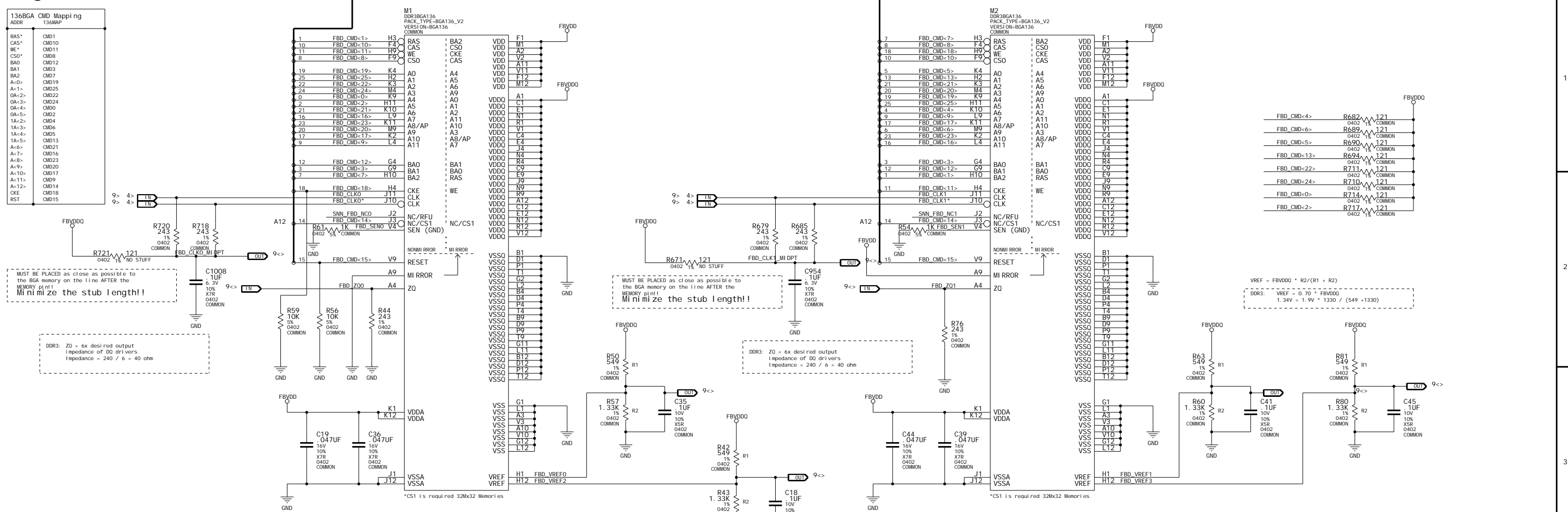
IP: design PAGE 7 OF 26

NAME	etal	DATE	17-JAN-2
------	------	------	----------

	H
--	---
















































## Page8: FBD Parti ti on










































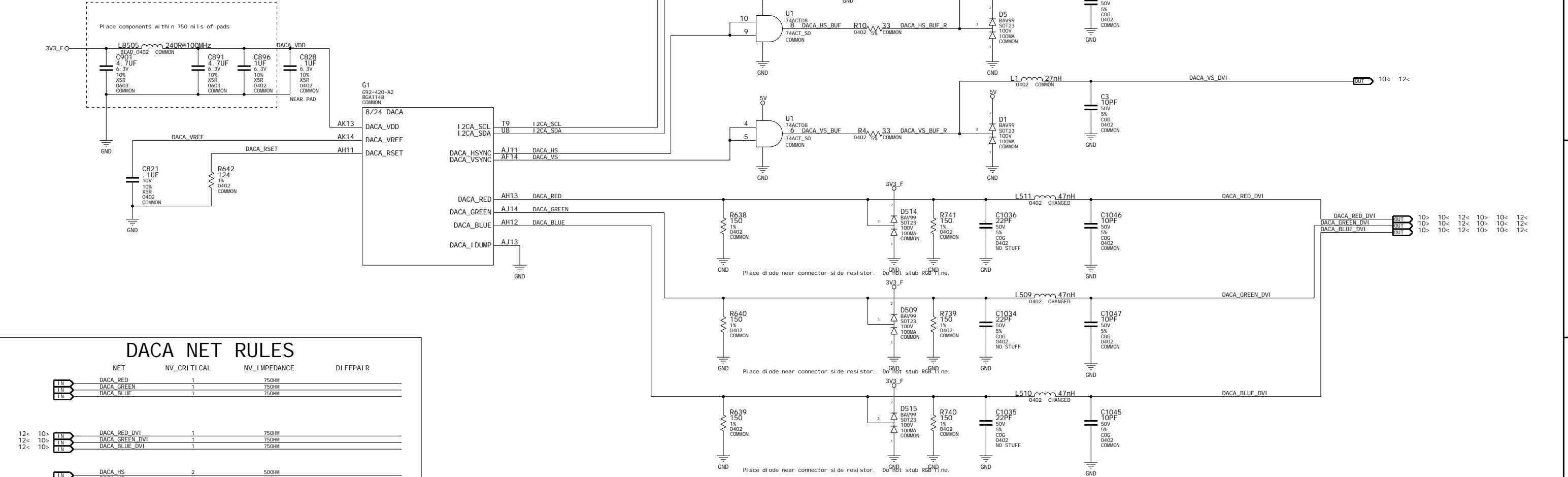
NET RULES for FrameBuffer A/B

NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
5<	3> 	FBA_CLK0	1	80DI FF
5<	3> 	FBA_CLK0*	1	80DI FF
5<	3> 	FBA_CLK1	1	80DI FF
5<	3> 	FBA_CLK1*	1	80DI FF
5<	3> 	FBA_CMD<28..0>	1	40OHM
5<	3> 	FBA_DQS_WP<7..0>	1	40OHM
5<	3> 	FBA_DQS_RN<7..0>	1	40OHM
5<	3> 	FBA_DQM<7..0>	1	40OHM
5<	3> 	FBA_D<63..0>	1	40OHM
NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
6<	3> 	FBB_CLK0	1	80DI FF
6<	3> 	FBB_CLK0*	1	80DI FF
6<	3> 	FBB_CLK1	1	80DI FF
6<	3> 	FBB_CLK1*	1	80DI FF
6<	3> 	FBB_CMD<28..0>	1	40OHM
6<	3> 	FBB_DQS_WP<7..0>	1	40OHM
6<	3> 	FBB_DQS_RN<7..0>	1	40OHM
6<	3> 	FBB_DQM<7..0>	1	40OHM
6<	3> 	FBB_D<63..0>	1	40OHM
NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
3<	3> 	FB_CAL_PD_VDDQ0	3	50OHM
3<	3> 	FB_CAL_PD_GND0	3	50OHM
3<	3> 	FB_CAL_TERM_GND0	3	50OHM
3<	3> 	FB_CAL_PD_VDDQ1	3	50OHM
3<	3> 	FB_CAL_PD_GND1	3	50OHM
3<	3> 	FB_CAL_TERM_GND1	3	50OHM
3<	3> 	FBA_DEBUG	1	40OHM
3<	3> 	FBB_DEBUG	1	40OHM
NET		VOLTAGE	MAX_CURRENT	MI N_WI DTH
3<	3> 	FBAB_PL LavDD	3.30000V	0.02A
5>	5> 	FBA_VREF0	1.47000V	0.02A
5>	5> 	FBA_VREF1	1.47000V	0.02A
5>	5> 	FBA_VREF2	1.47000V	0.02A
5>	5> 	FBA_VREF3	1.47000V	0.02A
5<	5< 	FBA_Z00	1.47000V	0.02A
5<	5< 	FBA_ZQ1	1.47000V	0.02A
5>	5> 	FBA_CLK0_MIDPT	1.05000V	
5>	5> 	FBA_CLK1_MIDPT	1.05000V	
6>	6> 	FBB_CLK0_MIDPT	1.05000V	
6>	6> 	FBB_CLK1_MIDPT	1.05000V	
6>	6> 	FBB_VREF0	1.47000V	0.02A
6>	6> 	FBB_VREF1	1.47000V	0.02A
6>	6> 	FBB_VREF2	1.47000V	0.02A
6>	6> 	FBB_VREF3	1.47000V	0.02A
6<	6< 	FBB_Z00	1.47000V	0.02A
6<	6< 	FBB_ZQ1	1.47000V	0.02A
3<	3> 	FB_VREF1	1.47000	0.02A
3<	3> 	FB_VREF2	1.47000	0.02A

NET RULES for FrameBuffer C/D

NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
7<	4> 	FBC_CLK0	1	80DI FF
7<	4> 	FBC_CLK0*	1	80DI FF
7<	4> 	FBC_CLK1	1	80DI FF
7<	4> 	FBC_CLK1*	1	80DI FF
7<	4> 	FBC_CMD<28..0>	1	40OHM
7<	4> 	FBC_DQS_WP<7..0>	1	40OHM
7<	4> 	FBC_DQS_RN<7..0>	1	40OHM
7<	4> 	FBC_DQM<7..0>	1	40OHM
7<	4> 	FBC_D<63..0>	1	40OHM
NET		NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
8<	4> 	FBD_CLK0	1	80DI FF
8<	4> 	FBD_CLK0*	1	80DI FF
8<	4> 	FBD_CLK1	1	80DI FF
8<	4> 	FBD_CLK1*	1	80DI FF
8<	4> 	FBD_CMD<28..0>	1	40OHM
8<	4> 	FBD_DQS_WP<7..0>	1	40OHM
8<	4> 	FBD_DQS_RN<7..0>	1	40OHM
8<	4> 	FBD_DQM<7..0>	1	40OHM
8<	4> 	FBD_D<63..0>	1	40OHM
4<	4> 	FBC_DEBUG	1	40OHM
4<	4> 	FBD_DEBUG	1	40OHM
NET		VOLTAGE	MAX_CURRENT	MI N_WI DTH
4<	4> 	FBCD_PL LavDD	3.30000V	0.02A
7>	7> 	FBC_VREF0	1.47000V	0.02A
7>	7> 	FBC_VREF1	1.47000V	0.02A
7>	7> 	FBC_VREF2	1.47000V	0.02A
7>	7> 	FBC_VREF3	1.47000V	0.02A
7<	7< 	FBC_Z00	1.47000V	0.02A
7<	7< 	FBC_ZQ1	1.47000V	0.02A
7>	7> 	FBC_CLK0_MIDPT	1.05000V	
7>	7> 	FBC_CLK1_MIDPT	1.05000V	
8>	8> 	FBD_CLK0_MIDPT	1.05000V	
8>	8> 	FBD_CLK1_MIDPT	1.05000V	
8>	8> 	FBD_VREF0	1.47000V	0.02A
8>	8> 	FBD_VREF1	1.47000V	0.02A
8>	8> 	FBD_VREF2	1.47000V	0.02A
8>	8> 	FBD_VREF3	1.47000V	0.02A
8<	8< 	FBD_Z00	1.47000V	0.02A
8<	8< 	FBD_ZQ1	1.47000V	0.02A

Page10: DACA Interface



DACA NET RULES

NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
DACA_RED	1	75OHM	
DACA_GREEN	1	75OHM	
DACA_BLUE	1	75OHM	
DACA_RED_DVI	1	75OHM	
DACA_GREEN_DVI	1	75OHM	
DACA_BLUE_DVI	1	75OHM	
DACA_HS	2	50OHM	
DACA_VS	2	50OHM	
DACA_HS_BUF	2	50OHM	
DACA_VS_BUF	2	50OHM	
DACA_HS_BUF_R	2	50OHM	
DACA_VS_BUF_R	2	50OHM	
DACA_HS_DVI	2	50OHM	
DACA_VS_DVI	2	50OHM	
I2CA_SCL	3	50OHM	
I2CA_SDA	3	50OHM	
I2CA_SCL_R	3	50OHM	
I2CA_SDA_R	3	50OHM	
I2CA_SCL_DVI	3	50OHM	
I2CA_SDA_DVI	3	50OHM	
DACA_VREF	12_0MI L		
DACA_RSET	12_0MI L		
DACA_VDD	3_30000V	0_100A	16_0MI L
DACA_GND	0_00000V		16_0MI L

NV I D I A CORPORATION

2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA

NV\_PN

600-10392-0001-200 A

ID

dest gn

PAGE

10 OF 26

NAME

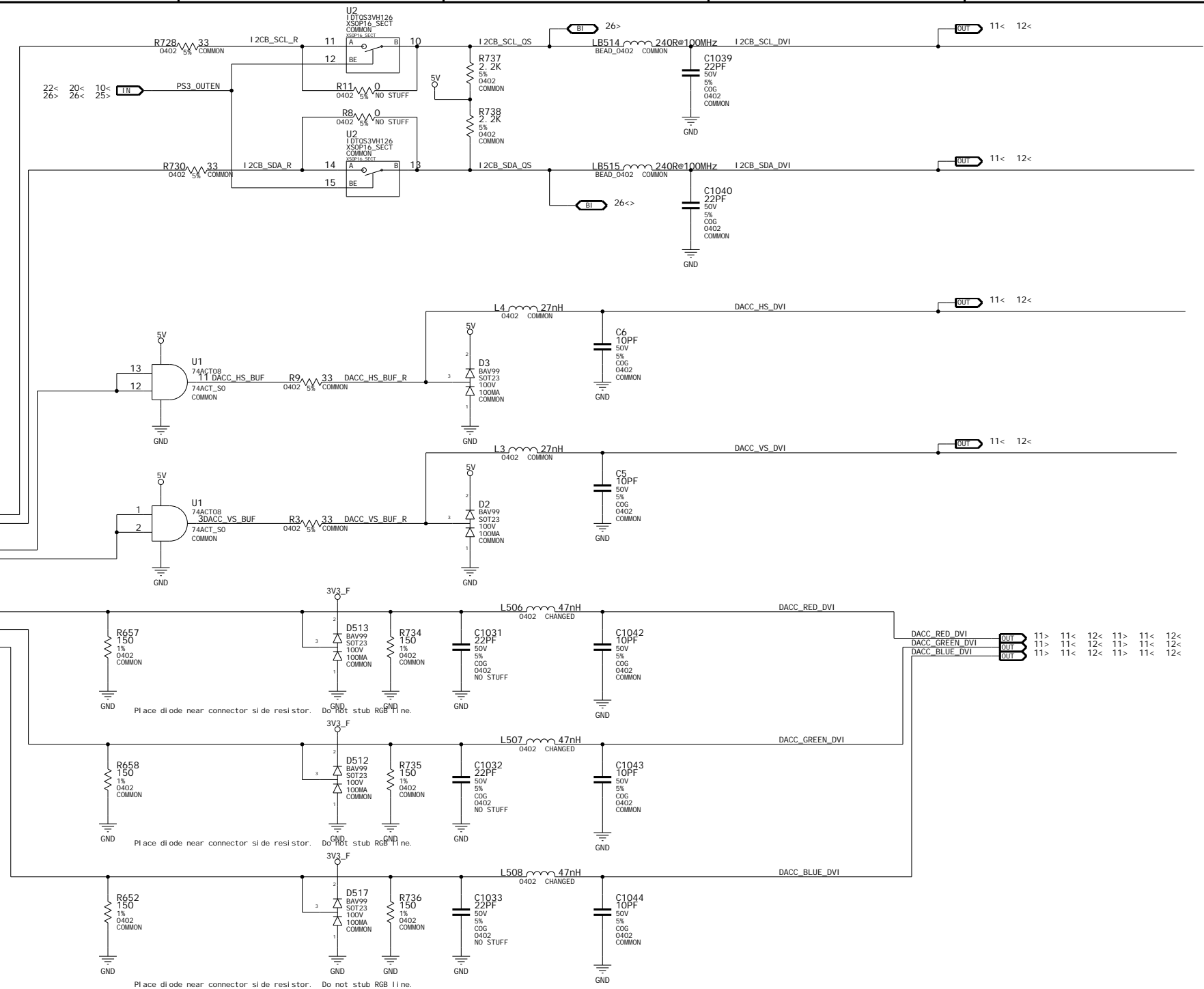
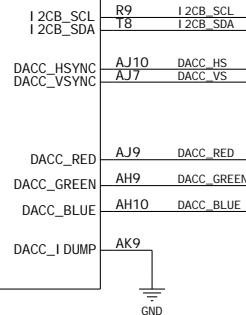
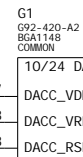
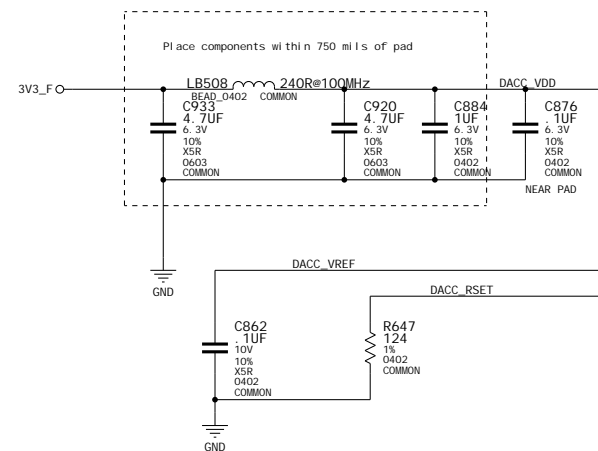
etal

DATE

17-JAN-2008


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

## Page11: DACC Interface




## DACC NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	DACC_RED	1	75OHM	
IN	DACC_GREEN	1	75OHM	
IN	DACC_BLUE	1	75OHM	

12<	11>		DACC RED DVI	1	750HM
12<	11>		DACC GREEN DVI	1	750HM
12<	11>		DACC BLUE DVI	1	750HM

1N	DACC_HS	2	500HM
1N	DACC_VS	2	500HM
1N	DACC_HS_BUF	2	500HM
1N	DACC_VS_BUF	2	500HM
1N	DACC_HS_BUF_R	2	500HM
1N	DACC_VS_BUF_R	2	500HM

12<	11>		DACC_HS_DVI	2	500HM
12<	11>		DACC_VS_DVI	2	500HM

IN	I2CB_SCL	3	500HM
IN	I2CB_SDA	3	500HM
IN	I2CB_SCL_R	3	500HM
IN	I2CB_SDA_R	3	500HM

12<	11>	IN	I2CB_SCL_DVI	3	500HM
12<	11>	IN	I2CB_SDA_DVI	3	500HM

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	DACC_VREF			12.0mil
IN	DACC_RSET			12.0mil

BI	DACC_VDD	3.30000V	0.100A	16.0MI L
TM	DACC_GND	0.000000V		16.0MI L

ASSEMBLY	P392 - SKU1
PAGE DETAIL	DACC Interface

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

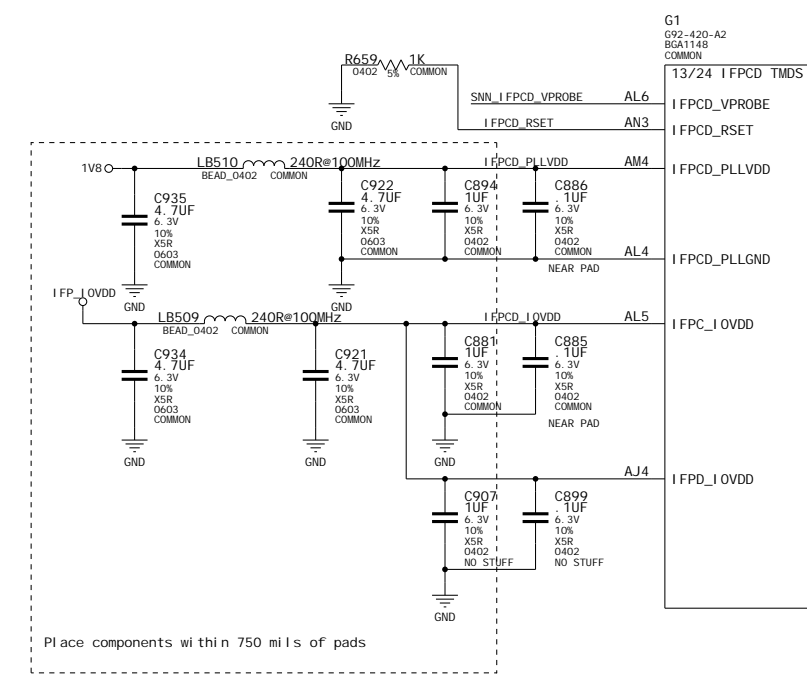
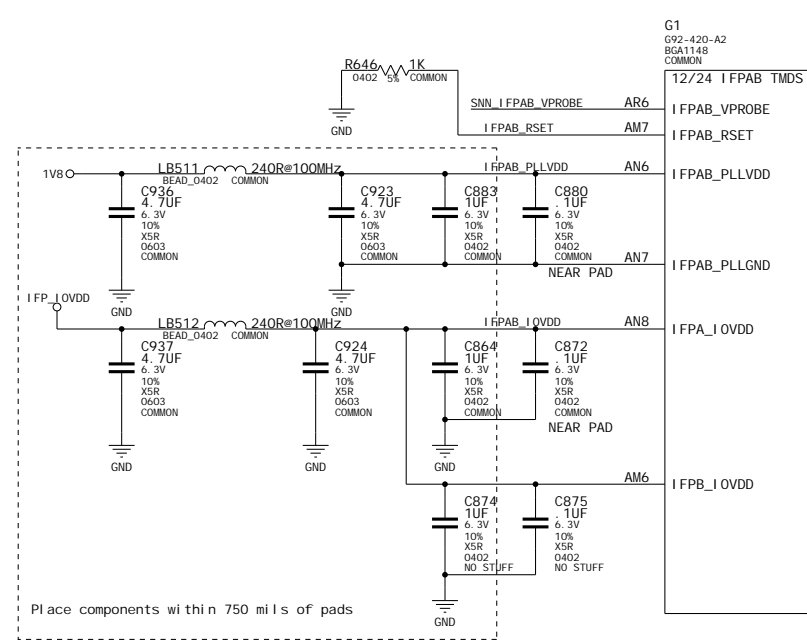
SANTA CLARA, CA 95050, USA

NV_PN	600-10392-0001-200 A
-------	----------------------

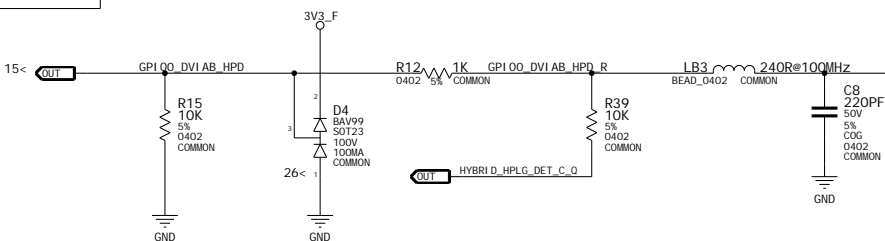
IP	des gn	PAGE	11 OF 26
----	--------	------	----------

NAME	etal	DATE	17-JAN-2008
------	------	------	-------------

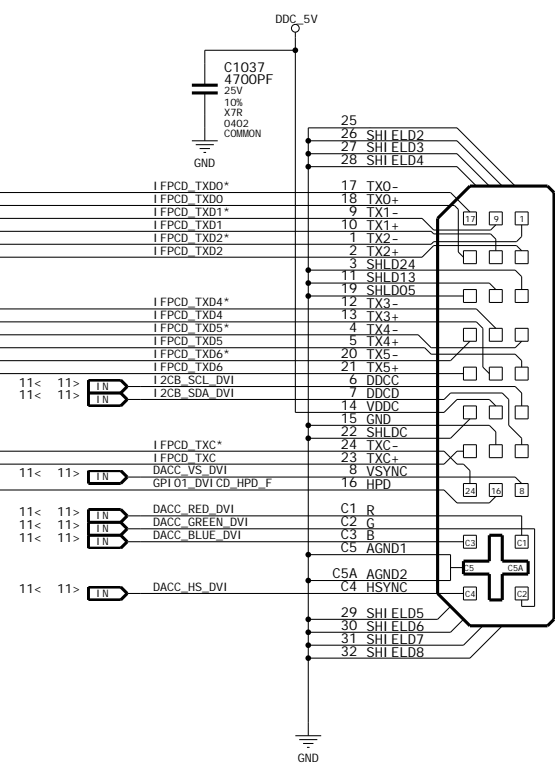
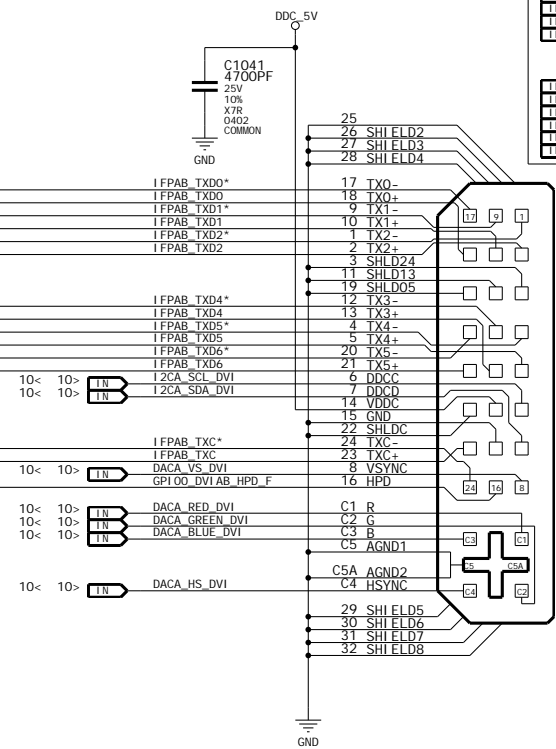
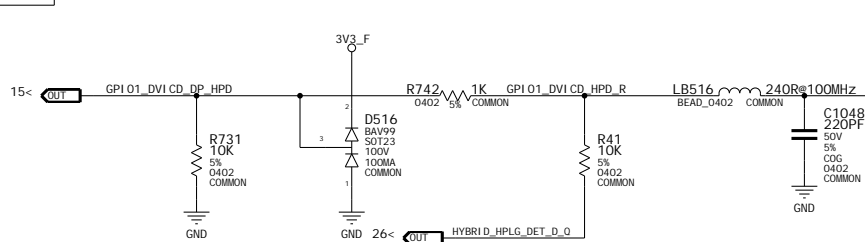
Page12: IFP A/B and C/D Interface



NET RULES				
NET	DIFFPAIR	NV_CRTICAL	NV_IMPEDANCE	
IFPA_TXC	AT9	IFPA_TXC*	IFPA_TXC	1
IFPA_TXC	AT8	IFPA_TXC	IFPA_TXC	1
IFPA_TXD0	AN4	IFPA_TXD0*	IFPA_TXD0	1
IFPA_TXD0	AN5	IFPA_TXD0	IFPA_TXD0	1
IFPA_TXD1	AT3	IFPA_TXD1*	IFPA_TXD1	1
IFPA_TXD1	AT4	IFPA_TXD1	IFPA_TXD1	1
IFPA_TXD2	AP4	IFPA_TXD2*	IFPA_TXD2	1
IFPA_TXD2	AP5	IFPA_TXD2	IFPA_TXD2	1
IFPA_TXD3	AR3	SNN_IFPA_TXD3*		
IFPA_TXD3	AR4	SNN_IFPA_TXD3		
IFPB_TXC	AP1	SNN_IFPB_TXC*		
IFPB_TXC	AR2	SNN_IFPB_TXC		
IFPB_TXD4	AP6	IFPB_TXD4*	IFPB_TXD4	1
IFPB_TXD4	AP7	IFPB_TXD4	IFPB_TXD4	1
IFPB_TXD5	AR7	IFPB_TXD5*	IFPB_TXD5	1
IFPB_TXD5	AR8	IFPB_TXD5	IFPB_TXD5	1
IFPB_TXD6	AT5	IFPB_TXD6*	IFPB_TXD6	1
IFPB_TXD6	AT6	IFPB_TXD6	IFPB_TXD6	1
IFPB_TXD7	AN2	SNN_IFPB_TXD7*		
IFPB_TXD7	AP2	SNN_IFPB_TXD7		



NET RULES				
NET	DIFFPAIR	NV_CRTICAL	NV_IMPEDANCE	
IFPC_TXC	AJ6	IFPC_TXC*	IFPC_TXC	1
IFPC_TXC	AH6	IFPC_TXC	IFPC_TXC	1
IFPC_TXD0	AL2	IFPC_TXD0*	IFPC_TXD0	1
IFPC_TXD0	AL1	IFPC_TXD0	IFPC_TXD0	1
IFPC_TXD1	AJ1	IFPC_TXD1*	IFPC_TXD1	1
IFPC_TXD1	AK1	IFPC_TXD1	IFPC_TXD1	1
IFPC_TXD2	AL3	IFPC_TXD2*	IFPC_TXD2	1
IFPC_TXD2	AM3	IFPC_TXD2	IFPC_TXD2	1
IFPD_TXC	AH5	SNN_IFPD_TXC*		
IFPD_TXC	AH4	SNN_IFPD_TXC		
IFPD_TXD4	AK2	IFPD_TXD4*	IFPD_TXD4	1
IFPD_TXD4	AK3	IFPD_TXD4	IFPD_TXD4	1
IFPD_TXD5	AK4	IFPD_TXD5*	IFPD_TXD5	1
IFPD_TXD5	AK5	IFPD_TXD5	IFPD_TXD5	1
IFPD_TXD6	AM1	IFPD_TXD6*	IFPD_TXD6	1
IFPD_TXD6	AN1	IFPD_TXD6	IFPD_TXD6	1



IFPABCD NET RULES

NET	NV_CRTICAL	NV_IMPEDANCE	DIFFPAIR
GPI00_DVIAB_HPD_F	3	50OHM	
GPI00_DVIAB_HPD_R	3	50OHM	
GPI01_DVICD_HPD_F	3	50OHM	
GPI01_DVICD_HPD_R	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_RSET			12.0MIL
IFPCD_RSET			12.0MIL
IFPAB_PLLVDD	3.30000V	0.03A	16.0MIL
IFPAB_I0VDD	3.30000V	0.09A	16.0MIL
IFPCD_PLLVDD	3.30000V	0.03A	16.0MIL
IFPCD_I0VDD	3.30000V	0.09A	16.0MIL

J3

DVI-I

DVI-I\_(SLIM\_)SHLD\_M

DVI-I\_SLIM\_SHLD\_M

COMMON

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA



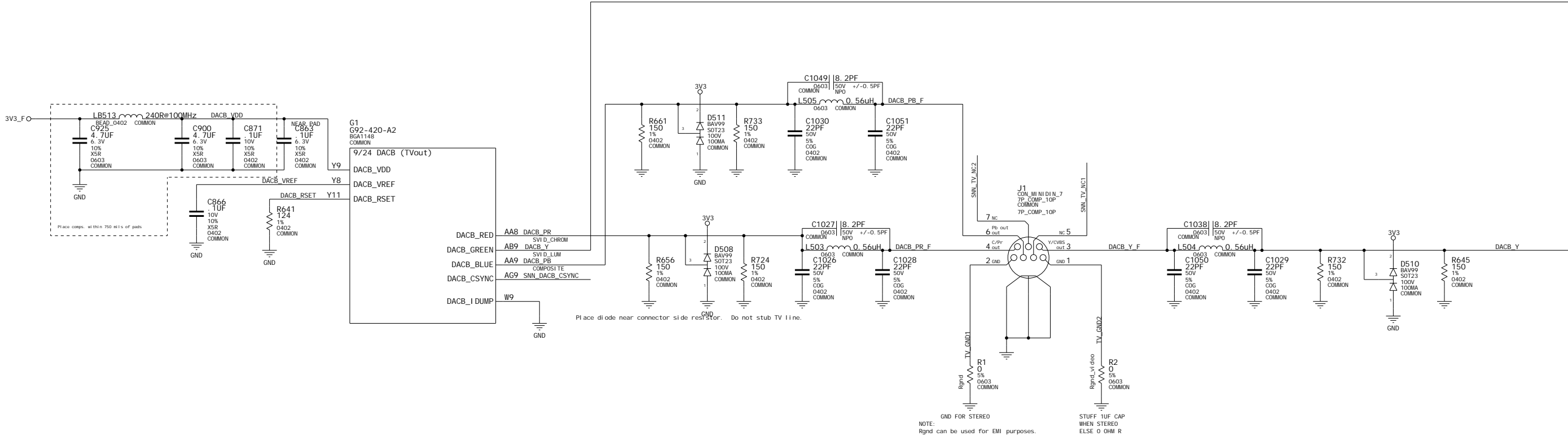
NV\_PN 600-10392-0001-200 A

ID	destgn	PAGE	12 OF 26
NAME	etal	DATE	17-JAN-2008

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

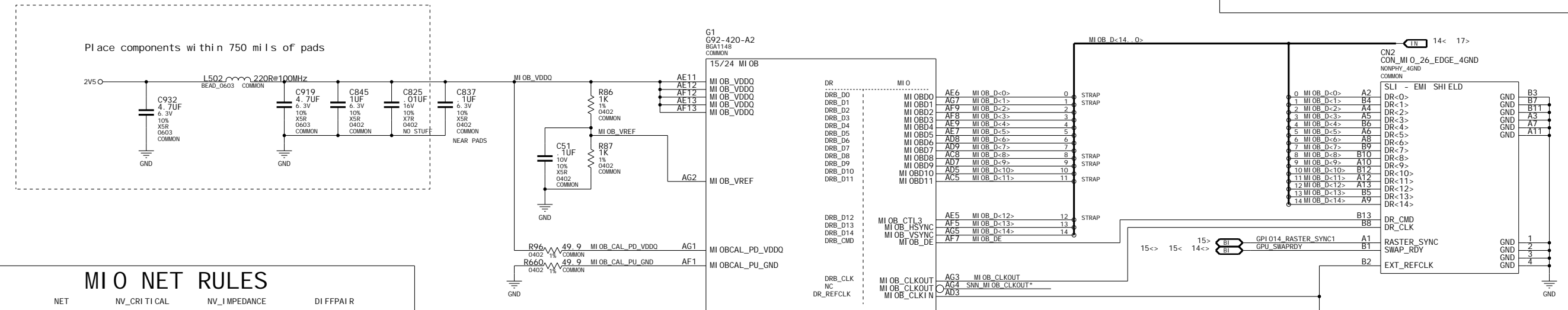
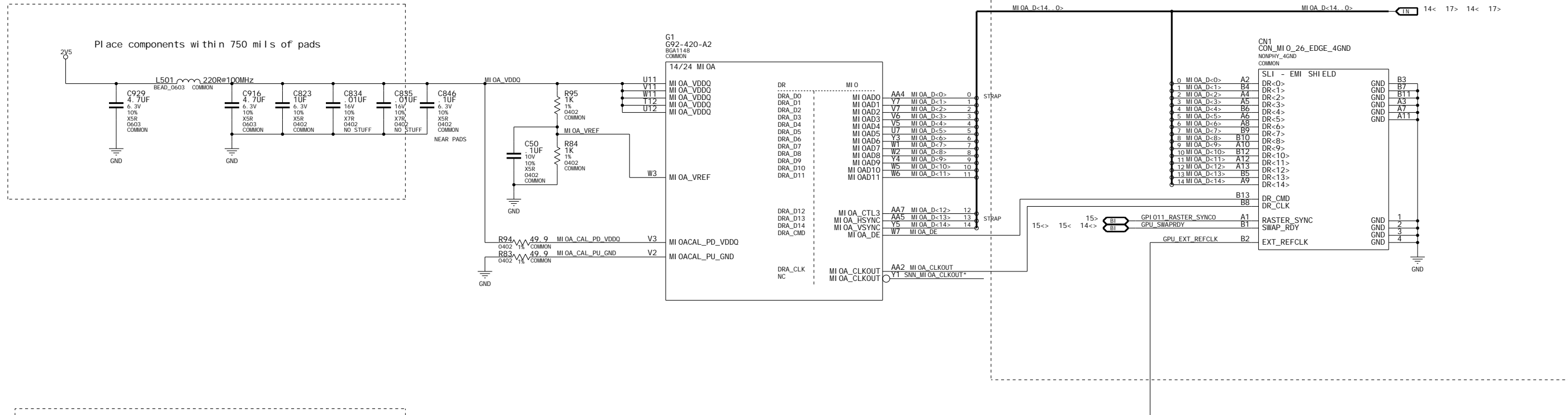
DACB NET RULES

NET		NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
	DACB_PR	1	75OHM	
	DACB_PR_F	1	75OHM	
	DACB_Y	1	75OHM	
	DACB_Y_F	1	75OHM	
	DACB_PB	1	75OHM	
	DACB_PB_F	1	75OHM	
NET		VOLTAGE	MAX_CURRENT	MIN_WIDTH
	DACB_VDD	3.30000V	0.200A	12.0MIL
	DACB_VREF			12.0MIL
	DACB_RSET			12.0MIL
	TV_GND1	0.000000V		12.0MIL










ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

## MI 0 Feature Connector



## MI 0 NET RULES

	NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
14< 17>	 M I O A_D<14...0>	1	50OHM	
	 M I O A_CLKOUT	1	50OHM	
	 M I O A_DE	1	50OHM	
	 M I O B_CLKOUT	1	50OHM	
14< 17>	 M I O B_D<14...0>	1	50OHM	
	 M I O B_DE	1	50OHM	
	 GPU_EXT_REFCLK	1	50OHM	

NET		VOLTAGE	MAX_CURRENT	MI_N_WI_DTH
1IN	MI_OA_VDDO	2.50000V	1.0A	30.0mI/L
1IN	MI_OA_VREF	1.25000V		12.0mI/L
1IN	MI_OACAL_PD_VDDO	2.50000V		12.0mI/L
1IN	MI_OACAL_PU_GND	0.000000V		12.0mI/L
1IN	MI_OB_VDDO	3.30000V	0.3A	12.0mI/L
1IN	MI_OB_VREF	1.65000V		12.0mI/L
1IN	MI_OBCAL_PD_VDDO	3.30000V		12.0mI/L
1IN	MI_OBCAL_PU_GND	0.000000V		12.0mI/L

ASSEMBLY	P392 - SKU1
PAGE DETAIL	Multi-use IO(MIO) Interface

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

Page15: MI SC: GPIO, I2C, BIOS, PLL, and XTAL

PLLVD D/VI D\_PLLVD D

I2CC / I2CH(+ HDCP ROM) / I2CS

MISC NET RULES

NET	NV_CRI TICAL	NV_I MPEDANCE	DIFFPAIR
I2CC_SCL	3	50OHM	
I2CC_SDA	3	50OHM	
I2CC_SCL_R	3	50OHM	
I2CC_SDA_R	3	50OHM	
I2CH_SCL	3	50OHM	
I2CH_SDA	3	50OHM	
I2CS_SCL	3	50OHM	
I2CS_SDA	3	50OHM	
I2CS_SCL_R	3	50OHM	
I2CS_SDA_R	3	50OHM	
ROM_CS*	3	50OHM	
ROM_SI	3	50OHM	
ROM_SO	3	50OHM	
ROM_SCLK	3	50OHM	
GPU_BUFRST*	3	50OHM	
GPU_SWAPRDY	3	50OHM	
GPU_TESTMODE	3	50OHM	
GPIO0_DV1_AB_HPD	3	50OHM	
GPIO1_DV1_CD_DP_HPD	3	50OHM	
GPIO4_FAN_PWM	3	50OHM	
GPIO5_VSELO	3	50OHM	
GPIO6_VSEL1	3	50OHM	
GPIO7_FAN_TACH	3	50OHM	
GPIO8_THERM_OVERT*	3	50OHM	
GPIO9_THERM_ALERT*	3	50OHM	
GPIO11_RASTER_SYNC	3	50OHM	
GPIO12_POWER_ALERT*	3	50OHM	
GPIO13_DP_KEEP	3	50OHM	
DP_XTAL_IN	1	50OHM	
XTAL_SSI_N	1	50OHM	
XTAL_IN	1	50OHM	
XTAL_OUT	1	50OHM	
XTAL_OUTBUFF	1	50OHM	
NET	VOLTAGE	MAX_CURRENT	MI N_WI DTH
GPU_PLLVD D	1.20000V	0.05A	12.0MI L
GPU_PL LAVD D	1.20000V	0.05A	12.0MI L
GPU_VI D_PL LAVD D	1.20000V	0.05A	12.0MI L
GPU_H_PL LAVD D	1.20000V	0.05A	12.0MI L

GPIO

GPIO Assignment Table

GPIO	I/O	Function
0	IN	DV1_HOTPLUG_DET_A
1	IN	DV1/DP_HOTPLUG_DET_C
2	IN	RAMCFG0
3	IN	RAMCFG1
4	OUT	FAN_PWM
5	OUT	VOLTAGE_SELECT_0
6	OUT	VOLTAGE_SELECT_1
7	IN	TACHOMETER_INPUT
8	OUT	THERM_OVERT*
9	IN	THERM_ALERT*
10	IN	RAMCFG2
11	I/O	RASTER (SLI) SYNC - 0
12	IN	POWER_ALERT*
13	IN	RAMCFG3
14	I/O	RASTER (SLI) SYNC - 1

XTAL

ROM / MI SC

(BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)

ASSEMBLY	P392 - SKU1
PAGE DETAIL	MISC: GPIO, I2C, BIOS, PLL, and XTAL

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

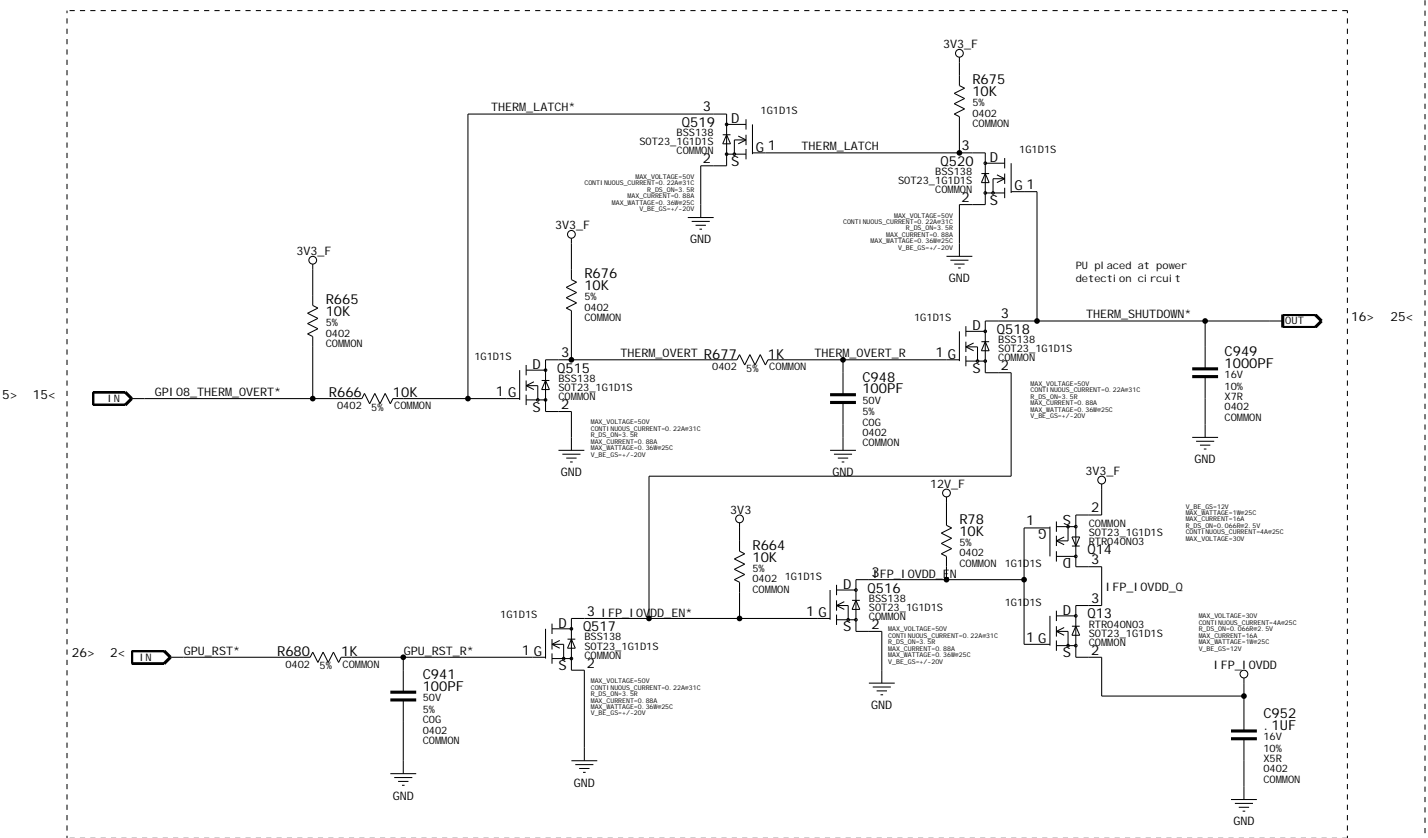
2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA



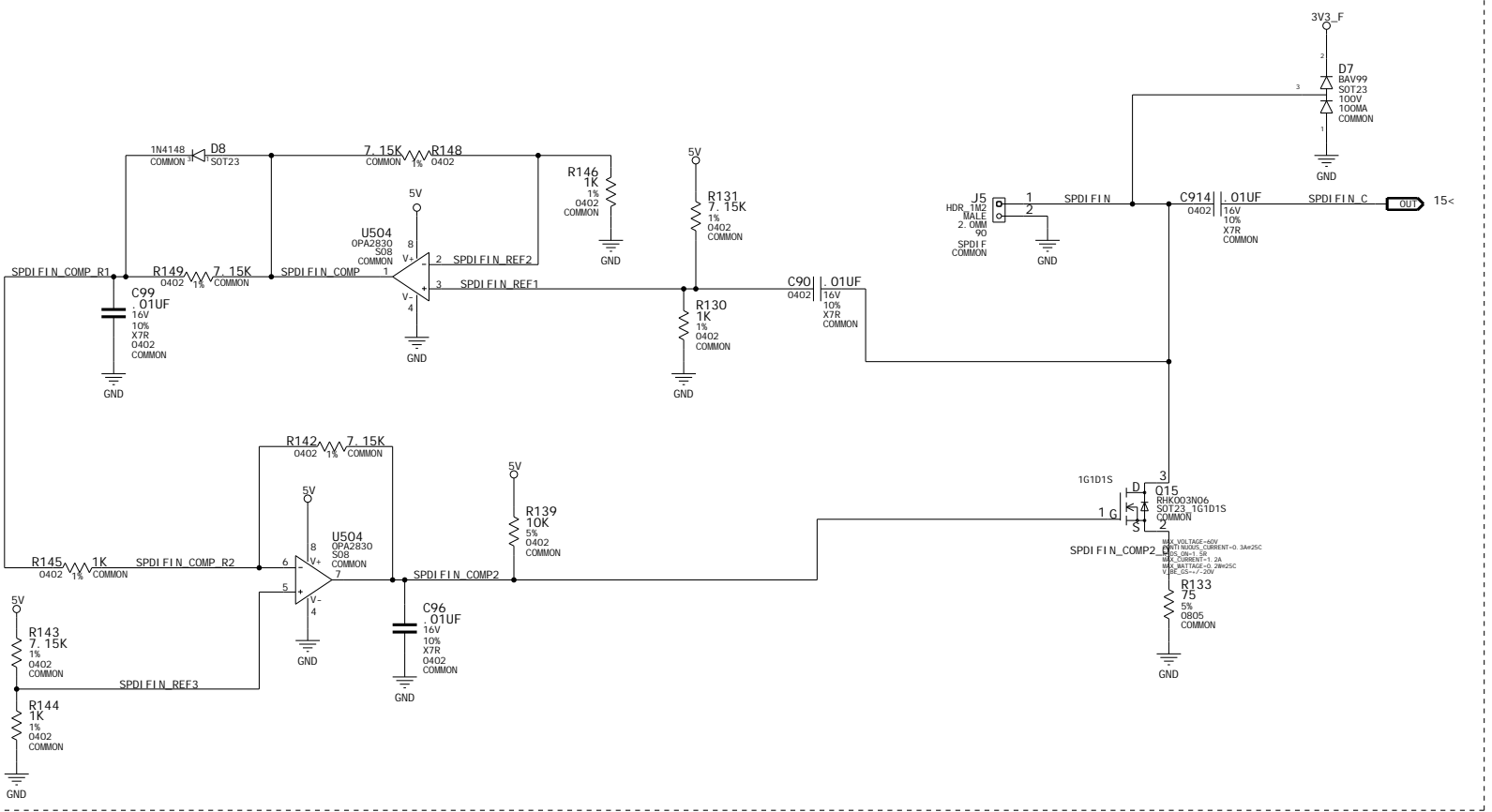
NV\_PN 600-10392-0001-200 A

ID	dest gn	PAGE	15 OF 26
NAME	etal	DATE	17-JAN-2008

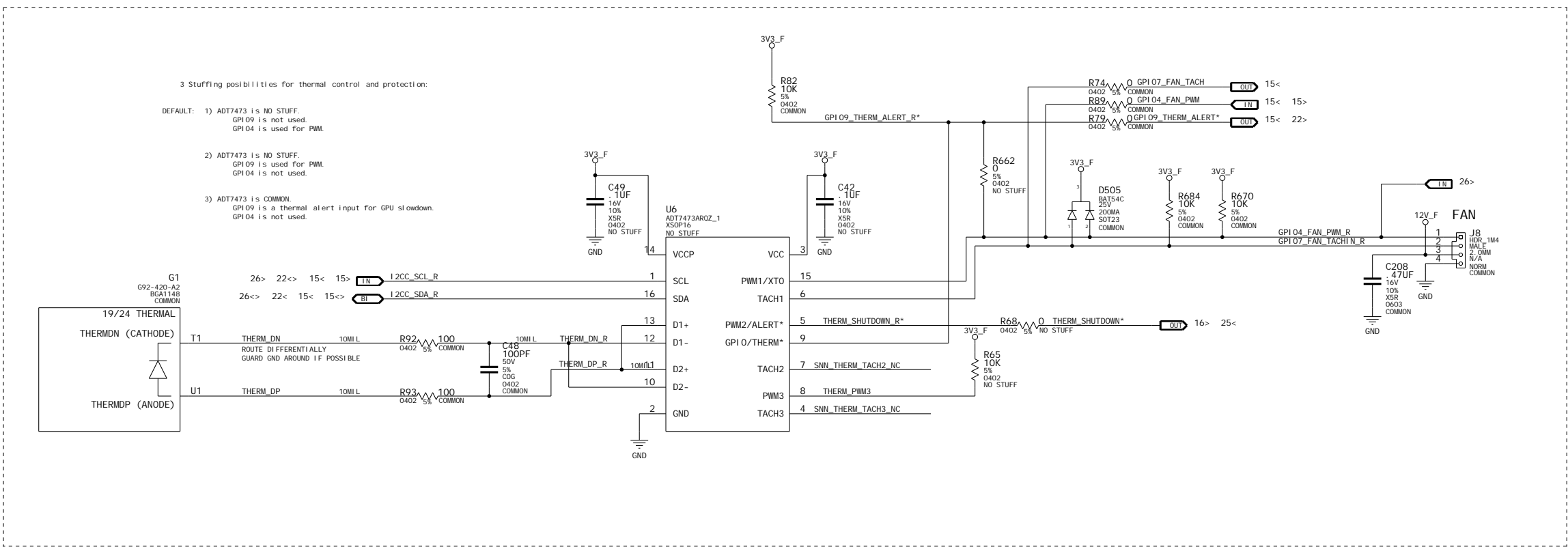
THERMAL PROTECTION & TMDs BACKDRIVE PROTECTION



SPDIF INPUT / DETECTION

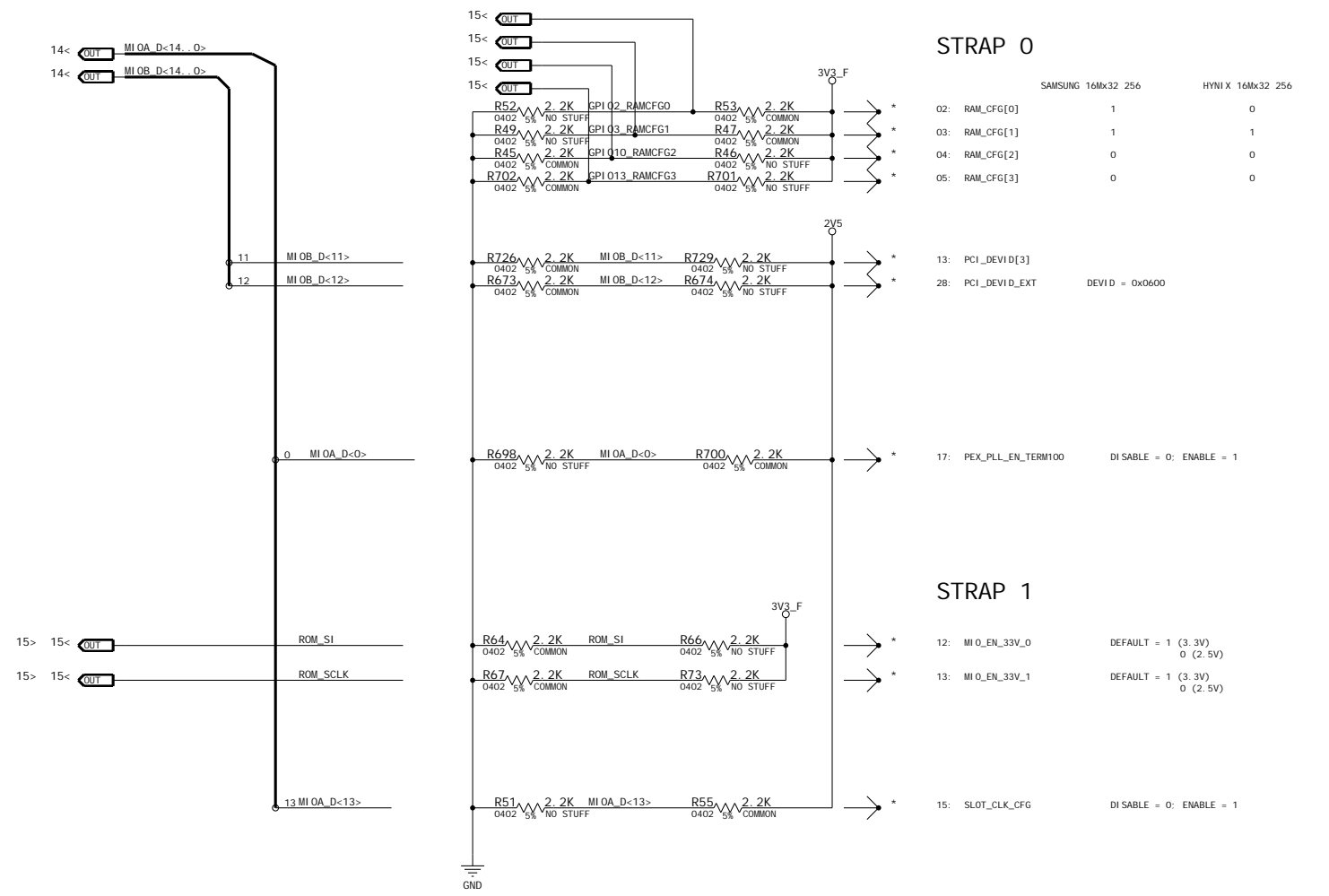


THERMAL CONTROL

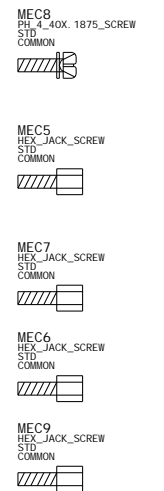
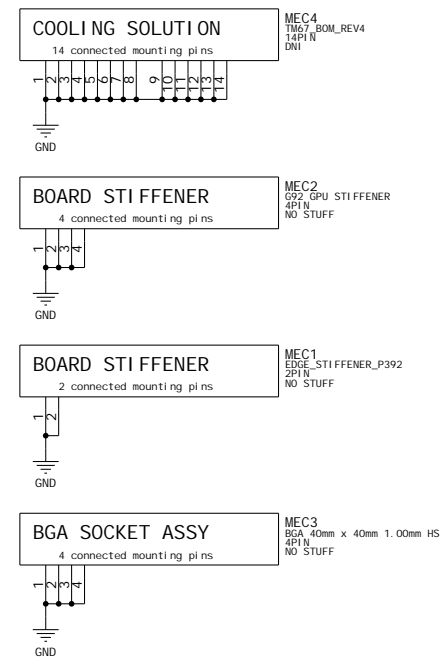
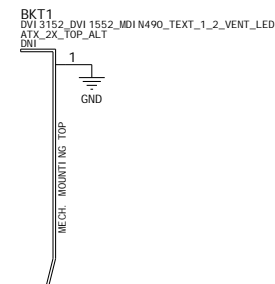




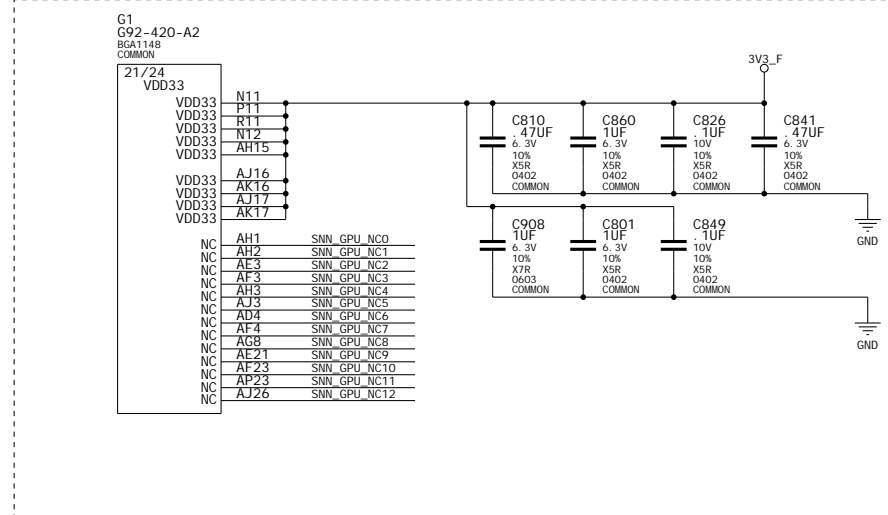
## STRAPS



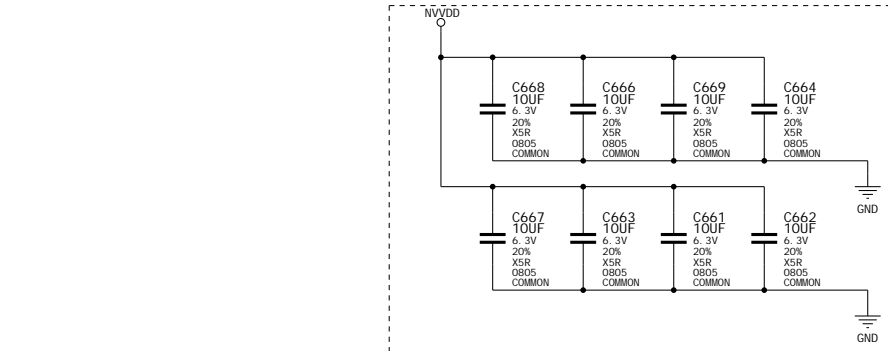
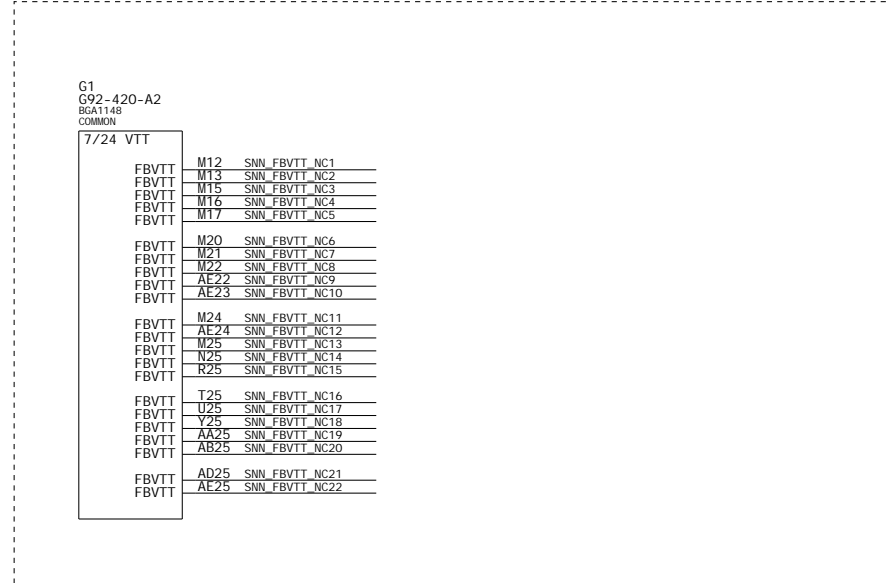
## MECHANICAL



## VDD33

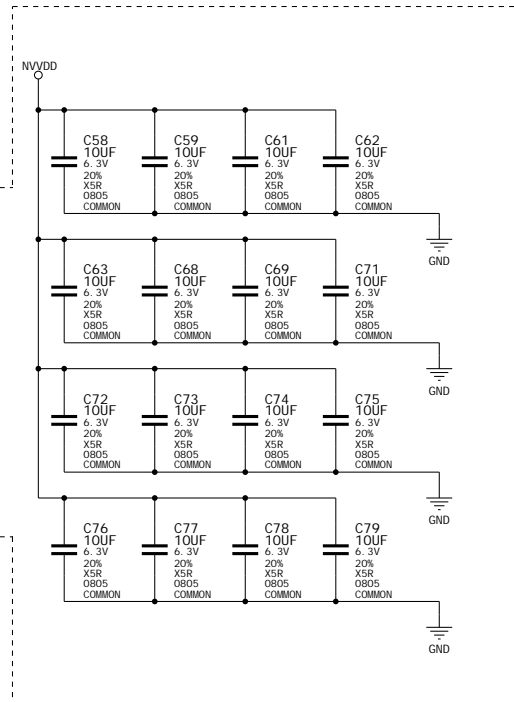
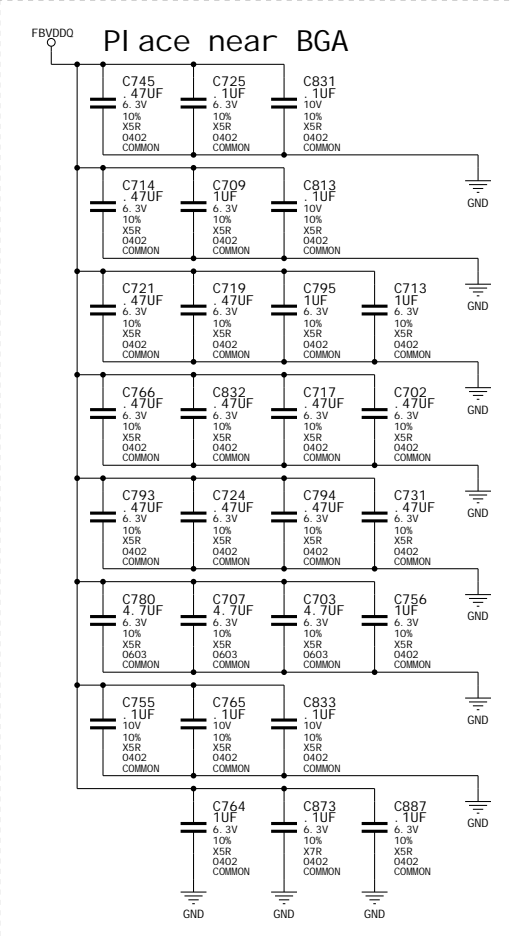


## FBVTT

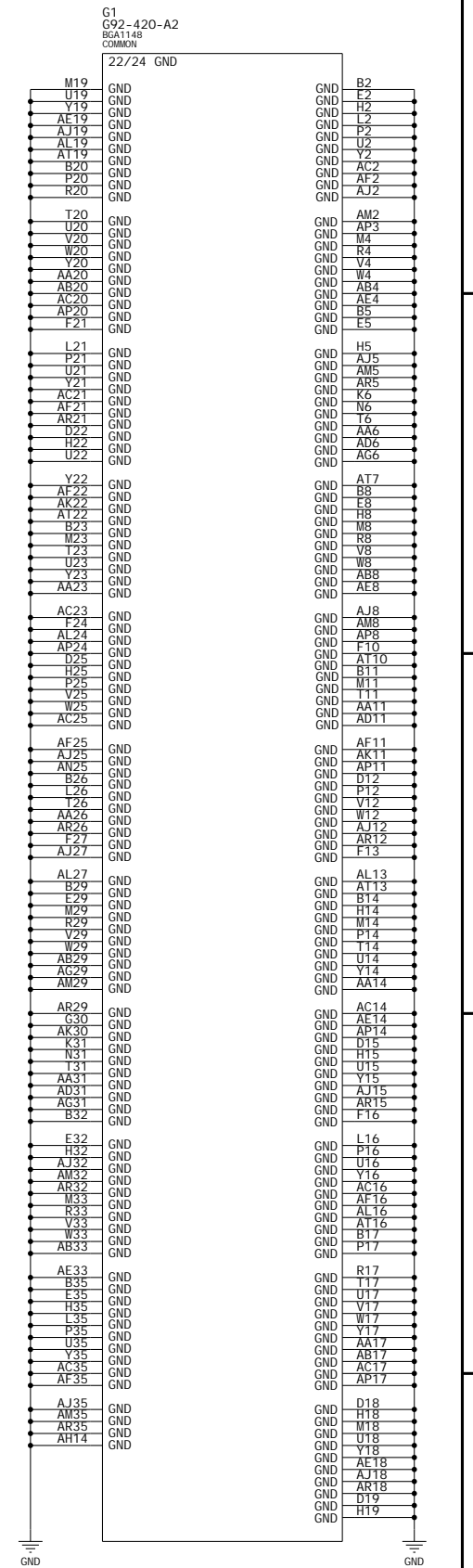
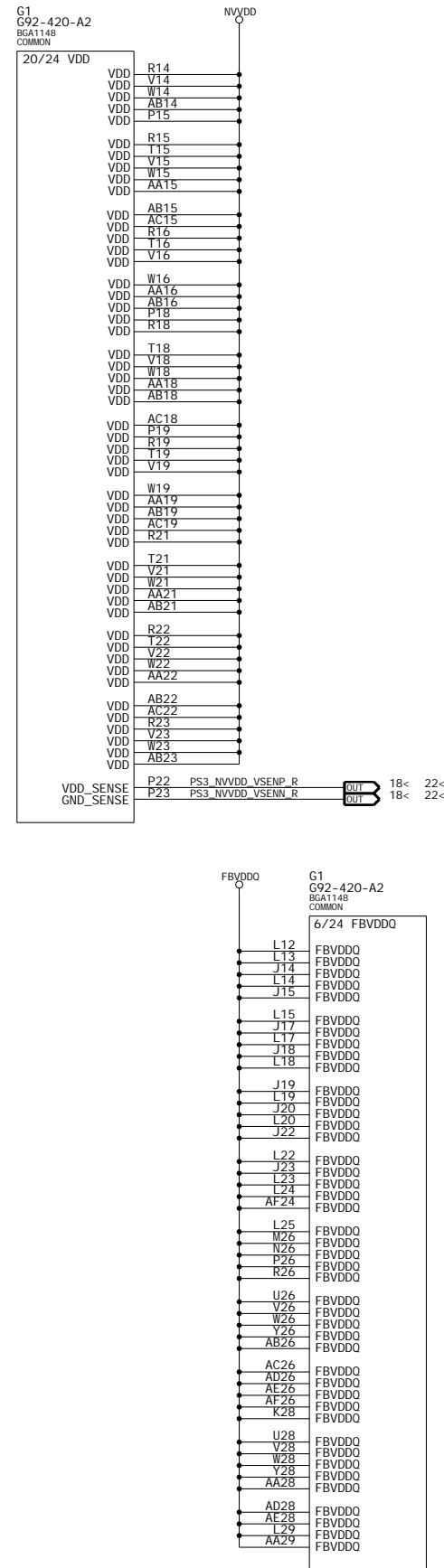
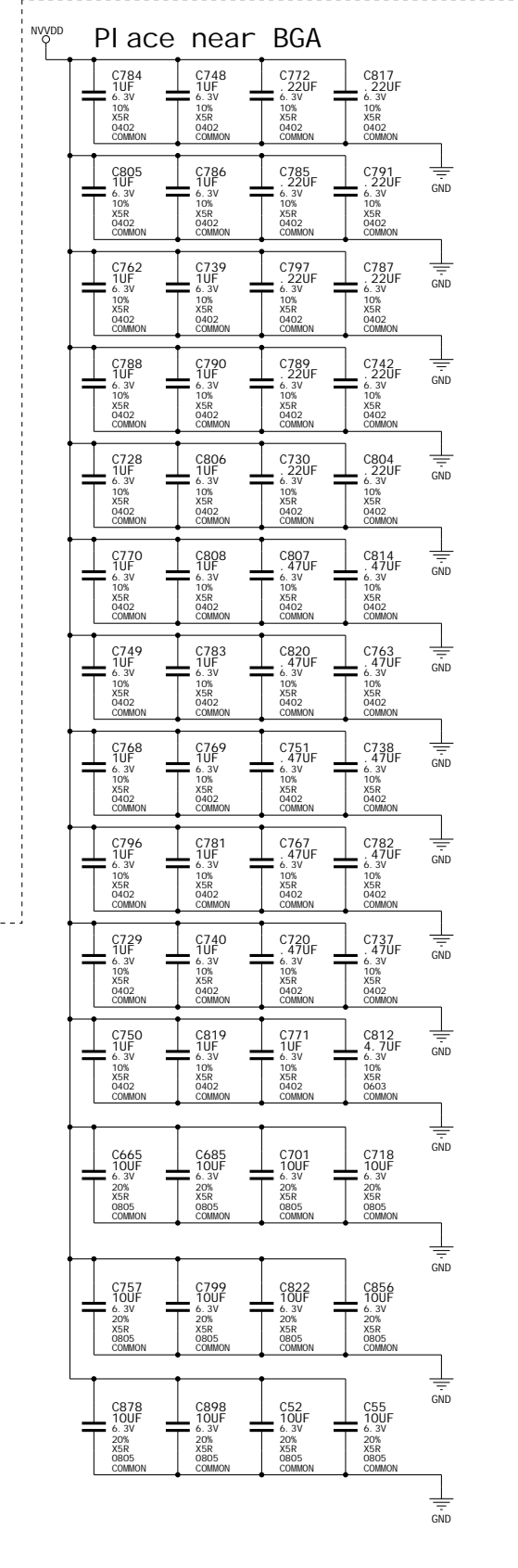


		NET	NV_CRI TICAL	NV_I MPEDANCE	DI FFPAI R
22<	18>	PS3_NVVDD_VSENP_R	1	80DI FF	PS3_NVVDD_VSEN
22<	18>	PS3_NVVDD_VSENN_R	1	80DI FF	PS3_NVVDD_VSEN

## FBVDDQ



## NVVDD

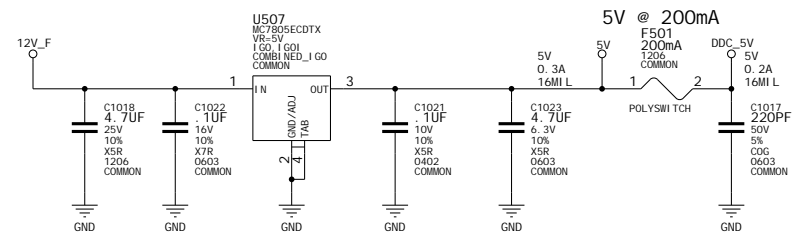


NVI DI A CORPORATI ON

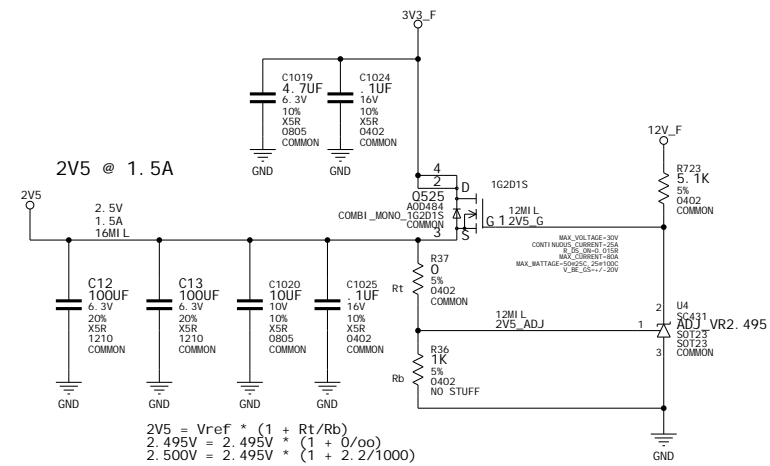
2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA			
NV_PN	600-10392-0001-200 A		
ID	desi gn	PAGE	18 OF 26
NAME	etal	DATE	17-JAN-2008

## 5V and DDC5V Supply



2V5



ASSEMBLY	P392 - SKU1
PAGE DETAIL	Power Supply: 5V, 2V5

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

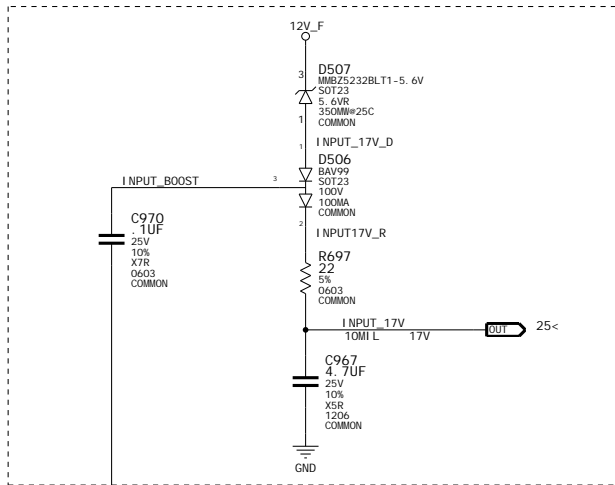
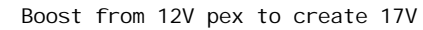
2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

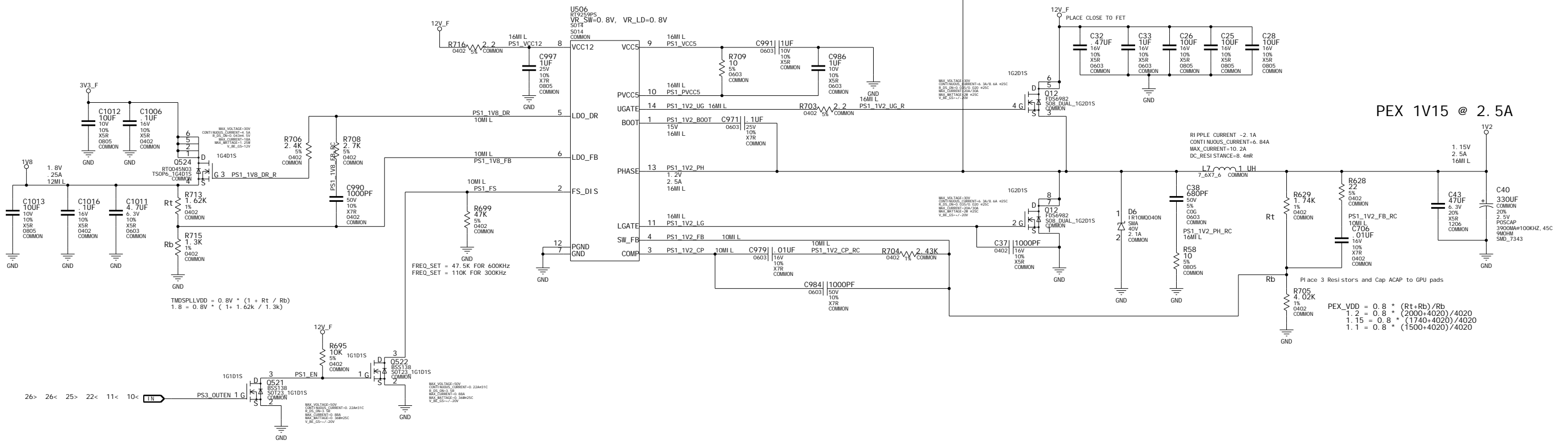
NV_PN	600-10392-0001-200 A
-------	----------------------


ID	design	PAGE	19 OF 26
NAME	etal	DATE	17-JAN-2008





Place these components near PEX regulator, then run 10MIL trace across the board for INPUT\_17V.



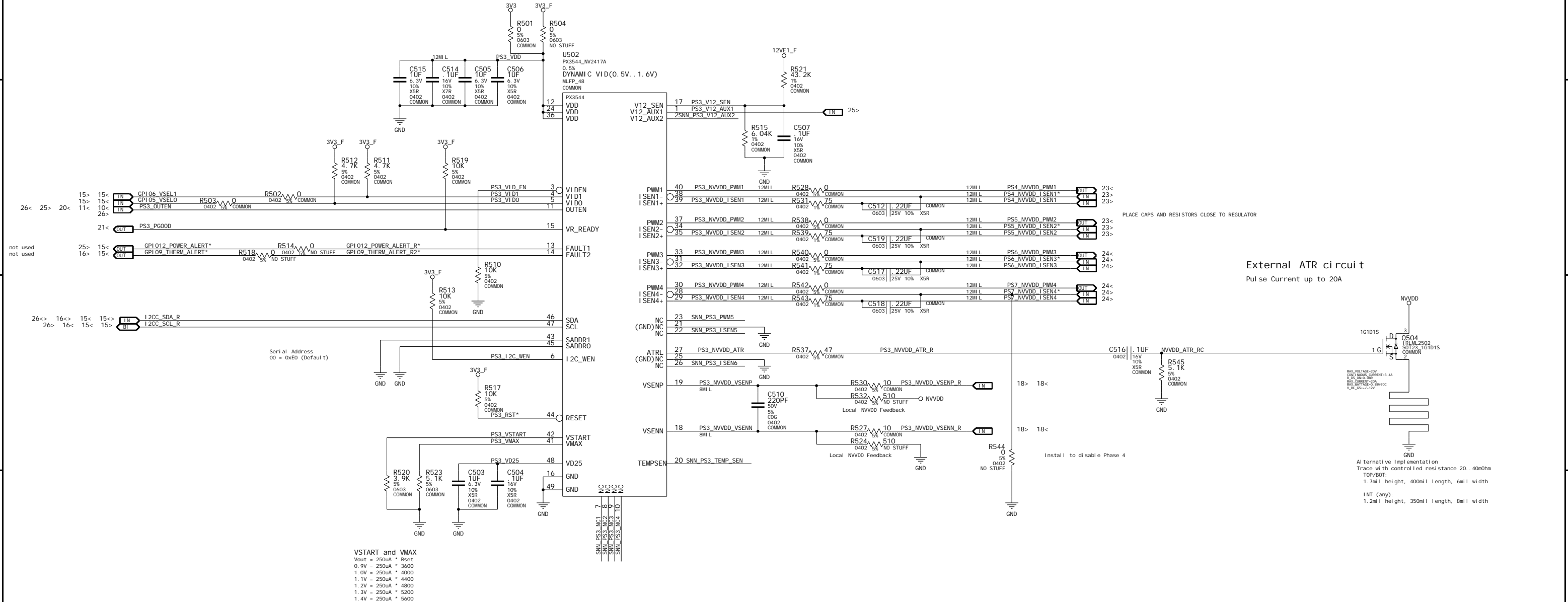
NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-10392-0001-200 A		
ID	desi gn	PAGE	20 OF 26
NAME	etal	DATE	17-JAN-2008

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.



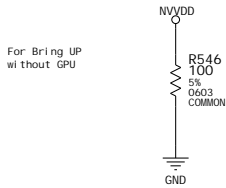
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

Page22: Power Supply: NVVDD Regulator



PHASE 1

PHASE 2

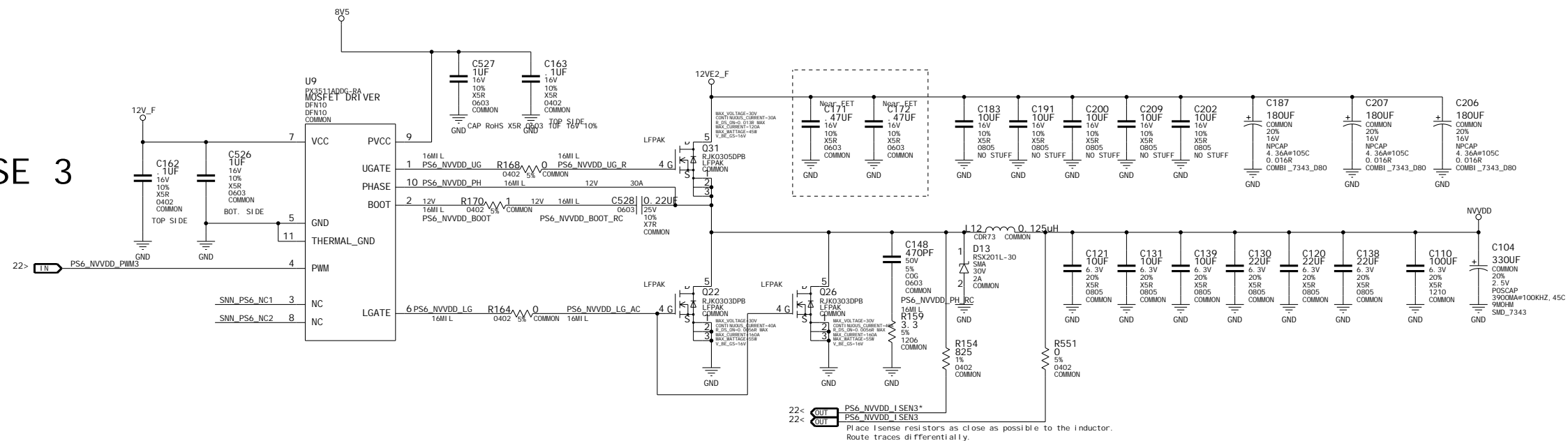


ASSEMBLY	P392 - SKU1
PAGE DETAIL	Power Supply: NVVDD Phase 1, 2

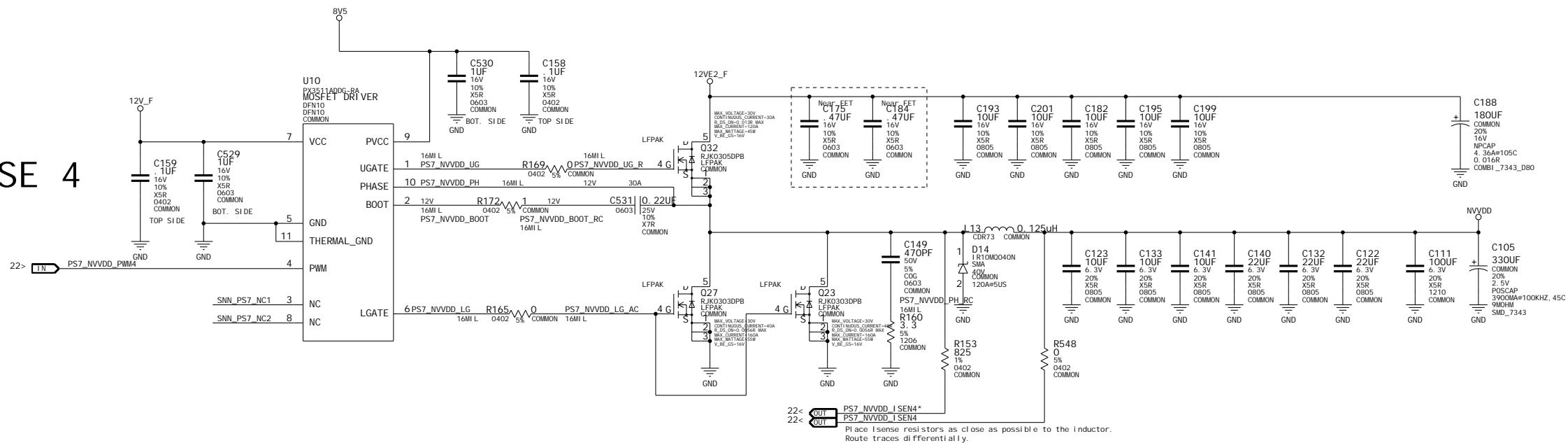
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-10392-0001-200 A		
ID	dest gn	PAGE	23 OF 26
NAME	etal	DATE	17-JAN-2008

## PHASE 3

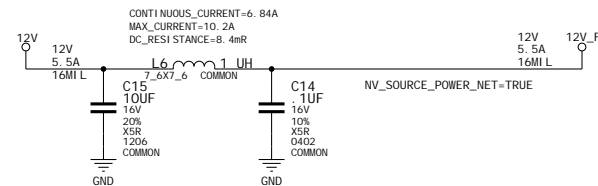


## PHASE 4

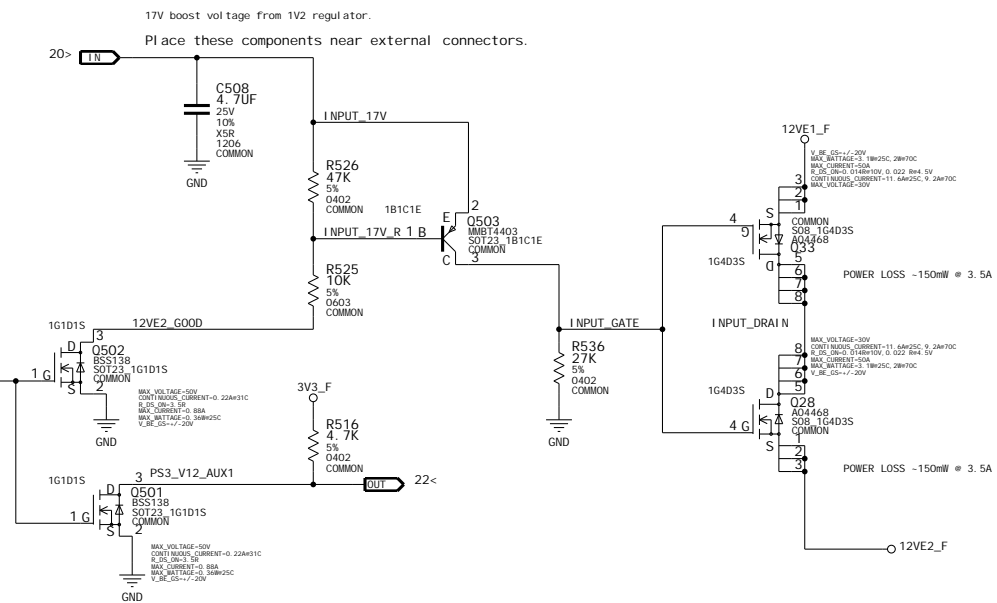




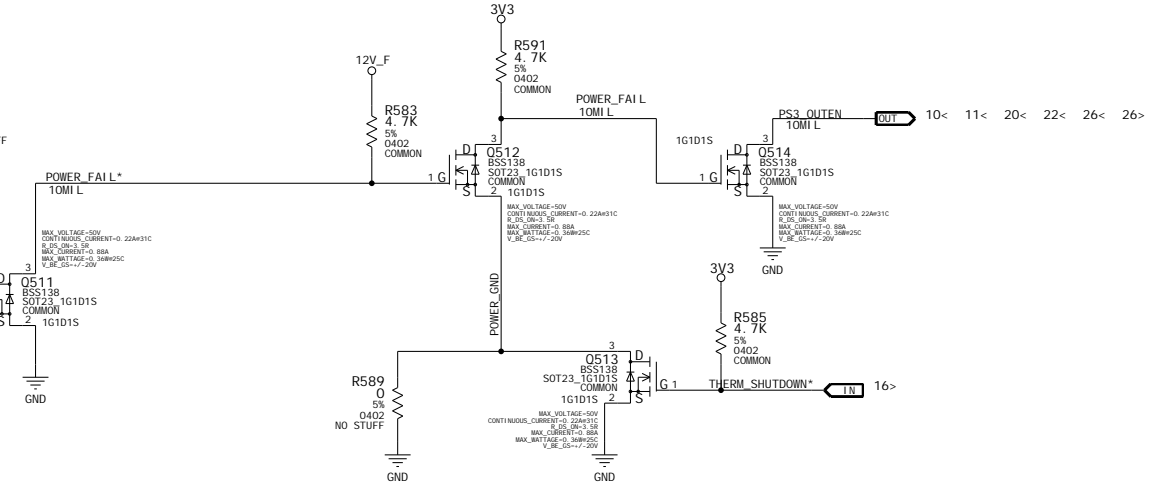
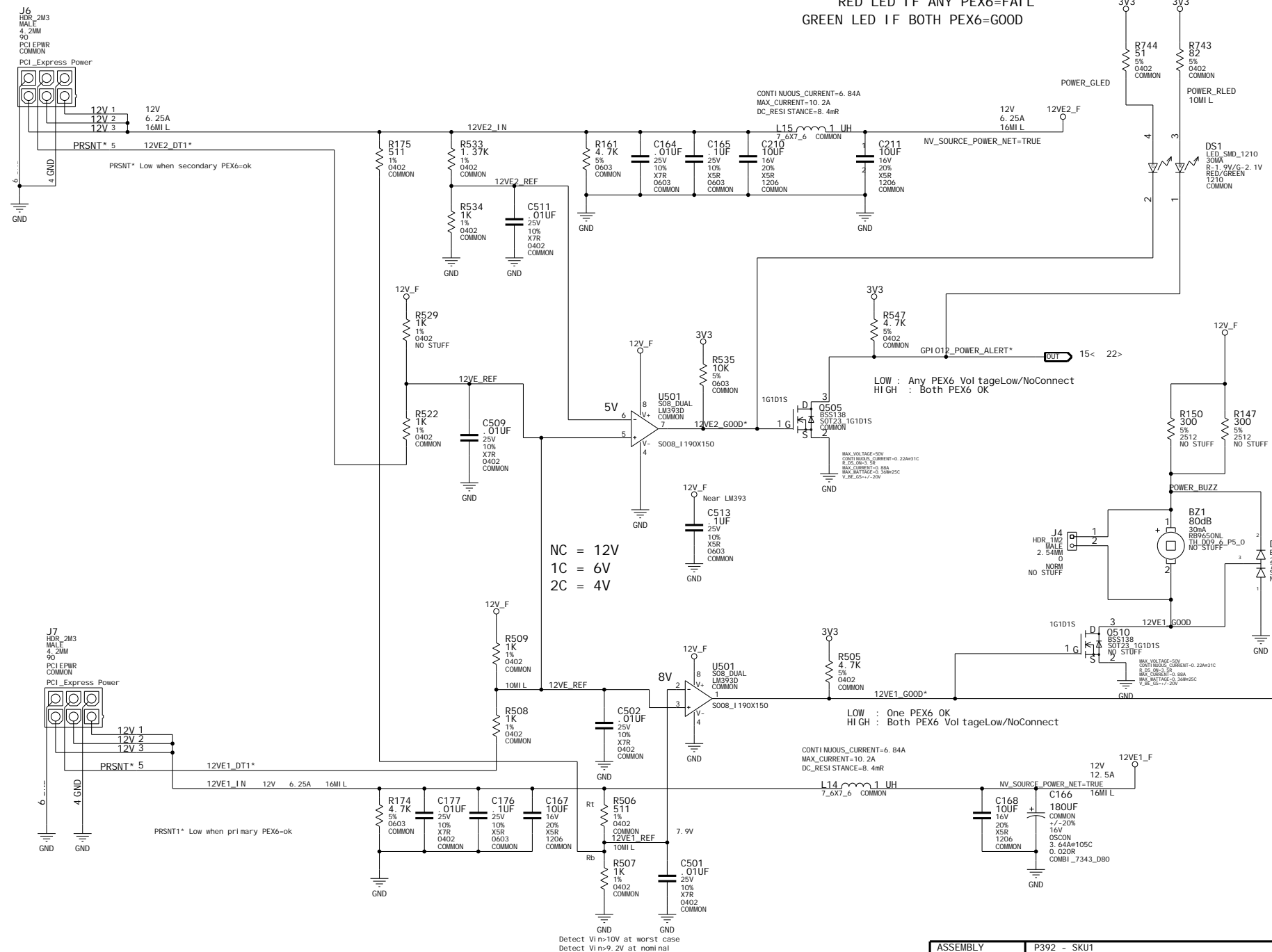
## POWER FILTER 12V



## BOOST CIRCUIT FOR PEX\_EXT RAIL MERGER



RED LED IF ANY PEX6=FAIL  
GREEN LED IF BOTH PEX6=GOOD

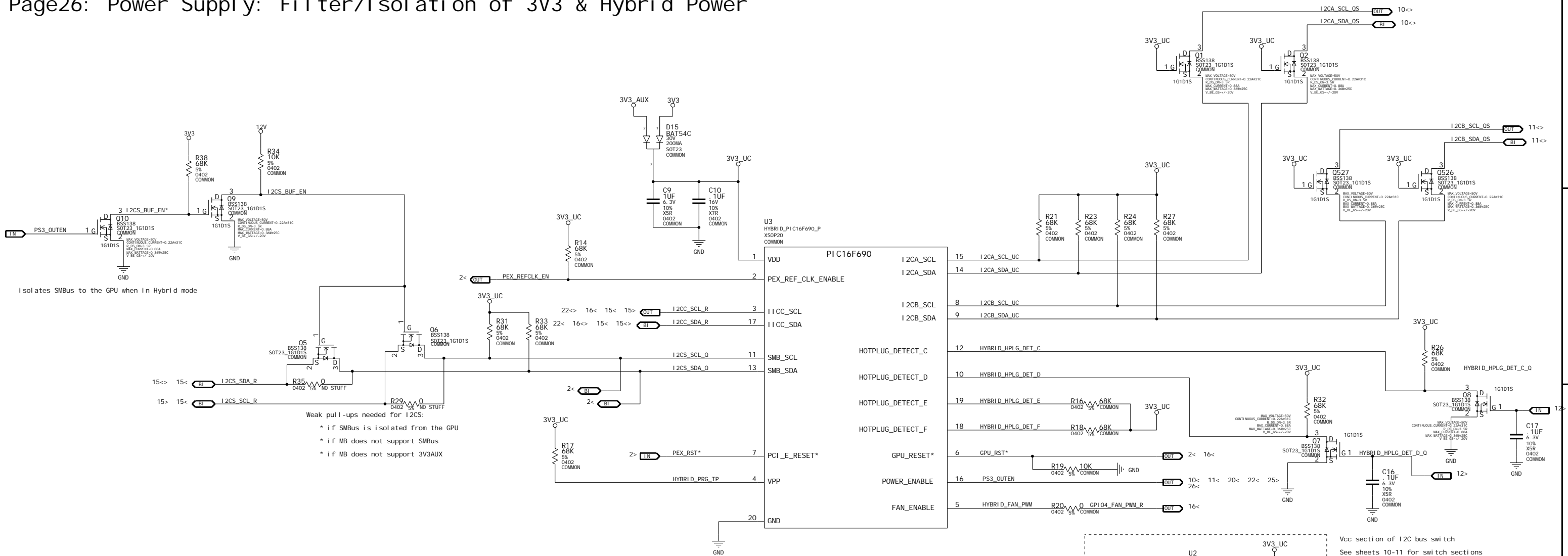


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

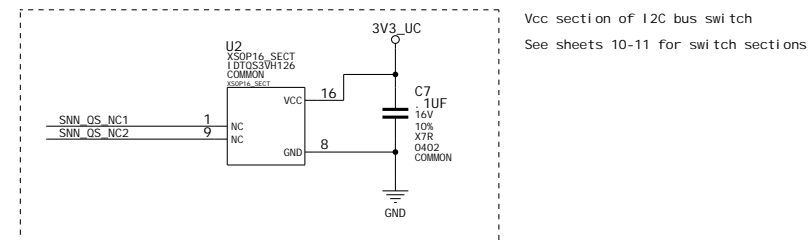
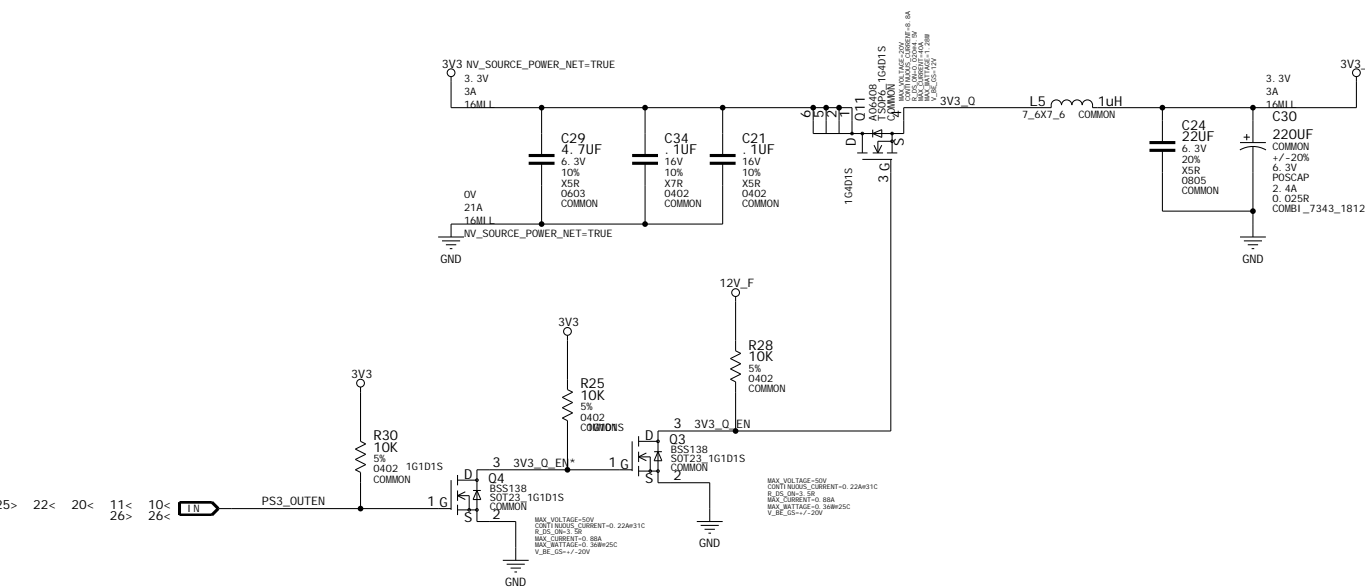
ASSEMBLY	P392 - SKU1
PAGE DETAIL	Power Supply: Filter/Detection of 3V3, 12V, 12V_PEX

<b>NV I D I A   C O R P O R A T I O N</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
<b>NV_PN      600-10392-0001-200    A</b>			
1D	desl gn	PAGE	25 OF 26
NAME	etal	DATE	17-JAN-2008

## Page26: Power Supply: Filter/Isolation of 3V3 &amp; Hybrid Power



## POWER FILTER 3V3



ASSEMBLY	P392 - SKU1
PAGE DETAIL	Power Supply: Filter/Isolation of 3V3 & Hybrid Power

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV_PN	600-10392-0001-200 A
-------	----------------------

IP: 192.168.1.100 PAGE: 26 OF 26

NAME	etal	DATE	17-JAN-20
------	------	------	-----------

