NV41/42/G70-P317, 256bit, 4M/8Mx32bit DDR3

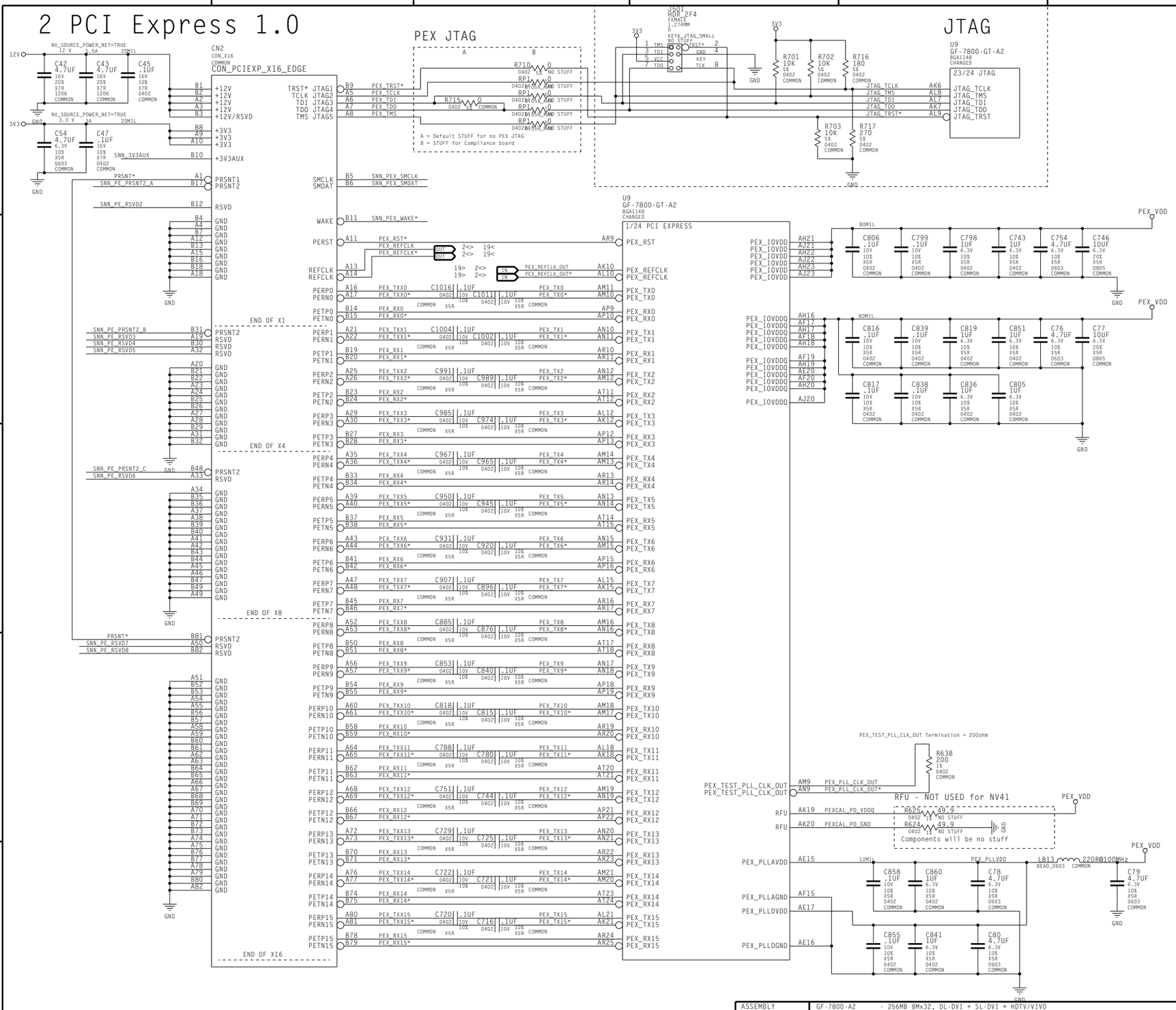
Page Overview

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	Overview

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10317-0002-100		
ID	design	PAGE	1 OF 28
NAME	John Lam	DATE	31-MAY-2005

2 PCI Express 1.0



3GIO NET RULES

NET	IMPEDANCE	CRITICAL	DIFFPAIR
PEX_REFCLK	100DIFF	1	PEX_REFCLK_OUT
PEX_REFCLK*	100DIFF	1	PEX_REFCLK_OUT
PEX_REFCLK_OUT	100DIFF	1	PEX_REFCLK_OUT
PEX_REFCLK_OUT*	100DIFF	1	PEX_REFCLK_OUT
PEX_TXO	100DIFF	1	PEX_TXO
PEX_TXO*	100DIFF	1	PEX_TXO
PEX_TX1	100DIFF	1	PEX_TX1
PEX_TX1*	100DIFF	1	PEX_TX1
PEX_TX2	100DIFF	1	PEX_TX2
PEX_TX2*	100DIFF	1	PEX_TX2
PEX_TX3	100DIFF	1	PEX_TX3
PEX_TX3*	100DIFF	1	PEX_TX3
PEX_TX4	100DIFF	1	PEX_TX4
PEX_TX4*	100DIFF	1	PEX_TX4
PEX_TX5	100DIFF	1	PEX_TX5
PEX_TX5*	100DIFF	1	PEX_TX5
PEX_TX6	100DIFF	1	PEX_TX6
PEX_TX6*	100DIFF	1	PEX_TX6
PEX_TX7	100DIFF	1	PEX_TX7
PEX_TX7*	100DIFF	1	PEX_TX7
PEX_TX8	100DIFF	1	PEX_TX8
PEX_TX8*	100DIFF	1	PEX_TX8
PEX_TX9	100DIFF	1	PEX_TX9
PEX_TX9*	100DIFF	1	PEX_TX9
PEX_TX10	100DIFF	1	PEX_TX10
PEX_TX10*	100DIFF	1	PEX_TX10
PEX_TX11	100DIFF	1	PEX_TX11
PEX_TX11*	100DIFF	1	PEX_TX11
PEX_TX12	100DIFF	1	PEX_TX12
PEX_TX12*	100DIFF	1	PEX_TX12
PEX_TX13	100DIFF	1	PEX_TX13
PEX_TX13*	100DIFF	1	PEX_TX13
PEX_TX14	100DIFF	1	PEX_TX14
PEX_TX14*	100DIFF	1	PEX_TX14
PEX_TX15	100DIFF	1	PEX_TX15
PEX_TX15*	100DIFF	1	PEX_TX15
PEX_RXO	100DIFF	1	PEX_RXO
PEX_RXO*	100DIFF	1	PEX_RXO
PEX_RX1	100DIFF	1	PEX_RX1
PEX_RX1*	100DIFF	1	PEX_RX1
PEX_RX2	100DIFF	1	PEX_RX2
PEX_RX2*	100DIFF	1	PEX_RX2
PEX_RX3	100DIFF	1	PEX_RX3
PEX_RX3*	100DIFF	1	PEX_RX3
PEX_RX4	100DIFF	1	PEX_RX4
PEX_RX4*	100DIFF	1	PEX_RX4
PEX_RX5	100DIFF	1	PEX_RX5
PEX_RX5*	100DIFF	1	PEX_RX5
PEX_RX6	100DIFF	1	PEX_RX6
PEX_RX6*	100DIFF	1	PEX_RX6
PEX_RX7	100DIFF	1	PEX_RX7
PEX_RX7*	100DIFF	1	PEX_RX7
PEX_RX8	100DIFF	1	PEX_RX8
PEX_RX8*	100DIFF	1	PEX_RX8
PEX_RX9	100DIFF	1	PEX_RX9
PEX_RX9*	100DIFF	1	PEX_RX9
PEX_RX10	100DIFF	1	PEX_RX10
PEX_RX10*	100DIFF	1	PEX_RX10
PEX_RX11	100DIFF	1	PEX_RX11
PEX_RX11*	100DIFF	1	PEX_RX11
PEX_RX12	100DIFF	1	PEX_RX12
PEX_RX12*	100DIFF	1	PEX_RX12
PEX_RX13	100DIFF	1	PEX_RX13
PEX_RX13*	100DIFF	1	PEX_RX13
PEX_RX14	100DIFF	1	PEX_RX14
PEX_RX14*	100DIFF	1	PEX_RX14
PEX_RX15	100DIFF	1	PEX_RX15
PEX_RX15*	100DIFF	1	PEX_RX15
PEX_PLL_CLK_OUT	100DIFF	1	PEX_PLL_CLK_OUT
PEX_PLL_CLK_OUT*	100DIFF	1	PEX_PLL_CLK_OUT

Matching Rule of Thumb

4 inch from Top of Gold Fingers to GPU
*2 inch Lane to Lane Skew

*No real Skew rule, but reducing the skew will minimize latency

NET	VOLTAGE
PEX_PLLVDD	1.2 V

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	PCI Express 1.0

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3 FrameBuffer: GPU Partition A/B

NET RULES

NET	VOLTAGE
FBA_PLLVDD	3.3 V
FBB_PLL_VDD	3.3 V
FBAB_PLLAVDD	1.4 V

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	MEMORY: GPU Partition A/B

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4 FrameBuffer: GPU Partition C/D

NET RULES

NET	VOLTAGE
FBC_PLLVDD	3.3 V
FBD_PLLVDD	3.3 V
FBCD_AVDD	1.4 V

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	MEMORY: GPU Partition C/D

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NV_PN	600-10317-0002-100		
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NAME	John Lam	DATE	31-MAY-2005

5 FrameBuffer: Partition A 8Mx32 BGA144 DDR3

FBA Partition

A-CSO-LOW-32bit

U13
DDR3BGA144
PACK_TYPE=BGA144
VERSION=BGA144
CHANGED

Low Sub-Partition

5< 3> IN FBA_CMD<25..0>

15	FBA_CMD<15>	M5	RAS
25	FBA_CMD<25>	N6	CAS
9	FBA_CMD<9>	N9	WE
8 (CS0)	FBA_CMD<8>	M10	CS
1	FBA_CMD<1>	N2	A0
3	FBA_CMD<3>	N3	A1
2	FBA_CMD<2>	M3	A2
0	FBA_CMD<0>	L3	A3
24	FBA_CMD<24>	L12	A4
22	FBA_CMD<22>	M12	A5
21	FBA_CMD<21>	N12	A6
23	FBA_CMD<23>	N13	A7
19	FBA_CMD<19>	N11	A8
20	FBA_CMD<20>	M11	A9
17	FBA_CMD<17>	M4	A10
16	FBA_CMD<16>	N4	A11
14	FBA_CMD<14>	L9	NC/A<12>
10	FBA_CMD<10>	N5	BA<0>
18	FBA_CMD<18>	N10	BA<1>
	SNN_FBA0_BA2	L6	NC/BA<2>
11	FBA_CMD<11>	M7	CKE
	FBA_CLK0	N7	CLK
	FBA_CLK0*	N8	CLK
	SNN_FBA0_NC1	E3	NC/RFU
	SNN_FBA0_NC2	E12	NC/RFU
	SNN_FBA0_NC3	M8	NC/RFU
12	FBA_CMD<12>	M6	RESET
	FBA_ZQ0	M9	ZQ
		F6	THERM
		F7	THERM
		F8	THERM
		F9	THERM
		G6	THERM
		G7	THERM
		G8	THERM
		G9	THERM
		H6	THERM
		H7	THERM
		H8	THERM
		H9	THERM
		J6	THERM
		J7	THERM
		J8	THERM
		J9	THERM

	VDD	D7	
	VDD	D8	
	VDD	E4	
	VDD	E11	
	VDD	L4	
	VDD	L7	
	VDD	L8	
	VDD	L11	
	VDDQ	C4	
	VDDQ	C5	
	VDDQ	C7	
	VDDQ	C8	
	VDDQ	C10	
	VDDQ	C11	
	VDDQ	F4	
	VDDQ	F11	
	VDDQ	G4	
	VDDQ	G11	
	VDDQ	H4	
	VDDQ	H11	
	VDDQ	J4	
	VDDQ	J11	
	VDDQ	K4	
	VDDQ	K11	
	VSSQ	B4	
	VSSQ	B11	
	VSSQ	D4	
	VSSQ	D5	
	VSSQ	D6	
	VSSQ	D9	
	VSSQ	D10	
	VSSQ	D11	
	VSSQ	E6	
	VSSQ	E9	
	VSSQ	F5	
	VSSQ	F10	
	VSSQ	G5	
	VSSQ	G10	
	VSSQ	H5	
	VSSQ	H10	
	VSSQ	J5	
	VSSQ	J10	
	VSSQ	K5	
	VSSQ	K10	
	VSS	E5	
	VSS	E7	
	VSS	E8	
	VSS	E10	
	VSS	K6	
	VSS	K7	
	VSS	K8	
	VSS	K9	
	VSS	L5	
	VSS	L10	
M2	FBA_VREF_DATA0		12MIL
M13	FBA_VREF_ADDR0		12MIL
	VREF		
	VREF		

CKE
R87 10K 5% 0402 COMMON
GND

RESET
R86 10K 5% 0402 COMMON
GND

R566 243 1% 0603 COMMON
GND

DDR3: ZQ = 6x desired output
Impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!

FBVDDQ

2	FBA_CMD<2>	121	R573
0	FBA_CMD<0>	121	R575
24	FBA_CMD<24>	121	R582
22	FBA_CMD<22>	121	R579
13	FBA_CMD<13>	121	R570
4	FBA_CMD<4>	121	R580
5	FBA_CMD<5>	121	R557
6	FBA_CMD<6>	121	R556
	FBA_CLK0	60.4	R565
	FBA_CLK0*	60.4	R564
	FBA_CLK1	60.4	R568
	FBA_CLK1*	60.4	R567

All: COMMON 1% 0402

H1 Sub-Partition

R89 511 1% 0402 COMMON
R88 1.3K 1% 0402 CHANGED
C84 .1UF 10V 10% X5R 0402 COMMON
R572 511 1% 0402 COMMON
R571 1.3K 1% 0402 CHANGED
C583 .1UF 10V 10% X5R 0402 COMMON

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 1.18K/(511 + 1.18K)

VREF:
M2 - DATA
M13 - ADDR

A-CSO-HI-32bit

U14
DDR3BGA144
PACK_TYPE=BGA144
VERSION=BGA144
CHANGED

	FBA_CMD<25..0>		
15	FBA_CMD<15>	M5	RAS
25	FBA_CMD<25>	N6	CAS
9	FBA_CMD<9>	N9	WE
8 (CS0)	FBA_CMD<8>	M10	CS
1	FBA_CMD<1>	N2	A0
3	FBA_CMD<3>	N3	A1
13	FBA_CMD<13>	M3	A2
4	FBA_CMD<4>	L3	A3
5	FBA_CMD<5>	L12	A4
6	FBA_CMD<6>	M12	A5
21	FBA_CMD<21>	N12	A6
23	FBA_CMD<23>	N13	A7
19	FBA_CMD<19>	N11	A8
20	FBA_CMD<20>	M11	A9
17	FBA_CMD<17>	M4	A10
16	FBA_CMD<16>	N4	A11
14	FBA_CMD<14>	L9	NC/A<12>
10	FBA_CMD<10>	N5	BA<0>
18	FBA_CMD<18>	N10	BA<1>
	SNN_FBA1_BA2	L6	NC/BA<2>
11	FBA_CMD<11>	M7	CKE
	FBA_CLK1	N7	CLK
	FBA_CLK1*	N8	CLK
	SNN_FBA1_NC1	E3	NC/RFU
	SNN_FBA1_NC2	E12	NC/RFU
	SNN_FBA1_NC3	M8	NC/RFU
12	FBA_CMD<12>	M6	RESET
	FBA_ZQ1	M9	ZQ
		F6	THERM
		F7	THERM
		F8	THERM
		F9	THERM
		G6	THERM
		G7	THERM
		G8	THERM
		G9	THERM
		H6	THERM
		H7	THERM
		H8	THERM
		H9	THERM
		J6	THERM
		J7	THERM
		J8	THERM
		J9	THERM

	VDD	D7	
	VDD	D8	
	VDD	E4	
	VDD	E11	
	VDD	L4	
	VDD	L7	
	VDD	L8	
	VDD	L11	
	VDDQ	C4	
	VDDQ	C5	
	VDDQ	C7	
	VDDQ	C8	
	VDDQ	C10	
	VDDQ	C11	
	VDDQ	F4	
	VDDQ	F11	
	VDDQ	G4	
	VDDQ	G11	
	VDDQ	H4	
	VDDQ	H11	
	VDDQ	J4	
	VDDQ	J11	
	VDDQ	K4	
	VDDQ	K11	
	VSSQ	B4	
	VSSQ	B11	
	VSSQ	D4	
	VSSQ	D5	
	VSSQ	D6	
	VSSQ	D9	
	VSSQ	D10	
	VSSQ	D11	
	VSSQ	E6	
	VSSQ	E9	
	VSSQ	F5	
	VSSQ	F10	
	VSSQ	G5	
	VSSQ	G10	
	VSSQ	H5	
	VSSQ	H10	
	VSSQ	J5	
	VSSQ	J10	
	VSSQ	K5	
	VSSQ	K10	
	VSS	E5	
	VSS	E7	
	VSS	E8	
	VSS	E10	
	VSS	K6	
	VSS	K7	
	VSS	K8	
	VSS	K9	
	VSS	L5	
	VSS	L10	
M2	FBA_VREF_DATA1		12MIL
M13	FBA_VREF_ADDR1		12MIL
	VREF		
	VREF		

R561 243 1% 0603 COMMON
GND

DDR3: ZQ = 6x desired output
Impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

FBVDDQ
R562 511 1% 0402 COMMON
R563 1.3K 1% 0402 CHANGED
C580 .1UF 10V 10% X5R 0402 COMMON
R552 511 1% 0402 COMMON
R549 1.3K 1% 0402 CHANGED
C562 .1UF 10V 10% X5R 0402 COMMON

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 1.18K/(511 + 1.18K)

NET RULES

NET	IMPEDANCE	CRITICAL	DIFFPAIR
5< 3> TL FBA_CLK0	100DIFF	1	FBA_CLK0
5< 3> TL FBA_CLK0*	100DIFF	1	FBA_CLK0
5< 3> TL FBA_CLK1	100DIFF	1	FBA_CLK1
5< 3> TL FBA_CLK1*	100DIFF	1	FBA_CLK1
5< 3> TL FBA_CMD<25..0>	40OHM	1	
5<> 3<> B1 FBAD<63..0>	40OHM	1	
5<> 3> B1 FBADQM<7..0>	40OHM	1	
5<> 3< B1 FBADQS_RN<7..0>	40OHM	1	
5<> 3> B1 FBADQS_WP<7..0>	40OHM	1	

144BGA CMD Mapping

CMD	ADDR	
CMD15	RAS*	
CMD25	CAS*	
CMD9	WE*	
CMD11	CKE	
CMD12	RESET	
CMD8	CS0*	
CMD7	CS1**notused	
CMD1	A<0>	
CMD3	A<1>	
CMD2	A<2>	Low Sub-Partition
CMD0	A<3>	
CMD24	A<4>	
CMD22	A<5>	
CMD13	A<2>	H1 Sub-Partition
CMD4	A<3>	
CMD5	A<4>	
CMD6	A<5>	
CMD21	A<6>	
CMD23	A<7>	
CMD19	A<8>	
CMD20	A<9>	
CMD17	A<10	
CMD16	A<11>	
CMD14	A<12>	
CMD10	BA0	
CMD18	BA1	

5<> 3<> B1 FBAD<63..0>

5<> 3> B1 FBADQM<7..0>

0	FBADQM<0>	C3	DQM
1	FBADQM<1>	J3	DQM
2	FBADQM<2>	C12	DQM
3	FBADQM<3>	J12	DQM
4	FBADQM<4>	J12	DQM
5	FBADQM<5>	J3	DQM
6	FBADQM<6>	C12	DQM
7	FBADQM<7>	C3	DQM

5<> 3< B1 FBADQS_RN<7..0>

0	FBADQS_RN<0>	B3	DQSR
1	FBADQS_RN<1>	H3	DQSR
2	FBADQS_RN<2>	B12	DQSR
3	FBADQS_RN<3>	H12	DQSR
4	FBADQS_RN<4>	H12	DQSR
5	FBADQS_RN<5>	H3	DQSR
6	FBADQS_RN<6>	B12	DQSR
7	FBADQS_RN<7>	B3	DQSR

5<> 3> B1 FBADQS_WP<7..0>

0	FBADQS_WP<0>	B2	DQSW
1	FBADQS_WP<1>	H2	DQSW
2	FBADQS_WP<2>	B13	DQSW
3	FBADQS_WP<3>	H13	DQSW
4	FBADQS_WP<4>	H13	DQSW
5	FBADQS_WP<5>	H2	DQSW
6	FBADQS_WP<6>	B13	DQSW
7	FBADQS_WP<7>	B2	DQSW

U13 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

0	FBAD<0>	B6	DQ0
1	FBAD<1>	C6	DQ1
2	FBAD<2>	B5	DQ2
3	FBAD<3>	B7	DQ3
4	FBAD<4>	C2	DQ4
5	FBAD<5>	D3	DQ5
6	FBAD<6>	E2	DQ6
7	FBAD<7>	D2	DQ7
8	FBAD<8>	G2	DQ0
9	FBAD<9>	G3	DQ1
10	FBAD<10>	F2	DQ2
11	FBAD<11>	F3	DQ3
12	FBAD<12>	J2	DQ4
13	FBAD<13>	K2	DQ5
14	FBAD<14>	K3	DQ6
15	FBAD<15>	L2	DQ7
16	FBAD<16>	B10	DQ0
17	FBAD<17>	B9	DQ1
18	FBAD<18>	B8	DQ2
19	FBAD<19>	C9	DQ3
20	FBAD<20>	C13	DQ4
21	FBAD<21>	E13	DQ5
22	FBAD<22>	D12	DQ6
23	FBAD<23>	D13	DQ7
24	FBAD<24>	G13	DQ0
25	FBAD<25>	F12	DQ1
26	FBAD<26>	F13	DQ2
27	FBAD<27>	G12	DQ3
28	FBAD<28>	K13	DQ4
29	FBAD<29>	K12	DQ5
30	FBAD<30>	L13	DQ6
31	FBAD<31>	J13	DQ7

U14 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

32	FBAD<32>	K12	DQ0
33	FBAD<33>	L13	DQ1
34	FBAD<34>	F13	DQ2
35	FBAD<35>	J13	DQ3
36	FBAD<36>	K13	DQ4
37	FBAD<37>	F12	DQ5
38	FBAD<38>	G12	DQ6
39	FBAD<39>	G13	DQ7
40	FBAD<40>	J2	DQ0
41	FBAD<41>	F3	DQ1
42	FBAD<42>	F2	DQ2
43	FBAD<43>	G2	DQ3
44	FBAD<44>	L2	DQ4
45	FBAD<45>	K2	DQ5
46	FBAD<46>	K3	DQ6
47	FBAD<47>	G3	DQ7
48	FBAD<48>	D13	DQ0
49	FBAD<49>	E13	DQ1
50	FBAD<50>	C13	DQ2
51	FBAD<51>	D12	DQ3
52	FBAD<52>	C9	DQ4
53	FBAD<53>	B9	DQ5
54	FBAD<54>	B8	DQ6
55	FBAD<55>	B10	DQ7
56	FBAD<56>	D3	DQ0
57	FBAD<57>	C2	DQ1
58	FBAD<58>	E2	DQ2
59	FBAD<59>	D2	DQ3
60	FBAD<60>	B5	DQ4
61	FBAD<61>	B7	DQ5
62	FBAD<62>	B6	DQ6
63	FBAD<63>	C6	DQ7

NVVDD
Reference Plane Transition Cap
C640 22UF 6.3V 20% X5R 0805 COMMON
C1074 120PF 50V 5% C0G 0402 COMMON
C1006 120PF 50V 5% C0G 0402 COMMON
GND

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	FrameBuffer: Partition A 8Mx32 BGA144 DDR3

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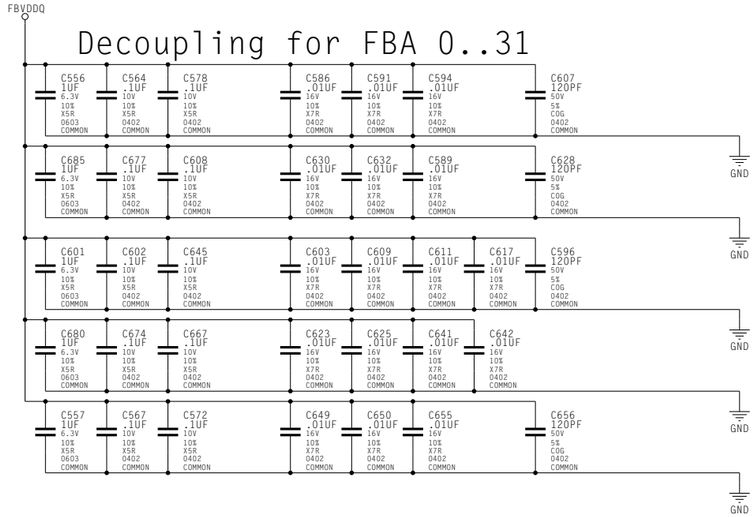
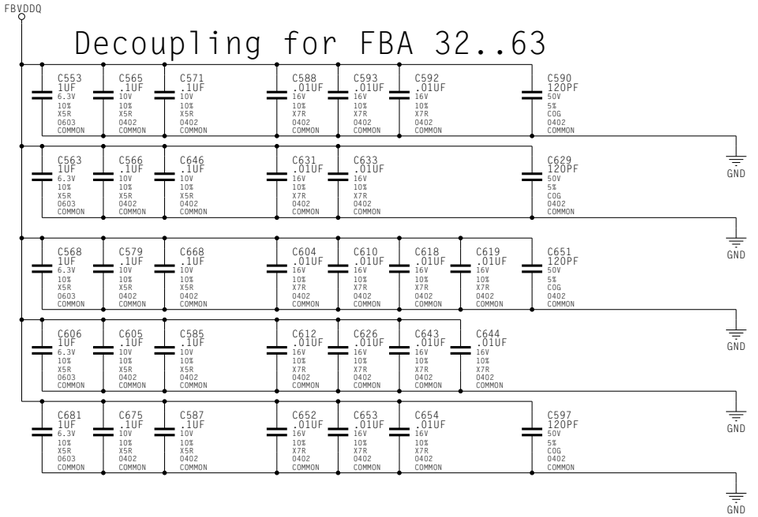
6 FrameBuffer: Partition A Decoupling

Decoupling for FBA 0..31



Decoupling for FBA 32..63



ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	FrameBuffer: Partition A Decoupling

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7 FrameBuffer: Partition B 8Mx32 BGA144 DDR3

FBB Partition

A-CSO-LOW-32bit

U11 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

Low Sub-Partition

A-CSO-HI-32bit

U12 DDR3BGA144 PACK_TYPE=BGA144 VERSION=BGA144 CHANGED

HI Sub-Partition

Termination for Sub-Partition and CLK MUST BE PLACED as close as possible to the BGA memory on the line BEFORE the MEMORY pin!! Minimize the stub length!!

DDR3: ZQ = 6x desired output impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

VREF:
M2 - DATA
M13 - ADDR

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 1.18K/(511 + 1.18K)

144BGA CMD Mapping

CMD	ADDR
CMD15	RAS*
CMD25	CAS*
CMD9	WE*
CMD11	CKE
CMD12	RESET
CMD8	CS0*
CMD7	CS1* *notused
CMD1	A<0>
CMD3	A<1>
CMD2	A<2>
CMD0	A<3>
CMD24	A<4>
CMD22	A<5>
CMD13	A<2>
CMD4	A<4>
CMD5	A<5>
CMD6	
CMD21	A<6>
CMD23	A<7>
CMD19	A<8>
CMD20	A<9>
CMD17	A<10
CMD16	A<11>
CMD14	A<12>
CMD10	BA0
CMD18	BA1

Low Sub-Partition

HI Sub-Partition

NET RULES

NET	IMPEDANCE	CRITICAL	DIFFPAIR
FBB_CLK0	100DIFF	1	FBB_CLK0
FBB_CLK0*	100DIFF	1	FBB_CLK0
FBB_CLK1	100DIFF	1	FBB_CLK1
FBB_CLK1*	100DIFF	1	FBB_CLK1
FBB_CMD<25..0>	40OHM	1	
FBBD<63..0>	40OHM	1	
FBBDQM<7..0>	40OHM	1	
FBBDQS_RN<7..0>	40OHM	1	
FBBDQS_WP<7..0>	40OHM	1	

Reference Plane Transition Cap

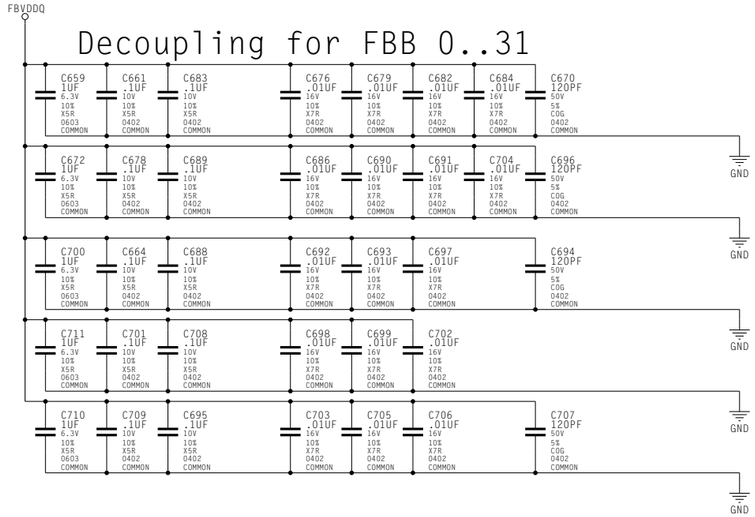
ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	FrameBuffer: Partition B 8Mx32 BGA144 DDR3

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

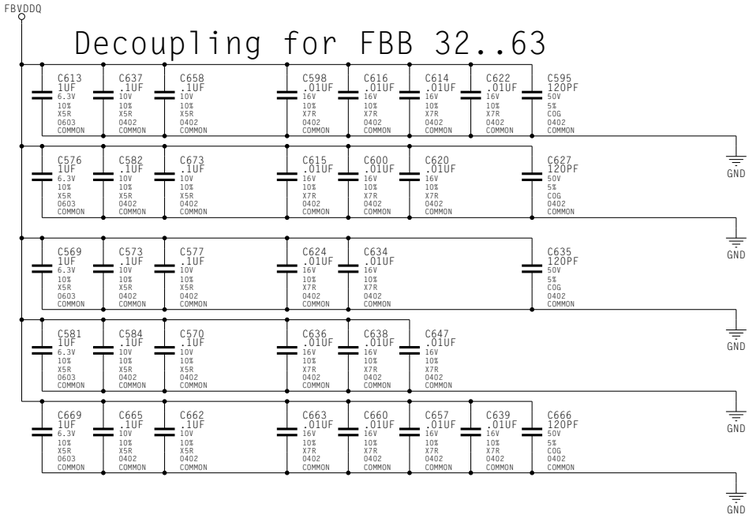
NV_PN	600-10317-0002-100		
ID	design	PAGE	7 OF 28
NAME	John Lam	DATE	31-MAY-2005

8 FrameBuffer: Partition B Decoupling

Decoupling for FBB 0..31



Decoupling for FBB 32..63



ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	FrameBuffer: Partition B Decoupling

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10317-0002-100		
ID	design	PAGE	8 OF 28
NAME	John Lam	DATE	31-MAY-2005

9 FrameBuffer: Partition C 8Mx32 BGA144 DDR3

FBC Partition

A-CSO-LOW-32bit

U8 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

A-CSO-HI-32bit

U10 DDR3BGA144 PACK_TYPE=BGA144 VERSION=BGA144 CHANGED

Termination for Sub-Partition and CLK MUST BE PLACED as close as possible to the BGA memory on the line BEFORE the MEMORY pin!! Minimize the stub length!!

Low Sub-Partition

HI Sub-Partition

FBVDDQ

FBC_CMD<25..0>

RAS CAS WE CS A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 NC/A<12> BA<0> BA<1> NC/BA<2> CKE CLK RESET ZQ

SNN_FBC0_NC1 SNN_FBC0_NC2 SNN_FBC0_NC3 — NC/RFU

R79 10K 5% 0402 COMMON — CKE

R627 10K 5% 0402 COMMON — RESET

R644 243 1% 0603 COMMON — ZQ

DDR3: ZQ = 6x desired output impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

R630 121 1% 0402 COMMON — FBC_CMD<2>
R632 121 1% 0402 COMMON — FBC_CMD<0>
R660 121 1% 0402 COMMON — FBC_CMD<24>
R659 121 1% 0402 COMMON — FBC_CMD<22>
R612 121 1% 0402 COMMON — FBC_CMD<13>
R607 121 1% 0402 COMMON — FBC_CMD<4>
R622 121 1% 0402 COMMON — FBC_CMD<5>
R623 121 1% 0402 COMMON — FBC_CMD<6>

R636 60.4 1% 0402 COMMON — FBC_CLK0
R639 60.4 1% 0402 COMMON — FBC_CLK0*
R617 60.4 1% 0402 COMMON — FBC_CLK1
R620 60.4 1% 0402 COMMON — FBC_CLK1*

R77 511 1% 0402 COMMON — R1
R78 1.3K 1% 0402 CHANGED — R2
C75 .1UF 10V 10% X5R 0402 COMMON

R663 511 1% 0402 COMMON — R1
R655 1.3K 1% 0402 CHANGED — R2
C947 .1UF 10V 10% X5R 0402 COMMON

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ = 1.26V = 1.8V * 1.18K/(511 + 1.18K)

VREF: M2 - DATA, M13 - ADDR

R621 243 1% 0603 COMMON — ZQ

DDR3: ZQ = 6x desired output impedence of DQ drivers Impedence = 240 / 6 = 40 ohm

R609 511 1% 0402 COMMON — R1
R611 1.3K 1% 0402 CHANGED — R2
C745 .1UF 10V 10% X5R 0402 COMMON

R81 511 1% 0402 COMMON — R1
R80 1.3K 1% 0402 CHANGED — R2
C81 .1UF 10V 10% X5R 0402 COMMON

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ = 1.26V = 1.8V * 1.18K/(511 + 1.18K)

12MIL

GND

144BGA CMD Mapping

CMD	ADDR	
CMD15	RAS*	
CMD25	CAS*	
CMD9	WE*	
CMD11	CKE	
CMD12	RESET	
CMD8	CS0*	
CMD7	CS1* *notused	
CMD1	A<0>	
CMD3	A<1>	
CMD2	A<2>	Low Sub-Partition
CMD0	A<3>	
CMD24	A<4>	
CMD22	A<5>	
CMD13	A<2>	HI Sub-Partition
CMD4	A<3>	
CMD5	A<4>	
CMD6	A<5>	
CMD21	A<6>	
CMD23	A<7>	
CMD19	A<8>	
CMD20	A<9>	
CMD17	A<10	
CMD16	A<11>	
CMD14	A<12>	
CMD10	BA0	
CMD18	BA1	

FBCD<63..0>

FBCDQM<7..0> — FBCDQM<0> FBCDQM<1> FBCDQM<2> FBCDQM<3> FBCDQM<4> FBCDQM<5> FBCDQM<6> FBCDQM<7>

FBCDQS_RN<7..0> — FBCDQS_RN<0> FBCDQS_RN<1> FBCDQS_RN<2> FBCDQS_RN<3> FBCDQS_RN<4> FBCDQS_RN<5> FBCDQS_RN<6> FBCDQS_RN<7>

FBCDQS_WP<7..0> — FBCDQS_WP<0> FBCDQS_WP<1> FBCDQS_WP<2> FBCDQS_WP<3> FBCDQS_WP<4> FBCDQS_WP<5> FBCDQS_WP<6> FBCDQS_WP<7>

U8 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

FBCD<0> FBCD<1> FBCD<2> FBCD<3> FBCD<4> FBCD<5> FBCD<6> FBCD<7> — DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
FBCDQM<0> FBCDQS_RN<0> FBCDQS_WP<0> — DQM DQSR DQSW

U8 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

FBCD<8> FBCD<9> FBCD<10> FBCD<11> FBCD<12> FBCD<13> FBCD<14> FBCD<15> — DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
FBCDQM<1> FBCDQS_RN<1> FBCDQS_WP<1> — DQM DQSR DQSW

U8 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

FBCD<16> FBCD<17> FBCD<18> FBCD<19> FBCD<20> FBCD<21> FBCD<22> FBCD<23> — DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
FBCDQM<2> FBCDQS_RN<2> FBCDQS_WP<2> — DQM DQSR DQSW

U8 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

FBCD<24> FBCD<25> FBCD<26> FBCD<27> FBCD<28> FBCD<29> FBCD<30> FBCD<31> — DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
FBCDQM<3> FBCDQS_RN<3> FBCDQS_WP<3> — DQM DQSR DQSW

U10 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

FBCD<32> FBCD<33> FBCD<34> FBCD<35> FBCD<36> FBCD<37> FBCD<38> FBCD<39> — DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
FBCDQM<4> FBCDQS_RN<4> FBCDQS_WP<4> — DQM DQSR DQSW

U10 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

FBCD<40> FBCD<41> FBCD<42> FBCD<43> FBCD<44> FBCD<45> FBCD<46> FBCD<47> — DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
FBCDQM<5> FBCDQS_RN<5> FBCDQS_WP<5> — DQM DQSR DQSW

U10 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

FBCD<48> FBCD<49> FBCD<50> FBCD<51> FBCD<52> FBCD<53> FBCD<54> FBCD<55> — DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
FBCDQM<6> FBCDQS_RN<6> FBCDQS_WP<6> — DQM DQSR DQSW

U10 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

FBCD<56> FBCD<57> FBCD<58> FBCD<59> FBCD<60> FBCD<61> FBCD<62> FBCD<63> — DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
FBCDQM<7> FBCDQS_RN<7> FBCDQS_WP<7> — DQM DQSR DQSW

NVVDD

Reference Plane Transition Cap

C728 22UF 6.3V 20% X5R 0805 COMMON
C671 120PF 50V 5% C0G 0402 COMMON
C621 120PF 50V 5% C0G 0402 COMMON

NET RULES

NET	IMPEDANCE	CRITICAL	DIFFPAIR
FBC_CLK0	100DIFF	1	FBC_CLK0
FBC_CLK0*	100DIFF	1	FBC_CLK0
FBC_CLK1	100DIFF	1	FBC_CLK1
FBC_CLK1*	100DIFF	1	FBC_CLK1
FBC_CMD<25..0>	40OHM	1	
FBCD<63..0>	40OHM	1	
FBCDQM<7..0>	40OHM	1	
FBCDQS_RN<7..0>	40OHM	1	
FBCDQS_WP<7..0>	40OHM	1	

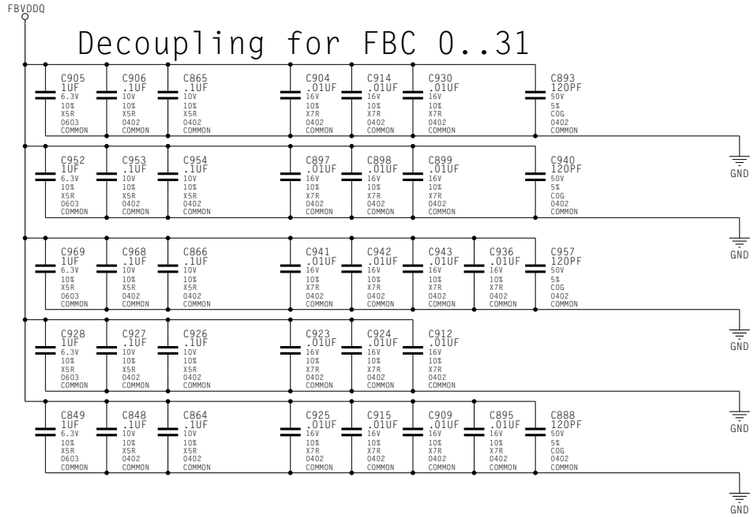
ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	FrameBuffer: Partition C 8Mx32 BGA144 DDR3

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

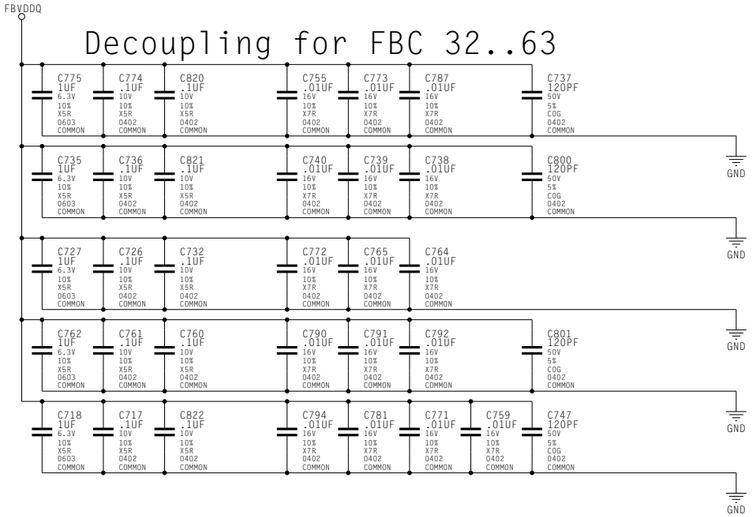
NV_PN	600-10317-0002-100		
ID	design	PAGE	9 OF 28
NAME	John Lam	DATE	31-MAY-2005

10 FrameBuffer: Partition C Decoupling

Decoupling for FBC 0..31



Decoupling for FBC 32..63



ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	FrameBuffer: Partition C Decoupling

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10317-0002-100		
ID	design	PAGE	10 OF 28
NAME	John Lam	DATE	31-MAY-2005

11 FrameBuffer: Partition D 8Mx32 BGA144 DDR3

FBD Partition

A-CSO-LOW-32bit

U2 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

A-CSO-HI-32bit

U4 DDR3BGA144 PACK_TYPE=BGA144 VERSION=BGA144 CHANGED

Termination for Sub-Partition and CLK MUST BE PLACED as close as possible to the BGA memory on the line BEFORE the MEMORY pin!! Minimize the stub length!!

Low Sub-Partition

HI Sub-Partition

DDR3: ZQ = 6x desired output impedence of DQ drivers Impedence = 240 / 6 = 40 ohm

VREF: M2 - DATA M13 - ADDR

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ 1.26V = 1.8V * 1.18K/(511 + 1.18K)

144BGA CMD Mapping

CMD	ADDR
CMD15	RAS*
CMD25	CAS*
CMD9	WE*
CMD11	CKE
CMD12	RESET
CMD8	CS0*
CMD7	CS1* *notused
CMD1	A<0>
CMD3	A<1>
CMD2	A<2>
CMD0	A<3>
CMD24	A<4>
CMD22	A<5>
CMD13	A<2>
CMD4	A<3>
CMD5	A<4>
CMD6	A<5>
CMD21	A<6>
CMD23	A<7>
CMD19	A<8>
CMD20	A<9>
CMD17	A<10
CMD16	A<11>
CMD14	A<12>
CMD10	BA0
CMD18	BA1

Low Sub-Partition / HI Sub-Partition

NET RULES

NET	IMPEDANCE	CRITICAL	DIFFPAIR
FBD_CLK0	100DIFF	1	FBD_CLK0
FBD_CLK0*	100DIFF	1	FBD_CLK0
FBD_CLK1	100DIFF	1	FBD_CLK1
FBD_CLK1*	100DIFF	1	FBD_CLK1
FBD_CMD<25..0>	40OHM	1	
FBDD<63..0>	40OHM	1	
FBDDQM<7..0>	40OHM	1	
FBDDQS_RN<7..0>	40OHM	1	
FBDDQS_WP<7..0>	40OHM	1	

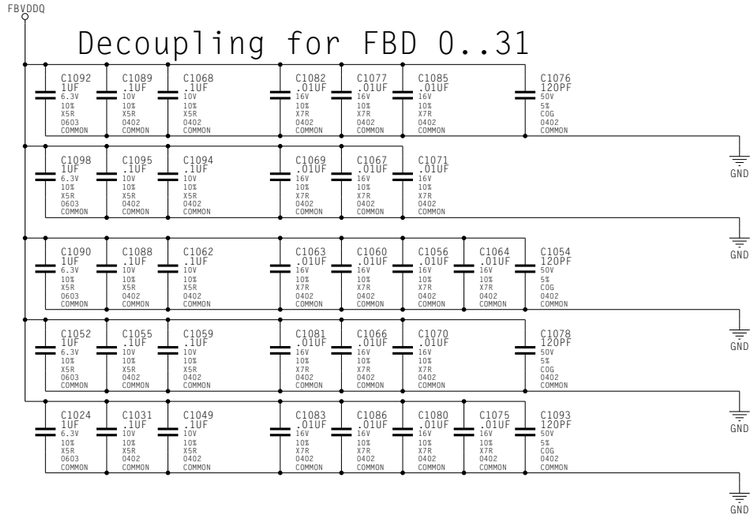
NVDD Reference Plane Transition Cap

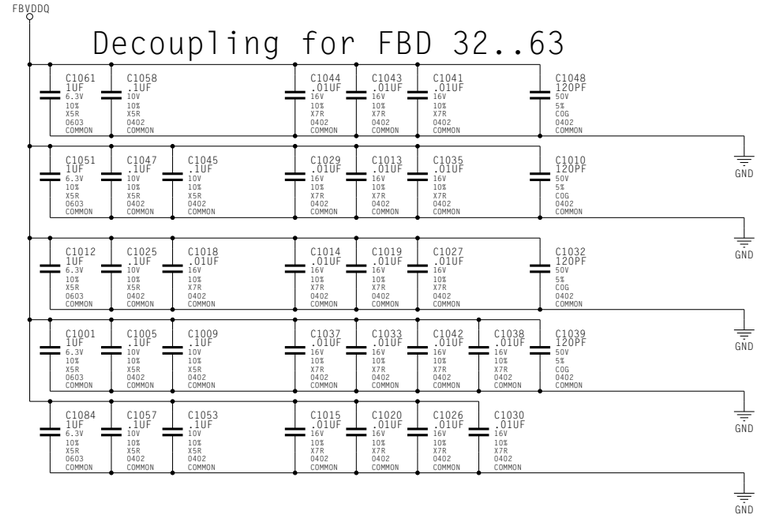
ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	FrameBuffer: Partition D 8Mx32 BGA144 DDR3

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10317-0002-100		
ID	design	PAGE	11 OF 28
NAME	John Lam	DATE	31-MAY-2005

12 FrameBuffer: Partition D Decoupling





ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	FrameBuffer: Partition D Decoupling

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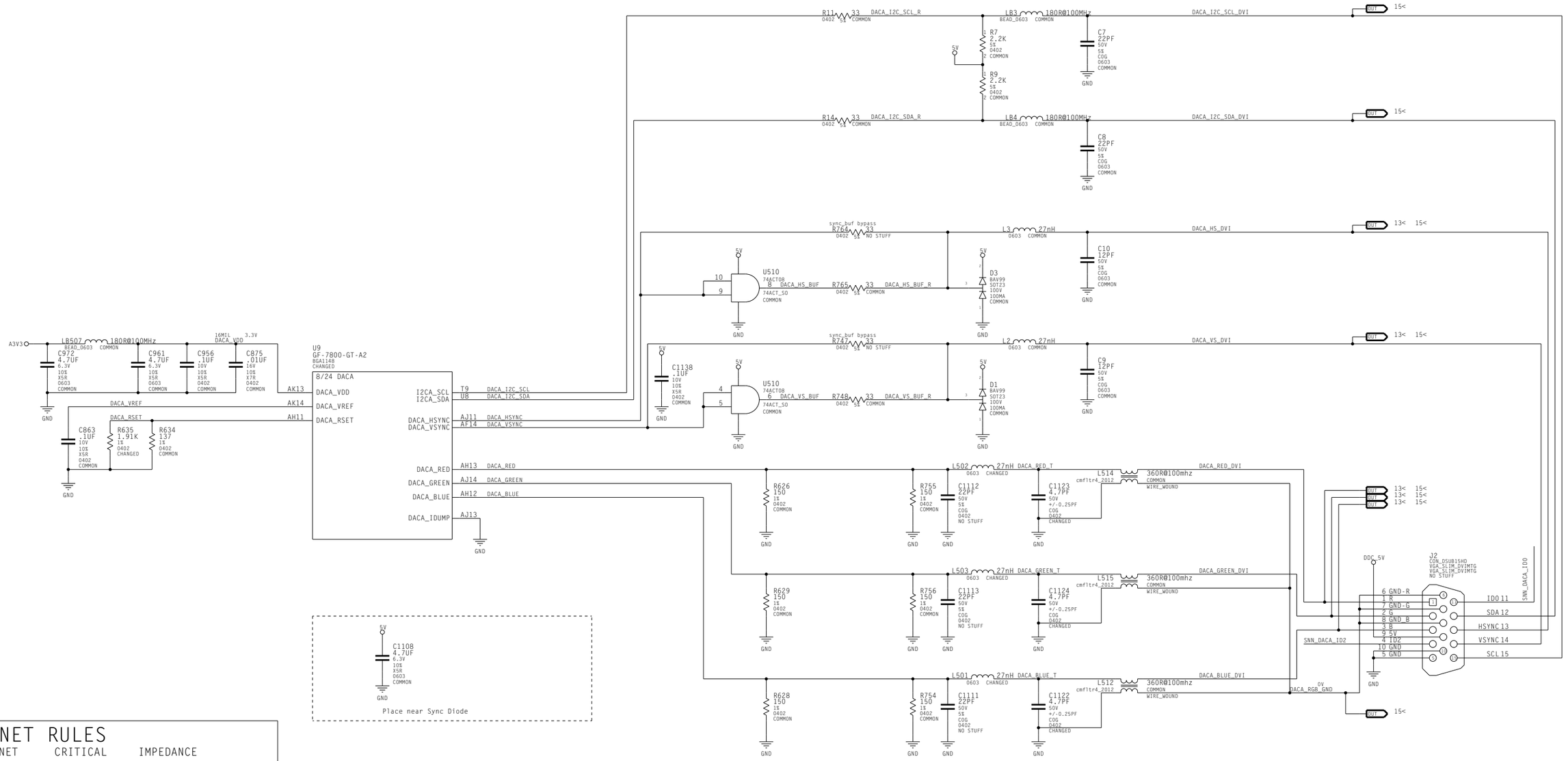
NV_PN	600-10317-0002-100		
ID	design	PAGE	12 OF 28
NAME	John Lam	DATE	31-MAY-2005

13 DACA Interface



NET RULES

	NET	CRITICAL	IMPEDANCE
IN	DACA_RED	1	50OHM
IN	DACA_GREEN	1	50OHM
IN	DACA_BLUE	1	50OHM
IN	DACA_RED_T	1	50OHM
IN	DACA_GREEN_T	1	50OHM
IN	DACA_BLUE_T	1	50OHM
13> IN	DACA_RED_DVI	1	75OHM
15< IN	DACA_GREEN_DVI	1	75OHM
13> IN	DACA_BLUE_DVI	1	75OHM
15<			
IN	DACA_HSYNC	2	50OHM
IN	DACA_VSYNC	2	50OHM
IN	DACA_HS_BUF	2	50OHM
IN	DACA_VS_BUF	2	50OHM
IN	DACA_HS_BUF_R	2	50OHM
IN	DACA_VS_BUF_R	2	50OHM
13> IN	DACA_HS_DVI	2	50OHM
15< IN	DACA_VS_DVI	2	50OHM

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	DACA Interface

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2701 SAN TOMAS EXPRESSWAY
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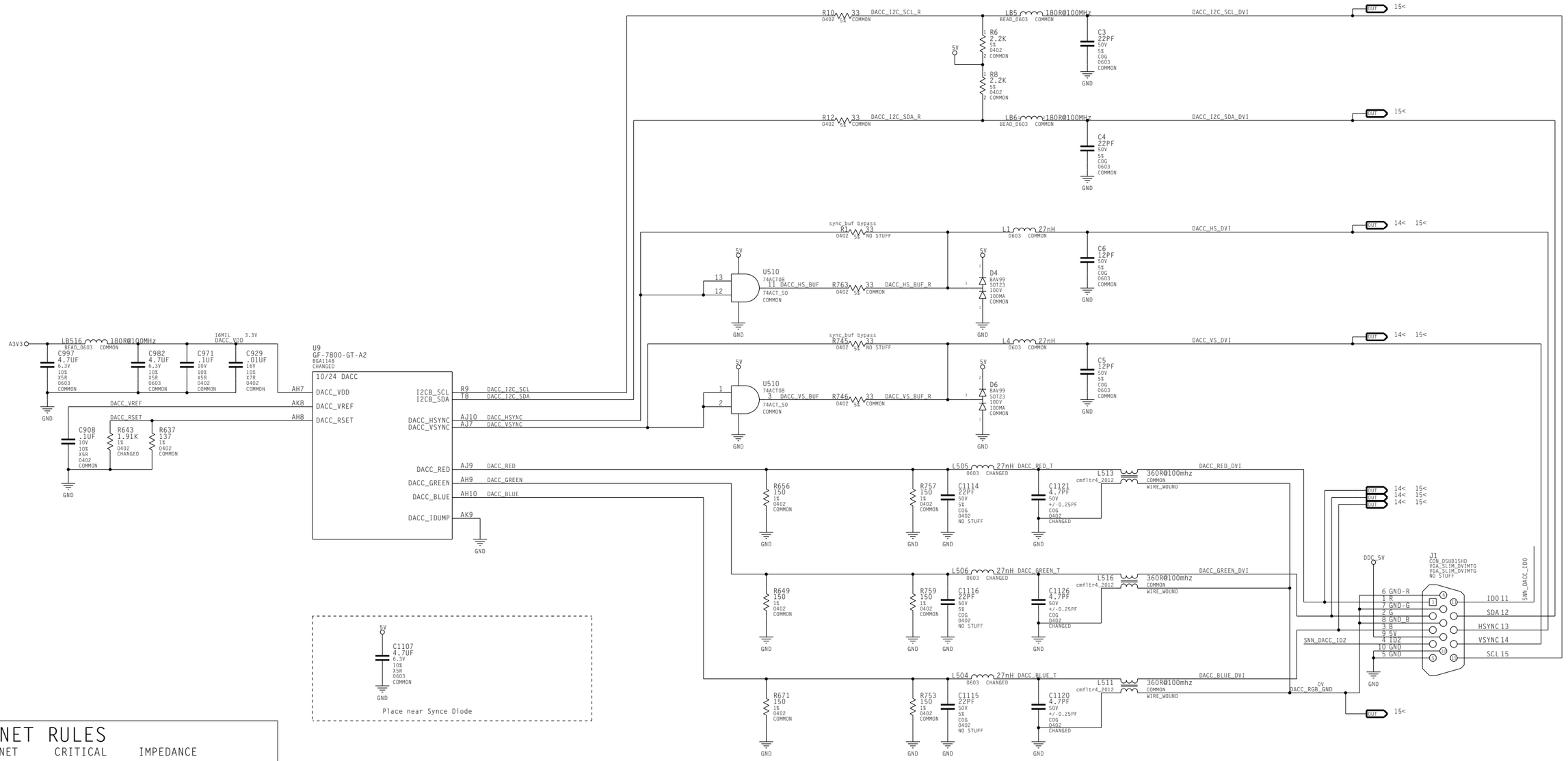
NV_PN	600-10317-0002-100		
ID	design	PAGE	13 OF 28
NAME	John Lam	DATE	31-MAY-2005

14 DACC Interface



NET RULES

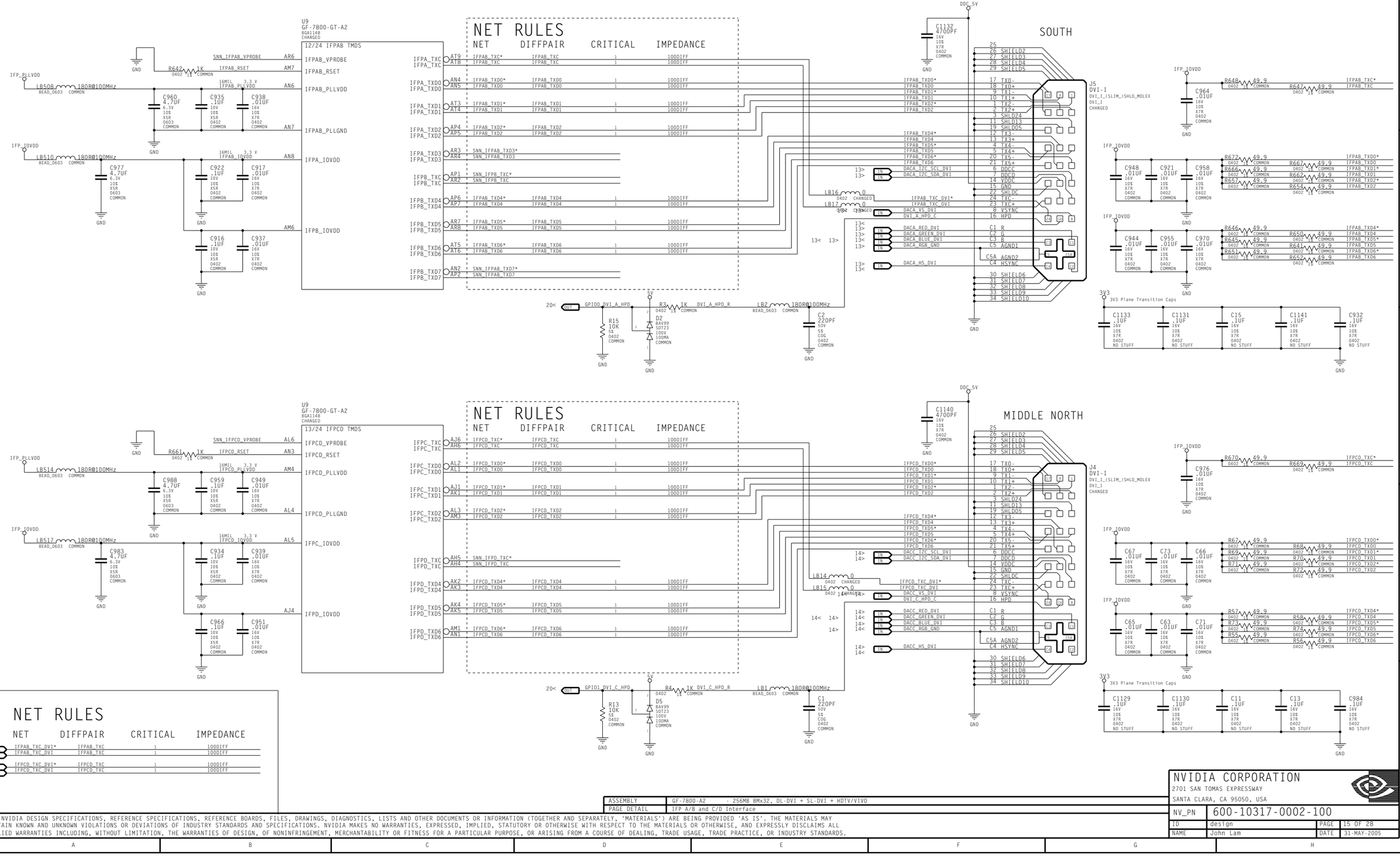
	NET	CRITICAL	IMPEDANCE
IN	DACC_RED	1	50OHM
IN	DACC_GREEN	1	50OHM
IN	DACC_BLUE	1	50OHM
IN	DACC_RED_T	1	50OHM
IN	DACC_GREEN_T	1	50OHM
IN	DACC_BLUE_T	1	50OHM
14> IN	DACC_RED_DVI	1	75OHM
15< IN	DACC_GREEN_DVI	1	75OHM
14> IN	DACC_BLUE_DVI	1	75OHM
15<			
IN	DACC_HSYNC	2	50OHM
IN	DACC_VSYNC	2	50OHM
IN	DACC_HS_BUF	2	50OHM
IN	DACC_VS_BUF	2	50OHM
IN	DACC_HS_BUF_R	2	50OHM
IN	DACC_VS_BUF_R	2	50OHM
15< IN	DACC_HS_DVI	2	50OHM
14> IN	DACC_VS_DVI	2	50OHM
15<			

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	DACC Interface

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10317-0002-100		
ID	design	PAGE	14 OF 28
NAME	John Lam	DATE	31-MAY-2005

15 IFP A/B and C/D Interface



NET RULES

NET	DIFFPAIR	CRITICAL	IMPEDANCE
IFPAB_TXC_DVI*	IFPAB_TXC	1	100DIFF
IFPAB_TXC_DVI	IFPAB_TXC	1	100DIFF
IFPCD_TXC_DVI*	IFPCD_TXC	1	100DIFF
IFPCD_TXC_DVI	IFPCD_TXC	1	100DIFF

ASSEMBLY	GF-7800-A2 - 256M8 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	IFP A/B and C/D Interface

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10317-0002-100		
ID	design	PAGE	15 OF 28
NAME	John Lam	DATE	31-MAY-2005

16 DACB Interface/Framelock

NET RULES

NET	CRITICAL	IMPEDANCE
COUT	1	50OHM
CVBS_YOUT	1	50OHM
CVBS_PBOUT	1	50OHM
MDIN_Cout_C	1	75OHM
MDIN_Yout_C	1	75OHM
MDIN_PBout_C	1	75OHM
CVBSYIN	1	50OHM
CHROMAIN	1	50OHM
CVBSYIN_R	1	50OHM
CHROMAIN_R	1	50OHM
MDIN_CVBSYIN_C	1	75OHM
MDIN_Cin_C	1	75OHM

STEREO 5V

F1 1A 1812 NO STUFF — 5V — 16MIL — DNI FOR VIVO — LB8 220R@100MHz BEAD_0805 NO STUFF — 16MIL MDIN_GND2_STEREO5V

Current = ~300mA

POLYSWITCH — 5V_POLY_STEREO — LB9 220R@100MHz BEAD_0805 NO STUFF — 16MIL STEREO_5V

STEREO 3D

To Framelock

5V — C1110 .1UF 10V 10% X5R 0402 NO STUFF — GND

5V — R749 3.3K 5% 0402 NO STUFF

20> IN STEREO

U509 SN74AHC1G08 SC70-5 NO STUFF — 4 BUFFSTEREO

R743 33 0402 5% NO STUFF — BUFFSTEREO_4pin

R744 33 0402 5% NO STUFF

GND

Internal Stereo Out

STEREO_5V — LB523 BEAD_0603 NO STUFF 180R@100MHz — BUFFSTEREO_C

J7 HDR_1M4 MALE 2.0MM N/A NORM NO STUFF

D515 BAV99 SOT23 100V 100MA NO STUFF — GND

C21 .1UF 10V 10% X5R 0402 NO STUFF — GND

C35 220PF 50V 5% COG 0603 NO STUFF — GND

LOW_INT_GND — R19 0 5% 0603 NO STUFF — GND

LOW_INT_SHLD — R23 0 5% 0603 NO STUFF — GND

D8 BAV99 SOT23 100V 100MA NO STUFF — GND

I2CC_SCL_BUFFSTEREO_R

Framelock

5V — U508 SN74AHC1G08 SC70-5 NO STUFF — 4 STEREO_FL_BUF

STEREO

R758 33 0402 5% NO STUFF — STEREO_FL

C1105 .1UF 10V 10% X5R 0402 NO STUFF — GND

I2CC_SCL

I2CC_SDA

GPIO4_VTG_RST

20< OUT

C1099 1000PF 16V 10% X7R 0402 NO STUFF — GND

make 10k when header not stuffed

20> 18<> BI SWAPRDY_A

20< OUT XTALSSIN

R752 0 0402 5% NO STUFF — Place close to GPU

C1046 .047UF 16V 10% X7R 0402 NO STUFF — FL_XTAL

R699 110 1% 0402 NO STUFF — GND

FRAMLOCK_CLKIN

J6 HDR_2X7 FEMALE 2.54MM 0 NO NORM NO STUFF — FRAMELOCK

Connector SDI - Female 075-20000-0012-000 Framelock - Male

1 SILK — 2 GND — 3 SCK — 4 GND — 5 SDA — 6 GND — 7 VRST — 8 RST* — 9 SRDY — 10 12V — 11 CLK — 12 12V — 13 GPIO — 14 INTR

BUFRST* — IN 17< 20>

1.5A required for SDI — EXT_12V

C1109 .047UF 16V 10% X7R 0402 NO STUFF

C1106 .1UF 16V 10% X7R 0402 NO STUFF

GND

GPIO10_FL_INT — BI 20<>

GPIO7_FL_IO — OUT 20<

R740 10K 5% 0402 NO STUFF

R741 10K 5% 0402 NO STUFF

GND

FILTER VALUES

HDTV/StandardTV

8.2pF/22pf — from codec — 0.56uH/1.8uH — to DIN connector — 82pF/330pF — 82pF/270pF

DACB_VDD — A3V3 — LB509 BEAD_0603 COMMON 180R@100MHz — 16MIL DACB_VDD

C975 4.7UF 6.3V 10% X5R 0603 COMMON

C962 4.7UF 6.3V 10% X5R 0603 COMMON

C919 .1UF 10V 10% X5R 0402 COMMON

C910 .01UF 16V 10% X7R 0402 COMMON

GND

DACB_VREF

C913 .1UF 10V 10% X5R 0402 COMMON — GND

DACB_RSET

R75 1.5K 1% 0402 NO STUFF

R681 499 1% 0402 NO STUFF

R633 1.82K 1% 0402 NO STUFF

R631 64.9 1% 0402 CHANGED — GND

DACB_RSET2

20> IN GPIO11_DACB_RSET

R690 10K 5% 0402 NO STUFF — GND

Q517 BSS138 SOT23_1G1D1S NO STUFF — 1G1D1S — MAX_VOLTAGE=50V CONTINUOUS_CURRENT=0.22AB1C R_DS_ON=3.5Ω MAX_POWER=0.88A MAX_WATTAGE=0.36AW25C V_BE_ON=+.35V — GND

U9 GF-7800-GT-A2 BGA1148 CHANGED

9/24 DACB (TVout)

Y9 DACB_VDD

Y8 DACB_VREF

Y11 DACB_RSET

AA8 DACB_RED — SVID_CHROM /COMPOSITE — COUT

AB9 DACB_GREEN — SVID_LUM — CVBS_YOUT

AA9 DACB_BLUE — COMPOSITE — CVBS_PBOUT

W9 DACB_IDUMP — GND

R668 150 1% 0402 COMMON

R640 150 1% 0402 COMMON

R653 150 1% 0402 COMMON

CVBS_PBOUT — R760 150 1% 0402 COMMON

C1127 8.2PF 50V +/-0.5PF NPO COMMON

L507 0.56uH 0603 COMMON — MDIN_PBout_C

C1117 82PF 50V 5% COG 0402 COMMON

C1136 82PF 50V 5% COG 0402 COMMON

R761 150 1% 0402 COMMON

C1128 8.2PF 50V +/-0.5PF NPO COMMON

L508 0.56uH 0603 COMMON — MDIN_Cout_C

C1118 82PF 50V 5% COG 0402 COMMON

C1137 82PF 50V 5% COG 0402 COMMON

J3 MINIDIN_10_VIVO V1V0 CHANGED — Pb out — C/Pr out — Y/CVBS out — C/Pr GND — Y/CVBS GND — T/CVBS — C in — GND

MDIN_GND2_STEREO5V

DDC_5V — C1143 4700PF 16V 10% X7R 0402 COMMON

MDIN_SCL_C_STEREO — LB7 BEAD_0603 COMMON 180R@100MHz — C14 220PF 50V 5% COG 0603 COMMON — STUFF (3) FOR STEREO/VIVO

DNI FOR STEREO R17 0 0402 5% COMMON — I2CC_SCL — IN 17< 20>

MDIN_SDA_C — LB525 BEAD_0603 COMMON 180R@100MHz — C1135 220PF 50V 5% COG 0603 COMMON — I2CC_SDA — BI 17<> 20<>

C1139 8.2PF 50V +/-0.5PF NPO COMMON

L510 0.56uH 0603 COMMON — MDIN_Yout_C — CVBS_YOUT

C1142 82PF 50V 5% COG 0402 COMMON

C1125 82PF 50V 5% COG 0402 COMMON

R762 150 1% 0402 COMMON

17< 16< OUT CVBSYIN — R751 18 0402 5% COMMON — R750 56 5% 0402 COMMON

Ind should be Stuff with 0ohm by default. Cap should be No-Stuff by default. CVBSYIN_R

D516 BAV99 SOT23 100V 100MA COMMON

L509 1.8uH 0603 COMMON — MDIN_CVBSYIN_C

C1119 270PF 50V 5% COG 0603 COMMON

C1134 330PF 50V 5% COG 0603 COMMON

MDIN_GND — Rgnd — R2 0 5% 0603 COMMON — GND FOR STEREO

Rgnd_video — R5 0 5% 0603 COMMON — STUFF 1UF CAP WHEN STEREO ELSE 0 OHM R

Ind should be Stuff with 0ohm by default. Cap should be No-Stuff by default. MDIN_Cin_C

L5 1.8uH 0603 COMMON

C12 330PF 50V 5% COG 0603 COMMON

C16 270PF 50V 5% COG 0603 COMMON

D7 BAV99 SOT23 100V 100MA COMMON

CHROMAIN_R — R16 18 0402 5% COMMON — CHROMAIN — OUT 16< 17<

R18 56 5% 0402 COMMON

NOTE:
Rgnd can be used for EMI purposes.

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	DACB Interface/Framelock

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

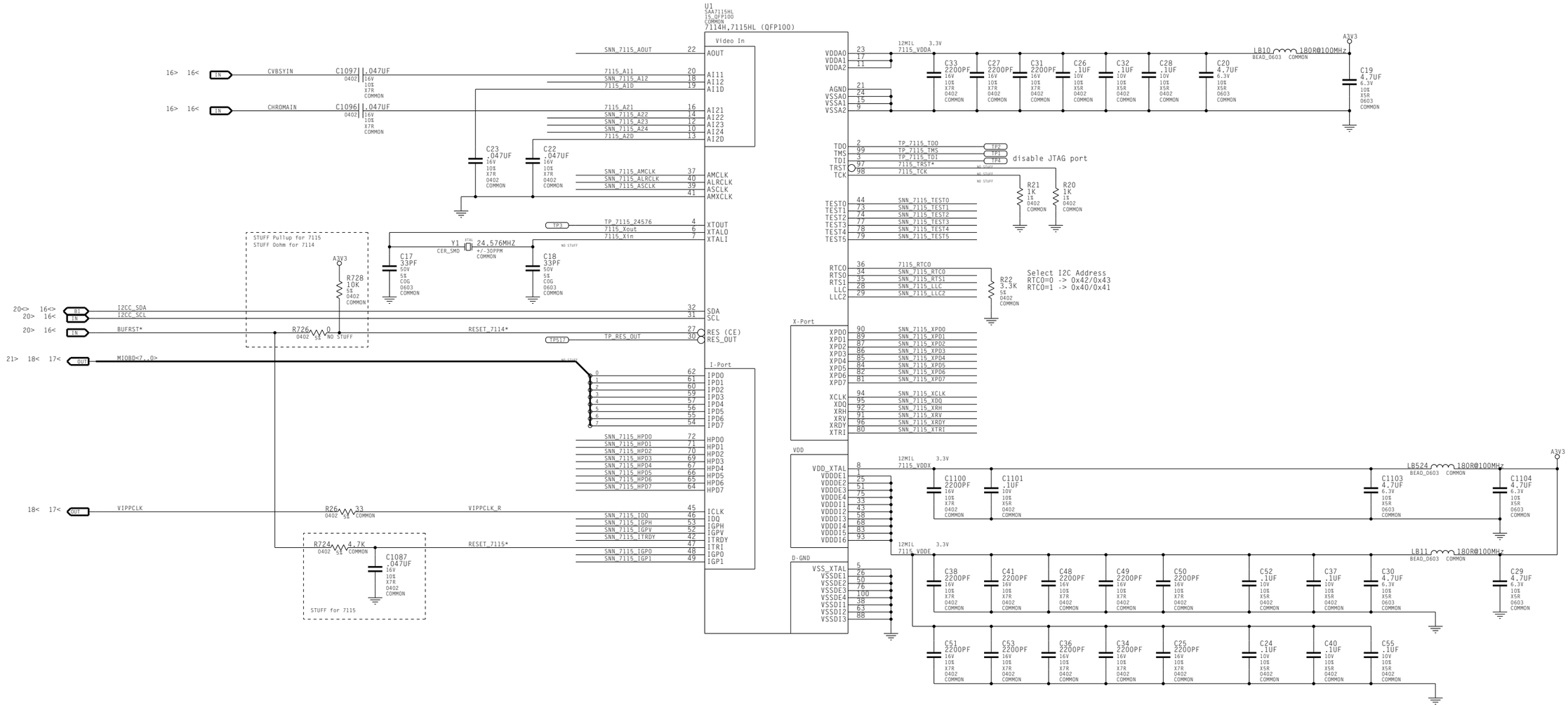
NV_PN	600-10317-0002-100		
ID	design	PAGE	16 OF 28
NAME	John Lam	DATE	31-MAY-2005

17 Video Capture (Philips 7115)

NET RULES

NET	IMPEDANCE	CRITICAL	
7115_Xout		1	
7115_Xin		1	
VIPPCLK	50OHM	1	18< 17>
VIPPCLK_R	50OHM	1	
MIOBD<7..0>	50OHM	2	21> 18< 17>

VIDEO CAPTURE



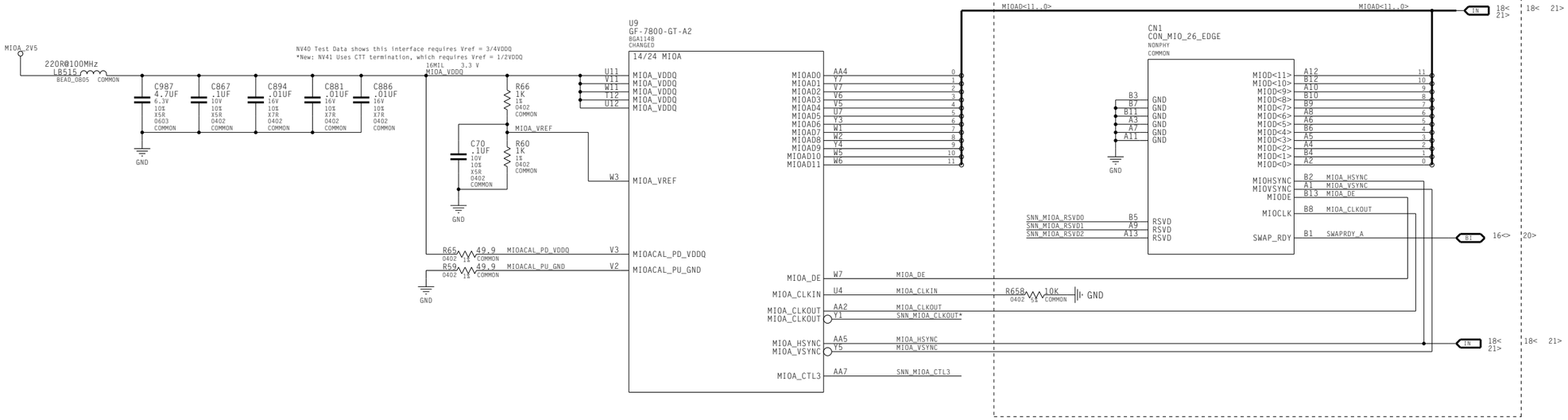
ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	Video Capture (Philips 7115)

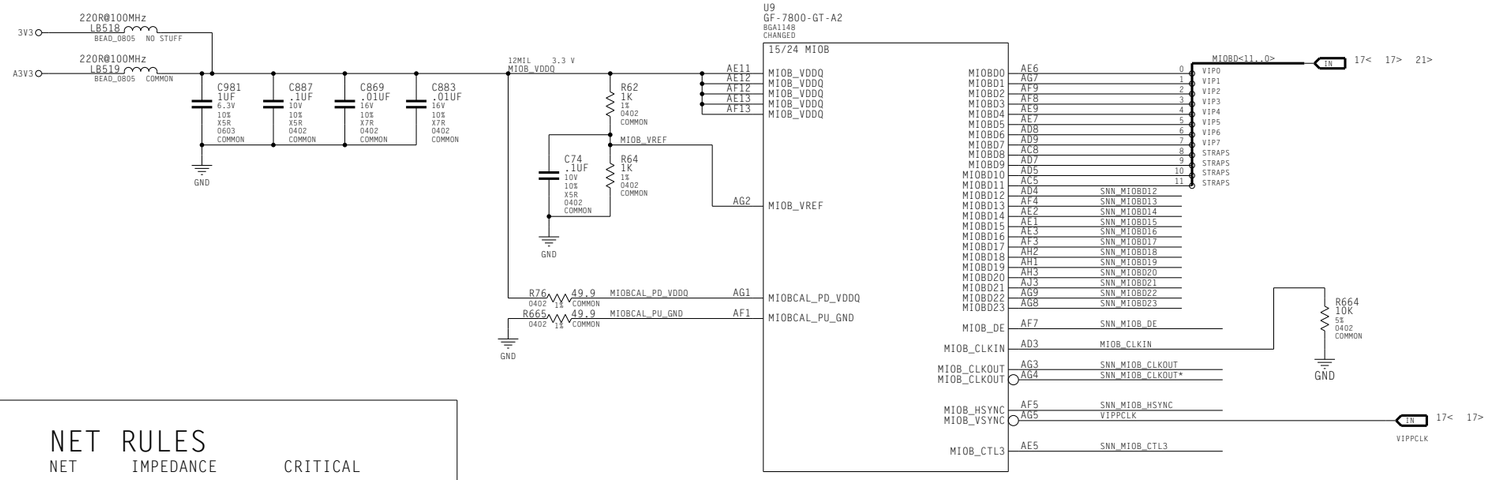
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10317-0002-100		
ID	design	PAGE	17 OF 28
NAME	John Lam	DATE	31-MAY-2005

18 Multi-use IO(MIO) Interface

MIO Feature Connector





NET RULES

	NET	IMPEDANCE	CRITICAL
21> 18<	MIOA_CLKOUT	50OHM	1
	MIOA_HSYNC	50OHM	2
	MIOA_VSYNC	50OHM	2
	MIOA_DE	50OHM	2
21> 18<	MIOAD<11..0>	50OHM	2

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	Multi-use IO(MIO) Interface

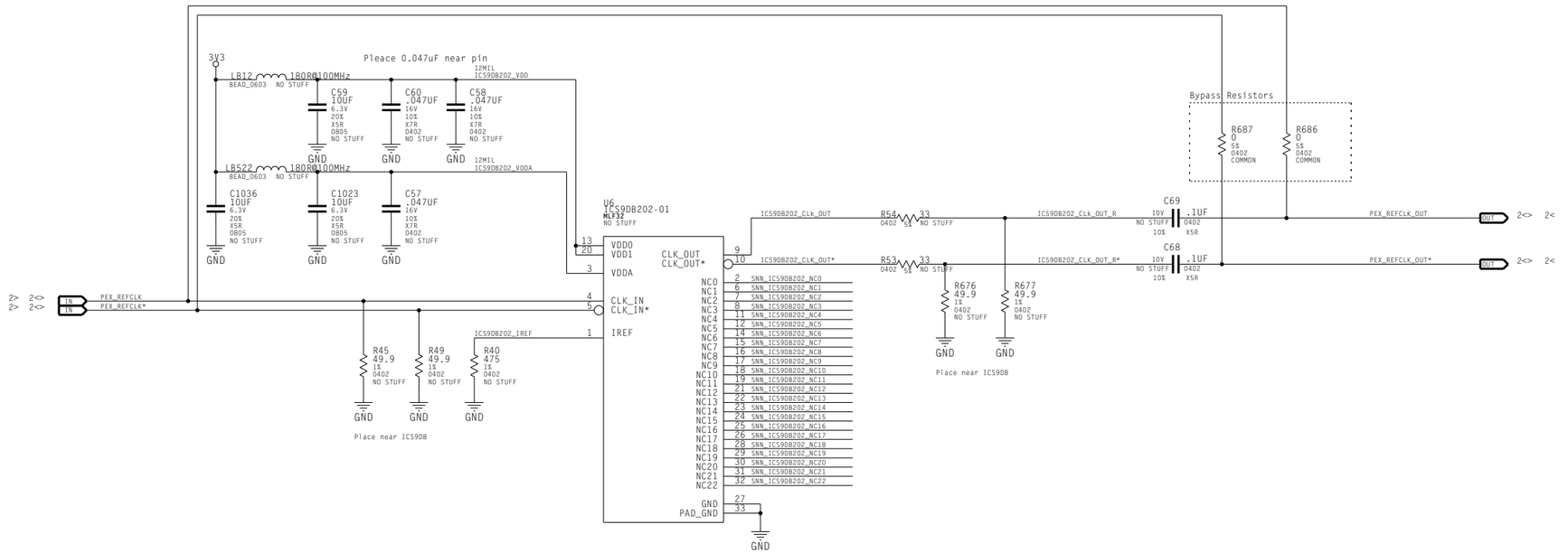
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10317-0002-100		
ID	design	PAGE	18 OF 28
NAME	John Lam	DATE	31-MAY-2005

19 PEX: Zero Delay Buffer

NET RULES

NET	IMPEDANCE	CRITICAL	DIFFPAIR
ICS9DB202_CLK_OUT	100DIFF	1	ICS9DB202_CLK_OUT
ICS9DB202_CLK_OUT*	100DIFF	1	ICS9DB202_CLK_OUT
ICS9DB202_CLK_OUT_R	100DIFF	1	ICS9DB202_CLK_OUT_R
ICS9DB202_CLK_OUT_R*	100DIFF	1	ICS9DB202_CLK_OUT_R



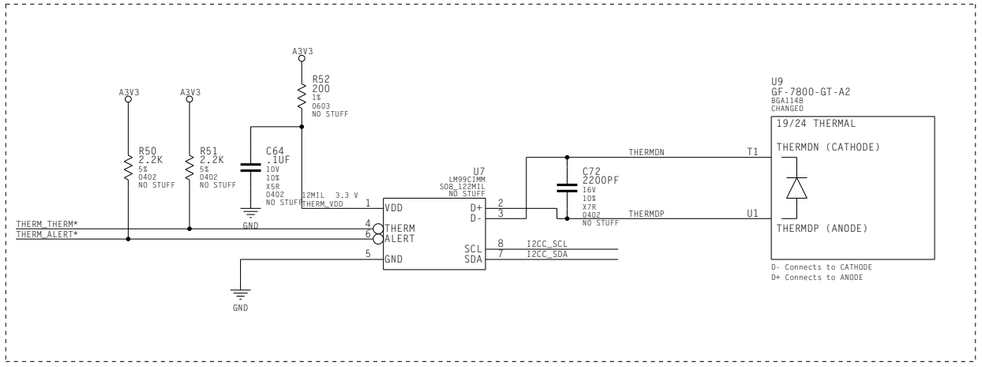
ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	PEX: Zero Delay Buffer

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

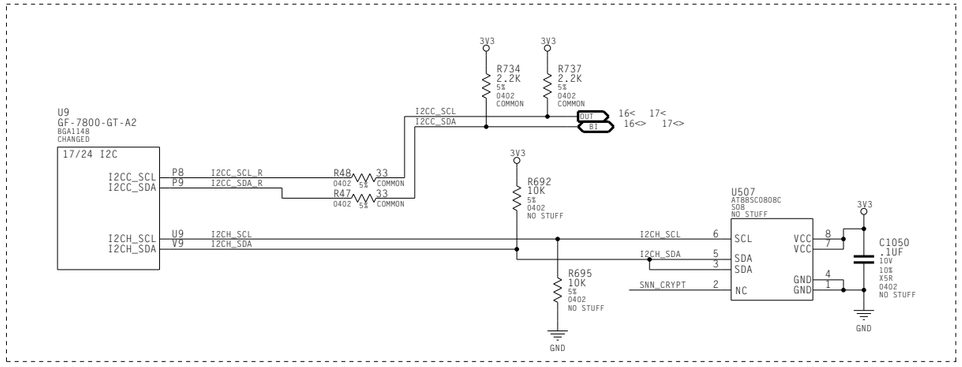
NV_PN	600-10317-0002-100		
ID	design	PAGE	19 OF 28
NAME	John Lam	DATE	31-MAY-2005

20 MISC: GPIO, I2C, THERMAL, BIOS, XTAL

Thermal Diode



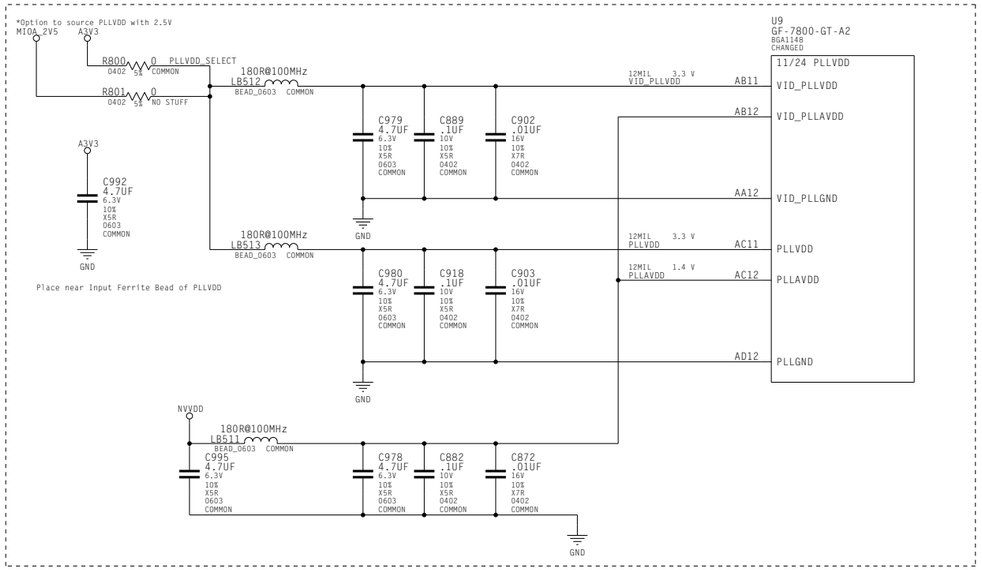
I2CC / I2CH(+ HDCP ROM)



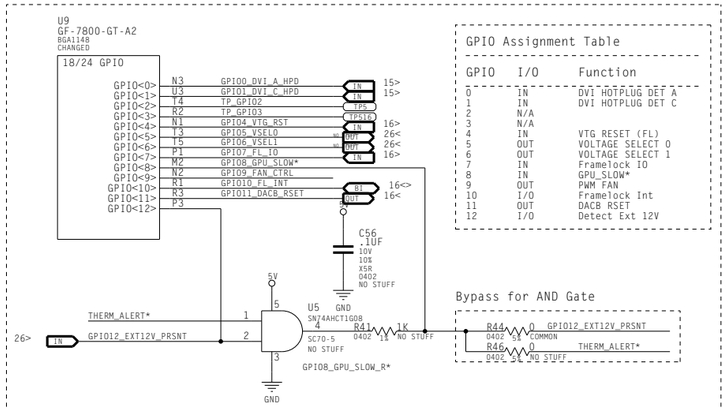
NET RULES

	NET	IMPEDANCE	CRITICAL
16> 20<	XTALIN	50OHM	1
	XTALOUT	50OHM	1
	XTALSSIN	50OHM	1
	THERMDN	50OHM	2
	THERMDP	50OHM	2

PLLVDD/VID_PLLVDD



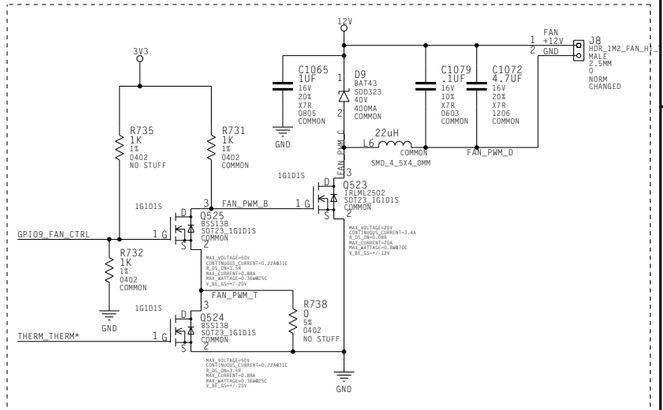
GPIO



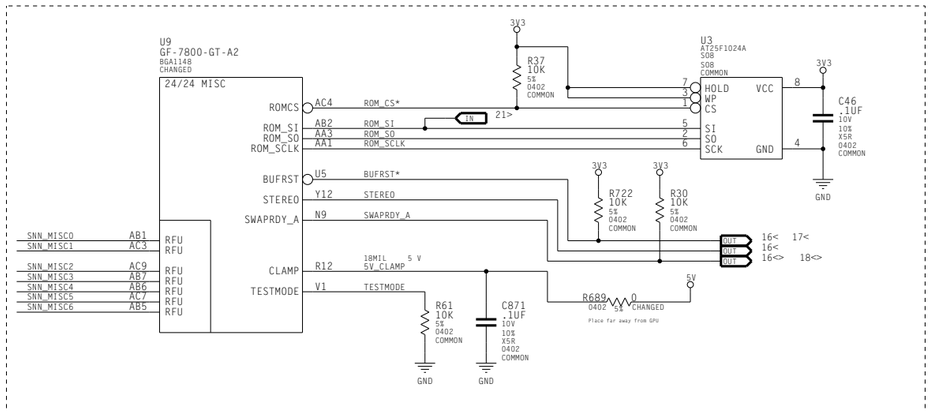
GPIO Assignment Table

GPIO	I/O	Function
0	IN	DVI HOTPLUG DET A
1	IN	DVI HOTPLUG DET C
2	N/A	
3	N/A	
4	IN	VTG RESET (FL)
5	OUT	VOLTAGE SELECT 0
6	OUT	VOLTAGE SELECT 1
7	IN	Framelock IO
8	IN	GPU_SLOW*
9	OUT	PWM FAN
10	I/O	Framelock Int
11	OUT	DACB RSET
12	I/O	Detect Ext 12V

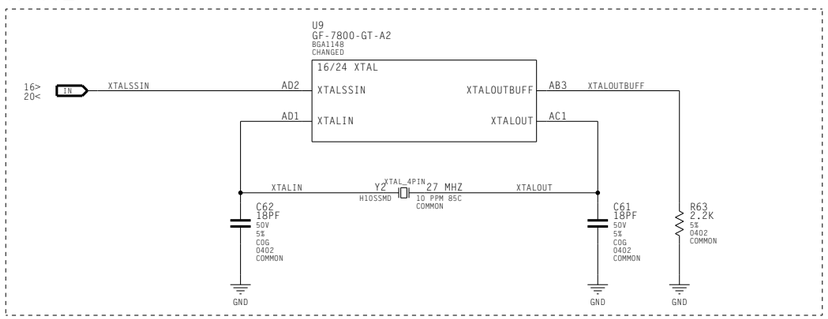
FAN CONTROL



ROM / MISC (BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)



XTAL

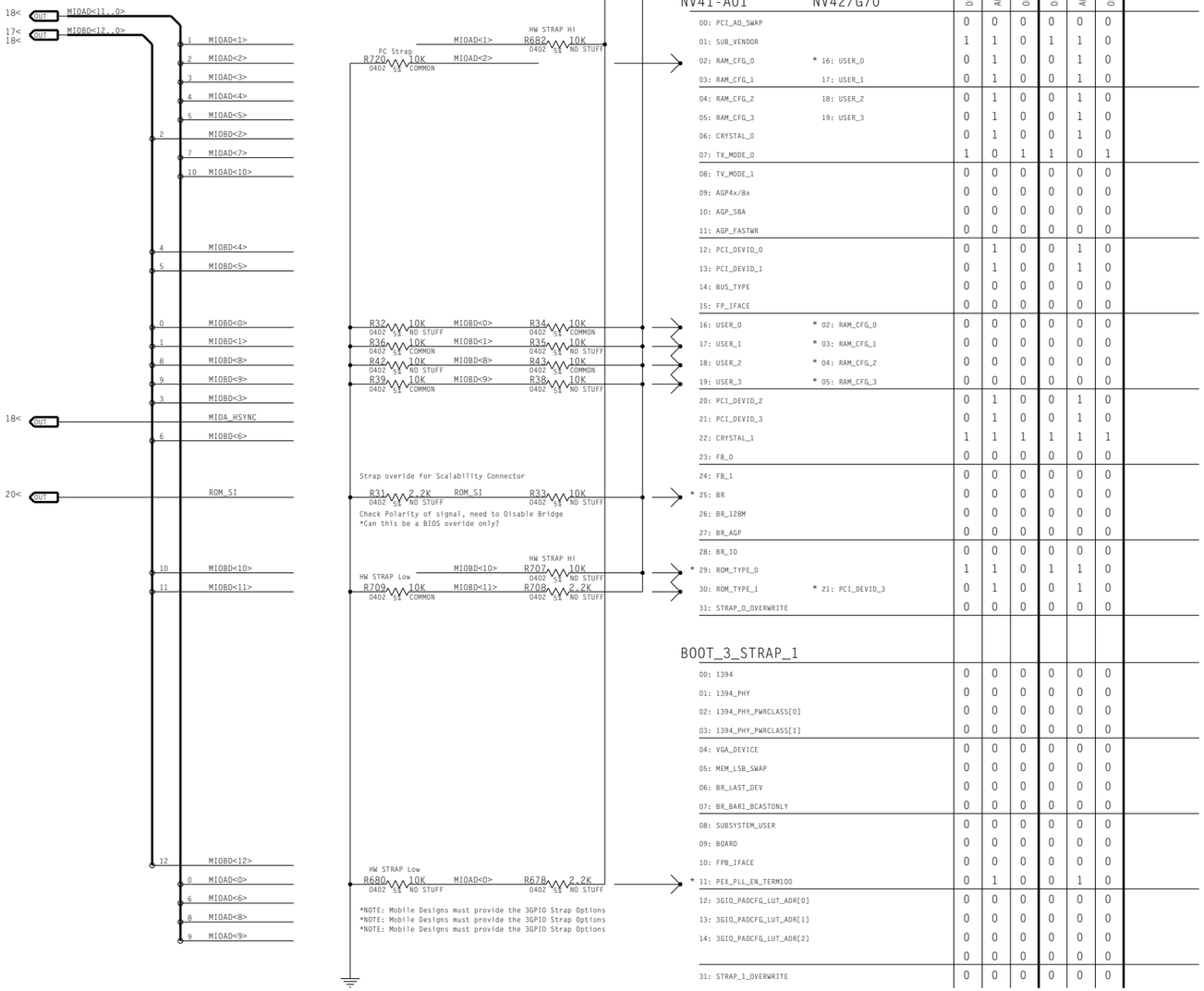


ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	MISC: GPIO, I2C, THERMAL, BIOS, XTAL

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10317-0002-100		
ID	design	PAGE	20 OF 28
NAME	John Lam	DATE	31-MAY-2005

21 Strapping Configuration



Standardized Straps
SUBVENDOR
ROMTYPE[1:0]
PCI_AD
BUS_TYPE
RAMCFG[3:0]
USER[0]
DEVID[3]

AND MASK
1 -> HARDWARE STRAP
0 -> BIOS STRAP

OR MASK
1 -> DESIRED=1 ANDMASK=0

SKU#	(256Mb) 0000			(256Mb) xxxx		
BOOT_0_STRAP_0						
NV41-A01 / **NV41-A02 NV42/G70**	DESIRED	AND MASK	OR MASK	DESIRED	AND MASK	OR MASK
00: PCI_AD_SWAP	0	0	0	0	0	0
01: SUB_VENDOR	1	1	0	1	1	0
02: RAM_CFG_0 * 16: USER_0	0	1	0	0	1	0
03: RAM_CFG_1 17: USER_1	0	1	0	0	1	0
04: RAM_CFG_2 18: USER_2	0	1	0	0	1	0
05: RAM_CFG_3 19: USER_3	0	1	0	0	1	0
06: CRYSTAL_0	0	1	0	0	1	0
07: TV_MODE_0	1	0	1	1	0	1
08: TV_MODE_1	0	0	0	0	0	0
09: AGP4x/Bx	0	0	0	0	0	0
10: AGP_SBA	0	0	0	0	0	0
11: AGP_FASTWR	0	0	0	0	0	0
12: PCI_DEVID_0	0	1	0	0	1	0
13: PCI_DEVID_1	0	1	0	0	1	0
14: BUS_TYPE	0	0	0	0	0	0
15: FP_IFACE	0	0	0	0	0	0
16: USER_0 * 02: RAM_CFG_0	0	0	0	0	0	0
17: USER_1 * 03: RAM_CFG_1	0	0	0	0	0	0
18: USER_2 * 04: RAM_CFG_2	0	0	0	0	0	0
19: USER_3 * 05: RAM_CFG_3	0	0	0	0	0	0
20: PCI_DEVID_2	0	1	0	0	1	0
21: PCI_DEVID_3	0	1	0	0	1	0
22: CRYSTAL_1	1	1	1	1	1	1
23: FB_0	0	0	0	0	0	0
24: FB_1	0	0	0	0	0	0
* 25: BR	0	0	0	0	0	0
26: BR_128M	0	0	0	0	0	0
27: BR_AGP	0	0	0	0	0	0
28: BR_IO	0	0	0	0	0	0
* 29: ROM_TYPE_0	1	1	0	1	1	0
30: ROM_TYPE_1 * 21: PCI_DEVID_3	0	1	0	0	1	0
31: STRAP_0_OVERWRITE	0	0	0	0	0	0
BOOT_3_STRAP_1						
00: 1394	0	0	0	0	0	0
01: 1394_PHY	0	0	0	0	0	0
02: 1394_PHY_PWRCLASS[0]	0	0	0	0	0	0
03: 1394_PHY_PWRCLASS[1]	0	0	0	0	0	0
04: VGA_DEVICE	0	0	0	0	0	0
05: MEM_LSB_SWAP	0	0	0	0	0	0
06: BR_LAST_DEV	0	0	0	0	0	0
07: BR_BAR1_BCASTONLY	0	0	0	0	0	0
08: SUBSYSTEM_USER	0	0	0	0	0	0
09: BOARD	0	0	0	0	0	0
10: FPB_IFACE	0	0	0	0	0	0
* 11: PEX_PLL_EN_TERM100	0	1	0	0	1	0
12: 3GIO_PADCFG_LUT_ADR[0]	0	0	0	0	0	0
13: 3GIO_PADCFG_LUT_ADR[1]	0	0	0	0	0	0
14: 3GIO_PADCFG_LUT_ADR[2]	0	0	0	0	0	0
	0	0	0	0	0	0
31: STRAP_1_OVERWRITE	0	0	0	0	0	0

NV41-A01 Strap Mapping
Last Checked Dec 19, 2003

HW Default		BIT FUNCTION	NORMAL PIN (RTL Name)
	0	PCI_AD	'NV_PEXTDEV_BOOT_0_STRAP_PCI_AD_NORMAL
1	1	SUB_VENDOR	MIOAD1 (Ccira_data[1])
	2	RAMCFG[0]	MIOAD2 (Ccira_data[2])
	3	RAMCFG[1]	MIOAD3 (Ccira_data[3])
	4	RAMCFG[2]	MIOAD4 (Ccira_data[4])
	5	RAMCFG[3]	MIOAD5 (Ccira_data[5])
0	6	CRYSTAL[0]	MIOBD2 (Ccirb_data[2])
1	7	TVMODE[0]	MIOAD7 (Ccira_data[7])
0	8	TVMODE[1]	MIOAD10 (Ccira_data[10])
	9	AGP_4X	'NV_PEXTDEV_BOOT_0_STRAP_AGP_4X_DISABLED
	10	AGP_SBA	'NV_PEXTDEV_BOOT_0_STRAP_AGP_SBA_DISABLED
	11	AGP_FASTWR	'NV_PEXTDEV_BOOT_0_STRAP_AGP_FASTWR_DISABLED
0	12	PCI_DEVID[0]	MIOBD4 (Ccirb_data[4])
0	13	PCI_DEVID[1]	MIOBD5 (Ccirb_data[5])
	14	AGP	'NV_PEXTDEV_BOOT_0_STRAP_BUS_TYPE_PCI
	15	FP_IFACE	'NV_PEXTDEV_BOOT_0_STRAP_FP_IFACE_12BIT
	16	Strap_user[0]	MIOBD0 (Ccirb_data[0])
	17	Strap_user[1]	MIOBD1 (Ccirb_data[1])
	18	Strap_user[2]	MIOBD8 (Ccirb_data[8])
	19	Strap_user[3]	MIOBD9 (Ccirb_data[9])
0	20	PCI_DEVID[2]	MIOBD3 (Ccirb_data[3])
0	21	PCI_DEVID[3]	MIOA_HSYNC (ccira_hsync)
	22	CRYSTAL[1]	MIOBD6 (Ccirb_data[6])
	23	FB[0]	0
	24	FB[1]	1
1	25	BR	ROM_SI (Rom_si)
	26	BR_128M	'NV_PEXTDEV_BOOT_0_STRAP_BR_REG_128M_DISABLED
	27	BR_AGP	'NV_PEXTDEV_BOOT_0_STRAP_BR_AGP_DEV_DISABLED
	28	BR_IO	'NV_PEXTDEV_BOOT_0_STRAP_BR_IO_DEV_DISABLED
1	29	ROMTYPE[0]	MIOBD10 (Ccirb_data[10])
0	30	ROMTYPE[1]	MIOBD11 (Ccirb_data[11])

NV_STRAP_1

BIT FUNCTION	NORMAL PIN (RTL Name)
0 1394	'NV_PEXTDEV_BOOT_3_STRAP_1_1394_DISABLED
1 1394_PHY	'NV_PEXTDEV_BOOT_3_STRAP_1_1394_PHY_DISABLED
2 1394_PHY_PWRCLASS[0]	0
3 1394_PHY_PWRCLASS[1]	0
4 VGA_DEVICE	'NV_PEXTDEV_BOOT_3_STRAP_1_VGA_DEVICE_ENABLED
5 MEM_LSB_SWAP	'NV_PEXTDEV_BOOT_3_STRAP_1_MEM_LSB_SWAP_DISABLED
6 BR_LAST_DEV	'NV_PEXTDEV_BOOT_3_STRAP_1_BR_LAST_DEV_DISABLED
7 BR_BAR1_BCASTONLY	'NV_PEXTDEV_BOOT_3_STRAP_1_BR_BAR1_BCASTONLY_ENABLED
8 SUBSYSTEM_USER	'NV_PEXTDEV_BOOT_3_STRAP_1_SUBSYSTEM_USER_DISABLED
9 BOARD	'NV_PEXTDEV_BOOT_3_STRAP_1_BOARD_0
1 10 FPB_IFACE	MIOBD12 (Ccirb_data[12])
0 11 PEX_PLL_EN_TERM100	MIOAD0 (Ccira_data[0])
0 12 3GIO_PADCFG_LUT_ADR[0]	MIOAD6 (Ccira_data[6])
0 13 3GIO_PADCFG_LUT_ADR[1]	MIOAD8 (Ccira_data[8])
0 14 3GIO_PADCFG_LUT_ADR[2]	MIOAD9 (Ccira_data[9])

*HW has Internal 10K Strap, need 1K to overide

SUB_VENDOR[0]	0 - NO_BIOS 1 - READ FROM BIOS (DESIRED)
RAM_CFG[3:0]	0000 N/A 0001 N/A 0010 N/A 0011 N/A 0100 N/A 0101 N/A 0110 N/A 0111 8PCS 8Mx32 SAMSUNG DDR3
CRYSTAL[1:0]	00 - 13.5 MHz 01 - 14.31818 MHz 10 - 27.000 MHz (DESIRED) 11 - UNKNOWN
TVMODE[1:0]	00 - SECAM 01 - NTSC (DESIRED) 10 - PAL 11 - CRT
PCI_DEVID[3:0]	0000 = NV41 = 0x0000 1100 = NV41-U-A1 = 0x0CC0
USER[3:0]	0000 - USER STRAP
FB[1:0]	00 - 64MEG (DESIRED) 01 - 128MEG 10 - 256MEG 11 - 512MEG
ROM_TYPE[1:0]	00 - PARALLEL (NOT SUPPORTED) 01 - SERIAL AT25F (DESIRED) 10 - SERIAL SST45VF/LF 11 - RFU
BR	0 - ENABLE 1 - DISABLED (Default)
FPB_IFACE	0 - 12Bit 1 - 24bit (Default)
PEX_PLL_EN_TERM100	0 - ENABLED (Internal 100ohm Term) 1 - DISABLED
3GIO_PADCFG_LUT_ADR[2:0]	000 = DEFAULT
STRAP_OVERWITE	0 - DISABLED (DESIRED) 1 - ENABLED

NV41-A02 Strap Mapping
Updated May 19, 2004

NV_STRAP_0

BIT FUNCTION	NORMAL PIN (RTL Name)
0 PCI_AD	'NV_PEXTDEV_BOOT_0_STRAP_PCI_AD_NORMAL
1 SUB_VENDOR	MIOAD1 (Ccira_data[1])
2 RAMCFG[0]	MIOBD0 (Ccirb_data[0])
3 RAMCFG[1]	MIOBD1 (Ccirb_data[1])
4 RAMCFG[2]	MIOBD8 (Ccirb_data[8])
5 RAMCFG[3]	MIOBD9 (Ccirb_data[9])
6 CRYSTAL0	MIOBD2 (Ccirb_data[2])
7 TVMODE[0]	MIOAD7 (Ccira_data[7])
8 TVMODE[1]	MIOAD10 (Ccira_data[10])
9 AGP_4X	'NV_PEXTDEV_BOOT_0_STRAP_AGP_4X_DISABLED
10 AGP_SBA	'NV_PEXTDEV_BOOT_0_STRAP_AGP_SBA_DISABLED
11 AGP_FASTWR	'NV_PEXTDEV_BOOT_0_STRAP_AGP_FASTWR_DISABLED
12 PCI_DEVID0[0]	MIOBD4 (Ccirb_data[4])
13 PCI_DEVID0[1]	MIOBD5 (Ccirb_data[5])
14 AGP	'NV_PEXTDEV_BOOT_0_STRAP_BUS_TYPE_AGP
15 FP_IFACE	'NV_PEXTDEV_BOOT_0_STRAP_FP_IFACE_12BIT
16 USER[0]	MIOAD2 (Ccira_data[2])
17 USER[1]	MIOAD3 (Ccira_data[3])
18 USER[2]	MIOAD4 (Ccira_data[4])
19 USER[3]	MIOAD5 (Ccira_data[5])
20 PCI_DEVID32[0]	MIOBD3 (Ccirb_data[3])
21 PCI_DEVID32[1]	MIOBD11 (Ccirb_data[11])
22 CRYSTAL1	MIOBD6 (Ccirb_data[6])
23 FB[0]	0
24 FB[1]	1
25 BR	ROM_SI (Rom_si)
26 BR_128M	'NV_PEXTDEV_BOOT_0_STRAP_BR_REG_128M_DISABLED
27 BR_AGP	'NV_PEXTDEV_BOOT_0_STRAP_BR_AGP_DEV_DISABLED
28 BR_IO	'NV_PEXTDEV_BOOT_0_STRAP_BR_IO_DEV_DISABLED
29 ROMTYPE[0]	MIOBD10 (Ccirb_data[10])
30 ROMTYPE[1]	0

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	Strapping Configuration

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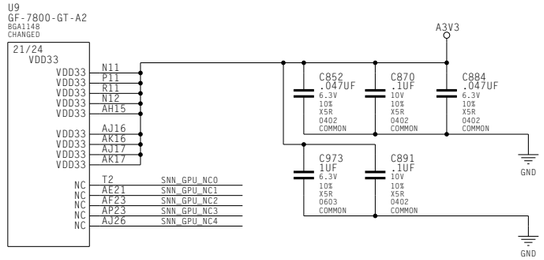
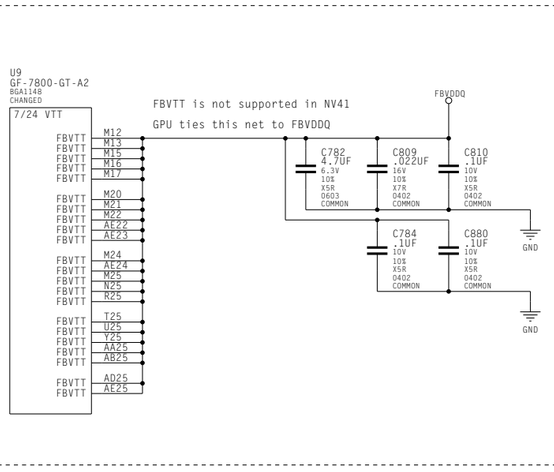
22 Power/GND and Decoupling

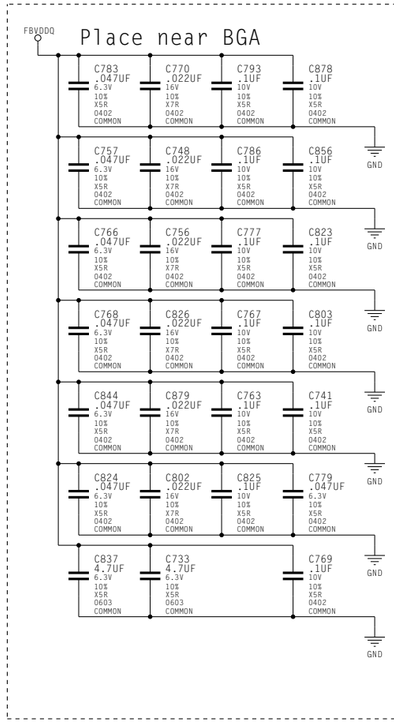
VDD33



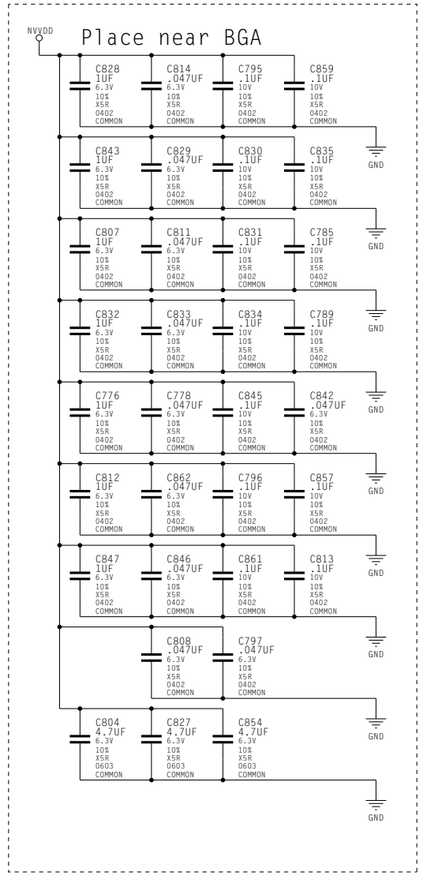
FBVTT

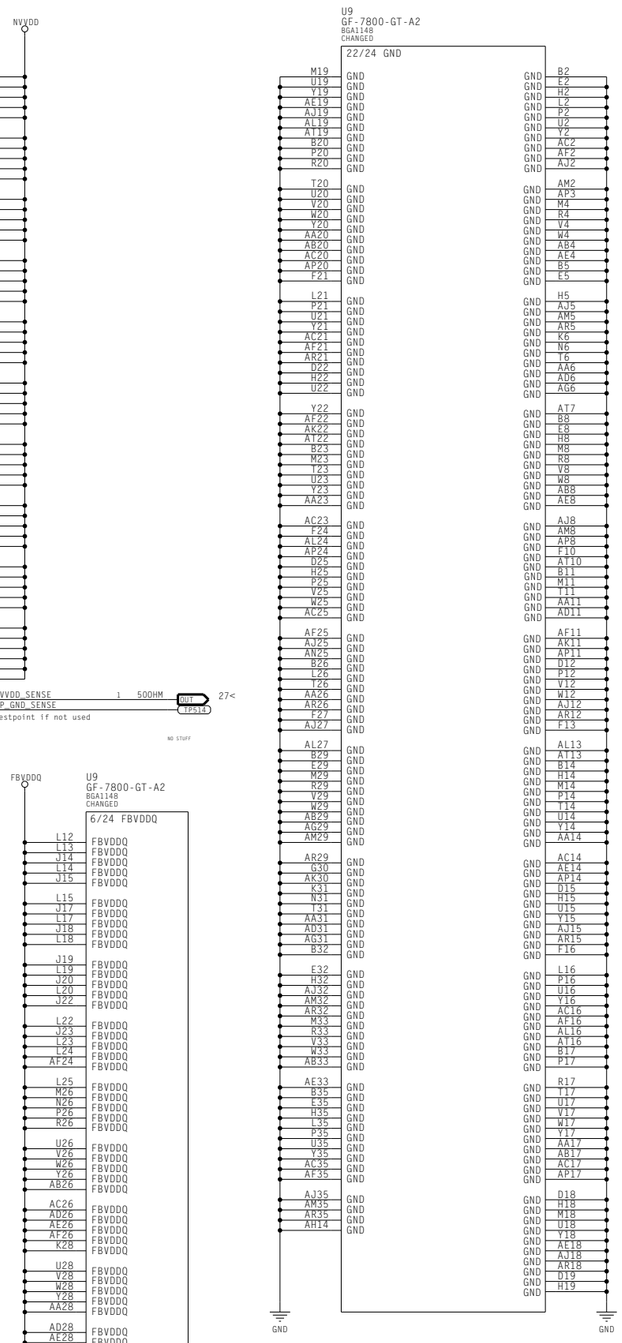


FBVDDQ



NVVDD





ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	Power/GND and Decoupling

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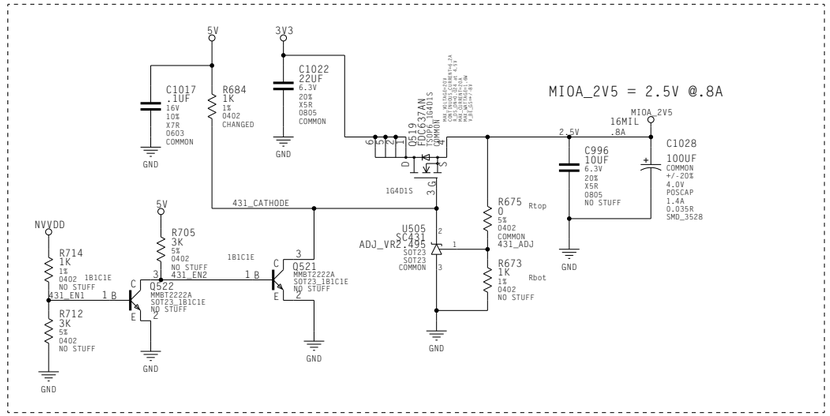
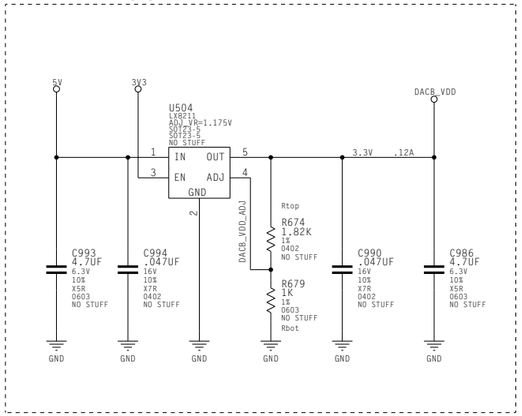
23 Power Supply I: TMDS/MIOA/DACB Alternate Supplies

MIOA_VDDQ



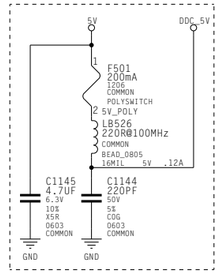
Vout = Vref * (1+Rtop/Rbot)
Vout = 2.5V * (1+0R/NO STUFF) = 2.5V

DACB Supply



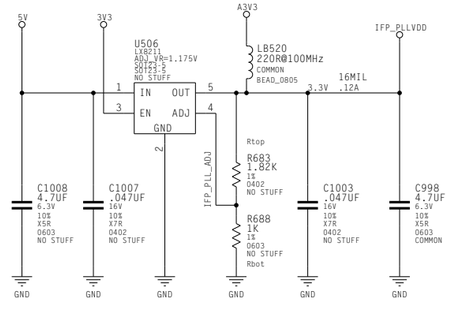
Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+1820/1000)

DDC_5V



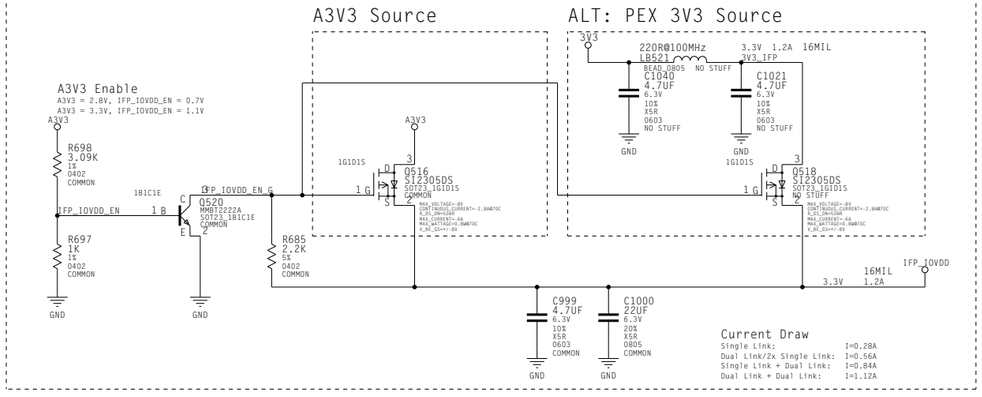
*E-DDC v1.1 spec requires only 50mA per connector
*Stereo requires 300mA per connector

TMDS PLL Supply



Vout = VRef * (1+Rtop/Rbot)
2.8V = 1.175V * (1+1400/1000)
3.31V = 1.175V * (1+1820/1000)

TMDS IOVDD Backdrive Prevention



ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	Power Supply I: TMDS/MIOA/DACB Alternate Supplies

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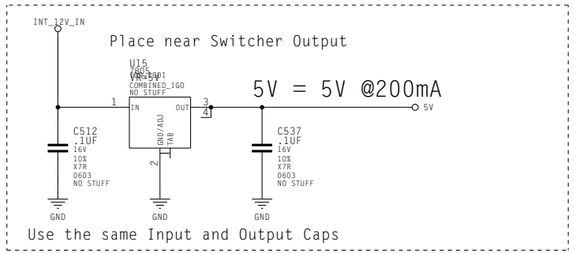
24 Power Supply II: 5V and A3V3

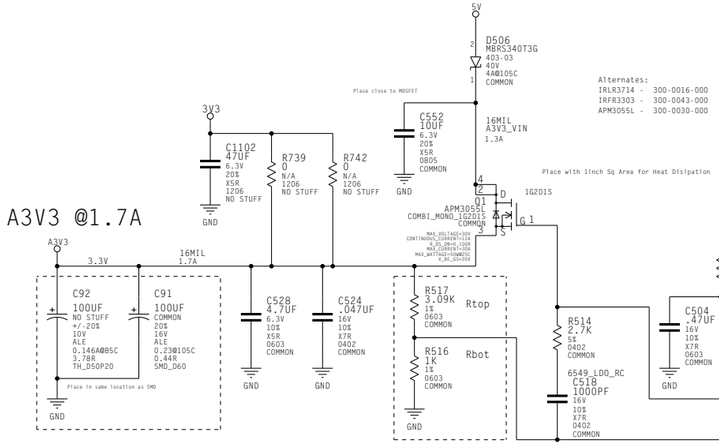
Alternate 5V regulator

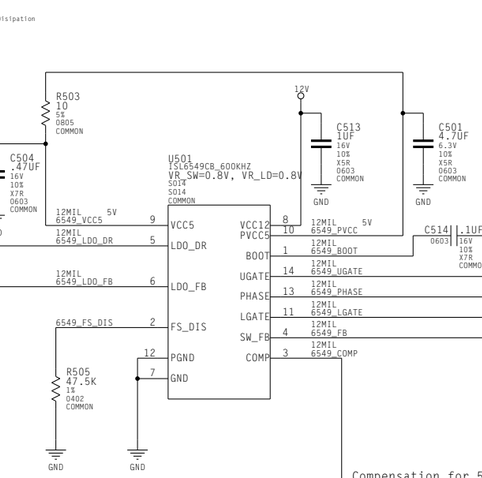


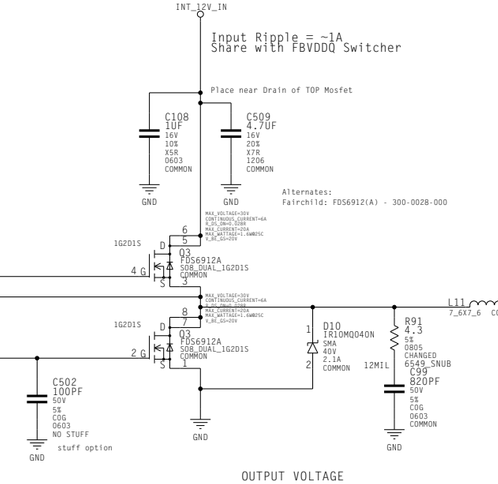
Only use this Alternate when A3V3 regulator is not Stuffed

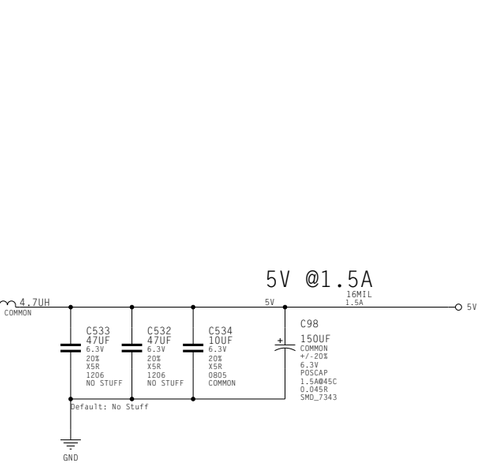
Conditions for Linear 5V:
1- If all Analog 3.3V circuits are tested to +/-10% tolerance
2- 5V Linear will supply DDC 5V + Diode protection circuits
3- Must Not use when Stereo is an Option

A3V3 @1.7A

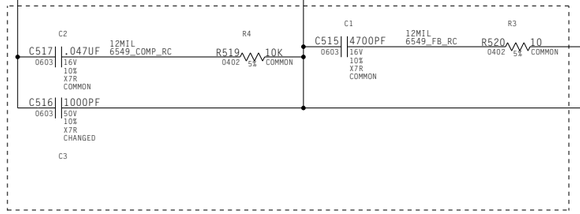




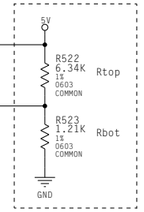




Compensation for 5V

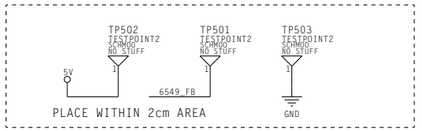


OUTPUT VOLTAGE



Vout = 0.8V * (1 + Rtop/Rbot)
5V = 0.8V * (1 + 6.34K/1.21K)

Shmoo TestPoints



ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	Power Supply II: 5V and A3V3

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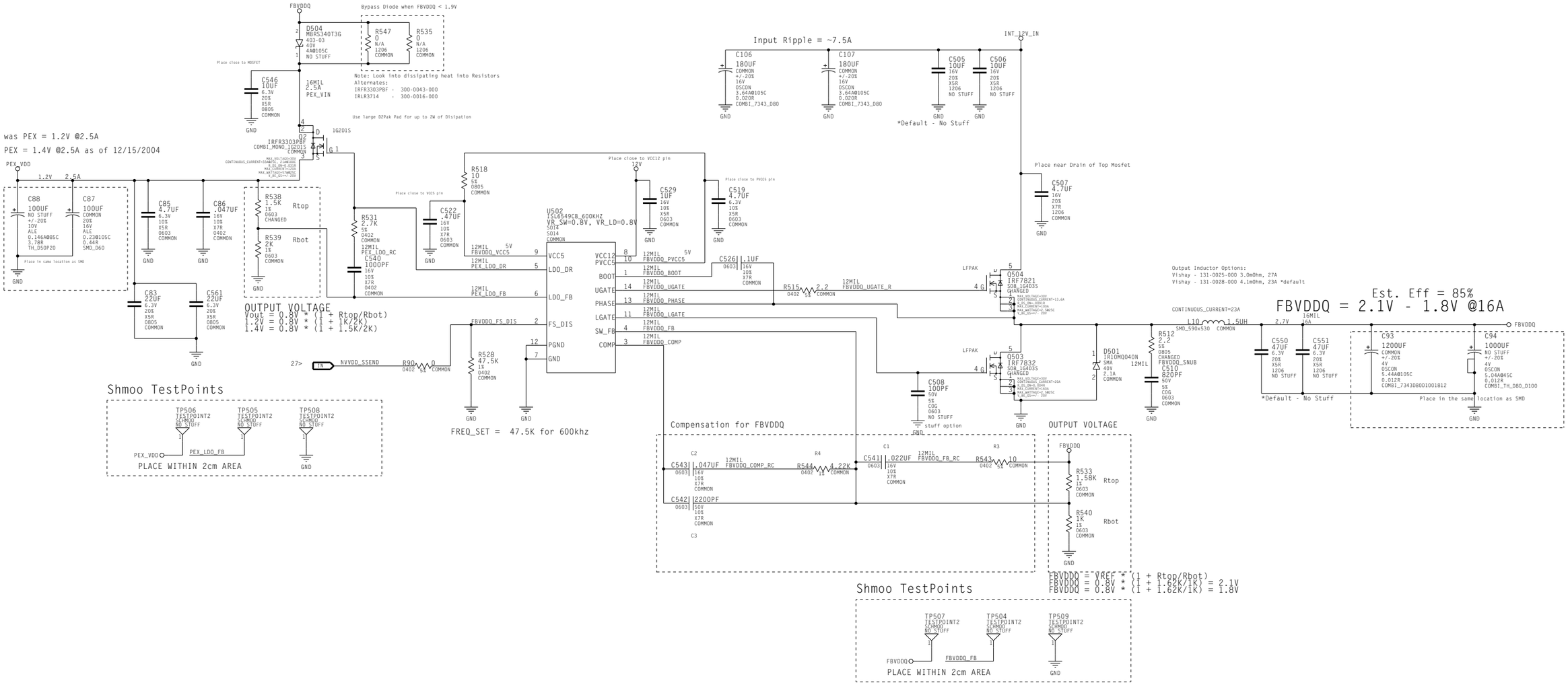
25 Power Supply III: FBVDDQ and PEX_VDD



ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	Power Supply III: FBVDDQ and PEX_VDD

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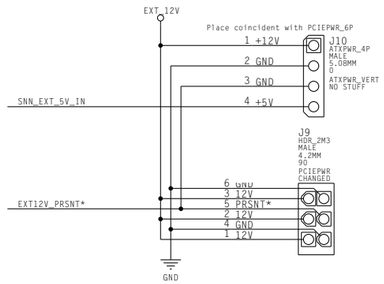
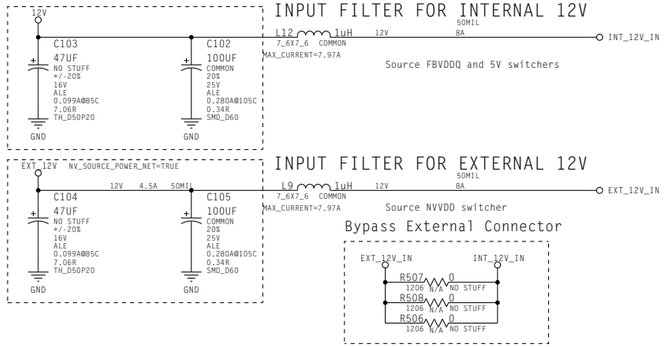
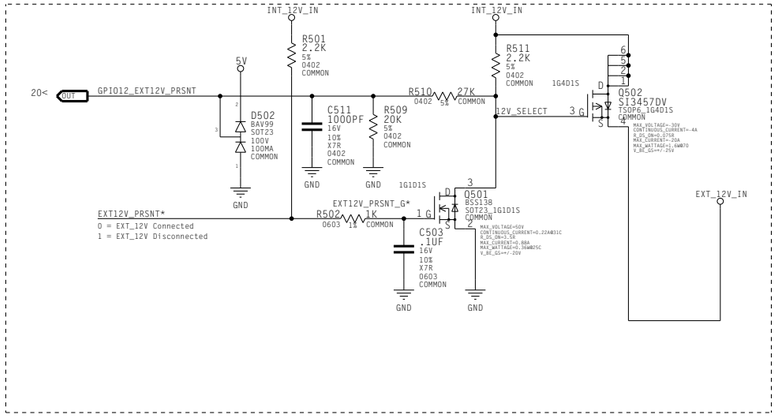
26 Power Supply IV: External 12V Power + NVVDD VID Control

Internal & External 12V Input Filters

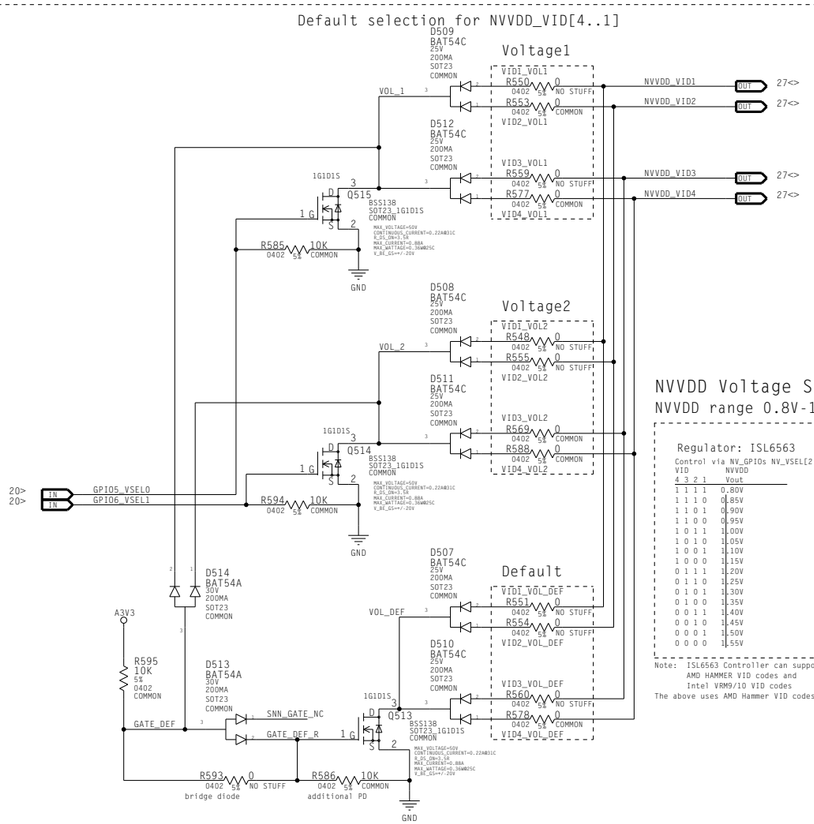




12V Input Selection for NVVDD



NVVDD VID CONTROL



NVVDD Voltage Select

NVVDD range 0.8V-1.55V

Regulator: ISL6563

Control via NV_GPIOs NV_VSEL[2..0] :

VID 4 3 2 1	NVVDD Vout
1 1 1 1	0.80V
1 1 1 0	0.85V
1 1 0 1	0.90V
1 1 0 0	0.95V
1 0 1 1	1.00V
1 0 1 0	1.05V
1 0 0 1	1.10V
1 0 0 0	1.15V
0 1 1 1	1.20V
0 1 1 0	1.25V
0 1 0 1	1.30V
0 1 0 0	1.35V
0 0 1 1	1.40V
0 0 1 0	1.45V
0 0 0 1	1.50V
0 0 0 0	1.55V

Note: ISL6563 Controller can support
AMD HAMMER VID codes and
Intel VRM9/10 VID codes
The above uses AMD Hammer VID codes

SKU Specific Codes

SKU		VID 4 3 2 1 0	NVVDD Vout
600-50317-0000 600-50317-0001	Default	0 1 0 0 1	1.325V
600-10317-0000	Default	0 1 1 1 0	1.200V
	Voltage1	0 1 0 1 0	1.300V
	Voltage2	0 0 1 1 0	1.400V
600-50317-0002	Default	0 1 1 0 1	1.225V
	Voltage1	0 0 1 1 1	1.375V
	Voltage2	0 0 1 1 1	1.375V

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	Power Supply IV: External 12V Power + NVVDD VID Control

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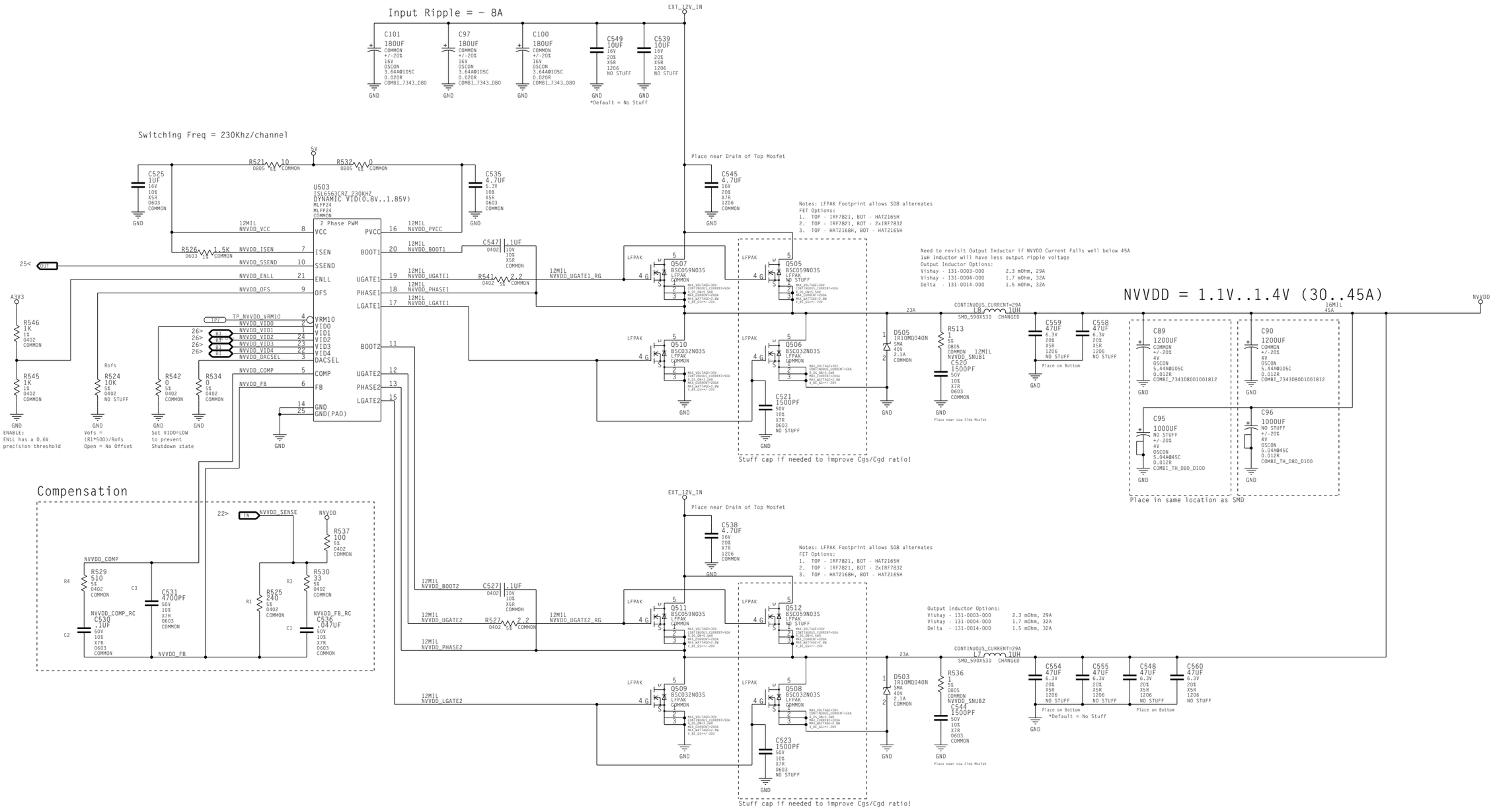
27 Power Supply V: NVVDD



ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
PAGE DETAIL	Power Supply V: NVVDD

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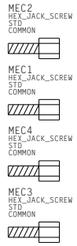
28 Mechanical: Bracket/Thermal Solution

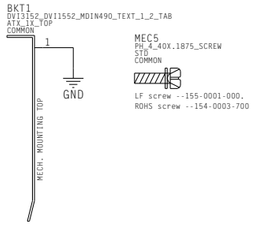
Brackets:

151-10001-0006-000 DVI,DVI,MDIN (text - 1-South, 2-North)
151-10001-0006-001 DB15,DVI,MDIN
151-10001-0006-002 DVI,DB15,MDIN
151-10001-0006-003 DB15,DB15,MDIN (text - 1-South, 2-North)

Connector Screws



Bracket Screw



Heatsink

365-00000-0008-001 - TM30 Fansink + memory heatsink interface material
095-0013-000 - TM30 Fansink
095-0014-000 - TM30 Quadro Fansink
285-00006-0000-000 - Interface Material

ALLEGRO FOOTPRINT SYMBOLS
FAN_GPU_2_68X3_30_B
HEATSINK_GPU_2_35X2_72_B
HEATSINK_MEM_5_34X3_52_B

ASSEMBLY	GF-7800-A2 - 256MB 8Mx32, DL-DVI + SL-DVI + HDTV/VIVO
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