

PG600-B02 NI GHTHAWK

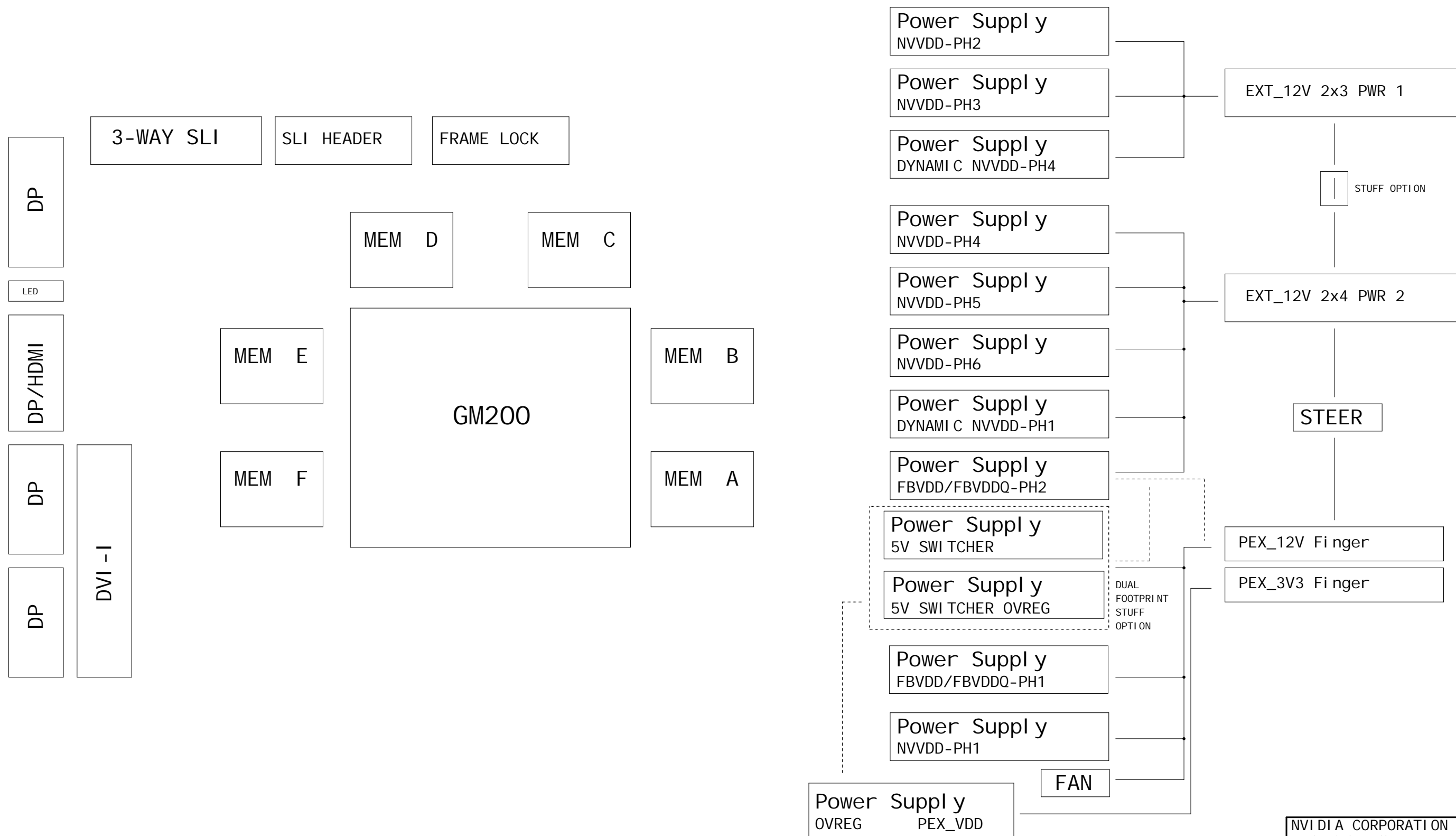
GB3B-384, 6GB GDDR5 128Mx32

DP + HDMI /DP + DP + DP + DVI -I

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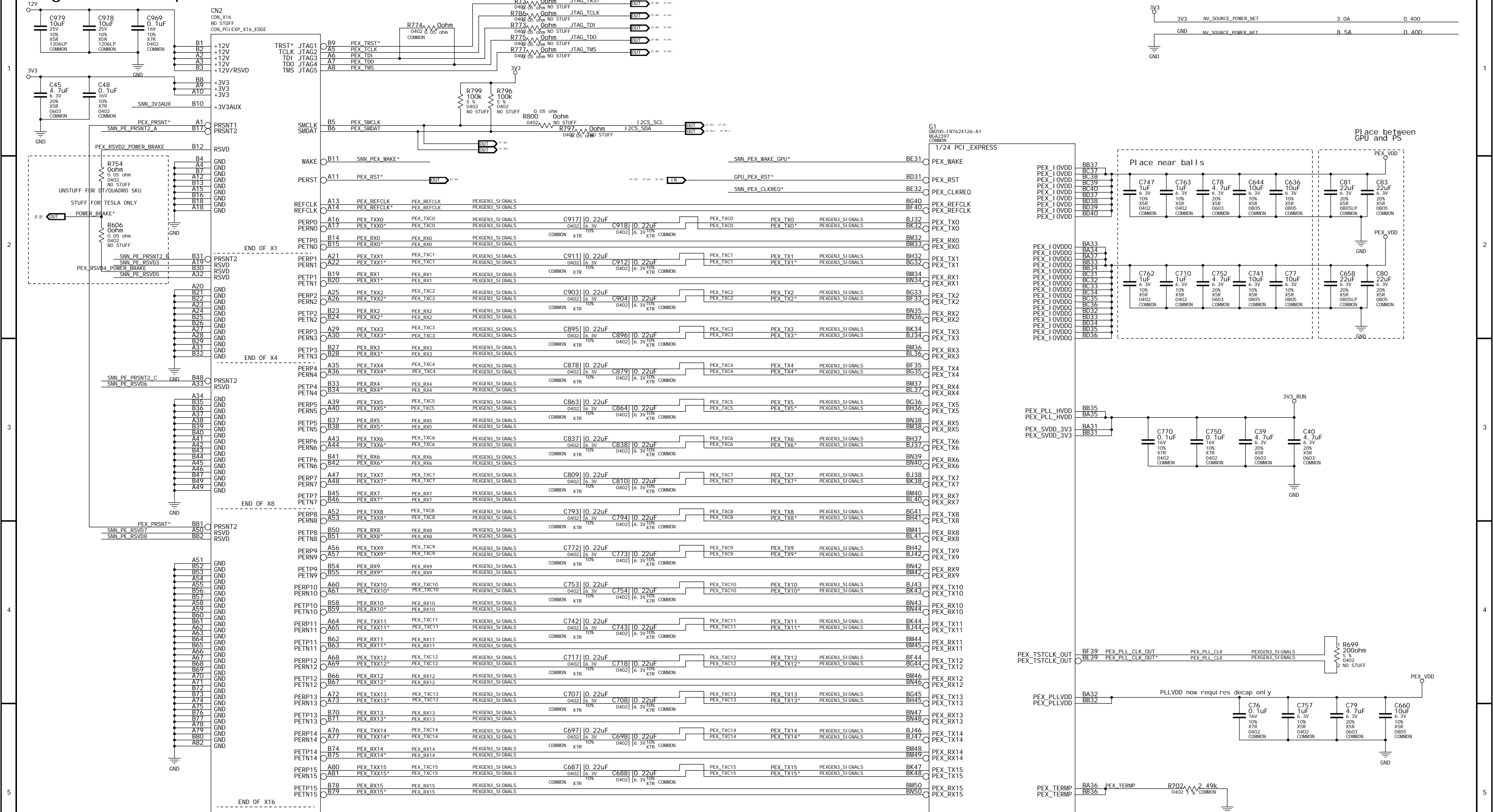


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PAGE DETAIL	Block Diagram

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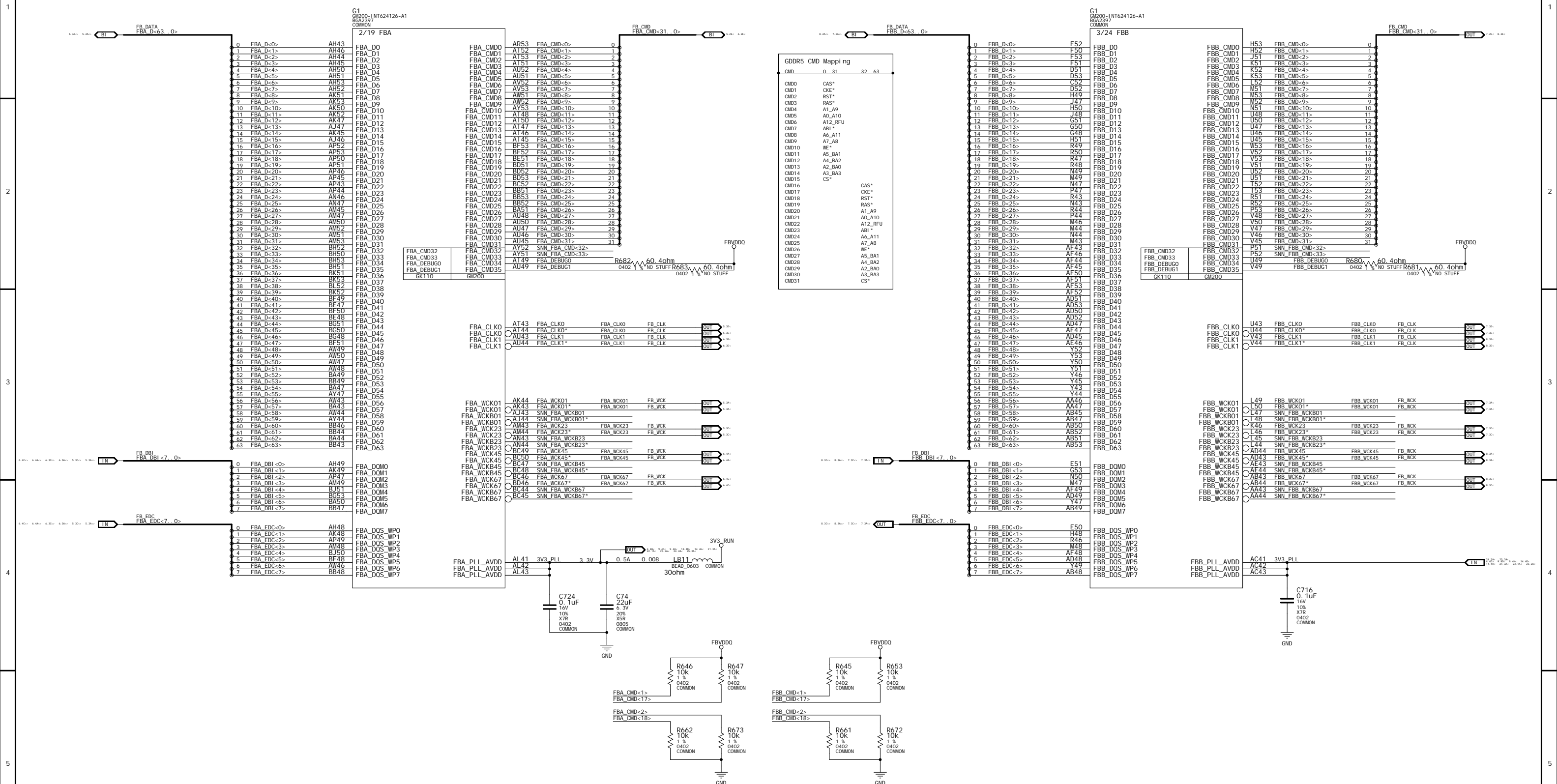
Page3: PCI Express

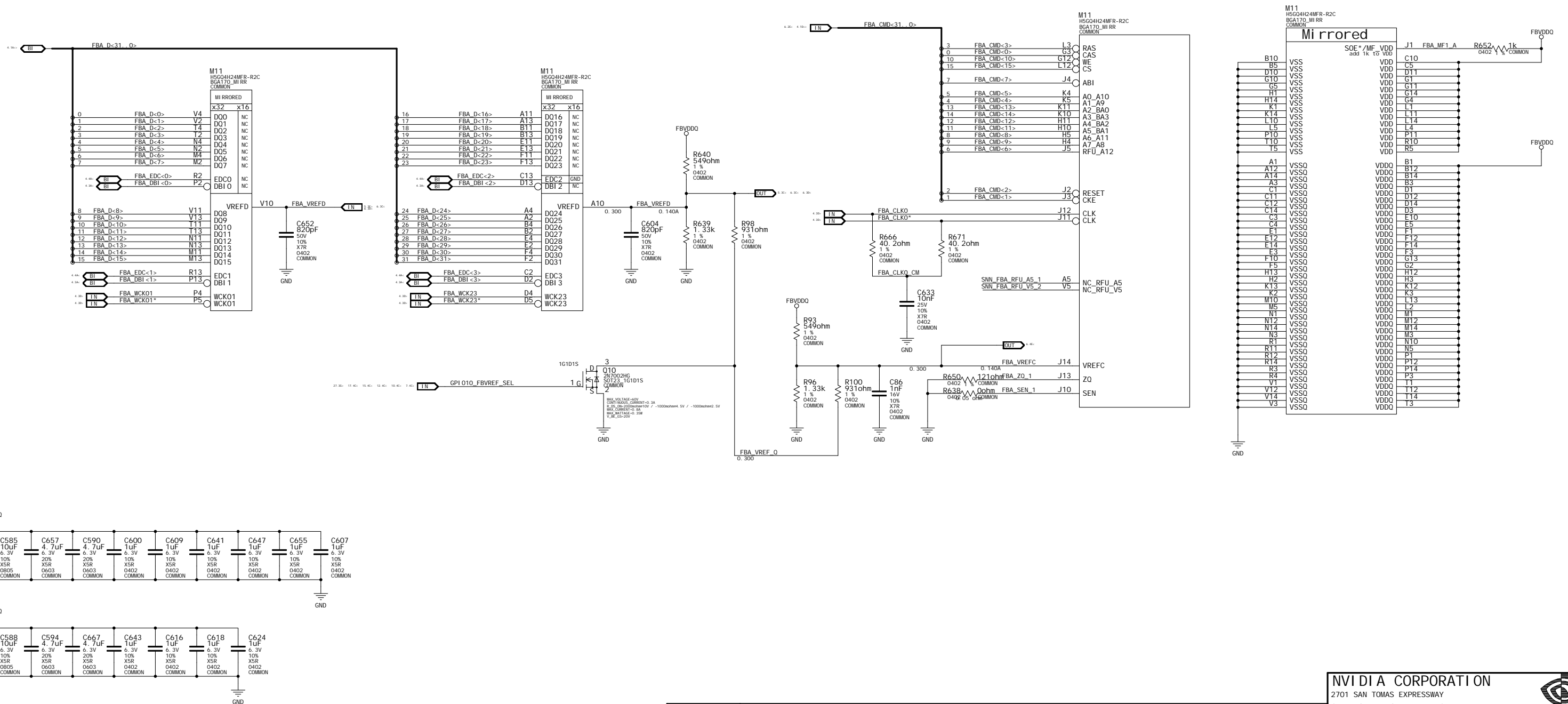


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PAGE DETAIL	PCI Express

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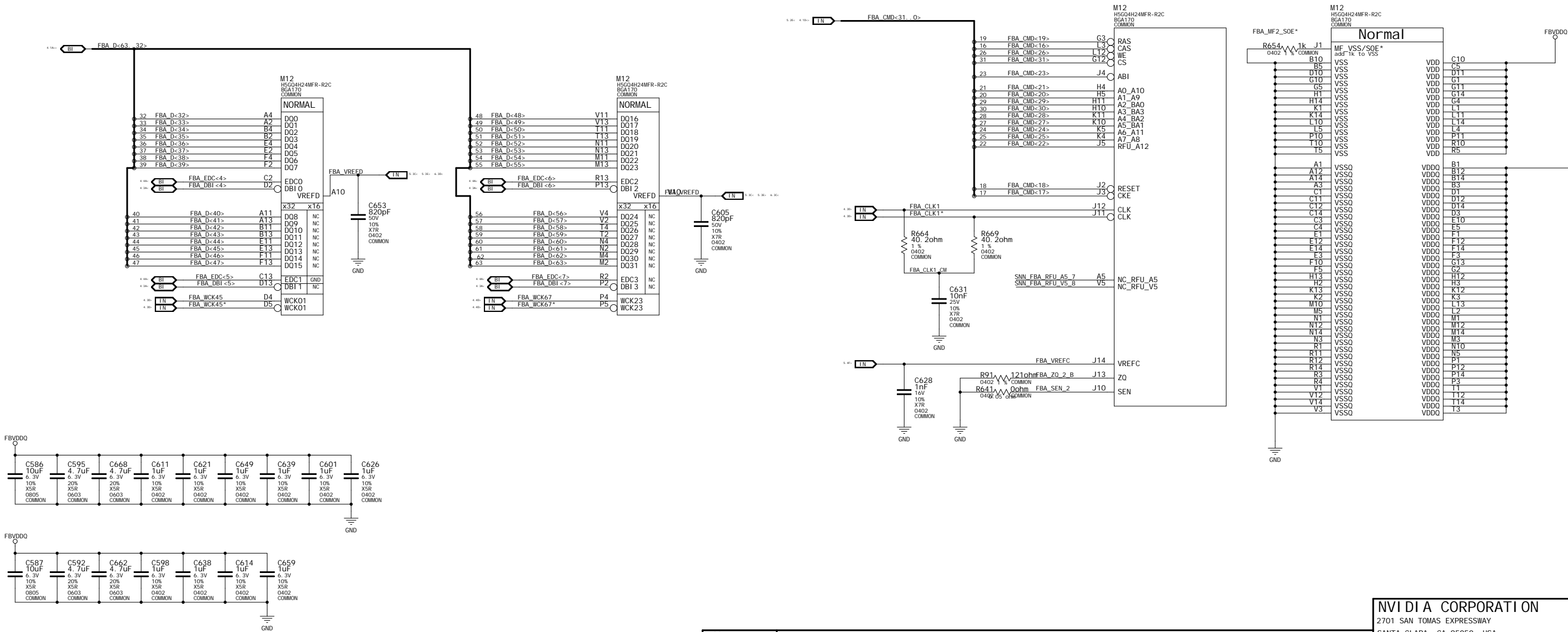
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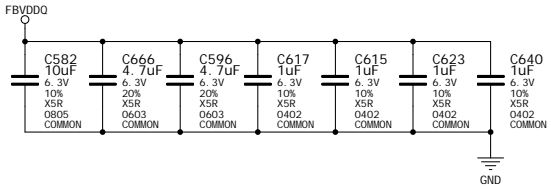
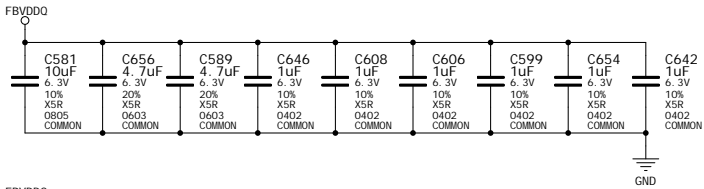
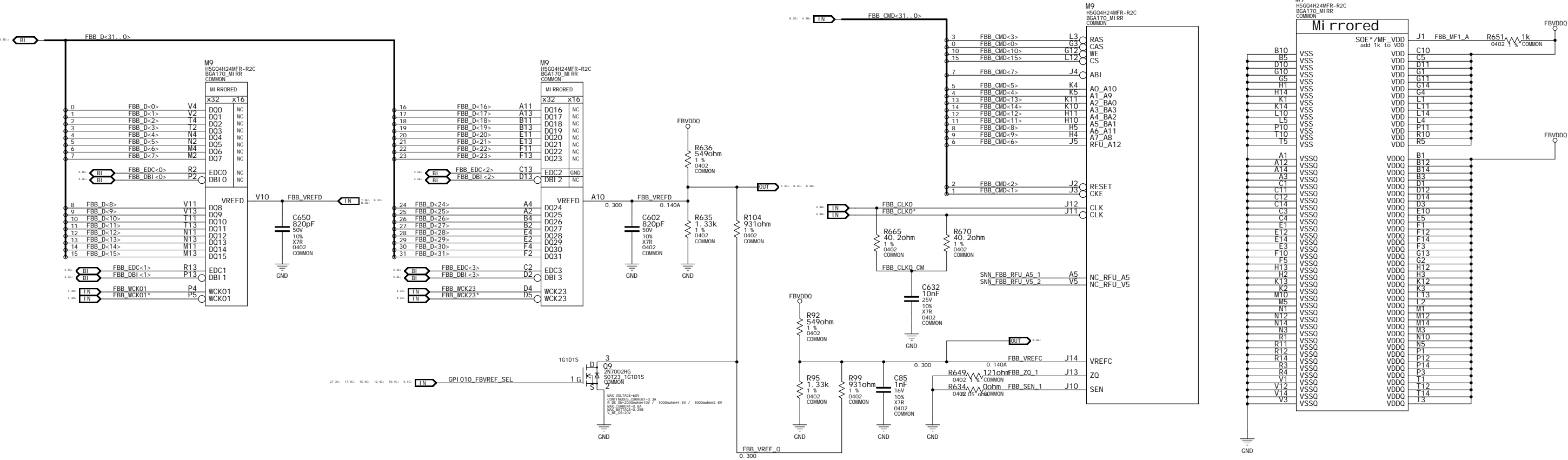
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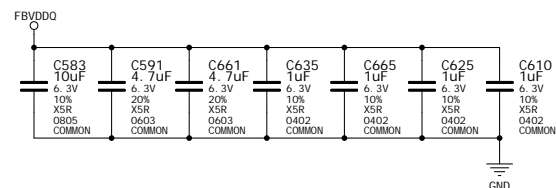
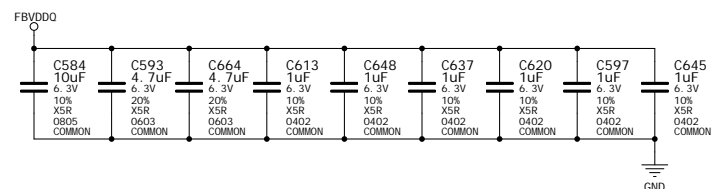
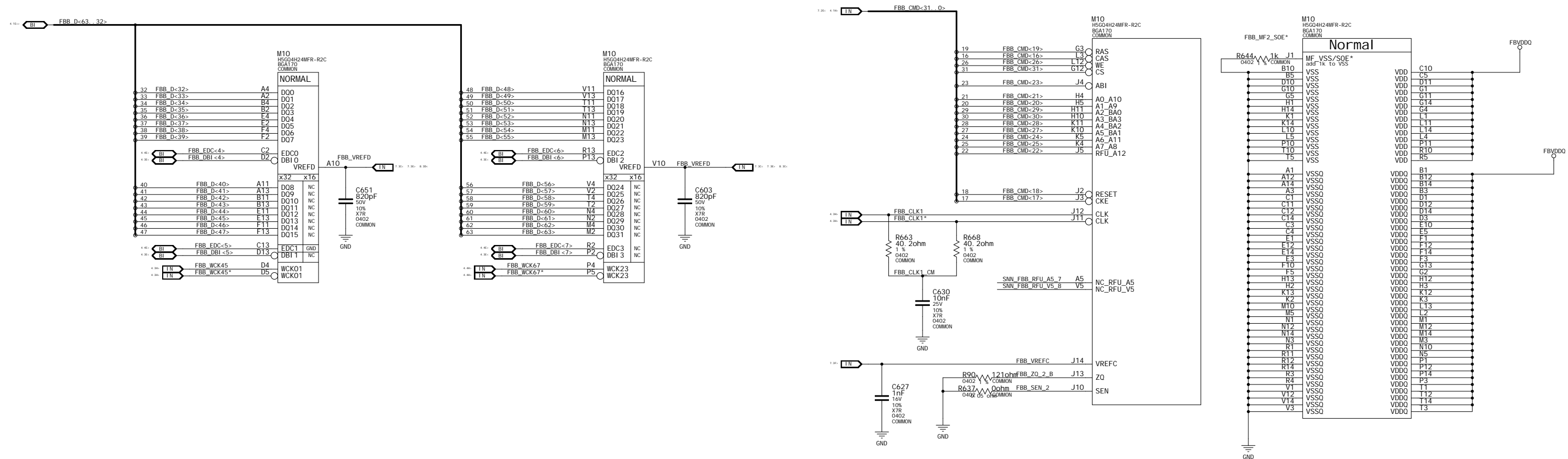
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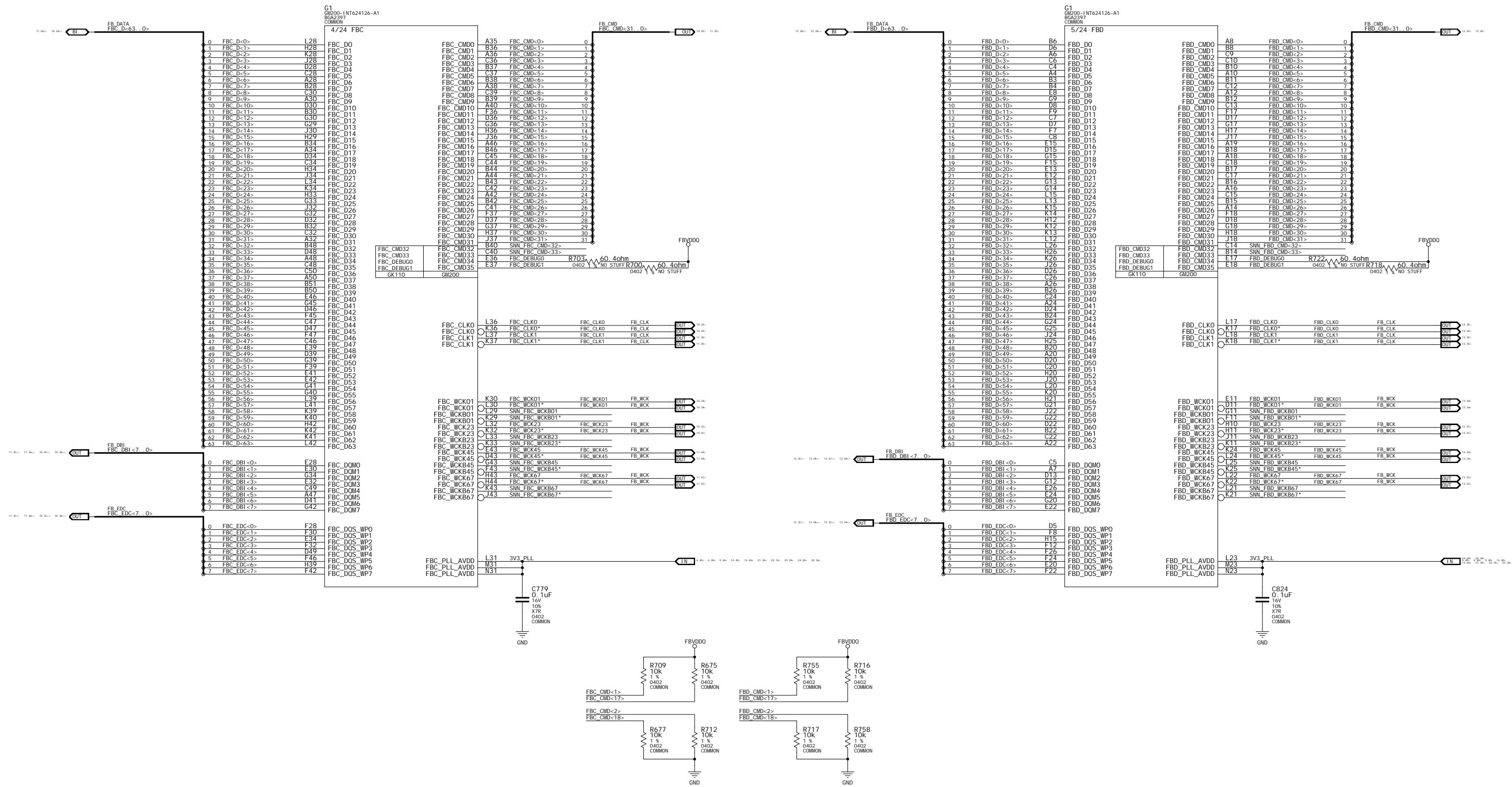
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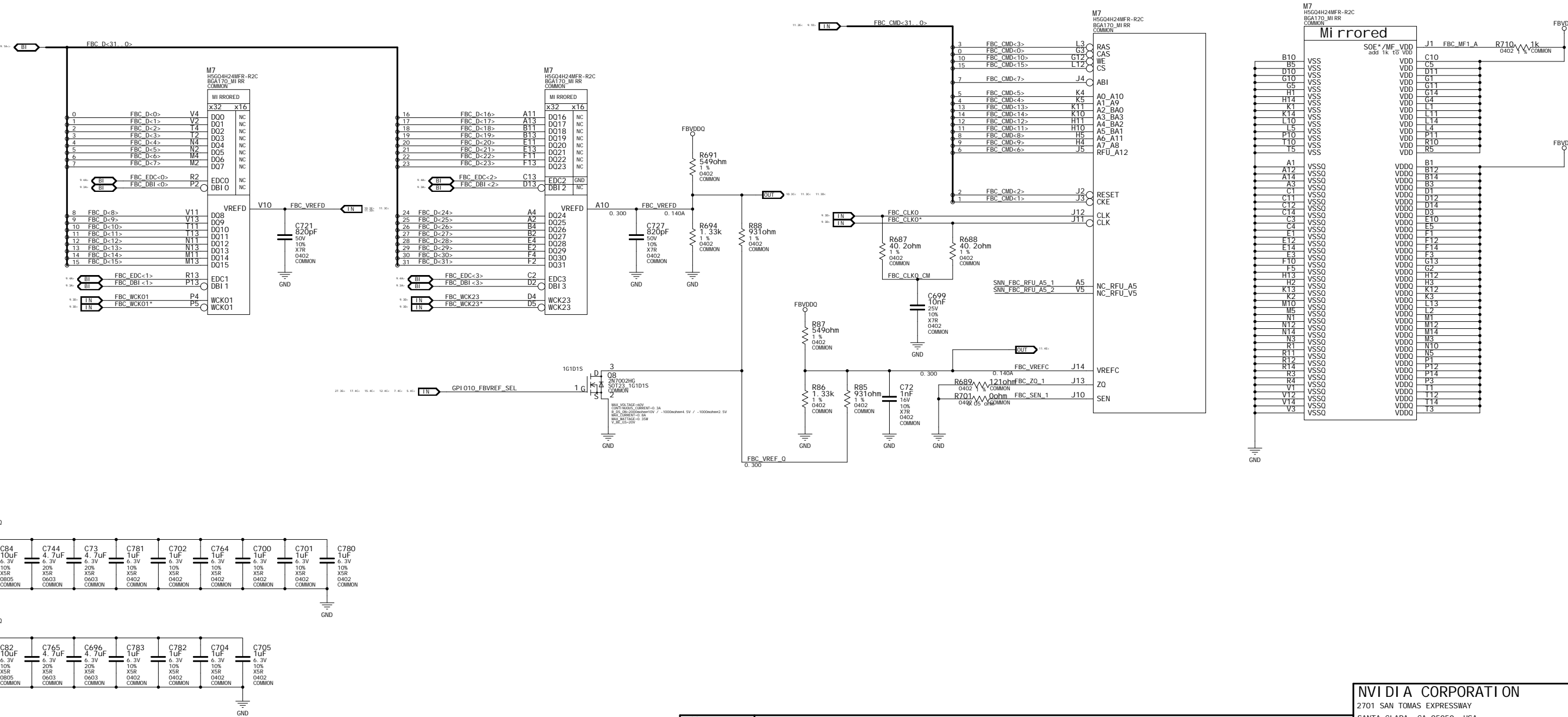
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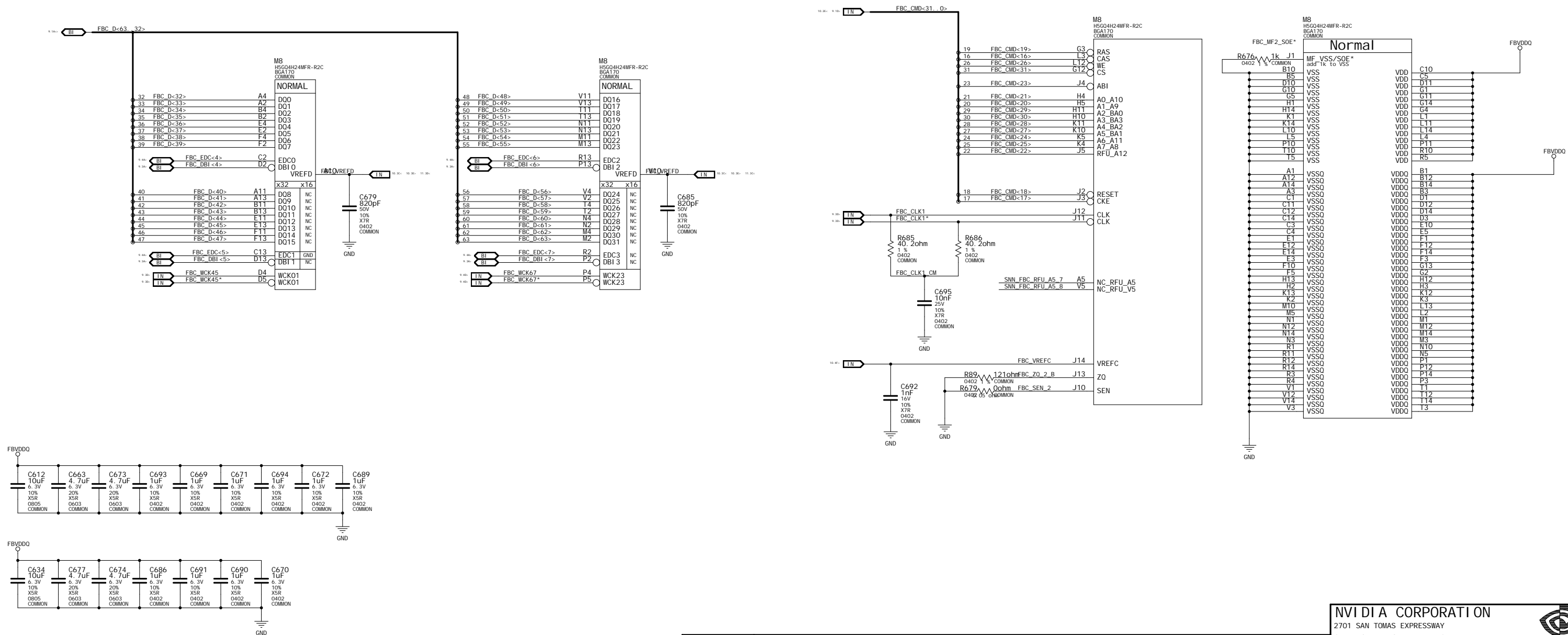
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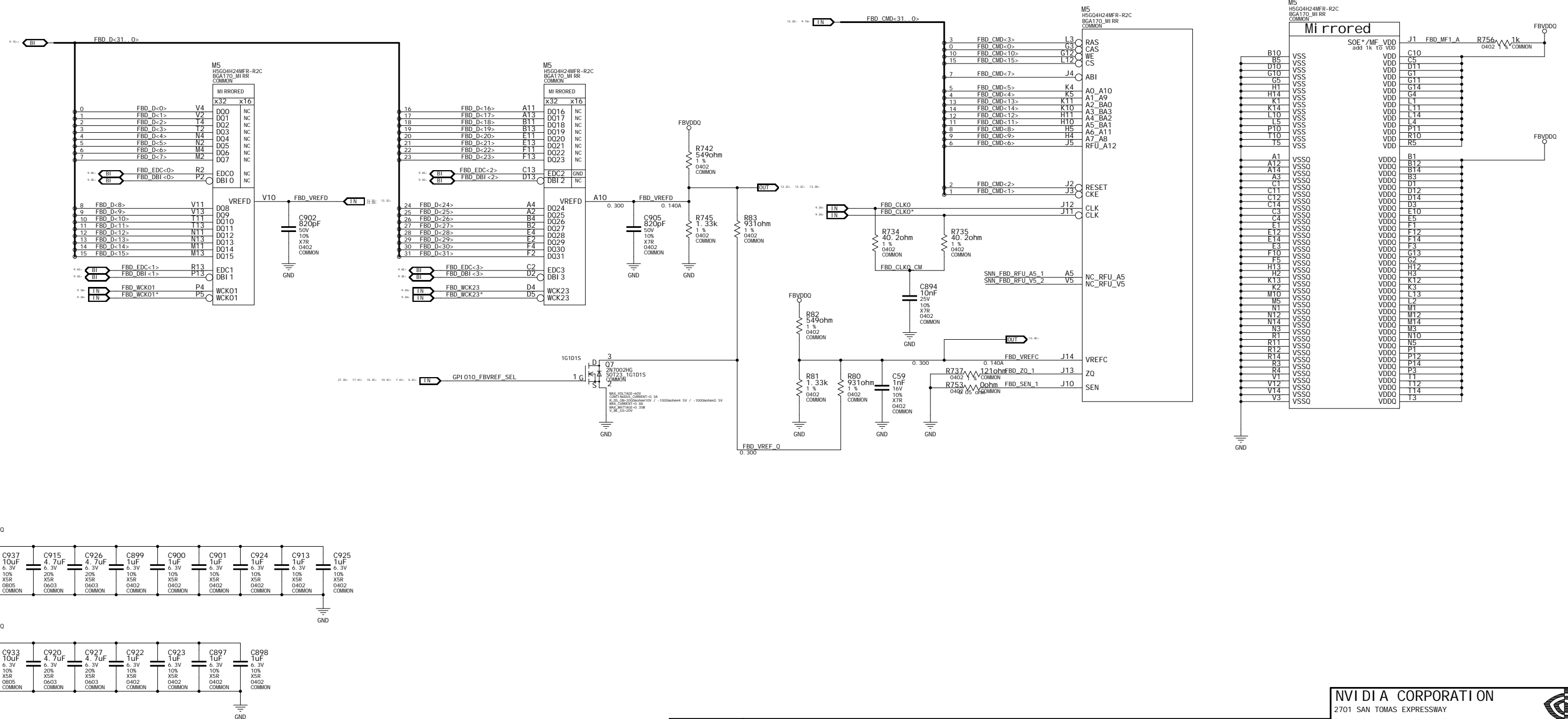
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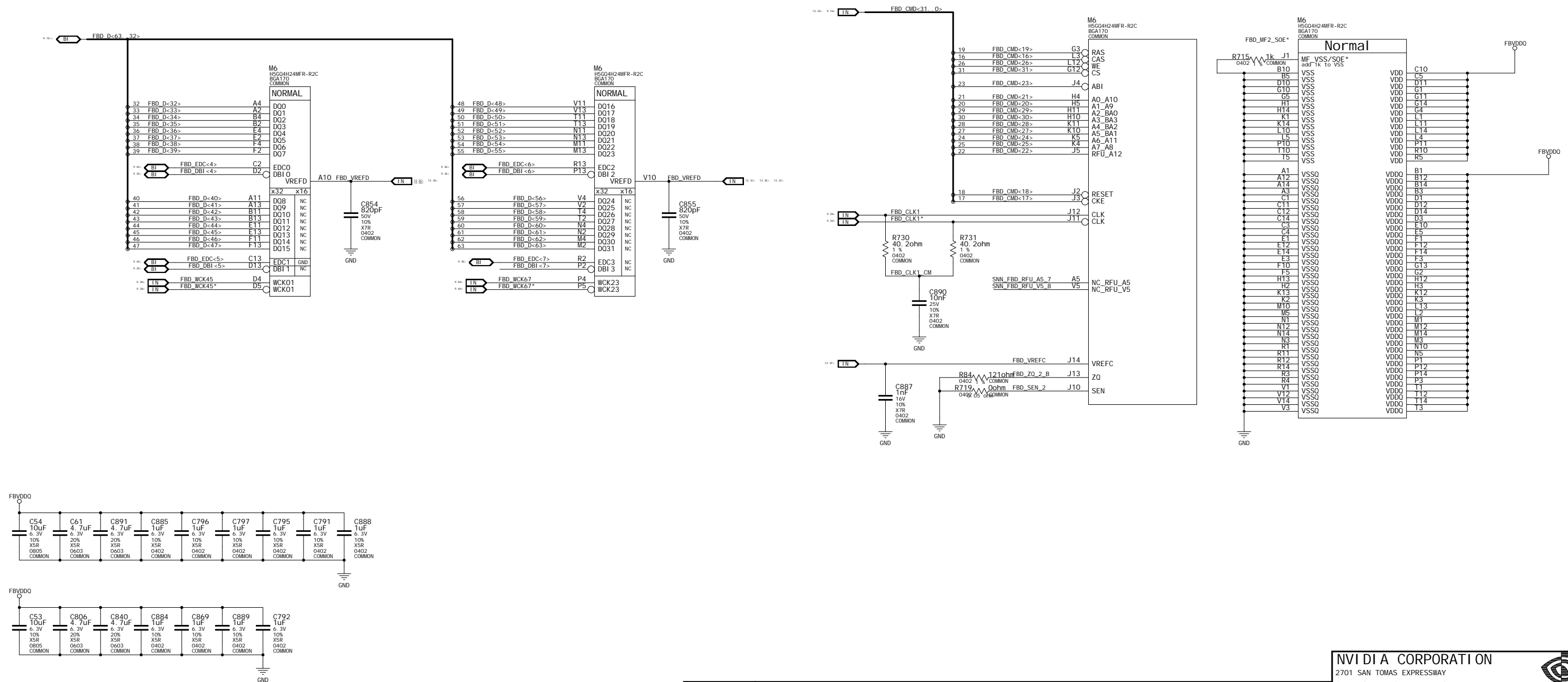


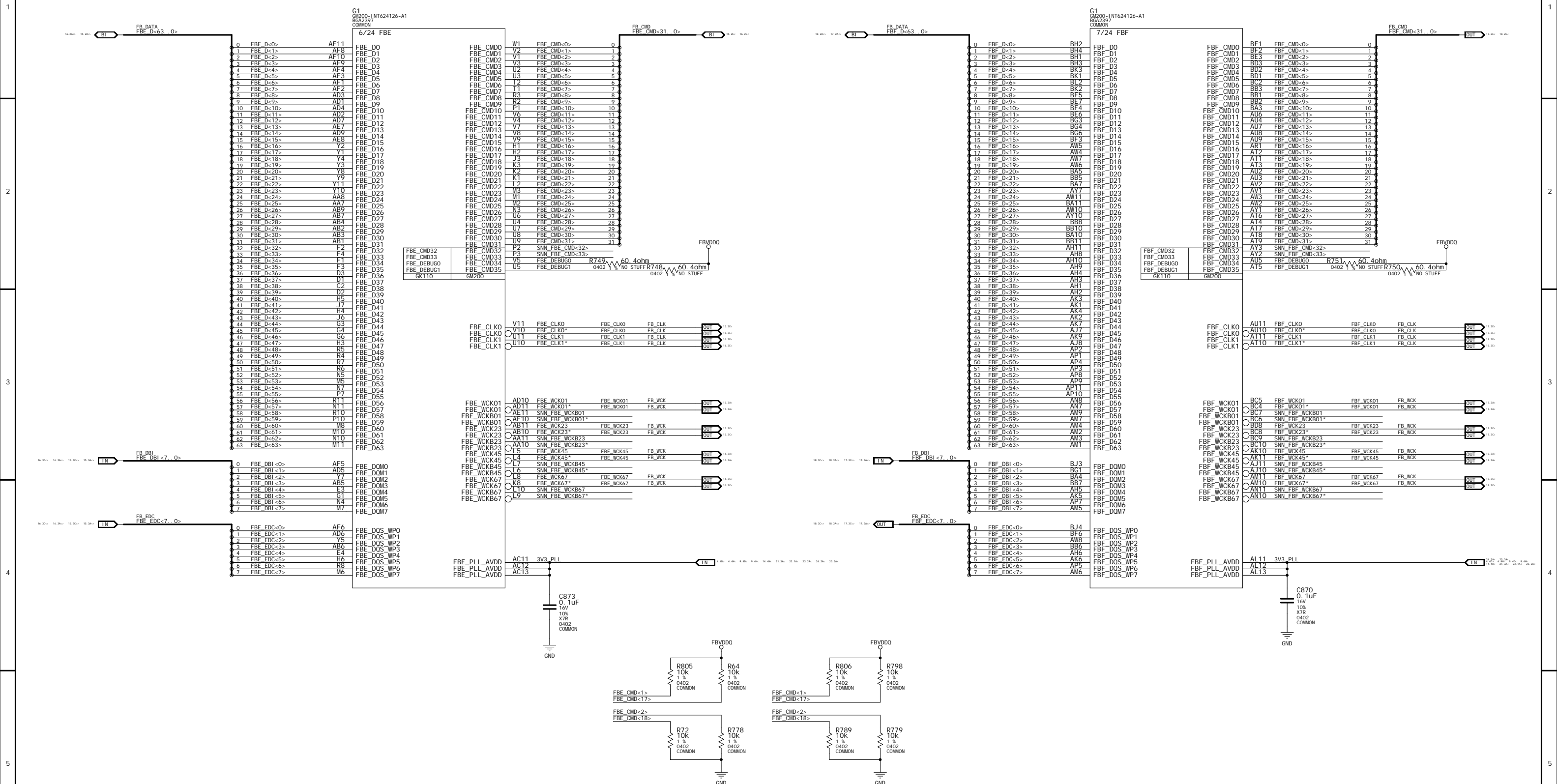


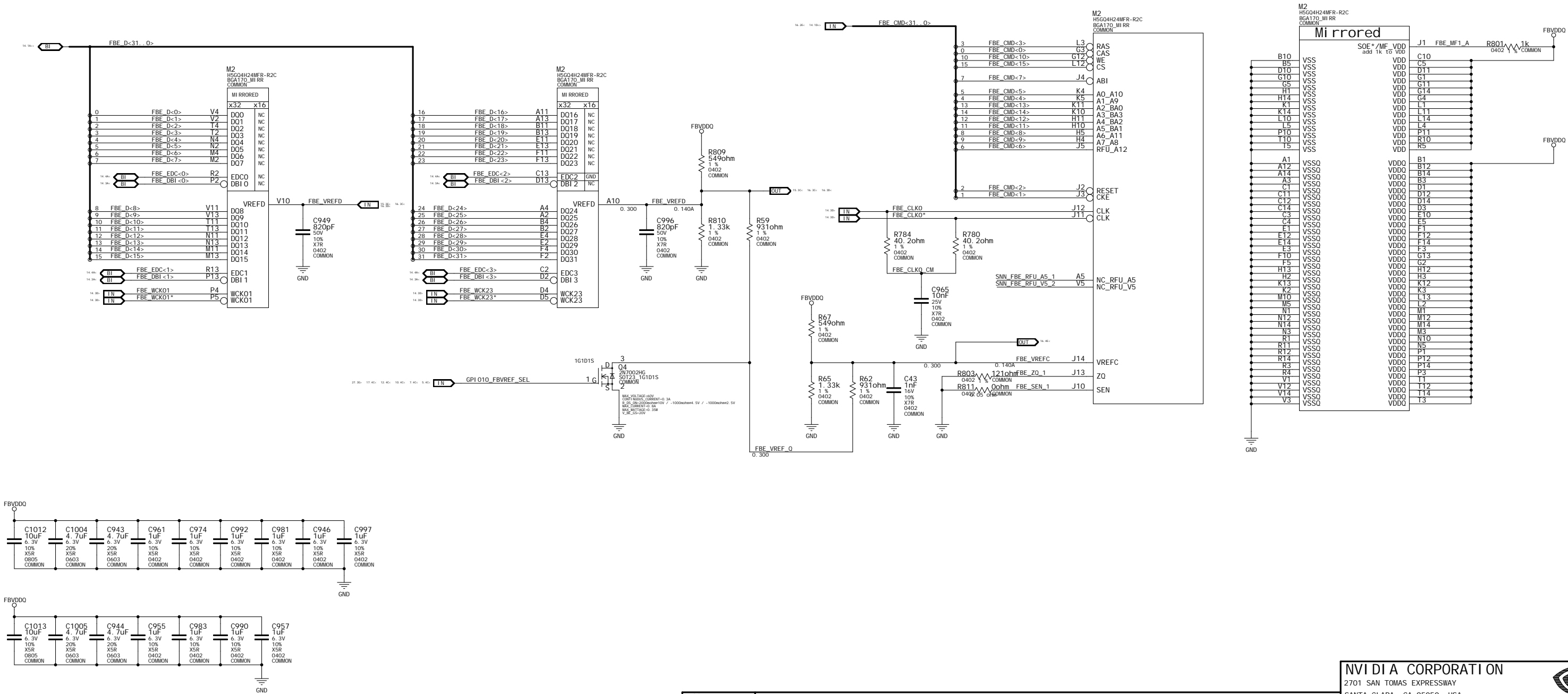
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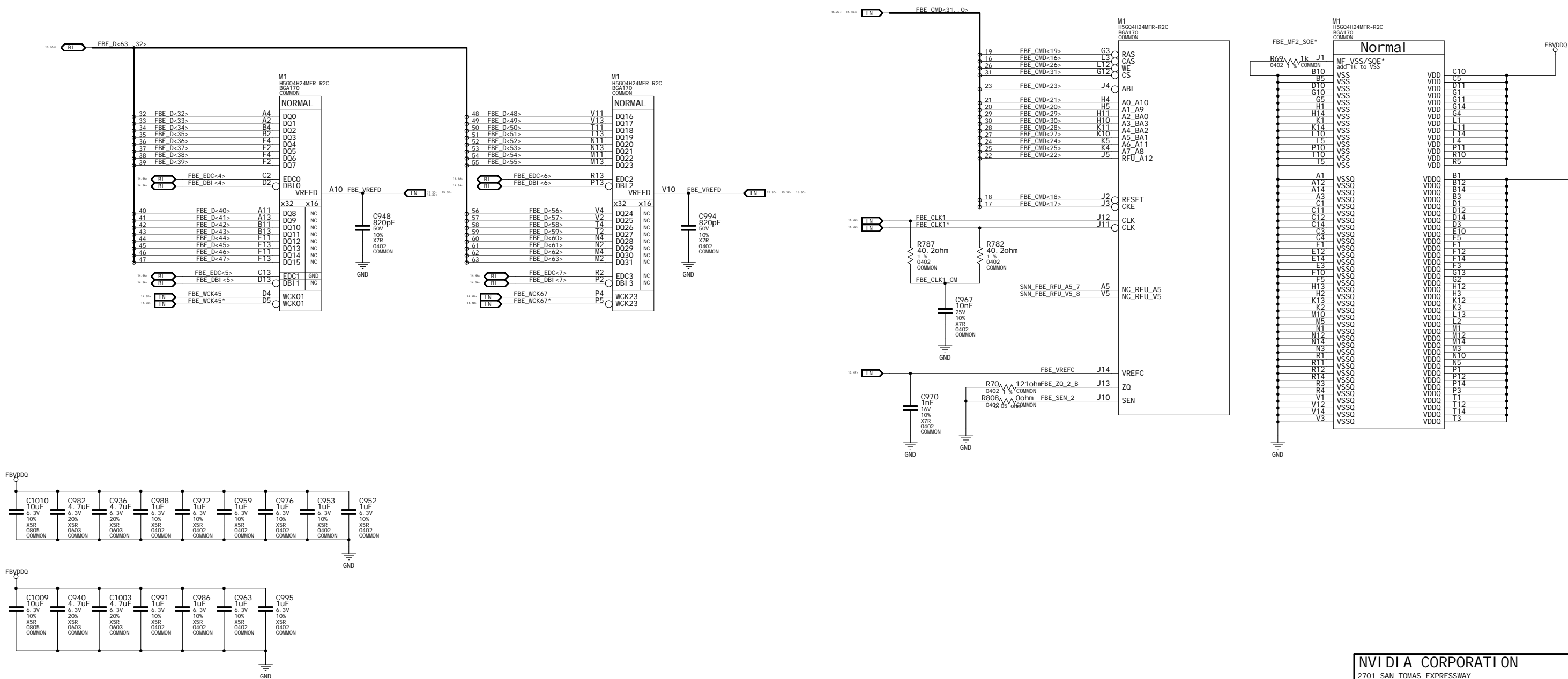




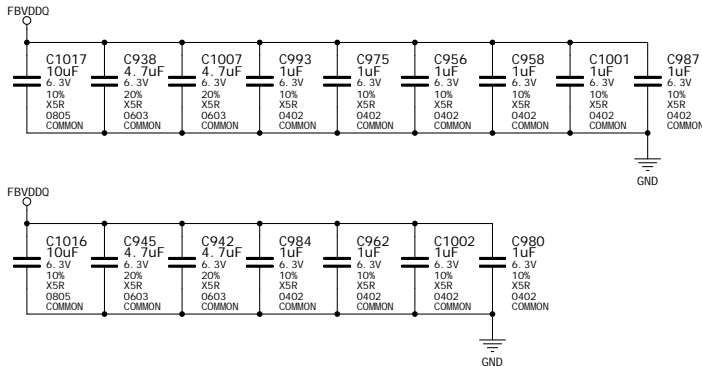




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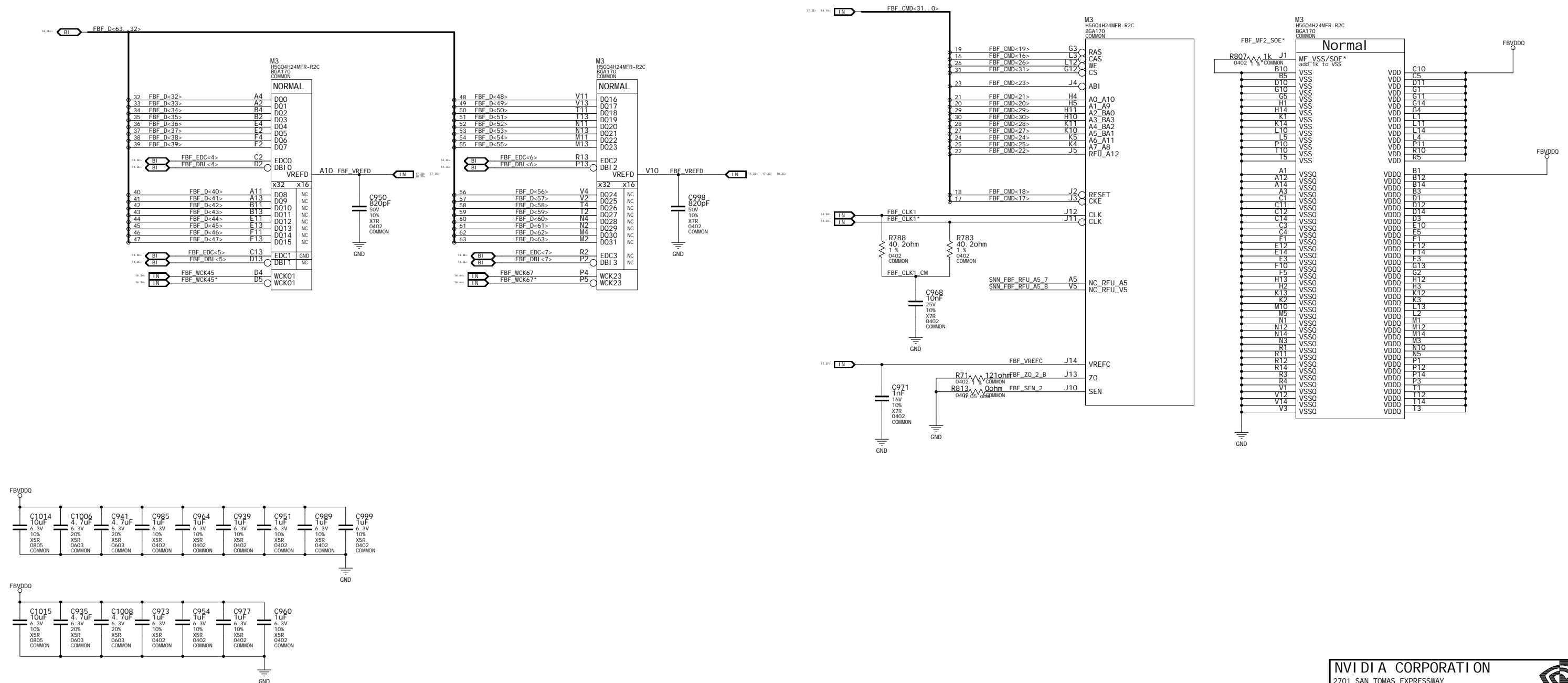
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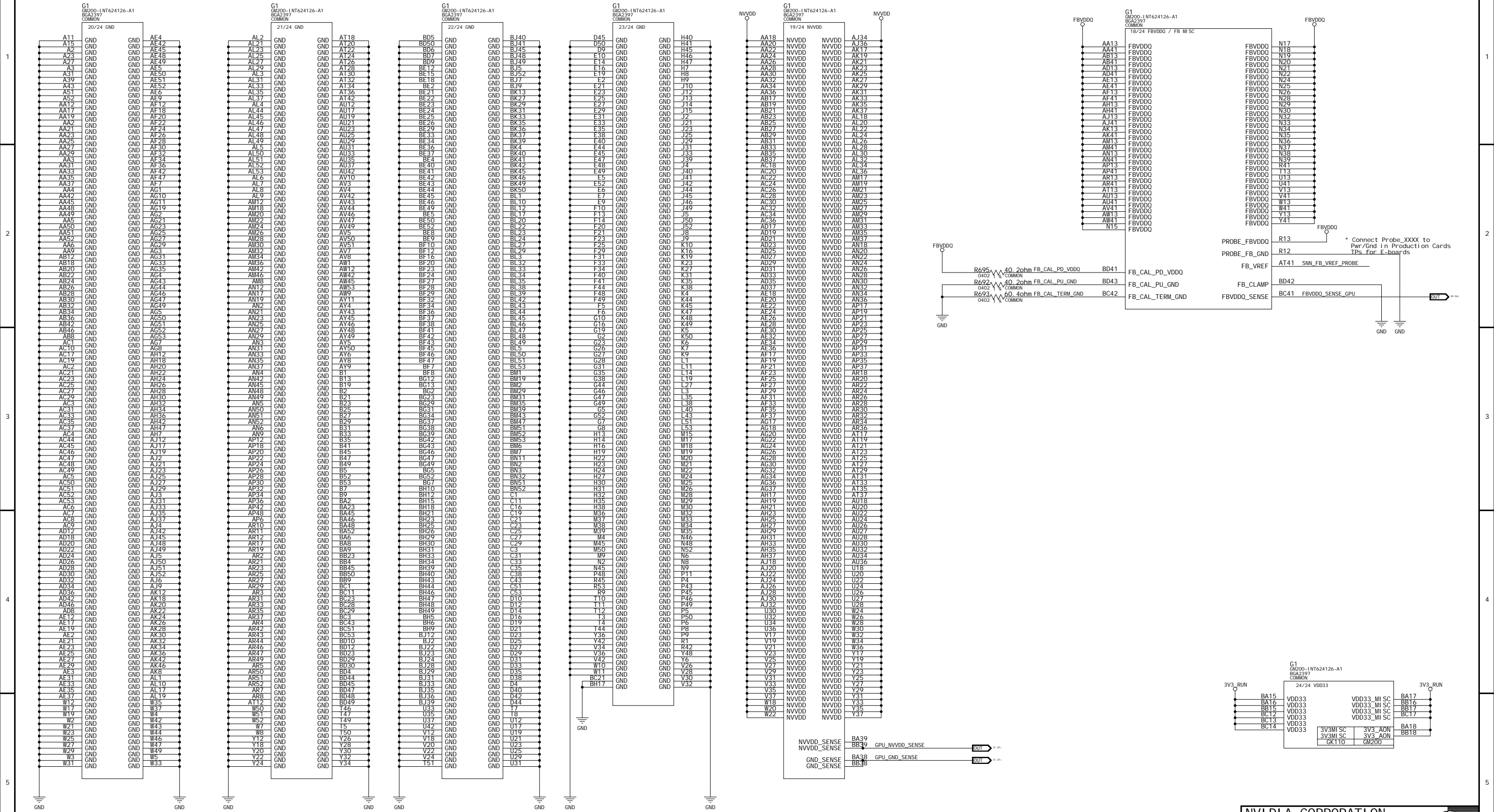


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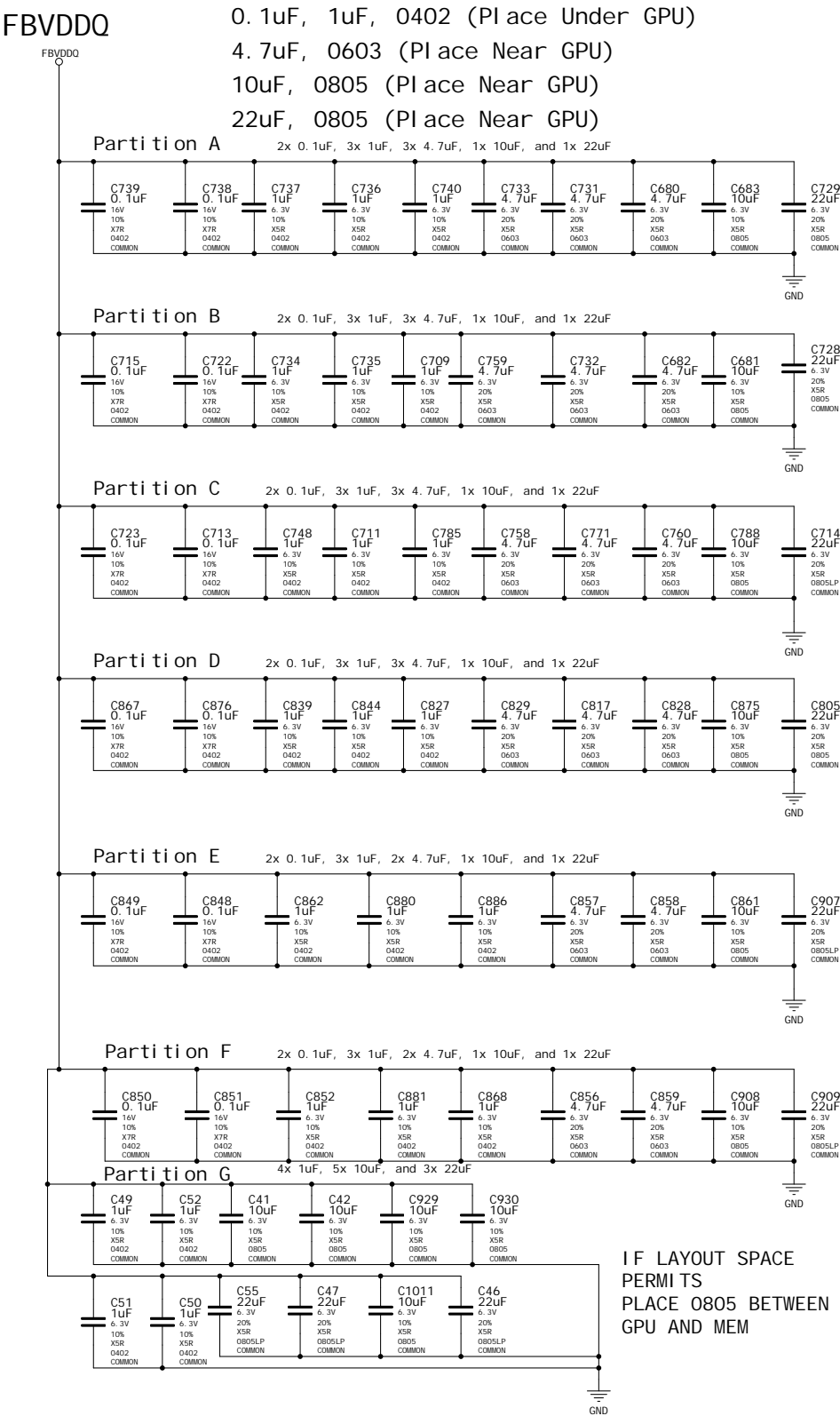
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Page19: GPU PWR and GND

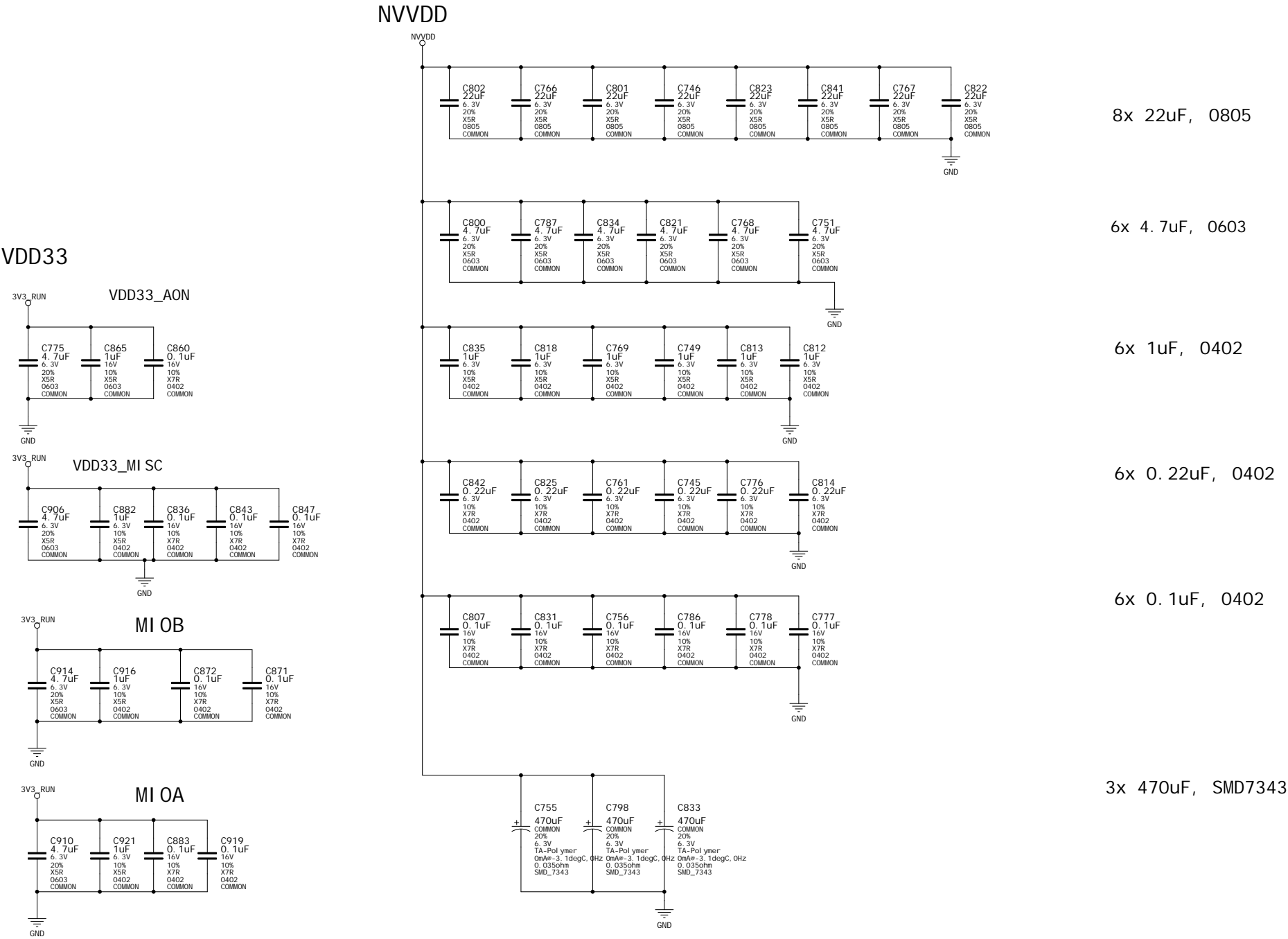


Based on GB3-X GDDR5 FBVDDQ Decap Guideline



NVVDD Decoupling caps. Place under GPU.

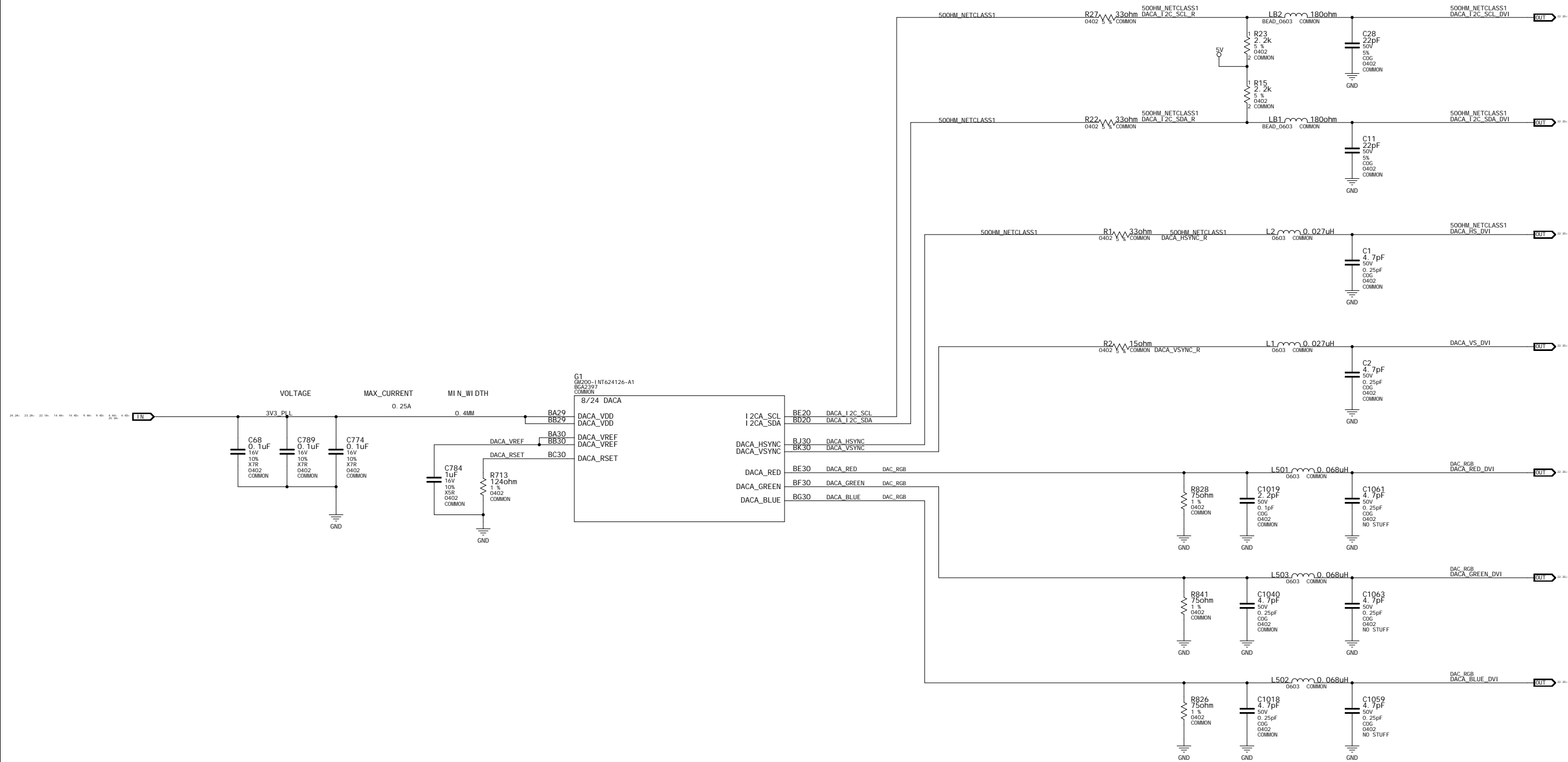
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Page21: DACA Interface



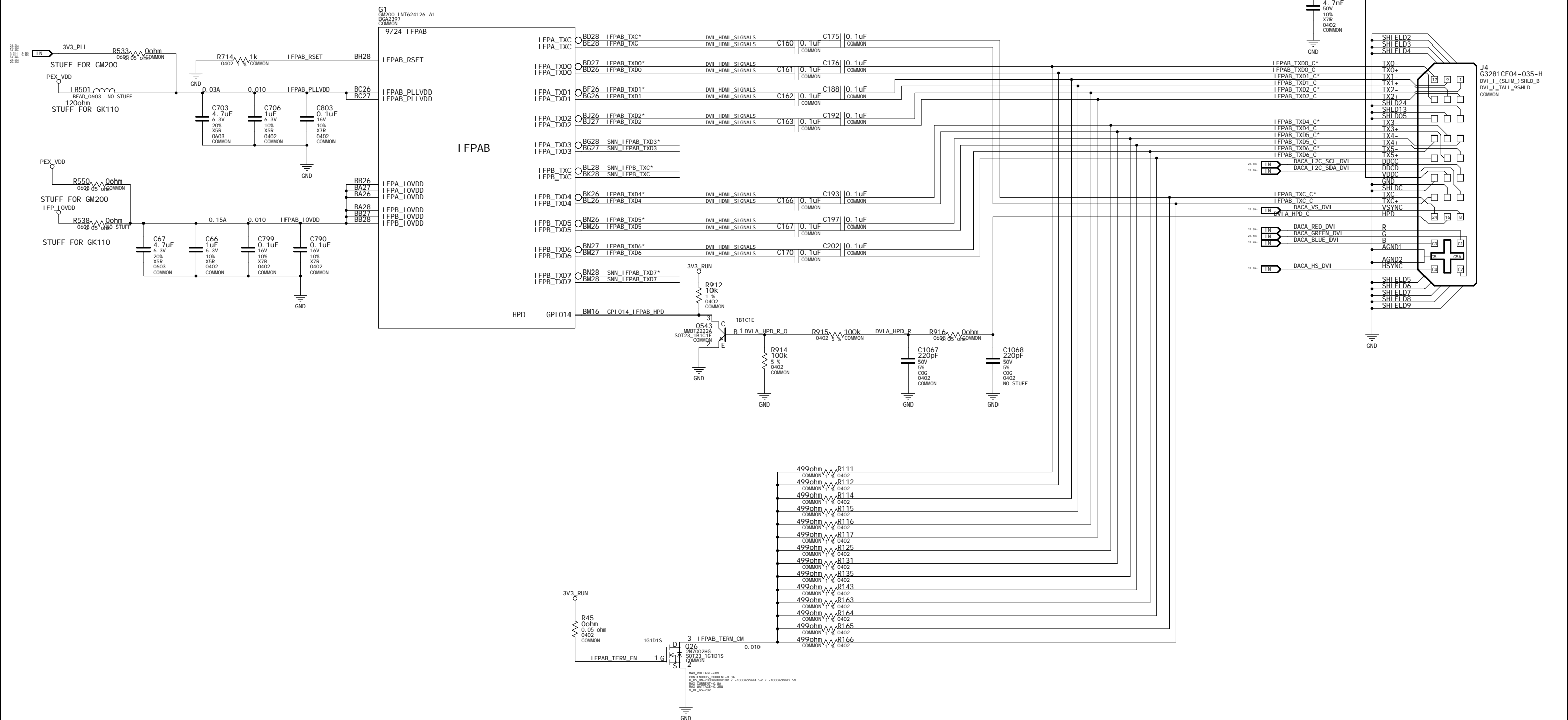
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Page22: I FPAB DVI -I -DL


AC COUPLING NOT NEEDED for KEPLER

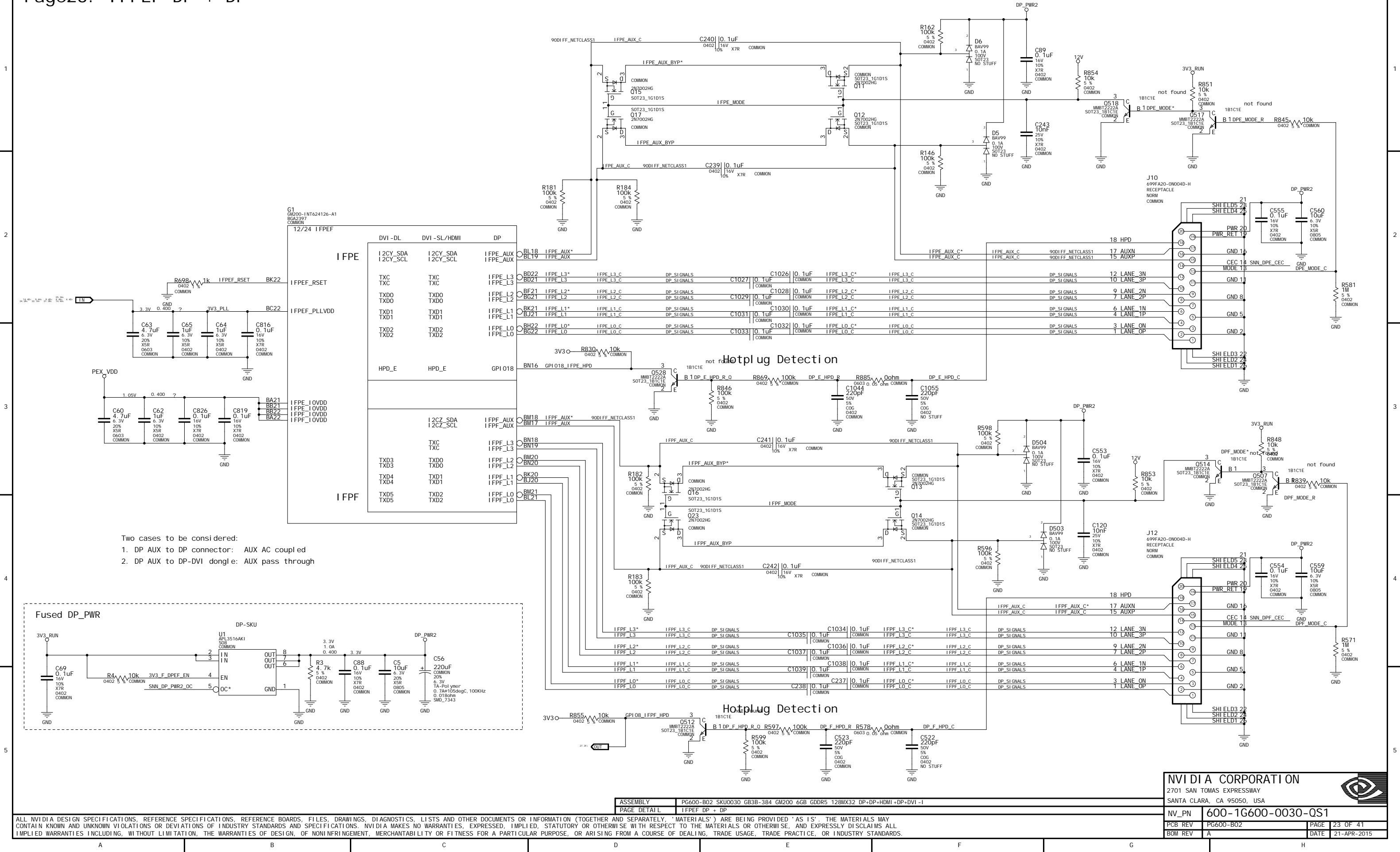
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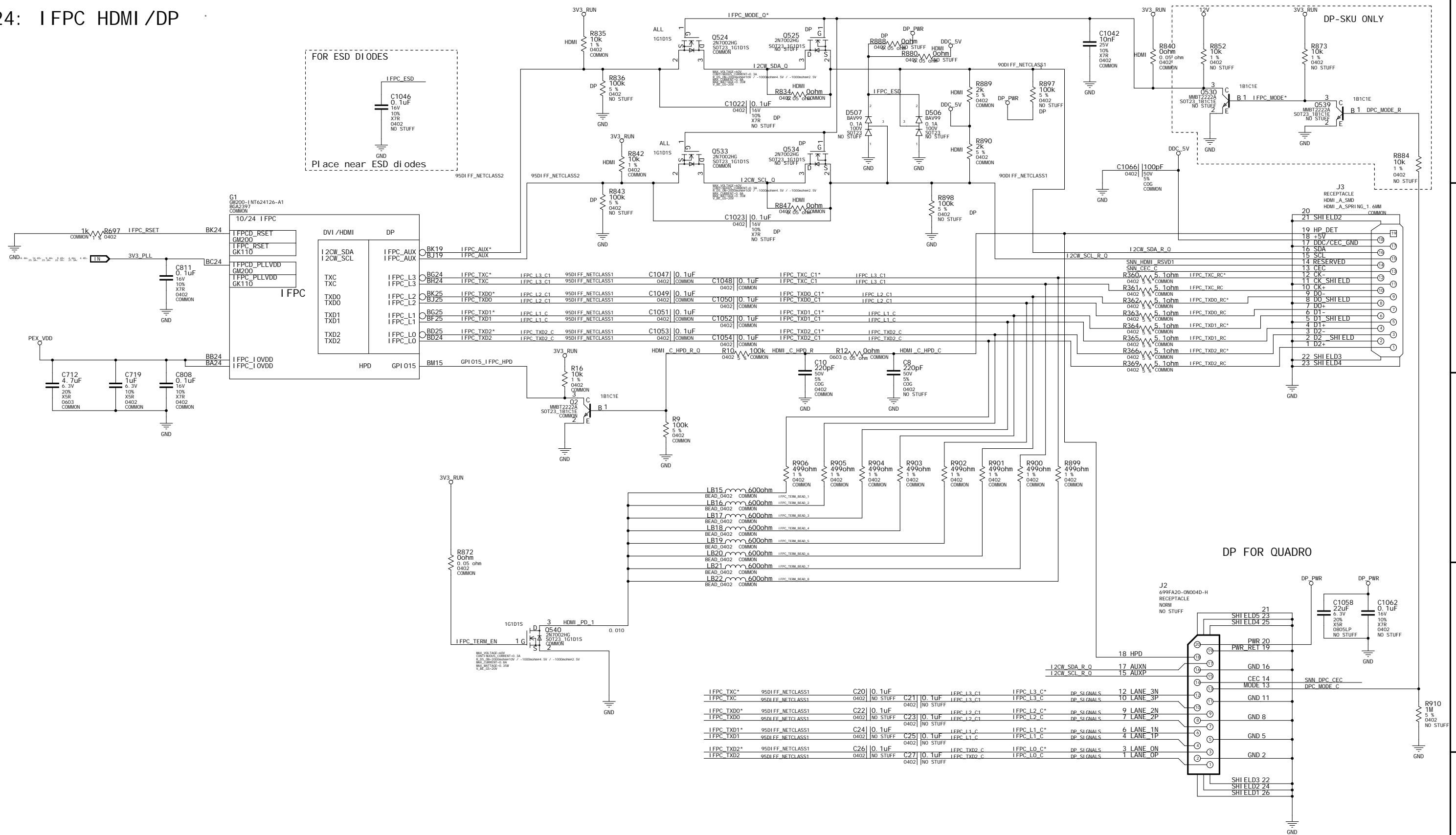


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- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

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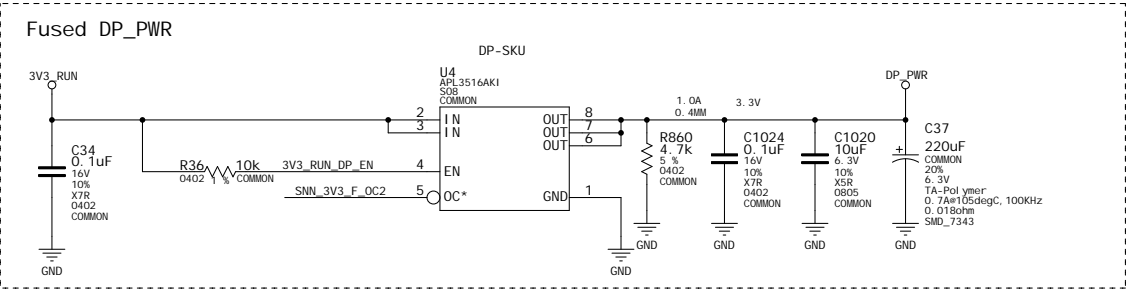
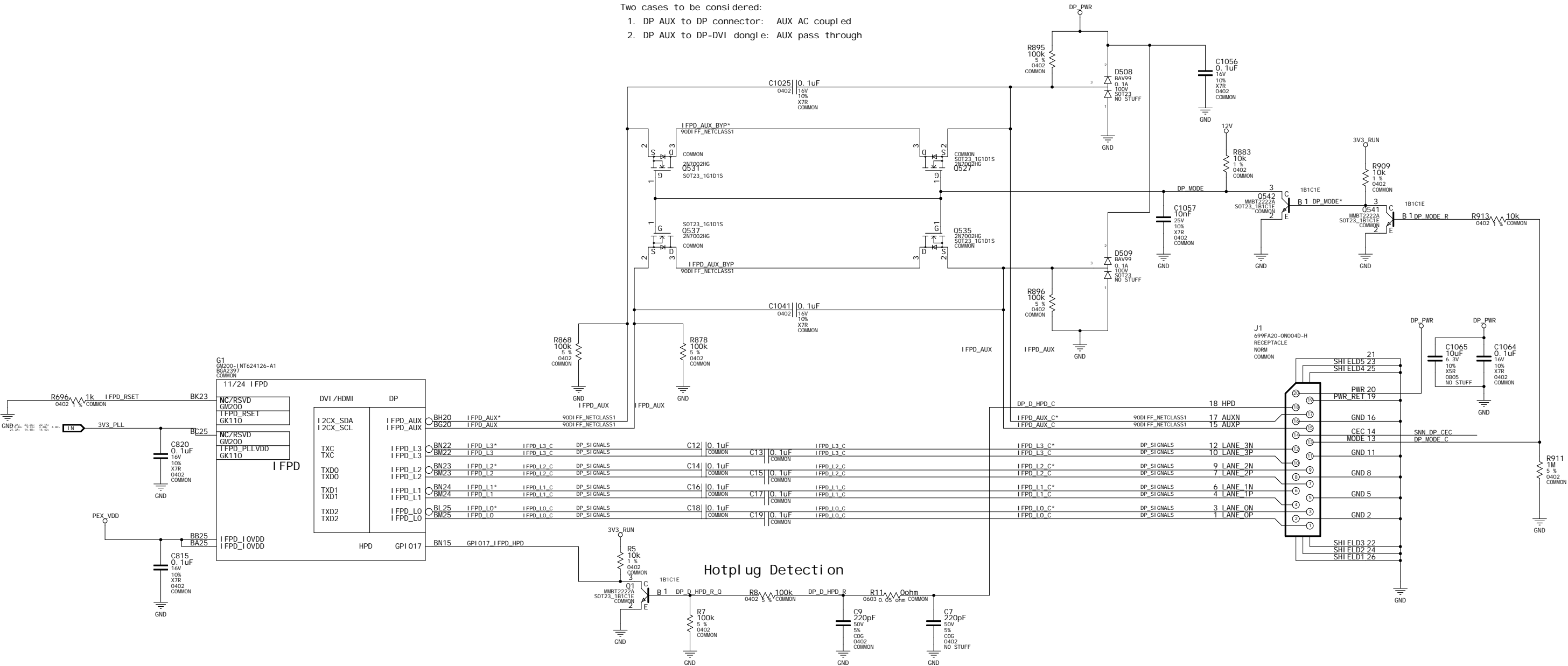
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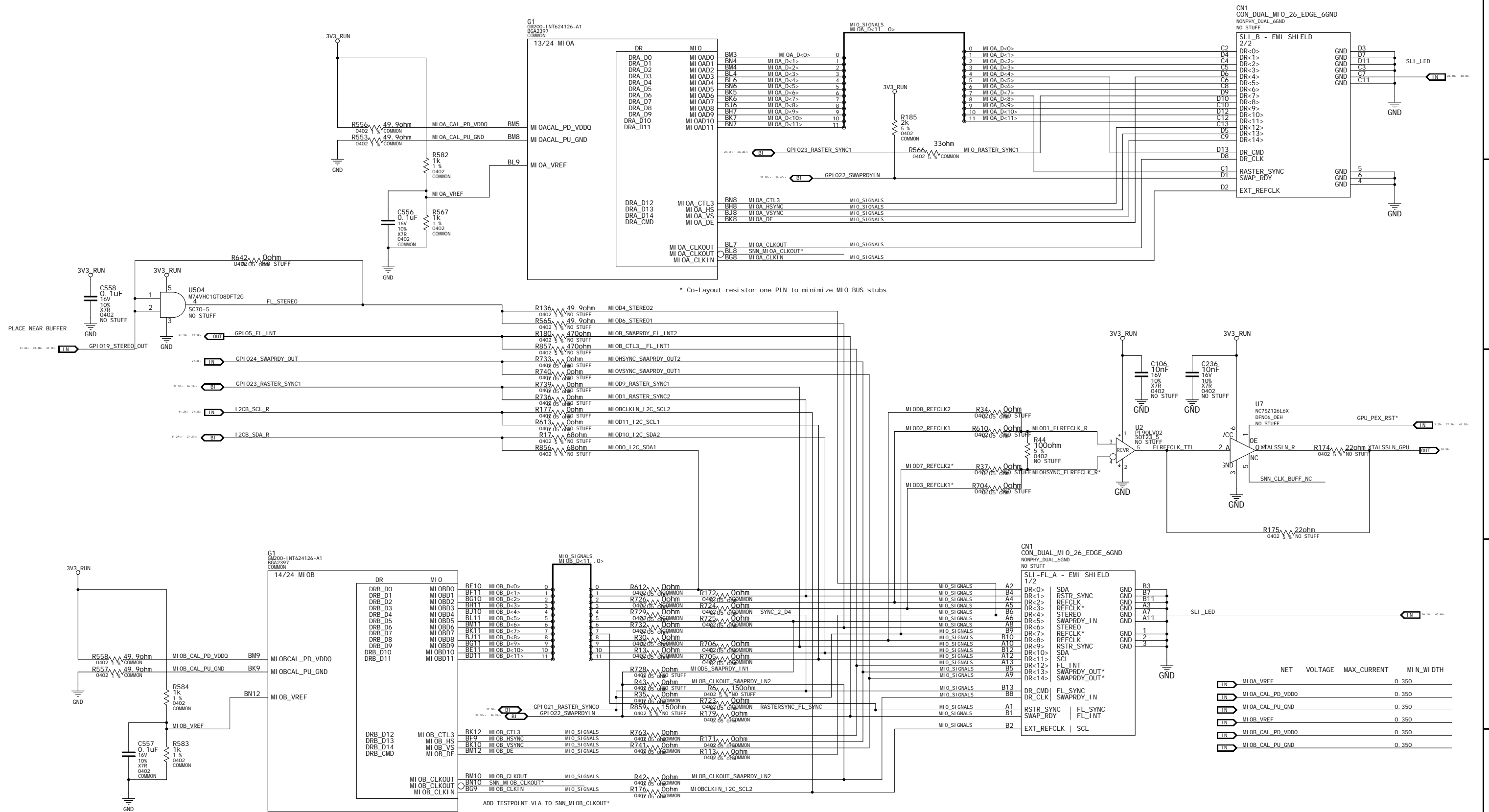
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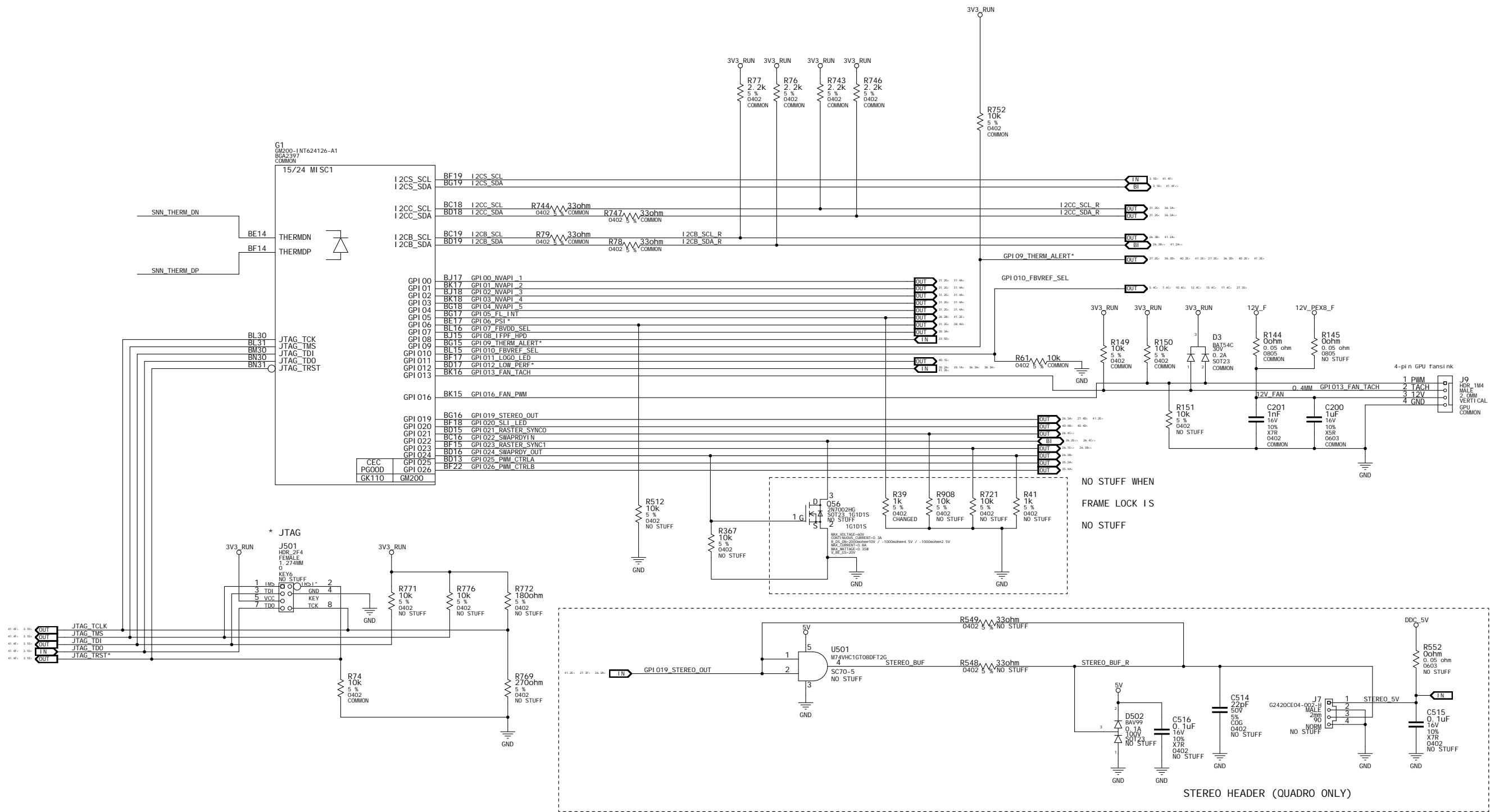
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Page26: MI 0A/B and FRAMELOCK Interface



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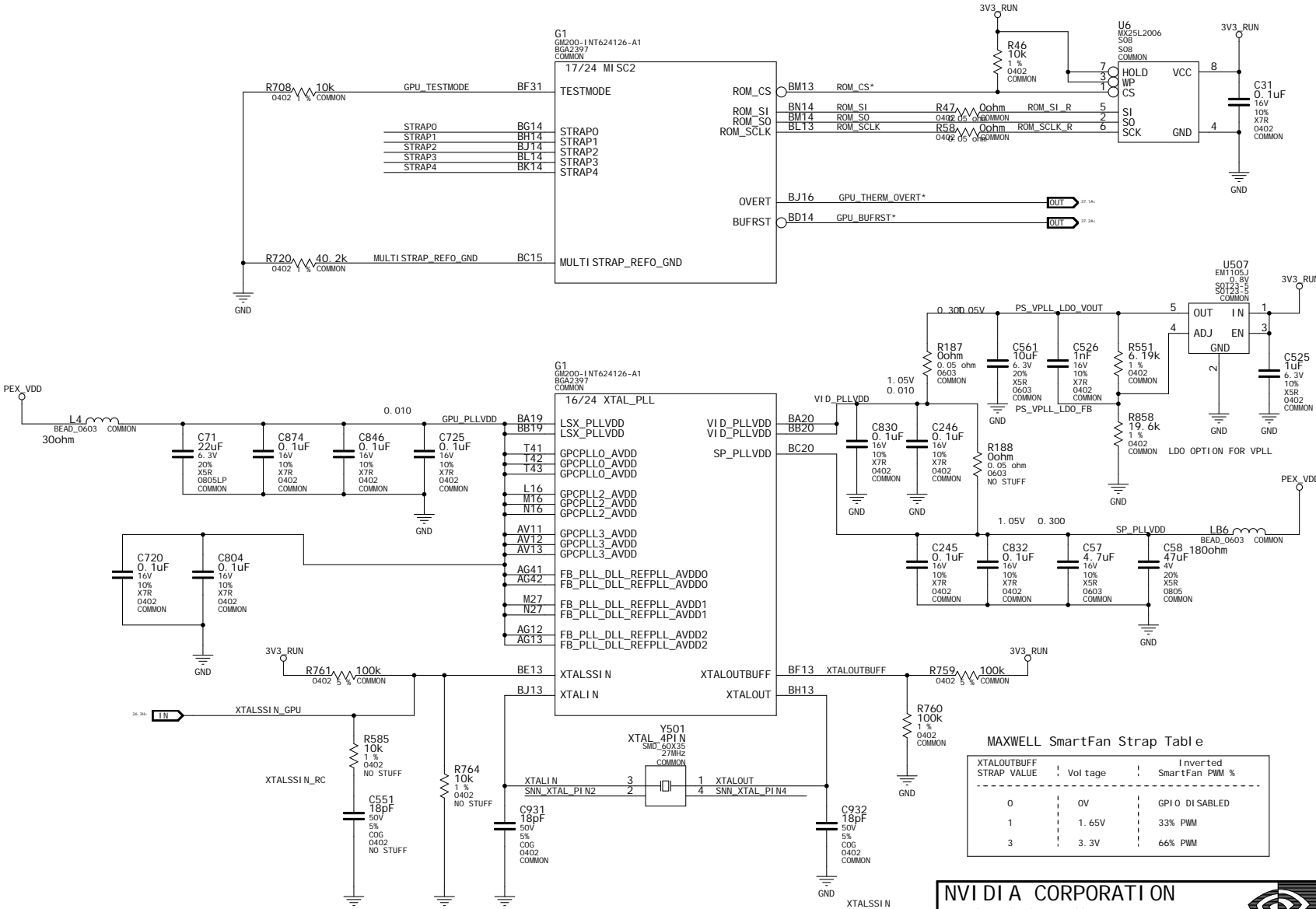
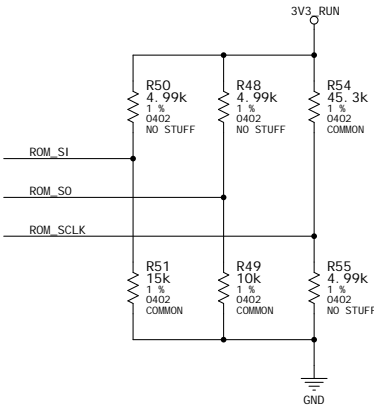
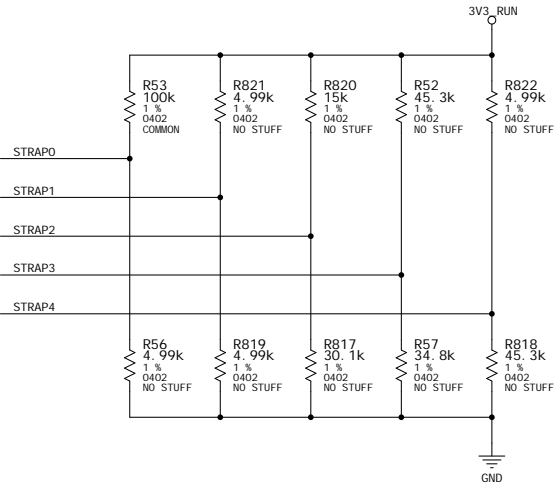


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Page28: MI SC2: ROM, XTAL, Straps

		GK110	GM200
STRAP0	USER_BIT [3:0]*	0000*	GC6_ENABLE(3.3V) PU
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	N/A
STRAP2	PCI_DEVICE [3:0]*	100A*	N/A
STRAP3	SOR_EXPOSED [3:0]*	1111*	N/A
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	N/A
	PEX_MAX_SPEED*	1* FOR GEN2/3*	N/A
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	N/A
	RESERVED	0*	N/A
	RAMCFG[0]*	1*	RAMCFG[0]*
ROM_SI	RAMCFG[1]*	0*	RAMCFG[1]*
	RAMCFG[2]*	1*	RAMCFG[2]*
	RAMCFG[3]*	0*	RAMCFG[3]*
	VGA_DEVICE*	1*	VGA_DEVICE* 1* For Enable
ROM_SO	SMB_ALT_ADDR*	0*	SMB_ALT_ADDR 0* For Disable
	FB[0]_APERTURE_SIZE*	1* For 128MB*	PCI_E_CFG 0* For Desktop
	FB[1]_APERTURE_SIZE*	0* For 128MB*	DEVICE_SEL 0* For DEVICE A
	PEX_PLL_EN_TERM100*	0* DISABLED*	SOR0_EXPOSED
	PCI_DEVICE_EXT[5]*	0*	SOR1_EXPOSED
ROM_SCLK	SUB_VENDOR*	1* Dedicated BIOS*	SOR2_EXPOSED
	PCI_DEVICE_EXT[4]*	0*	SOR3_EXPOSED

	MULTI_STRAP_REFO_GND
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND



MAXWELL SmartFan Strap Table		
XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	1.65V	33% PWM
3	3.3V	66% PWM

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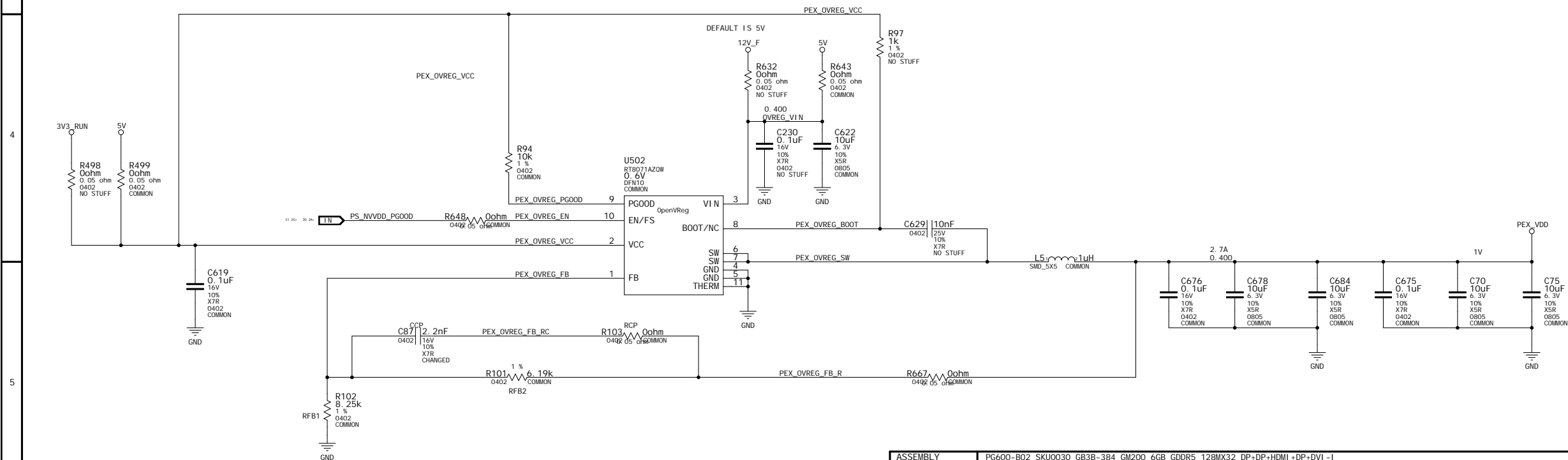
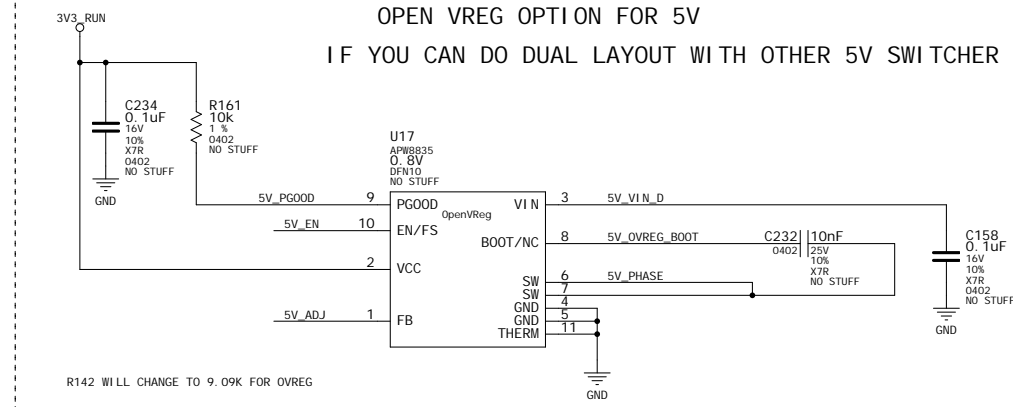
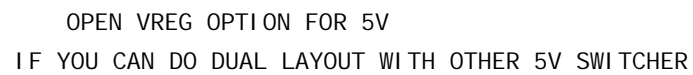
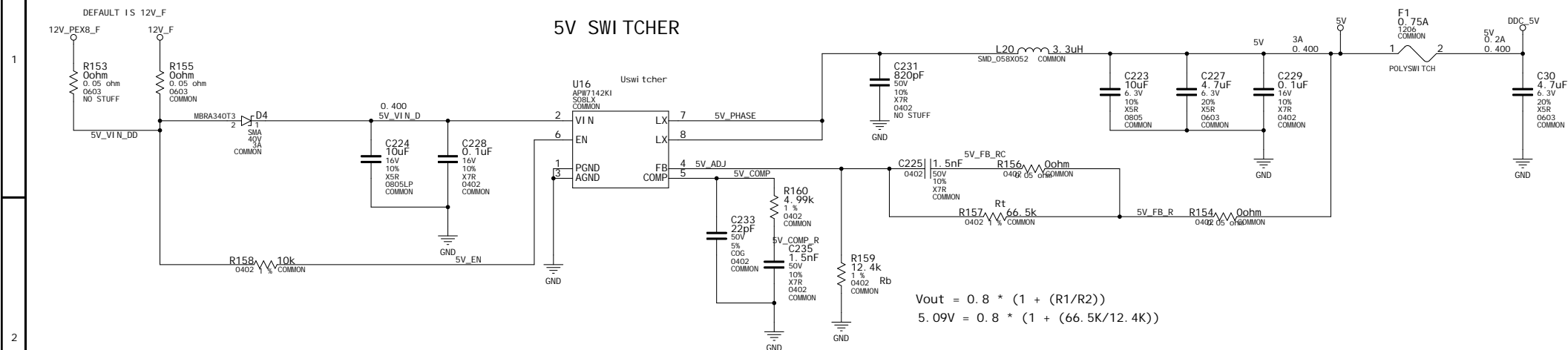
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BOM REV	A	DATE	21-APR-2015

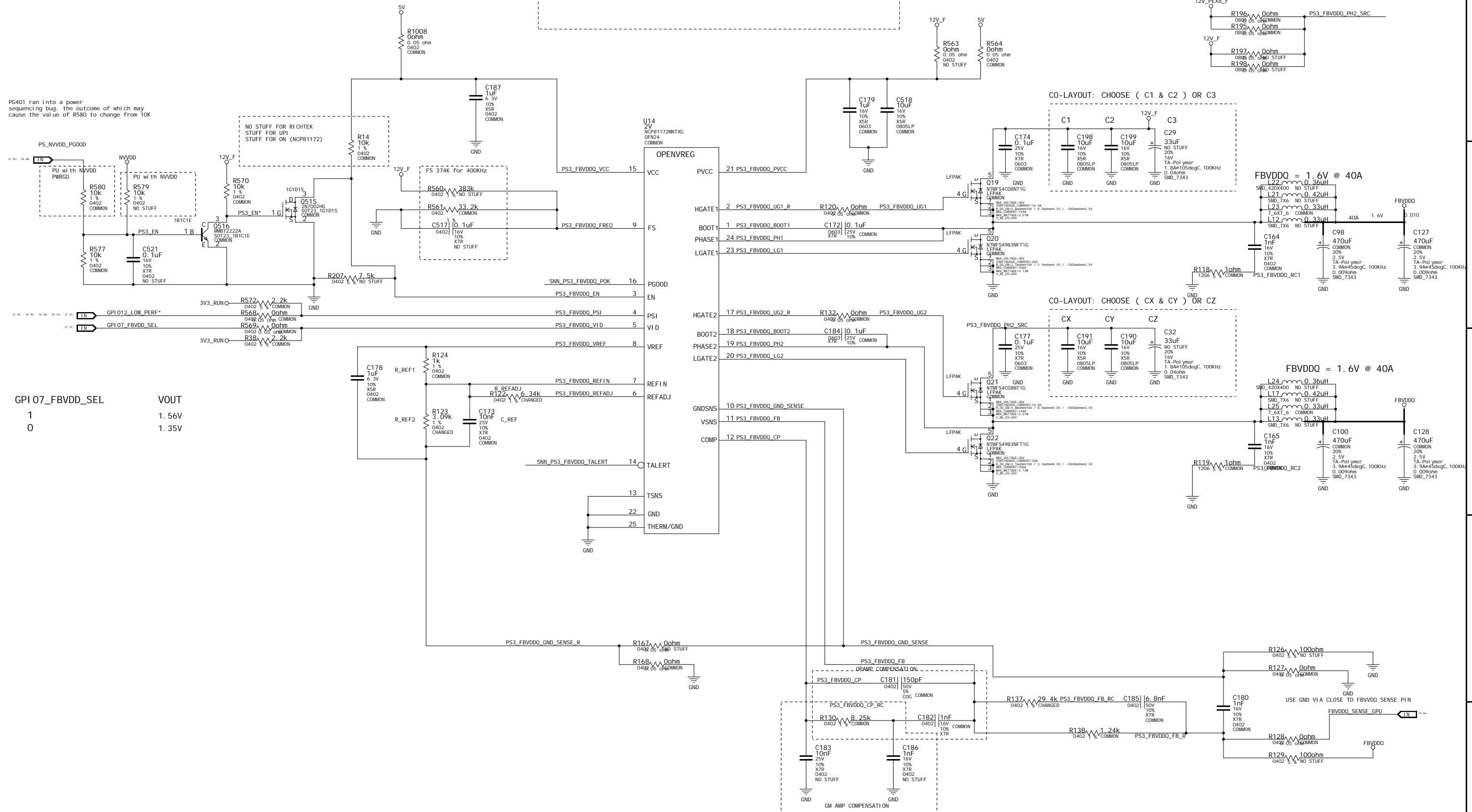
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Page30: PS: FBVDDQ



ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI +DP+DVI -
PAGE DETAIL	PS: FBVDD/Q

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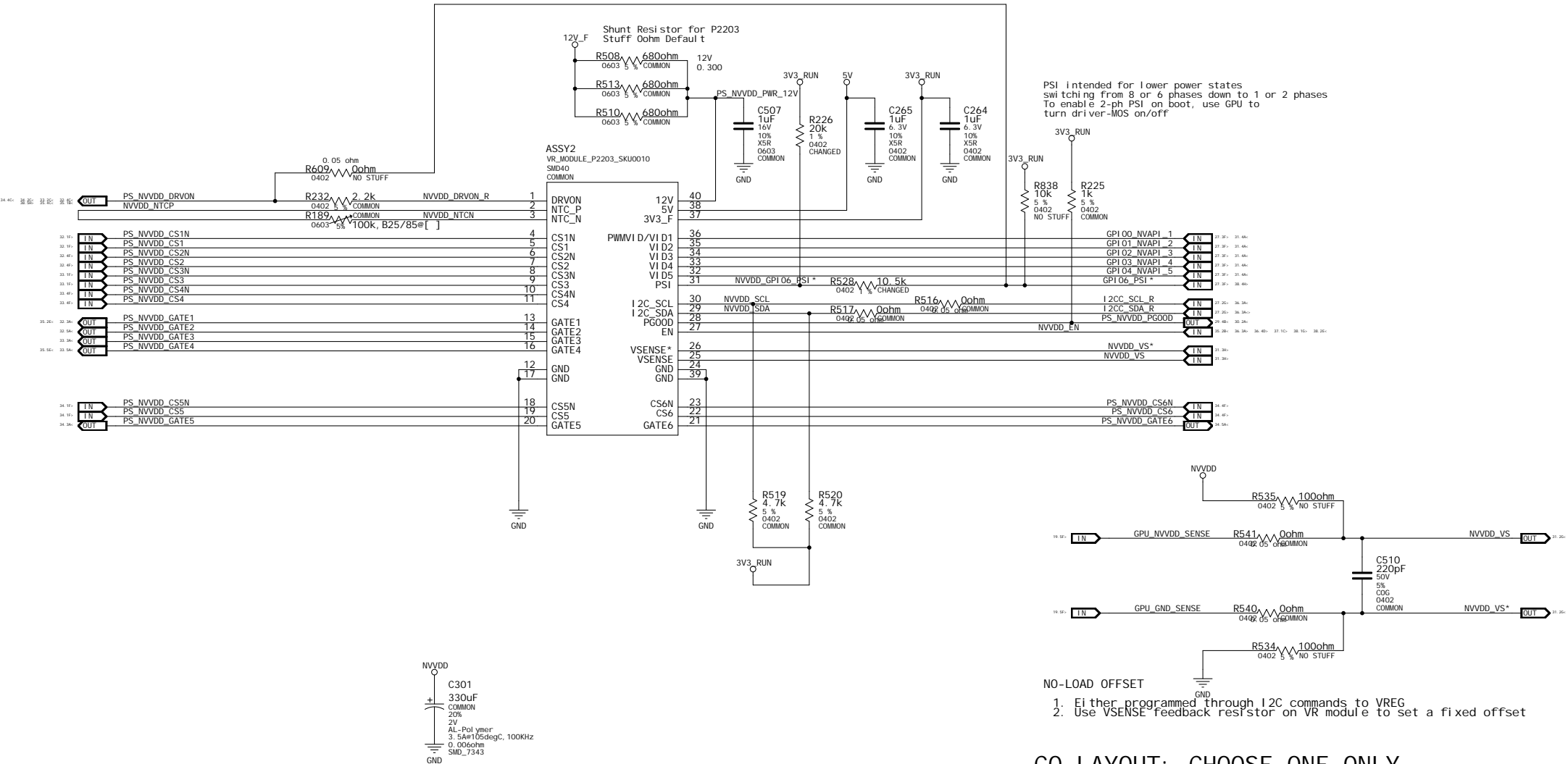


NV_PN	600-1G600-0030-QS1
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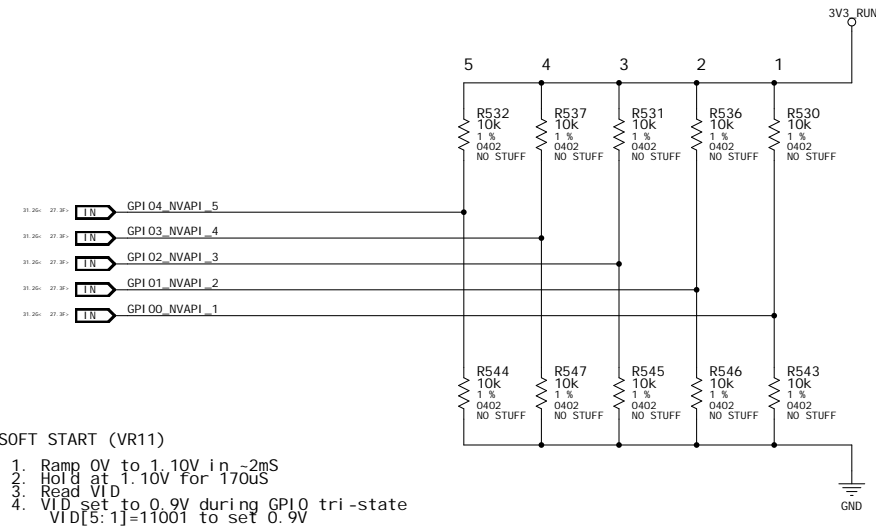
PCB REV	PG600-B02	PAGE	30 OF 41
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VID Table

GPI04	GPI03	GPI02	GPI01	GPI00	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V



CO-LAYOUT: CHOOSE ONE ONLY



- SOFT START (VR11)
1. Ramp 0V to 1.10V in ~2ms
 2. Hold at 1.10V for 170µs
 3. Read VID
 4. VID set to 0.9V during GPIO tri-state
- VID[5:1]=11001 to set 0.9V

- P-STATE VOLTAGES
1. P0 at 1.05V to 1.15V (depending on VB)
 2. P8/P12 at 0.80V

ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI+DP+DVI-I
PAGE DETAIL	PS: NVVDD Controller

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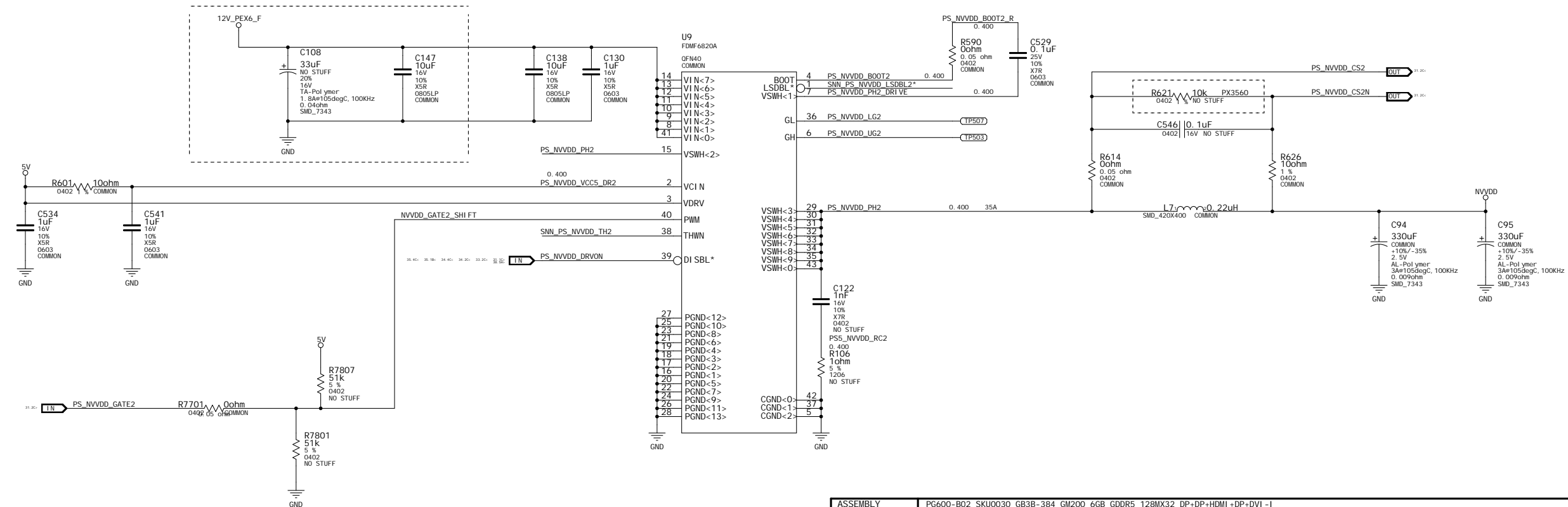
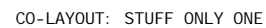
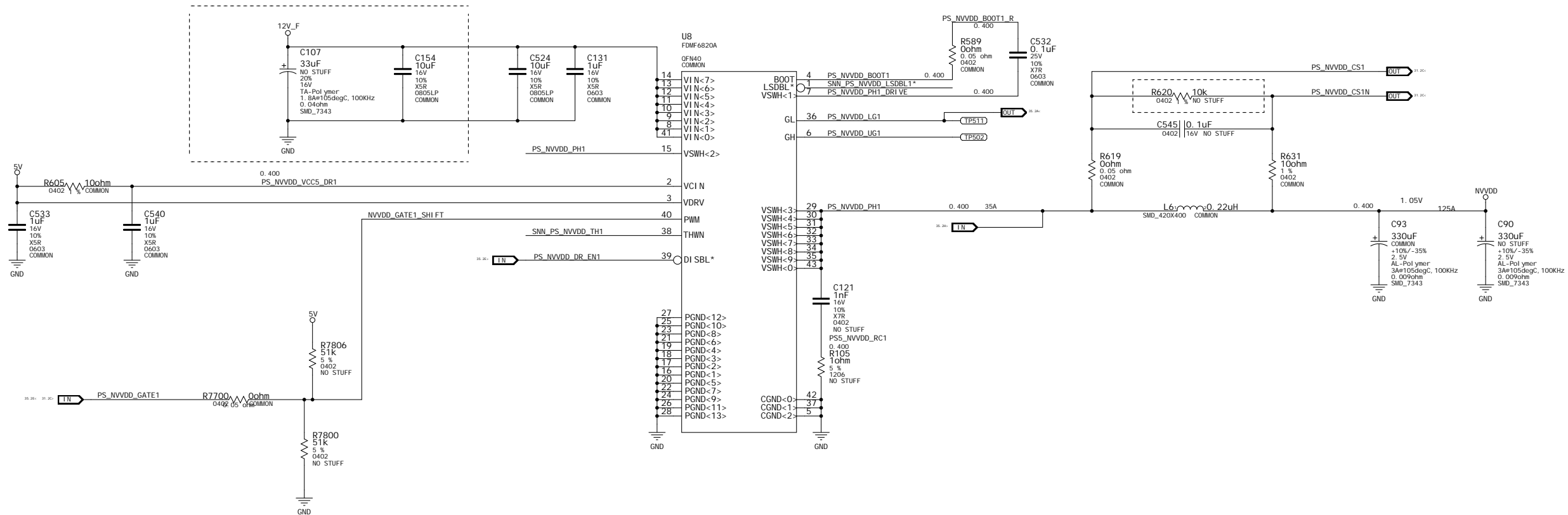
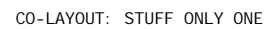
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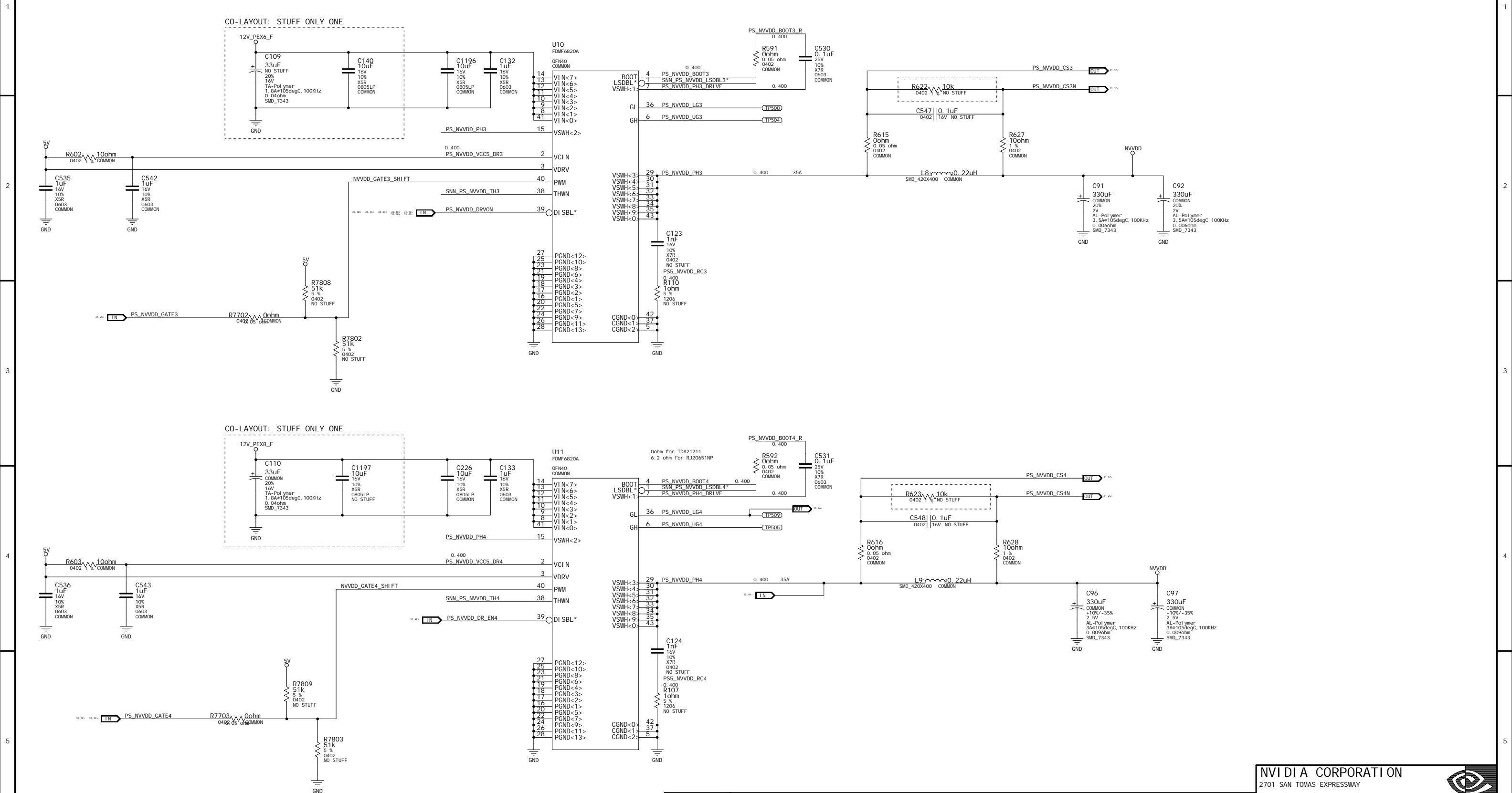
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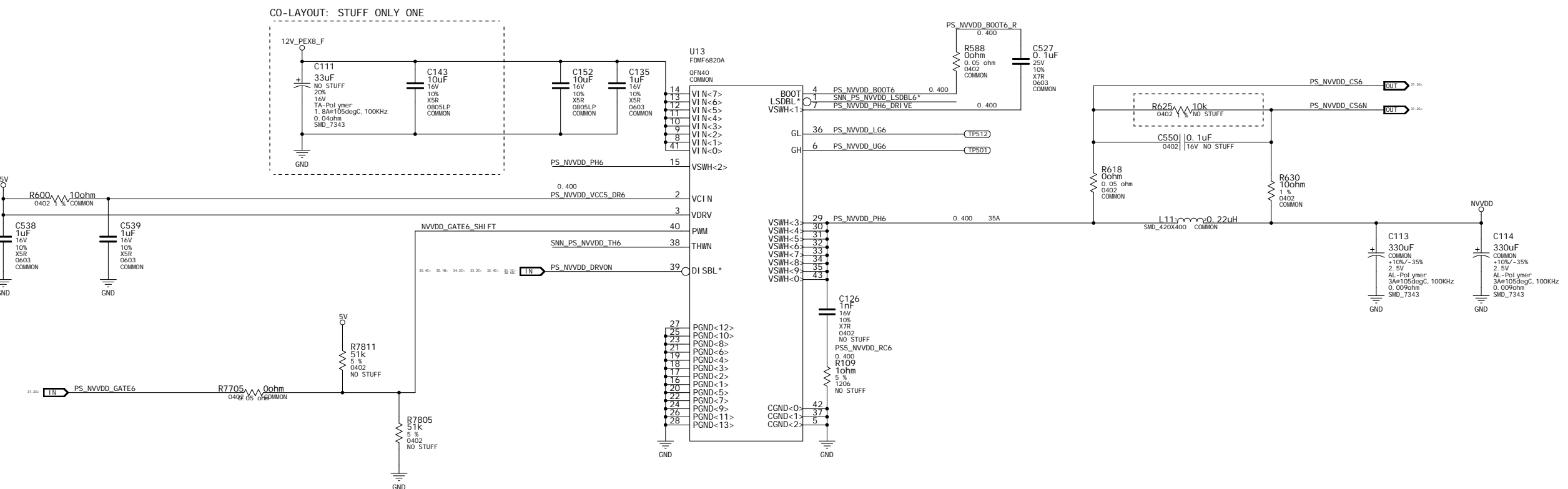
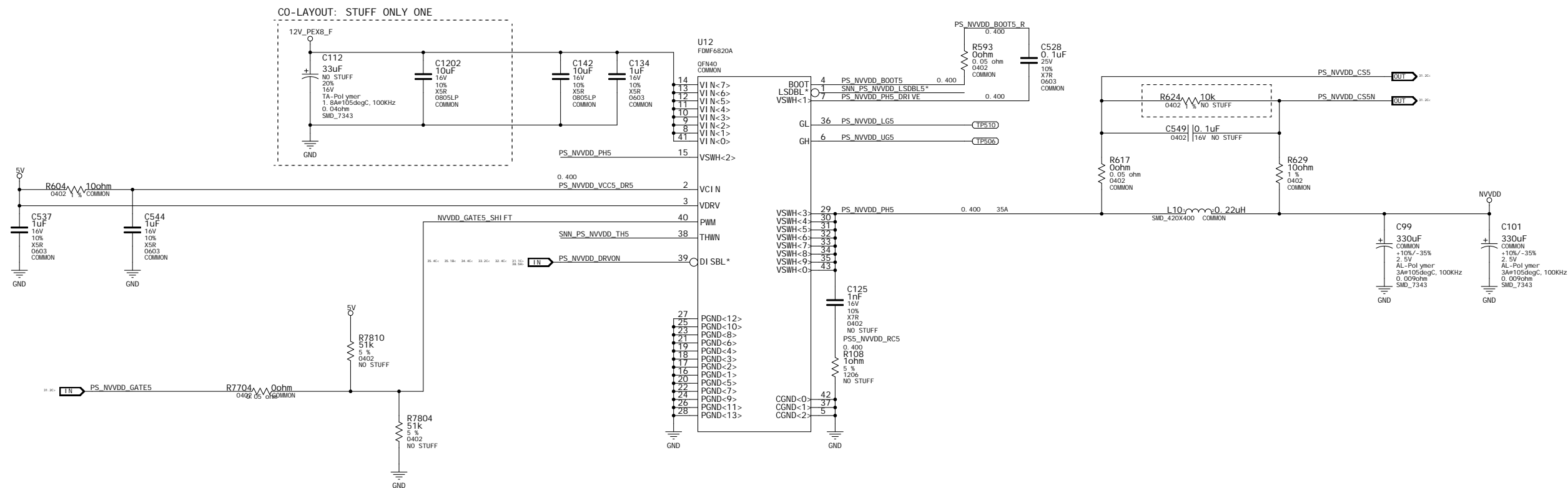


ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI +DP+DVI -I
PAGE DETAIL	PS: NVDD Phase 1, 2

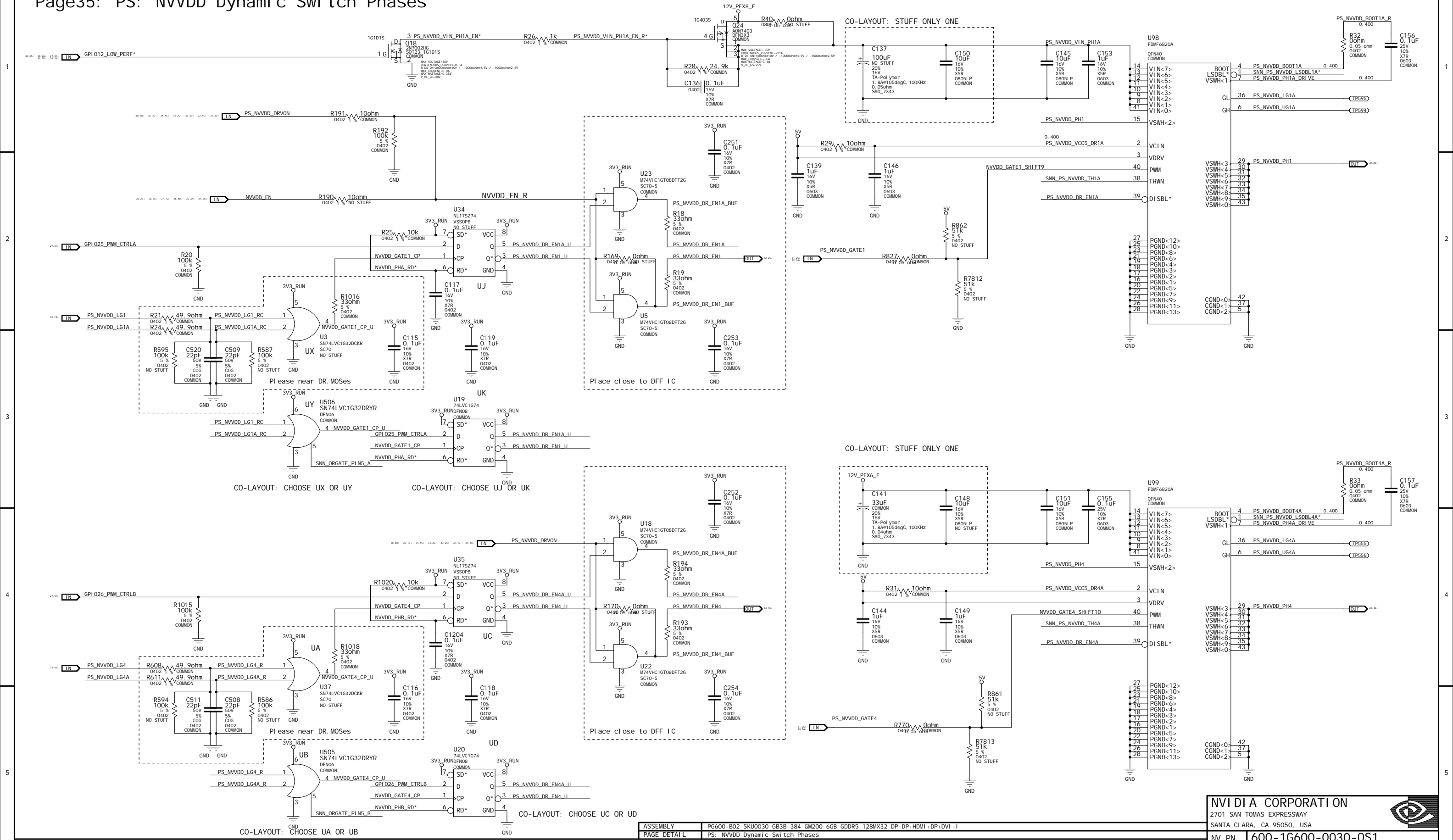
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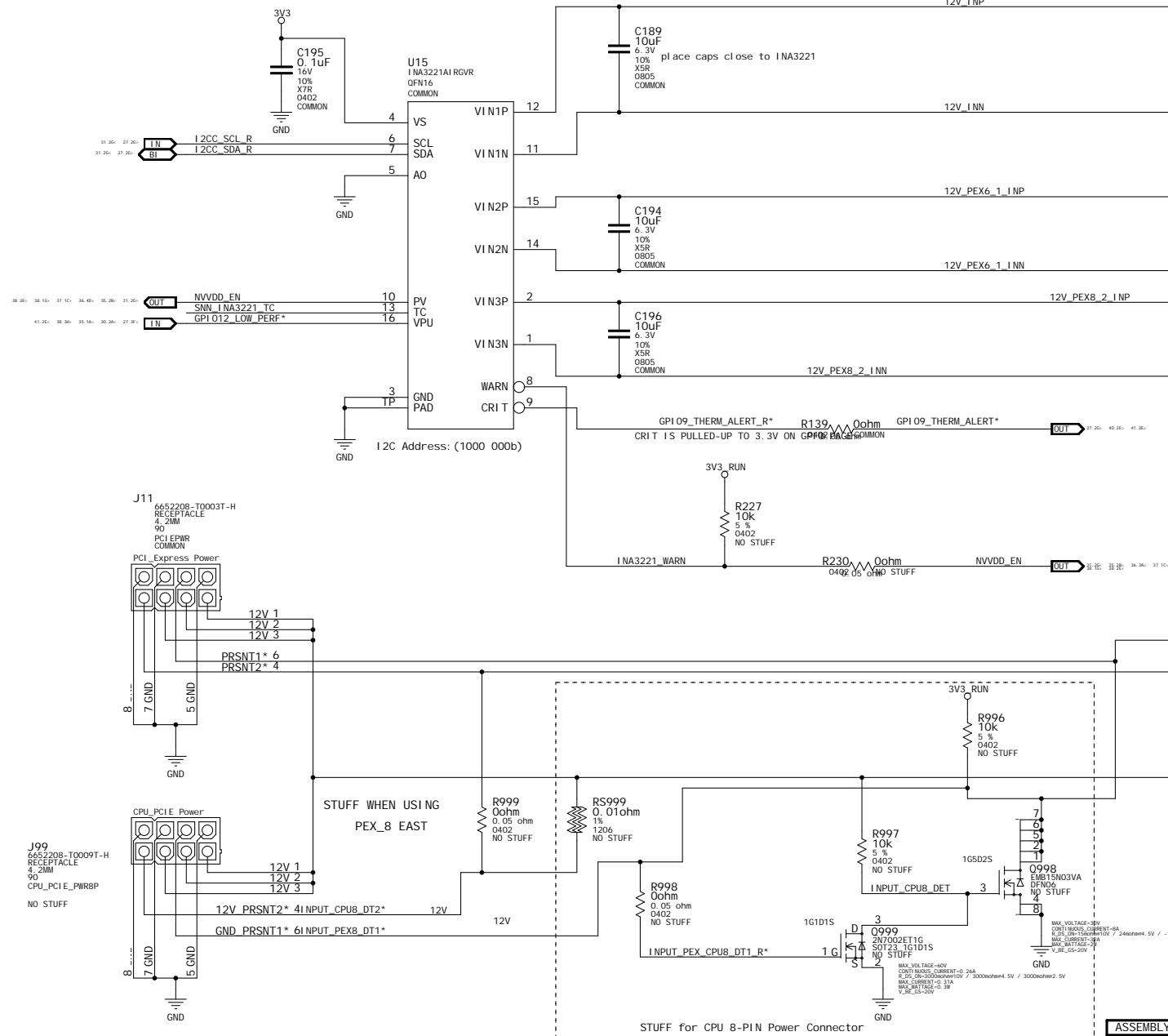
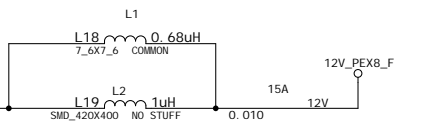
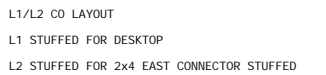
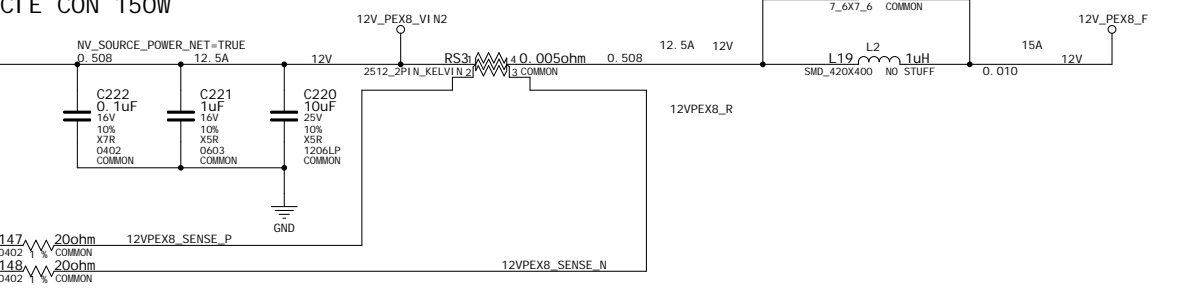
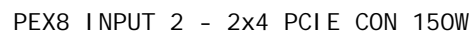
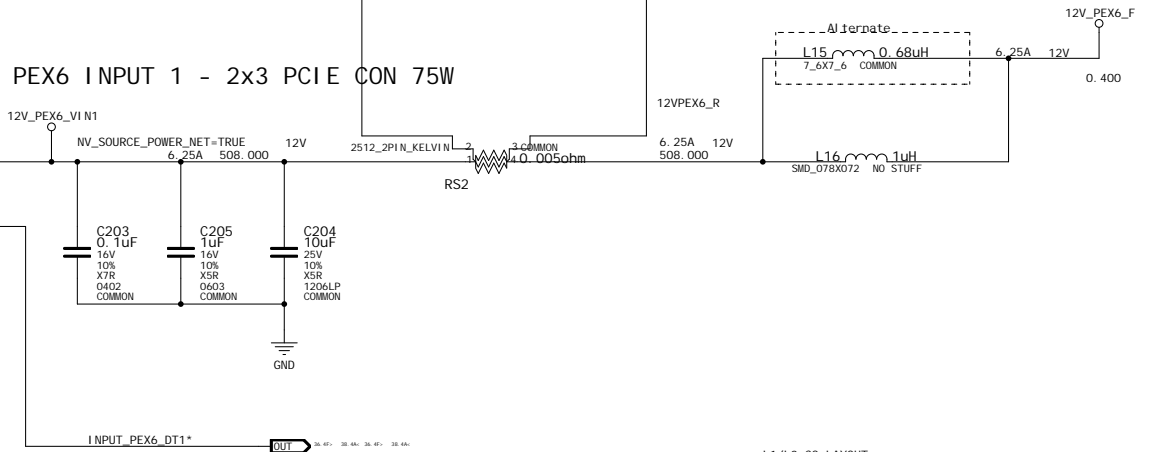
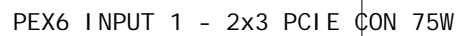
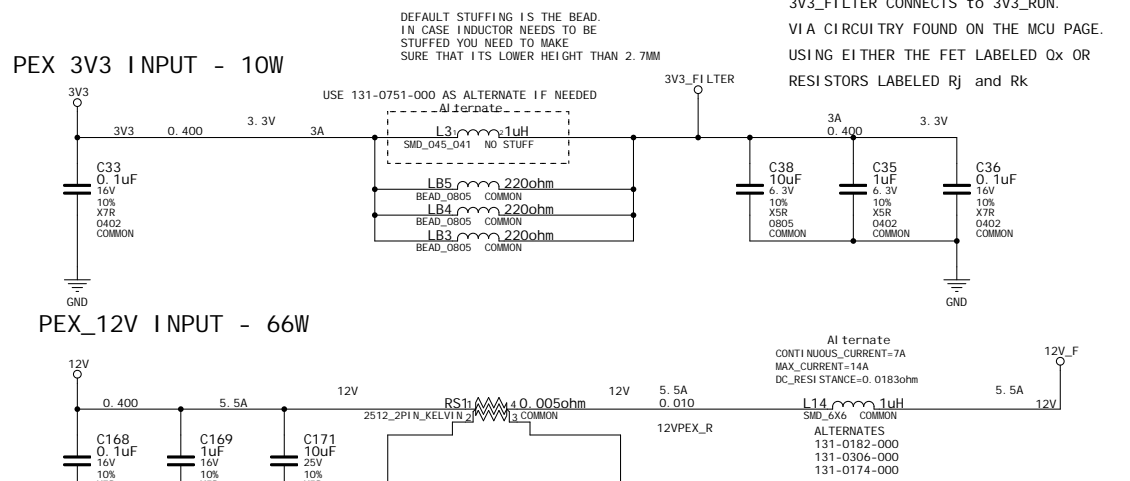
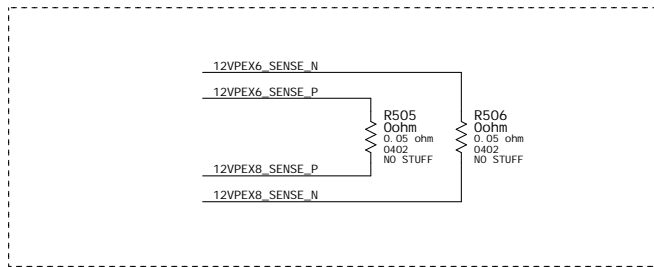


Page35: PS: NVVDD Dynamic Switch Phases



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ASSEMBLY	
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

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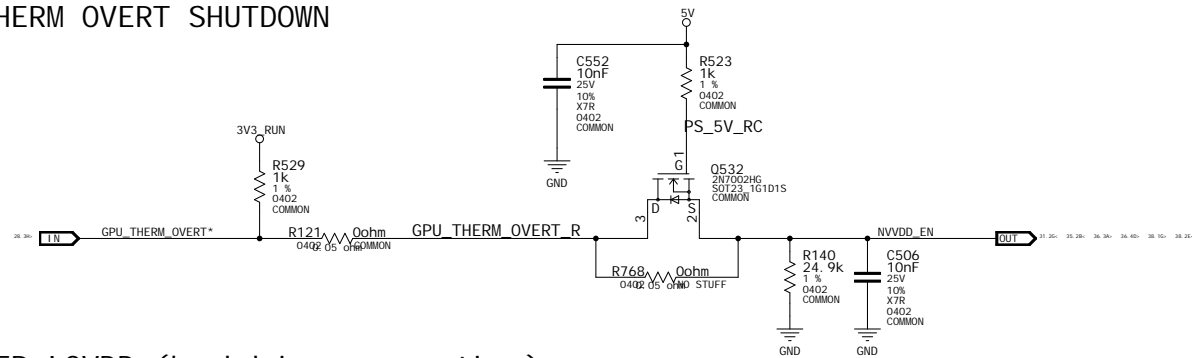


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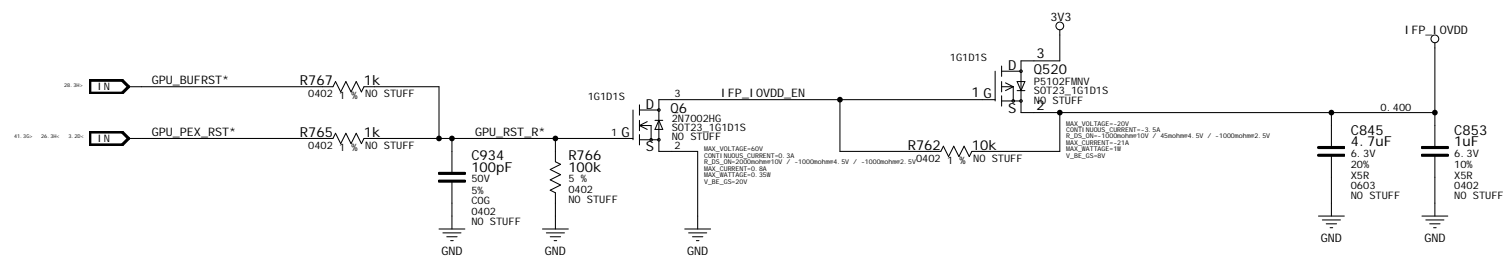
PCB REV	PG600-B02	PAGE	36 OF 41
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THERM OVERT SHUTDOWN



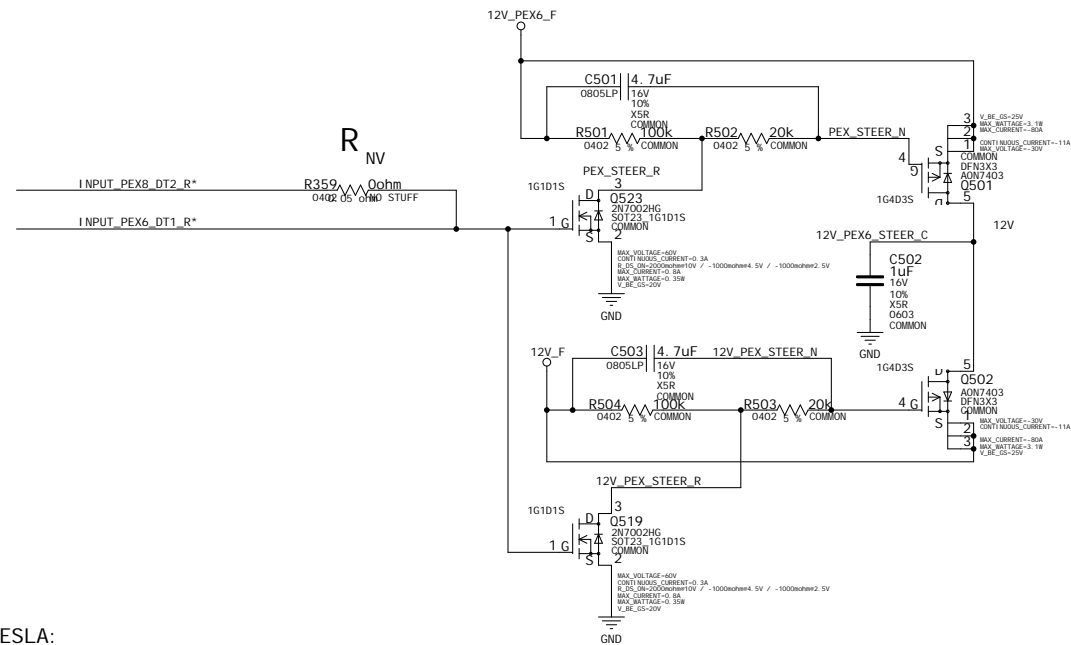
IFP_IOVDD (backdrive prevention)



Page38: PS: 12V Current Steering & Hot Unplug Detect

12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



QUADRO/TESLA:

PEX 6 INPUT CONNECTOR IS NOT LOADED

PEX 6 INPUT DETECT MUST BE DI SABLED

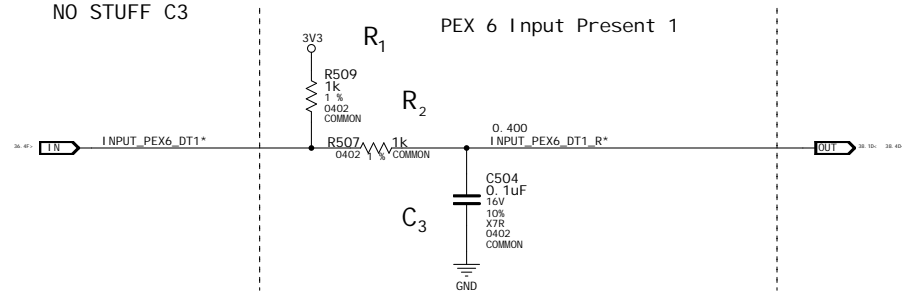
PEX 8 INPUT DETECT MUST BE USED TO CONTROL STEERING

STUFF Rnv IN STEERING CIRCUIT

NO STUFF R1

```
NO STUFF R2
```

NO STUFF C3



GeFORCE:

PEX 6 INPUT CONNECTOR IS LOADED

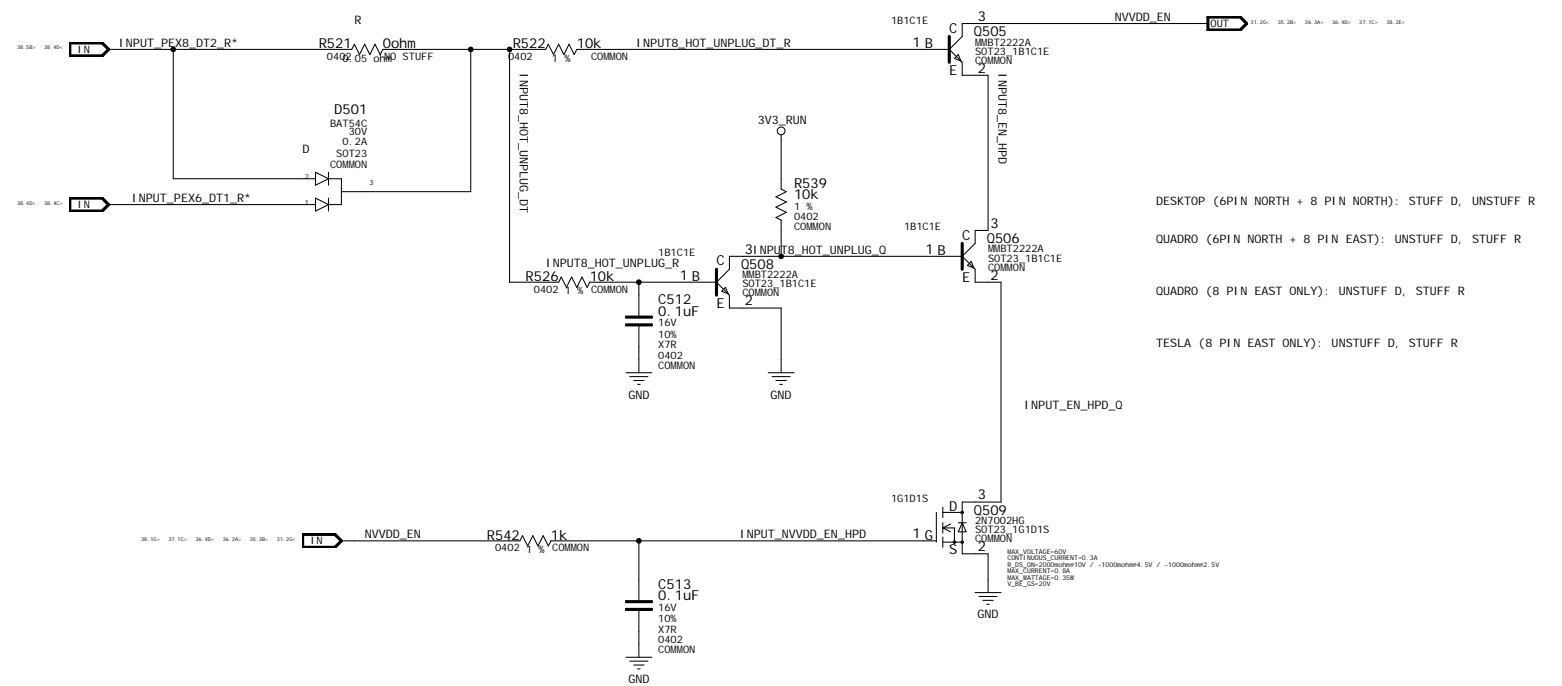
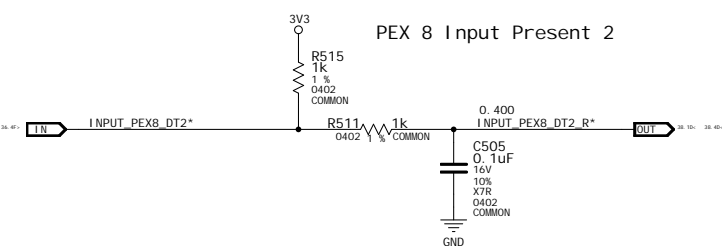
PEX 6 INPUT DETECT MUST BE USED TO CONTROL STEERING

NO STUFF Rnv IN STEERING CIRCUIT

STUFF R1

STUFF R2

STUFF C3



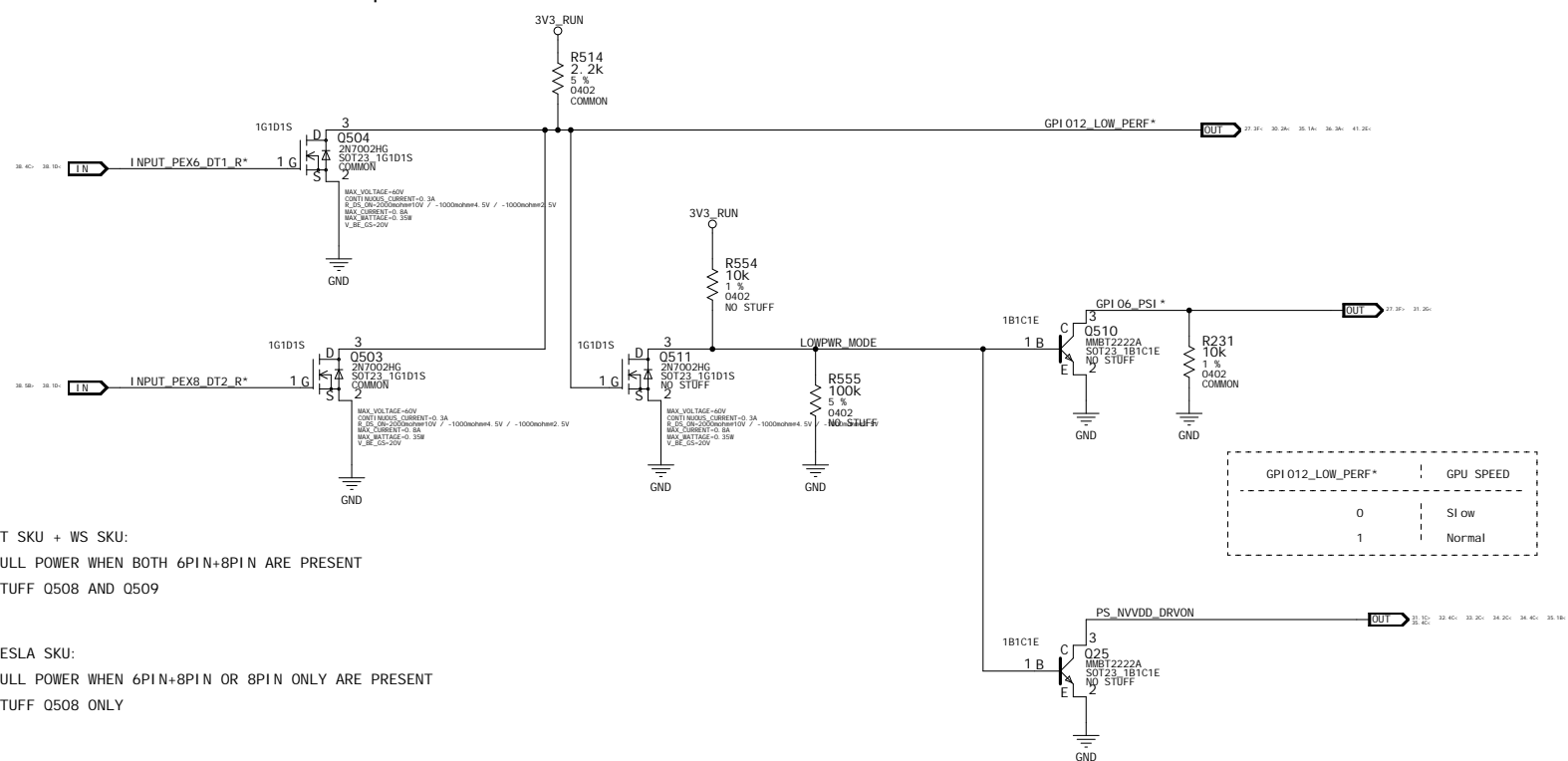
DESKTOP (6PIN NORTH + 8 PIN NORTH): STUFF D, UNSTUFF R

QUADRO (6PIN NORTH + 8 PIN EAST): UNSTUFF D, STUFF R

QUADRO (8 PIN EAST ONLY): UNSTUFF D, STUFF R

TESLA (8 PIN EAST ONLY): UNSTUFF D, STUFF R

PEX Input - Under Power Boot Controls



DT SKU + WS SKU:

FULL POWER WHEN BOTH 6PIN+8PIN ARE PRESENT

STUFF Q508 AND Q509


TESLA SKU:

FULL POWER WHEN 6PIN+8PIN OR 8PIN ONLY ARE PRESENT

STUFF Q508 ONLY

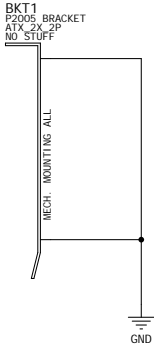
ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI+DP+DVI-I
PAGE DETAIL	PS: 12V Current Steering & Hot Unplug Detect

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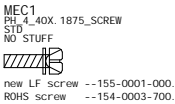
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BCM REV A	DATE 21-APR-2015		

Brackets:

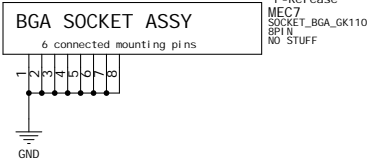
DVI DVI _HDMI _DP : 151-10001-0441-092



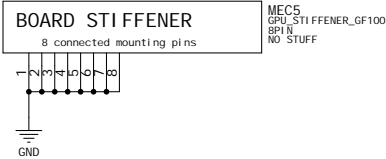
Bracket Screw



GPU SOCKET



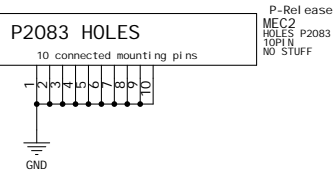
GPU Sti ffener (BRI NG-UP COOLER)



Sti ffener



Mechani cal Hol es Symbol



Bri ng Up Cooler

