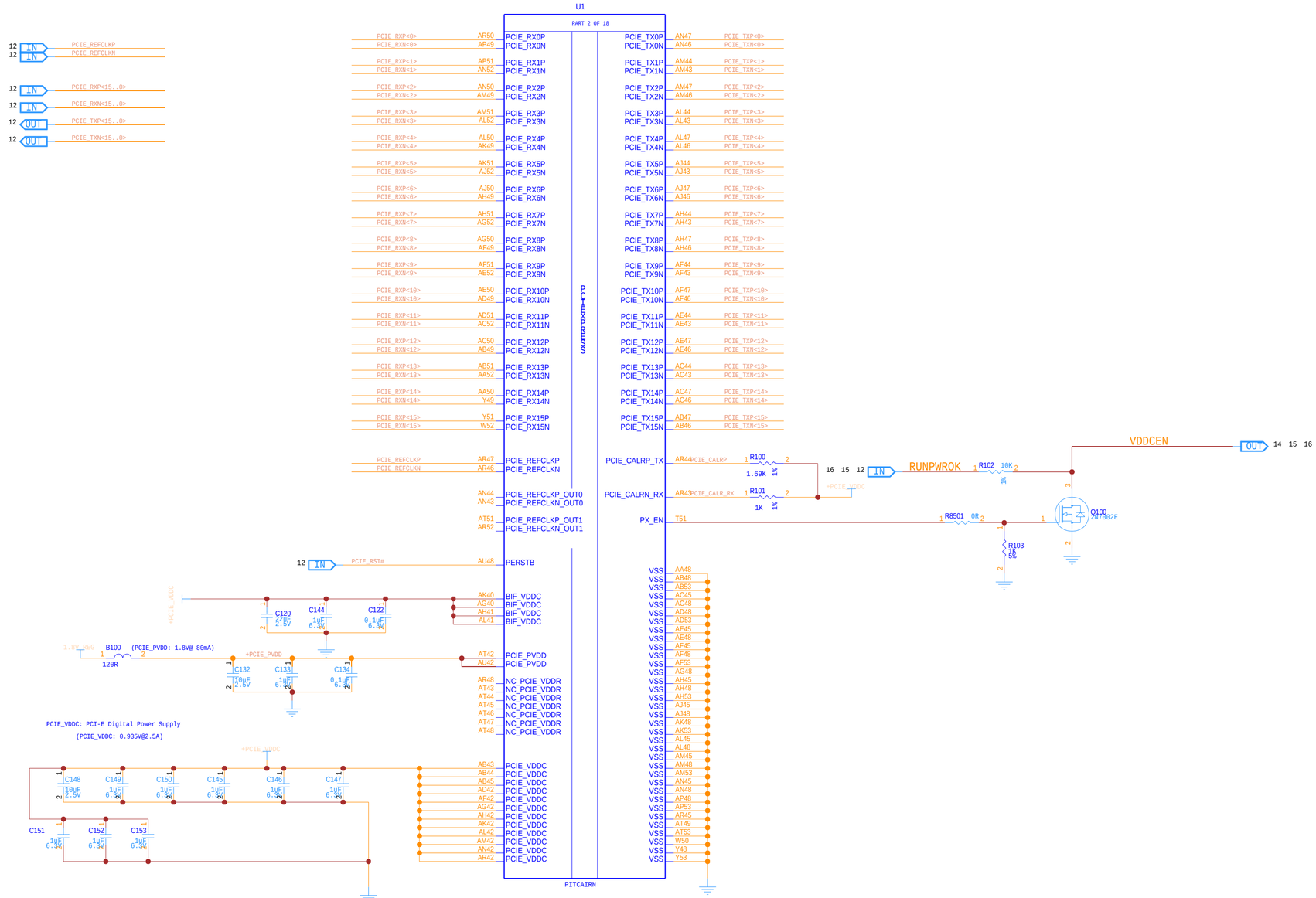

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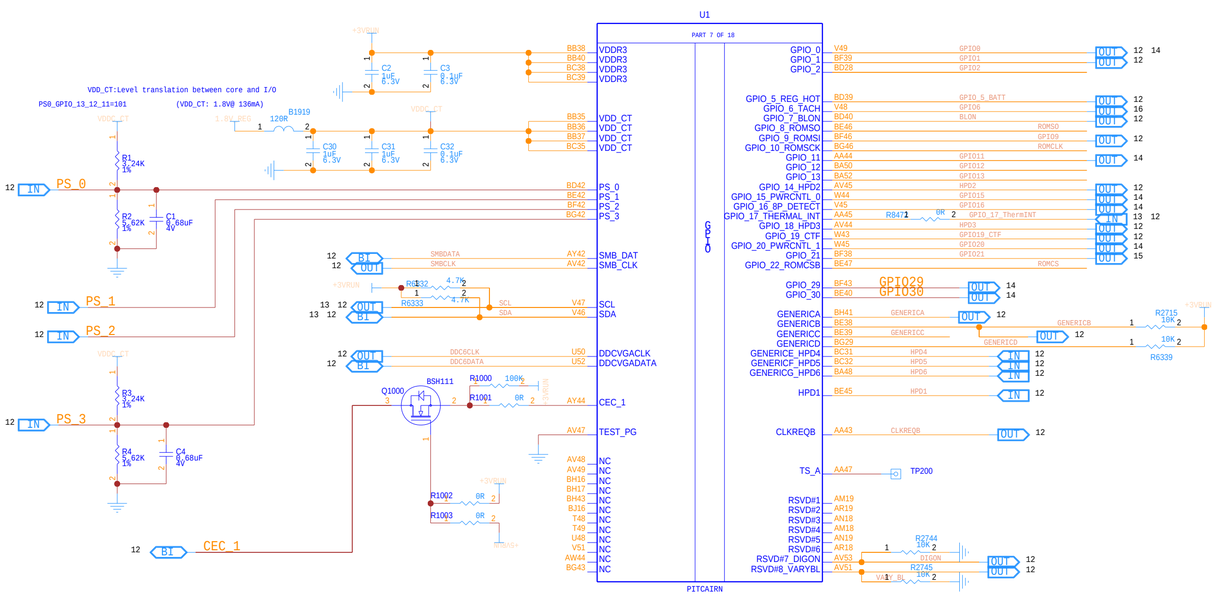
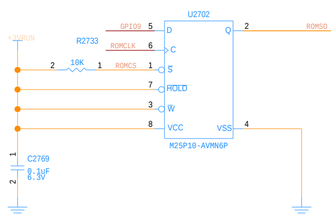
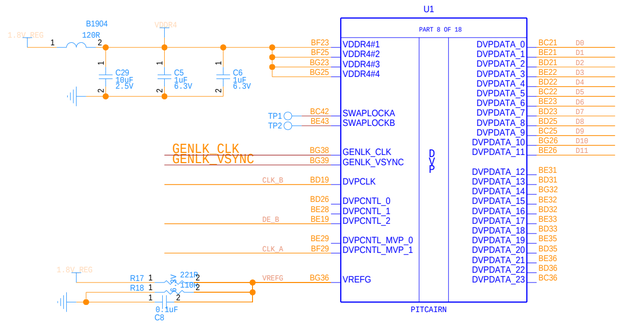
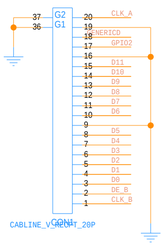
SHEET: Neptune_PCIE	
DATE: Thu May 23 14:48:06 2013 REV: 1.0	
SHEET NUMBER: 1 OF 18	TITLE: 105-C60857-00 Neptune G5 x32 MXM
DOCUMENT NUMBER: 105-CXXX00-00A 105-C60857-00	TITLE









CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
			0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	1
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	1

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO	GPIO21_BB_EN

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SHEET: Neptune_Straps

DATE: Thu May 23 14:48:07 2013 REV: 1.0

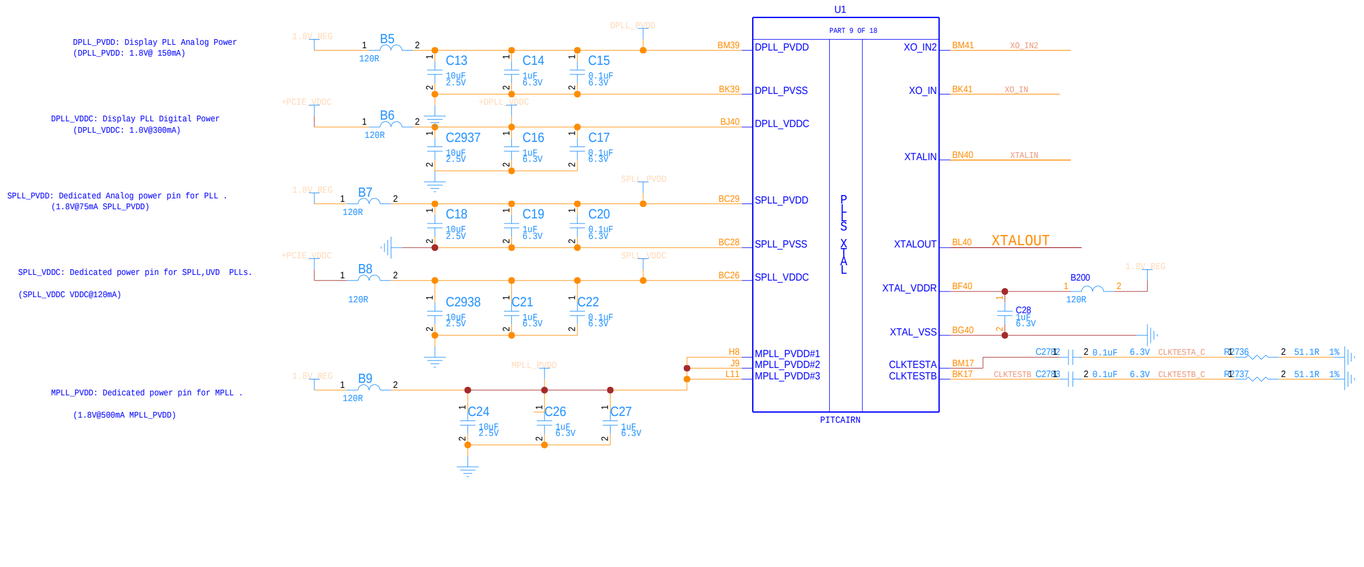
SHEET NUMBER: 2 OF 18

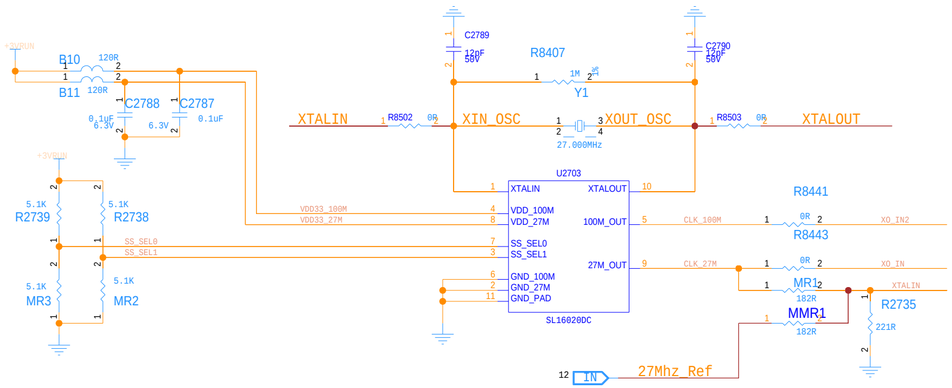
DOCUMENT NUMBER: 105-C60857-00
105-CXXX00-00A

NOTES: NOTE

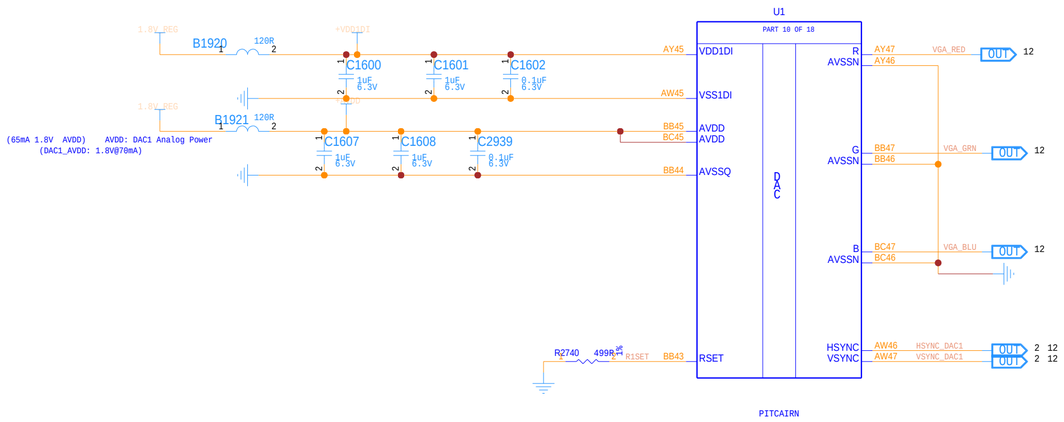
TITLE:
105-C60857-00 Neptune G5 x32 MXM

TITLE





AMD - GRAPHICS 1 COMMERCE VALLEY MARKHAM, ONTARIO, L3T 7X6	
SHEET: Neptune_CLK	
DATE: Thu May 23 14:48:07 2013	REV: 1.0
SHEET NUMBER: 3 OF 18	
DOCUMENT NUMBER: 105-C60857-00 105-CXXX00-00A	TITLE: 105-C60857-00 Neptune G5 x32 MXM TITLE



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MARKHAM, ONTARIO, L3T 7X6

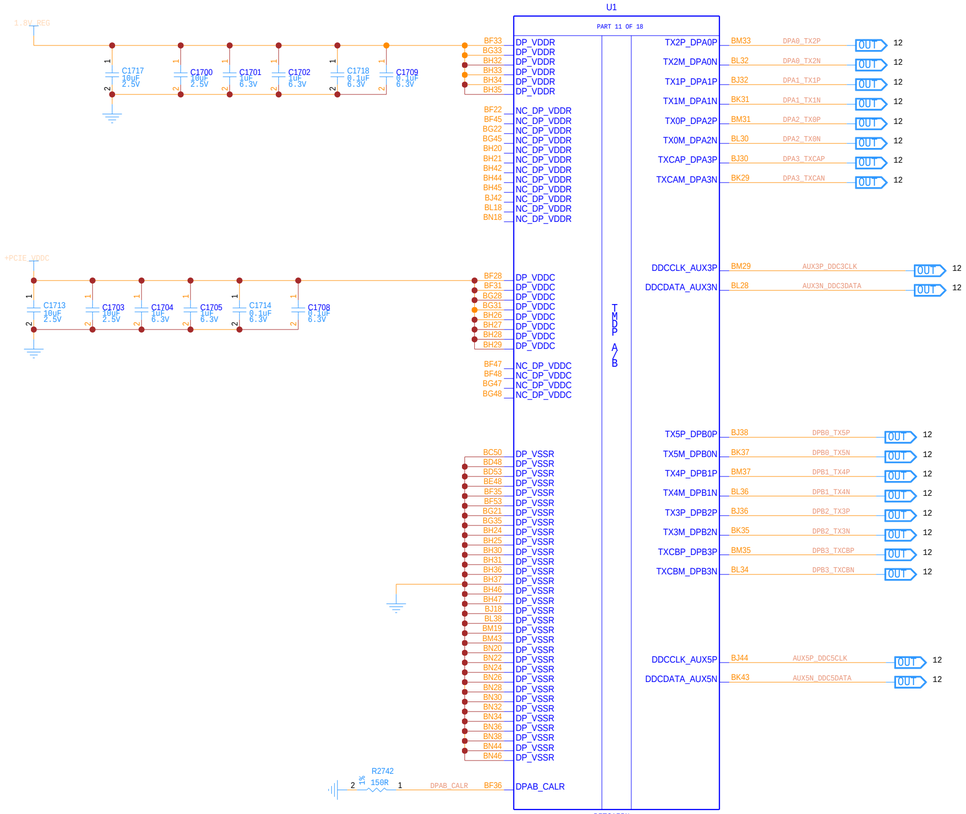
SHEET: Neptune_VGA

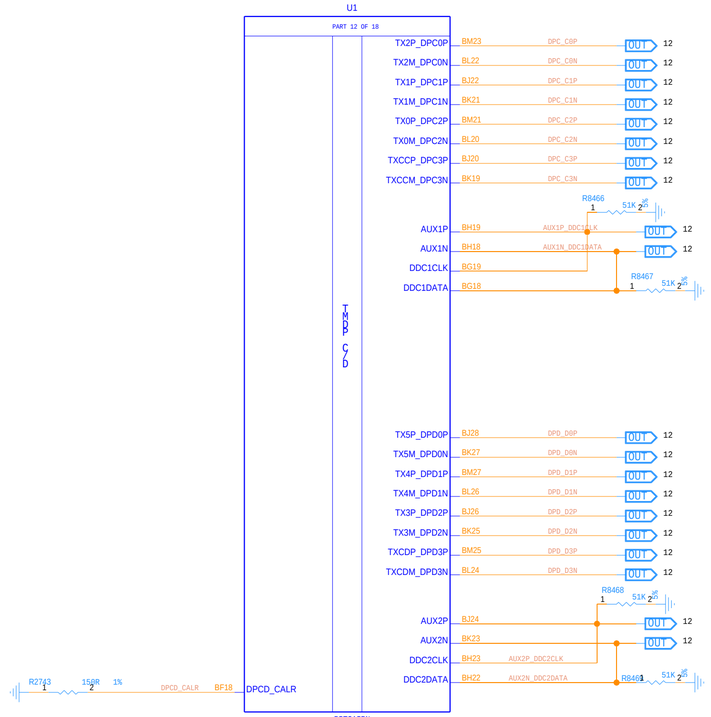
DATE: Thu May 23 14:48:07 2013 REV: 1.0

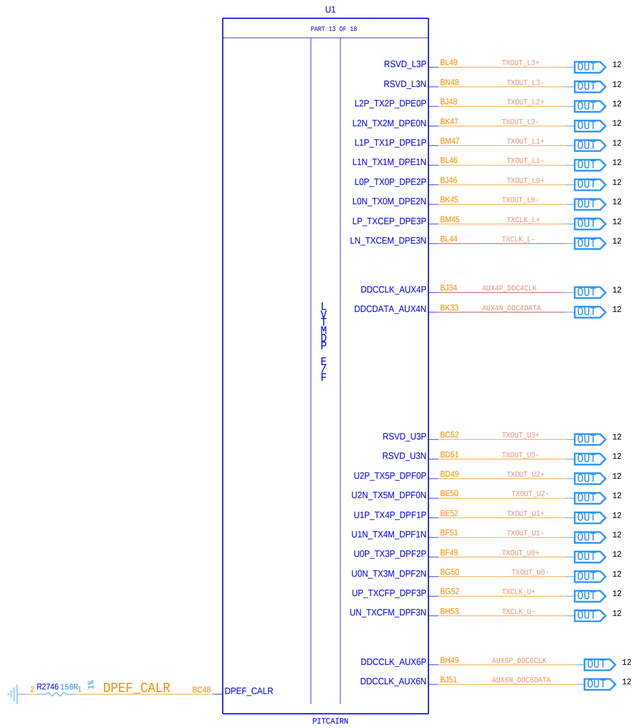
SHEET NUMBER: 4 OF 18

DOCUMENT NUMBER: 105-C60857-00
105-CXXX00-00A

TITLE:
105-C60857-00 Neptune G5 x32 MXM
TITLE







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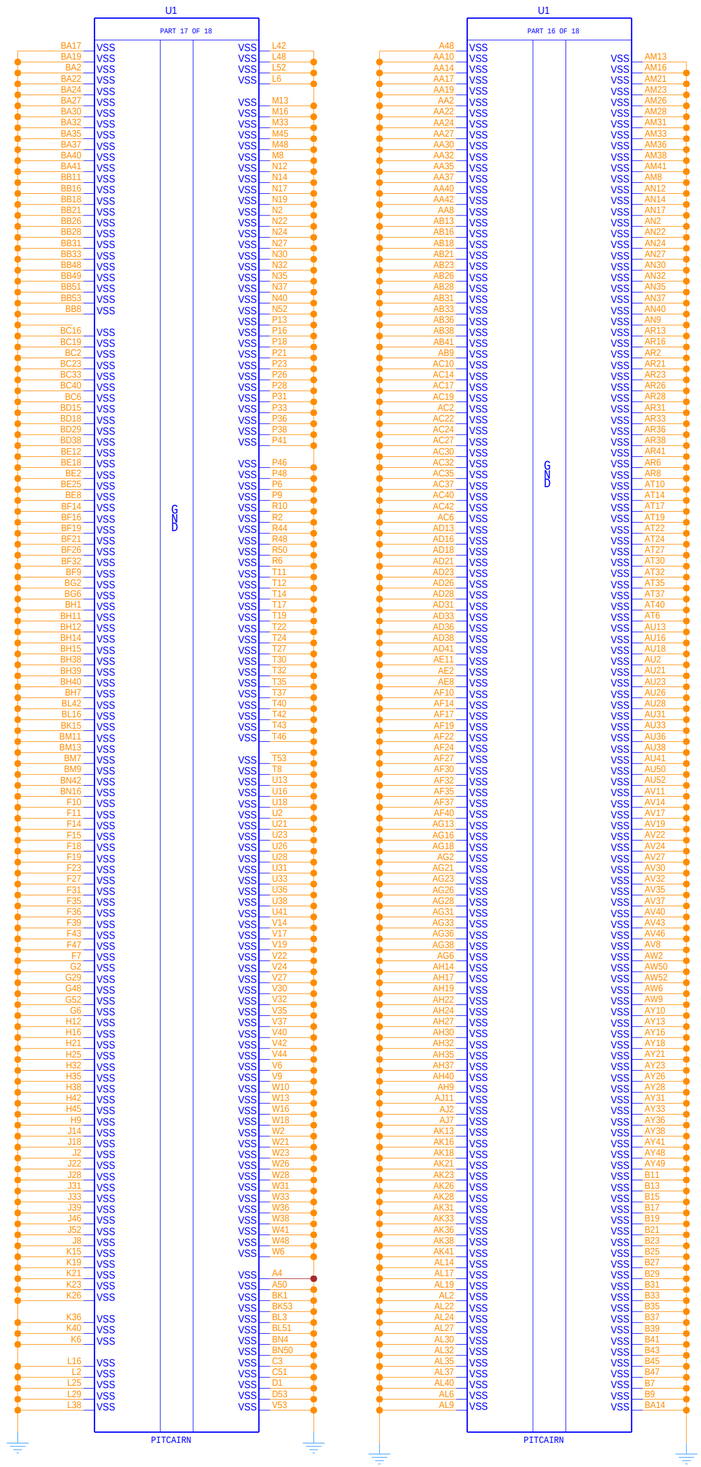
SHEET: Neptune_DPs	
DATE: Thu May 23 14:48:07 2013 REV: 1.0	
SHEET NUMBER: 5 OF 18	TITLE: 105-C60857-00 Neptune G5 x32 MXM
DOCUMENT NUMBER: 105-C60857-00 105-CXXX00-00A	TITLE
NOTES: NOTE	



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SHEET: Neptune_GND

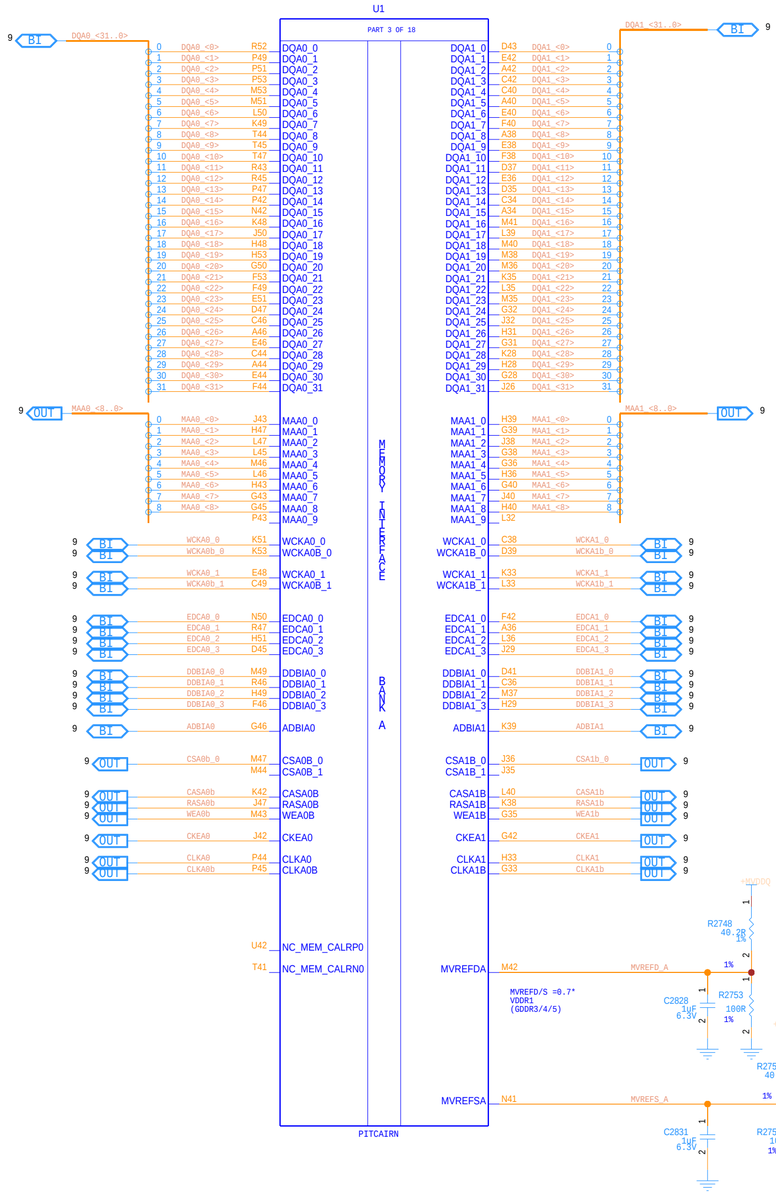
DATE: Thu May 23 14:48:08 2013 REV: 1.0

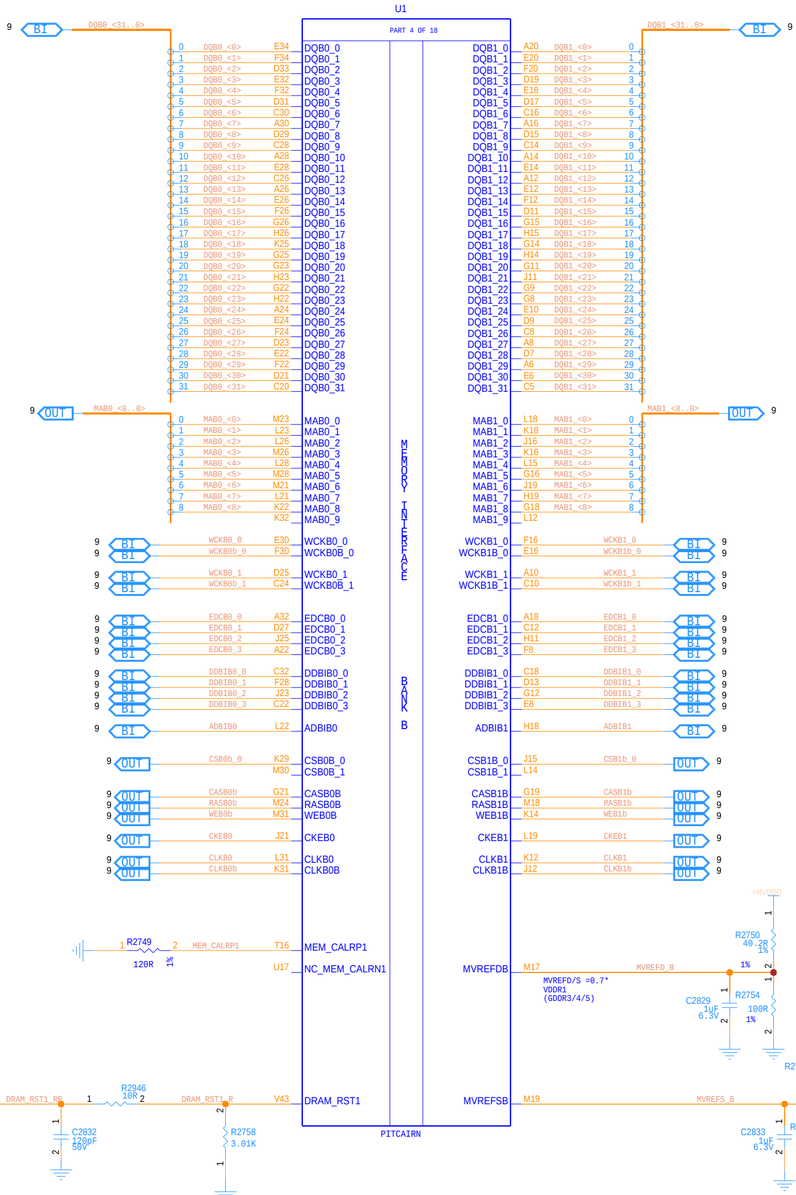
SHEET NUMBER: 6 OF 18

DOCUMENT NUMBER: 105-C60857-00
105-CXXX00-00A

TITLE: 105-C60857-00 Neptune G5 x32 MXM

TITLE





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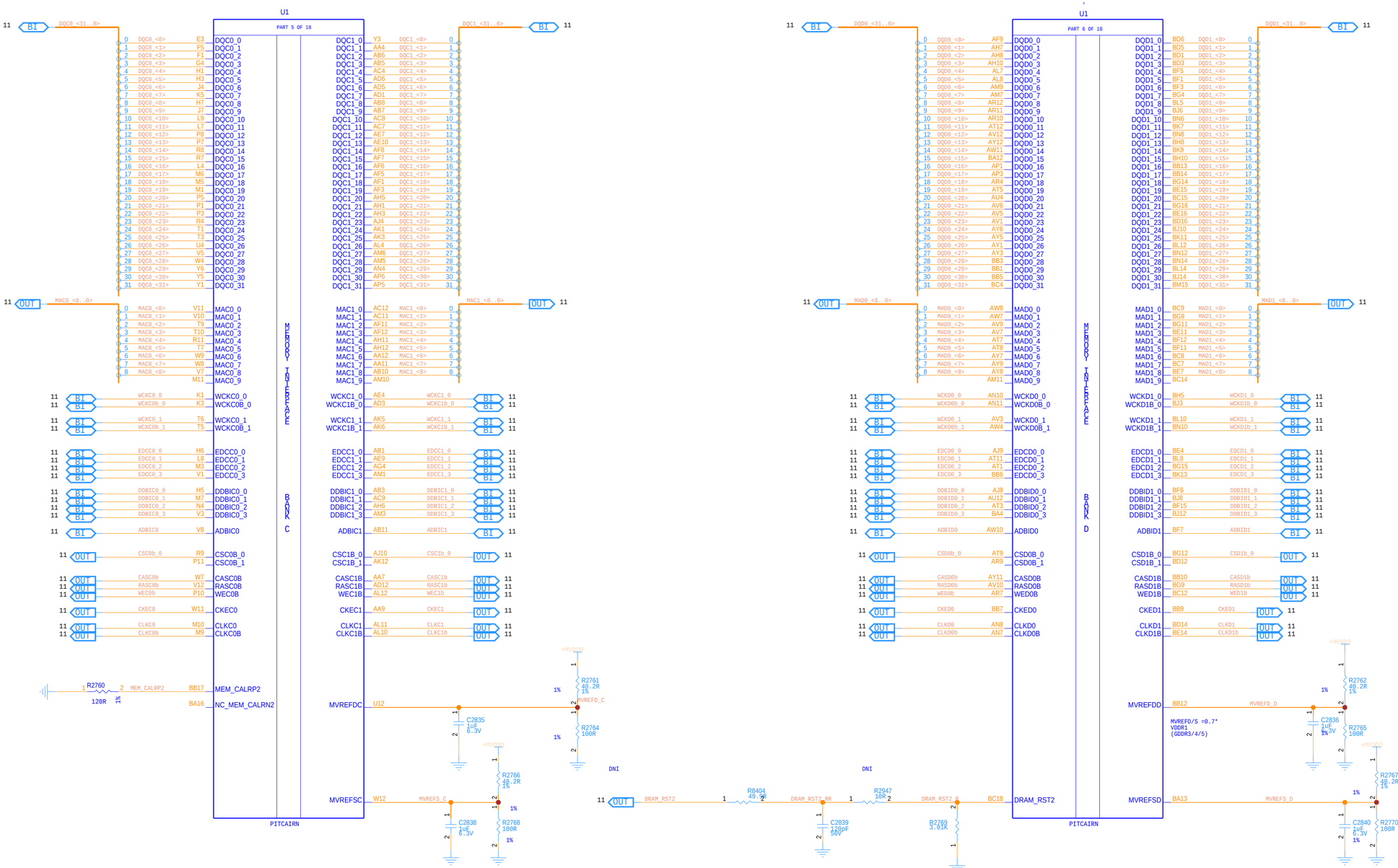
SHEET: Neptune_Memory A/B	
DATE: Thu May 23 14:48:08 2013 REV: 1.0	
SHEET NUMBER: 7 OF 18	TITLE: 105-C60857-00 Neptune G5 x32 MXM
DOCUMENT NUMBER: 105-C60857-00 105-CXXX00-00A	TITLE



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1 COMMERCE VALLEY
MARKHAM, ONTARIO, L3T 7X6

SHEET: Neptune_Memory C/D

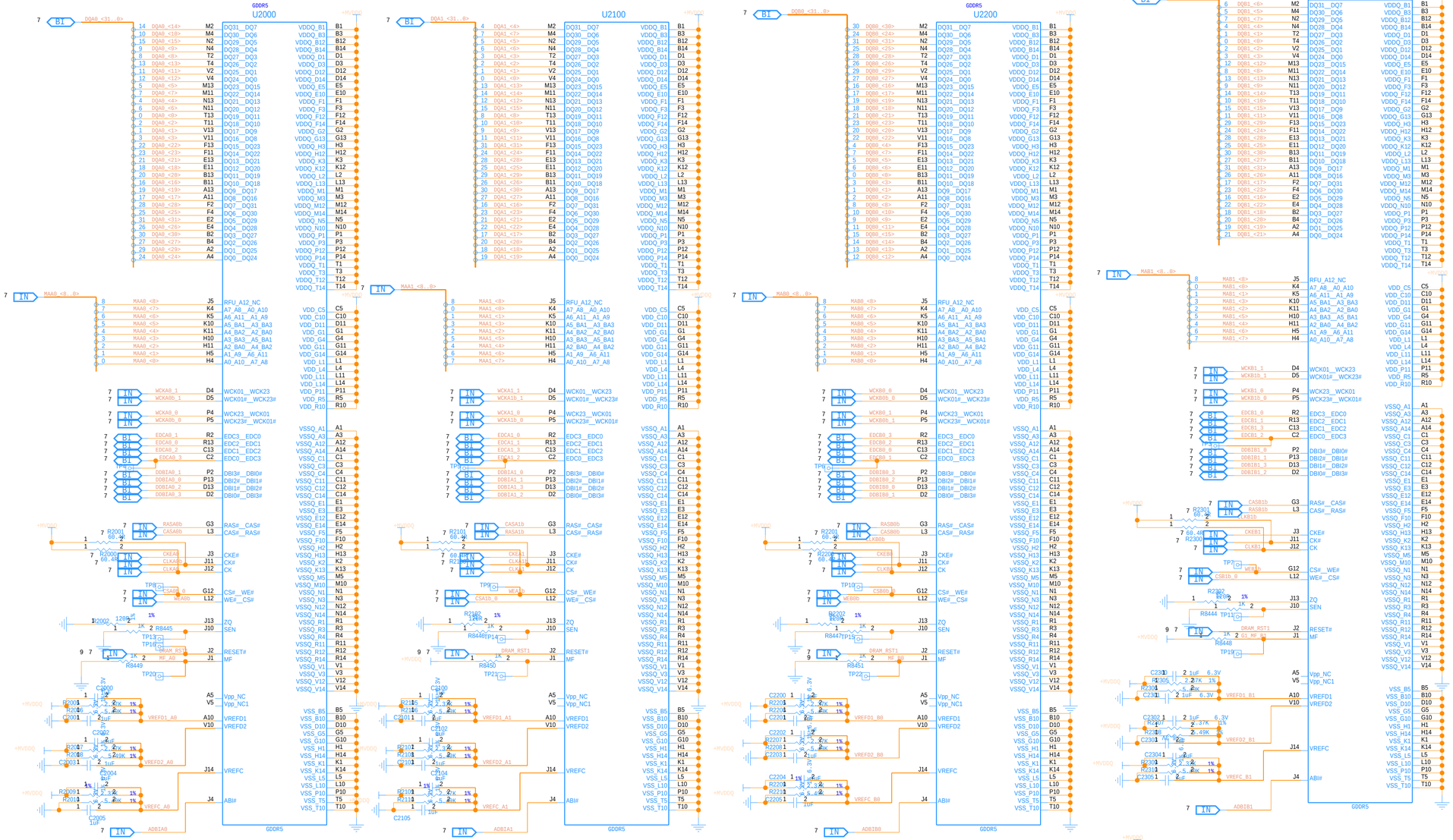
DATE: Thu May 23 14:48:09 2013 REV: 1.0

SHEET NUMBER: 8 OF 18

DOCUMENT NUMBER: 105-C60857-00
105-CXXX00-00A

TITLE: 105-C60857-00 Neptune G5 x32 MXM
TITLE

(5) GDDR5 Memory Channel A&B



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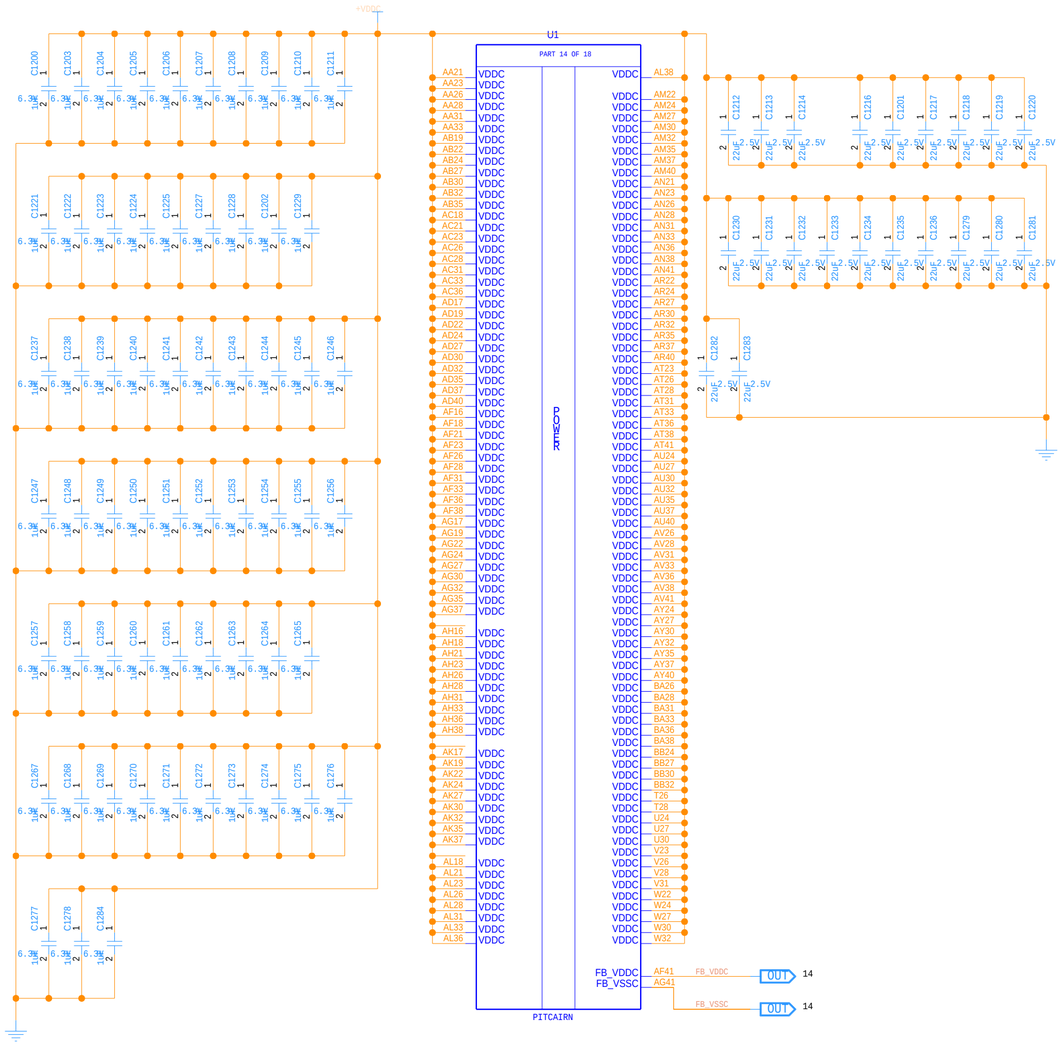
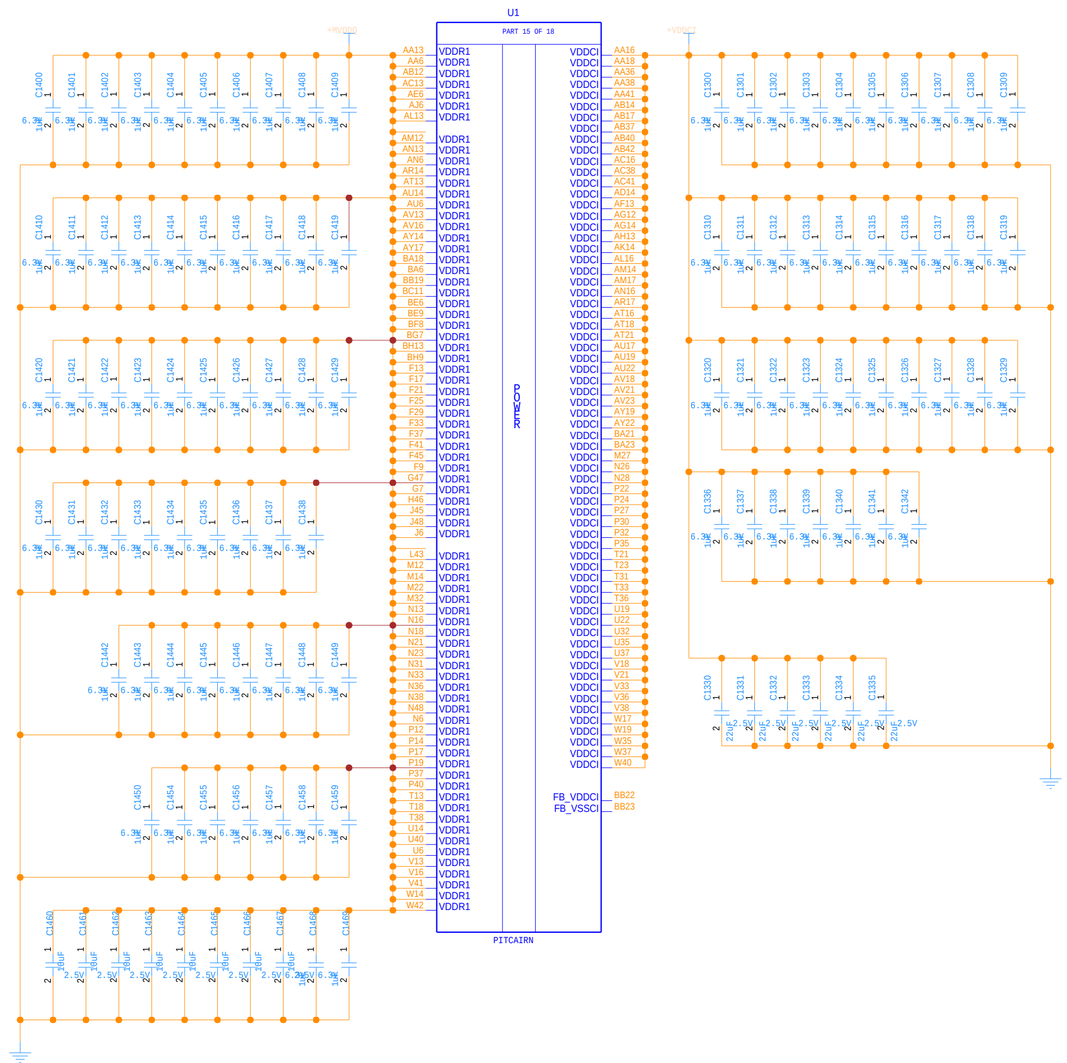
SHEET:	GDDR5 32MX32 A	
DATE:	Thu May 23 14:48:10 2013	REV: 1.0
SHEET NUMBER:	9 OF 18	
DOCUMENT NUMBER:	105-C60857-00 105-CXXX00-00A	
NOTES:	NOTE	

TITLE:

105-C60857-00 Neptune G5 x32 MXM

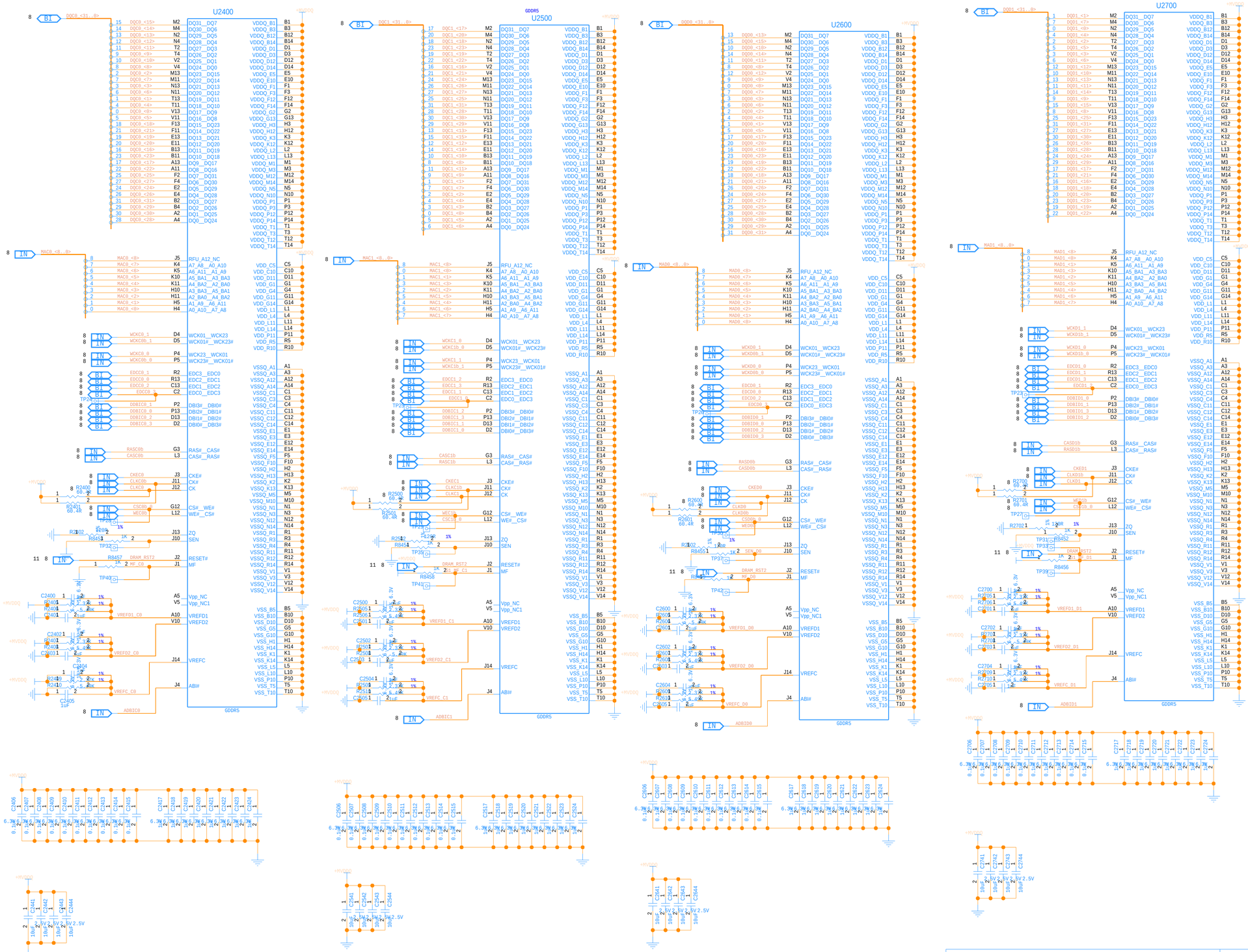
TITLE





AMD - GRAPHICS 1 COMMERCE VALLEY MARKHAM, ONTARIO, L3T 7X6	
SHEET: Neptune_POWER	
DATE: Thu May 23 14:48:10 2013	REV: 1.0
SHEET NUMBER: 10 OF 18	
DOCUMENT NUMBER: 105-C60857-00 105-CXXX00-00A	TITLE: 105-C60857-00 Neptune G5 x32 MXM TITLE

(6) GDDR5 Memory Channel C&D



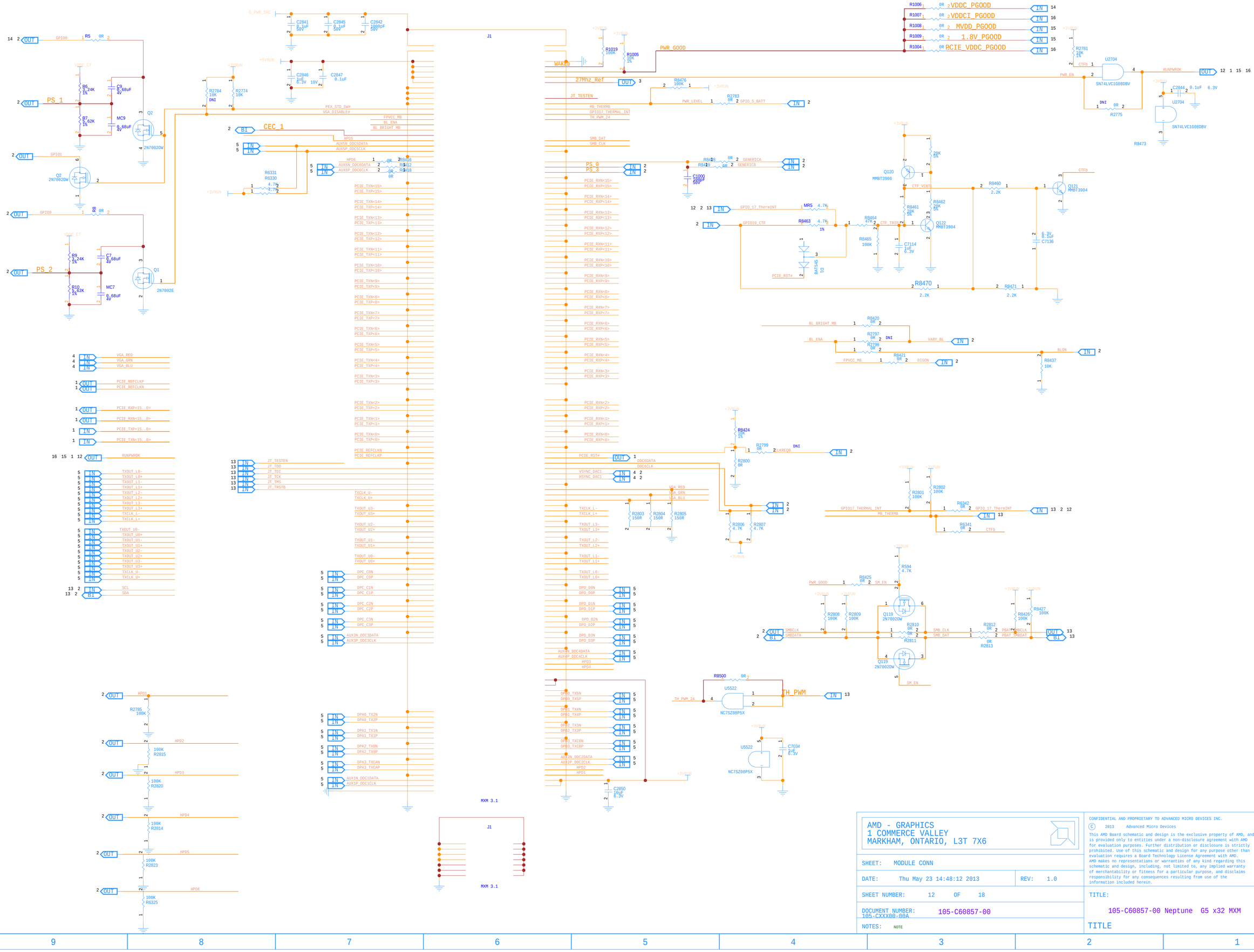
AMD - GRAPHICS
1 COMMERCE VALLEY
MARKHAM, ONTARIO, L3T 7X6

SHEET:	GDDR5 32MX32 B
DATE:	Thu May 23 14:48:11 2013
REV:	1.0
SHEET NUMBER:	11 OF 18
DOCUMENT NUMBER:	105-C60857-00
105-CXXX00-00A	
NOTES:	NOTE

TITLE:

105-C60857-00 Neptune G5 x32 MXM

TITLE



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SHEET: MODULE CONN

DATE: Thu May 23 14:48:12 2013 REV: 1.0

SHEET NUMBER: 12 OF 18

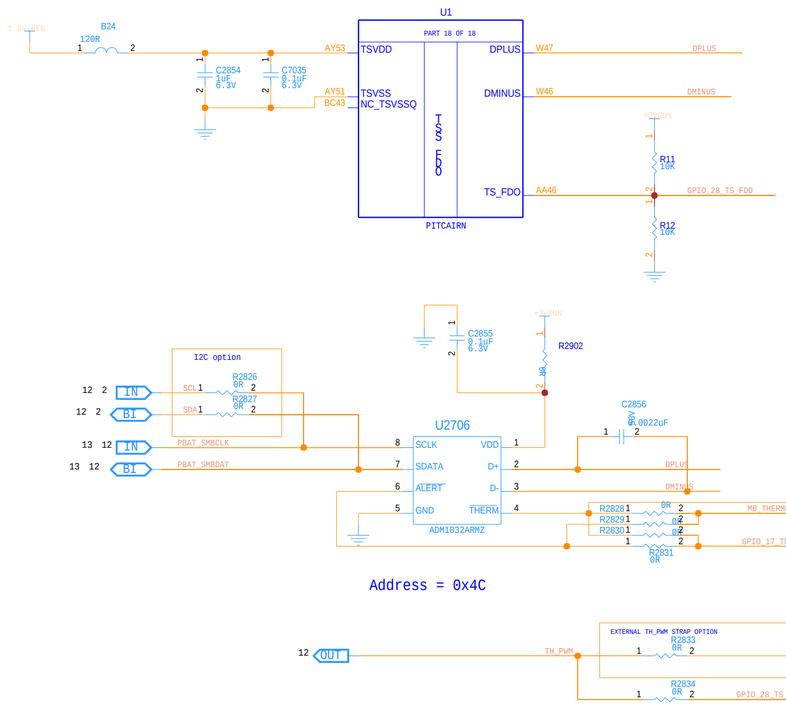
DOCUMENT NUMBER: 105-CXXX00-00A 105-C60857-00

NOTES: NOTE

TITLE:

105-C60857-00 Neptune G5 x32 MXM

TITLE



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SHEET: THERM & MISC	
DATE: Thu May 23 14:48:12 2013 REV: 1.0	
SHEET NUMBER: 13 OF 18	TITLE: 105-C60857-00 Neptune G5 x32 MXM
DOCUMENT NUMBER: 105-CXXX00-00A 105-C60857-00	TITLE

GPU CORE REG

CORE PWM THREE PHASE REGULATOR 0.8V- 1.10V @ 60A

GPIO20	GPIO15	GPIO30	GPIO29	
VID4	VID3	VID2	VID1	VDDC
0	0	0	0	1.100V
0	0	0	1	1.075V
0	0	1	0	1.050V
0	0	1	1	1.025V
0	1	0	0	1.000V
0	1	0	1	0.975V
0	1	1	0	0.950V
1	1	1	1	0.925V
1	0	0	0	0.900V
1	0	0	1	0.875V
1	0	1	0	0.850V
1	0	1	1	0.825V
1	1	0	0	0.800V

U5524 ISL6208CRZ

U5525 ISL62883CHRTZ

RT2 s/b placed close to phase 1 ouput inductor

SET OCP 90A

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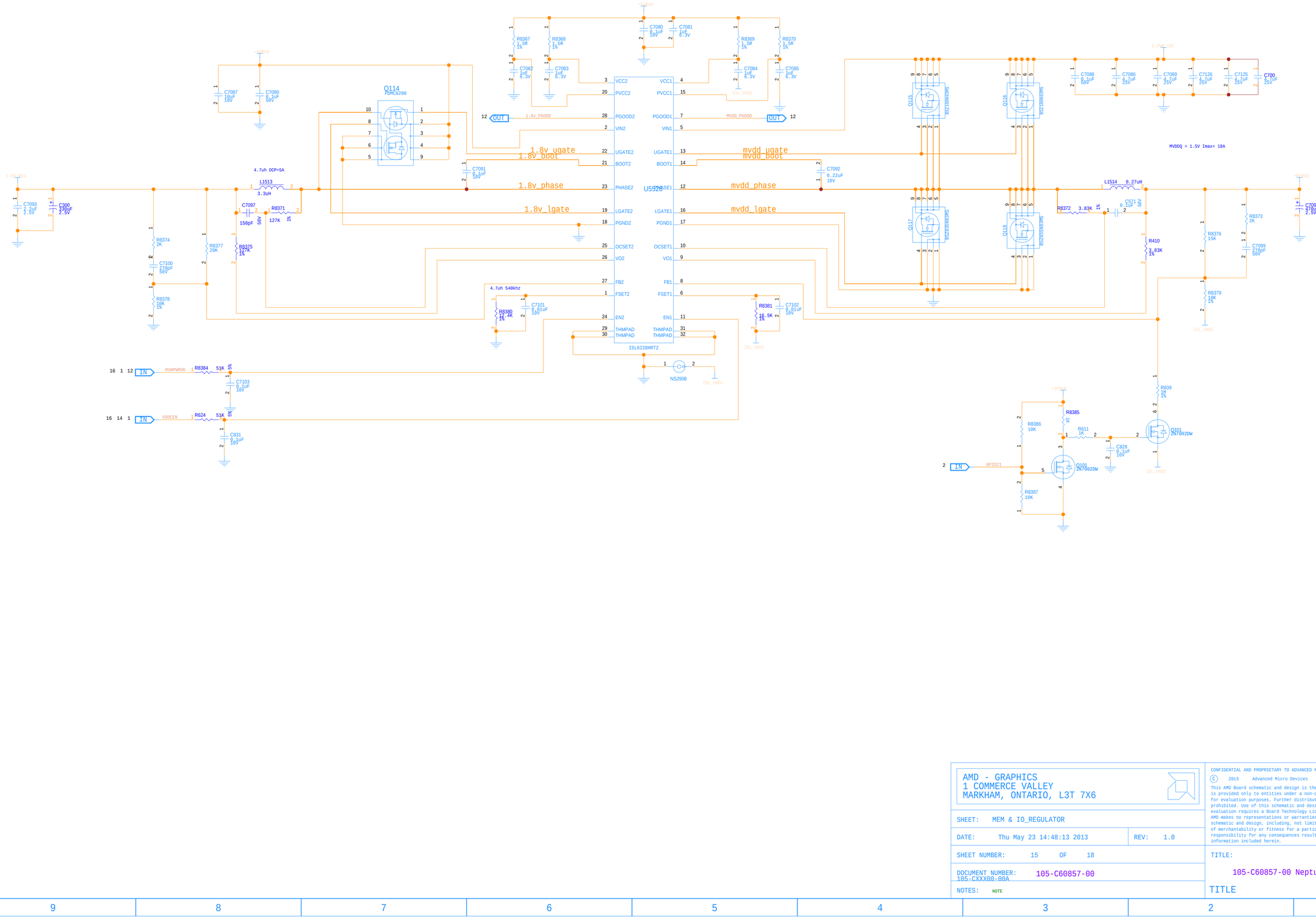
SHEET: CORE_REGULATOR	
DATE: Thu May 23 14:48:13 2013	REV: 1.0
SHEET NUMBER: 14 OF 18	
DOCUMENT NUMBER: 105-CXXX00-00A 105-C60857-00	
NOTES: NOTE	

TITLE: 105-C60857-00 Neptune G5 x32 MXM

TITLE



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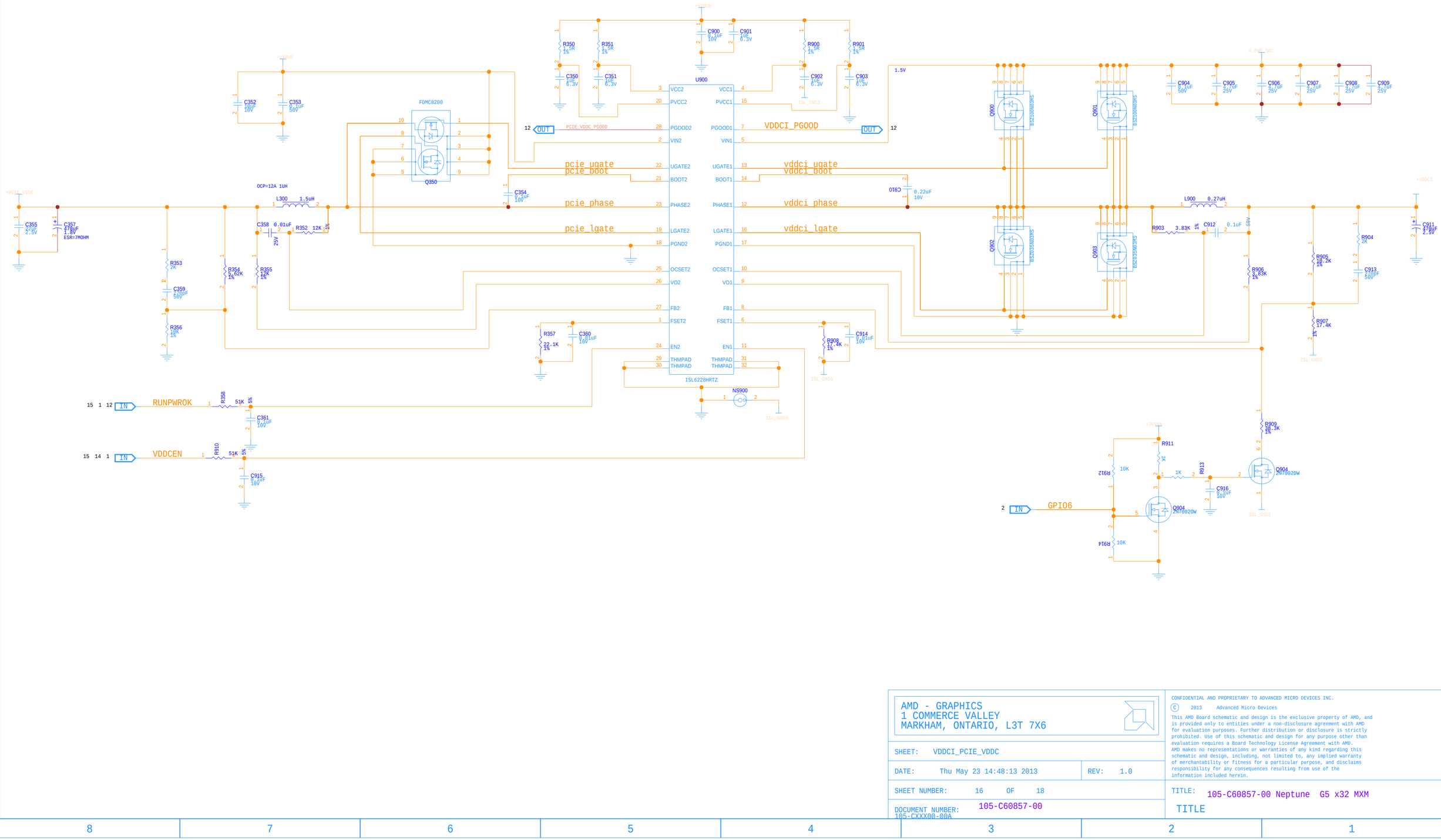
SHEET: MEM & IO_REGULATOR	
DATE: Thu May 23 14:48:13 2013	REV: 1.0
SHEET NUMBER: 15 OF 18	TITLE: 105-C60857-00 Neptune G5 x32 MXM
DOCUMENT NUMBER: 105-CXXX00-00A 105-C60857-00	TITLE
NOTES: NOTE	

VDDCI REGULATOR 0.9V/0.85V @ 12A



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SHEET: VDDCI_PCIE_VDDC	
DATE: Thu May 23 14:48:13 2013 REV: 1.0	
SHEET NUMBER: 16 OF 18	TITLE: 105-C60857-00 Neptune G5 x32 MXM
DOCUMENT NUMBER: 105-CXXX00-00A	105-C60857-00 TITLE

MEMORY CHANNEL A & B & C & D

GDDR5 8PCS 64Mx32/32Mx32

CH A&B&C&D

POWER REGULATORS

From +PWR_SRC

+VDDC, +MVDD, VDDCI

FROM +5VRUN

+0.935.1.8V_REG

From +3VRUN

From +VDDC

VDDC,

From +MVDD

VDDR1, MVDDQ/C,

FROM +1.8V_REG

VDDR4, VDD_CT, TSVDD,

PCIE_VDDR, PCIE_PVDD,
DPLL_PVDD, DPX_PVDD,
DPX_VDD18, MPV18, SPV18,

AVDD, VDD1DI,

FROM +pcie_vddc

PCIE_VDDC, DPLL_VDDC,

DPX_VDD10, SPV10, BIF_VDDC

MxM3.0 SOURCE

+3VRUN +5VRUN +PWR_SRC

SMPS ENABLE CIRCUIT

STRAPS

GPIO

BIOS

ROM

OSC/SS

XO_IN/XO_IN2

DYNAMIC MVDD

DYNAMIC VDDC

POWER DELIVERY

CRITICAL TEMPERATURE

PCIE

LVTMDP

TMDPEF

DDCAUX5

HPD5

TMDP

TMDPA

DDCAUX1

HPD1

TMDPB

DDCAUX2

HPD2

TMDPC

DDCAUX3

HPD3

TMDPD

DDCAUX4

HPD4

DAC1

DAC1 RGB

DDC6

V/HSYNC

THERMAL

GPIO3, GPIO4

SCL/SDA

D+/D-

GPIO17

GPIO19_CTF

I2C

TEMP. SENSING

INTERRUPT

EXTERNAL

TEMPERATURE

SENSOR

LVDS/DP_E

LVDS_LTXx/LTXx#
LVDS_UTXx/UTXx#

LVDS_DDC_CLK/DAT

DVI_HPD

DP_A

DP_A_Lx/Lx#

DP_A_AUX/AUX#

DP_A_HPD

DP_B

DP_B_LX/LX#

DP_B_AUX/AUX#

DP_B_HPD

DP_C

DP_C_LX/LX#

DP_C_AUX/AUX#

DP_C_HPD

DP_B

DP_B_LX/LX#

DP_B_AUX/AUX#

DP_B_HPD

VGA

VGA_RED/GREEN/BLUE

VGA_DDC_CLK/DAT

VGA_VSYNC/HSYNC

SMB_CLK/DAT

TH_ALERT#

TH_OVERT#

3VRUN

5VRUN

PWR_SRC

MXM3.1 CONNECTOR

MxM3.1 TYPE B

Wimbledon L2 GDDR5

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MARKHAM, ONTARIO, L3T 7X6

SHEET: SHEET TITLE

DATE: Thu May 23 14:48:14 2013 REV: 1.0

SHEET NUMBER: 17 OF 18

DOCUMENT NUMBER: 105-C60857-00
105-CXXX00-00A

TITLE: 105-C60857-00 Wimbledon G5 x32 MXM
TITLE

AMD

TITLE: TITLE

105-C60857-00 Neptune G5 x32 MXM

DOCUMENT NUMBER: 105-C60857-00
105-CXXX00-00A

DATE: Thu May 23 14:49:49 2013

SHEET NUMBER: 18 OF 18

REV: 1.0

REVISION HISTORY

ENGINEER: XXX

NOTES: NOTE

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1 COMMERCE VALLEY
MARKHAM, ONTARIO, L3T 7X6

SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
0	00A	03/12/12	Initial release on Base C429 rev.00
01	00	05/22/13	HWQ finihsed, release sch to rev.00