

P699-B01: GT215/6/8 MXM V3.0 TYPE A  
512/1024MB 128/64-BIT DDR3  
LVDS, QUAD DP, DVI, VGA

Table of Contents:

Page 1: Cover Page  
Page 2: PCI EXPRESS Interface  
Page 3: Frame Buffer GPU Interface  
Page 4: Frame Buffer Partition A Lower 32 Bits  
Page 5: Frame Buffer Partition A Upper 32 Bits  
Page 6: Frame Buffer Partition C Lower 32 Bits  
Page 7: Frame Buffer Partition C Upper 32 Bits  
Page 8: Memory Decoupling Caps  
Page 9: DAC\_A, DAC\_B, SPREAD, PLL, CRYSTAL  
Page 10: DP LINKS C, D, E, F  
Page 11: MXM Connector, I/O-Section  
Page 12: GPIOs, JTAG, Thermal Sensor  
Page 13: LVDS, VBIOS HDCP ROM, and CEC  
Page 14: MIOA, MIOB, GPU VDD\DCPLNG\GND  
Page 15: NVVDD Power Supply and 3V3\_RUN  
Page 16: FBVDDQ, PEXVDD, and VDD\_I/O\_PLL Power Supplies  
Page 17: STRAPS and MOUNTING HOLES

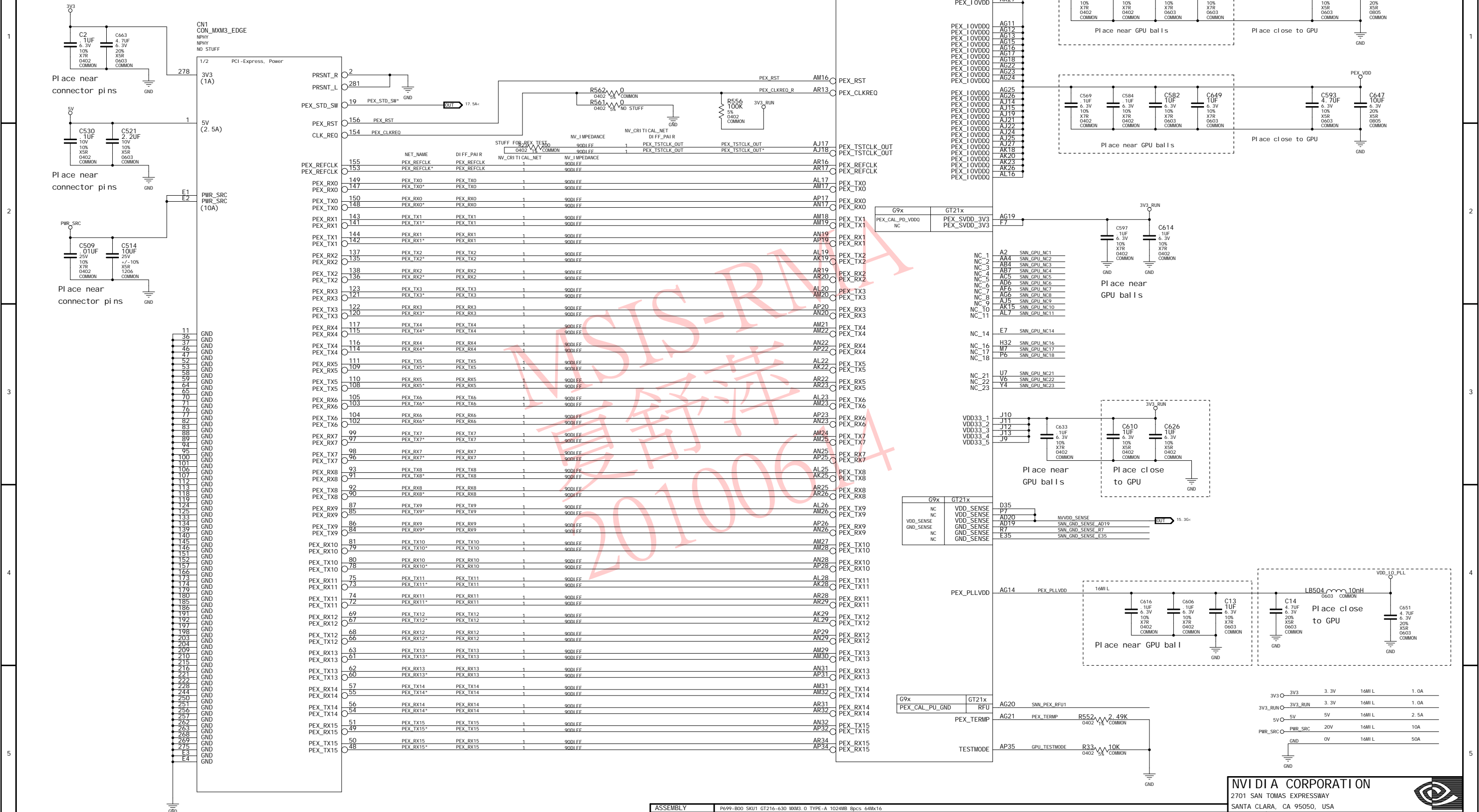
MSIS-RMA  
夏舒萍  
20100614

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10699-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
1	SKU0001	600-10699-0001-100	P699-ADD SKU1 GT216-630 MXM3.0 TYPE-A 1024MB 8pcs 64Mx16
2	SKU0002	600-10699-0002-100	P699-ADD SKU2 GT216-600 MXM3.0 TYPE-A 1024MB 8pcs 64Mx16
3	SKU0003	600-10699-0003-100	P699-ADD SKU3 GT218-730 MXM3.0 TYPE-A 512 MB 4pcs 64Mx16
4	SKU0005	600-10699-0005-100	P699-ADD SKU5 GT216-640 MXM3.0 TYPE-A 1024 MB 8pcs 64Mx16
5	SKU0501	600-50699-0501-100	P699-ADD SKU501 GT216-950 MXM3.0 TYPE-A 1024MB 8pcs 64Mx16
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

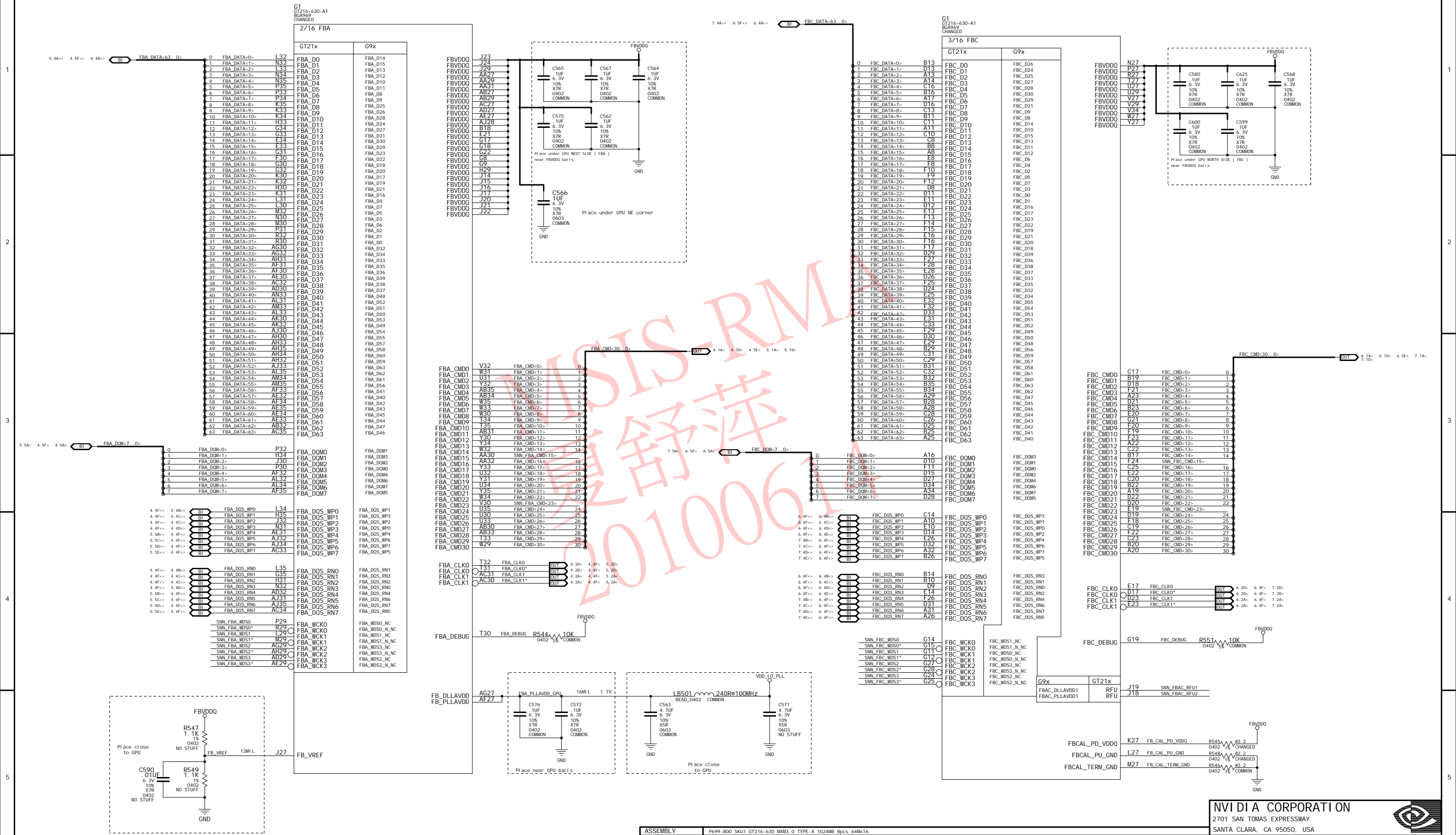
ASSEMBLY		P699-B00 SKU1 GT216-630 MXM3.0 TYPE-A 1024MB 8pcs 64Mx16		SANTA CLARA, CA 95050, USA			
PAGE DETAIL		Cover Page		NV_PN 600-10699-0015-200 A			
AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY VISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.				ID	p699	PAGE	1 OF 17
				NAME	si xu	DATE	08-JUL-2009

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

## 2. MXM 3.0 CONNECTOR, PCI EXPRESS INTERFACE



3. GPU MEMORY INTERFACE



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV\_PN

600-10699-0015-200 A

ID

p699

PAGE

3 OF 17

NAME

SI XU

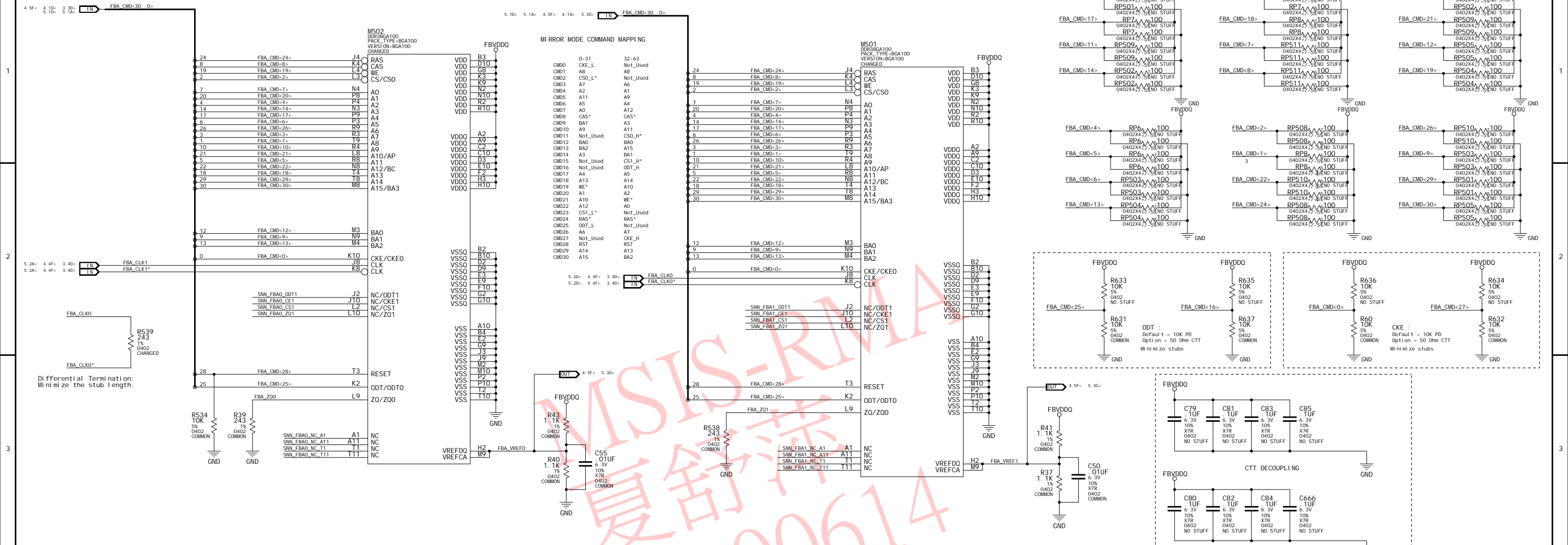
DATE

08-JUL-2009































ASSEMBLY	P699-B00 SKU1 GT216-630 MM3.0 TYPE-A 1024MB 8pins 64Mx16
PAGE DETAIL	Frame Buffer GPU Interface



#### 4. MEMORY PARTITION A LOWER 32 BITS



## MEMORY PARTITION AND SIGNAL CONSTRAINTS

			NET	DI FPFAI R	CRI TI CAL	I MPEDANCE
5. 2D<	4. 2D<	3. 4D>	 I N	FBA_CLK0	FBA_CLK0	70DI FF
5. 2D<	4. 2D<	3. 4D>	 I N	FBA_CLK0*	FBA_CLK0	70DI FF
5. 2A<	4. 2A<	3. 4D>	 I N	FBA_CLK1	FBA_CLK1	70DI FF
5. 2A<	4. 2A<	3. 4D>	 I N	FBA_CLK1*	FBA_CLK1	70DI FF
4. 4B<+	3. 4A<+		 B I	FBA_DQS_WP0	FBA0DQ0	80DI FF
4. 4B<+	3. 4A<+		 B I	FBA_DQS_RN0	FBA0DQ0	80DI FF
4. 4C<+	3. 4A<+		 B I	FBA_DQS_WP1	FBA0DQ1	80DI FF
4. 4C<+	3. 4A<+		 B I	FBA_DQS_RN1	FBA0DQ1	80DI FF
4. 4C<+	3. 4A<+		 B I	FBA_DQS_WP2	FBA0DQ2	80DI FF
4. 4C<+	3. 4A<+		 B I	FBA_DQS_RN2	FBA0DQ2	80DI FF
4. 4D<+	3. 4A<+		 B I	FBA_DQS_WP3	FBA0DQ3	80DI FF
4. 4D<+	3. 4A<+		 B I	FBA_DQS_RN3	FBA0DQ3	80DI FF
5. 5B<+	3. 4A<+		 B I	FBA_DQS_WP4	FBA0DQ4	80DI FF
5. 5B<+	3. 4A<+		 B I	FBA_DQS_RN4	FBA0DQ4	80DI FF
5. 5C<+	3. 4A<+		 B I	FBA_DQS_WP5	FBA0DQ5	80DI FF
5. 5C<+	3. 4A<+		 B I	FBA_DQS_RN5	FBA0DQ5	80DI FF
5. 5D<+	3. 4A<+		 B I	FBA_DQS_WP6	FBA0DQ6	80DI FF
5. 5D<+	3. 4A<+		 B I	FBA_DQS_RN6	FBA0DQ6	80DI FF
5. 5E<+	3. 4A<+		 B I	FBA_DQS_WP7	FBA0DQ7	80DI FF
5. 5E<+	3. 4A<+		 B I	FBA_DQS_RN7	FBA0DQ7	80DI FF
5. 4A<+	4. 4A<+	3. 1A<+	 B I	FBA_DATA<63..0>		40Q/H
5. 5A<	4. 5A<	3. 2A<+	 I N	FBA_DQM<7..0>		40Q/H
5. 1D<	5. 1A<	4. 1D<	 I N	FBA_CMD<30..0>		40Q/H
			NET	MI N_LI NE_WI DTH	VOLTAGE	
			 I N	FBA_VREF_PD	16MI L	0. 9V
5. 3D<	4. 3D>		 I N	FBA_VREF0	16MI L	0. 9V
5. 3G<+	4. 3G>		 I N	FBA_VREF1	16MI L	0. 9V
			 B I	FBA_Z00	16MI L	1. 8OV
5. 3B<+			 B I	FBA_Z01	16MI L	1. 8OV
			 B I	FBA_Z02	16MI L	1. 8OV
5. 3E<+			 B I	FBA_Z03	16MI L	1. 8OV

NVI DI A CORPORATI ON

2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA

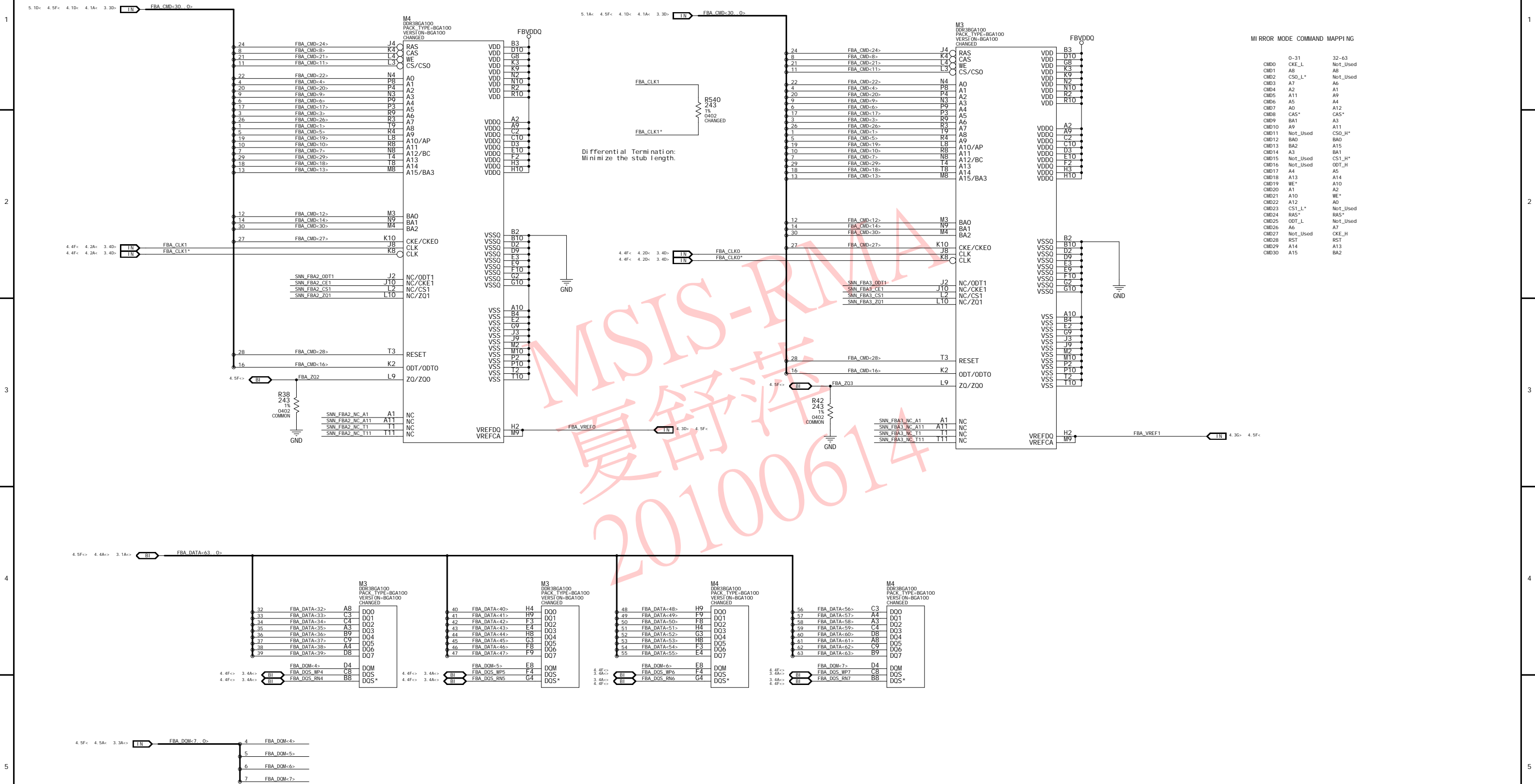


NV_PN	600-10699-0015-200 A		
ID	p699	PAGE	4 OF 17
NAME	si xu	DATE	08-JUL-2009

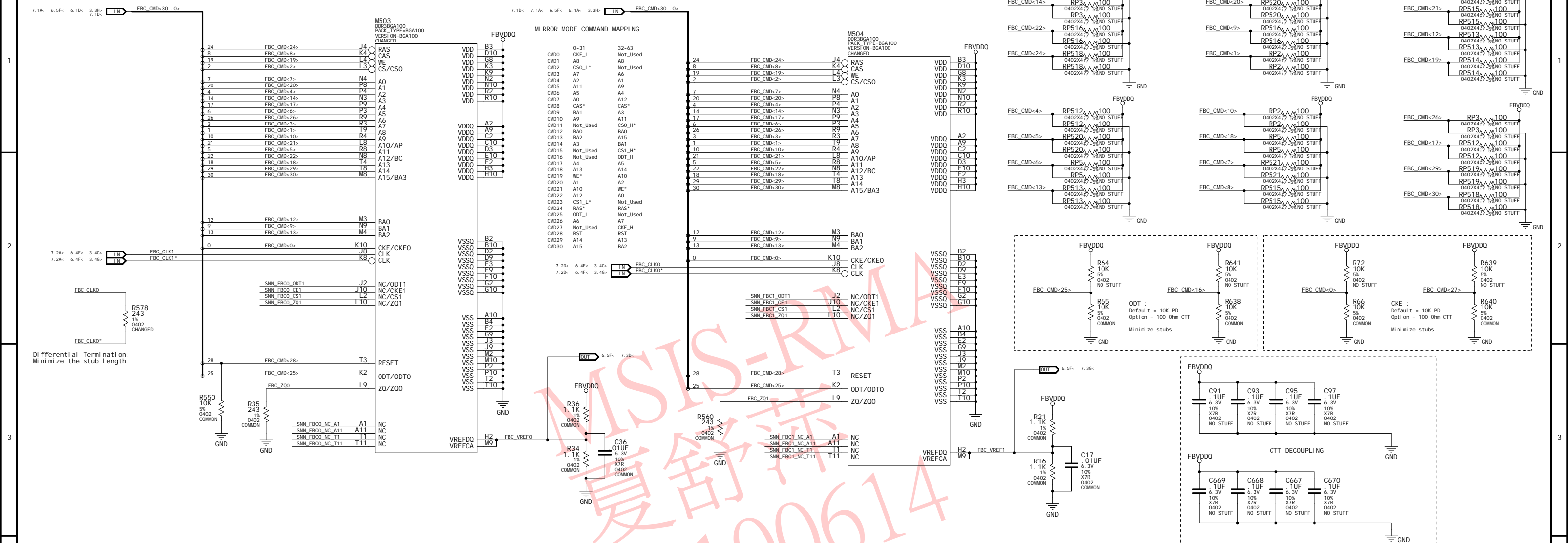
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	P699-B00 SKU1 GT216-630 MXM3.0 TYPE-A 1024MB 8pcs 64Mx16
PAGE DETAIL	Frame Buffer Partition A Lower 32 Bits

5. MEMORY PARTITION A UPPER 32 BITS



## 6. MEMORY PARTITION C LOWER 32 BITS



## MEMORY PARTITION C SIGNAL CONSTRAINTS

			NET	DI FFP41 R	CRI TI CAL	IMPEDANCE
7.2D<	6.2D<	3.4G<	1N	FBC_CLKO	FBC_CLKO	700I FF
7.2D<	6.2D<	3.4G<	1N	FBC_CLKO*	FBC_CLKO	700I FF
7.2A<	6.2A<	3.4G<	1N	FBC_CLK1	FBC_CLK1	700I FF
7.2A<	6.2A<	3.4G<	1N	FBC_CLK1*	FBC_CLK1	700I FF
6.4E<	3.4E<		1N	FBC_DOS_WPO	FBCDOS0	800I FF
6.4E<	3.4E<		B1	FBC_DOS_RNO	FBCDOS0	800I FF
6.4E<	3.4E<		B1	FBC_DOS_WP1	FBCDOS1	800I FF
6.4E<	3.4E<		B1	FBC_DOS_RN1	FBCDOS1	800I FF
6.4E<	3.4E<		B1	FBC_DOS_WP2	FBCDOS2	800I FF
6.4E<	3.4E<		B1	FBC_DOS_RN2	FBCDOS2	800I FF
6.4E<	3.4E<		B1	FBC_DOS_WP3	FBCDOS3	800I FF
6.4E<	3.4E<		B1	FBC_DOS_RN3	FBCDOS3	800I FF
7.4E<	3.4E<		B1	FBC_DOS_WP4	FBCDOS4	800I FF
7.4E<	3.4E<		B1	FBC_DOS_RN4	FBCDOS4	800I FF
7.4E<	3.4E<		B1	FBC_DOS_WP5	FBCDOS5	800I FF
7.4E<	3.4E<		B1	FBC_DOS_RN5	FBCDOS5	800I FF
7.4E<	3.4E<		B1	FBC_DOS_WP6	FBCDOS6	800I FF
7.4E<	3.4E<		B1	FBC_DOS_RN6	FBCDOS6	800I FF
7.4E<	3.4E<		B1	FBC_DOS_WP7	FBCDOS7	800I FF
7.4E<	3.4E<		B1	FBC_DOS_RN7	FBCDOS7	800I FF

7. 4A<	6. 4A<	3. 1E<	BI	FBC_DATA<63, 0>	2	400HM
7. 5A<	6. 5A<	3. 3D<	1N	FBC_DQM<-7, 0>	2	400HM
7. 1D<	7. 1A<	6. 1D<	1N	FBC_CMD<27, 0>	2	400HM
NET						
			1N	FBC_VREF_PD	MIN_LINewidth	VOLTAGE
7. 3D<	6. 3D<		1N	FBC_VREF0	16MI L	0. 9V
7. 3G<	6. 3F<		1N	FBC_VREF1	16MI L	0. 9V
			1N	FBC_VREF1	16MI L	0. 9V
			BI	FBC_Z00	16MI L	1. 80V
			BI	FBC_Z01	16MI L	1. 80V
7. 3B<			BI	FBC_Z02	16MI L	1. 80V
7. 3E<			BI	FBC_Z03	16MI L	1. 80V

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA

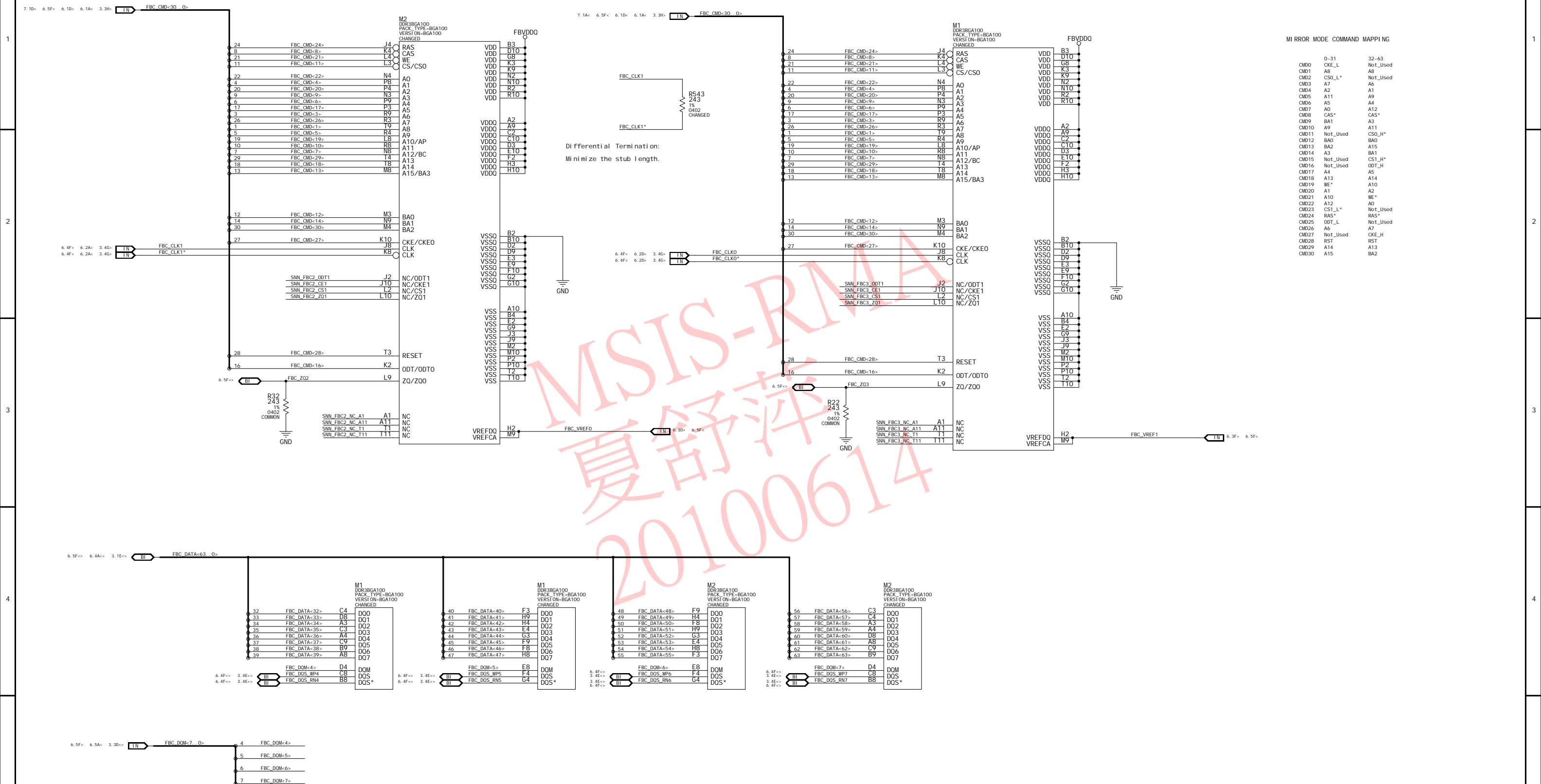


NV_PN	600-10699-0015-200 A
-------	----------------------

ID	p699	PAGE	6 OF 17
NAME	si xu	DATE	08-JUL-2009

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

## 7. MEMORY PARTITION C UPPER 32 BITS

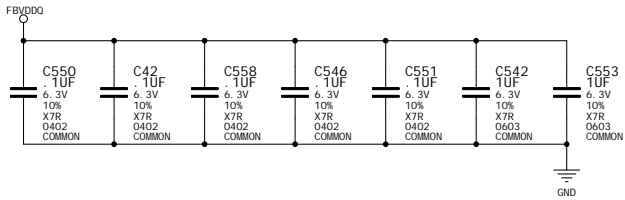


MII RROR MODE COMMAND MAPPING			2
	0-31	32-63	
CMD0	CKE_L	Not_Used	
CMD1	A8	A8	
CMD2	CS0_L*	Not_Used	
CMD3	A7	A6	
CMD4	A2	A1	
CMD5	A11	A9	
CMD6	A5	A4	
CMD7	A0	A12	
CMD8	CAS*	CAS*	
CMD9	BA1	A3	
CMD10	A9	A11	
CMD11	Not_Used	CS0_H*	
CMD12	BA0	BA0	
CMD13	BA2	A15	
CMD14	A3	BA1	
CMD15	Not_Used	CS1_H*	
CMD16	Not_Used	ODT_H	
CMD17	A4	A5	
CMD18	A13	A14	
CMD19	WE*	A10	
CMD20	A1	A2	
CMD21	A10	WE*	
CMD22	A12	A0	
CMD23	CS1_L*	Not_Used	
CMD24	RAS*	RAS*	
CMD25	ODT_L	Not_Used	
CMD26	A6	A7	
CMD27	Not_Used	CKE_H	
CMD28	RST	RST	
CMD29	A14	A13	
CMD30	A15	BA2	

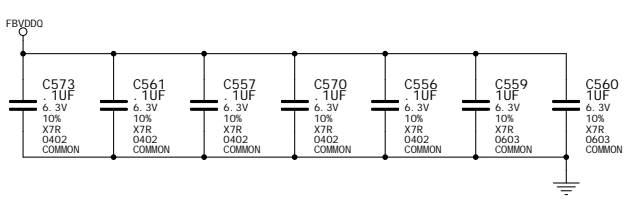


8. MEMORY DECOUPLING CAPS

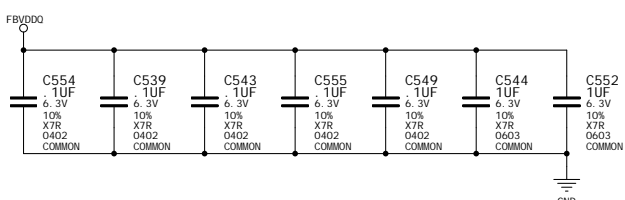
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 0-15



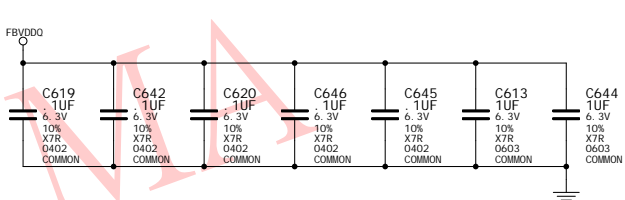
DECOUPLING CAPS FOR ONE MEMORY OF PARTION C LOWER BITS 0-15



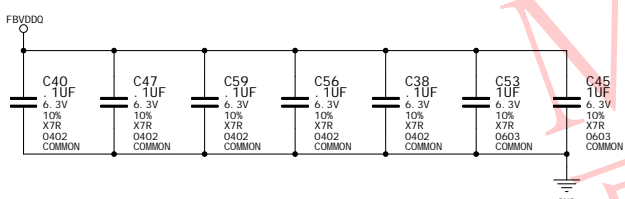
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 16-31



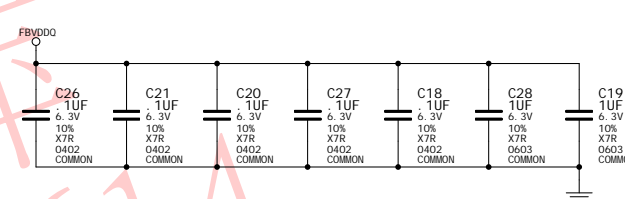
DECOUPLING CAPS FOR ONE MEMORY OF PARTION C LOWER BITS 16-31



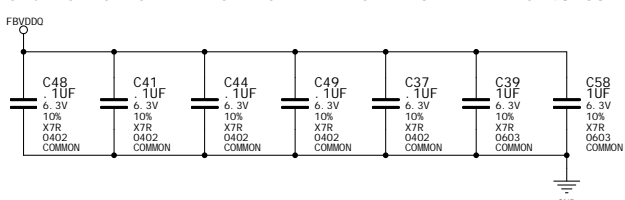
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 32-47



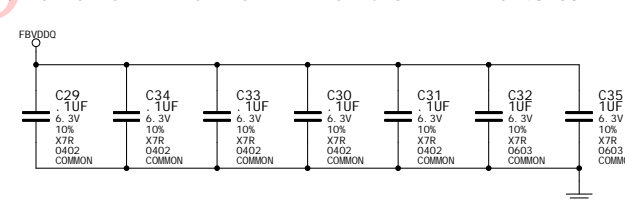
DECOUPLING CAPS FOR ONE MEMORY OF PARTION C UPPER BITS 32-47



DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 48-63



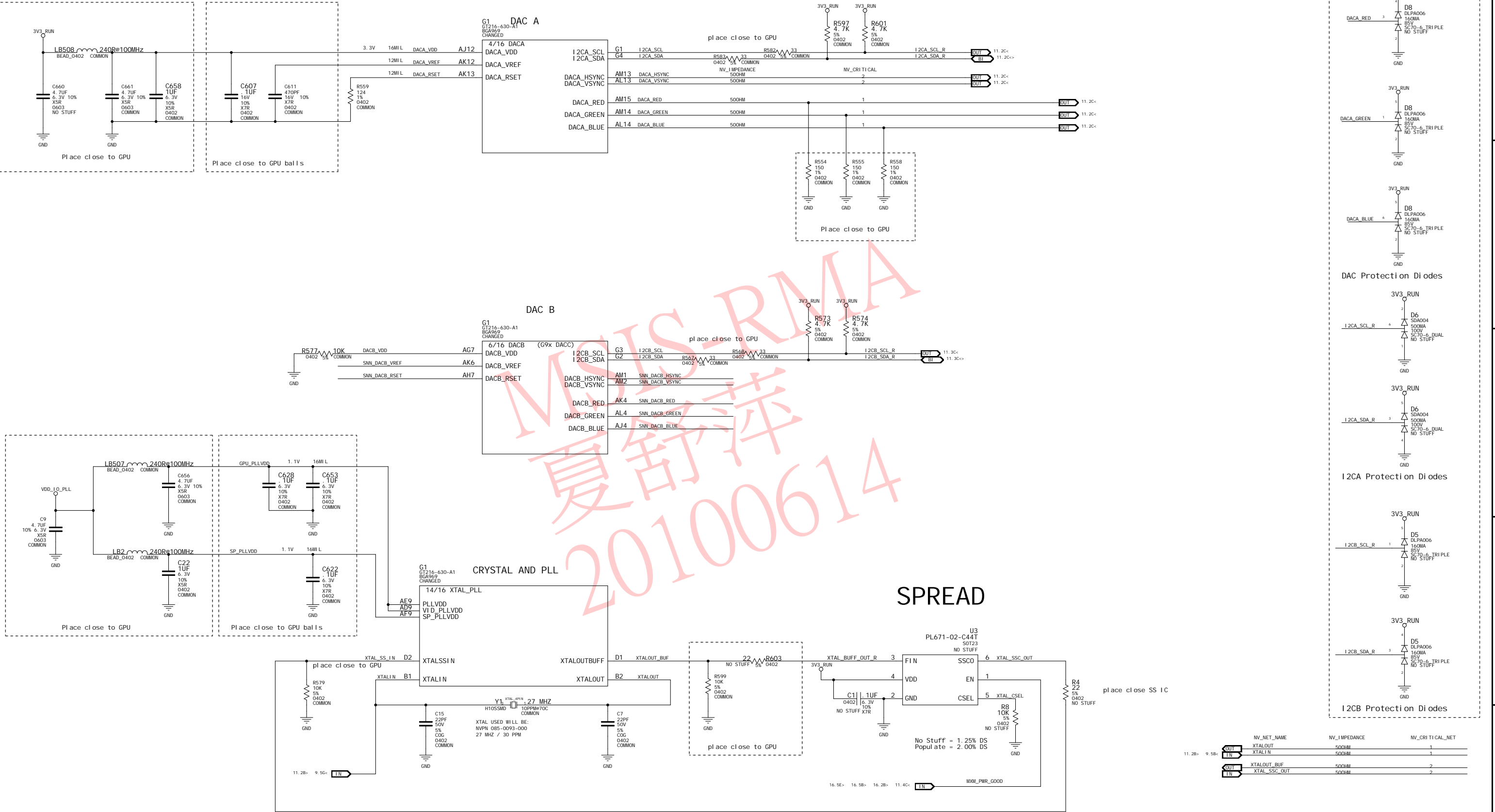
DECOUPLING CAPS FOR ONE MEMORY OF PARTION C UPPER BITS 48-63



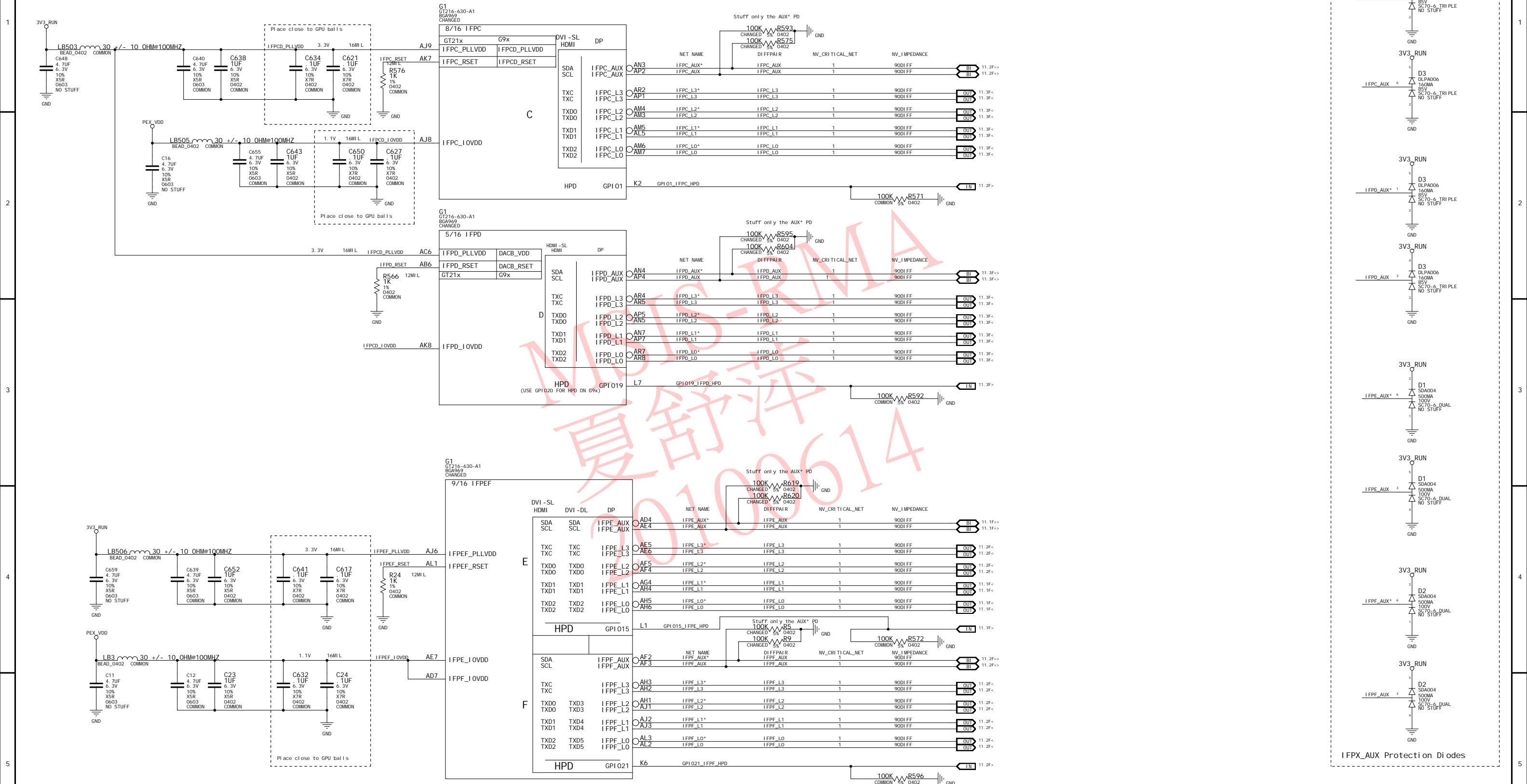
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.



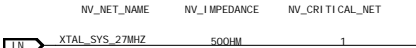
9. DAC\_A, DAC\_B, SPREAD, PLL, CRYSTAL



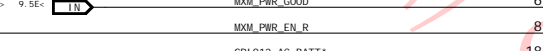
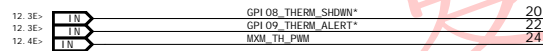
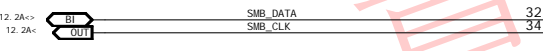
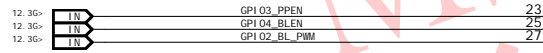
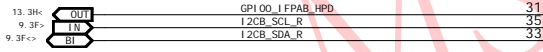
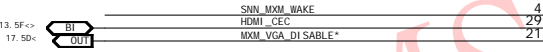
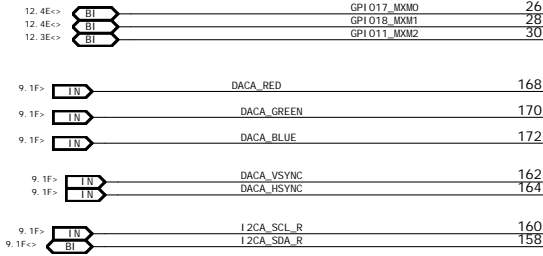
10. DP LINKS CD, LINK EF



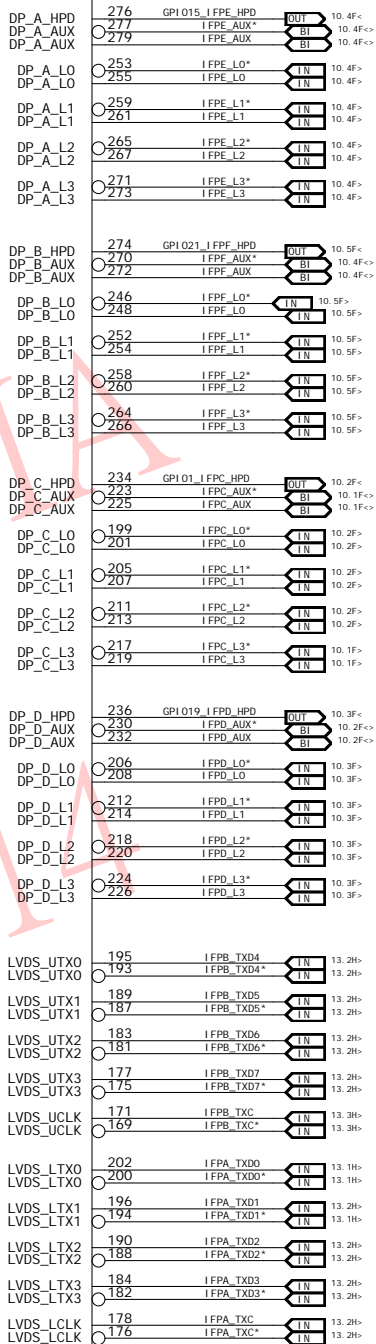
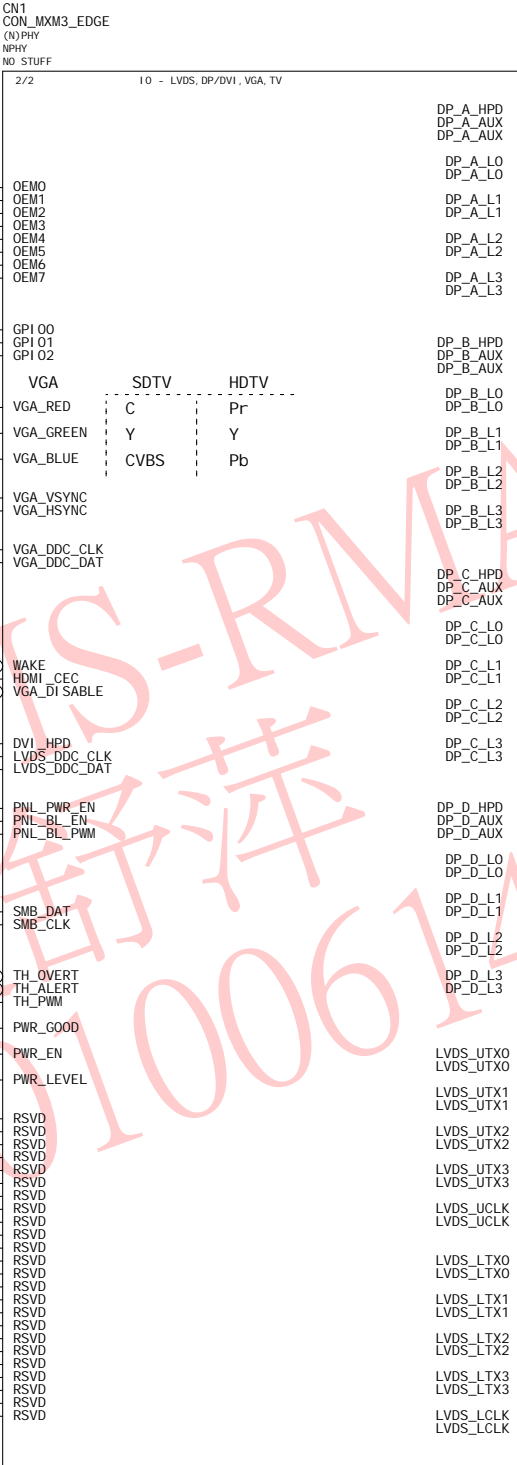
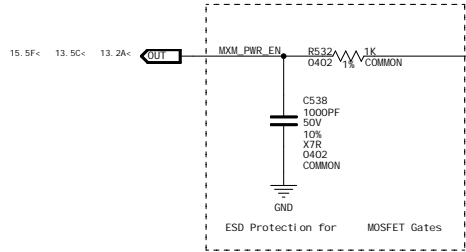
## 11. MXM CONNECTOR



SNN_MXM_OEM38	38
SNN_MXM_OEM39	39
SNN_MXM_OEM40	40
SNN_MXM_OEM41	41
SNN_MXM_OEM42	42
SNN_MXM_OEM43	43
SNN_MXM_OEM44	44
XTAL_SYS_27MHZ	45



Not for use with a compliant MXM 3.0 module  
Not for production (test only) no need for  
TP(s) on the resistro side



ASSEMBLY	P699-B00 SKU1 GT216-630 MXM3.0 TYPE-A 1024MB 8pcs 64Mx16
PAGE DETAIL	MXM Connector, 10-Section

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVI DI A CORPORATI ON

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

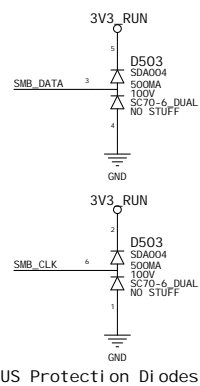
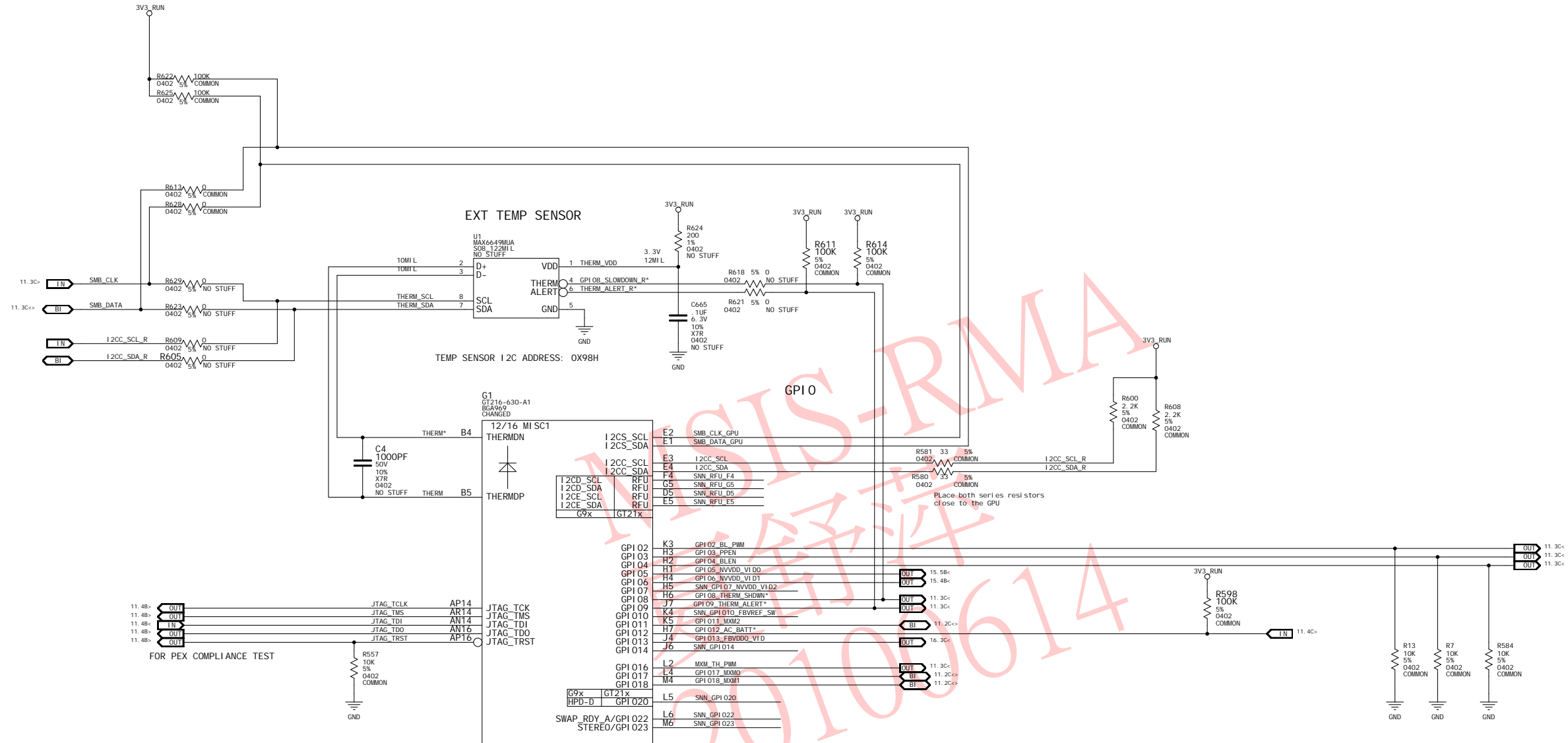
NV_PN	600-10699-0015-200 A
-------	----------------------

ID	p699	PAGE	11 OF 17
----	------	------	----------

NAME	si xu	DATE	08-JUL-2009
------	-------	------	-------------

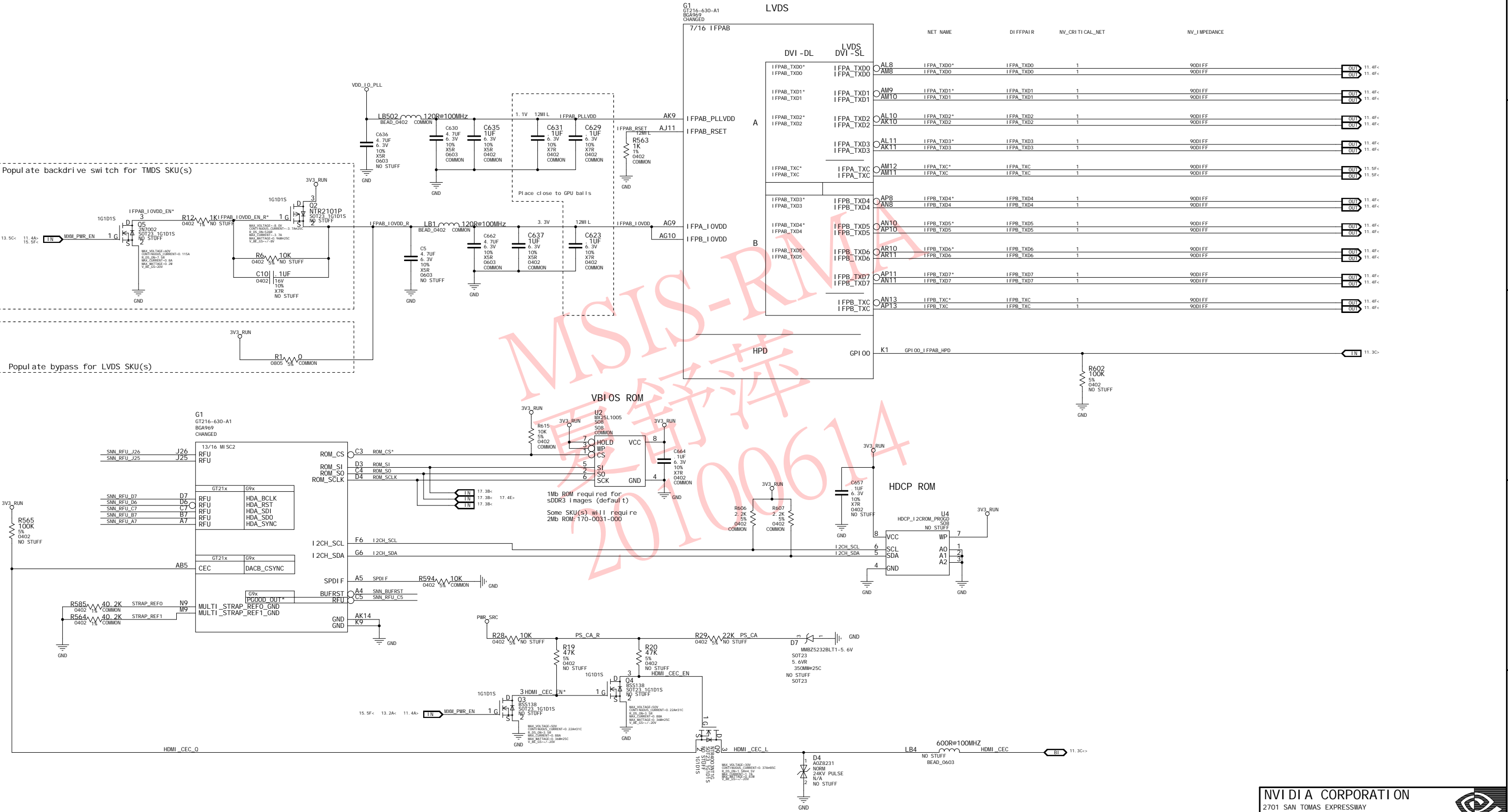


## 12. GPIO, JTAG, TEMP SENSOR

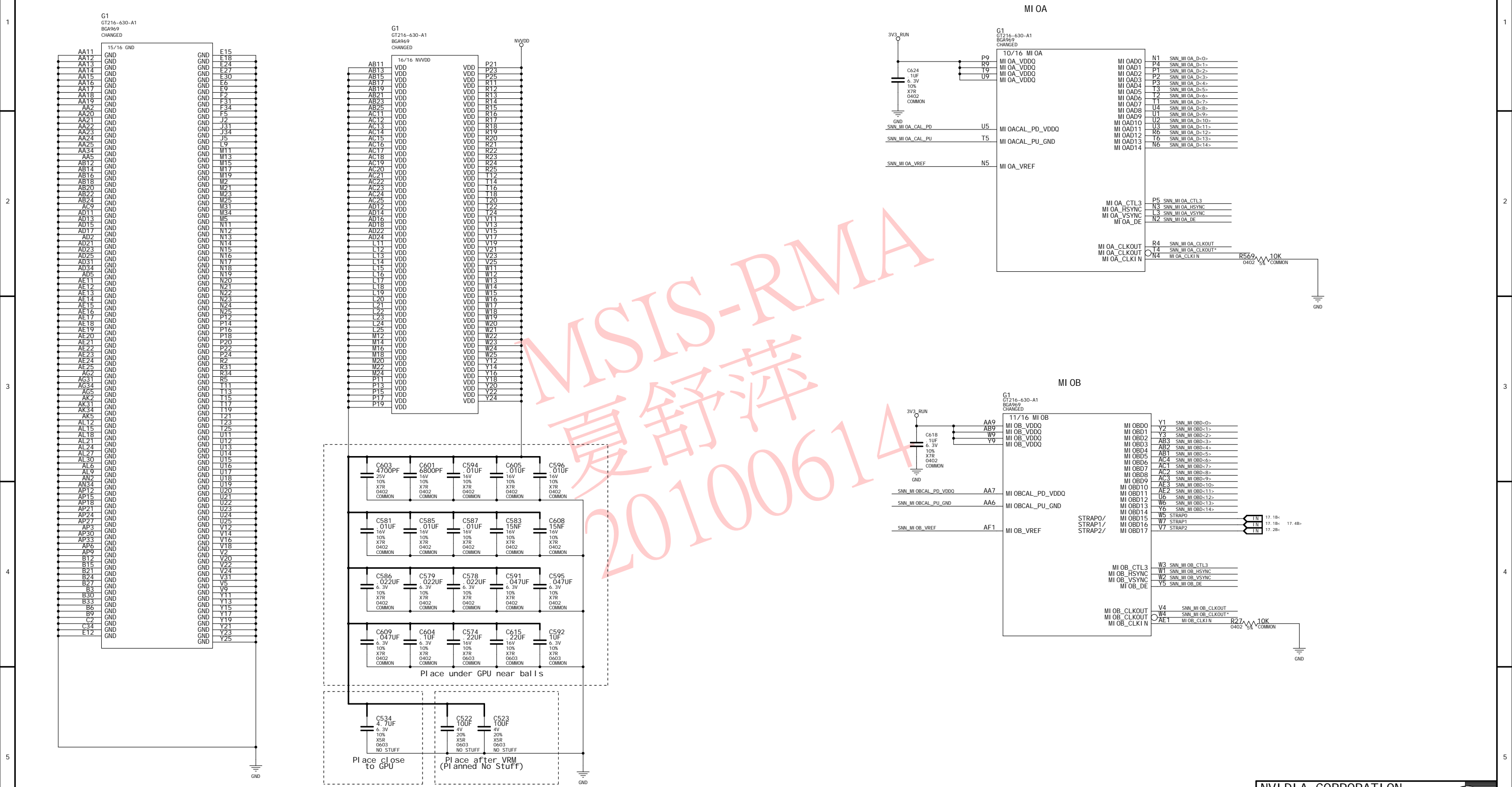




13. LVDS, VBI OS, HDCP ROM, CEC

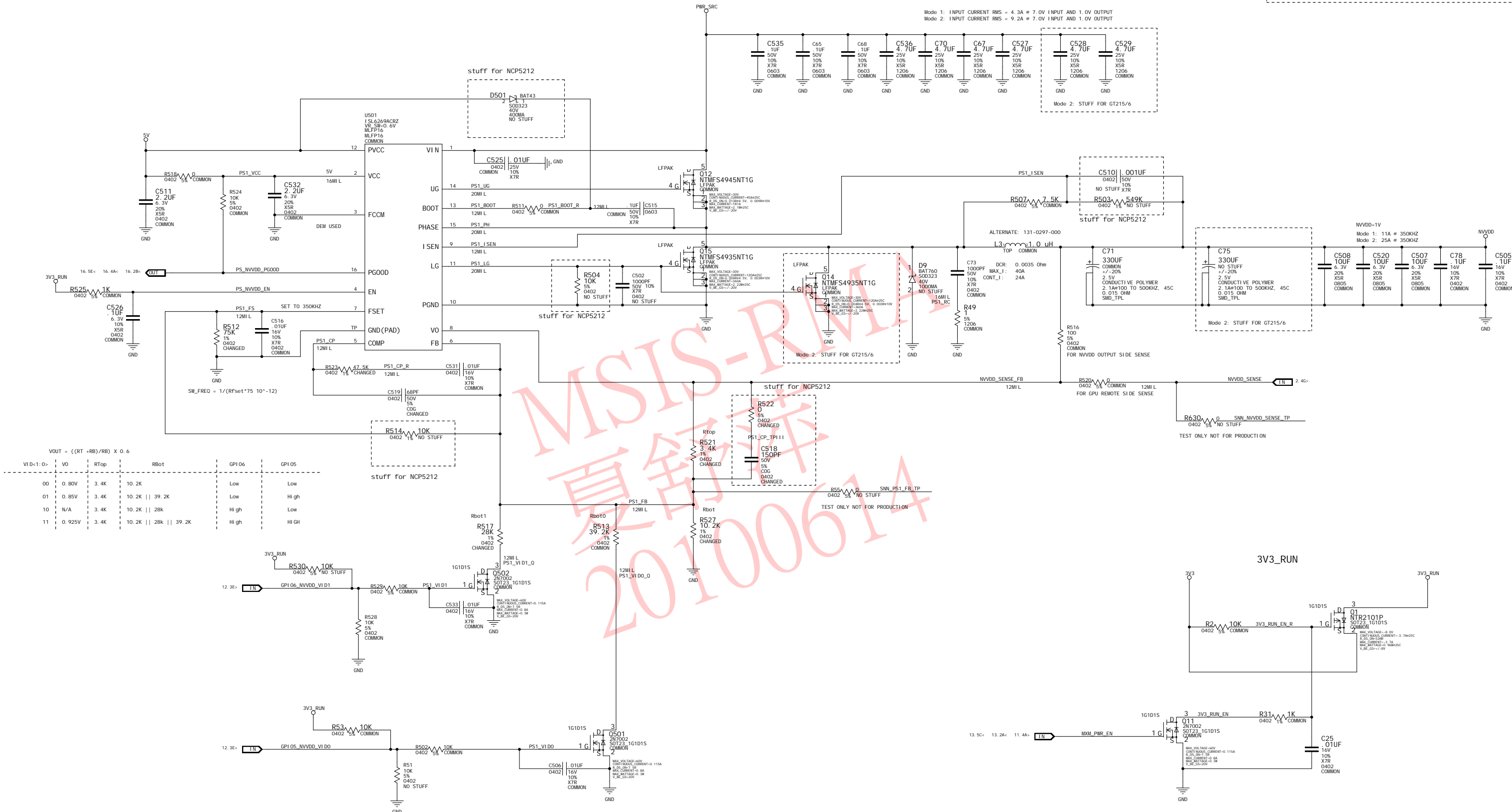


14. MI OA, MI OB, GPU VDD/DCPLNG/GND



## 15. NVVDD POWER SUPPLY AND 3V3\_RUN

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
NVVD0	NVDD	1V	20MIL
			30A



ASSEMBLY	P699-B00 SKU1 GT216-630 MXM3.0 TYPE-A 1024MB 8pcs 64Mx16
PAGE DETAIL	NVVD Power Supply and 3V3_RUN

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

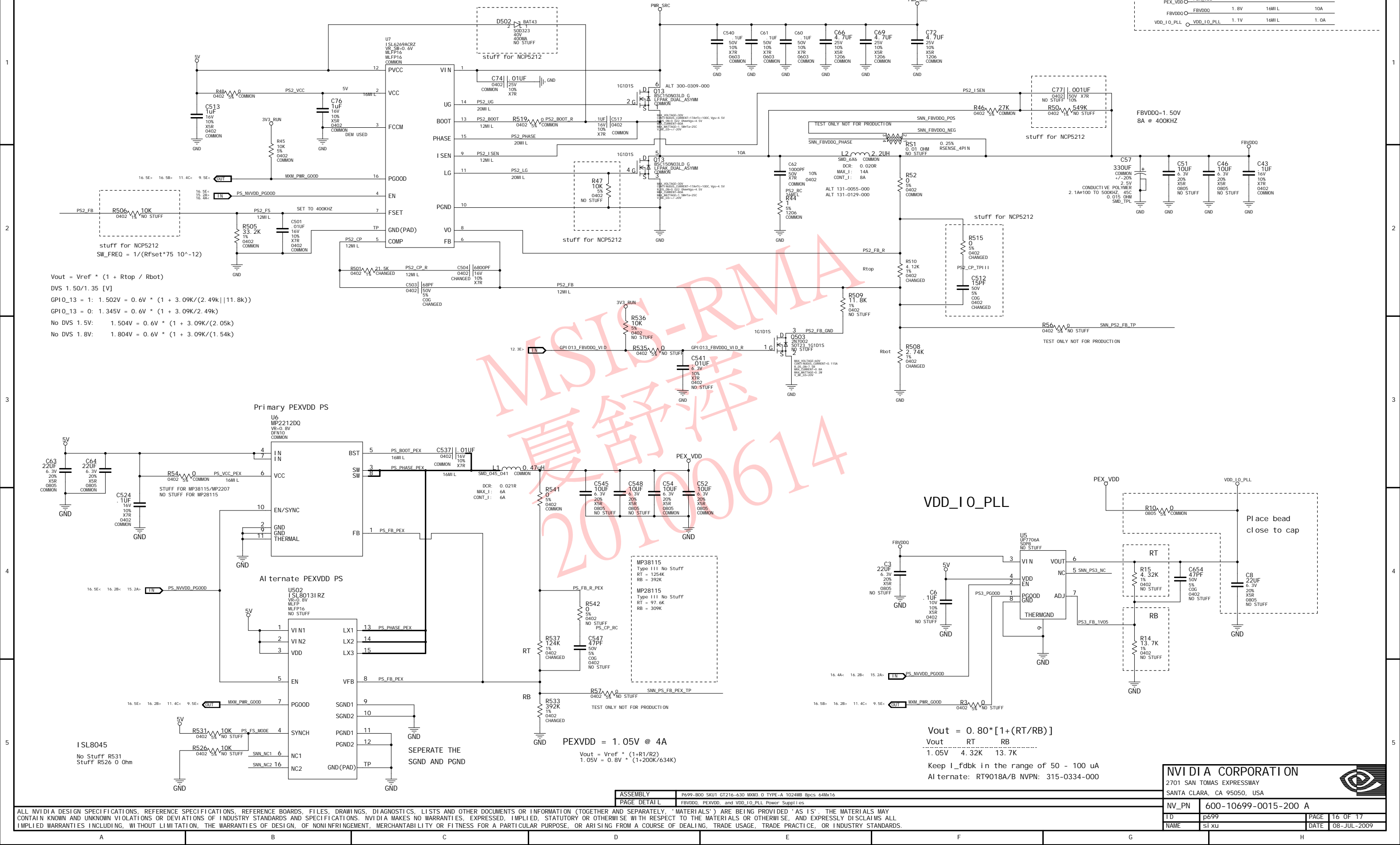
2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, US



NV_PN	600-10699-0015-200 A
-------	----------------------

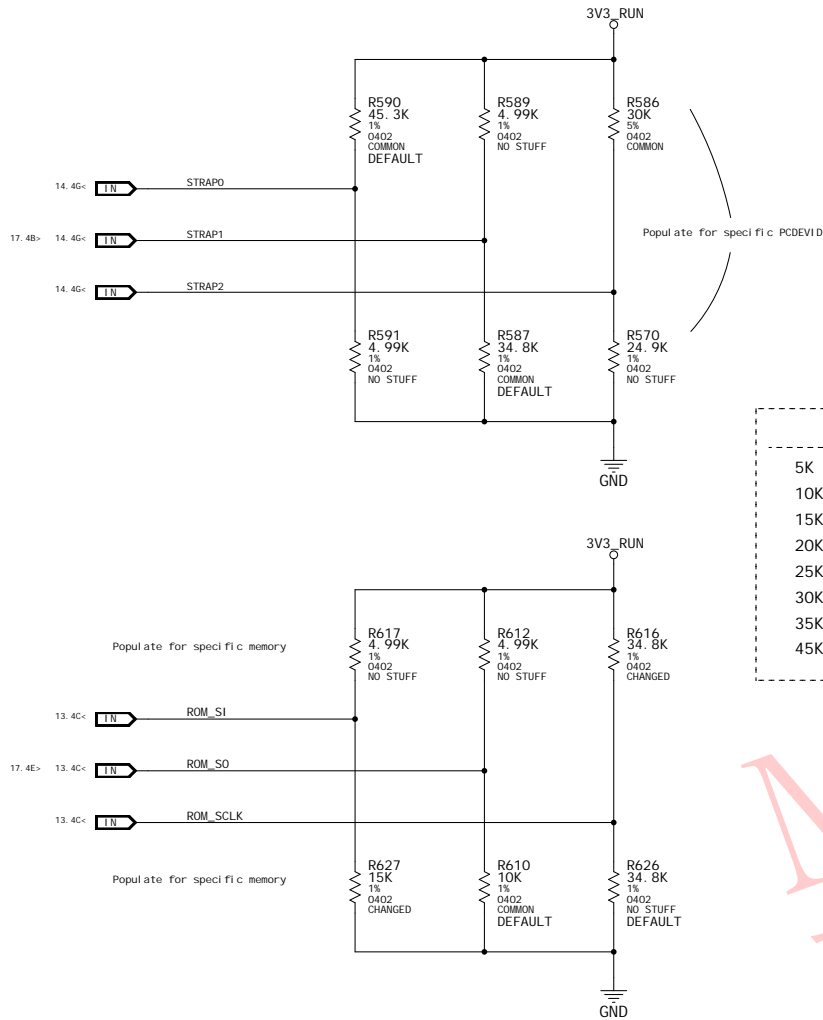
ID	p699	PAGE	15 OF 17
NAME	si xu	DATE	08-JUL-20

16. FBVDDQ, PEXVDD, AND VDD\_I O\_PLL POWER SUPPLIES





17. STRAPS, MOUNTING HOLES



	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111

STRAP0

STRAP1

STRAP2

ROM\_SO

ROM\_SI

ROM\_SCLK

USER\_BI T0

USER\_BI T1

USER\_BI T2

USER\_BI T3

Default t All SKU(s):

0xF = 45K PU

LVDS Panel EDID Mode

3GIO\_PADCFG\_LUT\_ADRO

3GIO\_PADCFG\_LUT\_ADR1

3GIO\_PADCFG\_LUT\_ADR2

3GIO\_PADCFG\_LUT\_ADR3

Set at HW reset by the PEX\_PADCFG Circuit

0x0: Desktop default t (normal swing) - 5k PD

0x6: Mobile default t (low swing) - 35k PD

PCI\_DEVID\_0

PCI\_DEVID\_1

PCI\_DEVID\_2

PCI\_DEVID\_3

PCDEVID\_3:0] Definitions (Note Actual DEVID set also depends on PCI\_DEVID\_4 )

	GT218	GT216	GT215
1000	5K PU	GT218-700	1000 5K PU GT216-600
0100	25K PD	GT218-730	0100 25K PD GT216-630
1100	25K PD		1100 25K PD GT216-640
			1100 25K PD GT216-950

VGA\_DEVICE

0: 3D DEVICE

Set at HW reset by the Device Detect Circuit

1: VGA DEVICE

SMB\_ALT\_ADDR

0: Thermal Sensor ADR = 0x9E

0x1 = 10K PD

FB\_O\_BAR\_SIZE

0: Default t

XCLK\_417

0: Default t

RAM\_CFG[3:0] Definitions

	GT218 64Mx16	GT215/6
0000	5K PD Reserved	0001 64Mx16 128-bit t 10K PD Qimonda
0001	10K PD Qimonda	0010 64Mx16 128-bit t 15K PD Hynix
0010	15K PD Hynix	0011 64Mx16 128-bit t 20K PD Samsung
0011	20K PD Samsung	0100 Reserved
		0101 32Mx16 128-bit t 30K PD Qimonda
0100	25K PD Reserved	0110 32Mx16 128-bit t 35K PD Hynix
0101	30K PD Qimonda	0111 32Mx16 128-bit t 45K PD Samsung
0110	35K PD Hynix	
0111	45K PD Samsung	

\* 32Mx16 MAY BE 64Mx16 run at 1/2 density

PEX\_PLL\_EN\_TERM100

0: DISABLED

SLOT\_CLK\_CONFIG

1: GPU and MCH COMMON REFCLK

0x6 = 35K PD PCDEVID\_EXT=0

SUB\_VENDOR

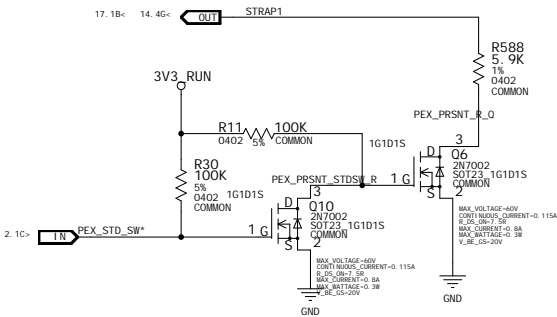
1: VBIOS ROM IS PRESENT

0xE = 35K PU PCDEVID\_EXT=1

PCI\_DEVID\_EXT

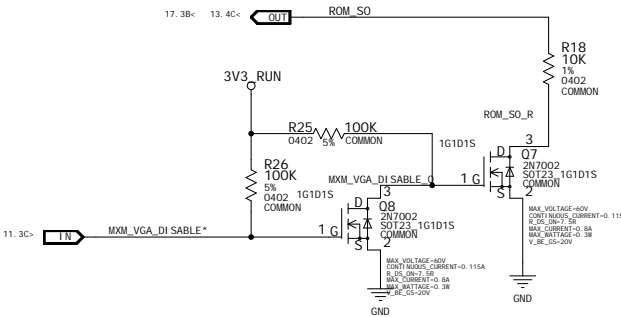
0: PCDEVID[4] = 0 or 1 (SKU Specific)

PEX\_PADCFG DETECT

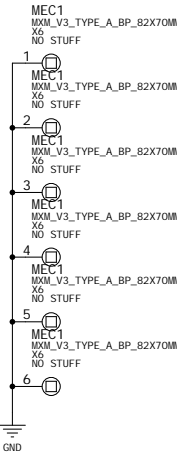


PEX_PRSTNSTD SW*	R_STRAP1	3_GIO_PADCFG_LUT<3..0>
FLOAT	35k	0x6 MOBILE_DEFAULT
GND	5k (35k    5.9k)	0x0 DESKTOP_DEFAULT

DEVICE DETECT



VGA_DISABLE#	R_ROM_SO	MODE
FLOAT	10k	0x1 VGA MODE
GND	5k (10k    10k)	0x0 3D ACCELERATOR



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA



NV\_PN 600-10699-0015-200 A

ID p699 PAGE 17 OF 17

NAME S1XU DATE 08-JUL-2009

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.