P1041-B01 GF104

GF104-300, 768MB/1536MB, GDDR5 192b 32M/64Mx32
DVI-I-DL, DVI-I-DL/DP, mHDMI

Table of Contents:

變更記錄

P3，C55 change to 1206 10u
P4~P14，add 跳頁&'<>'符號
P14,刪除所有網絡線
P17，add 6262 IC
P25,刪除原公版U2 & J501. 把I2CC接到6262IC
P27,接PS1_1V05_FB到6262,U4 foot_print 改為十字的
P28,改U8的FB接法，換L6為L04-22A8011-L65
P29，core部份PWM換UP6213+6284，OFS電壓開關抬50mV。頻率def400KHz，開關抬到600KHz.
P30-31，加driver IC 6284；去掉3顆input 電容；同時增加6個LED燈，增加CP1~CP12；為精簡線路，刪除L mos端與DRVL 0OHm電阻，刪除CSP，CSN 0Ω電阻；更換MOS & 電感；power前4相由PEX6_F1提供，后2相由PEX6_F2提供；電容部份保留公版。
P32,去除input 端12V 的LB電感
P33,加防彎條mec100，加6個十字光學點，加NVVDD，FBVDD &pex_vdd的測試點, 增加阻抗條

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11041-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-11041-0000-300	P1041 GF104-300 768MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
2	SKU0010	600-11041-0010-300	P1041 GF104-350 1024MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
3	QS1	600-11041-0000-QS1	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

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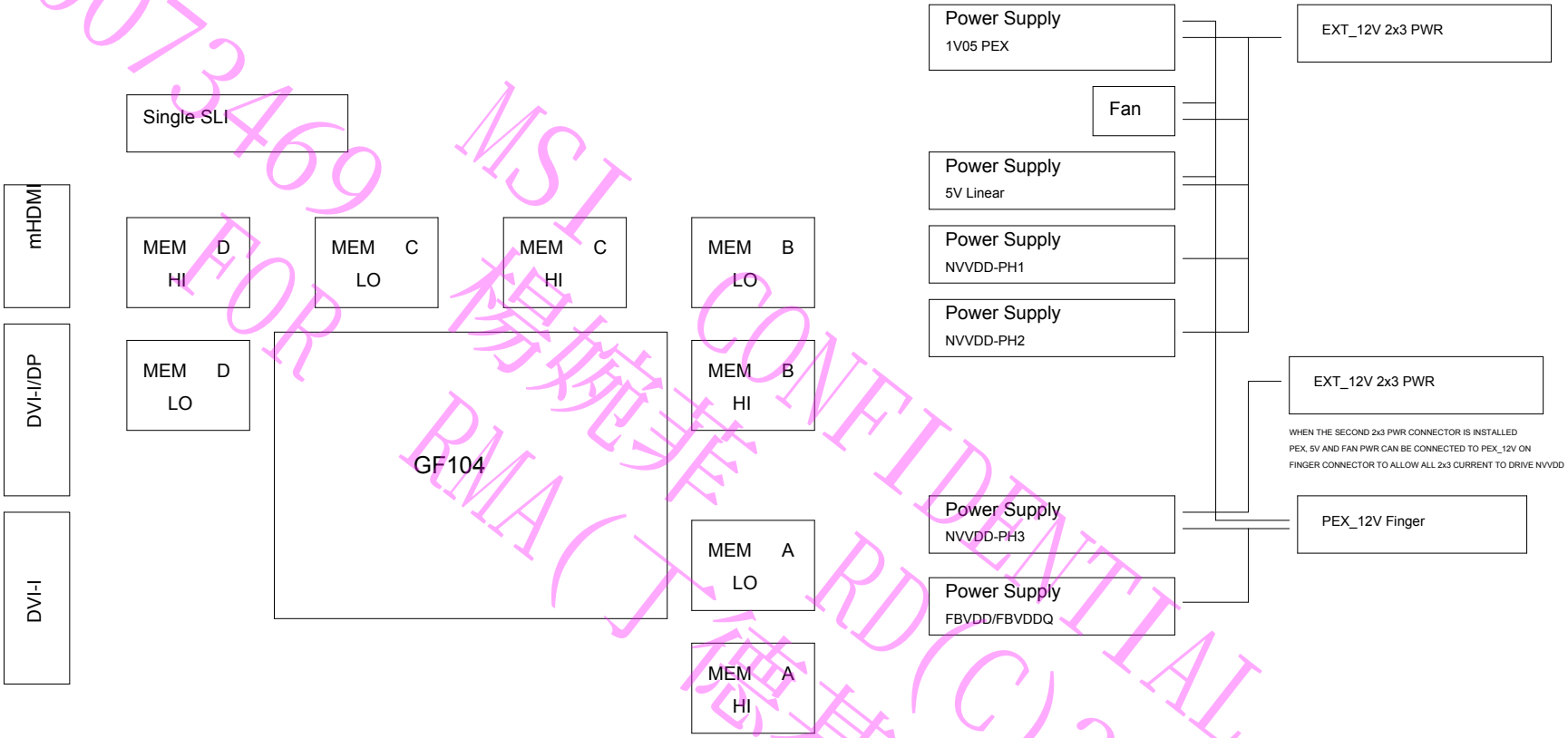
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-BASE-000		
PCB REV	P1041-B01	PAGE	
BOM REV	A	DATE	12-MAY-2010

Page2: Block Diagram



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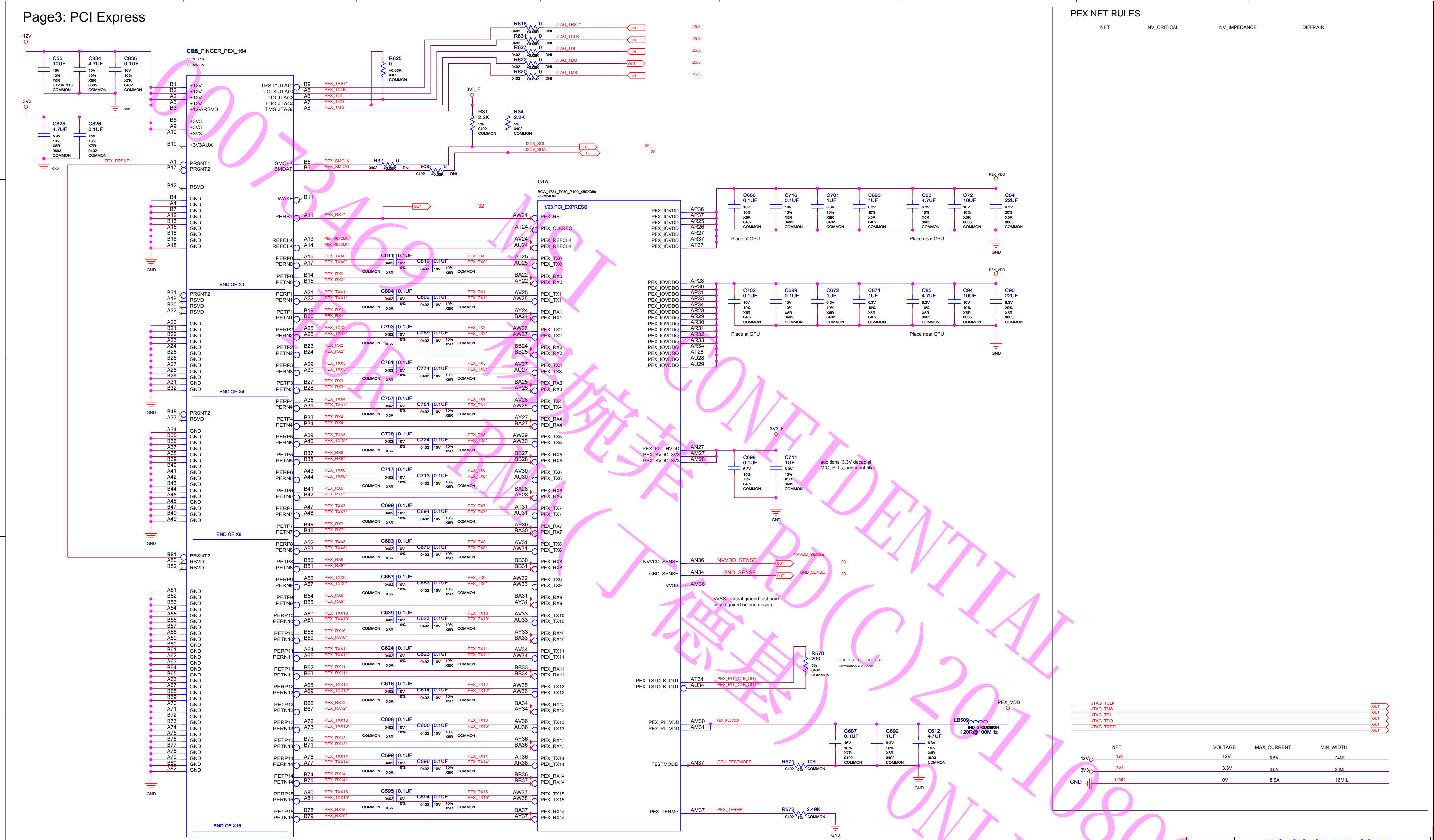
Page3: PCI Express



12V
3V3
C55 10UF
C834 4.7UF
C835 0.1UF
C825 4.7UF
C826 0.1UF
CON_FINGER_PEX_164
CON_X16
COMMON
+12V
+12V/RSVD
+3V3
+3V3AUX
PRSNT1
PRSNT2
RSVD
GND
END OF X1
END OF X4
END OF X8
END OF X16
TRST* JTAG1
TCLK JTAG2
TDI JTAG3
TDO JTAG4
TMS JTAG5
SMCLK
SMDAT
WAKE
PERST
REFCLK
R616 0
R631 0
R627 0
R622 0
R620 0
JTAG_TRST*
JTAG_TCLK
JTAG_TDI
JTAG_TDO
JTAG_TMS
R625 0
3V3_F
R31 2.2K
R34 2.2K
I2CS_SCL
I2CS_SDA
R32 0
R35 0
G1A
BGA_1731_P080_P100_450X350
1/23 PCI_EXPRESS
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_IOVDD
PEX_IOVDDQ
PEX_VDD
Place at GPU
Place near GPU
PEX_PLL_HVDD
PEX_SVDD_3V3
additional 3.3V decap at MIO, PLLs, and input filter
NVVDD_SENSE
GND_SENSE
VVSS
VVSS - virtual ground test point only required on one design
R570 200
PEX_TEST_PLL_CLK_OUT
Termination = 200ohm
PEX_TSTCLK_OUT
PEX_PLLVDD
LB500
120R@100MHz
C687 0.1UF
C692 1UF
C612 4.7UF
TESTMODE
GPU_TESTMODE
R571 10K
PEX_TERMP
R572 2.49K
PEX NET RULES
NET
NV_CRITICAL
NV_IMPEDANCE
DIFFPAIR
NET
VOLTAGE
MAX_CURRENT
MIN_WIDTH
12V 12V 5.5A 24MIL
3V3 3.3V 3.0A 20MIL
GND 0V 8.5A 16MIL

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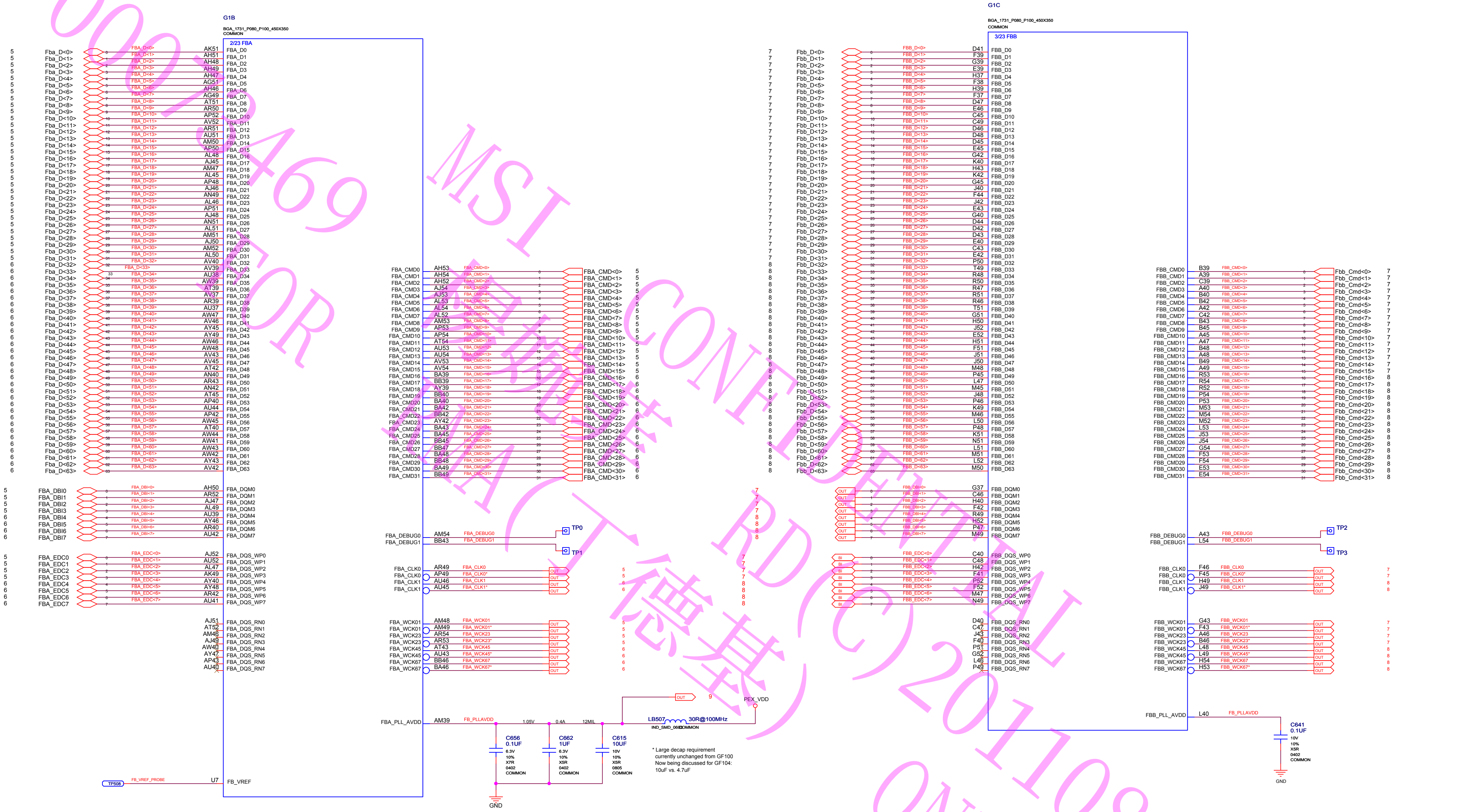
Page4: GPU Partition A/B



G1B
BGA_1731_P080_P100_450X350
COMMON
2/23 FBA
FBA_D0 … FBA_D63
FBA_CMD0 … FBA_CMD31
FBA_DQM0 … FBA_DQM7
FBA_DQS_WP0 … FBA_DQS_WP7
FBA_DQS_RN0 … FBA_DQS_RN7
FBA_DEBUG0
FBA_DEBUG1
TP0
TP1
FBA_CLK0
FBA_CLK1
FBA_WCK01
FBA_WCK23
FBA_WCK45
FBA_WCK67
FBA_PLL_AVDD
FB_VREF
TP508
FB_VREF_PROBE
C656 0.1UF
C662 1UF
C615 10UF
GND
LB507 30R@100MHz
PEX_VDD
* Large decap requirement currently unchanged from GF100 Now being discussed for GF104: 10uF vs. 4.7uF
G1C
BGA_1731_P080_P100_450X350
COMMON
3/23 FBB
FBB_D0 … FBB_D63
FBB_CMD0 … FBB_CMD31
FBB_DQM0 … FBB_DQM7
FBB_DQS_WP0 … FBB_DQS_WP7
FBB_DQS_RN0 … FBB_DQS_RN7
FBB_DEBUG0
FBB_DEBUG1
TP2
TP3
FBB_CLK0
FBB_CLK1
FBB_WCK01
FBB_WCK23
FBB_WCK45
FBB_WCK67
FBB_PLL_AVDD
C641 0.1UF
GND

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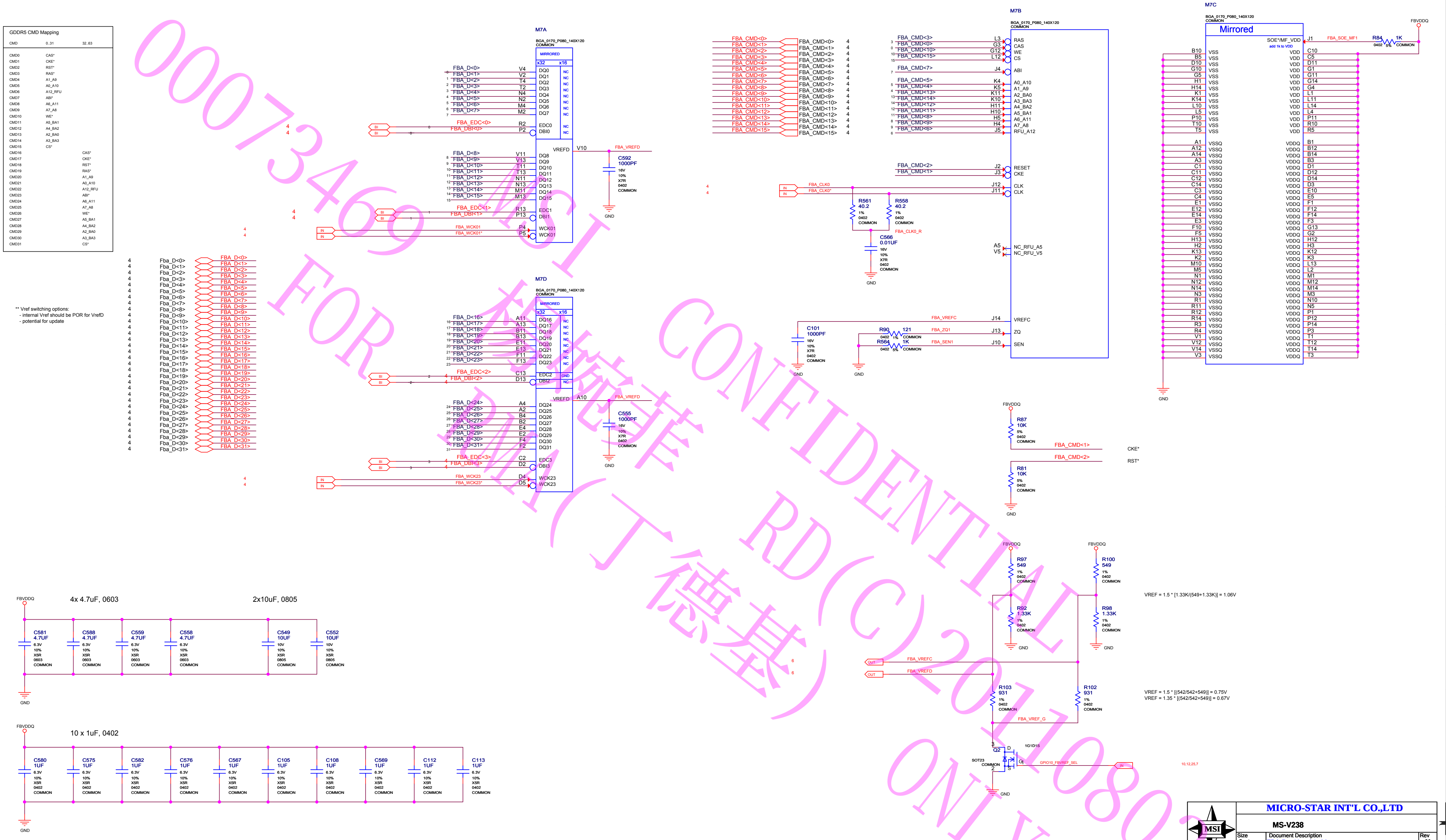
Page5: FBA Partition 31..0

GDDR5 CMD Mapping

CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update



M7A
BGA_0170_P080_140X120 COMMON
MIRRORED
M7B
M7C
Mirrored
M7D
FBA_D<0> … FBA_D<31>
FBA_CMD<0> … FBA_CMD<15>
FBA_EDC<0> FBA_EDC<1> FBA_EDC<2> FBA_EDC<3>
FBA_DBI<0> FBA_DBI<1> FBA_DBI<2> FBA_DBI<3>
FBA_WCK01 FBA_WCK01*
FBA_WCK23 FBA_WCK23*
FBA_VREFD
FBA_VREFC
FBA_CLK0 FBA_CLK0*
FBA_ZQ1
FBA_SEN1
C592 1000PF
C555 1000PF
C566 0.01UF
C101 1000PF
R561 40.2
R558 40.2
R90 121
R564 1K
R84 1K
R87 10K
R81 10K
CKE*
RST*
R97 549
R100 549
R92 1.33K
R98 1.33K
R103 931
R102 931
VREF = 1.5 * [1.33K/(549+1.33K)] = 1.06V
VREF = 1.5 * [(542/542+549)] = 0.75V
VREF = 1.35 * [(542/542+549)] = 0.67V
FBA_VREF_G
Q2
GPIO10_FBVREF_SEL
10,12,25,7
FBVDDQ
GND
4x 4.7uF, 0603
2x10uF, 0805
10 x 1uF, 0402
C581 4.7UF
C588 4.7UF
C559 4.7UF
C558 4.7UF
C549 10UF
C552 10UF
C580 1UF
C575 1UF
C582 1UF
C576 1UF
C567 1UF
C105 1UF
C108 1UF
C569 1UF
C112 1UF
C113 1UF

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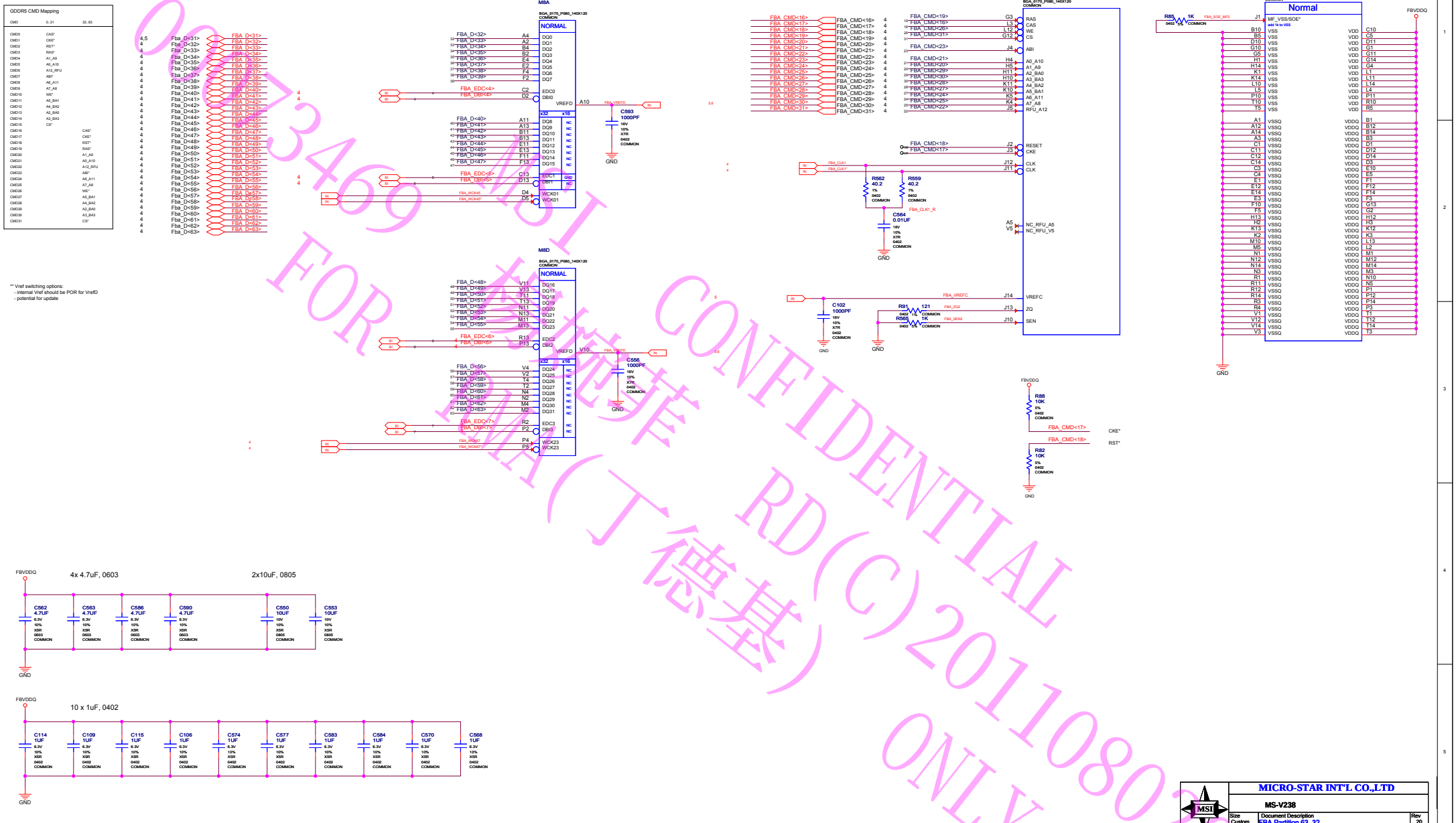
Page6: FBA Partition 63..32



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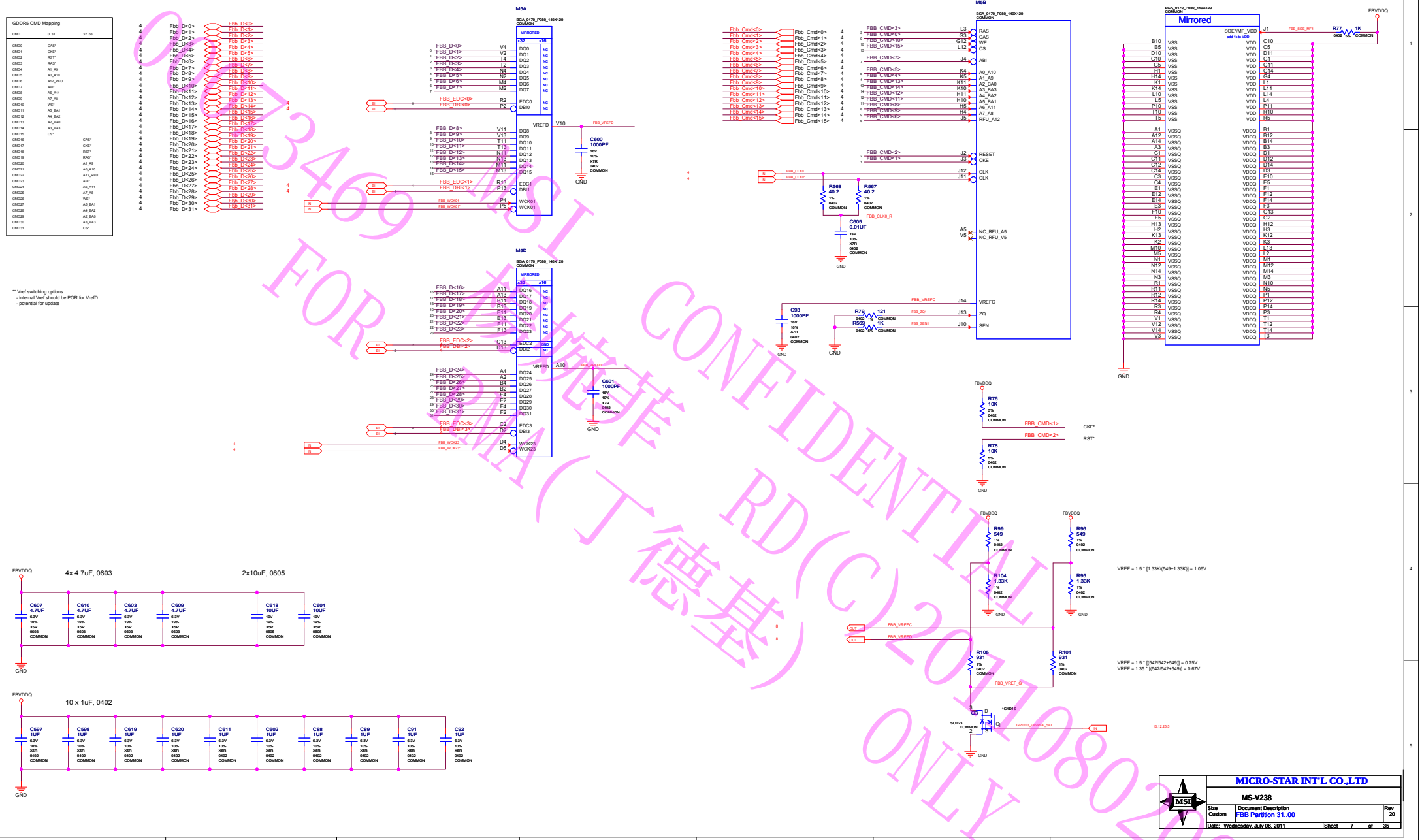
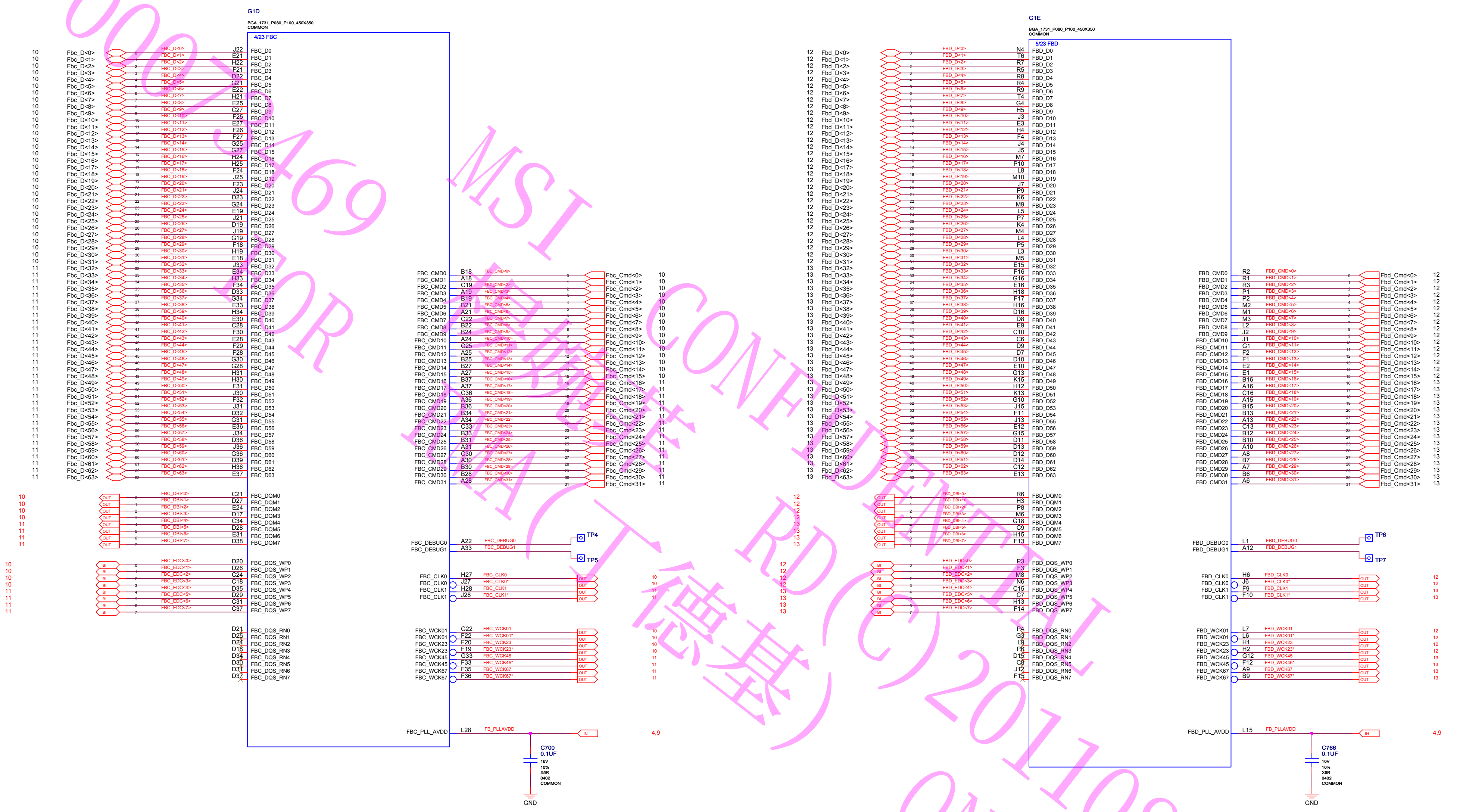
Page7: FBB Partition 31..0



Page8: FBB Partition 63..32

Page9: GPU Partition C/D



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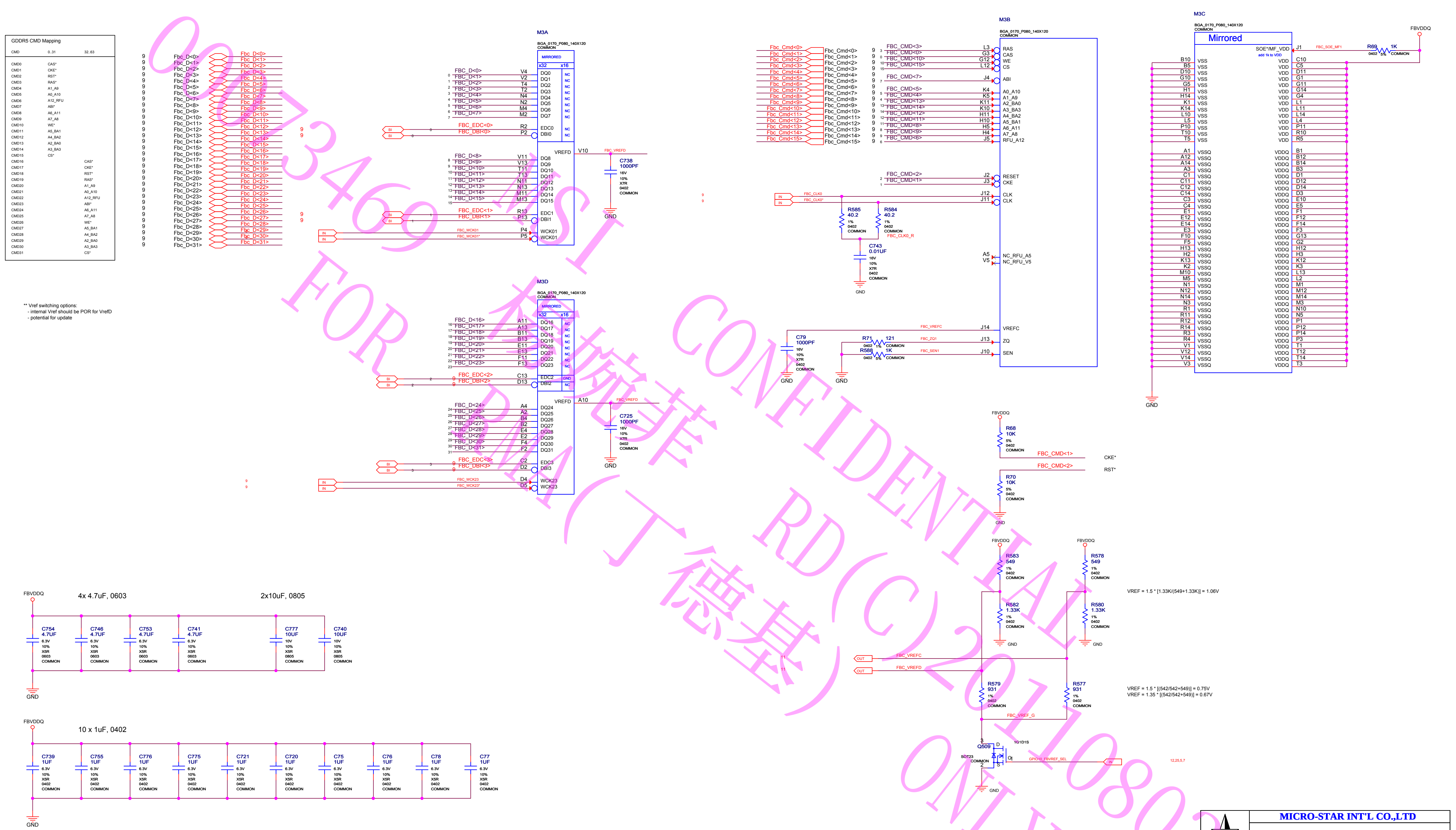
Page10: FBC Partition 31..0



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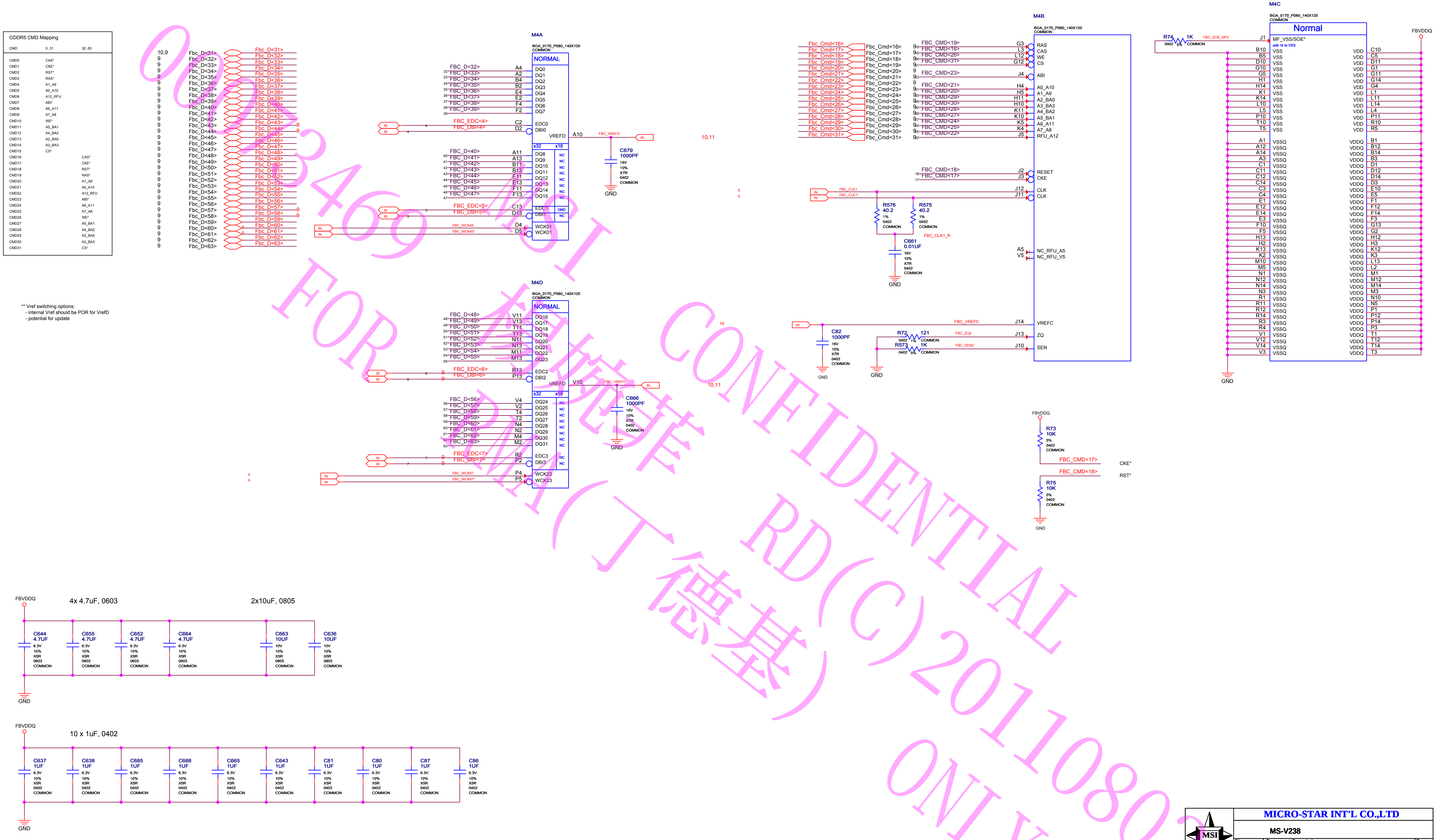
Page11: FBC Partition 63..32



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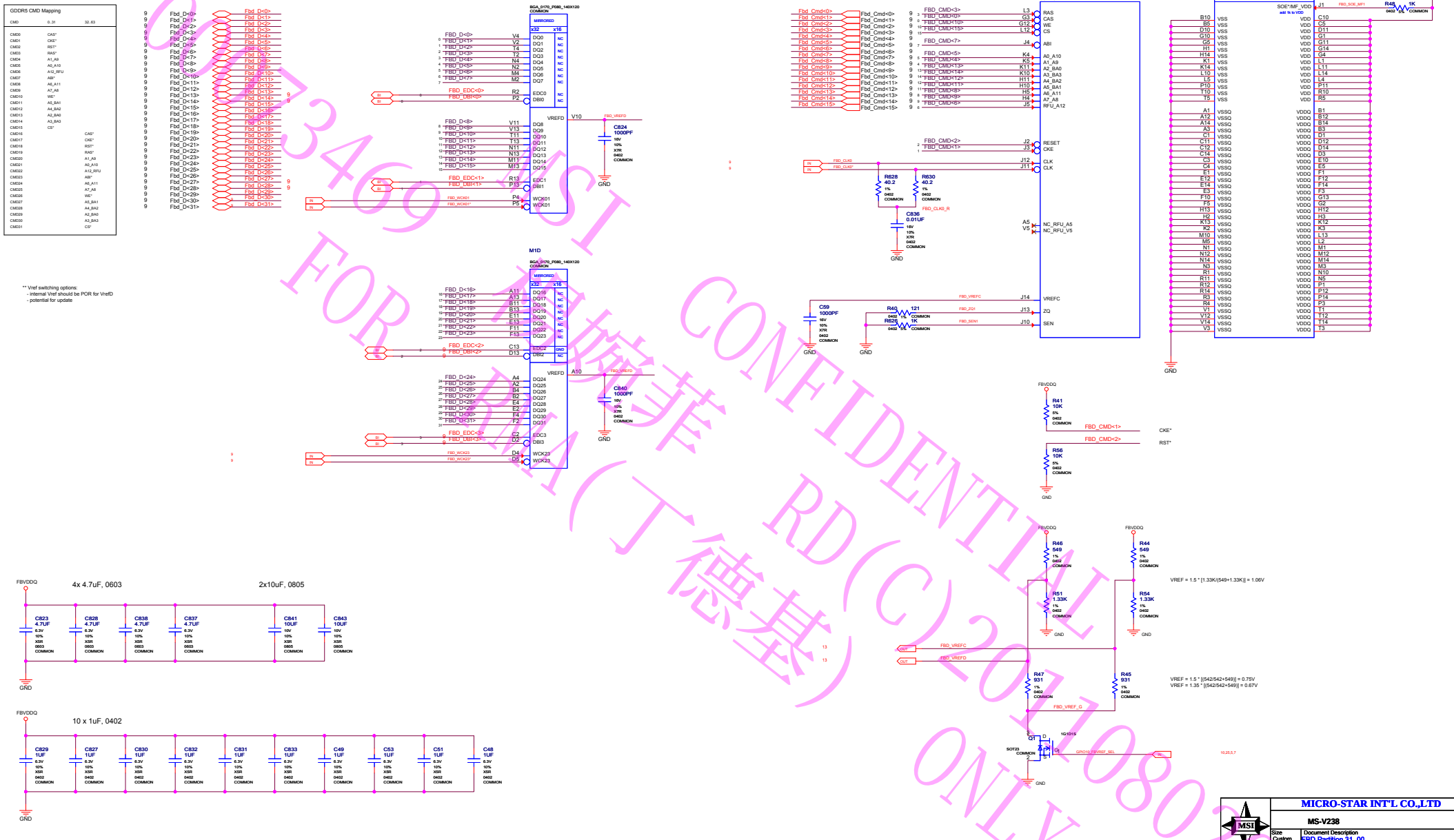
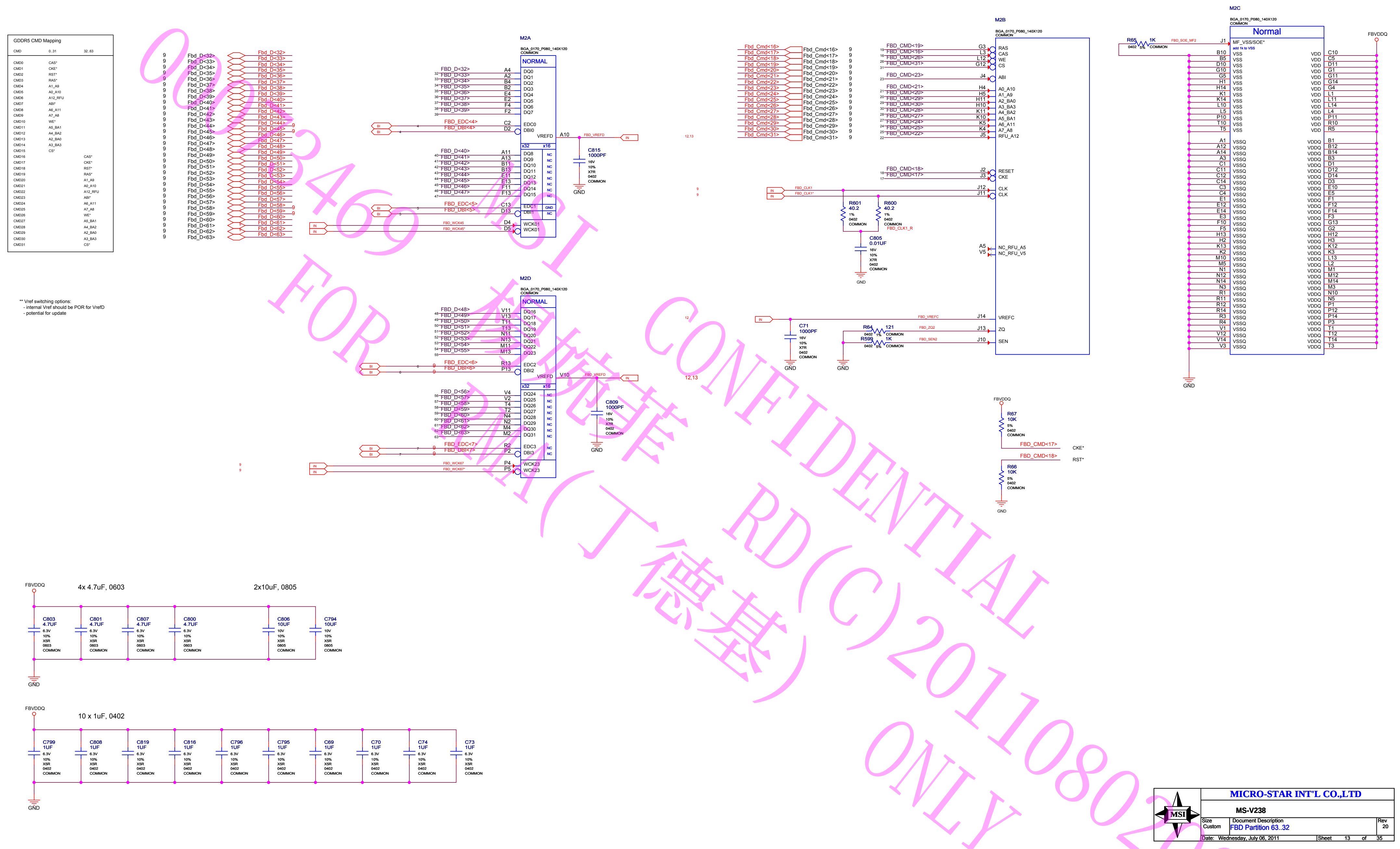
Page12: FBD Partition 31..0



Page13: FBD Partition 63..32



GDDR5 CMD Mapping
CMD 0..31 32..63
** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update
M2A
BGA_0170_P080_140X120
COMMON
NORMAL
M2D
M2B
M2C
Normal
FBVDDQ
GND
4x 4.7uF, 0603
2x10uF, 0805
10 x 1uF, 0402
C803 4.7UF
C801 4.7UF
C807 4.7UF
C800 4.7UF
C806 10UF
C794 10UF
C799 1UF
C808 1UF
C819 1UF
C816 1UF
C796 1UF
C795 1UF
C69 1UF
C70 1UF
C74 1UF
C73 1UF
C815 1000PF
C809 1000PF
C805 0.01UF
C71 1000PF
R601 40.2
R600 40.2
R64 121
R599 1K
R65 1K
R67 10K
R66 10K
FBD_CMD<17> CKE*
FBD_CMD<18> RST*
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Page14: FB Net Properties

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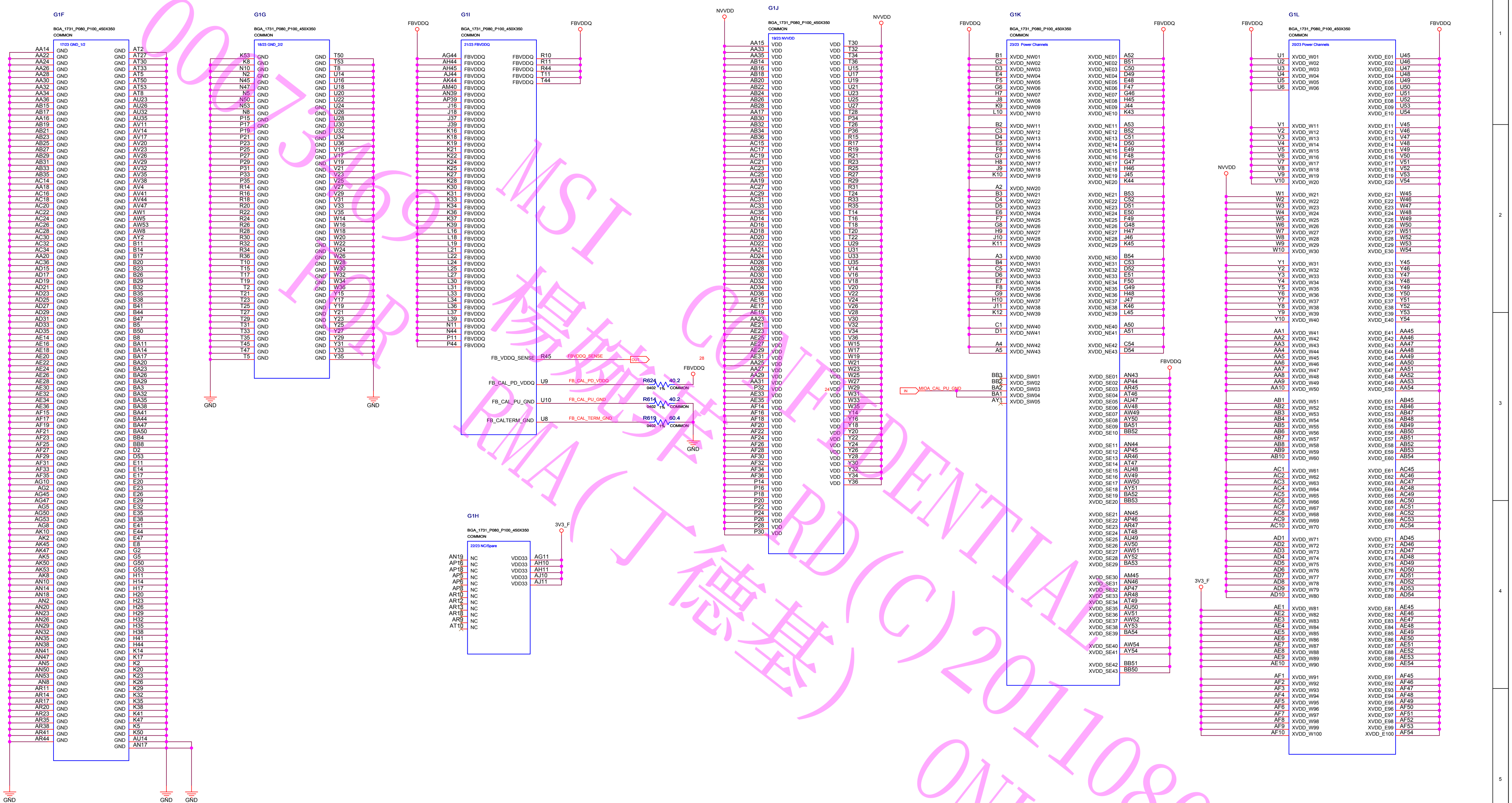
Page15: GPU PWR and GND

** Power channels are configurable.
XVDD_* pins are not connected on the substrate.
Therefore, XVDD_* pins can be assigned as needed.



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Page16: GPU Decoupling

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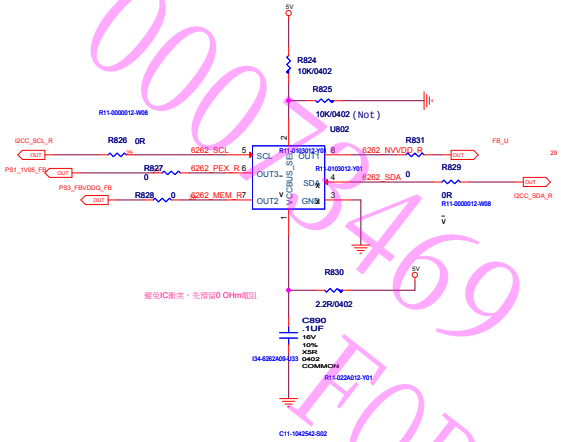
Page17: 6262



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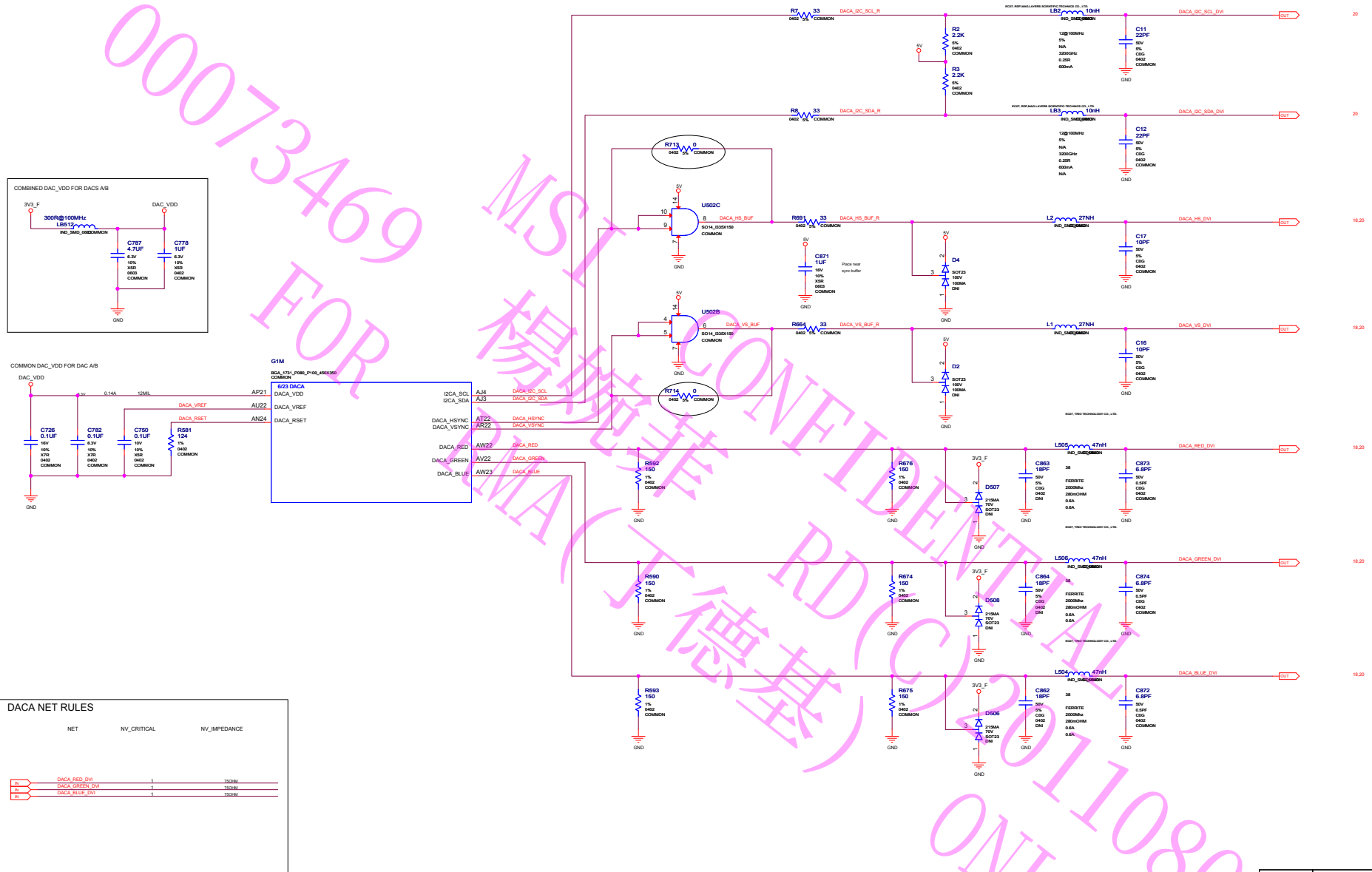
Page18: DACA (South)



DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE
DACA_RED_DVI	1	75OHM
DACA_GREEN_DVI	1	75OHM
DACA_BLUE_DVI	1	75OHM
DACA_HS_DVI	2	50OHM
DACA_VS_DVI	2	50OHM

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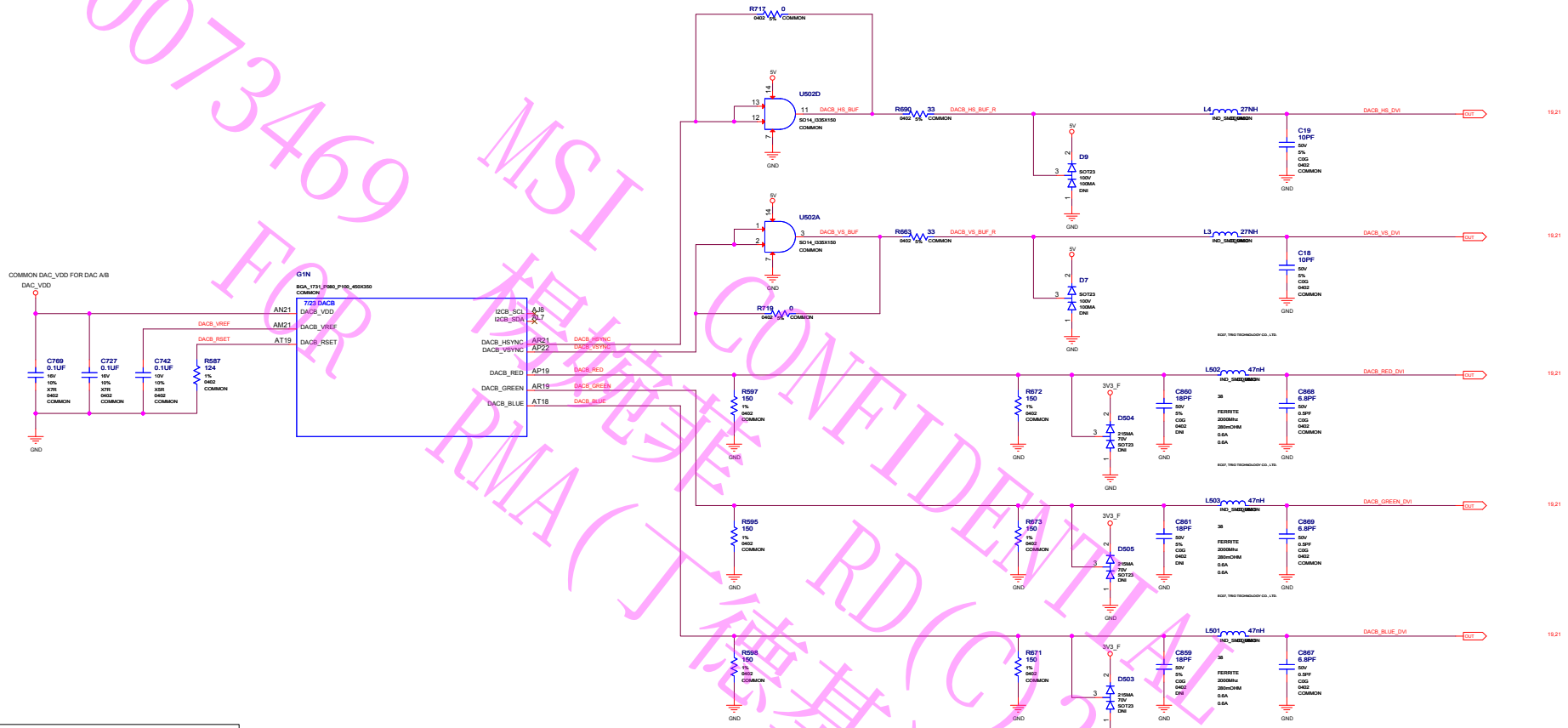

DACB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE
DACB_RED_DVI	1	75OHM
DACB_GREEN_DVI	1	75OHM
DACB_BLUE_DVI	1	75OHM
DACB_HS_DVI	2	50OHM
DACB_VS_DVI	2	50OHM

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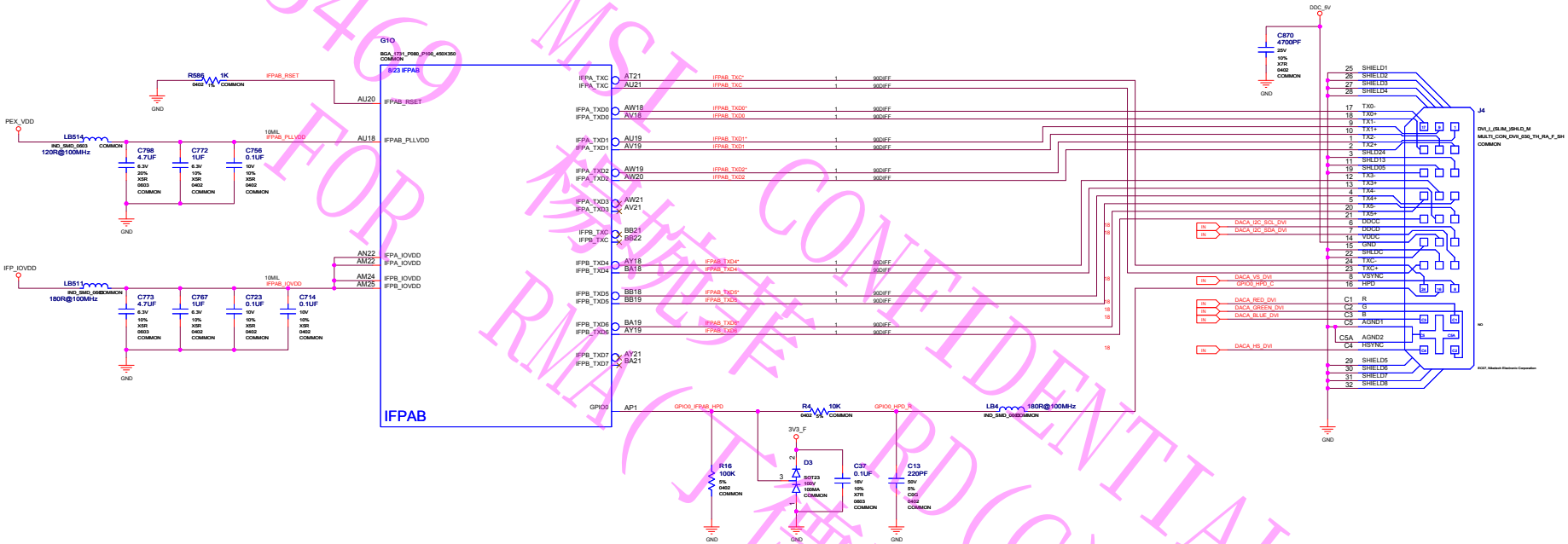
Page20: IFPAB DVI-I-DL (South)



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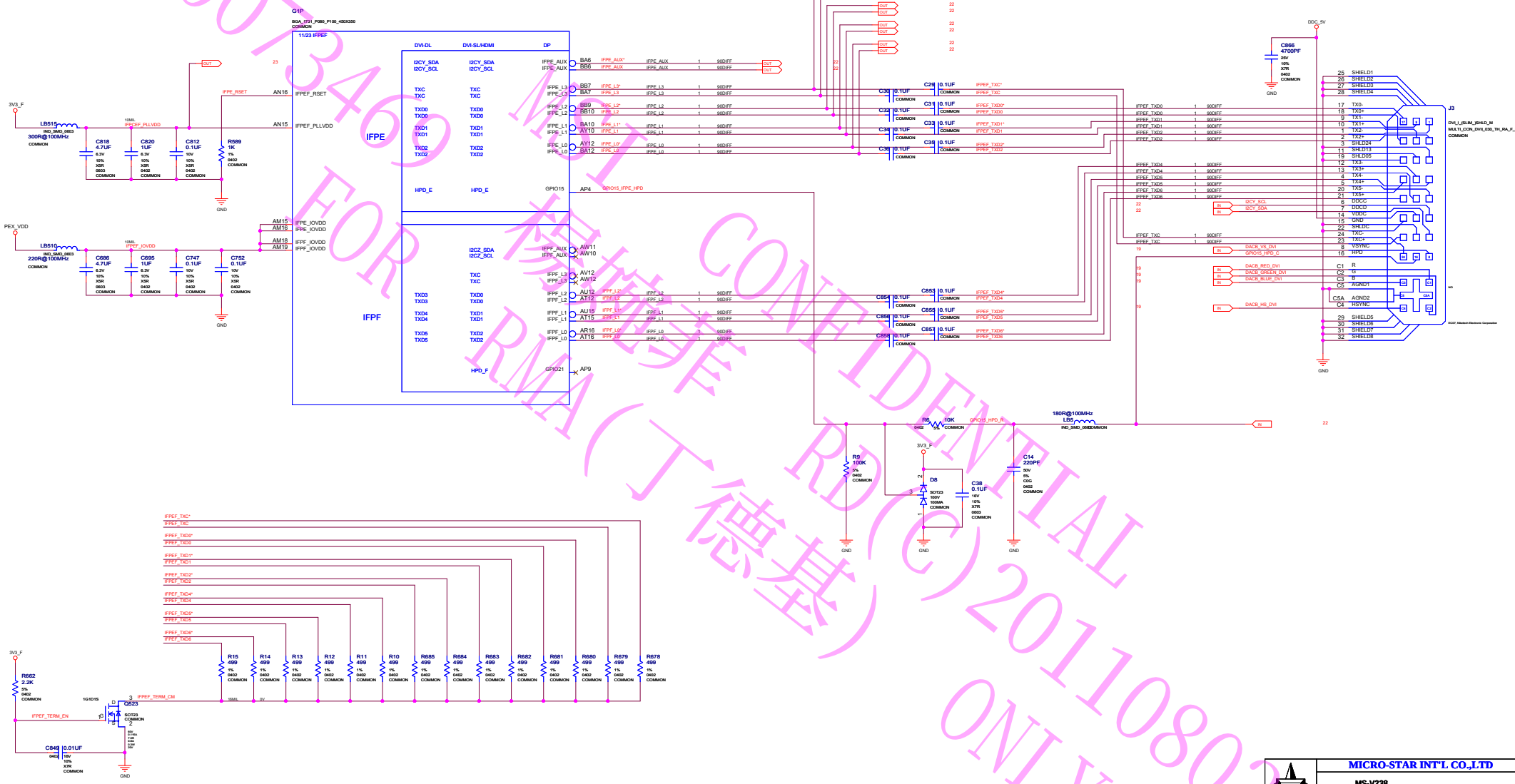
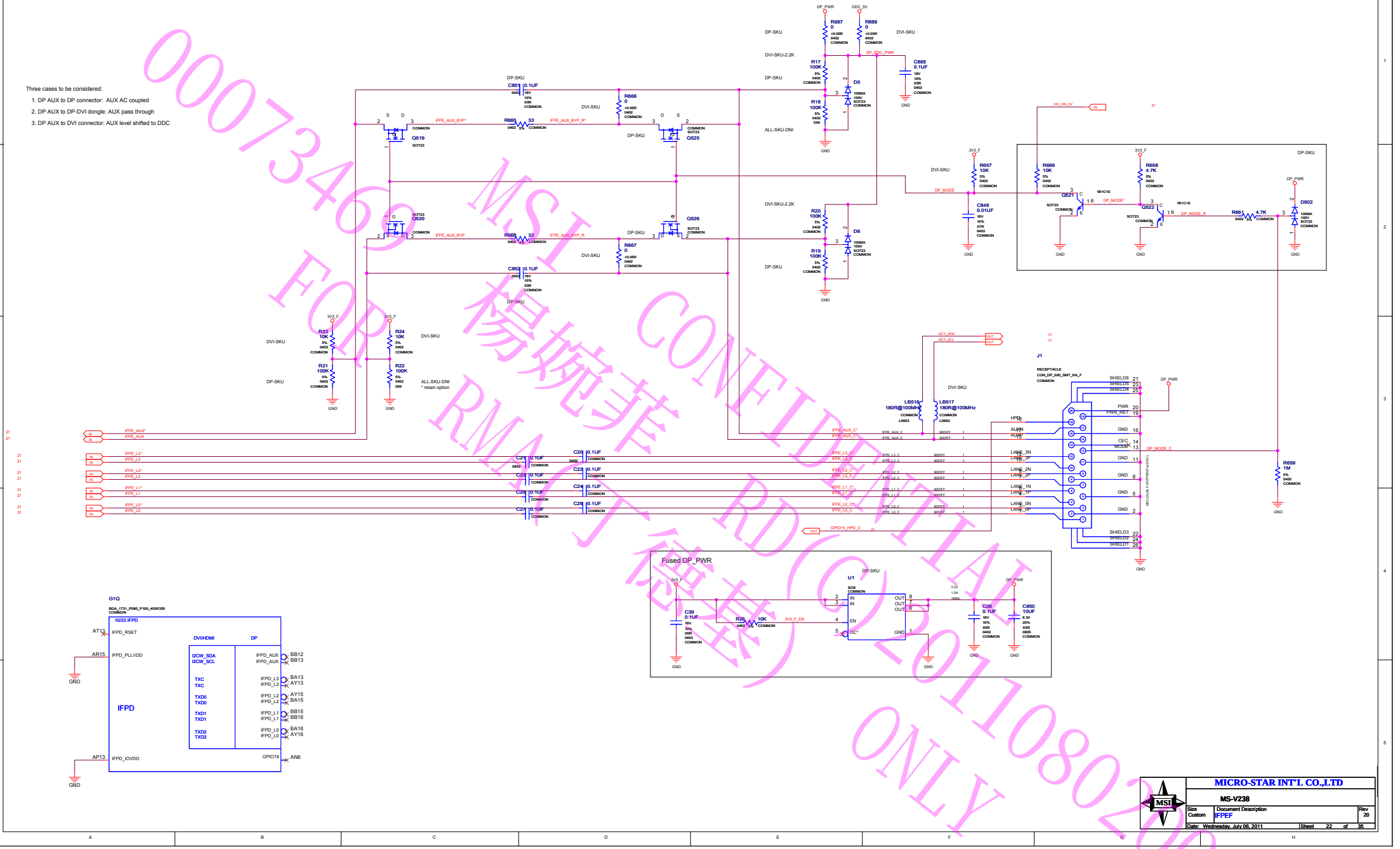
Page21: IFPEF DVI-I-DL (Mid)



Page22: IFPEF DP (Mid)

Three cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through
3. DP AUX to DVI connector: AUX level shifted to DDC



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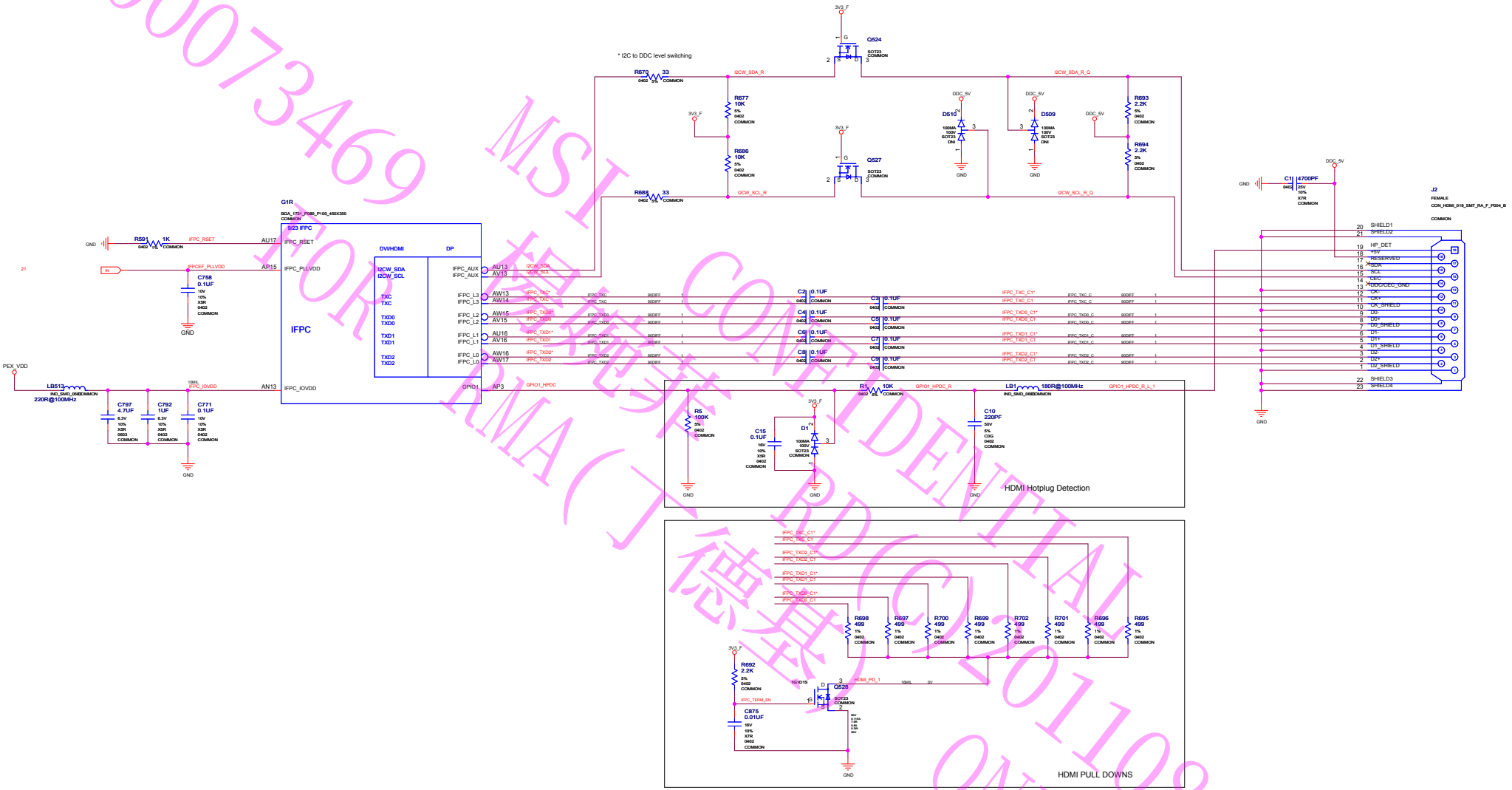
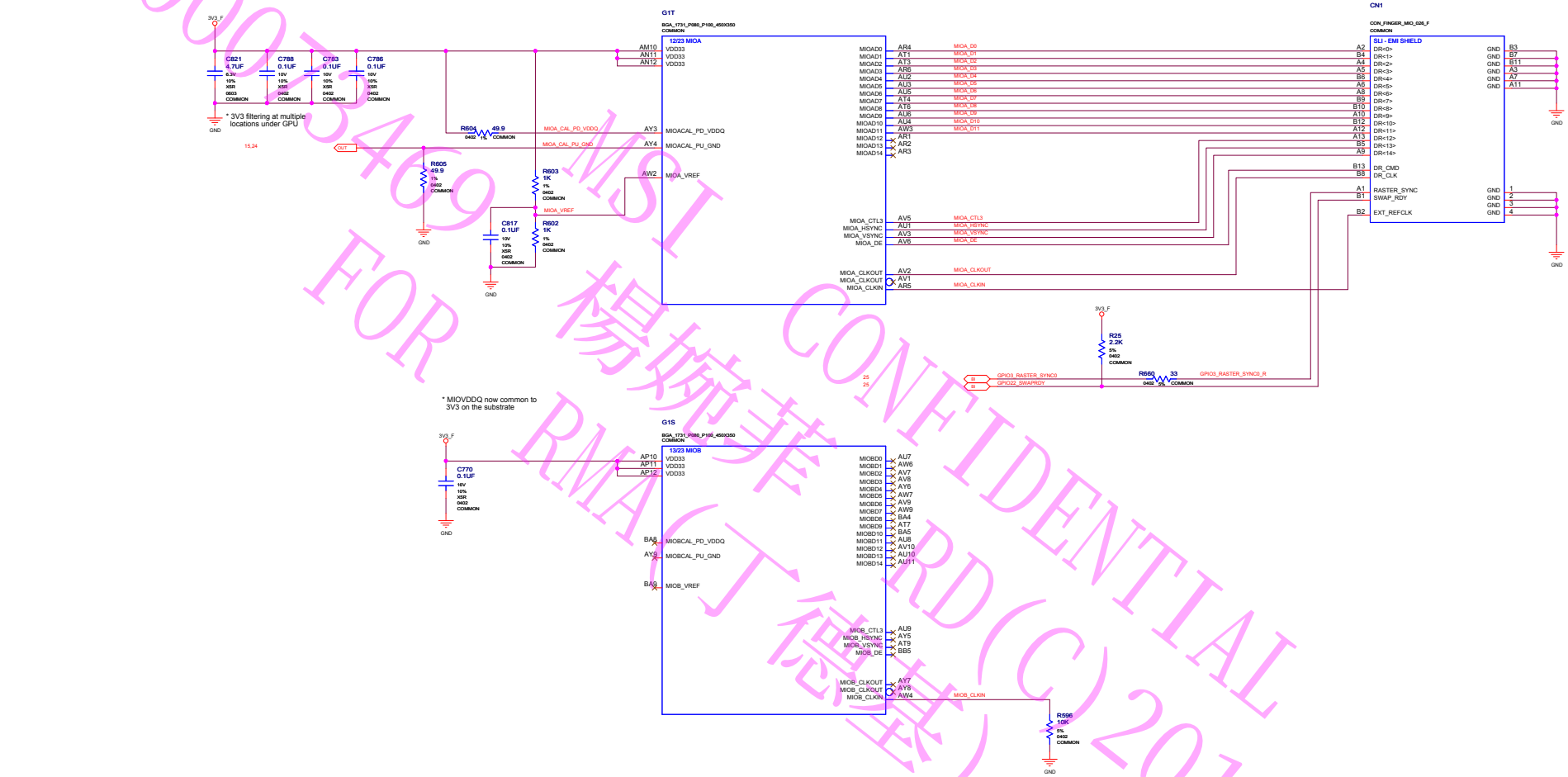
Page23: IFPC mHDMI (North)



Page24: Multi-use IO (MIO) Interface



MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR

NET	VOLTAGE	MIN_WIDTH
MIOA_CAL_PU_GND	0.6V	6MIL

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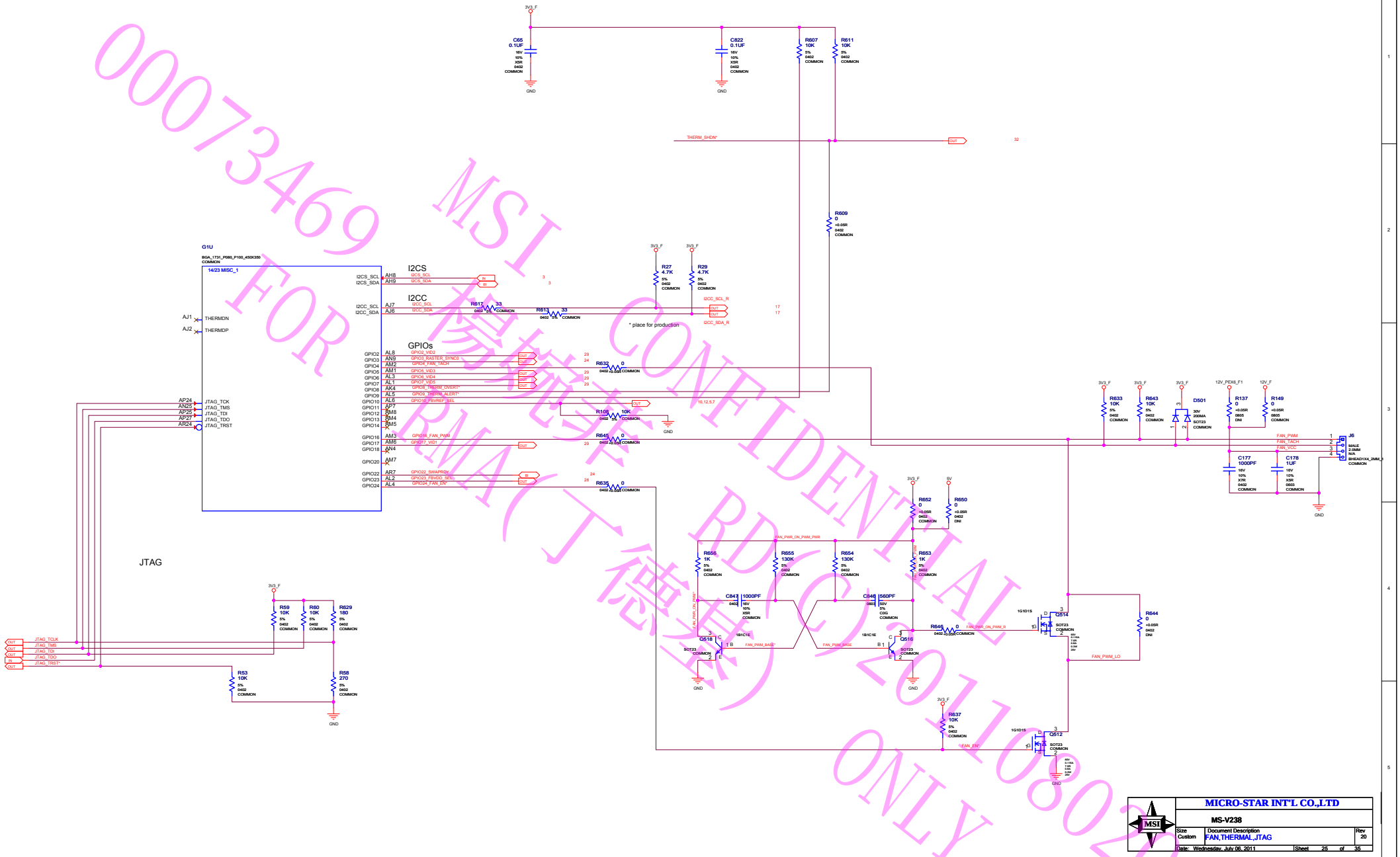
Page25: Misc: Fan, Thermal, JTAG, GPIO



Page26: Misc: ROM, HDCP, XTAL, Straps

STRAP0	USER_BIT [3..0]	0000:=> 5K PD
STRAP1	3GIO_PADCFG_LUT_ADR	0000 :=>5K PD 0000 Desktop
STRAP2	PCI_DEVID [3:0]	0010 For 0x0E22 :=> 15K PD 0100 For 0x0E24 :=> 25K PD
ROM_SI	RAMCFG[0]	
	RAMCFG[1]	
	RAMCFG[2]	
	RAMCFG[3]	
ROM_SO	VGA_DEVICE	1
	SMB_ALT_ADDR	0
	FB[0]_BAR_SIZE	0
	XCLK_417	0
ROM_SCLK	PEX_PLL_EN_TERM100	1 ENABLED
	SLOT_CLK_CFG	1 ENABLE
	SUB_VENDOR	1 Dedicated BIOS
	PCI_DEVID_EXT	0 0xC

32Mx32 256 bit Samsung for SKU 10 first memory
0011: PD 20K
32Mx32 256 bit Hynix for SKU 10 2'nd memory
0010: PD 15K

32Mx32 192 bit Samsung for SKU 0 first memory
1011: PU 20K
32Mx32 192 bit Hynix for SKU 0 2'nd memory
1010: PU 15K

10k PD

45K PD

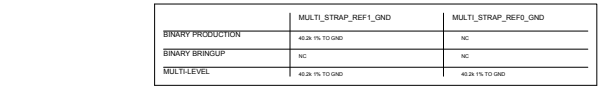
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

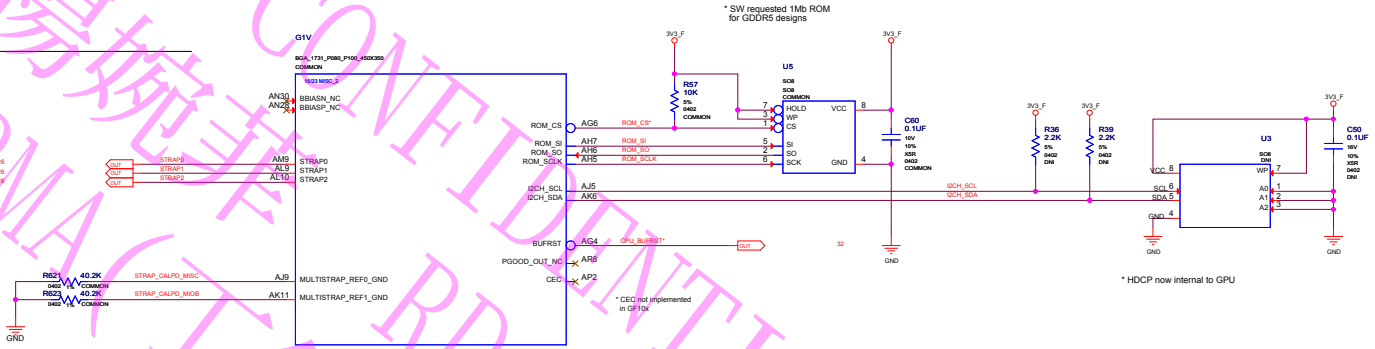
CFG[3:0] Config Width Vendor

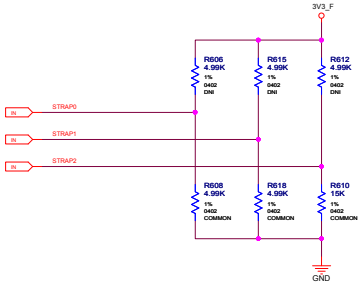
0000	Reserved	
0001	32Mx32 256-bit	Qimonda
0010	32Mx32 256-bit	Hynix
0011	32Mx32 256-bit	Samsung
0100	Reserved	
0101	64Mx32 256-bit	Qimonda
0110	64Mx32 256-bit	Hynix
0111	64Mx32 256-bit	Samsung
1000	Reserved	
1001	32Mx32 192-bit	Qimonda
1010	32Mx32 192-bit	Hynix
1011	32Mx32 192-bit	Samsung
1100	Reserved	
1101	64Mx32 192-bit	Qimonda
1110	64Mx32 192-bit	Hynix
1111	64Mx32 192-bit	Samsung

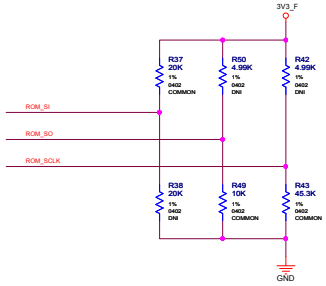
MISC NET RULES

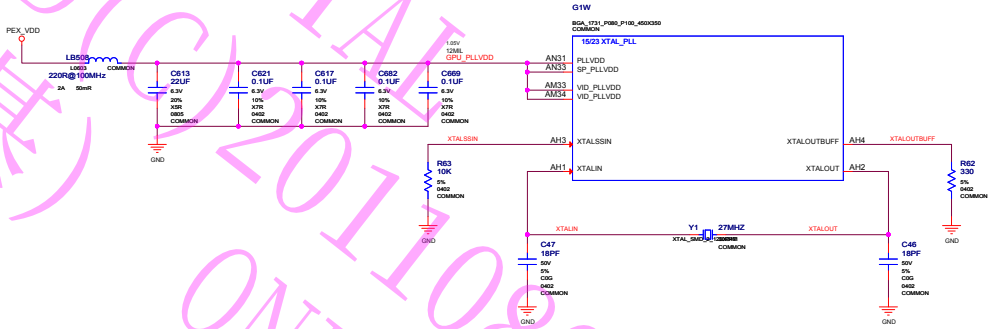
NET	NV_CRITICAL	NV_IMPEDANCE











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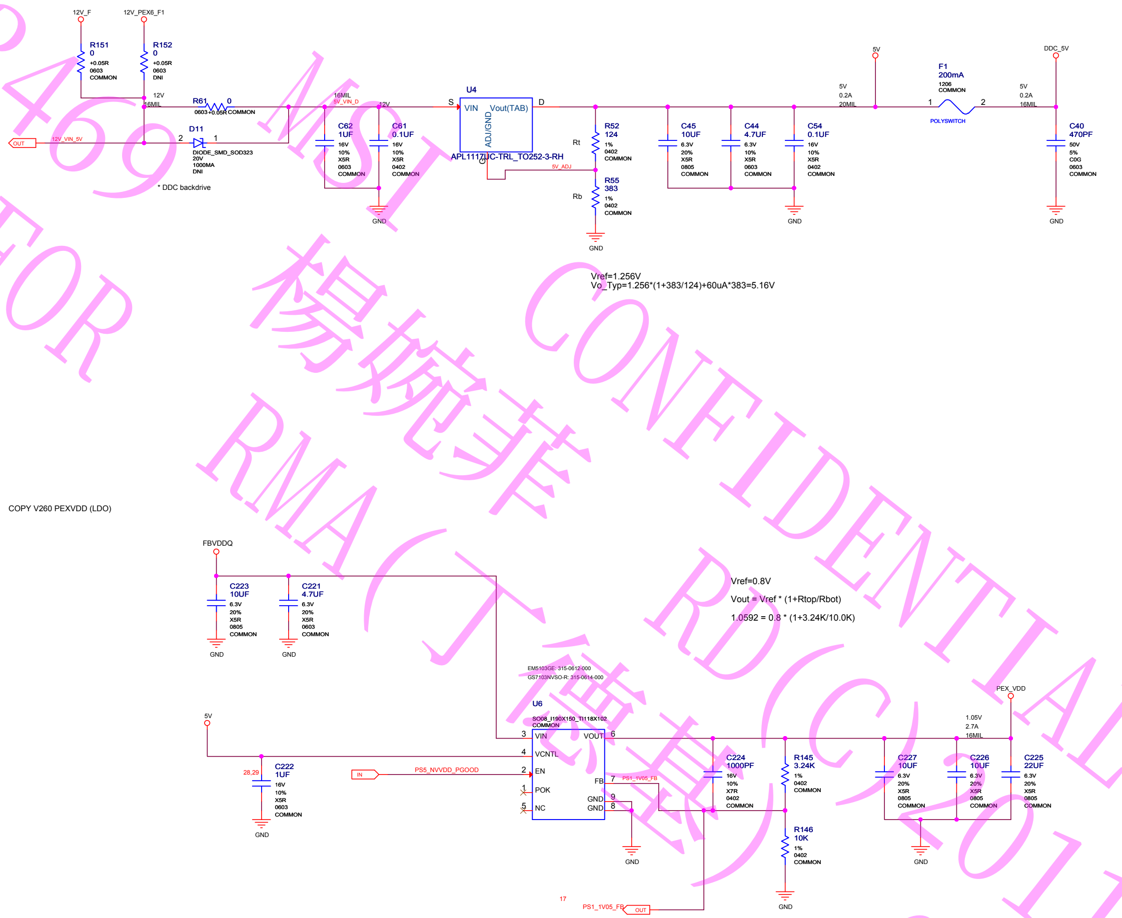
Page27: PS: 5V, PEX_VDD



12V_F
12V_PEX6_F1
R151 0
R152 0
R61 0
D11
DIODE_SMD_SOD323
* DDC backdrive
C62 1UF
C61 0.1UF
U4
VIN
Vout(TAB)
ADJ/GND
APL1117UC-TRL_TO252-3-RH
R52 124
R55 383
Rt
Rb
C45 10UF
C44 4.7UF
C54 0.1UF
5V
F1 200mA
POLYSWITCH
DDC_5V
C40 470PF
GND
Vref=1.256V
Vo_Typ=1.256*(1+383/124)+60uA*383=5.16V
COPY V260 PEXVDD (LDO)
FBVDDQ
C223 10UF
C221 4.7UF
Vref=0.8V
Vout = Vref * (1+Rtop/Rbot)
1.0592 = 0.8 * (1+3.24K/10.0K)
U6
VIN
VCNTL
EN
POK
NC
VOUT
FB
GND
PEX_VDD
C222 1UF
PS5_NVVDD_PGOOD
C224 1000PF
R145 3.24K
R146 10K
C227 10UF
C226 10UF
C225 22UF
PS1_1V05_FB

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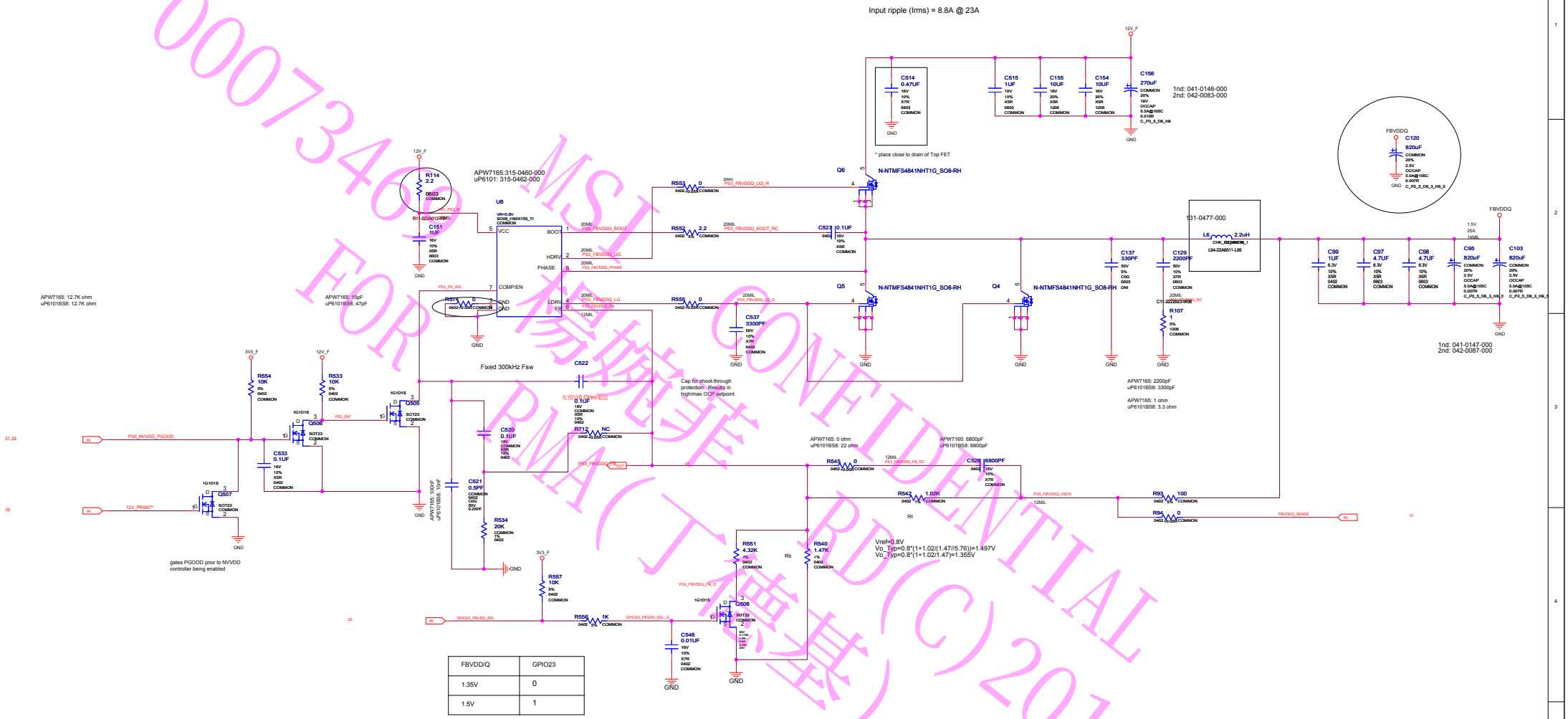
Page28: PS: FBVDD/Q



FBVDD/Q	GPIO23
1.35V	0
1.5V	1

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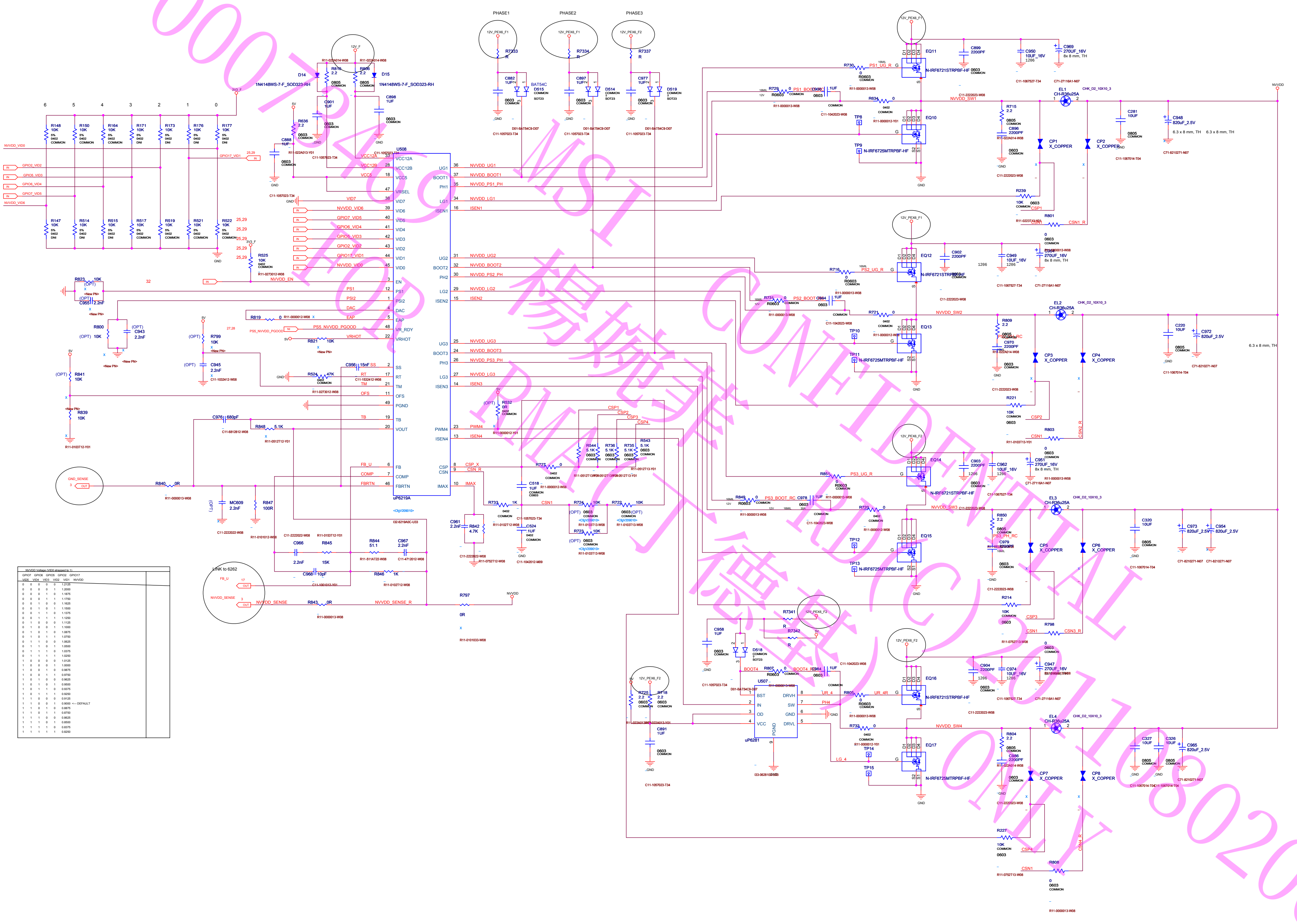
PS III: NVVDD Power Supply



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MSI	MICRO-STAR INT'L CO.,LTD	
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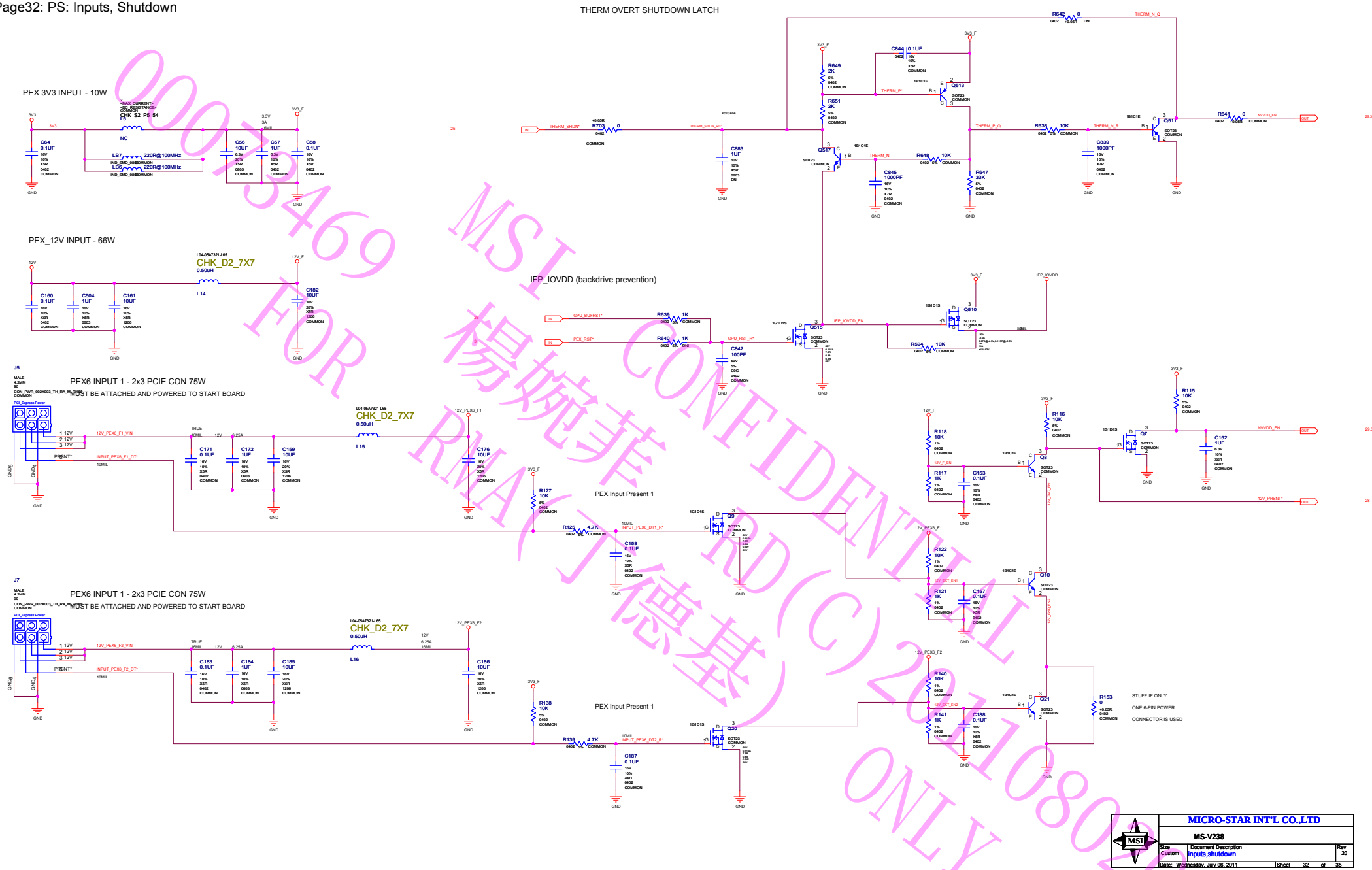
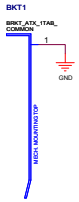
Page32: PS: Inputs, Shutdown



Page33: Mechanical: Bracket/Thermal Solution

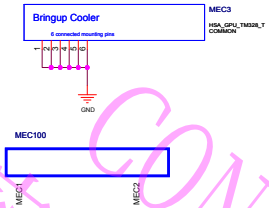
Brackets:

Bracket with DVI_DP_mHDMI : 151-10001-0355-071

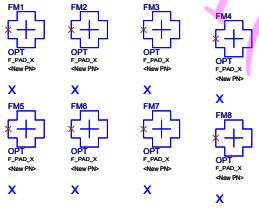


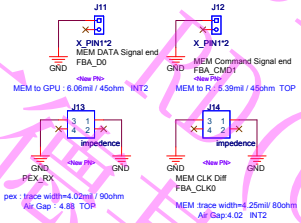
Bracket Screw

Cooler/GPU Stiffener



remove mec1





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Page34: Blank

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VID Table

GPIO7	GPIO6	GPIO5	GPIO2	GPIO17	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

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