

PCI-EXPRESS EDGE CONNECTOR

Production (No JTAG)	Install R1, R2 & Don't Install TSW1	
Internal Use Only	Install TSW1 & Don't Install R1 & R2	
	JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open
	NO JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)

PCIe RESET Buffered

Default: Install R9 & R11

6,16,17,18 PWR_GOOD

R11 10K

R12 0R

R9 0R

+3.3V

+3.3V_BUS

C4 100nF_6.3V

U11 NCT7500PSX_NL

PERST#_buf 218

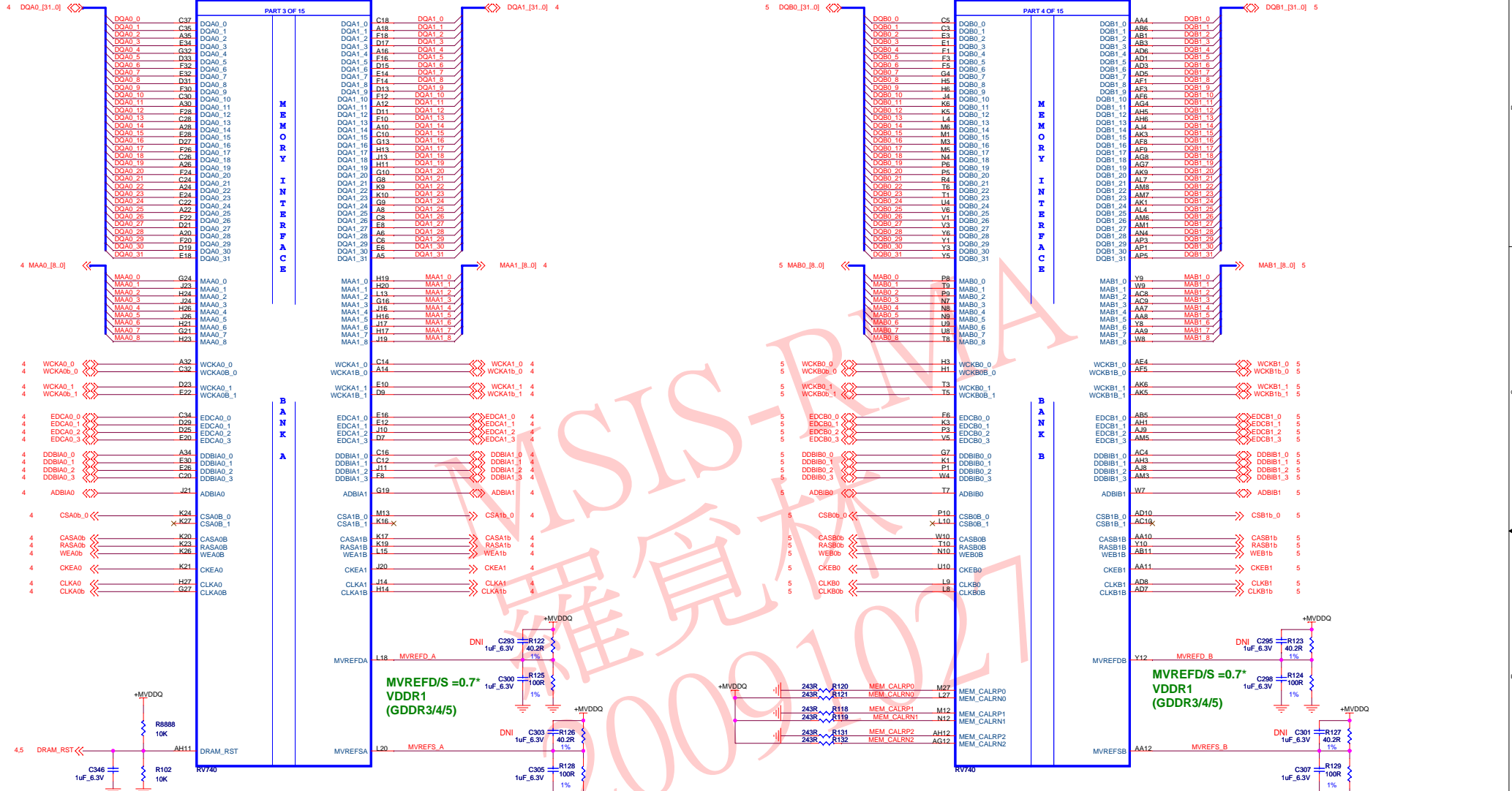
R3 0R

R_RST

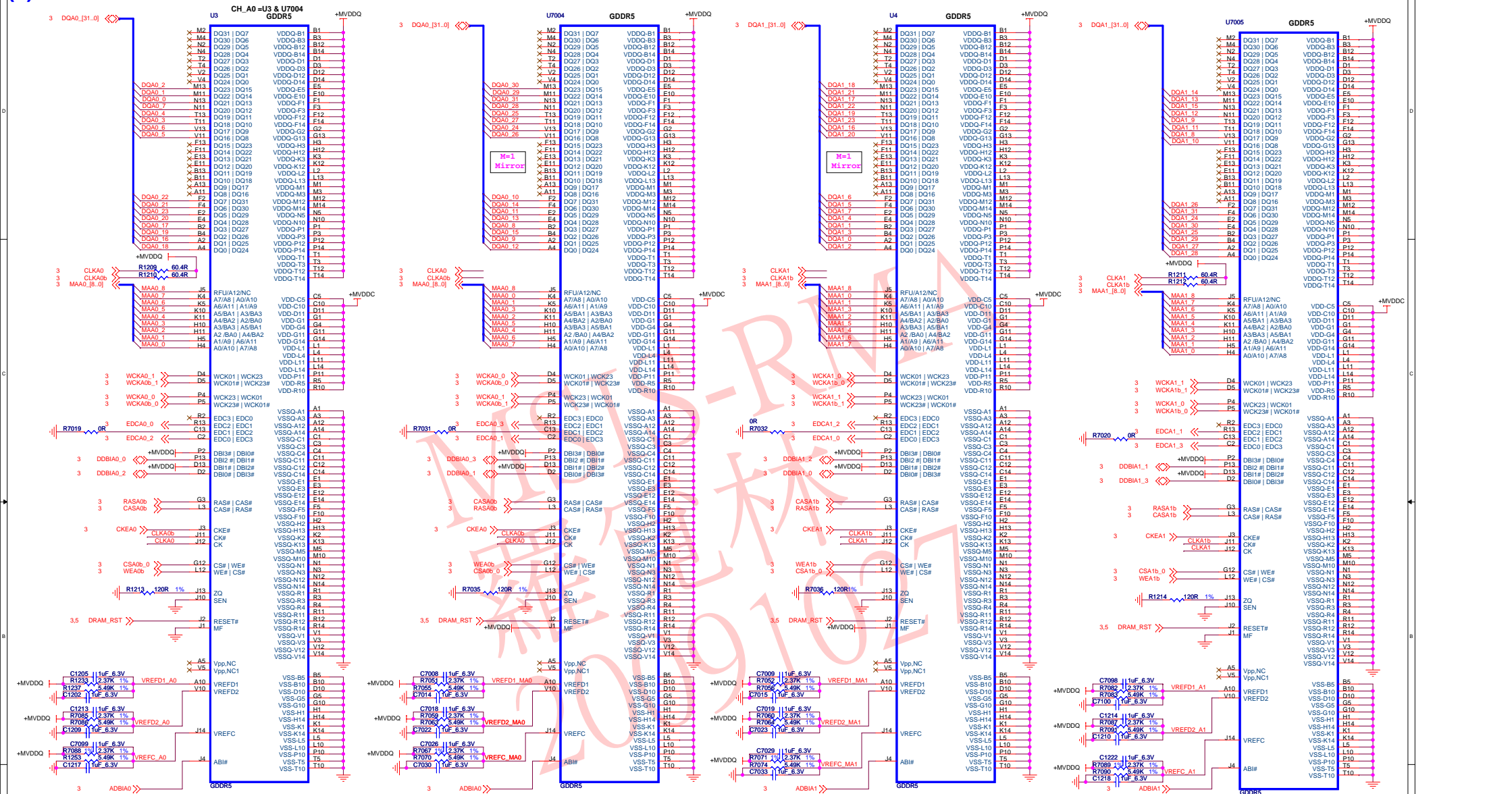
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DATE: Wednesday, May 13, 2009		Rev 6	
SHEET 1 of 19		Doc No. 105-B86300A-00	
Title RH RV740 1GB GDDR5 DVI-I TVO-DVII			

Doc No. 105-B86300-00A

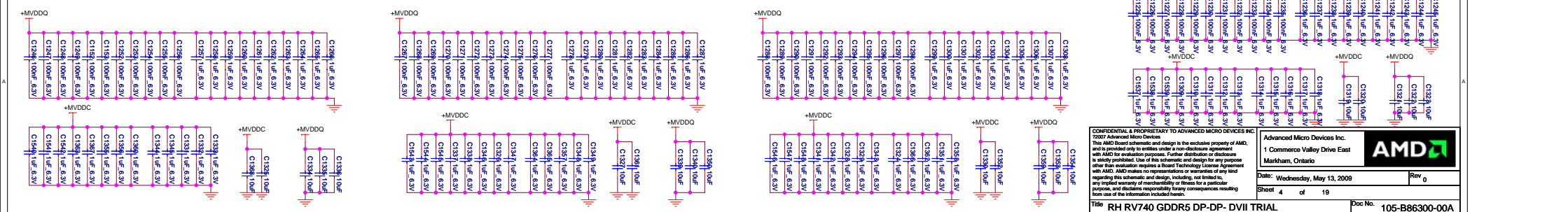
(3) RV740 MEM Interface Ch A&B



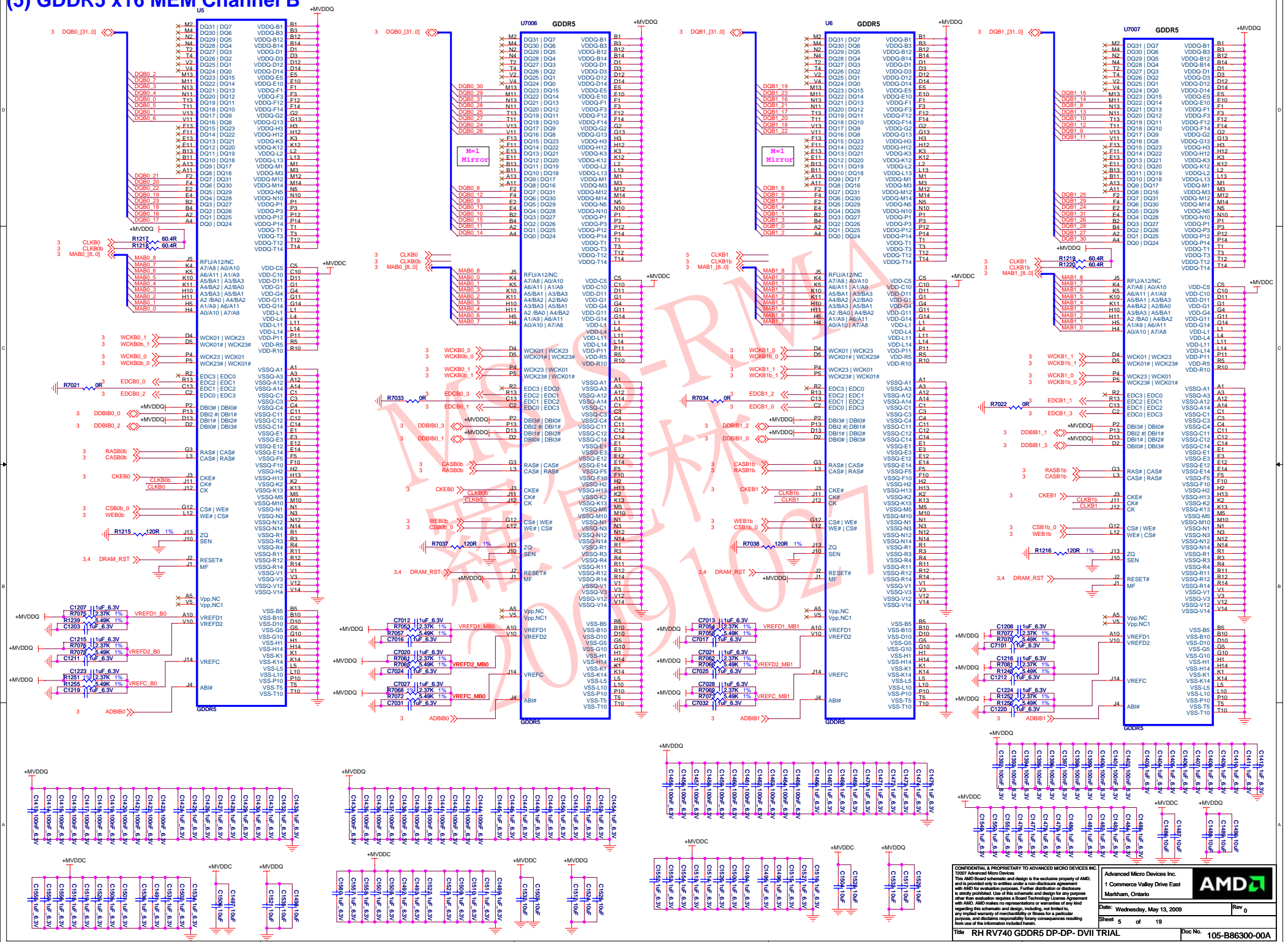
5	
(4) GDDR5 x16 MEM Channel A	



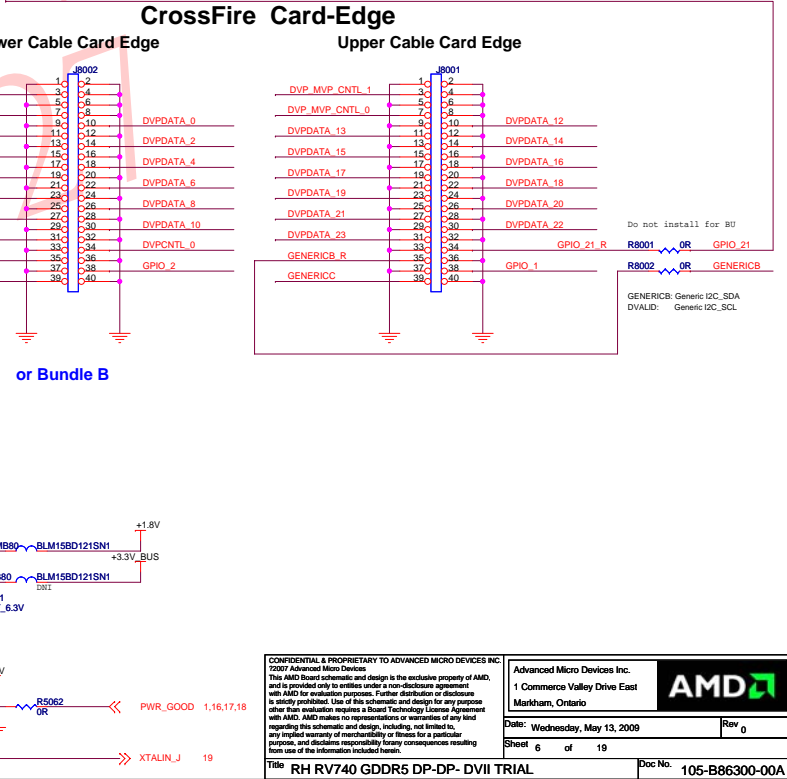
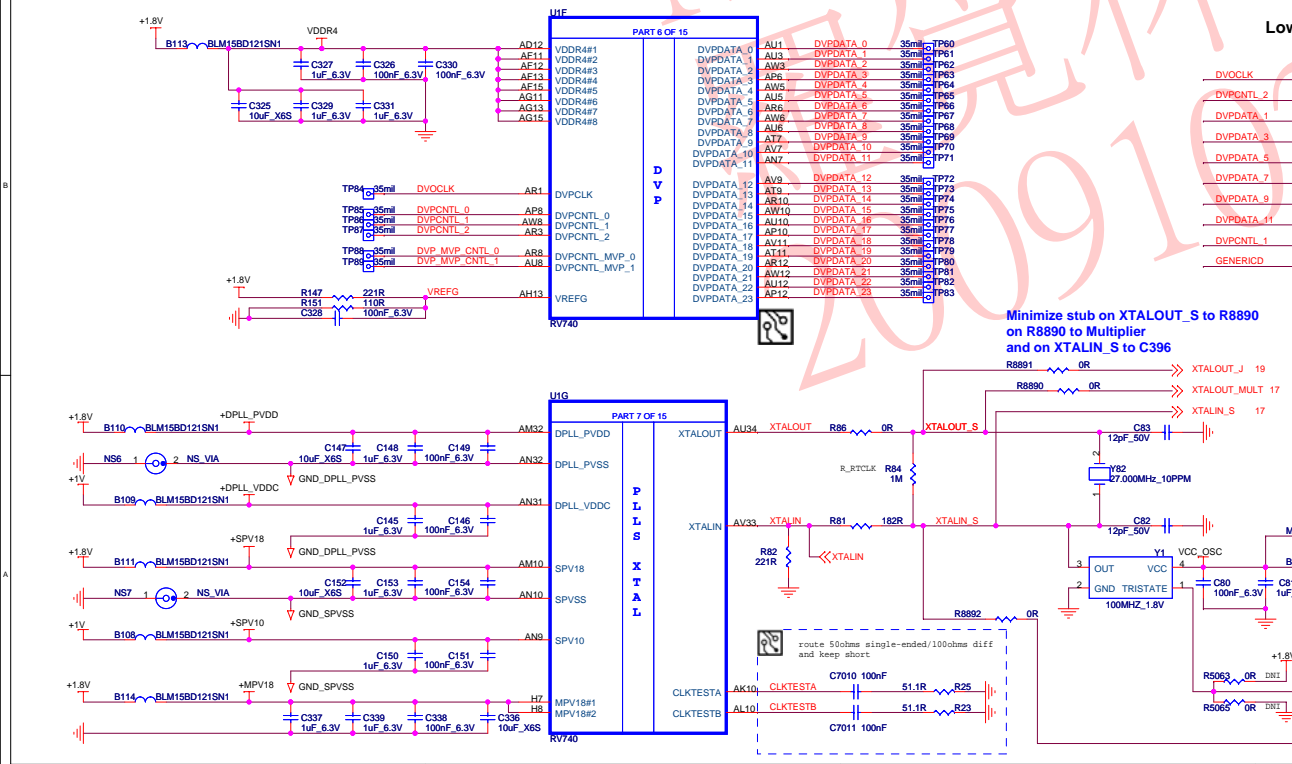
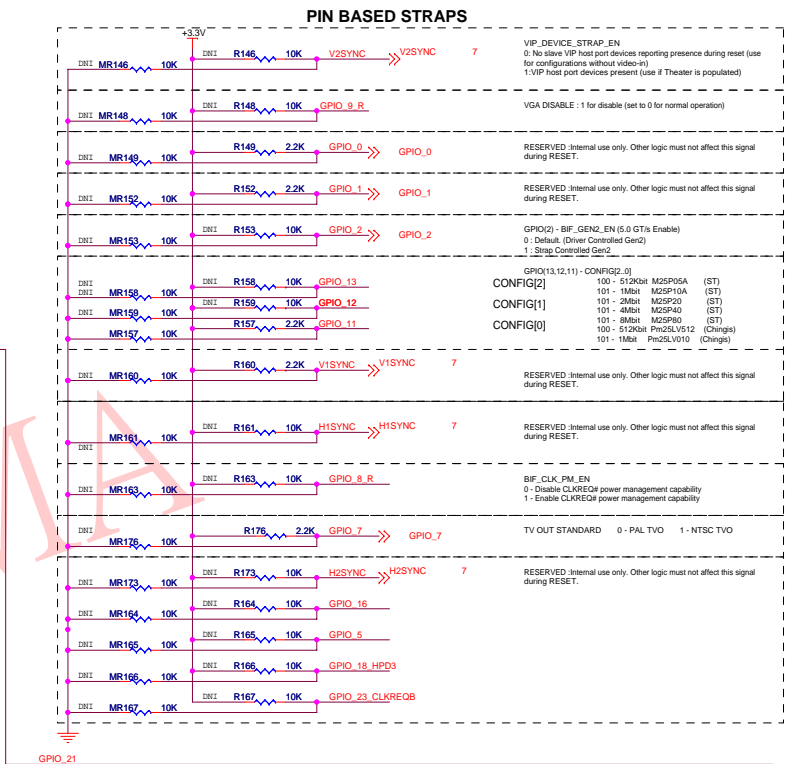
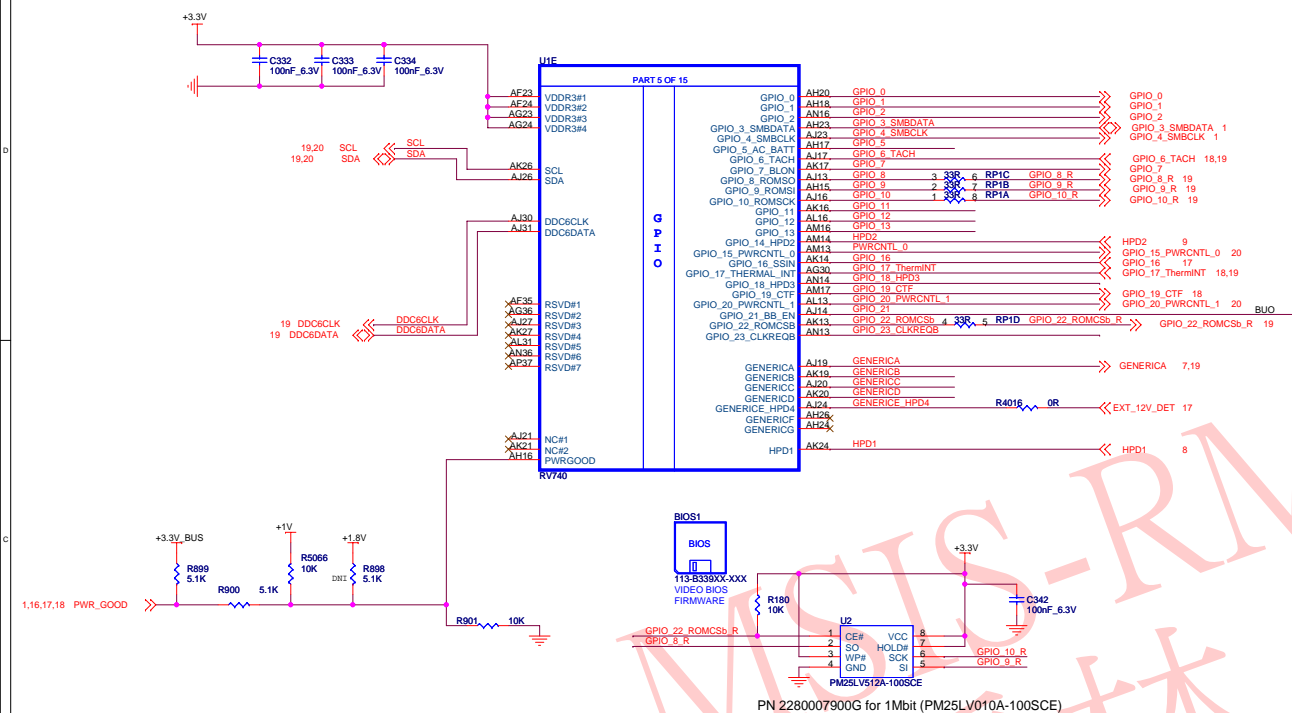
Use internal Vref memory voltage



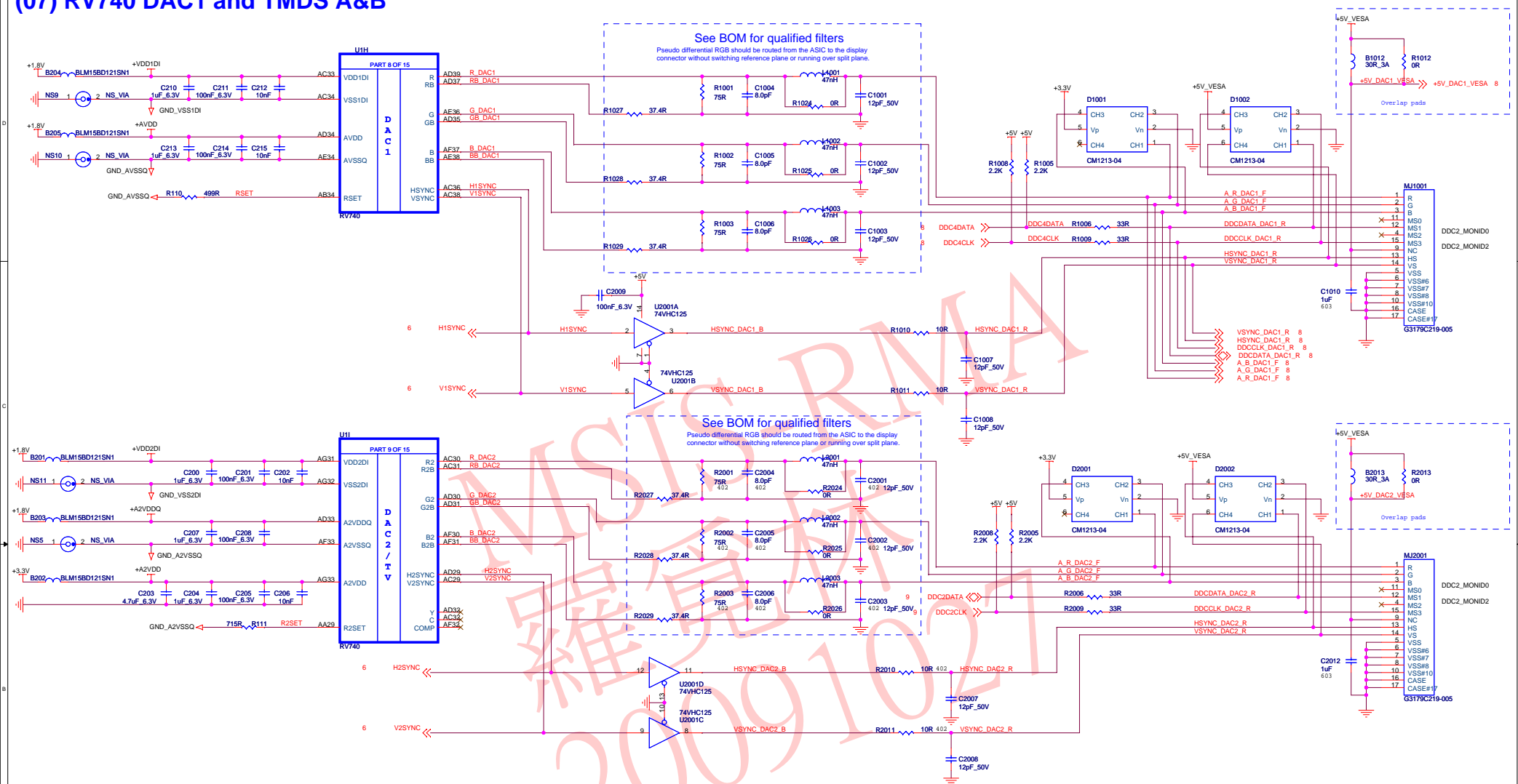
(5) GDDR5 x16 MEM Channel B



(06) RV740 GPIOs Strap CF XTAL



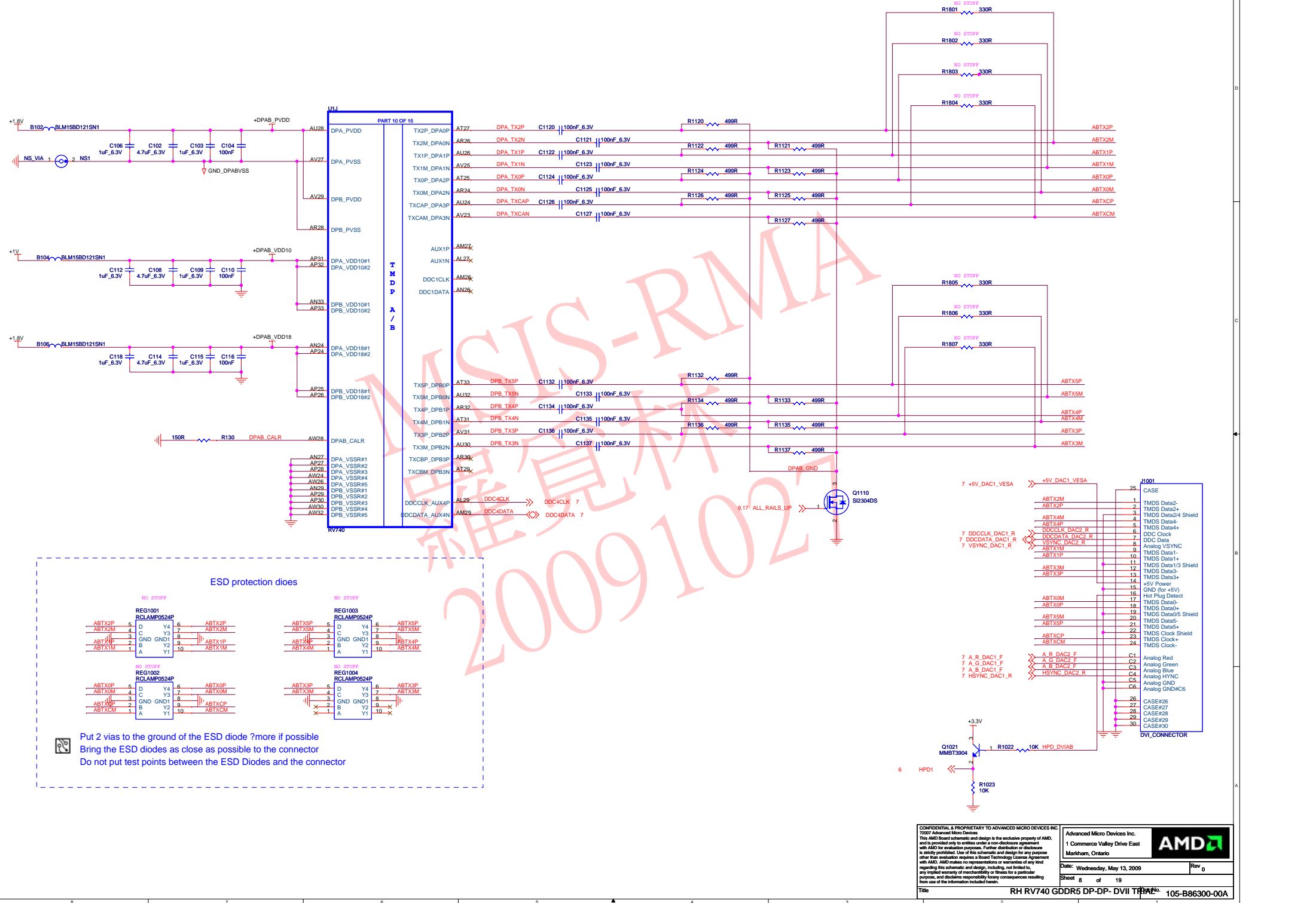
(07) RV740 DAC1 and TMDS A&B



The 7-pin MiniDIN footprint allows one of the two MiniDINs:

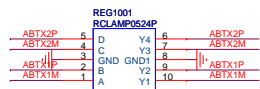
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

(08) RV740 TMD5 A&B

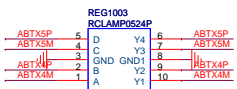


ESD protection diodes

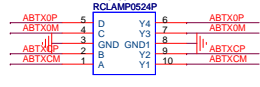
NO STUFF



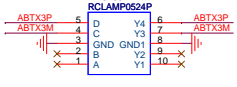
NO STUFF



NO STUFF



NO STUFF



Put 2 vias to the ground of the ESD diode ?more if possible
Bring the ESD diodes as close as possible to the connector
Do not put test points between the ESD Diodes and the connector

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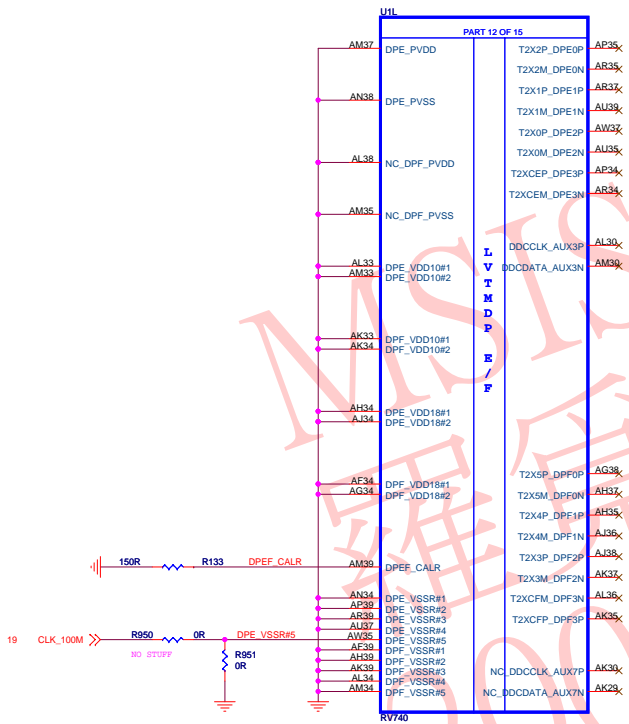
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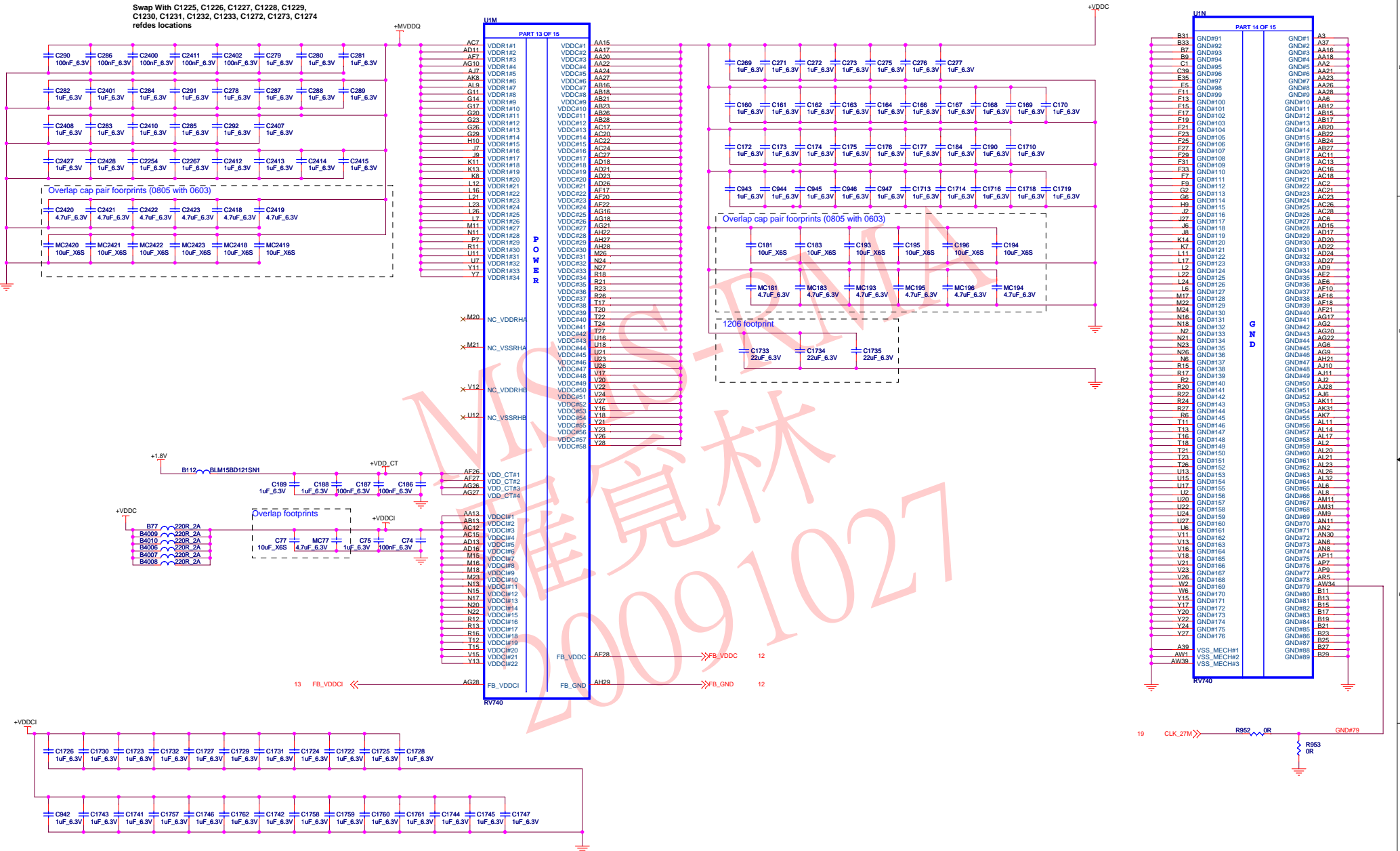
Rev 0

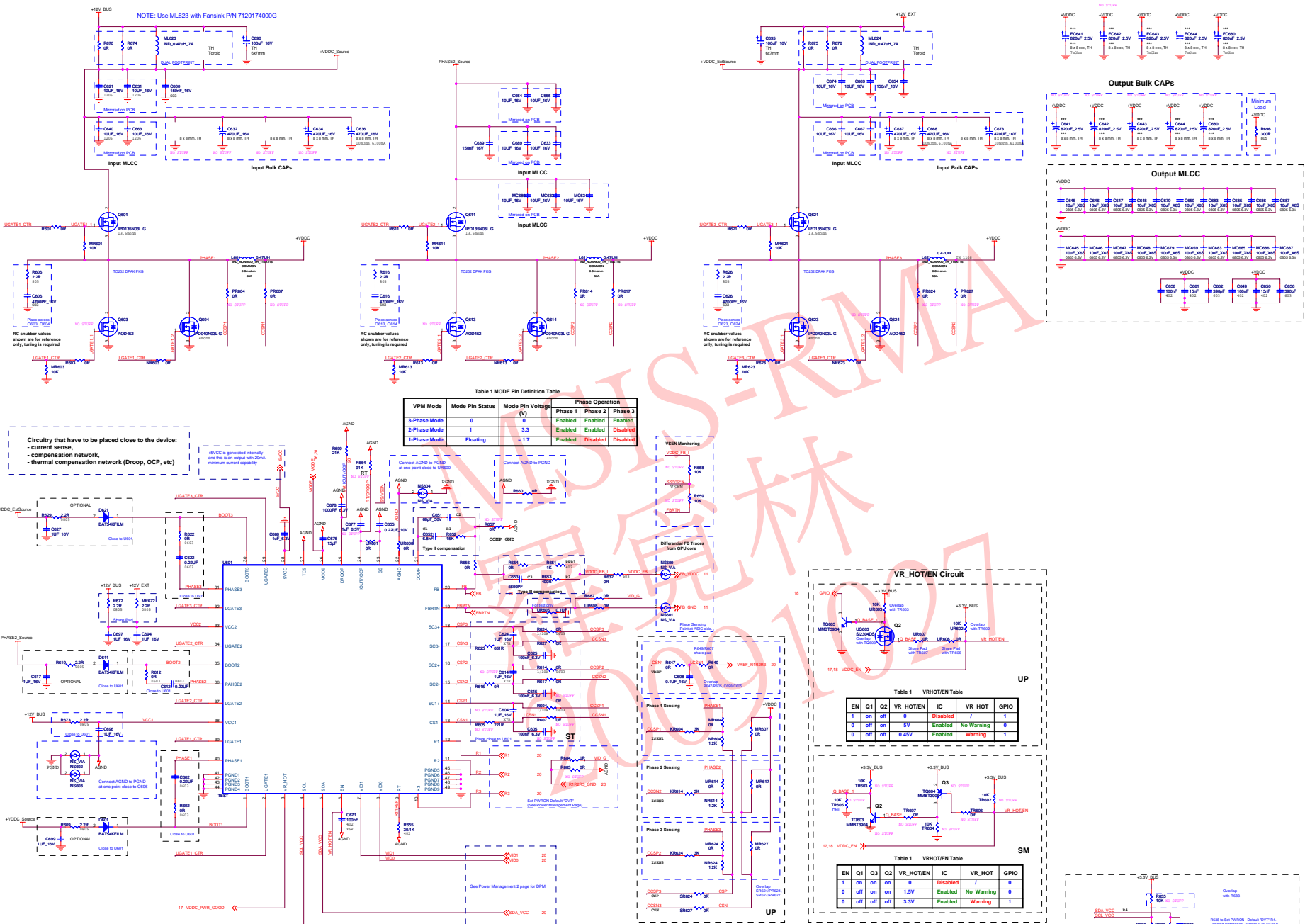
Title	RH RV740 GDDR5 DP-DP- DVII TRIPLE No.	Doc No.	105-B86300-00A
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(10) No Connect E&F



(11) RV740 Power & GND





Circuitry that have to be placed close to the device:

- current sense,
- compensation network,
- thermal compensation network (Drop, OCP, etc)

+VDDC is generated internally and pins are an output with 20mA maximum current capability

Table 1 MODE Pin Definition Table

VPM Mode	Mode Pin Status	Mode Pin Voltage (V)	Phase 1	Phase 2	Phase 3
3-Phase Mode	0	0	Enabled	Enabled	Enabled
2-Phase Mode	1	3.3	Enabled	Enabled	Disabled
1-Phase Mode	0	1.7	Enabled	Disabled	Disabled

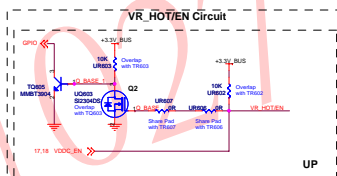


Table 1 VRHOTEN Table

EN	Q1	Q2	Q3	VR_HOTEN	IC	VR_HOT	GPIO
1	on	off	off	0	Disabled	7	1
0	off	on	off	5V	Enabled	No Warning	0
0	off	off	on	8.45V	Enabled	Warning	1

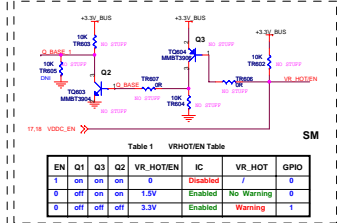
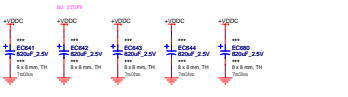


Table 1 VRHOTEN Table

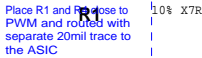
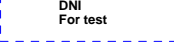
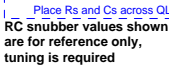
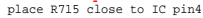
EN	Q1	Q2	Q3	VR_HOTEN	IC	VR_HOT	GPIO
1	on	on	on	0	Disabled	/	0
0	off	on	on	1.3V	Enabled	No Warning	0
0	off	off	on	3.3V	Enabled	Warning	1

Table 5 MODE Pin & Phase3 Strip Detection Table

App	Condition	Mode Pin	VPM Mode	Phase 3	IC Behavior
CASE 1	PartUp without EXT. 12V Cable	1	2-Ph	Open	IC enabled without detecting EXT. 12V (VCC2) voltage.
CASE 2	PartUp with EXT. 12V Cable	1	2-Ph	Open	Detect EXT. 12V (VCC2) voltage before IC enable.
CASE 3	PartUp with EXT. 12V Cable	1	Mode	Pull Down	



(13) VDDCI



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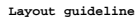
Rev 0

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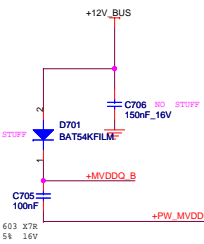
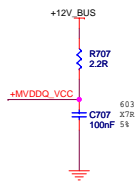
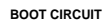
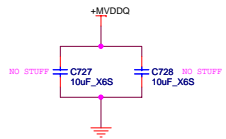
Doc No. 105-B86300-00A

Title	RH RV740 GDDR5 DP-DP- DVII TRIAL
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Doc No. 105-B86300-00A



- 4-position the controller (U703) such that Ldate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R71 and R722 next to the gate of the MOSFETs. Make the gate drive traces (PW MVDCD LOG and PW MVDCD HSD) as short and as wide as possible to reduce the trace inductance.
- 5-position the bypass capacitors for the MOSFETs as close to the MOSFETs as possible as possible. They are as follows:
- C70 bypass cap is C701, and Boost cap is C705.
 - C71 bypass cap is C711, and C712 is C714 close to the pin 7. Place the rest of the compensation network close to pins 3 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



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Date: Thursday, May 14, 2009


Rev 2

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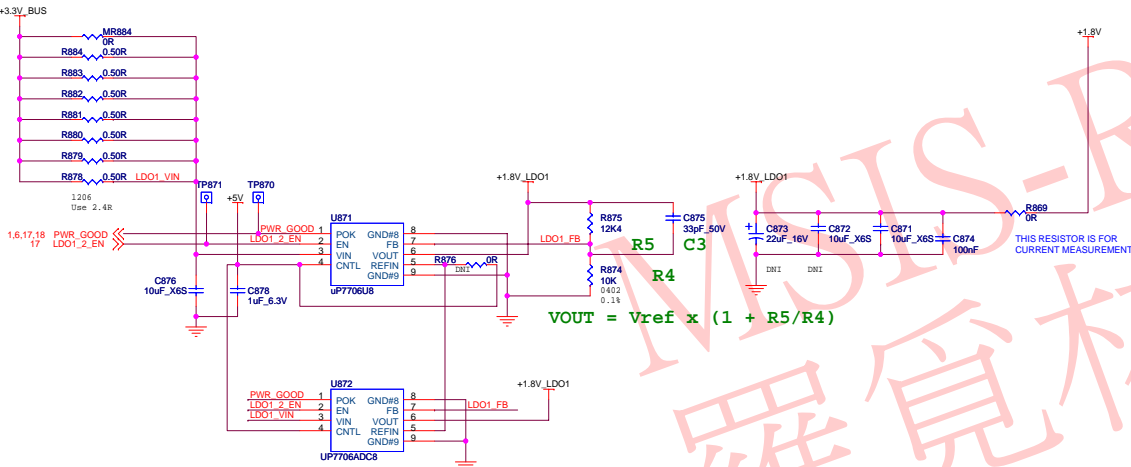
Title RV740 DDR3 1GB 8pcs 64Mx16 DVI VO DVI 6L FH CF Doc No. 105-B891xx-00A

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	Date: Wednesday, May 13, 2009			Rev 0
	Sheet 15 of 21			
	Title RH RV740 GDDR5 DP-DP- DVII TRIAL			Doc No. 105-B86300-00A

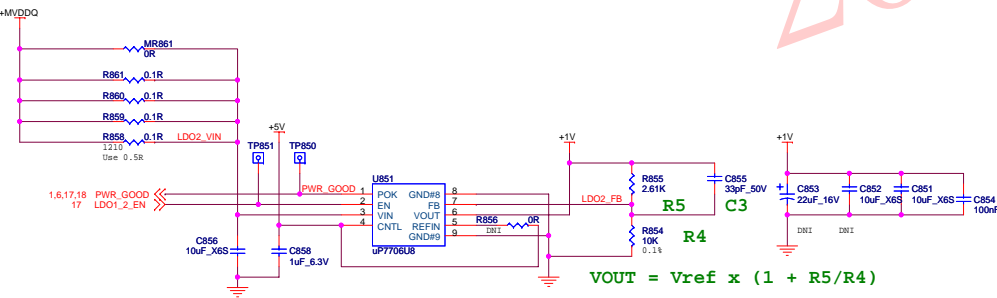
(14) Linear Regulators

LDO #1: Vin = 3.0V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 1.0A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



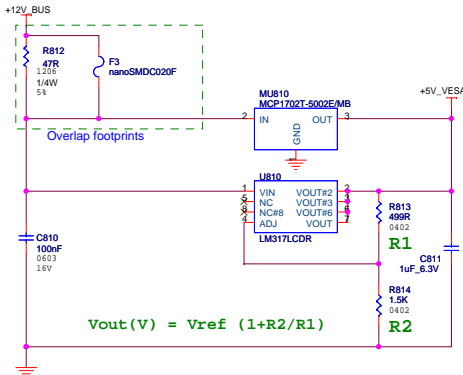
$$V_{OUT} = V_{ref} \times (1 + R5/R4)$$

LDO #2: Vin = +1.35V to 2.0V MAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



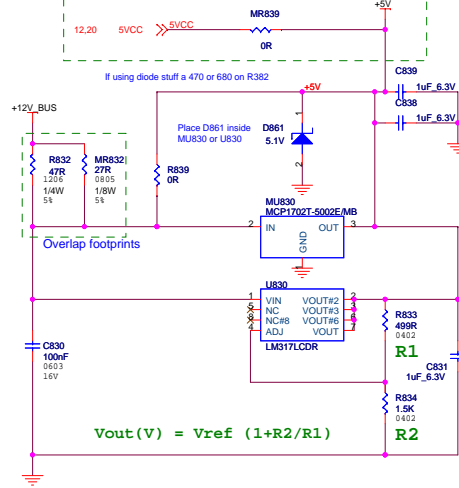
$$V_{OUT} = V_{ref} \times (1 + R5/R4)$$

Regulators for +5V, +5V_VESA and +5V_VESA2



$$V_{out}(V) = V_{ref} (1 + R2/R1)$$

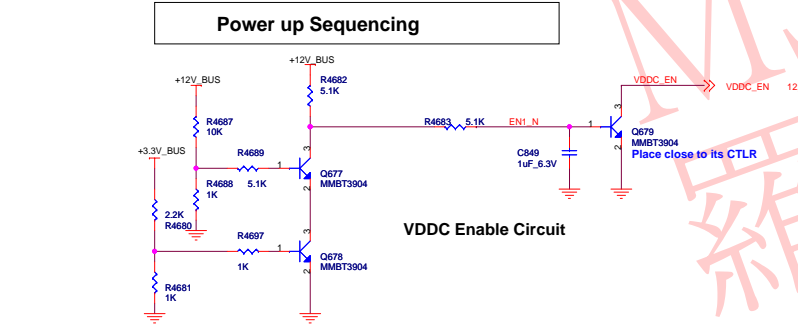
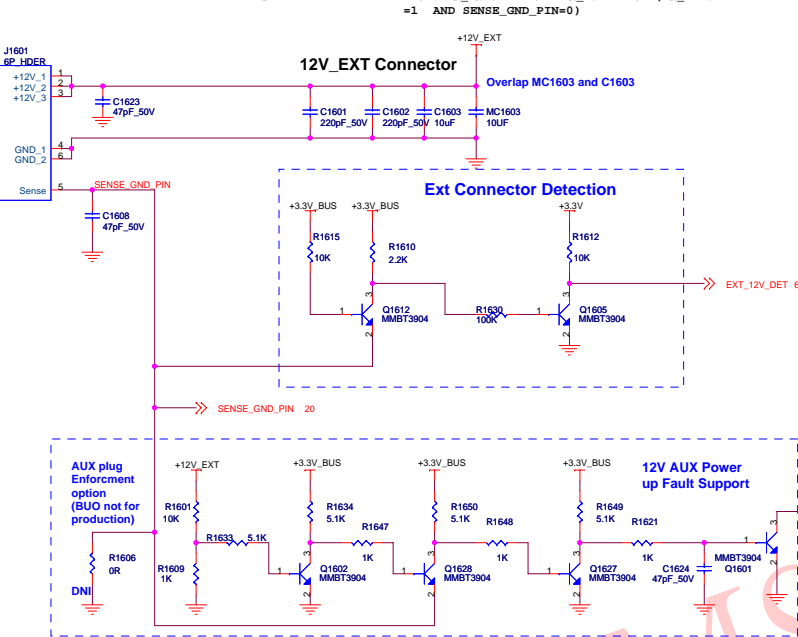
Install only R839 or MR839
See BOM for qualified option



$$V_{out}(V) = V_{ref} (1 + R2/R1)$$

(15) Power Management

VDDC is open collector and it is deactivated (pulled down to ground) when: EN_INTb =1 OR EN_Tb =1 OR (EN_EXTb =1 AND SENSE_GND_PIN=0)



SS Solutions

Clock range selection and device

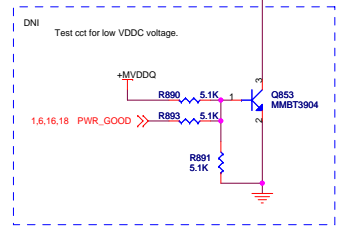
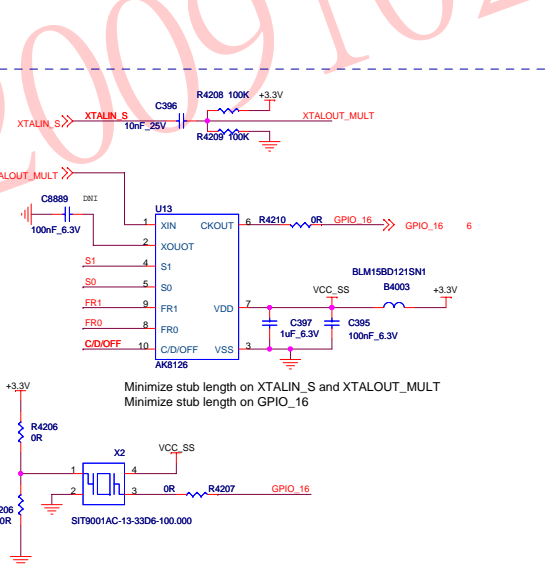
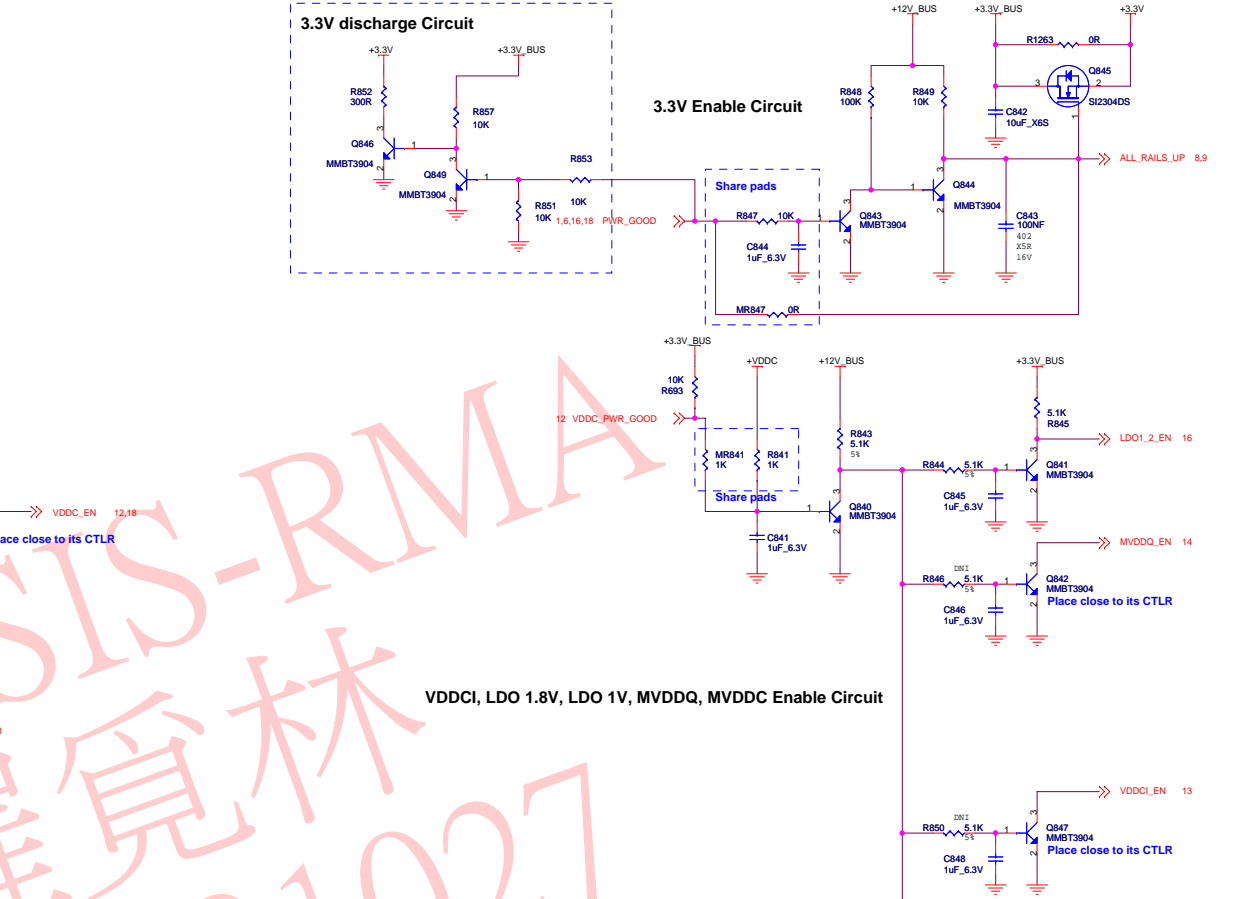
FR1	FR0	Input	Output	AKM P/N
H	L	64-128MHz	64-128MHz	AK8126A
H	H	27MHz	100MHz	AK8126B

Spread Mode

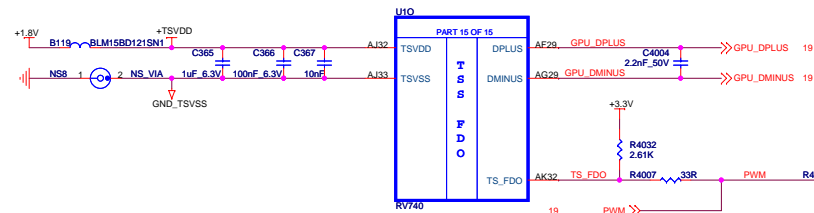
C/D/OFF	Input
L	DOWNSPREAD
H-L	NO Modulation
H	CENTER SPREAD

Spread Spectrum Modulation Charact.

S1	S0	AKM 8126B	AKM 8126A
L	H	-3.75%	
L	L	-0.625%	
H	L	-1.25%	
H	H	-1.875%	



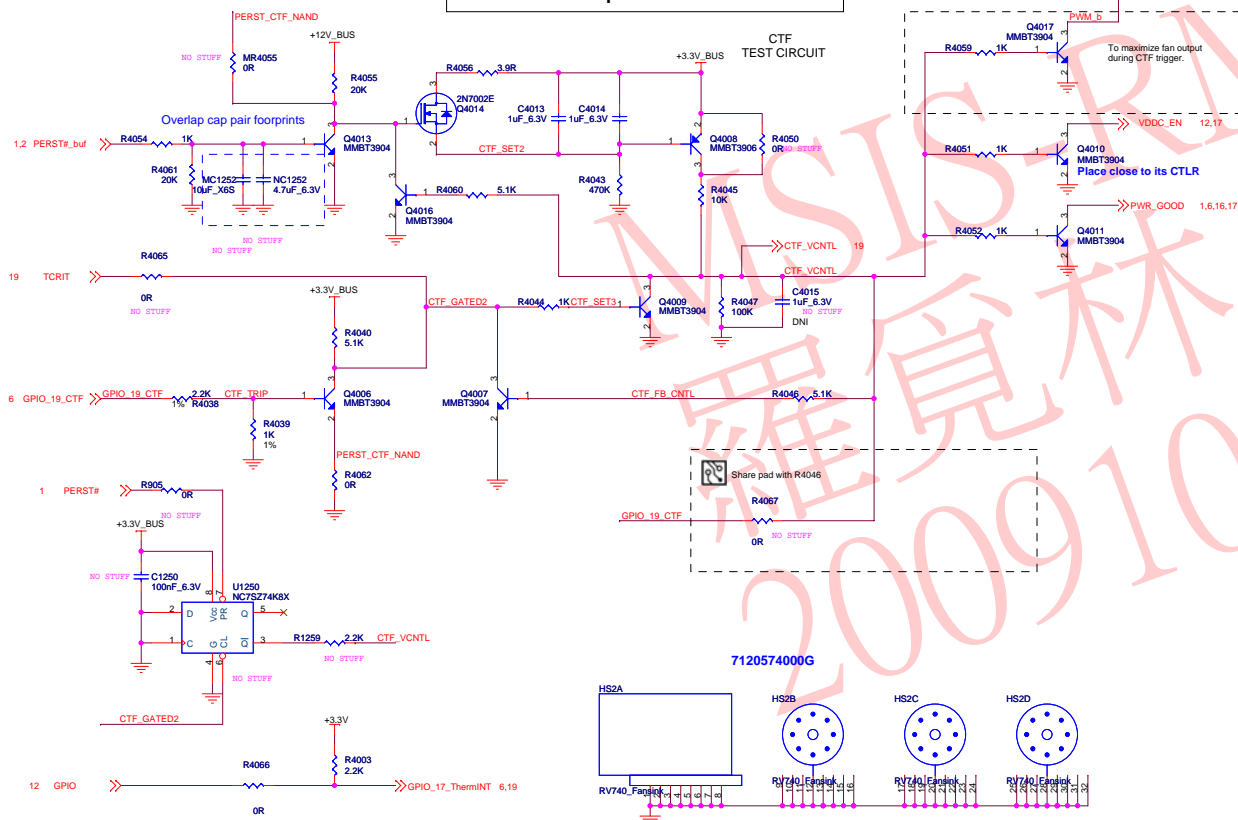
(16) Mechanical and Thermal Management



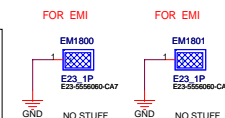
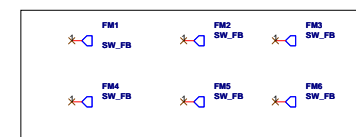
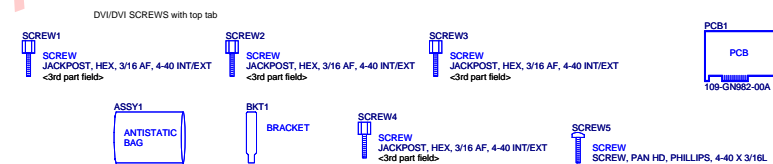
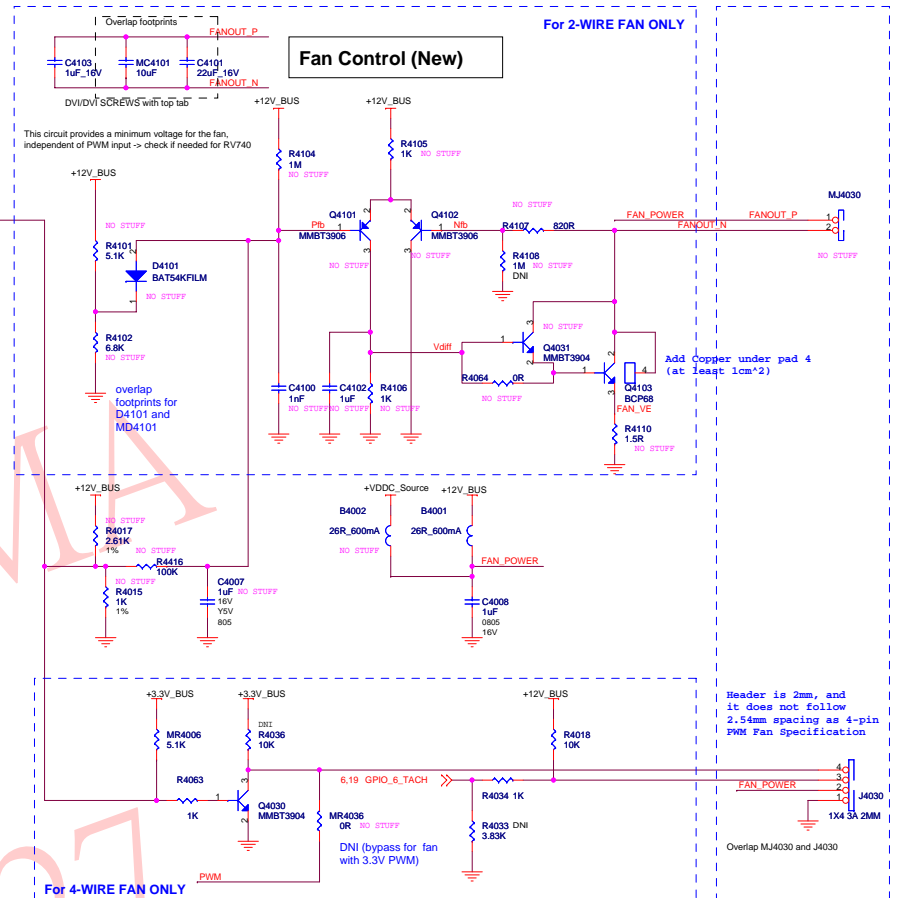
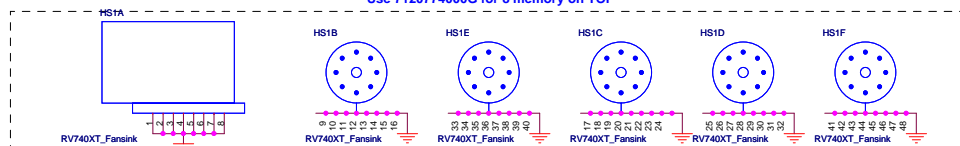
Warning: TS FDO is not 5V tolerant. MAX sink current 1.65mA


If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.

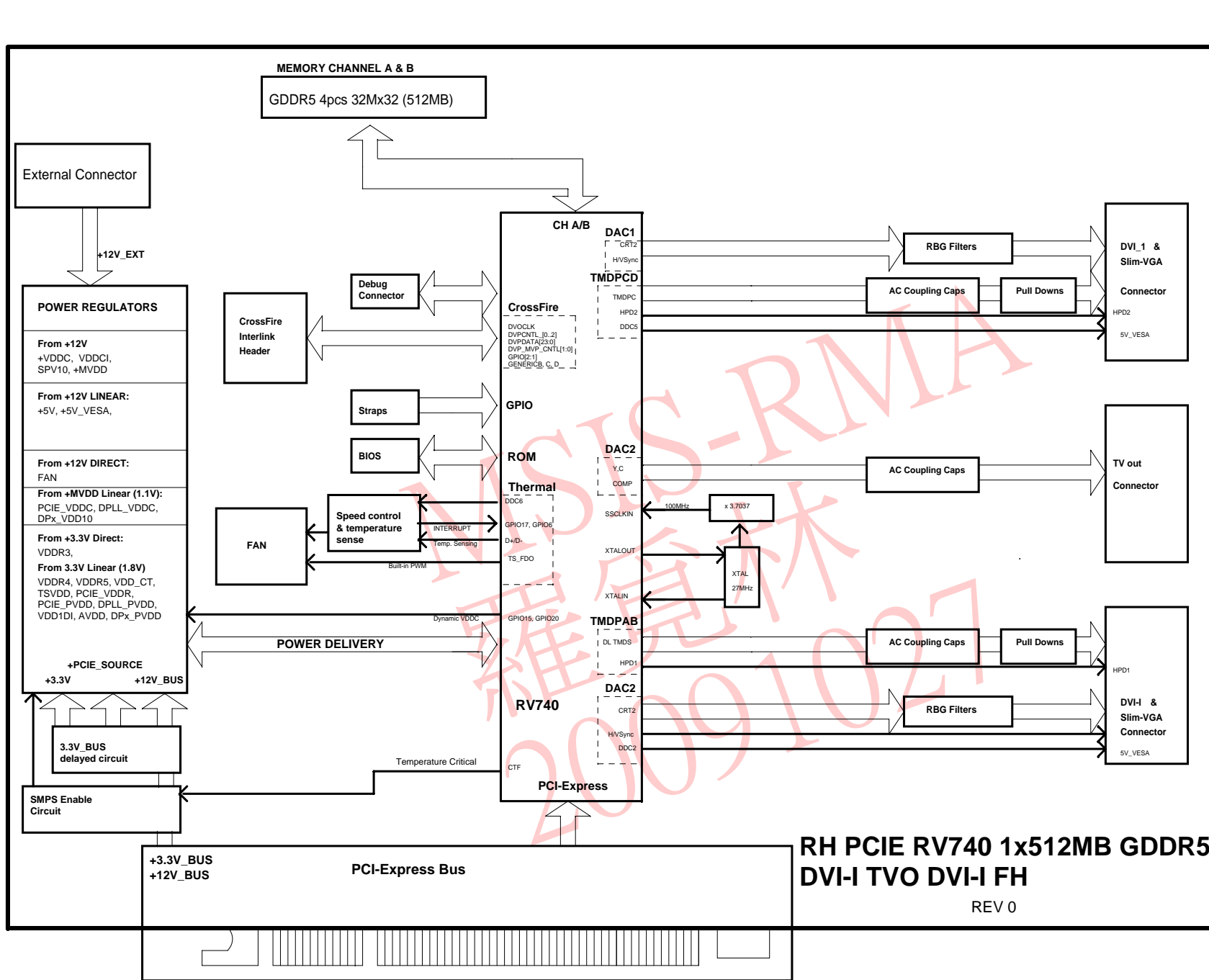
Critical Temperature Fault



Use 7120774000G for 8 memory on TOP



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<p>Title: RH RV740 GDDR5 DP-DP-DP DVI TRI</p>	
<p>Doc No: 105-B86300-00</p>	



**RH PCIE RV740 1x512MB GDDR5
DVI-I TVO DVI-I FH**
REV 0



RH RV740 GDDR5 DP-DP- DVII TRIAL

105-B86300-00A

Wednesday, May 13, 2009

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	09/01/06	Based on B743
	10	09/04/29	PAGE 7 : Remove TV function PAGE 9 : Change DVI to HDMI PAGE 12 :Change Inductor and CAP footprint, Remove Input CAP PAGE 13 :Change Inductor and CAP footprint, PAGE 14 : Change Inductor and CAP footprint

CAP footprint, Remove Input CAP
CAP footprint,
CAP footprint

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