

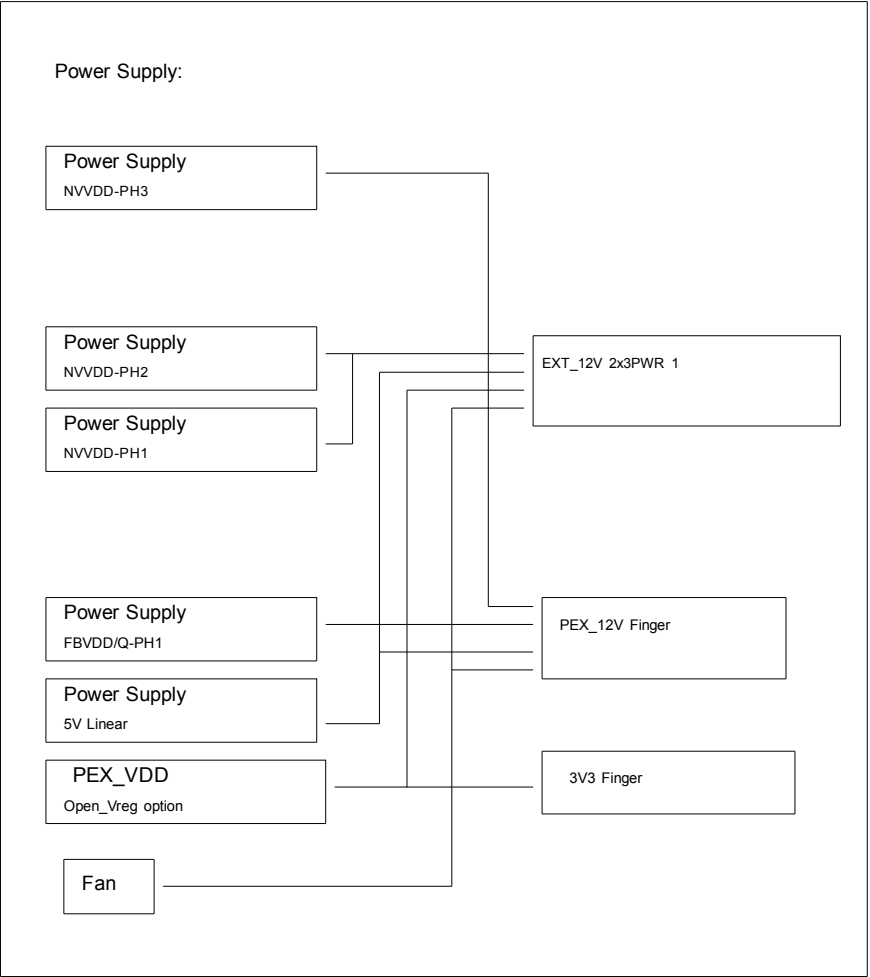
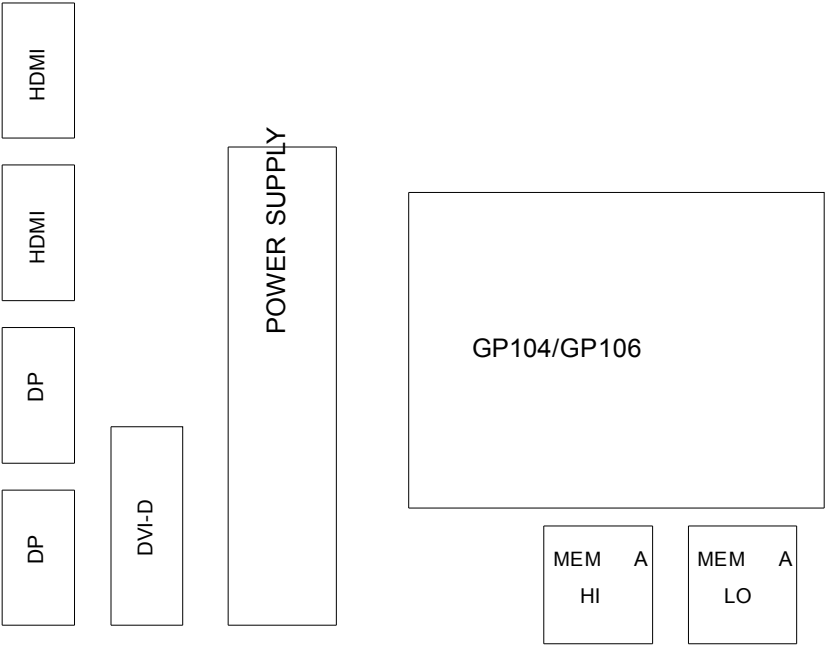
PG410 A01

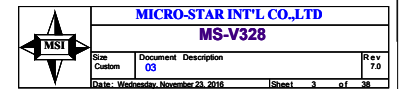
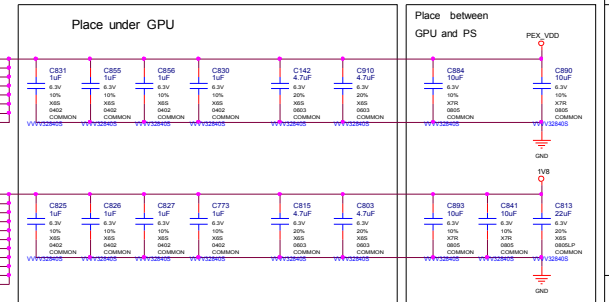
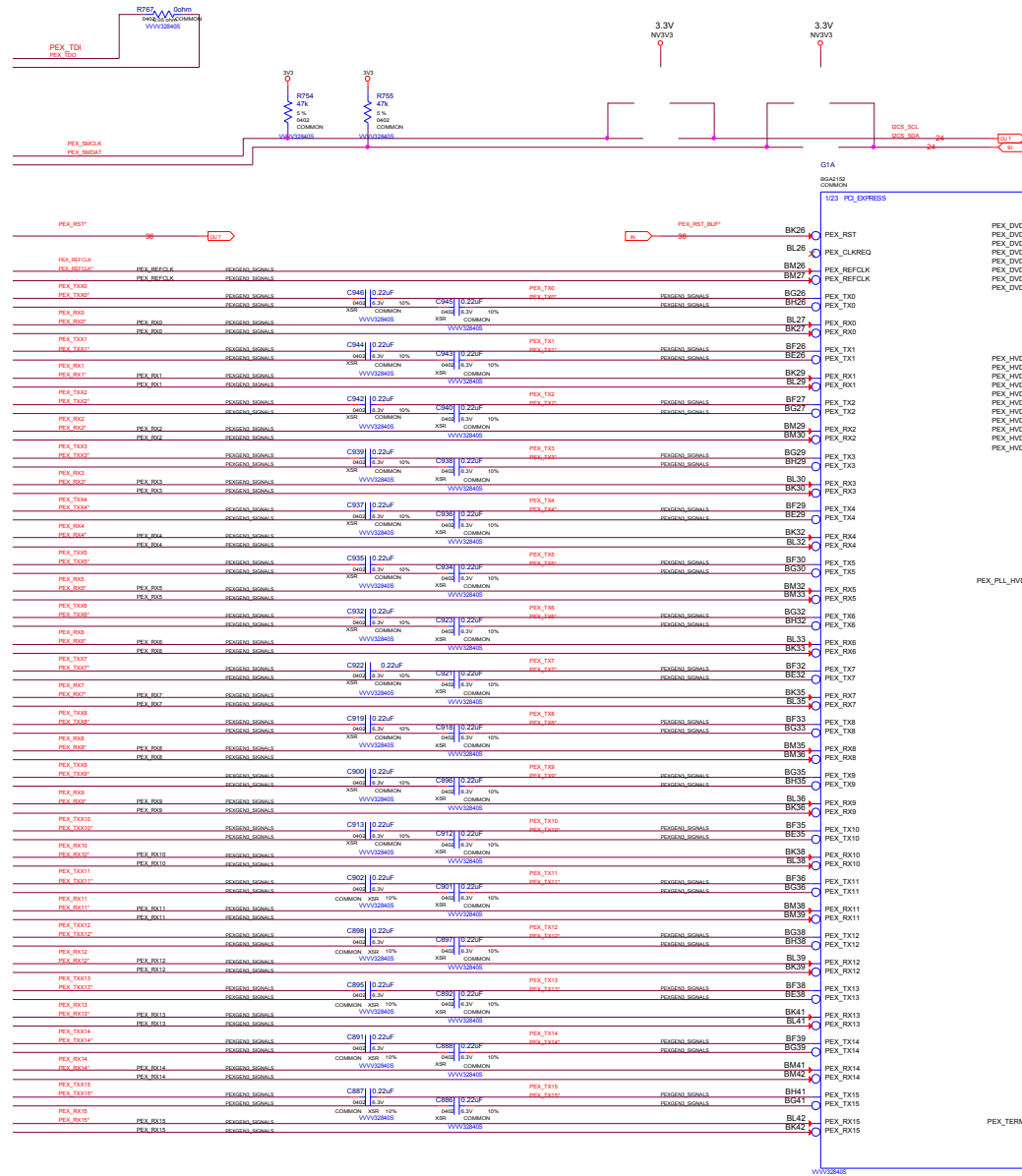
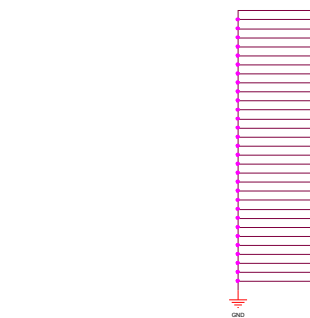
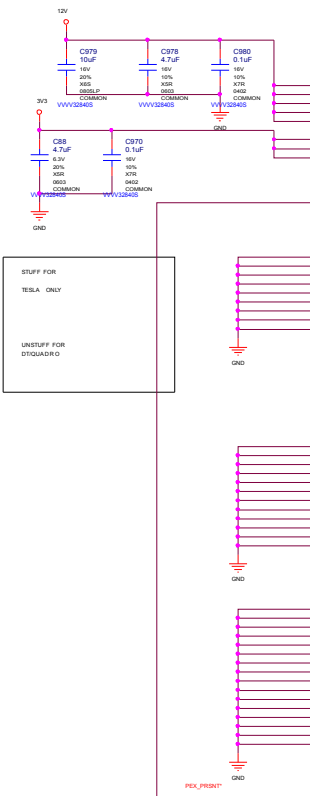
GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI + HDMI

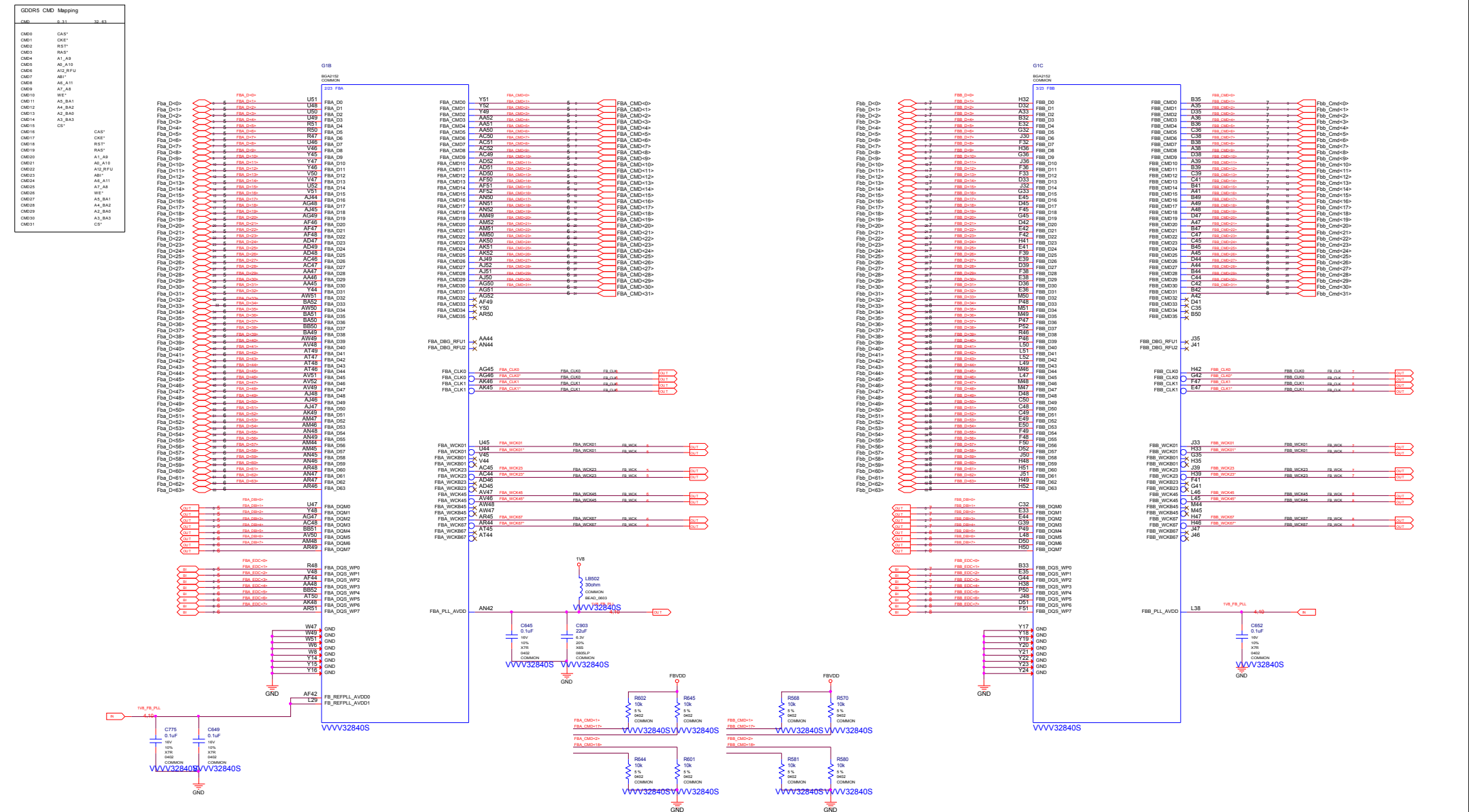
TABLE OF CONTENTS

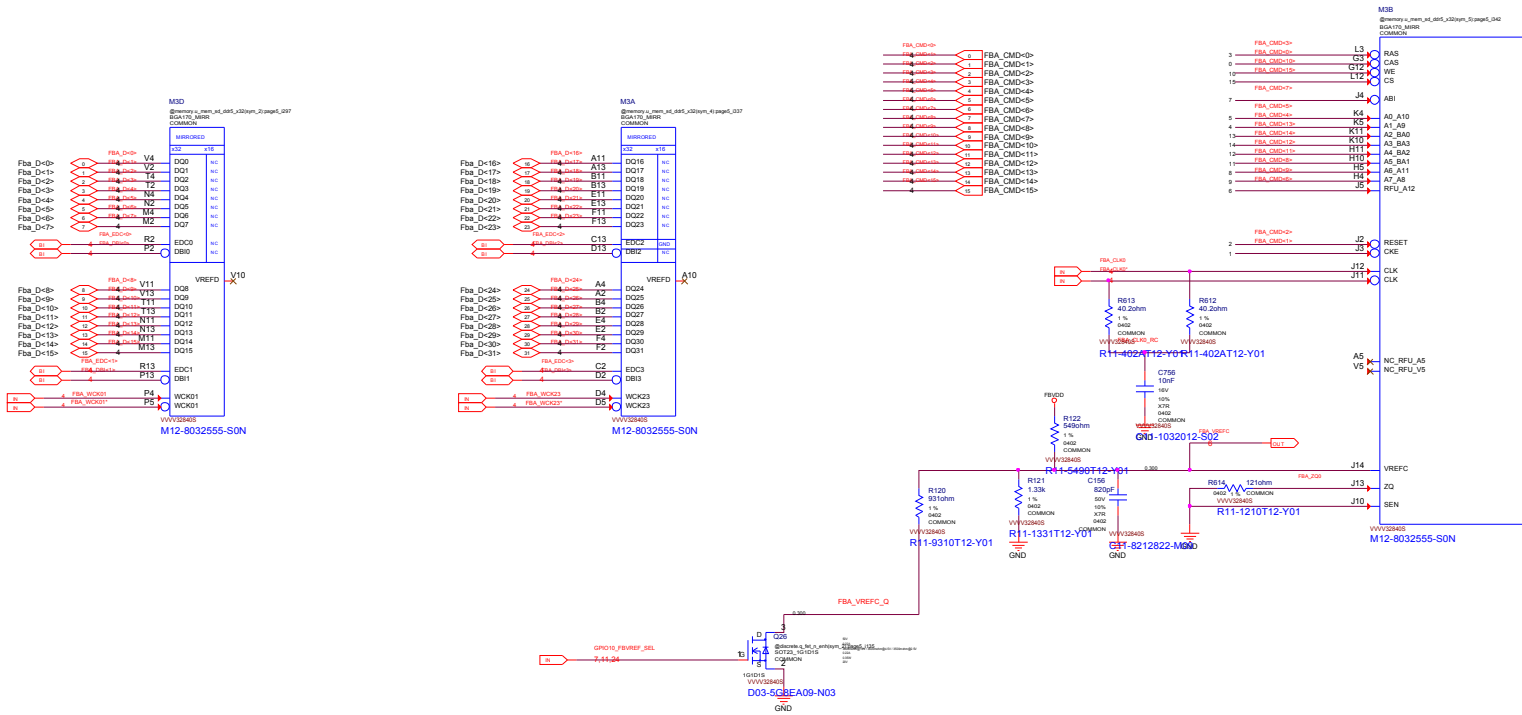
Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	GPU FB_AB
5	MEMORY: FBA[31:0]
6	MEMORY: FBA[63:32]
7	MEMORY: FBB[31:0]
8	MEMORY: FBB[63:32]
9	MEM FB_AB PWR
10	GPU FB_CD
11	MEMORY: FBC[31:0]
12	MEMORY: FBC[63:32]
13	MEMORY: FBD[31:0]
14	MEMORY: FBD[63:32]
15	MEM FB_CD PWR
16	GPU PWR & GND
17	GPU Decoupling
18	IFPAB DVI-D-DL
19	IFPE DP
20	IFPF DP
21	IFPC HDMI
22	IFPD HDMI
23	MIOA/B Interface and Frame Lock
24	MISC1: Fan, Thermal, JTAG, GPIO,STEREO
25	MISC2: ROM, XTAL,STRAPS

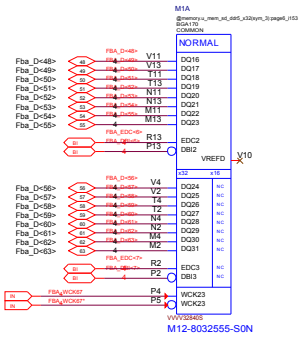
Page	Description
26	PS: 1V8_PLL, 1V8_AON
27	PS: 5V, PEX_VDD
28	PS: NV3V3, NV12V
29	PS: FBVDD
30	PS: NVVDD Controller
31	PS: NVVDD Phase 1,2 & 3
32	PS: NVVDD Rail Balance Login & Dynamic Phase
33	PS: Input, Filtering, and Monitoring
34	PS: 12V Power Steering,PSI Control & LED
35	PS: Shut Down and Sequencing
36	PS: GC6 MISC
37	MECH
38	Change History

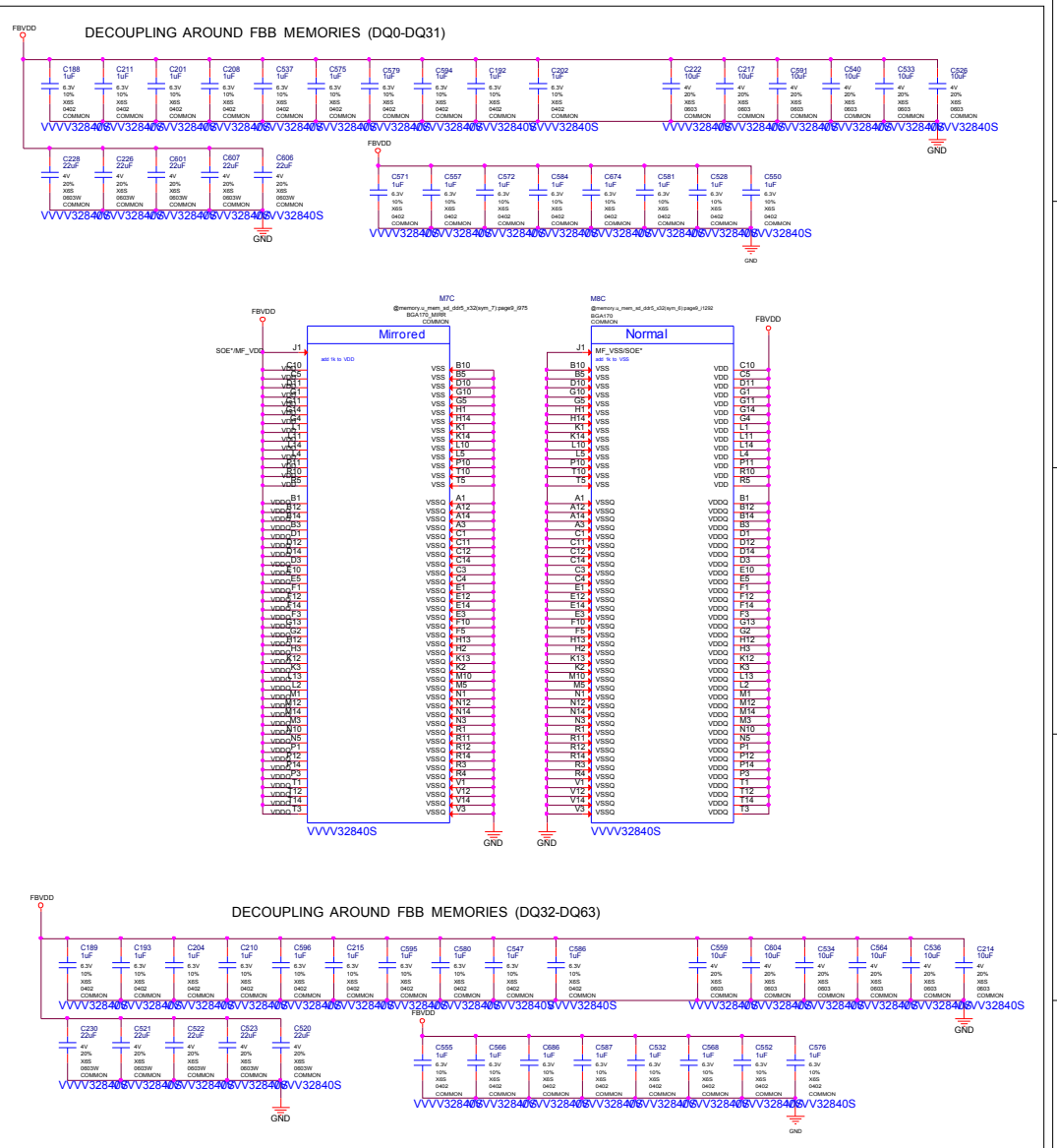
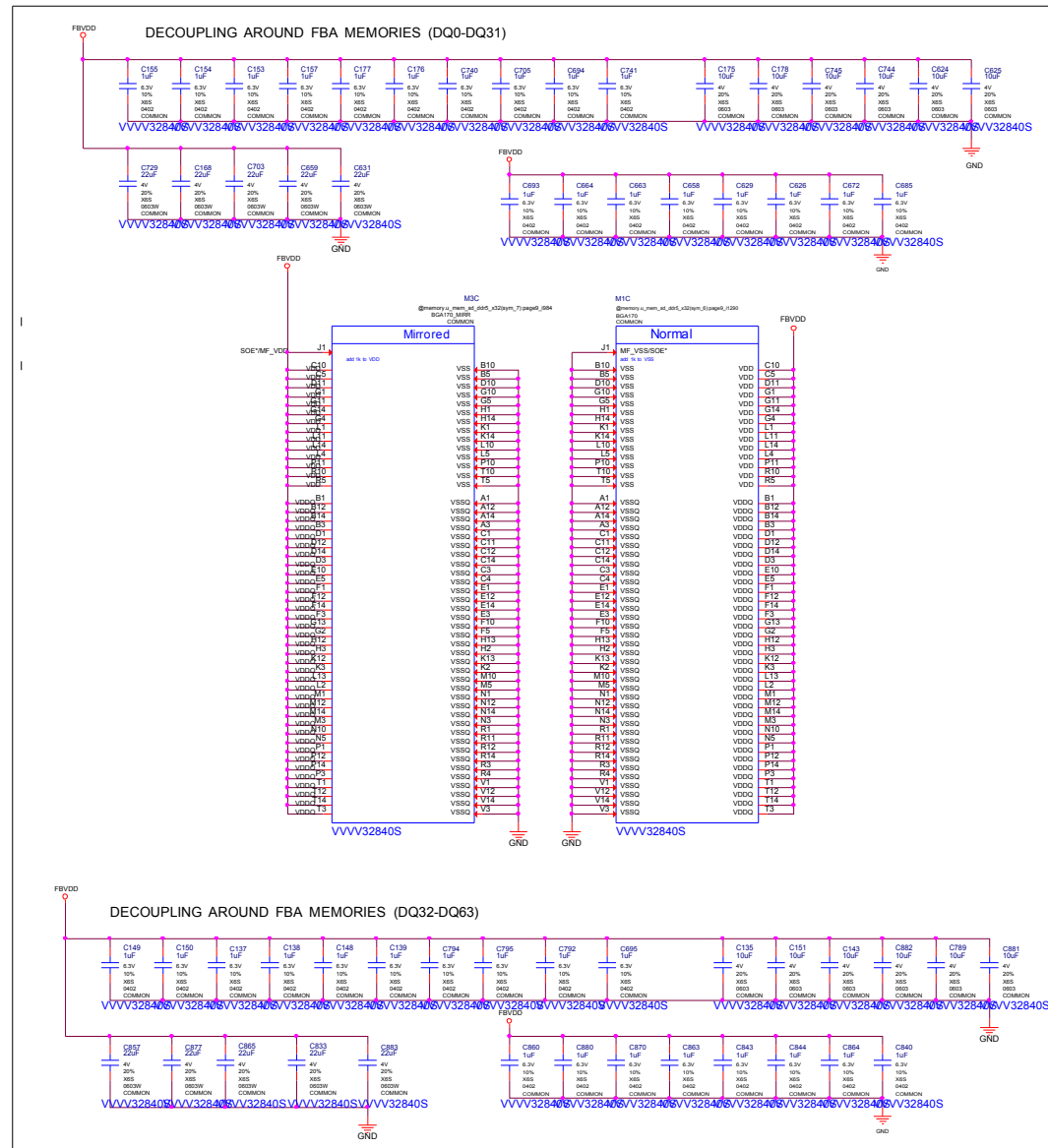










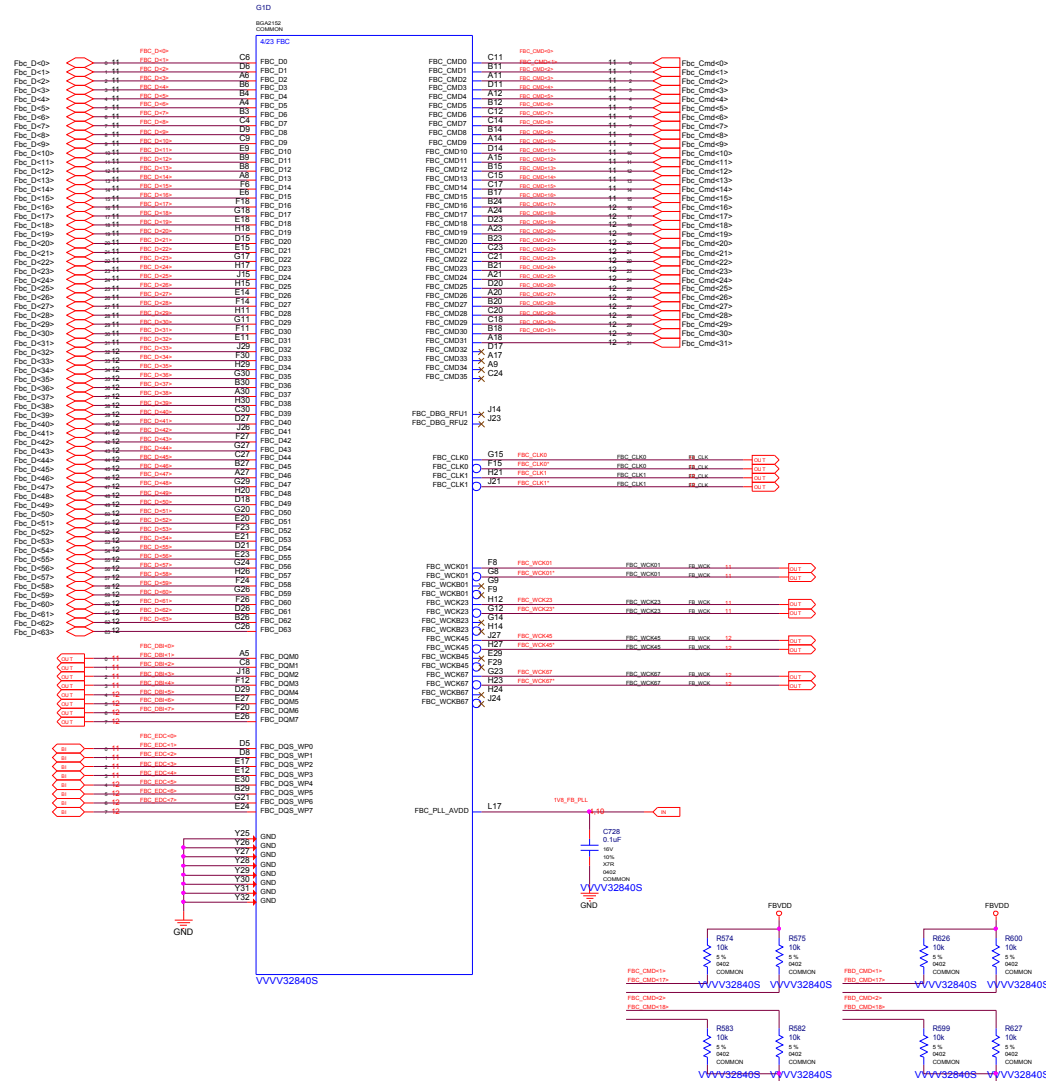


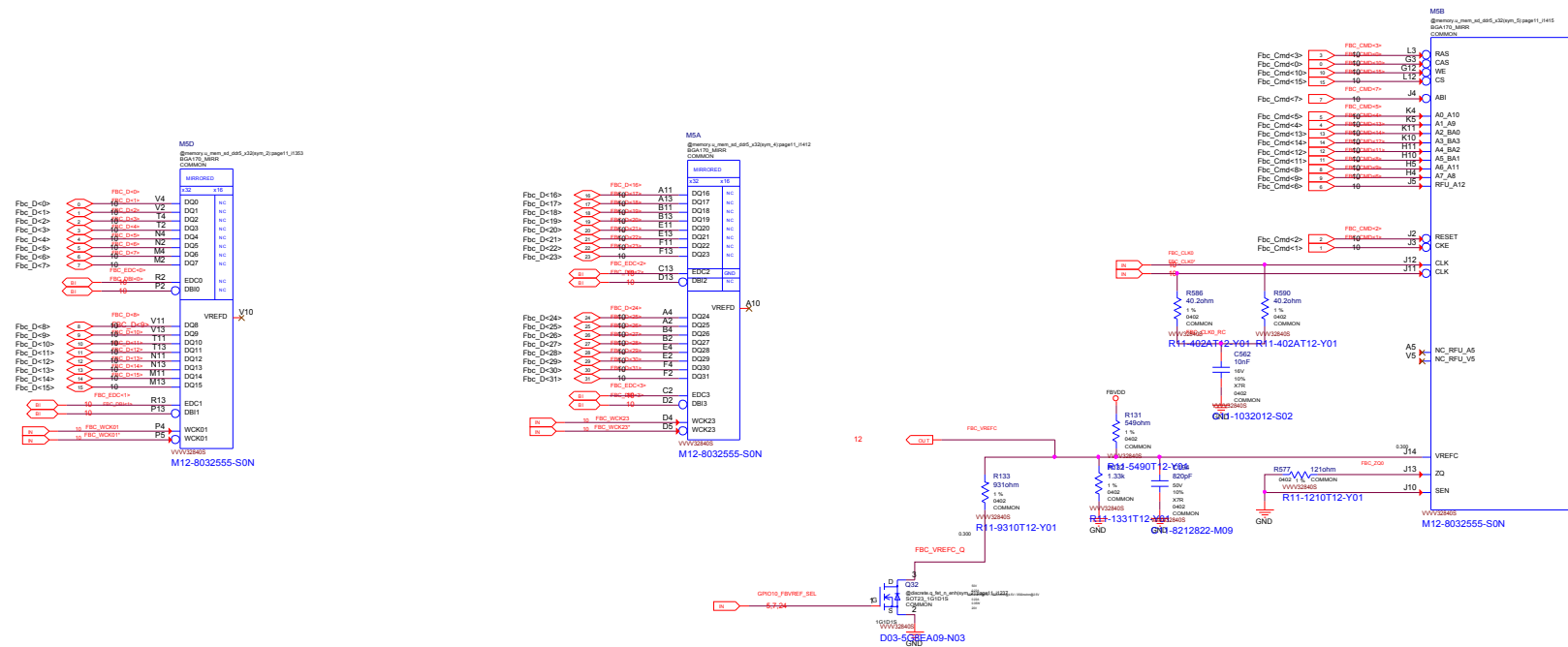
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GDOR5 CMD Mapping


CMD	0-31	32-63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A0	
CMD5	AS_A10	
CMD6	A02_RFU	
CMD7	AB*	
CMD8	AA_A11	
CMD9	A7_A0	
CMD10	WE*	
CMD11	AS_BA1	
CMD12	AA_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		BA0*
CMD20	A1_A0	
CMD21	AS_A10	
CMD22	A02_RFU	
CMD23	AB*	
CMD24	AA_A11	
CMD25	A7_A0	
CMD26	WE*	
CMD27	AS_BA1	
CMD28	AA_BA2	
CMD29	A2_BA0	
CMD30	A3_BA3	
CMD31	CS*	





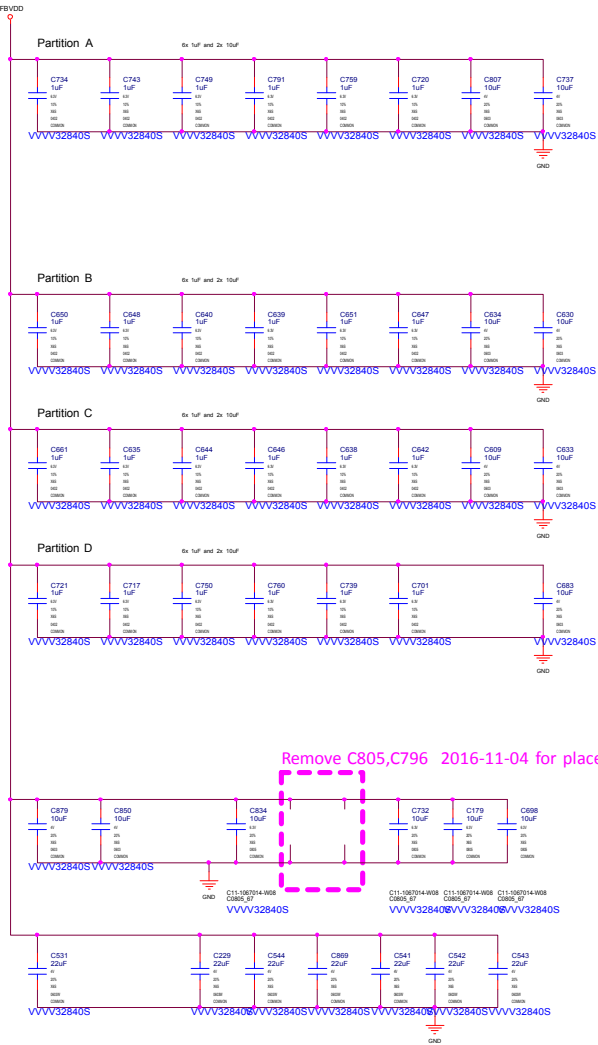


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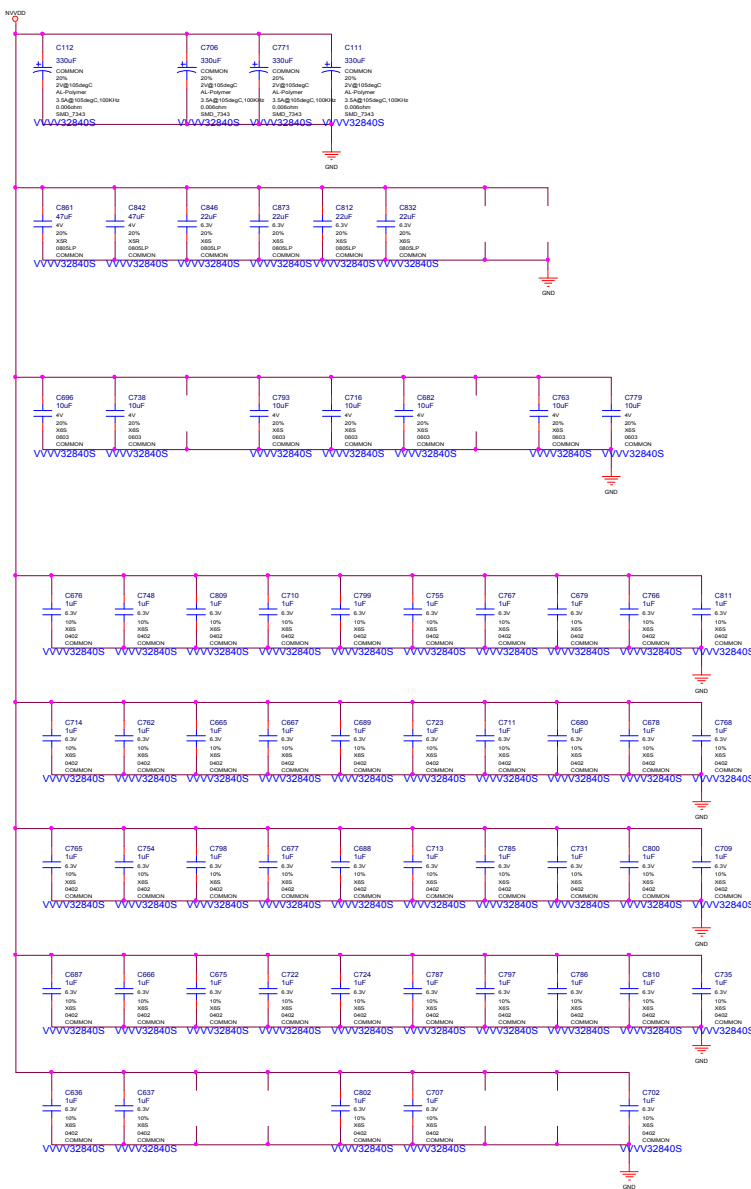


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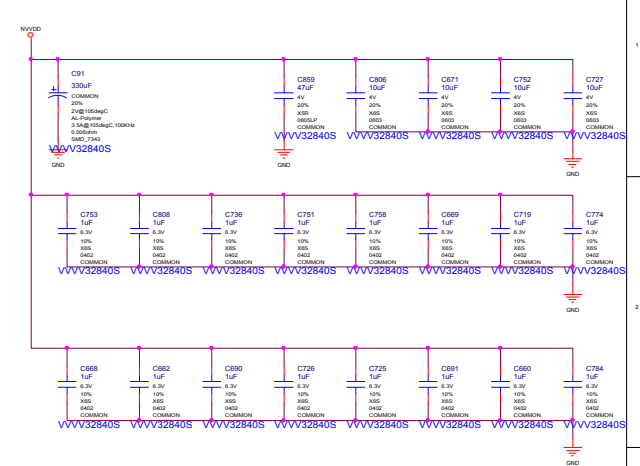
FBVDD



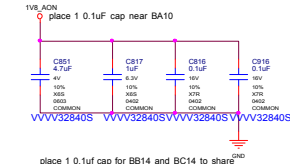
NVDD



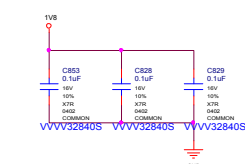
NVDD

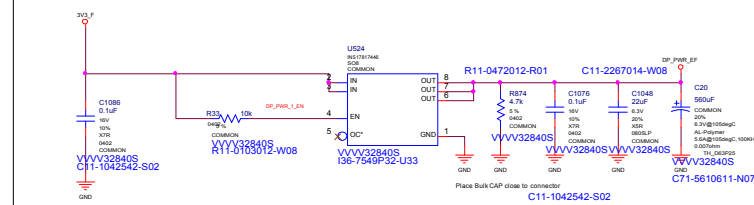


1V8_AON

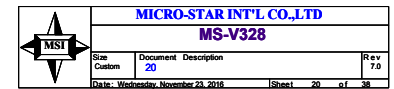


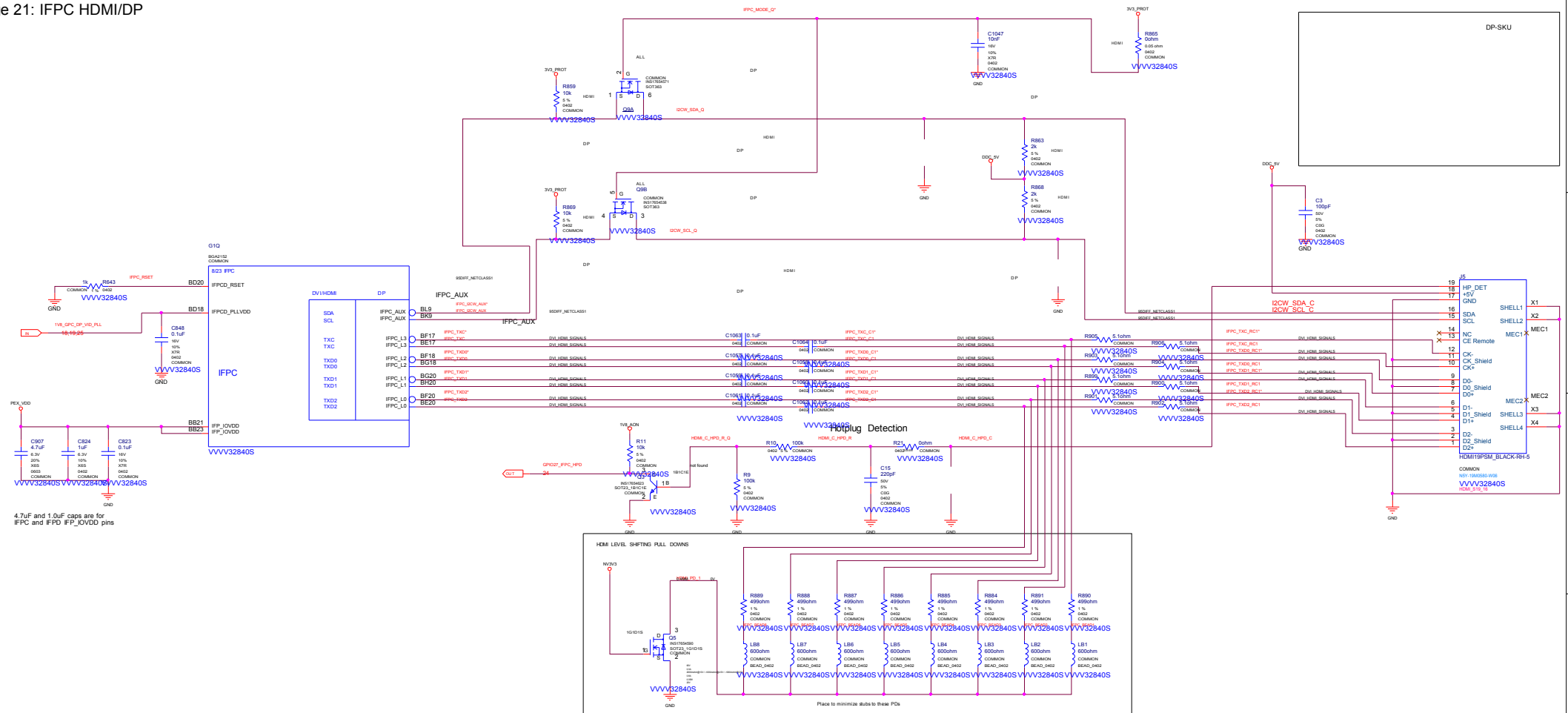
1V8_MAIN





Add DP

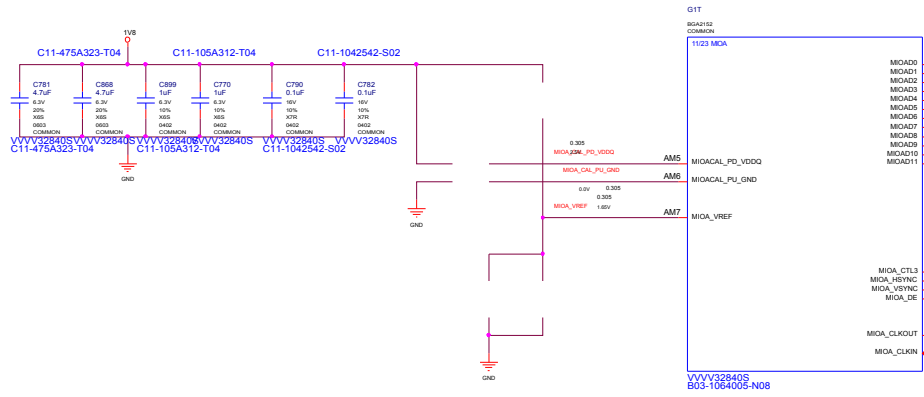




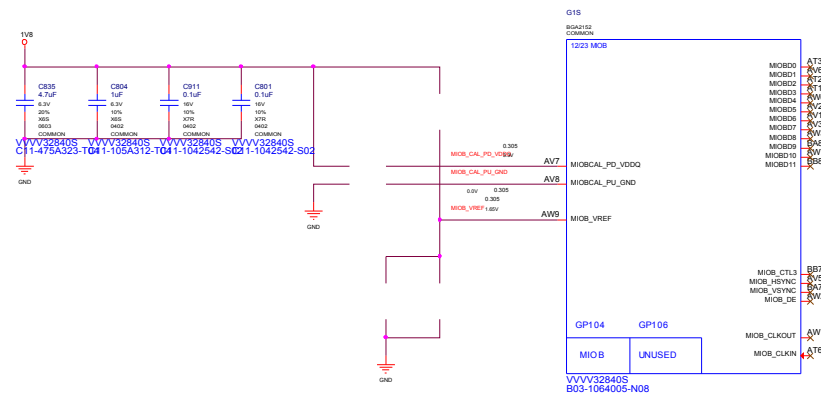
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Pad Overlap R1042 & R1043



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

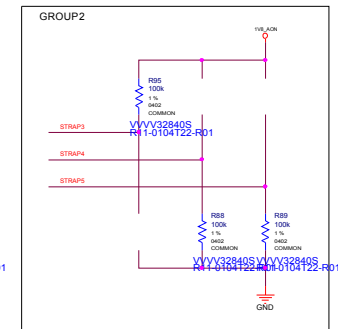
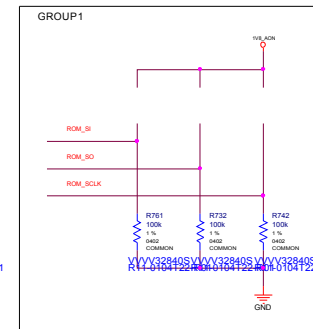
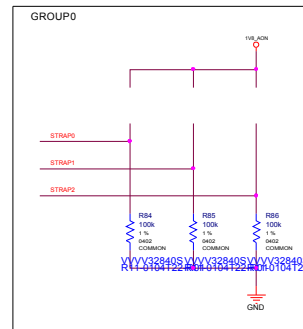
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

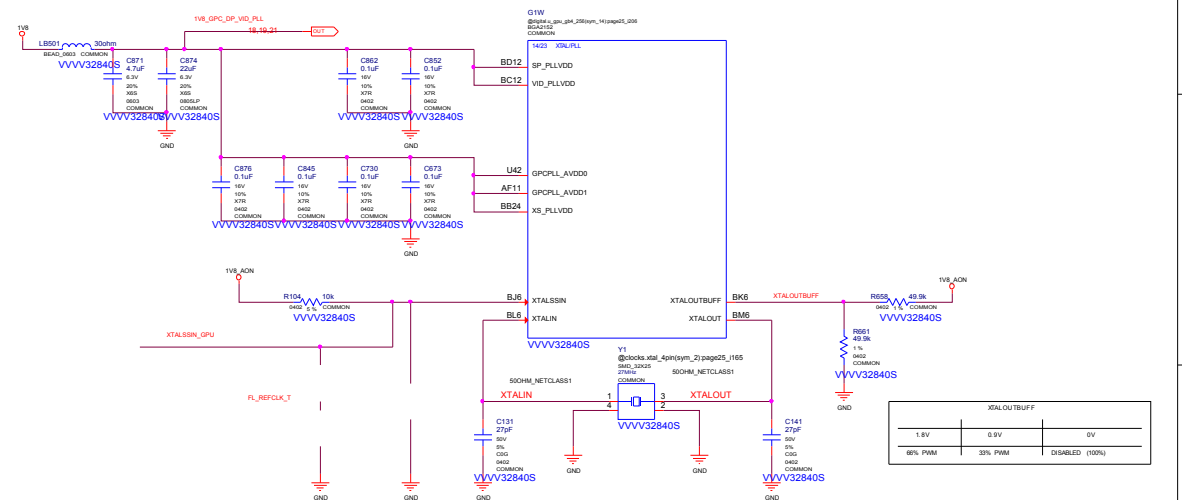
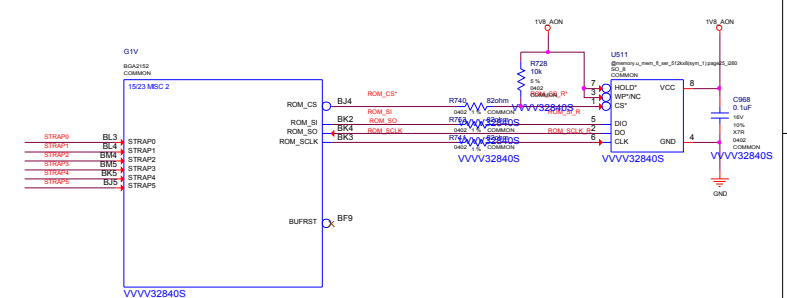
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

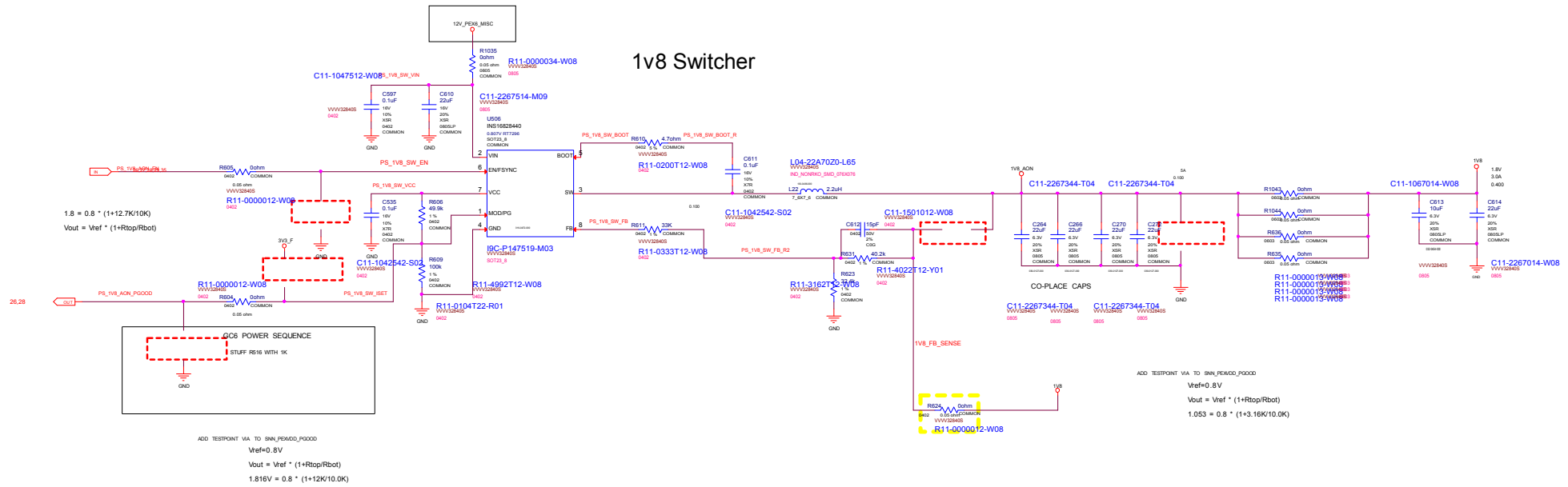



CFG(3:0)	Config	Width	Vendor
0000	256Mx32	256-bit	Samung
0001	256Mx32	256-bit	Micron
0010	256Mx32	256-bit	Hynix
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		

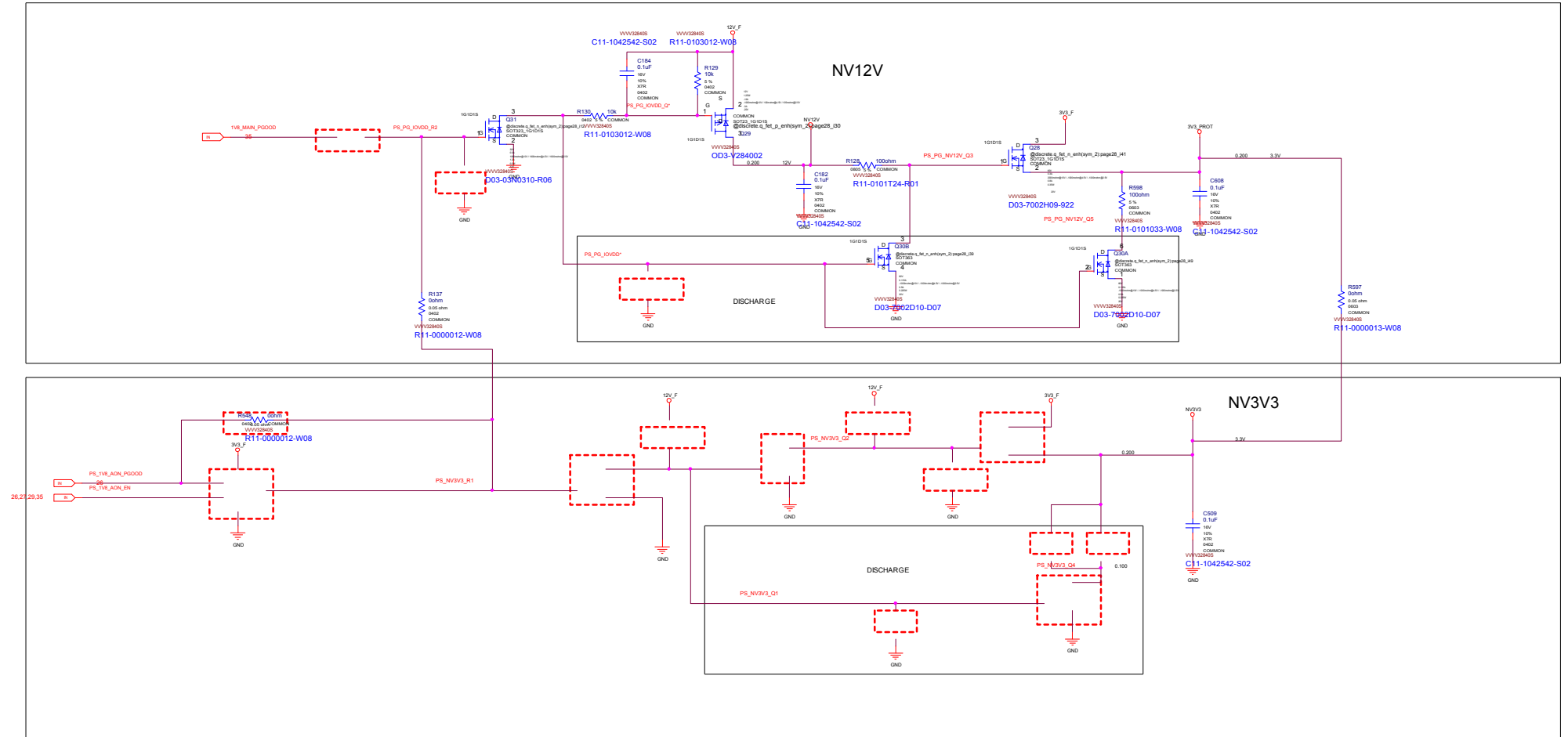


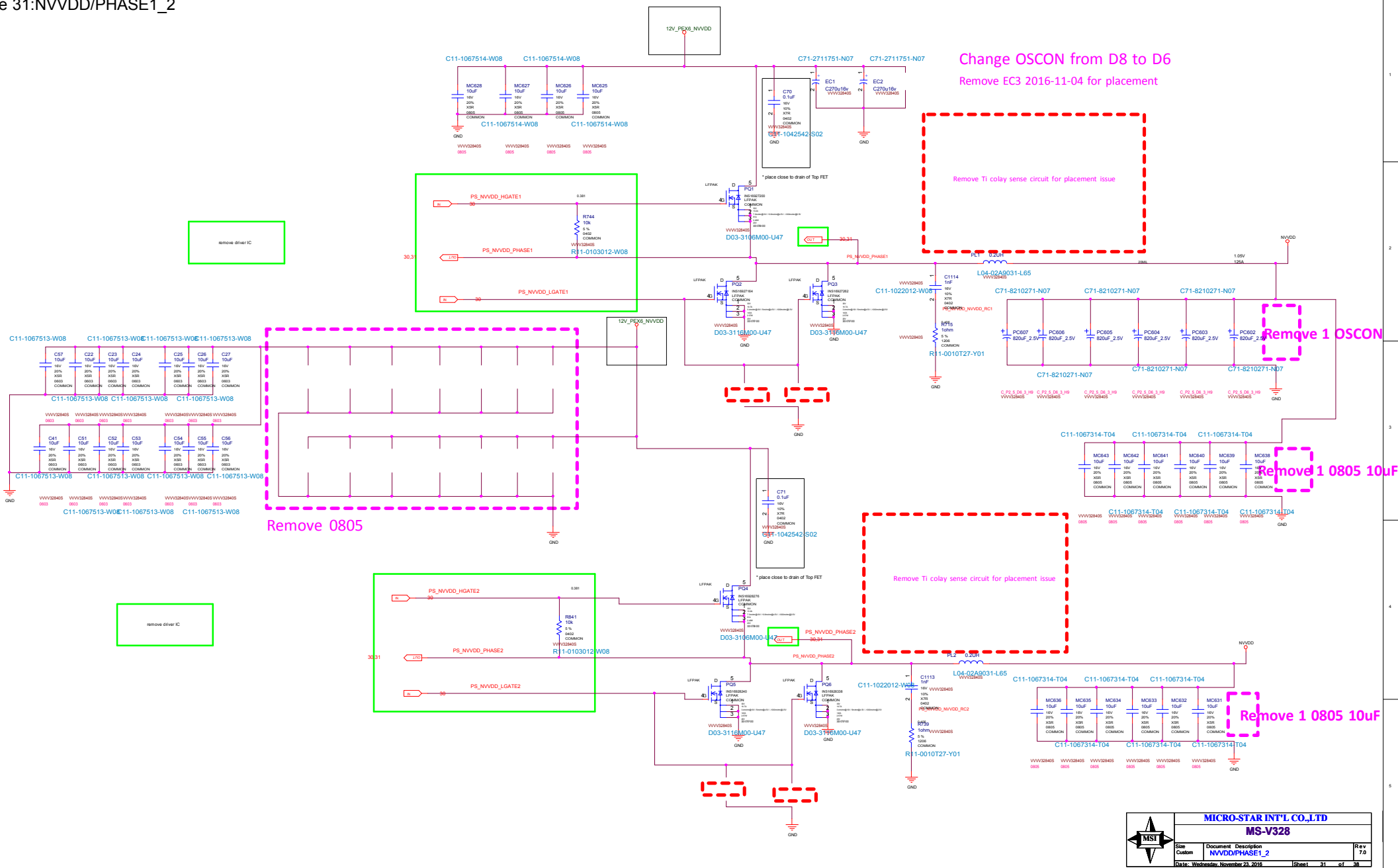
XTALOUT/BUFF		
1.8V	0.9V	0V
60% PWM	30% PWM	DISABLED (100%)

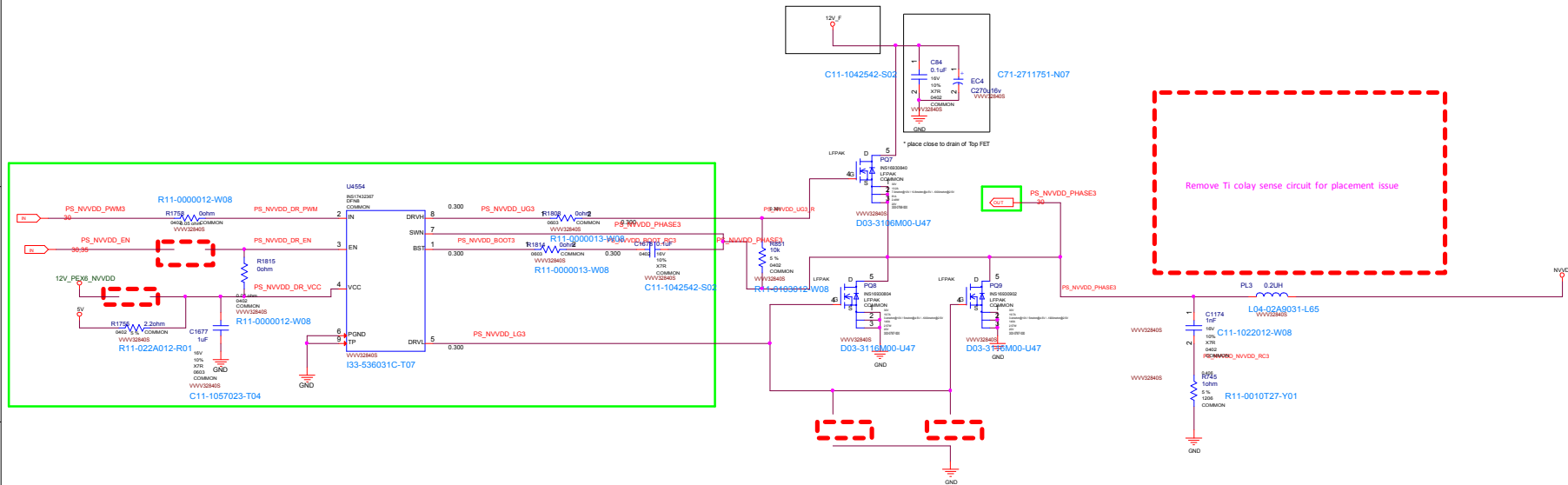
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			MS-V328	
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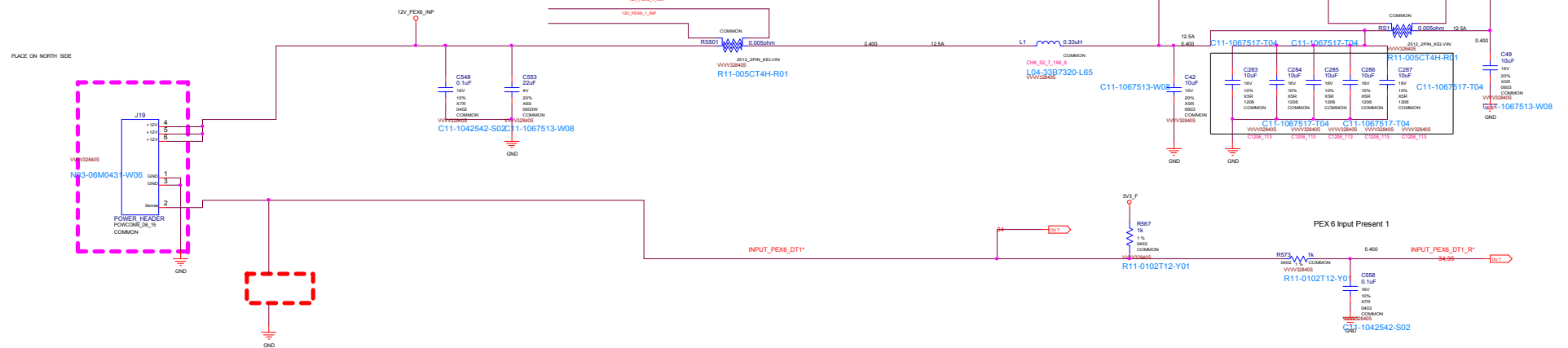
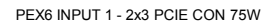
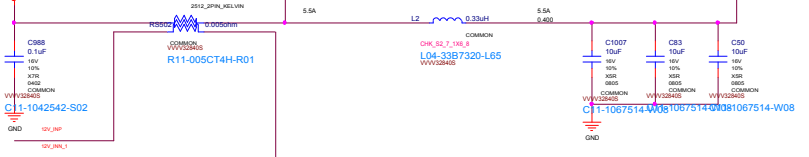
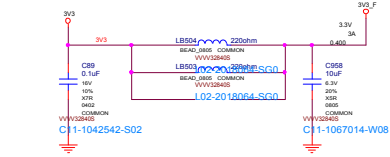
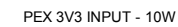
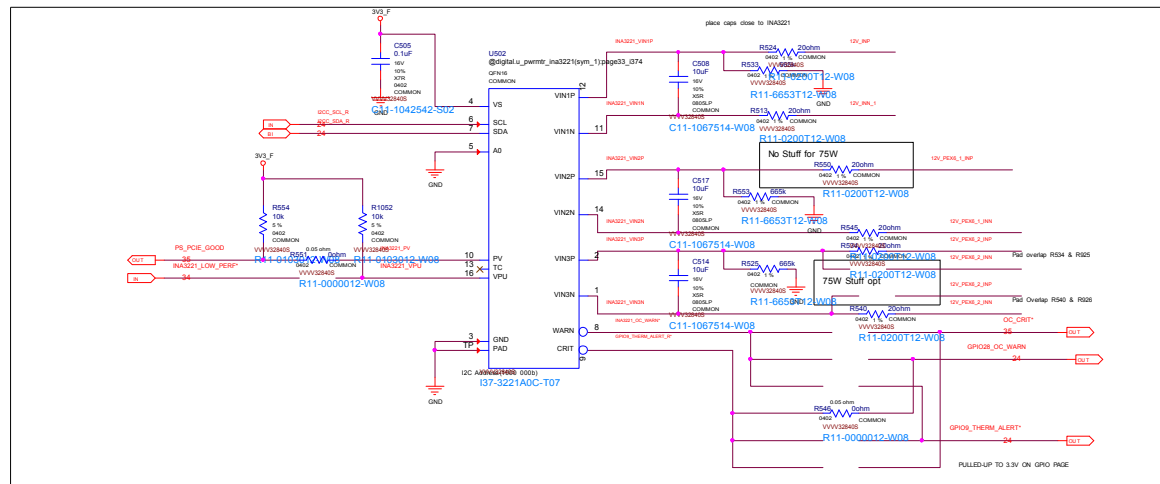






CORE 90A /3 =30A
 CORE 1 - EXT 6
 CORE 2 - EXT 6
 CORE 3 - BUS
 MEM 30A- BUS
 -BUS WARRING-

CORE 90A /4 =22.5A
 CORE 1 - EXT 6
 CORE 2 - EXT 6
 CORE 3 - BUS
 CORE 4 - EXT 6
 MEM 30A- BUS



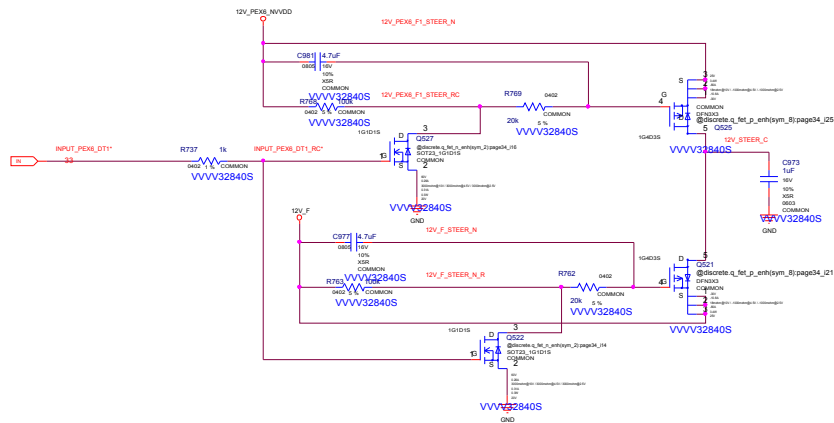
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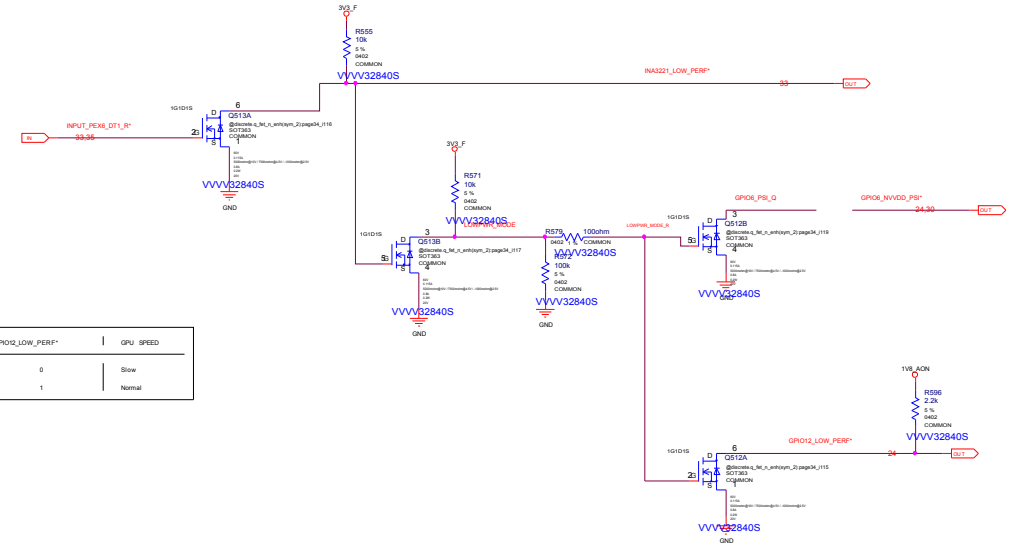
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12V CURRENT STEERING (UNDER POWER BOOT):

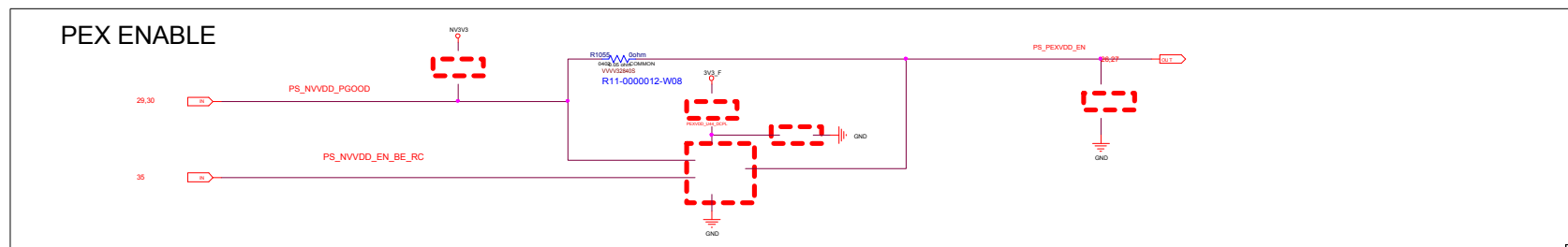
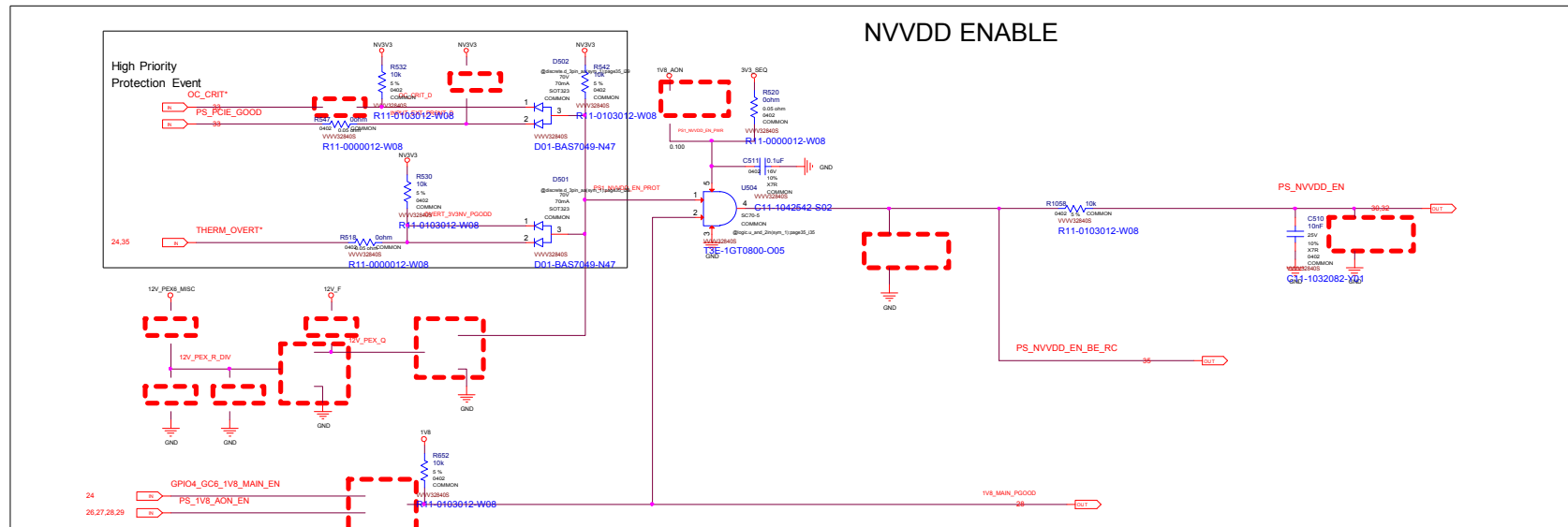
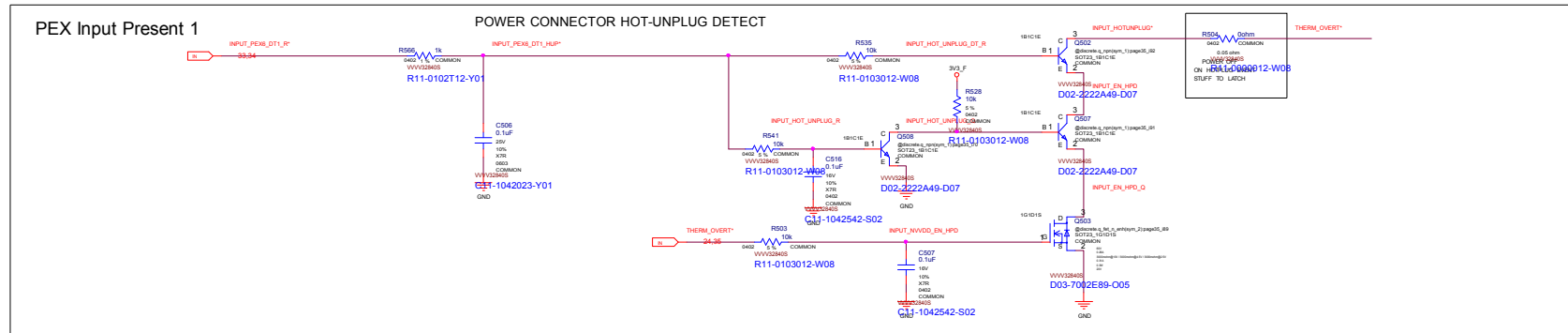
GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

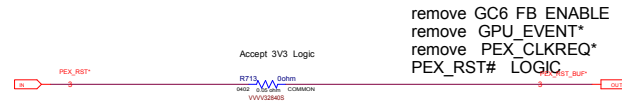


PEX Input - Power Level/PSI* Control



GeForce Logo LED





remove 5V LED NET

Brackets:



Remove: MEC12/MEC13/MEC14/MEC15/MEC11/MEC8/MECG2/MECG1

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Page38: Change History

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Page 18: Change DVI connector to high rise type from N5B-24F0521-H06 to N5B-24F0691-A43

Page 19: Add IFPE DP (N5W-20M0820-A43)

Page 20: Add IFPF DP (N5W-20M0820-A43)

Page 21: Change HDMI connector from N5Y-19M0760-W06 to N5Y-19M0580-W06

Page 22: Change DP to HDMI from V328-62 (N5Y-19M0580-W06)

Page 26: Remove 1v8, PEX LDO circuit, Check 1v8 with V328-31-030

Page 27: Check PEX & PEX Discharge with V328-31-030

Page 31:

Input: change OSCON from D8 to D6 and remove 0805 CoLay circuit

Output: Remove 1 Oscon and 2 0805 10uF cap

Page 33: Change 6pin power header to reverse type (N93-06M0431-W06)

Page 17: Remove C805,C796 for placement 2016-11-04

2016-11-04

Page 31: Remove EC3 for placement

2016-11-07

Page 37: Change BKT back to 2 hole

2016-11-15


Page 29: Change PR519 from 1206 to 0805 for snubber placement

2016-11-15

Page 27: Change PEX LB11 from L04-01071K0-M26 to L04-01073P0-L65

Page 27: Change 5V L502 from L04-47A70L0-T36 to L04-47A70Q0-L65

Page 26: Change 1v8 L22 from L04-22A70W0-T15 to L04-22A70Z0-L65

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