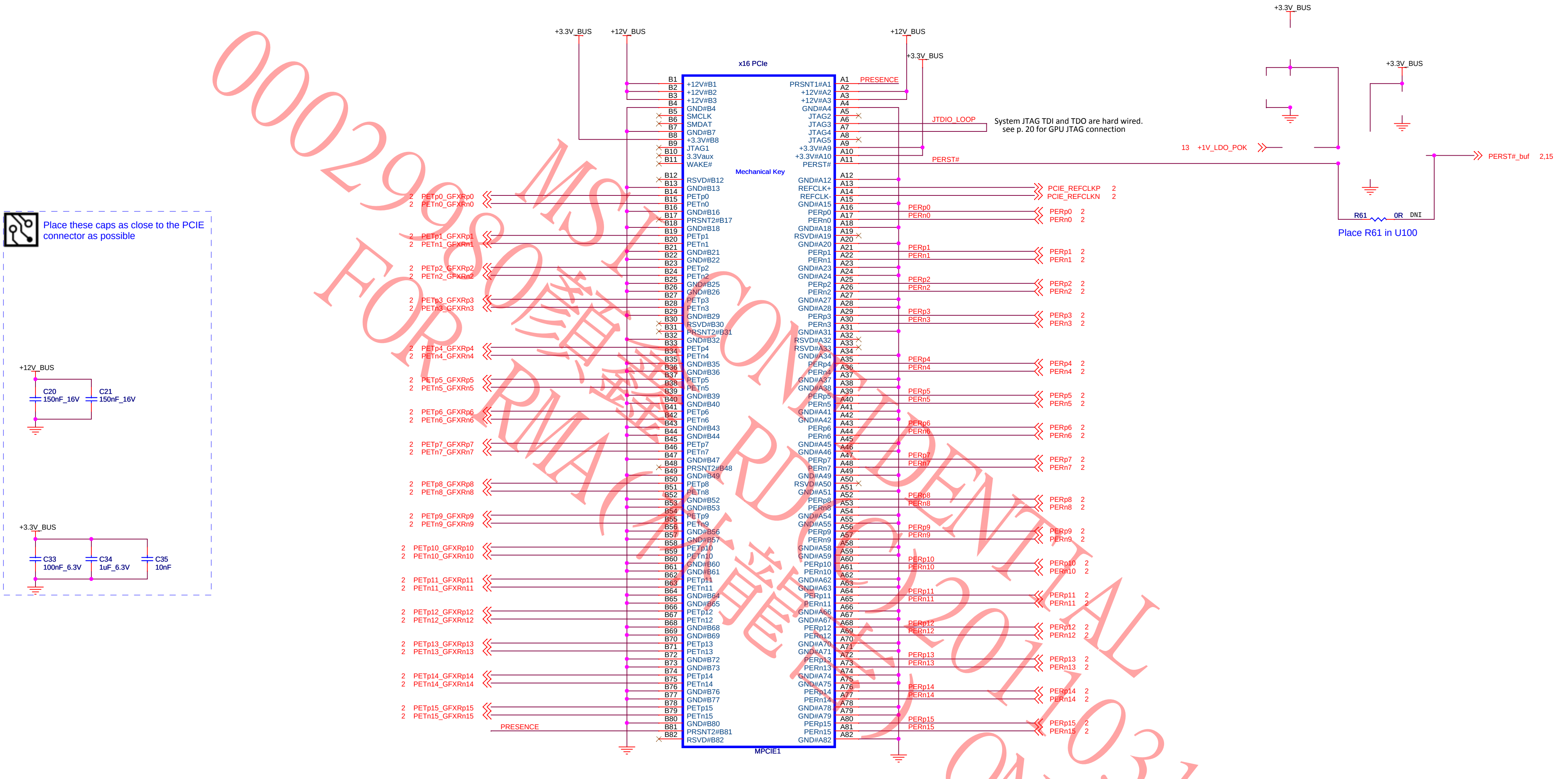
PCI-EXPRESS EDGE CONNECTOR

CEDAR SS



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
(symbol)	DIGITAL GROUND
(symbol)	ANALOG GROUND
BUO	BRING UP ONLY

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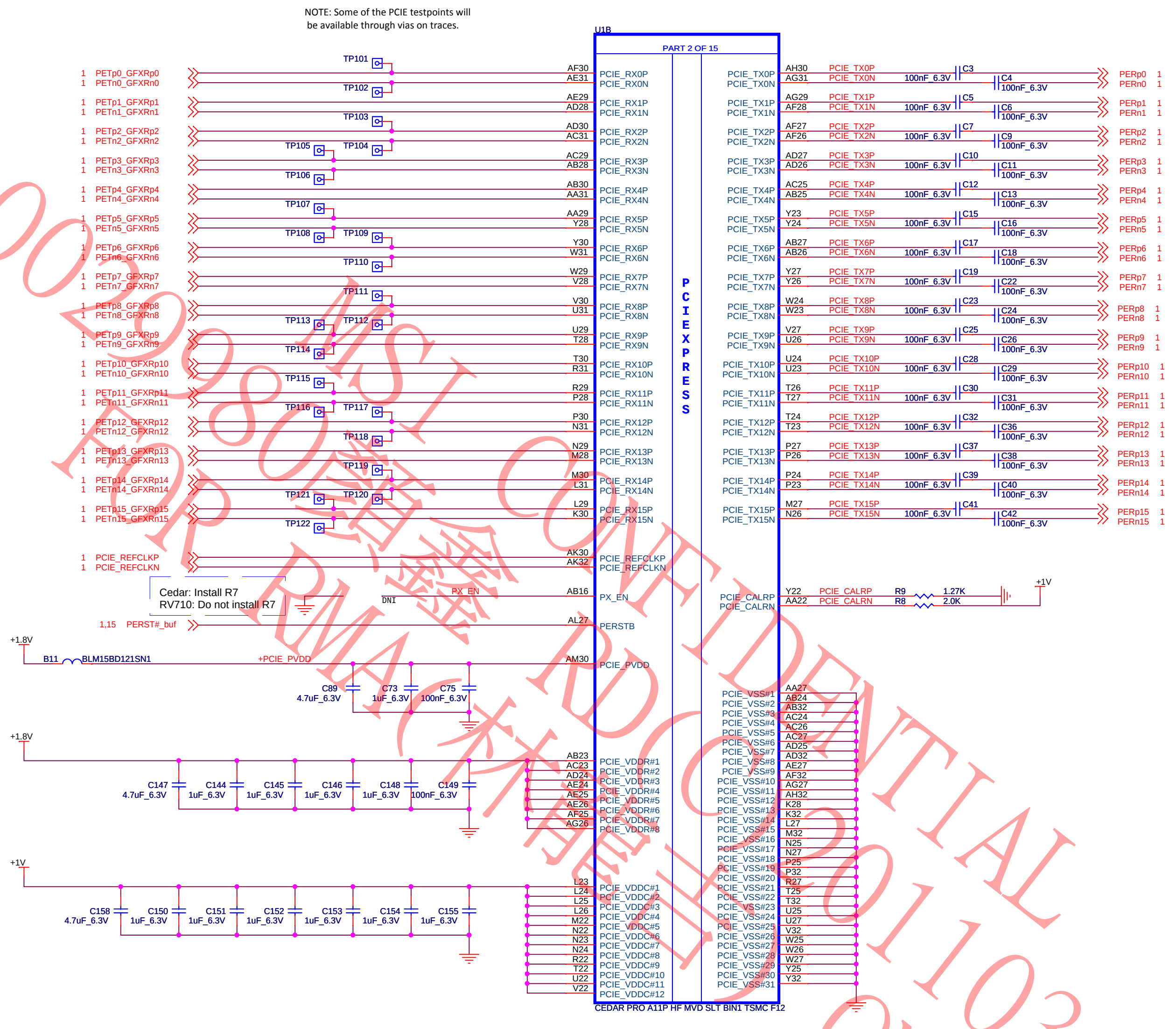
CEDAR PCIe Interface



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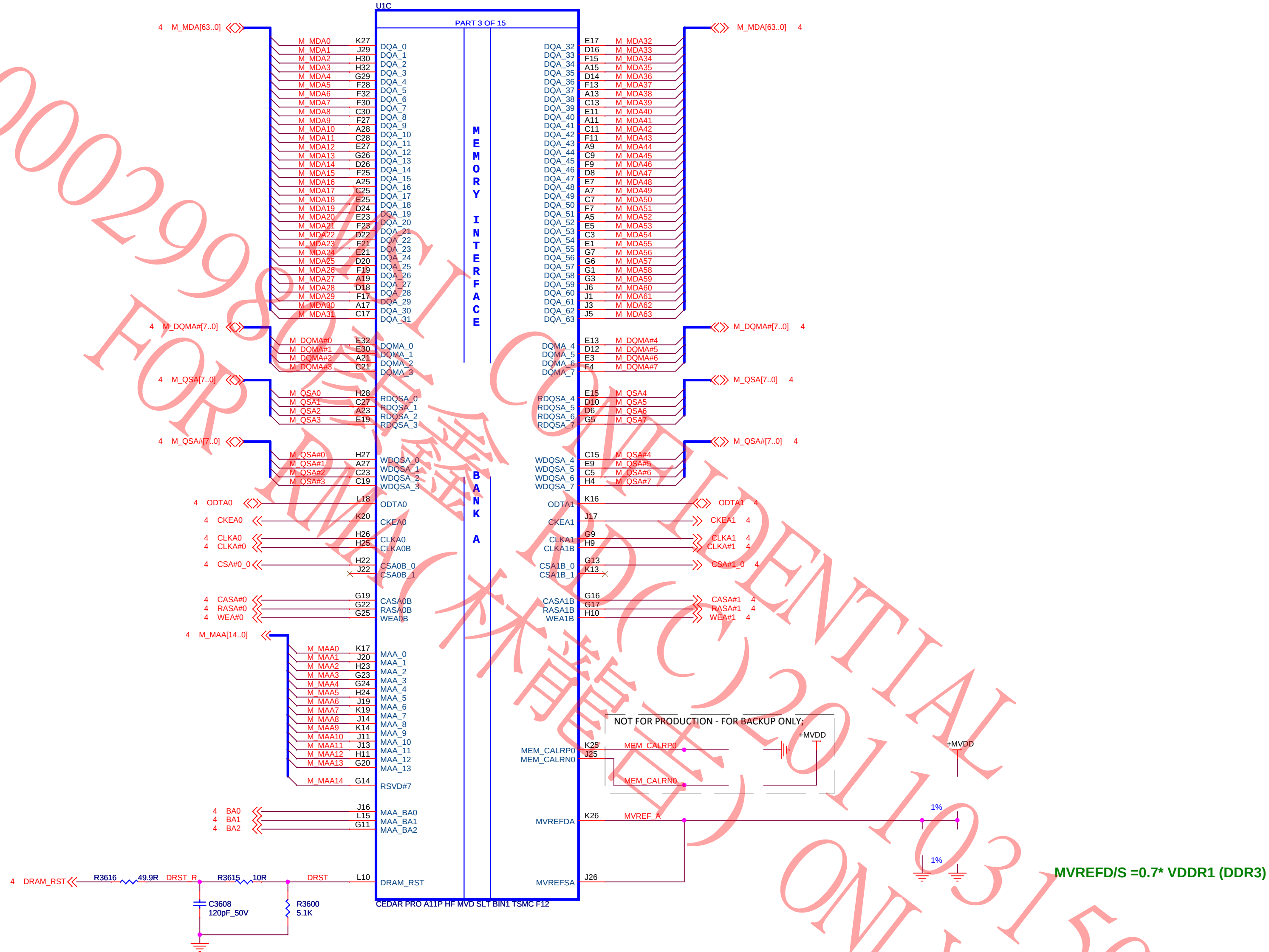
CEDAR MEM Interface Ch A&B



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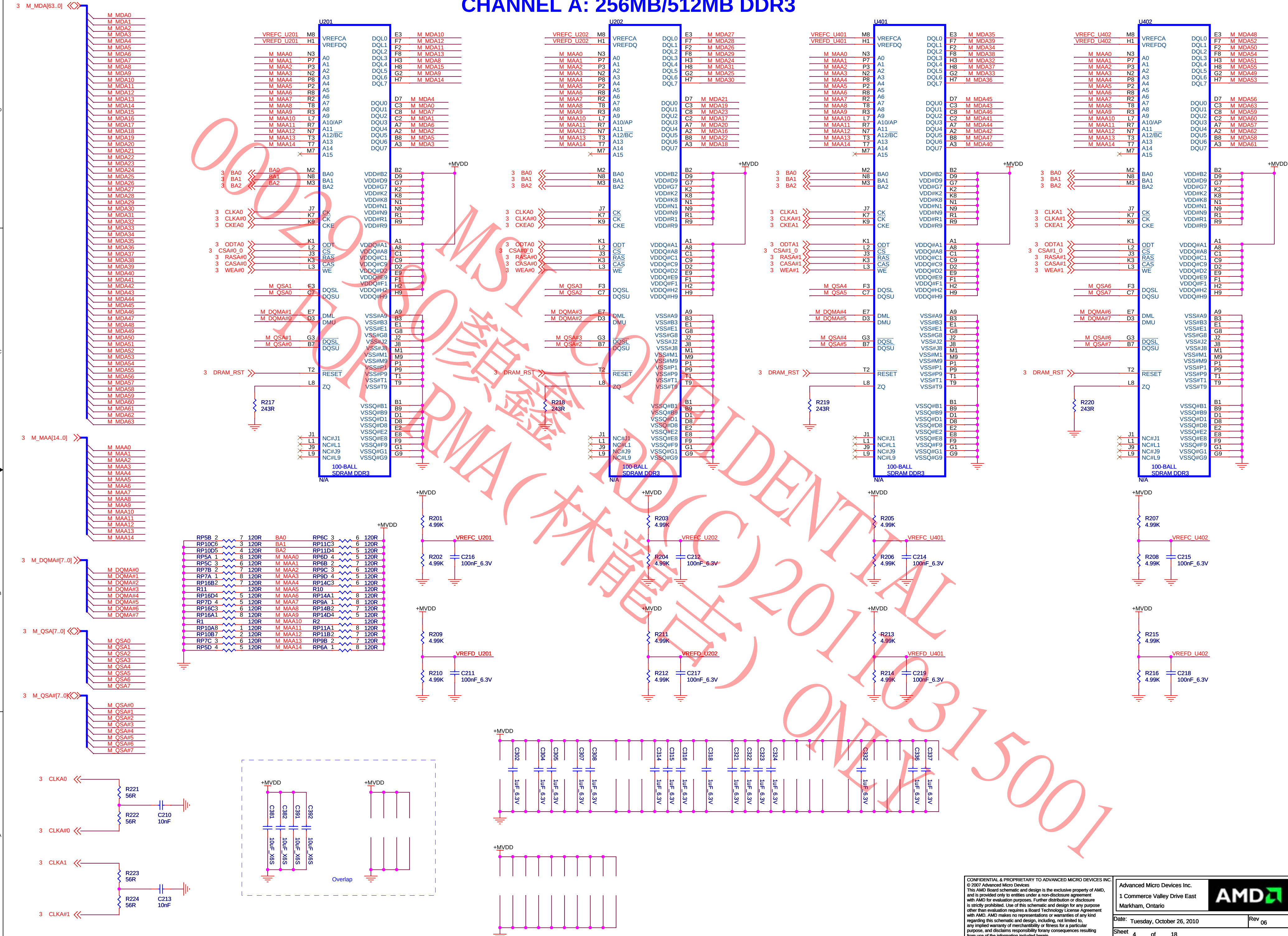
CHANNEL A: 256MB/512MB DDR3



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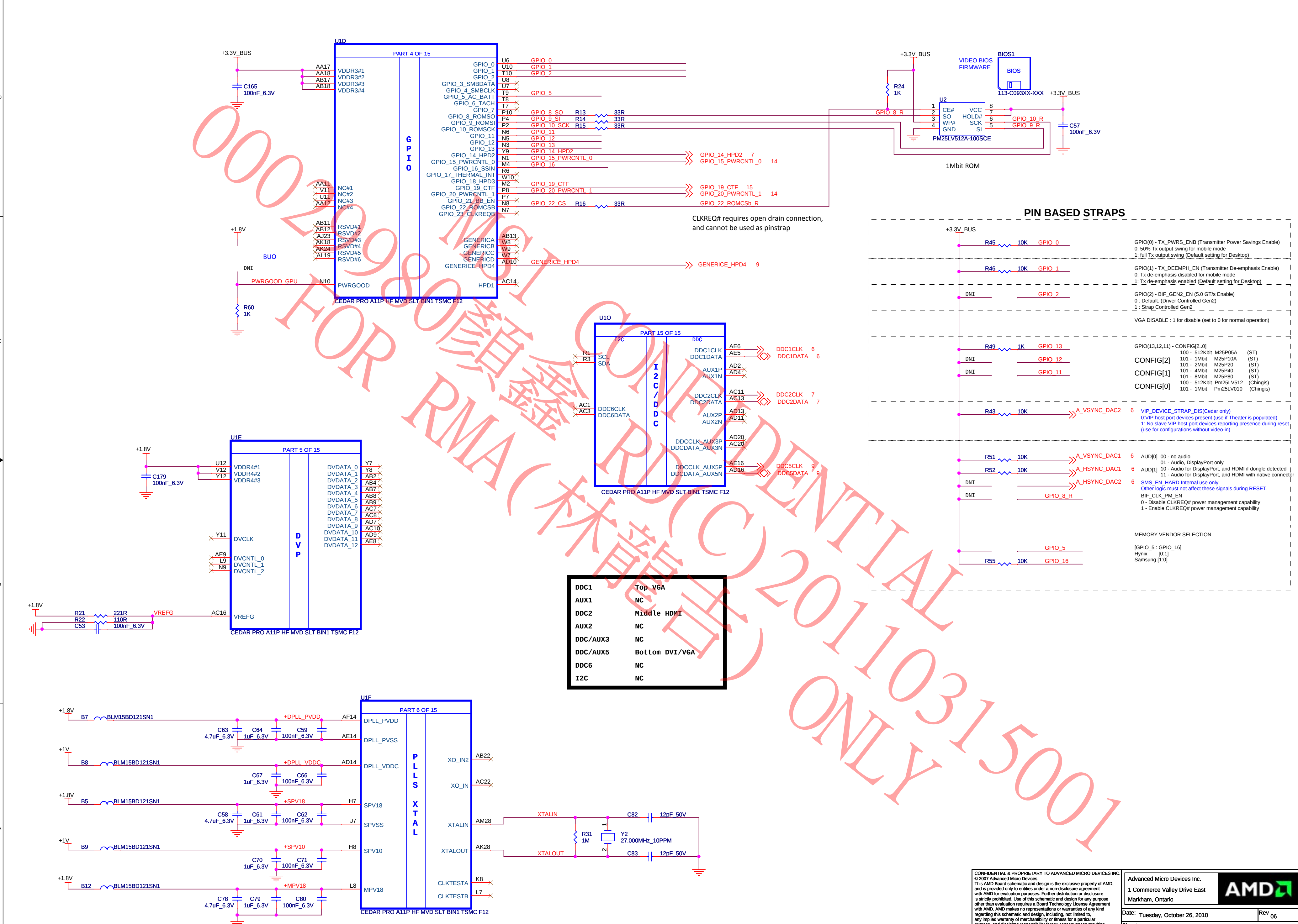
CEDAR GPIOs Strap CF XTAL OSC



DDC1	Top VGA
AUX1	NC
DDC2	Middle HDMI
AUX2	NC
DDC/AUX3	NC
DDC/AUX5	Bottom DVI/VGA
DDC6	NC
I2C	NC

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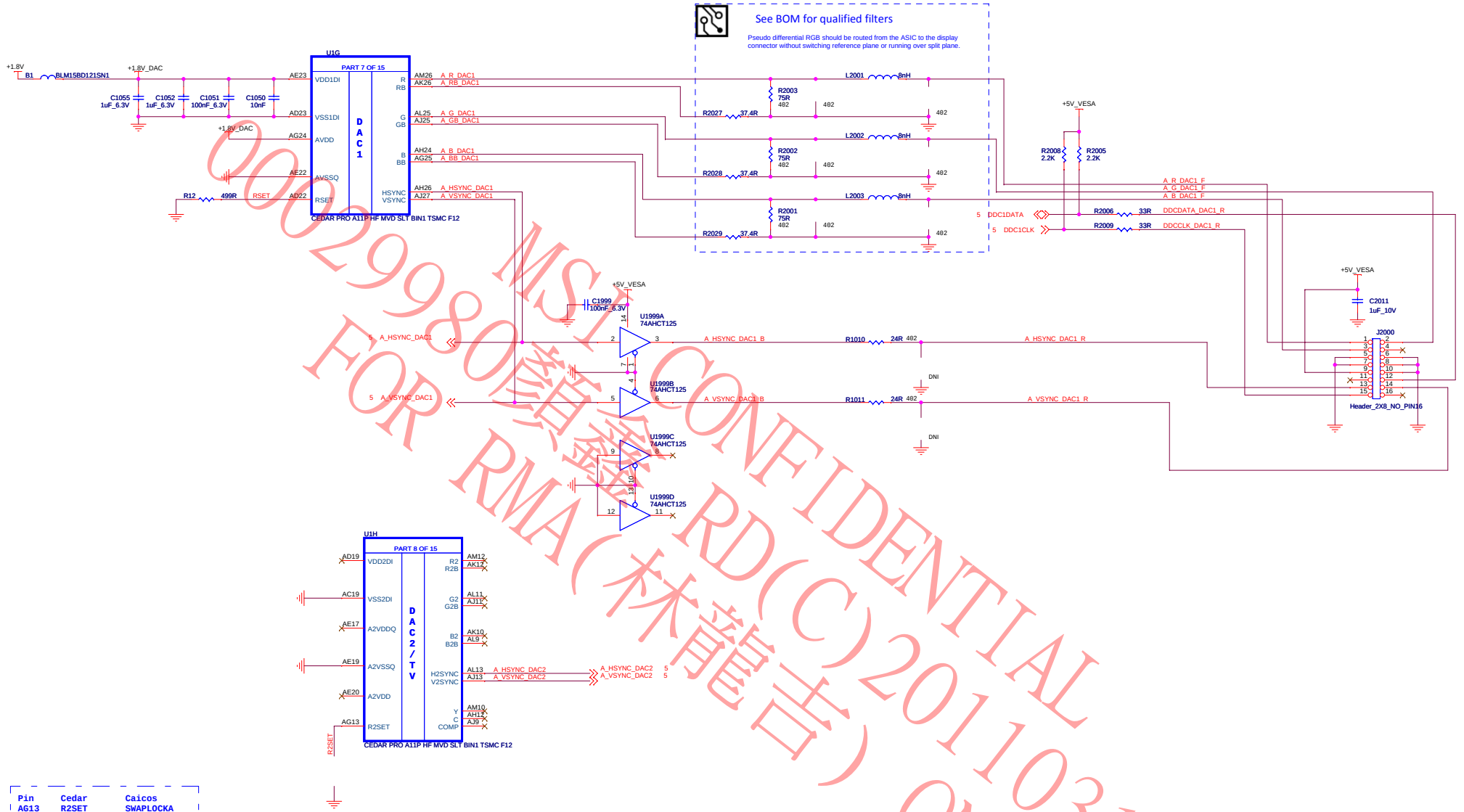
CEDAR DAC1 and DAC2



Pin	Cedar	Caicos
AG13	R2SET	SWAPLOCKA
AH12	C	SWAPLOCKB
AL13	H2SYNC	GENLK_CLK
AJ13	V2SYNC	GENLK_VSYNC
AE19	A2VSSQ	TSVSSQ

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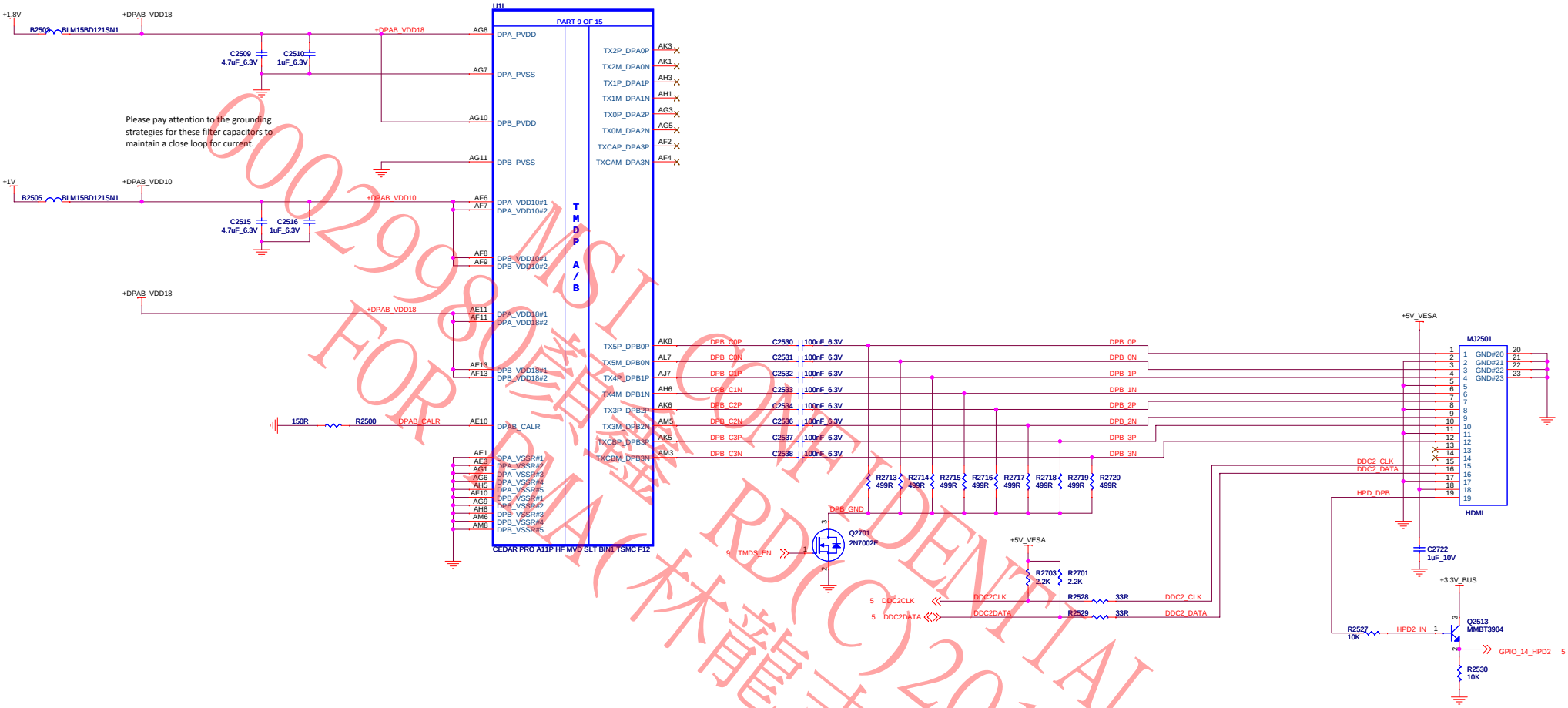
CEDAR TMDP A&B HDMI



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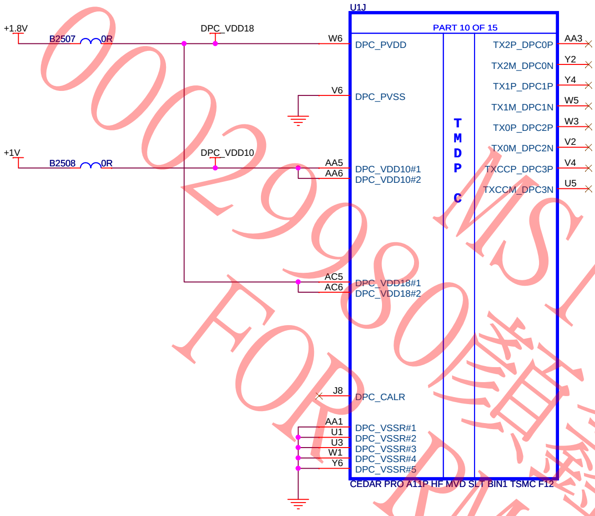
CEDAR Display Port C (Unused)



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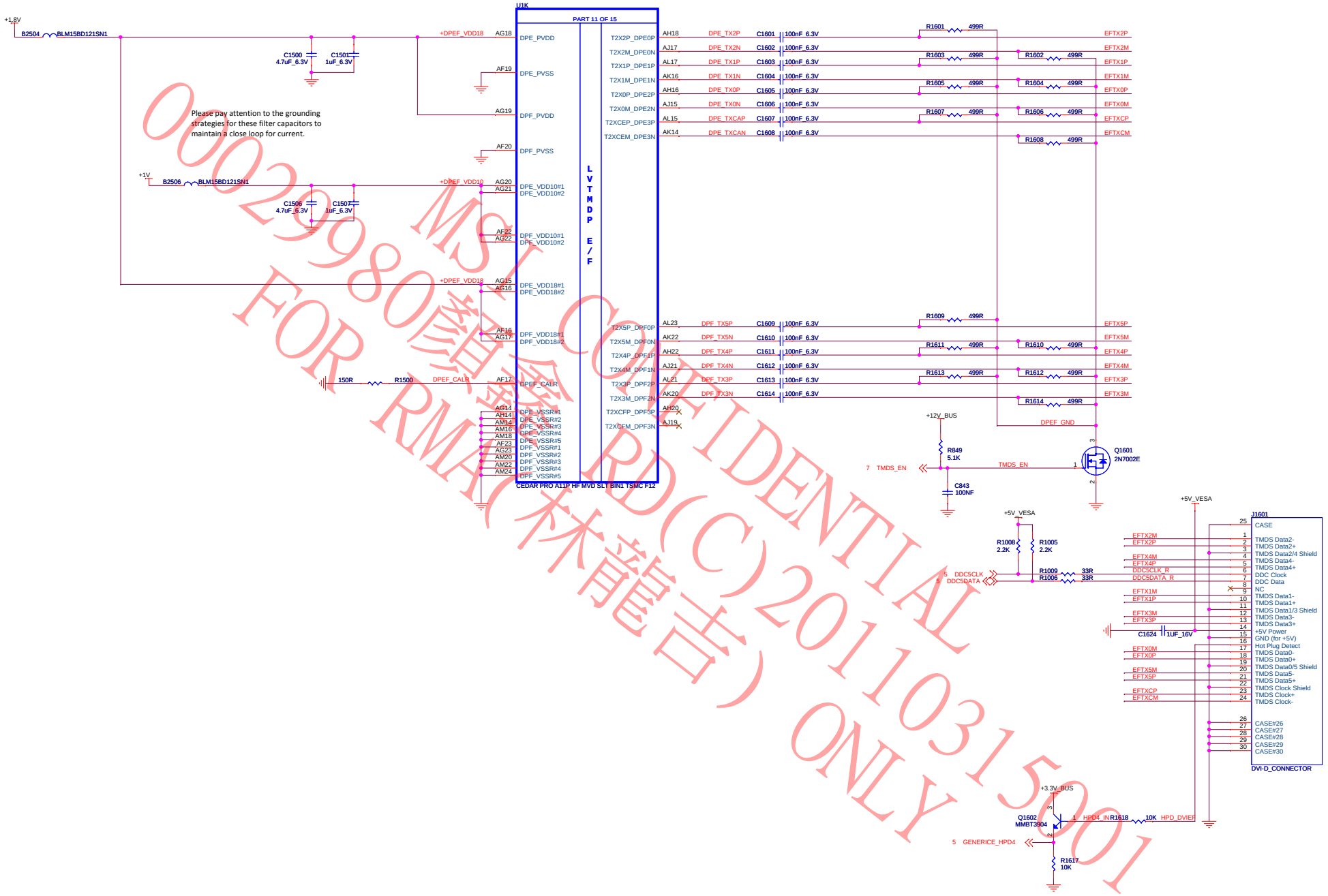
CEDAR LVTMDP E&F dDVI-I



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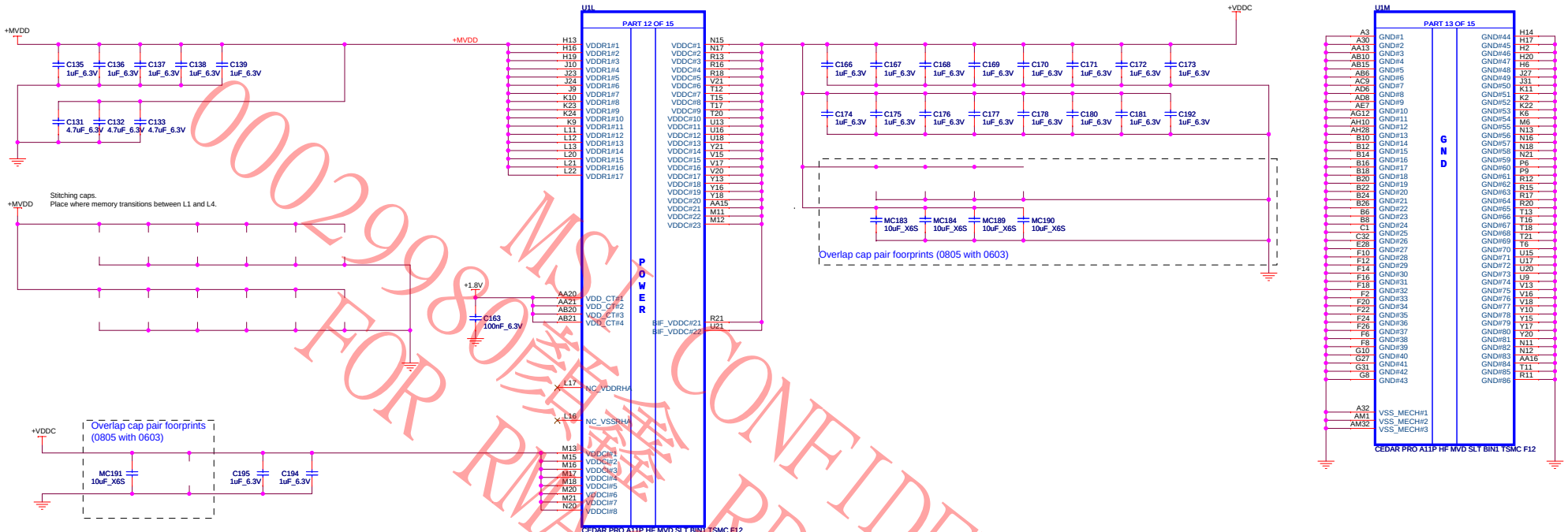
CEDAR Power & GND



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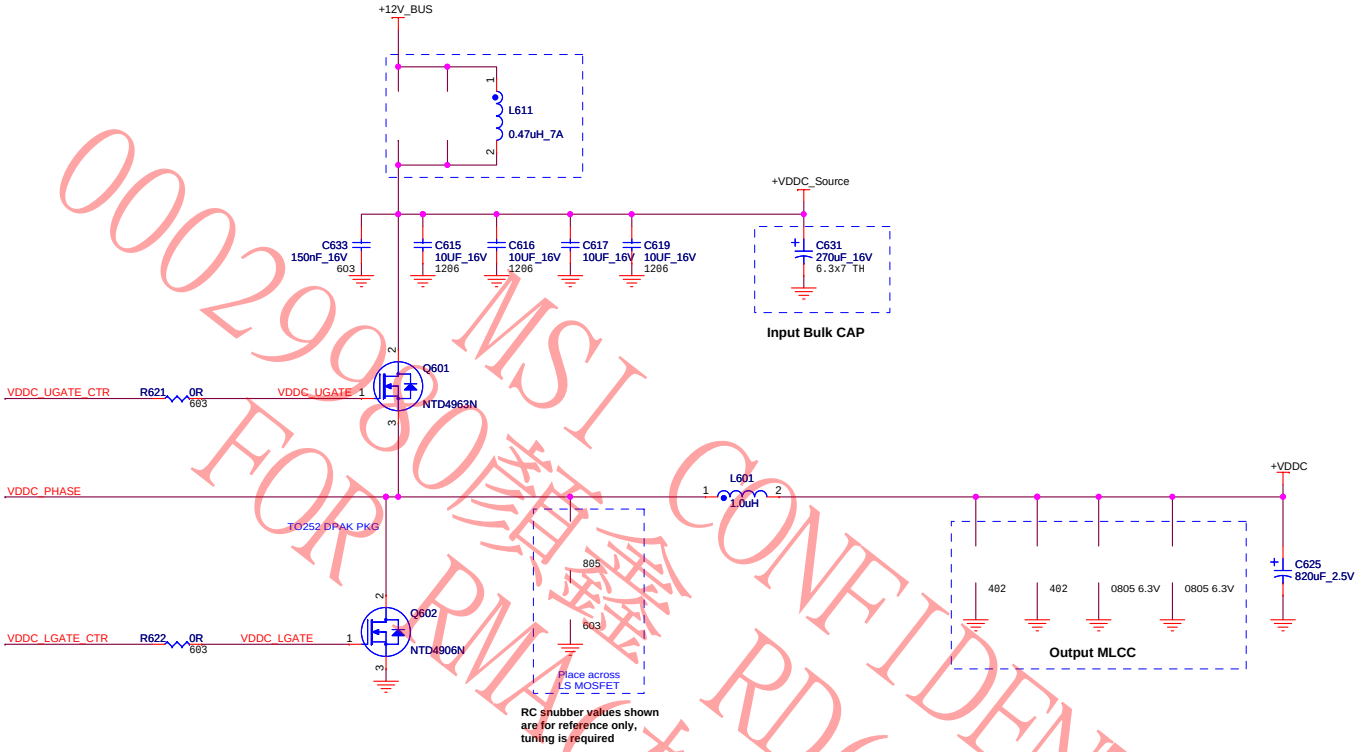

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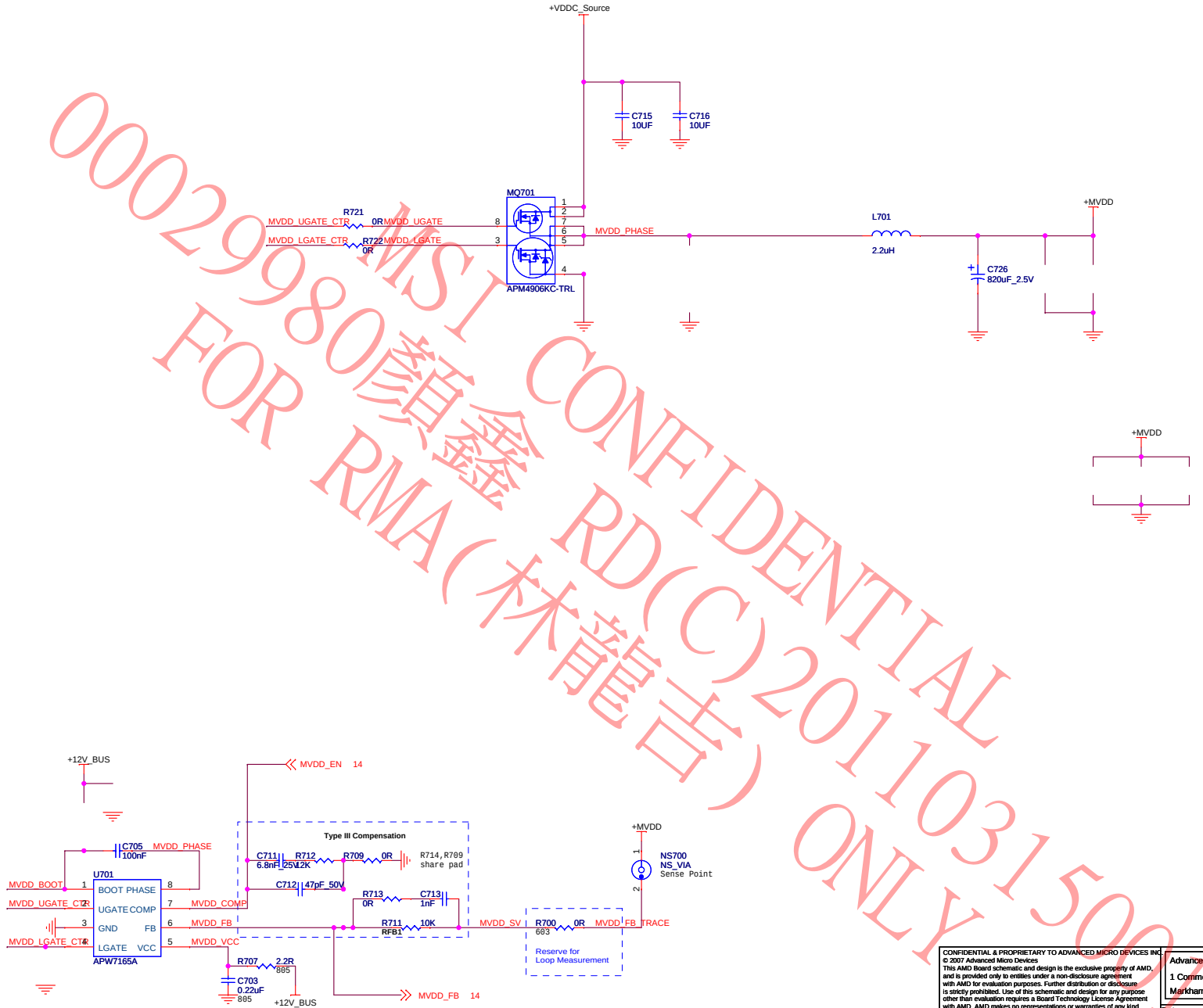

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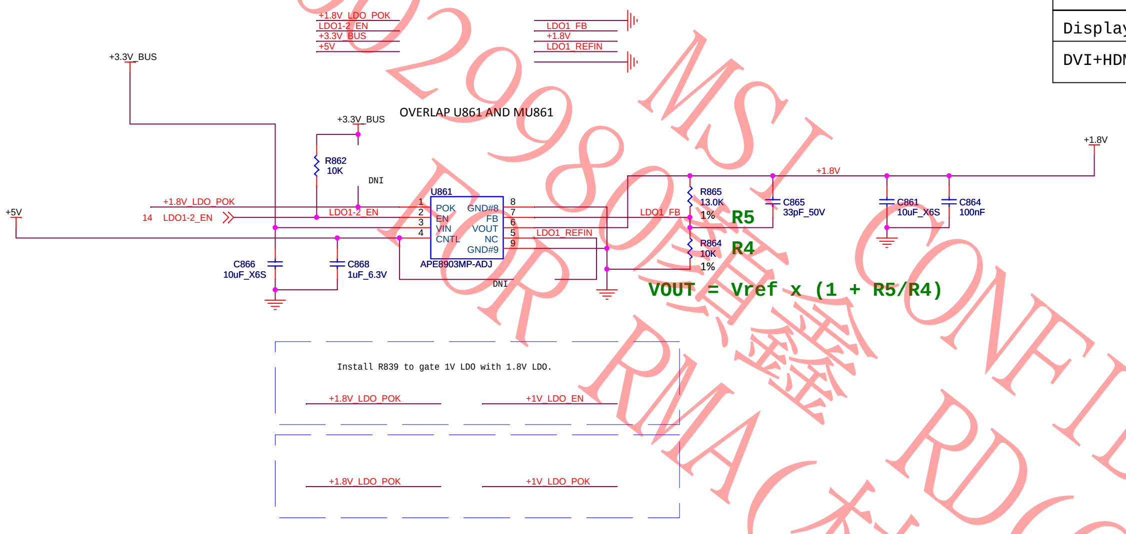
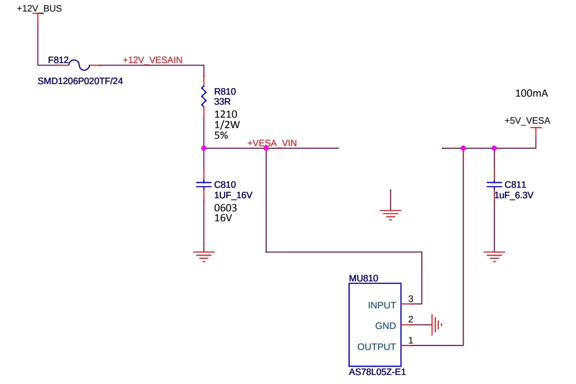
Linear Regulators

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	

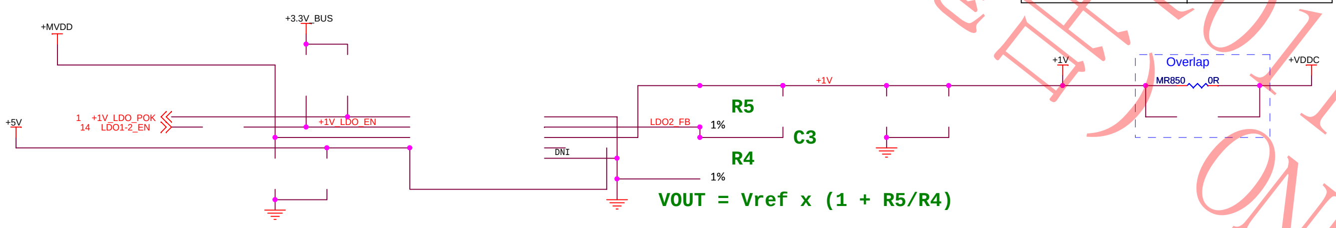


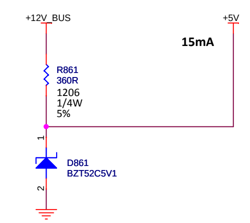
Regulators for +5V, +5V_VESA



LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	





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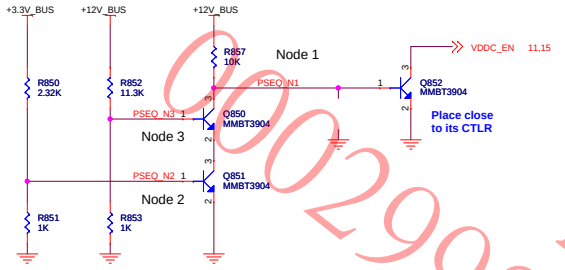
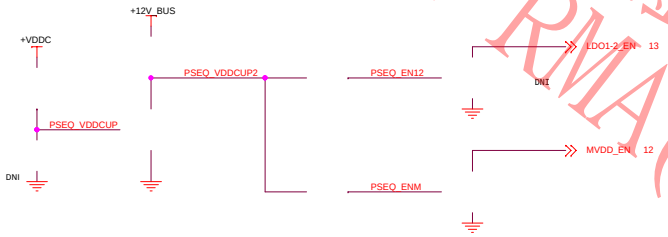
Power Management - Power Gating and Dynamic Voltage Control

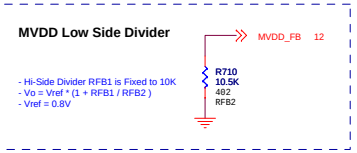
12V_BUS & 3V3_BUS POWER SEQUENCING



POWER SEQUENCING CIRCUIT

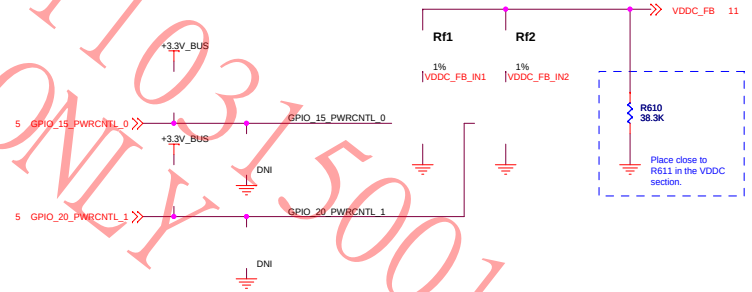


MVDD Low Side Divider



VDDC Low Side Divider

Cedar VDDC=1.0V R610=39.2K(31603922006)
RV710 VDDC=1.1V R610=23.7K(31602372006)



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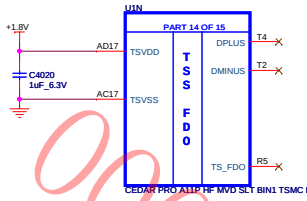
Mechanical and Thermal Management

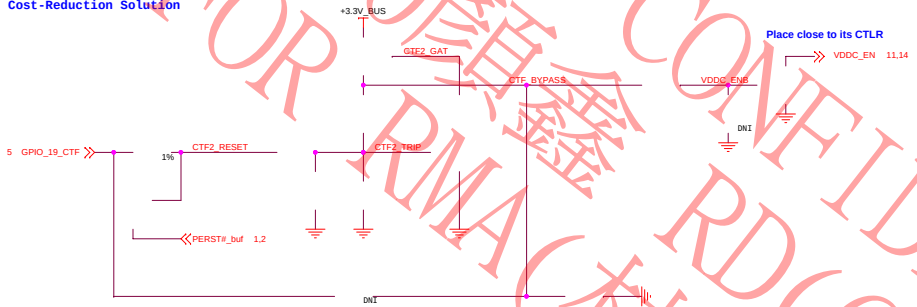


Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board.
This is an open collector signal. Active level is hard pull down to ground.

Critial Temperature Fault

Cost-Reduction Solution

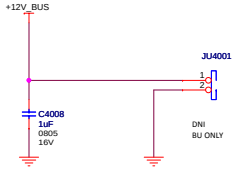


Fan Control

For 2-WIRE FAN ONLY

DVI/DVI SCREWS with top tab

This circuit provides a minimum voltage for the fan, independent of PWM input -> check if needed for RV710



Add Copper under pad 4
(at least 1cm^2)

Square Fansink 12W

H1
Cedar_Fansink

7120336200G

For DVI Connector

ASSY-SCREW200
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW201
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

7020000800G

Bracket Components

ASSY-SCREW202
SCREW
SCREW

7020005200G

SKU		P/N	CONFIGURATION	Form Factor
	PERCH	80200513000G	DVI + DP + VGA	FH / SS
BASS		80200514000G	DVI +HDMI+ VGA	FH / SS
	PERCH	80200516000G	DVI + DP	LP / SS
BASS		80200516A0G	DVI +HDMI	LP / SS
	PERCH	80200517000G	DVI + DP + VGA	FH / DS
BASS		80200517A0G	DVI +HDMI+ VGA	FH / DS

PCB1
PCB
109-C26737-00A

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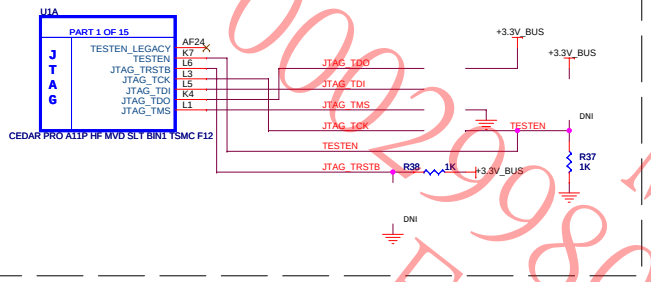
(19) Debug Circuits

JTAG



LM96163 FOR BACKUP THERMAL CONTROL

SWITCH CONNECTIONS TO PINSTRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

I2C VDDC Control

LED RED "ON" shows Fault

SCL/SDA PORT DEBUG ACCESS
Place connector on the back side
(easily accessible and not blocked by the heatsink).

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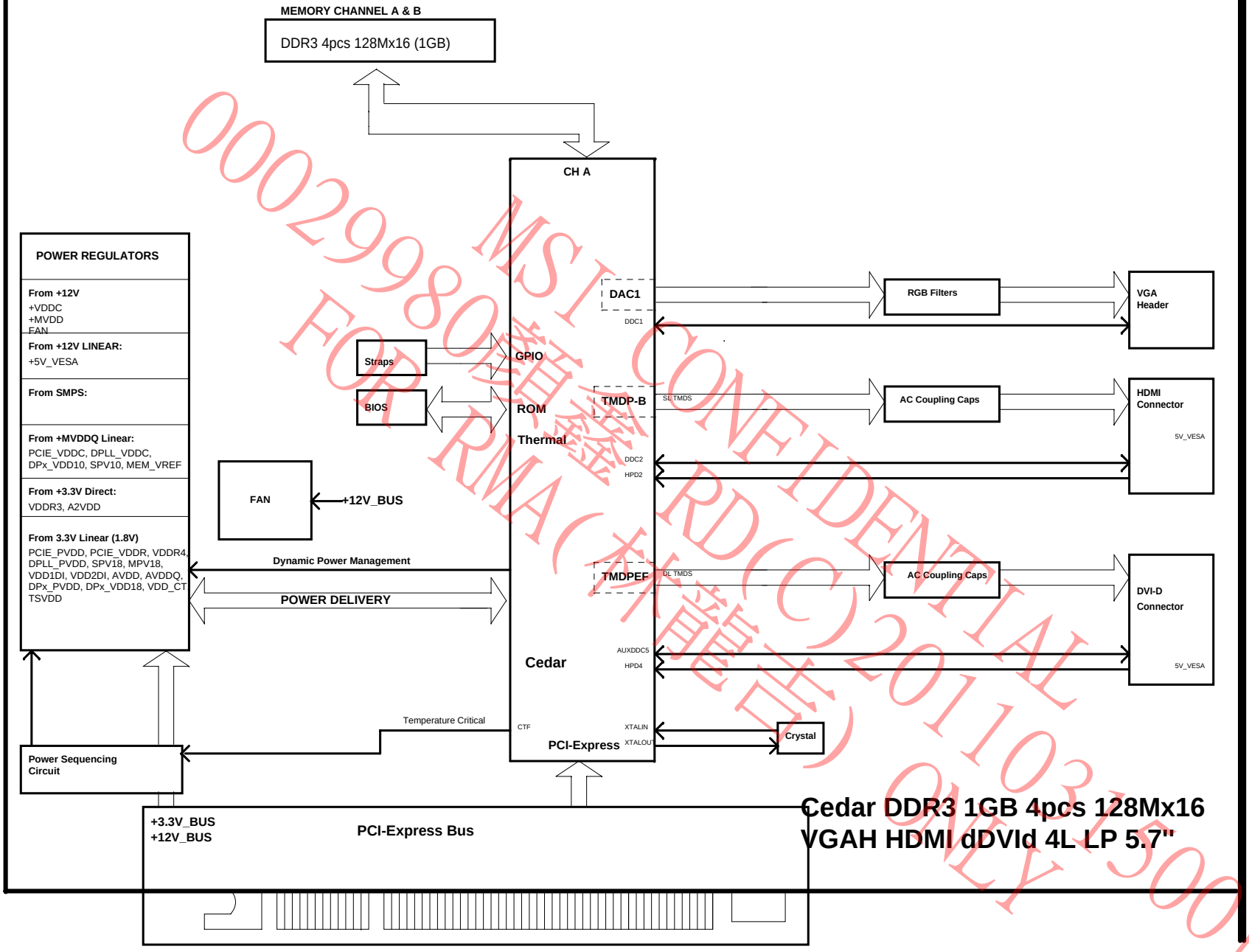

Cedar DDR3 1GB 4pcs 128Mx16
VGAH HDMI dDVId 4L LP 5.7"

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Canada, L3T 7X6
(905) 882-2600

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Title	Schematic No.	Date:
Cedar DDR3 1GB 1pcs 128Mx16 VGAH HDMI dDVId 4L	102-C26701-00	Tuesday, October 26, 2010

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 06

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/11/23	Initial Cedar schematic, based on C093