E4905-A00

N18P GDDR5 X32 128BITS
PCIE AND MODULAR DISPLAY

TABLE OF CONTENTS

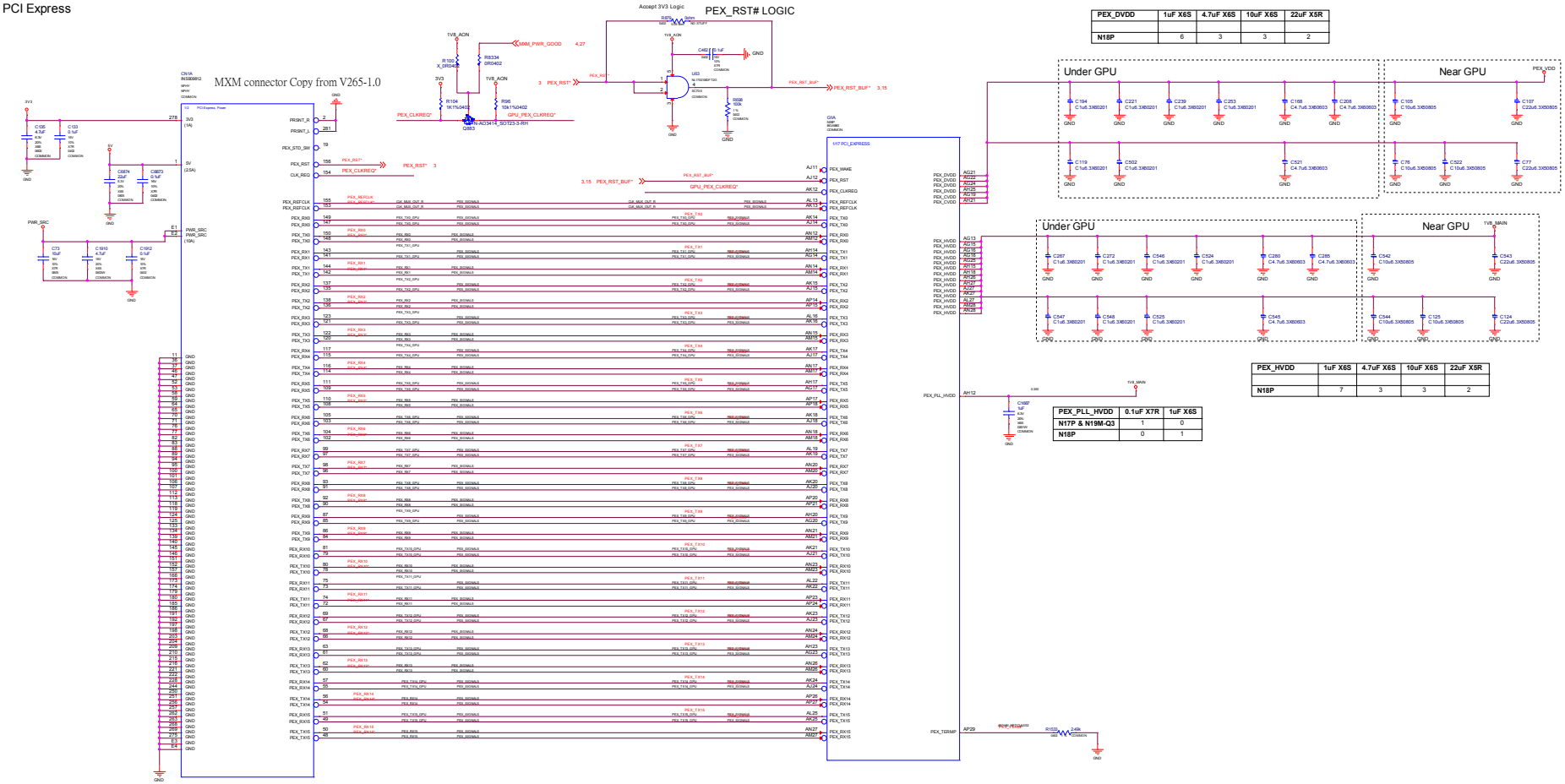
MICRO-STAR INT'L CO.,LTD

N19P

Size	Document Description	Rev
Custom	BLOCK DIAGRAM	1.0

Date: Wednesday, July 10, 2019 Sheet 2 of 29

PCI Express



PEX_DVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
N18P	6	3	3	2

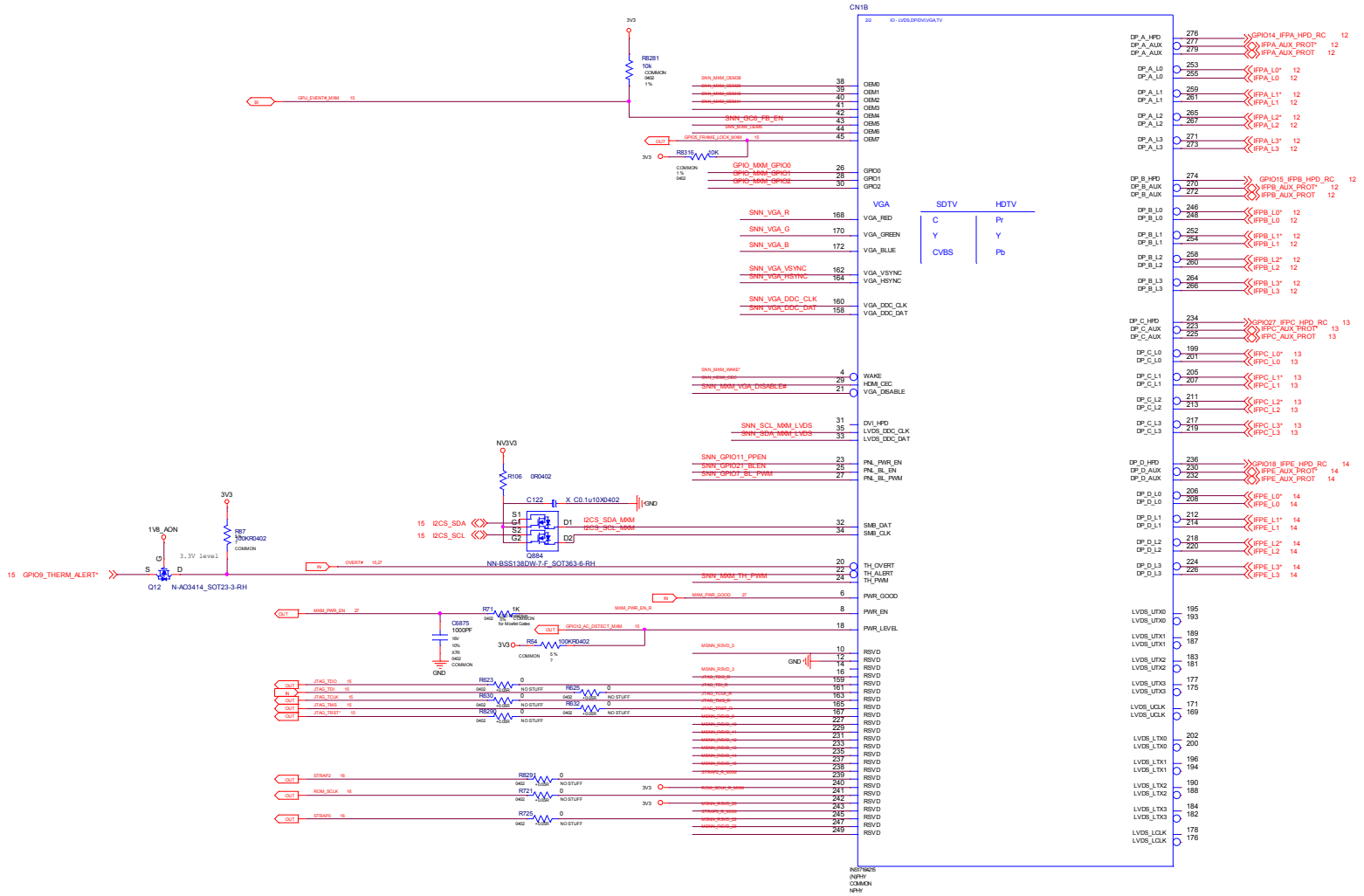
PEX_HVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
N18P	7	3	3	2

PEX_PLL_HVDD	0.1uF X7R	1uF X6S
N17P & N19M-Q3	1	0
N18P	0	1

MICRO-STAR INT'L CO.,LTD	
N19P	
Size: Custom	Document Description: PCI EXPRESS
Rev: 1.0	
Date: Wednesday, July 10, 2019	Sheet 3 of 29

PCI EXPRESS REFCLK SOURCE & TRACES

MXM connector Copy from V265-1.0



MICRO-STAR INT'L CO.,LTD

N19P

Size	Document Description	Rev
Custom	MXM Connector	1.0

Date: Wednesday, July 10, 2019 Sheet 4 of 29

MEMORY: GPU PARTITION A/B

PB_REFPLL_AVDD	0.1uF X7R	1uF X6S
N17P & N19M-Q3	1	0
N18P	0	1

DQ 40 ohm Single-End
TOP/BOTTOM 7 mil
L3/L4/L6 6.5 mil

DBI / EDC 40 ohm Single-End
TOP/BOTTOM 7 mil
L3/L4/L6 6.5 mil

CMD 45 ohm Single-End
TOP/BOTTOM 5.5 mil
L3/L4/L6 5.5 mil

CLK Zo = 80 ohm Differential
TOP/BOTTOM 5 / 4.5 mil
L3/L4/L6 4.5 / 4 mil

WCK Zo = 80 ohm Differential
TOP/BOTTOM 5 / 4.5 mil
L3/L4/L6 4.5 / 4 mil

FB_VREF	
N17P & N19M-Q3	NC
N18P	1K OHM pull-down

PBA_PLL_AVDD	0.1uF X7R	1uF X6S
N17P & N19M-Q3	1	0
N18P	0	1

PBx_PLL_AVDD	4.7uF X6S	22uF X6S
N17P & N19M-Q3	1	1
N18P	2	1

PBB_PLL_AVDD	0.1uF X7R	1uF X6S
N17P & N19M-Q3	1	0
N18P	0	1

CKE_A

CKE_B

RESET

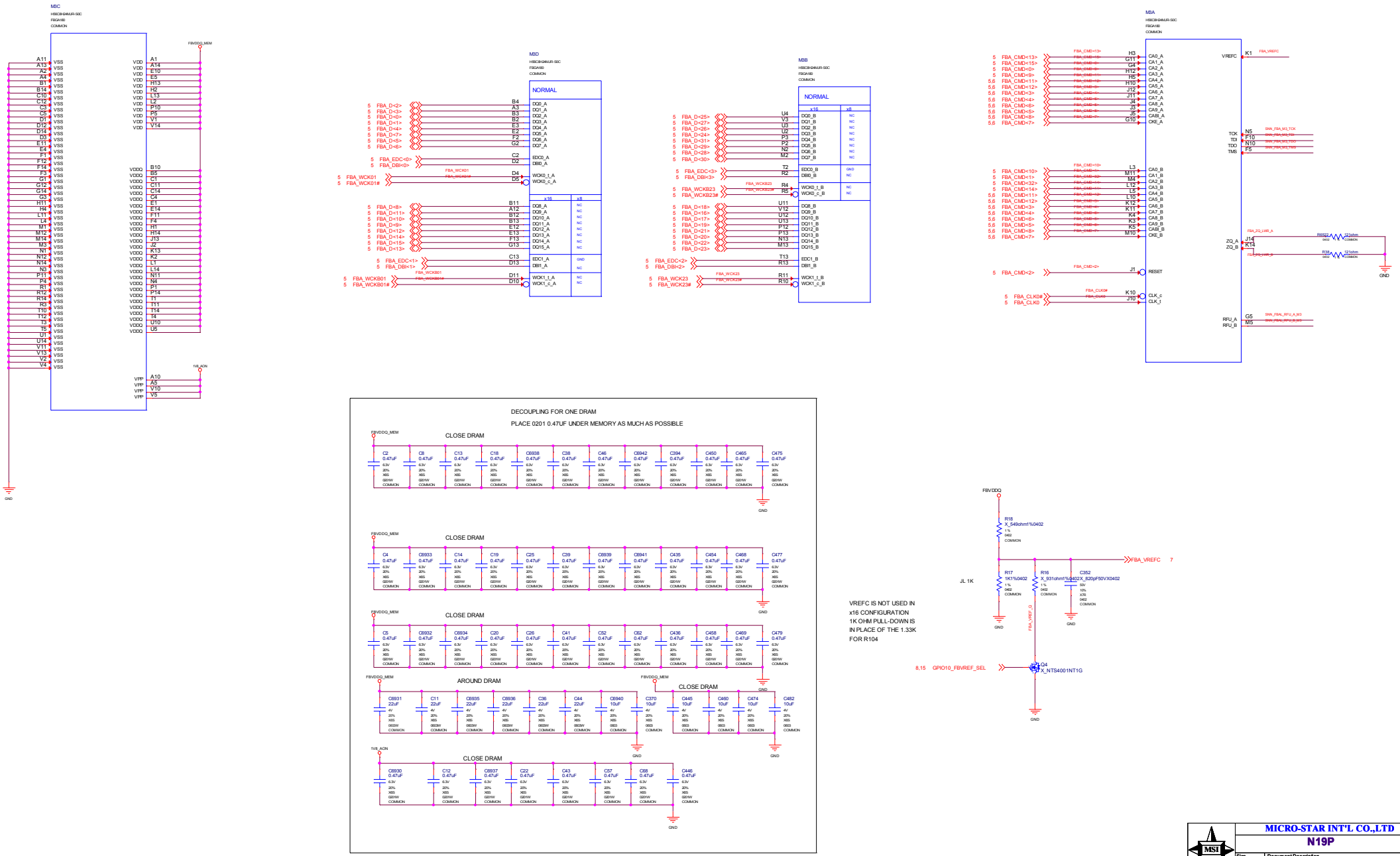
Under GPU

Place near GPU

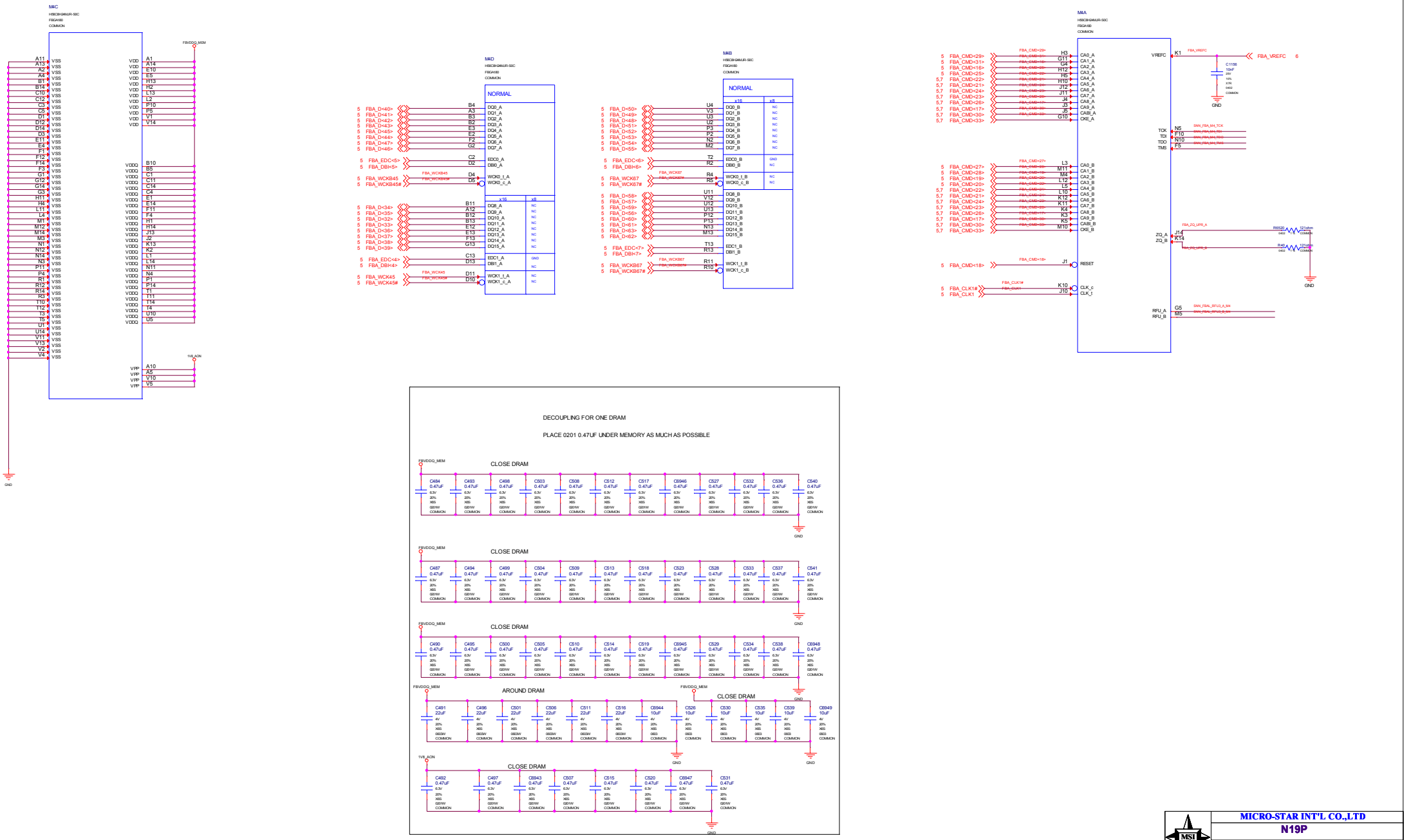
GDDR5_BGA170_MIRR COMMAND MAP

MICRO-STAR INT'L CO.,LTD		
N19P		
Size: Custom	Document Description: MEMORY_ GPU PARTITION A_	Rev: 1.0
Date: Wednesday, July 10, 2019	Sheet 5 of 29	

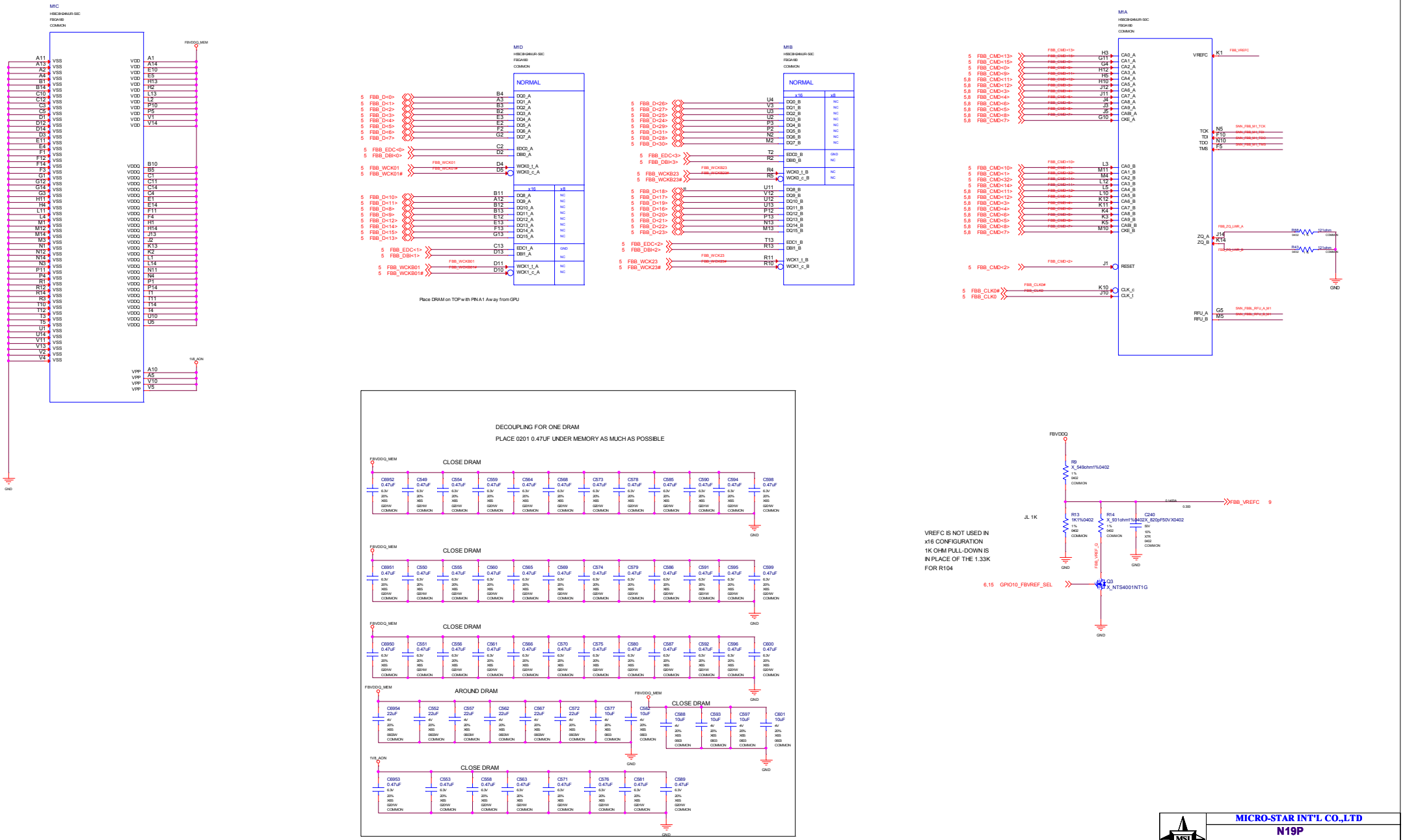
MEMORY: FBA[31:0]



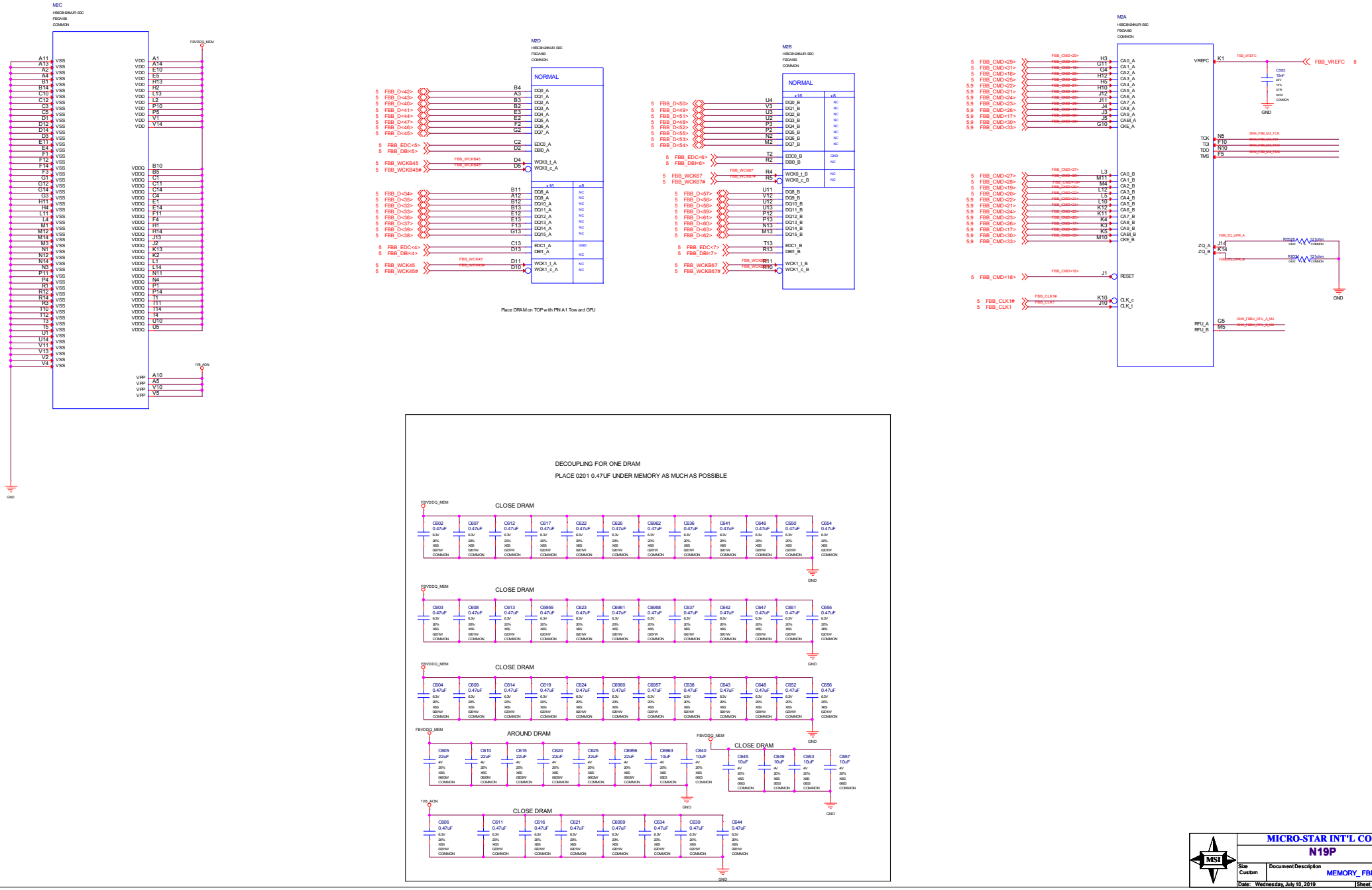
MEMORY: FBA[63:32]



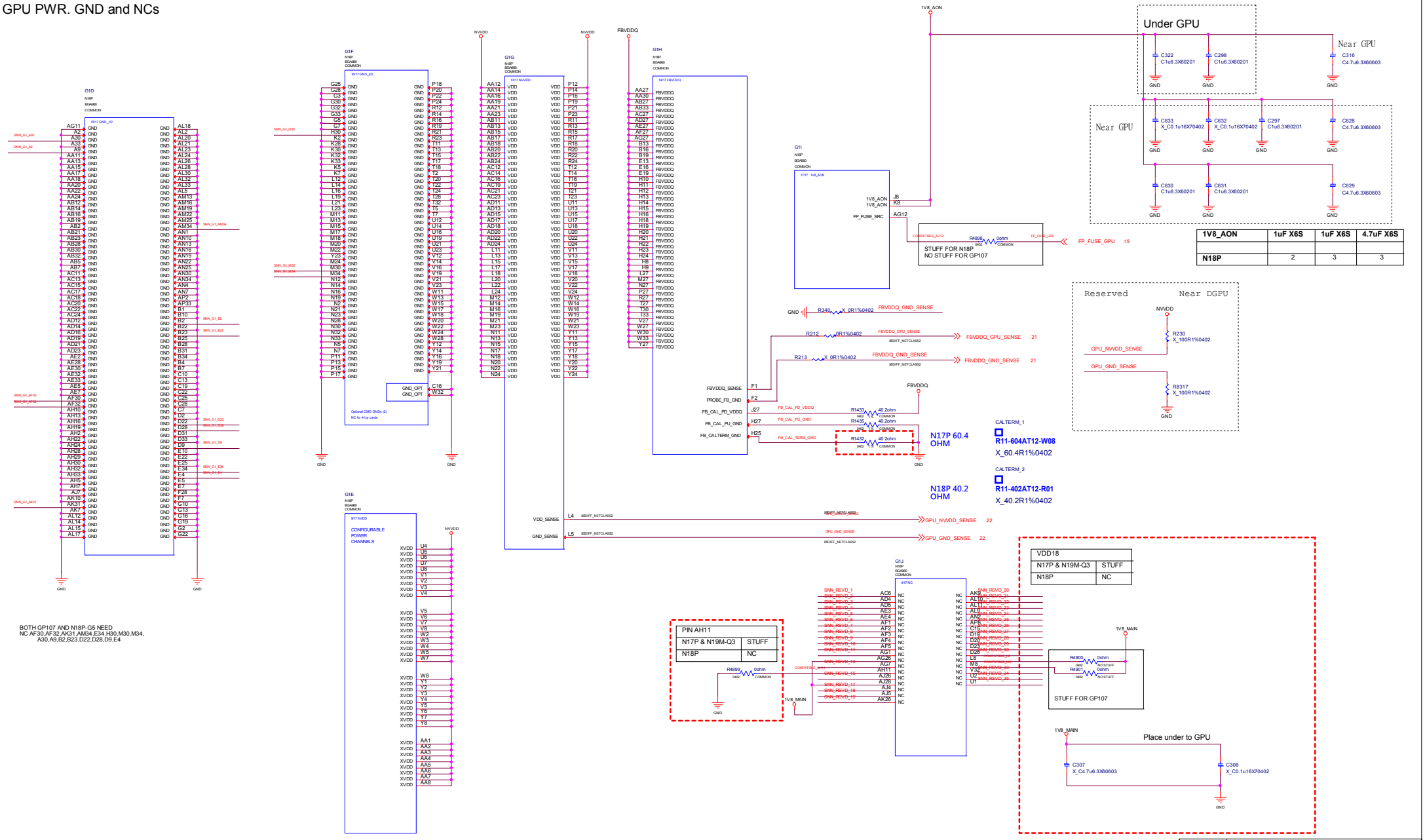
MEMORY: FBB[31:0]



MEMORY: FBB[63:32]



GPU PWR. GND and NCs



1V8_AON	1uF X6S	1uF X6S	4.7uF X6S
N18P	2	3	3

MICRO-STAR INT'L CO.,LTD

N19P

Size: Custom | Document Description: GPU PWR. GND and NCs | Rev: 1.0

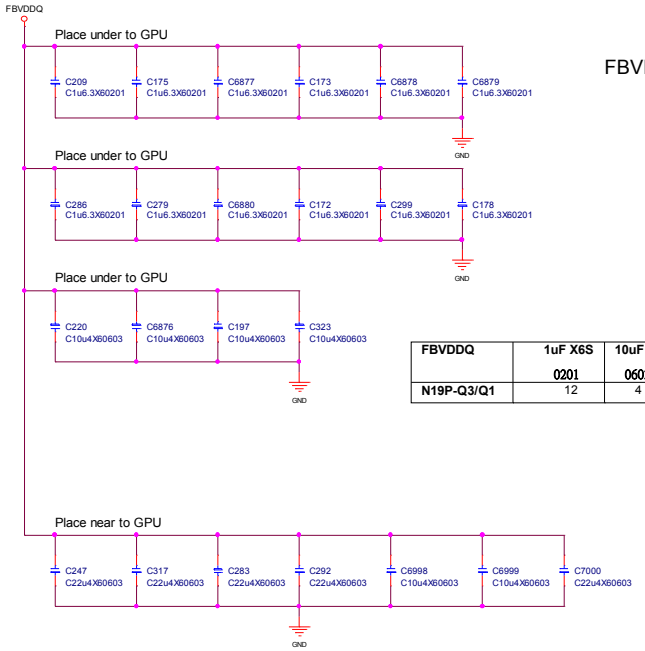
Date: Wednesday, July 10, 2019 | Sheet 10 of 29

GPU DECOUPLING

NVVDD

NVVDD	1uF X6S	10uF X6S	22uF X6S
	0201	0603	0805
N19P-Q3/Q1	13	34	15

FBVDDQ



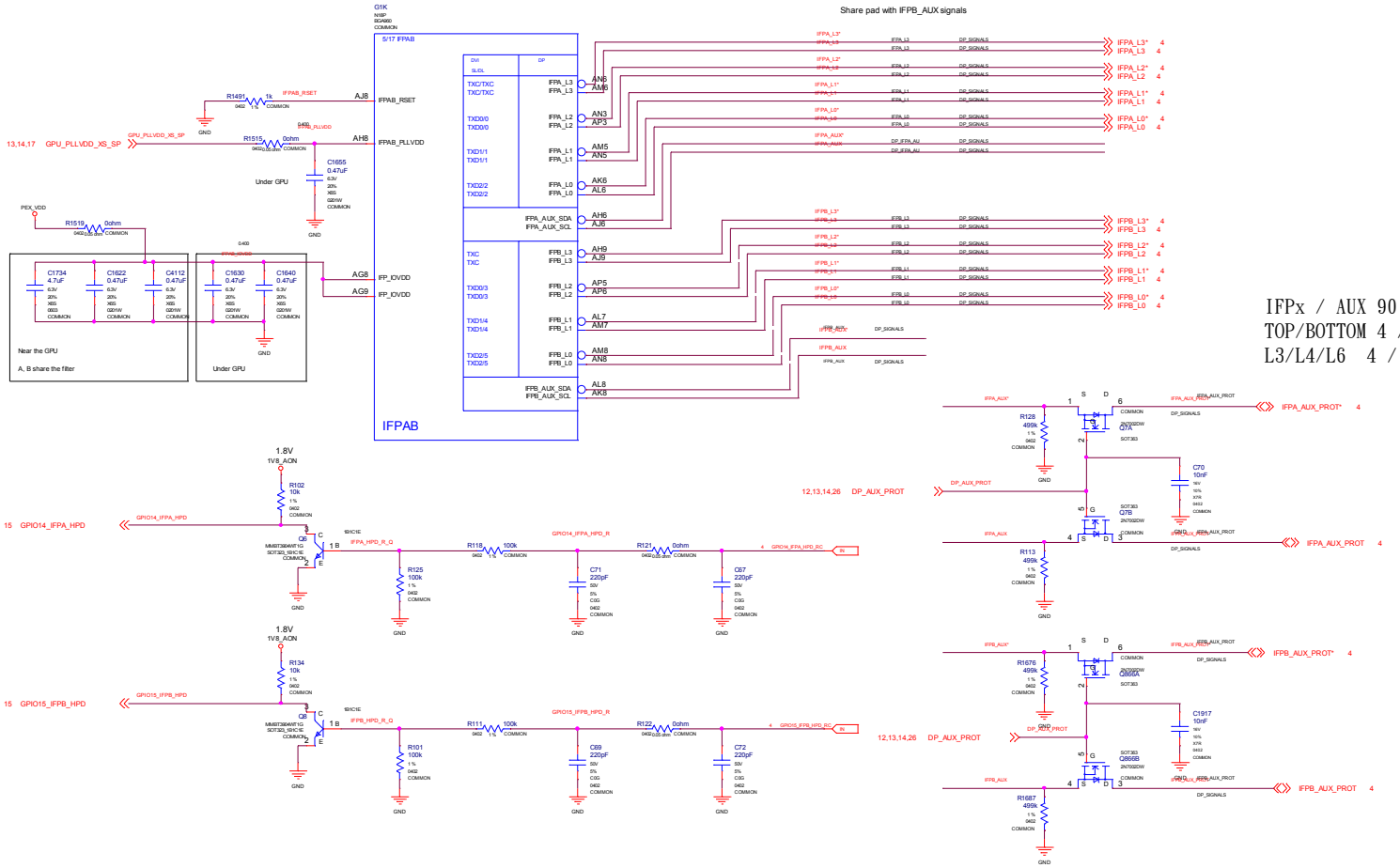
FBVDDQ	1uF X6S	10uF X6S	22uF X6S	10uF X6S
	0201	0603	0603	0603
N19P-Q3/Q1	12	4	5	2

MICRO-STAR INT'L CO.,LTD

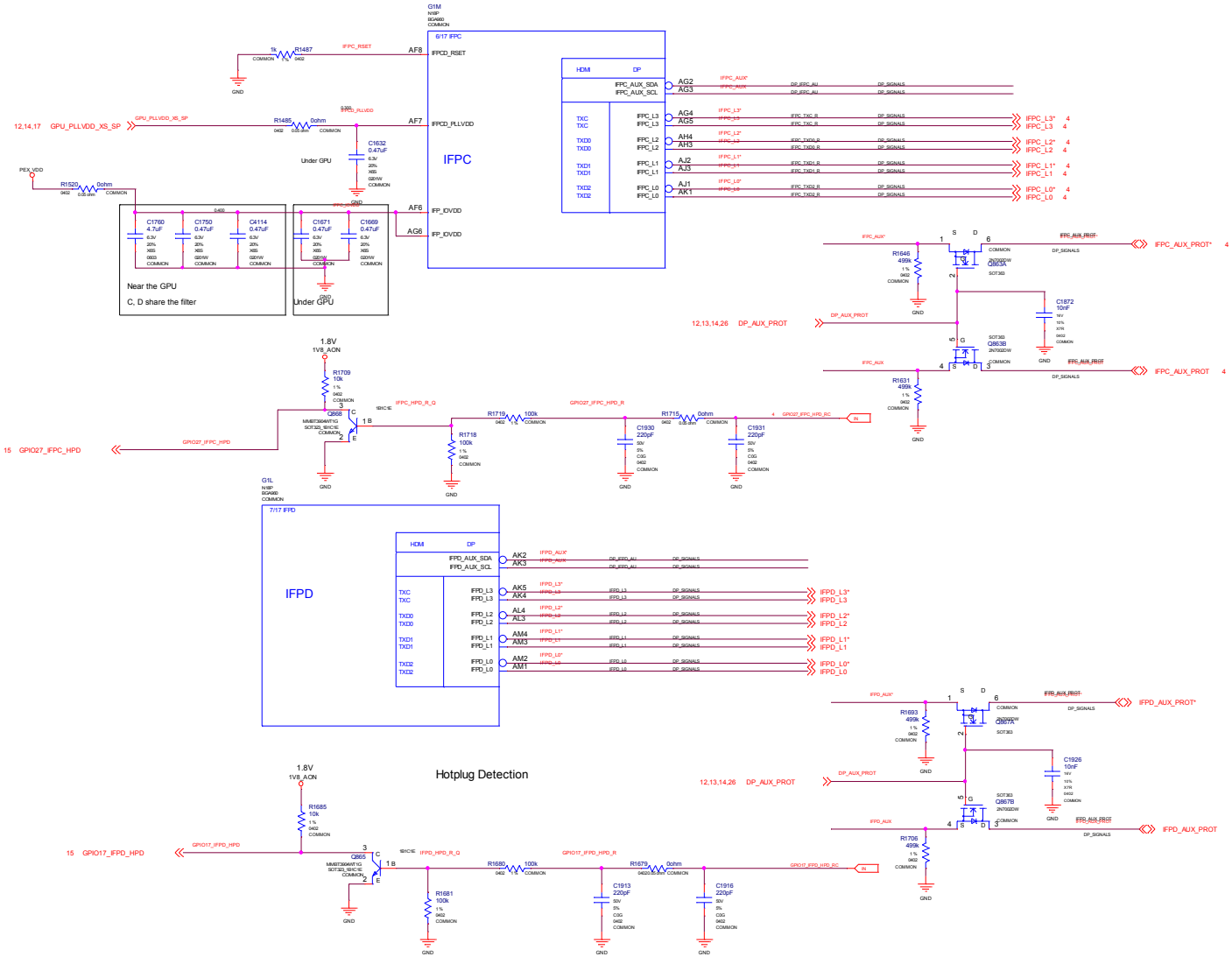
N19P

Size: Custom | Document Description: GPU DECOUPLING | Rev: 1.0

Date: Wednesday, July 10, 2019 | Sheet 11 of 29

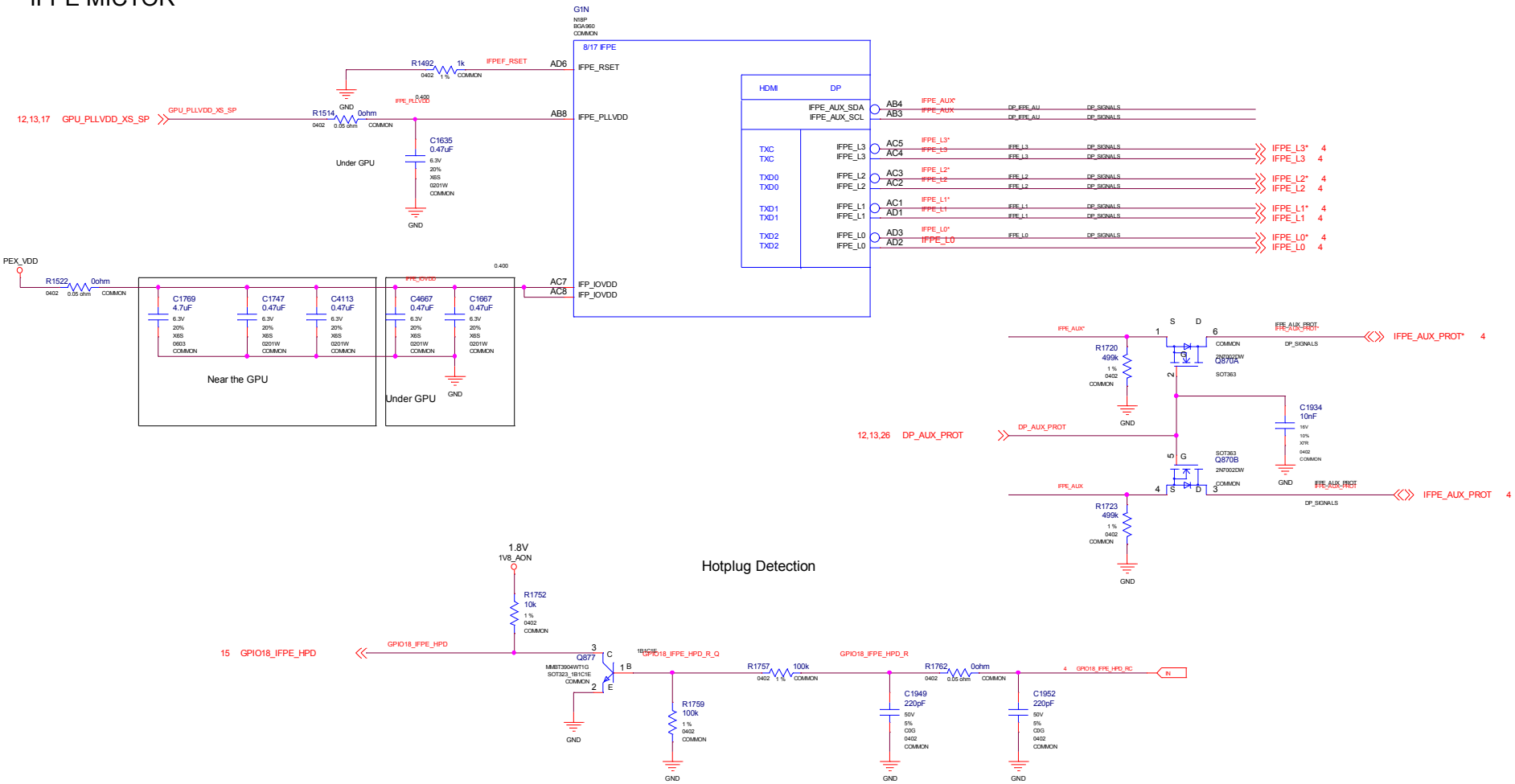

G1K
N19P BOARD COMMON
5/17 IFPAB
IFPAB
Share pad with IFPB_AUX signals
IFPA_RSET
IFPAB_RSET
IFPAB_PLLVDD
IFP_IOVDD
GPU_PLLVDD_XS_SP
Under GPU
Near the GPU
A, B share the filter
IFPA_AUX_SDA
IFPA_AUX_SCL
IFPB_AUX_SDA
IFPB_AUX_SCL
DP_AUX_PROT
IFPA_AUX_PROT*
IFPB_AUX_PROT*
GPIO14_IFPA_HPD
GPIO15_IFPB_HPD
1.8V
1V8_ACON
IFPx / AUX 90 ohm Differential
TOP/BOTTOM 4 / 5 mil
L3/L4/L6 4 / 6 mil

IFPCD DPIIM



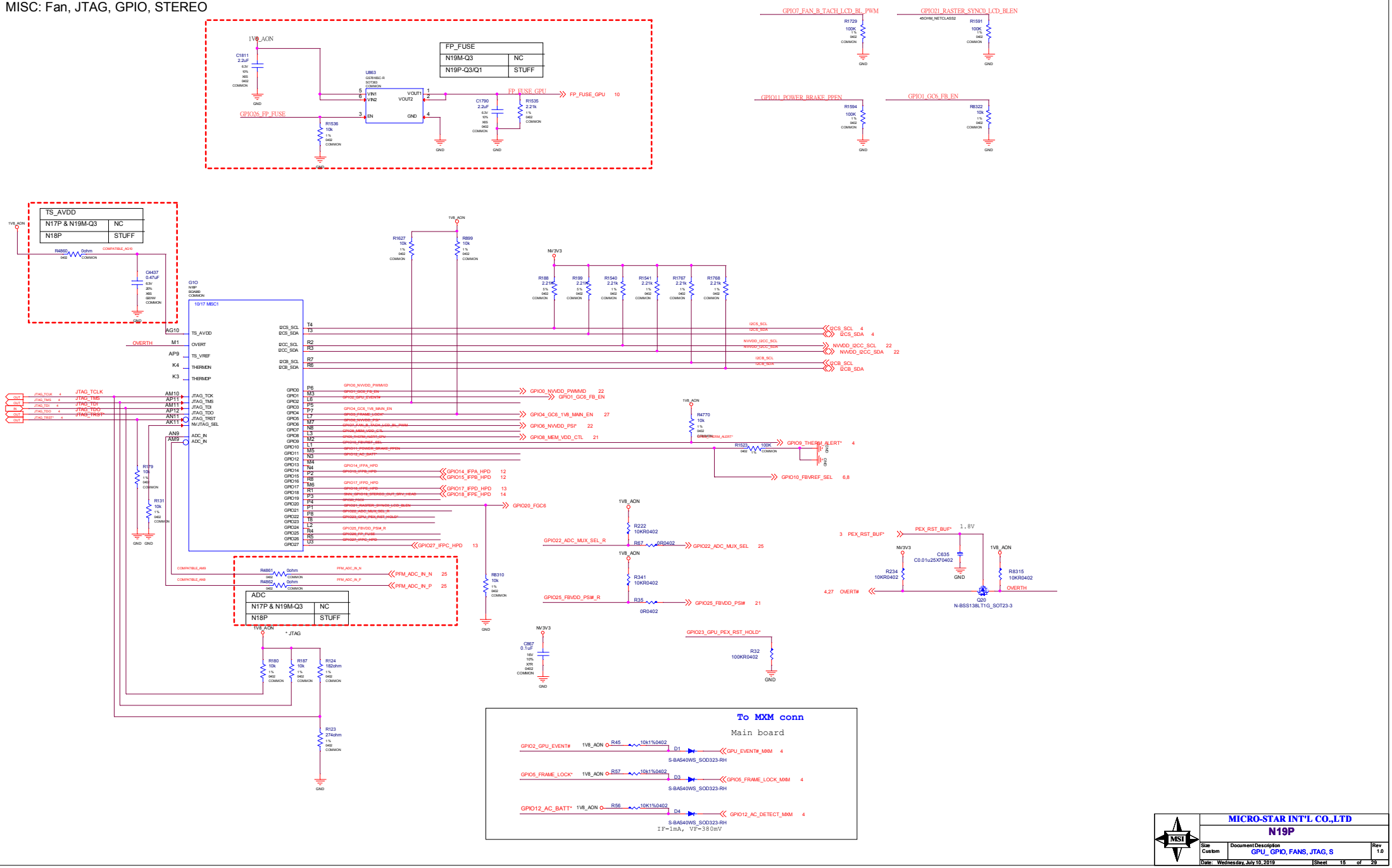
MICRO-STAR INT'L CO.,LTD			
N19P			
Size: Custom	Document Description: GPU IFPCD DPIIM		Rev: 1.0
Date: Wednesday, July 10, 2019		Sheet 13 of 29	

IFPE MICTOR



MSI	MICRO-STAR INT'L CO.,LTD	
	N19P	
Size: Custom	Document Description: GPU IFPE MICTOR	Rev: 1.0
Date: Wednesday, July 10, 2019	Sheet 14 of 29	

MISC: Fan, JTAG, GPIO, STEREO



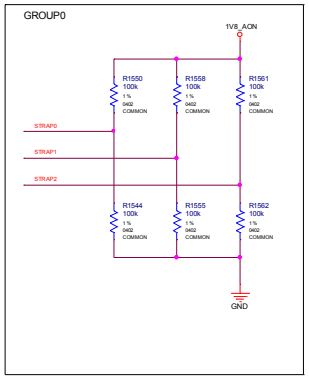
MISC2: ROM, Straps

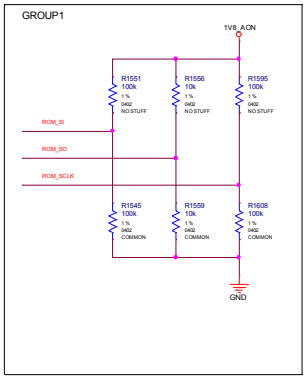
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

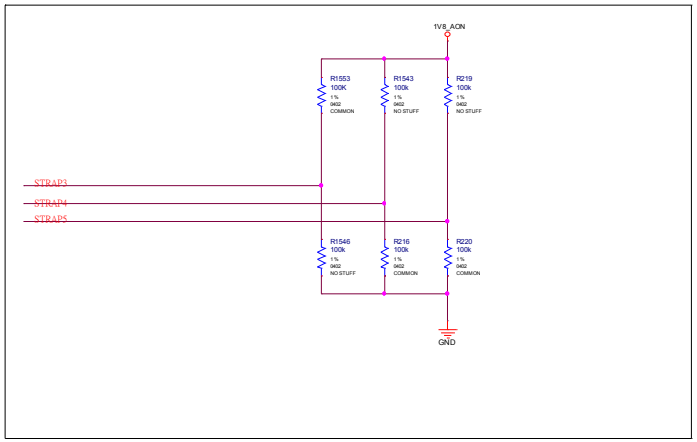
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

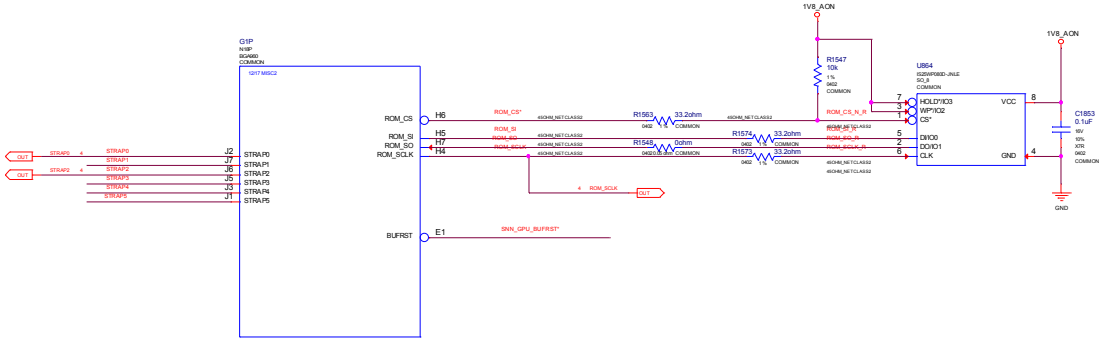
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	1:SMB_ALT_ADDR ENABLE 0:SMB_ALT_ADDR DISABLE
L	M	H	1	0	1	0	1:DEVID_SEL REBRAND 0:DEVID_SEL ORIGNAL
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	1:PCIE_CFG LOW POWER 0:PCIE_CFG HIGH POWER
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	1:VGA_DEVICE ENABLE 0:VGA_DEVICE DISABLE
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	









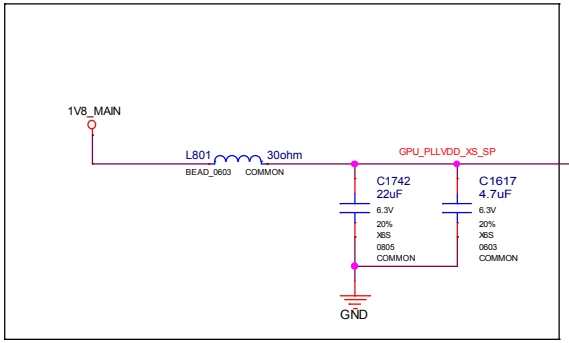
MICRO-STAR INT'L CO.,LTD

N19P

Size	Document Description	Rev
Custom	GPU_ROM, STRAPS	1.0
Date: Wednesday, July 10, 2019	Sheet 16 of 29	

MISC2: XTAL. PLL

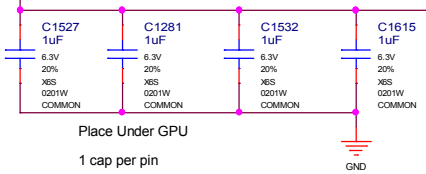
XSN_PLLVDD GPCPLL_AVDD SP_PLLVDD VID_PLLVDD	0.1uF X7R	1uF X6S	4.7uF X6S	22uF X6S
N17P & N19M-Q3	4	0	1	1
N18P	0	4	1	1



Place near GPU

0.400

GPU_PLLVDD_XS_SP 12,13,14

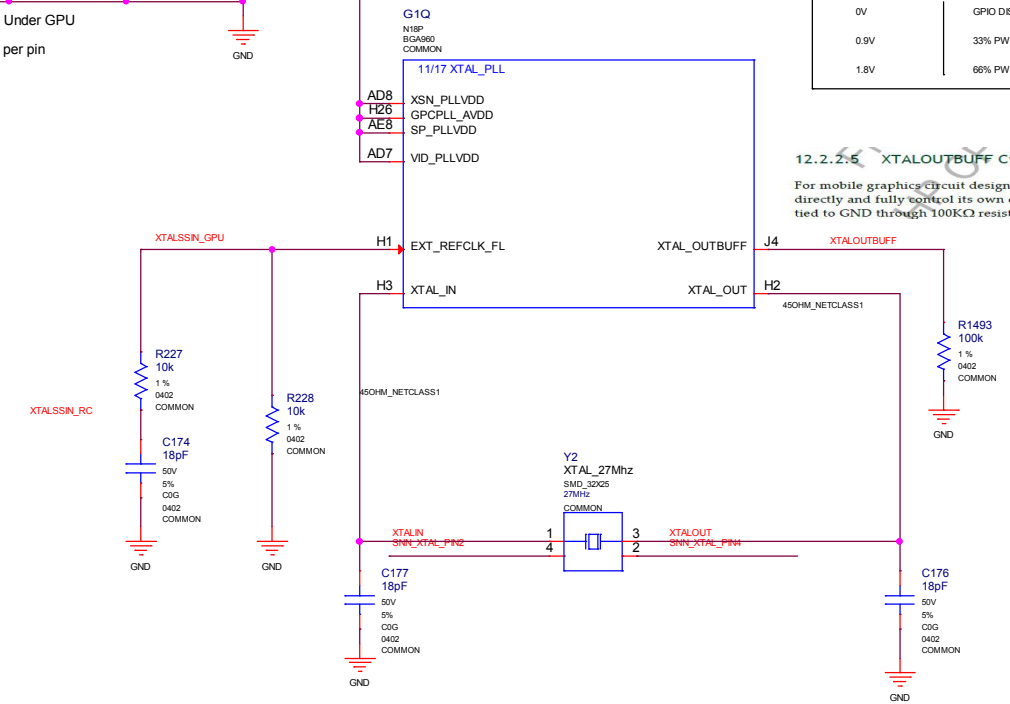


Place Under GPU

1 cap per pin

SmartFan Strap Table

Voltage	Inverted SmartFan PWM %
0V	GPIO DISABLED
0.9V	33% PWM
1.8V	66% PWM



12.2.2.5 XTALOUTBUFF Circuit Node

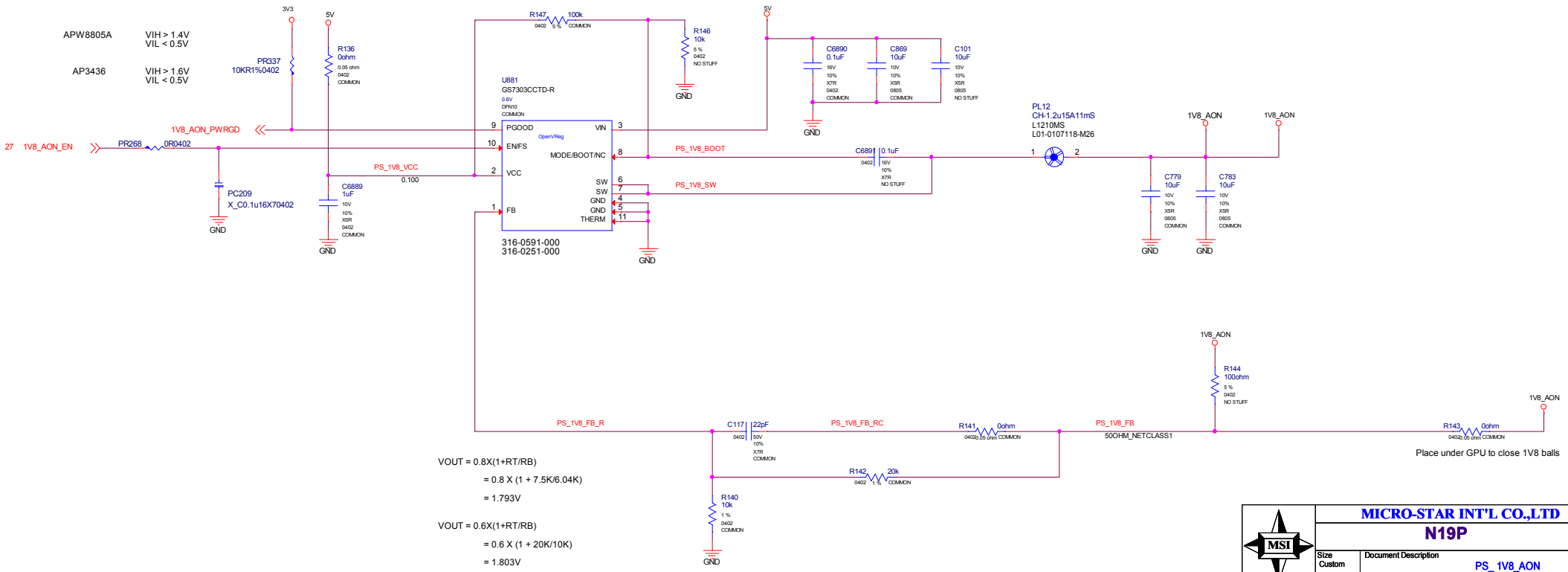
For mobile graphics circuit designs (or other designs wherein the graphics circuit does not directly and fully control its own cooling fan), the XTALOUTBUFF circuit node must be tied to GND through 100KΩ resistors.

MICRO-STAR INT'L CO.,LTD		
N19P		
Size B	Document Description: GPU_ XTAL, PLL	Rev 1.0
Date: Wednesday, July 10, 2019	Sheet 17 of 29	

PS: 1V8_AON

Voltage = 1.8V
Current = ? A
OCP(typi) = ? A

1V8_AON



Place under GPU to close 1V8 balls

VOUT = 0.8X(1+RT/RB)

= 0.8 X (1 + 7.5K/6.04K)

= 1.793V

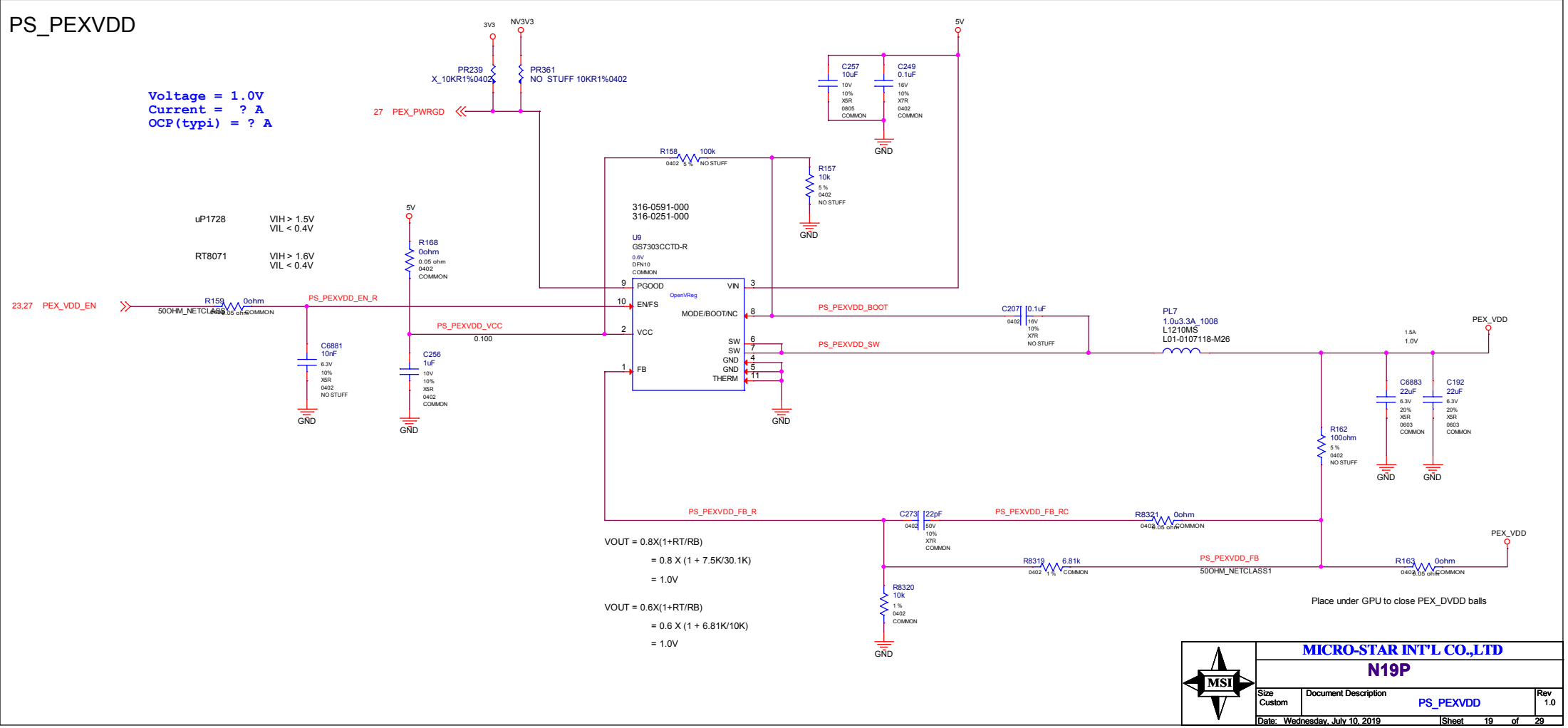
VOUT = 0.6X(1+RT/RB)

= 0.6 X (1 + 20K/10K)

= 1.803V

MICRO-STAR INT'L CO.,LTD		
N19P		
Size: Custom	Document Description: PS_ 1V8_AON	Rev: 1.0
Date: Wednesday, July 10, 2019	Sheet 18 of 29	

PS_PEXVDD

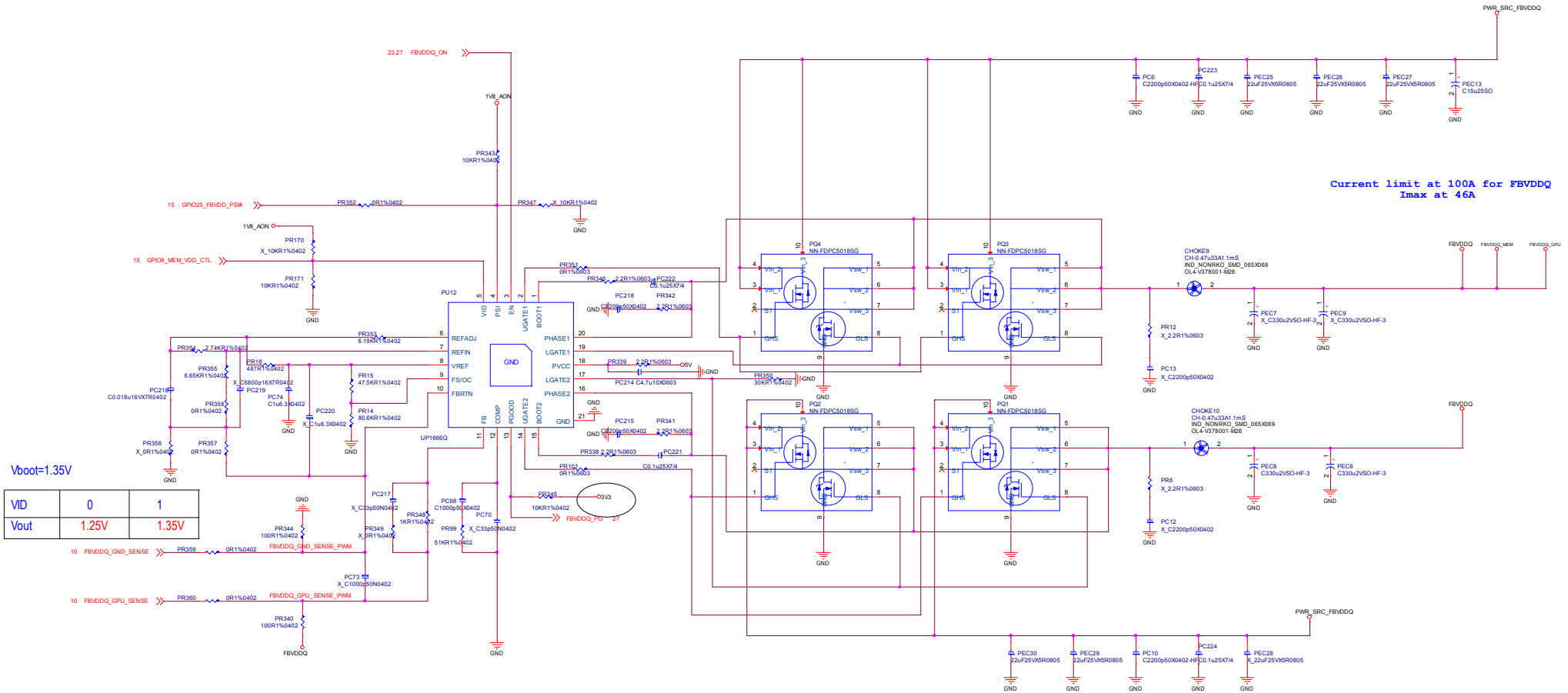


MICRO-STAR INT'L CO.,LTD		
N19P		
Size: Custom	Document Description: PS_PEXVDD	Rev: 1.0
Date: Wednesday, July 10, 2019	Sheet 19 of 29	

BLANK

MSI	MICRO-STAR INT'L CO.,LTD	
	N19P	
Size A	Document Description PS_ NV3V3	Rev 1.0
Date: Wednesday, July 10, 2019	Sheet 20 of 29	

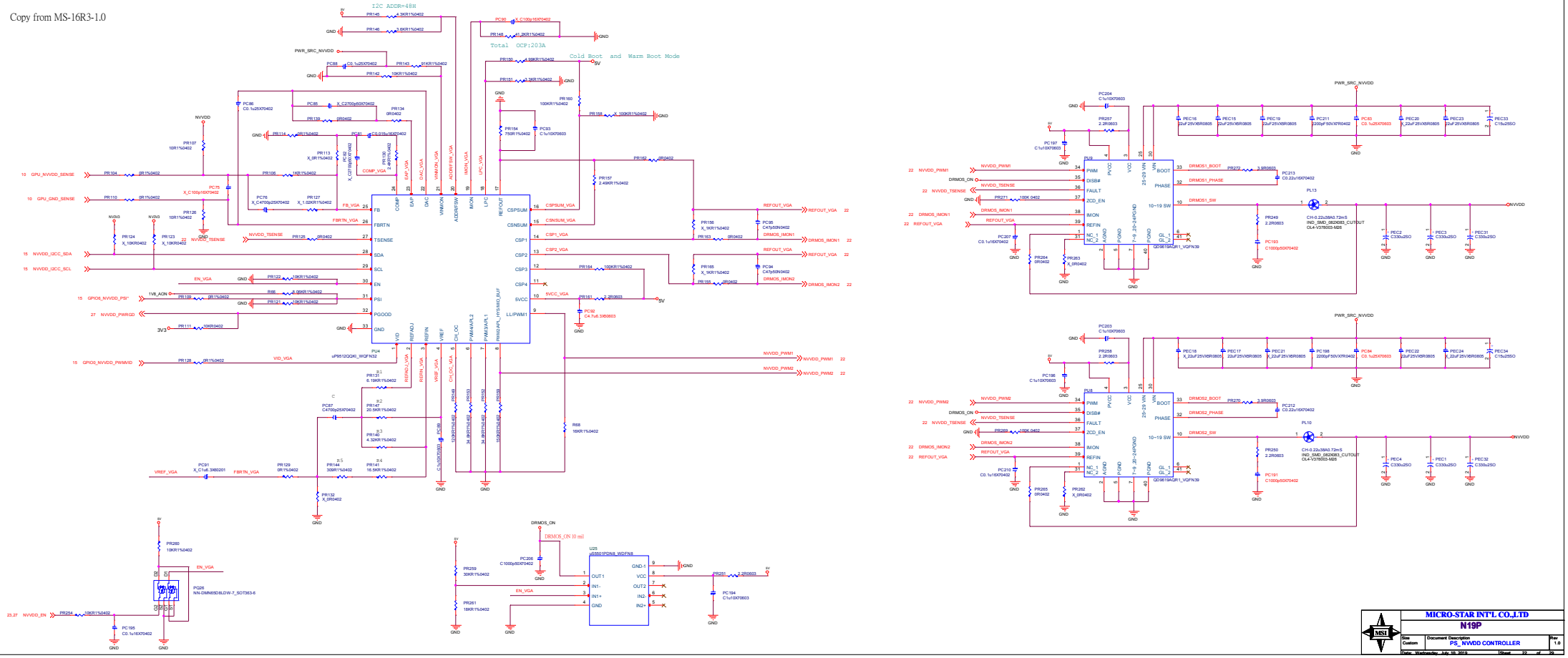
PS: FBVDD CONTROLLER



MICRO-STAR INT'L CO.,LTD		
N19P		
Size: Custom	Document Description: PS_ FBVDD CONTROLLER	Rev: 1.0
Date: Wednesday, July 10, 2019	Sheet 21 of 29	

PS: NVVDD CONTROLLER

Copy from MS-16R3-1.0



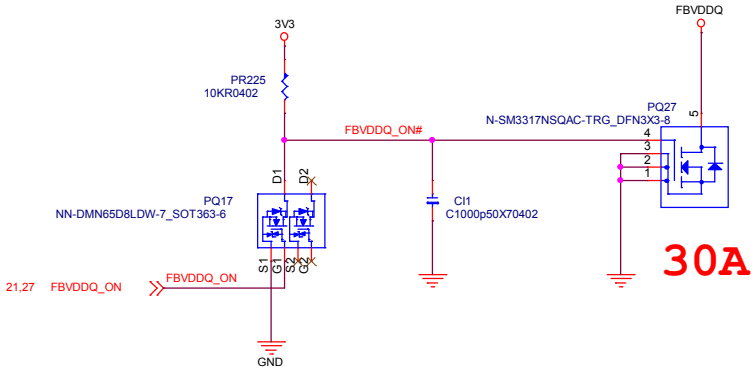
MICRO-STAR INT'L CO.,LTD

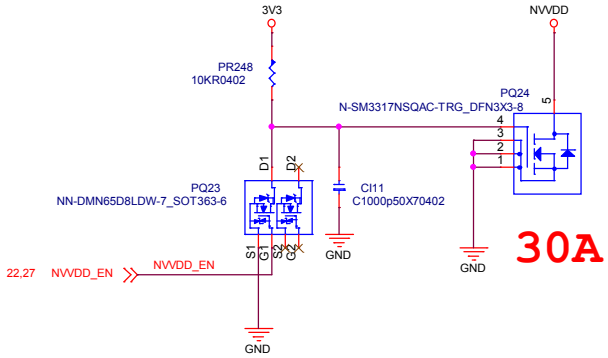
N19P

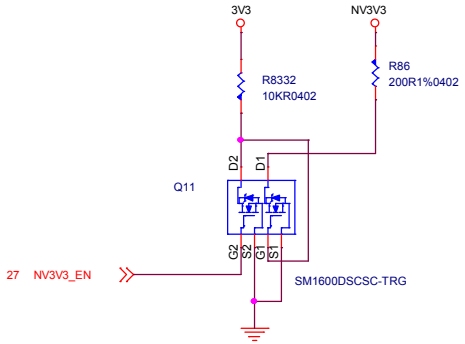
Size	Document Description	Rev
Custom	PS_ NVVDD CONTROLLER	1.0

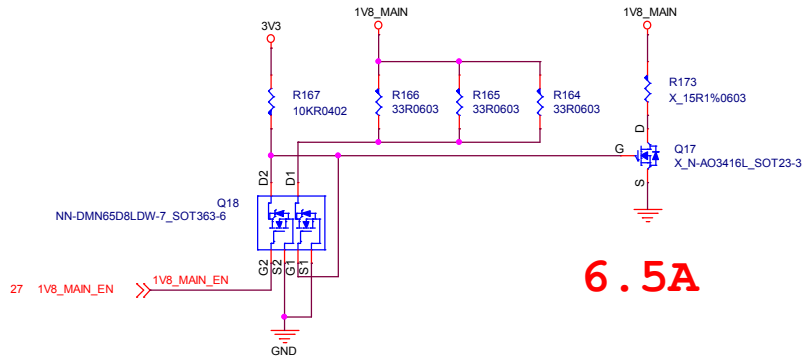
Date: Wednesday, July 30, 2014 | Sheet 22 of 29

Discharge

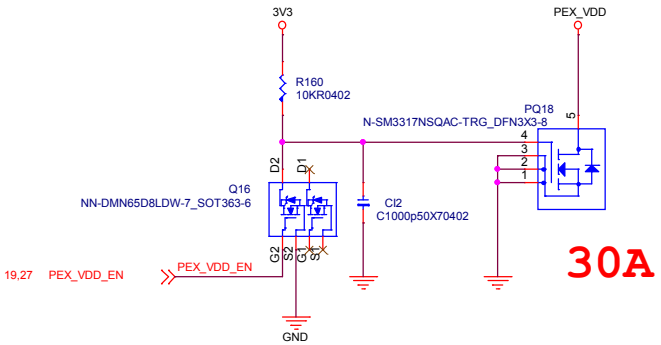








VGS(th): MIN:1.0 Max:2.0



MICRO-STAR INT'L CO.,LTD		
N19P		
Size: Custom	Document Description: DISCHARGE	Rev: 1.0
Date: Wednesday, July 10, 2019	Sheet 23 of 29	

Pin Name	N17P	N18P	N17P Functional Description	N17P Recommended Default Pull-up or Pull-down	N18P Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM	NVVDD_PWM_VID	PWM Output to control NVVDD	0 to 1V8 PWM output	
GPIO1	GC6_FB_EN	GC6_FB_EN	FB Enable for GC6 2.1	OD, 10K pull-down	OD, 10K pull-down
GPIO2	GPU_EVENT#	GPU_EVENT#	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON	10K pull-up to 1V8 _AON
GPIO3	NVVDDS_PWM	UNUSED	PWM output to control the NVVDDS power supply	0 to 1V8 output	
GPIO4	1V8_MAIN_EN	1V8_MAIN_EN	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8 _AON	OD, 10K pull-up to 1V8 _AON
GPIO5	FRM_LCK#	FRM_LCK#	Active low Frame Lock	OD, 10K pull-up to 1V8 _AON	OD, 10K pull-up to 1V8 _AON
GPIO6	NVVDD_PSI	NVVDD_PSI	Phase shedding	10K pull-up to 1V8 _AON	10K pull-up to 1V8 _AON
GPIO7	LCD_BL_PWM	LCD_BL_PWM	Panel Backlight PWM Brighteness Control	100K pull-down	100K pull-down
GPIO8	MEM_VDD_CTL	MEM_VDD_CTL	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	THERM_ALERT	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	MEM_VREF_CTL	Memory VREF Control	100K pull-down	100K pull-down
GPIO11	LCD_VCC	LCD_VCC	Panel Power Enable	100K pull-down	100K pull-down
GPIO12	PWR_LEVEL	PWR_LEVEL	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON	10K pull-up to 1V8_AON
GPIO13	LCD_BLEN	UNUSED	Panel Backlight Enable	100K pull-down	
GPIO14	HPD_A	HPD_A	Hot Plug Detect for IFPA		10K pull-up to 1V8 _AON
GPIO15	HPD_B	HPD_B	Hot Plug Detect for IFPB		10K pull-up to 1V8 _AON
GPIO16	SYS_PEX_RST_MON#	UNUSED	System side PCIe reset monitor	10K pull-up to 1V8 _AON	
GPIO17	HPD_D	HPD_D	Hot Plug Detect for IFPD		10K pull-up to 1V8 _AON
GPIO18	HPD_E	HPD_E	Hot Plug Detect for IFPE		10K pull-up to 1V8 _AON
GPIO19	3DVision	UNUSED	3D Vision L/R signal	100K pull-down	
GPIO20	GC5_MODE	NB_GC6			10K pull-down
GPIO21	UNUSED	LCD_BLEN			100K pull-down
GPIO22	UNUSED	ADC_MUX_SEL			2.2K pull-up See Circuit
GPIO23	GPU_PEX_RST_HOLD#	RESERVED	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3	100K pull-down
GPIO24	HPD_F	UNUSED	Hot Plug Detect for IFPF		
GPIO25	UNUSED	FBVDD_PSI#			
GPIO26	UNUSED	FP_FUSE			10K pull-down
GPIO27	HPD_C	HPD_C	Hot Plug Detect for IFPC		10K pull-up to 1V8 _AON

MSI

MICRO-STAR INT'L CO.,LTD

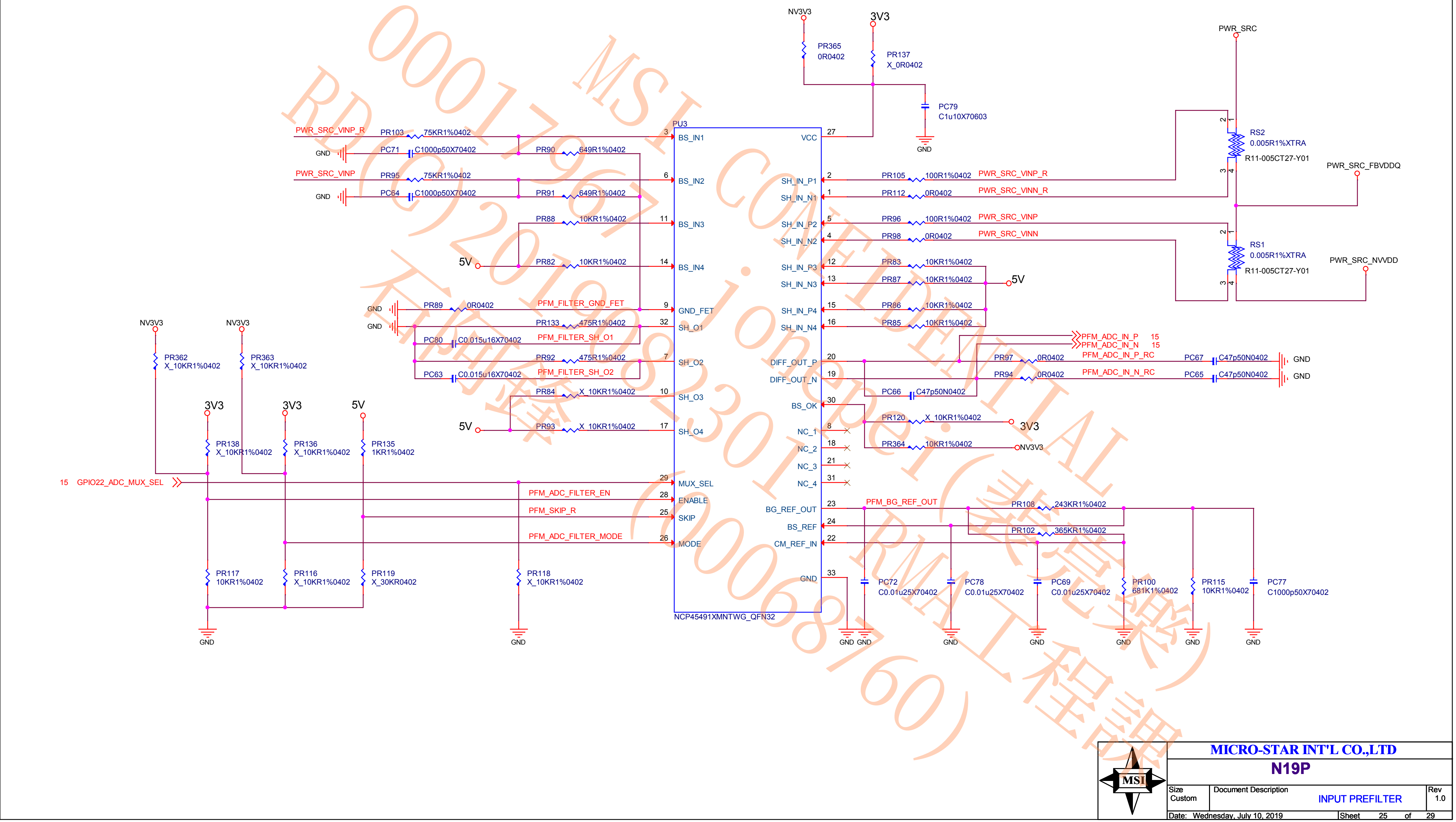
N19P

Size	Document Description	Rev
B	GPIO Functional Description	1.0

Date: Wednesday, July 10, 2019 Sheet 24 of 29

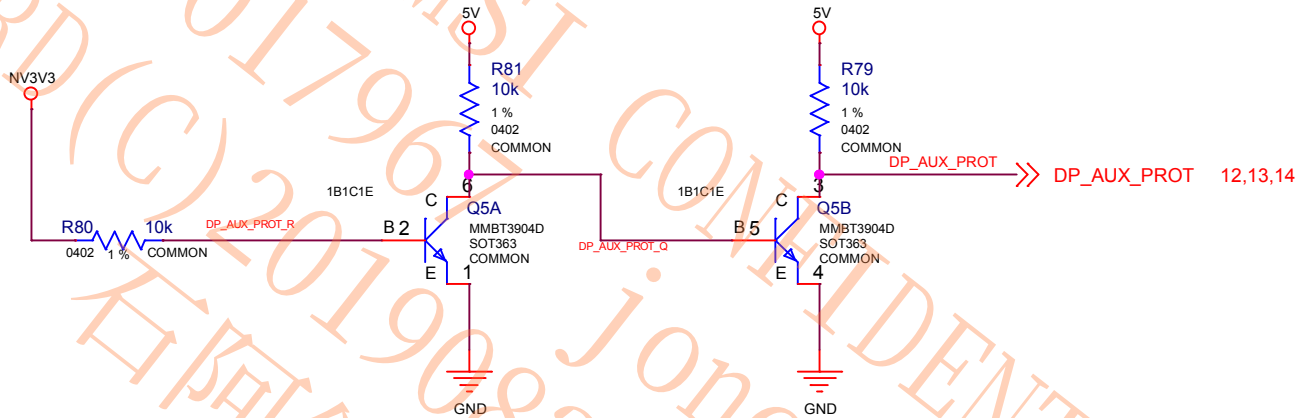
INPUT PREFILTER

On Semi	PR90,PR91	PR92,PR133	PR108	PR95,PR103	PC64,PC71
CONFIG	R954,R924	R977,R923	R950	R953,R952	C841,C836
N18P-G0	649R	475R	243K	75K	1.0nF



SEQUENCE:5V,1V8,NV3V3 ENABLE

DP_AUX Protection

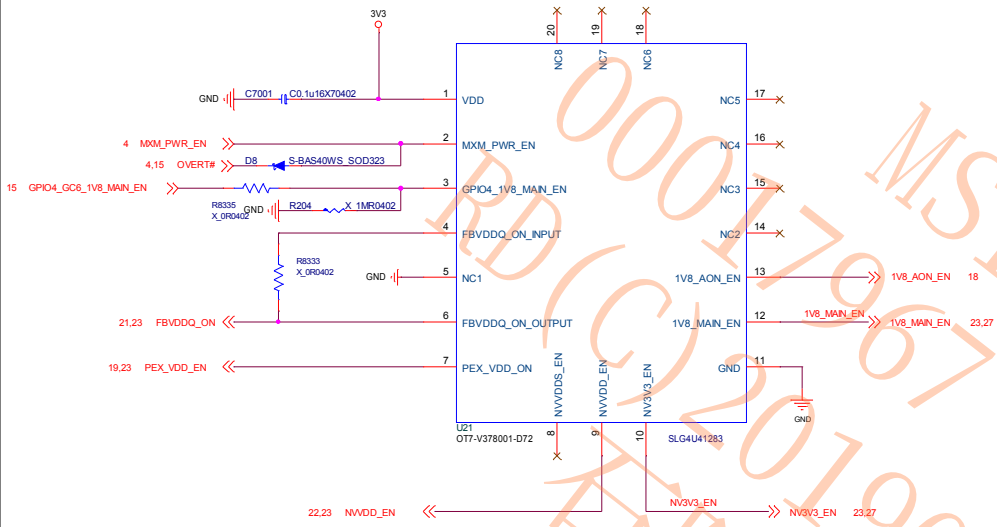


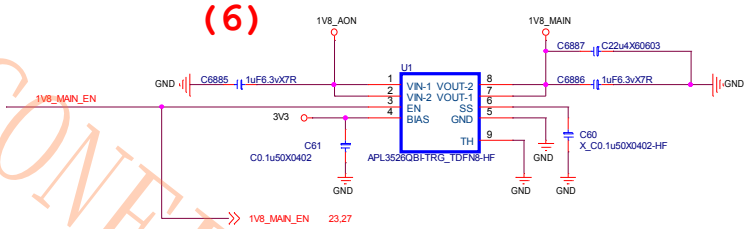
MSI	MICRO-STAR INT'L CO.,LTD	
	N19P	
Size A	Document Description: DP_AUX Protection	Rev 1.0
Date: Wednesday, July 10, 2019	Sheet 26 of 29	

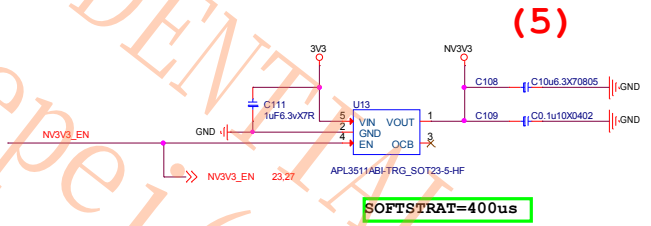
Power Sequence Control

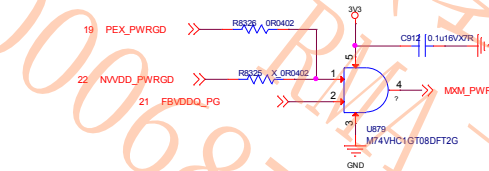
POWER ON= 1V8_AON->1V8_MAIN->NV3V3->NVVDD->PEX_VDD->FBVDDQ->DGPU_PWRGD

POWER OFF= PEX_VDD/FBVDDQ->NVVDD->NV3V3->1V8_MAIN->1V8_AON









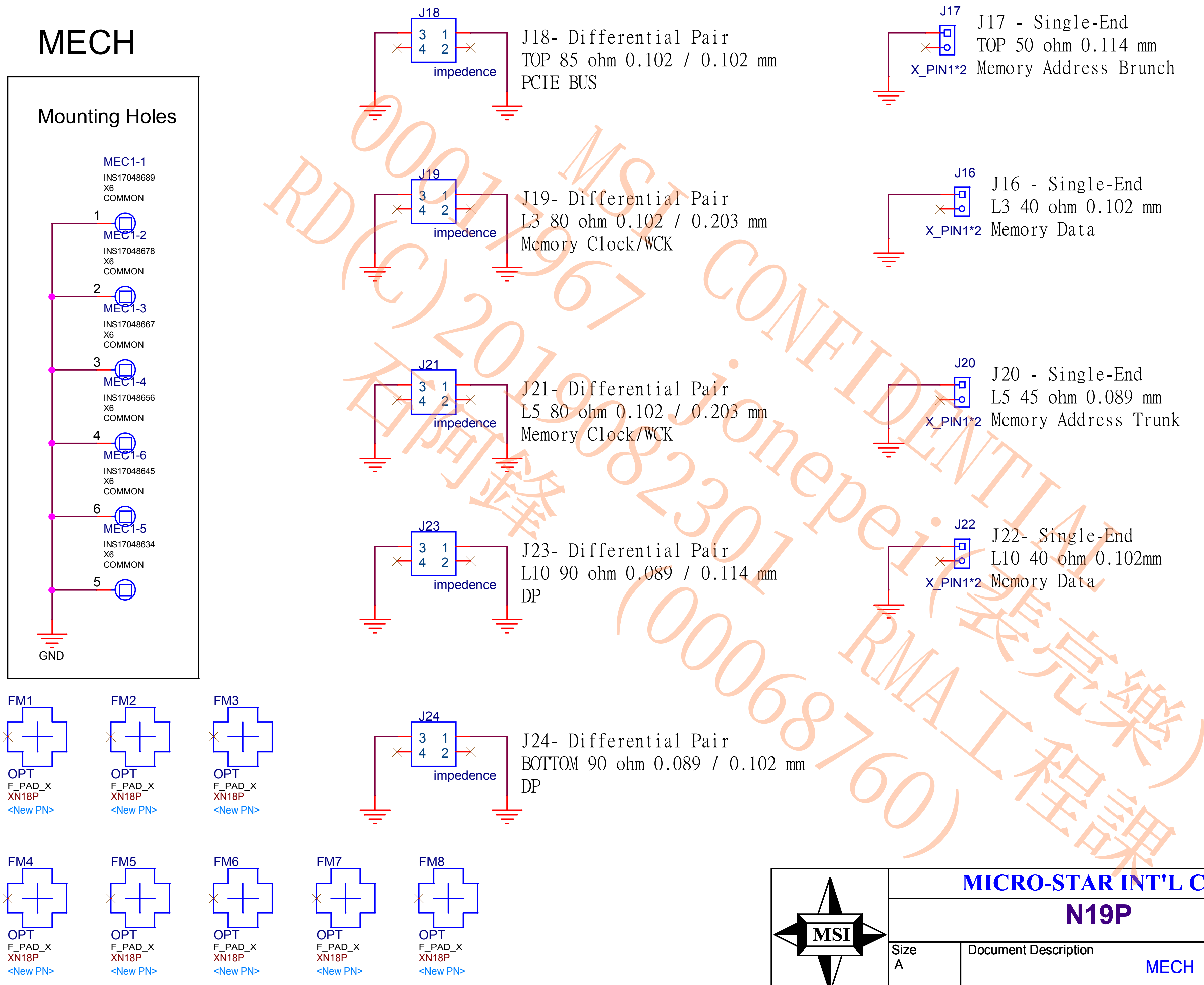
PIN2 MXM_PWR_EN is 3.3V INPUT
PIN3 GPIO4_GC6_PWR_EN is 1.8V INPUT
PIN4 FBVDDQ_ON_INPUT 3.3V INPUT
PIN6 FBVDDQ_ON_OUTPUT 3.3V OUTPUT
PIN7 PEX_VDD_EN_IC 3.3V OUTPUT
PIN9 NVVDD_EN_IC 3.3V OUTPUT
PIN12 1V8_MAIN_EN_IC 3.3V OUTPUT
PIN13 1V8_AON_EN_IC 3.3V OUTPUT

MICRO-STAR INT'L CO.,LTD
N19P
Size: Custom | Document Description: Sequence | Rev: 1.0
Date: Wednesday, July 10, 2019 | Sheet 27 of 29

SEQUENCE:DISCHARGE

MSI	MICRO-STAR INT'L CO.,LTD	
	N19P	
Size B	Document Description SEQUENCE_ DISCHARGE	Rev 1.0
Date: Wednesday, July 10, 2019	Sheet 28 of 29	

MECH



MICRO-STAR INT'L CO.,LTD		
N19P		
Size A	Document Description MECH	Rev 1.0
Date: Wednesday, July 10, 2019	Sheet 29 of 29	