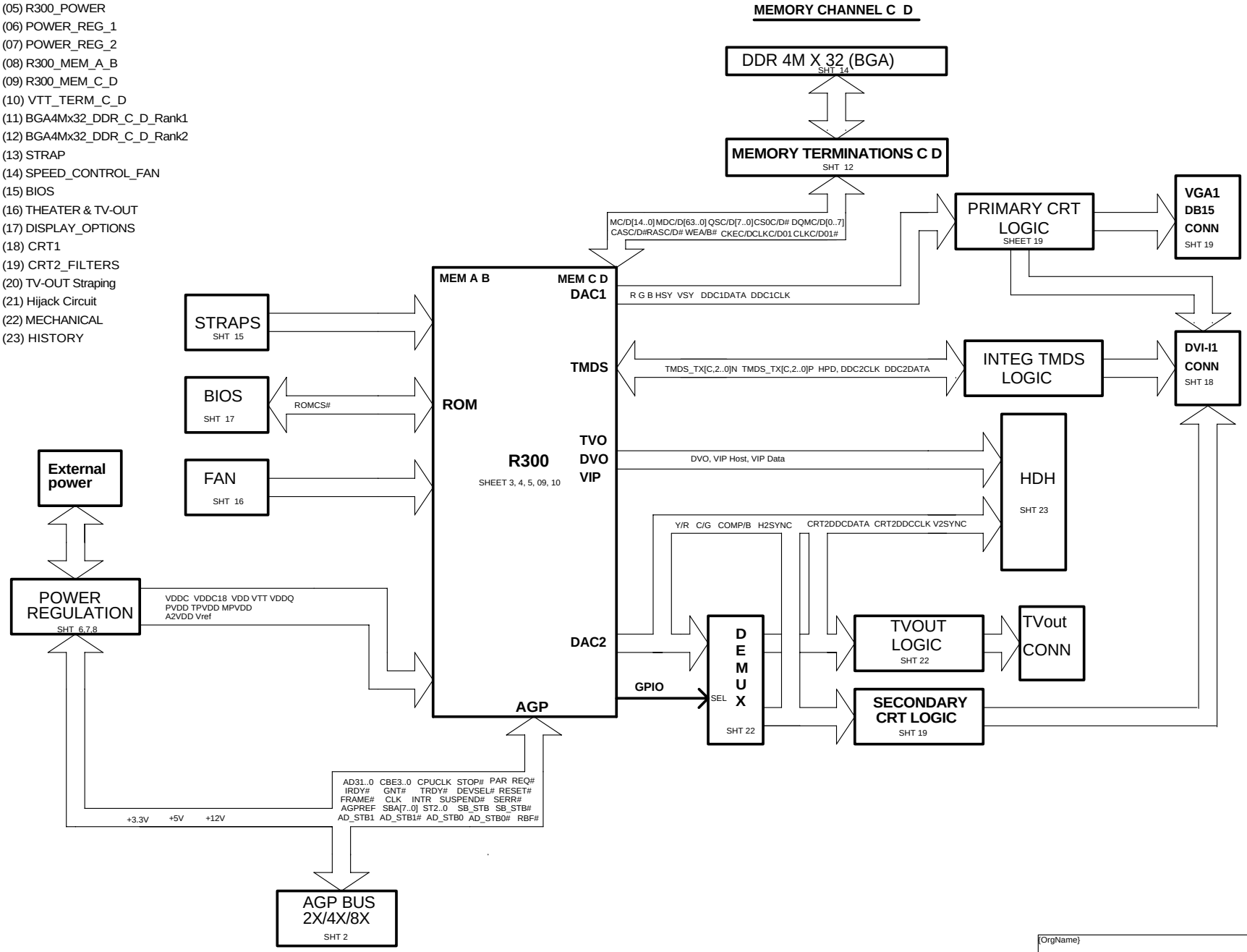
(01) Block
(02) AGP_4X/8X_BUS
(03) R300_AGP
(04) R300_MAIN
(05) R300_POWER
(06) POWER_REG_1
(07) POWER_REG_2
(08) R300_MEM_A_B
(09) R300_MEM_C_D
(10) VTT_TERM_C_D
(11) BGA4Mx32_DDR_C_D_Rank1
(12) BGA4Mx32_DDR_C_D_Rank2
(13) STRAP
(14) SPEED_CONTROL_FAN
(15) BIOS
(16) THEATER & TV-OUT
(17) DISPLAY_OPTIONS
(18) CRT1
(19) CRT2_FILTERS
(20) TV-OUT Straping
(21) Hijack Circuit
(22) MECHANICAL
(23) HISTORY



{OrgName}		
Size: Custom	Document Number: Block	Rev: 0A
Date: Wednesday, December 18, 2002	Sheet 1 of 21	

2X/4X/8X AGP BUS

GND_MPVSS GND_TPVSS GND_A2VSSN GND_AVSSQ GND_RSET GND_TVVSSN
GND_AVSSN GND_PVSS GND_TXVSSR GND_A2VSSQ GND_R2SET

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

+12V_BUS C1 4.7uF 16V ALU
+5V_BUS C2 100uF 16V
+3.3V_BUS C3 100uF 16V

AGP_C/BE#[3..0] AGP_AD[31..0] AGP_SBA[7..0] AGP_ST[2..0]

MAGP1 — UNIVERSAL AGP BUS

A1	12V	B1	OVRCNT#
A2	TYPEDET#	B2	5.0V
A3	GC_DET#/RESEVED	B3	5.0V
A4	USB-	B4	USB+
A5	GND	B5	GND
A6	INTA#	B6	INTB#
A7	RST#	B7	CLK
A8	GNT#	B8	REQ#
A9	VCC3.3	B9	VCC3.3
A10	ST1	B10	ST0
A11	MB_DET#/RESERVED	B11	ST2
A12	DBI_HI/PIPE#	B12	RBF#
A13	GND	B13	GND
A14	WBF#	B14	DBI_LO/RESERVED
A15	SBA1	B15	SBA0
A16	VCC3.3	B16	VCC3.3
A17	SBA3	B17	SBA2
A18	SB_STB#	B18	SB_STB
A19	GND	B19	GND
A20	SBA5	B20	SBA4
A21	SBA7	B21	SBA6
A22	KEY	B22	KEY
A23	KEY	B23	KEY
A24	KEY	B24	KEY
A25	KEY	B25	KEY
A26	AD30	B26	AD31
A27	AD28	B27	AD29
A28	VCC3.3	B28	VCC3.3
A29	AD26	B29	AD27
A30	AD24	B30	AD25
A31	GND	B31	GND
A32	AD_STB1#	B32	AD_STB1
A33	C/BE3#	B33	AD23
A34	VDDQ	B34	VDDQ
A35	AD22	B35	AD21
A36	AD20	B36	AD19
A37	GND	B37	GND
A38	AD18	B38	AD17
A39	AD16	B39	C/BE2#
A40	VDDQ	B40	VDDQ
A41	FRAME#	B41	IRDY#
A42	KEY	B42	KEY
A43	KEY	B43	KEY
A44	KEY	B44	KEY
A45	KEY	B45	KEY
A46	TRDY#	B46	DEVSEL#
A47	STOP#	B47	VDDQ
A48	PME#	B48	PERR#
A49	GND	B49	GND
A50	PAR	B50	SERR#
A51	AD15	B51	C/BE1#
A52	VDDQ	B52	VDDQ
A53	AD13	B53	AD14
A54	AD11	B54	AD12
A55	GND	B55	GND
A56	AD9	B56	AD10
A57	C/BE0#	B57	AD8
A58	VDDQ	B58	VDDQ
A59	AD_STB0#	B59	AD_STB0
A60	AD6	B60	AD7
A61	GND	B61	GND
A62	AD4	B62	AD5
A63	AD2	B63	AD3
A64	VDDQ	B64	VDDQ
A65	AD0	B65	AD1
A66	VREFGC	B66	VREFCG

TYDET R1 0R GND_TY

AGP_INTR# 3
AGP_GC_8X_DET# R2 0R
AGP_RST#
AGP_GNT# 3
AGP_MB_8X_DET# 3 R4 0R
AGP_DBI_HI 3 R5 0R
AGP_WBF# 3
AGP_SBSTB# 3 R7 8K2 +VDDQ_BUS
AGP_ADSTB1# 3 R9 8K2 +VDDQ_BUS
AGP_FRAME# 3
AGP_TRDY#_R 21
AGP_TRDY# 3,21
AGP_STOP# 3,21
AGP_STOP#_R 21 R13 X_0R R15 X_0R
AGP_PAR 3
AGP_ADSTB0# 3 R16 8K2 +VDDQ_BUS
AGP_VREFGC 3,21

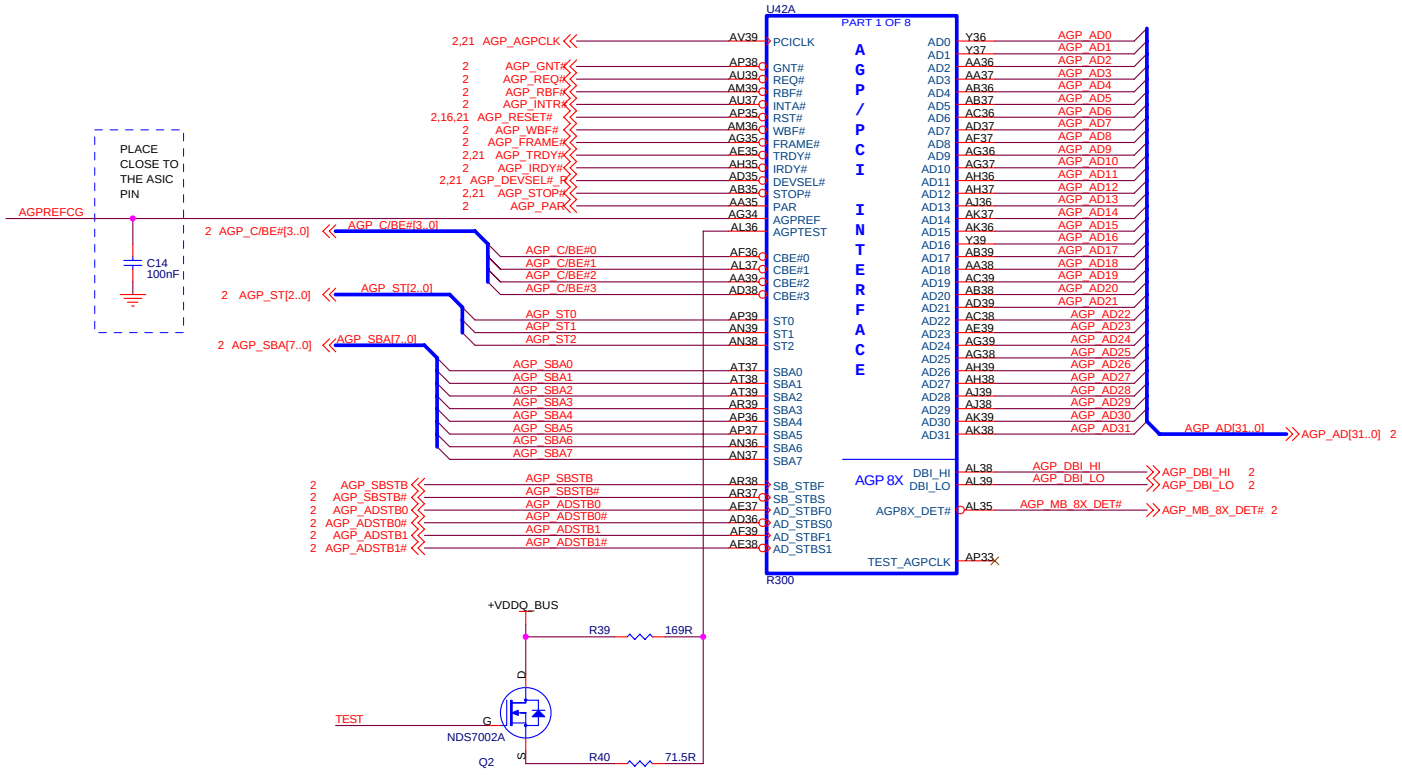
AGP_AGPCLK_R R3 0R AGP_AGPCLK 3,21
AGP_REQ# 3
C4 X_10pF
AGP_RBF# 3
AGP_DBI_LO_R R6 0R AGP_DBI_LO 3
AGP_SBSTB_R R8 0R AGP_SBSTB 3
AGP_ADSTB1_R R10 0R AGP_ADSTB1 3
AGP_IRDY# 3
AGP_DEVSEL#_R AGP_DEVSEL#_R 3,21
AGP_ADSTB0_R R17 0R AGP_ADSTB0 3
AGP_AGPREF 3
C1127 1.0uF

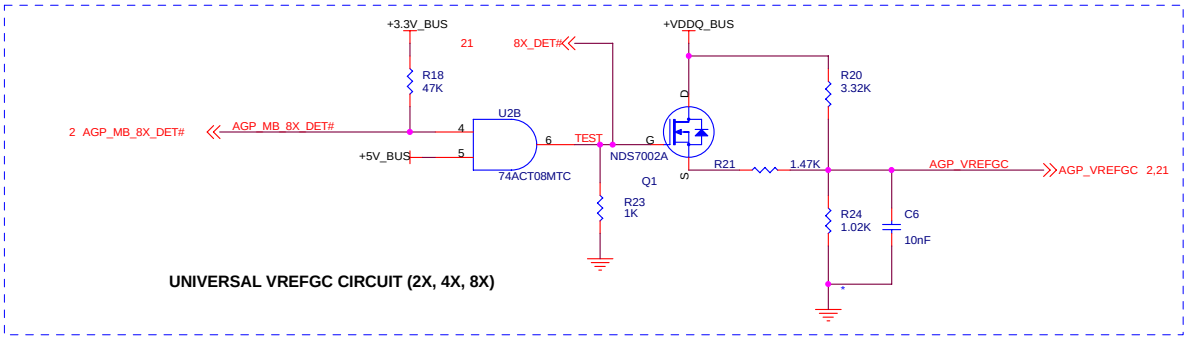
U2A 74ACT08MTC
3,16,21 AGP_RESET# R22 100R
C5 100nF R19 10K
AGP_RST#
PWGOOD_VDDC 6
R854 X_180R R25 180R
C731 X_100nF

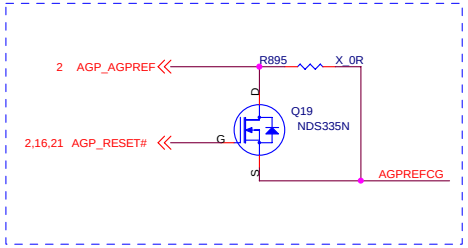
SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

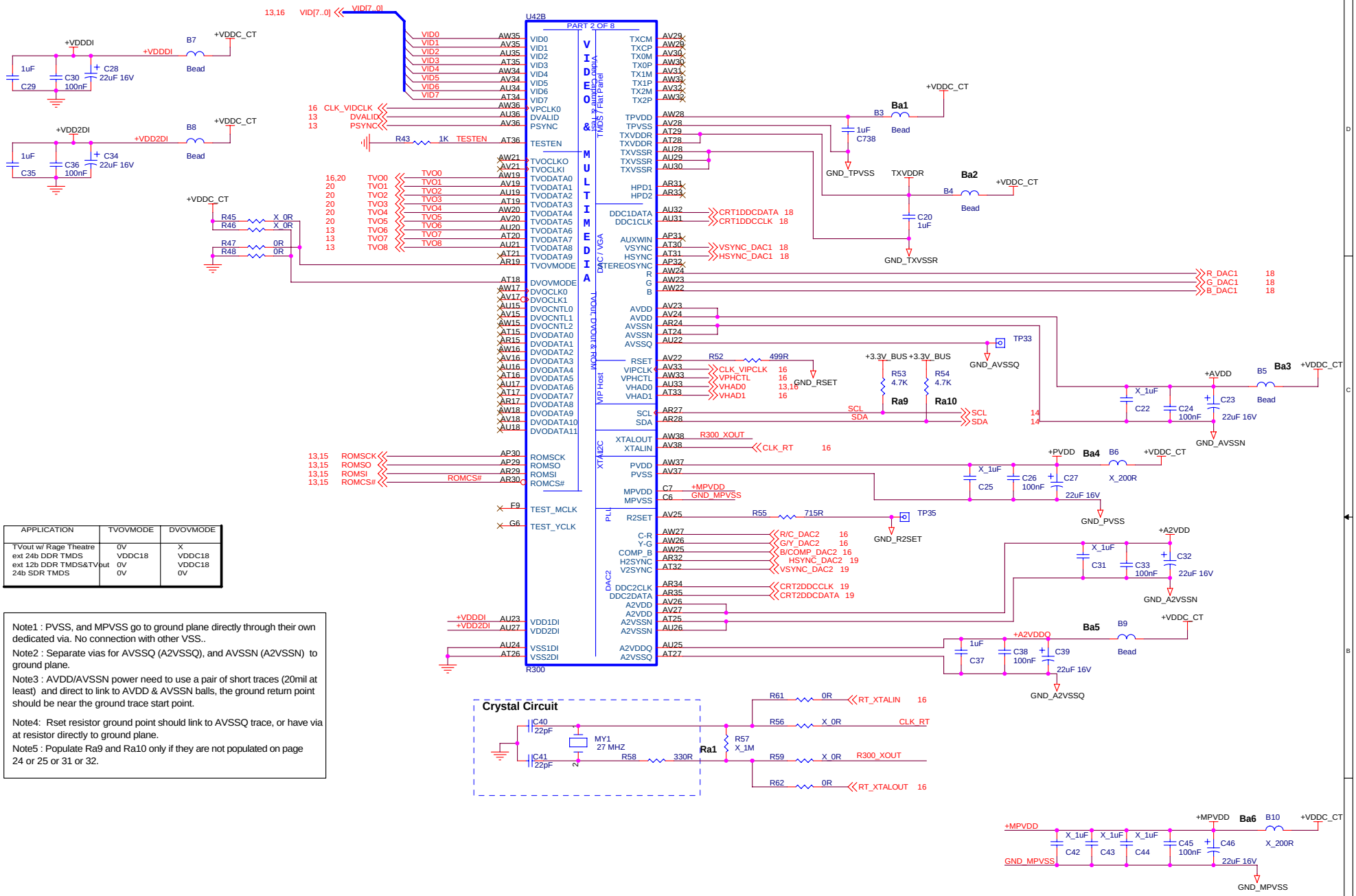
{OrgName}		
Size B	Document Number AGP_4X/8X_BUS	Rev 0A
Date: Wednesday, December 18, 2002	Sheet 2 of 23	







Size	Document Number	Rev
B	R300_AGP	0A
Date: Wednesday, December 18, 2002	Sheet 3 of 23	



APPLICATION	TVOVMODE	DVOVMODE
TVout w/ Rage Theatre	0V	X
ext 24b DDR TMDS	VDDC18	VDDC18
ext 12b DDR TMDS&TVout	0V	VDDC18
24b SDR TMDS	0V	0V

Note1 : PVSS, and MPVSS go to ground plane directly through their own dedicated via. No connection with other VSS..

Note2 : Separate vias for AVSSQ (A2VSSQ), and AVSSN (A2VSSN) to ground plane.

Note3 : AVDD/AVSSN power need to use a pair of short traces (20mil at least) and direct to link to AVDD & AVSSN balls, the ground return point should be near the ground trace start point.

Note4: Rset resistor ground point should link to AVSSQ trace, or have via at resistor directly to ground plane.

Note5 : Populate Ra9 and Ra10 only if they are not populated on page 24 or 25 or 31 or 32.

{Variant Name}

{OrgName}

Size	Document Number	Rev
B	R300_MAIN	0A

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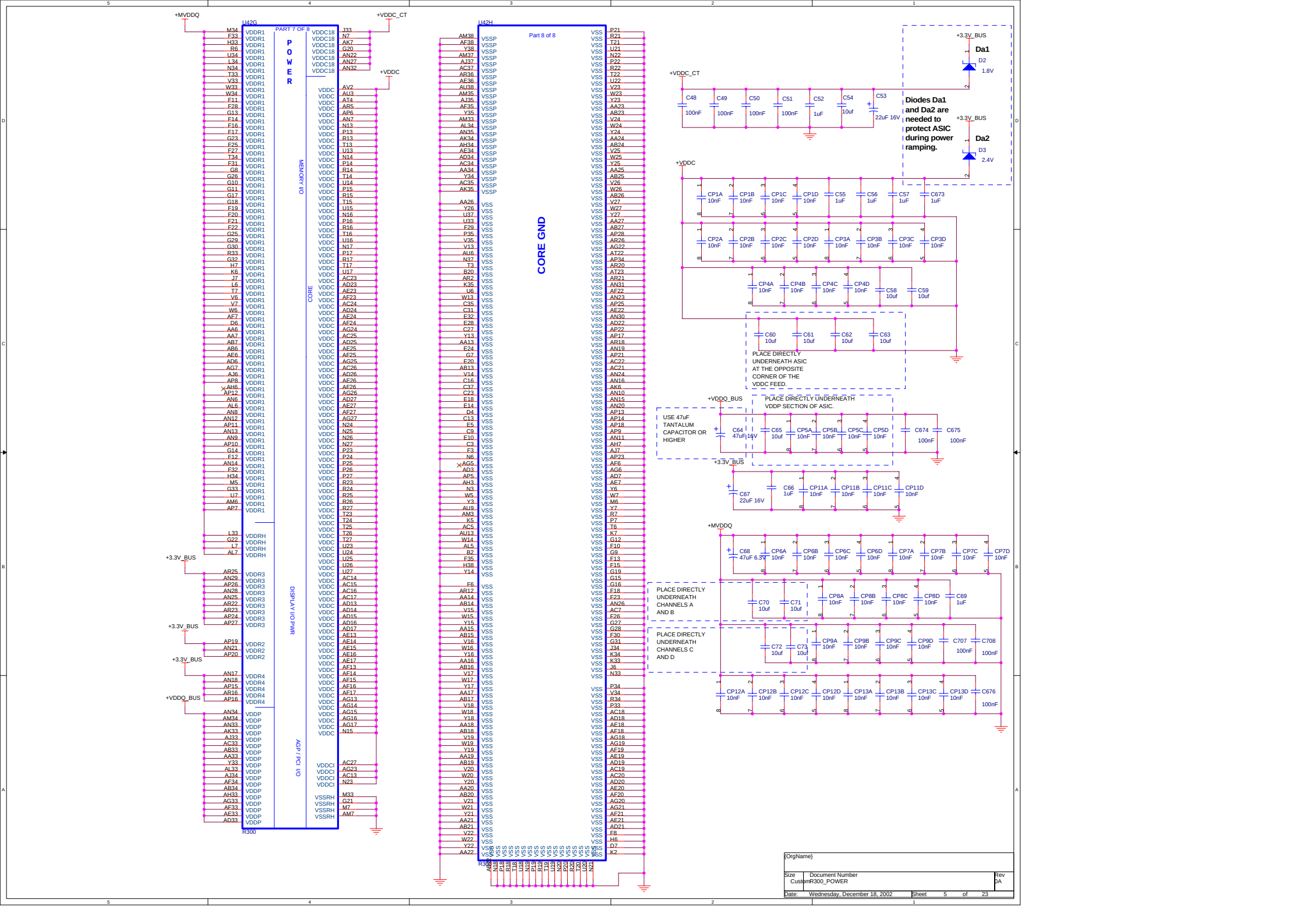
+MVDDQ
+VDDC_CT
+VDDC
+3.3V_BUS
+VDDQ_BUS
U42G
PART 7 OF 8
POWER
MEMORY I/O
CORE
DISPLAY I/O PWR
AGP / PCI-E I/O
R300
U42H
Part 8 of 8
CORE GND
Diodes Da1 and Da2 are needed to protect ASIC during power ramping.
Da1
D2
1.8V
Da2
D3
2.4V
PLACE DIRECTLY UNDERNEATH ASIC AT THE OPPOSITE CORNER OF THE VDDC FEED.
PLACE DIRECTLY UNDERNEATH VDDP SECTION OF ASIC.
USE 47uF TANTALUM CAPACITOR OR HIGHER
PLACE DIRECTLY UNDERNEATH CHANNELS A AND B
PLACE DIRECTLY UNDERNEATH CHANNELS C AND D
{OrgName}
Size Custom
Document Number R300_POWER
Rev 0A
Date: Wednesday, December 18, 2002
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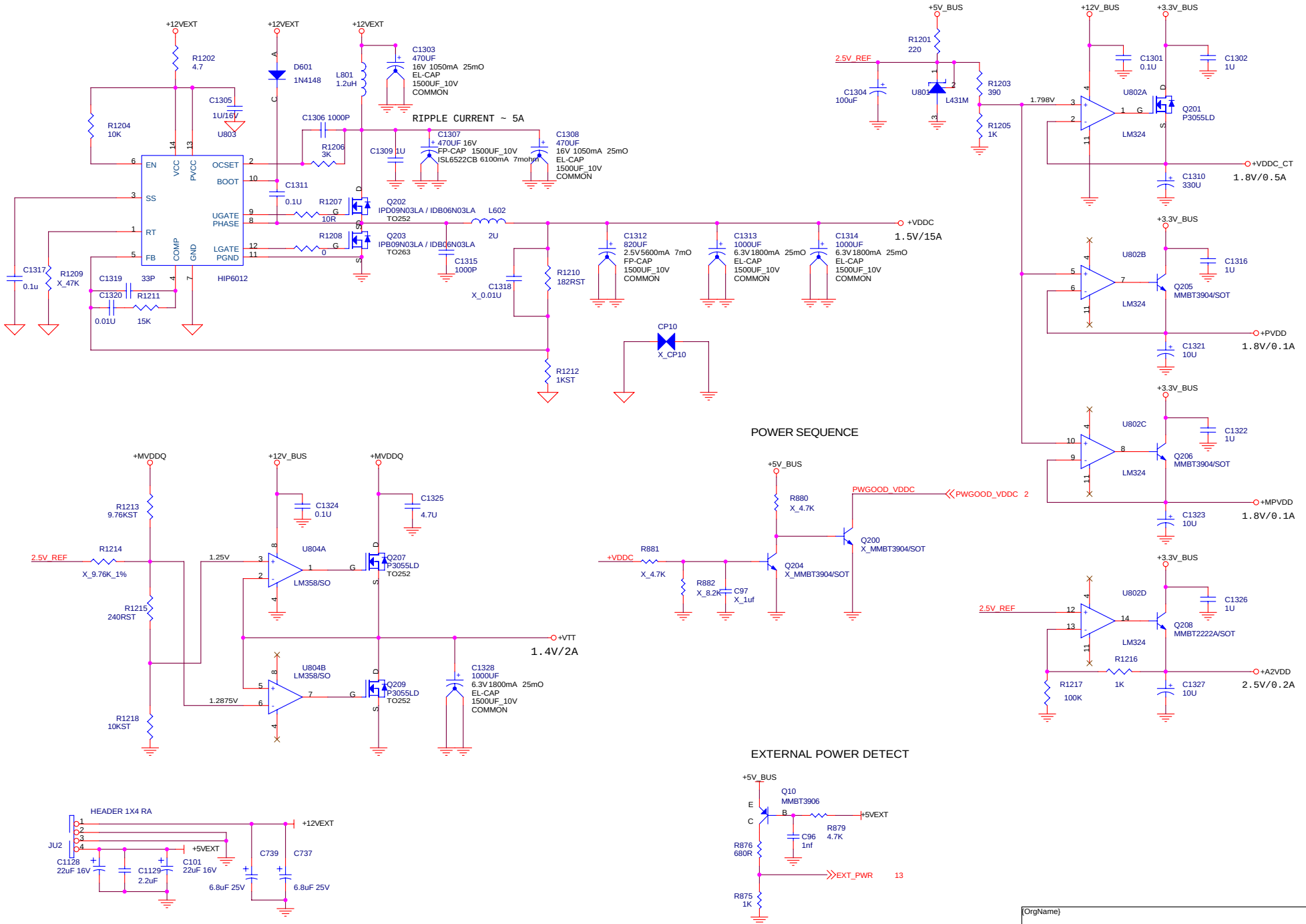

{OrgName}			
Size: Custom	Document Number: POWER_REG_1		Rev: 0A
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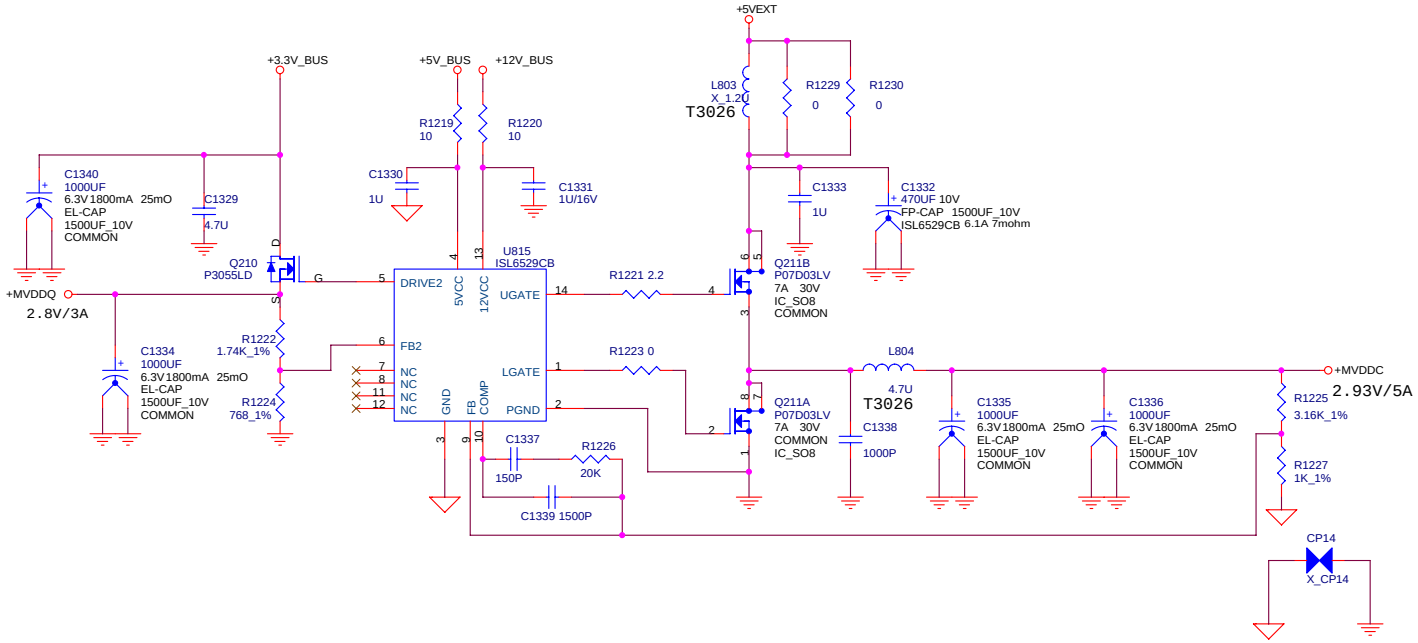
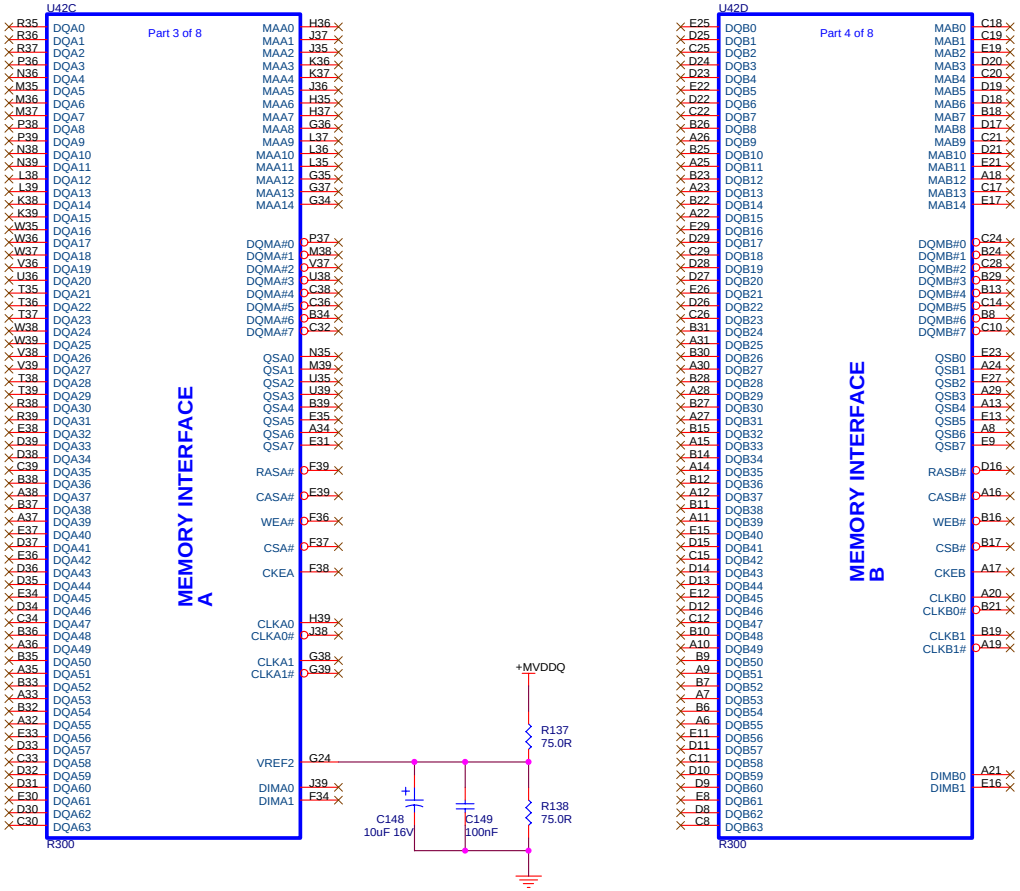


{OrgName}			
Size: Custom	Document Number: POWER_REG_2		Rev: 0A
Date: Wednesday, December 18, 2002	Sheet 7 of 23		

R-300
MEMORY CHANNELS A and B



{OrgName}		
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R-300
MEMORY CHANNELS C and D

MAC8X / MAC9X
R905 0R MAC8
R907 X_0R
R889 0R
R887 X_0R MAC9

MAD8X / MAD9X
R906 0R MAD8
R908 X_0R
R890 0R
R888 X_0R MAD9

POPULATE R907,R887,R908,R888 FOR SAMSUNG 8X32 ONLY

10,11,12 MAC[14..0] MAC[14..0]
10 MDC[63..0]

U42E — Part 5 of 8 — MEMORY INTERFACE C — R300

MDC0 G4 DQC0
MDC1 G3 DQC1
MDC2 H5 DQC2
MDC3 H4 DQC3
MDC4 J4 DQC4
MDC5 J3 DQC5
MDC6 K4 DQC6
MDC7 K3 DQC7
MDC8 D2 DQC8
MDC9 D1 DQC9
MDC10 E2 DQC10
MDC11 E1 DQC11
MDC12 G2 DQC12
MDC13 G1 DQC13
MDC14 H2 DQC14
MDC15 H1 DQC15
MDC16 C5 DQC16
MDC17 C4 DQC17
MDC18 D5 DQC18
MDC19 D3 DQC19
MDC20 E6 DQC20
MDC21 F5 DQC21
MDC22 F4 DQC22
MDC23 G5 DQC23
MDC24 B5 DQC24
MDC25 A5 DQC25
MDC26 B4 DQC26
MDC27 A4 DQC27
MDC28 A2 DQC28
MDC29 B1 DQC29
MDC30 C2 DQC30
MDC31 C1 DQC31
MDC32 P2 DQC32
MDC33 P1 DQC33
MDC34 R2 DQC34
MDC35 R1 DQC35
MDC36 U2 DQC36
MDC37 U1 DQC37
MDC38 V2 DQC38
MDC39 V1 DQC39
MDC40 U4 DQC40
MDC41 U3 DQC41
MDC42 V5 DQC42
MDC43 V4 DQC43
MDC44 W3 DQC44
MDC45 Y5 DQC45
MDC46 Y4 DQC46
MDC47 AA5 DQC47
MDC48 W2 DQC48
MDC49 W1 DQC49
MDC50 Y2 DQC50
MDC51 Y1 DQC51
MDC52 AB2 DQC52
MDC53 AB1 DQC53
MDC54 AC2 DQC54
MDC55 AC1 DQC55
MDC56 AA4 DQC56
MDC57 AA3 DQC57
MDC58 AB5 DQC58
MDC59 AB4 DQC59
MDC60 AC3 DQC60
MDC61 AD5 DQC61
MDC62 AD4 DQC62
MDC63 AE5 DQC63

MAC0 N2 MAC0
MAC1 N5 MAC1
MAC2 M2 MAC2
MAC3 M4 MAC3
MAC4 M3 MAC4
MAC5 M1 MAC5
MAC6 N4 MAC6
MAC7 N1 MAC7
MAC8 P4 MAC8X — MAC8
MAC9 L3 MAC9X — MAC9
MAC10 L4 MAC10
MAC11 L5 MAC11
MAC12 P5 MAC12
MAC13 P3 MAC13
MAC14 P6 MAC14

DQMC#0 H3 DQMC#0
DQMC#1 F2 DQMC#1
DQMC#2 E4 DQMC#2
DQMC#3 B3 DQMC#3
DQMC#4 T2 DQMC#4
DQMC#5 V3 DQMC#5
DQMC#6 AA2 DQMC#6
DQMC#7 AB3 DQMC#7
DQMC#[7..0] 10

QSC0 J5 QSC0
QSC1 F1 QSC1
QSC2 E3 QSC2
QSC3 A3 QSC3
QSC4 T1 QSC4
QSC5 W4 QSC5
QSC6 AA1 QSC6
QSC7 AC4 QSC7
QSC[7..0] 10

RASC# R4 RASC# — RASC# 10,11,12
CASC# T4 CASC# — CASC# 10,11,12
WEC# T5 WEC# — WEC# 10,11,12
CSC# R3 CSC# — CSC# 10,11
CKEC R5 — M_CKEC 10,11,12
CLKC0 K1 — M_CLKC0 10,11,12
CLKC0# J2 — M_CLKC0# 10,11,12
CLKC1 L2 — M_CLKC1 10,11,12
CLKC1# L1 — M_CLKC1# 10,11,12

C304 X_10pF C305 X_10pF C306 X_10pF C307 X_10pF FOR EMI

DIMC0 J1 R712 X_0R — DIMC0 11,12
DIMC1 U5 R713 X_0R — DIMC1 11,12

10,11,12 MAD[14..0] MAD[14..0]
10 MDD[63..0]

U42F — Part 6 of 8 — MEMORY INTERFACE D — R300

MDD0 AJ4 DQD0
MDD1 AJ3 DQD1
MDD2 AK5 DQD2
MDD3 AK4 DQD3
MDD4 AL3 DQD4
MDD5 AM5 DQD5
MDD6 AM4 DQD6
MDD7 AN5 DQD7
MDD8 AJ2 DQD8
MDD9 AJ1 DQD9
MDD10 AK2 DQD10
MDD11 AK1 DQD11
MDD12 AM2 DQD12
MDD13 AM1 DQD13
MDD14 AN2 DQD14
MDD15 AN1 DQD15
MDD16 AE4 DQD16
MDD17 AE3 DQD17
MDD18 AE5 DQD18
MDD19 AF4 DQD19
MDD20 AG3 DQD20
MDD21 AH5 DQD21
MDD22 AH4 DQD22
MDD23 AJ5 DQD23
MDD24 AD2 DQD24
MDD25 AD1 DQD25
MDD26 AE2 DQD26
MDD27 AE1 DQD27
MDD28 AG2 DQD28
MDD29 AG1 DQD29
MDD30 AH2 DQD30
MDD31 AH1 DQD31
MDD32 AV5 DQD32
MDD33 AW5 DQD33
MDD34 AV6 DQD34
MDD35 AW6 DQD35
MDD36 AV8 DQD36
MDD37 AW8 DQD37
MDD38 AV9 DQD38
MDD39 AW9 DQD39
MDD40 AT7 DQD40
MDD41 AU7 DQD41
MDD42 AR8 DQD42
MDD43 AT8 DQD43
MDD44 AT9 DQD44
MDD45 AR10 DQD45
MDD46 AT10 DQD46
MDD47 AU10 DQD47
MDD48 AV10 DQD48
MDD49 AW10 DQD49
MDD50 AV11 DQD50
MDD51 AW11 DQD51
MDD52 AV13 DQD52
MDD53 AW13 DQD53
MDD54 AV14 DQD54
MDD55 AW14 DQD55
MDD56 AR11 DQD56
MDD57 AT11 DQD57
MDD58 AU11 DQD58
MDD59 AT12 DQD59
MDD60 AT13 DQD60
MDD61 AR14 DQD61
MDD62 AT14 DQD62
MDD63 AU14 DQD63

MAD0 AT3 MAD0
MAD1 AT6 MAD1
MAD2 AR4 MAD2
MAD3 AP3 MAD3
MAD4 AR6 MAD4
MAD5 AR3 MAD5
MAD6 AT5 MAD6
MAD7 AU5 MAD7
MAD8 AU2 MAD8X — MAD8
MAD9 AP4 MAD9X — MAD9
MAD10 AN3 MAD10
MAD11 AN4 MAD11
MAD12 AU4 MAD12
MAD13 AU1 MAD13
MAD14 AV4 MAD14

DQMD#0 AK3 DQMD#0
DQMD#1 AL2 DQMD#1
DQMD#2 AF3 DQMD#2
DQMD#3 AF2 DQMD#3
DQMD#4 AV7 DQMD#4
DQMD#5 AU8 DQMD#5
DQMD#6 AV12 DQMD#6
DQMD#7 AU12 DQMD#7
DQMD#[7..0] 10

QSD0 AL4 QSD0
QSD1 AL1 QSD1
QSD2 AG4 QSD2
QSD3 AF1 QSD3
QSD4 AW7 QSD4
QSD5 AR9 QSD5
QSD6 AW12 QSD6
QSD7 AR13 QSD7
QSD[7..0] 10

RASD# AW4 RASD# — RASD# 10,11,12
CASD# AW2 CASD# — CASD# 10,11,12
WED# AW3 WED# — WED# 10,11,12
CSD# AV3 CSD# — CSD# 10,11
CKED AV1 — M_CKED 10,11,12
CLKD0 AR1 — M_CLKD0 10,11,12
CLKD0# AP2 — M_CLKD0# 10,11,12
CLKD1 AT2 — M_CLKD1 10,11,12
CLKD1# AT1 — M_CLKD1# 10,11,12

+MVDDQ
C308 X_10pF C309 X_10pF C310 X_10pF C311 X_10pF FOR EMI
VREF1 AC6 — R773 75.0R
C150 10uF 16V C151 100nF — R774 75.0R

DIMD0 AP1
DIMD1 AR7
MEMVMODE0 E7 — MEMMODE0
MEMVMODE1 F7 — MEMMODE1
MEMTEST F24
R166 47R

R714 X_0R — DIMD0 11,12
R715 X_0R — DIMD1 11,12

MEMMODE0 R164 4.7K
MEMMODE1 R165 X_4.7K DNI
+VDDC_CT
R167 4.7K
R168 X_4.7K DNI

+MVDDQ C893 0.1uF
+MVDDQ C894 0.1uF
+MVDDQ C895 0.1uF
+VDDC_CT C896 0.1uF
+VDDC_CT C897 0.1uF
+VDDC_CT C898 0.1uF

MEMVMODE[1:0]	MEMORY IO VOLTAGE
0 1	2.5V (DDR)
1 0	1.8V (DDR)
1 1	3.3V (SDR)

{OrgName}

Size	Document Number	Rev
B	R300_MEM_C_D	0A

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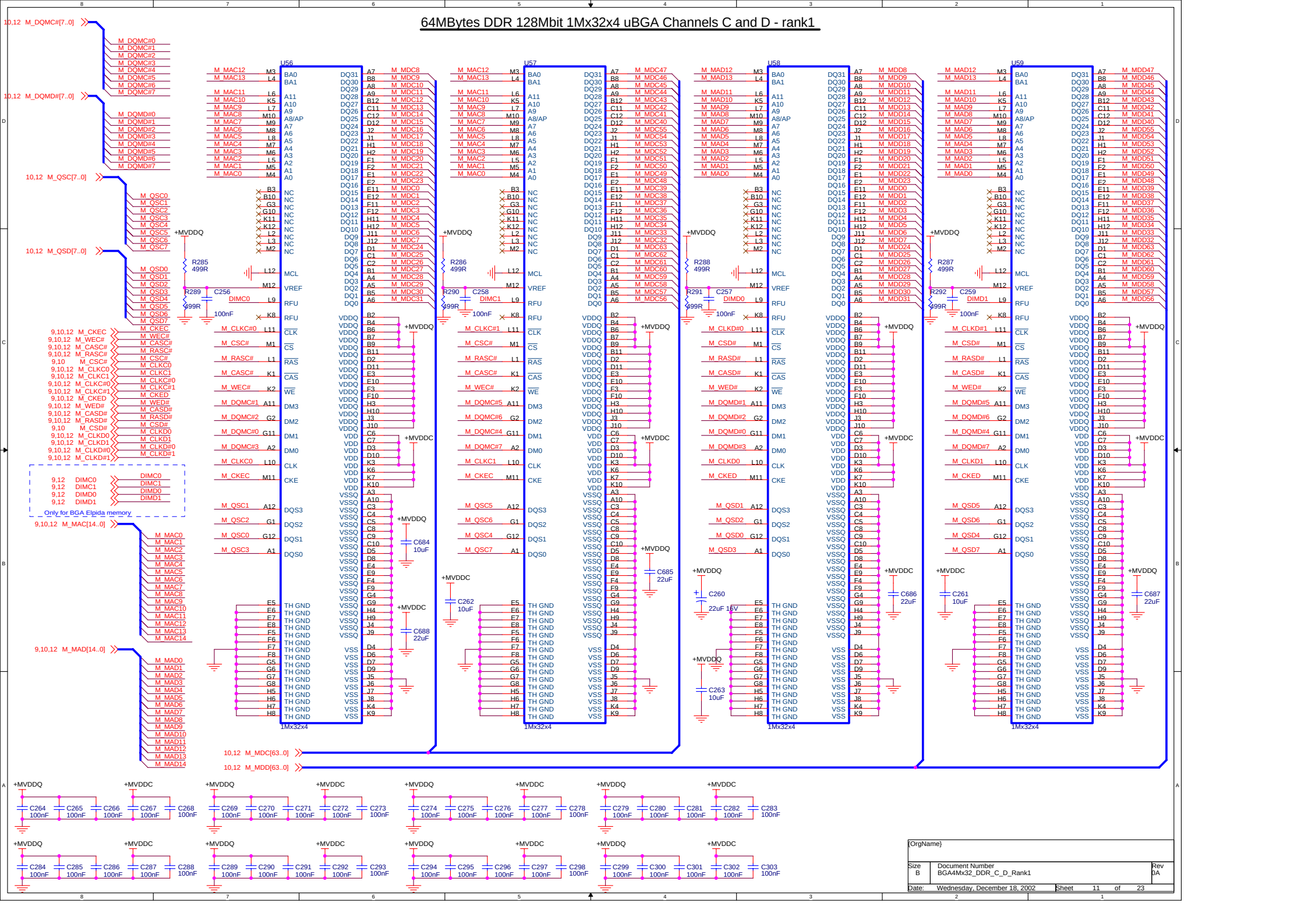
Vtt TERMINATION for DDR

Differential CLOCK termination

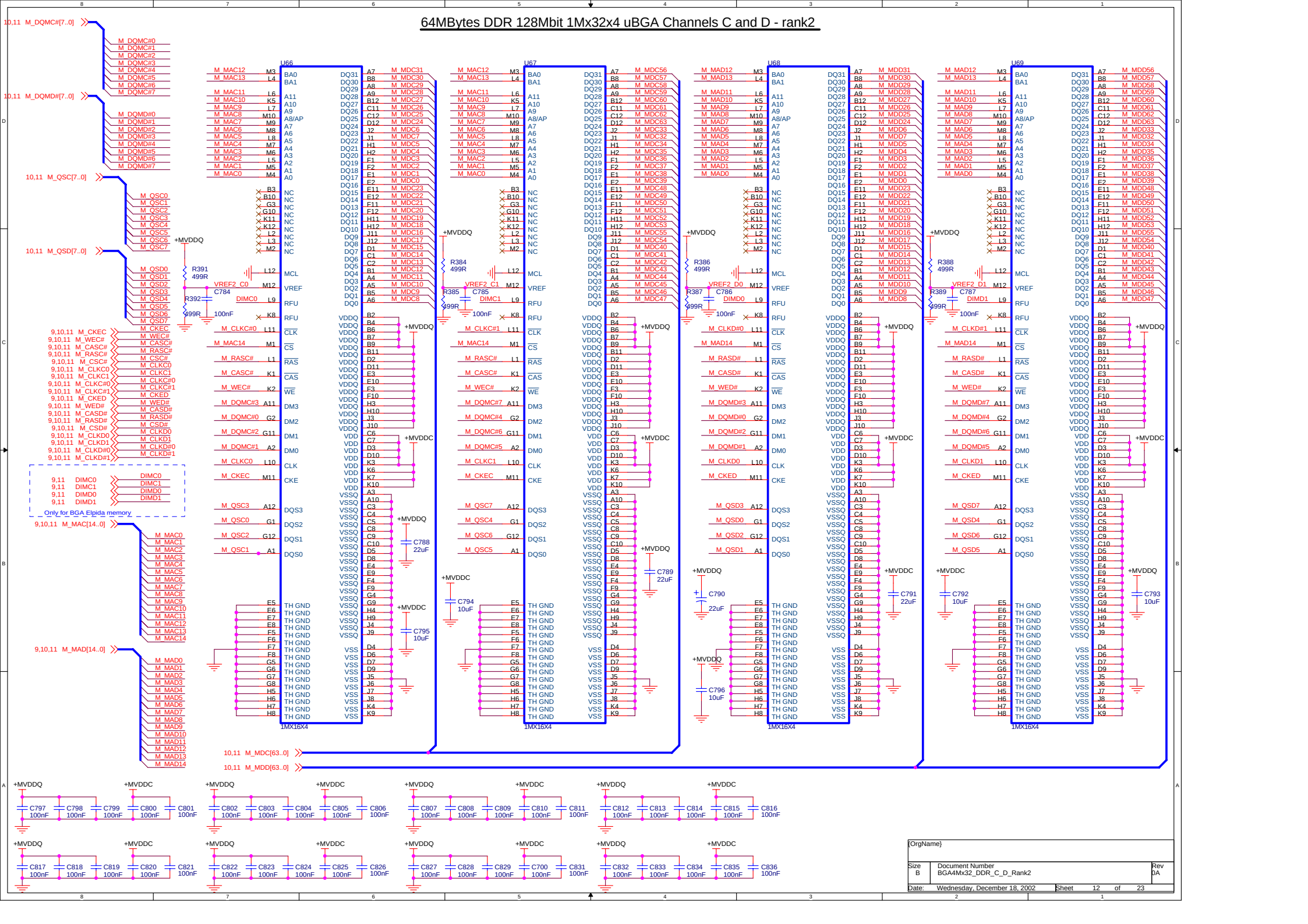
Differential termination should be placed close to the memory.

{OrgName}		
Size B	Document Number VTT_TERM_C_D	Rev 0A
Date: Wednesday, December 18, 2002	Sheet 10 of 23	

64MBytes DDR 128Mbit 1Mx32x4 uBGA Channels C and D - rank1

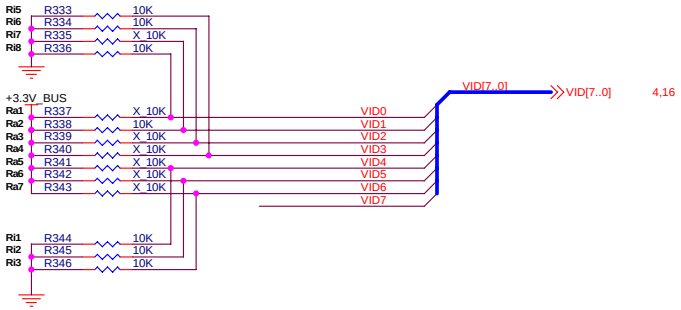


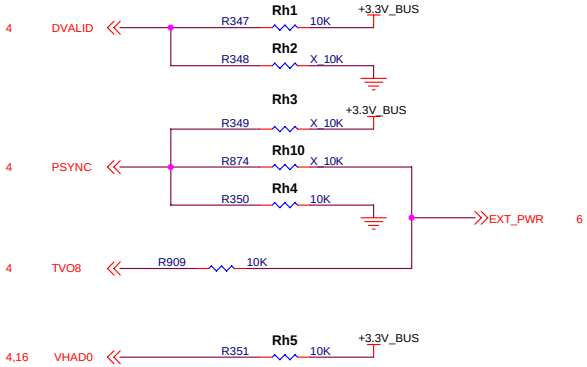
64MBytes DDR 128Mbit 1Mx32x4 uBGA Channels C and D - rank2

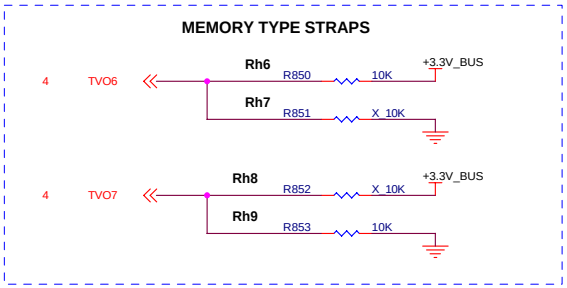


{OrgName}		
Size B	Document Number BGA4Mx32_DDR_C_D_Rank2	Rev 0A
Date: Wednesday, December 18, 2002	Sheet 12 of 23	

STRAPS







AGPFBSKEW -- VID(1:0)

Ra2	Ra1	Ri7	Ri8	
DNI	DNI	10K	10K	refclk slightly earlier than feedback (00)
DNI	10K	10K	DNI	refclk 1 tap earlier than feedback (01)
10K	DNI	DNI	10K	refclk 1 tap later than feedback DEFAULT (10)
10K	10K	DNI	DNI	refclk 2 taps earlier than feedback (11)

X0CLK_SKEW --VID(3:2)

Ra4	Ra3	Ri5	Ri6	
DNI	DNI	10K	10K	x0clk to agpclk 0 tap delay DEFAULT
DNI	10K	10K	DNI	x0clk to agpclk 1 tap delay
10K	DNI	DNI	10K	x0clk to agpclk 2 taps delay
10K	10K	DNI	DNI	x0clk to agpclk 3 taps delay

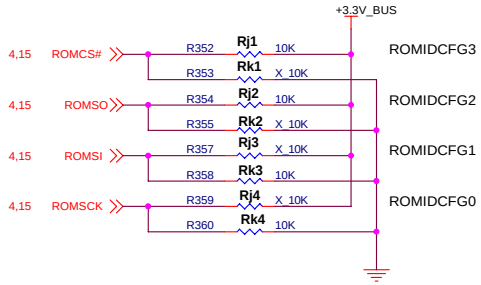
INSTALL	DEVICE ID
Rh1	NORMAL ID (default) Install it all the time when it is normal device ID
Rh2	Use workstation DEVICE_ID when WSEN = 1

INSTALL	DNI	ID_DISABLE
Rh4	**Rh10**	Normal operation
Rh3	**Rh10**	CHIP SHUTS DOWN
© **Rh10**	**Rh3 Rh4**	Circuitry for external power detection. (DEFAULT)

INSTALL	VIP DEVICE
Rh5	NO SLAVE VIP (DEFAULT) Install it when internal pull-up doesn't work
	SLAVE VIP --- VIP device will drive low when VIP is attached.

MEMORY TYPE STRAPS

MEMORY TYPE	Rh6	Rh7	Rh8	Rh9
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD



BUSCFG -- VID(6:4)

BUSTYPE_2 VID6		BUSTYPE_1 VID5		BUSTYPE_0 VID4		
Ra7	Ri3	Ra6	Ri2	Ra5	Ri1	AGP8X_DET = 0 (both GC and MB 8x capable) DESCRIPTION
DNI	10K	DNI	10K	DNI	10K	AGP 8X, 0.8V signaling PLL CLK, IDSEL = AD16
DNI	10K	DNI	10K	10K	DNI	AGP 8X, 0.8V signaling PLL CLK, IDSEL = AD17
DNI	10K	10K	DNI	DNI	10K	AGP 4X, 0.8V signaling PLL CLK, IDSEL = AD16
DNI	10K	10K	DNI	10K	DNI	AGP 4X, 0.8V signaling PLL CLK, IDSEL = AD17
						AGP8X_DET = 1 (either GC or MB not 8x capable)
DNI	10K	DNI	10K	DNI	10K	AGP 4X, PLL CLK, IDSEL = AD16
DNI	10K	DNI	10K	10K	DNI	AGP 4X, PLL CLK, IDSEL = AD17
DNI	10K	10K	DNI	DNI	10K	AGP 1X/2X, PLL CLK, IDSEL = AD16
DNI	10K	10K	DNI	10K	DNI	AGP 1X/2X, PLL CLK, IDSEL = AD17
10K	DNI	DNI	10K	DNI	10K	PCI 66MHz, PLL CLK
10K	DNI	DNI	10K	10K	DNI	PCI 33MHz, 3.3V, REF CLK
10K	DNI	10K	DNI	DNI	10K	AGP 1X, REF CLK, IDSEL = AD16
10K	DNI	10K	DNI	10K	DNI	AGP 1X, REF CLK, IDSEL = AD17

Rj1	Rk1	Rj2	Rk2	Rj3	Rk3	Rj4	Rk4	ROMIDCFG[3:0]
DNI	10K	DNI	10K	DNI	10K	DNI	10K	No ROM, CHG ID = 00
DNI	10K	DNI	10K	10K	DNI	DNI	10K	No ROM, CHG ID = 01
DNI	10K	10K	DNI	DNI	10K	DNI	10K	No ROM, CHG ID = 10
DNI	10K	10K	DNI	10K	DNI	DNI	10K	No ROM, CHG ID = 11
10K	DNI	DNI	10K	DNI	10K	DNI	10K	Parallel ROM on TVO (default)
10K	DNI	DNI	10K	DNI	10K	10K	DNI	Serial AT25F1024, ID's from ROM
10K	DNI	DNI	10K	10K	DNI	DNI	10K	Serial AT45DB011, ID's from ROM
10K	DNI	DNI	10K	10K	DNI	10K	DNI	Serial ST M25P10, ID's from ROM
10K	DNI	10K	DNI	DNI	10K	DNI	10K	Serial ST M25P05, ID's from ROM
10K	DNI	10K	DNI	DNI	10K	10K	DNI	Serial SST45LF010, ID's from ROM
10K	DNI	10K	DNI	10K	DNI	DNI	10K	Parallel ROM on DVO
10K	DNI	10K	DNI	10K	DNI	10K	DNI	Serial ISSI NX25F011B, ID's from ROM

{OrgName}		
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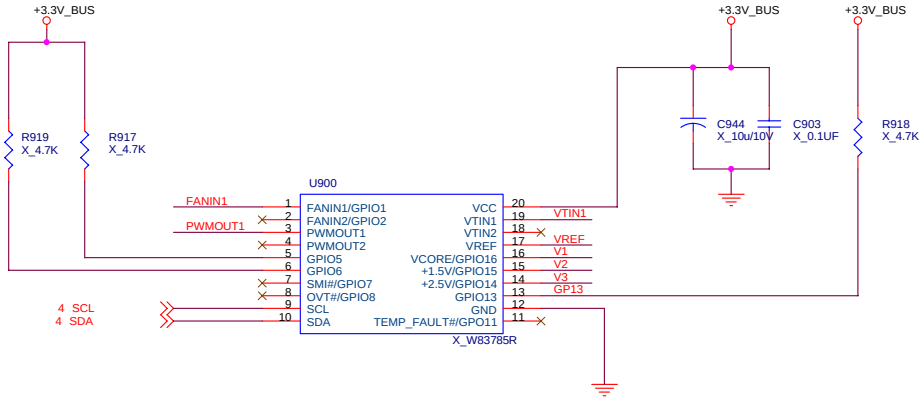
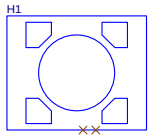
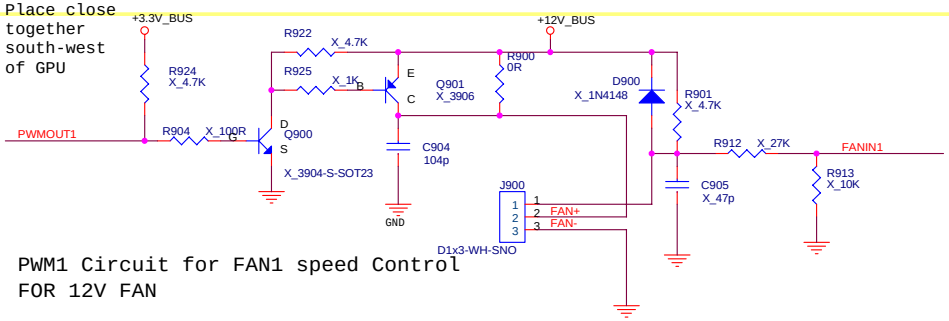
R566

SPEED CONTROLED FAN

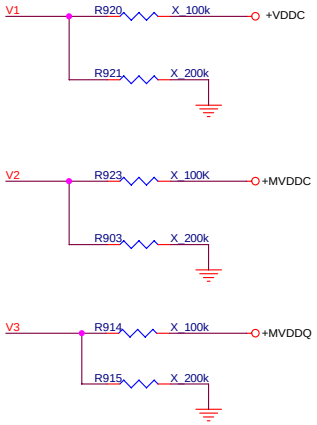




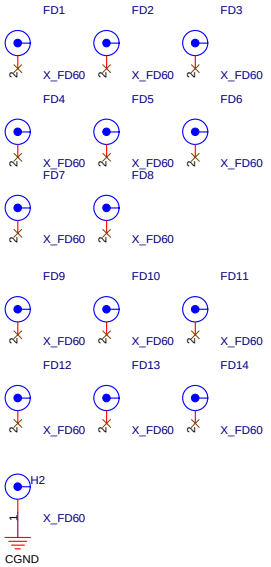
Place close together south-west of GPU

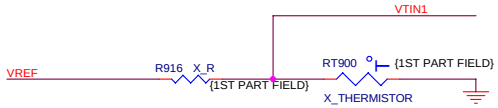


PWM1 Circuit for FAN1 speed Control
FOR 12V FAN



VOLTAGE SENSORING CIRCUIT





TEMPERATURE SENSORING CIRCUIT

{OrgName}		
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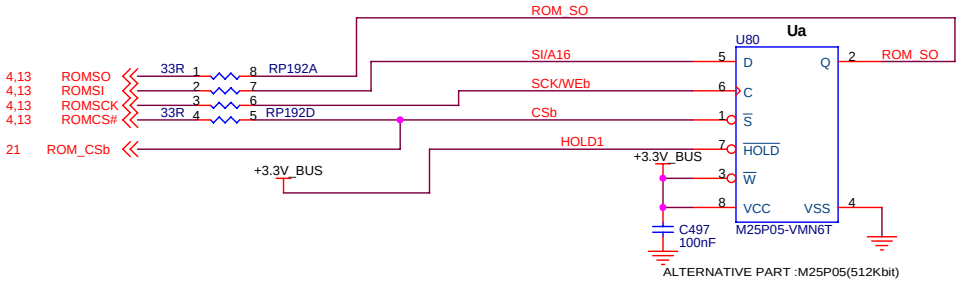
SERIAL EEPROM 512K/1M



{Variant Name}

{OrgName}

Size	Document Number	Rev
B	BIOS	0A

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Layout Guide line of THEATER

#1 : C385 and C386 have to be placed as close as possible to the pins of Rage THEATER

#2 : C397 should be placed close to J2

OPTIONAL +3.3V REGULATOR

+5V_BUS REG7 3.3V IN OUT ADJ CASE RVDD +3.3V_BUS

C374 100nF C373 100uF R376 X_0R

+3.3V_BUS

C566 100nF C375 100nF C376 100nF C377 100nF C378 22uF

U12

VDDR VDDR VDDR VDDR VDDC VDDC VDDC VDDR VDDC

SAD0 SAD1 SAD2 SAD3 SAD4 SAD5 SAD6 SAD7

DS_VIPCLK AS_HCTL SRDY_IRQB HAD0 HAD1

R195 33R CLK_VIPCLK 4

R196 33R VPHCTL 4

R197 33R VHAD0 4,13

R198 33R VHAD1 4

SDA SCL

R380 4.7K DNI +3.3V_BUS L0C1

ADO ADIO WS BITCLK

R381 10K

SPDIF MPPEN SPDIF R382 10K

RVDD

VAGCVDD VAGCVSS VAGCVSS VDACVDD VDACBVSS VDACJVSS

VIND0 VIND1 VIND2 VIND3 VIND4 VIND5 VIND6 VIND7 VINGATEA VINGATEB

CF CR VAGCCAP VIDEOGNDSENSE VCLAMPCAP

VADCDVDD VADCAVDD VADCDVSS VADCAVSS

COMP0 COMP1 COMP2 YF_COMP3 YR_COMP4

XTALIN XTALOUT TESTEN RESETB PLLVDD PLLVSS

BYTCLK SYNC Y_RED C_GREEN COMP_BLUE RSET

R148 200R CLK_RT 4

R374 383R R383 10K

CLKOUT0_GPIO0 CLKOUT1_GPIO1 CLKOUT2_GPIO2 GPIO3 GPIO4 GPIO5 GPIO6

R149 240R

PDATA0 PDATA1 PDATA2 PDATA3 PDATA4 PDATA5 PDATA6 PDATA7 PCLK

RP193A 33R VID0 VID1 VID2 VID3

RP194A 33R VID4 VID5 VID6 VID7

VID[7..0] VID[7..0] 4,13

R390 33R CLK_VIDCLK 4

VSSC VSSC VSSC VSSC VSSC VSSR VSSR VSSR VSSR VSSR VSSR VSSR VSSR VSSC VSSC

RAGE THEATER

PLACE AS CLOSE TO THE RAGE THEATRE AS POSSIBLE.

PLACE CLOSE TO RAGE THEATRE

RVDD R1097 10R B20 3.3uH C393 47uF C394 100nF

CR C889 2.2uF C924 68nF X7R C925 22nF

Comp/R C112 2.2uF YR C890 2.2uF

4 RT_XTALIN 4 RT_XTALOUT

2,3,21 AGP_RESET#

RVDD R1098 10R B34 3.3uH C399 47uF C400 100nF R393 3K3

PLACE CLOSE TO RAGE THEATRE

+3.3V_BUS BAV99 D79

YR L19 3.3uH YRIN R1063 75.0R 1% C885 330pF C886 330pF GND

+3.3V_BUS BAV99 D80

CR L11 3.3uH CRIN R1064 75.0R 1% C887 330pF C888 330pF GND

+3.3V_BUS BAV99 D78

Comp/R 3.3uH L28 CompR R1065 75.0R 1% C892 330pF C891 330pF GND

PLACE CLOSE TO CONNECTOR

+3.3V_BUS BAV99 D81

Y_DAC2 L4 1.8uH C383 82pF C384 33pF GND_TVVSSN CGND Luma_F Chroma_F Comp_F

+3.3V_BUS BAV99 D82

C_DAC2 L13 1.8uH C387 82pF C388 33pF R508 0R GND_TVVSSN CGND

COMP_DAC2 L15 1.8uH COMP1 C391 82pF C392 33pF GND_TVVSSN CGND

BAV99 D83 +3.3V_BUS

TV-OUT

4 R/C_DAC2

4 G/Y_DAC2

4 B/COMP_DAC2

+5V_BUS C735 100nF

Uv1

4,20 TVO0 19 B_DAC2 19 G_DAC2

U96 SEL 1A0 1A1 1B0 1B1 1C0 1C1 E VCC YA YB YC YD 1D1 1D0 GND PI5V330

R_DAC2 C_DAC2 R_DAC2 19

Layout Guide line of THEATER

#1 : C27 and C28 have to be placed as close as possible to the respective pins of Rage THEATER

#2 : VINGND should be seperated from Digital or Chassis Ground and have no loops

#3 : VINGND should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

Chroma_F R520 0R Comp_F R521 0R CRIN R522 X_0R

R519 0R Luma_F CVBSYIN R513 YRIN X_0R R514 CompR X_0R

P500 9-pin:4-pin:9-pin:3-pin CON_S_VIDEO_9P_STD VIVO:TV_OUT:VIDCAP:STEREO_OUT

CGND CGND

CRIN YRIN

P501 X_9-pin:4-pin:9-pin:3-pin CON_S_VIDEO_9P_STD VIVO:TV_OUT:VIDCAP:STEREO_OUT

CGND R523 X_0R CompR

AV_IN CompR

X_JACK+RCA-D3-SB-YL CGND CGND

JA CD-D1x4-BK-SBTJ

L29 3.3uH CRIN L30 3.3uH CompR L31 3.3uH YRIN

C109 33pF C110 33pF C111 33pF

AV_OUT

JACK+RCA-D3-SB-YL CGND CGND CGND

C395 10pF Comp_F

{Variant Name}

{OrgName}

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	CustomTHEATER & TV-OUT	0A

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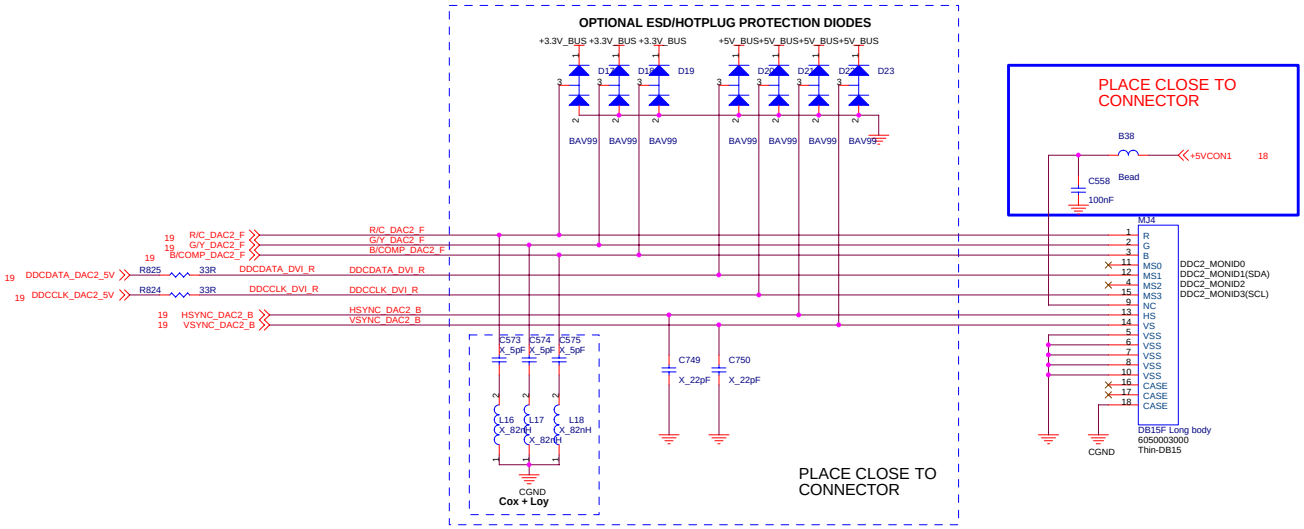
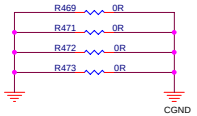
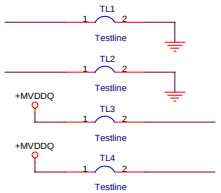




Impendence Test Line



{OrgName}		
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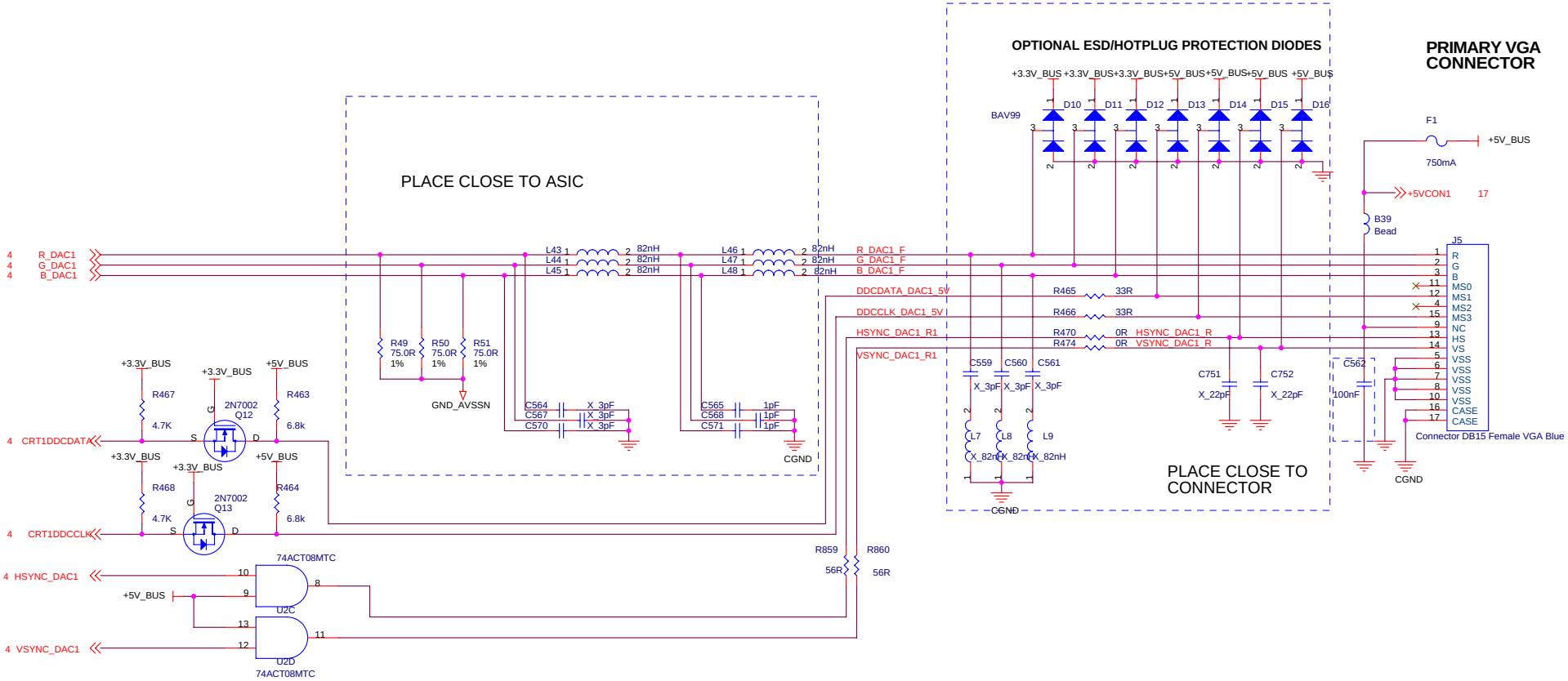
PRIMARY CRT INTERFACE



{OrgName}		
Size B	Document Number CRT1	Rev 0A
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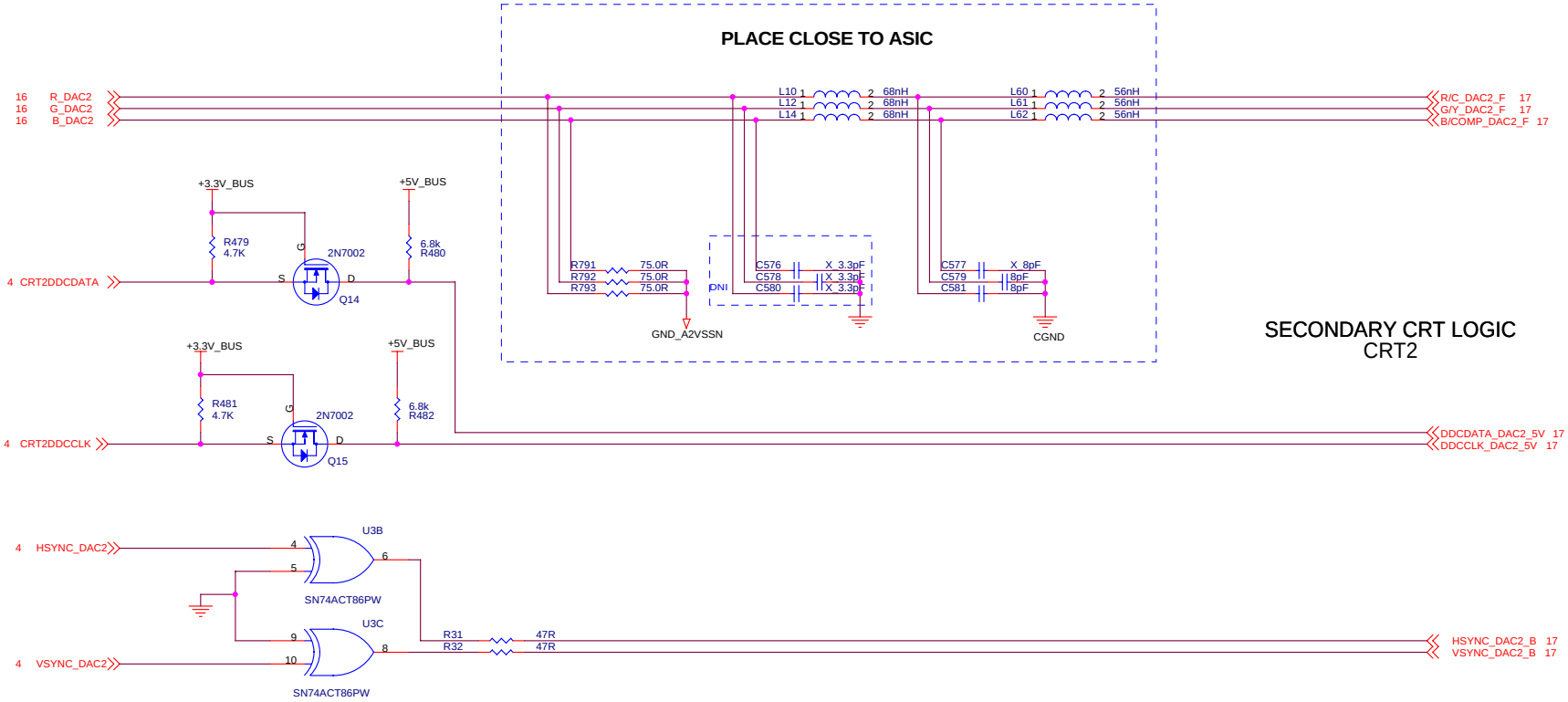

{OrgName}		
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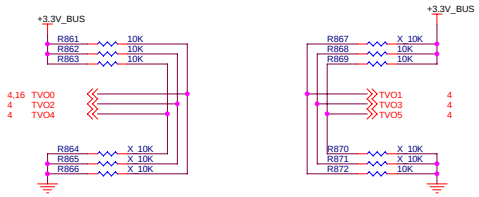
Daughter Card Straps



ADDED

TVO0 TVO3

00 DAC2 OFF

01 DAC2 ON AS TVO
10 DAC2 ON AS CRT
11 DAC2 ON FOR BOTH

TVO2

0 FOR YPrPb

1 FOR SVHS/CVBS

TVO1

0 FOR PAL

1 FOR NTSC

TVO 5

0 FOR NO VIDEO CAPATURE

1 FOR RAGE THEATER 1 OR 2

TVO4

0 FOR NO

1 FOR YES

{OrgName}		
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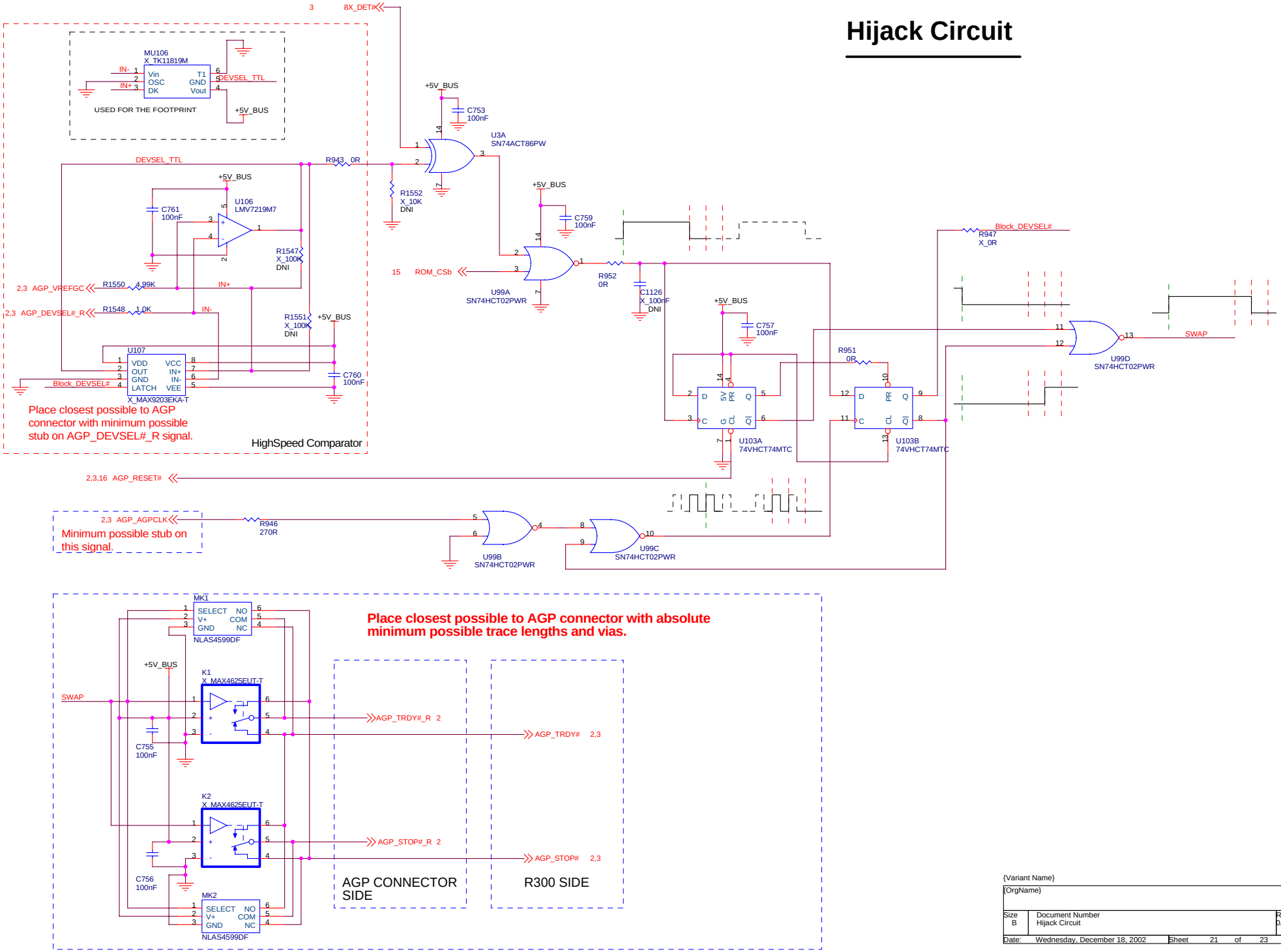
Hijack Circuit



{Variant Name}

{OrgName}

Size	Document Number	Rev
B	Hijack Circuit	0A

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