PCI-EXPRESS EDGE CONNECTOR

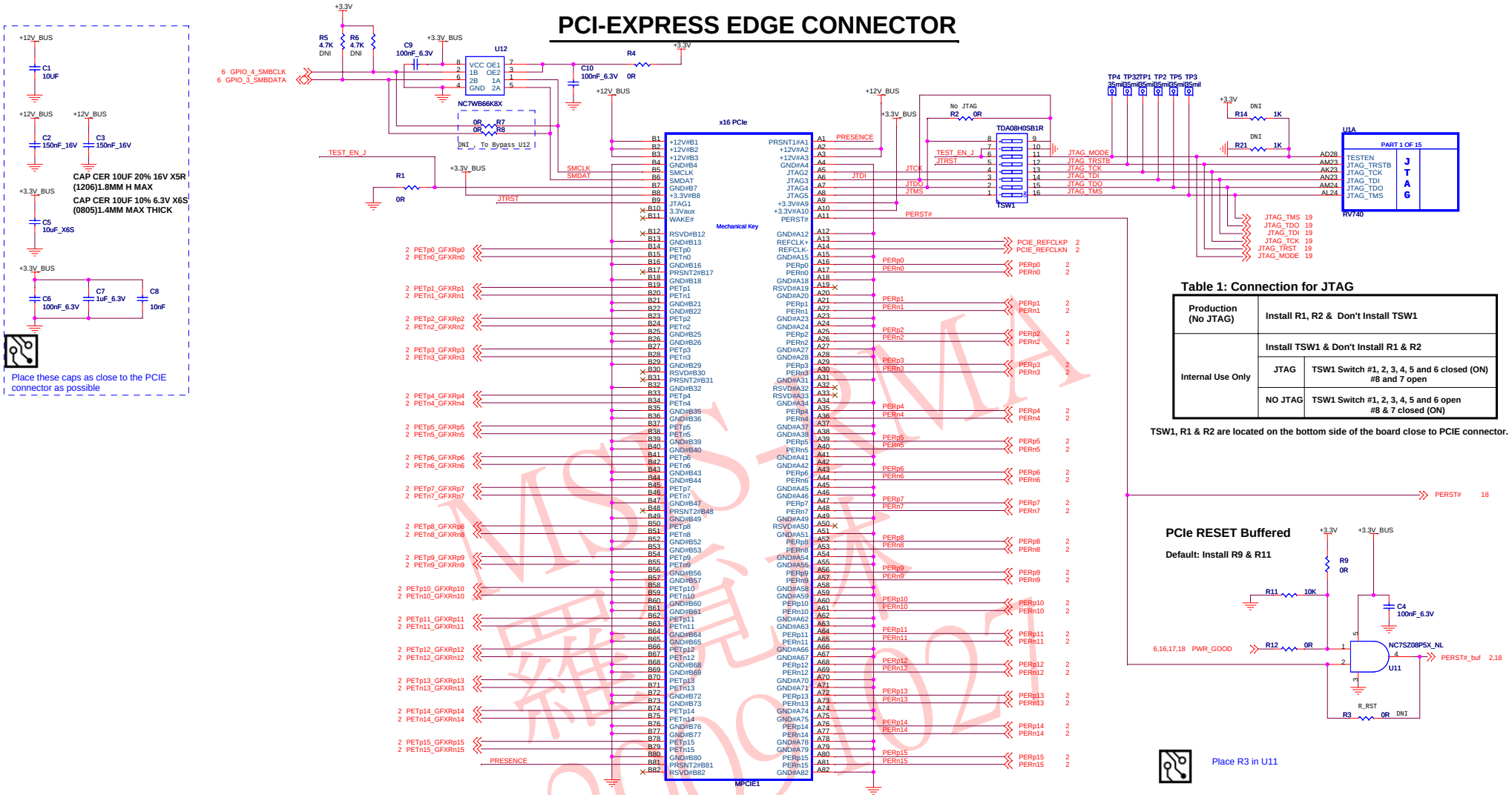

Table 1: Connection for JTAG

Production (No JTAG)	Install R1, R2 & Don't Install TSW1	
Internal Use Only	Install TSW1 & Don't Install R1 & R2	
	JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open
	NO JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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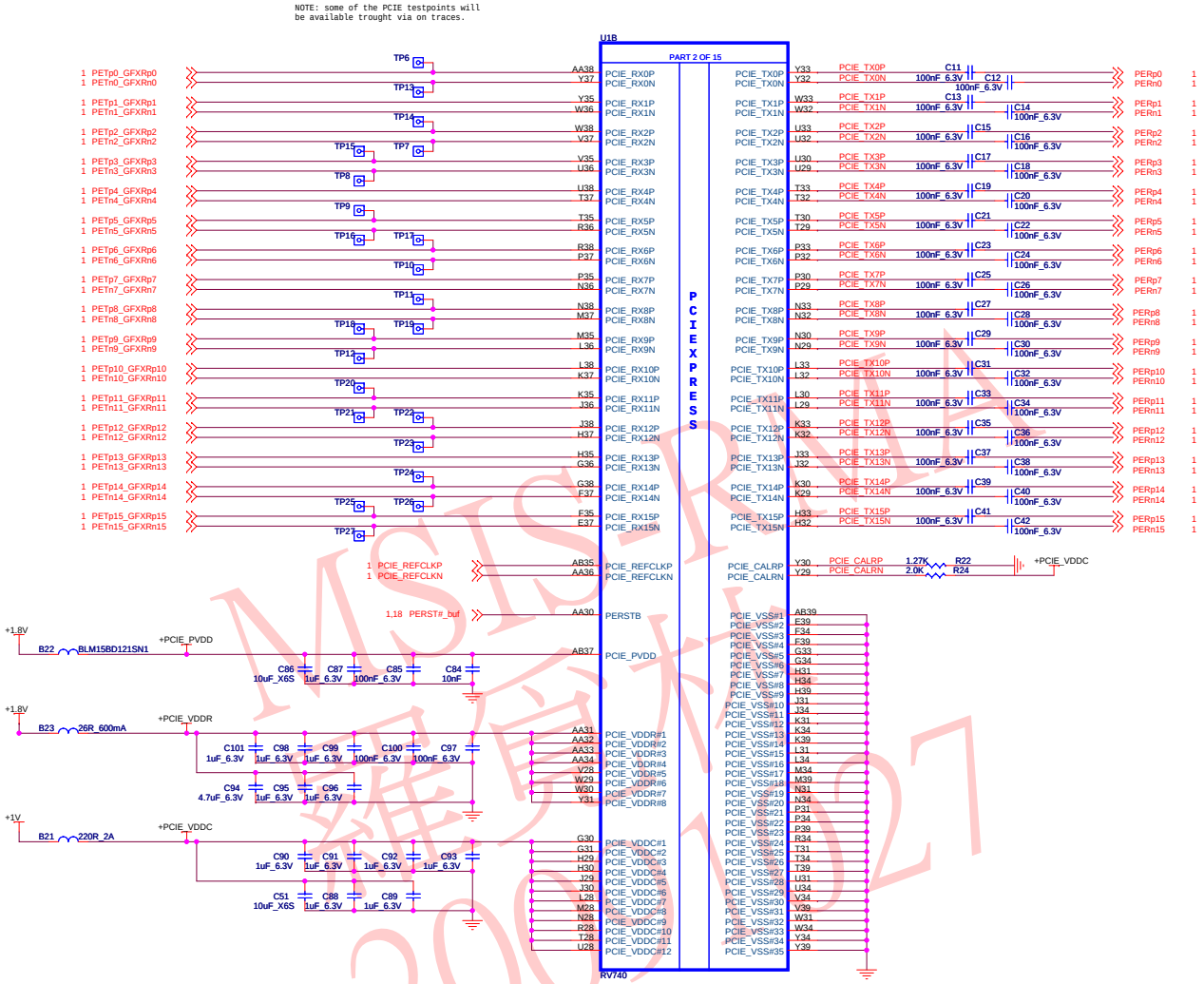
(2) RV740 PCIE Interface



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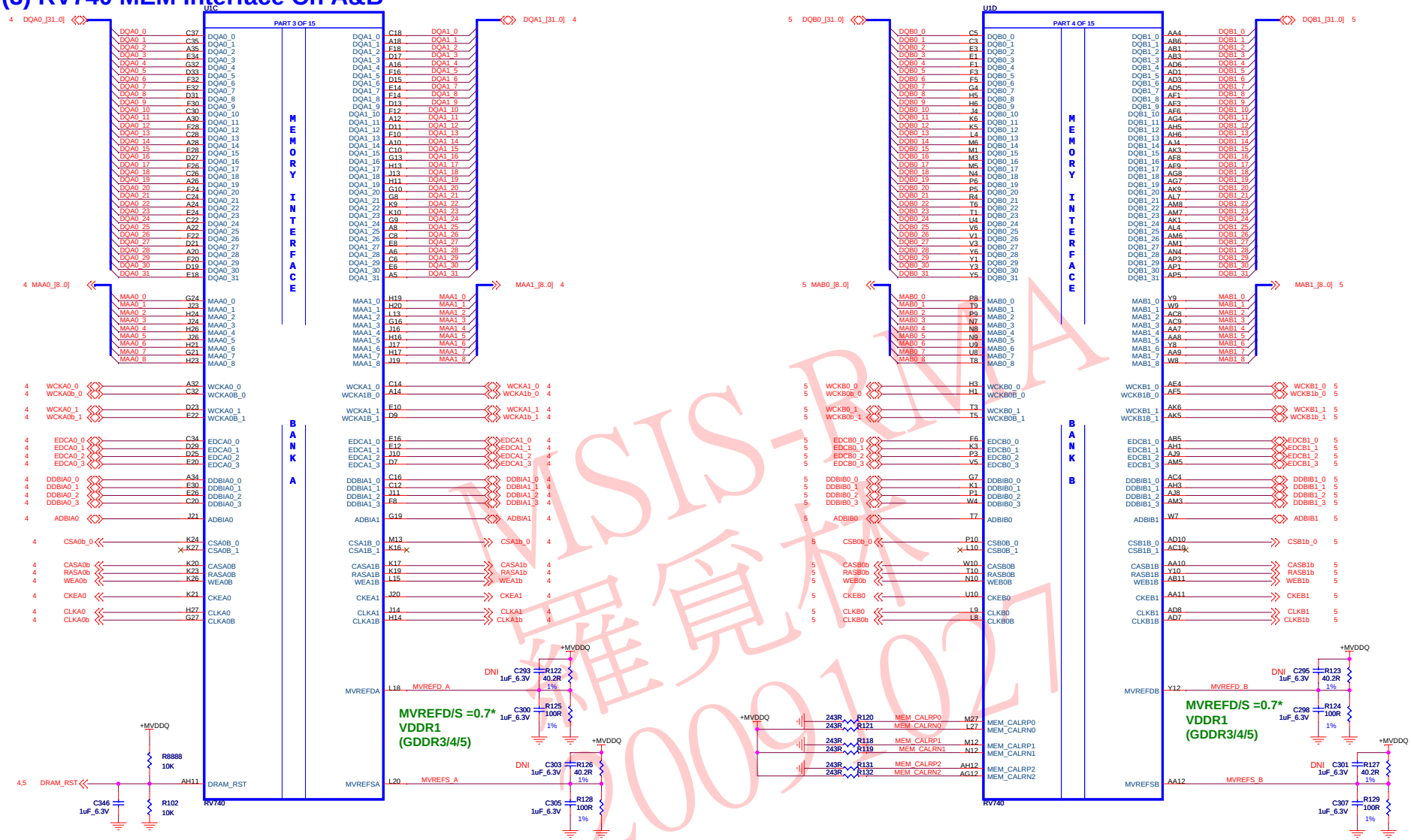
(3) RV740 MEM Interface Ch A&B



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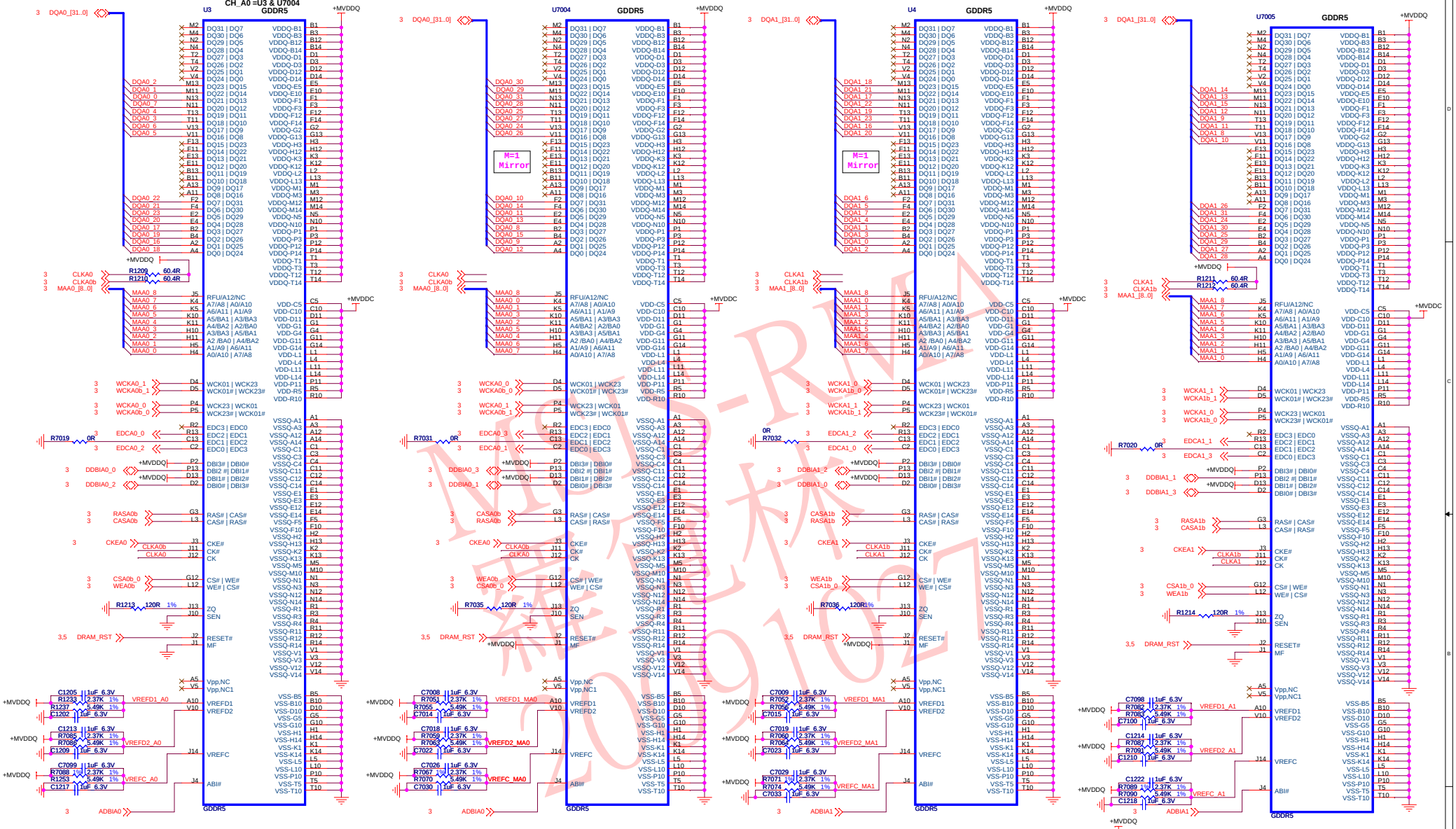
(4) GDDR5 x16 MEM Channel A



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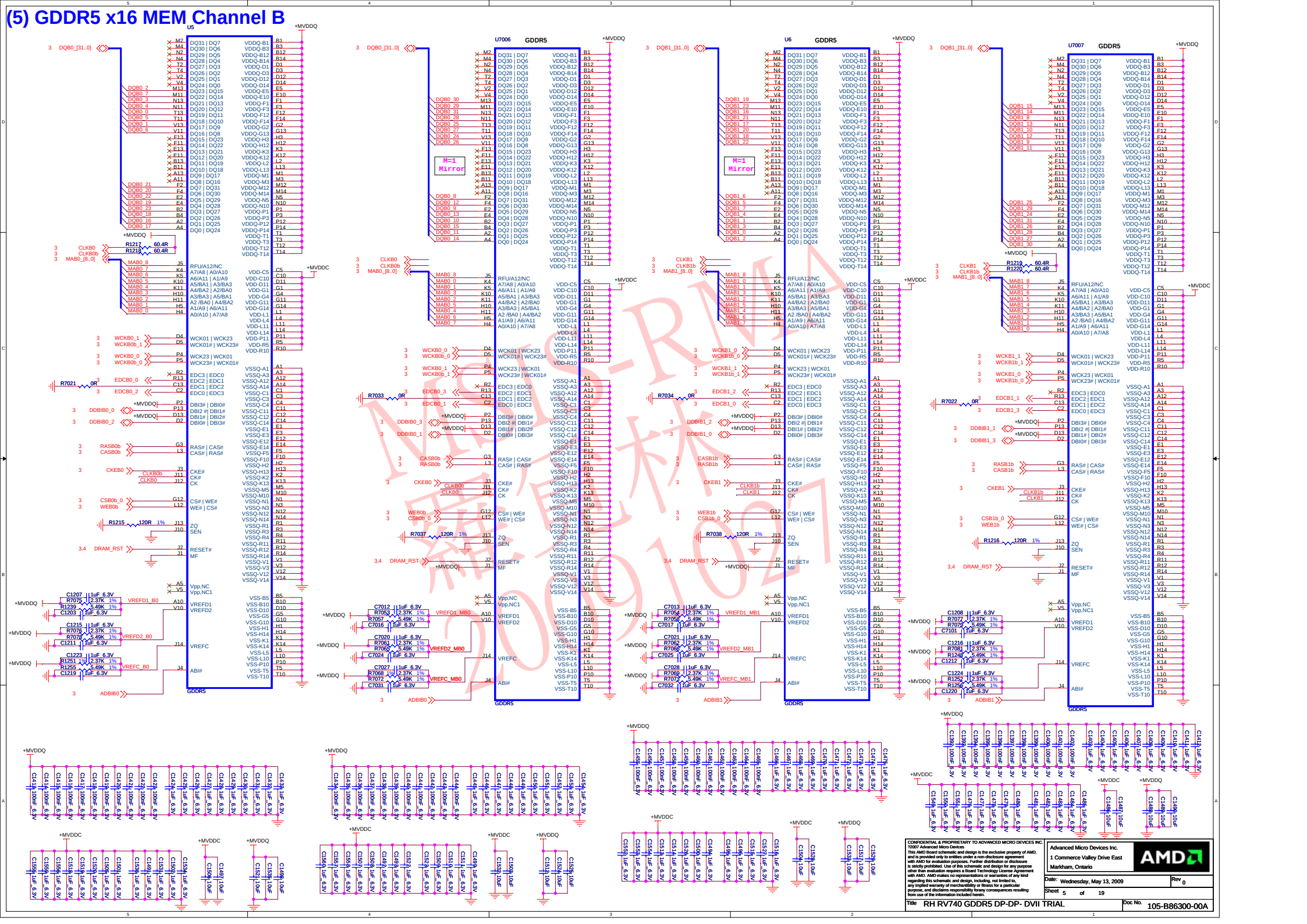
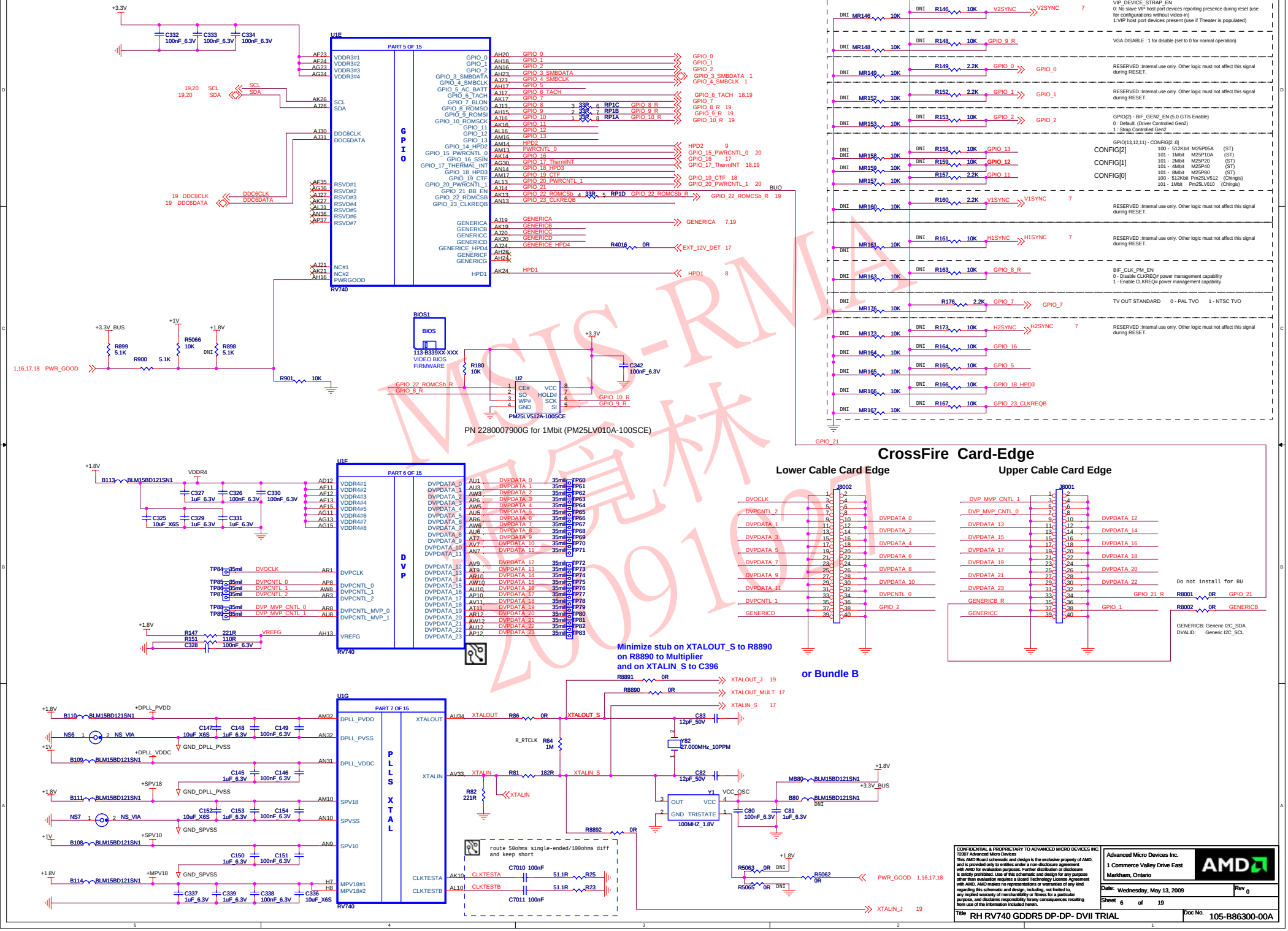
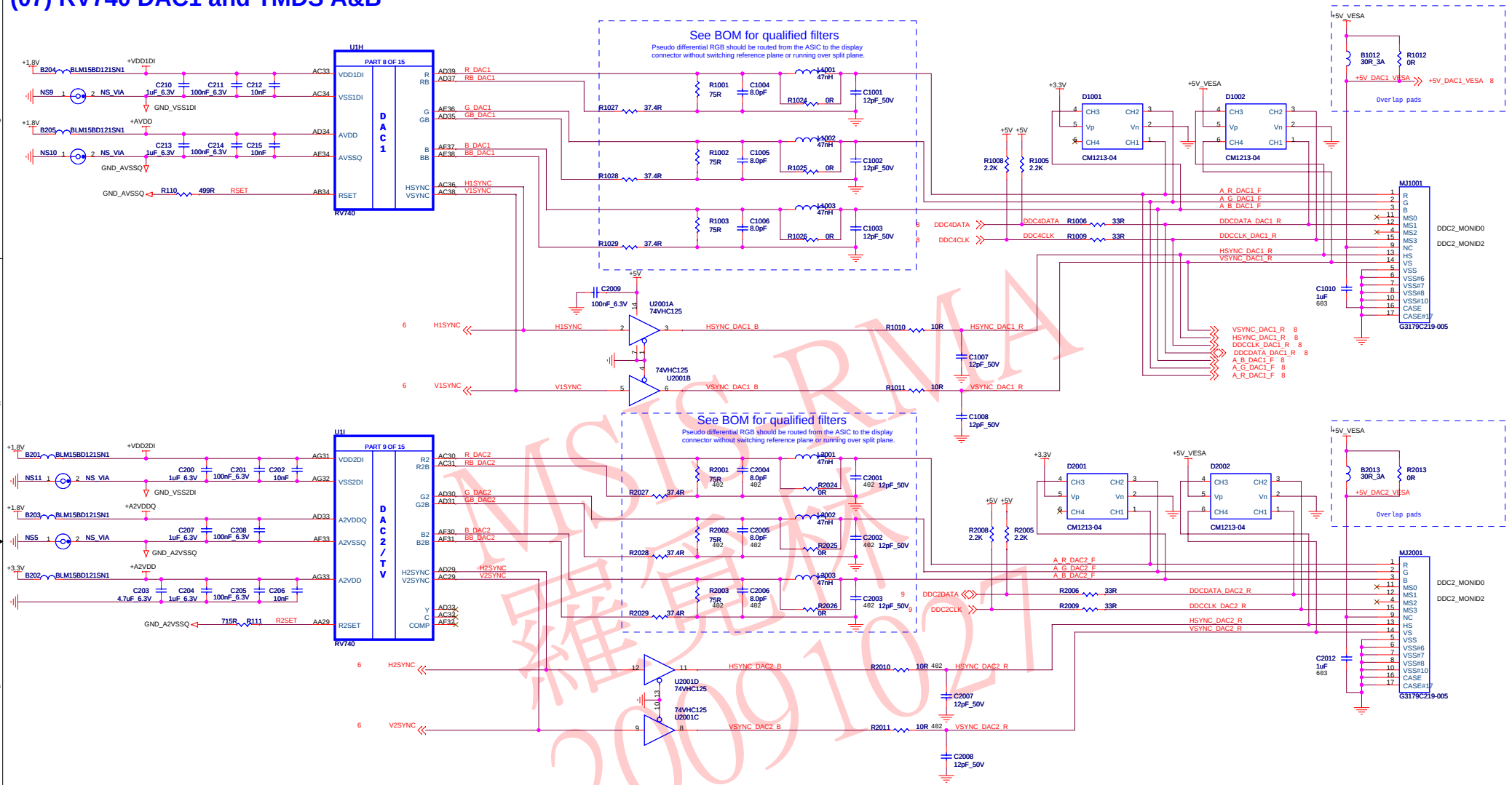
(5) GDDR5 x16 MEM Channel B



(06) RV740 GPIOs Strap CF XTAL



(07) RV740 DAC1 and TMDS A&B



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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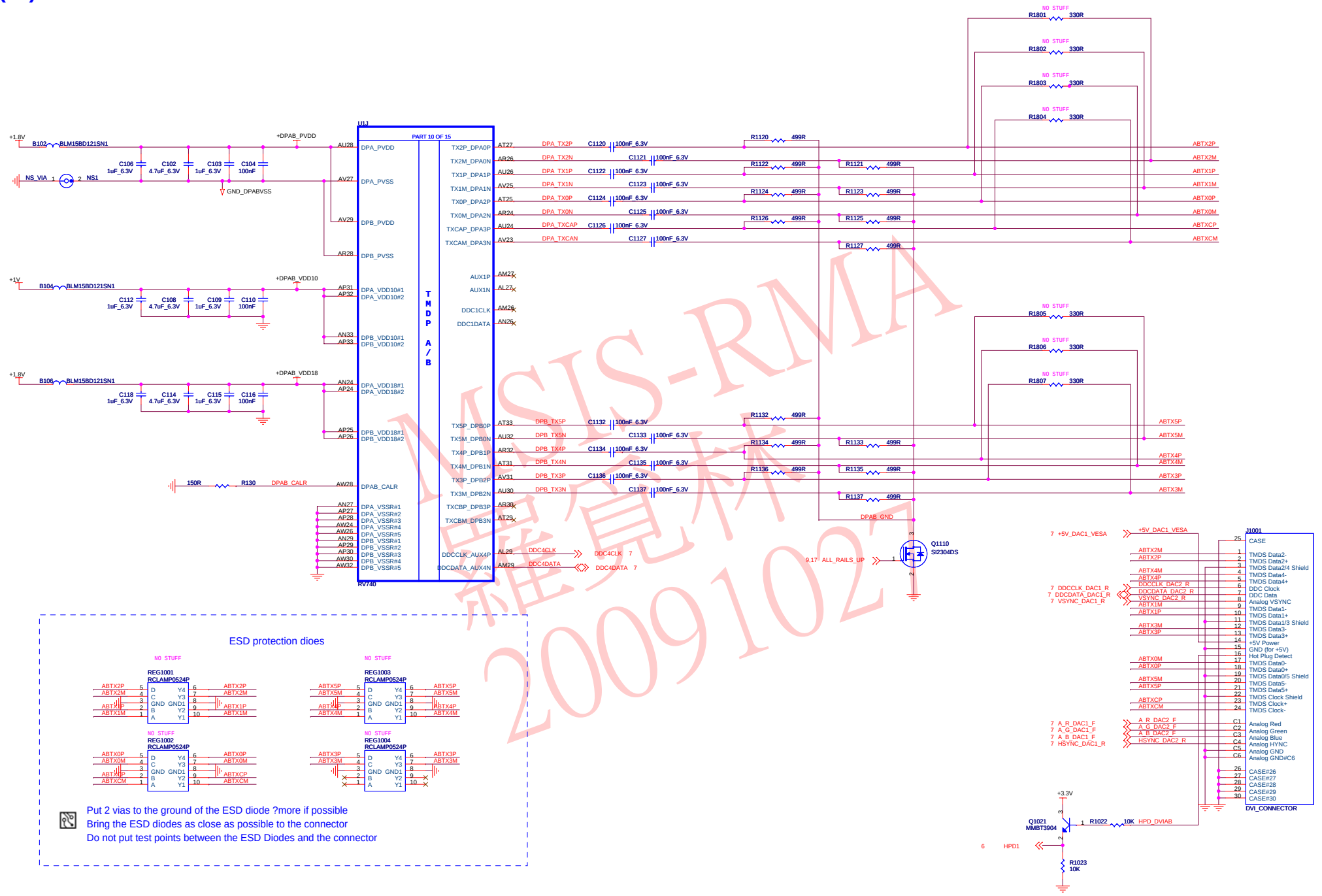
(08) RV740 TMDS A&B



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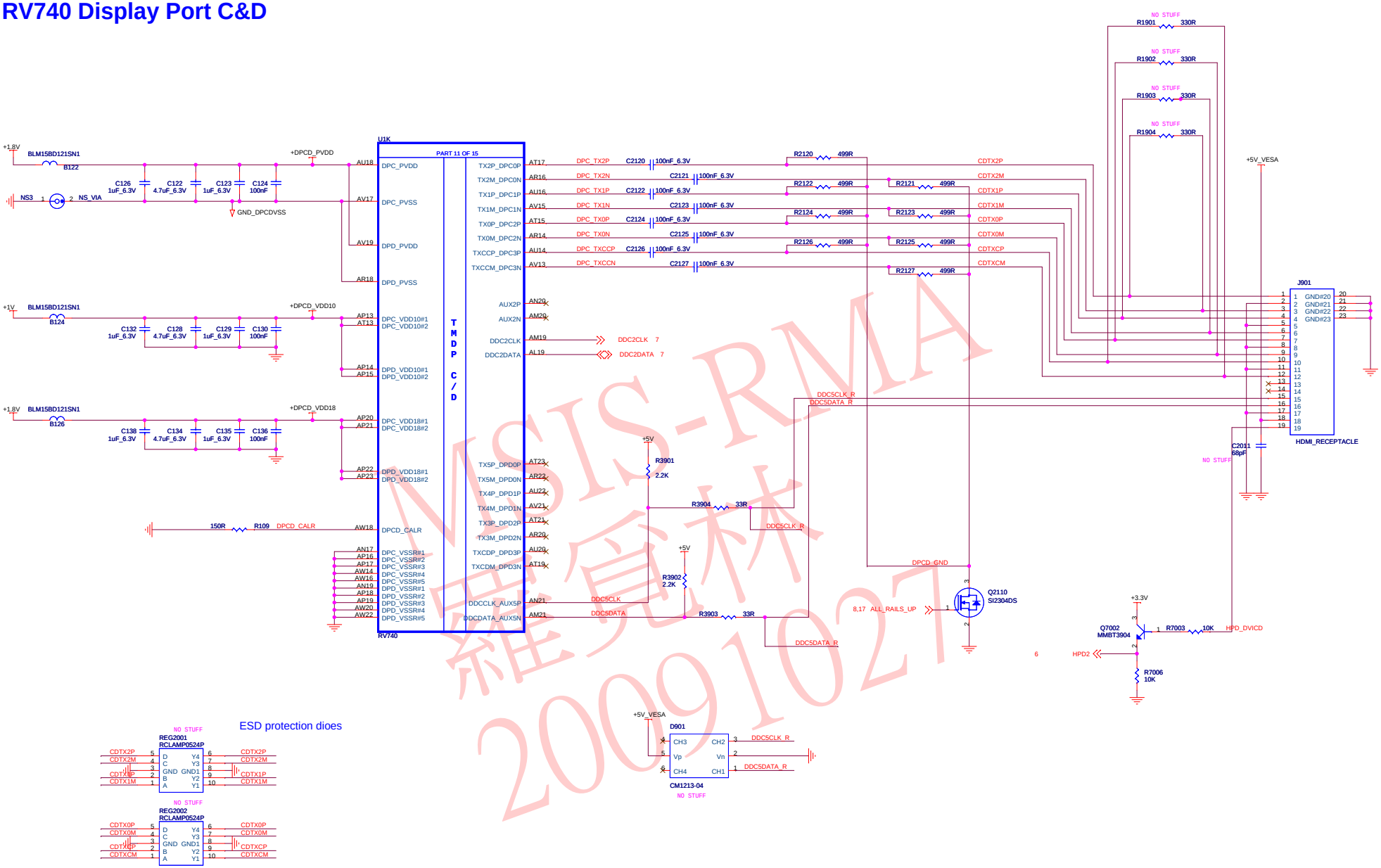
(09) RV740 Display Port C&D



Put 2 vias to the ground of the ESD diode ?more if possible
Bring the ESD diodes as close as possible to the connector
Do not put test points between the ESD Diodes and the connector

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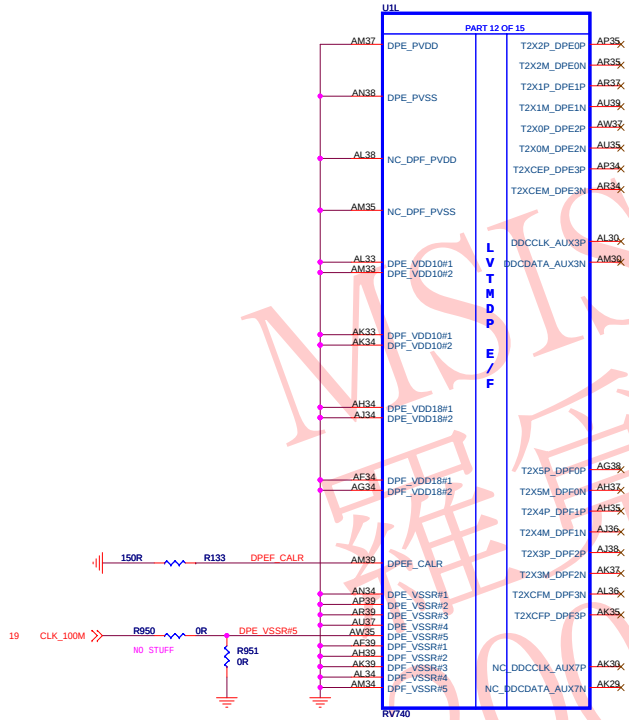
(10) No Connect E&F



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(11) RV740 Power & GND

Swap With C1225, C1226, C1227, C1228, C1229, C1230, C1231, C1232, C1233, C1272, C1273, C1274 refdes locations

+MVDDQ

U1M

PART 13 OF 15

POWER

RV740

Overlap cap pair foorprints (0805 with 0603)

Overlap footprints

1206 footprint

+VDDC

+VDDCI

+VDD_CT

+1.8V

FB_VDDCI

FB_VDDC

FB_GND

NC_VDDRHA

NC_VSSRHA

NC_VDDRHB

NC_VSSRHB

U1N

PART 14 OF 15

GND

RV740

CLK_27M

R952 0R

R953 0R

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(12) VDDC

PHASE 1

PHASE 2

PHASE 3

NOTE: Use ML623 with Fansink P/N 7120174000G

Input MLCC

Input Bulk CAPs

Output Bulk CAPs

Output MLCC

RC snubber values shown are for reference only, tuning is required

Table 1 MODE Pin Definition Table

VPM Mode	Mode Pin Status	Mode Pin Voltage (V)	Phase Operation		
			Phase 1	Phase 2	Phase 3
3-Phase Mode	0	0	Enabled	Enabled	Enabled
2-Phase Mode	1	3.3	Enabled	Enabled	Disabled
1-Phase Mode	Floating	~ 1.7	Enabled	Disabled	Disabled

Circuitry that have to be placed close to the device:
- current sense,
- compensation network,
- thermal compensation network (Droop, OCP, etc)

+5VCC is generated internally and this is an output with 20mA minimum current capability

Connect AGND to PGND at one point close to U8500

Connect AGND to PGND

Type II compensation

Type III compensation

Differential FB Traces from GPU core

VSEN Monitoring

Set PWRON Default "DVT" (See Power Management Page)

See Power Management 2 page for DPM

VR_HOT/EN Circuit

UP

Table 1 VRHOT/EN Table

EN	Q1	Q2	VR_HOT/EN	IC	VR_HOT	GPIO
1	on	off	0	Disabled	/	1
0	off	on	5V	Enabled	No Warning	0
0	off	off	0.45V	Enabled	Warming	1

SM

Table 1 VRHOT/EN Table

EN	Q1	Q3	Q2	VR_HOT/EN	IC	VR_HOT	GPIO
1	on	on	on	0	Disabled	/	0
0	off	on	on	1.5V	Enabled	No Warning	0
0	off	off	off	3.3V	Enabled	Warning	1

CASE1, CASE3 Special Case Power Up Detection

NOTE: This is for the IC that uses VCC2 for EXT_12V Detection.

Table 5 MODE Pin & Phase3 Strip Detection Table

App	Condition	Mode Pin	VPM Mode	Phase 3	IC Behavior
CASE 1	PwrUp without EXT_12V Cable	1	2-Ph Mode	Open	IC enabled without detecting EXT_12V (VCC2) voltage.
CASE 3	PwrUp with EXT_12V Cable	1	2-Ph Mode	Pull Down	Detect EXT_12V (VCC2) voltage before IC enable.

RT (For HW ver IC)

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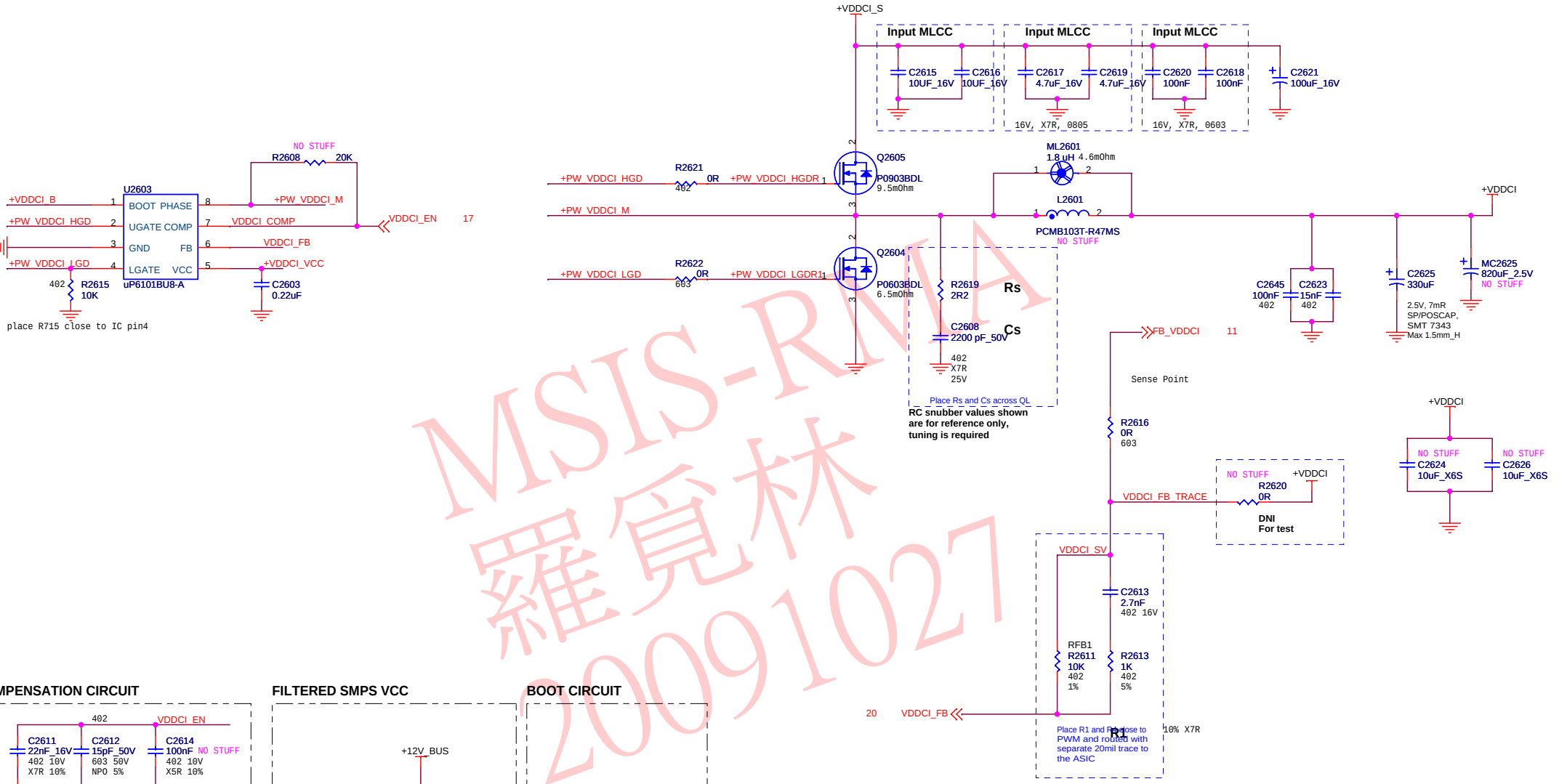
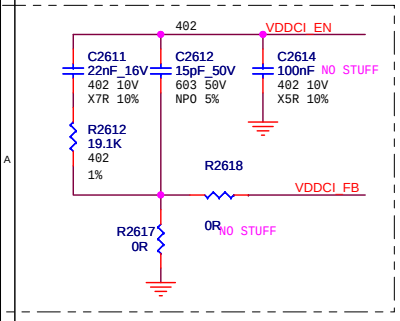
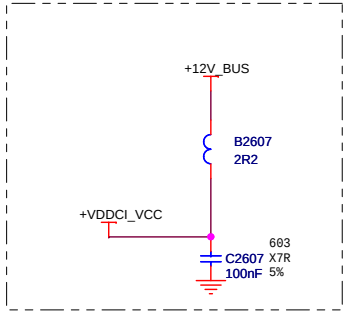
(13) VDDCI



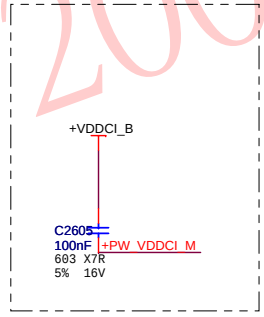
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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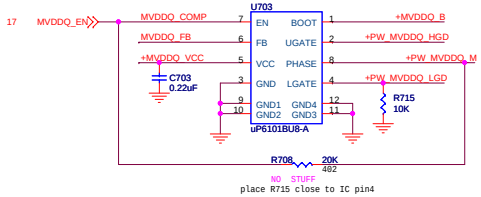
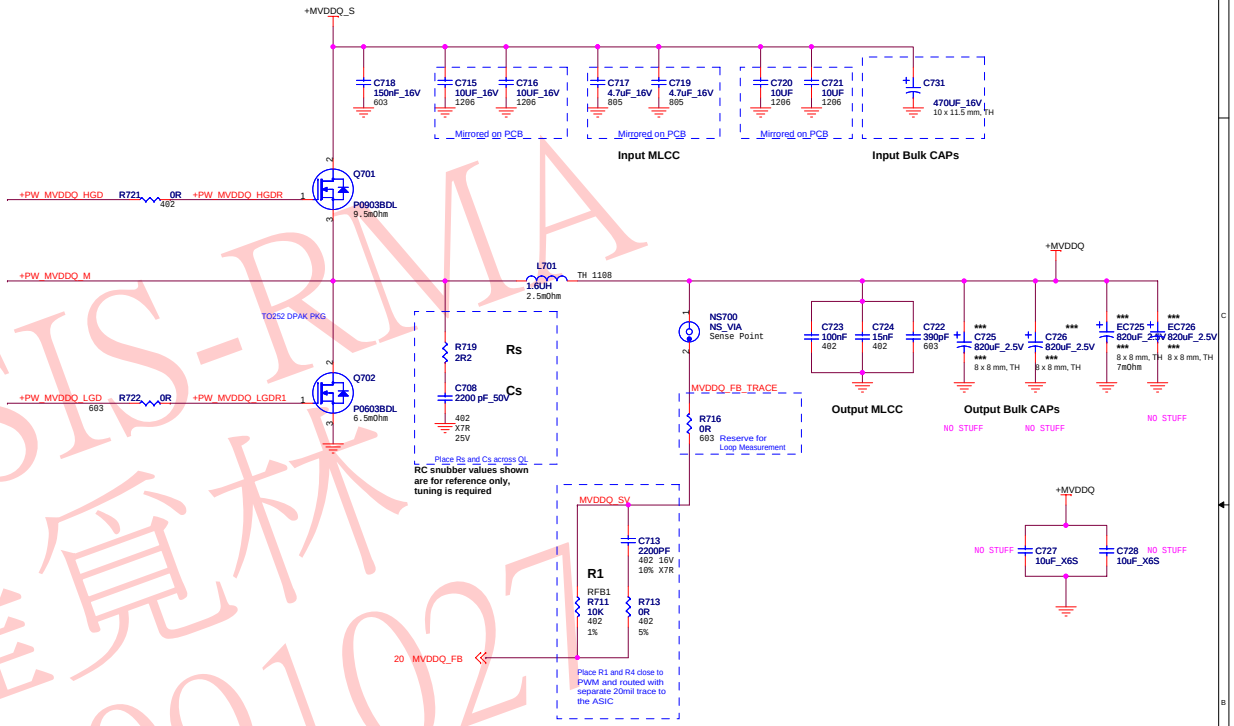
(14) MVDDQ

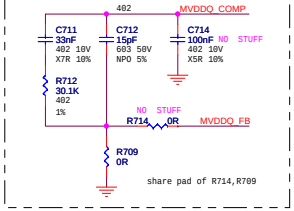


Layout guideline

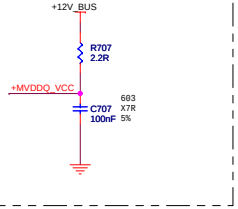
1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



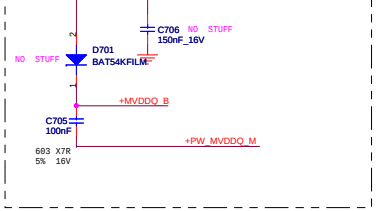
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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(15) MVDDC

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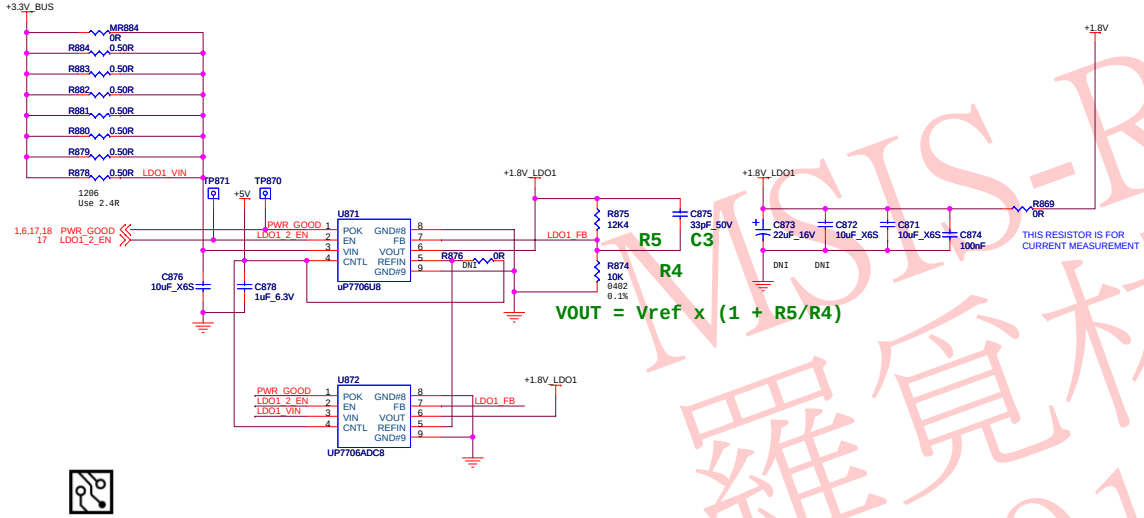
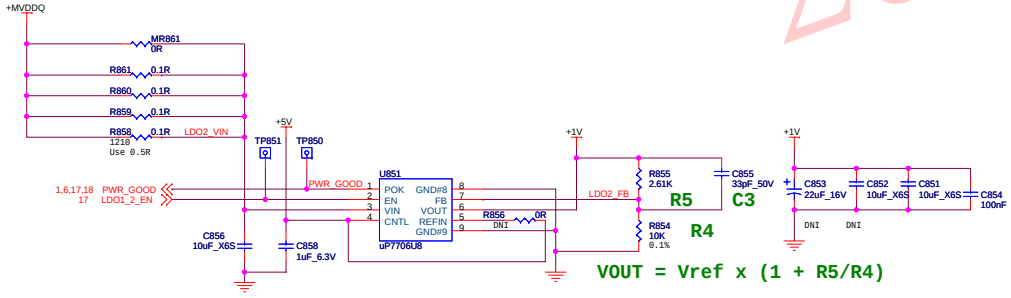
(14) Linear Regulators

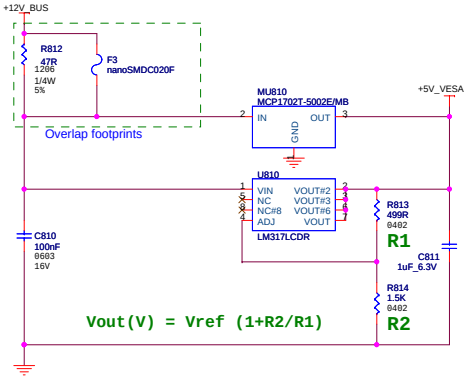
Regulators for +5V, +5V_VESA and +5V_VESA2

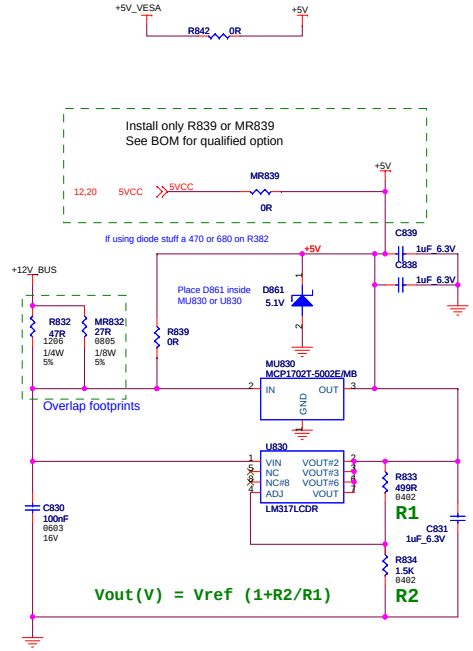
LDO #1: Vin = 3.0V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 1.0A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #2: Vin = +1.35V to 2.0VMAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling







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(15) Power Management

VDDC_EN is open collector and it is deactivated (pulled down to ground) when: EN_INTb =1 OR EN_Tb =1 OR (EN_EXTb =1 AND SENSE_GND_PIN=0)

12V_EXT Connector

J1601 6P_HDER
+12V_1, +12V_2, +12V_3, GND_1, GND_2, Sense
+12V_EXT
C1623 47pF_50V
C1601 220pF_50V
C1602 220pF_50V
C1603 10uF
MC1603 10UF
Overlap MC1603 and C1603
C1608 47pF_50V
SENSE_GND_PIN
SENSE_GND_PIN 20

Ext Connector Detection

+3.3V_BUS, +3.3V
R1615 10K
R1610 2.2K
R1612 10K
Q1612 MMBT3904
R1630 100K
Q1605 MMBT3904
EXT_12V_DET 6

AUX plug Enforcment option (BUO not for production)

12V AUX Power up Fault Support

+12V_EXT, +3.3V_BUS
R1606 0R DNI
R1601 10K
R1609 1K
R1633 5.1K
R1634 5.1K
R1647 1K
R1650 5.1K
R1648 1K
R1649 5.1K
R1621 1K
Q1602 MMBT3904
Q1628 MMBT3904
Q1627 MMBT3904
C1624 47pF_50V
MMBT3904 Q1601
VDDC_EN 12,18
Place close to its CTLR

Power up Sequencing

VDDC Enable Circuit

+12V_BUS, +3.3V_BUS
R4682 5.1K
R4687 10K
R4689
R4688 5.1K 1K
2.2K R4680
R4697 1K
R4681 1K
Q677 MMBT3904
Q678 MMBT3904
R4683 5.1K
EN1_N
C849 1uF_6.3V
Q679 MMBT3904
VDDC_EN
VDDC_EN 12,18
Place close to its CTLR

3.3V discharge Circuit

+3.3V, +3.3V_BUS
R852 300R
R857 10K
Q846 MMBT3904
Q849 MMBT3904
R853
R851 10K
1,6,16,18 PWR_GOOD

3.3V Enable Circuit

Share pads
R847 10K
C844 1uF_6.3V
MR847 0R
+12V_BUS, +3.3V_BUS, +3.3V
R848 100K
R849 10K
R1263 0R
Q845 SI2304DS
C842 10uF_X6S
Q843 MMBT3904
Q844 MMBT3904
C843 100NF 402 X5R 16V
ALL_RAILS_UP 8,9

VDDCI, LDO 1.8V, LDO 1V, MVDDQ, MVDDC Enable Circuit

+3.3V_BUS, +VDDC, +12V_BUS, +3.3V_BUS
10K R693
12 VDDC_PWR_GOOD
MR841 1K
R841 1K
Share pads
C841 1uF_6.3V
R843 5.1K 5%
Q840 MMBT3904
5.1K R845
R844 5.1K 5%
C845 1uF_6.3V
Q841 MMBT3904
LDO1_2_EN 16
MVDDQ_EN 14
DNI R846 5.1K 5%
C846 1uF_6.3V
Q842 MMBT3904
Place close to its CTLR
VDDCI_EN 13
DNI R850 5.1K 5%
C848 1uF_6.3V
Q847 MMBT3904
Place close to its CTLR

DNI
Test cct for low VDDC voltage.
+MVDDQ
R890 5.1K
1,6,16,18 PWR_GOOD
R893 5.1K
R891 5.1K
Q853 MMBT3904

SS Solutions

Clock range selection and device

FR1	FR0	Input	Output	AKM P/N
H	L	64-128MHz	64-128MHz	AK8126A
H	H	27MHz	100MHz	AK8126B

Spread Mode

C/D/OFF	Input
L	DOWNSPREAD
H-L	NO Modulation
H	CENTER SPREAD

Spread Spectrum Modulation Charact.

S1	S0	AKM 8126B	AKM 8126A
L	H	-.375%	
L	L	-0.625%	
H	L	-1.25%	
H	H	-1.875%	

FR1, FR0
R4200 0R, R4201 0R, MR4200 0R, MR4201 0R
+3.3V
R4202 10K
C/D/OFF
R4203 10K
R4204 10K, R4205 10K, MR4204 10K, MR4205 10K
S1, S0
Share pad

6 XTALIN_S
C396 10nF_25V
R4208 100K +3.3V
XTALOUT_MULT
R4209 100K
6 XTALOUT_MULT
C8889 100nF_6.3V DNI
U13 AK8126
XIN, XOUOT, S1, S0, FR1, FR0, C/D/OFF, CKOUT, VDD, VSS
R4210 0R GPIO_16
GPIO_16 6
BLM15BD121SN1
VCC_SS
B4003 +3.3V
C397 1uF_6.3V
C395 100nF_6.3V

Minimize stub length on XTALIN_S and XTALOUT_MULT
Minimize stub length on GPIO_16

+3.3V
R4206 0R
X2
VCC_SS
MR4206 0R
0R R4207 GPIO_16
SIT9001AC-13-33D6-100.000

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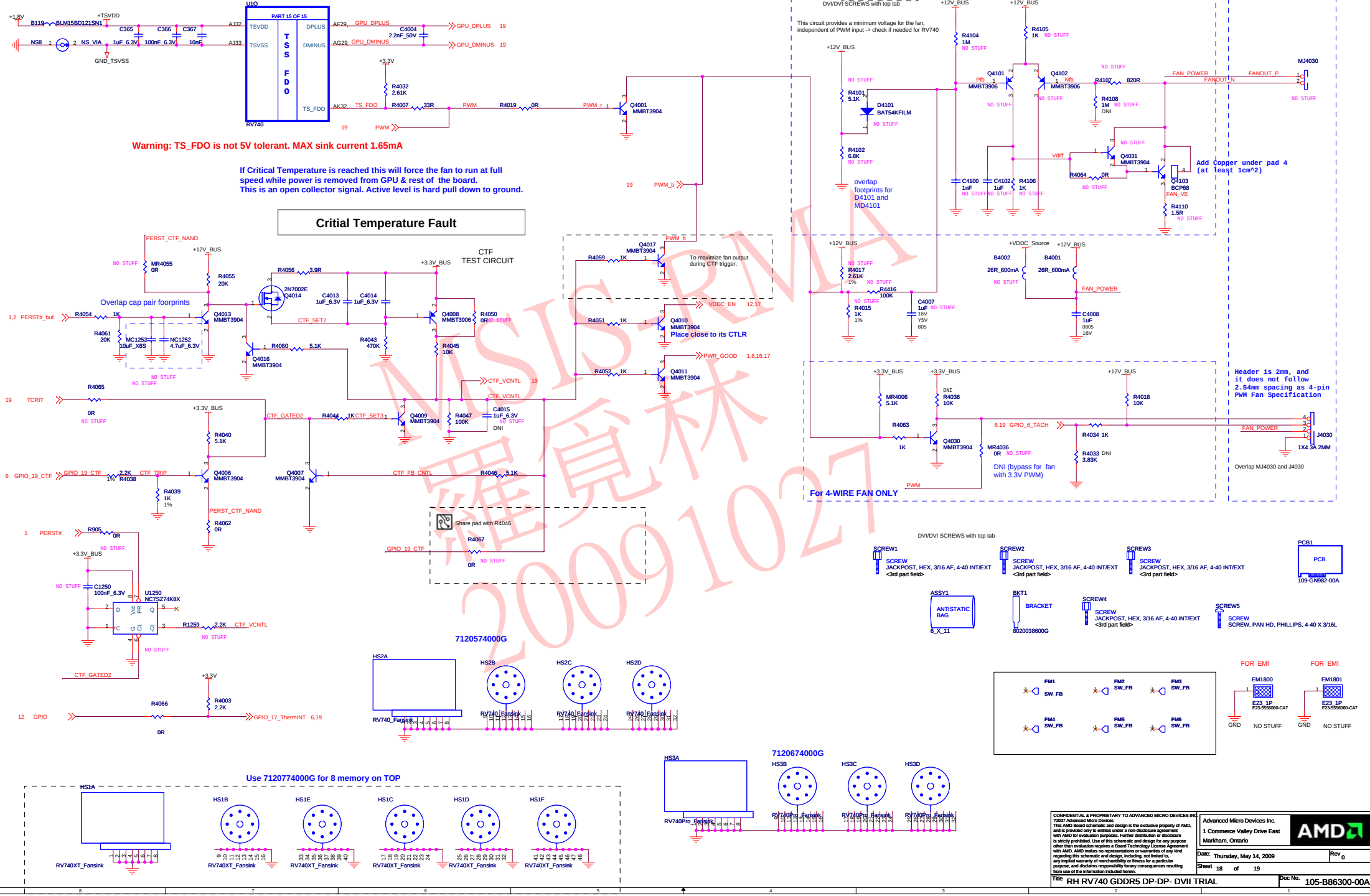
(16) Mechanical and Thermal Management



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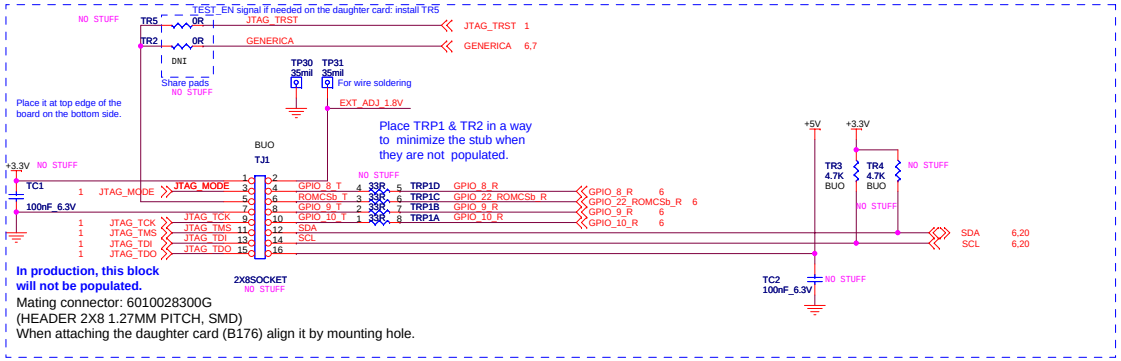
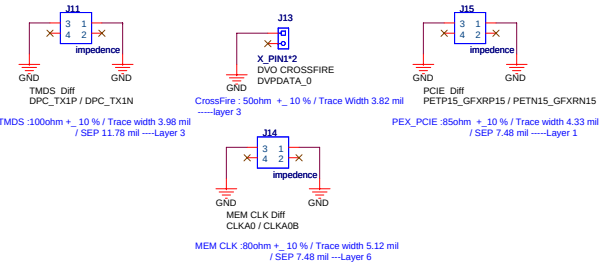
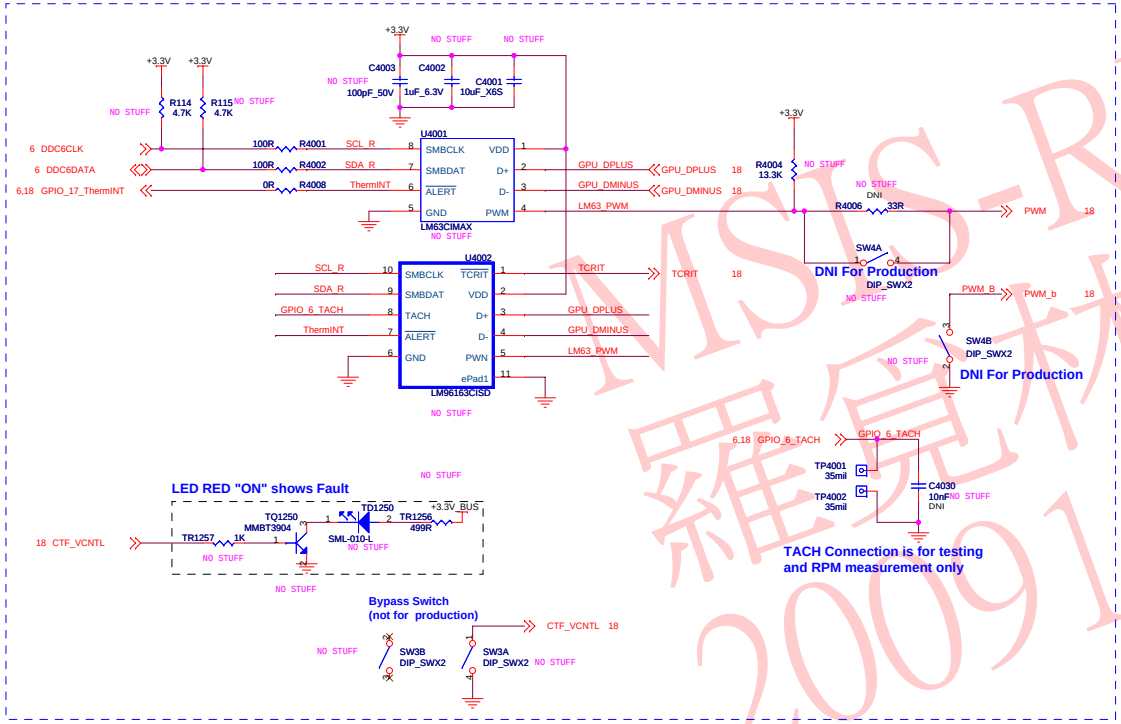
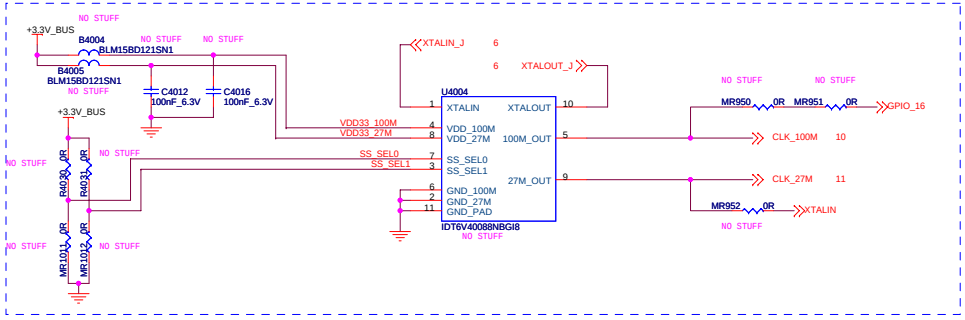
(17) Debug Circuits









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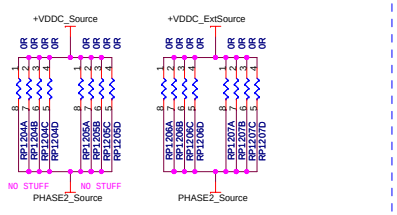
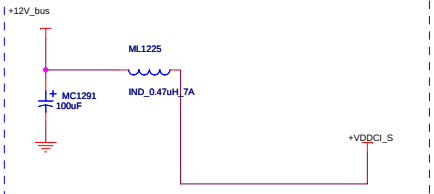
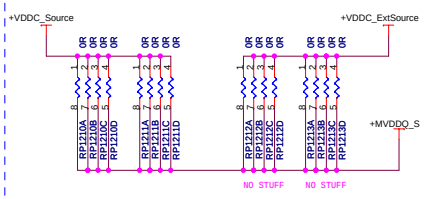
VDDC PHASE 2 Input Switching



VDDCI Input Switching



MVDDQ Input Switching

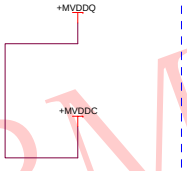


MVDDC Output Switching

Place close to MVDDC section
Mirrored on PCB

Place close to MVDDQ section
Mirrored on PCB

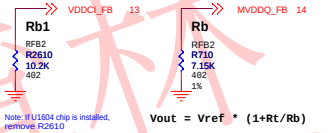
Mirrored on PCB



5-bit VID for VDDCI Setting

Place all parts close to the regulator that uses the voltage reference.
R1672 can be placed close to GPU for easy access to +3.3V.

Resistors to set the output voltages for +VDDCI, +MVDDQ and MVDDC.

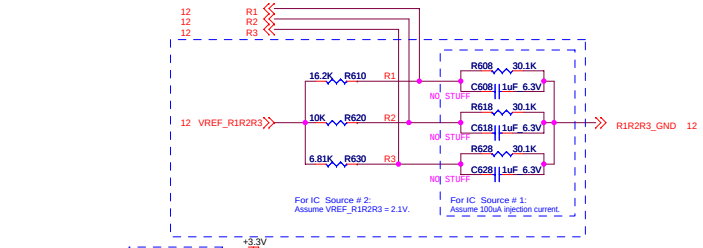


Vout = Vref * (1+Rt/Rb)

VDDC Setting

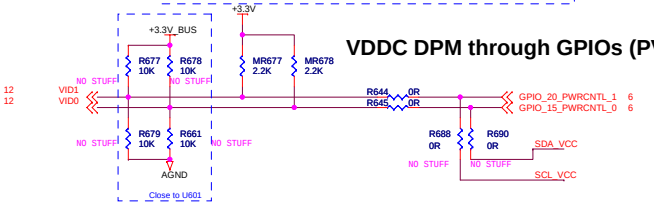
Set PWRON Default "DVT"

Analog Reference (Refer R to AGND)
Close to U601
Be careful when changing R655 value (VDDC IREF)

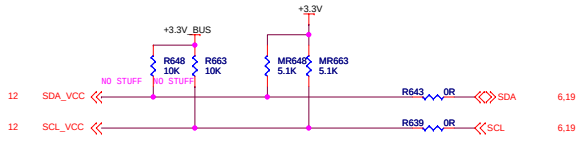


For Testing Only

VDDC DPM through GPIOs (PVID)



VDDC DPM through I2C (SVID)



MODE Pin Detection Circuit

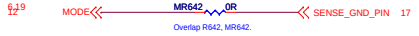
CASE 1 Configuration MODE Pin Detection Circuit

Case 1:
- Phase1,2 input from 12V_PCIE
- Phase3 input from 12V_EXT

Table 2 MODE Pin VS. Phase Operation

12V_EXT Cable	EXT_12V_DETb	MODE Pin	Phase Operation		
			Phase 1	Phase 2	Phase 3
On	GND	Low	Enabled	Enabled	Enabled
Off	Open	High	Enabled	Enabled	Disabled

CASE 2 Configuration MODE Pin Detection Circuit



Case 2:
- Phase1 input from 12V_PCIE
- Phase2,3 input from 12V_EXT

Table 3 MODE Pin VS. Phase Operation

12V_EXT Cable	EXT_12V_DETb	MODE Pin	Phase Operation		
			Phase 1	Phase 2	Phase 3
On	GND	Low	Enabled	Enabled	Enabled
Off	Open	Floating	Enabled	Disabled	Disabled

CASE 3 Configuration MODE Pin Detection Circuit

Case 3:
- Phase1 input from 12V_PCIE
- Phase2 input from 12V_EXT
- Phase3 disabled.

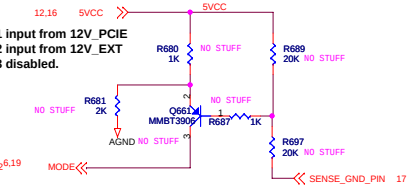


Table 4 MODE Pin VS. Phase Operation

12V_EXT Cable	EXT_12V_DETb	MODE Pin	Phase Operation		
			Phase 1	Phase 2	Phase 3
On	GND	High	Enabled	Enabled	Disabled
Off	Open	Floating	Enabled	Disabled	Disabled

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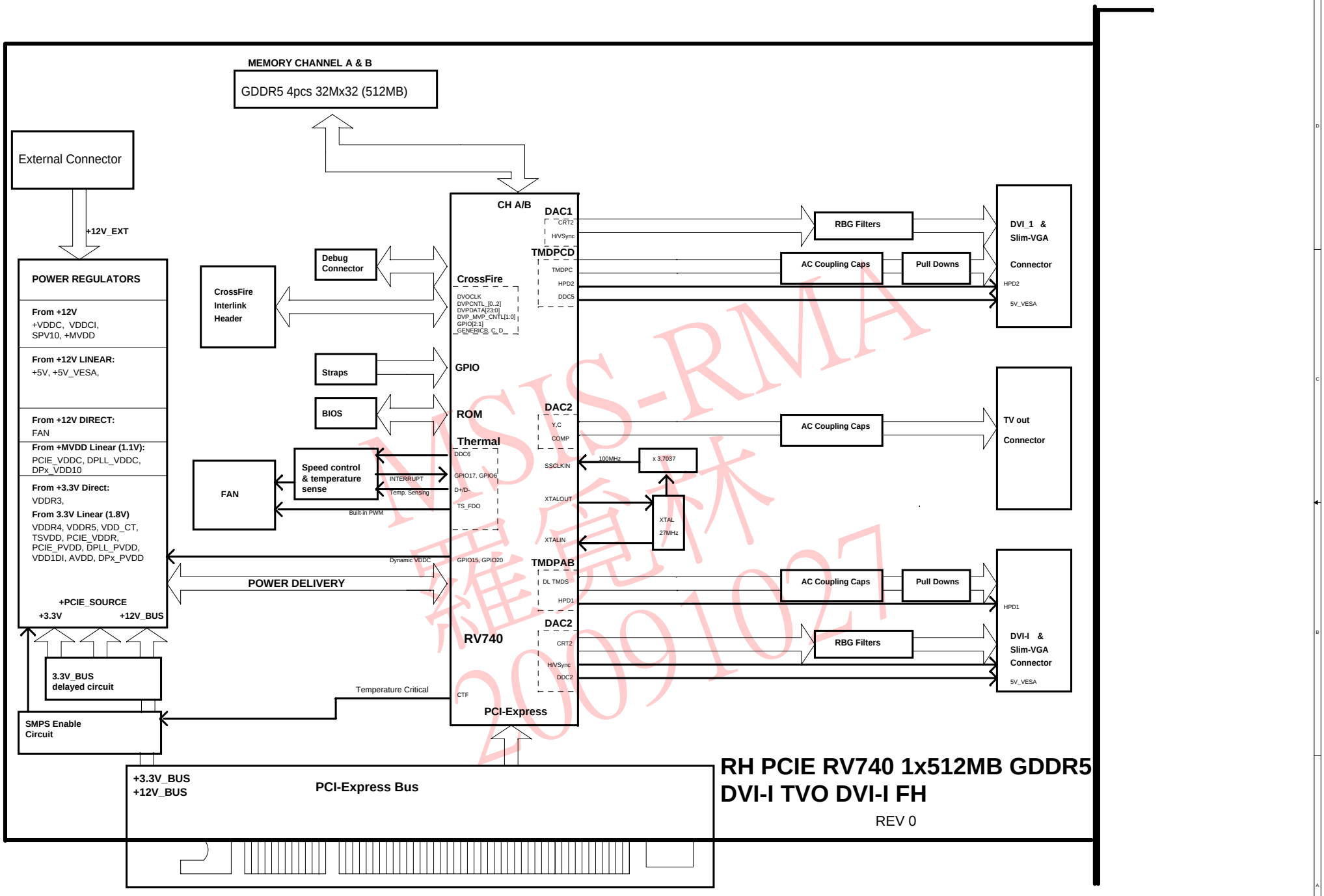

RH PCIE RV740 1x512MB GDDR5
DVI-I TVO DVI-I FH

REV 0

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Title	Schematic No.	Date:
RH RV740 GDDR5 DP-DP- DVII TRIAL	105-B86300-00A	Wednesday, May 13, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	09/01/06	Based on B743
	10	09/04/29	PAGE 7 : Remove TV function PAGE 9 : Change DVI to HDMI PAGE 12 :Change Inductor and CAP footprint, Remove Input CAP PAGE 13 :Change Inductor and CAP footprint, PAGE 14 : Change Inductor and CAP footprint