MS8877-0A

P70, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, video capture, T-BIOS, Hardware Monitor, AGP4X

PCI DEVICE ID 0X0=0X171 FOR NV17-128D.

HISTORY:

X00:
first version for layout start. No video capture, no stereo. NO DRC CHECK.

X01:
fixed PCB footprints for IC_SO14_150MIL and CON_DVI-I_RA
added end-termination r-packs for address-status-bus
changed RGB filter to integrated 5-pole only
added video capture, BIOS, Strapping
changed RefDes
NO DRC CHECK

X02:
added missing end termination for FBBAx
changed stereo 3pin header
added clamp diodes for TV-out and video capture
changed topology for 2nd DDC (VGA / DVI)
NO DRC CHECK

X03:
splitted analog/digital suply for SAA7113 (no component change)
Fixed some RefDes
Changed the strapping resistors cases to 0402
NO DRC CHECK

X04:
changed C617 to SMD0603
changed U502 and U503 to TSSOP14
added CKE connection to the memories
added D505 to the stereo section
changed L501, L502, L503 to 0603
NO DRC CHECK

X05:
changed U601 to SOT223-DPAK-D2PAK
added bracket
changed L600 to IND_CDR73
added VIP connector
NO DRC CHECK

X06:
deleted VIP
changed TPs to HOLE_48C28P
changed switcher gate circuit (no component change)
added C641 and C642 to the linear voltage regulator
pinswap of memory termination
NO DRC CHECK

X07:
deleted page 10: 5.b ViVo
changed filter topology for RGB
added return traces for RGB
NO DRC CHECK

X08:
added TV filter caps with reference to GND (C511,C517,C522)
separated RGB returns (NOTE: there will be a change for DAC2)
NO DRC CHECK

X09:
added net names to unused panel signals (test points)
NO DRC CHECK

X10:
added decoupling for DVO rail (C529 and C530)
added GND connection to pin 1 of U700
added R520 pull down for DVOCLKIN
DRC CHECK DONE

X11:
changed caps in power section to the combined footprints

X12:
data bus swappings

X13:
swapped CLKs for U201 and U202

X14:
connected the RGB returns of VGA2 together

X15:
update materials

X16:
update stuffings

X17-A01:
release A01
changed DVOVDD from VID3.3V to A3.3V
add linear regulator for NV17's VDD33
connected the IFP-RSETs to GND
deleted C134 and C135

X18:
change to target release A02
changed I2C assignments
added I2C filter components for ViVo (L506,L507,R521-R524,D506,D507,C531,C532)

X19:
added R243-R250 for clock pull-up.

X20-A02:
material changes.

X21-A03:
fixed values and descriptions for R609, R613 and C640
changed the RGB filter topology:
- delete R325-R330
- connect all DACRTN to GND
- move the 75R termination resistors to the connector
changed RGB clamping to A3.3V
add testpoint net XTALOUTBUFF
changed XTAL-load caps C320 and C321 to 18pF
removed obsolete 0603 0Ohm resistors
NO_STUFFed the stereo 3-pin header.

X22-A03:
changed bulk decoupling in VGA section from 3.3V to A3.3V
fixed DAC1BLUE (net name was missing)

X23-A03:
changed VDD33 to A3.3V

X24-A03:
added C643 for memory core decoupling

X25-A03:
changed the long body VGA connector to a three pin type
changed C425 connection for fan decoupling

PAGE OVERVIEW

Stuffing Options	Meaning
COMMON	common components for all skus
NO_STUFF	no assembly at all
XTAL_27	stuff the 27MHz xtal for the GPU
XTAL_14	stuff the 14.318MHz xtal for the GPU
VIVO	stuff video I/O
VIDCAP	stuff video capture
TV_OUT	stuff TV-out
DVI-I	stuff the DVI-I option
DVI	stuff the DVI-D option
2NDVGA	stuff a second VGA
NO_DVI	don't stuff any DVI
SYNC_DRIVER2	stuff the termination resistors for the DACB syncs
SYNC_DRIVER	stuff the sync driver chip
NO_SYNC_DRIVER2	bypass the sync driver for the DAC B syncs
NO_SYNC_DRIVER	bypass the sync driver for the DAC A syncs
STEREOSYNCS	stuff the switchable stereo sync circuit
STEREOSYNC2	sync stereo to DAC B
STEREOSYNC1	sync stereo to DAC A
STEREO	stuff the generic stereo circuit
SI2C_PROT	stuff the protection diodes for syncs and I2C at DAC A
RGB_PROT	stuff the protection diodes for RGB at DAC A
2NDVGA_RGB_PROT	stuff the protection diodes for RGB at DAC B
2NDSI2C_PROT	stuff the protection diodes for syncs and I2C at DAC B
SET_NVVDD_ISL	set NVVDD voltage at Intersil switcher
SET_NVVDD_IRU	set NVVDD voltage at IR/Uniseml switcher
SET_FBVDDQ_ISL	set FBVDDQ voltage at Intersil switcher
SET_FBVDDQ_IRU	set FBVDDQ voltage at IR/Uniseml switcher
NO_1117	bypass the A3.3V regulator to AGP3.3V
ISL	stuff the Intersil switcher
IRU	stuff the IR/Unisem switcher
FBVDD_3.3	connect FBVVDD with AGP3.3V
FBVDD_2.5	connect FBVVDD with FBVDDQ
1117_ADJ	stuff the adjustable regulator for A3,3V
1117	stuff the fixed regulator for A3,3V
PASSIVE_HS	have passive heatsink
FAN	fan sink and components
BRCKT_VGA_TV_VGA	Bracket VGA-TV-VGA
BRCKT_VGA_TV_DVI	Bracket VGA-TV-DVI
BRCKT_VGA_TV	Bracket VGA-TV
BRCKT_VGA	Bracket VGA
MEMSTRAP1111	strap memory to 1111
MEM-64B	stuff 64 bit memory - 2pcs
MEM-128B	stuff 128 bit memory - 4pcs
NV17-128D	stuff NV17-128D

140-10070-0000-A03
602-10070-0000-A03

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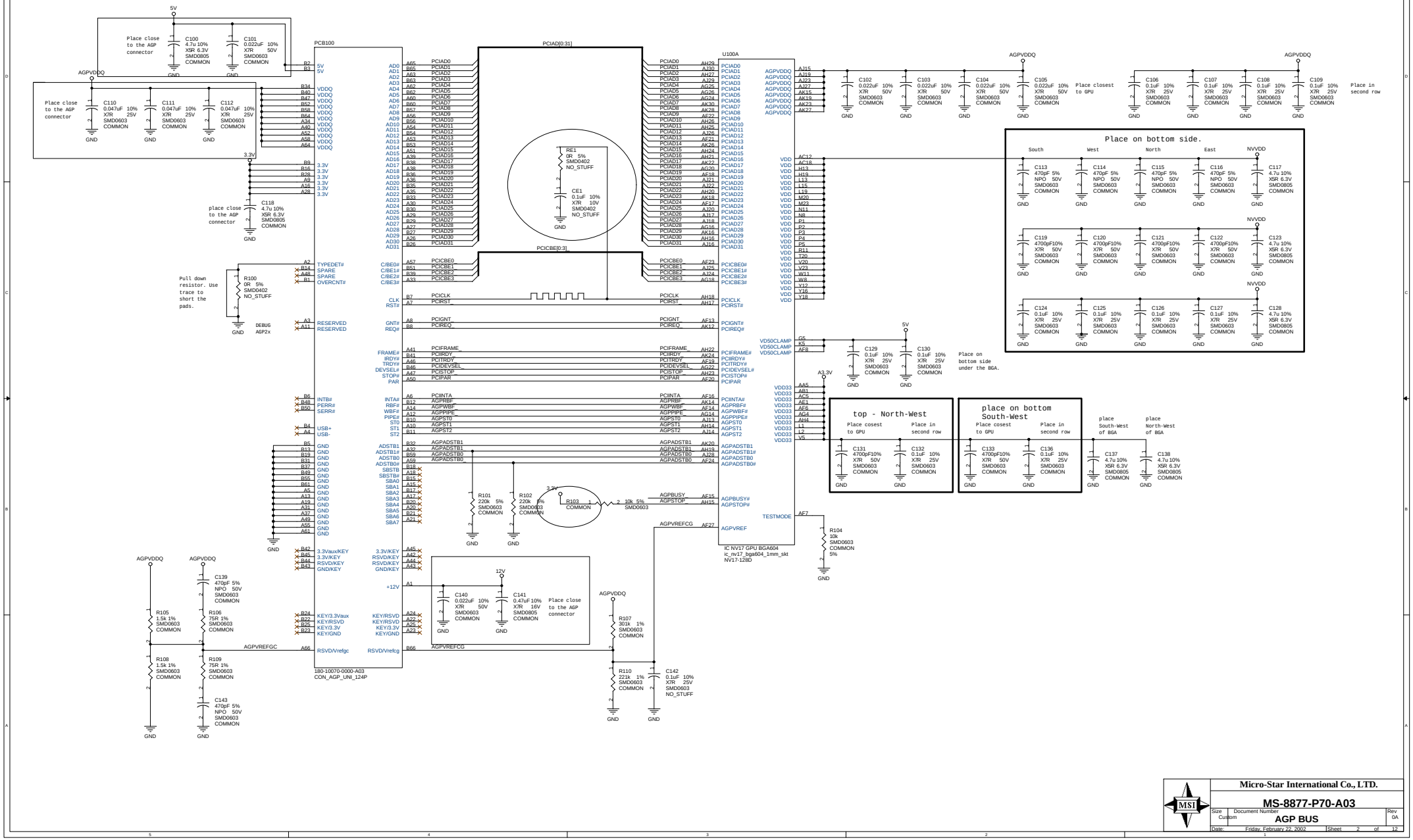
5V
AGPVDDQ
3.3V
GND
PCB100
PCIAD[0:31]
PCICBE[0:3]
U100A
IC NV17 GPU BGA604
ic_nv17_bga604_1mm_skt
NV17-128D
180-10070-0000-A03
CON_AGP_UNI_124P
Place close to the AGP connector
place close to the AGP connector
Pull down resistor, use trace to short the pads.
DEBUG AGP2x
Place closest to GPU
Place in second row
Place on bottom side.
Place on bottom side under the BGA.
top - North-West
place on bottom South-West
place South-West of BGA
place North-West of BGA
Place close to the AGP connector
12V
3.3V
A3.3V
TESTMODE
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AGP BUS
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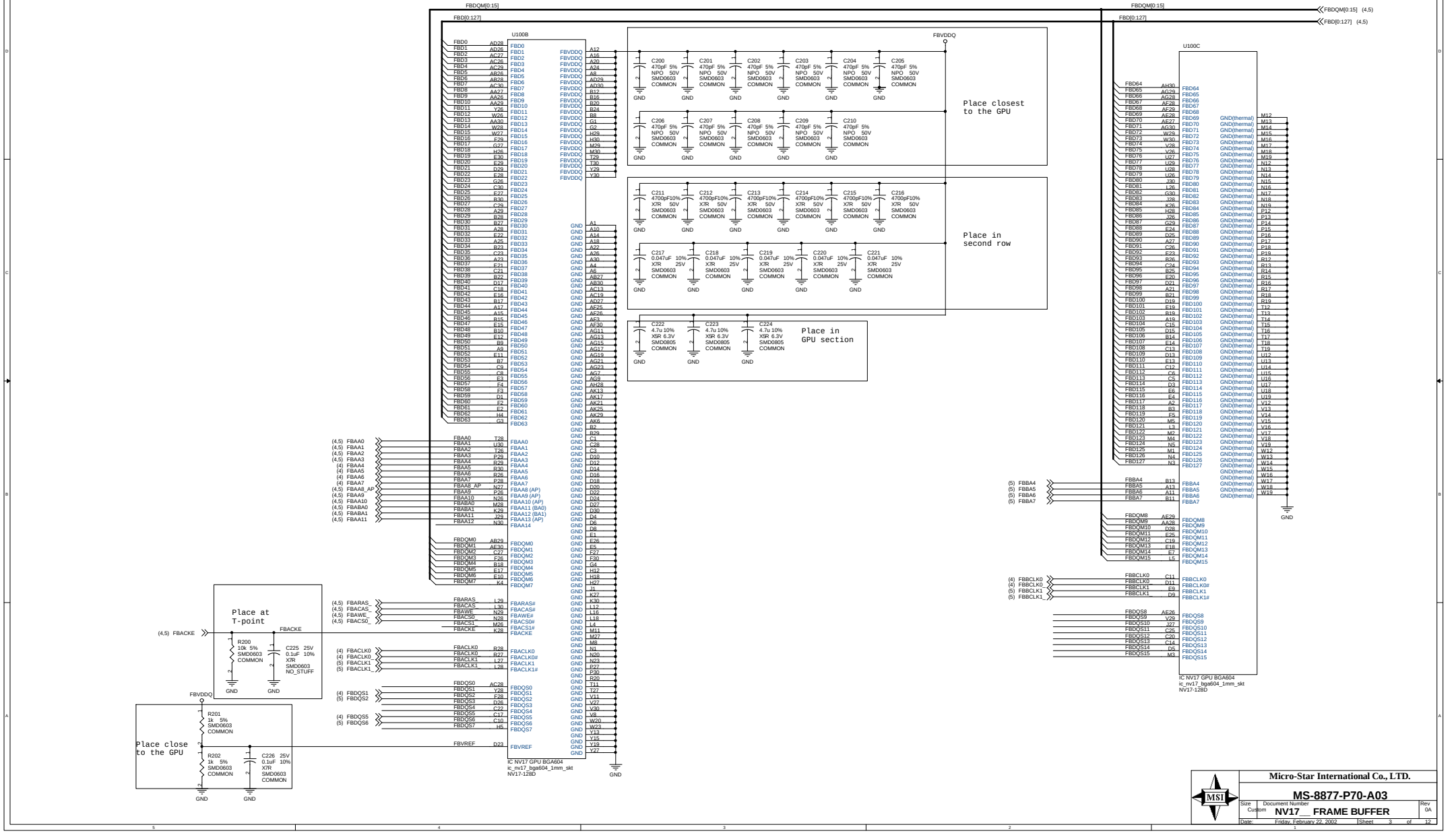
FBDQM[0:15]
FBD[0:127]
U100B
FBVDDQ
Place closest to the GPU
Place in second row
Place in GPU section
C200 470pF 5% NPO 50V SMD0603 COMMON
C201 470pF 5% NPO 50V SMD0603 COMMON
C202 470pF 5% NPO 50V SMD0603 COMMON
C203 470pF 5% NPO 50V SMD0603 COMMON
C204 470pF 5% NPO 50V SMD0603 COMMON
C205 470pF 5% NPO 50V SMD0603 COMMON
C206 470pF 5% NPO 50V SMD0603 COMMON
C207 470pF 5% NPO 50V SMD0603 COMMON
C208 470pF 5% NPO 50V SMD0603 COMMON
C209 470pF 5% NPO 50V SMD0603 COMMON
C210 470pF 5% NPO 50V SMD0603 COMMON
C211 4700pF10% X7R 50V SMD0603 COMMON
C212 4700pF10% X7R 50V SMD0603 COMMON
C213 4700pF10% X7R 50V SMD0603 COMMON
C214 4700pF10% X7R 50V SMD0603 COMMON
C215 4700pF10% X7R 50V SMD0603 COMMON
C216 4700pF10% X7R 50V SMD0603 COMMON
C217 0.047uF 10% X7R 25V SMD0603 COMMON
C218 0.047uF 10% X7R 25V SMD0603 COMMON
C219 0.047uF 10% X7R 25V SMD0603 COMMON
C220 0.047uF 10% X7R 25V SMD0603 COMMON
C221 0.047uF 10% X7R 25V SMD0603 COMMON
C222 4.7u 10% X5R 6.3V SMD0805 COMMON
C223 4.7u 10% X5R 6.3V SMD0805 COMMON
C224 4.7u 10% X5R 6.3V SMD0805 COMMON
GND
Place at T-point
R200 10k 5% SMD0603 COMMON
C225 25V 0.1uF 10% X7R SMD0603 NO_STUFF
R201 1k 5% SMD0603 COMMON
Place close to the GPU
R202 1k 5% SMD0603 COMMON
C226 25V 0.1uF 10% X7R SMD0603 COMMON
IC NV17 GPU BGA604
ic_nv17_bga604_1mm_skt
NV17-128D
U100C
IC NV17 GPU BGA604
ic_nv17_bga604_1mm_skt
NV17-128D
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NV17__ FRAME BUFFER
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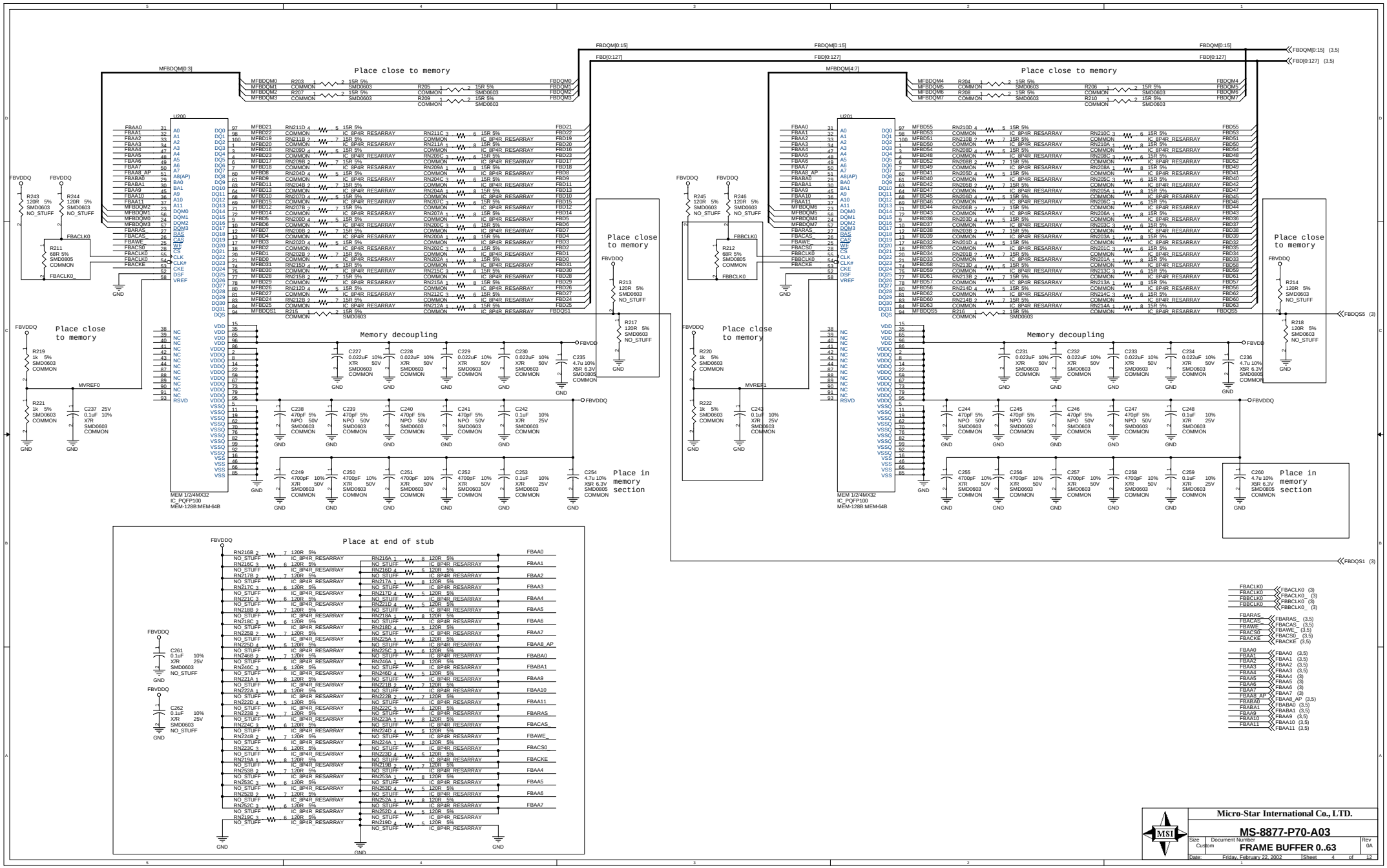
Place close to memory
Place close to memory
Place close to memory
Place close to memory
Place close to memory
Place close to memory
Memory decoupling
Memory decoupling
Place in memory section
Place in memory section
Place at end of stub
MFBDQM[0:3]
MFBDQM[4:7]
FBDQM[0:15]
FBD[0:127]
U200
U201
MEM 1/2/4MX32
IC_PQFP100
MEM-128B:MEM-64B
FBVDDQ
GND
FBACLK0
FBBCLK0
MVREF0
MVREF1
FBDQS5 (3)
FBDQS1 (3)
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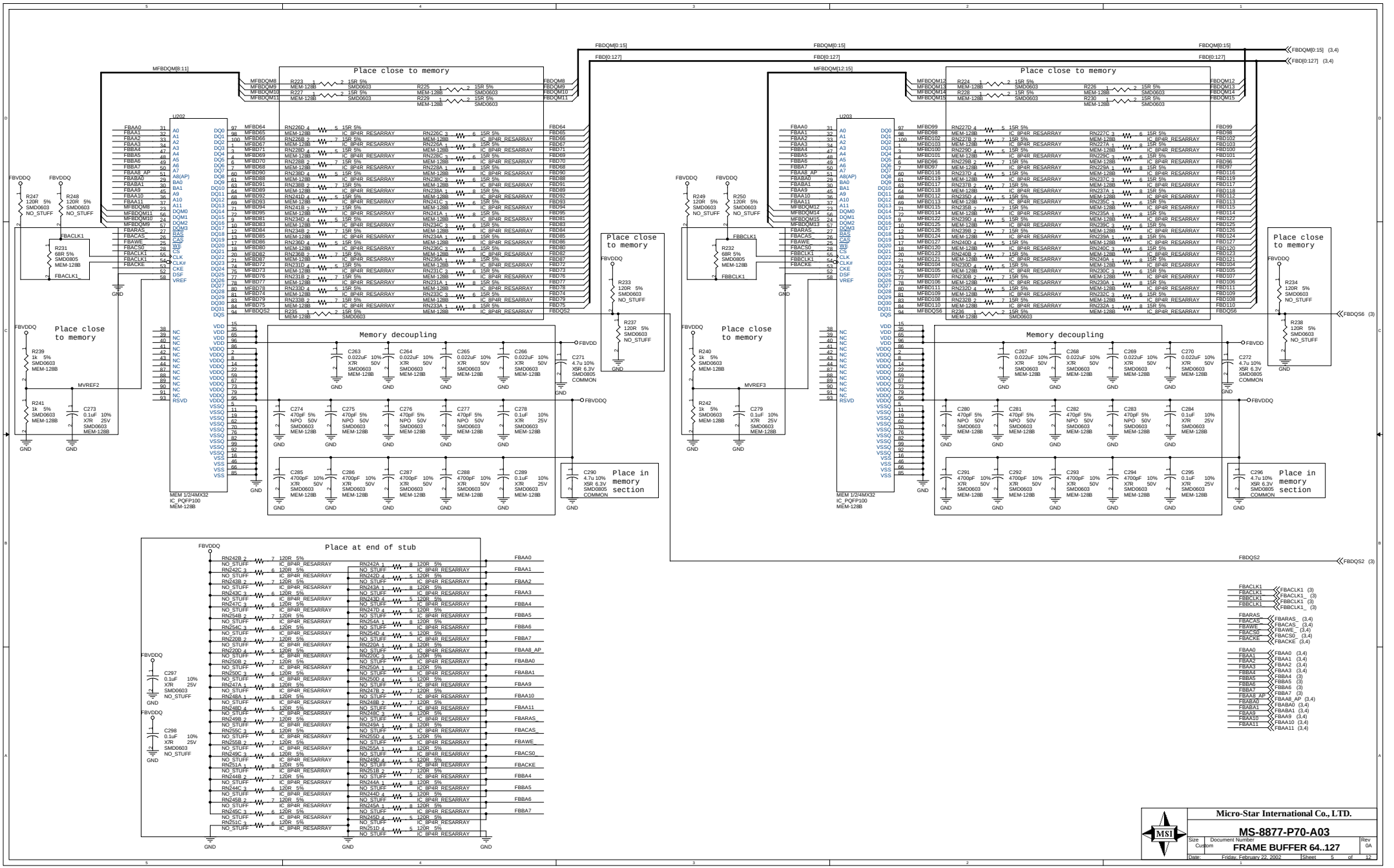

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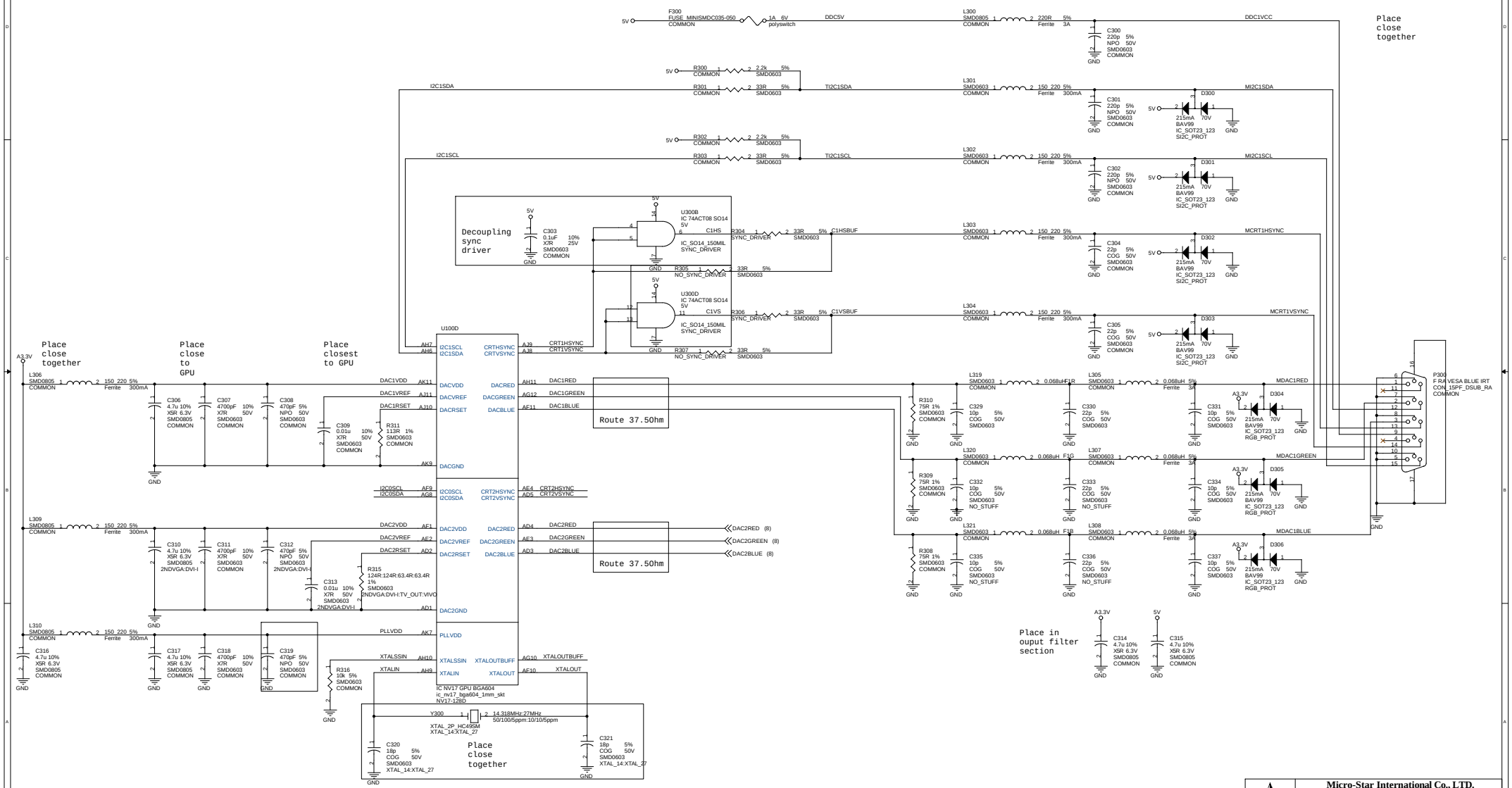

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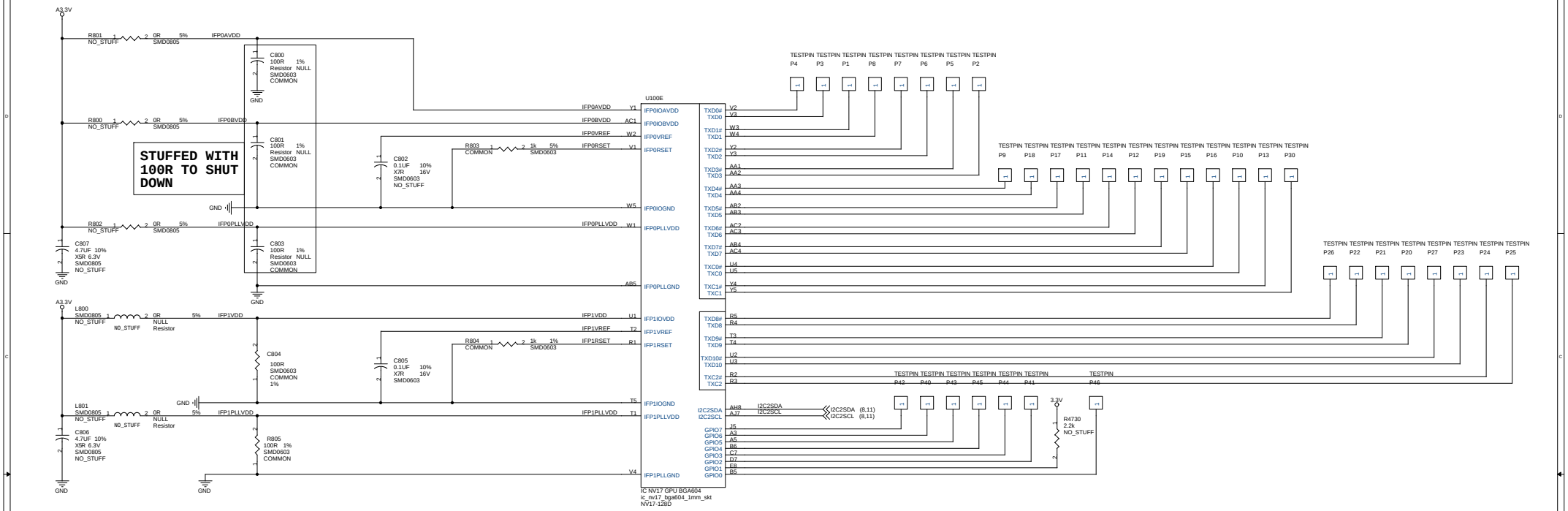

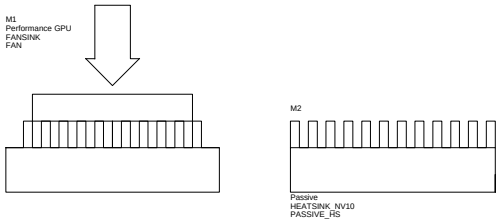

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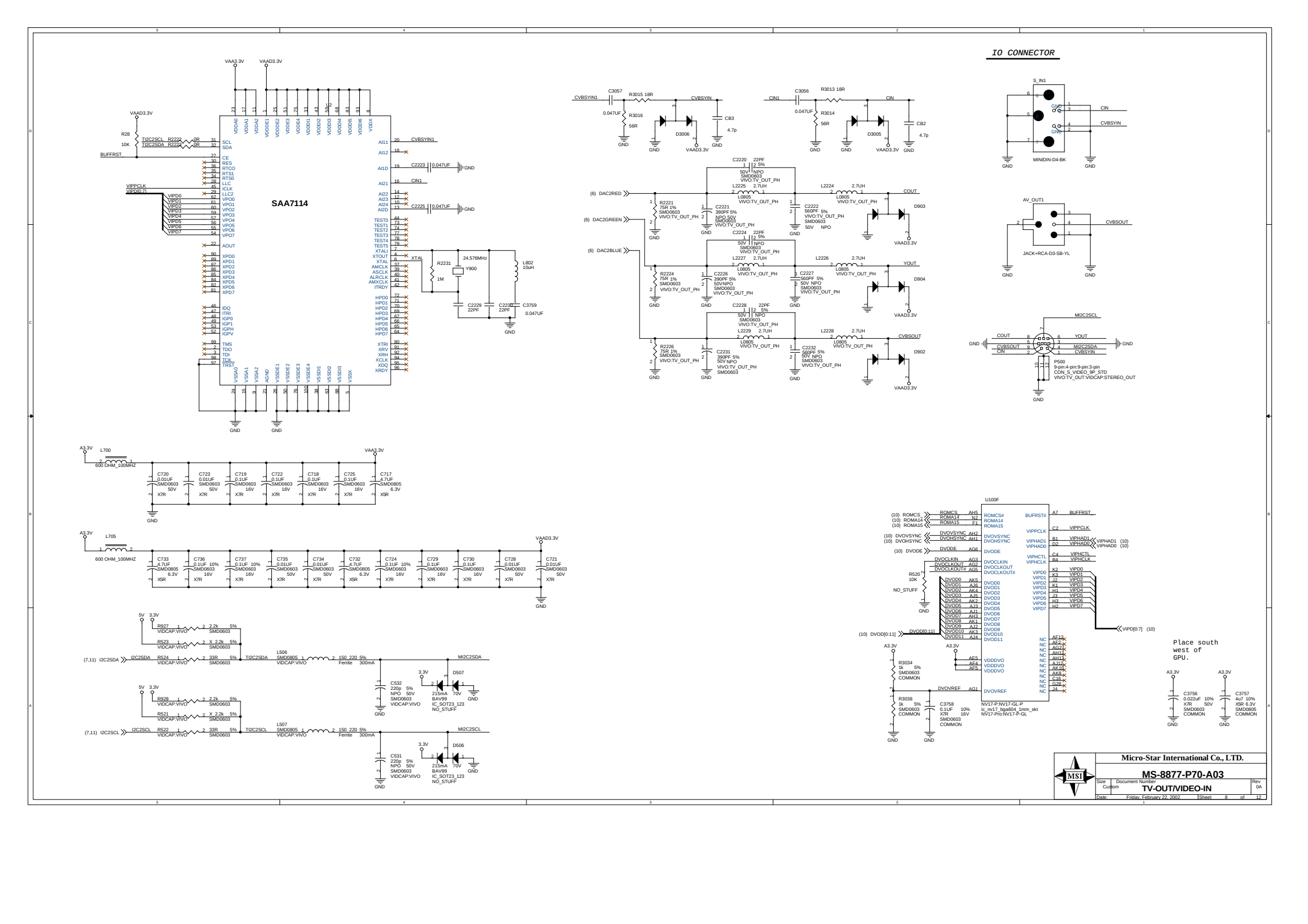
IO CONNECTOR
SAA7114
S_IN1
MINIDIN-D4-BK
AV_OUT1
JACK+RCA-D3-SB-YL
P500
9-pin:4-pin:9-pin:3-pin
CON_S_VIDEO_9P_STD
VIVO:TV_OUT:VIDCAP:STEREO_OUT
U100F
NV17-P:NV17-GL-P
ic_nv17_bga604_1mm_skt
NV17-Pro:NV17-P-GL
Place south west of GPU.
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TV-OUT/VIDEO-IN
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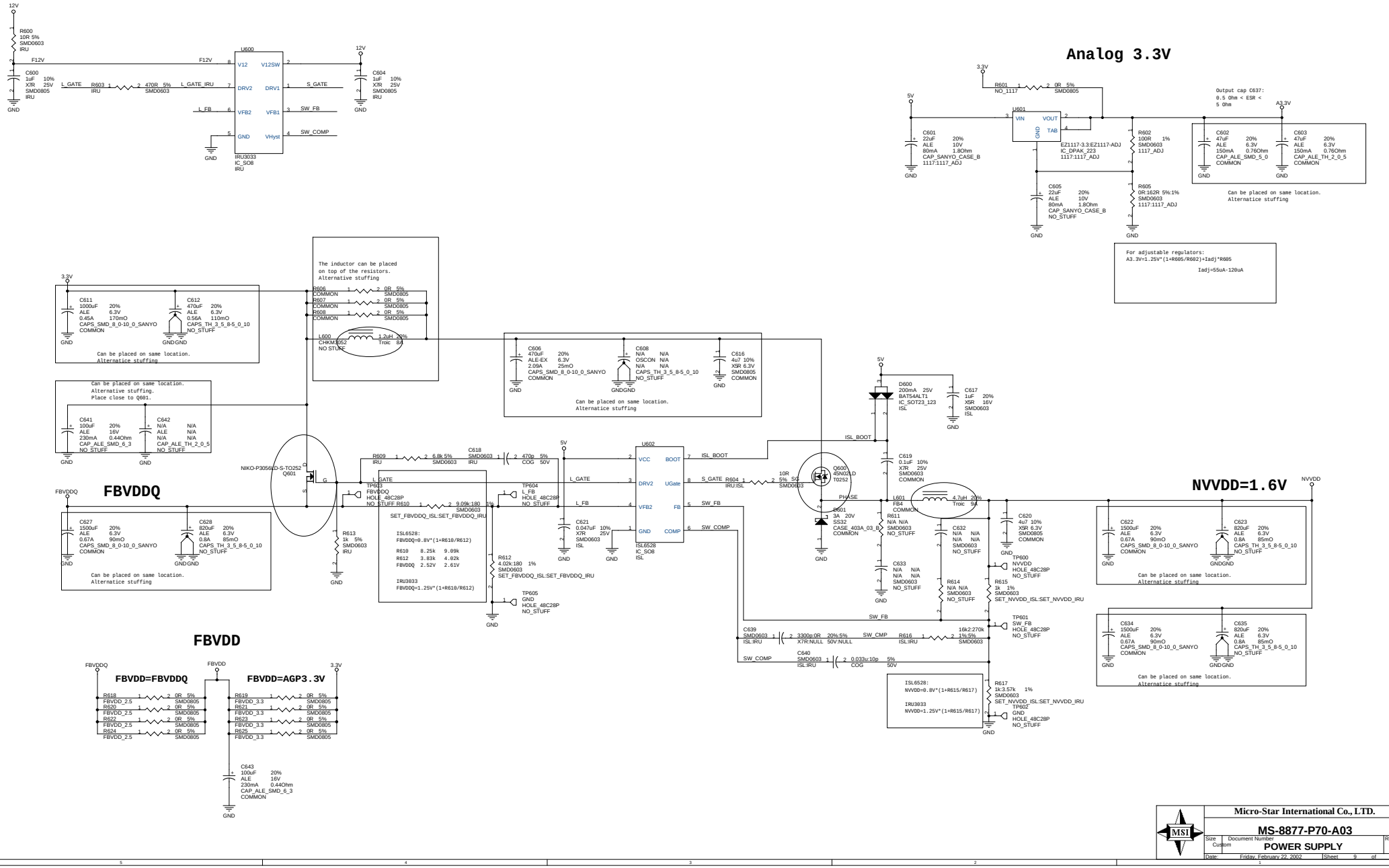
Analog 3.3V
FBVDDQ
FBVDD
NVVDD=1.6V
FBVDD=FBVDDQ
FBVDD=AGP3.3V
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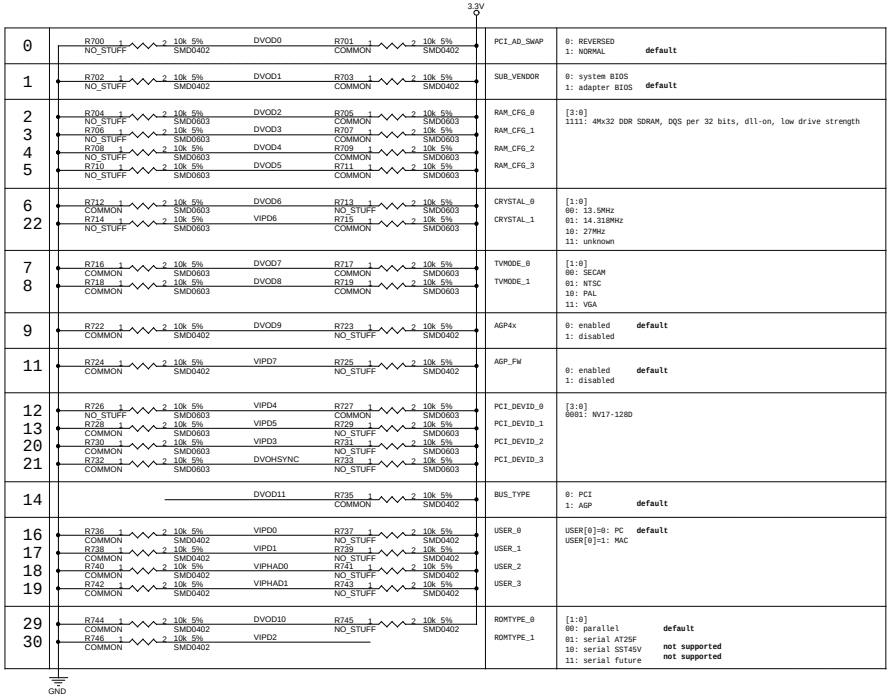
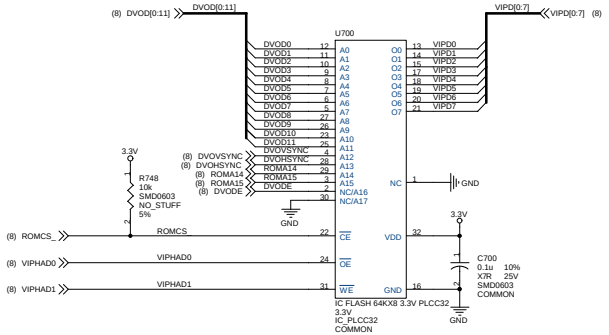
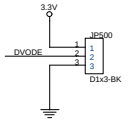
POWER SUPPLY



CHANGE 0402 TO 0603



Twin BIOS



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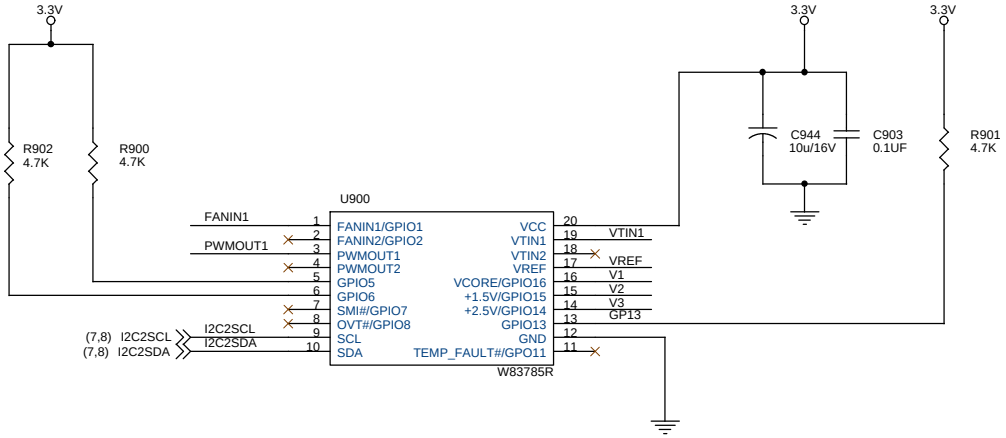
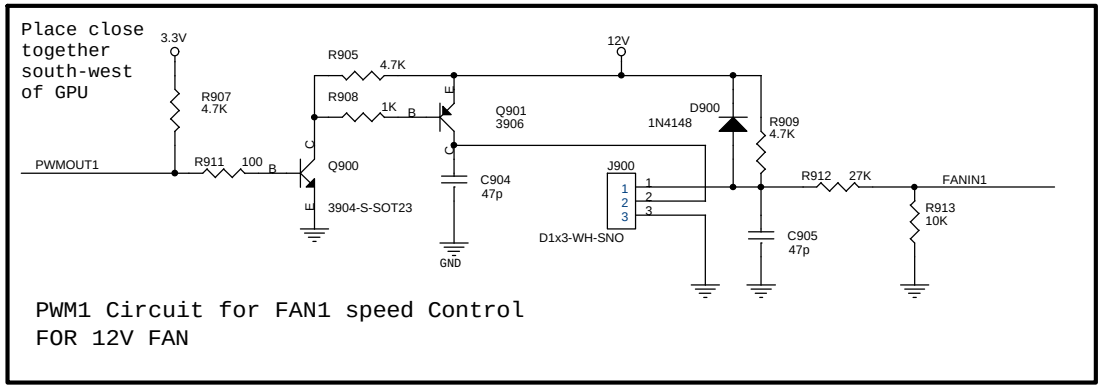
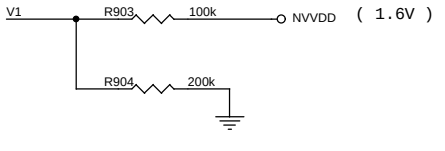
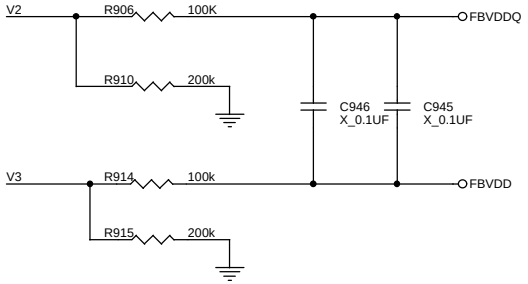


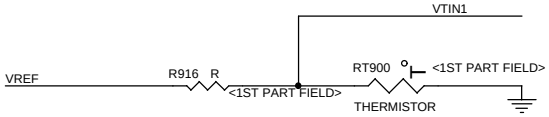


PWM1 Circuit for FAN1 speed Control
FOR 12V FAN





VOLTAGE SENSORING CIRCUIT



TEMPERATURE SENSORING CIRCUIT

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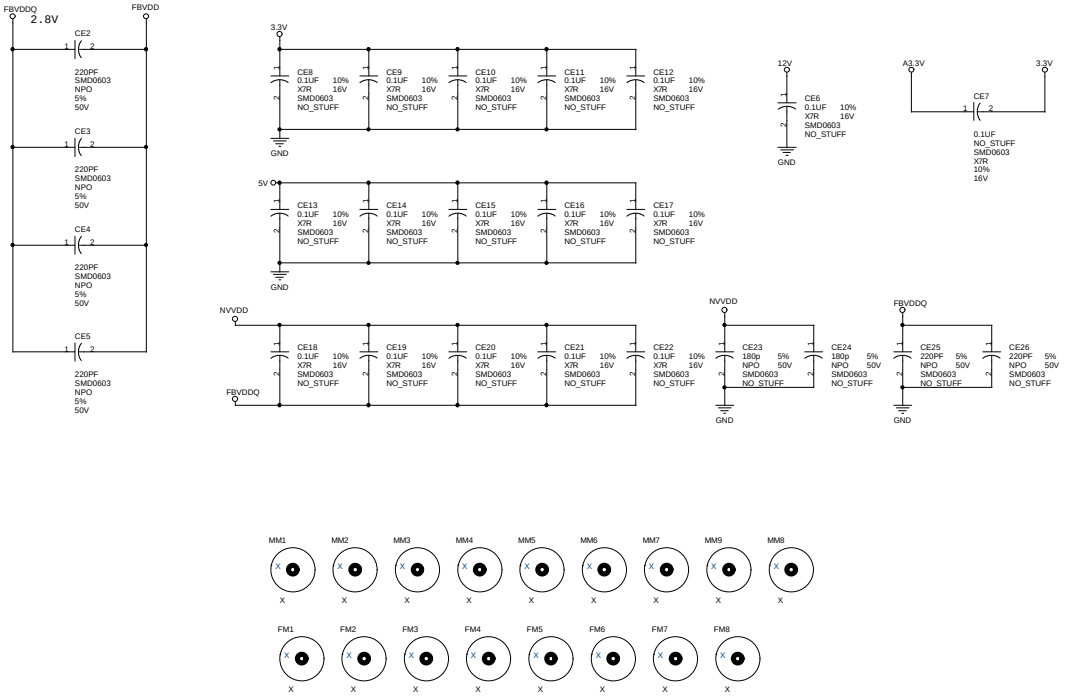
CE2-CE17 for EMI



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