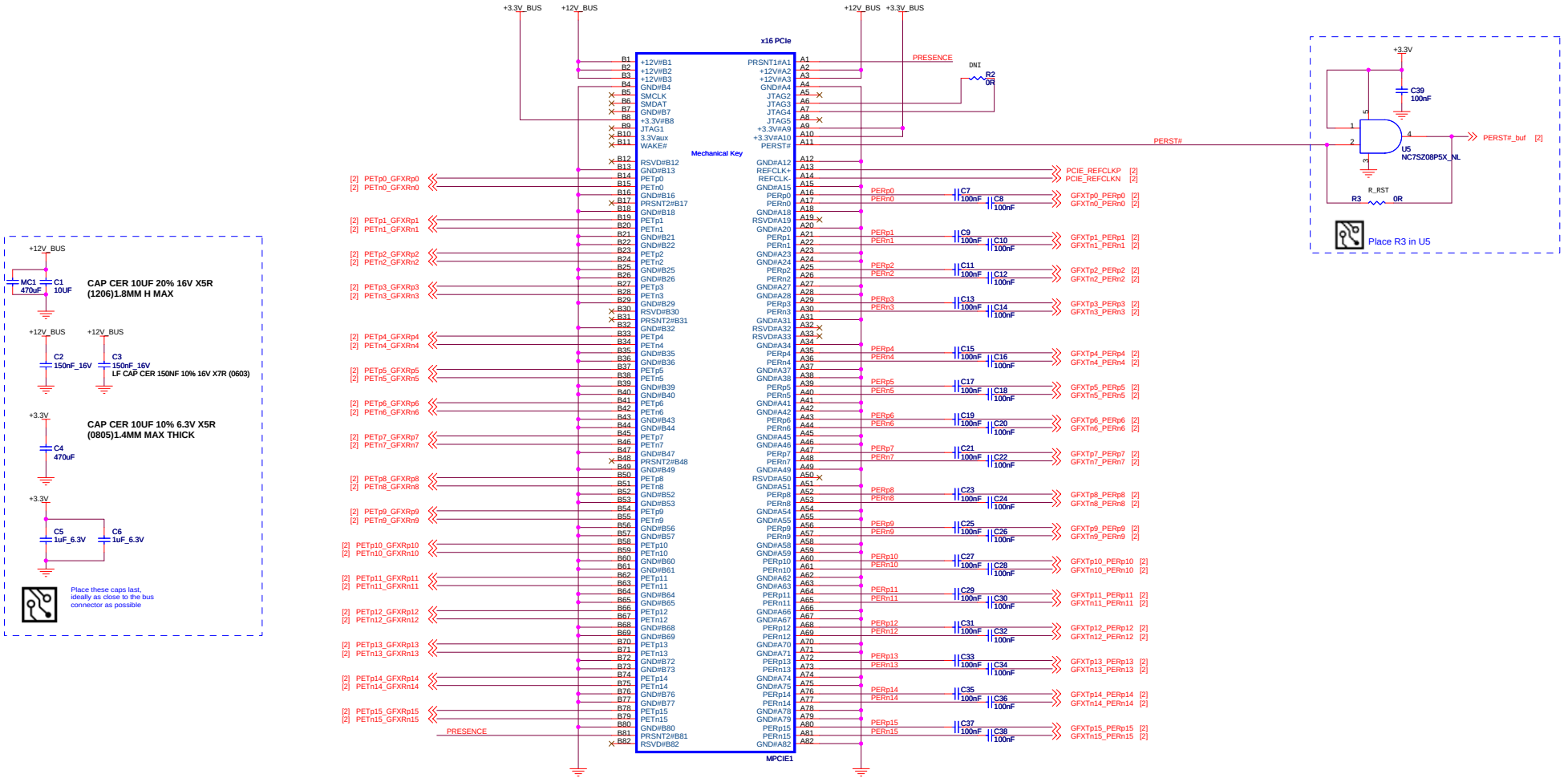
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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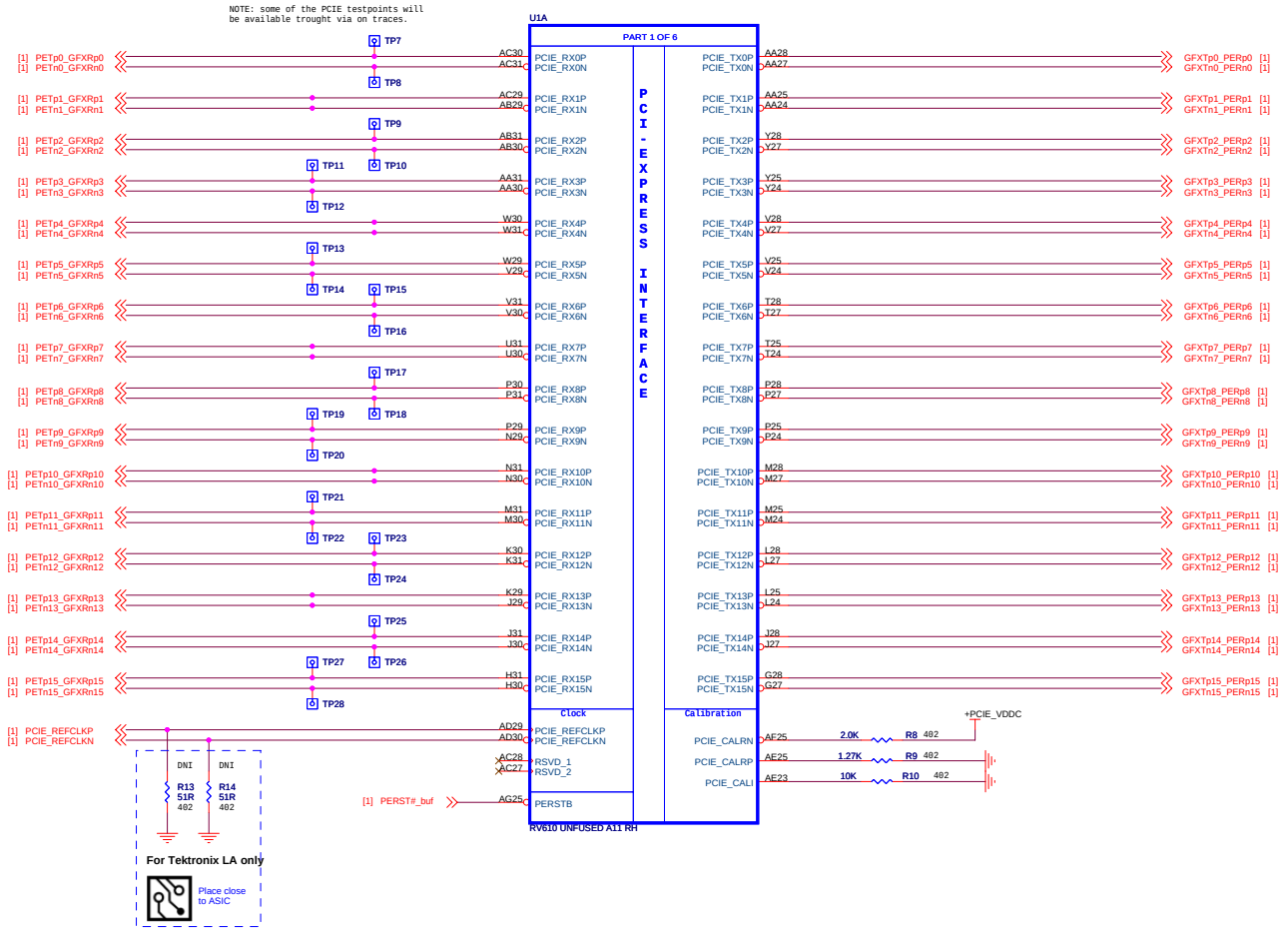
Size C	Document Number 105-B169xx-00A		Rev 32
Date: Friday, March 16, 2007	Sheet 1 of 19		



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Size C	Document Number 105-B169xx-00A	Rev 32
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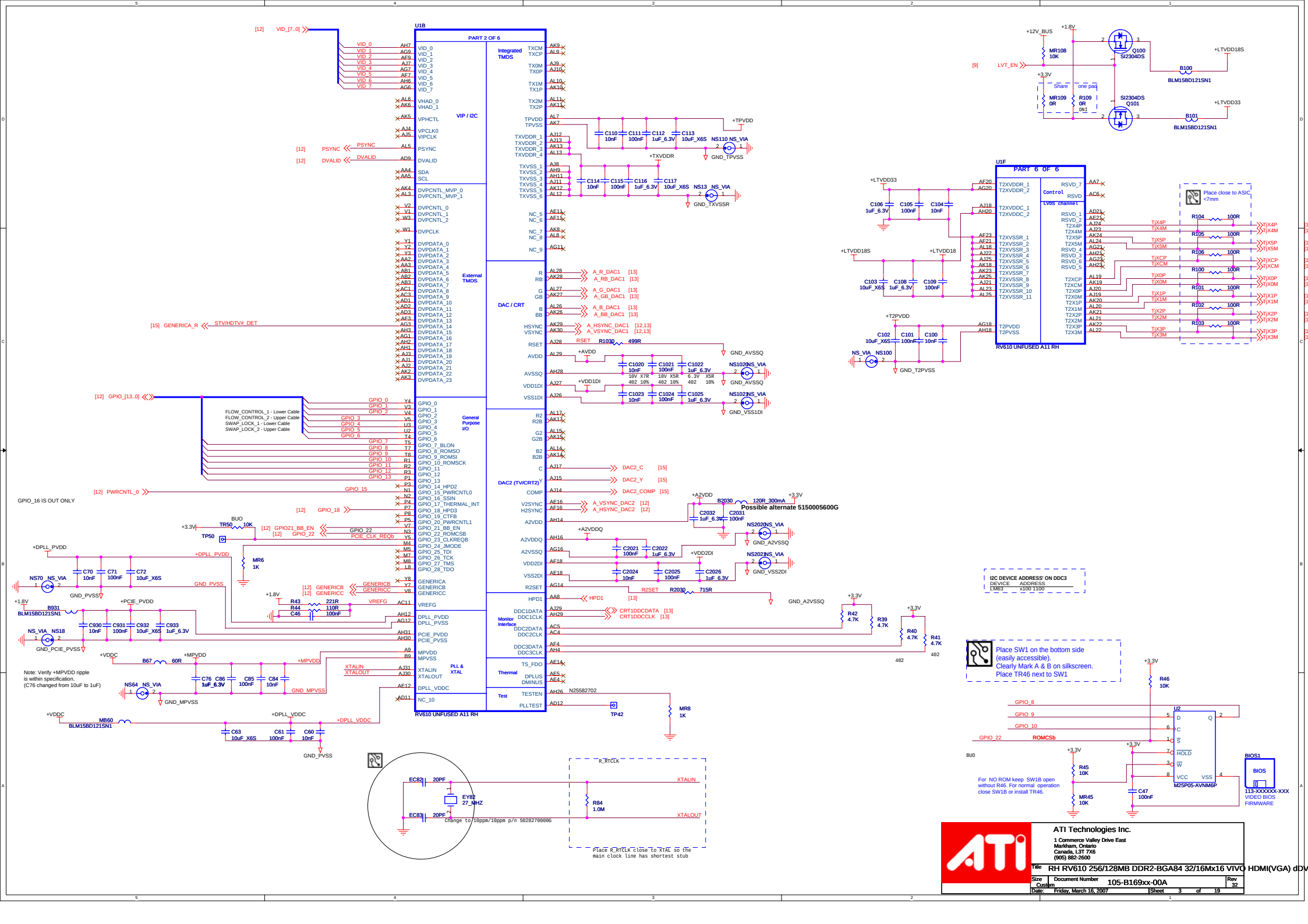
U1B
PART 2 OF 6
VIP / I2C
External TMDS
DAC / CRT
DAC2 (TV/CRT2)
General Purpose I/O
PLL & XTAL
Thermal
Test
RV610 UNFUSED A11 RH
U1F
PART 6 OF 6
Control
LVDS channel
RV610 UNFUSED A11 RH
Place close to ASIC <7mm
Place SW1 on the bottom side (easily accessible). Clearly Mark A & B on silkscreen. Place TR46 next to SW1
I2C DEVICE ADDRESS' ON DDC3
DEVICE ADDRESS
LM63 x100 1100
For NO ROM keep SW1B open without R46. For normal operation close SW1B or install TR46.
Change to 10ppm/10ppm p/n 5028270000
Place R_RTCLK close to XTAL so the main clock line has shortest stub
GPIO_16 IS OUT ONLY
Possible alternate 5150005600G
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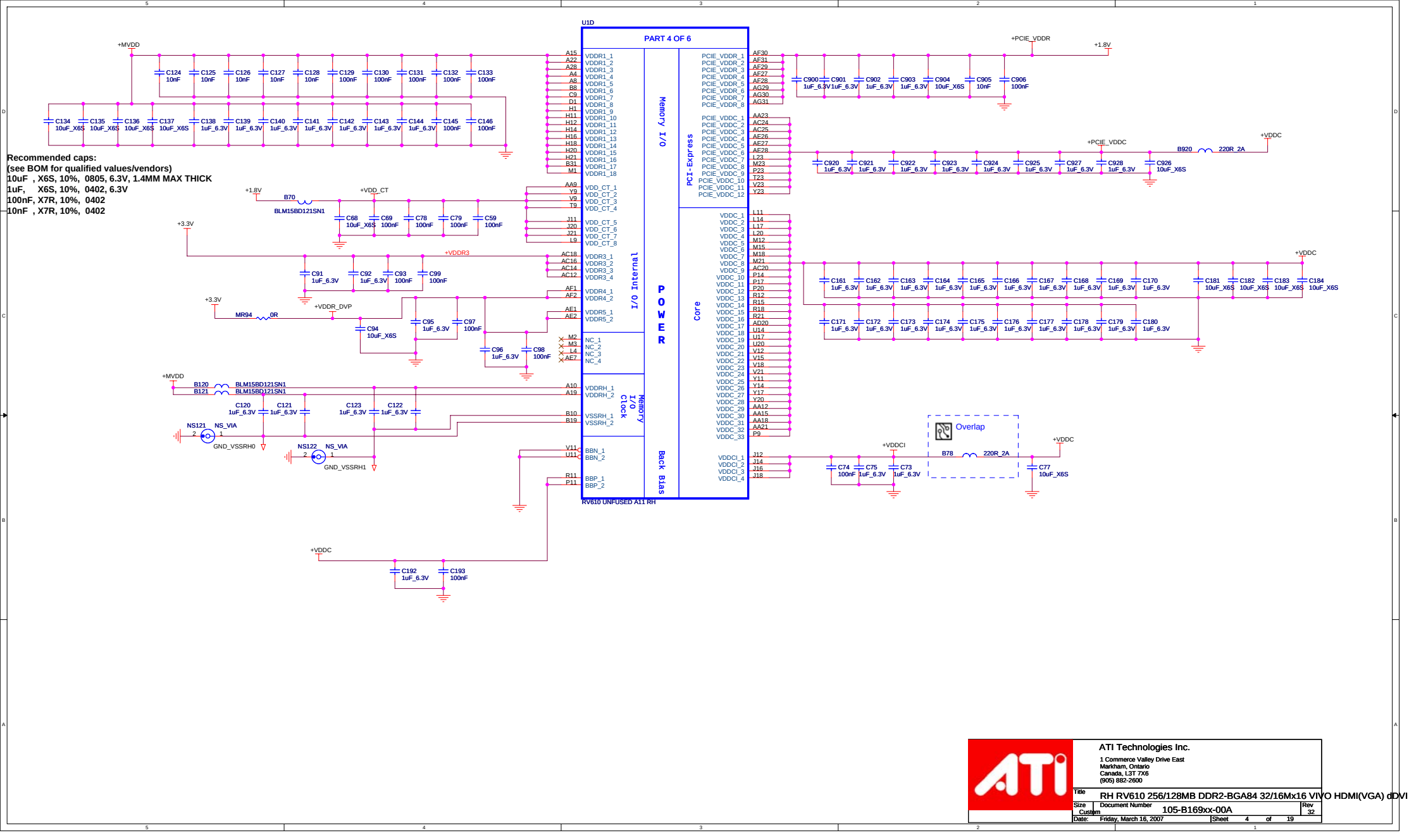
RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDV
105-B169xx-00A
Friday, March 16, 2007



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Title	RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI
Size: Custom	Document Number: 105-B169xx-00A
Rev: 32	
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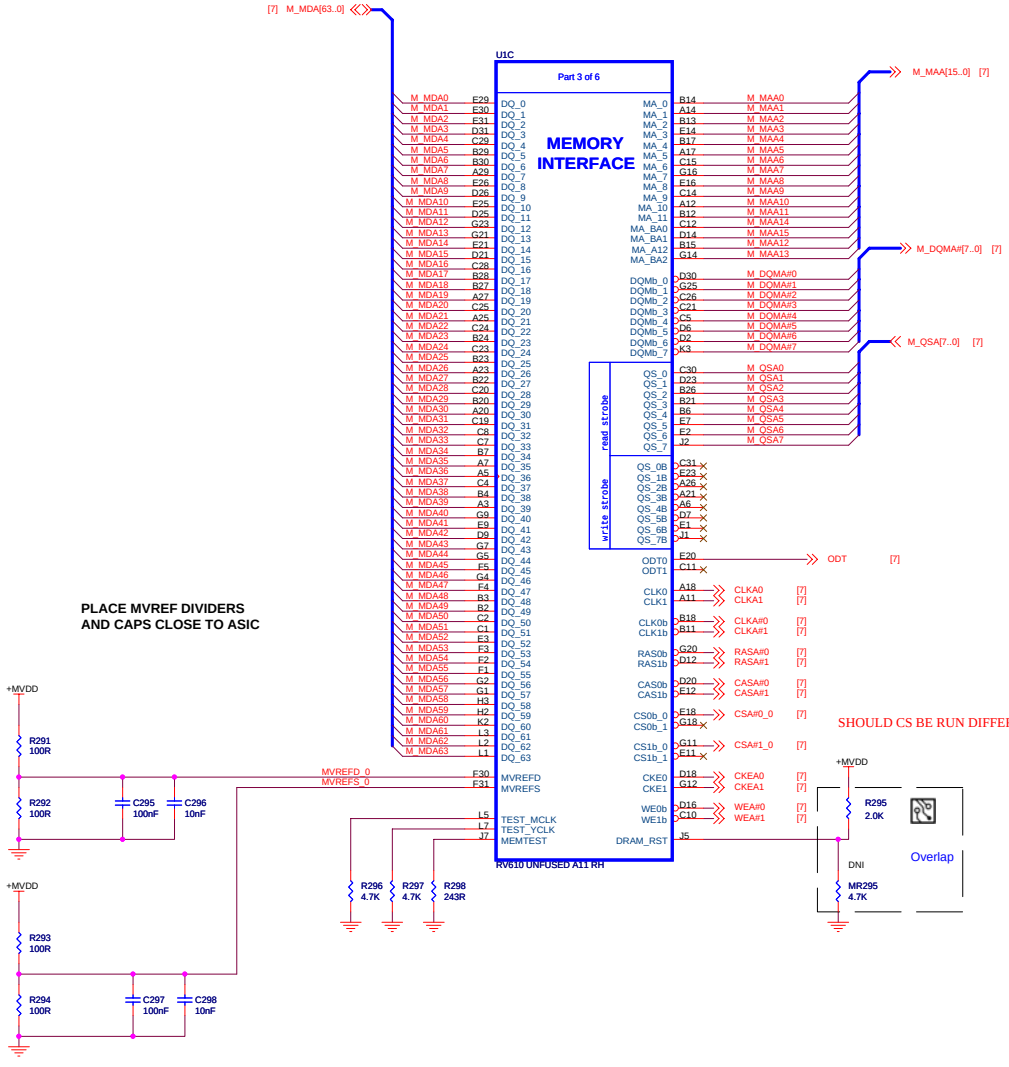

DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

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Size: C | Document Number: 105-B169xx-00A | Rev: 32

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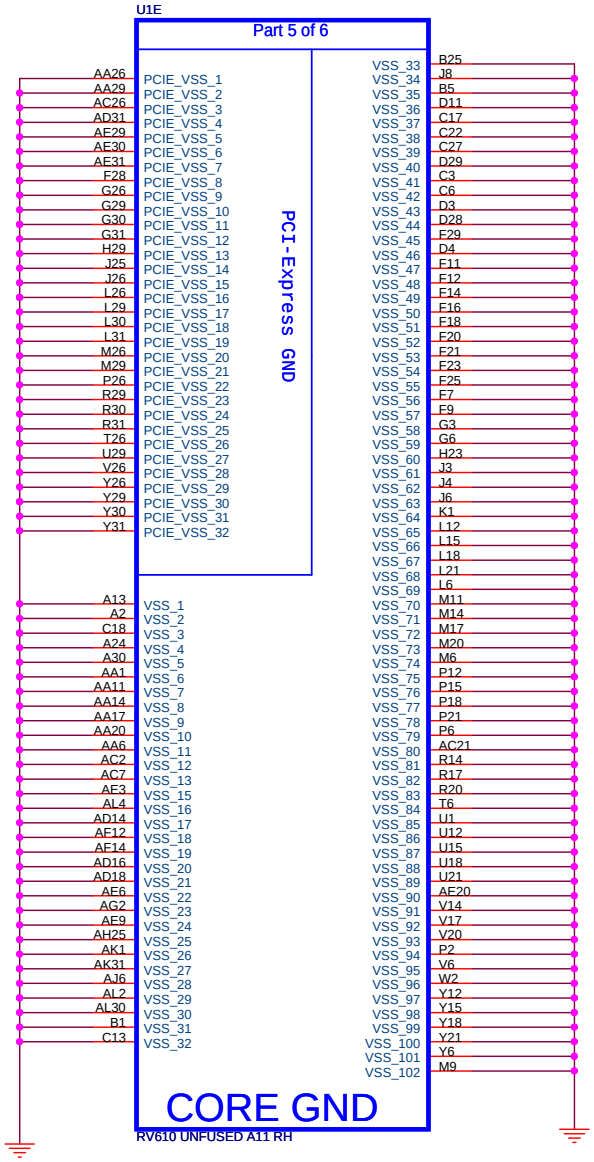

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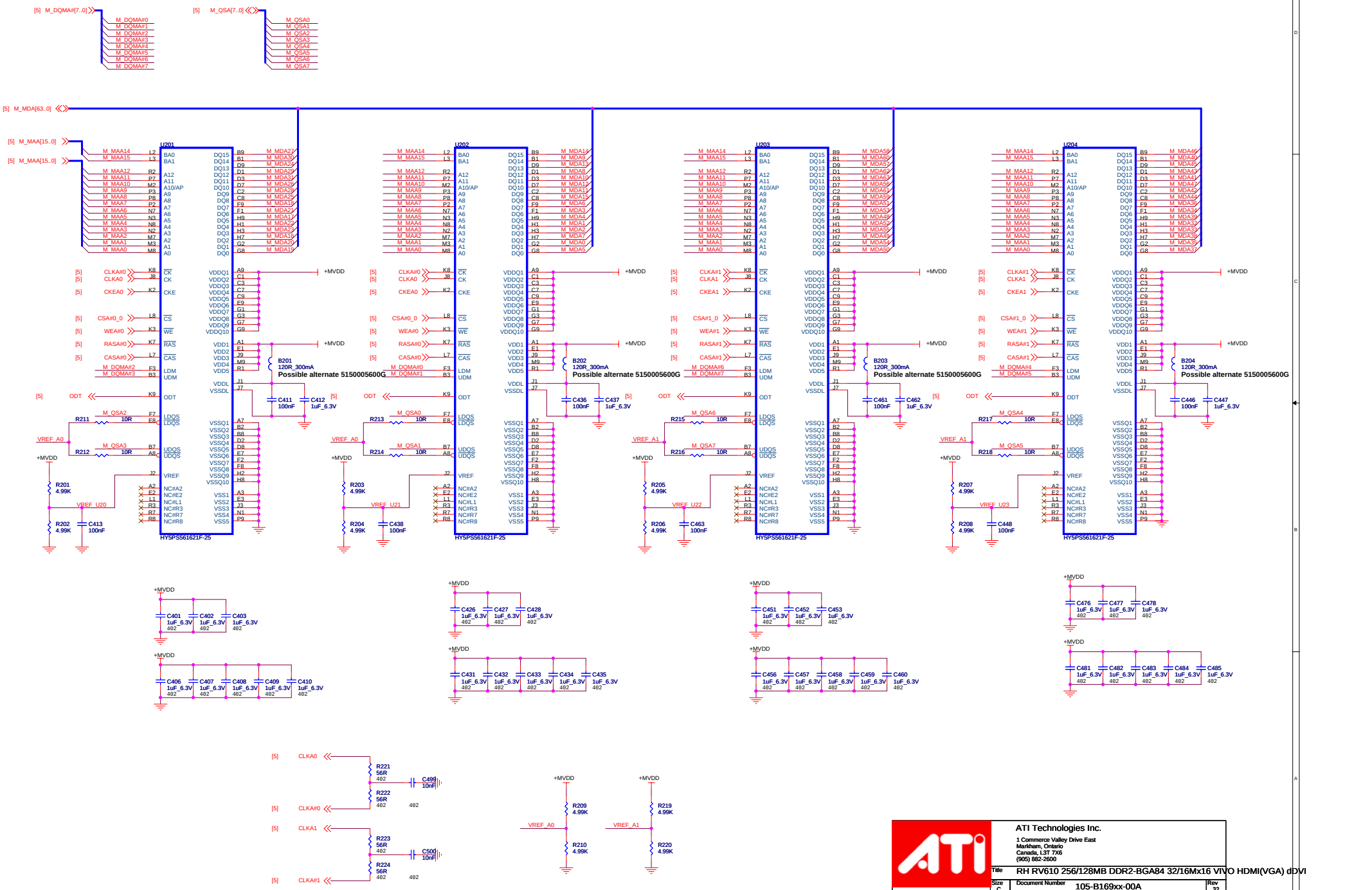
CHANNEL A: RANK 0 128MB DDR2



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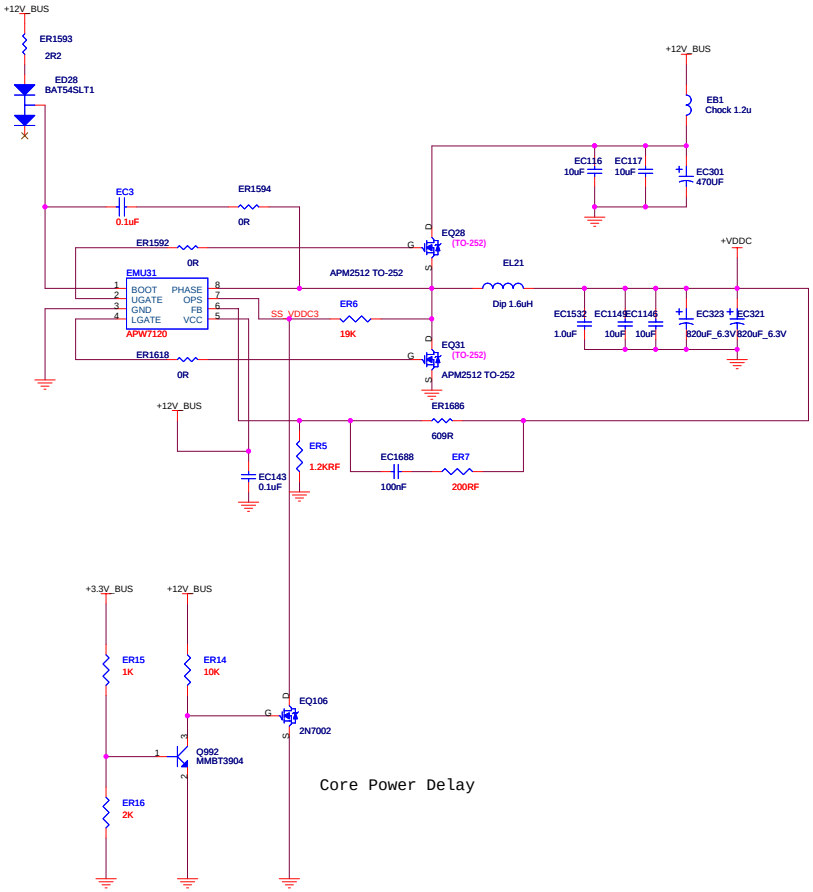
CORE REGULATOR +VDDC



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Title	TR RV630 - MVDD SMPS02	
Size: Custom	Document Number: 105-DB047-00A	Rev: 7
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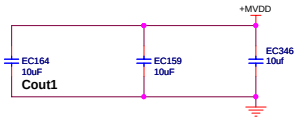

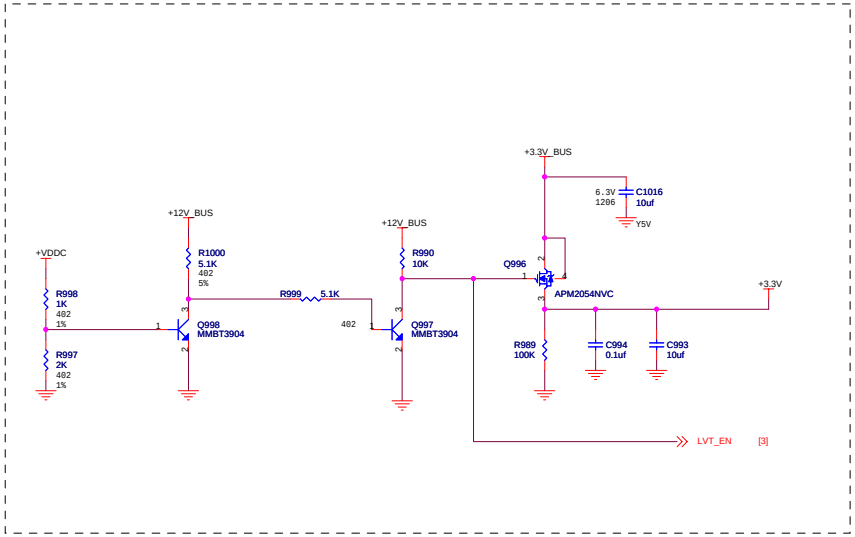

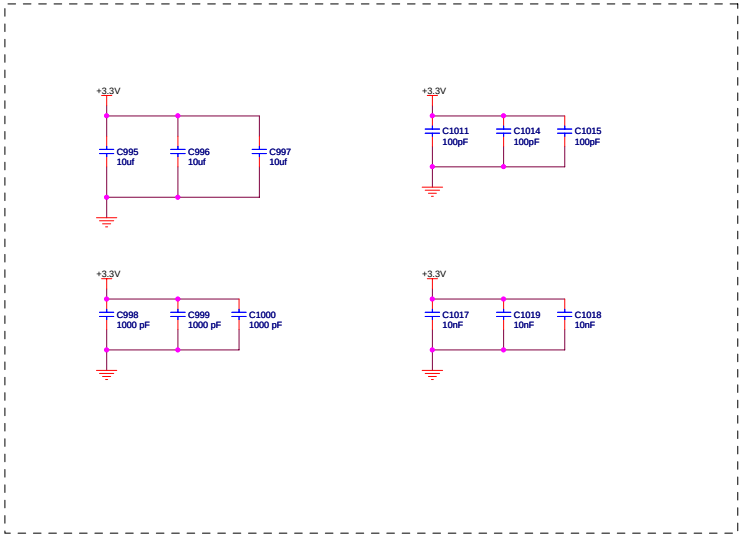

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Title	TR RV630 - MVDD SMPS02	
Size: Custom	Document Number: 105-DB047-00A	Rev: 7
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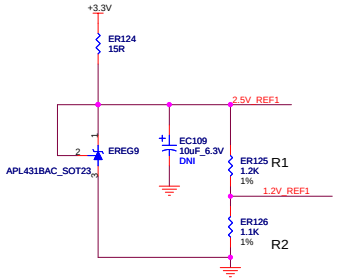
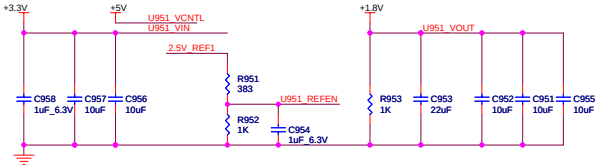
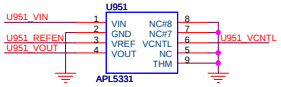
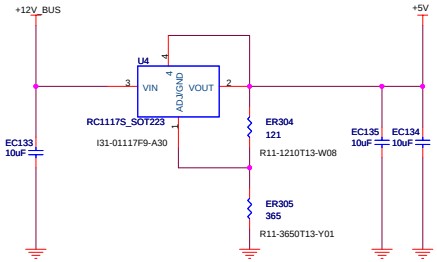
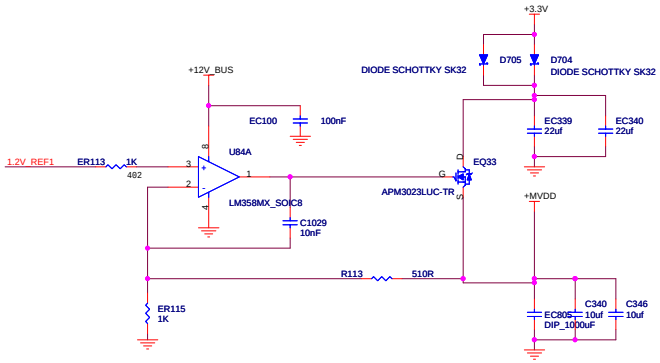




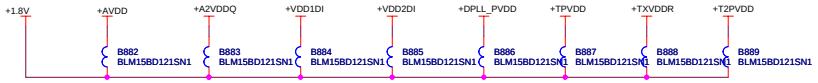




Vout=1.25V* [1+(ER305/ER304)]



Shared Power Rails



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PIN BASED STRAPS

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground High logic voltage

Signal

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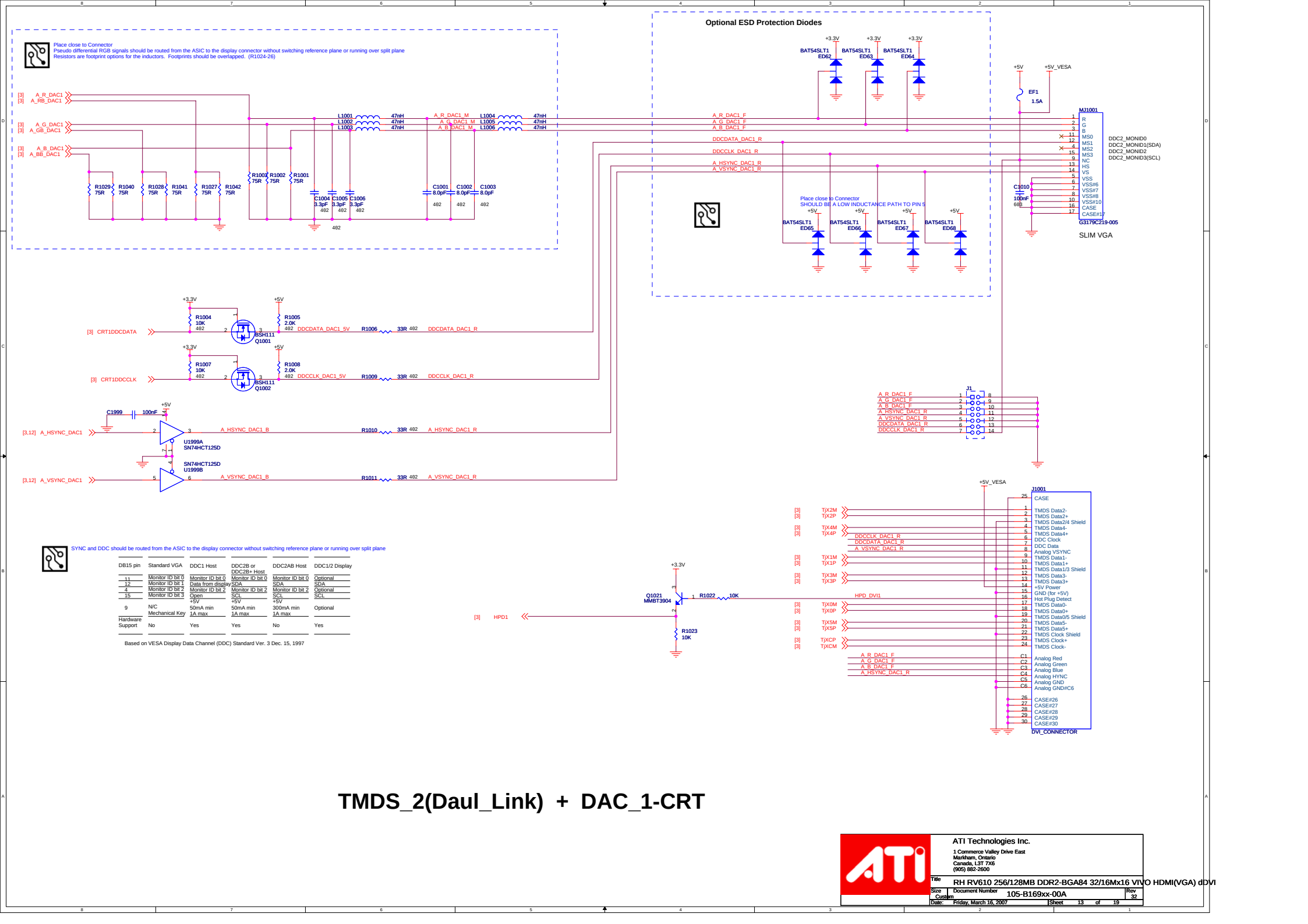

TMDS_2(Daul_Link) + DAC_1-CRT

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TMDS_1(Single_Link) + DAC_2-CRT

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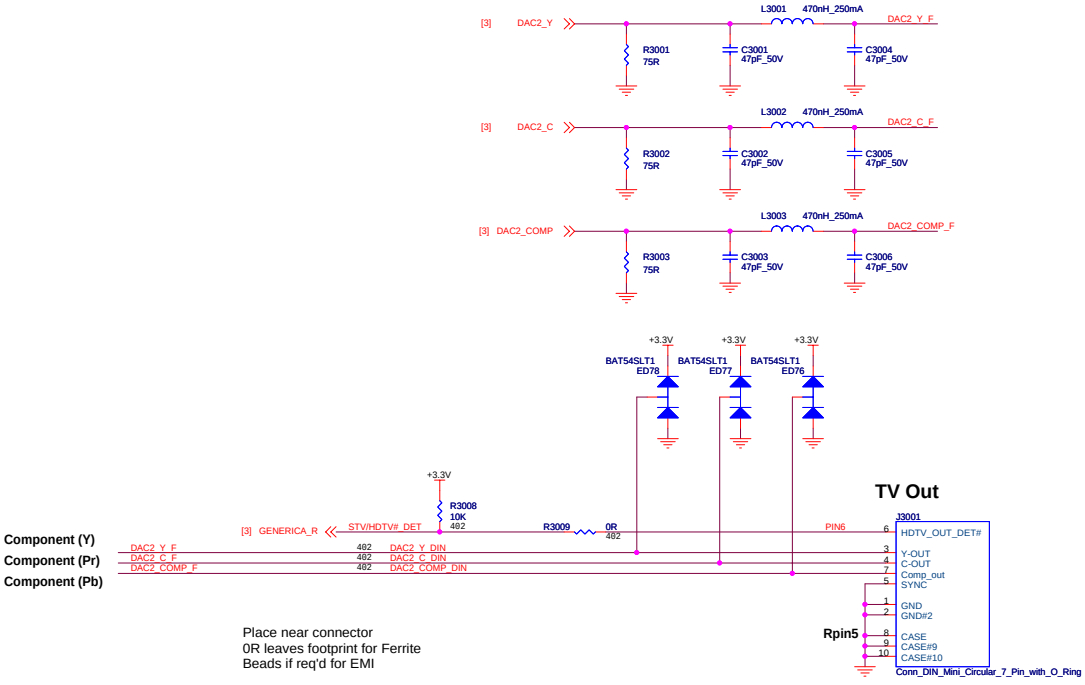

Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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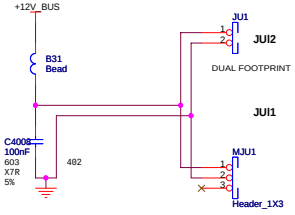

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DVI/VGA SCREWS

ASSY1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY3
BRACKET
8020040100G

80200439A0G (DVI+HDMI+DIN)

FM1
SW_FB

FM2
SW_FB

FM3
SW_FB

FM4
SW_FB

FM5
SW_FB

FM6
SW_FB

<Variant Name>

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<Variant Name>

Title

RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VG105 BM)

Schematic No. 113-B109xx-00A

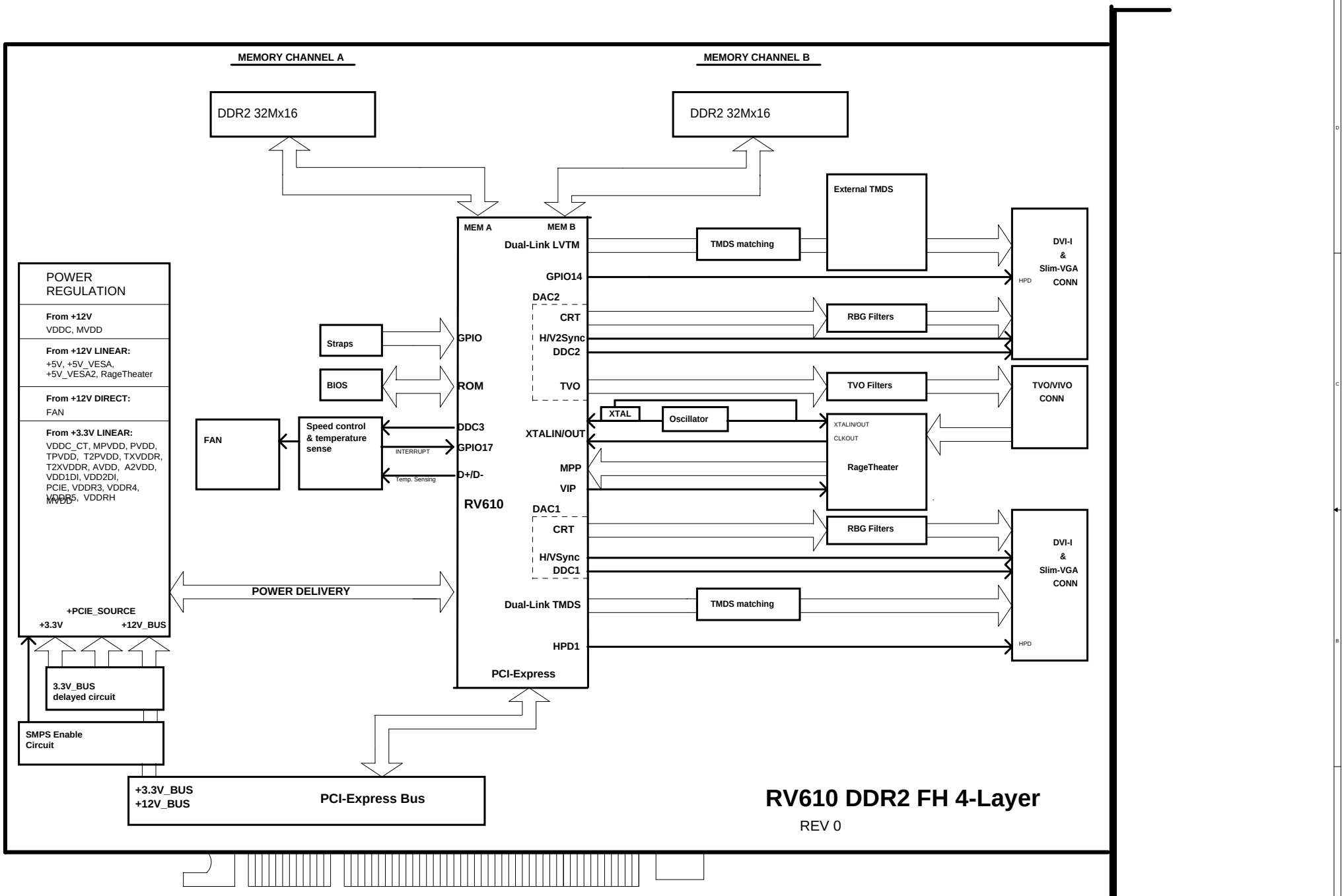
Date: Friday, March 16, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact ATI representative to obtain latest BOM closest to the application desired.**

Rev 32

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
		2006.12.01	UPDATE SCHEM. BOM MANAGEMENT.
		2006.12.14	UPDATE SCHEMATIC TO NETLIST WITH NO ERRORS
		2006.12.18	DORINA UPDATE MEM SWAP
		2006.12.19	REMOVE TP ON MEM - TO BE REPLCED BY 0.8MM PADS ON ALL LINES
		2006.12.20	CHANGED B67 to PN 5260014800G AND C76 to PN 4172010500G
0	00A	2006.12.21	J2 REMOVED
		2007.01.15	NC626 removed (VDDC output cap). LDO output resistor (R879, R880) moved closer to LDO. MVDD LDO input resistors changed to 1R. Debug header changed to include Gen1/2 switch. HDMI caps removed. Added thermal shutdown option to power sequencing.
		2007.01.16	REMOVE BACK BIAS, REMOVE MC624
		2007.01.17	REMOVE R5515, R5516, R5521, R5524 REMOVE R94
		2007.01.22	ADDED H3, H4, H5
		2007.01.22	DECAP CHANGES ON PAGE 3
		2007.01.23	HEATSINK GROUNDING ADJUSTED
		2007.01.23	DORINA - HEATSINK GNDING PINS ADJUSTED
		2007.01.24	RM JTAG + SMA CLOCK CONNECTIONS TO EASE LAYOUT CONGESTION
		2007.01.24	ADDED C300, C301, C302 (STITCHING CAPS) TO IMPROVE DDC LINES
		2007.01.24	FIXED ORCAD NETLIST PROBLEM; NO EFFECTIVE CHANGE.
		2007.01.24	ADD Q102 TO SOLVE A11 VDDR3 LEAKAGE PROBLEM.
1	00B	2007.01.25	CHNG REF DES OF VDDR3 LEAKAGE BLOCK TO Q/R-90
2	00C	2007.02.09	PCB mechanical updates only. No Schematic changes.



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