GA104-200 GPU

New Product Notice

NPN-10039-001_v01 | July 2020
NVIDIA CONFIDENTIAL | Prepared and Provided Under NDA

Document History

NPN-10039-001_v01

Version	Date	Authors	Description of Change
01	July 28, 2020	QL, DR	Initial release

New Product Notice

New Product Introduction

This NPN specifies the following new NVIDIA® GA104-200 GPU. This GPU is offered in the GB5-256 (2714-ball BGA, 40 mm × 40 mm) package only.

Notification	September, 2020	Planned Implementation	Per schedules below

Product Information

These new products represent the Performance consumer desktop GPU segment. They are based on the new NVIDIA Ampere graphics architecture and will be manufactured using qualified suppliers per our approved suppliers' list and are RoHS and Halogen-free compliant.

Key Specifications

	GA104-200
Product Part Number	GA104-200-A1
NVIDIA Part Number (used on labels of packaging materials)	GA104-200-A1
Device ID	0x2486
Memory Interface	256-bit GDDR6
Package	GB5-256

Impact of Change and Recommended Action

NVIDIA is committed to providing our customers with quality products that push the edge of technology and at the same time enable product segmentation. To help guarantee a rapid time-to-market launch and smooth and uninterrupted product supply, NVIDIA strongly recommends that customers qualify these GPUs as soon as possible.

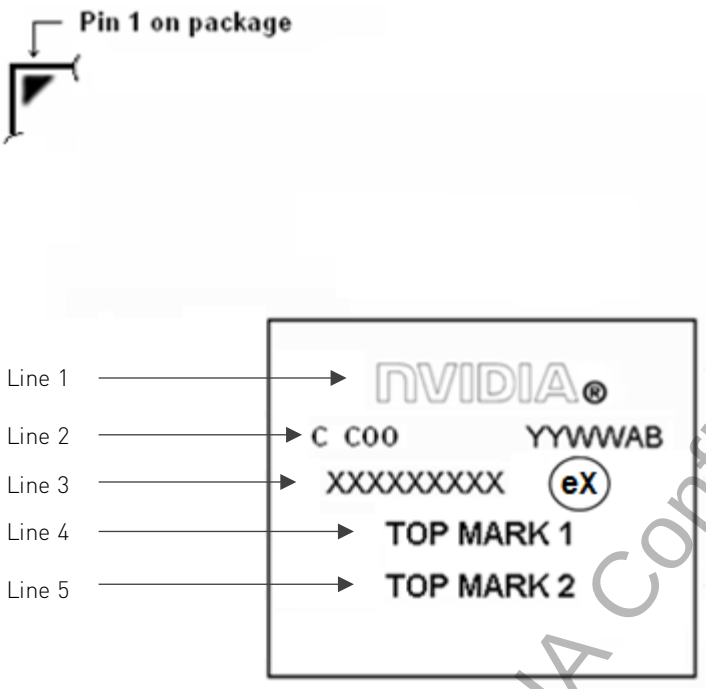
Forecasted Key Milestones

GA104-200-A1: QS ..... September 3, 2020

GA104-200-A1: Production ..... October, 2020

Product Marking and Traceability

GA104-200 **Markings**



Pin 1: Location of Pin 1 in upper left when reading the marking.

Line 1: Company Name

Line 2: Assembly information: plant identifier (C) and country of origin (COO):
- C = Plant identifier: A (ASE), B (Amkor K5), K (Amkor K4), R (ATT - Amkor Tech), S (SPIL), T (TSMC).
- COO = Country of origin: Taiwan for ASE, ATT, SPIL and TSMC, and Korea for Amkor K4 and Amkor K5.
- YYWW = Assembly date code
- AB = Mask revision

Line 3: Assembly lot number (XXXXXXXXX). The first character identifies the wafer Fab location:
Fab 1 = SNxxxxxx
Fab 2 = SAxxxxxx

Line 4: Product Part Number, for example: XXXXX-XX-XX

Line 5: Sample level, if applicable

Products Affected/Ordering Codes

Product	Marketing Part Number for P.O.	NVIDIA Part Number[1]	Comments
GA104-200	GA104-200 -A1	GA104-200-A1	GB5-256 (2714-ball BGA, 40 mm × 40 mm)

Note:

1. The NVIDIA Part Number is provided in this document as a reference product shipping and handling at factory. This is NVIDIA confidential.

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GeForce GA104
Graphics Processing Unit

Data Sheet

DS-10059-001_v01 | July 2020
NVIDIA CONFIDENTIAL | Prepared and Provided Under NDA

Document History

DS-10059-001_v01

Version	Date	Authors	Description of Change
01	July 30, 2020	SH, DR	Initial Release

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Introduction

Overview

This data sheet covers NVIDIA® Graphics Processing Unit for products listed in the title page, bringing a new level of performance and capability to visual graphics and computing applications. These GPUs support 256-bit frame buffer and 16 lanes of PCI Express GEN 4.0 interfaces.

Supported Technologies

- Direct3D 12 Ultimate and Shader Model 7.0
- OpenGL 4.6
- Vulkan 1.2
- NVIDIA® CUDA technology

Signal Descriptions

Overview

The signal description section contains definitions grouped under the following functions:

- "Conventions"
- "PCI Express Interface"
- "Frame Buffer Memory Interface"
- "ROM Access Signals"
- "I2C Interface"
- "Clock Reference Signals"
- "Digital Display Interface"
- "Power Rail Signals"

Note: Refer to Hardware Design Guide DG-09846-001 for detailed functionality and usage.

Conventions

- The following conventions are used to describe the signals for this GPU:
- Signal names listed in the ballout are written in bold sans serif font to distinguish them from other text. Single-ended active low signals are identified by an underscore and the letter "n" (_N) after the signal. For example, PEX_TX1_N indicates an active low signal. Signal names that do not appear in the ballout, but that are used for alternate interfaces are written in sans serif font without bold.
- A full list of signals and their operational characteristics referred to as I/O state codes are provided in "GPU Signal List".

PCI Express Interface

Table 2.1 PCI Express Interface

Signal	Description
PEX_RX[15:0] PEX_RX[15:0]_N	PCI Express Receive Data Bus This is the high-speed unidirectional differential input data bus. The raw data transfer rate is: 2.5 GTs per differential pair for PCI Express 1.1, 5.0 GTs for PCI Express 2.0, 8.0 GTs for PCI Express 3.0, and 16.0 GTs for PCI Express 4.0, including the symbol overhead for an embedded clock.
PEX_TX[15:0] PEX_TX[15:0]_N	PCI Express Transmit Data Bus This is the high-speed unidirectional differential output data bus. The raw data transfer rate is: 2.5 GTs per differential pair for PCI Express 1.1, 5.0 GTs for PCI Express 2.0, 8.0 GTs for PCI Express 3.0, and 16.0 GTs for PCI Express 4.0, including the symbol overhead for an embedded clock.
PEX_REFCLK PEX_REFCLK_N	PCI Express Reference Clock The reference clock is a differential low-jitter input the GPU uses for its internal timing purposes. This input clock may be spread spectrum. Refer to the latest PCI Express specification for details on the reference clock spread spectrum.
PEX_RST_N	PCI Express Reset The PEX_RST_N signal indicates when the power supply is within its specified voltage tolerance and is stable. It goes inactive after a delay time from the power rails, achieving specified tolerance and power up. Refer to the latest PCI Express specification for details on the PCI Express reset.
PEX_TERMP	PCI Express Input/Output Termination Calibration The PEX_TERMP signal provides the reference for the internal calibation of the PCI Express input/output termination. Use a pull-down to GND that is the same value as the desired termination.
PEX_CLKREQ_N	PCI Express Clock Request This active low signal is driven to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data.
PEX_WAKE_N	PCI Express Wake Request This active low signal is driven to request that the PCI Express interfaces wakes up from a lower power state

Frame Buffer Memory Interface

This GPU frame buffer memory interface supports GDDR6 memories. Each memory partition has its own set of command signals. Refer to the Hardware Design Guide to see how the frame buffer control signals map to the memory command signals.

Table 2.2 Frame Buffer Interface

Signal	Description
FBx_CMD[55:0] (x = A,B,C,D)	Command Address Bus Inversion (CABI_n) Used to reduce power consumption on the command Address bus.
	Reset (RESET_n) Asynchronous DRAM reset signal
	Memory Clock Enable (CKE_n) Enables the clock receivers for the target RAM.
	Command Address Inputs (CA[9:0]): The CA outputs receive DDR Command and Address inputs
FBx_CLK[1:0] FBx_CLK[1:0]_N (x=A,B,C,D)	Memory Clock Signals These are separate sets of clock signals for eachmemory partition. For a further reduction in loading, there are two sets of clocks per partition. Each partition has two clock pairs that control either the most significant 32 bits or the least significant 32 bits per partition. The active low CA signals switch on the falling clock edge. The active high CA signals switch on the rising clock edge. The memory clock signals are as follows: FBx_CLK0 and FBx_CLK0_N → FBx_D[31:0] FBx_CLK1 and FBx_CLK1_N → FBx_D[63:32] x= A,B,C,D.
FBx_D[63:0] (x=A,B,C,D)	Memory Data Bus These signals connect to data signals of the memory device for each 64-bit partition.
FBx_DQM[7:0] (x=A,B,C,D)	Data Bus Inversion (DBI) FBx_DQM[7:0] signals are connected to DBI[7:0] signals of the memory. Used to reduce power consumption and VDD noise of the DRAM.
FBx_DQS_WP[7:0] (x=A,B,C,D)	Error Detection Code (EDC) FBx_DQS_WP[7:0] signals are connected to the EDC[7:0] signals of the memory. The CRC data is communicated on these signals

Table 2.2 Frame Buffer Interface (Continued)

Signal	Description
FBx_WCK01 FBx_WCK01_N FBx_WCK23 FBx_WCK23_N FBx_WCK45 FBx_WCK45_N FBx_WCK67 FBx_WCK67_N (x=A,B,C,D) FBx_WCKB01 FBx_WCKB01_N FBx_WCKB23 FBx_WCKB23_N FBx_WCKB45 FBx_WCKB45_N FBx_WCKB67 FBx_WCKB67_N (x=A,B,C,D)	Differential clocks used as the reference for read and write data latching.
FB_CAL_PD_VDDQ FB_CAL_PU_GND	Calibration Pull-Down/Pull-Up When the frame buffer bus operates in high-speed source-synchronous mode, several signals require dynamic calibration. Other slower signals are calibrated once on power-up. FB_CAL_PD_VDDQ and FB_CAL_PU_ GND are used to compute the drive strength of the frame buffer pads. FB_CAL_PD_VDDQ connects to FBVDDQ and is pulled up through a precision resistor. FB_CAL_PU_GND is pulled down to GND through a precision resistor.
FB_CAL_TERM_GND	Termination Calibration Signal When the frame buffer bus operates in high-speed source-synchronous mode, it may use internal termination provided by the GPU. This signal provides the calibration for the internal termination. It should be tied to GND through a precision resistor that is the same value as the desired termination.
FB_VREF	Frame Buffer Voltage Reference Sets switching threshold for inputs on the frame buffer when the frame buffer input pads are set to input mode. This signal also functions as inbound read calibration. Follow design guide for proper connection.
FBVDDQ_SENSE	Frame Buffer Power Rail Sense Signal.

ROM Access Signals

Table 2.3 ROM Access Signals

Signal	Description
ROM_SCLK	Serial ROM Clock ROM_SCLK supplies the clock signal for accessing serial ROM data.
ROM_CS_N	Chip Select.
ROM_SI	Serial Output ROM_SI supplies the data signal to the SROM_SI serial ROM signal.
ROM_SO	Serial Input ROM_SO accepts the data signal input from SROM_SO of the serial ROM as input.

I2C Interface

Table 2.4 I2C Interface Signals

Signal	Description
I2CB_SCL I2CB_SDA	If not used for any external Bus, this bus may be used for embedded devices.
I2CC_SCL I2CC_SDA	Restricted to embedded devices such as voltage regulators and power monitors.
I2CS_SCL I2CS_SDA	Slave I2C-Compatible Bus Signal.

Clock Reference Signals

Table 2.5 Clock Reference Signals

Signal	Description
XTAL_IN XTAL_OUT	A series resonant crystal is connected between these two points to provide the reference clock for the internal clock synthesizers. Alternately, an external LVTTL clock oscillator output may be driven in XTAL_IN, leaving XTAL_OUT unconnected.
XTAL_OUTBUFF	XTAL_OUTBUFF is a buffered version of the XTAL_IN/ XTAL_OUT. Used as a strap to set the fan PWM.
EXT_REFCLK_FL	EXT_REFCLK_FL

Digital Display Interface

This GPU enables Links A, B, C, D, E, and F to support DisplayPort. Links can also be configured to support DVI and HDMI.

Table 2.6 Digital Display Interface Signals, Links A, B, C, D, E, and F

Signal	Description
IFPA_AUX_SCL/ IFPA_AUX_SDA_N	DisplayPort Auxiliary Lane (Link A)
IFPA_L0/IFPA_L0_N	DisplayPort Main Link Lane 0 (Link A)
IFPA_L1/IFPA_L1_N	DisplayPort Main Link Lane 1 (Link A)
IFPA_L2/IFPA_L2_N	DisplayPort Main Link Lane 2 (Link A)
IFPA_L3/IFPA_L3_N	DisplayPort Main Link Lane 3 (Link A)
IFPB_AUX_SCL IFPB_AUX_SDA_N	DisplayPort Auxiliary Lane (Link B)
IFPB_L0/IFPB_L0_N	DisplayPort Main Link Lane 0 (Link B)
IFPB_L1/IFPB_L1_N	DisplayPort Main Link Lane 1 (Link B)
IFPB_L2/IFPB_L2_N	DisplayPort Main Link Lane 2 (Link B)
IFPB_L3/IFPB_L3_N	DisplayPort Main Link Lane 3 (Link B)
IFPAB_RSET	Set Reference Current Generate a reference current through connecting an external resistor to this signal.
IFPC_AUX_SCL / IFPC_AUX_SDA_N	DisplayPort Auxiliary Lane (Link C)
IFPC_L0/IFPC_L0_N	DisplayPort Main Link Lane 0 (Link C)
IFPC_L1/IFPC_L1_N	DisplayPort Main Link Lane 1 (Link C)
IFPC_L2/IFPC_L2_N	DisplayPort Main Link Lane 2 (Link C)
IFPC_L3/IFPC_L3_N	DisplayPort Main Link Lane 3 (Link C)
IFPCD_RSET	Set Reference Current. Generates a reference current through connecting an external resistor to this signal.
IFPD_AUX_SCL/ IFPD_AUX_SDA_N	DisplayPort Auxiliary Lane (Link D)
IFPD_L0/IFPD_L0_N	DisplayPort Main Link Lane 0 (Link D)
IFPD_L1/IFPD_L1_N	DisplayPort Main Link Lane 1 (Link D)
IFPD_L2/IFPD_L2_N	DisplayPort Main Link Lane 2 (Link D)
IFPD_L3/IFPD_L3_N	DisplayPort Main Link Lane 3 (Link D)
IFPE_AUX_SCL/ IFPE_AUX_SDA_N	DisplayPort Auxiliary Lane (Link E)
IFPE_L0/IFPE_L0_N	DisplayPort Main Link Lane 0 (Link E)

Table 2.6 Digital Display Interface Signals, Links A, B, C, D, E, and F (Continued)

Signal	Description
IFPE_L1/IFPE_L1_N	DisplayPort Main Link Lane 1 (Link E)
IFPE_L2/IFPE_L2_N	DisplayPort Main Link Lane 2 (Link E)
IFPE_L3/IFPE_L3_N	DisplayPort Main Link Lane 3 (Link E)
IFPEF_RSET	Set Reference Current. Generates a reference current through connecting an external resistor to this signal
IFPF_AUX_SCL/ IFPF_AUX_SDA_N	DisplayPort Auxiliary Lane (Link F)
IFPF_L0/IFPF_L0_N	DisplayPort Main Link Lane 0 (Link F);
IFPF_L1/IFPF_L1_N	DisplayPort Main Link Lane 1 (Link F)
IFPF_L2/IFPF_L2_N	DisplayPort Main Link Lane 2 (Link F)
IFPF_L3/IFPF_L3_N	DisplayPort Main Link Lane 3 (Link F)

Power Rail Signals

IFP Power Rail Signals

Table 2.7 IFP Power Rail Signals

Signal	Description
IFP_IOVDD	0.95V supply for integrated Digital Display I/O Power Rails for all IFP links.
IFPAB_PLLVDD	1.8V supply for integrated Digital Display PLL Power Rails for the IFP-A and IFP-B links.
IFPCD_PLLVDD	1.8V supply for Integrated Digital Display PLL Power Rails for the IFP-C and IFP-D links.
IFPEF_PLLVDD	1.8V supply for Integrated Digital Display PLL Power Rails for the IFP-E link.

PEX Power Rail Signals

Table 2.8 PEX Power Rail Signals

Signal	Description
PEX_CVDD / PEX_DVDD	0.95V supply for PCIe interface/PLL digital power rail
PEX_CVDD_SENSE	PCIe 0.95V power supply rail sense signal
PEX_HVDD	1.8V supply for PCIe interface/PLL analog power rail
PEX_PLL_HVDD	1.8V supply for the PEX PLL

Frame Buffer Power Rail Signals

Table 2.9 Frame Buffer Power Rail Signals

Signal	Description
FB_PLLVDD	1.8V supply for Frame Buffer Digital Power Rails
FBVDDQ	Frame Buffer Power Rail
FBVDDQ_SENSE	Frame Buffer Power Rail Sense Signal

General Power Rail Signals

Table 2.10 General Power Rail Signals

Signal	Description
1V8	1.8V Power Rail
CORE_PLL_AVDD	Core PLL Analog Power Rail
GPCADC_AVDD	1.8V supply for Analog Power Rails for GPCs
SP_PLLVDD	1.8V supply for Core Clock PLL Analog Power Rail
VDD	Core Power Rail. Connect to NVVDD power supply
VDD_SENSE	Core Power NVVDD rail sense signal
VDDMS	Core Power Rail for NVVDD/MSVDD power rail
VDDMS_SENSE	Core Power sense signal for NVVDD/MSVDD
VID_PLLVDD	1.8V supply for Video Pixel Clock PLL Analog power rail

Test Signals

Table 2.11 Test Signals

Signal	Description
JTAG_TCK JTAG_TDI JTAG_TDO JTAG_TMS	JTAG test signals
NVJTAG_SEL	JTAG select

Miscellaneous Signals

Table 2.12 Miscellaneous Signals

Signal	Description
STRAP[5:0]	Strap signals
THERMDP THERMDN	Thermal Monitor Signals Leave floating and unconnected.
ADC_IN / ADC_IN_N	External current sense for power monitoring
GPIO [35:0]	General Purpose I/O

Electrical Specifications

This section provides absolute maximum ratings, operating conditions and GPIO electrical specifications for GPU products covered by this data sheet.

For more information about the core graphics voltage, frame buffer clock frequency, and core clock frequency values and electrical and thermal design guidelines for these products, refer to the SKU specific Electrical and Thermal Design Guidelines.

Table 3.1 Power Rail Operating Range and Absolute Max Limits

Power Rail	Description of Power Rail	Operating Conditions range			Absolute Max Ratings	
		Min (V)	Typ (V)	Max (V)[1]	Min (V)	Max (V)[2]
1V8	1.8 V power	1.692	1.8	1.908	-0.3	1.98
CORE_PLL_AVDD	Core PLL Analog	1.692	1.8	1.908	-0.3	1.98
FB_PLLVDD	Frame buffer PLL analog	1.692	1.8	1.908	-0.3	1.98
FBVDDQ[3]	Frame buffer power	1.08	1.35	1.485	-0.3	1.485
GPCADC_AVDD	Core PLL Analog	1.692	1.8	1.908	-0.3	1.98
IFP_IOVDD	Integrated Digital Display I/O power	0.9	0.95	1	-0.3	1.05
IFPAB_PLLVDD	Integrated Digital Display PLL power	1.692	1.8	1.908	-0.3	1.98
IFPCD_PLLVDD	Integrated Digital Display PLL power	1.692	1.8	1.908	-0.3	1.98
IFPEF_PLLVDD	Integrated Digital Display PLL power	1.692	1.8	1.908	-0.3	1.98
PEX_CVDD	PCIe interface/PLL digital power	0.9	0.95	1	-0.3	1.05
PEX_DVDD	PCIe interface/PLL digital power	0.9	0.95	1	-0.3	1.05
PEX_HVDD	PCIe interface/PLL analog power	1.692	1.8	1.908	-0.3	1.98
PEX_PLL_HVDD	PCIe interface PLL supply power	1.692	1.8	1.908	-0.3	1.98
SP_PLLVDD	Core clock PLL analog power	1.692	1.8	1.908	-0.3	1.98
VDD	Core power (NVVDD)	-2.5%	NVVDD[4]	+2.5%	-0.3	1.2
VDDMS	Core power (NVVDD/MSVDD)	-2.5%	NVVDD[4]	+2.5%	-0.3	1.2
VID_PLLVDD	Thermal controller/Pixel CLK PLL power	1.692	1.8	1.908	-0.3	1.98

[1]This specification defines the goals for the DC supply at VDD. Short pulses due to switching noise on VDD may exceed this limit.

[2]Stress greater than those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[3] Min/Typ/Max/ should meet memory vendor specification.

[4]NVVDD power rail voltage varies during normal operation of the GPU, this range can be found in the SKU specific Electrical and Thermal Design Guidelines.

Table 3.2 GPIO Electrical Specifications

Voh,Vih/min	Voh,Vih/max	Vol,Vil/min	Vol,Vil/max	Vi_mid max	Vi_mid min
1.50V	1.854V	0V	0.3V	0.3V	1.3V

GPU Signal List

This section contains the GPU signal list with I/O function and ball number for reference to location on the Ball Map. Refer to section "Ball Map" for more information.

Table 4.1 GPU Signal List I/O Key

B = Bidirectional signal
I = Input signal
O = Output signal
P = Power-related signal
Z= Tri-state output
AI = Analog input signal
AO = Analog output signal
NC = No Connect
RSVD = Reserved

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
1V8	BF10	P	+1.8V
1V8	BF11	P	+1.8V
1V8	BG10	P	+1.8V
1V8	BG11	P	+1.8V
ADC_IN	BP10	AI	-
ADC_IN_N	BR10	AI	-
CORE_PLL_AVDD	BF25	P	-
EXT_REFCLK_FL	BK8	I	+1.8V
FB_CAL_PD_VDDQ	W47	AI	FBVDDQ
FB_CAL_PU_GND	Y47	AI	FBVDDQ
FB_CAL_TERM_GND	W48	AI	FBVDDQ
FB_PLLVDD	AC46	P	-
FB_PLLVDD	AE11	P	-
FB_PLLVDD	AP46	P	-
FB_PLLVDD	L17	P	-
FB_PLLVDD	L35	P	-
FB_PLLVDD	T46	P	-
FB_VREF	W49	AI	FBVDDQ
FBA_CLK0	AP48	O	FBVDDQ
FBA_CLK0_N	AP47	O	FBVDDQ
FBA_CLK1	AR48	O	FBVDDQ
FBA_CLK1_N	AR47	O	FBVDDQ
FBA_CMD0	Y53	O	FBVDDQ
FBA_CMD1	AA56	O	FBVDDQ
FBA_CMD10	AF53	O	FBVDDQ
FBA_CMD11	AG56	O	FBVDDQ
FBA_CMD12	AH55	O	FBVDDQ
FBA_CMD13	AH56	O	FBVDDQ
FBA_CMD14	AJ56	O	FBVDDQ
FBA_CMD15	AJ53	O	FBVDDQ
FBA_CMD16	AK56	O	FBVDDQ
FBA_CMD17	AL55	O	FBVDDQ
FBA_CMD18	AL56	O	FBVDDQ
FBA_CMD19	AM56	O	FBVDDQ
FBA_CMD2	AB55	O	FBVDDQ
FBA_CMD20	AM53	O	FBVDDQ
FBA_CMD21	AN56	O	FBVDDQ
FBA_CMD22	AP55	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBA_CMD23	AP56	O	FBVDDQ
FBA_CMD24	AR56	O	FBVDDQ
FBA_CMD25_NC	AR53	NC	-
FBA_CMD26_NC	AT56	NC	-
FBA_CMD27	AR55	O	FBVDDQ
FBA_CMD28	BM56	O	FBVDDQ
FBA_CMD29	BM55	O	FBVDDQ
FBA_CMD3	AB56	O	FBVDDQ
FBA_CMD30	BL56	O	FBVDDQ
FBA_CMD31	BK55	O	FBVDDQ
FBA_CMD32	BK56	O	FBVDDQ
FBA_CMD33	BJ56	O	FBVDDQ
FBA_CMD34	BJ55	O	FBVDDQ
FBA_CMD35	BH56	O	FBVDDQ
FBA_CMD36	BG53	O	FBVDDQ
FBA_CMD37	BG56	O	FBVDDQ
FBA_CMD38	BF56	O	FBVDDQ
FBA_CMD39	BF55	O	FBVDDQ
FBA_CMD4	AC56	O	FBVDDQ
FBA_CMD40	BE56	O	FBVDDQ
FBA_CMD41	BD53	O	FBVDDQ
FBA_CMD42	BD56	O	FBVDDQ
FBA_CMD43	BC56	O	FBVDDQ
FBA_CMD44	BC55	O	FBVDDQ
FBA_CMD45	BB56	O	FBVDDQ
FBA_CMD46	BA53	O	FBVDDQ
FBA_CMD47	BA56	O	FBVDDQ
FBA_CMD48	AY56	O	FBVDDQ
FBA_CMD49	AY55	O	FBVDDQ
FBA_CMD5	AC53	O	FBVDDQ
FBA_CMD50	AW56	O	FBVDDQ
FBA_CMD51	AV53	O	FBVDDQ
FBA_CMD52	AV56	O	FBVDDQ
FBA_CMD53_NC	AU56	NC	-
FBA_CMD54_NC	AU55	NC	-
FBA_CMD55	AV55	O	FBVDDQ
FBA_CMD6	AD56	O	FBVDDQ
FBA_CMD7	AE55	O	FBVDDQ
FBA_CMD8	AE56	O	FBVDDQ
FBA_CMD9	AF56	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBA_D0	AC51	B	FBVDDQ
FBA_D1	AB48	B	FBVDDQ
FBA_D10	W53	B	FBVDDQ
FBA_D11	Y54	B	FBVDDQ
FBA_D12	Y52	B	FBVDDQ
FBA_D13	Y51	B	FBVDDQ
FBA_D14	Y49	B	FBVDDQ
FBA_D15	AB51	B	FBVDDQ
FBA_D16	AM54	B	FBVDDQ
FBA_D17	AL51	B	FBVDDQ
FBA_D18	AM52	B	FBVDDQ
FBA_D19	AJ54	B	FBVDDQ
FBA_D2	AC52	B	FBVDDQ
FBA_D20	AM47	B	FBVDDQ
FBA_D21	AM51	B	FBVDDQ
FBA_D22	AP50	B	FBVDDQ
FBA_D23	AM49	B	FBVDDQ
FBA_D24	AF54	B	FBVDDQ
FBA_D25	AF49	B	FBVDDQ
FBA_D26	AH51	B	FBVDDQ
FBA_D27	AF47	B	FBVDDQ
FBA_D28	AJ52	B	FBVDDQ
FBA_D29	AJ51	B	FBVDDQ
FBA_D3	AC49	B	FBVDDQ
FBA_D30	AH48	B	FBVDDQ
FBA_D31	AJ49	B	FBVDDQ
FBA_D32	BA49	B	FBVDDQ
FBA_D33	BD47	B	FBVDDQ
FBA_D34	BD54	B	FBVDDQ
FBA_D35	BD52	B	FBVDDQ
FBA_D36	BC51	B	FBVDDQ
FBA_D37	BD51	B	FBVDDQ
FBA_D38	BF51	B	FBVDDQ
FBA_D39	BD49	B	FBVDDQ
FBA_D4	AF52	B	FBVDDQ
FBA_D40	BG52	B	FBVDDQ
FBA_D41	BG51	B	FBVDDQ
FBA_D42	BG54	B	FBVDDQ
FBA_D43	BF49	B	FBVDDQ
FBA_D44	BJ54	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBA_D45	BG50	B	FBVDDQ
FBA_D46	BJ52	B	FBVDDQ
FBA_D47	BK53	B	FBVDDQ
FBA_D48	AP51	B	FBVDDQ
FBA_D49	AP53	B	FBVDDQ
FBA_D5	AC54	B	FBVDDQ
FBA_D50	AR52	B	FBVDDQ
FBA_D51	AR54	B	FBVDDQ
FBA_D52	AU51	B	FBVDDQ
FBA_D53	AR51	B	FBVDDQ
FBA_D54	AV51	B	FBVDDQ
FBA_D55	AR49	B	FBVDDQ
FBA_D56	AV49	B	FBVDDQ
FBA_D57	AV54	B	FBVDDQ
FBA_D58	AY51	B	FBVDDQ
FBA_D59	AV52	B	FBVDDQ
FBA_D6	AE51	B	FBVDDQ
FBA_D60	AY48	B	FBVDDQ
FBA_D61	BA54	B	FBVDDQ
FBA_D62	BA52	B	FBVDDQ
FBA_D63	BA51	B	FBVDDQ
FBA_D7	AF51	B	FBVDDQ
FBA_D8	W51	B	FBVDDQ
FBA_D9	W50	B	FBVDDQ
FBA_DQM0	AE50	B	FBVDDQ
FBA_DQM1	AB50	B	FBVDDQ
FBA_DQM2	AL50	B	FBVDDQ
FBA_DQM3	AH50	B	FBVDDQ
FBA_DQM4	BC50	B	FBVDDQ
FBA_DQM5	BF50	B	FBVDDQ
FBA_DQM6	AU50	B	FBVDDQ
FBA_DQM7	AY50	B	FBVDDQ
FBA_DQS_WP0	AE53	I	FBVDDQ
FBA_DQS_WP1	AB53	I	FBVDDQ
FBA_DQS_WP2	AL53	I	FBVDDQ
FBA_DQS_WP3	AH53	I	FBVDDQ
FBA_DQS_WP4	BC53	I	FBVDDQ
FBA_DQS_WP5	BF53	I	FBVDDQ
FBA_DQS_WP6	AU53	I	FBVDDQ
FBA_DQS_WP7	AY53	I	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBA_WCK01	AE48	O	FBVDDQ
FBA_WCK01_N	AE47	O	FBVDDQ
FBA_WCK23	AL48	O	FBVDDQ
FBA_WCK23_N	AL47	O	FBVDDQ
FBA_WCK45	BA47	O	FBVDDQ
FBA_WCK45_N	BA48	O	FBVDDQ
FBA_WCK67	AU48	O	FBVDDQ
FBA_WCK67_N	AU47	O	FBVDDQ
FBA_WCKB01	AC48	O	FBVDDQ
FBA_WCKB01_N	AC47	O	FBVDDQ
FBA_WCKB23	AJ48	O	FBVDDQ
FBA_WCKB23_N	AJ47	O	FBVDDQ
FBA_WCKB45	BC48	O	FBVDDQ
FBA_WCKB45_N	BC47	O	FBVDDQ
FBA_WCKB67	AV48	O	FBVDDQ
FBA_WCKB67_N	AV47	O	FBVDDQ
FBB_CLK0	K44	O	FBVDDQ
FBB_CLK0_N	J44	O	FBVDDQ
FBB_CLK1	J46	O	FBVDDQ
FBB_CLK1_N	K46	O	FBVDDQ
FBB_CMD0	B37	O	FBVDDQ
FBB_CMD1	A37	O	FBVDDQ
FBB_CMD10	B43	O	FBVDDQ
FBB_CMD11	A43	O	FBVDDQ
FBB_CMD12	A44	O	FBVDDQ
FBB_CMD13	D44	O	FBVDDQ
FBB_CMD14	A45	O	FBVDDQ
FBB_CMD15	B46	O	FBVDDQ
FBB_CMD16	A46	O	FBVDDQ
FBB_CMD17	A47	O	FBVDDQ
FBB_CMD18	D47	O	FBVDDQ
FBB_CMD19	A48	O	FBVDDQ
FBB_CMD2	A38	O	FBVDDQ
FBB_CMD20	B49	O	FBVDDQ
FBB_CMD21	A49	O	FBVDDQ
FBB_CMD22	B50	O	FBVDDQ
FBB_CMD23	A50	O	FBVDDQ
FBB_CMD24	C50	O	FBVDDQ
FBB_CMD25_NC	A51	NC	-
FBB_CMD26_NC	B52	NC	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBB_CMD27	C52	O	FBVDDQ
FBB_CMD28	Y56	O	FBVDDQ
FBB_CMD29	W56	O	FBVDDQ
FBB_CMD3	D38	O	FBVDDQ
FBB_CMD30	W55	O	FBVDDQ
FBB_CMD31	V56	O	FBVDDQ
FBB_CMD32	U53	O	FBVDDQ
FBB_CMD33	U56	O	FBVDDQ
FBB_CMD34	T56	O	FBVDDQ
FBB_CMD35	T55	O	FBVDDQ
FBB_CMD36	R56	O	FBVDDQ
FBB_CMD37	P53	O	FBVDDQ
FBB_CMD38	P56	O	FBVDDQ
FBB_CMD39	N56	O	FBVDDQ
FBB_CMD4	A39	O	FBVDDQ
FBB_CMD40	N55	O	FBVDDQ
FBB_CMD41	M56	O	FBVDDQ
FBB_CMD42	L53	O	FBVDDQ
FBB_CMD43	L56	O	FBVDDQ
FBB_CMD44	K56	O	FBVDDQ
FBB_CMD45	K55	O	FBVDDQ
FBB_CMD46	J56	O	FBVDDQ
FBB_CMD47	H53	O	FBVDDQ
FBB_CMD48	H56	O	FBVDDQ
FBB_CMD49	G56	O	FBVDDQ
FBB_CMD5	B40	O	FBVDDQ
FBB_CMD50	G55	O	FBVDDQ
FBB_CMD51	E56	O	FBVDDQ
FBB_CMD52	B54	O	FBVDDQ
FBB_CMD53_NC	B53	NC	-
FBB_CMD54_NC	A52	NC	-
FBB_CMD55	E55	O	FBVDDQ
FBB_CMD6	A40	O	FBVDDQ
FBB_CMD7	A41	O	FBVDDQ
FBB_CMD8	D41	O	FBVDDQ
FBB_CMD9	A42	O	FBVDDQ
FBB_D0	D37	B	FBVDDQ
FBB_D1	J37	B	FBVDDQ
FBB_D10	D34	B	FBVDDQ
FBB_D11	G34	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBB_D12	E35	B	FBVDDQ
FBB_D13	K34	B	FBVDDQ
FBB_D14	H35	B	FBVDDQ
FBB_D15	K35	B	FBVDDQ
FBB_D16	G47	B	FBVDDQ
FBB_D17	E44	B	FBVDDQ
FBB_D18	F46	B	FBVDDQ
FBB_D19	F44	B	FBVDDQ
FBB_D2	G37	B	FBVDDQ
FBB_D20	E46	B	FBVDDQ
FBB_D21	C47	B	FBVDDQ
FBB_D22	E47	B	FBVDDQ
FBB_D23	C49	B	FBVDDQ
FBB_D24	G40	B	FBVDDQ
FBB_D25	C41	B	FBVDDQ
FBB_D26	E41	B	FBVDDQ
FBB_D27	F41	B	FBVDDQ
FBB_D28	F43	B	FBVDDQ
FBB_D29	C44	B	FBVDDQ
FBB_D3	F37	B	FBVDDQ
FBB_D30	H41	B	FBVDDQ
FBB_D31	H44	B	FBVDDQ
FBB_D32	L51	B	FBVDDQ
FBB_D33	L52	B	FBVDDQ
FBB_D34	N51	B	FBVDDQ
FBB_D35	L49	B	FBVDDQ
FBB_D36	L54	B	FBVDDQ
FBB_D37	N47	B	FBVDDQ
FBB_D38	P51	B	FBVDDQ
FBB_D39	P49	B	FBVDDQ
FBB_D4	H38	B	FBVDDQ
FBB_D40	T51	B	FBVDDQ
FBB_D41	P52	B	FBVDDQ
FBB_D42	P54	B	FBVDDQ
FBB_D43	U47	B	FBVDDQ
FBB_D44	U51	B	FBVDDQ
FBB_D45	U52	B	FBVDDQ
FBB_D46	U54	B	FBVDDQ
FBB_D47	U49	B	FBVDDQ
FBB_D48	D52	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBB_D49	C53	B	FBVDDQ
FBB_D5	E38	B	FBVDDQ
FBB_D50	C54	B	FBVDDQ
FBB_D51	C55	B	FBVDDQ
FBB_D52	D55	B	FBVDDQ
FBB_D53	D54	B	FBVDDQ
FBB_D54	F56	B	FBVDDQ
FBB_D55	F49	B	FBVDDQ
FBB_D56	G53	B	FBVDDQ
FBB_D57	H49	B	FBVDDQ
FBB_D58	H51	B	FBVDDQ
FBB_D59	G51	B	FBVDDQ
FBB_D6	F40	B	FBVDDQ
FBB_D60	H52	B	FBVDDQ
FBB_D61	H54	B	FBVDDQ
FBB_D62	K48	B	FBVDDQ
FBB_D63	K51	B	FBVDDQ
FBB_D7	D40	B	FBVDDQ
FBB_D8	F34	B	FBVDDQ
FBB_D9	J34	B	FBVDDQ
FBB_DQM0	F38	B	FBVDDQ
FBB_DQM1	F35	B	FBVDDQ
FBB_DQM2	G46	B	FBVDDQ
FBB_DQM3	G43	B	FBVDDQ
FBB_DQM4	N50	B	FBVDDQ
FBB_DQM5	T50	B	FBVDDQ
FBB_DQM6	E49	B	FBVDDQ
FBB_DQM7	K50	B	FBVDDQ
FBB_DQS_WP0	C38	I	FBVDDQ
FBB_DQS_WP1	C35	I	FBVDDQ
FBB_DQS_WP2	D46	I	FBVDDQ
FBB_DQS_WP3	D43	I	FBVDDQ
FBB_DQS_WP4	N53	I	FBVDDQ
FBB_DQS_WP5	T53	I	FBVDDQ
FBB_DQS_WP6	E53	I	FBVDDQ
FBB_DQS_WP7	K53	I	FBVDDQ
FBB_WCK01	J40	O	FBVDDQ
FBB_WCK01_N	K40	O	FBVDDQ
FBB_WCK23	J43	O	FBVDDQ
FBB_WCK23_N	K43	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBB_WCK45	P47	O	FBVDDQ
FBB_WCK45_N	P48	O	FBVDDQ
FBB_WCK67	K47	O	FBVDDQ
FBB_WCK67_N	J47	O	FBVDDQ
FBB_WCKB01	K38	O	FBVDDQ
FBB_WCKB01_N	J38	O	FBVDDQ
FBB_WCKB23	K41	O	FBVDDQ
FBB_WCKB23_N	J41	O	FBVDDQ
FBB_WCKB45	T48	O	FBVDDQ
FBB_WCKB45_N	T47	O	FBVDDQ
FBB_WCKB67	L47	O	FBVDDQ
FBB_WCKB67_N	L48	O	FBVDDQ
FBC_CLK0	K22	O	FBVDDQ
FBC_CLK0_N	J22	O	FBVDDQ
FBC_CLK1	K23	O	FBVDDQ
FBC_CLK1_N	J23	O	FBVDDQ
FBC_CMD0	B5	O	FBVDDQ
FBC_CMD1	A5	O	FBVDDQ
FBC_CMD10	A10	O	FBVDDQ
FBC_CMD11	A11	O	FBVDDQ
FBC_CMD12	D11	O	FBVDDQ
FBC_CMD13	A12	O	FBVDDQ
FBC_CMD14	B13	O	FBVDDQ
FBC_CMD15	A13	O	FBVDDQ
FBC_CMD16	A14	O	FBVDDQ
FBC_CMD17	D14	O	FBVDDQ
FBC_CMD18	A15	O	FBVDDQ
FBC_CMD19	B16	O	FBVDDQ
FBC_CMD2	C5	O	FBVDDQ
FBC_CMD20	A16	O	FBVDDQ
FBC_CMD21	A17	O	FBVDDQ
FBC_CMD22	D17	O	FBVDDQ
FBC_CMD23	A18	O	FBVDDQ
FBC_CMD24	B19	O	FBVDDQ
FBC_CMD25_NC	A19	NC	-
FBC_CMD26_NC	A20	NC	-
FBC_CMD27	B20	O	FBVDDQ
FBC_CMD28	A36	O	FBVDDQ
FBC_CMD29	D35	O	FBVDDQ
FBC_CMD3	A6	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBC_CMD30	A35	O	FBVDDQ
FBC_CMD31	A34	O	FBVDDQ
FBC_CMD32	B34	O	FBVDDQ
FBC_CMD33	A33	O	FBVDDQ
FBC_CMD34	D32	O	FBVDDQ
FBC_CMD35	A32	O	FBVDDQ
FBC_CMD36	A31	O	FBVDDQ
FBC_CMD37	B31	O	FBVDDQ
FBC_CMD38	A30	O	FBVDDQ
FBC_CMD39	D29	O	FBVDDQ
FBC_CMD4	B7	O	FBVDDQ
FBC_CMD40	A29	O	FBVDDQ
FBC_CMD41	A28	O	FBVDDQ
FBC_CMD42	B28	O	FBVDDQ
FBC_CMD43	A27	O	FBVDDQ
FBC_CMD44	D26	O	FBVDDQ
FBC_CMD45	A26	O	FBVDDQ
FBC_CMD46	A25	O	FBVDDQ
FBC_CMD47	B25	O	FBVDDQ
FBC_CMD48	A24	O	FBVDDQ
FBC_CMD49	D23	O	FBVDDQ
FBC_CMD5	A7	O	FBVDDQ
FBC_CMD50	A23	O	FBVDDQ
FBC_CMD51	A22	O	FBVDDQ
FBC_CMD52	B22	O	FBVDDQ
FBC_CMD53_NC	A21	NC	-
FBC_CMD54_NC	D20	NC	-
FBC_CMD55	B23	O	FBVDDQ
FBC_CMD6	A8	O	FBVDDQ
FBC_CMD7	D8	O	FBVDDQ
FBC_CMD8	A9	O	FBVDDQ
FBC_CMD9	B10	O	FBVDDQ
FBC_D0	F7	B	FBVDDQ
FBC_D1	H5	B	FBVDDQ
FBC_D10	C2	B	FBVDDQ
FBC_D11	D3	B	FBVDDQ
FBC_D12	C3	B	FBVDDQ
FBC_D13	B4	B	FBVDDQ
FBC_D14	E4	B	FBVDDQ
FBC_D15	D5	B	FBVDDQ

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Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBC_D16	F17	B	FBVDDQ
FBC_D17	E14	B	FBVDDQ
FBC_D18	C14	B	FBVDDQ
FBC_D19	H14	B	FBVDDQ
FBC_D2	F8	B	FBVDDQ
FBC_D20	E17	B	FBVDDQ
FBC_D21	F16	B	FBVDDQ
FBC_D22	C17	B	FBVDDQ
FBC_D23	H17	B	FBVDDQ
FBC_D24	F10	B	FBVDDQ
FBC_D25	G10	B	FBVDDQ
FBC_D26	C11	B	FBVDDQ
FBC_D27	E11	B	FBVDDQ
FBC_D28	F11	B	FBVDDQ
FBC_D29	F13	B	FBVDDQ
FBC_D3	G5	B	FBVDDQ
FBC_D30	F14	B	FBVDDQ
FBC_D31	H11	B	FBVDDQ
FBC_D32	F26	B	FBVDDQ
FBC_D33	E26	B	FBVDDQ
FBC_D34	H26	B	FBVDDQ
FBC_D35	D28	B	FBVDDQ
FBC_D36	C26	B	FBVDDQ
FBC_D37	E29	B	FBVDDQ
FBC_D38	F28	B	FBVDDQ
FBC_D39	G28	B	FBVDDQ
FBC_D4	H8	B	FBVDDQ
FBC_D40	F31	B	FBVDDQ
FBC_D41	K29	B	FBVDDQ
FBC_D42	H29	B	FBVDDQ
FBC_D43	J28	B	FBVDDQ
FBC_D44	D31	B	FBVDDQ
FBC_D45	G31	B	FBVDDQ
FBC_D46	E32	B	FBVDDQ
FBC_D47	H31	B	FBVDDQ
FBC_D48	F19	B	FBVDDQ
FBC_D49	K17	B	FBVDDQ
FBC_D5	E8	B	FBVDDQ
FBC_D50	C20	B	FBVDDQ
FBC_D51	J19	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBC_D52	E20	B	FBVDDQ
FBC_D53	F20	B	FBVDDQ
FBC_D54	K20	B	FBVDDQ
FBC_D55	H20	B	FBVDDQ
FBC_D56	G22	B	FBVDDQ
FBC_D57	F22	B	FBVDDQ
FBC_D58	C23	B	FBVDDQ
FBC_D59	D22	B	FBVDDQ
FBC_D6	C8	B	FBVDDQ
FBC_D60	E23	B	FBVDDQ
FBC_D61	F23	B	FBVDDQ
FBC_D62	F25	B	FBVDDQ
FBC_D63	H23	B	FBVDDQ
FBC_D7	D10	B	FBVDDQ
FBC_D8	D2	B	FBVDDQ
FBC_D9	E1	B	FBVDDQ
FBC_DQM0	G7	B	FBVDDQ
FBC_DQM1	E3	B	FBVDDQ
FBC_DQM2	G16	B	FBVDDQ
FBC_DQM3	G13	B	FBVDDQ
FBC_DQM4	F29	B	FBVDDQ
FBC_DQM5	F32	B	FBVDDQ
FBC_DQM6	G19	B	FBVDDQ
FBC_DQM7	G25	B	FBVDDQ
FBC_DQS_WP0	D7	I	FBVDDQ
FBC_DQS_WP1	B3	I	FBVDDQ
FBC_DQS_WP2	D16	I	FBVDDQ
FBC_DQS_WP3	D13	I	FBVDDQ
FBC_DQS_WP4	C29	I	FBVDDQ
FBC_DQS_WP5	C32	I	FBVDDQ
FBC_DQS_WP6	D19	I	FBVDDQ
FBC_DQS_WP7	D25	I	FBVDDQ
FBC_WCK01	K13	O	FBVDDQ
FBC_WCK01_N	J13	O	FBVDDQ
FBC_WCK23	J16	O	FBVDDQ
FBC_WCK23_N	K16	O	FBVDDQ
FBC_WCK45	K31	O	FBVDDQ
FBC_WCK45_N	J31	O	FBVDDQ
FBC_WCK67	K25	O	FBVDDQ
FBC_WCK67_N	J25	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBC_WCKB01	K11	O	FBVDDQ
FBC_WCKB01_N	J11	O	FBVDDQ
FBC_WCKB23	J14	O	FBVDDQ
FBC_WCKB23_N	K14	O	FBVDDQ
FBC_WCKB45	K32	O	FBVDDQ
FBC_WCKB45_N	J32	O	FBVDDQ
FBC_WCKB67	J26	O	FBVDDQ
FBC_WCKB67_N	K26	O	FBVDDQ
FBD_CLK0	AC10	O	FBVDDQ
FBD_CLK0_N	AC9	O	FBVDDQ
FBD_CLK1	AB10	O	FBVDDQ
FBD_CLK1_N	AB9	O	FBVDDQ
FBD_CMD0	AU1	O	FBVDDQ
FBD_CMD1	AU4	O	FBVDDQ
FBD_CMD10	AL1	O	FBVDDQ
FBD_CMD11	AL4	O	FBVDDQ
FBD_CMD12	AK1	O	FBVDDQ
FBD_CMD13	AJ2	O	FBVDDQ
FBD_CMD14	AJ1	O	FBVDDQ
FBD_CMD15	AH1	O	FBVDDQ
FBD_CMD16	AH4	O	FBVDDQ
FBD_CMD17	AG1	O	FBVDDQ
FBD_CMD18	AF2	O	FBVDDQ
FBD_CMD19	AF1	O	FBVDDQ
FBD_CMD2	AT1	O	FBVDDQ
FBD_CMD20	AE1	O	FBVDDQ
FBD_CMD21	AE4	O	FBVDDQ
FBD_CMD22	AD1	O	FBVDDQ
FBD_CMD23	AC2	O	FBVDDQ
FBD_CMD24	AC1	O	FBVDDQ
FBD_CMD25_NC	AB1	NC	-
FBD_CMD26_NC	AB4	NC	-
FBD_CMD27	AB2	O	FBVDDQ
FBD_CMD28	G2	O	FBVDDQ
FBD_CMD29	G1	O	FBVDDQ
FBD_CMD3	AR2	O	FBVDDQ
FBD_CMD30	G3	O	FBVDDQ
FBD_CMD31	H1	O	FBVDDQ
FBD_CMD32	H2	O	FBVDDQ
FBD_CMD33	J1	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBD_CMD34	K4	O	FBVDDQ
FBD_CMD35	K1	O	FBVDDQ
FBD_CMD36	K2	O	FBVDDQ
FBD_CMD37	L1	O	FBVDDQ
FBD_CMD38	L2	O	FBVDDQ
FBD_CMD39	M1	O	FBVDDQ
FBD_CMD4	AR1	O	FBVDDQ
FBD_CMD40	N4	O	FBVDDQ
FBD_CMD41	N1	O	FBVDDQ
FBD_CMD42	P1	O	FBVDDQ
FBD_CMD43	P2	O	FBVDDQ
FBD_CMD44	R1	O	FBVDDQ
FBD_CMD45	T4	O	FBVDDQ
FBD_CMD46	T1	O	FBVDDQ
FBD_CMD47	U1	O	FBVDDQ
FBD_CMD48	U2	O	FBVDDQ
FBD_CMD49	V1	O	FBVDDQ
FBD_CMD5	AP1	O	FBVDDQ
FBD_CMD50	W4	O	FBVDDQ
FBD_CMD51	W1	O	FBVDDQ
FBD_CMD52	Y1	O	FBVDDQ
FBD_CMD53_NC	Y2	NC	-
FBD_CMD54_NC	AA1	NC	-
FBD_CMD55	W2	O	FBVDDQ
FBD_CMD6	AP4	O	FBVDDQ
FBD_CMD7	AN1	O	FBVDDQ
FBD_CMD8	AM2	O	FBVDDQ
FBD_CMD9	AM1	O	FBVDDQ
FBD_D0	AR4	B	FBVDDQ
FBD_D1	AP8	B	FBVDDQ
FBD_D10	AV9	B	FBVDDQ
FBD_D11	AU3	B	FBVDDQ
FBD_D12	AU6	B	FBVDDQ
FBD_D13	AU8	B	FBVDDQ
FBD_D14	AU10	B	FBVDDQ
FBD_D15	AR7	B	FBVDDQ
FBD_D16	AF6	B	FBVDDQ
FBD_D17	AH5	B	FBVDDQ
FBD_D18	AH3	B	FBVDDQ
FBD_D19	AF9	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBD_D2	AP6	B	FBVDDQ
FBD_D20	AE6	B	FBVDDQ
FBD_D21	AE8	B	FBVDDQ
FBD_D22	AE5	B	FBVDDQ
FBD_D23	AE10	B	FBVDDQ
FBD_D24	AL6	B	FBVDDQ
FBD_D25	AL3	B	FBVDDQ
FBD_D26	AL5	B	FBVDDQ
FBD_D27	AL8	B	FBVDDQ
FBD_D28	AJ6	B	FBVDDQ
FBD_D29	AL10	B	FBVDDQ
FBD_D3	AR6	B	FBVDDQ
FBD_D30	AH6	B	FBVDDQ
FBD_D31	AH8	B	FBVDDQ
FBD_D32	T5	B	FBVDDQ
FBD_D33	T6	B	FBVDDQ
FBD_D34	P6	B	FBVDDQ
FBD_D35	T8	B	FBVDDQ
FBD_D36	T3	B	FBVDDQ
FBD_D37	N5	B	FBVDDQ
FBD_D38	N3	B	FBVDDQ
FBD_D39	N6	B	FBVDDQ
FBD_D4	AM6	B	FBVDDQ
FBD_D40	L6	B	FBVDDQ
FBD_D41	N8	B	FBVDDQ
FBD_D42	K6	B	FBVDDQ
FBD_D43	L9	B	FBVDDQ
FBD_D44	K3	B	FBVDDQ
FBD_D45	K5	B	FBVDDQ
FBD_D46	J2	B	FBVDDQ
FBD_D47	K8	B	FBVDDQ
FBD_D48	AC7	B	FBVDDQ
FBD_D49	AE3	B	FBVDDQ
FBD_D5	AP3	B	FBVDDQ
FBD_D50	AC6	B	FBVDDQ
FBD_D51	AC4	B	FBVDDQ
FBD_D52	AB3	B	FBVDDQ
FBD_D53	AB5	B	FBVDDQ
FBD_D54	AB6	B	FBVDDQ
FBD_D55	AB8	B	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBD_D56	W6	B	FBVDDQ
FBD_D57	W8	B	FBVDDQ
FBD_D58	W5	B	FBVDDQ
FBD_D59	Y6	B	FBVDDQ
FBD_D6	AP5	B	FBVDDQ
FBD_D60	W3	B	FBVDDQ
FBD_D61	U9	B	FBVDDQ
FBD_D62	U6	B	FBVDDQ
FBD_D63	T10	B	FBVDDQ
FBD_D7	AM9	B	FBVDDQ
FBD_D8	AU5	B	FBVDDQ
FBD_D9	AV6	B	FBVDDQ
FBD_DQM0	AM7	B	FBVDDQ
FBD_DQM1	AV7	B	FBVDDQ
FBD_DQM2	AF7	B	FBVDDQ
FBD_DQM3	AJ7	B	FBVDDQ
FBD_DQM4	P7	B	FBVDDQ
FBD_DQM5	L7	B	FBVDDQ
FBD_DQM6	Y7	B	FBVDDQ
FBD_DQM7	U7	B	FBVDDQ
FBD_DQS_WP0	AM4	I	FBVDDQ
FBD_DQS_WP1	AV4	I	FBVDDQ
FBD_DQS_WP2	AF4	I	FBVDDQ
FBD_DQS_WP3	AJ4	I	FBVDDQ
FBD_DQS_WP4	P4	I	FBVDDQ
FBD_DQS_WP5	L4	I	FBVDDQ
FBD_DQS_WP6	Y4	I	FBVDDQ
FBD_DQS_WP7	U4	I	FBVDDQ
FBD_WCK01	AP9	O	FBVDDQ
FBD_WCK01_N	AP10	O	FBVDDQ
FBD_WCK23	AH10	O	FBVDDQ
FBD_WCK23_N	AH9	O	FBVDDQ
FBD_WCK45	P10	O	FBVDDQ
FBD_WCK45_N	P9	O	FBVDDQ
FBD_WCK67	Y10	O	FBVDDQ
FBD_WCK67_N	Y9	O	FBVDDQ
FBD_WCKB01	AR9	O	FBVDDQ
FBD_WCKB01_N	AR10	O	FBVDDQ
FBD_WCKB23	AJ10	O	FBVDDQ
FBD_WCKB23_N	AJ9	O	FBVDDQ

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBD_WCKB45	N10	O	FBVDDQ
FBD_WCKB45_N	N9	O	FBVDDQ
FBD_WCKB67	W9	O	FBVDDQ
FBD_WCKB67_N	W10	O	FBVDDQ
FBVDDQ	AB11	P	-
FBVDDQ	AB46	P	-
FBVDDQ	AC11	P	-
FBVDDQ	AE46	P	-
FBVDDQ	AF11	P	-
FBVDDQ	AF46	P	-
FBVDDQ	AH11	P	-
FBVDDQ	AH46	P	-
FBVDDQ	AJ11	P	-
FBVDDQ	AJ46	P	-
FBVDDQ	AL11	P	-
FBVDDQ	AL46	P	-
FBVDDQ	AM11	P	-
FBVDDQ	AM46	P	-
FBVDDQ	AP11	P	-
FBVDDQ	AR11	P	-
FBVDDQ	AR46	P	-
FBVDDQ	AU11	P	-
FBVDDQ	AU46	P	-
FBVDDQ	AV11	P	-
FBVDDQ	AV46	P	-
FBVDDQ	AY46	P	-
FBVDDQ	BA46	P	-
FBVDDQ	BC46	P	-
FBVDDQ	K10	P	-
FBVDDQ	L11	P	-
FBVDDQ	L13	P	-
FBVDDQ	L14	P	-
FBVDDQ	L16	P	-
FBVDDQ	L19	P	-
FBVDDQ	L20	P	-
FBVDDQ	L22	P	-
FBVDDQ	L23	P	-
FBVDDQ	L25	P	-
FBVDDQ	L26	P	-
FBVDDQ	L28	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
FBVDDQ	L29	P	-
FBVDDQ	L31	P	-
FBVDDQ	L32	P	-
FBVDDQ	L34	P	-
FBVDDQ	L37	P	-
FBVDDQ	L38	P	-
FBVDDQ	L40	P	-
FBVDDQ	L41	P	-
FBVDDQ	L43	P	-
FBVDDQ	L44	P	-
FBVDDQ	L46	P	-
FBVDDQ	N11	P	-
FBVDDQ	N46	P	-
FBVDDQ	P11	P	-
FBVDDQ	P46	P	-
FBVDDQ	T11	P	-
FBVDDQ	U11	P	-
FBVDDQ	U46	P	-
FBVDDQ	W11	P	-
FBVDDQ	W46	P	-
FBVDDQ	Y11	P	-
FBVDDQ	Y46	P	-
FBVDDQ_SENSE	E54	P	-
FUSE_SRC	BH25	P	-
GND	A2	P	-
GND	A3	P	-
GND	A54	P	-
GND	A55	P	-
GND	AA10	P	-
GND	AA13	P	-
GND	AA14	P	-
GND	AA15	P	-
GND	AA16	P	-
GND	AA17	P	-
GND	AA18	P	-
GND	AA19	P	-
GND	AA2	P	-
GND	AA20	P	-
GND	AA21	P	-
GND	AA22	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AA23	P	-
GND	AA24	P	-
GND	AA25	P	-
GND	AA26	P	-
GND	AA27	P	-
GND	AA28	P	-
GND	AA29	P	-
GND	AA30	P	-
GND	AA31	P	-
GND	AA32	P	-
GND	AA33	P	-
GND	AA34	P	-
GND	AA35	P	-
GND	AA36	P	-
GND	AA37	P	-
GND	AA38	P	-
GND	AA39	P	-
GND	AA4	P	-
GND	AA40	P	-
GND	AA41	P	-
GND	AA42	P	-
GND	AA43	P	-
GND	AA44	P	-
GND	AA47	P	-
GND	AA49	P	-
GND	AA51	P	-
GND	AA53	P	-
GND	AA55	P	-
GND	AA6	P	-
GND	AA8	P	-
GND	AB47	P	-
GND	AB49	P	-
GND	AB52	P	-
GND	AB54	P	-
GND	AB7	P	-
GND	AC13	P	-
GND	AC14	P	-
GND	AC15	P	-
GND	AC16	P	-
GND	AC17	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AC18	P	-
GND	AC19	P	-
GND	AC20	P	-
GND	AC21	P	-
GND	AC22	P	-
GND	AC23	P	-
GND	AC24	P	-
GND	AC25	P	-
GND	AC26	P	-
GND	AC27	P	-
GND	AC28	P	-
GND	AC29	P	-
GND	AC3	P	-
GND	AC30	P	-
GND	AC31	P	-
GND	AC32	P	-
GND	AC33	P	-
GND	AC34	P	-
GND	AC35	P	-
GND	AC36	P	-
GND	AC37	P	-
GND	AC38	P	-
GND	AC39	P	-
GND	AC40	P	-
GND	AC41	P	-
GND	AC42	P	-
GND	AC43	P	-
GND	AC44	P	-
GND	AC5	P	-
GND	AC50	P	-
GND	AC55	P	-
GND	AC8	P	-
GND	AD10	P	-
GND	AD2	P	-
GND	AD4	P	-
GND	AD47	P	-
GND	AD49	P	-
GND	AD51	P	-
GND	AD53	P	-
GND	AD55	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AD6	P	-
GND	AD8	P	-
GND	AE13	P	-
GND	AE14	P	-
GND	AE15	P	-
GND	AE16	P	-
GND	AE17	P	-
GND	AE18	P	-
GND	AE19	P	-
GND	AE2	P	-
GND	AE20	P	-
GND	AE21	P	-
GND	AE22	P	-
GND	AE23	P	-
GND	AE24	P	-
GND	AE25	P	-
GND	AE26	P	-
GND	AE27	P	-
GND	AE28	P	-
GND	AE29	P	-
GND	AE30	P	-
GND	AE31	P	-
GND	AE32	P	-
GND	AE33	P	-
GND	AE34	P	-
GND	AE35	P	-
GND	AE36	P	-
GND	AE37	P	-
GND	AE38	P	-
GND	AE39	P	-
GND	AE40	P	-
GND	AE41	P	-
GND	AE42	P	-
GND	AE43	P	-
GND	AE44	P	-
GND	AE49	P	-
GND	AE52	P	-
GND	AE54	P	-
GND	AE7	P	-
GND	AE9	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AF10	P	-
GND	AF3	P	-
GND	AF48	P	-
GND	AF5	P	-
GND	AF50	P	-
GND	AF55	P	-
GND	AF8	P	-
GND	AG10	P	-
GND	AG13	P	-
GND	AG14	P	-
GND	AG15	P	-
GND	AG16	P	-
GND	AG17	P	-
GND	AG18	P	-
GND	AG19	P	-
GND	AG2	P	-
GND	AG20	P	-
GND	AG21	P	-
GND	AG22	P	-
GND	AG23	P	-
GND	AG24	P	-
GND	AG25	P	-
GND	AG26	P	-
GND	AG27	P	-
GND	AG28	P	-
GND	AG29	P	-
GND	AG30	P	-
GND	AG31	P	-
GND	AG32	P	-
GND	AG33	P	-
GND	AG34	P	-
GND	AG35	P	-
GND	AG36	P	-
GND	AG37	P	-
GND	AG38	P	-
GND	AG39	P	-
GND	AG4	P	-
GND	AG40	P	-
GND	AG41	P	-
GND	AG42	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AG43	P	-
GND	AG44	P	-
GND	AG47	P	-
GND	AG49	P	-
GND	AG51	P	-
GND	AG53	P	-
GND	AG55	P	-
GND	AG6	P	-
GND	AG8	P	-
GND	AH2	P	-
GND	AH47	P	-
GND	AH49	P	-
GND	AH52	P	-
GND	AH54	P	-
GND	AH7	P	-
GND	AJ13	P	-
GND	AJ14	P	-
GND	AJ15	P	-
GND	AJ16	P	-
GND	AJ17	P	-
GND	AJ18	P	-
GND	AJ19	P	-
GND	AJ20	P	-
GND	AJ21	P	-
GND	AJ22	P	-
GND	AJ23	P	-
GND	AJ24	P	-
GND	AJ25	P	-
GND	AJ26	P	-
GND	AJ27	P	-
GND	AJ28	P	-
GND	AJ29	P	-
GND	AJ3	P	-
GND	AJ30	P	-
GND	AJ31	P	-
GND	AJ32	P	-
GND	AJ33	P	-
GND	AJ34	P	-
GND	AJ35	P	-
GND	AJ36	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AJ37	P	-
GND	AJ38	P	-
GND	AJ39	P	-
GND	AJ40	P	-
GND	AJ41	P	-
GND	AJ42	P	-
GND	AJ43	P	-
GND	AJ44	P	-
GND	AJ5	P	-
GND	AJ50	P	-
GND	AJ55	P	-
GND	AJ8	P	-
GND	AK10	P	-
GND	AK2	P	-
GND	AK4	P	-
GND	AK47	P	-
GND	AK49	P	-
GND	AK51	P	-
GND	AK53	P	-
GND	AK55	P	-
GND	AK6	P	-
GND	AK8	P	-
GND	AL13	P	-
GND	AL14	P	-
GND	AL15	P	-
GND	AL16	P	-
GND	AL17	P	-
GND	AL18	P	-
GND	AL19	P	-
GND	AL2	P	-
GND	AL20	P	-
GND	AL21	P	-
GND	AL22	P	-
GND	AL23	P	-
GND	AL24	P	-
GND	AL25	P	-
GND	AL26	P	-
GND	AL27	P	-
GND	AL28	P	-
GND	AL29	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AL30	P	-
GND	AL31	P	-
GND	AL32	P	-
GND	AL33	P	-
GND	AL34	P	-
GND	AL35	P	-
GND	AL36	P	-
GND	AL37	P	-
GND	AL38	P	-
GND	AL39	P	-
GND	AL40	P	-
GND	AL41	P	-
GND	AL42	P	-
GND	AL43	P	-
GND	AL44	P	-
GND	AL49	P	-
GND	AL52	P	-
GND	AL54	P	-
GND	AL7	P	-
GND	AL9	P	-
GND	AM10	P	-
GND	AM3	P	-
GND	AM48	P	-
GND	AM5	P	-
GND	AM50	P	-
GND	AM55	P	-
GND	AM8	P	-
GND	AN10	P	-
GND	AN13	P	-
GND	AN14	P	-
GND	AN15	P	-
GND	AN16	P	-
GND	AN17	P	-
GND	AN18	P	-
GND	AN19	P	-
GND	AN2	P	-
GND	AN20	P	-
GND	AN21	P	-
GND	AN22	P	-
GND	AN23	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AN24	P	-
GND	AN25	P	-
GND	AN26	P	-
GND	AN27	P	-
GND	AN28	P	-
GND	AN29	P	-
GND	AN30	P	-
GND	AN31	P	-
GND	AN32	P	-
GND	AN33	P	-
GND	AN34	P	-
GND	AN35	P	-
GND	AN36	P	-
GND	AN37	P	-
GND	AN38	P	-
GND	AN39	P	-
GND	AN4	P	-
GND	AN40	P	-
GND	AN41	P	-
GND	AN42	P	-
GND	AN43	P	-
GND	AN44	P	-
GND	AN47	P	-
GND	AN49	P	-
GND	AN51	P	-
GND	AN53	P	-
GND	AN55	P	-
GND	AN6	P	-
GND	AN8	P	-
GND	AP2	P	-
GND	AP49	P	-
GND	AP52	P	-
GND	AP54	P	-
GND	AP7	P	-
GND	AR13	P	-
GND	AR14	P	-
GND	AR15	P	-
GND	AR16	P	-
GND	AR17	P	-
GND	AR18	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AR19	P	-
GND	AR20	P	-
GND	AR21	P	-
GND	AR22	P	-
GND	AR23	P	-
GND	AR24	P	-
GND	AR25	P	-
GND	AR26	P	-
GND	AR27	P	-
GND	AR28	P	-
GND	AR29	P	-
GND	AR3	P	-
GND	AR30	P	-
GND	AR31	P	-
GND	AR32	P	-
GND	AR33	P	-
GND	AR34	P	-
GND	AR35	P	-
GND	AR36	P	-
GND	AR37	P	-
GND	AR38	P	-
GND	AR39	P	-
GND	AR40	P	-
GND	AR41	P	-
GND	AR42	P	-
GND	AR43	P	-
GND	AR44	P	-
GND	AR5	P	-
GND	AR50	P	-
GND	AR8	P	-
GND	AT10	P	-
GND	AT2	P	-
GND	AT4	P	-
GND	AT47	P	-
GND	AT49	P	-
GND	AT51	P	-
GND	AT53	P	-
GND	AT55	P	-
GND	AT6	P	-
GND	AT8	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AU14	P	-
GND	AU15	P	-
GND	AU16	P	-
GND	AU17	P	-
GND	AU18	P	-
GND	AU19	P	-
GND	AU2	P	-
GND	AU20	P	-
GND	AU21	P	-
GND	AU22	P	-
GND	AU23	P	-
GND	AU24	P	-
GND	AU25	P	-
GND	AU26	P	-
GND	AU27	P	-
GND	AU28	P	-
GND	AU29	P	-
GND	AU30	P	-
GND	AU31	P	-
GND	AU32	P	-
GND	AU33	P	-
GND	AU34	P	-
GND	AU35	P	-
GND	AU36	P	-
GND	AU37	P	-
GND	AU38	P	-
GND	AU39	P	-
GND	AU40	P	-
GND	AU41	P	-
GND	AU42	P	-
GND	AU43	P	-
GND	AU49	P	-
GND	AU52	P	-
GND	AU54	P	-
GND	AU7	P	-
GND	AU9	P	-
GND	AV10	P	-
GND	AV3	P	-
GND	AV5	P	-
GND	AV50	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AV8	P	-
GND	AW10	P	-
GND	AW14	P	-
GND	AW15	P	-
GND	AW16	P	-
GND	AW17	P	-
GND	AW18	P	-
GND	AW19	P	-
GND	AW2	P	-
GND	AW20	P	-
GND	AW21	P	-
GND	AW22	P	-
GND	AW23	P	-
GND	AW24	P	-
GND	AW25	P	-
GND	AW26	P	-
GND	AW27	P	-
GND	AW28	P	-
GND	AW29	P	-
GND	AW30	P	-
GND	AW31	P	-
GND	AW32	P	-
GND	AW33	P	-
GND	AW34	P	-
GND	AW35	P	-
GND	AW36	P	-
GND	AW37	P	-
GND	AW38	P	-
GND	AW39	P	-
GND	AW4	P	-
GND	AW40	P	-
GND	AW41	P	-
GND	AW42	P	-
GND	AW43	P	-
GND	AW47	P	-
GND	AW49	P	-
GND	AW51	P	-
GND	AW53	P	-
GND	AW55	P	-
GND	AW6	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	AW8	P	-
GND	AY47	P	-
GND	AY49	P	-
GND	AY52	P	-
GND	AY54	P	-
GND	B1	P	-
GND	B11	P	-
GND	B12	P	-
GND	B14	P	-
GND	B15	P	-
GND	B17	P	-
GND	B18	P	-
GND	B2	P	-
GND	B21	P	-
GND	B24	P	-
GND	B26	P	-
GND	B27	P	-
GND	B29	P	-
GND	B30	P	-
GND	B32	P	-
GND	B33	P	-
GND	B35	P	-
GND	B36	P	-
GND	B38	P	-
GND	B39	P	-
GND	B41	P	-
GND	B42	P	-
GND	B44	P	-
GND	B45	P	-
GND	B47	P	-
GND	B48	P	-
GND	B51	P	-
GND	B55	P	-
GND	B56	P	-
GND	B6	P	-
GND	B8	P	-
GND	B9	P	-
GND	BA14	P	-
GND	BA15	P	-
GND	BA16	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BA17	P	-
GND	BA18	P	-
GND	BA19	P	-
GND	BA20	P	-
GND	BA21	P	-
GND	BA22	P	-
GND	BA23	P	-
GND	BA24	P	-
GND	BA25	P	-
GND	BA26	P	-
GND	BA27	P	-
GND	BA28	P	-
GND	BA29	P	-
GND	BA30	P	-
GND	BA31	P	-
GND	BA32	P	-
GND	BA33	P	-
GND	BA34	P	-
GND	BA35	P	-
GND	BA36	P	-
GND	BA37	P	-
GND	BA38	P	-
GND	BA39	P	-
GND	BA40	P	-
GND	BA41	P	-
GND	BA42	P	-
GND	BA43	P	-
GND	BA50	P	-
GND	BA55	P	-
GND	BB47	P	-
GND	BB49	P	-
GND	BB51	P	-
GND	BB53	P	-
GND	BB55	P	-
GND	BC14	P	-
GND	BC15	P	-
GND	BC16	P	-
GND	BC17	P	-
GND	BC18	P	-
GND	BC19	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BC20	P	-
GND	BC21	P	-
GND	BC22	P	-
GND	BC23	P	-
GND	BC24	P	-
GND	BC25	P	-
GND	BC26	P	-
GND	BC27	P	-
GND	BC28	P	-
GND	BC29	P	-
GND	BC30	P	-
GND	BC31	P	-
GND	BC32	P	-
GND	BC33	P	-
GND	BC34	P	-
GND	BC35	P	-
GND	BC36	P	-
GND	BC37	P	-
GND	BC38	P	-
GND	BC39	P	-
GND	BC40	P	-
GND	BC41	P	-
GND	BC42	P	-
GND	BC43	P	-
GND	BC49	P	-
GND	BC52	P	-
GND	BC54	P	-
GND	BD15	P	-
GND	BD16	P	-
GND	BD19	P	-
GND	BD20	P	-
GND	BD23	P	-
GND	BD24	P	-
GND	BD27	P	-
GND	BD30	P	-
GND	BD33	P	-
GND	BD34	P	-
GND	BD37	P	-
GND	BD38	P	-
GND	BD41	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BD42	P	-
GND	BD48	P	-
GND	BD50	P	-
GND	BD55	P	-
GND	BE10	P	-
GND	BE2	P	-
GND	BE4	P	-
GND	BE49	P	-
GND	BE51	P	-
GND	BE53	P	-
GND	BE55	P	-
GND	BE6	P	-
GND	BE8	P	-
GND	BF52	P	-
GND	BF54	P	-
GND	BG12	P	-
GND	BG15	P	-
GND	BG18	P	-
GND	BG21	P	-
GND	BG24	P	-
GND	BG30	P	-
GND	BG33	P	-
GND	BG36	P	-
GND	BG39	P	-
GND	BG42	P	-
GND	BG49	P	-
GND	BG55	P	-
GND	BH13	P	-
GND	BH2	P	-
GND	BH4	P	-
GND	BH51	P	-
GND	BH53	P	-
GND	BH55	P	-
GND	BH6	P	-
GND	BH8	P	-
GND	BJ12	P	-
GND	BJ14	P	-
GND	BJ15	P	-
GND	BJ17	P	-
GND	BJ18	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BJ20	P	-
GND	BJ21	P	-
GND	BJ23	P	-
GND	BJ24	P	-
GND	BJ31	P	-
GND	BJ33	P	-
GND	BJ35	P	-
GND	BJ37	P	-
GND	BJ39	P	-
GND	BJ41	P	-
GND	BJ43	P	-
GND	BJ45	P	-
GND	BJ53	P	-
GND	BJ9	P	-
GND	BK31	P	-
GND	BK33	P	-
GND	BK35	P	-
GND	BK37	P	-
GND	BK39	P	-
GND	BK41	P	-
GND	BK43	P	-
GND	BK45	P	-
GND	BK54	P	-
GND	BL12	P	-
GND	BL15	P	-
GND	BL18	P	-
GND	BL2	P	-
GND	BL21	P	-
GND	BL24	P	-
GND	BL30	P	-
GND	BL32	P	-
GND	BL34	P	-
GND	BL36	P	-
GND	BL38	P	-
GND	BL4	P	-
GND	BL40	P	-
GND	BL42	P	-
GND	BL44	P	-
GND	BL46	P	-
GND	BL55	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BL6	P	-
GND	BL9	P	-
GND	BM14	P	-
GND	BM17	P	-
GND	BM20	P	-
GND	BM23	P	-
GND	BM30	P	-
GND	BM32	P	-
GND	BM34	P	-
GND	BM36	P	-
GND	BM38	P	-
GND	BM40	P	-
GND	BM42	P	-
GND	BM44	P	-
GND	BM46	P	-
GND	BM48	P	-
GND	BN10	P	-
GND	BN11	P	-
GND	BN12	P	-
GND	BN13	P	-
GND	BN14	P	-
GND	BN15	P	-
GND	BN16	P	-
GND	BN17	P	-
GND	BN18	P	-
GND	BN19	P	-
GND	BN20	P	-
GND	BN21	P	-
GND	BN22	P	-
GND	BN23	P	-
GND	BN24	P	-
GND	BN30	P	-
GND	BN31	P	-
GND	BN32	P	-
GND	BN33	P	-
GND	BN34	P	-
GND	BN35	P	-
GND	BN36	P	-
GND	BN37	P	-
GND	BN38	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	BN39	P	-
GND	BN4	P	-
GND	BN40	P	-
GND	BN41	P	-
GND	BN42	P	-
GND	BN43	P	-
GND	BN44	P	-
GND	BN45	P	-
GND	BN46	P	-
GND	BN47	P	-
GND	BN48	P	-
GND	BN6	P	-
GND	BN9	P	-
GND	BP1	P	-
GND	BP32	P	-
GND	BP34	P	-
GND	BP36	P	-
GND	BP38	P	-
GND	BP40	P	-
GND	BP42	P	-
GND	BP44	P	-
GND	BP46	P	-
GND	BP48	P	-
GND	BR1	P	-
GND	BR12	P	-
GND	BR15	P	-
GND	BR18	P	-
GND	BR2	P	-
GND	BR21	P	-
GND	BR24	P	-
GND	BR30	P	-
GND	BR6	P	-
GND	BR9	P	-
GND	BT2	P	-
GND	BT3	P	-
GND	C1	P	-
GND	C10	P	-
GND	C13	P	-
GND	C16	P	-
GND	C19	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	C22	P	-
GND	C25	P	-
GND	C28	P	-
GND	C31	P	-
GND	C34	P	-
GND	C37	P	-
GND	C4	P	-
GND	C40	P	-
GND	C43	P	-
GND	C46	P	-
GND	C56	P	-
GND	C7	P	-
GND	D12	P	-
GND	D15	P	-
GND	D18	P	-
GND	D21	P	-
GND	D24	P	-
GND	D27	P	-
GND	D30	P	-
GND	D33	P	-
GND	D36	P	-
GND	D39	P	-
GND	D4	P	-
GND	D42	P	-
GND	D45	P	-
GND	D48	P	-
GND	D49	P	-
GND	D51	P	-
GND	D53	P	-
GND	D6	P	-
GND	D9	P	-
GND	E10	P	-
GND	E13	P	-
GND	E16	P	-
GND	E19	P	-
GND	E2	P	-
GND	E22	P	-
GND	E25	P	-
GND	E28	P	-
GND	E31	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	E34	P	-
GND	E37	P	-
GND	E40	P	-
GND	E43	P	-
GND	E5	P	-
GND	E52	P	-
GND	E7	P	-
GND	F1	P	-
GND	F12	P	-
GND	F15	P	-
GND	F18	P	-
GND	F2	P	-
GND	F21	P	-
GND	F24	P	-
GND	F27	P	-
GND	F30	P	-
GND	F33	P	-
GND	F36	P	-
GND	F39	P	-
GND	F4	P	-
GND	F42	P	-
GND	F45	P	-
GND	F47	P	-
GND	F48	P	-
GND	F51	P	-
GND	F53	P	-
GND	F55	P	-
GND	F6	P	-
GND	F9	P	-
GND	G11	P	-
GND	G14	P	-
GND	G17	P	-
GND	G20	P	-
GND	G23	P	-
GND	G26	P	-
GND	G29	P	-
GND	G32	P	-
GND	G35	P	-
GND	G38	P	-
GND	G4	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	G41	P	-
GND	G44	P	-
GND	G49	P	-
GND	G52	P	-
GND	G54	P	-
GND	G8	P	-
GND	H10	P	-
GND	H12	P	-
GND	H13	P	-
GND	H15	P	-
GND	H16	P	-
GND	H18	P	-
GND	H19	P	-
GND	H21	P	-
GND	H22	P	-
GND	H24	P	-
GND	H25	P	-
GND	H27	P	-
GND	H28	P	-
GND	H3	P	-
GND	H30	P	-
GND	H32	P	-
GND	H33	P	-
GND	H34	P	-
GND	H36	P	-
GND	H37	P	-
GND	H39	P	-
GND	H4	P	-
GND	H40	P	-
GND	H42	P	-
GND	H43	P	-
GND	H45	P	-
GND	H46	P	-
GND	H47	P	-
GND	H48	P	-
GND	H50	P	-
GND	H55	P	-
GND	H6	P	-
GND	H7	P	-
GND	H9	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	J10	P	-
GND	J17	P	-
GND	J20	P	-
GND	J29	P	-
GND	J35	P	-
GND	J4	P	-
GND	J49	P	-
GND	J51	P	-
GND	J53	P	-
GND	J55	P	-
GND	J6	P	-
GND	J8	P	-
GND	K12	P	-
GND	K15	P	-
GND	K18	P	-
GND	K19	P	-
GND	K21	P	-
GND	K24	P	-
GND	K27	P	-
GND	K28	P	-
GND	K30	P	-
GND	K33	P	-
GND	K36	P	-
GND	K37	P	-
GND	K39	P	-
GND	K42	P	-
GND	K45	P	-
GND	K49	P	-
GND	K52	P	-
GND	K54	P	-
GND	K7	P	-
GND	K9	P	-
GND	L10	P	-
GND	L3	P	-
GND	L5	P	-
GND	L50	P	-
GND	L55	P	-
GND	L8	P	-
GND	M10	P	-
GND	M2	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	M4	P	-
GND	M47	P	-
GND	M49	P	-
GND	M51	P	-
GND	M53	P	-
GND	M55	P	-
GND	M6	P	-
GND	M8	P	-
GND	N14	P	-
GND	N16	P	-
GND	N18	P	-
GND	N2	P	-
GND	N20	P	-
GND	N22	P	-
GND	N24	P	-
GND	N26	P	-
GND	N28	P	-
GND	N29	P	-
GND	N31	P	-
GND	N33	P	-
GND	N35	P	-
GND	N37	P	-
GND	N39	P	-
GND	N41	P	-
GND	N43	P	-
GND	N48	P	-
GND	N52	P	-
GND	N54	P	-
GND	N7	P	-
GND	P3	P	-
GND	P5	P	-
GND	P50	P	-
GND	P55	P	-
GND	P8	P	-
GND	R10	P	-
GND	R13	P	-
GND	R14	P	-
GND	R15	P	-
GND	R16	P	-
GND	R17	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	R18	P	-
GND	R19	P	-
GND	R2	P	-
GND	R20	P	-
GND	R21	P	-
GND	R22	P	-
GND	R23	P	-
GND	R24	P	-
GND	R25	P	-
GND	R26	P	-
GND	R27	P	-
GND	R28	P	-
GND	R29	P	-
GND	R30	P	-
GND	R31	P	-
GND	R32	P	-
GND	R33	P	-
GND	R34	P	-
GND	R35	P	-
GND	R36	P	-
GND	R37	P	-
GND	R38	P	-
GND	R39	P	-
GND	R4	P	-
GND	R40	P	-
GND	R41	P	-
GND	R42	P	-
GND	R43	P	-
GND	R44	P	-
GND	R47	P	-
GND	R49	P	-
GND	R51	P	-
GND	R53	P	-
GND	R55	P	-
GND	R6	P	-
GND	R8	P	-
GND	T2	P	-
GND	T49	P	-
GND	T52	P	-
GND	T54	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	T7	P	-
GND	T9	P	-
GND	U10	P	-
GND	U13	P	-
GND	U14	P	-
GND	U15	P	-
GND	U16	P	-
GND	U17	P	-
GND	U18	P	-
GND	U19	P	-
GND	U20	P	-
GND	U21	P	-
GND	U22	P	-
GND	U23	P	-
GND	U24	P	-
GND	U25	P	-
GND	U26	P	-
GND	U27	P	-
GND	U28	P	-
GND	U29	P	-
GND	U3	P	-
GND	U30	P	-
GND	U31	P	-
GND	U32	P	-
GND	U33	P	-
GND	U34	P	-
GND	U35	P	-
GND	U36	P	-
GND	U37	P	-
GND	U38	P	-
GND	U39	P	-
GND	U40	P	-
GND	U41	P	-
GND	U42	P	-
GND	U43	P	-
GND	U44	P	-
GND	U48	P	-
GND	U5	P	-
GND	U50	P	-
GND	U55	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	U8	P	-
GND	V10	P	-
GND	V2	P	-
GND	V4	P	-
GND	V47	P	-
GND	V49	P	-
GND	V51	P	-
GND	V53	P	-
GND	V55	P	-
GND	V6	P	-
GND	V8	P	-
GND	W13	P	-
GND	W14	P	-
GND	W15	P	-
GND	W16	P	-
GND	W17	P	-
GND	W18	P	-
GND	W19	P	-
GND	W20	P	-
GND	W21	P	-
GND	W22	P	-
GND	W23	P	-
GND	W24	P	-
GND	W25	P	-
GND	W26	P	-
GND	W27	P	-
GND	W28	P	-
GND	W29	P	-
GND	W30	P	-
GND	W31	P	-
GND	W32	P	-
GND	W33	P	-
GND	W34	P	-
GND	W35	P	-
GND	W36	P	-
GND	W37	P	-
GND	W38	P	-
GND	W39	P	-
GND	W40	P	-
GND	W41	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GND	W42	P	-
GND	W43	P	-
GND	W44	P	-
GND	W52	P	-
GND	W54	P	-
GND	W7	P	-
GND	Y3	P	-
GND	Y48	P	-
GND	Y5	P	-
GND	Y50	P	-
GND	Y55	P	-
GND	Y8	P	-
GND_SENSE	BR48	P	-
GNDMS_SENSE	BR49	P	-
GPCADC_AVDD	BF9	P	-
GPIO0	BP2	B	+1.8V
GPIO1	BN3	B	+1.8V
GPIO10	BK4	B	+1.8V
GPIO11	BK3	B	+1.8V
GPIO12	BK2	B	+1.8V
GPIO13	BK1	B	+1.8V
GPIO14	BJ6	B	+1.8V
GPIO15	BJ5	B	+1.8V
GPIO16	BJ4	B	+1.8V
GPIO17	BJ3	B	+1.8V
GPIO18	BJ2	B	+1.8V
GPIO19	BJ1	B	+1.8V
GPIO2	BN2	B	+1.8V
GPIO20	BH1	B	+1.8V
GPIO21	BG7	B	+1.8V
GPIO22	BG6	B	+1.8V
GPIO23	BG5	B	+1.8V
GPIO24	BG4	B	+1.8V
GPIO25	BG3	B	+1.8V
GPIO26	BG2	B	+1.8V
GPIO27	BG1	B	+1.8V
GPIO28	BF1	B	+1.8V
GPIO29	BF2	B	+1.8V
GPIO3	BM4	B	+1.8V
GPIO30	BF3	B	+1.8V

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
GPIO31	BF4	B	+1.8V
GPIO32	BF5	B	+1.8V
GPIO33	BF6	B	+1.8V
GPIO34	BF7	B	+1.8V
GPIO35	BF8	B	+1.8V
GPIO4	BM3	B	+1.8V
GPIO5	BM2	B	+1.8V
GPIO6	BM1	B	+1.8V
GPIO7	BL1	B	+1.8V
GPIO8	BK6	B	+1.8V
GPIO9	BK5	B	+1.8V
I2CB_SCL	BN8	O	+1.8V
I2CB_SDA	BM8	B	+1.8V
I2CC_SCL	BM7	O	+1.8V
I2CC_SDA	BN7	B	+1.8V
I2CS_SCL	BL8	O	+1.8V
I2CS_SDA	BL7	B	+1.8V
IFP_IOVDD	BF13	P	-
IFP_IOVDD	BF14	P	-
IFP_IOVDD	BF16	P	-
IFP_IOVDD	BF17	P	-
IFP_IOVDD	BF19	P	-
IFP_IOVDD	BF20	P	-
IFP_IOVDD	BF22	P	-
IFP_IOVDD	BF23	P	-
IFP_IOVDD	BG13	P	-
IFP_IOVDD	BG14	P	-
IFP_IOVDD	BG16	P	-
IFP_IOVDD	BG17	P	-
IFP_IOVDD	BG19	P	-
IFP_IOVDD	BG20	P	-
IFP_IOVDD	BG23	P	-
IFPA_AUX_SCL	BT11	O	-
IFPA_AUX_SDA_N	BT10	B	-
IFPA_L0	BP23	O	-
IFPA_L0_N	BR23	O	-
IFPA_L1	BT23	O	-
IFPA_L1_N	BT22	O	-
IFPA_L2	BR22	O	-
IFPA_L2_N	BP22	O	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
IFPA_L3	BP20	O	-
IFPA_L3_N	BR20	O	-
IFPAB_PLLVDD	BH22	P	-
IFPAB_RSET	BH23	AI	-
IFPB_AUX_SCL	BP11	O	-
IFPB_AUX_SDA_N	BR11	B	-
IFPB_L0	BJ25	O	-
IFPB_L0_N	BK25	O	-
IFPB_L1	BL23	O	-
IFPB_L1_N	BK23	O	-
IFPB_L2	BJ22	O	-
IFPB_L2_N	BK22	O	-
IFPB_L3	BM22	O	-
IFPB_L3_N	BL22	O	-
IFPC_AUX_SCL	BL10	O	-
IFPC_AUX_SDA_N	BM10	B	-
IFPC_L0	BL20	O	-
IFPC_L0_N	BK20	O	-
IFPC_L1	BJ19	O	-
IFPC_L1_N	BK19	O	-
IFPC_L2	BM19	O	-
IFPC_L2_N	BL19	O	-
IFPC_L3	BL17	O	-
IFPC_L3_N	BK17	O	-
IFPCD_PLLVDD	BH19	P	-
IFPCD_RSET	BH20	AI	-
IFPD_AUX_SCL	BM11	O	-
IFPD_AUX_SDA_N	BL11	B	-
IFPD_L0	BT20	O	-
IFPD_L0_N	BT19	O	-
IFPD_L1	BR19	O	-
IFPD_L1_N	BP19	O	-
IFPD_L2	BP17	O	-
IFPD_L2_N	BR17	O	-
IFPD_L3	BT17	O	-
IFPD_L3_N	BT16	O	-
IFPE_AUX_SCL	BK11	O	-
IFPE_AUX_SDA_N	BJ11	B	-
IFPE_L0	BM16	O	-
IFPE_L0_N	BL16	O	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
IFPE_L1	BL14	O	-
IFPE_L1_N	BK14	O	-
IFPE_L2	BJ13	O	-
IFPE_L2_N	BK13	O	-
IFPE_L3	BM13	O	-
IFPE_L3_N	BL13	O	-
IFPEF_PLLVDD	BH16	P	-
IFPEF_RSET	BH17	AI	-
IFPF_AUX_SCL	BJ10	O	-
IFPF_AUX_SDA_N	BK10	B	-
IFPF_L0	BR16	O	-
IFPF_L0_N	BP16	O	-
IFPF_L1	BP14	O	-
IFPF_L1_N	BR14	O	-
IFPF_L2	BT14	O	-
IFPF_L2_N	BT13	O	-
IFPF_L3	BR13	O	-
IFPF_L3_N	BP13	O	-
JTAG_TCK	BP25	I	+1.8V
JTAG_TDI	BT25	I	+1.8V
JTAG_TDO	BR25	O	+1.8V
JTAG_TMS	BN25	I	+1.8V
JTAG_TRST_N	BM25	I	+1.8V
NC	AV1	NC	-
NC	AV2	NC	-
NC	BG9	NC	-
NC	BH10	NC	-
NC	BH11	NC	-
NC	BH14	NC	-
NC	BJ16	NC	-
NC	BJ7	NC	-
NC	BJ8	NC	-
NC	BK16	NC	-
NC	BN49	NC	-
NC	BP50	NC	-
NC	BR50	NC	-
NC	BR51	NC	-
NC	BT51	NC	-
NC	D50	NC	-
NC	E50	NC	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
NC	F50	NC	-
NC	G50	NC	-
NC	G6	NC	-
NC	N49	NC	-
NVJTAG_SEL	BL25	I	+1.8V
OVERT	BK7	B	+1.8V
PEX_CLKREQ_N	BP31	O	+1.8V
PEX_CVDD	BF31	P	-
PEX_CVDD	BG31	P	-
PEX_CVDD	BH31	P	-
PEX_CVDD_SENSE	BK46	P	-
PEX_DVDD	BF32	P	-
PEX_DVDD	BF34	P	-
PEX_DVDD	BF35	P	-
PEX_DVDD	BF37	P	-
PEX_DVDD	BG32	P	-
PEX_DVDD	BG34	P	-
PEX_DVDD	BG35	P	-
PEX_DVDD	BG37	P	-
PEX_DVDD	BH32	P	-
PEX_DVDD	BH34	P	-
PEX_DVDD	BH35	P	-
PEX_DVDD	BH37	P	-
PEX_HVDD	BF38	P	-
PEX_HVDD	BF40	P	-
PEX_HVDD	BF41	P	-
PEX_HVDD	BG38	P	-
PEX_HVDD	BG40	P	-
PEX_HVDD	BG41	P	-
PEX_HVDD	BG43	P	-
PEX_HVDD	BG44	P	-
PEX_HVDD	BH38	P	-
PEX_HVDD	BH40	P	-
PEX_HVDD	BH41	P	-
PEX_HVDD	BH43	P	-
PEX_HVDD	BH44	P	-
PEX_PLL_HVDD	BF43	P	-
PEX_REFCLK	BJ30	I	-
PEX_REFCLK_N	BK30	I	-
PEX_RST_N	BT30	I	+1.8V

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
PEX_RX0	BR32	I	-
PEX_RX0_N	BT32	I	-
PEX_RX1	BP33	I	-
PEX_RX1_N	BR33	I	-
PEX_RX10	BR42	I	-
PEX_RX10_N	BT42	I	-
PEX_RX11	BP43	I	-
PEX_RX11_N	BR43	I	-
PEX_RX12	BR44	I	-
PEX_RX12_N	BT44	I	-
PEX_RX13	BP45	I	-
PEX_RX13_N	BR45	I	-
PEX_RX14	BR46	I	-
PEX_RX14_N	BT46	I	-
PEX_RX15	BP47	I	-
PEX_RX15_N	BR47	I	-
PEX_RX2	BR34	I	-
PEX_RX2_N	BT34	I	-
PEX_RX3	BP35	I	-
PEX_RX3_N	BR35	I	-
PEX_RX4	BR36	I	-
PEX_RX4_N	BT36	I	-
PEX_RX5	BP37	I	-
PEX_RX5_N	BR37	I	-
PEX_RX6	BR38	I	-
PEX_RX6_N	BT38	I	-
PEX_RX7	BP39	I	-
PEX_RX7_N	BR39	I	-
PEX_RX8	BR40	I	-
PEX_RX8_N	BT40	I	-
PEX_RX9	BP41	I	-
PEX_RX9_N	BR41	I	-
PEX_TERMP	BT50	AI	-
PEX_TX0	BL31	O	-
PEX_TX0_N	BM31	O	-
PEX_TX1	BJ32	O	-
PEX_TX1_N	BK32	O	-
PEX_TX10	BL41	O	-
PEX_TX10_N	BM41	O	-
PEX_TX11	BJ42	O	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
PEX_TX11_N	BK42	O	-
PEX_TX12	BL43	O	-
PEX_TX12_N	BM43	O	-
PEX_TX13	BJ44	O	-
PEX_TX13_N	BK44	O	-
PEX_TX14	BL45	O	-
PEX_TX14_N	BM45	O	-
PEX_TX15	BL47	O	-
PEX_TX15_N	BM47	O	-
PEX_TX2	BL33	O	-
PEX_TX2_N	BM33	O	-
PEX_TX3	BJ34	O	-
PEX_TX3_N	BK34	O	-
PEX_TX4	BL35	O	-
PEX_TX4_N	BM35	O	-
PEX_TX5	BJ36	O	-
PEX_TX5_N	BK36	O	-
PEX_TX6	BL37	O	-
PEX_TX6_N	BM37	O	-
PEX_TX7	BJ38	O	-
PEX_TX7_N	BK38	O	-
PEX_TX8	BL39	O	-
PEX_TX8_N	BM39	O	-
PEX_TX9	BJ40	O	-
PEX_TX9_N	BK40	O	-
PEX_WAKE_N	BR31	B	-
ROM_CS_N	BP7	O	+1.8V
ROM_SCLK	BT7	O	+1.8V
ROM_SI	BR7	B	+1.8V
ROM_SO	BT8	B	+1.8V
RSVD	A4	RSVD	-
RSVD	A53	RSVD	-
RSVD	BN1	RSVD	-
RSVD	BN56	RSVD	-
RSVD	BT4	RSVD	-
RSVD	BT53	RSVD	-
RSVD	D1	RSVD	-
RSVD	D56	RSVD	-
SP_PLLVDD	BG22	P	-
STRAP0	BM5	I	+1.8V

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
STRAP1	BN5	I	+1.8V
STRAP2	BP4	I	+1.8V
STRAP3	BP3	I	+1.8V
STRAP4	BR3	I	+1.8V
STRAP5	BR4	I	+1.8V
THERMDN	BR8	AO	-
THERMDP	BP8	AI	-
TS_VREF	BG8	AO	-
VDD	AB14	P	-
VDD	AB15	P	-
VDD	AB16	P	-
VDD	AB17	P	-
VDD	AB18	P	-
VDD	AB19	P	-
VDD	AB20	P	-
VDD	AB21	P	-
VDD	AB22	P	-
VDD	AB23	P	-
VDD	AB24	P	-
VDD	AB25	P	-
VDD	AB26	P	-
VDD	AB27	P	-
VDD	AB28	P	-
VDD	AB29	P	-
VDD	AB30	P	-
VDD	AB31	P	-
VDD	AB32	P	-
VDD	AB33	P	-
VDD	AB34	P	-
VDD	AB35	P	-
VDD	AB36	P	-
VDD	AB37	P	-
VDD	AB38	P	-
VDD	AB39	P	-
VDD	AB40	P	-
VDD	AB41	P	-
VDD	AB42	P	-
VDD	AB43	P	-
VDD	AD14	P	-
VDD	AD15	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AD16	P	-
VDD	AD17	P	-
VDD	AD18	P	-
VDD	AD19	P	-
VDD	AD20	P	-
VDD	AD21	P	-
VDD	AD22	P	-
VDD	AD23	P	-
VDD	AD24	P	-
VDD	AD25	P	-
VDD	AD26	P	-
VDD	AD27	P	-
VDD	AD28	P	-
VDD	AD29	P	-
VDD	AD30	P	-
VDD	AD31	P	-
VDD	AD32	P	-
VDD	AD33	P	-
VDD	AD34	P	-
VDD	AD35	P	-
VDD	AD36	P	-
VDD	AD37	P	-
VDD	AD38	P	-
VDD	AD39	P	-
VDD	AD40	P	-
VDD	AD41	P	-
VDD	AD42	P	-
VDD	AD43	P	-
VDD	AF14	P	-
VDD	AF15	P	-
VDD	AF16	P	-
VDD	AF17	P	-
VDD	AF18	P	-
VDD	AF19	P	-
VDD	AF20	P	-
VDD	AF21	P	-
VDD	AF22	P	-
VDD	AF23	P	-
VDD	AF24	P	-
VDD	AF25	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AF26	P	-
VDD	AF27	P	-
VDD	AF28	P	-
VDD	AF29	P	-
VDD	AF30	P	-
VDD	AF31	P	-
VDD	AF32	P	-
VDD	AF33	P	-
VDD	AF34	P	-
VDD	AF35	P	-
VDD	AF36	P	-
VDD	AF37	P	-
VDD	AF38	P	-
VDD	AF39	P	-
VDD	AF40	P	-
VDD	AF41	P	-
VDD	AF42	P	-
VDD	AF43	P	-
VDD	AH14	P	-
VDD	AH15	P	-
VDD	AH16	P	-
VDD	AH17	P	-
VDD	AH18	P	-
VDD	AH19	P	-
VDD	AH20	P	-
VDD	AH21	P	-
VDD	AH22	P	-
VDD	AH23	P	-
VDD	AH24	P	-
VDD	AH25	P	-
VDD	AH26	P	-
VDD	AH27	P	-
VDD	AH28	P	-
VDD	AH29	P	-
VDD	AH30	P	-
VDD	AH31	P	-
VDD	AH32	P	-
VDD	AH33	P	-
VDD	AH34	P	-
VDD	AH35	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AH36	P	-
VDD	AH37	P	-
VDD	AH38	P	-
VDD	AH39	P	-
VDD	AH40	P	-
VDD	AH41	P	-
VDD	AH42	P	-
VDD	AH43	P	-
VDD	AK14	P	-
VDD	AK15	P	-
VDD	AK16	P	-
VDD	AK17	P	-
VDD	AK18	P	-
VDD	AK19	P	-
VDD	AK20	P	-
VDD	AK21	P	-
VDD	AK22	P	-
VDD	AK23	P	-
VDD	AK24	P	-
VDD	AK25	P	-
VDD	AK26	P	-
VDD	AK27	P	-
VDD	AK28	P	-
VDD	AK29	P	-
VDD	AK30	P	-
VDD	AK31	P	-
VDD	AK32	P	-
VDD	AK33	P	-
VDD	AK34	P	-
VDD	AK35	P	-
VDD	AK36	P	-
VDD	AK37	P	-
VDD	AK38	P	-
VDD	AK39	P	-
VDD	AK40	P	-
VDD	AK41	P	-
VDD	AK42	P	-
VDD	AK43	P	-
VDD	AM14	P	-
VDD	AM15	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AM16	P	-
VDD	AM17	P	-
VDD	AM18	P	-
VDD	AM19	P	-
VDD	AM20	P	-
VDD	AM21	P	-
VDD	AM22	P	-
VDD	AM23	P	-
VDD	AM24	P	-
VDD	AM25	P	-
VDD	AM26	P	-
VDD	AM27	P	-
VDD	AM28	P	-
VDD	AM29	P	-
VDD	AM30	P	-
VDD	AM31	P	-
VDD	AM32	P	-
VDD	AM33	P	-
VDD	AM34	P	-
VDD	AM35	P	-
VDD	AM36	P	-
VDD	AM37	P	-
VDD	AM38	P	-
VDD	AM39	P	-
VDD	AM40	P	-
VDD	AM41	P	-
VDD	AM42	P	-
VDD	AM43	P	-
VDD	AP14	P	-
VDD	AP15	P	-
VDD	AP16	P	-
VDD	AP17	P	-
VDD	AP18	P	-
VDD	AP19	P	-
VDD	AP20	P	-
VDD	AP21	P	-
VDD	AP22	P	-
VDD	AP23	P	-
VDD	AP24	P	-
VDD	AP25	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	AP26	P	-
VDD	AP27	P	-
VDD	AP28	P	-
VDD	AP29	P	-
VDD	AP30	P	-
VDD	AP31	P	-
VDD	AP32	P	-
VDD	AP33	P	-
VDD	AP34	P	-
VDD	AP35	P	-
VDD	AP36	P	-
VDD	AP37	P	-
VDD	AP38	P	-
VDD	AP39	P	-
VDD	AP40	P	-
VDD	AP41	P	-
VDD	AP42	P	-
VDD	AP43	P	-
VDD	P14	P	-
VDD	P15	P	-
VDD	P16	P	-
VDD	P17	P	-
VDD	P18	P	-
VDD	P19	P	-
VDD	P20	P	-
VDD	P21	P	-
VDD	P22	P	-
VDD	P23	P	-
VDD	P24	P	-
VDD	P25	P	-
VDD	P26	P	-
VDD	P27	P	-
VDD	P28	P	-
VDD	P29	P	-
VDD	P30	P	-
VDD	P31	P	-
VDD	P32	P	-
VDD	P33	P	-
VDD	P34	P	-
VDD	P35	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	P36	P	-
VDD	P37	P	-
VDD	P38	P	-
VDD	P39	P	-
VDD	P40	P	-
VDD	P41	P	-
VDD	P42	P	-
VDD	P43	P	-
VDD	T14	P	-
VDD	T15	P	-
VDD	T16	P	-
VDD	T17	P	-
VDD	T18	P	-
VDD	T19	P	-
VDD	T20	P	-
VDD	T21	P	-
VDD	T22	P	-
VDD	T23	P	-
VDD	T24	P	-
VDD	T25	P	-
VDD	T26	P	-
VDD	T27	P	-
VDD	T28	P	-
VDD	T29	P	-
VDD	T30	P	-
VDD	T31	P	-
VDD	T32	P	-
VDD	T33	P	-
VDD	T34	P	-
VDD	T35	P	-
VDD	T36	P	-
VDD	T37	P	-
VDD	T38	P	-
VDD	T39	P	-
VDD	T40	P	-
VDD	T41	P	-
VDD	T42	P	-
VDD	T43	P	-
VDD	V14	P	-
VDD	V15	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	V16	P	-
VDD	V17	P	-
VDD	V18	P	-
VDD	V19	P	-
VDD	V20	P	-
VDD	V21	P	-
VDD	V22	P	-
VDD	V23	P	-
VDD	V24	P	-
VDD	V25	P	-
VDD	V26	P	-
VDD	V27	P	-
VDD	V28	P	-
VDD	V29	P	-
VDD	V30	P	-
VDD	V31	P	-
VDD	V32	P	-
VDD	V33	P	-
VDD	V34	P	-
VDD	V35	P	-
VDD	V36	P	-
VDD	V37	P	-
VDD	V38	P	-
VDD	V39	P	-
VDD	V40	P	-
VDD	V41	P	-
VDD	V42	P	-
VDD	V43	P	-
VDD	Y14	P	-
VDD	Y15	P	-
VDD	Y16	P	-
VDD	Y17	P	-
VDD	Y18	P	-
VDD	Y19	P	-
VDD	Y20	P	-
VDD	Y21	P	-
VDD	Y22	P	-
VDD	Y23	P	-
VDD	Y24	P	-
VDD	Y25	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDD	Y26	P	-
VDD	Y27	P	-
VDD	Y28	P	-
VDD	Y29	P	-
VDD	Y30	P	-
VDD	Y31	P	-
VDD	Y32	P	-
VDD	Y33	P	-
VDD	Y34	P	-
VDD	Y35	P	-
VDD	Y36	P	-
VDD	Y37	P	-
VDD	Y38	P	-
VDD	Y39	P	-
VDD	Y40	P	-
VDD	Y41	P	-
VDD	Y42	P	-
VDD	Y43	P	-
VDD_SENSE	BT48	P	-
VDDMS	AB13	P	-
VDDMS	AB44	P	-
VDDMS	AD13	P	-
VDDMS	AD44	P	-
VDDMS	AF13	P	-
VDDMS	AF44	P	-
VDDMS	AH13	P	-
VDDMS	AH44	P	-
VDDMS	AK13	P	-
VDDMS	AK44	P	-
VDDMS	AM13	P	-
VDDMS	AM44	P	-
VDDMS	AP13	P	-
VDDMS	AP44	P	-
VDDMS	AT13	P	-
VDDMS	AT14	P	-
VDDMS	AT15	P	-
VDDMS	AT16	P	-
VDDMS	AT17	P	-
VDDMS	AT18	P	-
VDDMS	AT19	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	AT20	P	-
VDDMS	AT21	P	-
VDDMS	AT22	P	-
VDDMS	AT23	P	-
VDDMS	AT24	P	-
VDDMS	AT25	P	-
VDDMS	AT26	P	-
VDDMS	AT27	P	-
VDDMS	AT28	P	-
VDDMS	AT29	P	-
VDDMS	AT30	P	-
VDDMS	AT31	P	-
VDDMS	AT32	P	-
VDDMS	AT33	P	-
VDDMS	AT34	P	-
VDDMS	AT35	P	-
VDDMS	AT36	P	-
VDDMS	AT37	P	-
VDDMS	AT38	P	-
VDDMS	AT39	P	-
VDDMS	AT40	P	-
VDDMS	AT41	P	-
VDDMS	AT42	P	-
VDDMS	AT43	P	-
VDDMS	AT44	P	-
VDDMS	AU13	P	-
VDDMS	AU44	P	-
VDDMS	AV13	P	-
VDDMS	AV14	P	-
VDDMS	AV15	P	-
VDDMS	AV16	P	-
VDDMS	AV17	P	-
VDDMS	AV18	P	-
VDDMS	AV19	P	-
VDDMS	AV20	P	-
VDDMS	AV21	P	-
VDDMS	AV22	P	-
VDDMS	AV23	P	-
VDDMS	AV24	P	-
VDDMS	AV25	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	AV26	P	-
VDDMS	AV27	P	-
VDDMS	AV28	P	-
VDDMS	AV29	P	-
VDDMS	AV30	P	-
VDDMS	AV31	P	-
VDDMS	AV32	P	-
VDDMS	AV33	P	-
VDDMS	AV34	P	-
VDDMS	AV35	P	-
VDDMS	AV36	P	-
VDDMS	AV37	P	-
VDDMS	AV38	P	-
VDDMS	AV39	P	-
VDDMS	AV40	P	-
VDDMS	AV41	P	-
VDDMS	AV42	P	-
VDDMS	AV43	P	-
VDDMS	AV44	P	-
VDDMS	AW13	P	-
VDDMS	AW44	P	-
VDDMS	AY13	P	-
VDDMS	AY14	P	-
VDDMS	AY15	P	-
VDDMS	AY16	P	-
VDDMS	AY17	P	-
VDDMS	AY18	P	-
VDDMS	AY19	P	-
VDDMS	AY20	P	-
VDDMS	AY21	P	-
VDDMS	AY22	P	-
VDDMS	AY23	P	-
VDDMS	AY24	P	-
VDDMS	AY25	P	-
VDDMS	AY26	P	-
VDDMS	AY27	P	-
VDDMS	AY28	P	-
VDDMS	AY29	P	-
VDDMS	AY30	P	-
VDDMS	AY31	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	AY32	P	-
VDDMS	AY33	P	-
VDDMS	AY34	P	-
VDDMS	AY35	P	-
VDDMS	AY36	P	-
VDDMS	AY37	P	-
VDDMS	AY38	P	-
VDDMS	AY39	P	-
VDDMS	AY40	P	-
VDDMS	AY41	P	-
VDDMS	AY42	P	-
VDDMS	AY43	P	-
VDDMS	AY44	P	-
VDDMS	BA13	P	-
VDDMS	BA44	P	-
VDDMS	BB13	P	-
VDDMS	BB14	P	-
VDDMS	BB15	P	-
VDDMS	BB16	P	-
VDDMS	BB17	P	-
VDDMS	BB18	P	-
VDDMS	BB19	P	-
VDDMS	BB20	P	-
VDDMS	BB21	P	-
VDDMS	BB22	P	-
VDDMS	BB23	P	-
VDDMS	BB24	P	-
VDDMS	BB25	P	-
VDDMS	BB26	P	-
VDDMS	BB27	P	-
VDDMS	BB28	P	-
VDDMS	BB29	P	-
VDDMS	BB30	P	-
VDDMS	BB31	P	-
VDDMS	BB32	P	-
VDDMS	BB33	P	-
VDDMS	BB34	P	-
VDDMS	BB35	P	-
VDDMS	BB36	P	-
VDDMS	BB37	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	BB38	P	-
VDDMS	BB39	P	-
VDDMS	BB40	P	-
VDDMS	BB41	P	-
VDDMS	BB42	P	-
VDDMS	BB43	P	-
VDDMS	BB44	P	-
VDDMS	BC13	P	-
VDDMS	BC44	P	-
VDDMS	BD13	P	-
VDDMS	BD14	P	-
VDDMS	BD17	P	-
VDDMS	BD18	P	-
VDDMS	BD21	P	-
VDDMS	BD22	P	-
VDDMS	BD25	P	-
VDDMS	BD26	P	-
VDDMS	BD28	P	-
VDDMS	BD29	P	-
VDDMS	BD31	P	-
VDDMS	BD32	P	-
VDDMS	BD35	P	-
VDDMS	BD36	P	-
VDDMS	BD39	P	-
VDDMS	BD40	P	-
VDDMS	BD43	P	-
VDDMS	BD44	P	-
VDDMS	N13	P	-
VDDMS	N15	P	-
VDDMS	N17	P	-
VDDMS	N19	P	-
VDDMS	N21	P	-
VDDMS	N23	P	-
VDDMS	N25	P	-
VDDMS	N27	P	-
VDDMS	N30	P	-
VDDMS	N32	P	-
VDDMS	N34	P	-
VDDMS	N36	P	-
VDDMS	N38	P	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
VDDMS	N40	P	-
VDDMS	N42	P	-
VDDMS	N44	P	-
VDDMS	P13	P	-
VDDMS	P44	P	-
VDDMS	T13	P	-
VDDMS	T44	P	-
VDDMS	V13	P	-
VDDMS	V44	P	-
VDDMS	Y13	P	-
VDDMS	Y44	P	-
VDDMS_SENSE	BP49	P	-
VID_PLLVDD	BG25	P	-
XTAL_IN	BT5	AI	+1.8V
XTAL_OUT	BR5	AO	+1.8V
XTAL_OUTBUFF	BP5	O	+1.8V
XVDD_1	AY1	NC	-
XVDD_10	AY10	NC	-
XVDD_100	BL49	NC	-
XVDD_101	BJ47	NC	-
XVDD_102	BH46	NC	-
XVDD_103	BG45	NC	-
XVDD_104	BF44	NC	-
XVDD_105	BT55	NC	-
XVDD_106	BR54	NC	-
XVDD_107	BP53	NC	-
XVDD_108	BN52	NC	-
XVDD_109	BL50	NC	-
XVDD_11	AY11	NC	-
XVDD_110	BK49	NC	-
XVDD_111	BJ48	NC	-
XVDD_112	BH47	NC	-
XVDD_113	BG46	NC	-
XVDD_114	BR55	NC	-
XVDD_115	BP54	NC	-
XVDD_116	BN53	NC	-
XVDD_117	BM52	NC	-
XVDD_118	BL51	NC	-
XVDD_119	BK50	NC	-
XVDD_12	BA1	NC	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
XVDD_120	BJ49	NC	-
XVDD_121	BG47	NC	-
XVDD_122	BF46	NC	-
XVDD_123	BR56	NC	-
XVDD_124	BP55	NC	-
XVDD_125	BN54	NC	-
XVDD_126	BM53	NC	-
XVDD_127	BK51	NC	-
XVDD_128	BJ50	NC	-
XVDD_129	BH49	NC	-
XVDD_13	BA2	NC	-
XVDD_130	BG48	NC	-
XVDD_131	BF47	NC	-
XVDD_132	BP56	NC	-
XVDD_133	BN55	NC	-
XVDD_134	BM54	NC	-
XVDD_135	BL53	NC	-
XVDD_136	BK52	NC	-
XVDD_137	BJ51	NC	-
XVDD_138	BF48	NC	-
XVDD_139	BE47	NC	-
XVDD_14	BA3	NC	-
XVDD_140	BD46	NC	-
XVDD_15	BA4	NC	-
XVDD_16	BA5	NC	-
XVDD_17	BA6	NC	-
XVDD_18	BA7	NC	-
XVDD_19	BA8	NC	-
XVDD_2	AY2	NC	-
XVDD_20	BA9	NC	-
XVDD_21	BA10	NC	-
XVDD_22	BA11	NC	-
XVDD_23	BB2	NC	-
XVDD_24	BB4	NC	-
XVDD_25	BB6	NC	-
XVDD_26	BB8	NC	-
XVDD_27	BB10	NC	-
XVDD_28	BC1	NC	-
XVDD_29	BC2	NC	-
XVDD_3	AY3	NC	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
XVDD_30	BC3	NC	-
XVDD_31	BC4	NC	-
XVDD_32	BC5	NC	-
XVDD_33	BC6	NC	-
XVDD_34	BC7	NC	-
XVDD_35	BC8	NC	-
XVDD_36	BC9	NC	-
XVDD_37	BC10	NC	-
XVDD_38	BC11	NC	-
XVDD_39	BD1	NC	-
XVDD_4	AY4	NC	-
XVDD_40	BD2	NC	-
XVDD_41	BD3	NC	-
XVDD_42	BD4	NC	-
XVDD_43	BD5	NC	-
XVDD_44	BD6	NC	-
XVDD_45	BD7	NC	-
XVDD_46	BD8	NC	-
XVDD_47	BD9	NC	-
XVDD_48	BD10	NC	-
XVDD_49	BD11	NC	-
XVDD_5	AY5	NC	-
XVDD_50	BT26	NC	-
XVDD_51	BR26	NC	-
XVDD_52	BP26	NC	-
XVDD_53	BN26	NC	-
XVDD_54	BM26	NC	-
XVDD_55	BL26	NC	-
XVDD_56	BK26	NC	-
XVDD_57	BJ26	NC	-
XVDD_58	BH26	NC	-
XVDD_59	BG26	NC	-
XVDD_6	AY6	NC	-
XVDD_60	BF26	NC	-
XVDD_61	BR27	NC	-
XVDD_62	BN27	NC	-
XVDD_63	BL27	NC	-
XVDD_64	BJ27	NC	-
XVDD_65	BG27	NC	-
XVDD_66	BT28	NC	-

Table 4.2 GPU Signal List

Signal Name	Ball #	I/O	Drive
XVDD_67	BR28	NC	-
XVDD_68	BP28	NC	-
XVDD_69	BN28	NC	-
XVDD_7	AY7	NC	-
XVDD_70	BM28	NC	-
XVDD_71	BL28	NC	-
XVDD_72	BK28	NC	-
XVDD_73	BJ28	NC	-
XVDD_74	BH28	NC	-
XVDD_75	BG28	NC	-
XVDD_76	BF28	NC	-
XVDD_77	BT29	NC	-
XVDD_78	BR29	NC	-
XVDD_79	BP29	NC	-
XVDD_8	AY8	NC	-
XVDD_80	BN29	NC	-
XVDD_81	BM29	NC	-
XVDD_82	BL29	NC	-
XVDD_83	BK29	NC	-
XVDD_84	BJ29	NC	-
XVDD_85	BH29	NC	-
XVDD_86	BG29	NC	-
XVDD_87	BF29	NC	-
XVDD_88	BT52	NC	-
XVDD_89	BR52	NC	-
XVDD_9	AY9	NC	-
XVDD_90	BN50	NC	-
XVDD_91	BM49	NC	-
XVDD_92	BL48	NC	-
XVDD_93	BK47	NC	-
XVDD_94	BJ46	NC	-
XVDD_95	BT54	NC	-
XVDD_96	BR53	NC	-
XVDD_97	BP52	NC	-
XVDD_98	BN51	NC	-
XVDD_99	BM50	NC	-

Packaging and Mechanical Specifications

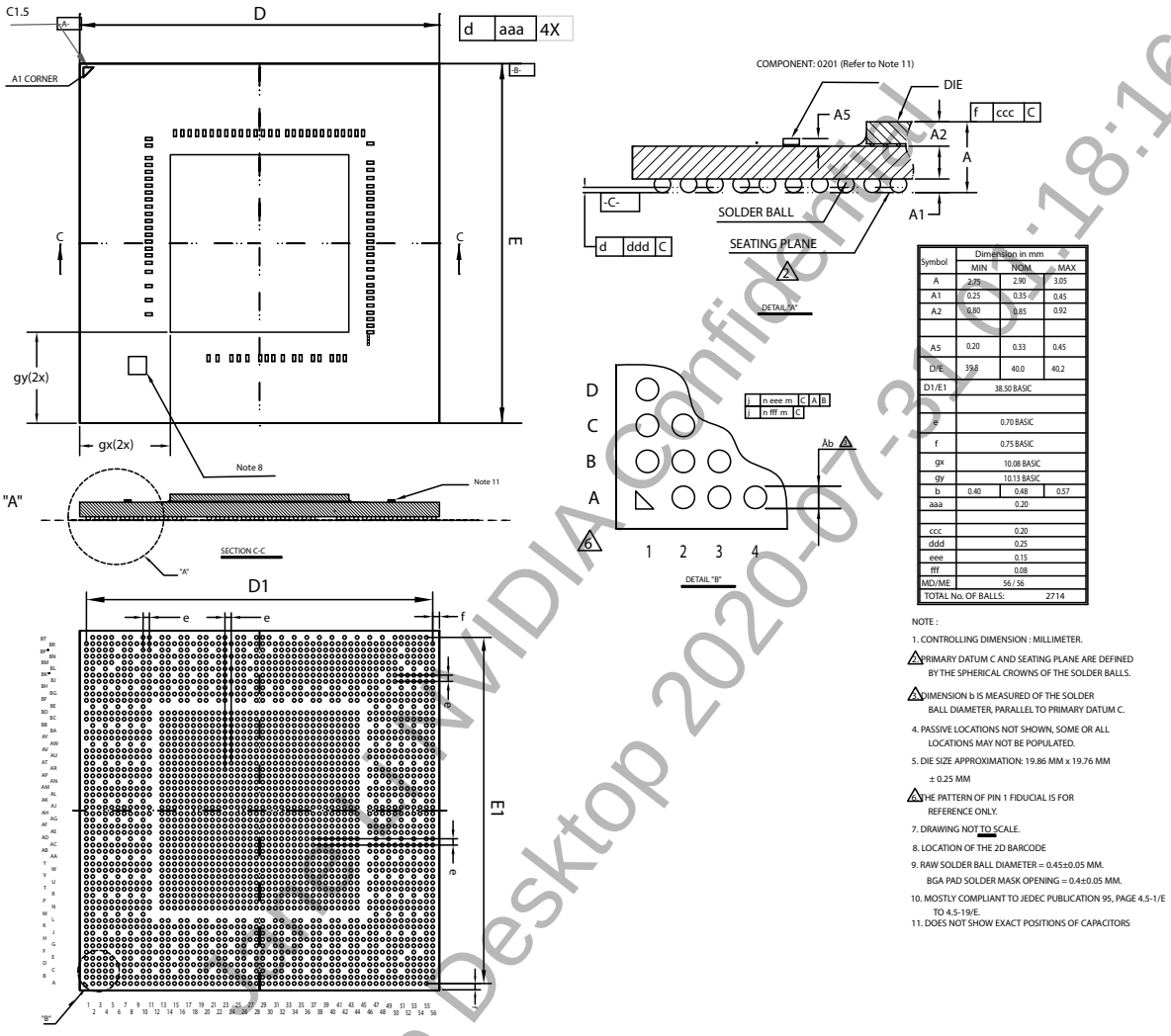
This section provides the following specifications and characteristics for this GPU.

- "Package Specifications"
- "Mechanical Specifications"
- "Environmental Conditions"

Package Specifications

Figure 5.1 shows the package specifications in a 40 mm x 40 mm FCBGA package with 2714 balls.

Figure 5.1 Package Specification



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	2.75	2.90	3.05
A1	0.25	0.35	0.45
A2	0.80	0.85	0.92
A5	0.20	0.33	0.45
D/E	39.8	40.0	40.2
D1/E1	38.50 BASIC		
e	0.70 BASIC		
f	0.75 BASIC		
gx	10.08 BASIC		
gy	10.13 BASIC		
b	0.40	0.48	0.57
aaa	0.20		
ccc	0.20		
ddd	0.25		
eee	0.15		
fff	0.08		
MD/ME	56 / 56		
TOTAL No. OF BALLS:	2714		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED OF THE SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. PASSIVE LOCATIONS NOT SHOWN, SOME OR ALL LOCATIONS MAY NOT BE POPULATED.
5. DIE SIZE APPROXIMATION: 19.86 MM x 19.76 MM ± 0.25 MM
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
7. DRAWING NOT TO SCALE.
8. LOCATION OF THE 2D BARCODE
9. RAW SOLDER BALL DIAMETER = 0.45±0.05 MM. BGA PAD SOLDER MASK OPENING = 0.4±0.05 MM.
10. MOSTLY COMPLIANT TO JEDEC PUBLICATION 95, PAGE 4.5-1/E TO 4.5-19/E.
11. DOES NOT SHOW EXACT POSITIONS OF CAPACITORS

Mechanical Specifications

Table 5.1 Mechanical Specifications

Symbol	Parameter	Min	Nominal	Max	Units	Notes
P_{cont}	Maximum allowable pressure during PCA, system assembly and operation.	-	⩽60	⩽80	psi	1
T_{reflow}	Maximum package temperature during surface mount to printed circuit board	Refer to NVIDIA specifications 630-0011-001				
e_{max}	Maximum allowable strain during PCA, system assembly or operation			⩽500	µstrains	2

Notes:

1) This specification is based on the following conditions:

a. This specification is based on solder ball deformation and die chips and cracks. Additional requirements may be needed to meet the thermal performance and/or long term reliability as to specific application,
b. When a compliant thermal interface is used between die and heat sink, the bond line thickness must have less than 20% in variation.
he pressure should be measured on the top of the die surface by an instrument equipped pressure sensors. See details in "GPU Load Distribution Measurement Application Note".
d. Nominal pressure is the total force divided by the die surface area. Since the pressure may have variations across the whole surfaces. The following additional requirement is applied:

i. The pressure has to be measured from the top of the die surface with a grid resolution of 1x1mm2 for the pressure sensor.

e. Both nominal and maximum pressure requirement must be met.

2) Strain measurement shall follow IPC-9704, particularly on following items:

a. The strain shall be measured on the top side of PCB close to the four corners of the package. A rigid PCB is assumed.

b. For generic application, the max. allowable strain must be no more than 500 µstrains for a board thickness from 1.0 to 3.2mm. A separate requirement may be specified and the qualification test should be performed if

i. A sensitive PCB laminate and build up structure is used where the pad cratering occurs at a PCB strain of 500 µstrains or below.

ii. A weak surface finish of PCB is used where cracked solder joint has been observed at a PCB strain of 500 µstrains or below.

iii. The strain rate is too high (.5000 µstrains/second) during the PCA operations.

c. For PCB thickness less than 1,0mm, the max. allowable strain shall follow IPC 9704.

Environmental Conditions

Table 5.2 Environmental Conditions

Environment	Condition
Storage temperature	-40 °C to 125 °C
Operating humidity	5% to 90% RH
Storage humidity	5% to 95% RH

Ball Map

The GPU ball map is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
A		GND	GND	RSVD	FBC_CMD1	FBC_CMD3	FBC_CMD5	FBC_CMD6	FBC_CMD8	FBC_CMD10	FBC_CMD11	FBC_CMD13	FBC_CMD15	FBC_CMD16	FBC_CMD18	FBC_CMD20	FBC_CMD21	FBC_CMD23	FBC_CMD25_NC	FBC_CMD26_NC	FBC_CMD53_NC	FBC_CMD51	FBC_CMD50	FBC_CMD48	FBC_CMD46	FBC_CMD45	FBC_CMD43	FBC_CMD41	FBC_CMD40	FBC_CMD38	FBC_CMD36	FBC_CMD35	FBC_CMD33	FBC_CMD31	FBC_CMD30	FBC_CMD28	FBB_CMD1	FBB_CMD2	FBB_CMD4	FBB_CMD6	FBB_CMD7	FBB_CMD9	FBB_CMD11	FBB_CMD12	FBB_CMD14	FBB_CMD16	FBB_CMD17	FBB_CMD19	FBB_CMD21	FBB_CMD23	FBB_CMD25_NC	FBB_CMD54_NC	RSVD	GND	GND	
B	GND	GND	FBC_DQS_WP1	FBC_D13	FBC_CMD0	GND	FBC_CMD4	GND	GND	FBC_CMD9	GND	GND	FBC_CMD14	GND	GND	FBC_CMD19	GND	GND	FBC_CMD24	FBC_CMD27	GND	FBC_CMD52	FBC_CMD55	GND	FBC_CMD47	GND	GND	FBC_CMD42	GND	GND	FBC_CMD37	GND	GND	FBC_CMD32	GND	GND	FBB_CMD0	GND	GND	FBB_CMD5	GND	GND	FBB_CMD10	GND	GND	FBB_CMD15	GND	GND	FBB_CMD20	FBB_CMD22	GND	FBB_CMD26_NC	FBB_CMD53_NC	FBB_CMD52	GND	GND
C	GND	FBC_D10	FBC_D12	GND	FBC_CMD2		GND	FBC_D6		GND	FBC_D26		GND	FBC_D18		GND	FBC_D22		GND	FBC_D50		GND	FBC_D58		GND	FBC_D36		GND	FBC_DQS_WP4		GND	FBC_DQS_WP5		GND	FBB_DQS_WP1		GND	FBB_DQS_WP0		GND	FBB_D25		GND	FBB_D29		GND	FBB_D21		FBB_D23	FBB_CMD24		FBB_CMD27	FBB_D49	FBB_D50	FBB_D51	GND
D	RSVD	FBC_D8	FBC_D11	GND	FBC_D15	GND	FBC_DQS_WP0	FBC_CMD7	GND	FBC_D7	FBC_CMD12	GND	FBC_DQS_WP3	FBC_CMD17	GND	FBC_DQS_WP2	FBC_CMD22	GND	FBC_DQS_WP6	FBC_CMD54_NC	GND	FBC_D59	FBC_CMD49	GND	FBC_DQS_WP7	FBC_CMD44	GND	FBC_D35	FBC_CMD39	GND	FBC_D44	FBC_CMD34	GND	FBB_D10	FBC_CMD29	GND	FBB_D0	FBB_CMD3	GND	FBB_D7	FBB_CMD8	GND	FBB_DQS_WP3	FBB_CMD13	GND	FBB_DQS_WP2	FBB_CMD18	GND	GND	NC	GND	FBB_D48	GND	FBB_D53	FBB_D52	RSVD
E	FBC_D9	GND	FBC_DQM1	FBC_D14	GND		GND	FBC_D5		GND	FBC_D27		GND	FBC_D17		GND	FBC_D20		GND	FBC_D52		GND	FBC_D60		GND	FBC_D33		GND	FBC_D37		GND	FBC_D46		GND	FBB_D12		GND	FBB_D5		GND	FBB_D26		GND	FBB_D17		FBB_D20	FBB_D22		FBB_DQM6	NC		GND	FBB_DQS_WP6	FBVDDQ_SENSE	FBB_CMD55	FBB_CMD51
F	GND	GND		GND		GND	FBC_D0	FBC_D2	GND	FBC_D24	FBC_D28	GND	FBC_D29	FBC_D30	GND	FBC_D21	FBC_D16	GND	FBC_D48	FBC_D53	GND	FBC_D57	FBC_D61	GND	FBC_D62	FBC_D32	GND	FBC_D38	FBC_DQM4	GND	FBC_D40	FBC_DQM5	GND	FBB_D8	FBB_DQM1	GND	FBB_D3	FBB_DQM0	GND	FBB_D6	FBB_D27	GND	FBB_D28	FBB_D19	GND	FBB_D18	GND	GND	FBB_D55	NC	GND		GND		GND	FBB_D54
G	FBD_CMD29	FBD_CMD28	FBD_CMD30	GND	FBC_D3	NC	FBC_DQM0	GND		FBC_D25	GND		FBC_DQM3	GND		FBC_DQM2	GND		FBC_DQM6	GND		FBC_D56	GND		FBC_DQM7	GND		FBC_D39	GND		FBC_D45	GND		FBB_D11	GND		FBB_D2	GND		FBB_D24	GND		FBB_DQM3	GND		FBB_DQM2	FBB_D16		GND	NC	FBB_D59	GND	FBB_D56	GND	FBB_CMD50	FBB_CMD49
H	FBD_CMD31	FBD_CMD32	GND	GND	FBC_D1	GND	GND	FBC_D4	GND	GND	FBC_D31	GND	GND	FBC_D19	GND	GND	FBC_D23	GND	GND	FBC_D55	GND	GND	FBC_D63	GND	GND	FBC_D34	GND	GND	FBC_D42	GND	FBC_D47	GND	GND	GND	FBB_D14	GND	GND	FBB_D4	GND	GND	FBB_D30	GND	GND	FBB_D31	GND	GND	GND	GND	FBB_D57	GND	FBB_D58	FBB_D60	FBB_CMD47	FBB_D61	GND	FBB_CMD48
J	FBD_CMD33	FBD_D46		GND		GND		GND		GND	FBC_WCKB01_N		FBC_WCK01_N	FBC_WCKB23		FBC_WCK23	GND		FBC_D51	GND		FBC_CLK0_N	FBC_CLK1_N		FBC_WCK67_N	FBC_WCKB67		FBC_D43	GND		FBC_WCK45_N	FBC_WCKB45_N		FBB_D9	GND		FBB_D1	FBB_WCKB01_N		FBB_WCK01	FBB_WCKB23_N		FBB_WCK23	FBB_CLK0_N		FBB_CLK1	FBB_WCK67_N		GND		GND		GND		GND	FBB_CMD46
K	FBD_CMD35	FBD_CMD36	FBD_D44	FBD_CMD34	FBD_D45	FBD_D42	GND	FBD_D47	GND	FBVDDQ	FBC_WCKB01	GND	FBC_WCK01	FBC_WCKB23_N	GND	FBC_WCK23_N	FBC_D49	GND	GND	FBC_D54	GND	FBC_CLK0	FBC_CLK1	GND	FBC_WCK67	FBC_WCKB67_N	GND	GND	FBC_D41	GND	FBC_WCK45	FBC_WCKB45	GND	FBB_D13	FBB_D15	GND	GND	FBB_WCKB01	GND	FBB_WCK01_N	FBB_WCKB23	GND	FBB_WCK23_N	FBB_CLK0	GND	FBB_CLK1_N	FBB_WCK67	FBB_D62	GND	FBB_DQM7	FBB_D63	GND	FBB_DQS_WP7	GND	FBB_CMD45	FBB_CMD44
L	FBD_CMD37	FBD_CMD38	GND	FBD_DQS_WP5	GND	FBD_D40	FBD_DQM5	GND	FBD_D43	GND	FBVDDQ		FBVDDQ	FBVDDQ		FBVDDQ	FB_PLLVDD		FBVDDQ	FBVDDQ		FBVDDQ	FBVDDQ		FBVDDQ	FBVDDQ		FBVDDQ	FBVDDQ		FBVDDQ	FBVDDQ		FBVDDQ	FB_PLLVDD		FBVDDQ	FBVDDQ		FBVDDQ	FBVDDQ		FBVDDQ	FBVDDQ		FBVDDQ	FBB_WCKB67	FBB_WCKB67_N	FBB_D35	GND	FBB_D32	FBB_D33	FBB_CMD42	FBB_D36	GND	FBB_CMD43
M	FBD_CMD39	GND		GND		GND		GND		GND																																					GND		GND		GND		GND		GND	FBB_CMD41
N	FBD_CMD41	GND	FBD_D38	FBD_CMD40	FBD_D37	FBD_D39	GND	FBD_D41	FBD_WCKB45_N	FBD_WCKB45	FBVDDQ		VDDMS	GND	VDDMS	GND	VDDMS	GND	VDDMS	GND	VDDMS	GND	VDDMS	GND	VDDMS	GND	VDDMS	GND	GND	VDDMS	GND	VDDMS	GND	VDDMS	GND	VDDMS	GND	VDDMS	GND	VDDMS	GND	VDDMS	GND	VDDMS		FBVDDQ	FBB_D37	GND	NC	FBB_DQM4	FBB_D34	GND	FBB_DQS_WP4	GND	FBB_CMD40	FBB_CMD39
P	FBD_CMD42	FBD_CMD43	GND	FBD_DQS_WP4	GND	FBD_D34	FBD_DQM4	GND	FBD_WCK45_N	FBD_WCK45	FBVDDQ		VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS		FBVDDQ	FBB_WCK45	FBB_WCK45_N	FBB_D39	GND	FBB_D38	FBB_D41	FBB_CMD37	FBB_D42	GND	FBB_CMD38
R	FBD_CMD44	GND		GND		GND		GND		GND			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND		GND		GND		GND		GND	FBB_CMD36
T	FBD_CMD46	GND	FBD_D36	FBD_CMD45	FBD_D32	FBD_D33	GND	FBD_D35	GND	FBD_D63	FBVDDQ		VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS		FB_PLLVDD	FBB_WCKB45_N	FBB_WCKB45	GND	FBB_DQM5	FBB_D40	GND	FBB_DQS_WP5	GND	FBB_CMD35	FBB_CMD34
U	FBD_CMD47	FBD_CMD48	GND	FBD_DQS_WP7	GND	FBD_D62	FBD_DQM7	GND	FBD_D61	GND	FBVDDQ		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		FBVDDQ	FBB_D43	GND	FBB_D47	GND	FBB_D44	FBB_D45	FBB_CMD32	FBB_D46	GND	FBB_CMD33
V	FBD_CMD49	GND		GND		GND		GND		GND			VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS			GND		GND		GND		GND		GND	FBB_CMD31
W	FBD_CMD51	FBD_CMD55	FBD_D60	FBD_CMD50	FBD_D58	FBD_D56	GND	FBD_D57	FBD_WCKB67	FBD_WCKB67_N	FBVDDQ		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		FBVDDQ	FB_CAL_PD_VDDQ	CAL_TERM_G	FB_VREF	FBA_D9	FBA_D8	GND	FBA_D10	GND	FBB_CMD30	FBB_CMD29
Y	FBD_CMD52	FBD_CMD53_NC	GND	FBD_DQS_WP6	GND	FBD_D59	FBD_DQM6	GND	FBD_WCK67_N	FBD_WCK67	FBVDDQ		VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS		FBVDDQ	B_CAL_PU_GN	GND	FBA_D14	GND	FBA_D13	FBA_D12	FBA_CMD0	FBA_D11	GND	FBB_CMD28
AA	FBD_CMD54_NC	GND		GND		GND		GND		GND			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND		GND		GND		GND		GND	FBA_CMD1
AB	FBD_CMD25_NC	FBD_CMD27	FBD_D52	FBD_CMD26_NC	FBD_D53	FBD_D54	GND	FBD_D55	FBD_CLK1_N	FBD_CLK1	FBVDDQ		VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS		FBVDDQ	GND	FBA_D1	GND	FBA_DQM1	FBA_D15	GND	FBA_DQS_WP1	GND	FBA_CMD2	FBA_CMD3
AC	FBD_CMD24	FBD_CMD23	GND	FBD_D51	GND	FBD_D50	FBD_D48	GND	FBD_CLK0_N	FBD_CLK0	FBVDDQ		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		FB_PLLVDD	FBA_WCKB01_N	FBA_WCKB01	FBA_D3	GND	FBA_D0	FBA_D2	FBA_CMD5	FBA_D5	GND	FBA_CMD4
AD	FBD_CMD22	GND		GND		GND		GND		GND			VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS			GND		GND		GND		GND		GND	FBA_CMD6
AE	FBD_CMD20	GND	FBD_D49	FBD_CMD21	FBD_D22	FBD_D20	GND	FBD_D21	GND	FBD_D23	FB_PLLVDD		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		FBVDDQ	FBA_WCK01_N	FBA_WCK01	GND	FBA_DQM0	FBA_D6	GND	FBA_DQS_WP0	GND	FBA_CMD7	FBA_CMD8
AF	FBD_CMD19	FBD_CMD18	GND	FBD_DQS_WP2	GND	FBD_D16	FBD_DQM2	GND	FBD_D19	GND	FBVDDQ		VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS		FBVDDQ	FBA_D27	GND	FBA_D25	GND	FBA_D7	FBA_D4	FBA_CMD10	FBA_D24	GND	FBA_CMD9
AG	FBD_CMD17	GND		GND		GND		GND		GND			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND		GND		GND		GND		GND	FBA_CMD11
AH	FBD_CMD15	GND	FBD_D18	FBD_CMD16	FBD_D17	FBD_D30	GND	FBD_D31	FBD_WCK23_N	FBD_WCK23	FBVDDQ		VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS		FBVDDQ	GND	FBA_D30	GND	FBA_DQM3	FBA_D26	GND	FBA_DQS_WP3	GND	FBA_CMD12	FBA_CMD13
AJ	FBD_CMD14	FBD_CMD13	GND	FBD_DQS_WP3	GND	FBD_D28	FBD_DQM3	GND	FBD_WCKB23_N	FBD_WCKB23	FBVDDQ		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		FBVDDQ	FBA_WCKB23_N	FBA_WCKB23	FBA_D31	GND	FBA_D29	FBA_D28	FBA_CMD15	FBA_D19	GND	FBA_CMD14
AK	FBD_CMD12	GND		GND		GND		GND		GND			VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS			GND		GND		GND		GND		GND	FBA_CMD16
AL	FBD_CMD10	GND	FBD_D25	FBD_CMD11	FBD_D26	FBD_D24	GND	FBD_D27	GND	FBD_D29	FBVDDQ		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		FBVDDQ	FBA_WCK23_N	FBA_WCK23	GND	FBA_DQM2	FBA_D17	GND	FBA_DQS_WP2	GND	FBA_CMD17	FBA_CMD18
AM	FBD_CMD9	FBD_CMD8	GND	FBD_DQS_WP0	GND	FBD_D4	FBD_DQM0	GND	FBD_D7	GND	FBVDDQ		VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS		FBVDDQ	FBA_D20	GND	FBA_D23	GND	FBA_D21	FBA_D18	FBA_CMD20	FBA_D16	GND	FBA_CMD19
AN	FBD_CMD7	GND		GND		GND		GND		GND			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND		GND		GND		GND		GND	FBA_CMD21
AP	FBD_CMD5	GND	FBD_D5	FBD_CMD6	FBD_D6	FBD_D2	GND	FBD_D1	FBD_WCK01	FBD_WCK01_N	FBVDDQ		VDDMS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDMS		FB_PLLVDD	FBA_CLK0_N	FBA_CLK0	GND	FBA_D22	FBA_D48	GND	FBA_D49	GND	FBA_CMD22	FBA_CMD23
AR	FBD_CMD4	FBD_CMD3	GND	FBD_D0	GND	FBD_D3	FBD_D15	GND	FBD_WCKB01	FBD_WCKB01_N	FBVDDQ		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		FBVDDQ	FBA_CLK1_N	FBA_CLK1	FBA_D55	GND	FBA_D53	FBA_D50	FBA_CMD25_NC	FBA_D51	FBA_CMD27	FBA_CMD24
AT	FBD_CMD2	GND		GND		GND		GND		GND			VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS			GND		GND		GND		GND		GND	FBA_CMD26_NC
AU	FBD_CMD0	GND	FBD_D11	FBD_CMD1	FBD_D8	FBD_D12	GND	FBD_D13	GND	FBD_D14	FBVDDQ		VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS		FBVDDQ	FBA_WCK67_N	FBA_WCK67	GND	FBA_DQM6	FBA_D52	GND	FBA_DQS_WP6	GND	FBA_CMD54_NC	FBA_CMD53_NC
AV	NC	NC	GND	FBD_DQS_WP1	GND	FBD_D9	FBD_DQM1	GND	FBD_D10	GND	FBVDDQ		VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS		FBVDDQ	FBA_WCKB67_N	FBA_WCKB67	FBA_D56	GND	FBA_D54	FBA_D59	FBA_CMD51	FBA_D57	FBA_CMD55	FBA_CMD52
AW		GND		GND		GND		GND		GND			VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS			GND		GND		GND		GND		GND	FBA_CMD50
AY	XVDD_1	XVDD_2	XVDD_3	XVDD_4	XVDD_5	XVDD_6	XVDD_7	XVDD_8	XVDD_9	XVDD_10	XVDD_11		VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS		FBVDDQ	GND	FBA_D60	GND	FBA_DQM7	FBA_D58	GND	FBA_DQS_WP7	GND	FBA_CMD49	FBA_CMD48
BA	XVDD_12	XVDD_13	XVDD_14	XVDD_15	XVDD_16	XVDD_17	XVDD_18	XVDD_19	XVDD_20	XVDD_21	XVDD_22		VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS		FBVDDQ	FBA_WCK45	FBA_WCK45_N	FBA_D32	GND	FBA_D63	FBA_D62	FBA_CMD46	FBA_D61	GND	FBA_CMD47
BB		XVDD_23		XVDD_24		XVDD_25		XVDD_26		XVDD_27			VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS	VDDMS			GND		GND		GND		GND		GND	FBA_CMD45
BC	XVDD_28	XVDD_29	XVDD_30	XVDD_31	XVDD_32	XVDD_33	XVDD_34	XVDD_35	XVDD_36	XVDD_37	XVDD_38		VDDMS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDMS		FBVDDQ	FBA_WCKB45_N	FBA_WCKB45	GND	FBA_DQM4	FBA_D36	GND	FBA_DQS_WP4	GND	FBA_CMD44	FBA_CMD43
BD	XVDD_39	XVDD_40	XVDD_41	XVDD_42	XVDD_43	XVDD_44	XVDD_45	XVDD_46	XVDD_47	XVDD_48	XVDD_49		VDDMS	VDDMS	GND	GND	VDDMS	VDDMS	GND	GND	VDDMS	VDDMS	GND	GND	VDDMS	VDDMS	GND	VDDMS	VDDMS	GND	VDDMS	VDDMS	GND	GND	VDDMS	VDDMS	GND	GND	VDDMS	VDDMS	GND	GND	VDDMS	VDDMS		XVDD_140	FBA_D33	GND	FBA_D39	GND	FBA_D37	FBA_D35	FBA_CMD41	FBA_D34	GND	FBA_CMD42
BE		GND		GND		GND		GND		GND																																					XVDD_139		GND		GND		GND		GND	FBA_CMD40
BF	GPIO28	GPIO29	GPIO30	GPIO31	GPIO32	GPIO33	GPIO34	GPIO35	GPCADC_AVDD	1V8	1V8		IFP_IOVDD	IFP_IOVDD		IFP_IOVDD	IFP_IOVDD		IFP_IOVDD	IFP_IOVDD		IFP_IOVDD	IFP_IOVDD		CORE_PLL_AVDD	XVDD_60		XVDD_76	XVDD_87		PEX_CVDD	PEX_DVDD		PEX_DVDD	PEX_DVDD		PEX_DVDD	PEX_HVDD		PEX_HVDD	PEX_HVDD		PEX_PLL_HVDD	XVDD_104		XVDD_122	XVDD_131	XVDD_138	FBA_D43	FBA_DQM5	FBA_D38	GND	FBA_DQS_WP5	GND	FBA_CMD39	FBA_CMD38
BG	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	TS_VREF	NC	1V8	1V8	GND	IFP_IOVDD	IFP_IOVDD	GND	IFP_IOVDD	IFP_IOVDD	GND	IFP_IOVDD	IFP_IOVDD	GND	SP_PLLVDD	IFP_IOVDD	GND	VID_PLLVDD	XVDD_59	XVDD_65	XVDD_75	XVDD_86	GND	PEX_CVDD	PEX_DVDD	GND	PEX_DVDD	PEX_DVDD	GND	PEX_DVDD	PEX_HVDD	GND	PEX_HVDD	PEX_HVDD	GND	PEX_HVDD	PEX_HVDD	XVDD_103	XVDD_113	XVDD_121	XVDD_130	GND	FBA_D45	FBA_D41	FBA_D40	FBA_CMD36	FBA_D42	GND	FBA_CMD37
BH	GPIO20	GND		GND		GND		GND		NC	NC		GND	NC		IFPEF_PLLVDD	IFPEF_RSET		IFPCD_PLLVDD	IFPCD_RSET		IFPAB_PLLVDD	IFPAB_RSET		FUSE_SRC	XVDD_58		XVDD_74	XVDD_85		PEX_CVDD	PEX_DVDD		PEX_DVDD	PEX_DVDD		PEX_DVDD	PEX_HVDD		PEX_HVDD	PEX_HVDD		PEX_HVDD	PEX_HVDD		XVDD_102	XVDD_112		XVDD_129		GND		GND		GND	FBA_CMD35
BJ	GPIO19	GPIO18	GPIO17	GPIO16	GPIO15	GPIO14	NC	NC	GND	FPF_AUX_SC	PE_AUX_SDA	GND	IFPE_L2	GND	GND	NC	GND	GND	IFPC_L1	GND	GND	IFPB_L2	GND	GND	IFPB_L0	XVDD_57	XVDD_64	XVDD_73	XVDD_84	PEX_REFCLK	GND	PEX_TX1	GND	PEX_TX3	GND	PEX_TX5	GND	PEX_TX7	GND	PEX_TX9	GND	PEX_TX11	GND	PEX_TX13	GND	XVDD_94	XVDD_101	XVDD_111	XVDD_120	XVDD_128	XVDD_137	FBA_D46	GND	FBA_D44	FBA_CMD34	FBA_CMD33
BK	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	OVERT	EXT_REFCLK_FL		PF_AUX_SDA	FPE_AUX_SC		IFPE_L2_N	IFPE_L1_N		NC	IFPC_L3_N		IFPC_L1_N	IFPC_L0_N		IFPB_L2_N	IFPB_L1_N		IFPB_L0_N	XVDD_56		XVDD_72	XVDD_83	PEX_REFCLK_N	GND	PEX_TX1_N	GND	PEX_TX3_N	GND	PEX_TX5_N	GND	PEX_TX7_N	GND	PEX_TX9_N	GND	PEX_TX11_N	GND	PEX_TX13_N	GND	PEX_CVDD_SENSE	XVDD_93		XVDD_110	XVDD_119	XVDD_127	XVDD_136	FBA_D47	GND	FBA_CMD31	FBA_CMD32
BL	GPIO7	GND		GND		GND	I2CS_SDA	I2CS_SCL	GND	FPC_AUX_SC	PD_AUX_SDA	GND	IFPE_L3_N	IFPE_L1	GND	IFPE_L0_N	IFPC_L3	GND	IFPC_L2_N	IFPC_L0	GND	IFPB_L3_N	IFPB_L1	GND	NVJTAG_SEL	XVDD_55	XVDD_63	XVDD_71	XVDD_82	GND	PEX_TX0	GND	PEX_TX2	GND	PEX_TX4	GND	PEX_TX6	GND	PEX_TX8	GND	PEX_TX10	GND	PEX_TX12	GND	PEX_TX14	GND	PEX_TX15	XVDD_92	XVDD_100	XVDD_109	XVDD_118		XVDD_135		GND	FBA_CMD30
BM	GPIO6	GPIO5	GPIO4	GPIO3	STRAP0		I2CC_SCL	I2CB_SDA		PC_AUX_SDA	FPD_AUX_SC		IFPE_L3	GND		IFPE_L0	GND		IFPC_L2	GND		IFPB_L3	GND		JTAG_TRST_N	XVDD_54		XVDD_70	XVDD_81	GND	PEX_TX0_N	GND	PEX_TX2_N	GND	PEX_TX4_N	GND	PEX_TX6_N	GND	PEX_TX8_N	GND	PEX_TX10_N	GND	PEX_TX12_N	GND	PEX_TX14_N	GND	PEX_TX15_N	GND	XVDD_91	XVDD_99		XVDD_117	XVDD_126	XVDD_134	FBA_CMD29	FBA_CMD28
BN	RSVD	GPIO2	GPIO1	GND	STRAP1	GND	I2CC_SDA	I2CB_SCL	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	JTAG_TMS	XVDD_53	XVDD_62	XVDD_69	XVDD_80	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	NC	XVDD_90	XVDD_98	XVDD_108	XVDD_116	XVDD_125	XVDD_133	RSVD
BP	GND	GPIO0	STRAP3	STRAP2	TAL_OUTBUF		ROM_CS_N	THERMDP		ADC_IN	FPB_AUX_SC		IFPF_L3_N	IFPF_L1		IFPF_L0_N	IFPD_L2		IFPD_L1_N	IFPA_L3		IFPA_L2_N	IFPA_L0		JTAG_TCK	XVDD_52		XVDD_68	XVDD_79		PEX_CLKREQ_N	GND	PEX_RX1	GND	PEX_RX3	GND	PEX_RX5	GND	PEX_RX7	GND	PEX_RX9	GND	PEX_RX11	GND	PEX_RX13	GND	PEX_RX15	GND	VDDMS_SENSE	NC		XVDD_97	XVDD_107	XVDD_115	XVDD_124	XVDD_132
BR	GND	GND	STRAP4	STRAP5	XTAL_OUT	GND	ROM_SI	THERMDN	GND	ADC_IN_N	PB_AUX_SDA	GND	IFPF_L3	IFPF_L1_N	GND	IFPF_L0	IFPD_L2_N	GND	IFPD_L1	IFPA_L3_N	GND	IFPA_L2	IFPA_L0_N	GND	JTAG_TDO	XVDD_51	XVDD_61	XVDD_67	XVDD_78	GND	PEX_WAKE_	PEX_RX0	PEX_RX1_N	PEX_RX2	PEX_RX3_N	PEX_RX4	PEX_RX5_N	PEX_RX6	PEX_RX7_N	PEX_RX8	PEX_RX9_N	PEX_RX10	PEX_RX11_N	PEX_RX12	PEX_RX13_N	PEX_RX14	PEX_RX15_N	GND_SENSE	GNDMS_SENSE	NC	NC	XVDD_89	XVDD_96	XVDD_106	XVDD_114	XVDD_123
BT		GND	GND	RSVD	XTAL_IN		ROM_SCLK	ROM_SO		PA_AUX_SDA	FPA_AUX_SC		IFPF_L2_N	IFPF_L2		IFPD_L3_N	IFPD_L3		IFPD_L0_N	IFPD_L0		IFPA_L1_N	IFPA_L1		JTAG_TDI	XVDD_50		XVDD_66	XVDD_77	PEX_RST_N		PEX_RX0_N		PEX_RX2_N		PEX_RX4_N		PEX_RX6_N		PEX_RX8_N		PEX_RX10_N		PEX_RX12_N		PEX_RX14_N		VDD_SENSE		PEX_TERMP	NC	XVDD_88	RSVD	XVDD_95	XVDD_105	

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