P1041-B01 GF104

GF104-300, 768MB/1536MB, GDDR5 192b 32M/64Mx32
DVI-I-DL, DVI-I-DL/DP, mHDMI

Table of Contents:

變更記錄

P3，C55 change to 1206 10u
P4~P14，add 跳頁&'<>'符號
P14,刪除所有網絡線
P17，add 6262 IC
P25,刪除原公版U2 & J501. 把I2CC接到6262IC
P27,接PS1_1V05_FB到6262,U4 foot_print 改爲十字的
P28,改U8的FB接法，換L6爲L04-22A8011-L65
P29，core部份PWM換UP6213+6284，OFS電壓開關抬50mV。頻率def400KHz，開關抬到600KHz.
P30-31，加driver IC 6284；去掉3顆input 電容；同時增加6個LED燈，增加CP1~CP12；爲精簡線路，刪除L mos端與DRVL 0OHm電阻，刪除CSP，CSN 0Ω電阻；更換MOS & 電感；power前4相由PEX6_F1提供，后2相由PEX6_F2提供；電容部份保留公版。
P32,去除input 端12V 的LB電感
P33,加防彎條mec100，加6個十字光學點，加NVVDD，FBVDD &pex_vdd的測試點, 增加阻抗條

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11041-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-11041-0000-300	P1041 GF104-300 768MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
2	SKU0010	600-11041-0010-300	P1041 GF104-350 1024MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
3	QS1	600-11041-0000-QS1	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
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PAGE DETAIL	Title

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
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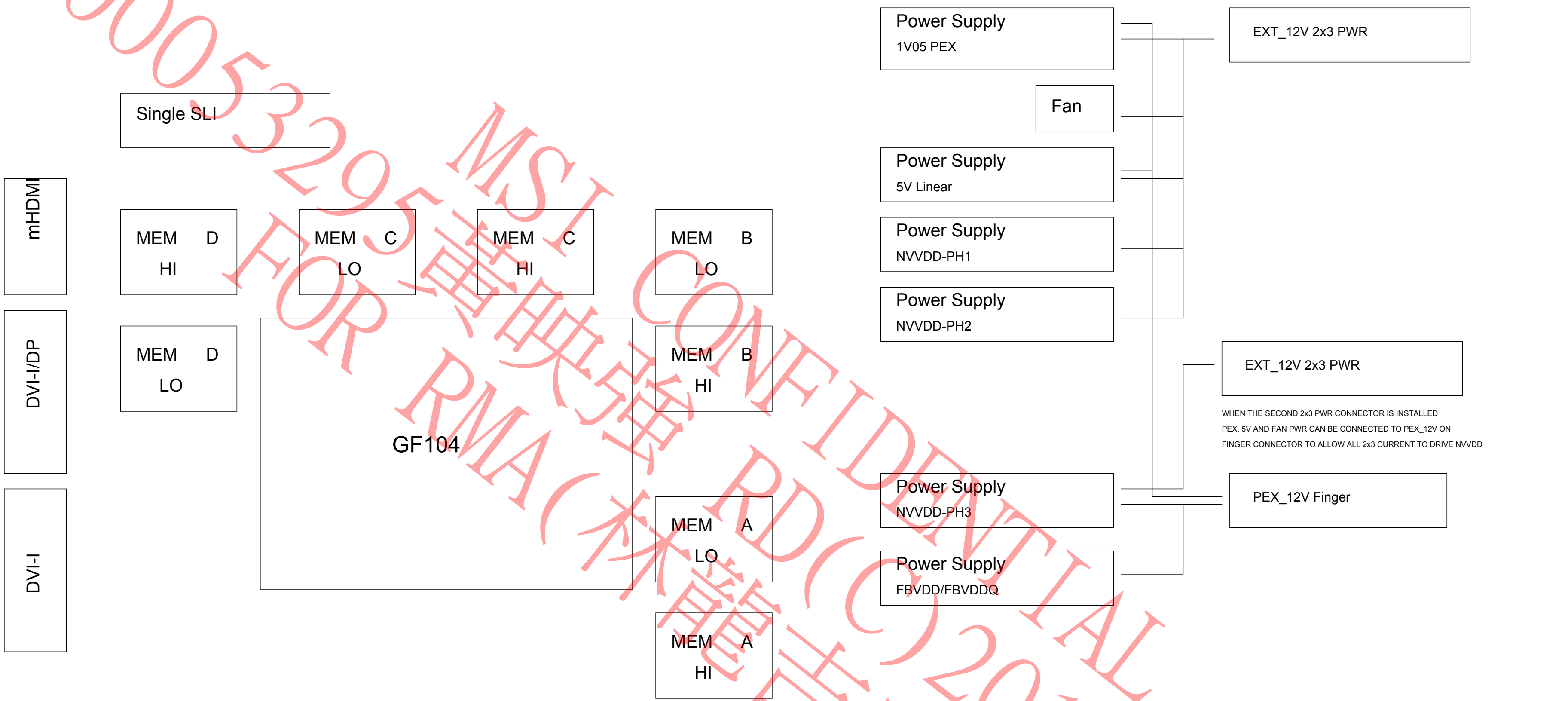
NV_PN	600-11041-BASE-000		
PCB REV	P1041-B01	PAGE	
BOM REV	A	DATE	12-MAY-2010

Page2: Block Diagram



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PAGE DETAIL	Block Diagram

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Page3: PCI Express

PEX NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	24MIL
3V3	3.3V	3.0A	20MIL
GND	0V	8.5A	16MIL

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express

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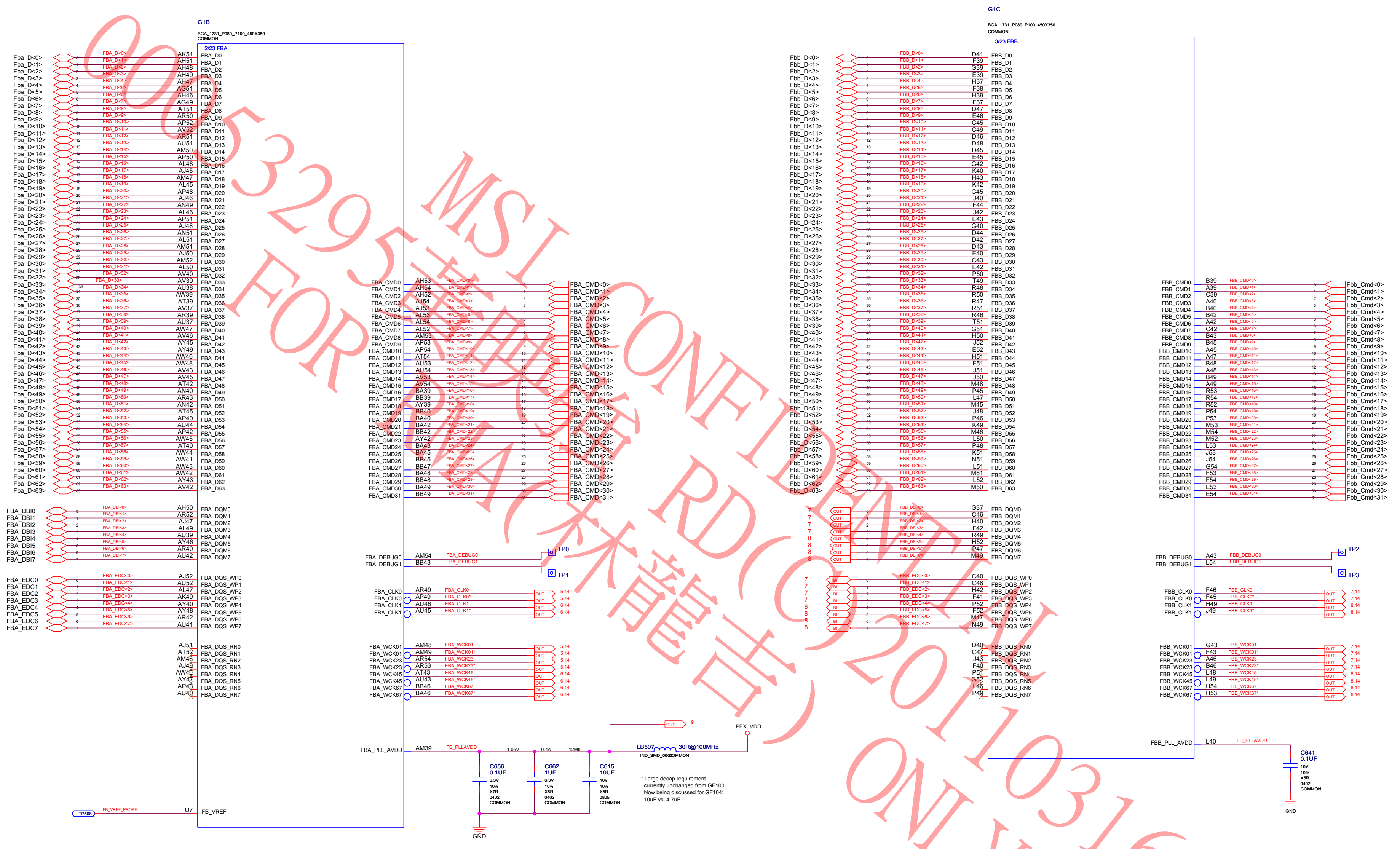
Page4: GPU Partition A/B



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PAGE DETAIL	GPU Partition A/B

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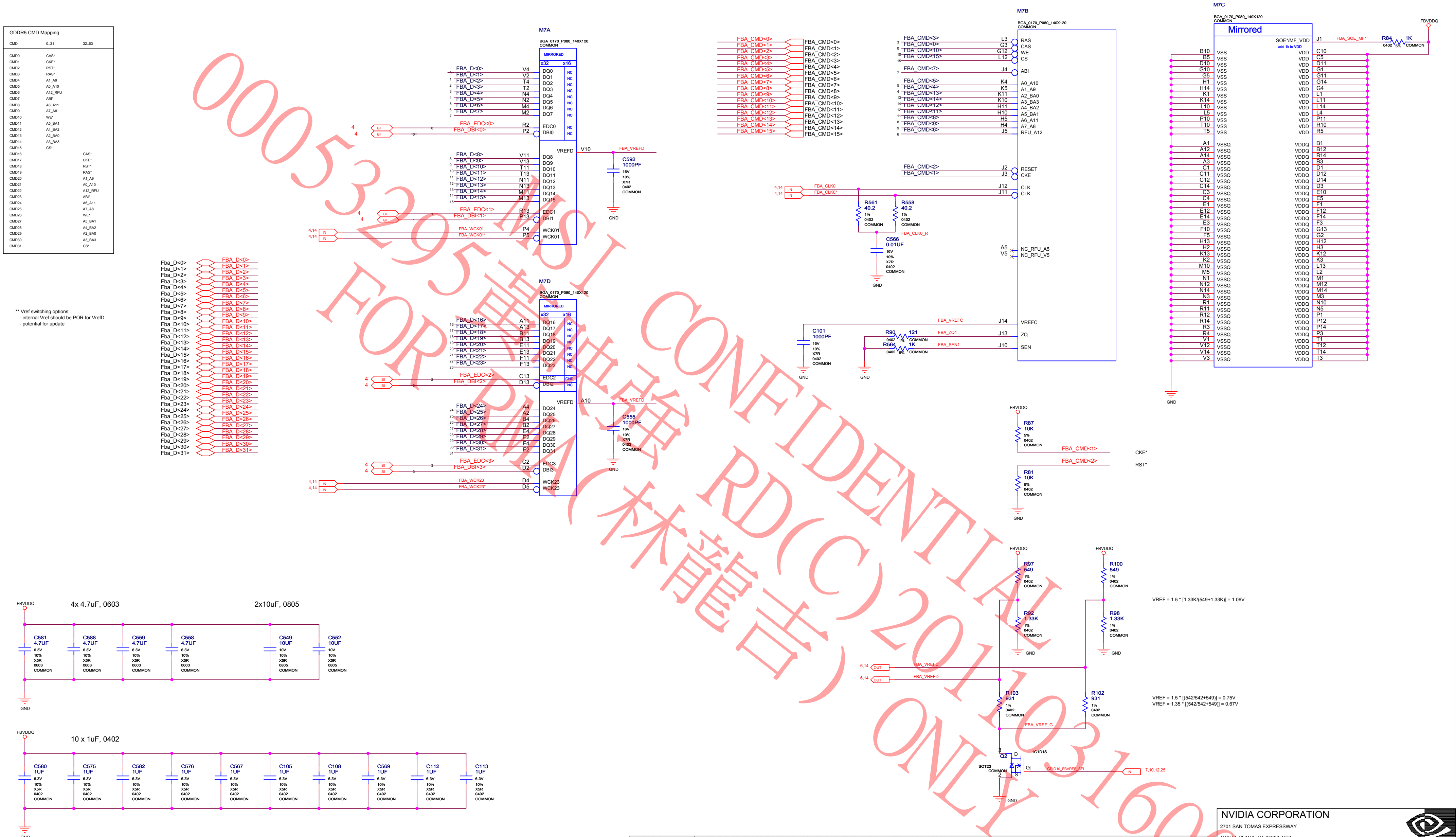
Page5: FBA Partition 31..0

GDDR5 CMD Mapping

CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA Partition 31..0

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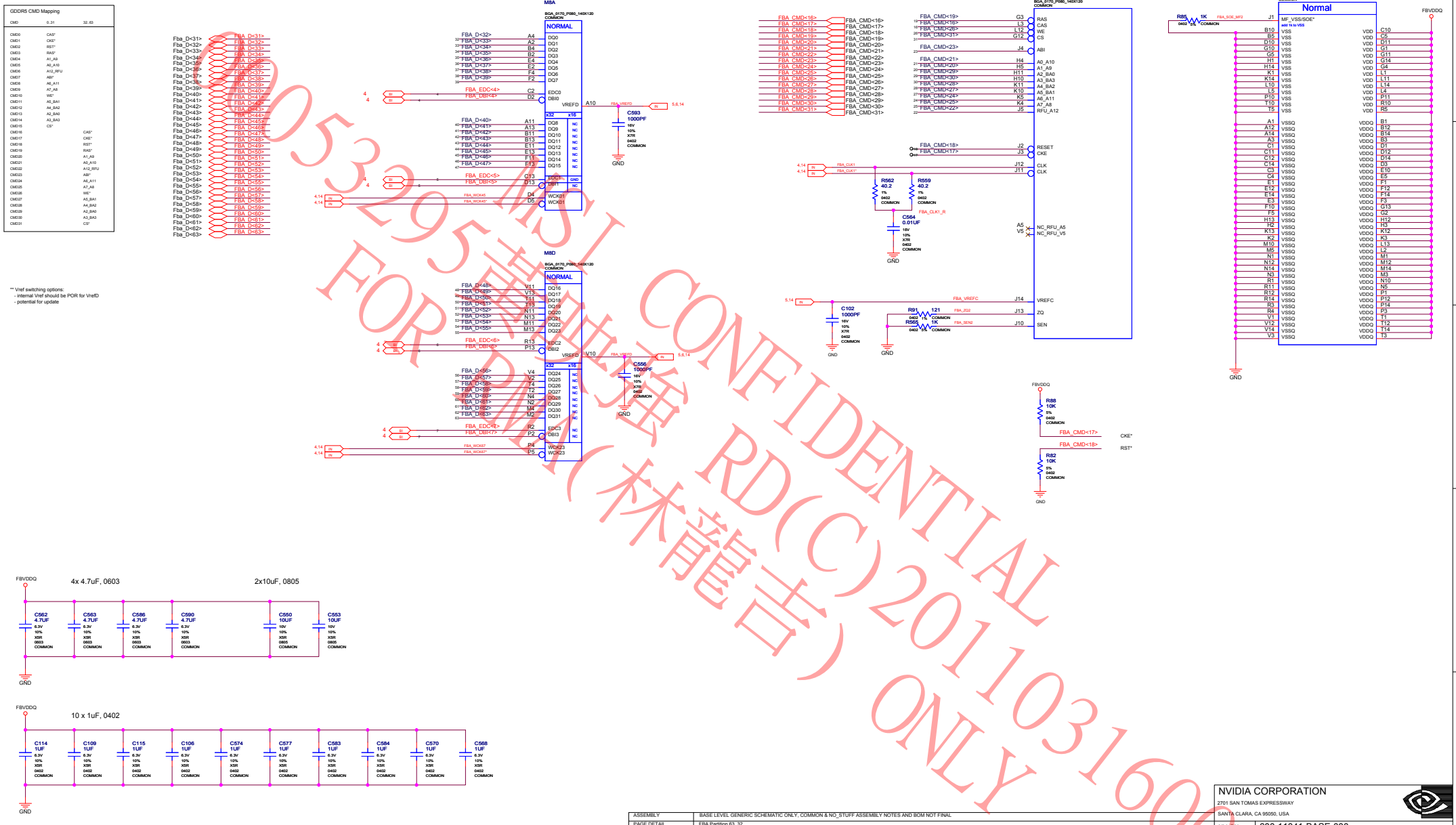
Page6: FBA Partition 63..32



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA Partition 63..32

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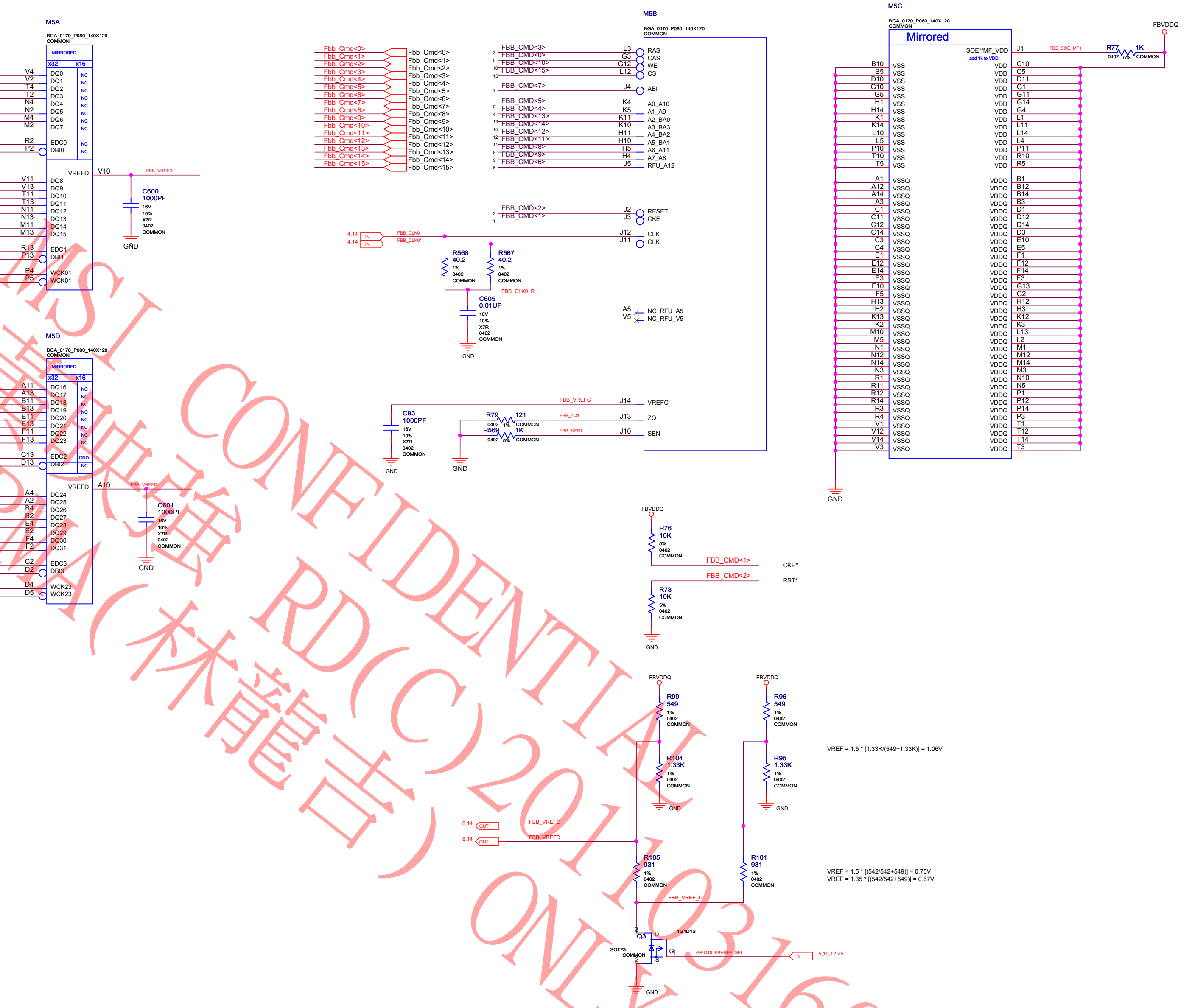
Page7: FBB Partition 31..0

GDDR5 CMD Mapping

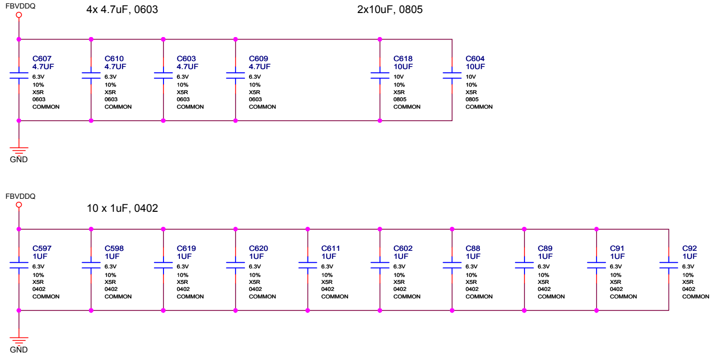
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update



FBVDDQ 4x 4.7uF, 0603 2x10uF, 0805

FBVDDQ 10 x 1uF, 0402



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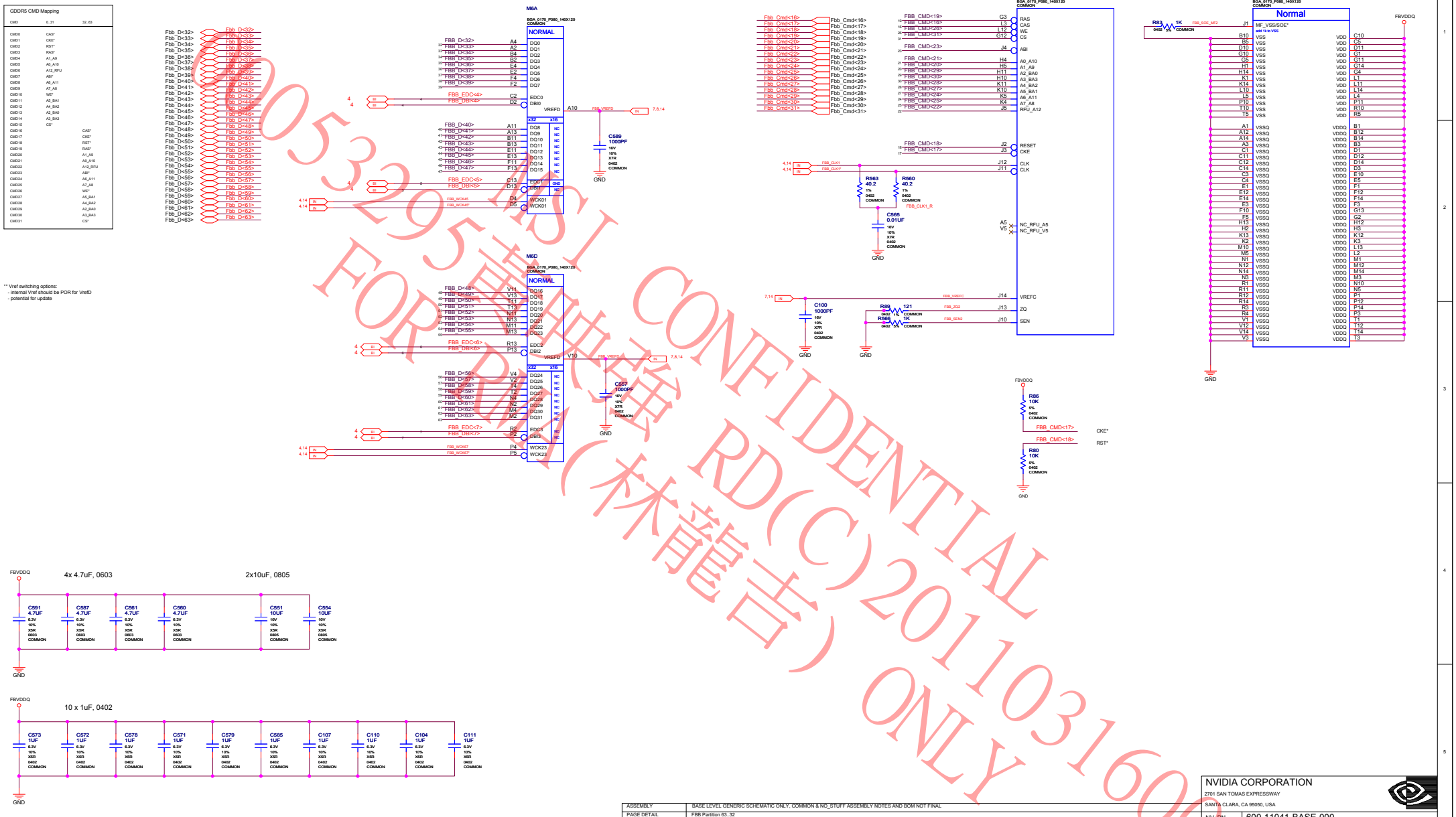
Page8: FBB Partition 63..32



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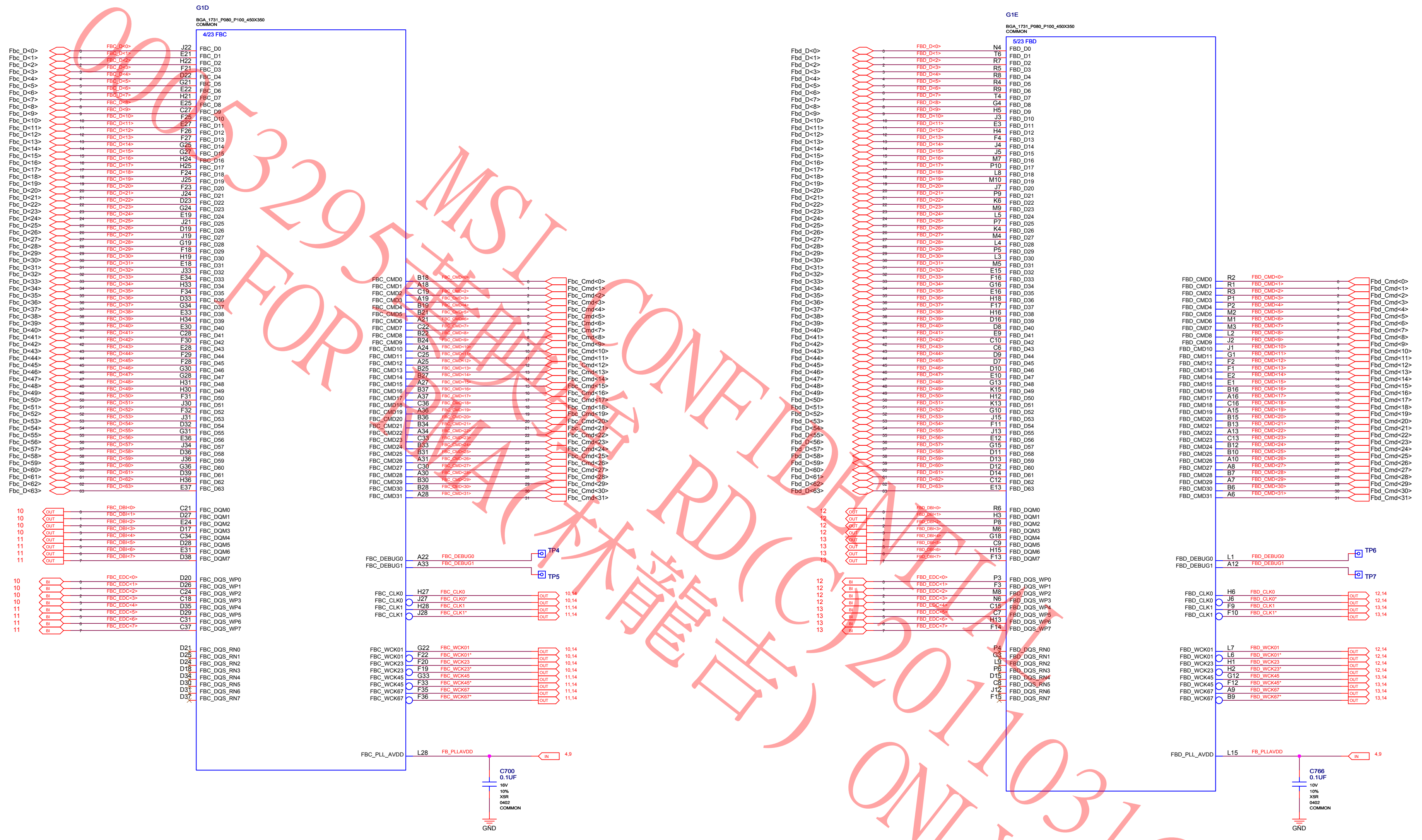
Page9: GPU Partition C/D



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PAGE DETAIL	GPU Partition C/D

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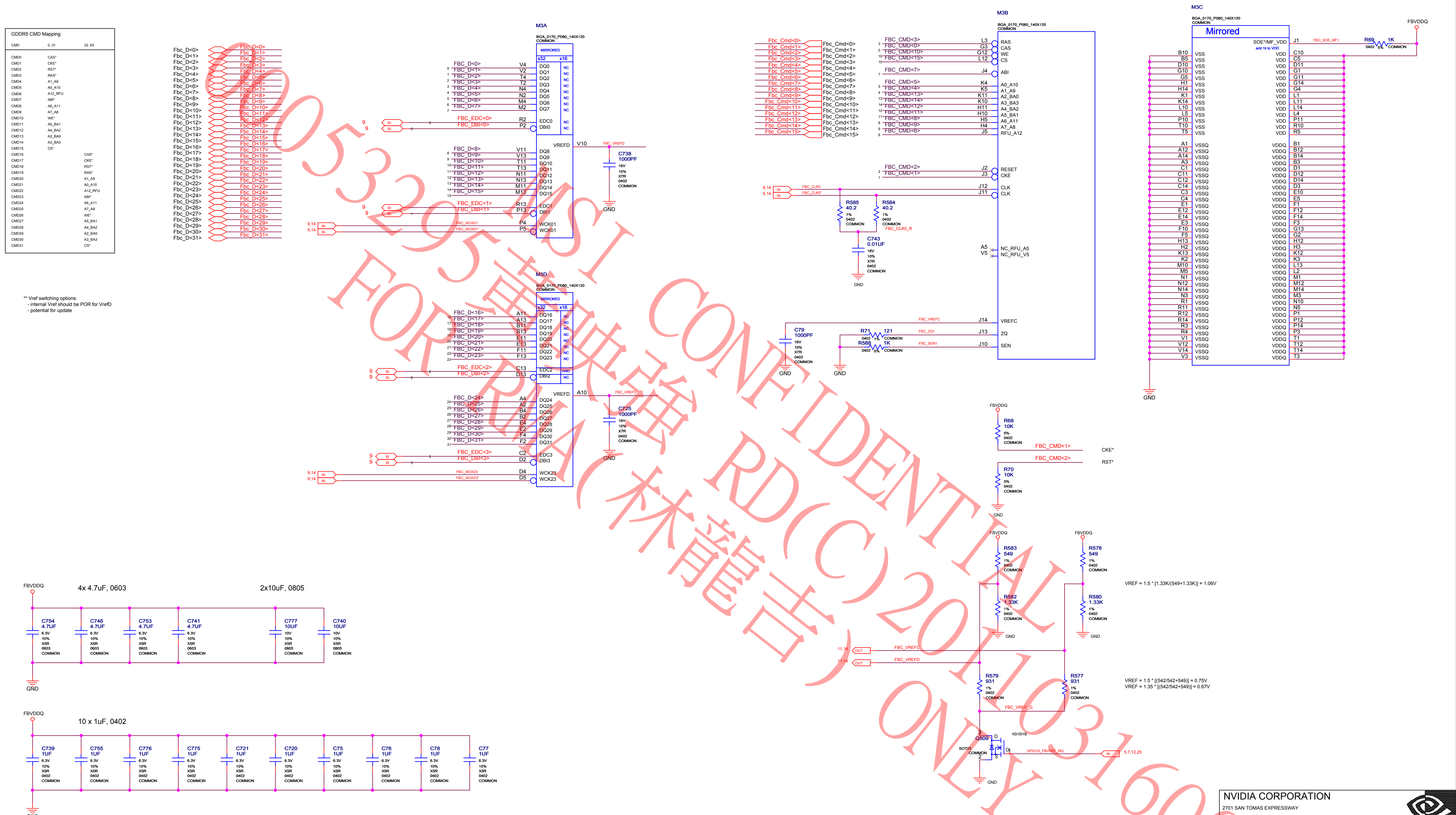
Page10: FBC Partition 31..0



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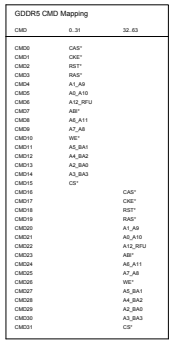

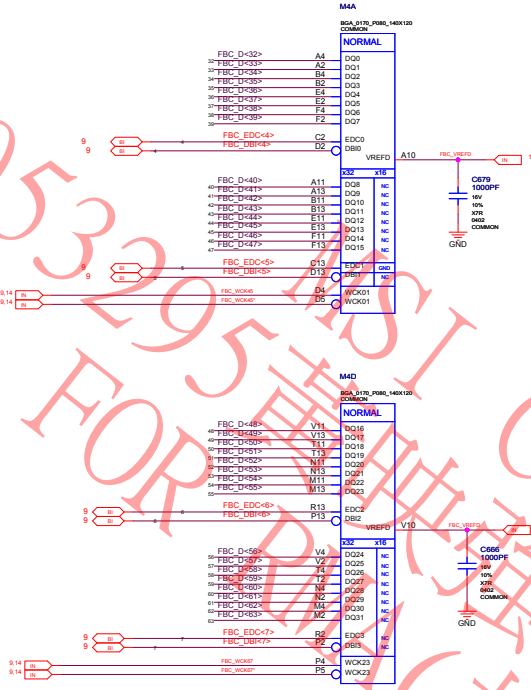

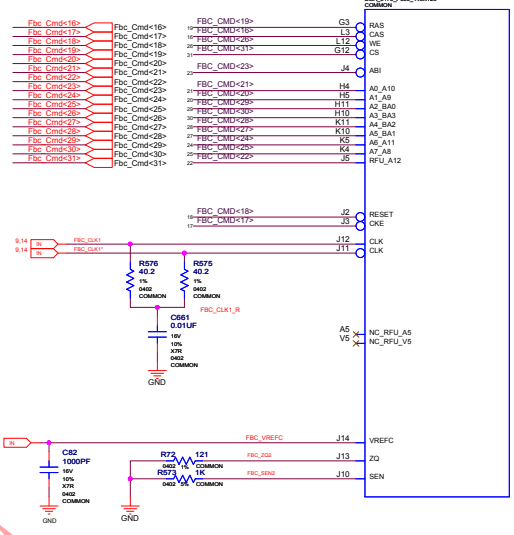

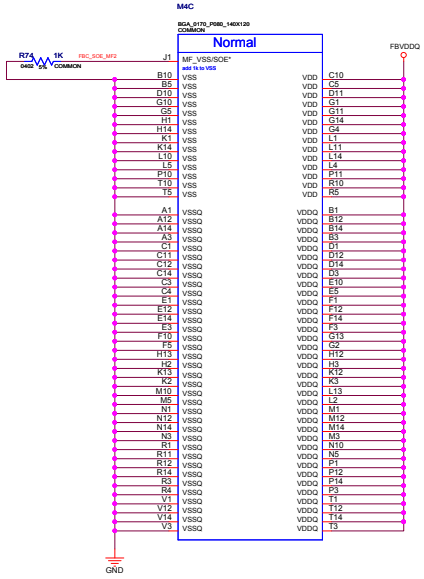

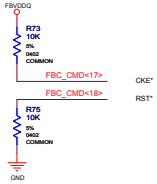

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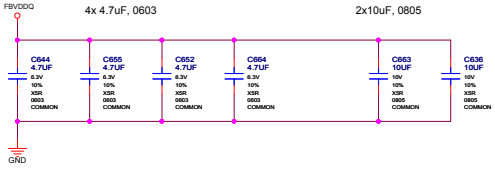
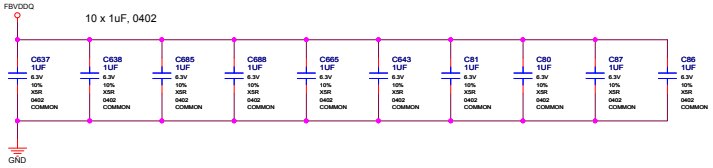
- internal Vref should be POR for VrefD
- potential for update





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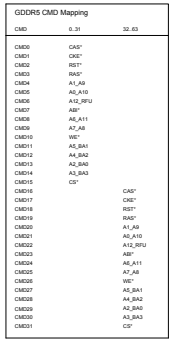

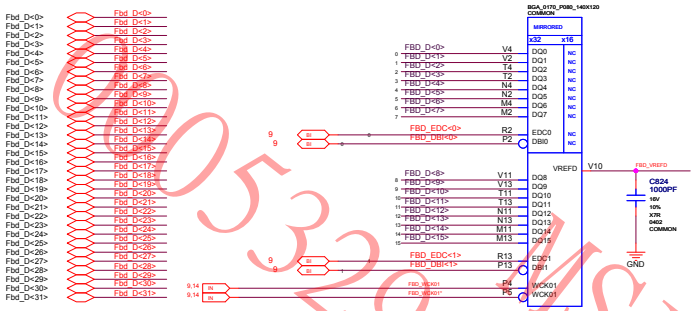

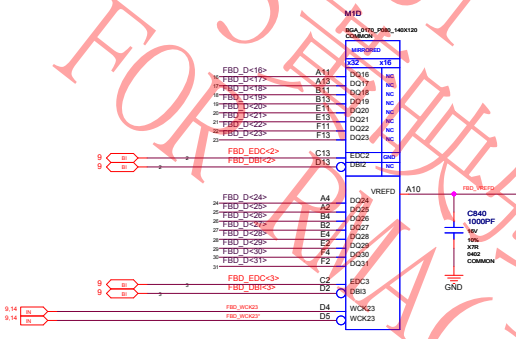

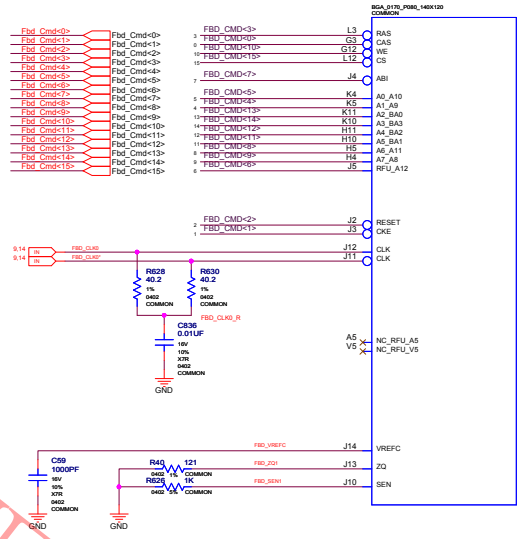

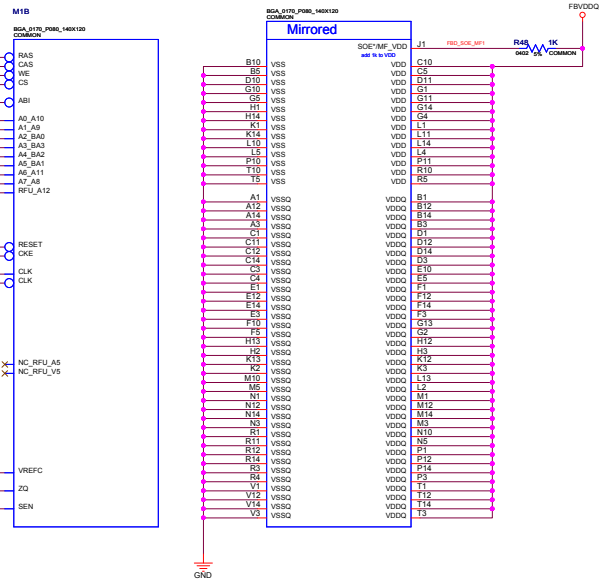

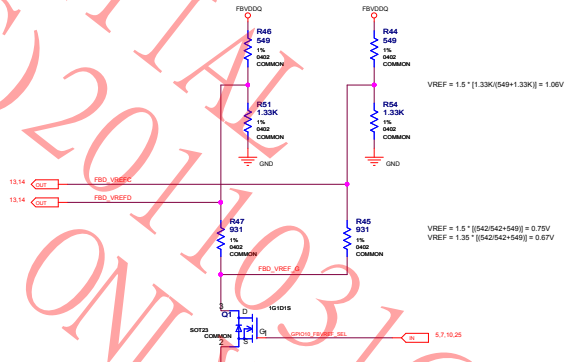

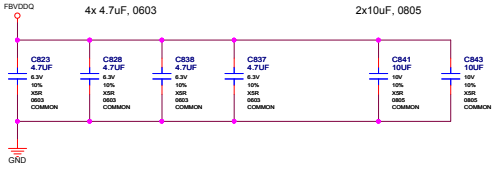

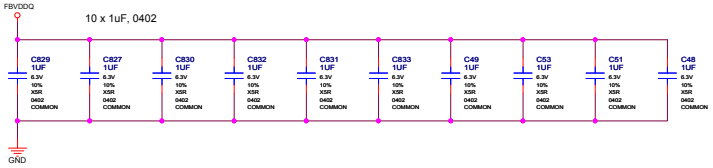

** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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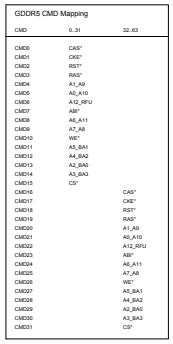

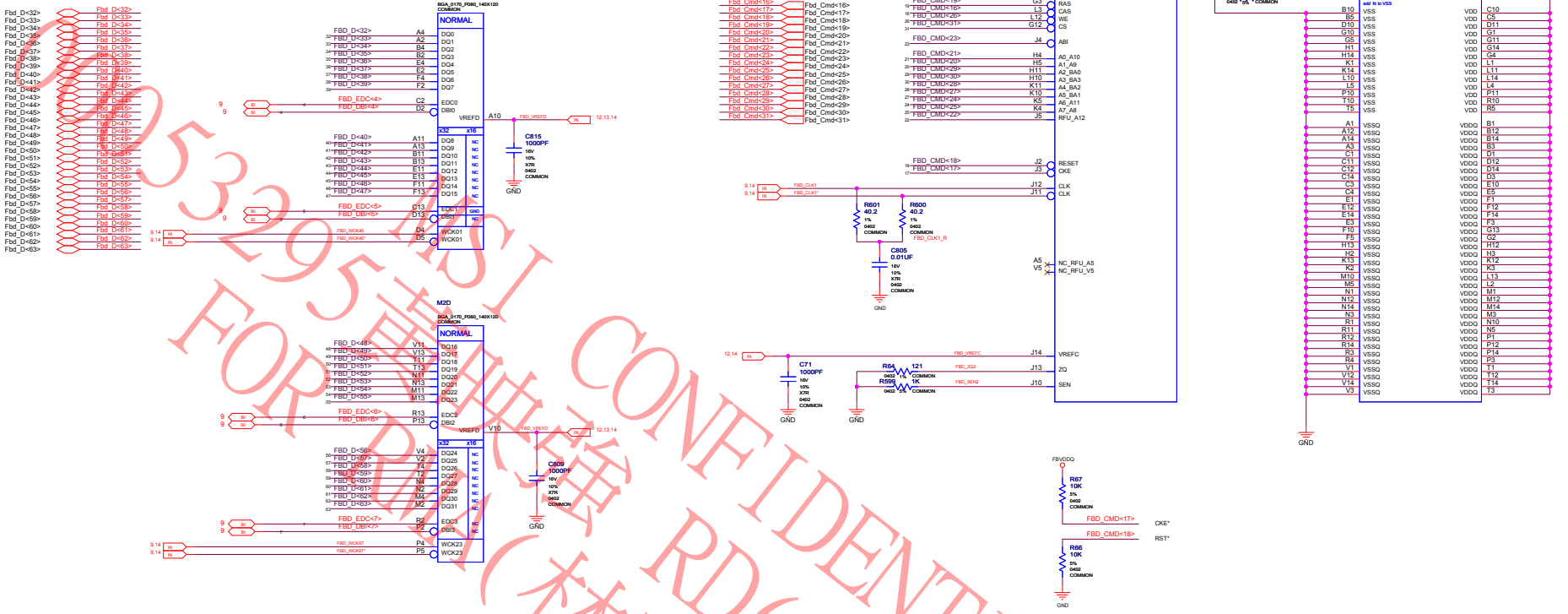

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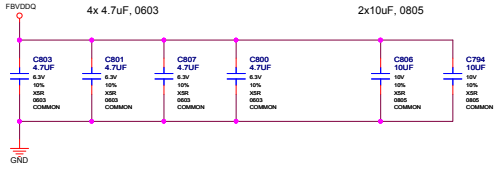

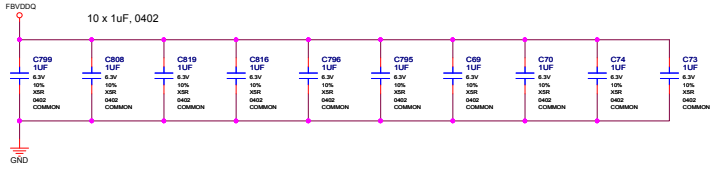

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Page14: FB Net Properties

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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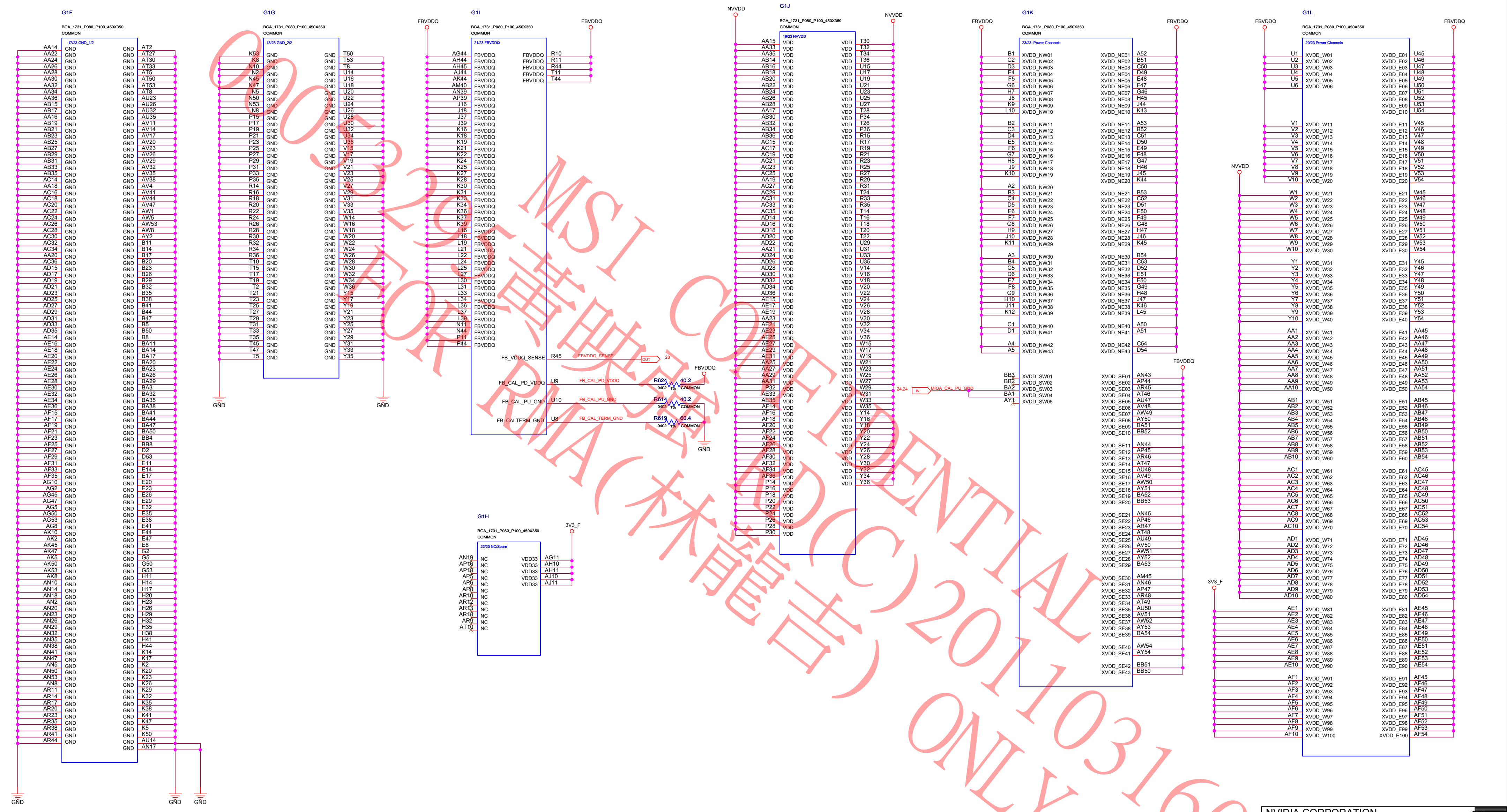
Page15: GPU PWR and GND

** Power channels are configurable.
XVDD_* pins are not connected on the substrate.
Therefore, XVDD_* pins can be assigned as needed.



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	GPU PWR and GND

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Page16: GPU Decoupling

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	GPU Decoupling

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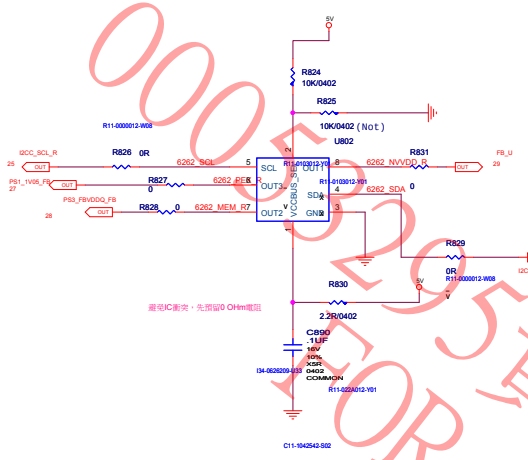

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PCB REV	P1041-B01	PAGE	
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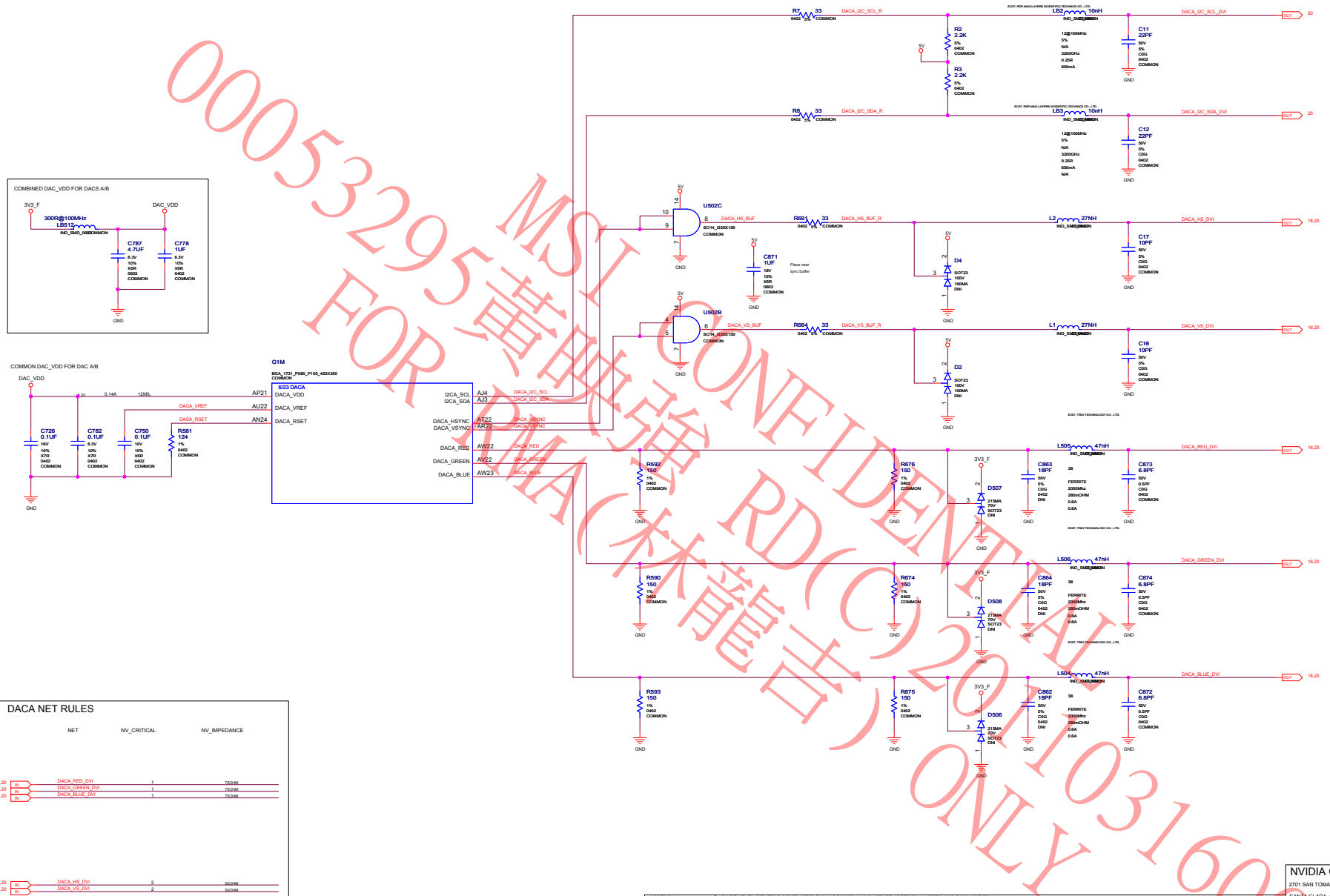

DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE
DACA_RED_DVI	1	75OHM
DACA_GREEN_DVI	1	75OHM
DACA_BLUE_DVI	1	75OHM
DACA_HS_DVI	2	50OHM
DACA_VS_DVI	2	50OHM

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA (South)

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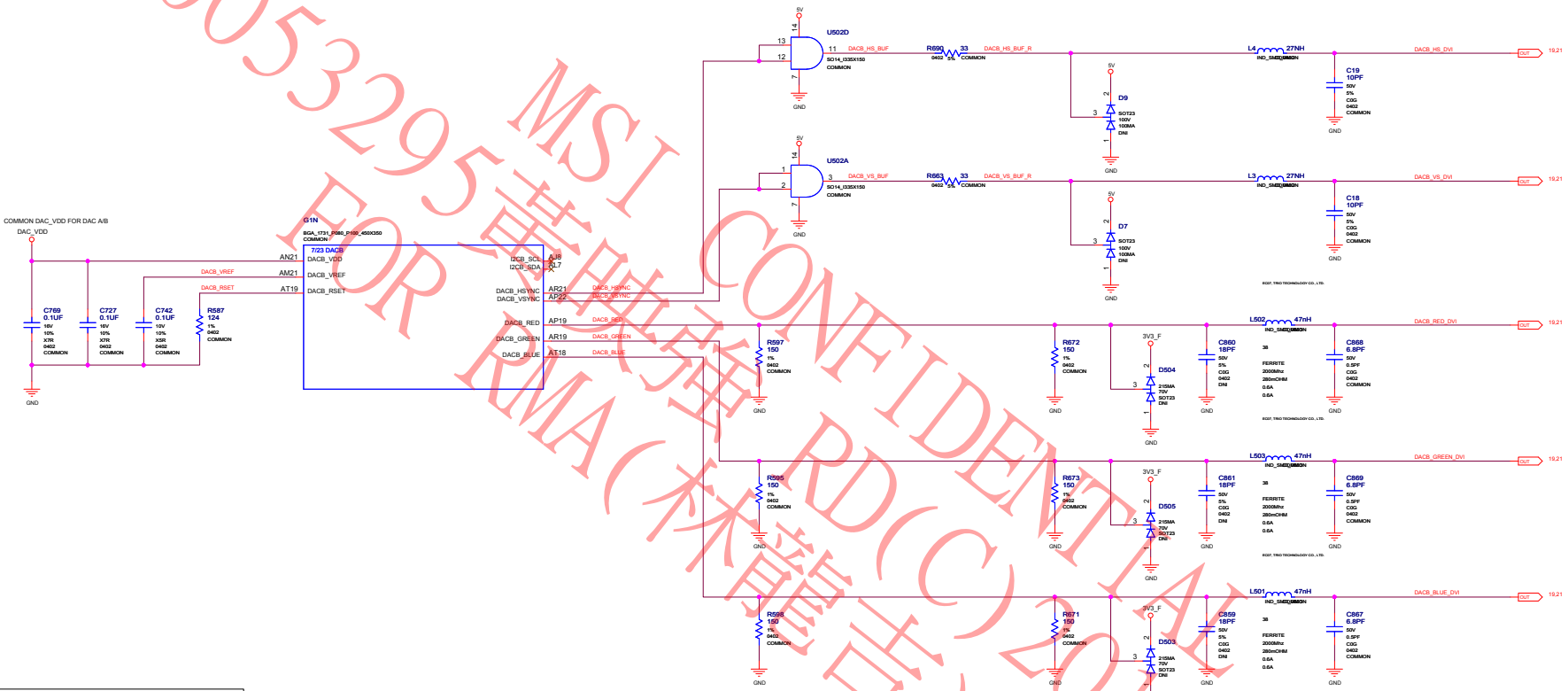
Page19: DACB (Mid)



DACB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE
DACB_RED_DVI	1	75OHM
DACB_GREEN_DVI	1	75OHM
DACB_BLUE_DVI	1	75OHM
DACB_HS_DVI	2	50OHM
DACB_VS_DVI	2	50OHM

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB (Mid)

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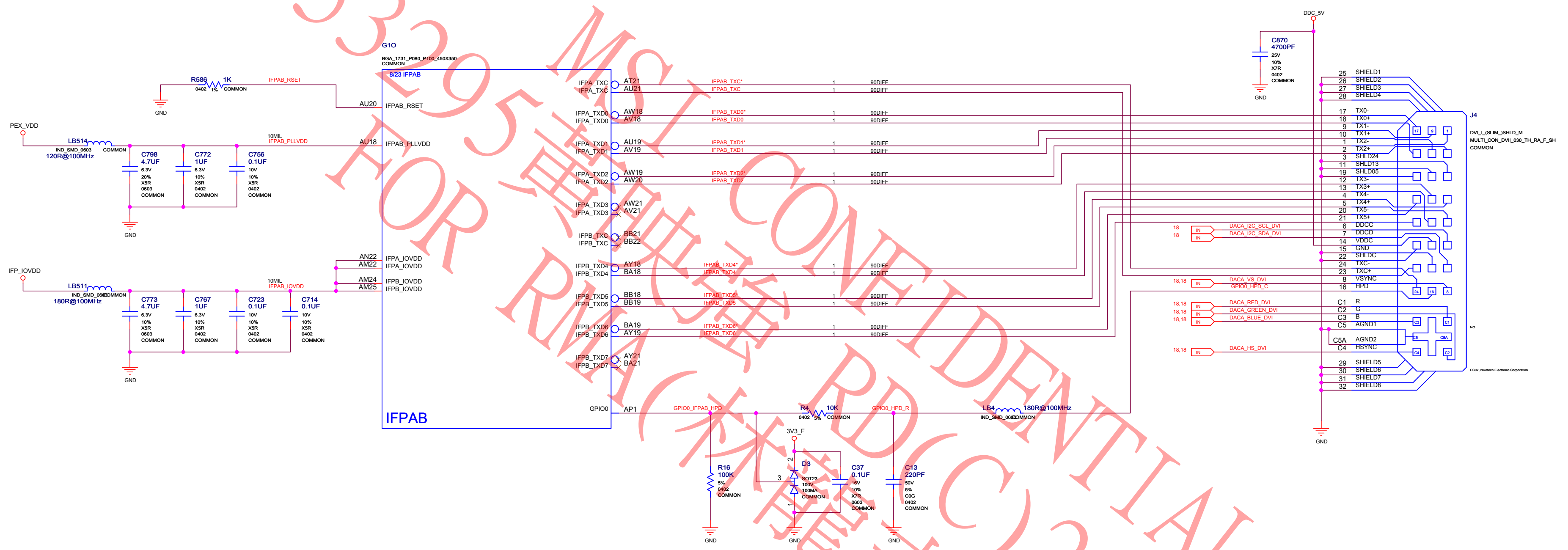
Page20: IFPAB DVI-I-DL (South)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPAB DVI-DL (South)

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PCB REV	P1041-B01	PAGE	
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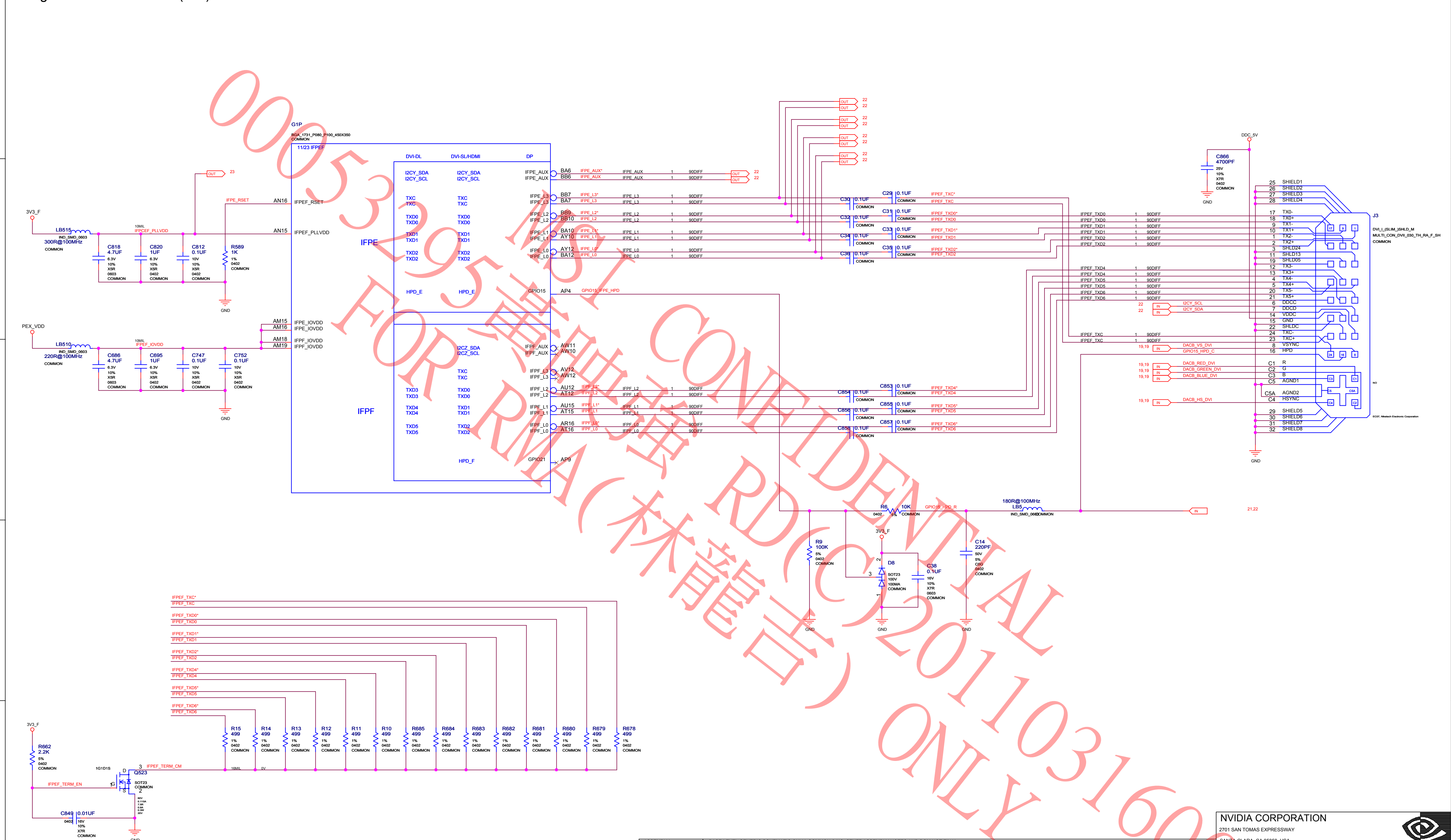
Page21: IFPEF DVI-I-DL (Mid)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPEF DVI-DL (Mid)

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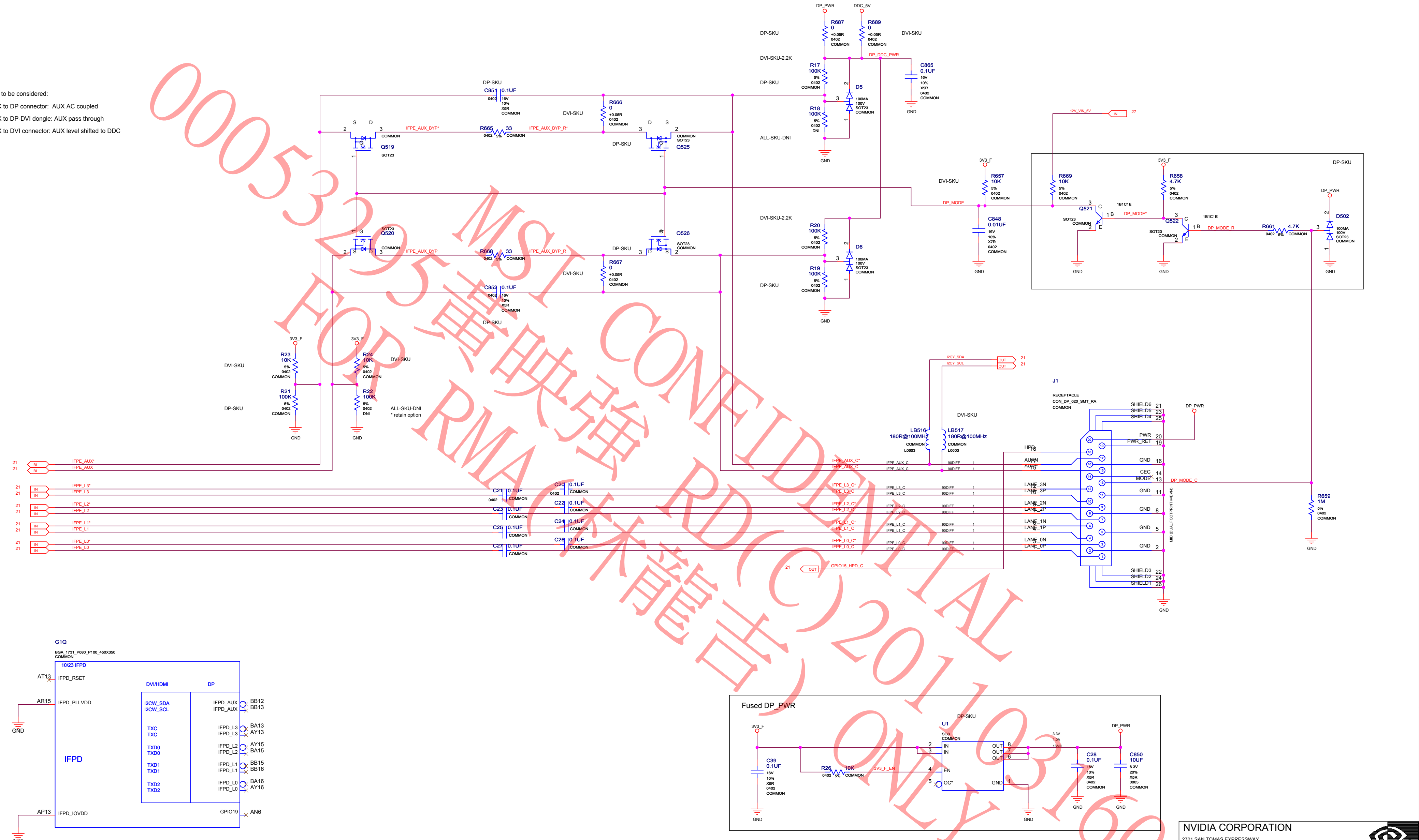
Page22: IFPEF DP (Mid)

Three cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through
3. DP AUX to DVI connector: AUX level shifted to DDC



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL	
PAGE DETAIL	IFPEF DP (Mid)	

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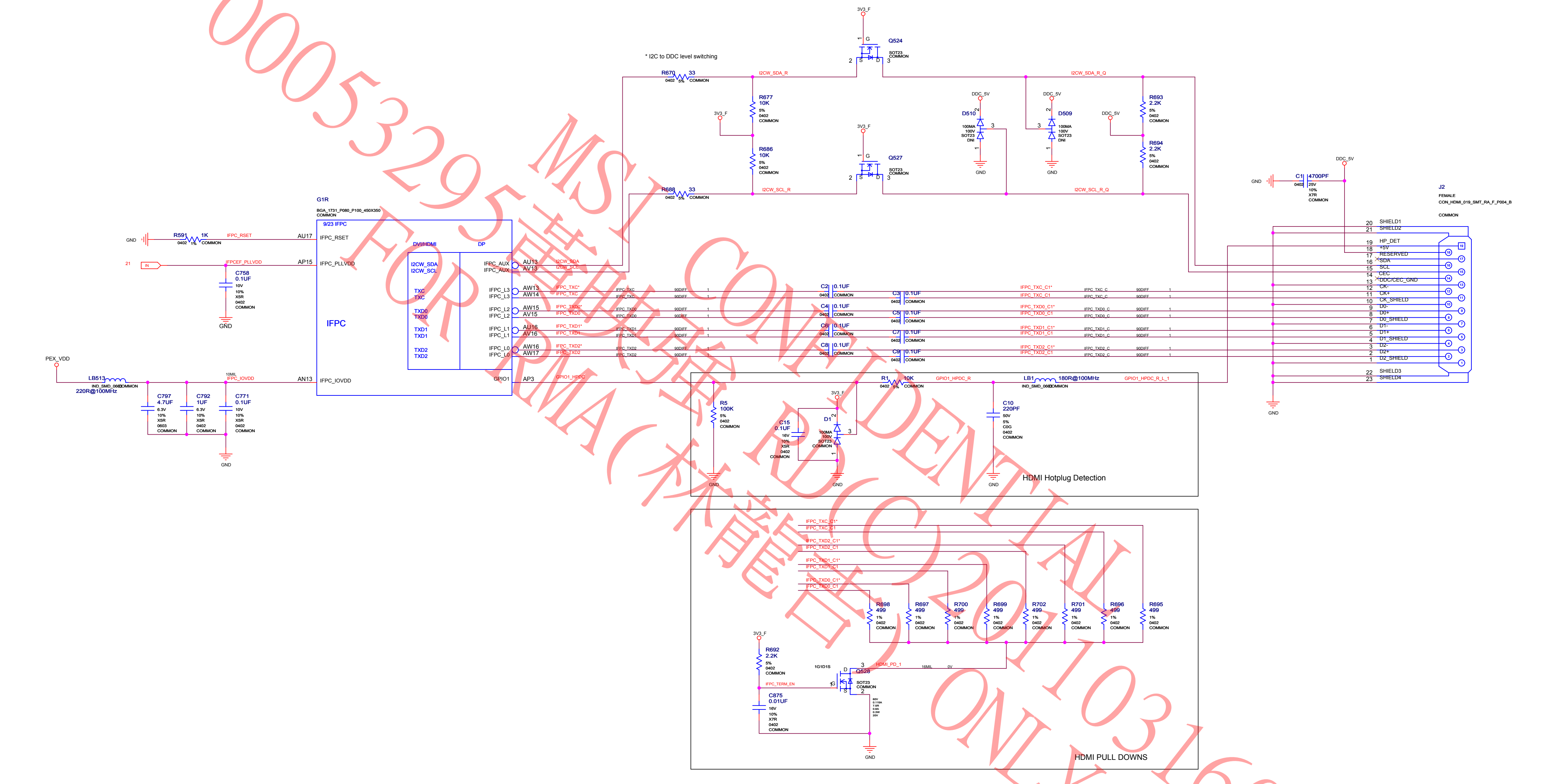
Page23: IFPC mHDMI (North)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPC mHDMI (North)

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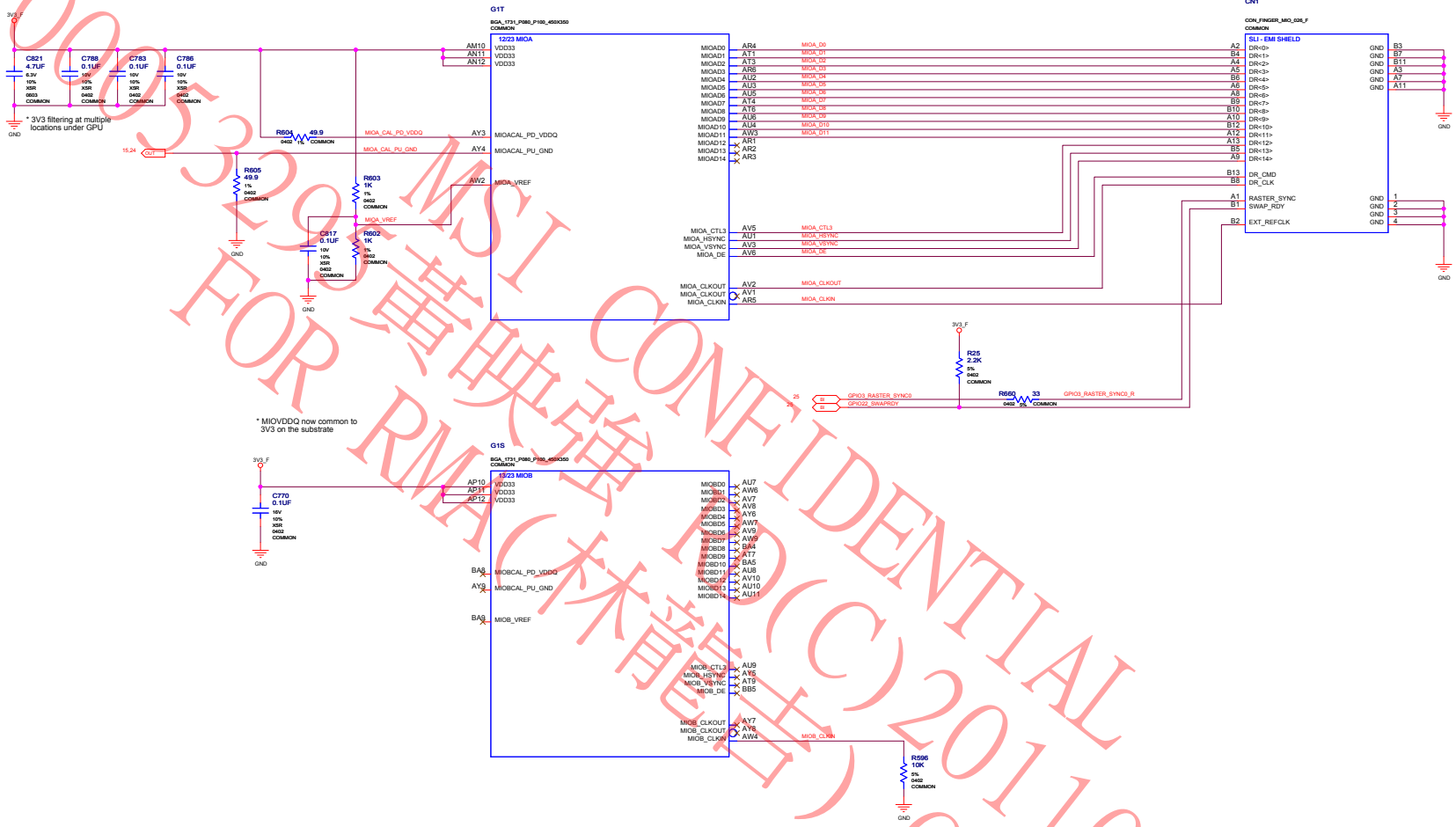
Page24: Multi-use IO (MIO) Interface



MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR

NET	VOLTAGE	MIN_WIDTH
MIOA_CAL_PU_GND	0.6V	6MIL

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Multi-use IO (MIO) Interface

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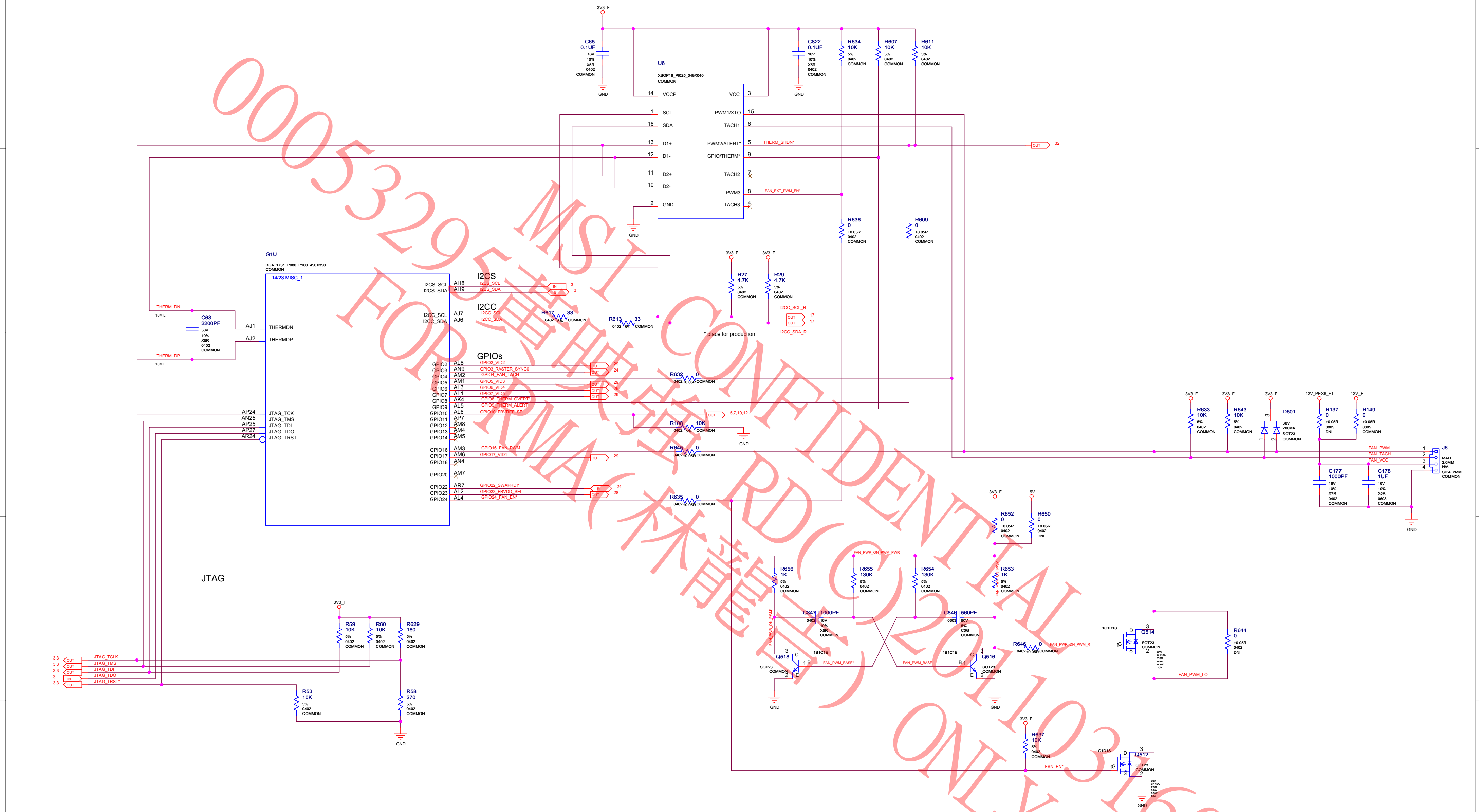
Page25: Misc: Fan, Thermal, JTAG, GPIO



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Misc: Fan, Thermal, JTAG, GPIO

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Page26: Misc: ROM, HDCP, XTAL, Straps

STRAP0	USER_BIT [3..0]	0000:=> 5K PD	
STRAP1	3GIO_PADCFG_LUT_ADR	0000 :=>5K PD	0000 Desktop
		0010 For 0x0E22 :=> 15K PD	
STRAP2	PCI_DEVID [3:0]	0100 For 0x0E24 :=> 25K PD	
ROM_SI	RAMCFG[0]		
	RAMCFG[1]		
	RAMCFG[2]		
	RAMCFG[3]		
ROM_SO	VGA_DEVICE	1	
	SMB_ALT_ADDR	0	10k PD
	FB[0]_BAR_SIZE	0	
	XCLK_417	0	
ROM_SCLK	PEX_PLL_EN_TERM100	1 ENABLED	
	SLOT_CLK_CFG	1 ENABLE	
	SUB_VENDOR	1 Dedicated BIOS	45K PD
	PCI_DEVID_EXT	0 0xC	

32Mx32 256 bit Samsung for SKU 10 first memory
0011: PD 20K
32Mx32 256 bit Hynix for SKU 10 2nd memory
0010: PD 15K

32Mx32 192 bit Samsung for SKU 0 first memory
1011: PU 20K
32Mx32 192 bit Hynix for SKU 0 2nd memory
1010: PU 15K

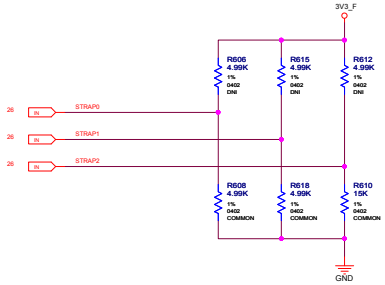
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

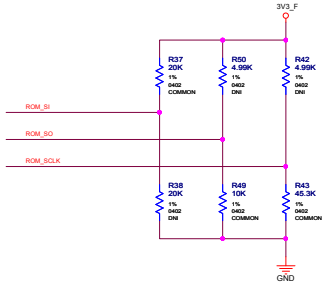
CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit	Qimonda
0010	32Mx32 256-bit	Hynix
0011	32Mx32 256-bit	Samsung
0100	Reserved	
0101	64Mx32 256-bit	Qimonda
0110	64Mx32 256-bit	Hynix
0111	64Mx32 256-bit	Samsung
1000	Reserved	
1001	32Mx32 192-bit	Qimonda
1010	32Mx32 192-bit	Hynix
1011	32Mx32 192-bit	Samsung
1100	Reserved	
1101	64Mx32 192-bit	Qimonda
1110	64Mx32 192-bit	Hynix
1111	64Mx32 192-bit	Samsung

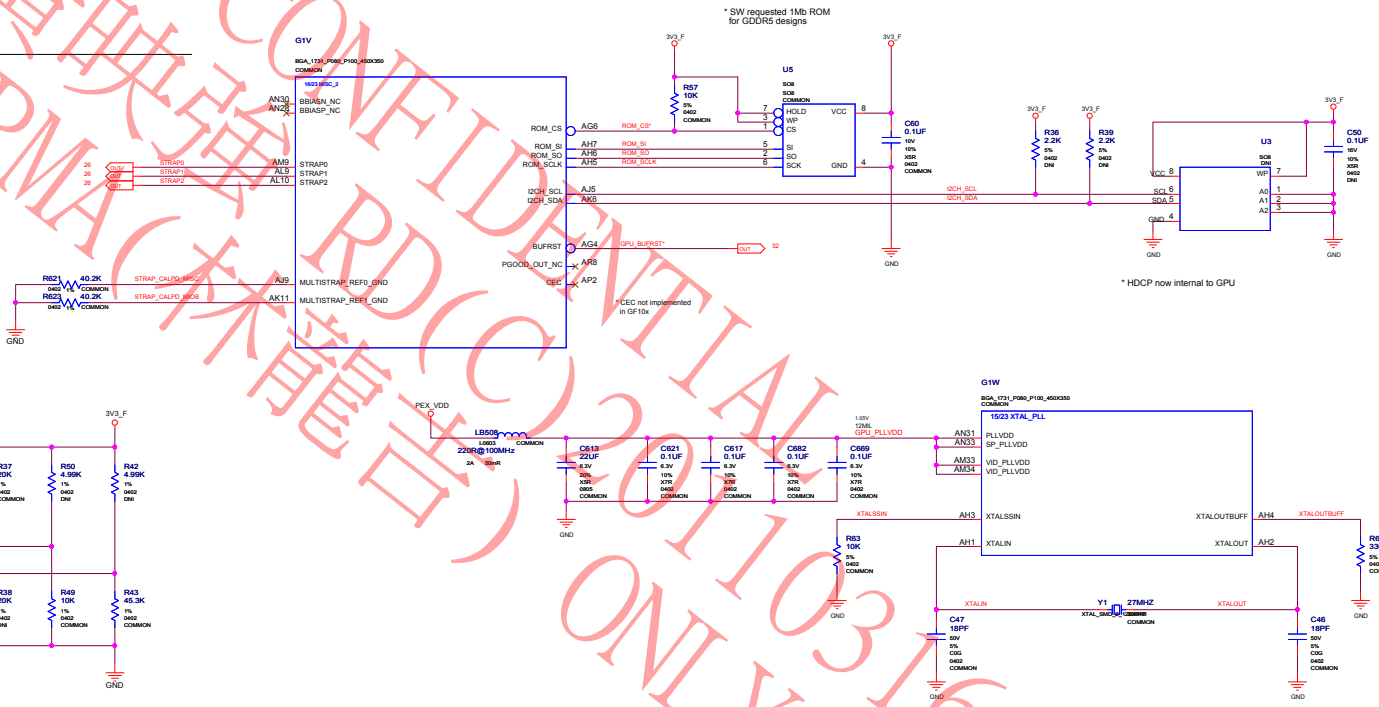
MISC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE

	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	40.2k 1% TO GND	NC
BINARY BRINGUP	NC	NC
MULTI-LEVEL	40.2k 1% TO GND	40.2k 1% TO GND







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Misc: ROM, HDCP, XTAL, Straps

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NV_PN	600-11041-BASE-000		
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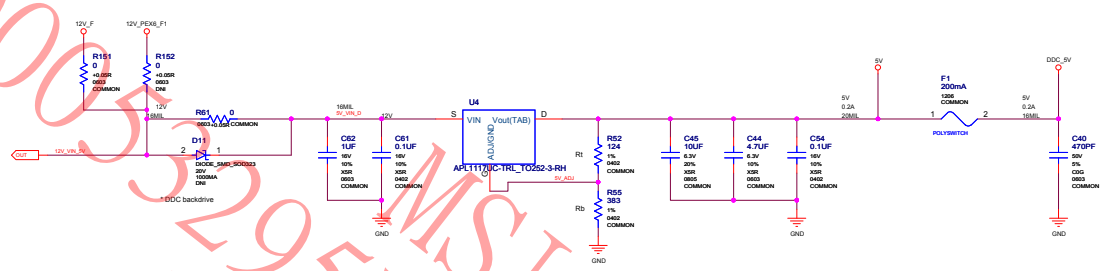
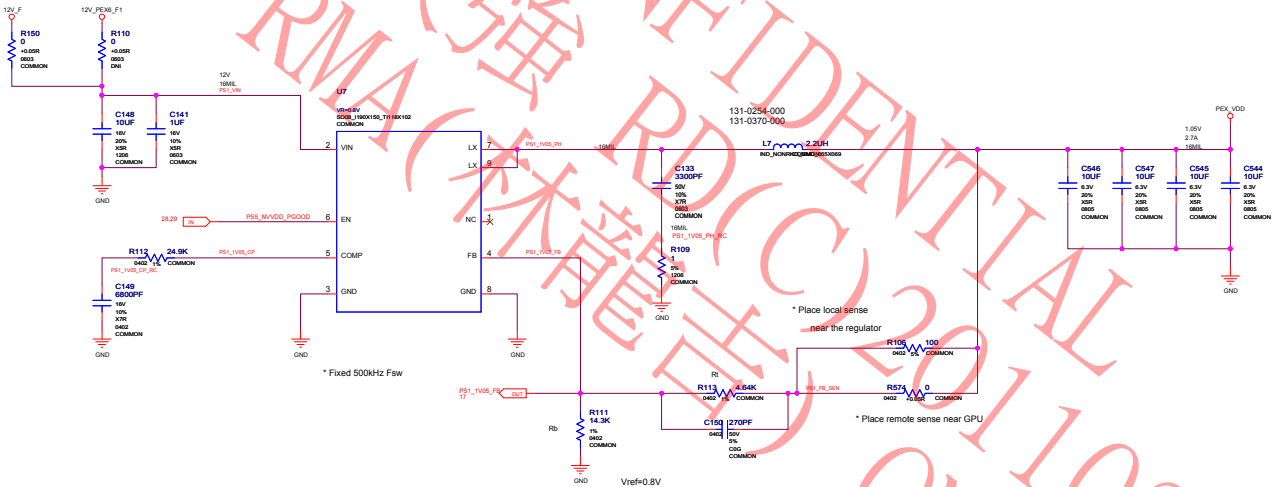


Vref=1.256V
Vo_Typ=1.256*(1+383/124)+60uA*383=5.16V

Input ripple (Irms) = ~0.9A @ 2.7A



Vref=0.8V
Vo_Typ=0.8*(1+Rt/Rb)=1.0467V
Vo_Typ=0.8*(1+4.64K/14.3K)=1.0596V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: 5V, PEX_VDD

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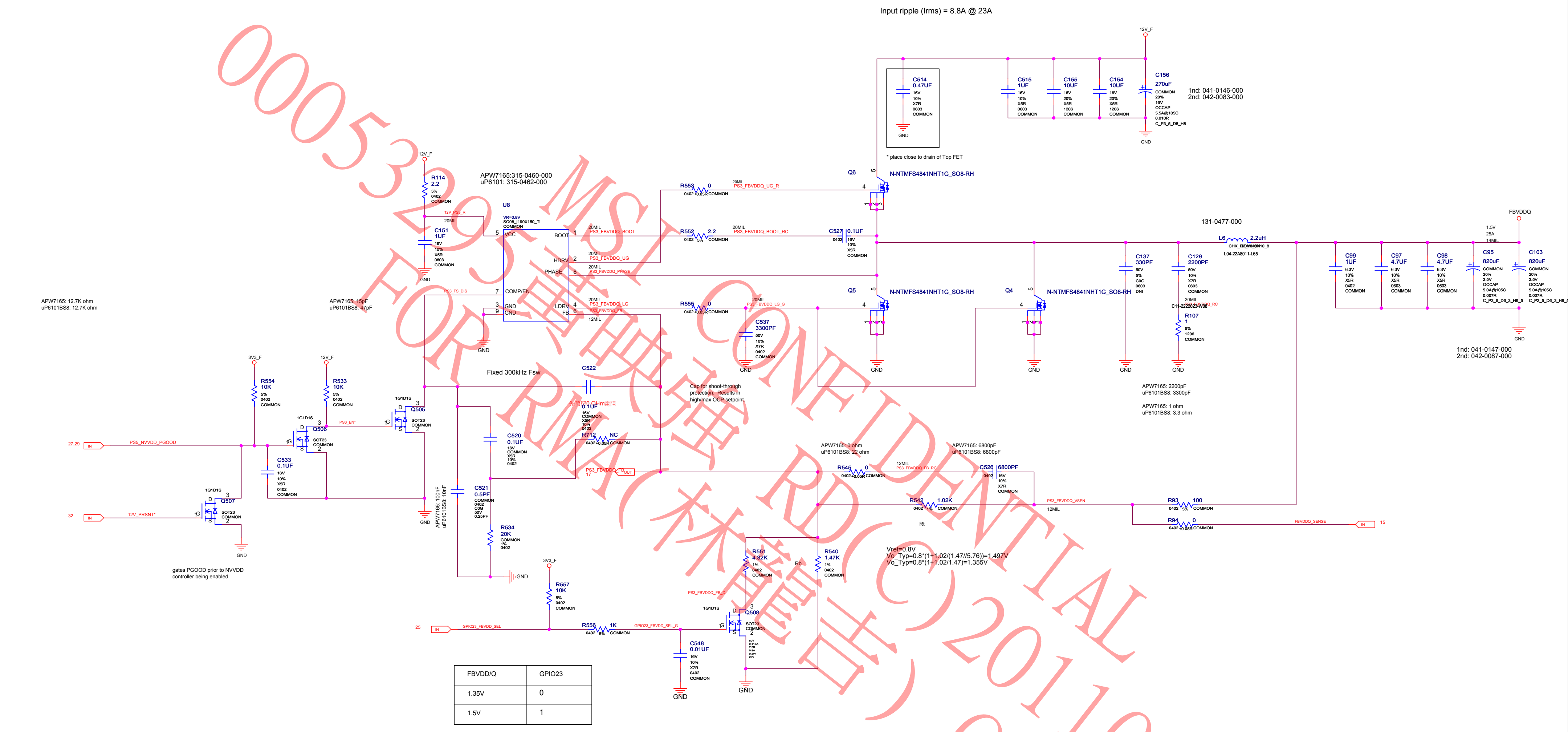
Page28: PS: FBVDD/Q



FBVDD/Q	GPIO23
1.35V	0
1.5V	1

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: FBVDD/Q

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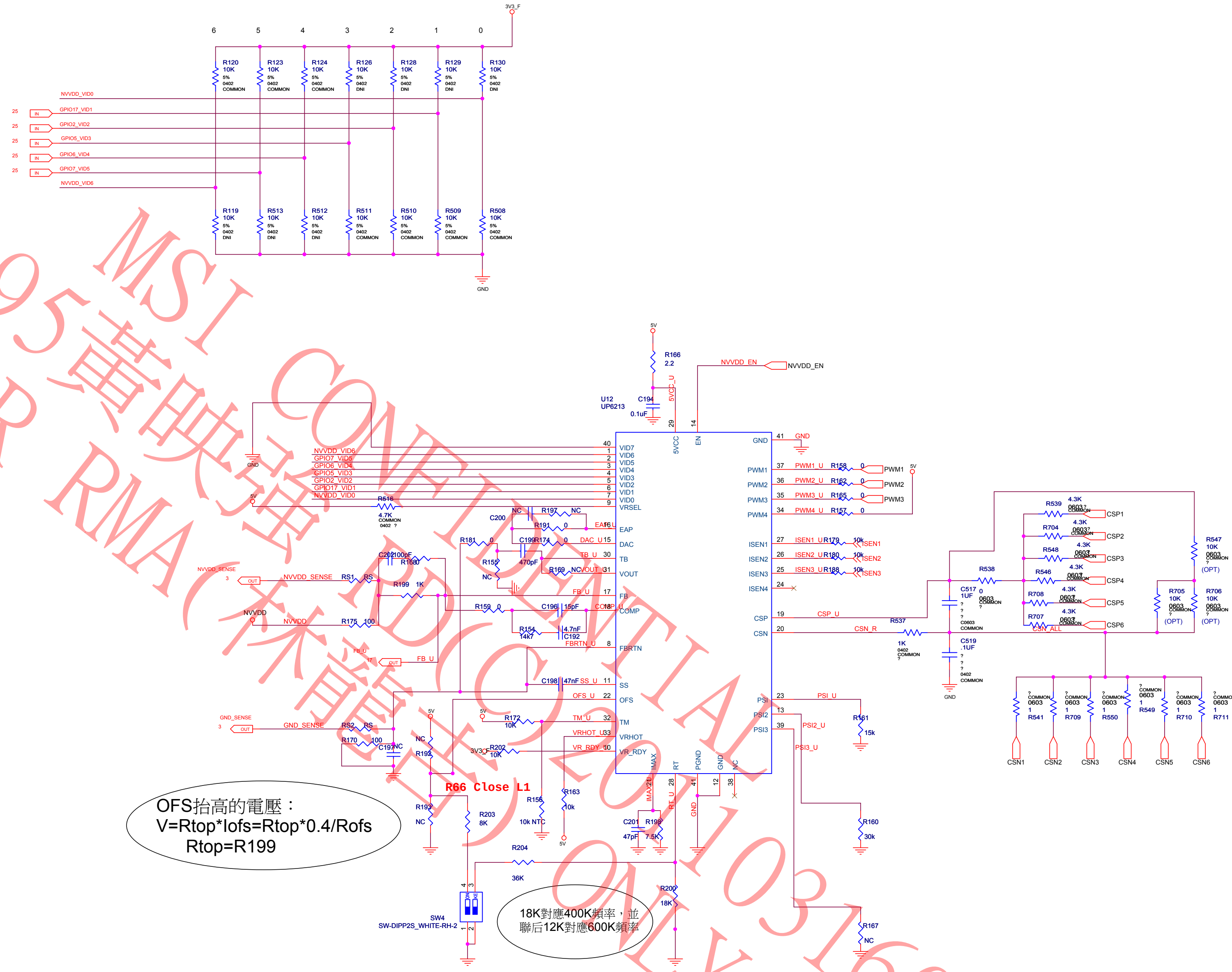
PAGE
DATE 12-MAY-2010

Page29: PS: NVVDD Controller

VID Table

GPIO7 VID_5	GPIO6 VID_4	GPIO5 VID_3	GPIO2 VID_2	GPIO17 VID_1	VOUT
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD Controller
NV_PN	600-11041-BASE-000
PCB REV	P1041-B01
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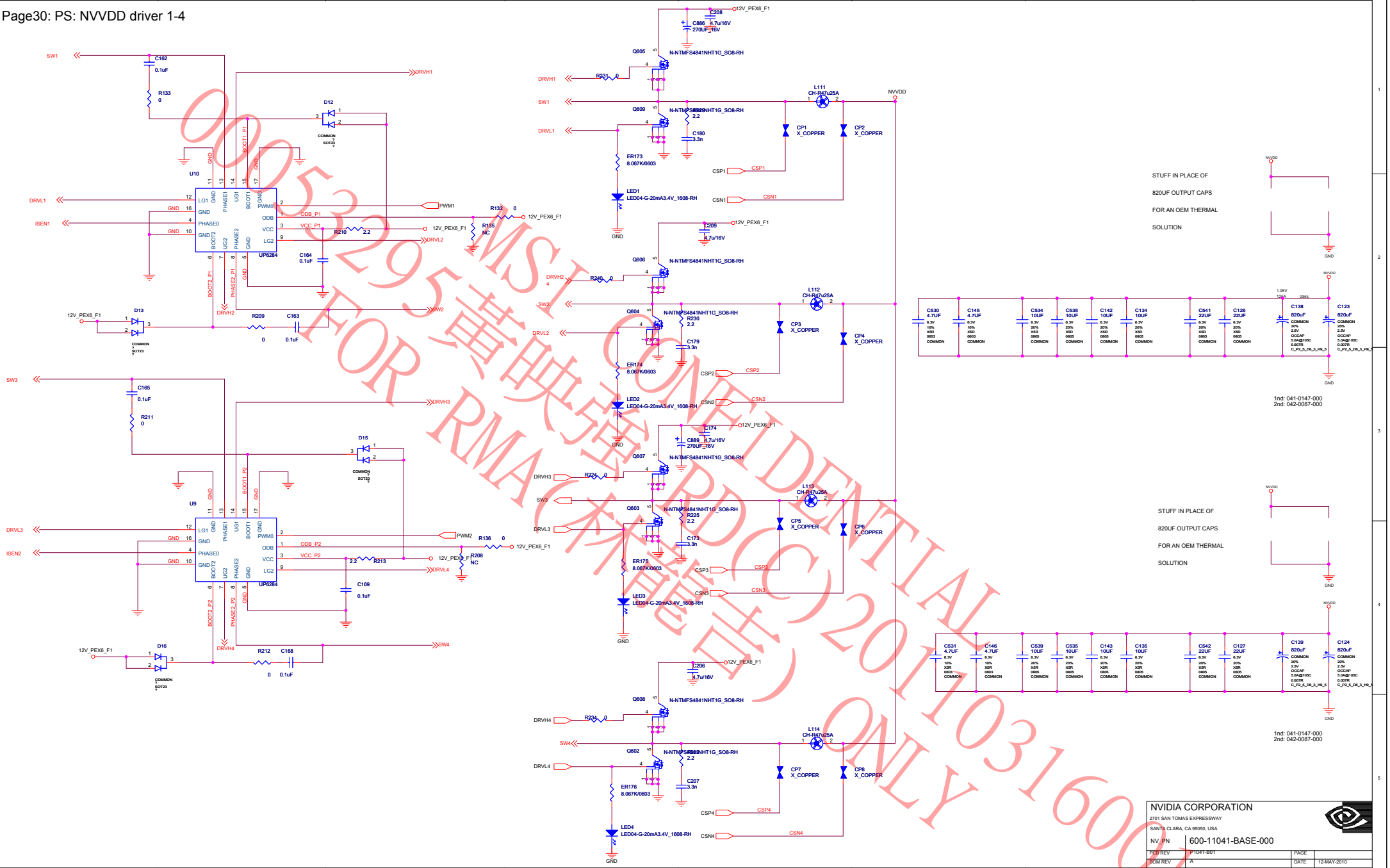
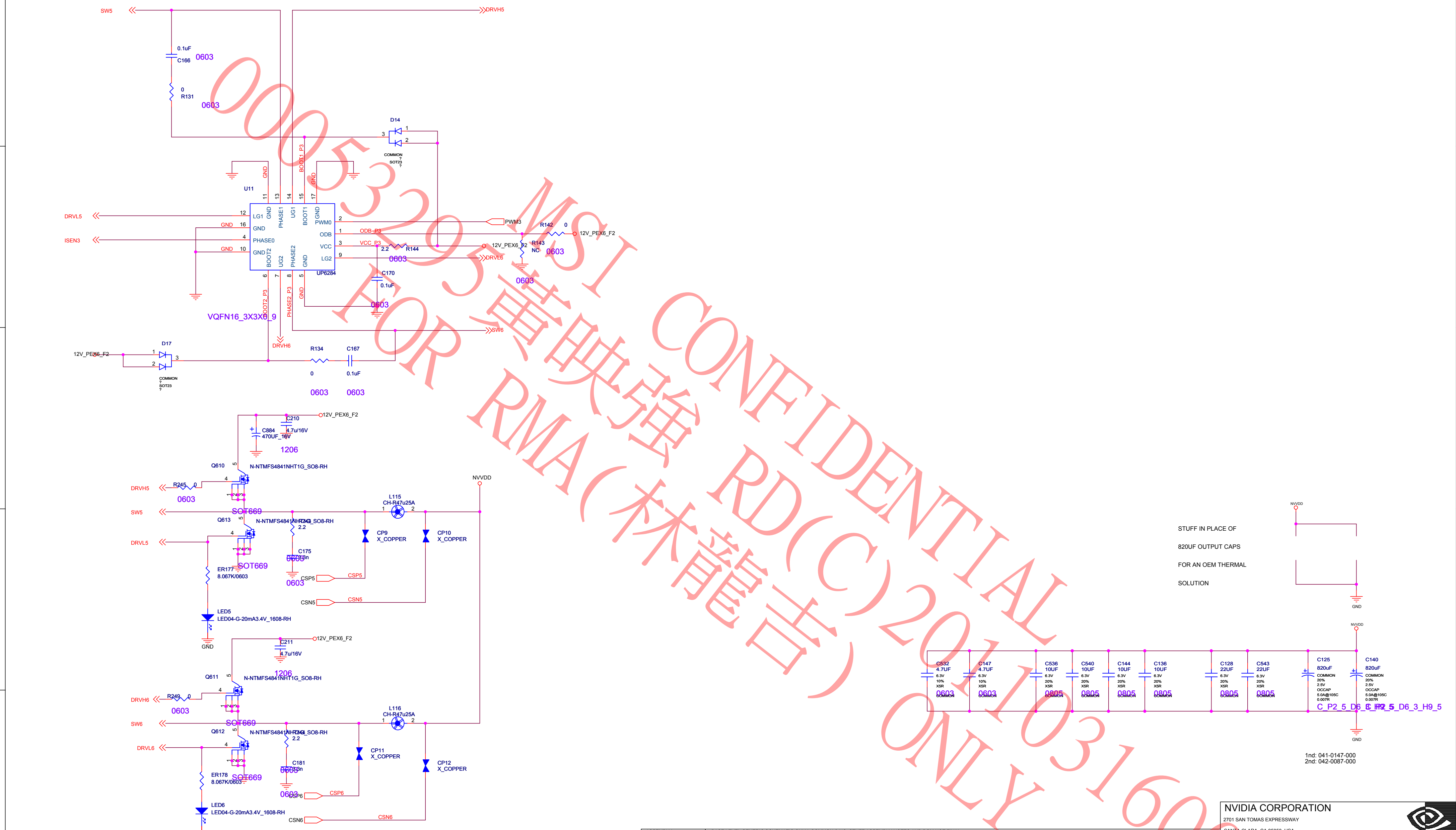
Page30: PS: NVVDD driver 1-4



Page31: PS: NVVDD driver 5-6



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD Phase 3

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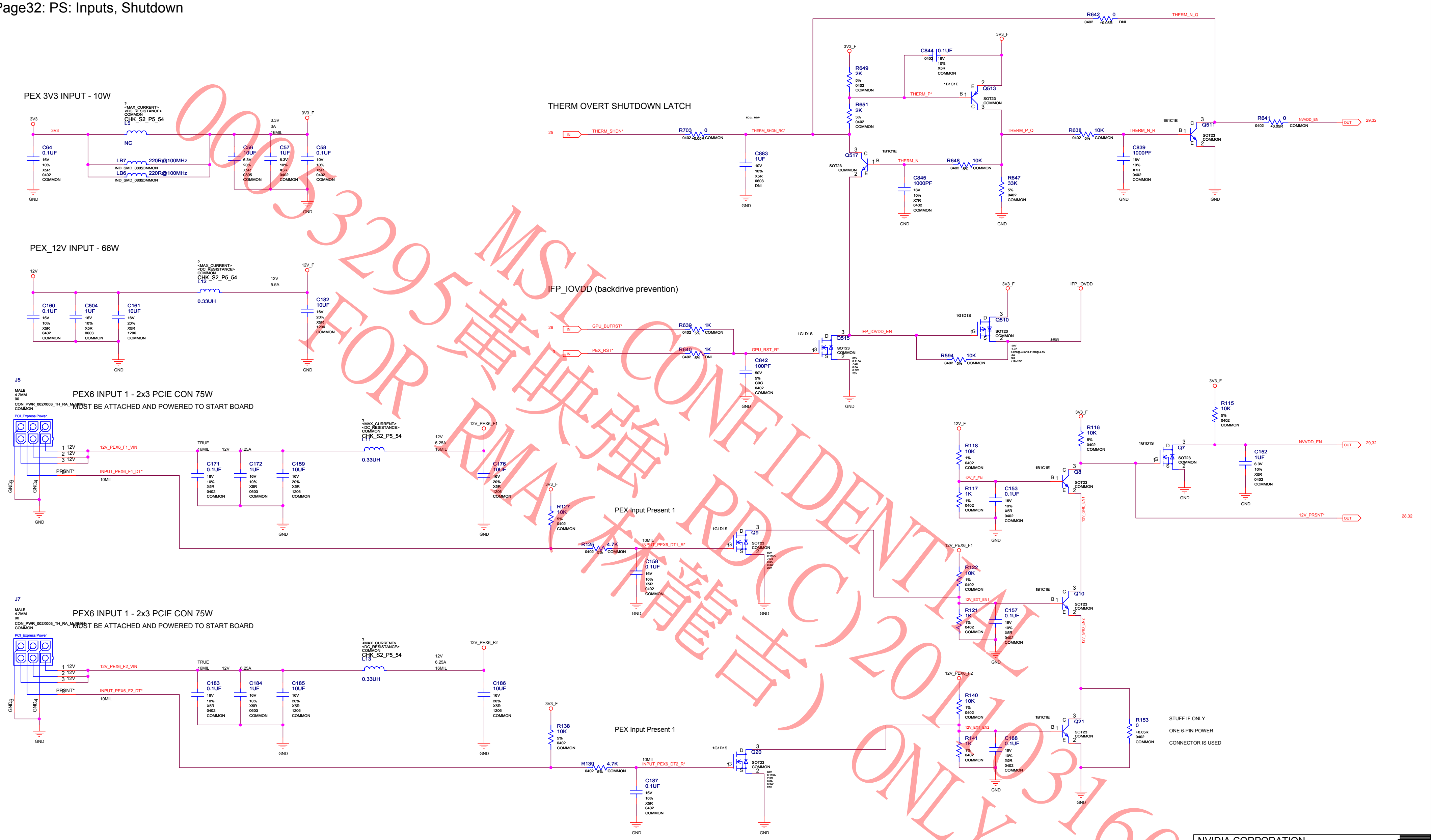
Page32: PS: Inputs, Shutdown



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: Inputs, Shutdown
NV_PN	600-11041-BASE-000
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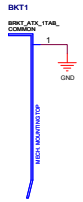
PAGE	
DATE	12-MAY-2010

Page33: Mechanical: Bracket/Thermal Solution

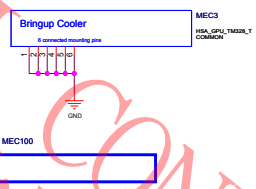
Brackets:

Bracket with DVI_DP_mHDMI : 151-10001-0355-071

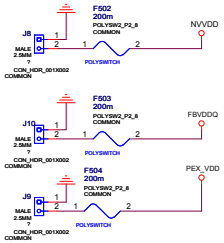


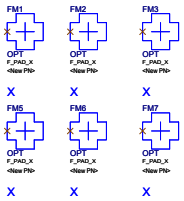
Bracket Screw

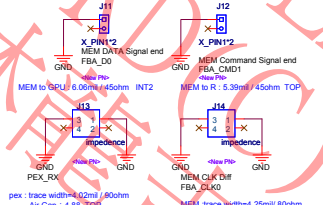
Cooler/GPU Stiffener



remove mec1







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Mechanical: Bracket/Thermal Solution

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Page34: Blank

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Blank

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