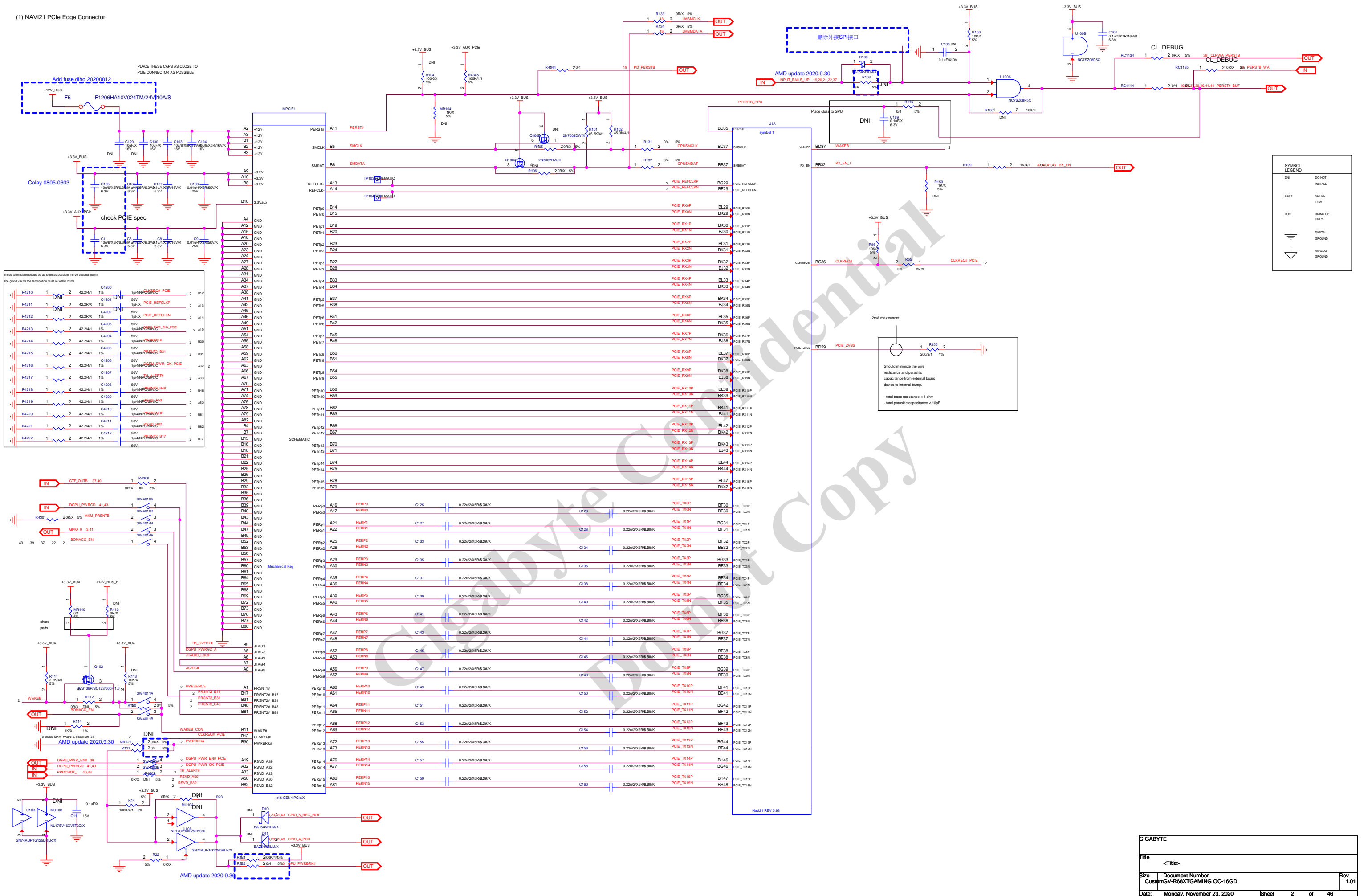
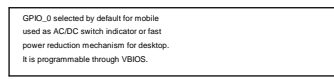


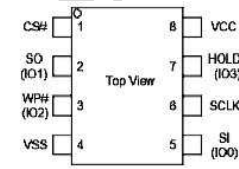
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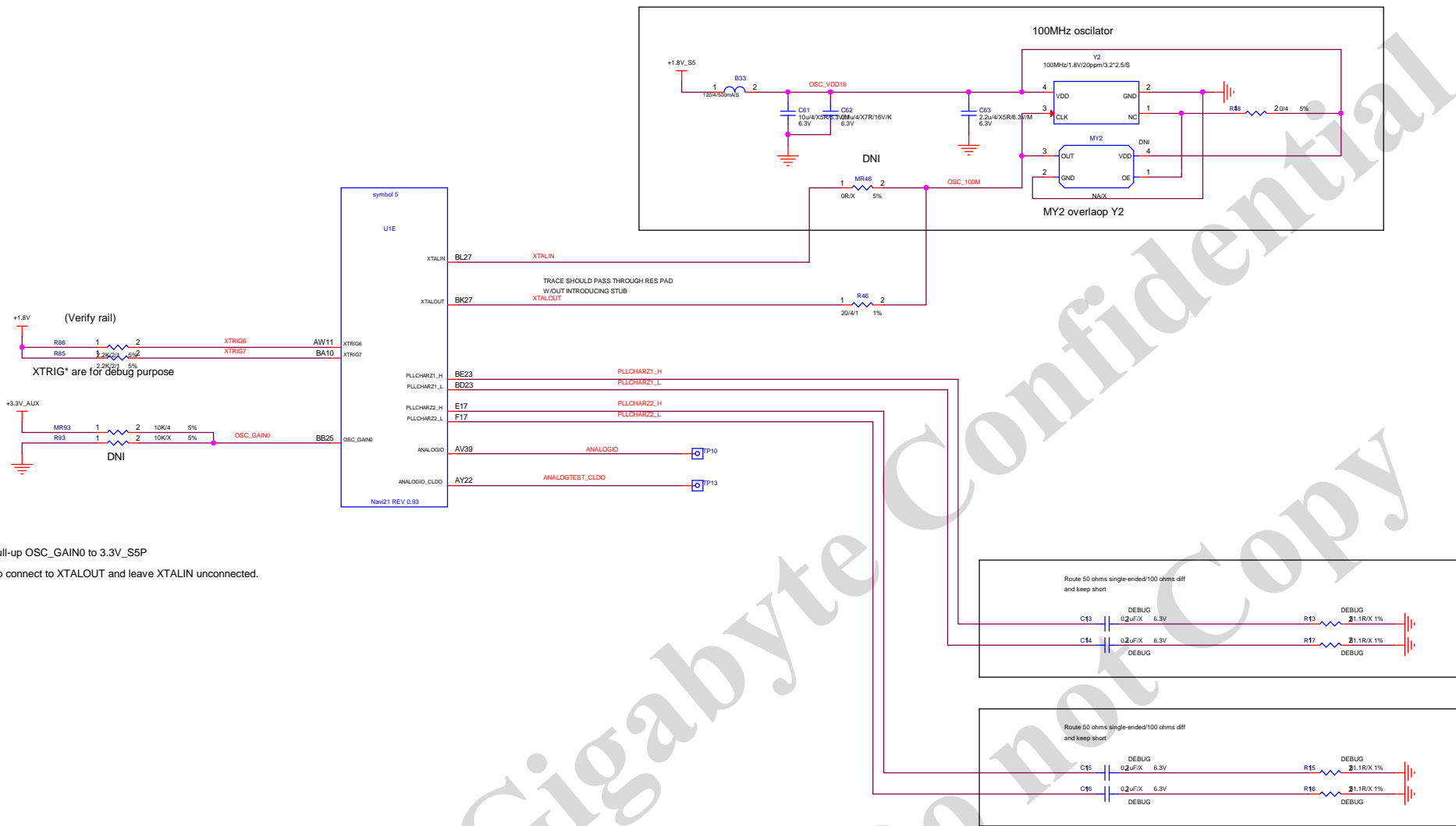
SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	GFX PHASES 8&9
2	NAVI 21 - PCIe Interface	27	GFX PHASES 11
3	NAVI 21 - GPIOs	28	GFX PHASES 5&7
4	NAVI 21 XTAL	29	GFX PHASES 3&10
5	XGMI	30	SOC PHASE 1&2
6	NAVI 21 MEM CH AB	31	VDD_MEM & VDDCI CONTROLLER
7	NAVI 21 MEM CH CD	32	VDD_MEM PHASES 1&2
8	NAVI 21 MEM CH EF	33	VDDCI_MEM PHASE 1
9	NAVI 21 MEM CH GH	34	NAVI 21 DECAPS
10	GDDR6 MEM CH CD	35	NAVI 21 POWER
11	GDDR6 MEM CH EF	36	NAVI 21 POWER and GND
12	GDDR6 MEM CH GH	37	POWER_MANAGEMENT
13	GDDR6 MEM CH AB	38	ClampWA
14	NAVI21 TMDPA - USB-C	39	SVI2 & BxMACO
15	NAVI21 TMDPF - HDMI	40	THERMAL
16	NAVI21 TMDPC&E - DP	41	DPM_Status_LED & GDDR6_JTAG
17	NAVI21 TMDPA	42	PI Debug
18	NAVI21 USB	43	DEBUG
19	PD Controller	44	History
20	USB-C PORT 1		
21	USB_5V_1.8V_0.75V		
22	MODS CONTROL & POWER		
23	GFX & SOC CONTROLLER		
24	GFX PHASES 1&2		
25	GFX PHASES 4&6		





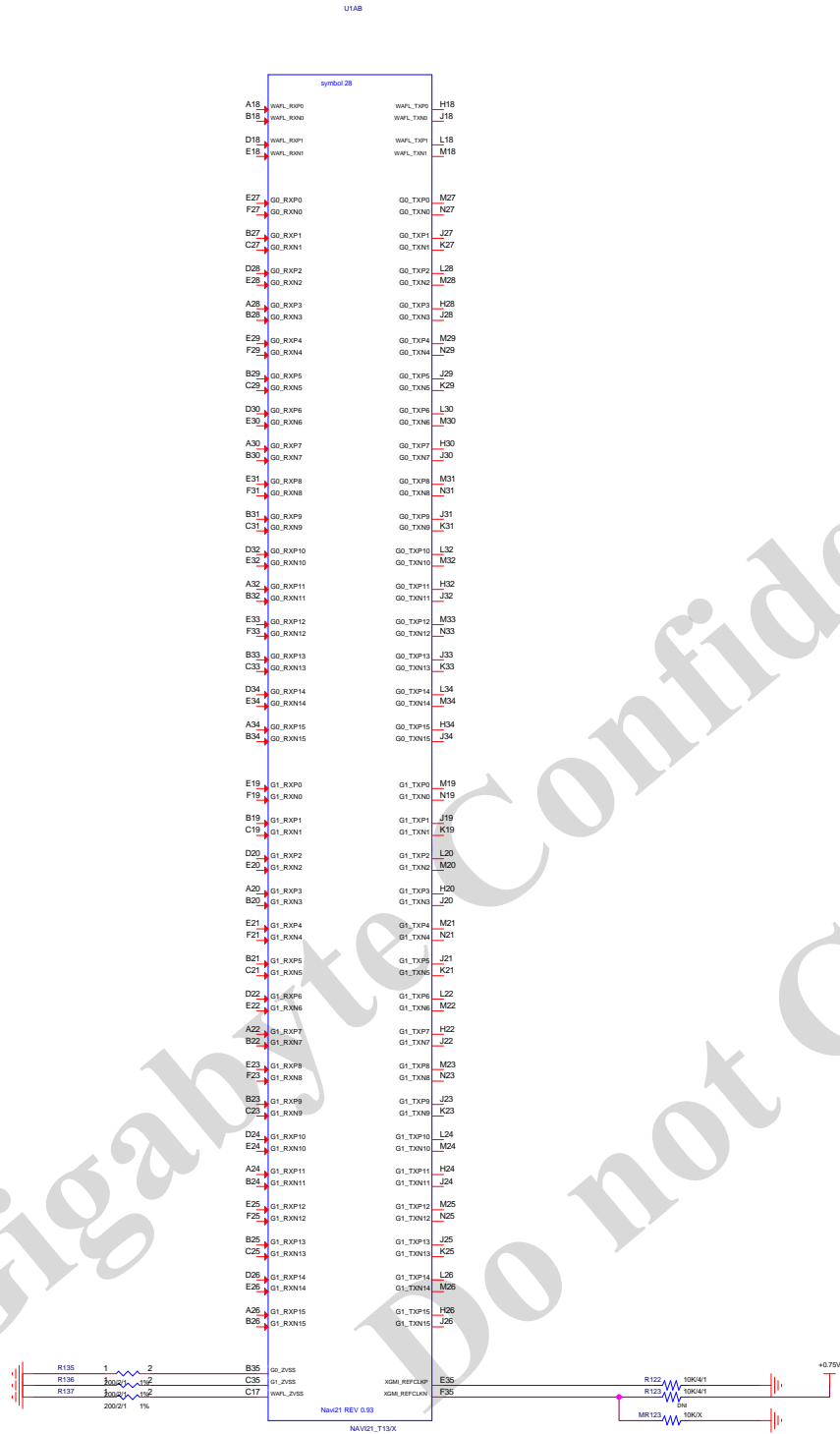
Note: Internal PU/PD at GPIO pad is 40k strength in 14nm design spec

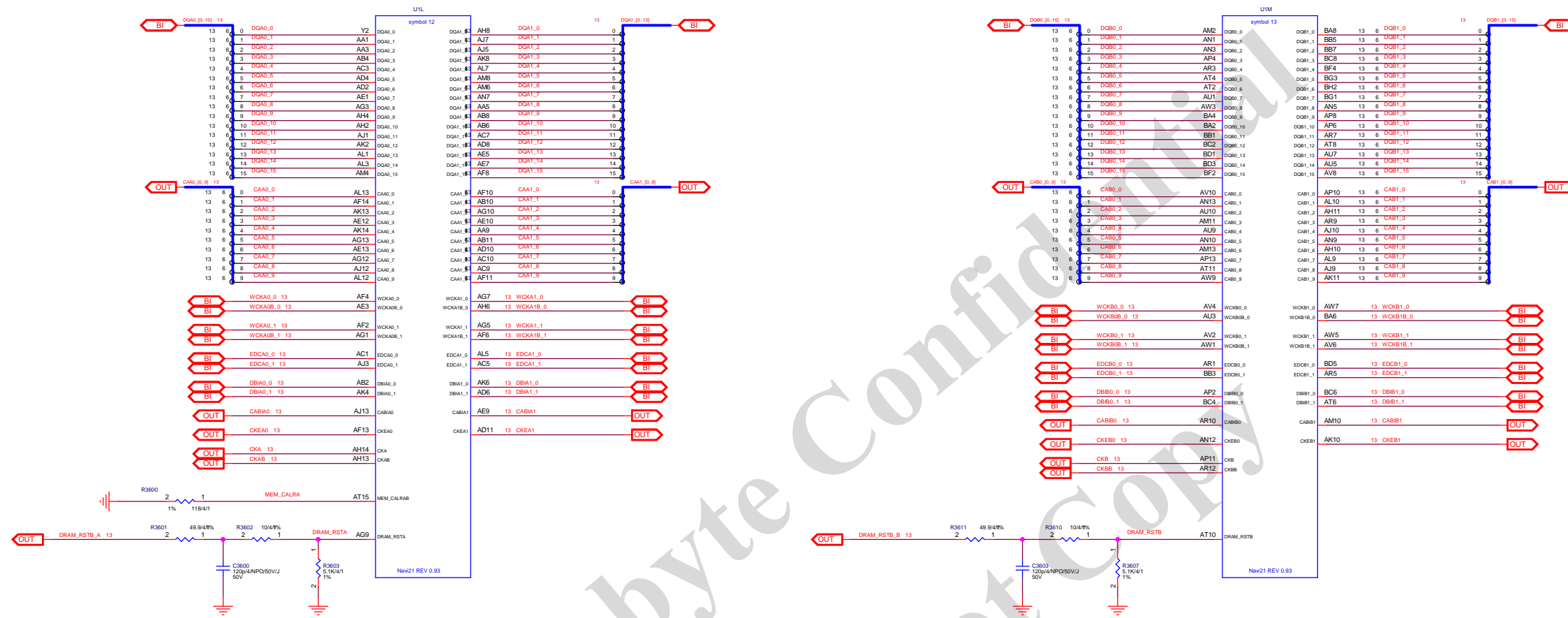


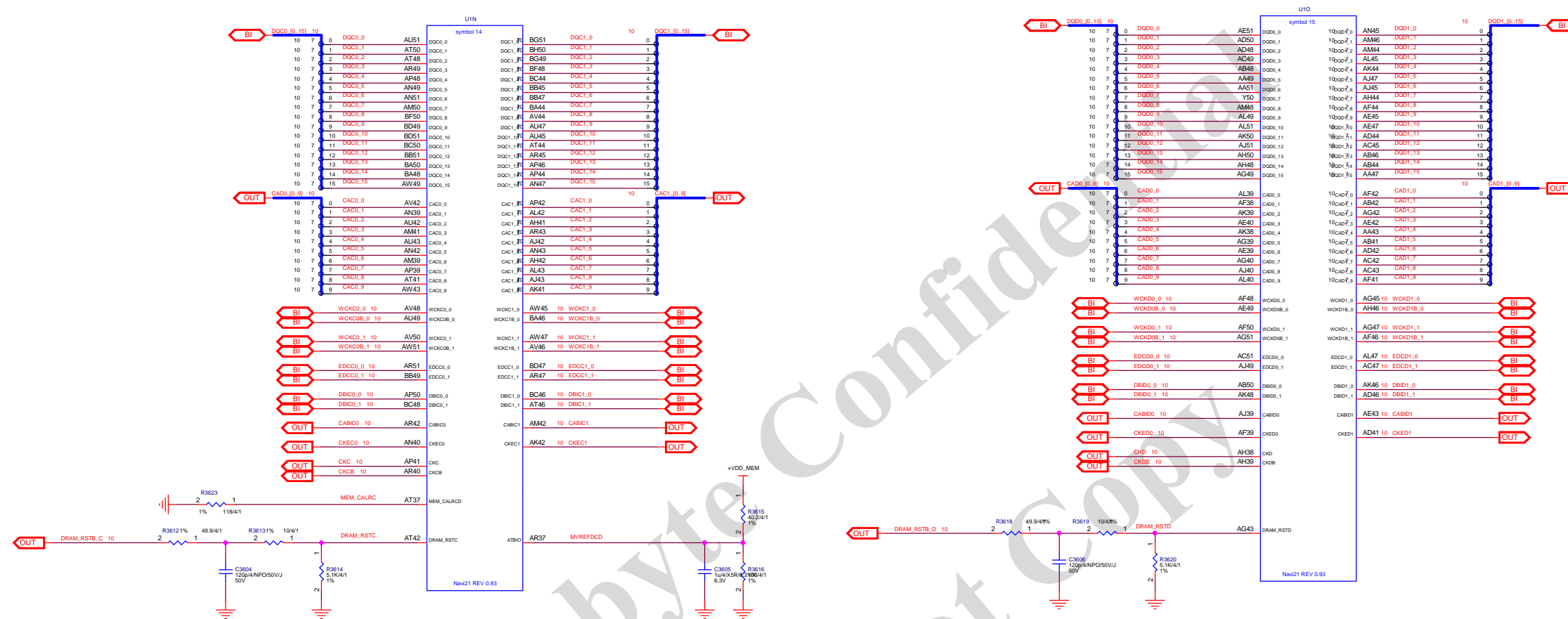


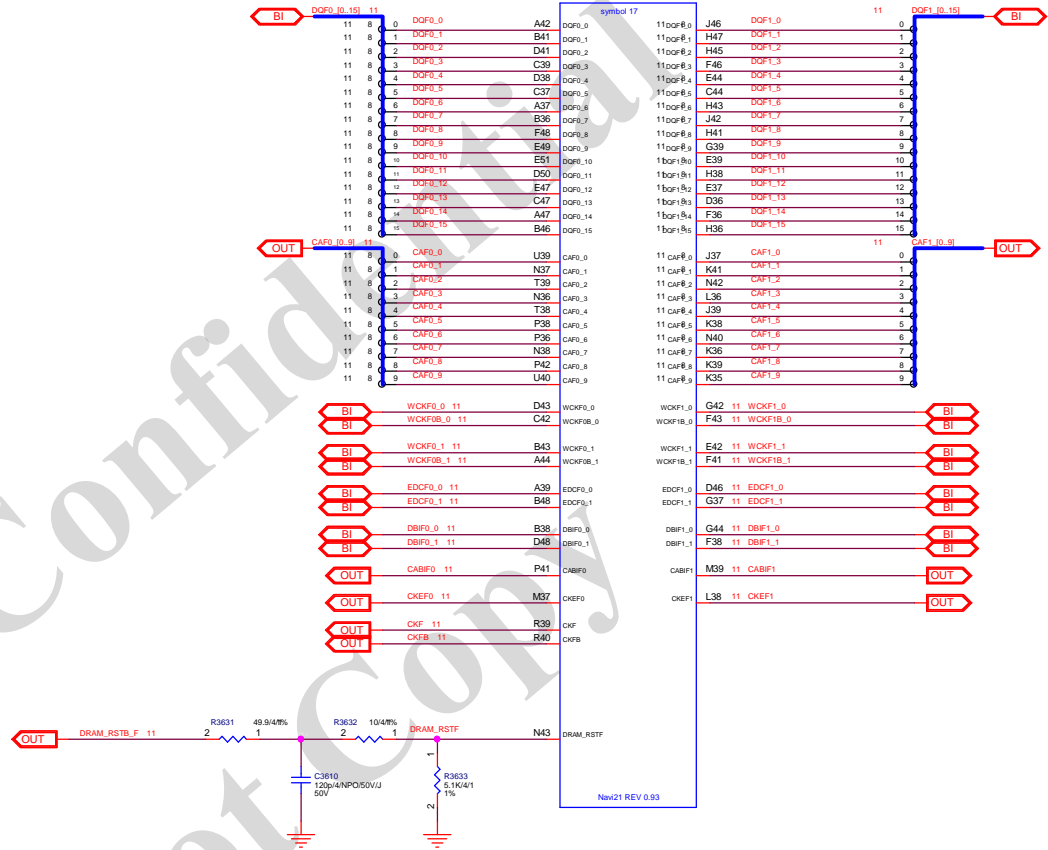
Default OSC_GAIN is 0x7. Pull-up OSC_GAIN0 to 3.3V_S5P
When 0x7, external clock chip connect to XTALOUT and leave XTALIN unconnected.

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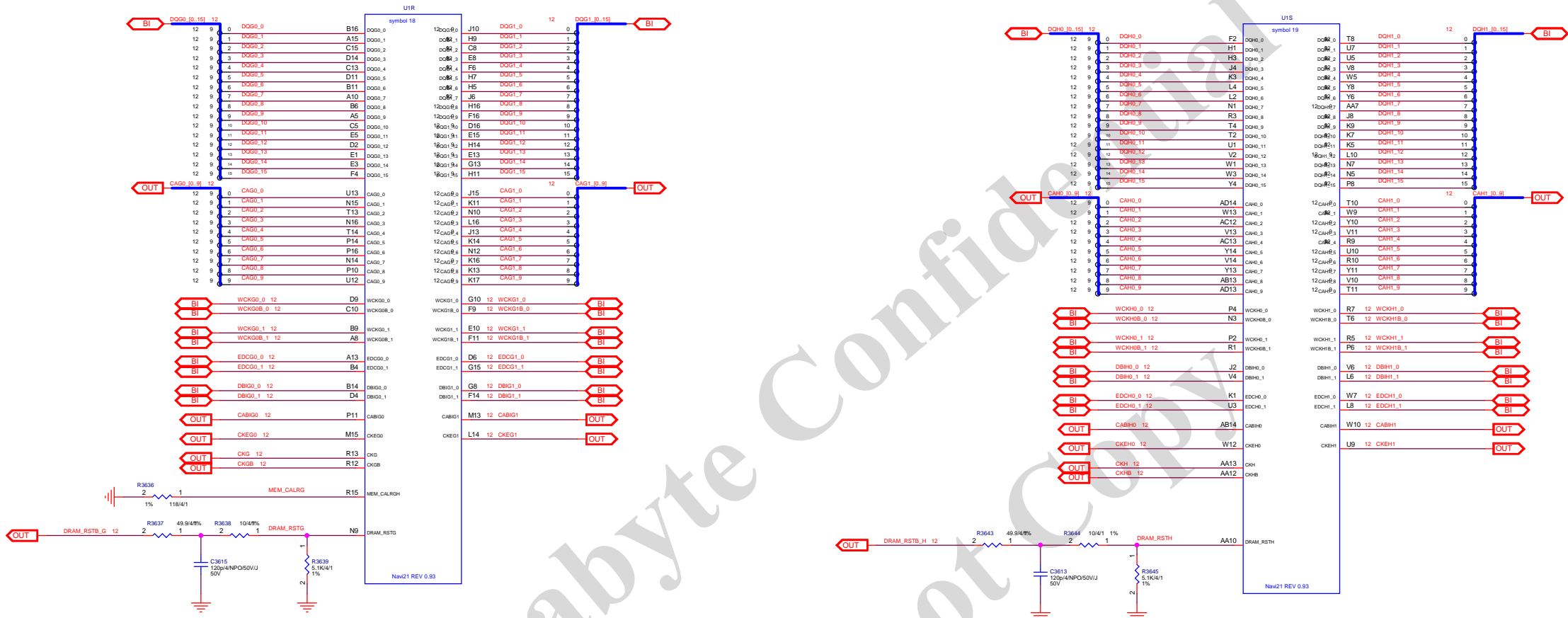


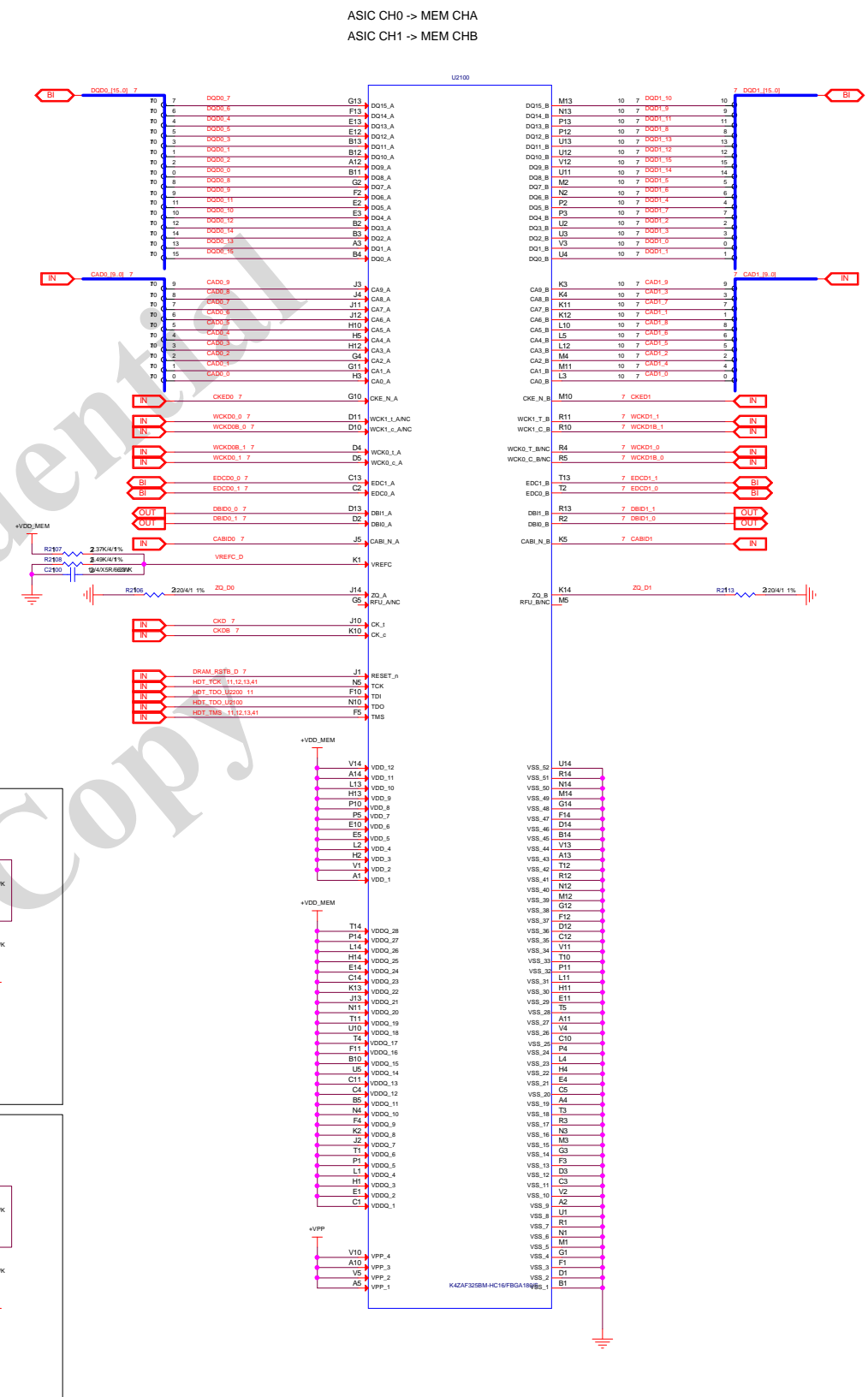
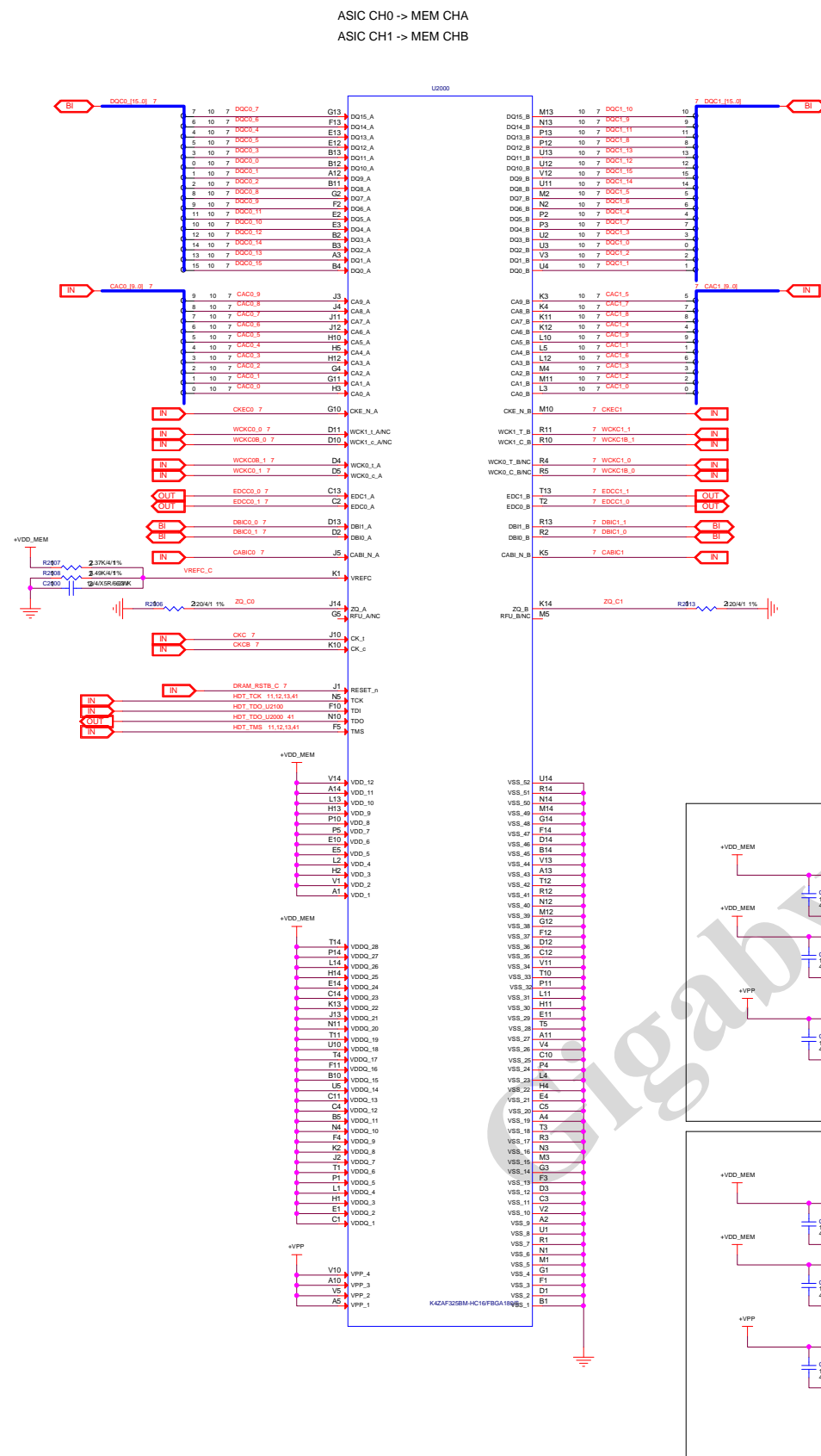


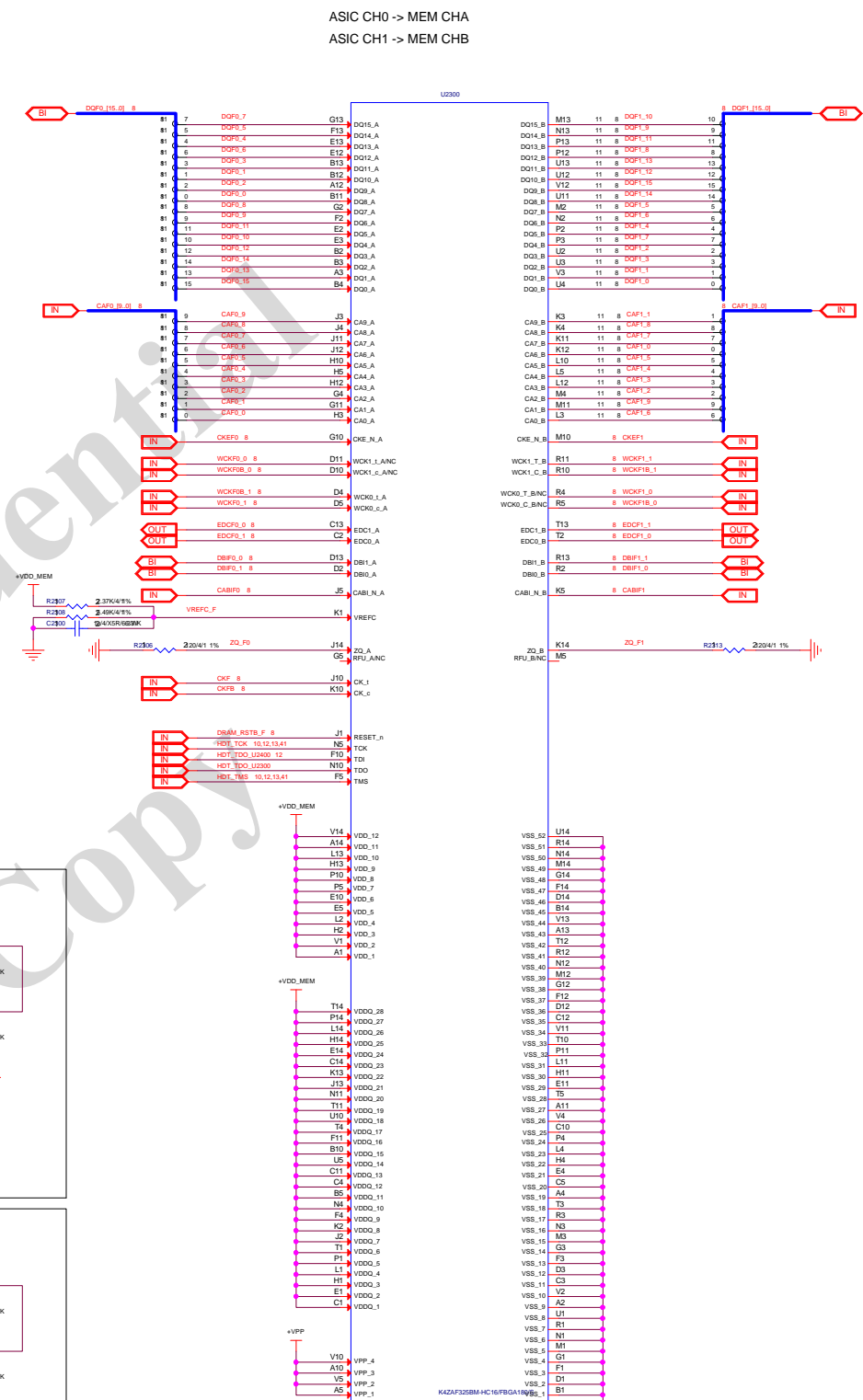
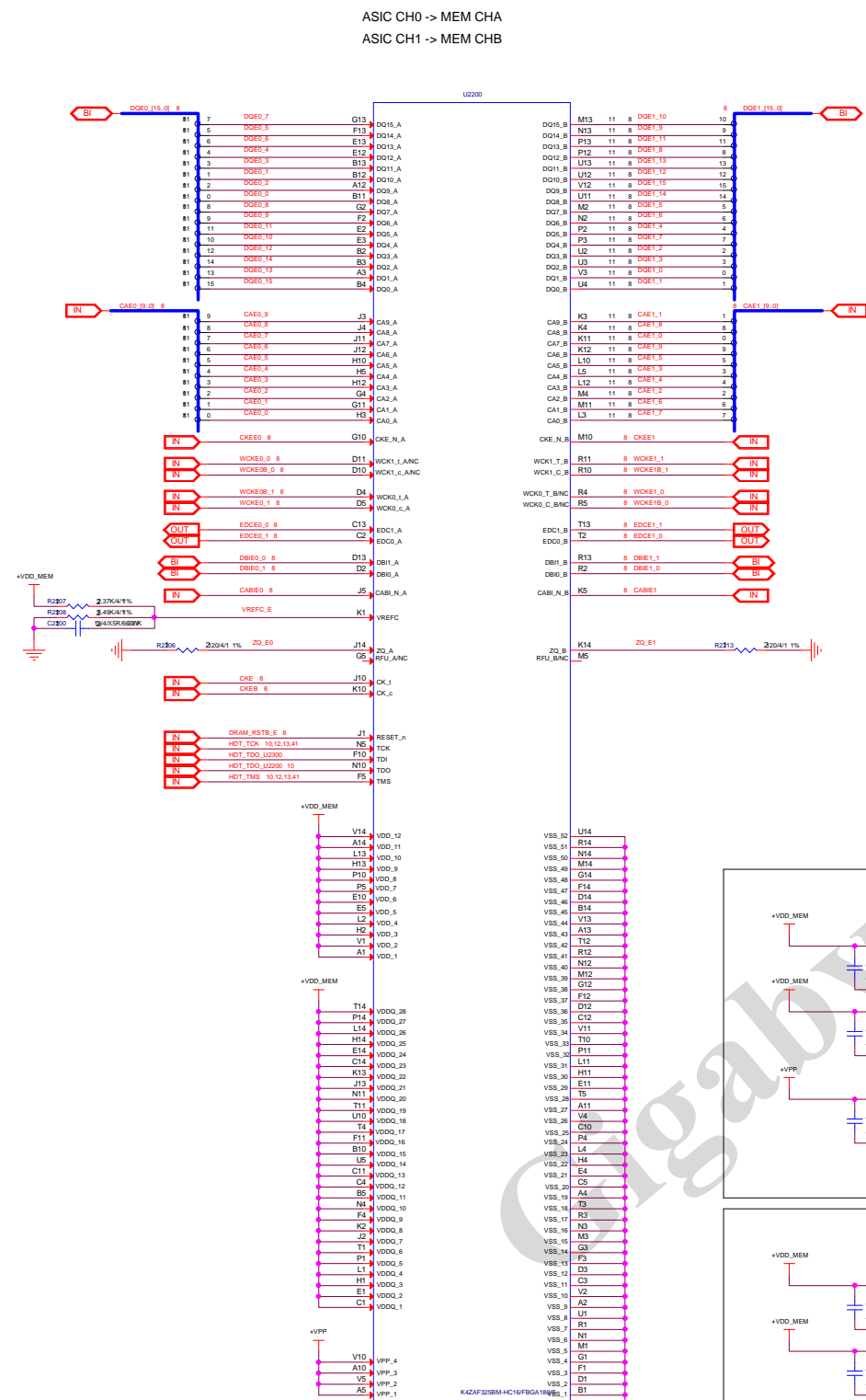


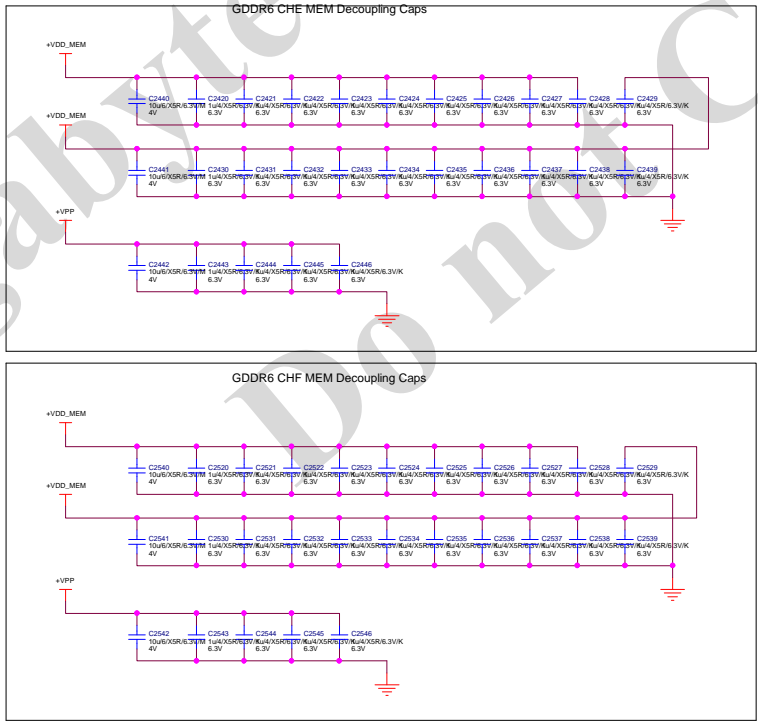
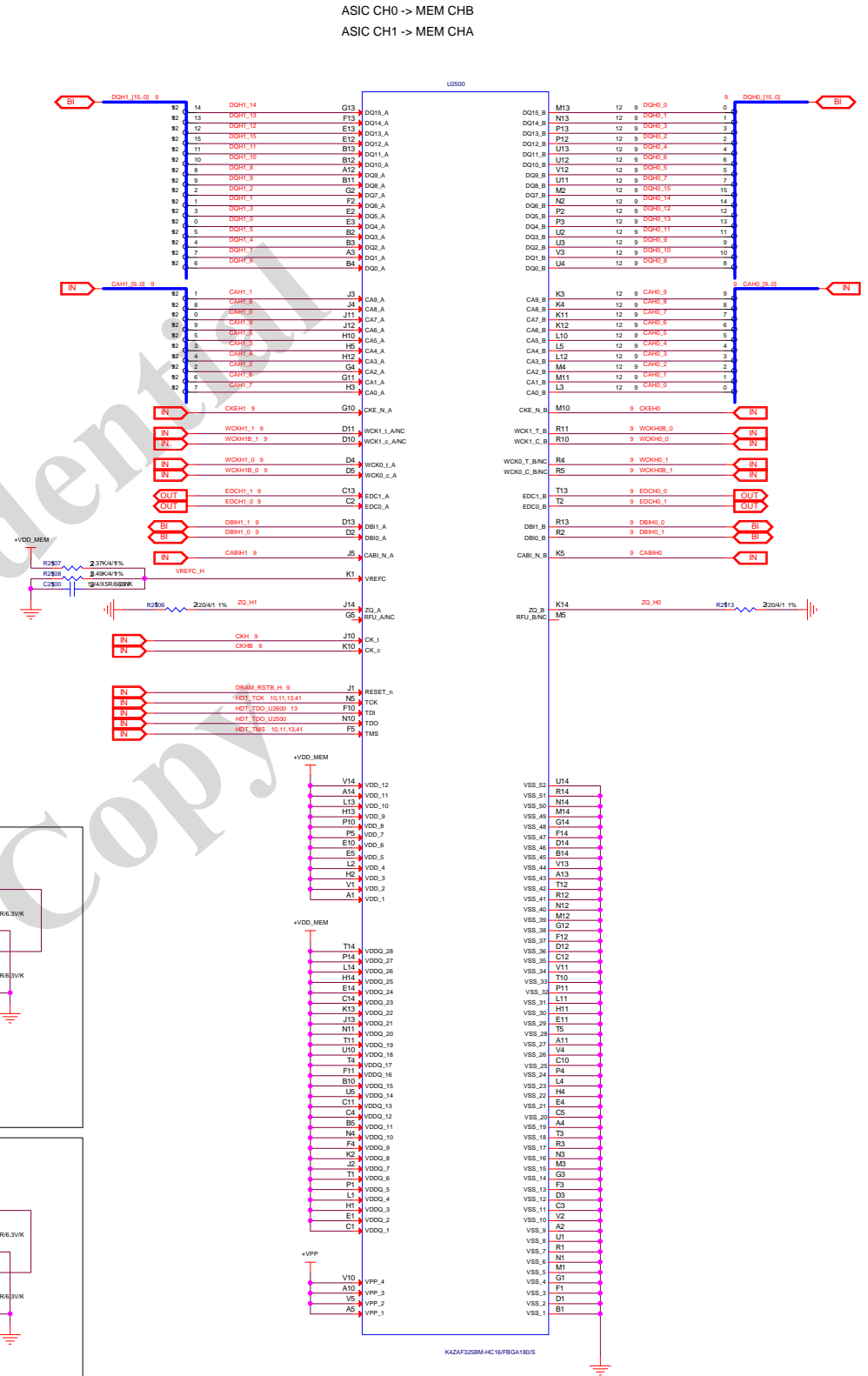
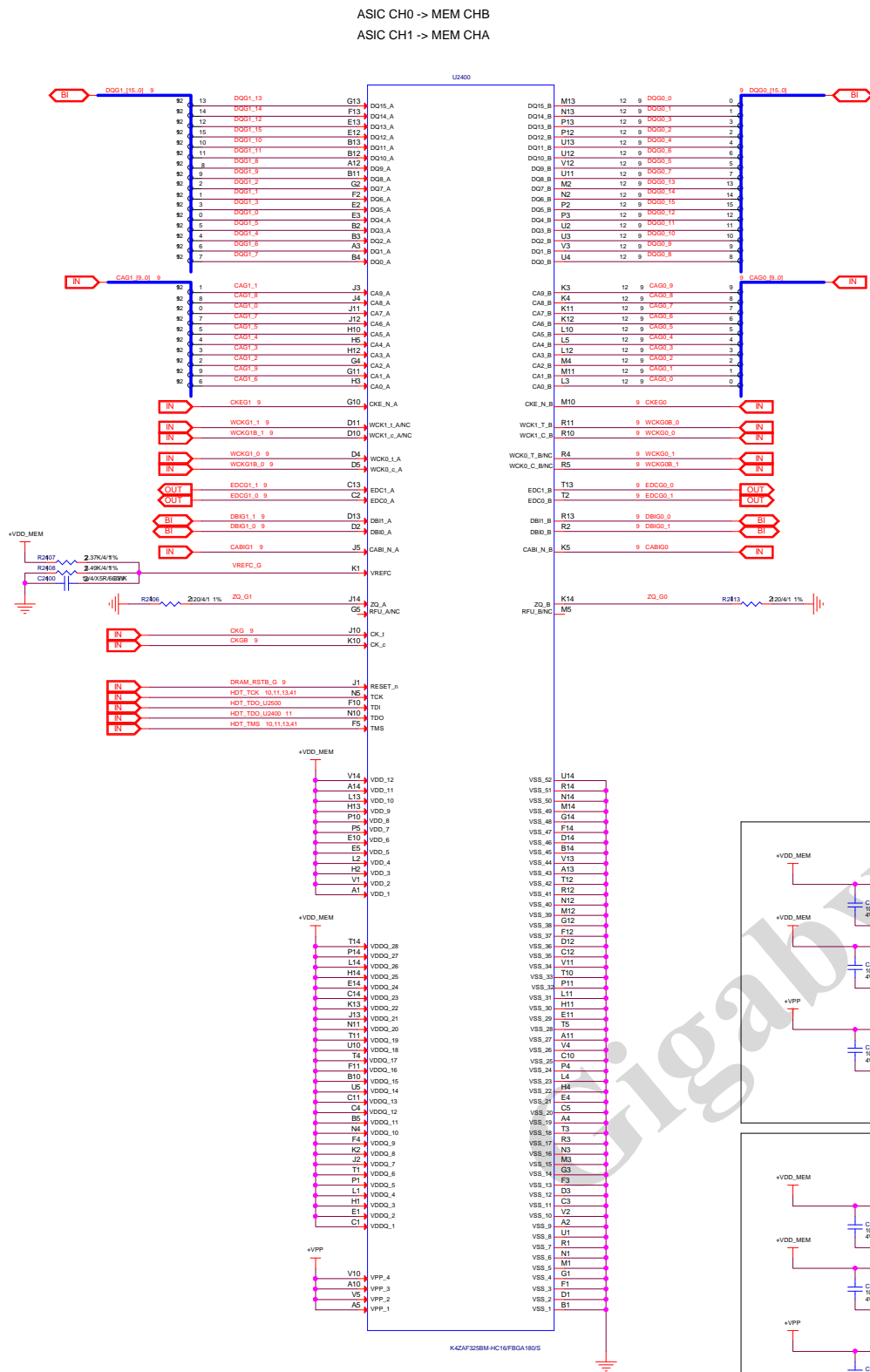


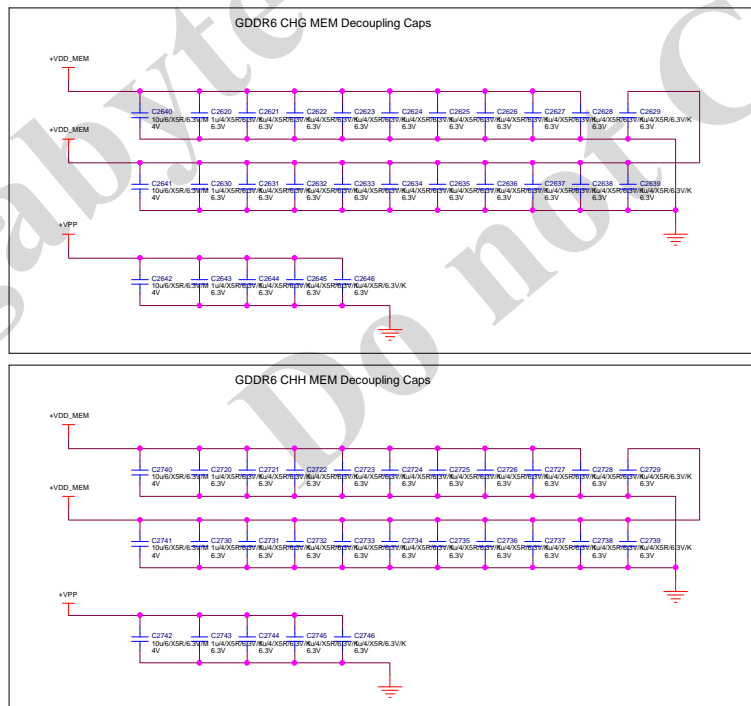
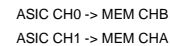
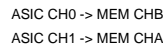
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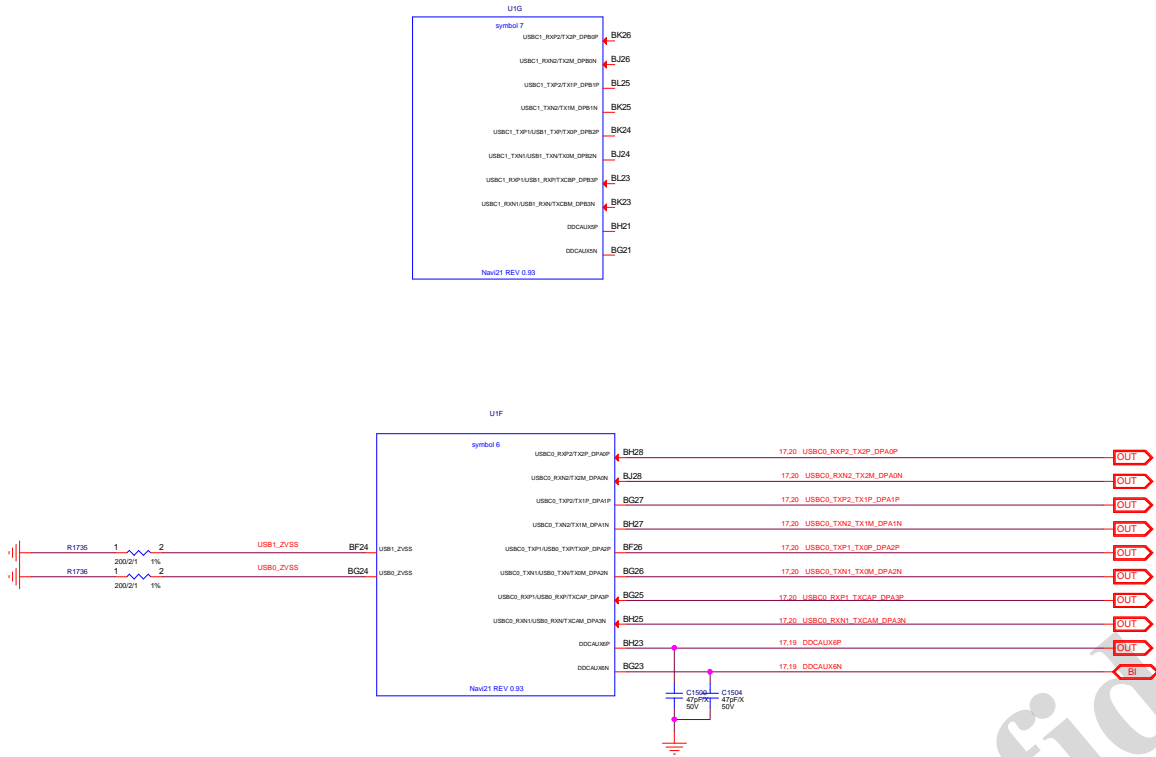




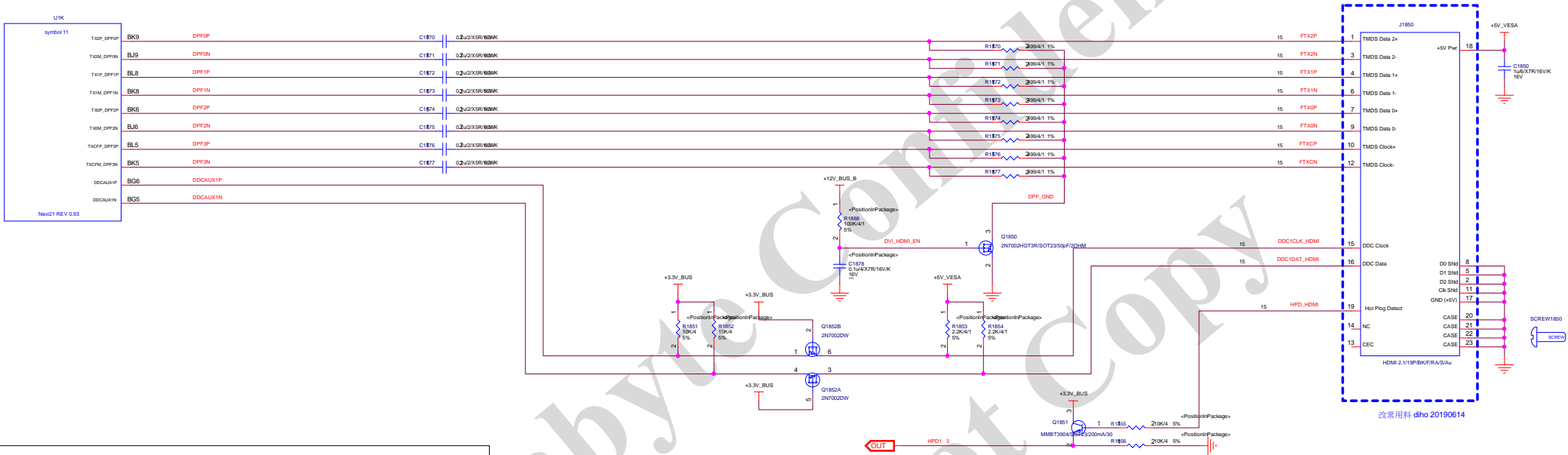




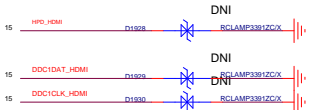
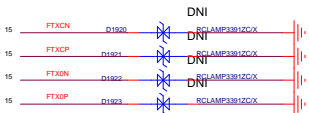


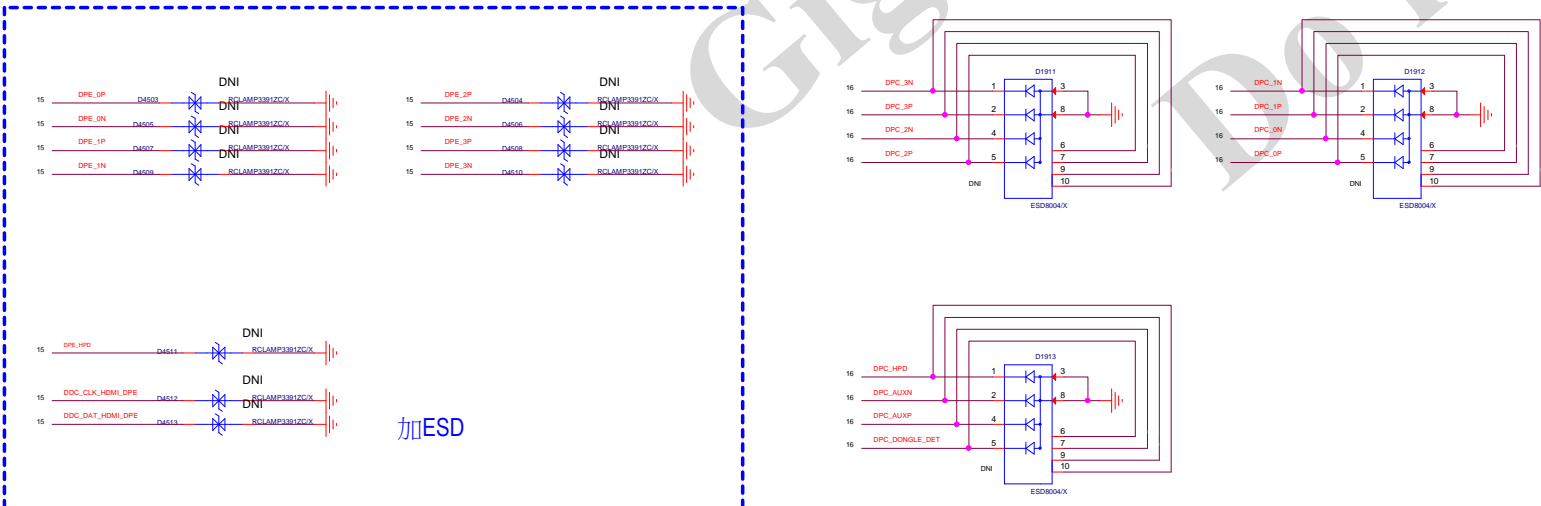
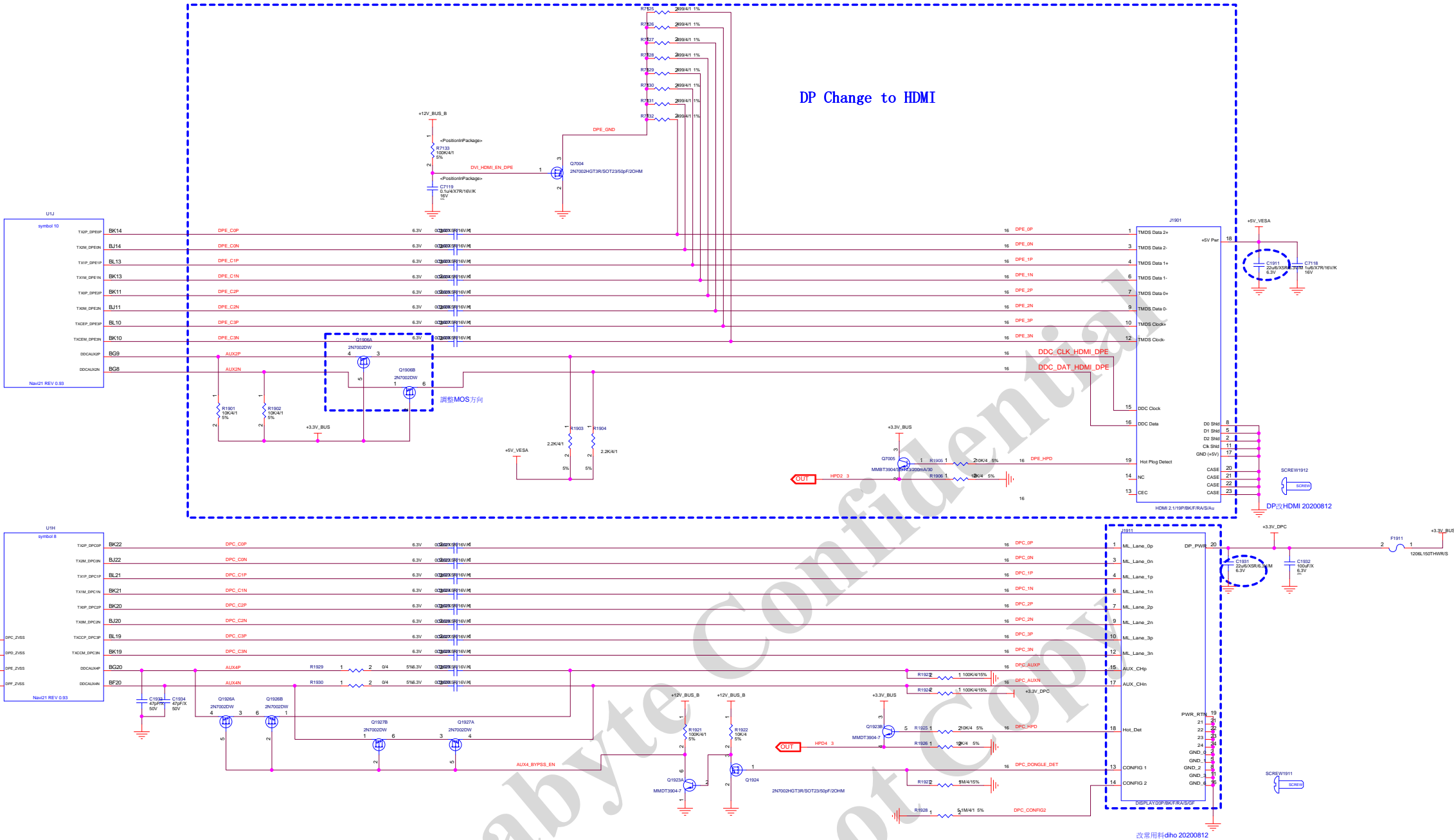


U11		
symbol 9	TX0P_DP0P	BK18
	TX0M_DP0M	BL18
	TX1P_DP1P	BL17
	TX1M_DP1M	BK17
	TX2P_DP2P	BK16
	TX2M_DP2M	BL16
	TX3P_DP3P	BL15
	TX3M_DP3M	BK15
	DDCAUXP	BG14
	DDCAUXN	BF14
NAVI21 REV 0.93		

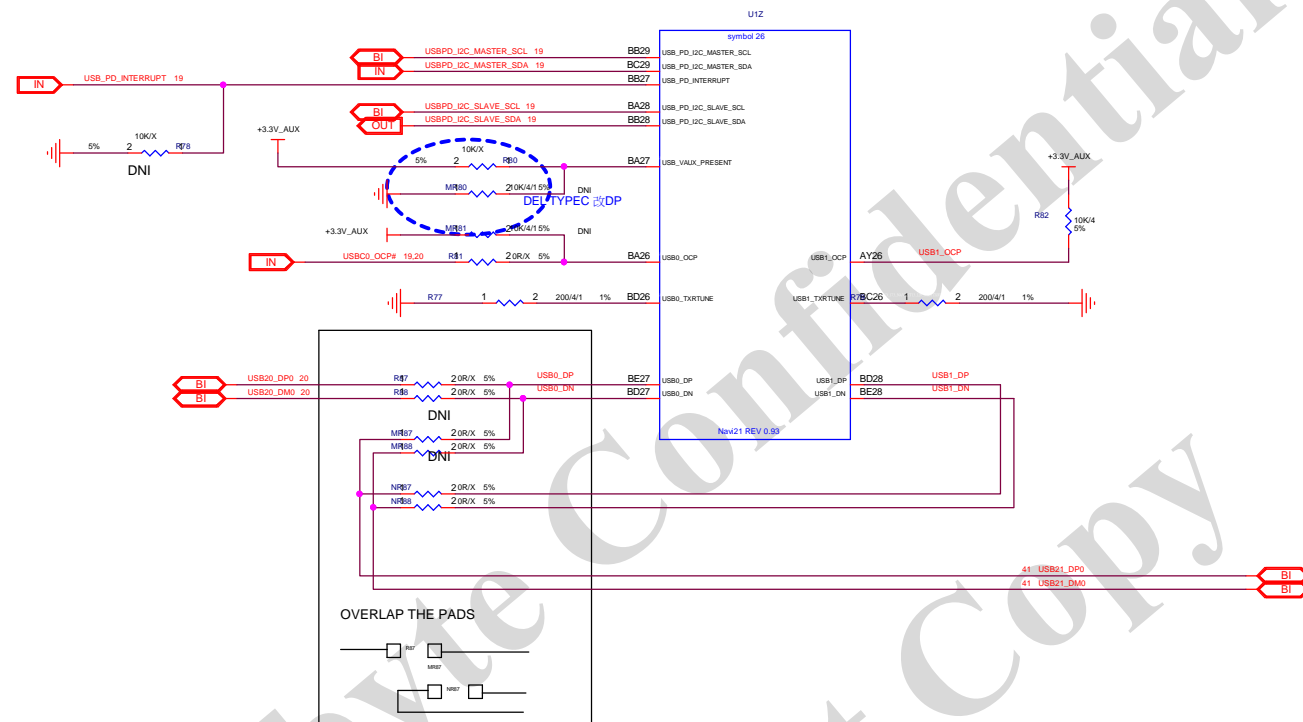


OPTIONAL ESD PROTECTION DIODES

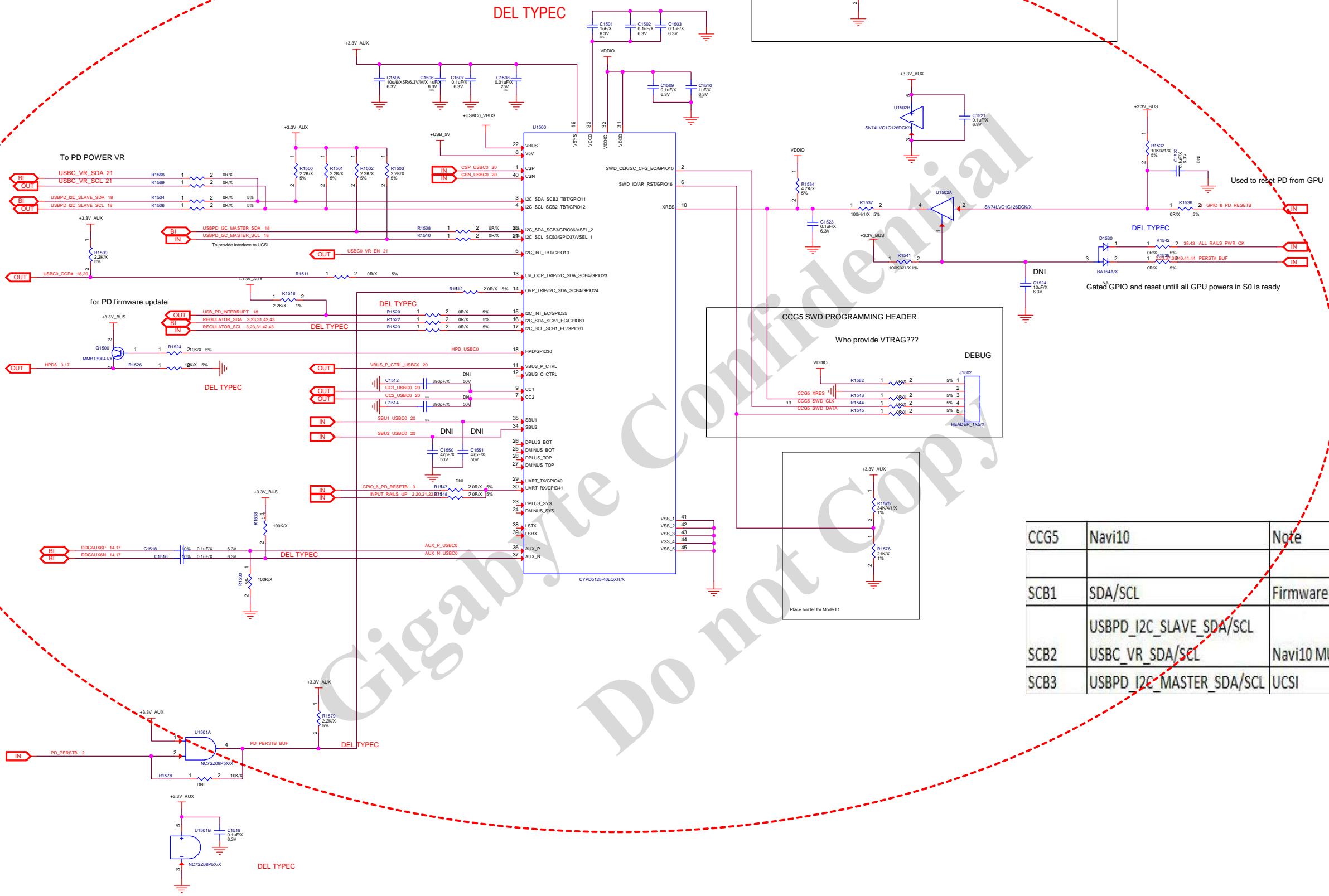




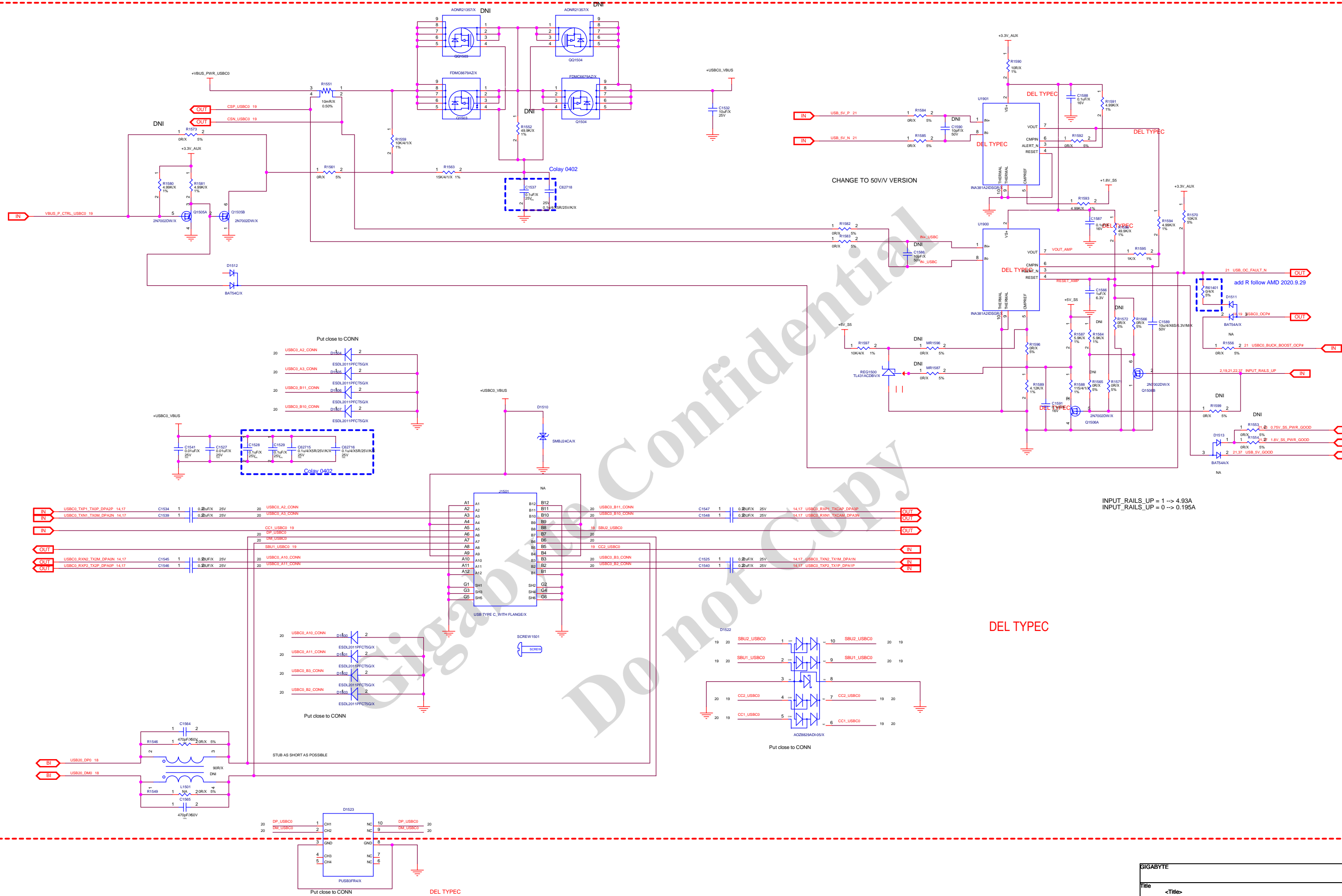
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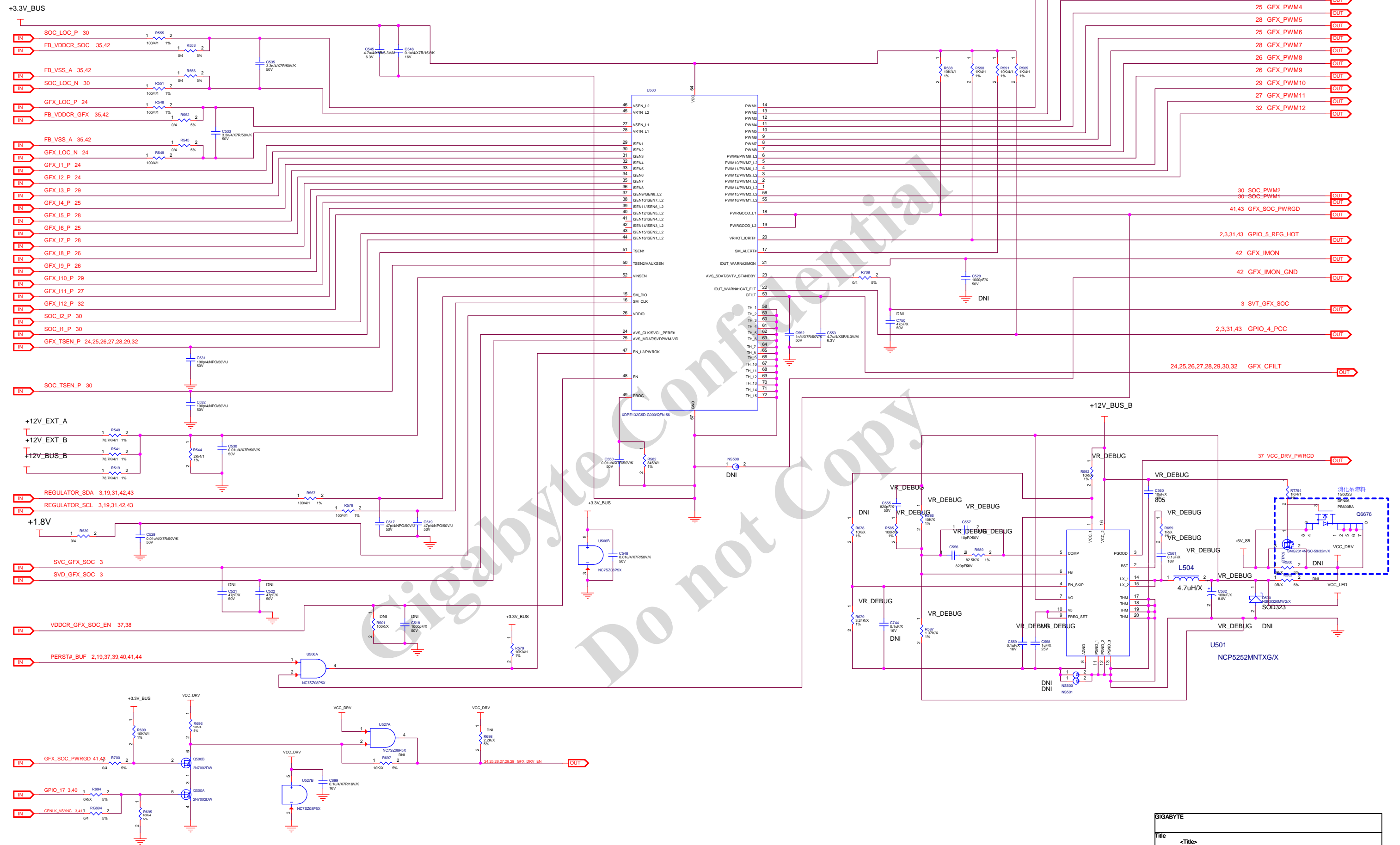
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SCB1	SDA/SCL	Firmware update/SMU
	USBPD_I2C_SLAVE_SDA/SCL	
SCB2	USBC_VR_SDA/SCL	Navi10 MUX/PD_Regulator/re-driver
SCB3	USBPD_I2C_MASTER_SDA/SCL	UCSI

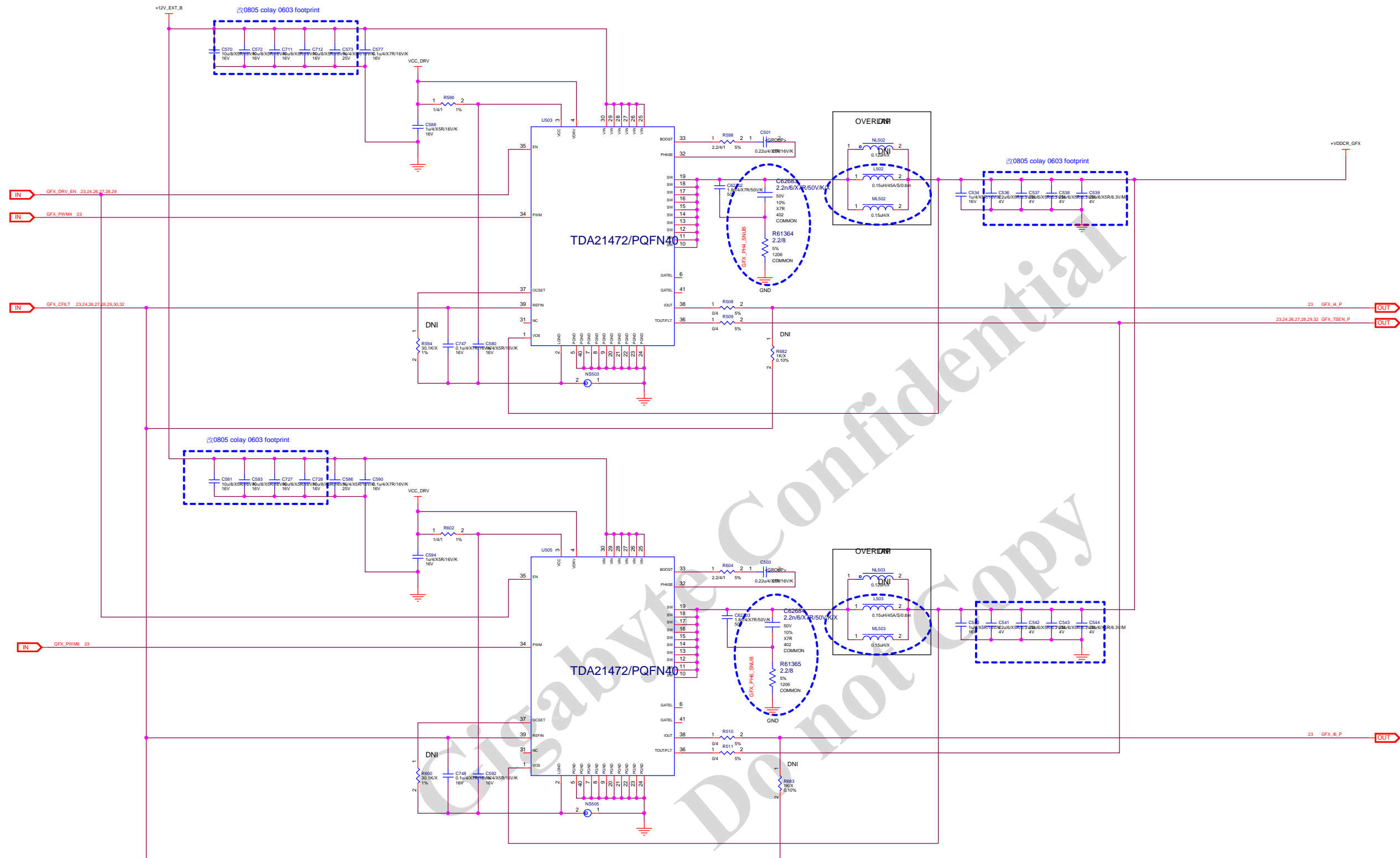


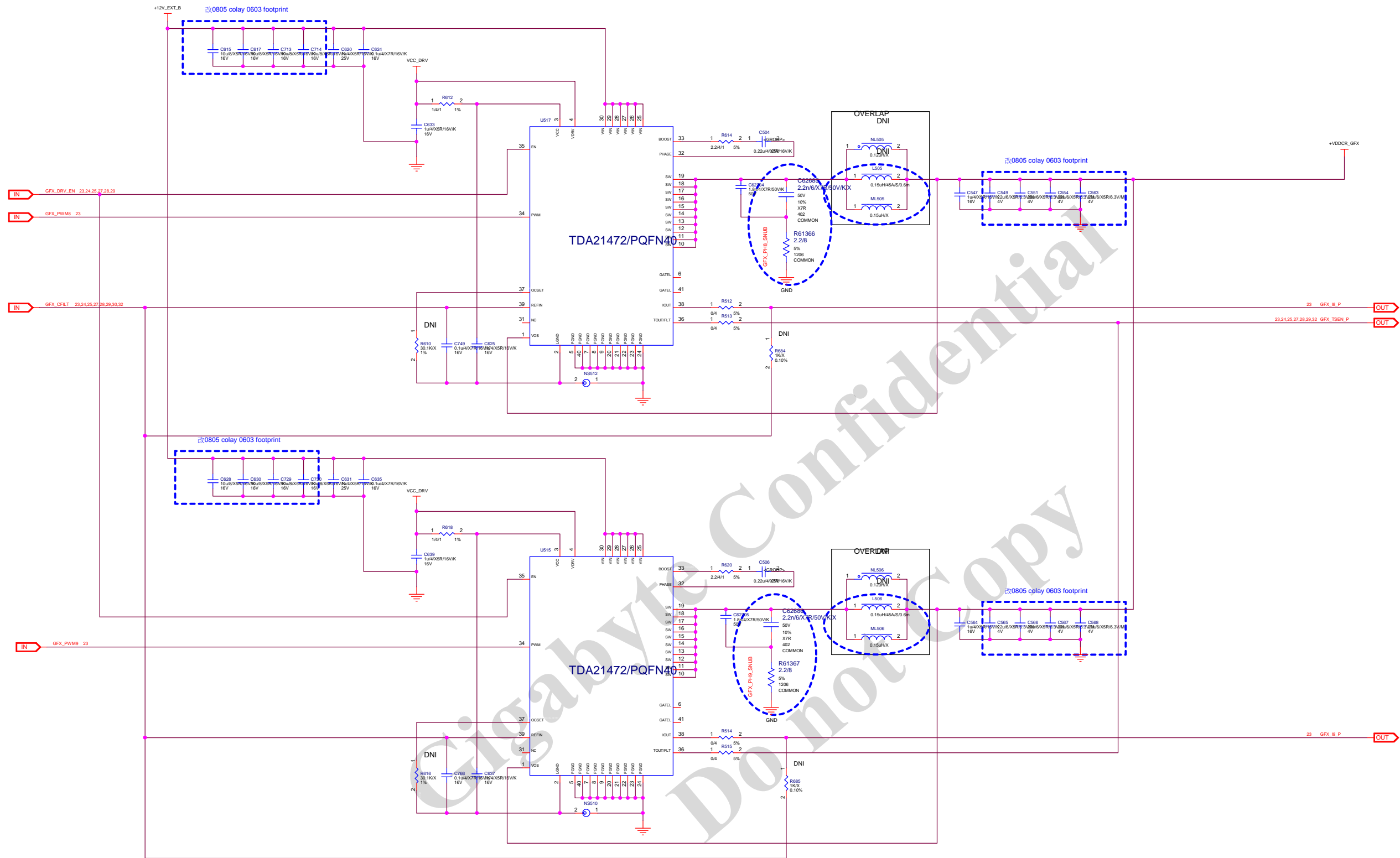
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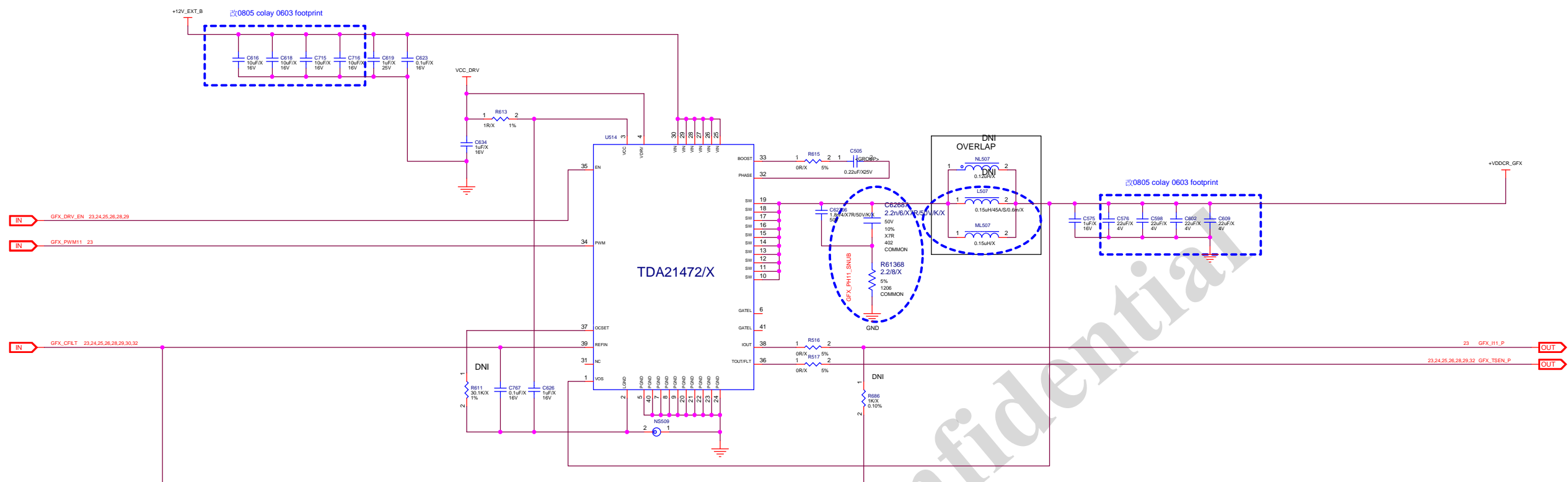
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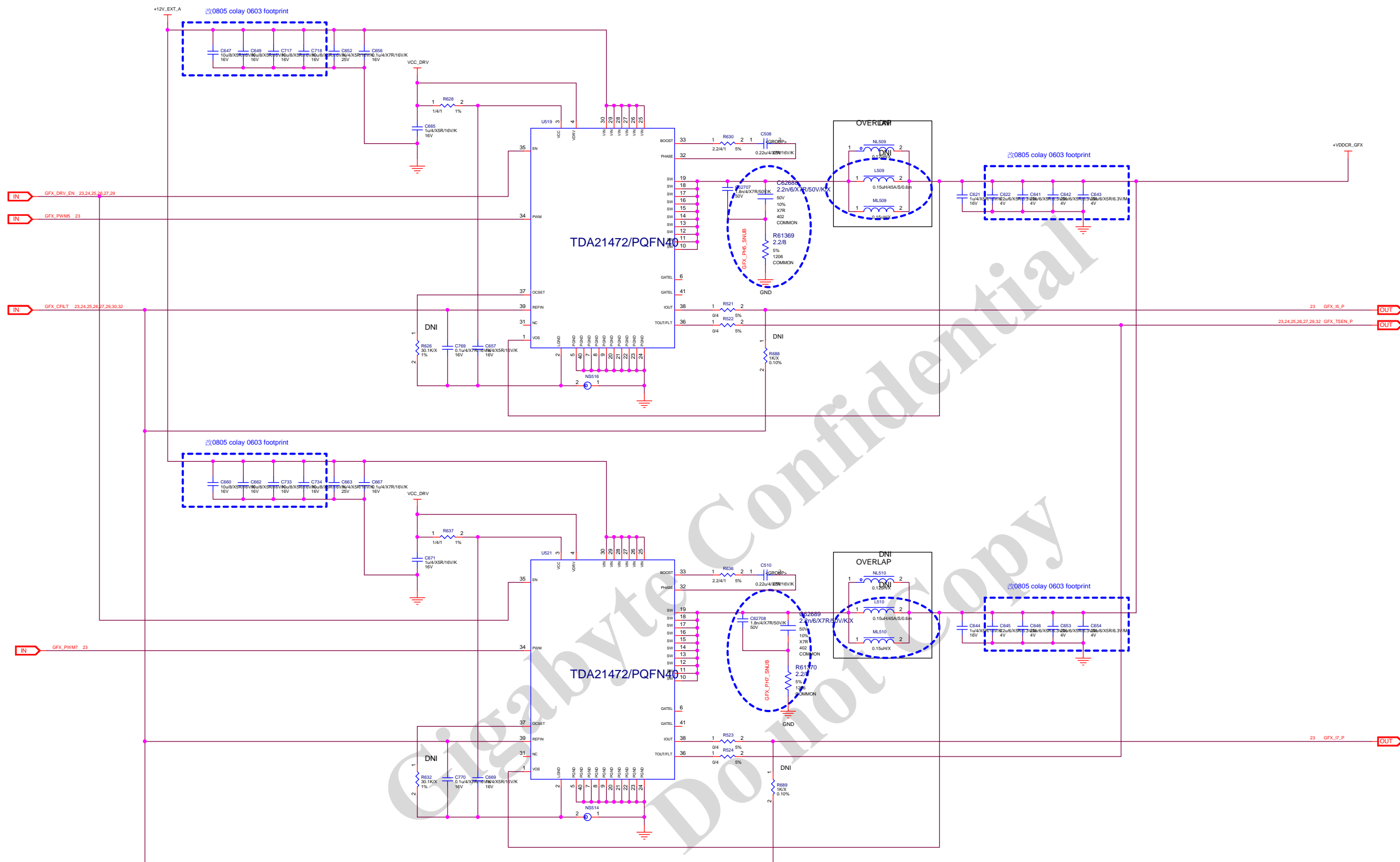
(14) GFX & SOC CONTROLLER

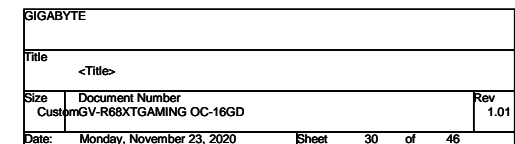




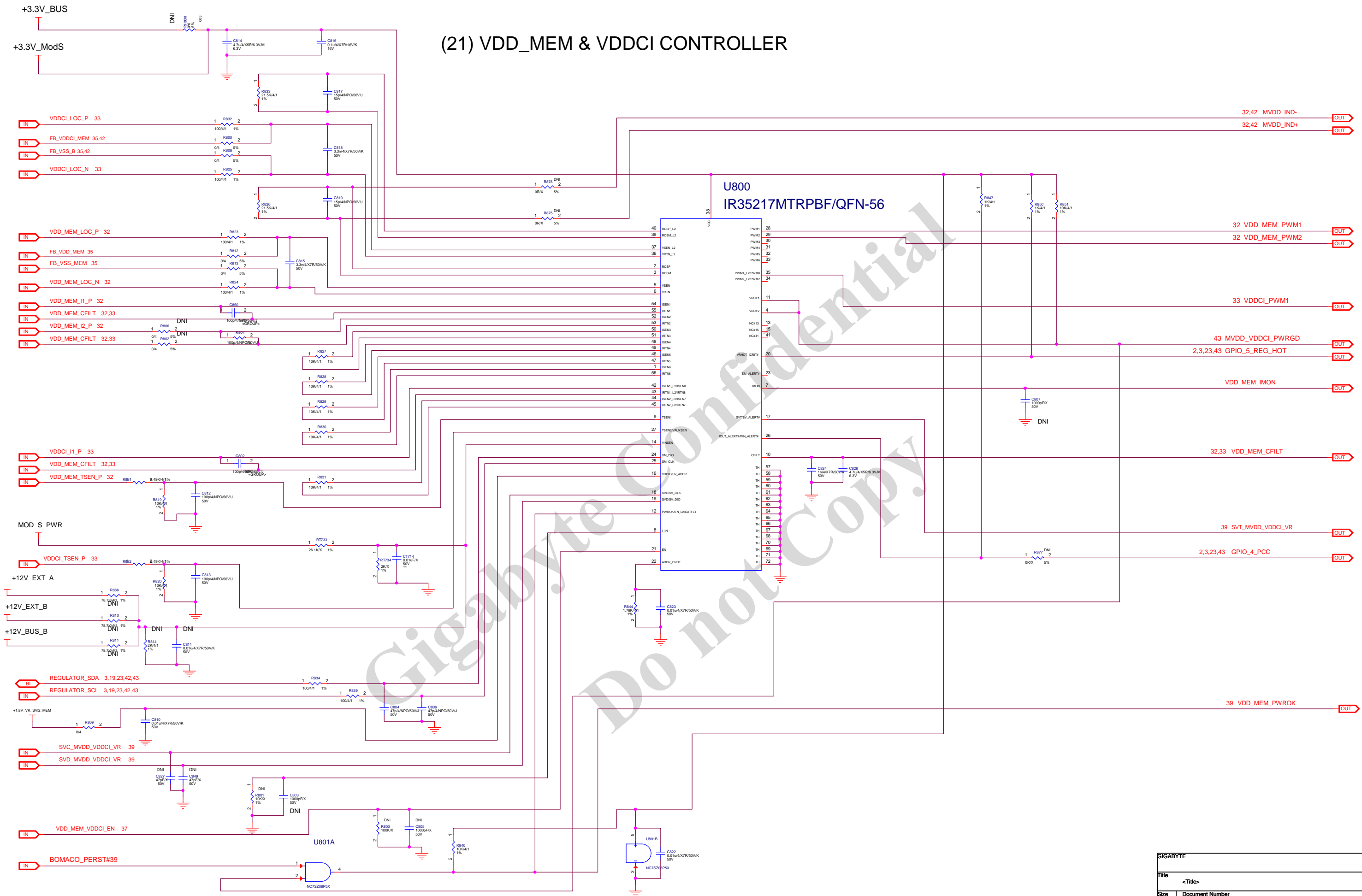




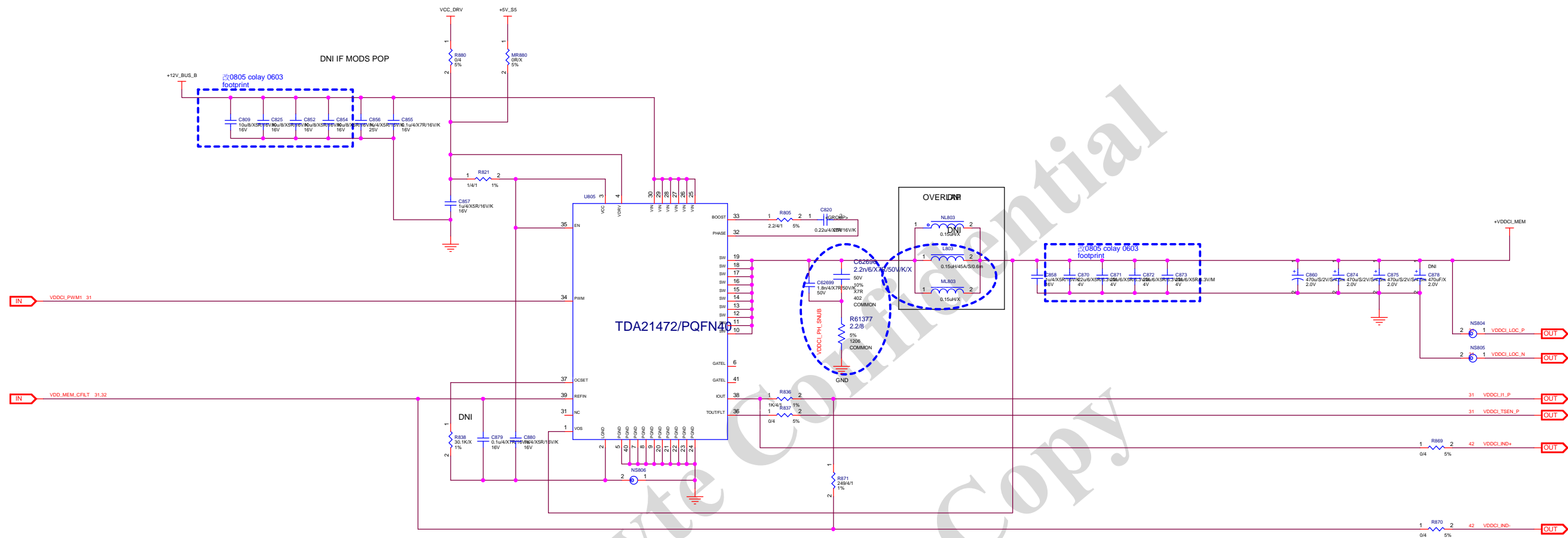


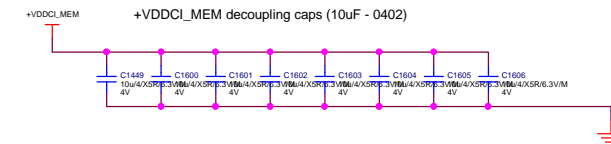
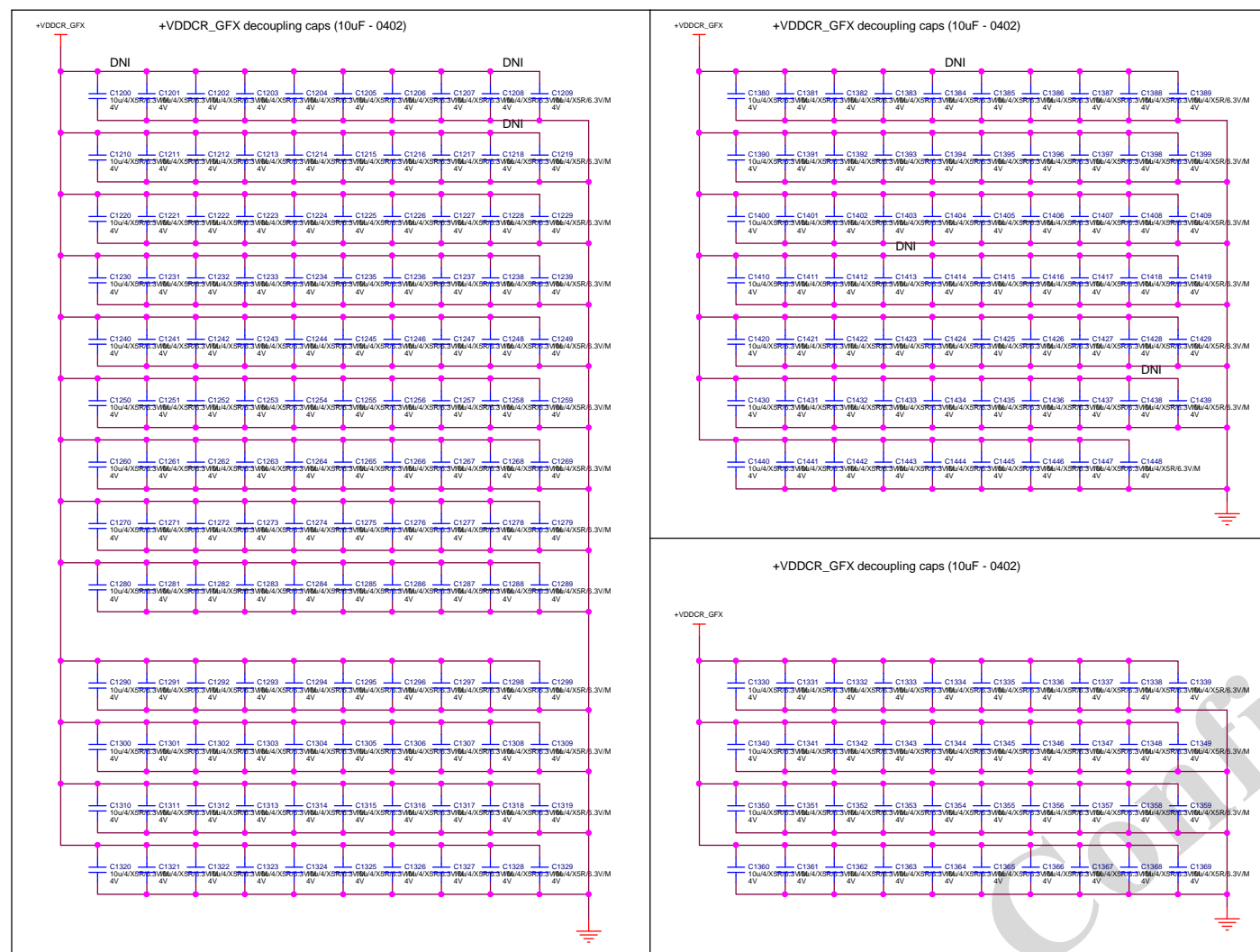


(21) VDD_MEM & VDDCI CONTROLLER



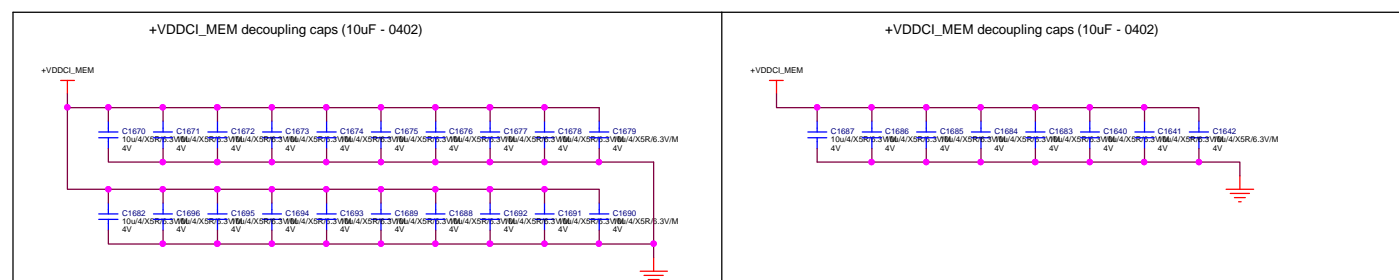
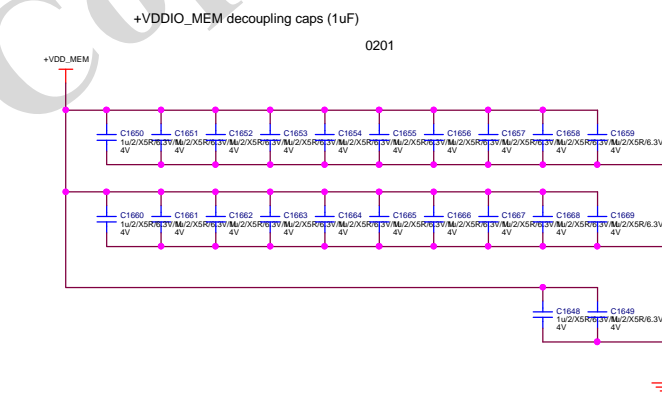
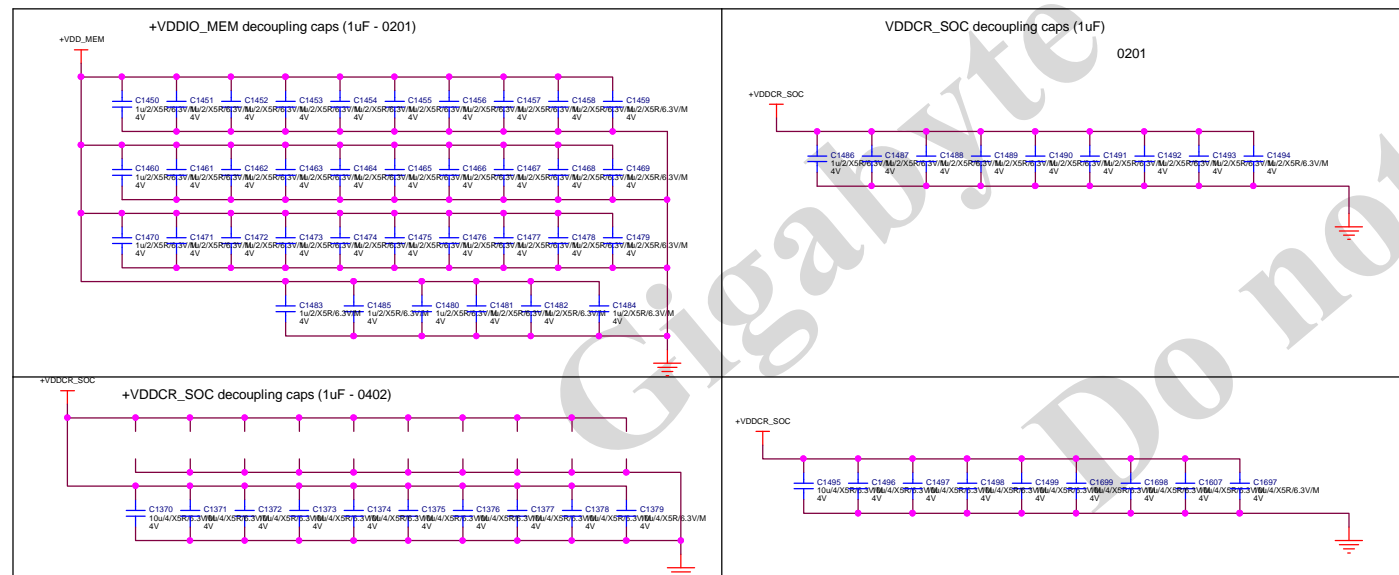
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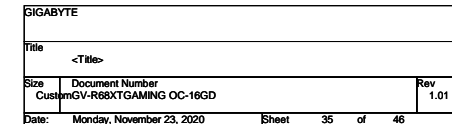


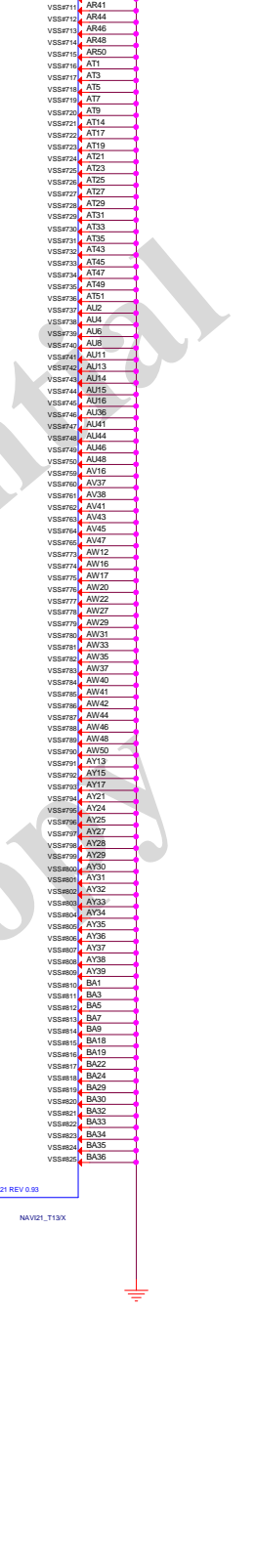
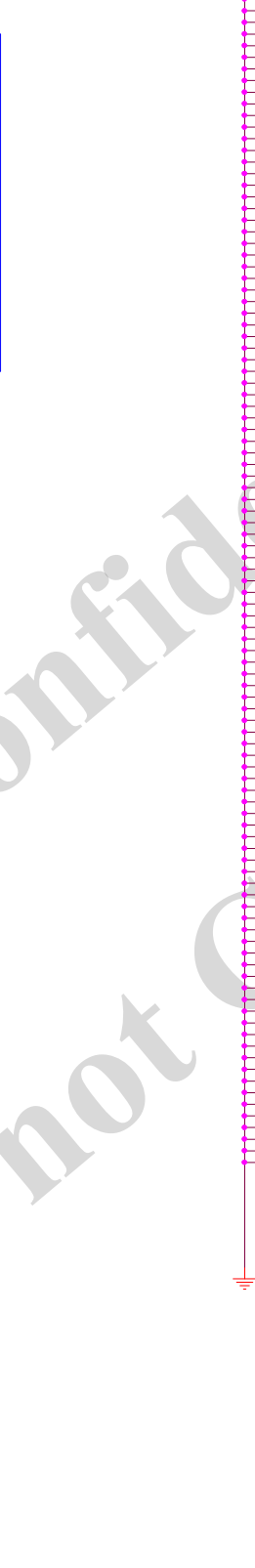
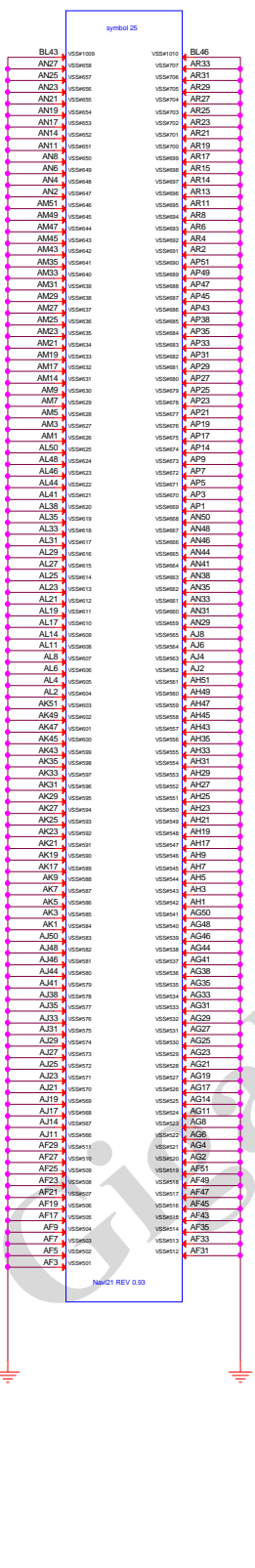
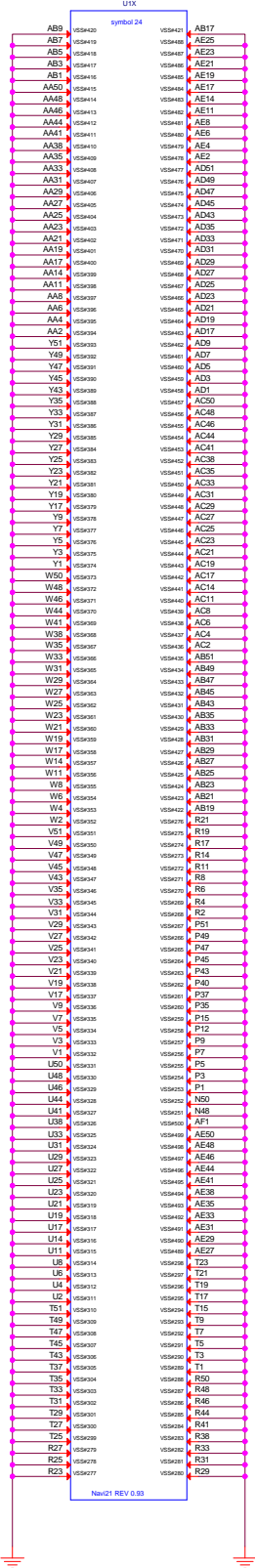
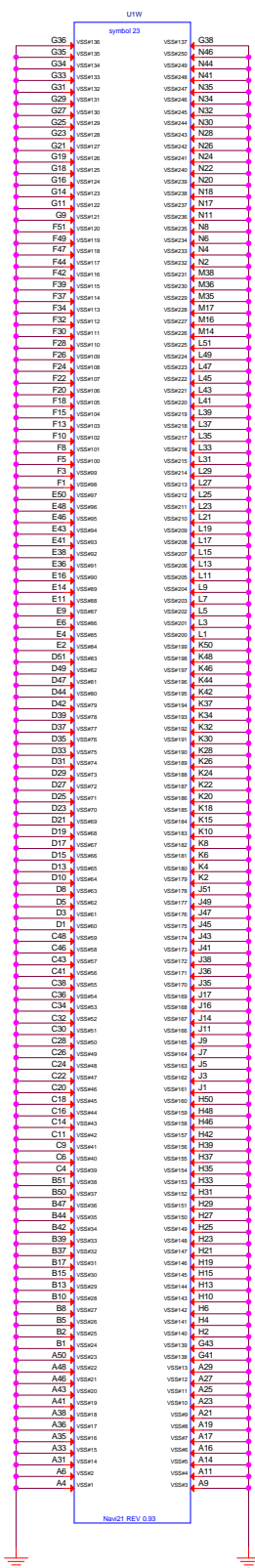


DNI these six caps to match SLT board and keep the design consistent across SKUs

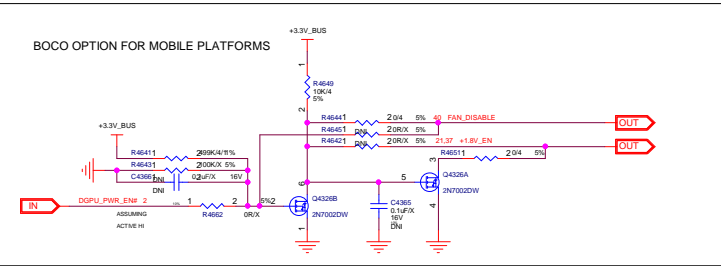
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- C1208
- C1200
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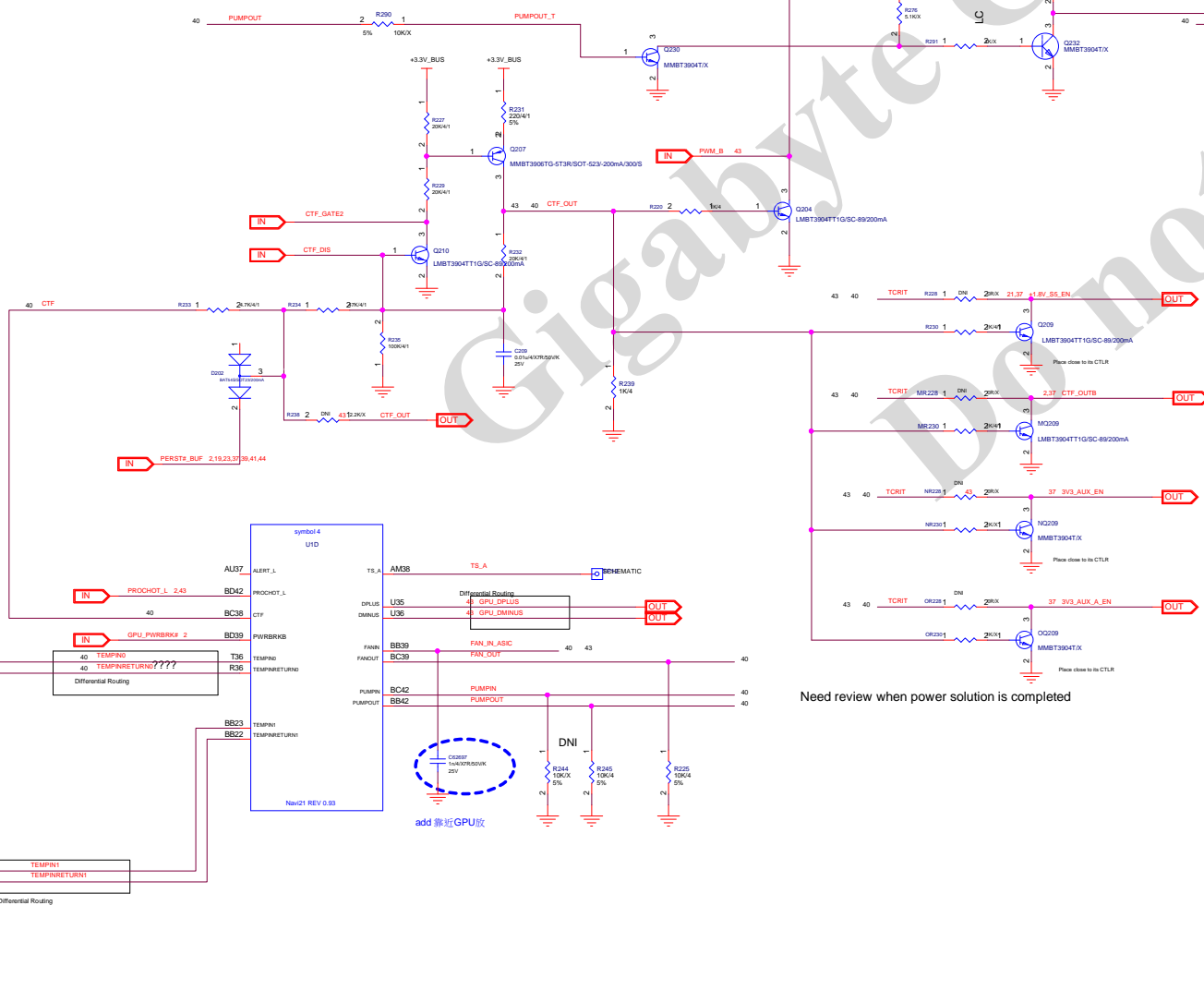
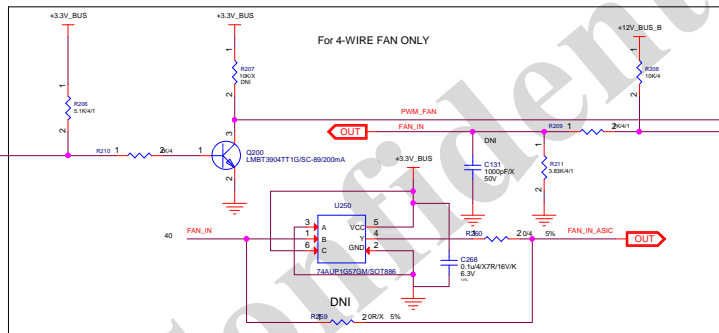
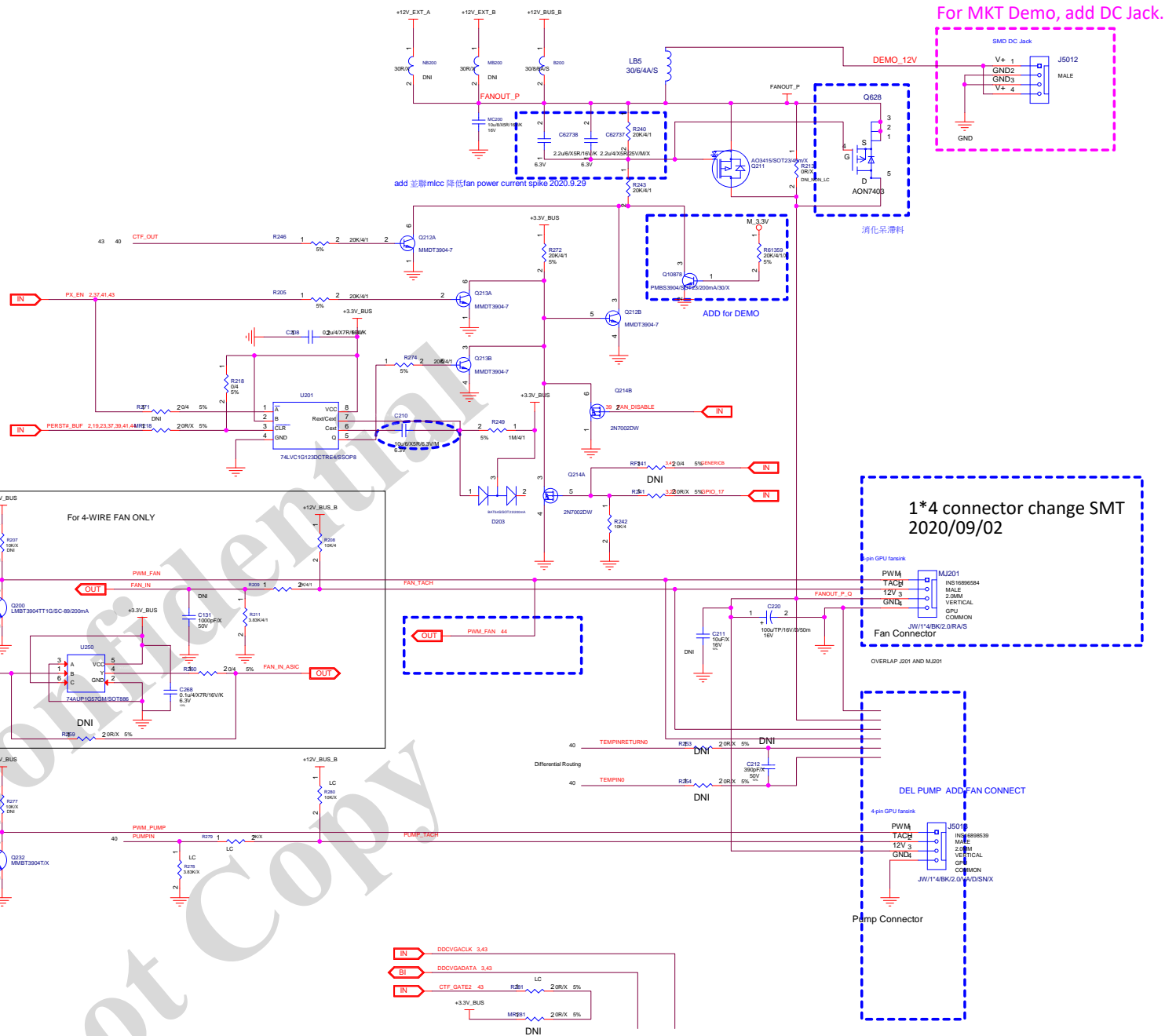
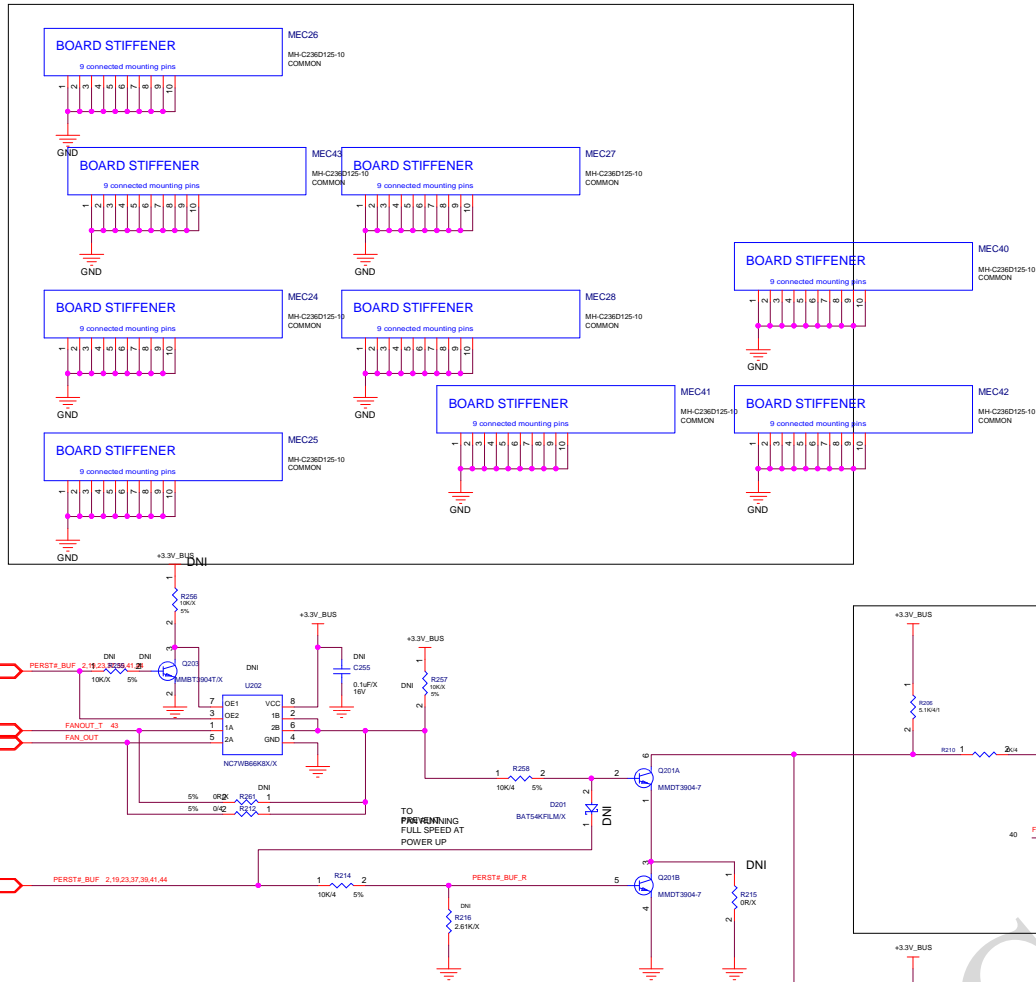


Power Rail at ASIC	Used logic	ON/OFF Status
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	ON
VDDIO_PCIE	PCIe PHY	ON
VDDAN_C	PHY	ON
VDDAN_18	PLL, PHY, etc	ON
VDDIO_18	1.8V GPIO, I2C, etc	ON
VDDIO_33	3.3V GPIO	ON
VDDAN_* EFUSE	EFUSE	ON
VDDCR_S5*	USB	ON

Power Rail at ASIC	Used logic	ON/OFF Status for BOMACO-A
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IP	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	OFF
VDDIO_PCIE	PCIe PHY	OFF
VDDAN_C	PHY	OFF
VDDAN_18	PLL, PHY, etc	OFF
VDDIO_18	1.8V GPIO, I2C, etc	OFF
VDDIO_33	3.3V GPIO	OFF
VDDAN * EFUSE	EFUSE	OFF
VDDCR_S5	USB	ON

Signals [Ⓢ]	Default [Ⓢ]	BOCO [Ⓢ]	BOMACO [Ⓢ]
PX EN [Ⓢ]	LOW [Ⓢ]	N/A [Ⓢ]	N/A [Ⓢ]
MACO EN [Ⓢ]	N/A [Ⓢ]	N/A [Ⓢ]	N/A [Ⓢ]
PERSTb [Ⓢ]	HIGH [Ⓢ]	1>0>1 [Ⓢ]	1>0>1 [Ⓢ]
PWR EN [Ⓢ]	HIGH [Ⓢ]	LOW [Ⓢ]	LOW [Ⓢ]
BOMACO EN [Ⓢ]	LOW [Ⓢ]	LOW [Ⓢ]	HIGH [Ⓢ]

BOMACO EN	SVC PU/PD	SVD PU/PD
HIGH	PU	PU
LOW	bootVID	bootVID

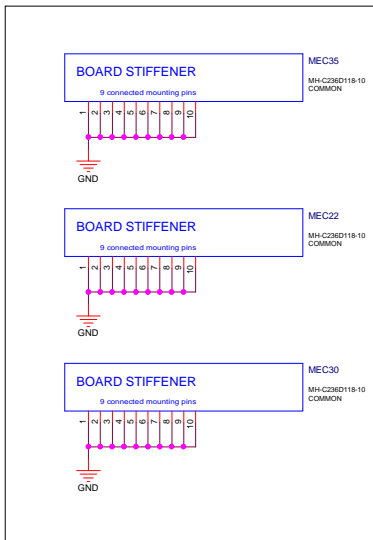


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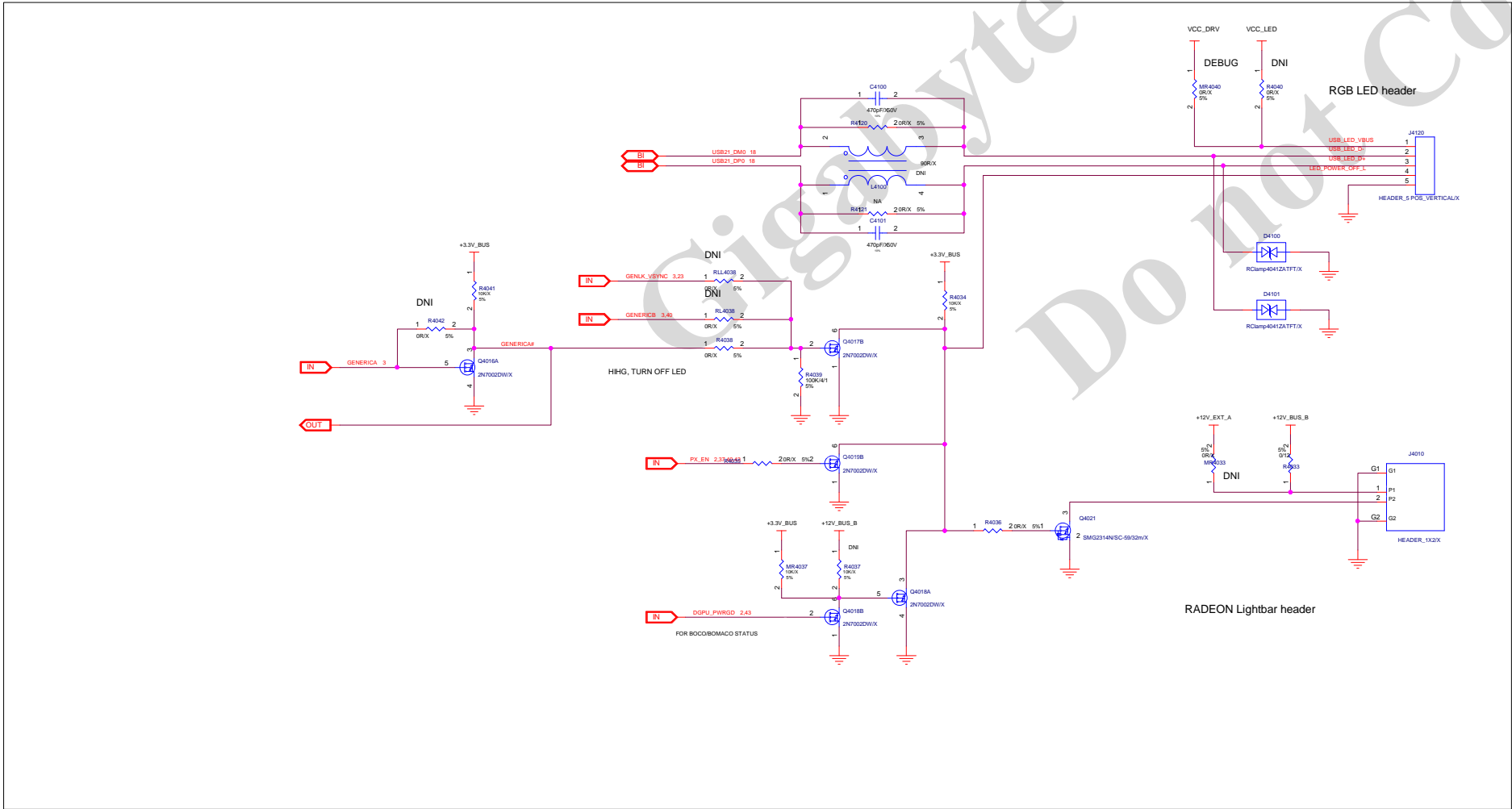
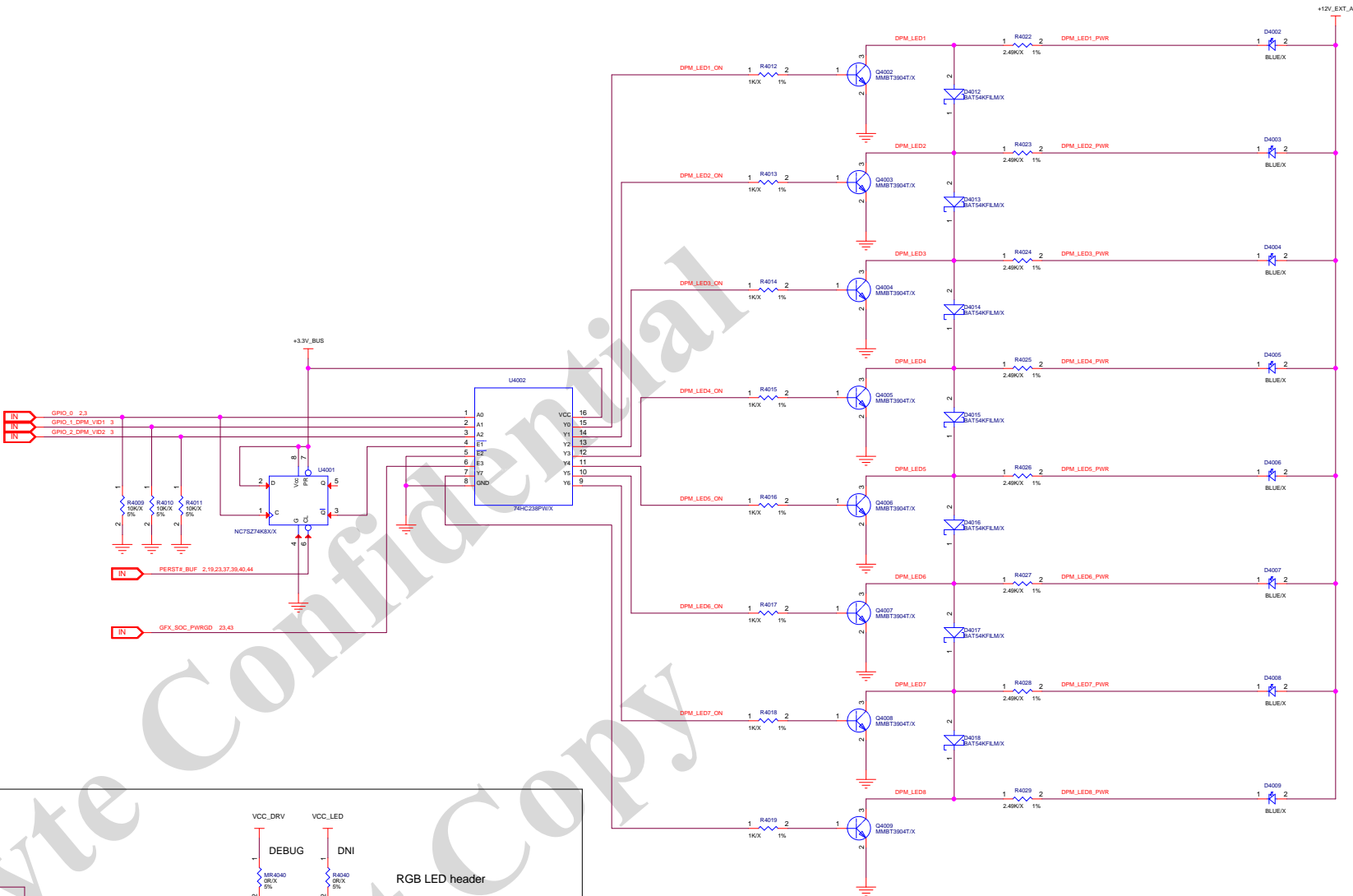
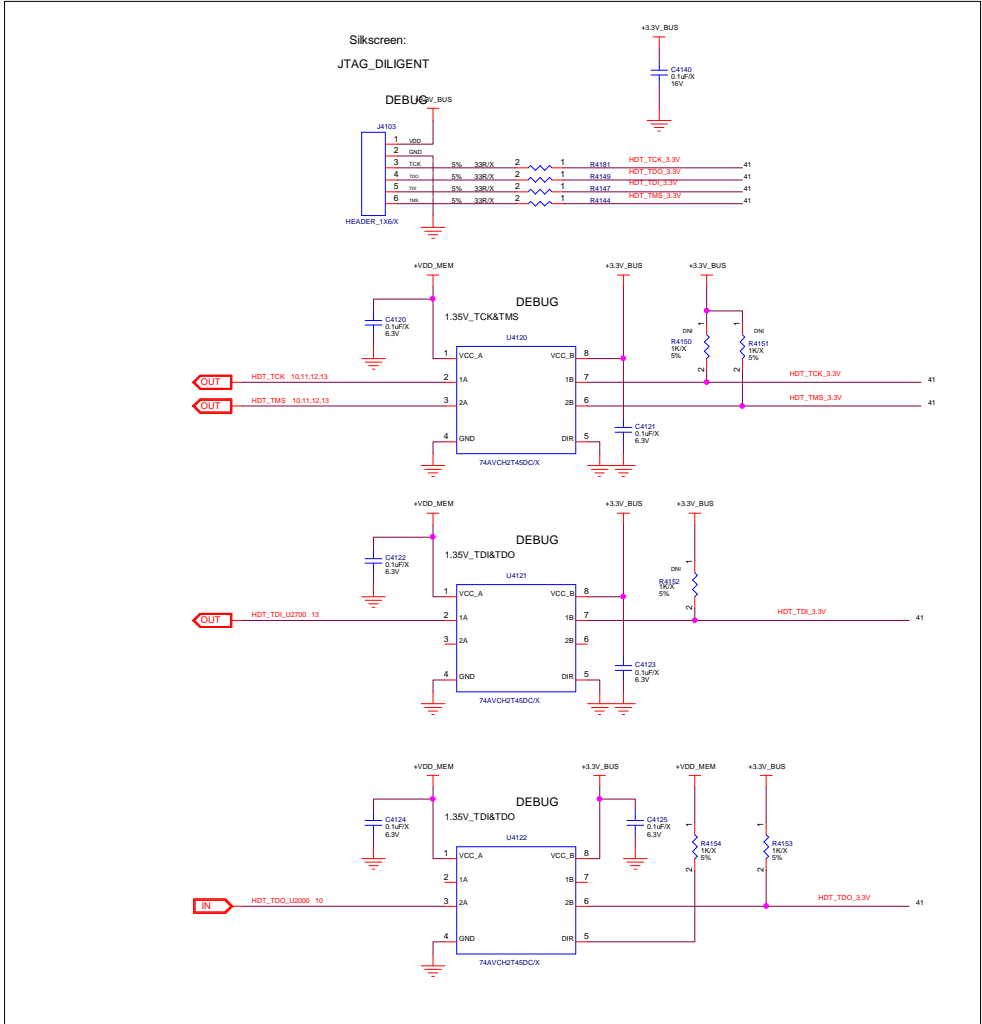
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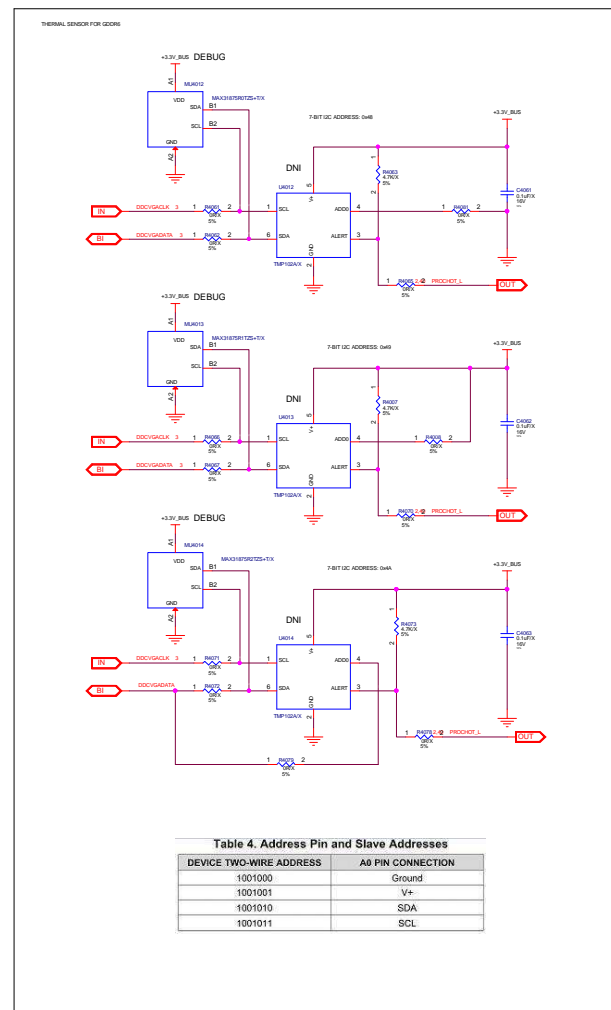
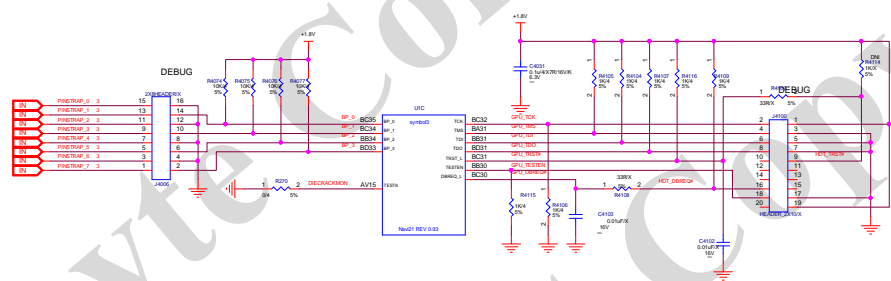
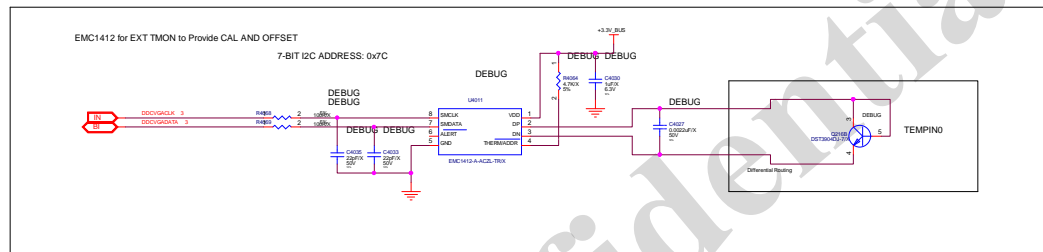
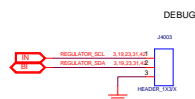
MOS SINK

MOS SINK

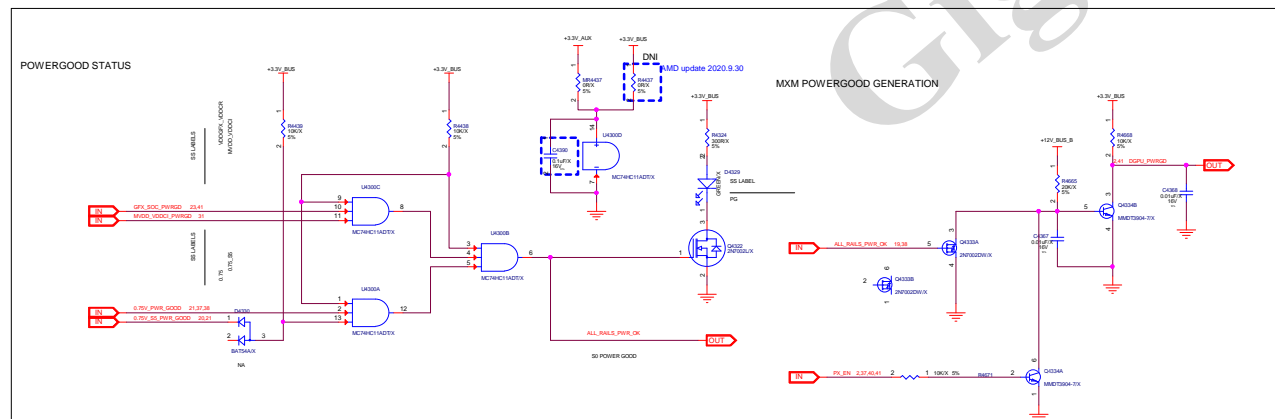
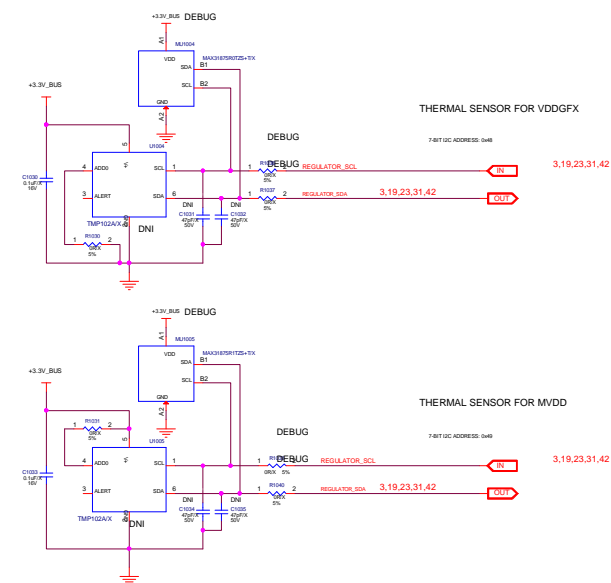


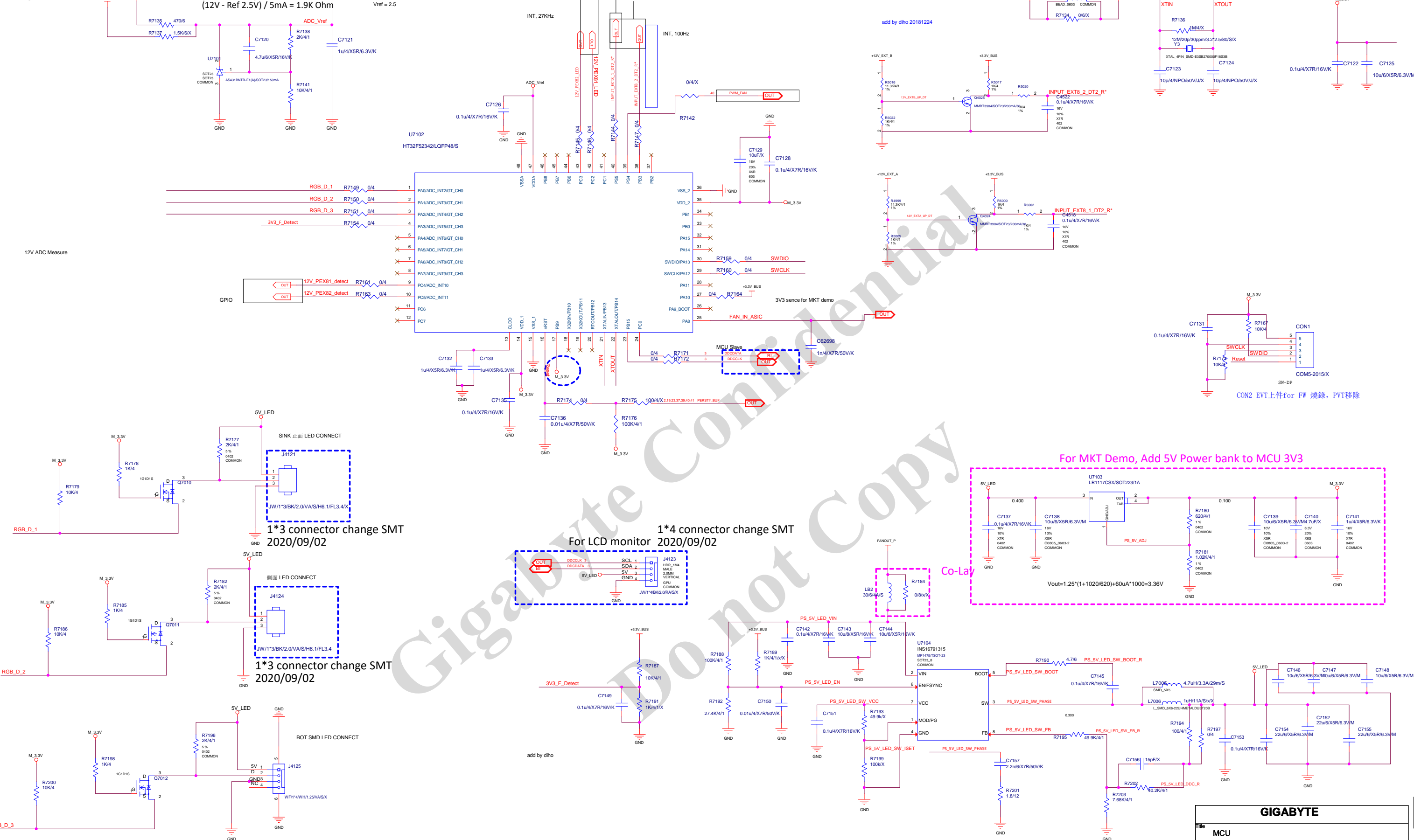
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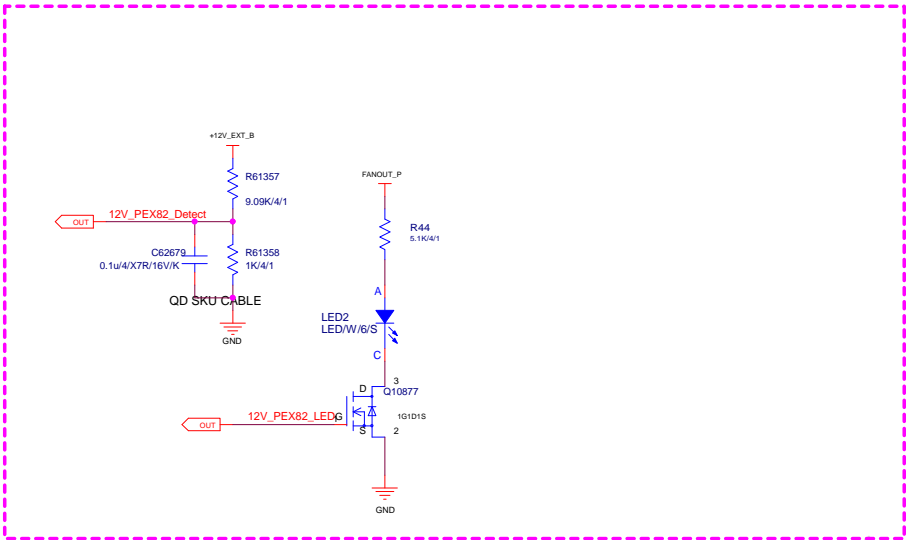
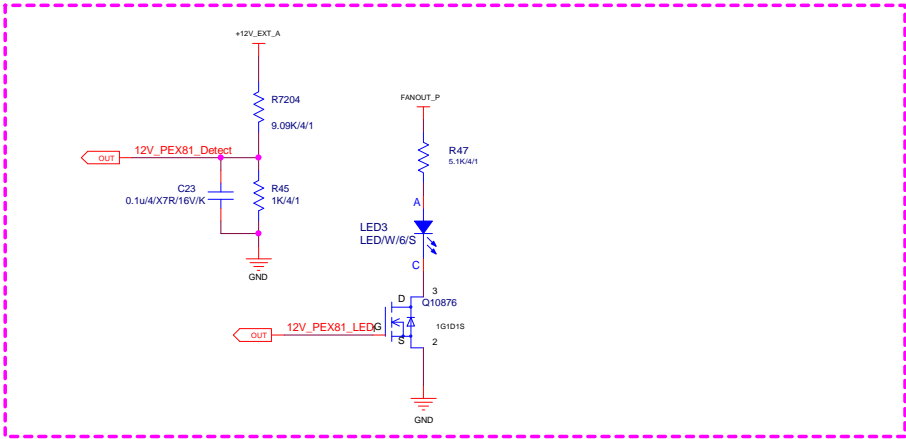




DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL







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0	A	07/23/2019	Initial schematic creation
1	-00B	Nov 11 2019	Added MODS circuit
1	-00C	Jan 21 2020	Connected +1.8V_S5 to OSC_VDD18 Gated +VBUS_PWR_USBC0 by +1.8V_USBC0 Power protection circuits

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