

G94-P545-A01 - GDDR3, DVI/VGA + DVI/VGA + HDTV/SDTV-Out

REV	VARIANT	NVPIN	ASSEMBLY
B	BASE	600-10545-xxxx-100	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0100	600-10545-9100-100	G94-400 650MHz/1000MHz 512MB 18MA32 BGAT136 GDDR3, DVI+DL+DVI+DL+HDTV-Out (Bring Up SKU)
2	SKU000	600-10545-0000-100	G94-400 650MHz/1000MHz 512MB 18MA32 BGAT136 GDDR3, DVI+DL+DVI+DL+HDTV-Out
3	SKU0010	600-10545-0010-100	G94-300 600MHz/800MHz 512MB 18MA32 BGAT136 GDDR3, DVI+DL+DVI+DL+HDTV-Out
4	SKU0020	600-10545-0020-100	G94-200 500MHz/600MHz 384MB 18MA32 BGAT136 GDDR3, DVI+DL+DVI+DL+HDTV-Out
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V127-0A Base on P545


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2.PAGE21: ADD GPIO circuit
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4.PAGE 27: remove PEX_VDD power switch circuit
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9.PAGE 16/17 : ADD EMI bridge R
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11.PAGE 15 remove J2_D_SUB SLIM CONNECT
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V127-20 Base on V127-0A

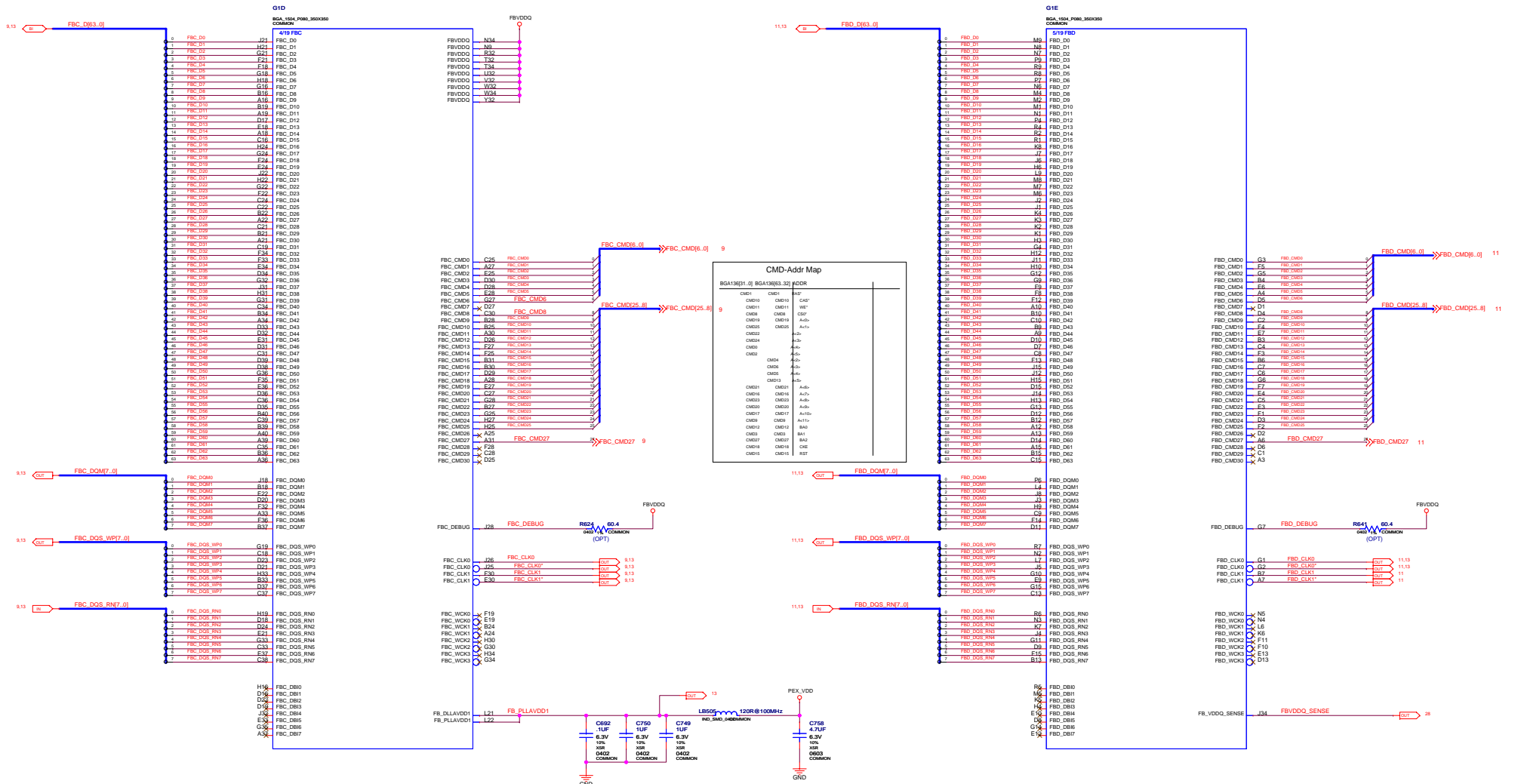
- 1.PAGE30 .CO-LAYOUT RT9258 circuit

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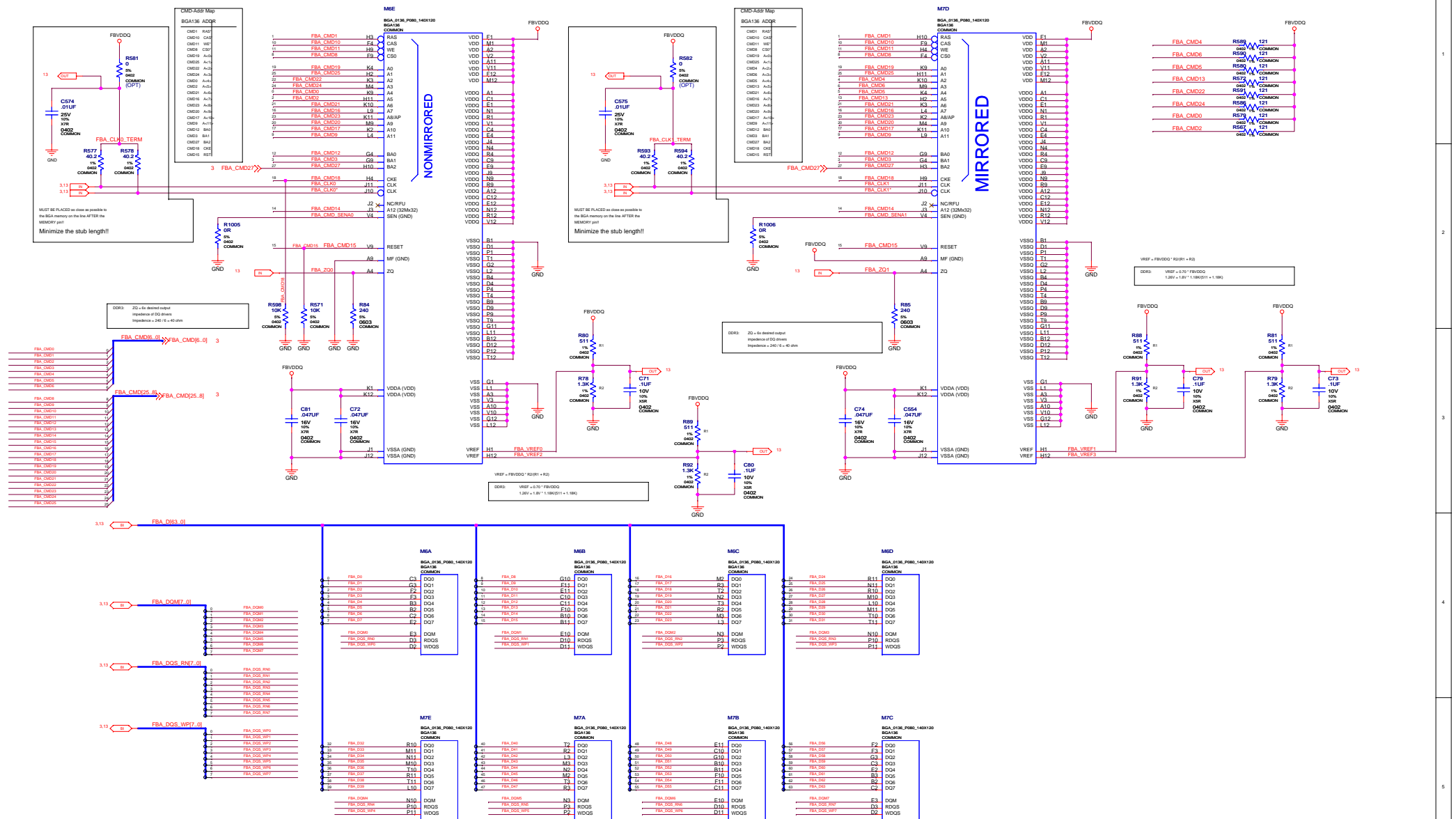
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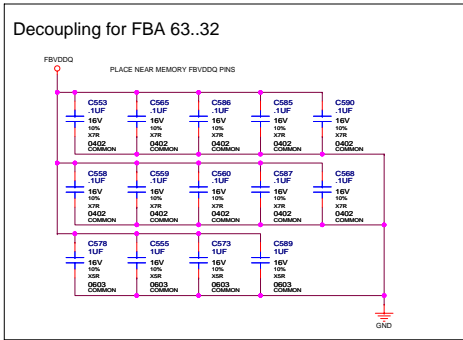
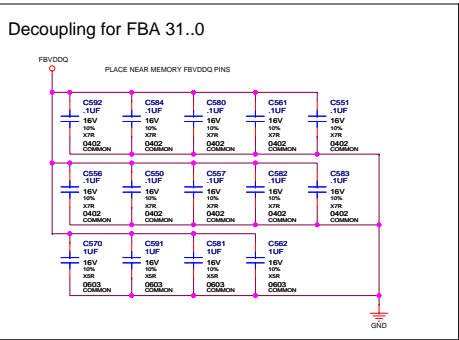


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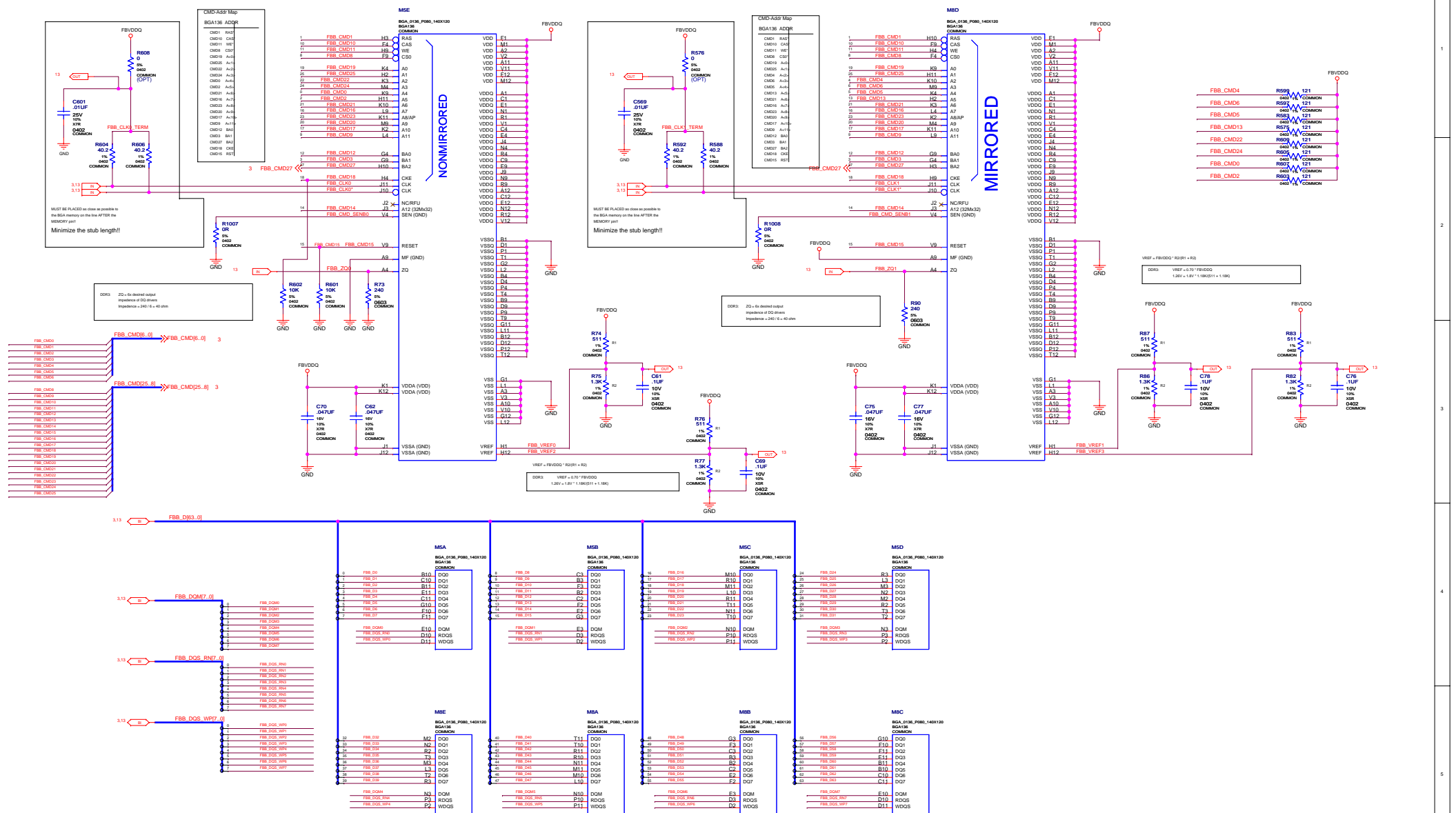
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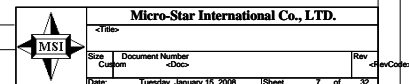
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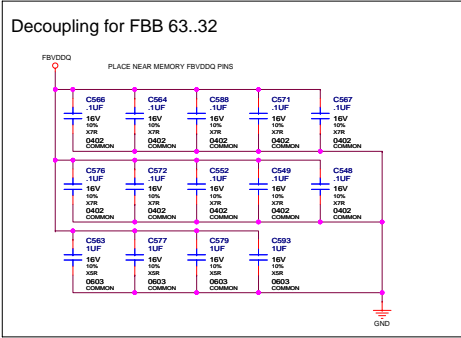
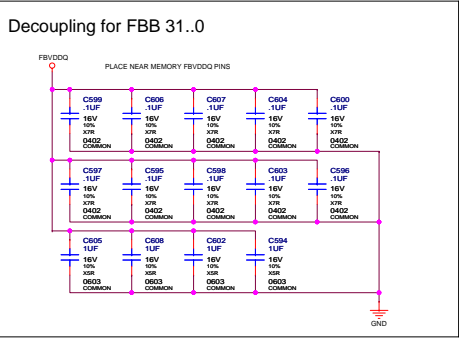
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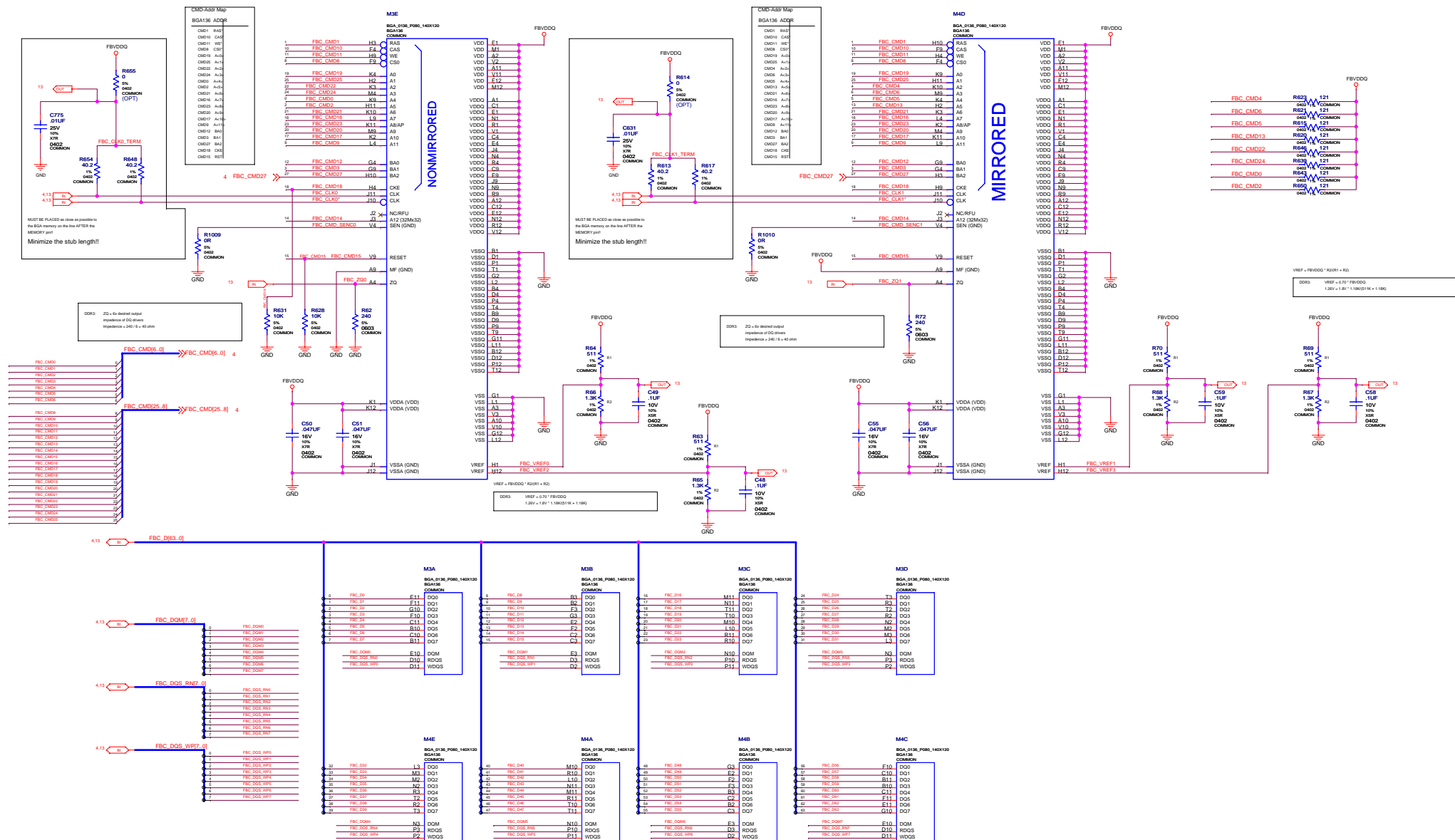
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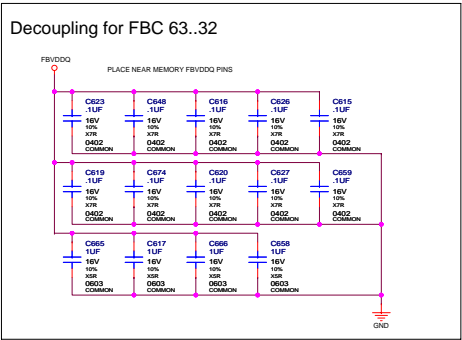
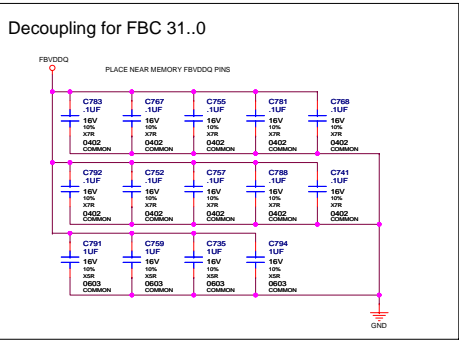
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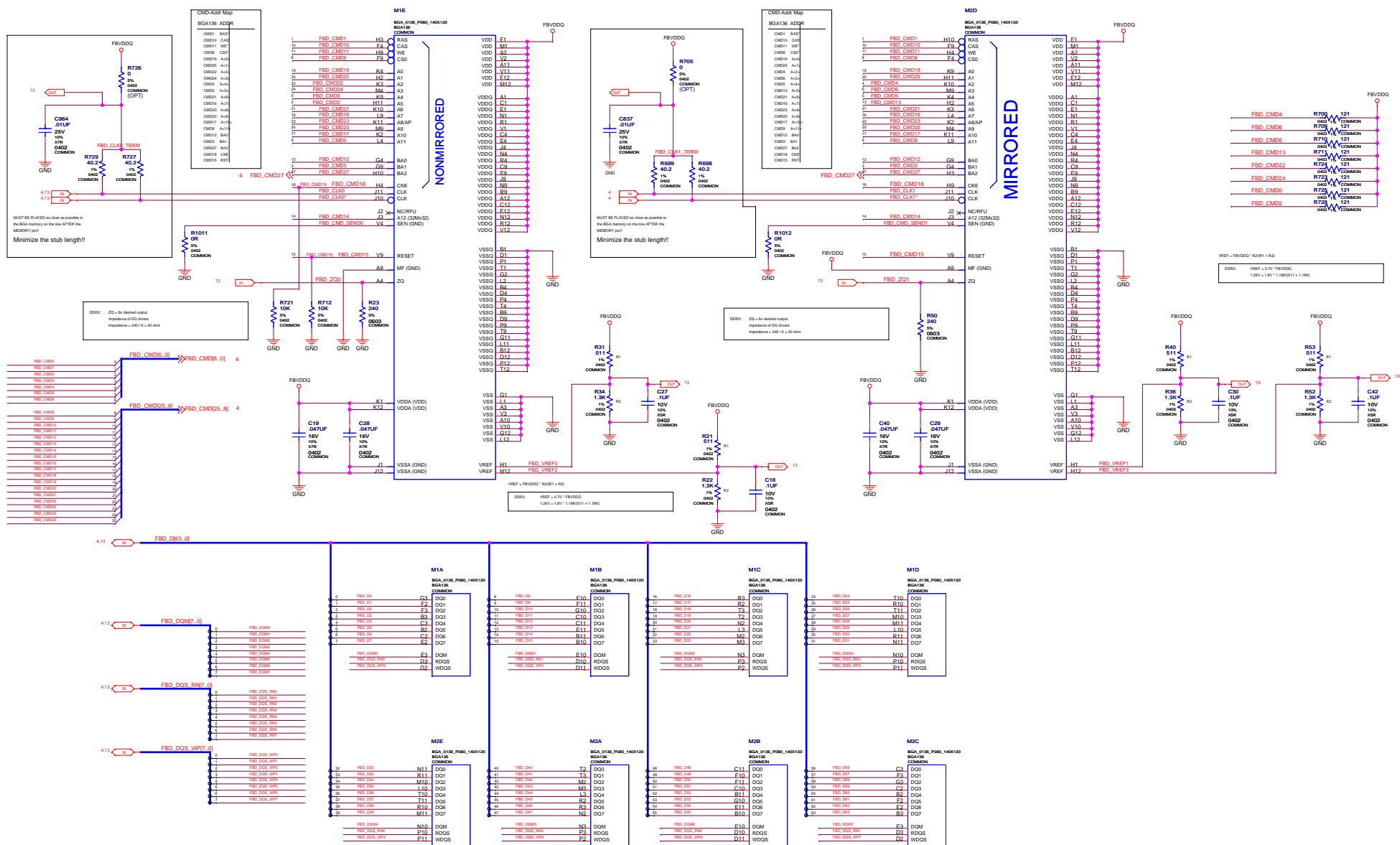
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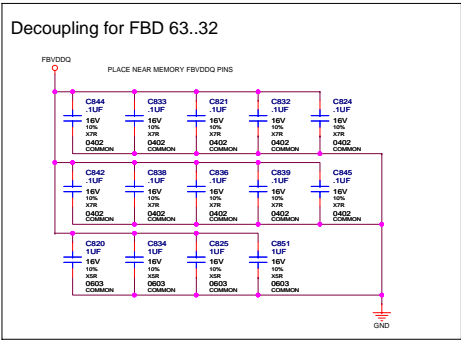
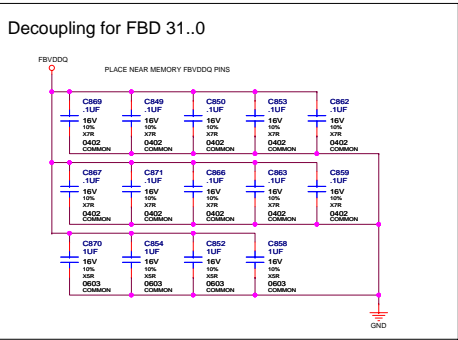


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FBD Partition Decoupling



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NET RULES for FBA and FBB

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
3.5	FBA_CLK0	1	RIGHT FBA_CLK0
3.5	FBB_CLK0P	1	RIGHT FBA_CLK0
3.5	FBA_CLK0_TERM	1	RIGHT FBA_CLK0
3.5	FBB_CLK1	1	RIGHT FBA_CLK1
3.5	FBB_CLK1P	1	RIGHT FBA_CLK1
3.5	FBB_CLK1_TERM	1	RIGHT FBA_CLK1

NET	NV_CRITICAL_NET	IMPEDANCE
3.5	FBA_DQS_WRT0_0	1
3.5	FBB_DQS_WRT0_0	1
3.5	FBA_DQS_WRT0_1	1
3.5	FBB_DQS_WRT0_1	1
3.5	FBA_DQS_WRT0_2	1
3.5	FBB_DQS_WRT0_2	1

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
3.7	FBA_CLK0	1	RIGHT FBA_CLK0
3.7	FBB_CLK0P	1	RIGHT FBA_CLK0
3.7	FBA_CLK0_TERM	1	RIGHT FBA_CLK0
3.7	FBB_CLK1	1	RIGHT FBA_CLK1
3.7	FBB_CLK1P	1	RIGHT FBA_CLK1
3.7	FBB_CLK1_TERM	1	RIGHT FBA_CLK1

NET	NV_CRITICAL_NET	IMPEDANCE
3.7	FBA_DQS_WRT0_0	1
3.7	FBB_DQS_WRT0_0	1
3.7	FBA_DQS_WRT0_1	1
3.7	FBB_DQS_WRT0_1	1
3.7	FBA_DQS_WRT0_2	1
3.7	FBB_DQS_WRT0_2	1

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
3	FBA_PLAVDD0	1.1V	0.05A
3	FBA_VREF	1.20V	0.05A
5	FBA_VREF0	1.20V	0.05A
5	FBB_VREF0P	1.20V	0.05A
5	FBA_VREF2	1.20V	0.05A
5	FBB_VREF2P	1.20V	0.05A
5	FBA_VREF3	1.20V	0.05A
5	FBB_VREF3P	1.20V	0.05A
5	FBA_VDD	1.20V	0.05A
5	FBB_VDD	1.20V	0.05A
7	FBA_VREF0	1.20V	0.05A
7	FBB_VREF0P	1.20V	0.05A
7	FBA_VREF2	1.20V	0.05A
7	FBB_VREF2P	1.20V	0.05A
7	FBA_VREF3	1.20V	0.05A
7	FBB_VREF3P	1.20V	0.05A
7	FBA_VDD	1.20V	0.05A
7	FBB_VDD	1.20V	0.05A

NET RULES for FBC and FBD

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
4.9	FBC_CLK0	1	RIGHT FBC_CLK0
4.9	FBD_CLK0P	1	RIGHT FBC_CLK0
4.9	FBC_CLK0_TERM	1	RIGHT FBC_CLK0
4.9	FBD_CLK1	1	RIGHT FBC_CLK1
4.9	FBD_CLK1P	1	RIGHT FBC_CLK1
4.9	FBD_CLK1_TERM	1	RIGHT FBC_CLK1

NET	NV_CRITICAL_NET	IMPEDANCE
4.9	FBC_DQS_WRT0_0	1
4.9	FBD_DQS_WRT0_0	1
4.9	FBC_DQS_WRT0_1	1
4.9	FBD_DQS_WRT0_1	1
4.9	FBC_DQS_WRT0_2	1
4.9	FBD_DQS_WRT0_2	1

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
4.11	FBC_CLK0	1	RIGHT FBC_CLK0
4.11	FBD_CLK0P	1	RIGHT FBC_CLK0
4.11	FBC_CLK0_TERM	1	RIGHT FBC_CLK0
3.7	FBC_CLK1	1	RIGHT FBC_CLK1
3.7	FBD_CLK1P	1	RIGHT FBC_CLK1
3.7	FBD_CLK1_TERM	1	RIGHT FBC_CLK1

NET	NV_CRITICAL_NET	IMPEDANCE
4.11	FBC_DQS_WRT0_0	1
4.11	FBD_DQS_WRT0_0	1
4.11	FBC_DQS_WRT0_1	1
4.11	FBD_DQS_WRT0_1	1
4.11	FBC_DQS_WRT0_2	1
4.11	FBD_DQS_WRT0_2	1

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
4	FBA_PLAVDD0	1.1V	0.05A
9	FBC_VREF0	1.20V	0.05A
9	FBD_VREF0P	1.20V	0.05A
9	FBC_VREF2	1.20V	0.05A
9	FBD_VREF2P	1.20V	0.05A
9	FBC_VREF3	1.20V	0.05A
9	FBD_VREF3P	1.20V	0.05A
9	FBC_VDD	1.20V	0.05A
9	FBD_VDD	1.20V	0.05A
11	FBC_VREF0	1.20V	0.05A
11	FBD_VREF0P	1.20V	0.05A
11	FBC_VREF2	1.20V	0.05A
11	FBD_VREF2P	1.20V	0.05A
11	FBC_VREF3	1.20V	0.05A
11	FBD_VREF3P	1.20V	0.05A
11	FBC_VDD	1.20V	0.05A
11	FBD_VDD	1.20V	0.05A

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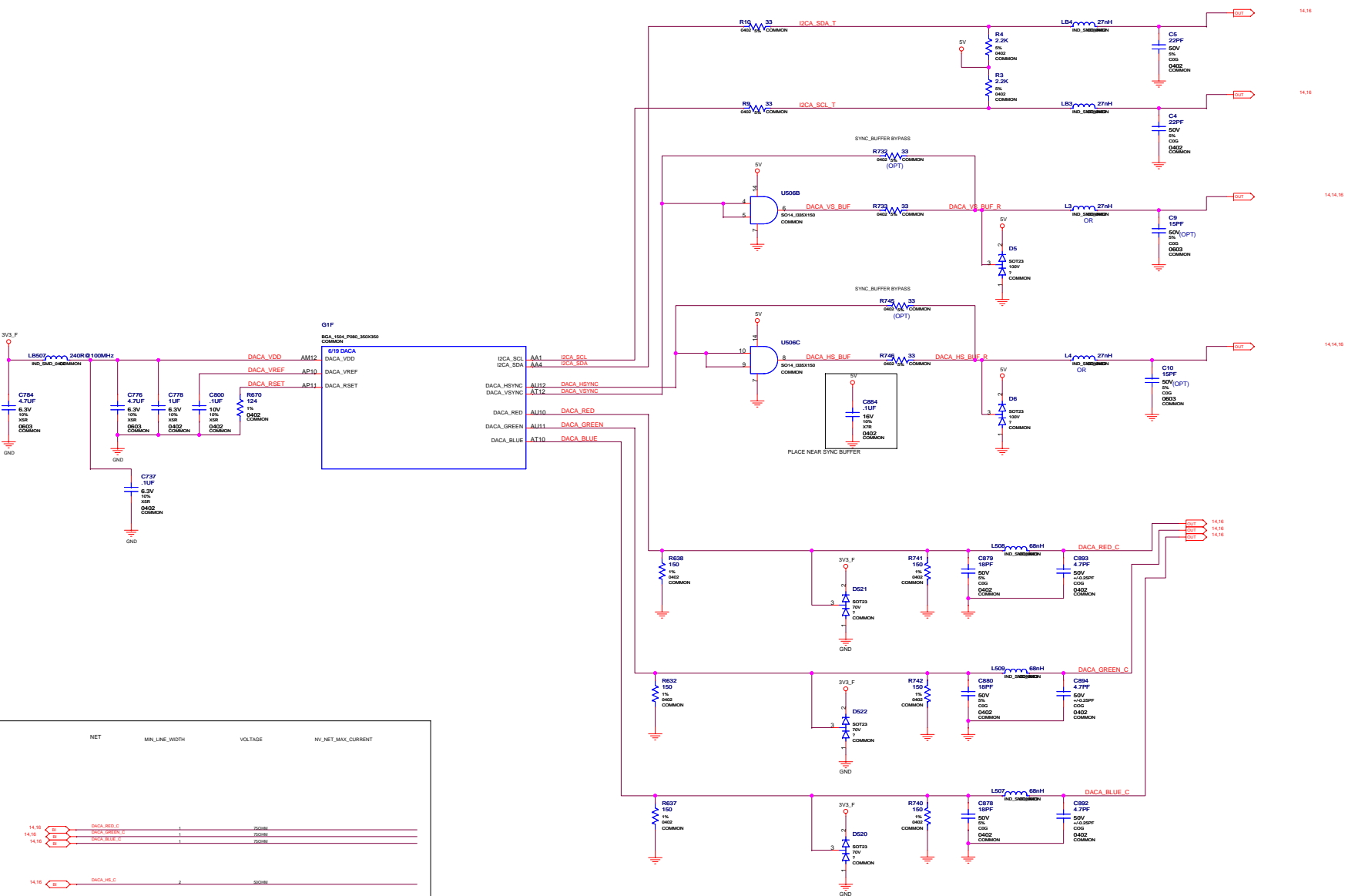


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DACA RGB-FILTER



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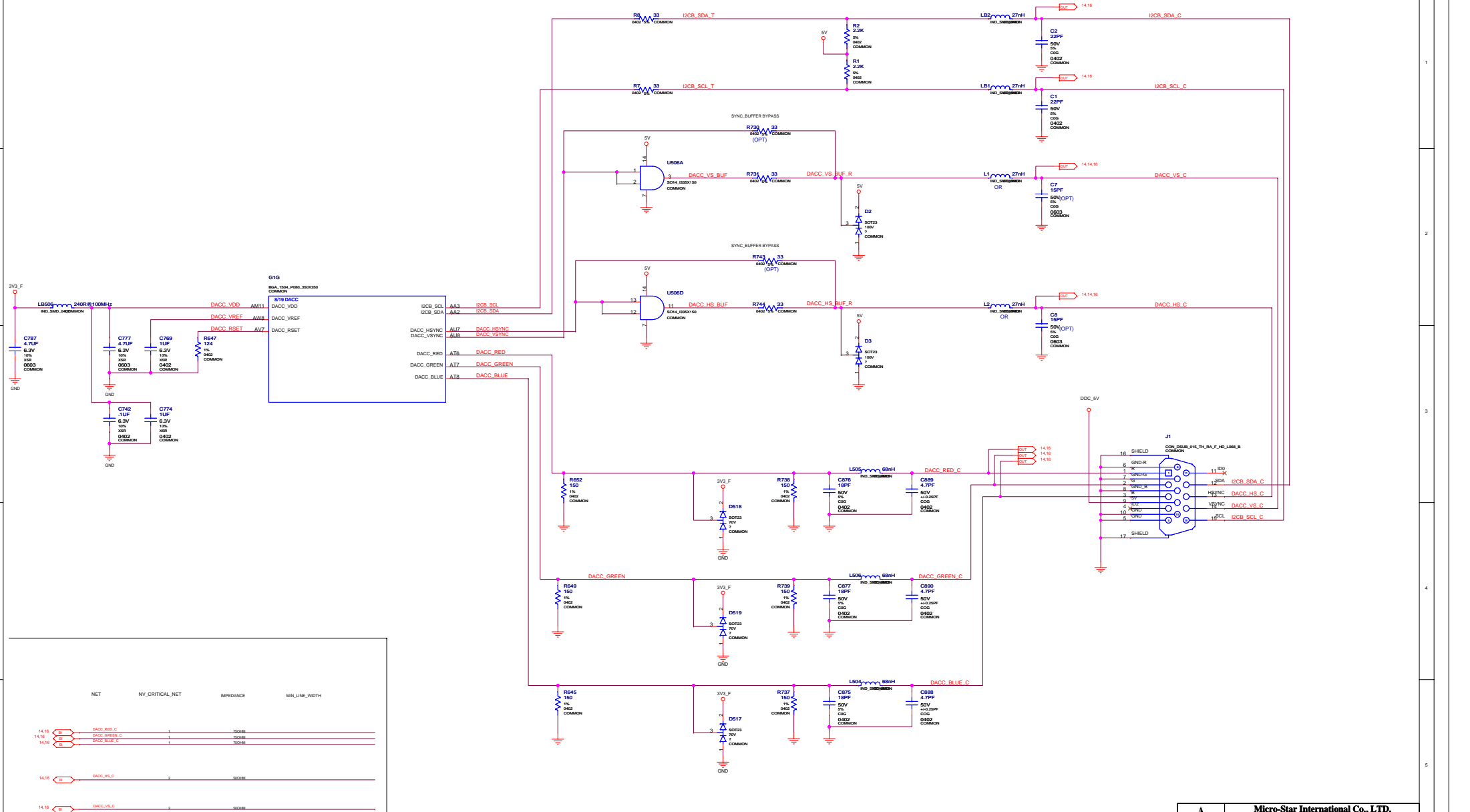


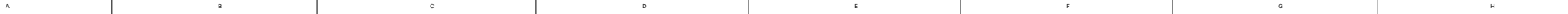
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DACC RGB-FILTER





DVIAB Hotplug Detection

The schematic diagram illustrates the hotplug detection circuit for DVIAB. The signal line GP100_DVI_A_HPD is connected to a 10K resistor R12, which is connected to a 3V3_F supply. The signal line also passes through a 1K resistor R9 and a 180R inductor L18 before reaching a DVI connector. The DVI connector has pins for HPD, SENSE, and GND. The HPD pin is connected to the 3V3_F supply through a 10K resistor R9. The SENSE pin is connected to the 3V3_F supply through a 180R inductor L18. The GND pin is connected to GND. The DVI connector also has pins for D0, D1, D2, and D3, which are connected to GND through 500PF capacitors C8, C9, C10, and C11 respectively.

ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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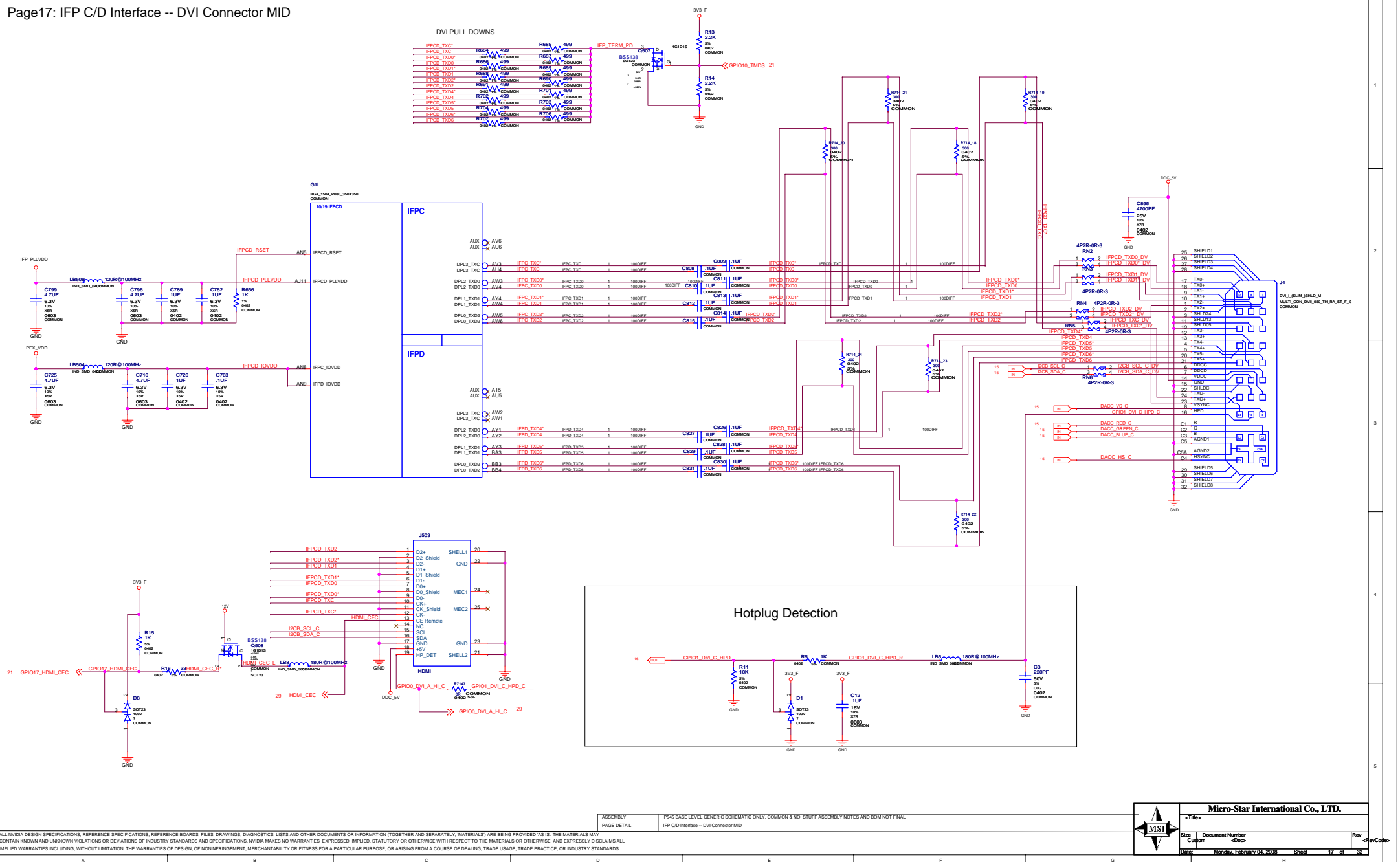
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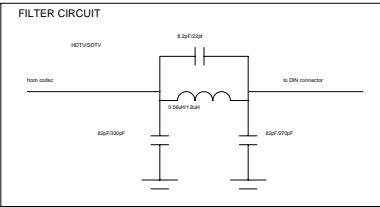
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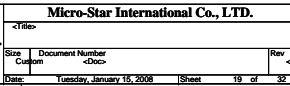
Date: Tuesday, January 15, 2008 Sheet 16 of 32

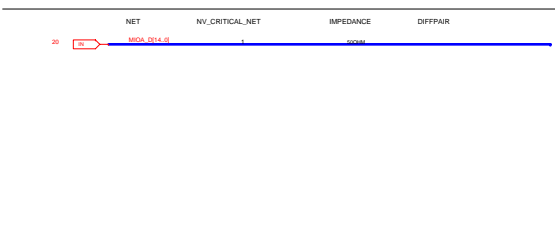
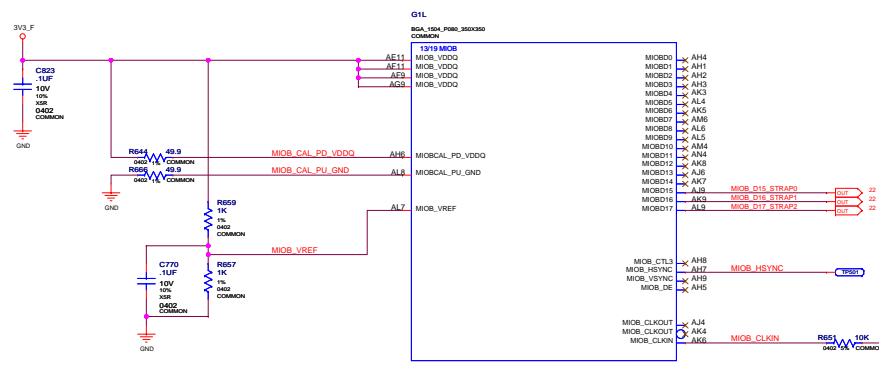
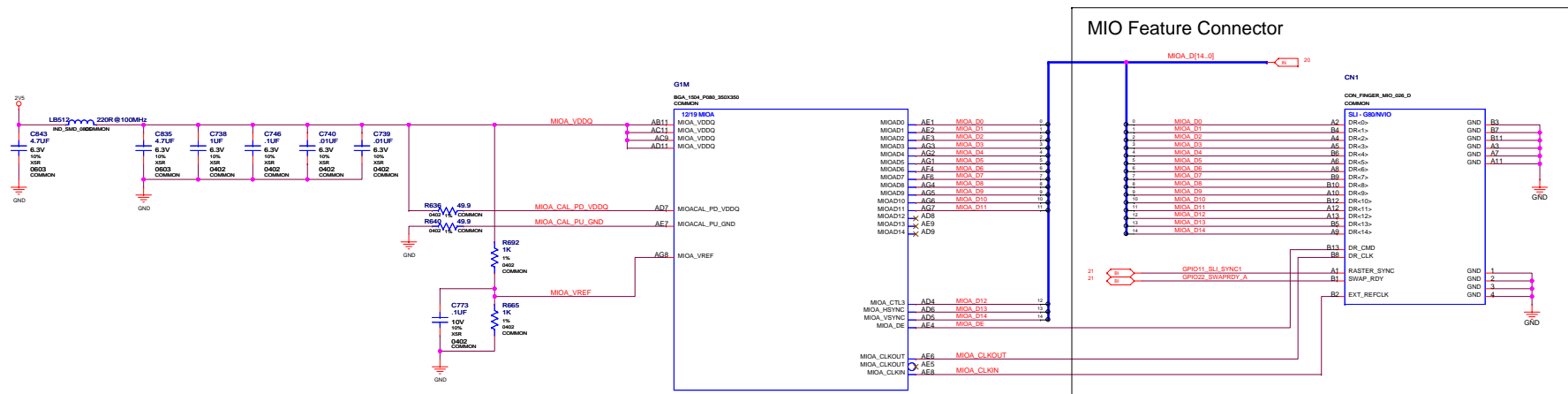
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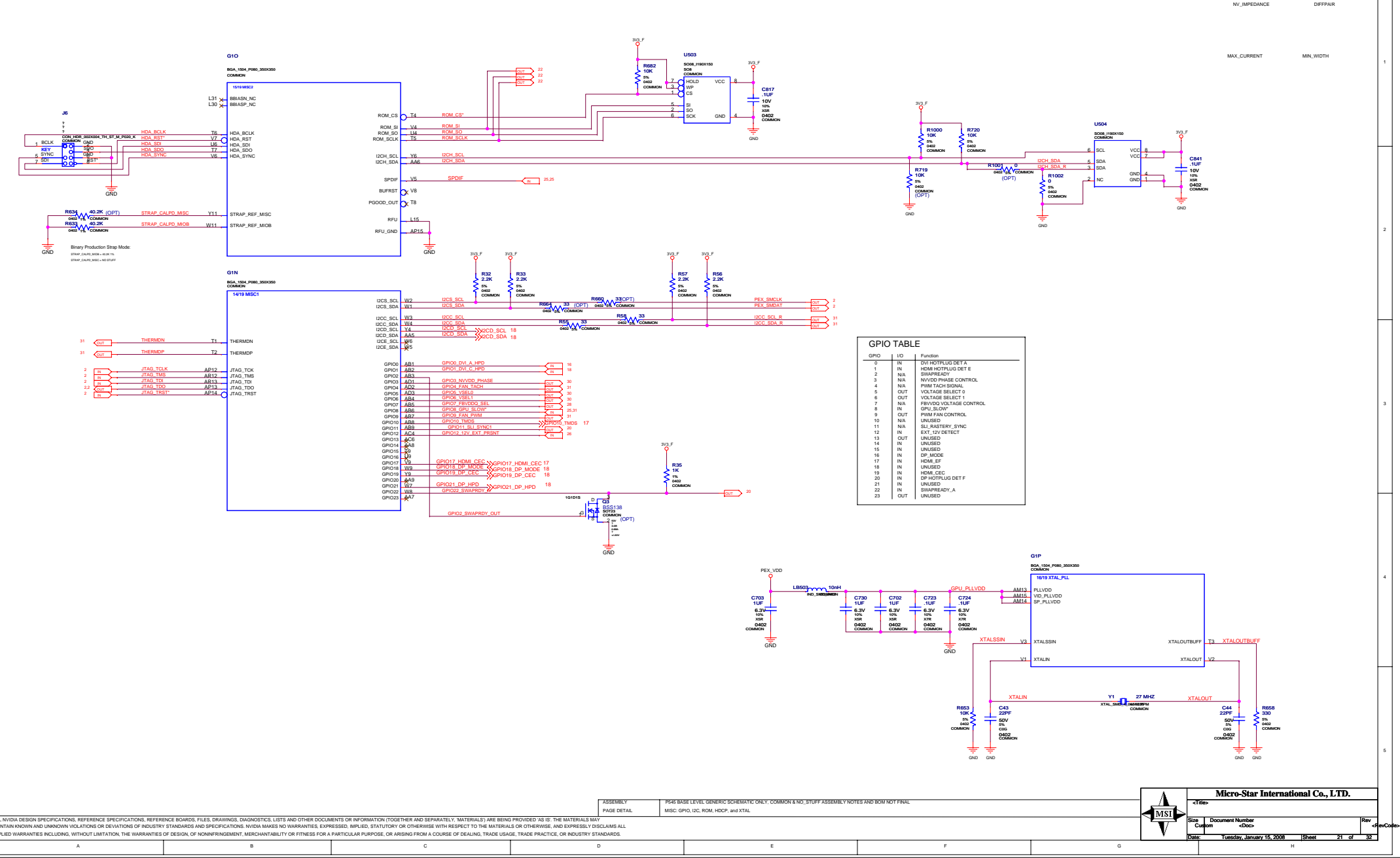


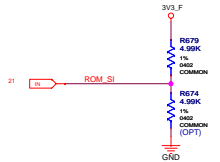


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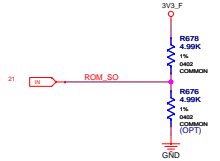




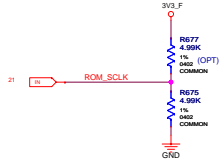


STRAP PIN	STRAP NAME	
ROM_SI	PCI_DEVID_EXT	

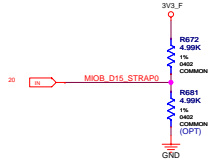
3V3	GND
5K	1 0



STRAP PIN	STRAP NAME	
ROM_SO	SLOT_CLK_CFG	



STRAP PIN	STRAP NAME	
ROM_SCLK	PCI_DEVID[3]	

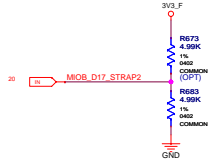
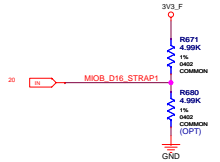


STRAP PIN	STRAP NAME	
STRAP0	RAMCFG0	
STRAP1	RAMCFG1	
STRAP2	RAMCFG2	

* RAMCFG[2:0]


256MB (8Mx32)	512MB (16Mx32)	1024MB (32Mx32)
101 --- 256-bit Qimonda	001 --- 256-bit Qimonda	101 --- 256-bit Hynix
110 --- 256-bit Hynix	010 --- 256-bit Hynix	110 --- 256-bit Hynix
111 --- 256-bit Samsung	011 --- 256-bit Samsung	111 --- 256-bit Samsung

* VBIOS will be defined on a per SKU basis.



BGA_1554_P1560_3503350	
COMMON	
AP19	NC
AC34	NC
AC35	NC
AC36	NC
AC37	NC
AF34	NC
AF35	NC
AF36	NC
AF37	NC
AG34	NC
AG35	NC
AG36	NC
AG37	NC
AM34	NC
AM35	NC
AM36	NC
AM37	NC
AP34	NC
AP35	NC
AP36	NC
AP37	NC
AT34	NC
AT35	NC
AT36	NC
AT37	NC
AU34	NC
AU35	NC
AU36	NC
AU37	NC
AV34	NC
AV35	NC
AV36	NC
AV37	NC
EW34	NC
EW35	NC
EW36	NC
EW37	NC
F34	NC
F35	NC
F36	NC
F37	NC
G34	NC
G35	NC
G36	NC
G37	NC
H34	NC
H35	NC
H36	NC
H37	NC
I34	NC
I35	NC
I36	NC
I37	NC
J34	NC
J35	NC
J36	NC
J37	NC
K34	NC
K35	NC
K36	NC
K37	NC
L34	NC
L35	NC
L36	NC
L37	NC
M34	NC
M35	NC
M36	NC
M37	NC
N34	NC
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R34	NC
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S34	NC
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S37	NC
T34	NC
T35	NC
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U34	NC
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Z37	NC

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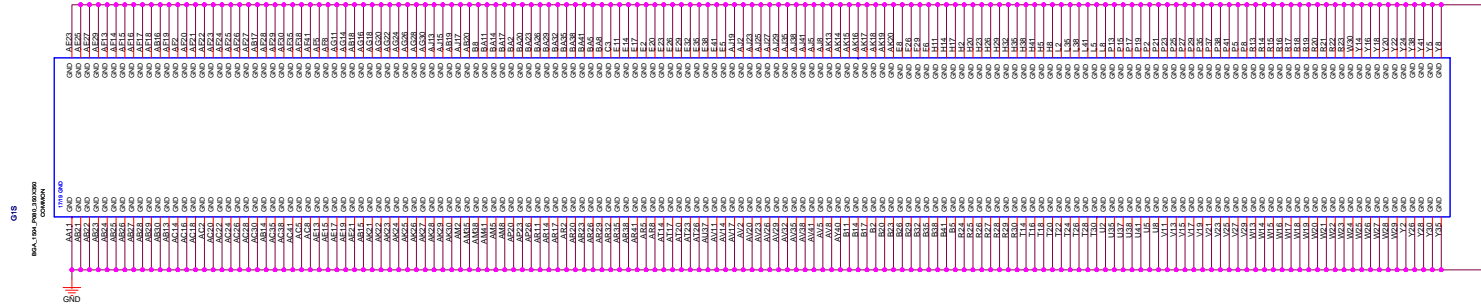
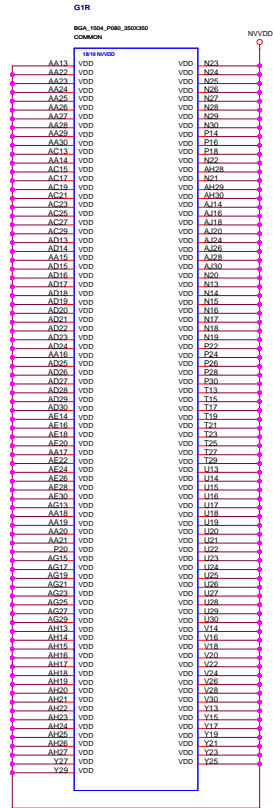
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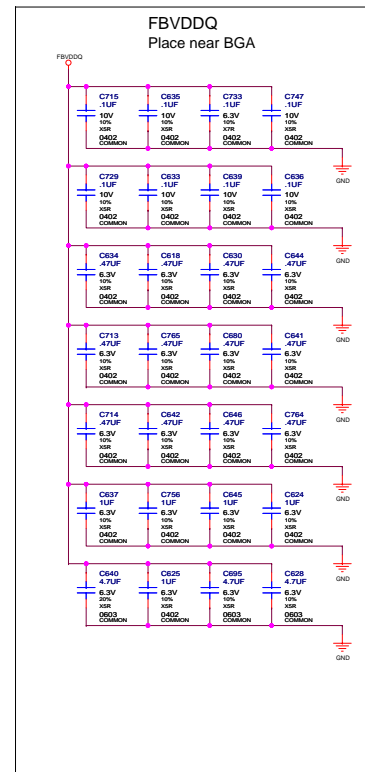
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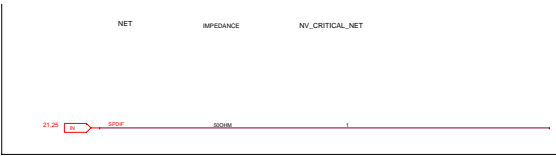
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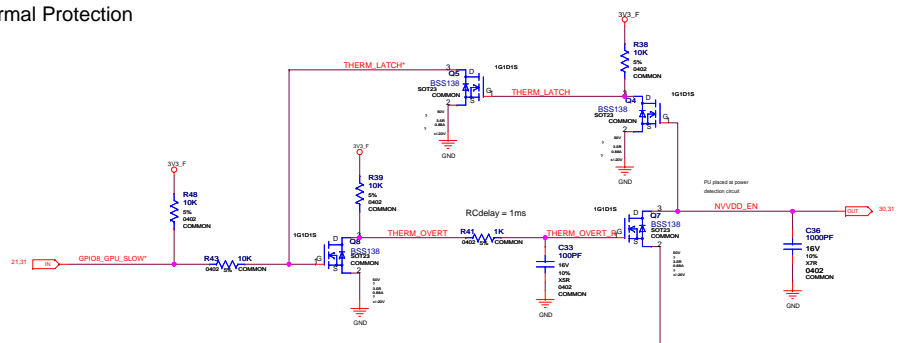
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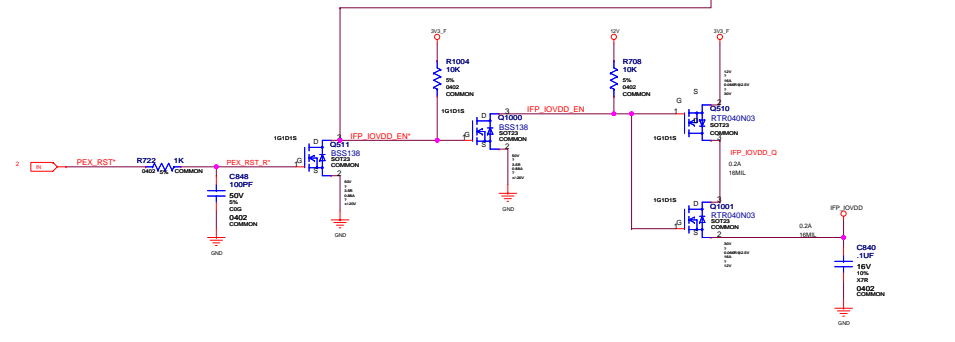


Thermal Protection

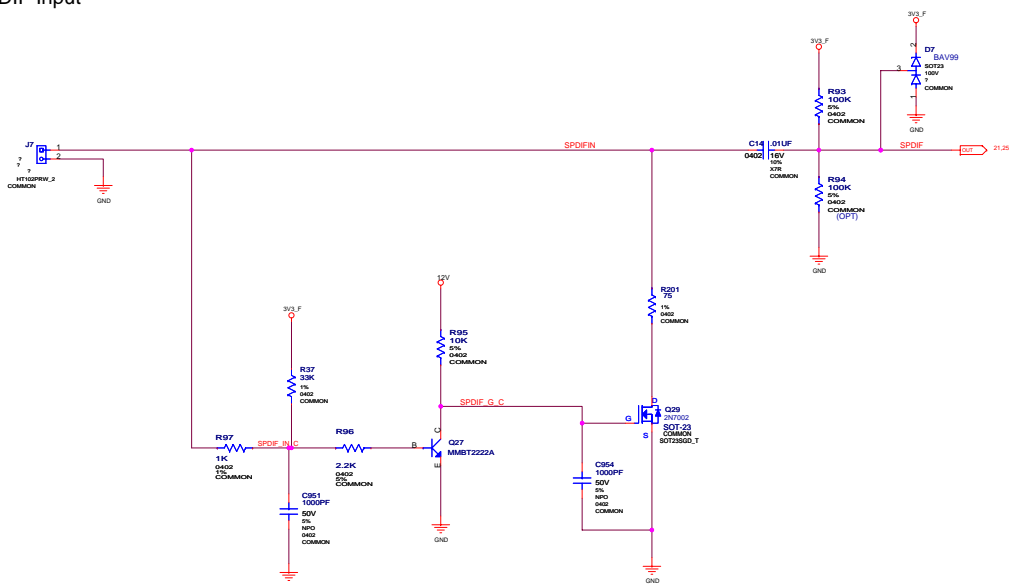


IFP_IOVDD Backdrive Prevention

Stuffing possibilities for thermal control and protection

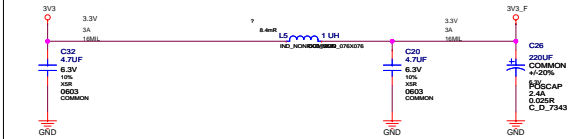


SPDIF Input



3V3 Power Supply Filter

3V3_F = 3.3V @ 2.5A



12V Power Supply Filter

12V_F = 12V @ 5.5A

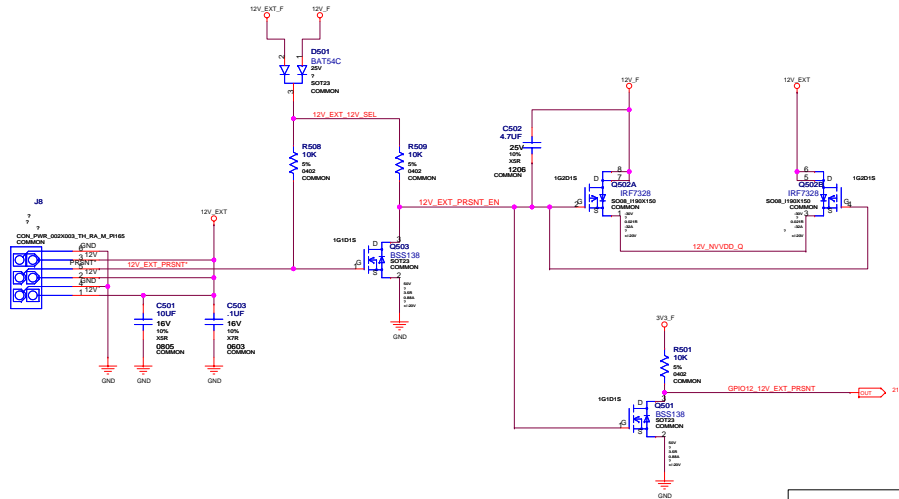


12V_EXT Power Supply Filter

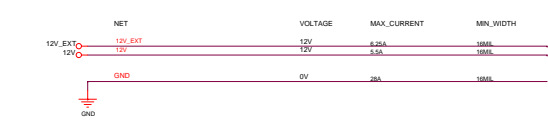
12V_EXT_F = 12V @ 6.25A



INPUT POWER SELECTION for NVVDD



GPIO12	
EMERGENCY MODE (12V_EXT present)	0
150W POWER MODE (12V_EXT NOT present)	1



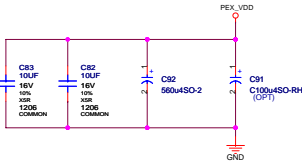
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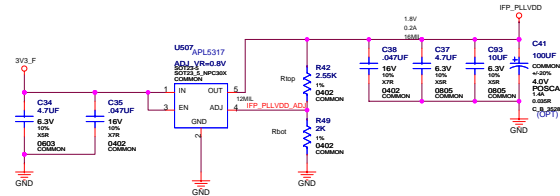
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IFP_PLLVDD Power Supply

IFP_PLLVDD = 1.8V @ 200mA

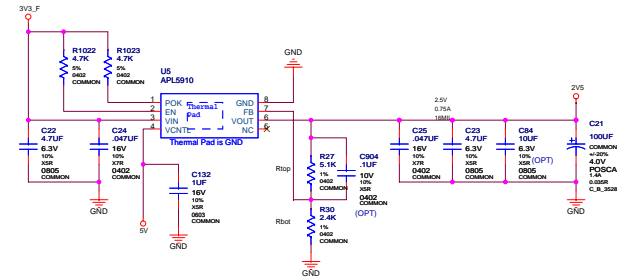
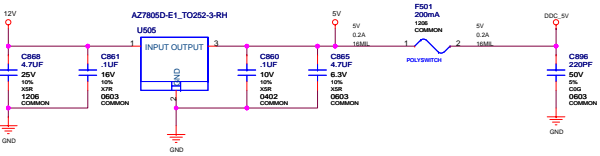


$$IFP_PLLVDD = VREF * (1 + (Rtop / Rbot))$$
$$1.82V = 0.8V * (1 + (2.5K/2K))$$

5V and DDC_5V Power Supply

DDC_5V = 5V @ 200mA

LAYOUT NOTE: ADD MIN 200MM² COPPER AROUND THIS DP4K FOR HEAT DISSIPATION



$$2V5 = VREF * (1 + (Rtop / Rbot))$$
$$2.5V = 0.8V * (1 + (5.1K/2.4K))$$

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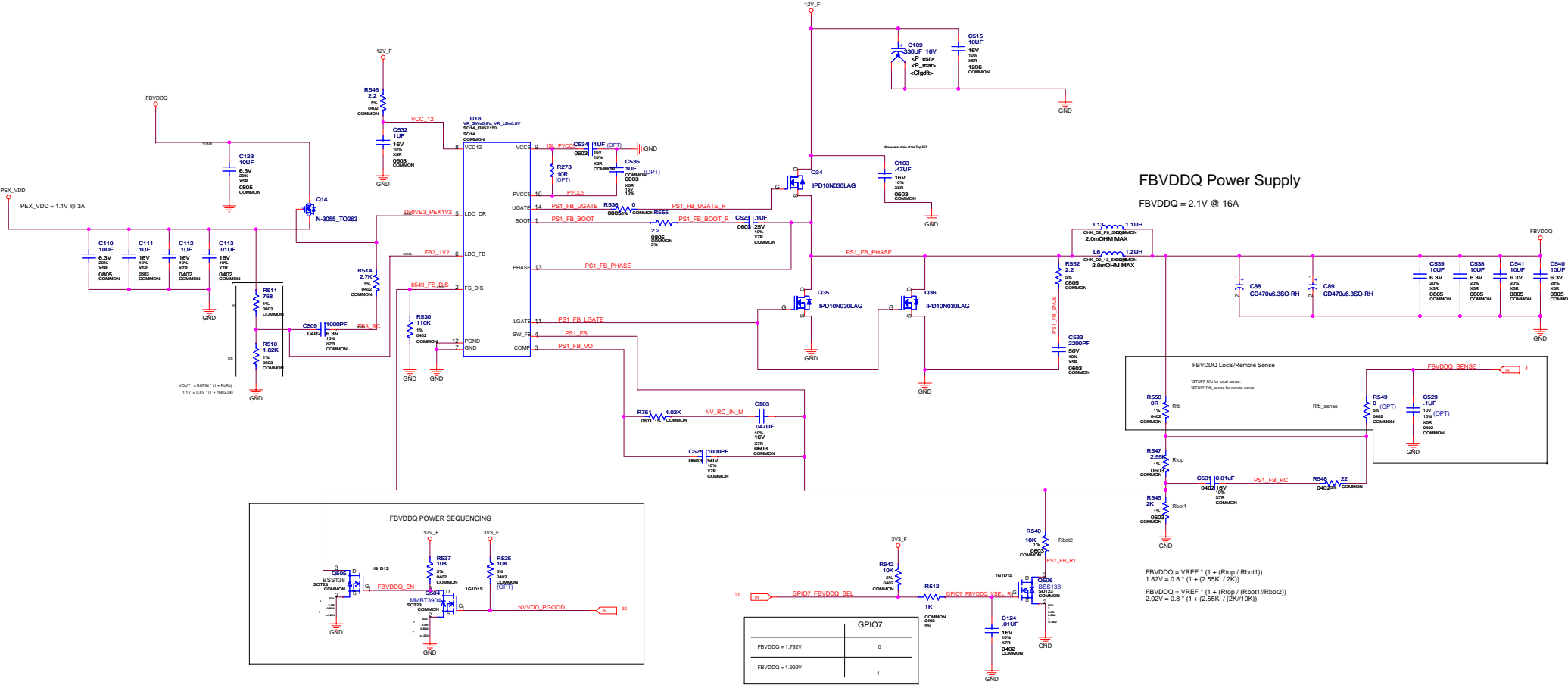
ASSEMBLY PAGE DETAIL PS II: PEX_VDD, IFP_PLLVDD, 2V5, 5V, and DDC_5V Power Supply



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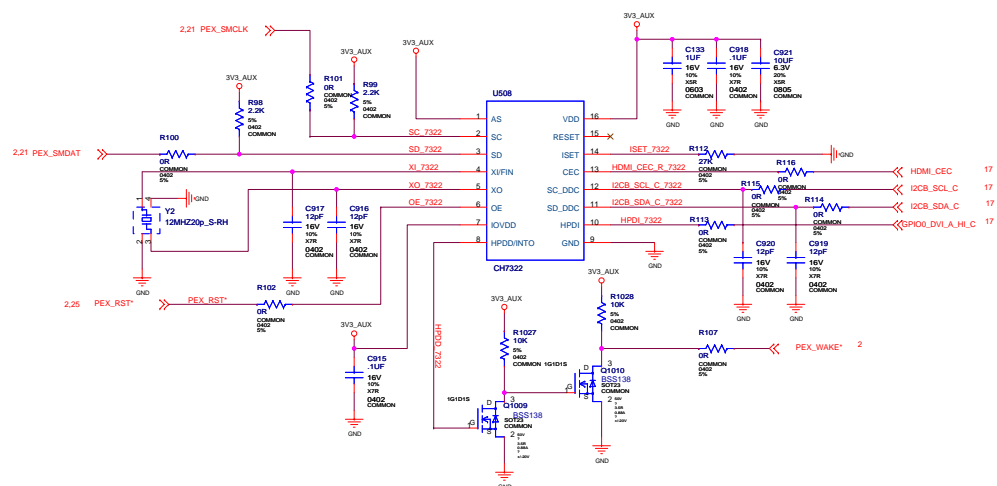
ASSEMBLY PAGE DETAIL PS III FBVDDQ Power Supply



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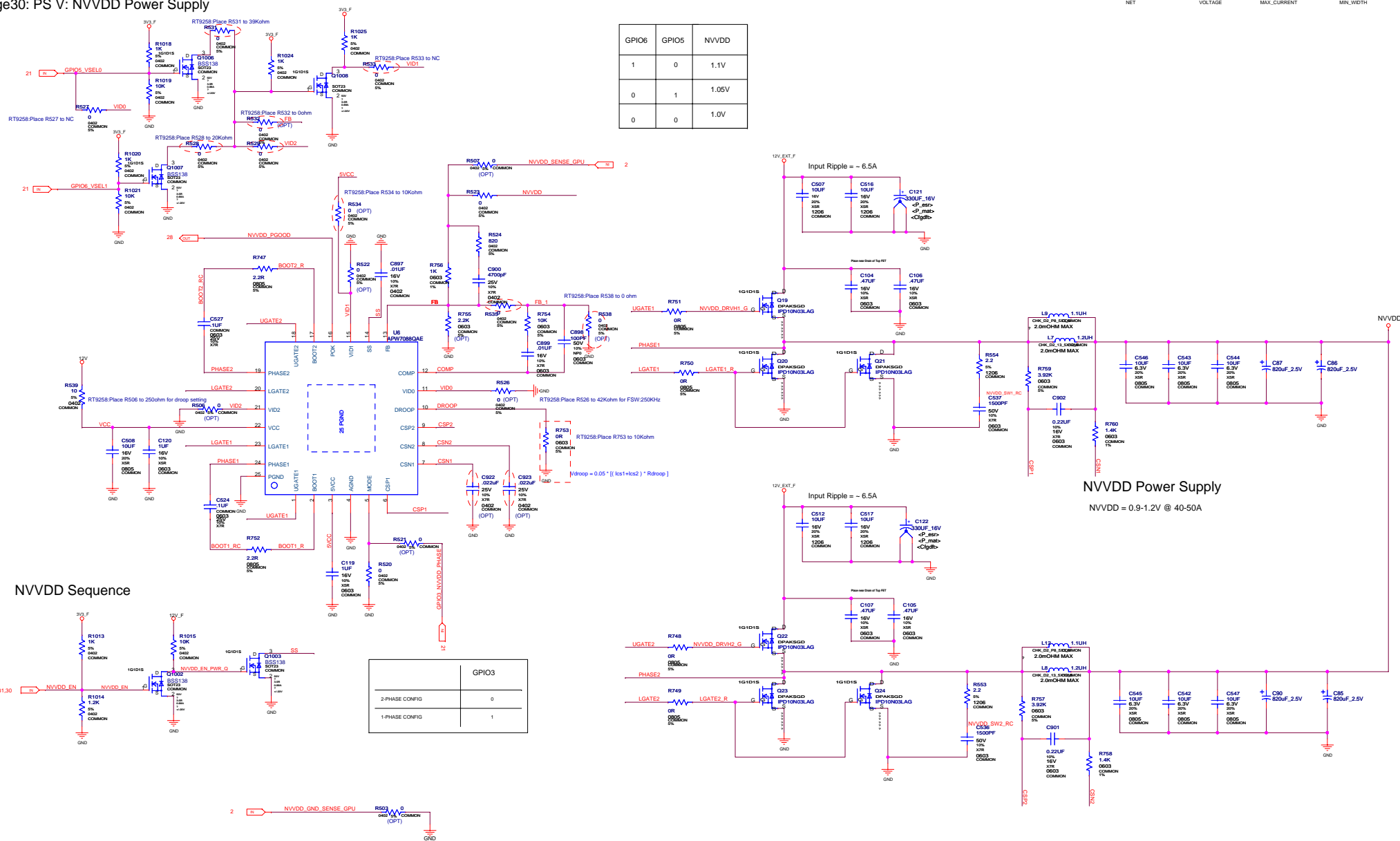
NVVDD Voltage Select
NVVDD range 0.80V-1.40V

Regulator: ADF3208
Control via NV_GPIOs NV_VSEL[1..0]

VID		NVDD	
6	543210	Vout	Q94
0	111111	0.80V	
0	110111	0.85V	
0	110011	0.90V	
0	101111	0.95V	
0	101011	1.00V	
0	100111	1.05V	
0	100011	1.10V	
0	011111	1.15V	
0	011011	1.20V	
0	010111	1.25V	
0	010011	1.30V	
0	001111	1.35V	
0	001011	1.40V	

⇒ Default
⇒ Voltage1
⇒ Voltage2

GPI06	GPI05	NVDD
1	0	1.1V
0	1	1.05V
0	0	1.0V



	GPI03
2-PHASE CONFIG	0
1-PHASE CONFIG	1

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ASSEMBLY	PS46 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS V: NVVDD Power Supply



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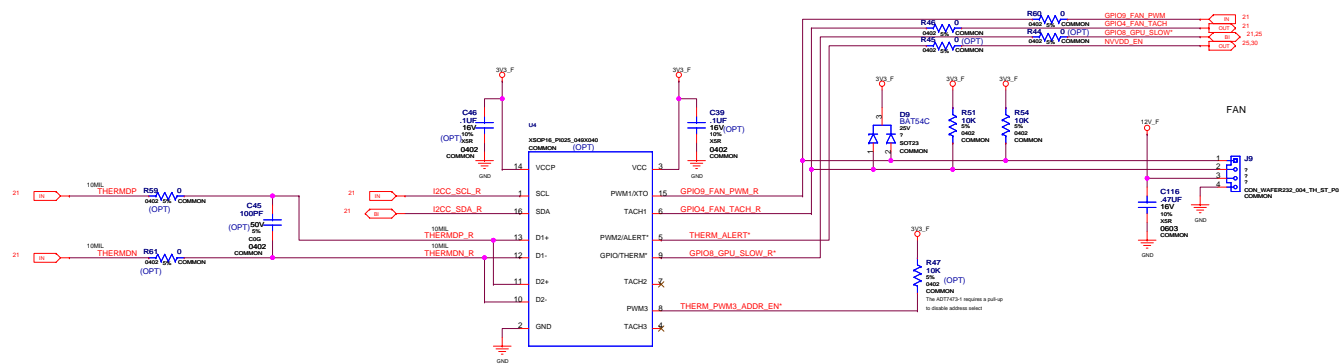
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ADT7473 External Fan/Thermal Control



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ASSEMBLY	P446 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Diode and Fan Control



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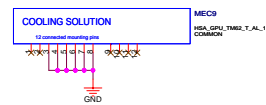
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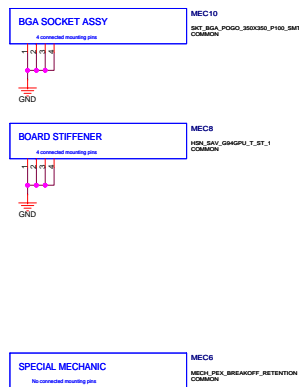
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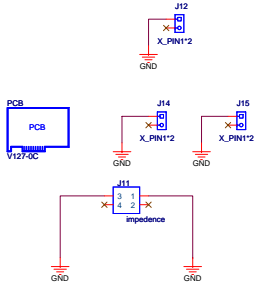
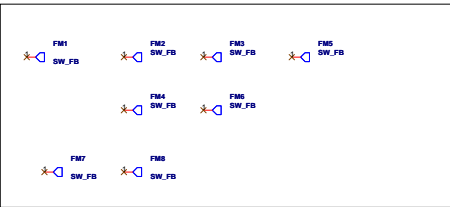
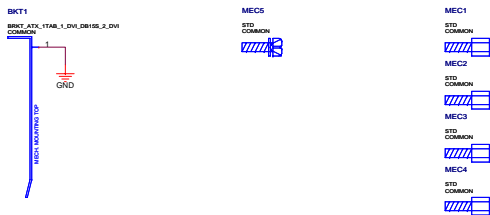
Thermal



Mechanical



Bracket



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ASSEMBLY
PAGE DETAIL

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Thermal, Mechanical, and Bracket



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