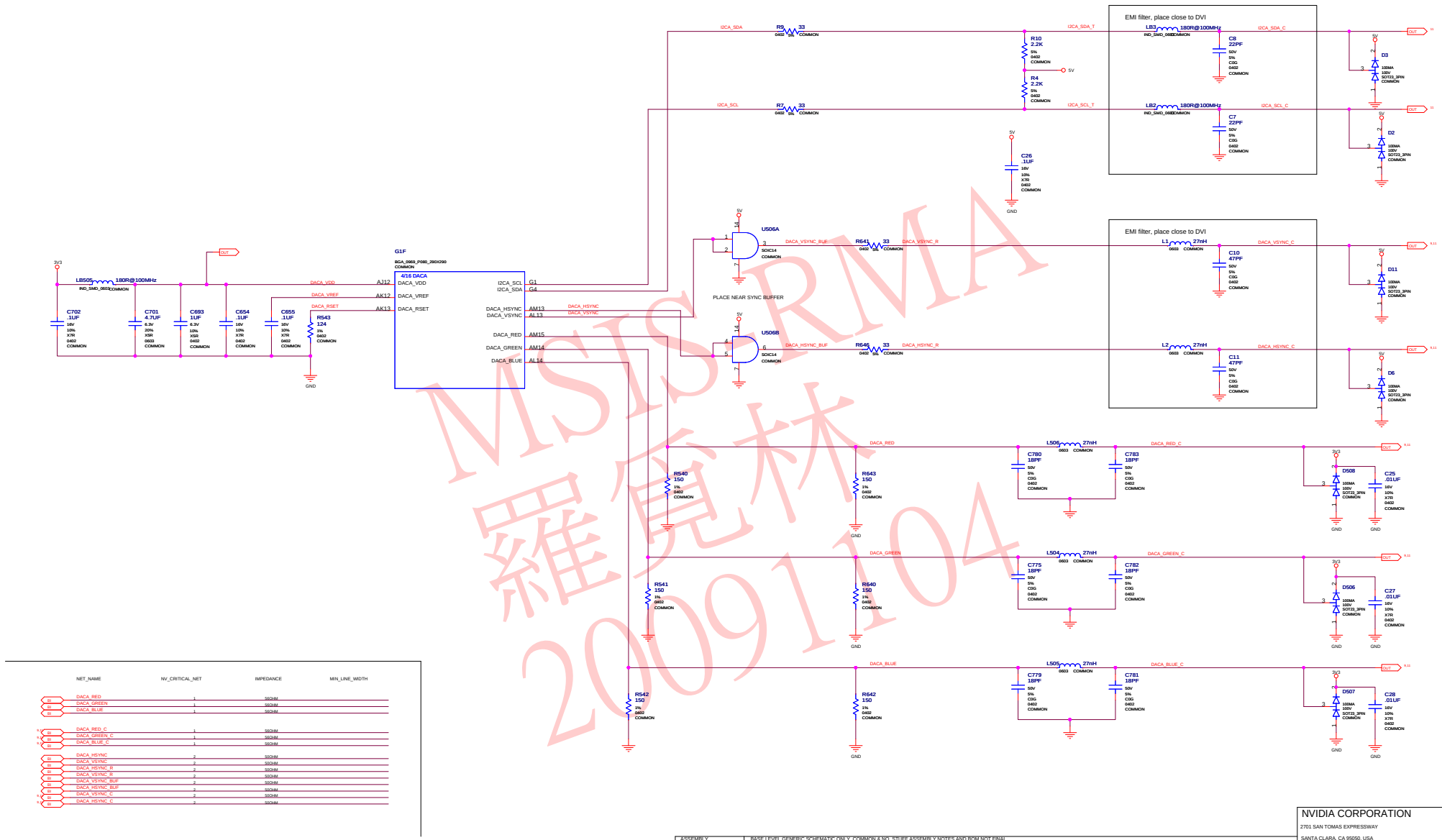
DACA (SOUTH DVI-I)



NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACA_RED	1	50OHM	
DACA_GREEN	1	50OHM	
DACA_BLUE	1	50OHM	
DACA_RED_C	1	50OHM	
DACA_GREEN_C	1	50OHM	
DACA_BLUE_C	1	50OHM	
DACA_HSYNC	2	50OHM	
DACA_VSYNC	2	50OHM	
DACA_HSYNC_R	2	50OHM	
DACA_VSYNC_R	2	50OHM	
DACA_VSYNC_BUF	2	50OHM	
DACA_HSYNC_BUF	2	50OHM	
DACA_VSYNC_C	2	50OHM	
DACA_HSYNC_C	2	50OHM	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA (SOUTH DVI-I)

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ID		PAGE	
NAME		DATE	05-FEB-2009

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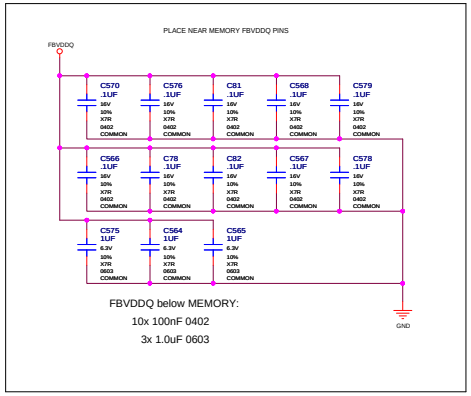
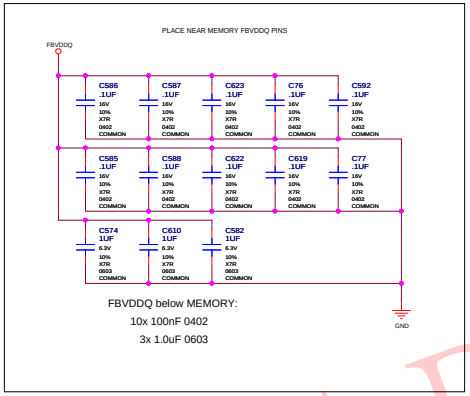
FBC DECOUPLING CAPS & NVVDD DECOUPLING CAPS

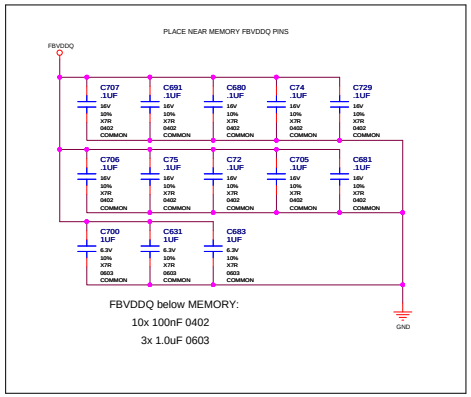
Decoupling for FBC 0..15



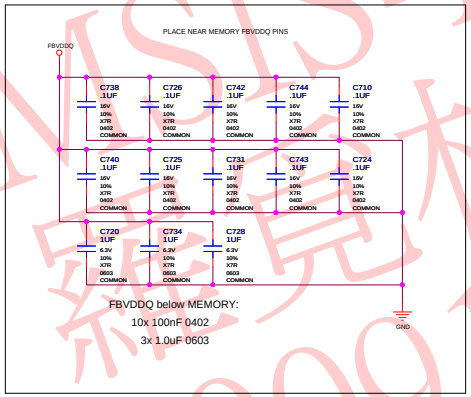
Decoupling for FBC 16..31

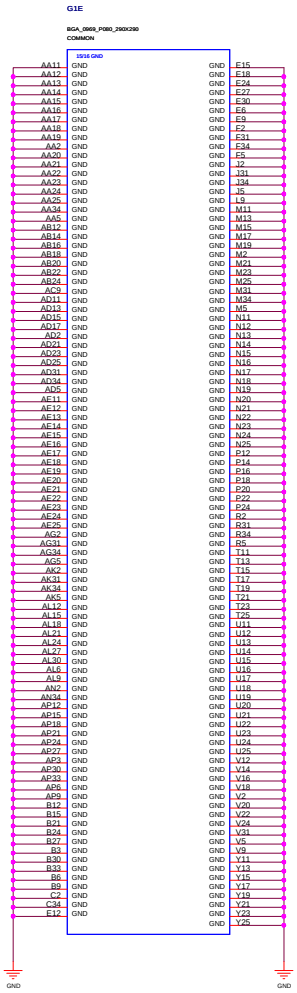


Decoupling for FBC 32..47



Decoupling for FBC 48..63





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PAGE DETAIL	FBC DECOUPLING CAPS
NV_PN	600-10681-base-100 A
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PAGE	
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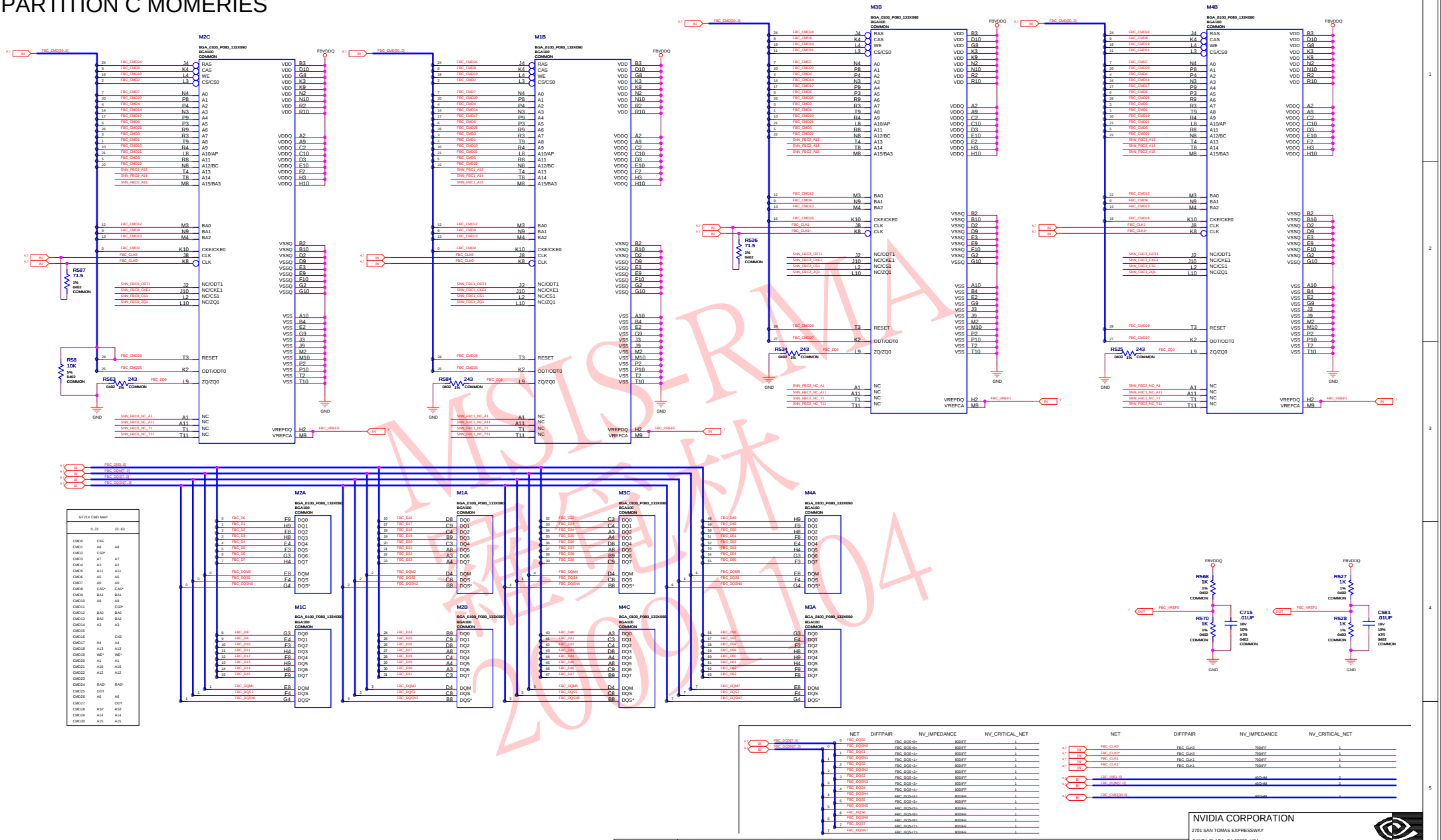
PARTITION C MOMERIES



GT21X CMD MAP		
	0..31	32..63
CMD0	CKE	
CMD1	A8	A8
CMD2	CS0*	
CMD3	A7	A7
CMD4	A2	A2
CMD5	A11	A11
CMD6	A5	A5
CMD7	A0	A0
CMD8	CAS*	CAS*
CMD9	BA1	BA1
CMD10	A9	A9
CMD11		CS0*
CMD12	BA0	BA0
CMD13	BA2	BA2
CMD14	A3	A3
CMD15		
CMD16		CKE
CMD17	A4	A4
CMD18	A13	A13
CMD19	WE*	WE*
CMD20	A1	A1
CMD21	A10	A10
CMD22	A12	A12
CMD23		
CMD24	RAS*	RAS*
CMD25	ODT	
CMD26	A6	A6
CMD27		ODT
CMD28	RST	RST
CMD29	A14	A14
CMD30	A15	A15

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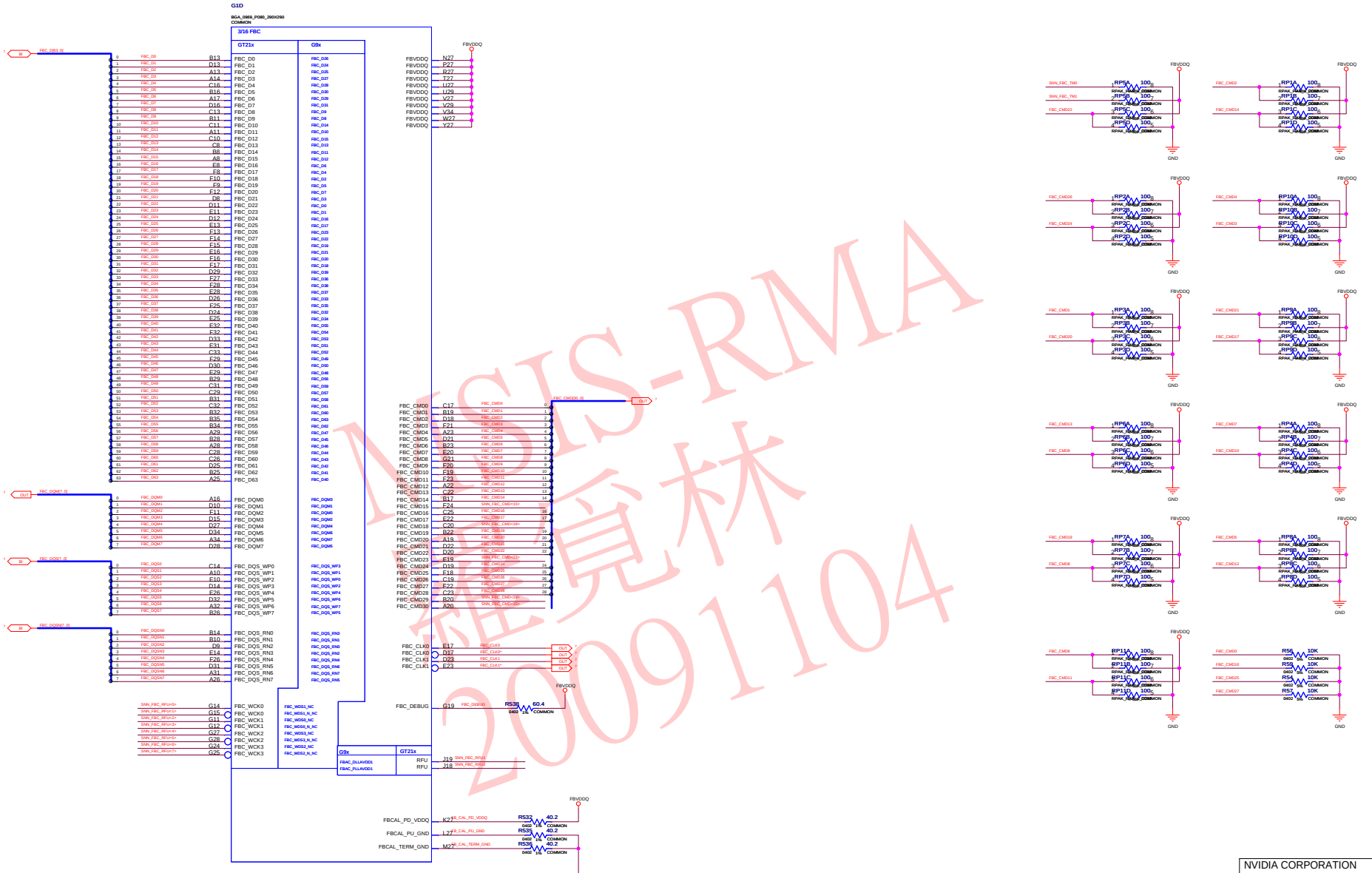
PARTITION C FRAME BUFFER INTERFACE



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PARTITION C FRAME BUFFER INTERFACE

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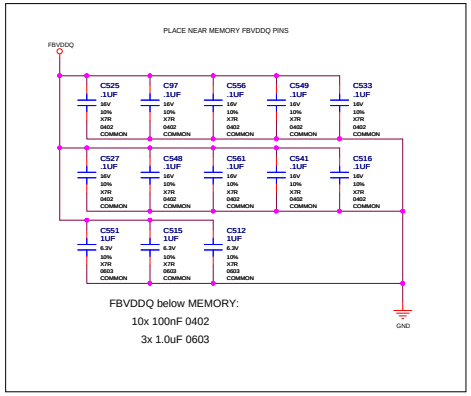
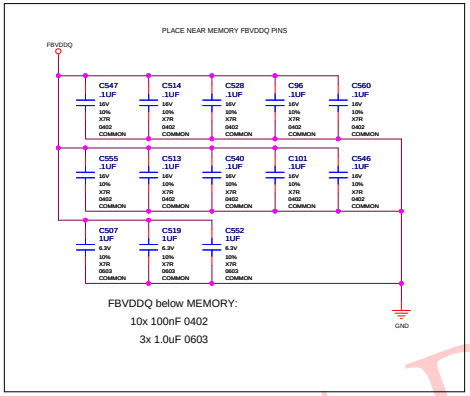
FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS

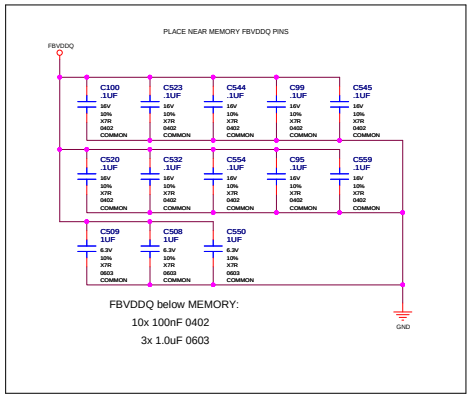
Decoupling for FBA 0..15



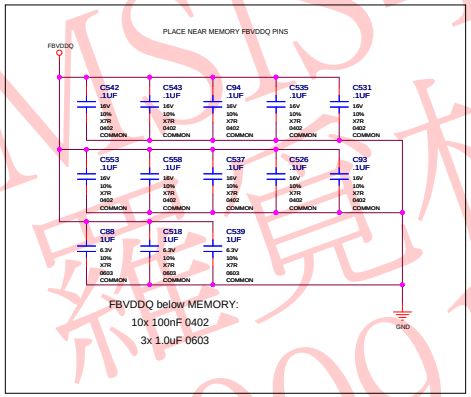
Decoupling for FBA 16..31

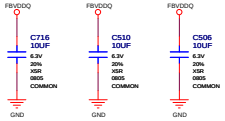


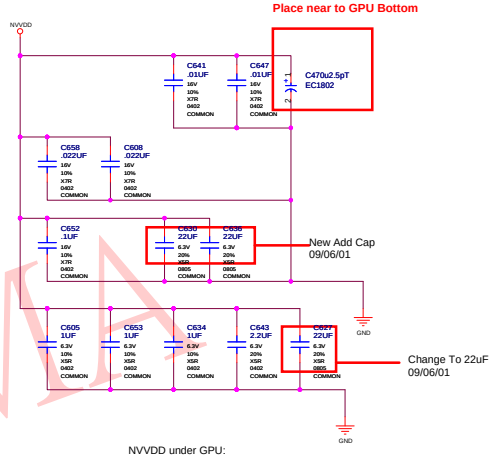
Decoupling for FBA 32..47



Decoupling for FBA 48..63



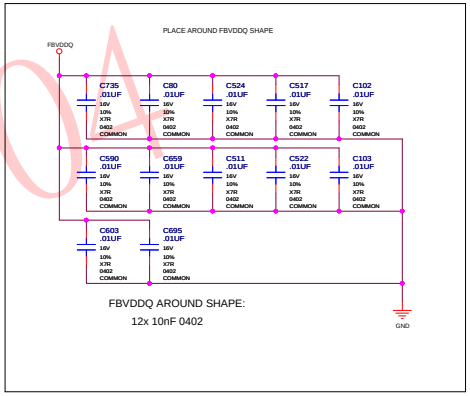


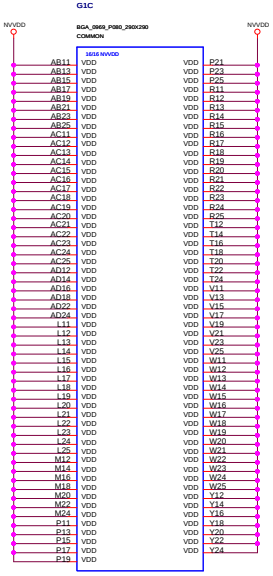


NVVDD under GPU:

4x 0.01uF 0402 X7R
5x 0.022uF 0402 X7R
2x 0.047uF 0402 X7R
1x 0.1uF 0402 X7R
1x 0.22uF 0402 X7R
4x 1.0uF 0402 X5R
1x 2.2uF 0402 X5R
2x 10uF 0805 X5R

Decoupling for EMI





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PAGE DETAIL	FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS

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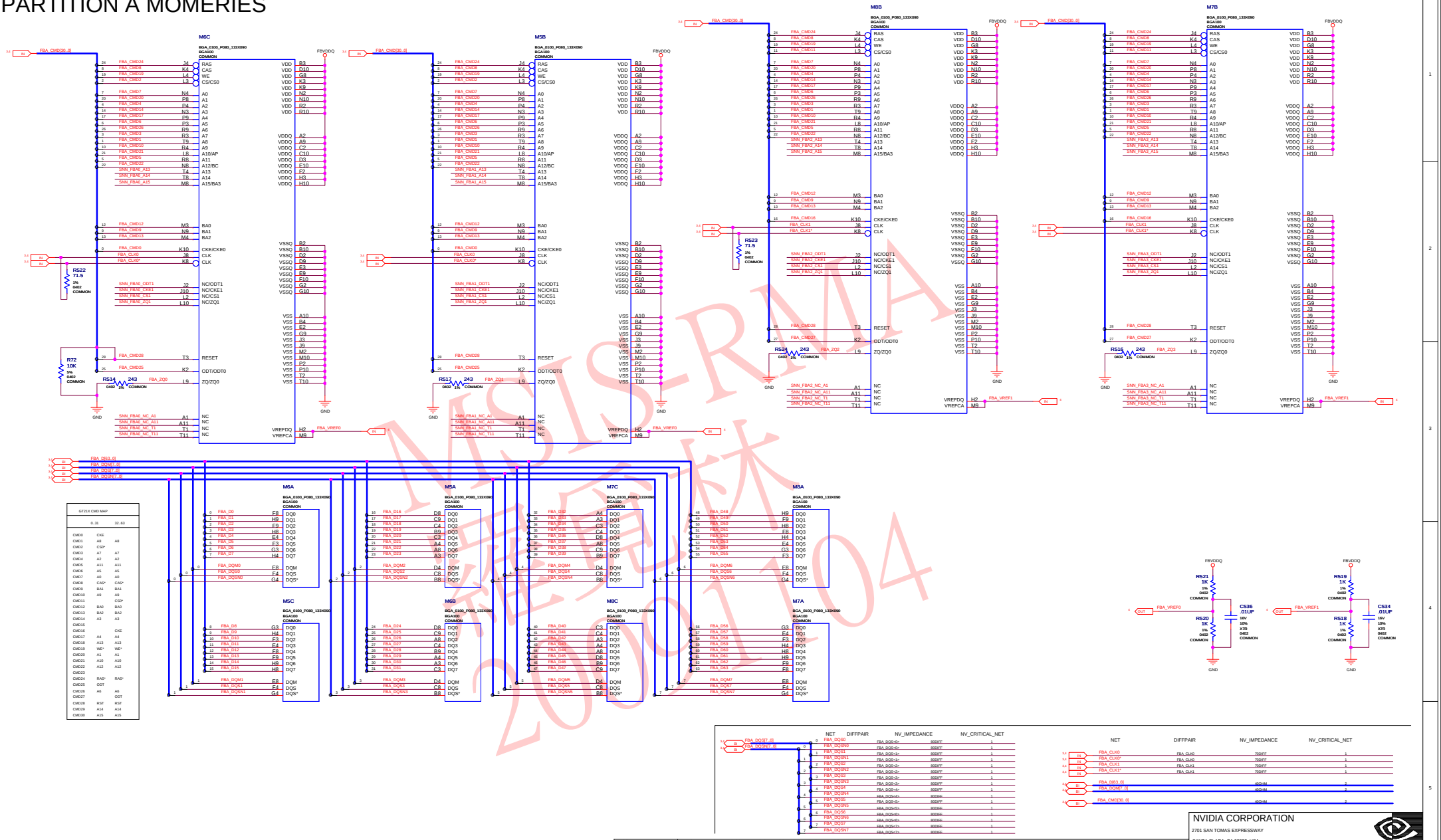
PARTITION A MOMERIES



GT21X CMD MAP

	0..31	32..63
CMD0	CKE	
CMD1	A8	A8
CMD2	CS0*	
CMD3	A7	A7
CMD4	A2	A2
CMD5	A11	A11
CMD6	A5	A5
CMD7	A0	A0
CMD8	CAS*	CAS*
CMD9	BA1	BA1
CMD10	A9	A9
CMD11		CS0*
CMD12	BA0	BA0
CMD13	BA2	BA2
CMD14	A3	A3
CMD15		
CMD16		CKE
CMD17	A4	A4
CMD18	A13	A13
CMD19	WE*	WE*
CMD20	A1	A1
CMD21	A10	A10
CMD22	A12	A12
CMD23		
CMD24	RAS*	RAS*
CMD25	ODT	
CMD26	A6	A6
CMD27		ODT
CMD28	RST	RST
CMD29	A14	A14
CMD30	A15	A15

NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
FBA_DQS0	FBA_DQS<0>	900IFF	1
FBA_DQSN0	FBA_DQS<0>	900IFF	1
FBA_DQS1	FBA_DQS<1>	900IFF	1
FBA_DQSN1	FBA_DQS<1>	900IFF	1
FBA_DQS2	FBA_DQS<2>	900IFF	1
FBA_DQSN2	FBA_DQS<2>	900IFF	1
FBA_DQS3	FBA_DQS<3>	900IFF	1
FBA_DQSN3	FBA_DQS<3>	900IFF	1
FBA_DQS4	FBA_DQS<4>	900IFF	1
FBA_DQSN4	FBA_DQS<4>	900IFF	1
FBA_DQS5	FBA_DQS<5>	900IFF	1
FBA_DQSN5	FBA_DQS<5>	900IFF	1
FBA_DQS6	FBA_DQS<6>	900IFF	1
FBA_DQSN6	FBA_DQS<6>	900IFF	1
FBA_DQS7	FBA_DQS<7>	900IFF	1
FBA_DQSN7	FBA_DQS<7>	900IFF	1

NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
FBA_CLK0	FBA_CLK0	70DIFF	1
FBA_CLK0*	FBA_CLK0	70DIFF	1
FBA_CLK1	FBA_CLK1	70DIFF	1
FBA_CLK1*	FBA_CLK1	70DIFF	1
FBA_DQ[63..0]		40OHM	2
FBA_DQM[7..0]		40OHM	2
FBA_CMD[30..0]		40OHM	2

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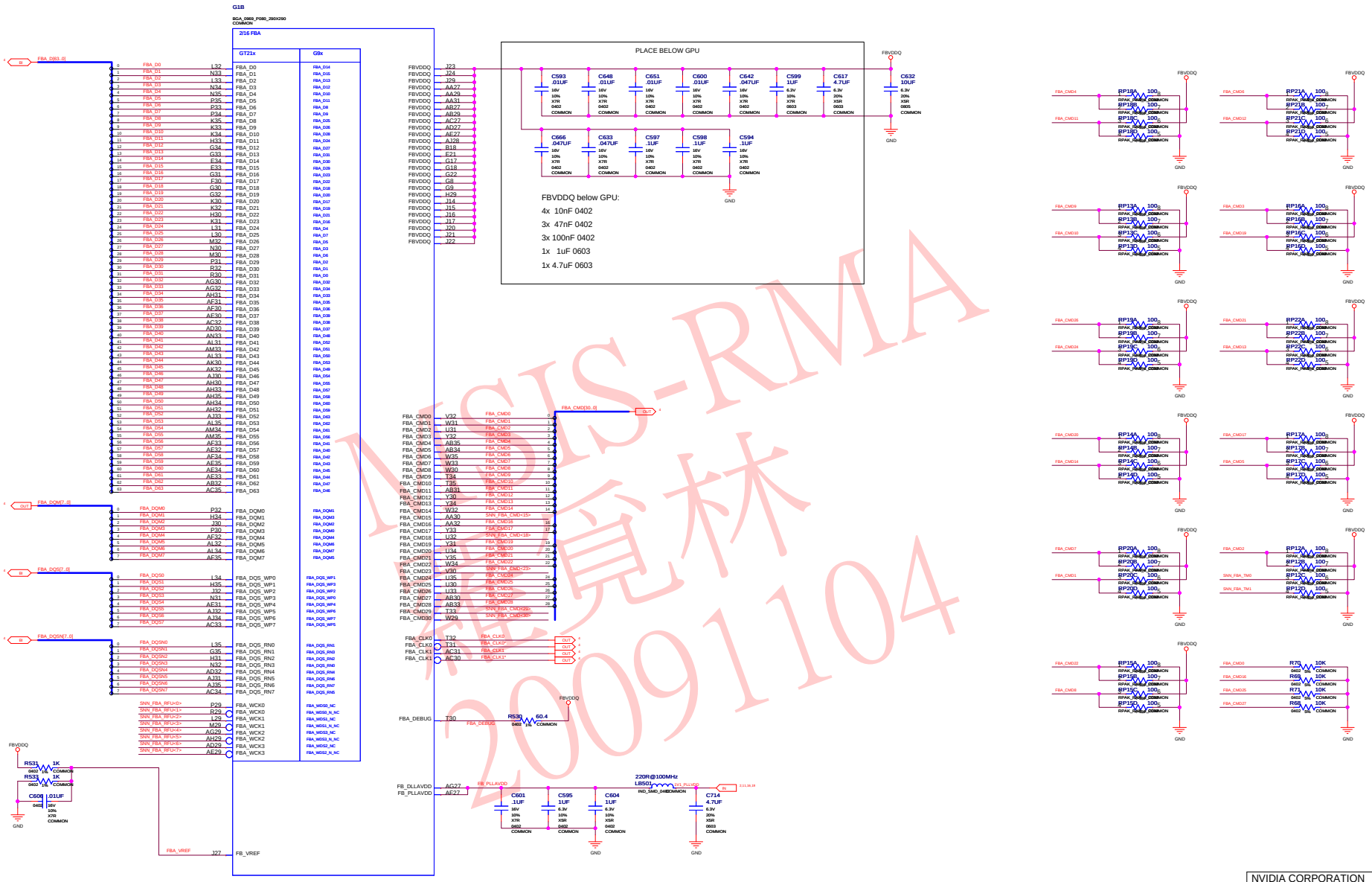
NAME		DATE	05-FEB-2009

PARTITION A FRAME BUFFER INTERFACE



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ASSEMBLY	
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NAME		DATE	05-FEB-2009

Title: Cnxf Part
Report:
Design: p881
Date: Jan 22
13:35:02 2009

BKT1 [16.4E]
C1 [12.4F]
C2 [10.3G]
C3 [12.3G]
C4 [11.2G]
C5 [12.4F]
C6 [10.3G]
C7 [9.2G]
C8 [9.1G]
C9 [19.4D]
C10 [9.2G]
C11 [9.3G]
C12 [12.2D]
C13 [12.3E]
C14 [12.3E]
C15 [12.3E]
C16 [12.3E]
C17 [12.3E]
C18 [12.3E]
C19 [12.3E]
C20 [12.3E]
C21 [12.2G]
C22 [10.2G]
C23 [11.4F]
C24 [10.1G]
C25 [10.2G]
C26 [10.2F]
C27 [9.2F]
C28 [19.4C]
C29 [11.4E]
C30 [19.4B]
C31 [20.3B]
C32 [19.4C]
C33 [21.1E]
C34 [20.3B]
C35 [21.1E]
C36 [19.4B]
C37 [19.4A]
C38 [20.3B]
C39 [21.3B]
C40 [21.3G]
C41 [20.2C]
C42 [21.3F]
C43 [21.3B]
C44 [20.2C]
C45 [17.4G]
C46 [21.3G]
C47 [17.4G]
C48 [21.3F]
C49 [2.1A]
C50 [17.3G]
C51 [21.1G]
C52 [21.3C]
C53 [18.5F]
C54 [21.1F]
C55 [18.4F]
C56 [21.4D]
C57 [21.4G]
C58 [17.4C]
C59 [2.1A]
C60 [2.1A]
C61 [21.1G]
C62 [21.4H]
C63 [19.4F]
C64 [21.1F]
C65 [21.3H]
C66 [16.3C]
C67 [16.3D]
C68 [19.2B]
C69 [19.2C]
C70 [2.4G]
C71 [16.3A]
C72 [8.3B]
C73 [10.3B]
C74 [8.3B]
C75 [8.3A]
C76 [8.1D]
C77 [8.2D]
C78 [8.2A]
C79 [21.4B]
C80 [5.4F]
C81 [8.1B]
C82 [8.2B]
C83 [20.2G]
C84 [20.2H]
C85 [20.3G]
C86 [20.2F]
C87 [20.2G]
C88 [20.3G]

C89 [20.2F]
C90 [20.2F]
C91 [20.3H]
C92 [21.4G]
C93 [20.3G]
C94 [5.3D]
C95 [5.3D]
C96 [5.3B]
C97 [5.1D]
C98 [5.1A]
C99 [20.4C]
C100 [5.3B]
C101 [5.3A]
C102 [5.2D]
C103 [20.4F]
C104 [5.4F]
C105 [5.4F]
C106 [5.5C]
C107 [20.3G]
C108 [20.3D]
C109 [20.3F]
C110 [20.3D]
C111 [21.4D]
C112 [21.4D]
C113 [21.3E]
C114 [21.4H]
C115 [21.4G]
C116 [20.2G]
C117 [21.4H]
C118 [21.4G]
C119 [15.2B]
C120 [21.3C]
C130 [17.1E]
C131 [17.2E]
C132 [21.4E]
C501 [20.2E]
C502 [20.2D]
C503 [5.2C]
C504 [5.4A]
C505 [5.4A]
C506 [5.5C]
C507 [5.4F]
C508 [5.2B]
C509 [5.2C]
C510 [5.1C]
C511 [5.2A]
C512 [5.2B]
C513 [5.4F]
C514 [5.4C]
C515 [5.2C]
C516 [5.3A]
C517 [20.2C]
C518 [5.4F]
C519 [5.3A]
C520 [5.4F]
C521 [5.1A]
C522 [5.3D]
C523 [5.2A]
C524 [5.1D]
C525 [20.2D]
C526 [20.3C]
C527 [5.3D]
C528 [5.3A]
C529 [5.1B]
C530 [4.4H]
C531 [5.3D]
C532 [4.4G]
C533 [5.3D]
C534 [5.4C]
C535 [5.4D]
C536 [5.2D]
C537 [5.2B]
C538 [5.3C]
C539 [5.3C]
C540 [5.3B]
C541 [5.3B]
C542 [5.2D]
C543 [5.1C]
C544 [5.2A]
C545 [5.1B]
C546 [5.4B]
C547 [5.2A]
C548 [5.2D]
C549 [5.3C]
C550 [5.3B]
C551 [5.2C]
C552 [5.1B]
C553 [20.2F]
C554 [5.3C]
C555 [5.3B]
C556 [5.1D]
C557 [5.2B]
C558 [20.2G]
C559 [20.2G]
C560 [8.2A]
C561 [8.2B]

C562 [8.2A]
C563 [8.2B]
C564 [8.1B]
C565 [2.5C]
C566 [8.1A]
C567 [2.5C]
C568 [2.5C]
C569 [2.5C]
C570 [8.2C]
C571 [8.2A]
C572 [8.1A]
C573 [2.5C]
C574 [8.2B]
C575 [8.1B]
C576 [2.5C]
C577 [7.4H]
C578 [8.2D]
C579 [2.4C]
C580 [2.4C]
C581 [8.2C]
C582 [8.1C]
C583 [8.1C]
C584 [8.2C]
C585 [2.4C]
C586 [5.4E]
C587 [2.4C]
C588 [8.1D]
C589 [3.1D]
C590 [3.2E]
C591 [3.5D]
C592 [3.5D]
C593 [2.4C]
C594 [3.2D]
C595 [3.2D]
C596 [3.1E]
C597 [3.1D]
C598 [3.5C]
C599 [2.4C]
C600 [5.4E]
C601 [3.5D]
C602 [5.2E]
C603 [3.5A]
C604 [2.1F]
C605 [5.2F]
C606 [2.4C]
C607 [8.2C]
C608 [5.2F]
C609 [2.1F]
C610 [5.2F]
C611 [5.2F]
C612 [2.4C]
C613 [2.1E]
C614 [3.1E]
C615 [2.1F]
C616 [8.2D]
C617 [5.1E]
C618 [5.2F]
C619 [8.2D]
C620 [8.1D]
C621 [2.4C]
C622 [2.1F]
C623 [5.1F]
C624 [5.2G]
C625 [2.4C]
C626 [2.2E]
C627 [5.2F]
C628 [8.4A]
C629 [3.1E]
C630 [3.2D]
C631 [5.2F]
C632 [2.1F]
C633 [5.2F]
C634 [2.1F]
C635 [2.1F]
C636 [2.1E]
C637 [2.3C]
C638 [5.1F]
C639 [3.1E]
C640 [5.2F]
C641 [2.4E]
C642 [2.3C]
C643 [2.1F]
C644 [5.1F]
C645 [3.1D]
C646 [5.2E]
C647 [5.2F]
C648 [3.1D]
C649 [5.2F]
C650 [5.2F]
C651 [9.3B]
C652 [9.3B]
C653 [2.4E]
C654 [2.3F]
C655 [5.2E]
C656 [5.4F]
C657 [16.3B]

C658 [11.3B]
C659 [2.3F]
C660 [15.3B]
C661 [12.2B]
C662 [3.2D]
C663 [11.3B]
C664 [2.3C]
C665 [2.3C]
C666 [2.4F]
C667 [12.2B]
C668 [2.2F]
C669 [12.4B]
C670 [16.3B]
C671 [11.3B]
C672 [11.3B]
C673 [2.2F]
C674 [2.4F]
C675 [8.3B]
C676 [8.3B]
C677 [2.2F]
C678 [8.4B]
C679 [10.3B]
C680 [17.3B]
C681 [11.3B]
C682 [2.3C]
C683 [2.3C]
C684 [11.3B]
C685 [2.2G]
C686 [8.3A]
C687 [10.3B]
C688 [11.3B]
C689 [9.3A]
C690 [16.3B]
C691 [5.4F]
C692 [12.4A]
C693 [2.3C]
C694 [8.4A]
C695 [9.3A]
C696 [12.2A]
C697 [10.3A]
C698 [9.3A]
C699 [2.3C]
C700 [12.4A]
C701 [8.3B]
C702 [8.3A]
C703 [8.3A]
C704 [11.3A]
C705 [2.3C]
C706 [8.3D]
C707 [16.3B]
C708 [10.3A]
C709 [11.3A]
C710 [2.3C]
C711 [3.5D]
C712 [7.4G]
C713 [5.5B]
C714 [12.2A]
C715 [19.2C]
C716 [19.2G]
C717 [8.4C]
C718 [19.2F]
C719 [2.2C]
C720 [2.2C]
C721 [8.3D]
C722 [8.3C]
C723 [8.3C]
C724 [8.4G]
C725 [8.3B]
C726 [17.2C]
C728 [8.3D]
C729 [2.2C]
C730 [2.2C]
C731 [8.4C]
C732 [5.4E]
C733 [18.3F]
C734 [19.2F]
C735 [8.3C]
C736 [8.3C]
C737 [2.2C]
C738 [8.3D]
C739 [8.3D]
C740 [8.3D]
C742 [2.2C]
C743 [21.2A]
C744 [21.2F]
C746 [21.2F]
C748 [21.1F]
C750 [21.2E]
C752 [21.2C]
C755 [2.1A]
C757 [21.2C]
C758 [21.3E]
C759 [21.3F]
C760 [21.4F]
C761 [21.3F]
C762 [21.2B]

C763 [9.2E]
C764 [10.3E]
C765 [10.4E]
C766 [10.4E]
C767 [12.4B]
C768 [9.4F]
C769 [10.4F]
C770 [10.4F]
C771 [10.3F]
C772 [9.5F]
C773 [9.3F]
C774 [9.5F]
C775 [9.4F]
C776 [9.3F]
CN1 [2.3B]
D1 [12.4E]
D2 [9.2E]
D3 [9.1E]
D4 [10.2E]
D5 [10.1E]
D6 [12.2E]
D7 [9.3F]
D8 [10.2F]
D9 [10.3F]
D10 [9.2F]
D11 [11.4E]
D12 [12.2E]
D13 [17.4F]
D14 [19.4B]
D15 [17.3F]
D16 [18.5G]
D501 [20.3F]
D502 [17.2E]
D503 [17.2F]
D508 [10.3E]
D509 [10.5E]
D510 [10.4E]
D511 [9.4E]
D512 [9.5E]
D513 [9.4E]
F1 [19.4C]
G1 [2.3D]
G1 [3.3C]
G1 [5.4H]
G1 [8.3C]
G1 [8.3G]
G1 [9.3C]
G1 [10.3C]
G1 [11.3C]
G1 [12.4B]
G1 [13.3D]
G1 [14.3D]
G1 [15.2C 15.4C]
G1 [16.3C]
G1 [17.3C]
G1 [18.4C]
J1 [10.5G]
J2 [12.3H]
J3 [11.3D]
J4 [10.4D]
J5 [17.4H]
J6 [17.3H]
J7 [17.5B]
L1 [9.2G]
L2 [9.3G]
L3 [10.3G]
L4 [10.2C]
L5 [21.2G]
L7 [17.4F]
L8 [21.4G]
L10 [20.2G]
L11 [20.2G]
LS01 [10.4E]
LS02 [10.4F]
LS03 [10.3E]
LS04 [9.4F]
LS05 [9.4F]
LS06 [9.3F]
LB1 [12.4F]
LB2 [9.2G]
LB3 [9.1G]
LB4 [11.4F]
LB5 [10.1F]
LB6 [10.1F]
LB501 [3.5D]
LB502 [11.3A]
LB503 [2.4F]
LB504 [9.2A]
LB505 [11.3A]
LB506 [16.3A]
LB507 [12.2A]
LB508 [10.2A]
LB509 [12.3A]
M1 [7.2D 7.4B 7.4C]
M2 [7.4B 7.4C 7.2B]
M3 [7.2F 7.4D 7.4E]
M4 [7.4E 7.4D 7.2H]
M5 [4.4C 4.4B 4.2D]
M6 [4.2B 4.4B 4.4C]
M7 [4.2H 4.4E 4.4D]
M8 [4.2F 4.4E 4.4D]
MEC1 [16.2F]
MEC2 [16.2F]
MEC3 [16.3E]
MEC4 [16.2E]
MEC5 [16.2E]
MEC6 [16.3G]
Q1 [12.4D]
Q2 [12.1E]
Q3 [12.2E]
Q4 [11.4D]
Q5 [20.2B]
Q6 [21.4F]
Q7 [21.4F]
Q8 [17.4F]
Q9 [21.2F]
Q10 [21.2F]
Q11 [19.4G]
Q12 [19.4F]
Q13 [17.2E]
Q14 [20.2E]
Q15 [20.3E]
Q16 [20.4F]
Q17 [20.4B]
Q18 [20.4C]
Q19 [21.4B]
Q20 [17.1E]
Q502 [17.2F]
Q503 [21.2B]
Q504 [21.2B]
Q505 [21.3B]
Q507 [21.2B]
Q508 [12.4A]
R1 [12.4D]
R2 [12.4F]
R3 [12.4E]
R4 [9.1F]
R5 [12.2F]
R6 [9.2E]
R7 [10.1E]
R8 [9.1E]
R9 [9.1F]
R10 [11.4E]
R11 [10.1F]
R12 [10.1E]
R13 [10.1F]
R14 [12.2D]
R15 [12.1D]
R16 [11.4D]
R17 [12.2F]
R18 [11.4D]
R19 [12.2D]
R20 [12.2D]
R21 [19.4B]
R22 [19.4B]
R23 [19.4A]
R24 [17.4G]
R25 [17.4F]
R26 [2.1B]
R27 [2.1C]
R28 [17.4C]
R29 [18.4E]
R30 [18.4E]
R31 [18.5E]
R32 [18.5F]
R33 [17.5C]
R34 [2.2C]
R35 [17.3G]
R36 [17.2E]
R37 [17.3G]
R38 [17.2E]
R39 [17.4C]
R40 [17.4B]
R41 [17.1E]
R42 [19.4F]
R43 [17.5C]
R44 [19.4G]
R45 [19.2C]
R46 [19.2C]
R47 [19.2C]
R48 [17.2D]
R49 [17.2C]
R50 [18.4D]
R51 [17.3E]

R52 [17.4E]
R53 [13.3C]
R54 [15.5D]
R55 [10.3B]
R56 [8.4H]
R57 [2.1C]
R58 [8.4H]
R59 [8.4H]
R60 [7.3A]
R61 [8.4H]
R62 [20.2F]
R63 [20.4B]
R64 [20.4B]
R65 [20.2E]
R66 [20.4E]
R67 [20.4E]
R68 [20.4E]
R69 [20.4F]
R70 [20.4F]
R71 [20.4G]
R72 [3.4H]
R73 [3.4H]
R74 [20.3G]
R75 [20.3D]
R76 [3.4H]
R77 [3.4H]
R78 [4.3A]
R79 [21.4A]
R80 [21.4A]
R81 [21.4B]
R82 [21.1B]
R83 [15.1B]
R84 [15.3D]
R85 [21.4C]
R86 [21.4C]
R101 [20.4B]
R167 [21.1E]
R168 [21.3A]
R169 [21.3A]
R170 [21.4A]
R171 [21.3A]
R172 [21.3B]
R173 [21.3B]
R174 [21.2C]
R175 [21.3C]
R176 [21.3C]
R177 [21.3C]
R178 [21.2C]
R179 [21.2C]
R180 [21.2C]
R181 [21.3C]
R182 [21.3C]
R183 [21.4D]
R184 [21.3D]
R185 [21.4D]
R186 [21.4D]
R187 [21.3E]
R189 [21.3E]
R190 [21.1E]
R191 [21.1E]
R194 [17.1E]
R195 [17.2E]
R196 [17.2E]
R197 [21.2B]
R199 [21.3C]
R200 [21.4D]
R201 [21.4E]
R202 [21.4E]
R203 [21.2C]
R501 [20.2D]
R502 [20.2D]
R503 [20.3C]
R504 [20.3C]
R505 [20.3B]
R506 [20.3B]
R507 [4.3A]
R508 [4.3G]
R509 [20.2D]
R510 [4.3C]
R511 [4.4H]
R512 [4.4H]
R513 [4.4G]
R514 [4.4G]
R515 [4.2A]
R516 [4.2E]
R517 [4.3E]
R518 [7.3G]
R519 [7.2E]
R520 [7.4H]
R521 [7.4H]
R522 [2.5F]
R523 [3.4D]
R524 [3.5A]
R525 [6.5D]
R526 [3.5A]
R527 [7.3E]

R528 [6.5D]
R529 [6.5D]
R530 [2.5F]
R531 [6.4D]
R532 [2.2C]
R533 [9.3D]
R534 [9.4D]
R535 [9.5D]
R536 [9.3B]
R537 [13.3C]
R538 [18.4B]
R539 [11.3B]
R540 [12.3B]
R541 [18.2B]
R542 [18.4B]
R543 [18.2C]
R544 [14.3C]
R545 [10.3D]
R546 [18.2B]
R547 [10.4D]
R548 [18.2B]
R549 [10.5D]
R550 [18.2C]
R551 [18.2B]
R552 [14.3C]
R553 [16.3D]
R554 [7.3A]
R555 [17.3D]
R556 [17.3D]
R557 [17.2C]
R558 [16.3C]
R559 [7.4G]
R560 [18.2D]
R561 [7.4G]
R562 [18.3F]
R563 [18.2D]
R565 [19.2F]
R566 [19.2F]
R567 [18.2D]
R568 [19.2F]
R569 [17.3E]
R570 [18.2D]
R572 [17.3E]
R573 [18.2E]
R574 [18.2E]
R580 [7.3C]
R581 [7.2A]
R582 [21.2B]
R583 [21.2A]
R584 [21.2A]
R589 [21.2E]
R590 [21.2F]
R591 [2.1C]
R595 [21.2D]
R596 [2.1C]
R597 [2.1C]
R599 [2.1B]
R603 [2.1C]
R604 [21.2C]
R605 [21.4D]
R610 [21.3F]
R611 [21.2B]
R612 [21.3E]
R614 [10.3D]
R615 [10.5D]
R616 [10.4D]
R617 [9.4E]
R618 [9.2E]
R619 [9.5E]
R620 [9.3E]
R621 [9.3E]
R622 [12.4A]
R623 [10.2E]
R624 [12.4B]
R625 [12.4B]
R626 [12.4B]
R627 [12.4B]
R628 [12.4B]
R629 [12.4B]
R630 [12.4B]
R631 [12.4B]
R632 [10.3E]
RP1 [6.1H 6.1H 6.1H 6.1H]
RP2 [6.2G 6.2G 6.2G 6.2G]
RP3 [6.2G 6.3G 6.2G 6.3G]
RP4 [6.3H 6.3H 6.3H 6.3H]
RP5 [6.1G 6.1G 6.1G 6.1G]
RP6 [6.3G 6.3G 6.3G 6.3G]
RP7 [6.4G 6.4G 6.4G 6.4G]

RP8 [6.4H 6.4H 6.4H 6.4H]
RP9 [6.3H 6.3H 6.2H 6.2H]
RP10 [6.2H 6.2H 6.2H 6.2H]
RP11 [6.4G 6.4G 6.4G 6.4G]
RP12 [3.4H 3.4H 3.4H 3.4H]
RP13 [3.2G 3.2G 3.2G 3.2G]
RP14 [3.3G 3.3G 3.3G 3.3G]
RP15 [3.4G 3.4G 3.4G 3.4G]
RP16 [3.2H 3.2H 3.2H 3.2H]
RP17 [3.3H 3.3H 3.3H 3.3H]
RP18 [3.1G 3.1G 3.1G 3.1G]
RP19 [3.3G 3.3G 3.2G 3.2G]
RP20 [3.4G 3.4G 3.4G 3.4G]
RP21 [3.1H 3.1H 3.1H 3.1H]
RP22 [3.3H 3.3H 3.2H 3.2H]
U1 [12.2E]
U2 [19.4B]
U3 [18.5F]
U4 [18.4F]
U5 [19.2B]
U6 [21.3D]
US01 [20.3D]
US02 [17.2B]
US03 [18.3F]
US04 [19.2F]
US06 [9.2D 9.3D]
US06 [10.2D 10.3D]
Y1 [16.3C]

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NAME	<ENGINEER>	DATE	05-FEB-2009

SNN_FBA2_NC_A1 4.3E
SNN_FBA2_NC_A11 4.3E
SNN_FBA2_NC_T1 4.3E
SNN_FBA2_NC_T11 4.3E
SNN_FBA2_ODT1 4.2E
SNN_FBA2_ZQ1 4.2E
SNN_FBA3_CKE1 4.2G
SNN_FBA3_CS1 4.2G
SNN_FBA3_NC_A1 4.3G
SNN_FBA3_NC_A11 4.3G
SNN_FBA3_NC_T1 4.3G
SNN_FBA3_NC_T11 4.3G
SNN_FBA3_ODT1 4.2G
SNN_FBA3_ZQ1 4.2G
SNN_FBA_CMD<15> 3.3C
SNN_FBA_CMD<23> 3.4C
SNN_FBA_CMD<29> 3.4C
SNN_FBA_CMD<30> 3.4C
SNN_FBA_RFU<0> 3.4B
SNN_FBA_RFU<1> 3.4B
SNN_FBA_RFU<2> 3.4B
SNN_FBA_RFU<3> 3.4B
SNN_FBA_RFU<4> 3.4B
SNN_FBA_RFU<5> 3.4B
SNN_FBA_RFU<6> 3.4B
SNN_FBA_RFU<7> 3.5B
SNN_FBC0_CKE1 7.2A
SNN_FBC0_CS1 7.2A
SNN_FBC0_NC_A1 7.3A
SNN_FBC0_NC_A11 7.3A
SNN_FBC0_NC_T1 7.3A
SNN_FBC0_NC_T11 7.3A
SNN_FBC0_ODT1 7.2A
SNN_FBC0_ZQ1 7.2A
SNN_FBC1_CKE1 7.2C
SNN_FBC1_CS1 7.2C
SNN_FBC1_NC_A1 7.3C
SNN_FBC1_NC_A11 7.3C
SNN_FBC1_NC_T1 7.3C
SNN_FBC1_NC_T11 7.3C
SNN_FBC1_ODT1 7.2C
SNN_FBC1_ZQ1 7.2C
SNN_FBC2_CKE1 7.2E
SNN_FBC2_CS1 7.2E
SNN_FBC2_NC_A1 7.3E
SNN_FBC2_NC_A11 7.3E
SNN_FBC2_NC_T1 7.3E
SNN_FBC2_NC_T11 7.3E
SNN_FBC2_ODT1 7.2E
SNN_FBC2_ZQ1 7.2E
SNN_FBC3_CKE1 7.2G
SNN_FBC3_CS1 7.2G
SNN_FBC3_NC_A1 7.3G
SNN_FBC3_NC_A11 7.3G
SNN_FBC3_NC_T1 7.3G
SNN_FBC3_NC_T11 7.3G
SNN_FBC3_ODT1 7.2G
SNN_FBC3_ZQ1 7.2G
SNN_FBC_CMD<15> 6.3C
SNN_FBC_CMD<23> 6.4C
SNN_FBC_CMD<29> 6.4C
SNN_FBC_CMD<30> 6.4C
SNN_FBC_RFU1 6.5C
SNN_FBC_RFU2 6.5C
SNN_FBC_RFU<0> 6.4B
SNN_FBC_RFU<1> 6.4B
SNN_FBC_RFU<2> 6.4B
SNN_FBC_RFU<3> 6.4B
SNN_FBC_RFU<4> 6.4B
SNN_FBC_RFU<5> 6.5B
SNN_FBC_RFU<6> 6.5B
SNN_FBC_RFU<7> 6.5B
SNN_GND_SENSE_1 2.4E
SNN_GND_SENSE_3 2.4E
SNN_GPIO2 17.3C
SNN_GPIO3 17.3C
SNN_GPIO10 17.3C
SNN_GPIO11 17.3C
SNN_GPIO12 17.3C
SNN_GPIO14 17.4C
SNN_GPIO15 14.3E
SNN_GPIO17 17.4C
SNN_GPIO18 17.4C
SNN_GPIO19 13.3E
SNN_GPIO20 17.4C
SNN_GPIO21 14.4E
SNN_GPIO22 17.4C
SNN_GPIO23 17.4C
SNN_HDA_BCLK 18.4C
SNN_HDA_RST* 18.4C
SNN_HDA_SDI 18.4C
SNN_HDA_SDO 18.4C
SNN_HDA_SYNC 18.4C
SNN_HDMI_CEC 12.3G
SNN_HDMI_RSVD 12.3G
SNN_I2CD_SCL 17.3C

SNN_I2CD_SDA 17.3C
SNN_I2CE_SCL 17.3C
SNN_I2CE_SDA 17.3C
SNN_I2C_EN 12.3E
SNN_I2C_NC 12.2D
SNN_IFPA_TXD3 11.3D
SNN_IFPA_TXD3* 11.3D
SNN_IFPB_TXD7 11.3D
SNN_IFPB_TXD7* 11.3D
SNN_IFPD_AUX 13.3E
SNN_IFPD_AUX* 13.3E
SNN_IFPD_L0 13.3E
SNN_IFPD_L0* 13.3E
SNN_IFPD_L1 13.3E
SNN_IFPD_L1* 13.3E
SNN_IFPD_L2 13.3E
SNN_IFPD_L2* 13.3E
SNN_IFPD_L3 13.3E
SNN_IFPD_L3* 13.3E
SNN_IFPD_RSET 13.3C
SNN_IFPEF_RSET 14.3C
SNN_IFPE_AUX 14.2E
SNN_IFPE_AUX* 14.2E
SNN_IFPE_TXC 14.3E
SNN_IFPE_TXC* 14.2E
SNN_IFPE_TXD0 14.3E
SNN_IFPE_TXD0* 14.3E
SNN_IFPE_TXD1 14.3E
SNN_IFPE_TXD1* 14.3E
SNN_IFPE_TXD2 14.3E
SNN_IFPE_TXD2* 14.3E
SNN_IFPF_AUX 14.3E
SNN_IFPF_AUX* 14.3E
SNN_IFPF_TXC 14.3E
SNN_IFPF_TXC* 14.3E
SNN_IFPF_TXD0 14.3E
SNN_IFPF_TXD0* 14.3E
SNN_IFPF_TXD1 14.3E
SNN_IFPF_TXD1* 14.3E
SNN_IFPF_TXD2 14.4E
SNN_IFPF_TXD2* 14.4E
SNN_J25 18.3C
SNN_J26 18.3C
SNN_MIOACAL_PD_VDD 15.2B
Q
SNN_MIOACAL_PU_GND 15.2B
SNN_MIOAD<0> 15.1D
SNN_MIOAD<1> 15.1D
SNN_MIOAD<2> 15.1D
SNN_MIOAD<3> 15.2D
SNN_MIOAD<4> 15.2D
SNN_MIOAD<5> 15.2D
SNN_MIOAD<6> 15.2D
SNN_MIOAD<7> 15.2D
SNN_MIOAD<8> 15.2D
SNN_MIOAD<9> 15.2D
SNN_MIOAD<10> 15.2D
SNN_MIOAD<11> 15.2D
SNN_MIOAD<12> 15.2D
SNN_MIOAD<13> 15.2D
SNN_MIOAD<14> 15.2D
SNN_MIOAD_CTL3 15.2D
SNN_MIOA_CLKOUT 15.2D
SNN_MIOA_CLKOUT* 15.2D
SNN_MIOA_DE 15.2D
SNN_MIOA_HSYNC 15.2D
SNN_MIOA_VREF 15.2B
SNN_MIOA_VSYNC 15.2D
SNN_MIOB<0> 15.3D
SNN_MIOB<1> 15.3D
SNN_MIOB<2> 15.3D
SNN_MIOB<3> 15.3D
SNN_MIOB<4> 15.3D
SNN_MIOB<5> 15.4D
SNN_MIOB<6> 15.4D
SNN_MIOB<7> 15.4D
SNN_MIOB<8> 15.4D
SNN_MIOB<9> 15.4D
SNN_MIOB<10> 15.4D
SNN_MIOB<11> 15.4D
SNN_MIOBD<12> 15.4D
SNN_MIOBD<13> 15.4D
SNN_MIOBD<14> 15.4D
SNN_MIOB_CAL_PD_VD 15.4B
DQ
SNN_MIOB_CAL_PU_GN 15.4B
D
SNN_MIOB_CLKOUT 15.4D
SNN_MIOB_CLKOUT* 15.4D
SNN_MIOB_CTL3 15.4D
SNN_MIOB_DE 15.4D
SNN_MIOB_VREF 15.4B
SNN_MIOB_VSYNC 15.4D
SNN_NC<1> 2.2E
SNN_NC<2> 2.2E
SNN_NC<3> 2.2E

SNN_NC<4> 2.2E
SNN_NC<5> 2.3E
SNN_NC<6> 2.3E
SNN_NC<7> 2.3E
SNN_NC<8> 2.3E
SNN_NC<9> 2.3E
SNN_NC<10> 2.3E
SNN_NC<11> 2.3E
SNN_NC<14> 2.3E
SNN_NC<16> 2.3E
SNN_NC<17> 2.3E
SNN_NC<18> 2.3E
SNN_NC<21> 2.3E
SNN_NC<22> 2.3E
SNN_NC<23> 2.3E
SNN_PEX_RFU 2.5E
SNN_PEX_WAKE* 2.2B
SNN_PE_PRSNT2_A 2.1A
SNN_PE_PRSNT2_B 2.2A
SNN_PE_PRSNT2_C 2.3A
SNN_PE_RSVD2 2.2A
SNN_PE_RSVD3 2.2A
SNN_PE_RSVD4 2.2A
SNN_PE_RSVD5 2.2A
SNN_PE_RSVD6 2.3A
SNN_PE_RSVD7 2.4A
SNN_PE_RSVD8 2.4A
SNN_PGOOD_OUT* 18.4D
SNN_VDD_SENSE_1 2.4E
SNN_VDD_SENSE_3 2.4E
SNN_VGA_ID0 10.4G
SNN_VGA_ID0L 10.4G
SNN_VGA_ID2 10.4G
SNN_VGA_ID2L 10.5G
SPDIF_IN 18.4D
STRAP0 15.4E 18.2A
STRAP1 15.4E 18.2A
STRAP2 15.4E 18.2A
STRAP_REF0 18.4C
STRAP_REF1 18.4C
THERM_ALERT 17.2C
THERM_DA 17.3B
THERM_DC 17.3B
THERM_NPN 17.2E
THERM_OVERTMP* 17.2D
THERM_PNP 17.1E
THERM_THERM 17.2C
XTAL_IN 16.3C
XTAL_OUT 16.3D
XTAL_OUTBUFF 16.3D
XTAL_SSIN 16.3C

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Title: Basenet Report
Design: p681
Date: Jan 22 13:35:02 2009

Base nets and synonyms for
p681_lib.p681(@p681_lib.p681(sch_1))
Base Signal Location([Zone][dir])

1V1_ADJ 19.2B
1V1_PLLVDD 2.4G 3.5E 11.2A 16.3A
19.2C
1V8_ADJ 19.2F
3V3 2.1A
3V3_INFO 18.5F
5V 19.4C
5V_ADJ 19.4B
12V 2.1A
12V_D 19.4A
12V_F 21.1F
DACA_BLUE 9.4E 9.5A
DACA_BLUE_C 9.4H 9.5A 11.3G
DACA_GREEN 9.4E 9.5A
DACA_GREEN_C 9.4H 9.5A 11.3G
DACA_HSYNC 9.3C 9.5A
DACA_HSYNC_BUF 9.3E 9.5A
DACA_HSYNC_C 9.3H 9.5A 11.3G
DACA_HSYNC_R 9.3E 9.5A
DACA_RED 9.3E 9.5A
DACA_RED_C 9.3H 9.5A 11.3G
DACA_RSET 9.3B
DACA_VDD 9.2B
DACA_VREF 9.3B
DACA_VSYNC 9.3C 9.5A
DACA_VSYNC_BUF 9.2E 9.5A
DACA_VSYNC_C 9.2H 9.5A 11.3G
DACA_VSYNC_R 9.2E 9.5A
DACB_BLUE 10.4D 10.5A
DACB_BLUE_C 10.4F 10.5A
DACB_GREEN 10.4D 10.5A
DACB_GREEN_C 10.4F 10.5A
DACB_HSYNC 10.3C 10.5A
DACB_HSYNC_BUF 10.3E 10.5A
DACB_HSYNC_C 10.3G 10.5A
DACB_HSYNC_R 10.3E 10.5A
DACB_RED 10.3D 10.5A
DACB_RED_C 10.3F 10.5A
DACB_RSET 10.3B
DACB_VDD 10.2B
DACB_VREF 10.2B
DACB_VSYNC 10.3C 10.5A
DACB_VSYNC_BUF 10.2E 10.5A
DACB_VSYNC_C 10.2G 10.5A
DACB_VSYNC_R 10.2E 10.5A
DDC_5V 19.4D
FBA_CLK0 3.4D 4.2A 4.2C 4.5G
FBA_CLK0* 3.4D 4.2A 4.2C 4.5G
FBA_CLK1 3.4D 4.2D 4.2F 4.5G
FBA_CLK1* 3.4D 4.2D 4.2F 4.5G
FBA_CMD<0> 3.3C 3.4G 4.2A 4.2C
FBA_CMD<30..0> 3.3D 4.1A 4.1C 4.1D
4.1F 4.5G
FBA_CMD<1> 3.3C 3.4F 4.1A 4.1C
4.1E 4.1G
FBA_CMD<2> 3.3C 3.4G 4.1A 4.1C
FBA_CMD<3> 3.2G 3.3C 4.1A 4.1C
4.1E 4.1G
FBA_CMD<4> 3.1F 3.3C 4.1A 4.1C
4.1E 4.1G
FBA_CMD<5> 3.3C 3.3G 4.1A 4.1C
4.1E 4.1G
FBA_CMD<6> 3.1G 3.3C 4.1A 4.1C
4.1E 4.1G
FBA_CMD<7> 3.3C 3.4F 4.1A 4.1C
4.1E 4.1G
FBA_CMD<8> 3.3C 3.4F 4.1A 4.1C
4.1E 4.1G
FBA_CMD<9> 3.2F 3.3C 4.2A 4.2C
4.2E 4.2G
FBA_CMD<10> 3.2F 3.3C 4.1A 4.1C
4.1E 4.1G
FBA_CMD<11> 3.1F 3.3C 4.1E 4.1G
FBA_CMD<12> 3.1G 3.3C 4.2A 4.2C
4.2E 4.2G
FBA_CMD<13> 3.3C 3.3G 4.2A 4.2C
4.2E 4.2G
FBA_CMD<14> 3.3C 3.3F 4.1A 4.1C
4.1E 4.1G
FBA_CMD<16> 3.3C 3.4G 4.2E 4.2G
FBA_CMD<17> 3.3C 3.3G 4.1A 4.1C
4.1E 4.1G
FBA_CMD<19> 3.2G 3.3C 4.1A 4.1C
4.1E 4.1G
FBA_CMD<20> 3.3F 3.4C 4.1A 4.1C
4.1E 4.1G

FBA_CMD<21> 3.2G 3.4C 4.1A 4.1C
4.1E 4.1G
FBA_CMD<22> 3.4C 3.4F 4.1E 4.1G
4.2A 4.2C
FBA_CMD<24> 3.3F 3.4C 4.1A 4.1C
4.1E 4.1G
FBA_CMD<25> 3.4C 3.4G 4.3A 4.3C
FBA_CMD<26> 3.2F 3.4C 4.1A 4.1C
4.1E 4.1G
FBA_CMD<27> 3.4C 3.4G 4.2E 4.2G
FBA_CMD<28> 3.4C 4.2E 4.2G 4.3A
4.3C
FBA_D<0> 3.1B 4.3B
FBA_D<63..0> 3.1A 4.3A 4.5G
FBA_D<1> 3.1B 4.3B
FBA_D<2> 3.1B 4.4B
FBA_D<3> 3.1B 4.4B
FBA_D<4> 3.1B 4.4B
FBA_D<5> 3.1B 4.4B
FBA_D<6> 3.1B 4.4B
FBA_D<7> 3.1B 4.4B
FBA_D<8> 3.1B 4.4B
FBA_D<9> 3.1B 4.4B
FBA_D<10> 3.1B 4.4B
FBA_D<11> 3.1B 4.4B
FBA_D<12> 3.2B 4.4B
FBA_D<13> 3.2B 4.4B
FBA_D<14> 3.2B 4.4B
FBA_D<15> 3.2B 4.4B
FBA_D<16> 3.2B 4.3C
FBA_D<17> 3.2B 4.3C
FBA_D<18> 3.2B 4.4C
FBA_D<19> 3.2B 4.4C
FBA_D<20> 3.2B 4.4C
FBA_D<21> 3.2B 4.4C
FBA_D<22> 3.2B 4.4C
FBA_D<23> 3.2B 4.4C
FBA_D<24> 3.2B 4.4C
FBA_D<25> 3.2B 4.4C
FBA_D<26> 3.2B 4.4C
FBA_D<27> 3.2B 4.4C
FBA_D<28> 3.2B 4.4C
FBA_D<29> 3.2B 4.4C
FBA_D<30> 3.2B 4.4C
FBA_D<31> 3.2B 4.3D
FBA_D<32> 3.2B 4.3D
FBA_D<33> 3.2B 4.3D
FBA_D<34> 3.2B 4.4D
FBA_D<35> 3.2B 4.4D
FBA_D<36> 3.2B 4.4D
FBA_D<37> 3.2B 4.4D
FBA_D<38> 3.2B 4.4D
FBA_D<39> 3.2B 4.4D
FBA_D<40> 3.2B 4.4D
FBA_D<41> 3.2B 4.4D
FBA_D<42> 3.3B 4.4D
FBA_D<43> 3.3B 4.4D
FBA_D<44> 3.3B 4.4D
FBA_D<45> 3.3B 4.4D
FBA_D<46> 3.3B 4.4D
FBA_D<47> 3.3B 4.4D
FBA_D<48> 3.3B 4.3E
FBA_D<49> 3.3B 4.3E
FBA_D<50> 3.3B 4.4E
FBA_D<51> 3.3B 4.4E
FBA_D<52> 3.3B 4.4E
FBA_D<53> 3.3B 4.4E
FBA_D<54> 3.3B 4.4E
FBA_D<55> 3.3B 4.4E
FBA_D<56> 3.3B 4.4E
FBA_D<57> 3.3B 4.4E
FBA_D<58> 3.3B 4.4E
FBA_D<59> 3.3B 4.4E
FBA_D<60> 3.3B 4.4E
FBA_D<61> 3.3B 4.4E
FBA_D<62> 3.3B 4.4E
FBA_D<63> 3.3B 4.4E
FBA_DEBUG 3.4C
FBA_DQM<0> 3.3B 4.4B
FBA_DQM<7..0> 3.3A 4.3A 4.5G
FBA_DQM<1> 3.3B 4.4B
FBA_DQM<2> 3.3B 4.4C
FBA_DQM<3> 3.3B 4.4C
FBA_DQM<4> 3.3B 4.4D
FBA_DQM<5> 3.3B 4.4D
FBA_DQM<6> 3.4B 4.4E
FBA_DQM<7> 3.4B 4.4E
FBA_DQS<0> 3.4B 4.4B 4.5E
FBA_DQS<7..0> 3.4A 4.3A 4.5E
FBA_DQS<1> 3.4B 4.4B 4.5E
FBA_DQS<2> 3.4B 4.4C 4.5E
FBA_DQS<3> 3.4B 4.4C 4.5E
FBA_DQS<4> 3.4B 4.4D 4.5E
FBA_DQS<5> 3.4B 4.4D 4.5E
FBA_DQS<6> 3.4B 4.4E 4.5E
FBA_DQS<7> 3.4B 4.4E 4.5E

FBA_DQSN<0> 3.4B 4.4B 4.5E
FBA_DQSN<7..0> 3.4A 4.3A 4.5E
FBA_DQSN<1> 3.4B 4.4B 4.5E
FBA_DQSN<2> 3.4B 4.4C 4.5E
FBA_DQSN<3> 3.4B 4.4C 4.5E
FBA_DQSN<4> 3.4B 4.4D 4.5E
FBA_DQSN<5> 3.4B 4.4D 4.5E
FBA_DQSN<6> 3.4B 4.4E 4.5E
FBA_DQSN<7> 3.4B 4.4E 4.5E
FBA_VREF 3.5B
FBA_VREF0 4.3C 4.3E 4.4G
FBA_VREF1 4.3F 4.3H 4.4H
FBA_ZQ0 4.3A
FBA_ZQ1 4.3C
FBA_ZQ2 4.3E
FBA_ZQ3 4.3G
FBC_CLK0 6.4D 7.2A 7.2C 7.5G
FBC_CLK0* 6.4D 7.3A 7.2C 7.5G
FBC_CLK1 6.4D 7.2D 7.2F 7.5G
FBC_CLK1* 6.4D 7.2D 7.2F 7.5G
FBC_CMD<0> 6.3C 6.4G 7.2A 7.2C
FBC_CMD<30..0> 6.3D 7.1A 7.1C 7.1D
7.1F 7.5G
FBC_CMD<1> 6.2F 6.3C 7.1A 7.1C
7.1E 7.1G
FBC_CMD<2> 6.1G 6.3C 7.1A 7.1C
FBC_CMD<3> 6.2G 6.3C 7.1A 7.1C
7.1E 7.1G
FBC_CMD<4> 6.2G 6.3C 7.1A 7.1C
7.1E 7.1G
FBC_CMD<5> 6.3C 6.4G 7.1A 7.1C
7.1E 7.1G
FBC_CMD<6> 6.3C 6.4F 7.1A 7.1C
7.1E 7.1G
FBC_CMD<7> 6.3C 6.3G 7.1A 7.1C
7.1E 7.1G
FBC_CMD<8> 6.3C 6.4F 7.1A 7.1C
7.1E 7.1G
FBC_CMD<9> 6.3C 6.3F 7.2A 7.2C
7.2E 7.2G
FBC_CMD<10> 6.3C 6.3G 7.1A 7.1C
7.1E 7.1G
FBC_CMD<11> 6.3C 6.4F 7.1E 7.1G
FBC_CMD<12> 6.3C 6.4G 7.2A 7.2C
7.2E 7.2G
FBC_CMD<13> 6.3C 6.3F 7.2A 7.2C
7.2E 7.2G
FBC_CMD<14> 6.1G 6.3C 7.1A 7.1C
7.1E 7.1G
FBC_CMD<16> 6.3C 6.4G 7.2E 7.2G
FBC_CMD<17> 6.3C 6.3G 7.1A 7.1C
7.1E 7.1G
FBC_CMD<18> 6.1F 6.3C 7.1E 7.1G
7.2A 7.2C
FBC_CMD<19> 6.3C 6.4F 7.1A 7.1C
7.1E 7.1G
FBC_CMD<20> 6.3F 6.4C 7.1A 7.1C
7.1E 7.1G
FBC_CMD<21> 6.3G 6.4C 7.1A 7.1C
7.1E 7.1G
FBC_CMD<22> 6.1F 6.4C 7.1E 7.1G
7.2A 7.2C
FBC_CMD<24> 6.2F 6.4C 7.1A 7.1C
7.1E 7.1G
FBC_CMD<25> 6.4C 6.4G 7.3A 7.3C
FBC_CMD<26> 6.2F 6.4C 7.1A 7.1C
7.1E 7.1G
FBC_CMD<27> 6.4C 6.4G 7.2E 7.2G
FBC_CMD<28> 6.4C 7.2E 7.2G 7.3A
7.3C
FBC_D<0> 6.1B 7.3B
FBC_D<63..0> 6.1A 7.3A 7.5G
FBC_D<1> 6.1B 7.4B
FBC_D<2> 6.1B 7.4B
FBC_D<3> 6.1B 7.4B
FBC_D<4> 6.1B 7.4B
FBC_D<5> 6.1B 7.4B
FBC_D<6> 6.1B 7.4B
FBC_D<7> 6.1B 7.4B
FBC_D<8> 6.1B 7.4B
FBC_D<9> 6.1B 7.4B
FBC_D<10> 6.1B 7.4B
FBC_D<11> 6.1B 7.4B
FBC_D<12> 6.2B 7.4B
FBC_D<13> 6.2B 7.4B
FBC_D<14> 6.2B 7.4B
FBC_D<15> 6.2B 7.4B
FBC_D<16> 6.2B 7.3C
FBC_D<17> 6.2B 7.4C
FBC_D<18> 6.2B 7.4C
FBC_D<19> 6.2B 7.4C
FBC_D<20> 6.2B 7.4C
FBC_D<21> 6.2B 7.4C
FBC_D<22> 6.2B 7.4C
FBC_D<23> 6.2B 7.4C
FBC_D<24> 6.2B 7.4C

FBC_D<25> 6.2B 7.4C
FBC_D<26> 6.2B 7.4C
FBC_D<27> 6.2B 7.4C
FBC_D<28> 6.2B 7.4C
FBC_D<29> 6.2B 7.4C
FBC_D<30> 6.2B 7.4C
FBC_D<31> 6.2B 7.4C
FBC_D<32> 6.2B 7.3D
FBC_D<33> 6.2B 7.4D
FBC_D<34> 6.2B 7.4D
FBC_D<35> 6.2B 7.4D
FBC_D<36> 6.2B 7.4D
FBC_D<37> 6.2B 7.4D
FBC_D<38> 6.2B 7.4D
FBC_D<39> 6.2B 7.4D
FBC_D<40> 6.2B 7.4D
FBC_D<41> 6.2B 7.4D
FBC_D<42> 6.3B 7.4D
FBC_D<43> 6.3B 7.4D
FBC_D<44> 6.3B 7.4D
FBC_D<45> 6.3B 7.4D
FBC_D<46> 6.3B 7.4D
FBC_D<47> 6.3B 7.4D
FBC_D<48> 6.3B 7.3E
FBC_D<49> 6.3B 7.4E
FBC_D<50> 6.3B 7.4E
FBC_D<51> 6.3B 7.4E
FBC_D<52> 6.3B 7.4E
FBC_D<53> 6.3B 7.4E
FBC_D<54> 6.3B 7.4E
FBC_D<55> 6.3B 7.4E
FBC_D<56> 6.3B 7.4E
FBC_D<57> 6.3B 7.4E
FBC_D<58> 6.3B 7.4E
FBC_D<59> 6.3B 7.4E
FBC_D<60> 6.3B 7.4E
FBC_D<61> 6.3B 7.4E
FBC_D<62> 6.3B 7.4E
FBC_D<63> 6.3B 7.4E
FBC_DEBUG 6.4C
FBC_DQM<0> 6.3B 7.4B
FBC_DQM<7..0> 6.3A 7.3A 7.5G
FBC_DQM<1> 6.3B 7.4B
FBC_DQM<2> 6.3B 7.4C
FBC_DQM<3> 6.3B 7.4C
FBC_DQM<4> 6.3B 7.4D
FBC_DQM<5> 6.3B 7.4D
FBC_DQM<6> 6.4B 7.4E
FBC_DQM<7> 6.4B 7.4E
FBC_DQS<0> 6.4B 7.4B 7.5E
FBC_DQS<7..0> 6.4A 7.3A 7.5E
FBC_DQS<1> 6.4B 7.4B 7.5E
FBC_DQS<2> 6.4B 7.4C 7.5E
FBC_DQS<3> 6.4B 7.4C 7.5E
FBC_DQS<4> 6.4B 7.4D 7.5E
FBC_DQS<5> 6.4B 7.4D 7.5E
FBC_DQS<6> 6.4B 7.4E 7.5E
FBC_DQS<7> 6.4B 7.4E 7.5E
FBC_DQSN<0> 6.4B 7.4B 7.5E
FBC_DQSN<7..0> 6.4A 7.3A 7.5E
FBC_DQSN<1> 6.4B 7.4B 7.5E
FBC_DQSN<2> 6.4B 7.4C 7.5E
FBC_DQSN<3> 6.4B 7.4C 7.5E
FBC_DQSN<4> 6.4B 7.4D 7.5E
FBC_DQSN<5> 6.4B 7.4D 7.5E
FBC_DQSN<6> 6.4B 7.4E 7.5E
FBC_DQSN<7> 6.4B 7.4E 7.5E
FBC_VREF0 7.3C 7.3E 7.4G
FBC_VREF1 7.3F 7.3H 7.4H
FBC_ZQ0 7.3A
FBC_ZQ1 7.3C
FBC_ZQ2 7.3E
FBC_ZQ3 7.3G
FBVDDQ 20.2H
FBVDDQ_RBOT 20.4F
FBVDDQ_VSEL 20.4E
FB_CAL_PD_VDDQ 6.5C
FB_CAL_PU_GND 6.5C
FB_CAL_TERM_GND 6.5C
FB_PLLAVDD 3.5C
GPIO0_HPD_DVI 11.4D
GPIO0_HPD_DVI_Q 11.4D
GPIO0_HPD_DVI_R 11.4E
GPIO0_HPD_DVI_RL 11.3G
GPIO1_HPDC 12.4C
GPIO1_HPDC_Q 12.4D
GPIO1_HPDC_R 12.4F
GPIO1_HPDC_R_L 12.4G
GPIO4_FAN_TACH 17.3C
GPIO5_NVVDD_VSEL1 17.3D 21.1A 21.3A
GPIO6_NVVDD_VSEL2 17.3D 21.3A
GPIO7_NVVDD_VSEL3 17.3D 21.2A 21.4A
GPIO8_THERM_OVERTM 17.3C
I²
GPIO9_FAN_PWM 17.3C
GPIO9_FAN_PWM_Q 17.4F

GPIO9_FAN_PWM_Q_L 17.4G
GPIO9_FAN_PWM_R 17.3F
GPIO13_FBVDDQ_VSEL 17.4D 20.4D
GPIO16_FAN_PWM 17.4C
GPU_PLLVDD 16.3B
GPU_TESTMODE 2.5E
HDMI_PD_1 12.4B
I2CA_SCL 9.2C 9.2D
I2CA_SCL_C 9.2H 11.3G
I2CA_SCL_T 9.2F
I2CA_SDA 9.1D 9.2C
I2CA_SDA_C 9.1H 11.3G
I2CA_SDA_T 9.1F
I2CB_SCL 10.2C
I2CB_SCL_R 10.1E
I2CB_SCL_R_L 10.1G
I2CB_SDA 10.2C
I2CB_SDA_R 10.1E
I2CB_SDA_R_L 10.1G
I2CC_SCL 17.2B 17.3F 18.5E
I2CC_SCL_G 17.3C
I2CC_SDA 17.2B 17.3F 18.5E
I2CC_SDA_G 17.3C
I2CH_SCL 18.4D
I2CH_SDA 18.4D
I2CS_SCL 2.1C 17.3F
I2CS_SDA 2.2C 17.3F
I2CW_SCL 12.3C
I2CW_SCL_R 12.2D
I2CW_SCL_R_Q 12.2E
I2CW_SDA 12.3C
I2CW_SDA_R 12.1D
I2CW_SDA_R_Q 12.1E
IFPAB_IOVDD 11.3B
IFPAB_PLLVDD 11.2B
IFPAB_RSET 11.3B
IFPA_TXC 11.3D
IFPA_TXC* 11.3D
IFPA_TXD0 11.2D
IFPA_TXD0* 11.2D
IFPA_TXD1 11.2D
IFPA_TXD1* 11.2D
IFPA_TXD2 11.3D
IFPA_TXD2* 11.2D
IFPB_TXD4 11.3D
IFPB_TXD4* 11.3D
IFPB_TXD5 11.3D
IFPB_TXD5* 11.3D
IFPB_TXD6 11.3D
IFPB_TXD6* 11.3D
IFPCEF_PLLVDD 14.3C
IFPC_IOVDD 12.3A
IFPC_PLLVDD 12.3A
IFPC_RSET 12.3A
IFPC_TXC 12.3D
IFPC_TXC* 12.3D
IFPC_TXC_C1 12.3F 12.4B
IFPC_TXC_C1* 12.3F 12.4B
IFPC_TXD0 12.3D
IFPC_TXD0* 12.3D
IFPC_TXD0_C1 12.3F 12.4B
IFPC_TXD0_C1* 12.3F 12.4B
IFPC_TXD1 12.3D
IFPC_TXD1* 12.3D
IFPC_TXD1_C1 12.3F 12.4B
IFPC_TXD1_C1* 12.3F 12.4B
IFPC_TXD2 12.3D
IFPC_TXD2* 12.3D
IFPC_TXD2_C1 12.3F 12.4B
IFPC_TXD2_C1* 12.3F 12.4B
IFPD_IOVDD 13.3C
IFPD_PLLVDD 13.3C
IFPEF_IOVDD 14.3C
IFP_IOVDD_EN* 17.2E 19.4G
IFP_IOVDD_EN_RC 19.4F
IFP_PLLVDD 12.2A 19.2G
JTAG_TCLK 2.1C 17.4A
JTAG_TDI 2.1C 17.4A
JTAG_TDO 2.1C 17.5A
JTAG_TMS 2.1C 17.4A
JTAG_TRST* 2.1C 17.5A
MIOA_CLKIN 15.2D
MIOA_VDDQ 15.1C
MIOB_CLKIN 15.4D
NVVDD 21.2H
NVVDD_CP 21.3C
NVVDD_CP_RC 21.4D
NVVDD_CSN 21.3D
NVVDD_CSN_R 21.3D
NVVDD_CSP 21.3D
NVVDD_EAP 21.3C
NVVDD_EN 17.2F 21.2A
NVVDD_EN* 17.1E
NVVDD_FB 21.4D
NVVDD_FB_RC 21.4D
NVVDD_GND_SENSE 2.4F 21.4B

NVVDD_GND_SENSE_R 21.2B 21.4C
NVVDD_IOFS 21.2C
NVVDD_MODE 21.2C
NVVDD_MODE_Q 21.1B
NVVDD_MODE_R 21.2B
NVVDD_REFIN 21.3C
NVVDD_RSET 21.3C
NVVDD_SENSE 2.4F 21.4D
NVVDD_SENSE_R 21.4E
NVVDD_SS 21.3C
NVVDD_VID 21.3C
NVVDD_VREF 21.3C
NVVDD_VSEL2 21.3B
NVVDD_VSEL2_Q 21.3B
NVVDD_VSEL3 21.4B
NVVDD_VSEL3_Q 21.3C
PEX_CLKREQ* 2.1C
PEX_PLLVDD 2.4E
PEX_PLL_CLK_OUT 2.2C
PEX_PLL_CLK_OUT* 2.2C
PEX_PRSNT1* 2.1A
PEX_REFCLK 2.1G 2.2B
PEX_REFCLK* 2.1G 2.2B
PEX_RST* 2.2D 19.4E
PEX_RX0 2.2B 2.4G
PEX_RX0* 2.2B 2.4G
PEX_RX1 2.2B 2.4G
PEX_RX1* 2.2B 2.4G
PEX_RX2 2.2B 2.4G
PEX_RX2* 2.3B 2.4G
PEX_RX3 2.3B 2.4G
PEX_RX3* 2.3B 2.4G
PEX_RX4 2.3B 2.4G
PEX_RX4* 2.3B 2.4G
PEX_RX5 2.3B 2.4G
PEX_RX5* 2.3B 2.4G
PEX_RX6 2.3B 2.4G
PEX_RX6* 2.3B 2.4G
PEX_RX7 2.3B 2.4G
PEX_RX7* 2.4B 2.4G
PEX_RX8 2.4B 2.4G
PEX_RX8* 2.4B 2.4G
PEX_RX9 2.4B 2.4G
PEX_RX9* 2.4B 2.4G
PEX_RX10 2.4B 2.4G
PEX_RX10* 2.4B 2.4G
PEX_RX11 2.4B 2.4G
PEX_RX11* 2.4B 2.4G
PEX_RX12 2.4B 2.5G
PEX_RX12* 2.5B 2.5G
PEX_RX13 2.5B 2.5G
PEX_RX13* 2.5B 2.5G
PEX_RX14 2.5B 2.5G
PEX_RX14* 2.5B 2.5G
PEX_RX15 2.5B 2.5G
PEX_RX15* 2.5B 2.5G
PEX_SMCLK 2.1B
PEX_SMDAT 2.1B
PEX_TCLK 2.1B
PEX_TDI 2.1B
PEX_TDO 2.1B
PEX_TERMP 2.5E
PEX_TMS 2.1B
PEX_TRST* 2.1B
PEX_TX0 2.1G 2.2D
PEX_TX0* 2.1G 2.2D
PEX_TX1 2.1G 2.2D
PEX_TX1* 2.1G 2.2D
PEX_TX2 2.2B 2.2G
PEX_TX2* 2.2D 2.2G
PEX_TX3 2.2G 2.3D
PEX_TX3* 2.2G 2.3D
PEX_TX4 2.2G 2.3D
PEX_TX4* 2.2G 2.3D
PEX_TX5 2.2G 2.3D
PEX_TX5* 2.2G 2.3D
PEX_TX6 2.2G 2.3D
PEX_TX6* 2.2G 2.3D
PEX_TX7 2.2G 2.3D
PEX_TX7* 2.2G 2.3D
PEX_TX8 2.2G 2.4D
PEX_TX8* 2.2G 2.4D
PEX_TX9 2.2G 2.4D
PEX_TX9* 2.2G 2.4D
PEX_TX10 2.2G 2.4D
PEX_TX10* 2.2G 2.4D
PEX_TX11 2.2G 2.4D
PEX_TX11* 2.2G 2.4D
PEX_TX12 2.2G 2.4D
PEX_TX12* 2.2G 2.4D
PEX_TX13 2.2G 2.5D
PEX_TX13* 2.2G 2.5D
PEX_TX14 2.2G 2.5D
PEX_TX14* 2.2G 2.5D
PEX_TX15 2.2G 2.5D
PEX_TX15* 2.2G 2.5D

PEX_TX0 2.2B 2.3G
PEX_TX0* 2.2B 2.3G
PEX_TX1 2.2B 2.3G
PEX_TX1* 2.2B 2.3G
PEX_TX2 2.2B 2.3G
PEX_TX2* 2.2B 2.3G
PEX_TX3 2.3B 2.3G
PEX_TX3* 2.3B 2.3G
PEX_TX4 2.3B 2.3G
PEX_TX4* 2.3B 2.3G
PEX_TX5 2.3B 2.3G
PEX_TX5* 2.3B 2.3G
PEX_TX6 2.3B 2.3G
PEX_TX6* 2.3B 2.3G
PEX_TX7 2.3B 2.3G
PEX_TX7* 2.3B 2.3G
PEX_TX8 2.3G 2.4B
PEX_TX8* 2.3G 2.4B
PEX_TX9 2.3G 2.4B
PEX_TX9* 2.3G 2.4B
PEX_TX10 2.3G 2.4B
PEX_TX10* 2.3G 2.4B
PEX_TX11 2.3G 2.4B
PEX_TX11* 2.3G 2.4B
PEX_TX12 2.3G 2.4B
PEX_TX12* 2.3G 2.4B
PEX_TX13 2.3G 2.5B
PEX_TX13* 2.3G 2.5B
PEX_TX14 2.3G 2.5B
PEX_TX14* 2.4G 2.5B
PEX_TX15 2.4G 2.5B
PEX_TX15* 2.4G 2.5B
PEX_VDD 20.3B
PS_1V1_CP 20.3B
PS_1V1_DR 20.2C
PS_1V1_FB 20.3C
PS_FBVDDQ_BOOT 20.2D
PS_FBVDDQ_CP 20.3D
PS_FBVDDQ_CP_RC 20.3D
PS_FBVDDQ_EN 20.4B
PS_FBVDDQ_EN* 20.4C
PS_FBVDDQ_FB 20.3D
PS_FBVDDQ_FB_RC 20.4G
PS_FBVDDQ_FS_DIS 20.3C
PS_FBVDDQ_LG 20.3D
PS_FBVDDQ_PH 20.3D
PS_FBVDDQ_PVCC 20.2D
PS_FBVDDQ_PVCC_R 20.2C
PS_FBVDDQ_RC 20.2F
PS_FBVDDQ_UG 20.2D
PS_FBVDDQ_UG_R 20.2E
PS_FBVDDQ_VCC 20.2D
PS_NVVDD_BOOT1 21.2D
PS_NVVDD_BOOT2 21.3D
PS_NVVDD_EN 21.2C
PS_NVVDD_EN* 21.2B
PS_NVVDD_LG1 21.2D
PS_NVVDD_LG2 21.3D
PS_NVVDD_PH1 21.2D
PS_NVVDD_PH2 21.3D
PS_NVVDD_RC1 21.2F
PS_NVVDD_RC2 21.3F
PS_NVVDD_UG1 21.2D
PS_NVVDD_UG1_R 21.2E
PS_NVVDD_UG2 21.3D
PS_NVVDD_UG2_R 21.3E
PS_NVVDD_VCC9 21.2C
PS_NVVDD_VCC12 21.2C
ROM_CS* 18.3D
ROM_SCLK 18.2C 18.3D 18.3D
ROM_SI 18.2C 18.3D 18.3D
ROM_SO 18.2C 18.3D 18.3D
SNN_3V3AUX 2.1A
SNN_BIOB_HSYNC 15.4D
SNN_BTXC 11.3D
SNN_BTXC* 11.3D
SNN_BURST* 18.4D
SNN_CEC 18.4C
SNN_FBA0_CKE1 4.2A
SNN_FBA0_CS1 4.2A
SNN_FBA0_NC_A1 4.3A
SNN_FBA0_NC_A11 4.3A
SNN_FBA0_NC_T1 4.3A
SNN_FBA0_NC_T11 4.3A
SNN_FBA0_ODT1 4.2A
SNN_FBA0_ZQ1 4.2A
SNN_FBA1_CKE1 4.2C
SNN_FBA1_CS1 4.2C
SNN_FBA1_NC_A1 4.3C
SNN_FBA1_NC_A11 4.3C
SNN_FBA1_NC_T1 4.3C
SNN_FBA1_NC_T11 4.3C
SNN_FBA1_ODT1 4.2C
SNN_FBA1_ZQ1 4.2C
SNN_FBA2_CKE1 4.2E
SNN_FBA2_CS1 4.2E

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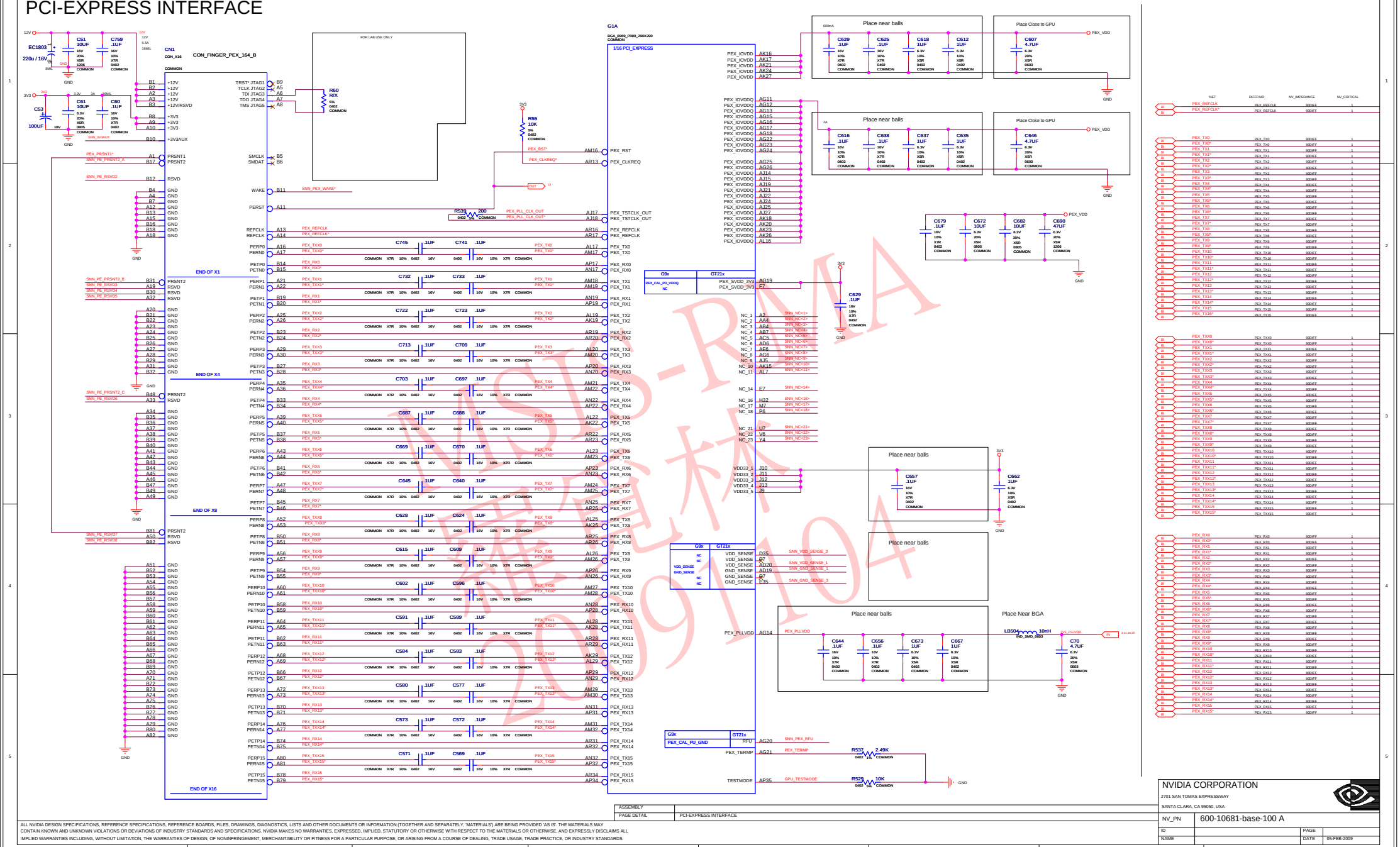
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10681-base-100 A		
ID		PAGE	
NAME	<ENGINEER>	DATE	05-FEB-2009

PCI-EXPRESS INTERFACE



NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL
PEX_REFCLK	PEX_REFCLK	90DIFF	1
PEX_REFCLK*	PEX_REFCLK	90DIFF	1
PEX_TX0	PEX_TX0	90DIFF	1
PEX_TX0*	PEX_TX0	90DIFF	1
PEX_TX1	PEX_TX1	90DIFF	1
PEX_TX1*	PEX_TX1	90DIFF	1
PEX_TX2	PEX_TX2	90DIFF	1
PEX_TX2*	PEX_TX2	90DIFF	1
PEX_TX3	PEX_TX3	90DIFF	1
PEX_TX3*	PEX_TX3	90DIFF	1
PEX_TX4	PEX_TX4	90DIFF	1
PEX_TX4*	PEX_TX4	90DIFF	1
PEX_TX5	PEX_TX5	90DIFF	1
PEX_TX5*	PEX_TX5	90DIFF	1
PEX_TX6	PEX_TX6	90DIFF	1
PEX_TX6*	PEX_TX6	90DIFF	1
PEX_TX7	PEX_TX7	90DIFF	1
PEX_TX7*	PEX_TX7	90DIFF	1
PEX_TX8	PEX_TX8	90DIFF	1
PEX_TX8*	PEX_TX8	90DIFF	1
PEX_TX9	PEX_TX9	90DIFF	1
PEX_TX9*	PEX_TX9	90DIFF	1
PEX_TX10	PEX_TX10	90DIFF	1
PEX_TX10*	PEX_TX10	90DIFF	1
PEX_TX11	PEX_TX11	90DIFF	1
PEX_TX11*	PEX_TX11	90DIFF	1
PEX_TX12	PEX_TX12	90DIFF	1
PEX_TX12*	PEX_TX12	90DIFF	1
PEX_TX13	PEX_TX13	90DIFF	1
PEX_TX13*	PEX_TX13	90DIFF	1
PEX_TX14	PEX_TX14	90DIFF	1
PEX_TX14*	PEX_TX14	90DIFF	1
PEX_TX15	PEX_TX15	90DIFF	1
PEX_TX15*	PEX_TX15	90DIFF	1
PEX_TX0	PEX_TX0	90DIFF	1
PEX_TX0*	PEX_TX0	90DIFF	1
PEX_TX1	PEX_TX1	90DIFF	1
PEX_TX1*	PEX_TX1	90DIFF	1
PEX_TX2	PEX_TX2	90DIFF	1
PEX_TX2*	PEX_TX2	90DIFF	1
PEX_TX3	PEX_TX3	90DIFF	1
PEX_TX3*	PEX_TX3	90DIFF	1
PEX_TX4	PEX_TX4	90DIFF	1
PEX_TX4*	PEX_TX4	90DIFF	1
PEX_TX5	PEX_TX5	90DIFF	1
PEX_TX5*	PEX_TX5	90DIFF	1
PEX_TX6	PEX_TX6	90DIFF	1
PEX_TX6*	PEX_TX6	90DIFF	1
PEX_TX7	PEX_TX7	90DIFF	1
PEX_TX7*	PEX_TX7	90DIFF	1
PEX_TX8	PEX_TX8	90DIFF	1
PEX_TX8*	PEX_TX8	90DIFF	1
PEX_TX9	PEX_TX9	90DIFF	1
PEX_TX9*	PEX_TX9	90DIFF	1
PEX_TX10	PEX_TX10	90DIFF	1
PEX_TX10*	PEX_TX10	90DIFF	1
PEX_TX11	PEX_TX11	90DIFF	1
PEX_TX11*	PEX_TX11	90DIFF	1
PEX_TX12	PEX_TX12	90DIFF	1
PEX_TX12*	PEX_TX12	90DIFF	1
PEX_TX13	PEX_TX13	90DIFF	1
PEX_TX13*	PEX_TX13	90DIFF	1
PEX_TX14	PEX_TX14	90DIFF	1
PEX_TX14*	PEX_TX14	90DIFF	1
PEX_TX15	PEX_TX15	90DIFF	1
PEX_TX15*	PEX_TX15	90DIFF	1
PEX_RX0	PEX_RX0	90DIFF	1
PEX_RX0*	PEX_RX0	90DIFF	1
PEX_RX1	PEX_RX1	90DIFF	1
PEX_RX1*	PEX_RX1	90DIFF	1
PEX_RX2	PEX_RX2	90DIFF	1
PEX_RX2*	PEX_RX2	90DIFF	1
PEX_RX3	PEX_RX3	90DIFF	1
PEX_RX3*	PEX_RX3	90DIFF	1
PEX_RX4	PEX_RX4	90DIFF	1
PEX_RX4*	PEX_RX4	90DIFF	1
PEX_RX5	PEX_RX5	90DIFF	1
PEX_RX5*	PEX_RX5	90DIFF	1
PEX_RX6	PEX_RX6	90DIFF	1
PEX_RX6*	PEX_RX6	90DIFF	1
PEX_RX7	PEX_RX7	90DIFF	1
PEX_RX7*	PEX_RX7	90DIFF	1
PEX_RX8	PEX_RX8	90DIFF	1
PEX_RX8*	PEX_RX8	90DIFF	1
PEX_RX9	PEX_RX9	90DIFF	1
PEX_RX9*	PEX_RX9	90DIFF	1
PEX_RX10	PEX_RX10	90DIFF	1
PEX_RX10*	PEX_RX10	90DIFF	1
PEX_RX11	PEX_RX11	90DIFF	1
PEX_RX11*	PEX_RX11	90DIFF	1
PEX_RX12	PEX_RX12	90DIFF	1
PEX_RX12*	PEX_RX12	90DIFF	1
PEX_RX13	PEX_RX13	90DIFF	1
PEX_RX13*	PEX_RX13	90DIFF	1
PEX_RX14	PEX_RX14	90DIFF	1
PEX_RX14*	PEX_RX14	90DIFF	1
PEX_RX15	PEX_RX15	90DIFF	1
PEX_RX15*	PEX_RX15	90DIFF	1

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NV_PN	600-10681-base-100 A		
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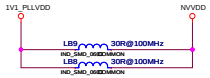
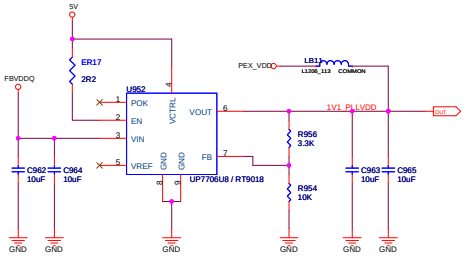
NAME		DATE	05-FEB-2009

WSD-RMA 2009104

LINEAR POWER SUPPLIES

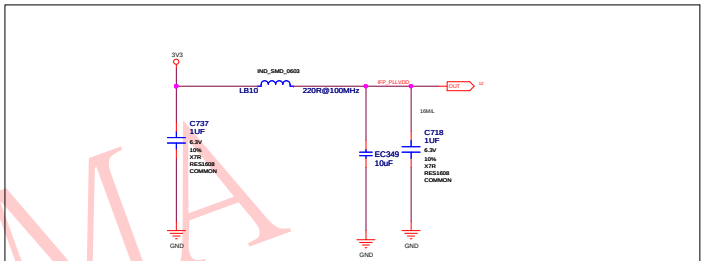


PEX_PLLVDD SUPPLY (OPTIAN)



Vout=0.8V * (1+ R956 / R954)

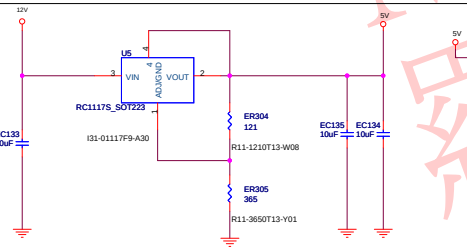
IFP_PLLVDD SUPPLY



VOUT = Vref * (1 + Rbot / Rtop)

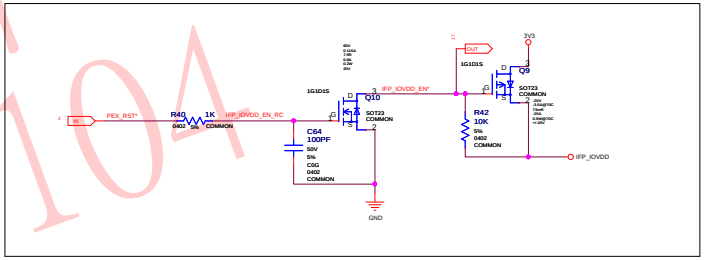
1.793V = 0.8V * (1 + 1k / 0.806k)

5V & DDC_5V REGULATOR



Vout=1.25V* [1+(ER305/ER304)]

IFP_IOVDD BACKDRIVE PREVENTION



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINEAR POWER SUPPLIES

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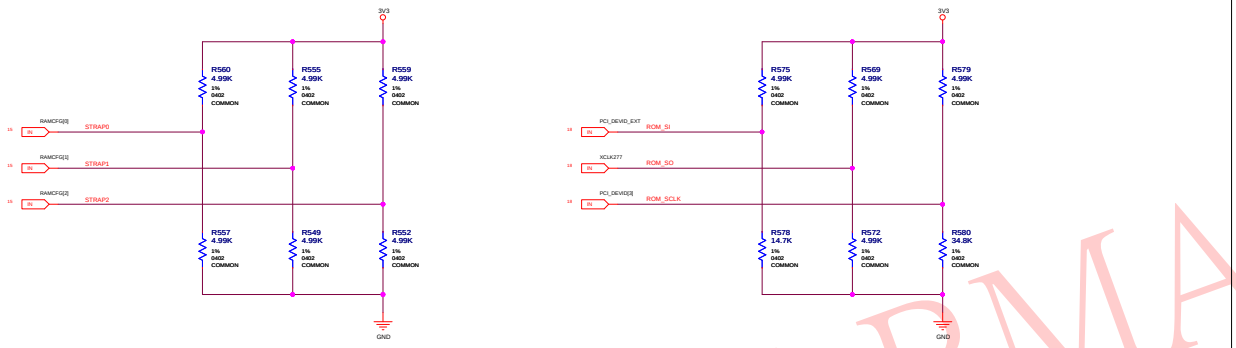
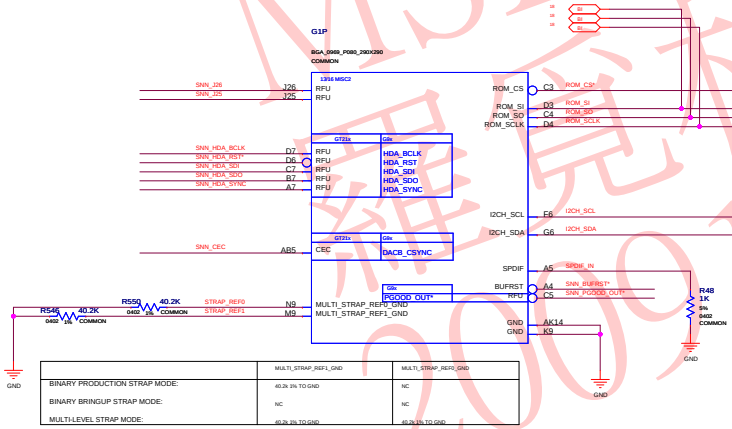
BIOS ROM, HDCP ROM, STRAPPING OPTIONS

STRAPPING OPTIONS



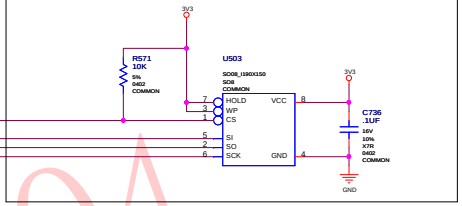
Strap0	USER[3:0]	EDID: 1111	45k PU
Strap1	3GIO_PADCFG[2:0]	DESKTOP: 0000	5k PD
Strap2	PCI_DEVID[3:0]	GT216-200: 0A21 0001	10k PD
ROM_SI	RAMCFG[3:0]		
ROM_SCLK	3: PCI_DEVID_EXT 2: SUB_VENDOR (1 = BIOS rom present) 1: SLOT_CLK_CFG (1 = common clk MCH/GPU) 0: PEX_PLL_EN_TERM (0 = disable pll term)	0110	35k PD
ROM_SO	3: XLK_417 (0 = POR 277MHz) 2: FB_0_BAR_SIZE (0 = POR 256MB) 1: SMB_ALT_ADDR (0=POR, 1= multiGPU) 0: VGA_DEVICE (0=3D device, 1=POR VGA device)	0001	5k PD

0	PD 5k	8	PU 5k
1	PD 10k	9	PU 10k
2	PD 15k	10	PU 15k
3	PD 20k	11	PU 20k
4	PD 25k	12	PU 25k
5	PD 30k	13	PU 30k
6	PD 35k	14	PU 35k
7	PD 45k	15	PU 45k

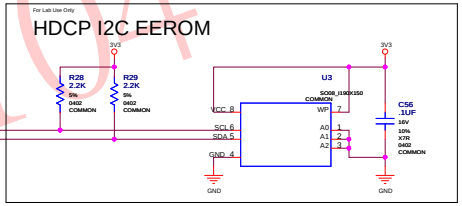


	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION STRAP MODE:	40.2k 1% TO GND	NC
BINARY BRINGUP STRAP MODE:	NC	NC
MULTI-LEVEL STRAP MODE:	40.2k 1% TO GND	40.2k 1% TO GND

BIOS ROM(serial)



HDCP I2C EEROM



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

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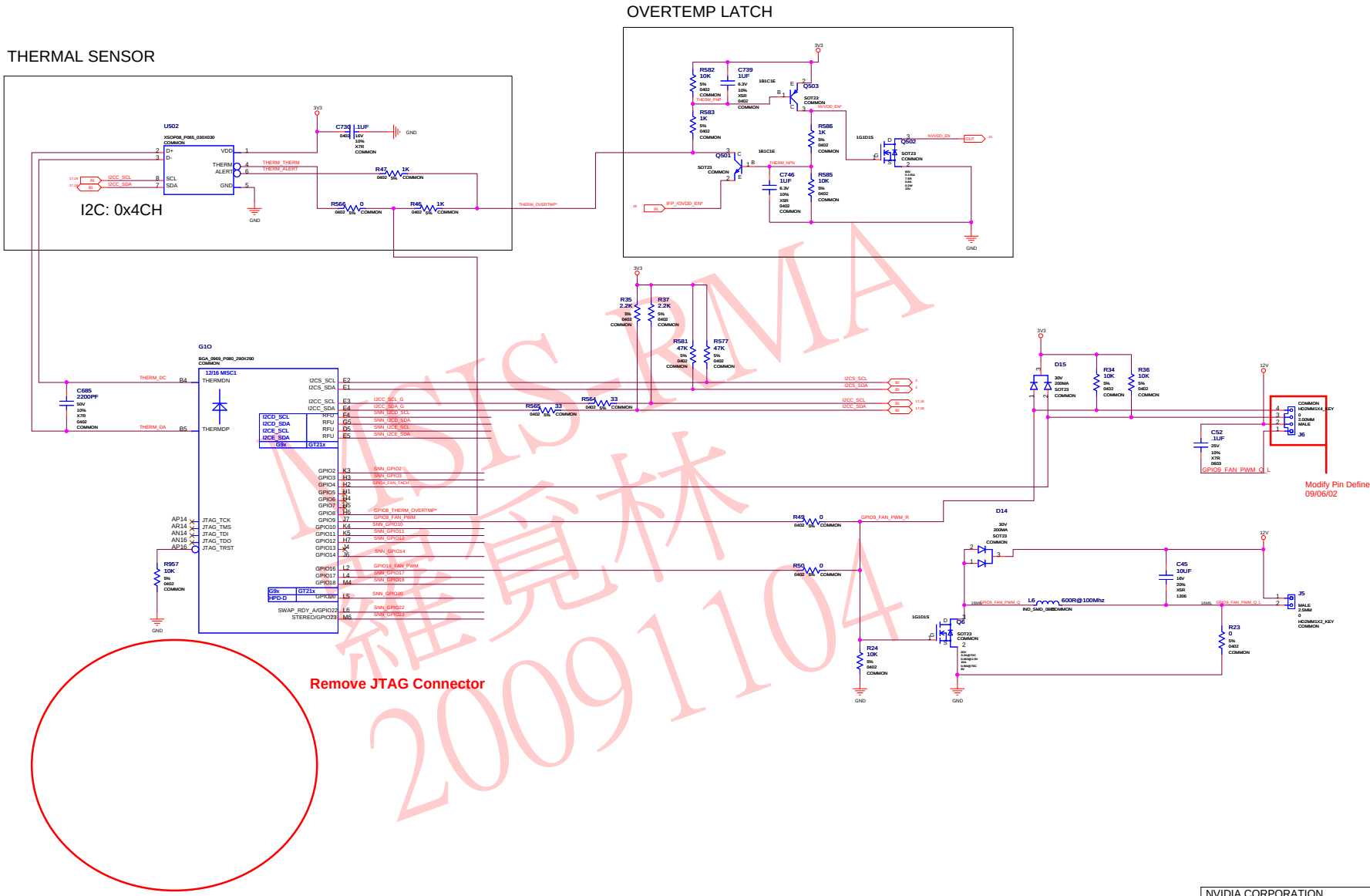
EXTERNAL THERMAL SENSOR, FAN CONTROL, GPIO, JTAG



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	EXTERNAL THERMAL SENSOR, FAN CONTROL, GPIO, JTAG

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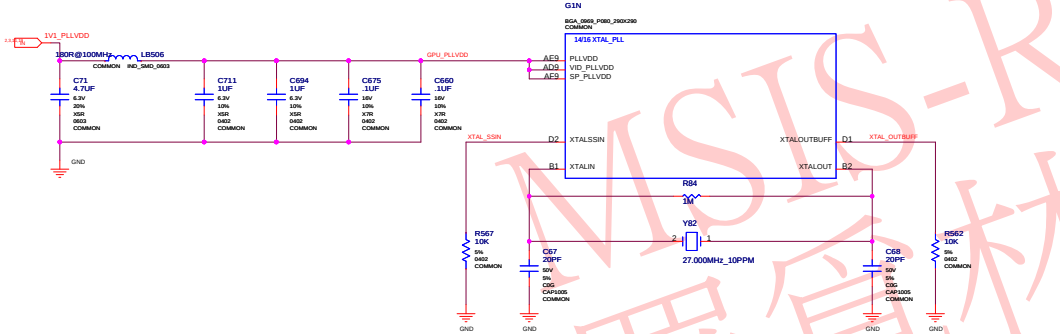
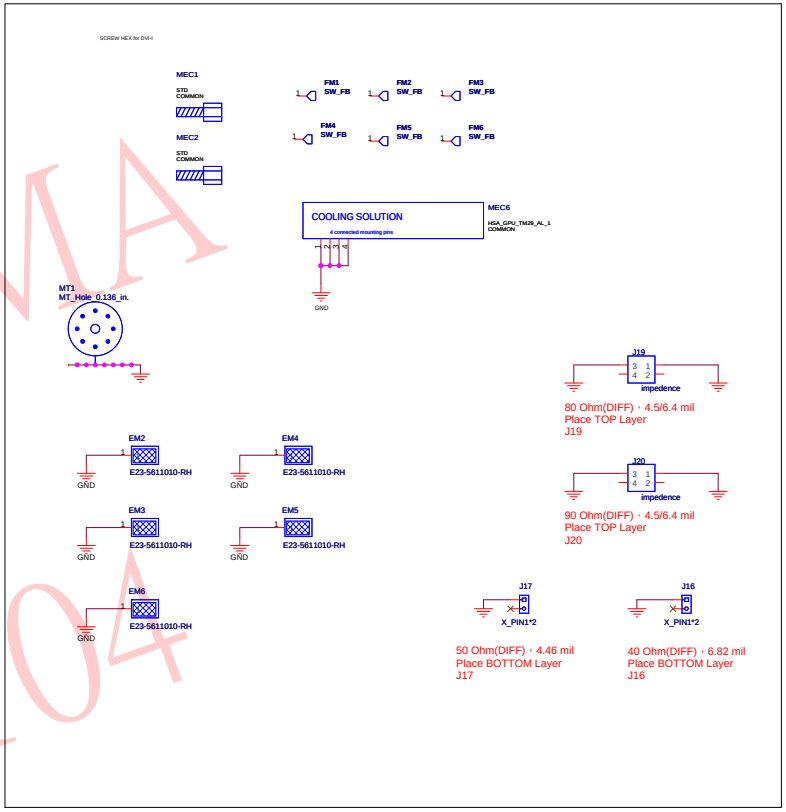
XTAL, MECHANICALS, THERMALS

XTAL/GPU_PLLVDD





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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, MECHANICALS, THERMALS

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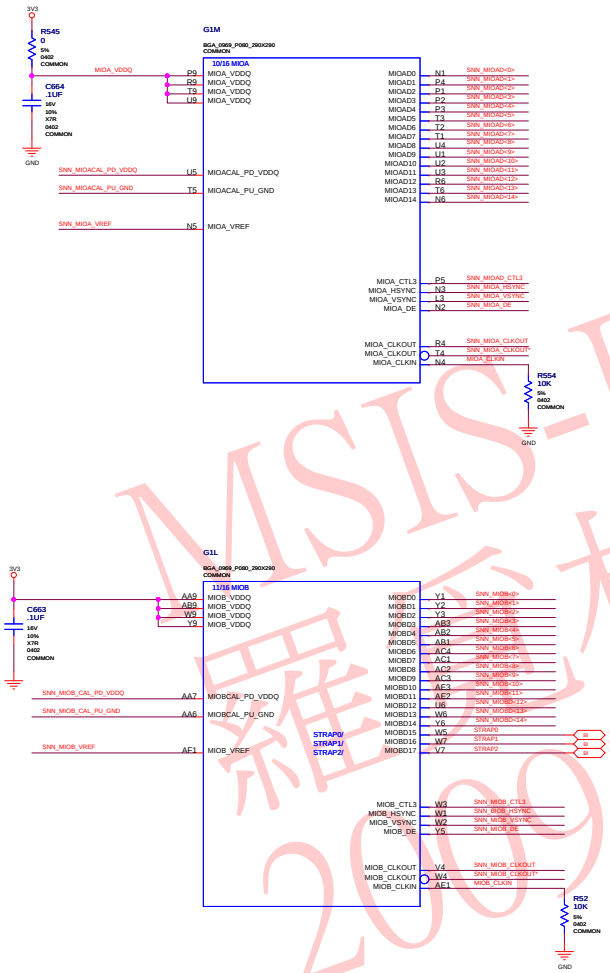
MIOA & MIOB



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB

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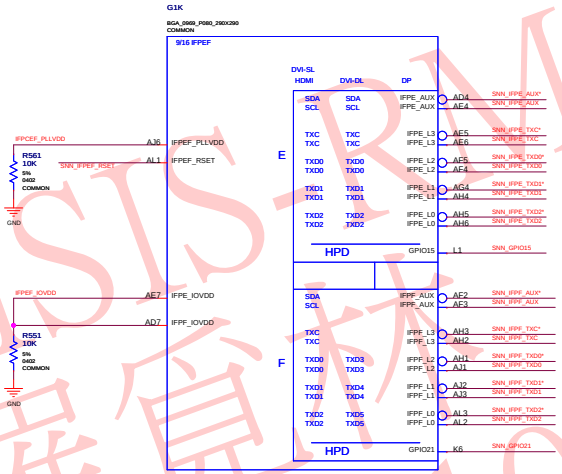
IFP EF (UNUSED)



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2009/11/04

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP EF (UNUSED)

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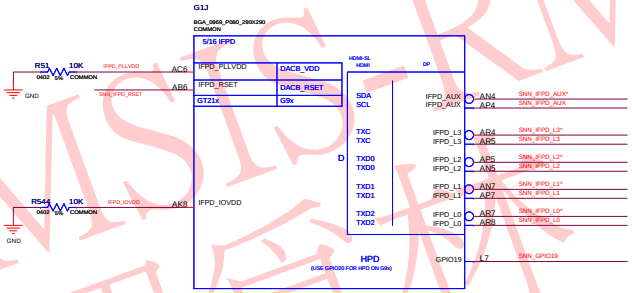
NV_PN	600-10681-base-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

IFP D (UNUSED)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP D (UNUSED)

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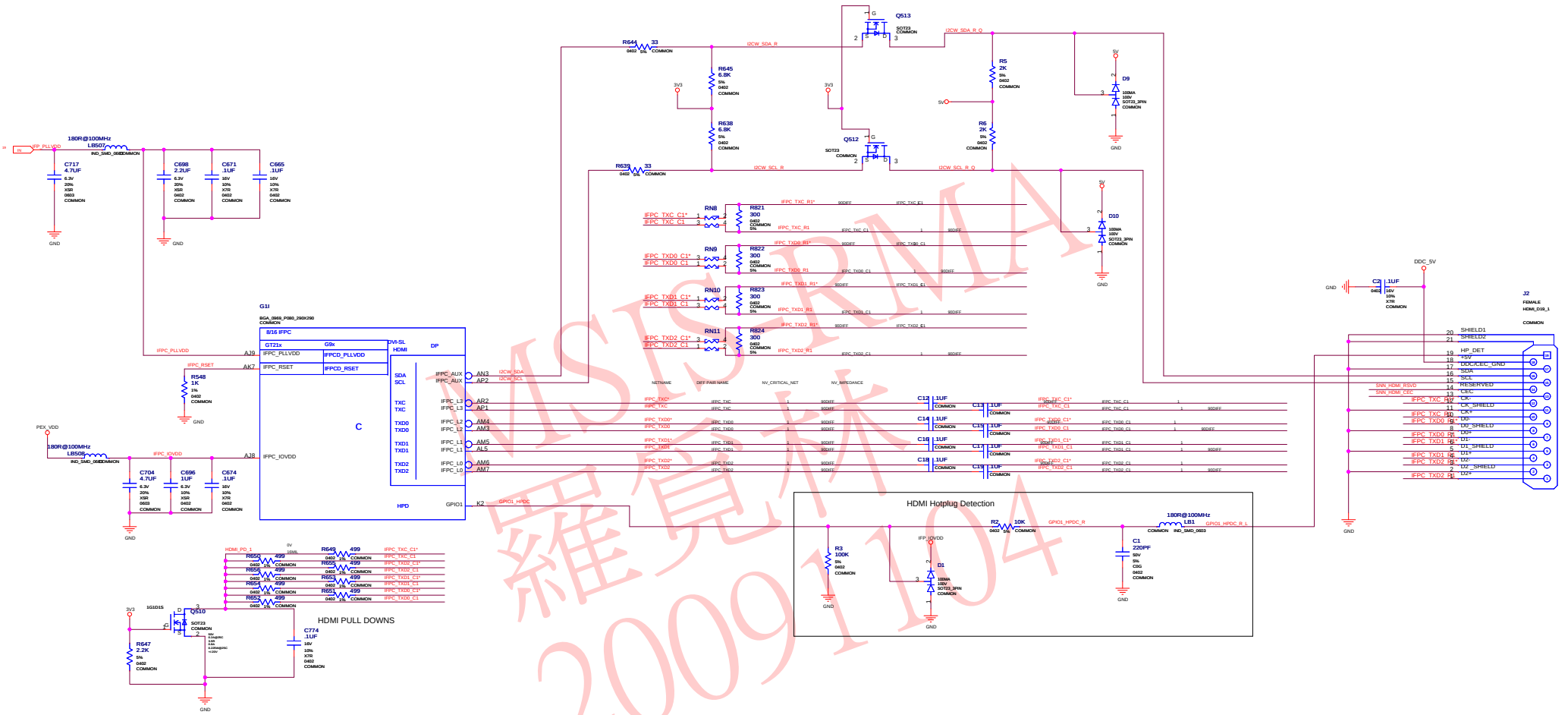
NAME		DATE	05-FEB-2009

IFP C (NORTH HDMI)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP C (NORTH HDMI)

NV_PN	600-10681-base-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

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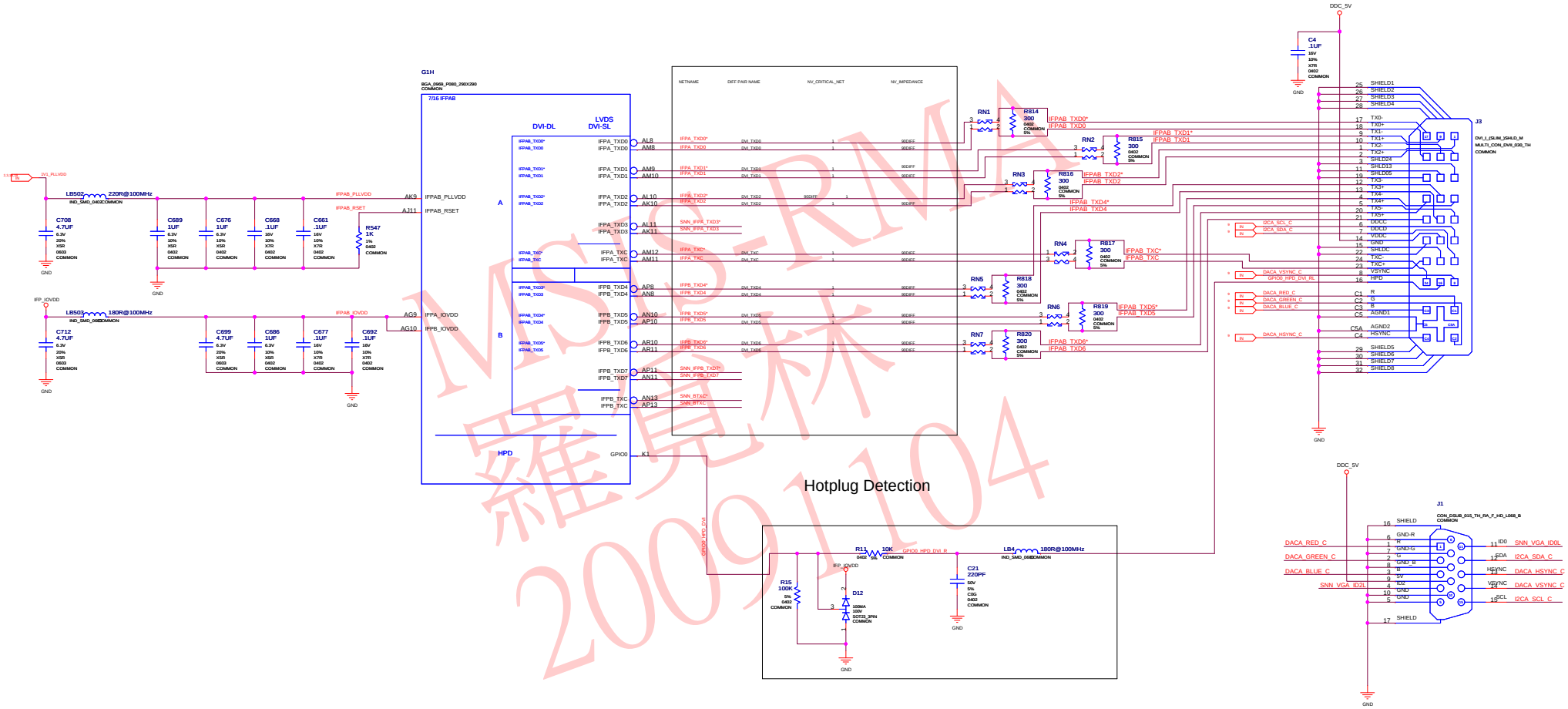
IFP AB (SOUTH DVI-I)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP AB (SOUTH DVI-I)

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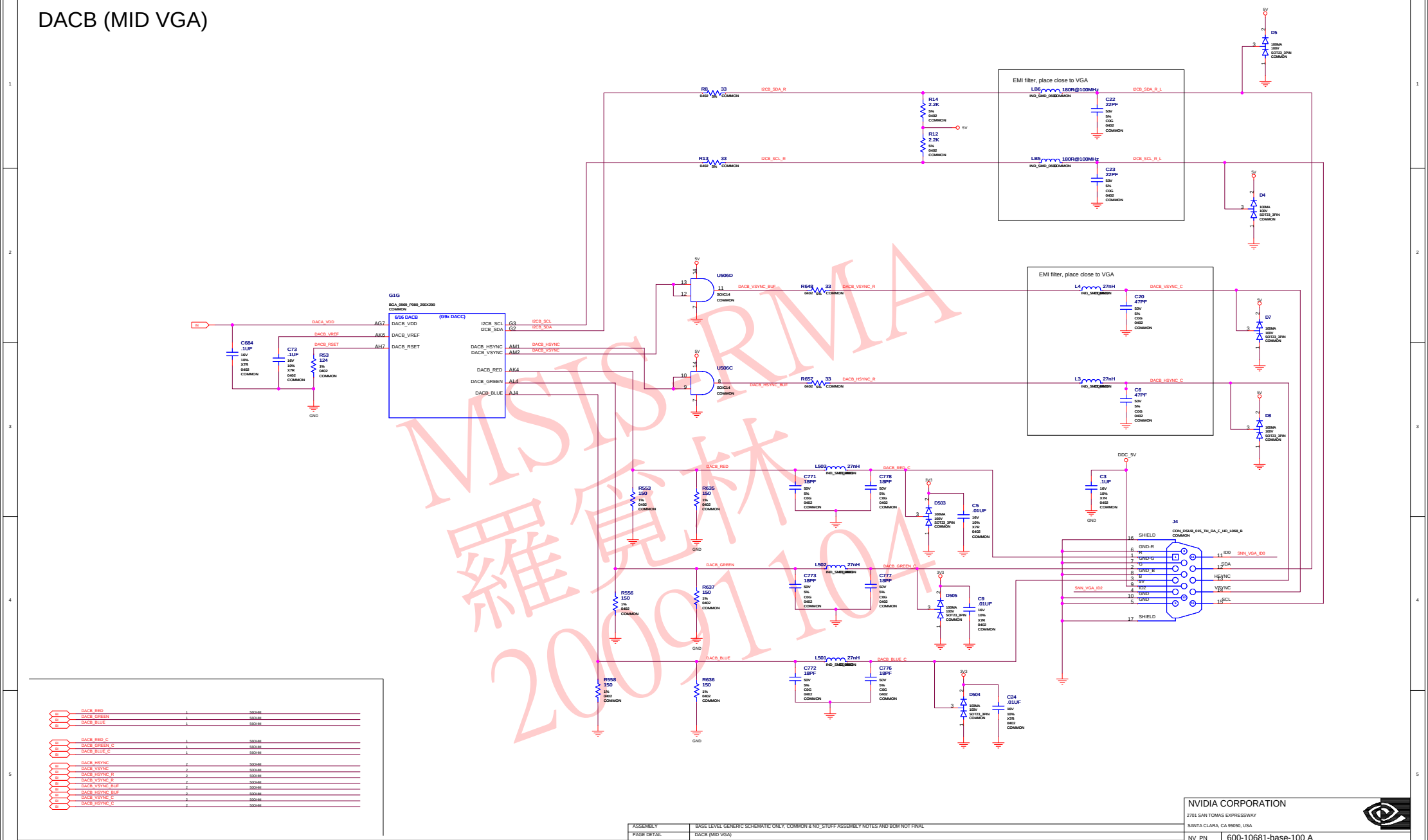
NAME		DATE	05-FEB-2009

DACB (MID VGA)



DACB_RED	1	50OHM	
DACB_GREEN	1	50OHM	
DACB_BLUE	1	50OHM	
DACB_RED_C	1	50OHM	
DACB_GREEN_C	1	50OHM	
DACB_BLUE_C	1	50OHM	
DACB_HSYNC	2	50OHM	
DACB_VSYNC	2	50OHM	
DACB_HSYNC_R	2	50OHM	
DACB_VSYNC_R	2	50OHM	
DACB_VSYNC_BUF	2	50OHM	
DACB_HSYNC_BUF	2	50OHM	
DACB_VSYNC_C	2	50OHM	
DACB_HSYNC_C	2	50OHM	

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB (MID VGA)

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P681-A01 GT215/216 DESKTOP GB1-128 DDR3
PCI-EXPRESSx16 DL-DVI VGA HDMI

Page 1: P681-A01 OVERVIEW
Page 2: PCI-EXPRESS INTERFACE
Page 3: PARTITION A FRAME BUFFER INTERFACE
Page 4: PARTITION A MEMORIES
Page 5: FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS
Page 6: PARTITION C FRAME BUFFER INTERFACE
Page 7: PARTITION C MEMORIES
Page 8: FBC DECOUPLING CAPS
Page 9: DACA (SOUTH DVI-I)
Page 10: DACB (MID VGA)
Page 11: IFP AB (SOUTH DVI-I)
Page 12: IFP C (NORTH HDMI)
Page 13: IFP D (UNUSED)
Page 14: IFP EF (UNUSED)
Page 15: MIOA & MIOB
Page 16: XTAL, MECHANICALS, THERMALS
Page 17: EXTERNAL THERMAL SENSOR, FAN CONTROL, GPIO, JTAG
Page 18: BIOS ROM, HDCP ROM, STRAPPING OPTIONS
Page 19: LINEAR POWER SUPPLIES
Page 20: FBVDDQ/PEXVDD POWER SUPPLY
Page 21: NVVDD POWER SUPPLY

V199 For Lenovo Schematic Change List 2009/03/31 by STEVEN CHANG

Page 2: Remove JTAG Component

Page 10: Move J1 D-SUB Connector to Page 11

Page 11: Add Slim Type D-SUB Connector

Page 17: Remove JTAG Connector

Page 19: Remove IFP_PLLVDD SUPPLY LDO IC

Page 19: Add UP7706 LDO to Change PEX_VDD Power Supply

Page 19: Change AP1117 LDO External Schematic Design

Page 20: Change UP6161 PWM IC to use
UP6101 PWM IC Solution For FBVDDQ Power Supply

Page 20: Change UP6210 PWM IC to use
RT9232 PWM IC Solution For NVVDD Power Supply

Page 20: Remove NVVDD SENSE Net

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SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10681-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10681-0001-100	GT216-300 600/1500MHz 1024MB 64Mx16 BGA100 800MHz DDR3 DVI-I/VGA/HDMI
2	SKU0002	600-10681-0002-100.	GT216-300 600/1500MHz 1024MB 64Mx16 BGA100 1000MHz DDR3 DVI-I/VGA/HDMI
3	SKU0011	600-10681-0011-100	GT215-300 600/1500MHz 1024MB 64Mx16 BGA100 900MHz DDR3 DVI-I/VGA/HDMI
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P681-A01 OVERVIEW

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2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10681-base-100 A		
ID		PAGE	
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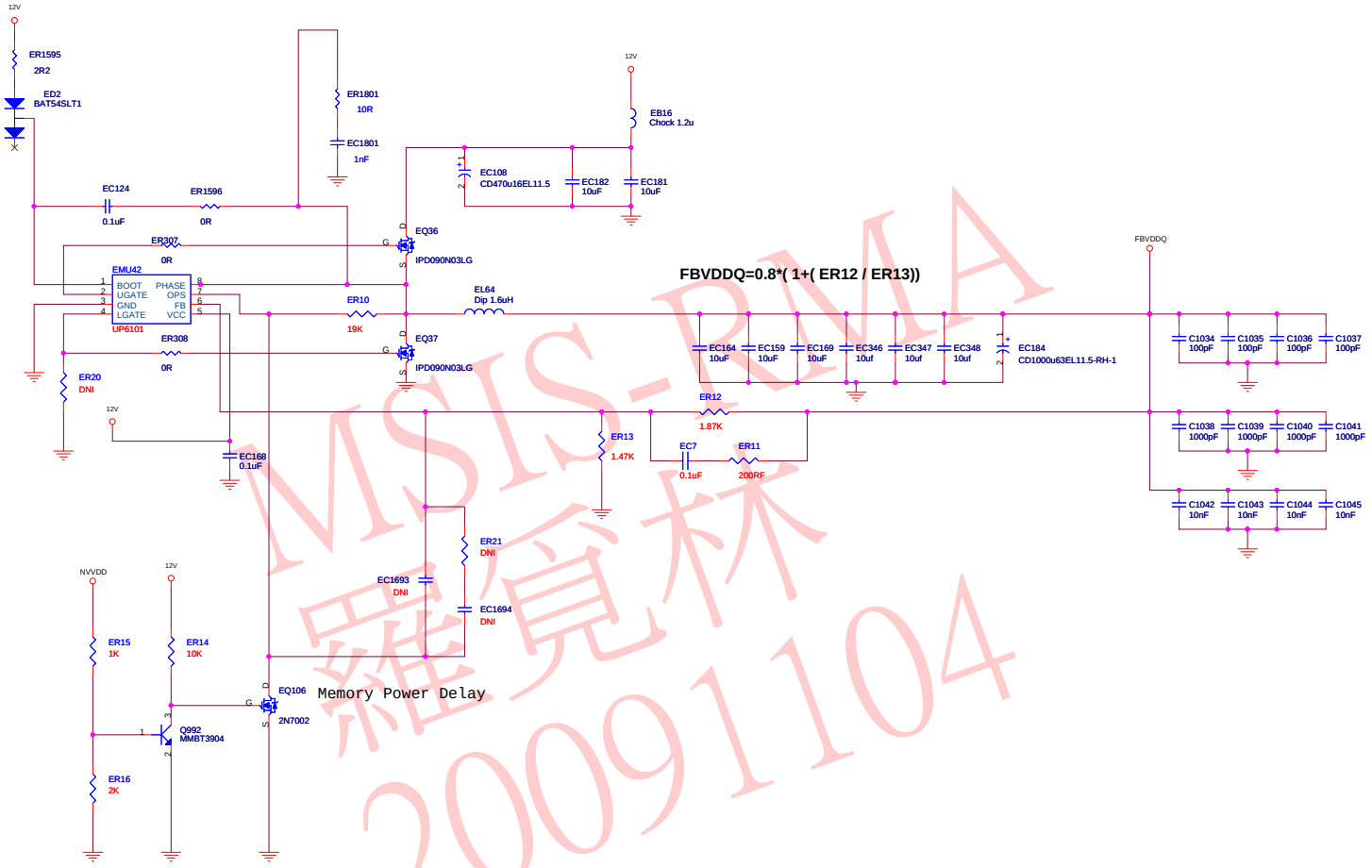
FBVDDQ POWER SUPPLY



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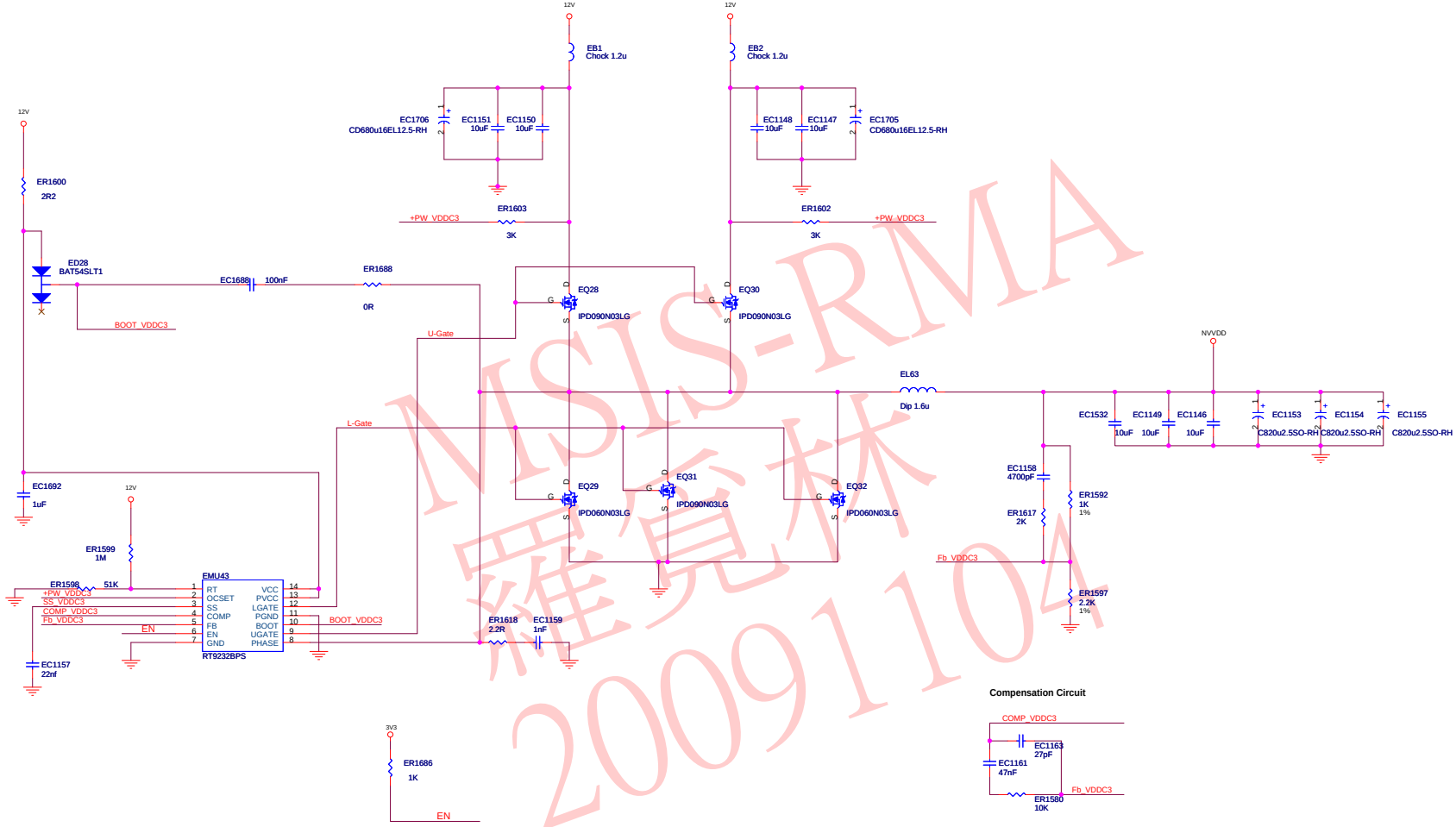
NVVDD POWER

CORE REGULATOR NVVDD



NVVDD=0.8*(1+(ER1592 / ER1597))

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