

MS-V013 VER 10

NV-AGP NV44A 128MB, BGA 8MX16 DDR,VGA,DVI-I,TV-OUT(HT-10)

P362: NV44A, TSOP MEMORY x16

- Page1: P362 Overview
- Page2: AGP Interface
- Page3: Frame Buffer Interface
- Page4: Memory 1st bank 0..31
- Page5: Memory 1st bank 32..63
- Page6: DAC-A, DB15 Connector
- Page7: DAC-B, MUX, DB15
- Page8: TMDS Interface
- Page9: MIOA, MIOB Interface, LPC-ROM
- Page10: STRAPS, Mechanical Parts
- Page11: XTAL, GPIO, BIOS, Fan Control, JTAG Headers
- Page12: VIDEO CAPTURE: SAA7115
- Page13: PowerSupplyI: NVVDD, FBVDDQ
- Page14: PowerSupplyII: 5V, DDC5V, F3V3, TMDS_PLLVDD
- Page15: VIDEO CONNECTORS: MiniDIN, 2x6 HDR

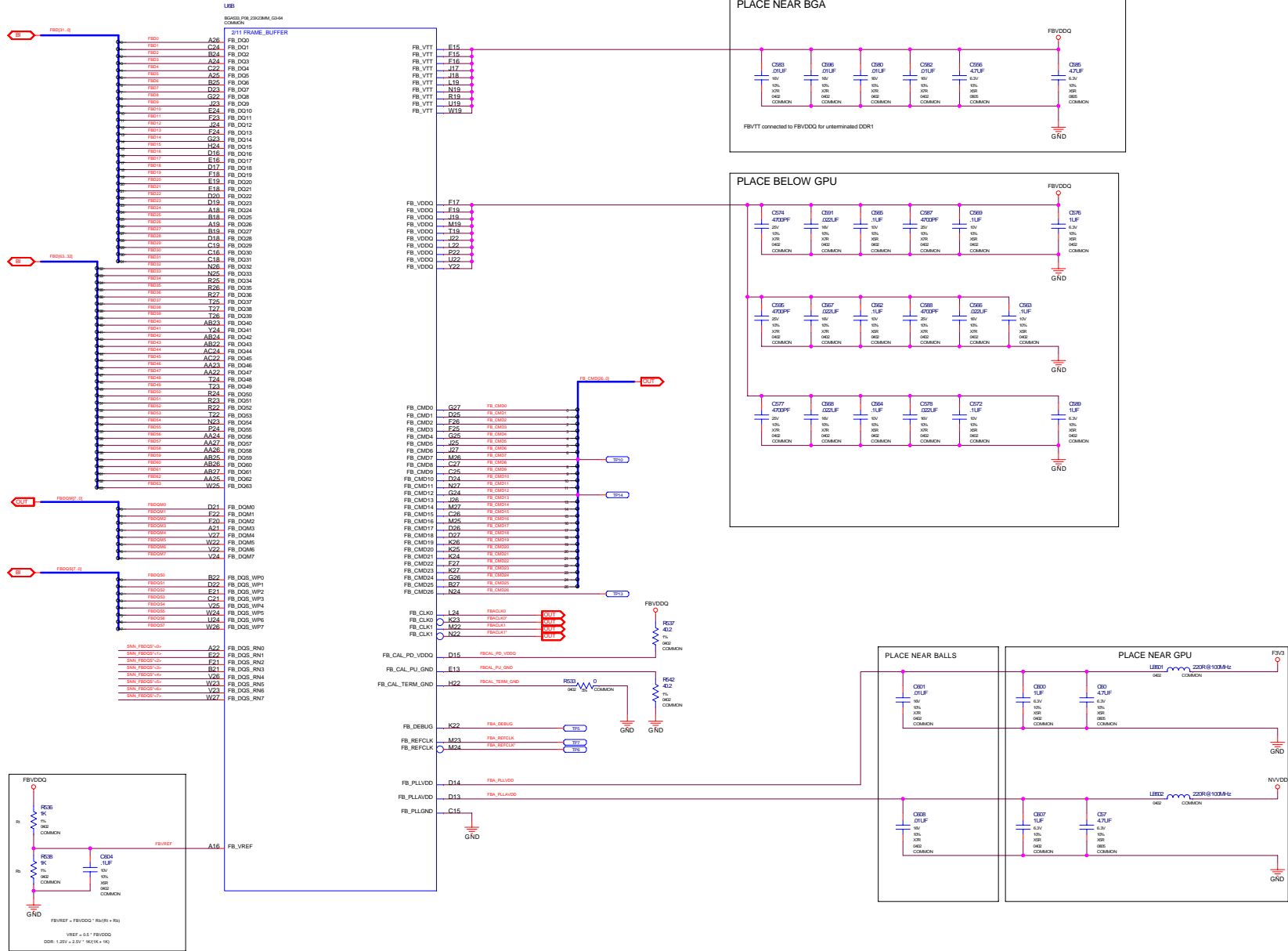
REV	VARIANT	NVPN	ASSEMBLY
8	BASE	800-83pp-xxxx-vvv	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	0000	800-10362-0000-000	NV44A, 392250, 128MB/64-66, 16Mx16, VGA+DVI+HDTV-out
2	0001	800-10362-0001-000	<UNDEFINED>
3	0002	800-10362-0002-000	<UNDEFINED>
4	0003	800-10362-0003-000	NV44A, 392250, 128MB/64-66, 16Mx16, VGA+DVI+HDTV-out, VIDEO IN
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REV HISTORY

A01

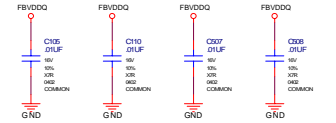
- 1/31/2005:
- 1.PAGE12:VIDEO CAPTURE: Removed SAA7115 Function
Removed:
U2
C15,16,18,19,20,21,22,686,687,688,689,690,691,692,693,694,695,696,697,698,
699,700,701,702,703,704,705,708,709,710,711,712,713,714,715,716,717,718
R15,R16,R17,R20,R21,R653
LB9,LB10,LB511
- 2.Removed Page4: Memory 1st bank 0..31:
Removed:
C107
- 3.Removed Page11: XTAL,GPIO,BIOS,Fan Control:
Removed:
J7
- 4.Changed Page6: DAC-A, DB15 Connector: DACA Sling-type CRT
Removed:
J4
Add:
J3001,J503
- 5.Changed Page7: DAC-B, MUX, DB15:DACB DVI-I
Removed:
J1
- 6.Added Page8: TMDS Interface: EMI suggestion
Added:
R838-R845,R861-R864,L810-L813
- 7.Removed Page15: VIDEO CONNECTORS: MiniDIN, 2x6 HDR: TV-IN(Pin1,2) Circuit
Removed:
LB3,LB4
C7,C8
R7,R8,R9,R10
- 8.Changed Footprint Page10: STRAPS, Mechanical Parts
R640,641/ 595,601 / 596,602 / 643,644 / 651,652 / 647,648
/ 649,650 / 645,646 / 598,604 / 597,603 / 631,632 / 606,608
- 9.Changed Page14: PowerSupplyII: 5V, DDC5V, A3V3, F3V3, TMDS_PLLVDD :
PWM Circuit R,L,C,Mos Cost Down
Removed:
R525
L6,L7,L8
Q3,Q4,Q6
Add:
R999,R1000,R1001,R1002
C200,C201,C202,C203,C204,C205,C206,C207
C1501,C1502
Q10,Q11,Q12
L805,L602
- 6/7/2005:
- Turn 10 PCB
- 1.Cost Down AVL(-):
L810,L811,L812,L813
J3000
C516,C522,C551,C552,R509,R524
D10
- 2.Cost Down AVL(+):
J6,
R23,R838,R839,R840,R841,R842,R843,R844,R845
- 3.Cost Down change:
L602,

GPU: FB-Interface

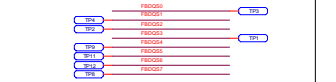


Net Name	NET_SPACING_RULE
NET1	FRICAL_P0_0000
NET2	FRICAL_P0_0000
NET3	FRICAL_TERRA_0000
NET4	FR10LVED
NET5	FR10LVED
NET6	FR10LVED
NET7	FR10LVED
NET8	FR10LVED

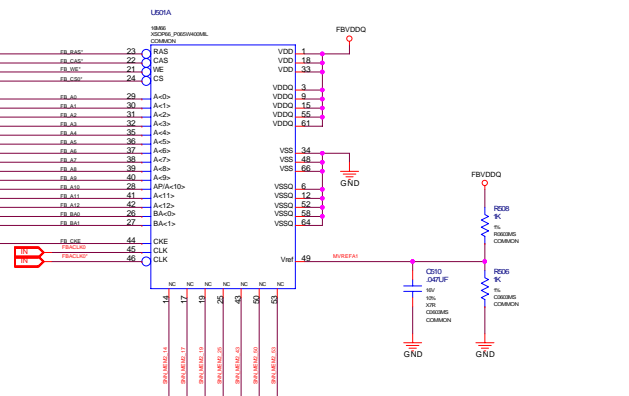
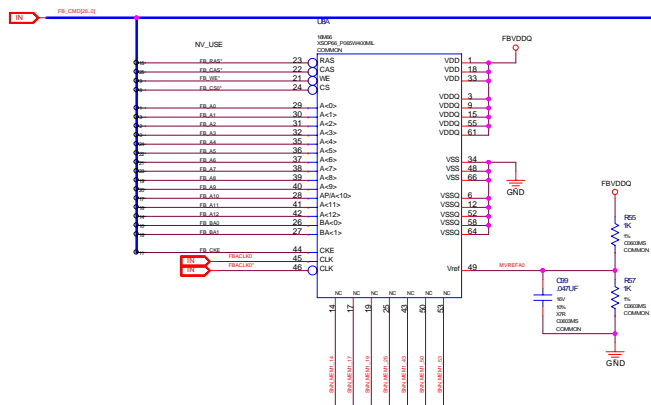
X-Caps for FB_CMD BUS



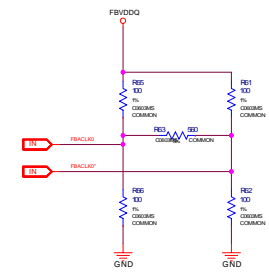
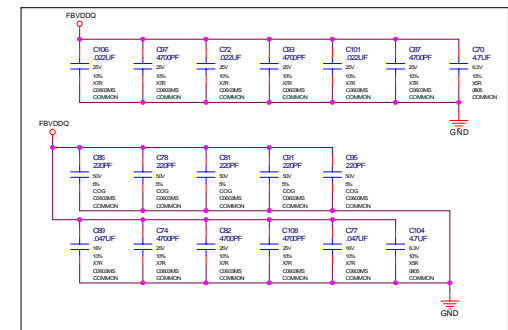
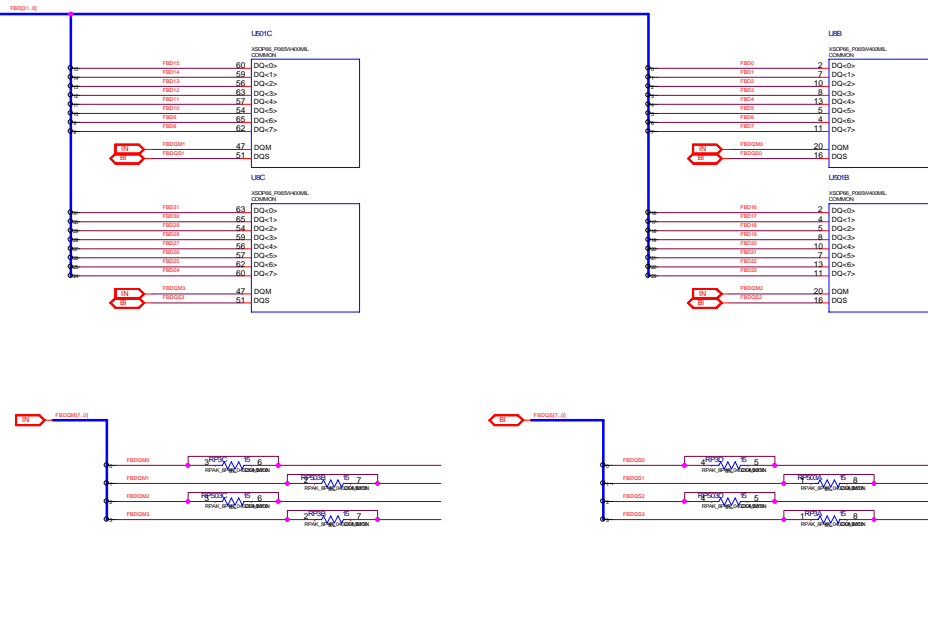
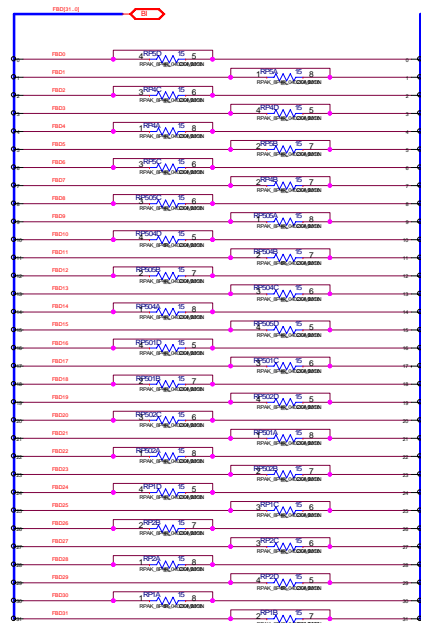
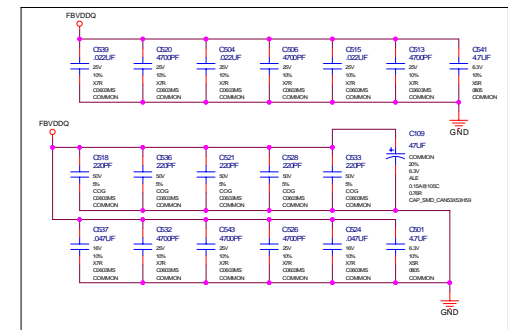
LABTESTPOINTS



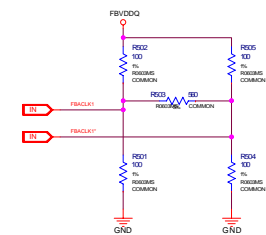
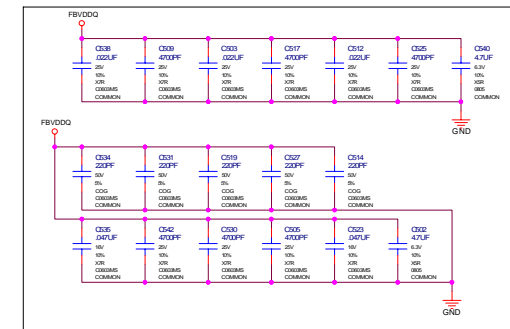
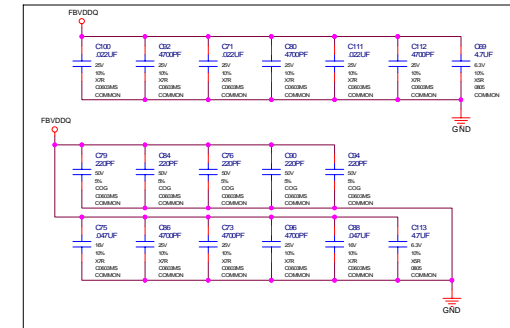
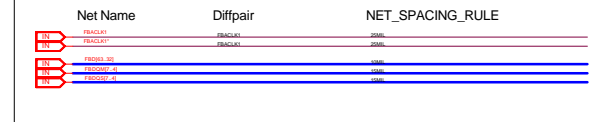
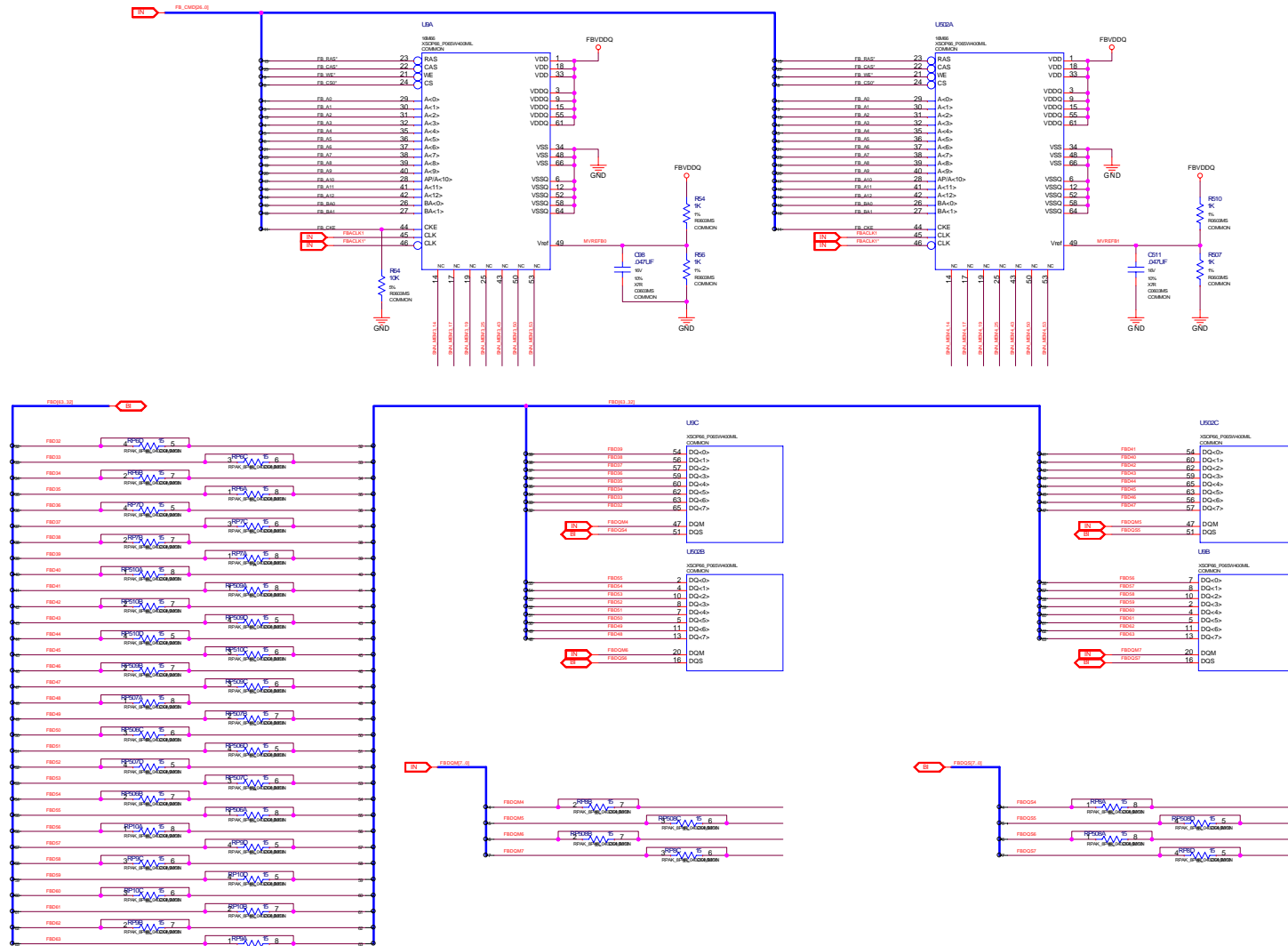
Memory Bit 0..31



Net Name	Diffpair	NET_SPACING_RULE
FDAC42	FDAC43	2000
FDAC42P	FDAC43	2000
FD001_0		1000
FD0000_0		1000
FD0000_0		1000
FD40000_0		1000

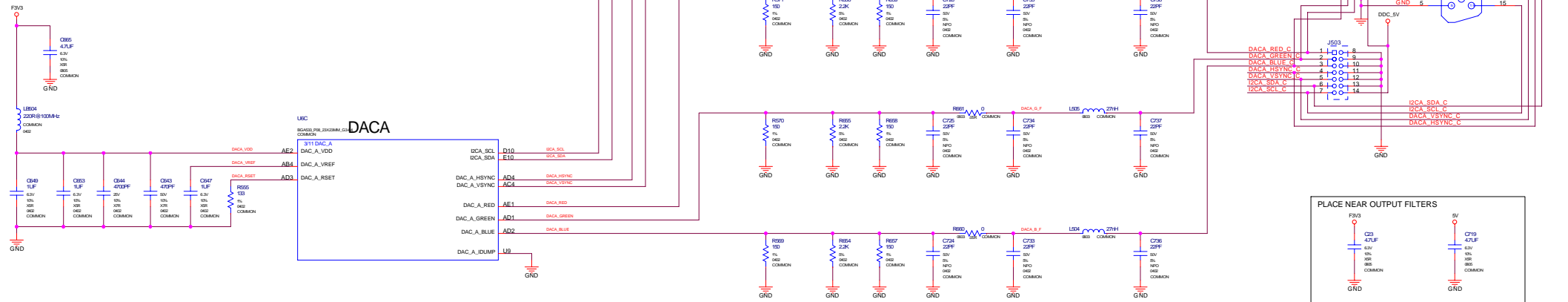
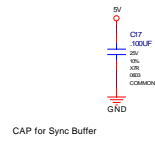


Memory Bit 32..63

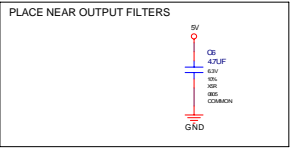
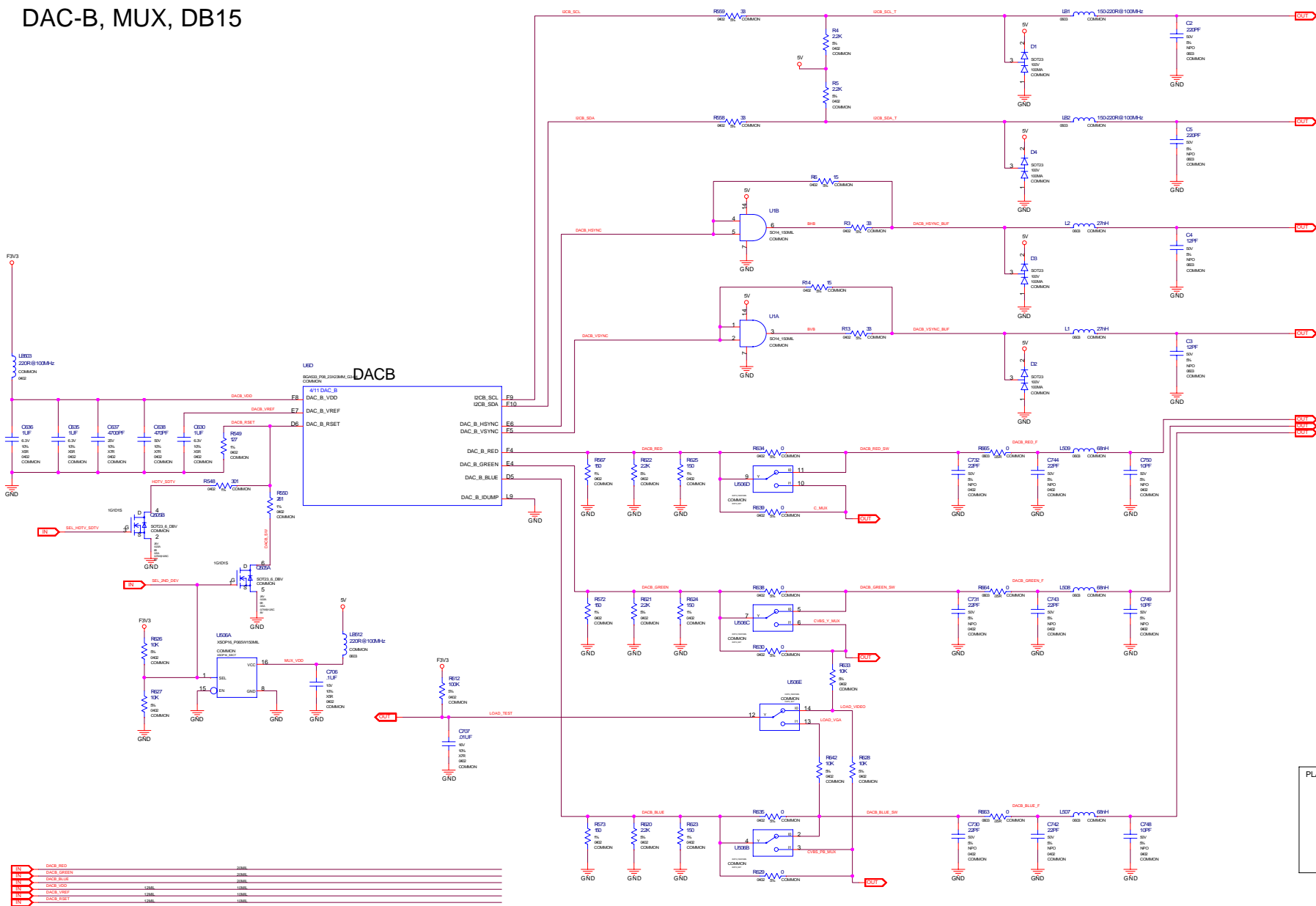


DAC-A, DB15 Connector

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100%	DATA_V02NC		100MIL
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100%	DATA_V03NC		100MIL
100%	DATA_V04BNC		100MIL
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100%	DATA_W05U		100MIL
100%	DATA_W05V		100MIL
100%	DATA_W05W		100MIL
100%	DATA_W05X		100MIL
100%	DATA_W05Y		100MIL
100%	DATA_W05Z		100MIL
100%	DATA_W06A		100MIL
100%	DATA_W06B		100MIL
100%	DATA_W06C		100MIL
100%	DATA_W06D		100MIL
100%	DATA_W06E		100MIL
100%	DATA_W06F		100MIL
100%	DATA_W06G		100MIL
100%	DATA_W06H		100MIL
100%	DATA_W06I		100MIL
100%	DATA_W06J		100MIL
100%	DATA_W06K		100MIL
100%	DATA_W06L		100MIL
100%	DATA_W06M		100MIL
100%	DATA_W06N		100MIL
100%	DATA_W06O		100MIL

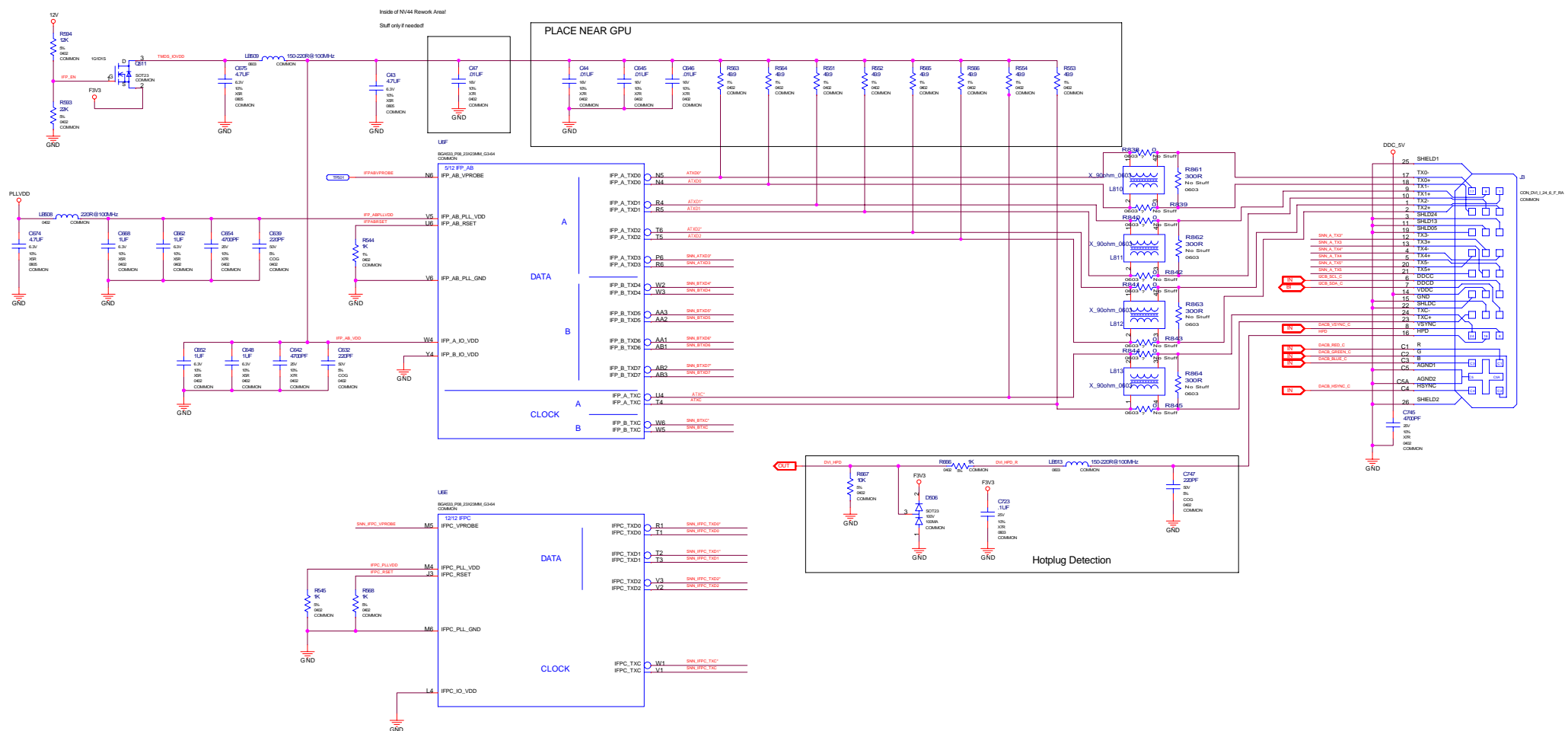


DAC-B, MUX, DB15

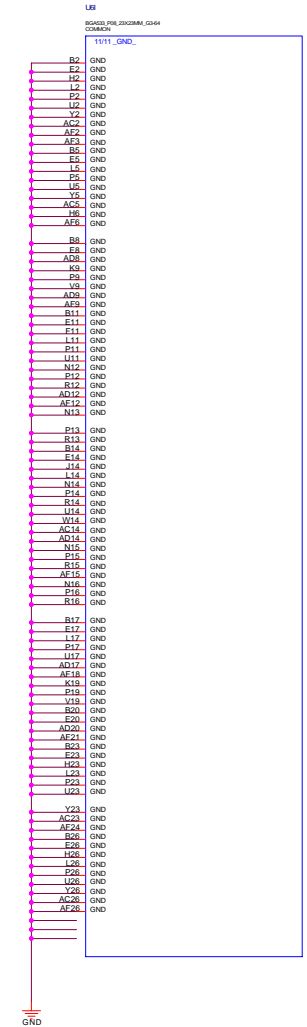
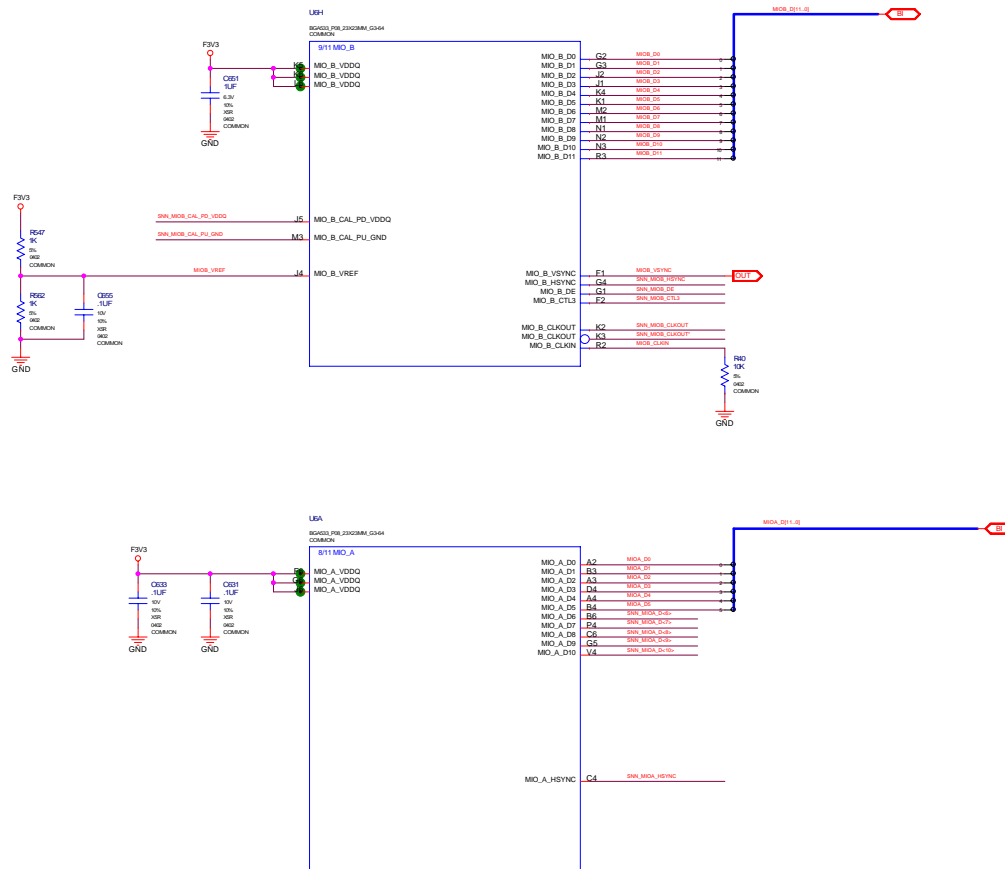


Internal TMDS, DVI-Connector

Net Name	Diffpair	NET_SPACING_RULE	Voltage
Net1	BT_ABP11_VDD		3.3V
Net2	BT_AB_VDD		3.3V
Net3	47502	ATAC	200M_GDS_300M
Net4	47502	ATAC	200M_GDS_300M
Net5	47502	ATAC	200M_GDS_300M
Net6	47502	ATAC	200M_GDS_300M
Net7	47502	ATAC	200M_GDS_300M
Net8	47502	ATAC	200M_GDS_300M
Net9	47502	ATAC	200M_GDS_300M
Net10	47502	ATAC	200M_GDS_300M
Net11	47502	ATAC	200M_GDS_300M

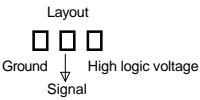


MIOA, MIOB Interface, LPC-ROM

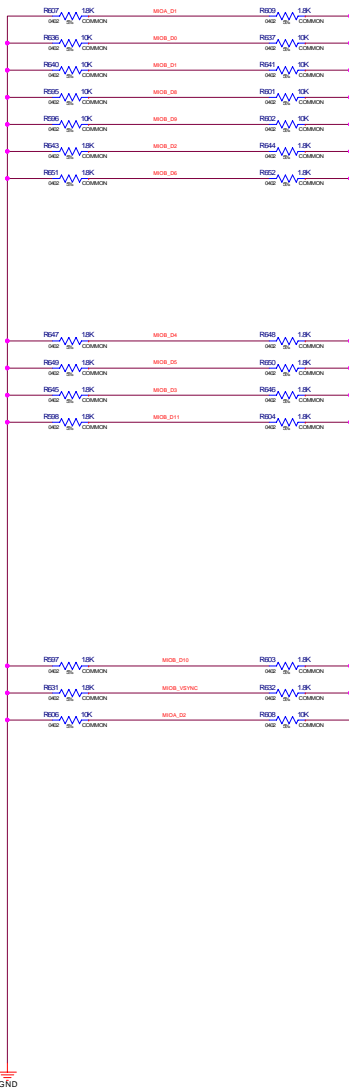


STRAPS, Mechanical Parts

Overlap pads to save space
and to prevent assembly of
both resistors.



NV44 STRAPS

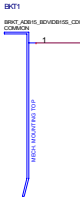


Bit	Signal	Values
00	PCI_AD_STAMP	0 REVERSED 1 NORMAL
01	SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS
02	RAM_CFG_0	See Hsp Tuning Pattern/Problems... Also see Hsp Tuning Pattern/Problems...
03	RAM_CFG_1	
04	RAM_CFG_2	
05	RAM_CFG_3	
06	CRYSTAL_0	00 13.500 MHz 01 14.31818 MHz 10 27.000 MHz 11 UNKNOWN
22	CRYSTAL_1	
07	TV_MODE_0	00 SECAM 01 NTSC 10 PAL 11 CRT
08	TV_MODE_1	
09	ASP_30_34	0 ASP03 ENABLED 1 ASP03 DISABLED
10	ASP_35A	0 SBA ENABLED 1 SBA DISABLED
11	ASP_FASTTWR	0 F/W ENABLED 1 F/W DISABLED
12	PCI_DEV0_0	0000 default by silicon straps
13	PCI_DEV0_1	
20	PCI_DEV0_2	
21	PCI_DEV0_3	
14	BUS_TYPE	0 PCI 1 AGP
15	FP_FACE	0 0468 1 128H (DEFAULT)
23	FB_0	00 64H 01 128H 10 256H (DEFAULT) 11 512M
24	FB_1	
25	BR	0 BRIDGE DISABLED 1 BRIDGE ENABLED
26	BR_128H	BR BIT'S IGNORED IF BRIDGE IS DISABLED
27	BR_AGP	
28	BR_ID	
29	ROM_TYPE_0	0 PARALLEL 01 SERIAL_AT2SF 10 SERIAL_16T4050F 11 LPC
30	ROM_TYPE_1	
16	USER_0	0000 (DEFAULT)
17	USER_1	
18	USER_2	
19	USER_3	
REV_FLT_EN_TERR100		
SIOD_PIOCFG_LUT_ADDR[0]		
SIOD_PIOCFG_LUT_ADDR[1]		

CABLE



PCB



MEC3



MEC4



MEC5

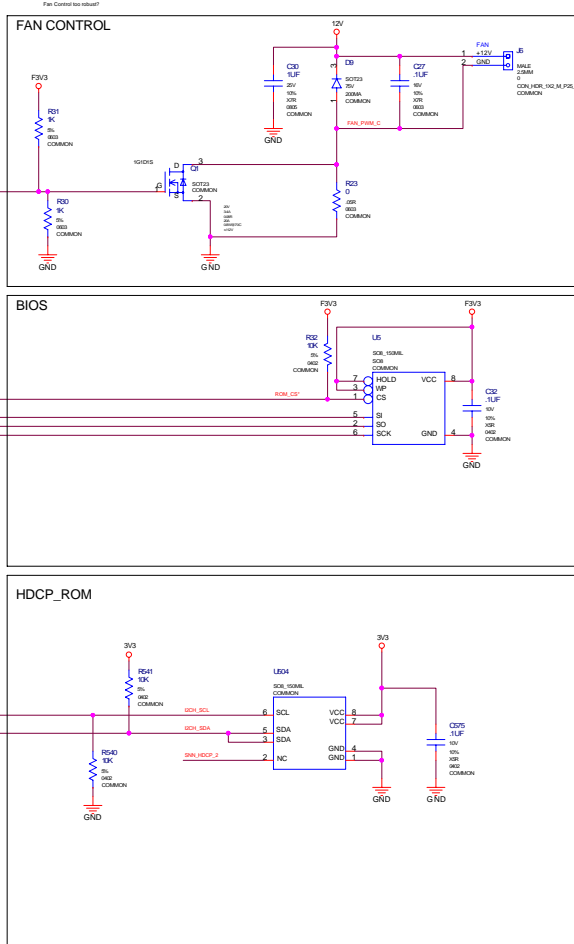
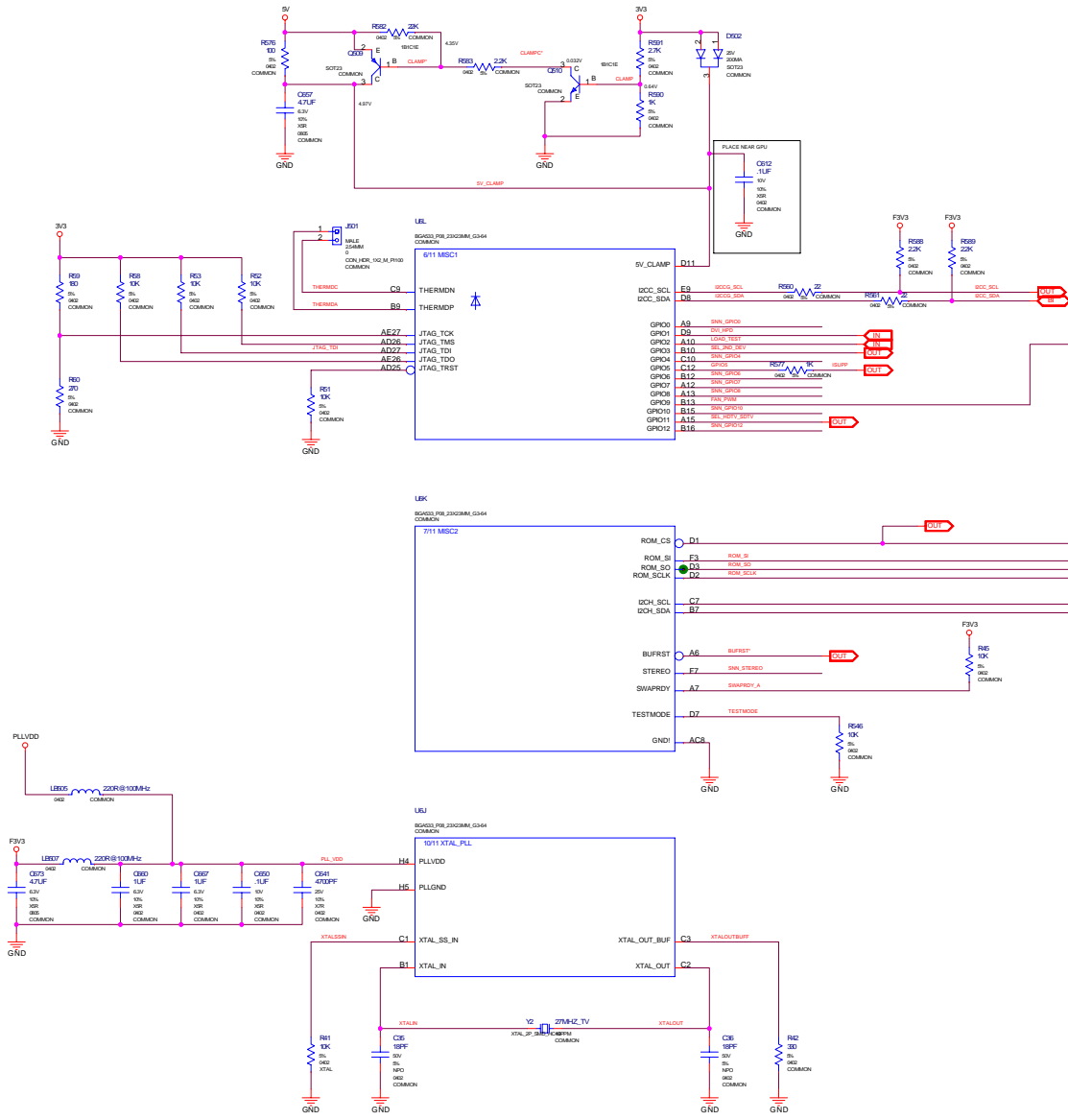


MEC2



XTAL, GPIO, BIOS, Fan Control, JTAG Headers

Net Name	NET_PHYSICAL_TYPE	NET_SPACING_RULE
XTALIN	SWL_TRACE	20MIL
XTALOUT	SWL_TRACE	20MIL
PLLVDD	SWML_TRACE	10MIL
PLLVSS	SWML_TRACE	10MIL

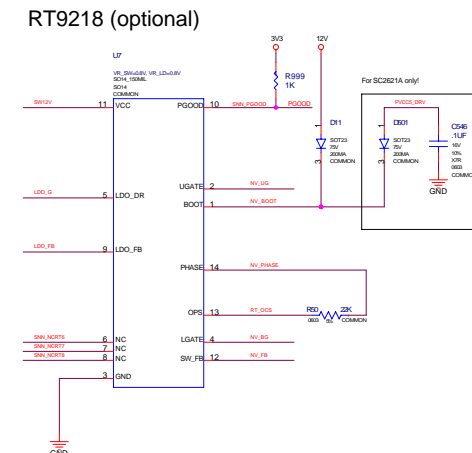
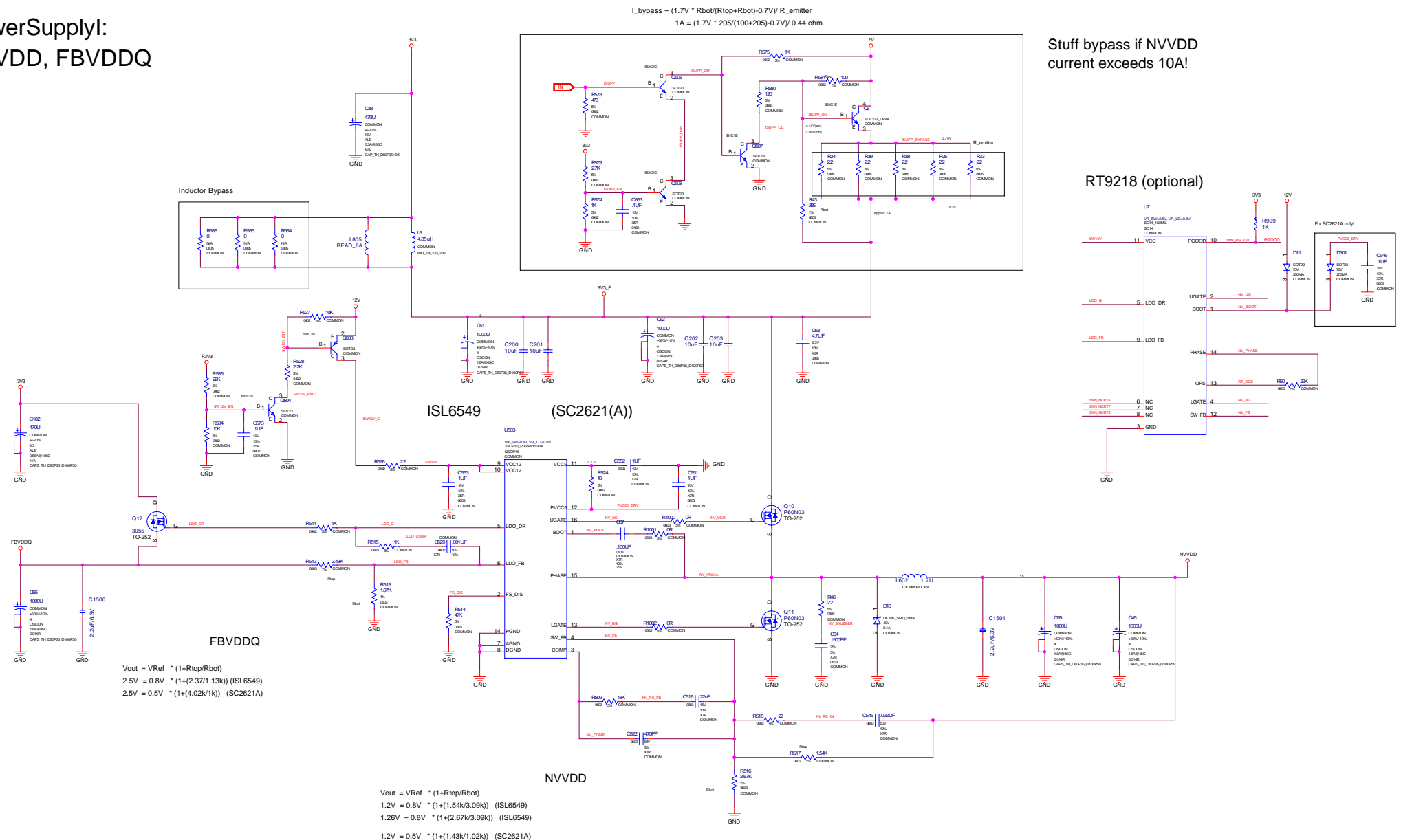


PowerSupply:
NVVDD, FBVDDQ

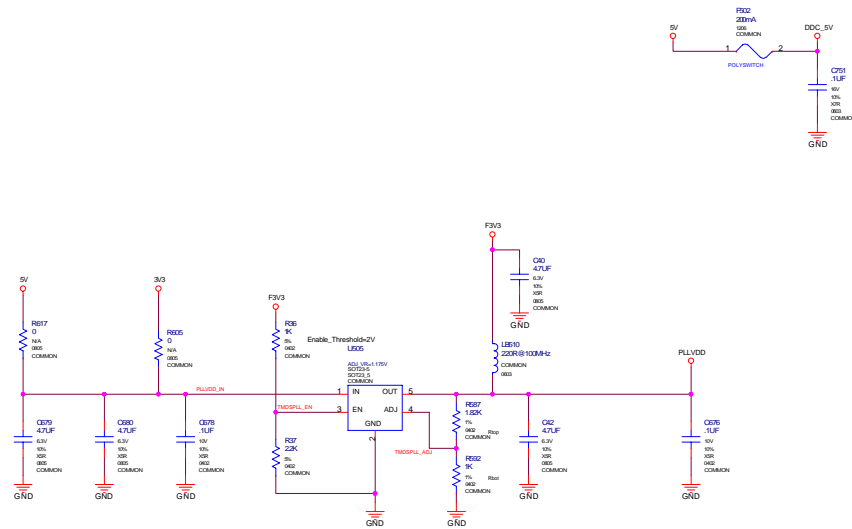
$$I_{\text{bypass}} = (1.7V \cdot R_{\text{bot}} / (R_{\text{top}} + R_{\text{bot}}) - 0.7V) / R_{\text{emitter}}$$

$$1A = (1.7V \cdot 205 / (100 + 205) - 0.7V) / 0.44 \text{ ohm}$$

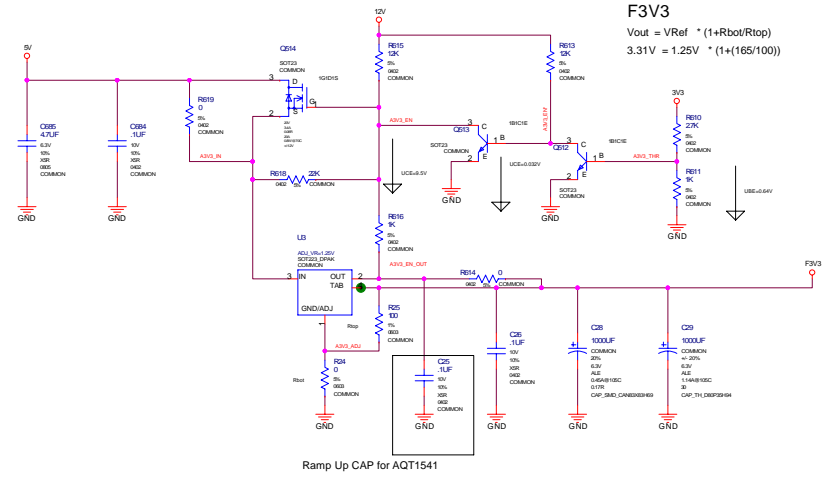
Stuff bypass if NVVDD
current exceeds 10A!



PowerSupplyII: DDC5V, F3V3, TMDS_PLLVDD



TMDS_PLLVDD
 $V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$
 $3.31V = 1.175V * (1 + (1.82k/1k))$



Net Name	NET_PHYSICAL_TYPE	Voltage
SW (0) DDC_5V	120kΩ	5V
FPGA	120kΩ	3.3V
PLLVD0	120kΩ	3.3V
1V1 1V1_P1	120kΩ	1.0V

SV_FUSED

125 ns

500 ns

