

P393-A01 Base Design

P393-A01, G92, 8Mx32/16Mx32 GDDR3 (800/1000 MHz),
DVI-I-DL, DVI-I-DL/DisplayPort, HDTVout/Stereo

Table of Contents:

Page 1: Overview
Page 2: PCI Express 1.0
Page 3: MEMORY: GPU Partition A/B
Page 4: MEMORY: GPU Partition C/D
Page 5: FBA Partition
Page 6: FBB Partition
Page 7: FBC Partition
Page 8: FBD Partition
Page 9: FrameBuffer Net Rules
Page 10: DACA Interface
Page 11: DACC Interface
Page 12: IFP A/B and C/D Interface
Page 13: DACB and Stereo Interface
Page 14: Multi-use IO(MIO) Interface
Page 15: DisplayPort Transmitter
Page 16: MISC: GPIO, I2C, BIOS, PLL, and XTAL
Page 17: Thermal Control/Protection and SPDIF Input
Page 18: Power/GND and Decoupling
Page 19: Configuration Straps and Mechanical
Page 20: Power Supply: 5V, STEREO_5V, 2V5, DP_PWR
Page 21: Power Supply: 1V2, 1V8
Page 22: Power Supply: FBVDD/Q, 8V5
Page 23: Power Supply: NVVDD Regulator
Page 24: Power Supply: NVVDD Phase 1 & 2
Page 25: Power Supply: NVVDD Phase 3
Page 26: Power Supply: Filter/Detection 3V3, 12V, 12V_PEX6
Page 27: Power Supply: Hybrid Power

- 1.V117-0C Base on P393
 - 2.page 2 del Q1209,R1219,R58,R55,C63 circuit ,del net pex_rst link page27
 - 3.page 10 del I2CA_SCR_R,I2CA_SDA_R link net Page 27
 - 4.page 11 del I2CB_SCR_R,I2CB_SDA_R link net page27
 - 5.page 15 del Display port circuit
 - 6.page 16 del I2CS for Hybrid power circuit , del GPIO 4/10 net, R91 link gnd, del R66,R75
 - 7.page 14 del MIOB_D2/3/4/5/6/7/10 net link page 19
 - 8.page 20 del DP_POWER circuit
 - 9.page 27 del Hybrid power circuit
 - 10.page 3/5/6. update FBA_CMD(25..0)/FBB_CMD(25..0)
 - 11.page 4/7/8. update FBC_CMD(25..0)/FBD_CMD(25..0)
 - 12.page 17. del GPIO4_FAN_PWM_R net
- V117-0D Base on P393
- 1.page 10 DAC-A Co-lay slim D-sub with DVI
 - 2.page 11 DAC-C Co-lay slim D-sub with DVI
 - 3.page 17 Modify SPIDF in circuit and co-lay MAX6649 circuit with ATD7473
 - 4.page 21 Modify 1V8 power circuit.
 - 5.page 22 Modify 1V2 and FBVDD power circuit.
 - 6.page 23 Modify NVVDD power circuit.
 - 7.page 26 Del 3V3_Q power and change 12V chock to DIP
 - 8.page 19 Del MEC2
 - 9.page 20 Del 5V STEREO Supply
- V117-300 Base on P393 and V117-0D
- 1.page 23 correct Q510 and add 0 ohm by pass
 - 2.page 22 Change L11 and C167,C168 footprint

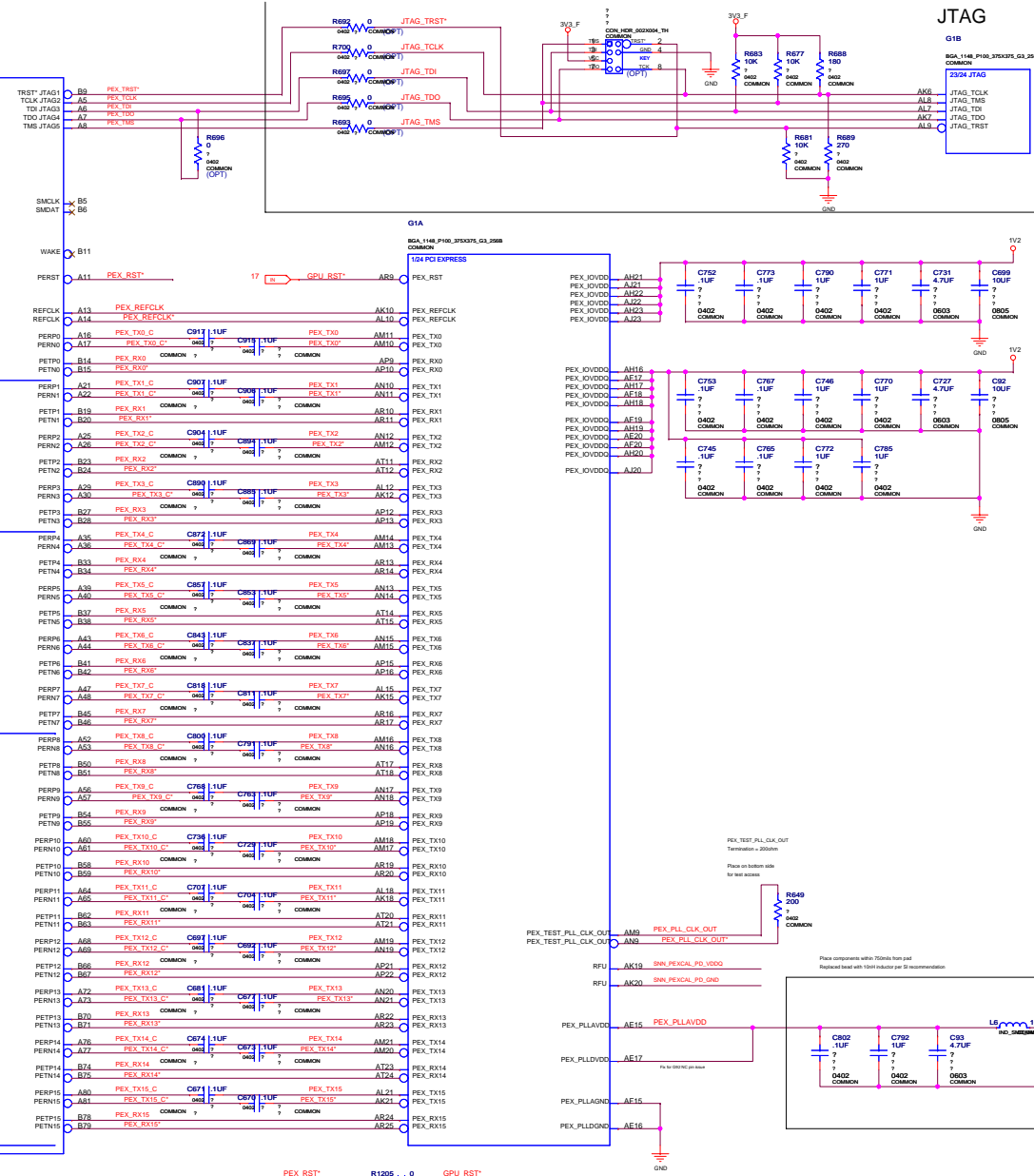
REV	VARIANT	NPVN	ASSEMBLY
B	BASE	800-10393-base-100	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKL_DT_0000	800-10393-0000-100	P393 G92-300 512MB GDDR3 16Mx32 DVI-I+HDTV
2	SKL_DT_0002	800-10393-0002-100	P393 G92-200 512MB GDDR3 16Mx32 DVI-I+HDTV
3	SKL_W8_0501	800-10393-0501-100	P393 G92-475 512MB GDDR3 16Mx32 DVI-I+HP+STEREO
4	SKL_W8_0501	800-10393-0501-100	P393 G92-850 512MB GDDR3 16Mx32 DVI-I+HDTV
5	SKL_DT_0004	800-10393-0004-100	P393 G92-275 512MB GDDR3 16Mx32 DVI-I+HDTV
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
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ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview



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SUMMARY			
Size	Document Number	MS-V117	
Custom			Rev 100
Date:	Friday, December 14, 2007	Sheet	1 of 27



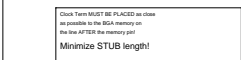

* PROMOTER maintains design system
Stall only to bypass the micro-controller
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ASSEMBLY PAGE DETAIL	P303 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL PCI Express 1.0
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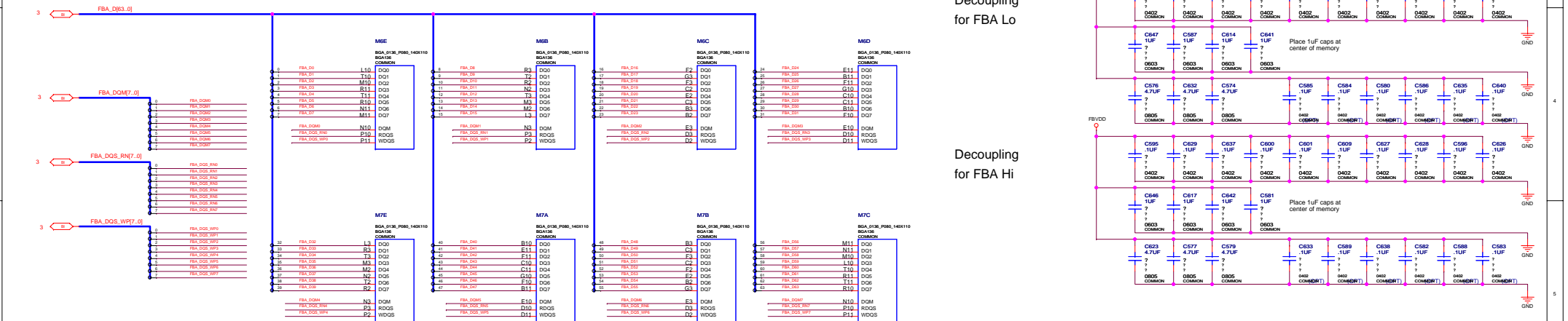


Minimize STUB length!

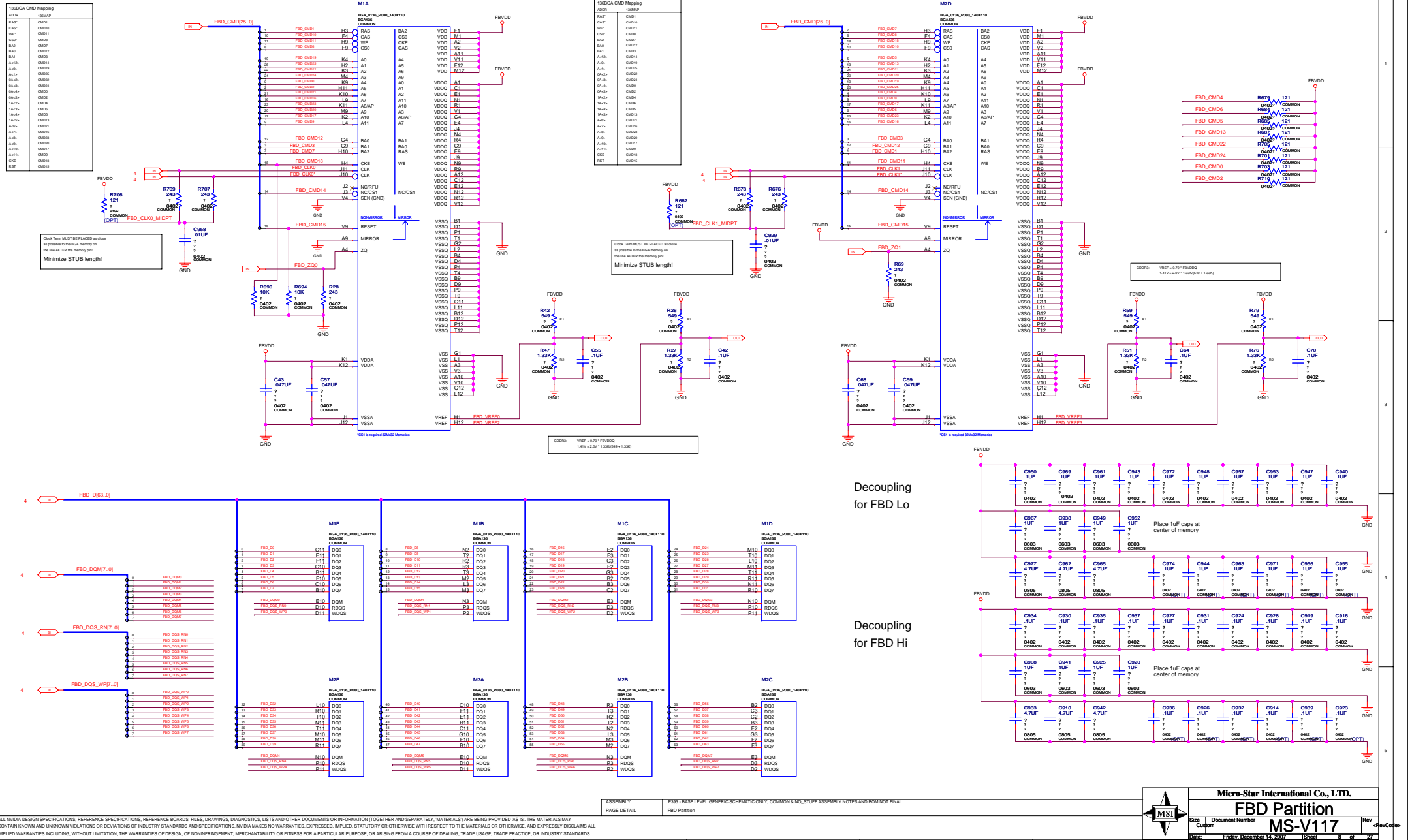
GOOR3: $V_{REF} = 0.70 \cdot FBV_{DDQ}$
 $1.41V = 2.0V \cdot 1.33K/549 + 1.33K$

Decoupling for FBA Lo

Decoupling for FBA Hi



138BGA CMD Mapping	
RAS	CM01
CAS	CM02
WE	CM03
CS0	CM04
BA2	CM07
BA0	CM08
BA1	CM09
A0	CM10
A1	CM11
A2	CM12
A3	CM13
A4	CM14
A5	CM15
A6	CM16
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NET RULES for FrameBuffer A/B

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
OUT FBA_CLK0 3.5	1	800FF	FBA_CLK0
OUT FBA_CLK0P 3.5	1	800FF	FBA_CLK0
OUT FBA_CLK1 3.5	1	800FF	FBA_CLK1
OUT FBA_CLK1P 3.5	1	800FF	FBA_CLK1

OUT FBA_CMDS0 3.5	1	800H	
OUT FBA_CMDS0P 3.5	1	800H	
OUT FBA_CMDS1 3.5	1	800H	
OUT FBA_CMDS1P 3.5	1	800H	
OUT FBA_VIO 3.5	1	800H	
B			

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
OUT FBB_CLK0 3.5	1	800FF	FBB_CLK0
OUT FBB_CLK0P 3.5	1	800FF	FBB_CLK0
OUT FBB_CLK1 3.5	1	800FF	FBB_CLK1
OUT FBB_CLK1P 3.5	1	800FF	FBB_CLK1

OUT FBB_CMDS0 3.5	1	800H	
OUT FBB_CMDS0P 3.5	1	800H	
OUT FBB_CMDS1 3.5	1	800H	
OUT FBB_CMDS1P 3.5	1	800H	
OUT FBB_VIO 3.5	1	800H	
B			

B FBA_DEB0 3	1	800H	
B FBA_DEB0 3	1	800H	
B			

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
B FBAB_PLAVDD 3	1.2V	0.02A	12MIL
B FBA_VREF0 5	1.40V	0.02A	12MIL
B FBA_VREF1 5	1.40V	0.02A	12MIL
B FBA_VREF2 5	1.40V	0.02A	12MIL
B FBA_VREF3 5	1.40V	0.02A	12MIL
B FBA_Z00 5	2.0V	0.02A	12MIL
B FBA_Z01 5	2.0V	0.02A	12MIL

B FBB_VREF0 5	1.40V	0.02A	12MIL
B FBB_VREF1 5	1.40V	0.02A	12MIL
B FBB_VREF2 5	1.40V	0.02A	12MIL
B FBB_VREF3 5	1.40V	0.02A	12MIL
B FBB_Z00 5	2.0V	0.02A	12MIL
B FBB_Z01 5	2.0V	0.02A	12MIL

B FB_VREF1 3	1.40V	0.02A	12MIL
B FB_VREF2 3	1.40V	0.02A	12MIL

NET RULES for FrameBuffer C/D

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
OUT FBC_CLK0 4.7	1	800FF	FBC_CLK0
OUT FBC_CLK0P 4.7	1	800FF	FBC_CLK0
OUT FBC_CLK1 4.7	1	800FF	FBC_CLK1
OUT FBC_CLK1P 4.7	1	800FF	FBC_CLK1

OUT FBC_CMDS0 4.7	1	800H	
OUT FBC_CMDS0P 4.7	1	800H	
OUT FBC_CMDS1 4.7	1	800H	
OUT FBC_CMDS1P 4.7	1	800H	
OUT FBC_VIO 4.7	1	800H	
B			

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
OUT FBD_CLK0 4.8	1	800FF	FBD_CLK0
OUT FBD_CLK0P 4.8	1	800FF	FBD_CLK0
OUT FBD_CLK1 4.8	1	800FF	FBD_CLK1
OUT FBD_CLK1P 4.8	1	800FF	FBD_CLK1

OUT FBD_CMDS0 4.8	1	800H	
OUT FBD_CMDS0P 4.8	1	800H	
OUT FBD_CMDS1 4.8	1	800H	
OUT FBD_CMDS1P 4.8	1	800H	
OUT FBD_VIO 4.8	1	800H	
B			

B FBD_DEB0 4	1	800H	
B FBD_DEB0 4	1	800H	
B			

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
B FBBD_PLAVDD 4	1.2V	0.02A	12MIL
B FBC_VREF0 7	1.40V	0.02A	12MIL
B FBC_VREF1 7	1.40V	0.02A	12MIL
B FBC_VREF2 7	1.40V	0.02A	12MIL
B FBC_VREF3 7	1.40V	0.02A	12MIL
B FBC_Z00 7	2.0V	0.02A	12MIL
B FBC_Z01 7	2.0V	0.02A	12MIL

B FBD_VREF0 5	1.40V	0.02A	12MIL
B FBD_VREF1 5	1.40V	0.02A	12MIL
B FBD_VREF2 5	1.40V	0.02A	12MIL
B FBD_VREF3 5	1.40V	0.02A	12MIL
B FBD_Z00 5	2.0V	0.02A	12MIL
B FBD_Z01 5	2.0V	0.02A	12MIL

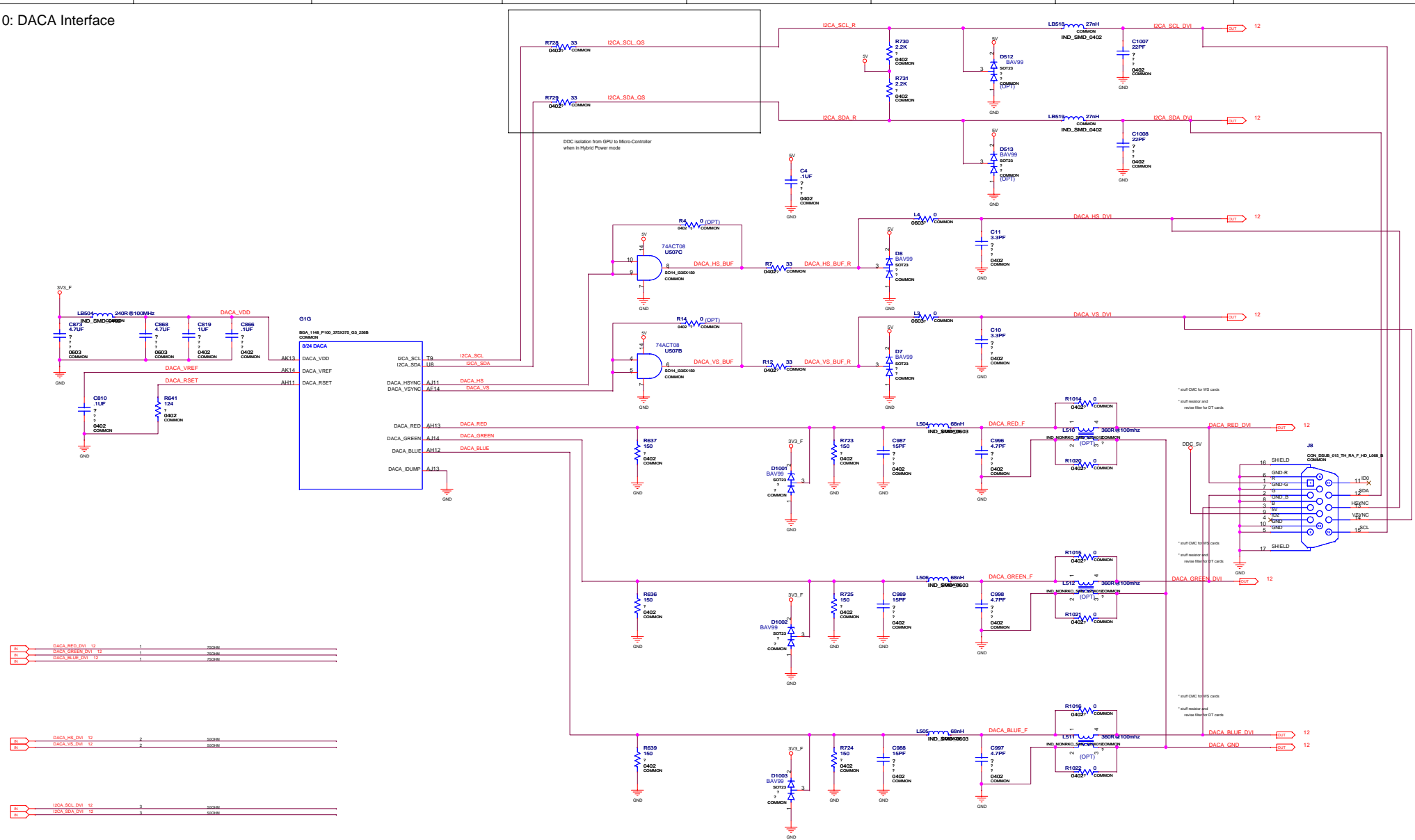
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ASSEMBLY
PAGE DETAIL

FOU - BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO SHIP ASSEMBLY NOTES AND BOM NOT FINAL
FrameBuffer Net Rules



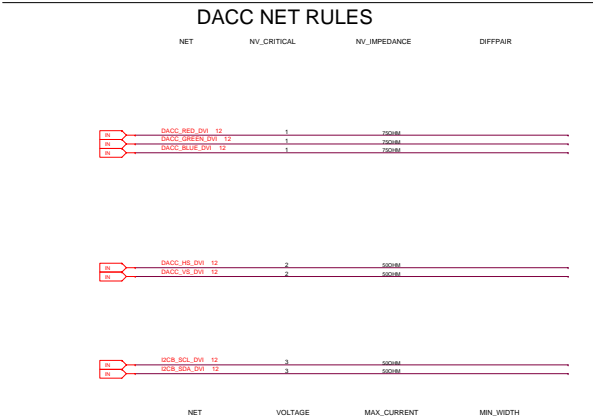
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Size	Document Number	Rev	
Custom	<Doc>	<Rev Code>	
Date:	Friday, December 14, 2007	Sheet	9 of 27



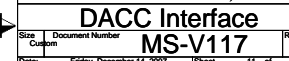
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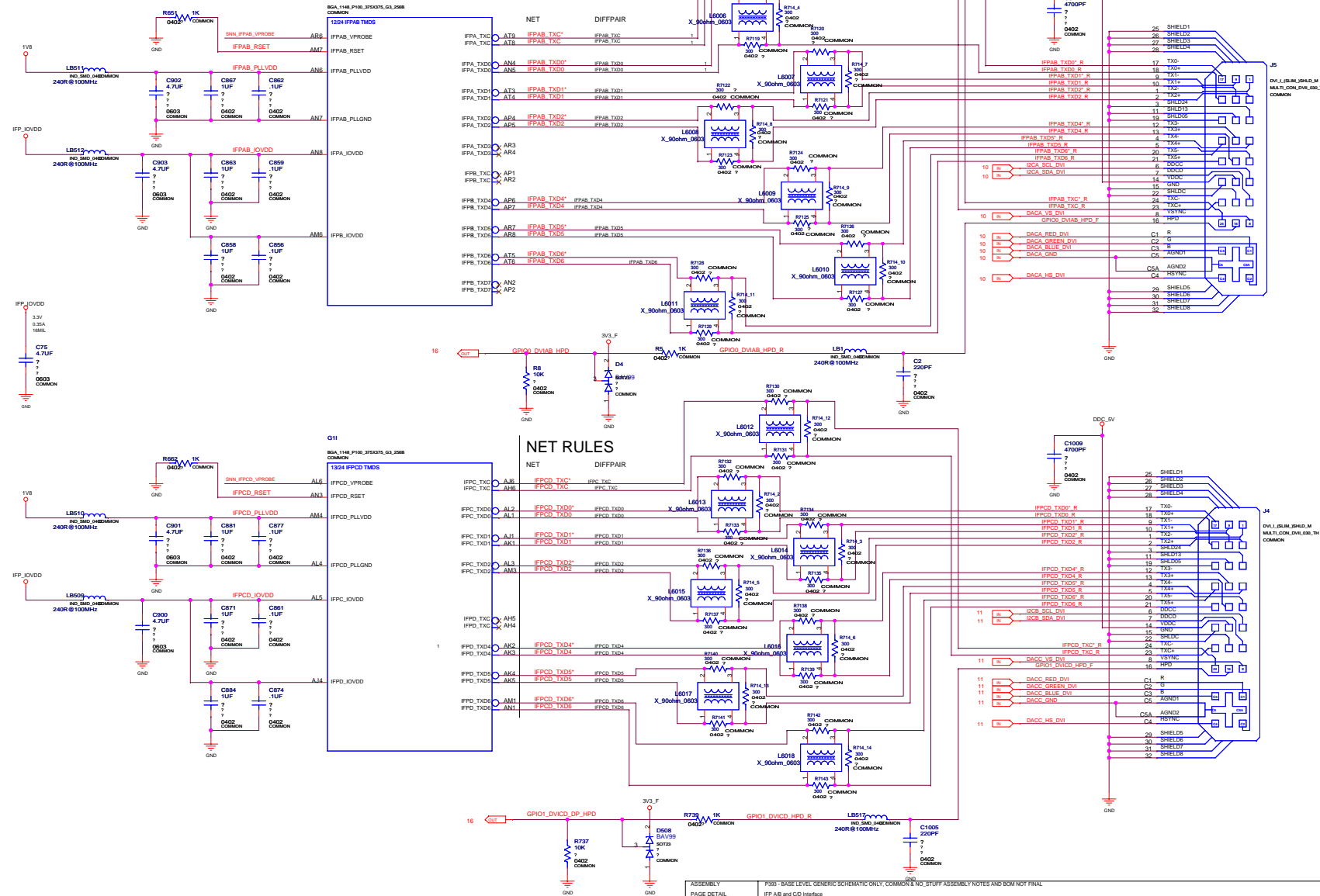
ASSEMBLY	P303 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA Interface





ASSEMBLY	P300 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC Interface





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NOTE:
Bond can be used for EMI purposes

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ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB and Stereo Interface



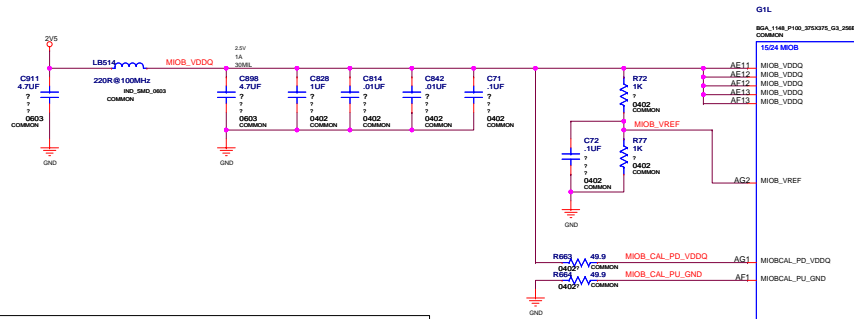
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DACB and Stereo Interface

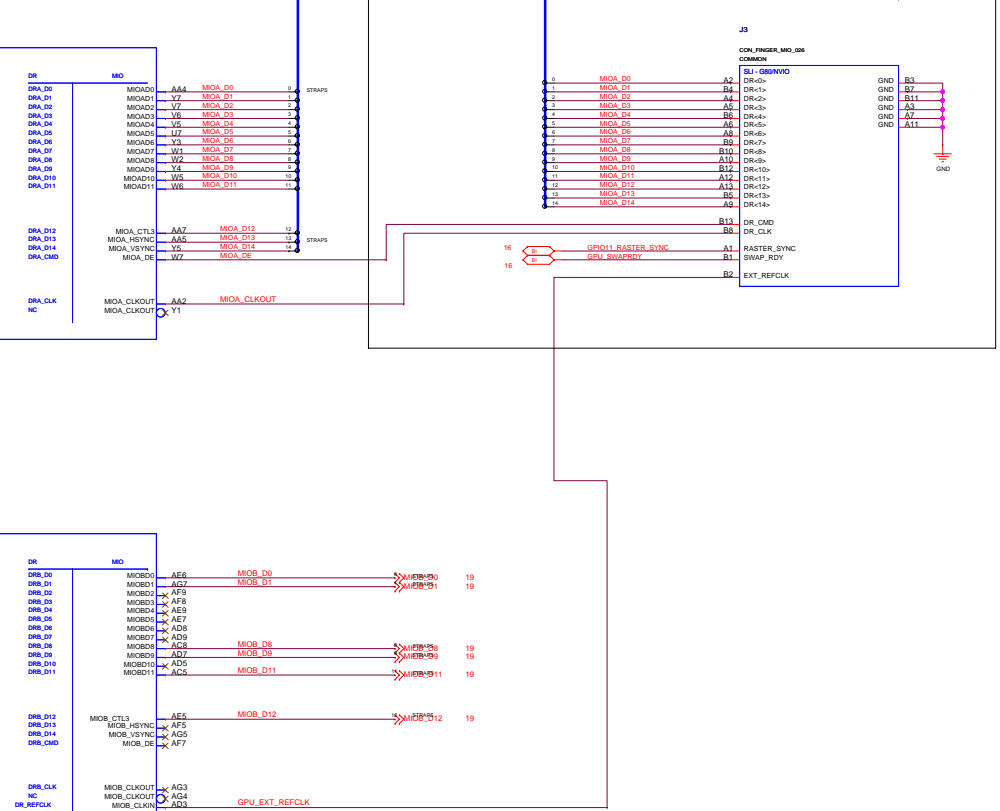
MS-V117


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NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
MIDA_D[14..]_19	1	500UM	



	Micro-Star International Co., LTD.		
	Multi-use IO(MIO) Interface		
	Size	Document Number	Rev
	Custom	MS-V117	1.0
Date:	Expiry: December 14, 2007	1 Sheet	1 of 1

Page15: Display Port (Analogix ANX9802/ANX9805)

* DCC keepers circuit removed

* ANX9805 support

pin 76 - GPIO3 to DP mode, from pin 13, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 74 - GPIO2, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 73 - DCC support via I2C and pull-up, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 71 - SPOUT1 - tie to GND, input select 01 through internal register

pin 70 - SPOUT0 - support for Audio input, grounded on ANX9802
- place GND resistor away from ANX device if needed

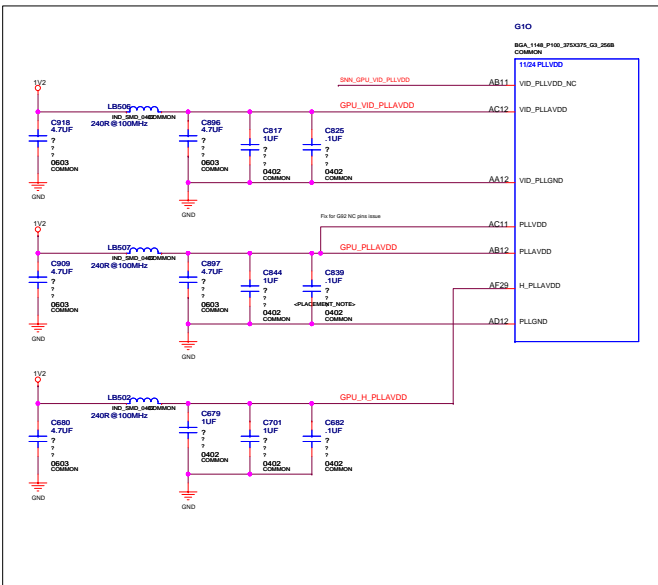
pin 68 - NC - tie to GND

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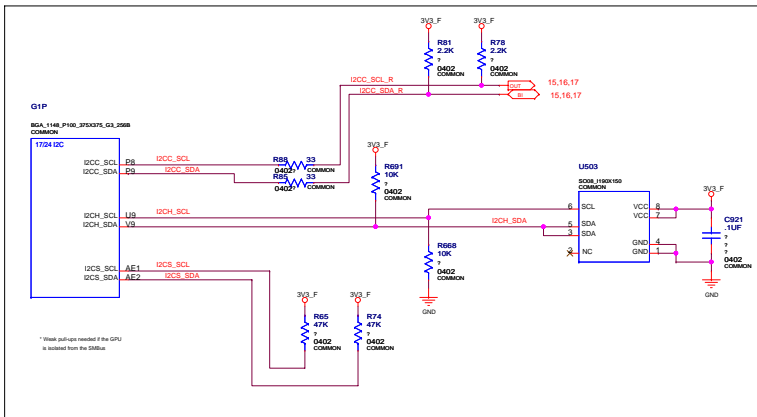
ASSEMBLY	PORT - BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO-STEP ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display Port



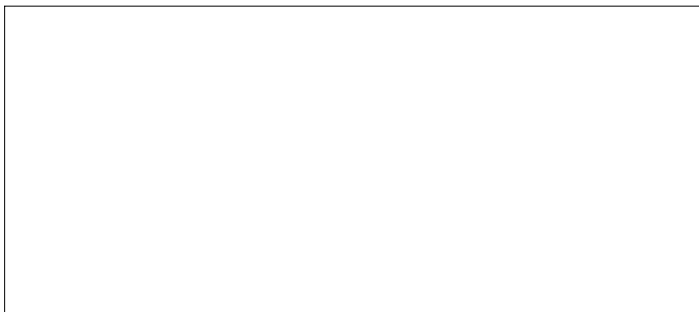
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Date:	Friday, December 14, 2007	Sheet	15 of 27



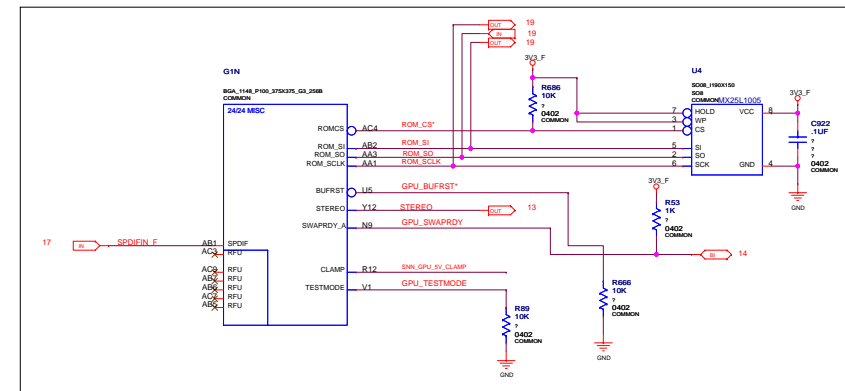
I2CS isolation for Hybrid Power



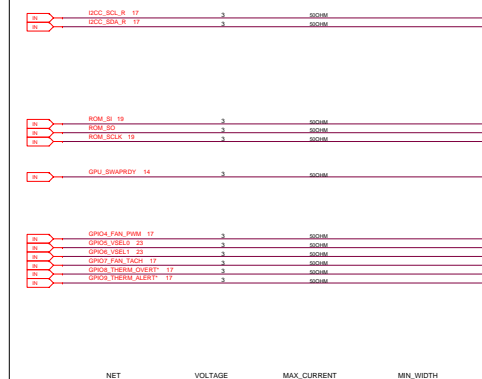
I2CS isolation for Hybrid Power



(BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)

[illegible]

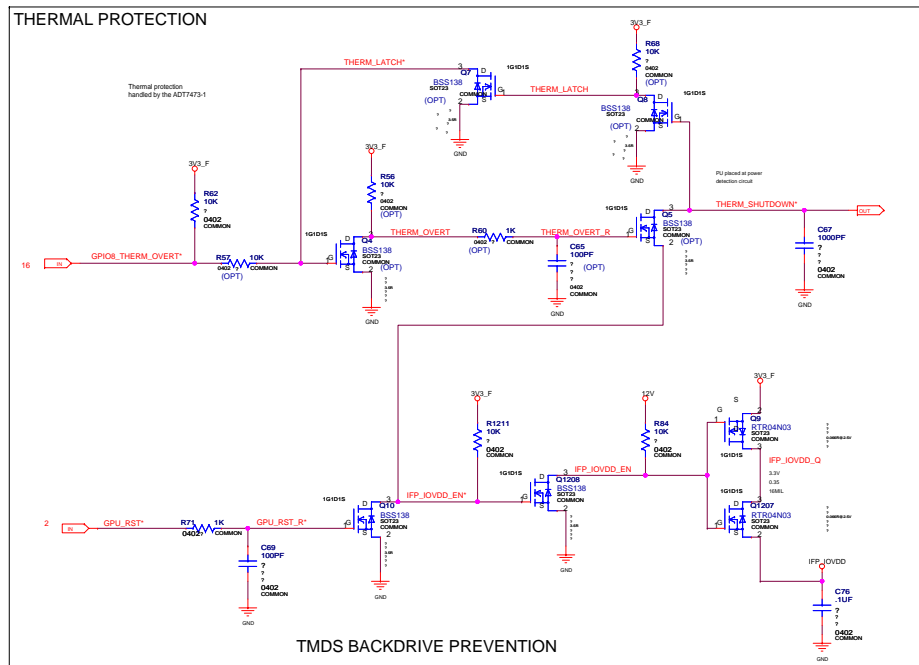
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98	0	0	0
99	0	0	0



The schematic diagram illustrates the internal structure of the Q1R module. The module is represented by a blue rectangle with four pins: AD2 (top left), AD1 (bottom left), AB3 (top right), and AC1 (bottom right). Inside the module, a 16Q4 XTL crystal is connected between AD2 and AD1. A 27 MHz oscillator (Y1) is connected between AD1 and AC1. A 330V capacitor (C77) is connected between AC1 and ground. A 10K resistor (R52) is connected between AD2 and ground. A 330V capacitor (C78) is connected between AD1 and ground. The module is connected to a 5V supply (V5) and ground (GND). The external components are labeled as follows: R52 (10K), C78 (330V), C77 (330V), Y1 (27 MHz), and V5 (5V). The module is also connected to a 5V supply (V5) and ground (GND) through a 330V capacitor (C77) and a 10K resistor (R52).

GPIO	I/O	Function
0	IN	DVI Hoping Detect South
1	IN	DVI or DP Hoping Detect Mid
2	IN	Framebuffer Interrupt
3	BI	Framebuffer GPIO#0 Dongle Detect
4	OUT	Fan PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fan Tach Input
8	OUT	THERM_OVERT*
9	IN	THERM_ALERT*
10	OUT	DisplayPort Interrupt
11	OUT	RASTER (SL) SYNC
12	IN	POWER_ALERT*
13	OUT	DP IC Keeper
14	IN	Framebuffer SYNC

THERMAL PROTECTION

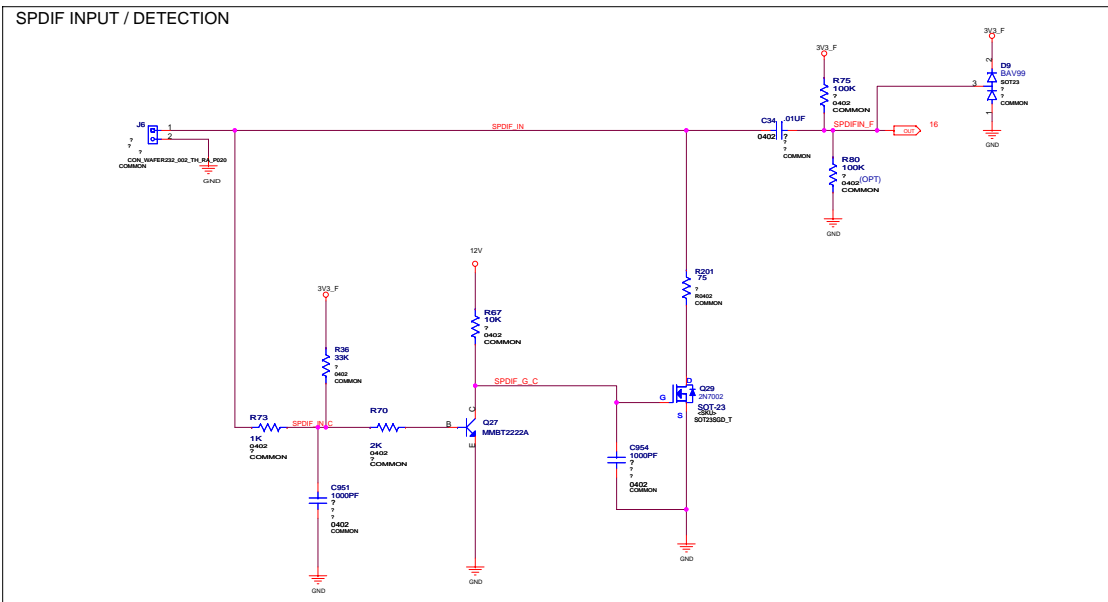


Scaling possibilities for thermal control and protection

2) ADT7473 is COMMON

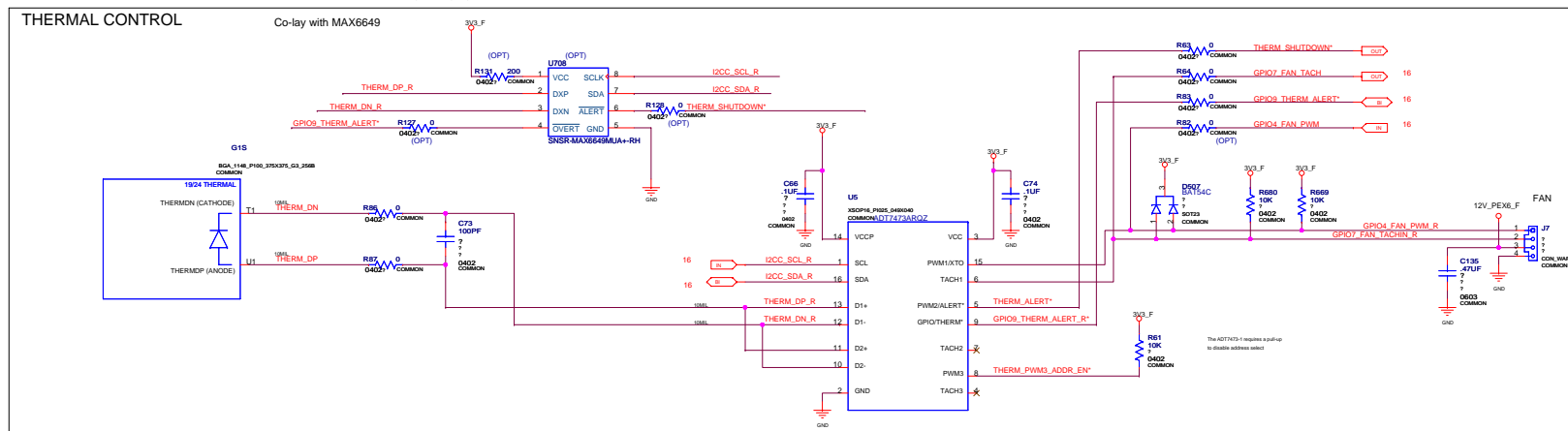
GPIO4 is not used.
GPIO7 is the tach input from the fan
GPIO9 is the thermal alert for GPU slowdown.
With a newer version of the ADT chip, PWM2 can optionally be used for shutdown

SPDIF INPUT / DETECTION



THERMAL CONTROL

Co-lay with MAX6649



The FAN connector needs to move
as follows for mechanical / ID support:

- * move -43mils in Y
- * move +33mils in X

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Control/Protection and SPDIF Input



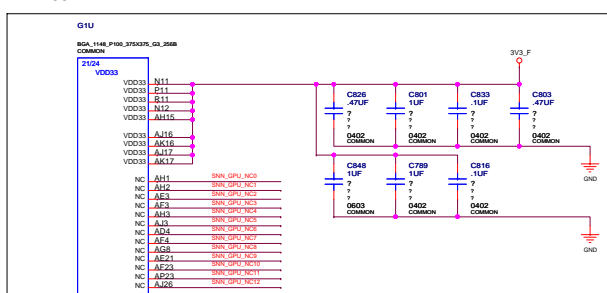
	Micro-Star International Co., LTD.
	Thermal Control/Protection and SPDIF Input

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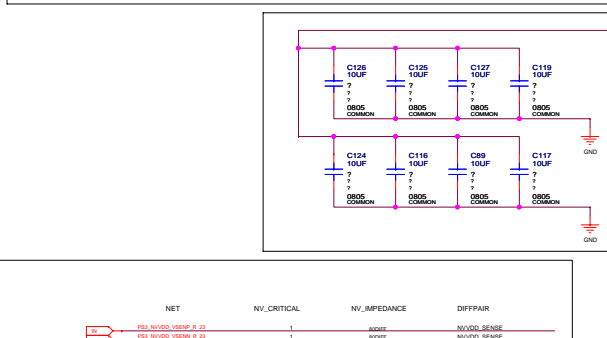
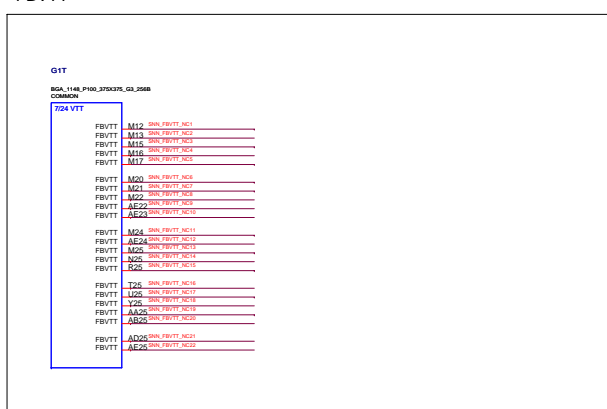
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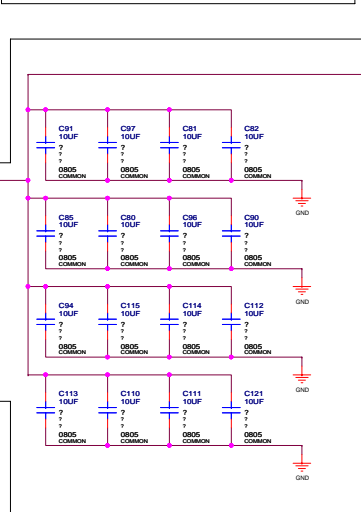
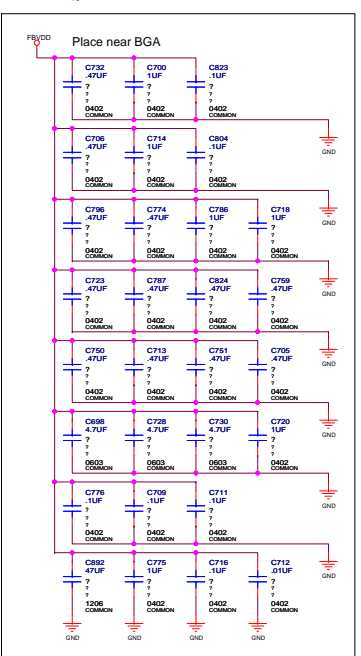
VDD33



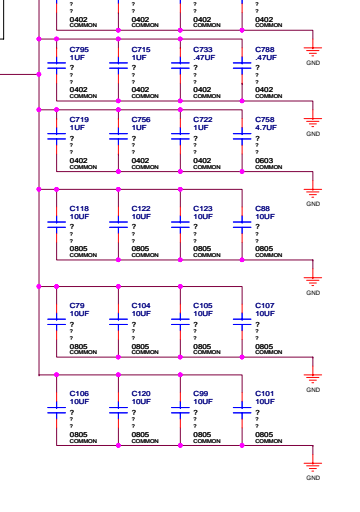
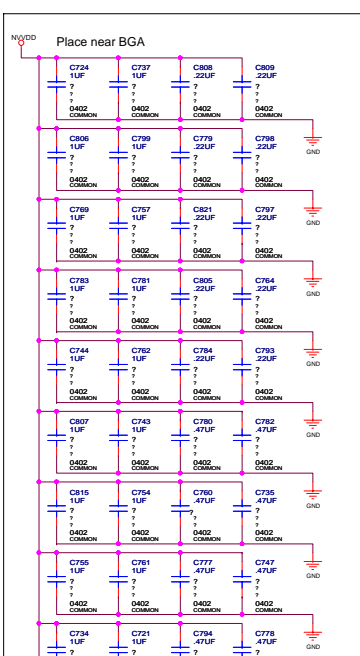
FBVTT



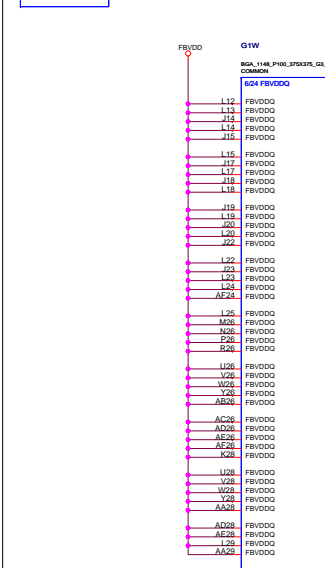
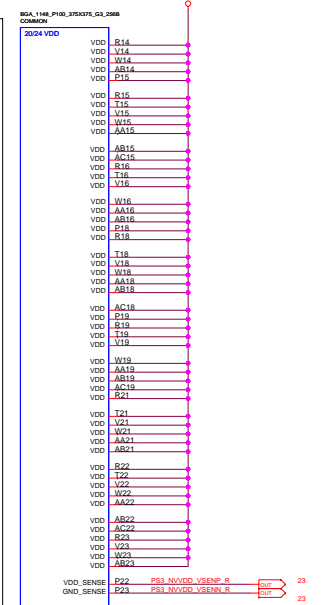
FBVDDQ



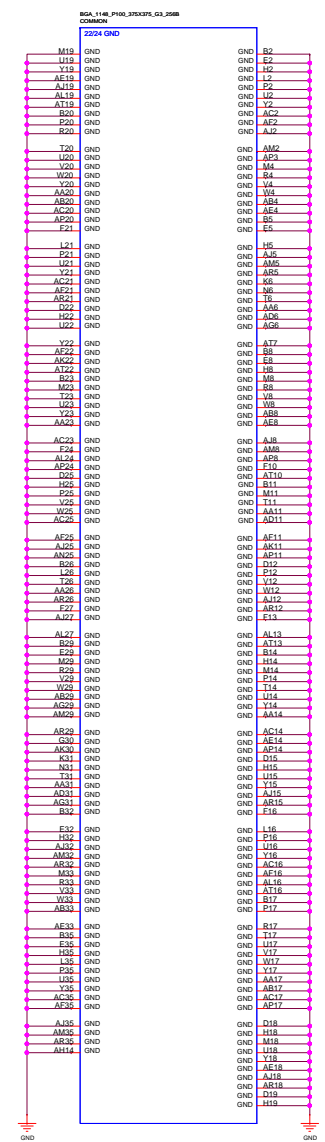
NVVDD



G1V



G1X



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ASSEMBLY	P193 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power/GND and Decoupling



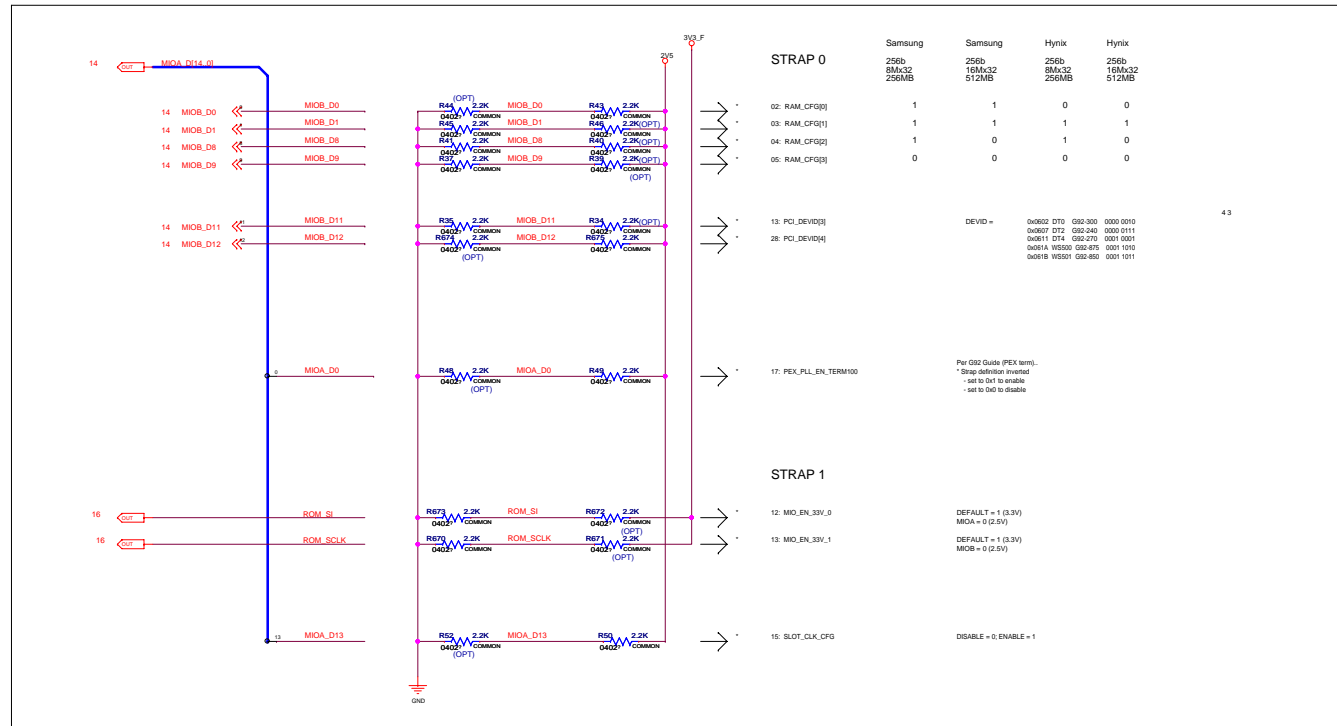
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Power/GND and Decoupling

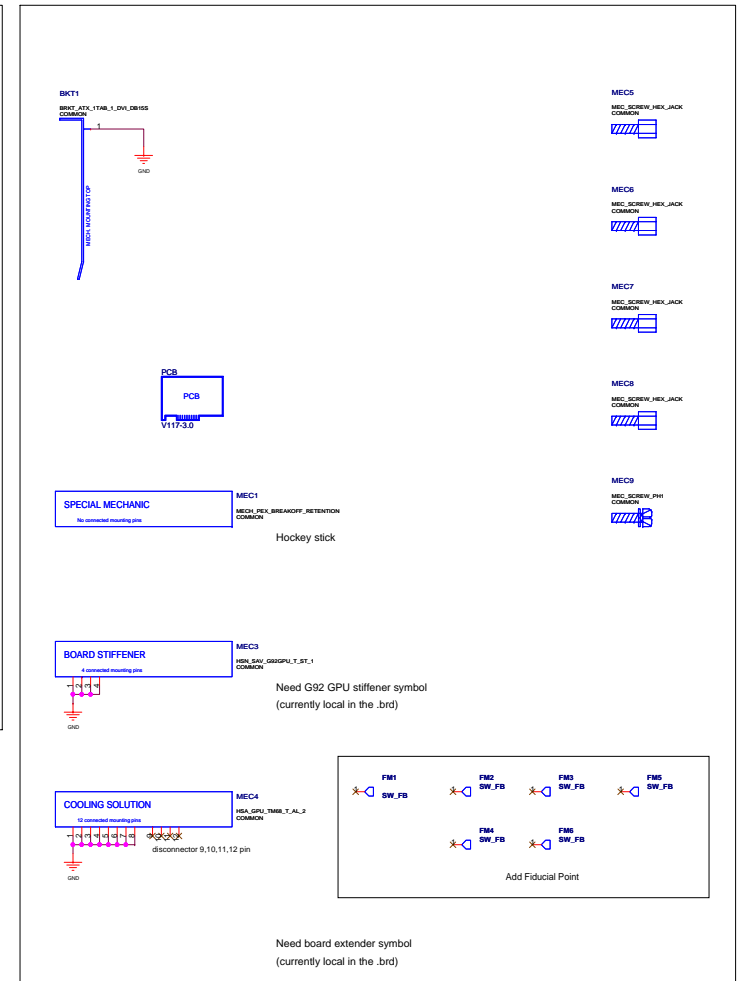
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Custom	MS-V117

Date: Friday, December 14, 2007 Sheet 18 of

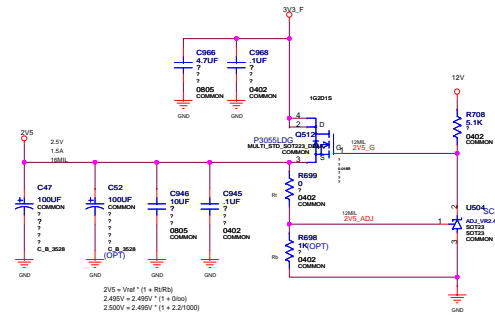
STRAPS



MECHANICAL

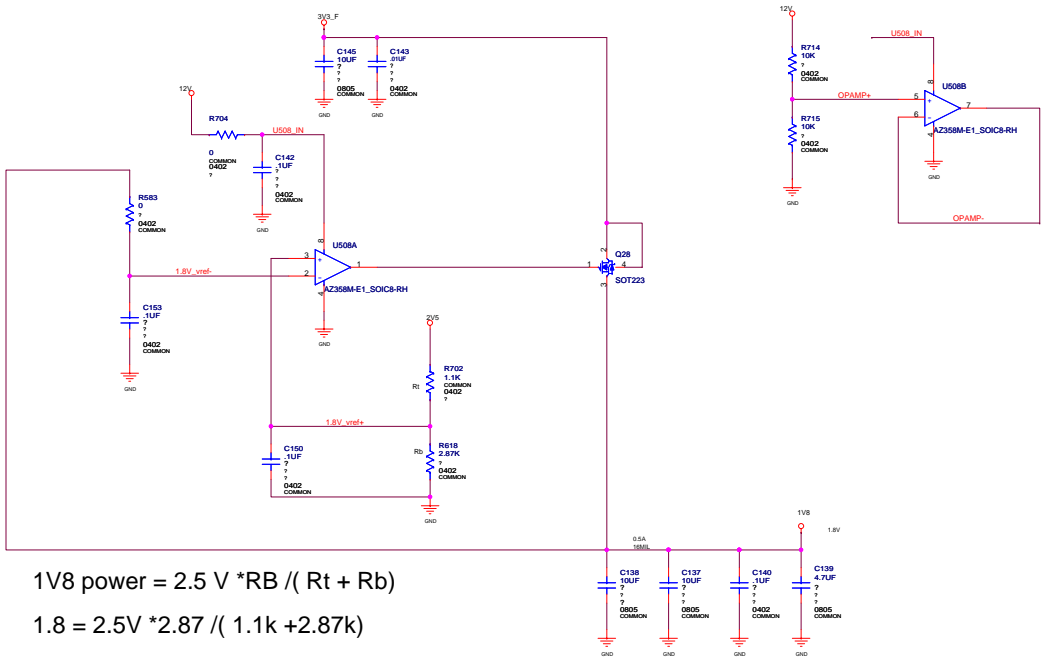


2V5 Supply


$$\begin{aligned} 2V_5 &= V_{ref} * (1 + R_t/R_b) \\ 2.495V &= 2.495V * (1 + 0/\infty) \\ 2.500V &= 2.495V * (1 + 2.2/1000) \end{aligned}$$

ASSEMBLY	P303 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 5V, STEREO_5V, 2V5, DP_PWR

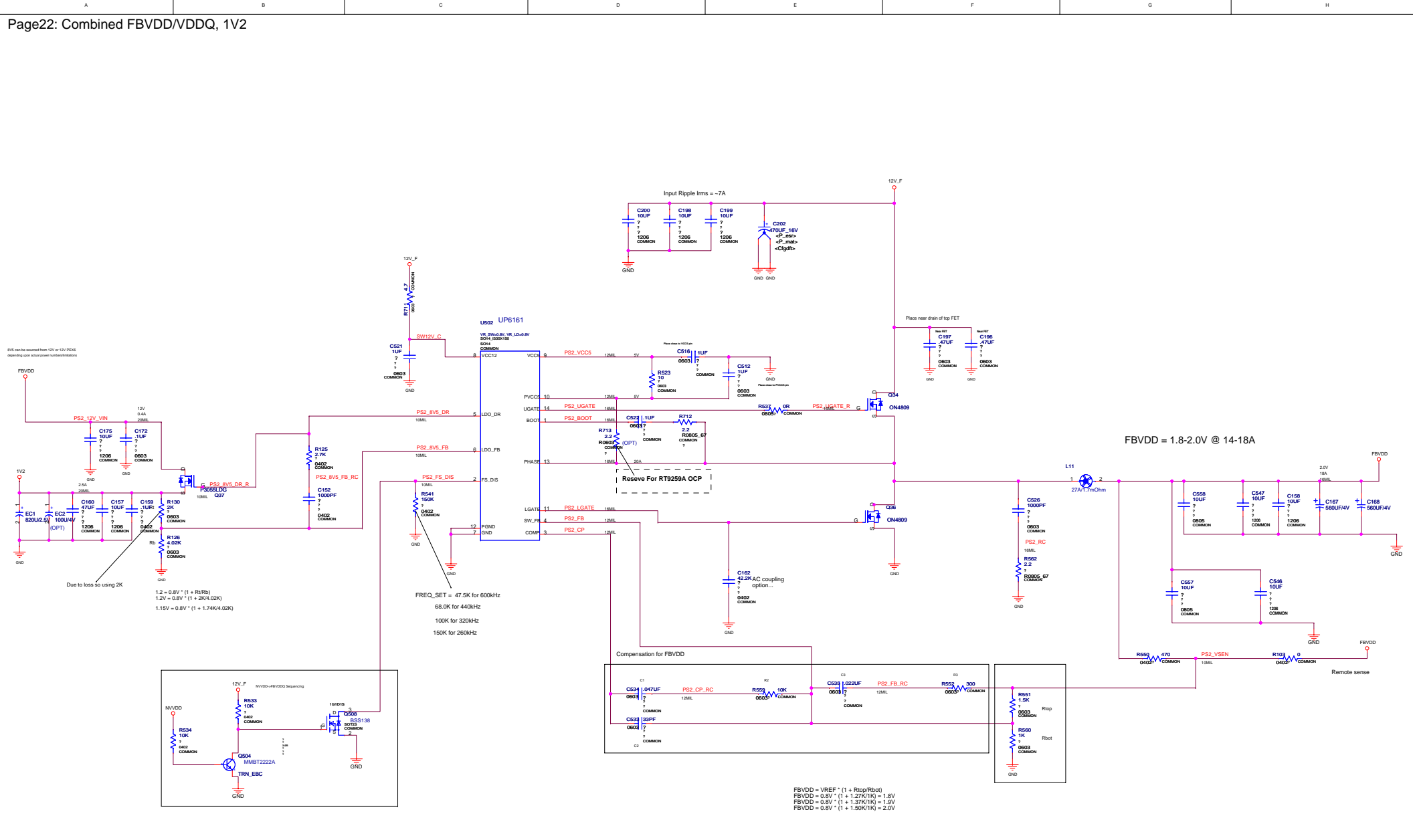




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ASSEMBLY
PAGE DETAIL
PUSH: BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO-STOP ASSEMBLY NOTES AND BOM NOT FINAL
Power Supply 1V2, 1V8

Micro-Star International Co., LTD.			
1V8			
Size	Document Number	Rev	RevCode
Custom	MS-V117		
Date	Friday, December 14, 2007	Sheet	21 of 27

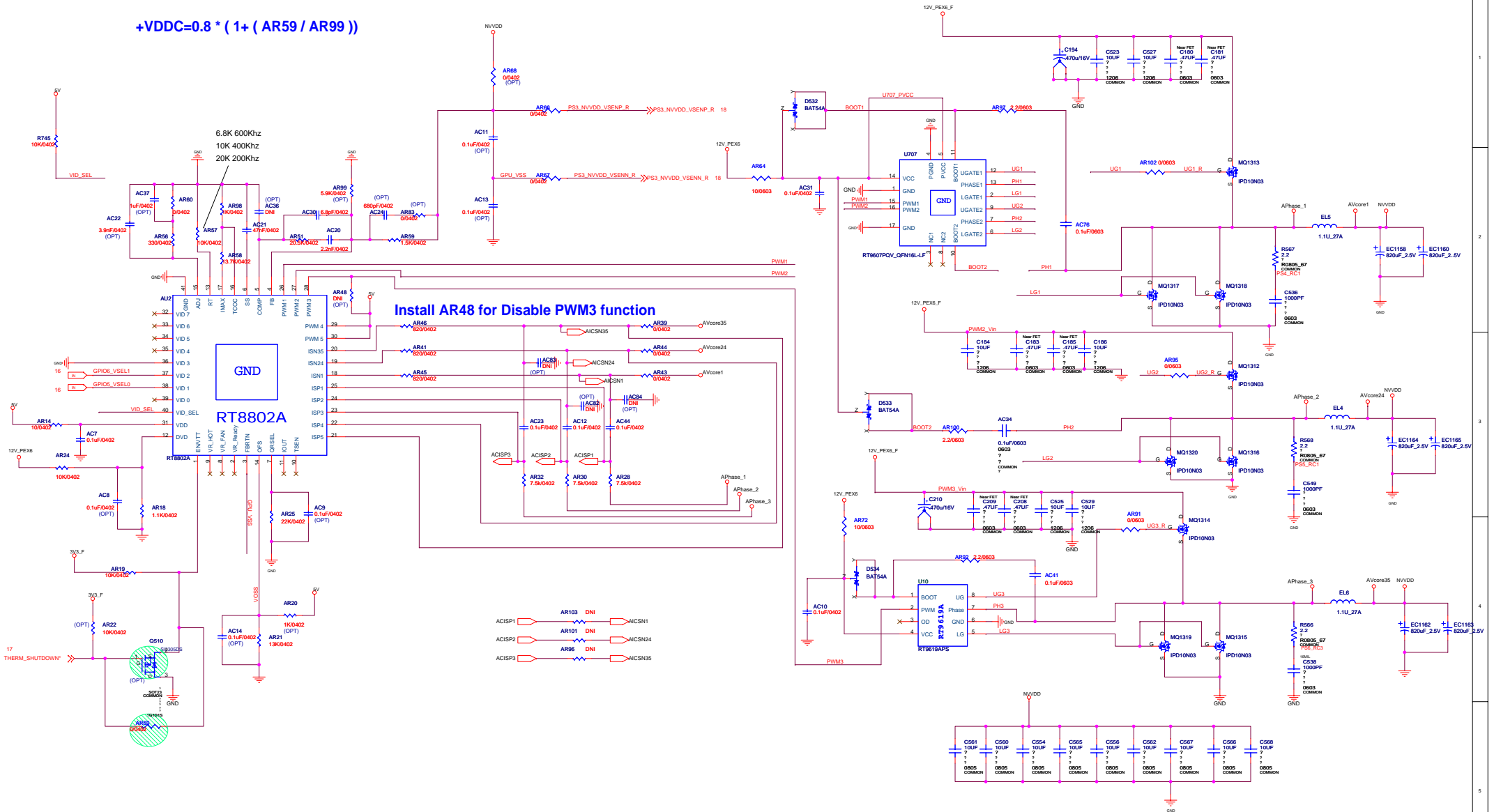


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ASSEMBLY	P303 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: FBVDDIQ, 8V5



$$+VDDC=0.8 * (1 + (AR59 / AR99))$$



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ASSEMBLY PAGE DETAIL
PWB: BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO-STOP ASSEMBLY NOTES AND BOM NOT FINAL
Power Supply NVVDD Regulator

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		NVVDD	
Size	Document Number	Rev	
Custom	V117	Rev 0	
Date	Friday, December 14, 2007	Sheet	23 of 27

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ASSEMBLY	POWER - BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO-STEP ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply NVVDD Phase 1 & 2



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Date:	Friday, December 14, 2007	Sheet	24 of 29

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ASSEMBLY
PAGE DETAIL

POWER - BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO-STEP ASSEMBLY NOTES AND BOM NOT FINAL
Power Supply NVVDD Phase 1

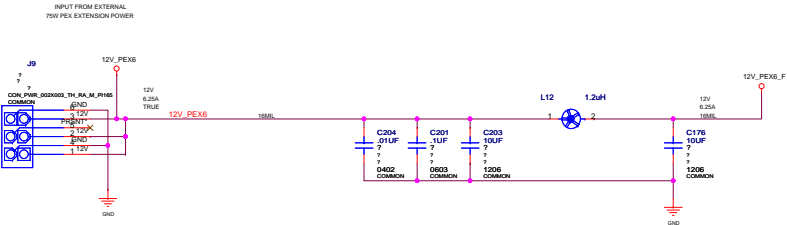
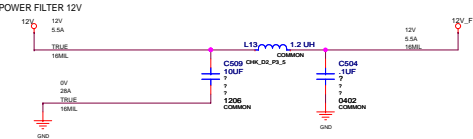
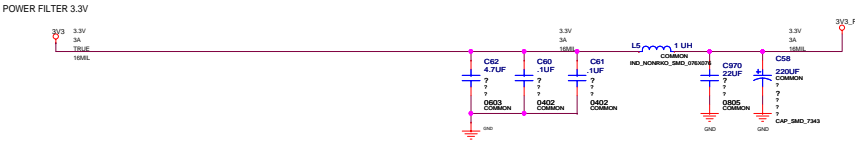


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Date	Friday, December 14, 2007
Sheet	25 of 27

Rev

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ASSEMBLY PAGE DETAIL P381-6A3E[LEVEL:GENERIC] SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND/OR NOT FINAL Power Supply: Filter/Detection of 3V3, 12V, 12V_PEX6

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3V3,12V,12V_PEX

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Date: Friday, December 14, 2007 15:28:27

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Rev 27

Weak pull-ups needed for DCS:
* If SMBus is isolated from the GPU
* If MB does not support SMBus
* If MB does not support 3V3ALX

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ASSEMBLY	POWER - BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO-STEP ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply Hybrid Power



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Size	Document Number		Rev
Custom	<Doc>		<RevCode>
Date:	Friday, December 14, 2007	Sheet 27 of 27	