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Drawn By			Draw No: 2c008
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A

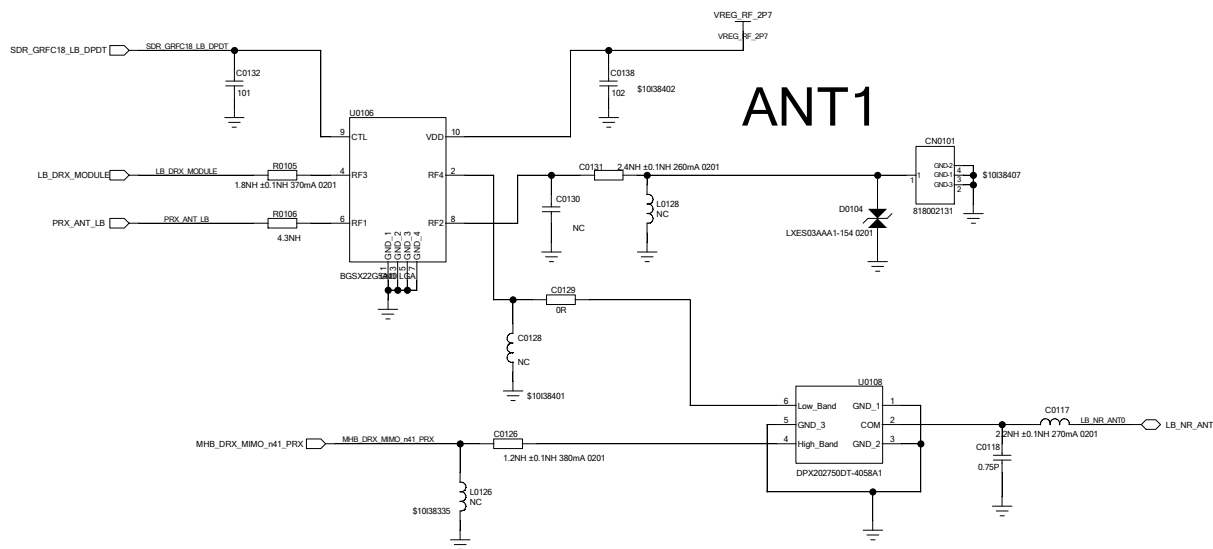
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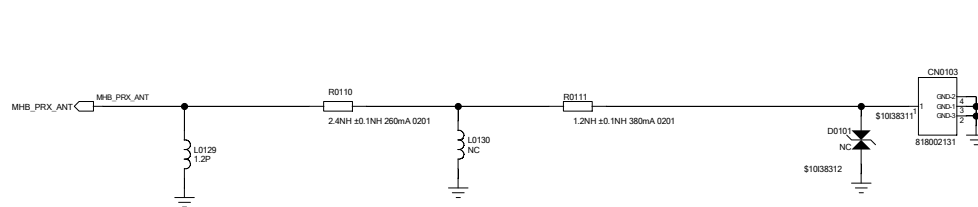
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ANT4

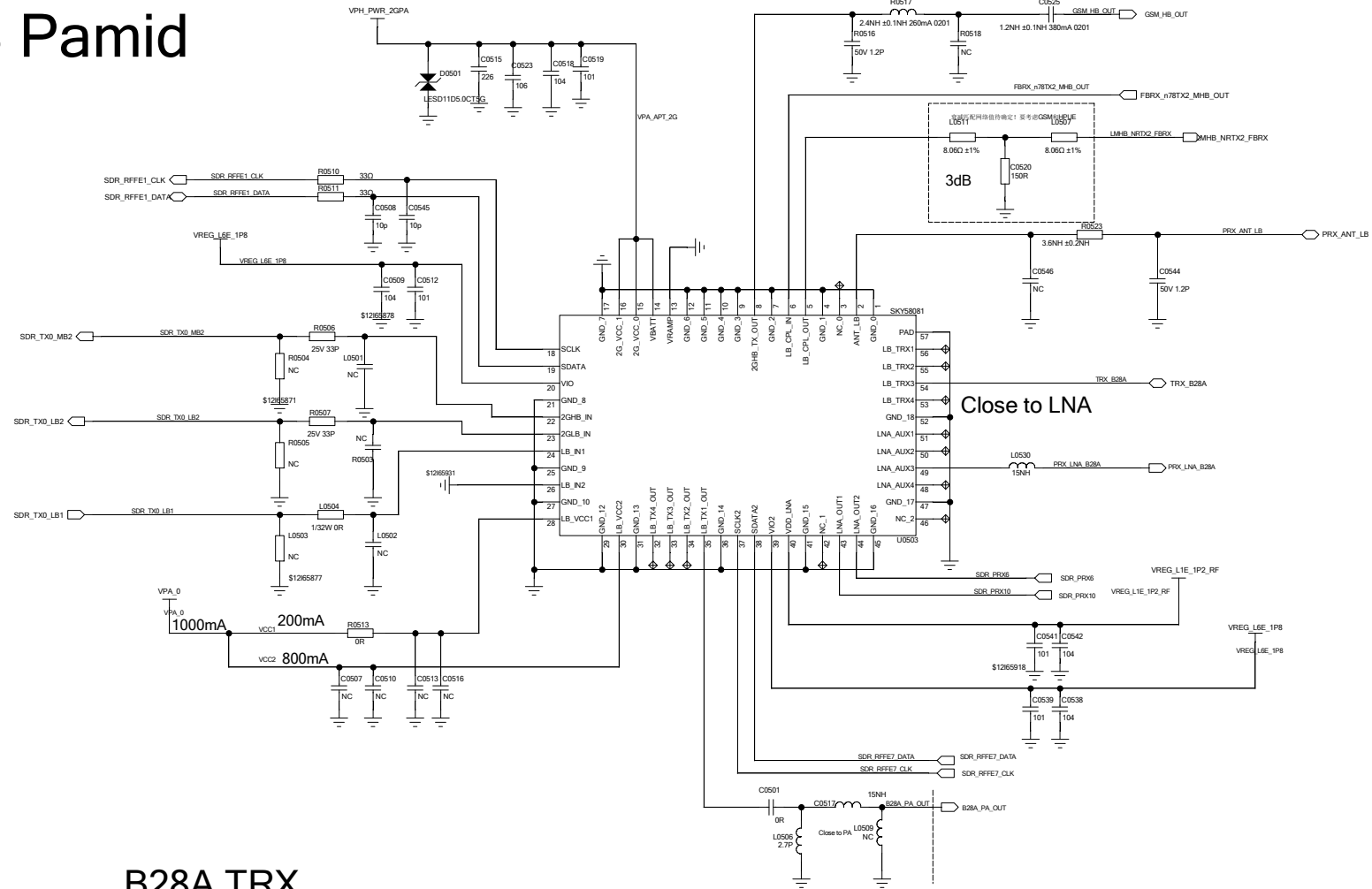
NFC



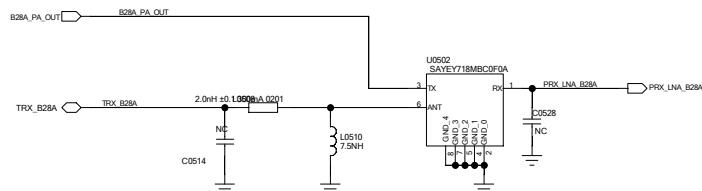
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Standard By			
Approved By			




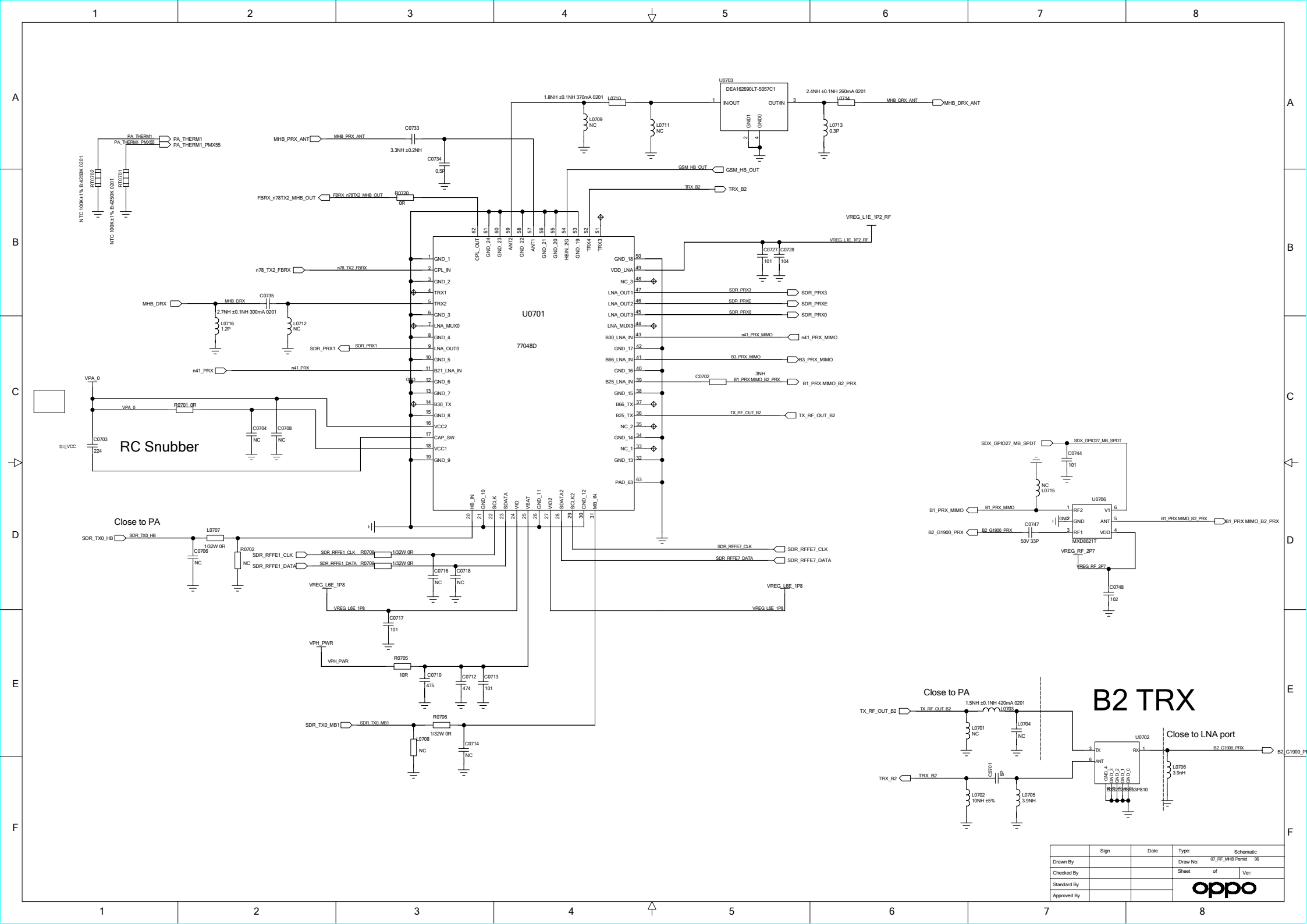
LB Pamid

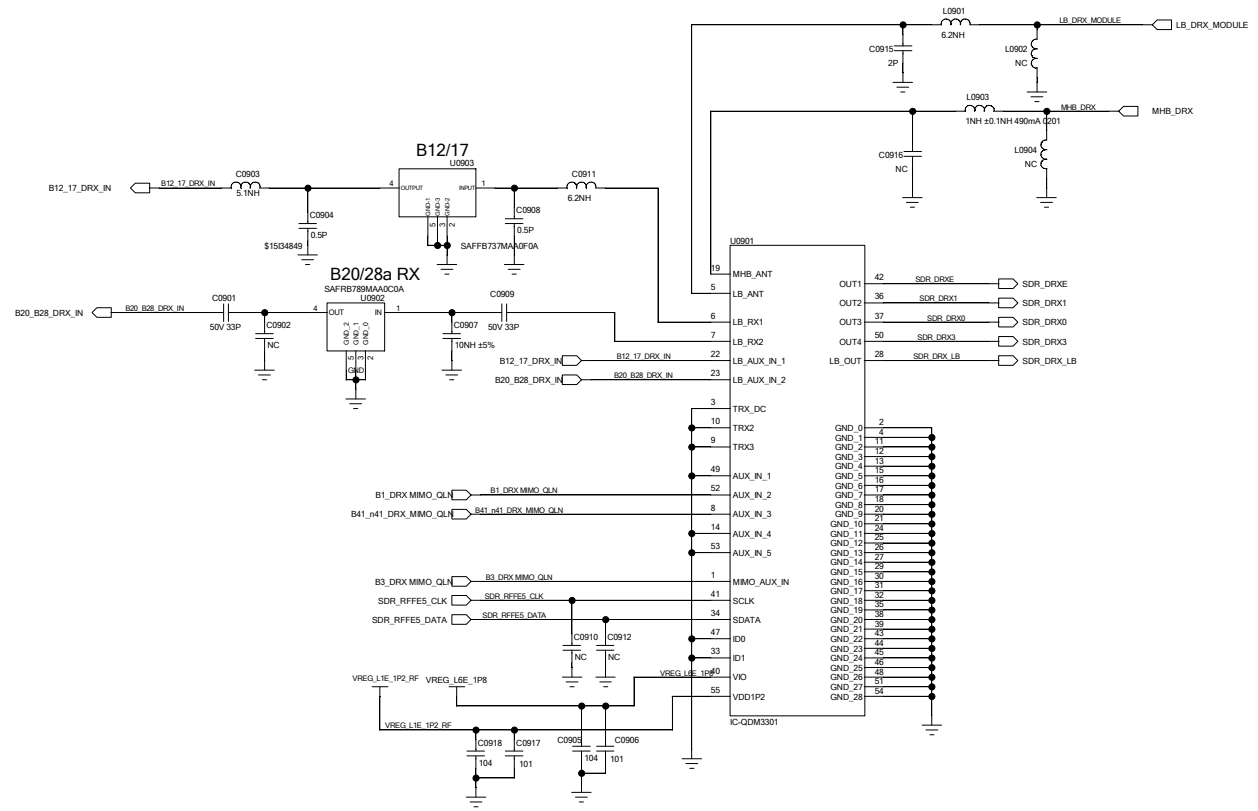


B28A TRX



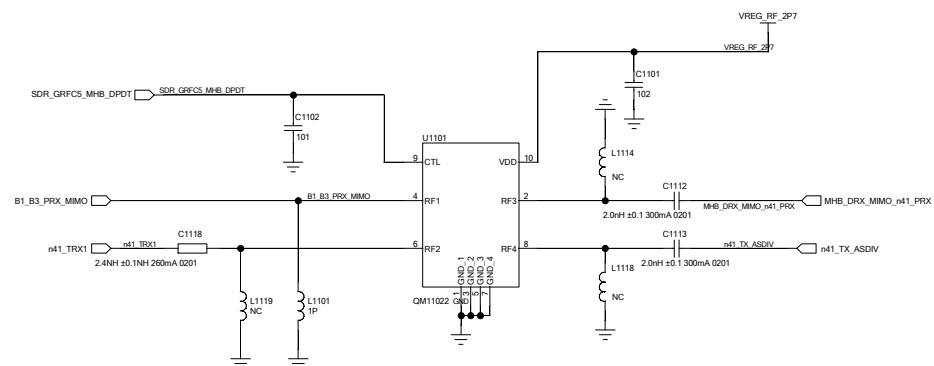
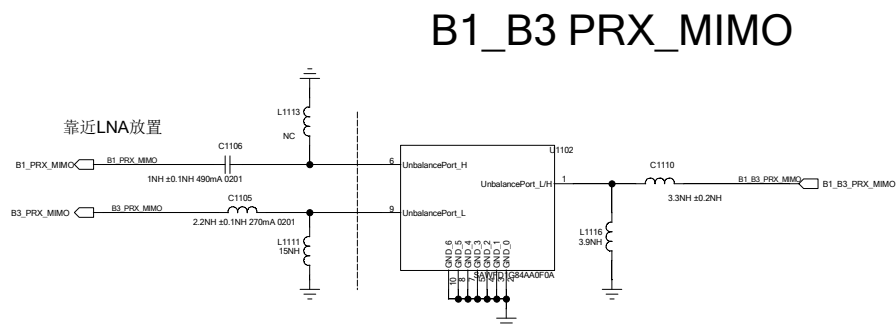
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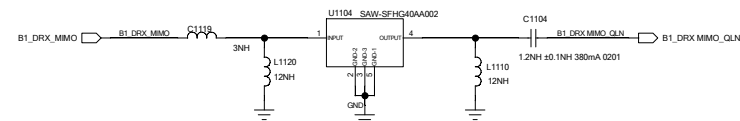
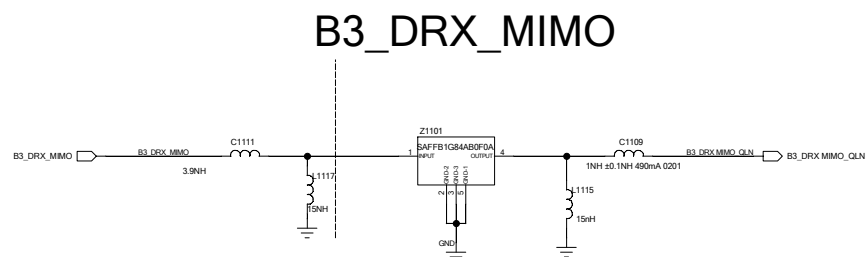
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Standard By			
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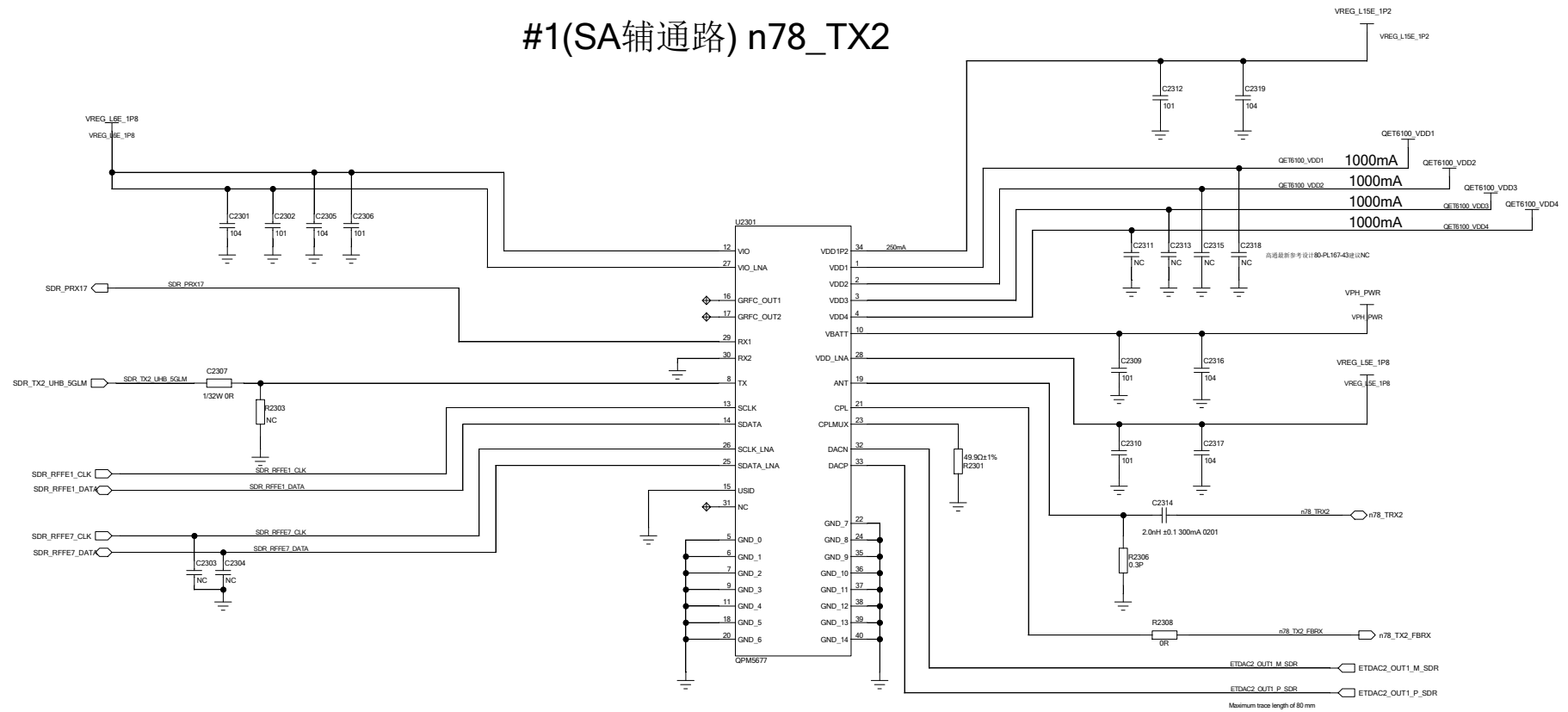
DRX MIMO


B1_DRX_MIMO



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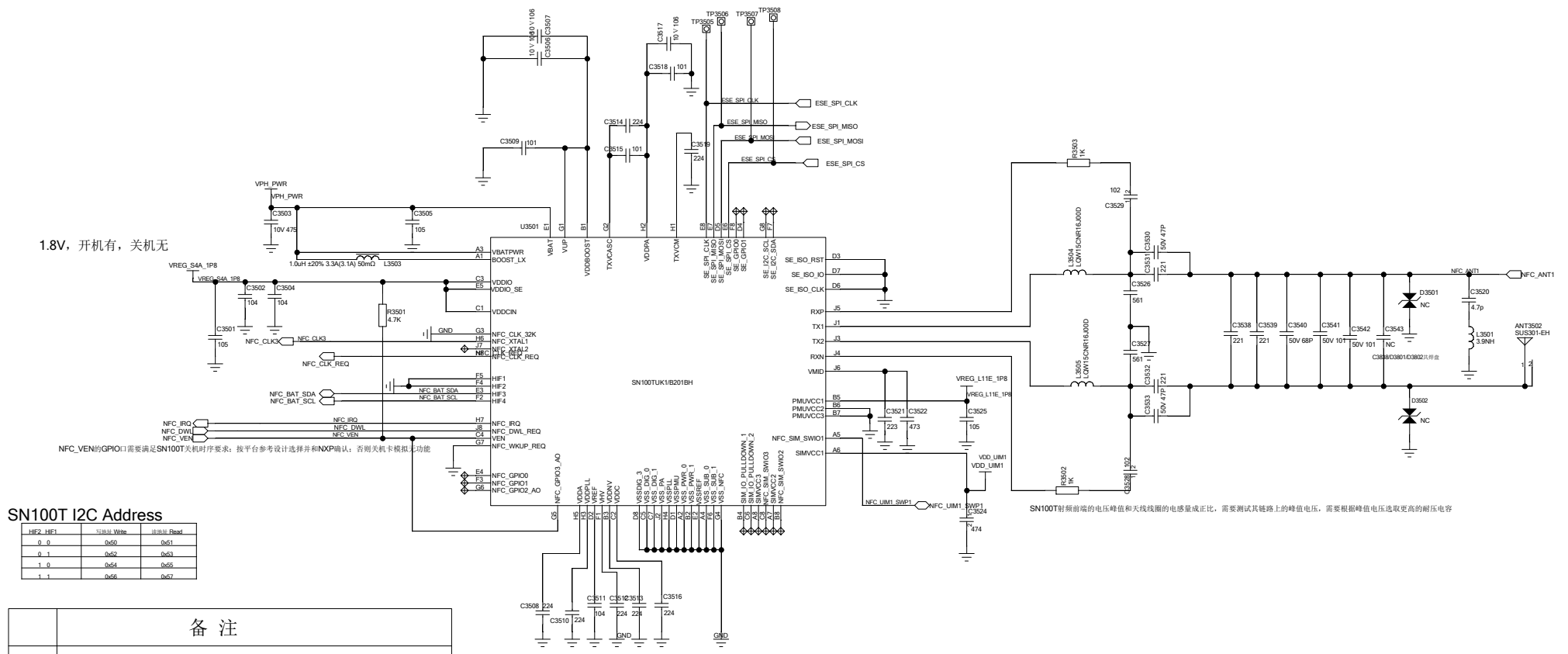
#1(SA辅通路) n78_TX2



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Standard By			
Approved By			

NFC高配版兼容共体方案

1.8V, 开机有, 关机无

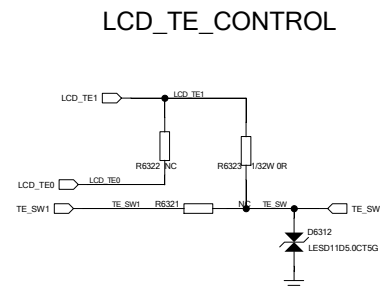
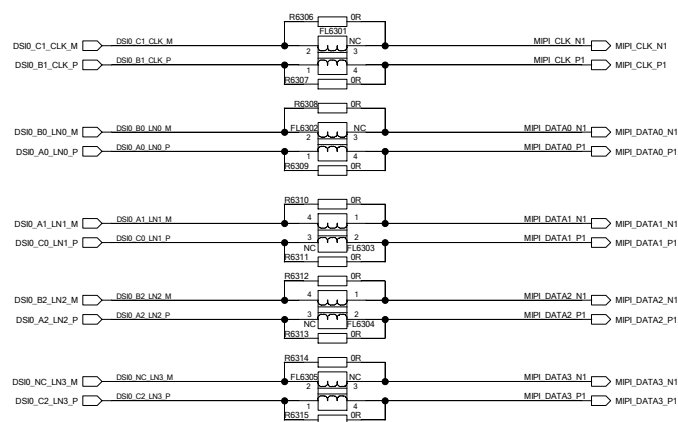
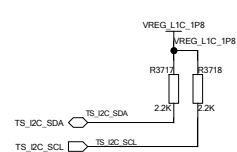
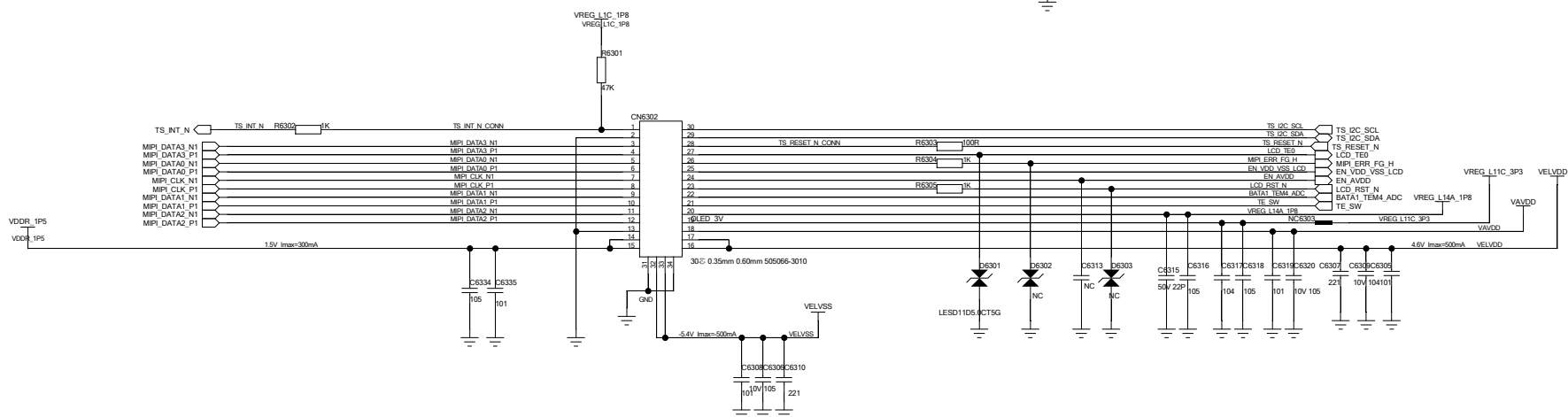
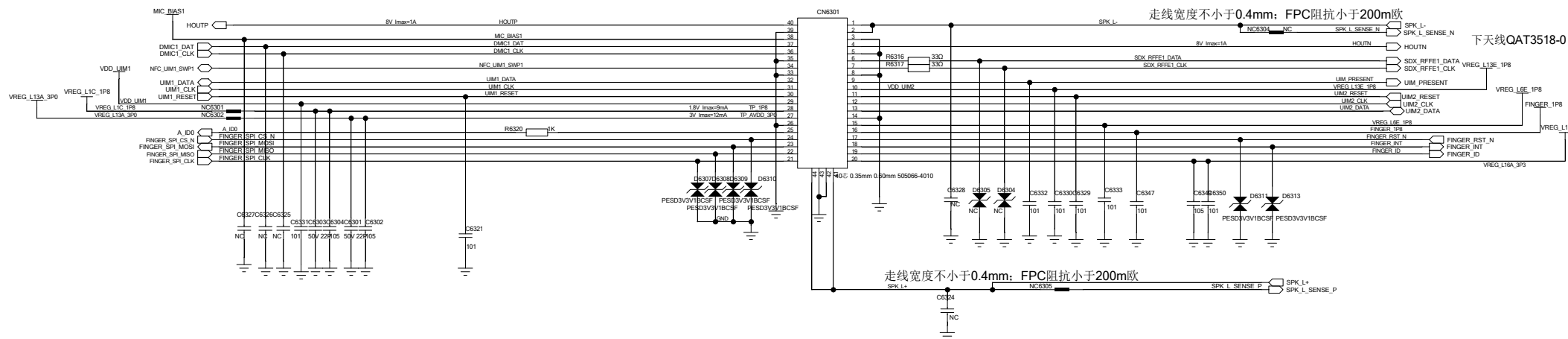


SN100T I2C Address


HF2_HF1	写地址 Write	读地址 Read
0_0	0x50	0x51
0_1	0x52	0x53
1_0	0x54	0x55
1_1	0x56	0x57

备注	
1	SN100T single die 内部集成NFC Controller+eSE+DC/DC; 如不需要DC/DC可通过修改cfg 将DC/DC bypass
2	SN100T使用系统时钟, 不需要预留外部晶振, 开关卡模拟性能相同
3	SN100T/F PIN2PIN, 电路图兼容这两个方案; SN100U 与SN100T/F PIN2PIN,但SN100U内部多个eSIM模块D3、D6、D7 三个接口需要接到AP端, SN100T/F这三个接口需要接地:

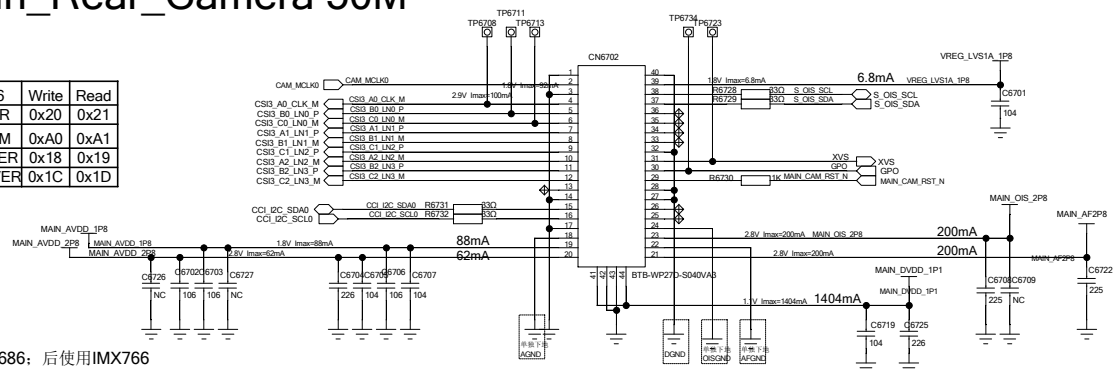
TO_L_FPC_40PIN+30PIN



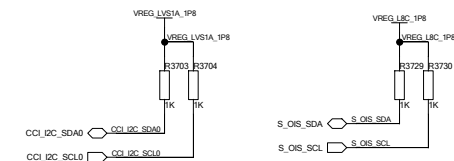
DISPLAY

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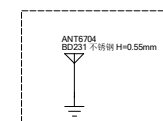
IMX686	Write	Read
SENSOR	0x20	0x21
EEPROM	0xA0	0xA1
AF DRIVER	0x18	0x19
OIS DRIVER	0x1C	0x1D




DVT前使用IMX686; 后使用IMX766
IMX686时AVDD 2.9V; IMX766时AVDD 2.8V

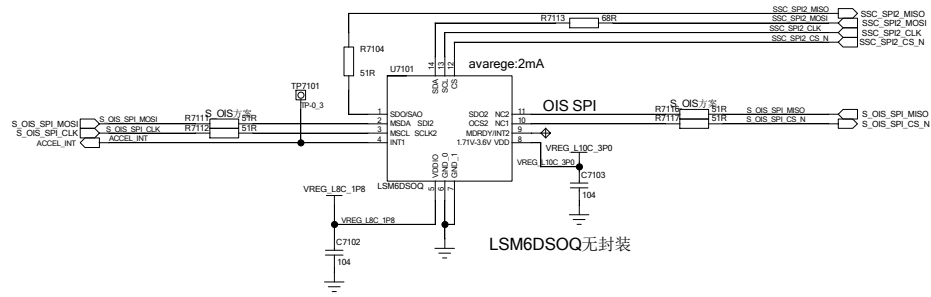


摄像头支架接地弹片



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Approved By			

A+G

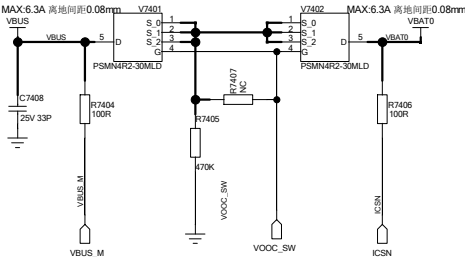
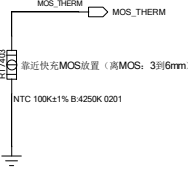
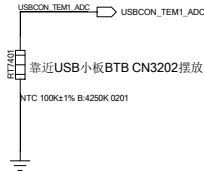


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Fast Charge

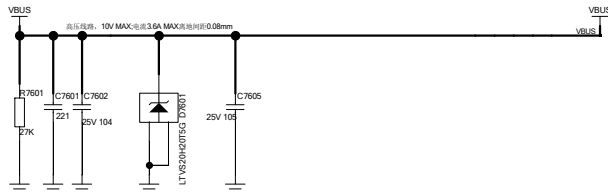
Fast Charge




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Approved By			



USB NVP



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Drawn By			Draw No:	Schematic
Checked By		76, C	76, C	BAT_RST_GRP_SWITCH Ver:
Standard By				
Approved By				

Power Wireless-15W(默认伏达)

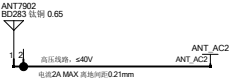
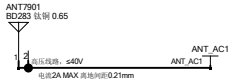


Figure 1: USB Contact Detect Circuit Diagram. The circuit uses a USB_CONTACT_IN pin connected to a diode D8119 (NC) and a resistor R8131 (12K±1%). The output of R8131 is connected to a node that branches to R8132 (88K±1%), R8133 (20K±1%), and a node labeled 'H: No Contact L: Contact'. This node is also connected to R8134 (330K±1%) and R8135 (47K±1%), which are connected to ground. A 100nF capacitor C8134 is connected between the node and ground. The circuit is powered by VREG_S4A (1P8) and VREG_S4B (1P8). A USB103 module is connected to the node, with its VCC, IN, and VEE pins. The USB103 module is also connected to a USB_ACC_INT pin, which is connected to a USB_ACC_INT pin. A 104 capacitor is connected between the USB_ACC_INT pin and ground. The circuit is designed to detect the presence of a USB contact by measuring the voltage drop across the resistors and the current through the diode.

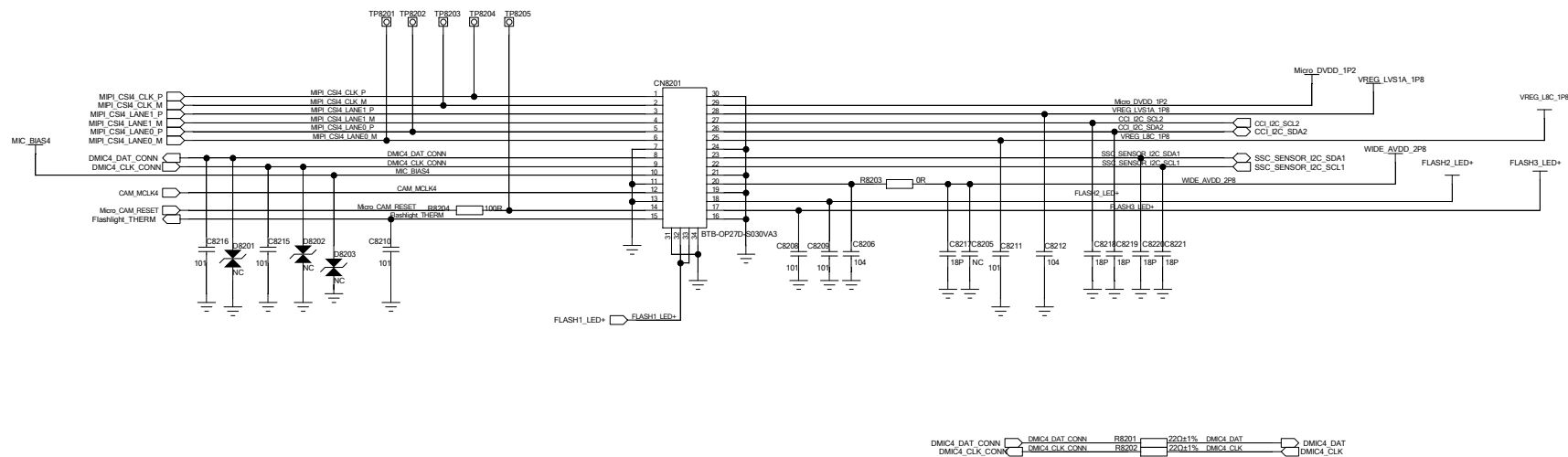
The USB3.1 schematic diagram illustrates the electrical connections for a USB3.1 port. It includes a detailed view of the C8101 connector pinout, showing signals such as USB_CONTACT_IN, USB_TEMP_ADC1, USB_SBU2_CONN_1, USB_GSBU2_1, USB_SBU1_CONN_1, USB_GSBU1_1, USB_TEMP_ADC2, and various USB SS, RX, TX, and DP pins. The diagram also shows the internal wiring and component placement, including capacitors (C8102, C8106, C8104, C8136, C8108, C8118), diodes (ESD6391CN-2/TR, DFN0402, ES03K08-CN-2/ES03K08-2N, LESB9H12CT5G), and a TVS diode (V8US). A note specifies that C8121/C8122 should be placed close to BTB. A warning at the bottom states: "TVS使用Vrwm>=10V的型号，注意TVS寄生电容值+CC线上电容的总容值不超过600pF".


[illegible]

补光灯、色温传感器、闪光灯、背部MIC

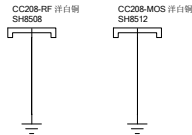
SSC_SENSOR_IC_SDA1

SSC_SENSOR_IC_SCL1



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屏蔽支架



BTB扣合支架



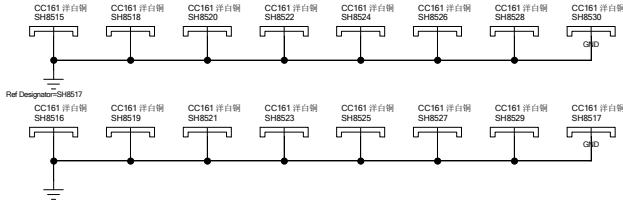
螺钉垫片



RF Cable线夹

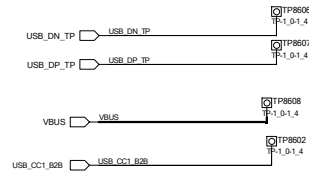


3板4板焊接垫片



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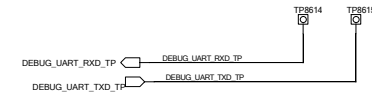
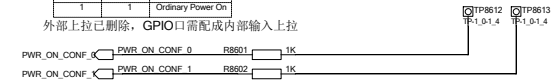
TEST POINT



综测校准测试点 BOOT MODE

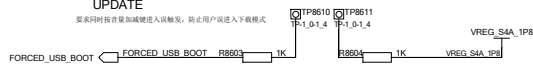
CONF. 0	CONF. 1	Mode
0	0	Factory Mode
0	1	WLAN Final Test
1	0	RF mode
1	1	Ordinary Power On

外部上拉已删除，GPIO口需配成内部输入上拉



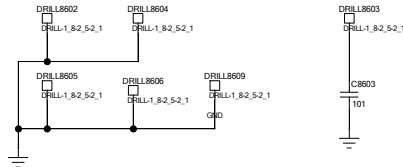
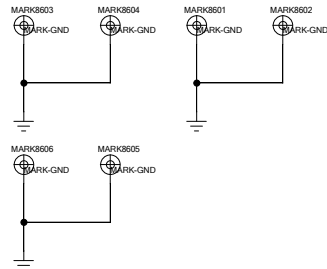
UPDATE

要求同时按住增加键进入该模式，防止用户误进入下载模式



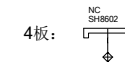
MARK POINT

MTG



高温锡膏贴片

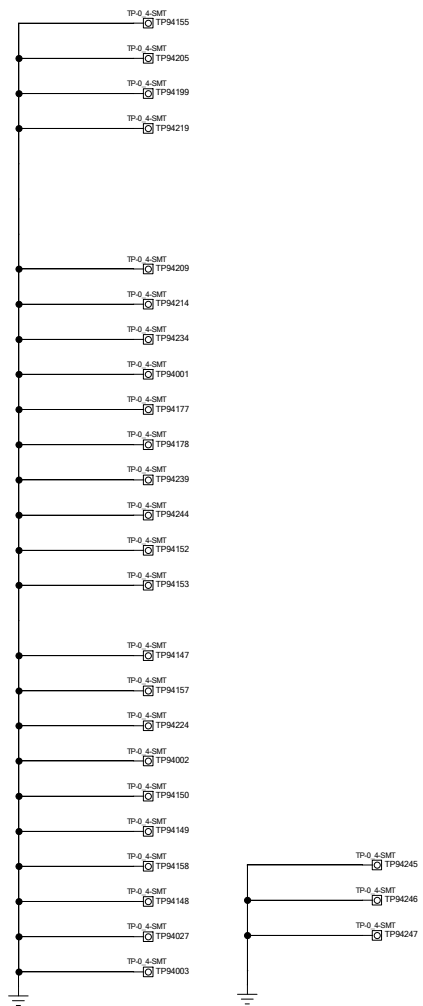
低温锡膏贴片



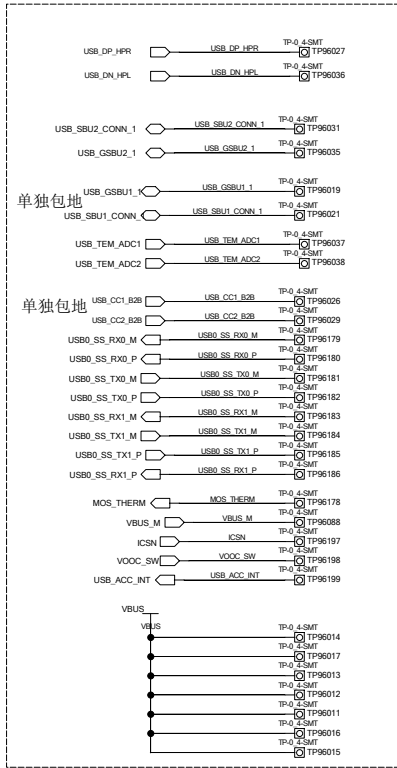
MARK POINT

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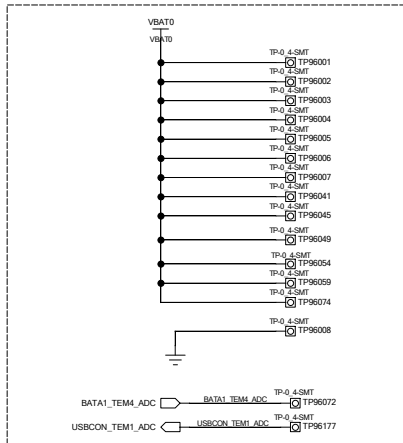
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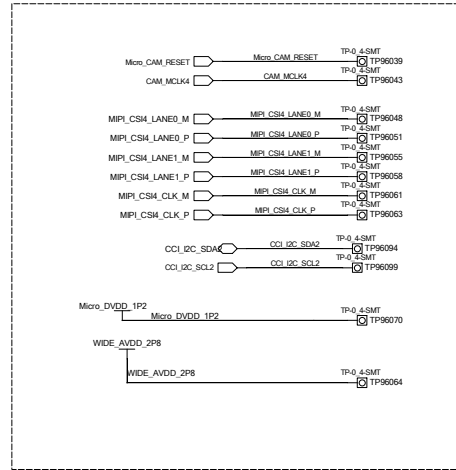
USB CONN



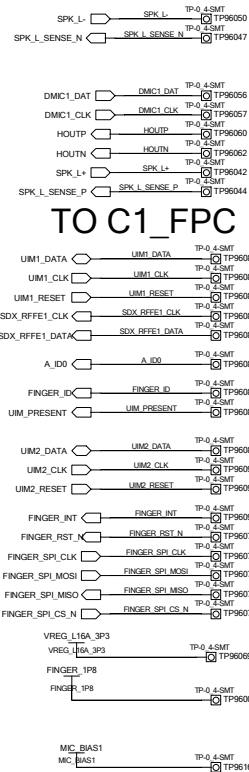
BAT CONN



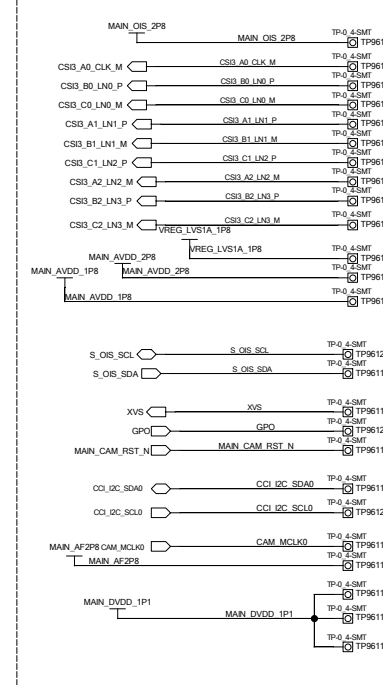
Micro CAM CONN



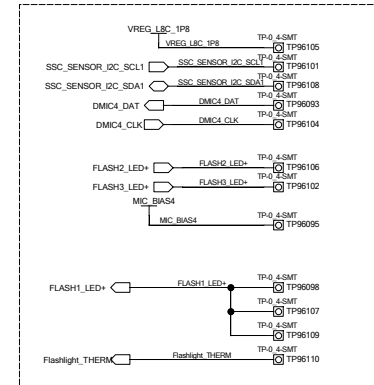
MAIN FPC CONN



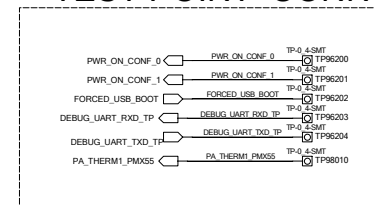
MAIN CAM CONN



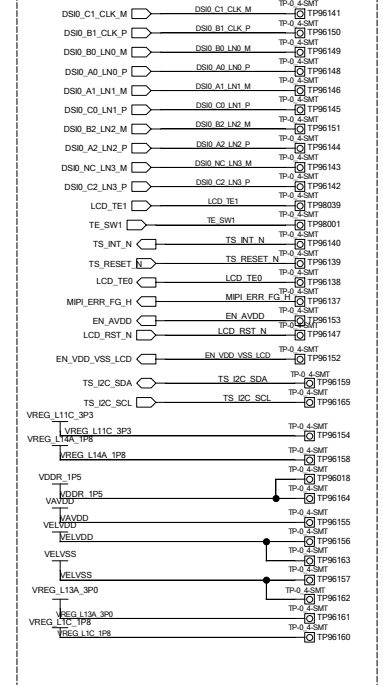
SENOSR FPC CONN



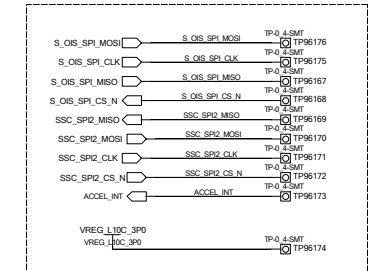
TEST POINT CONN



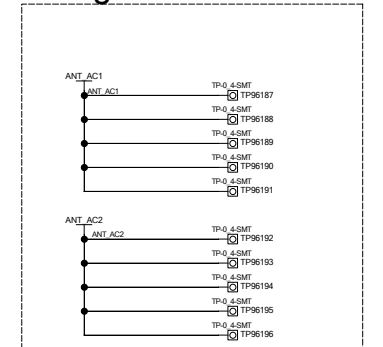
OLED CONN



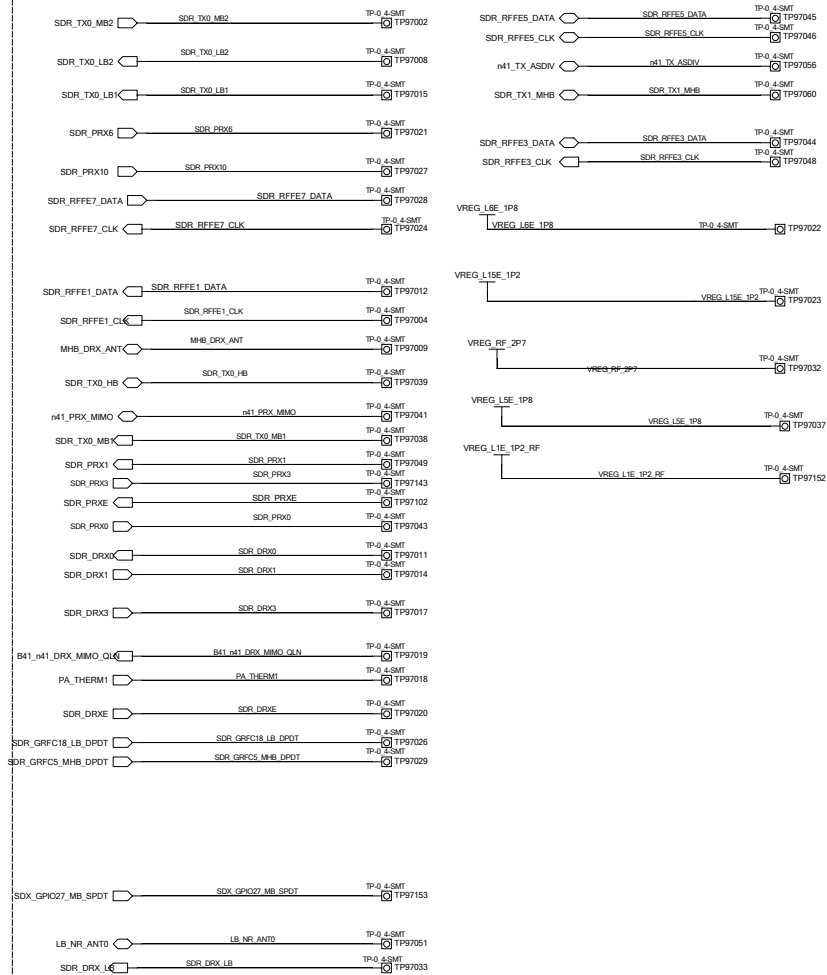
A+G SENOSR CONN



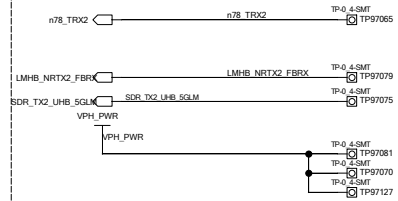
Charge Wireless CONN



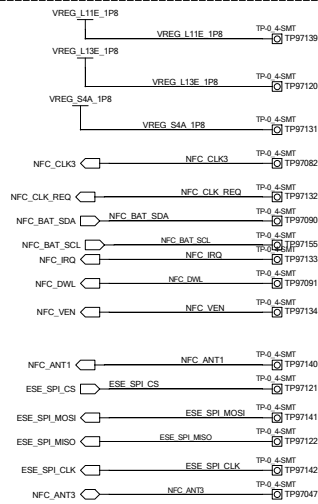
SKY58081 MHB TRX



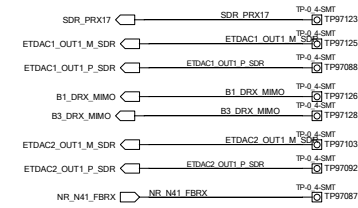
N78 TX2



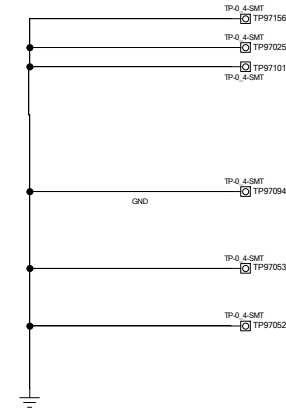
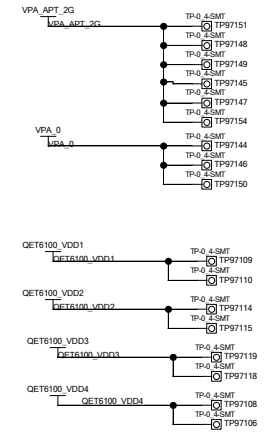
NFC

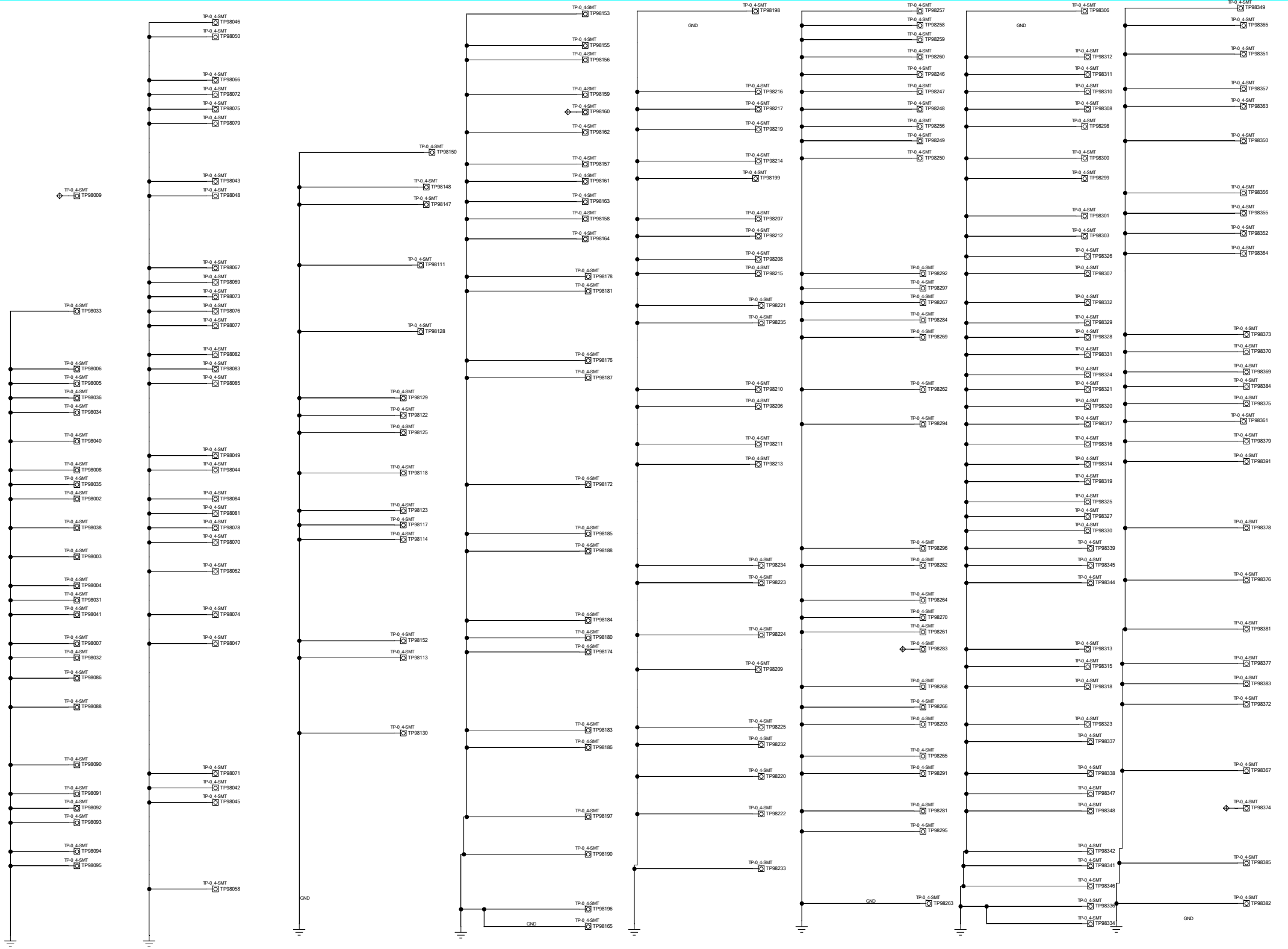


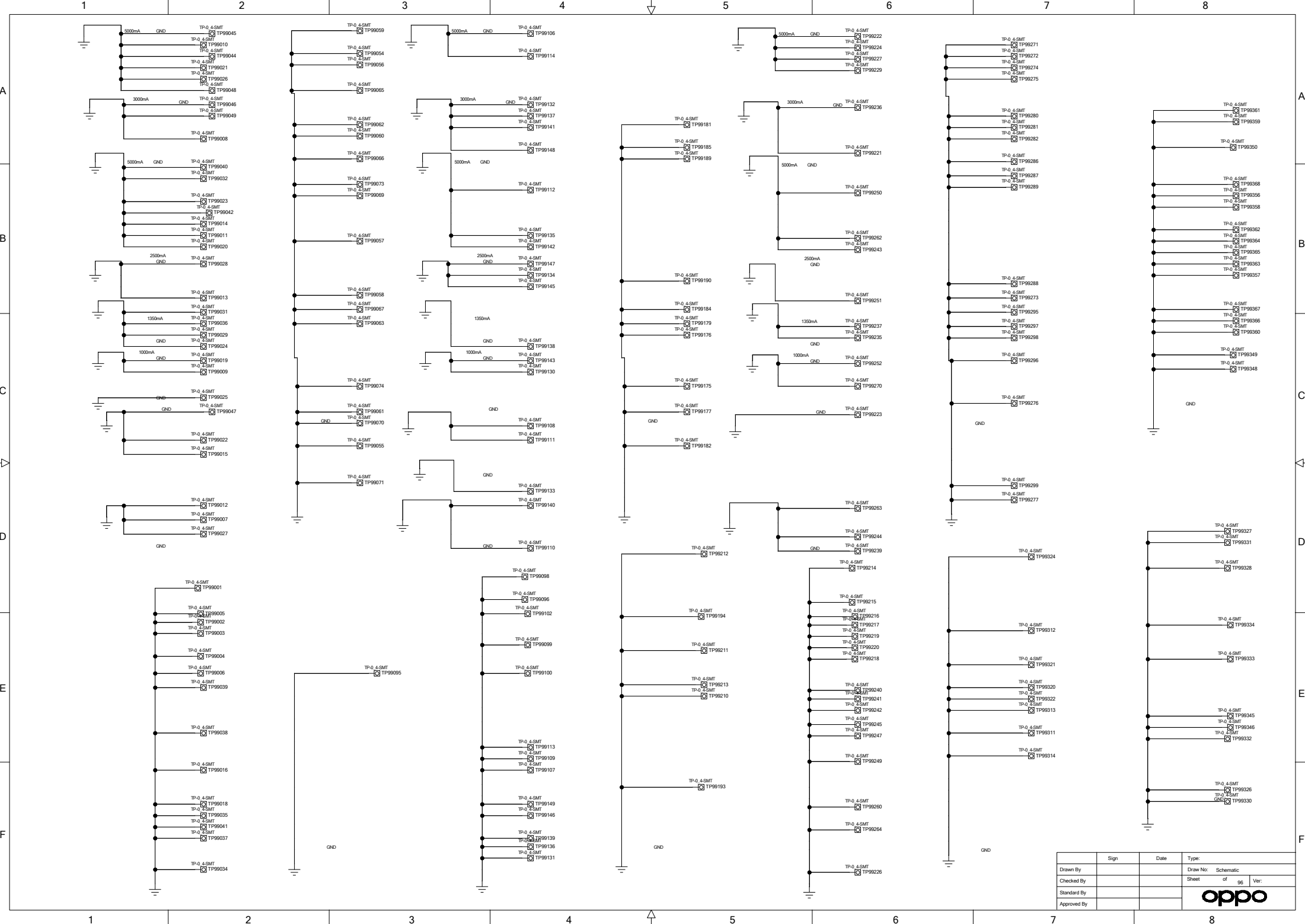
N79 TX



ET Power

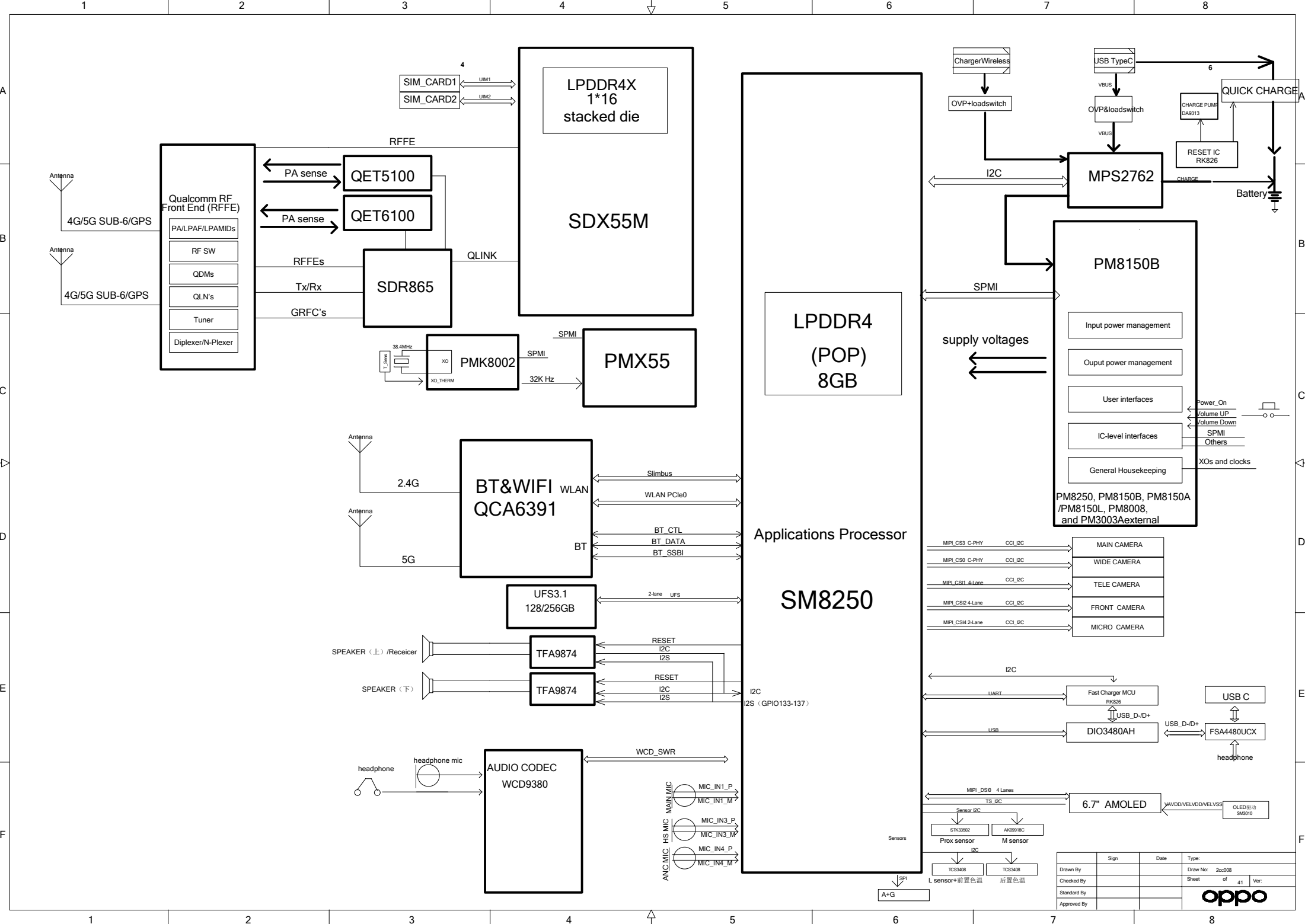






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Approved By			





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Checked By			Sheet of 41 Ver:
Standard By			
Approved By			

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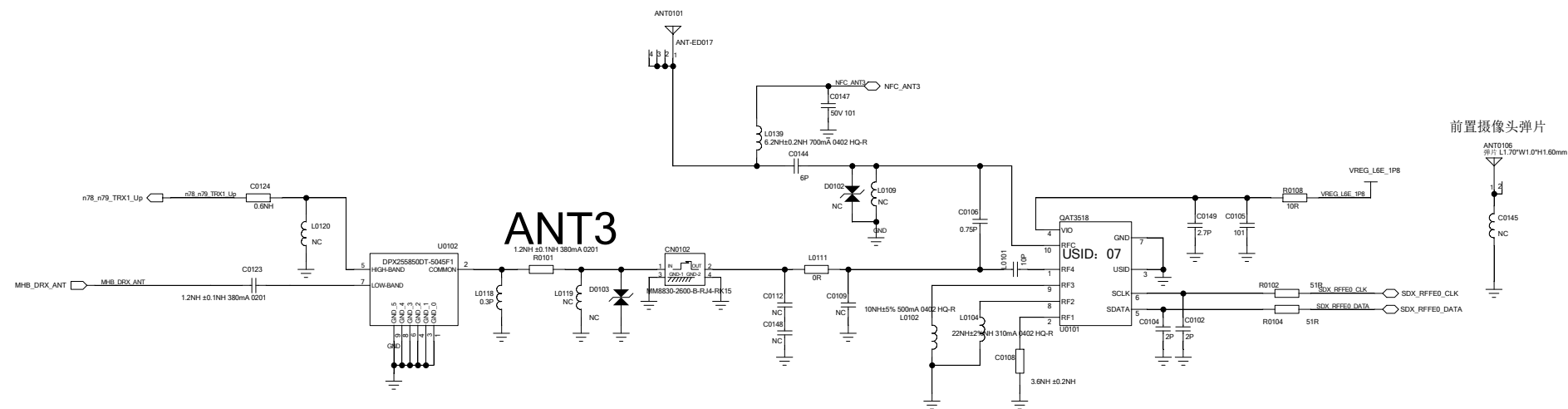
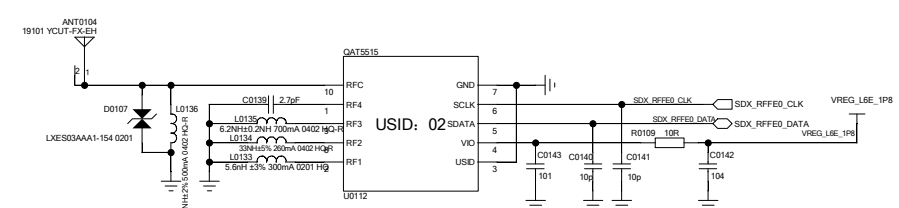
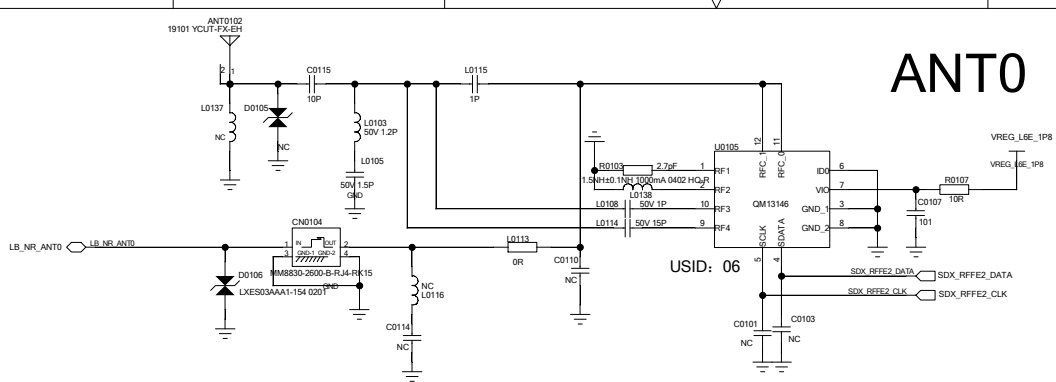
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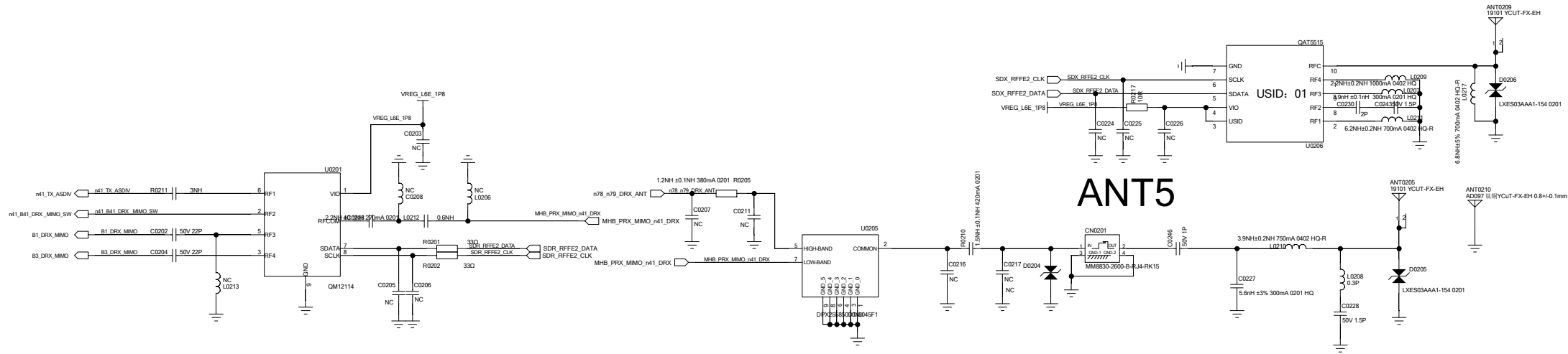
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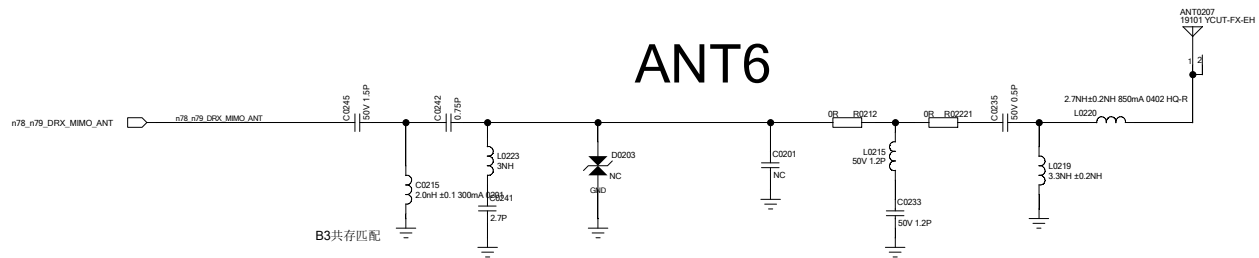


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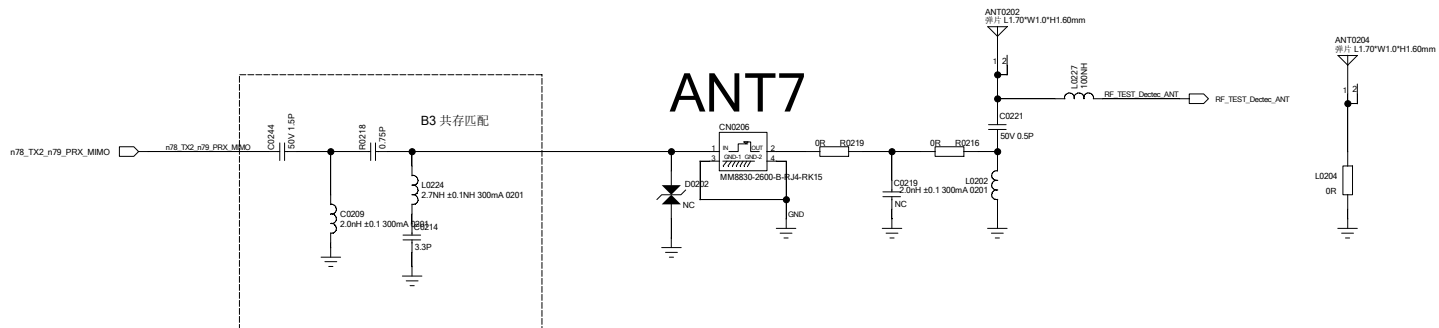
ANT5:MHB DRX MIMO+n41 DRX + N78/79 DRX



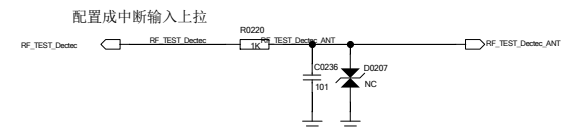
ANT6



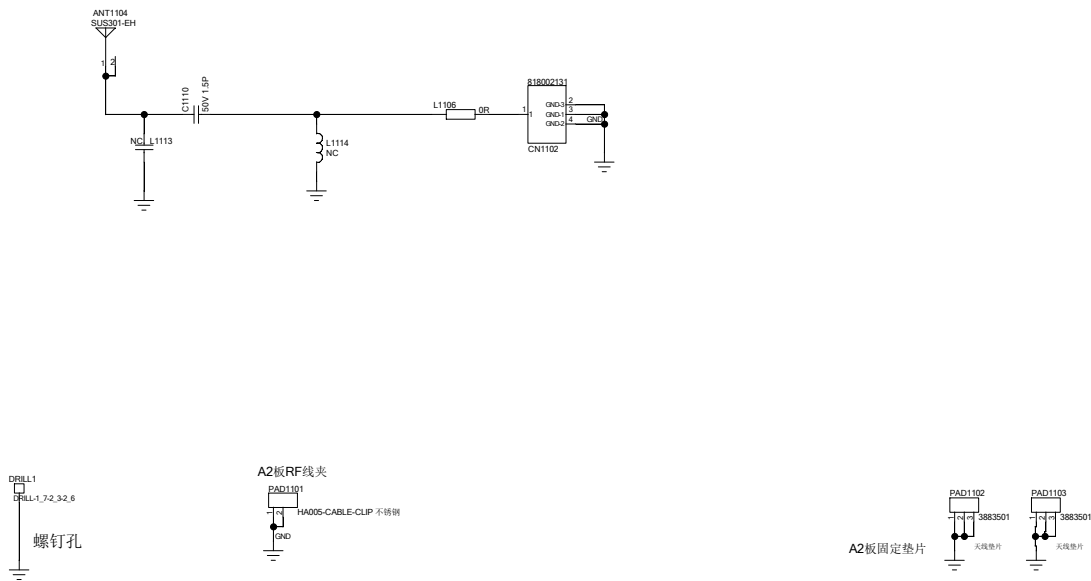
ANT7



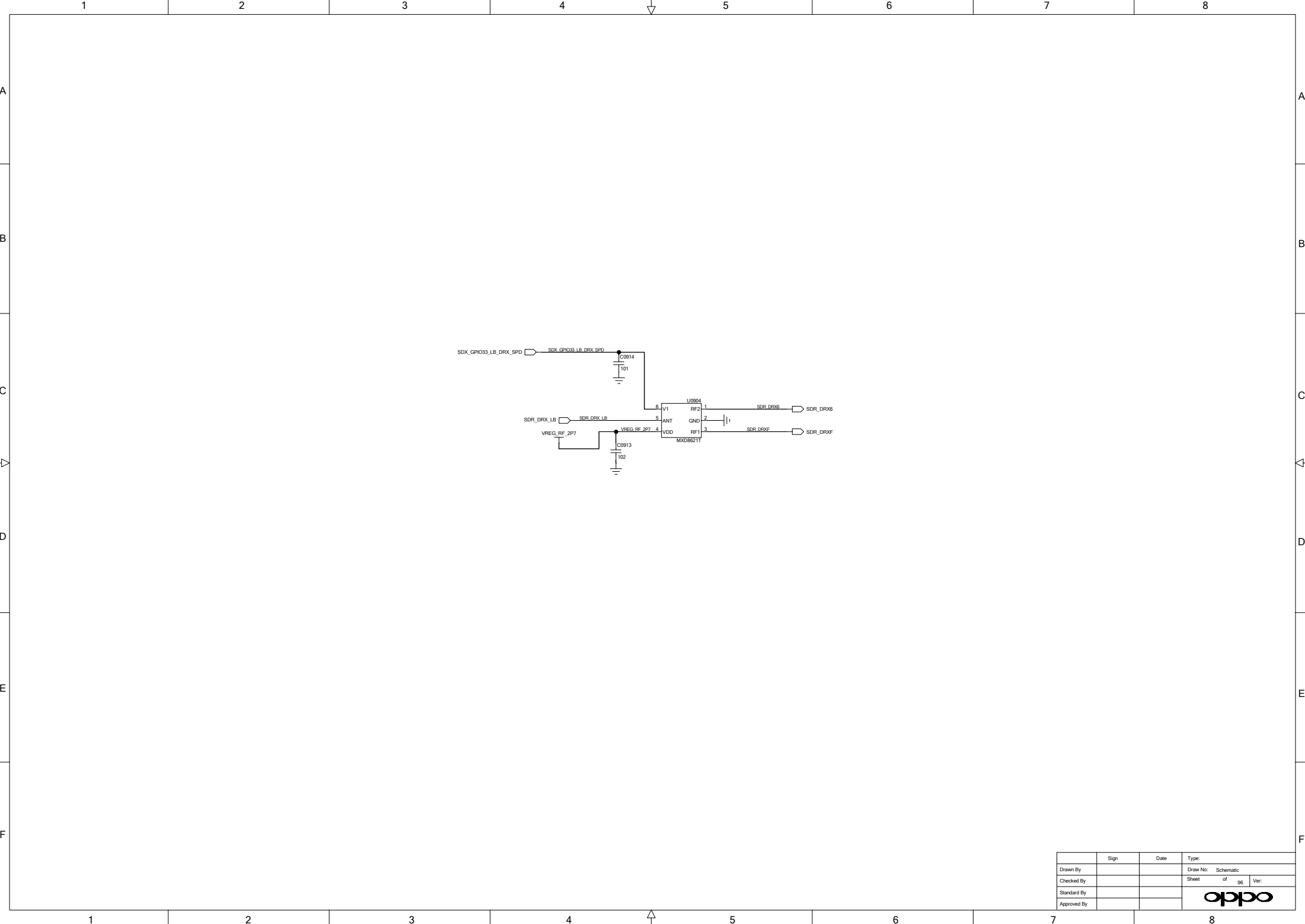
压板传导测试检测电路



ANT4 MHB PRX

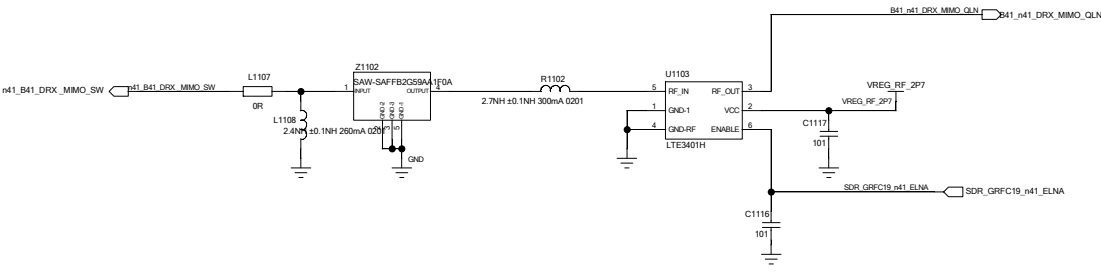


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Approved By				

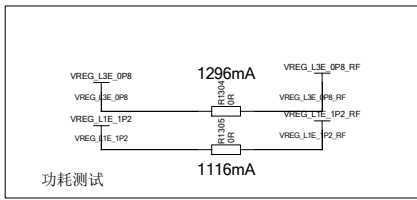
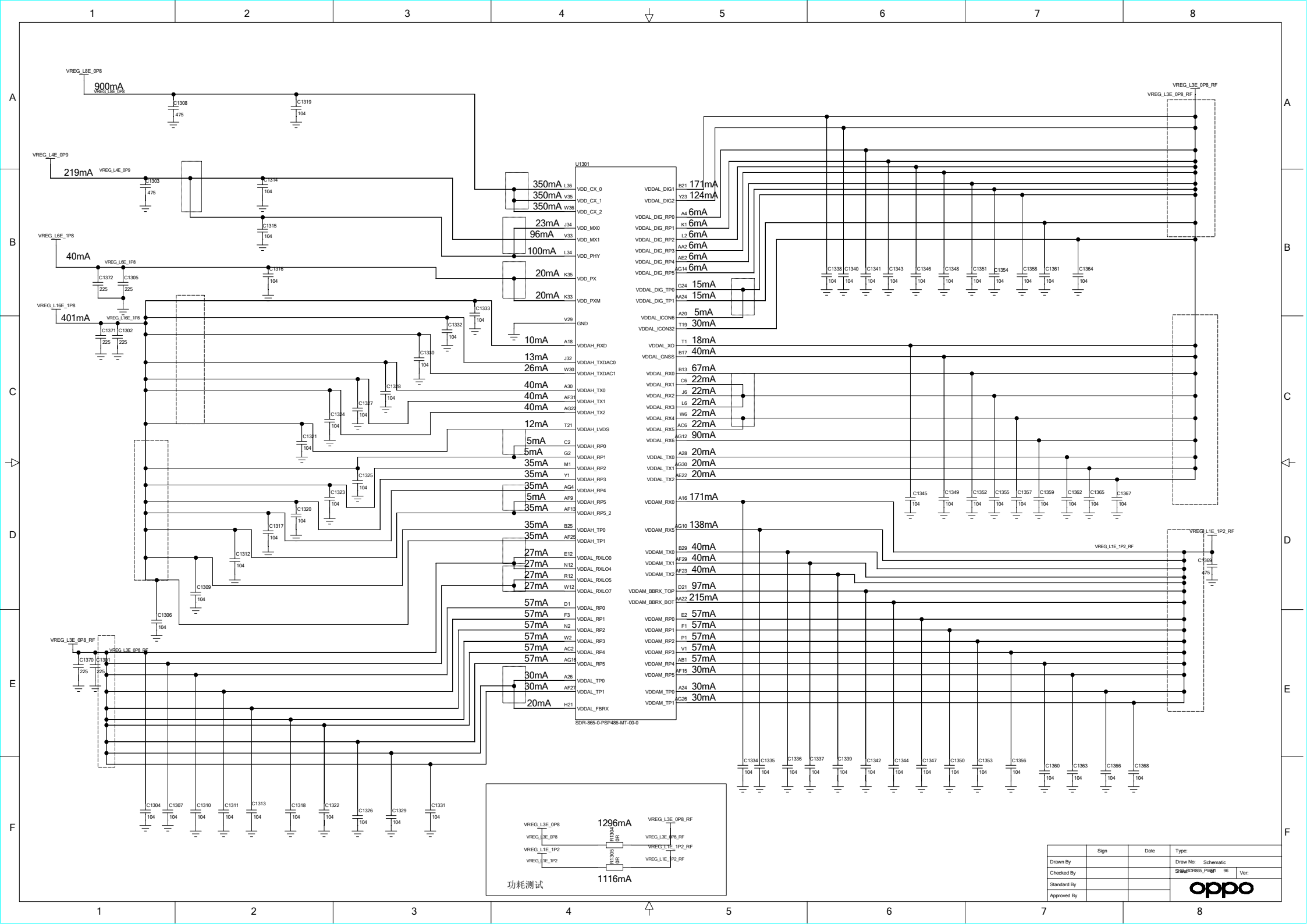


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Drawn By			Draw No: Schematic	
Checked By			Sheet	of 96 Ver:
Standard By			oppo	
Approved By				

Place Close to ANT5



	Sign	Date	Type:	
Drawn By			Draw No.	Schematic
Checked By			Sheet	of 96 Ver:
Standard By			oppo	
Approved By				



	Sign	Date	Type
Drawn By			Draw No: Schematic:
Checked By			SDR-865-0-PSF486-MT-00-0 96 Ver:
Standard By			
Approved By			

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PDN Guidelines for LPDDR4X					
	Tolerance		DC R	AC Z@20MHz	De-cap. Combination
	(DC)	(AC+DC)			
VDDQ(0.6V)	±18mV	±30mV	<15mΩ	<38mΩ	Ch. A 2.2uF 1ea + 100nF 2ea Ch. B 2.2uF 1ea + 100nF 2ea
VDDQ(1.1V)	±33mV	±55mV	<8mΩ	<38mΩ	Ch. A 4.7uF 1ea + 100nF 2ea Ch. B 4.7uF 1ea + 100nF 2ea
VDD(1.1V)	±55mV	±90mV	<40mΩ	<125mΩ	Ch. A 2.2uF 1ea + 100nF 2ea Ch. B 2.2uF 1ea + 100nF 2ea

	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By			Shu@SCR885, G99 96 Ver:
Standard By			
Approved By			

oppo

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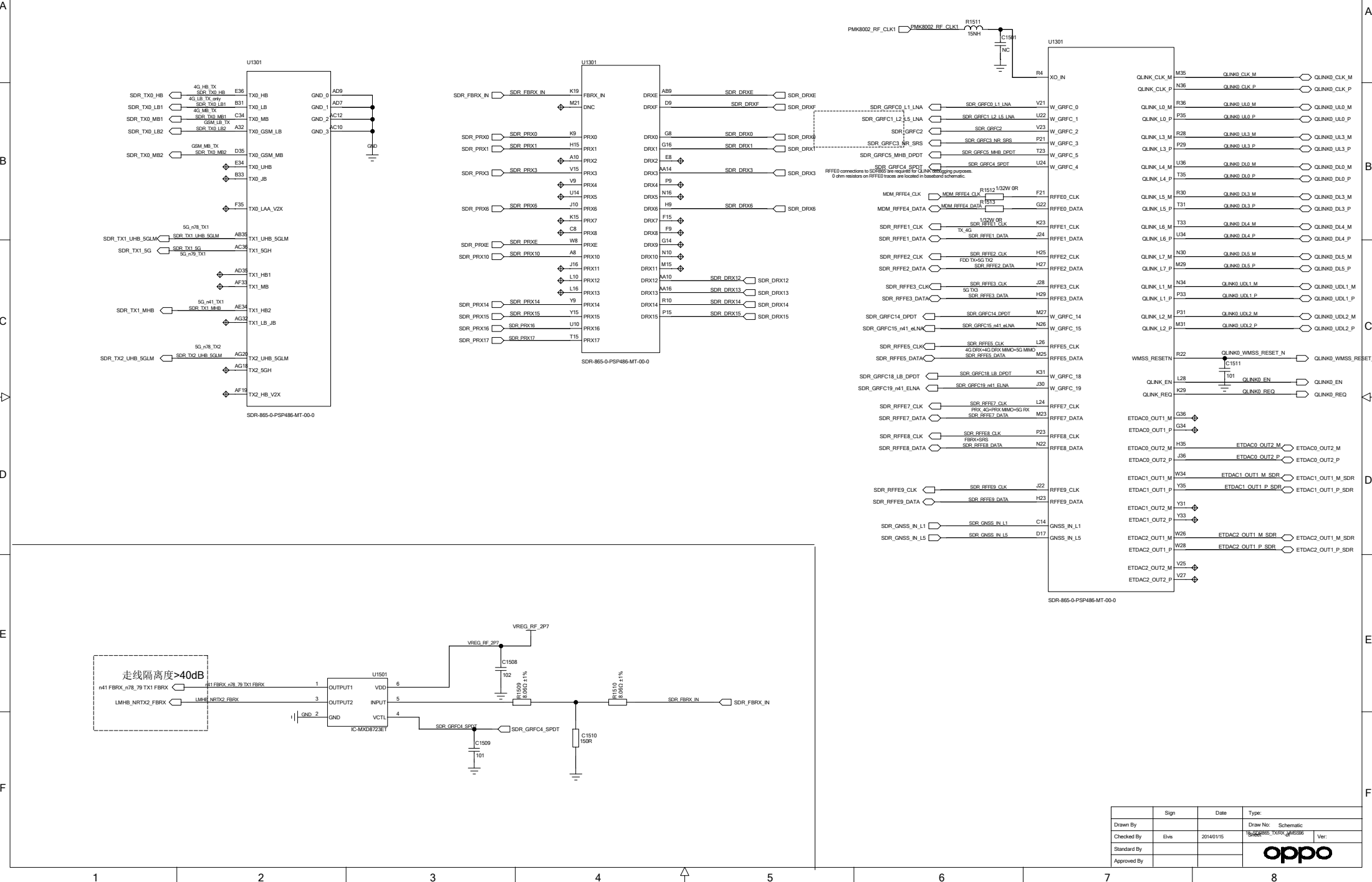
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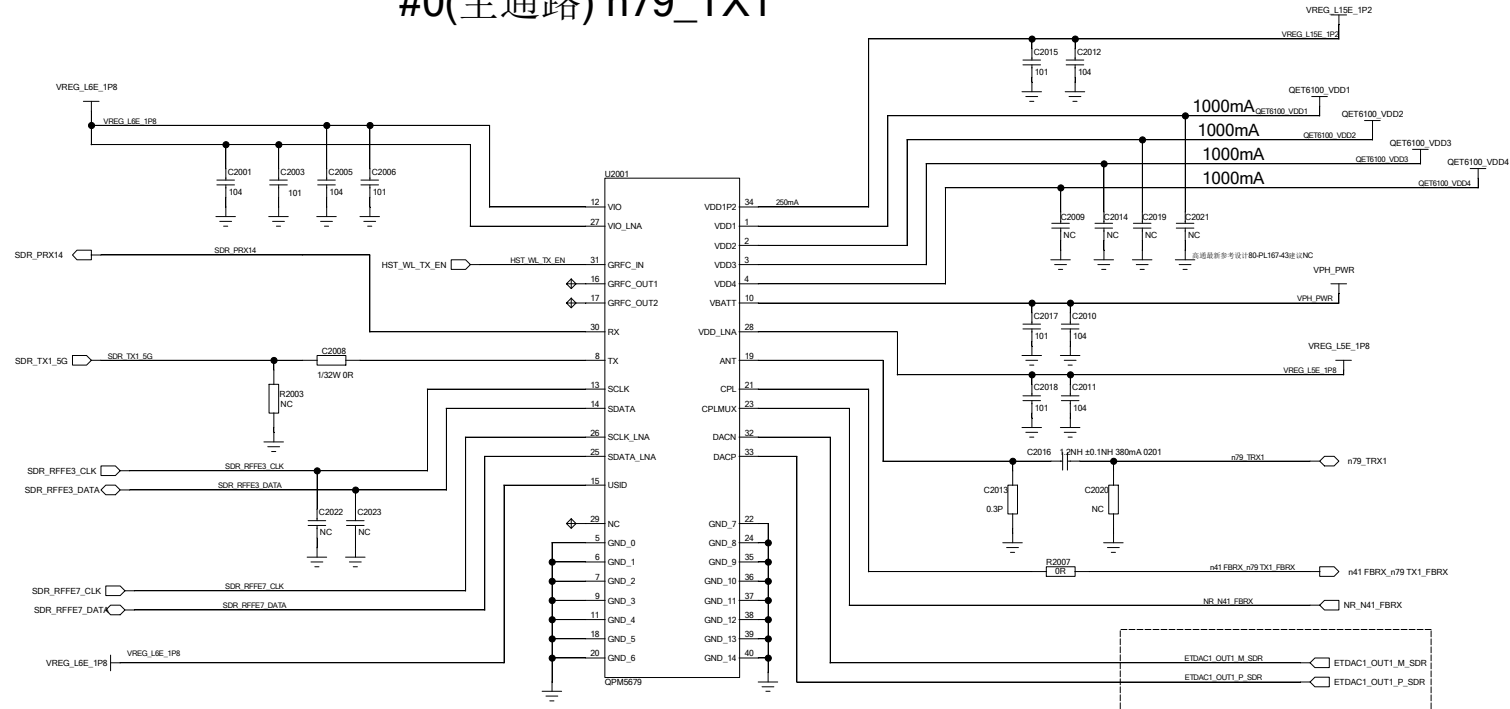
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	Sign	Date	Type
Drawn By	Elvis	2014/01/15	Draw No: Schematic
Checked By			1504865-TX/RX-PPSP486 Ver:
Standard By			
Approved By			

oppo

#0(主通路) n79_TX1

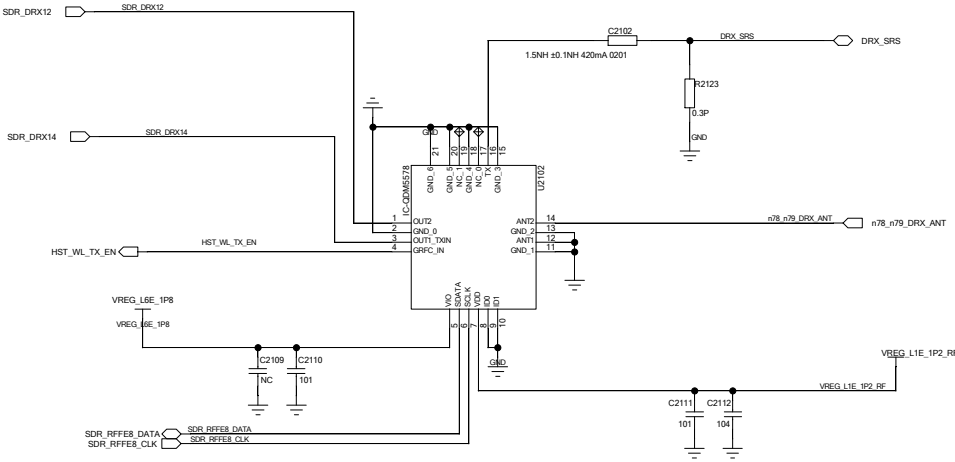


Maximum trace length of 80 mm
MTP trace width is 0.16 mm
25-500 characteristic impedance (single-ended for each PIM)
Daisy chain routing (from SDR to QPM1, then from QPM1 to QPM2, and so on, avoid branching and stubs)

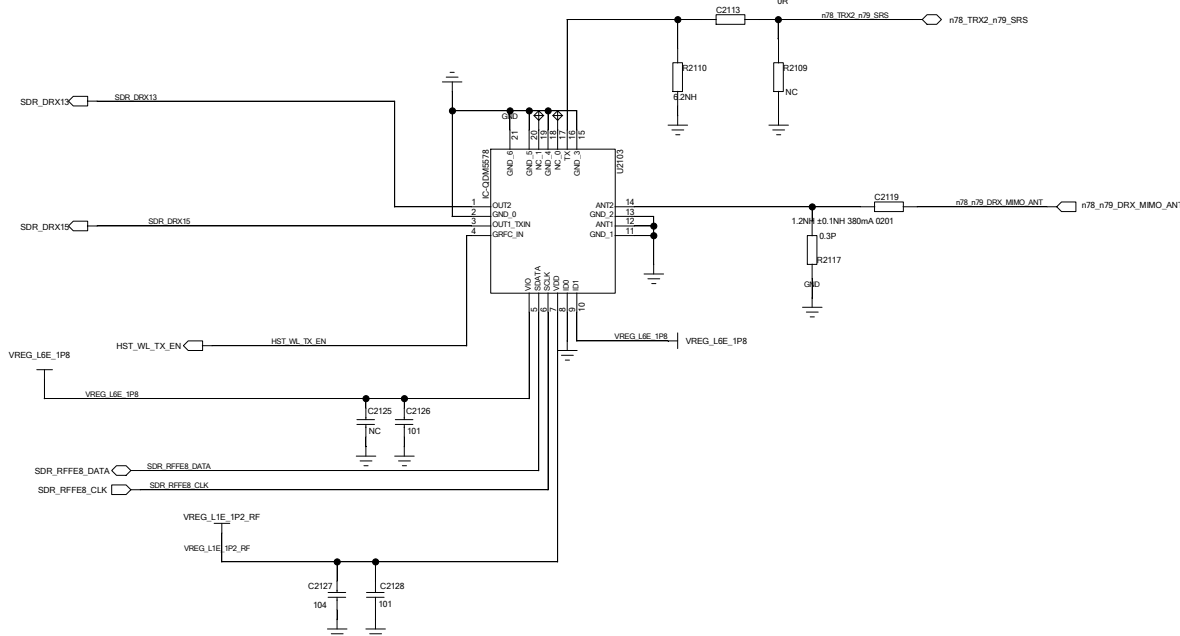
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Drawn By			Draw No: Schematic
Checked By			Sheet of 99 Ver:
Standard By			
Approved By			

oppo

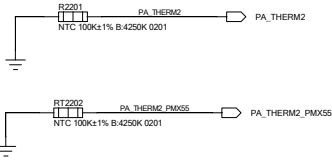
n78-n79_DRX



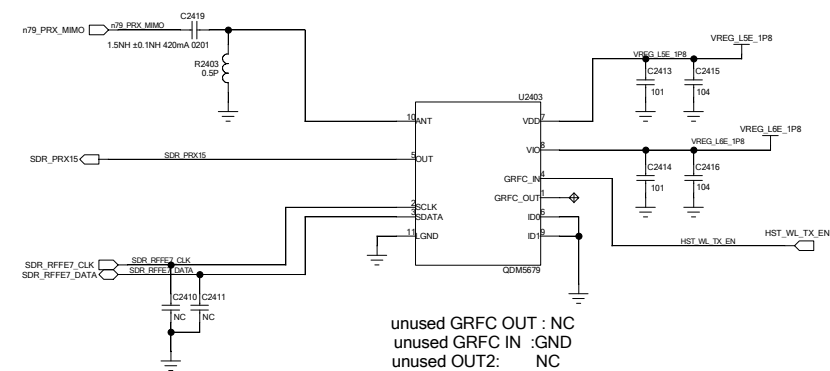
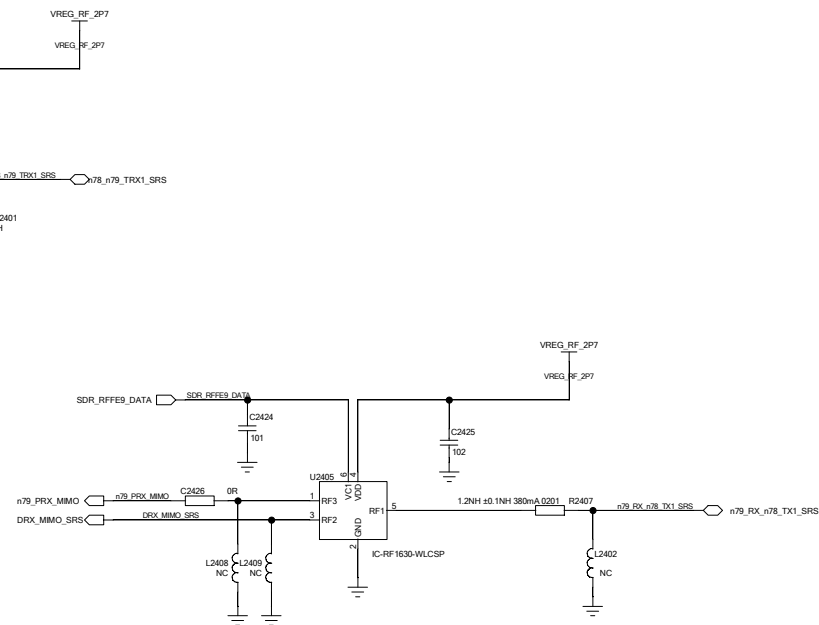
n78-n79_DRXMIMO



放2板，用于监控主板5G PA使用



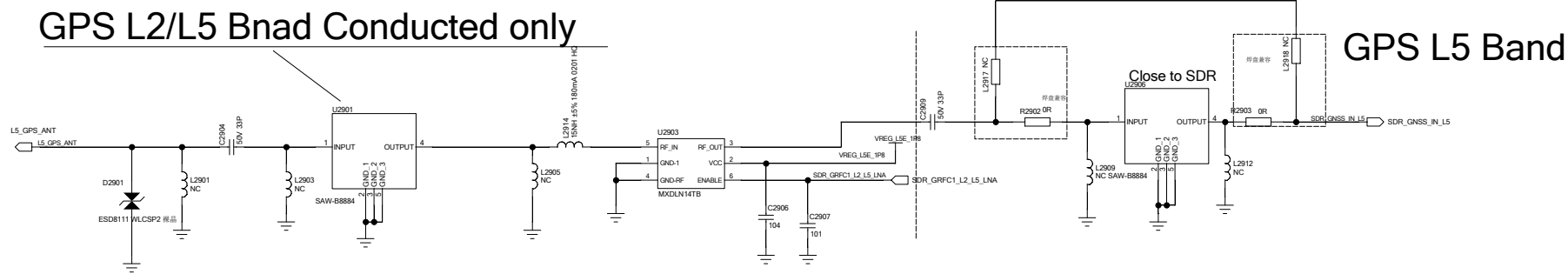
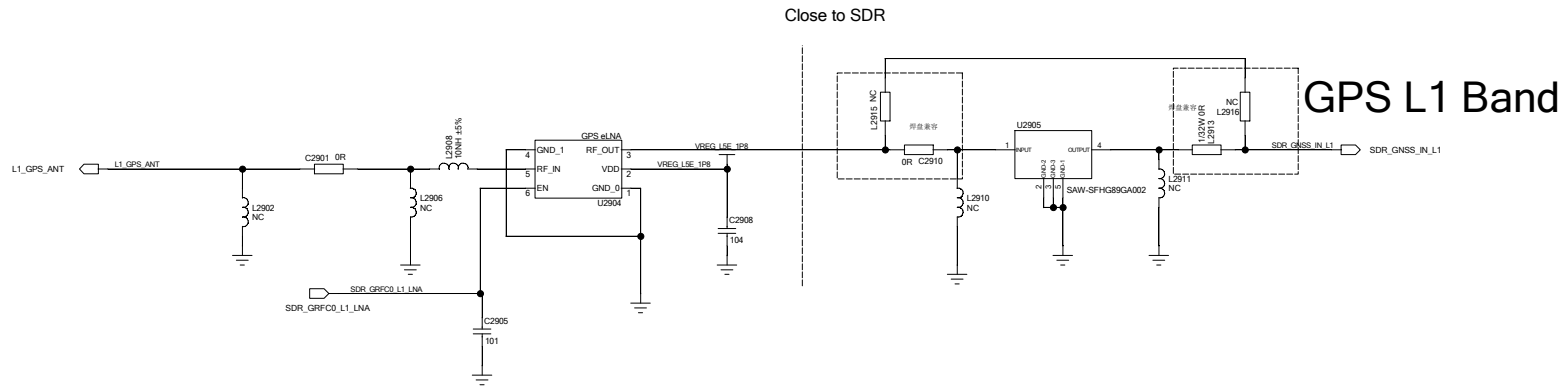
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Drawn By			Draw No.	Schematic
Checked By			Sheet of	Ver:
Standard By			oppo	
Approved By		96		



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unused GRFC OUT : NC
unused GRFC IN  :GND
unused OUT2:    NC

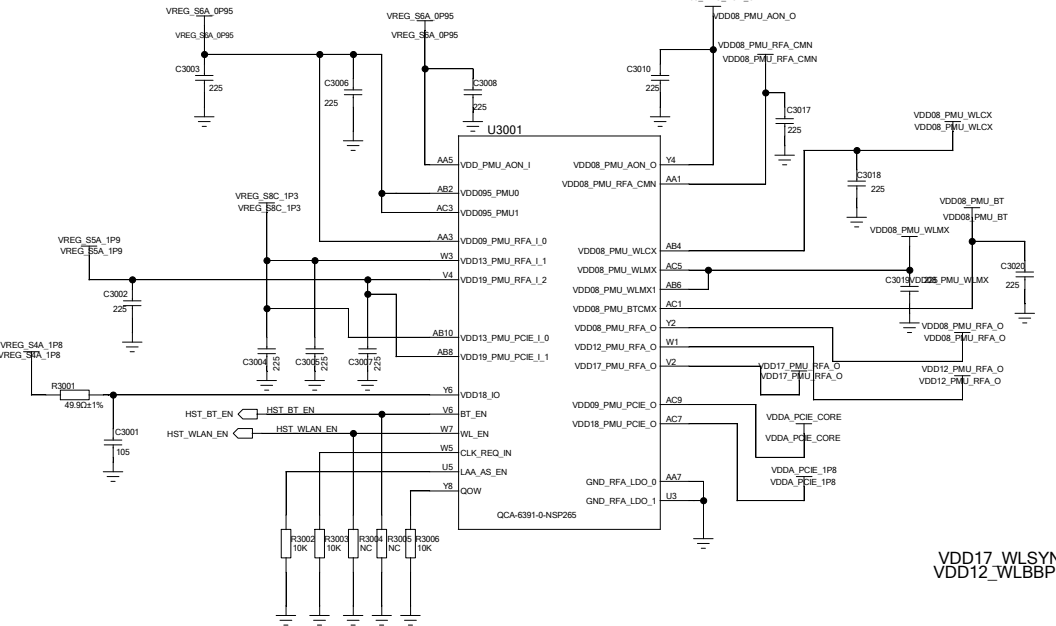
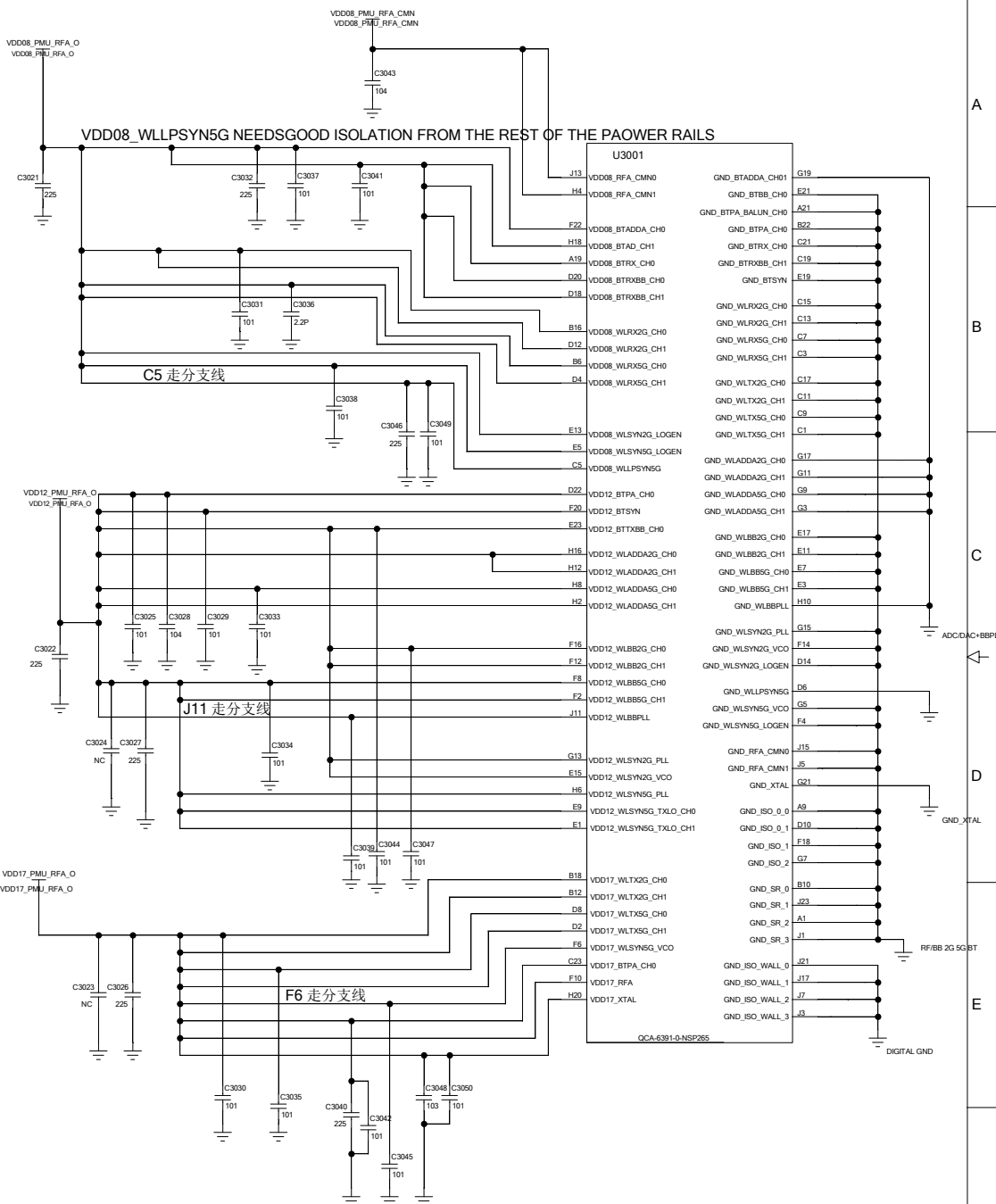
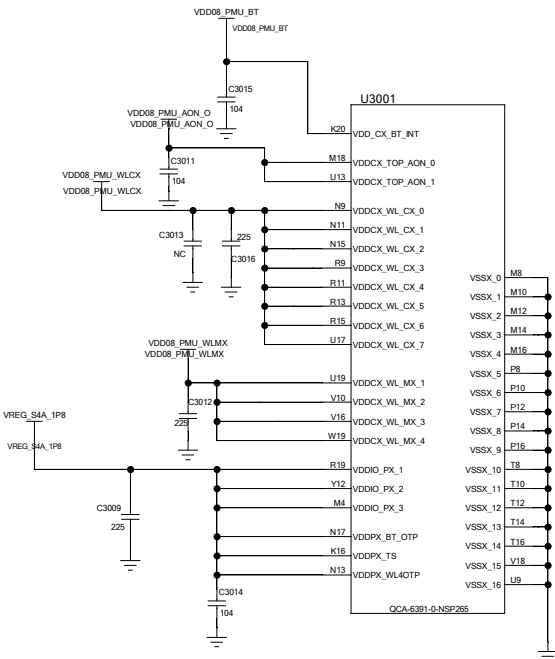
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	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By			Sheet 49_GPS of 96 Ver:
Standard By			
Approved By			



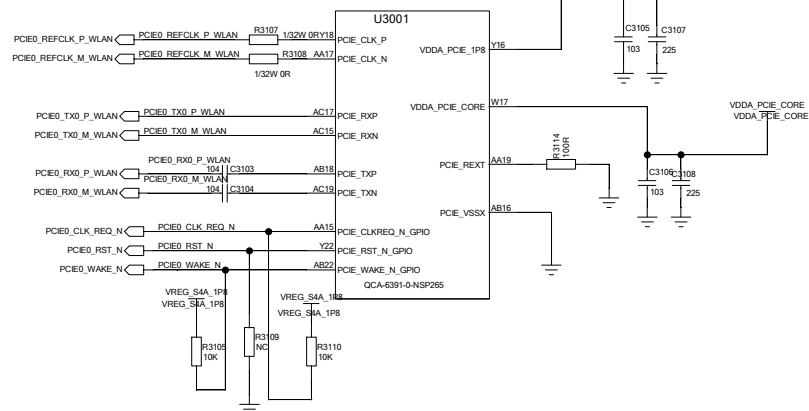
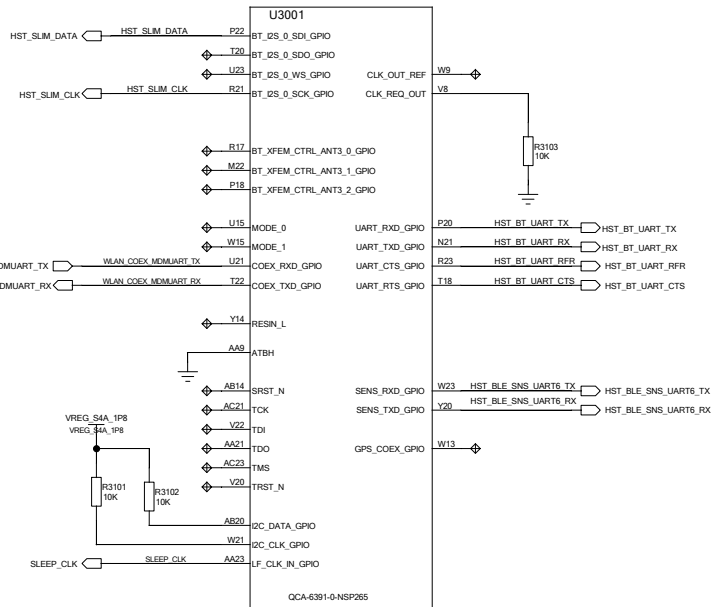
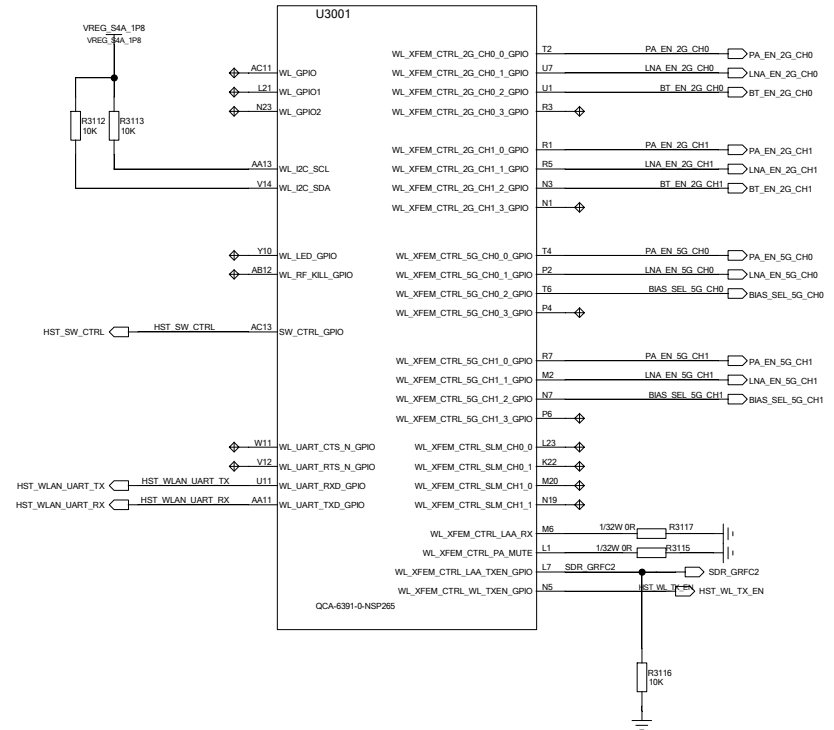
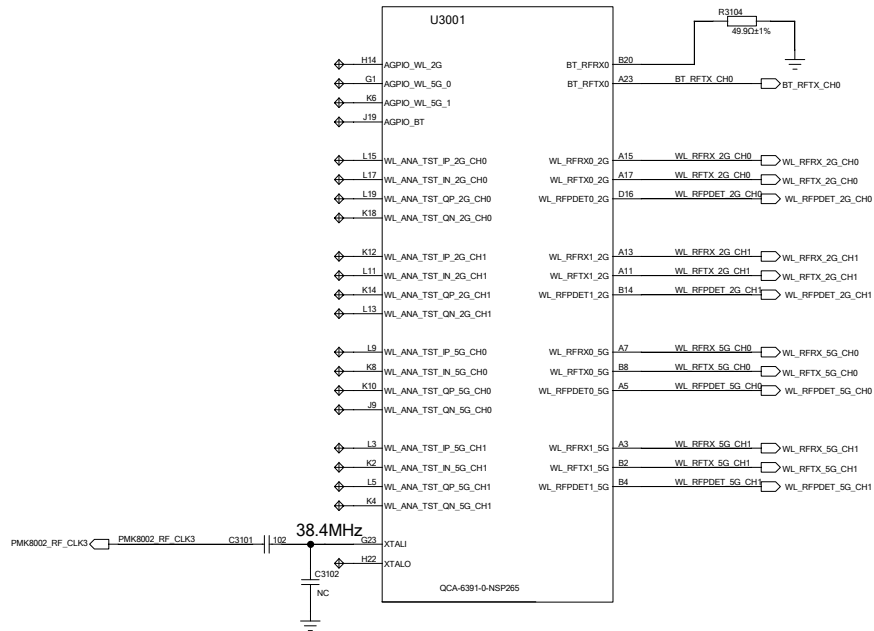
PIN脚名称	PIN脚	电流大小
VDD_PMU_AON_I	AA5	100mA
VDD095_PMU	AB2 AC3	1250mA
VDD09_PMU_RFA_I	AA3	200mA
VREG_S8C_1P3	W3	400mA
VREG_S5A_1P9	V4	400mA
VDD13_PMU_PCIE_I	AB10	400mA
VDD19_PMU_PCIE_I	AB8	400mA
VDD08_PMU_RFA_CMN	AA1	50mA
VDD08_PMU_AON_O	Y4	50mA
VDD08_PMU_WLCX	AB4	750mA
VDD08_PMU_WLMX	AC5 AB6	450mA
VDD08_PMU_BTCMX	AC1	50mA
VDD08_PMU_RFA_O	Y2	200mA
VDD12_PMU_RFA_O	W1	400mA
VDD17_PMU_RFA_O	V2	400mA
VDD09_PMU_PCIE_O	AC9	400mA
VDD18_PMU_PCIE_O	AC7	400mA
VCC5G_FEM		600mA
VCC2G_FEM		600mA



VDD17_WLSYN5G_VCO NEEDSGOOD ISOLATION FROM THE REST OF THE PAOWER RAILS
VDD12_WLBBPLL NEEDS GOOD ISOLATION FROM BB 1.2V、VCOBTPA 1.7V、 and RX 0.8V


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Drawn By	Draw No:	Schematic
Checked By	Sheet	of 96 Ver:
Standard By		
Approved By		





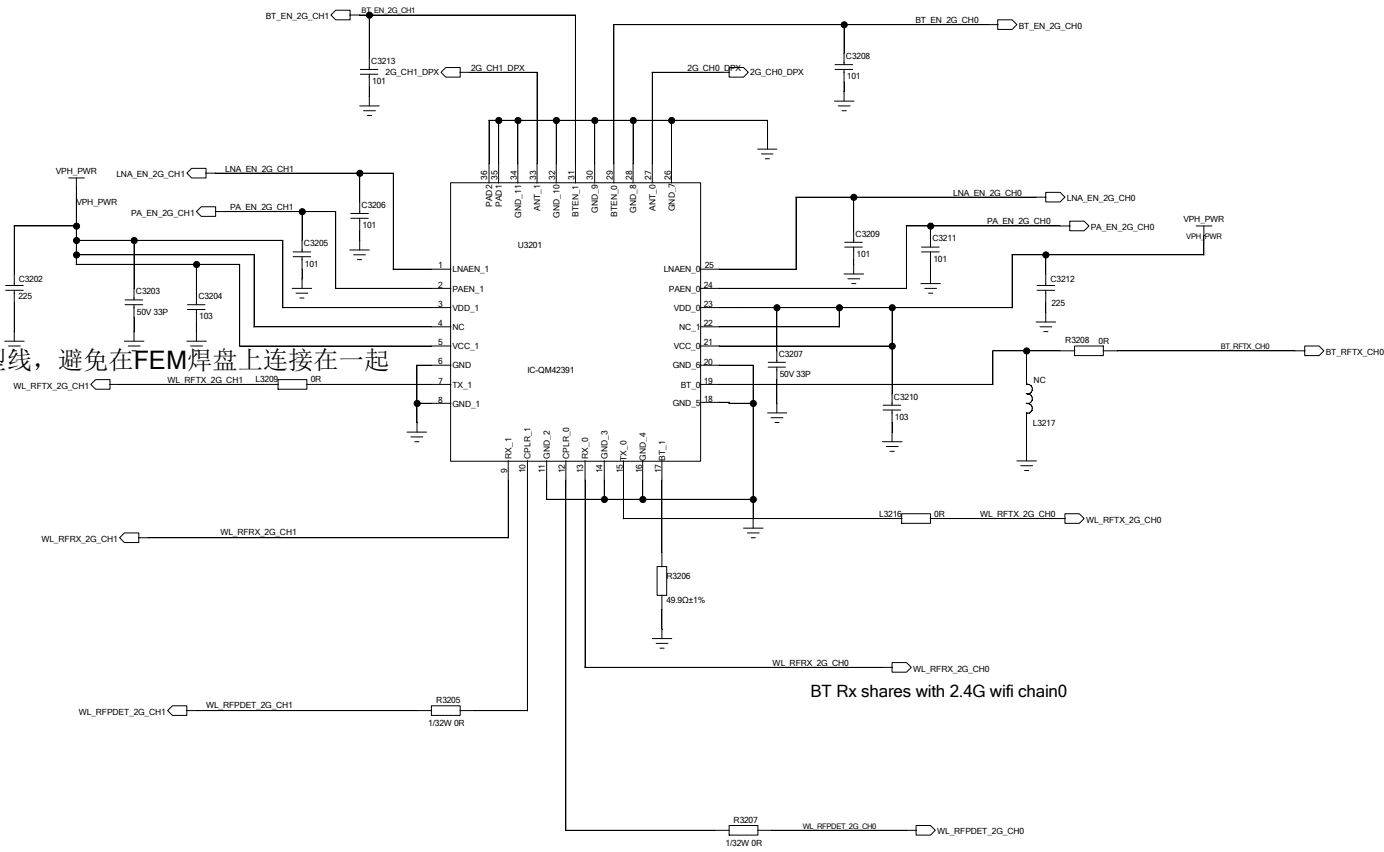
SUM_CH0_CTL1	SUM_CH0_CTL0	
0	0	48MHz
0	1	76.8MHz
1	0	96MHz
1	1	38.4MHz

SLIM_CH1_CTL1
XO_TXCO_SEL
0: XO
1: TCXO

	Sign	Date	Type:	
Drawn By			Draw No:	Schematic
Checked By			Sheet	of 21 Ver:
Standard By				
Approved By				



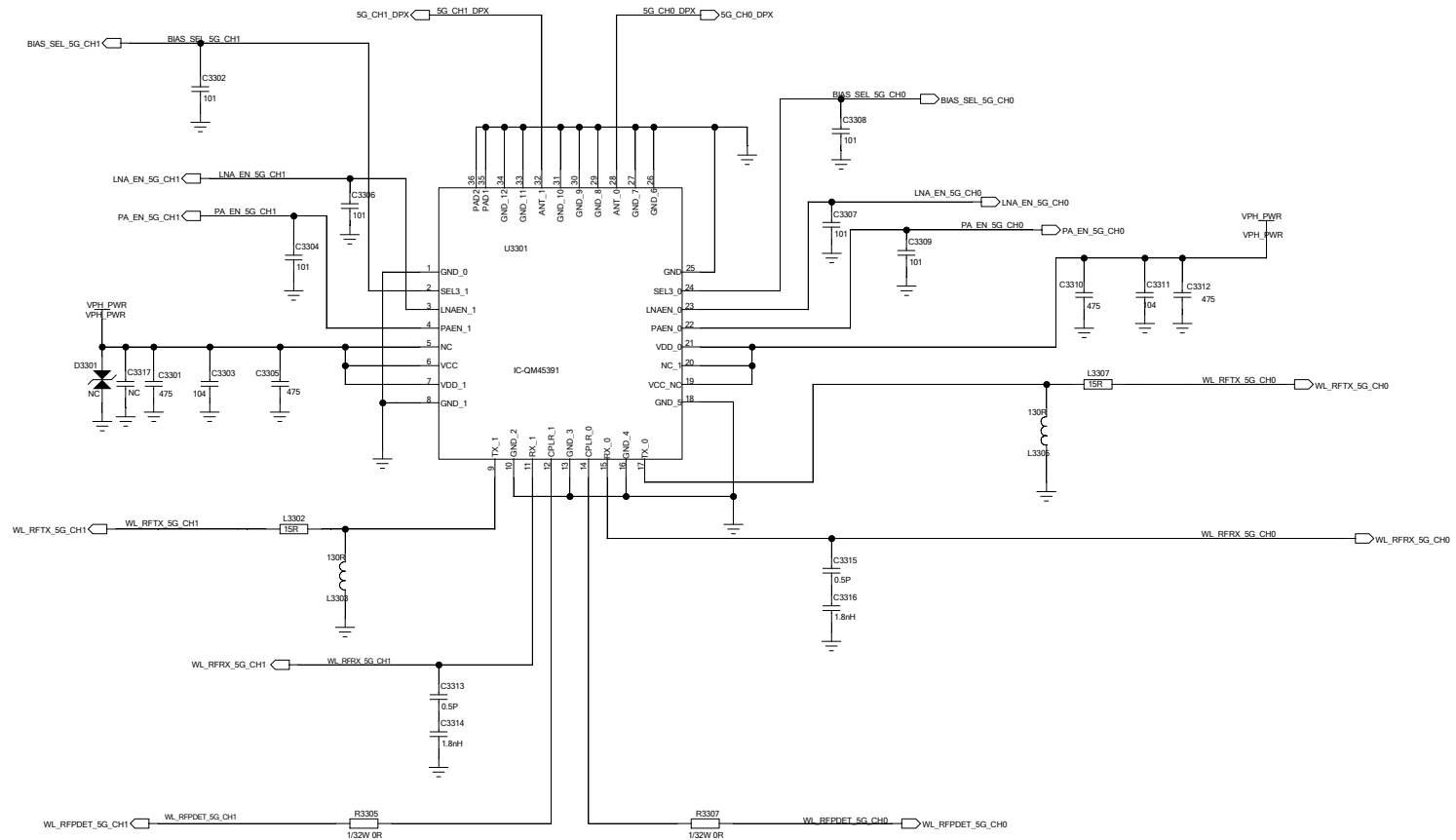
FEM电源供电需要走星型线，避免在FEM焊盘上连接在一起



BT Rx shares with 2.4G wifi chain0

Drawn By	Sign	Date	Type:
Checked By			Draw No: Schematic
Standard By			Sheet of 21 Ver:
Approved By			oppo

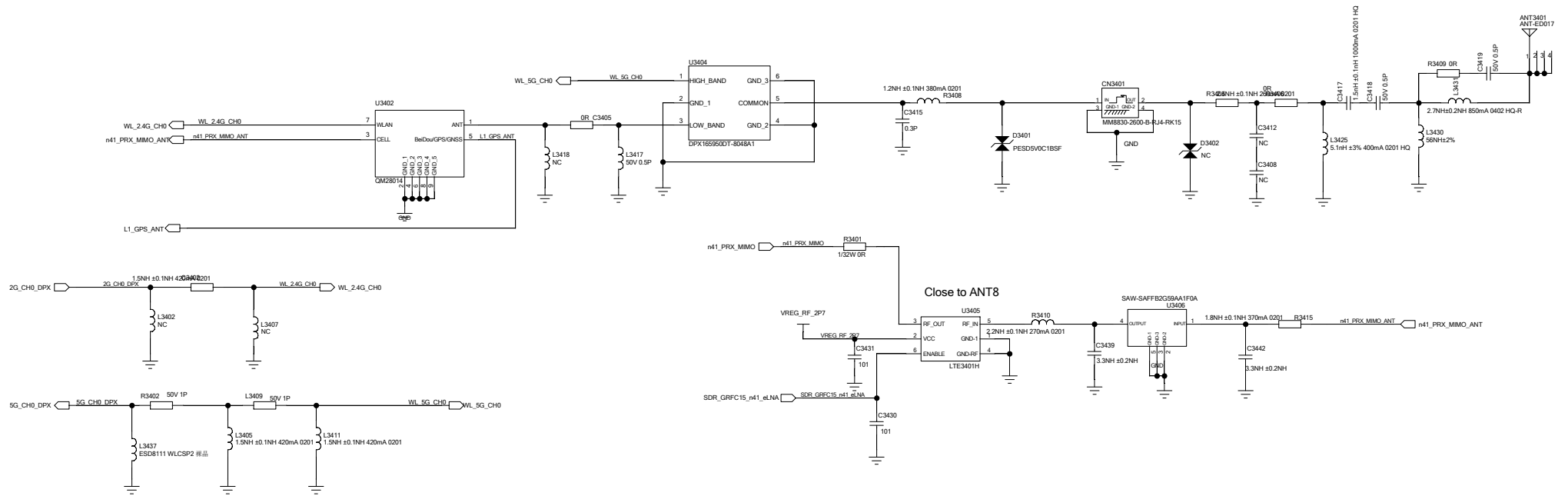
FEM电源供电需要走星型线，避免在FEM焊盘上连接在一起



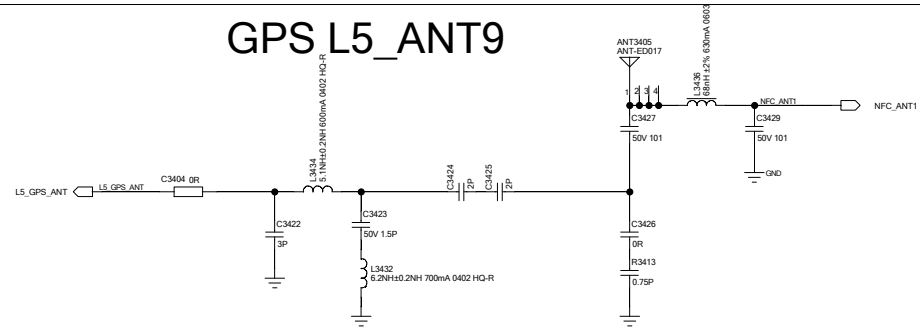
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Drawn By			Draw No: Schematic
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Standard By			
Approved By			

oppo

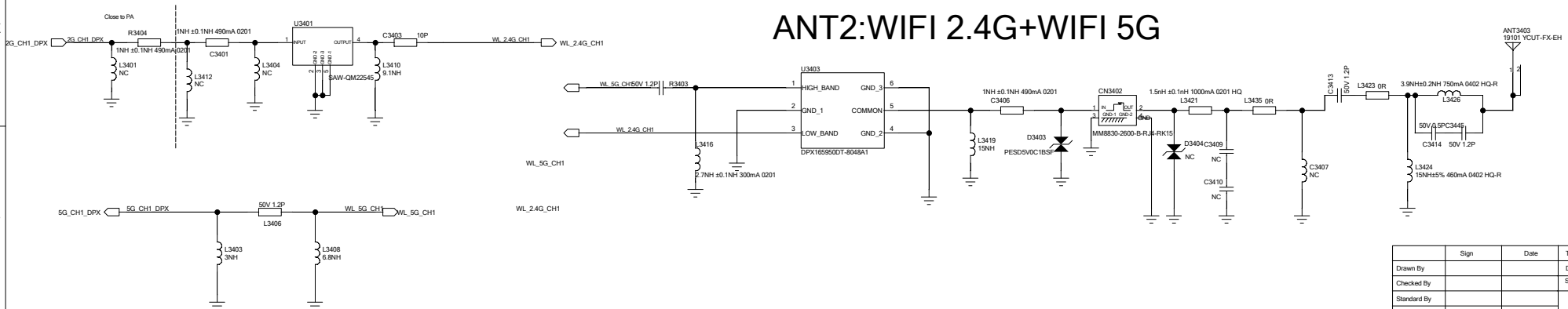
GPS L1&2.4G CH0&N41 MHB PRX_ANT8




GPS_L5_ANT9

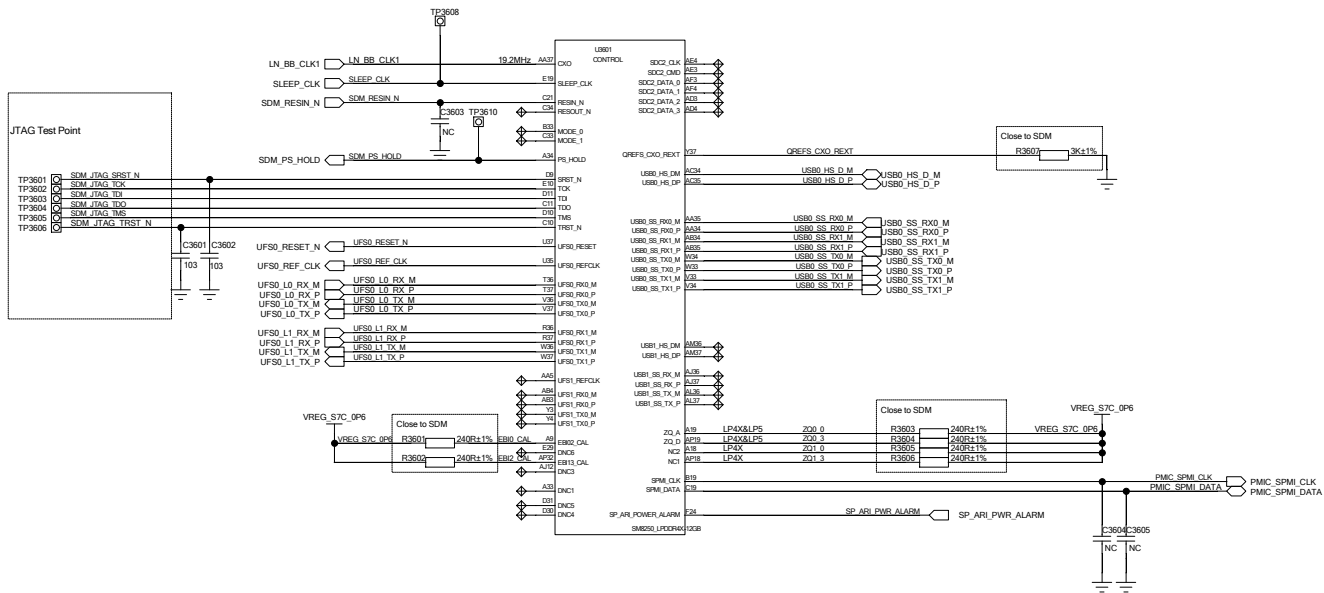


ANT2:WIFI 2.4G+WIFI 5G



	Sign	Date	Type:	
Drawn By			Draw No:	
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Standard By				
Approved By				

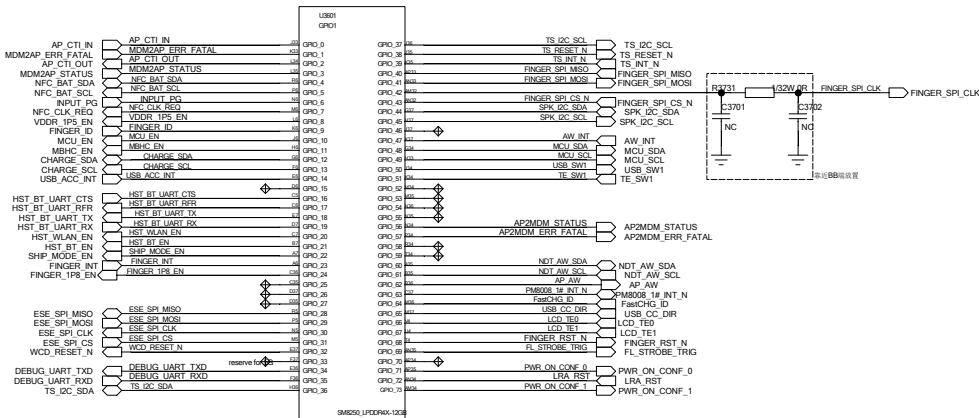
SDM865 CONTROL



Drawn By	Sign	Date	Type:
Checked By			Draw No: Schematic
Standard By			Sheet 38 of 38
Approved By			Sheet 38 of 38



SDM865 GPIO1



Boot Configuration GPIO Settings

Boot Configuration	GPIO	Function	Comments
BOOT_CONFIG_0	GPIO_05	WDOG_DISABLE	Output watchdog control signal
BOOT_CONFIG_1	GPIO_08	FAST_BOOT_0	Select external boot device
BOOT_CONFIG_2	GPIO_04	FAST_BOOT_1	Select external boot device
BOOT_CONFIG_3	GPIO_09	FAST_BOOT_2	Select external boot device
BOOT_CONFIG_4	GPIO_07	FAST_BOOT_3	Select external boot device
BOOT_CONFIG_9	GPIO_07	USE_SERIAL_NUM	

GPIO 17 the serial number is used as part of authentication
Secure boot public key hash is stored in the fuse
Secure boot private key is used for the verification process
Secure boot private key is used for the verification process

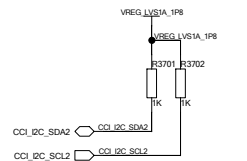
Note: If secure boot is not required, ensure that there are no external pulls on these GPIOs. The external pulls can force the SDM device to enter secure boot or select a different boot device.

FAST_BOOT Configuration

FAST_BOOT[3:0]	Boot device/comments
0000	UFS (1) Then microSD on SDC2 (2) Then SSHS/FSS USB on USB 3.1 (3)
0001	MicroSD on SDC2 (1) Then UFS (2)
0010	SSHS/FSS USB on USB 3.1 (3) MicroSD on SDC2 (1)
0011	SSHS/FSS USB on USB 3.1 (2)

I2C PULLUP

FRONT Camera I2C2

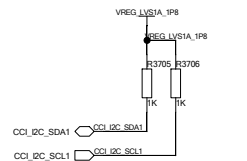


I2C device	CCI_IC Address	Write address
LR camera sensor	0X21	0X20
LR camera EEPROM	0XA8	0XA8

Main Camera I2C0

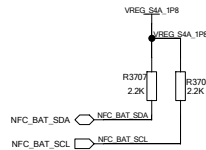
IMX686/IMX766(TBD)		
I2C device	CCI_IC Address	Write address
LR camera sensor	0X21	0X20
LR camera driver	0X19	0X18
LR camera EEPROM	0XA1	0XA0

WIDE Camera I2C1



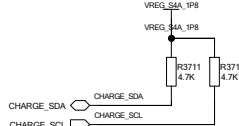
I2C device	CCI_IC Address	Write address
RR camera sensor	0X35	0X34
RR camera driver	0XE5	0XE4
RR camera EEPROM	0XA3	0XA2

NFC



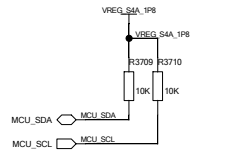
I2C device	Read Address	Write address
NFC	0d51	0d50

MP2762 CHARGE



I2C device	AW Address	Write address
MP2762	0d19	0d18
N17619	0dC3	0dC2

GAUGE

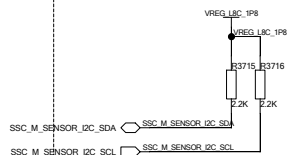


I2C device	AW Address	Write address
MP2762	0d15	0d14
GAUGE	0dC1	0dC0
U1711	0d4B	0d4A

TP I2C

I2C device	LPI Address	Write address
TP	0d41	0d40

MSENSOR I2C

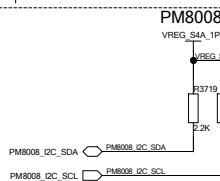


I2C device	LPI Address	Write address
MP2762	0d71	0d70
Msensor	0d61	0d60

ALS +Color sensor&P sensor I2C

I2C device	Read Address	Write address
Color	0d73	0d72
Als&P	0d6C	0d6B

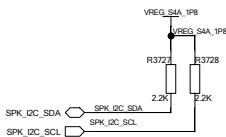
S_OIS I2C



NDT TOUCH//LRA

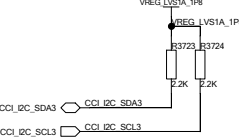
I2C device	Read Address	Write address
NDT_AW_SDA	0d85	0d84
NDT_AW_SCL	0d85	0d84

SMIPA/Type C FSA4480/HALL



I2C device	Read Address	Write address
3000A	0dC1	0dC0
SPK SMART PA	0d7B	0d7A
REC SMART PA	0d7B	0d7A
FSA4480/UXC	0d85	0d84


TELE Camera I2C3



I2C device	CCI_IC Address	Write address
RR camera sensor	0X5B	0X5A
RR camera driver	0X19	0X18
RR camera EEPROM	0XA1	0XA0

Rear color I2C

I2C device	Read Address	Write address
Rear color	0d73	0d72

	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By			Sheet 37 of 37 SDM865 I2C_PULL
Standard By			
Approved By			

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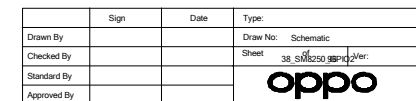
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SDM865 DSI/CSI/PCIE

WIDE_Camera 50M

TELE_Camera 13M

FRONT Camera

MAIN Camera

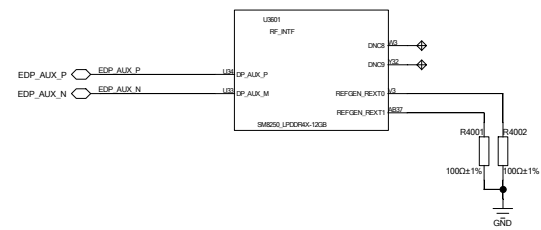
Micro_Camera_5M

DISPLAY

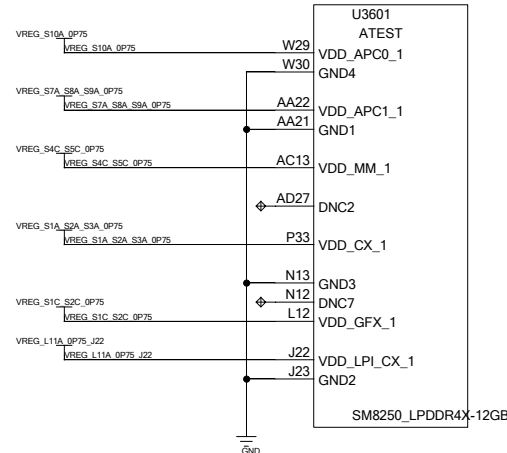
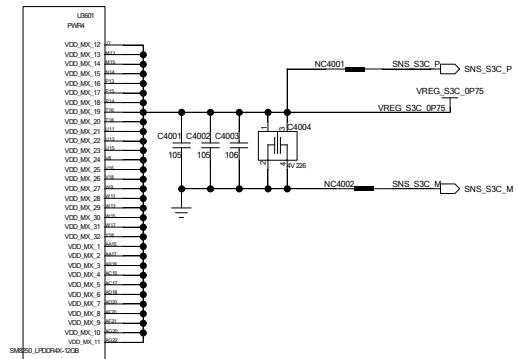
WLAN

Drawn By	Sign	Date	Type:
Checked By			Draw No: Schematic
Standard By			Sheet 39 of 39
Approved By			oppor

SDM865 RF_INTERFACE

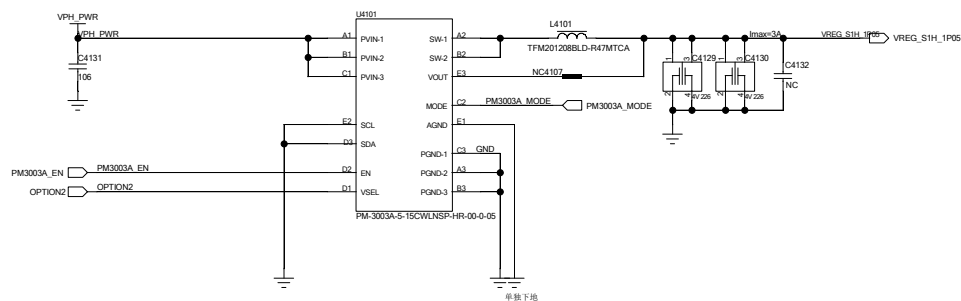
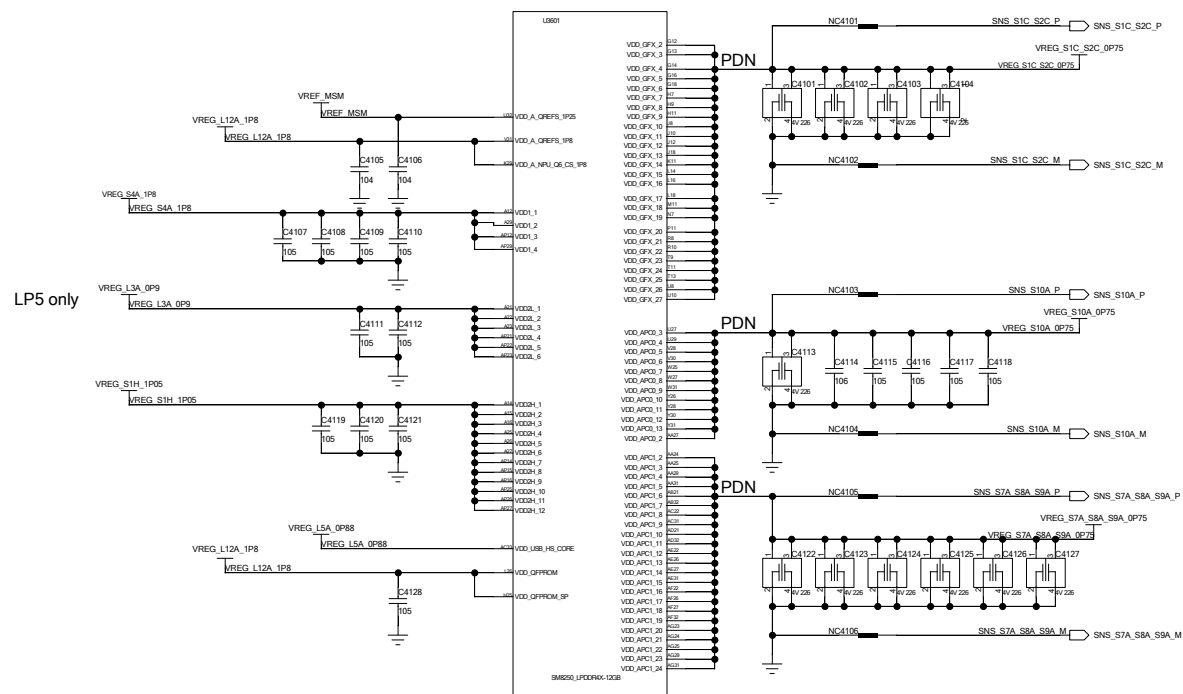


SDM865 PWR4/ATEST



	Sign	Date	Type
Drawn By			Draw No: Schematic
Checked By			Sheet 40 of 50
Standard By			Office
Approved By			oppo

SDM865 PWR1



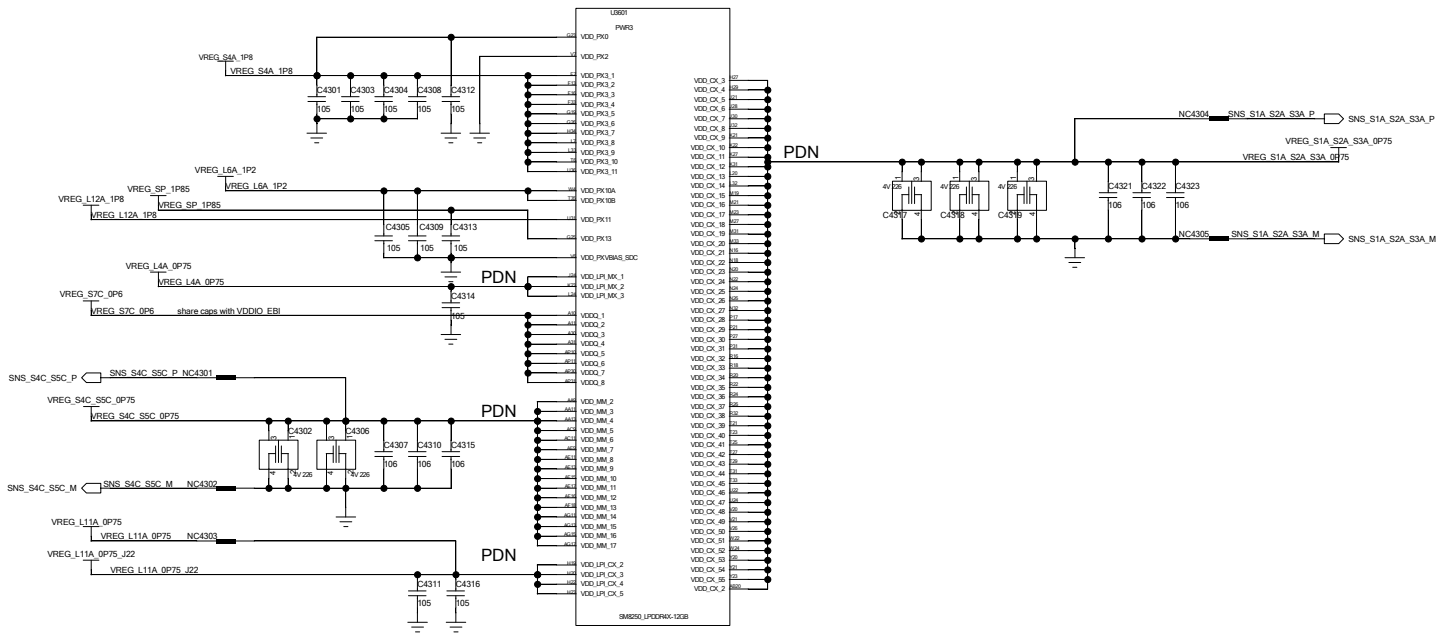
Sign	Date	Type
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Checked By		Sheet 41 of 41
Standard By		Standard By
Approved By		Approved By

oppo

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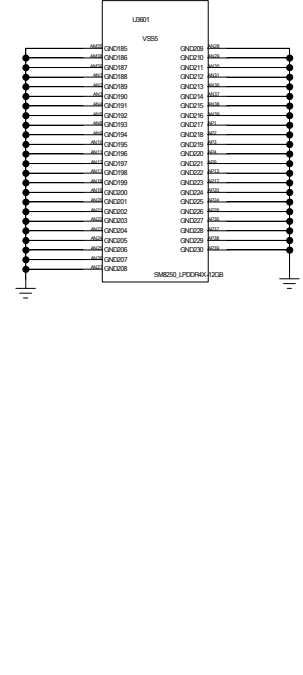
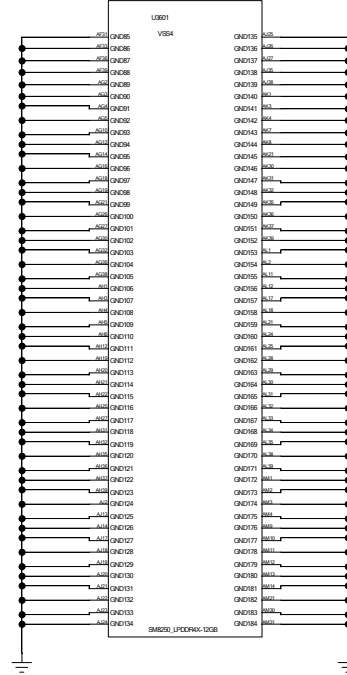
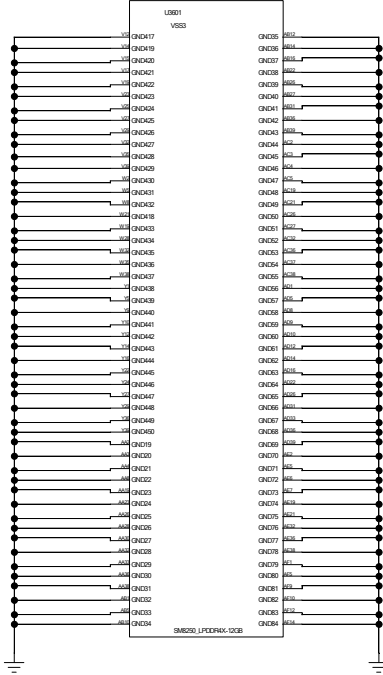
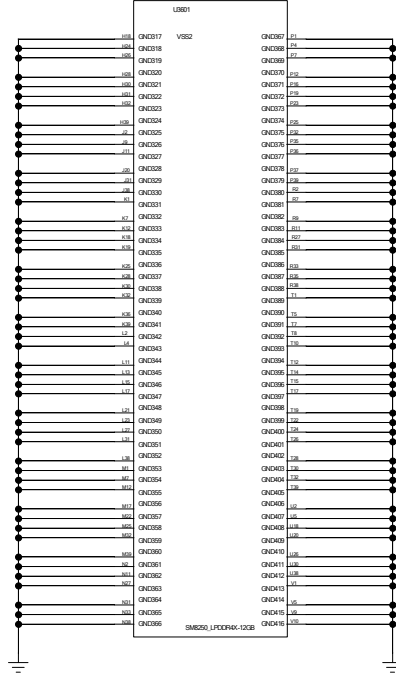
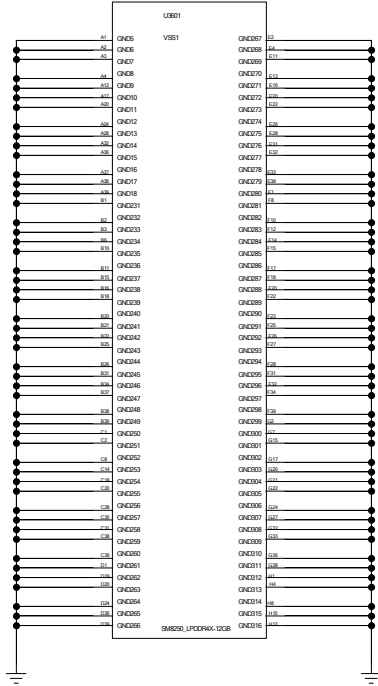
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SDM865 PWR3



	Sign	Date	Type:
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Checked By			Sheet 43 of 50
Standard By			Ver: 1.0
Approved By			oppo

SDM865 GND/NC



Sign	Date	Type:
Drawn By	44	Schematic
Checked By	44	Sheet
Standard By		
Approved By		

oppo

PMR735B_RF_PMIC

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Drawn By			Draw No.	Schematic:	
Checked By			Sheet	45 No. 96	Ver:
Standard By					
Approved By					

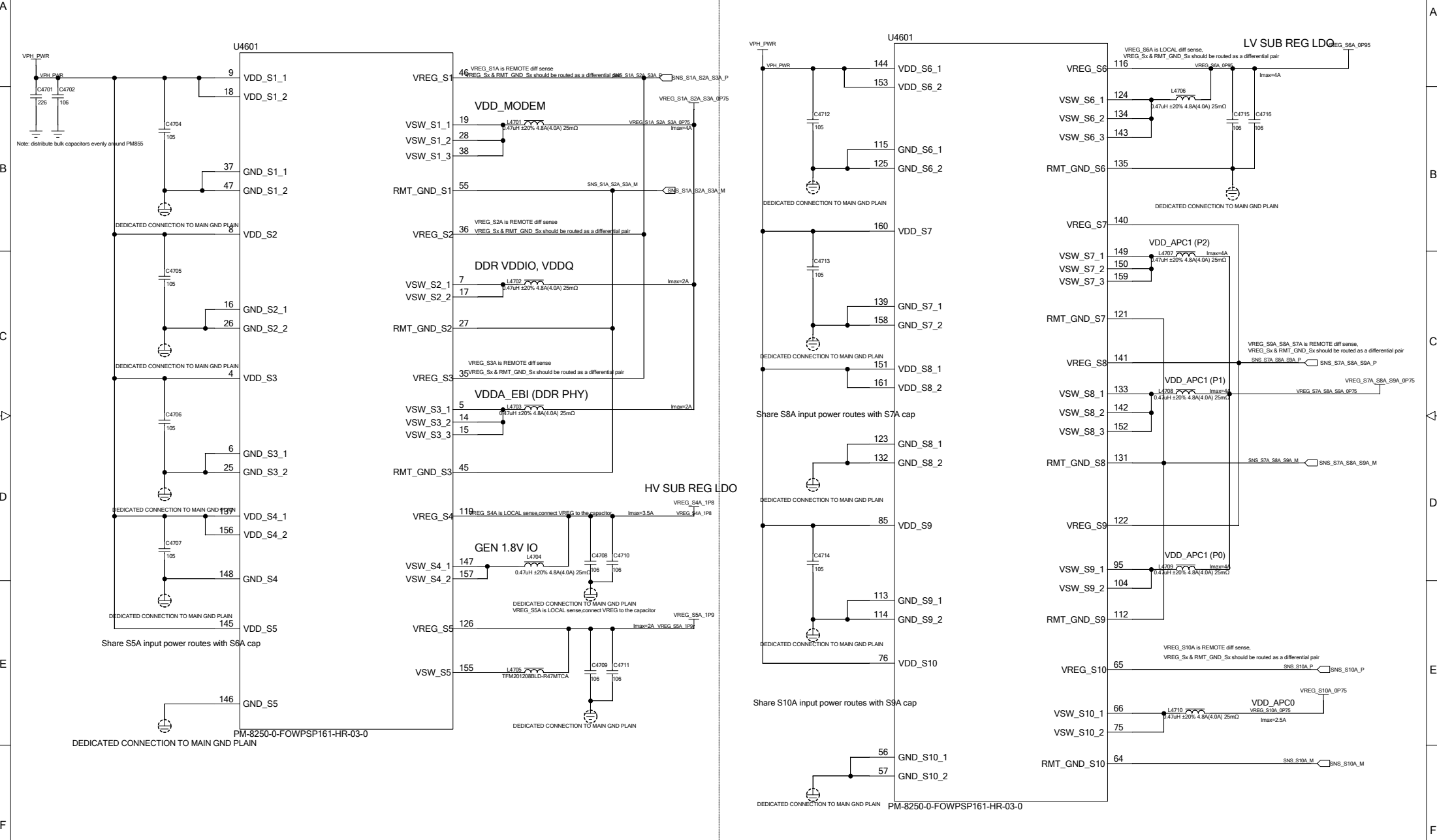
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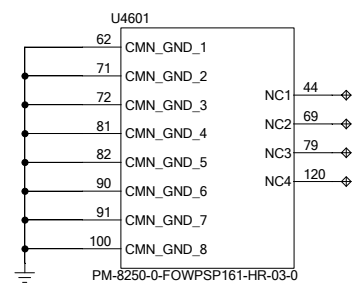
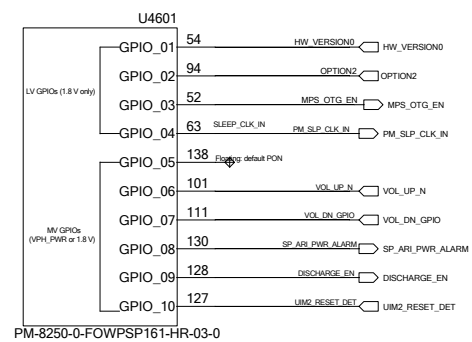
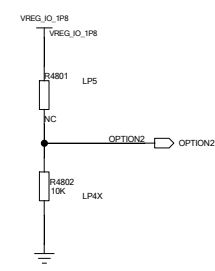
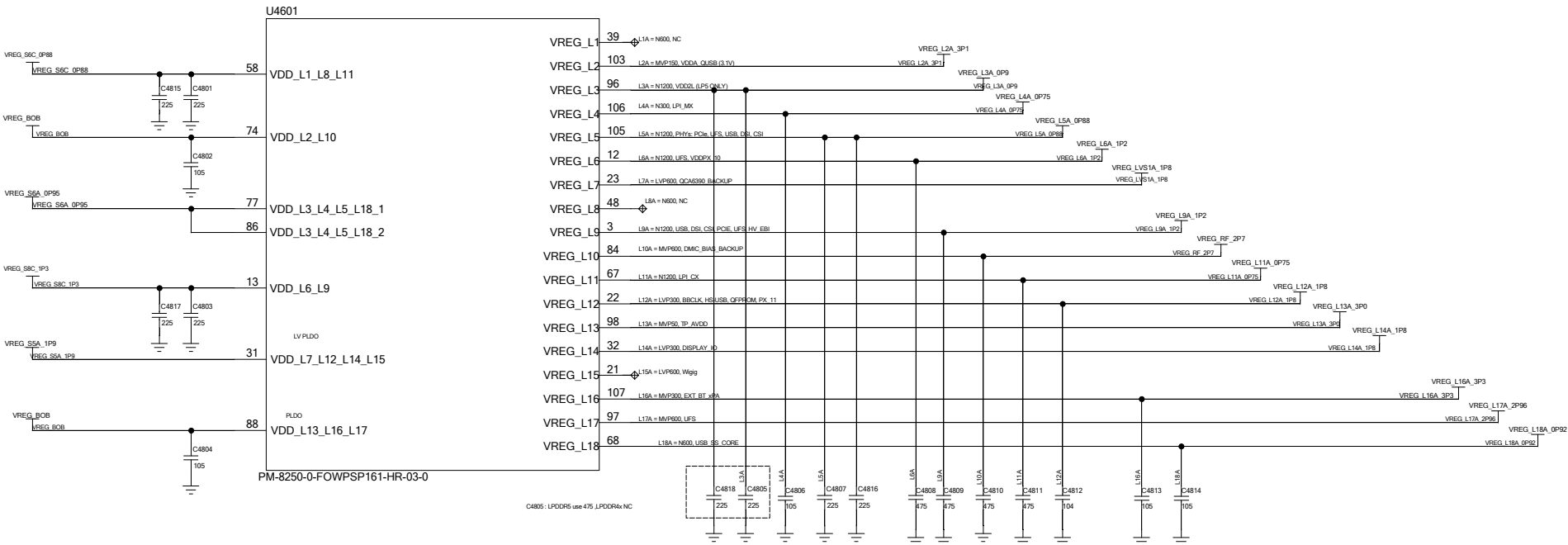
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Checked By			45-80000-ENTRREGIPROBAND Ver:
Standard By			
Approved By			



PM855_BUCK



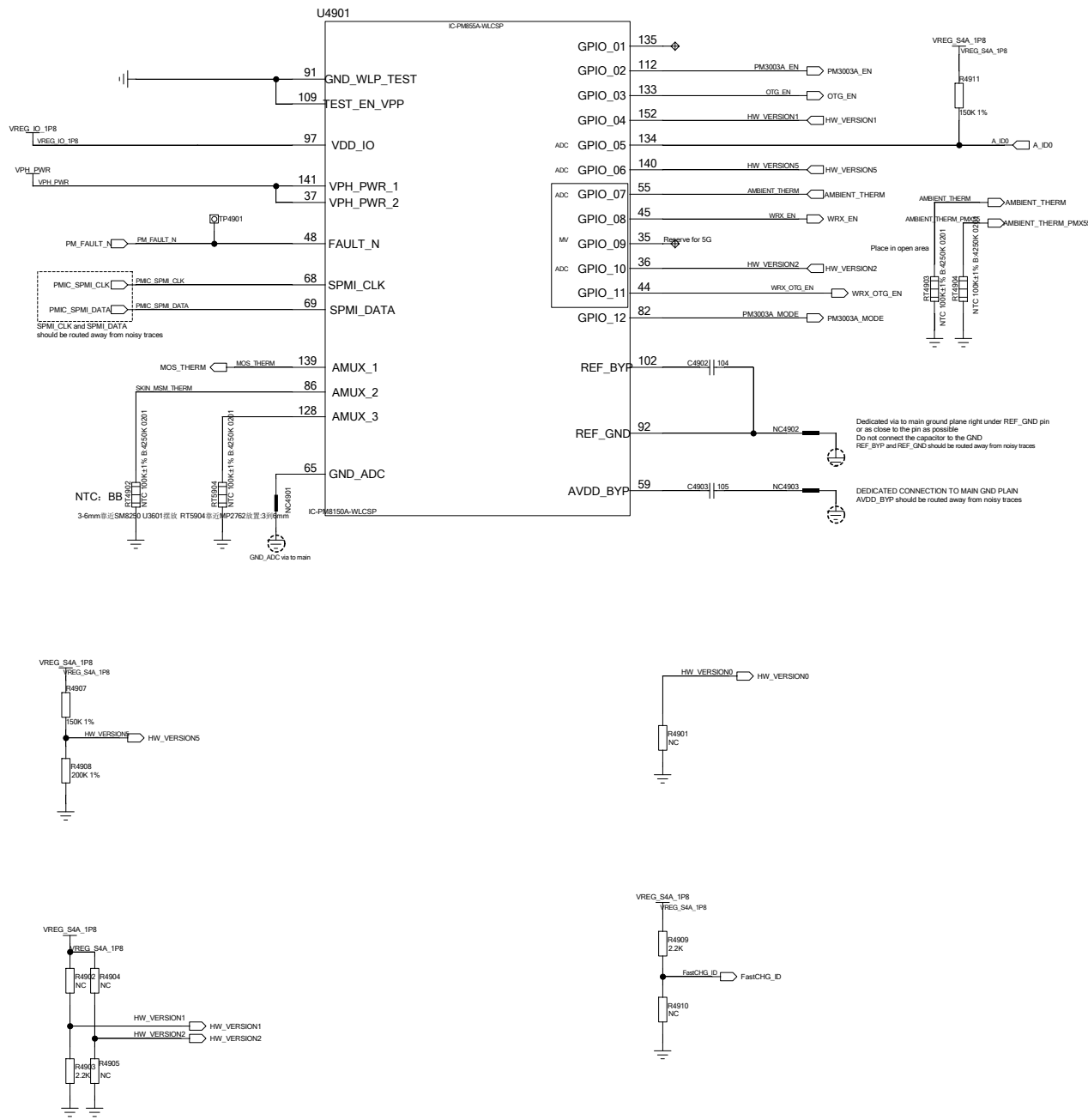
PM855_LDOS/GPIO/GND



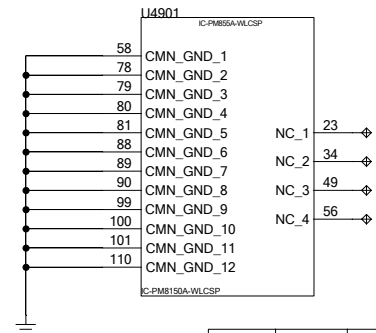
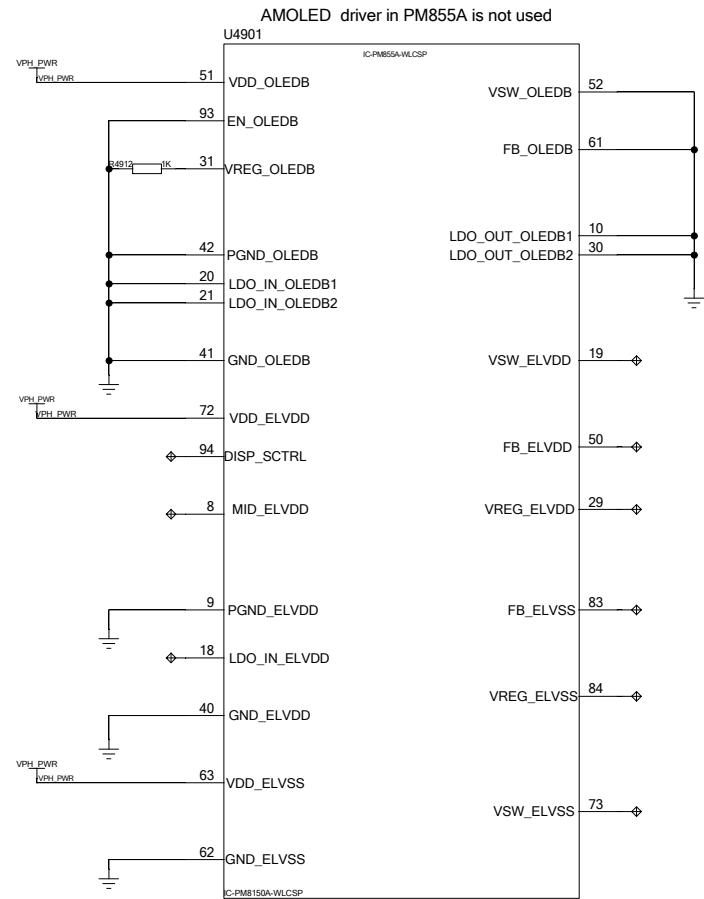
Drawn By	Sign	Date	Type
Checked By			Draw No: SchematPM855_LDOS/GPIO/GND
Standard By			Sheet of Ver:
Approved By			




PM855A_CONTROL/GPIO

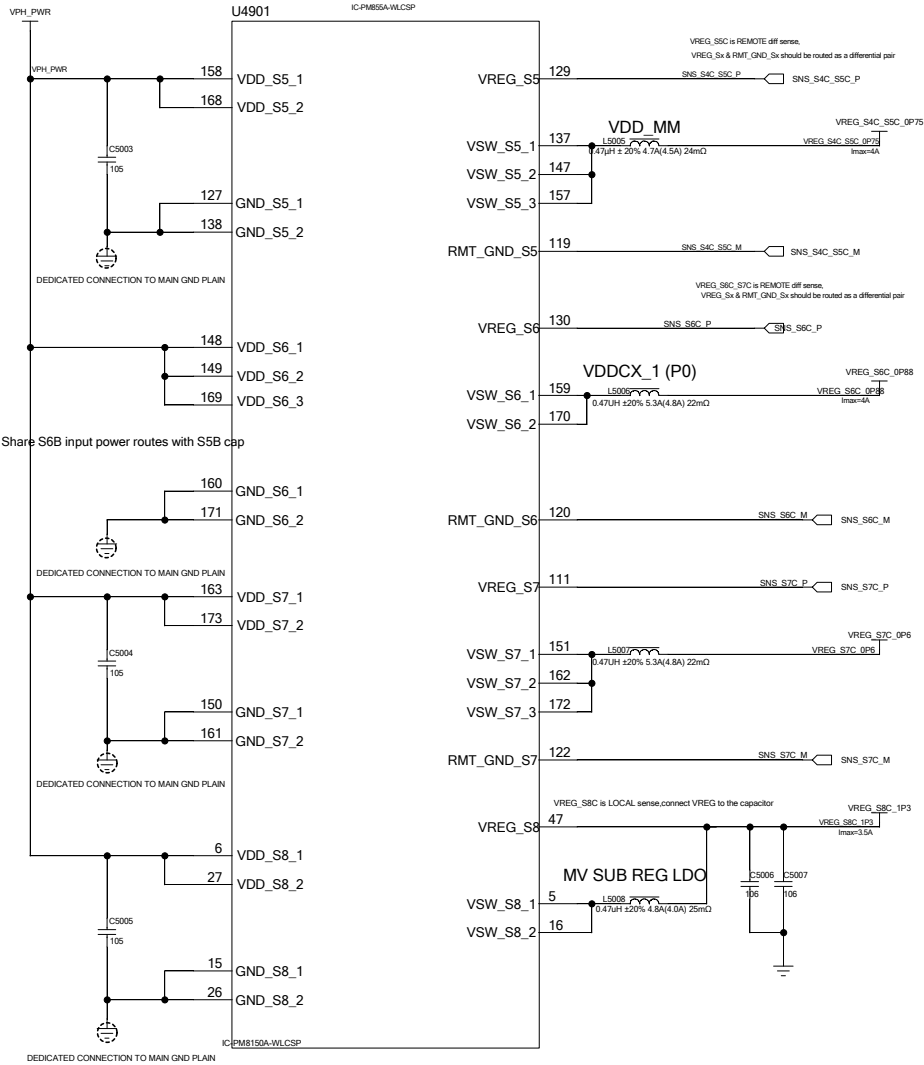


PM855A_OLEDB/AB/IBB/ELVDD/ELVSS

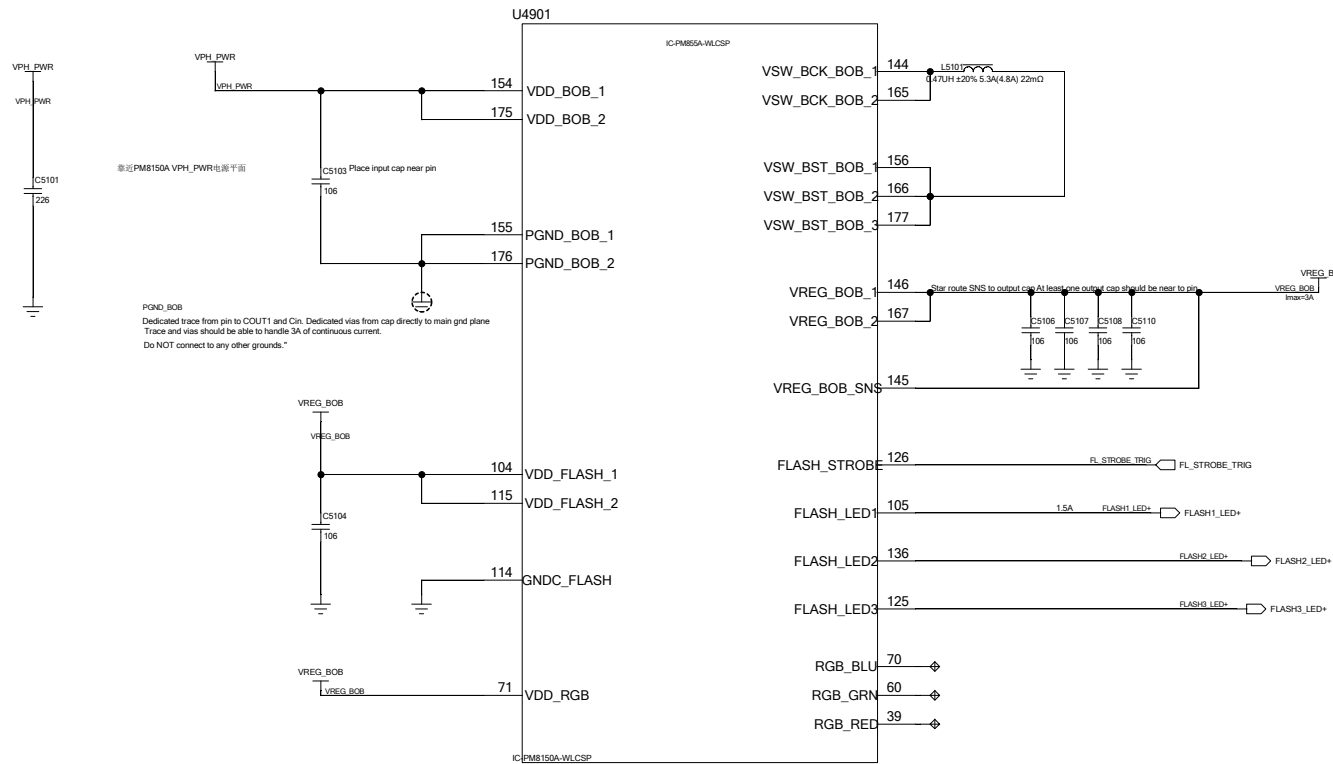
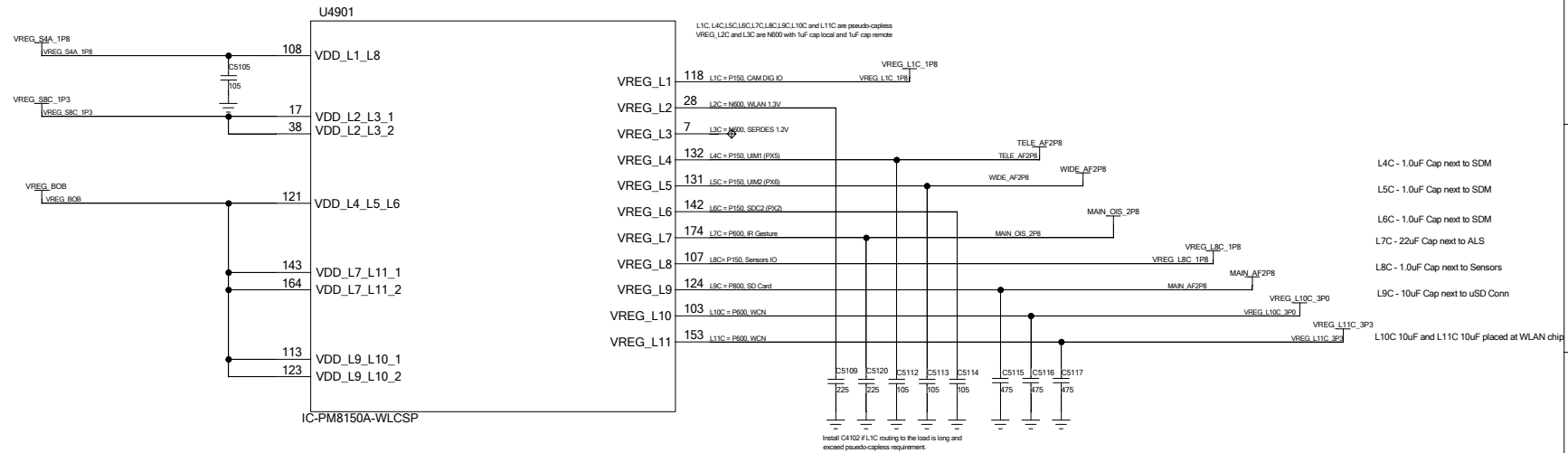



	Sign	Date	Type:	
Drawn By			Draw No:	SC-20150501-CONTROL/GPIO/0001
Checked By			Sheet	of Ver:
Standard By				
Approved By				

F

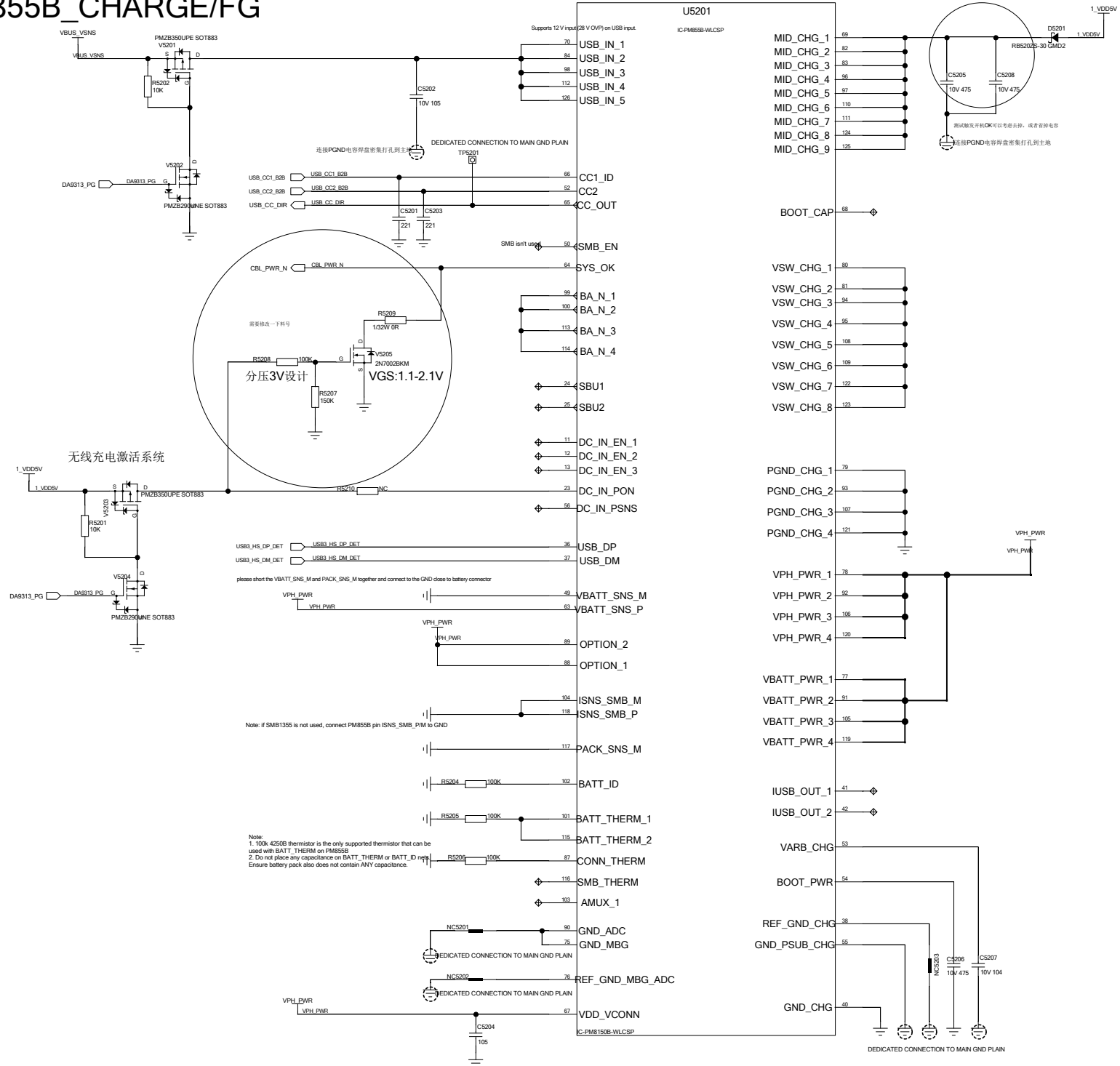
F


PM855A_LDOS/BOB/FLASH



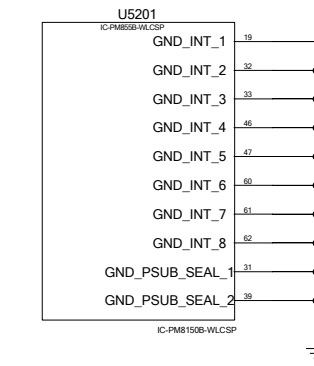
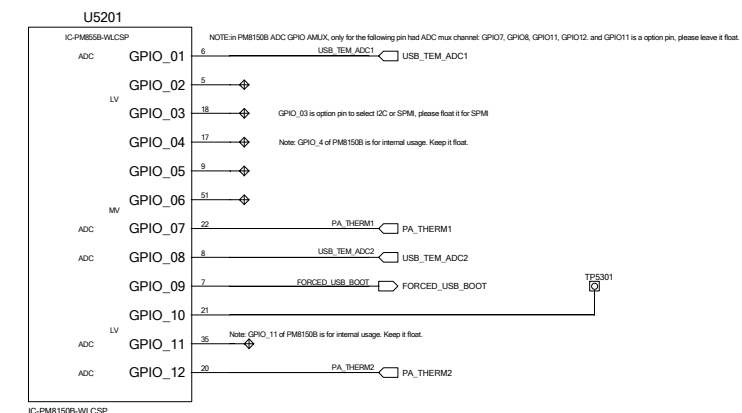
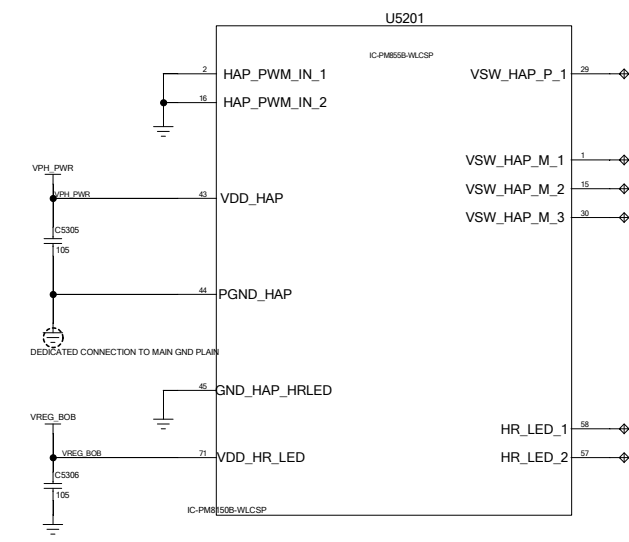
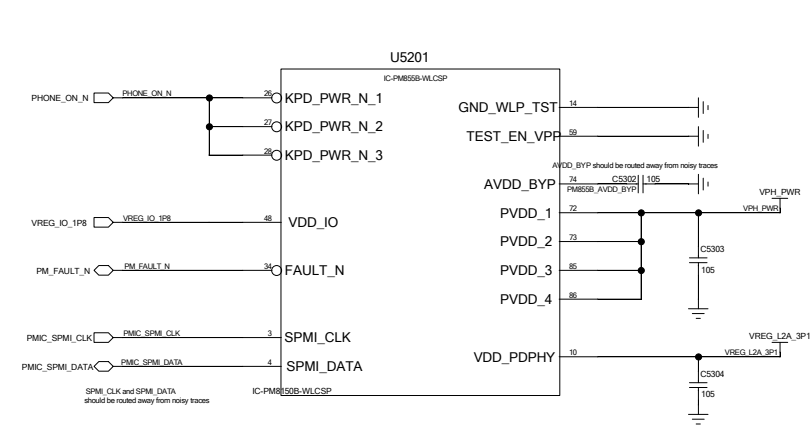
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Drawn By			Draw No: <u>Schedul</u> <u>150A_LDOS/BOB/FLSM</u>	
Checked By			Sheet	of Ver:
Standard By				
Approved By				

PM855B_CHARGE/FG



	Sign	Date	Type:	
Drawn By			Draw No: S2_PMB150B_CHARGEFG	
Checked By			Sheet	Schematic Ver: 96
Standard By				
Approved By				

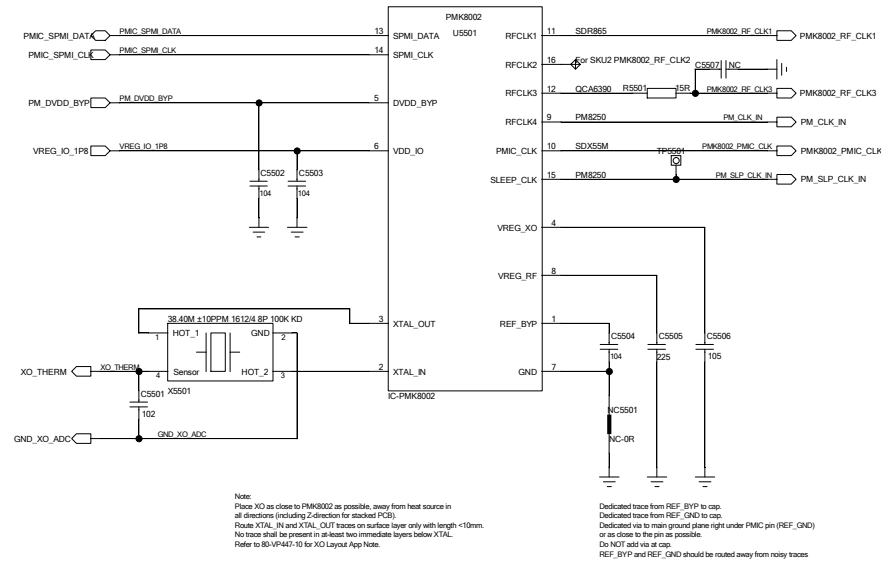
PM855B_HK/GPIO



Drawn By	Sign	Check	Type
Checked By			Drawn By: Schemata@PM855B-HK/GPIO 196
Standard By			Sheet of Ver:
Approved By			

oppo

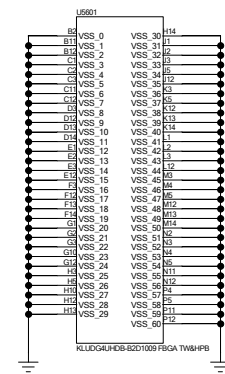
PMK8002



	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By			Sheet 55 of 55 Ver:
Standard By			
Approved By			




F



POP LPDDR5/LPDDR4X



	Sign	Date	Type:	
Drawn By			Draw No: Schematic	
Checked By			Sheet MEMORY_USB 96	Ver:
Standard By				
Approved By				

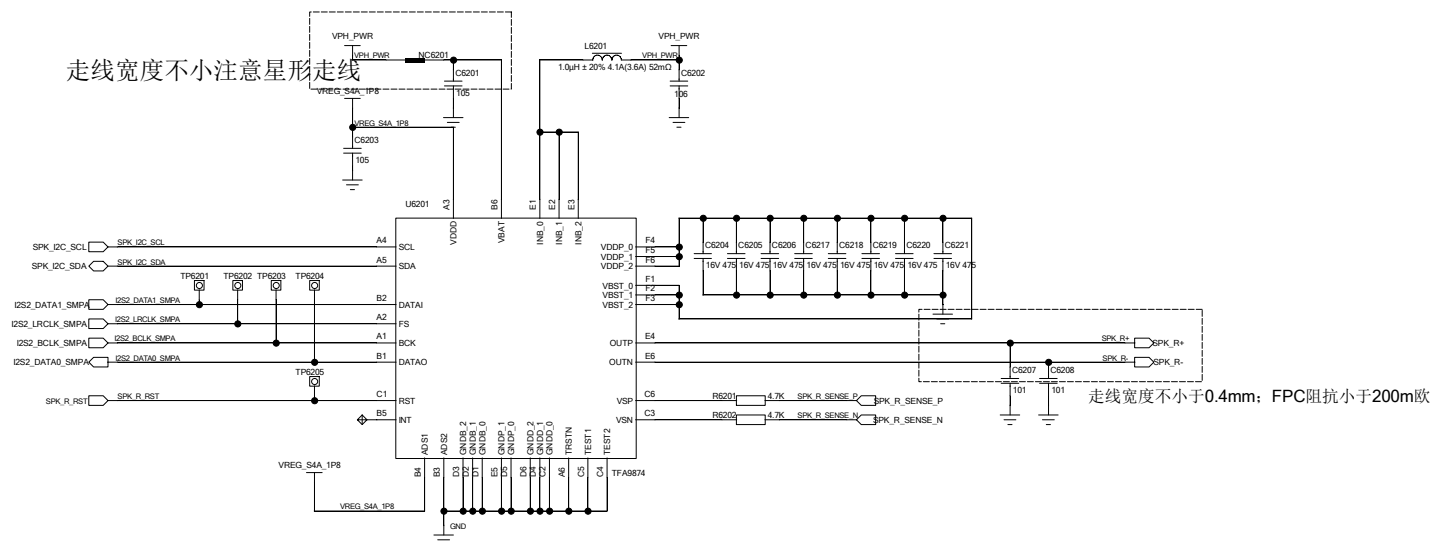
A



C

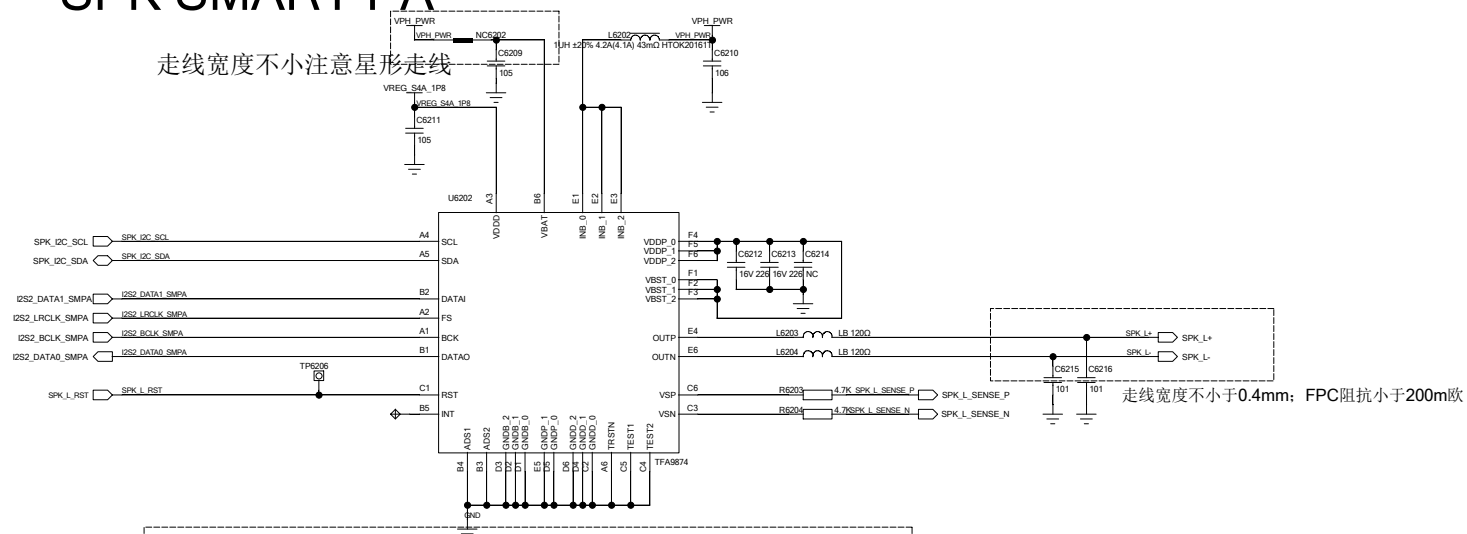
F

测试点禁止删除，量产后用油墨覆盖




PGND需要连成地岛然后再单独打孔下主地，地孔需要尽量多；

SPK SMART PA



PGND需要连成地岛然后再单独打孔下主地，地孔需要尽量多。

	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By			Sheet of 96 62 AUDIO Smart PA AK4377 Ver:
Standard By			
Approved By			

A

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A

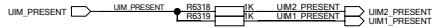
B

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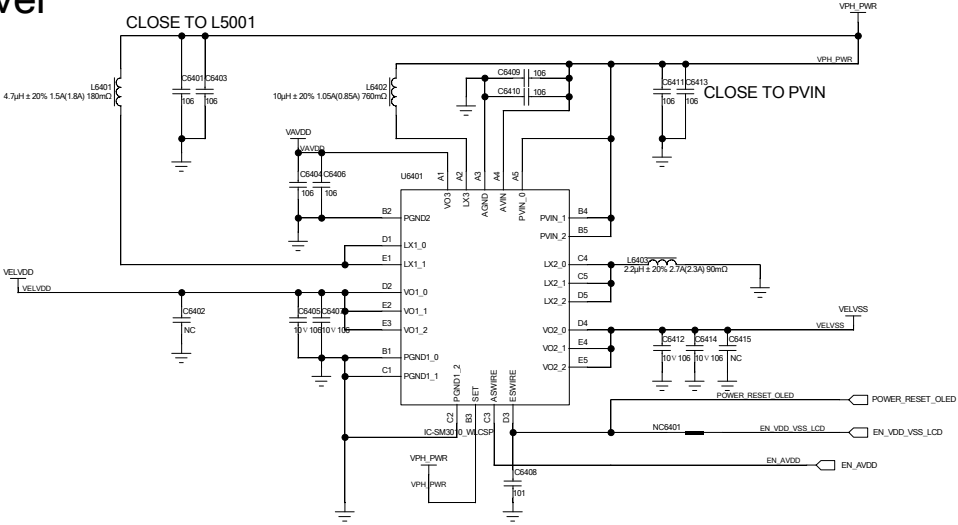
E

F

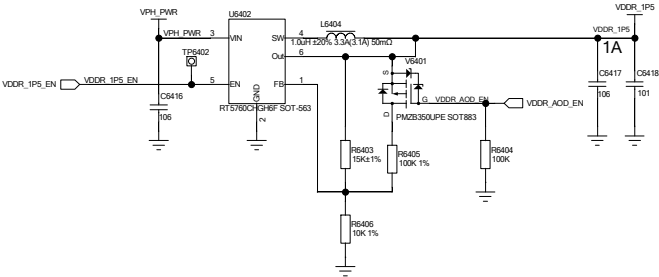


	Sign	Date	Type:	
Drawn By			Draw No: Schematic	
Checked By			638467P_IL_Dra	BTB6 Ver:
Standard By			oppo	
Approved By				

OLED Driver



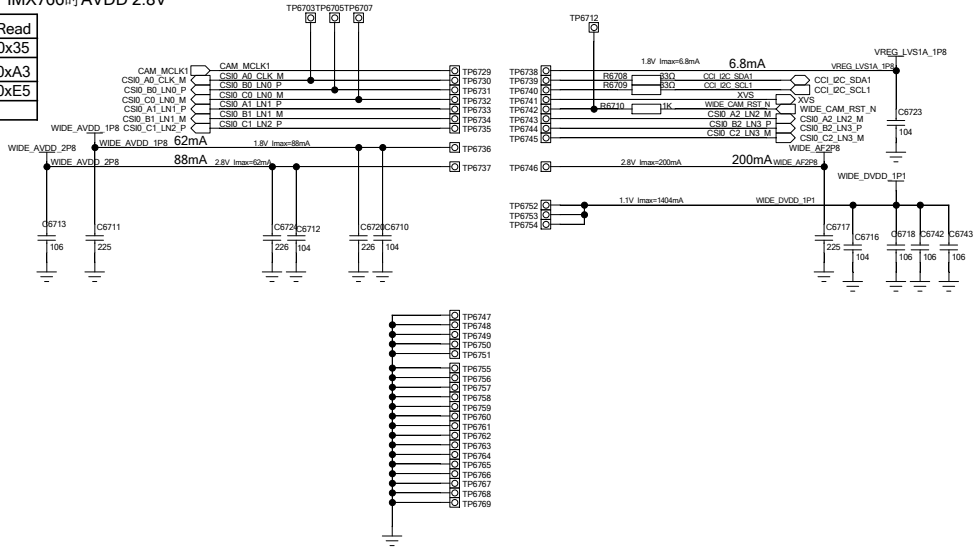
OLED_DCDC



WIDE_Camera 50M

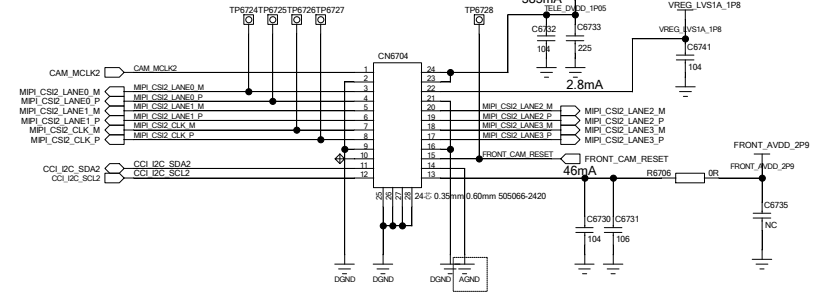
DVT前使用IMX686; 后使用IMX766
IMX686时AVDD 2.9V; IMX766时AVDD 2.8V

IMX686	Write	Read
SENSOR	0x34	0x35
EEPROM	0xA2	0xA3
AF DRIVER	0xE4	0xE5

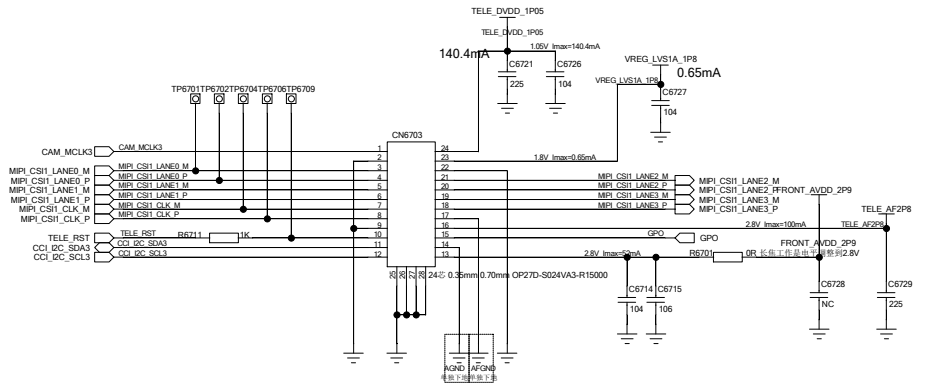


Front_Camera1_32M

IMX686	CCU_IC	Write address
CCU device	Address	Write address
LR camera sensor	0x21	0x20
LR camera EEPROM	0xA9	0xA8

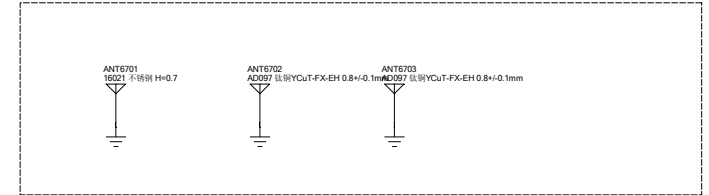


TELE_Camera 13M

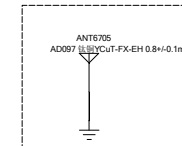


S5K3M5SX04	Write	Read
SENSOR	0x5A	0x5B
EEPROM	0xA0	0xA1
AF DRIVER	0x18	0x19

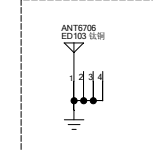
摄像头支架接地弹片



天线接地弹片



摄像头钢片接地弹片-TOP

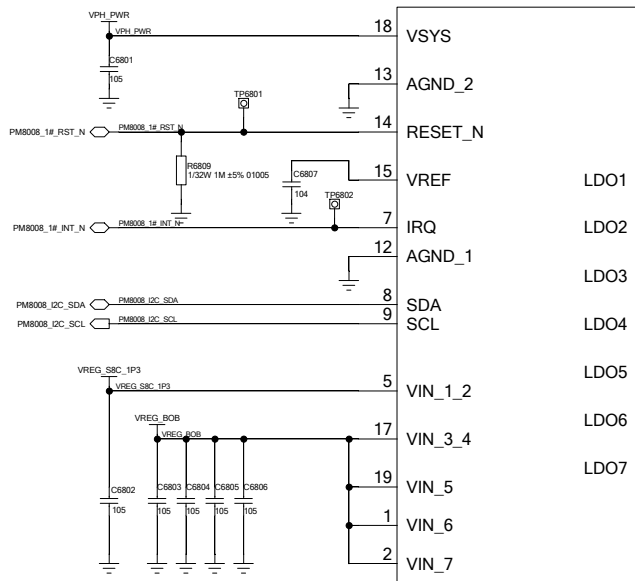


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Drawn By	Draw No	Schematic
Checked By	Sheet	07_CAMERA0818 Ver.
Standard By		
Approved By		

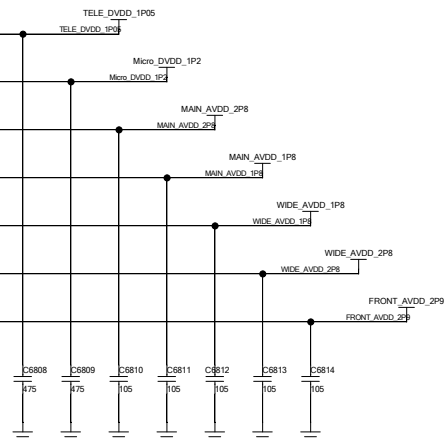
oppo

PM8008

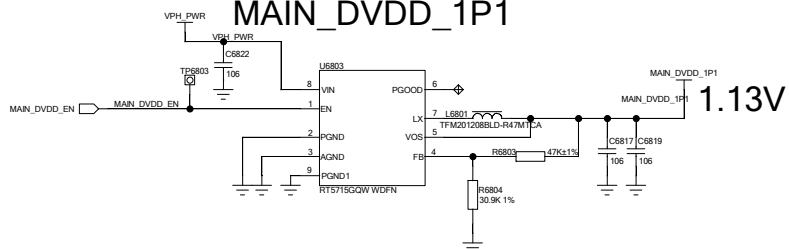
U6802



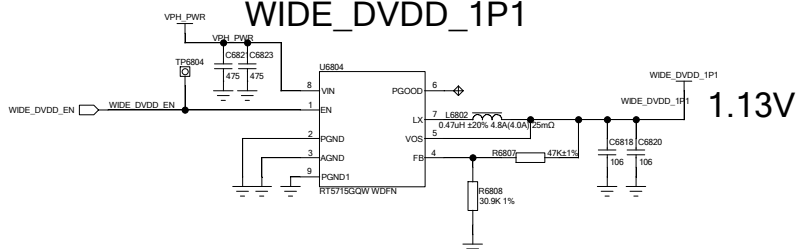
PM-8008-0-WLPSP20-HR-X0-0



MAIN_DVDD_1P1



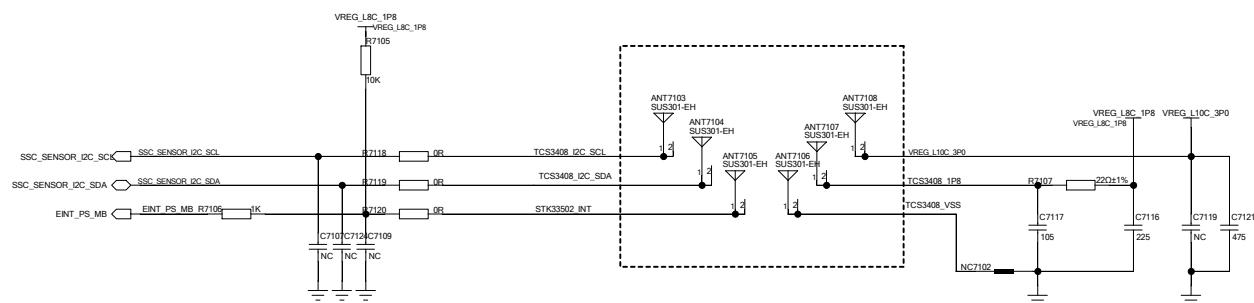
WIDE_DVDD_1P1




Sign	Date	Type
Drawn By		Draw No: Schematic
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Standard By		
Approved By		

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TO J1 Board




	Sign	Date	Type:		
Drawn By			Draw No: Schematic		
Checked By			Sheet	of 96	Ver:
Standard By					
Approved By					

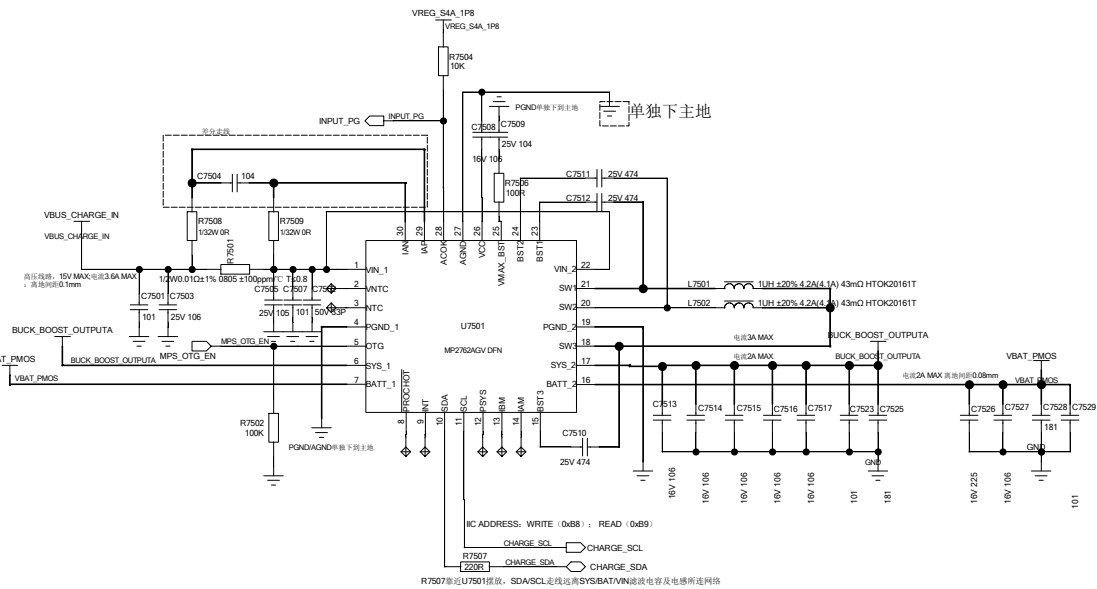
F



开关状态	电平	
	USB SW_CTRL1	USB SW_CTRL
USB应↔手机UART通路	L	L
USB应↔快充ASIC USB通路	H	L

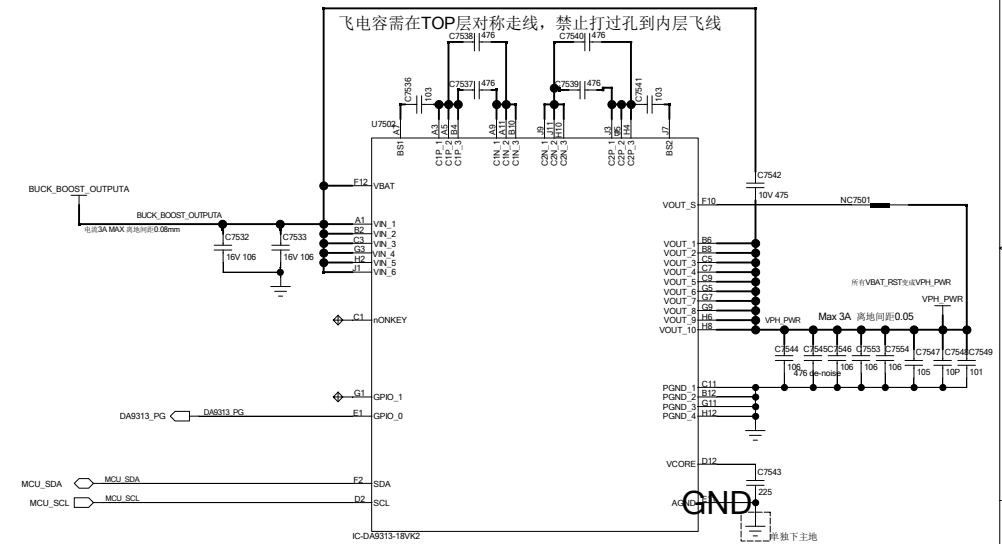
	Sign	Date	Type:	
Drawn By			Draw No: Schematic	
Checked By			Sheet	of 96 Ver:
Standard By				
Approved By				


BUCK-BOOST CHARGE



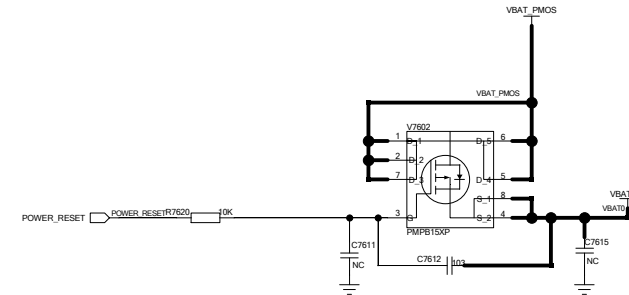
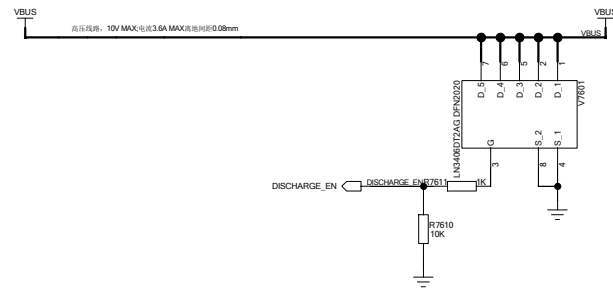
CHARGE PUMP

兼容单电芯时全部NC



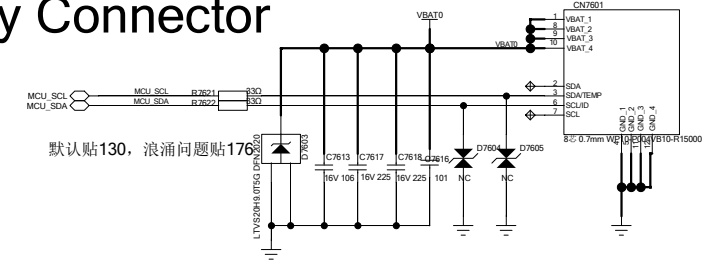
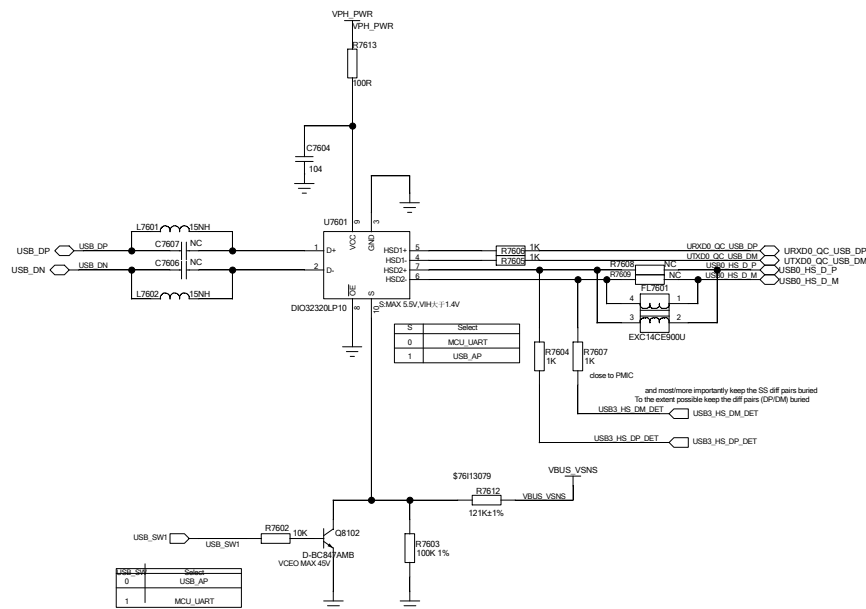
	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By		75.015668	BUCK, BQ85T, PUMP
Standard By			Ver:
Approved By			


HW RESET



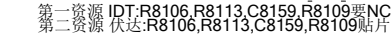
Battery Connector

如果电池座布局右边，正极靠近板内侧，布局左边，负极靠近板子内侧

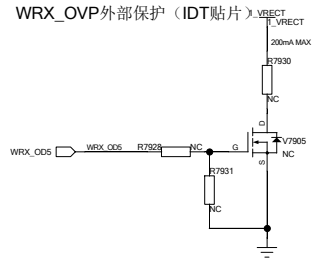


	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By		76 C	6089 BAT_RST_WP_SINTO Ver:
Standard By			
Approved By			

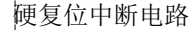
Power Wireless-15W(默认伏达)



R7922默认NC，贴铜片短接
对应位号SH7901

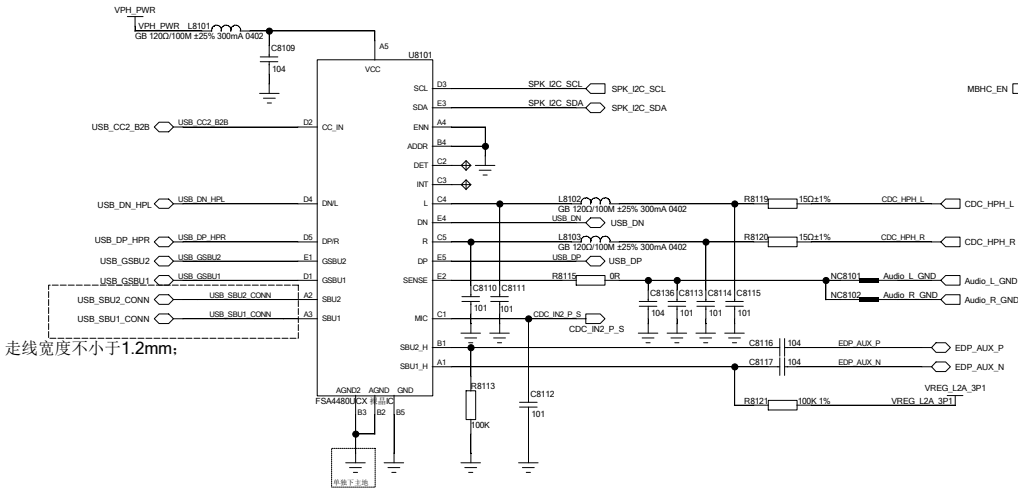


OVP+LoadSwitch

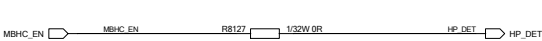


USB Audio Switch

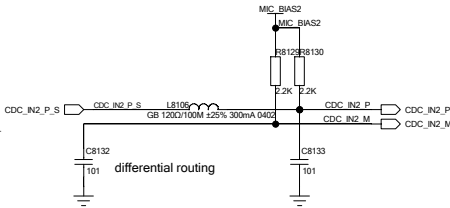
FSA4480UCX I2C Address (R:0x85; W:0x84)



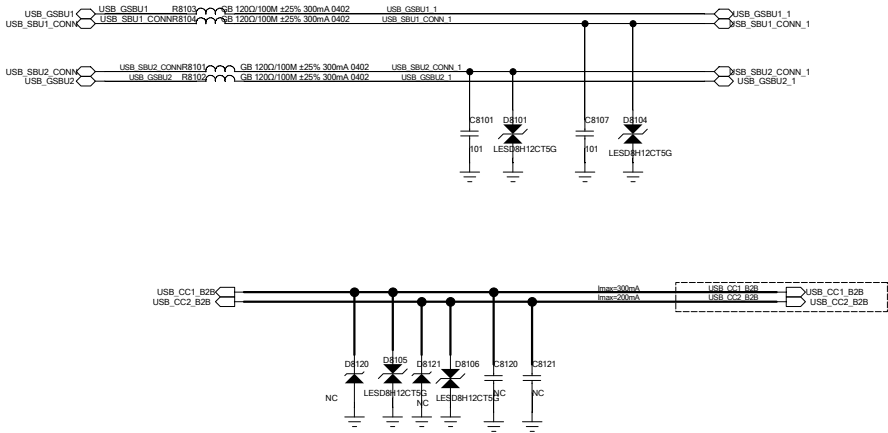
EAR DET



EAR MIC



TO U_FPC



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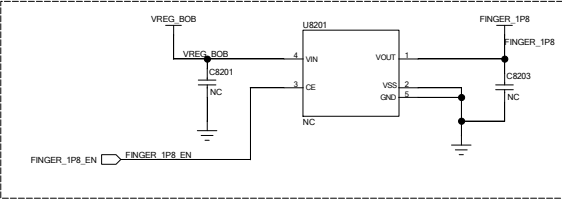
F

TO C1_FPC

指纹、SIM、主mic、天线控制、马达、SPK、版本识别

Micro_Camera_5M

指纹G3兼容电容



	Sign	Date	Type:	
Drawn By			Draw No:	Schematic
Checked By			Sheet	of 41 Ver:
Standard By			oppo	
Approved By				

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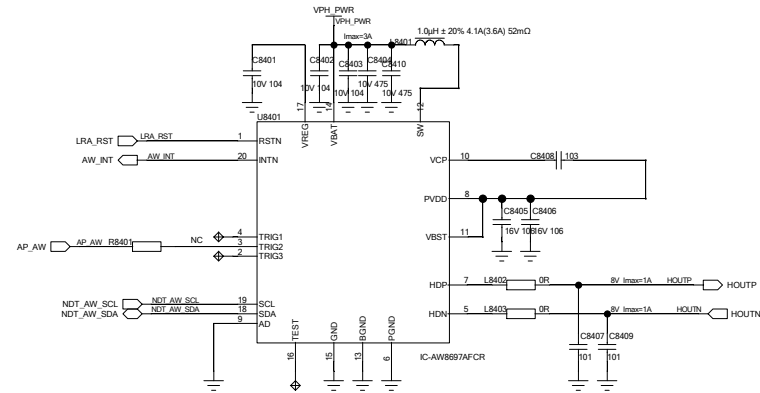
5

6

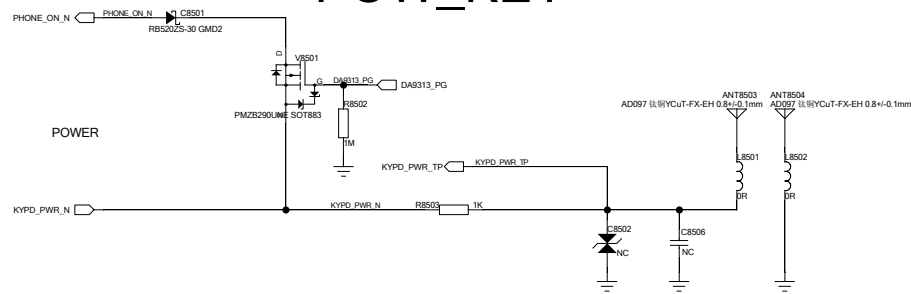
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8

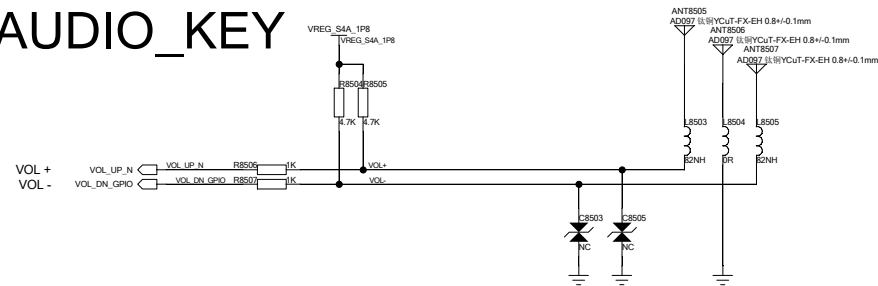
LRA Driver



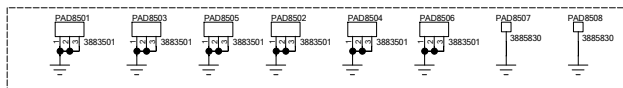
POW_KEY



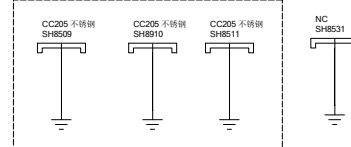
AUDIO_KEY



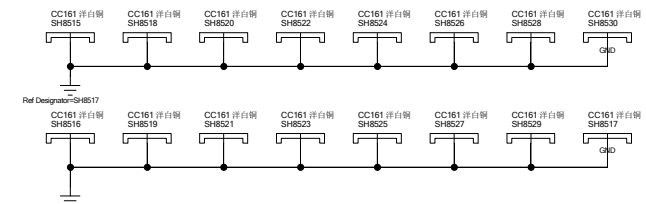
TOP螺钉接地垫片



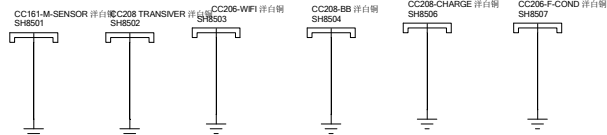
补强钢片



2板4板焊接垫片




屏蔽支架



RF Cable线夹1

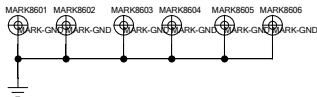


	Sign	Date	Type:	
Drawn By			Draw No: Schematic	
Checked By			Sheet of 96	Ver:
Standard By				
Approved By				

TEST POINT

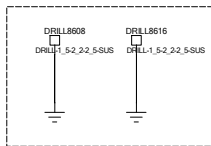


MARK POINT

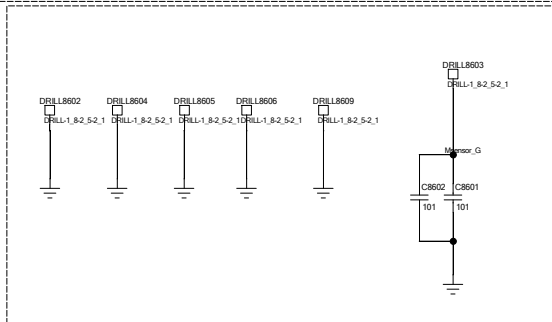
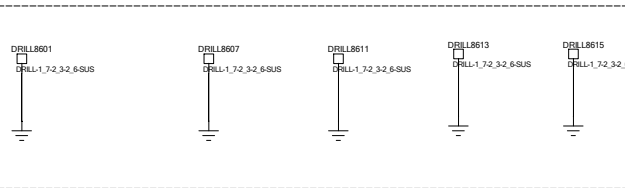


主板螺钉1.7

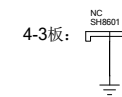
主板螺钉1.5



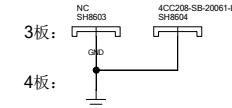
主板螺钉1.8



高温锡膏贴片



低温锡膏贴片



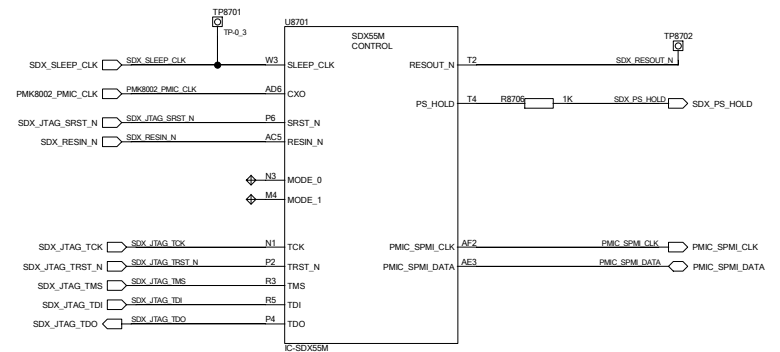
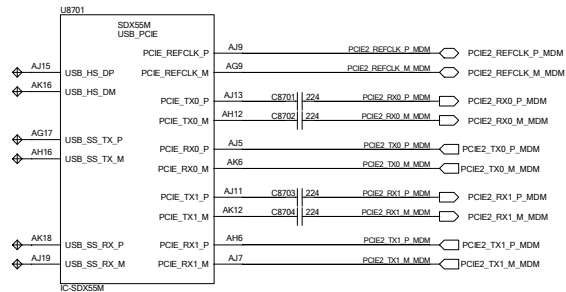
广角摄像头垫高板



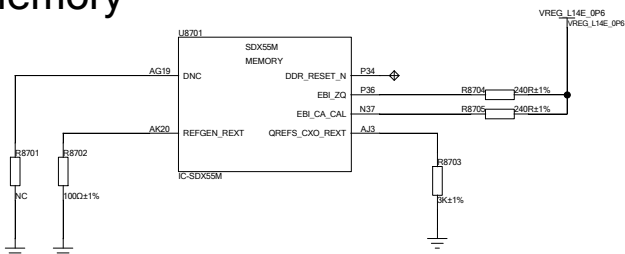
	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By			Sheet 86_1 of Mar12 Ver:
Standard By			
Approved By			

oppo

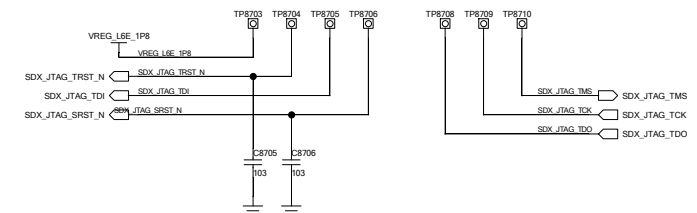
SDX55M - RFFE/ PCIE/ Control



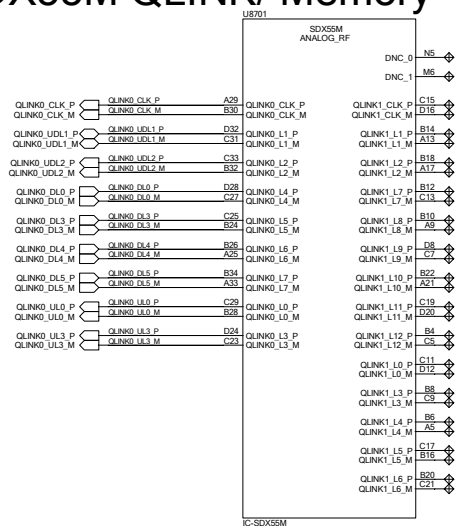
Memory



JTAG



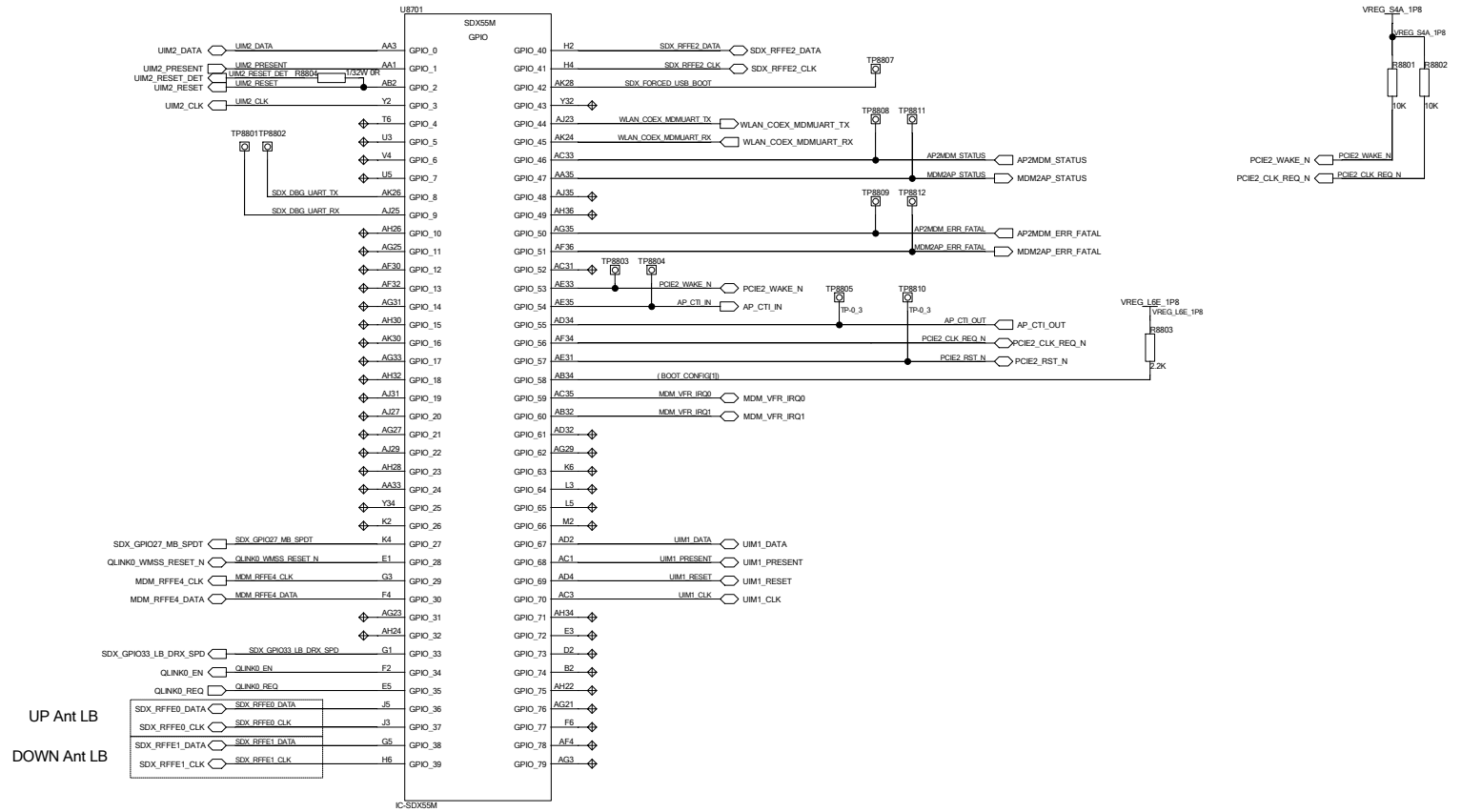
SDX55M QLINK/ Memory




	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By			Sheet of 96 Ver:
Standard By			
Approved By			

oppo

SDX55M_GPIO



Note: Ensure that there are no unintentional external pull-ups on the following GPIOs and these GPIOs are NOT logic high unintentionally before SDX55M comes out of reset GPIO_24, 31, 42, 47, 49, 54, 55, 59, 63 and 75.

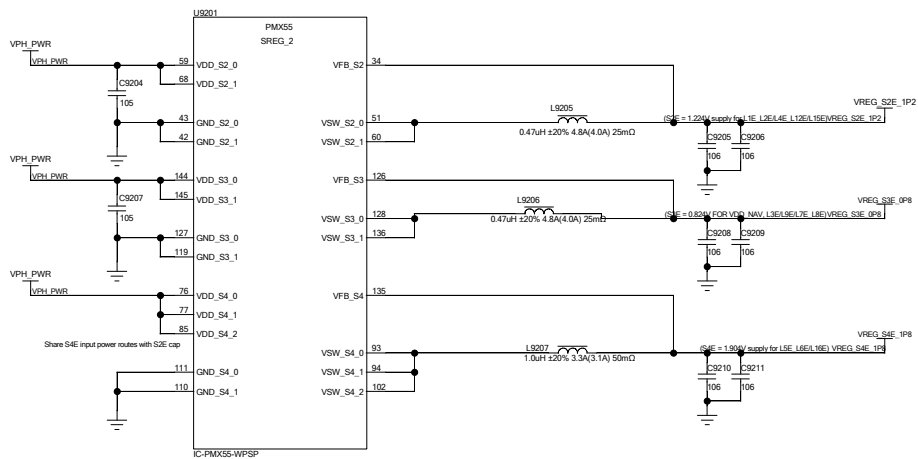
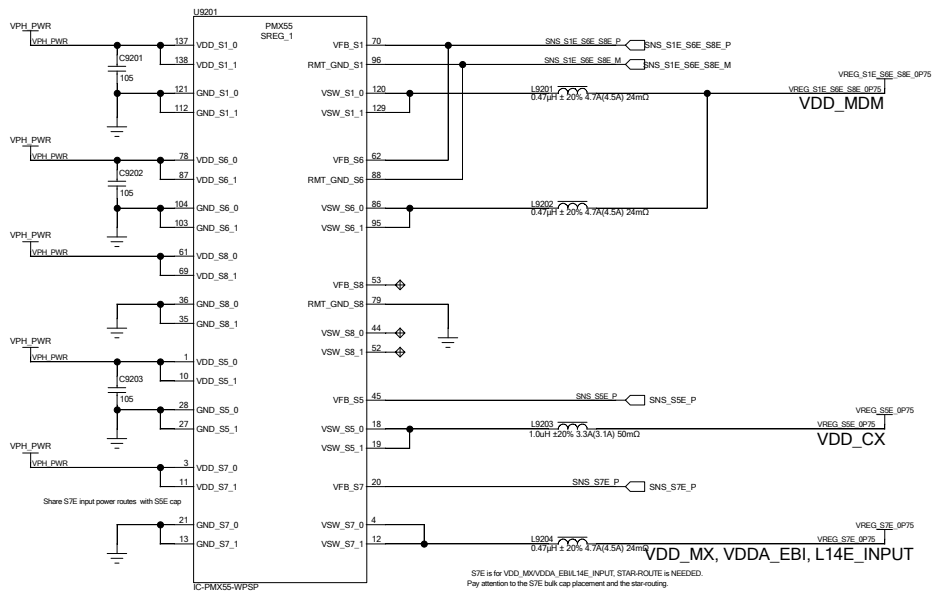
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Drawn By			Draw No: Schematic	
Checked By			Sheet of 96	Ver:
Standard By				
Approved By				


A



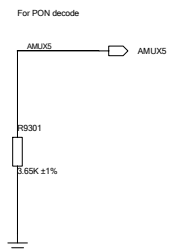
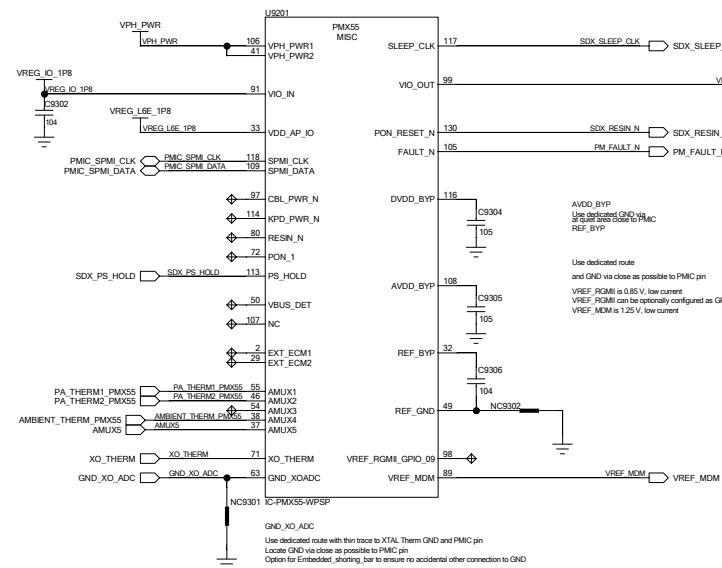
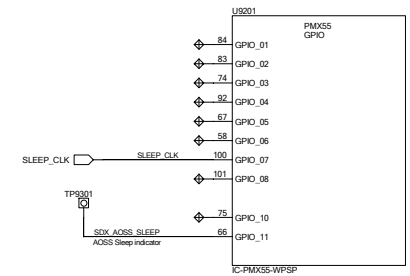
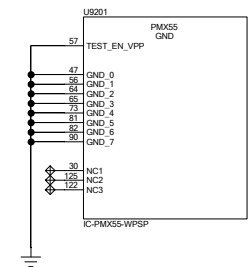
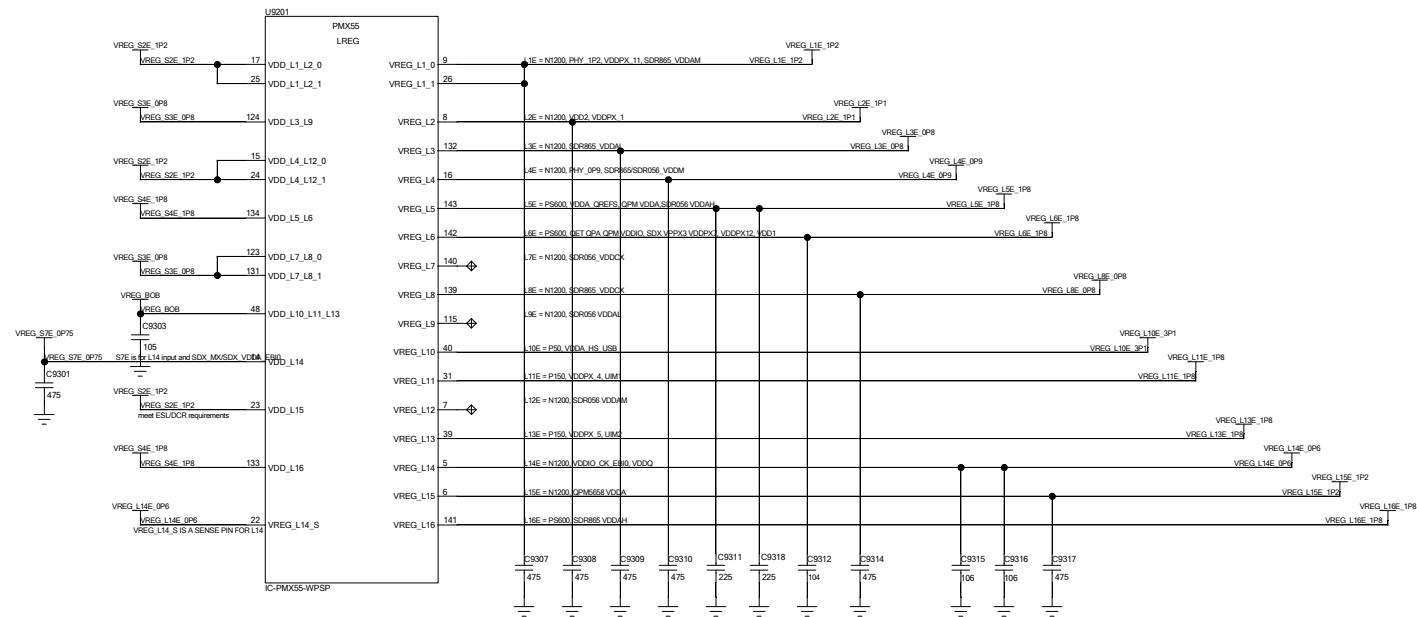
B


PMIC_PMX55_BUCKS

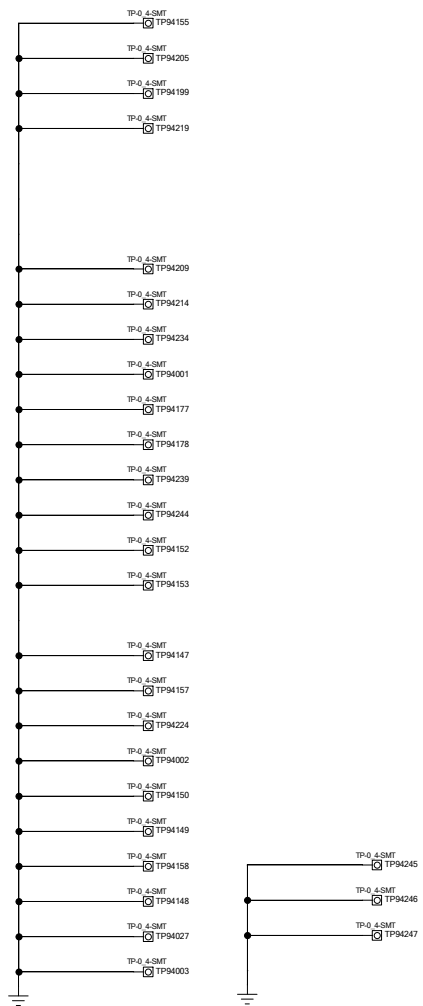


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Drawn By			Draw No: Schematic
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Standard By			
Approved By			

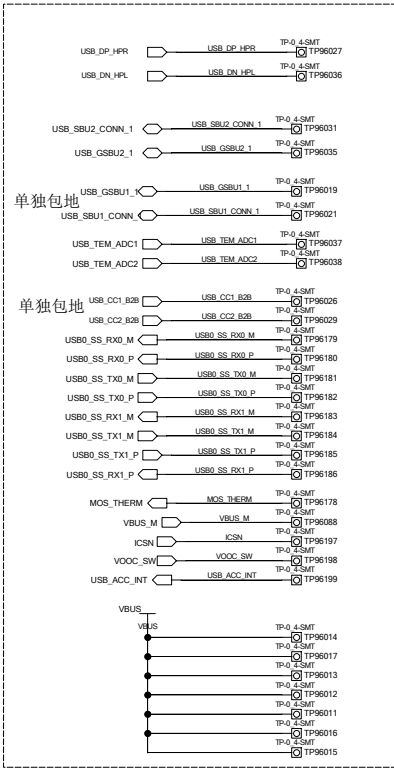
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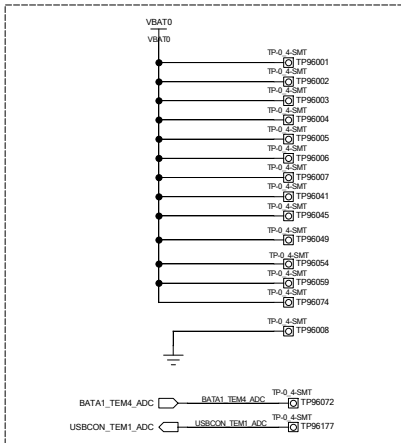
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Drawn By			Draw No.	Schematic
Checked By			Sheet	of 96 Ver:
Standard By				
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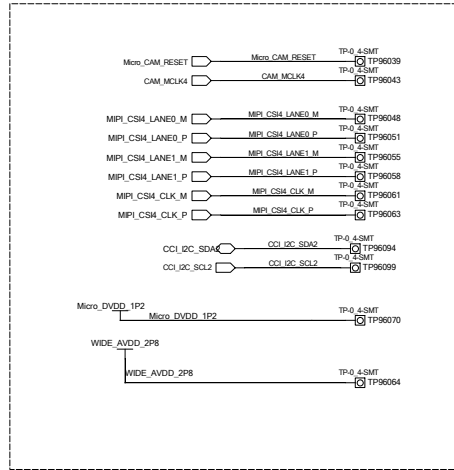
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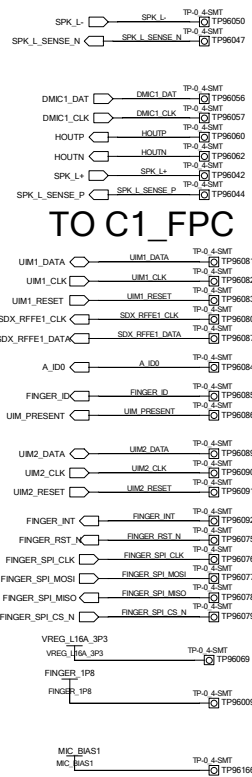
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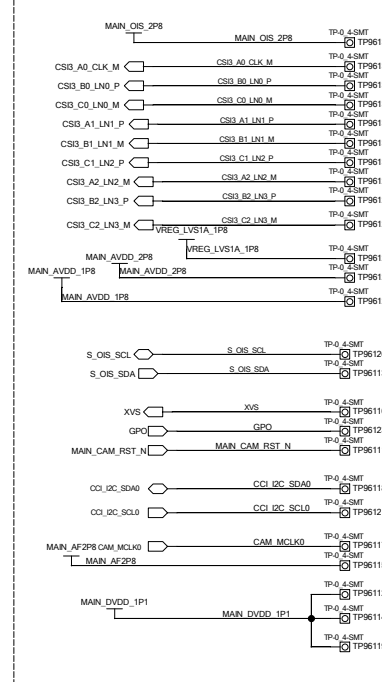
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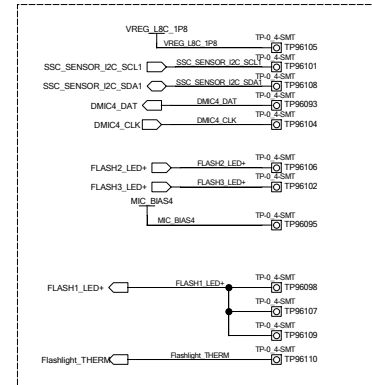
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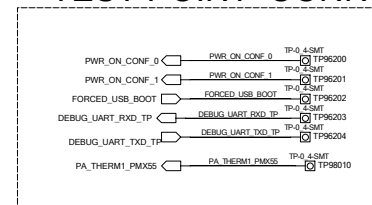
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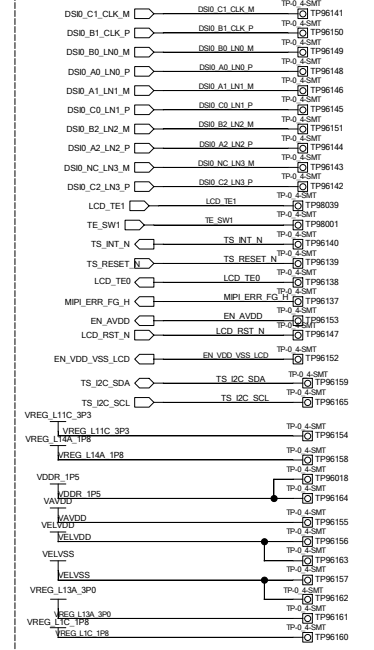
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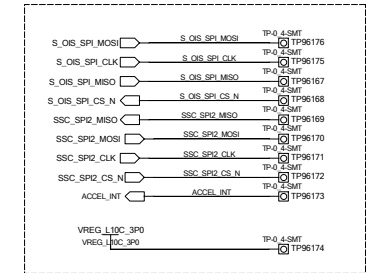
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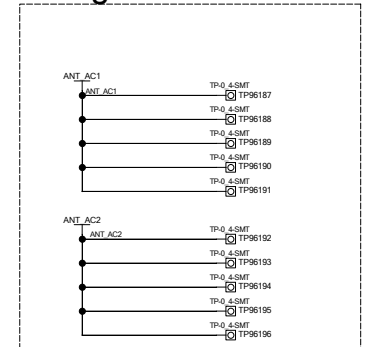
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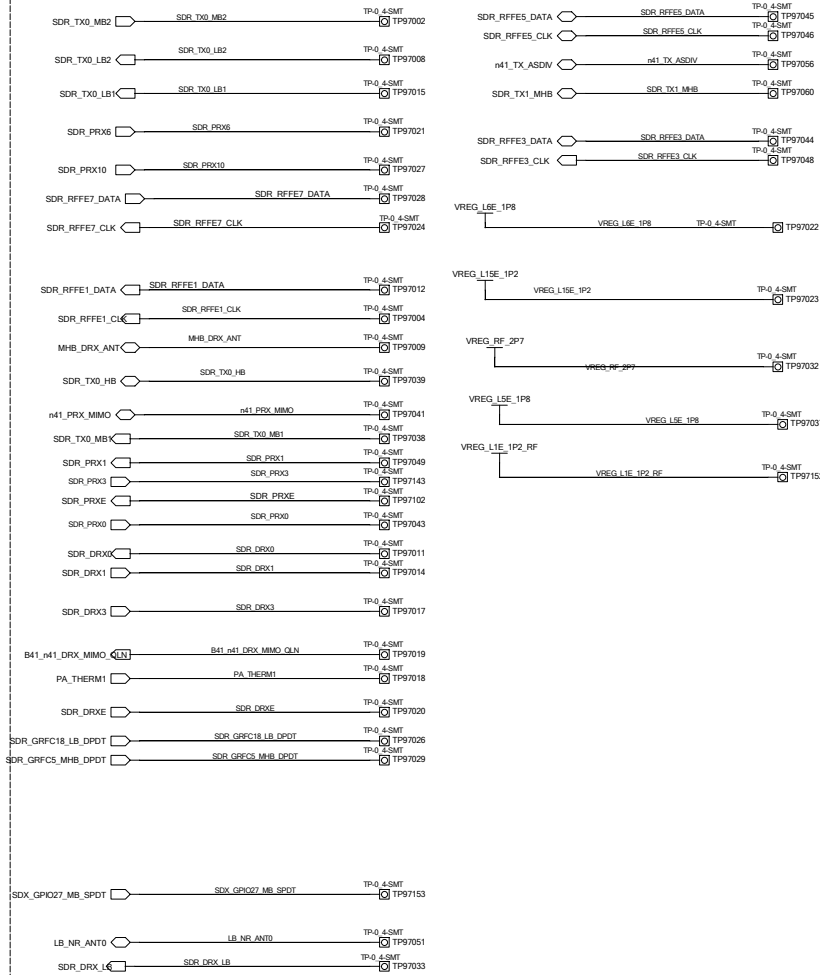
A+G SENOSR CONN



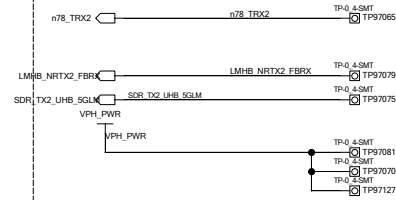
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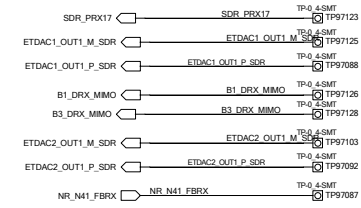
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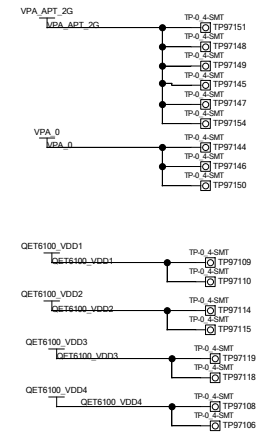
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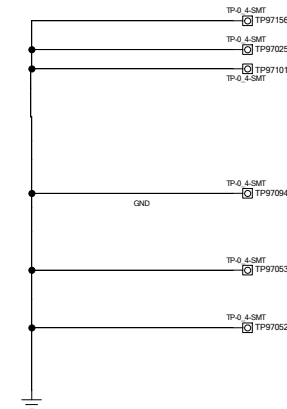
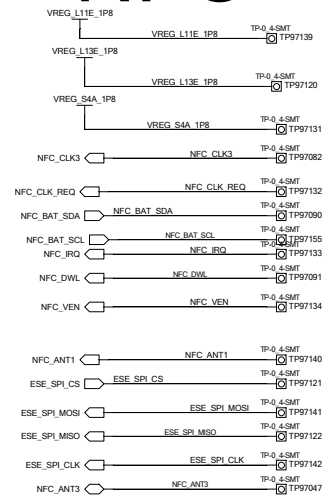
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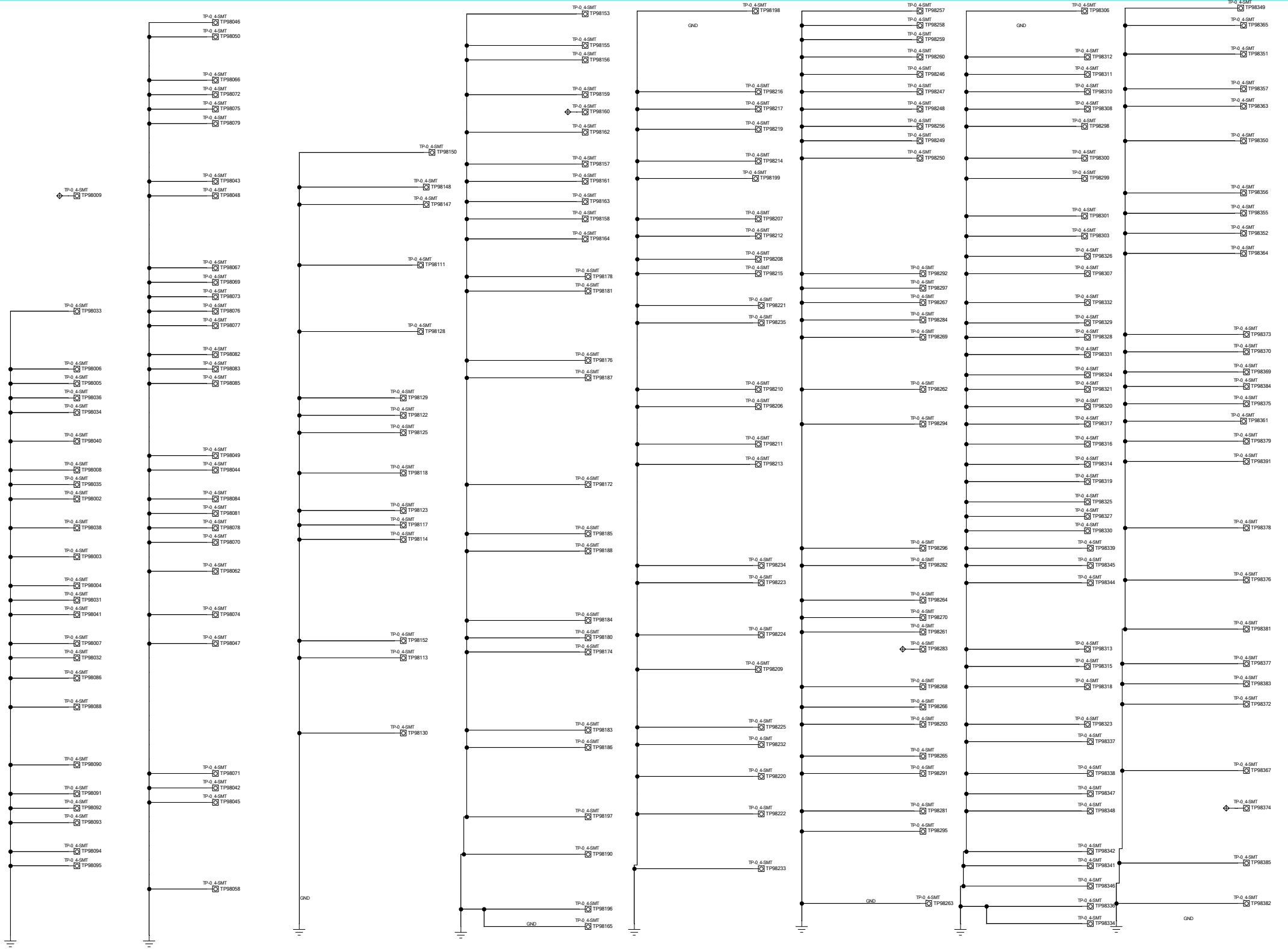


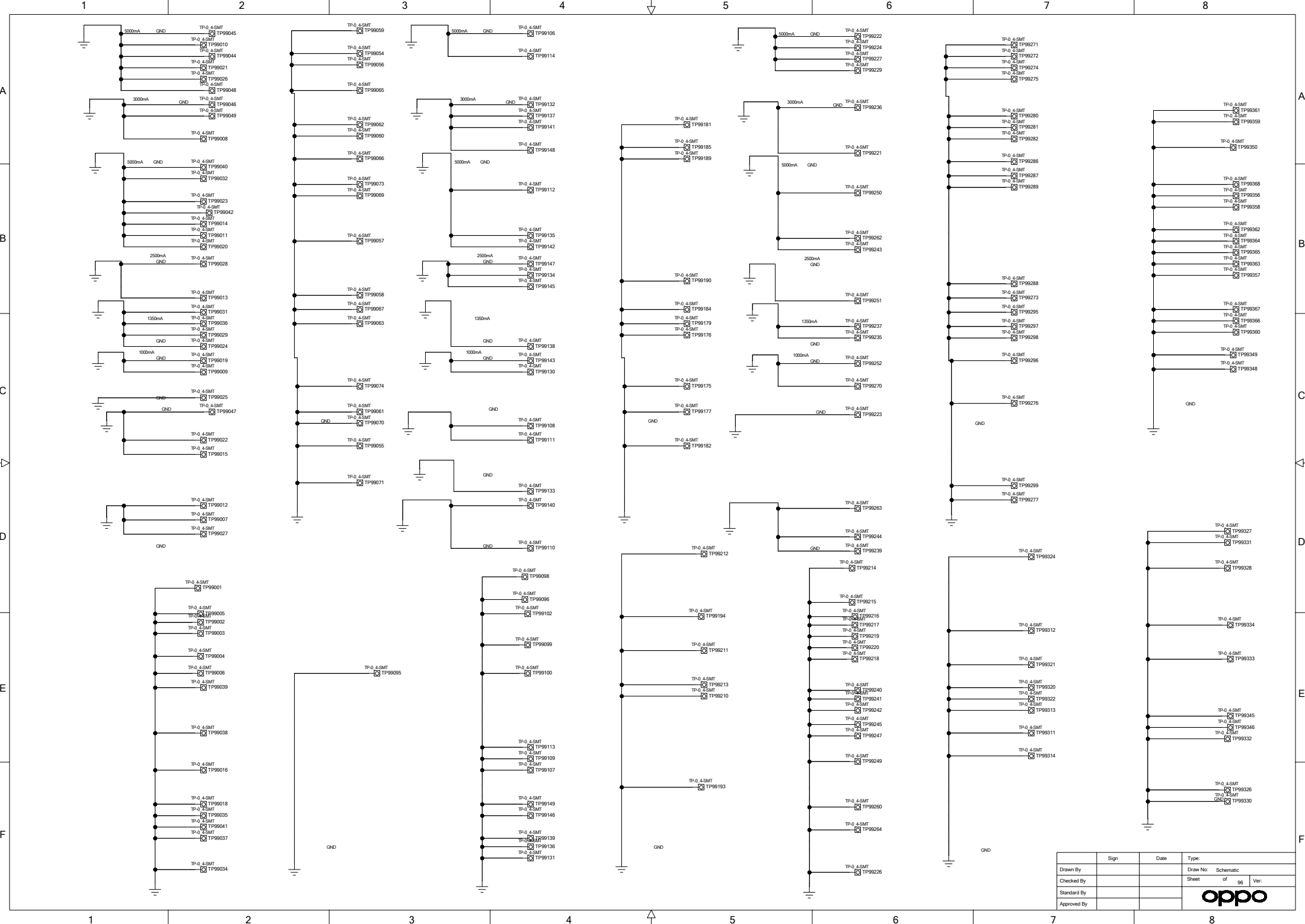
ET Power



NFC







	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By			Sheet of 96 Ver:
Standard By			
Approved By			

