

## PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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base on V372-02S change for D18 Z  
1. P.23 remove SL1 & BRIDGE\_LED\_VDD & SL1\_BRG\_PRST\*  
2. P.52 remove LED change FAN connector  
3. P.53 remove LED  
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0727:

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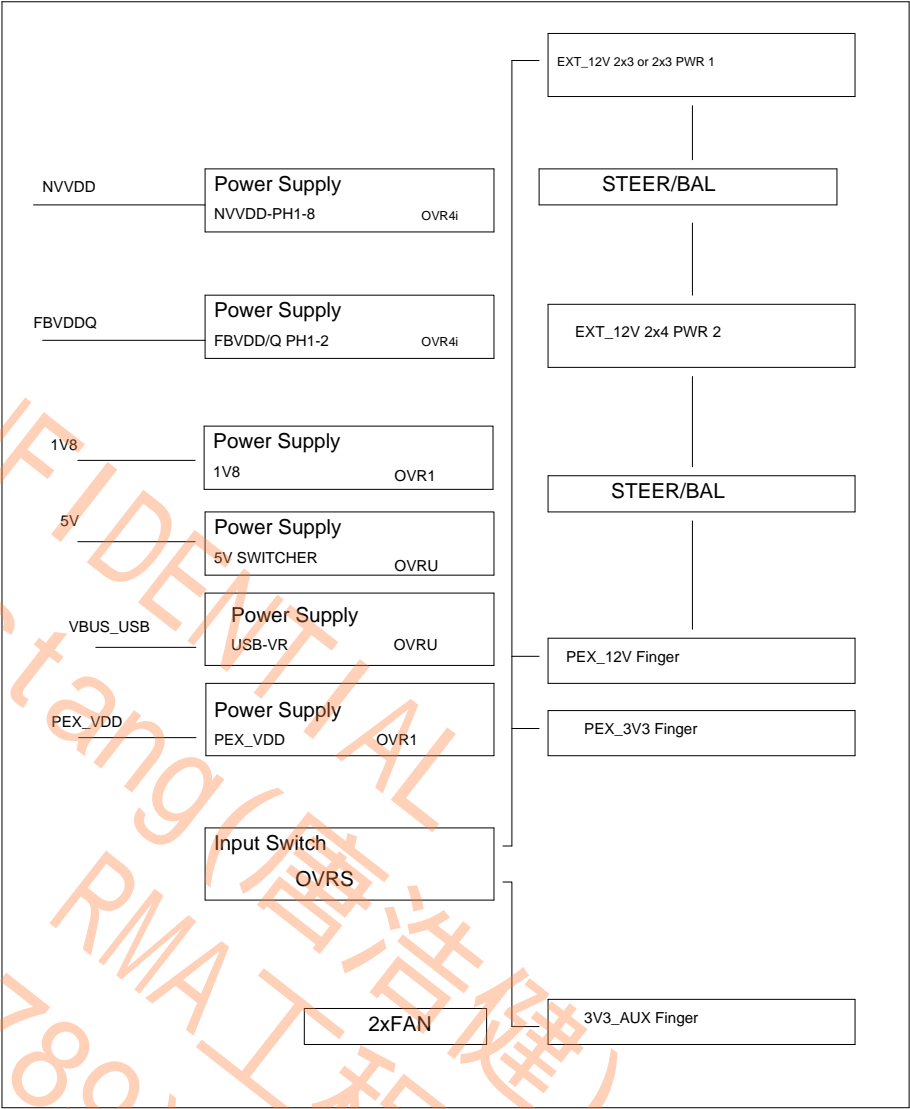
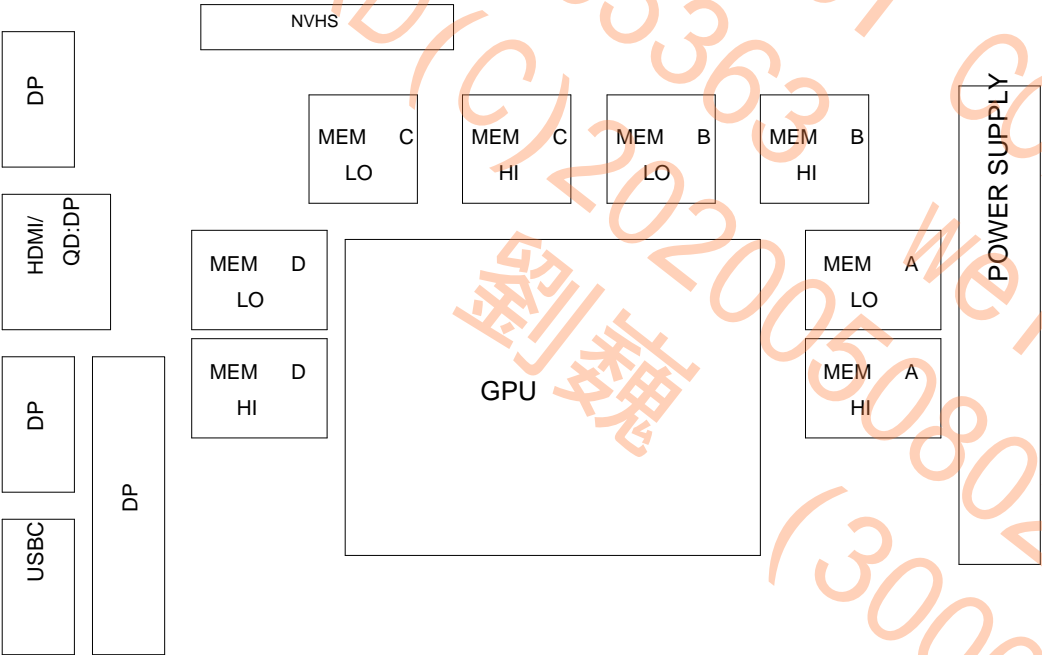
page 54: change GPU screw holes to small size

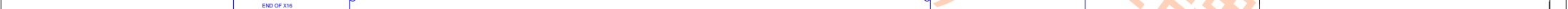


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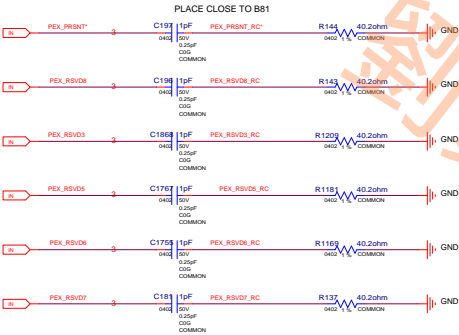
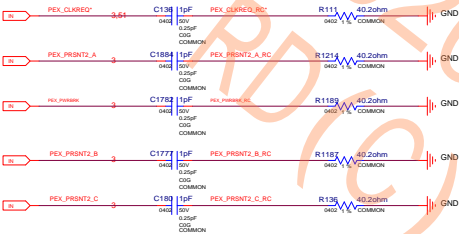
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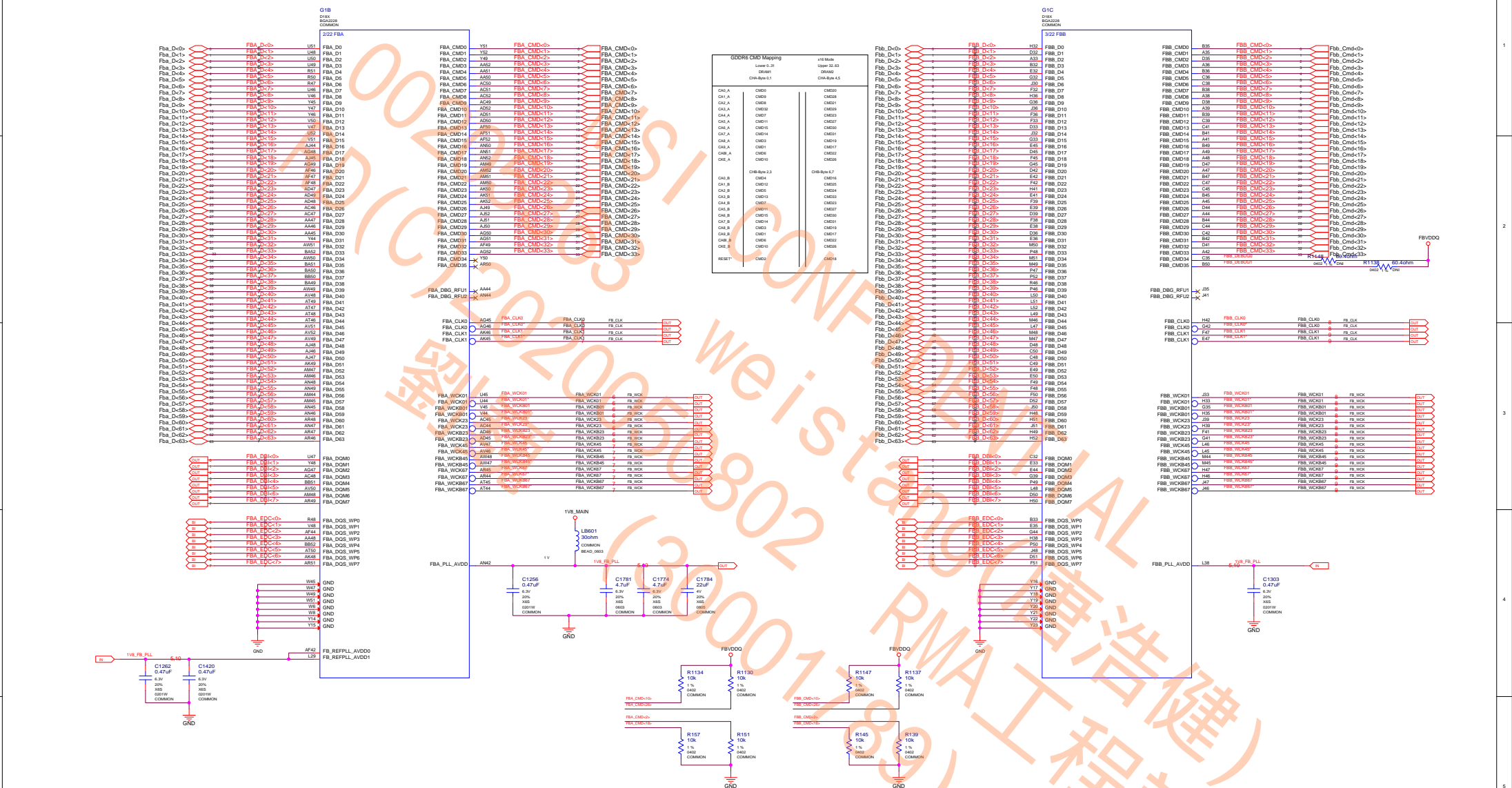
|                                 |                         |     |
|---------------------------------|-------------------------|-----|
| Size                            | Document Description    | Rev |
| Custom                          | Page1:Table of Contents | 7.3 |
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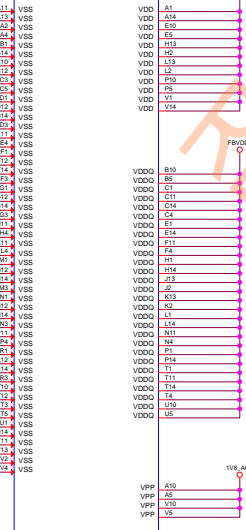


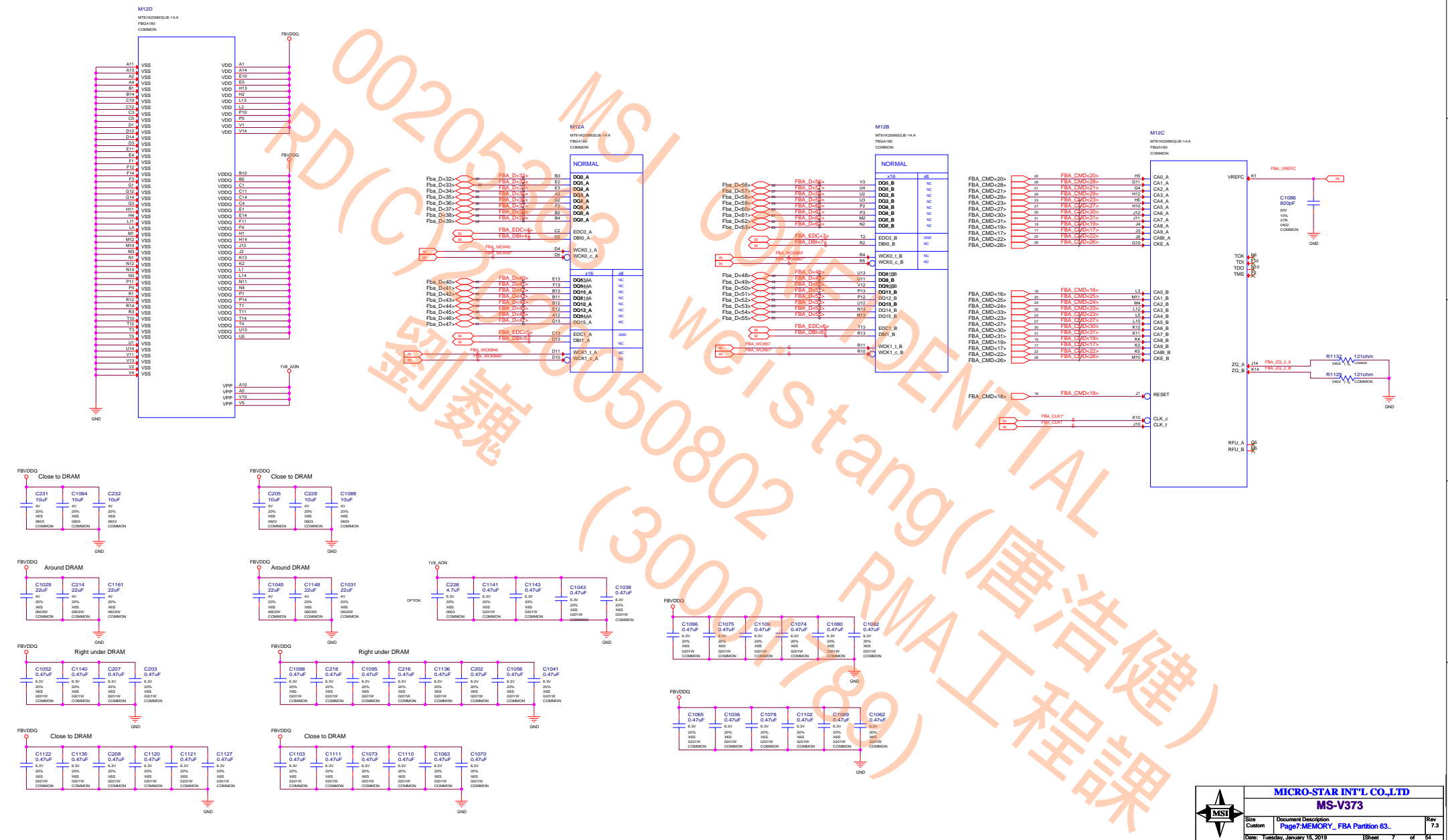


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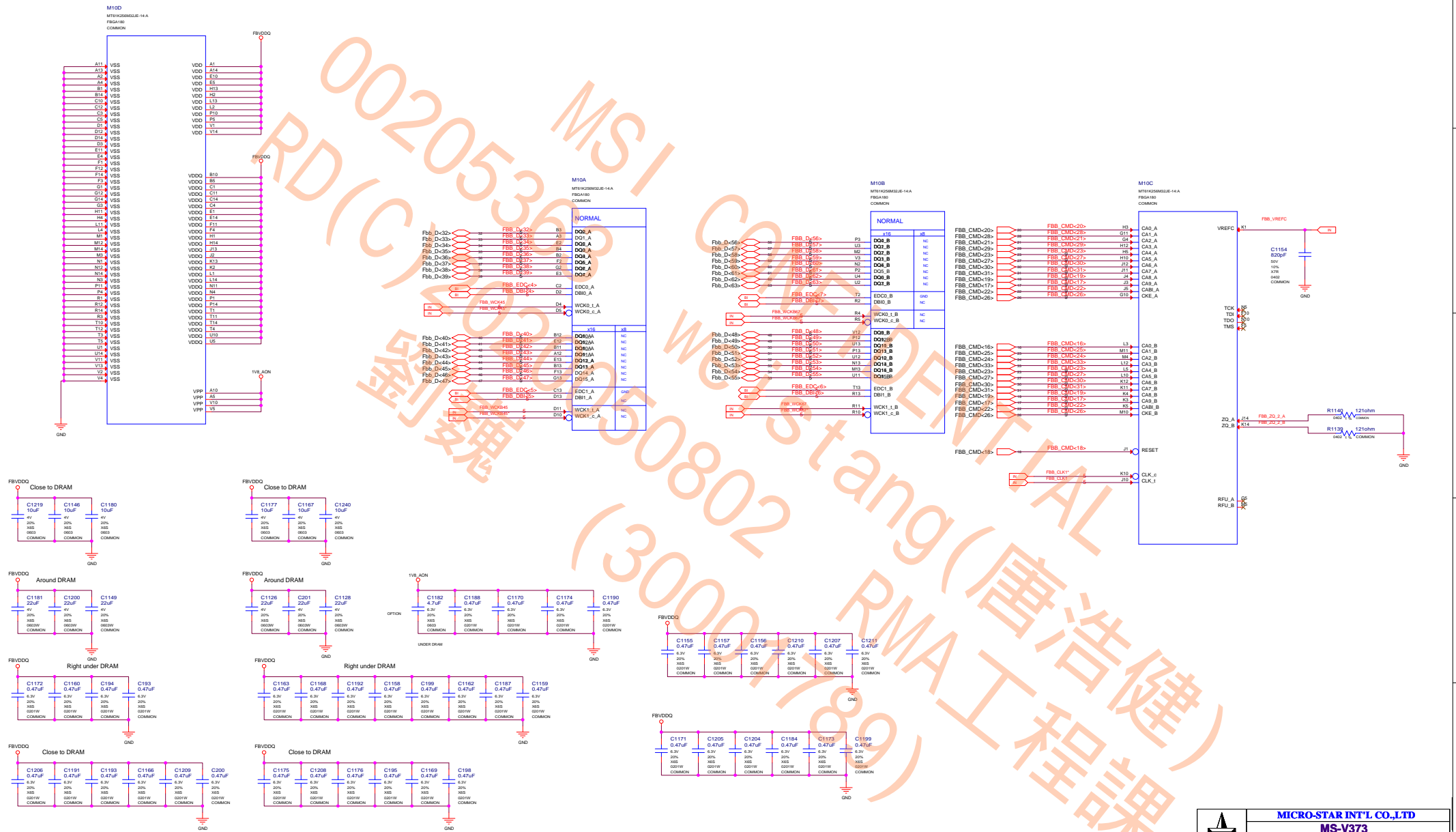
M11D  
MT8128S000UE-14-A  
FPGA(40)  
COMMON

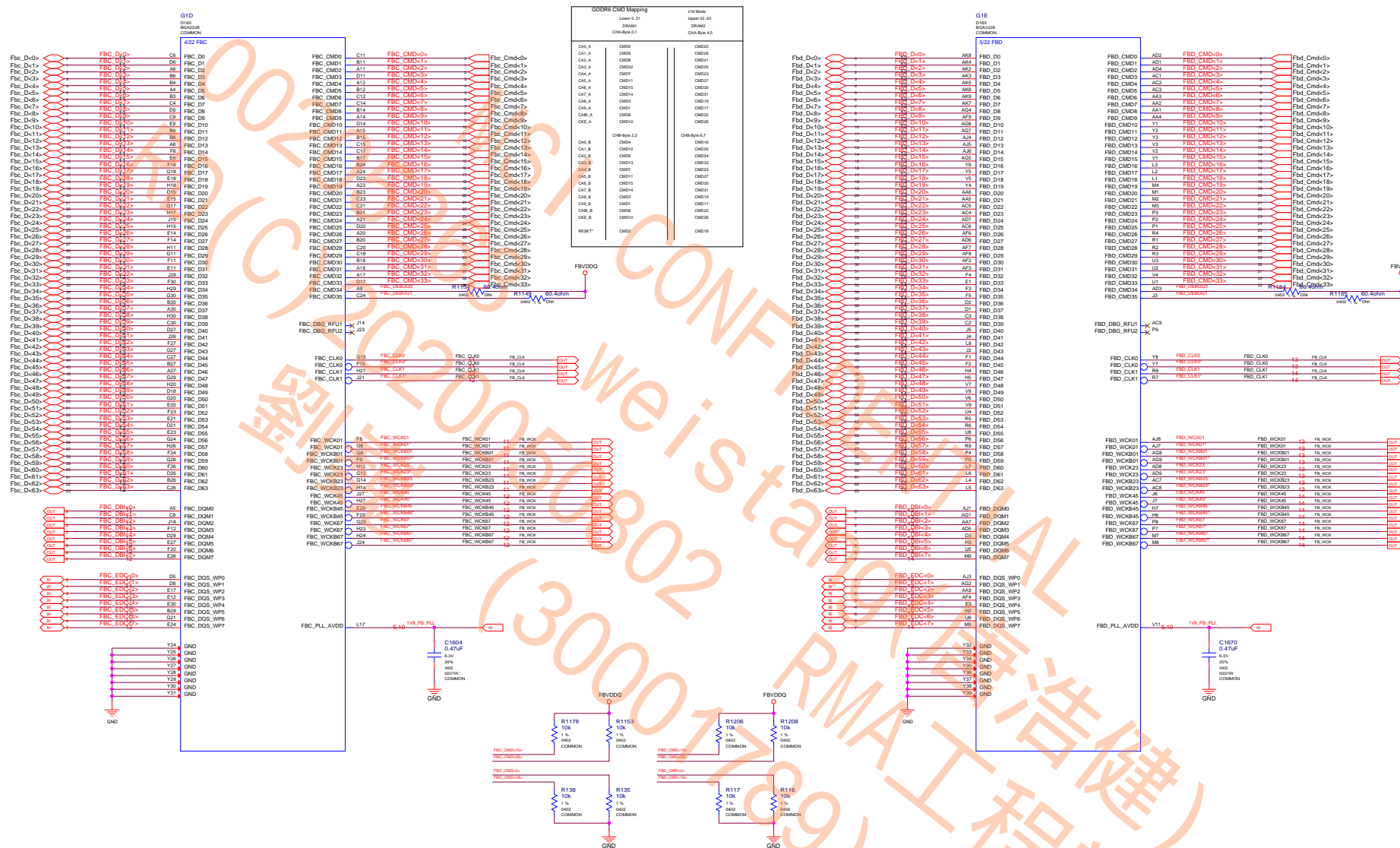




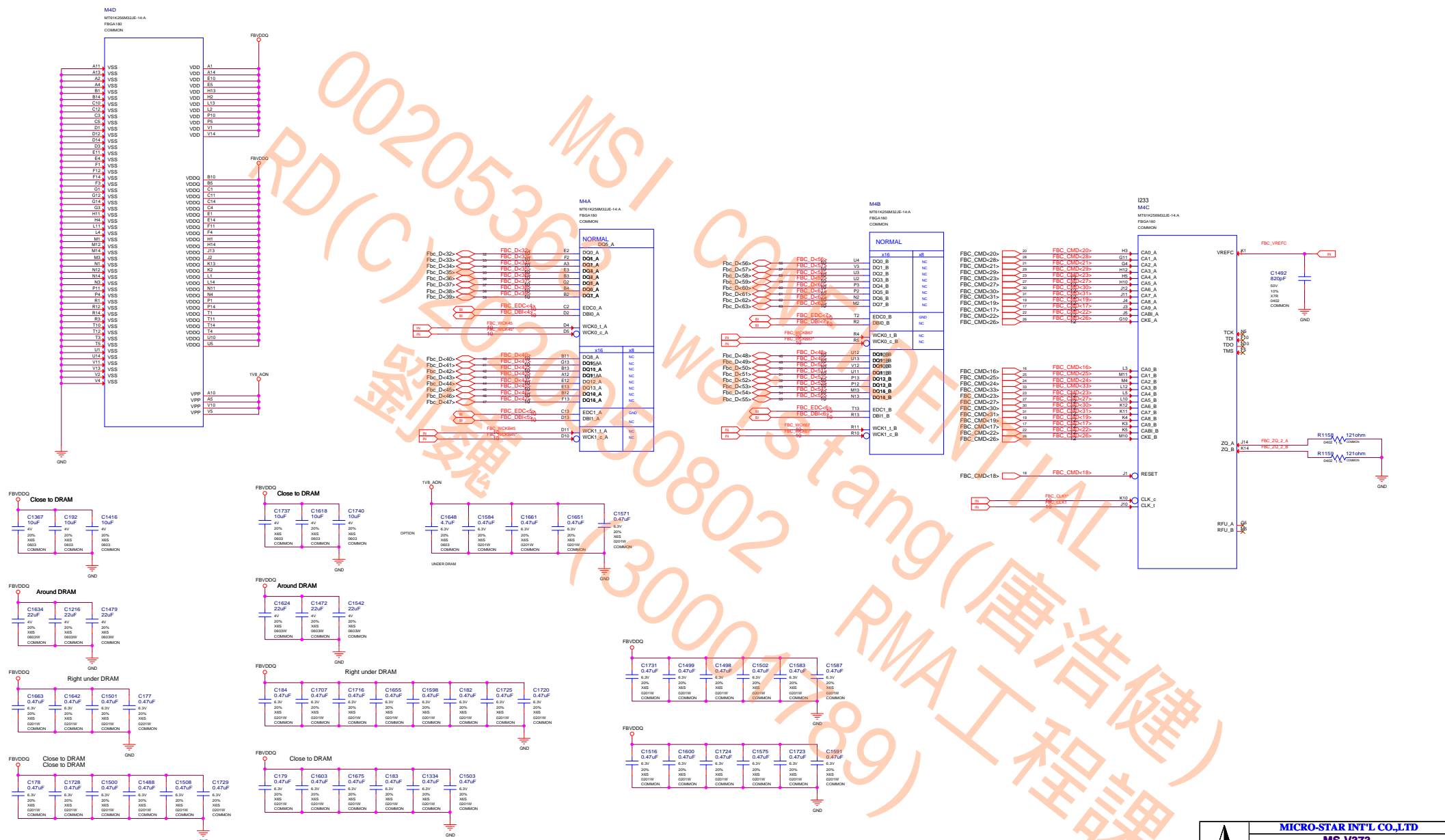




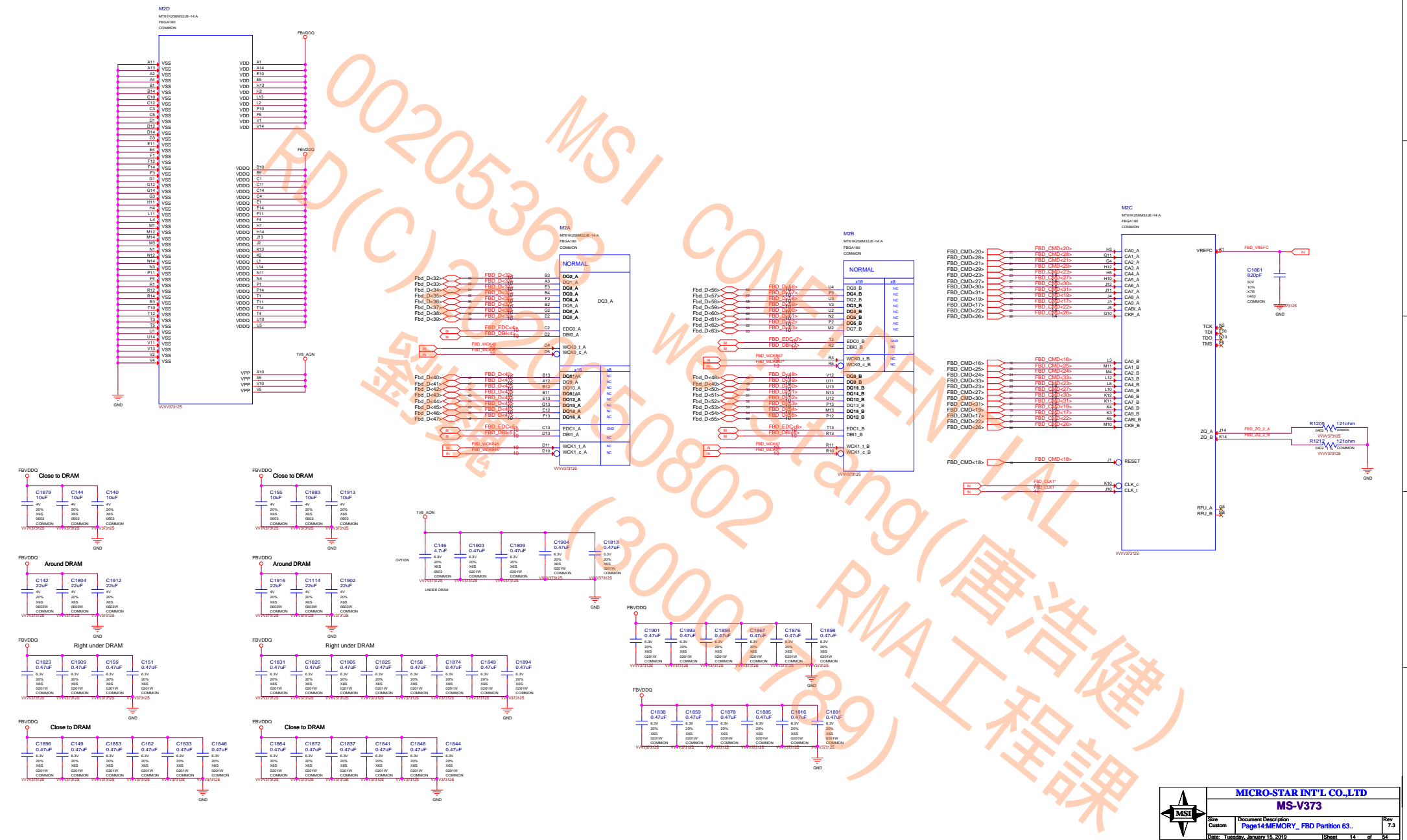




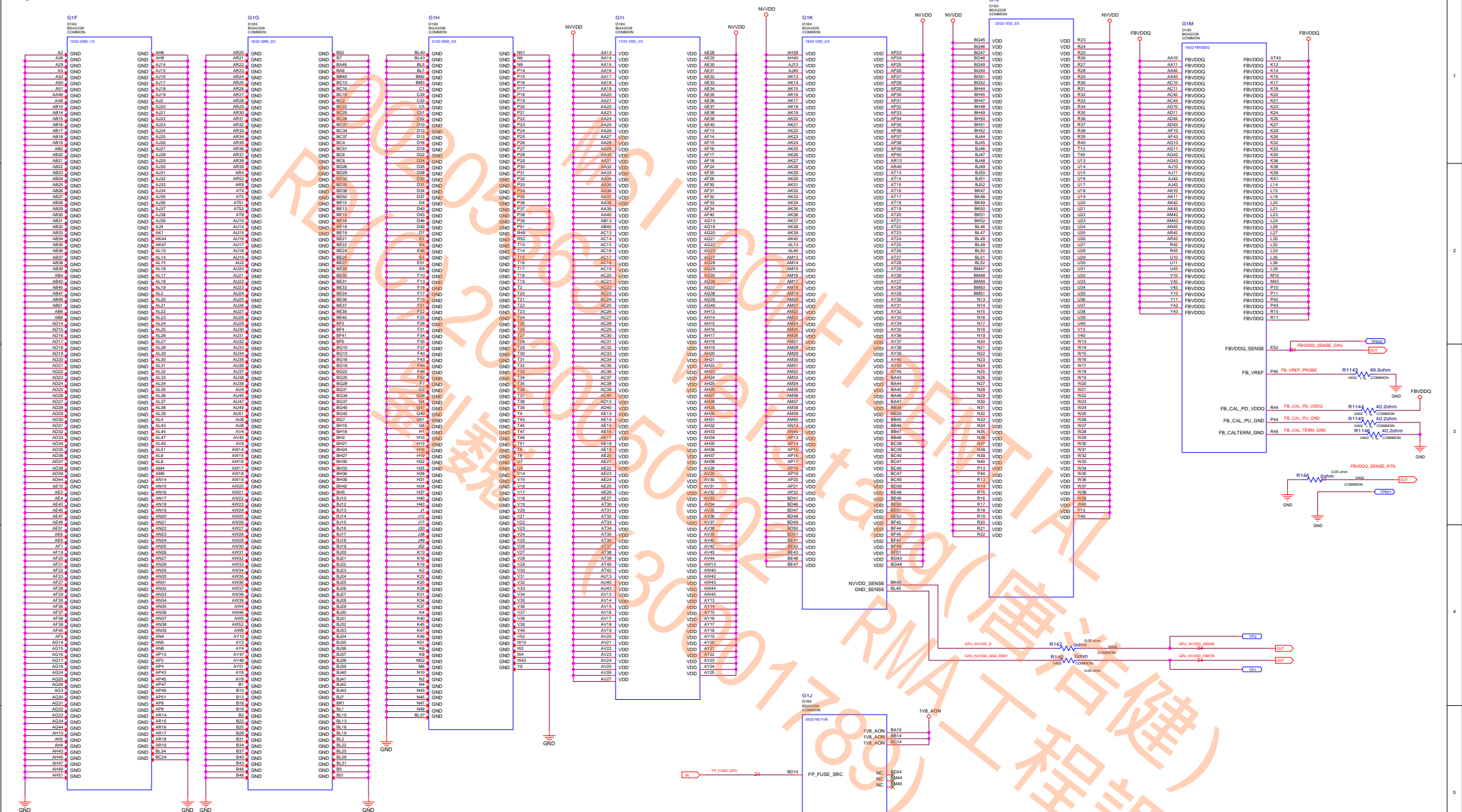










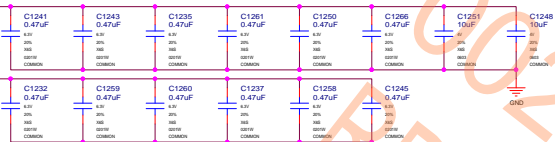




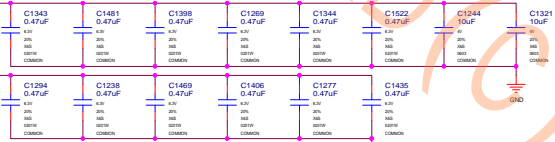
## NVVDD

## FBVDDQ

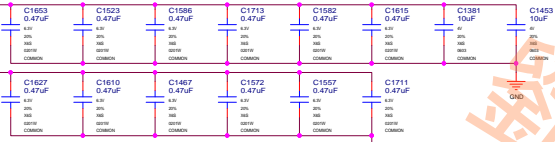
## Partition A



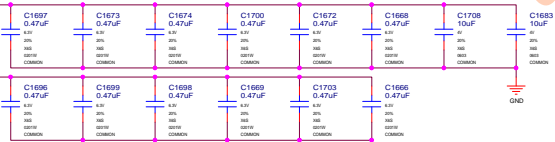
## Partition B



## Partition C



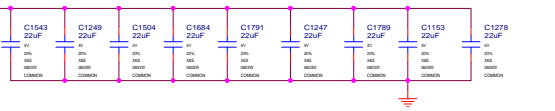
## Partition D



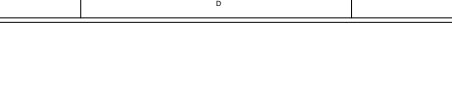
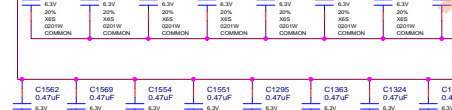
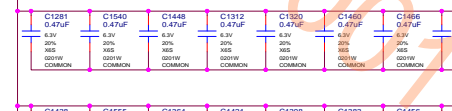
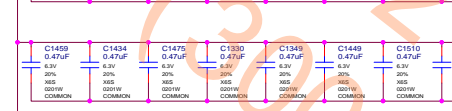
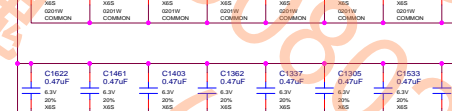
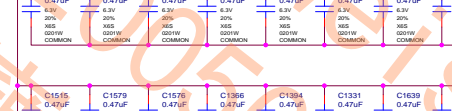
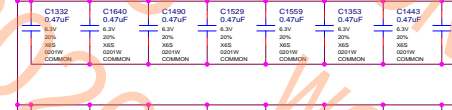
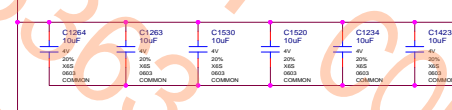
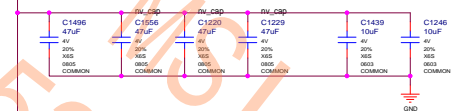
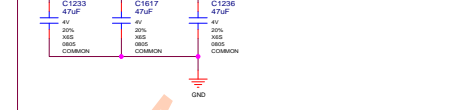
## Place Close to GPU



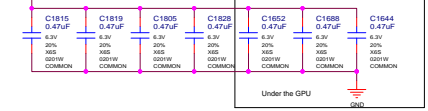
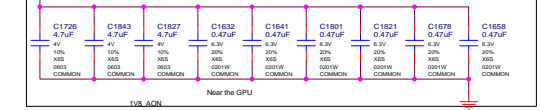
## Place Close to GPU



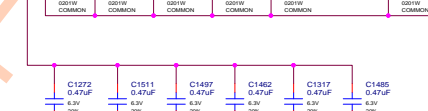
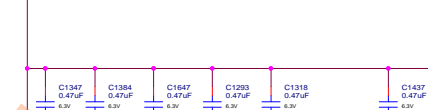
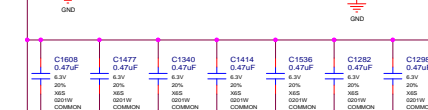
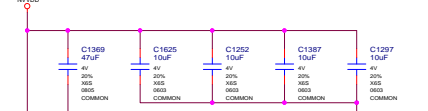
## NVVDD

032-0532-000  
XES  
0805

## 1V8\_AON



## NVVDD

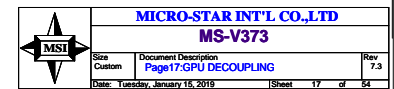
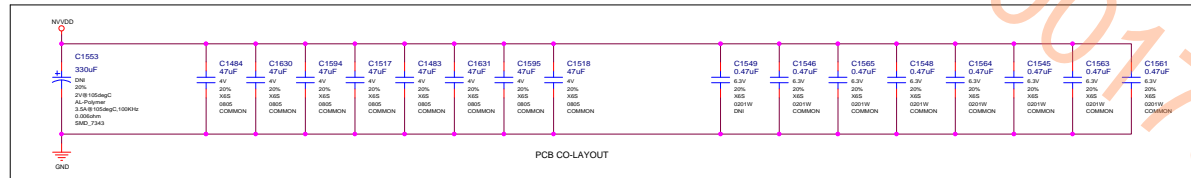
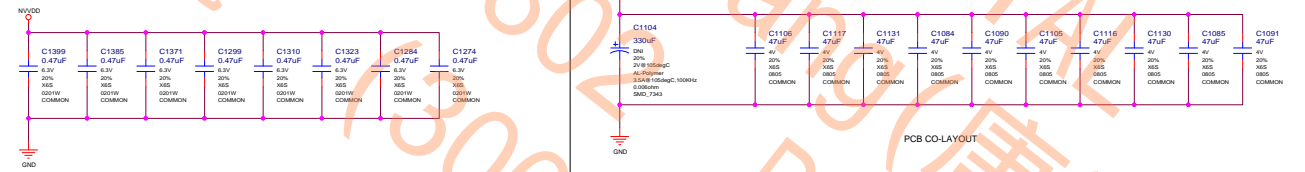
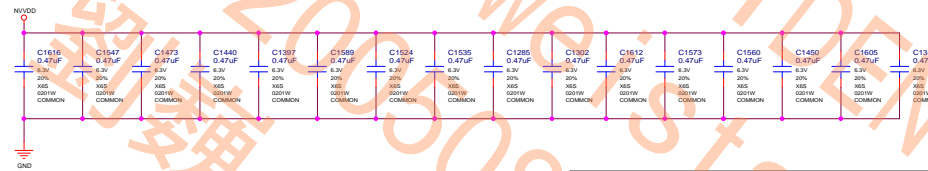
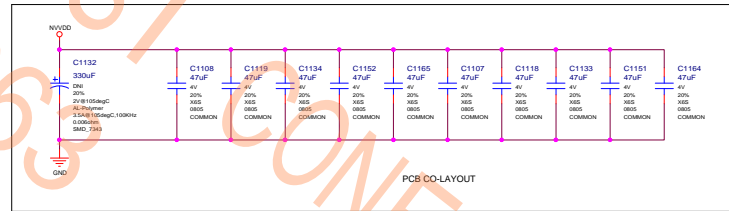
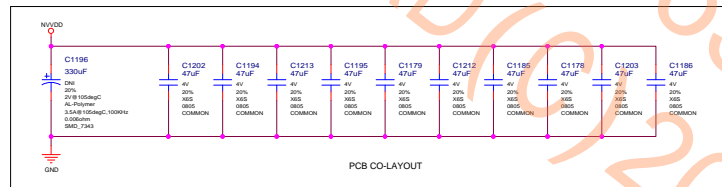
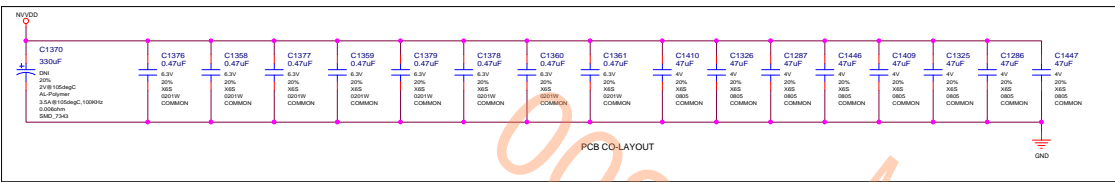


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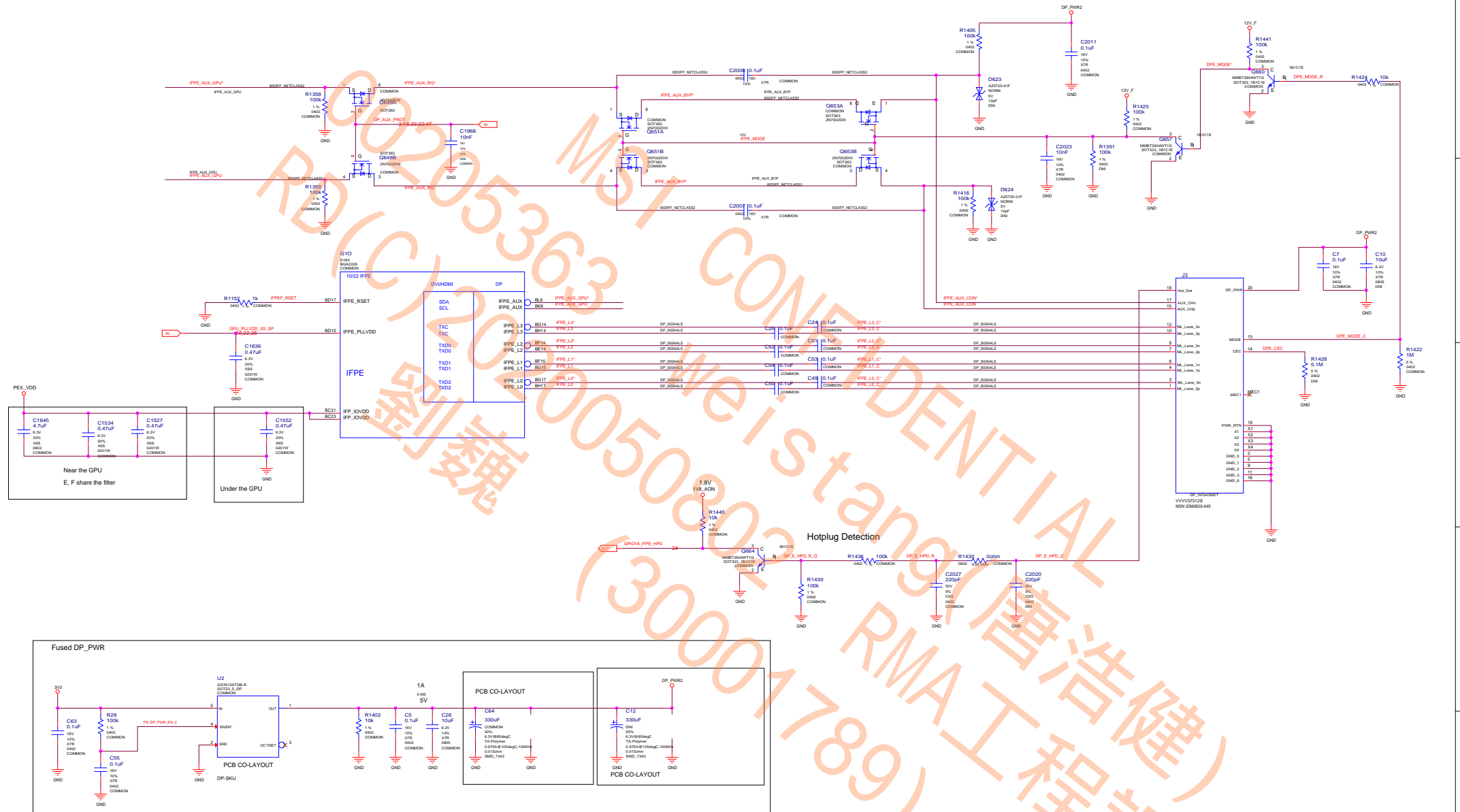
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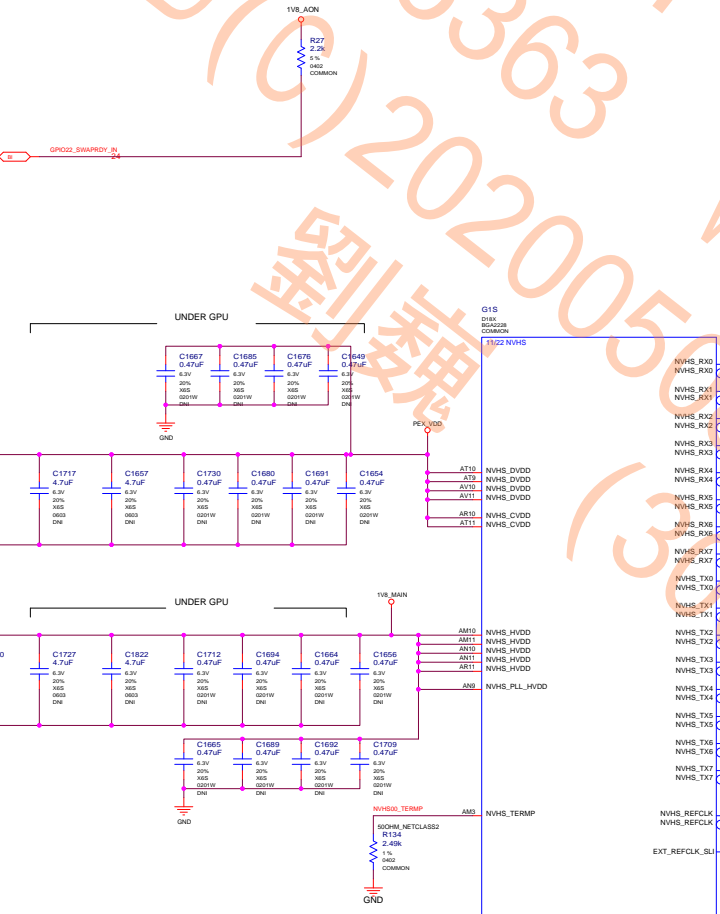














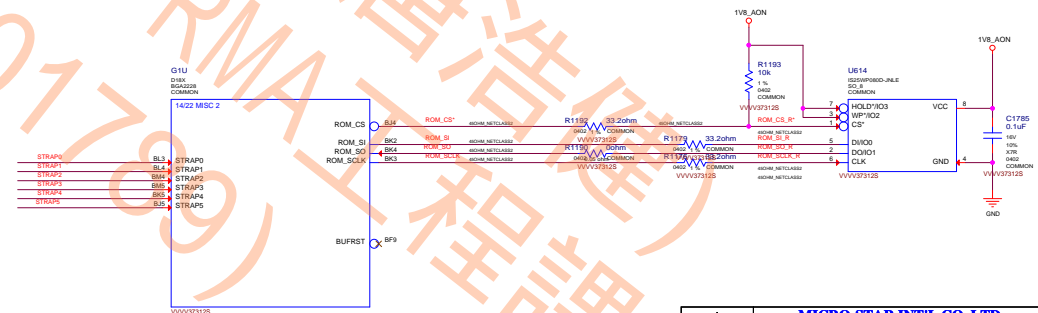
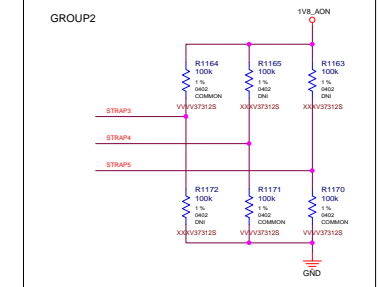
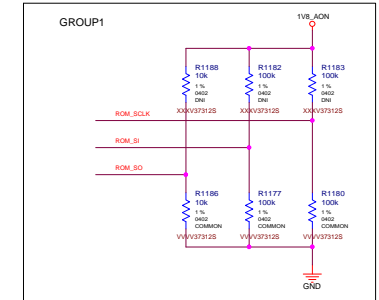
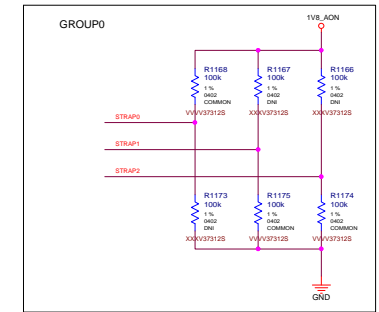
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

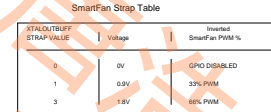
| STRAP2 | STRAP1 | STRAP0 | RAMCFG[4:0] |            |
|--------|--------|--------|-------------|------------|
| L      | L      | L      | 0000        | RAMCFG TBD |
| L      | L      | H      | 0001        | RAMCFG TBD |
| L      | H      | L      | 0010        | RAMCFG TBD |
| L      | H      | H      | 0011        | RAMCFG TBD |
| H      | H      | L      | 0110        | RAMCFG TBD |
| H      | H      | H      | 0111        | RAMCFG TBD |

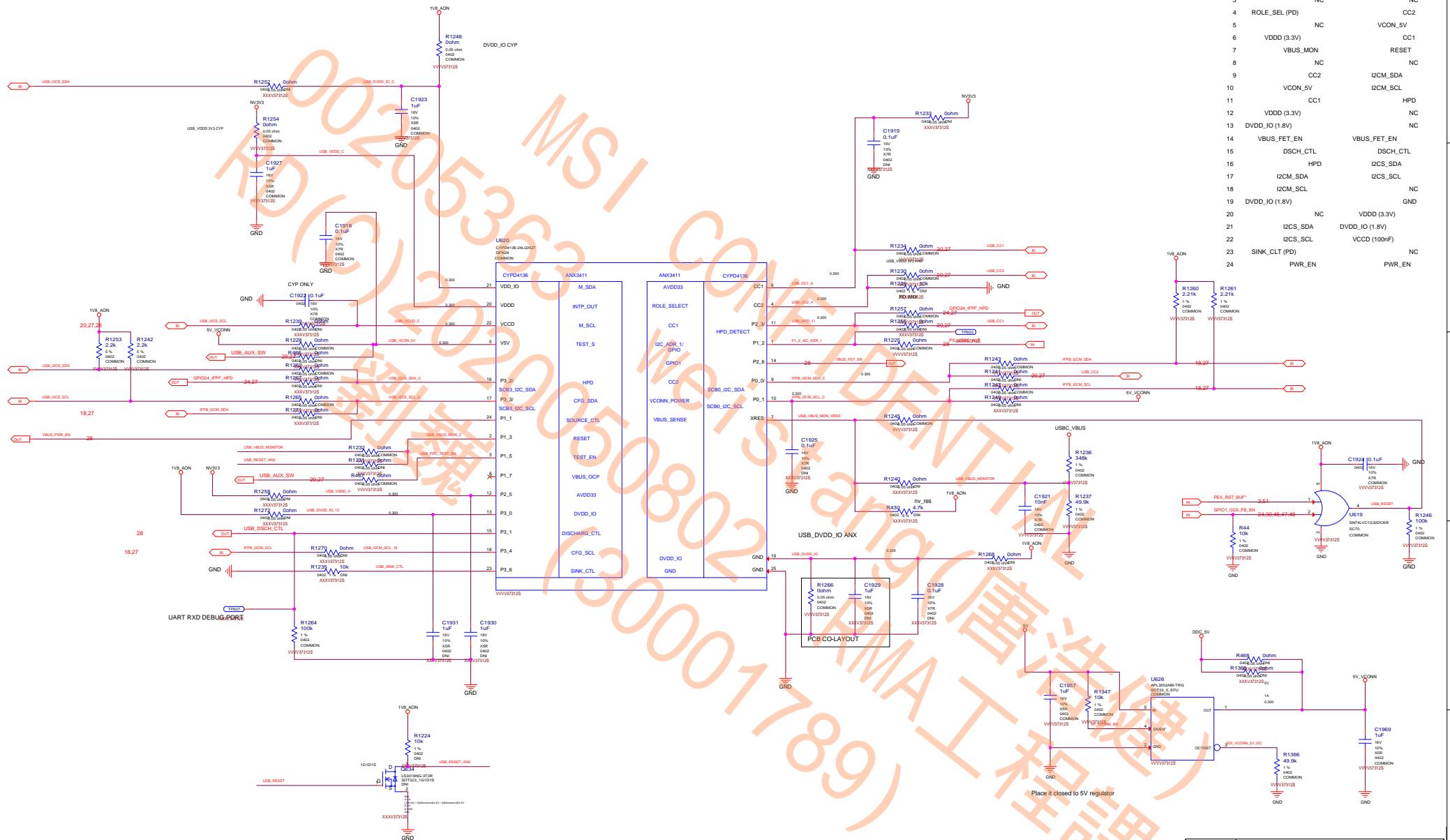
| ROM_SO | ROM_SI | ROM_SCLK | DUMMY[2:0] FS_OVERT | 1:ENABLE 0:DISABLE |         |
|--------|--------|----------|---------------------|--------------------|---------|
| L      | L      | L        | XXX1                | FS_OVERT ENABLE    | DEFAULT |
| L      | L      | M        | XXX0                | FS_OVERT DISABLE   |         |

| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |                        |
|--------|--------|--------|--------------|-----------|----------|------------|------------------------|
| M      | H      | H      | 1            | 1         | 1        | 1          |                        |
| M      | H      | L      | 1            | 1         | 1        | 0          | 1:SMB_ALT_ADDR ENABLE  |
| M      | L      | H      | 1            | 1         | 0        | 1          | 0:SMB_ALT_ADDR DISABLE |
| M      | L      | L      | 1            | 1         | 0        | 0          | 1:DEVID_SEL REBRAND    |
| L      | H      | M      | 1            | 0         | 1        | 1          | 0:DEVID_SEL ORIGINAL   |
| L      | M      | H      | 1            | 0         | 1        | 0          | 1:PCIE_CFG LOW POWER   |
| L      | M      | L      | 1            | 0         | 0        | 1          | 0:PCIE_CFG HIGH POWER  |
| L      | L      | M      | 1            | 0         | 0        | 0          | 1:VGA_DEVICE ENABLE    |
| H      | H      | H      | 0            | 1         | 1        | 1          | 0:VGA_DEVICE DISABLE   |
| H      | H      | L      | 0            | 1         | 1        | 0          |                        |
| H      | L      | H      | 0            | 1         | 0        | 1          |                        |
| H      | L      | L      | 0            | 1         | 0        | 0          |                        |
| L      | H      | H      | 0            | 0         | 1        | 1          |                        |
| L      | H      | L      | 0            | 0         | 1        | 0          |                        |
| L      | L      | H      | 0            | 0         | 0        | 1          | Default                |
| L      | L      | L      | 0            | 0         | 0        | 0          |                        |

| RAMCFG[4:0] | DENSITY | WIDTH   | VENDOR  |
|-------------|---------|---------|---------|
| 00000       | 8Gb     | 256-bit | Samsung |
| 00001       | 8Gb     | 256-bit | Micron  |
| 00010       | 8Gb     | 256-bit | Hynix   |
|             |         |         |         |
| 00110       | 16Gb    | 256-bit | Samsung |
| 00111       | 16Gb    | 256-bit | Samsung |
|             |         |         |         |

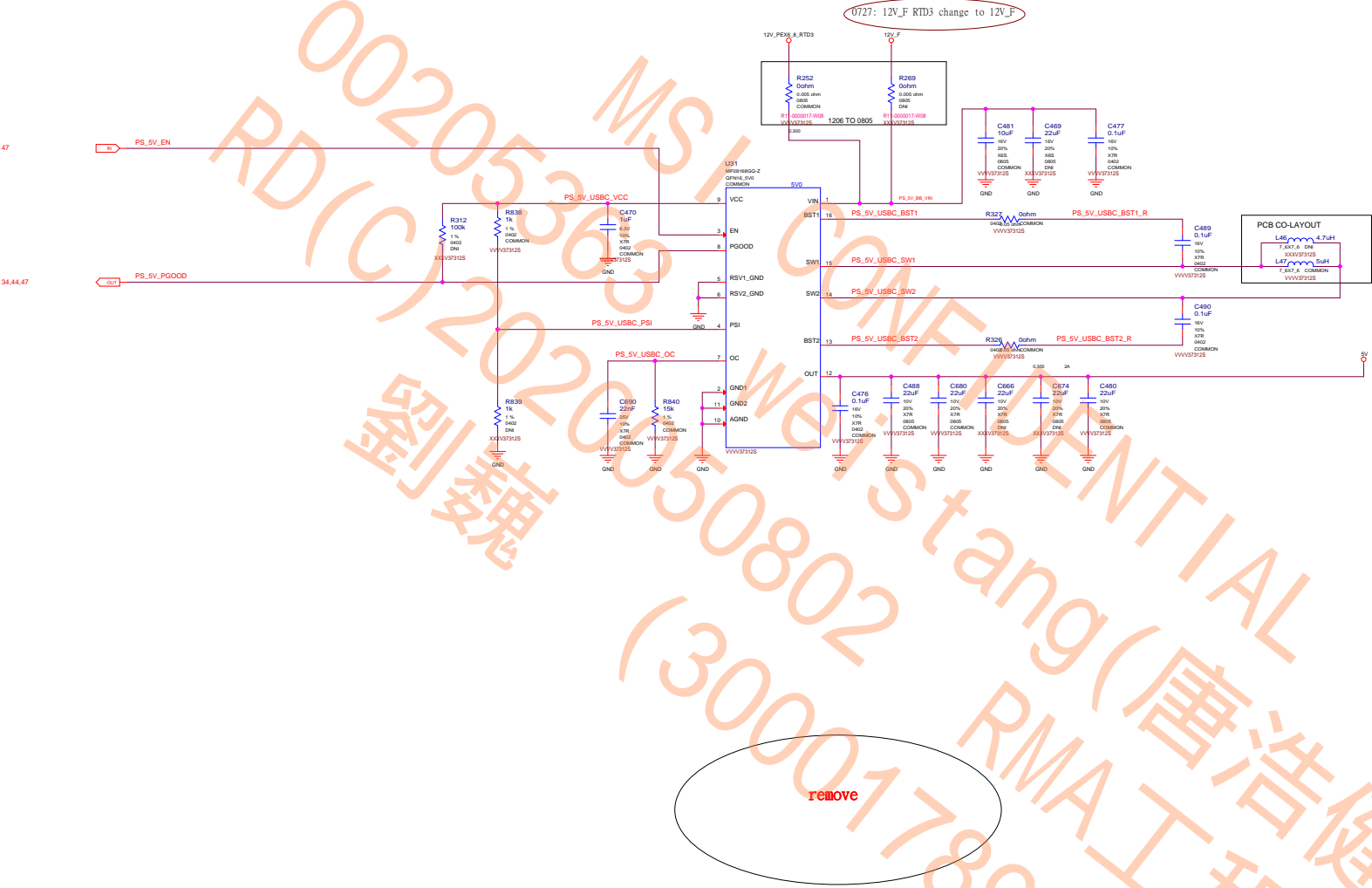




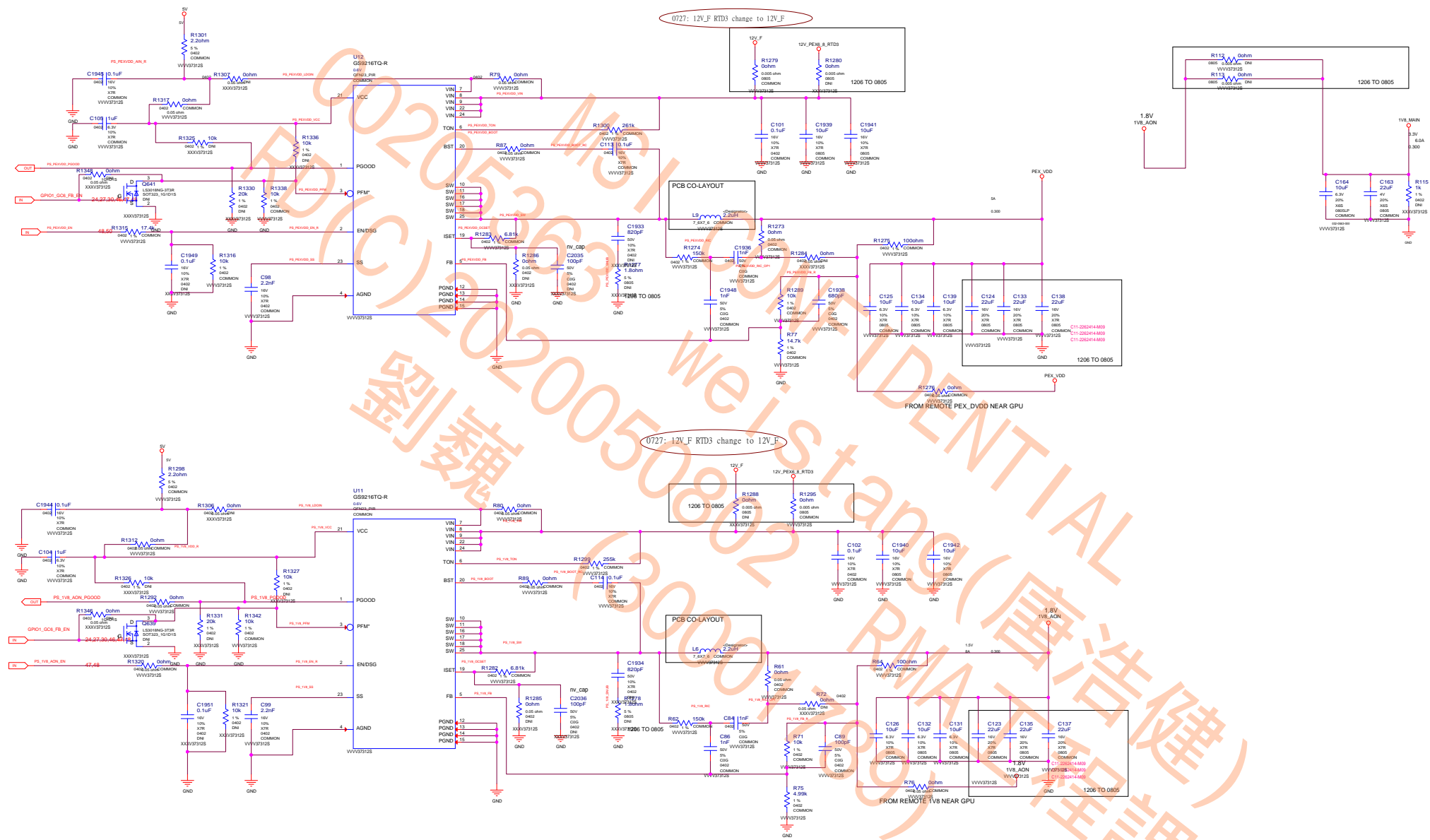


| PIN | ANX            | CYP            |
|-----|----------------|----------------|
| 1   | TP             |                |
| 2   | RESET          | VBUS_MON       |
| 3   | NC             | NC             |
| 4   | ROLE_SEL (PD)  | CC2            |
| 5   | NC             | VCON_5V        |
| 6   | VDDD (3.3V)    | CC1            |
| 7   | VBUS_MON       | RESET          |
| 8   | NC             | NC             |
| 9   | CC2            | I2CM_SDA       |
| 10  | VCON_5V        | I2CM_SCL       |
| 11  | CC1            | HPD            |
| 12  | VDDD (3.3V)    | NC             |
| 13  | DVDD_IO (1.8V) | NC             |
| 14  | VBUS_FET_EN    | VBUS_FET_EN    |
| 15  | DSCH_CTL       | DSCH_CTL       |
| 16  | HPD            | I2CS_SDA       |
| 17  | I2CM_SDA       | I2CS_SCL       |
| 18  | I2CM_SCL       | NC             |
| 19  | DVDD_IO (1.8V) | GND            |
| 20  | NC             | VDDD (3.3V)    |
| 21  | I2CS_SDA       | DVDD_IO (1.8V) |
| 22  | I2CS_SCL       | VCCD (100kF)   |
| 23  | SINK_CLT (PD)  | NC             |
| 24  | PWR_EN         | PWR_EN         |









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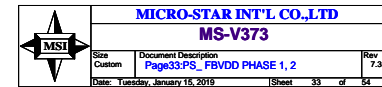
MS-V373

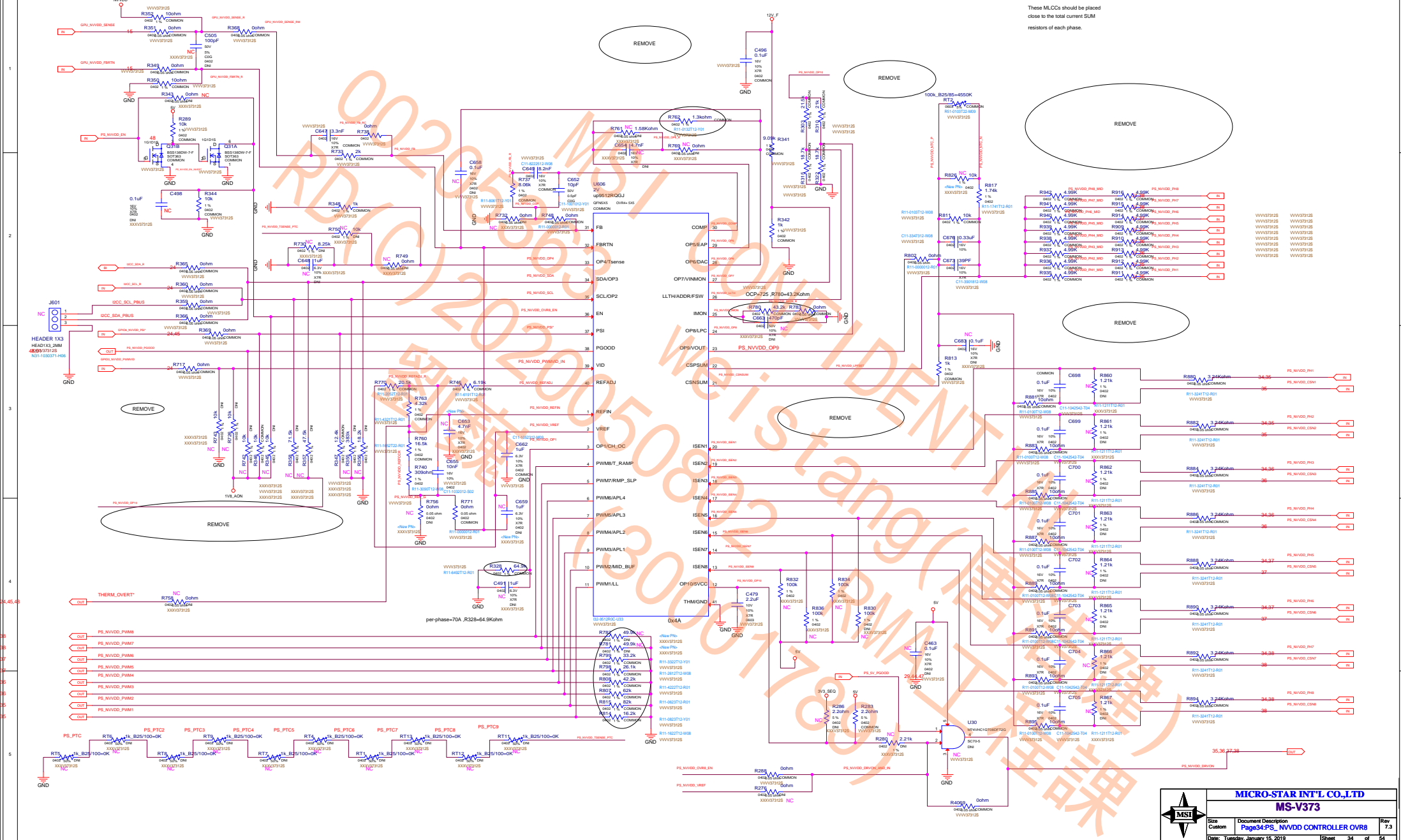
|                |   |            |
|----------------|---|------------|
| Size<br>Custom | Document Description<br>Page30:PS_PEXVDD, 1V8 | Rev<br>7.3 |
|----------------|---|------------|

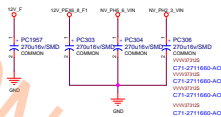


MSI CONFIDENTIAL  
00205363  
RD(C)2020050802  
劉魏  
weistang (唐浩健)  
(30001789)  
RMA工程課

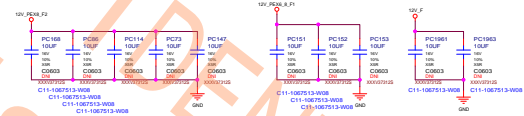
|                                 |                                |                |
|---------------------------------|--------------------------------|----------------|
| MICRO-STAR INT'L CO.,LTD        |                                |                |
| MS-V373                         |                                |                |
| Size                            | Document Description           | Rev            |
| Custom                          | Page32:PS_FBVD Controller OVR3 | 7.3            |
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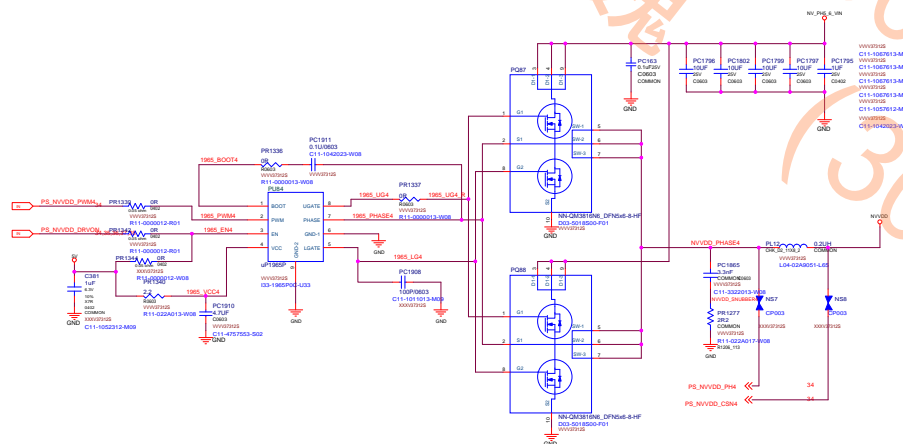
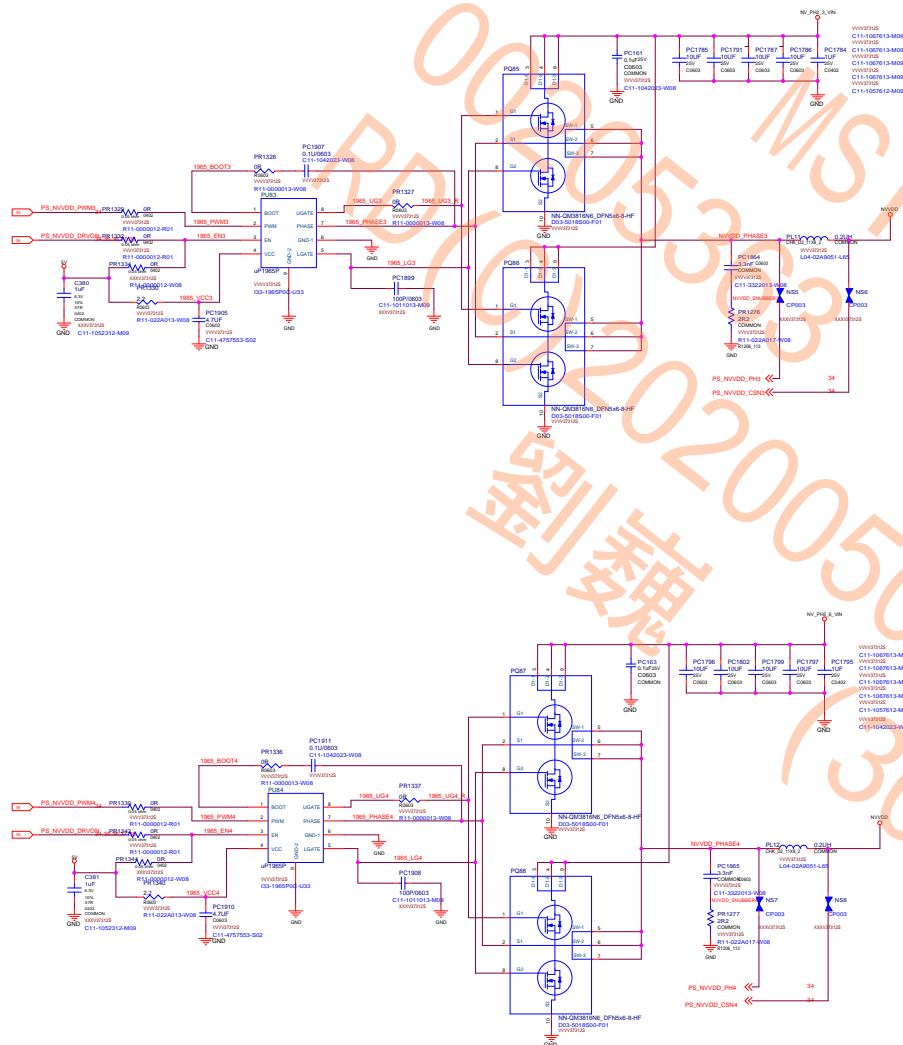




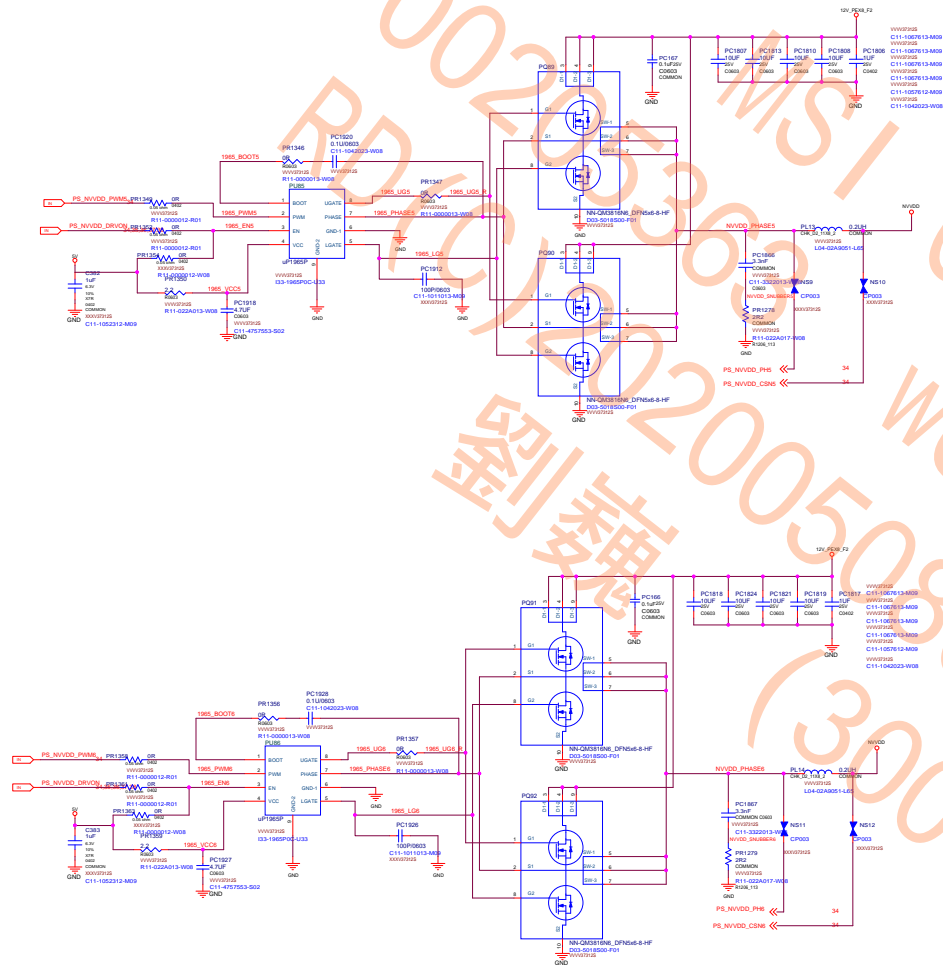


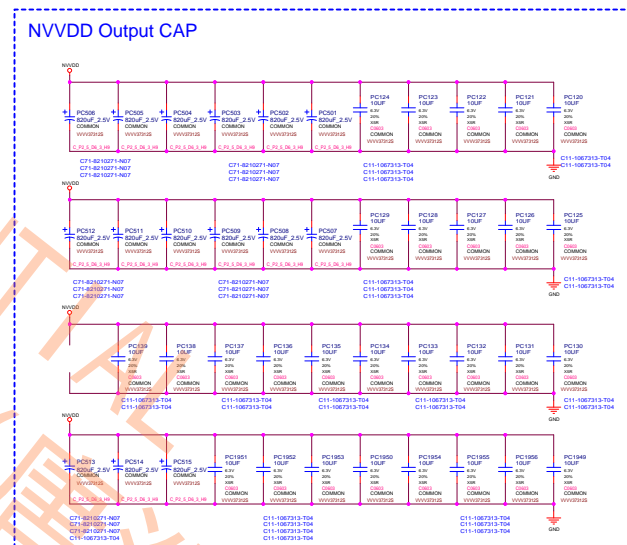
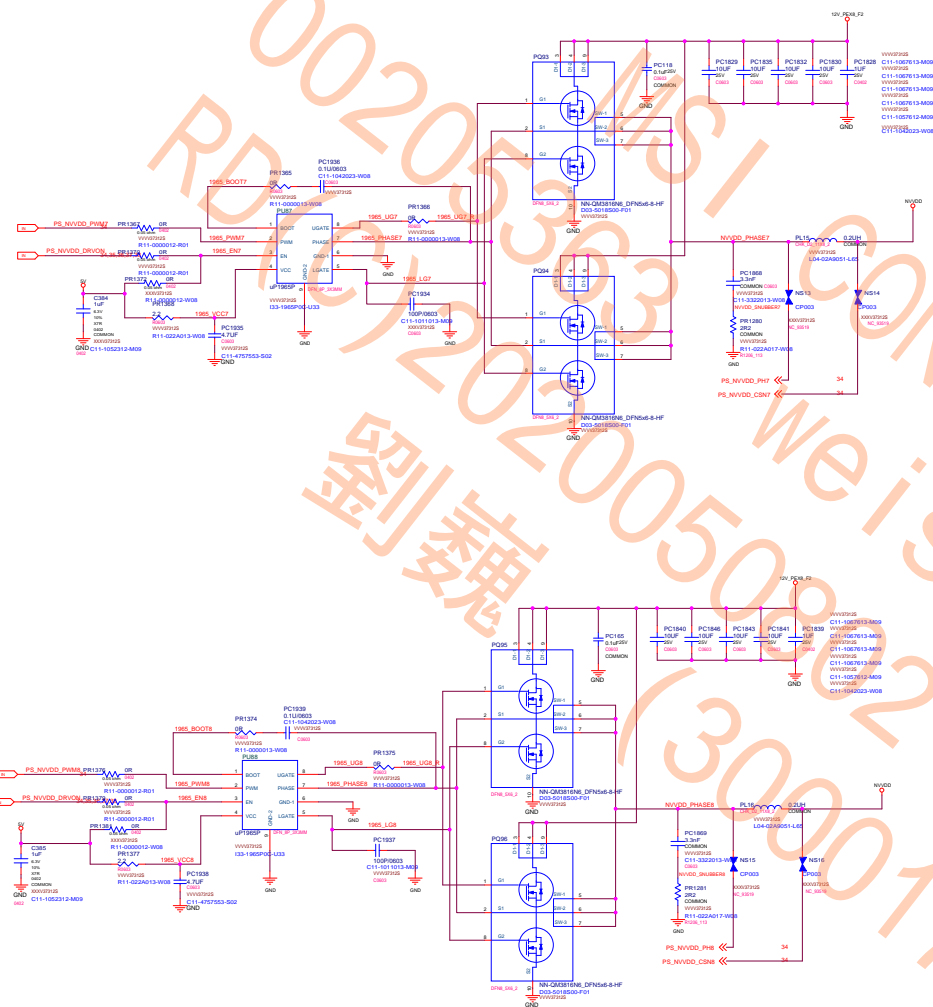
## Backup







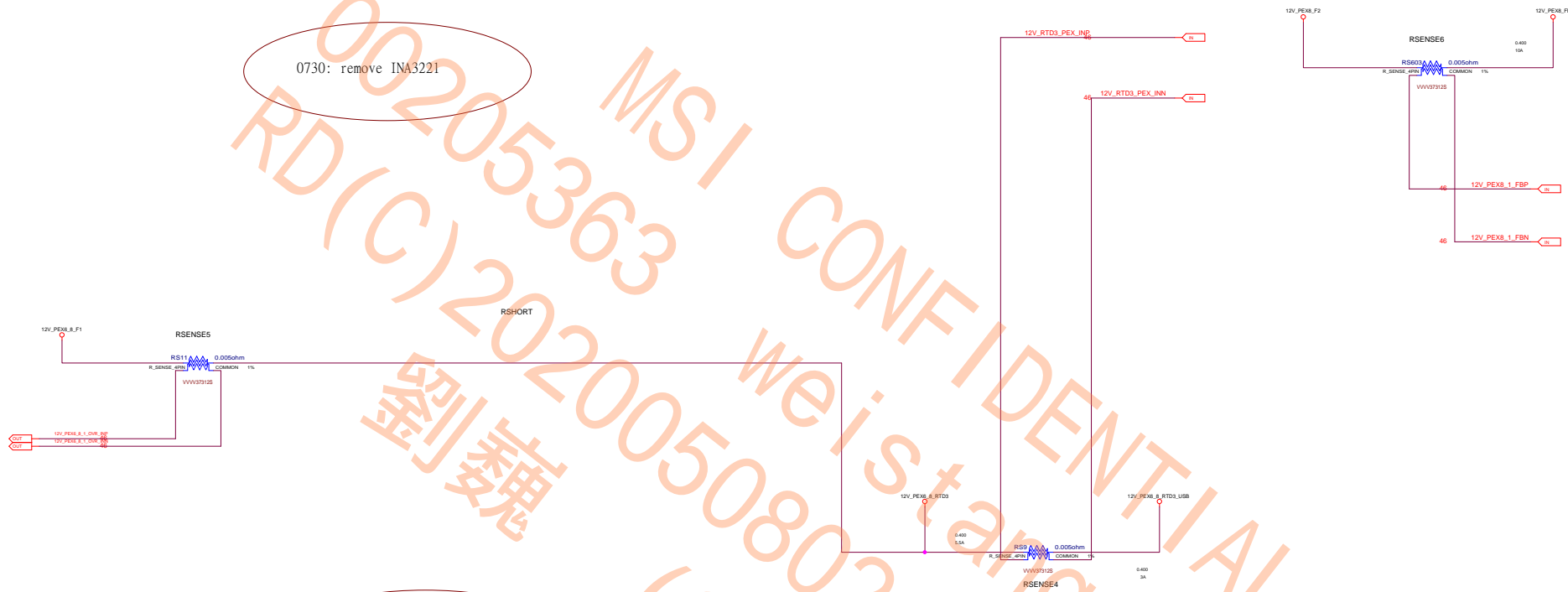


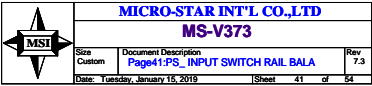


| AND GATE LOGIC FOR P-BOARD |        |        |       |
|----------------------------|--------|--------|-------|
| GPIO1                      | GPIO29 | SWITCH | VOUT  |
| 0                          | 0      | 0      | 12V_F |
| 0                          | 1      | 0      | 12V_F |
| 1                          | 0      | 0      | 12V_F |
| 1                          | 1      | 1      | 3V3A  |

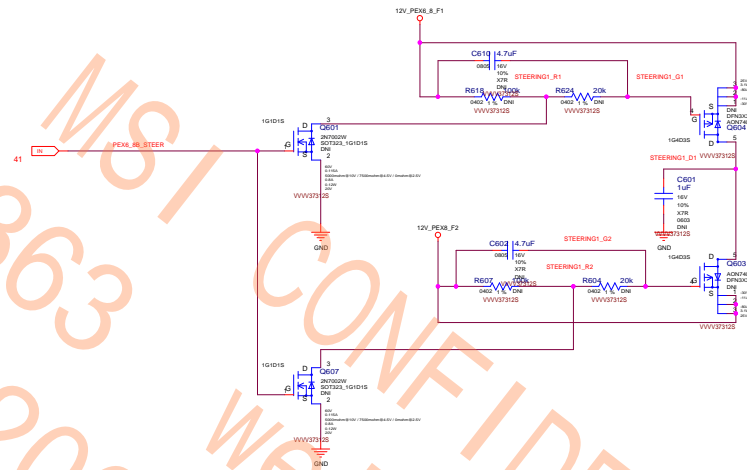
| AND GATE LOGIC FOR P-BOARD |        |        |      |
|----------------------------|--------|--------|------|
| GPIO1                      | GPIO29 | SWITCH | VOUT |
| 0                          | 0      | 0      | 3V3  |
| 0                          | 1      | 0      | 3V3  |
| 1                          | 0      | 0      | 3V3  |
| 1                          | 1      | 1      | 3V3A |

0727: remove

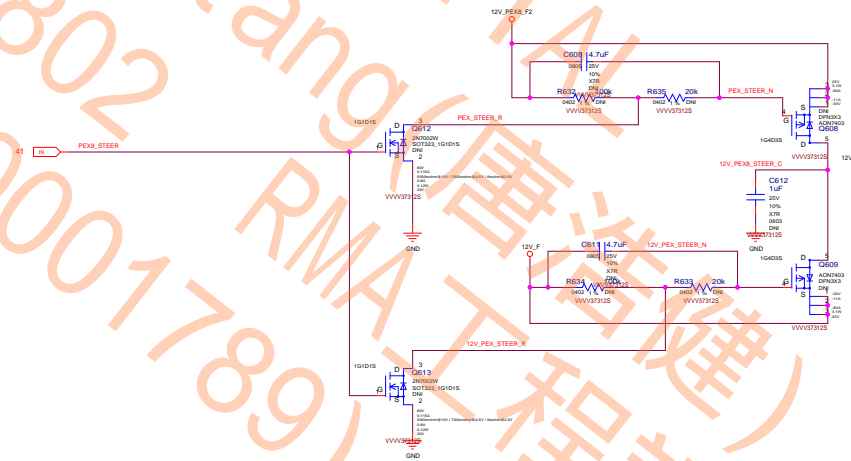




12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



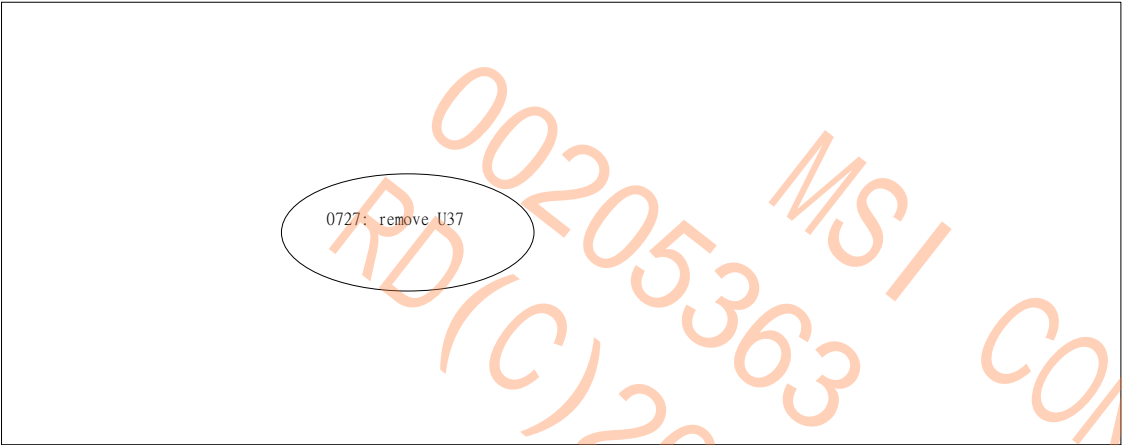
12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



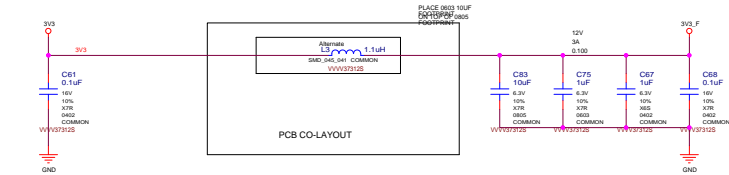
|                                 |  |                |            |
|---------------------------------|--|----------------|------------|
| MICRO-STAR INT'L CO.,LTD        |  |                |            |
| MS-V373                         |  |                |            |
| Size<br>Custom                  | Document Description<br>Page42:PS_12V CURRENT STEERING |                | Rev<br>7.3 |
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weistang(唐浩健)  
(30001789)  
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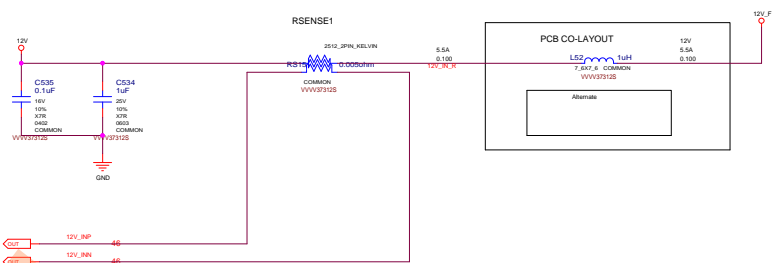
|                                 |                                 |                |
|---------------------------------|---------------------------------|----------------|
| MICRO-STAR INT'L CO.,LTD        |                                 |                |
| MS-V373                         |                                 |                |
| Size                            | Document Description            | Rev            |
| Custom                          | Page43.PS_VR THERMAL PROTECTION | 7.3            |
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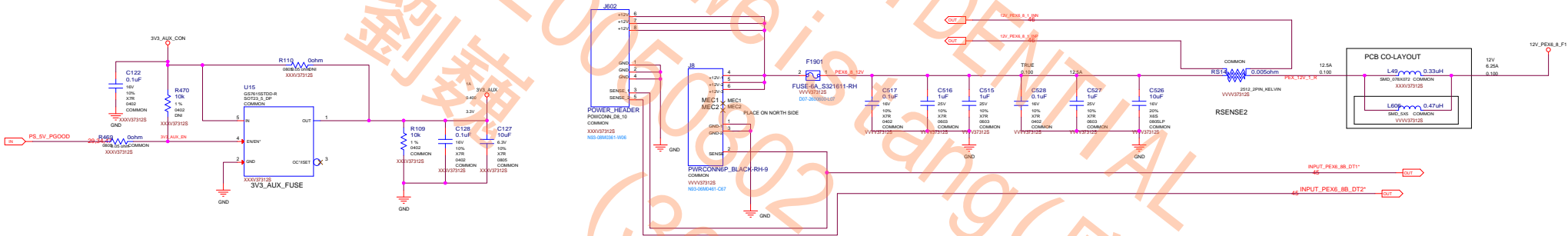
PEX 3V3 INPUT - 10W



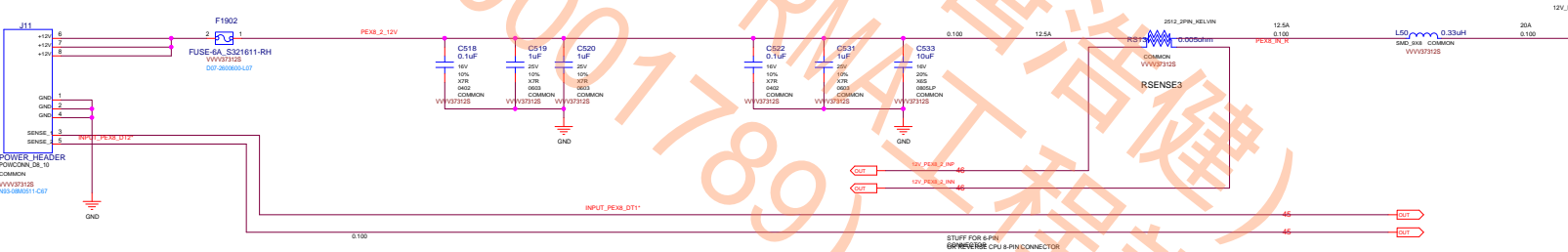
PEX\_12V INPUT - 66W



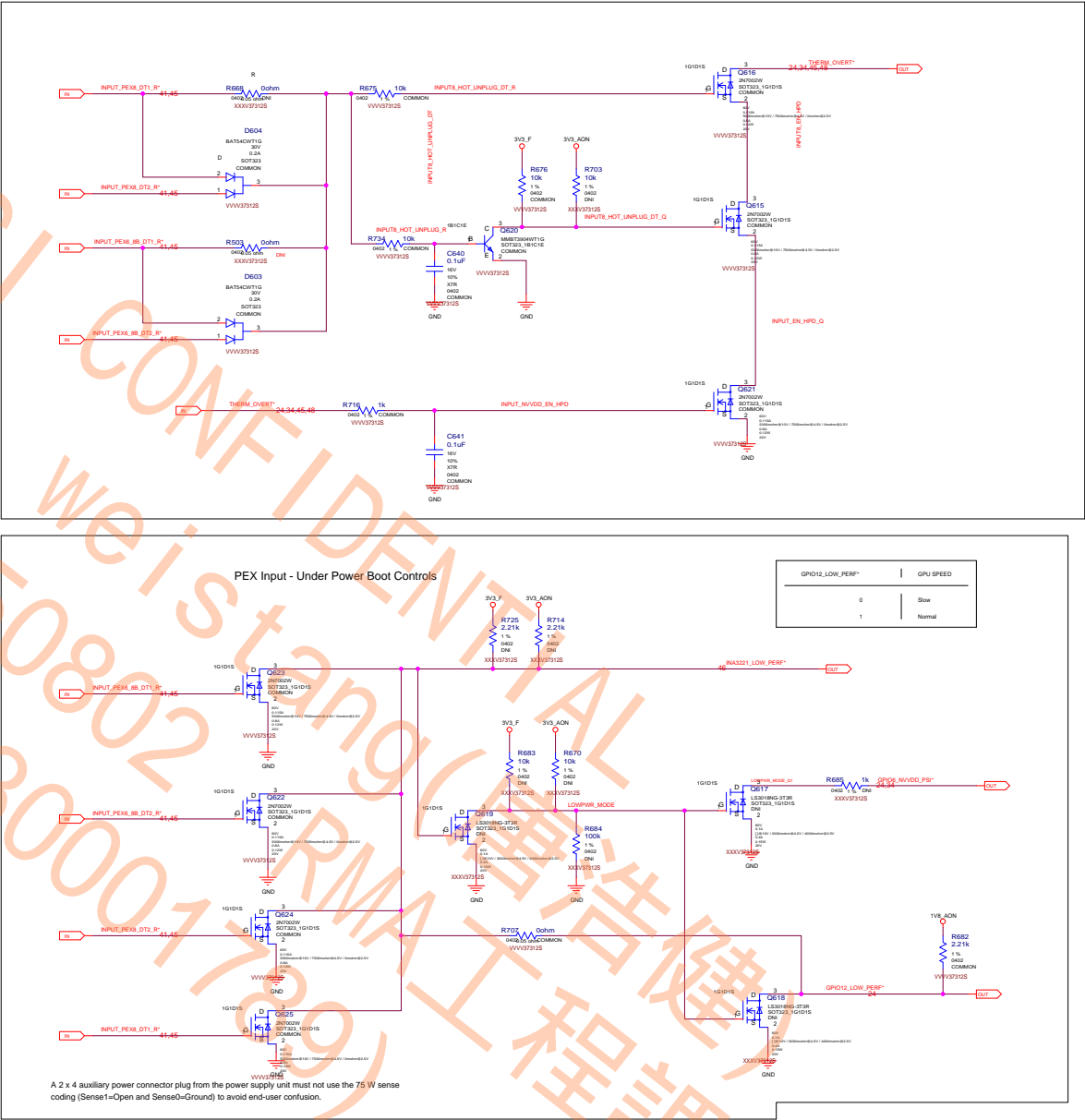
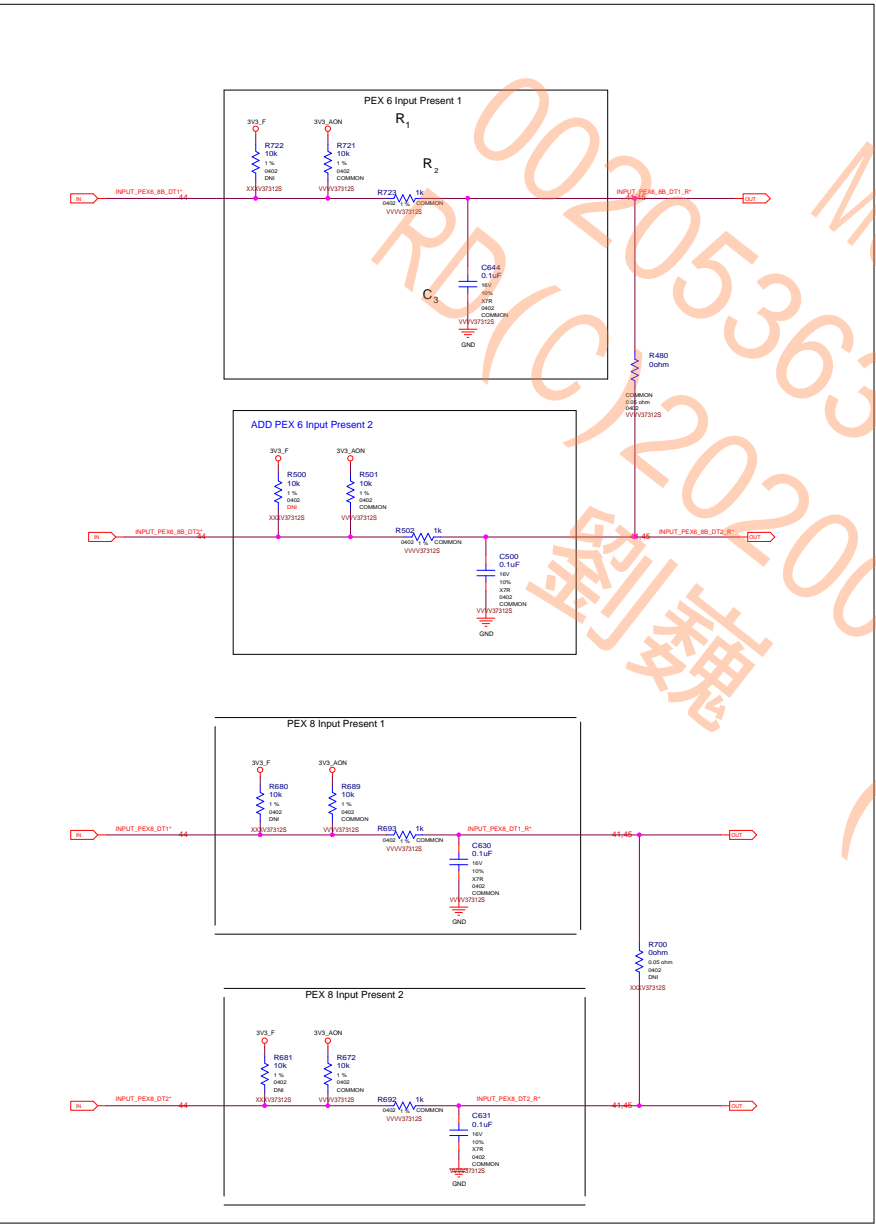
PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W

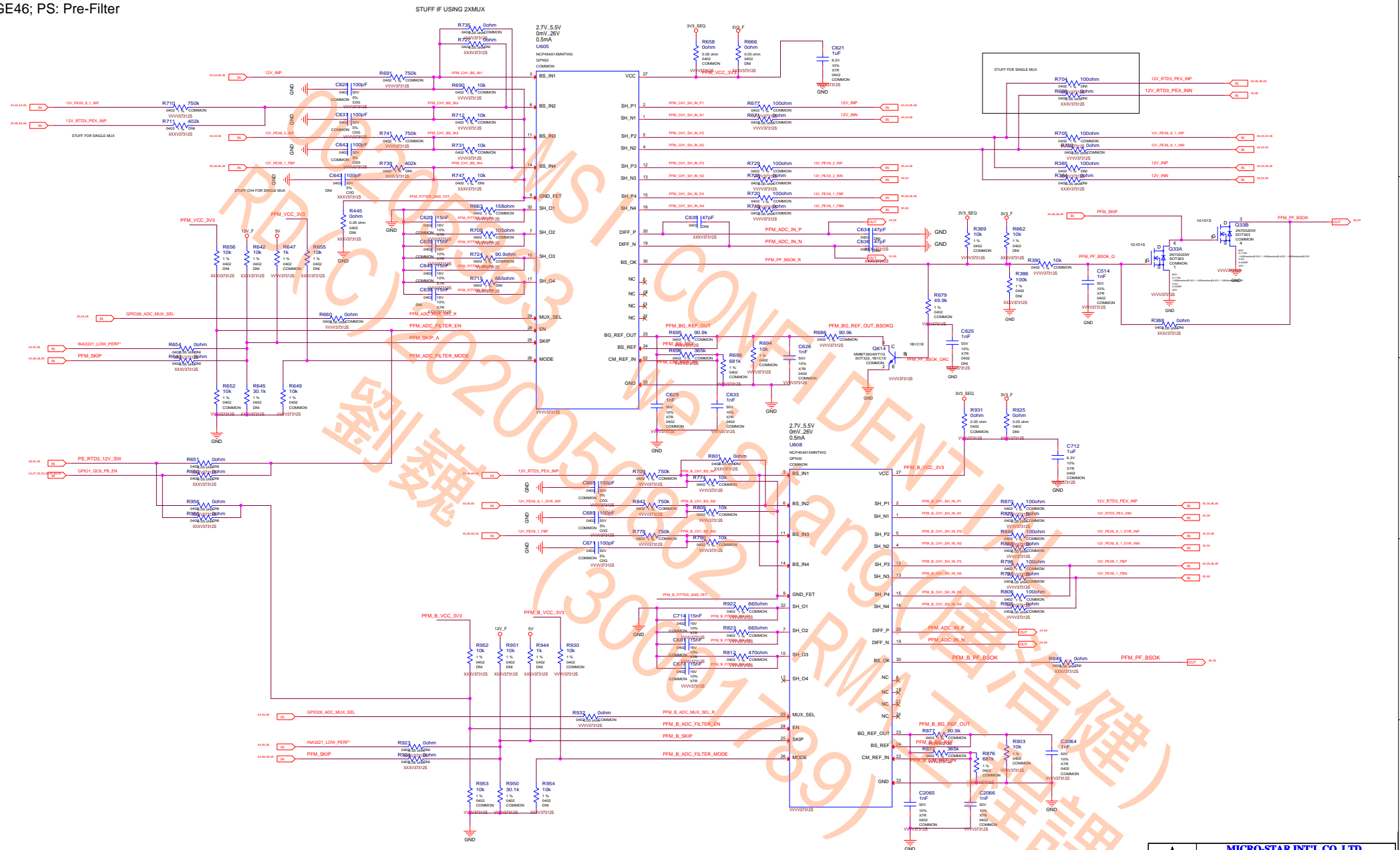




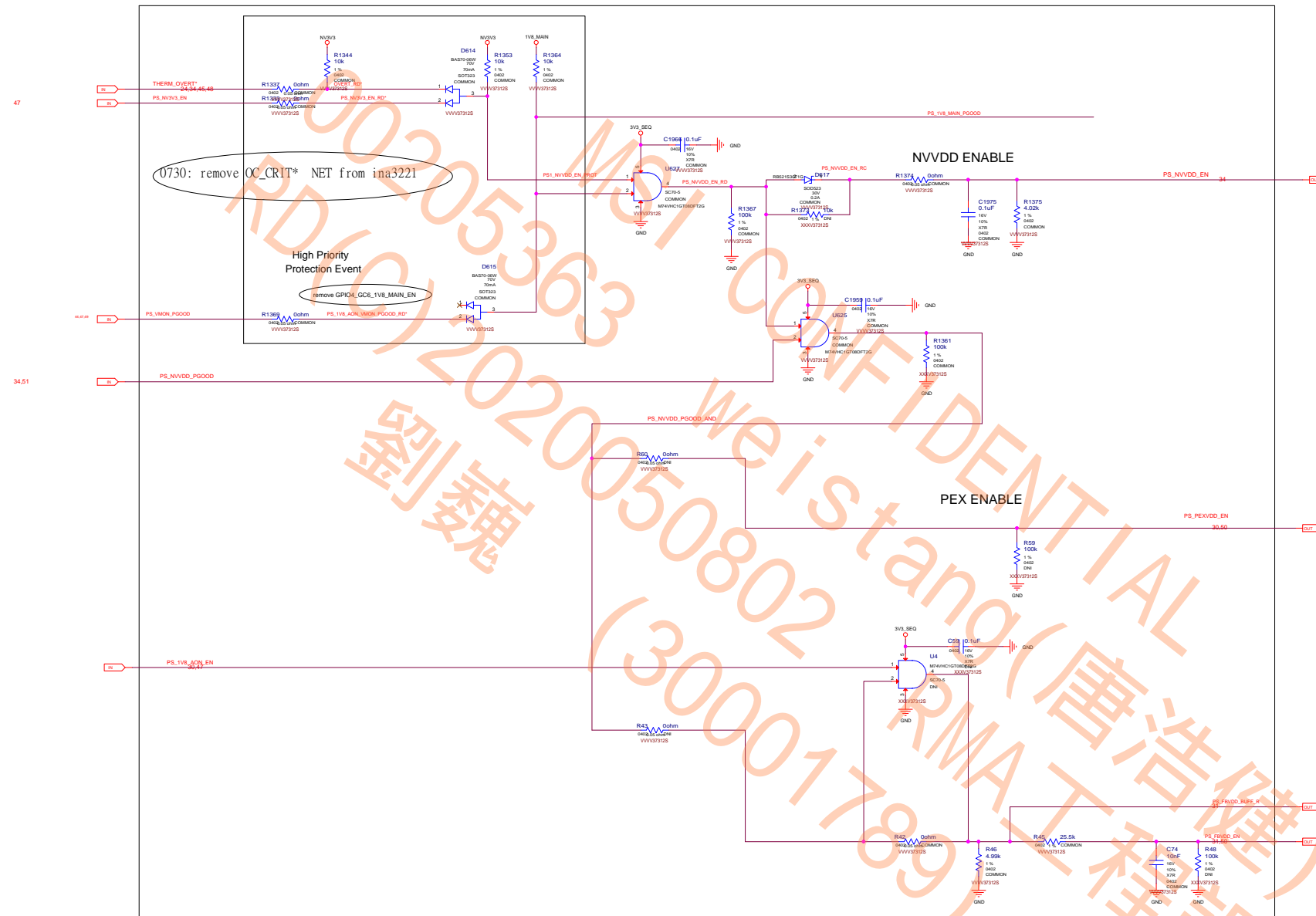


| GPI012_LOW_PERF* | GPIU SPEED |
|------------------|------------|
| 0                | Slow       |
| 1                | Normal     |

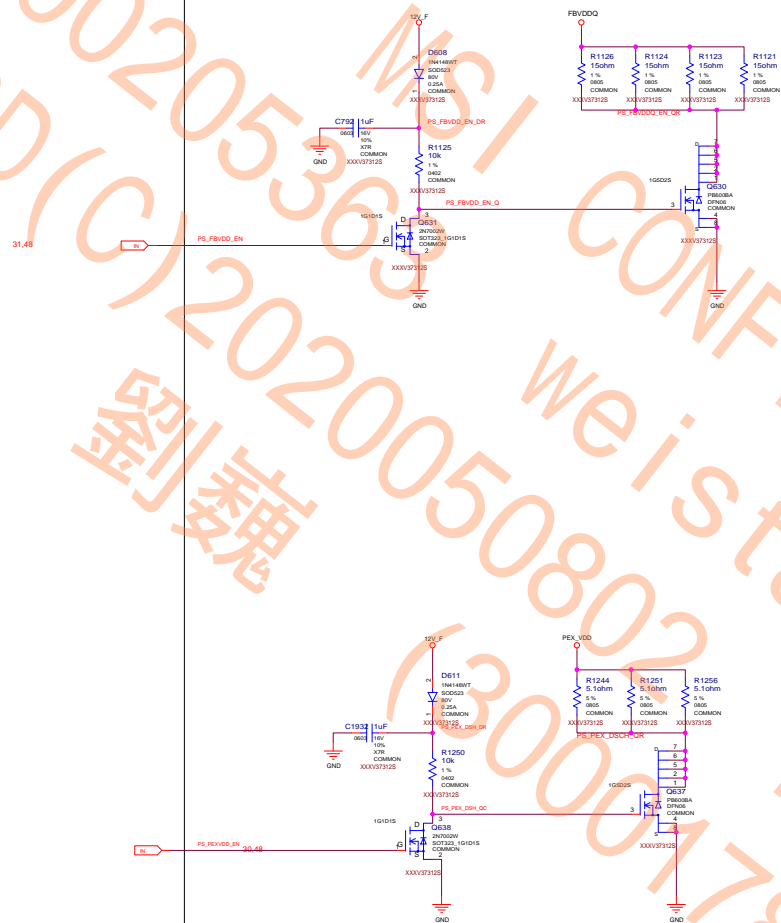
A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 V sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.



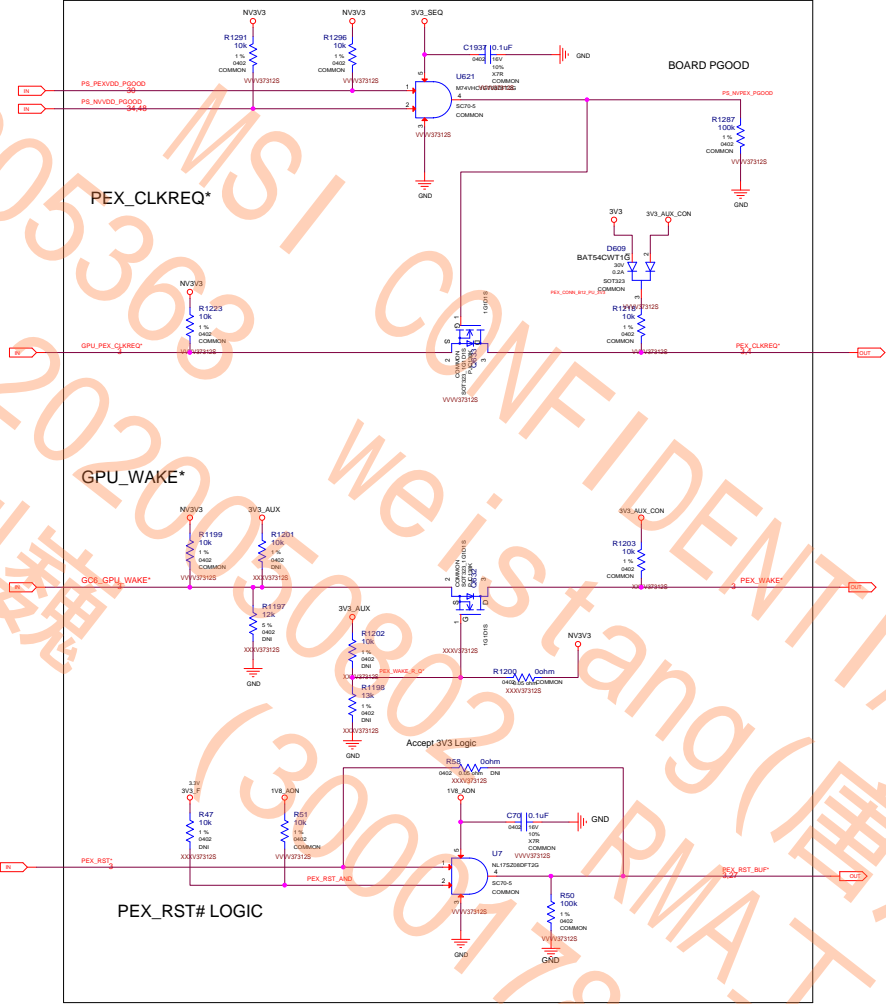






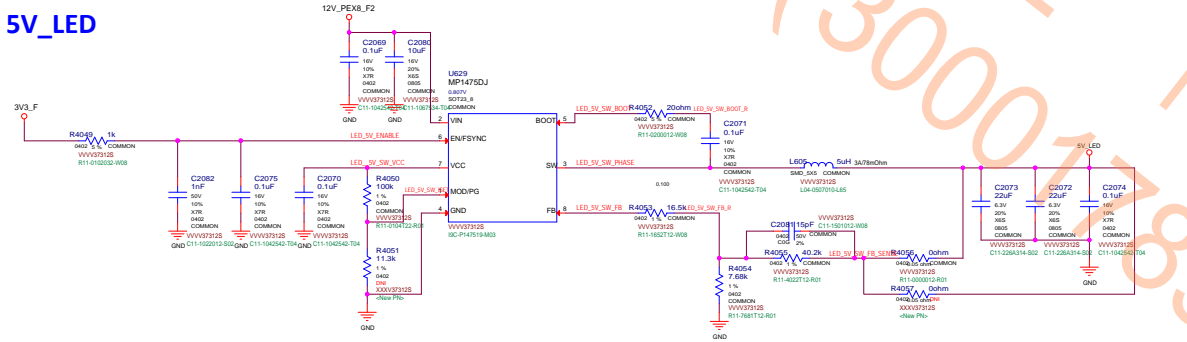
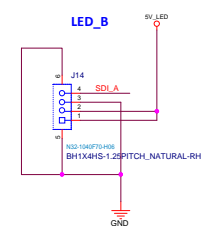
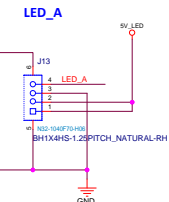
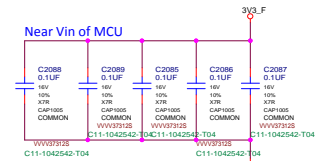
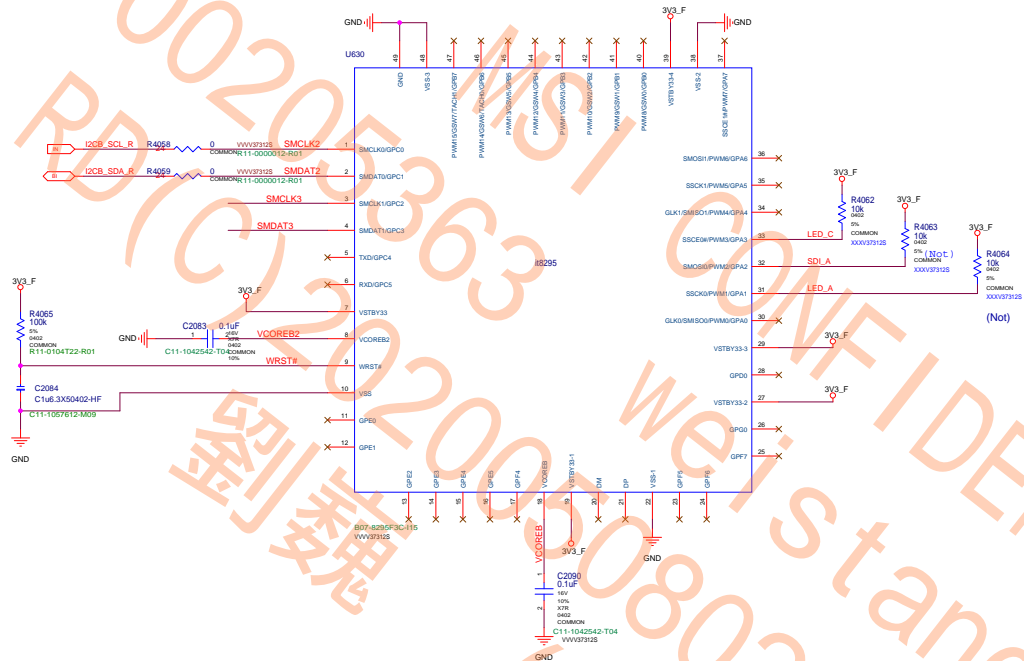
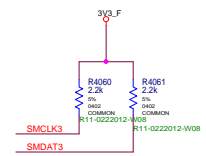
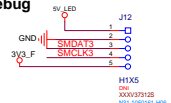


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