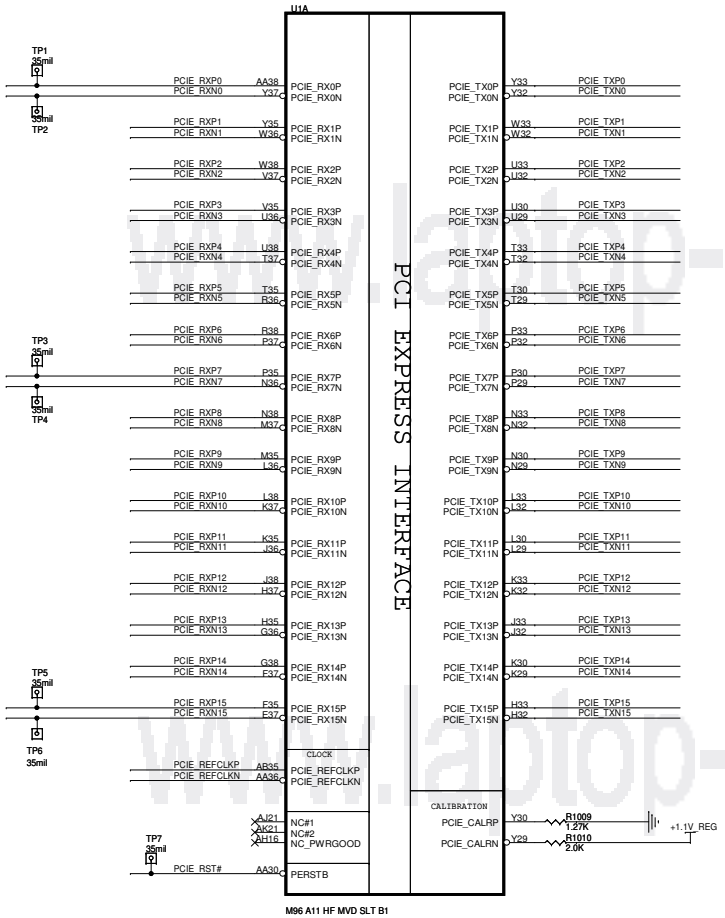

M96 A11 HF MVD SLT B1

(9,11) PCIE_RST# → PCIE_RST#

(9) PCIE_REFCLKP → PCIE_REFCLKP
(9) PCIE_REFCLKN → PCIE_REFCLKN

(9) PCIE_RXP[15..0] → PCIE_RXP[15..0]
(9) PCIE_RXN[15..0] → PCIE_RXN[15..0]
(9) PCIE_TXP[15..0] → PCIE_TXP[15..0]
(9) PCIE_TXN[15..0] → PCIE_TXN[15..0]

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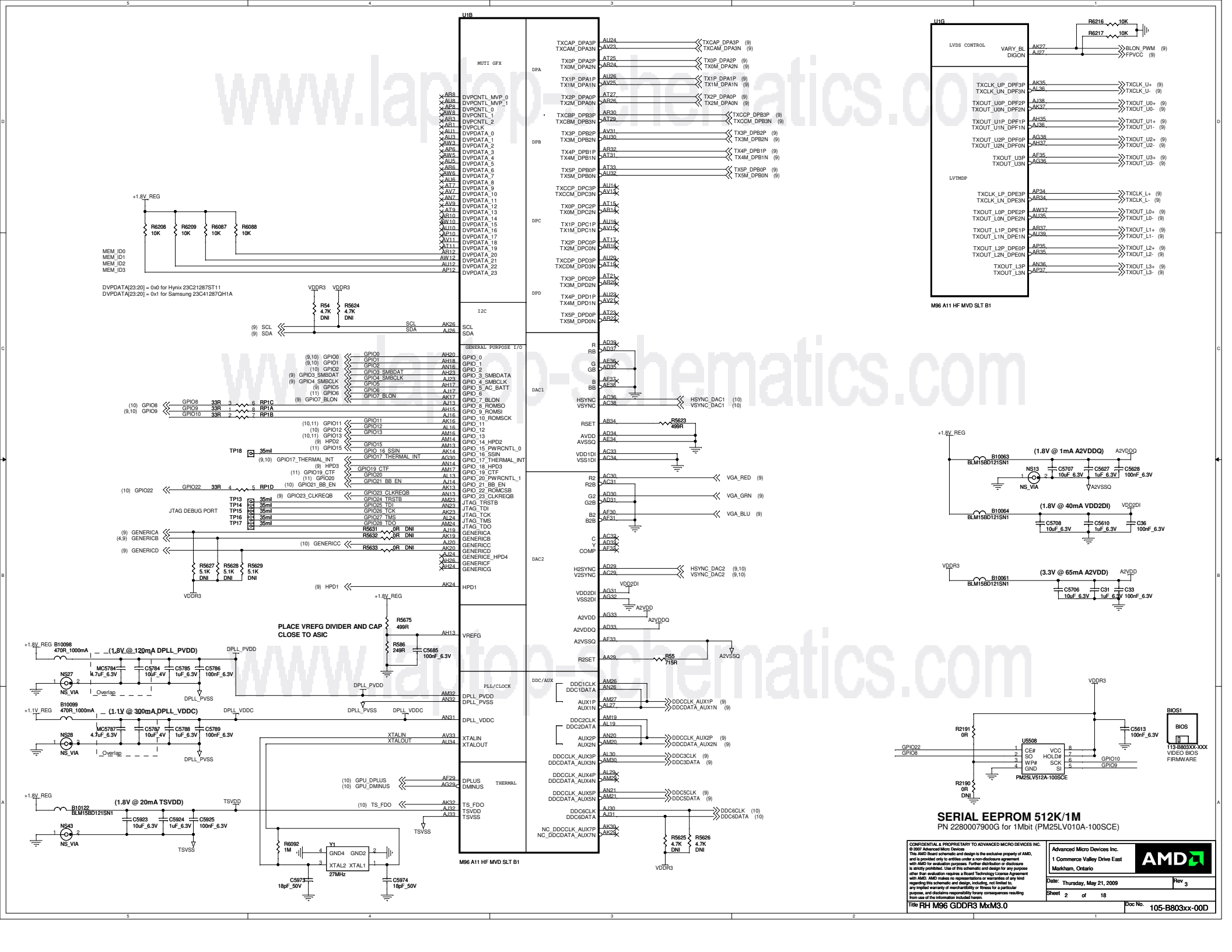

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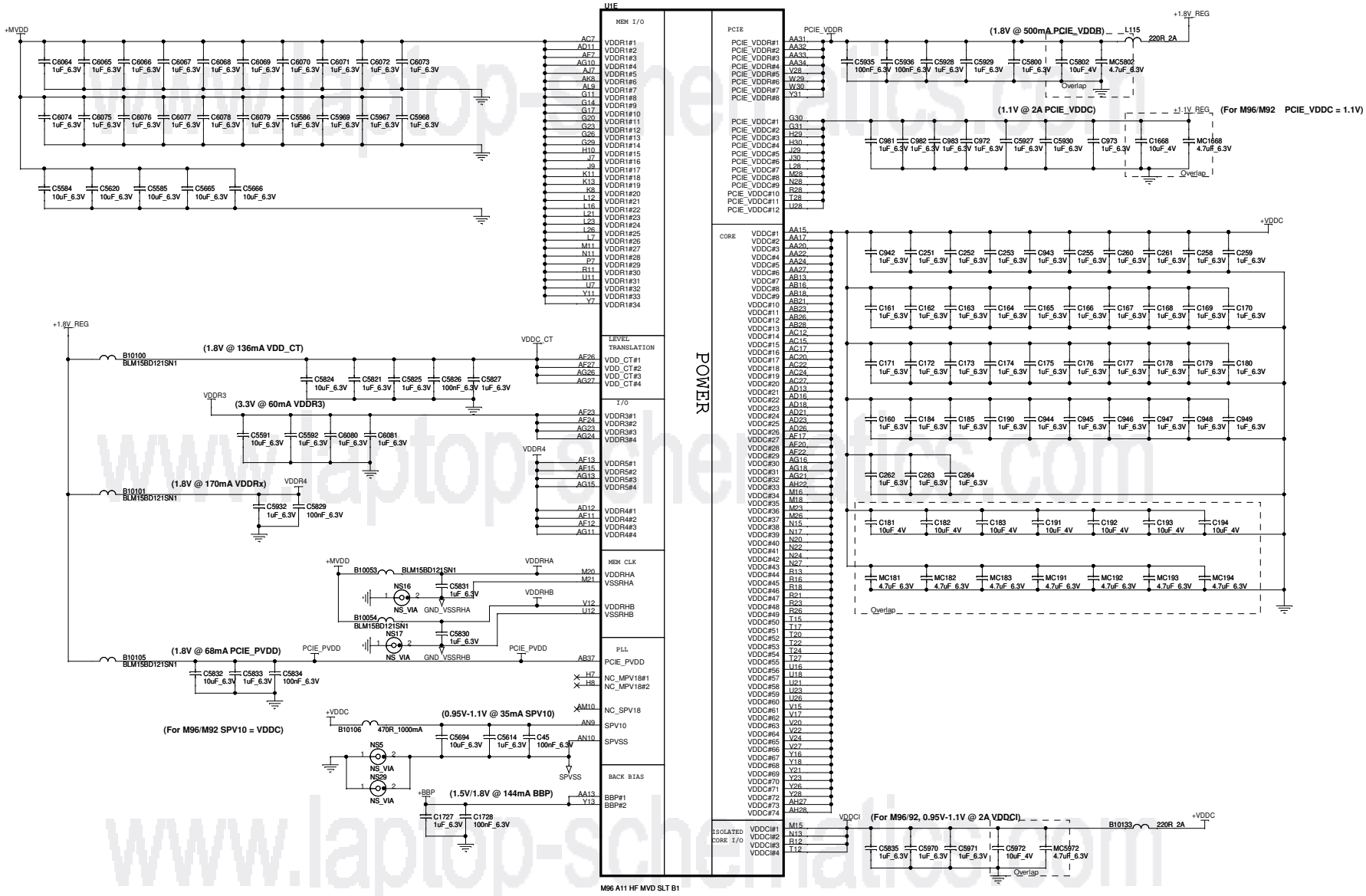
Title RH M96 GDDR3 MxM3.0	Doc No. 105-B803xx-00D



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Title	RH M96 GDDR3 MxM3.0
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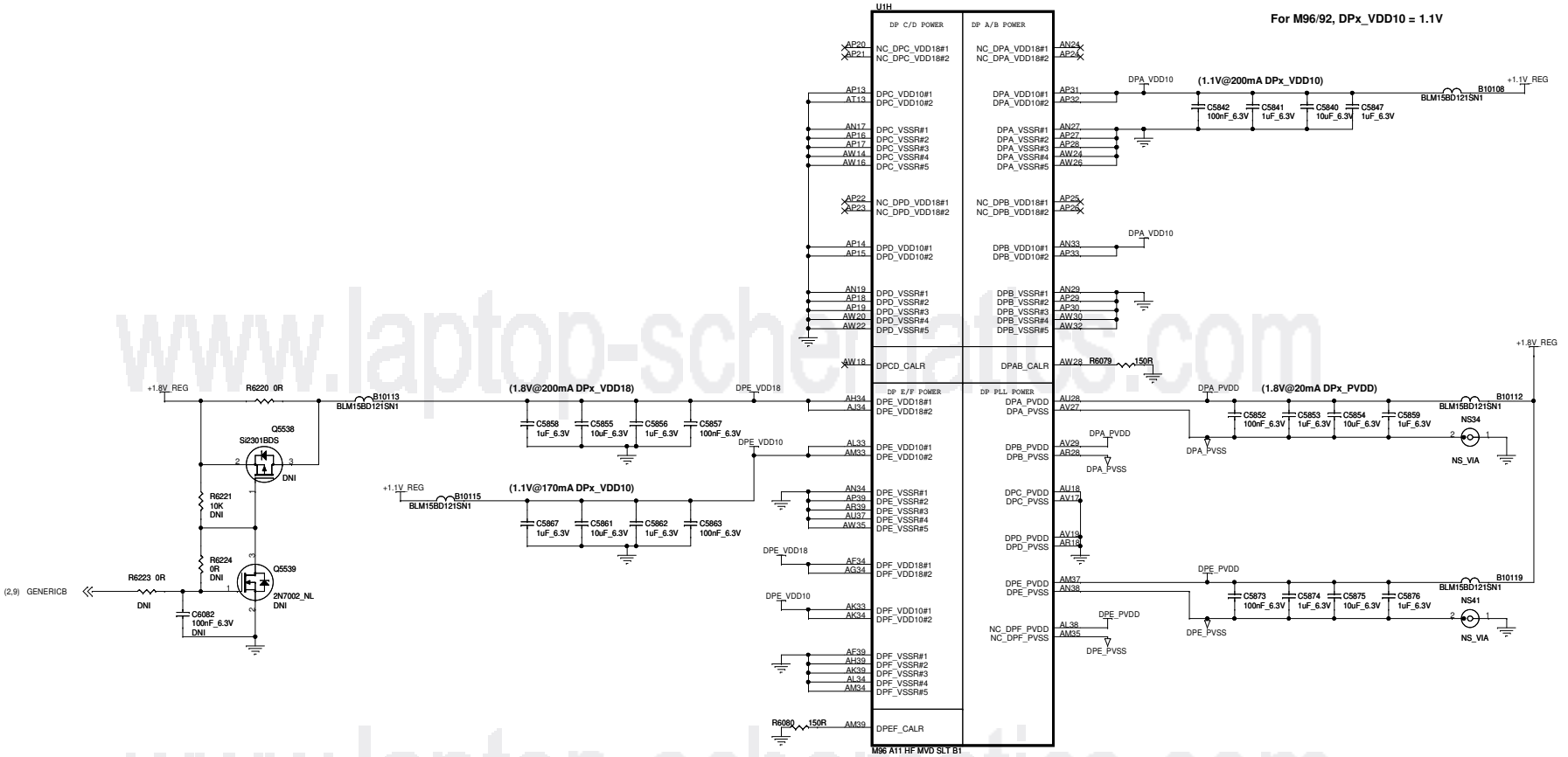

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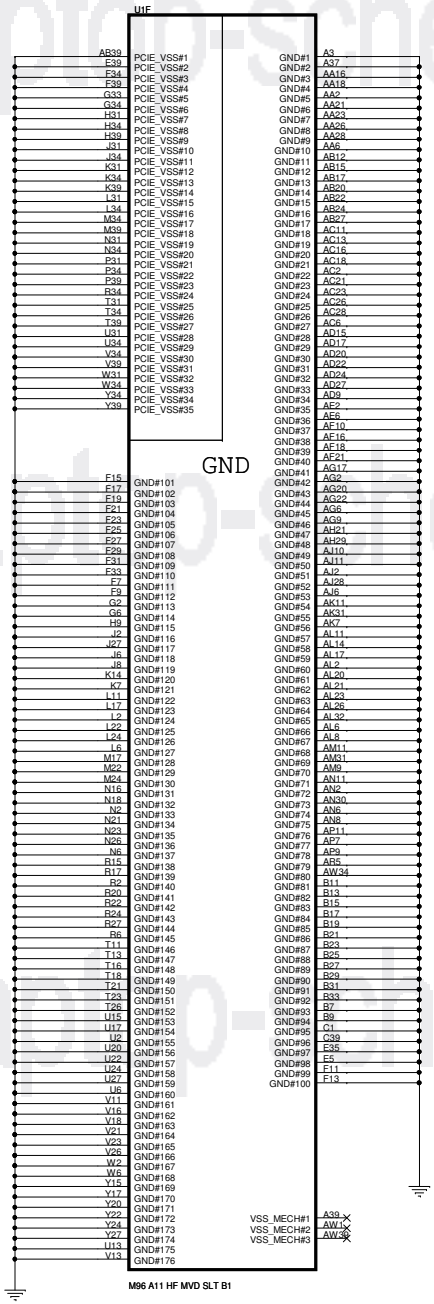

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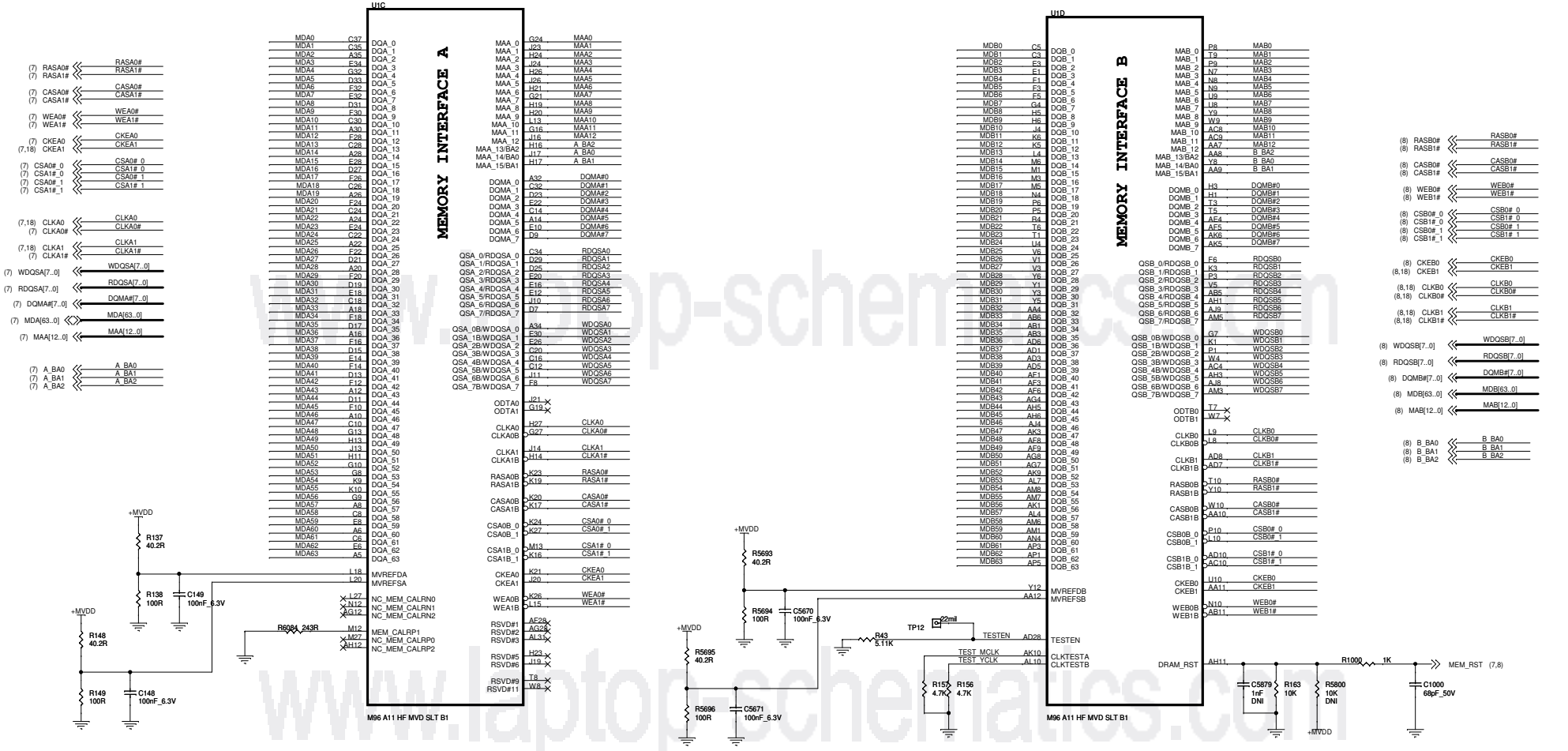

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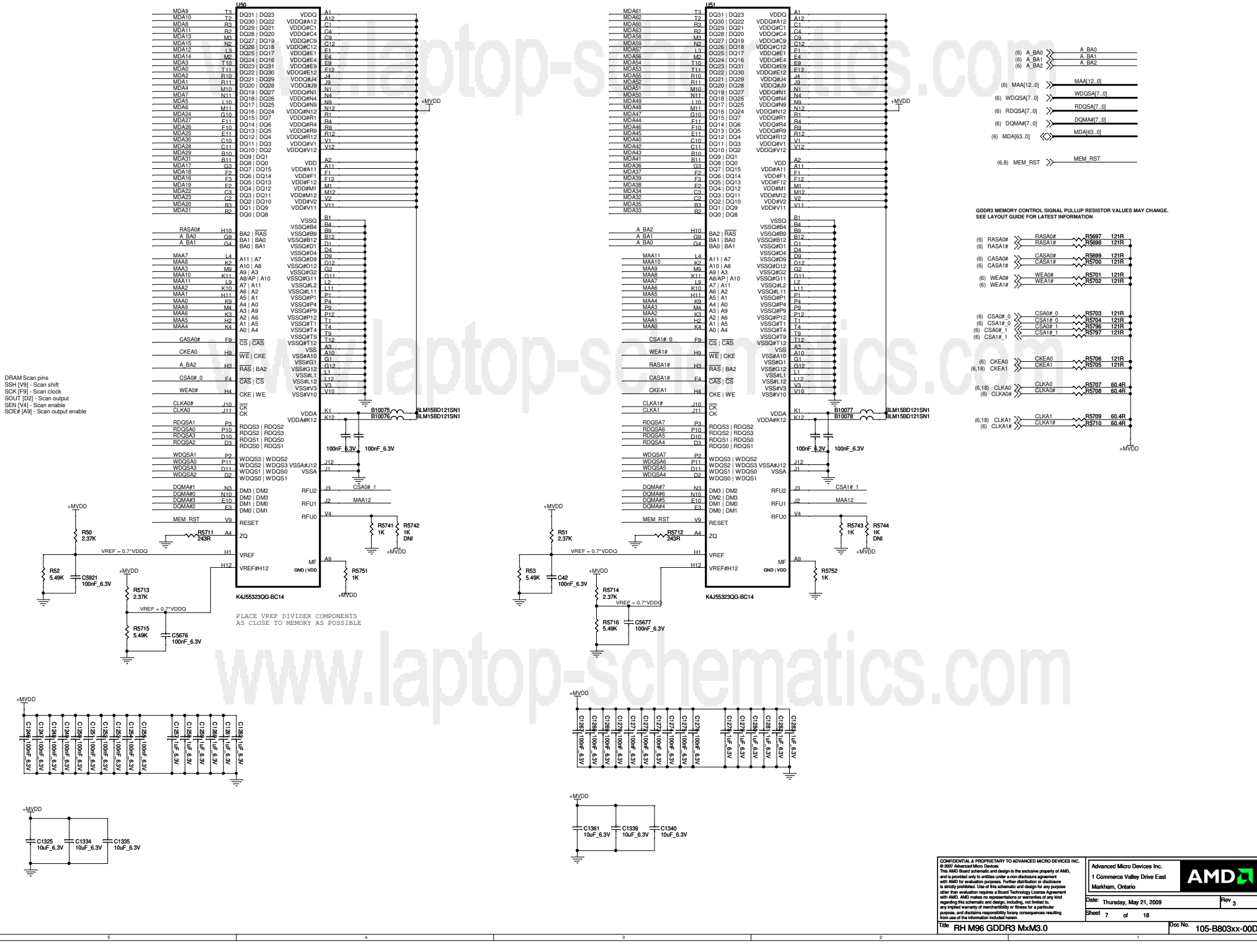
GDDR3 32X32 MEMORY



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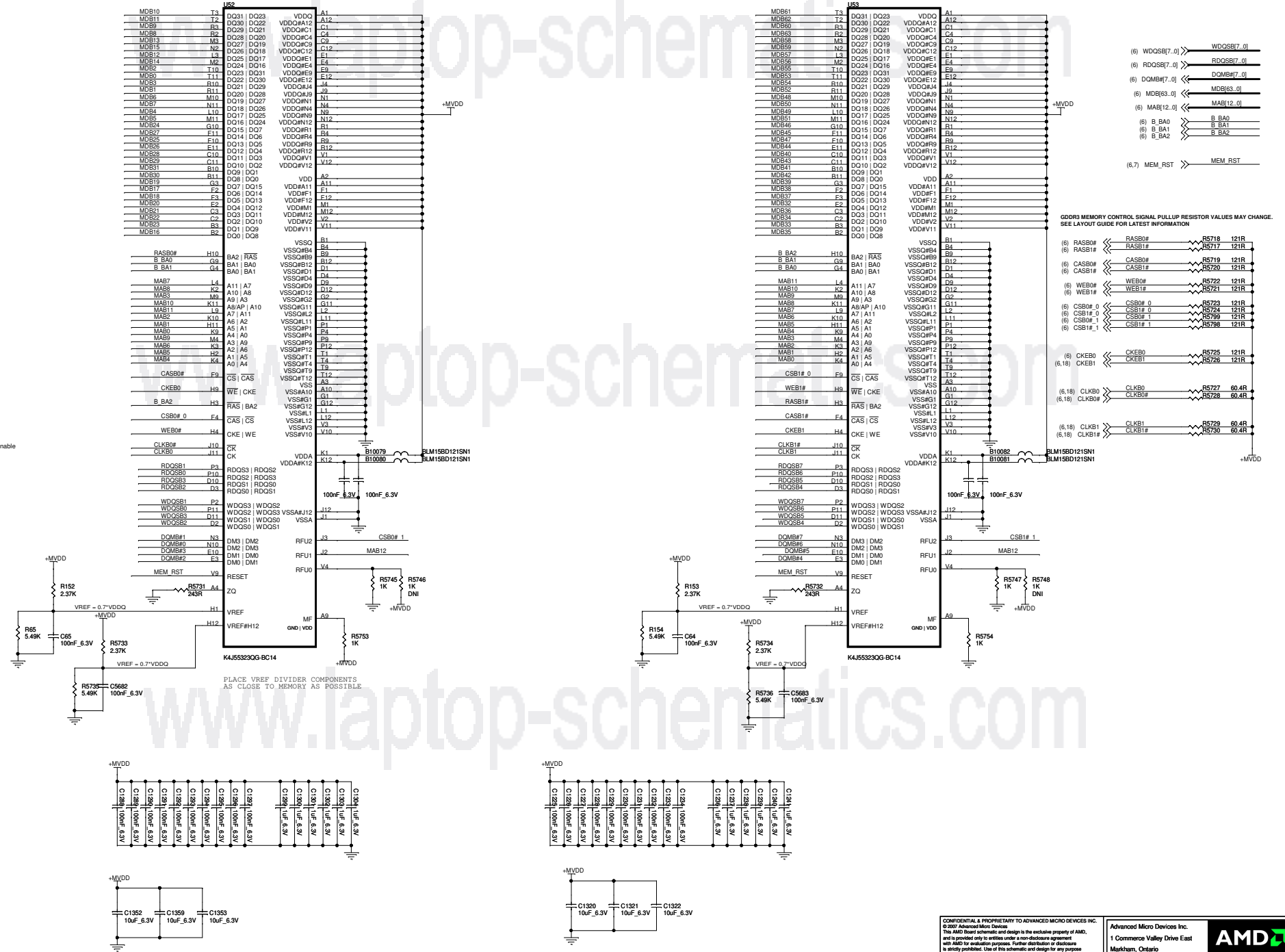
GDDR3 32X32 MEMORY



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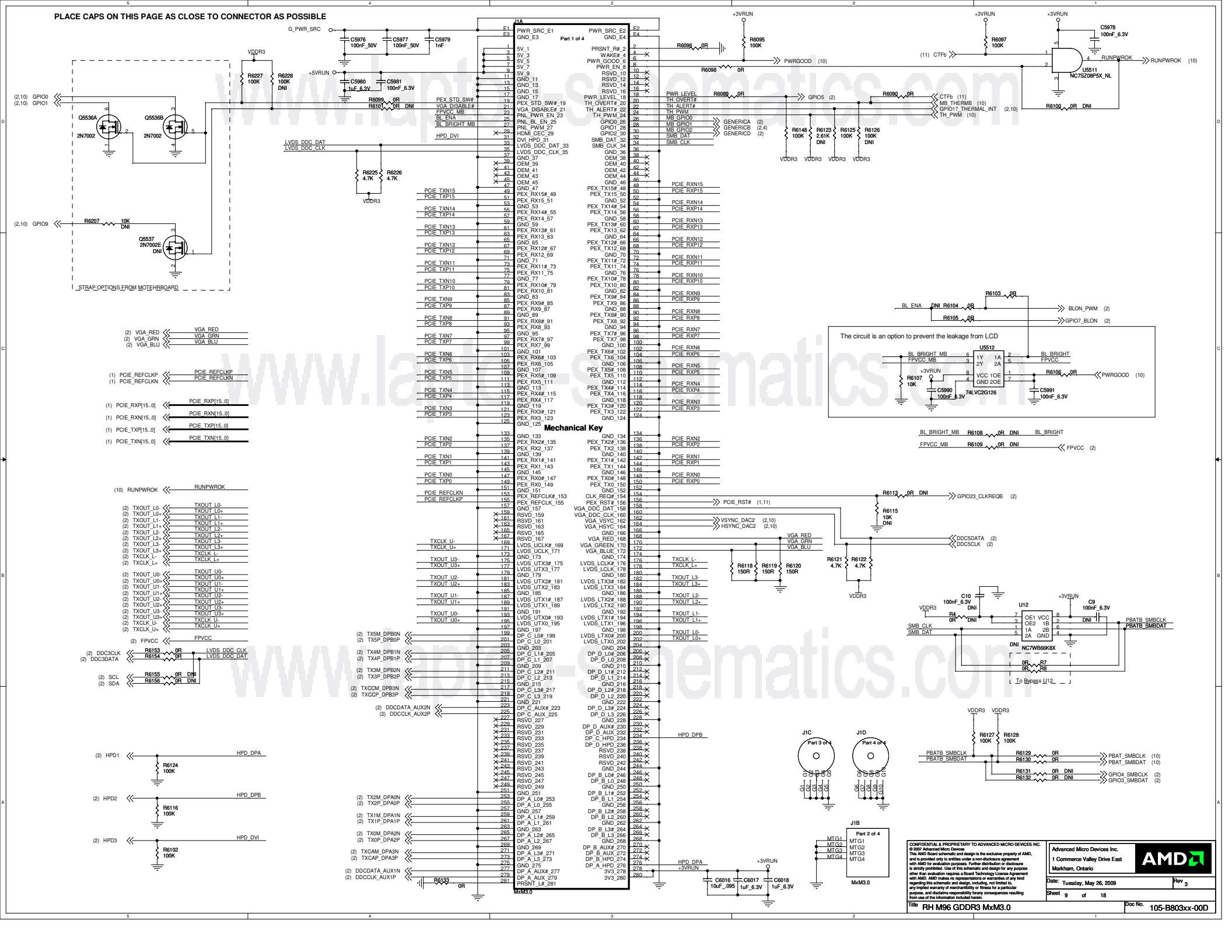
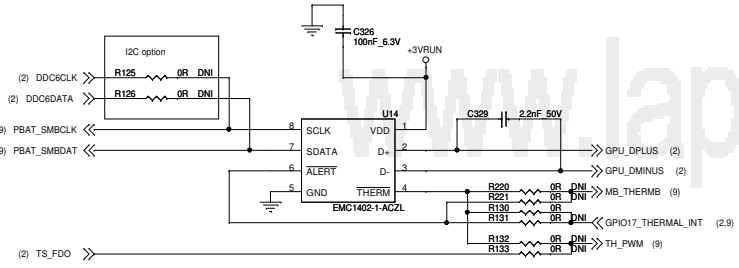
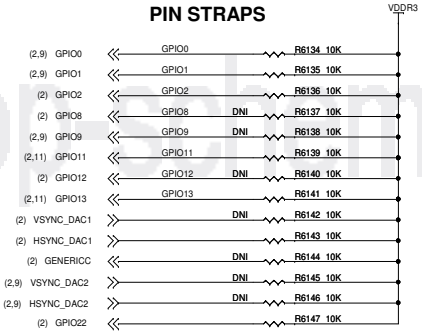
PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE





Power Up Sequence

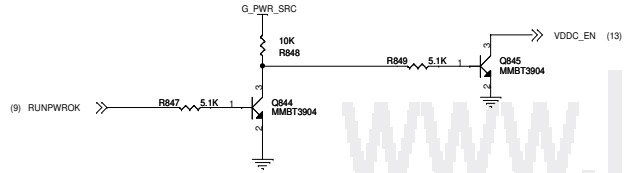
PIN STRAPS

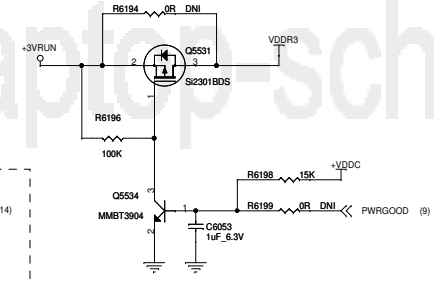


CONFIGURATION STRAPS

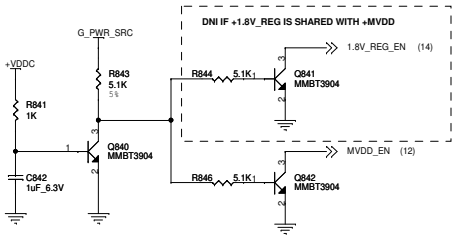
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

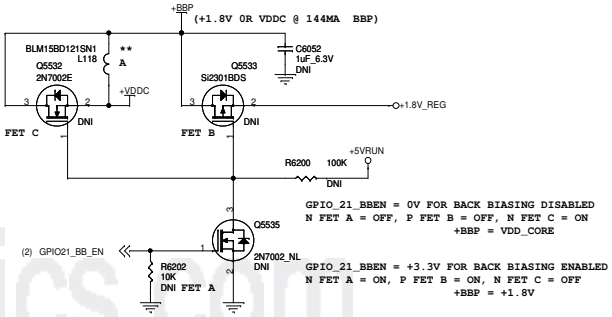
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing GPIO0 and GPIO1 pulls ups need to be stuffed with Q5536 if system board is controlling the PCIE swing.	0
TX_DEEMPH_EN	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	PCIE Gen2 Enable 0: Advertises the PCIE device as 2.5GT/s capable at power-on 1: Advertises the PCIE device as 5.0GT/s capable at power-on	1
BIF_CLK_PM_EN	GPIO8	Master control for CLKREQb 0: Disabled 1: Enabled	0
BIF_VGA DIS	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU) GPIO9 pull up needs to be stuffed with Q5537 if system board is controlling the VGA capacity	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	1
ROMIDCFG[2:0]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type	XXX 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)
VIP_DEVICE_STRAP_ENA	V2SYNC	VIP Device Strap Enable 0: Slave VIP host port devices present 1: No slave VIP host port devices reporting presence	0
AUD[1] AUD[0]	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
SMS_EN_HARD CCBYPASS	H2SYNC GENERICC	Reserved Reserved	N/A





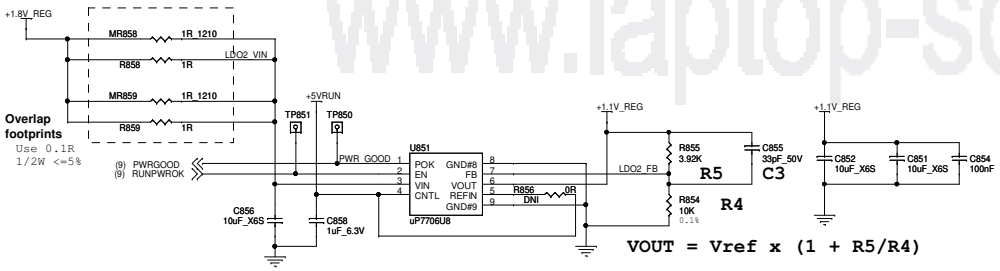
VDDR3 Enable Circuit





LDO #2: Vin = +1.8V +/-5% Vout = +1.1V +/- 2% Iout = 1.7A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



VOUT = Vref x (1 + R5/R4)

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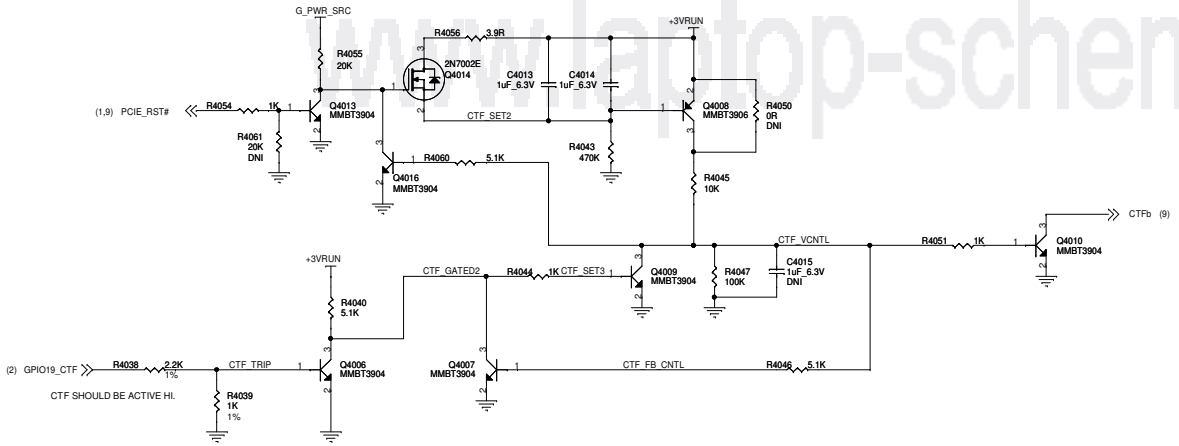
Critial Temperature Fault

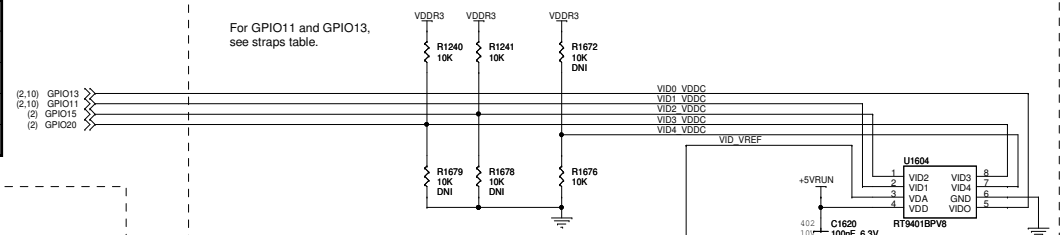


Power Play

GPIO20	GPIO15	VDDC
0	0	1.20V
0	1	1.12V
1	0	1.04V
1	1	0.95V

VID for VDDC Setting

For GPIO11 and GPIO13, see straps table.

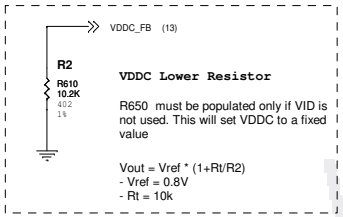


R1689 & R1690 must be selected to limit MAX ref voltage to MAX VDDC.

See BOM for qualified values.

Table 4 VDDC Vref Mode Selection

Vref Mode	R636	R639/C659	Vref (V)
Internal	Populate	NC	0.6
External	NC	Populate	set by VID IC (U1604)

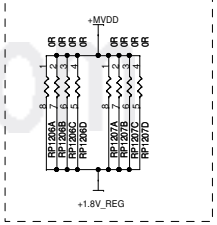


VDDC Lower Resistor

R650 must be populated only if VID is not used. This will set VDDC to a fixed value

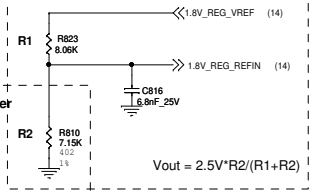
Vout = Vref * (1+Rt/R2)
- Vref = 0.8V
- Rt = 10k

MVDD & 1.8V_REG Share



DNI IF +1.8V_REG IS SHARED WITH +MVDD

For Version 2 1.8V_REG Controller



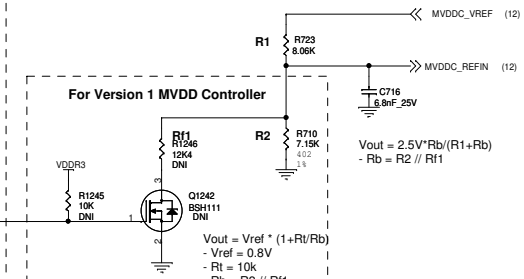
Vout = 2.5V*R2/(R1+R2)

For Version 1 1.8V_REG Controller

Vout = Vref * (1+Rt/R2)
- Vref = 0.8V
- Rt = 10k

GPIO6	MVDD
0	TBD
1	TBD

For Version 2 MVDD Controller



Vout = 2.5V*Rb/(R1+Rb)
- Rb = R2 // Rf1

For Version 1 MVDD Controller

Vout = Vref * (1+Rt/Rb)
- Vref = 0.8V
- Rt = 10k
- Rb = R2 // Rf1

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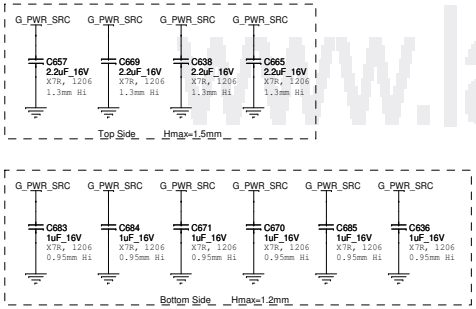
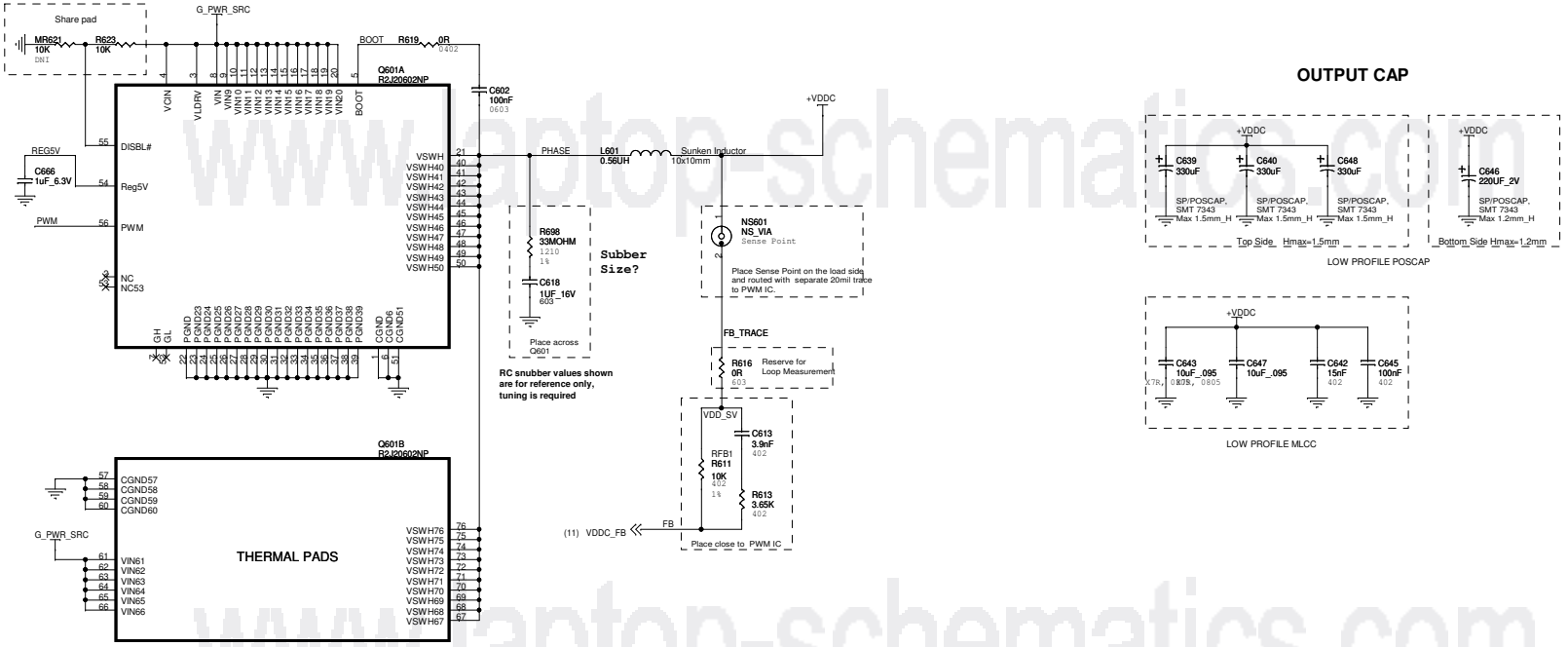
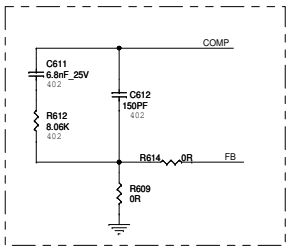
INPUT CAP



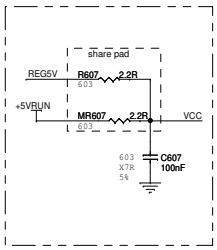


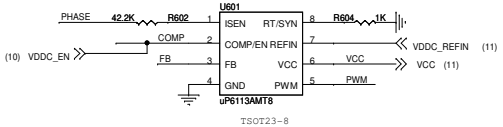
OUTPUT CAP

COMPENSATION CIRCUIT



FILTERED SMPS VCC





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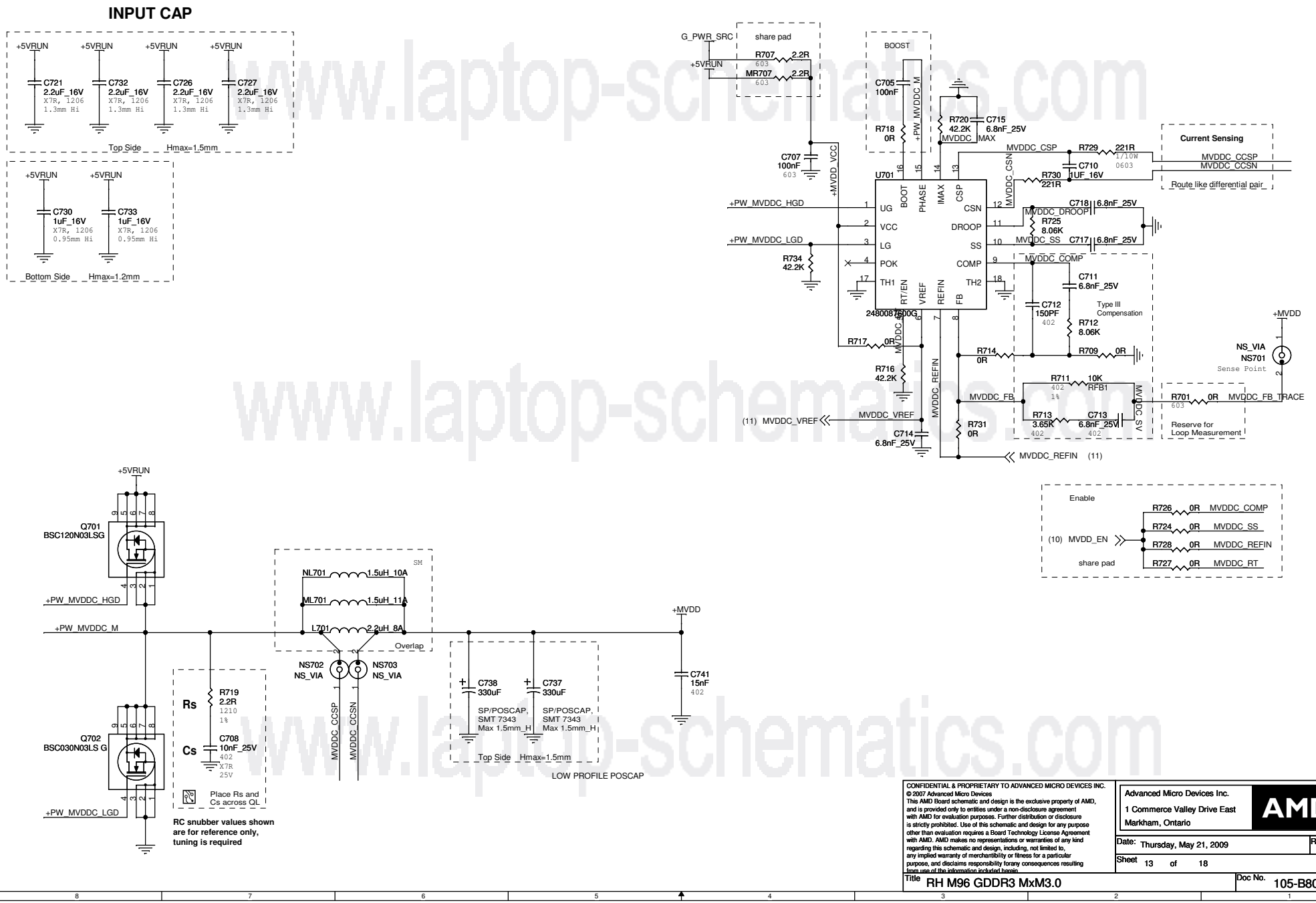

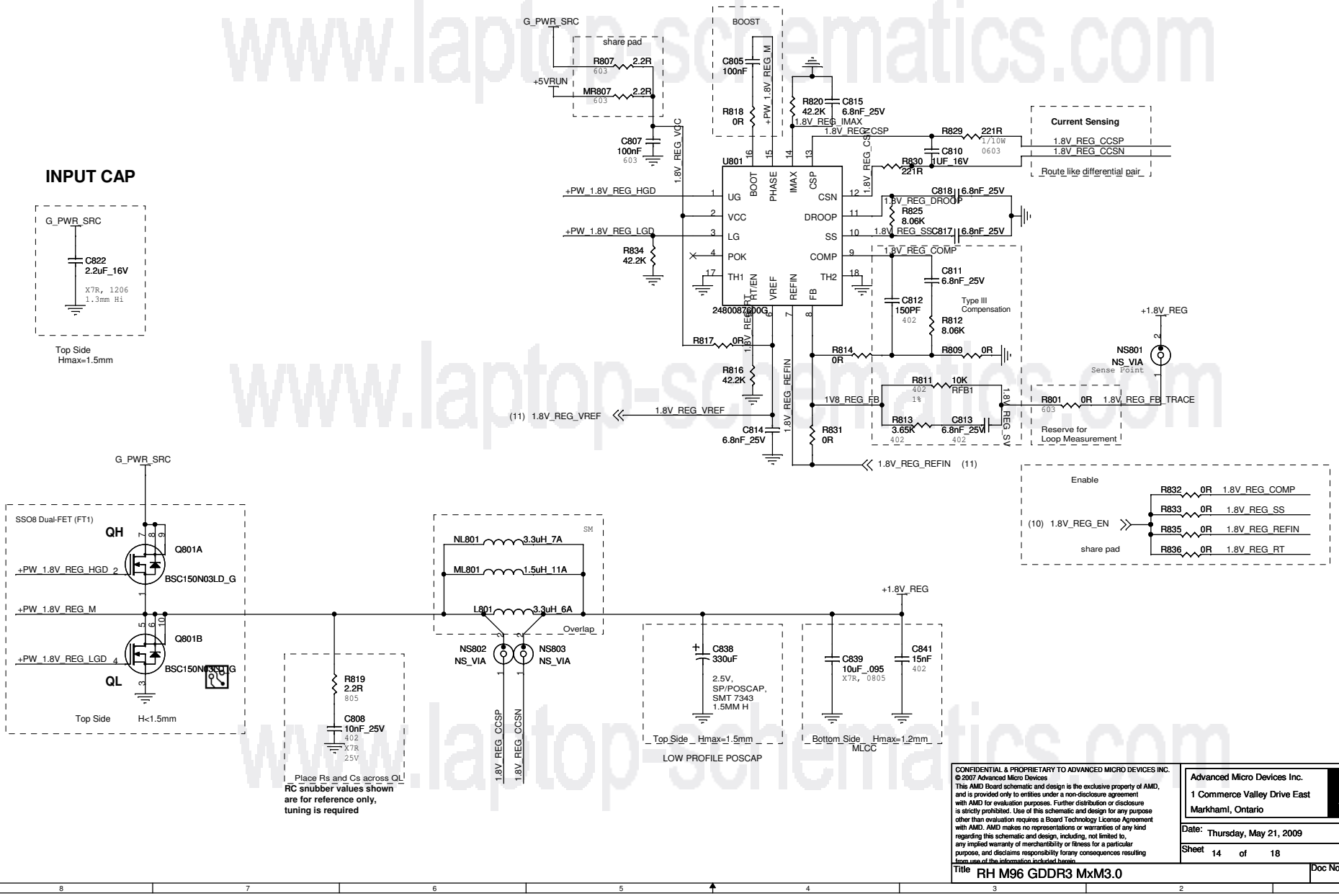

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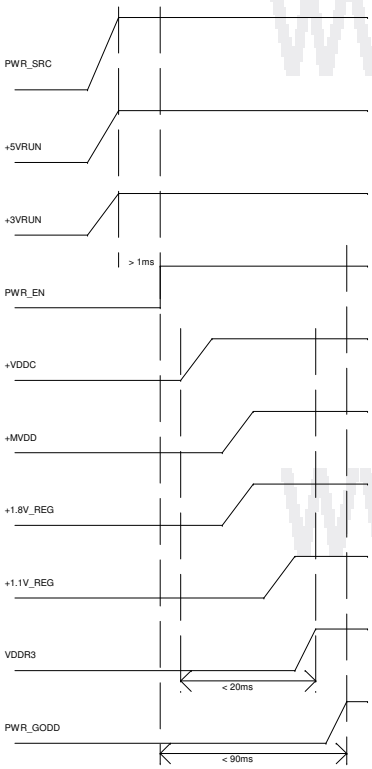
POWER UP SEQUENCE (not to scale)



VDDC, VDDCI, SPV10

VDDR1, VDDRH, MVDDQ/C

VDDR4/5, VDD_CT, TSVDD, PCIE_VDDR, PCIE_PVDD, DPLL_PVDD, DPx_PVDD, DPx_VDD18, A2VDDQ, VDD2DI

PCIE_VDDC, DPLL_VDDC, DPx_VDD10

+1.1V_REG AND VDDR3 RAMP UP SEQUENCE CAN BE INTERCHANGED.

VDDR3, A2VDD

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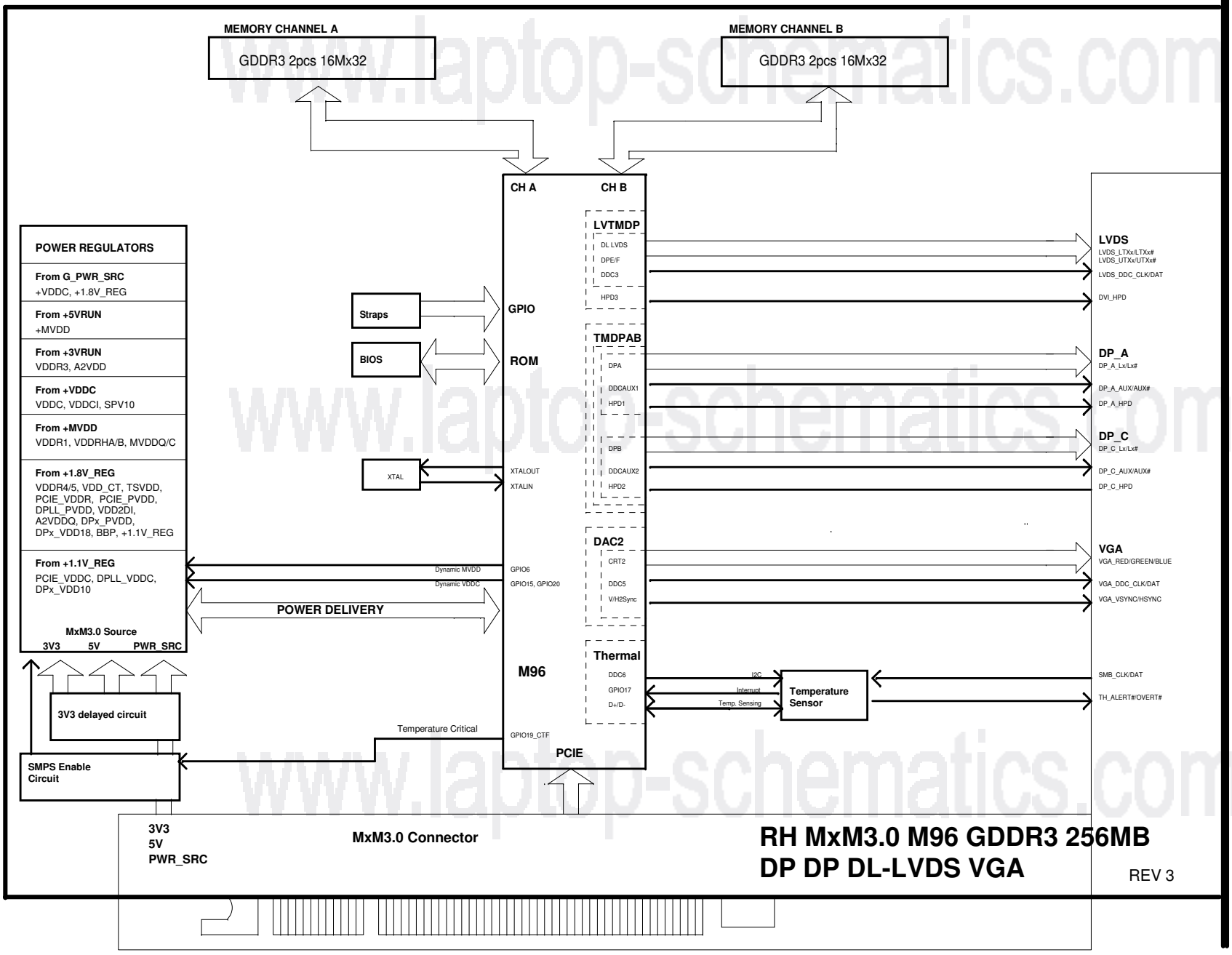

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Title	Schematic No.	Date:
RH M96 GDDR3 MxM3.0	105-B803xx-00D	Thursday, May 21, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 3

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	08/12/31	Initial design for M96 GDDR3 MxM3.0 based on B703-00C
1	00B	09/04/15	Add boundry scan feature for DRAMs; Add R5751~R5754 Add R5741~R5748 Add a series resistor (R1000) and a shunt cap (C1000) to mem_rst
2	00C	09/04/22	Add R6227, R6228 Update J1 (non-plated holes connected to ground)

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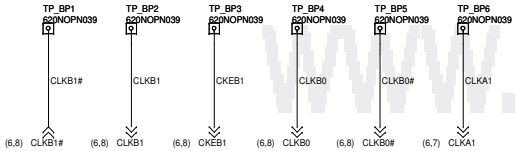

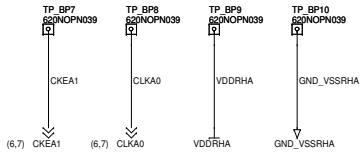

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