PG132-A02

320W, FH Std PCB, 320b, GDDR6X 2CH x16 DP + DP + DP + HDMI

TABLE OF CONTENTS

Page	Description	Page	Description	Page	Description
1	Table of Contents		MISC: THERMAL, JTAG, GPIO	51	BLANK
2	BLOCK DIAGRAM	27	IFPA UNUSED, IFPB UNUSED	52	PS: NVVDD Controller_OVR8
3	PCI EXPRESS	28	IFPE DP	53	PS: NVVDD PH1 (PWM1)
4	MEMORY: GPU PARTITION A/B	29	IFPD DP	54	PS: NVVDD PH2(PWM6)
5	MEMORY: FBA PARTITION[31:0]	30	IFPC HDMI/DP	55	PS: NVVDD PH3 (PWM3) and P
6	MEMORY: FBA PARTITION[63:32]	31	IFPF DP	56	PS: NVVDD PH5(PWM7) and Ph
7	MEMORY: FBB PARTITION[31:0]	32	MISC. ROM, STRAPS	57	PS: NVVDD PH6 (PWM7)
8	MEMORY: FBB PARTITION[63:32]	33	MISC. XTAL, PLL	58	PS: NVVDD PH8(PWM5) and Ph
9	MEMORY: GPU PARTITION C/D	34	PS: 5V	59	PS: NVVDD PH10 (PWM4)
10	MEMORY: FBC PARTITION[31:0]	35	PS: PEX_DVDD and 1V8	60	Colayout_Notes
11	MEMORY: FBC PARTITION[63:32]	36	BLANK	61	BLANK
12	MEMORY: FBD PARTITION[31:0]	37	PS: FBVDD Controller OVR3	62	PS: NVVDD OUTPUT CAP(TOP)
13	MEMORY: FBD PARTITION[63:32]	38	PS: FBVDDQ OVR4	63	BLANK
14	MEMORY: GPU PARTITION E/F	39	PS: FBVDD PH1	64	PS: INPUT SWITCH RTD3
15	MEMORY: FBE PARTITION[31:0]	40	PS: FBVDD PH3	65	BLANK
16	MEMORY: FBE PARTITION[63:32]	41	PS: FBVDD PH2	66	PS: INPUTS, FILTERING, and, I
17	MEMORY: FBF PARTITION[31:0]	42	PS: FBVDD PH4	67	PS: HOT UNPLUG
18	MEMORY: FBF PARTITION[63:32]	43	PS: FBVDD OUTPUT CAP	68	PS: Discrete Power Steering
19	GPU GND, RFUs & RSVD	44	PS: FBVDD_OUTPUT_CAP_NEAR_MEMORY	69	PS: PREFILTER
20	GPU POWERS	45	PS: MSVDD CONTROLLER	70	PS: PREFILTER B
21	GPU DECOUPLING NVVDD	46	PS: MSVDD PH1	71	Sequence: 5V, 1V8, 3V3_SEQ
22	GPU DECOUPLING FBVDDQ	47	PS: MSVDD PH2	72	Sequence: NV, PEX, FB EN
23	GPU DECOUPLING MSVDD	48	PS: MSVDD PH3 and PH5	73	Sequence: 3V3 MONITOR
24	BLANK	49	PS: MSVDD PH4 and PH6	74	Sequence: MISC
25	NVHS x16	50	PS: MSVDD OUTPUT CAP(TOP)	75	MISC: LED & FAN

53	PS: NVVDD PH1 (PWM1)
54	PS: NVVDD PH2(PWM6)
55	PS: NVVDD PH3 (PWM3) and PH4 (PWM3)
56	PS: NVVDD PH5(PWM7) and PH7(PWM8)
57	PS: NVVDD PH6 (PWM7)
58	PS: NVVDD PH8(PWM5) and PH9(PWM2)
59	PS: NVVDD PH10 (PWM4)
60	Colayout_Notes
61	BLANK
62	PS: NVVDD OUTPUT CAP(TOP)
63	BLANK
64	PS: INPUT SWITCH RTD3
65	BLANK
66	PS: INPUTS, FILTERING, and, MONITORING
67	PS: HOT UNPLUG
68	PS: Discrete Power Steering
69	PS: PREFILTER
70	PS: PREFILTER B
71	Sequence: 5V, 1V8, 3V3_SEQ
72	Sequence: NV, PEX, FB EN
73	Sequence: 3V3 MONITOR
74	· · · · · · · · · · · · · · · · · · ·
75	MISC: LED & FAN



2701 SAN TOMAS EXPRESSWAY

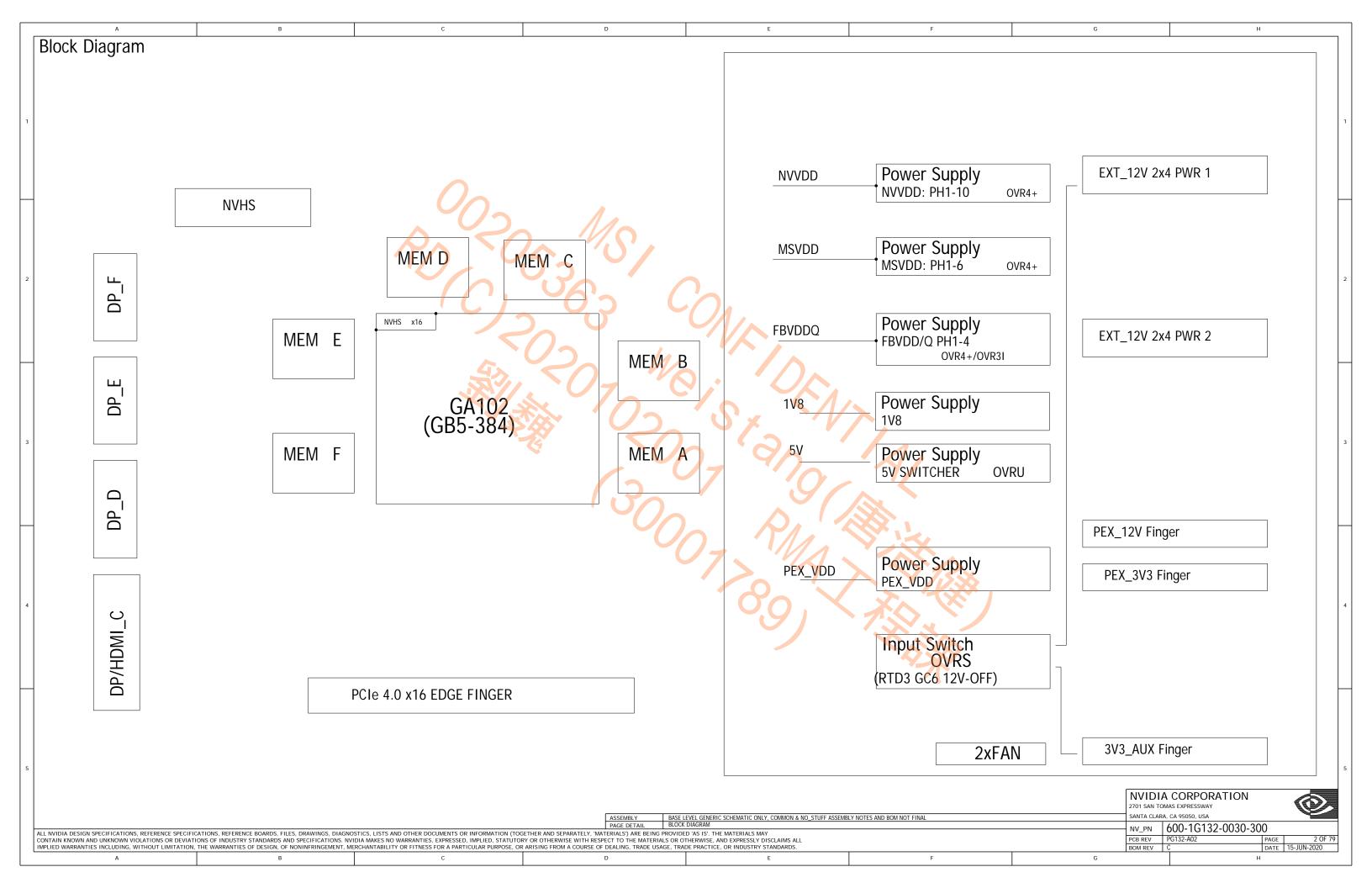
SANTA CLARA, CA 95050, USA

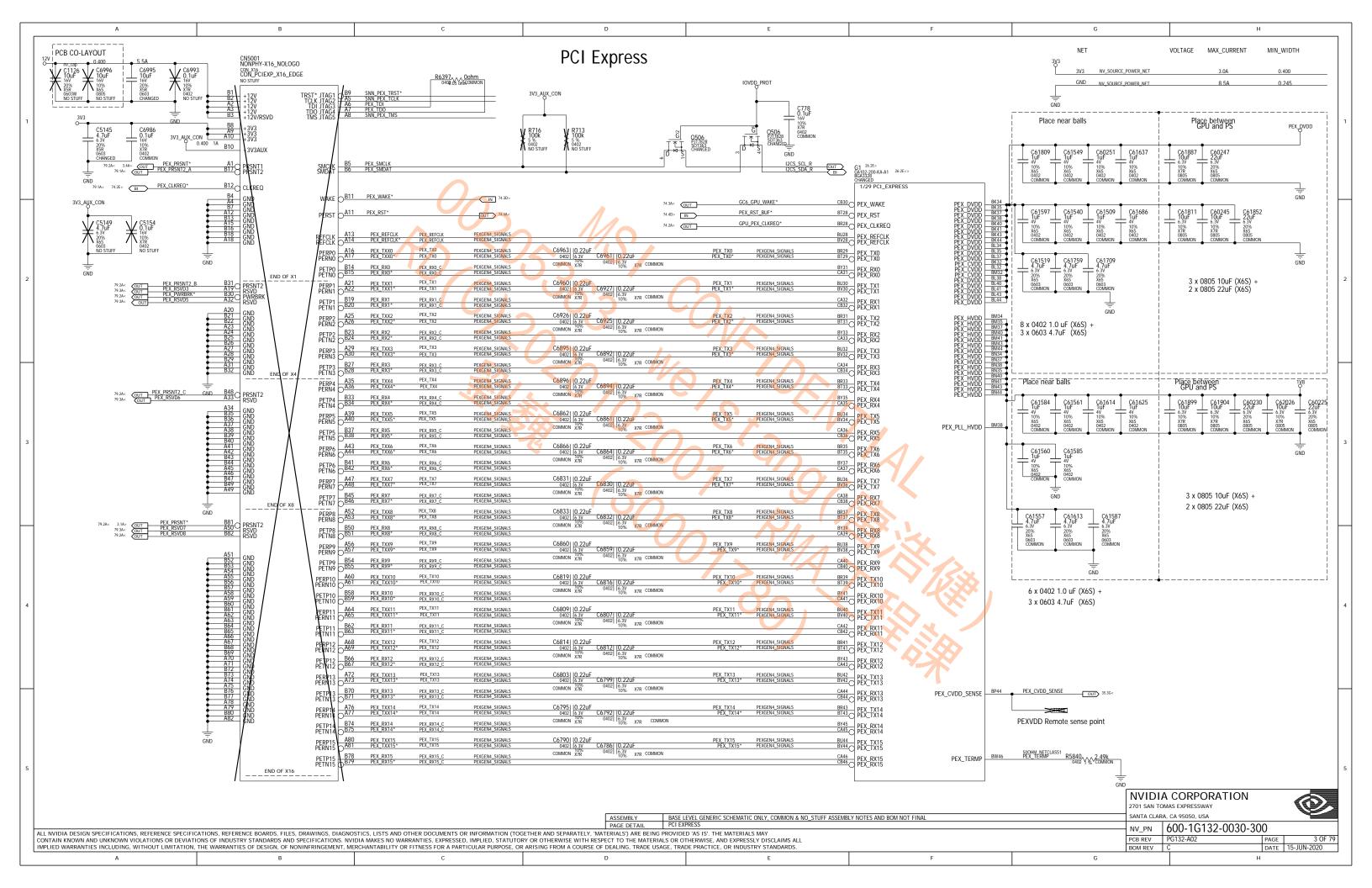
NV_PN 600-1G132-0030-300

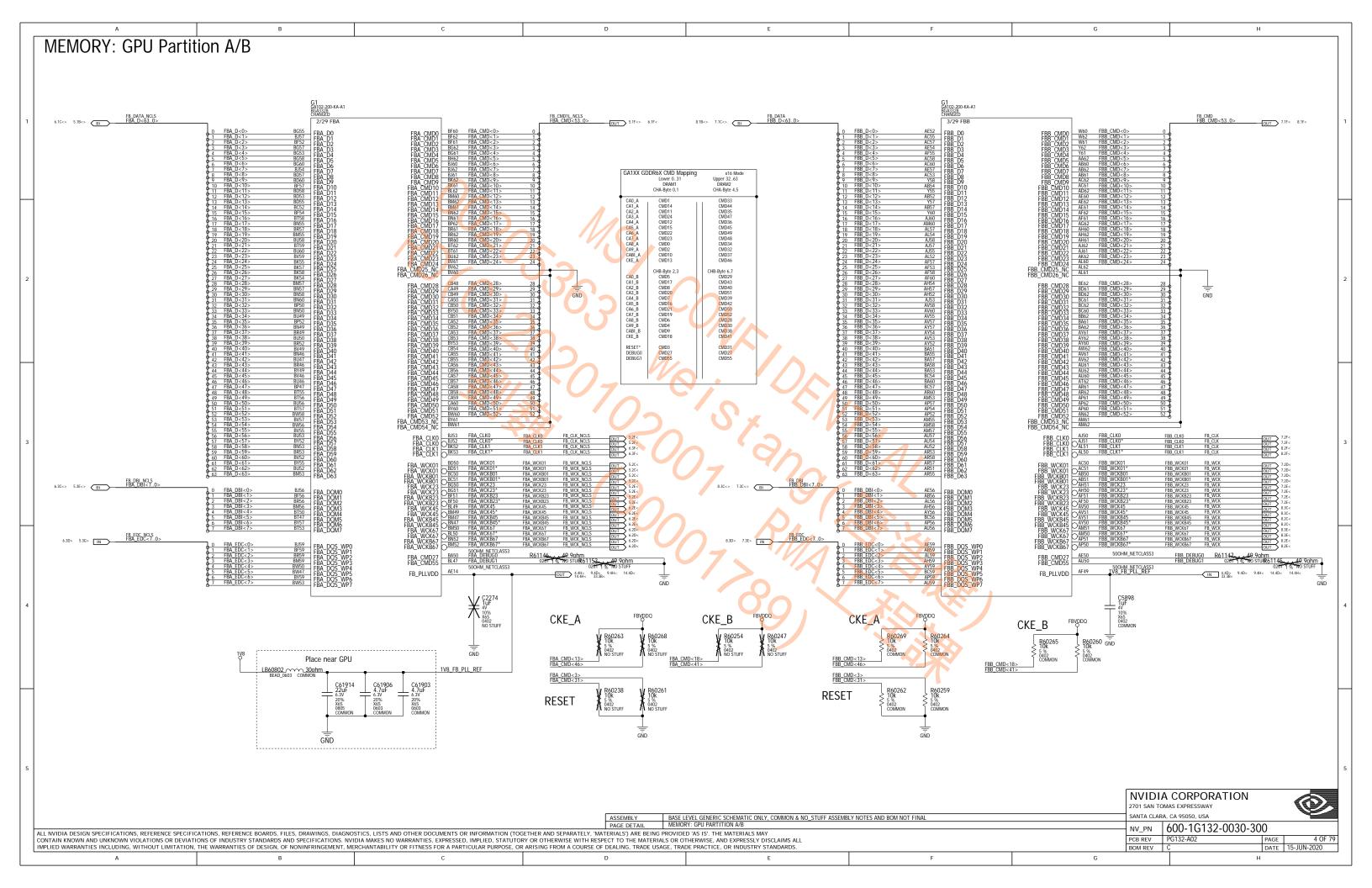
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

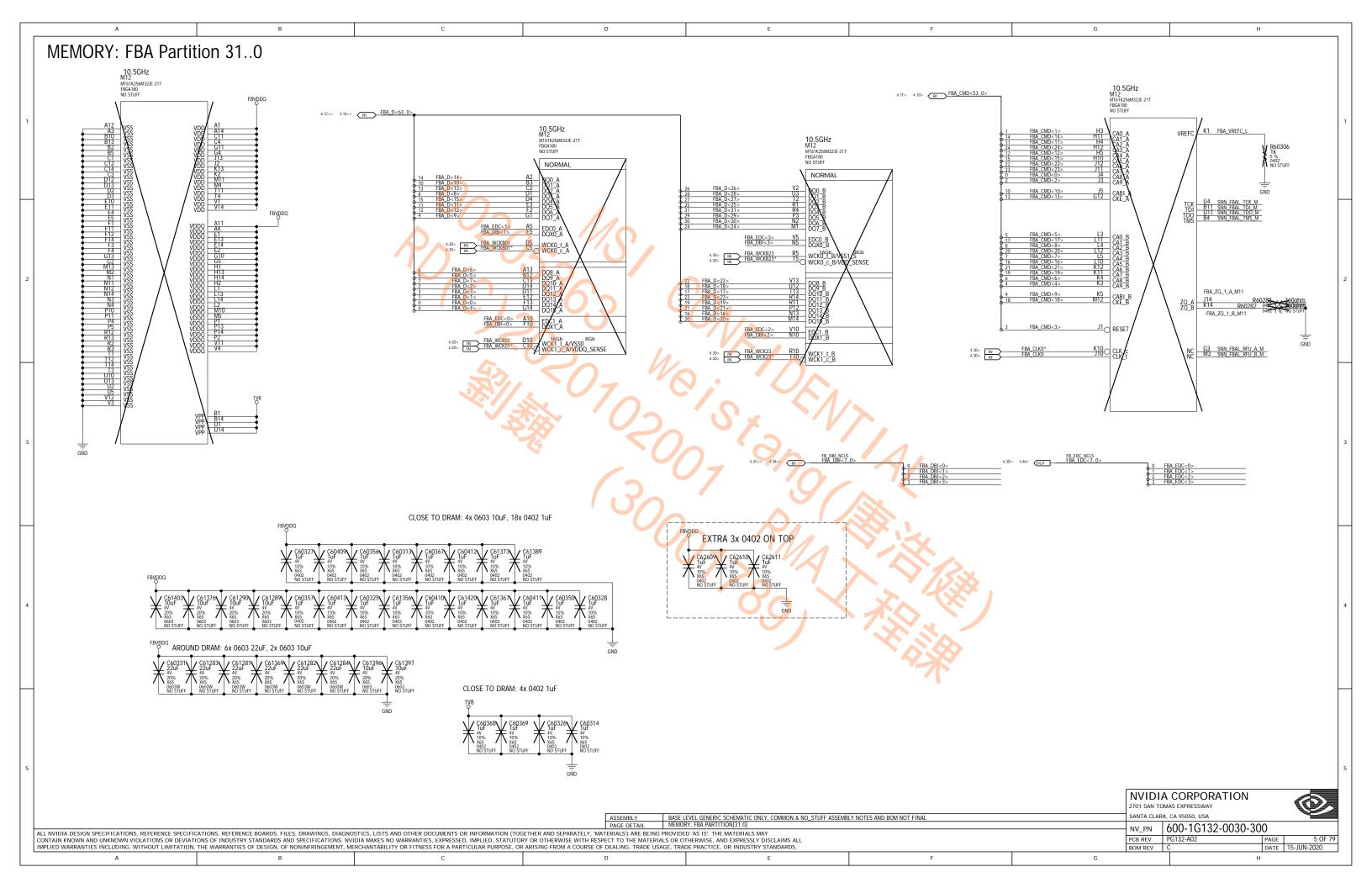
PCB REV PG132-A02
BOM REV C

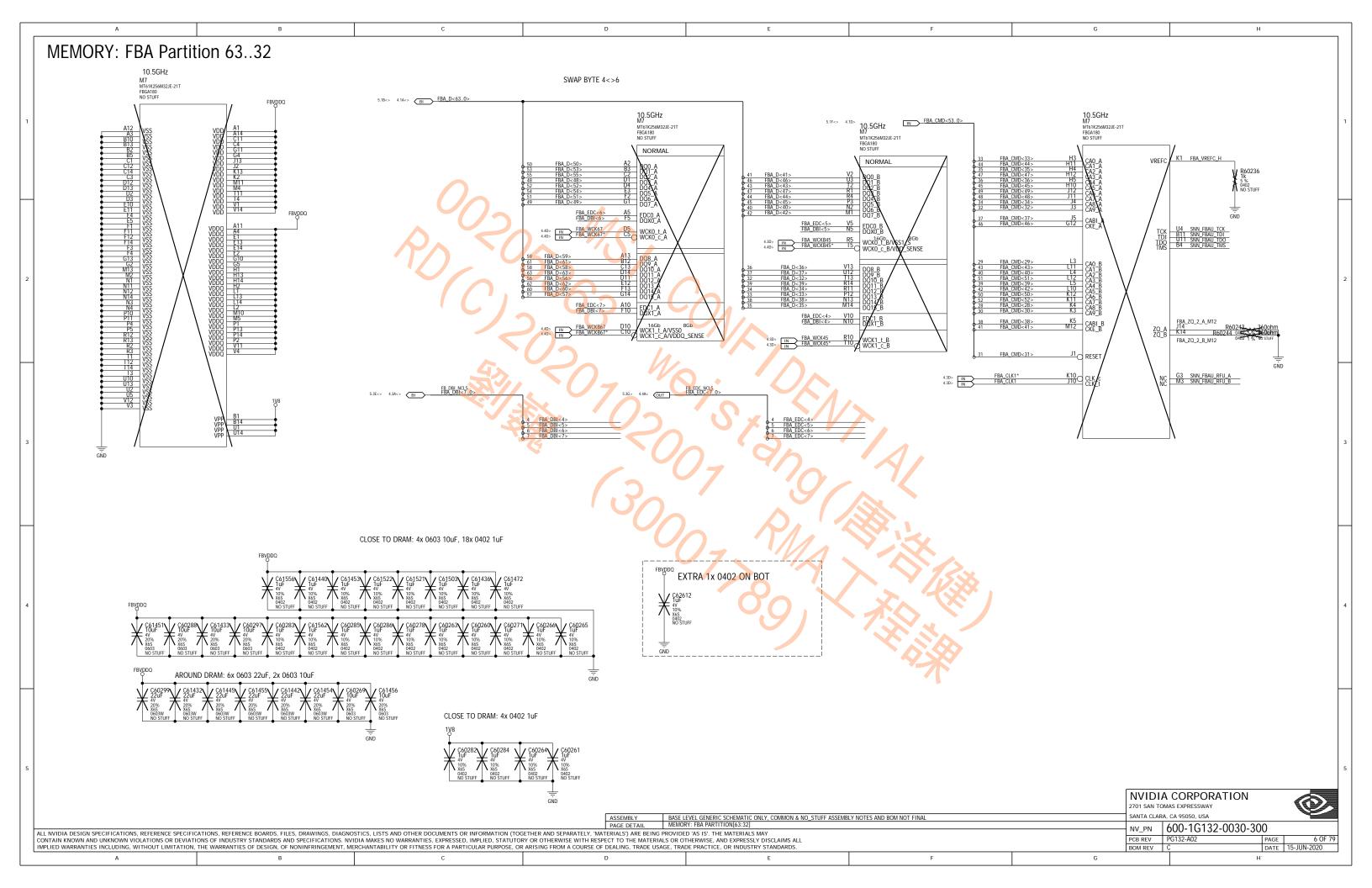
PAGE 1 OF 79
DATE 15-JUN-2020

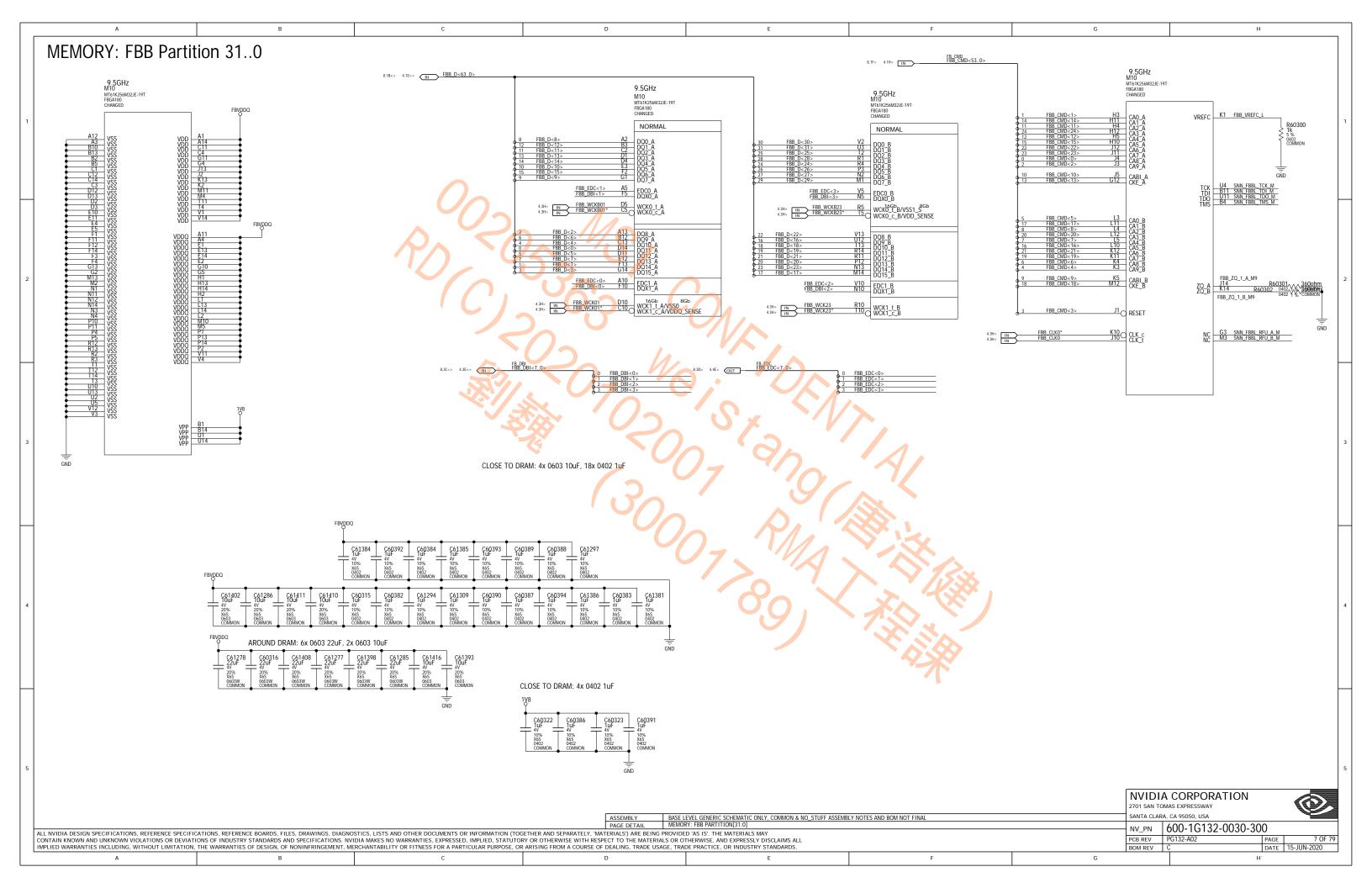


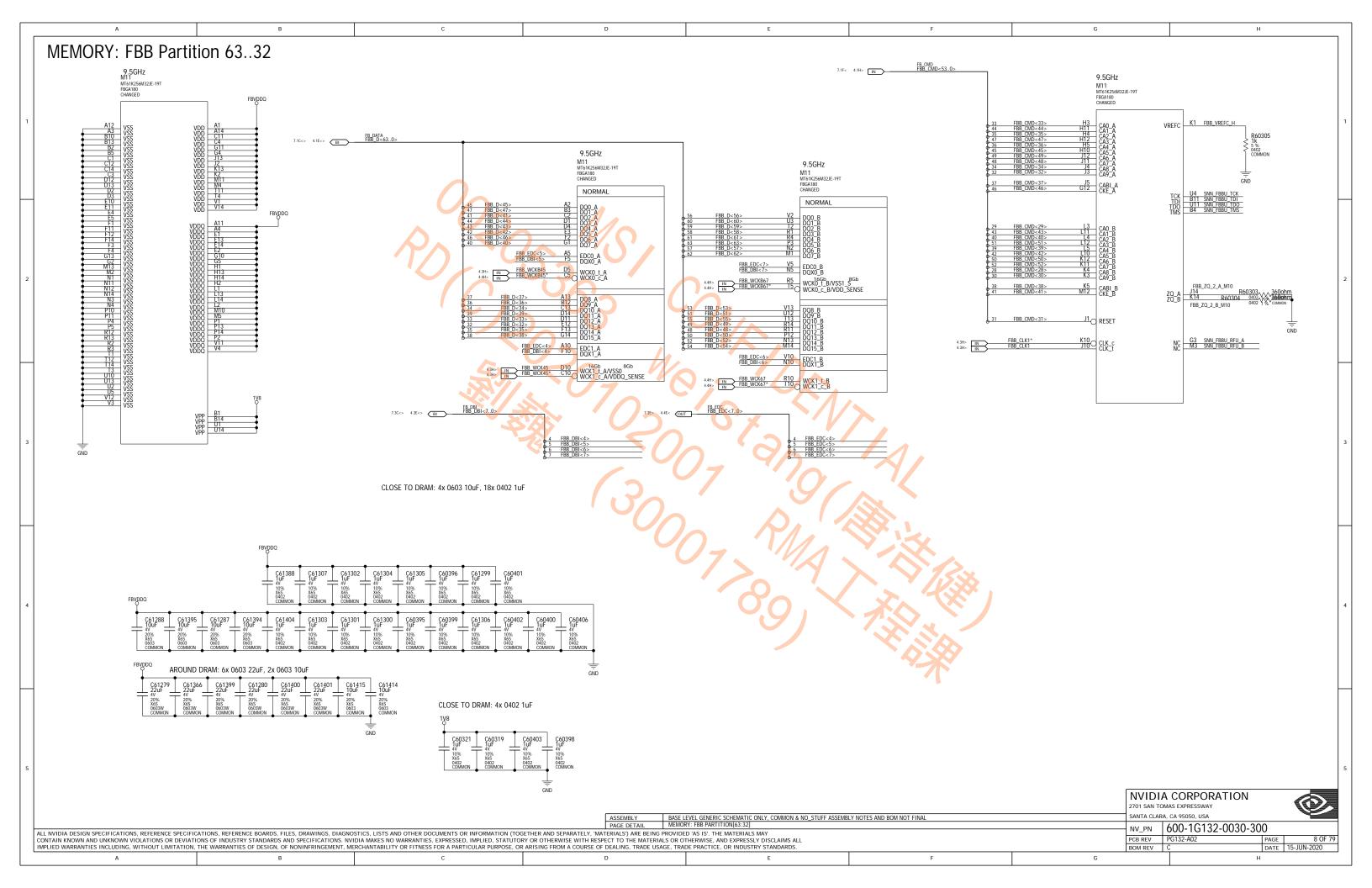


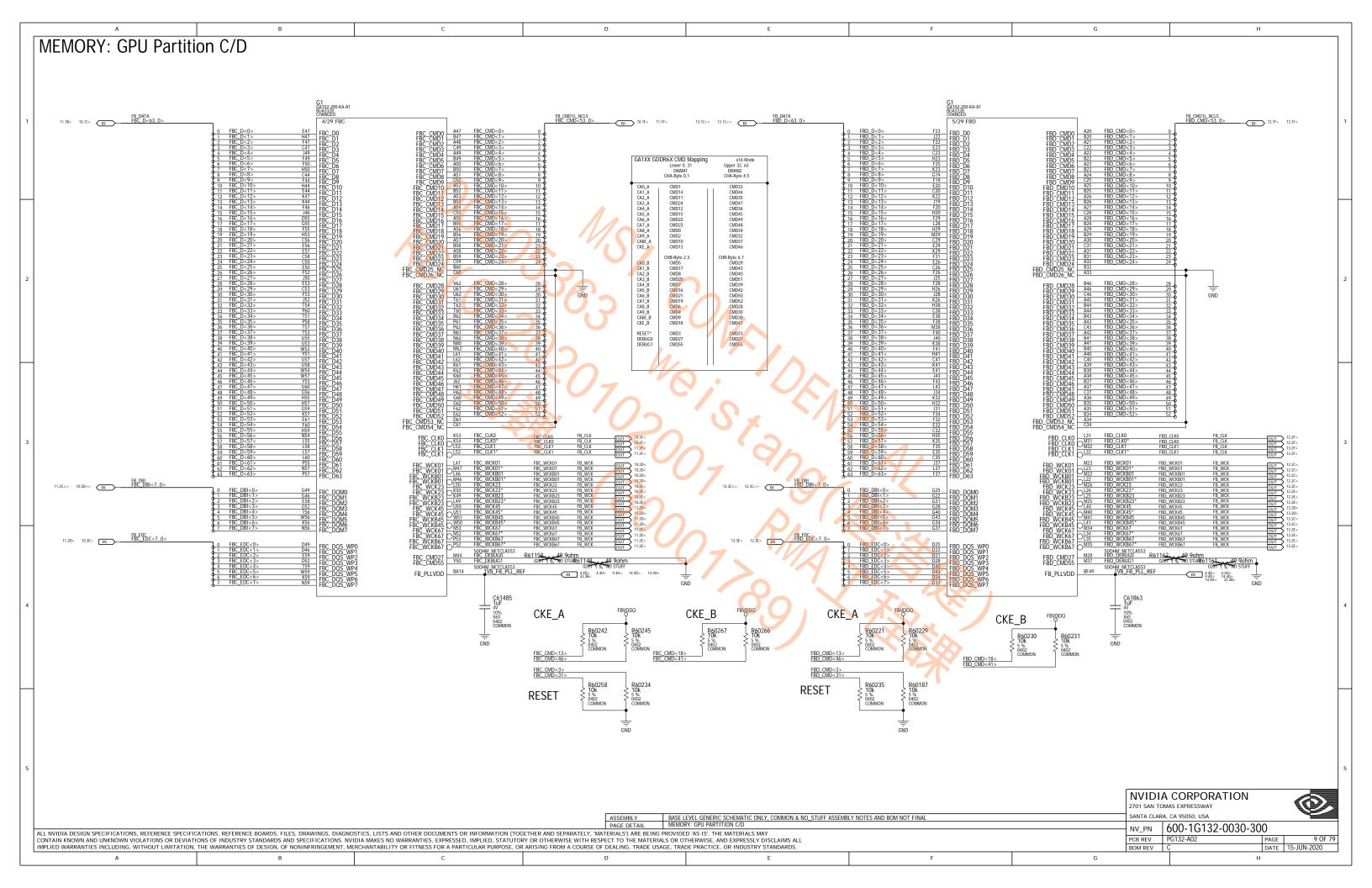


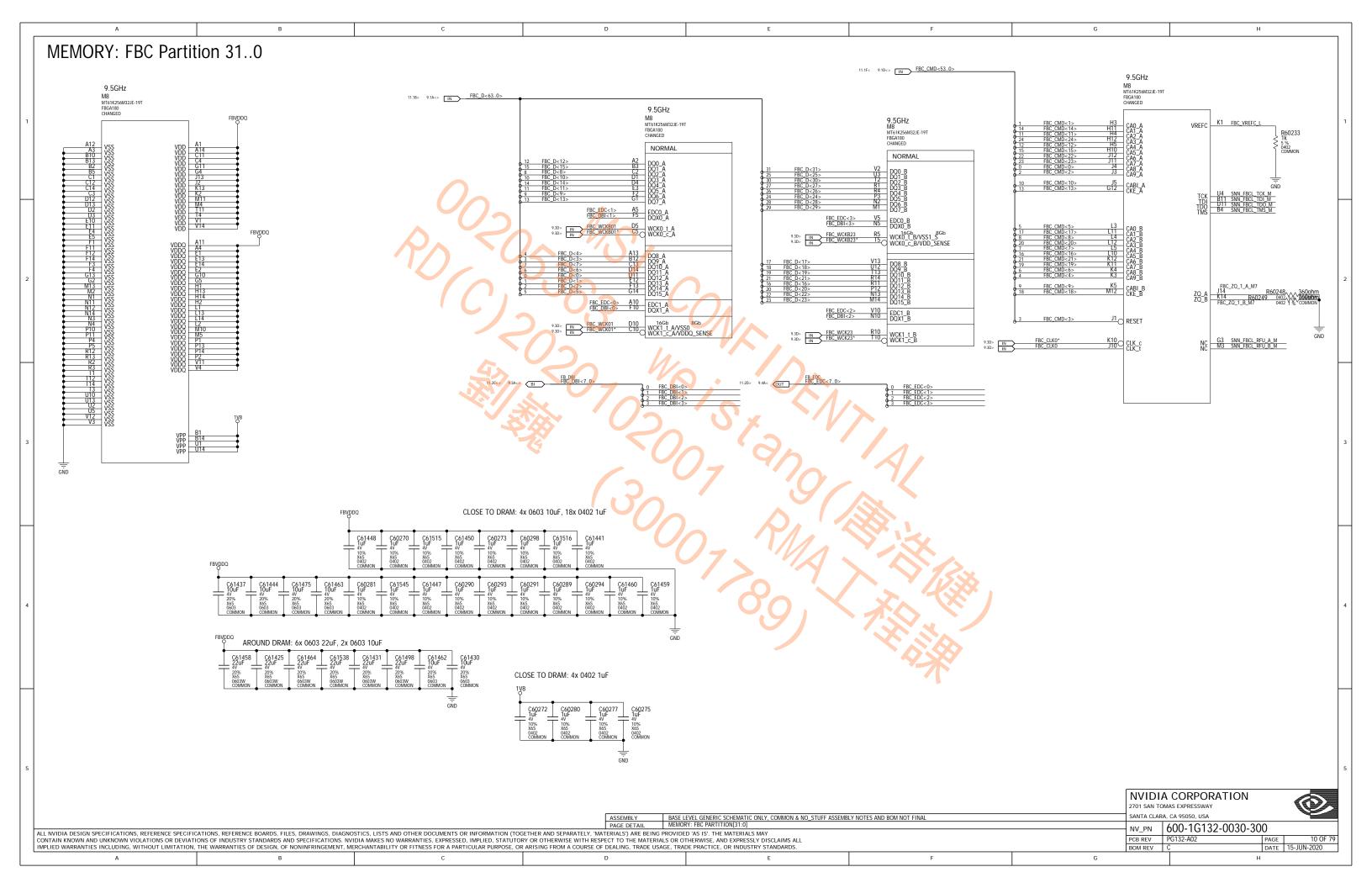


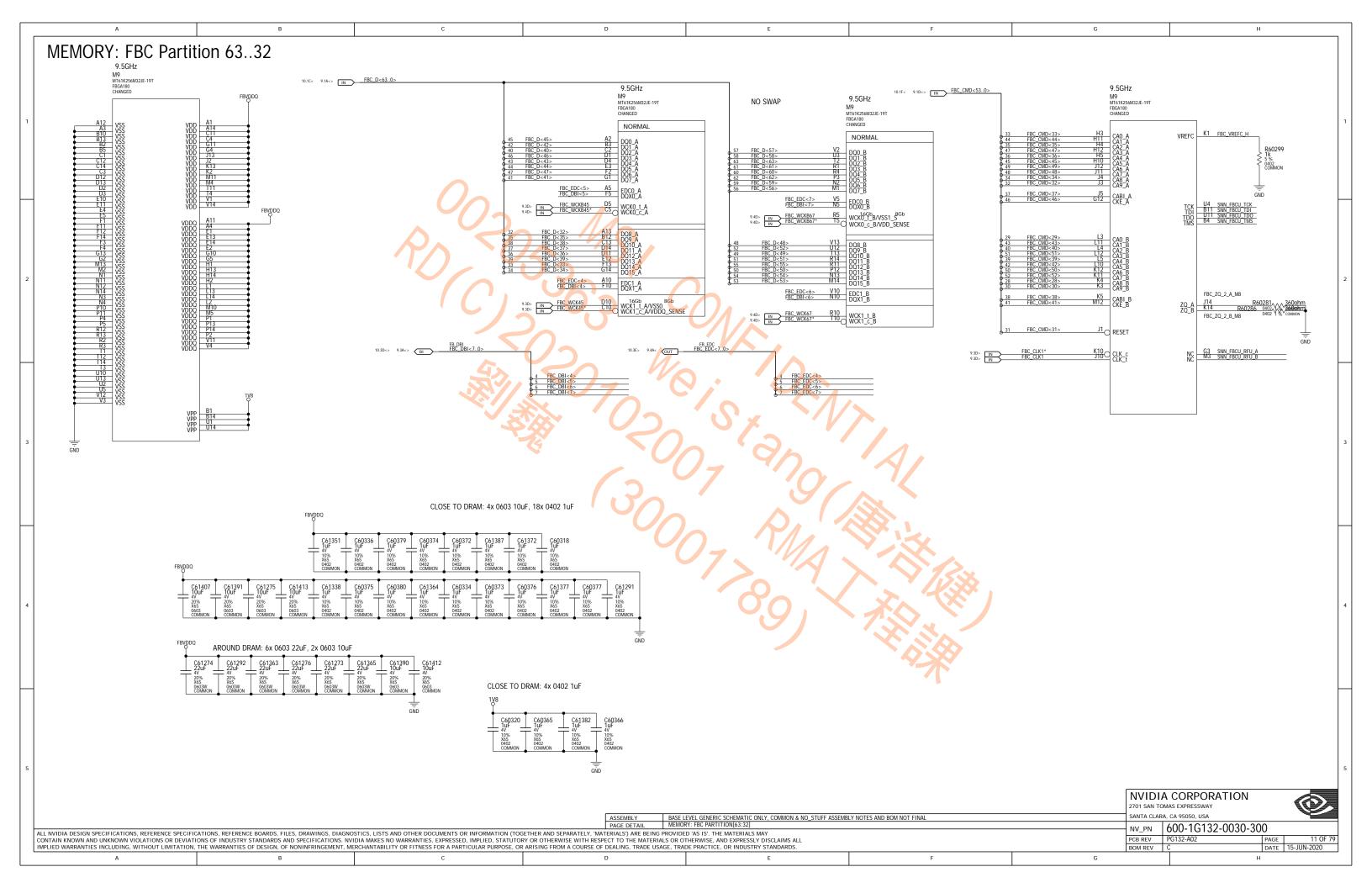


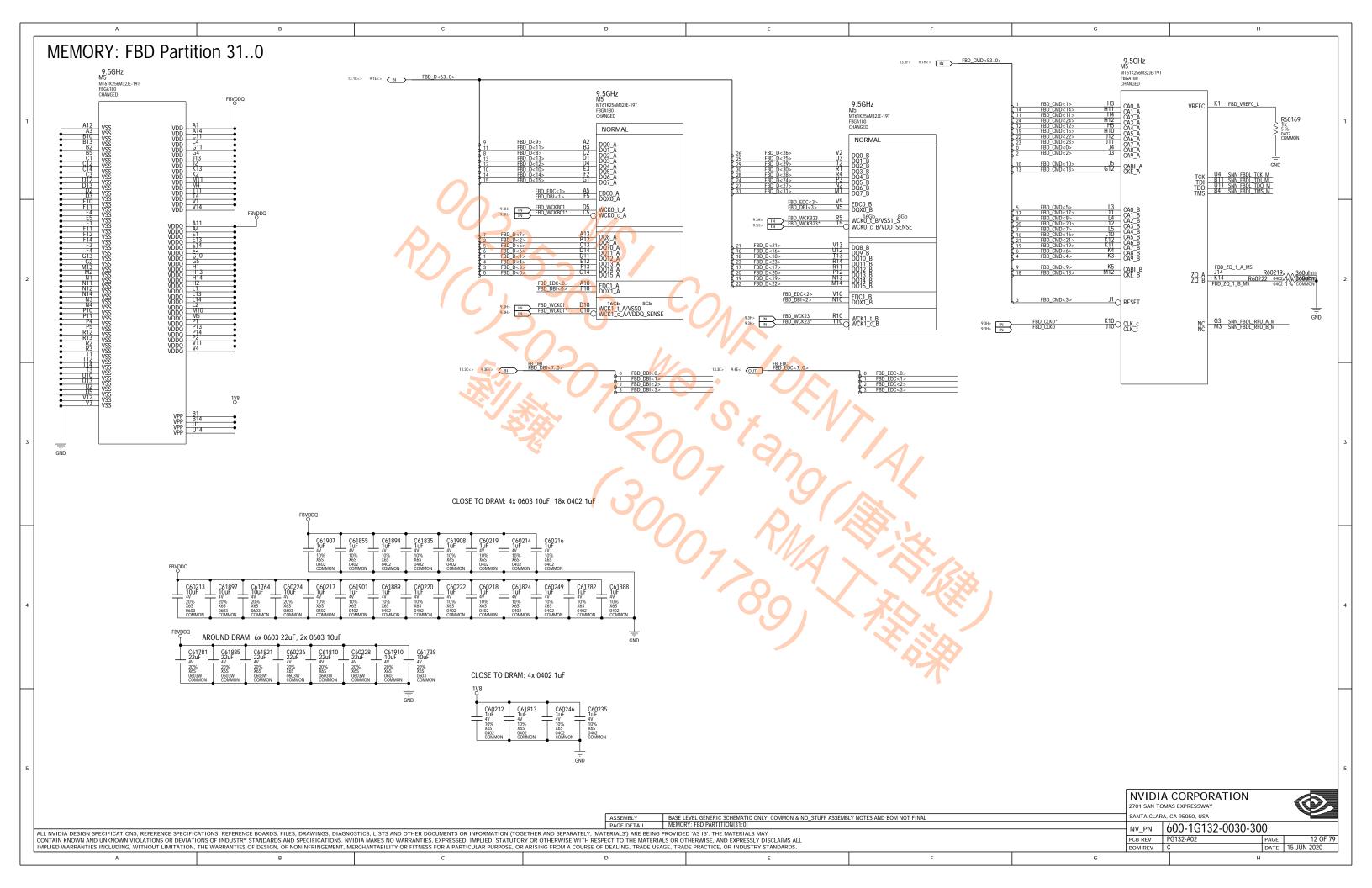


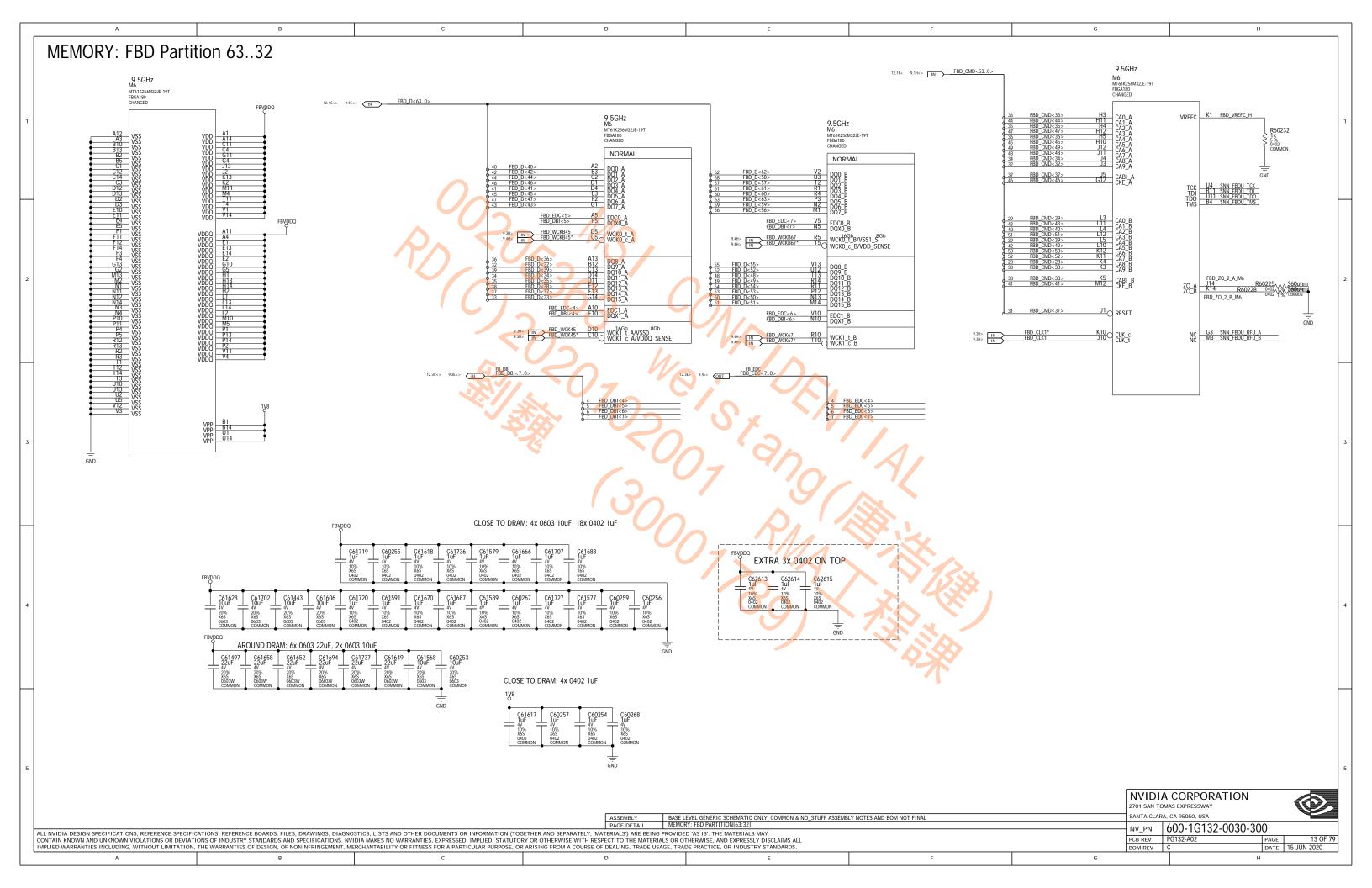


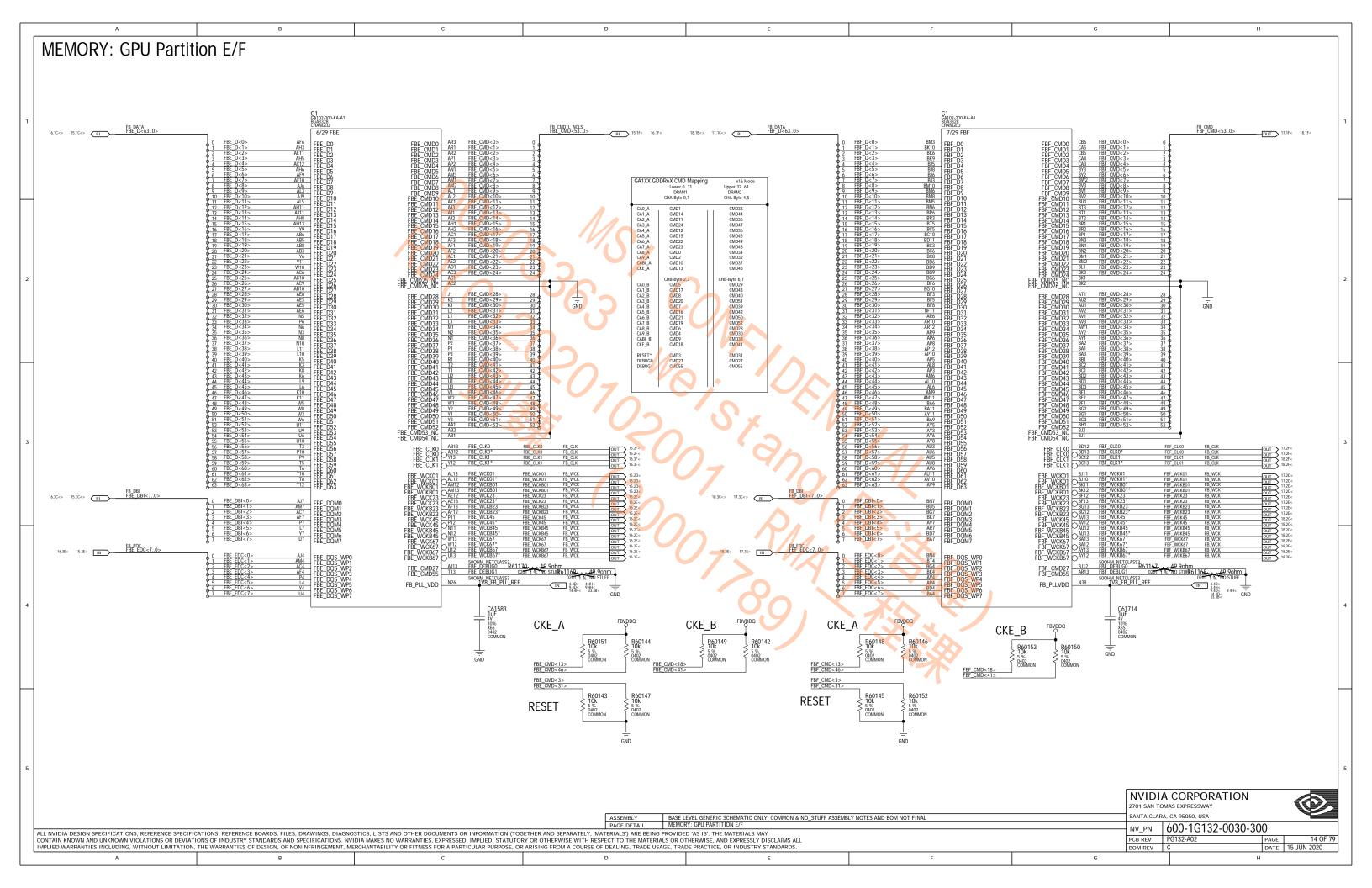


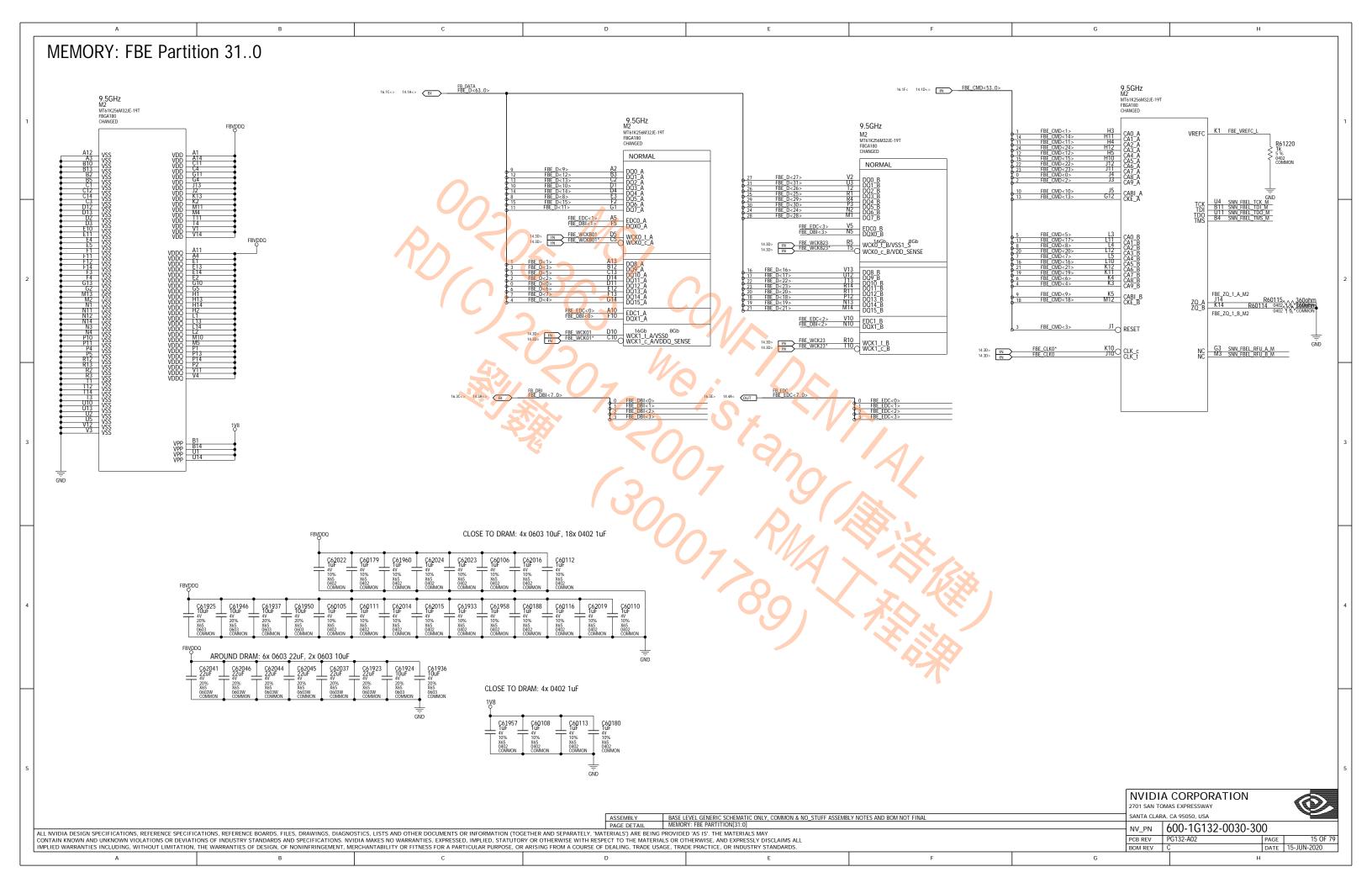


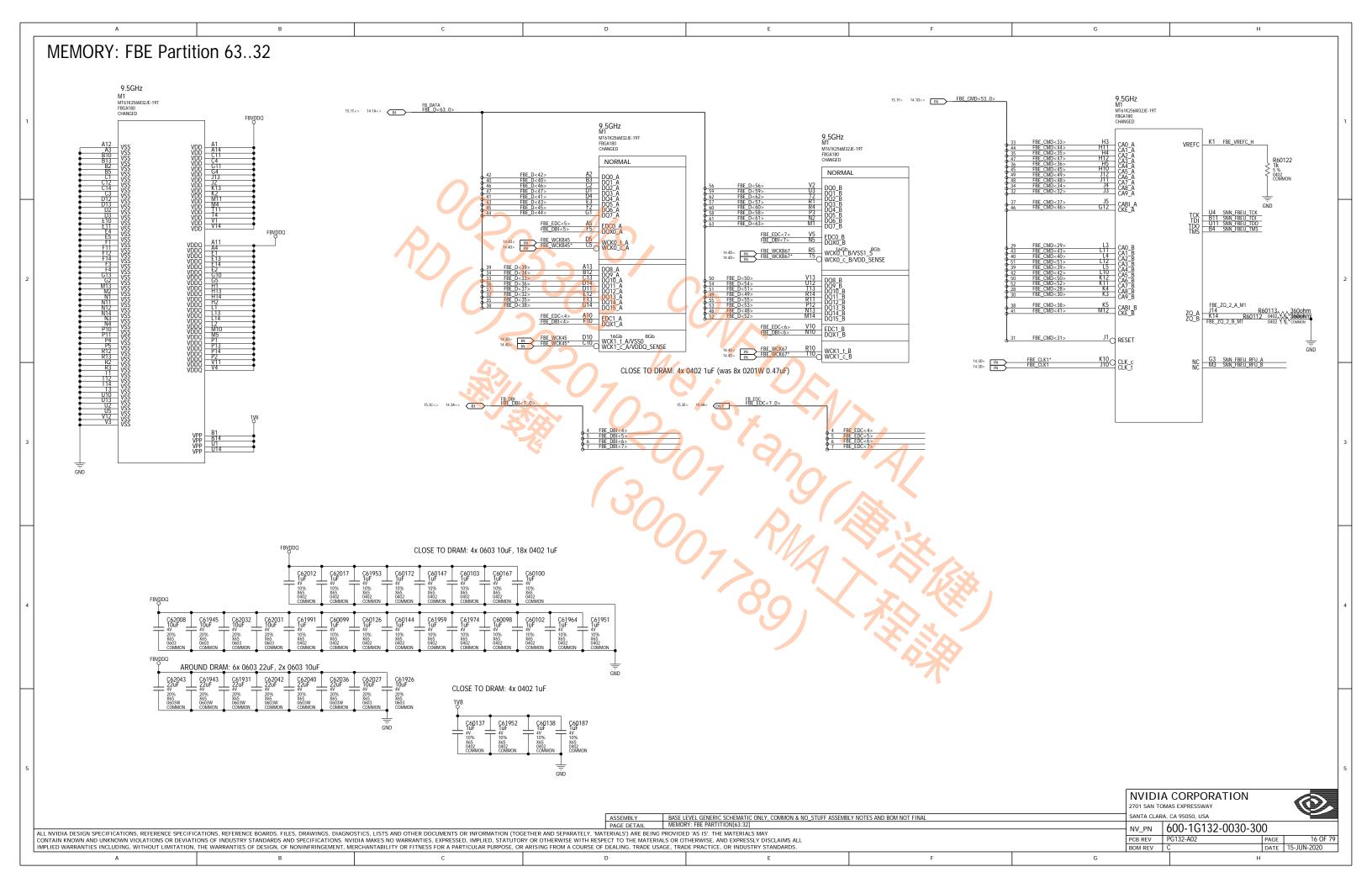


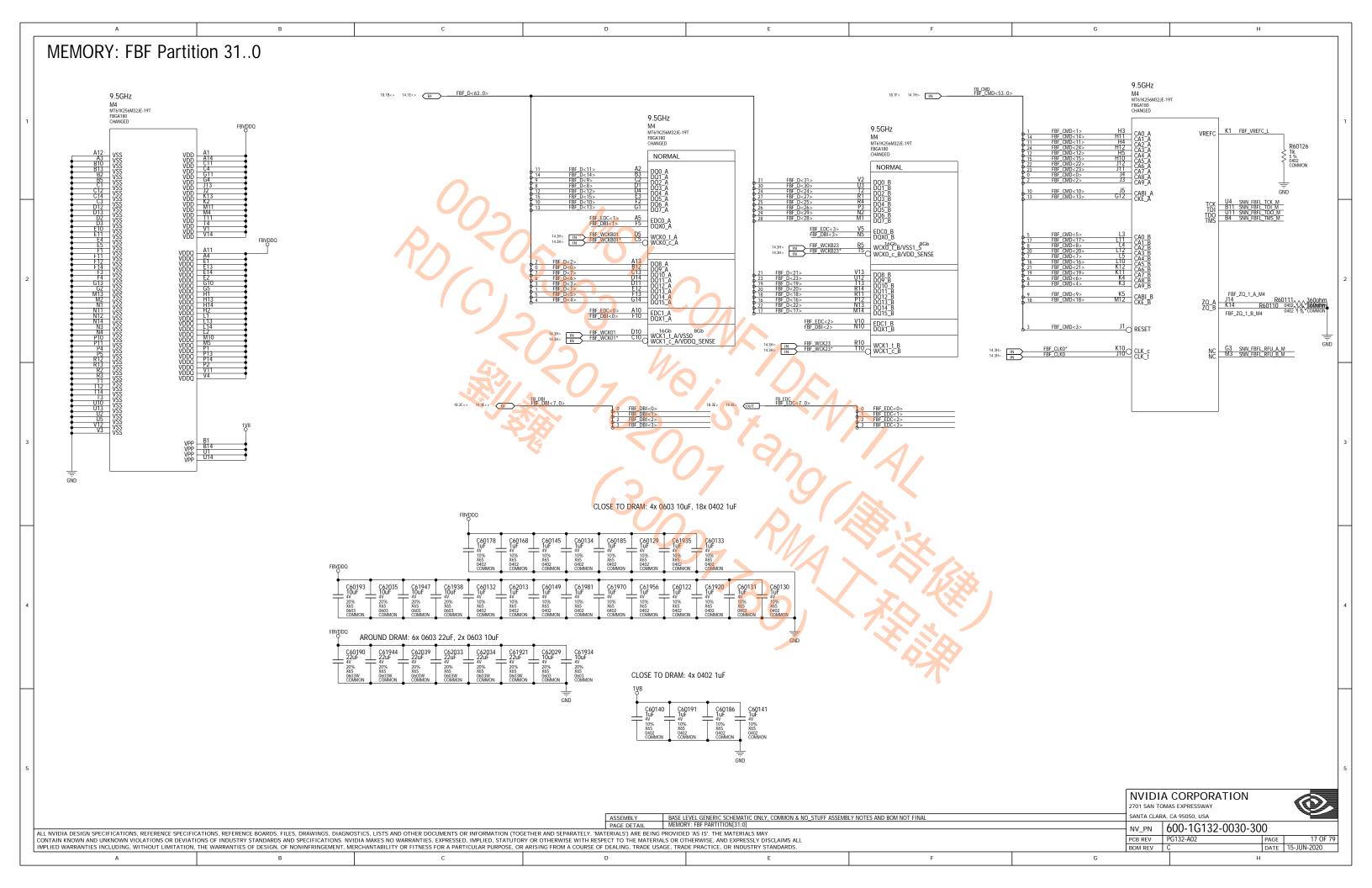


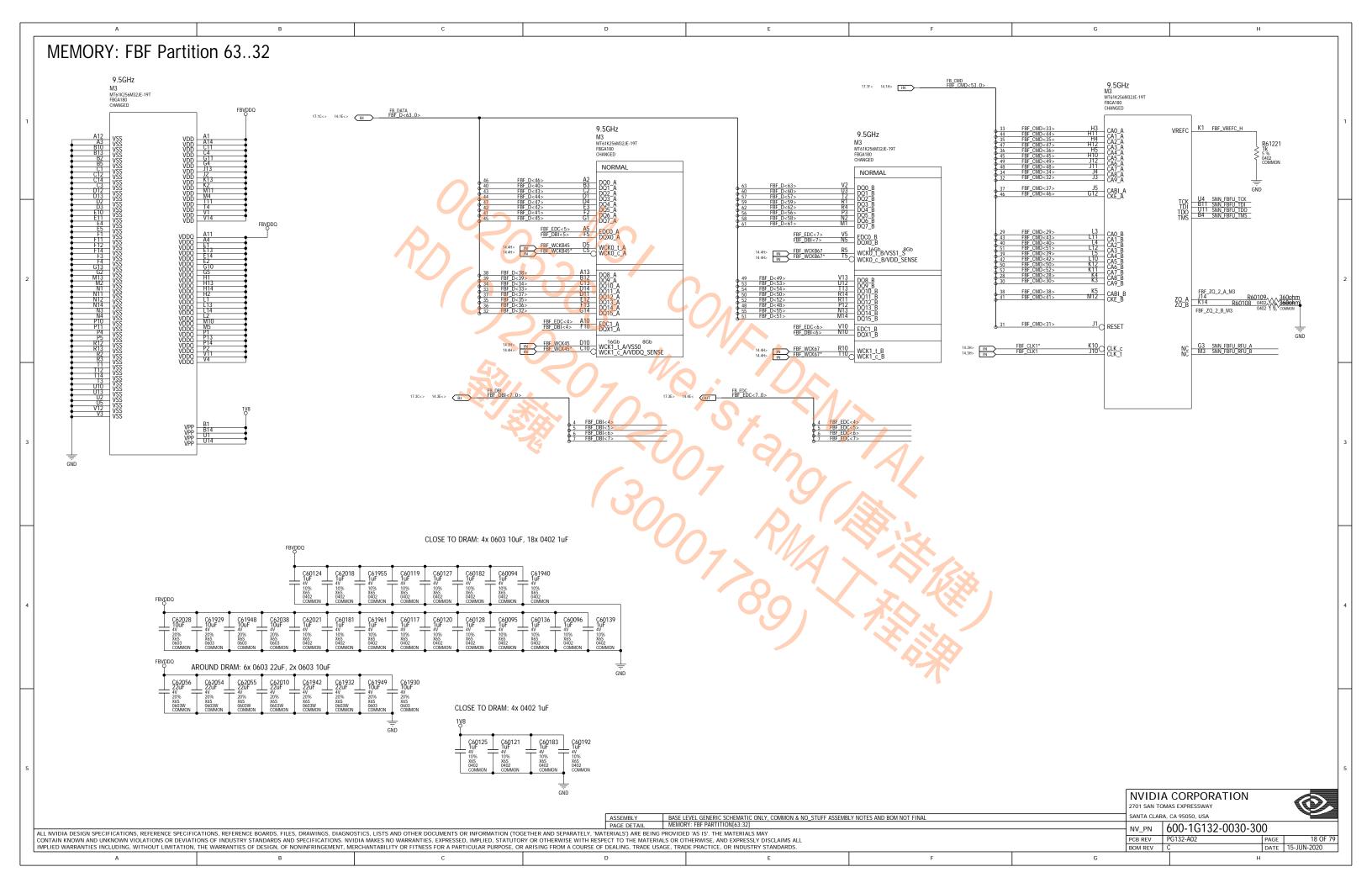


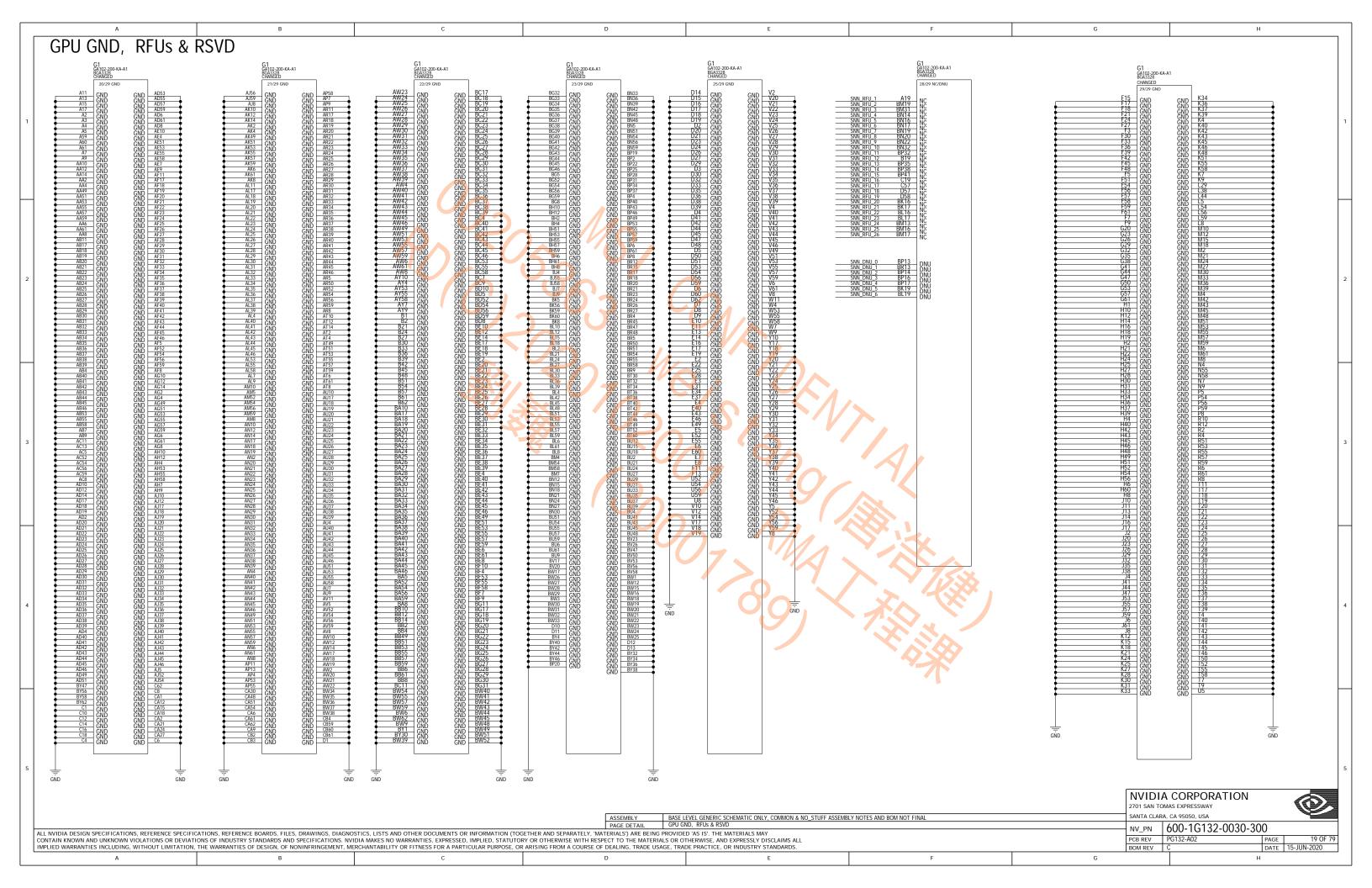


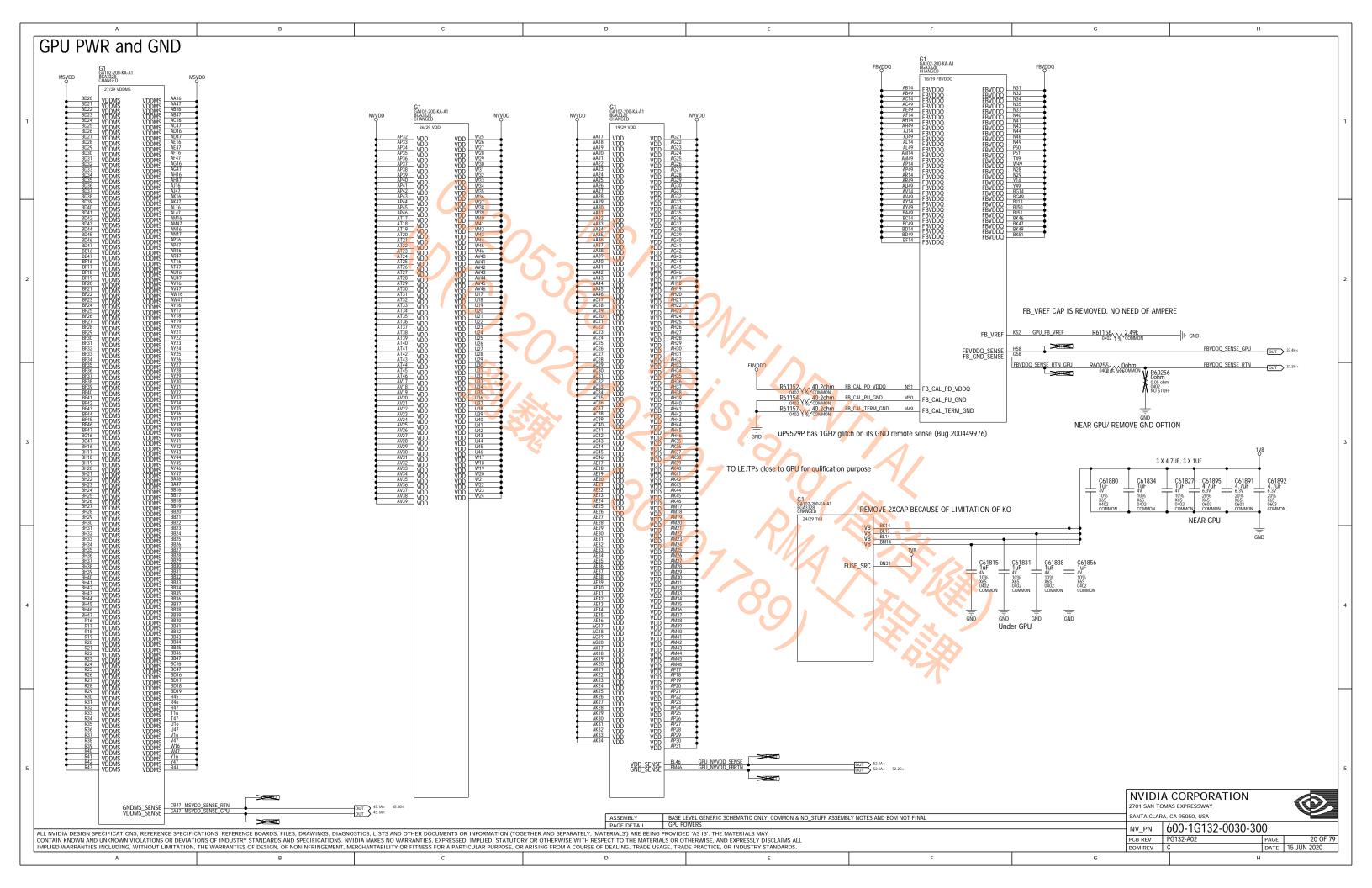


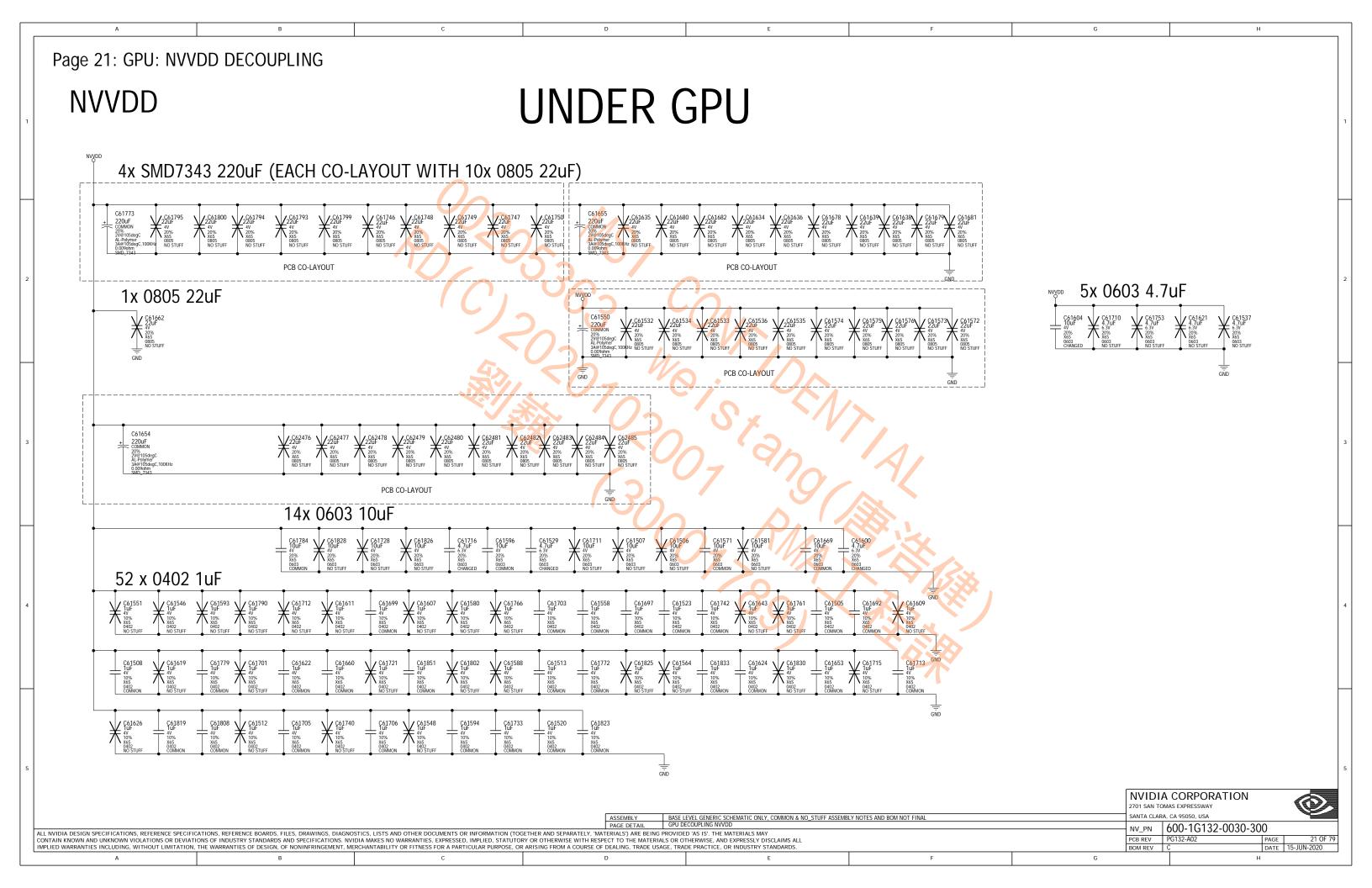








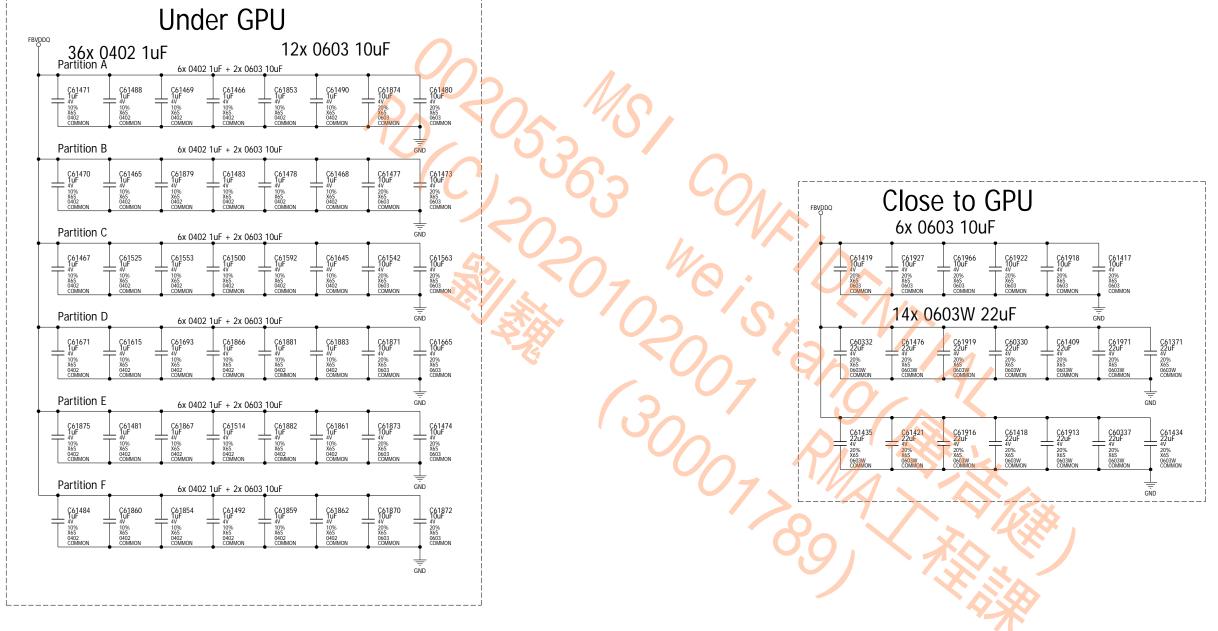




Page 22: GPU: FBVDD DECOUPLING

FBVDDQ

Under GPU



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV_PN 600-1G132-0030-300

PCB REV PG132-A02 PAGE 22 0F 79

BOM REV C DATE 15-JUN-2020

