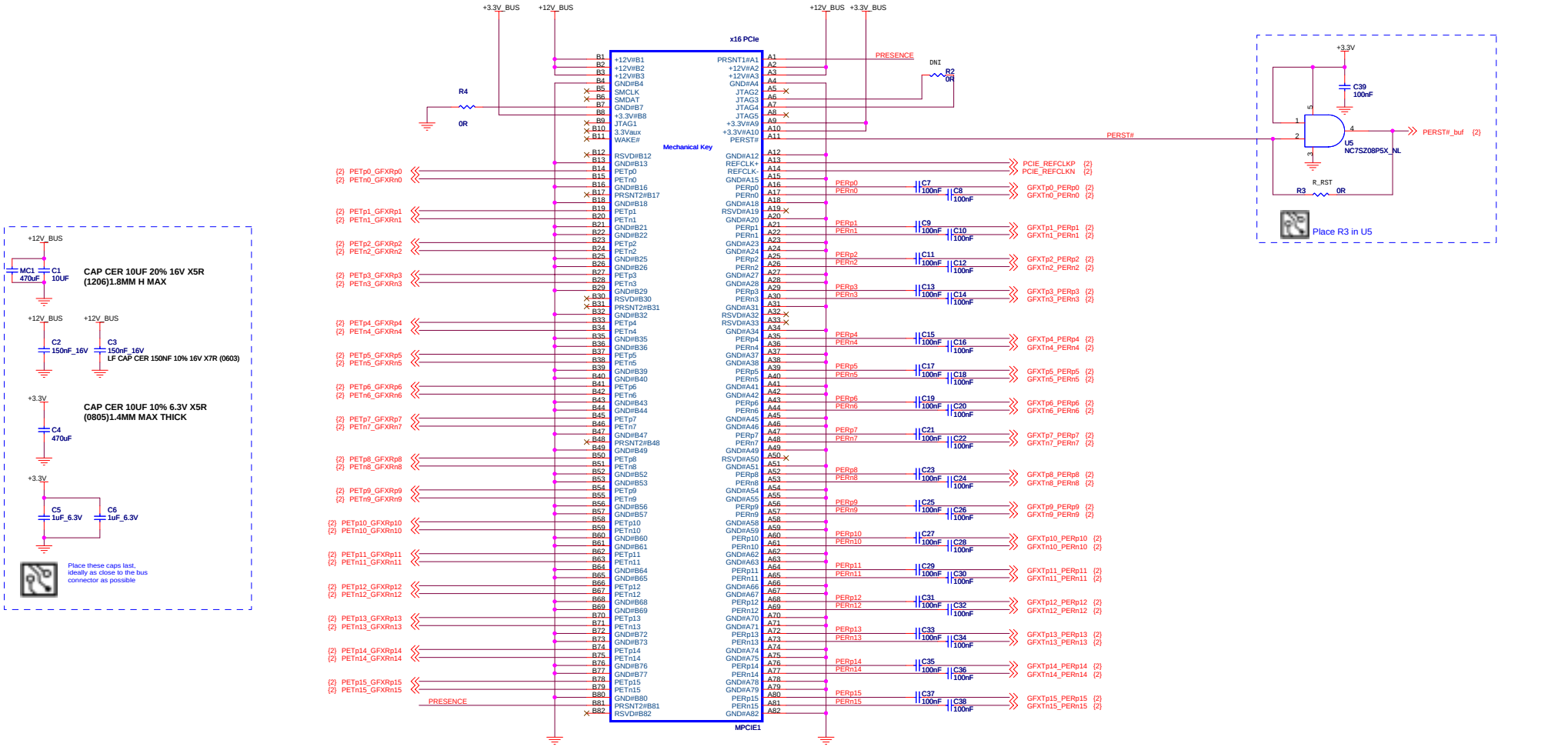
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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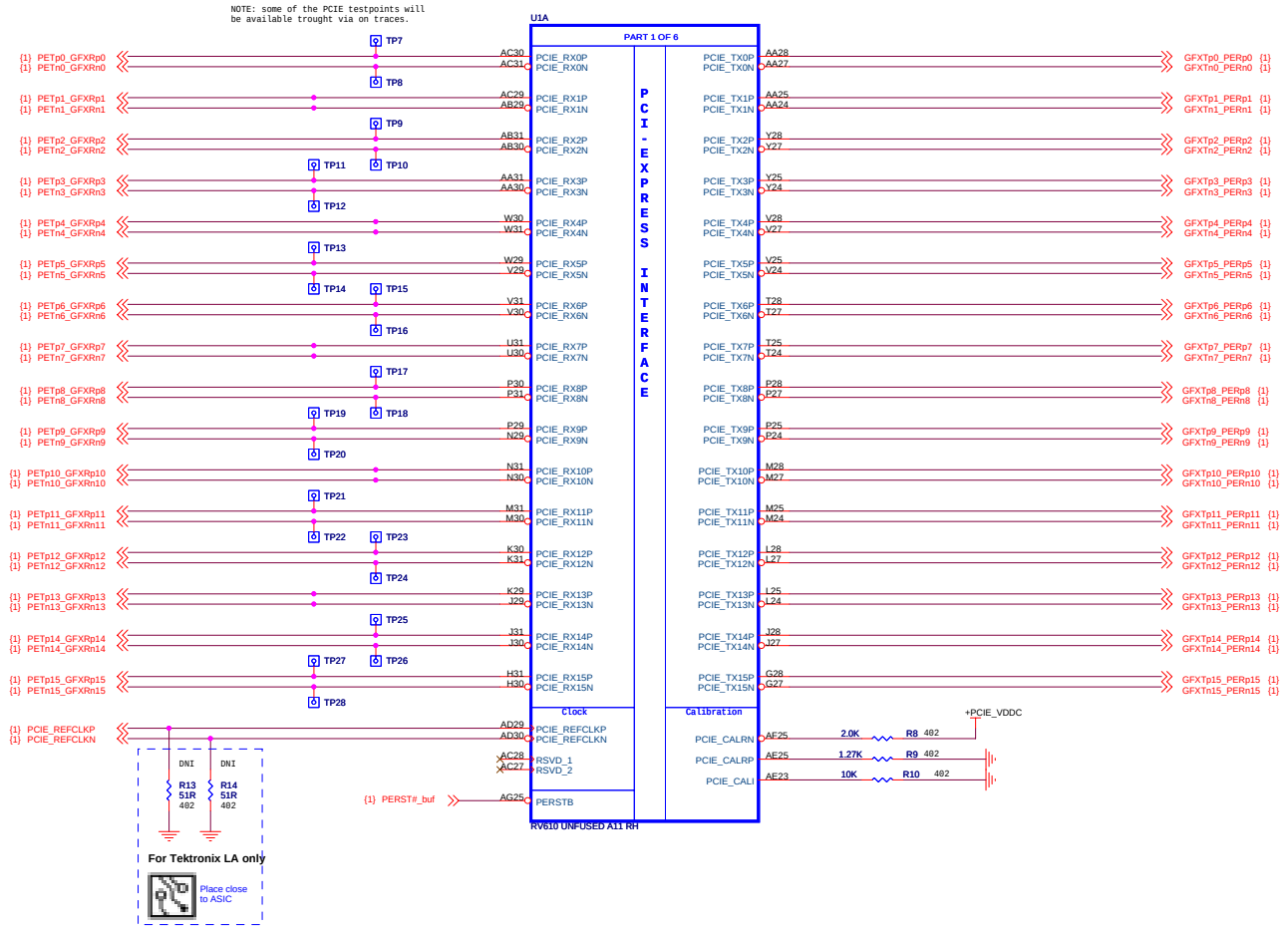
Size C	Document Number 105-B169xx-00A		Rev 32
Date: Wednesday, April 23, 2008		Sheet 1 of 19	



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Title	RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI		
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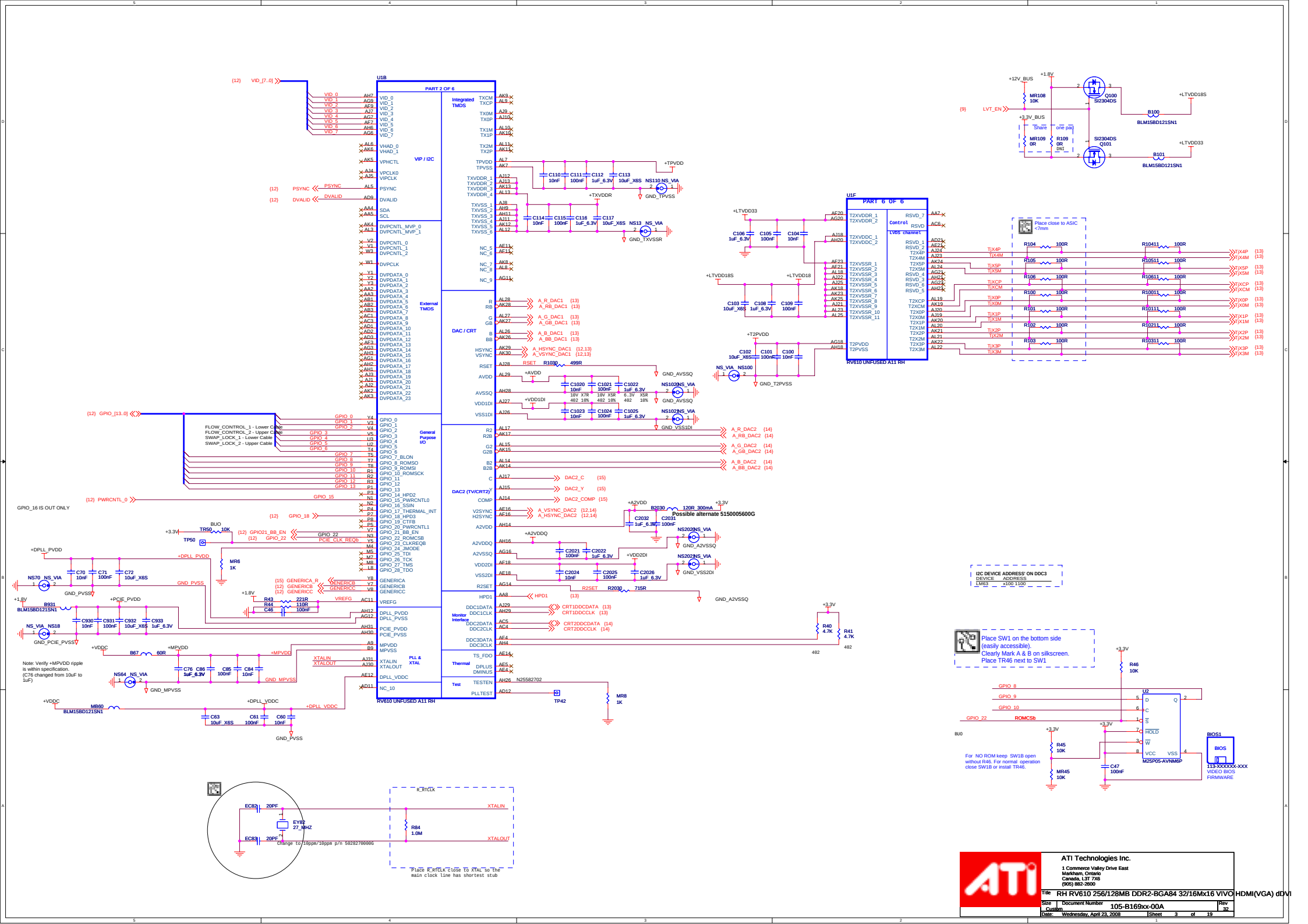
U1B
PART 2 OF 6
RV610 UNFUSED A11 RH
U1F
PART 6 OF 6
RV610 UNFUSED A11 RH
Integrated TMDS
VIP / I2C
External TMDS
DAC / CRT
General Purpose I/O
DAC2 (TV/CRT2)
Monitor Interface
Thermal
Test
PLL & XTAL
Control
LVDS channel
FLOW_CONTROL_1 - Lower Cable
FLOW_CONTROL_2 - Upper Cable
SWAP_LOCK_1 - Lower Cable
SWAP_LOCK_2 - Upper Cable
GPIO_16 IS OUT ONLY
Note: Verify +MPVDD ripple is within specification. (C76 changed from 10uF to 1uF)
Possible alternate 5150005600G
I2C DEVICE ADDRESS' ON DDC3
DEVICE ADDRESS
LM63 x100 1100
Place SW1 on the bottom side (easily accessible). Clearly Mark A & B on silkscreen. Place TR46 next to SW1
For NO ROM keep SW1B open without R46. For normal operation close SW1B or install TR46.
Place close to ASIC <7mm
Place R_RTCLK close to XTAL so the main clock line has shortest stub
Change to 10ppm/10ppm p/n 502827000G
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Size: Custom
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Date: Wednesday, April 23, 2008
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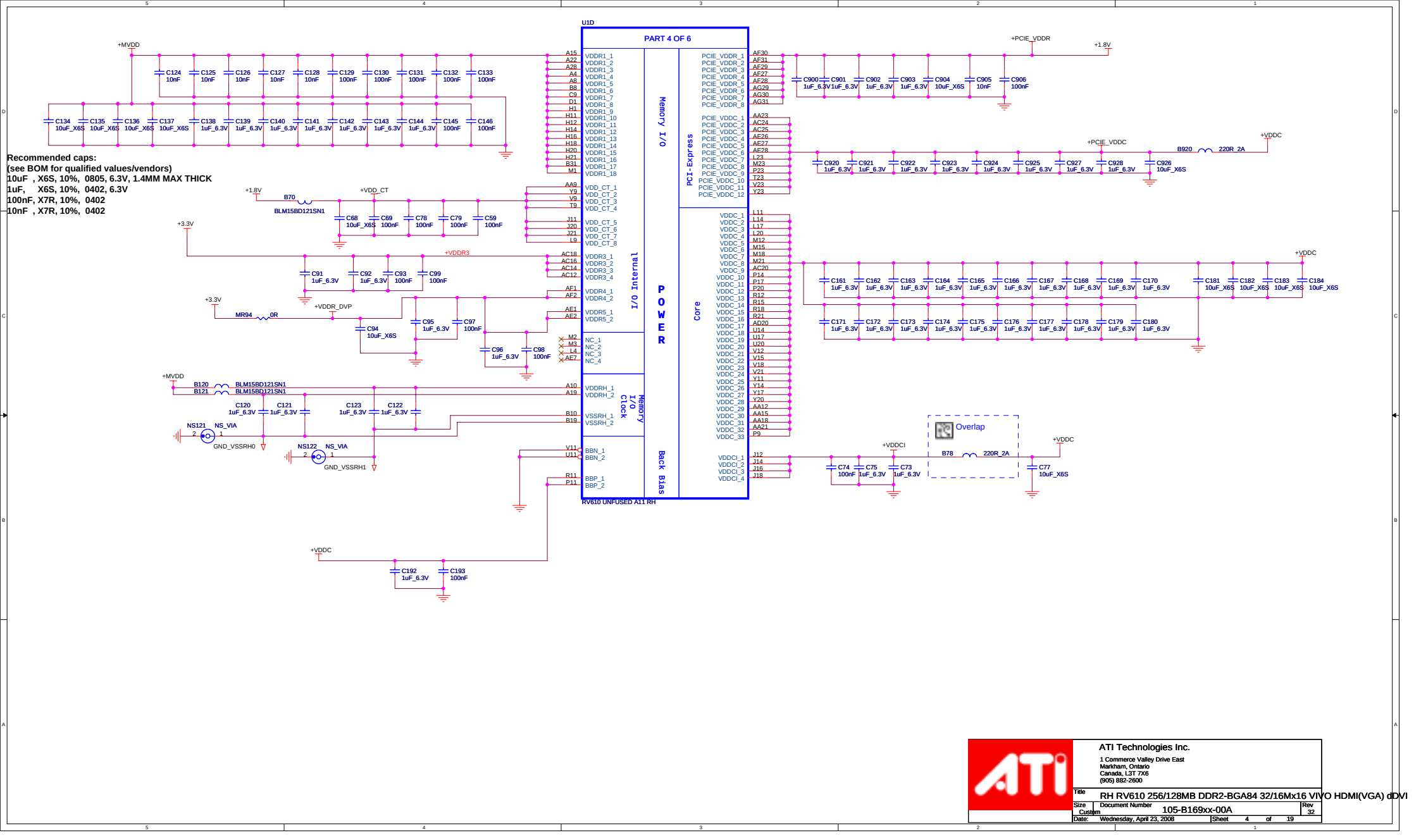

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Title	RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI		
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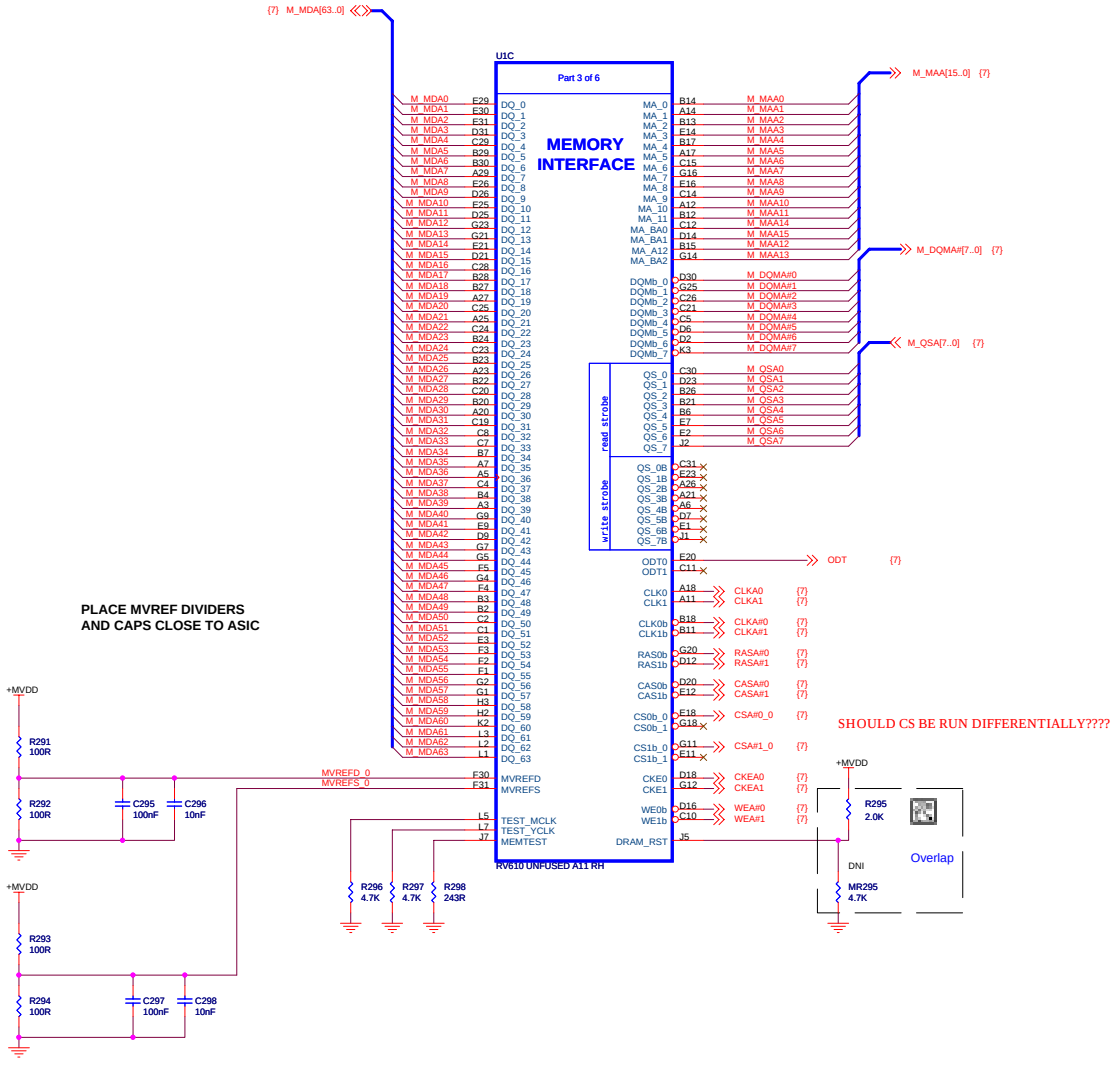

DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

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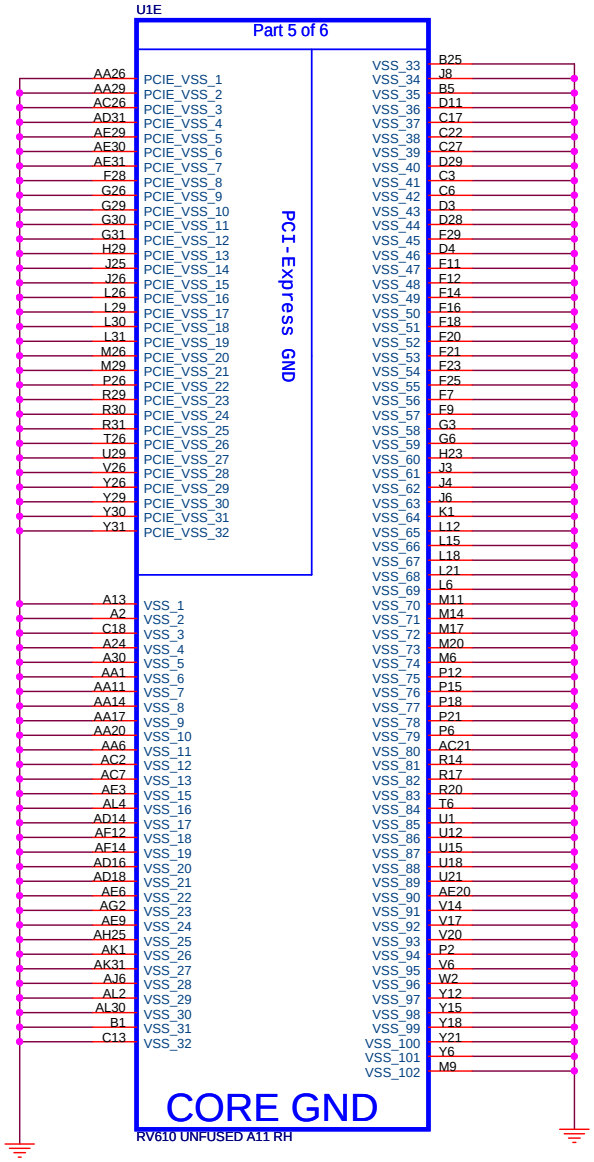

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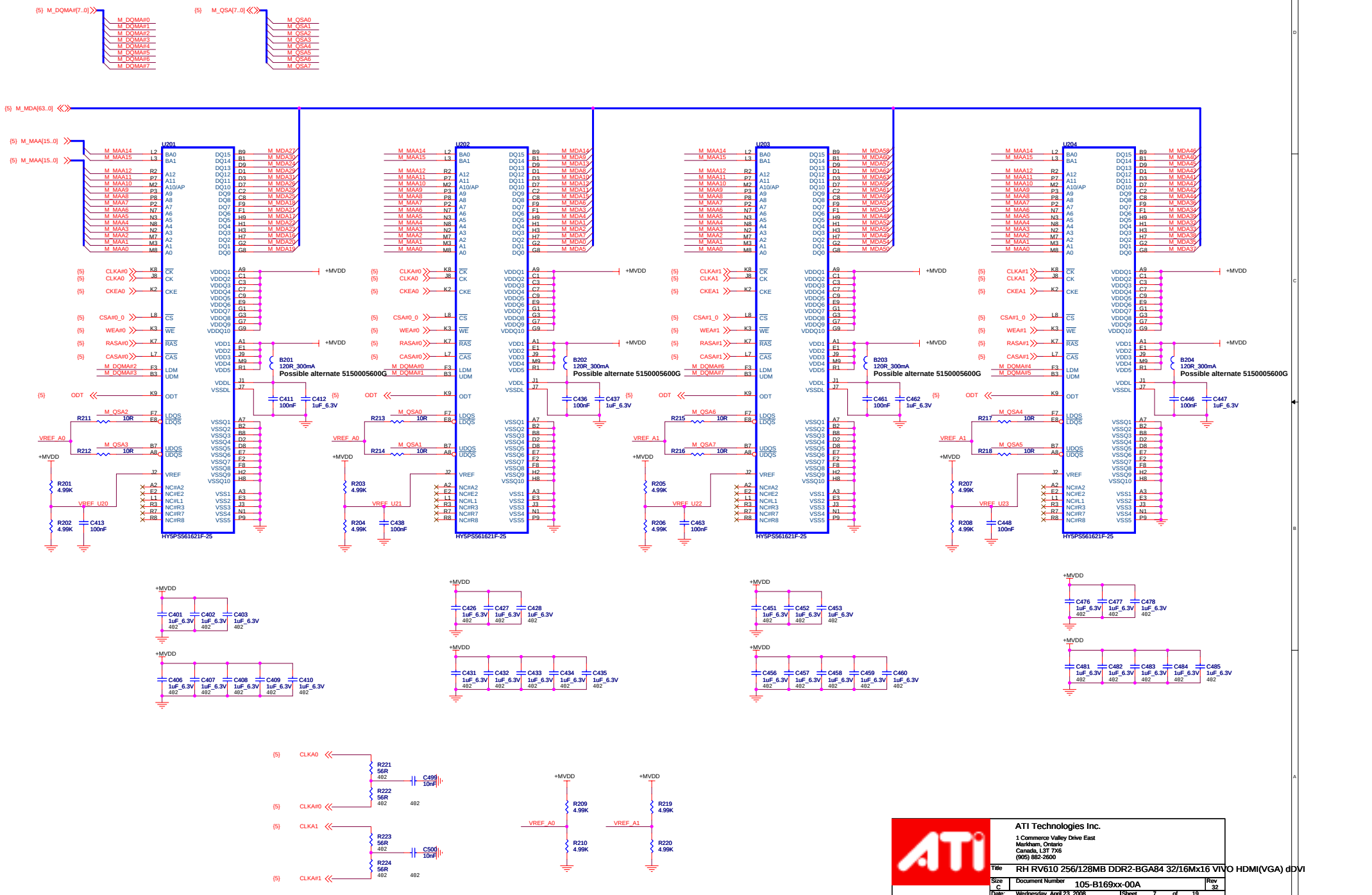
CHANNEL A: RANK 0 128MB DDR2



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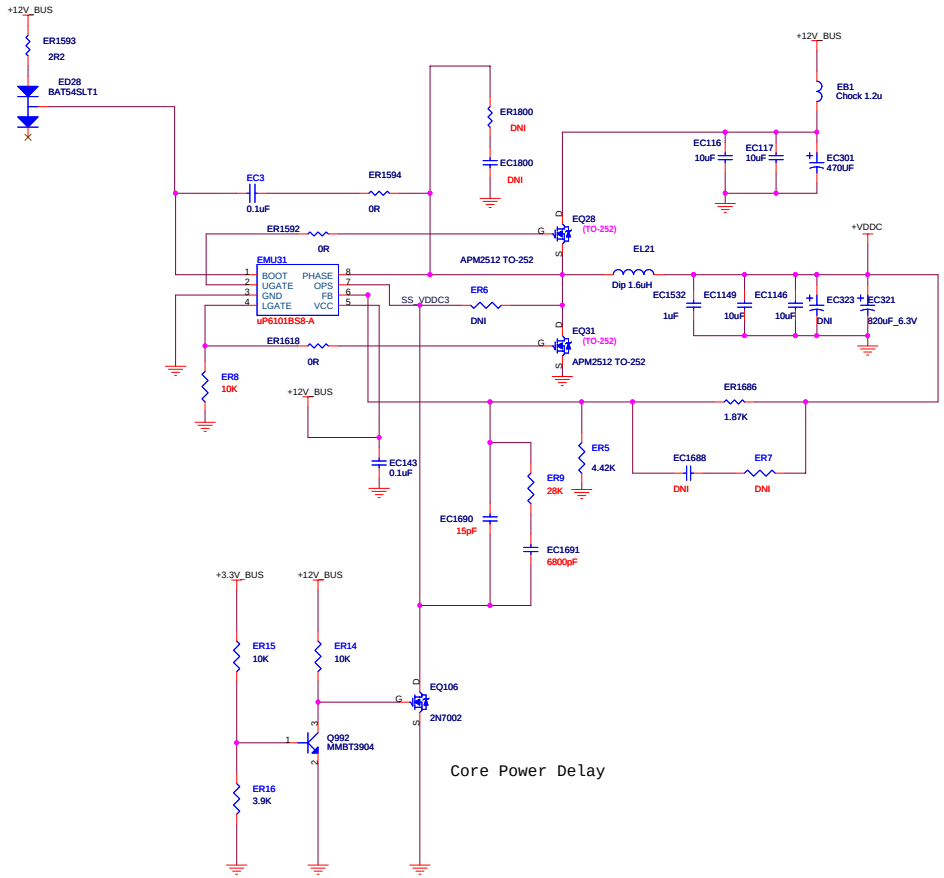
CORE REGULATOR +VDDC



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Title	TR RV630 - MVDD SMPS02	
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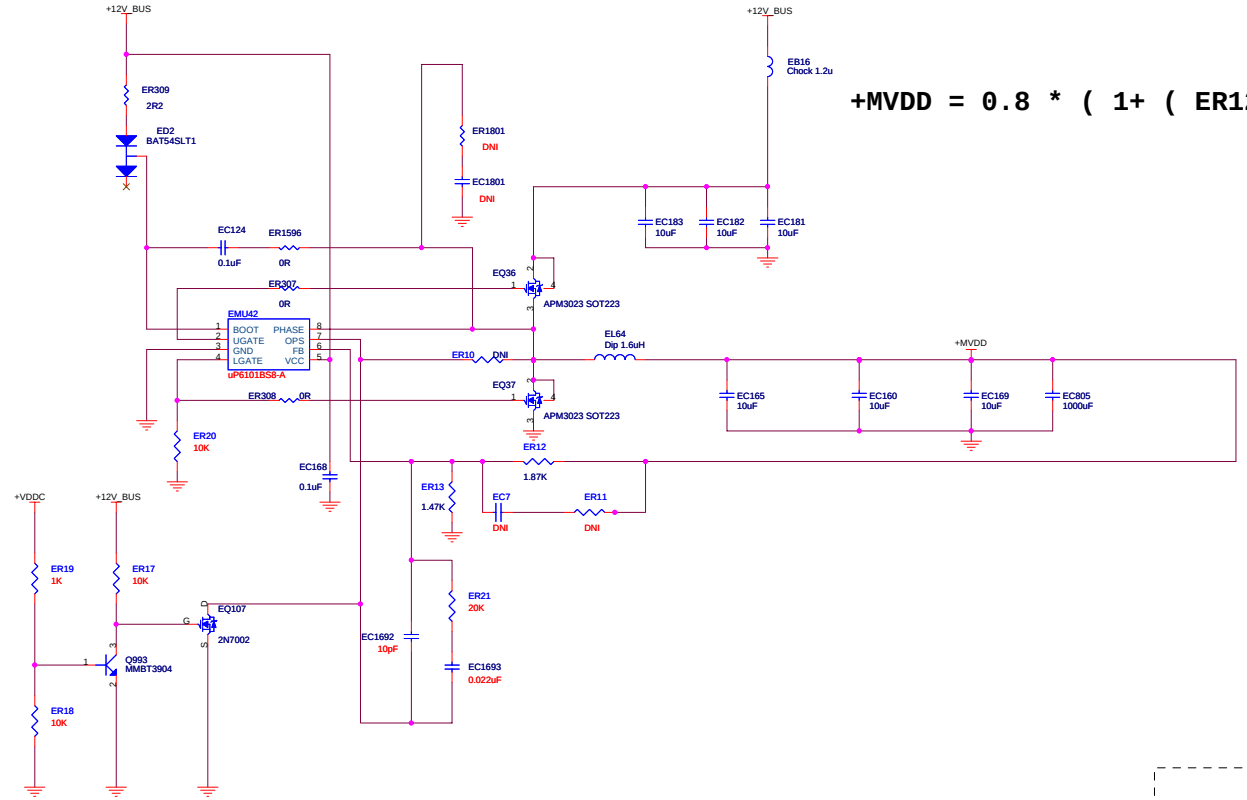
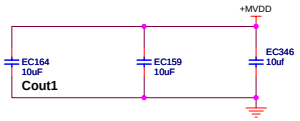
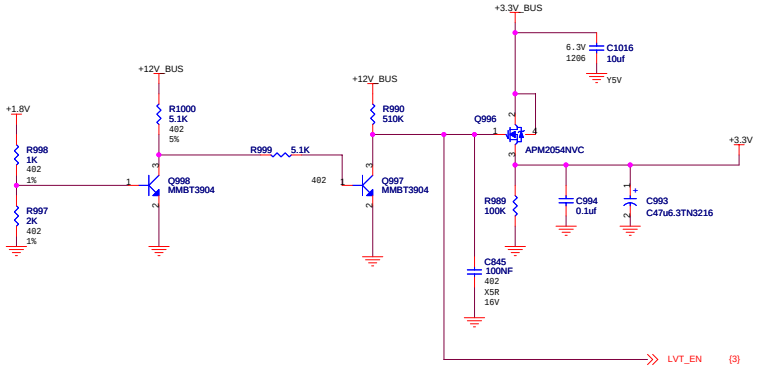
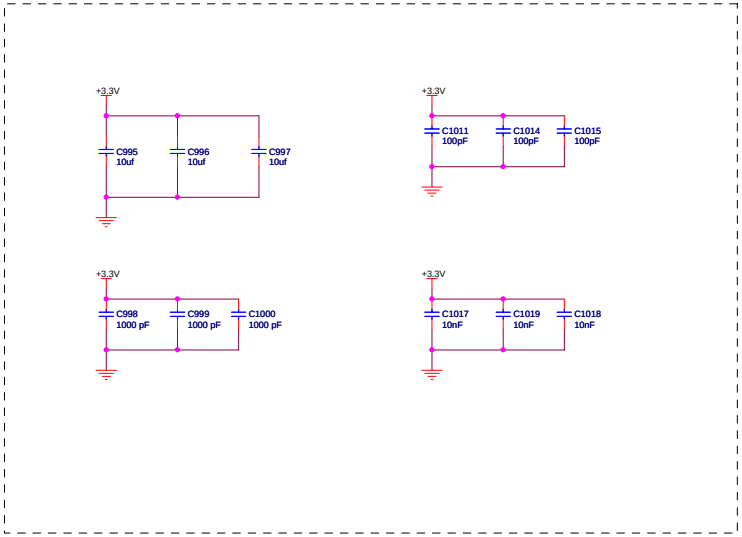


Memory Power Seq

+MVDD = 0.8 * (1+ (ER12 / ER13))







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Title TR RV630 - MVDD SMPS02

Size	Document Number	Rev
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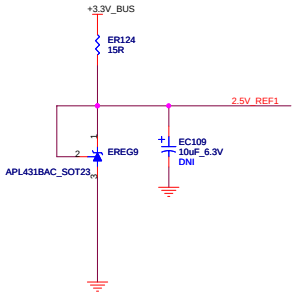
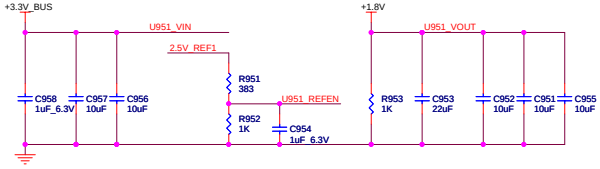
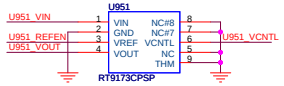
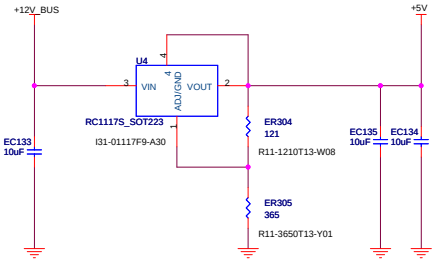
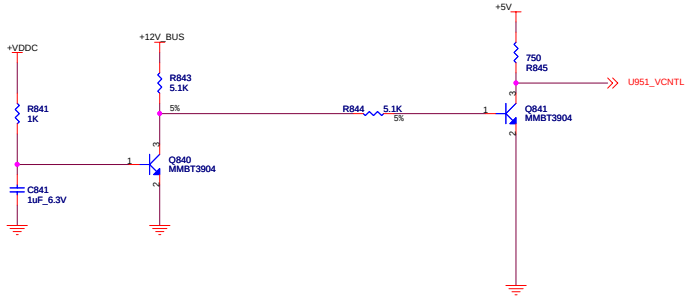




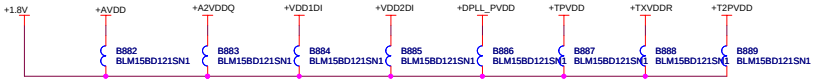




Vout=1.25V* [1+(ER305/ER304)]



Shared Power Rails



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PIN BASED STRAPS

+3.3V

DNI	MR50	10K	R50	10K	GPIO_0	
DNI	MR51	10K	R51	10K	GPIO_1	
	MR52	10K	DNI R52	10K	GPIO_2	
	MR53	10K	DNI R53	10K	GPIO_3	
	MR54	10K	1K for BUO R54	10K	GPIO_4	
	MR55	10K	DNI R55	10K	GPIO_5	
	MR56	10K	DNI R56	10K	GPIO_6	
	MR57	10K	NTSC R57	10K	GPIO_7	
	MR58	10K	DNI R58	10K	GPIO_8	
	MR59	10K	R59	10K	GPIO_9	
	MR63	10K	R63	10K	GPIO_13	
	MR62	10K	R62	10K	GPIO_12	
	MR61	10K	R61	10K	GPIO_11	
DNI	MR65	10K	DNI R65	10K	GENERICC	
DNI	MR64	10K	DNI R64	10K	GENERICB	
	MR66	10K	R66	10K	A_VSYNC_DAC1	A_VSYNC_DAC1 {3,13}
	MR67	10K	R67	10K	A_HSYNC_DAC1	A_HSYNC_DAC1 {3,13}
	MR68	10K	DNI R68	10K	PSYNC	
	MR69	10K	DNI R69	10K	GPIO21_BB_EN	GPIO21_BB_EN {3}
	MR70	10K	DNI R70	10K	VID_0	
	MR71	10K	DNI R71	10K	VID_1	
	MR72	10K	DNI R72	10K	VID_2	
DNI	MR73	10K	R73	10K	VID_3	
	MR74	10K	DNI R74	10K	VID_4	
	MR75	10K	DNI R75	10K	VID_5	
	MR76	10K	DNI R76	10K	VID_6	
	MR77	10K	DNI R77	10K	VID_7	
DNI	MR80	10K	R80	10K	A_VSYNC_DAC2	A_VSYNC_DAC2 {3,14}
	MR79	10K	DNI R79	10K	A_HSYNC_DAC2	A_HSYNC_DAC2 {3,14}
	MR60	10K	DNI R60	10K	DVALID	
DNI	MR87	10K	DNI R87	10K		PWRCNTL_0 {3}
DNI	MR46	10K			GPIO_22	GPIO_22 {3}
DNI	MR88	10K	R88	10K		GPIO_18 {3}

PSYNC {3}
DVALID {3}

GENERICB {3}
GENERICC {3}

{3} VID_[7..0]
VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
VID_7

{3} GPIO_[13..0]
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - ATI Internal Use Only - Reserved (Default: 00)

GPIO(4) - DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(7) - TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

GPIO(8) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0] IF BIOS_ROM_EN=1 [default] (GPIO_22)
tmel - AT25F512A (512 kbit)0010
AT25F1024A (1 Mbit)0011
ST Microelectronics- M25P05A (512 kbit) 0100
M25P10A (1 Mbit) 0101
M25P20 (2 Mbit) 0101
Chingis (formerly PMC) -
Pm25LV512 (512 kbit) 0100
Pm25LV010 (1 Mbit) 0101

If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. (Config 3 = don care).
x000 128MB
x001 256MB
x010 64MB
x011 32MB
x100 512MB
x101 1GB
x110 2GB
x111 4GB

GENERICC, GENERICB - ATI Internal Use Only - Reserved (Default: 0)

VSYNC - VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - ATI Internal Use Only - Reserved (Default 0)

PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO_21 - ATI Internal Use Only - Reserved (Default: 0)

VID_0 - ATI Internal Use Only - Reserved (Default: 0)

VID_1 - MSI_DIS (Default: 0)

VID_2 - ATI Internal Use Only - Reserved (Default: 0)

VID_3 - BIF_AUDIO_EN
0 - Disable HD Audio 1- Enable HD Audio

VID_4 - ATI Internal Use Only - Reserved (Default: 0)

VID_5 - 64BAR_EN_A (Default: 0)
Enable 64-bit BARS

VID_6:7 - ATI Internal Use Only - Reserved (Default: 00)

VSYNC - MEMORY CONFIG ATI Board Feature I
0 = single rank memory, 1 = dual rank memory

HSYNC2 - ATI Internal Use Only - Reserved (Default: 0)

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

GPIO_15 - FOR FUTURE EXPANSION

GPIO_22_ROMCSb - Enable external BIOS ROM device (Default 1)

GPIO_18 - MEMORY CONFIG BANK SELECT
0 - 4 BANKS, 1 - 8 BANKS

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground High logic voltage

Signal

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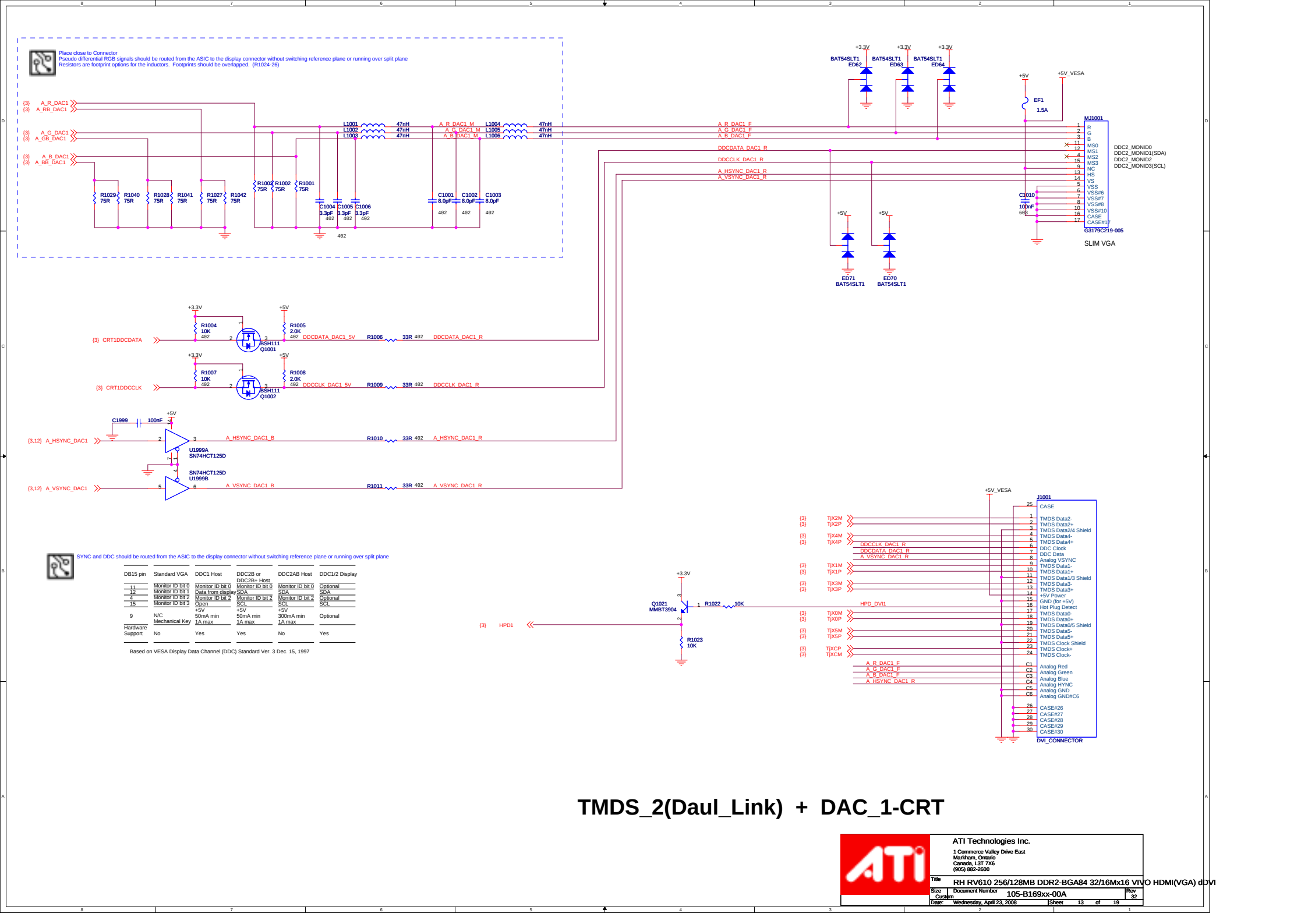

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C Mechanical Key	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	No	Yes	Yes	No	Yes

TMDS_2(Daul_Link) + DAC_1-CRT

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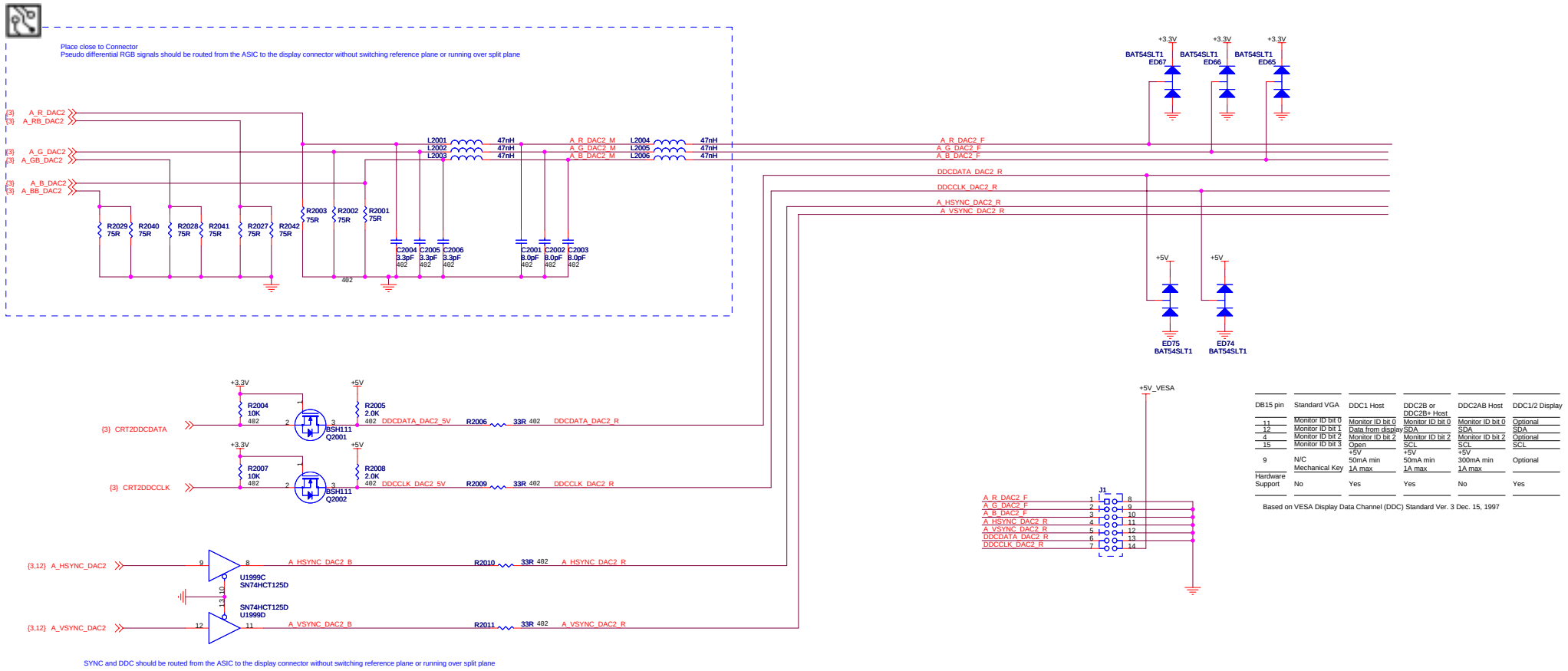

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	+5V Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

Very important to meet HDMI compliance requirements
Capacitance of SDADDC_HDMI & SCLDDC_HDMI nets to Power/GND planes must be less than 50pF (try to make it lower)

55mA current limited +5V rail

TMDS_1(Single_Link) + DAC_2-CRT

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Size: Custom | Document Number: 105-B169xx-00A | Rev: 32

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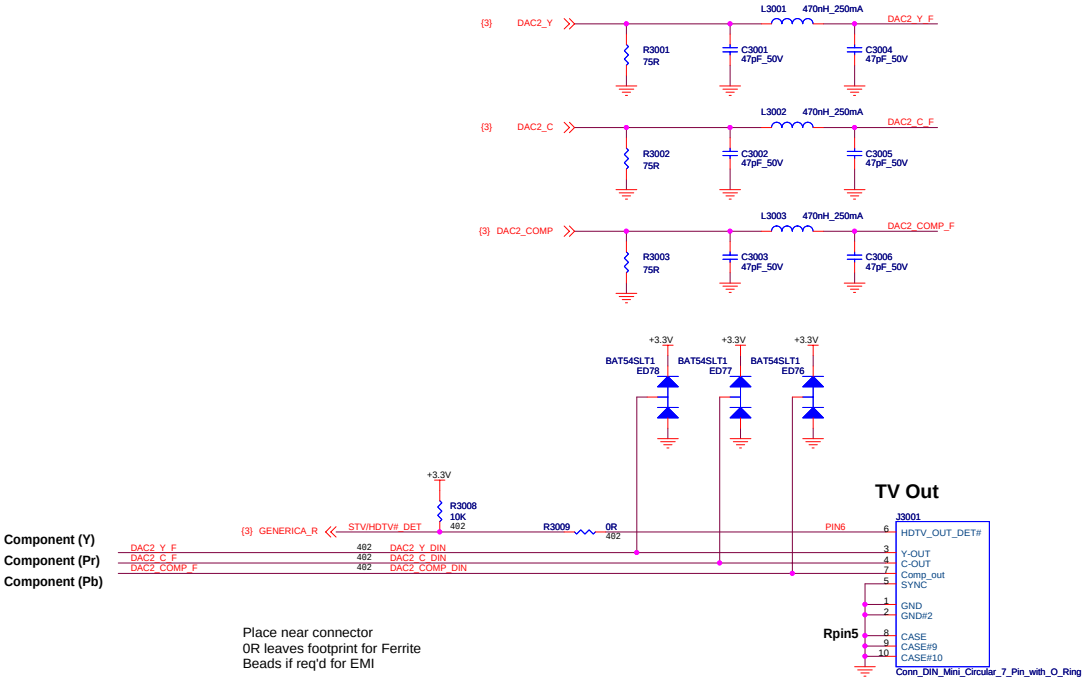

Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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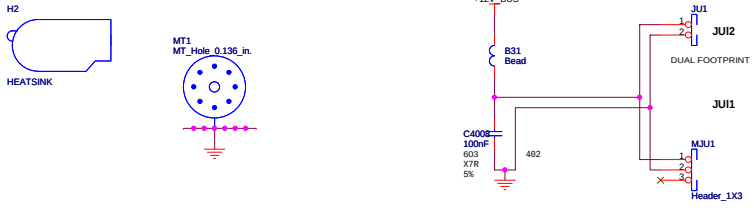
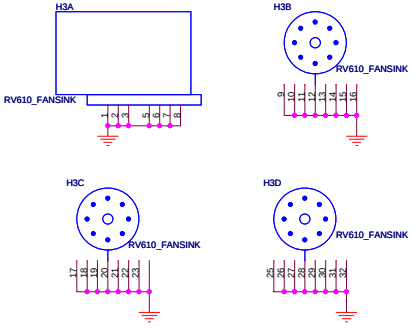


80200439A0G (DVI+HDMI+DIN)



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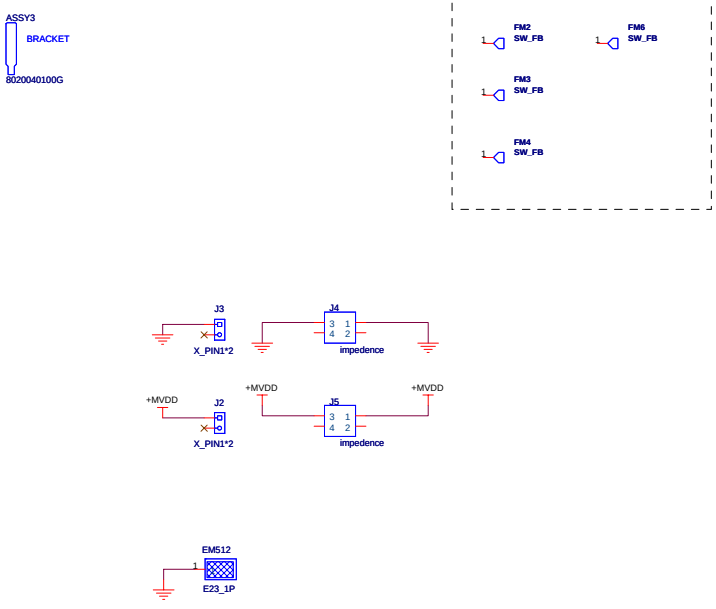

<Variant Name>

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<Variant Name>

Title

RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VG105 BM)

Schematic No. 113-B319xx-00A

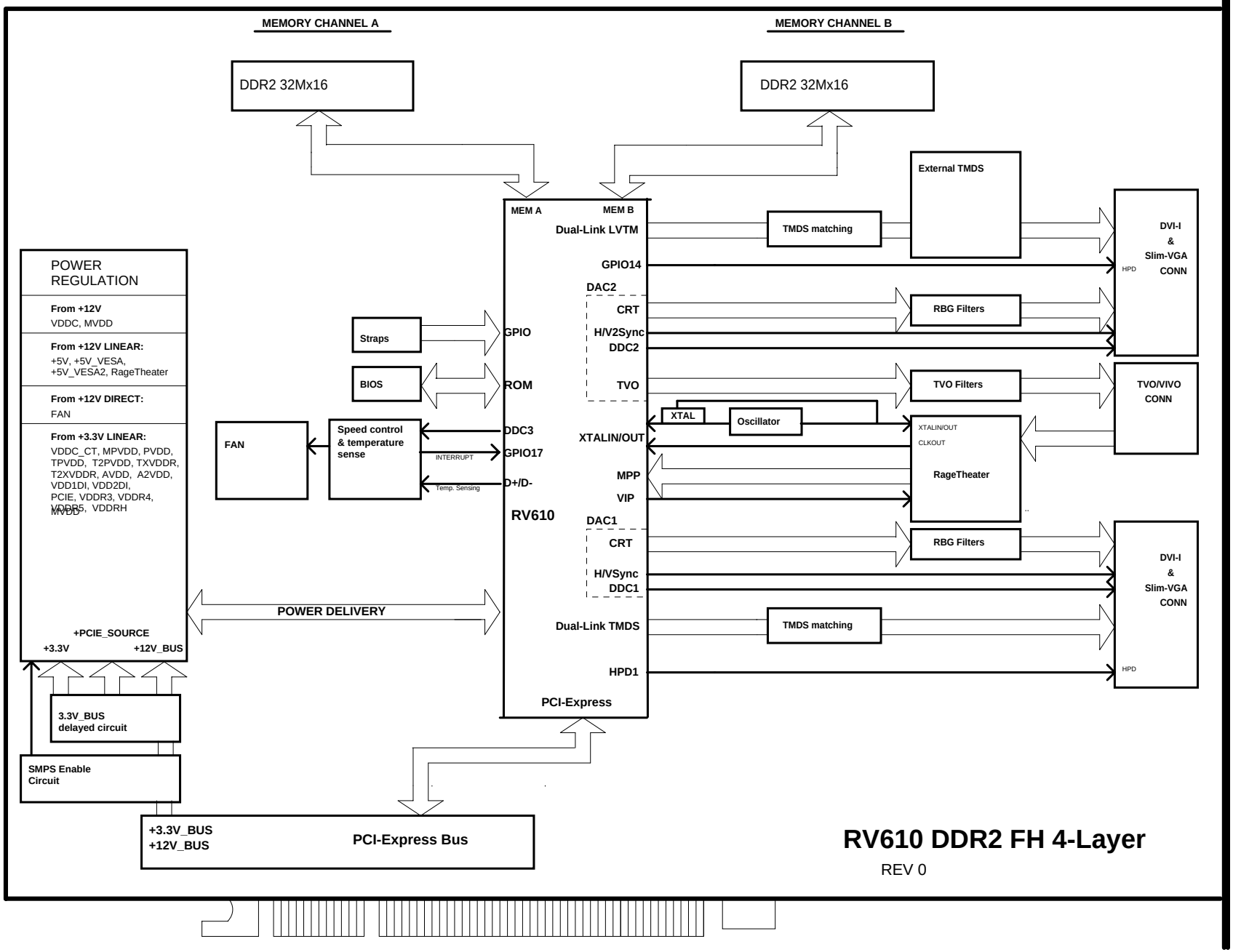
Date: Wednesday, April 23, 2008

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact ATI representative to obtain latest BOM closest to the application desired.**

Rev 32

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
		2006.12.01	UPDATE SCHEM. BOM MANAGEMENT.
		2006.12.14	UPDATE SCHEMATIC TO NETLIST WITH NO ERRORS
		2006.12.18	DORINA UPDATE MEM SWAP
		2006.12.19	REMOVE TP ON MEM - TO BE REPLCED BY 0.8MM PADS ON ALL LINES
		2006.12.20	CHANGED B67 to PN 5260014800G AND C76 to PN 4172010500G
0	00A	2006.12.21	J2 REMOVED
		2007.01.15	NC626 removed (VDDC output cap). LDO output resistor (R879, R880) moved closer to LDO. MVDD LDO input resistors changed to 1R. Debug header changed to include Gen1/2 switch. HDMI caps removed. Added thermal shutdown option to power sequencing.
		2007.01.16	REMOVE BACK BIAS, REMOVE MC624
		2007.01.17	REMOVE R5515, R5516, R5521, R5524 REMOVE R94
		2007.01.22	ADDED H3, H4, H5
		2007.01.22	DECAP CHANGES ON PAGE 3
		2007.01.23	HEATSINK GROUNDING ADJUSTED
		2007.01.23	DORINA - HEATSINK GNDING PINS ADJUSTED
		2007.01.24	RM JTAG + SMA CLOCK CONNECTIONS TO EASE LAYOUT CONGESTION
		2007.01.24	ADDED C300, C301, C302 (STITCHING CAPS) TO IMPROVE DDC LINES
		2007.01.24	FIXED ORCAD NETLIST PROBLEM; NO EFFECTIVE CHANGE.
		2007.01.24	ADD Q102 TO SOLVE A11 VDDR3 LEAKAGE PROBLEM.
1	00B	2007.01.25	CHNG REF DES OF VDDR3 LEAKAGE BLOCK TO Q/R-90
2	00C	2007.02.09	PCB mechanical updates only. No Schematic changes.



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