

PG110-A00

GP108 64Bit GDDR5 X32

HDMI/DP + DVI-D/DP

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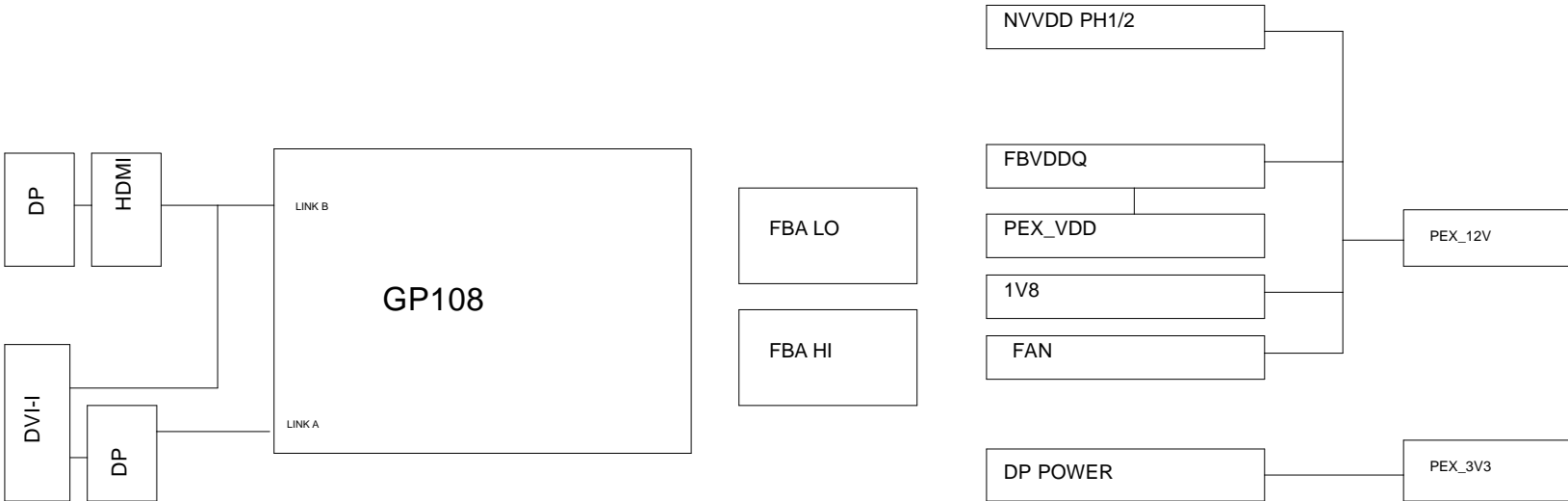
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Block Diagram

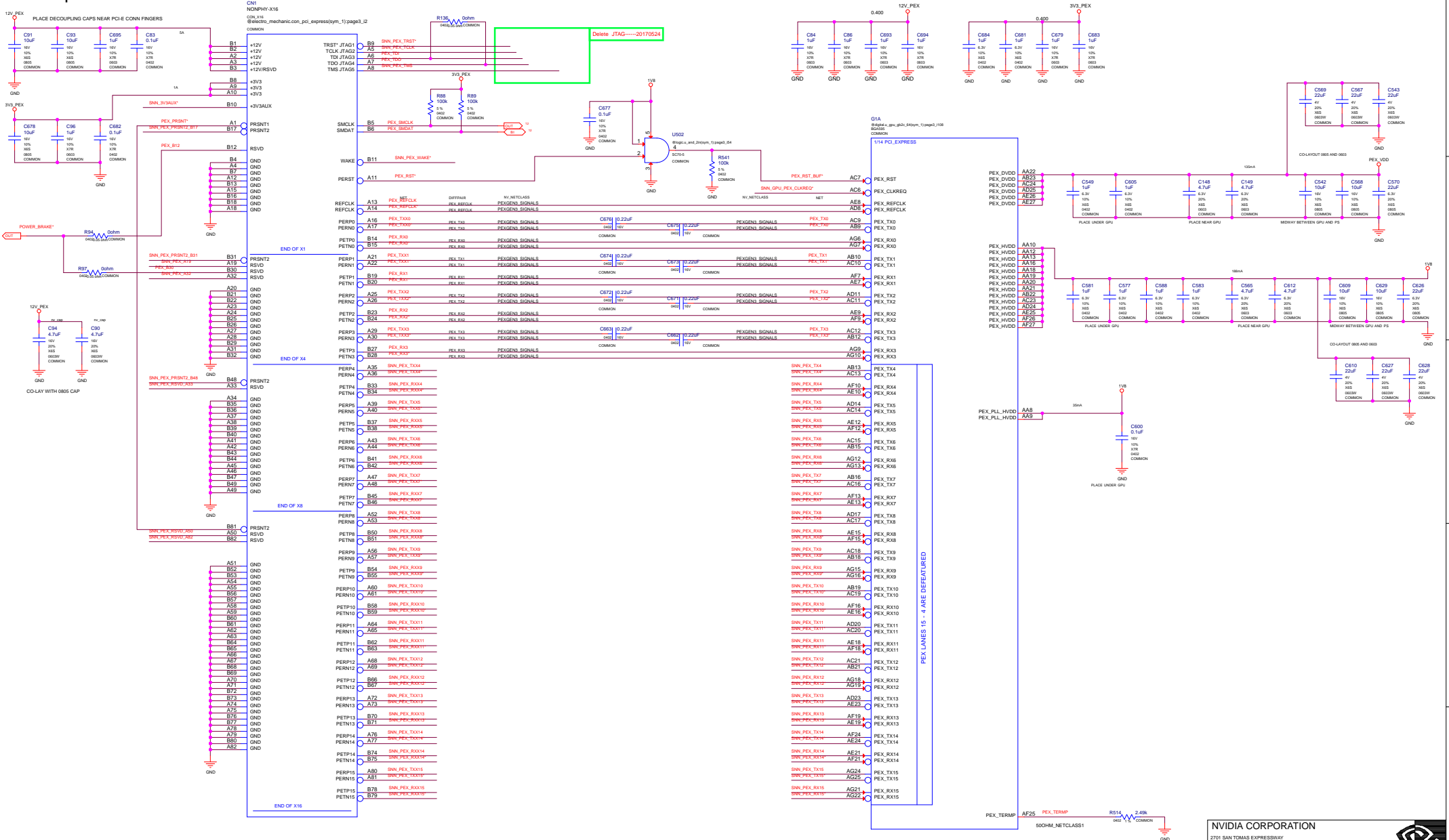


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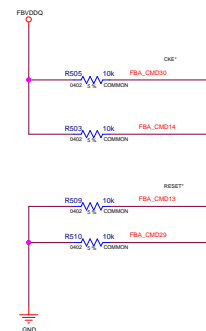
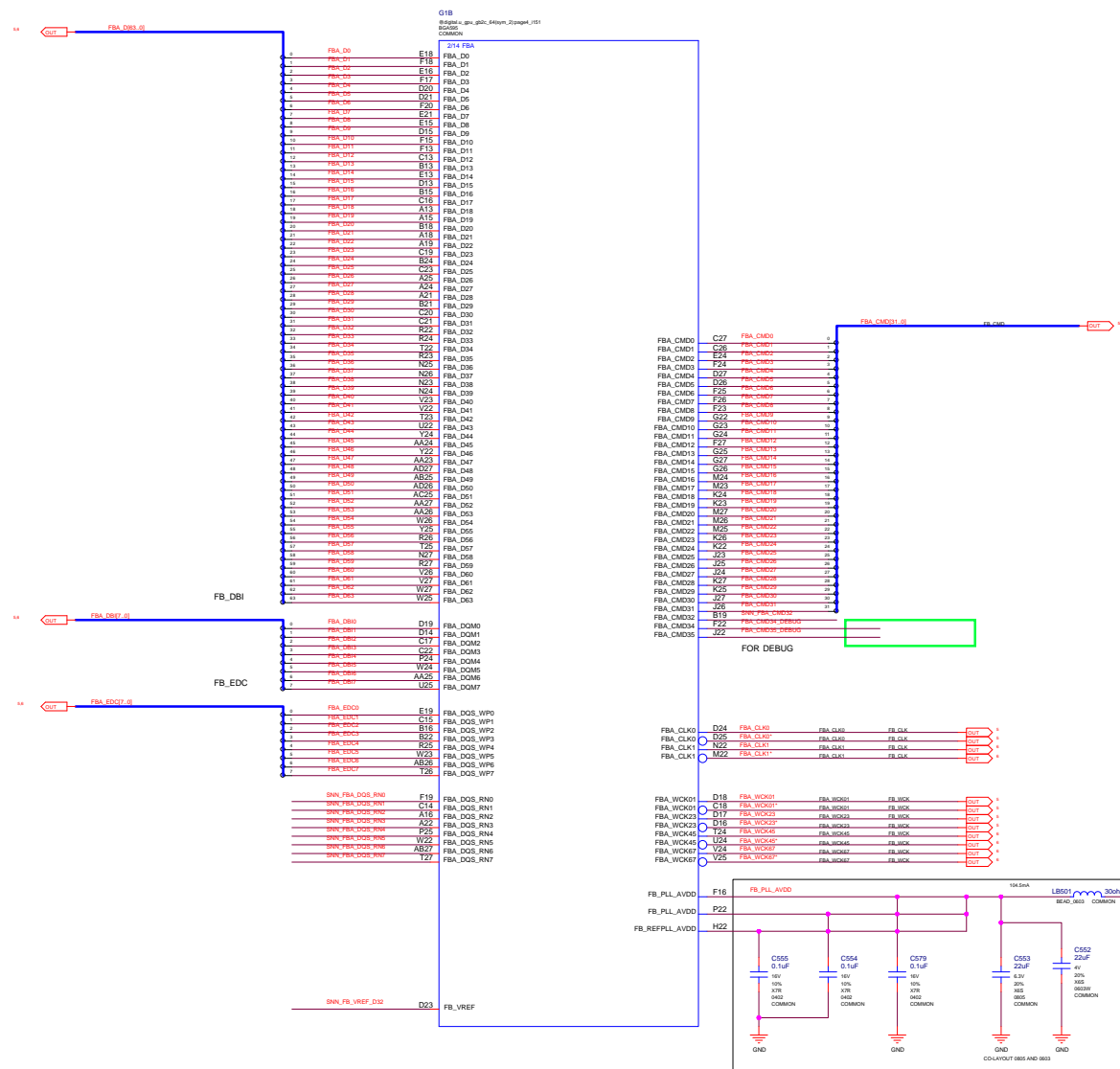
PCI Express




ASSEMBLY	ASSEMBLY DESCRIPTION	SANTA CLARA, CA 95050, USA	
PAGE DETAIL	PCI Express	NV_PN	
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ISOLATES ALL		PCB REV	PG110-A00
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GPU Frame Buffer

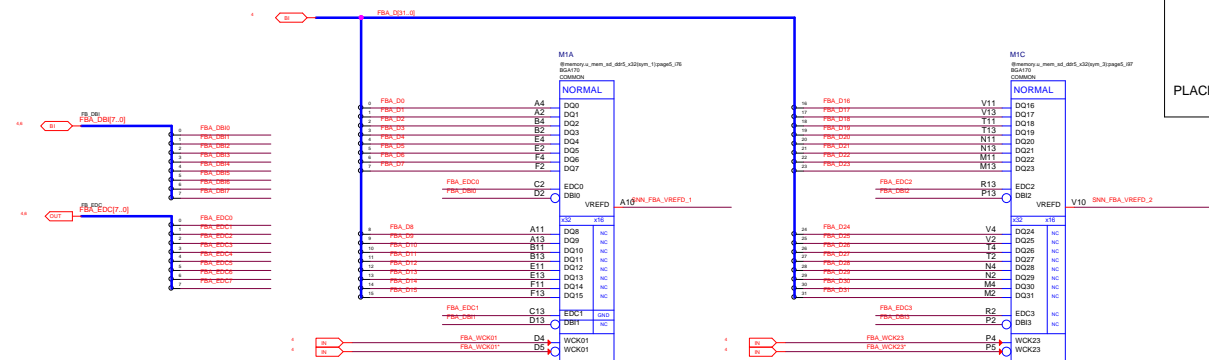
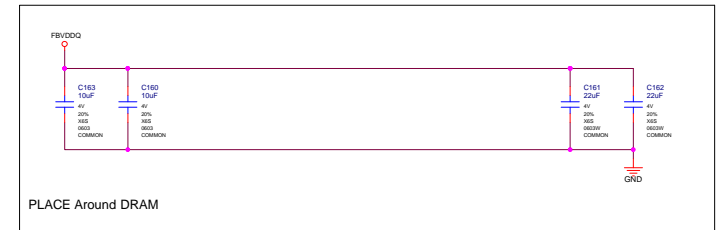
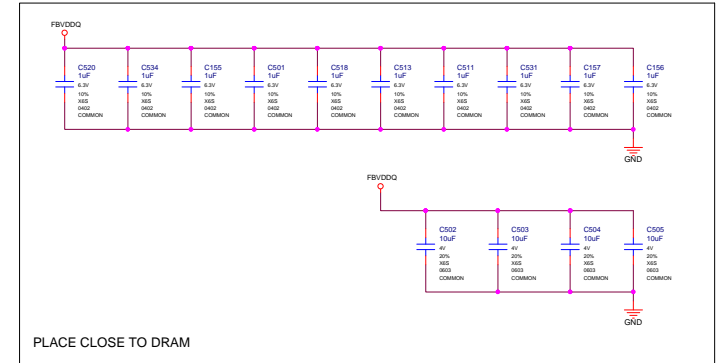
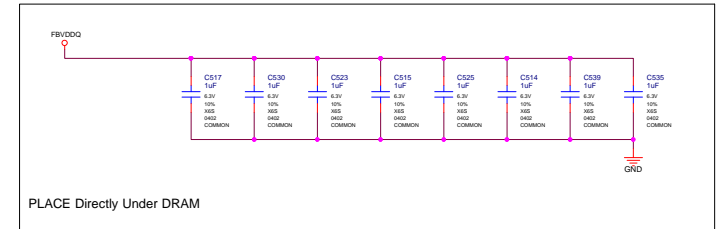
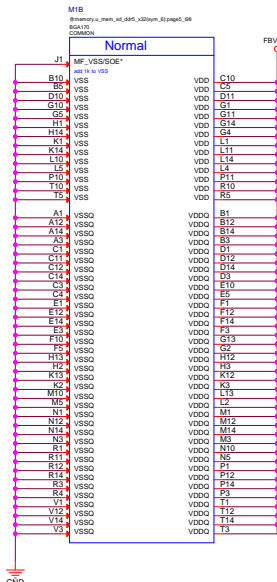
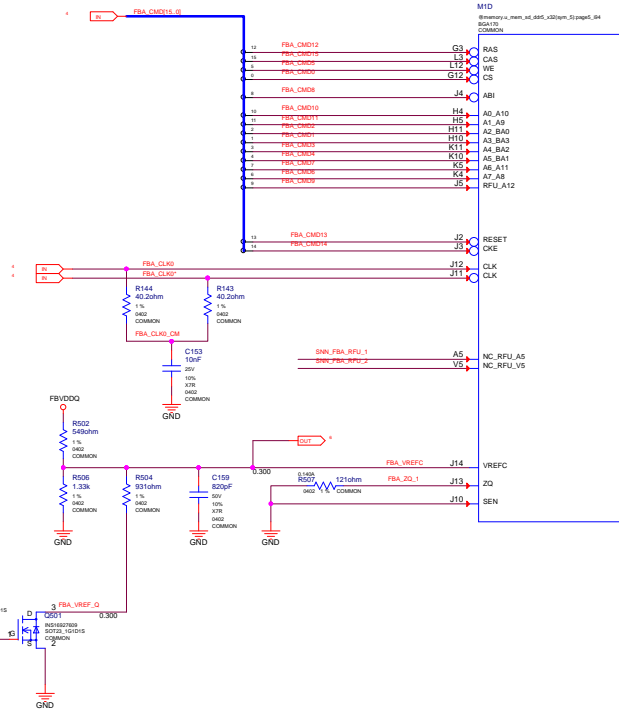


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FBA bits 31..00

CMD	0.31	32.63
CMD0	CS ¹	
CMD1	A3_BA0	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A6_BA1	
CMD5	WEC	
CMD6	A7_A8	
CMD7	AB ¹	
CMD8	AB ¹	
CMD9	A12_RFU	
CMD10	AL_A11	
CMD11	A1_A9	
CMD12	BA0 ¹	
CMD13	RS1	
CMD14	CAS ¹	
CMD15	CAS ¹	
CMD16		CS ¹
CMD17		A3_BA0
CMD18		A4_BA2
CMD19		AB ¹
CMD20		WEC ¹
CMD21		A7_A8
CMD22		AB ¹
CMD23		AL_A11
CMD24		A12_RFU
CMD25		A6_A10
CMD26		A1_A9
CMD27		RS1 ¹
CMD28		CAS ¹
CMD29		CAS ¹
CMD30		CAS ¹
CMD31		CAS ¹



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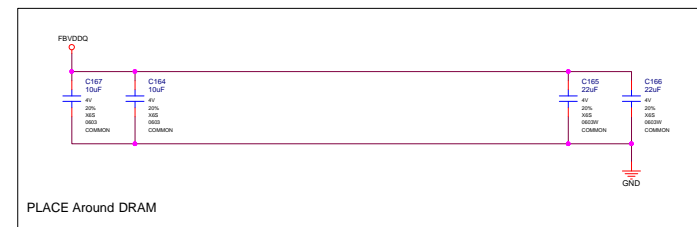
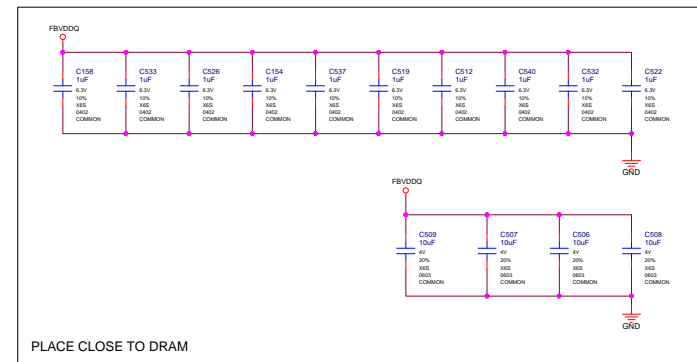
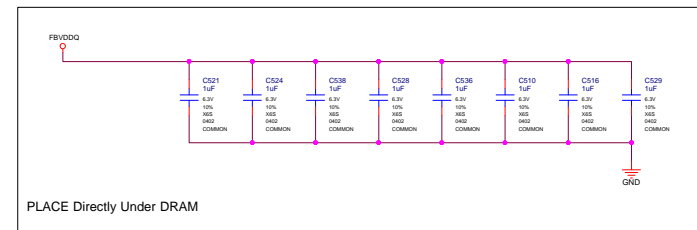
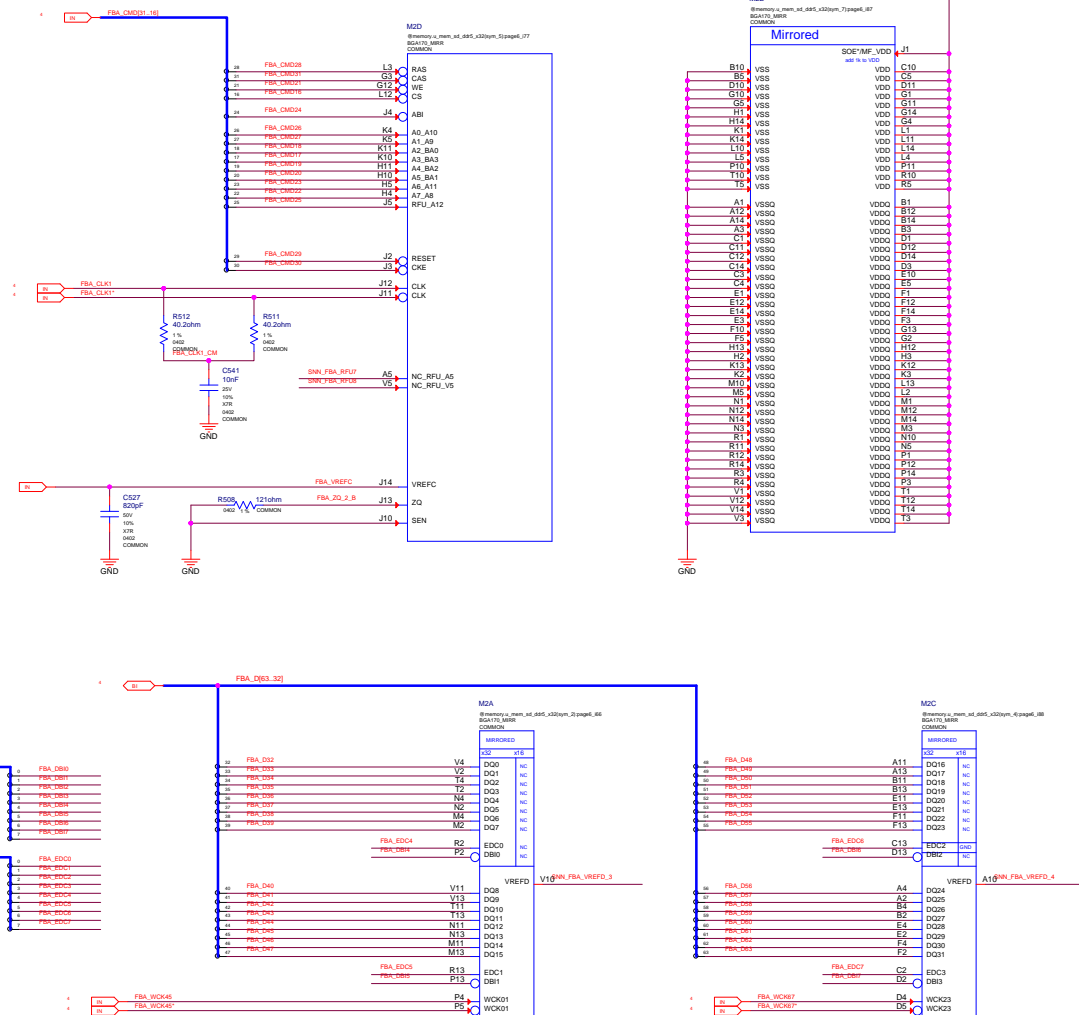
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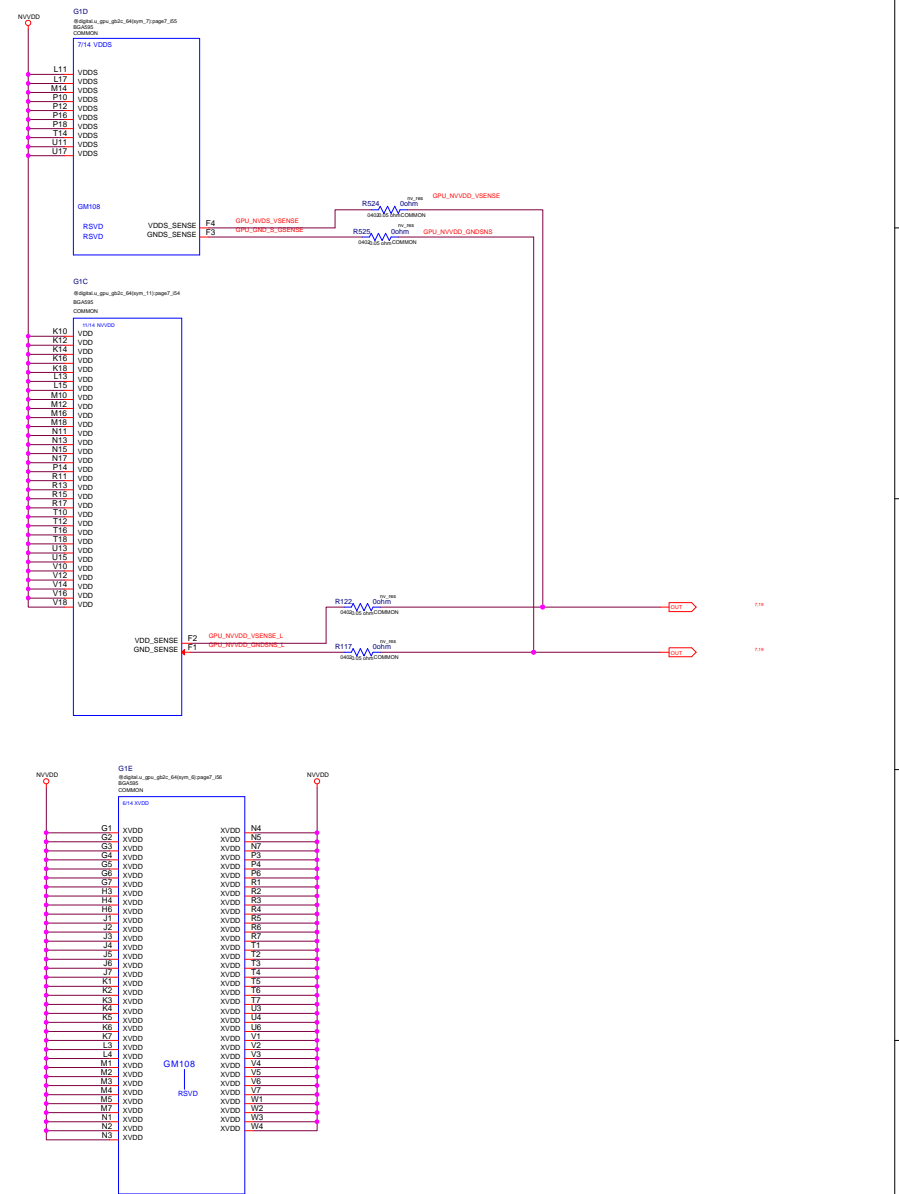
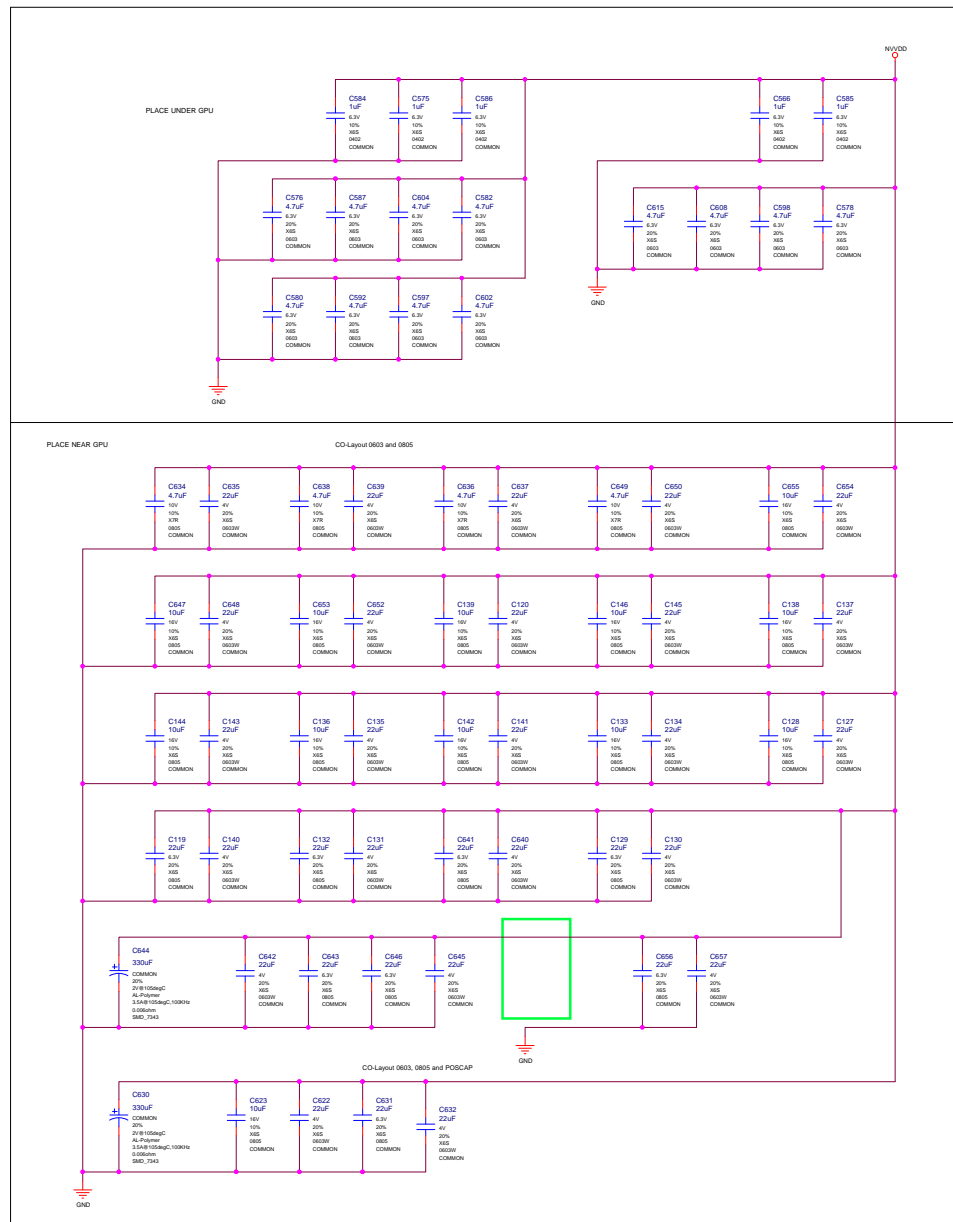
FBA bits 63..32

GDDR5_BGA170_MiRR

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CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB*	
CMD9	A12_RFU	
CMD10	A0_A1	
CMD11	A1_A9	
CMD12	RA5*	
CMD13	RS1*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		AB*
CMD25		A12_RFU
CMD26		A2_A10
CMD27		A0_A9
CMD28		RA5*
CMD29		RS1*
CMD30		CKE*
CMD31		CAS*



NVVVD Decoupling



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PAGE DETAIL
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NVVVD Decoupling

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PCB REV PG110-A00

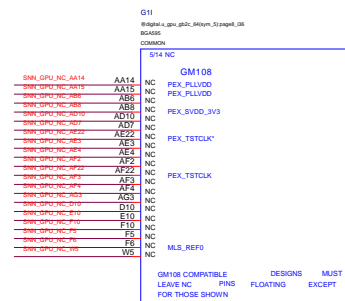
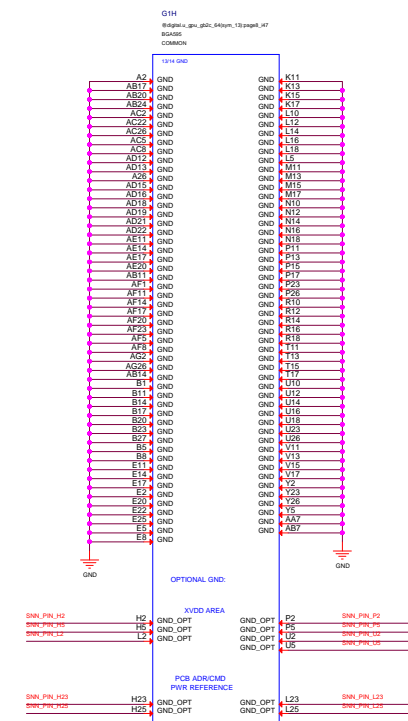
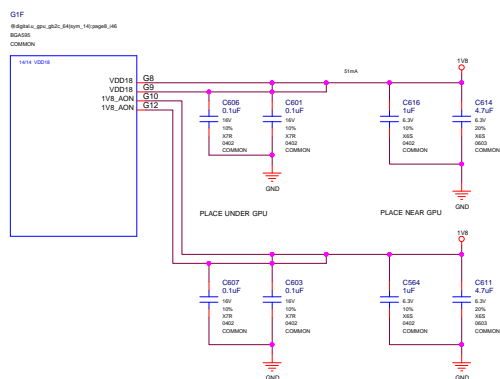
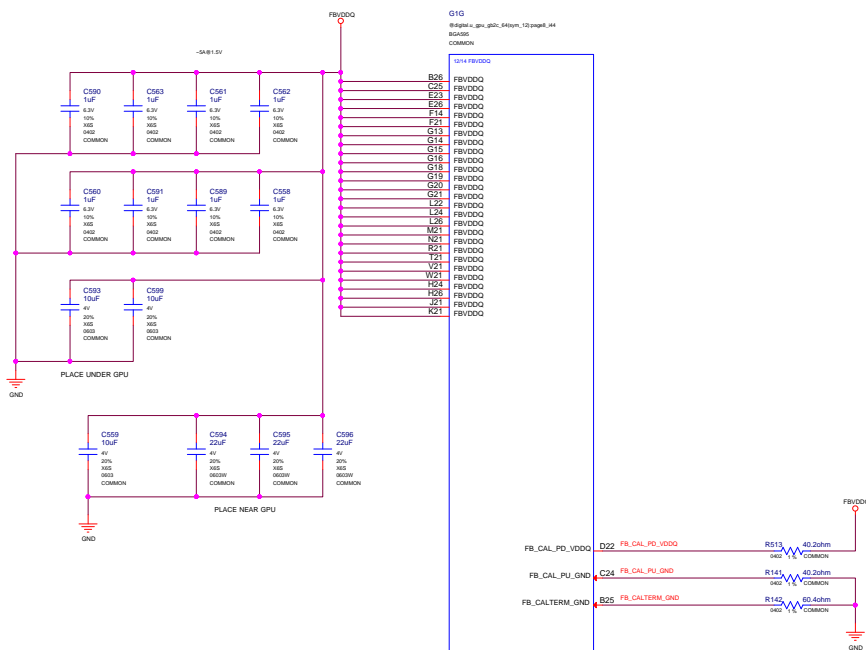
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FBVDDQ and 1V8 Decoupling



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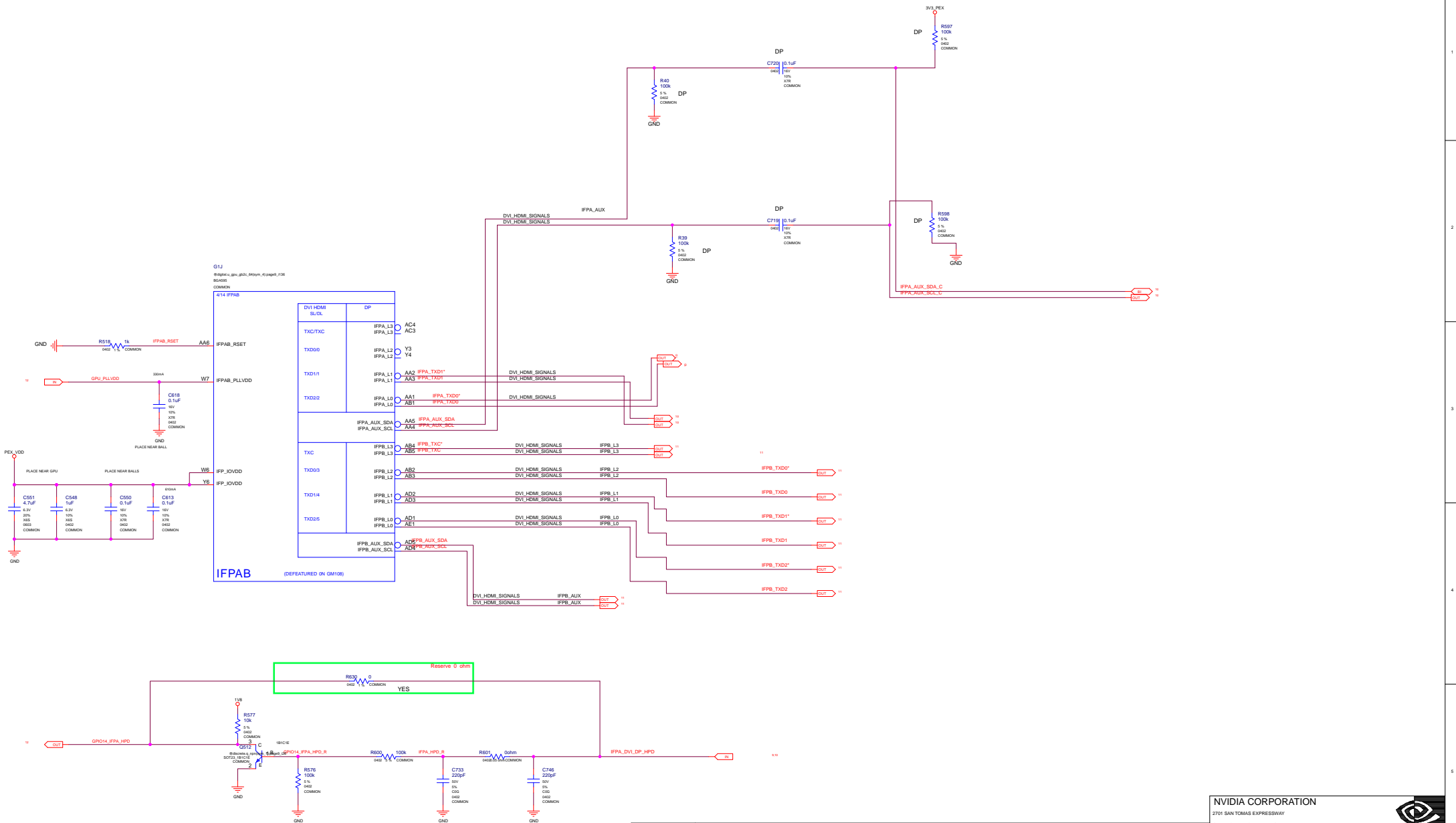


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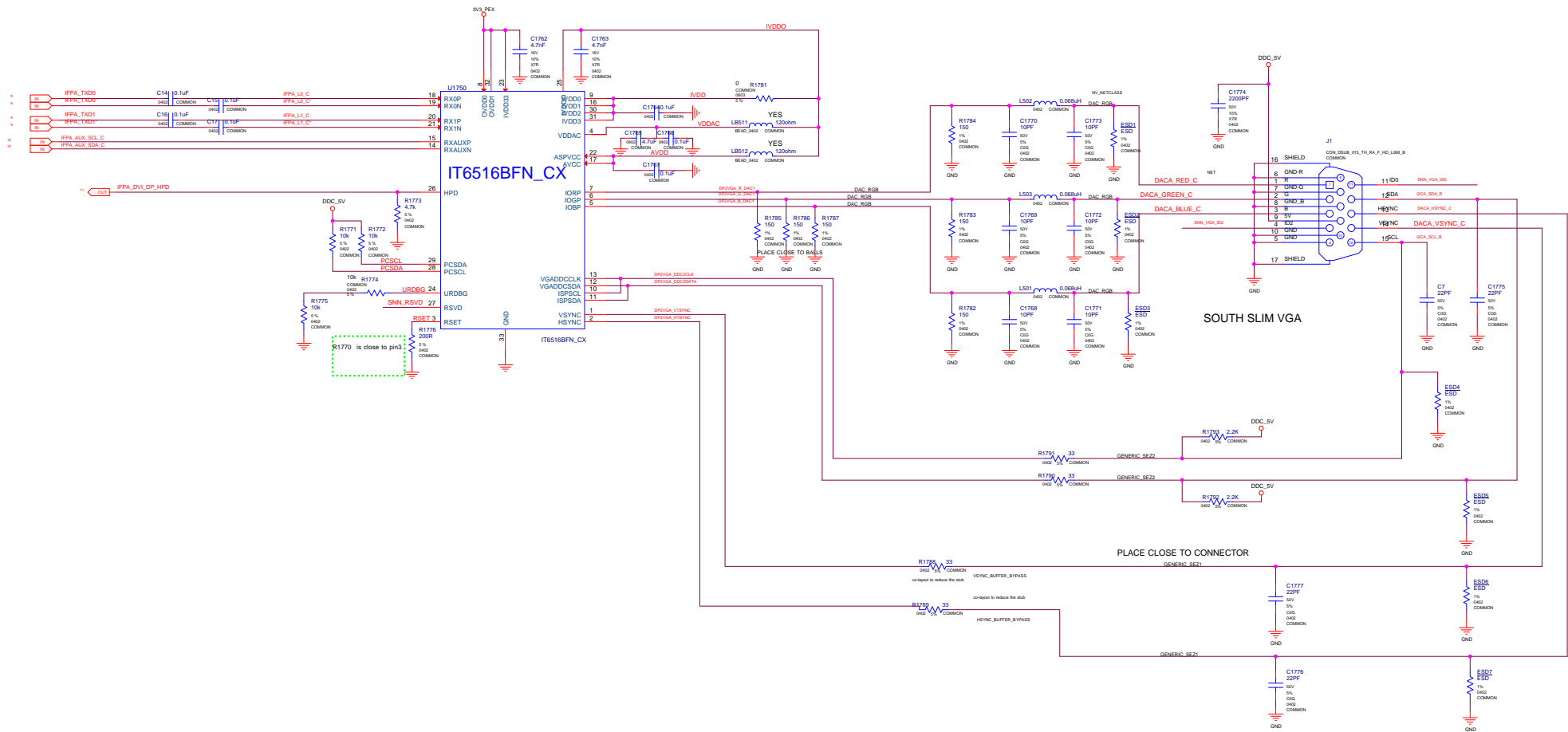
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ASSEMBLY	ASSEMBLY_DESCRIPTION
PAGE DETAIL	FBVDDQ and 1V8 Decoupling

IFPAB DL DVI-D



IFPA DP



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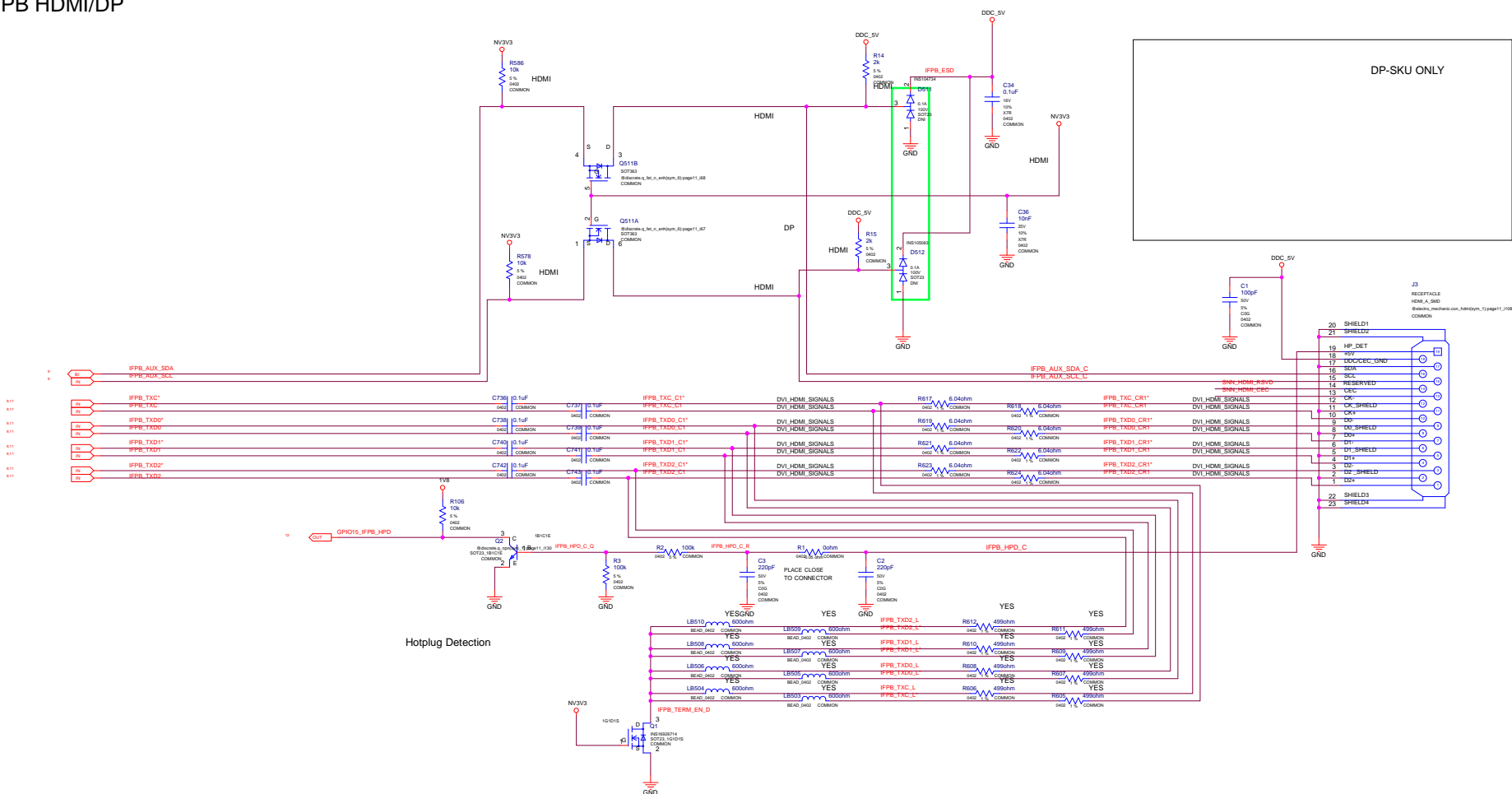


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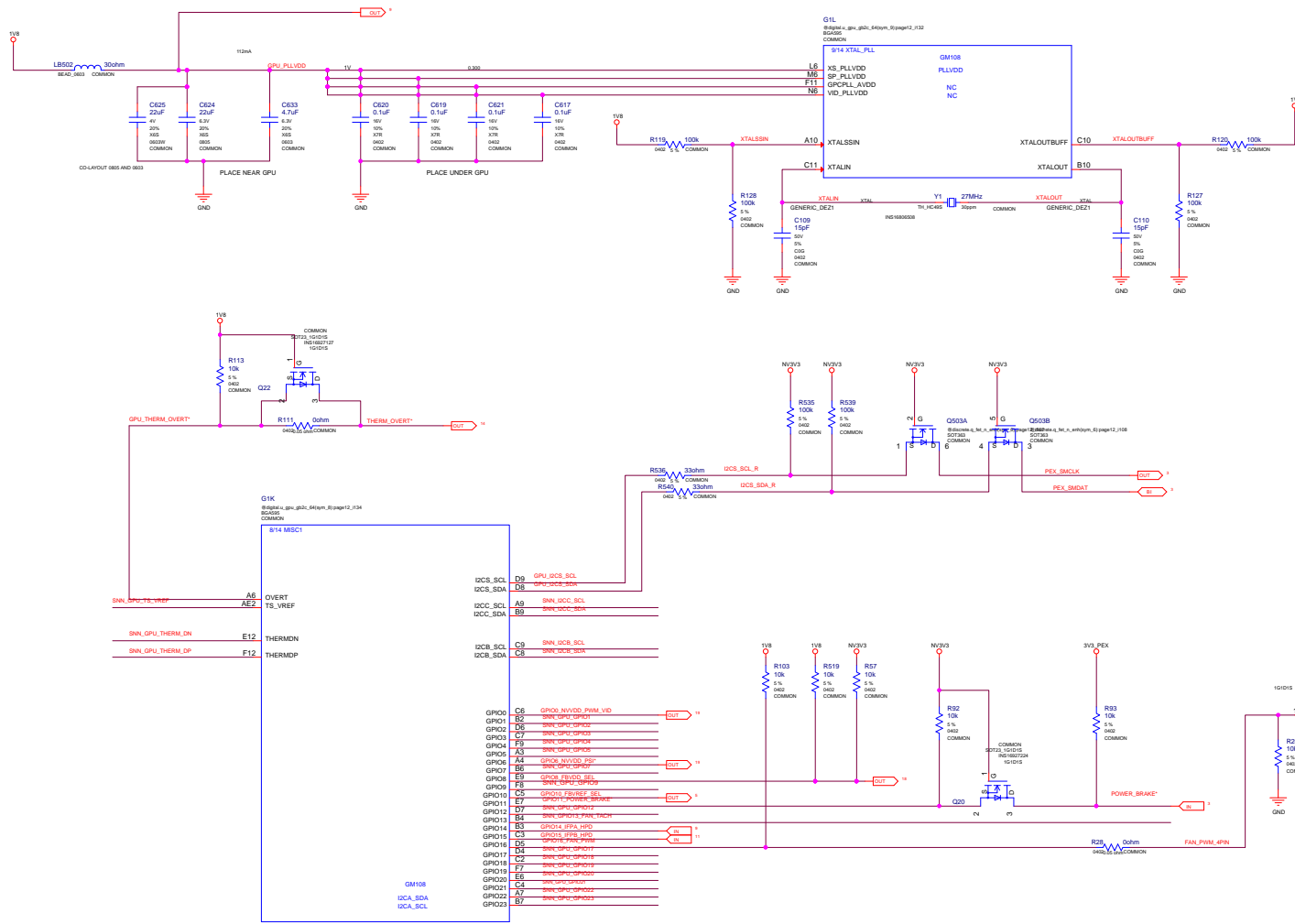
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IFPB HDMI/DP



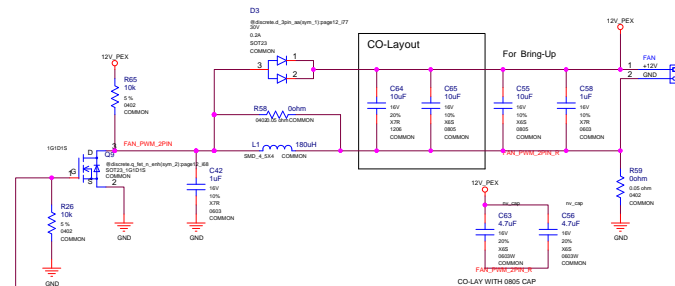
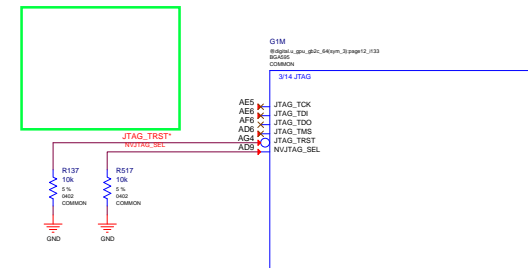
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JTAG,GPIO&XTAL



Smart Fan

XTALOUTBUFF	GPIO PWM %
PU	66% HIGH
MID	33% HIGH (2-PIN DEFAULT)
PD	100% HIGH



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	JTAG,GPIOKXTAL

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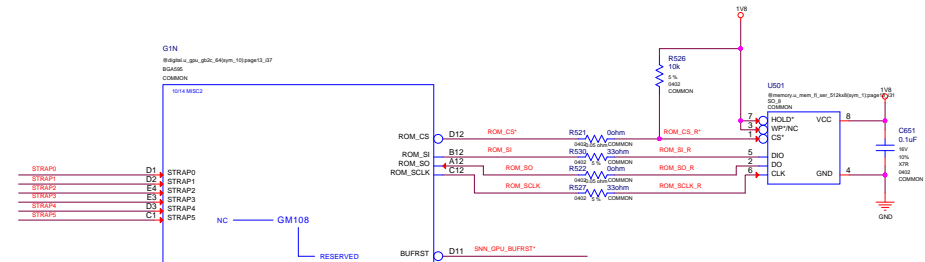
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ROM & STRAPS

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	DEFAULT
L	L	H	0001	
L	H	L	0010	
L	H	H	0011	
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	

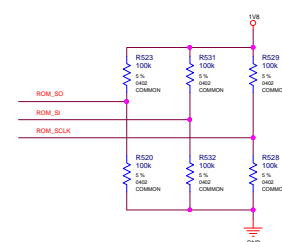
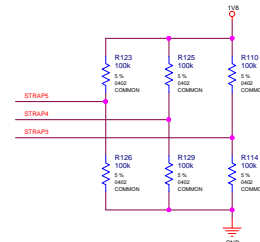
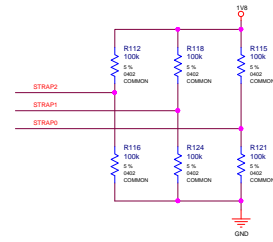
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
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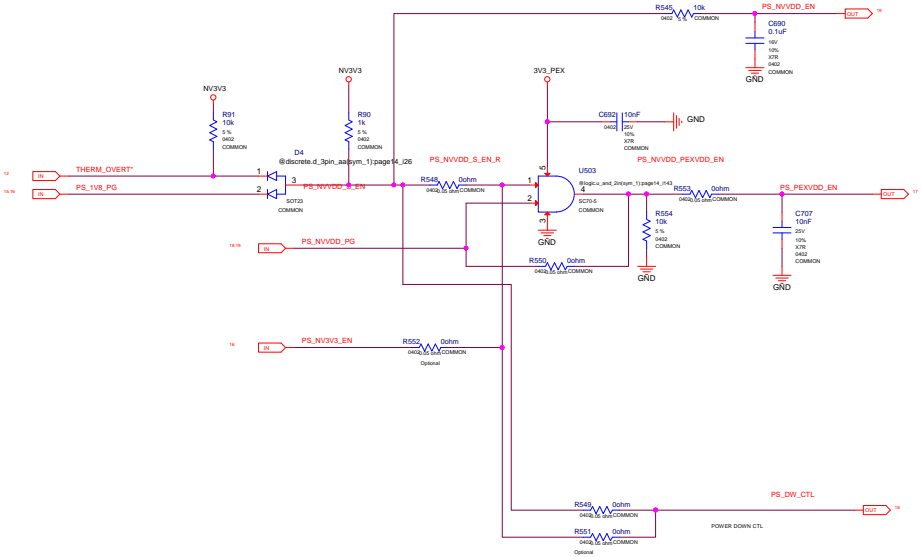
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Power Sequence




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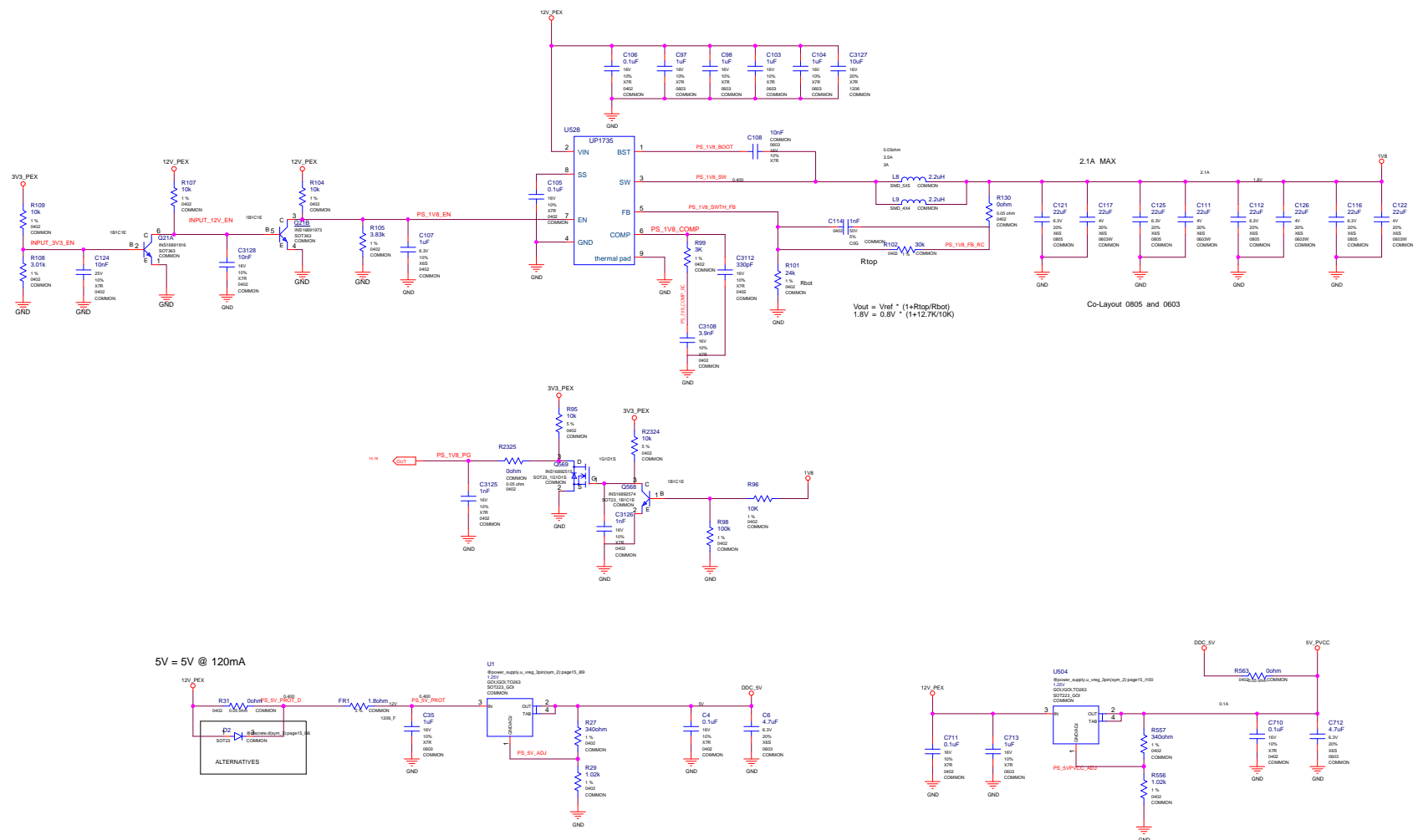
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POWER:1V8 & 5V



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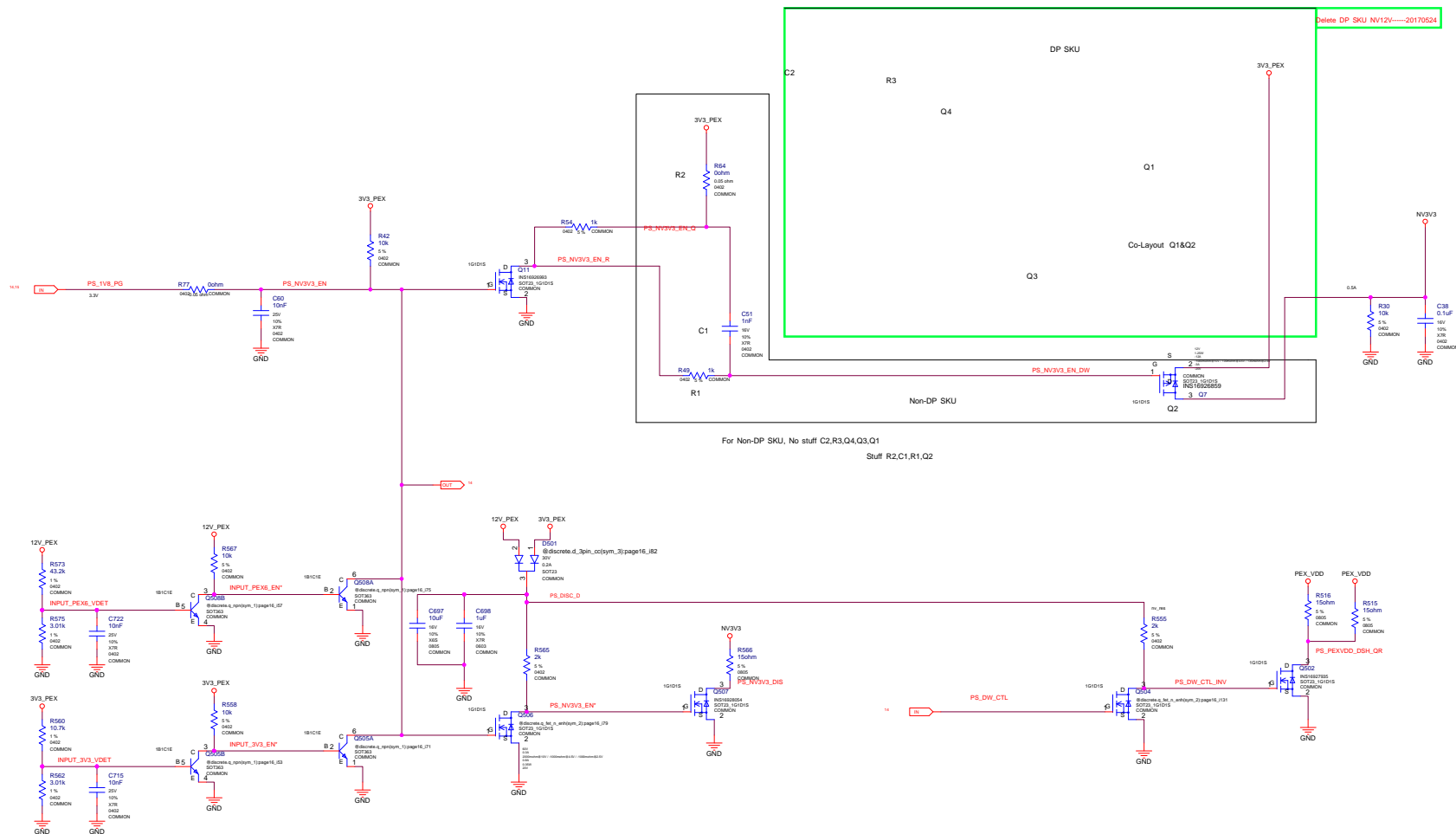
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POWER: NV3V3, NV12V



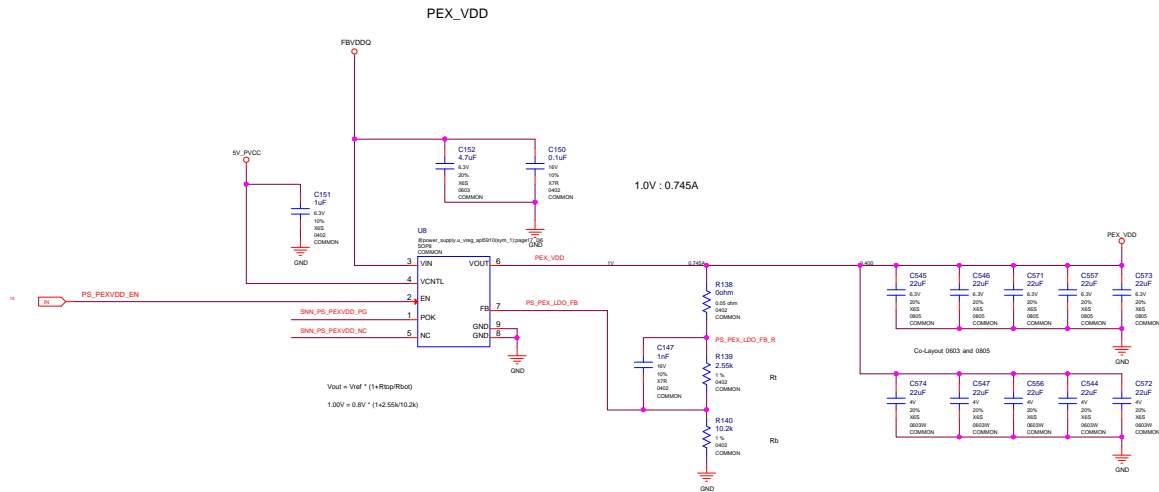
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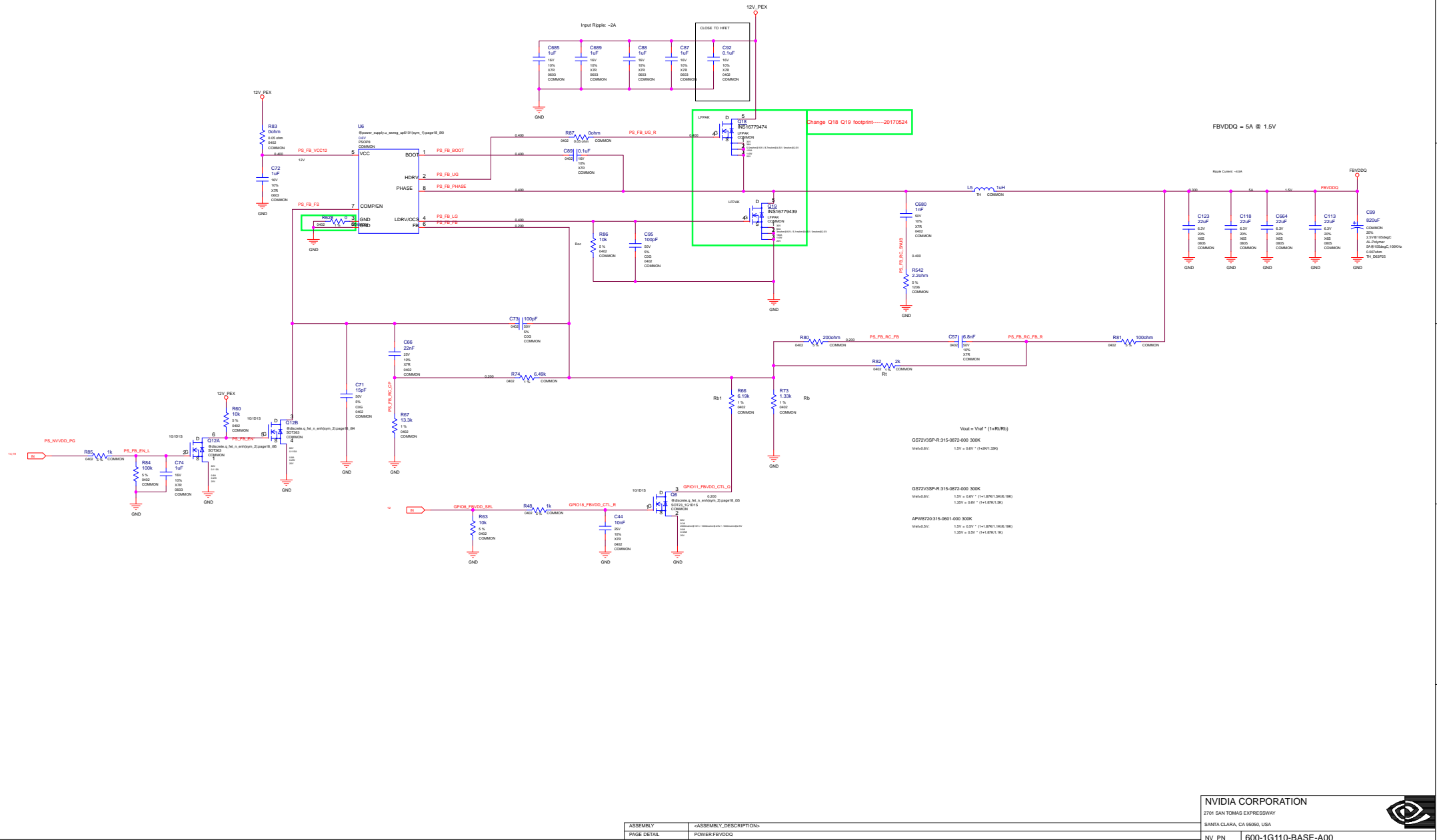
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POWER:FBVDDQ



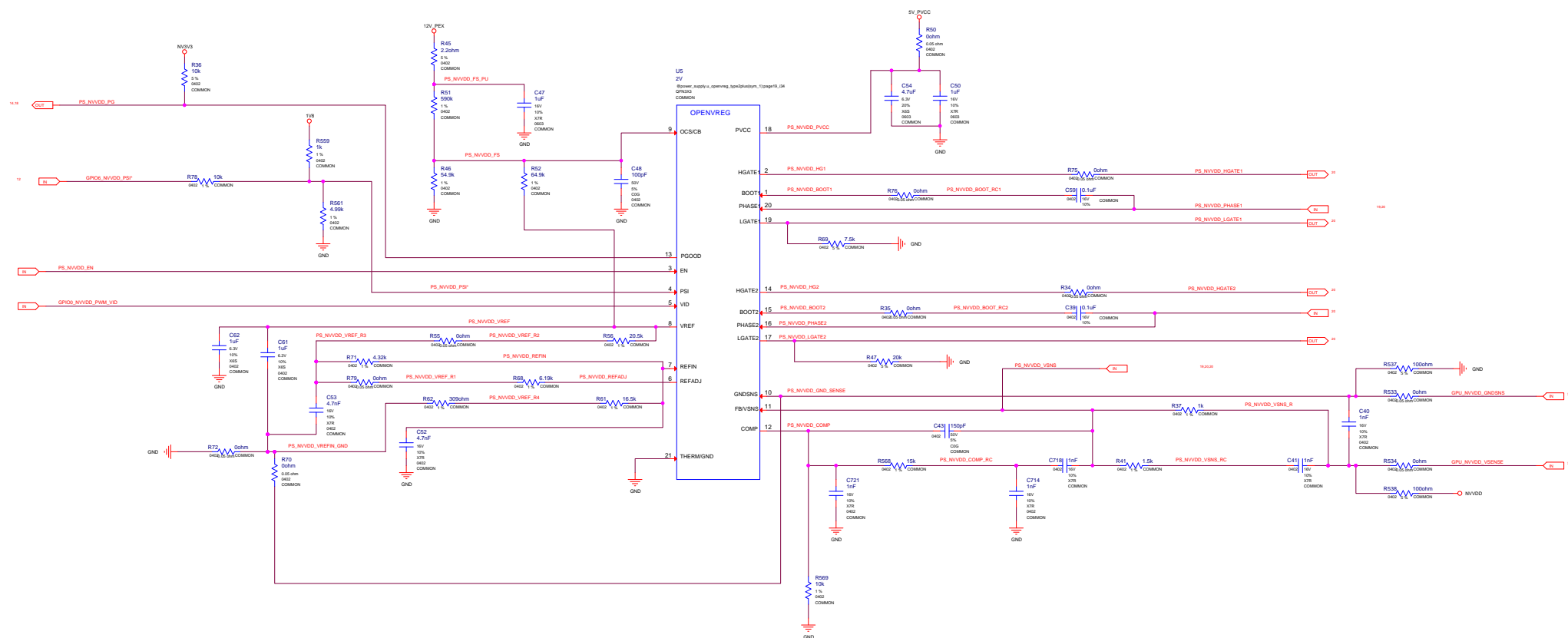
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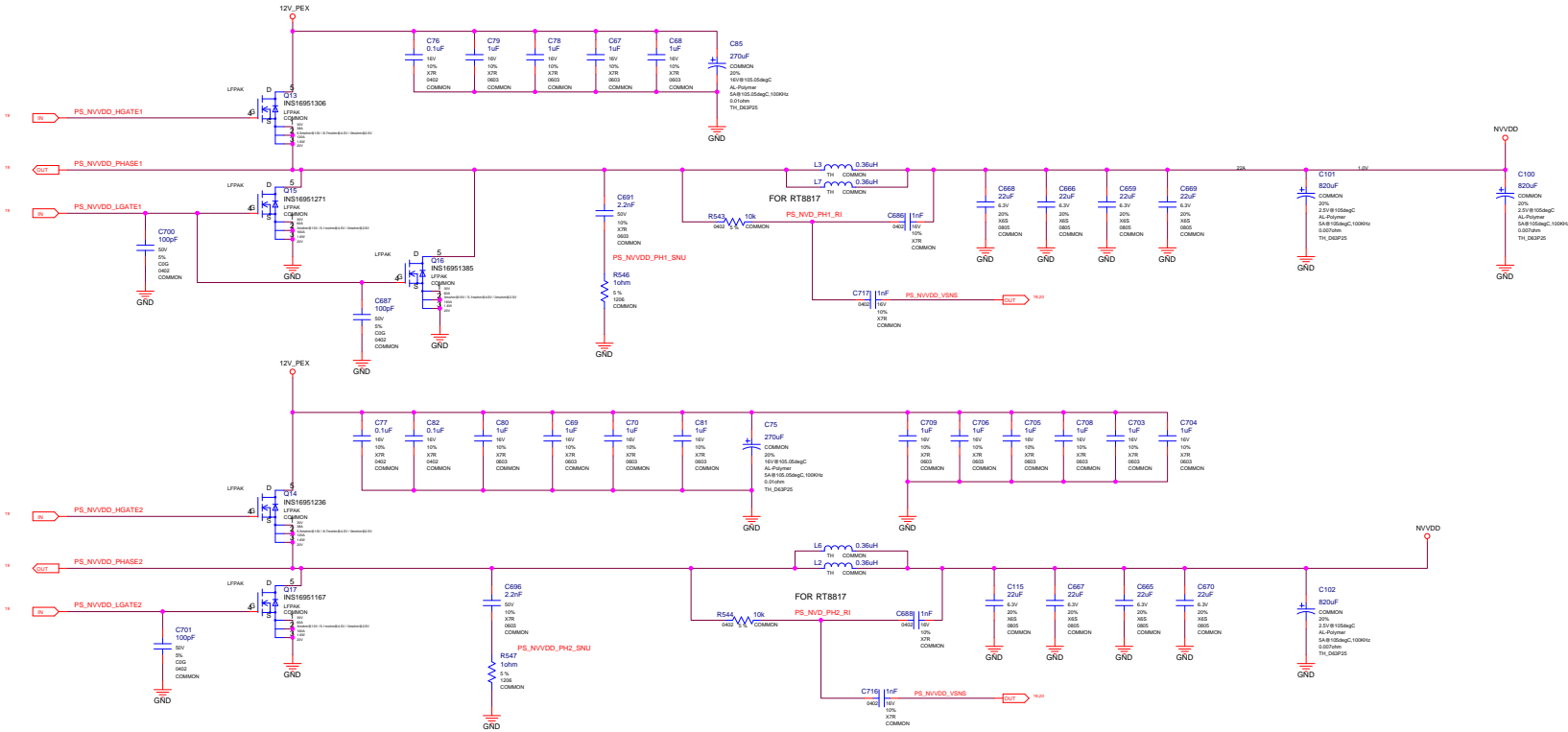


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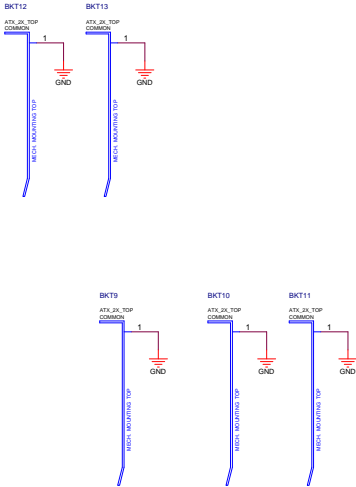
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Mechanical



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