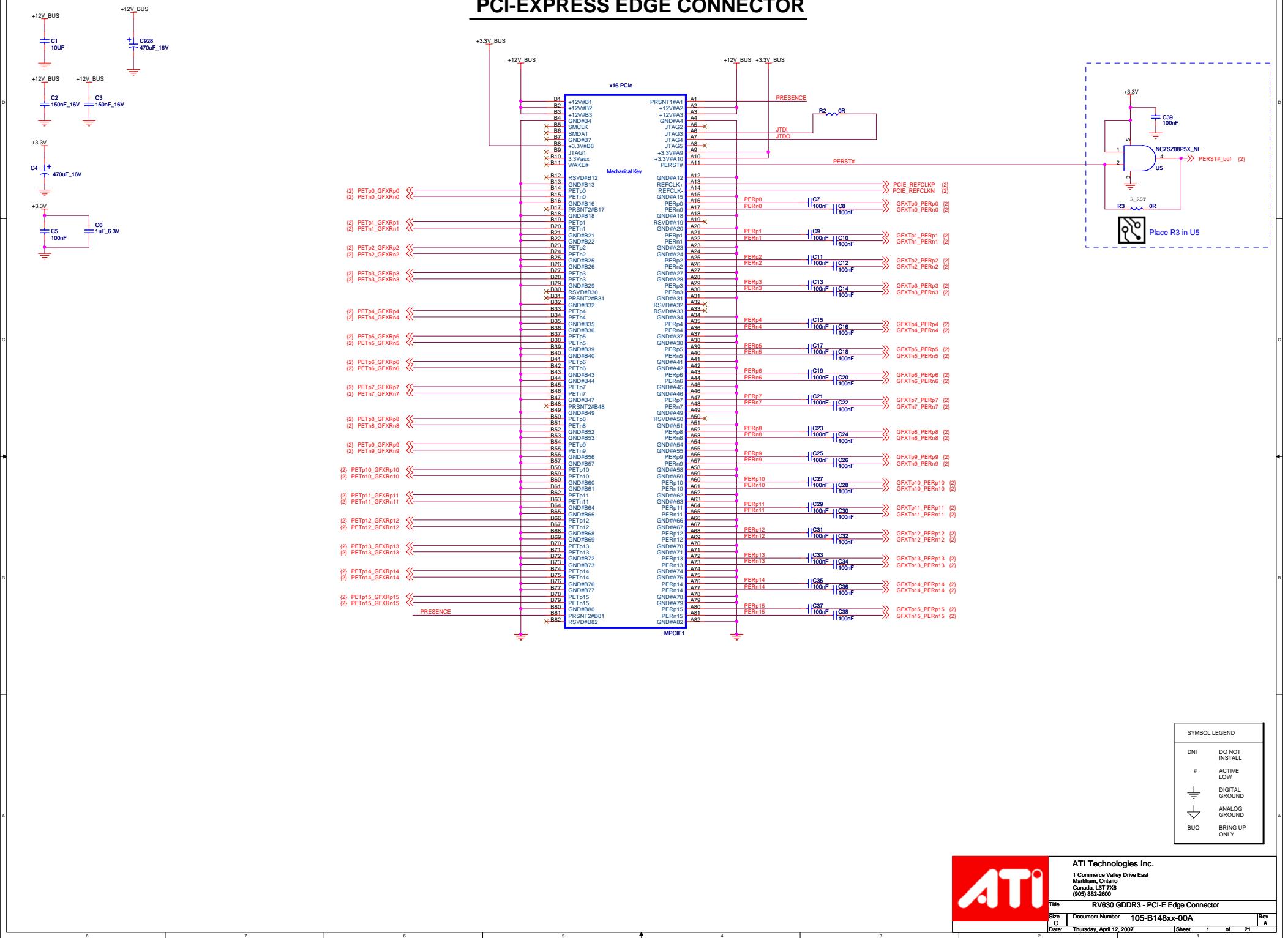
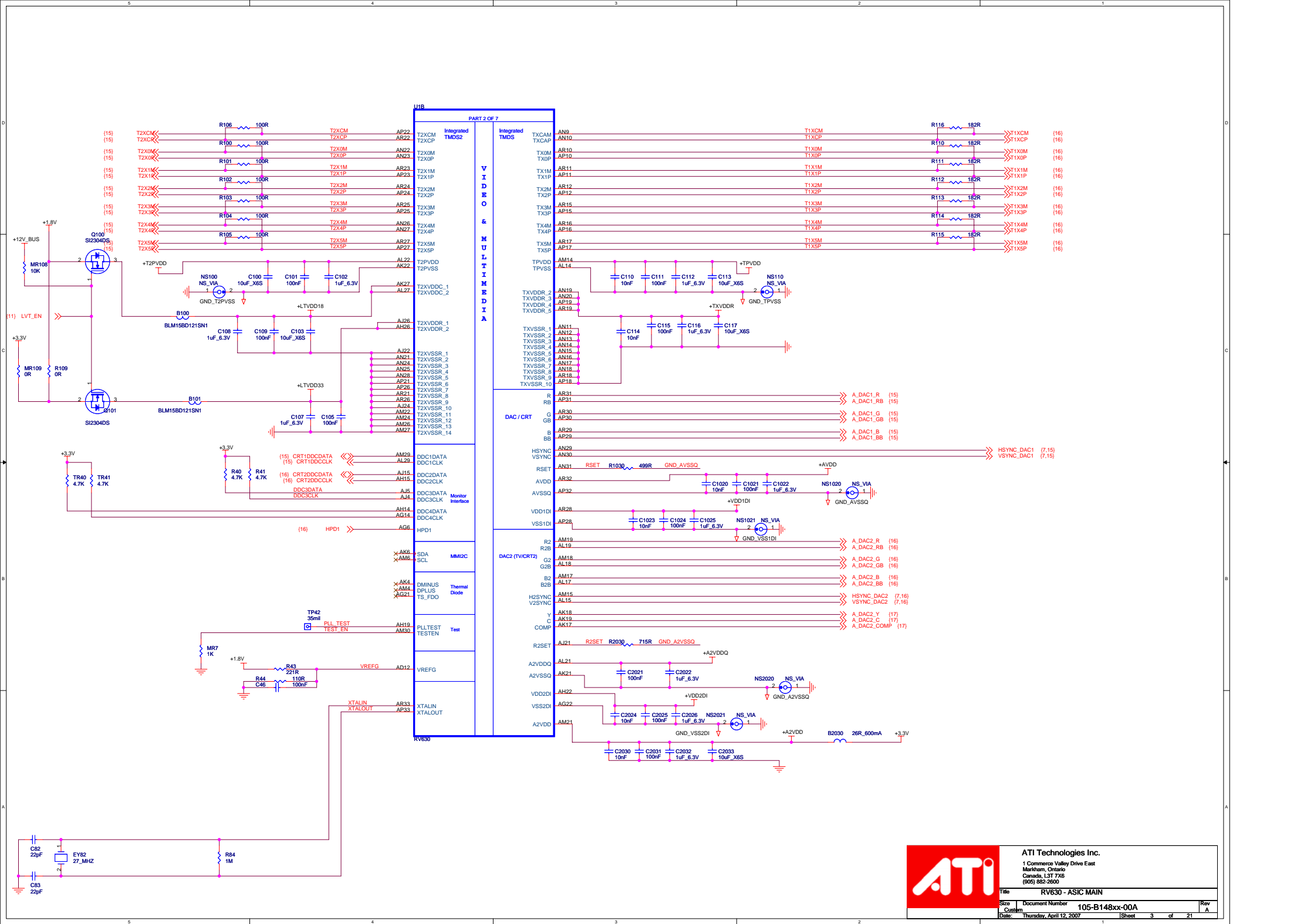


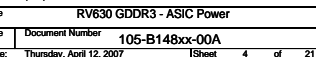
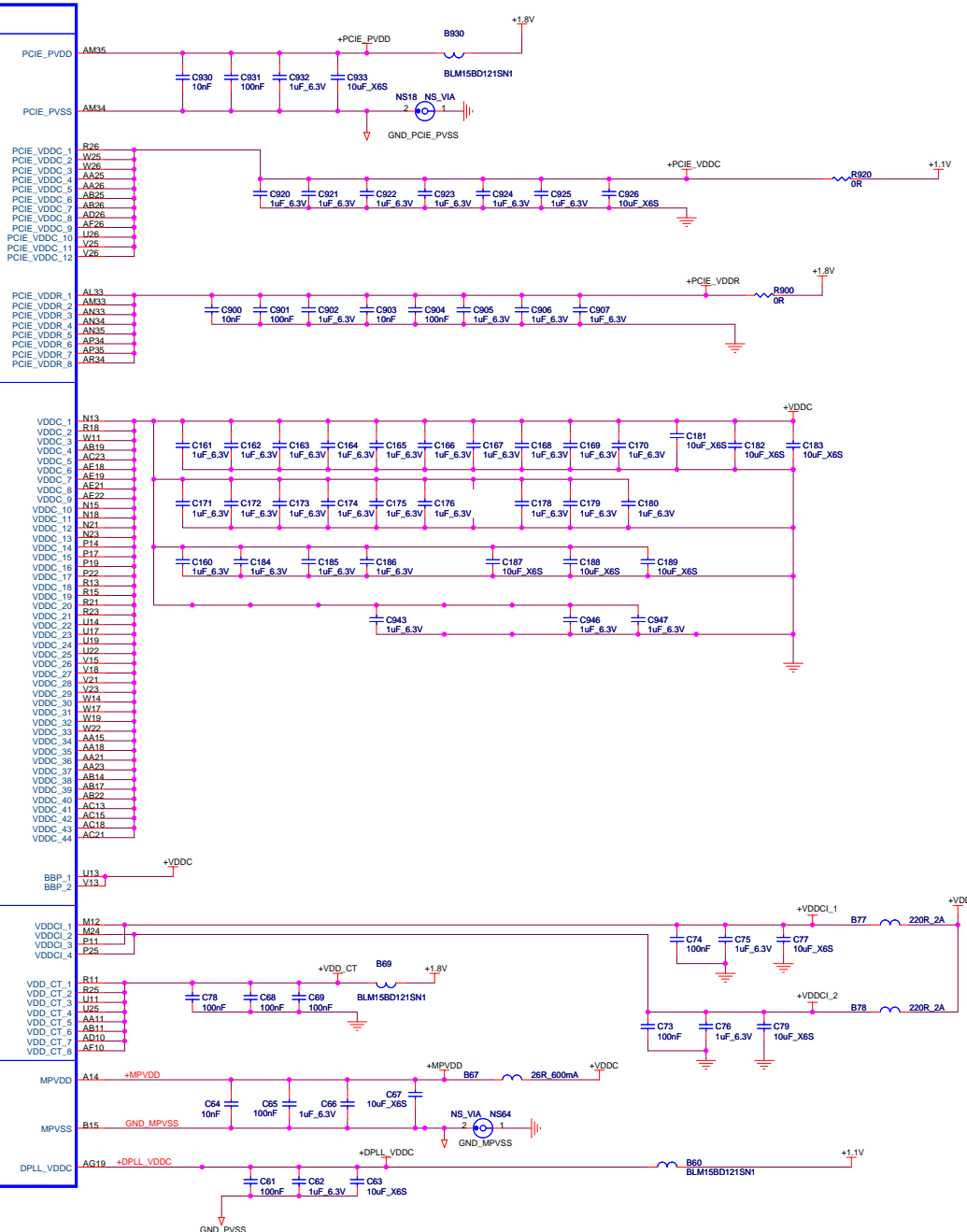
PCI-EXPRESS EDGE CONNECTOR

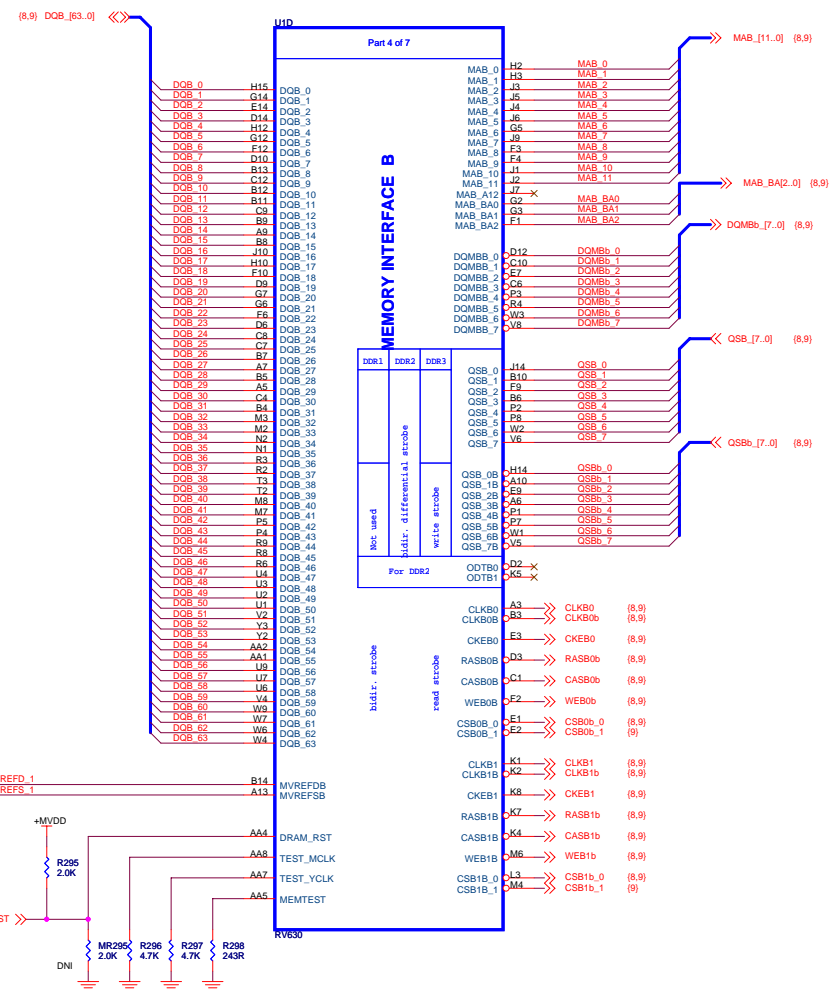
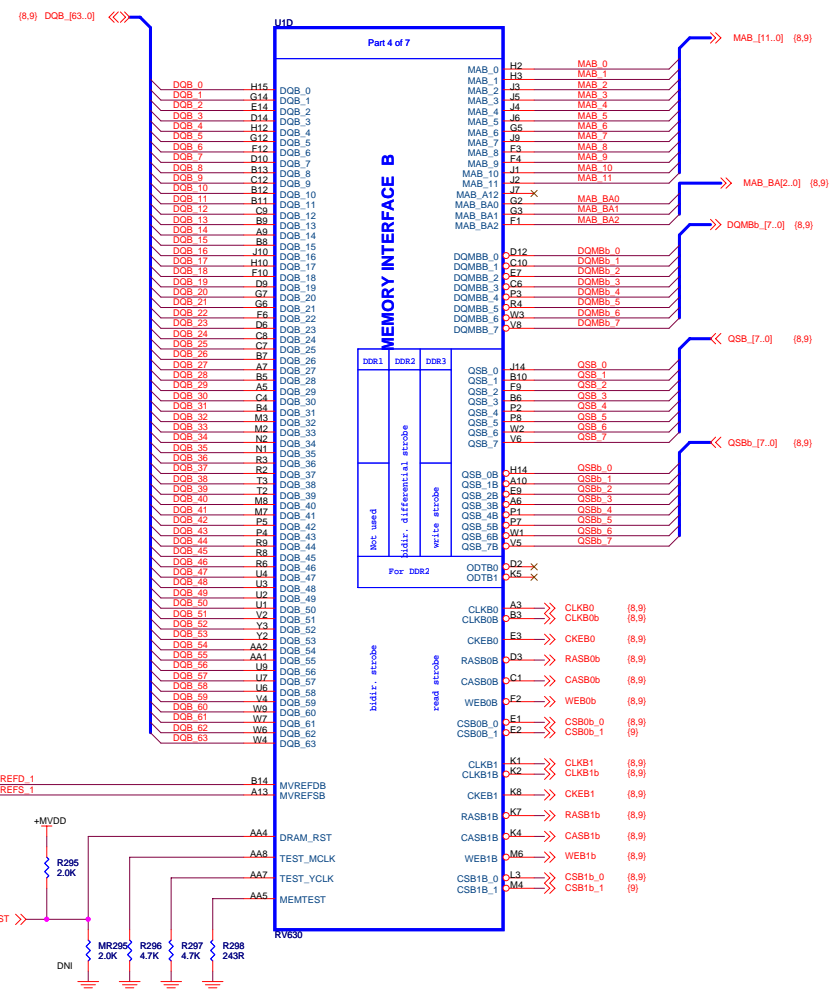


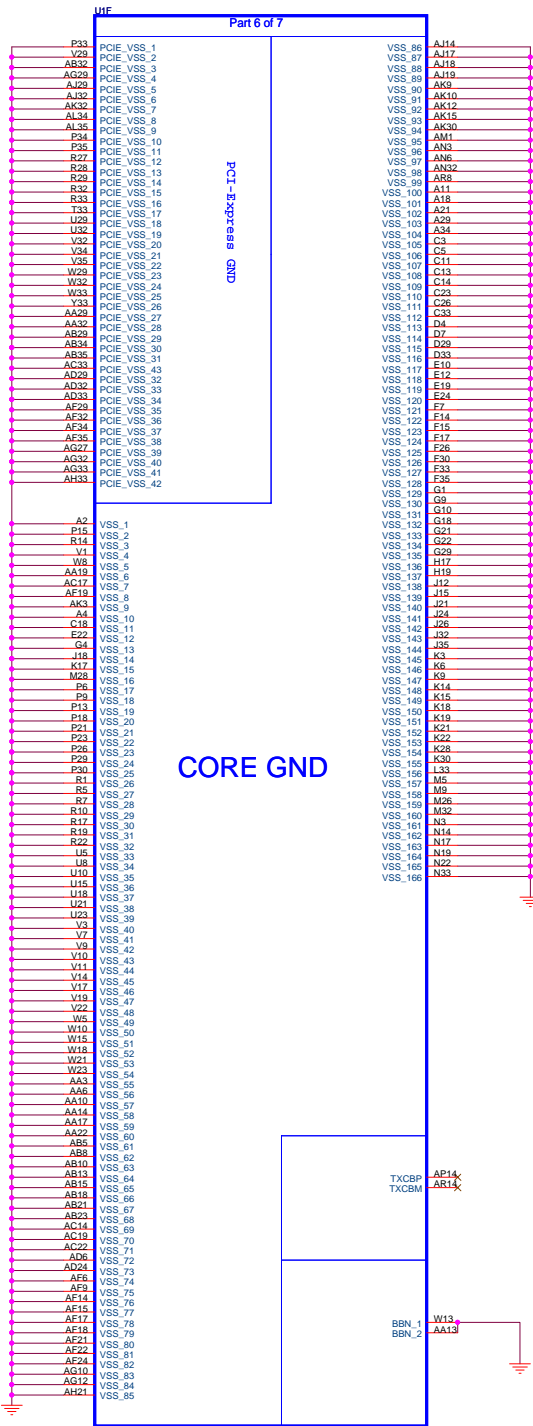


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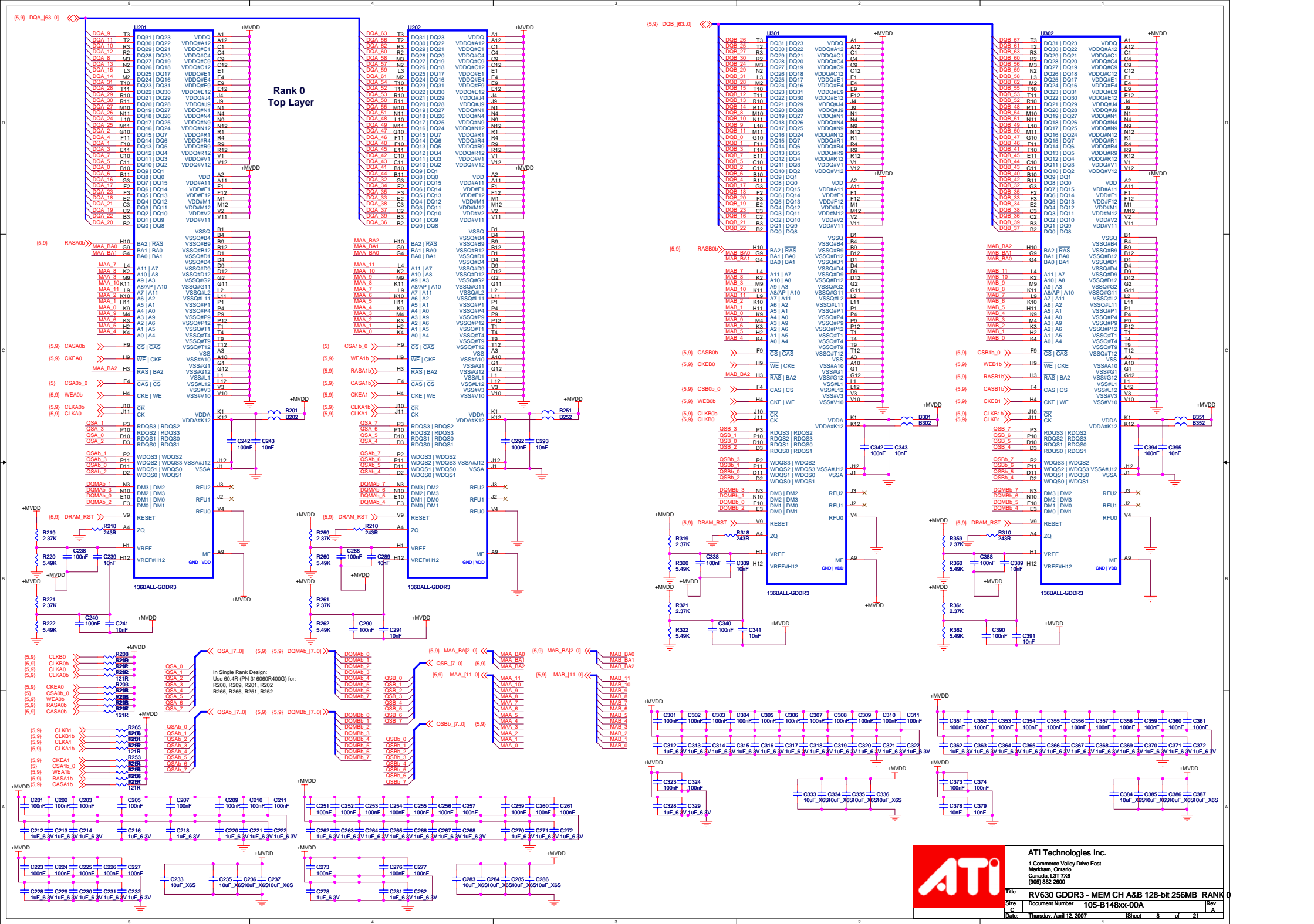
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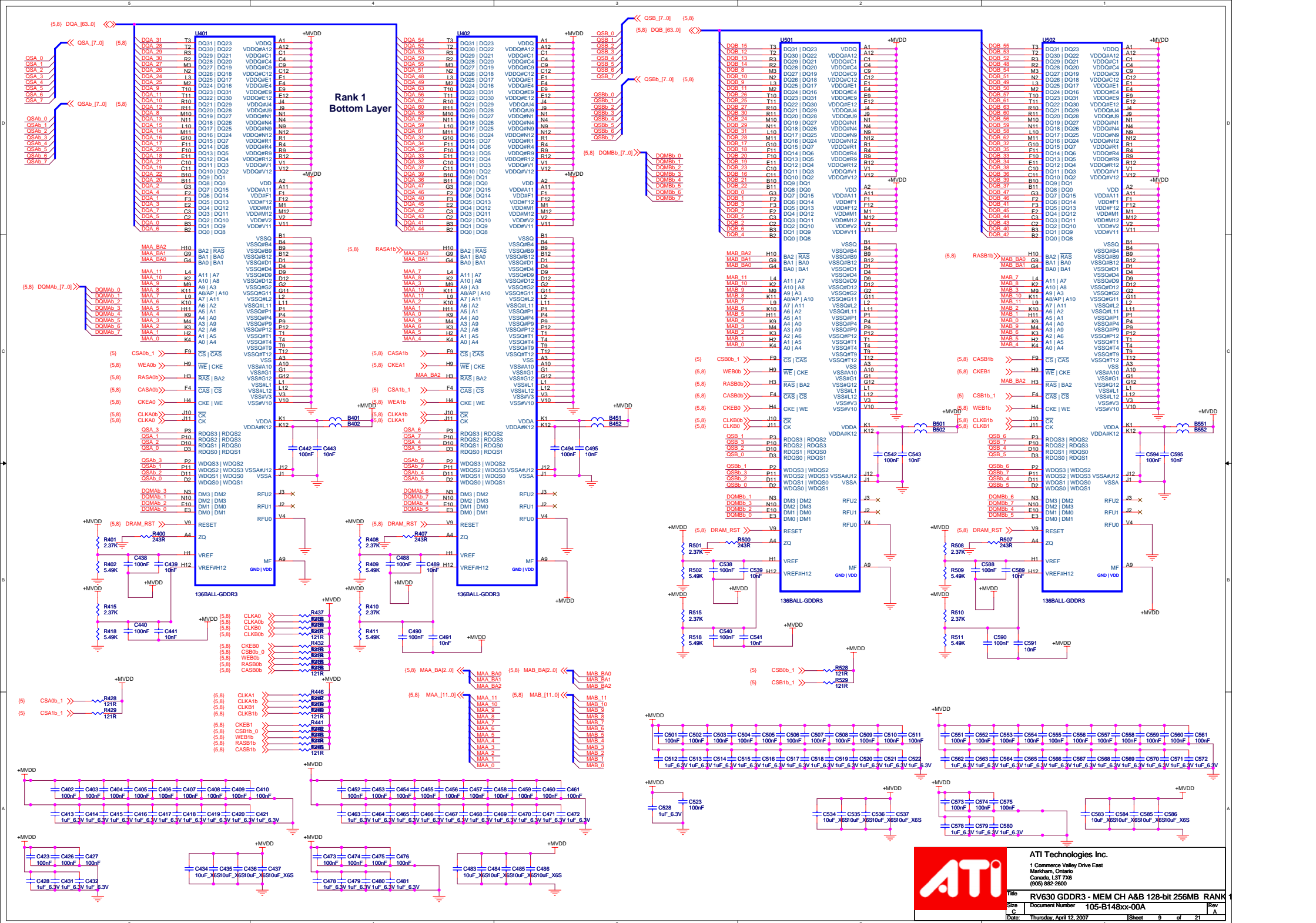


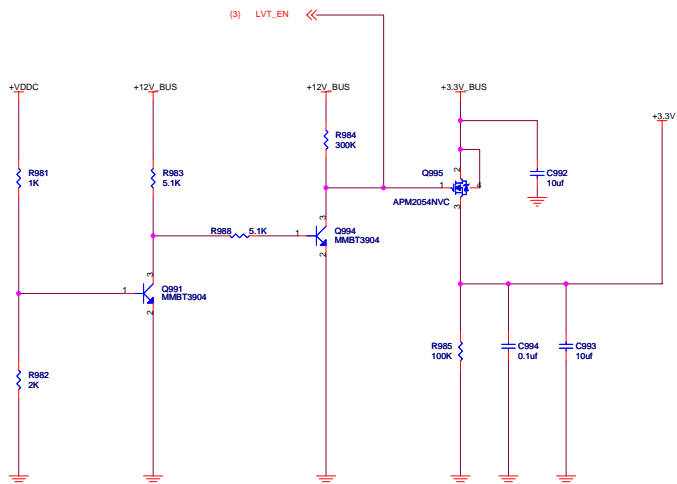


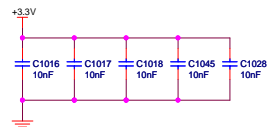
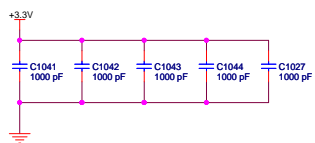
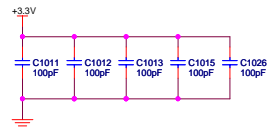
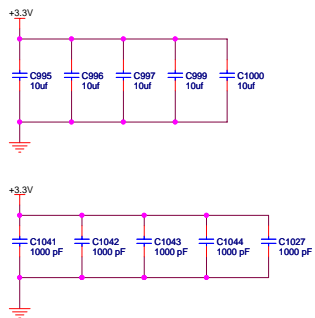
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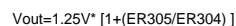
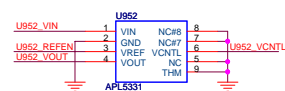
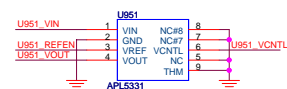
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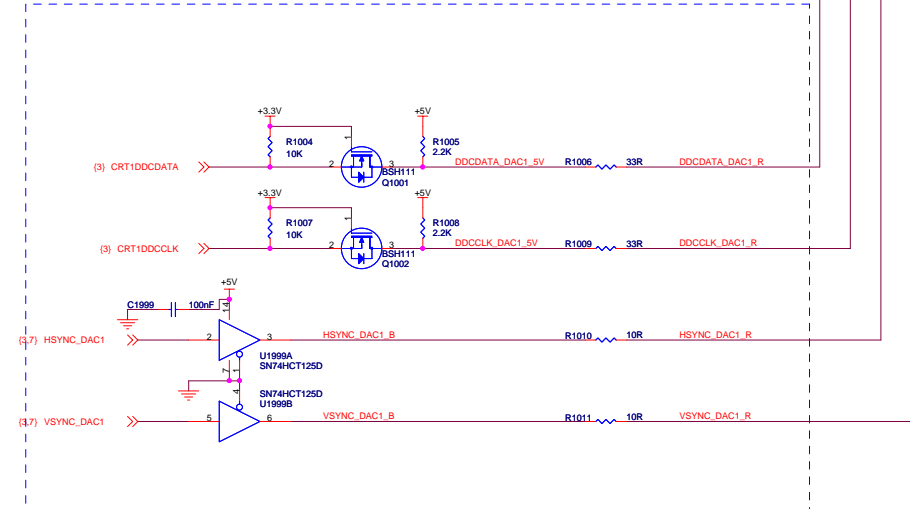
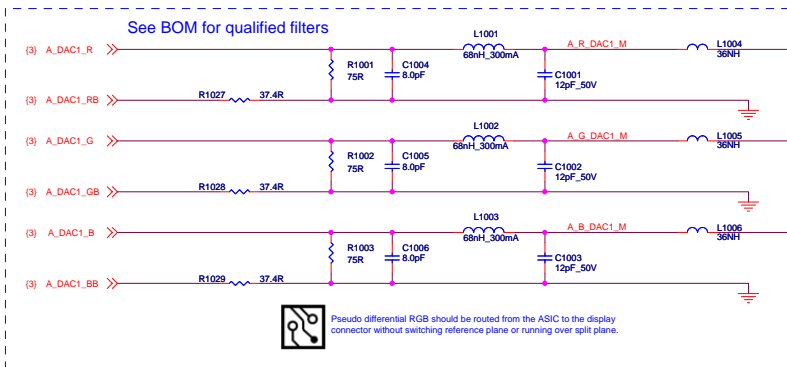




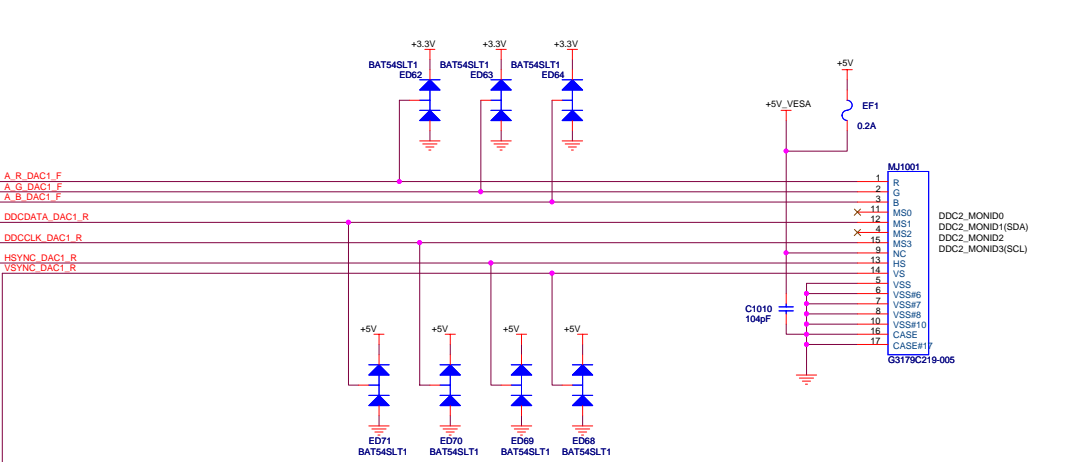


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Title		RV630 GDDR3 - Linear Regulators	
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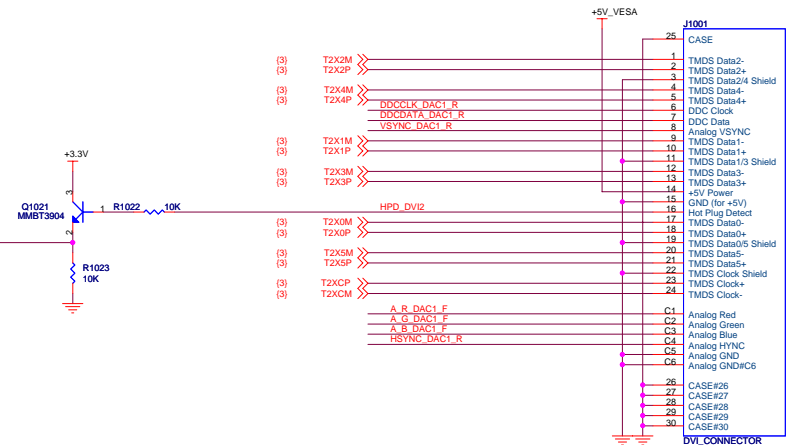


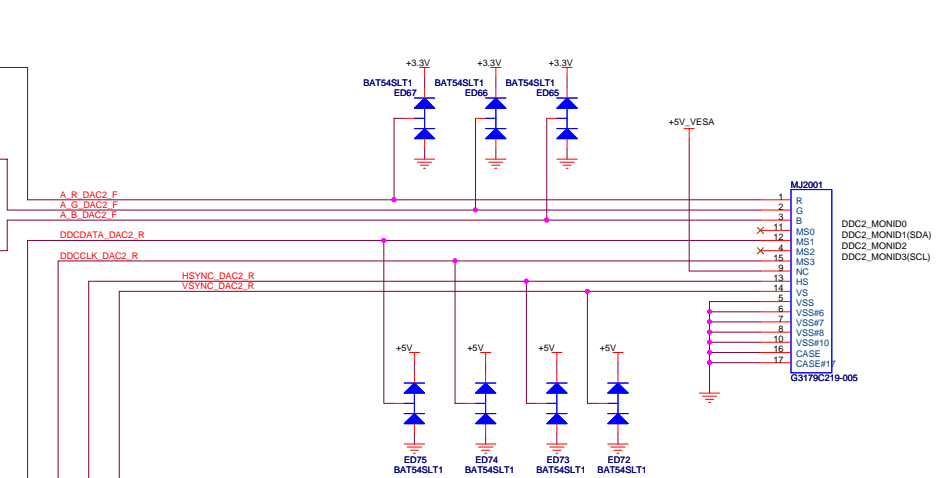
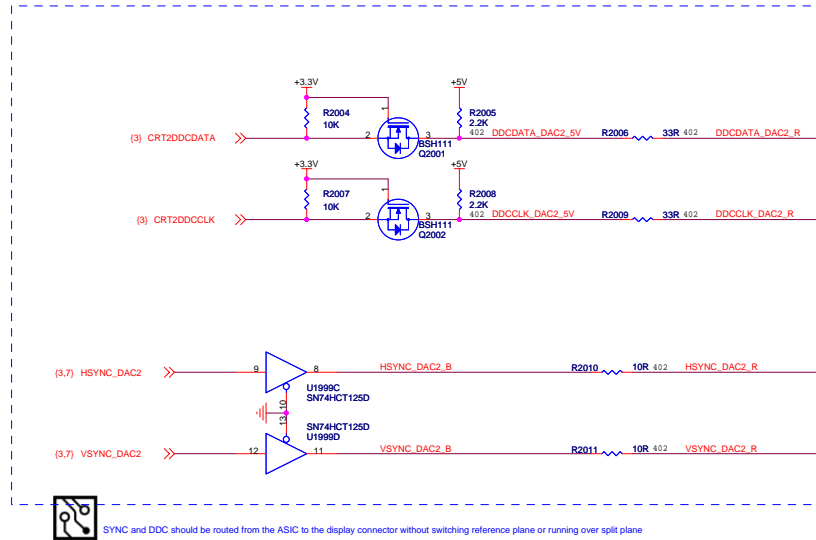
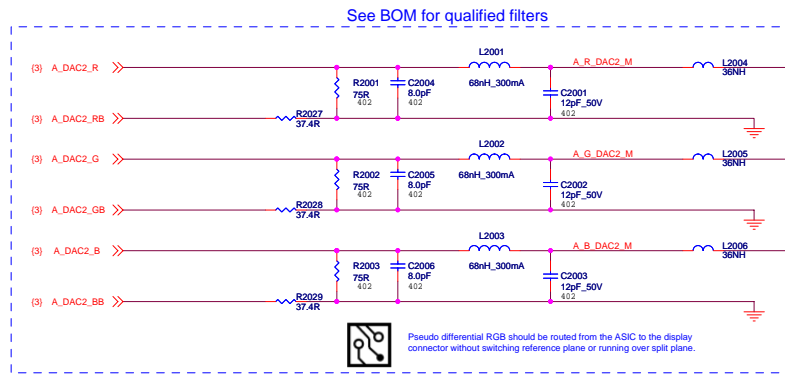
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display SDA	SDA	SDA	Optional
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	Optional
9	N/C	+5V	+5V	+5V	Optional
Support	No	Yes	Yes	No	Yes

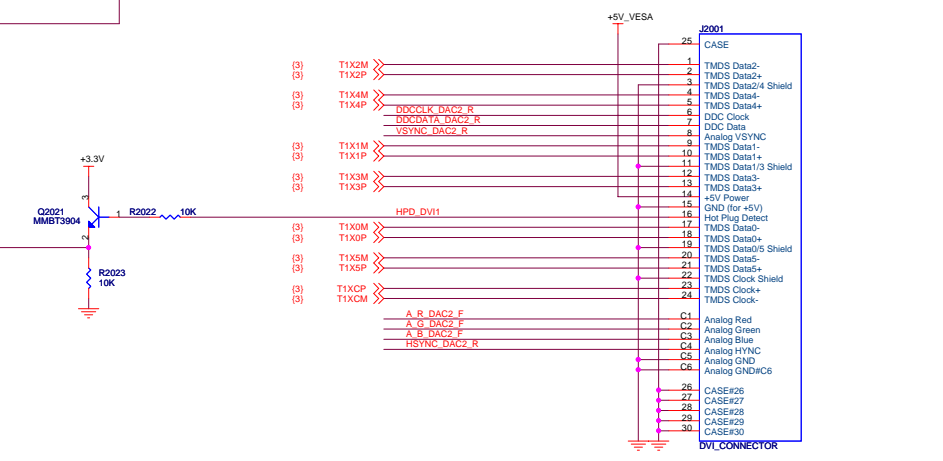
Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

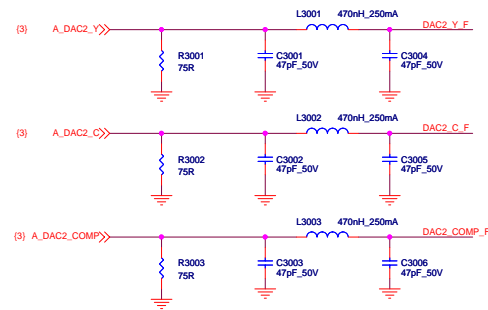




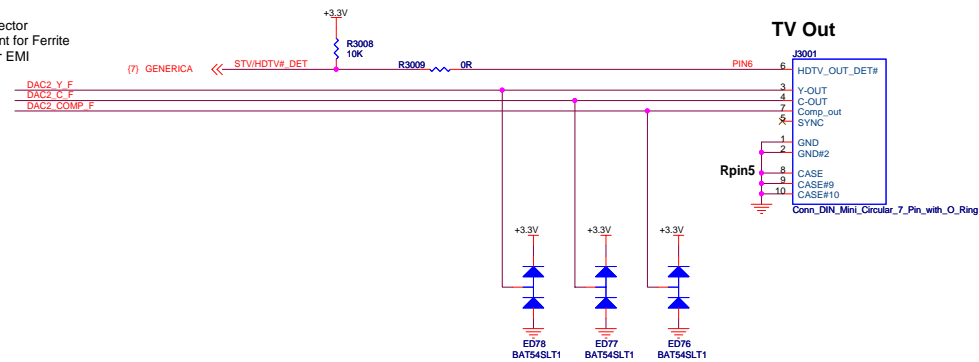
DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional	Optional
12	Monitor ID bit 1	Data from display SDA	SDA	Optional	Optional
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional	Optional
15	Monitor ID bit 3	Open	SCL	Optional	Optional
9	N/C	+5V	+5V	+5V	Optional
Hardware Support	No	Yes	Yes	No	Yes
		50mA min 1A max	50mA min 1A max	50mA min 1A max	

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





Place near connector
OR leaves footprint for Ferrite
Beads if req'd for EMI



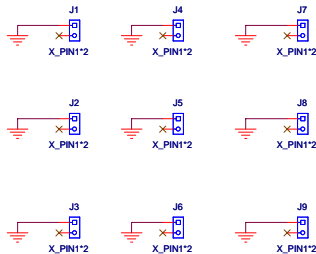
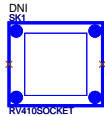
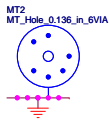
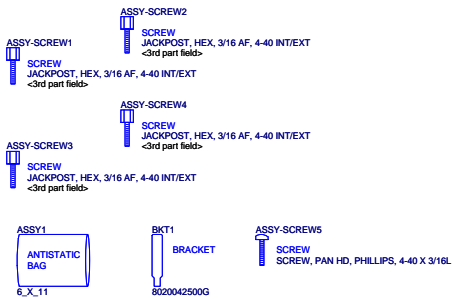
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DVI/DVI SCREWS with top tab



<Variant Name>

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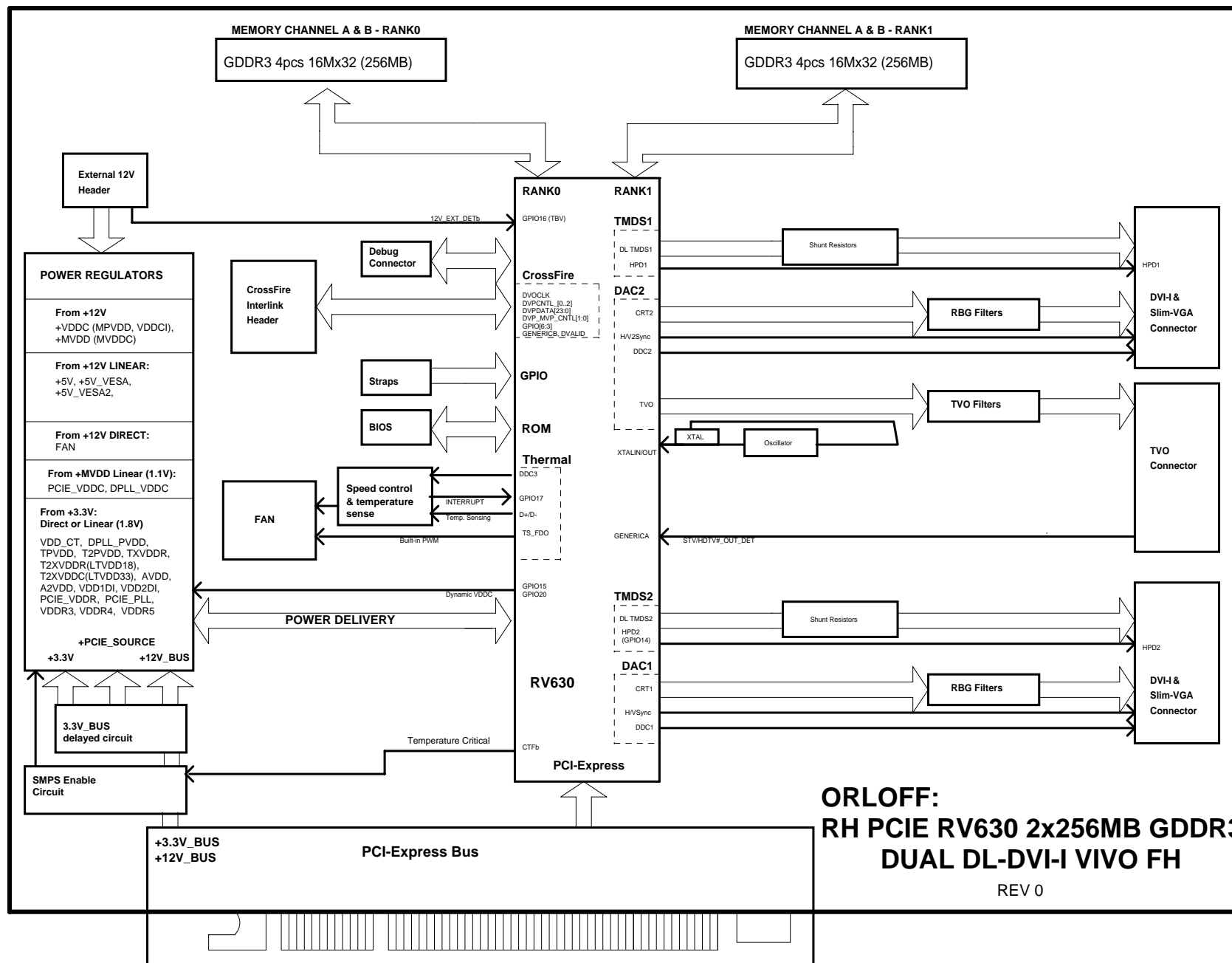
Title	Schematic No.	Date:
RH PCIE RV630 2x256MB GDDR3 DUAL DL-DVI-I VIVO FH	105-B148xx-00A	Thursday, April 12, 2007

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.

Rev A

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/02/06	Initial design for RV630 GDDR3



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Title RV630 GDDR3 - BLOCK DIAGRAM

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