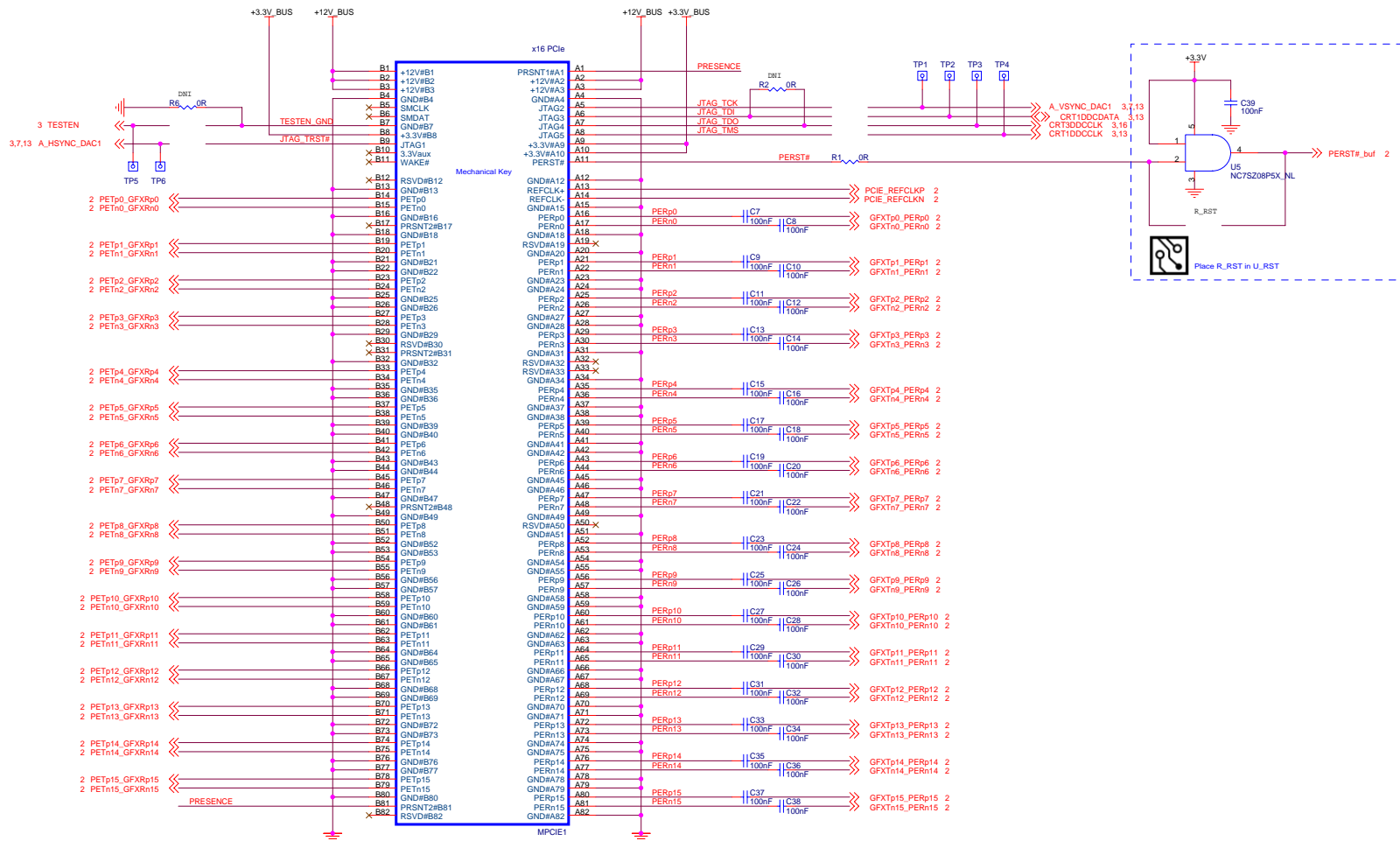
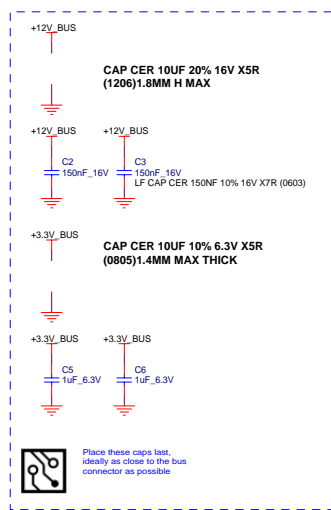
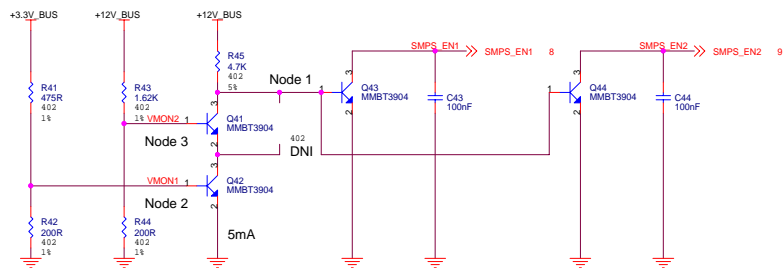


PCI-EXPRESS EDGE CONNECTOR



POWER SEQUENCING



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation. Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be held low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

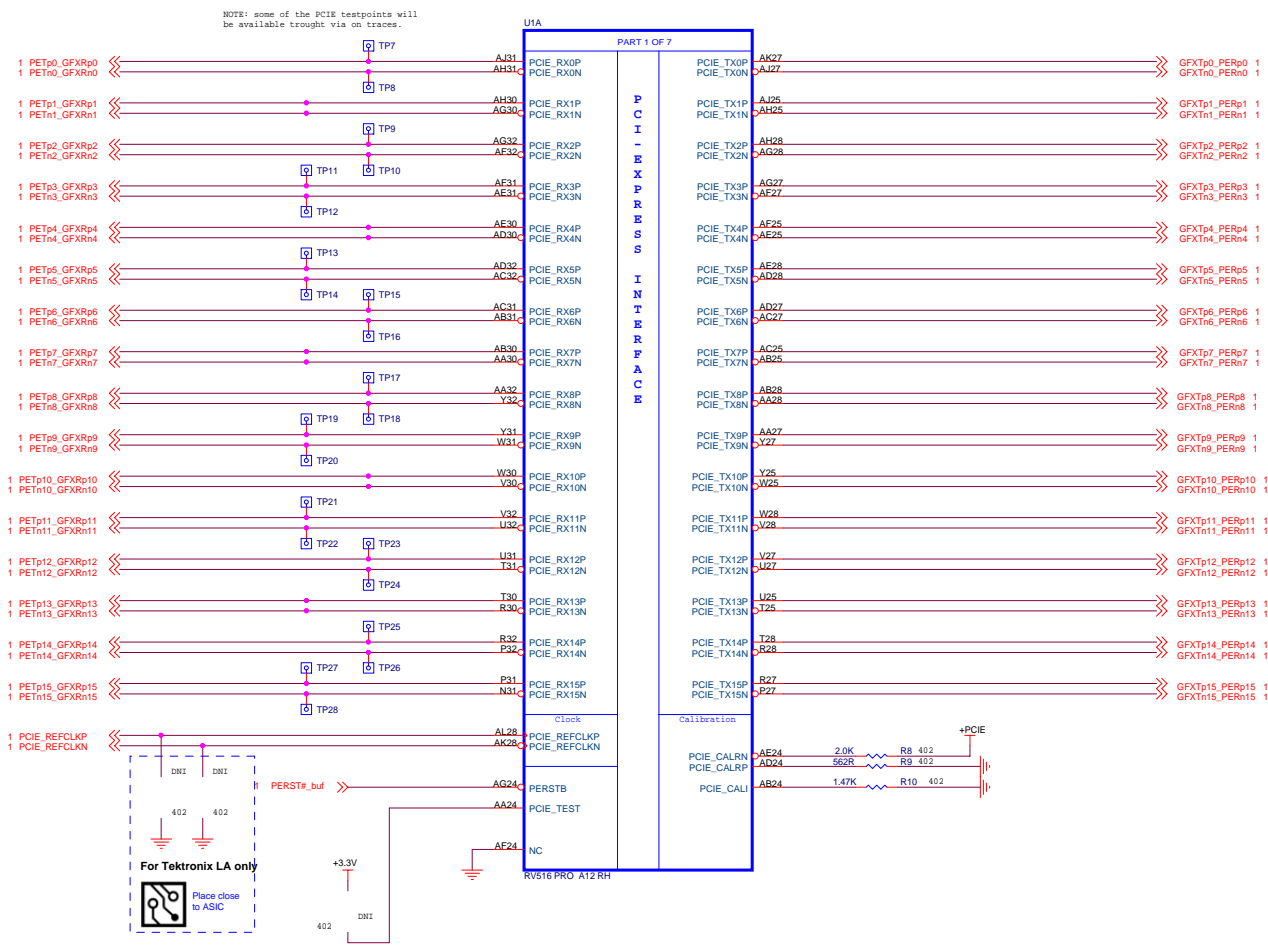
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

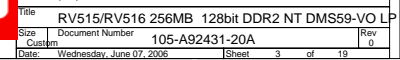
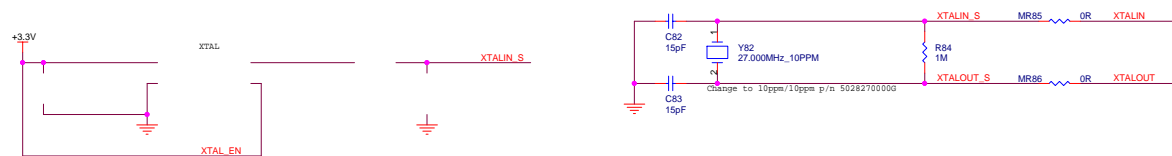


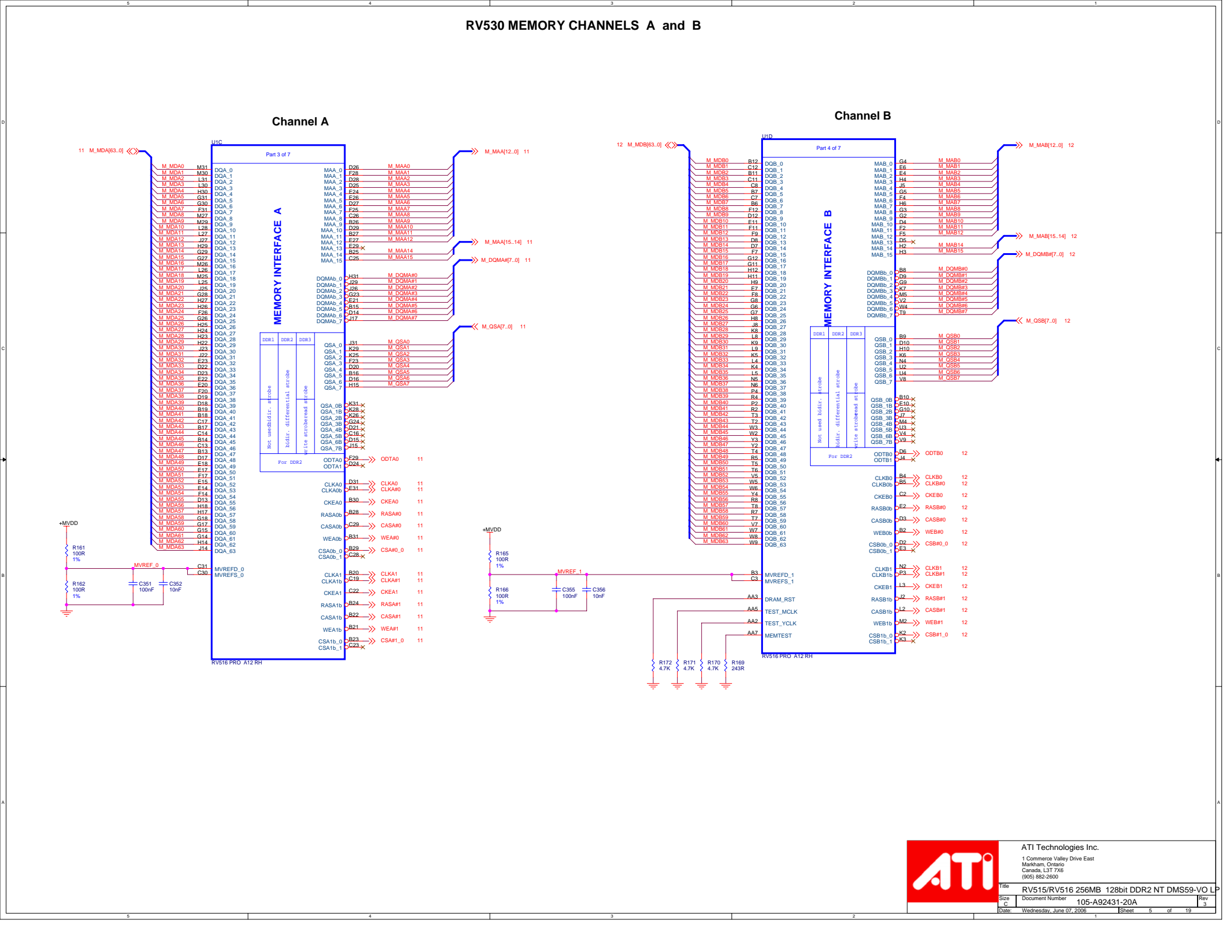
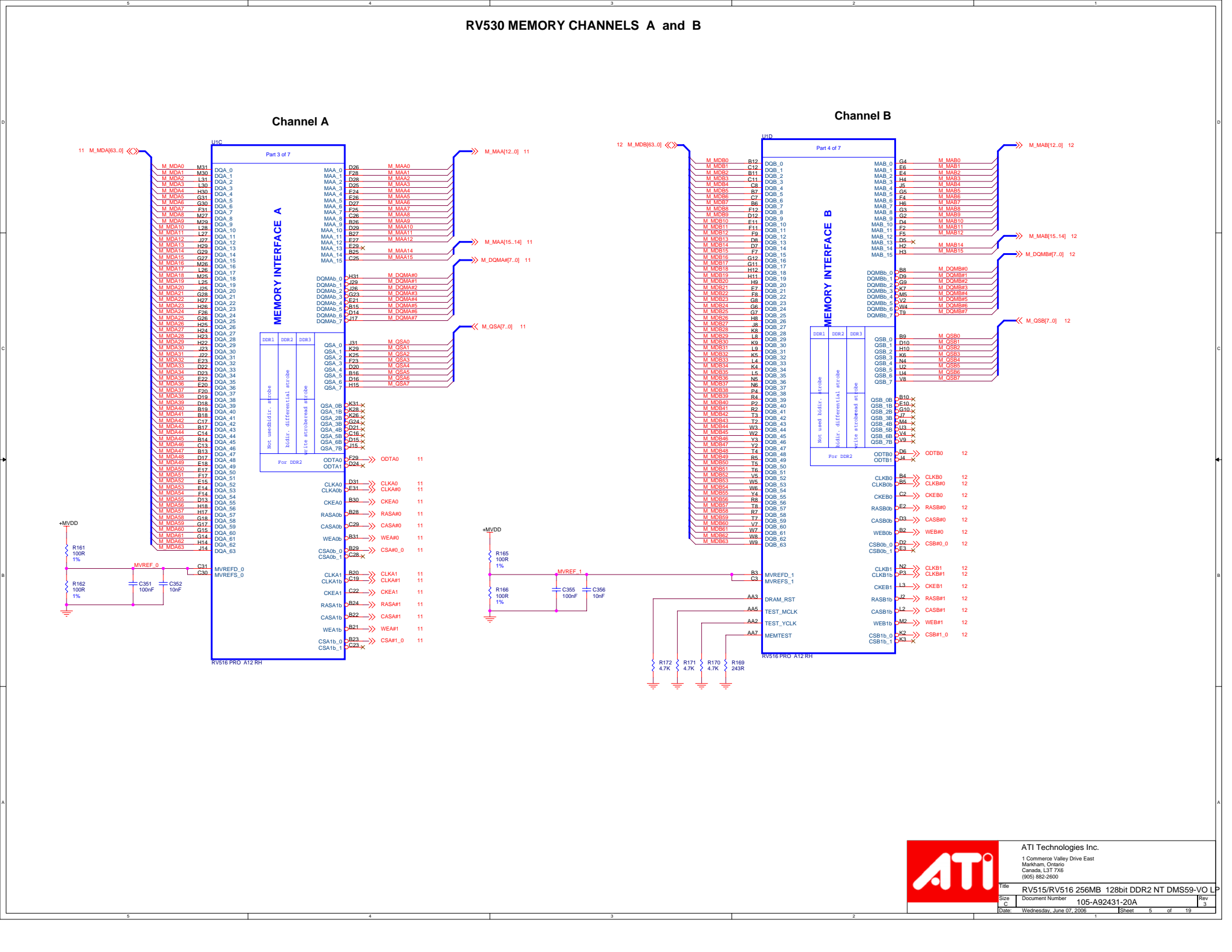
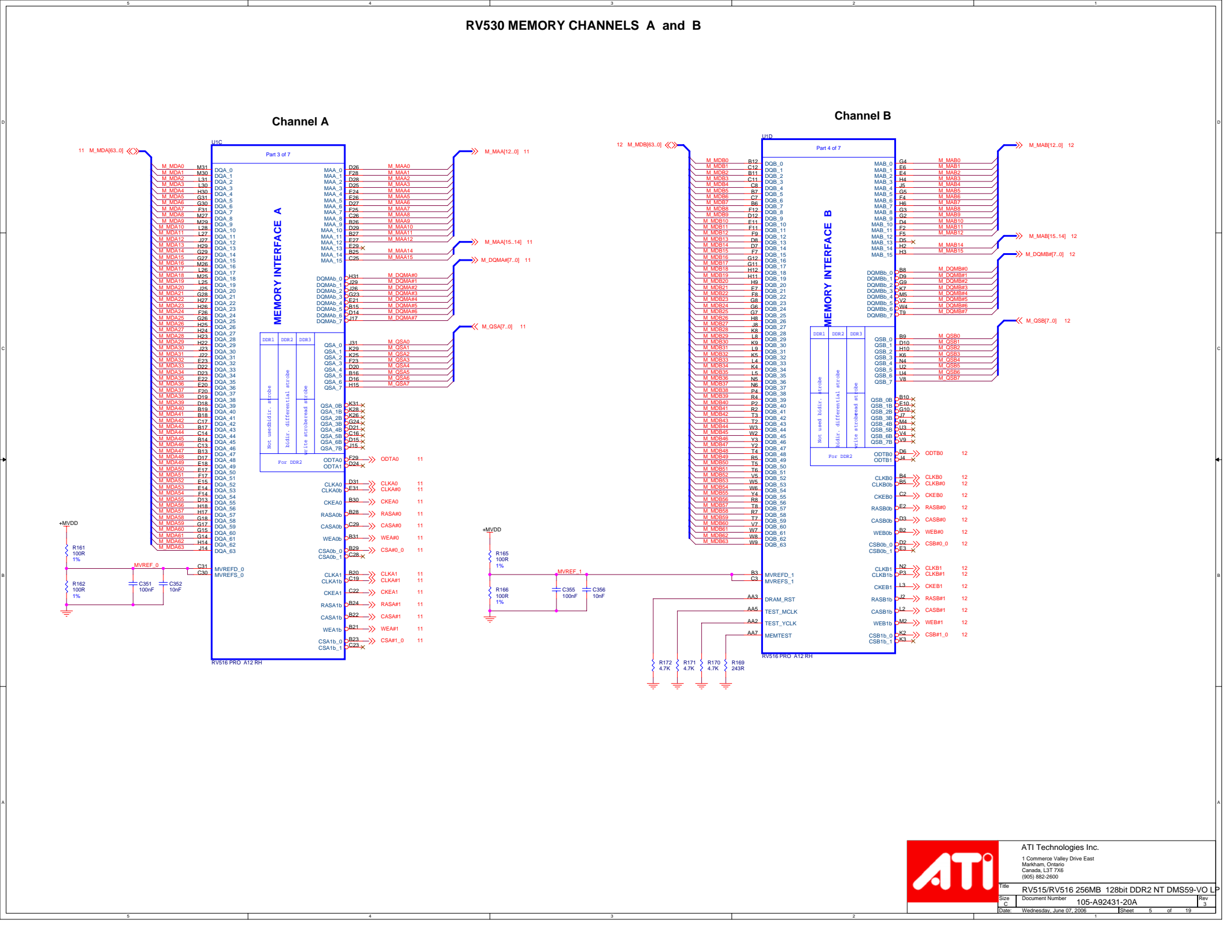
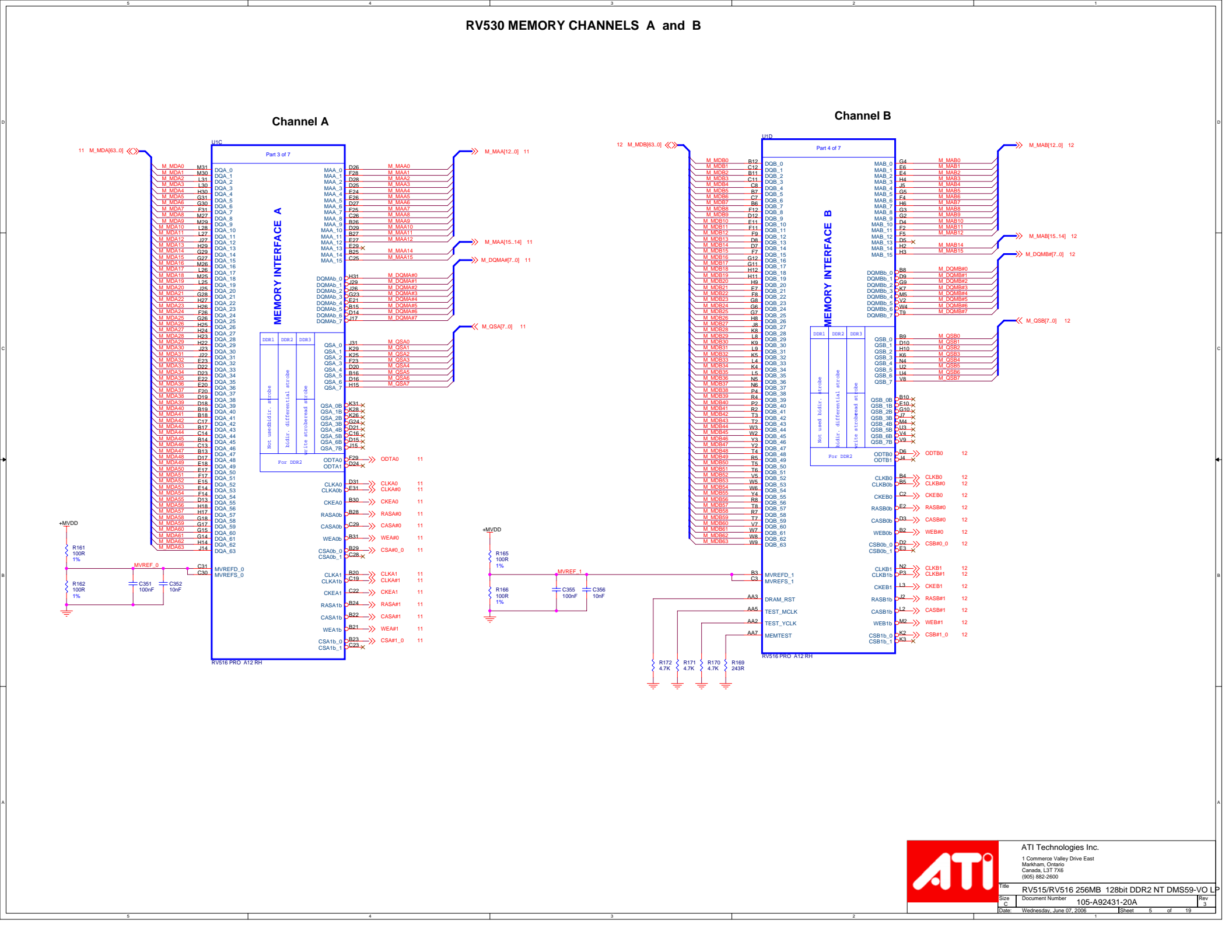
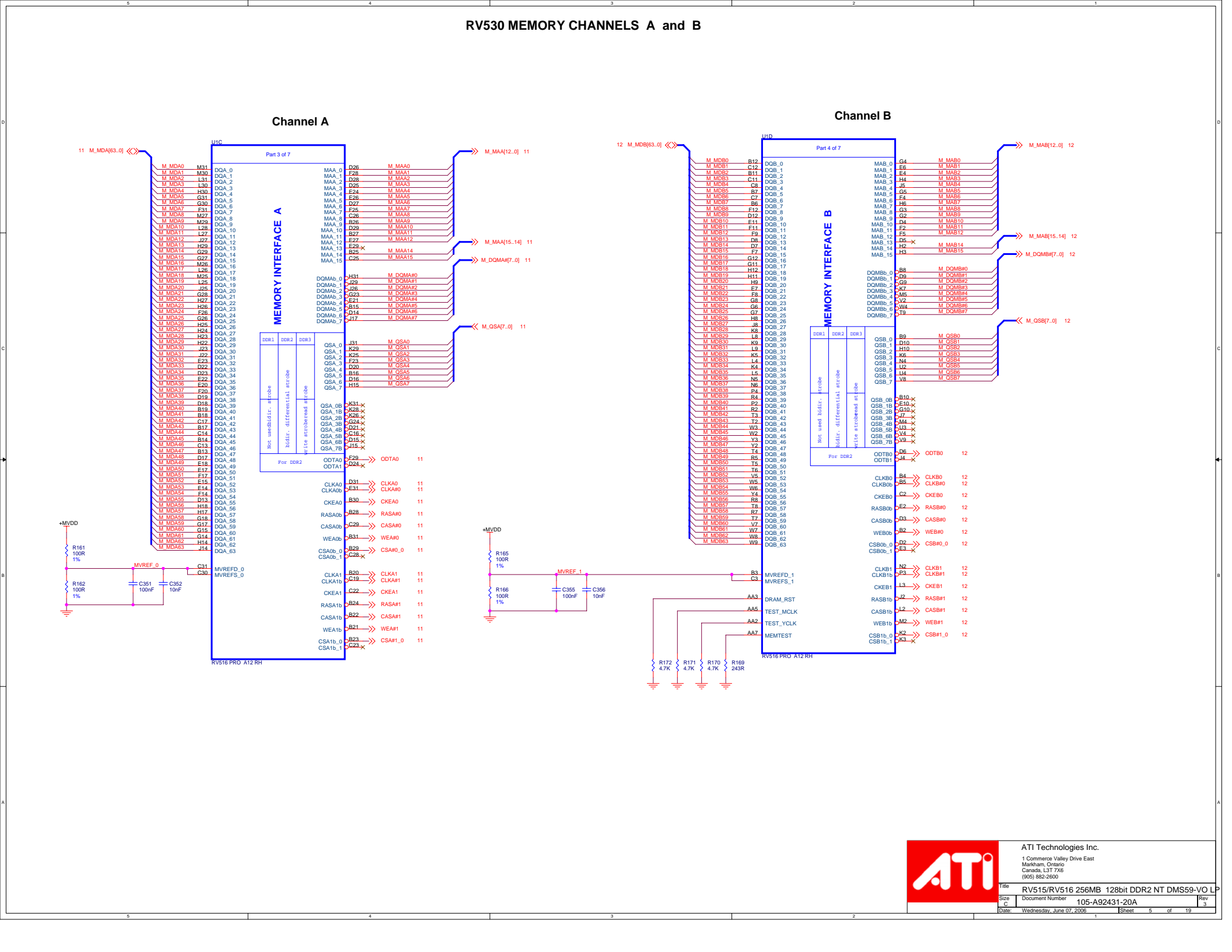
ATI Technologies Inc.

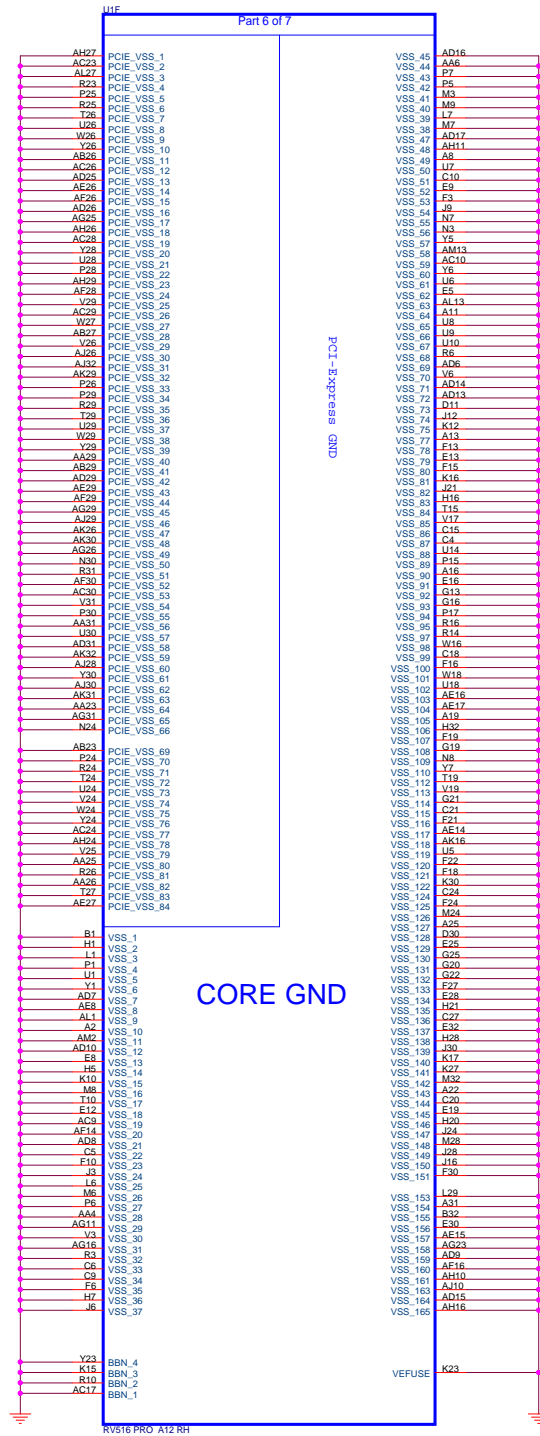
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2660

Title	RV515/RV516 256MB 128bit DDR2 NT DMS59-VO LP		
Size	Document Number	105-A92431-20A	Rev 3
Date	Wednesday, June 07, 2006	Sheet 1 of 19	









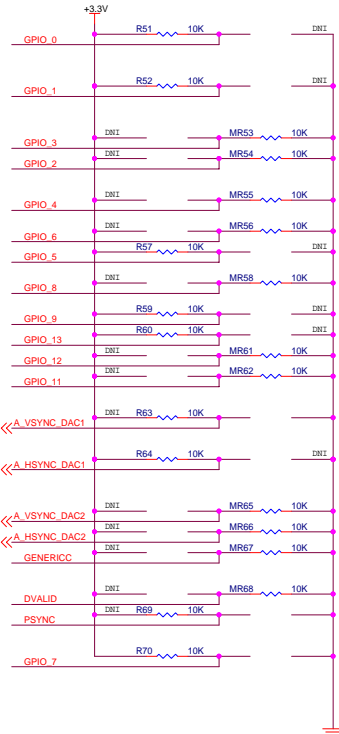
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV515/RV516 256MB 128bit DDR2 NT DMS59-VO L		
Size	Document Number		
C	105-A92431-20A		
Date	Wednesday, June 07, 2006	Sheet	6 of 19
			Rev 3

DVPDATA	ALTERNATE USE
DVPDATA_0	-
DVPDATA_1	-
DVPDATA_2	-
DVPDATA_3	-
DVPDATA_4	-
DVPDATA_5	-
DVPDATA_6	-
DVPDATA_7	-
DVPDATA_8	-
DVPDATA_9	-
DVPDATA_10	-
DVPDATA_11	-
DVPDATA_12	-
DVPDATA_13	-
DVPDATA_14	STVHDTV#_OUT_DET (INPUT)
DVPDATA_15	-
DVPDATA_16	TESTOUT(0) (OUTPUT)
DVPDATA_17	TESTOUT(1) (OUTPUT)
DVPDATA_18	TESTOUT(2) (OUTPUT) NTSC/PAL#_TVO_DET (INPUT)
DVPDATA_19	TESTOUT(3) (OUTPUT)
DVPDATA_20	TESTOUT(4) (OUTPUT)
DVPDATA_21	TESTOUT(5) (OUTPUT)
DVPDATA_22	TESTOUT(6) (OUTPUT)
DVPDATA_23	TESTOUT(7) (OUTPUT)

DEBUG BUS	
No testpoint means the net can be accessed from a pad somewhere else	
TP31	DVPDATA_16
TP32	DVPDATA_17
TP33	DVPDATA_18
TP34	DVPDATA_19
TP35	DVPDATA_20
TP36	DVPDATA_21
TP37	DVPDATA_22
TP38	DVPDATA_23

PIN BASED STRAPS



GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI POE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI POE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - Miscellaneous PCI-Express Modes
00: Halt impedance calibration before transmitter is enabled and enable receiver detection (Default setting for Desktop)
01: Allow impedance calibration to continue on in the background AFTER transmitter has been enabled and enable receiver detection.
10: Bypass common-mode detection & receiver detection and halt impedance calibration before TX_EN
11: Short-circuit internal feedback and halt impedance calibration before TX_EN and enable receiver detection.

GPIO(4) - DEBUG_ACCESS: 0 for normal operation, 1 for debug mode

GPIO(6:5) - PLL_BIAS_RD (Reduced mirror bias setting for PHY PLL) ATI POE FEATURE III
Provide 4 different BIAS settings - Set to 00 for R520

GPIO(8) - FORCE_COMPLIANCE: 0 for Normal operation, 1 for Force into Compliance Mode

GPIO(9:13:11) - ROMIDCFG(3:0)
1001 - 1M AT72SF1024 ROM (Almael)
1010 - 1M AT45DB011 ROM (Almael)
1011 - 1M M25P10 ROM (ST)
1100 - 512K M25P05 ROM (ST) (ATI default)
1101 - 1M SST45LF010 ROM (SST), 1M W45B512 ROM (Winbond), 512K W45B012 ROM (Winbond)
1110 - 1M SST35VF010 ROM (SST), 512K SST29VF512 ROM (SST)
1111 - 1M NX25F011B ROM (NexFlash)

VSYN - VIP_DEVICE
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

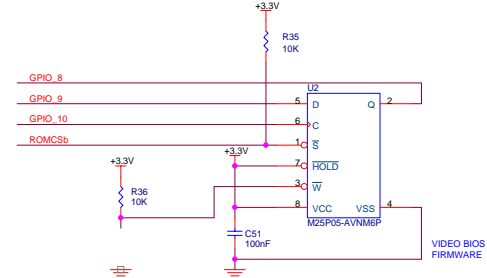
HSYNC - DWINGRD ATI Feature I
This straps allow a Workstation bonded part to be downgraded to a normal part on a board. This allow inventory management to better balance demand.
0 - Device remain a Workstation grade part
1 - Part is downgraded to a Normal part

H2SYNC_V2SYNC_GENERIC - Star Memory System repair mode ATI Feature II
000 - Default

Memory Vendor Straps for DDR2, 16Mx16 and 32Mx16:
ATI Board Feature II

TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper position 2-3)
1 - NTSC TVO (Jumper position 1-2)

[31:24]B MC_MISC_0	MEMTYPE[1:0] (PSYNC-DVALID)	Memory
20h	[0:0]	Common and Infineon 16Mx16 2.0V
21h	[0:1]	Samsung 16Mx16
22h	[1:0]	Infineon 16Mx16 1.8V
23h	[1:1]	Hynix 16Mx16
24h	[0:0]	Micron 16Mx16
25h	[0:1]	Elpida 16Mx16
26h	[1:0]	Reserved
27h	[1:1]	Reserved
28h	[0:0]	Common 32Mx16
29h	[0:1]	Samsung 32Mx16
2Ah	[1:0]	Infineon 32Mx16
2Bh	[1:1]	Hynix 32Mx16
2Ch	[0:0]	Micron 32Mx16
2Dh	[0:1]	Elpida 32Mx16
2Eh	[1:0]	Reserved
2Fh	[1:1]	Reserved



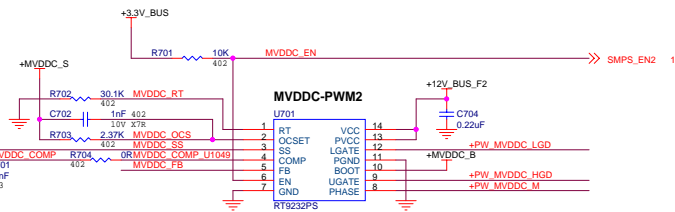
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title: RV515/RV516 256MB 128bit DDR2 NT DMS59-VOL P
Size: Document Number 105-A92431-20A
Date: Wednesday, June 07, 2006 Sheet 7 of 19

MVDDC-PWM1

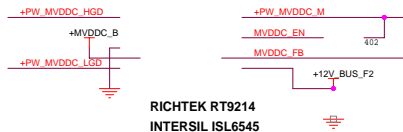


MAXIM MAX1954
MAXIM MAX1954A



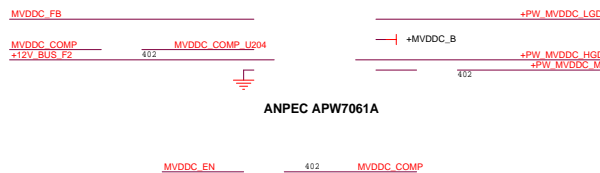
INTERSIL ISL6522
RICHTEK RT9232A
ANPEC APW7062A
ANPEC APW7062B

MVDDC-PWM3

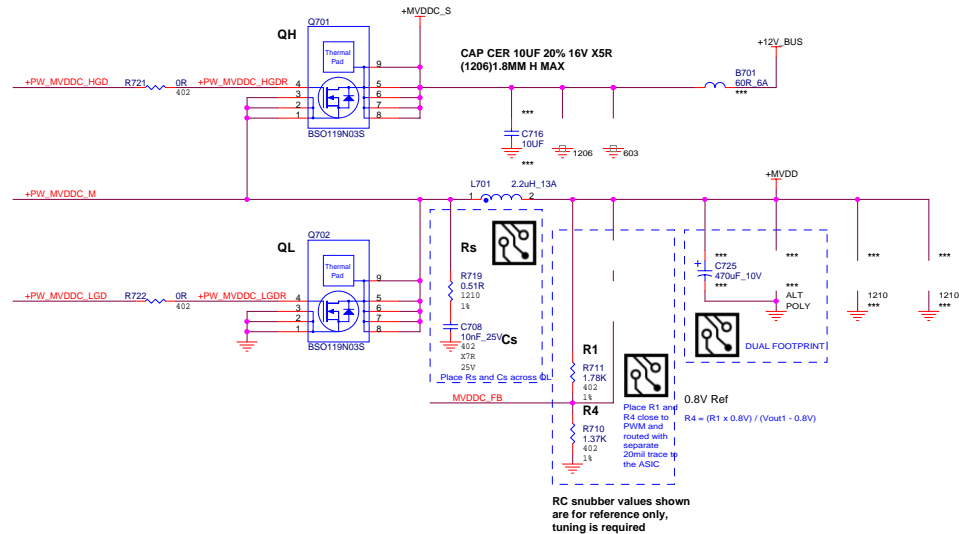


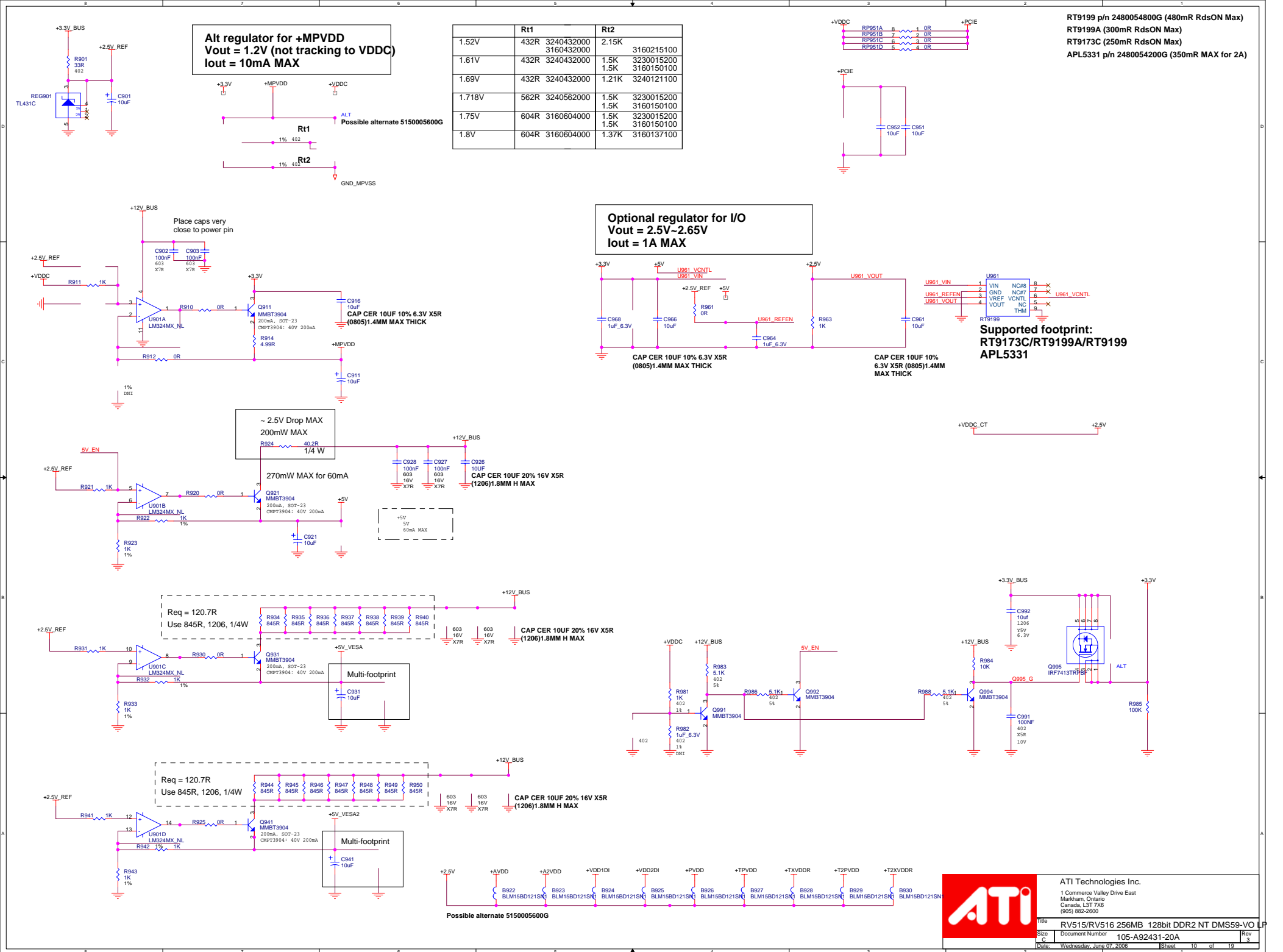
RICHTEK RT9214
INTERSIL ISL6545

MVDDC-PWM4

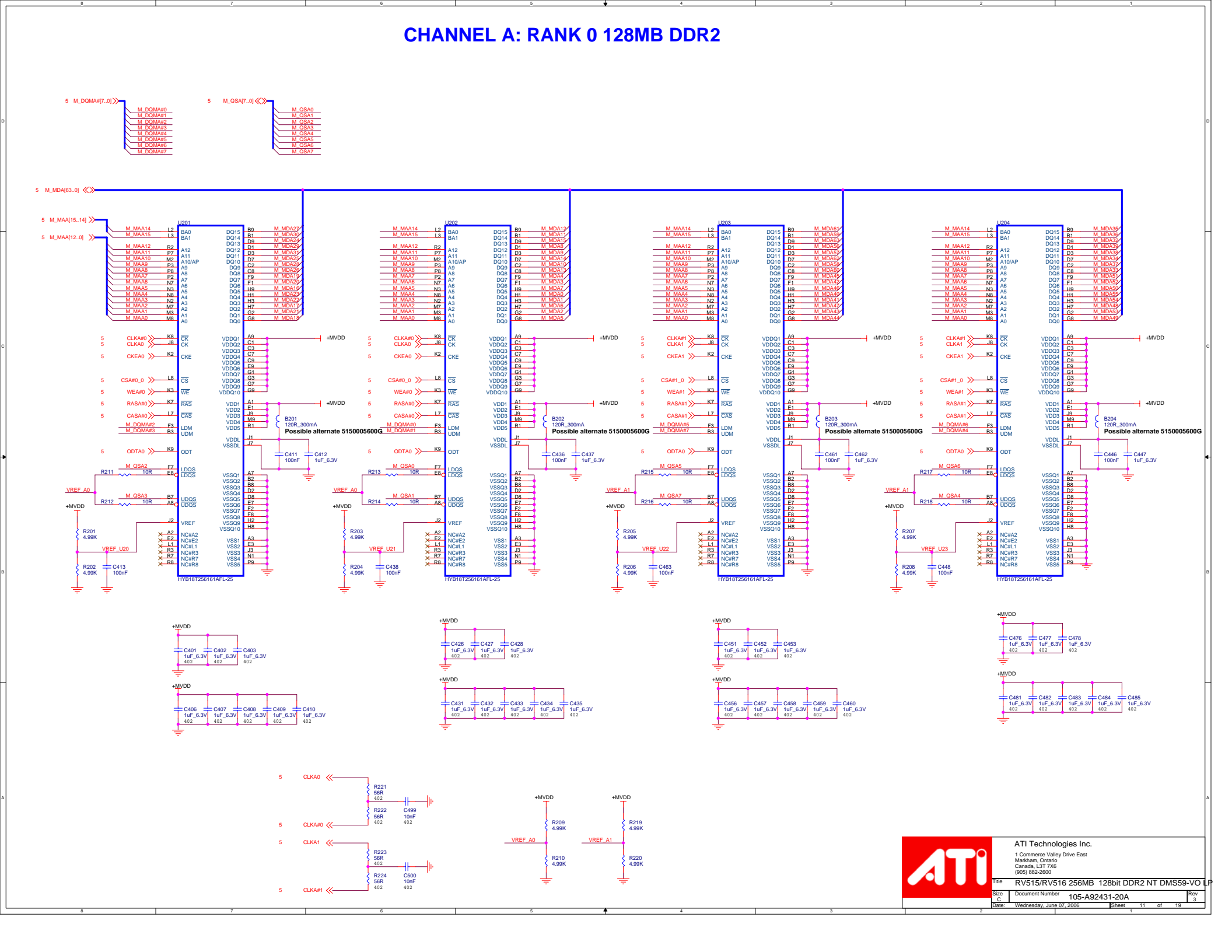
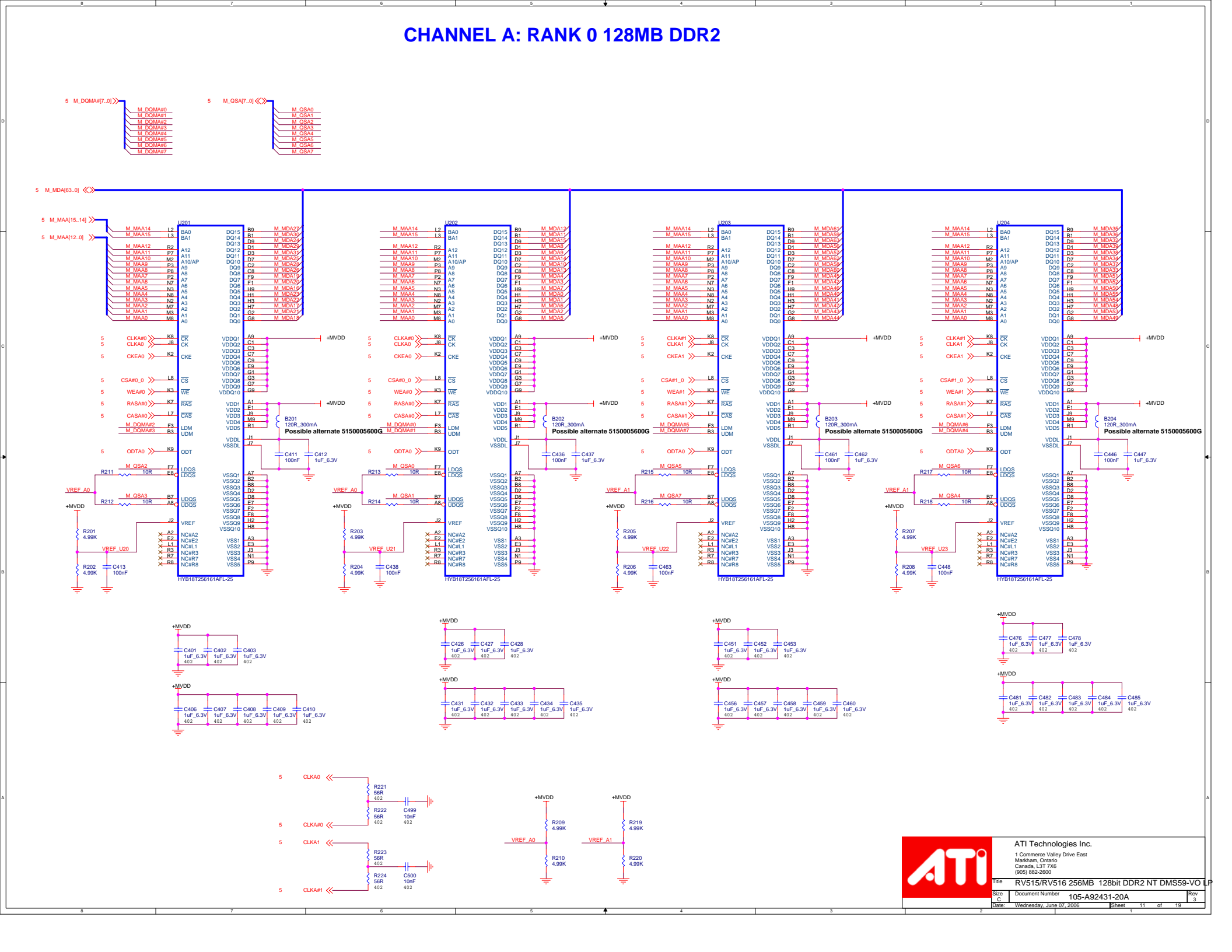


ANPEC APW7061A





CHANNEL A: RANK 0 128MB DDR2



CHANNEL A: RANK 0 128MB DDR2

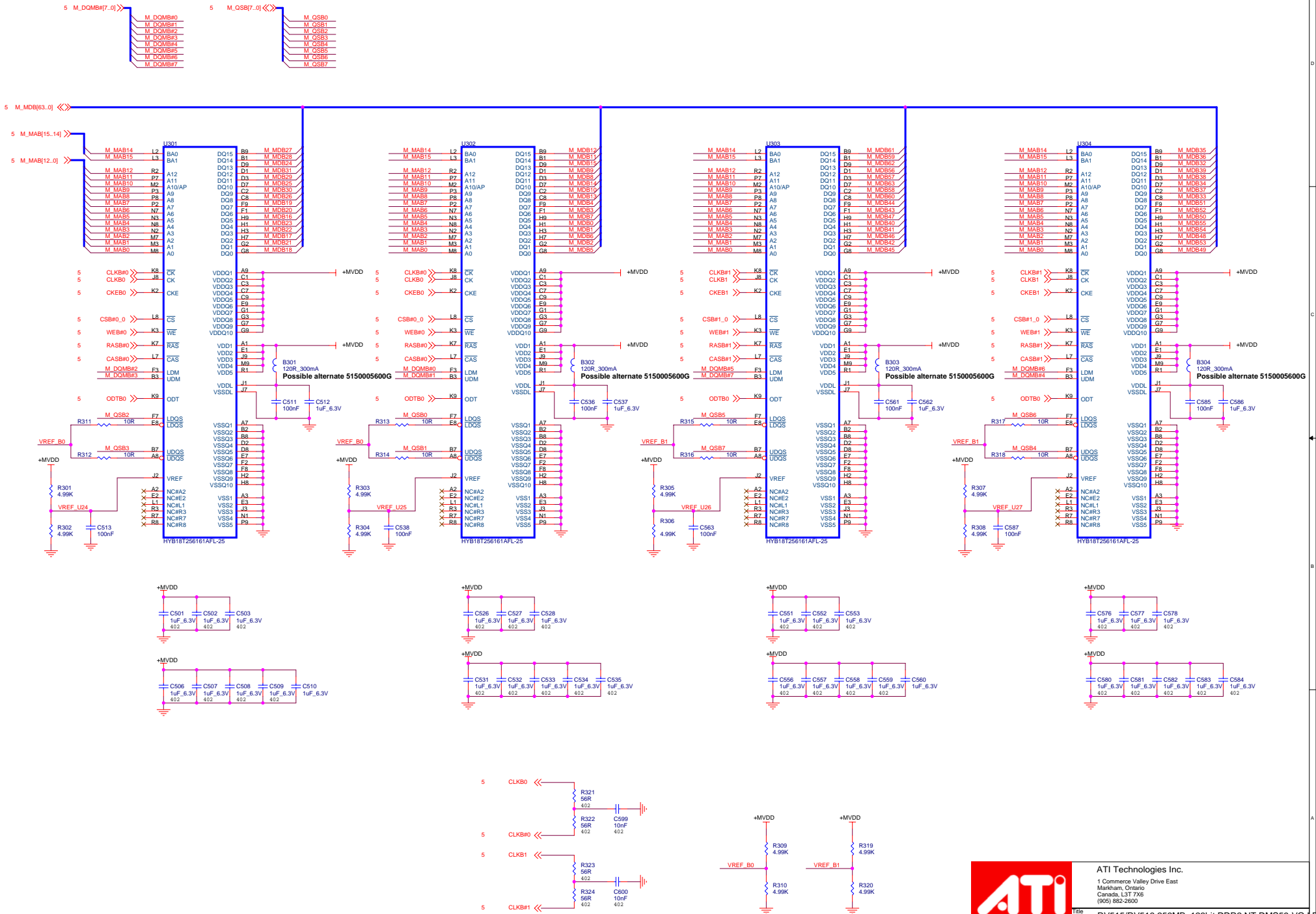
CHANNEL A: RANK 0 128MB DDR2

CHANNEL A: RANK 0 128MB DDR2

CHANNEL A: RANK 0 128MB DDR2

[illegible][illegible]

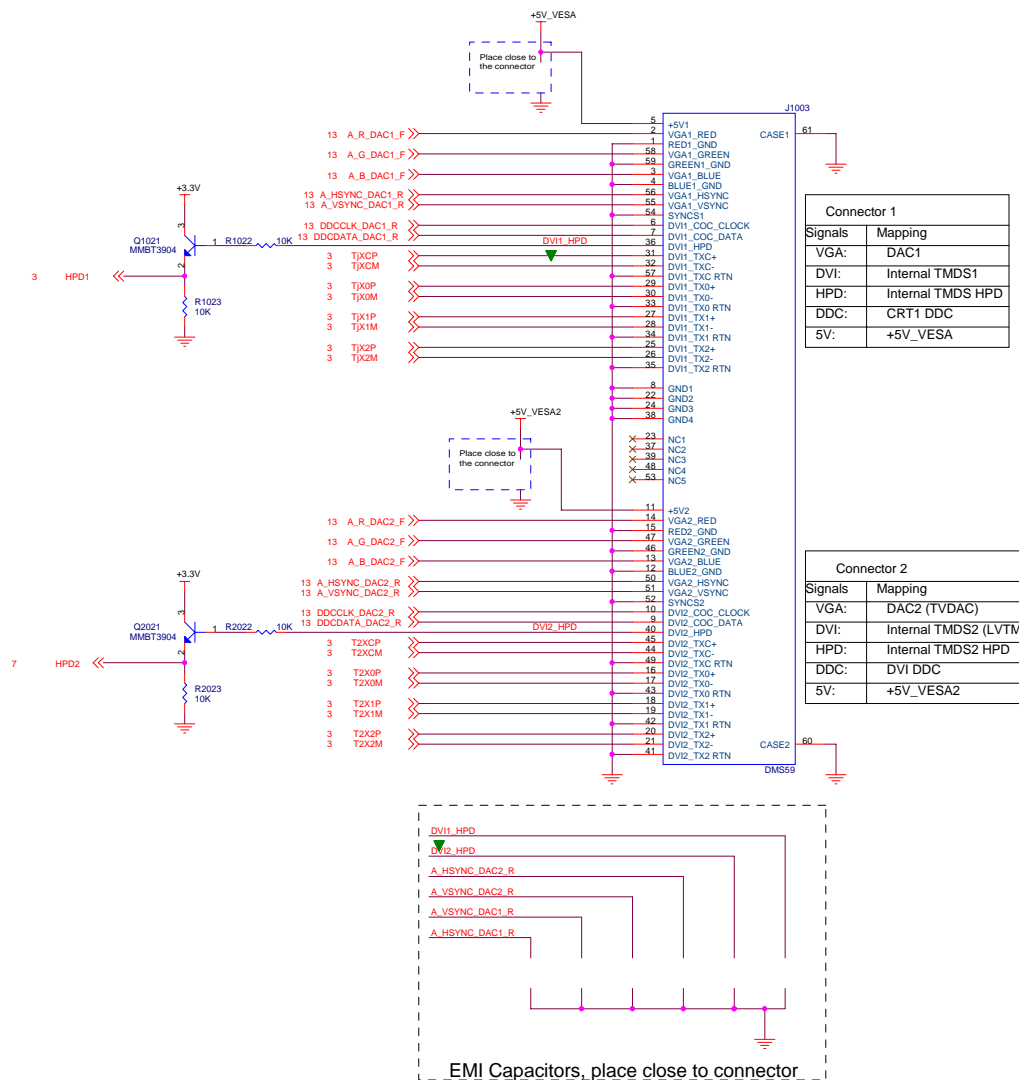
CHANNEL B: RANK 0 128MB DDR2



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

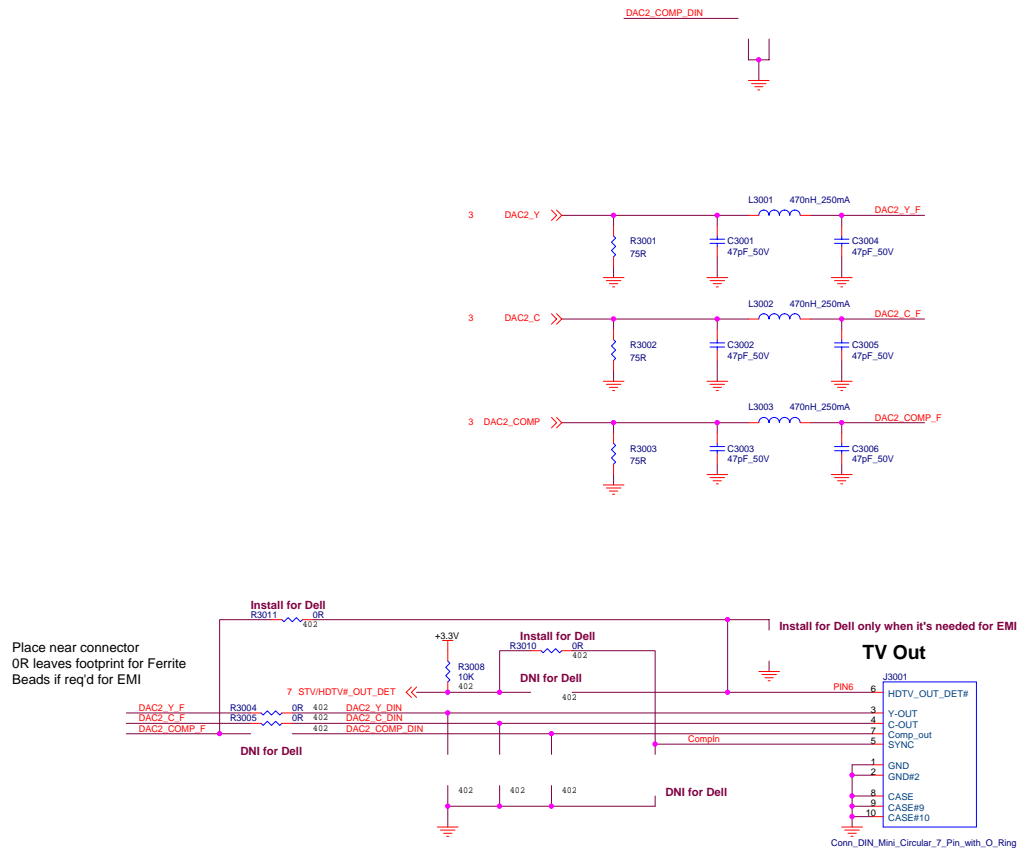
Title		RV515/RV516 256MB 128bit DDR2 NT DMS59-VO LP	
Size	Document Number	105-A92431-20A	Rev 3
Date	Wednesday, June 07, 2006		Sheet 12 of 19

VESA Multi-Display Interface DMS-59 Connector



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada L3T 7X5
(905) 882-2600

File: RV515/RV516 256MB 128bit DDR2 NT DMS59-VO LP
Size: Custom
Document Number: 105-A92431-20A
Date: Wednesday, June 07, 2006
Sheet: 14 of 19
Rev: 0



The 7-pin MiniDIN footprint allows one of the two MiniDINs:

- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

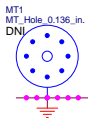


ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV515/RV516 256MB 128bit DDR2 NT DMS59-VO LP
Size	Document Number
Date	105-A92431-20A
Rev	3

DVI/VGA SCREWS

- ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16
ASSY
- ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40
ASSY
- ASSY-SCREW5
SCREW
JACKPOST, HEX, 3/16 AF, 4-40
ASSY
- ASSY-SCREW6
SCREW
JACKPOST, HEX, 3/16 AF, 4-40
ASSY



DNI



LP brackets

ATX brackets





TitleRV515/RV516 256MB 128bit DDR2 NT DMS59-VO LP

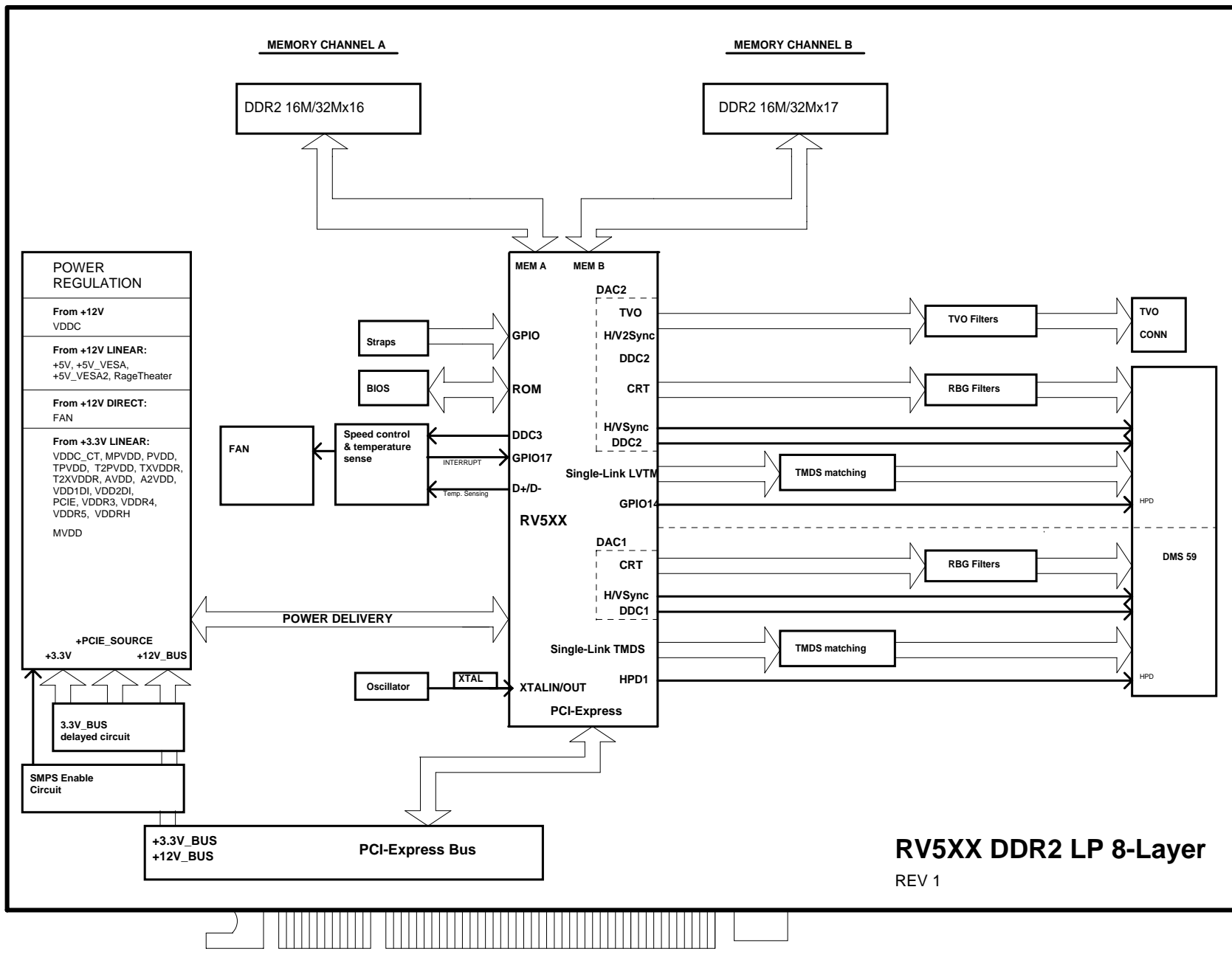
Schematic No.105-A92431-20A

Date:Wednesday, June 07, 2006

REVISION HISTORY

Rev3

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	02/21/06	Initial release , ASIC, Memory & PS from A771 revD
1	00	04/21/06	-00 PCB release, No PCB effecting schematic Changes (only ASSY-SCREW6 added for BOM usage), Layout improvements on TMDS reference ground on L3 & Fan trace on bottom layer
2	10	04/27/06	-10 PCB release, No PCB effecting schematic Changes, Few Layout improvements for EMI (increase spacing of power plans from TMDS pairs)
3	20A	05/16/06	-20A PCB release, Adding ML601 as dual footprint for NL601 in VDDC SMPS , Moving TV DAC Filter far from VDDC regulator , All TVO Filter caps (C3001-6) changed to 402



RV5XX DDR2 LP 8-Layer
REV 1



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV515/RV516 256MB 128bit DDR2 NT DMS59-VO LP	Rev	3
Size	C	Document Number	105-A92431-20A
Date	Wednesday, June 07, 2006	Sheet	19 of 19