PG180-A02

256b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

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base on V372-02S change for D18 Z
1. P.23 remove SLI & BRIDGE_LED_VDD & SLI_BRG_PRST*
2. P.52 remove LED change FAN connector
3. P.53 remove LED
4. P.38&44 add FUSE
5. P.5~14 mem add < >
6. P.53 LED use V336-0D
7. P.32 remove
8. P.35~38 dual MOS
9. P.33 change dual MOS
10. P.43 remove
11. P.31 change to UP1666
12. P.21 remove colay DP

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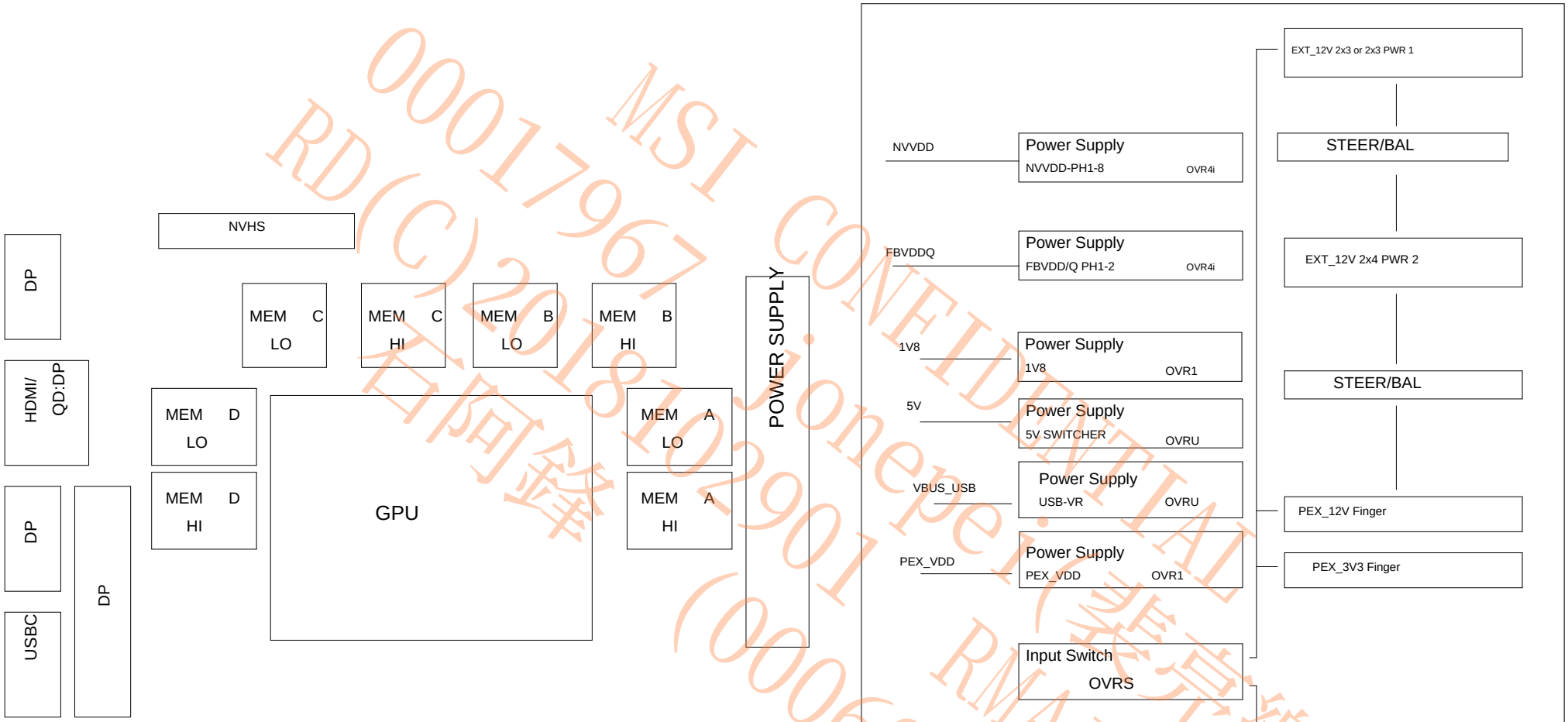
Page2: Block Diagram



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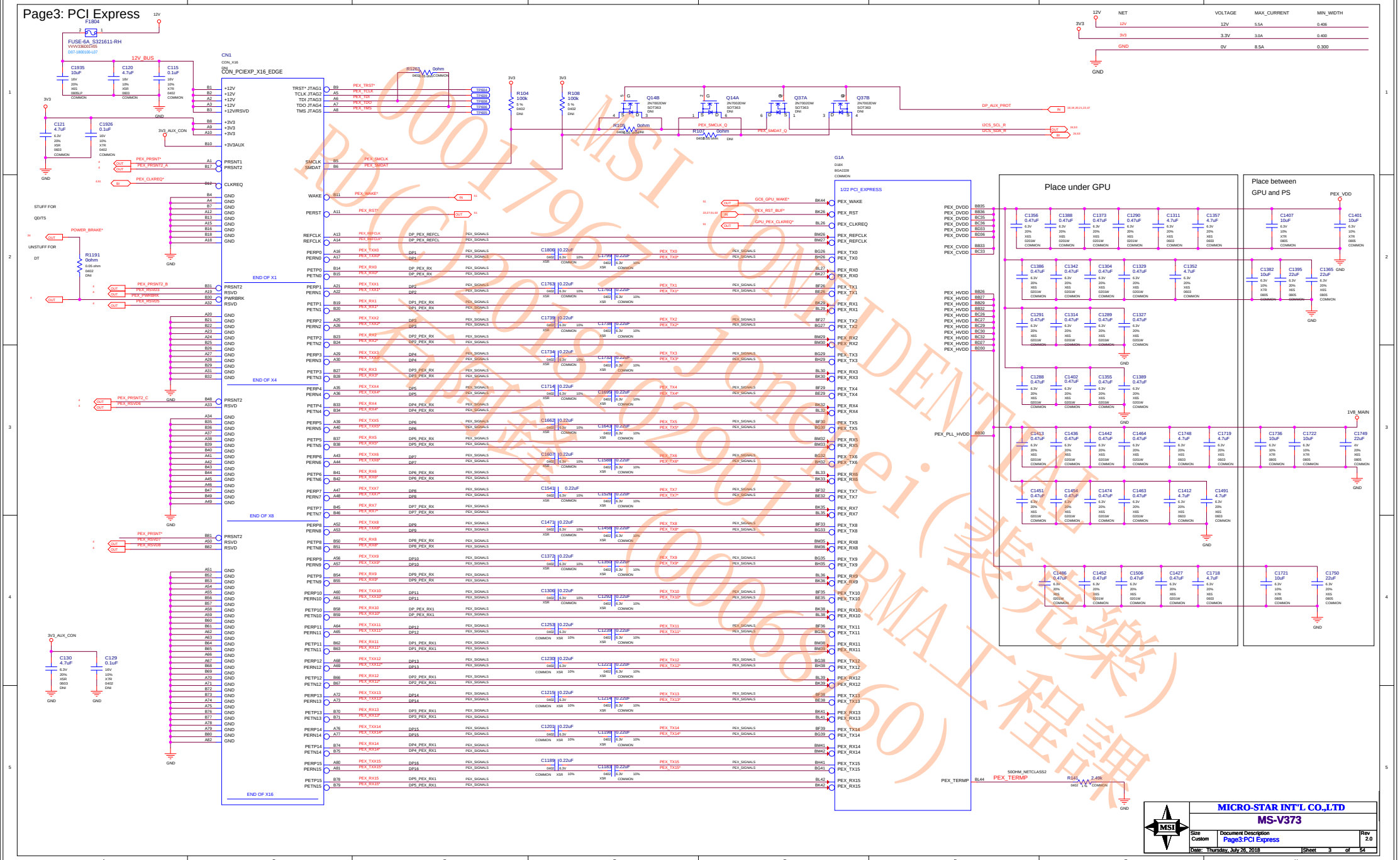
Page3: PCI Express



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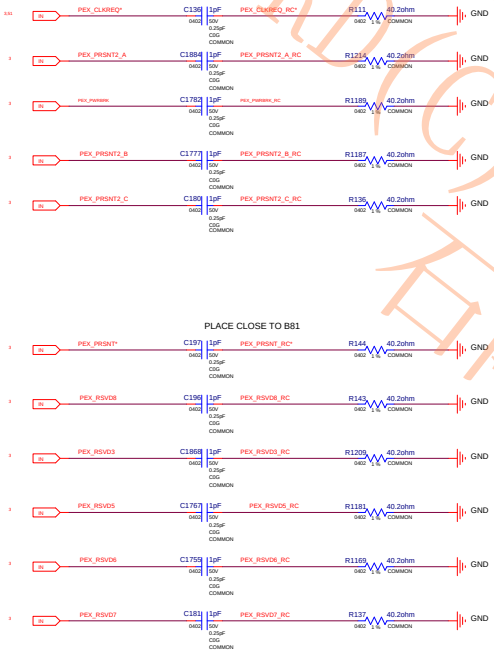
Page4: PCI Termination



PLACE CLOSE TO B81

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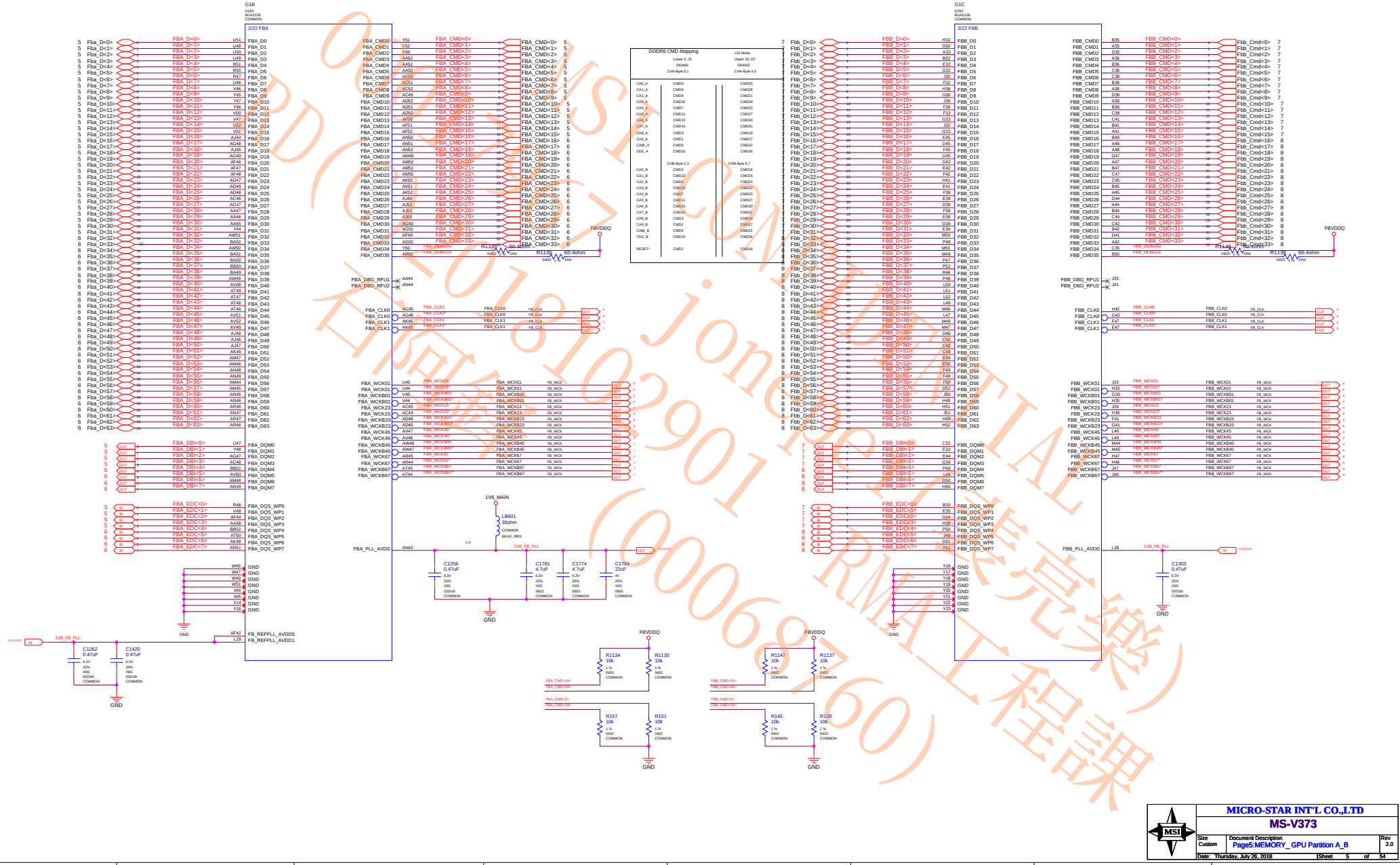
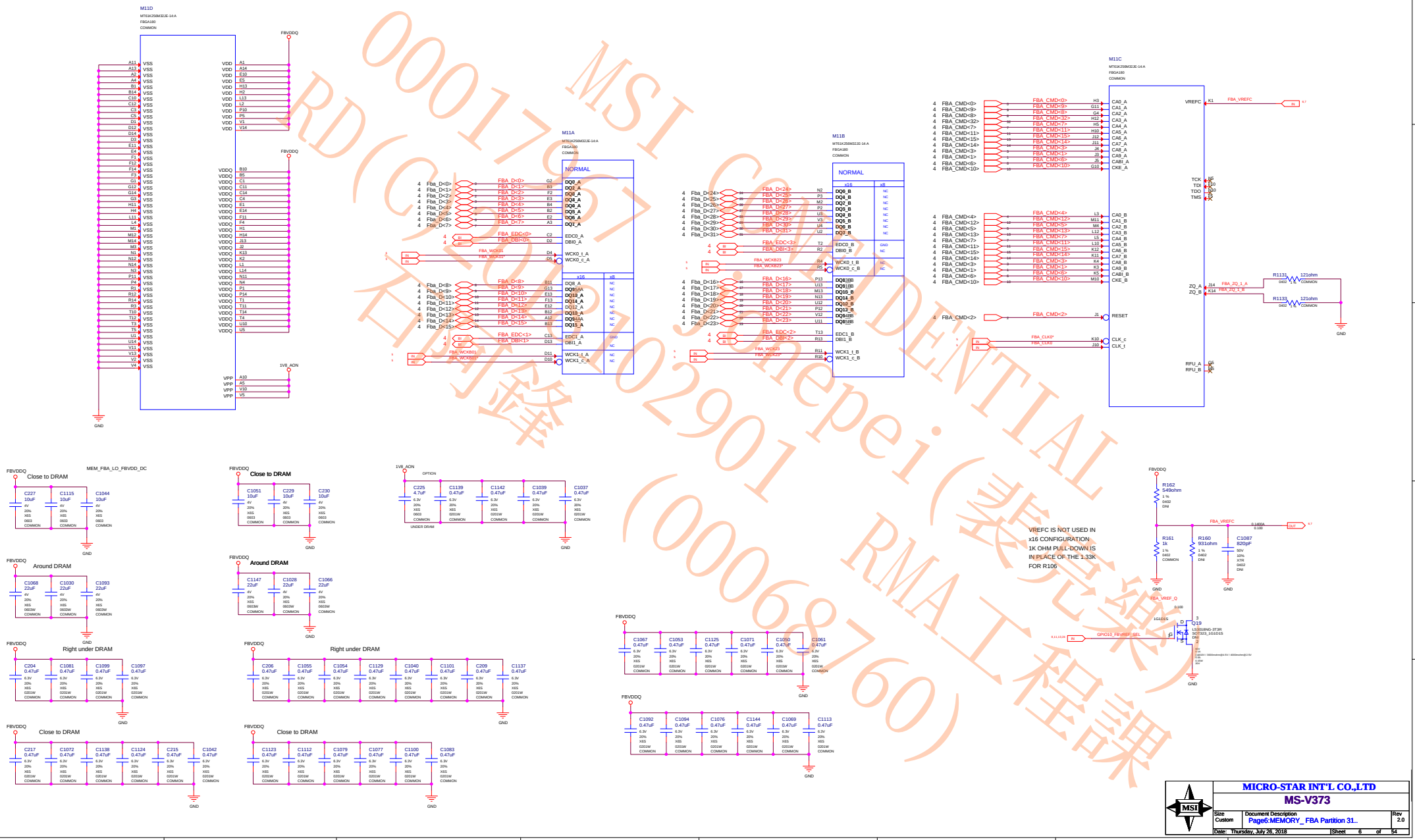
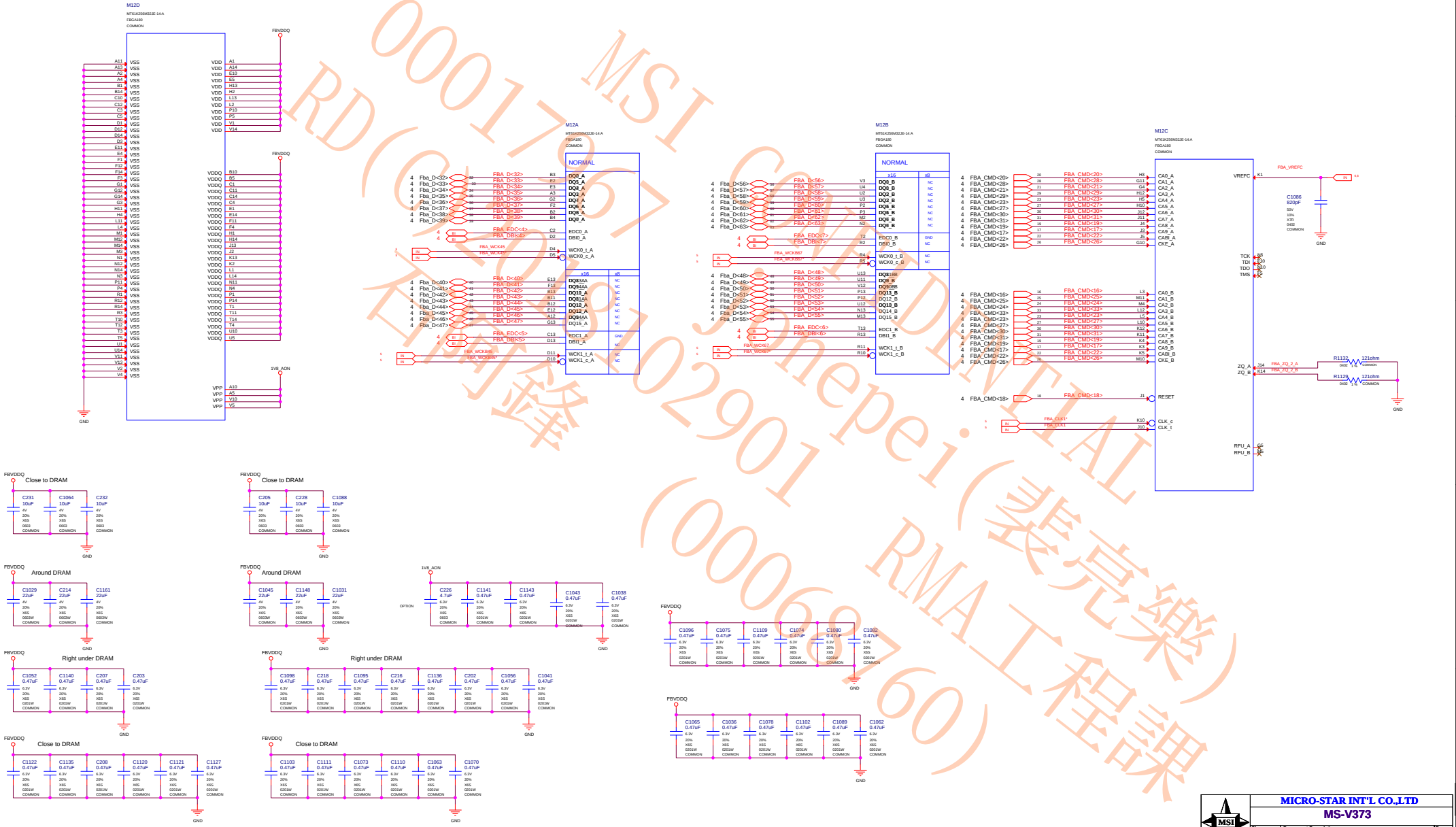
Page5: MEMORY: GPU Partition A/B



Page6: MEMORY: FBA Partition 31..0



Page7: MEMORY: FBA Partition 63..32



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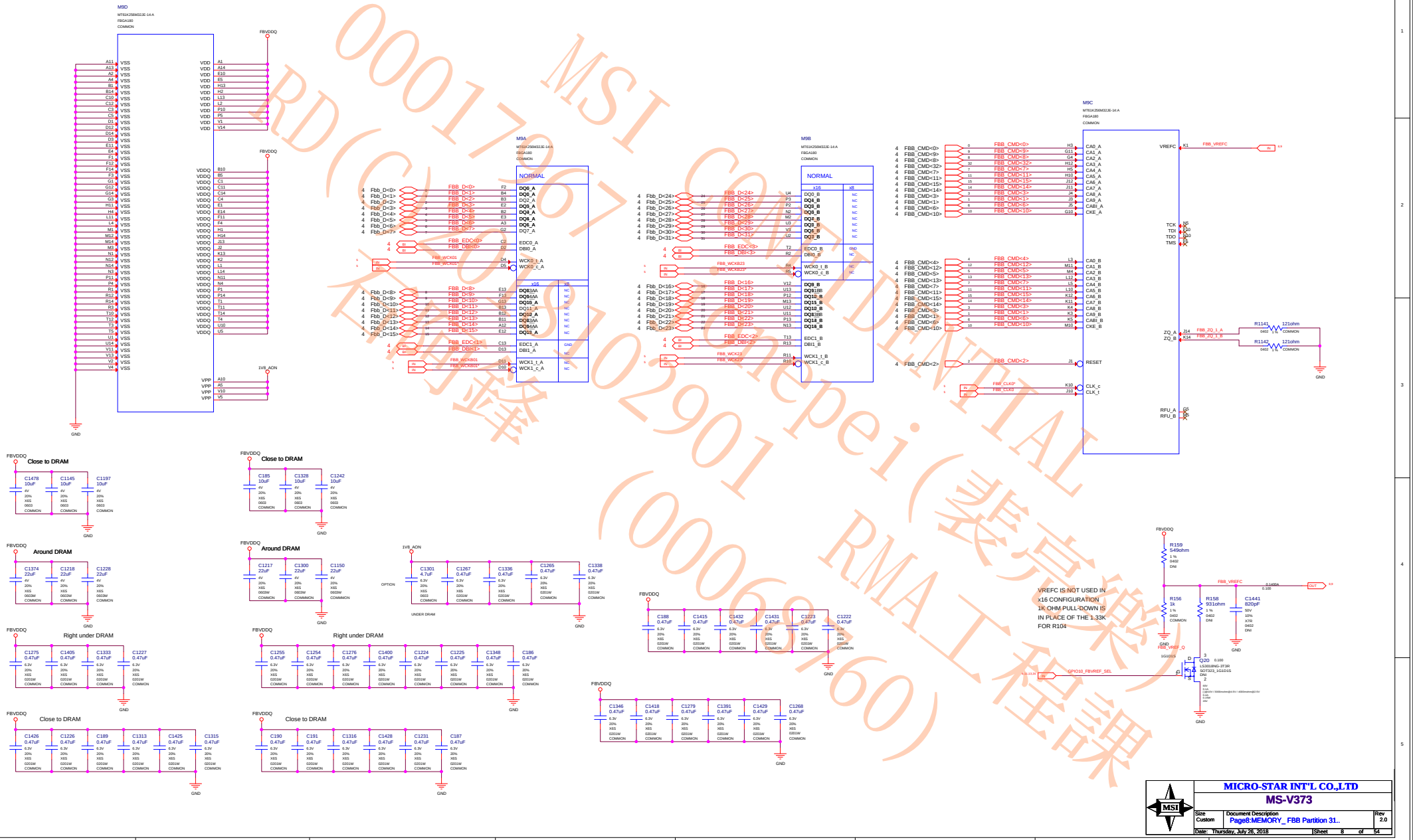
Page8: MEMORY: FBB Partition 31..0



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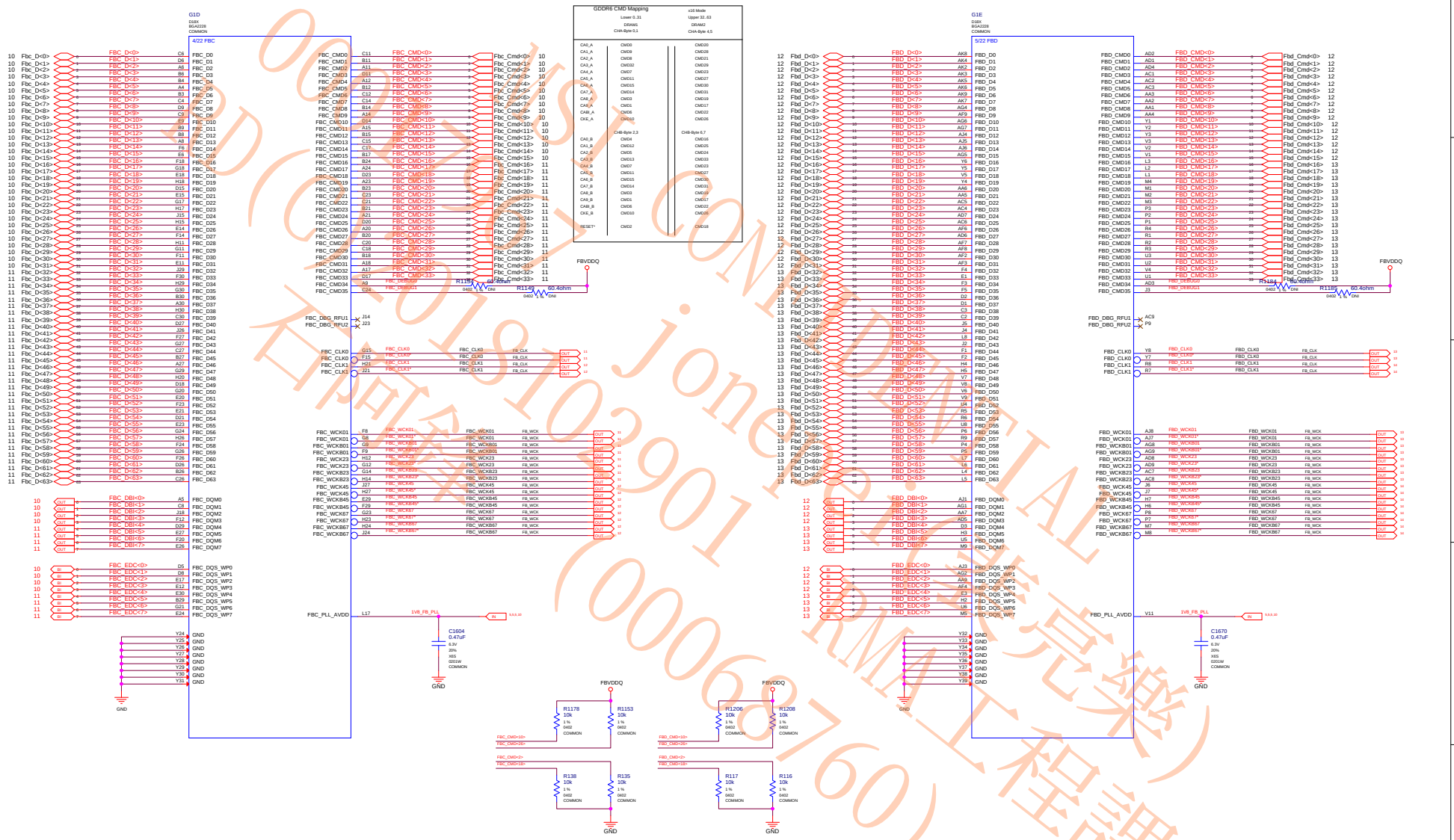
Page10: MEMORY: GPU Partition C/D



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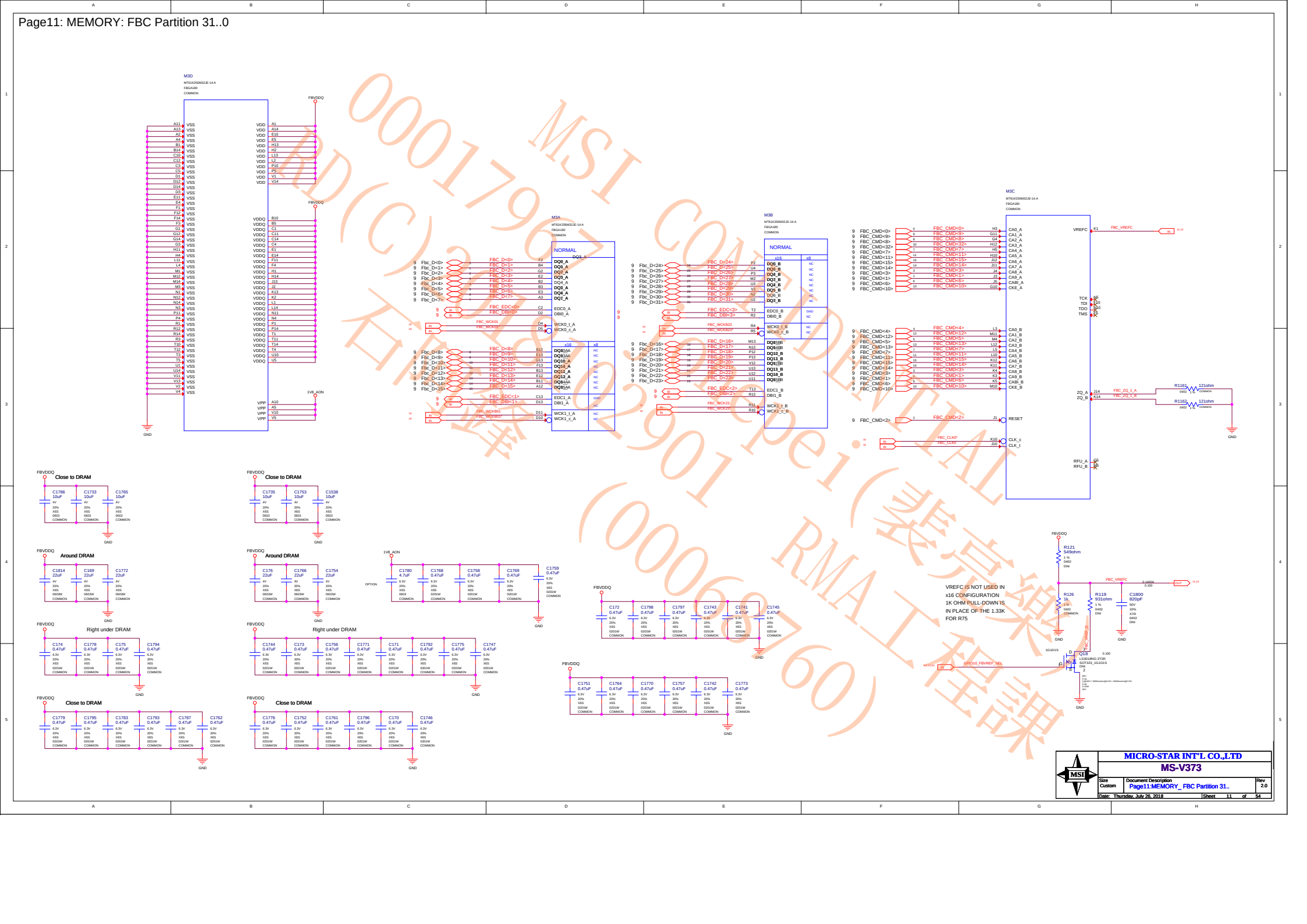
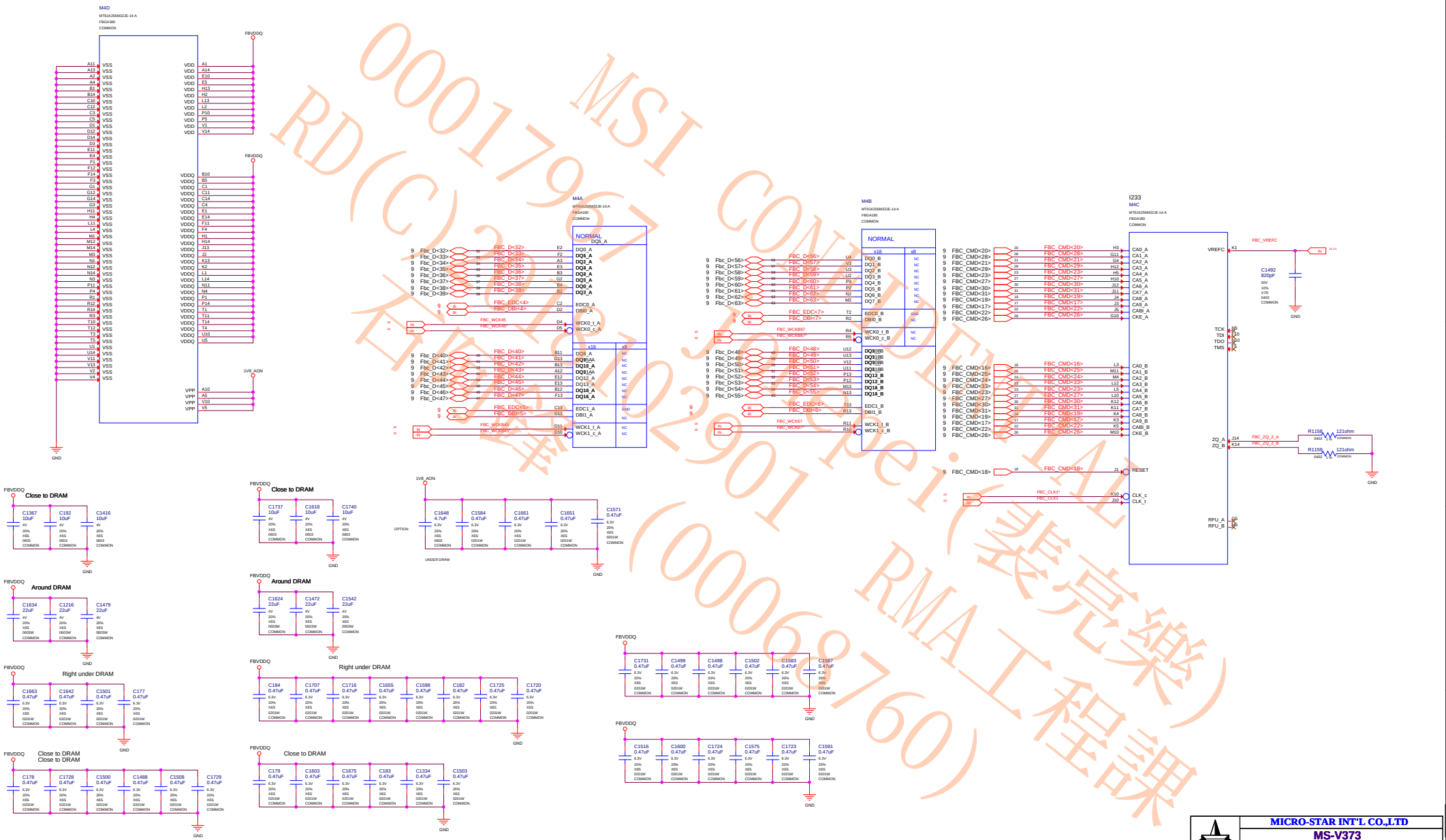
Page11: MEMORY: FBC Partition 31..0





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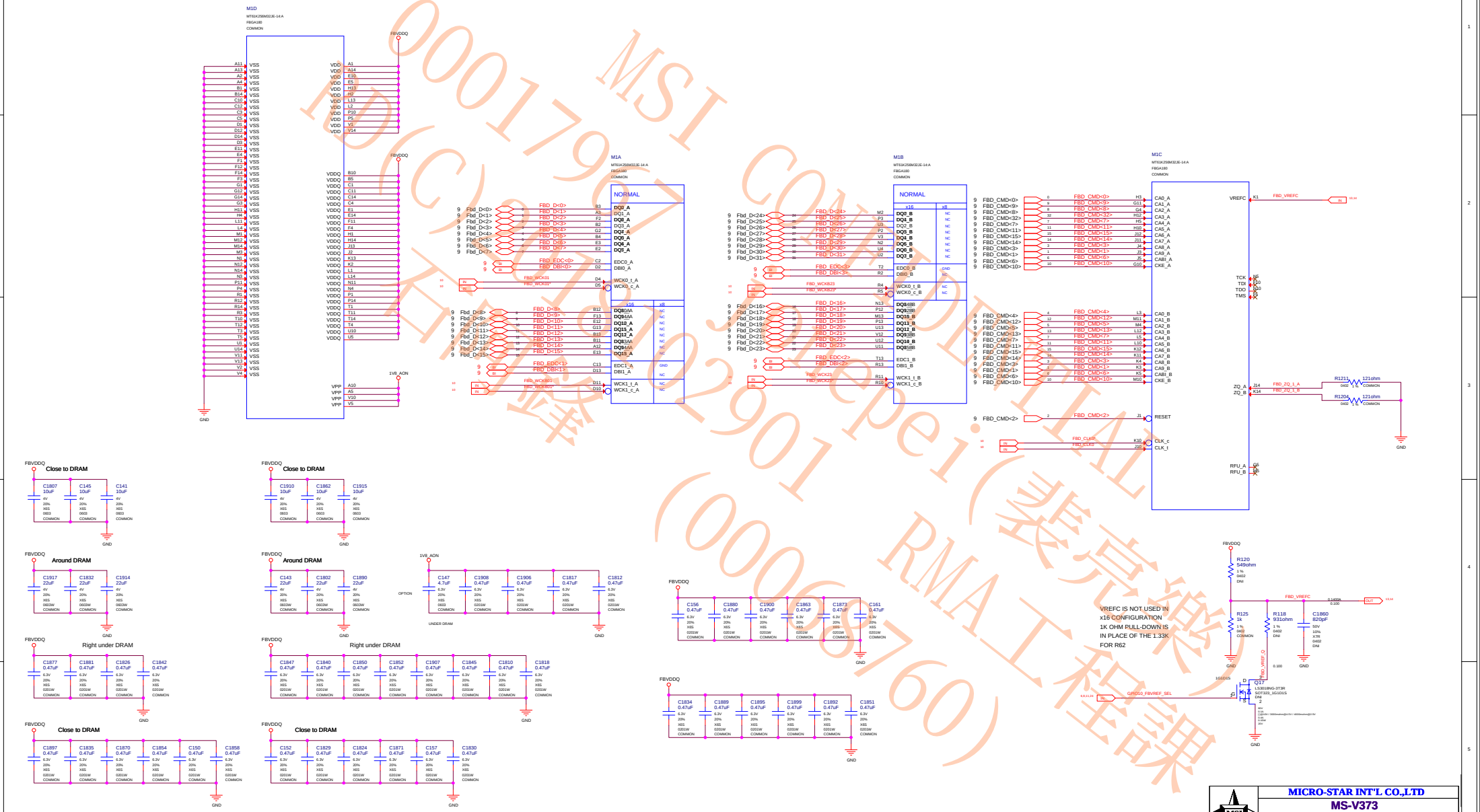

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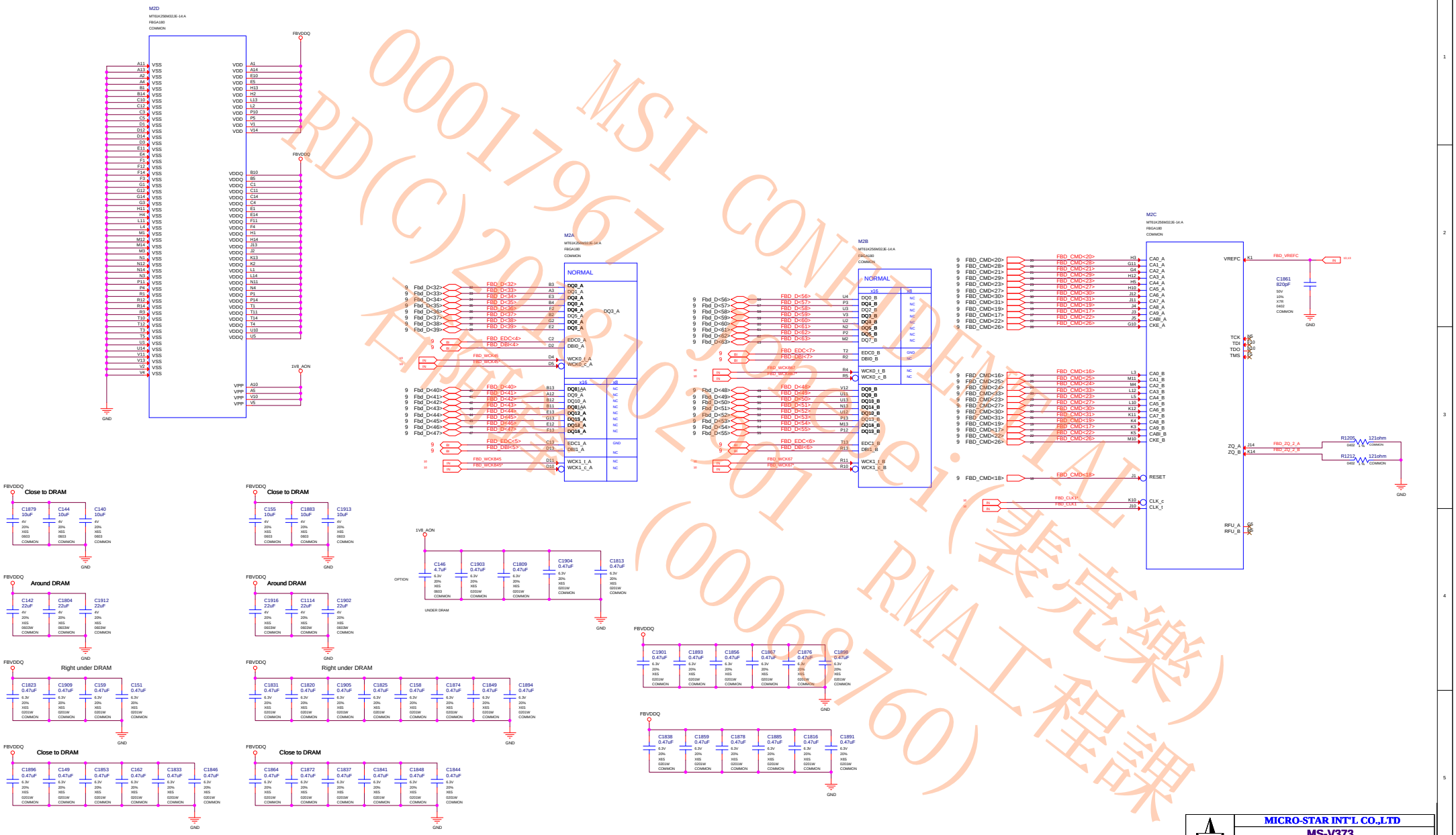
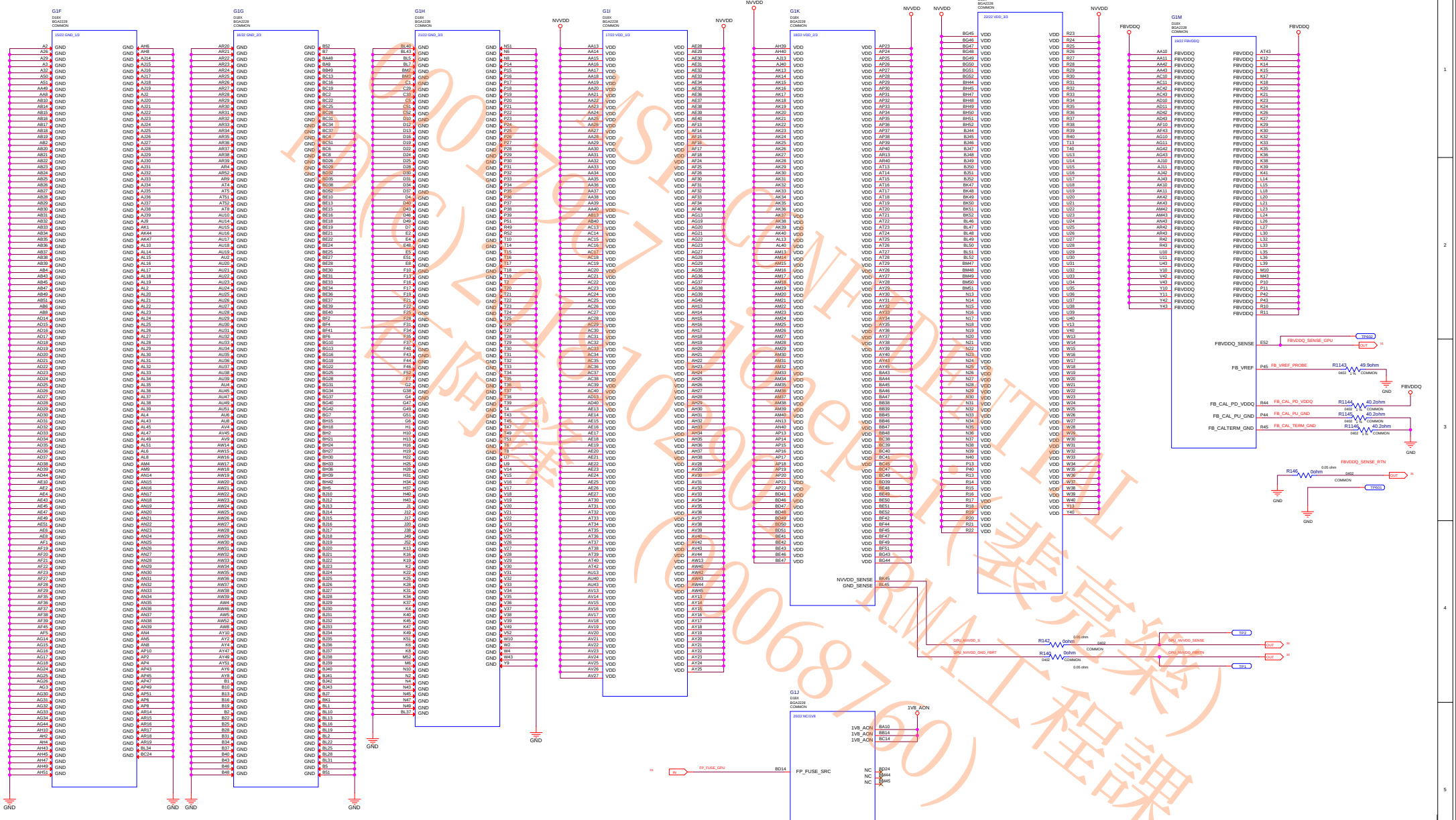


Page15: GPU PWR and GND



Page16: GPU Decoupling

FBVDDQ

FBVDDQ

Partition A — 6x 1uF and 2x 10uF

C1241 C1243 C1235 C1261 C1250 C1266 C1251 C1248
C1232 C1259 C1260 C1237 C1258 C1245
GND

Partition B — 6x 1uF and 2x 10uF

C1343 C1481 C1398 C1269 C1344 C1522 C1244 C1321
C1294 C1238 C1469 C1406 C1277 C1435
GND

Partition C — 6x 1uF and 2x 10uF

C1653 C1523 C1586 C1713 C1582 C1615 C1381 C1453
C1627 C1610 C1467 C1572 C1557 C1711
GND

Partition D — 6x 1uF and 2x 10uF

C1697 C1673 C1674 C1700 C1672 C1668 C1708 C1683
C1696 C1699 C1698 C1669 C1703 C1666
GND

Place Close to GPU

C1637 C1682 C1687 C1679
GND

Place Close to GPU

C1543 C1249 C1504 C1684 C1791 C1247 C1789 C1153 C1278
GND

NVVDD

NVVDD

C1233 C1617 C1236
GND

nv_cap nv_cap nv_cap

C1496 C1556 C1220 C1229 C1439 C1246
GND

C1264 C1263 C1530 C1520 C1234 C1423 C1493 C1597
GND

C1332 C1640 C1490 C1529 C1559 C1353 C1443 C1375 C1322 C1525 C1480 C1494 C1509 C1514 C1528
GND

C1307 C1470 C1422 C1495 C1633 C1345 C1271 C1445 C1390 C1505 C1404 C1419 C1433 C1444 C1457
GND

C1515 C1579 C1576 C1366 C1394 C1331 C1639 C1380 C1566 C1482 C1354 C1411 C1424 C1309 C1270
GND

C1622 C1461 C1403 C1362 C1337 C1305 C1533 C1619 C1507 C1392 C1550 C1578 C1430 C1635 C1626
GND

C1459 C1434 C1475 C1330 C1349 C1449 C1510 C1296 C1396 C1368 C1417 C1544 C1280 C1638 C1283
GND

C1281 C1540 C1448 C1312 C1320 C1460 C1466 C1465 C1393 C1581 C1335 C1351 C1570 C1585 C1602
GND

C1438 C1555 C1364 C1421 C1308 C1383 C1456 C1489 C1339 C1601 C1319 C1521 C1512 C1623 C1613
GND

C1562 C1569 C1554 C1551 C1295 C1363 C1324 C1455 C1468 C1476 C1611 C1596 C1408 C1592 C1567 C1273 C1539
GND

032-0532-000
X6S
0805

1V8_AON

1V8_AON

C1726 C1843 C1827 C1632 C1641 C1801 C1821 C1678 C1658
Near the GPU
GND

1V8_AON

C1815 C1819 C1805 C1828 C1652 C1688 C1644
Under the GPU
GND

NVVDD

NVVDD

C1369 C1625 C1252 C1387 C1297
GND

C1608 C1477 C1340 C1414 C1536 C1282 C1298 C1487
GND

C1347 C1384 C1647 C1293 C1318 C1437 C1628
GND

C1272 C1511 C1497 C1462 C1317 C1485
GND

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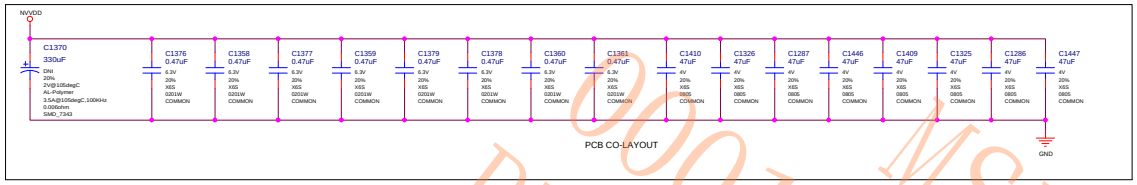
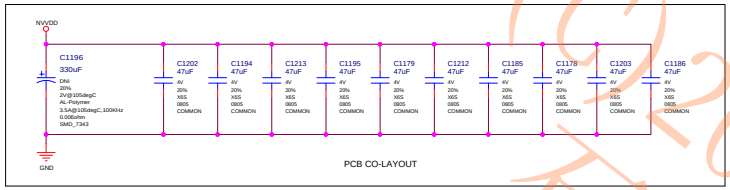
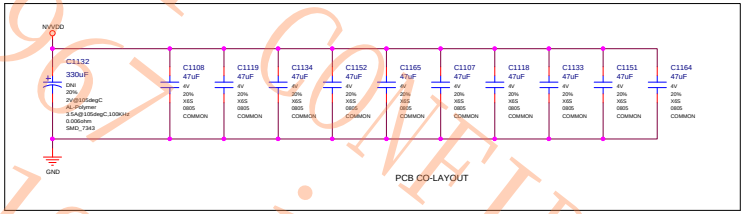
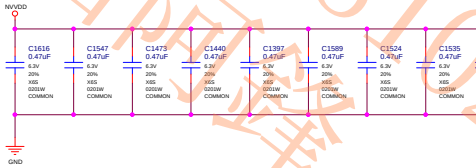
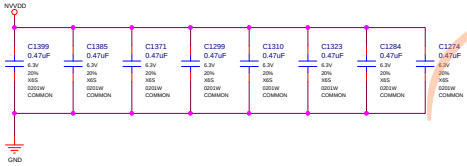
Page17: GPU Decoupling

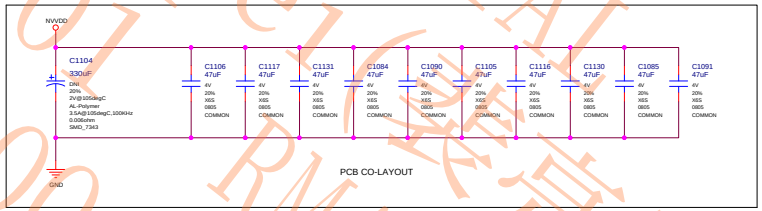


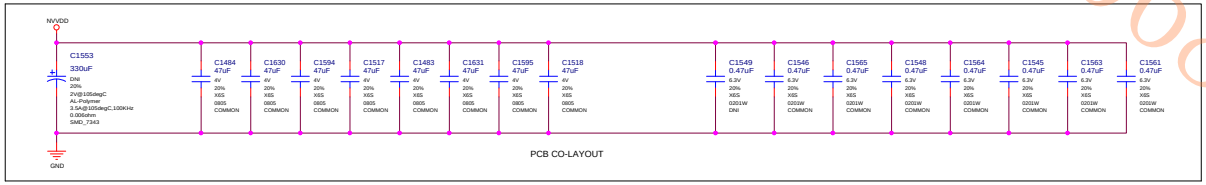












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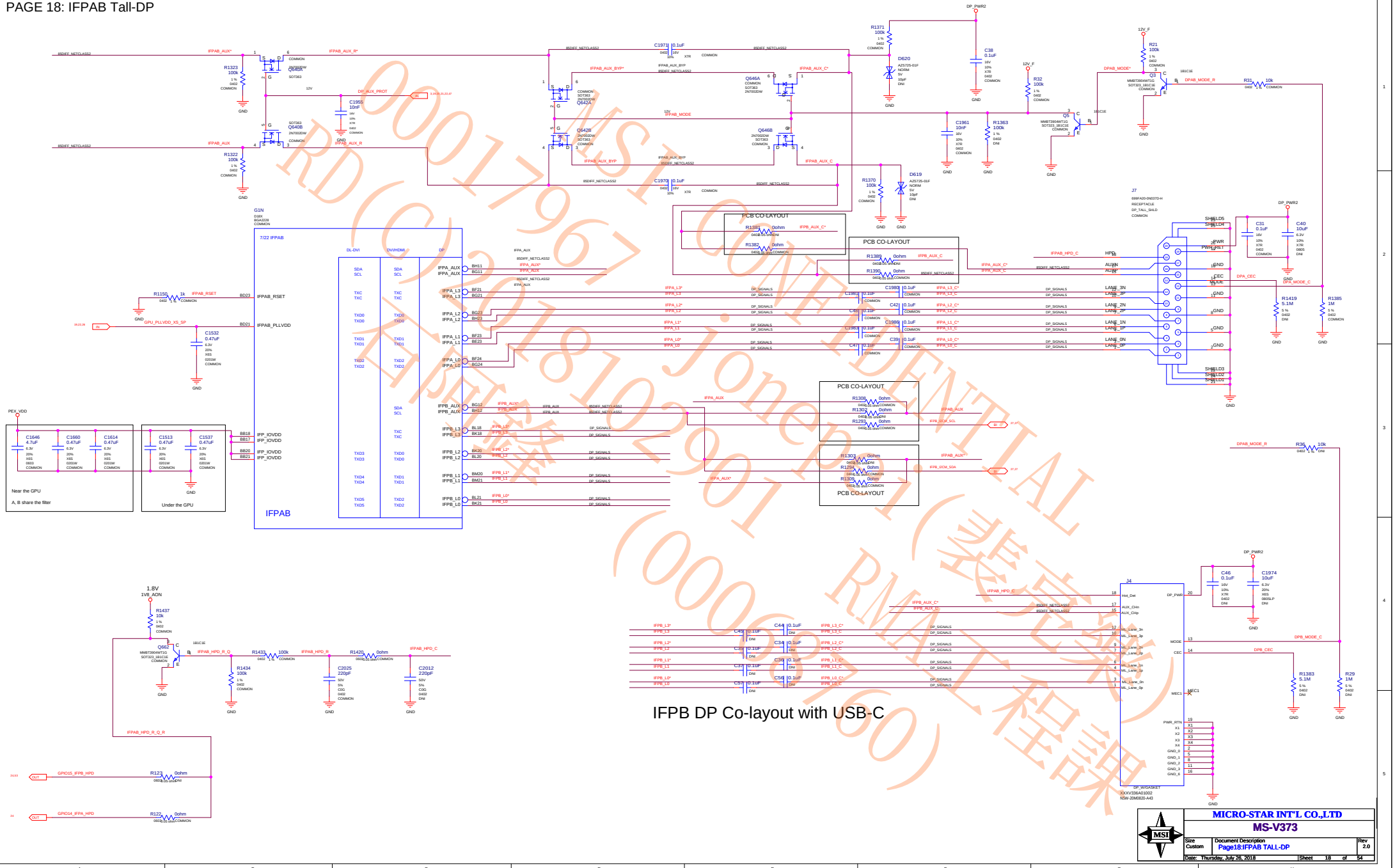
PAGE 18: IFPAB Tall-DP



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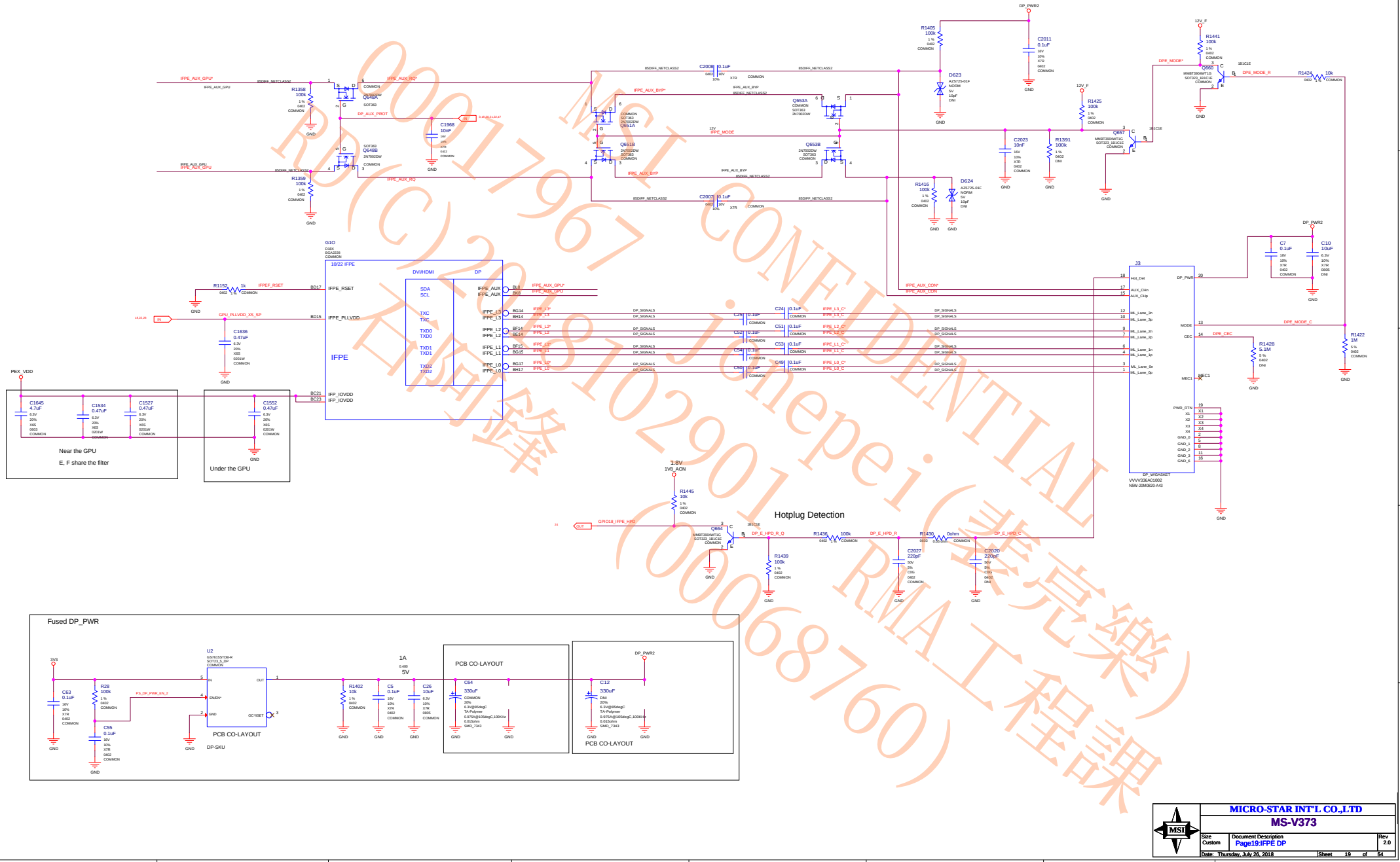
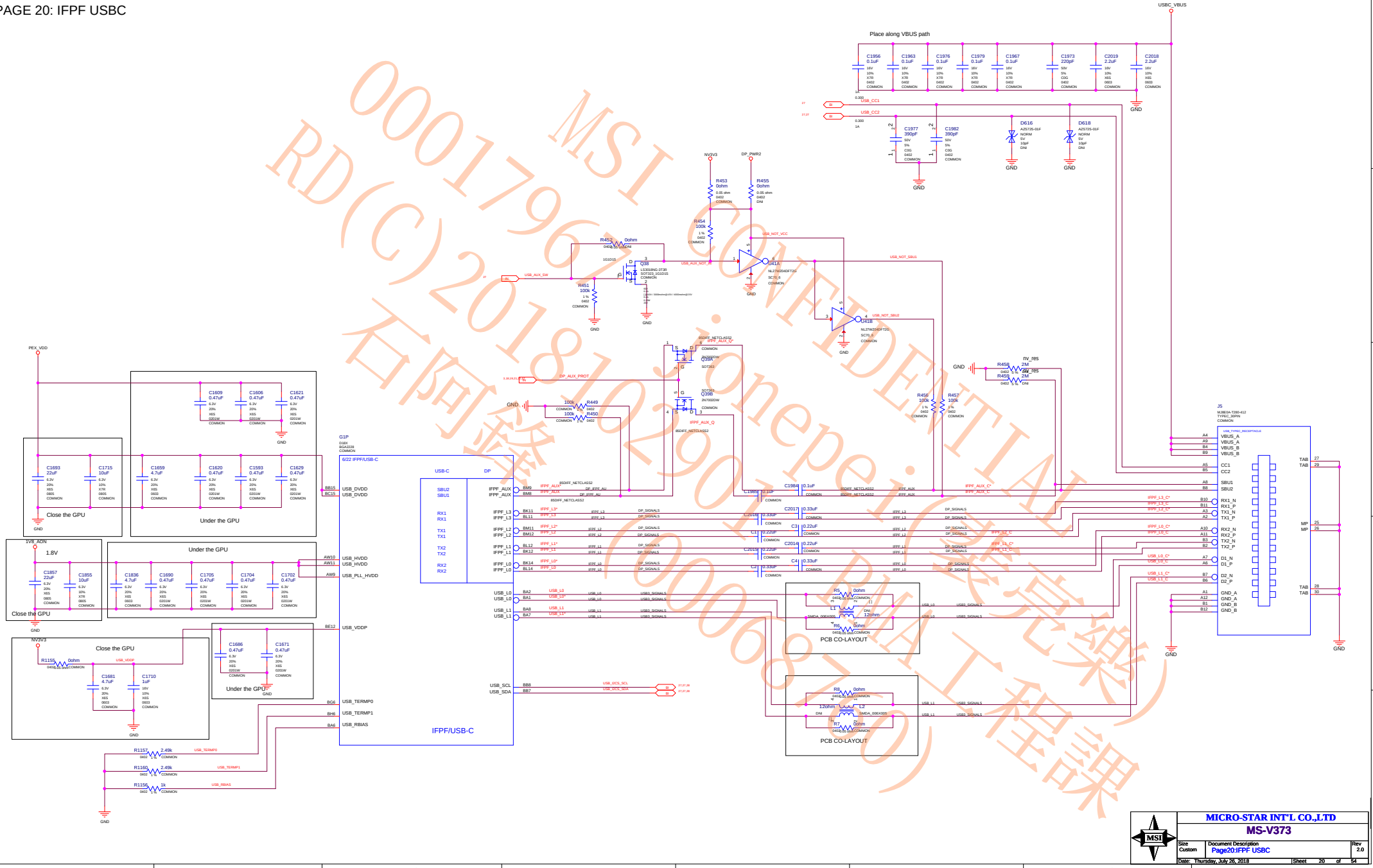
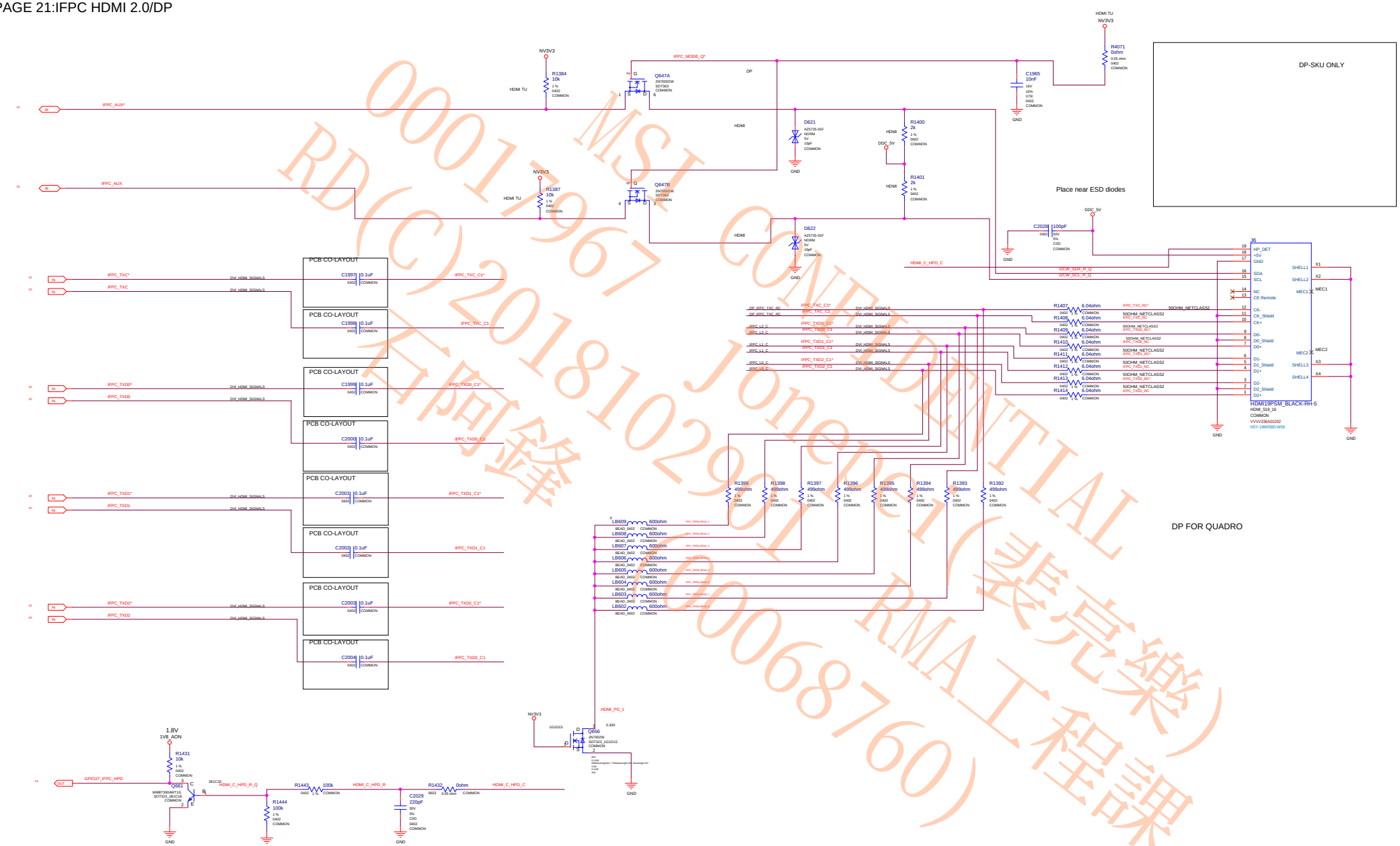
PAGE 19: IFPE DP





PAGE 21:IFPC HDMI 2.0/DP



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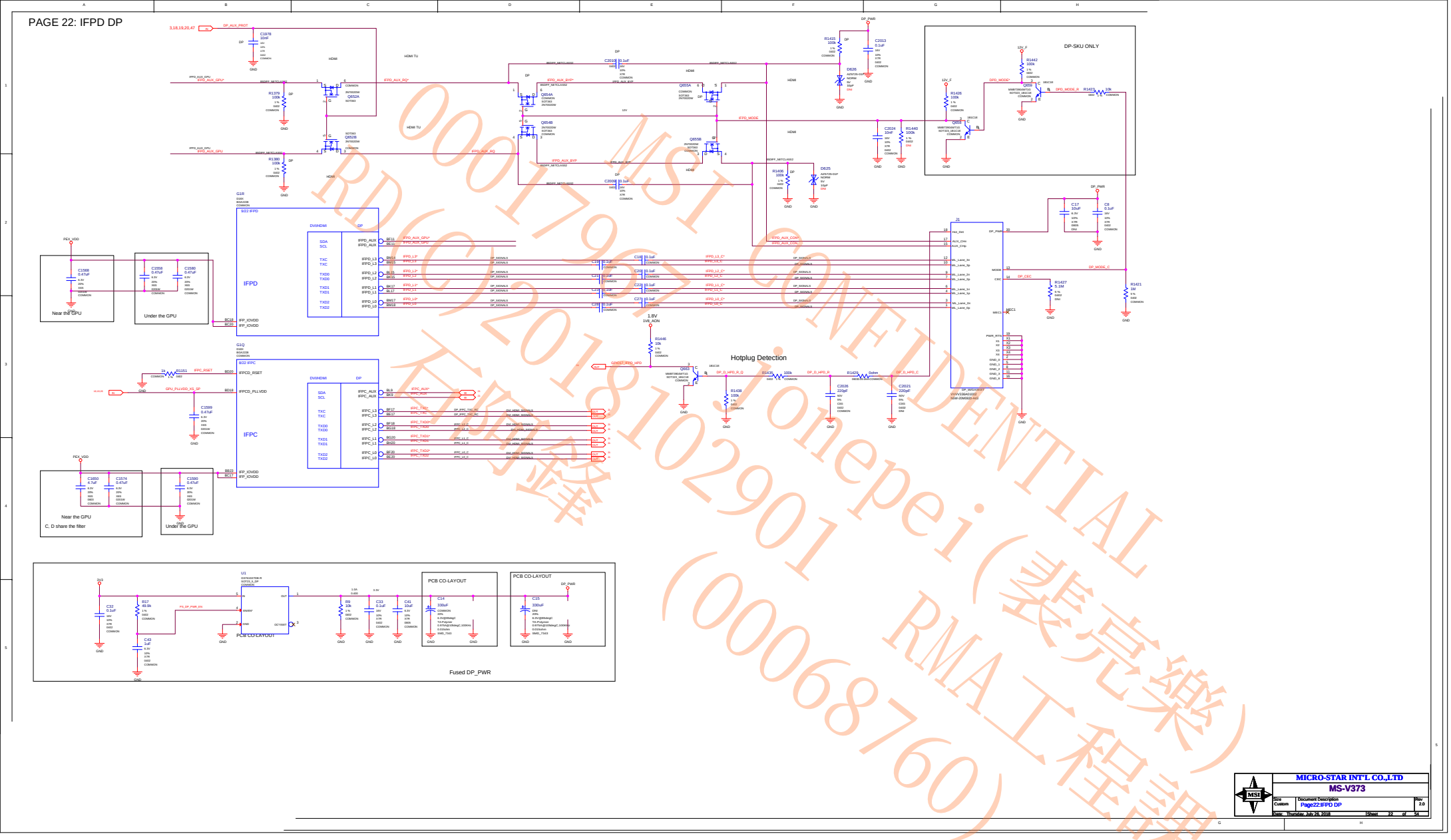
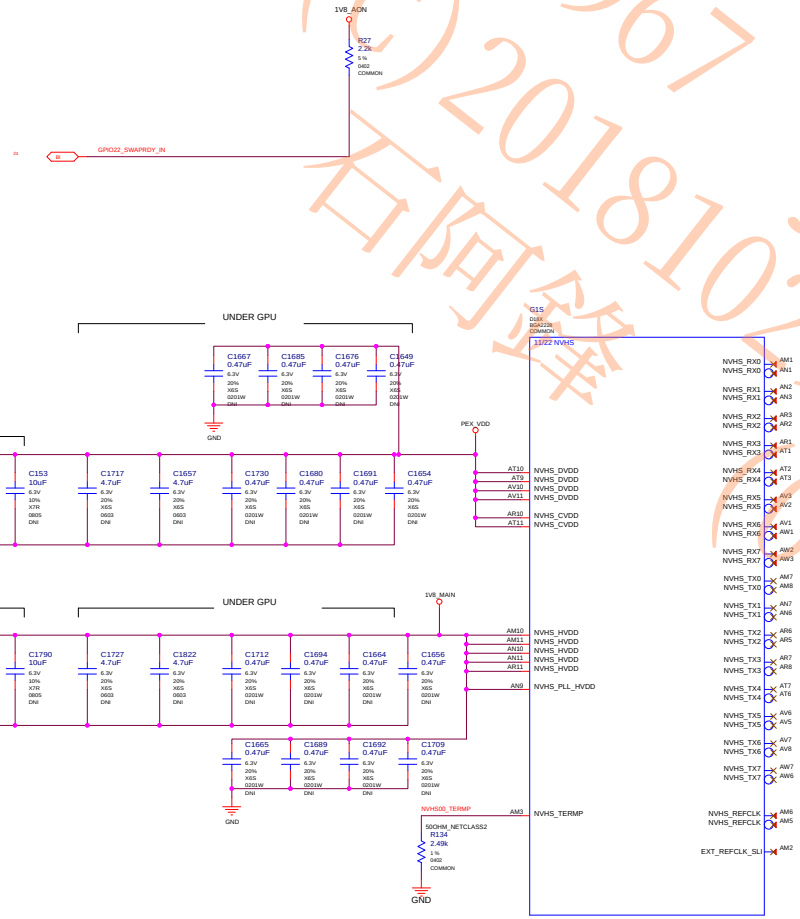


PAGE 23: NVHS Interface



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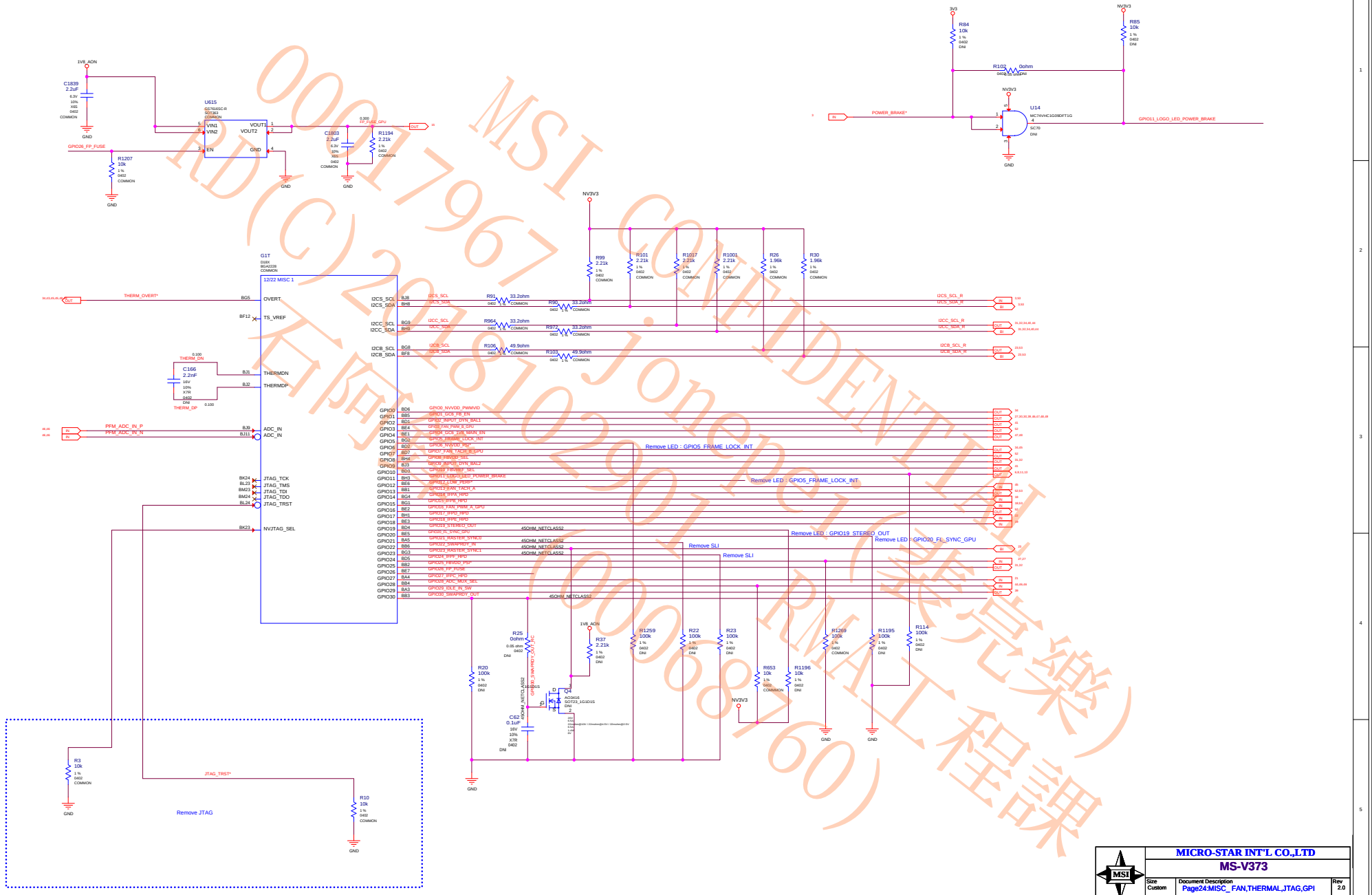
PAGE 24: MISC: Fan, Thermal, JTAG, GPIO, STEREO



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PAGE 25: MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

DEFAULT

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

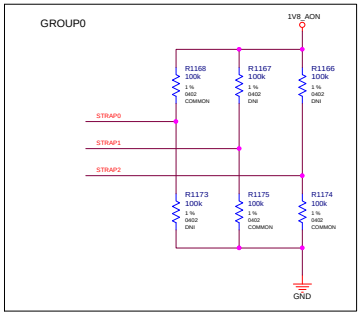
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

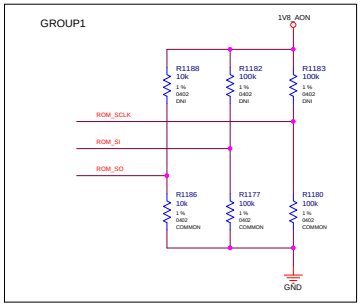
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

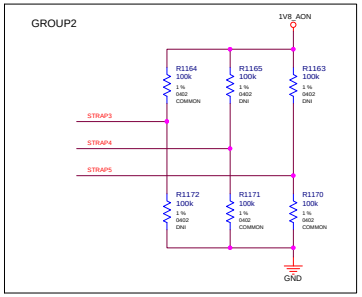
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

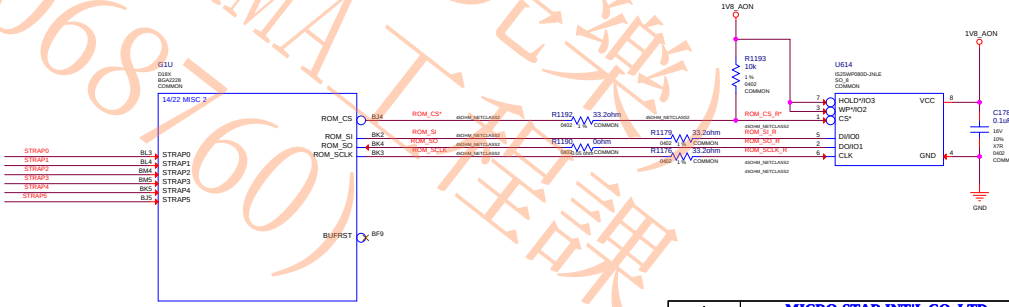
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default









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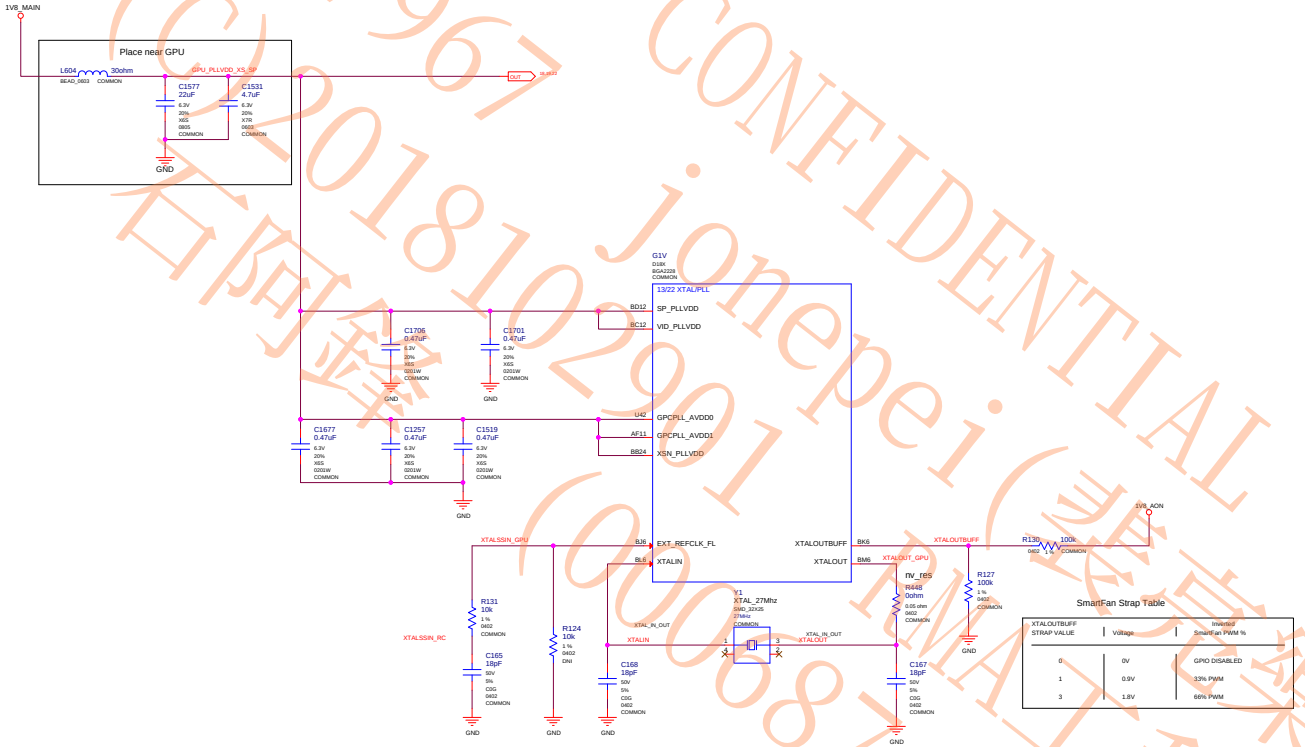
PAGE 26: MISC: XTAL. PLL



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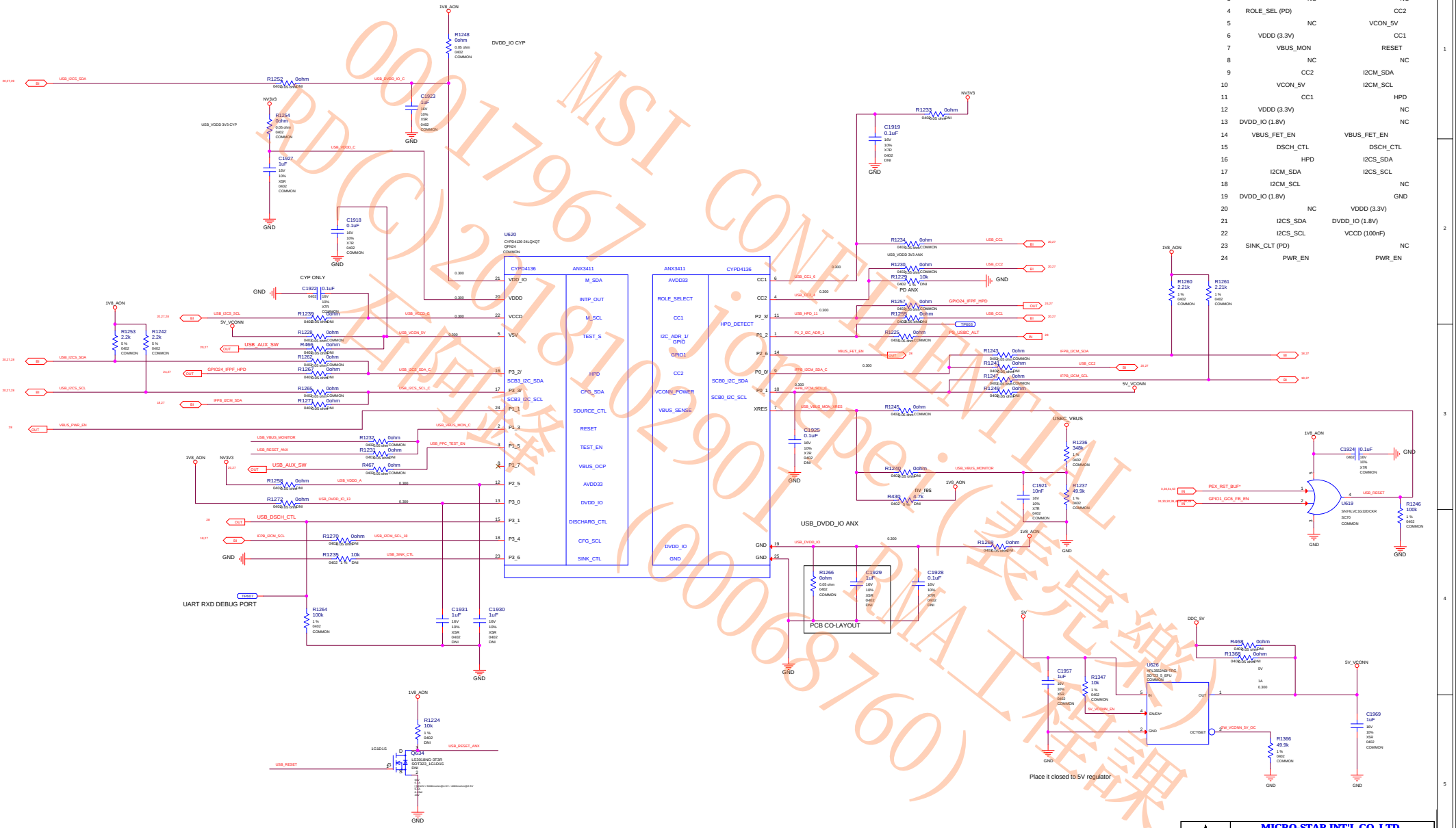
PAGE 27: MISC: USB PPC

PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN



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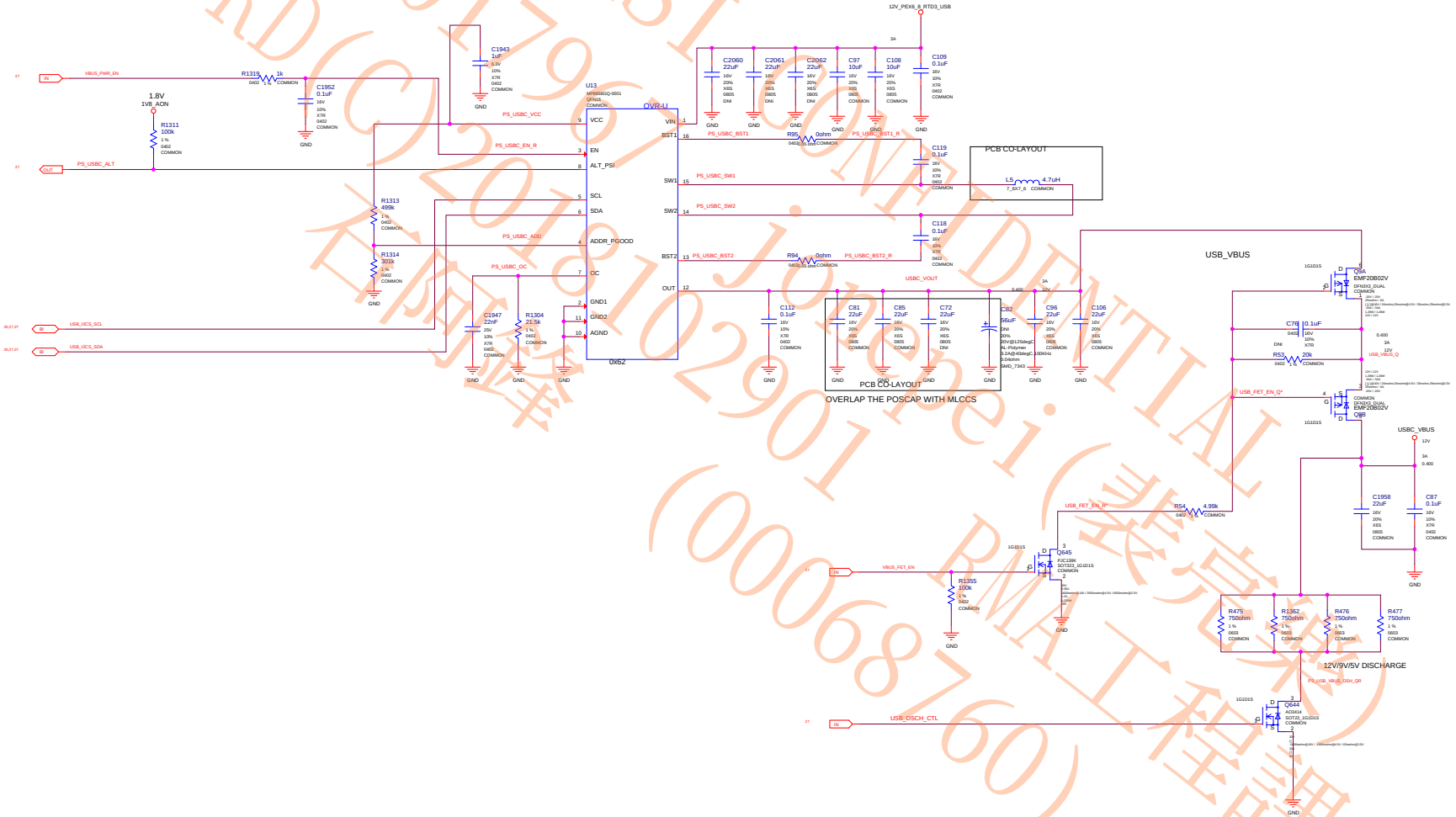
PAGE 28: PS: USB VR



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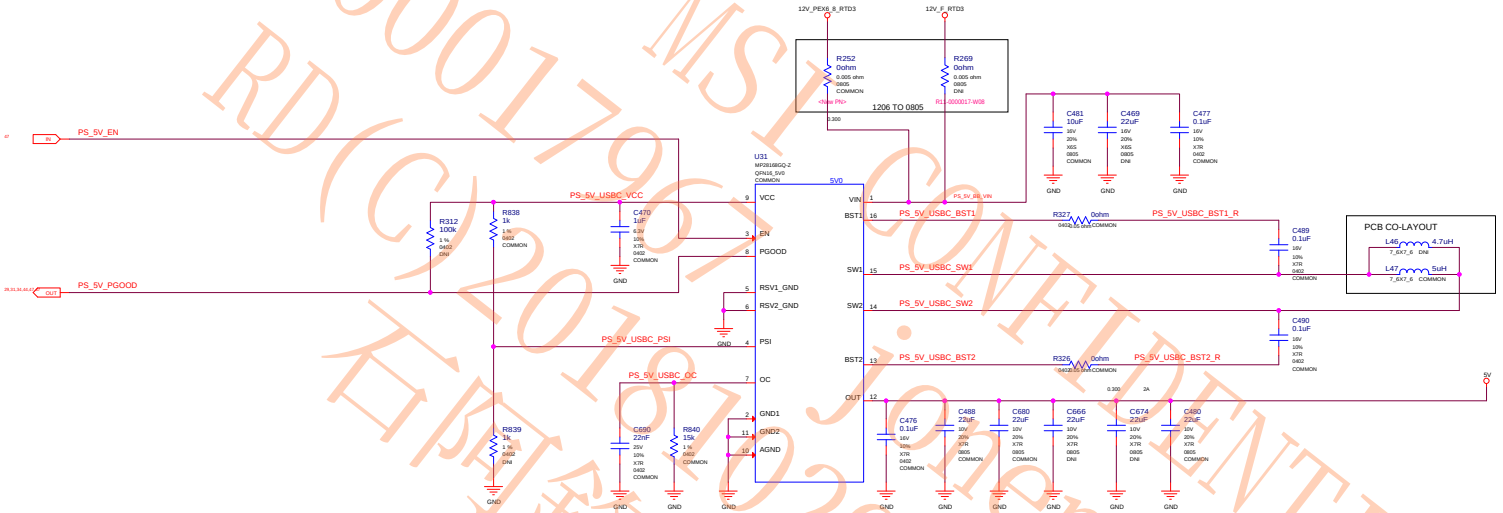
PAGE 29: PS: 5V, 5V_BACKUP



remove

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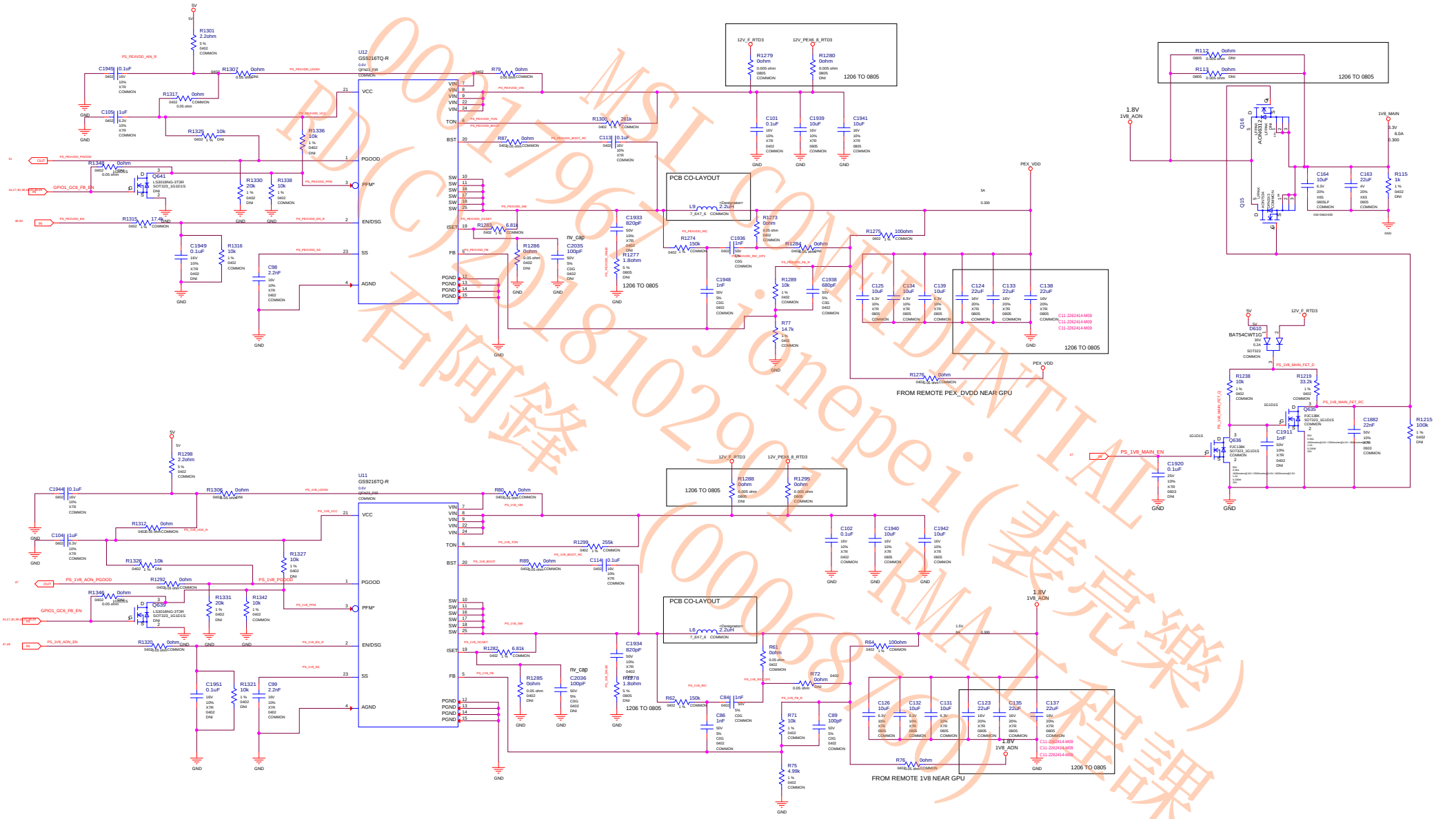
PAGE 30: PS: PEXVDD, 1V8



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Size: Custom	Document Description: Page30:PS_ PEXVDD, 1V8		Rev: 2.0
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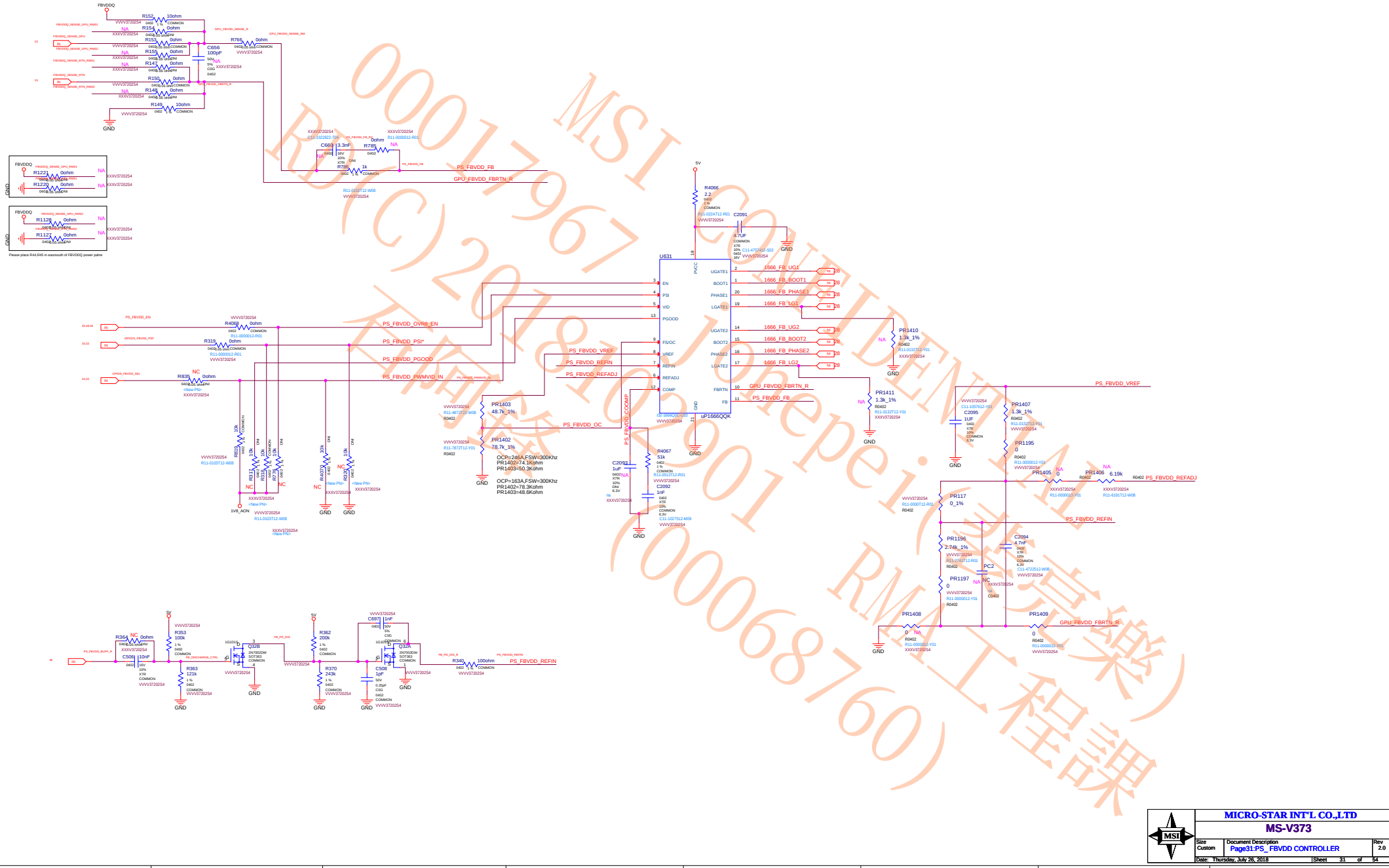
PAGE 31: PS: FBVDD Controller



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PAGE 32: PS: FBVDD Controller OVR3

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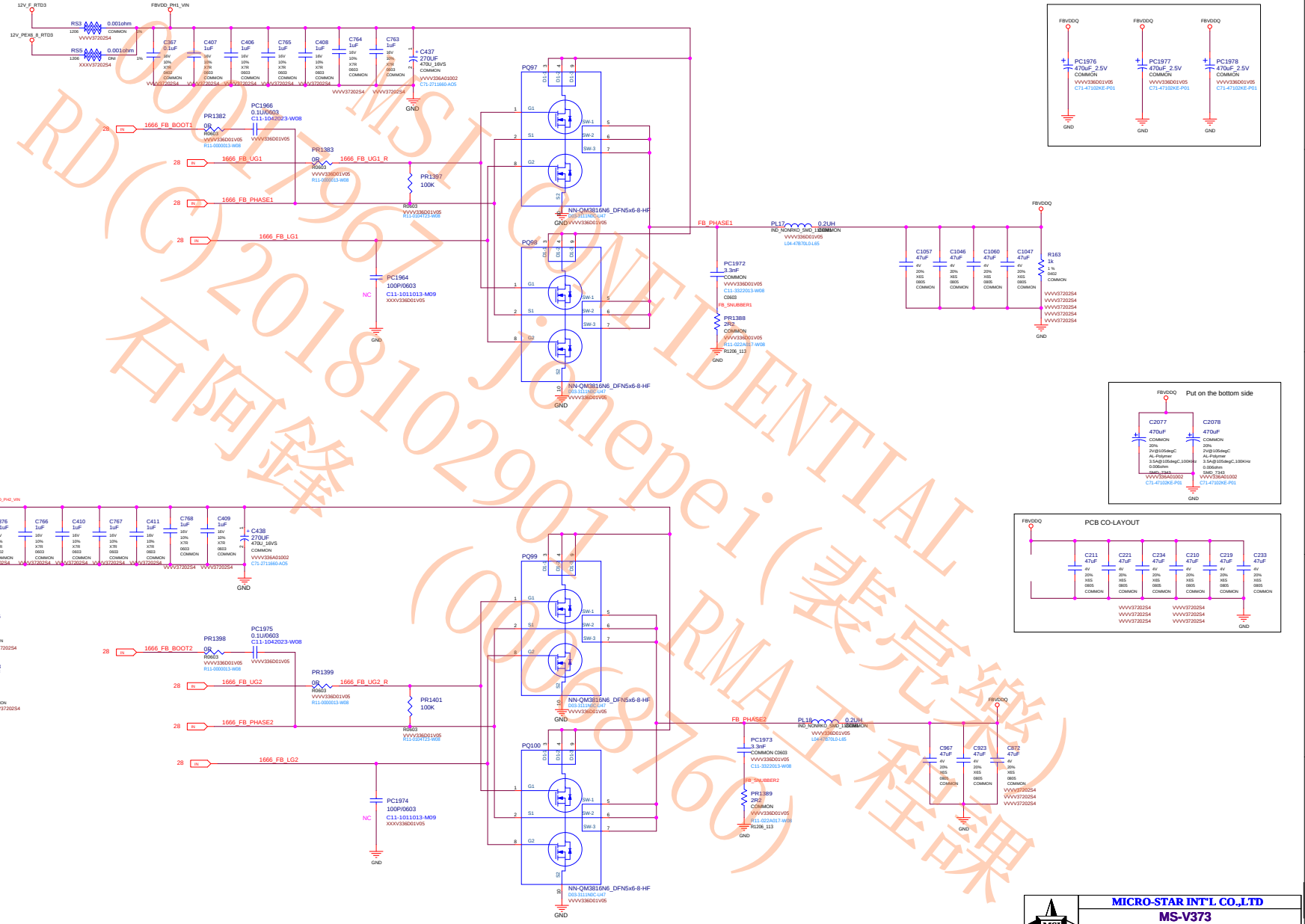
PAGE 33: PS: FBVDD Phase 1, 2



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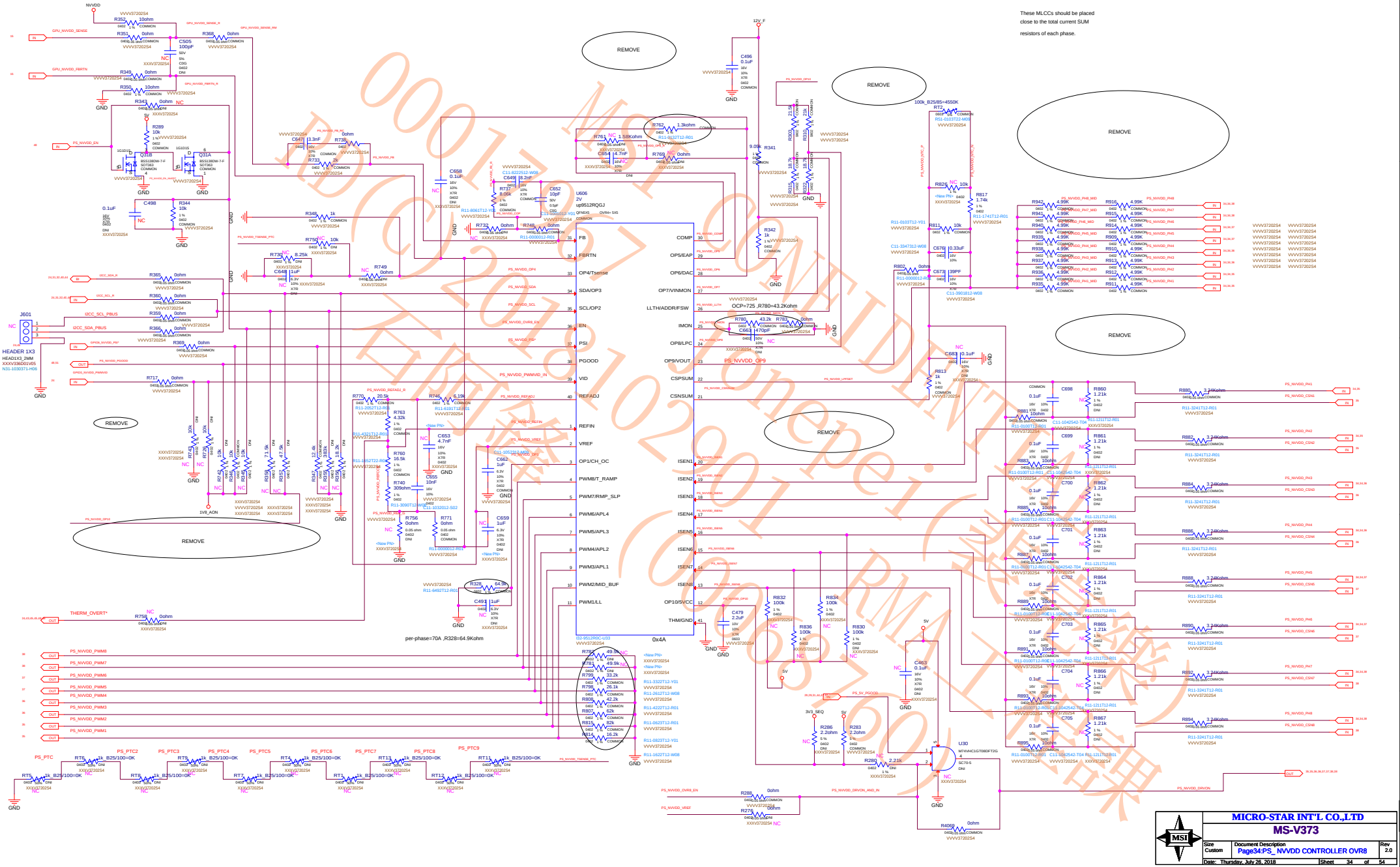
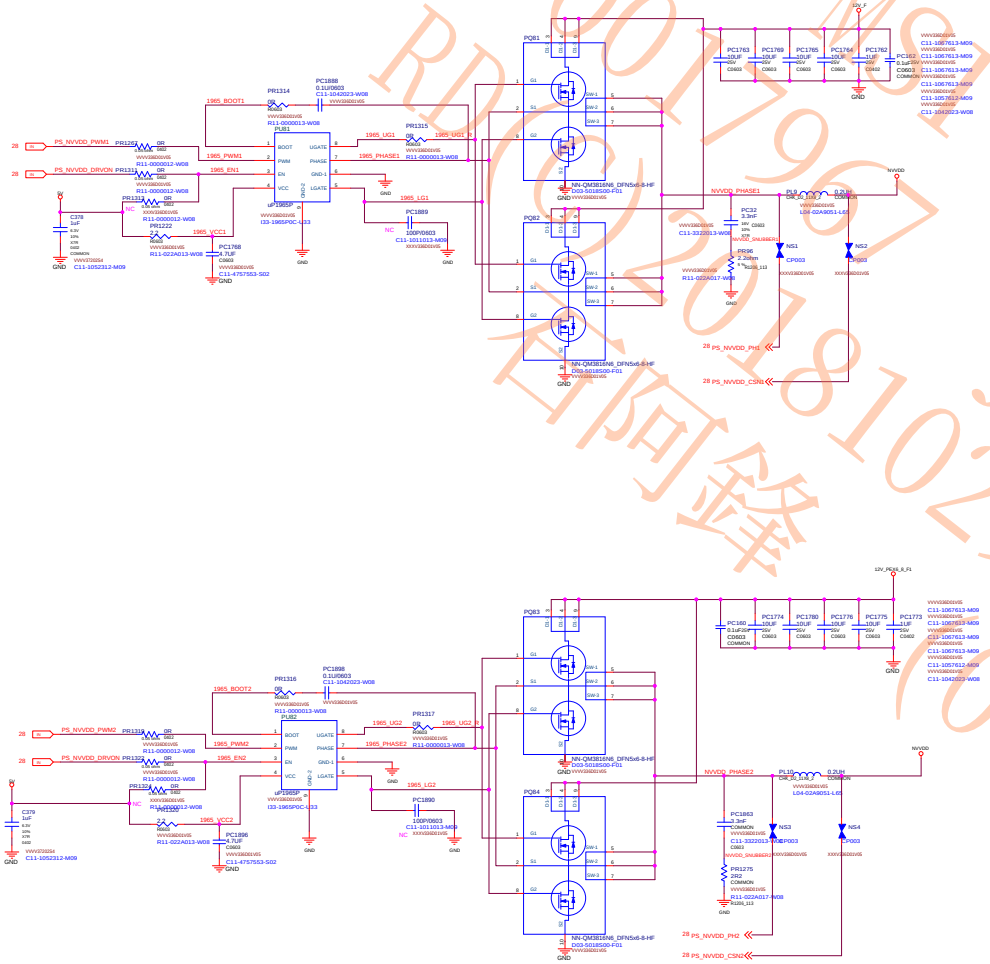
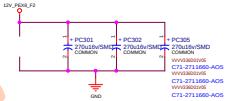
PAGE 34: PS: NVVDD Controller OVR8

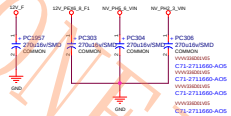


PAGE 35: PS: NVVDD Phase 1, 2

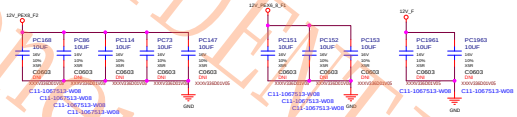


EXT_12V Input CAP





Backup



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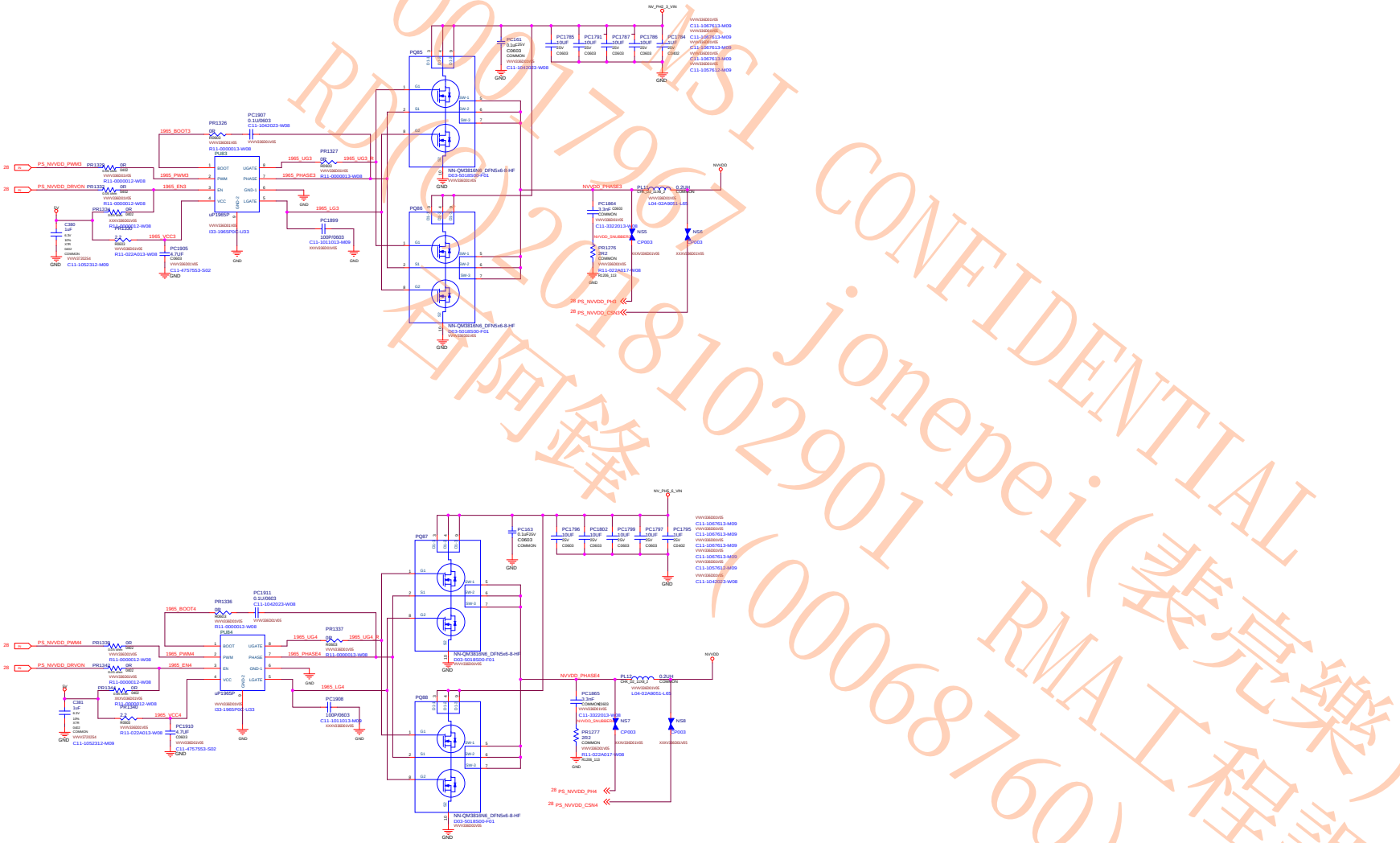

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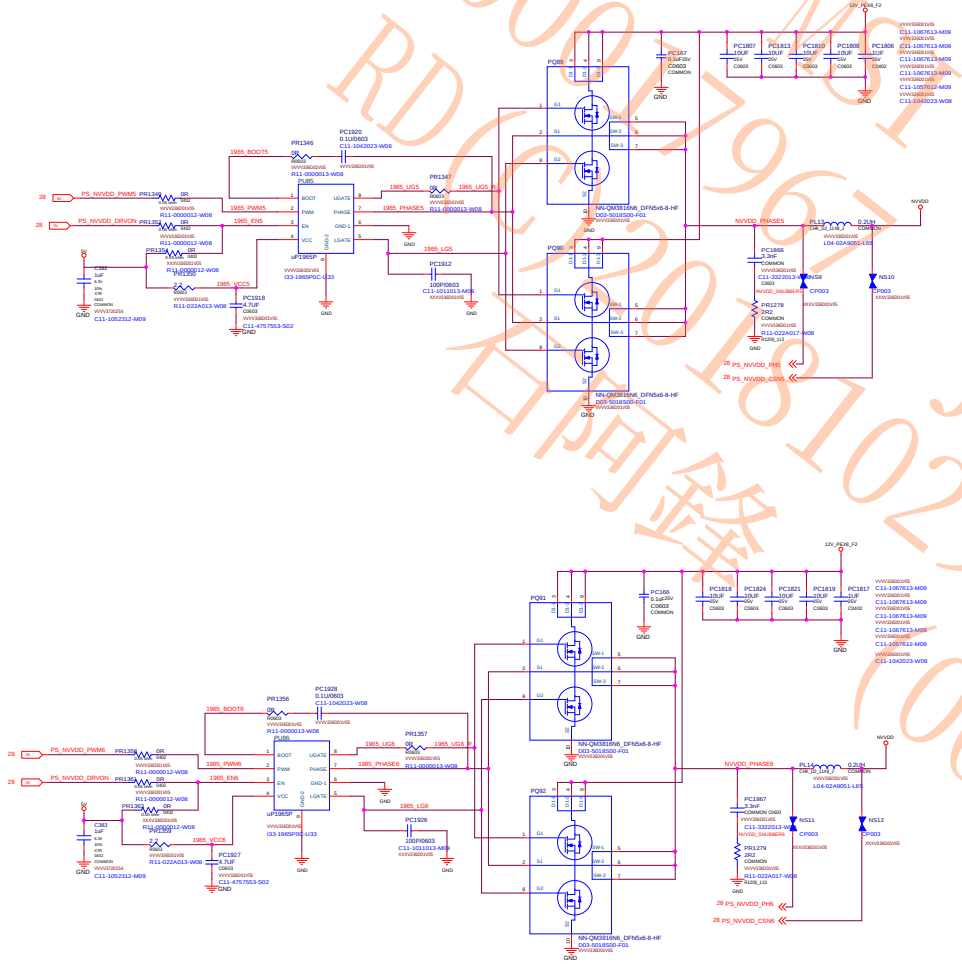

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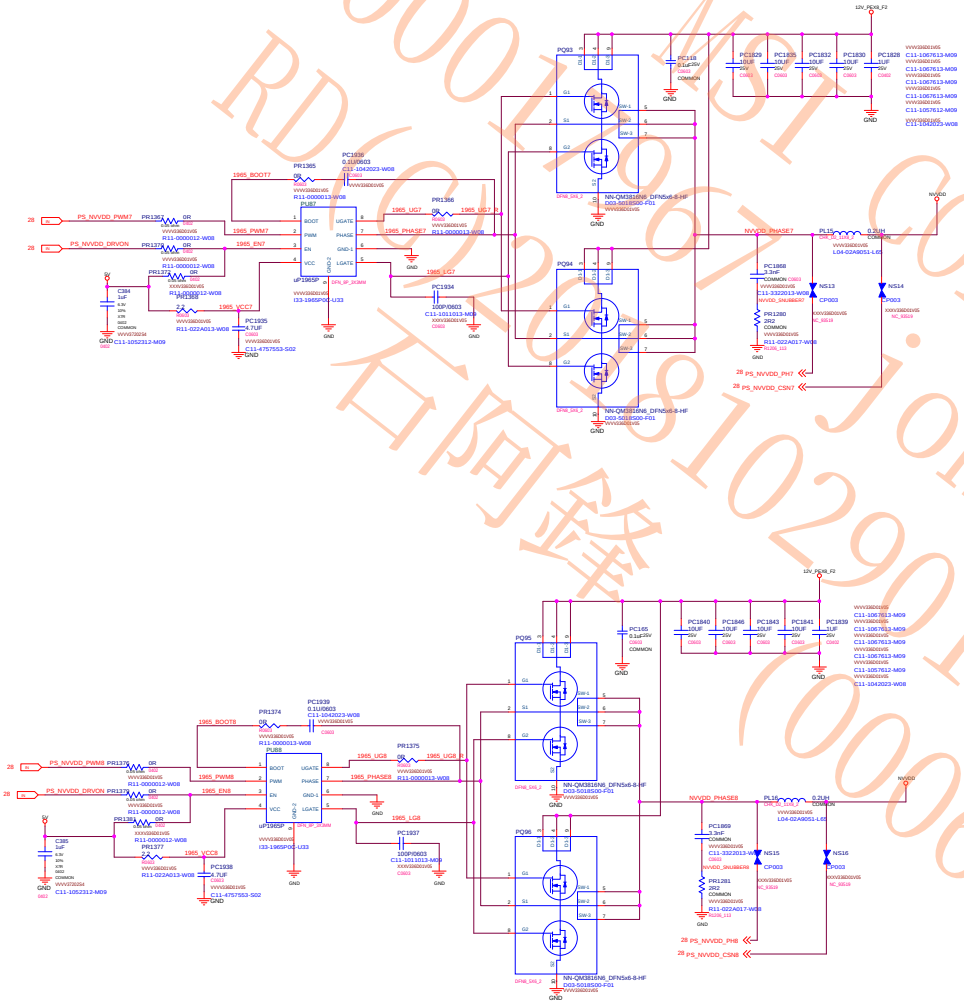

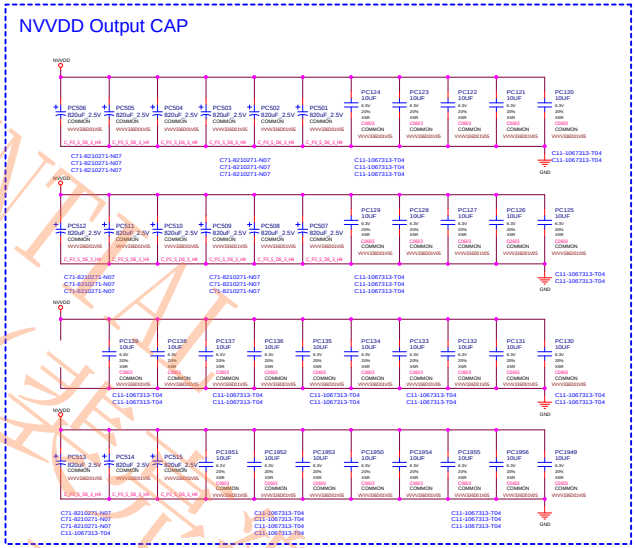

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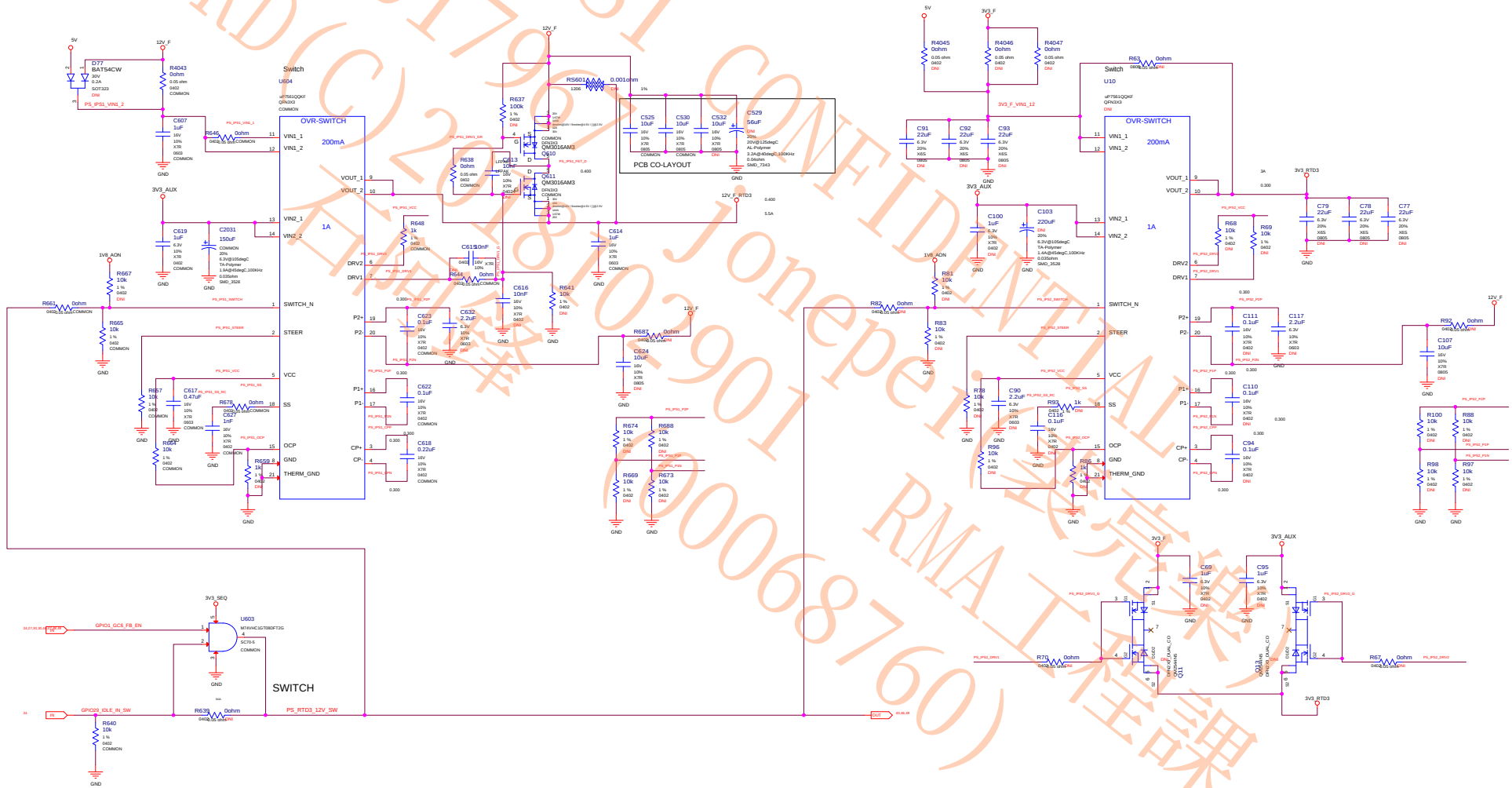
AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



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Size: Custom	Document Description: Page39:PS_ INPUT SWITCH RTD3	Rev: 2.0
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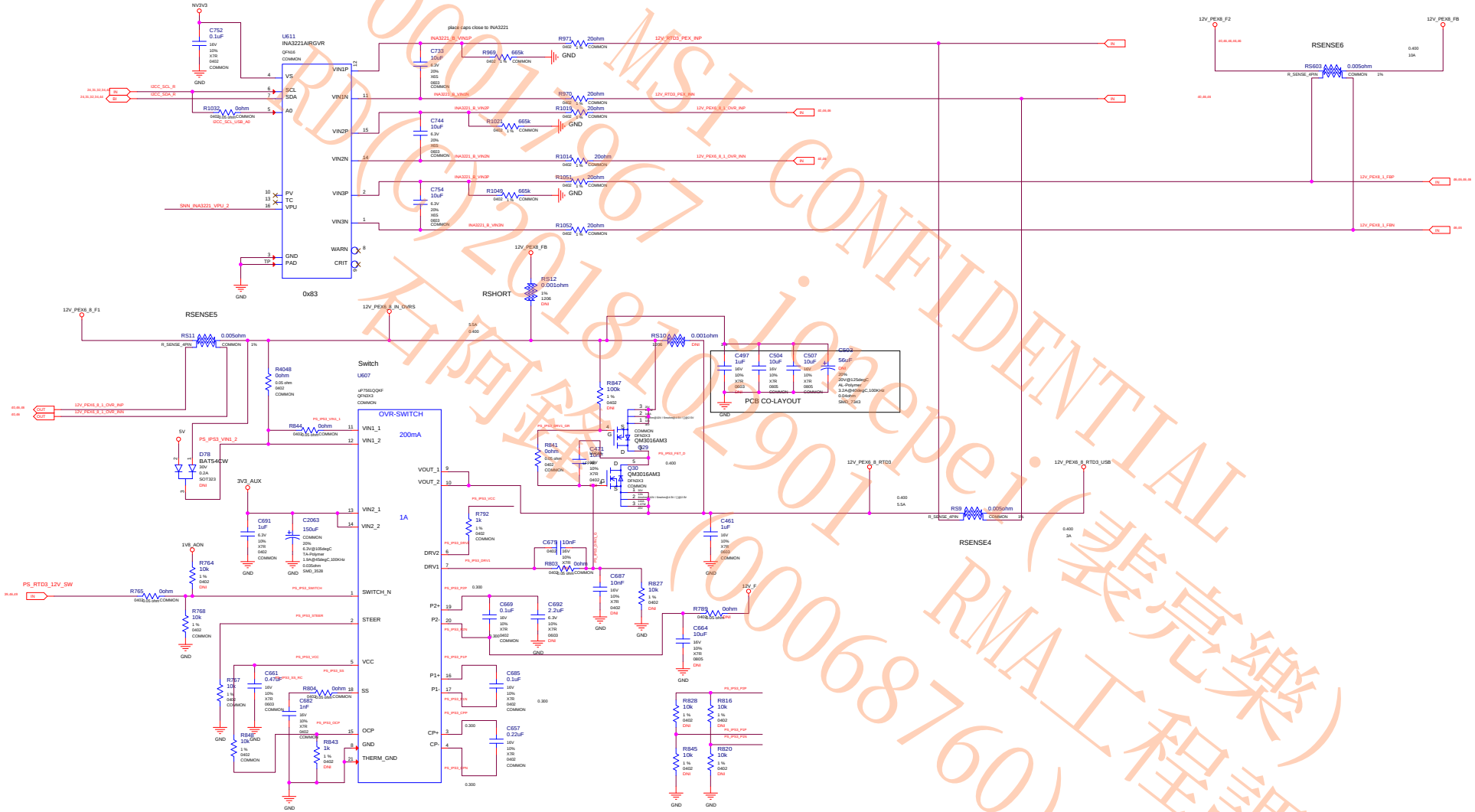

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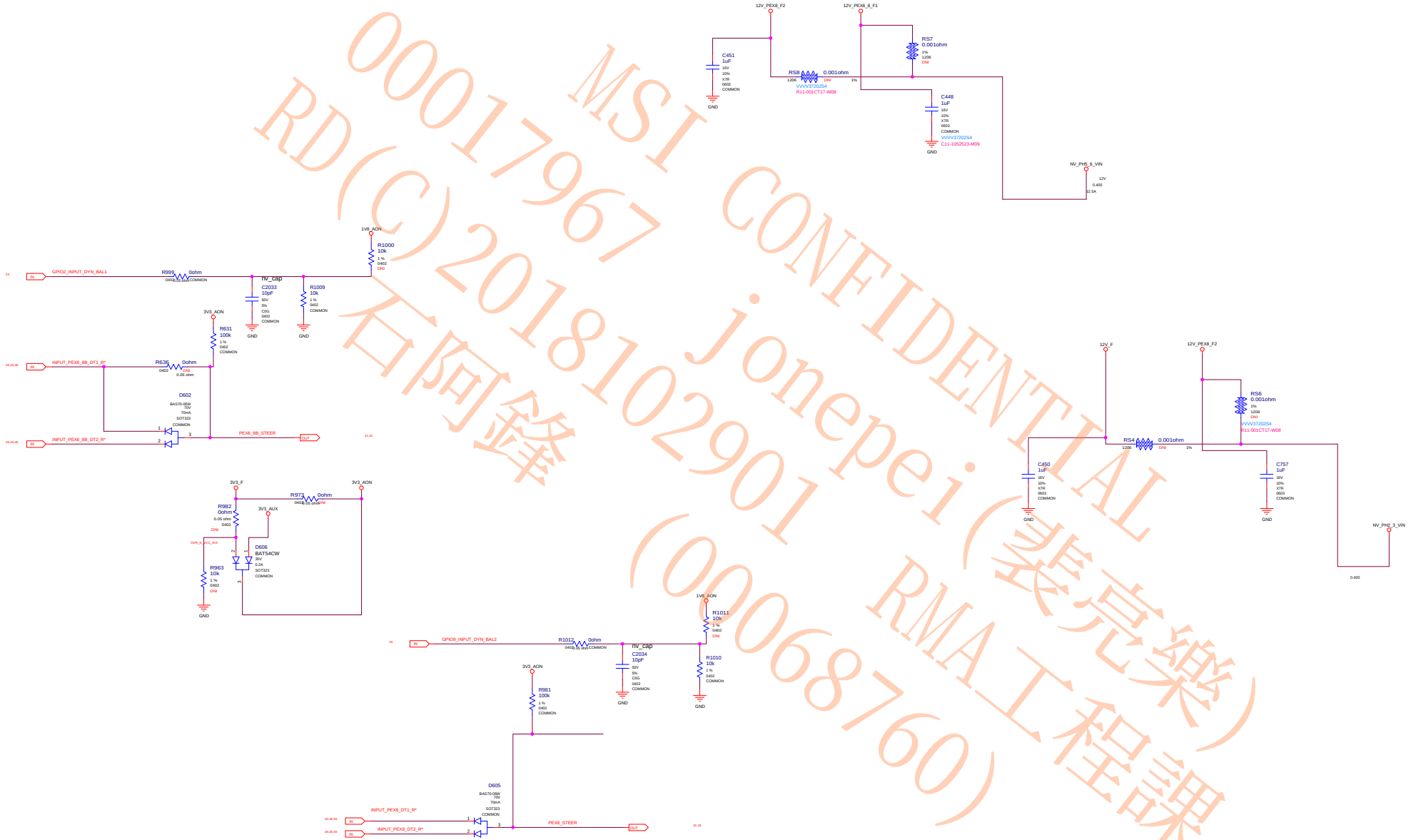
PAGE 41: PS: INPUT SWITCH Rail Balance



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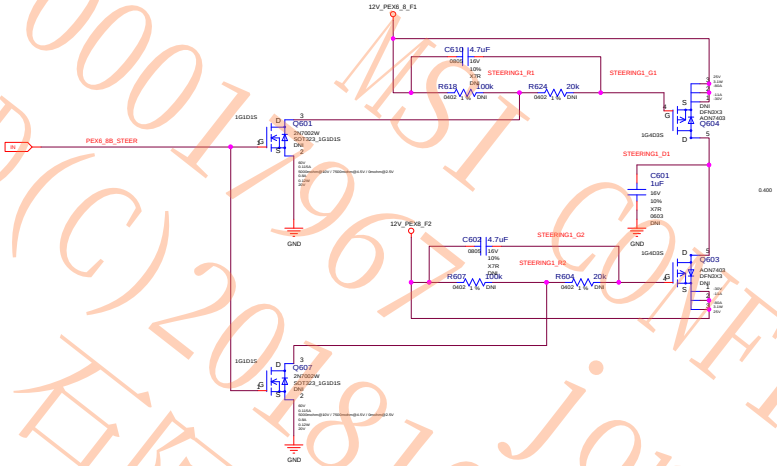
PAGE 42: PS: 12V CURRENT STEERING

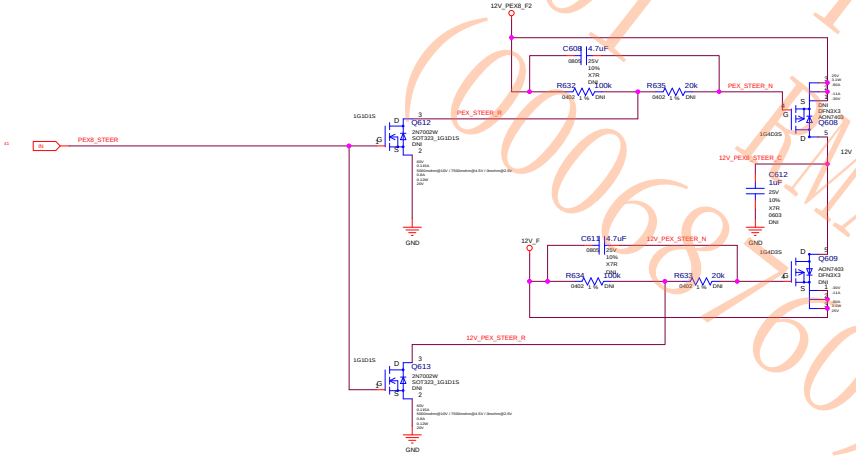
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



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PAGE 43: PS: VR THERMAL PROTECTION

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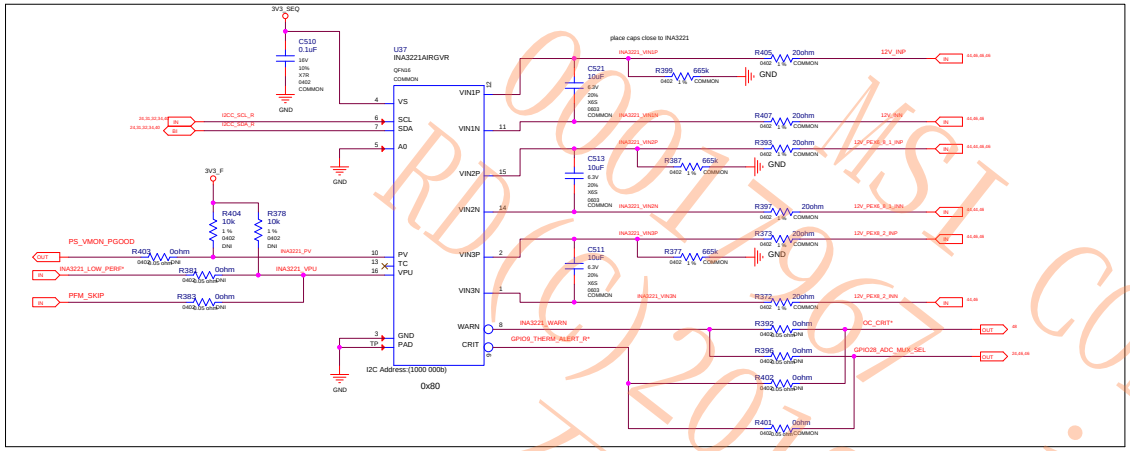
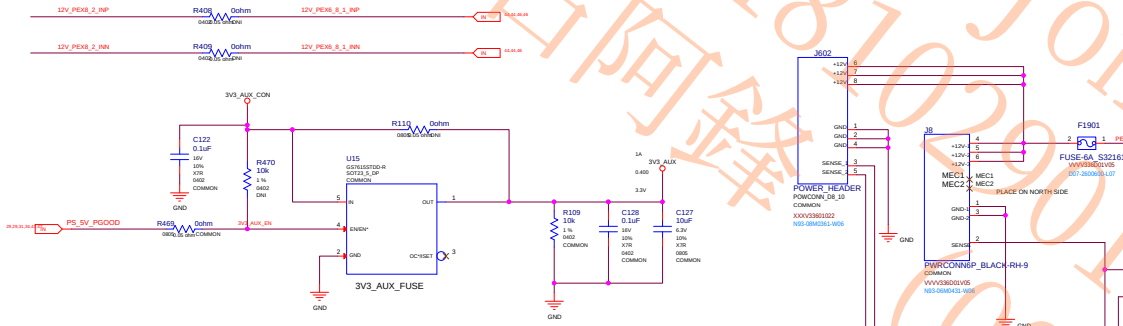
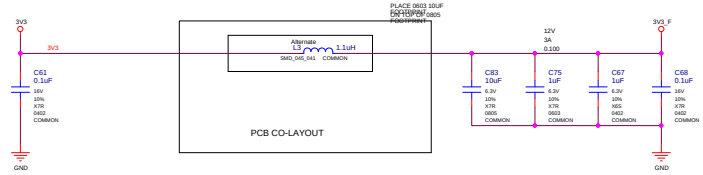
PAGE 44: PS: Inputs, Filtering, and Monitoring



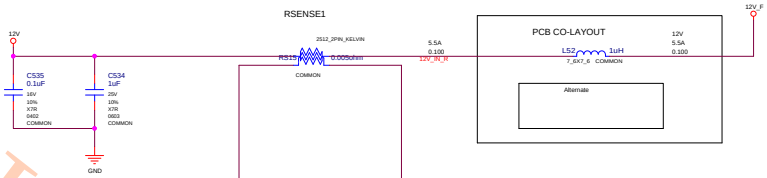
PEX6 INPUT 1 - 2x3 PCIE CON 75W

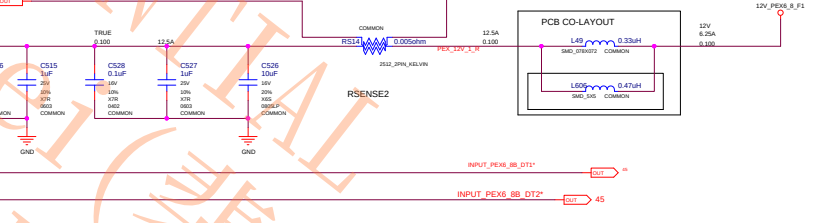


PEX 3V3 INPUT - 10W

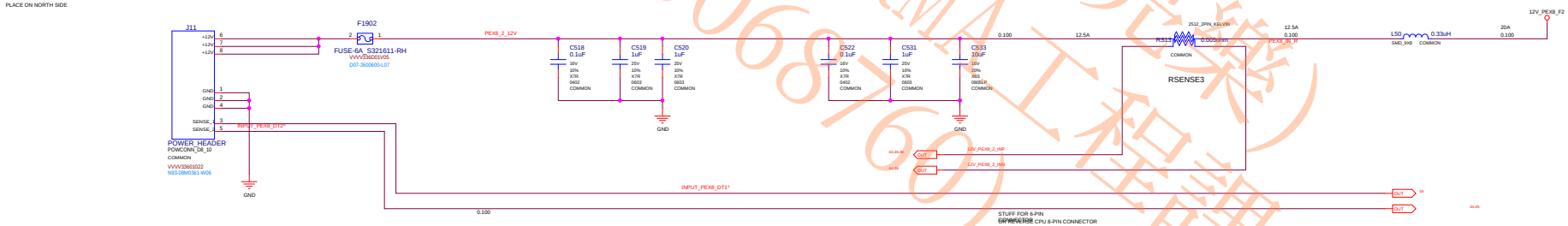


PEX_12V INPUT - 66W





PEX8 INPUT 2 - 2x4 PCIE CON 150W



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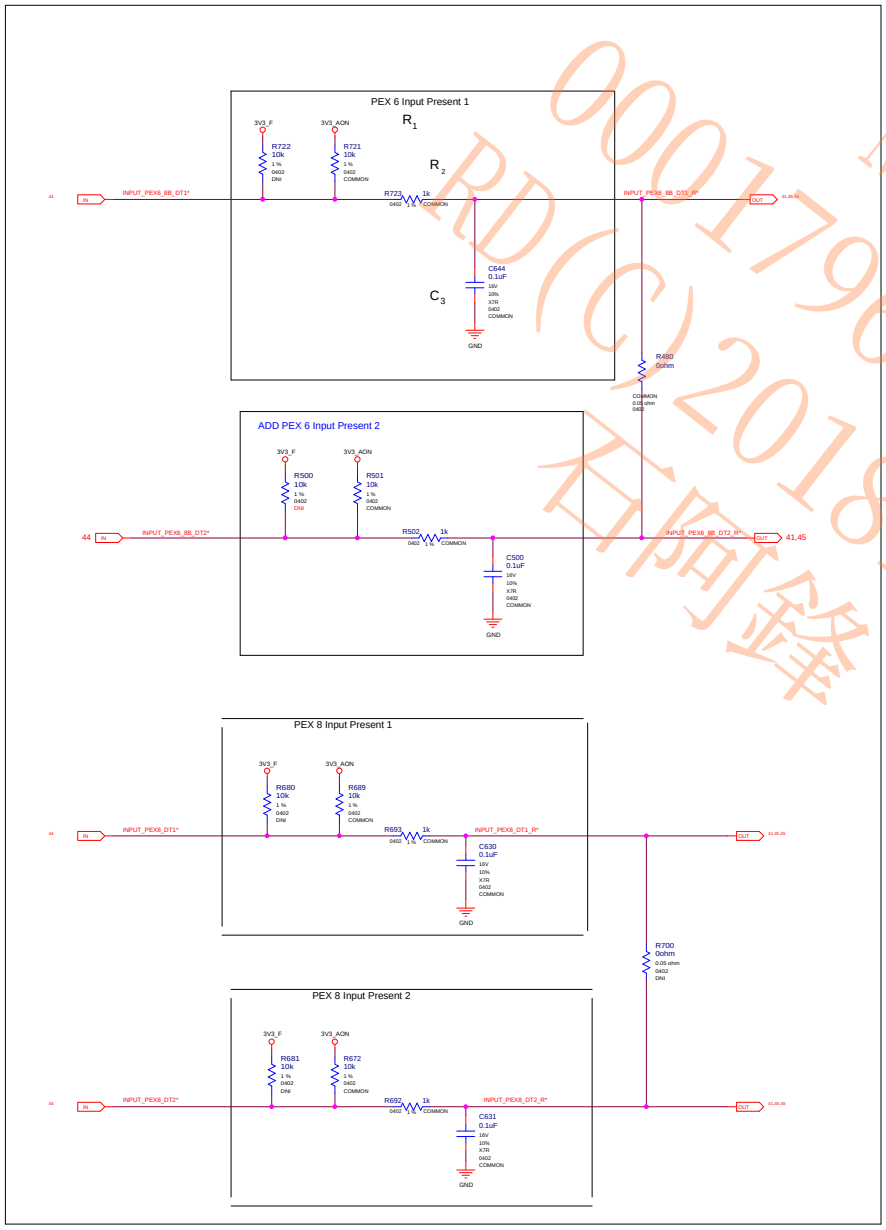
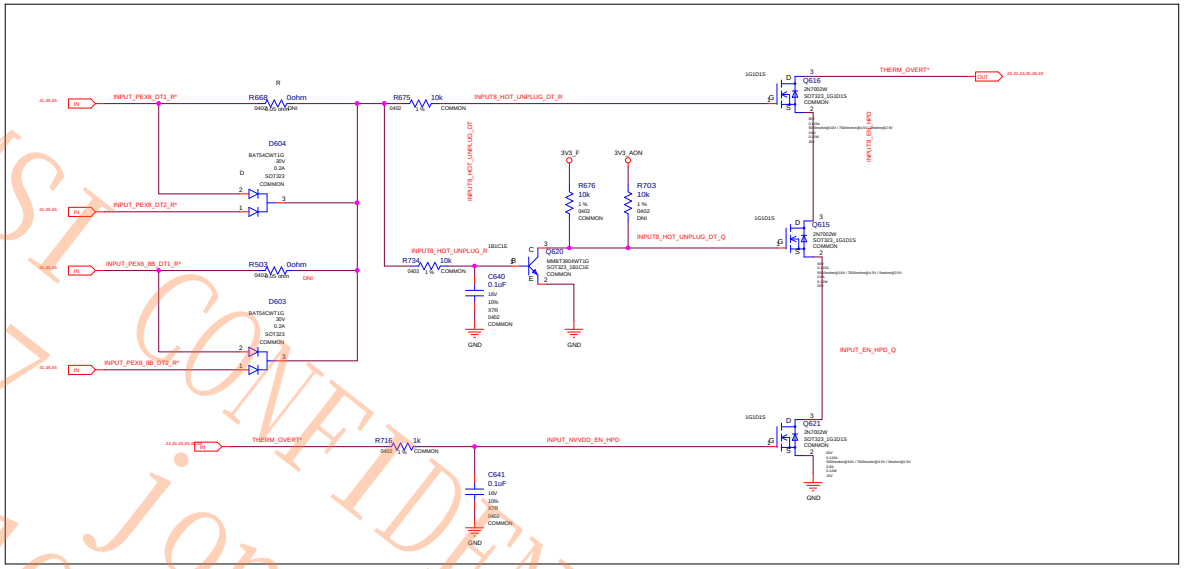
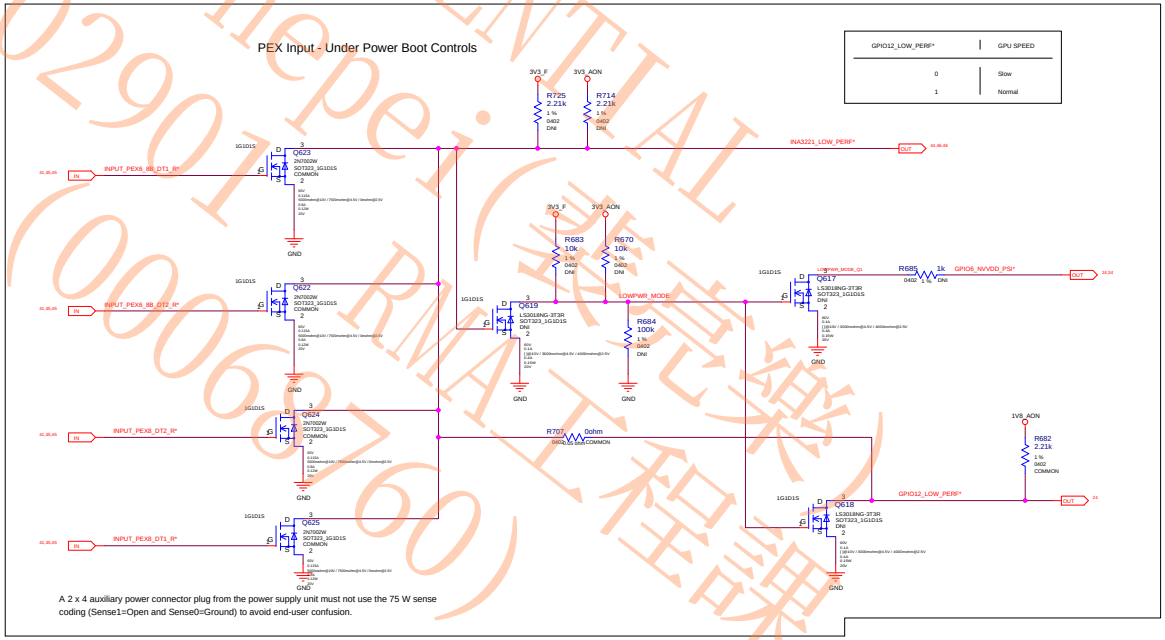
PAGE 45: PS: Current Steering, Hot Unplug Detect







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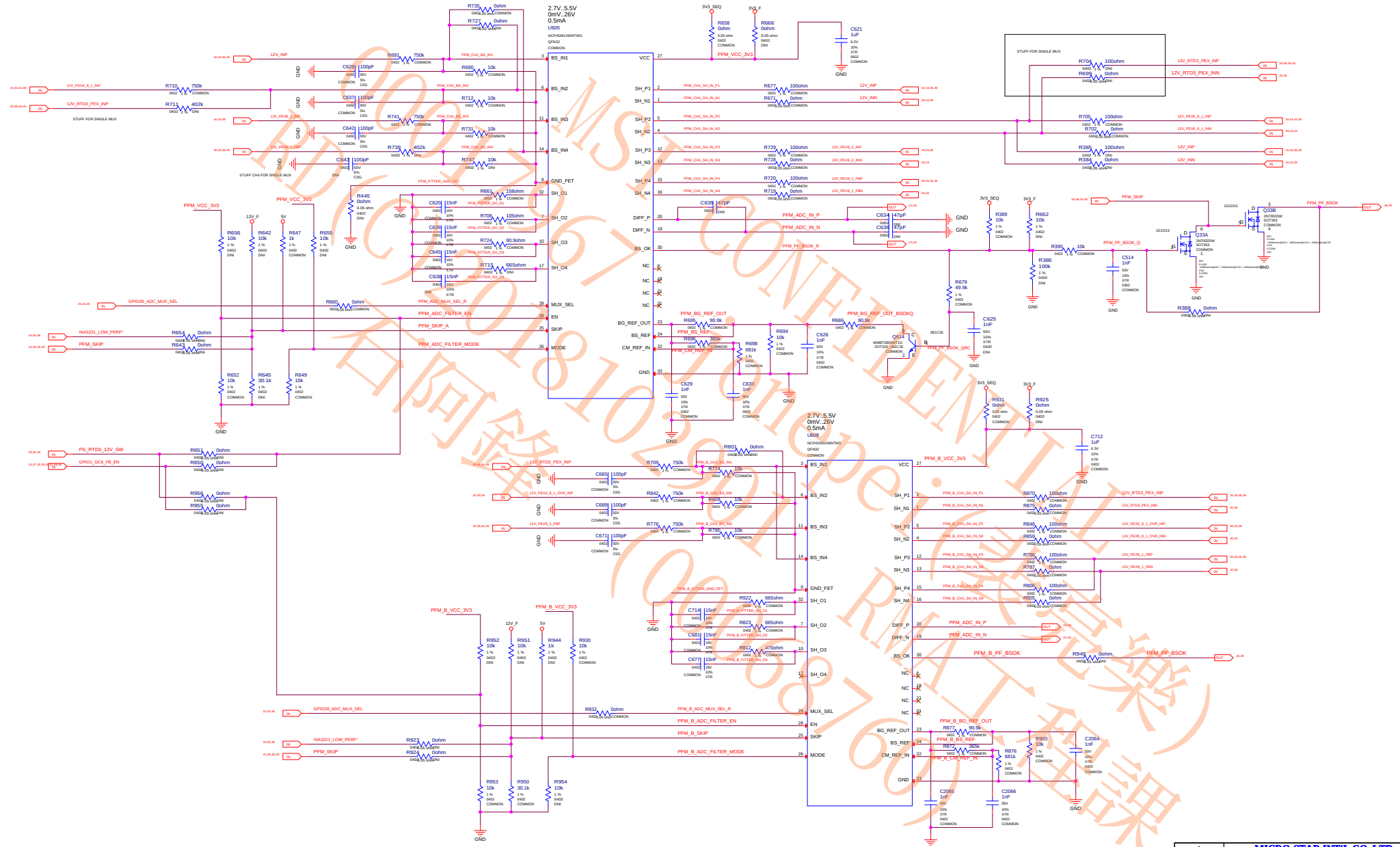
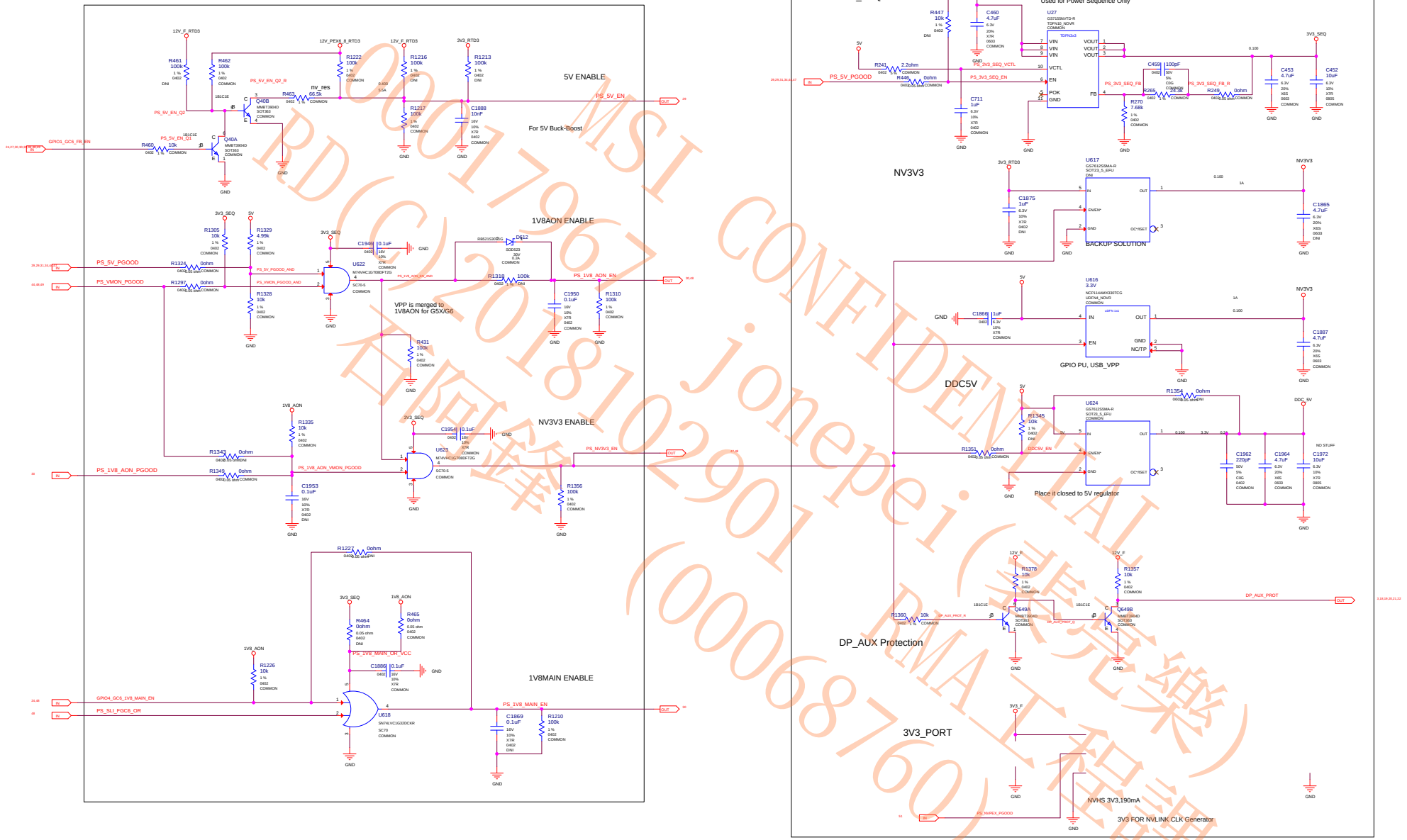
PAGE46; PS: Pre-Filter



PAGE 47: SEQUENCE:5V,1V8,NV3V3 ENABLE



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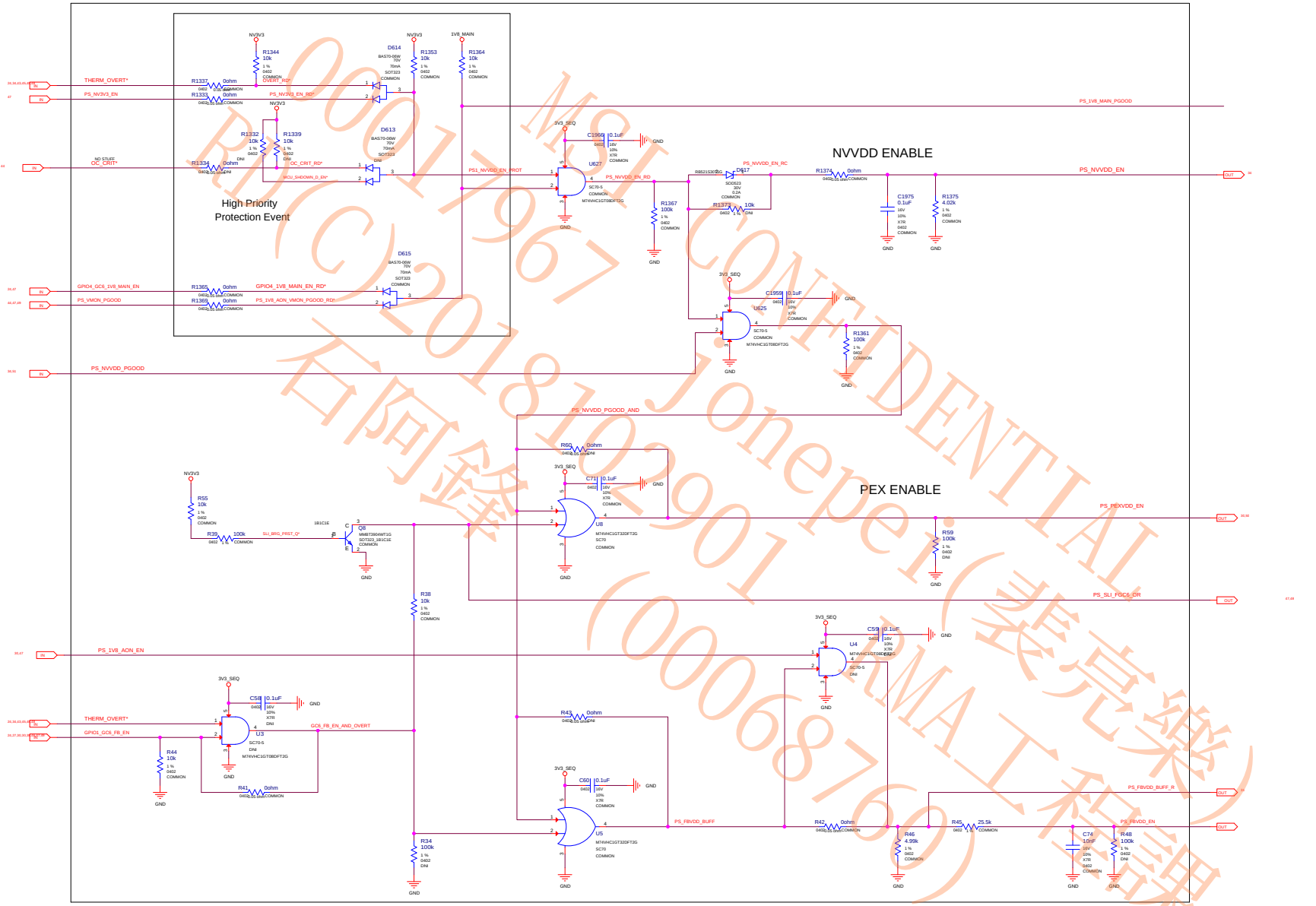
PAGE 48: SEQUENCE:NV,PEX,FB ENABLE



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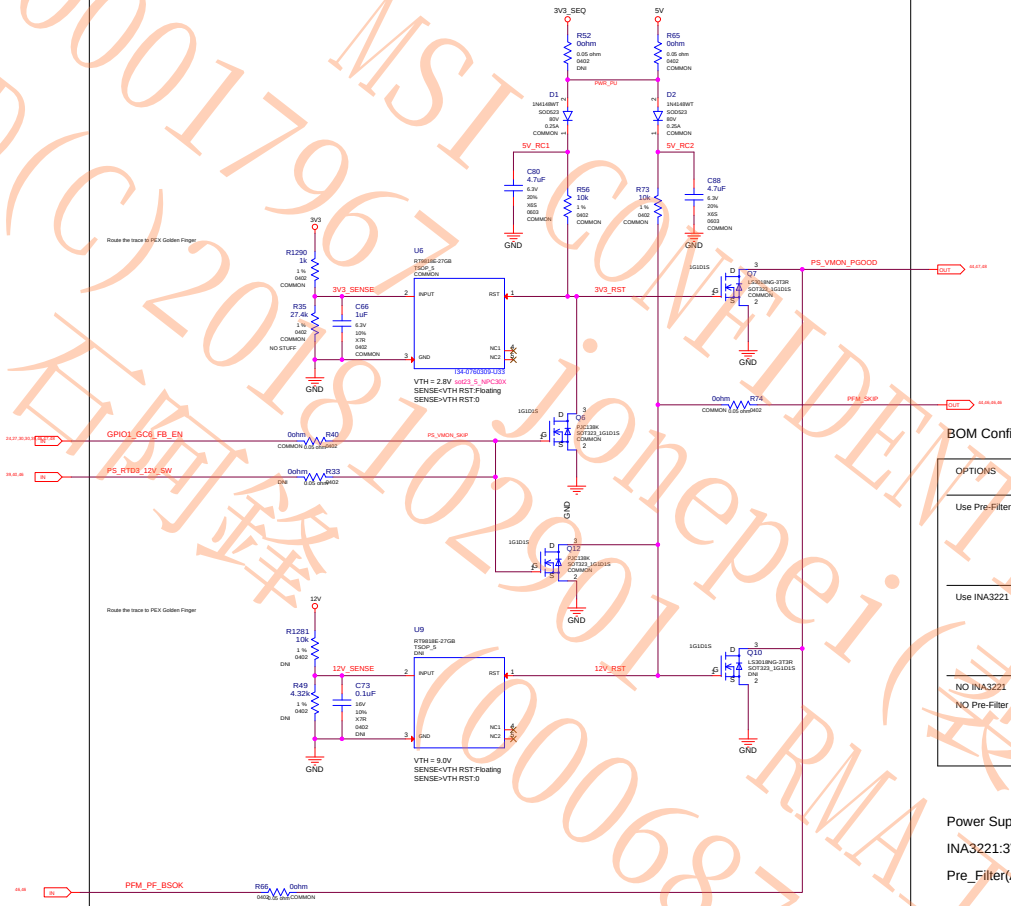
PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX and All Input 12Vs

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Size: Custom | Document Description: Page49:SEQUENCE_ PCIE VOLTAGE MON | Rev: 2.0
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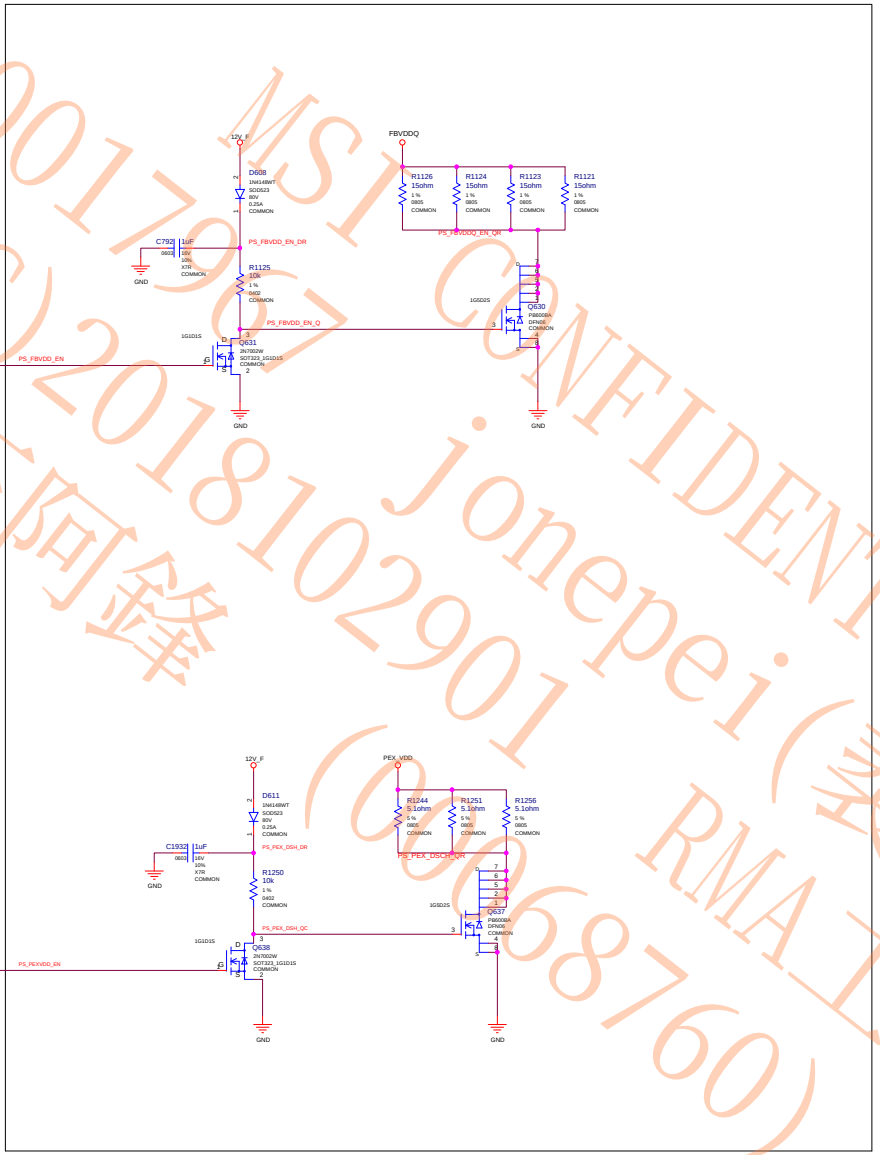
PAGE 50: SEQUENCE:DISCHARGE



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Size: Custom	Document Description: Page50:SEQUENCE_ DISCHARGE	Rev: 2.0
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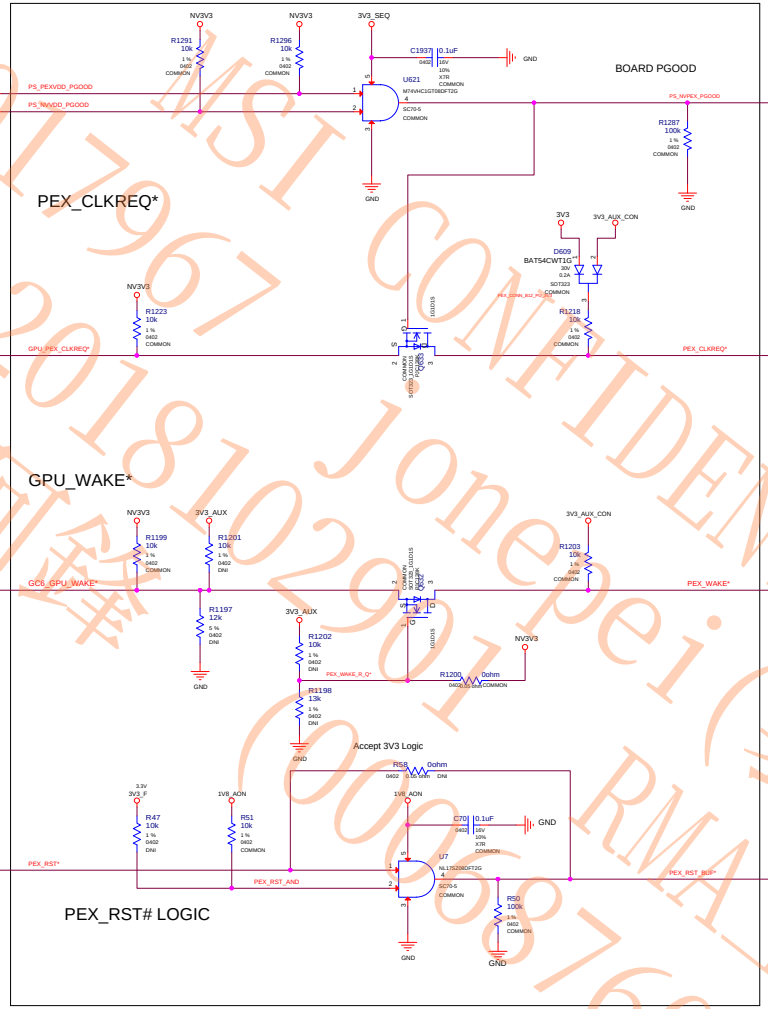
PAGE 51: SEQUENCE:MISC



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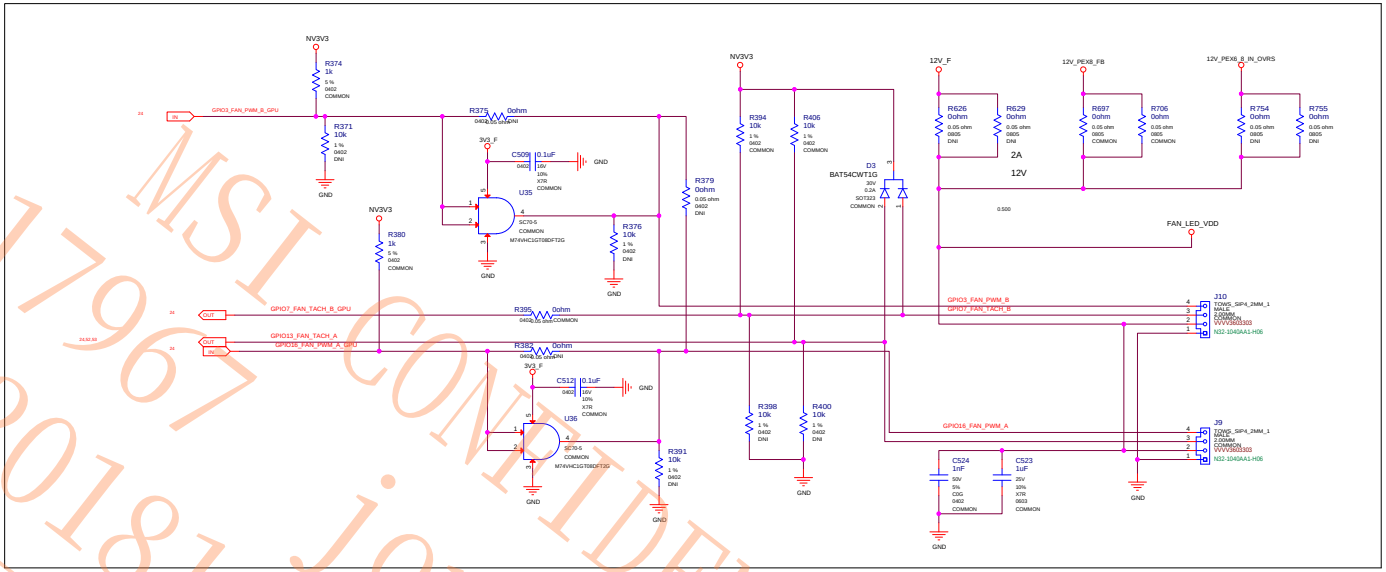
PAGE 52: LED & FAN HEADERS



LED BOOST

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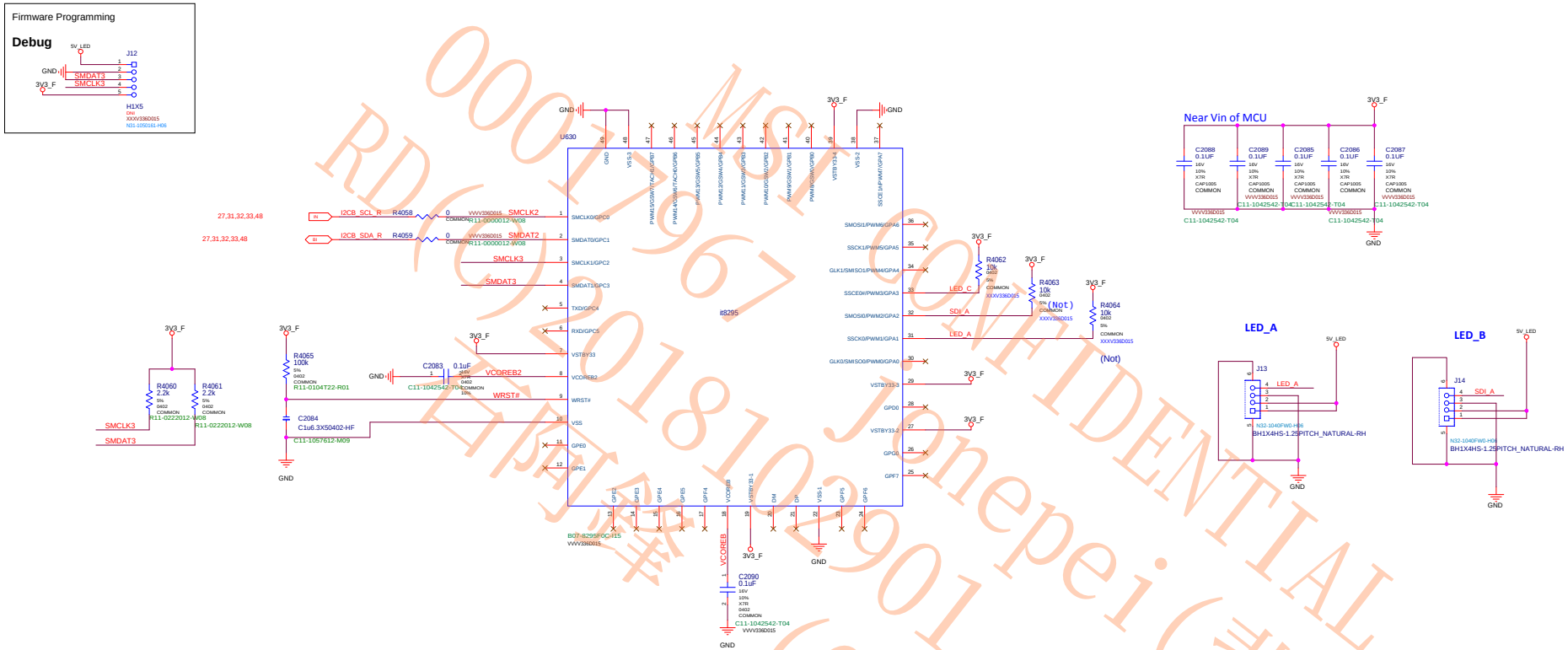

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PAGE 54:MECHANICAL;BRACKET/THERMAL SOLUTION

FAN
STIFFNER
NO PINS
VVVV3600708
OE3-V320001

HS1
STIFFNER
NO PINS
VVVV3600708
OE3-V320002

HS2
STIFFNER
NO PINS
VVVV3600708
OE3-V320101

PCIE
STIFFNER
NO PINS
VVVV3600708
E24-V320103-P08

Screw

BKTSCREW1
VVVV3600708
E41-1304009-H75

HDMISCREW1
VVVV3600708
E43-1303012-H75

TYPE-C
VVVV3600708
E43-1203040-P65

BKTSCREW2
VVVV3600708
E41-1304009-H75

HI_DP
VVVV3600708
E43-1203040-P65

BOARD STIFFENER
No connected mounting pins
MEC501
Back Cover
NOPIN
DNI

GPU Mounting holes
MEC4-1
MEC4-2
MEC4-3
MEC4-4
MEC4-5
MEC4-6
MEC4-7
MEC4-8
D18X
X8
DNI
GND

Brackets:

BKT1
BRACKET
ATX_2X_2P
DNI
MECH MOUNTING ALL
GND

J18
impedence

J19
impedence

J17
X_PIN1*2

J16
X_PIN1*2

PCB
PCB
109-GN982-00A
COMMON
VVVV3600708
PD0-0V36060-T53

HDMI_FEE
HDMI
$$$$$$
HDMI_FEE
COMMON
VVVV3600708
YG1-RHDM003-000

STIFFENER

Mechanical Holes Symbol
MEC10
MEC11
MEC12
MEC13
MEC14
MEC15
MEC16
MEC17
MEC18
MEC19
H_R220D125
GND

FM1
FM2
FM3
FM4
FM5
FM6
FM7
FM8
OPT
F_PAD_X

GPU Socket Symbol
BGA SOCKET ASSY
12 connected mounting pins
MEC3
SOCKET_BGA
128PIN
DNI
GND

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