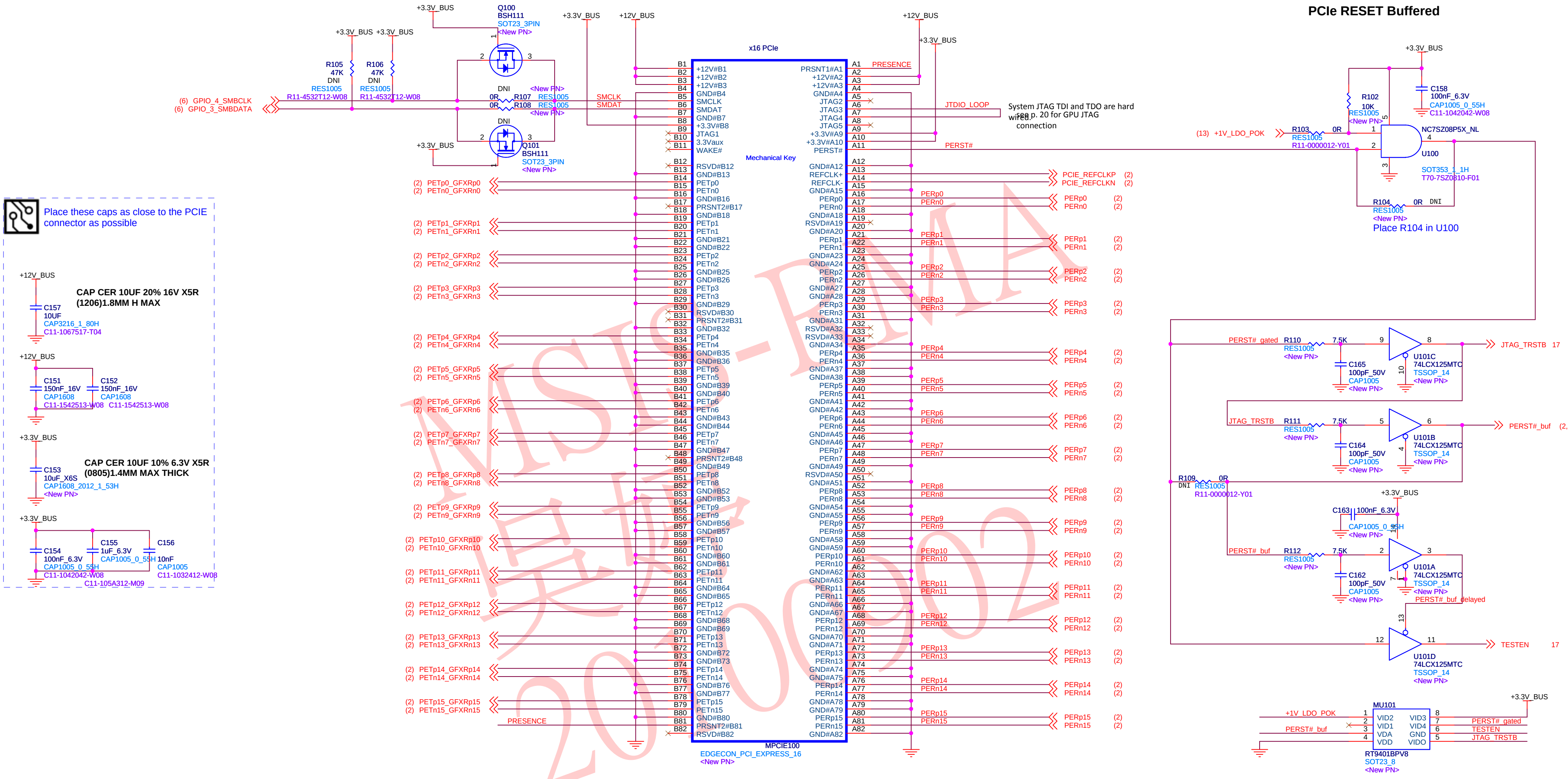
V215-20 REDWOOD DDR3 64*16 *8 1GB

PCI-EXPRESS EDGE CONNECTOR

REDWOOD
ROGUE



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
⏚	DIGITAL GROUND
⏚	ANALOG GROUND
BUO	BRING UP ONLY

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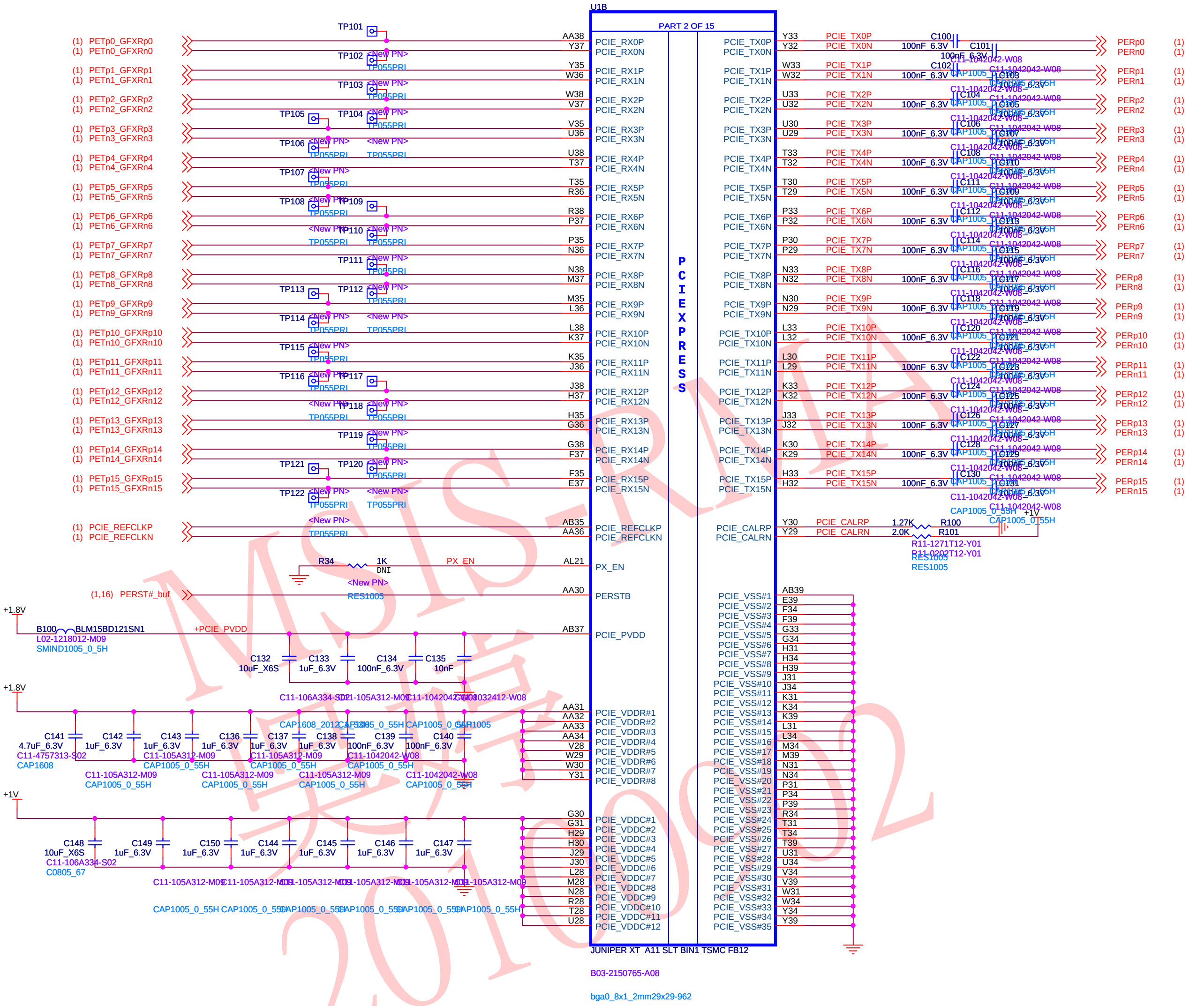
(2) REDWOOD PCIe Interface

NOTE: Some of the PCIE testpoints will be available through vias on traces.



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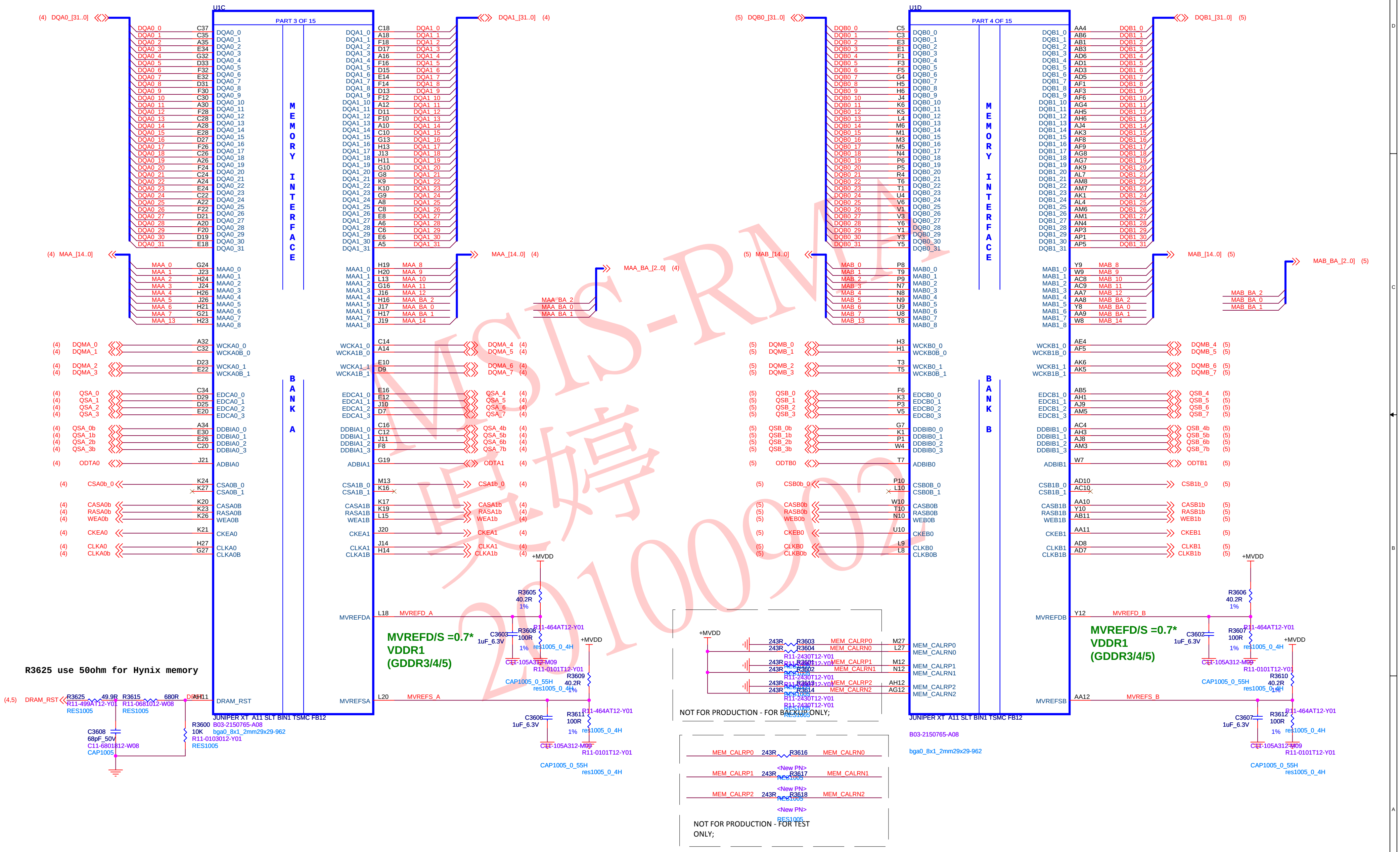
(3) REDWOOD MEM Interface Ch A&B



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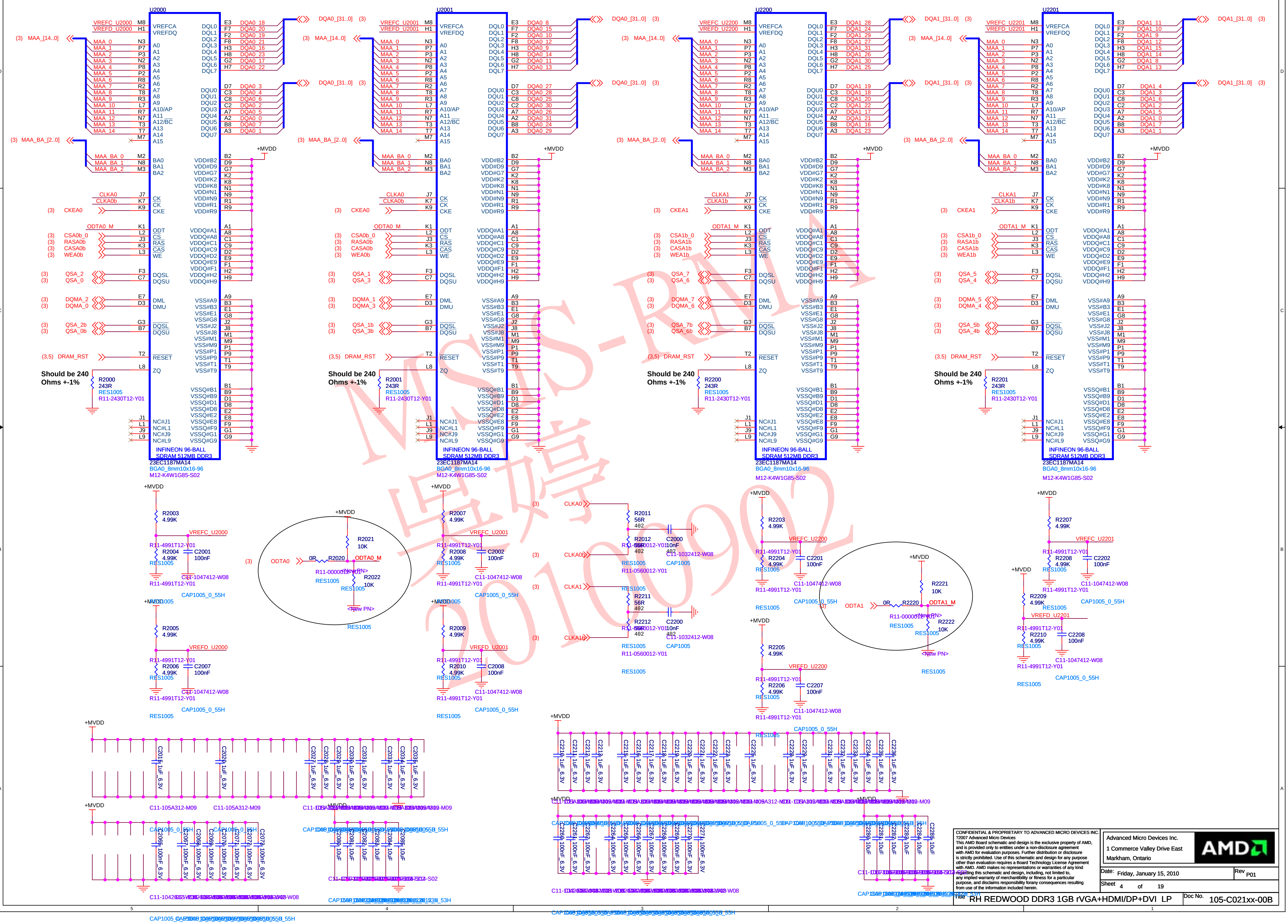
(4) DDR3 Memory Channel A



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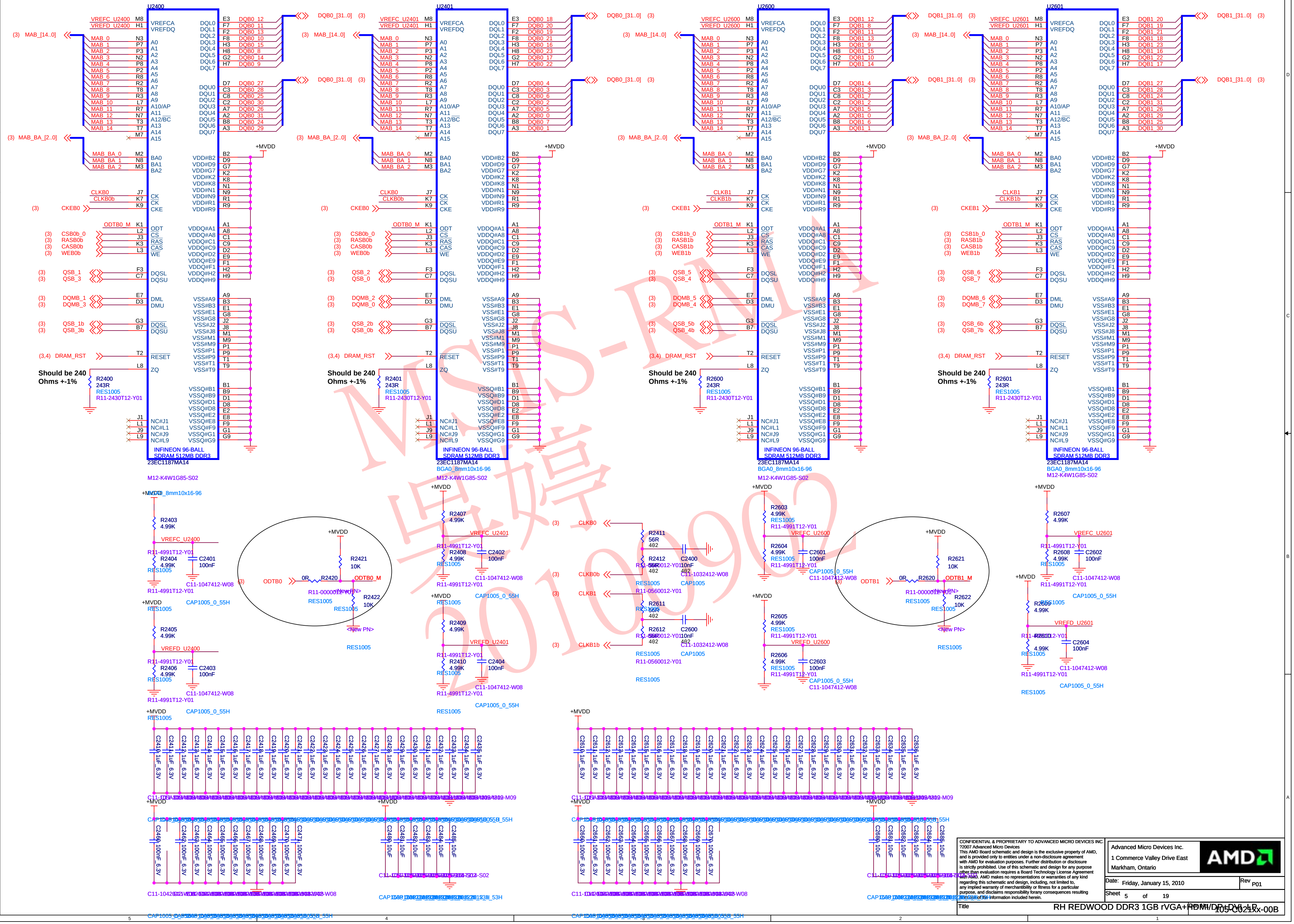
(5) DDR3 Memory Channel B



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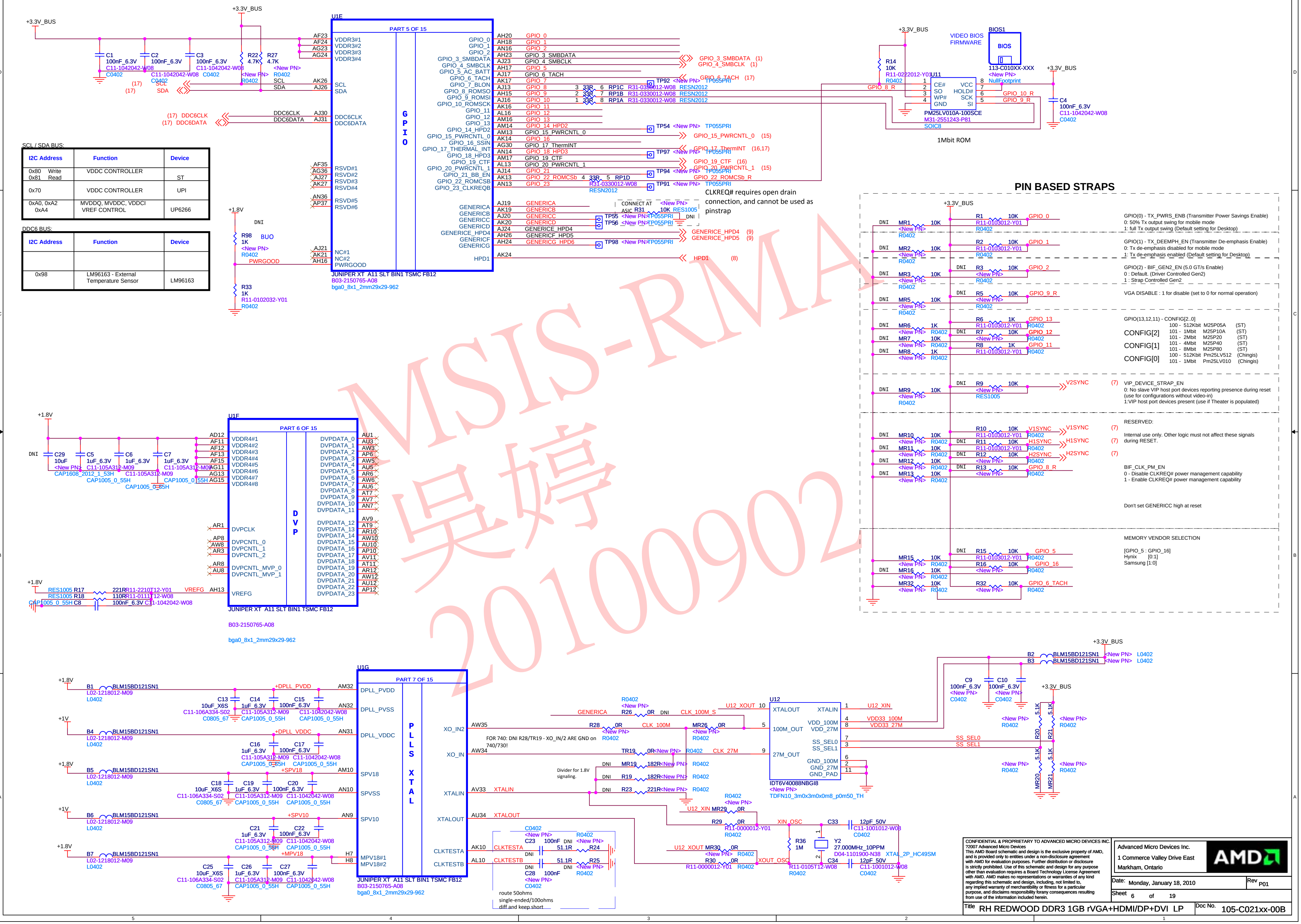
(06) REDWOOD GPIOs Strap CF XTAL OSC


+3.3V_BUS
U1E
PART 5 OF 15
VDDR3#1
VDDR3#2
VDDR3#3
VDDR3#4
SCL
SDA
DDC6CLK
DDC6DATA
RSVD#1
RSVD#2
RSVD#3
RSVD#4
RSVD#5
RSVD#6
NC#1
NC#2
PWRGOOD
GPIO
GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6_TACH
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
GENERICF_HPD5
GENERICG
HPD1
JUNIPER XT A11 SLT BIN1 TSMC FB12
B03-2150765-A08
bga0_8x1_2mm29x29-962
C1 100nF_6.3V C11-1042042-W08 C0402
C2 100nF_6.3V C11-1042042-W08 C0402
C3 100nF_6.3V C11-1042042-W08 C0402
R22 4.7K R27 4.7K <New PN> R0402
(17) SCL
(17) SDA
(17) DDC6CLK
(17) DDC6DATA
+1.8V
DNI
R98 1K BUO <New PN> R0402
PWRGOOD
R33 1K R11-0102032-Y01 R0402
GPIO_3_SMBDATA (1)
GPIO_4_SMBCLK (1)
GPIO_6_TACH (17)
TP92 <New PN> TP055PRI
RP1C RP1B RP1A 33R R31-0330012-W08 RESN2012
TP54 <New PN> TP055PRI
GPIO_15_PWRCNTL_0 (15)
GPIO_17_ThermINT (16,17)
TP97 <New PN> TP055PRI
GPIO_19_CTF (16)
GPIO_20_PWRCNTL_1 (15)
TP94 <New PN> TP055PRI
GPIO_22_ROMCSb_R
RP1D 33R R31-0330012-W08 RESN2012
TP91 <New PN> TP055PRI
CONNECT AT ASIC R31 10K <New PN> RES1005 DNI
TP55 TP56 <New PN> TP055PRI
GENERICE_HPD4 (9)
GENERICE_HPD5 (9)
TP98 <New PN> TP055PRI
HPD1 (8)
VIDEO BIOS FIRMWARE
BIOS1 BIOS 113-C010XX-XXX <New PN> NullFootprint
R14 10K R11-0222012-Y01 R0402
U11 CE# SO WP# GND VCC HOLD# SCK SI
PM25LV010A-100SCE M31-2551243-P81 SOIC8
GPIO_8_R GPIO_10_R GPIO_9_R
C4 100nF_6.3V C11-1042042-W08 C0402
1Mbit ROM
PIN BASED STRAPS
MR1 10K R1 10K R11-0103012-Y01 GPIO_0
MR2 10K R2 10K GPIO_1
MR3 10K R3 10K GPIO_2
MR5 10K R5 10K GPIO_9_R
MR6 1K R6 1K GPIO_13
MR7 10K R7 10K GPIO_12
MR8 1K R8 1K GPIO_11
MR9 10K R9 10K RES1005 V2SYNC (7)
MR10 10K R10 10K V1SYNC (7)
MR11 10K R11 10K H1SYNC (7)
MR12 10K R12 10K H2SYNC (7)
MR13 10K R13 10K GPIO_8_R
MR15 10K R15 10K GPIO_5
MR16 10K R16 10K GPIO_16
MR32 10K R32 10K GPIO_6_TACH
+1.8V
U1F
PART 6 OF 15
VDDR4#1
VDDR4#2
VDDR4#3
VDDR4#4
VDDR4#5
VDDR4#6
VDDR4#7
VDDR4#8
DVPCLK
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_MVP_0
DVPCNTL_MVP_1
VREFG
DVP
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
C29 10uF <New PN> CAP1608_2012_1_53H
C5 1uF_6.3V C11-105A312-M09 CAP1005_0_55H
C6 1uF_6.3V C11-105A312-M09 CAP1005_0_55H
C7 1uF_6.3V C11-105A312-M09 CAP1005_0_55H
RES1005 R17 221R R11-2210012-Y01
RES1005 R18 110R R11-0111012-W08
CAP1005_0_55H C8 100nF_6.3V C11-1042042-W08
VREFG
U1G
PART 7 OF 15
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
SPV18
SPVSS
SPV10
MPV18#1
MPV18#2
PLLS XTAL
XO_IN2
XO_IN
XTALIN
XTALOUT
CLKTESTA
CLKTESTB
B1 BLM15BD121SN1 L02-1218012-M09 L0402 +DPLL_PVDD
C13 10uF_X6S C11-106A334-S02 C0805_67
C14 1uF_6.3V C11-105A312-M09 CAP1005_0_55H
C15 100nF_6.3V C11-1042042-W08 CAP1005_0_55H
+1V
B4 BLM15BD121SN1 +DPLL_VDDC
C16 1uF_6.3V C17 100nF_6.3V
B5 BLM15BD121SN1 +SPV18
C18 10uF_X6S C19 1uF_6.3V C20 100nF_6.3V
B6 BLM15BD121SN1 +SPV10
C21 1uF_6.3V C22 100nF_6.3V
B7 BLM15BD121SN1 +MPV18
C25 10uF_X6S C26 1uF_6.3V C27 100nF_6.3V
GENERICA R26 0R DNI CLK_100M_S
R28 0R CLK_100M
MR26 0R
TR19 0R CLK_27M
MR19 182R R19 182R R23 221R
XTALIN XTALOUT
C23 100nF R24 51.1R CLKTESTA
C28 100nF R25 51.1R CLKTESTB
U12 XTALOUT XTALIN 100M_OUT VDD_100M VDD_27M SS_SEL0 SS_SEL1 27M_OUT GND_100M GND_27M GND_PAD
IDT6V40088NBGI8 <New PN> TDFN10_3m0x3m0x0m8_p0m50_TH
U12_XOUT U12_XIN VDD33_100M VDD33_27M SS_SEL0 SS_SEL1
B2 B3 BLM15BD121SN1 <New PN> L0402
C9 100nF_6.3V C10 100nF_6.3V
MR20 MR21 R20 R21 5.1K
MR29 0R U12_XIN
R29 0R XIN_OSC
R36 1M
Y2 27.000MHz_10PPM D04-1101900-N38 XTAL_2P_HC49SM
C33 12pF_50V C11-1001012-W08 C0402
C34 12pF_50V C11-1001012-W08 C0402
MR30 0R R30 0R XOUT_OSC U12_XOUT

CLKREQ# requires open drain connection, and cannot be used as pinstrap

FOR 740: DNI R28/TR19 - XO_IN2/2 ARE GND on 740/730!

Divider for 1.8V signaling.

route 50ohms single-ended/100ohms diff and keep short

SCL / SDA BUS:

I2C Address	Function	Device
0x80 Write 0x81 Read	VDDC CONTROLLER	ST
0x70	VDDC CONTROLLER	UPI
0xA0, 0xA2 0xA4	MVDDQ, MVDDC, VDDCI VREF CONTROL	UP6266

DDC6 BUS:

I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO(13,12,11) - CONFIG[2..0]

CONFIG[2]
CONFIG[1]
CONFIG[0]

100 - 512Kbit M25P05A (ST)
101 - 1Mbit M25P10A (ST)
101 - 2Mbit M25P20 (ST)
101 - 4Mbit M25P40 (ST)
101 - 8Mbit M25P80 (ST)
100 - 512Kbit Pm25LV512 (Chingis)
101 - 1Mbit Pm25LV010 (Chingis)

VIP_DEVICE_STRAP_EN
0: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)
1:VIP host port devices present (use if Theater is populated)

RESERVED:

Internal use only. Other logic must not affect these signals during RESET.

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

Don't set GENERICC high at reset

MEMORY VENDOR SELECTION

[GPIO_5 : GPIO_16]
Hynix [0:1]
Samsung [1:0]

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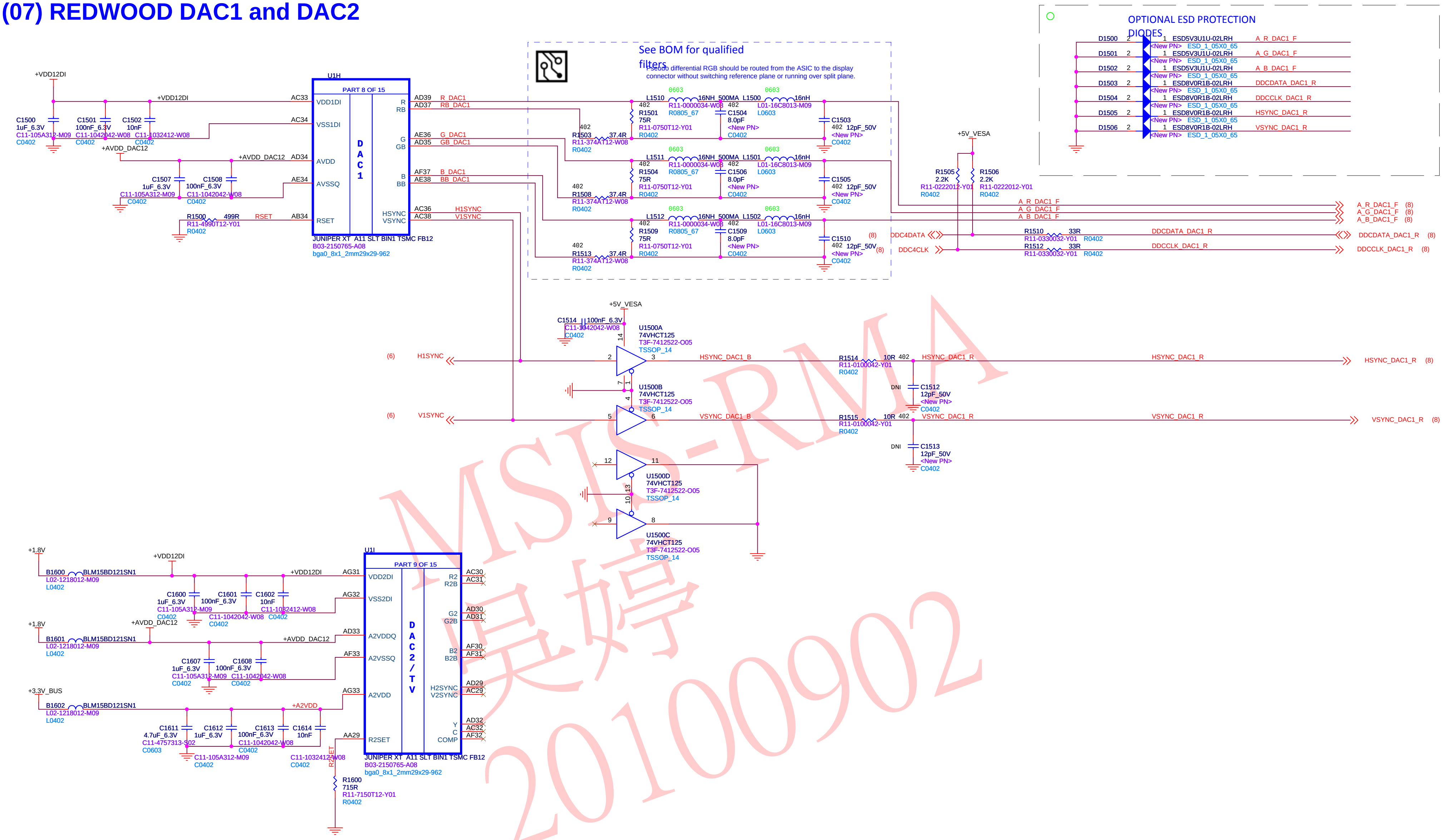
(07) REDWOOD DAC1 and DAC2


OPTIONAL ESD PROTECTION DIODES
D1500 ESD5V3U1U-02LRH A_R_DAC1_F
D1501 ESD5V3U1U-02LRH A_G_DAC1_F
D1502 ESD5V3U1U-02LRH A_B_DAC1_F
D1503 ESD8V0R1B-02LRH DDCDATA_DAC1_R
D1504 ESD8V0R1B-02LRH DDCCLK_DAC1_R
D1505 ESD8V0R1B-02LRH HSYNC_DAC1_R
D1506 ESD8V0R1B-02LRH VSYNC_DAC1_R
<New PN> ESD_1_05X0_65
See BOM for qualified filters
Route differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.
U1H
PART 8 OF 15
DAC1
VDD1DI
VSS1DI
AVDD
AVSSQ
RSET
R RB
G GB
B BB
HSYNC VSYNC
AC33 AC34 AD34 AE34 AB34
AD39 AD37 AE36 AD35 AF37 AE38 AC36 AC38
R_DAC1 RB_DAC1 G_DAC1 GB_DAC1 B_DAC1 BB_DAC1 H1SYNC V1SYNC
JUNIPER XT A11 SLT BIN1 TSMC FB12
B03-2150765-A08
bga0_8x1_2mm29x29-962
+VDD12DI
+AVDD_DAC12
C1500 1uF_6.3V C11-105A312-M09 C0402
C1501 100nF_6.3V C11-1042042-W08 C0402
C1502 10nF C11-1032412-W08 C0402
C1507 1uF_6.3V C11-105A312-M09 C0402
C1508 100nF_6.3V C11-1042042-W08 C0402
R1500 499R R11-4990T12-Y01 R0402 RSET
L1510 16NH_500MA R11-0000034-W08
L1500 16nH L01-16C8013-M09 L0603
L1511 16NH_500MA L1501 16nH
L1512 16NH_500MA L1502 16nH
0603
R1501 75R R11-0750T12-Y01 R0402
R1504 75R R11-0750T12-Y01 R0402
R1509 75R R11-0750T12-Y01 R0402
R0805_67
R1503 37.4R R11-374AT12-W08 R0402
R1508 37.4R R11-374AT12-W08 R0402
R1513 37.4R R11-374AT12-W08 R0402
C1504 8.0pF <New PN> C0402
C1506 8.0pF <New PN> C0402
C1509 8.0pF <New PN> C0402
C1503 12pF_50V <New PN> C0402
C1505 12pF_50V <New PN> C0402
C1510 12pF_50V <New PN> C0402
402
+5V_VESA
R1505 2.2K R11-0222012-Y01 R0402
R1506 2.2K R11-0222012-Y01 R0402
A_R_DAC1_F (8)
A_G_DAC1_F (8)
A_B_DAC1_F (8)
(8) DDC4DATA
(8) DDC4CLK
R1510 33R R11-0330032-Y01 R0402 DDCDATA_DAC1_R
R1512 33R R11-0330032-Y01 R0402 DDCCLK_DAC1_R
DDCDATA_DAC1_R (8)
DDCCLK_DAC1_R (8)
C1514 100nF_6.3V C11-1042042-W08 C0402
U1500A 74VHCT125 T3F-7412522-O05 TSSOP_14
U1500B 74VHCT125 T3F-7412522-O05 TSSOP_14
U1500C 74VHCT125 T3F-7412522-O05 TSSOP_14
U1500D 74VHCT125 T3F-7412522-O05 TSSOP_14
(6) H1SYNC
(6) V1SYNC
HSYNC_DAC1_B
VSYNC_DAC1_B
R1514 10R R11-0100042-Y01 R0402
R1515 10R R11-0100042-Y01 R0402
HSYNC_DAC1_R
VSYNC_DAC1_R
HSYNC_DAC1_R (8)
VSYNC_DAC1_R (8)
DNI C1512 12pF_50V <New PN> C0402
DNI C1513 12pF_50V <New PN> C0402
U1I
PART 9 OF 15
DAC2/TV
VDD2DI
VSS2DI
A2VDDQ
A2VSSQ
A2VDD
R2SET
R2 R2B
G2 G2B
B2 B2B
H2SYNC V2SYNC
Y C COMP
AG31 AG32 AD33 AF33 AG33 AA29
AC30 AC31 AD30 AD31 AF30 AF31 AD29 AC29 AD32 AC32 AF32
JUNIPER XT A11 SLT BIN1 TSMC FB12
B03-2150765-A08
bga0_8x1_2mm29x29-962
+1.8V
+3.3V_BUS
+VDD12DI
+AVDD_DAC12
+A2VDD
B1600 BLM15BD121SN1 L02-1218012-M09 L0402
B1601 BLM15BD121SN1 L02-1218012-M09 L0402
B1602 BLM15BD121SN1 L02-1218012-M09 L0402
C1600 1uF_6.3V C11-105A312-M09 C0402
C1601 100nF_6.3V C11-1042042-W08 C0402
C1602 10nF C11-1032412-W08 C0402
C1607 1uF_6.3V C11-105A312-M09 C0402
C1608 100nF_6.3V C11-1042042-W08 C0402
C1611 4.7uF_6.3V C11-4757313-S02 C0603
C1612 1uF_6.3V C11-105A312-M09 C0402
C1613 100nF_6.3V C11-1042042-W08 C0402
C1614 10nF C11-1032412-W08 C0402
R2SET
R1600 715R R11-7150T12-Y01 R0402

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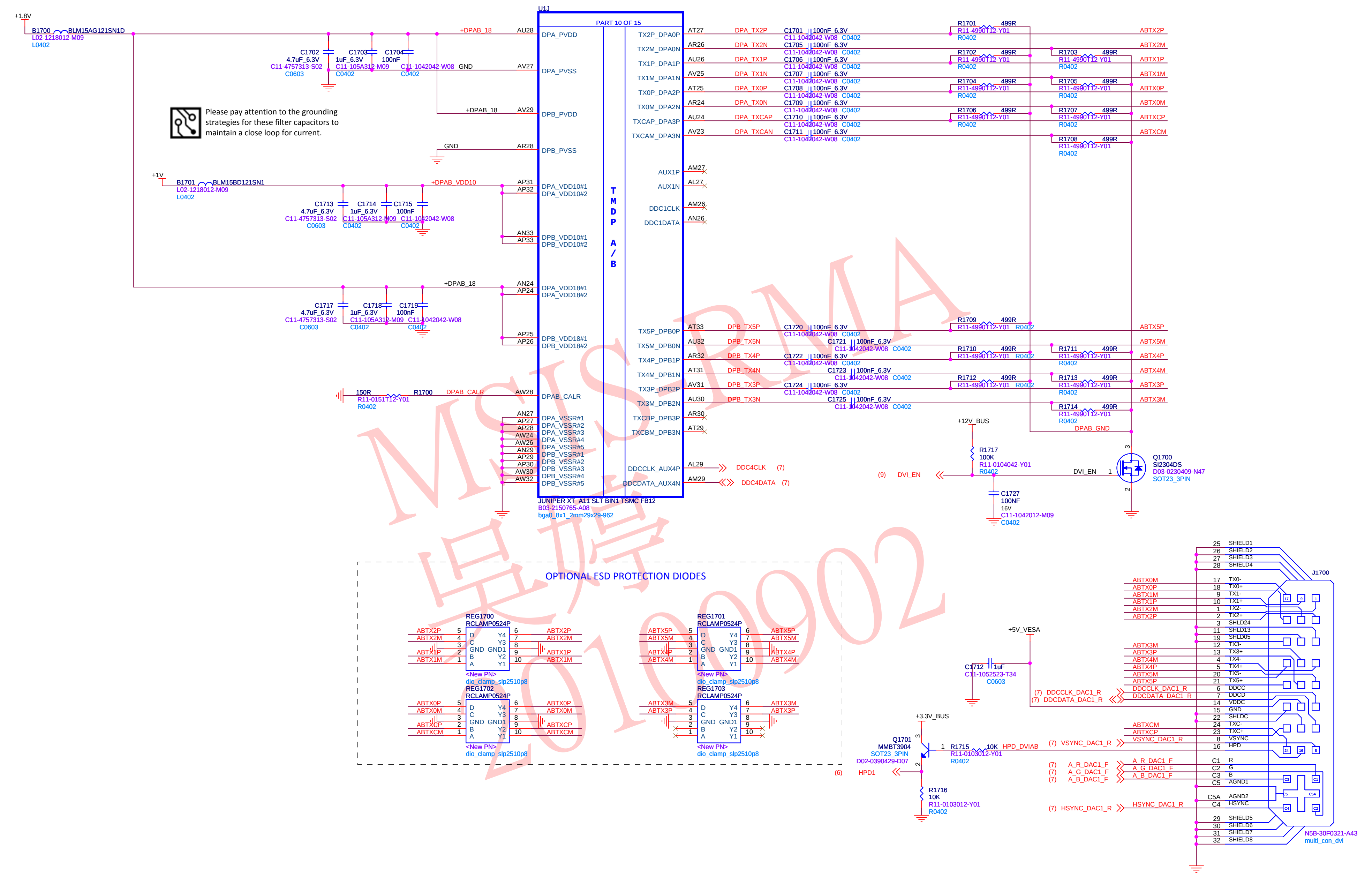
(08) REDWOOD TMDP A&B dDVI-I TOP



Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

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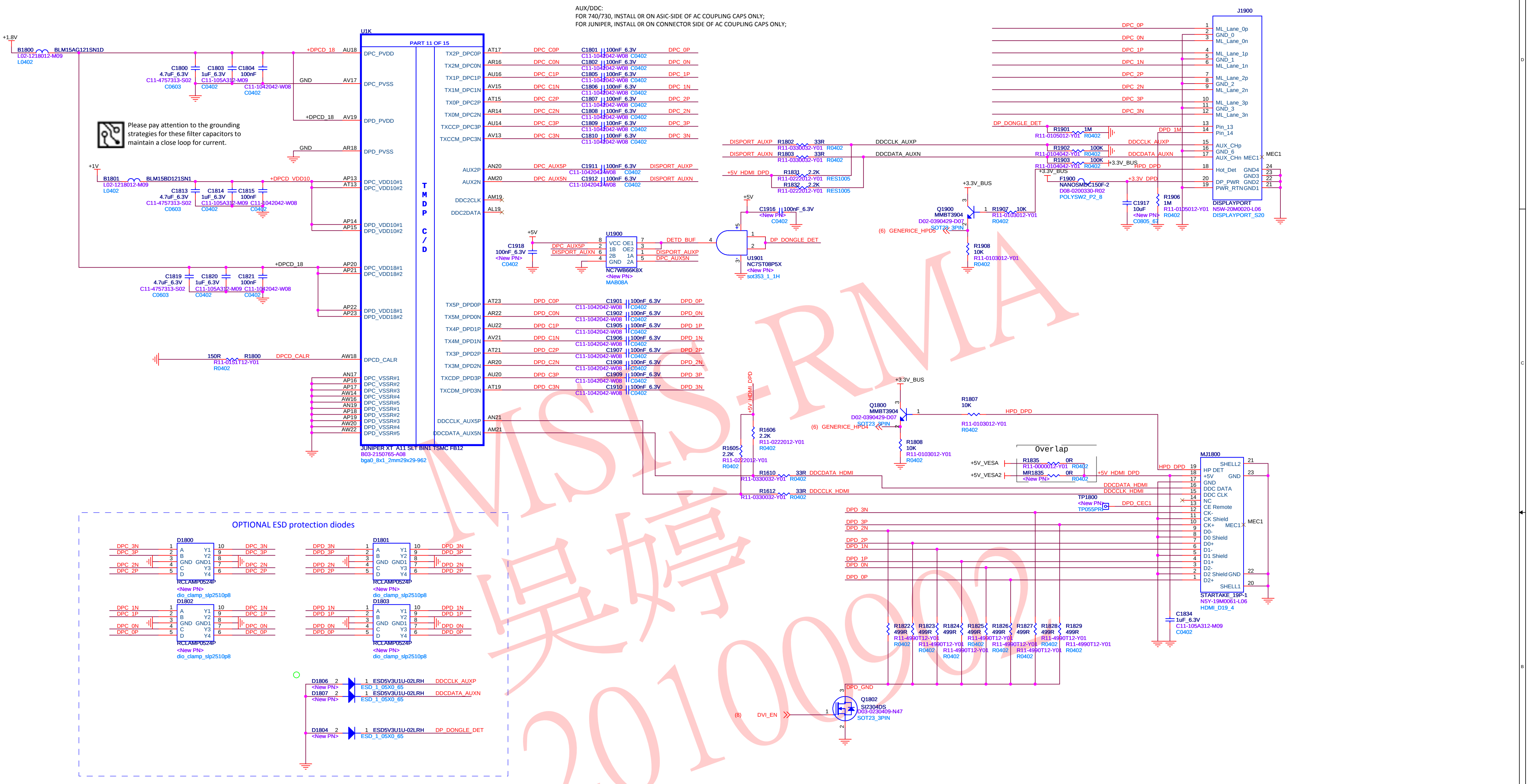
(09) REDWOOD Display Port C & Display Port/HDMI D

AUX/DDC:
FOR 740/730, INSTALL 0R ON ASIC-SIDE OF AC COUPLING CAPS ONLY;
FOR JUNIPER, INSTALL 0R ON CONNECTOR SIDE OF AC COUPLING CAPS ONLY;



Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

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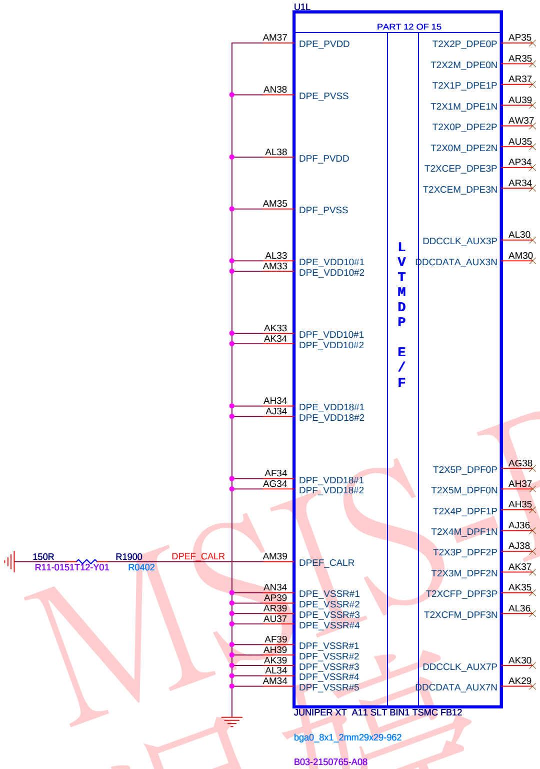
(10) REDWOOD LVTMDP E&F



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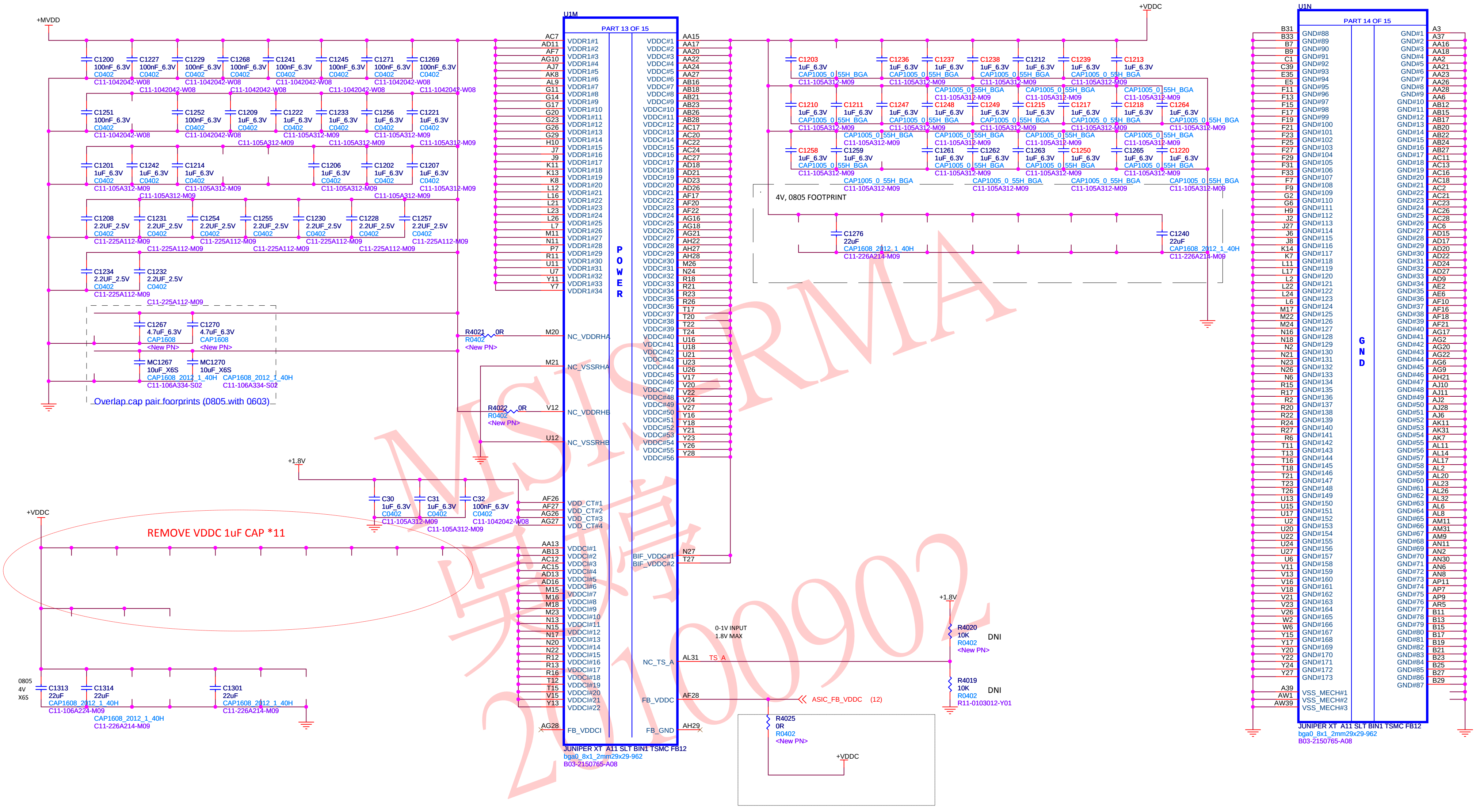
(11) REDWOOD Power & GND



+MVDD
C1200 100nF_6.3V C0402 C11-1042042-W08
C1227 100nF_6.3V C0402 C11-1042042-W08
C1229 100nF_6.3V C0402 C11-1042042-W08
C1268 100nF_6.3V C0402 C11-1042042-W08
C1241 100nF_6.3V C0402 C11-1042042-W08
C1245 100nF_6.3V C0402 C11-1042042-W08
C1271 100nF_6.3V C0402 C11-1042042-W08
C1269 100nF_6.3V C0402 C11-1042042-W08
C1251 100nF_6.3V C0402 C11-1042042-W08
C1252 100nF_6.3V C0402 C11-1042042-W08
C1209 1uF_6.3V C0402 C11-105A312-M09
C1222 1uF_6.3V C0402 C11-105A312-M09
C1233 1uF_6.3V C0402 C11-105A312-M09
C1256 1uF_6.3V C0402 C11-105A312-M09
C1221 1uF_6.3V C0402 C11-105A312-M09
C1201 1uF_6.3V C0402 C11-105A312-M09
C1242 1uF_6.3V C0402 C11-105A312-M09
C1214 1uF_6.3V C0402 C11-105A312-M09
C1206 1uF_6.3V C0402 C11-105A312-M09
C1202 1uF_6.3V C0402 C11-105A312-M09
C1207 1uF_6.3V C0402 C11-105A312-M09
C1208 2.2UF_2.5V C0402 C11-225A112-M09
C1231 2.2UF_2.5V C0402 C11-225A112-M09
C1254 2.2UF_2.5V C0402 C11-225A112-M09
C1255 2.2UF_2.5V C0402 C11-225A112-M09
C1230 2.2UF_2.5V C0402 C11-225A112-M09
C1228 2.2UF_2.5V C0402 C11-225A112-M09
C1257 2.2UF_2.5V C0402 C11-225A112-M09
C1234 2.2UF_2.5V C0402 C11-225A112-M09
C1232 2.2UF_2.5V C0402 C11-225A112-M09
C1267 4.7uF_6.3V CAP1608 <New PN>
C1270 4.7uF_6.3V CAP1608 <New PN>
MC1267 10uF_X6S CAP1608_2012_1_40H C11-106A334-S02
MC1270 10uF_X6S CAP1608_2012_1_40H C11-106A334-S02
Overlap cap pair footprints (0805 with 0603)
R4021 0R R0402 <New PN>
R4022 0R R0402 <New PN>
+1.8V
C30 1uF_6.3V C0402 C11-105A312-M09
C31 1uF_6.3V C0402 C11-105A312-M09
C32 100nF_6.3V C0402 C11-1042042-W08
+VDDC
REMOVE VDDC 1uF CAP *11
0805 4V X6S
C1313 22uF CAP1608_2012_1_40H C11-106A224-M09
C1314 22uF CAP1608_2012_1_40H C11-226A214-M09
C1301 22uF CAP1608_2012_1_40H C11-226A214-M09
U1M
PART 13 OF 15
POWER
VDDR1#1 … VDDR1#34
AC7 AD11 AF7 AG10 AJ7 AK8 AL9 G11 G14 G17 G20 G23 G26 G29 H10 J7 J9 K11 K13 K8 L12 L16 L21 L23 L26 L7 M11 N11 P7 R11 U11 U7 Y11 Y7
NC_VDDRHA M20
NC_VSSRHA M21
NC_VDDRHB V12
NC_VSSRHB U12
VDD_CT#1 … VDD_CT#4 AF26 AF27 AG26 AG27
VDDCI#1 … VDDCI#22
AA13 AB13 AC12 AC15 AD13 AD16 M15 M16 M18 M23 N13 N15 N17 N20 N22 R12 R13 R16 T12 T15 V15 Y13
VDDC#1 … VDDC#56
AA15 AA17 AA20 AA22 AA24 AA27 AB16 AB18 AB21 AB23 AB26 AB28 AC17 AC20 AC22 AC24 AC27 AD18 AD21 AD23 AD26 AF17 AF20 AF22 AG16 AG18 AG21 AH22 AH27 AH28 M26 N24 R18 R21 R23 R26 T17 T20 T22 T24 U16 U18 U21 U23 U26 V17 V20 V22 V24 V27 Y16 Y18 Y21 Y23 Y26 Y28
BIF_VDDC#1 N27
BIF_VDDC#2 T27
NC_TS_A AL31 TS_A
FB_VDDC AF28
FB_VDDCI AG28
FB_GND AH29
JUNIPER XT A11 SLT BIN1 TSMC FB12
bga0_8x1_2mm29x29-962
B03-2150765-A08
C1203 1uF_6.3V CAP1005_0_55H_BGA C11-105A312-M09
C1236 C1237 C1238 C1212 C1239 C1213
C1210 C1211 C1247 C1248 C1249 C1215 C1217 C1218 C1264
C1258 C1259 C1261 C1262 C1263 C1250 C1265 C1220
4V, 0805 FOOTPRINT
C1276 22uF CAP1608_2012_1_40H C11-226A214-M09
C1240 22uF CAP1608_2012_1_40H C11-226A214-M09
0-1V INPUT
1.8V MAX
R4020 10K R0402 <New PN> DNI
R4019 10K R0402 R11-0103012-Y01 DNI
ASIC_FB_VDDC (12)
R4025 0R R0402 <New PN>
+VDDC
U1N
PART 14 OF 15
GND
GND#1 … GND#173
VSS_MECH#1 VSS_MECH#2 VSS_MECH#3
A39 AW1 AW39
JUNIPER XT A11 SLT BIN1 TSMC FB12
bga0_8x1_2mm29x29-962
B03-2150765-A08

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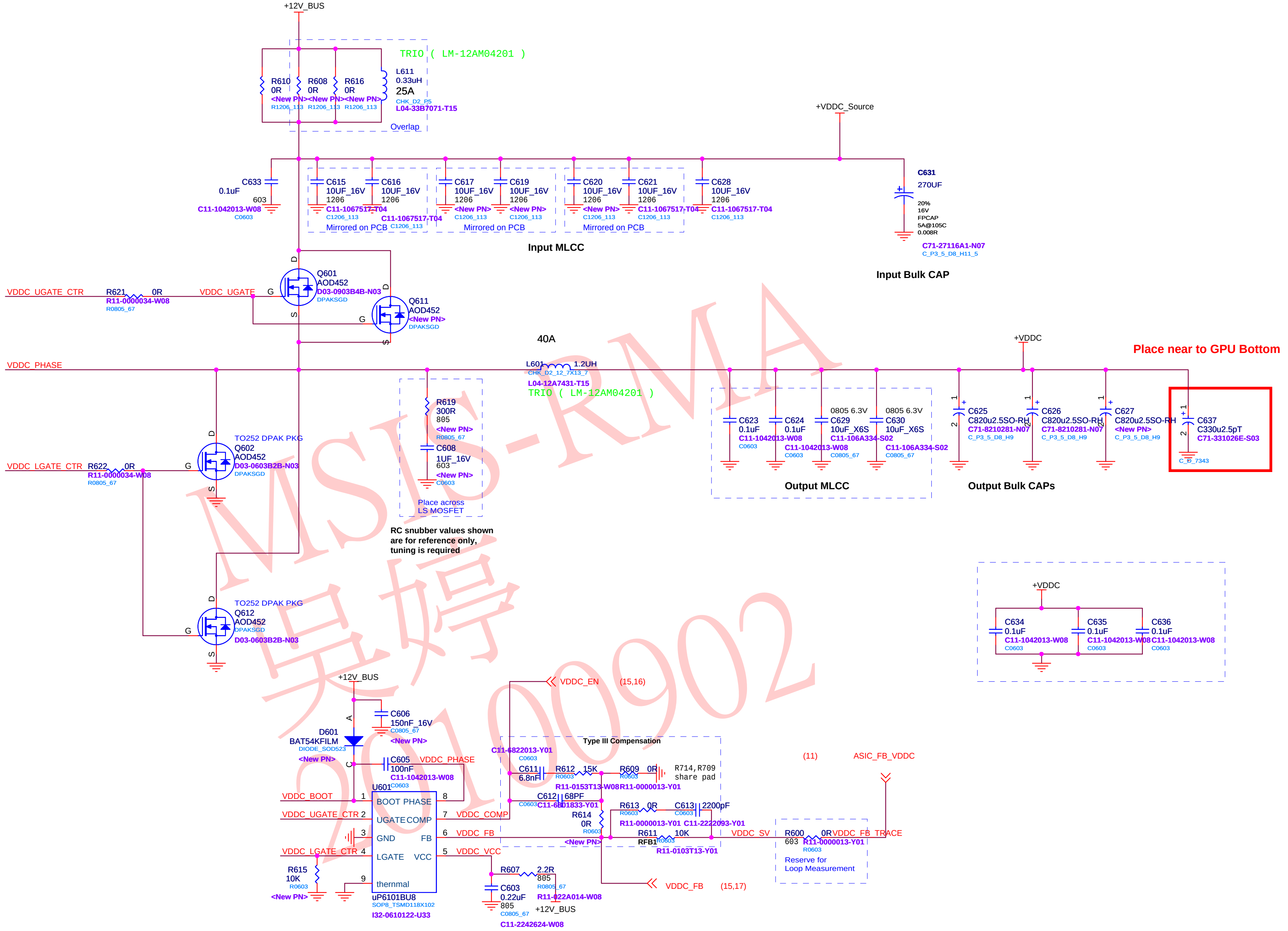

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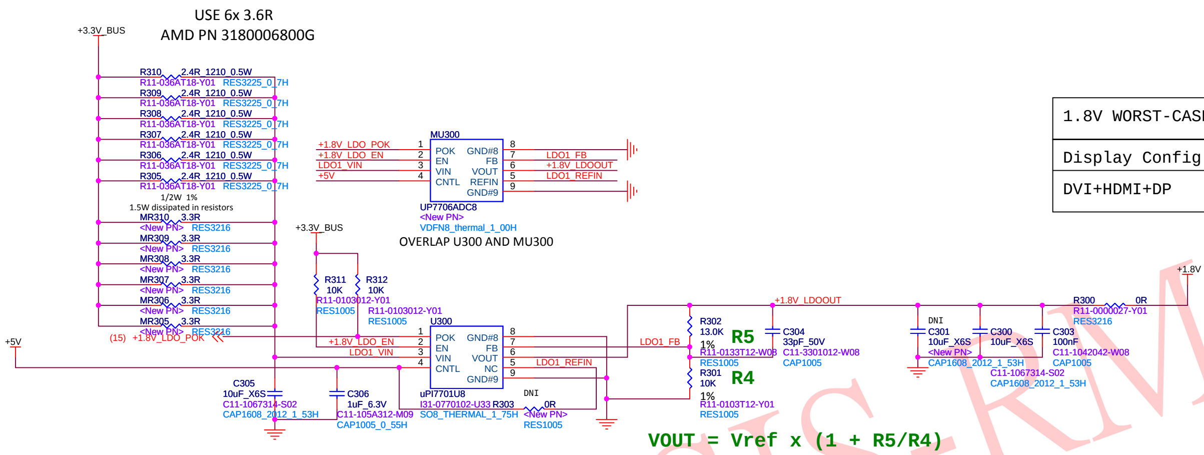
(15) Linear Regulators

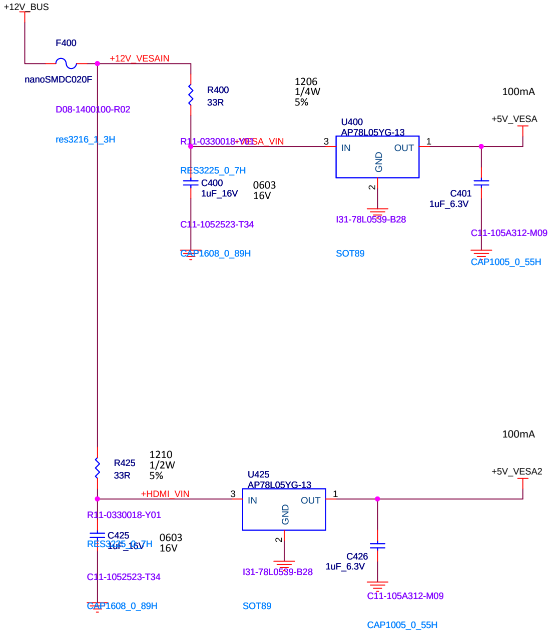
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

Regulators for +5V, +5V_VESA and +5V_HDMI


USE 6x 3.6R
AMD PN 3180006800G
+3.3V_BUS
R310 2.4R_1210_0.5W R11-036AT18-Y01 RES3225_0_7H
R309 2.4R_1210_0.5W R11-036AT18-Y01 RES3225_0_7H
R308 2.4R_1210_0.5W R11-036AT18-Y01 RES3225_0_7H
R307 2.4R_1210_0.5W R11-036AT18-Y01 RES3225_0_7H
R306 2.4R_1210_0.5W R11-036AT18-Y01 RES3225_0_7H
R305 2.4R_1210_0.5W R11-036AT18-Y01 RES3225_0_7H
1/2W 1%
1.5W dissipated in resistors
MR310 3.3R <New PN> RES3216
MR309 3.3R <New PN> RES3216
MR308 3.3R <New PN> RES3216
MR307 3.3R <New PN> RES3216
MR306 3.3R <New PN> RES3216
MR305 3.3R <New PN> RES3216
MU300
+1.8V_LDO_POK
+1.8V_LDO_EN
LDO1_VIN
+5V
POK EN VIN CNTL GND#8 FB VOUT REFIN GND#9
LDO1_FB
+1.8V_LDOOUT
LDO1_REFIN
UP7706ADC8
<New PN>
VDFN8_thermal_1_00H
OVERLAP U300 AND MU300
+3.3V_BUS
R311 10K R11-0103012-Y01 RES1005
R312 10K R11-0103012-Y01 RES1005
U300
POK EN VIN CNTL GND#8 FB VOUT NC GND#9
+5V
(15) +1.8V_LDO_POK
+1.8V_LDO_EN
LDO1_VIN
LDO1_FB
LDO1_REFIN
C305 10uF_X6S C11-1067314-S02 CAP1608_2012_1_53H
C306 1uF_6.3V C11-105A312-M09 CAP1005_0_55H
uPI7701U8 I31-0770102-U33 SO8_THERMAL_1_75H
R303 DNI 0R <New PN> RES1005
R302 13.0K 1% R11-0133T12-W08 RES1005
R5
R301 10K 1% R11-0103T12-Y01 RES1005
R4
C304 33pF_50V C11-3301012-W08 CAP1005
+1.8V_LDOOUT
DNI C301 10uF_X6S <New PN> CAP1608_2012_1_53H
C300 10uF_X6S C11-1067314-S02 CAP1608_2012_1_53H
C303 100nF C11-1042042-W08 CAP1005
R300 0R R11-0000027-Y01 RES3216
+1.8V
VOUT = Vref x (1 + R5/R4)

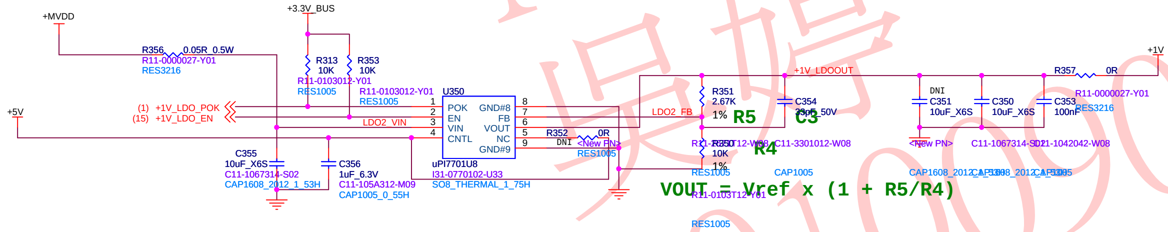
1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

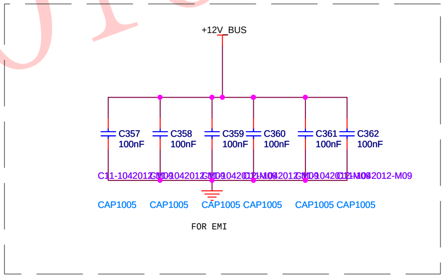


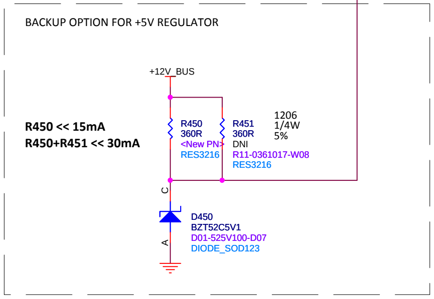
LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA


+MVDD
R356 0.05R_0.5W R11-0000027-Y01 RES3216
+3.3V_BUS
R313 10K R11-0103012-Y01 RES1005
R353 10K R11-0103012-Y01 RES1005
+5V
(1) +1V_LDO_POK
(15) +1V_LDO_EN
LDO2_VIN
U350
POK EN VIN CNTL GND#8 FB VOUT NC GND#9
C355 10uF_X6S C11-1067314-S02 CAP1608_2012_1_53H
C356 1uF_6.3V C11-105A312-M09 CAP1005_0_55H
uPI7701U8 I31-0770102-U33 SO8_THERMAL_1_75H
R352 DNI 0R <New PN> RES1005
LDO2_FB
R351 2.67K 1% R11-2670T12-W08
R5
R350 10K 1% R11-0103T12-Y01 RES1005
R4
C354 33pF_50V C11-3301012-W08 CAP1005
C3
+1V_LDOOUT
DNI C351 10uF_X6S <New PN> CAP1608_2012_1_53H
C350 10uF_X6S C11-1067314-S02 CAP1608_2012_1_53H
C353 100nF C11-1042042-W08 CAP1005
R357 0R R11-0000027-Y01 RES3216
+1V
VOUT = Vref x (1 + R5/R4)




BACKUP OPTION FOR +5V REGULATOR
R450 << 15mA
R450+R451 << 30mA
+12V_BUS
R450 360R <New PN> RES3216
R451 360R DNI R11-0361017-W08 RES3216
1206 1/4W 5%
+5V
C
A
D450 BZT52C5V1 D01-525V100-D07 DIODE_SOD123

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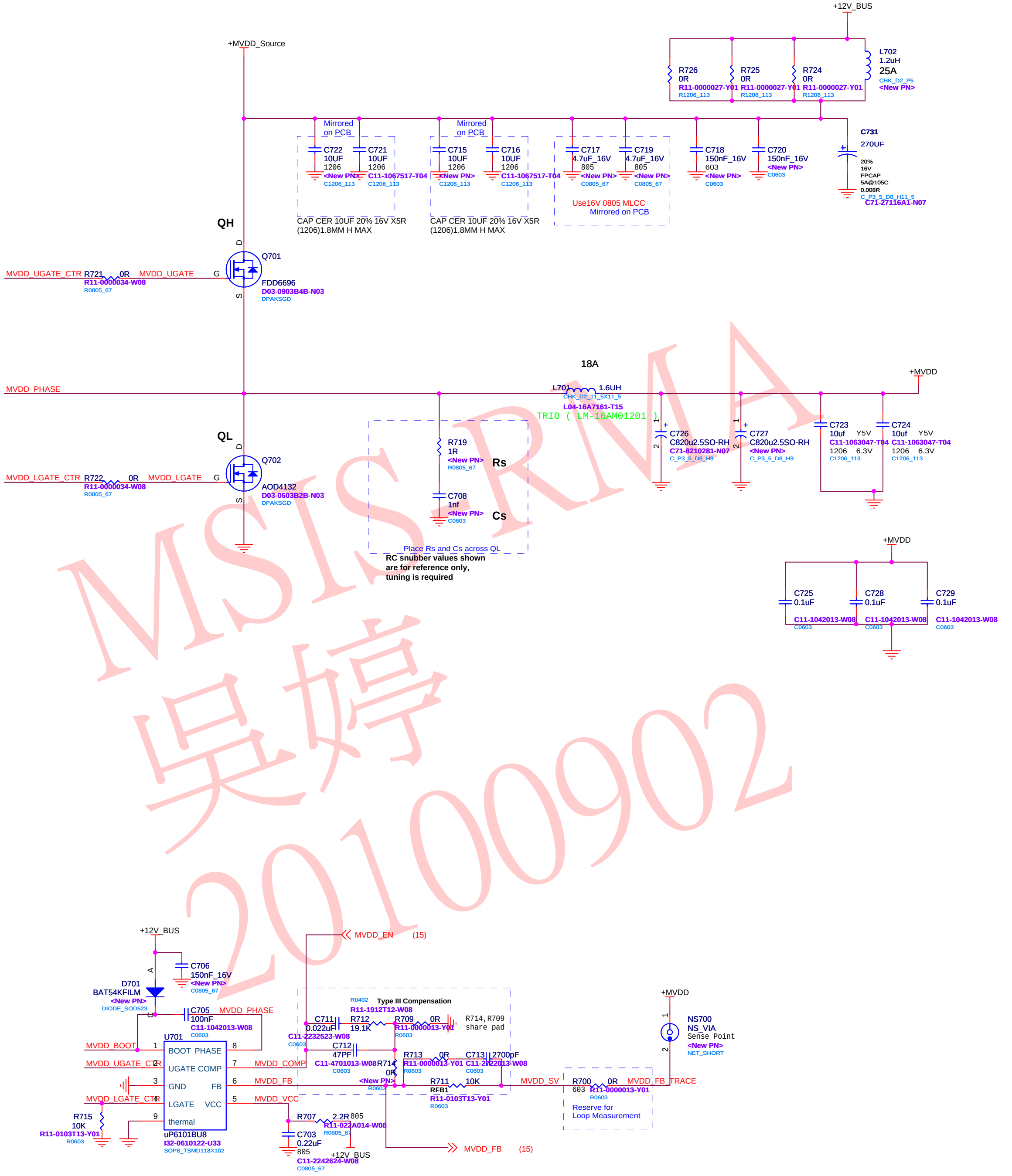

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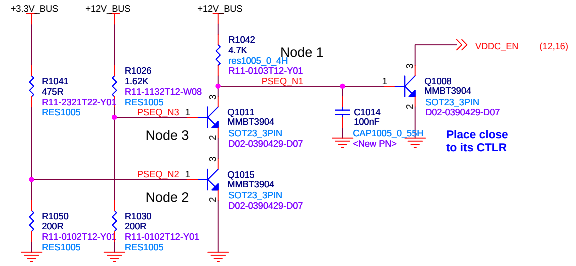
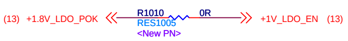
(16) Power Management - Power Gating and Dynamic Voltage Control

12V_BUS & 3V3_BUS POWER SEQUENCING

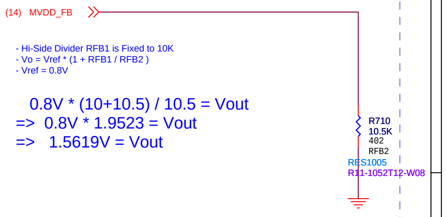


Place close to its CTLR

Install R1010 to gate 1V LDO with 1.8V LDO.



MVDD Low Side Divider

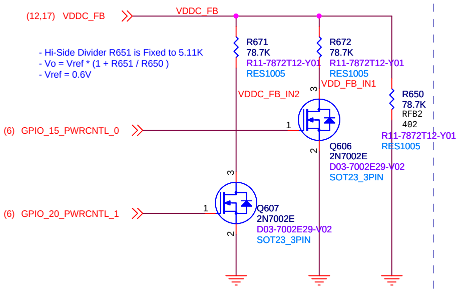


- Hi-Side Divider RFB1 is Fixed to 10K
- Vo = Vref * (1 + RFB1 / RFB2)
- Vref = 0.8V

0.8V * (10+10.5) / 10.5 = Vout
=> 0.8V * 1.9523 = Vout
=> 1.5619V = Vout

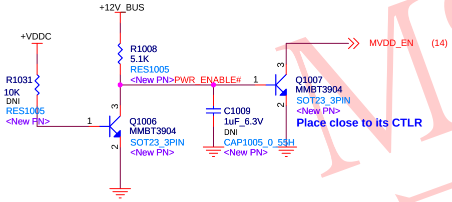
VDDC Low Side Divider

R650 must be pouplated only if VID is not used and
VDDC VREFIN is pulled high to >4.5V.
Then this will set VDDC to a fixed value.



- Hi-Side Divider R651 is Fixed to 5.11K
- Vo = Vref * (1 + R651 / R650)
- Vref = 0.6V

POWER SEQUENCING CIRCUIT



Place close to its CTLR

	Rtop = 10k	Rtop = 1k
00	0.8V * (10+78.7) / 78.7 = Vout => 0.8V * 1.127 = Vout => 0.90165V = Vout	0.8V * (1+7.87) / 7.87 = Vout => 0.8V * 1.127 = Vout => 0.90165V = Vout
01 / 10	0.8V * (10+39.35) / 39.35 = Vout => 0.8V * 1.254 = Vout => 1.0033 = Vout	0.8V * (1+3.935) / 39.35 = Vout => 0.8V * 1.254 = Vout => 1.0033 = Vout
11	0.8V * (10+26.23) / 26.23 = Vout => 0.8V * 1.3811 = Vout => 1.104955= Vout	0.8V * (1+2.623) / 26.23 = Vout => 0.8V * 1.3811 = Vout => 1.104955= Vout

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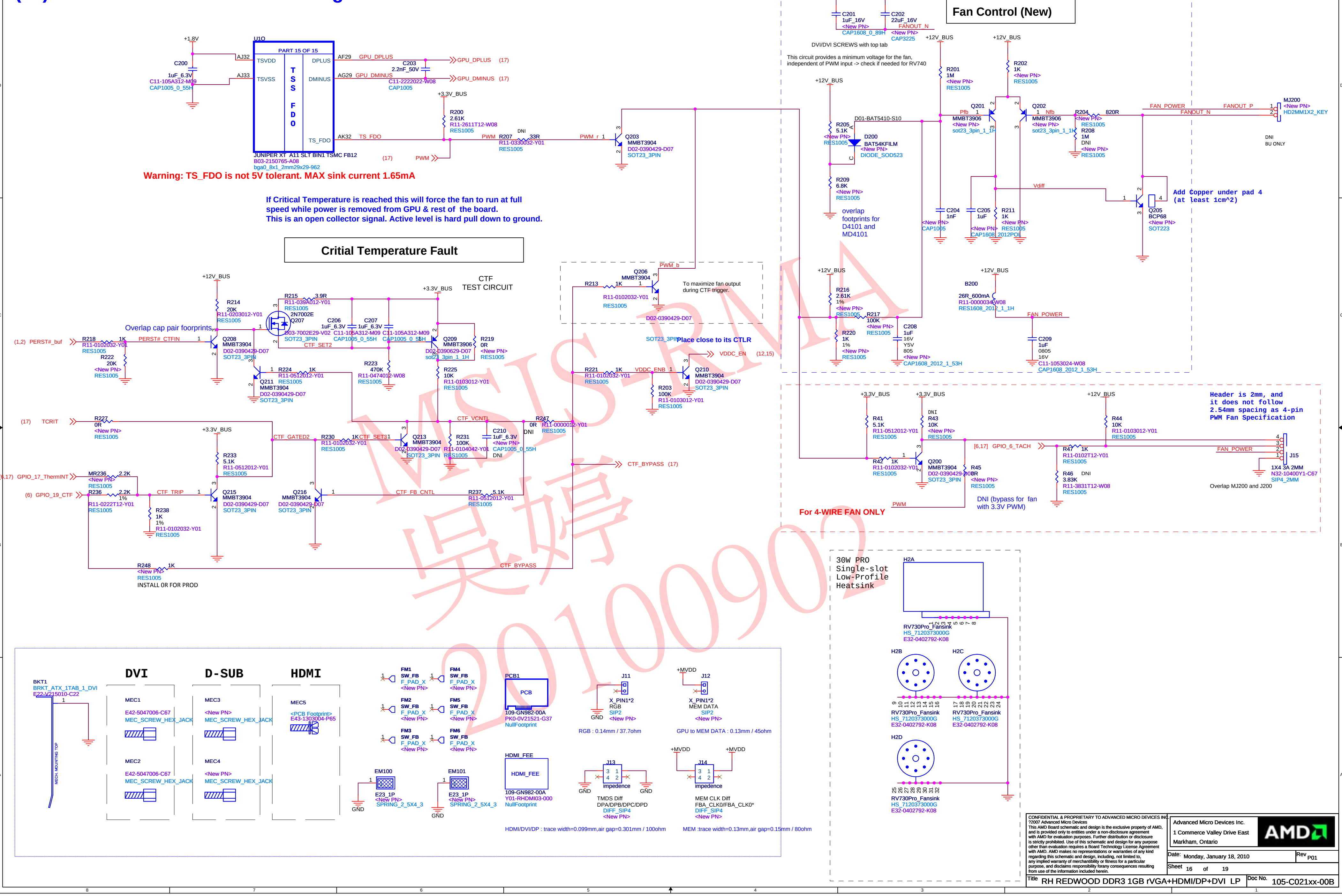
(19) Mechanical and Thermal Management



Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.

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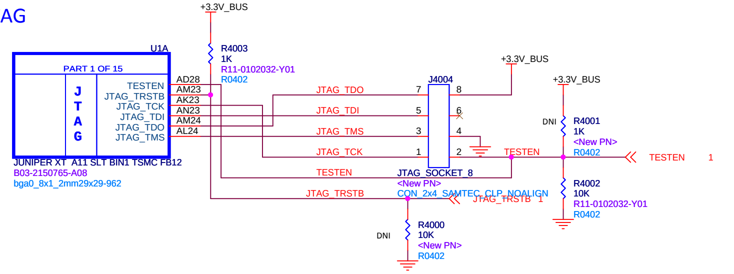
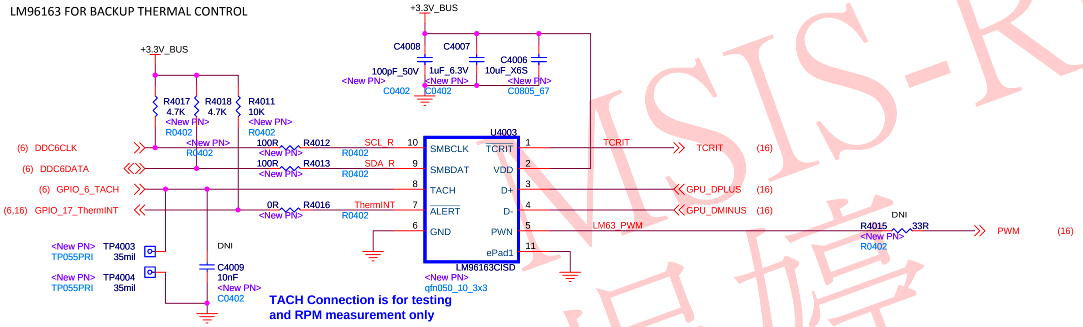
(19) Debug Circuits

JTAG

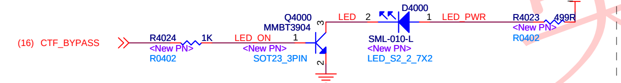


LM96163 FOR BACKUP THERMAL CONTROL

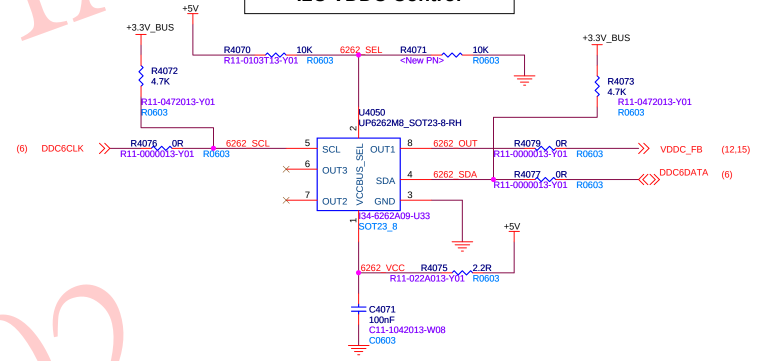


TACH Connection is for testing and RPM measurement only

LED RED "ON" shows Fault

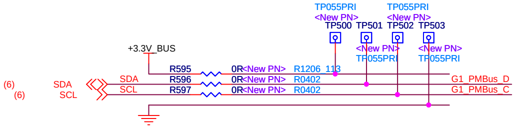


I2C VDDC Control



SCL/SDA PORT DEBUG ACCESS

Place testpoints together on the back side
(easily accessible and not blocked by the heatsink).



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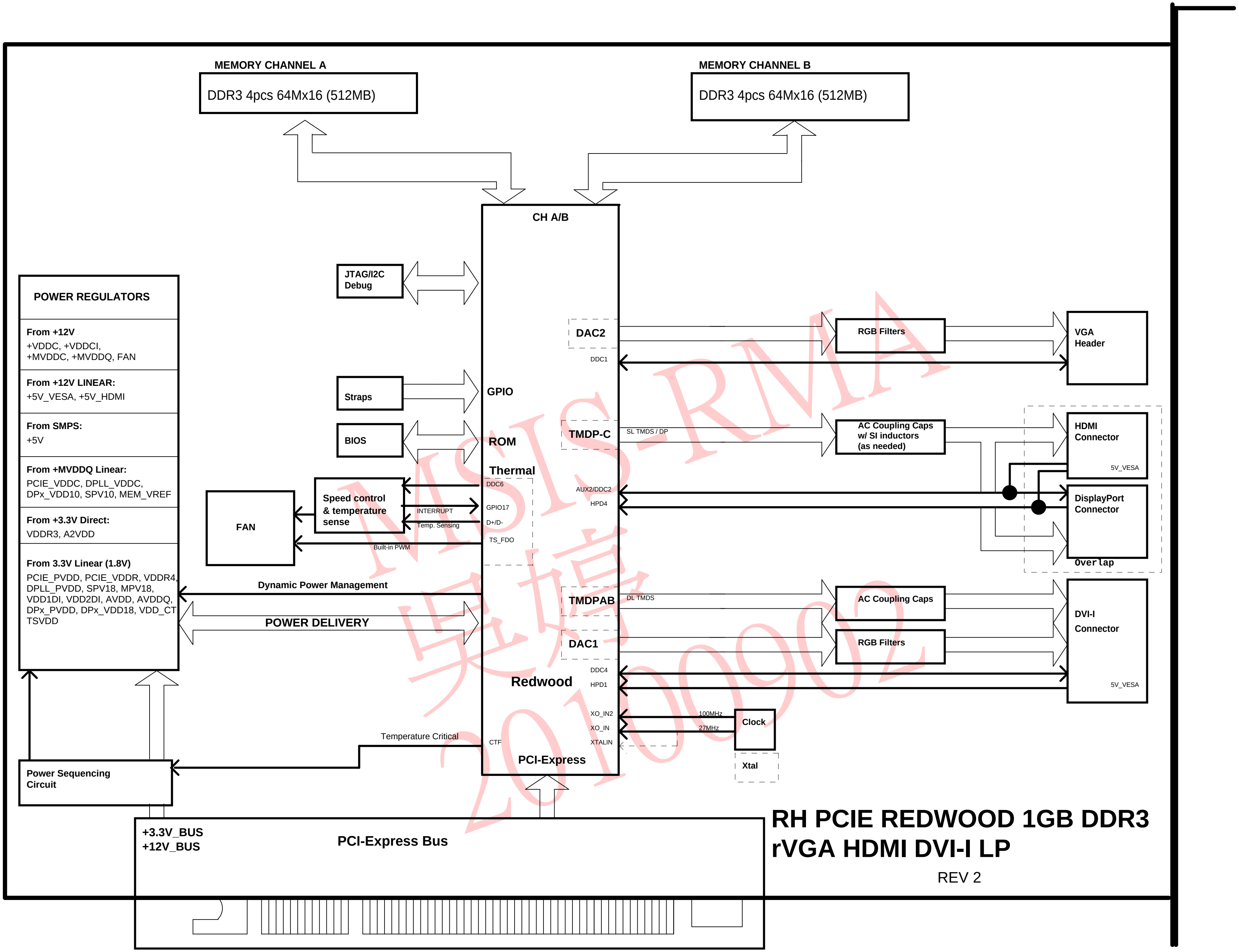

RH PCIE REDWOOD 1GB DDR3 rVGA HDMI DVI-I LP

REV 2

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Canada, L3T 7X6
(905) 882-2600

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Title

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Schematic No.

105-C024xx-00B

Date:

Friday, January 15, 2010

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev P01

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/06/11	REDWOOD PRO DDR3 1GB BASED ON C020
	00B	2009/07/17	REDWOOD PRO DDR3 1GB BASED ON C021 00A
			......