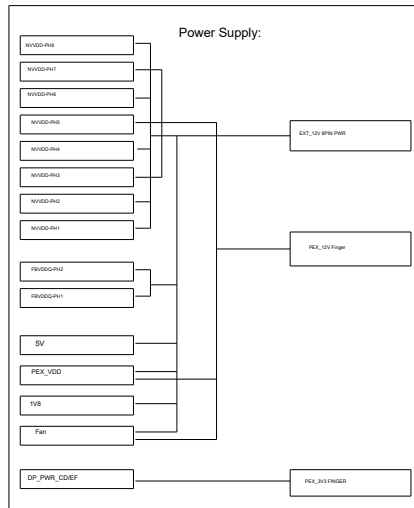
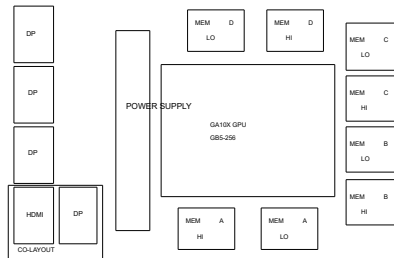
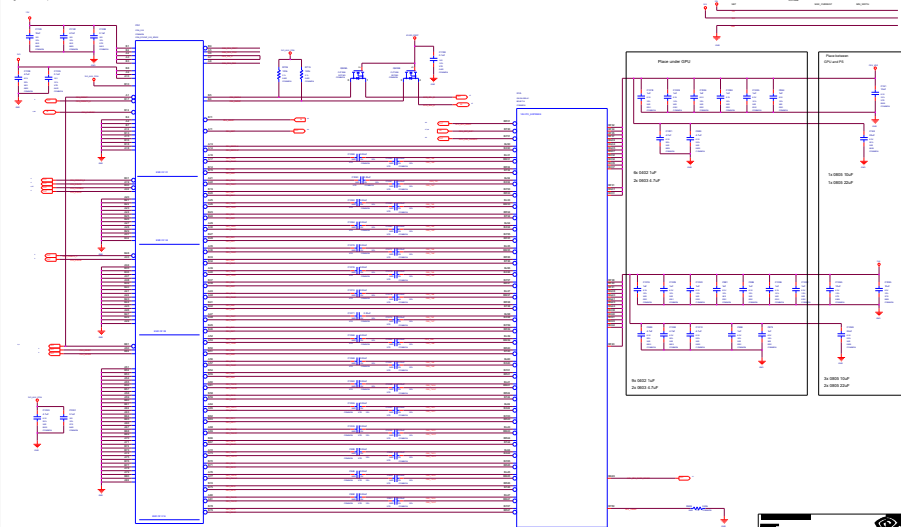


GA104/GA106 GB5256
DP + DP + DP + HDMI/DP

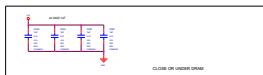
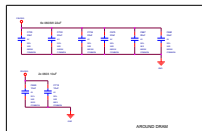
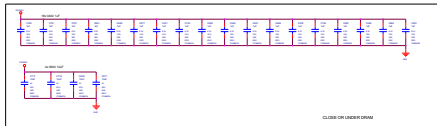
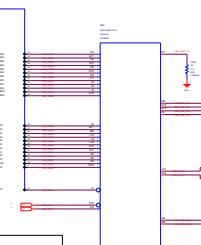
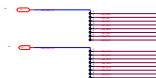
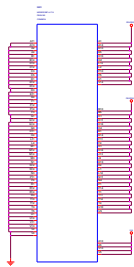
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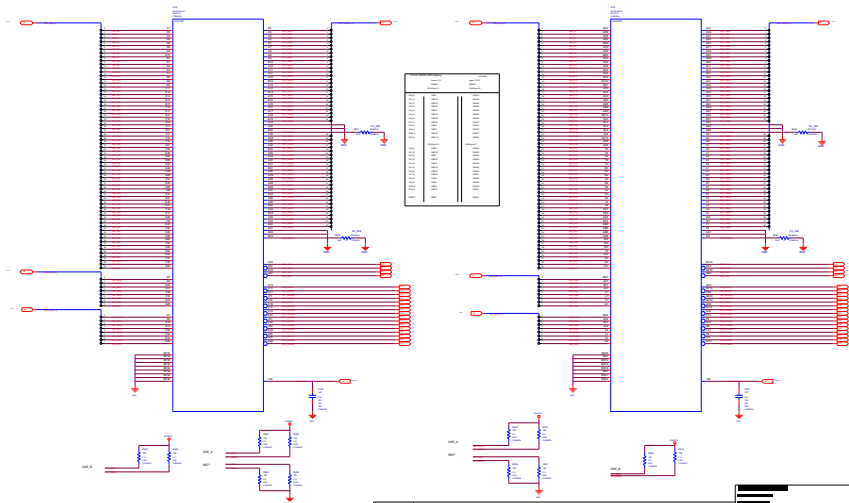
Page	Description	Page	Description
1	Table of Contents	26	MISC: ROM, XTAL, STRAPS
2	BLOCK DIAGRAM	27	MISC2: JTAG, GPIO, ADC, I2C, OVERT
3	PCI Express	28	Blank
4	PCIs GEN4 RC Termination	29	PS: 1V8
5	MEMORY: GPU Partition A/B	30	PS: 5V
6	MEMORY: FBA Partition 32.0	31	PS: PEKIDD
7	MEMORY: FBA Partition 63.32	32	PS: FBVDDQ
8	MEMORY: FBB Partition 31.0	33	PS: FBVDDQ PH2
9	MEMORY: FBB Partition 63.32	34	PS: NVVDD CNTL
10	MEMORY: GPU Partition C/D	35	PS: NVVDD PHASE 1 & 2
11	MEMORY: FBC Partition 31.0	36	PS: NVVDD PHASE 3 & 5
12	MEMORY: FBC Partition 63.32	37	PS: NVVDD PHASE 4
13	MEMORY: FBD Partition 31.0	38	PS: NVVDD PHASE 6 & 8
14	MEMORY: FBD Partition 63.32	39	PS: NVVDD PHASE 7
15	GPU PWR and GND	40	Blank
16	GPU PWR and GND 2	41	INPUT SWITCH RTD3
17	GPU XVID	42	INPUT POWER, FILTERING
18	GPU DECOUPLING FBVDDQ	43	MISC: Hot Unplug
19	GPU DECOUPLING NVVDD	44	SEQ: 3V3_SEQ, DDC_5V/DP_AUX_PROT
20	GPU DECOUPLING NVVDD 2	45	SEQ: NAVDD, PEKIDD AND FBVDDQ ENABLE
21	IFPA8 DVI-D-OL	46	SEQ: MISC
22	IFPE DP	47	SEQUENCE: VOLTAGE MONITOR
23	IFPE DP	48	FAN & LED
24	IFPD DP	49	OVRRM POWER SENSE
25	IFPC HDMI/DP	50	MISC

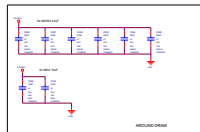
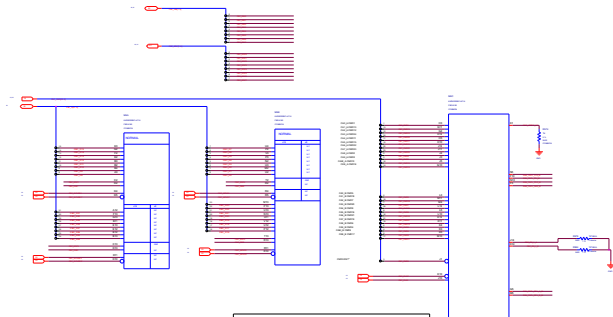
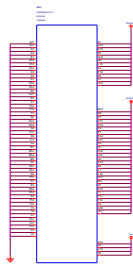




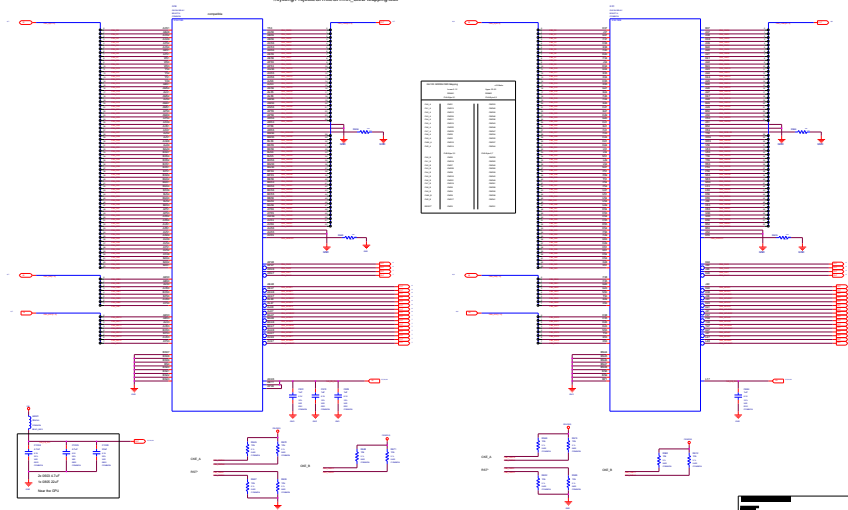


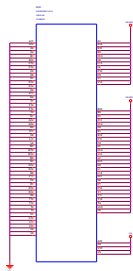




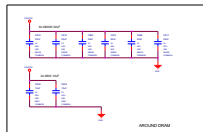
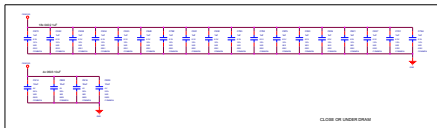
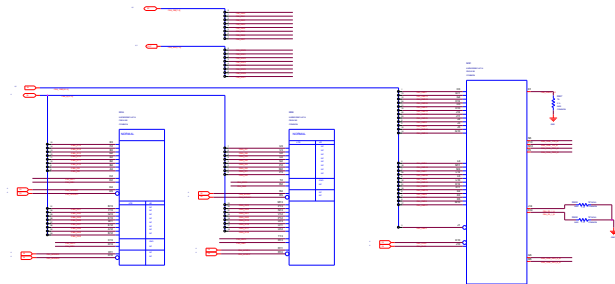


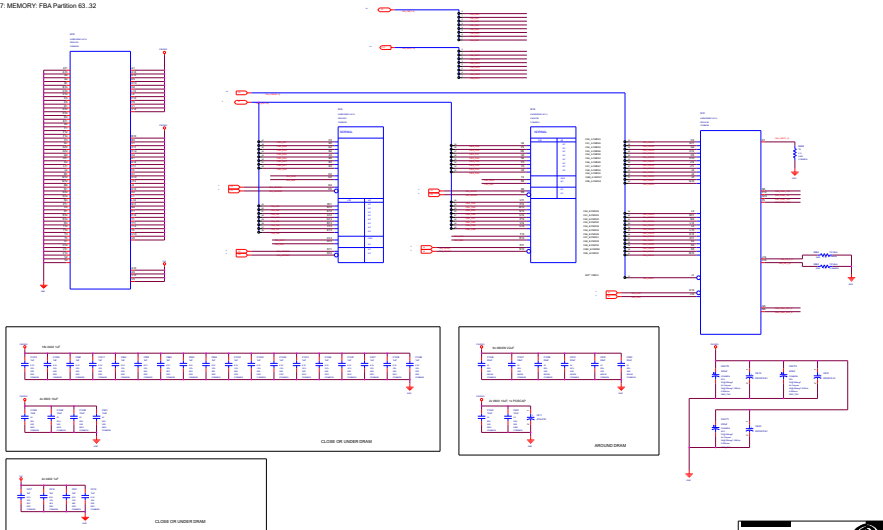
/kyesang/Projects/GA/xx/GA00X_CMD-Mapping.xlsx

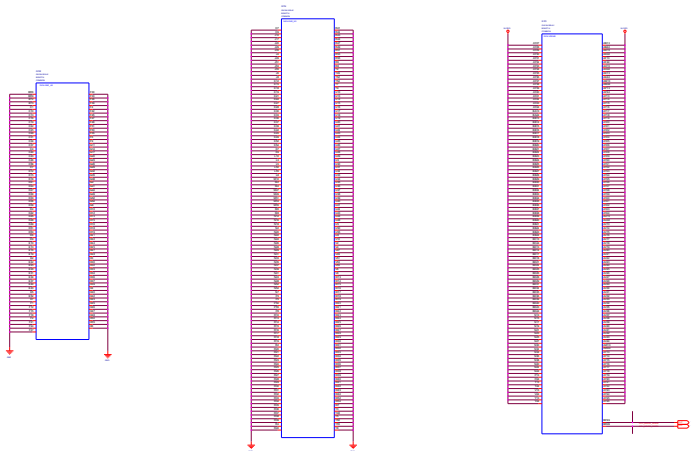




Storage class: at least 2-year class and 10-year class for each cap.

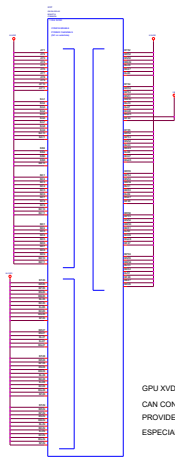






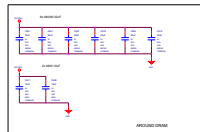
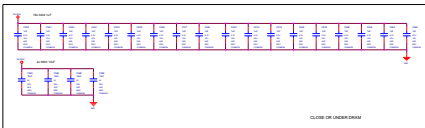
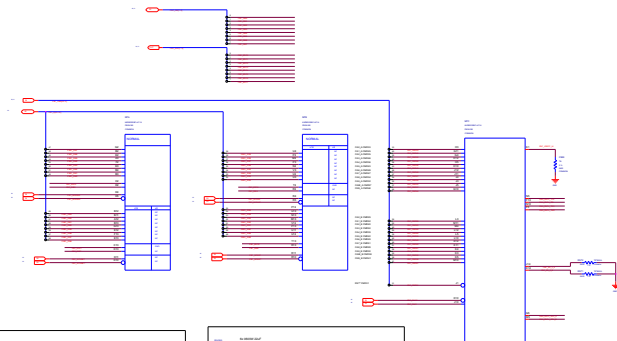
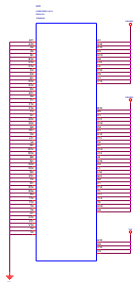
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DESIGNER	WANG, JIN
CHECKER	WANG, JIN

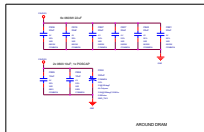
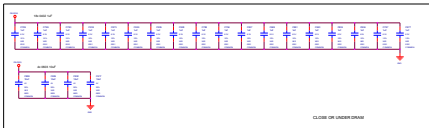
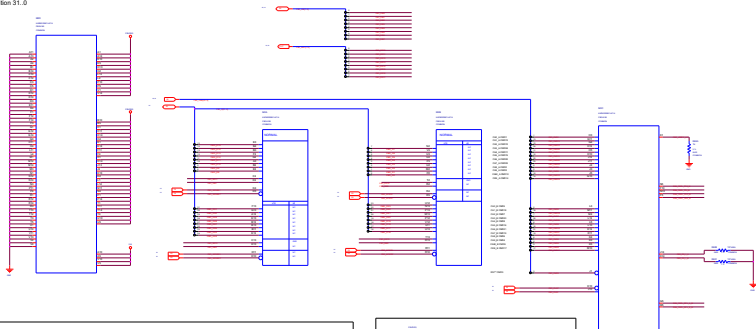
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DATE	2023-08-01
DESIGNER	WANG, JIN
CHECKER	WANG, JIN

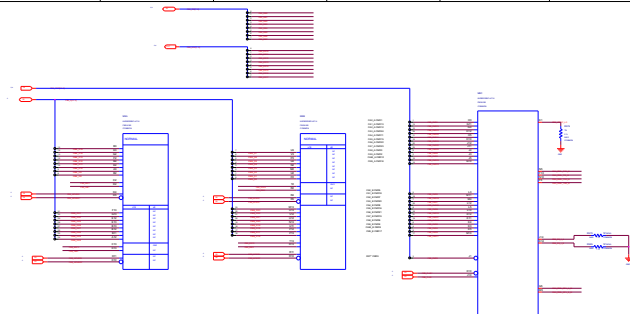


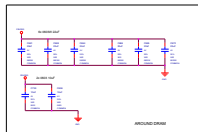
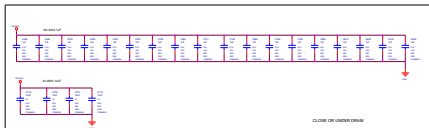
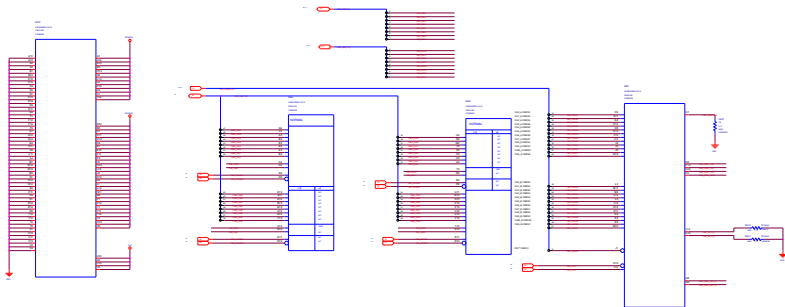
GPU XVDD BALLS (NC IN SUBSTRATE):

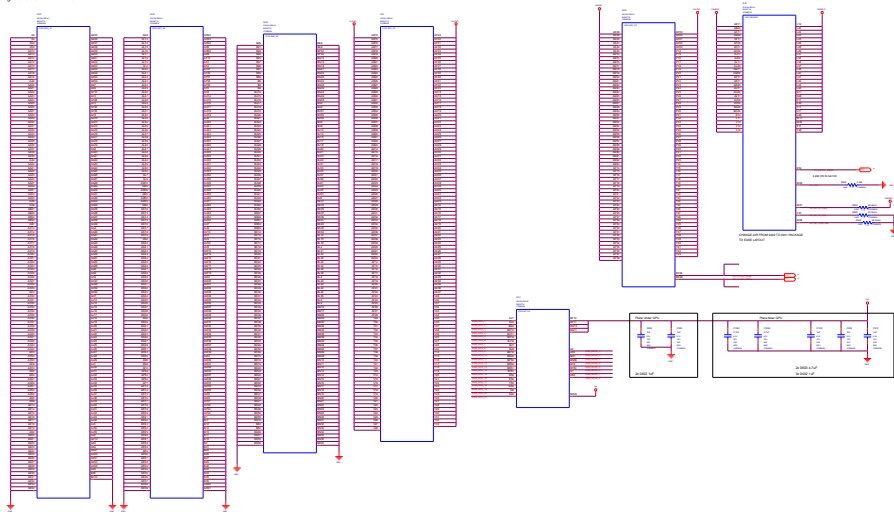
CAN CONNECT TO ANY POWER NET (NV/MS/1V8/PEX, etc.) ON SYSTEM BOARD,
 PROVIDE FLEXIBILITY TO OPTIMIZE POWER CHANNELS ON SYSTEM BOARD,
 ESPECIALLY USEFUL FOR LOW-COST DESIGN WITH REDUCED PCB LAYERS.

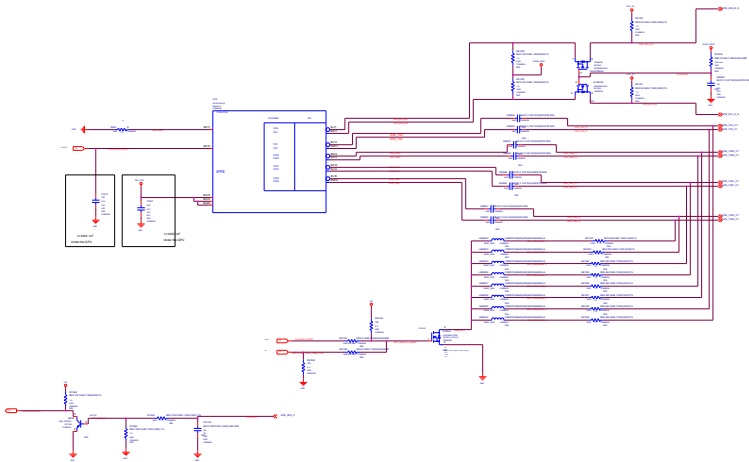


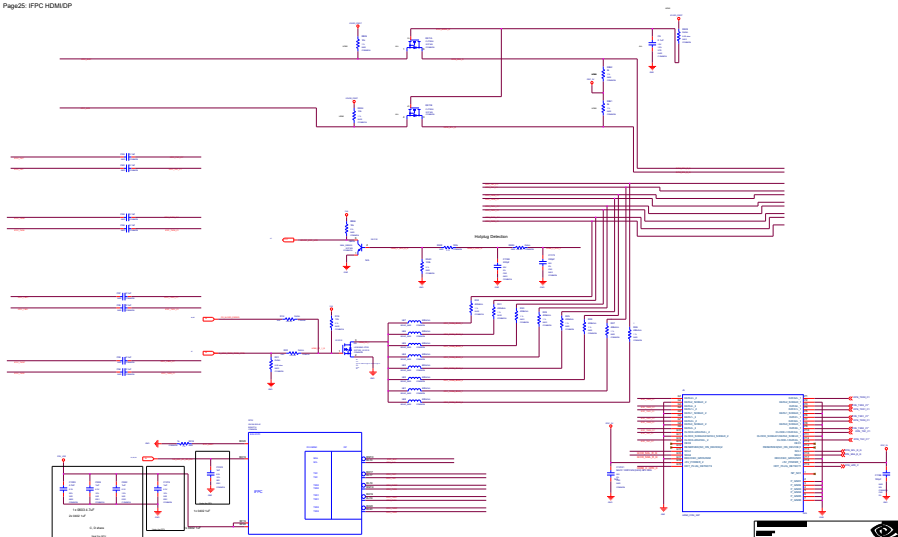


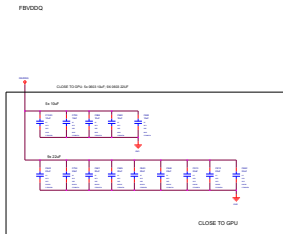
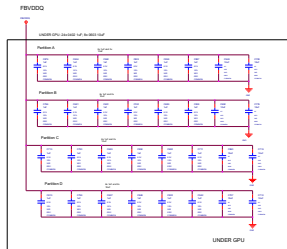


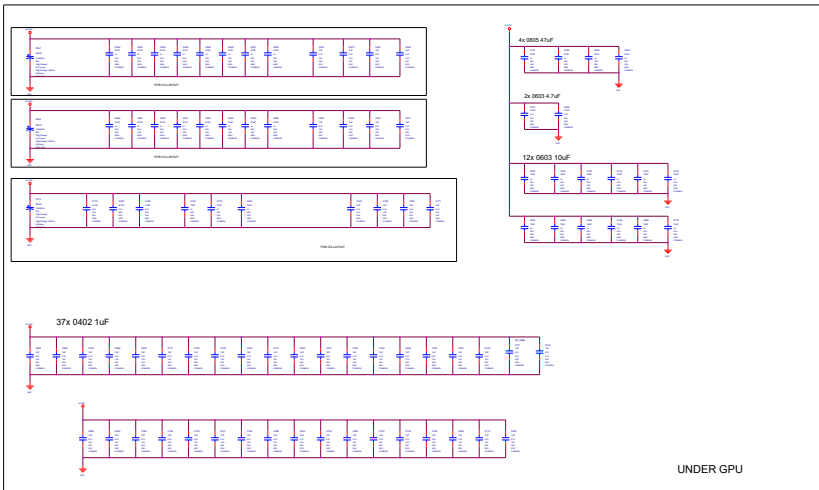


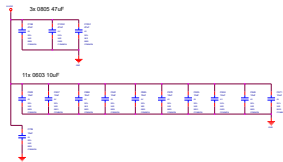
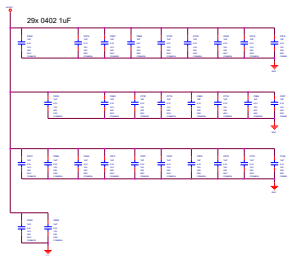
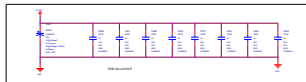




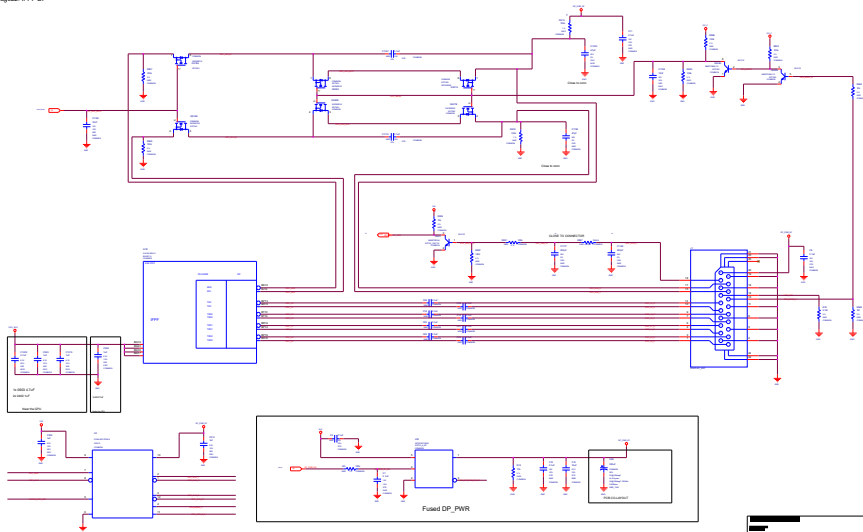




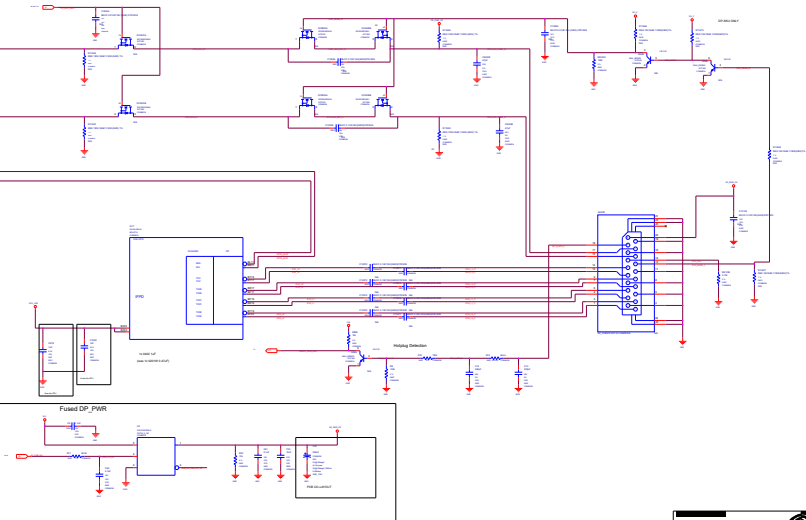


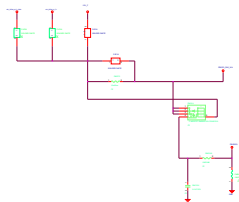
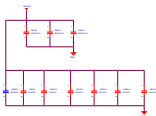
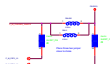
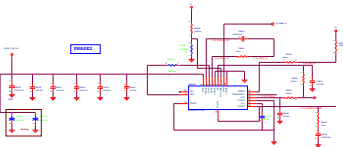
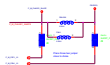
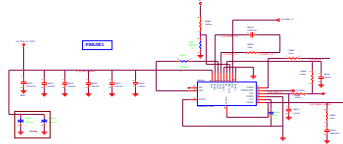


UNDER GPU



Rev	1
Date	2010-01-01
Author	...





Barcode/ID #	DENSITY	WIDTH	VENDOR	USE
00000	800	200.00	Barcoding	A
00007	800	200.00	Mediscan	A
00010	800	200.00	Regina	10
00011	800	200.00	Barcoding	C
00010	800	200.00	Mediscan	A
00010	800	200.00	Regina	10
00010	1000	200.00	Barcoding	10
00010				

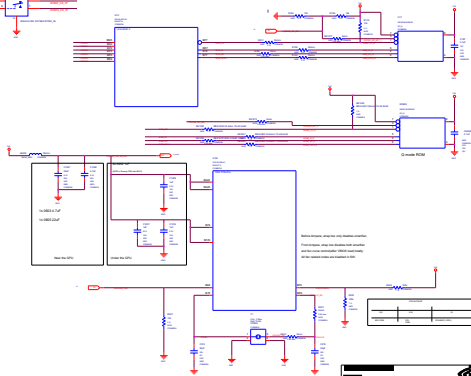
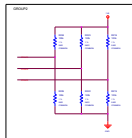
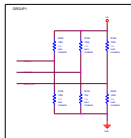
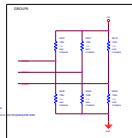
ROM_ID	ROM_ID	ROM_ID	BOOTING/NO_BOOT	ENABLE/DISABLE
H	H	H	BOOT	FE_OVERWRITE_ENABLE
L	L	L	NO_BOOT	FE_OVERWRITE_DISABLE

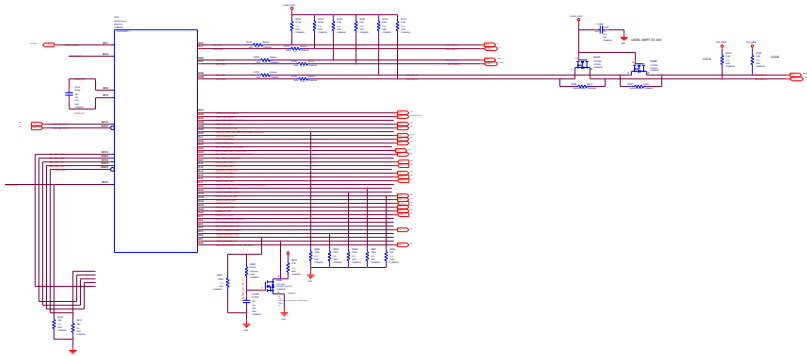
[illegible]

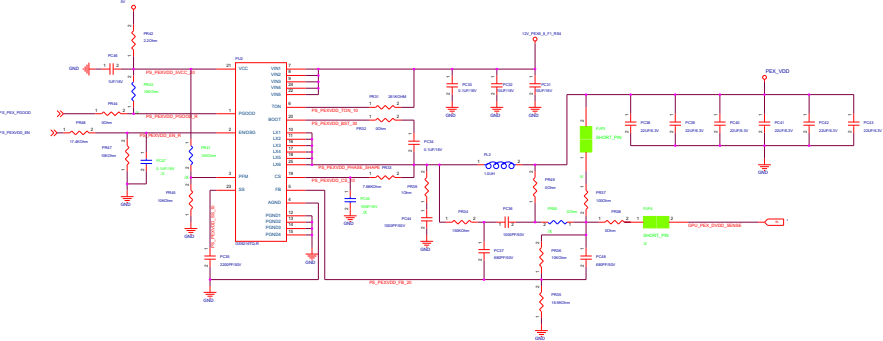
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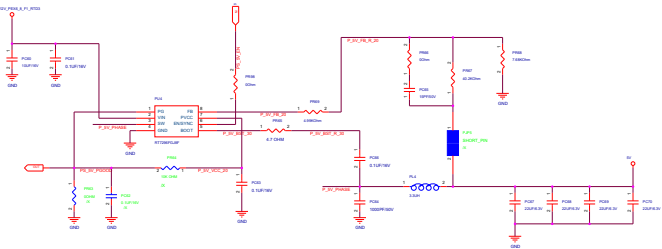
+ POE_CFG:LOW POWER
+ POE_CFG:HIGH POWER
+ VISA_DEVICE ENABLE
+ VISA_DEVICE DISABLE

```

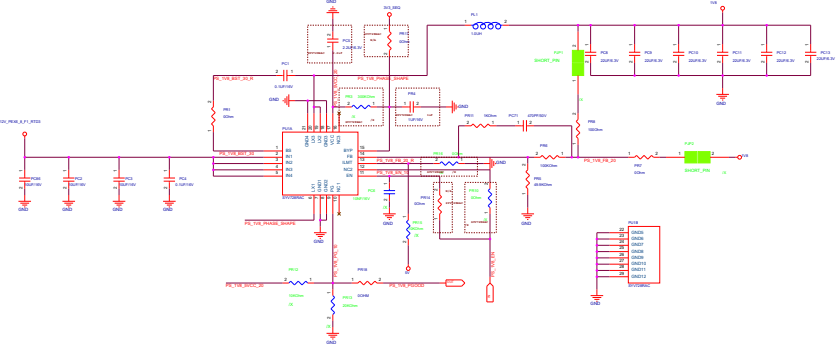


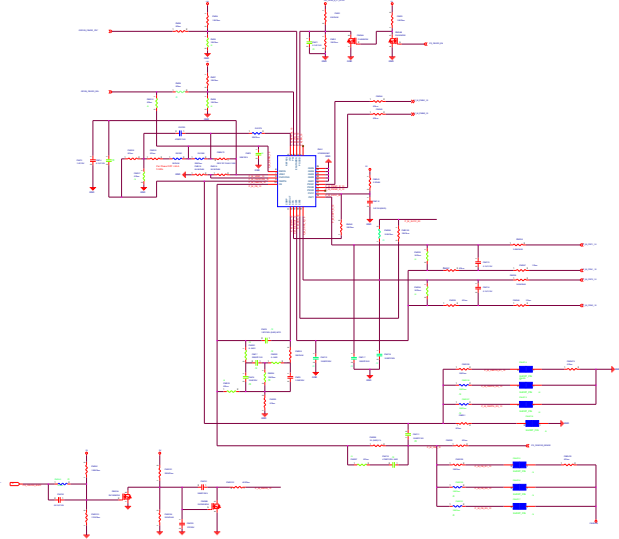






Name Clausen					
Title B		Discipline / Member Clausen			Sex Males
Public		Membership Expires On: 08/01/2027		Private	C G F I

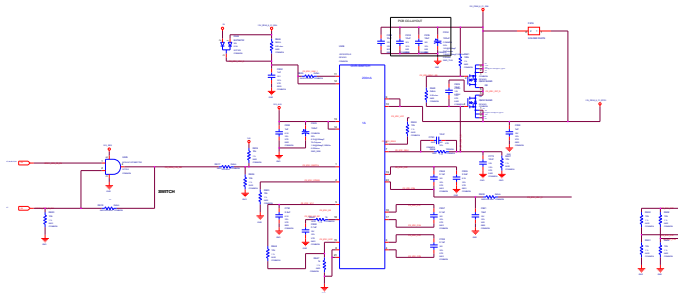


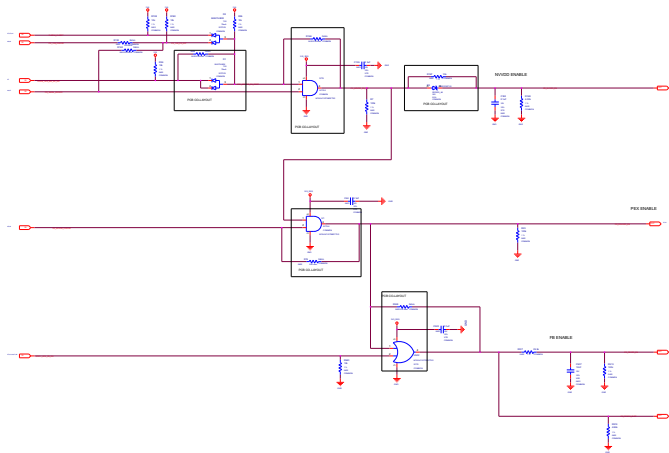


AND GATE LOGIC

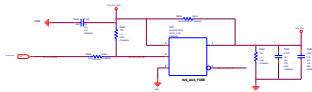
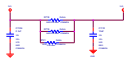
Q124	Q125	SWITCH	VOUT
0	0	0	0V
0	1	0	0V
1	0	0	0V
1	1	0	3.3V

SWITCH	VOUT
0	VOUT = 0V0
1	VOUT = 3V3

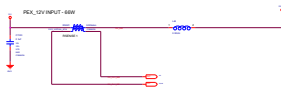




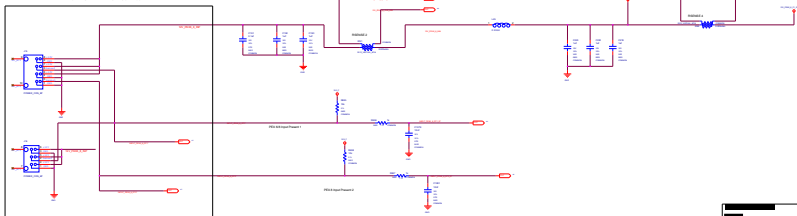
PEX_3V3 INPUT - 10W

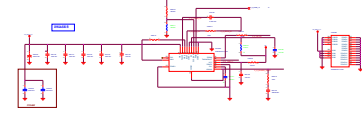
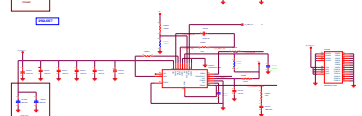
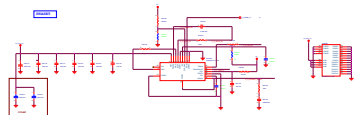
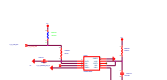
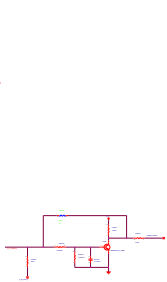
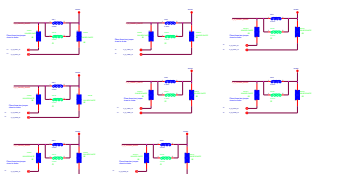
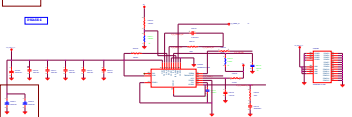
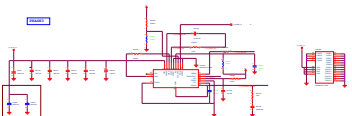
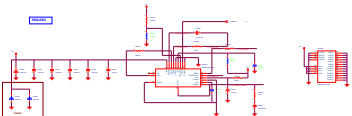
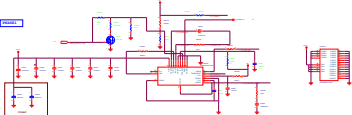


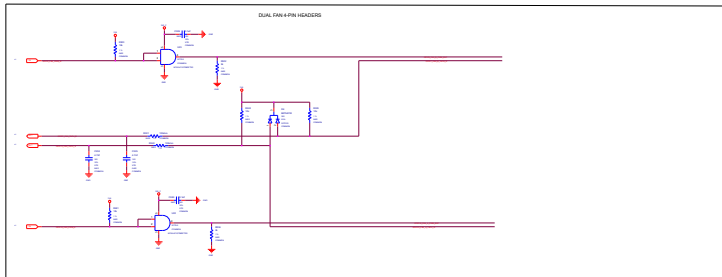
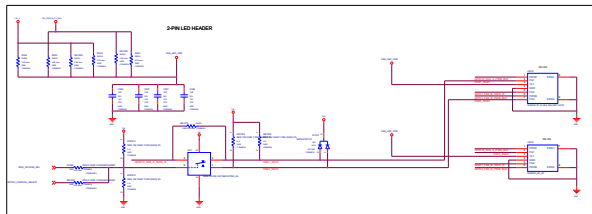
PEX_12V INPUT - 60W

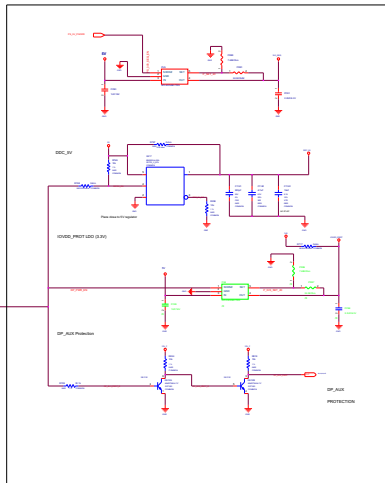
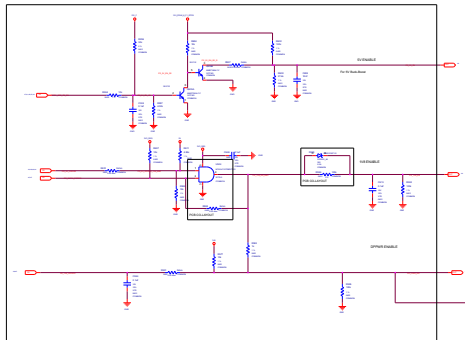


PEX8 INPUT 1 - 24V PCIe CON 150W

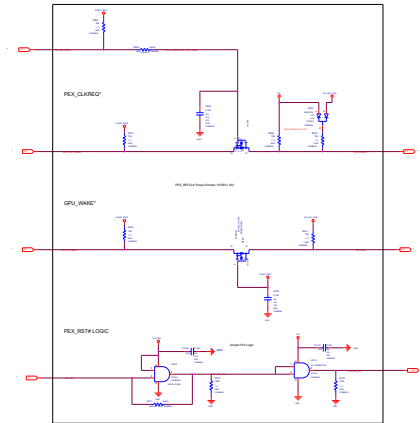


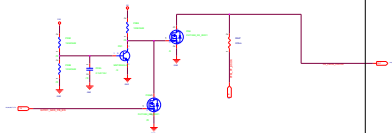


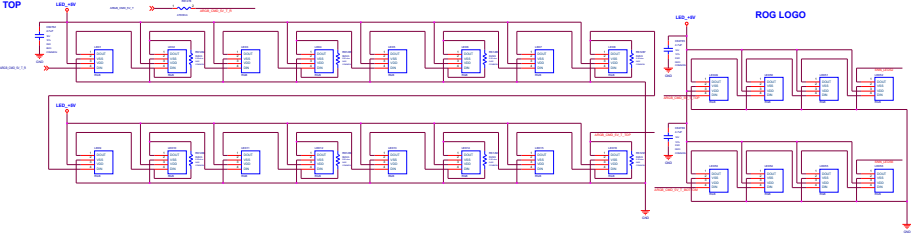


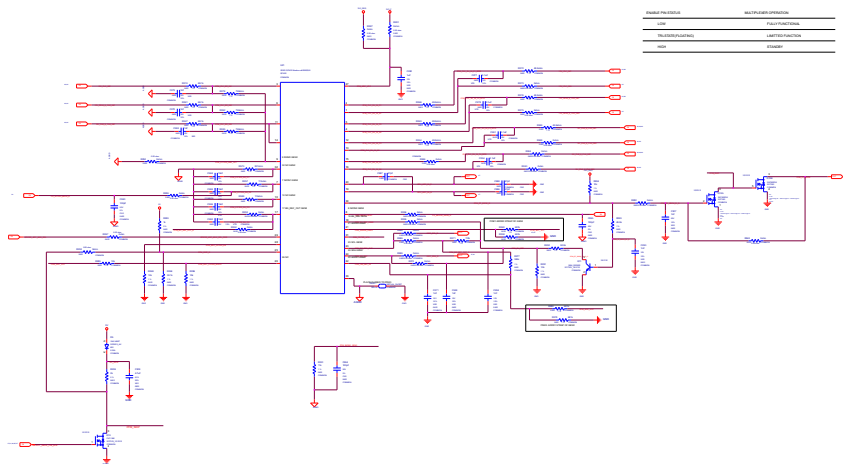






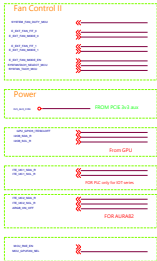
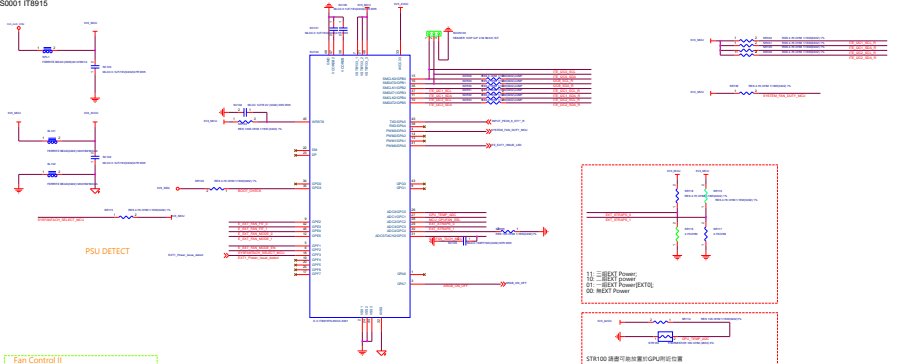
[illegible]

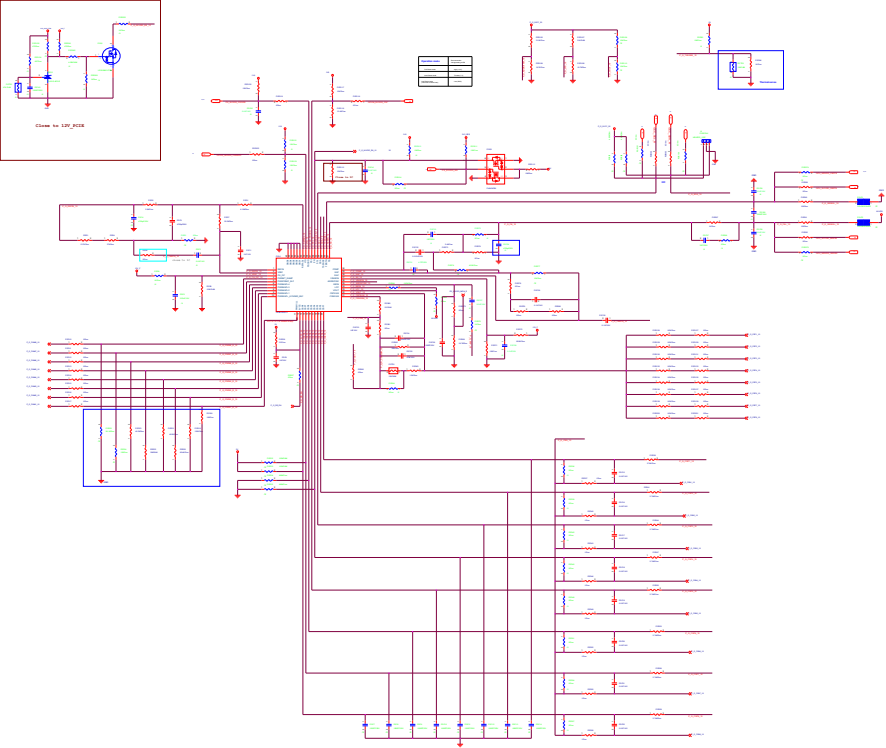




MODE PM STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRILS(SET/PLACING)	STAND ALONE
HIGH	DEVICE B

ENABLE PM STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRILS(SET/PLACING)	LIMITED FUNCTION
HIGH	STANDBY





Power



From 12V (for 外模式風扇使用, 任一組12V皆可)

From PCIE 3V3_AUX (for ITE)

From BUS 3V3 (for ITE logic判斷)

3v3_prot start after pex

From 5V (for 背板LED)

1V8

12V

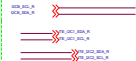


from ite for strix to swap fan1 and fan3 tach



From EXT 0 (外部電源第一組)

PSU DETECT INPUT



I2C

GPU I2CB Master (for ITE / ENE/NCT3933)

from ITE(FOR PLC ONLY)

ITE I2C MASTER (FOR AURA2 /UEST COLAY)

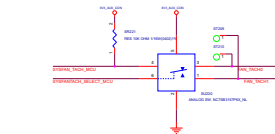
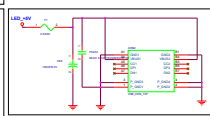
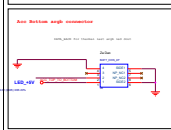
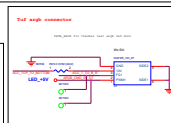
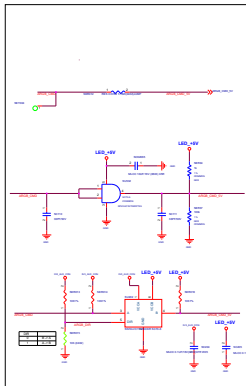
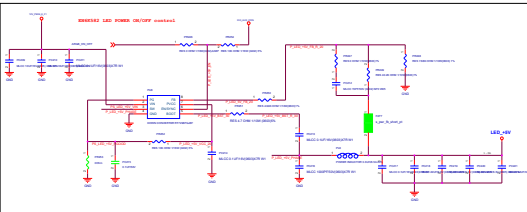
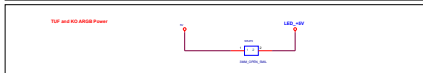
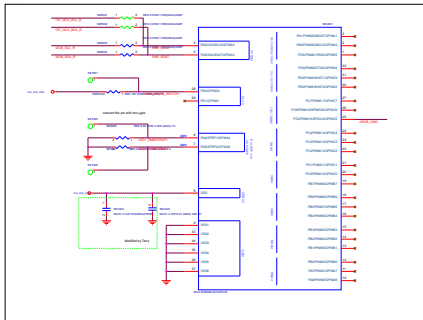
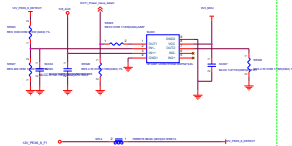
[illegible]

Diagram illustrating the mapping of the 16-bit VFX_FPAF_PRT_0 register to the 16-bit VFX_FPAF_PRT_1 register. The mapping is shown as a series of bit shifts. The top row shows the 16-bit register VFX_FPAF_PRT_0 with bits 15 down to 0. The bottom row shows the 16-bit register VFX_FPAF_PRT_1 with bits 15 down to 0. The mapping is indicated by arrows and bit numbers: bit 15 of VFX_FPAF_PRT_0 maps to bit 15 of VFX_FPAF_PRT_1, bit 14 maps to bit 14, bit 13 maps to bit 13, bit 12 maps to bit 12, bit 11 maps to bit 11, bit 10 maps to bit 10, bit 9 maps to bit 9, bit 8 maps to bit 8, bit 7 maps to bit 7, bit 6 maps to bit 6, bit 5 maps to bit 5, bit 4 maps to bit 4, bit 3 maps to bit 3, bit 2 maps to bit 2, bit 1 maps to bit 1, and bit 0 maps to bit 0.

File				
<File>				
Date	Encountered Member			City
II	<Date>			<State>
Date	Monday August 24, 2009		Time	8:00 AM



EXT1



VIN+ > 10.8V: Vout = L

VIN+ < 10.8V: Vout = HI

$$10.8V \times 20K\Omega / (100K\Omega + 20K\Omega) = 1.8V$$

SR301/SR311, 若僅需做一般連接度檢測, 其他零件可以省略, 但SR301/SR310/SR328需上件4.7K



EXT12V INPUT

EXT POWER connected DETECT PIN



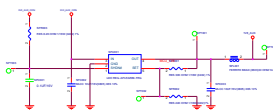
OUTPUT: AS ITE8915 INPUT



from ite8915



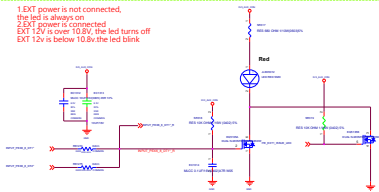
1v8_ref



$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2} \right)$$

$$0.8 \times (1 + 30K/24K) = 1.8V$$

1.EXT power is not connected,
the led is always on
2.EXT power is connected
EXT 12V is over 10.8V, the led turns off
EXT 12v is below 10.8v.the led blink





CAN ICES-3 (B)/NMB-3(B)



Re-design logo
Do not place this on reference board

