<Variant Name>

Title

PCIE RV370 64-bit 32/64MB BGA DI-VO-V LS

Schematic No.

105-A628XX-00A

Date:

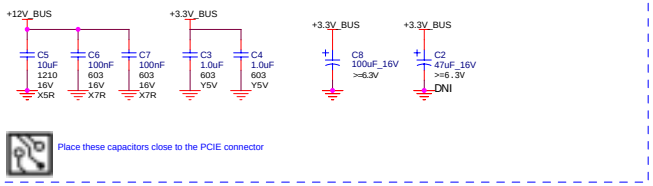
Monday, May 02, 2005

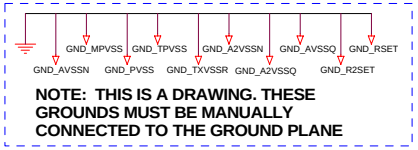
REVISION HISTORY

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	2005-01-07	PRELIMINARY BASED ON 105-A53300-00A

PCI-EXPRESS EDGE CONNECTOR





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Canada, L3T 7X6
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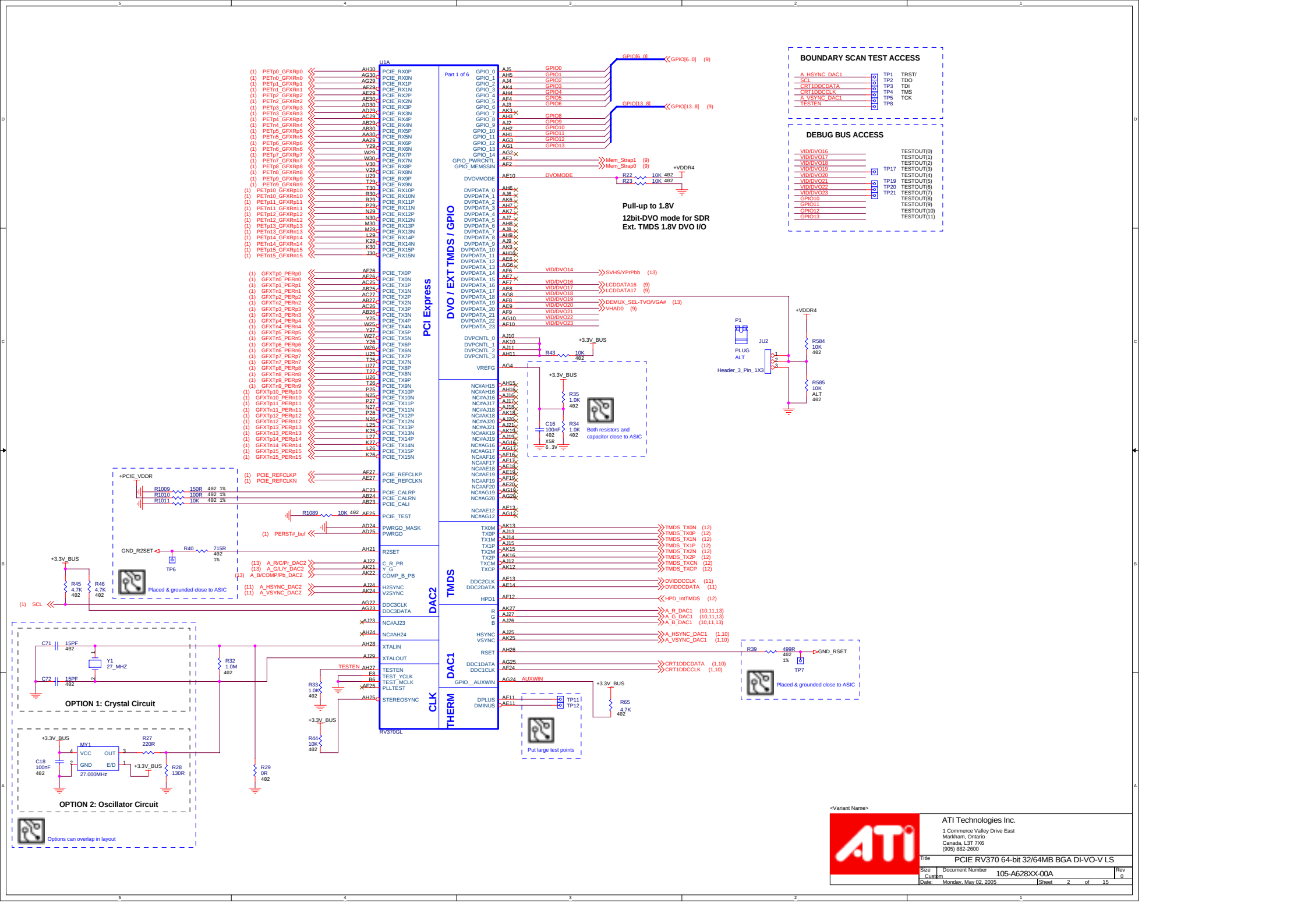
Title	PCIE RV370 64-bit 32/64MB BGA DI-VO-V LS		
Size C	Document Number 105-A628XX-00A		Rev 0
Date: Monday, May 02, 2005	Sheet 1	of 15	


U1A
Part 1 of 6
PCI Express
DVO / EXT TMDS / GPIO
TMDS
DAC2
DAC1
CLK
THERM
RV370GL
BOUNDARY SCAN TEST ACCESS
DEBUG BUS ACCESS
Pull-up to 1.8V
12bit-DVO mode for SDR
Ext. TMDS 1.8V DVO I/O
Both resistors and capacitor close to ASIC
Placed & grounded close to ASIC
Put large test points
OPTION 1: Crystal Circuit
OPTION 2: Oscillator Circuit
Options can overlap in layout
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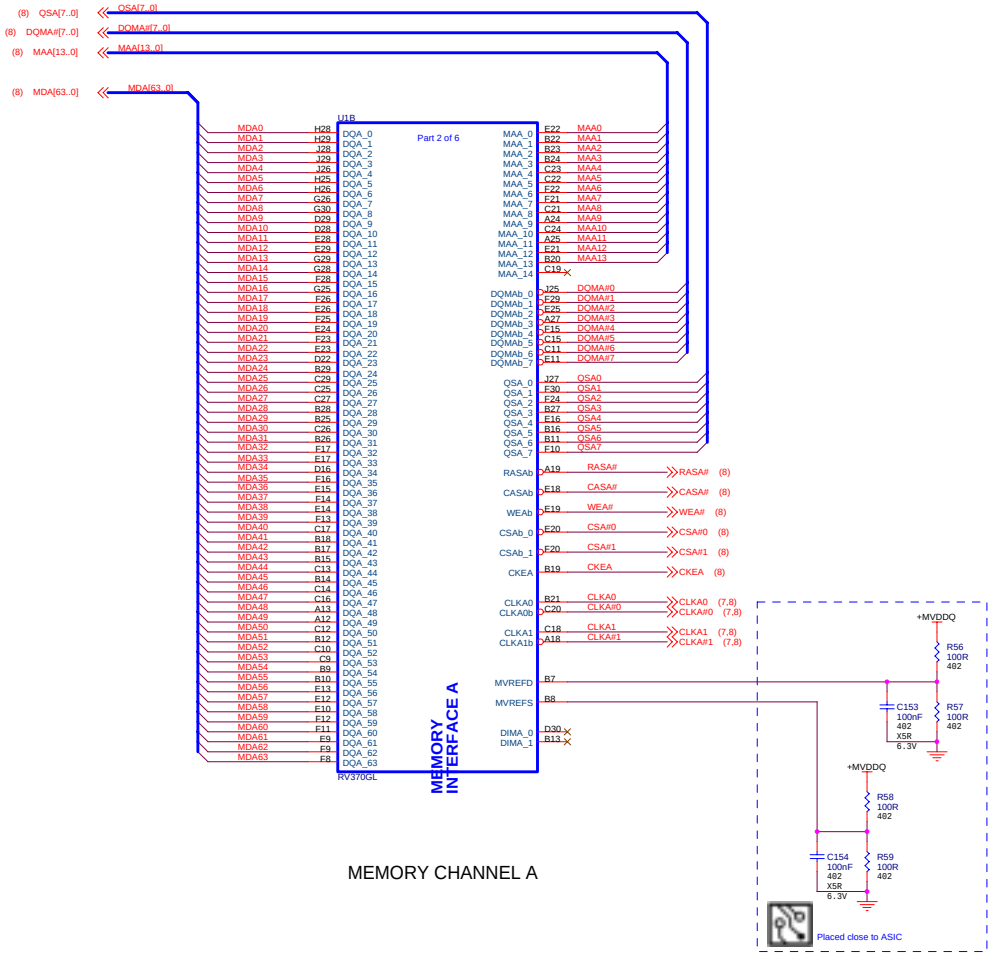
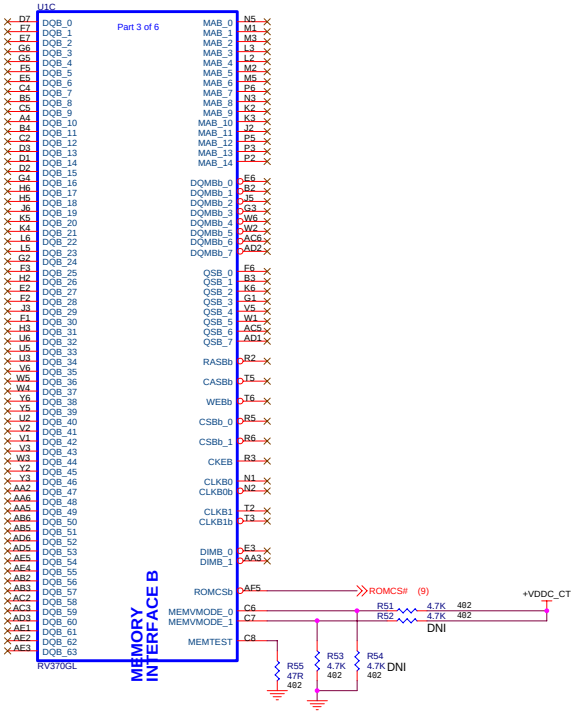


MEMORY CHANNEL A



MEMORY CHANNEL B

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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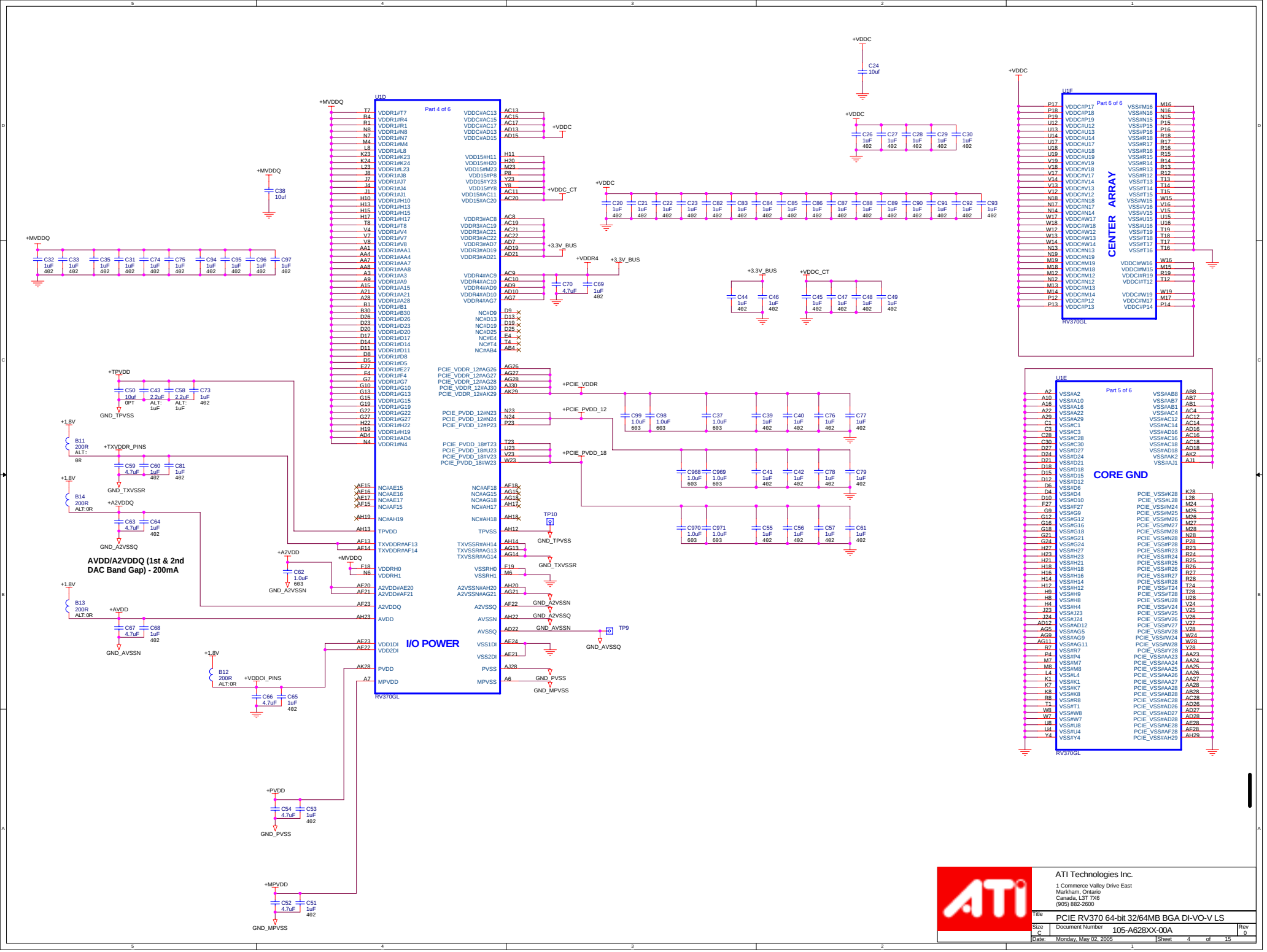
U1D
Part 4 of 6
I/O POWER
RV370GL
U1F
Part 6 of 6
CENTER ARRAY
RV370GL
U1E
Part 5 of 6
CORE GND
RV370GL
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
+MVDDQ
+VDDC
+VDDC_CT
+3.3V_BUS
+VDDR4
+TPVDD
+1.8V
+TXVDDR_PINS
+A2VDDQ
+AVDD
+VDDOI_PINS
+PVDD
+MPVDD
+A2VDD
+PCIE_VDDR
+PCIE_PVDD_12
+PCIE_PVDD_18
GND_TPVSS
GND_TXVSSR
GND_A2VSSQ
GND_A2VSSN
GND_AVSSN
GND_TPVSS
GND_TXVSSR
GND_A2VSSN
GND_AVSSN
GND_PVSS
GND_MPVSS
TP10
TP9
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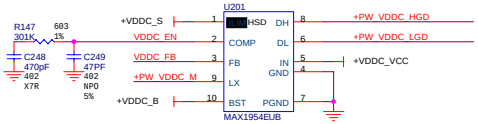
Regulator for VDDC (ASIC Core)

Vout = 1.2V ~ 1.3V

Part	Vout	R1	R2
0.8V Ref	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
	1.25V	1.00K 1% ATI P/N 3240100100	1.78K 1% ATI P/N 3240178100
	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100

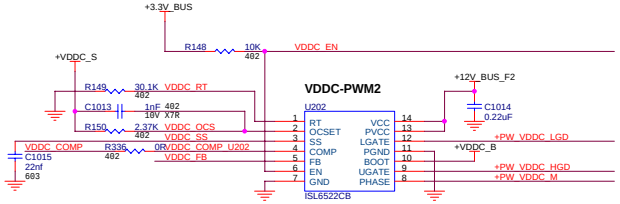
VDDC-PWM1



MAXIM MAX1954

MAXIM MAX1954A

VDDC-PWM2



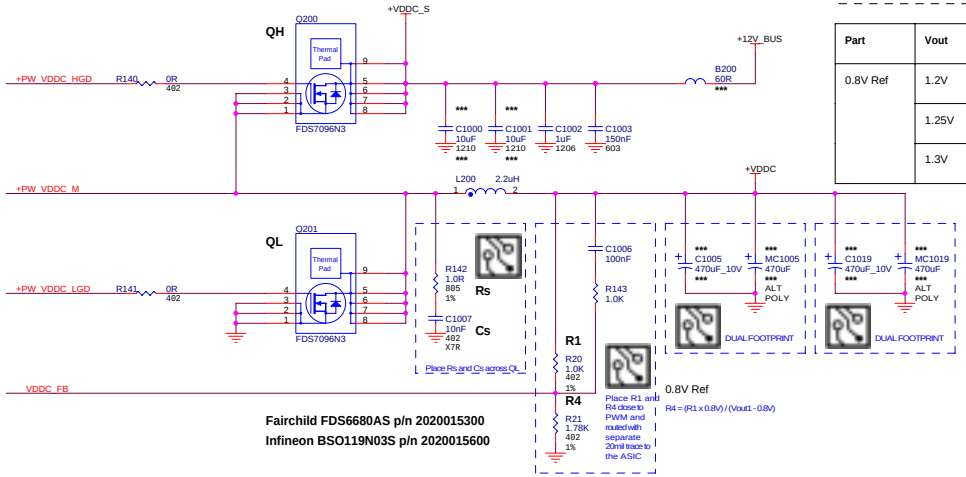
INTERSIL ISL6522

RICHTEK RT9232A

ANPEC APW7062A

ANPEC APW7062B

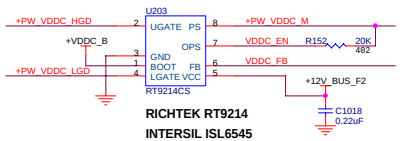
QH / QL



Fairchild FDS6680AS p/n 2020015300

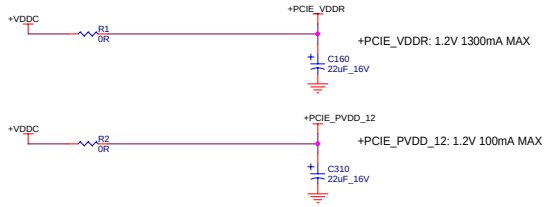
Infineon BSO119N03S p/n 2020015600

VDDC-PWM3

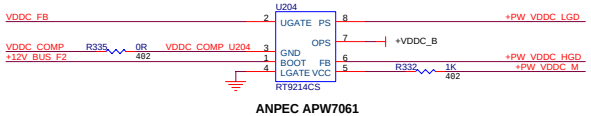


RICHTEK RT9214

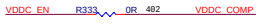
INTERSIL ISL6545



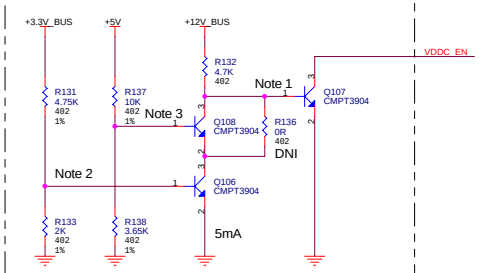
VDDC-PWM4



ANPEC APW7061



POWER SEQUENCING



Power Sequence Circuit to ensure SMPS_EN is released after +12V and +3.3V are both in regulation.

Note 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Note 2 When +3.3V gets closed to regulation, one of the two conditions of releasing SMPS_EN is active

Target for 920mV when +3.3 at min regulation (worse case)

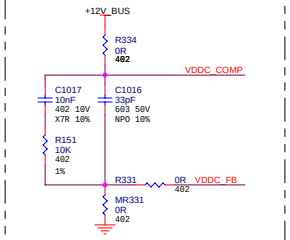
Typical trigger when +3.3V ramps above 2.2V (650mV)

Note 3 When +5V (derived from +12V) gets closed to regulation, one of the two conditions of releasing SMPS_EN is active

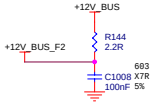
Target for 1.2V when +5 at min regulation (worse case)

Typical trigger when +5V ramps above 3.2V (850mV)

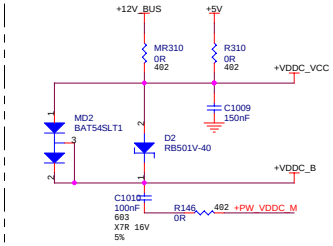
COMPENSATION CIRCUIT



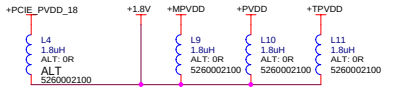
FILTERED +12V_BUS



BOOT CIRCUIT



+MPVDD: 10mA MAX
+PVDD: 25mA MAX
+TPVDD: 50mA MAX



Rails derived from +1.8V

+AVDD: 10mA MAX

+A2VDDQ: 20mA MAX

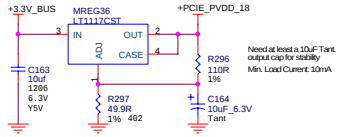
+VDDOI_PINS: 20mA MAX

+TXVDDR_PINS: 20mA MAX

Alt. Regulator for PCIE_PVDD_18

Vout = 1.82V

Iout = 500mA MAX



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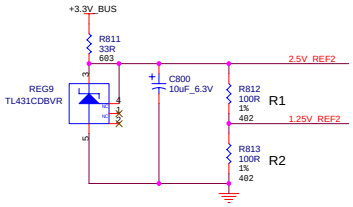
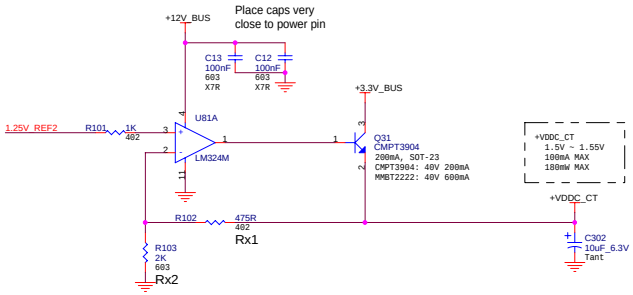
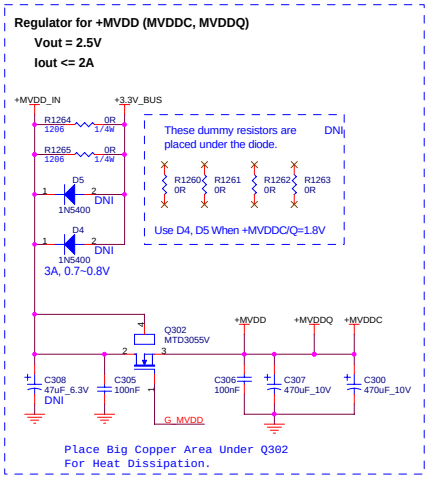


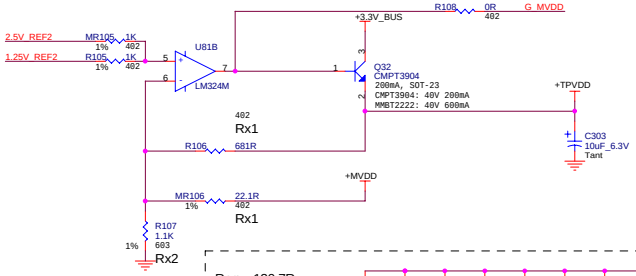
Voltage Req.	R1	R2
0.8V	150R P/N 3160150000 402	71.5R P/N 324075R500
1.25V	100R P/N 3160100000 402	100R P/N 3160100000 402
1.5V	100R P/N 3160100000 402	150R P/N 3160150000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

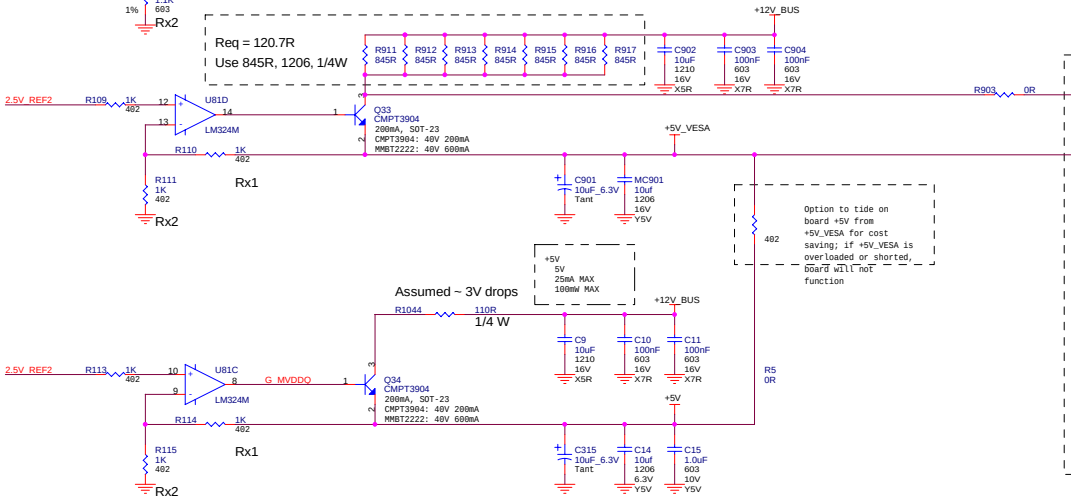
Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.55	475R (402, 1%) P/N 3160475000	2K (1%) P/N 3160200100 (402) P/N 3240200100 (603)
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240150100

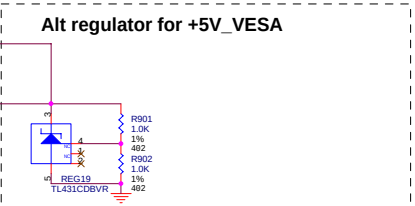
Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.61V	221R (402, 1%) P/N 3160221000	4.99K (402, 1%) P/N 3160499100
2.55V 2.5V Ref	22.1R 316022R100G 402	1.1K 3240110100G 603
2.5V	0R P/N 3230000000 603 P/N 3150000000 402	DNI



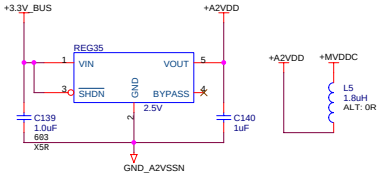




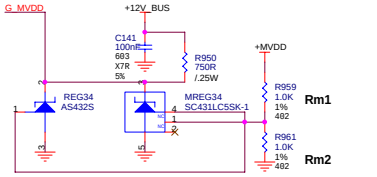




Alt. regulator for +A2VDD
Vout = 2.5V
Iout = 120mA MAX

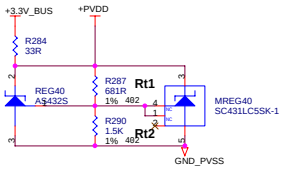


Alt. regulator for +MVDD
Vout = 2.5V ~ 2.6V
Iout <= 2A MAX

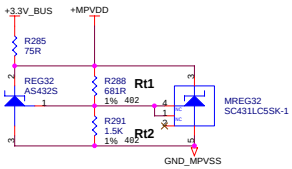


	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100

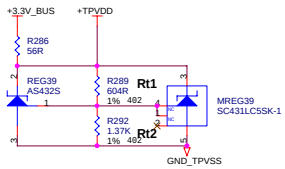
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



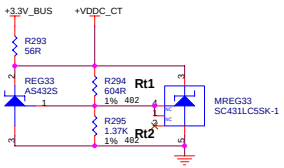
Alt regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX



Alt. regulator for +TPVDD
Vout = 1.65V ~ 1.85V
Iout = 20mA MAX



Alt. regulator for +VDDC_CT
Vout = 1.5V ~ 1.55V
Iout = 100mA MAX



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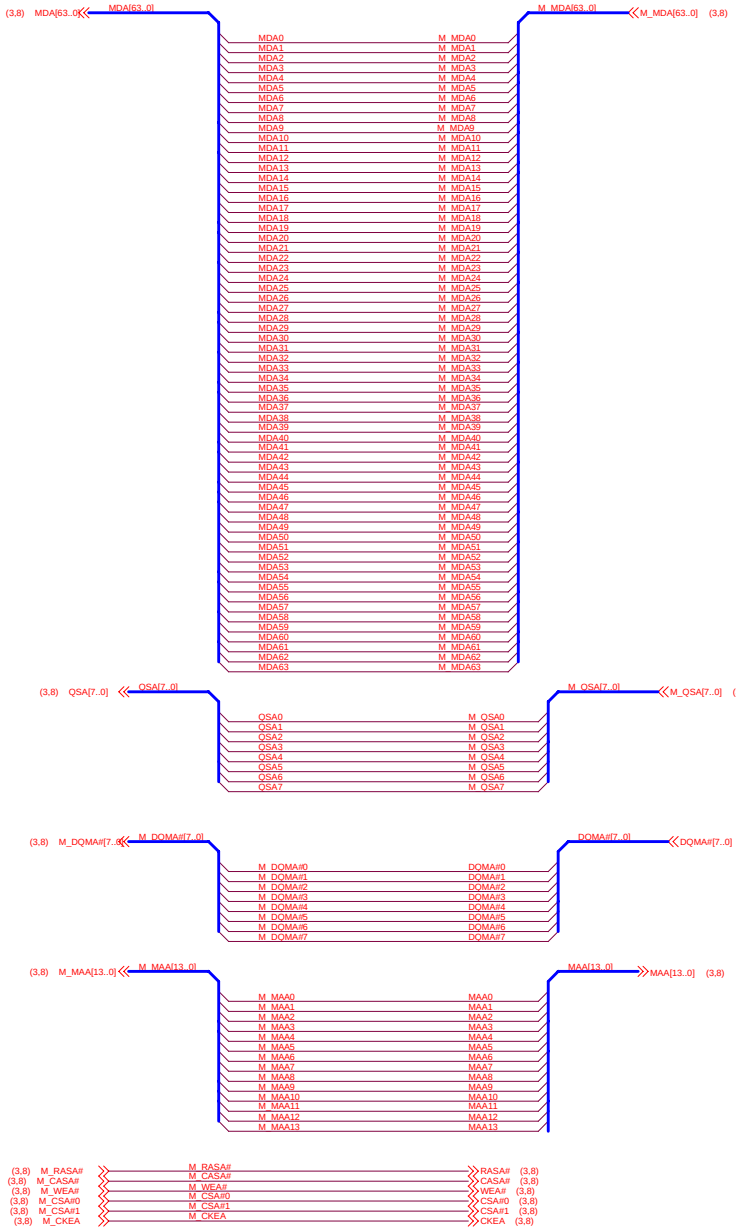
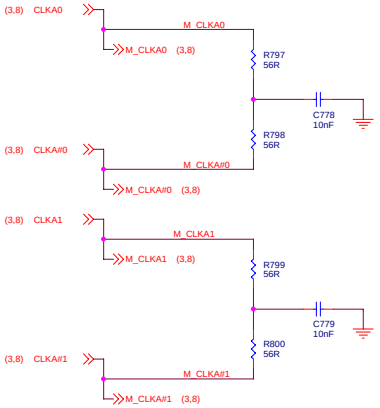


CLOCK terminations



<Variant Name>

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Size	Document Number	Rev
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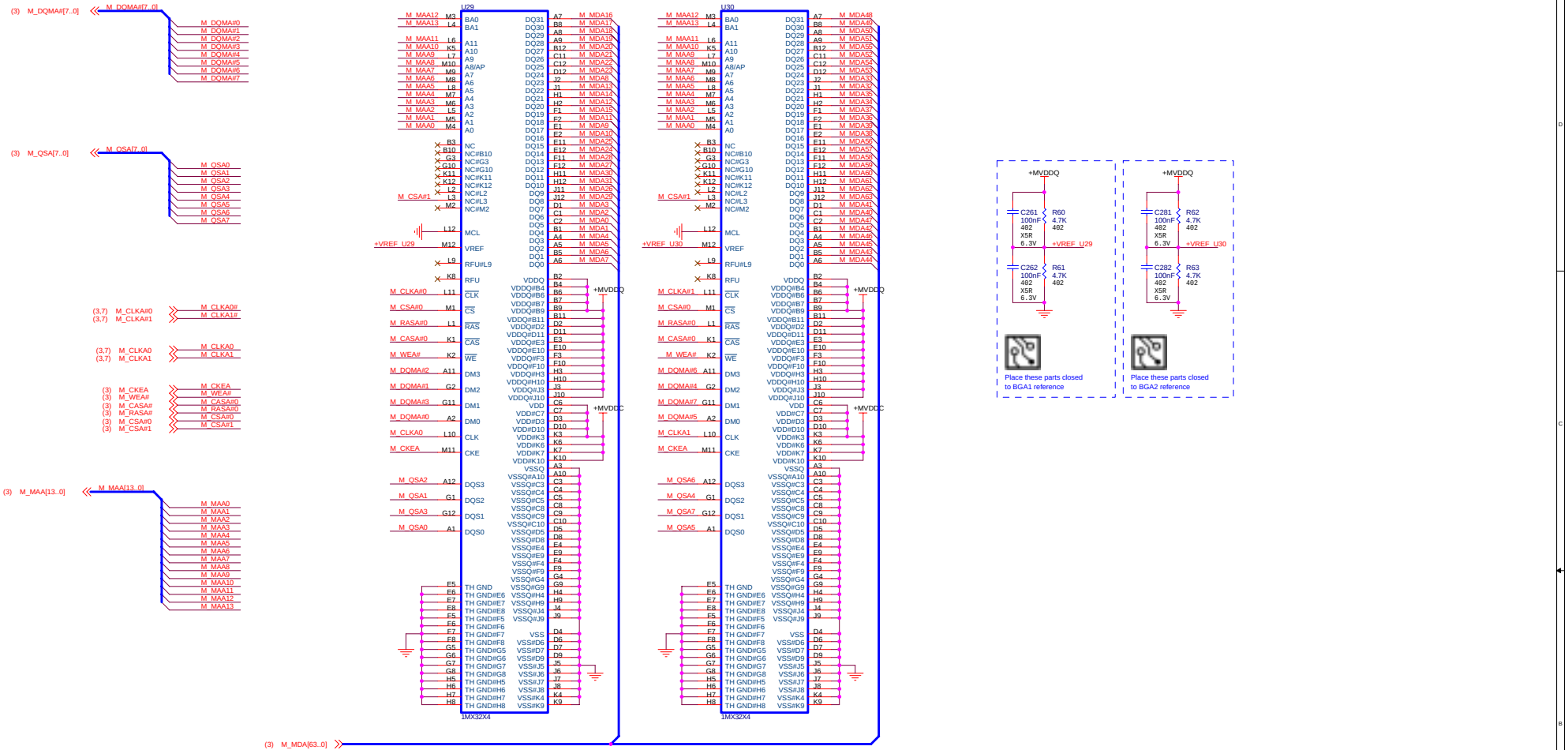

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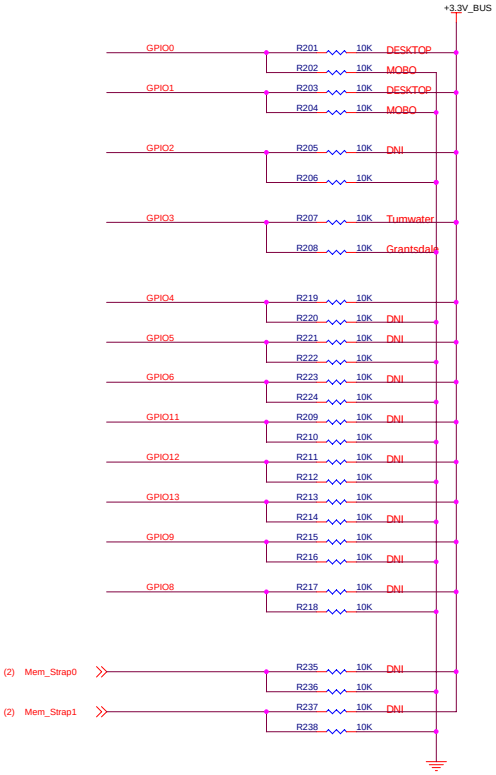
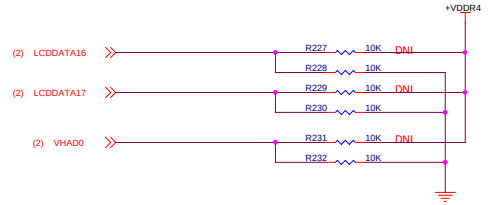
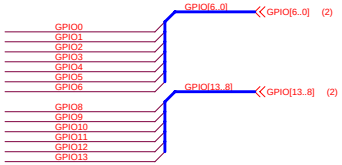
OPTION STRAPS





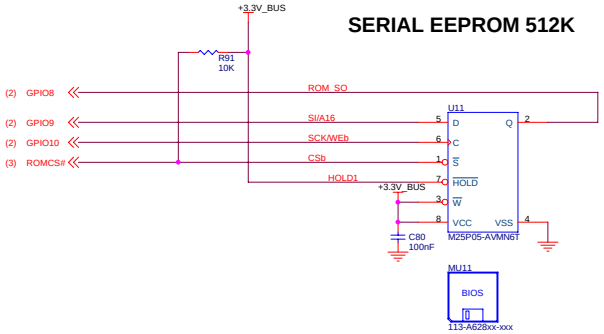


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K



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Canada, L3T 7X6
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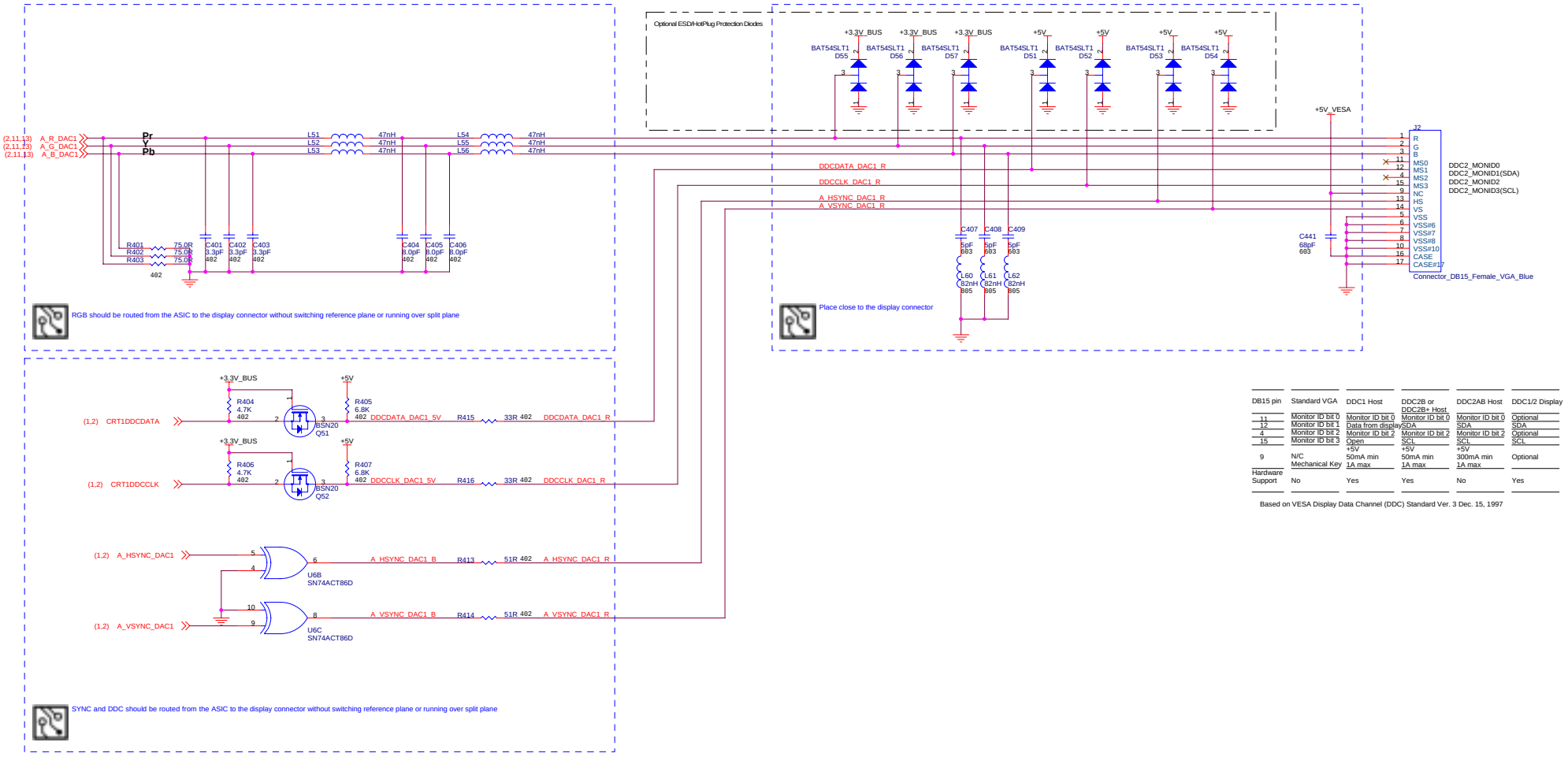

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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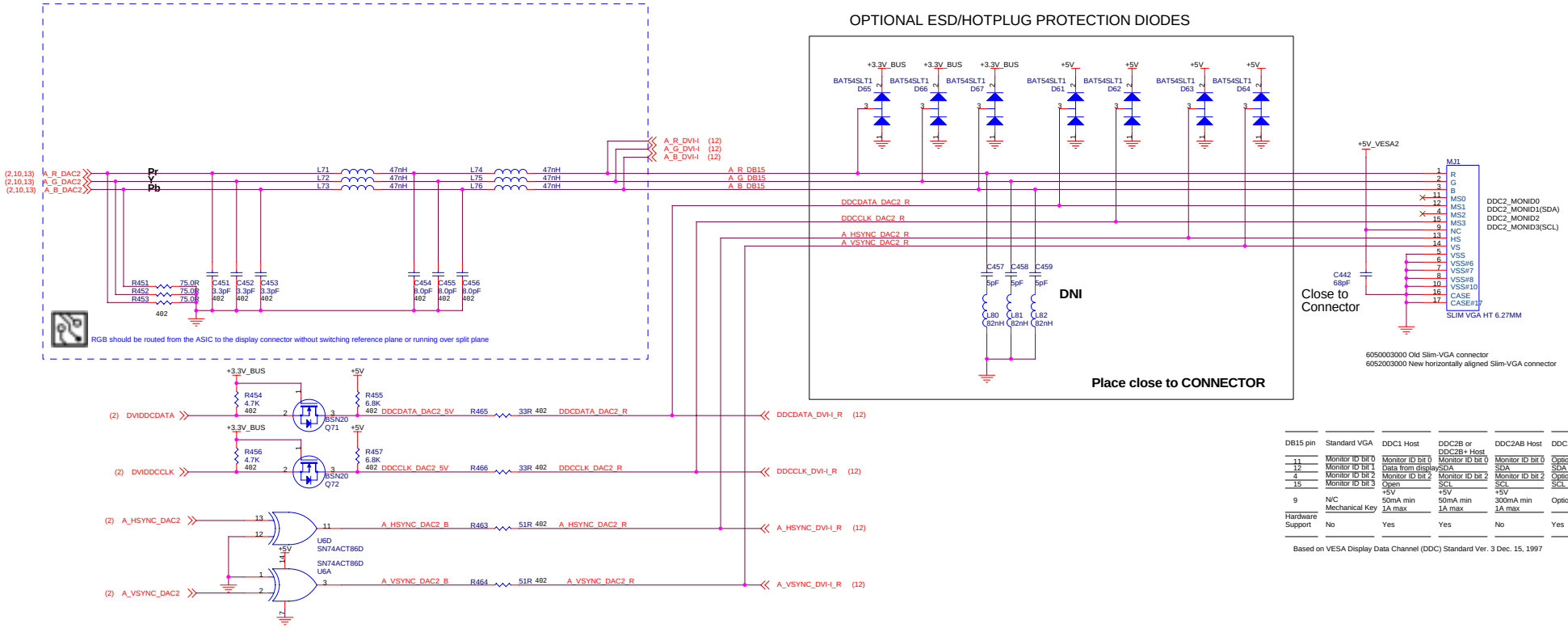
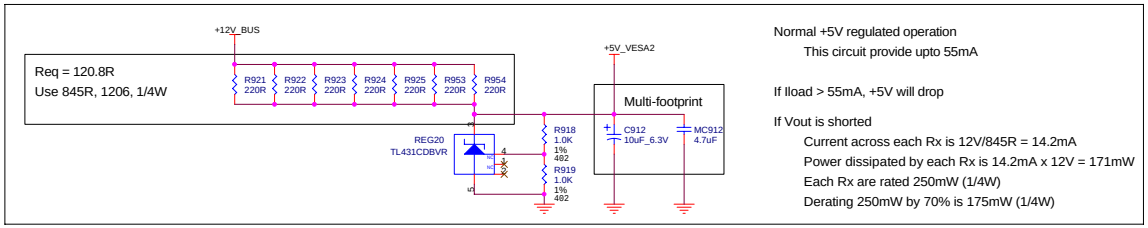


DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V	+5V	+5V	Optional
	Mechanical Key	50mA min	50mA min	300mA min	
		1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



Normal +5V regulated operation
This circuit provide upto 55mA

If Iload > 55mA, +5V will drop

If Vout is shorted
Current across each Rx is 12V/845R = 14.2mA
Power dissipated by each Rx is 14.2mA x 12V = 171mW
Each Rx are rated 250mW (1/4W)
Derating 250mW by 70% is 175mW (1/4W)

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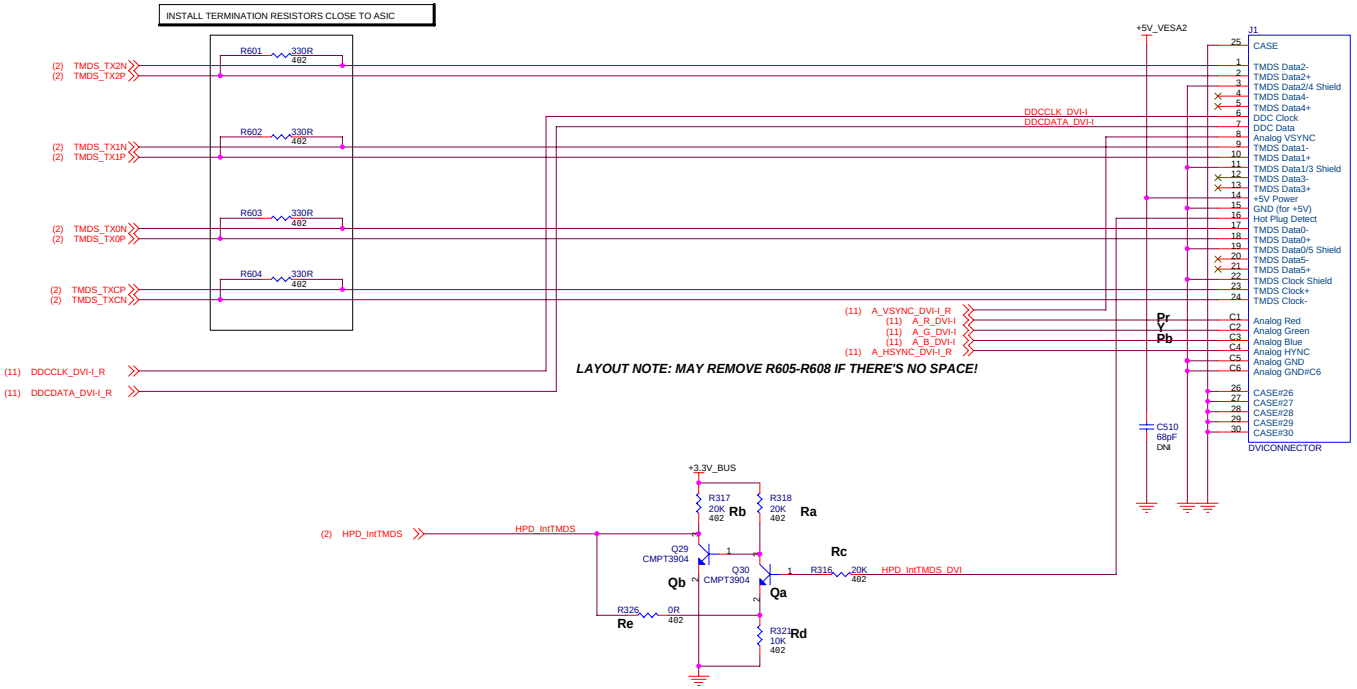
PRIMARY DVI-I CONNECTOR



LAYOUT NOTE: MAY REMOVE R605-R608 IF THERE'S NO SPACE!

STUFFING OPTIONS

Hot-Plug Detect Circuit	MUST INSTALL	MUST NOT INSTALL
Type A	Ra, Rb, Rc, Rd=0R, Qa, Qb	Re
Type B	Ra=0R, Rc, Rd=10K, Re, Qa	Rb, Qb

	HPD_ExtTMDS_DVI	HPD_ExtTMDS Type A	HPD_ExtTMDS Type B
NC	High Z	0 (0V)	0 (0V)
Connected	5V	1 (3.3V)	1 (3.3V)

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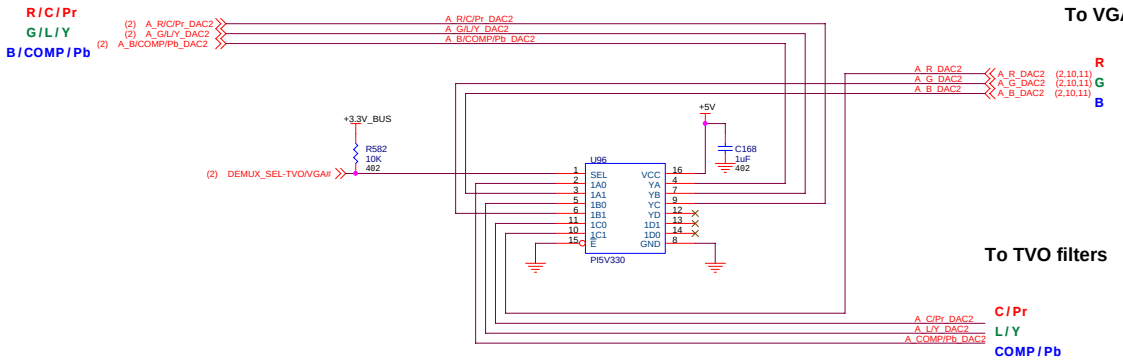
From DAC2

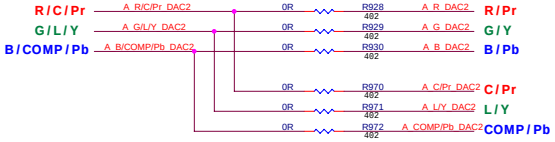
DAC2 DeMux



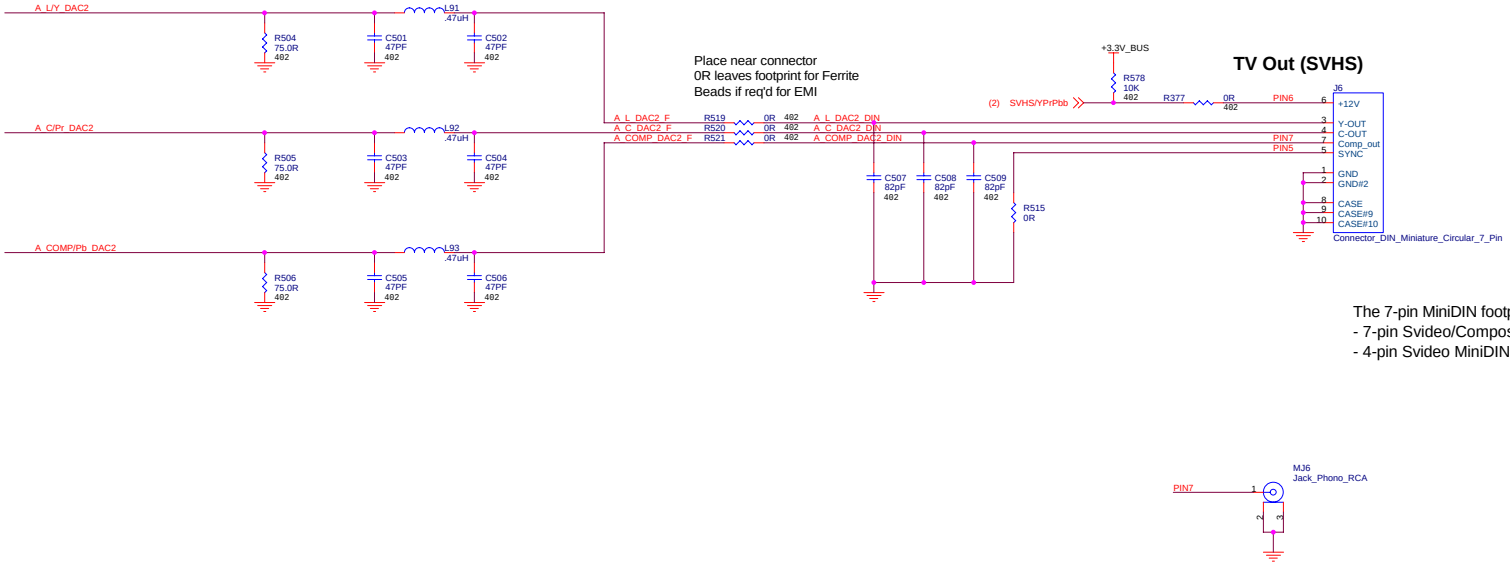
To VGA Filters

To TVO filters

DAC2 DeMux BYPASS



Place Resistors close to ASIC.



Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI

TV Out (SVHS)

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500
- 4-pin Svideo MiniDIN P/N 6070001000

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DVI/VGA SCREWS

ASSY1
SCREW
JACKSCREW

ASSY2
SCREW
JACKSCREW

ASSY15
SCREW
JACKSCREW

ASSY16
SCREW
JACKSCREW

Bracket Screws

ASSY3
SCREW
PAN_HEAD

MISC. BOARD PARTS

ASSY7
ANTISTATIC BAG
6_X_11
9040000900

ASSY6
ANTISTATIC BAG
6_X_11
9040000900

ASSY8
BLANK LABEL
9050005900

ASSY9
LABEL
2"_X_0.25"
9050004600

ASSY5
ATI LOGO LABEL
ATI_LOGO_LABEL
9110054500

ASSY10
ATI LOGO LABEL
ATI_LOGO_LABEL
9110054500

+12V_BUS
1
2
JU1

H101
heatsink
7120005800

H100
HEATSINK
7120005100

Spring push-pin

MH101
HEATSINK
7120002700

MH100
HEATSINK
7120008000

ITW push-pin

MT1
MT_Hole_0.136_in.

ATX Brackets

ASSY14
BRACKET
DVI, DIN, VGA
8020037000

ASSY12
BRACKET
VGA, DIN, VGA
8020037100

ASSY11
BRACKET
DVI, VGA
80200370A0

ASSY13
BRACKET
80200371A0

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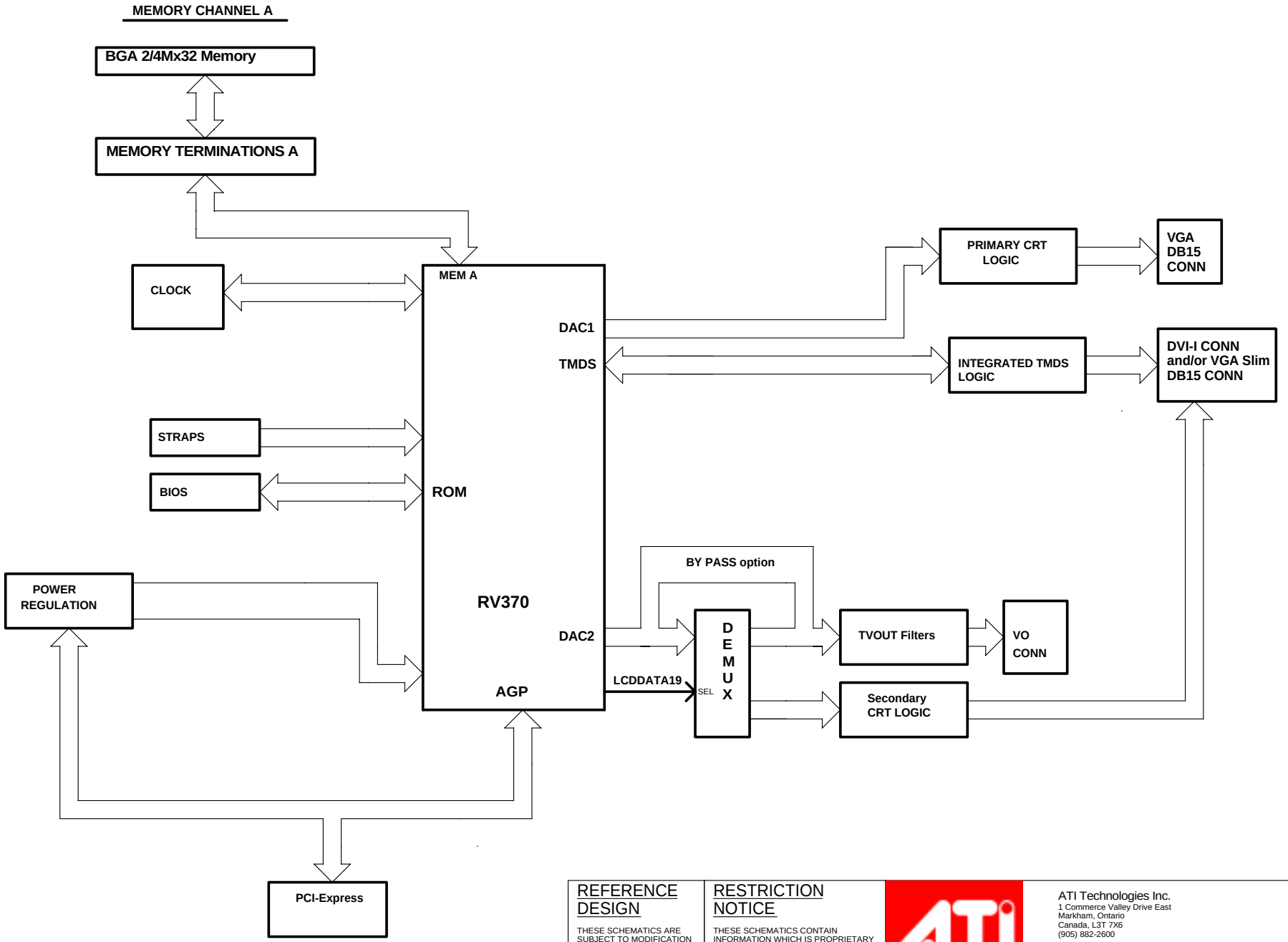

REFERENCE DESIGN

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RESTRICTION NOTICE

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