P672: GT215-128bit, 32Mx32 GDDR5

DL-DVI, VGA, HDMI

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10672-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10672-0001-100	GT215-450, 550/1375MHz 512MB 32Mx16 BGA170 1800MHz GDDR5 DVI-I/VGA/HDMI
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TABLE OF CONTENTS

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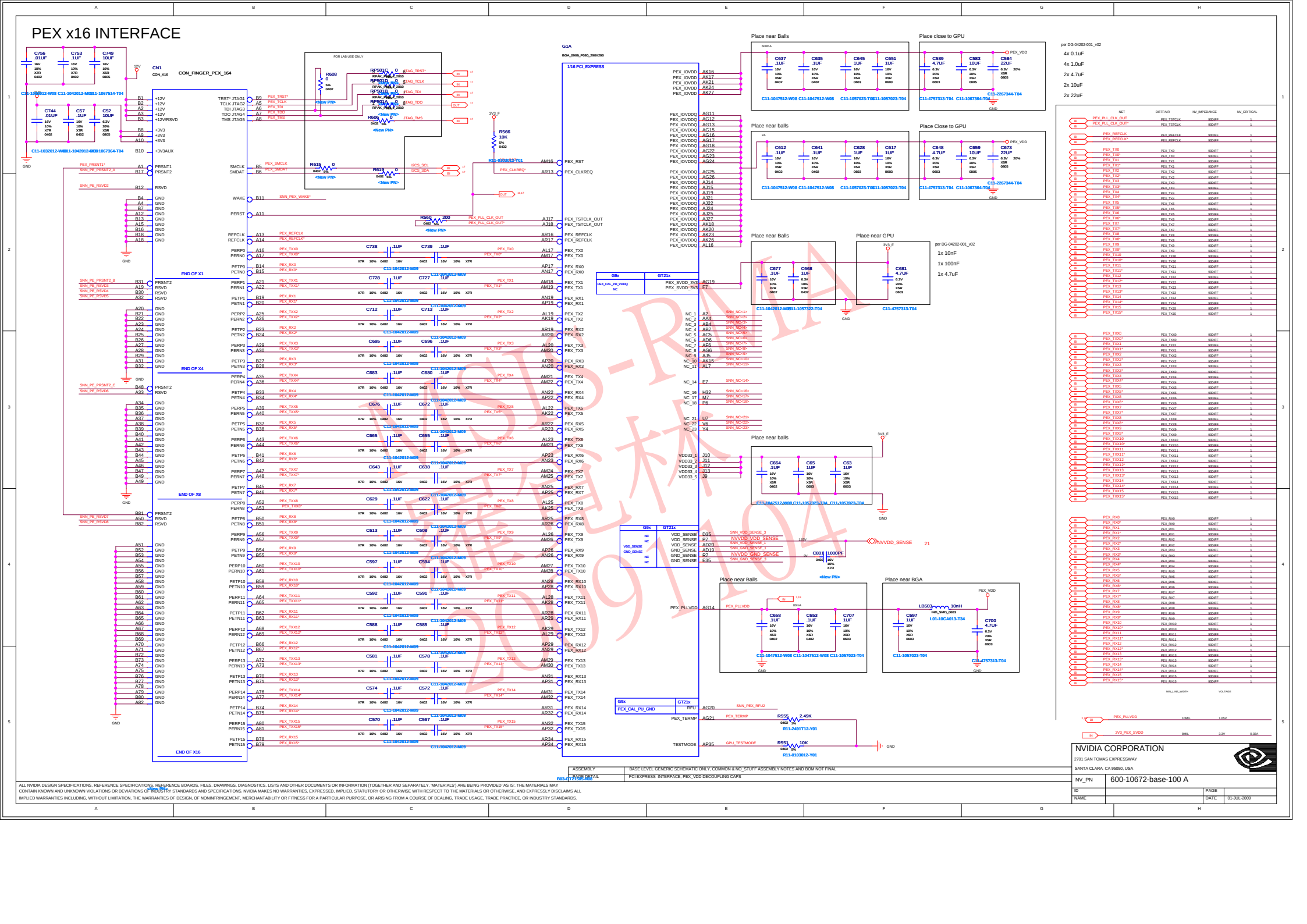
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

PEX x16 INTERFACE

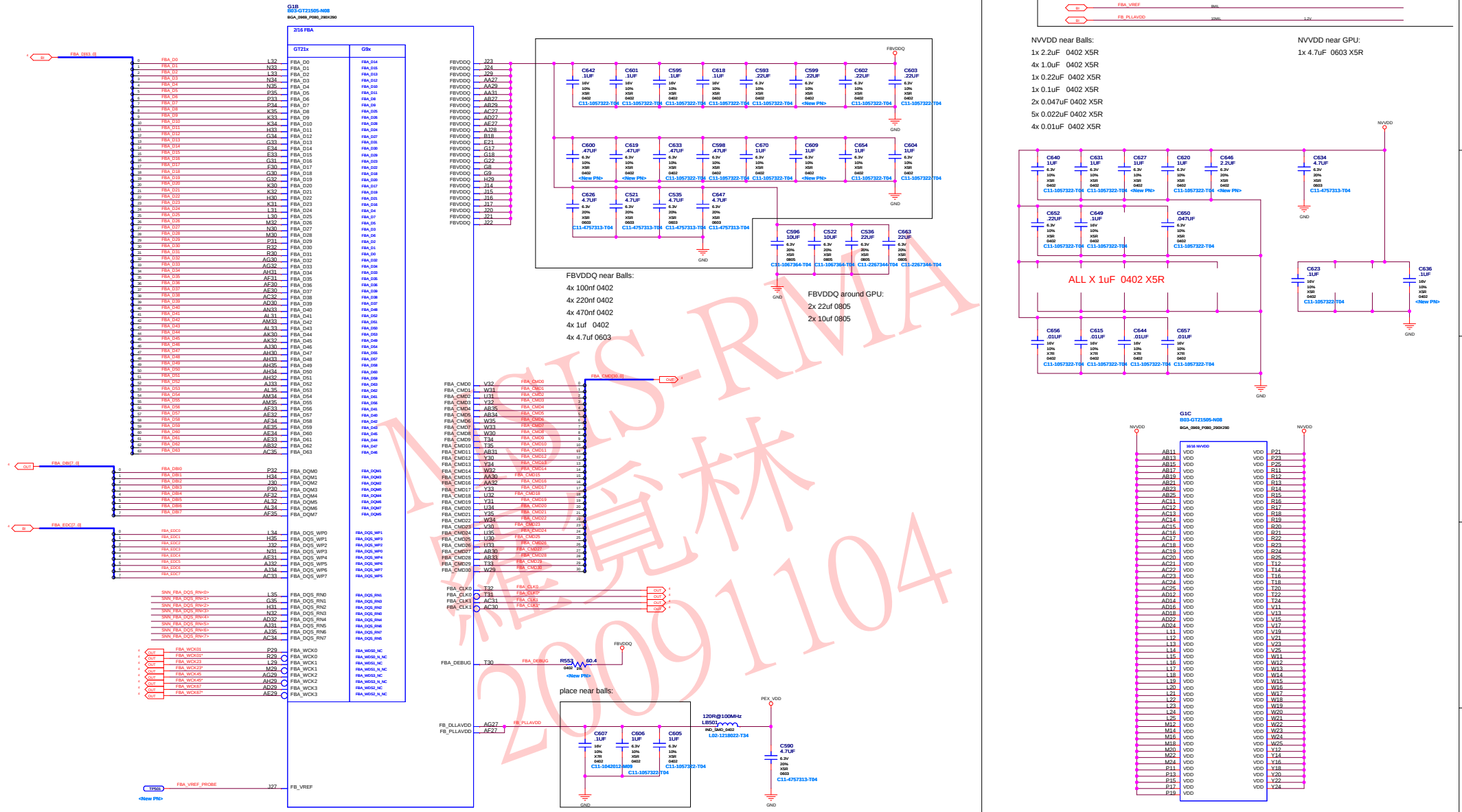


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS

B03-C172505-A03

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

MEMORY Partition A - GPU, FBVDD/Q & NVVDD DECOUPLING



NET	MIN_LINE_WIDTH	VOLTAGE
FBA_VREF	8MIL	
FB_PLLAVDD	10MIL	1.2V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY INTERFACE, GPU NVVDD & FBVDDQ DECOUPLING CAPS

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NV_PN	600-10672-base-100 A		
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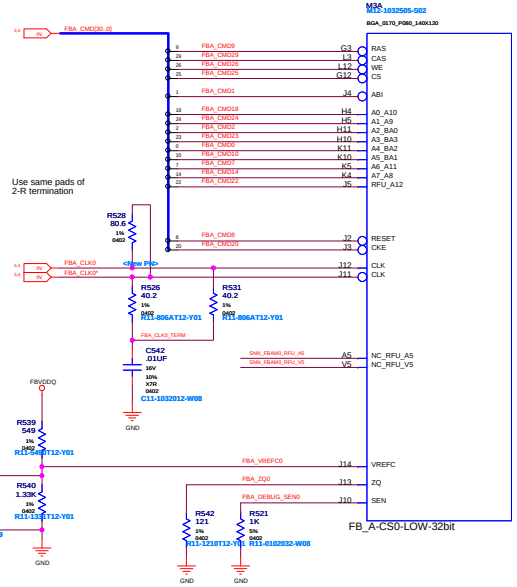
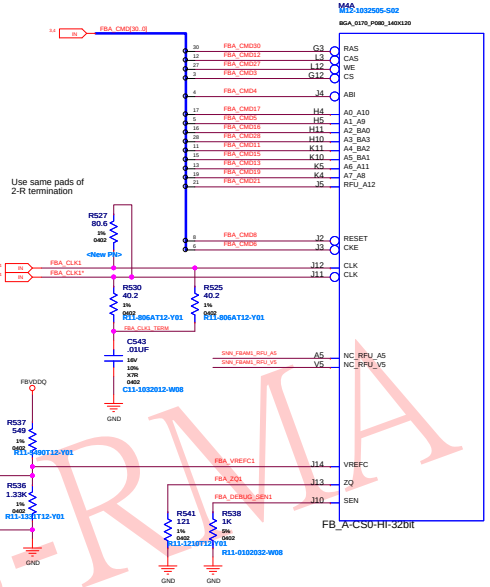
MEMORY Partition A



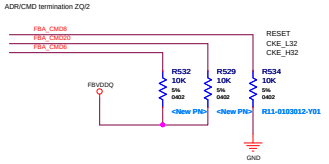
GT21x CMD MAP

	0..31	32..63
CMD0	A4_BA2	
CMD1	ABI*	
CMD2	A3_BA0	
CMD3		CS*
CMD4		ABI*
CMD5		A1_A9
CMD6		CKE*
CMD7	A5_A11	
CMD8	RST*	RST*
CMD9	RAS*	
CMD10	A5_BA1	
CMD11		A4_BA2
CMD12		CAS*
CMD13		A6_A11
CMD14	A7_A8	
CMD15		A5_BA1
CMD16		A2_BA0
CMD17		A0_A10
CMD18	A0_A10	
CMD19		A7_A8
CMD20	CKE*	
CMD21		A12_RFU
CMD22	A12_RFU	
CMD23	A3_BA3	
CMD24	A1_A9	
CMD25	CS*	
CMD26	WE*	
CMD27		WE*
CMD28		A3_BA3
CMD29	CAS*	
CMD30		RAS*

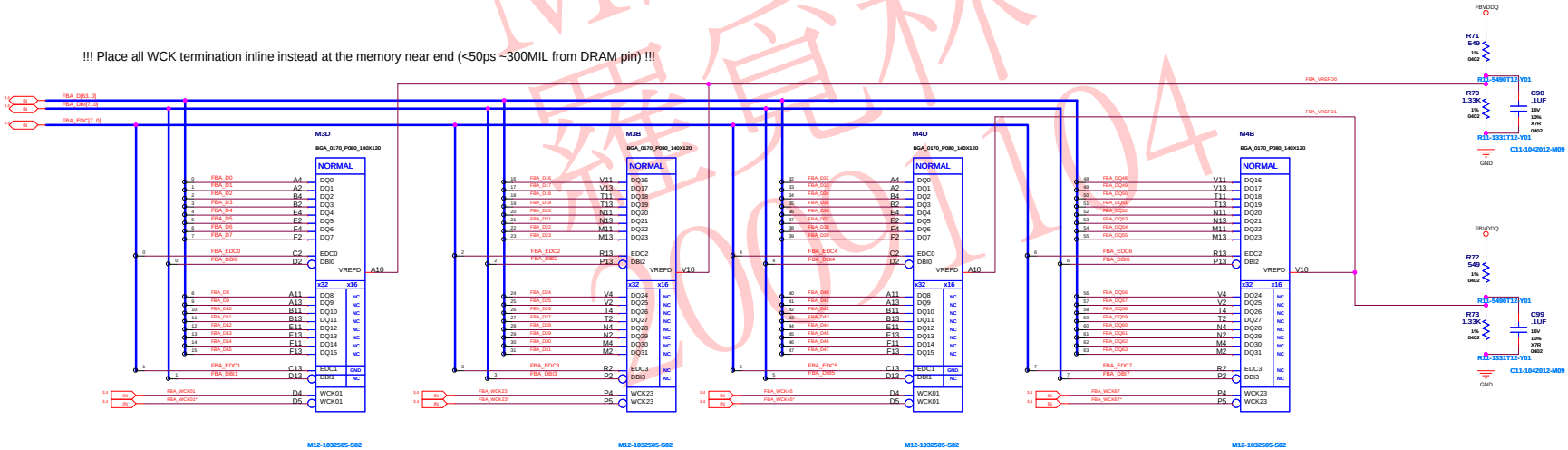


NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
FBA_DBI[3..0]		40OHM	1
FBA_DBI[7..0]		40OHM	1
FBA_EDC[7..0]		40OHM	1
FBA_CMD[30..0]		40OHM	1
FBA_CLK0	FBA_CLK0	80DIFF	1
FBA_CLK0*	FBA_CLK0	80DIFF	1
FBA_CLK1	FBA_CLK1	80DIFF	1
FBA_CLK1*	FBA_CLK1	80DIFF	1
FBA_WCK01	FBA_WCLK01	80DIFF	1
FBA_WCK01*	FBA_WCLK01	80DIFF	1
FBA_WCK23	FBA_WCLK23	80DIFF	1
FBA_WCK23*	FBA_WCLK23	80DIFF	1
FBA_WCK45	FBA_WCLK45	80DIFF	1
FBA_WCK45*	FBA_WCLK45	80DIFF	1
FBA_WCK67	FBA_WCLK67	80DIFF	1
FBA_WCK67*	FBA_WCLK67	80DIFF	1

	VOLTAGE	MIN_LINE_WIDTH
FBA_VREFC0	0.900V	12MIL
FBA_VREFC1	0.900V	12MIL
FBA_VREFD0	0.900V	12MIL
FBA_VREFD1	0.900V	12MIL
FBA_CLK0_TERM	0.900V	7.03MIL
FBA_CLK1_TERM	0.900V	7.03MIL
FBA_WCK01_CT	0.900V	7.03MIL
FBA_WCK23_CT	0.900V	7.03MIL
FBA_WCK45_CT	0.900V	7.03MIL
FBA_WCK67_CT	0.900V	7.03MIL



!!! Place all WCK termination inline instead at the memory near end (<50ps ~300MIL from DRAM pin) !!!



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 32Mx32 GDDR5 MEMORIES, FBA CLK TERMS

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NV_PN	600-10672-base-100 A		
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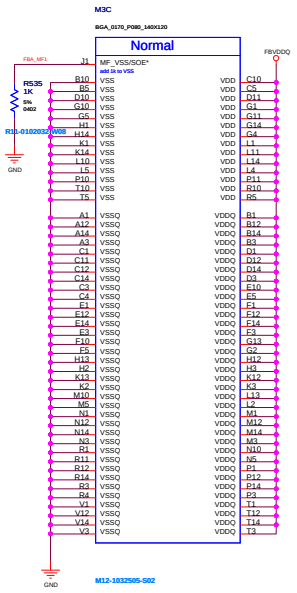
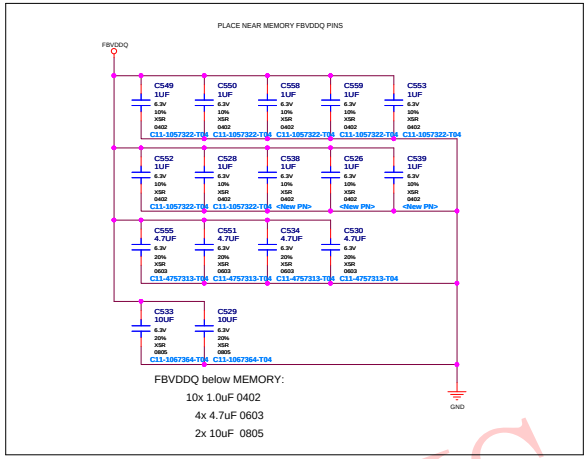
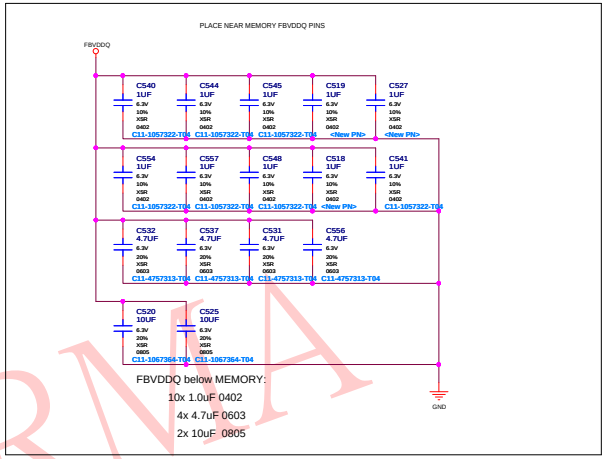
MEMORY Partition A - Decoupling

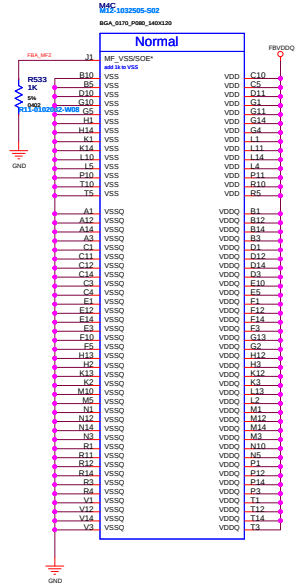


Decoupling for FBA 0..31

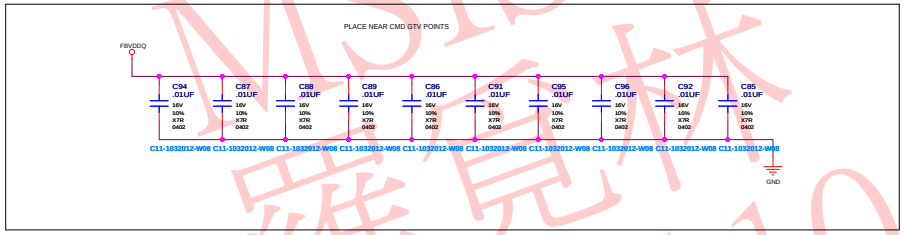


Decoupling for FBA 32..63





Return path coupling GND/FBVDDQ for FBA



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

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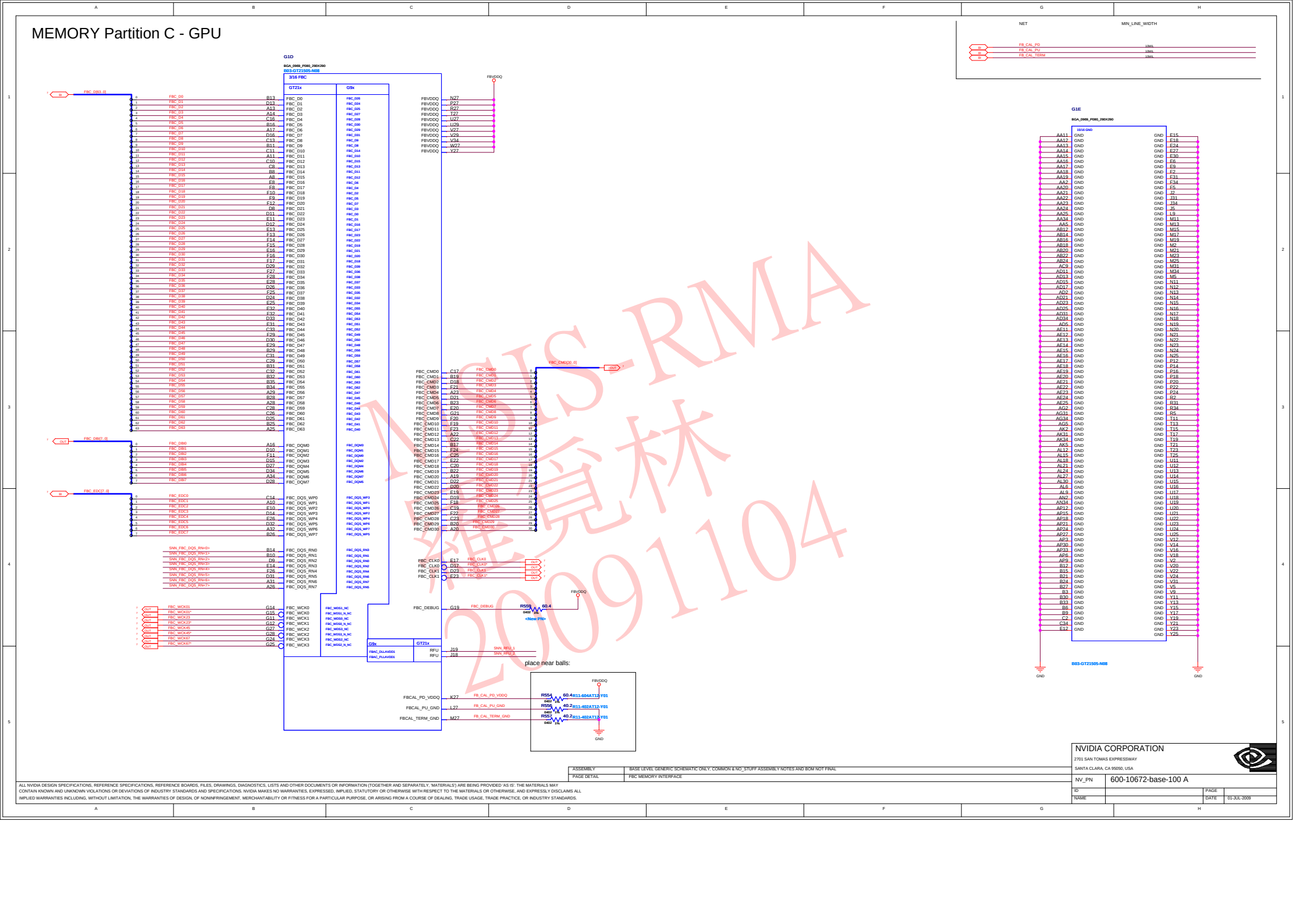
MEMORY Partition C - GPU



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY INTERFACE

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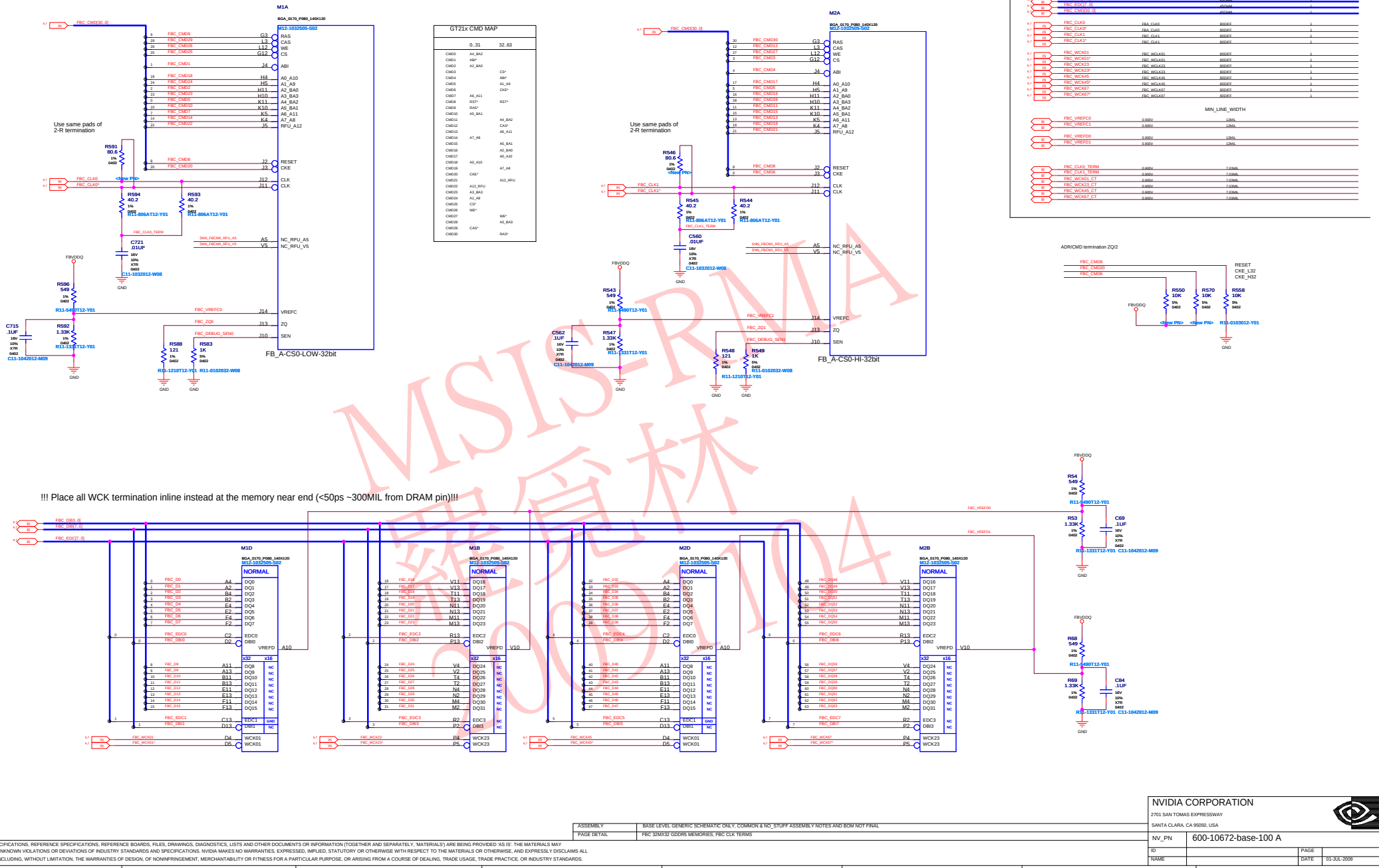
MEMORY Partition C



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 32MX32 GDDR5 MEMORIES, FBC CLK TERMS

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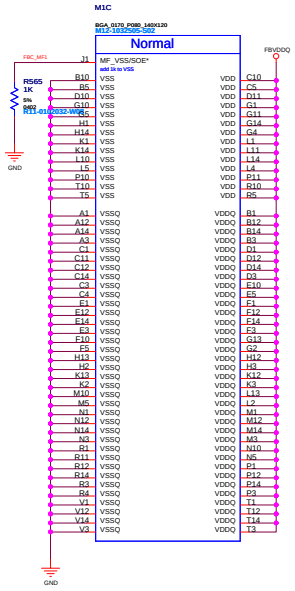
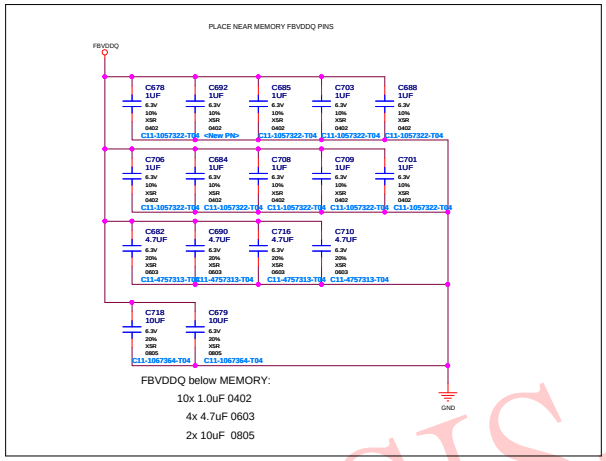
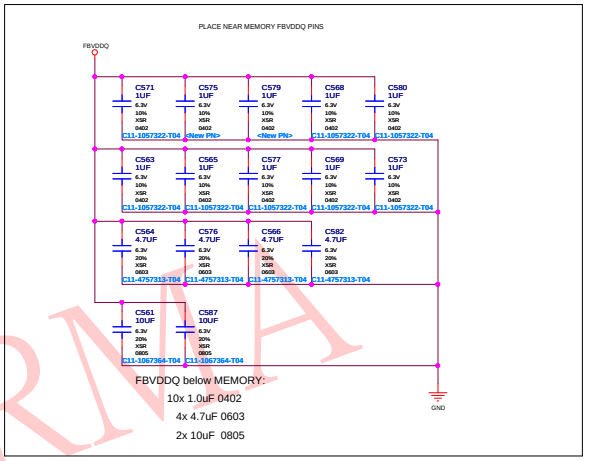
MEMORY PARTITION C DECOUPLING



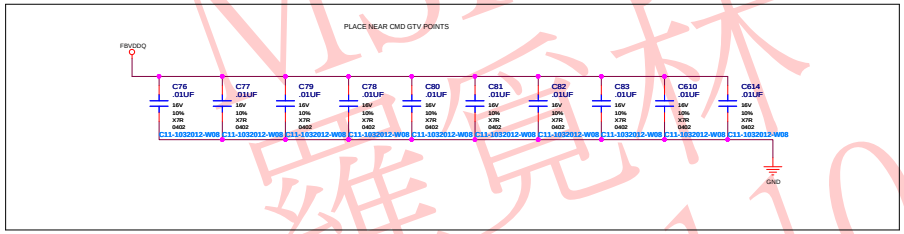
Decoupling for FBC 0..31

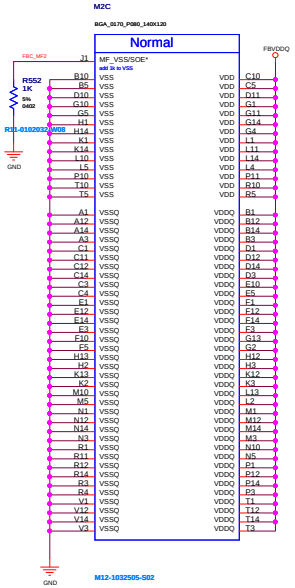


Decoupling for FBC 32..63



Return path coupling GND/FBVDDQ for FBC





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS

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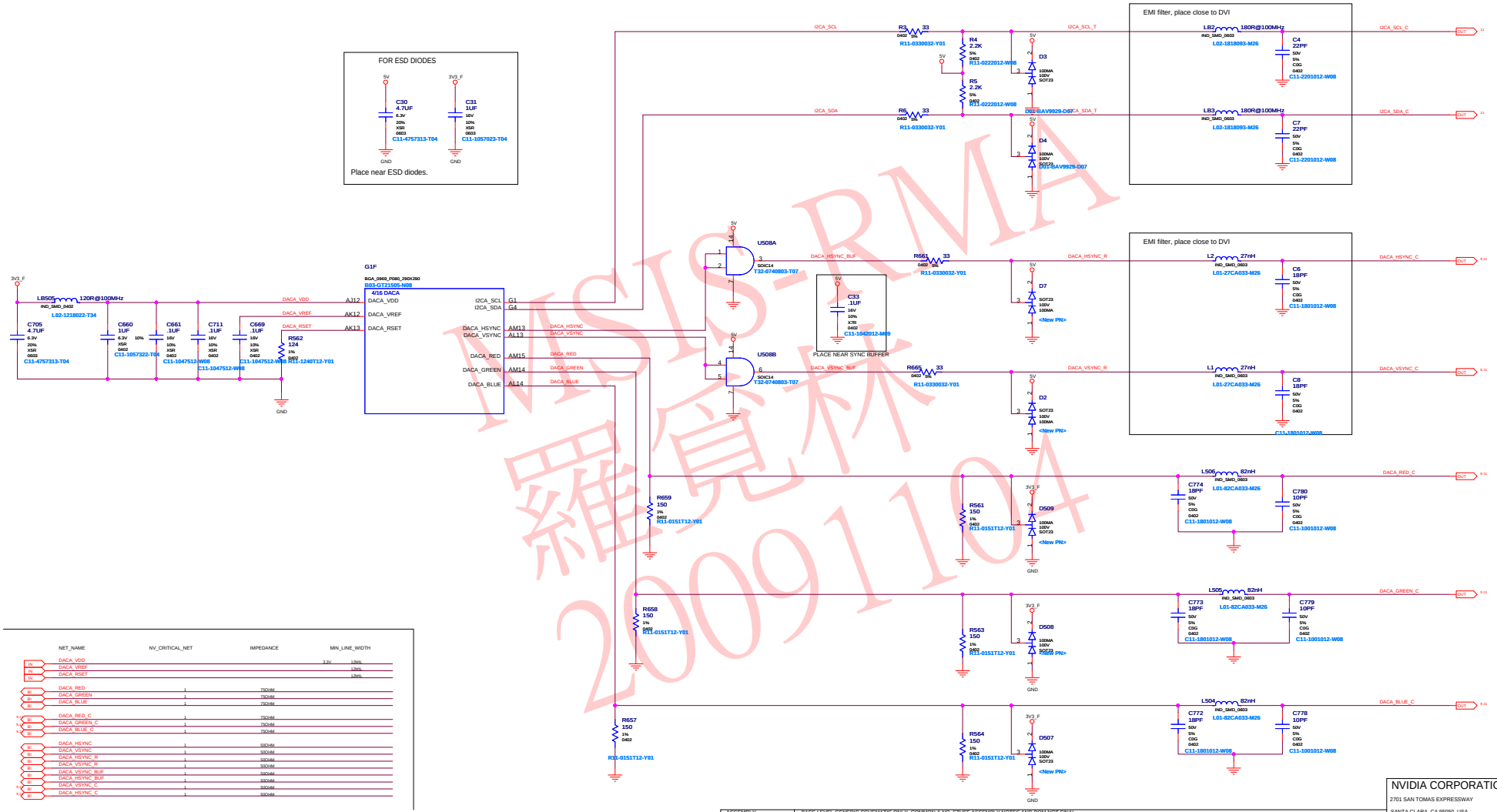
Primary Display (DACA), DVI-I (South)

DACA FILTER



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA (PRIMARY DVI-I)

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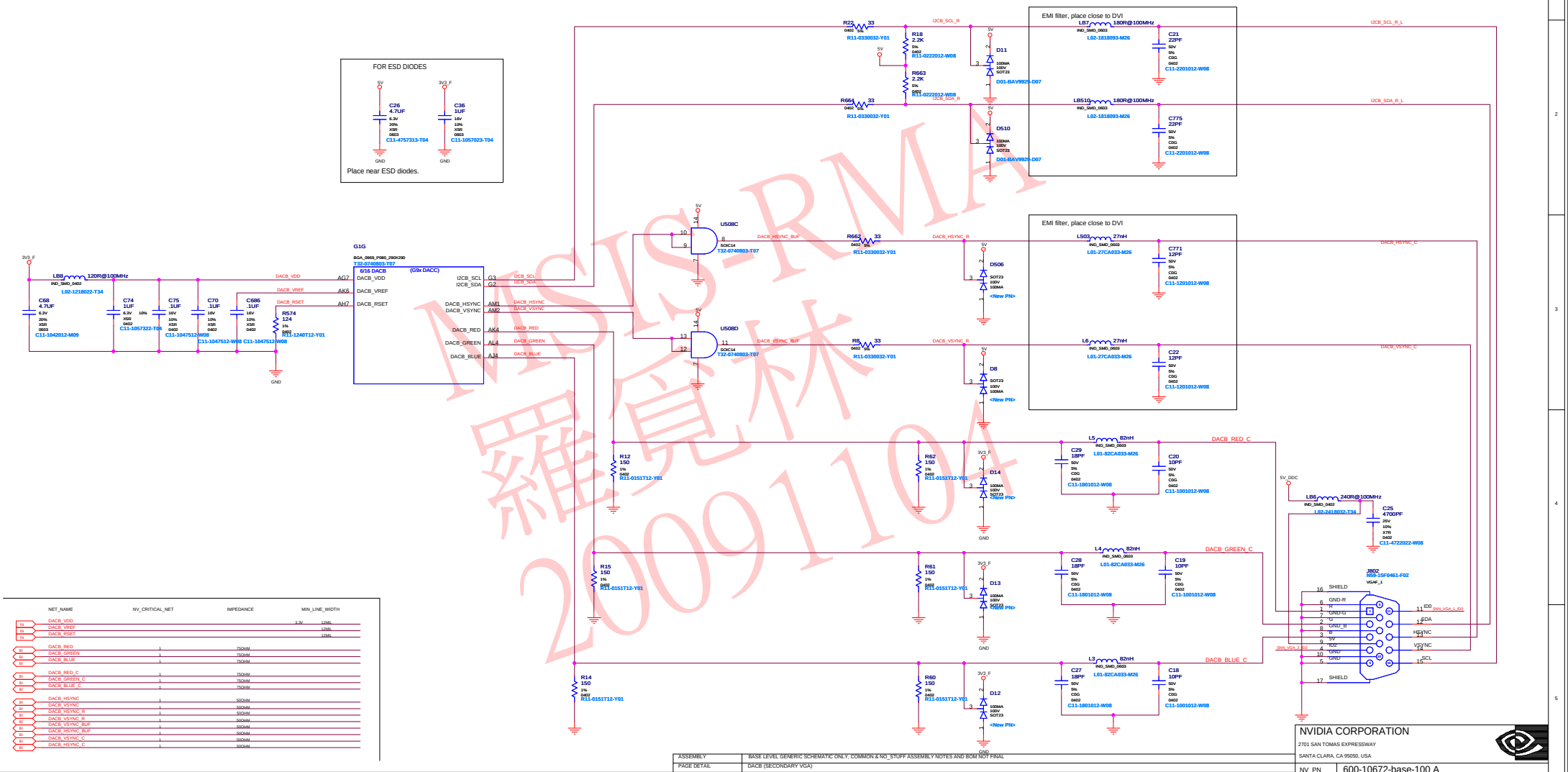
Secondary Display (DACB), VGA (Mid)

DACB FILTER



NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACB_VDD			3.3V 12MIL
DACB_VREF			12MIL
DACB_RSET			12MIL
DACB_RED	1	75OHM	
DACB_GREEN	1	75OHM	
DACB_BLUE	1	75OHM	
DACB_RED_C	1	75OHM	
DACB_GREEN_C	1	75OHM	
DACB_BLUE_C	1	75OHM	
DACB_HSYNC	1	50OHM	
DACB_VSYNC	1	50OHM	
DACB_HSYNC_R	1	50OHM	
DACB_VSYNC_R	1	50OHM	
DACB_VSYNC_BUF	1	50OHM	
DACB_HSYNC_BUF	1	50OHM	
DACB_VSYNC_C	1	50OHM	
DACB_HSYNC_C	1	50OHM	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB (SECONDARY VGA)

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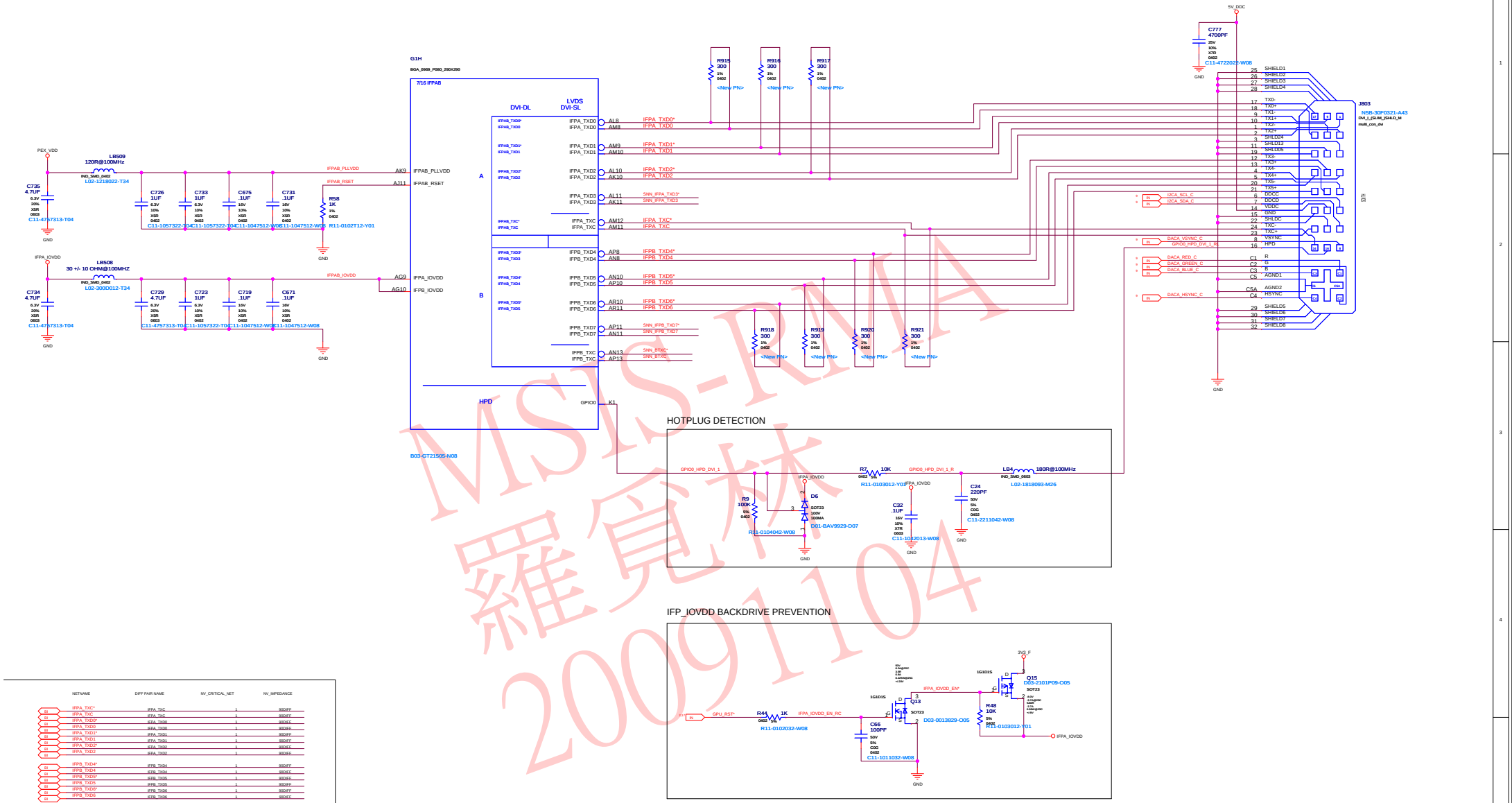
LINK A/B: TMDS, Primary DVI-I DL (South)



NETNAME	DIFF PAIR NAME	NV_CRITICAL_NET	NV_IMPEDANCE
IFPA_TXC*	IFPA_TXC	1	90DIFF
IFPA_TXC	IFPA_TXC	1	90DIFF
IFPA_TXD0*	IFPA_TXD0	1	90DIFF
IFPA_TXD0	IFPA_TXD0	1	90DIFF
IFPA_TXD1*	IFPA_TXD1	1	90DIFF
IFPA_TXD1	IFPA_TXD1	1	90DIFF
IFPA_TXD2*	IFPA_TXD2	1	90DIFF
IFPA_TXD2	IFPA_TXD2	1	90DIFF
IFPB_TXD4*	IFPB_TXD4	1	90DIFF
IFPB_TXD4	IFPB_TXD4	1	90DIFF
IFPB_TXD5*	IFPB_TXD5	1	90DIFF
IFPB_TXD5	IFPB_TXD5	1	90DIFF
IFPB_TXD6*	IFPB_TXD6	1	90DIFF
IFPB_TXD6	IFPB_TXD6	1	90DIFF
IFPAB_PLLVDD	12MIL		1.05V
IFPAB_IOVDD	12MIL		3.3V
IFPAB_RSET	12MIL		

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK A/B: DVI-I (SOUTH)

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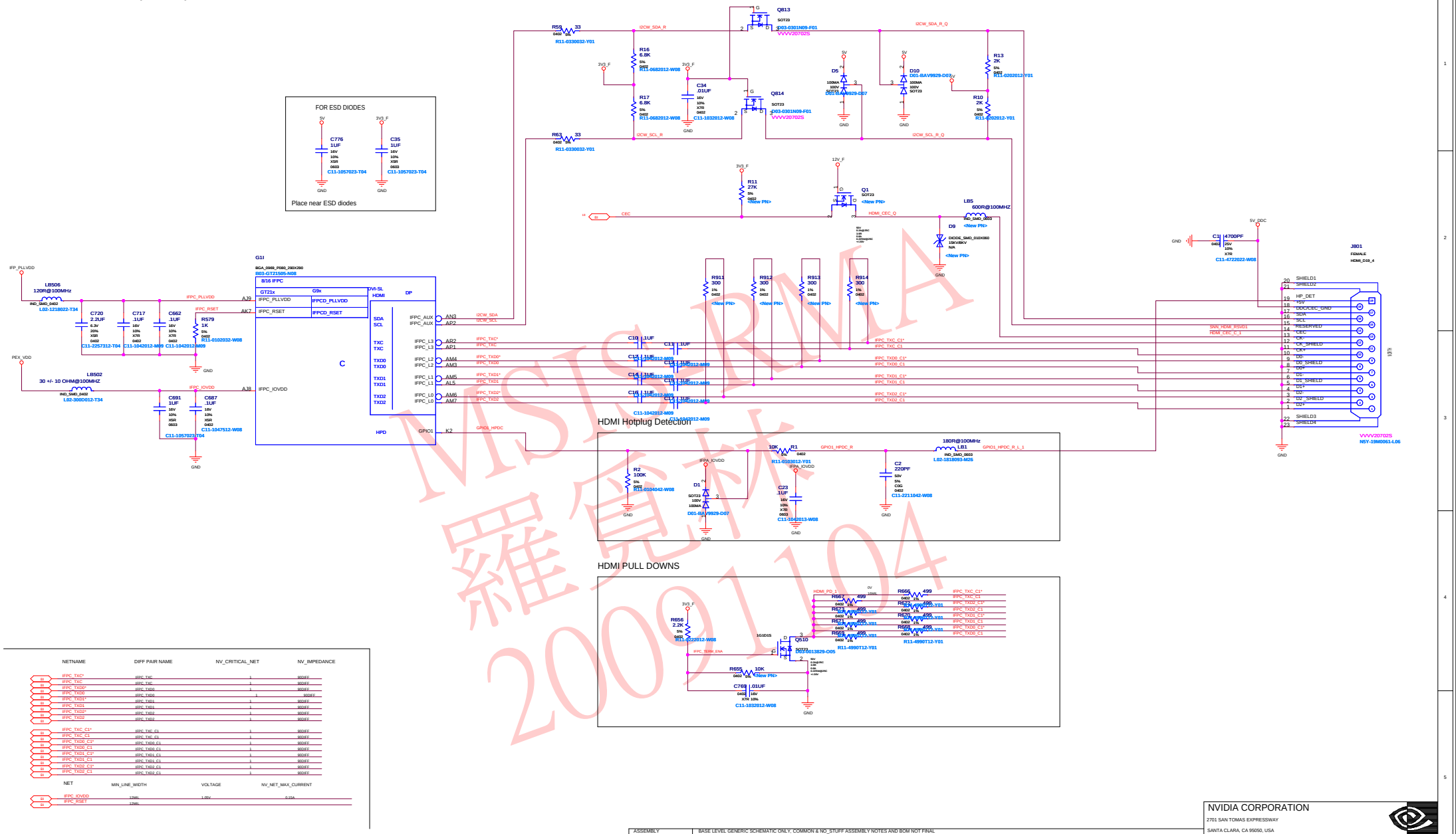
LINK C: HDMI (North)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK C: HDMI (NORTH)

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NV_PN	600-10672-base-100 A		
ID		PAGE	
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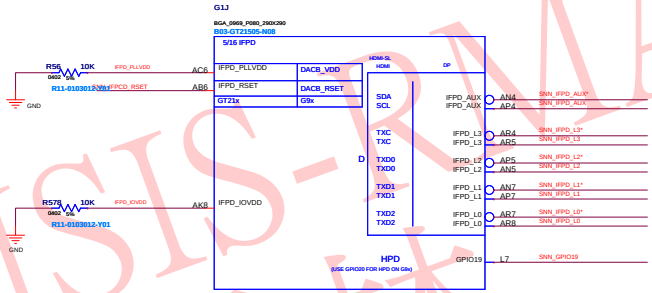
LINK D: UNUSED



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK D (UNUSED)

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NV_PN	600-10672-base-100 A		
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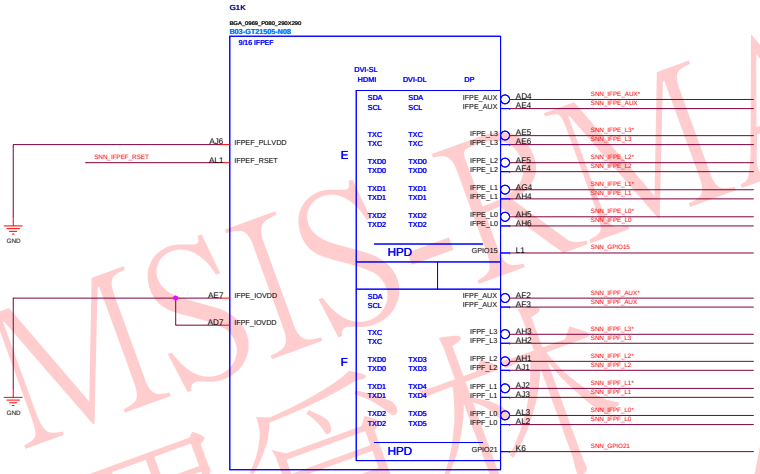
LINK E/F: (UNUSED)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK E/F: (UNUSED)

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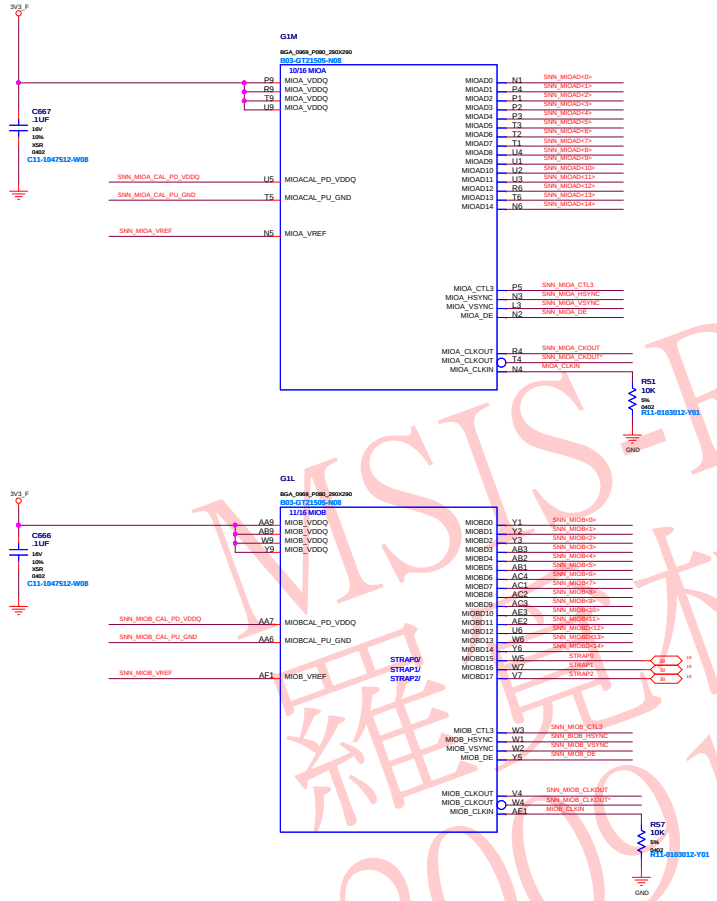
NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

MIOA/B UNUSED



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB (UNUSED)

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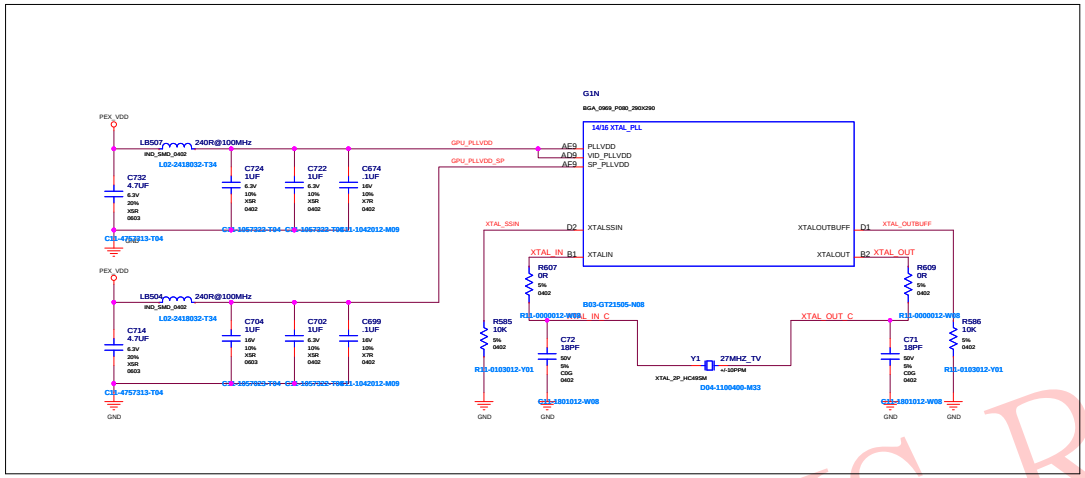
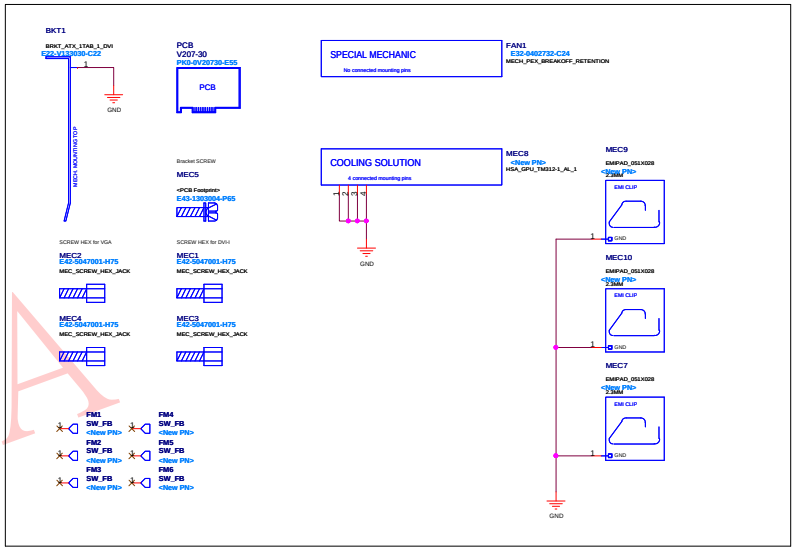
NAME		DATE	01-JUL-2009

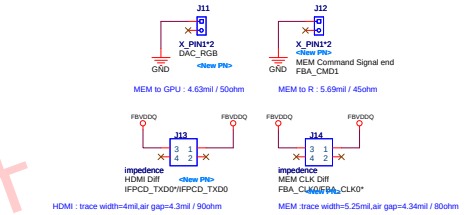
XTAL, MECHANICALS

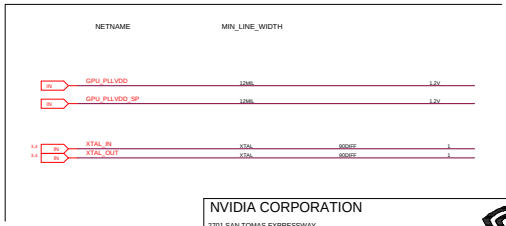
XTAL/GPU_PLLVDD



MECHANICALS & THERMALS







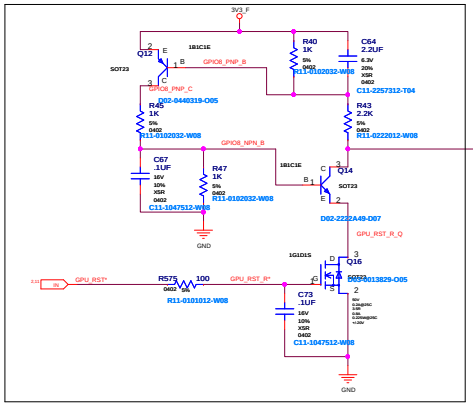
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, MECHANICALS, THERMALS

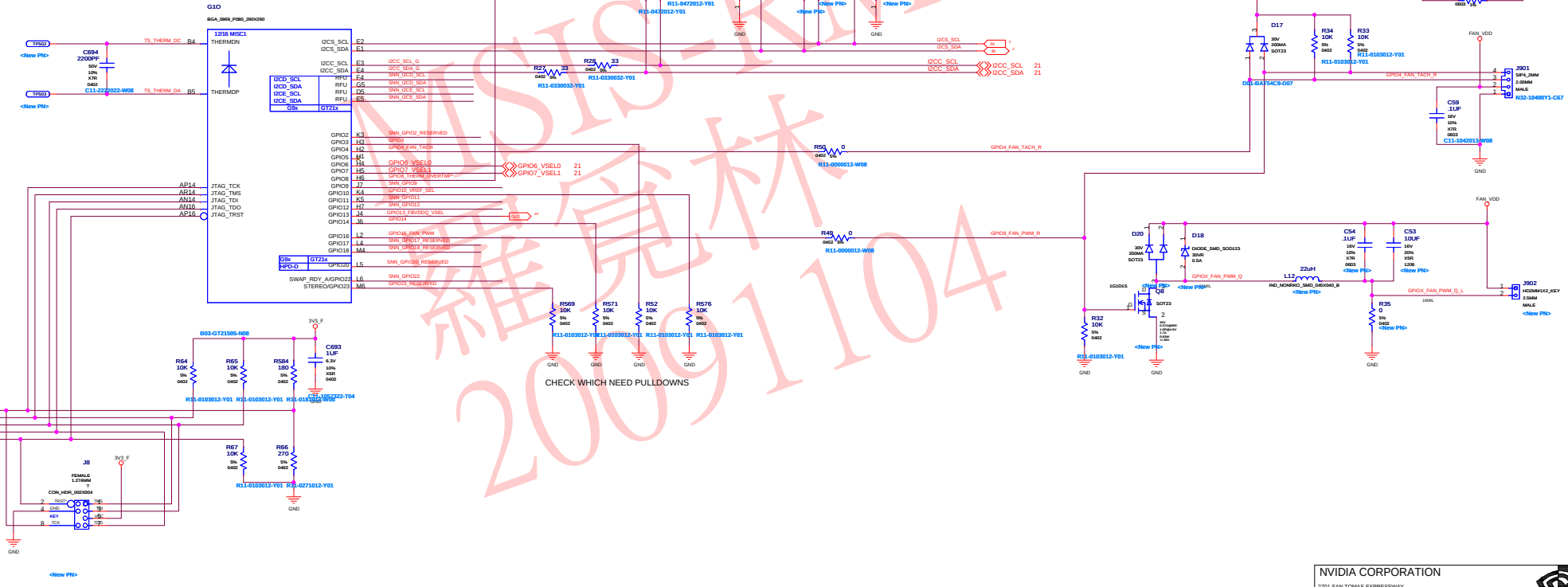
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

THERM ALERT, FAN CONTROL, GPIO & JTAG

THERM ALERT LATCH





NETNAME	MIN_LINE_WIDTH	CURRENT
THERM_DC	10MIL	
THERM_DA	10MIL	
FAN_PWM	8MIL	
FAN_PWM_R	8MIL	
THERM_DA_R	10MIL	
THERM_DC_R	10MIL	
FAN_VDD	16MIL	1A

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FAN CONTROL, THERMAL ALERT, GPIO, JTAG

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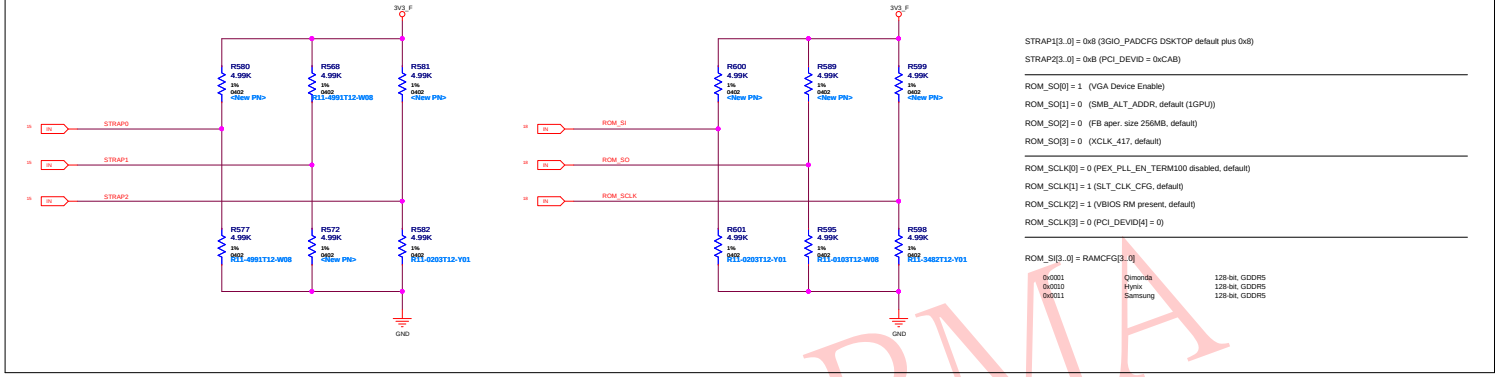
NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

STRAPPING, VBIOS, INFOROM

STRAPPING OPTIONS



STRAP1[3..0] = 0x8 (3GIO_PADCFG DSKTOP default plus 0x8)

STRAP2[3..0] = 0xB (PCI_DEVID = 0xCAB)

ROM_SO[0] = 1 (VGA Device Enable)

ROM_SO[1] = 0 (SMB_ALT_ADDR, default (1GPU))

ROM_SO[2] = 0 (FB aper. size 256MB, default)

ROM_SO[3] = 0 (XCLK_417, default)

ROM_SCLK[0] = 0 (PEX_PLL_EN_TERM100 disabled, default)

ROM_SCLK[1] = 1 (SLT_CLK_CFG, default)

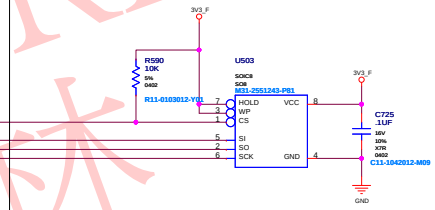
ROM_SCLK[2] = 1 (VBIOS RM present, default)

ROM_SCLK[3] = 0 (PCI_DEVID[4] = 0)

ROM_SI[3..0] = RAMCFG[3..0]

0x0001	Qimonda	128-bit, GDDR5
0x0010	Hynix	128-bit, GDDR5
0x0011	Samsung	128-bit, GDDR5

BIOS ROM(serial)



	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION STRAP MODE:	40.2k 1% TO GND	NC
	B83-GT21505-N08	
BINARY BRINGUP STRAP MODE:	NC	NC
MULTI-LEVEL STRAP MODE:	40.2k 1% TO GND	40.2k 1% TO GND

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	VBIOS ROM, INFOROM, STRAPPING OPTIONS

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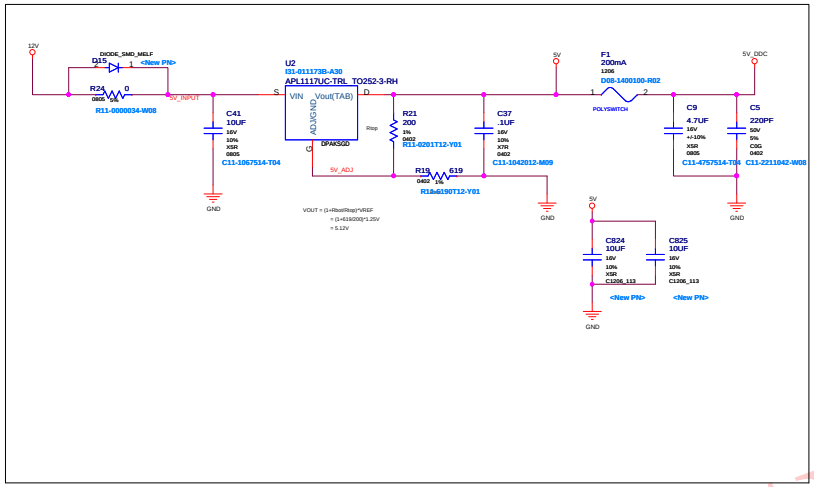
NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

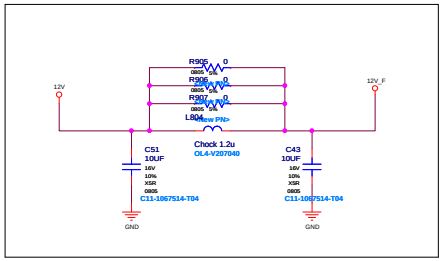
POWER SUPPLY: 5V, 5V_DDC, 1V8, INPUT FILTER

5V REGULATOR

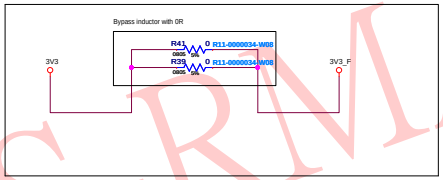


5V DDC

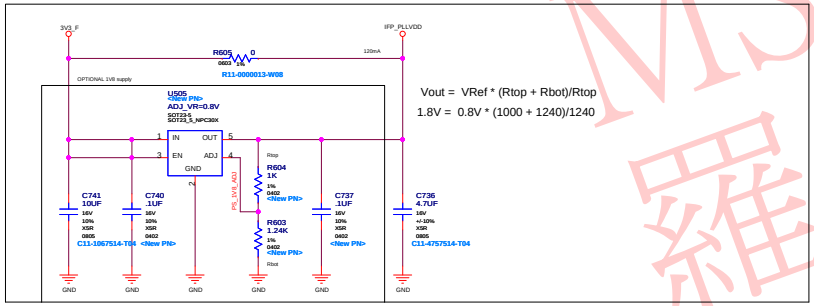
12V filter



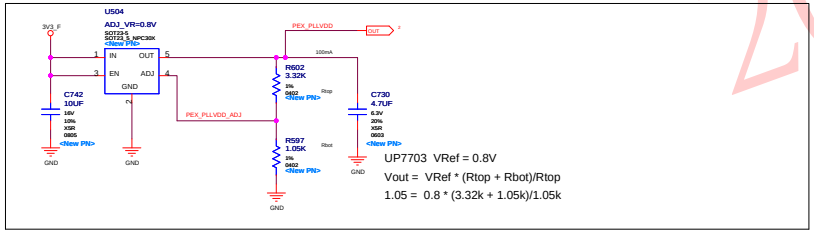
3.3V filter



IFPCEF PLLVDD supply



PEX_PLLVDD (optional)



NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	0.1A	12MIL	5V
5V_INPUT	0.2A	12MIL	5V
PS_1V8_ADJ		10MIL	1.8V
IFPA_IOVDD	0.3A	12MIL	3.2V
12V	6A	20MIL	12V
3V3	3A	12MIL	3.2V
3V3_F	4A	20MIL	3.3V
5V	0.3A	12MIL	5V
5V_DDC	0.1A	12MIL	5V
GND		10MIL	0V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	5V, DDC5V, IFP PLLVDD, IFP IOVDD, 3V3 FILTER, 12V FILTER

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NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

POWER SUPPLY: FBVDDQ, PEX_VDD

FBVDDQ Power Supply 1.35-1.50V@15A

Irms = 5.3A @ 1.5V / 15A (1.0uH)

FBVDDQ = 1.5V / 15A

30A

PEXVDD LINEAR

optional bypass

PEXVDD GATING

GPIO13	
FBVDDQ = 1.35V	0
FBVDDQ = 1.55V	1

FBVDDQ = VREF * (1 + (Rtop / Rbot))
1.358V = 0.8V * (1 + (698 / 1K))

FBVDDQ = VREF * (1 + (Rtop / Rbot ll Rbot1))
1.548V = 0.8V * (1 + (698 / (1K ll 2.94K))

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
NVVDD	20MIL	1.0V	40A
FBVDDQ	20MIL	1.5V	15A
PEX_VDD	20MIL	1.05V	3A

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBVDDQ SINGLE PHASE SWITCHER; PEX_VDD LINEAR

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NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

Title: Basenet Report
Design: design
Date: Jun 9 10:09:58 2009

Base nets and synonyms for
design_lib.DESIGN(@design_lib.design(sch
_1))
Base Signal Location([Zone][dir])

3V3 19.1G
3V3_F 19.1G
3V3_INFOROM 18.4F
3V3_PEX_SVDD 2.5G
3V3_PRSNT 21.2A
5V 19.1G
5V_ADJ 19.2B
5V_DDC 19.1G
5V_DDC_VGA 10.3G
5V_FUSED 19.1G
5V_INPUT 19.1A 19.1G
5V_PHASE 19.2B
12V 19.1G
12V_F 19.1G
12V_PRSNT 21.2A
CEC 12.2D 18.4B
CEC_GT216 18.4B
DACA_BLUE 9.3C 9.5A
DACA_BLUE_C 9.5A 9.5H 11.2G
DACA_GREEN 9.3C 9.5A
DACA_GREEN_C 9.4H 9.5A 11.2G
DACA_HSYNC 9.3C 9.5A
DACA_HSYNC_BUF 9.3D 9.5A
DACA_HSYNC_C 9.3H 9.5A 11.2G
DACA_HSYNC_R 9.3F 9.5A
DACA_RED 9.3C 9.5A
DACA_RED_C 9.4H 9.5A 11.2G
DACA_RSET 9.3B 9.5A
DACA_VDD 9.3B 9.5A
DACA_VREF 9.3B 9.5A
DACA_VSYNC 9.3C 9.5A
DACA_VSYNC_BUF 9.3D 9.5A
DACA_VSYNC_C 9.3H 9.5A 11.2G
DACA_VSYNC_R 9.3F 9.5A
DACB_BLUE 10.3C 10.5A
DACB_BLUE_C 10.5A 10.5G
DACB_GREEN 10.3C 10.5A
DACB_GREEN_C 10.4G 10.5A
DACB_HSYNC 10.3C 10.5A
DACB_HSYNC_BUF 10.3D 10.5A
DACB_HSYNC_C 10.3H 10.5A
DACB_HSYNC_R 10.3E 10.5A
DACB_RED 10.3C 10.5A
DACB_RED_C 10.4G 10.5A
DACB_RSET 10.3B 10.5A
DACB_VDD 10.3B 10.5A
DACB_VREF 10.3B 10.5A
DACB_VSYNC 10.3C 10.5A
DACB_VSYNC_BUF 10.3D 10.5A
DACB_VSYNC_C 10.3H 10.5A
DACB_VSYNC_R 10.3E 10.5A
FAN_PWM 17.1G
FAN_PWM_R 17.1G
FAN_VDD 17.1G
FBA_CLK0 3.4D 4.1F 4.2A
FBA_CLK0* 3.4D 4.1F 4.2A
FBA_CLK0_TERM 4.2B 4.2F
FBA_CLK1 3.4D 4.1F 4.2D
FBA_CLK1* 3.4D 4.1F 4.2D
FBA_CLK1_TERM 4.2E 4.2F
FBA_CMD<0> 3.3C 4.1B
FBA_CMD<30..0> 3.3D 4.1A 4.1D 4.1F
FBA_CMD<1> 3.3C 4.1B
FBA_CMD<2> 3.3C 4.1B
FBA_CMD<3> 3.3C 4.1E
FBA_CMD<4> 3.3C 4.1E
FBA_CMD<5> 3.3C 4.1E
FBA_CMD<6> 3.3C 4.2E 4.2G
FBA_CMD<7> 3.3C 4.1B
FBA_CMD<8> 3.3C 4.2B 4.2E 4.2G
FBA_CMD<9> 3.3C 4.1B
FBA_CMD<10> 3.3C 4.1B
FBA_CMD<11> 3.3C 4.1E
FBA_CMD<12> 3.3C 4.1E
FBA_CMD<13> 3.3C 4.1E
FBA_CMD<14> 3.3C 4.1B
FBA_CMD<15> 3.3C 4.1E
FBA_CMD<16> 3.3C 4.1E
FBA_CMD<17> 3.3C 4.1E
FBA_CMD<18> 3.3C 4.1B
FBA_CMD<19> 3.3C 4.1E
FBA_CMD<20> 3.3C 4.2B 4.2G
FBA_CMD<21> 3.3C 4.1E
FBA_CMD<22> 3.3C 4.1B
FBA_CMD<23> 3.3C 4.1B
FBA_CMD<24> 3.3C 4.1B
FBA_CMD<25> 3.3C 4.1B

FBA_CMD<26> 3.4C 4.1B
FBA_CMD<27> 3.4C 4.1E
FBA_CMD<28> 3.4C 4.1E
FBA_CMD<29> 3.4C 4.1B
FBA_CMD<30> 3.4C 4.1E
FBA_D<0> 3.1B 4.4B
FBA_D<63..0> 3.1A 4.1F 4.4A
FBA_D<1> 3.1B 4.4B
FBA_D<2> 3.1B 4.4B
FBA_D<3> 3.1B 4.4B
FBA_D<4> 3.1B 4.4B
FBA_D<5> 3.1B 4.4B
FBA_D<6> 3.1B 4.4B
FBA_D<7> 3.1B 4.4B
FBA_D<8> 3.1B 4.4B
FBA_D<9> 3.1B 4.4B
FBA_D<10> 3.1B 4.4B
FBA_D<11> 3.1B 4.5B
FBA_D<12> 3.1B 4.5B
FBA_D<13> 3.1B 4.5B
FBA_D<14> 3.1B 4.5B
FBA_D<15> 3.2B 4.5B
FBA_D<16> 3.2B 4.4C
FBA_D<17> 3.2B 4.4C
FBA_D<18> 3.2B 4.4C
FBA_D<19> 3.2B 4.4C
FBA_D<20> 3.2B 4.4C
FBA_D<21> 3.2B 4.4C
FBA_D<22> 3.2B 4.4C
FBA_D<23> 3.2B 4.4C
FBA_D<24> 3.2B 4.4C
FBA_D<25> 3.2B 4.4C
FBA_D<26> 3.2B 4.4C
FBA_D<27> 3.2B 4.5C
FBA_D<28> 3.2B 4.5C
FBA_D<29> 3.2B 4.5C
FBA_D<30> 3.2B 4.5C
FBA_D<31> 3.2B 4.5C
FBA_D<32> 3.2B 4.4D
FBA_D<33> 3.2B 4.4D
FBA_D<34> 3.2B 4.4D
FBA_D<35> 3.2B 4.4D
FBA_D<36> 3.2B 4.4D
FBA_D<37> 3.2B 4.4D
FBA_D<38> 3.2B 4.4D
FBA_D<39> 3.2B 4.4D
FBA_D<40> 3.2B 4.4D
FBA_D<41> 3.2B 4.4D
FBA_D<42> 3.2B 4.4D
FBA_D<43> 3.2B 4.5D
FBA_D<44> 3.2B 4.5D
FBA_D<45> 3.3B 4.5D
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FBA_D<58> 3.3B
FBA_D<59> 3.3B
FBA_D<60> 3.3B
FBA_D<61> 3.3B
FBA_D<62> 3.3B
FBA_D<63> 3.3B
FBA_DBI<0> 3.3B 4.4B
FBA_DBI<7..0> 3.3A 4.1F 4.4A
FBA_DBI<1> 3.3B 4.5B
FBA_DBI<2> 3.3B 4.4C
FBA_DBI<3> 3.3B 4.5C
FBA_DBI<4> 3.3B 4.4D
FBA_DBI<5> 3.3B 4.5D
FBA_DBI<6> 3.3B 4.4E
FBA_DBI<7> 3.3B 4.5E
FBA_DEBUG 3.4D
FBA_DEBUG_SEN0 4.3B
FBA_DEBUG_SEN1 4.3E
FBA_EDC<0> 3.4B 4.4B
FBA_EDC<7..0> 3.4A 4.1F 4.4A
FBA_EDC<1> 3.4B 4.5B
FBA_EDC<2> 3.4B 4.4C
FBA_EDC<3> 3.4B 4.5C
FBA_EDC<4> 3.4B 4.4D
FBA_EDC<5> 3.4B 4.5D
FBA_EDC<6> 3.4B 4.4E
FBA_EDC<7> 3.4B 4.5E
FBA_VREF 3.1F
FBA_VREFC0 4.1F 4.2B
FBA_VREFC1 4.1F 4.2E
FBA_VREFD0 4.2F 4.4F
FBA_VREFD1 4.2F 4.4F

FBA_VREF_PROBE 3.5B
FBA_WCK01 3.4A 4.1F 4.5A
FBA_WCK01* 3.4A 4.1F 4.5A
FBA_WCK01_CT 4.2F 4.5B
FBA_WCK23 3.4A 4.1F 4.5C
FBA_WCK23* 3.4A 4.1F 4.5C
FBA_WCK23_CT 4.2F 4.5C
FBA_WCK45 3.4A 4.1F 4.5D
FBA_WCK45* 3.4A 4.1F 4.5D
FBA_WCK45_CT 4.2F 4.5D
FBA_WCK67 3.4A 4.1F 4.5E
FBA_WCK67* 3.4A 4.1F 4.5E
FBA_WCK67_CT 4.2F 4.5E
FBA_ZQ0 4.2B
FBA_ZQ1 4.2E
FBC_CLK0 6.4D 7.1G 7.2A
FBC_CLK0* 6.4D 7.1G 7.2A
FBC_CLK0_TERM 7.2B 7.2G
FBC_CLK1 6.4D 7.1G 7.2D
FBC_CLK1* 6.4D 7.1G 7.2D
FBC_CLK1_TERM 7.2E 7.2G
FBC_CMD<0> 6.3C 7.1B
FBC_CMD<30..0> 6.3D 7.1A 7.1D 7.1G
FBC_CMD<1> 6.3C 7.1B
FBC_CMD<2> 6.3C 7.1B
FBC_CMD<3> 6.3C 7.1E
FBC_CMD<4> 6.3C 7.1E
FBC_CMD<5> 6.3C 7.1E
FBC_CMD<6> 6.3C 7.2E 7.2G
FBC_CMD<7> 6.3C 7.1B
FBC_CMD<8> 6.3C 7.2B 7.2E 7.2G
FBC_CMD<9> 6.3C 7.1B
FBC_CMD<10> 6.3C 7.1B
FBC_CMD<11> 6.3C 7.1E
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FBC_CMD<14> 6.3C 7.1B
FBC_CMD<15> 6.3C 7.1E
FBC_CMD<16> 6.3C 7.1E
FBC_CMD<17> 6.3C 7.1E
FBC_CMD<18> 6.3C 7.1B
FBC_CMD<19> 6.3C 7.1E
FBC_CMD<20> 6.3C 7.2B 7.2G
FBC_CMD<21> 6.3C 7.1E
FBC_CMD<22> 6.3C 7.1B
FBC_CMD<23> 6.4C 7.1B
FBC_CMD<24> 6.4C 7.1B
FBC_CMD<25> 6.4C 7.1B
FBC_CMD<26> 6.4C 7.1B
FBC_CMD<27> 6.4C 7.1E
FBC_CMD<28> 6.4C 7.1E
FBC_CMD<29> 6.4C 7.1B
FBC_CMD<30> 6.4C 7.1E
FBC_D<0> 6.1A 7.4B
FBC_D<63..0> 6.1A 7.1G 7.4A
FBC_D<1> 6.1A 7.4B
FBC_D<2> 6.1A 7.4B
FBC_D<3> 6.1A 7.4B
FBC_D<4> 6.1A 7.4B
FBC_D<5> 6.1A 7.4B
FBC_D<6> 6.1A 7.4B
FBC_D<7> 6.1A 7.4B
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FBC_D<9> 6.1A 7.4B
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FBC_D<12> 6.1A 7.5B
FBC_D<13> 6.1A 7.5B
FBC_D<14> 6.1A 7.5B
FBC_D<15> 6.2A 7.5B
FBC_D<16> 6.2A 7.4C
FBC_D<17> 6.2A 7.4C
FBC_D<18> 6.2A 7.4C
FBC_D<19> 6.2A 7.4C
FBC_D<20> 6.2A 7.4C
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FBC_D<22> 6.2A 7.4C
FBC_D<23> 6.2A 7.4C
FBC_D<24> 6.2A 7.4C
FBC_D<25> 6.2A 7.4C
FBC_D<26> 6.2A 7.4C
FBC_D<27> 6.2A 7.4C
FBC_D<28> 6.2A 7.5C
FBC_D<29> 6.2A 7.5C
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FBC_D<31> 6.2A 7.5C
FBC_D<32> 6.2A 7.4D
FBC_D<33> 6.2A 7.4D
FBC_D<34> 6.2A 7.4D
FBC_D<35> 6.2A 7.4D
FBC_D<36> 6.2A 7.4D
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FBC_D<40> 6.2A 7.4D
FBC_D<41> 6.2A 7.4D

FBC_D<42> 6.2A 7.4D
FBC_D<43> 6.2A 7.4D
FBC_D<44> 6.2A 7.5D
FBC_D<45> 6.3A 7.5D
FBC_D<46> 6.3A 7.5D
FBC_D<47> 6.3A 7.5D
FBC_D<48> 6.3A
FBC_D<49> 6.3A
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FBC_D<51> 6.3A
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FBC_D<54> 6.3A
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FBC_D<60> 6.3A
FBC_D<61> 6.3A
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FBC_DEBUG_SEN1 7.3E
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FBC_WCK01* 6.4A 7.1G 7.5A
FBC_WCK01_CT 7.2G 7.5B
FBC_WCK23 6.4A 7.1G 7.5C
FBC_WCK23* 6.4A 7.1G 7.5C
FBC_WCK23_CT 7.2G 7.5C
FBC_WCK45 6.4A 7.1G 7.5D
FBC_WCK45* 6.4A 7.1G 7.5D
FBC_WCK45_CT 7.2G 7.5D
FBC_WCK67 6.4A 7.1G 7.5E
FBC_WCK67* 6.5A 7.1G 7.5E
FBC_WCK67_CT 7.2G 7.5F
FBC_ZQ0 7.2B
FBC_ZQ1 7.3E
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FB_CAL_PD_VDDQ 6.5C
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FB_CAL_PU_GND 6.5C
FB_CAL_TERM 6.1G
FB_CAL_TERM_GND 6.5C
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GPIO0_HPD_DVI_1_R 11.3E
GPIO0_HPD_DVI_1_RL 11.2G
GPIO1_HPDC 12.3C
GPIO1_HPDC_R 12.3E
GPIO1_HPDC_R_L_1 12.3F
GPIO3 17.3C
GPIO4_FAN_TACH 17.3C
GPIO4_FAN_TACH_R 17.3F 17.3H
GPIO5_VSEL0 17.3D 21.1A
GPIO5_VSEL_R 21.1A
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GPIO6_VSEL1_R 21.4A
GPIO7_VSEL2 17.3D 21.3A
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GPIO8_PNP_C 17.1B
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GPIO16_FAN_PWM 17.4C
GPIO23_RESERVED 17.4C
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GPIOX_FAN_PWM_Q_L 17.4H
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GPU_PLLVDD_SP 16.1B 16.5G
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GPU_RST_R_Q 17.2B
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HDMI_CEC_Q 12.2E
HDMI_PD_1 12.4E
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IFPA_IOVDD_EN_RC 11.4E
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IFPA_TXD4* 11.2D 11.5A
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JTAG_TDO 2.1C 17.5A
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MIOA_VDDQ 15.1B
MIOB_CLKIN 15.4D
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NVVDD_CSP 21.4D

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ROM_SO 18.2D 18.3C 18.3C
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SNN_BTXC* 11.3D
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R1612 [7.2G]
R1613 [6.5D]
R1614 [2.5E]
R1615 [6.5D]
R1616 [6.5D]
R1617 [7.2H]
R1618 [2.2C]
R1619 [6.4D]
R1620 [9.4E]
R1621 [9.3B]
R1622 [7.2G]
R1623 [9.4E]
R1624 [9.5E]
R1625 [11.2B]
R1627 [18.4B]
R1628 [13.3C]
R1630 [12.3B]
R1631 [18.4B]
R1632 [13.2C]
R1633 [7.3B]
R1634 [10.4D]
R1635 [2.1C]
R1636 [17.4E]
R1637 [10.3B]
R1638 [10.5D]
R1639 [17.4D]
R1640 [2.1B]
R1641 [16.2D]
R1642 [10.4D]
R1644 [17.4D]
R1645 [17.3E]
R1646 [17.4D]
R1647 [16.2C]
R1648 [7.2B]
R1649 [7.2B]
R1650 [7.2B]
R1651 [19.5B]
R1652 [19.5B]
R1653 [17.1B]
R1655 [19.4B]
R1656 [17.4D]
R1657 [19.4B]
R1658 [17.2E]
R1659 [17.1B]
R1660 [17.2C]
R1661 [18.2B]
R1662 [19.3B]
R1663 [18.2C]
R1664 [17.1B]
R1665 [18.1C]
R1666 [18.1B]
R1667 [17.2B]
R1668 [18.1C]
R1669 [17.2E]
R1670 [18.2D]
R1671 [18.2C]
R1672 [18.1D]
R1673 [17.2B]
R1674 [11.5F]
R1675 [18.1E]
R1676 [18.2E]
R1677 [18.2E]
R1678 [18.1E]
R1679 [18.3E]
R1680 [2.1D]
R1681 [17.4B]
R1687 [12.1D]
R1688 [12.1D]
R1689 [12.1D]
R1690 [12.1D]
R1691 [10.5E]
R1692 [10.4E]
R1693 [10.4E]
R1700 [9.5D]
R1701 [9.4D]
R1702 [9.4D]
R1703 [12.4E]
R1704 [12.4D]
R1707 [12.1F]
R1708 [12.1F]
RP1 [2.1C 2.1C 2.1C 2.1C]
TP1501 [3.5B]
TP1502 [17.3A]
TP1503 [17.3A]
U1 [19.2B]
U8 [21.3D]
U502 [20.2C]
U507 [9.3D 9.3D]
U507 [10.3D 10.3D]
U1001 [12.1G]
U1003 [19.1B]
U1006 [18.4F]
U1504 [19.5A]
U1505 [19.4A]
U1506 [18.3E]
Y1001 [16.2C]
Y1002 [16.2C]

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	<edit here to insert page detail>

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NV_PN	600-10672-base-100 A		
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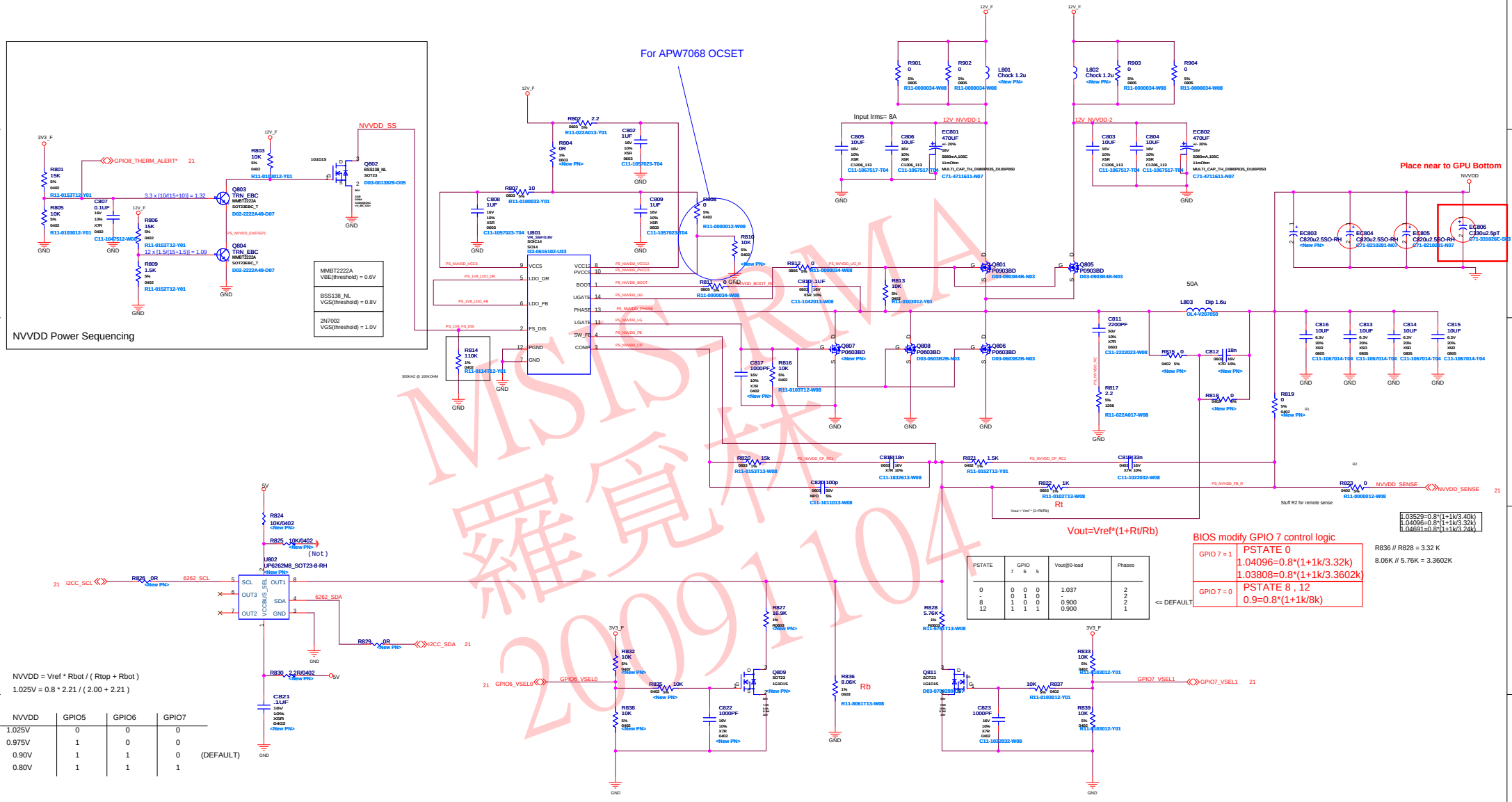
Power Supply III: NVVDD



PSTATE	GPIO 7 6 5	Vout@0-load	Phases
0	0 0 0	1.037	2
-	0 1 0	-	2
8	1 0 0	0.900	2
12	1 1 1	0.900	1

<= DEFAULT

NVVDD	GPIO5	GPIO6	GPIO7
1.025V	0	0	0
0.975V	1	0	0
0.90V	1	1	0
0.80V	1	1	1

(DEFAULT)

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	NVVDD POWER SUPPLY

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