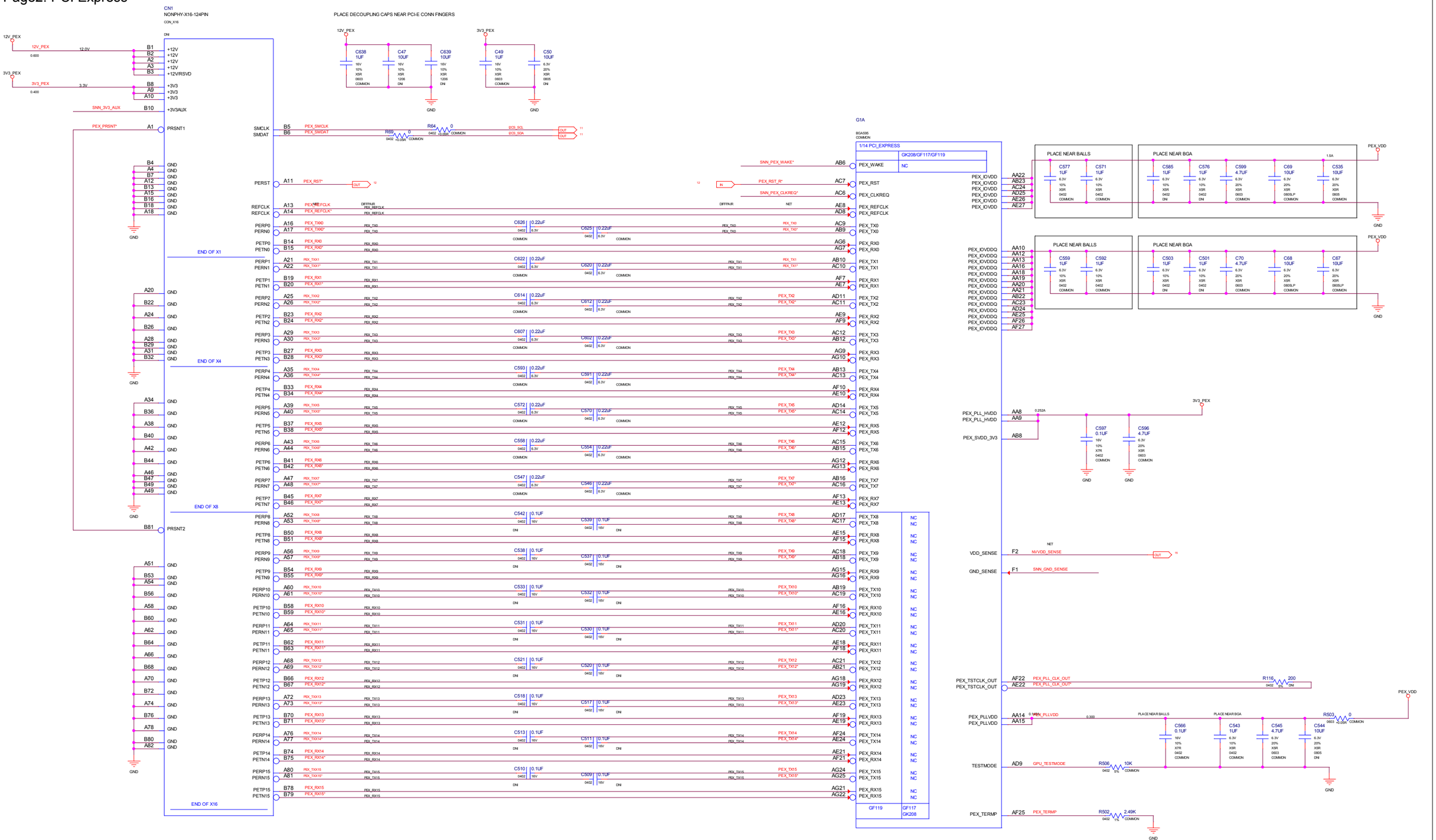
Page2: PCI Express



Page3: GPU MEMORY FBA

G1B

BGA595
COMMON

2/14 FBA

NC	FB_CLAMP
GF119	GF117/GK208

FB_PLLAVDD	FB_DLLAVDD
GF117	GF119/GK208

CMD	RANK0	RANK1		
	<31..0>	<63..32>	<31..0>	<63..32>
CMD0	ODT_L	NOT USED	ODT_L	NOT USED
CMD1	NOT USED	NOT USED	CS1_L*	NOT USED
CMD2	CS0_L*	NOT USED	NOT USED	NOT USED
CMD3	CKE_L	NOT USED	CKE_L	NOT USED
CMD4	A<9>	A<9>	A<11>	A<11>
CMD5	A<6>	A<6>	A<7>	A<7>
CMD6	A<3>	A<3>	BA1	BA1
CMD7	A<0>	A<0>	A<12>	A<12>
CMD8	A<8>	A<8>	A<8>	A<8>
CMD9	A<12>	A<12>	A<0>	A<0>
CMD10	A<1>	A<1>	A<2>	A<2>
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A<13>	A<13>	A<14>	A<14>
CMD13	BA1	BA1	A<3>	A<3>
CMD14	A<14>	A<14>	A<13>	A<13>
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16	NOT USED	NOT USED	ODT_H	NOT USED ODT_H
CMD17	NOT USED	NOT USED	NOT USED	NOT USED CS1_H*
CMD18	NOT USED	NOT USED	CS0_H*	NOT USED NOT USED
CMD19	NOT USED	NOT USED	CKE_H	NOT USED CKE_H
CMD20	RST	RST	RST	RST
CMD21	A<7>	A<7>	A<6>	A<6>
CMD22	A<4>	A<4>	A<5>	A<5>
CMD23	A<11>	A<11>	A<9>	A<9>
CMD24	A<2>	A<2>	A<1>	A<1>
CMD25	A<10>	WE*	WE*	
CMD26	A<5>	A<5>	A<4>	A<4>
CMD27	BA2	BA2	NOT USED	NOT USED
CMD28	WE*	WE*	A<10>	A<10>
CMD29	BA0	BA0	BA0	BA0
CMD30	NOT USED	NOT USED	BA2	BA2

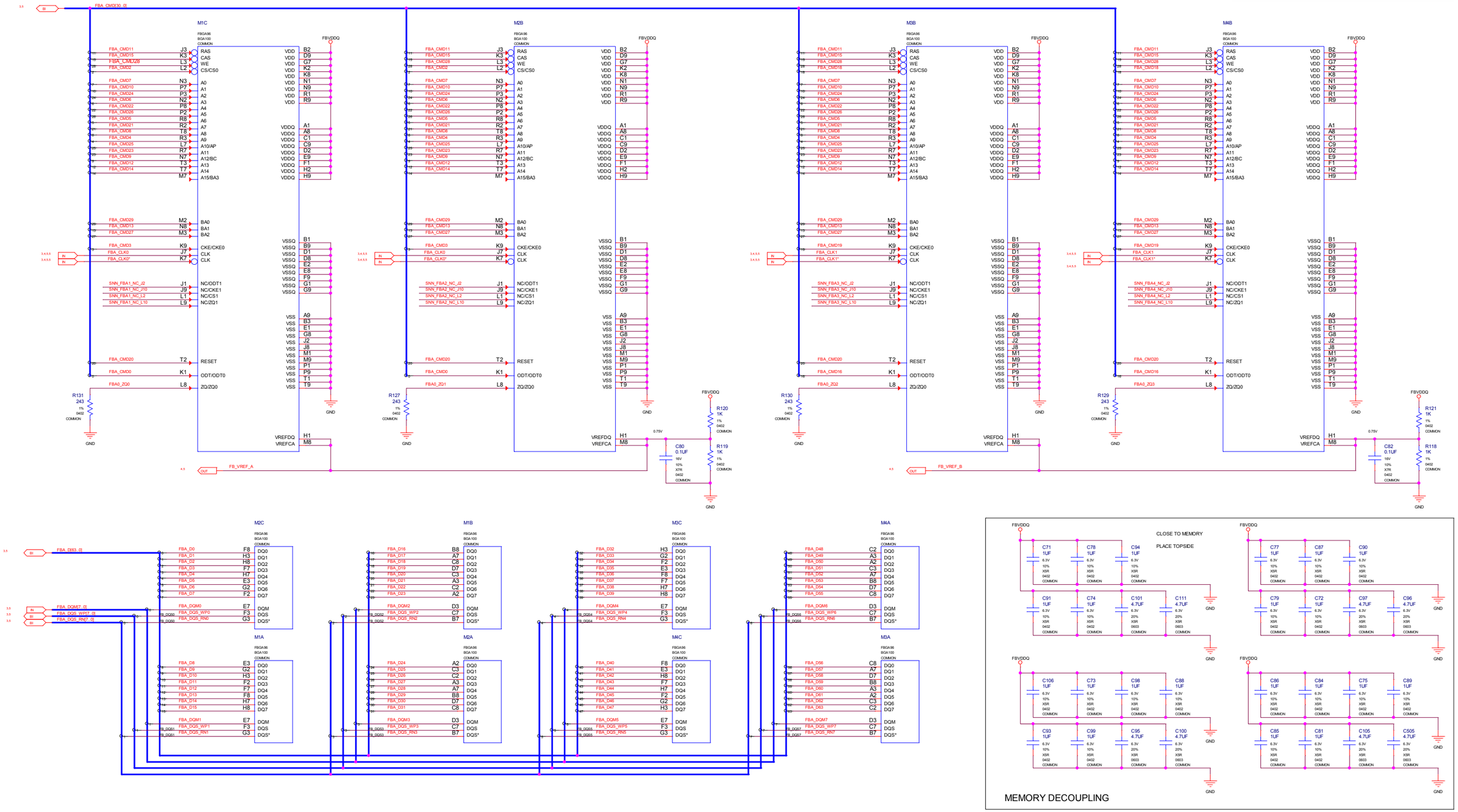
PD REQUIRED FOR INITIALIZATION

CLK TERMINATION

CMD TERMINATION

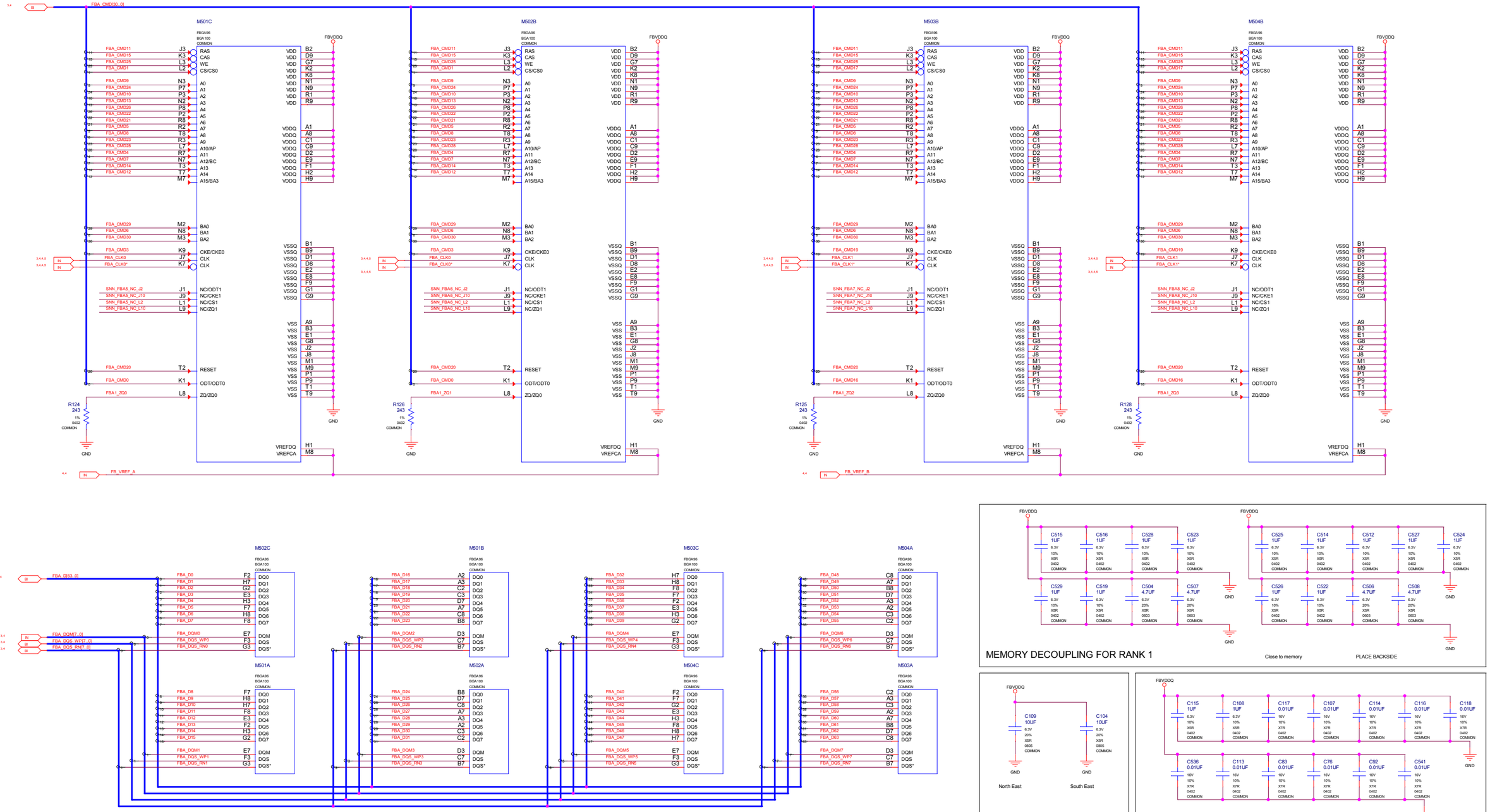
Page4: FBA DDR3 MEMORY RANK 0

Net Name	MIN_WIDTH
FB_VREF_A	0.300
FB_VREF_B	0.300

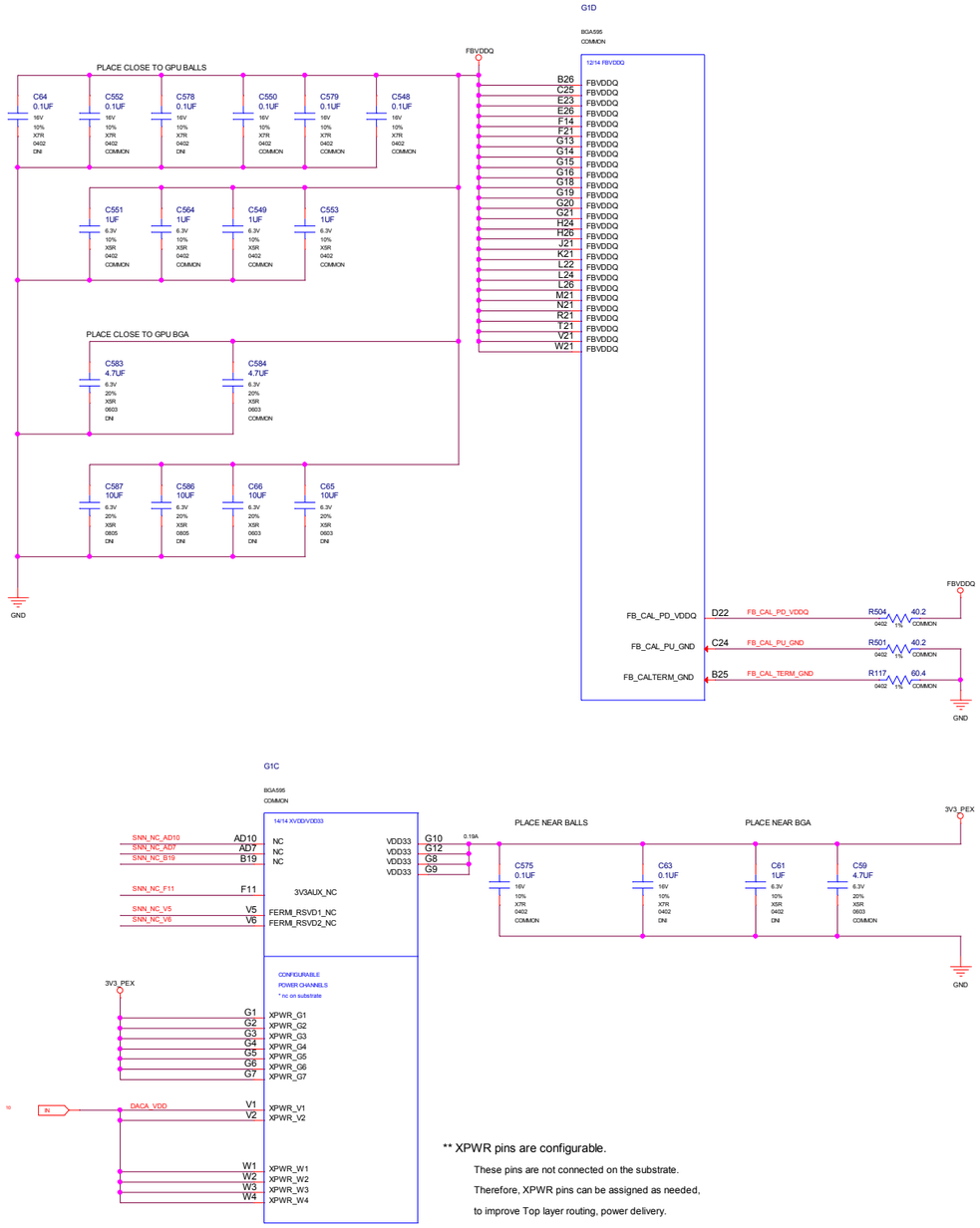


A

Page5: FBA DDR3 MEMORY RANK 1



Page6: POWER/DECOUPLING: NVVDD,FBVDDQ,VDD33,GND

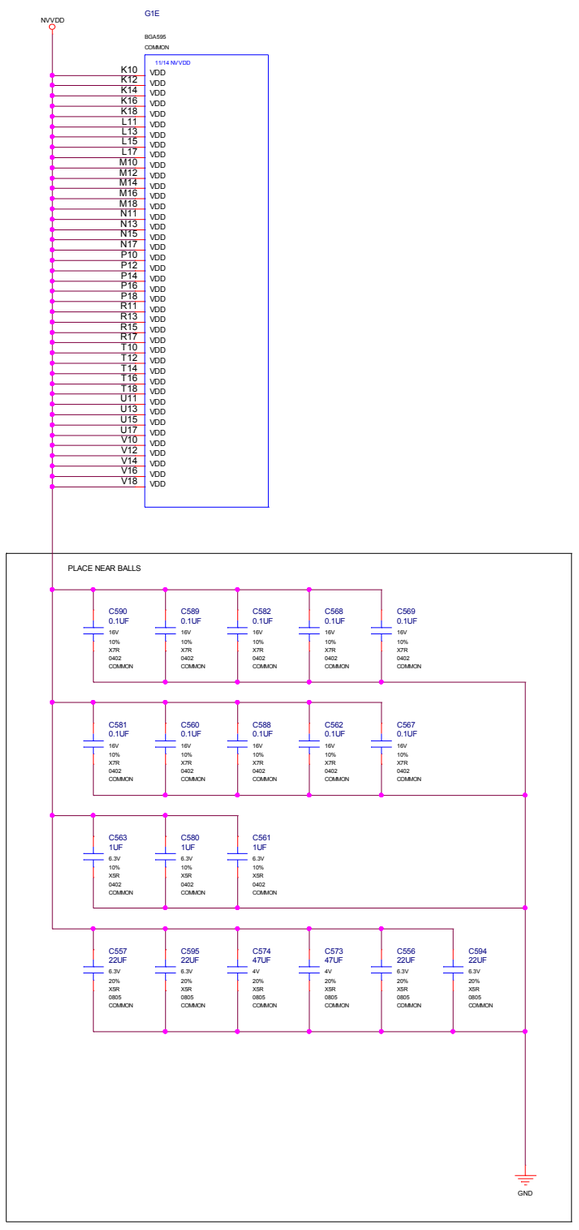


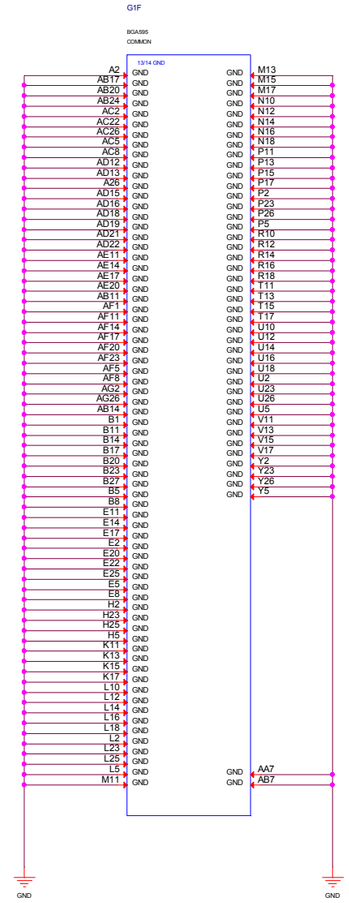
** XPWR pins are configurable.

These pins are not connected on the substrate.

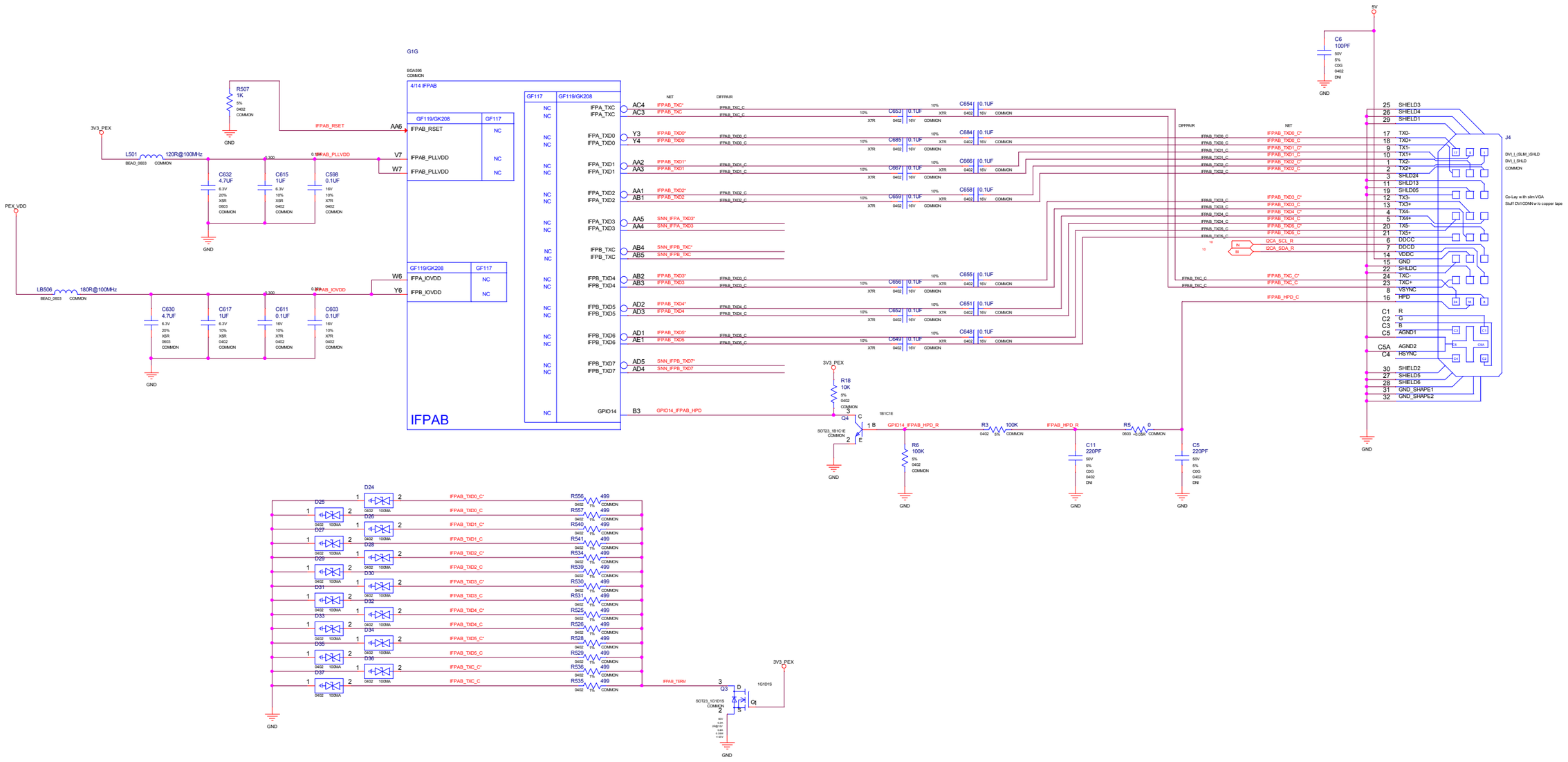
Therefore, XPWR pins can be assigned as needed,

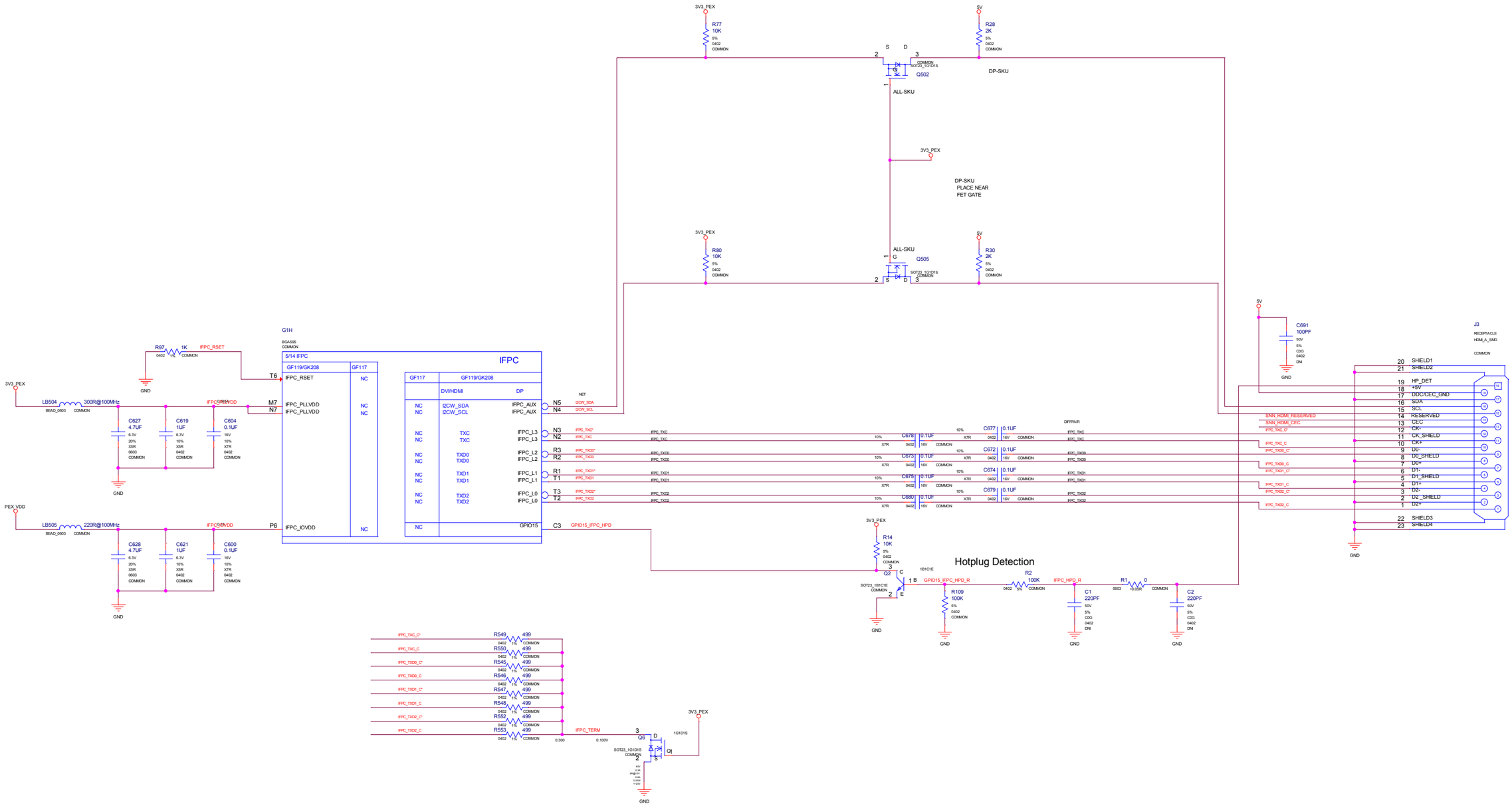
to improve Top layer routing, power delivery.



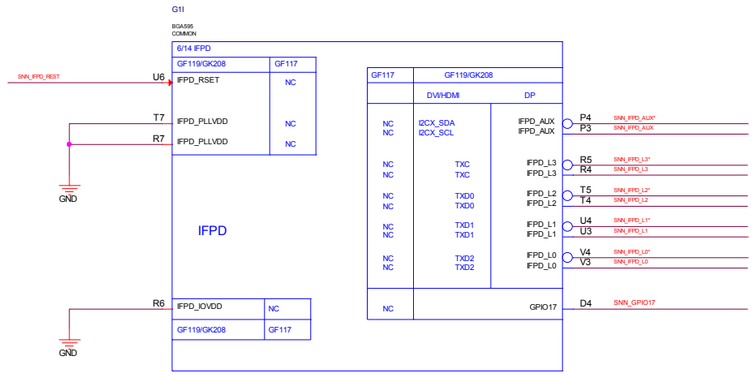


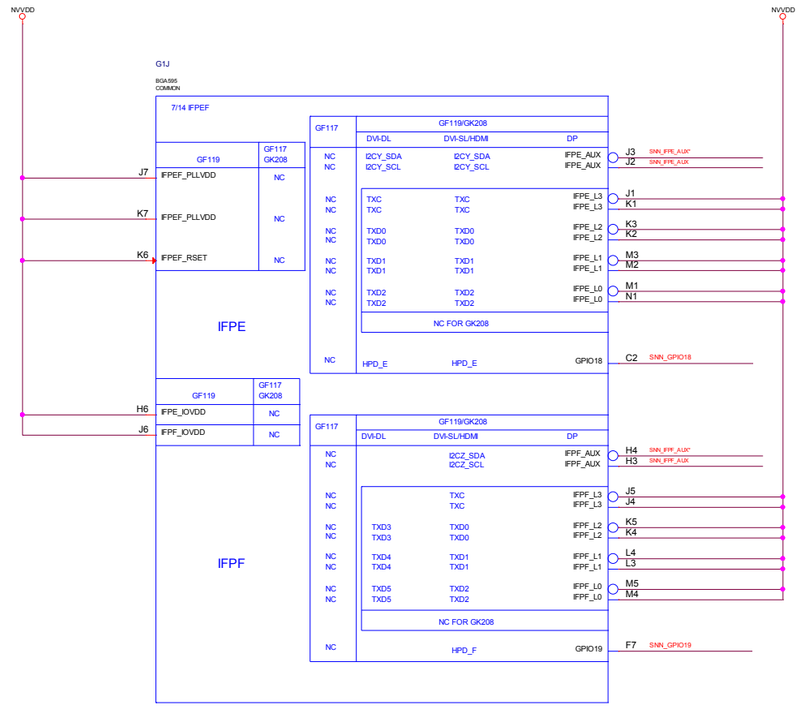
Page7: IFPAB TMDS DUAL LINK




IFPC
Hotplug Detection
DP-SKU
ALL-SKU
DP-SKU
PLACE NEAR
FET GATE
3V3_PEX
5V
GND
G1H
5/14 IFPC
GF119/GK208
GF117
DVI/HDMI
DP
IFPC_RSET
IFPC_PLLVDD
IFPC_IOVDD
IFPC_AUX
IFPC_L3
IFPC_L2
IFPC_L1
IFPC_L0
GPIO15_IFPC_HPD
I2CW_SDA
I2CW_SCL
TXC
TXD0
TXD1
TXD2
R77
10K
R28
2K
Q502
R80
10K
R30
2K
Q505
R97
1K
IFPC_RSET
LB504
300R@100MHz
LB505
220R@100MHz
C627
4.7UF
C619
1UF
C604
0.1UF
C628
4.7UF
C621
1UF
C600
0.1UF
C691
100PF
J3
RECEPTACLE
HDMI_A_SMD
SHIELD1
SHIELD2
HP_DET
+5V
DDC/CEC_GND
SDA
SCL
RESERVED
CEC
CK-
CK_SHIELD
CK+
D0-
D0_SHIELD
D0+
D1-
D1_SHIELD
D1+
D2-
D2_SHIELD
D2+
SHIELD3
SHIELD4
SNN_HDMI_RESERVED
SNN_HDMI_CEC
C677
C678
C673
C675
C680
C672
C674
C679
0.1UF
R14
10K
Q2
R109
100K
R2
100K
R1
0
C1
220PF
C2
220PF
R549
R550
R545
R546
R547
R548
R562
R553
499
IFPC_TERM
0.300
0.100V
Q6
Q1
1G1D1S
1B1C1E

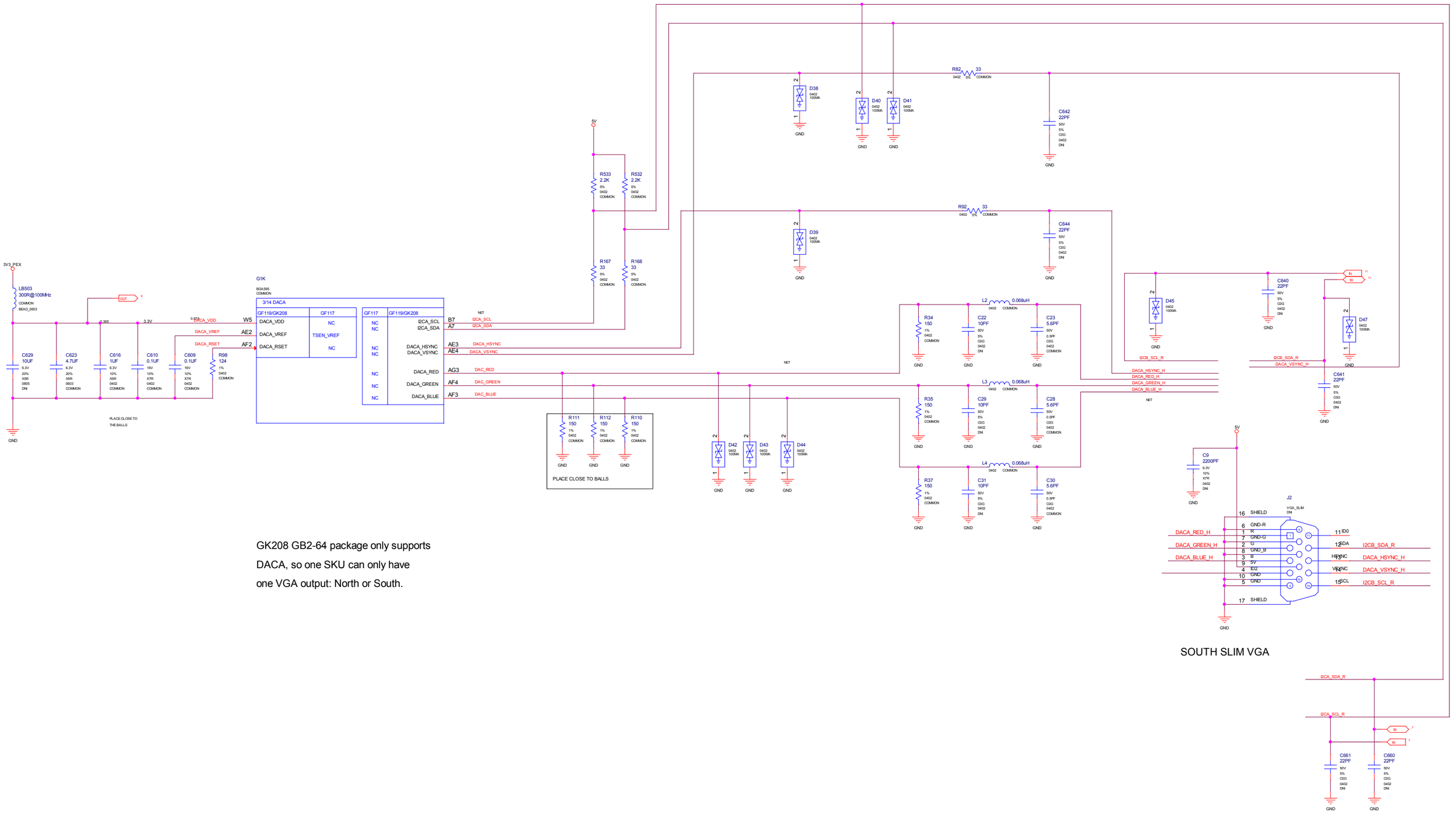
Page9: UNUSED IFPD,IFPE & IFPF





Page10: DACA VGA

GK208 GB2-64 package only supports DACA, so one SKU can only have one VGA output: North or South.



SOUTH SLIM VGA

Page11: BIOS,JTAG,GPIO & XTAL

Smart Fan

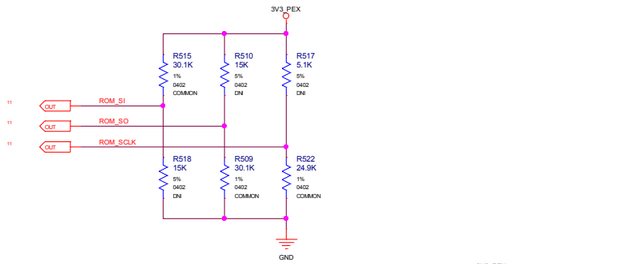
XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

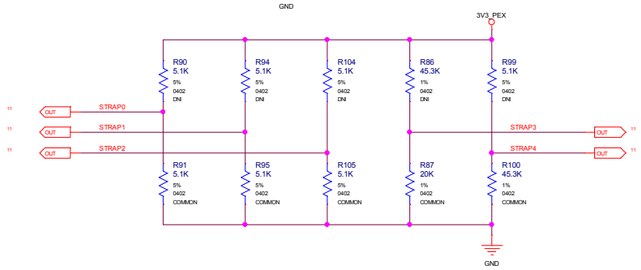
Package Pin Name	MLS Mode	Bringup Mode	Production Mode
MULTI_STRAP_REF0_GND	pull-down	no-stuff	no-stuff/pull-down
MULTI_STRAP_REF1_GND	pull-down	no-stuff	no-stuff/pull-down
MULTI_STRAP_REF2_GND	pull-down	no-stuff	pull-down/no-stuff

x16 mode Strap Definitions

RAMCFG[5:2]	Config	FB Bus Width	Definitions
0000		64-bit	Reserved
0001	256Mx16 DDR3	64-bit	Micron
0010	256Mx16 DDR3	64-bit	Hynix
0011	256Mx16 DDR3	64-bit	Samsung
0100		64-bit	Reserved
0101	128Mx16 DDR3	64-bit	Micron
0110	128Mx16 DDR3	64-bit	Hynix
0111	128Mx16 DDR3	64-bit	Samsung
1000		64-bit	Reserved
1001	256Mx16 DDR3 Dual Rank	64-bit	Micron
1010	256Mx16 DDR3 Dual Rank	64-bit	Hynix
1011	256Mx16 DDR3 Dual Rank	64-bit	Samsung
1100		64-bit	Reserved
1101	128Mx16 DDR3 Dual Rank	64-bit	Micron
1110	128Mx16 DDR3 Dual Rank	64-bit	Hynix
1111	128Mx16 DDR3 Dual Rank	64-bit	Samsung

STRAPS





SKU 0 DEVID = 0x1283

SKU 1 DEVID = 0x1280

TABLE 1: STRAP DECODE ACCORDING TO TERMINATION RESISTANCE/VOLTAGE

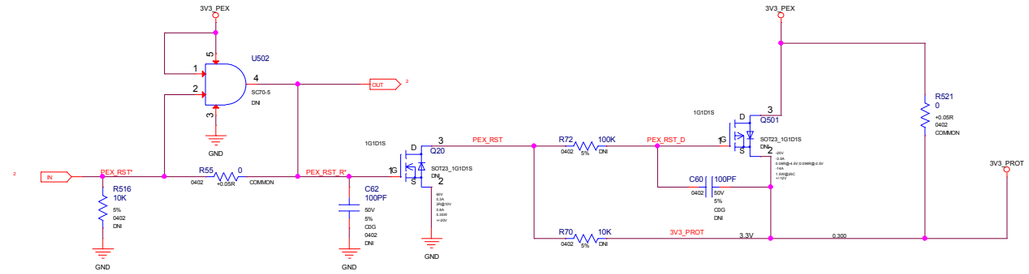
TERMINATION RESISTANCE	TERMINATION VOLTAGE 3V3 [3:0]	TERMINATION VOLTAGE GND [3:0]
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

STRAP PIN MODE TABLE

PIN NAME	MULTI-LEVEL bit [3:0]	BINARY BRINGUP
STRAP0	USER[3:0]	3GIO_PADCFG_LUT_ADR0
STRAP1	3GIO_PADCFG_ADR[3:0]	3GIO_PADCFG_LUT_ADR1
STRAP2	PCI_DEVID[3:0]	3GIO_PADCFG_LUT_ADR2
STRAP3	SOR[3:0]_EXPOSED	3GIO_PADCFG_LUT_ADR3
STRAP4	RESERVED, RESERVED, PCIE_MAX_SPEED, DP_PLL_VDD_33V	PCI_MAX_SPEED
ROM_SCLK	PCIDEVID[4], SUB_VENDOR, PCIDEVID[5], PEX_PLL_EN_TERM	SMB_ALT_ADDR
ROM_SI	RAMCFG[3:0]	SUB_VENDOR
ROM_SO	FB[1], FB[0], SMB_ALT_ADDR, VGA_DEVICE	VGA_DEVICE

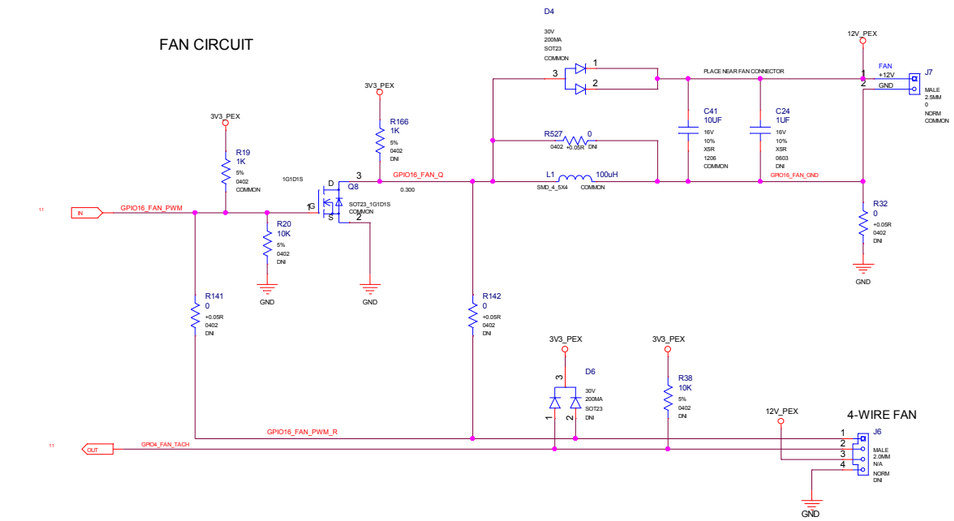
NOTE 2: See table 1 for the correct value/SLOCATION of the strap resistor for the desired modes

Backdrive Prevention

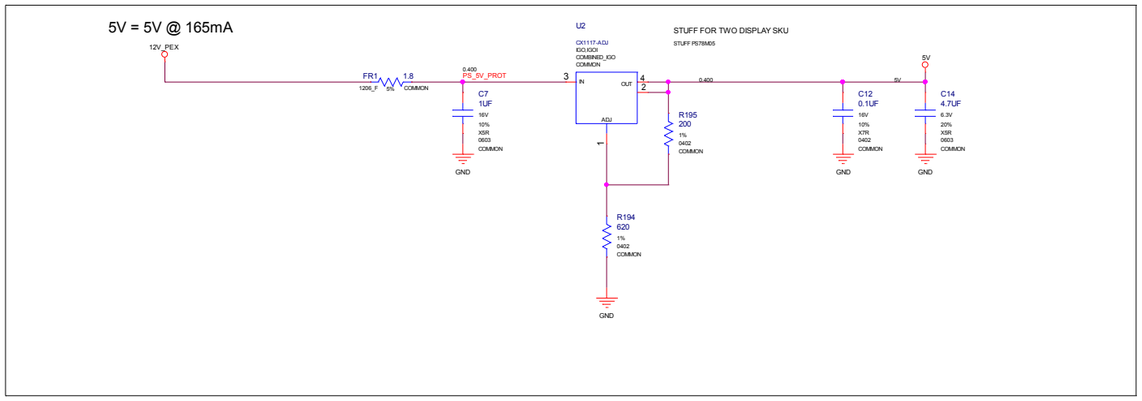


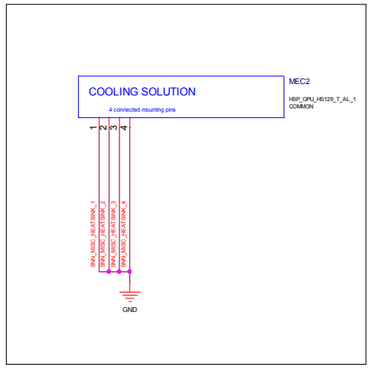
3V3_PROT = 3.3V @ 320mA

FAN CIRCUIT



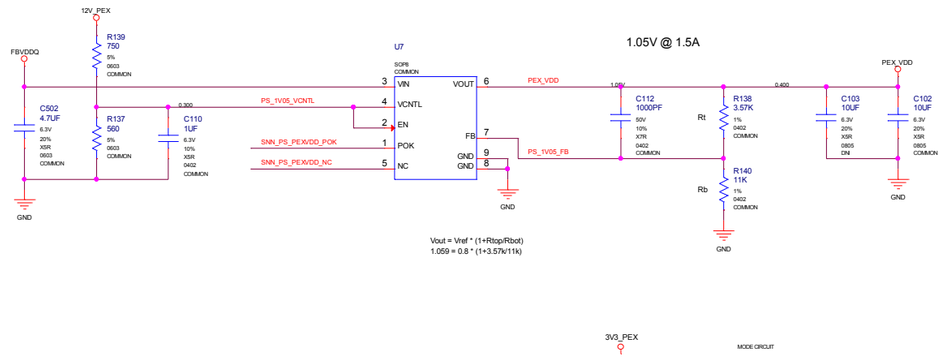
Page13: PS 5V,PEXVDD



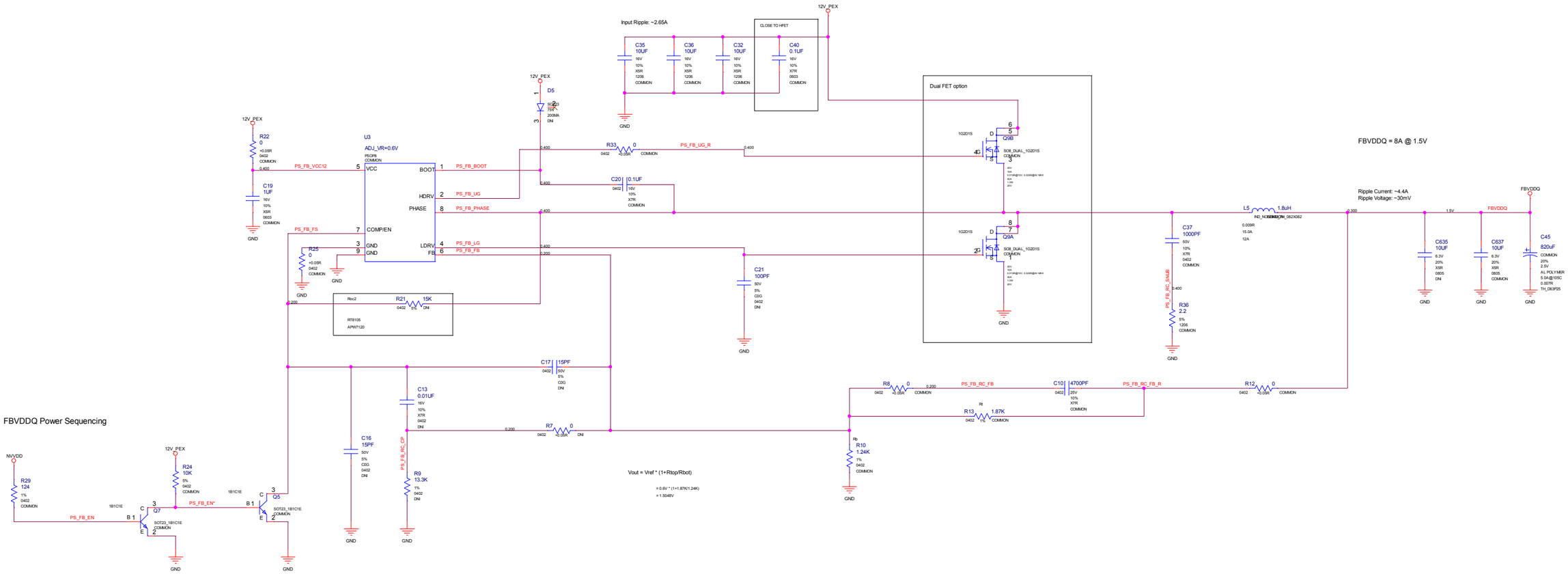


1

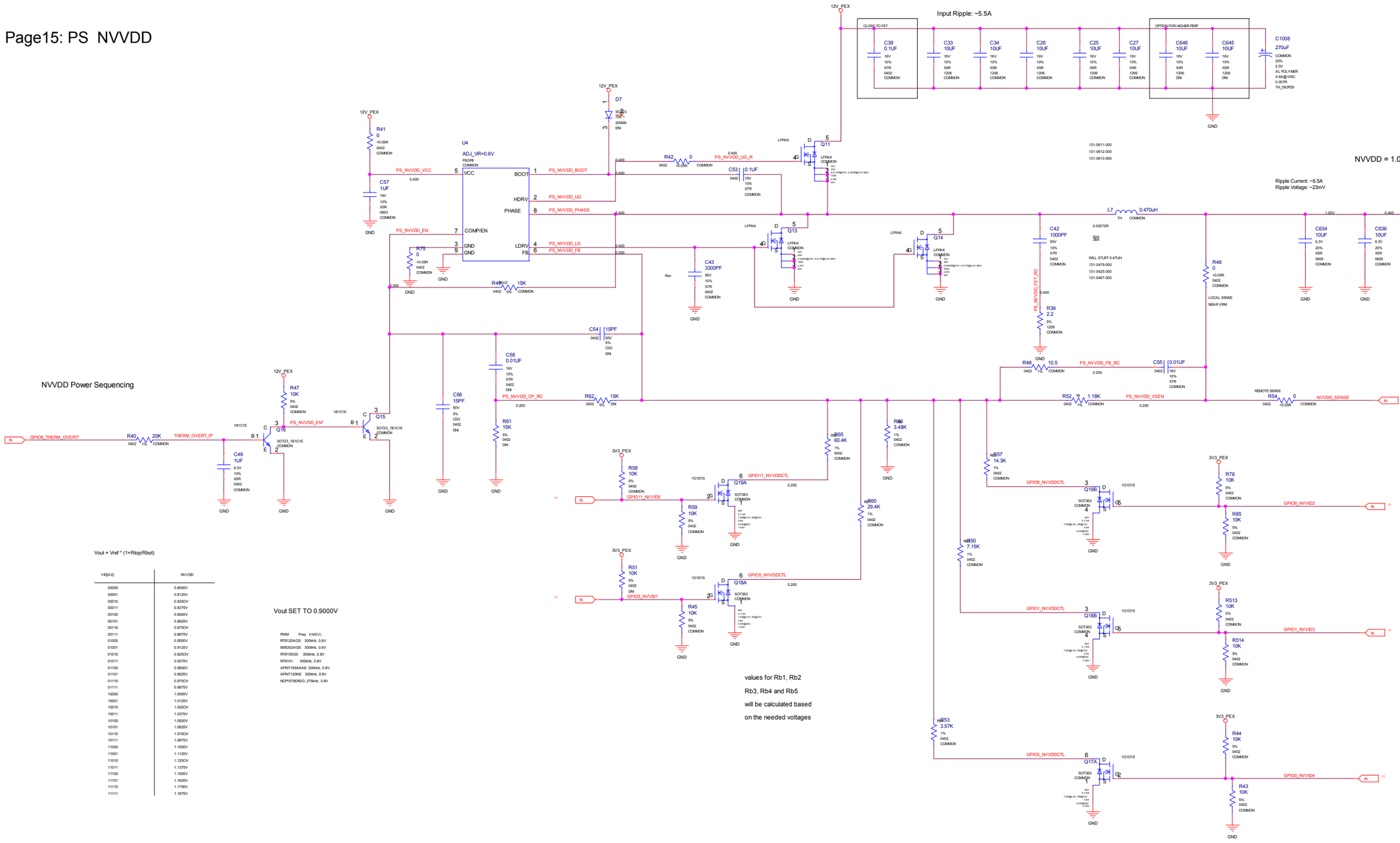
PEX_VDD



Page14: PS FBVDDQ



Page15: PS NVVDD



VID[4:0]	NVVDD
00000	0.8000V
00001	0.8125V
00010	0.8250V
00011	0.8375V
00100	0.8500V
00101	0.8625V
00110	0.8750V
00111	0.8875V
01000	0.9000V
01001	0.9125V
01010	0.9250V
01011	0.9375V
01100	0.9500V
01101	0.9625V
01110	0.9750V
01111	0.9875V
10000	1.0000V
10001	1.0125V
10010	1.0250V
10011	1.0375V
10100	1.0500V
10101	1.0625V
10110	1.0750V
10111	1.0875V
11000	1.1000V
11001	1.1125V
11010	1.1250V
11011	1.1375V
11100	1.1500V
11101	1.1625V
11110	1.1750V
11111	1.1875V

PWM Freq Vref(V)
RT8120AGS: 300kHz, 0.6V
EMB30AGE: 300kHz, 0.6V
RT8105GS: 300kHz, 0.8V
RT8101: 300kHz, 0.8V
APW7165AKAE: 300kHz, 0.8V
APW7123KE: 300kHz, 0.8V
NCP5709DRQ: 275kHz, 0.8V