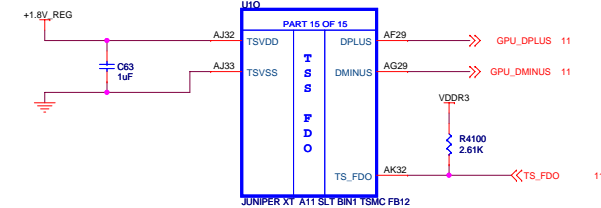
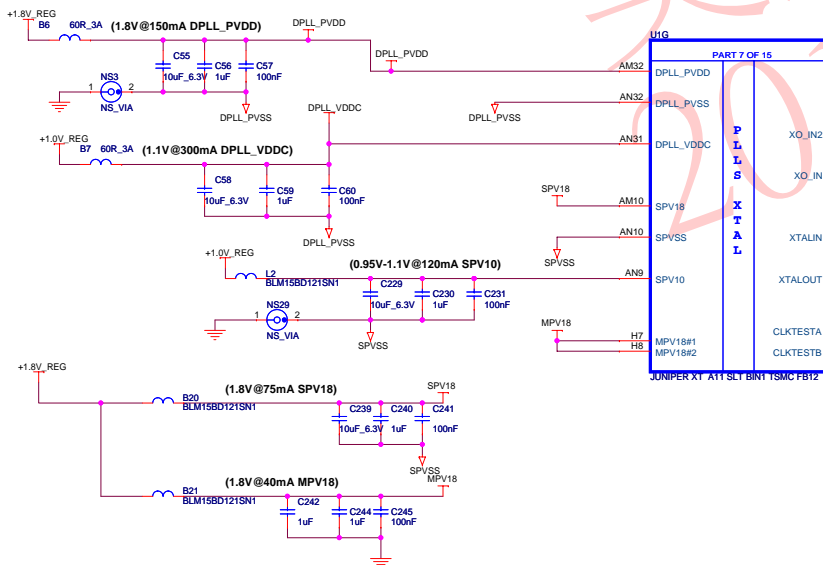


PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC




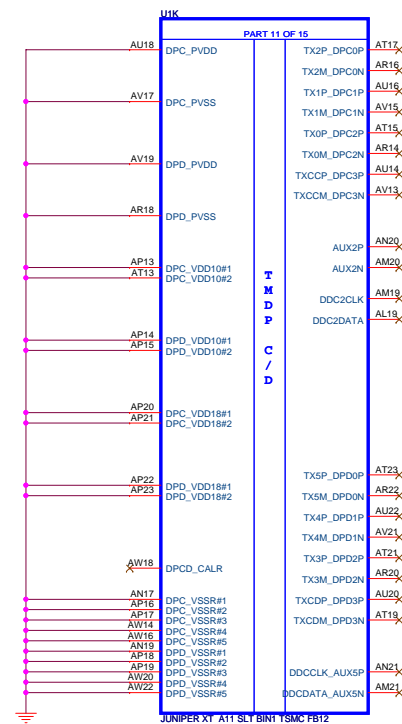
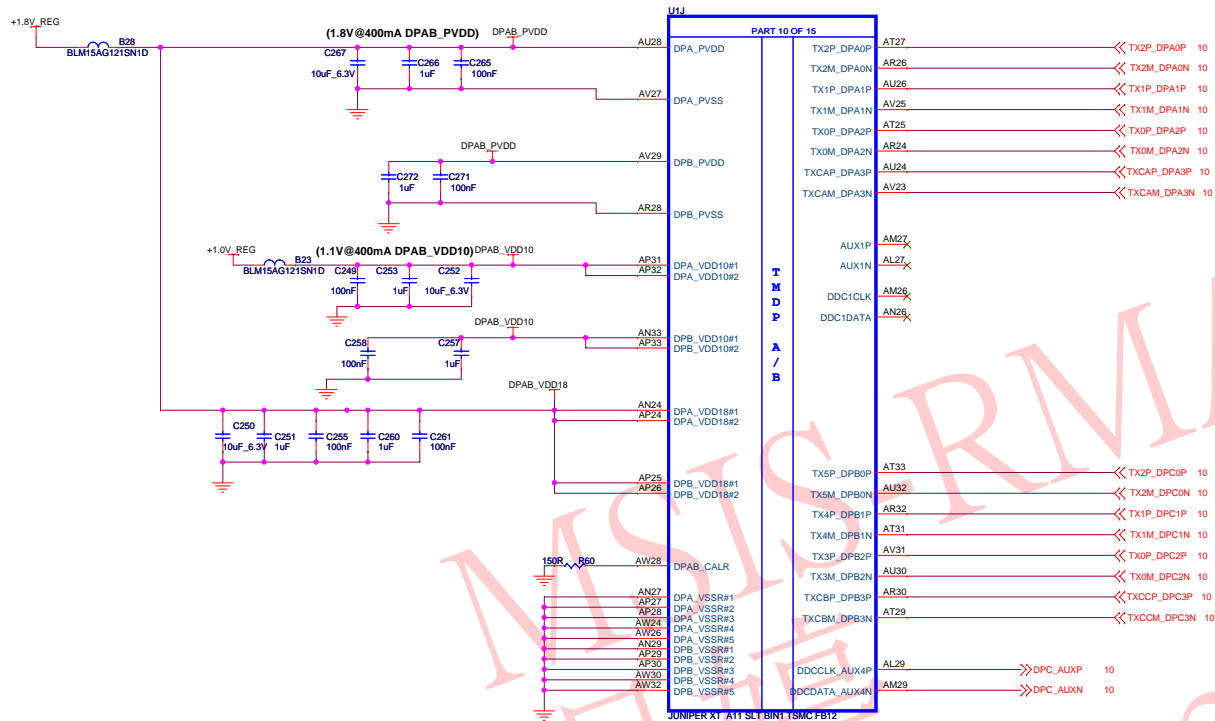
A 256MB MEMORY APERTURE SIZE
CAN BE DEFINED USING A SEPARATE
ROM OR STRAPPING

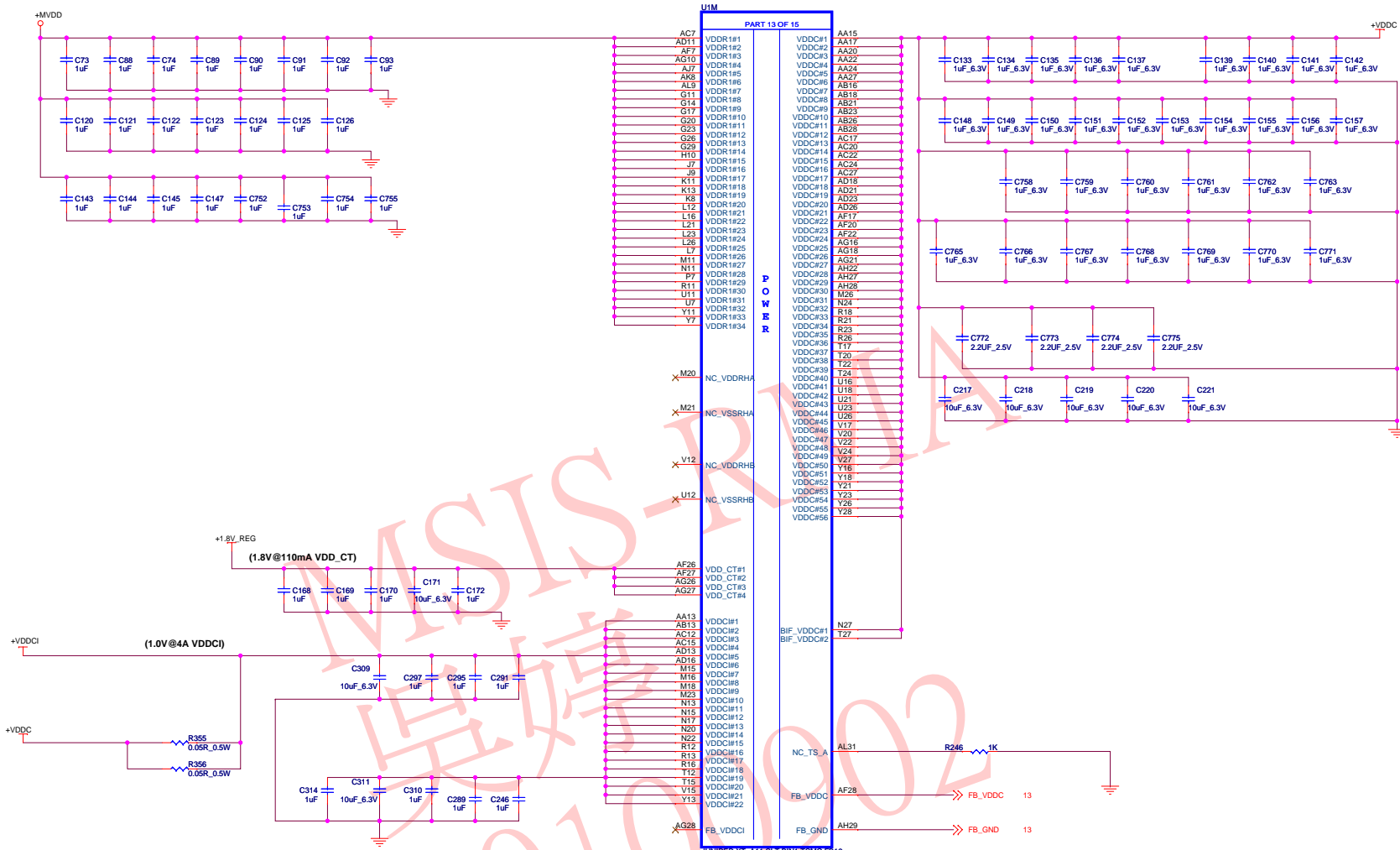
A 256MB MEMORY APERTURE SIZE
CAN BE DEFINED USING A SEPARATE
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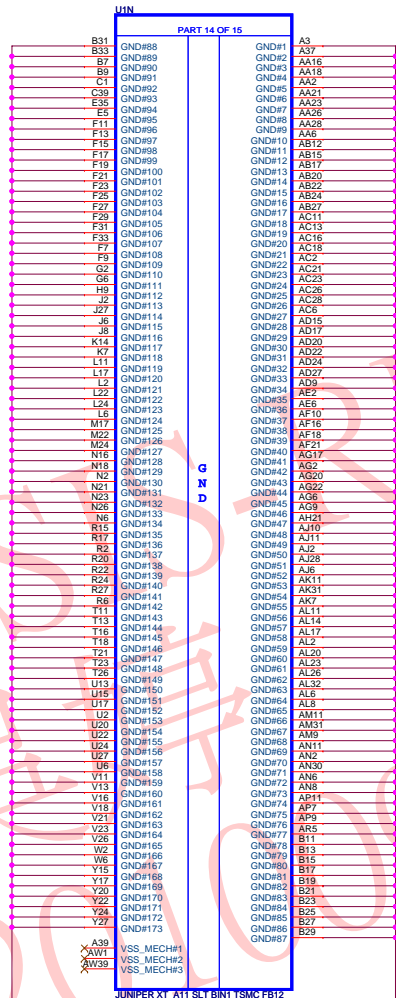
SERIAL EEPROM 512K/1M

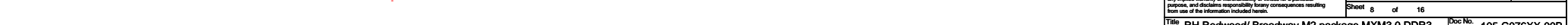
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Date: Monday, December 07, 2009		
Sheet 2 of 16		





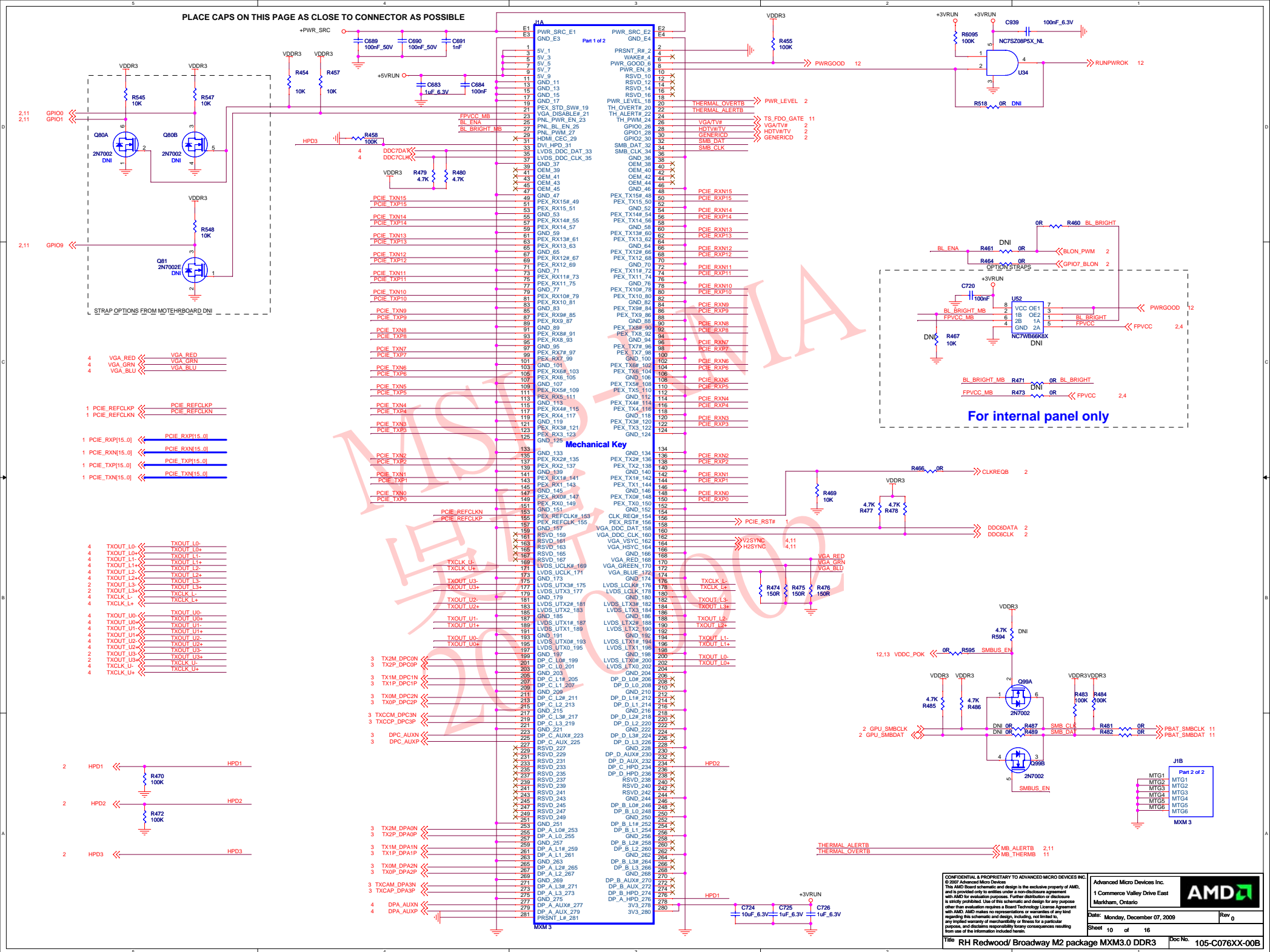


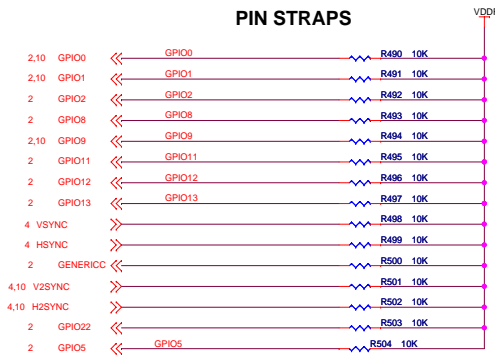


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<p>Advanced Micro Devices Inc. AMD 1 Commerce Valley Drive East Mukwonago, Ontario</p>	<p>Date: <u>Monday, December 07, 2009</u> Rev <u>0</u> Sheet <u>8</u> of <u>16</u></p>		
<p>Title: RH Redwood/ Broadway M2 package MXM3.0 DDR3 Doc No: 105-C076XX-00B</p>			

CHANNEL B: 256MB/512MB DDR3





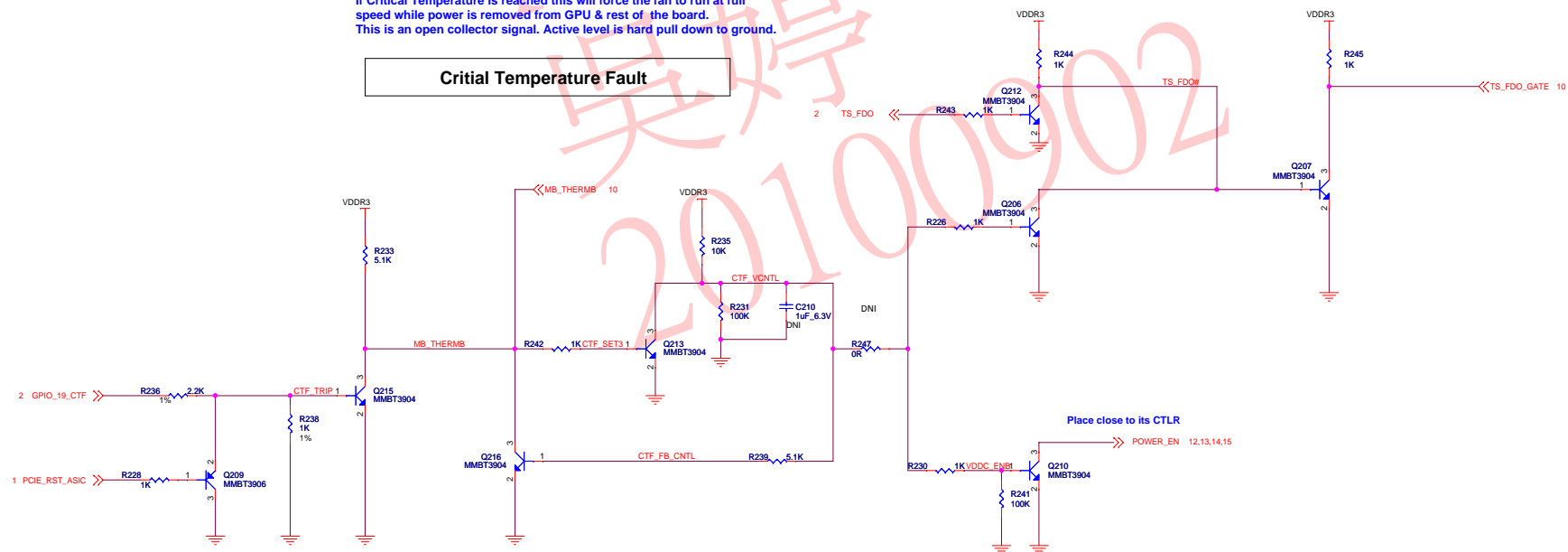


CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	[GPIO13:11]	SERIAL_ROM_TYPE_OR_MEMORY_APERTURE_SIZE_SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNCC		0
CC2VPASS	GENERICCC		0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSYNCC	Audio function present	1
MEMORY_CFG1G	[GPIO5,GPIO16]		
HYNX	[0:1]		
SAMSUNG	[1:0]		

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

HZSYNC	GENERICC
<p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
GPI0_28_TDO	GPI021_BB_EN

Critical Temperature Fault



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Date: Monday, December 07, 2009

Rev

Sheet 11 of 16

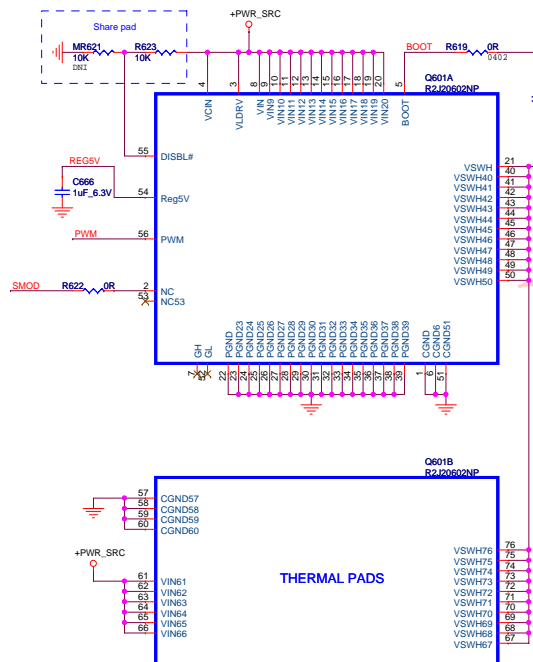
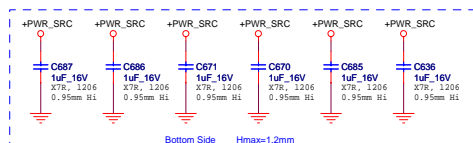
16

Page MYM3.0.DDB

DDP

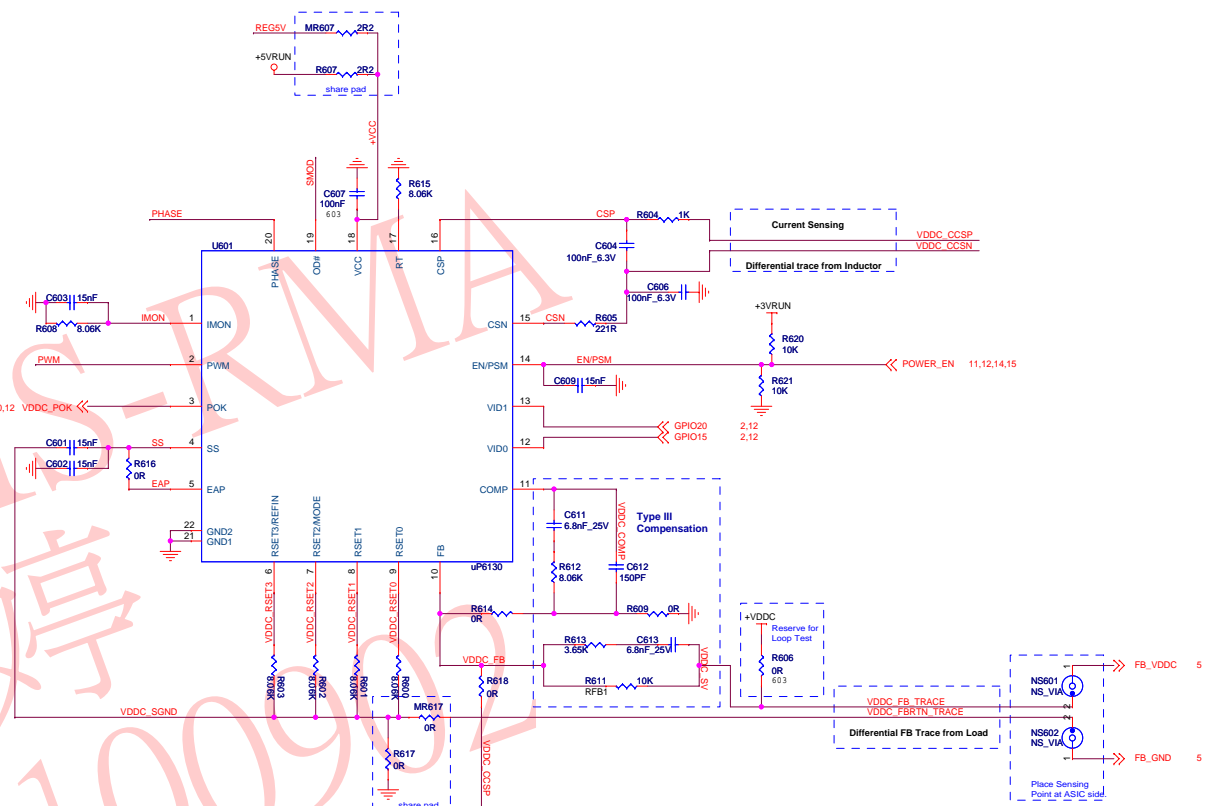
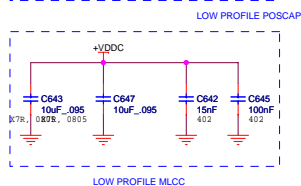
Title	RH Redwood/ Broadway M2 package MXM3.0 DDR3
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Doc No. 105-C076XX-00B



Pin Difference Between R2J2062NP and R2J2065NP		
	R2J2062NP	R2J2065NP
3	VLDRV	NC
8	VIN	NC
2	NC	LSDBL4
52	NC	TURN

Top Side Hmax=1.5mm



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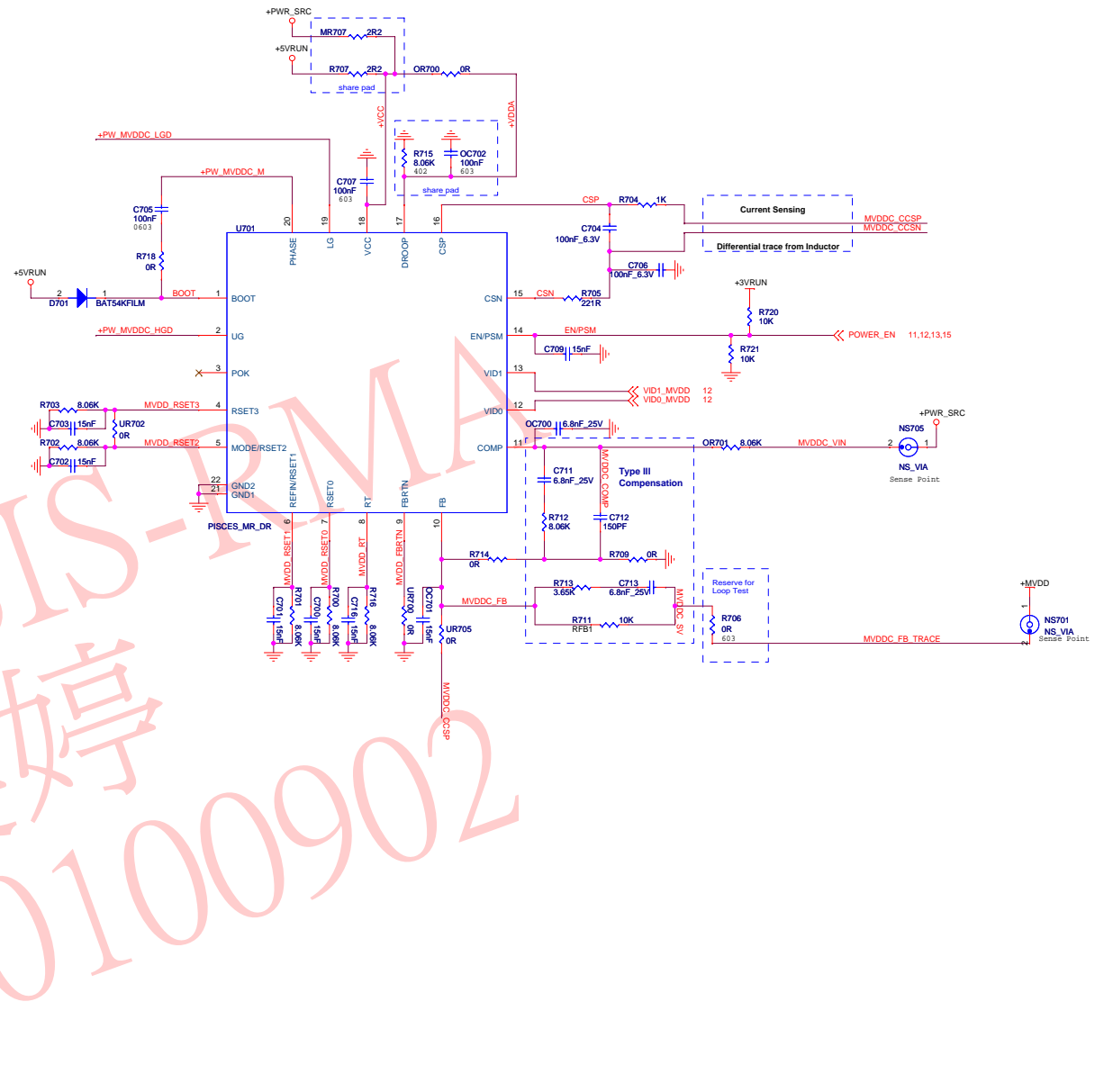
Sheet 13 of 16

Title	RH Redwood/ Broadway M2 package MXM3.0 DDR3
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Doc No.	105-C076XX-00E
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The diagram illustrates the power plane layout, divided into a Top Side and a Bottom Side. The Top Side features four capacitors (C721, C732, C729, C731) connected to PWR_SRC and GND, with dimensions Hmax=1.5mm. The Bottom Side features two capacitors (C730, C733) connected to PWR_SRC and GND, with dimensions Hmax=1.2mm.


Capacitor	Value	Part Number	Dimensions
C721	2.2uF, 16V	X7R, 1206	1.3mm x 1.3mm
C732	2.2uF, 16V	X7R, 1206	1.3mm x 1.3mm
C729	2.2uF, 16V	X7R, 1206	1.3mm x 1.3mm
C731	2.2uF, 16V	X7R, 1206	1.3mm x 1.3mm
C730	1uF, 16V	X7R, 1206	0.95mm x 0.95mm
C733	1uF, 16V	X7R, 1206	0.95mm x 0.95mm

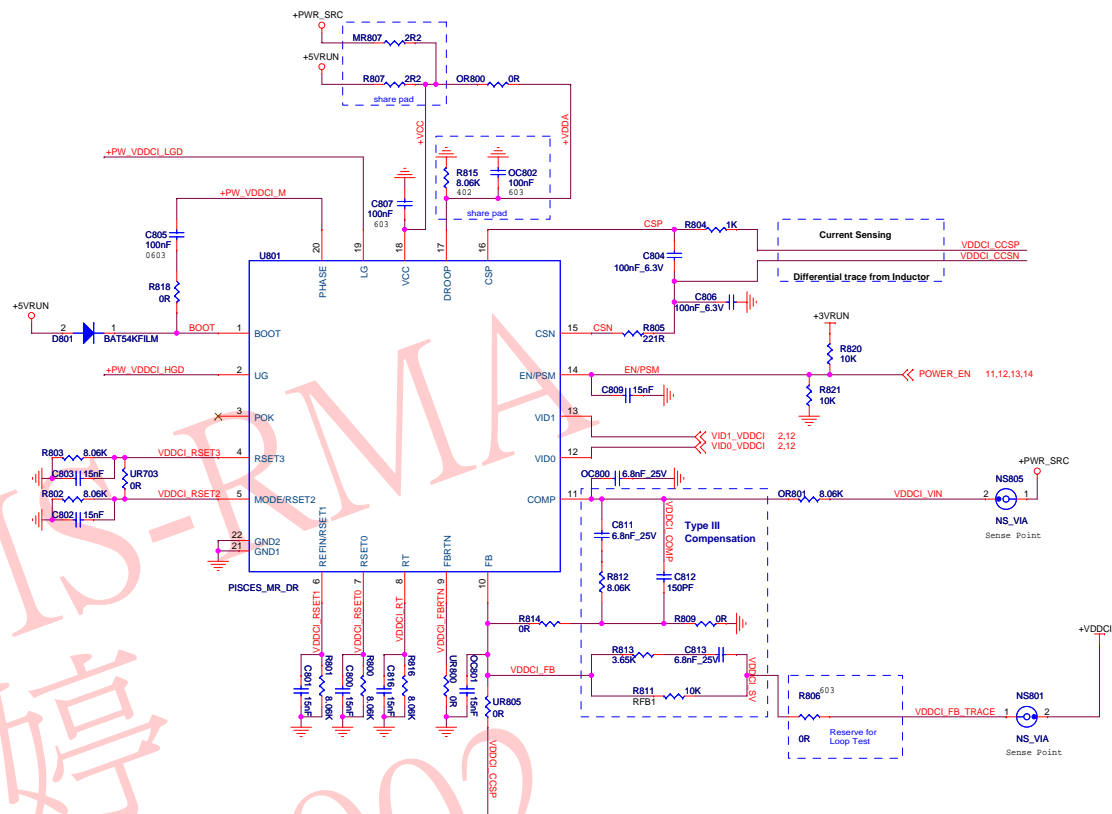
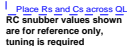
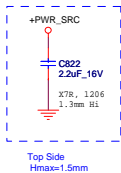


RC snubber values shown
are for reference only,
tuning is required

MVDCC_CSP

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Date: Monday, December 07, 2009		Rev 0	
Sheet 14 of 16			
Page MXM3.0 DDR3		Doc No. 105-C076XX-00B	



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Sheet 15 of 16

Doc No. 105-C076XX-00B

<div>AMD</div>			Title		Schematic No.		Date:	
			RH Redwood/ Broadway M2 package MXM3.0 DDR3		105-C076XX-00B		Monday, December 07, 2009	
			REVISION HISTORY		NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.			Rev 0
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION					
0	00A	09/27/09	Create new SCHs					
	00B	12/03/09	Added PWR_EN short to DrMOS Added DrMOS Thermal Pad					
			<div>MSIS-RMA 吳婷 20100902</div>					