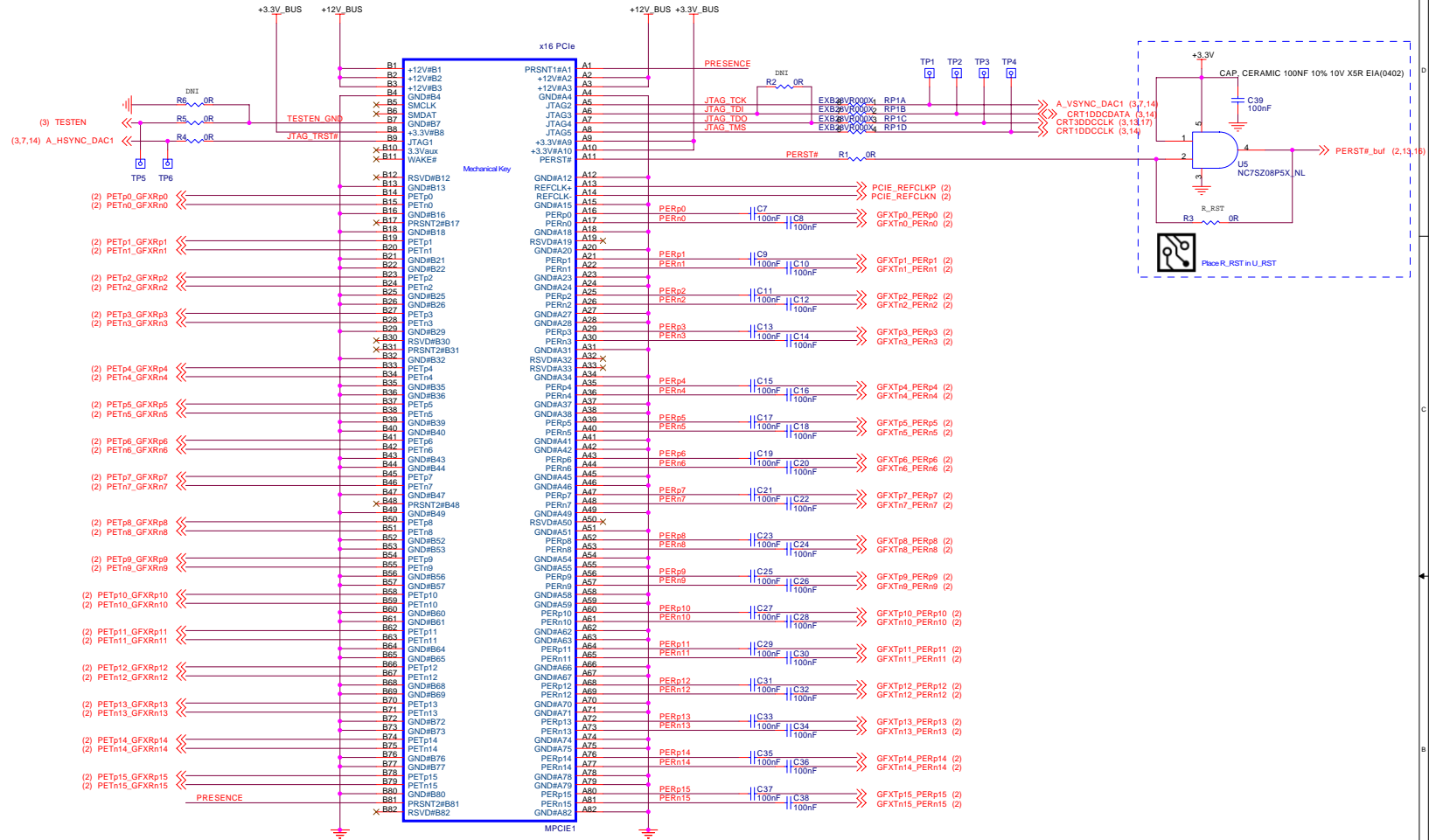
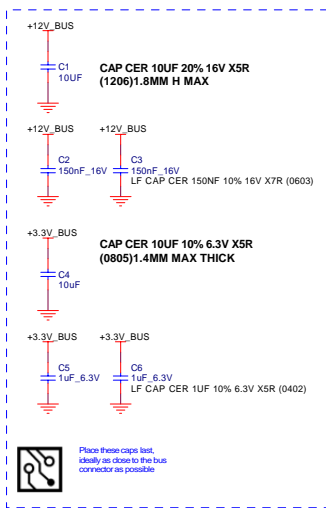
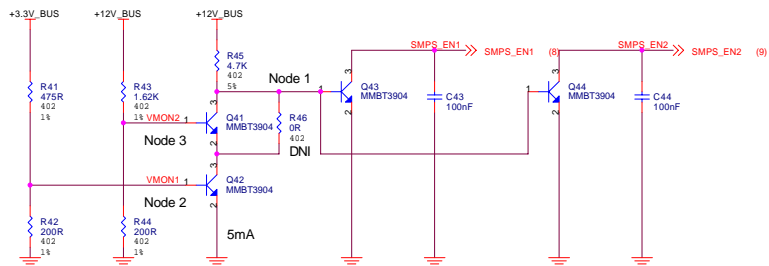


PCI-EXPRESS EDGE CONNECTOR



POWER SEQUENCING



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation. Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

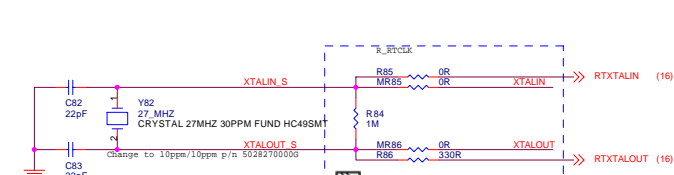
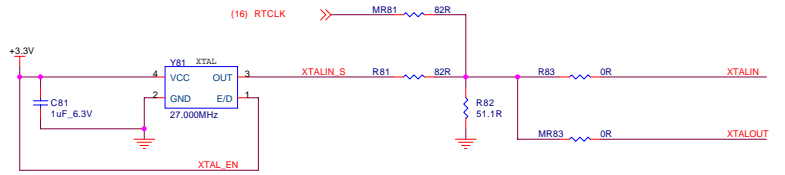
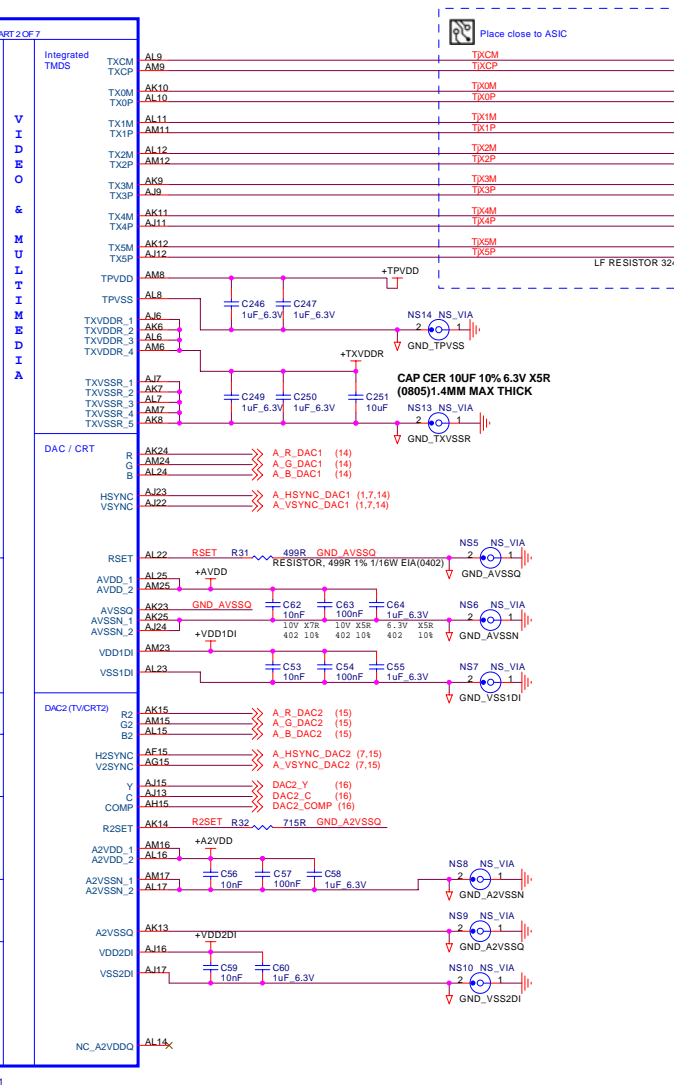
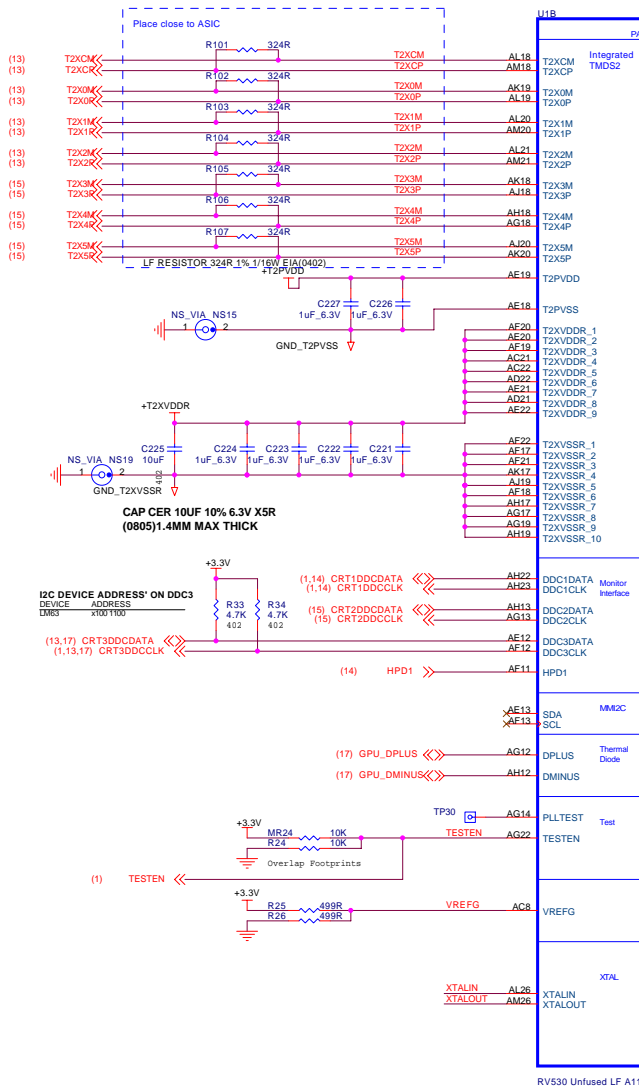
- Node 1** When +12V ramps above min Vbe, SMPS_EN will be held low
- Node 2** When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active
- Target ~ 900mV when +3.3 at min regulation (worse case)
- Typical trigger when +3.3V ramps above 2.2V (650mV)
- Node 3** When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active
- Target ~ 1.25V when +12 at min regulation (worse case)
- Typical trigger when +12V ramps above 10V (1.1V)

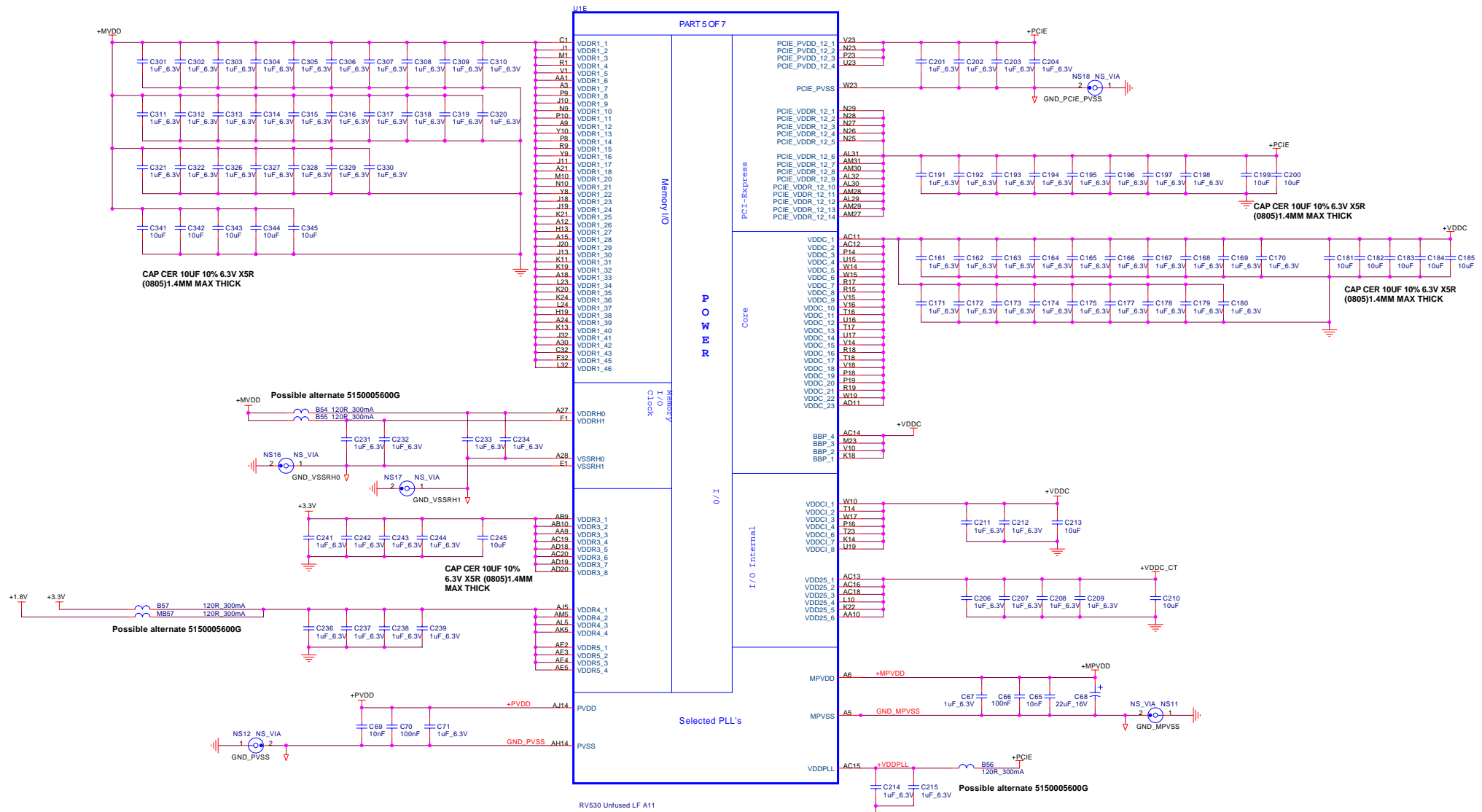
| SYMBOL LEGEND | |
|---------------|----------------|
| DNI | DO NOT INSTALL |
| # | ACTIVE LOW |
| ⏏ | DIGITAL GROUND |
| ⏏ | ANALOG GROUND |



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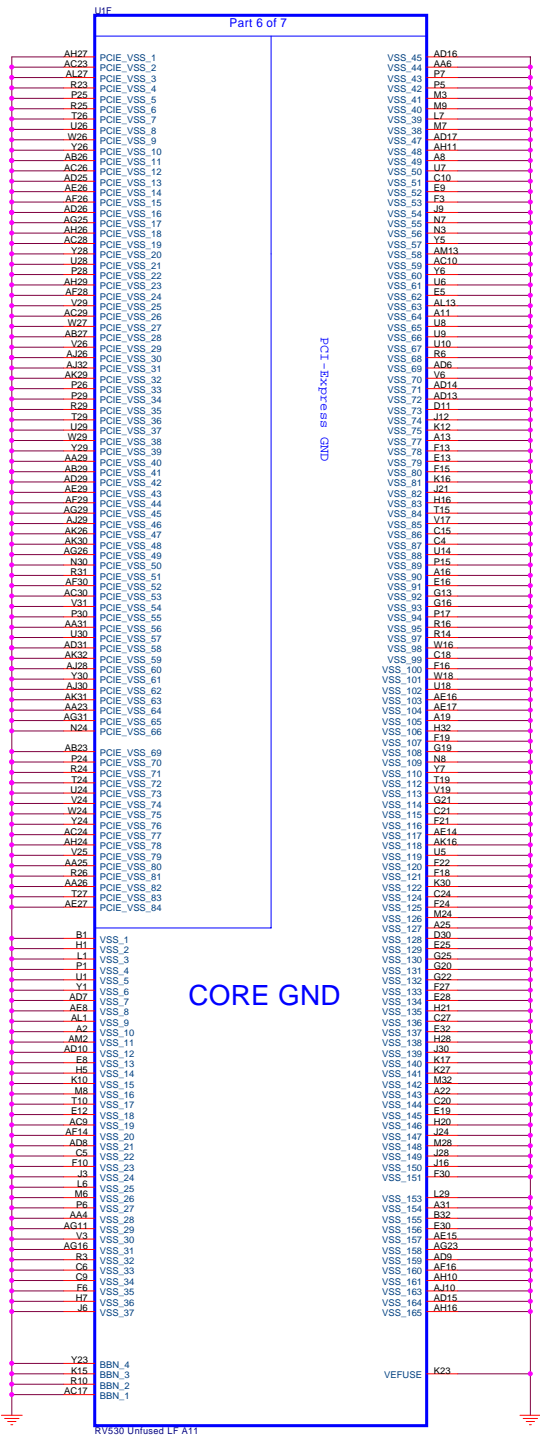
| | |
|-------|--|
| Title | RV530/RV515 256MB DDR3-136 Dual 2x DVI VIVO FH |
| Size | Document Number 105-A671xx-00A |
| Sheet | 1 of 20 |
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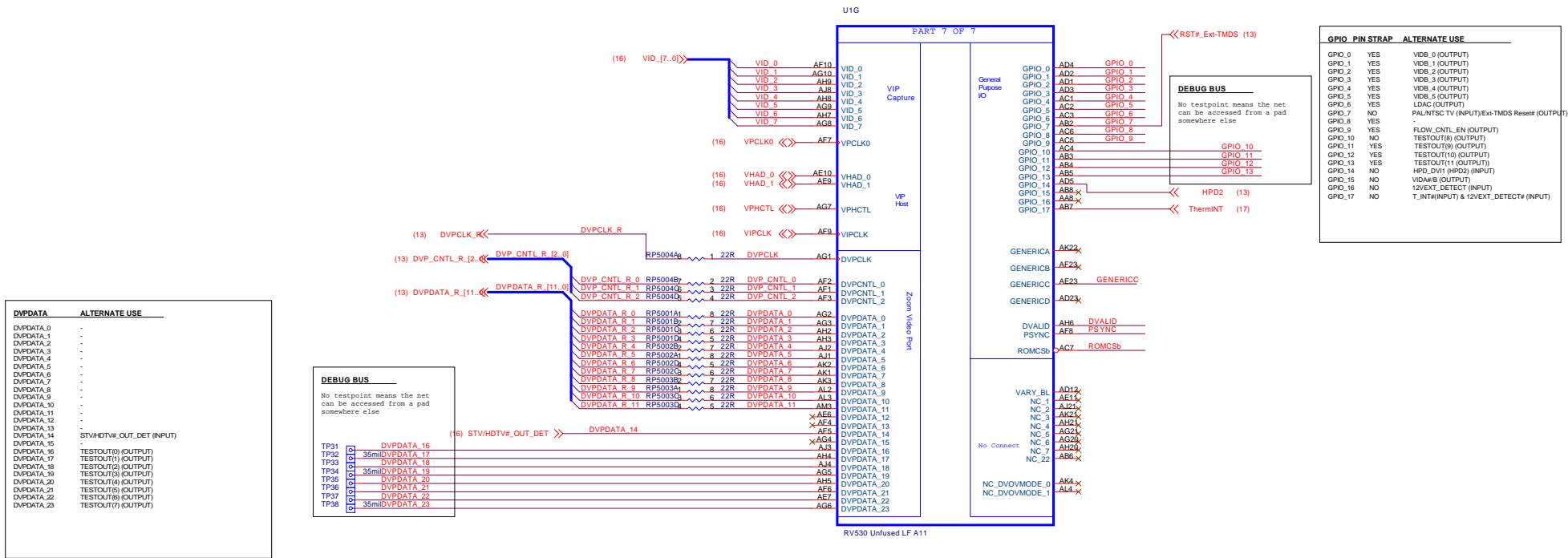
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Title: RV530/RV515 256MB DDR3-136 Dual 2xDV1 VIVO FH
 Size: C
 Document Number: 105-A671xx-00A
 Date: Saturday, August 06, 2005
 Sheet: 4 of 20
 Rev: 0

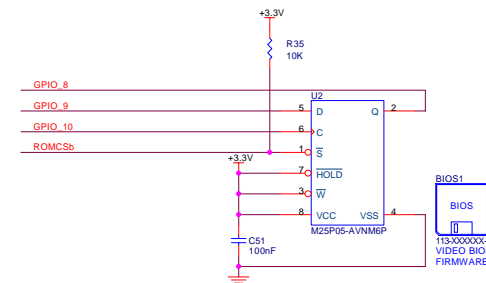
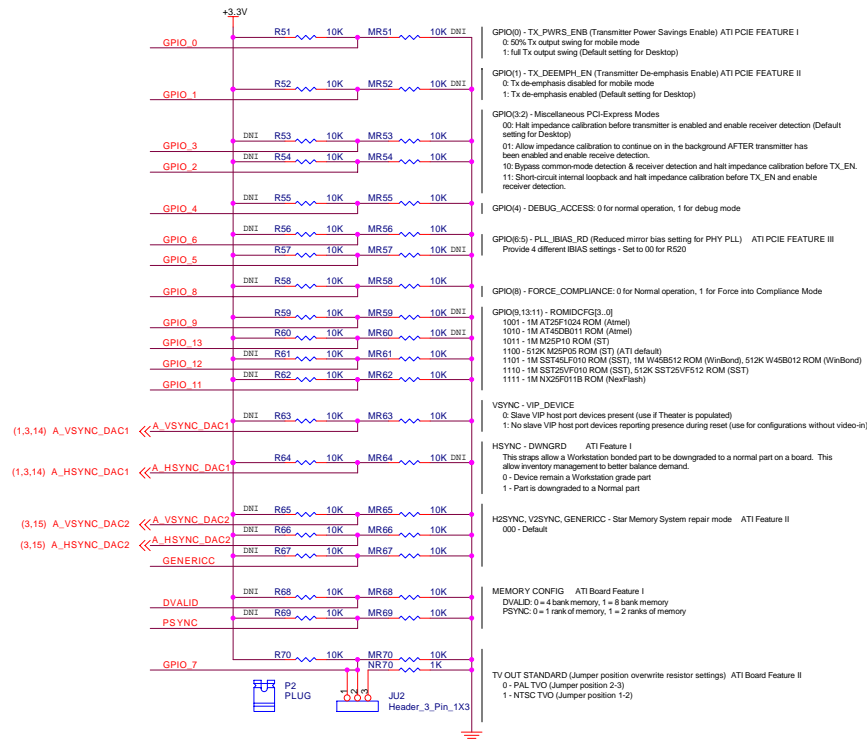


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Date: Saturday, August 06, 2005 Sheet: 6 of 20



PIN BASED STRAPS

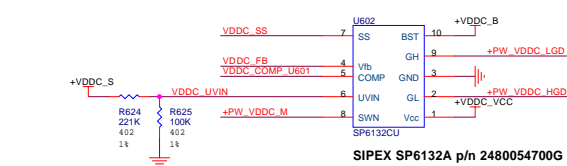


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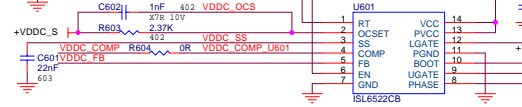
| | | | |
|-------|---|----------------|---------|
| Title | RV530/RV515 256MB DDR3-136 Dual 2xDV1 VIVO FH | Rev | 9 |
| Size | Document Number | 105-A671xx-00A | |
| Date | Saturday, August 06, 2005 | Sheet | 7 of 20 |

VDDC-PWM1



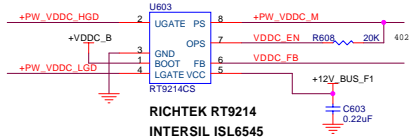
SIPEX SP6132CU p/n 2480054700G

VDDC-PWM2



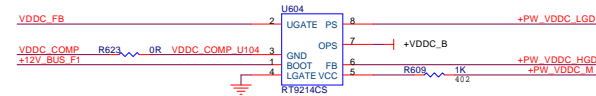
INTERISL ISL6522/ISL6535
RICHTEK RT9232/RT9232A
ANPEC APW7062A
ANPEC APW7062B

VDDC-PWM3



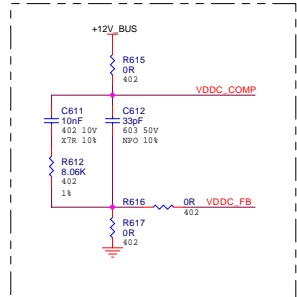
RICHTEK RT9214
INTERISL ISL6545

VDDC-PWM4

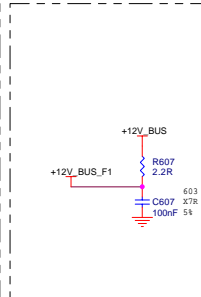


ANPEC APW7061A

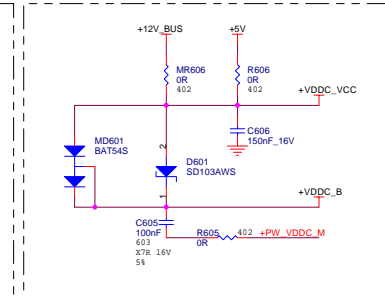
COMPENSATION CIRCUIT



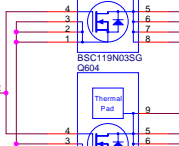
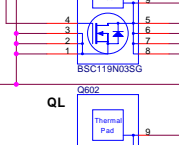
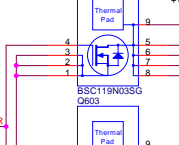
FILTERED +12V_BUS



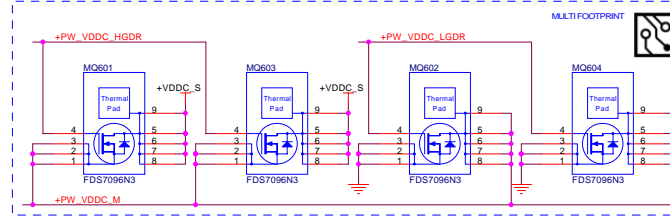
BOOT CIRCUIT



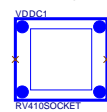
QH



RC snubber values shown are for reference only, tuning is required



This symbol is used for 103 SMPS p/n.



Regulator for VDDC (ASIC Core)

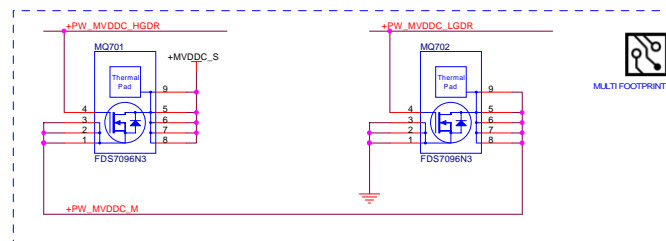
Vout = 1V ~ 1.3V

| Part | Vout | R1 | R2 |
|----------|-------|----------|----------|
| 0.8V Ref | 1.2V | 1.00K 1% | 2.00K 1% |
| | 1.25V | 1.00K 1% | 1.78K 1% |
| | 1.3V | 1.00K 1% | 1.6K 1% |



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| Part | Vout | R1 | R2 |
|----------|------|----------------|---------------|
| 0.8V Ref | 1.9V | 1.78K | 1.3K |
| | 2.0V | 1.69K 1.78K | 1.1K 1.21K |
| | | | |

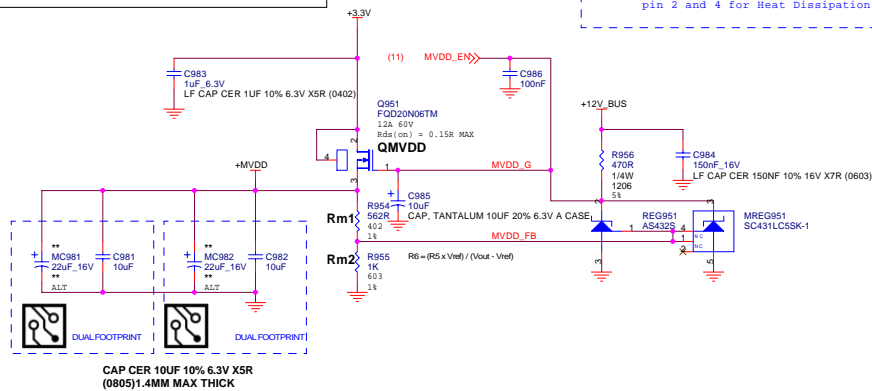


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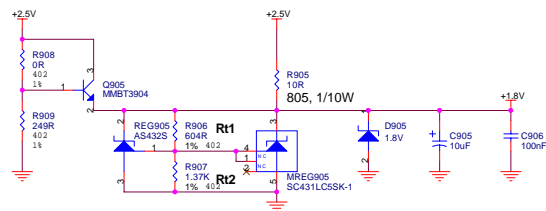
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|--------|-----------------|--|---------------------------|---|-------|---------|--|
| Title | | | | RV530/RV515 256MB DDR3-136 Dual 2xDVI VIVO FH | | | |
| Size | Document Number | | | | | Rev | |
| Custom | 105-A671xx-00A | | | | | 0 | |
| Date: | | | Saturday, August 06, 2005 | | Sheet | 9 of 20 | |

Regulator for +MVDDQ
Vout = 1.85V ~ 2.65V
Iout = 1.7A MAX
P_QMVDD = 2.5W MAX

Place Big Copper Area Under QMVDD
pin 2 and 4 for Heat Dissipation.



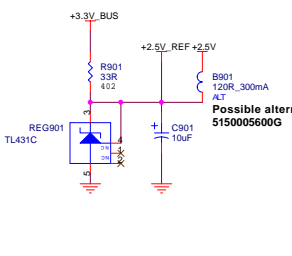
| Voltage Req. | Rm1 | Rm2 |
|----------------------|------------------------------------|------------|
| 2.85V | | |
| 2.55V | 22.1R 316022R100G 1.1K 3240110100G | 2.5V Ref. |
| 2.5V | 0R 31500000000 DNI | 2.5V Ref. |
| 2.1V min | 681R 3160681000G 953R 3240953000 | 1.24V Ref. |
| 2.0V min | 681R 3160681000G 1.1K 3240110100G | 1.24V Ref. |
| 1.9V min, 1.94V nom. | 562R 3160562000G 1K 3160100100G | 1.24V Ref. |



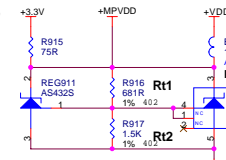
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| | |
|--------|--|
| Title | RV530/RV515 256MB DDR3-136 Dual 2xDTV1 VIVO FH |
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| Rev | 0 |

Alt regulator for +MPVDD
Vout = 1.2V (not tracking to VDDC)
Iout = 10mA MAX

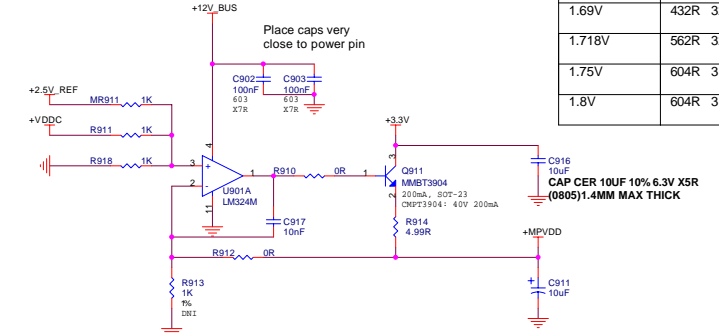


Possible alternate
5150005600G



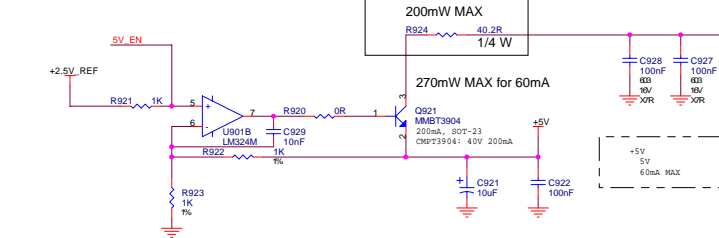
Possible alternate 5150005600G

| | Rt1 | Rt2 |
|--------|-------------------------------|------------------------------------|
| 1.52V | 432R 3240432000 3160432000 | 2.15K 3160215100 |
| 1.61V | 432R 3240432000 | 1.5K 3230015200 1.5K 3160150100 |
| 1.69V | 432R 3240432000 | 1.21K 3240121100 |
| 1.718V | 562R 3240562000 | 1.5K 3230015200 1.5K 3160150100 |
| 1.75V | 604R 3160604000 | 1.5K 3230015200 1.5K 3160150100 |
| 1.8V | 604R 3160604000 | 1.37K 3160137100 |



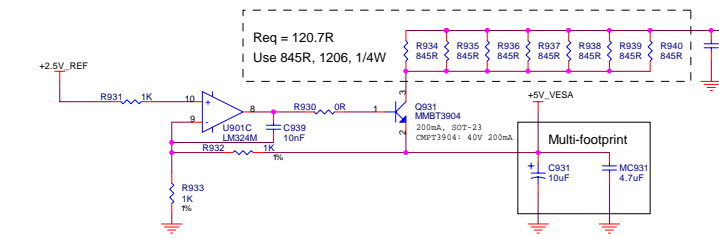
Place caps very close to power pin

CAP CER 10UF 10% 6.3V X5R
 (0805)1.4MM MAX THICK



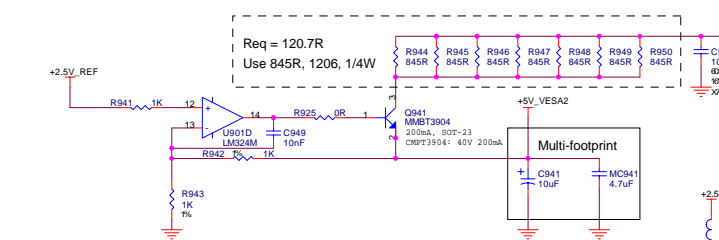
~ 2.5V Drop MAX
 200mW MAX
 270mW MAX for 60mA

CAP CER 10UF 10% 16V X5R
 (1206)1.8MM H MAX



Req = 120.7R
 Use 845R, 1206, 1/4W

Multi-footprint
 MC931 4.7uF

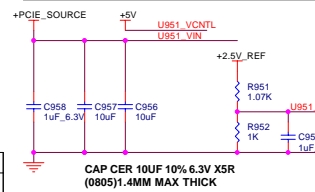


Req = 120.7R
 Use 845R, 1206, 1/4W

Multi-footprint
 MC941 4.7uF

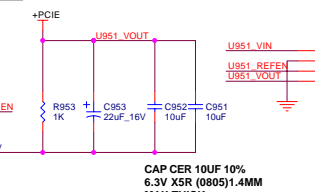
Possible alternate 5150005600G

Optional regulator for +PCIE
Vout = 1.2V ~1.25V
Iout = 1.2A MAX



CAP CER 10UF 10% 6.3V X5R
 (0805)1.4MM MAX THICK

Optional regulator for +PCIE
Vout = 1.2V ~1.25V
Iout = 1.2A MAX

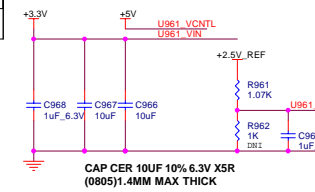


CAP CER 10UF 10% 6.3V X5R
 (0805)1.4MM MAX THICK

RT9199 p/n 2480054800G (480mR RdsON Max)
 RT9199A (300mR RdsON Max)
 RT9173C (250mR RdsON Max)
 APL5331 p/n 2480054200G (350mR MAX for 2A)

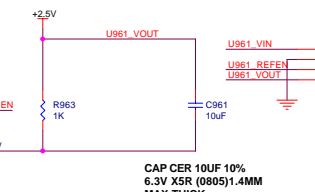
Supported footprint:
RT9173C/RT9199A/RT9199
APL5331

Optional regulator for +2.5V
Vout = 2.5V
Iout = 600mA MAX



CAP CER 10UF 10% 6.3V X5R
 (0805)1.4MM MAX THICK

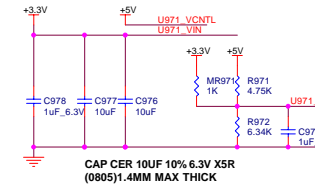
Optional regulator for +2.5V
Vout = 2.5V
Iout = 600mA MAX



CAP CER 10UF 10% 6.3V X5R
 (0805)1.4MM MAX THICK

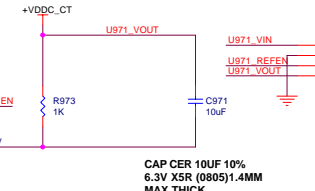
Supported footprint:
RT9173C/RT9199A/RT9199
APL5331

Optional Regulator for +VDDC_CT
Vout = 2.5V ~ 2.85V
Iout = 100mA MAX



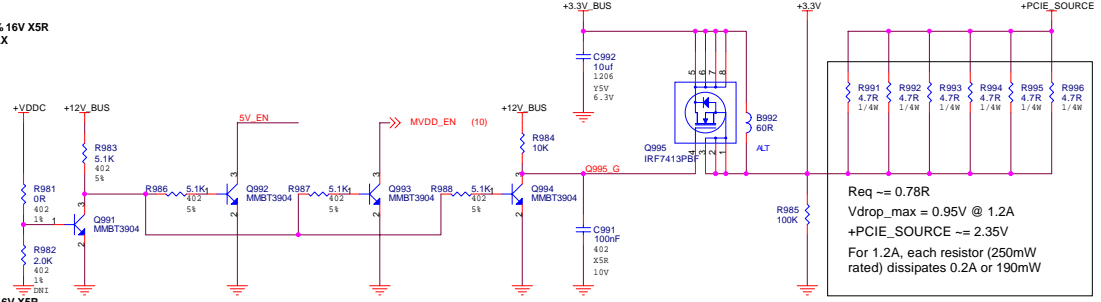
CAP CER 10UF 10% 6.3V X5R
 (0805)1.4MM MAX THICK

Optional Regulator for +VDDC_CT
Vout = 2.5V ~ 2.85V
Iout = 100mA MAX



CAP CER 10UF 10% 6.3V X5R
 (0805)1.4MM MAX THICK

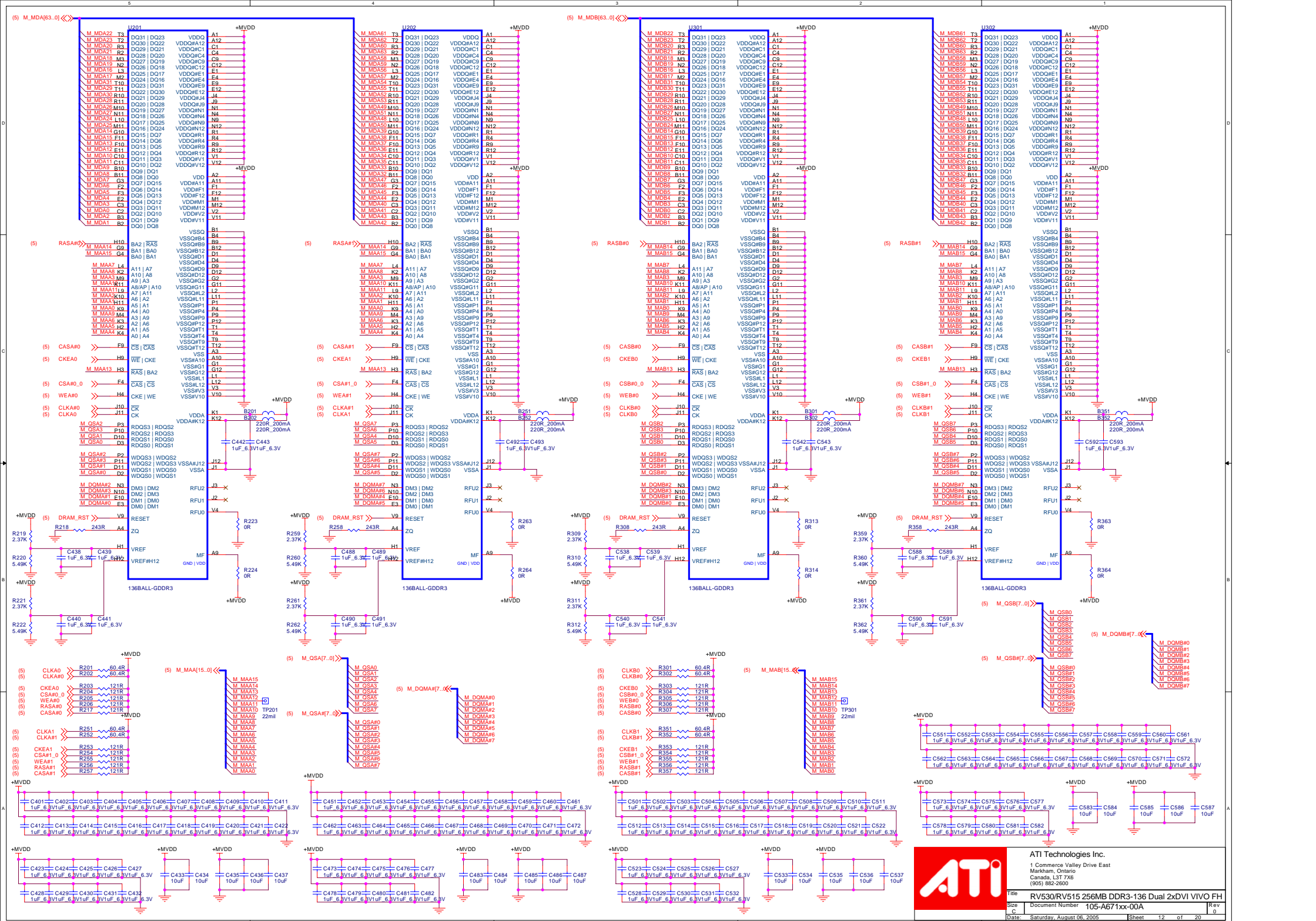
Supported footprint:
RT9173C/RT9199A/RT9199
APL5331

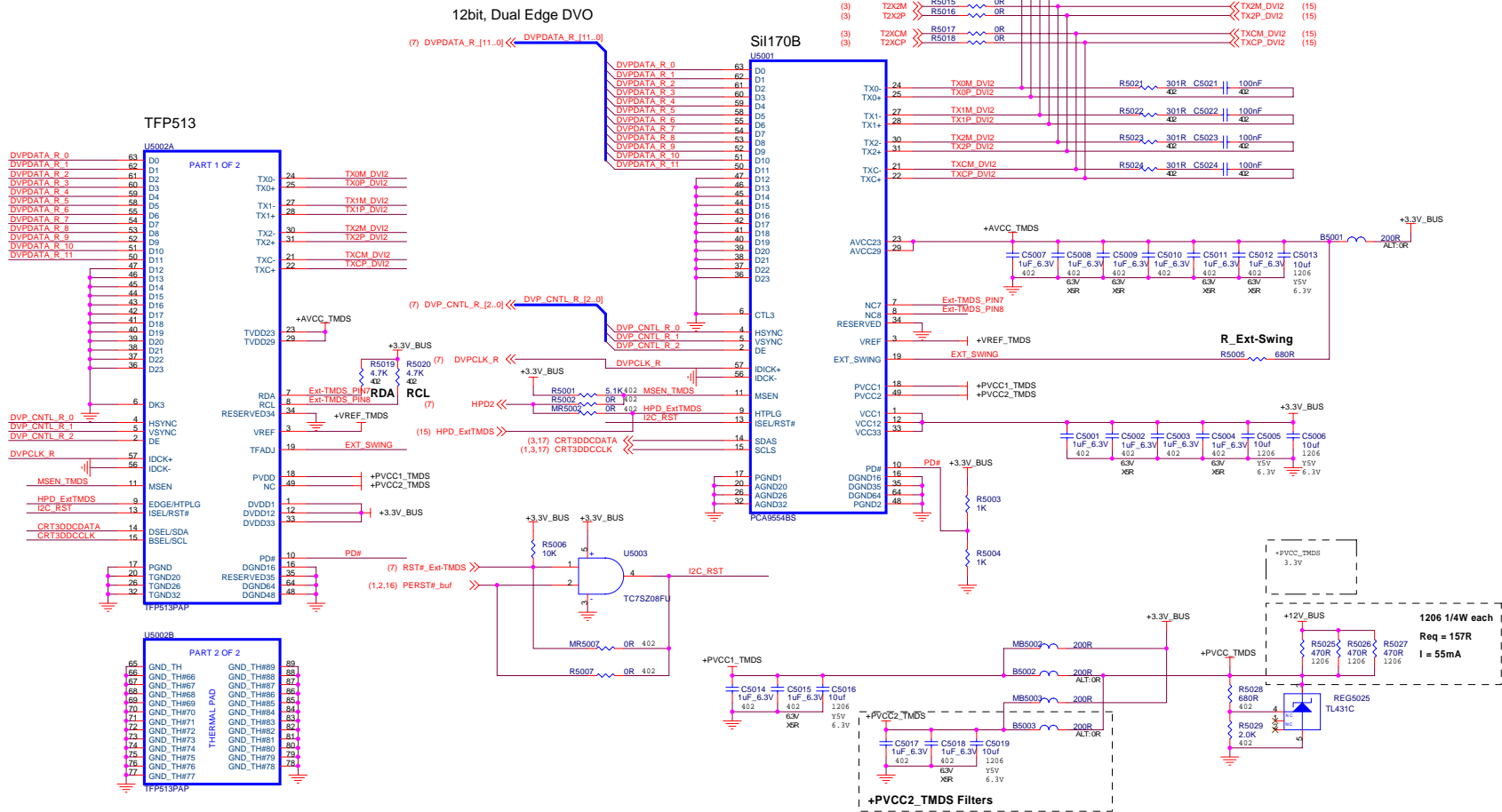


Req ~ 0.78R
 Vdrop_max = 0.95V @ 1.2A
 +PCIE_SOURCE ~ 2.35V
 For 1.2A, each resistor (250mW rated) dissipates 0.2A or 190mW



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STUFFING OPTIONS

| EXT TMDs TX TO BE USED | MUST INSTALL | MUST NOT INSTALL | CAN BE REMOVED |
|------------------------|--|------------------|--------------------------------|
| SiI170B | SiI170B, +PVCC2_TMDs Filters R_Ext-Swing = | TFP513 | RDA, RCL |
| TFP513 | TFP513, RDA, RCL 505R <= R_Ext-Swing <= 1515R | SiI170B | (Optional) +PVCC2_TMDs Filters |

NOTE:
1 - Other components are to be installed.
2 - Components marked as DNI should not be installed. They should only be installed if default board settings are to be changed in which case other components may have to be adjusted accordingly.



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| | | | |
|-------|--|---------------------------|----------------|
| Title | RV530/RV515 256MB DDR3-136 Dual 2x DVI VIVO FH | | |
| Size | Document Number | 105-A671xx-00A | Rev 0 |
| Date | Customer | Saturday, August 06, 2005 | Sheet 13 of 20 |

(3) A_R_DAC2
(3) A_G_DAC2
(3) A_B_DAC2



RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane

(3) CRT2DDCDATA

(3) CRT2DDCLK

(3,7) A_HSYNC_DAC2

(3,7) A_VSYNC_DAC2



SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

(13) HPD_ExtTMS

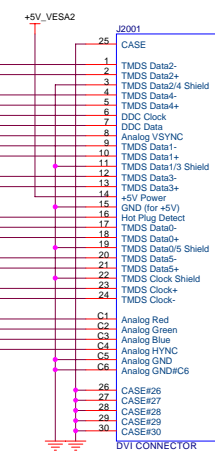
(3) TX3M_DV12
(3) TX3P_DV12
(3) TX4M_DV12
(3) TX4P_DV12
(3) TX5M_DV12
(3) TX5P_DV12

(13) TX2M_DV12
(13) TX2P_DV12
(3) TX4M_DV12
(3) TX4P_DV12
(13) TX1M_DV12
(13) TX1P_DV12
(3) TX3M_DV12
(3) TX3P_DV12
(13) TX0M_DV12
(13) TX0P_DV12
(3) TX9M_DV12
(3) TX9P_DV12
(13) TXCP_DV12
(13) TXCM_DV12

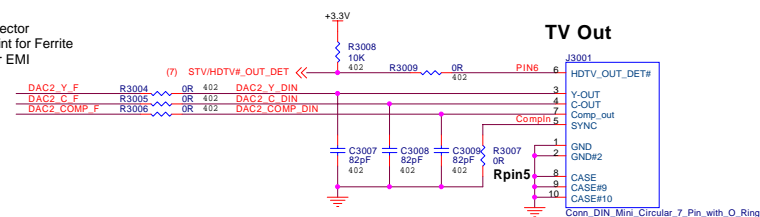
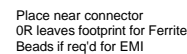
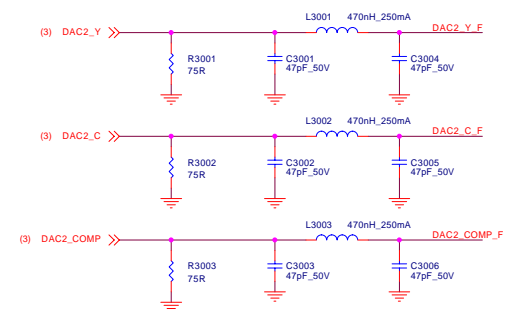
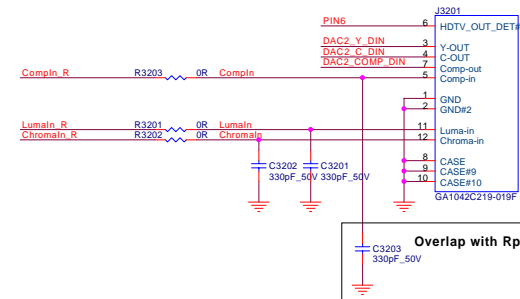
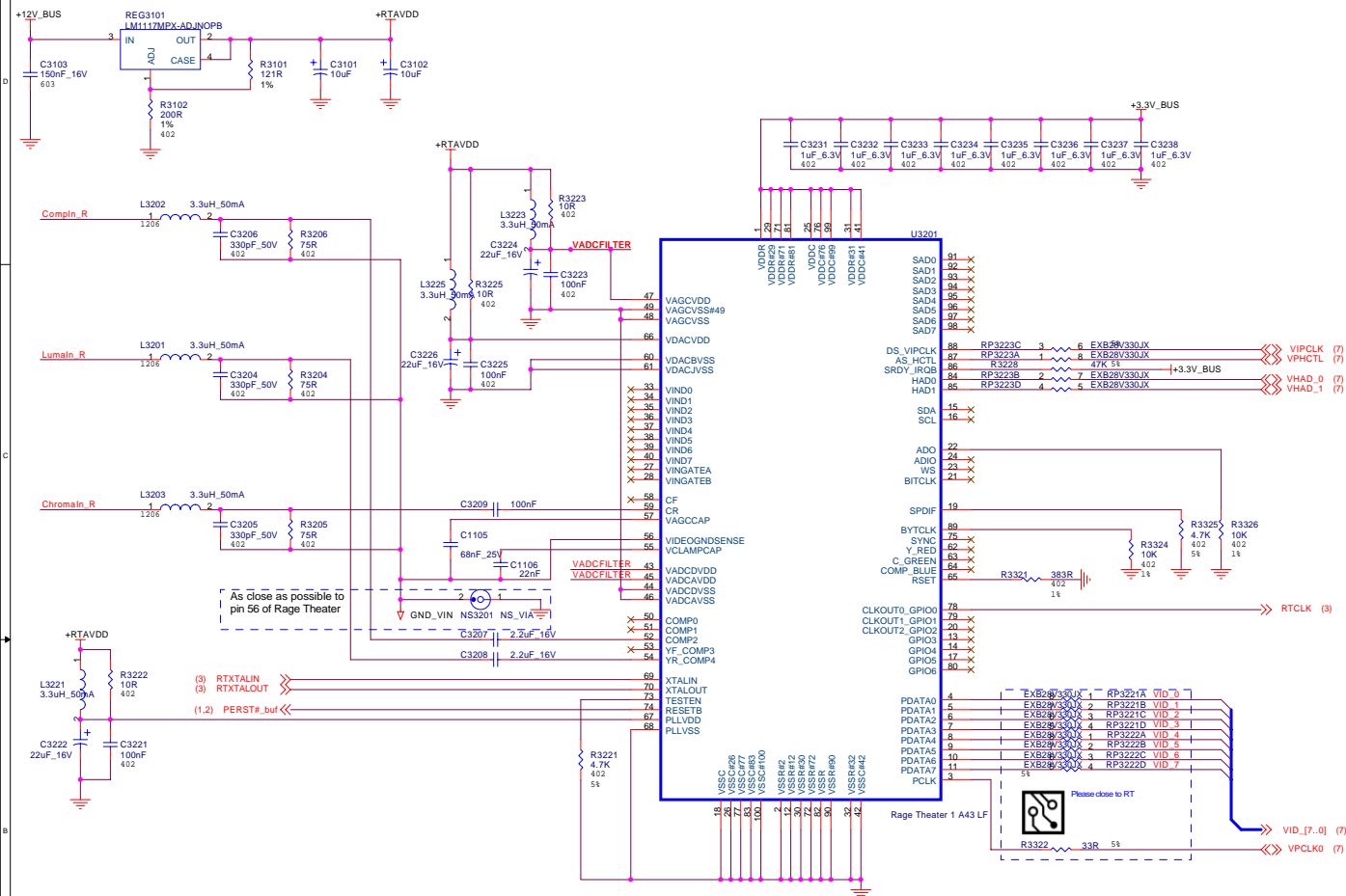
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
A_HSYNC_DAC2_R

| DB15 pin | Standard VGA | DDC1 Host | DDC2B or DDC2B+ Host | DDC2AB Host | DDC1/2 Display |
|------------------|------------------|------------------|----------------------|------------------|----------------|
| 11 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Optional |
| 12 | Monitor ID bit 1 | Monitor ID bit 1 | Monitor ID bit 1 | Monitor ID bit 1 | Optional |
| 4 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Optional |
| 15 | Monitor ID bit 3 | Open | Monitor ID bit 3 | Monitor ID bit 3 | Optional |
| 9 | N/C | +5V | +5V | +5V | Optional |
| Hardware Support | No | Yes | Yes | No | Yes |

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



+RTAVDD
Vout = 3.3V
Iout = 125mA MAX, 80mA RMS



The 7-pin MiniDIN footprint allows one of the two MiniDINs:

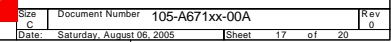
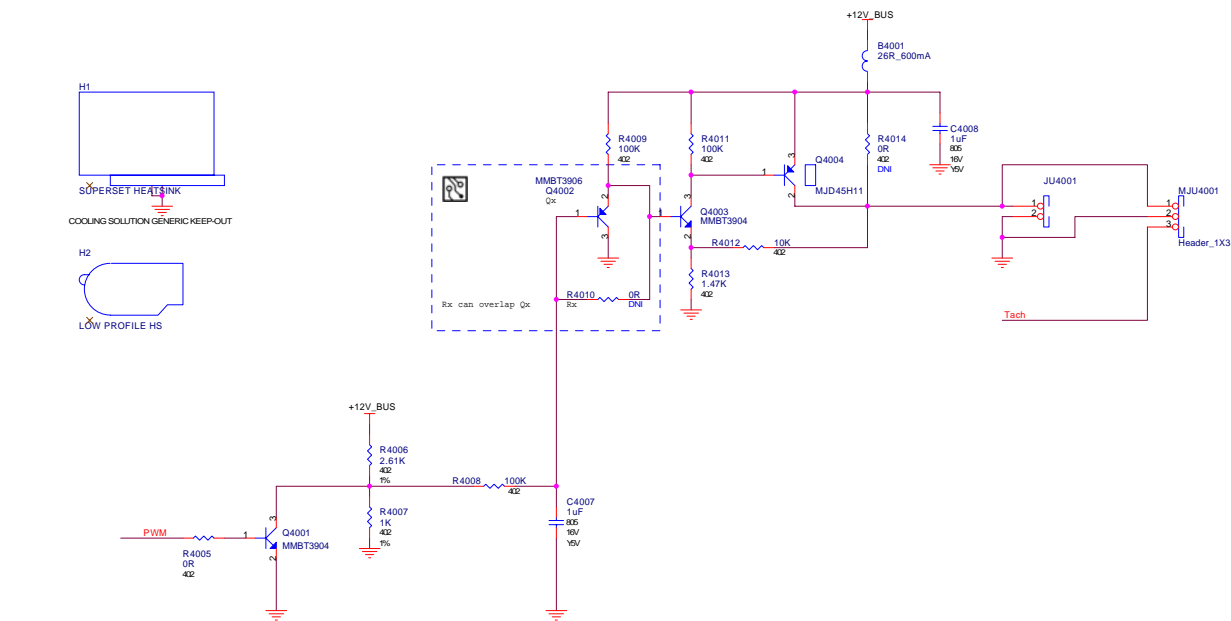
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G



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| | | | | | | | |
|-------|--|-----------------|--|---|--|----------------|--|
| Title | | | | RV530/RV515 256MB DDR3-136 Dual 2xDVI VIVO FH | | | |
| Size | | Document Number | | | | Rev | |
| C | | 105-A671xx-00A | | | | 0 | |
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DVI/VGA SCREWS

- ASSY-SCREW1

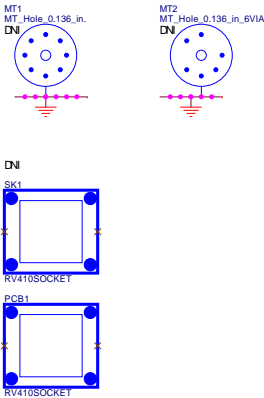
SCREW
JACKSCREW
ASSY
7020000800
- ASSY-SCREW2

SCREW
JACKSCREW
ASSY
7020000800
- ASSY-SCREW5

SCREW
PAN_HEAD
7020001700
- ASSY-SCREW3

SCREW
JACKSCREW
ASSY
7020000800
- ASSY-SCREW4

SCREW
JACKSCREW
ASSY
7020000800



<Variant Name>



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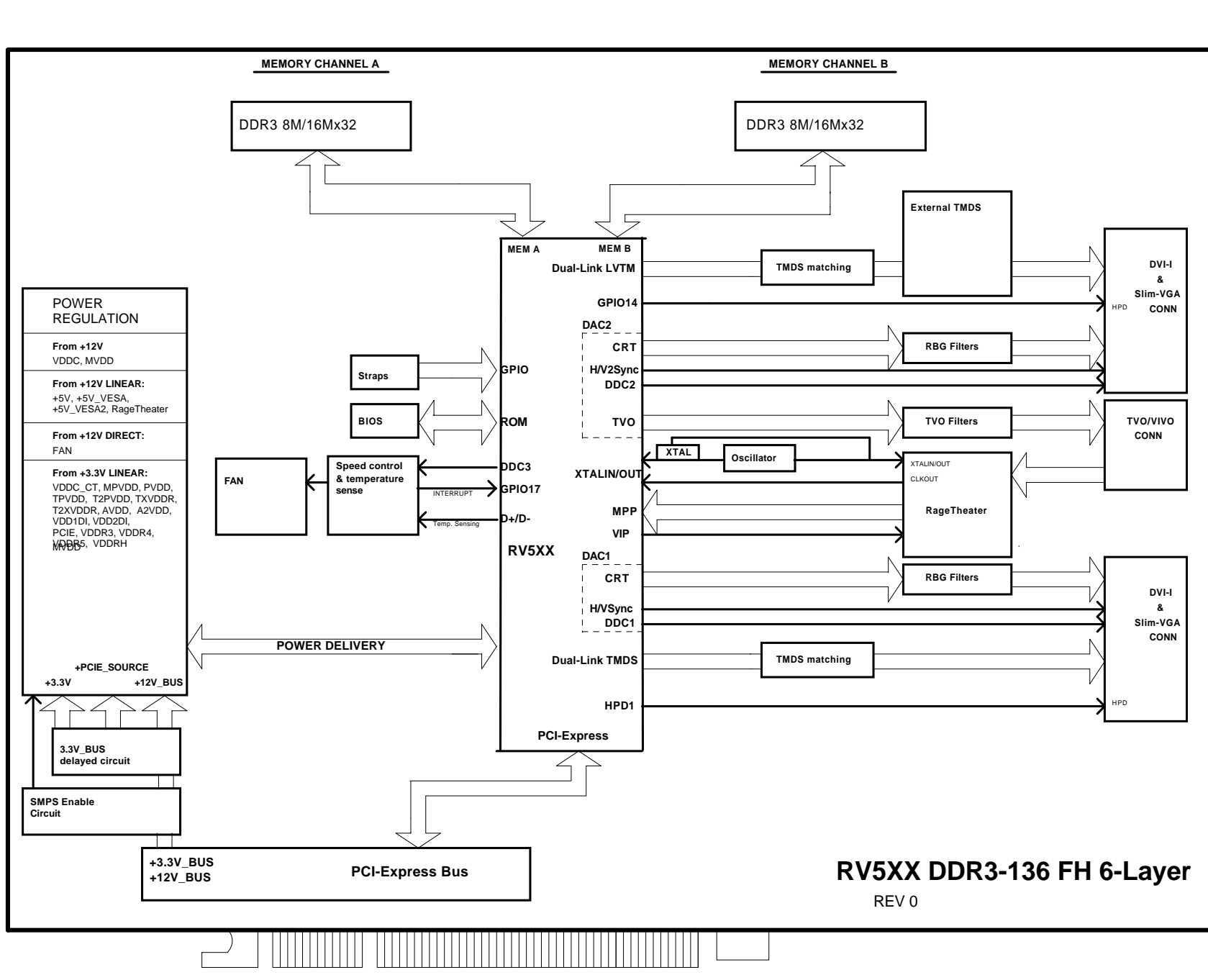


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| Title | Schematic No. | Date: |
| RV530/RV515 256MB DDR3-136 Dual 2xDVI VIVO FH | 105-A671xx-00A | Saturday, August 06, 2005 |

REVISION HISTORY

Rev 0

| Sch Rev | PCB Rev | Date | REVISION DESCRIPTION |
|---------|---------|----------|--|
| 0 | 00A | 05/07/20 | Design based on A676-00B and memory of A675-00B (pg 01) Delete redundant SMPS_EN circuits (pg 03) Remove TMDS joins and add TMDS2 terminations (pg 04) Add 1.8V option for VDDR4 and VDDR5 (pg 05) Add additional separate MVREF, QS# and address; remove ODT for DDR2 (pg 07) Add DVO port and GPIO7 for ext TMDS reset (pg 11) Change power sequence circuit for +5V and add 1.8V power supply (pg 12) Add memory based on A675-00B (pg 13) Add ext TMDS HDCP support (pg 14) Remove HPD2 option (pg 15) Add 2nd DVI connector (pg 16) Remove C3241, C3242, C3243, C3244 and C3245. Remove +MVDDC/+MVDDQ reference, use only +MVDD |



RV5XX DDR3-136 FH 6-Layer

REV 0



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