

PG142-B00


DP + DP + DP + HDMI/DP

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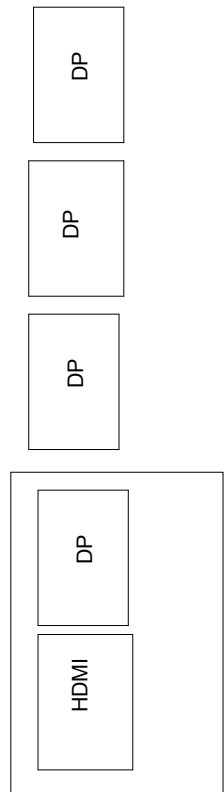


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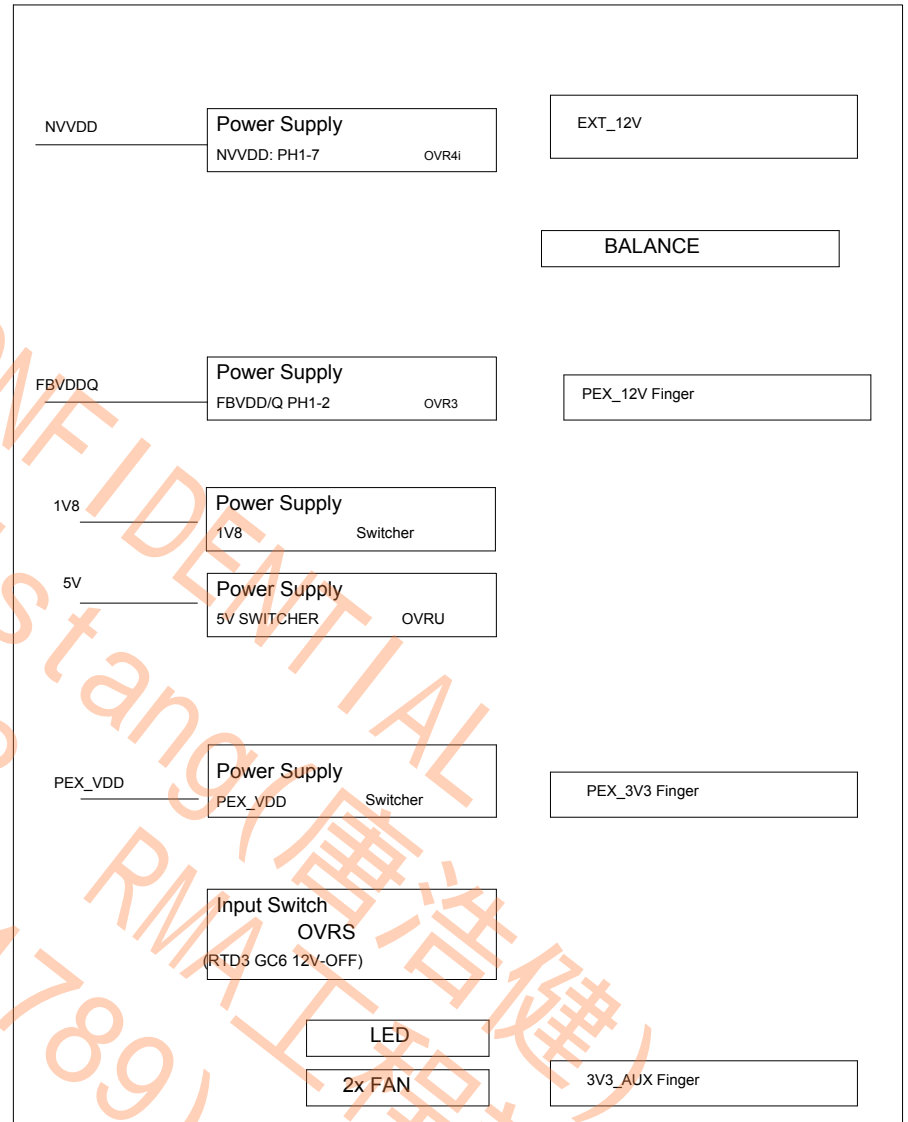
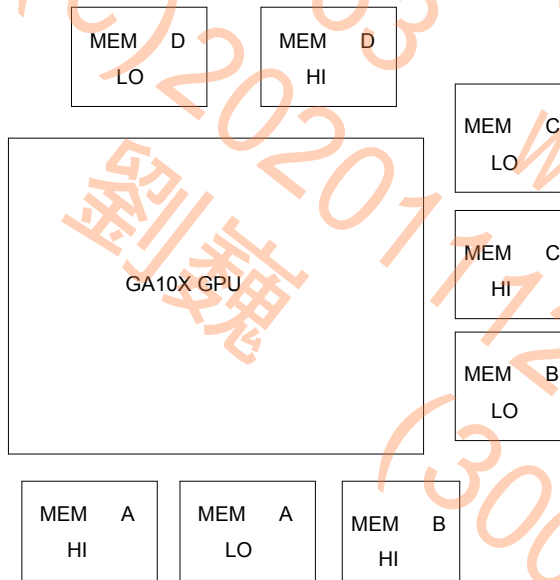
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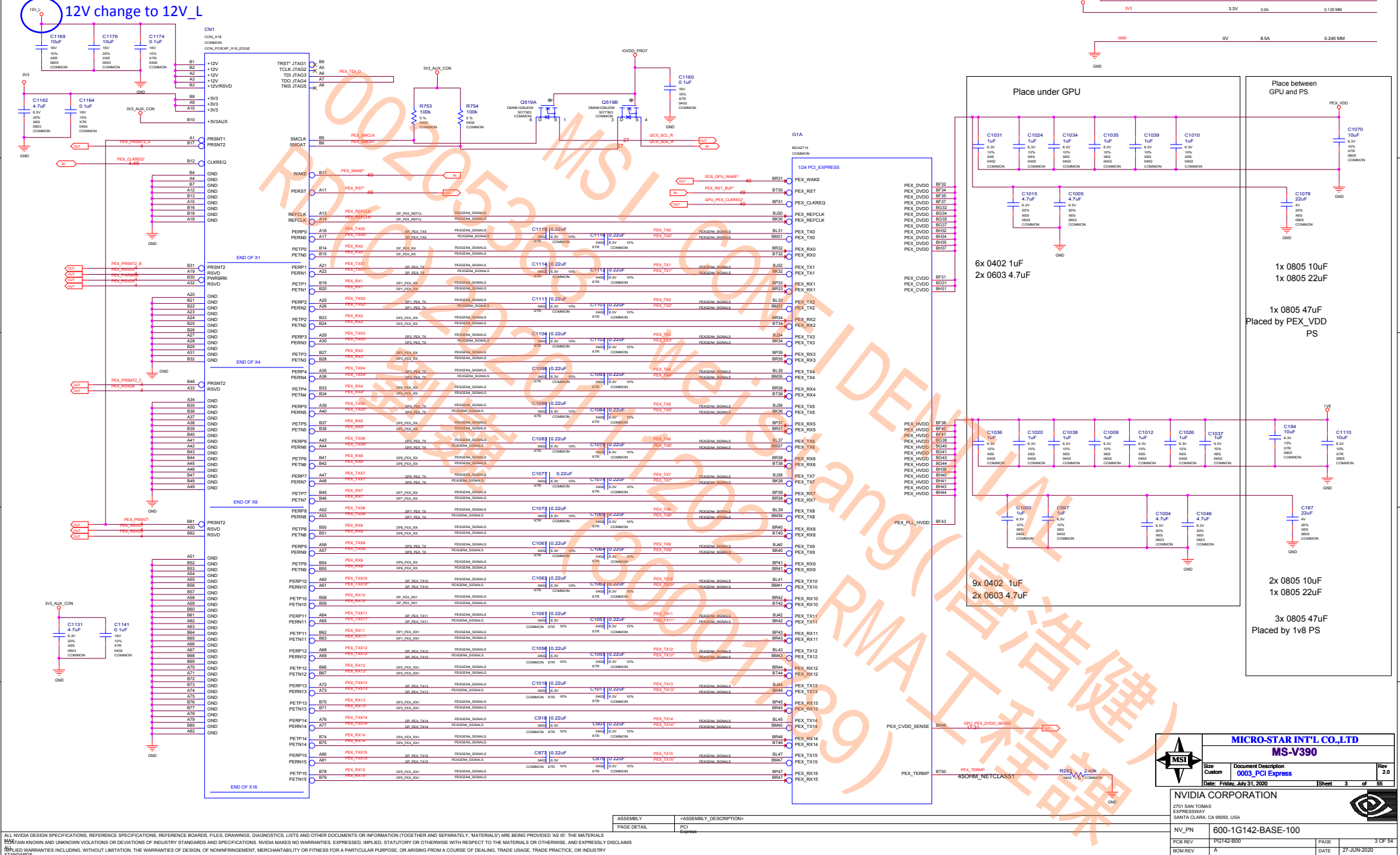
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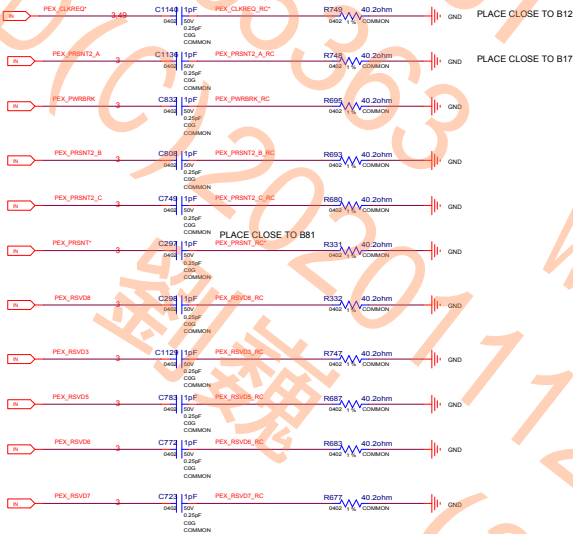
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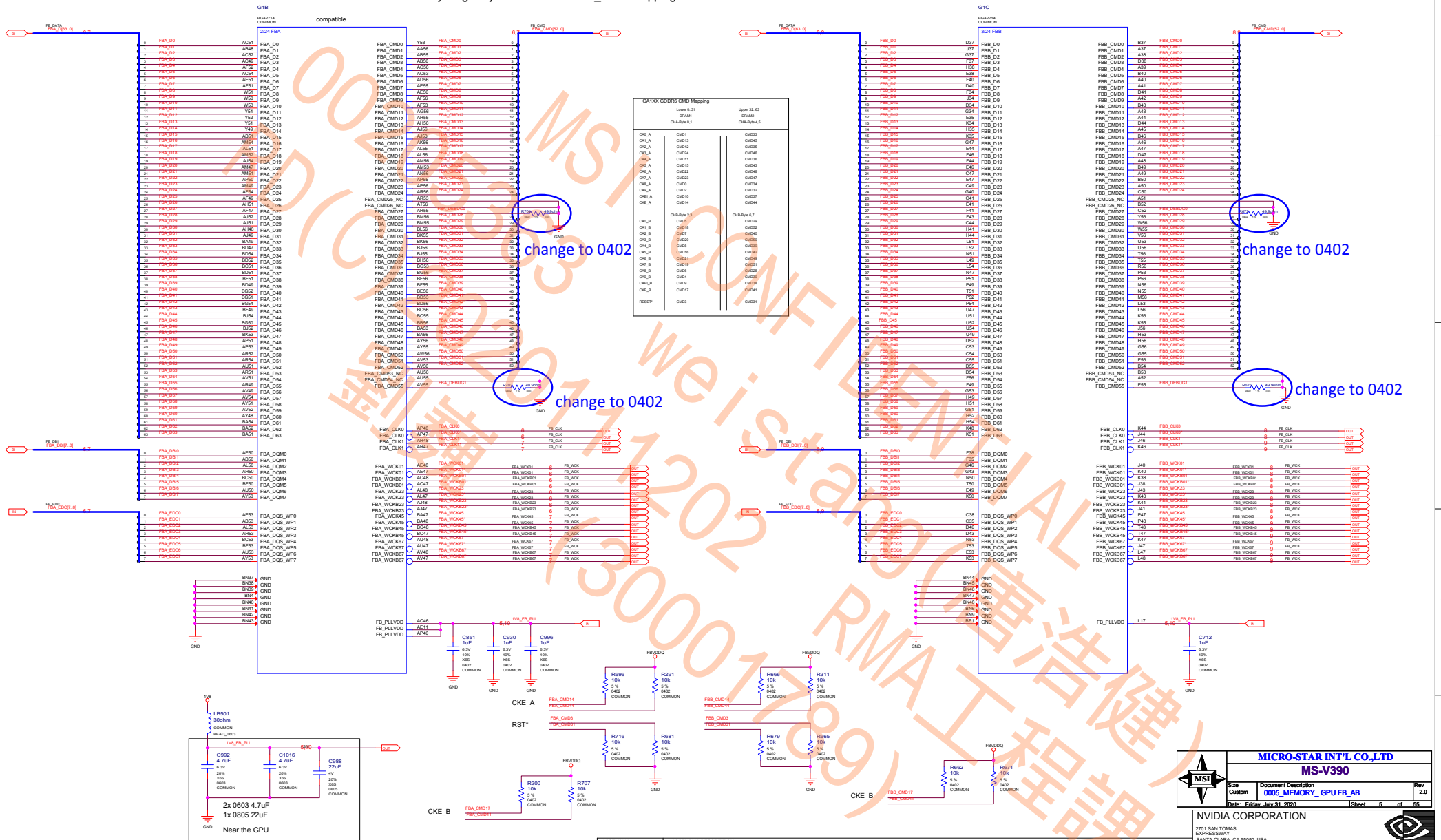
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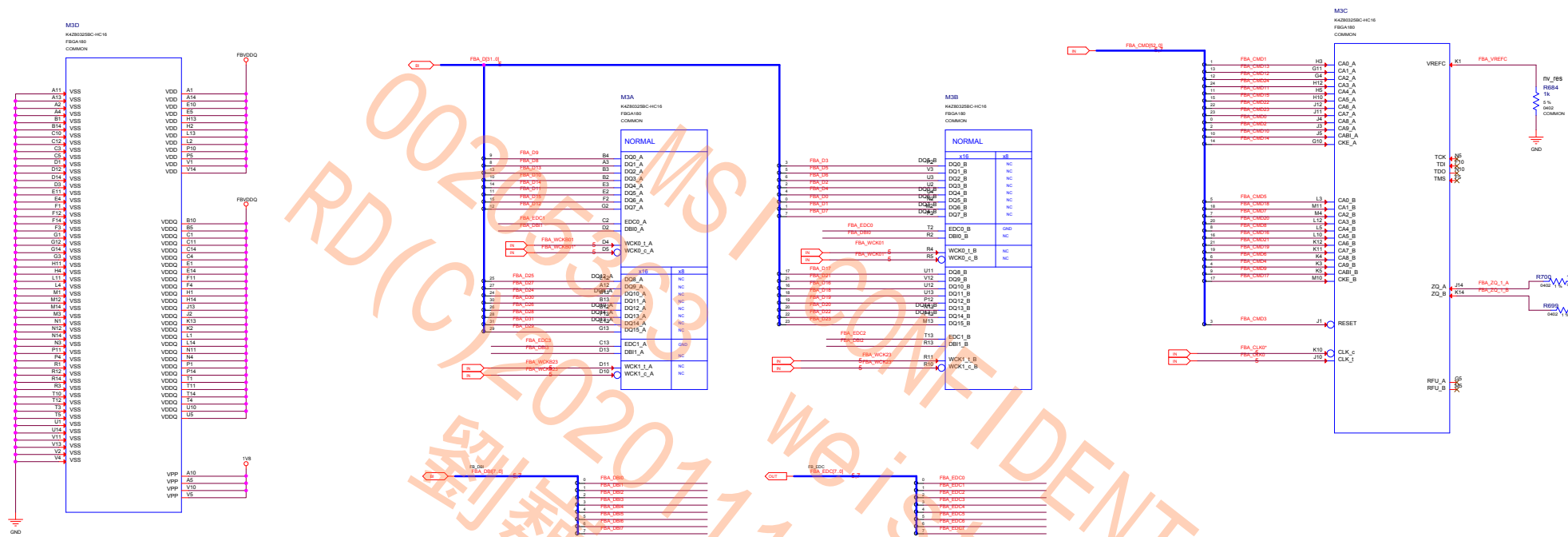
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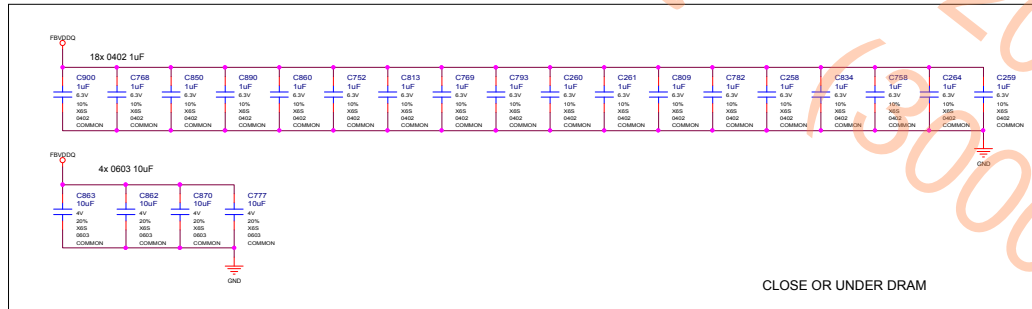
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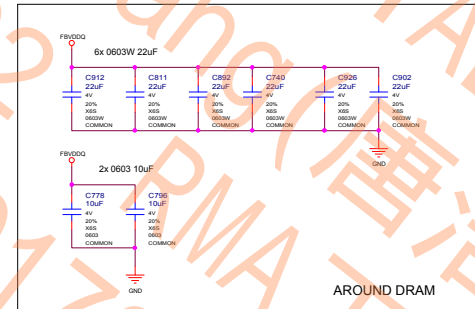
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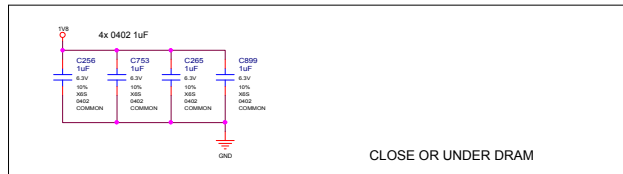
decap via : at least 2 gnd vias and 2 power vias for each cap



CLOSE OR UNDER DRAM




AROUND DRAM

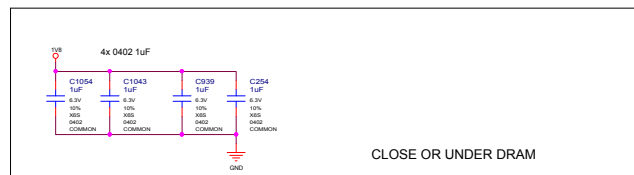
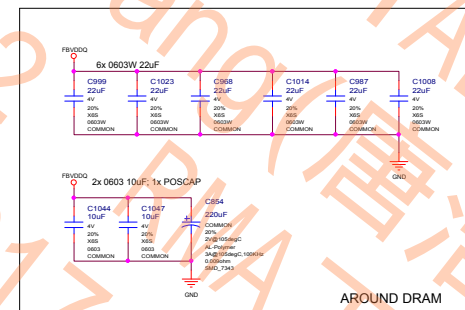
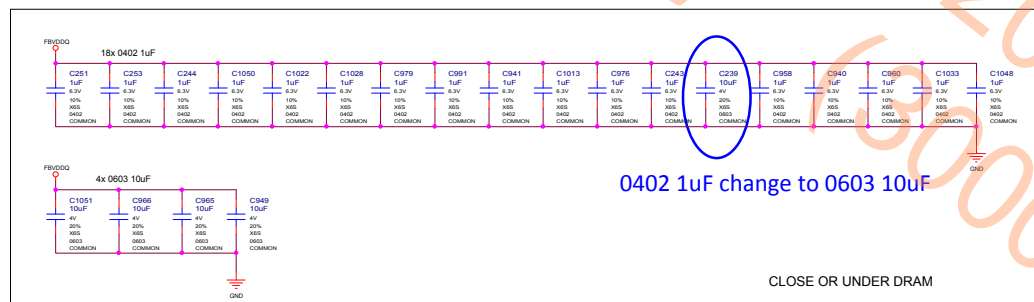
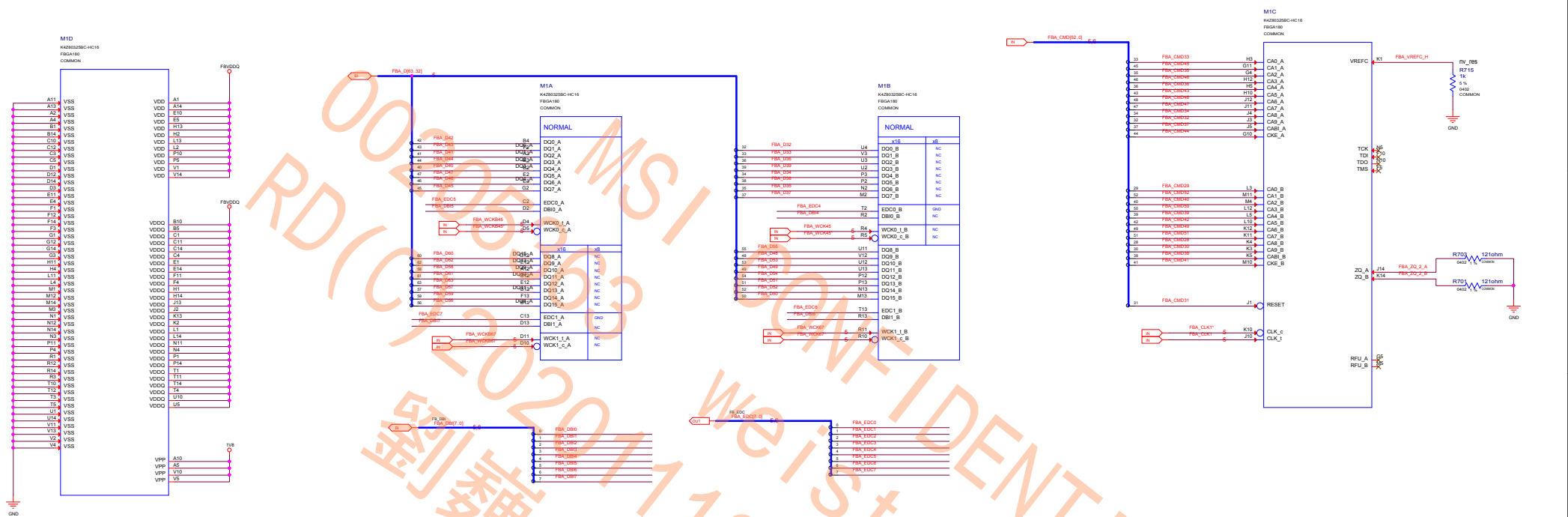


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
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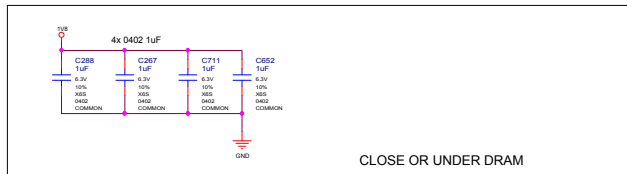
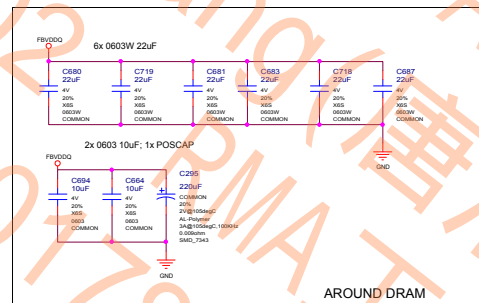
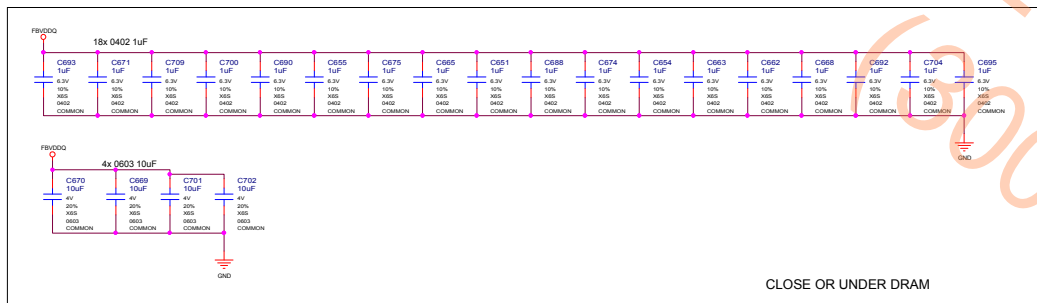
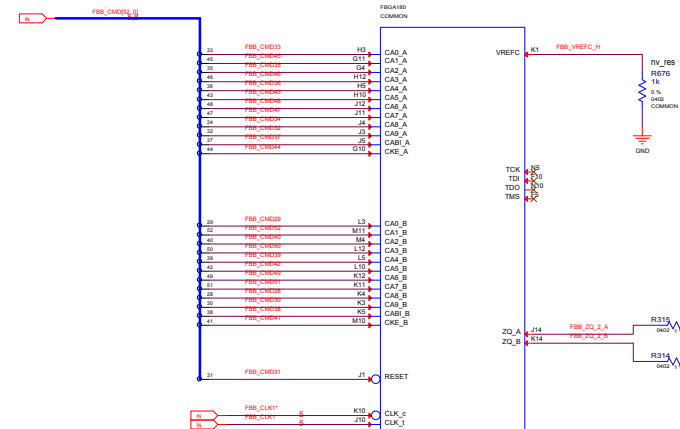
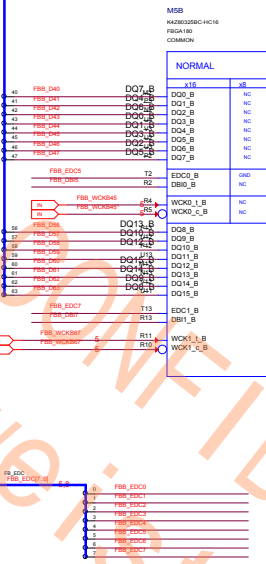
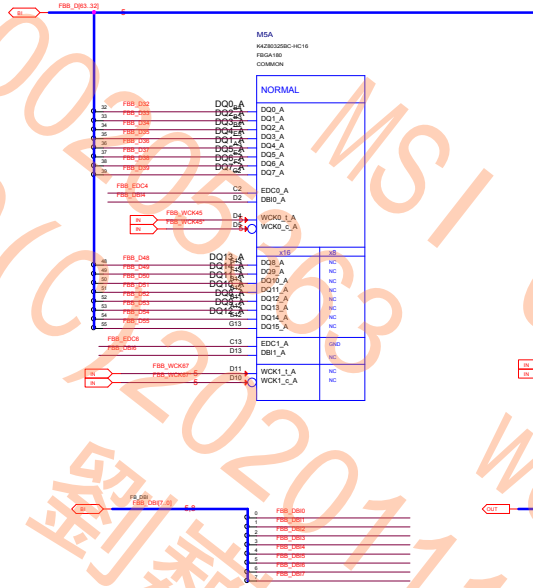
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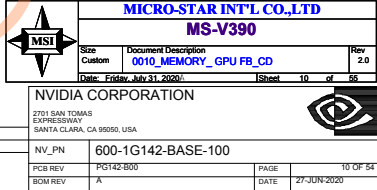


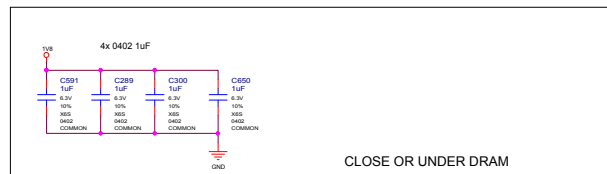
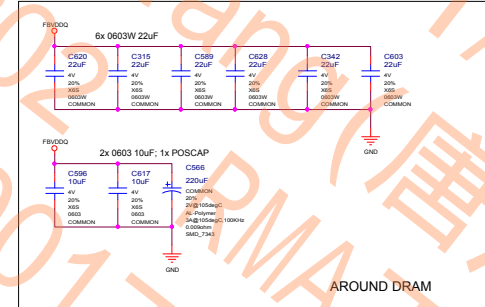
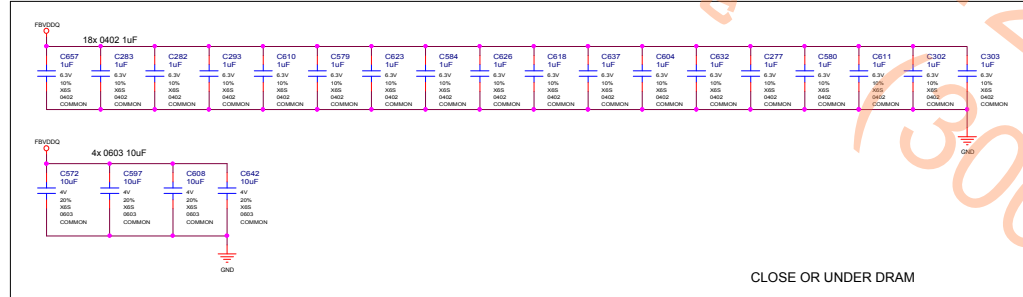





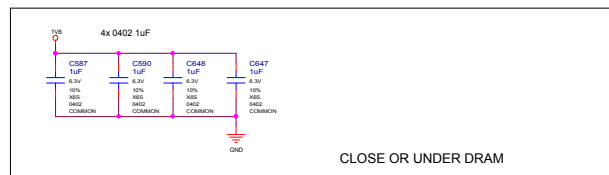
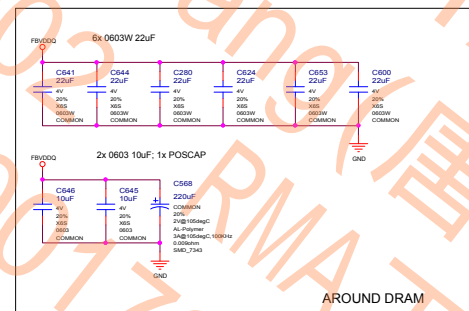
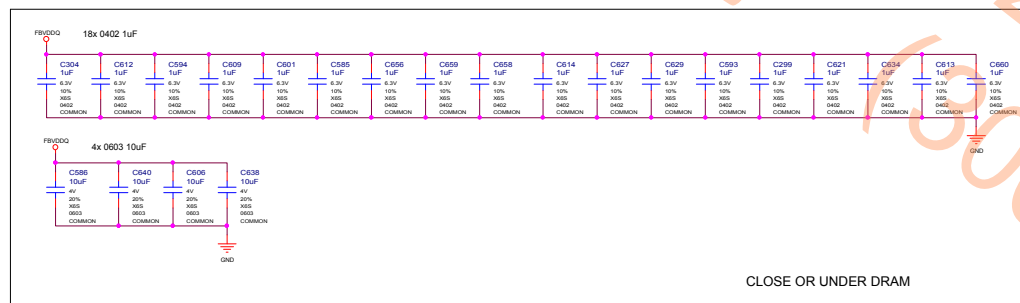
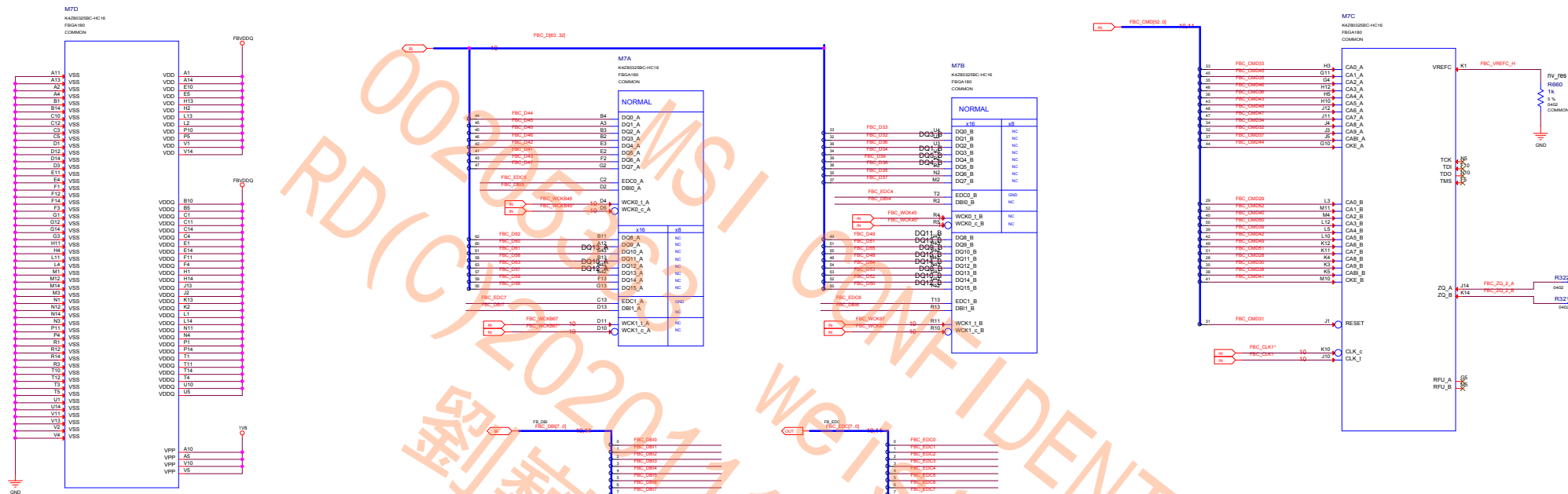
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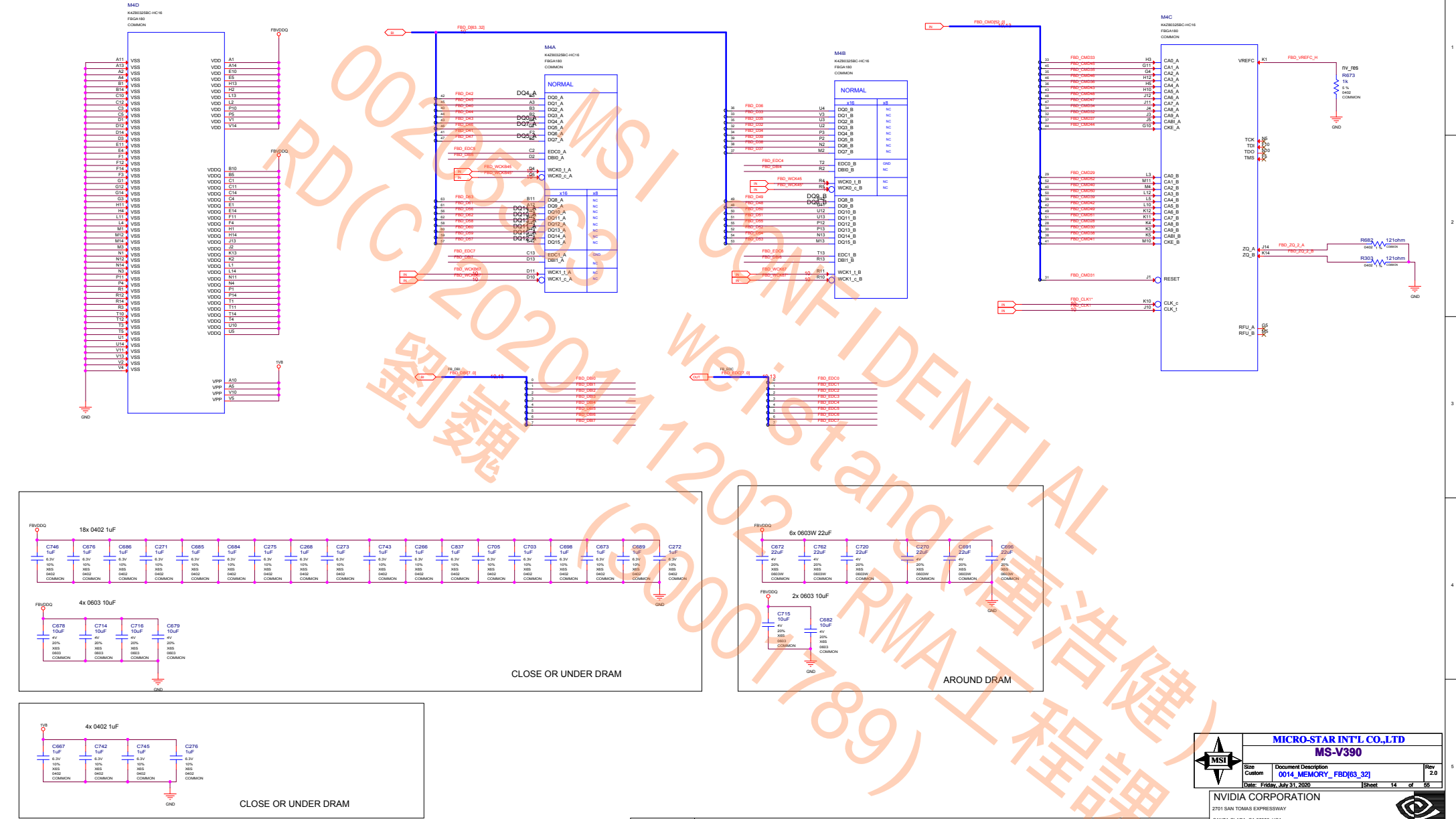


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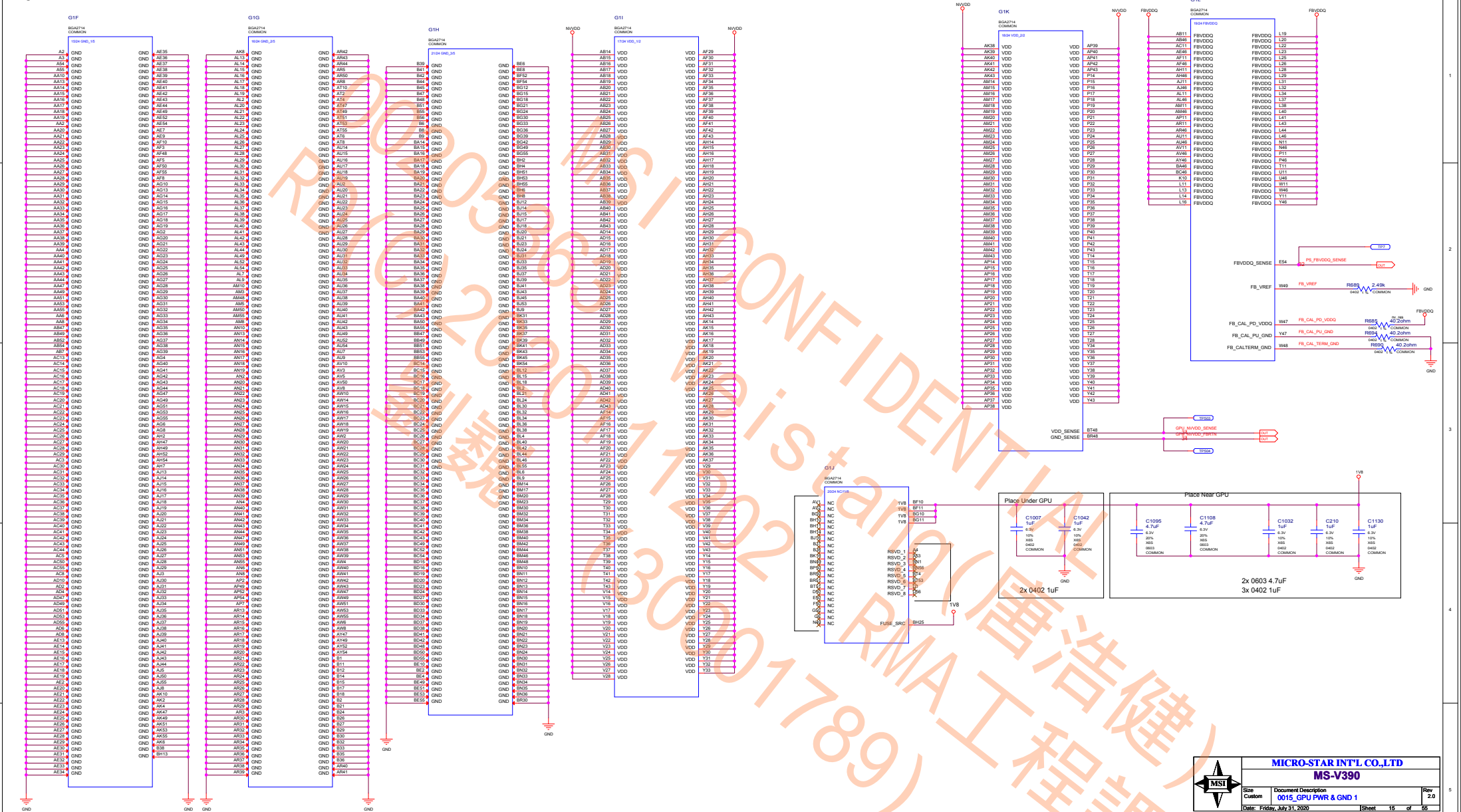
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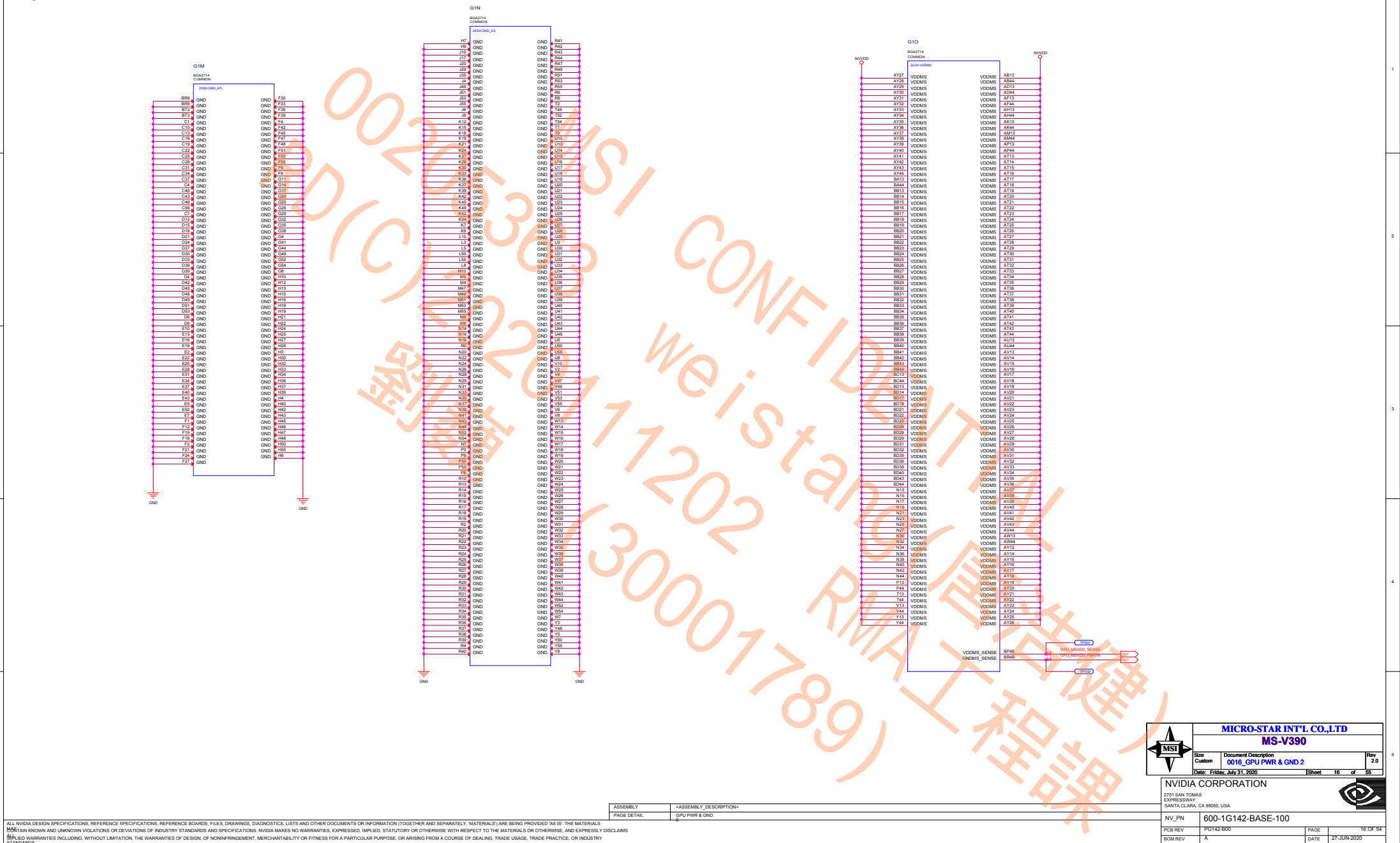




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ASSEMBLY  
PAGE DETAIL


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GPU PWR & GND

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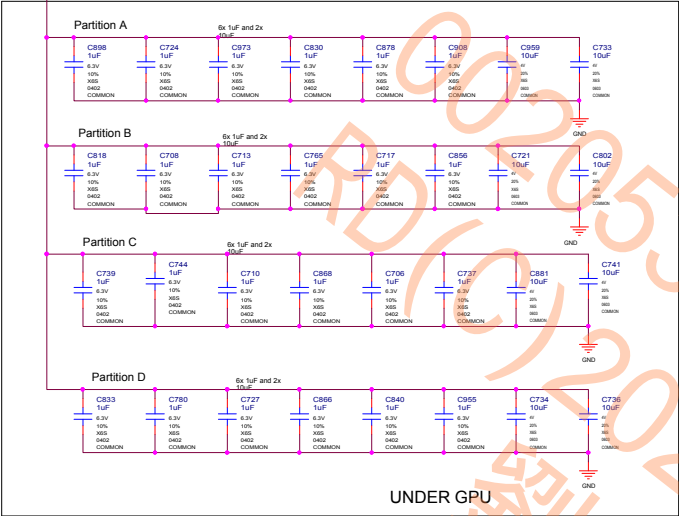
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FBVDDQ

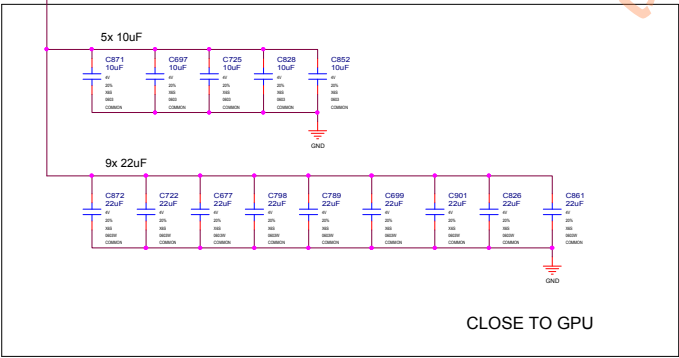
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UNDER GPU

FBVDDQ


5x 0603 10uF; 9x 0603 22uF




CLOSE TO GPU

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PAGE DETAIL	GPU DECOUPLING FBVDDQ

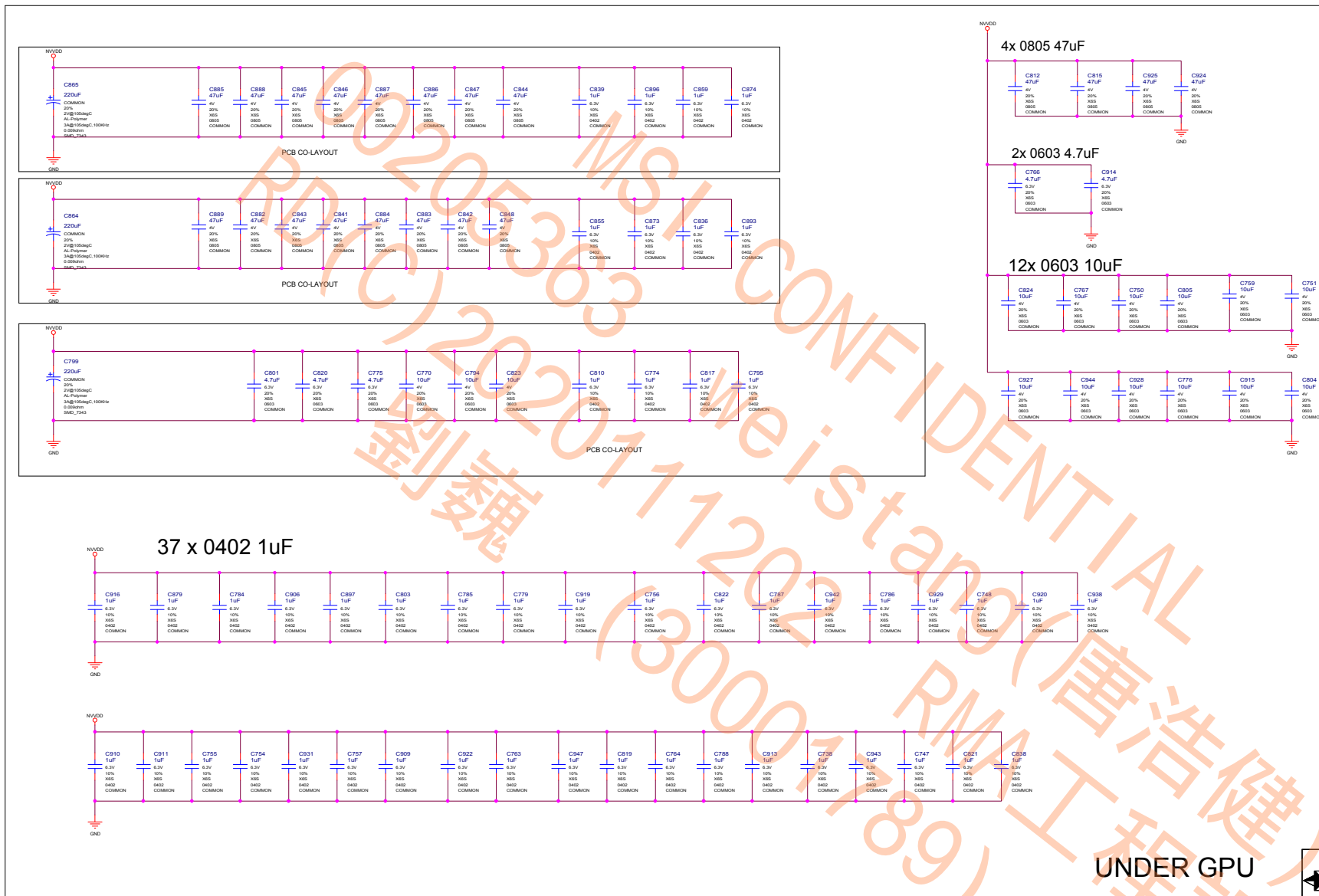


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Size	Document Description	Rev	
Custom	0018_GPU DECOUPLING FBVDDQ	2.0	
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NV_PN	600-1G142-BASE-100		
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BOM REV	A	DATE	27-JUN-2020

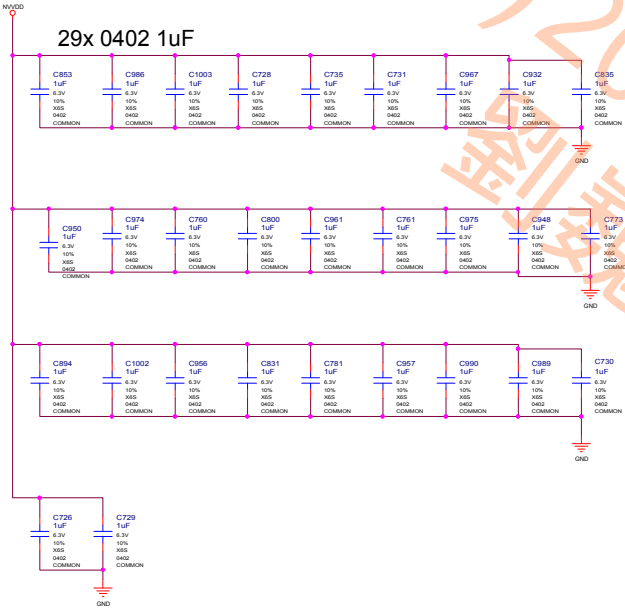
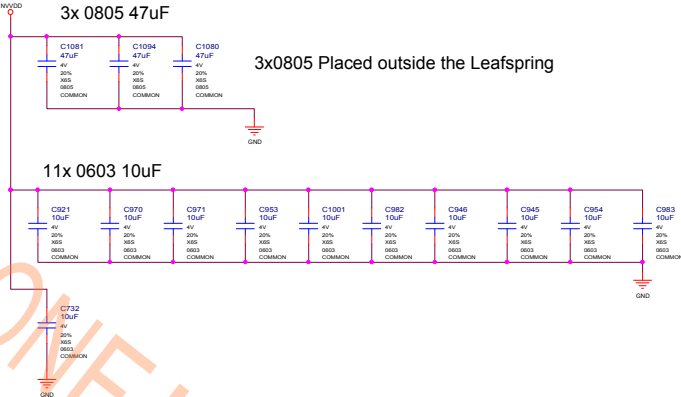
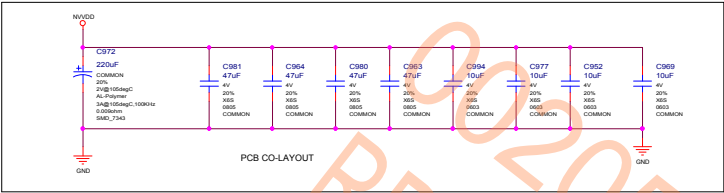


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ASSEMBLY  
PAGE DETAIL

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GPU DECOUPLING NVVDD

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UNDER GPU



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Size: Custom

Document Description: 0020\_GPU DECOUPLING NVVDD

Rev: 2.0


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NV\_PN: 600-1G142-BASE-100

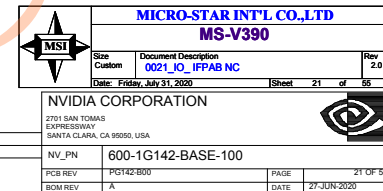
PCB REV: A

ICOM REV: A

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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
		TBD		

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

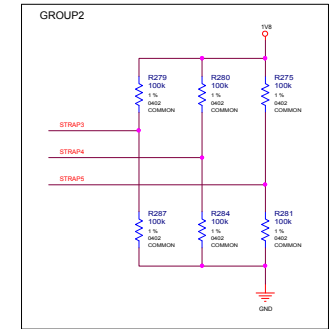
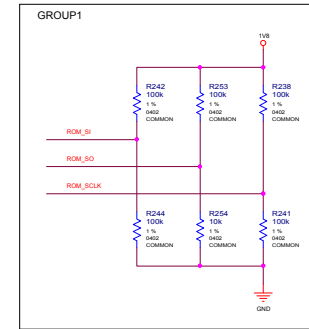
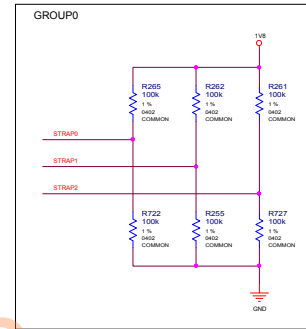
ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0]FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
H	H	M	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
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L	L	L	0	0	0	0

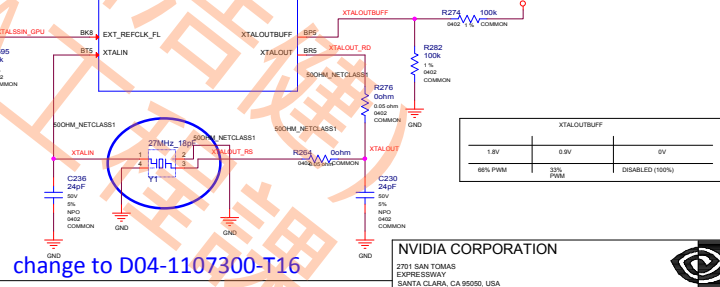
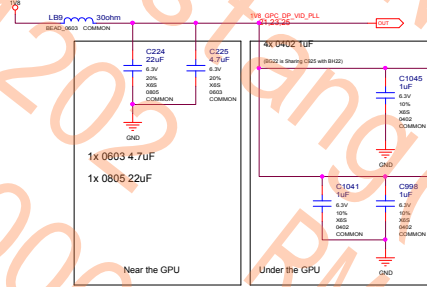
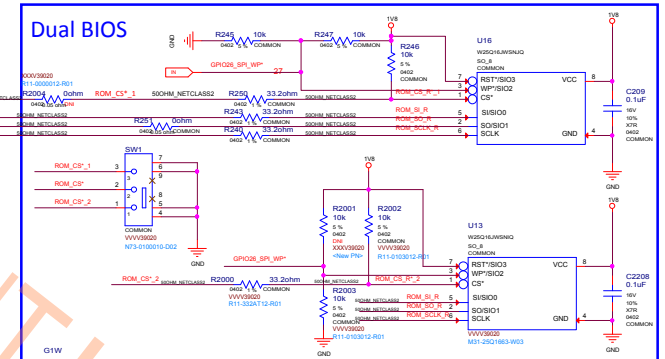
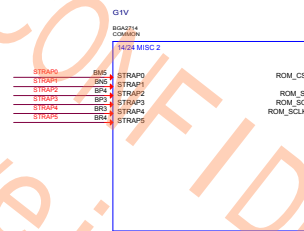
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



DEFAULT



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Size	Document Description	Rev
Custom	0026_MISC1_ROMx2_XTAL_STRAPS	2.0
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ASSEMBLY	*ASSEMBLY DESCRIPTION*	
PAGE DETAIL	MISC1: ROM, XTAL, STRAPS	

change to D04-1107300-T16

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NV_PN	600-1G142-BASE-100	
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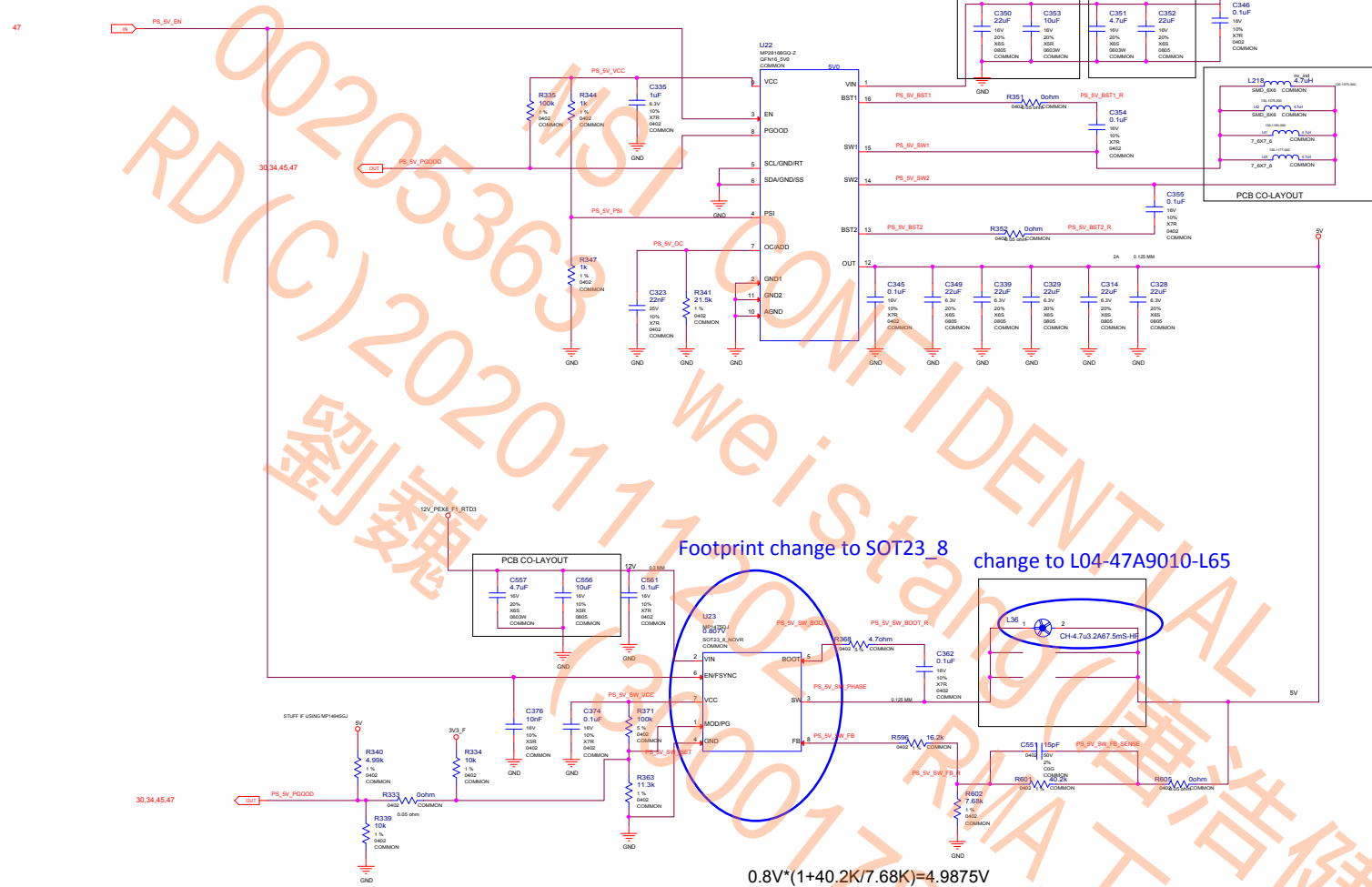
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Date: Friday, July 31, 2020		Sheet 28 of 55	
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NV_PN	600-1G142-BASE-100		
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C1206 change to C0805


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	Date: <b>Friday, July 31, 2020</b>		Sheet <b>29</b> of <b>50</b>
	<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA		
<b>NV_PN</b> <b>600-1G142-BASE-100</b>			
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		<b>0030_PSB_5V</b>	<b>2.0</b>
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nv_PV	<b>600-1G142-BASE-100</b>	
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HF change to OL4-V390002-L65

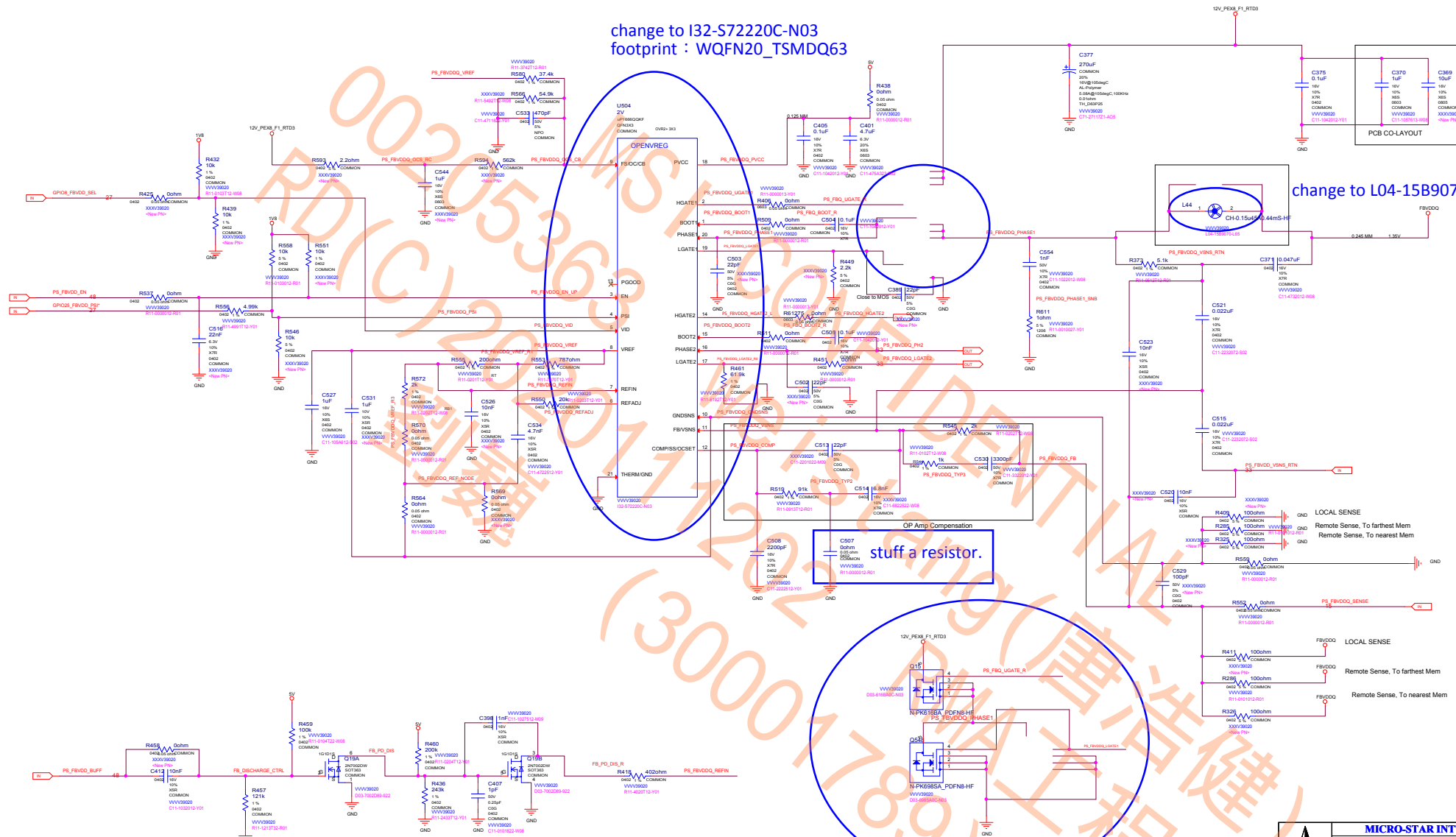
C1206 change to C0805

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	Date: <b>Friday, July 31, 2020</b>		Sheet <b>31</b> of <b>35</b>
<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
			
<b>NV_PN</b> <b>600-1G142-BASE-100</b>			
PCB REV	P0142-B00	PAGE	31 OF 54
BOM REV	A	DATE	21-JUN-2020


change to I32-S72220C-N03  
footprint : WQFN20\_TSMDQ63

change to L04-15B9070-L65

stuff a resistor.



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**NV\_PN** 600-1G142-BASE-100

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ICOM REV	A	DATE	27-JUN-2020		






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SANTA CLARA, CA 95050, USA			
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BCM REV	A	DATE	27-JUN-2020

NV\_PH4\_6\_VIN change to 12V\_PEX8\_F2

## NVVDD PH4(PWM4)

reverse to public board cap

change to OL4-V390003-L65  
footprint:public board.

delete co-layout MLCC

reverse to public board cap

## NVVDD PH6(PWM6)

reverse to public board cap

U3,U4,U5,U6,U7,U8,U9,U10,U15,U18  
change to I33-302041C-O05  
footprint : PQFN31change to OL4-V390003-L65  
footprint:public board

delete co-layout MLCC

reverse to public board cap

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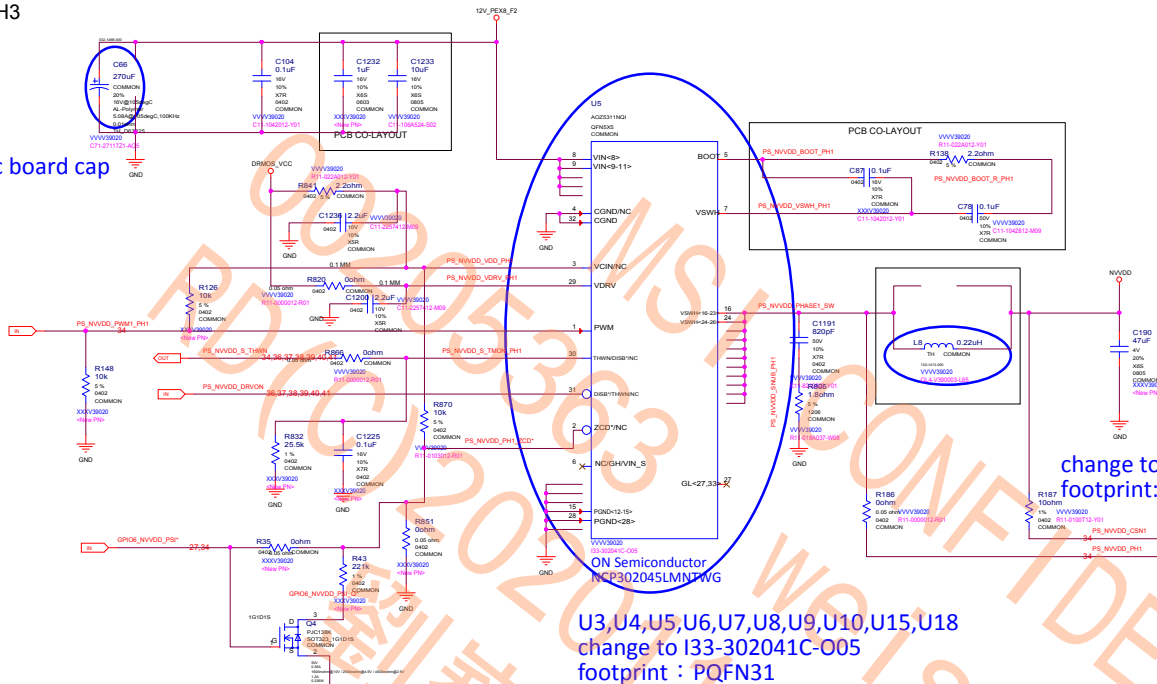
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PAGE DETAIL	PS_NVVDD PH4, PH6

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MS-V390			
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Custom	0036_PS_NVVDD PH4, PH6	2.0	
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NV_PN		600-I-G142-BASE-100	
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## NVVDD PH1(PWM1)

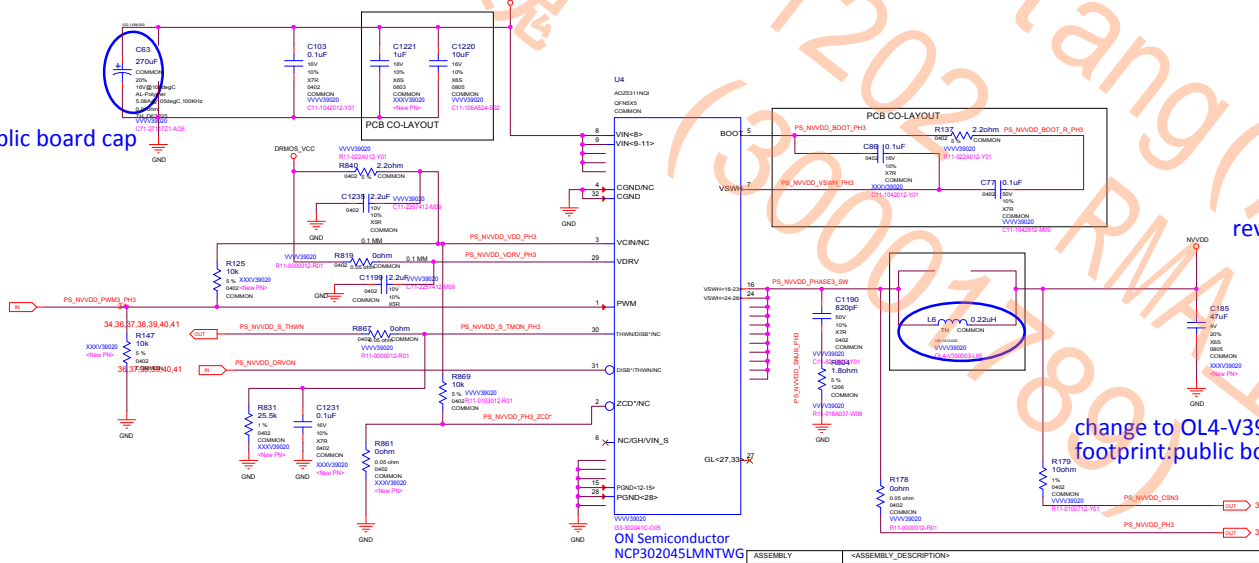
reverse to public board cap



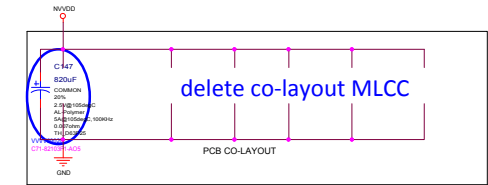
U3,U4,U5,U6,U7,U8,U9,U10,U15,U18  
change to I33-302041C-005  
footprint : PQFN31

## NVVDD PH3(PWM3)

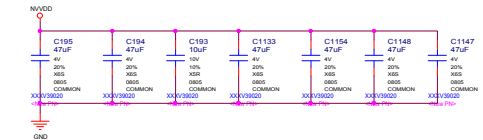
reverse to public board cap



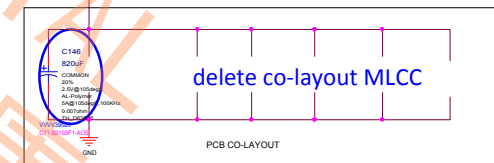
U4  
change to I33-302041C-005  
footprint : PQFN31



reverse to public board cap



change to OL4-V390003-L65  
footprint:public board



reverse to public board cap

colayout only no self standing mlccs

change to OL4-V390003-L65  
footprint:public board

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Size	Document Description	Rev	
Custom	0037_PS_NVDD PH1, PH3	2.0	
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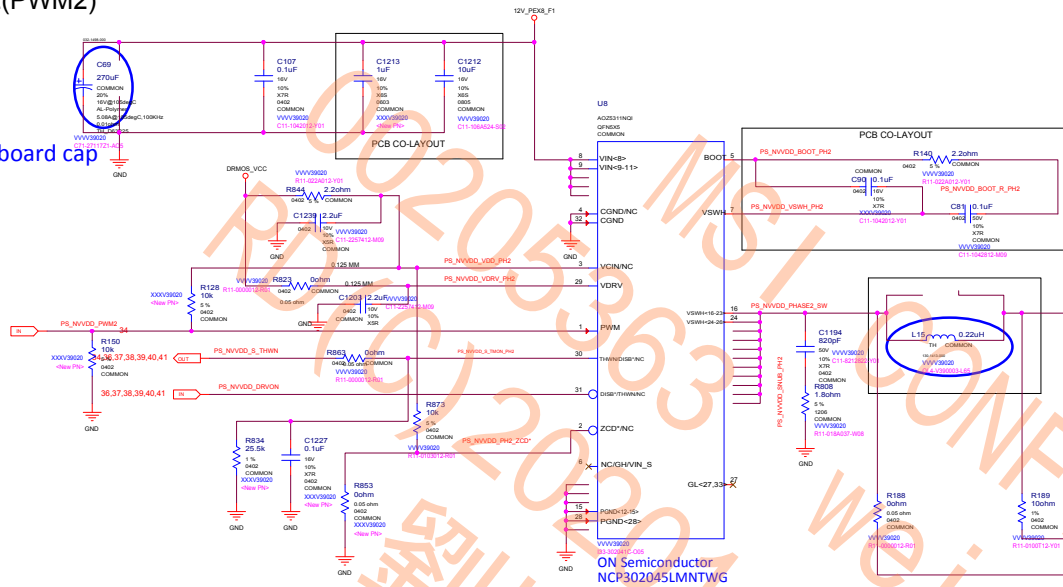


NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
ICOM REV	A
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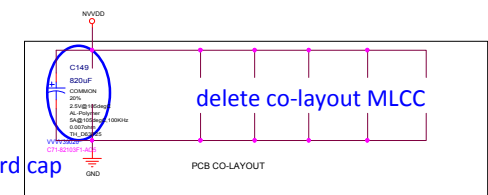
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## NVVDD PH2(PWM2)

reverse to public board cap

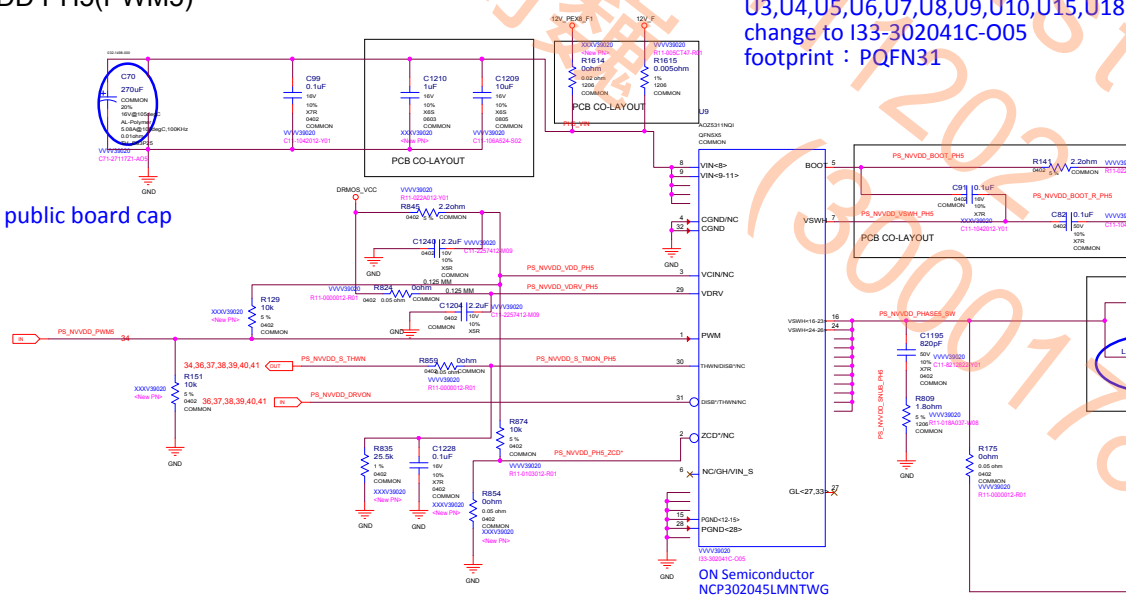


reverse to public board cap



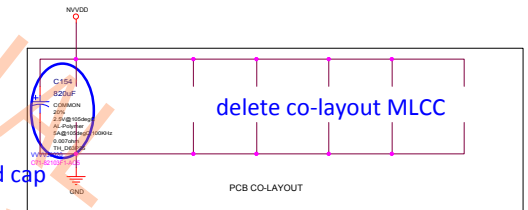
## NVVDD PH5(PWM5)

reverse to public board cap



U3,U4,U5,U6,U7,U8,U9,U10,U15,U18  
change to I33-302041C-005  
footprint : PQFN31

reverse to public board cap



change to OL4-V390003-L65  
footprint:public board

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Size	Custom	Document Description	0038_PS_NVDD PH2, PH5
Date:	Fri, Jul 31, 2020	Rev	2.0
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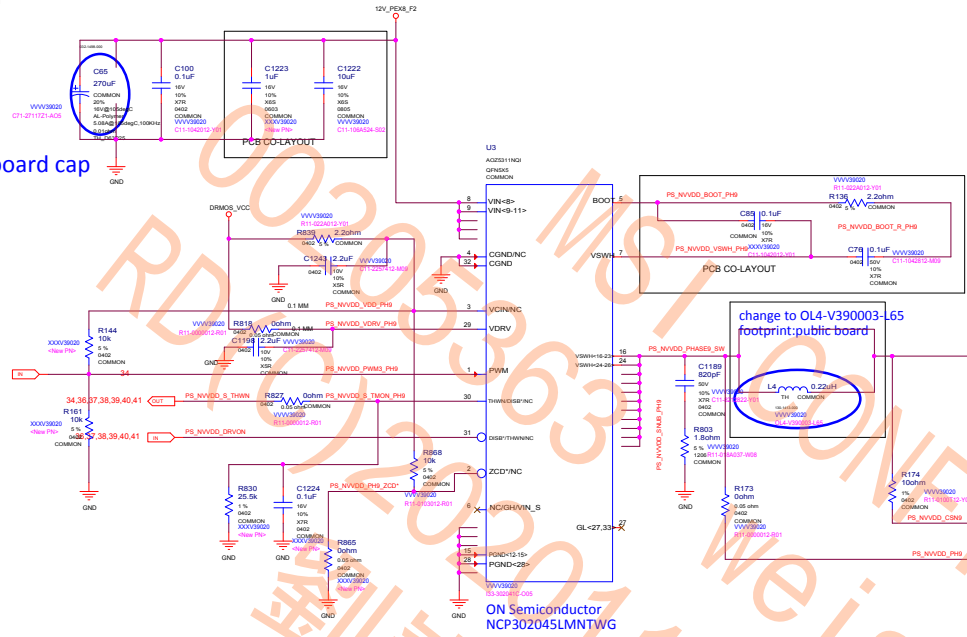
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PCB REV	PG142-B00
ICOM REV	A
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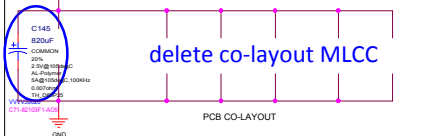
NVVDD PH9(PWM3)

reverse to public board cap



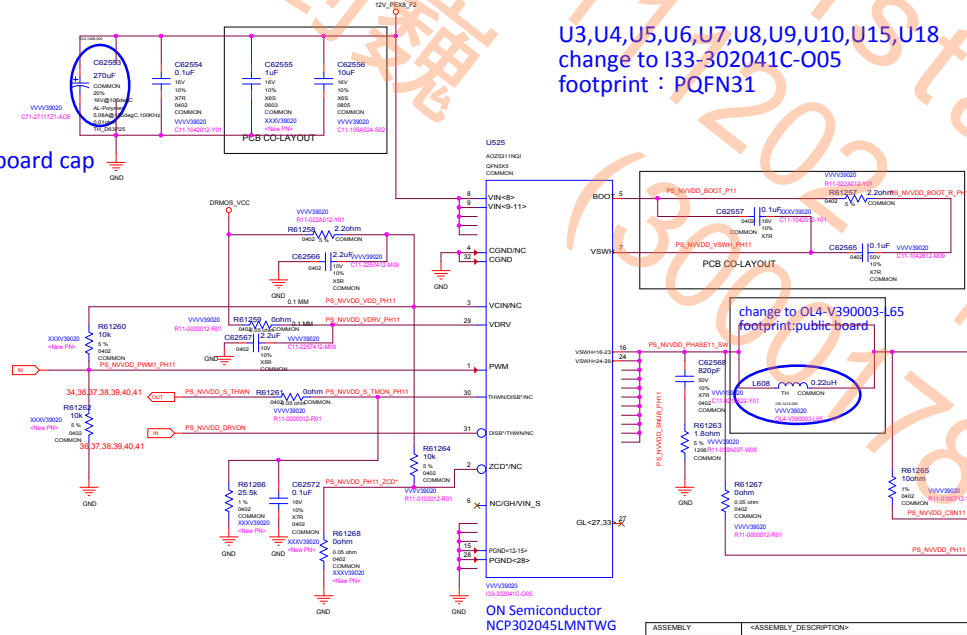
reverse to public board cap

delete co-layout MLCC



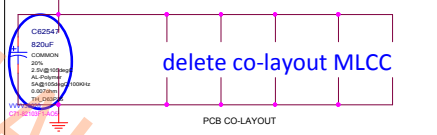
NVVDD PH11(PWM1)

reverse to public board cap



reverse to public board cap

delete co-layout MLCC



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reverse to public board cap

reverse to public board cap

delete co-layout MLCC

change to OL4-V390003-L65  
footprint:public board

NVVDD PH8(PWM8)


reverse to public board cap

U3,U4,U5,U6,U7,U8,U9,U10,U15,U18  
change to I33-302041C-O05  
footprint : PQFN31

delete co-layout MLCC

reverse to public board cap

change to OL4-V390003-L65  
footprint:public board



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POWER CONNECTOR HOT-UNPLUG DETECT

delete POWER CONNECTOR HOT-UNPLUG DETECT


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

delete 12V CURRENT STEERING

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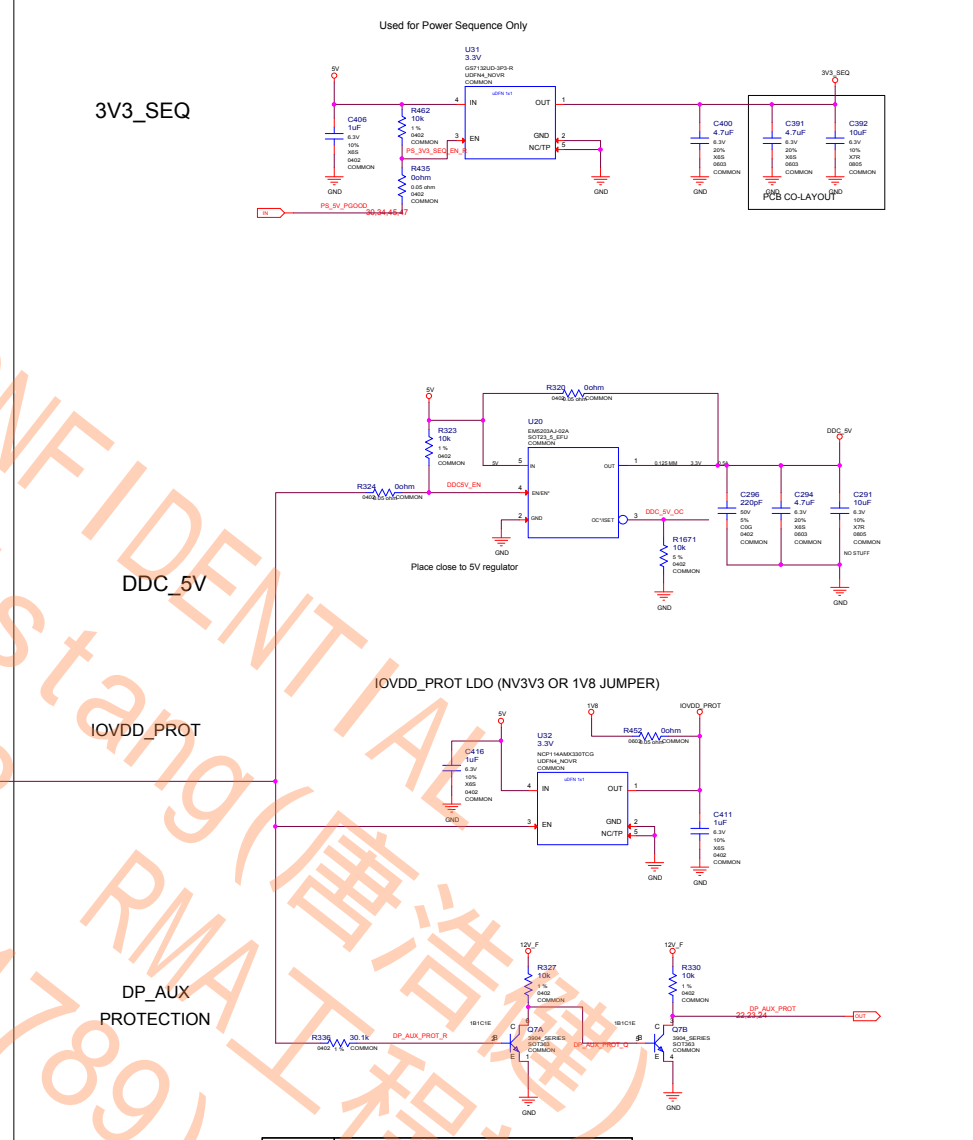
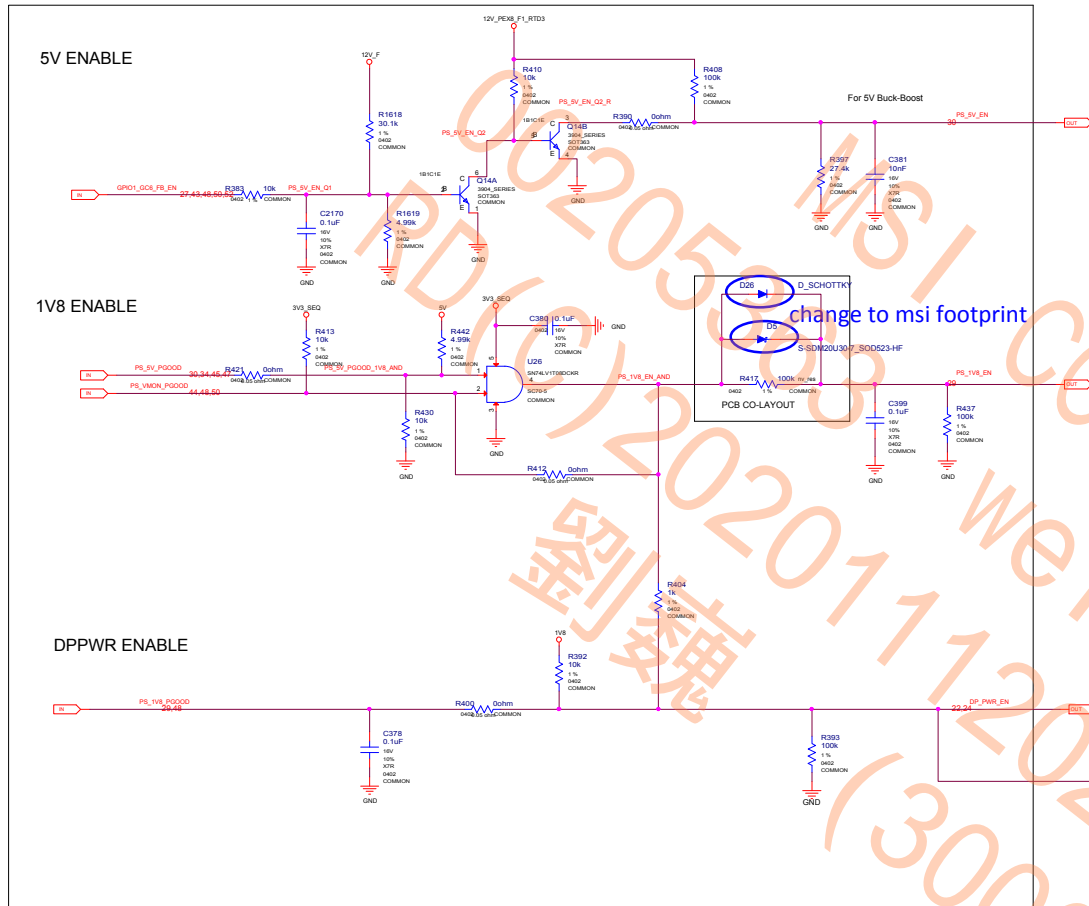
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**MS-V390**  
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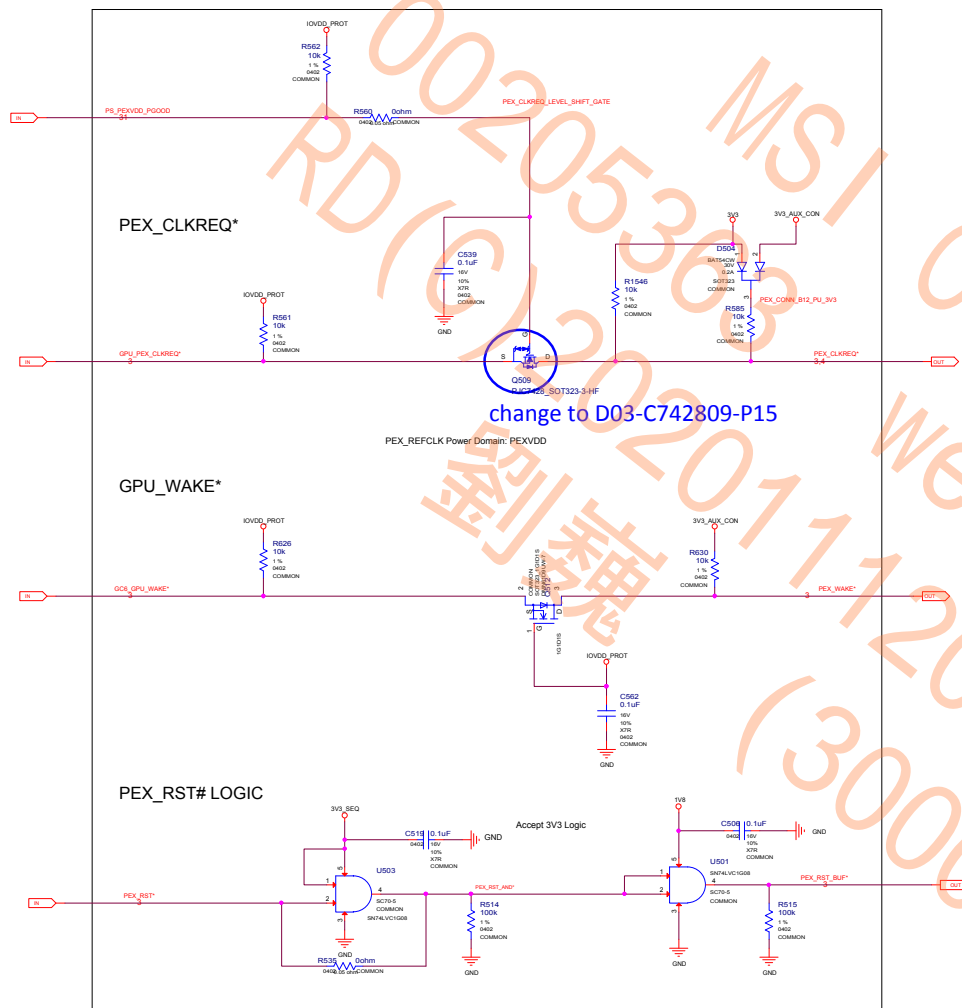
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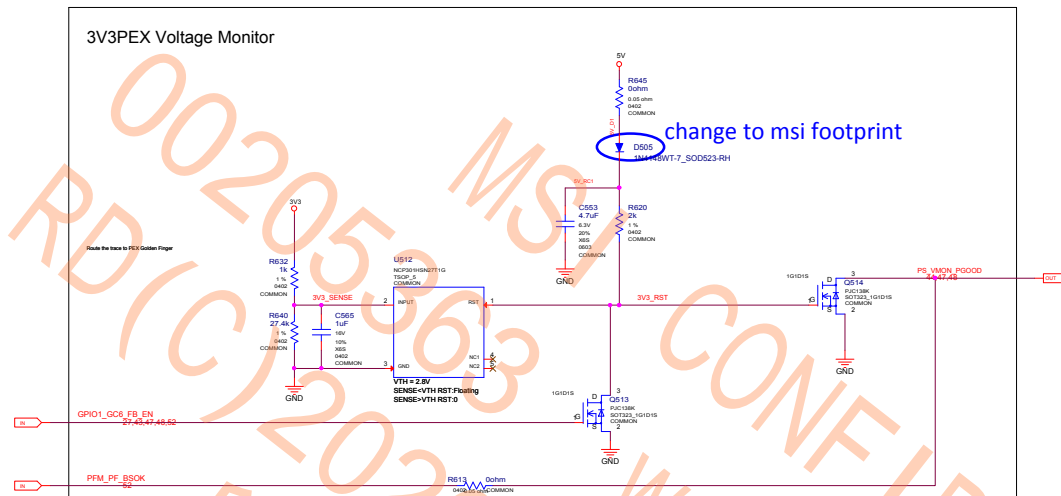
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## BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A


Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
VMON_PG0OD	OPEN-DRAIN	Floting(H) once both 3V3 and 12V reach Vth
GC6_FB_EN		Enable for RTD3/GC6 resistance.Use to Mask the VMON_PG0OD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSK0	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

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	Size	Document Description	Rev
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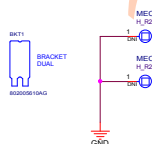
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SV_PN	<b>600-1G142-BASE-100</b>	
TGCR REV	PG142-800	
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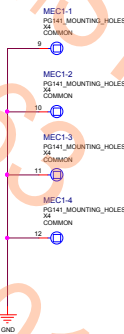




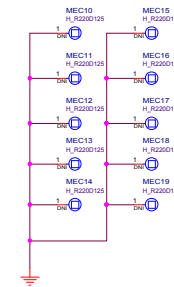
Bracket & Bracket hole: 2pcs  
footprint:H\_R220D125



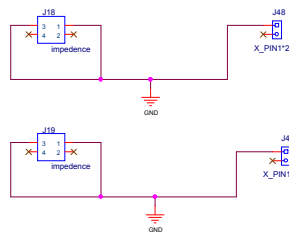
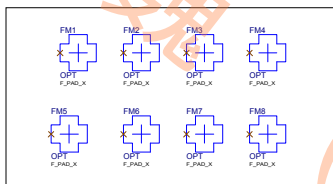
Fan module hole: 4 pcs  
footprint : same as public board



Fan module hole: 10 pcs  
footprint:H\_R220D125



删除CLP1~CLP3



Bracket Screw

BKTSREW1

COMMON

WV93620

P00-0139020-048

E41-1394200-H75

BKTSREW2

COMMON

WV93620

P00-0139020-048

E41-1394200-H75

HDMISCREW1

COMMON

WV93620

P00-0139020-048

E41-1394200-H75



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