

P1077-A01

GF108, GT215/6/8 MXM V3.0 TYPE A 1024/2048MB 128/64-BIT DDR3
LVDS, QUAD DP, DVI, VGA

TABLE OF CONTENTS

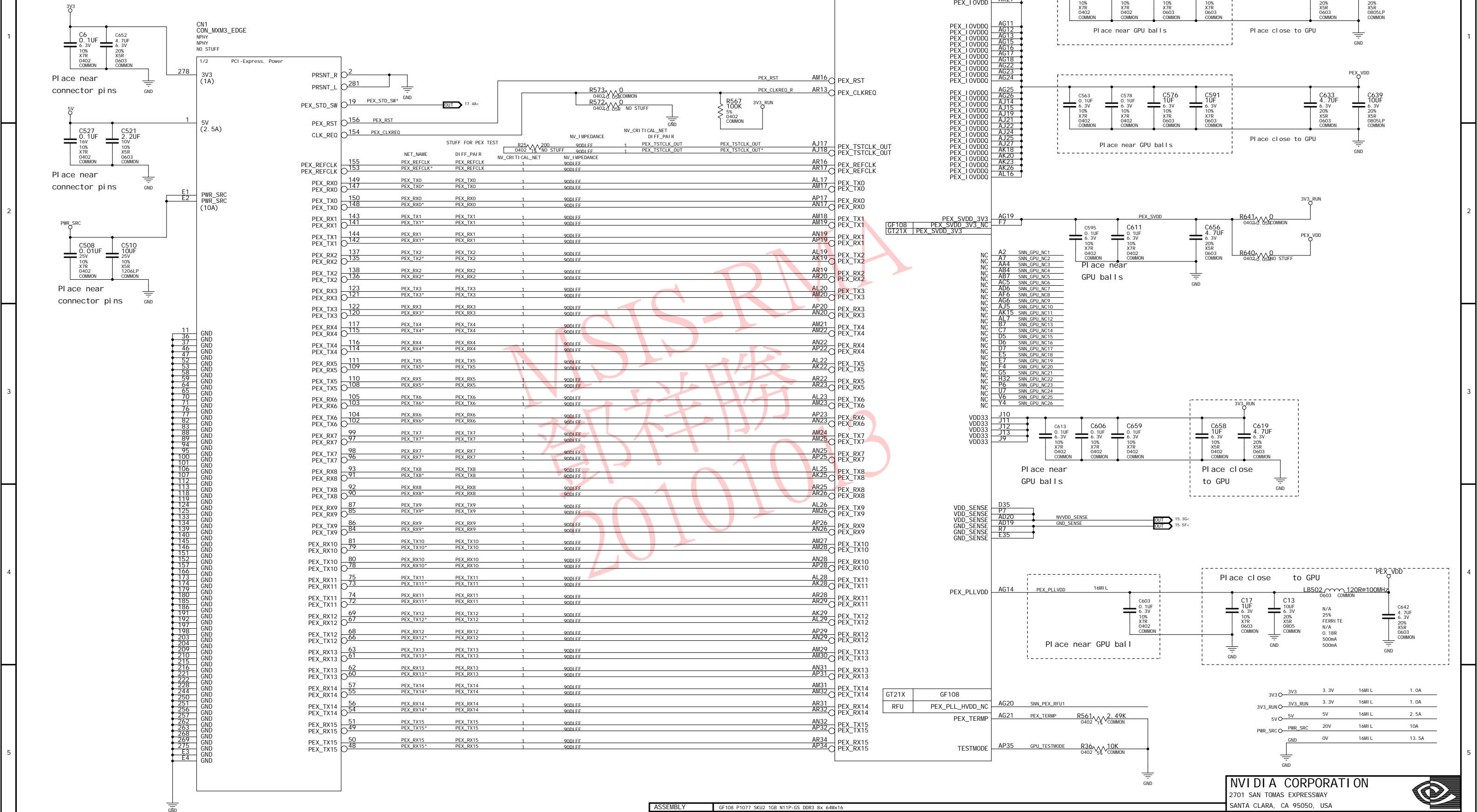
Page	Description
1	Table of Contents
2	PCI EXPRESS Interface
3	Frame Buffer GPU Interface
4	Frame Buffer Partition A Lower 32 Bits
5	Frame Buffer Partition A Upper 32 Bits
6	Frame Buffer Partition B Lower 32 Bits
7	Frame Buffer Partition B Upper 32 Bits
8	Memory Decoupling Caps
9	DAC_A, DAC_B, SPREAD, CRYSTAL
10	DP LINKS C, D, E, F
11	MXM Connector, IO-Section
12	GPIOs, JTAG, Thermal Sensor, Info ROM
13	LVDS, VBIOS
14	MIOA, MIOB, GPU VDD\DCPLNG\GND
15	NVDD Power Supply and 3V3_RUN
16	FBVDDQ, PEXVDD, and VDD_IO_PLL Power Supplies
17	STRAPS and MOUNTING HOLES
18-20	<edit here to insert page detail>

SKU	VARI ANT	NVPN	ASSEMBLY
B	BASE	602-11077-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
1	SKU0001	602-11077-0001-100	GF108 P1077 SKU1 2GB N11P-GS DDR3 8x 128Mx16
2	SKU0002	602-11077-0002-100	GF108 P1077 SKU2 1GB N11P-GS DDR3 8x 64Mx16
3	SKU0004	602-11077-0004-100	GF108 P1077 SKU4 1GB N11P-GE DDR3 8X 64MX16
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA		
NV_PN	602-11077-0002-100	
PCB REV	P1077-A01	PAGE 1 OF 20
BOM REV	A	DATE 24-MAY-2010

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

2. MXM 3.0 CONNECTOR, PCI EXPRESS INTERFACE



ASSEMBLY	GF108 P1077 SKU2 1GB N11P-GS DDR3 8x 64Mx16
PAGE DETAIL	PCI EXPRESS Interface

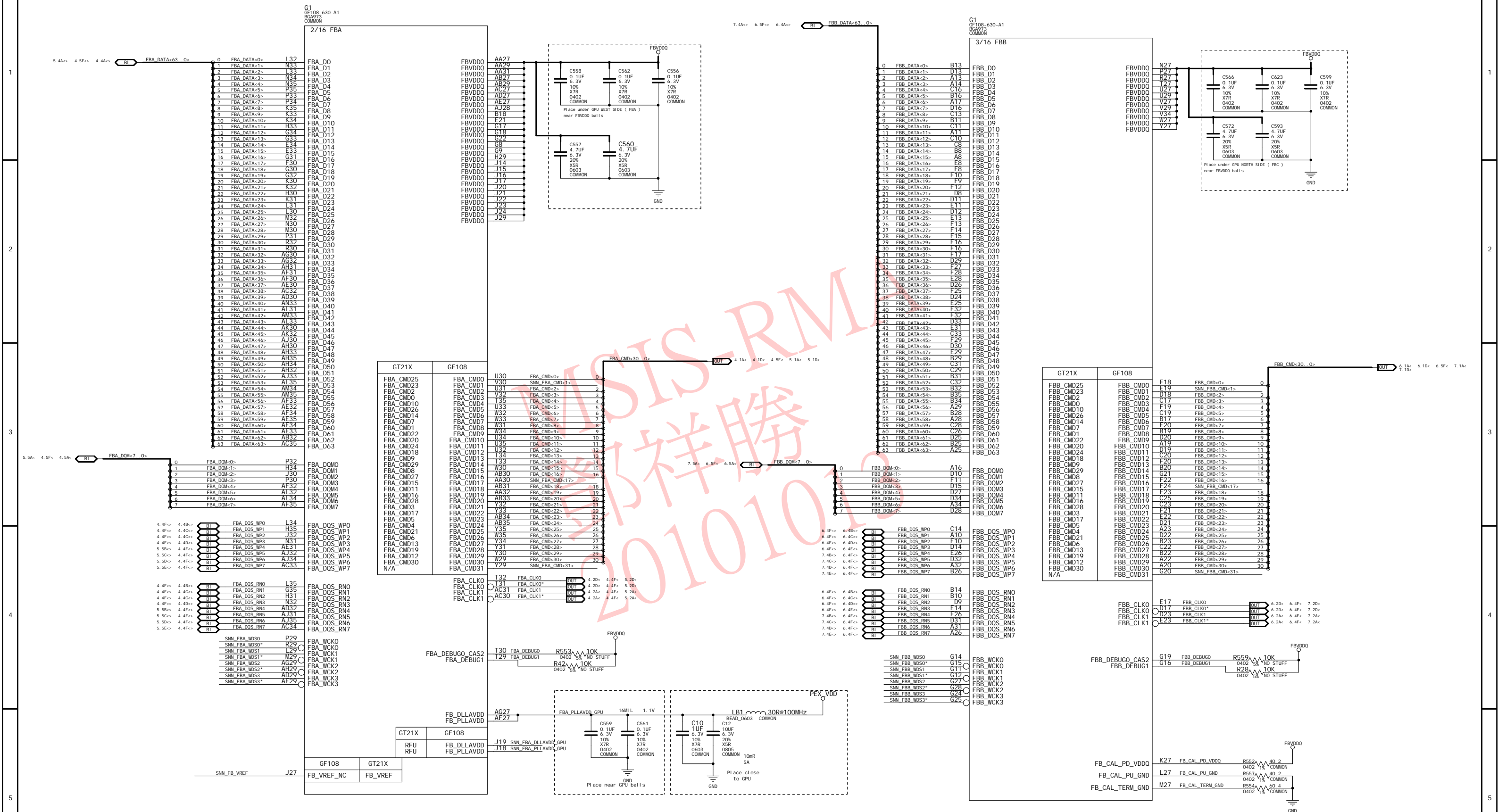
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

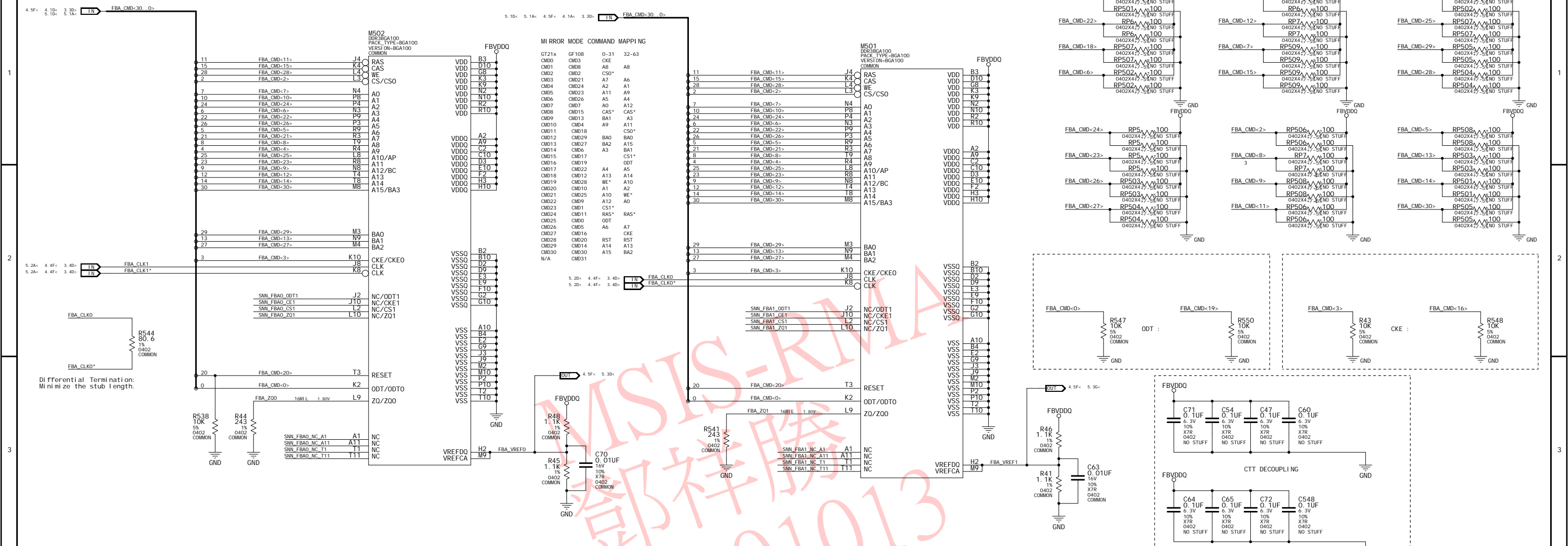
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-11077-0002-100		
PCB REV	P1077-A01	PAGE	2 OF 20
BOM REV	A	DATE	24-MAY-2010

3. GPU MEMORY INTERFACE



4. MEMORY PARTITION A LOWER 32 BITS



MEMORY PARTITION AND SIGNAL CONSTRAINTS

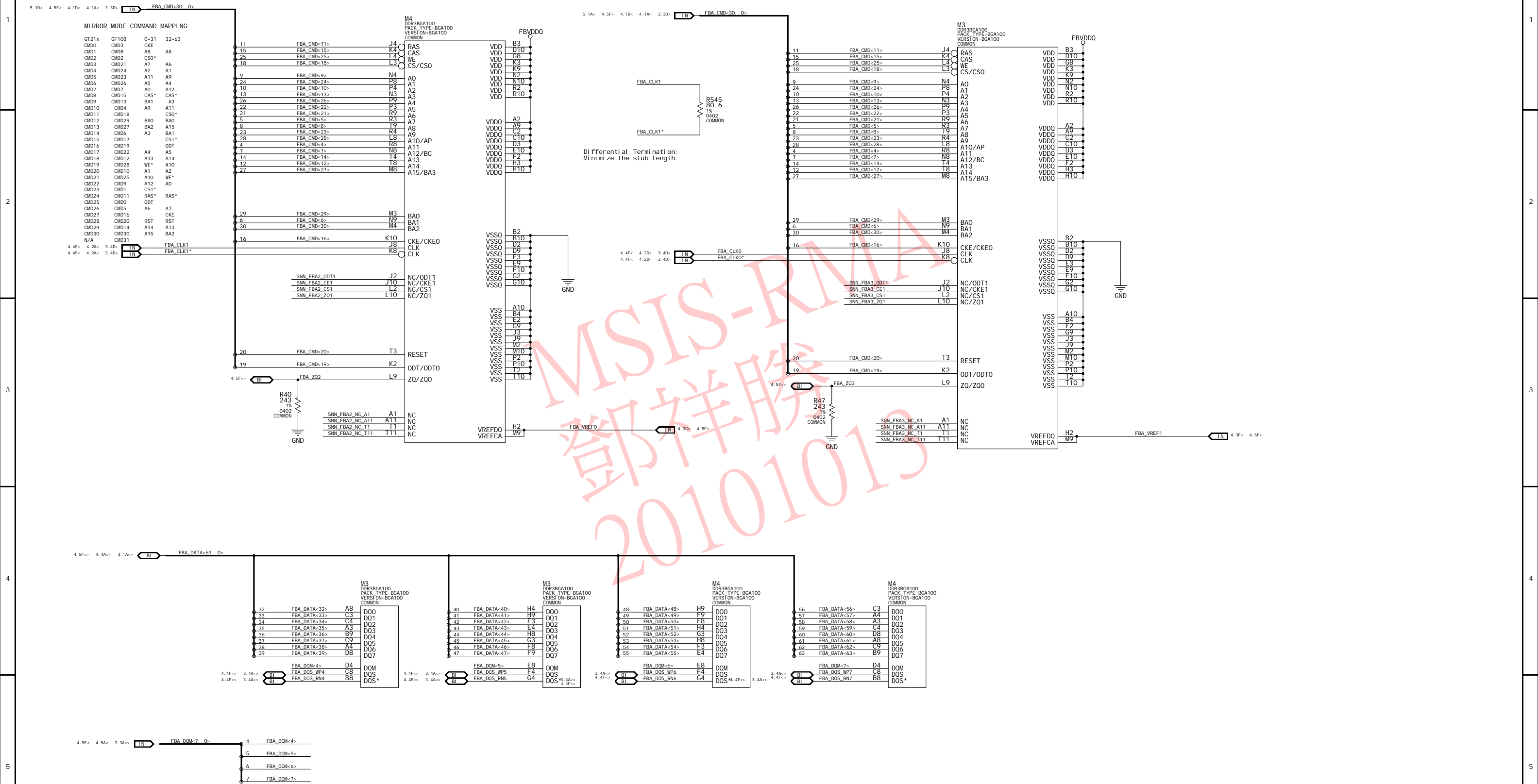
			NET	DI FPAI R	CRI TI CAL	I MPEDANCE
5. 2D<	4. 2D<	3. 4D>	1N	FBA_CLK0	FBA_CLK0	80DI FF
5. 2D>	4. 2D<	3. 4D>	1N	FBA_CLK0*	FBA_CLK0	80DI FF
5. 2A<	4. 2A<	3. 4D>	1N	FBA_CLK1	FBA_CLK1	80DI FF
5. 2A>	4. 2A<	3. 4D>	1N	FBA_CLK1*	FBA_CLK1	80DI FF
4. 4B<	3. 4A<	3. 4D>	1N	FBA_DQS_WP0	FBA_DQS0	80DI FF
4. 4B>	3. 4A<	3. 4D>	B1	FBA_DQS_RN0	FBA_DQS0	80DI FF
4. 4C<	3. 4A<	3. 4D>	B1	FBA_DQS_WP1	FBA_DQS1	80DI FF
4. 4C>	3. 4A<	3. 4D>	B1	FBA_DQS_RN1	FBA_DQS1	80DI FF
4. 4C<	3. 4A<	3. 4D>	B1	FBA_DQS_WP2	FBA_DQS2	80DI FF
4. 4C>	3. 4A<	3. 4D>	B1	FBA_DQS_RN2	FBA_DQS2	80DI FF
4. 4D<	3. 4A<	3. 4D>	B1	FBA_DQS_WP3	FBA_DQS3	80DI FF
4. 4D>	3. 4A<	3. 4D>	B1	FBA_DQS_RN3	FBA_DQS3	80DI FF
5. 5B<	3. 4A<	3. 4D>	B1	FBA_DQS_WP4	FBA_DQS4	80DI FF
5. 5B>	3. 4A<	3. 4D>	B1	FBA_DQS_RN4	FBA_DQS4	80DI FF
5. 5C<	3. 4A<	3. 4D>	B1	FBA_DQS_WP5	FBA_DQS5	80DI FF
5. 5C>	3. 4A<	3. 4D>	B1	FBA_DQS_RN5	FBA_DQS5	80DI FF
5. 5D<	3. 4A<	3. 4D>	B1	FBA_DQS_WP6	FBA_DQS6	80DI FF
5. 5D>	3. 4A<	3. 4D>	B1	FBA_DQS_RN6	FBA_DQS6	80DI FF
5. 5E<	3. 4A<	3. 4D>	B1	FBA_DQS_WP7	FBA_DQS7	80DI FF
5. 5E>	3. 4A<	3. 4D>	B1	FBA_DQS_RN7	FBA_DQS7	80DI FF

5.4A<	4.4A<	3.1A<	BI	FBA_DATA<63..0>	2	45OHM
5.5A<	4.5A<	3.3A<	IN	FBA_DATA<7..0>	2	45OHM
5.10A<	5.1A<	4.10A<	IN	FBA_CMD<30..0>	2	45OHM

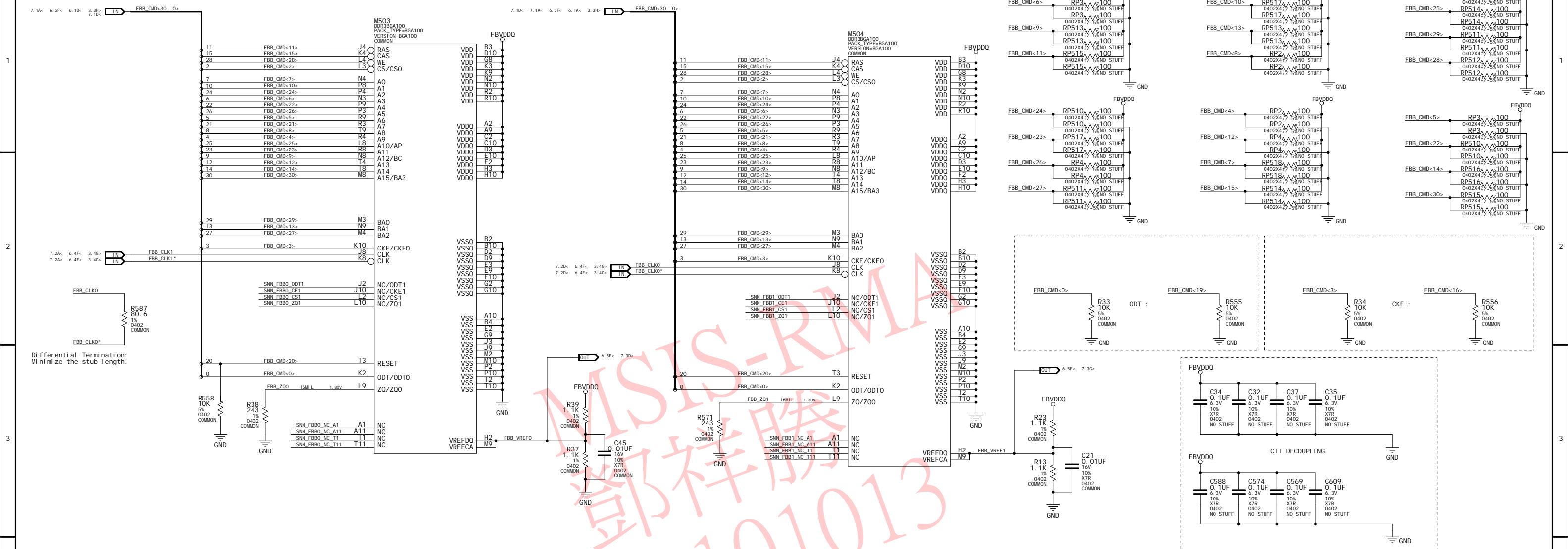
NET		MI_N_L1_NE_WI_DTH	VOLTAGE
5.3D<	4.3C<	FBA_VREF0	1.6mV
5.3G<	4.3F<	FBA_VREF1	0.9V

5. 3B<>		FBA_Z02	16MIL L	1.80V
5. 3E<>		FBA_Z03	16MIL L	1.80V

5. MEMORY PARTITION A UPPER 32 BITS



6. MEMORY PARTITION B LOWER 32 BITS



MEMORY PARTITION C SIGNAL CONSTRAINTS

NET	DIFFPAIR	CRITICAL	IMPEDANCE
FBB_CLK0	FBB_CLK0	1	80DFF
FBB_CLK1	FBB_CLK1	1	80DFF
FBB_CLK1*	FBB_CLK1	1	80DFF
FBB_DQS_WP0	FBB_DQS0	1	80DFF
FBB_DQS_WP1	FBB_DQS1	1	80DFF
FBB_DQS_WP2	FBB_DQS2	1	80DFF
FBB_DQS_WP3	FBB_DQS3	1	80DFF
FBB_DQS_WN0	FBB_DQS4	1	80DFF
FBB_DQS_WN1	FBB_DQS5	1	80DFF
FBB_DQS_WN2	FBB_DQS6	1	80DFF
FBB_DQS_WN3	FBB_DQS7	1	80DFF
FBB_DQS_WP0	FBB_DQS0	1	80DFF
FBB_DQS_WP1	FBB_DQS1	1	80DFF
FBB_DQS_WP2	FBB_DQS2	1	80DFF
FBB_DQS_WP3	FBB_DQS3	1	80DFF
FBB_DQS_WN0	FBB_DQS4	1	80DFF
FBB_DQS_WN1	FBB_DQS5	1	80DFF
FBB_DQS_WN2	FBB_DQS6	1	80DFF
FBB_DQS_WN3	FBB_DQS7	1	80DFF
FBB_DATA<63>		2	45OHM
FBB_DOM<7>		2	45OHM
FBB_CMD<30>		2	45OHM
FBB_VREF0			0.9V
FBB_VREF1			0.9V
FBB_Z02			1.80V
FBB_Z03			1.80V

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



NV_PN 602-11077-0002-100

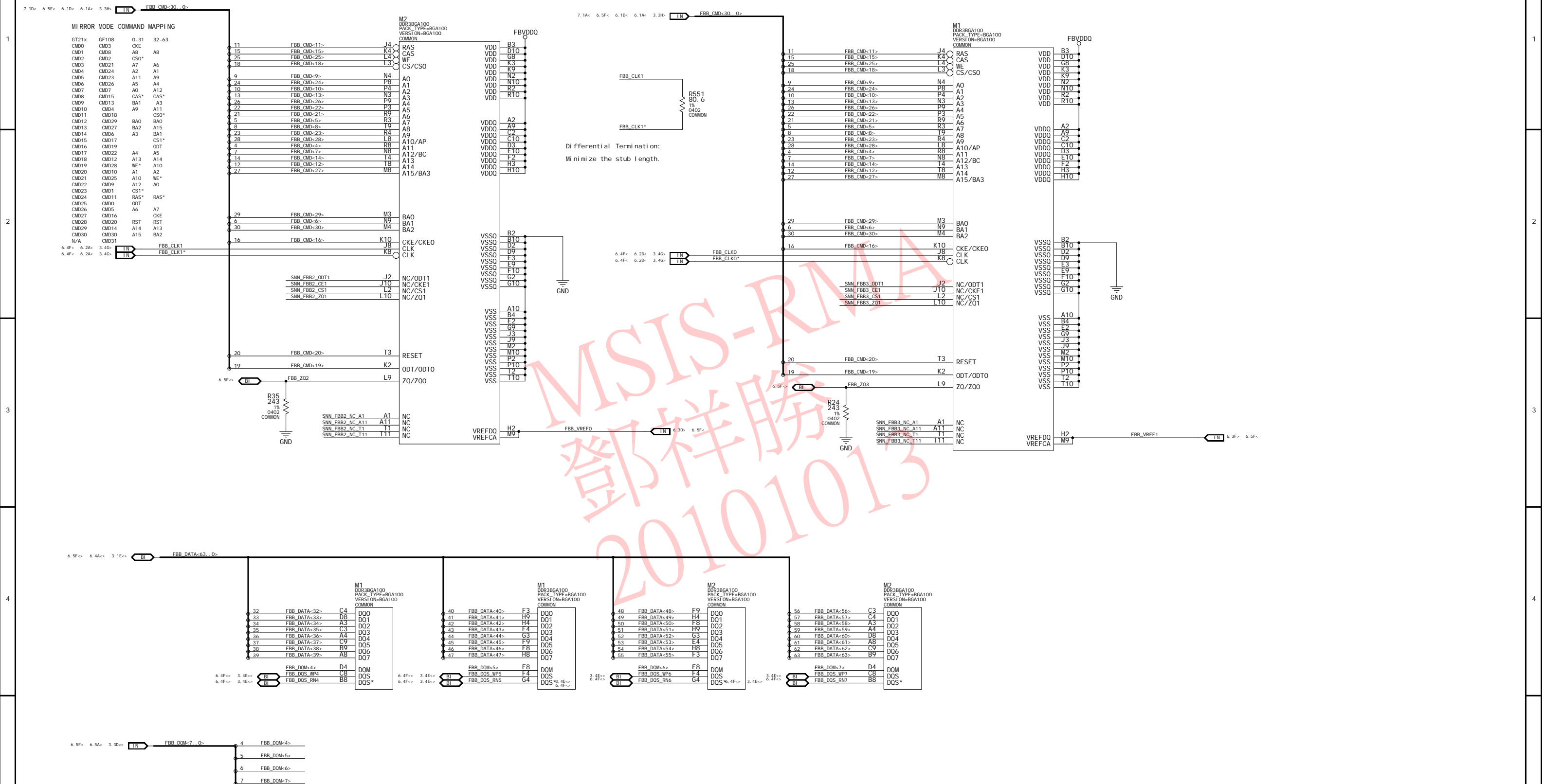
PCB REV P1077-A01
BOM REV A

PAGE 6 OF 20
DATE 24-MAY-2010

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

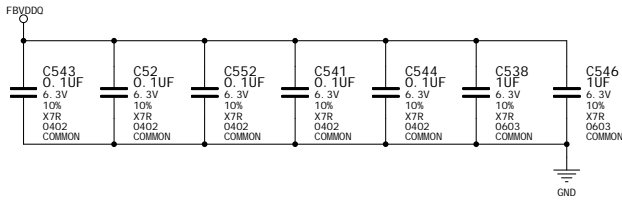
ASSEMBLY GF108 P1077 SKU2 1GB N1P-GS DDR3 8x 64Mx16
PAGE DETAIL Frame Buffer Partition B Lower 32 Bits

7. MEMORY PARTITION B UPPER 32 BITS

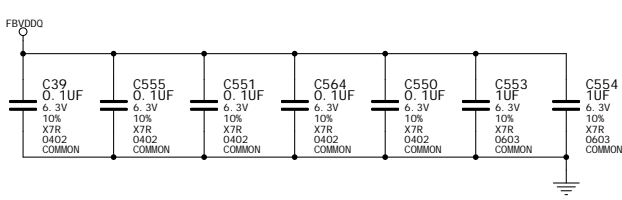


8. MEMORY DECOUPLING CAPS

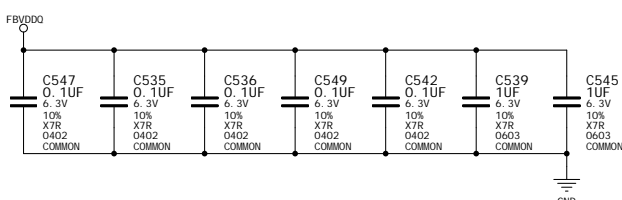
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 0-15



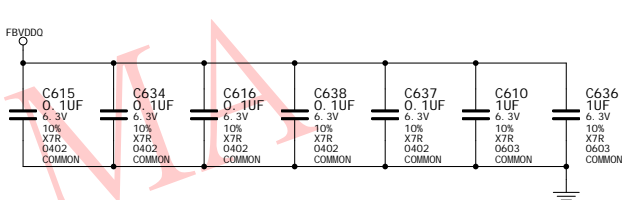
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B LOWER BITS 0-15



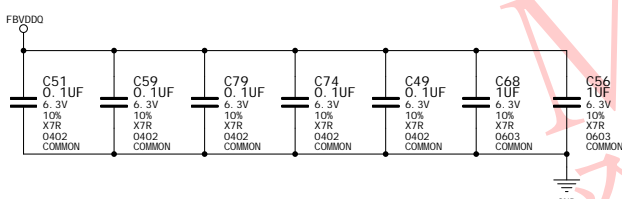
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 16-31



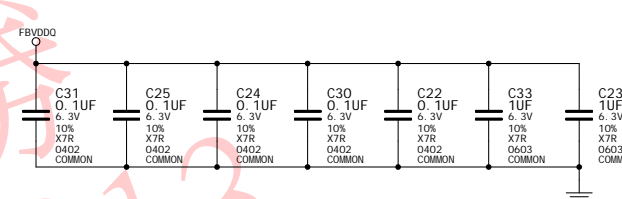
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B LOWER BITS 16-31



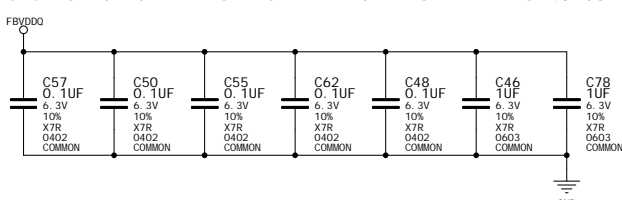
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 32-47



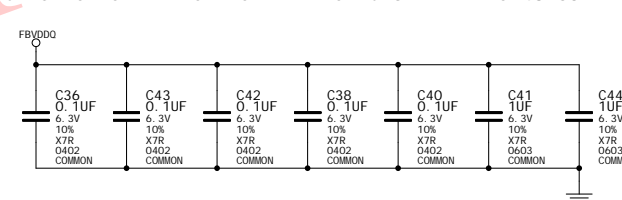
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B UPPER BITS 32-47



DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 48-63

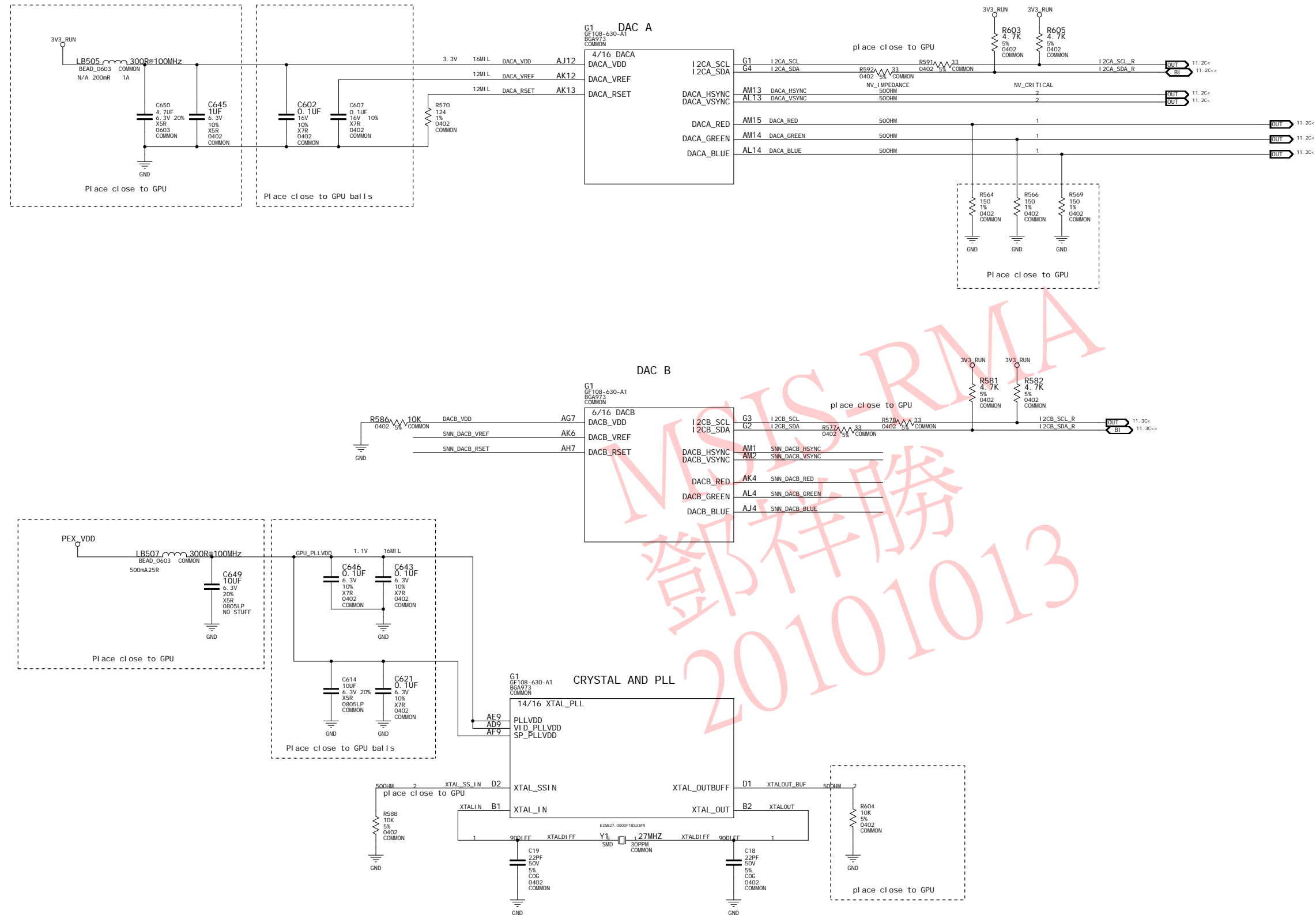


DECOUPLING CAPS FOR ONE MEMORY OF PARTION C UPPER BITS 48-63



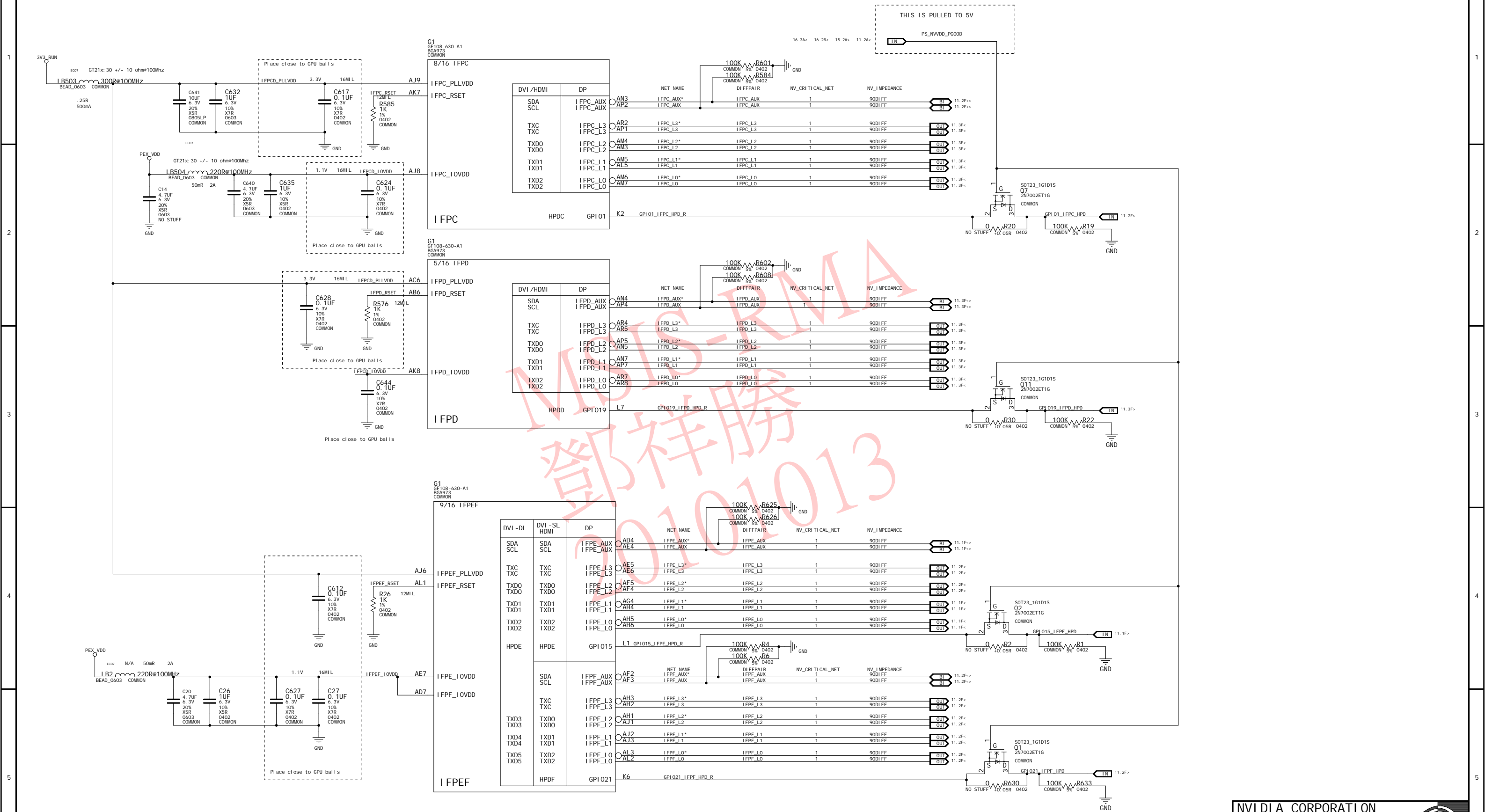
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

9. DAC_A, DAC_B, PLL, CRYSTAL




ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

10. DP LINKS CD, LINK EF



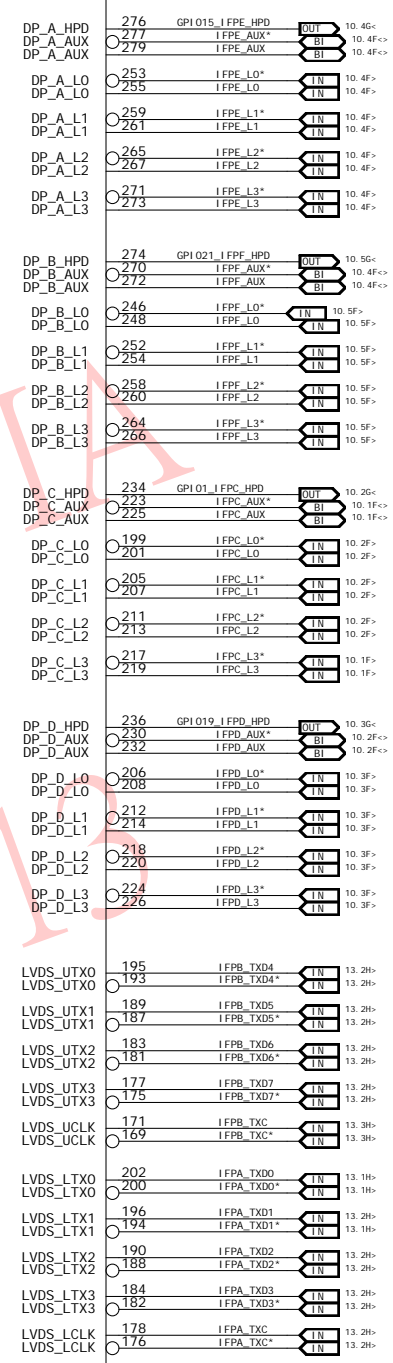
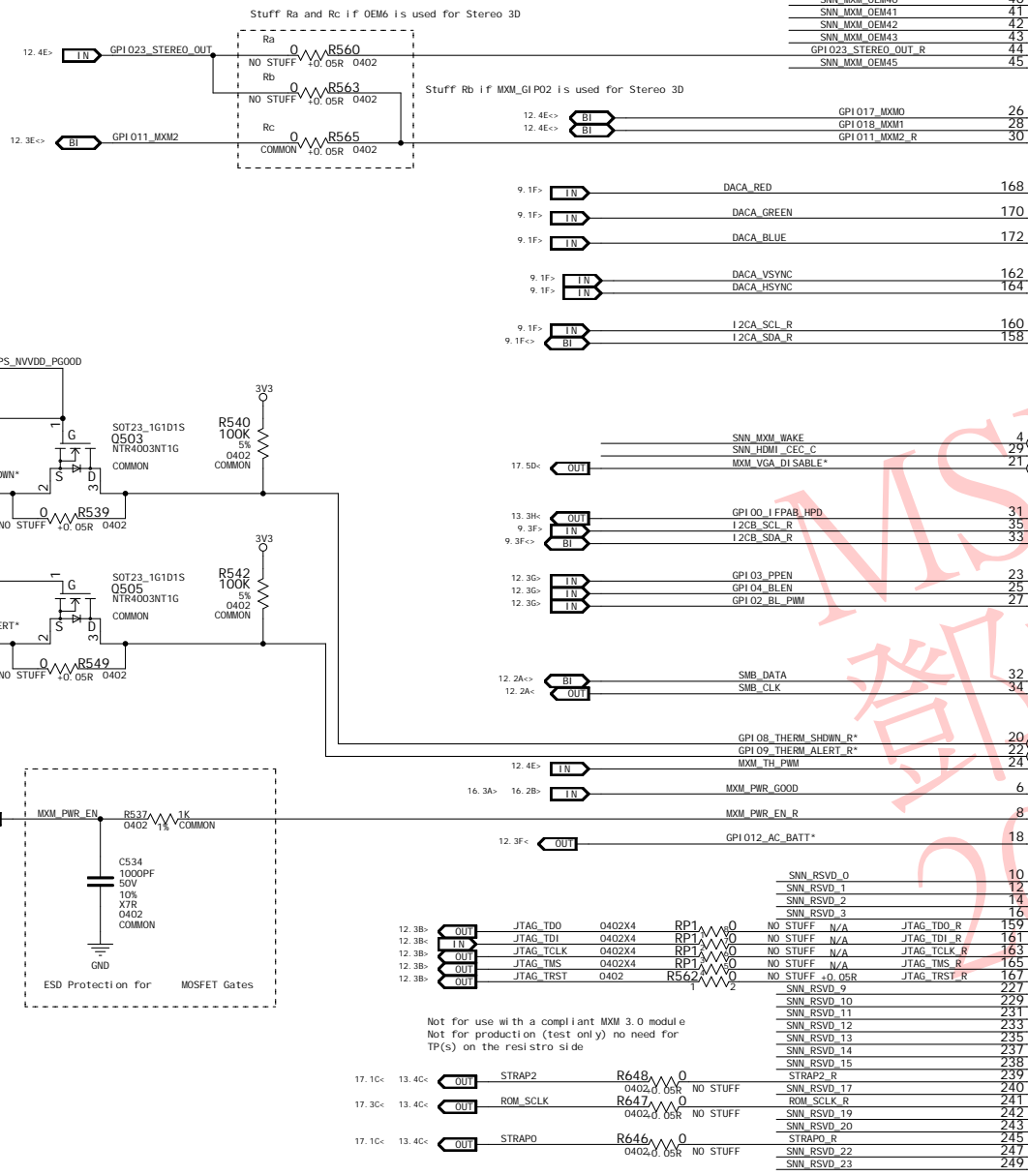
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	GF108 P1077 SKU2 1GB N11P-GS DDR3 8x 64Mx16
PAGE DETAIL	DP LINKS C, D, E, F

NVI DI A CORPORATI ON			
2701 SAN TOMAS EXPRESSWAY			
CA 95050, USA			
NV_CN	602-11077-0002-100		
PCB REV	P1077-A01	PAGE	10 OF 20
BOM REV	A	DATE	24-MAY-2010

11. MXM CONNECTOR

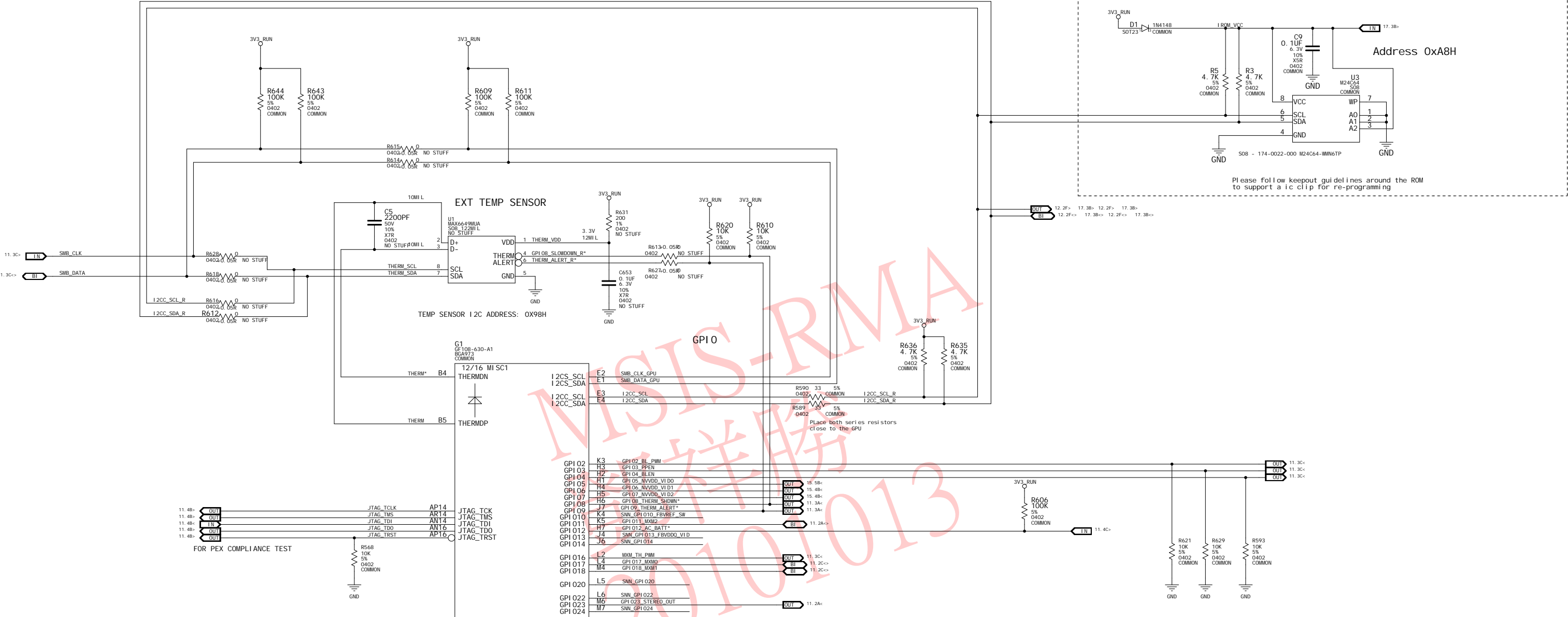
5



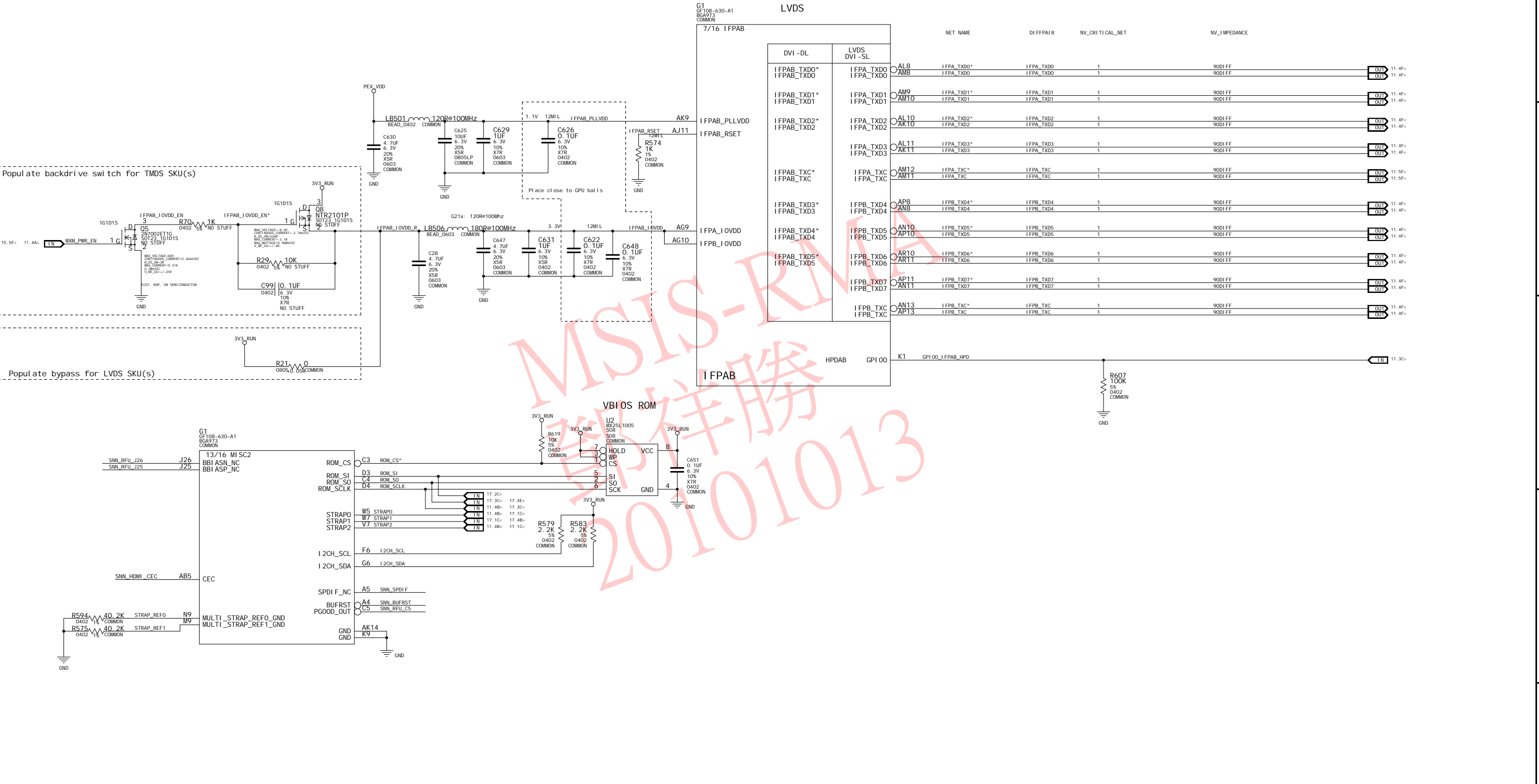
ASSEMBLY	GF108 P1077 SKU2 1GB N11P-GS DDR3 8x 64Mx16
PAGE DETAIL	MXM Connector, 10-Section

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

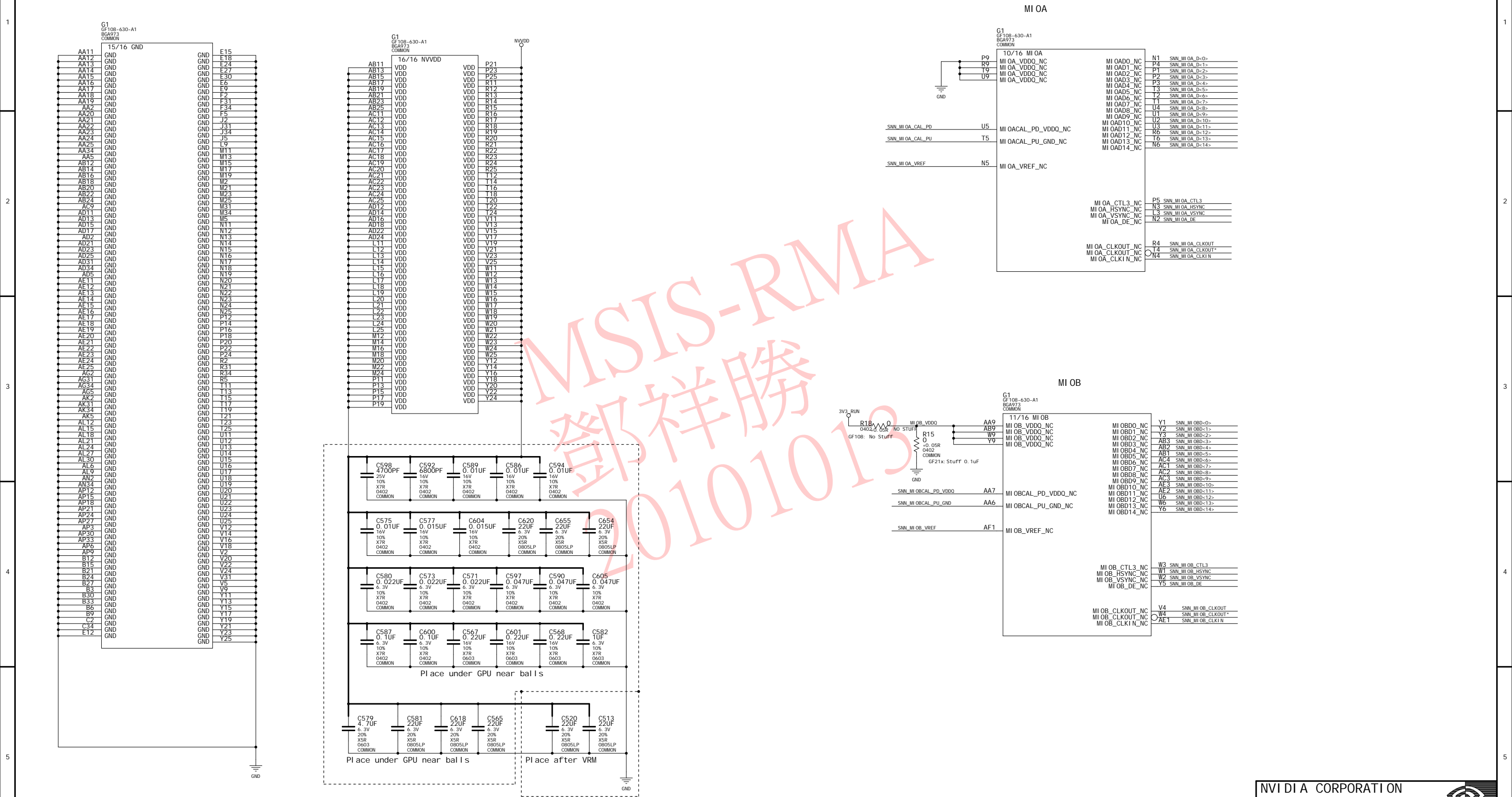
12. GPIO, JTAG, TEMP SENSOR, Info ROM



13. LVDS, VBI OS



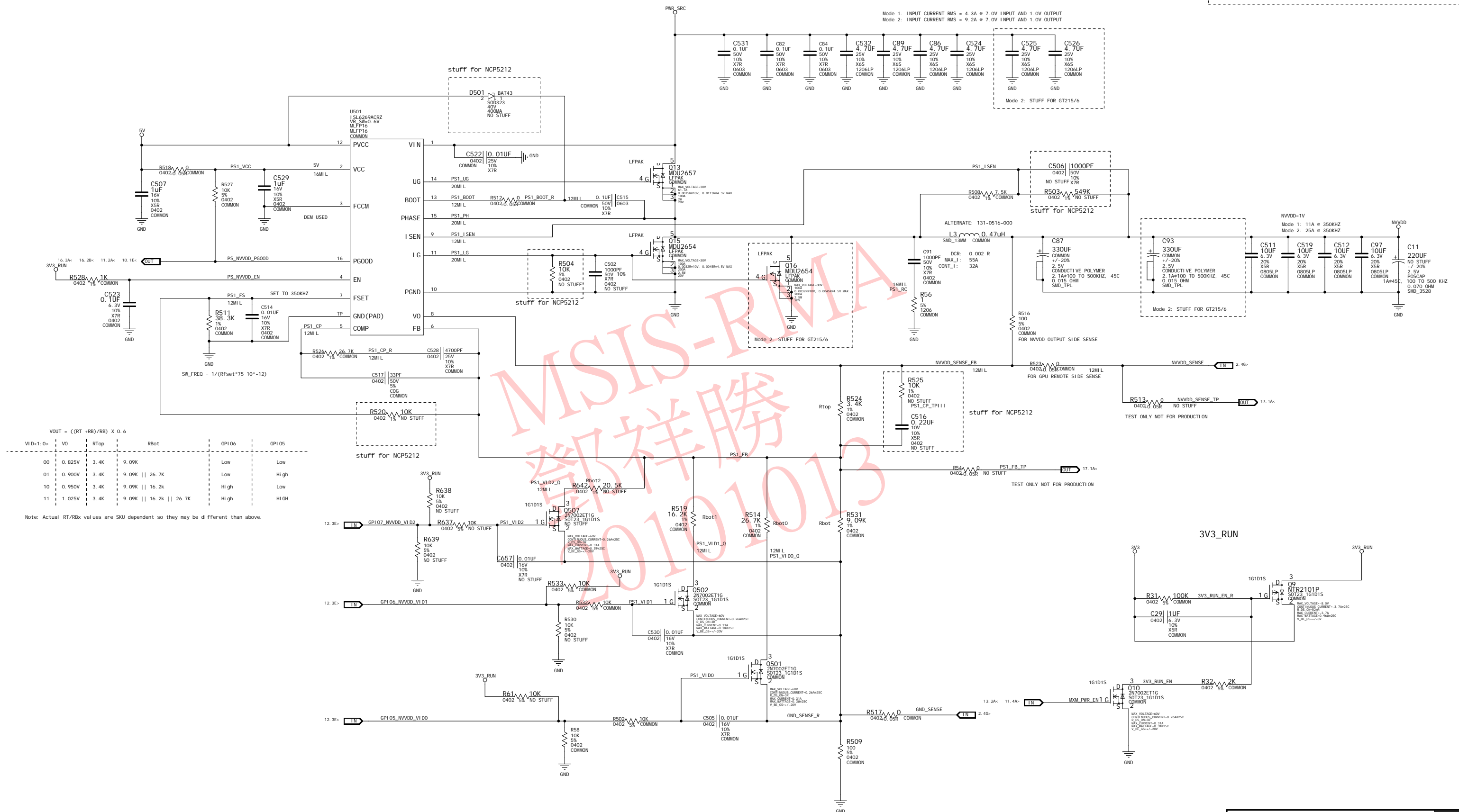
14. MI OA, MI OB, GPU VDD/DCPLNG/GND



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

15. NVVDD POWER SUPPLY AND 3V3_RUN

	NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
NVDD0	NVDD	1V	20MIL	30A



ASSEMBLY	GF108 P1077 SKU2 1GB N11P-GS DDR3 8x 64Mx16
PAGE DETAIL	NVDD Power Supply and 3V3_RUN

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

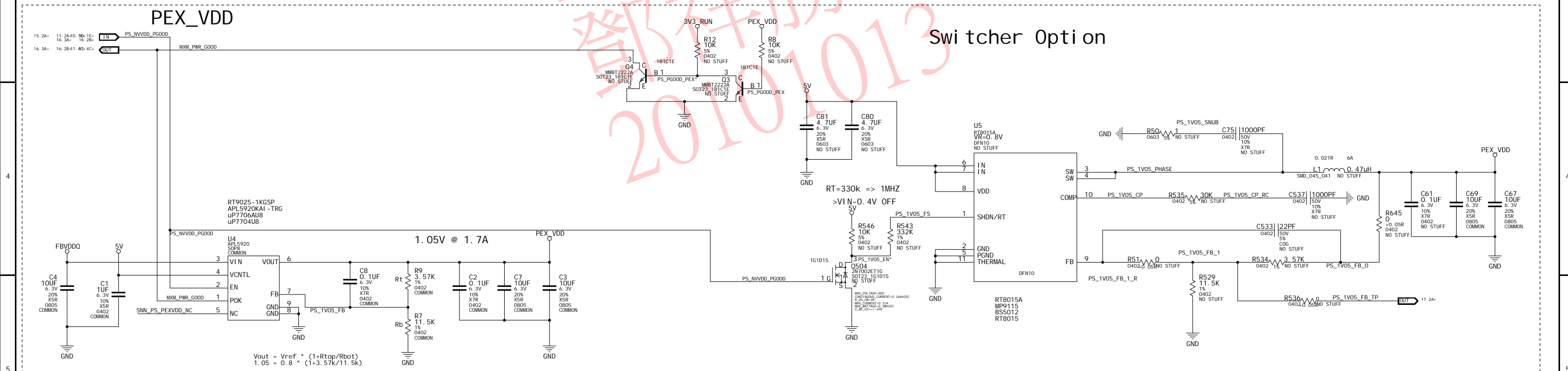
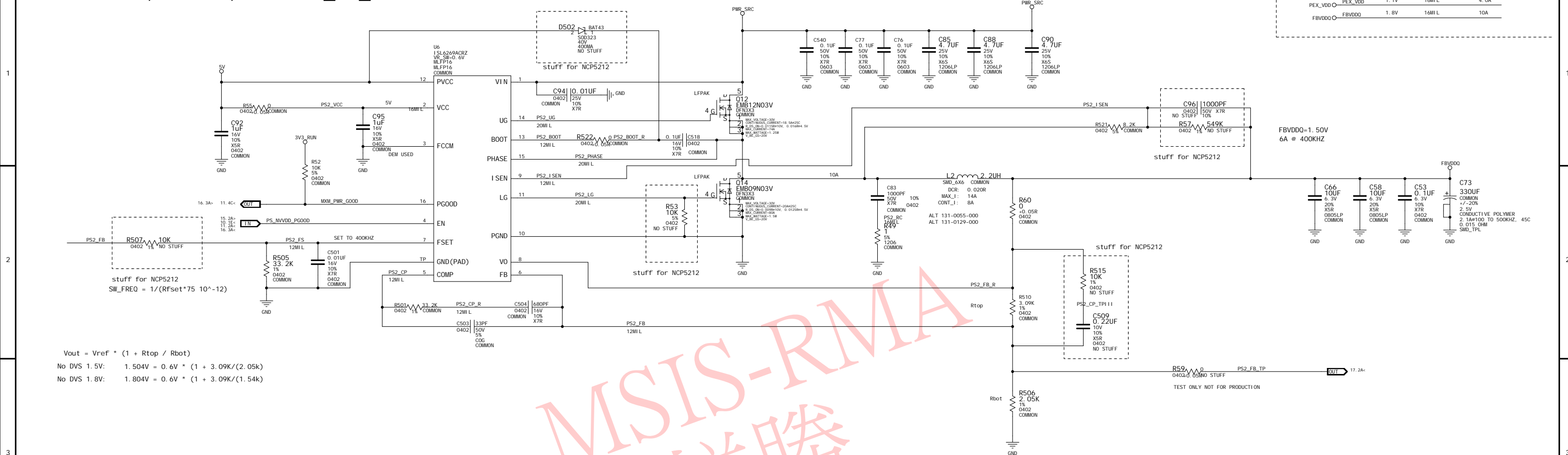
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



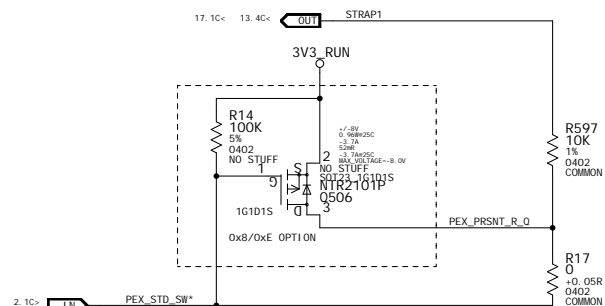
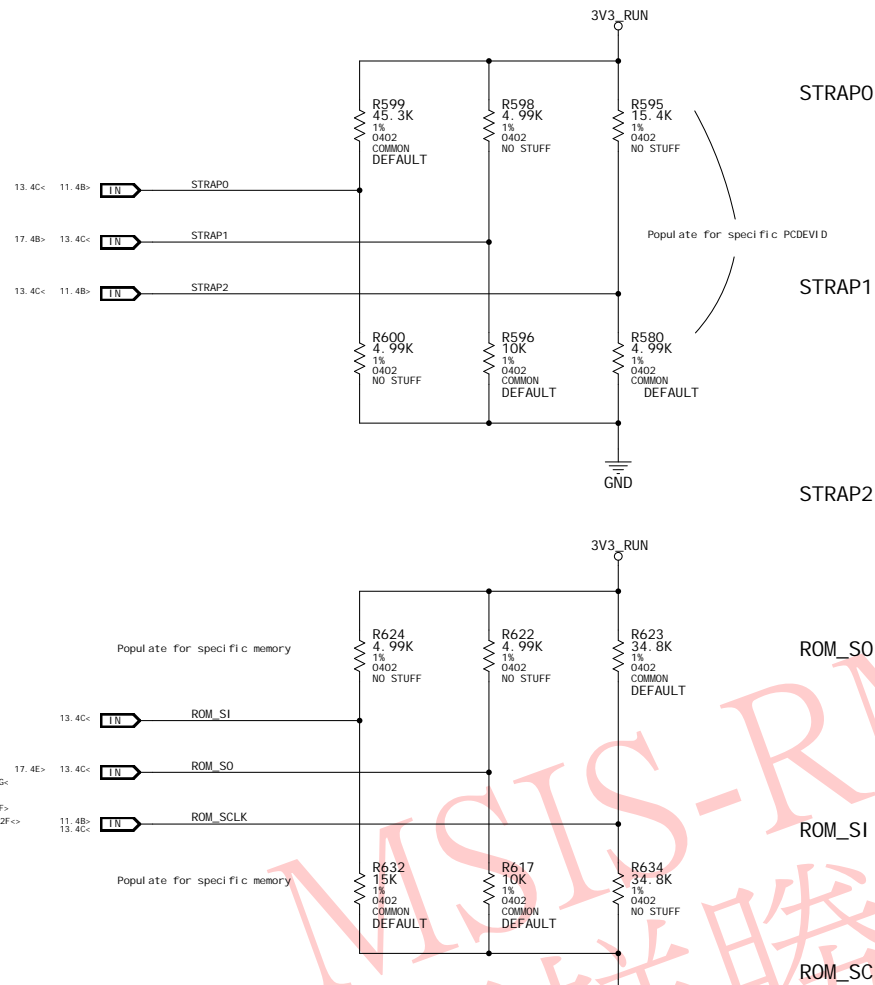
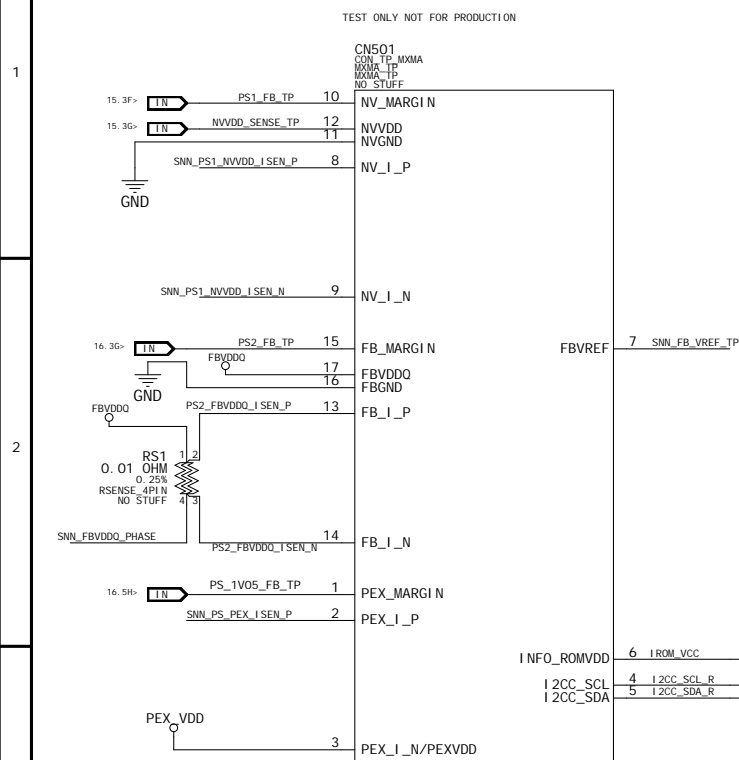
NV_PN	602-11077-0002-100
-------	--------------------

PCB REV	P1077-A01	PAGE	15 OF 20
BOM REV	A	DATE	24-MAY-2010

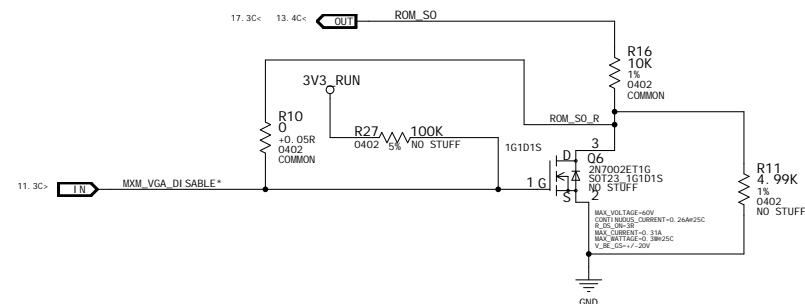
16. FBVDDQ, PEXVDD, AND VDD_IO_PLL POWER SUPPLIES



17. STRAPS, MOUNTING HOLES



PEX_PRSN_TSTDW*	R_STRAP1	3_GI0_PADCFG_LUT<3..0>
Float	10kPD	0x1 MOBILE_DEFAULT
GND	5kPD (10k 10k)	0x0 DESKTOP_DEFAULT
Float	34.8kPU	0xE MOBILE_DEFAULT
GND	5kPU (34.8k//5.9k)	0x8 DESKTOP_DEFAULT



VGA_DI SABLE#	R_ROM_S0	MODE
FLOAT	10k	0x1 VGA MODE
GND	5k (10k 10k)	0x0 3D ACCELERATOR
GND	15k (5k + 10k)	0x2 3D Device with SMB ALT ADDR

USER_BI T0	Default All SKU(s):
USER_BI T1	0xF = 45K PU
USER_BI T2	LVDS Panel EDID Mode
USER_BI T3	

```
3GI O_PADCFG_LUT_ADR0
3GI O_PADCFG_LUT_ADR1
3GI O_PADCFG_LUT_ADR2
3GI O_PADCFG_LUT_ADR3
```

Default All SKU(s):
0xF = 45K PU
LVDS Panel EDID Mode

Set at HW reset by the PEX_PADCFG Circuit

0x0:	Desktop default (normal swing)	- 5k PD
0x1:	Mobile default (low swing)	- 10k PD

PCIDeviceID	PCIDeviceID_3:0	Definitions (Note)	Actual	DEVID	set also depends on	PCIDeviceID_4
PCI_DEVICE_D_0		GT218 1000 5K PD 0100 25K PD	1000 5K PD 0100 25K PD 1100 25K PD 1100 25K PD	GT216 C1216-600 C1216-630 C1216-640 C1216-950		
PCI_DEVICE_D_1		GT218-700 GT218-730			0000 5K PD	GF108-630
PCI_DEVICE_D_2						
PCI_DEVICE_D_3						

VGA_DEVICE	0: 3D DEVICE 1: VGA DEVICE	Set at HW reset by the Device Detect Circuit
------------	-------------------------------	--

SMB_ALT_ADDR 0: Thermal Sensor ADR = 0x9E

0x1 = 10K PD

FB_0_BAR_SIZE	0: Default
---------------	------------

RAM_CFG[3:0]				Defi ni ti ons			
RAM_CFG_0	GF108 64Mx16					GT215/6	
0000	5K PD	Reserved		0001	Reserved	1001	Reserved
0001	10K PD	Reserved		0001 64Mx16 128-bl t 10K PD QI munda		1001 64Mx16 64-bl t 10K PD QI munda	
0010	15K PD	Reserved	DEFAULT	0010 64Mx16 128-bl t 15K PD QI munda		1010 64Mx16 64-bl t 15K PD QI munda	
0011	20K PD	SAMSUNG		0011 64Mx16 128-bl t 20K PD Samsung		1011 64Mx16 64-bl t 20K PD Samsung	
RAM_CFG_2	GT108 128Mx16			0100	Reserved	1100	Reserved
0100	25K PD	Reserved		0101 32Mx16 128-bl t 30K PD QI munda		1101 128Mx16 64-bl t 30K PD QI munda	
0101	30K PD	Reserved		0110 32Mx16 128-bl t 35K PD Hyni x		1110 128Mx16 64-bl t 35K PD Hyni x	
0110	35K PD	Reserved		0111 32Mx16 128-bl t 45K PD Samsung		1111 128Mx16 64-bl t 45K PD Samsung	
0111	40K PD	SAMSUNG					
				* 32Mx16 MAY BE 64Mx16 run at 1/2 density			

PEX_PLL_EN_TERM100 0: DI SABLED

SLOT_CLK_CONFIG	1: GPU and MCH COMMON REFCLK
-----------------	------------------------------

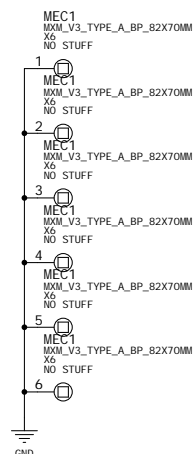
0x6 = 35K PD PCDEVI D_EXT=0

```
SUB_VENDOR          1: VBIOS ROM IS PRESENT
```

0xE = 35K PU PCDEVID_EXT=1

PCI_DEVICE_EXT	0: PCDEVICE[4] = 0 or 1 (SKU Specific)
----------------	--

	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111



A		B		C		D		E		F		G		H	
1	Title: Basenet Report Design: p1077_a01 Date: May 21 21:03:21 2010 Base nets and synonyms for p1077_a01.lib p1077_A01(ep1077_a01.lib p 1077_a01(sch_1)) Base Signal Location([Zone][dir])			FBA_DATA<14> 3.1B 4.4C FBA_DATA<15> 3.1B 4.4C FBA_DATA<16> 3.1B 4.4D FBA_DATA<17> 3.2B 4.4D FBA_DATA<18> 3.2B 4.4D FBA_DATA<19> 3.2B 4.4D FBA_DATA<20> 3.2B 4.4D FBA_DATA<21> 3.2B 4.4D FBA_DATA<22> 3.2B 4.4D FBA_DATA<23> 3.2B 4.4D FBA_DATA<24> 3.2B 4.4E FBA_DATA<25> 3.2B 4.4E FBA_DATA<26> 3.2B 4.4E FBA_DATA<27> 3.2B 4.4E FBA_DATA<28> 3.2B 4.4E FBA_DATA<29> 3.2B 4.4E FBA_DATA<30> 3.2B 4.4E FBA_DATA<31> 3.2B 4.4E FBA_DATA<32> 3.2B 5.4B FBA_DATA<33> 3.2B 5.4B FBA_DATA<34> 3.2B 5.4B FBA_DATA<35> 3.2B 5.4B FBA_DATA<36> 3.2B 5.4B FBA_DATA<37> 3.2B 5.4B FBA_DATA<38> 3.2B 5.4B FBA_DATA<39> 3.2B 5.4B FBA_DATA<40> 3.2B 5.4C FBA_DATA<41> 3.2B 5.4C FBA_DATA<42> 3.2B 5.4C FBA_DATA<43> 3.2B 5.4C FBA_DATA<44> 3.2B 5.4C FBA_DATA<45> 3.2B 5.4C FBA_DATA<46> 3.2B 5.4C FBA_DATA<47> 3.3B 5.4C FBA_DATA<48> 3.3B 5.4D FBA_DATA<49> 3.3B 5.4D FBA_DATA<50> 3.3B 5.4D FBA_DATA<51> 3.3B 5.4D FBA_DATA<52> 3.3B 5.4D FBA_DATA<53> 3.3B 5.4D FBA_DATA<54> 3.3B 5.4D FBA_DATA<55> 3.3B 5.4D FBA_DATA<56> 3.3B 5.4E FBA_DATA<57> 3.3B 5.4E FBA_DATA<58> 3.3B 5.4E FBA_DATA<59> 3.3B 5.4E FBA_DATA<60> 3.3B 5.4E FBA_DATA<61> 3.3B 5.4E FBA_DATA<62> 3.3B 5.4E FBA_DATA<63> 3.3B 5.4E FBA_DEBUG0 3.4C FBA_DEBUG1 3.4C FBA_DOM<0> 3.3B 4.4B 4.5B FBA_DOM<7..0> 3.3A<> 4.5A< 4.5F< 5.5A< FBA_DOM<1> 3.3B 4.4C 4.5B FBA_DOM<2> 3.3B 4.4D 4.5B FBA_DOM<3> 3.3B 4.4E 4.5B FBA_DOM<4> 3.3B 5.4B 5.5B FBA_DOM<5> 3.3B 5.4C 5.5B FBA_DOM<6> 3.3B 5.4D 5.5B FBA_DOM<7> 3.3B 5.4E 5.5B FBA_DOS_RN0 3.4A<> 4.4B<> 4.4F<> FBA_DOS_RN1 3.4A<> 4.4C<> 4.4F<> FBA_DOS_RN2 3.4A<> 4.4C<> 4.4F<> FBA_DOS_RN3 3.4A<> 4.4D<> 4.4F<> FBA_DOS_RN4 3.4A<> 4.4F<> 5.5B<> FBA_DOS_RN5 3.4A<> 4.4F<> 5.5C<> FBA_DOS_RN6 3.4A<> 4.4F<> 5.5D<> FBA_DOS_RN7 3.4A<> 4.4F<> 5.5E<> FBA_DOS_WP0 3.4A<> 4.4B<> 4.4F<> FBA_DOS_WP1 3.4A<> 4.4C<> 4.4F<> FBA_DOS_WP2 3.4A<> 4.4C<> 4.4F<> FBA_DOS_WP3 3.4A<> 4.4D<> 4.4F<> FBA_DOS_WP4 3.4A<> 4.4F<> 5.5B<> FBA_DOS_WP5 3.4A<> 4.4F<> 5.5C<> FBA_DOS_WP6 3.4A<> 4.4F<> 5.5D<> FBA_DOS_WP7 3.4A<> 4.4F<> 5.5E<> FBA_PL_LAVDD_GPU 3.5C FBA_VREF0 4.3C< 4.5F< 5.3D< FBA_VREF1 4.3F< 4.5F< 5.3C< FBA_ZOO 4.3B FBA_ZO1 4.3D FBA_ZO2 4.5F<> 5.3B<> FBA_ZO3 4.5F<> 5.3E<> FBB_CLK0 3.4G< 6.2A 6.2D< 6.4F< 7.2D< FBB_CLK0* 3.4G< 6.2A 6.2D< 6.4F< 7.2D< FBB_CLK1 3.4G< 6.2A< 6.4F< 7.1D 7.2A< FBB_CLK1* 3.4G< 6.2A< 6.4F< 7.1D 7.2A< FBB_CMD<0> 3.3C 6.2F 6.3B 6.3D FBB_CMD<30..0> 3.3H< 6.1A< 6.1D< 6.5F< 7.1A< 7.1D< FBB_CMD<2> 3.3C 6.1B 6.1D 6.1F FBB_CMD<3> 3.3C 6.2B 6.2D 6.2G FBB_CMD<4> 3.3C 6.1B 6.1D 6.1G FBB_CMD<5> 3.3C 6.1B 6.1D 6.1H			FBB_CMD<6> 7.1B 7.1E 3.3G 6.1B 6.1D 6.1F FBB_CMD<7> 3.3G 6.1B 6.1D 6.2G FBB_CMD<8> 3.3G 6.1B 6.1D 6.1G 7.1B 7.2E FBB_CMD<9> 3.3G 6.1F 6.2B 6.2D 7.1B 7.1E FBB_CMD<10> 3.3G 6.1B 6.1D 6.1G 7.1B 7.1E FBB_CMD<11> 3.3G 6.1B 6.1D 6.1F 7.1B 7.1E FBB_CMD<12> 3.3G 6.1G 6.2B 6.2D 7.2B 7.2E FBB_CMD<13> 3.3G 6.1G 6.2B 6.2D 7.1B 7.1E FBB_CMD<14> 3.3G 6.2B 6.2D 6.2H 7.2B 7.2E FBB_CMD<15> 3.3G 6.1B 6.1D 6.2G 7.1B 7.1E FBB_CMD<16> 3.3G 6.2H 7.2B 7.2E FBB_CMD<18> 3.3G 6.1G 7.1B 7.1E FBB_CMD<19> 3.3G 6.2F 7.3B 7.3E FBB_CMD<20> 3.3C 6.3B 6.3D 7.3B 7.3E FBB_CMD<21> 3.3G 6.1B 6.1D 6.1H 7.1B 7.1E FBB_CMD<22> 3.3G 6.1B 6.1D 6.1H 7.1B 7.1E FBB_CMD<23> 3.3G 6.1B 6.1F 6.2D 7.2B 7.2E FBB_CMD<24> 3.4G 6.1B 6.1D 6.1F 7.1B 7.1E FBB_CMD<25> 3.4G 6.1B 6.1H 6.2D 7.1B 7.1E FBB_CMD<26> 3.4G 6.1B 6.1D 6.2F 7.1B 7.1E FBB_CMD<27> 3.4G 6.2B 6.2D 6.2F 7.2B 7.2E FBB_CMD<28> 3.4G 6.1B 6.1D 6.1H 7.2B 7.2E FBB_CMD<29> 3.4G 6.1H 6.2B 6.2D 7.2B 7.2E FBB_CMD<30> 3.4C 6.2B 6.2D 6.2H 7.2B 7.2E FBB_DATA<0> 3.1E 6.4B FBB_DATA<63..0> 3.1E<> 6.4A<> 6.5F<> 7.4A<> FBB_DATA<1> 3.1E 6.4B FBB_DATA<2> 3.1E 6.4B FBB_DATA<3> 3.1E 6.4B FBB_DATA<4> 3.1E 6.4B FBB_DATA<5> 3.1E 6.4B FBB_DATA<6> 3.1E 6.4B FBB_DATA<7> 3.1E 6.4B FBB_DATA<8> 3.1E 6.4C FBB_DATA<9> 3.1E 6.4C FBB_DATA<10> 3.1E 6.4C FBB_DATA<11> 3.1E 6.4C FBB_DATA<12> 3.1E 6.4C FBB_DATA<13> 3.1E 6.4C FBB_DATA<14> 3.1E 6.4C FBB_DATA<15> 3.1E 6.4C FBB_DATA<16> 3.2E 6.4D FBB_DATA<17> 3.2E 6.4D FBB_DATA<18> 3.2E 6.4D FBB_DATA<19> 3.2E 6.4D FBB_DATA<20> 3.2E 6.4D FBB_DATA<21> 3.2E 6.4D FBB_DATA<22> 3.2E 6.4D FBB_DATA<23> 3.2E 6.4E FBB_DATA<24> 3.2E 6.4E FBB_DATA<25> 3.2E 6.4E FBB_DATA<26> 3.2E 6.4E FBB_DATA<27> 3.2E 6.4E FBB_DATA<28> 3.2E 6.4E FBB_DATA<29> 3.2E 6.4E FBB_DATA<30> 3.2E 6.4E FBB_DATA<31> 3.2E 6.4E FBB_DATA<32> 3.2E 7.4B FBB_DATA<33> 3.2E 7.4B FBB_DATA<34> 3.2E 7.4B FBB_DATA<35> 3.2E 7.4B FBB_DATA<36> 3.2E 7.4B FBB_DATA<37> 3.2E 7.4B FBB_DATA<38> 3.2E 7.4B FBB_DATA<39> 3.2E 7.4B FBB_DATA<40> 3.2E 7.4C FBB_DATA<41> 3.2E 7.4C FBB_DATA<42> 3.2E 7.4C FBB_DATA<43> 3.2E 7.4C FBB_DATA<44> 3.2E 7.4C FBB_DATA<45> 3.2E 7.4C FBB_DATA<46> 3.3E 7.4C FBB_DATA<47> 3.3E 7.4C FBB_DATA<48> 3.3E 7.4D FBB_DATA<49> 3.3E 7.4D FBB_DATA<50> 3.3E 7.4D FBB_DATA<51> 7.2B 7.2E FBB_DATA<52> 3.3E 7.4D			FBB_DATA<53> 3.3E 7.4D FBB_DATA<54> 3.3E 7.4D FBB_DATA<55> 3.3E 7.4D FBB_DATA<56> 3.3E 7.4E FBB_DATA<57> 3.3E 7.4E FBB_DATA<58> 3.3E 7.4E FBB_DATA<59> 3.3E 7.4E FBB_DATA<60> 3.3E 7.4E FBB_DATA<61> 3.3E 7.4E FBB_DATA<62> 3.3E 7.4E FBB_DATA<63> 3.3E 7.4E FBB_DEBUG0 3.4G FBB_DEBUG1 3.4G FBB_DOM<0> 3.3E 6.4B 6.5B FBB_DOM<7..0> 3.3D<> 6.5A< 6.5F< 7.5A< FBB_DOM<1> 3.3E 6.4C 6.5B FBB_DOM<2> 3.3E 6.4D 6.5B FBB_DOM<3> 3.3E 6.4E 6.5B FBB_DOM<4> 3.3E 7.4B 7.5B FBB_DOM<5> 3.3E 7.4C 7.5B FBB_DOM<6> 3.3E 7.4D 7.5B FBB_DOM<7> 3.3E 7.4E 7.5B FBB_DOS_RN0 3.4E<> 6.4B<> 6.4F<> FBB_DOS_RN1 3.4E<> 6.4C<> 6.4F<> FBB_DOS_RN2 3.4E<> 6.4D<> 6.4F<> FBB_DOS_RN3 3.4E<> 6.4E<> 6.4F<> FBB_DOS_RN4 3.4E<> 6.4F<> 7.4B<> FBB_DOS_RN5 3.4E<> 6.4F<> 7.4C<> FBB_DOS_RN6 3.4E<> 6.4F<> 7.4D<> FBB_DOS_RN7 3.4E<> 6.4F<> 7.4E<> FBB_DOS_WP0 3.4E<> 6.4B<> 6.4F<> FBB_DOS_WP1 3.4E<> 6.4C<> 6.4F<> FBB_DOS_WP2 3.4E<> 6.4D<> 6.4F<> FBB_DOS_WP3 3.4E<> 6.4E<> 6.4F<> FBB_DOS_WP4 3.4E<> 6.4F<> 7.4B<> FBB_DOS_WP5 3.4E<> 6.4F<> 7.4C<> FBB_DOS_WP6 3.4E<> 6.4F<> 7.4D<> FBB_DOS_WP7 3.4E<> 6.4F<> 7.4E<> FBB_VREF0 6.3D< 6.5F< 7.3D< FBB_VREF1 6.3F< 6.5F< 7.3G< FBB_ZOO 6.3B FBB_ZO1 6.3D FBB_ZO2 6.5F<> 7.3B<> FBB_ZO3 6.5F<> 7.3E<> FBVDDQ 16.1G FB_CAL_PD_VDDQ 3.5G FB_CAL_PU_GND 3.5G FB_CAL_TERM_GND 3.5G GND_SENSE 2.4G< 15.5F< GND_SENSE_R 15.5E GPIO0..I FPA_B_HPD 11.3C< 13.3H< GPIO1..I FPC_HPD 10.2G< 11.2F< GPIO1..I FPC_HPD_R 10.2D GPIO2..BL_PWM 11.3C< 12.3G< GPIO3..PPEN 11.3C< 12.3G< GPIO4..BLEN 11.3C< 12.3G< GPIO5..NVVDD_VI D0 12.3E< 15.5B< GPIO6..NVVDD_VI D1 12.3E< 15.4B< GPIO7..NVVDD_VI D2 12.3E< 15.4B< GPIO8..SLOWDOWN_R* 12.2C GPIO8..THERM_SHOWN* 11.3A< 12.3E< GPIO8..THERM_SHOWN.. 11.3C R* GPIO9..THERM_ALERT* 11.3A< 12.3E< GPIO9..THERM_ALERT.. 11.3C R* GPIO11..MXM2 11.2A<> 12.3E<> GPIO11..MXM2_R 11.2C GPIO12..AC_BATT* 11.4C< 12.3F< GPIO15..I FPE_HPD 10.4G< 11.1F< GPIO15..I FPE_HPD_R 10.4D GPIO17..MXM0 11.2C<> 12.4E<> GPIO18..MXM1 11.2C<> 12.4E<> GPIO19..I FPD_HPD 10.3G< 11.3F< GPIO19..I FPD_HPD_R 10.3D GPIO21..I FPF_HPD 10.5G< 11.2F< GPIO21..I FPF_HPD_R 10.5D GPIO23..STEREO_OUT 11.2A< 12.4E> GPIO23..STEREO_OUT.. 11.2C R GPU_PLLVDD 9.3B GPU_TESTMODE 2.5F I2CA_SCL 9.1D I2CA_SCL_R 9.1F< 11.2C< I2CA_SDA 9.1D I2CA_SDA_R 9.1F<> 11.2C<> I2CB_SCL 9.3D I2CB_SCL_R 9.3F< 11.3C< I2CB_SDA 9.3D I2CB_SDA_R 9.3F<> 11.3C<> I2CC_SCL 12.3D I2CC_SCL_R 12.2F< 12.2F> 17.3B> I2CC_SDA 12.3D I2CC_SDA_R 12.2F<> 12.2F<> 17.3B<> I2CH_SCL 13.4C I2CH_SDA 13.4C IFPAB_I OVDD 13.2D IFPAB_I OVDD_EN 13.2A IFPAB_I OVDD_EN* 13.2B			IFPAB_I OVDD_R 13.2C IFPAB_PLLVDD 13.2D IFPAB_RSET 13.2D IFPA_TXC 11.5F< 13.2H> IFPA_TXC* 11.5F< 13.2H> IFPA_TXD0 11.4F< 13.1H> IFPA_TXD0* 11.4F< 13.1H> IFPA_TXD1 11.4F< 13.2H> IFPA_TXD1* 11.4F< 13.1H> IFPA_TXD2 11.4F< 13.2H> IFPA_TXD2* 11.4F< 13.2H> IFPA_TXD3 11.4F< 13.2H> IFPA_TXD3* 11.4F< 13.2H> IFPB_TXC 11.4F< 13.3H> IFPB_TXC* 11.4F< 13.3H> IFPB_TXD4 11.4F< 13.2H> IFPB_TXD4* 11.4F< 13.2H> IFPB_TXD5 11.4F< 13.2H> IFPB_TXD6 11.4F< 13.2H> IFPB_TXD6* 11.4F< 13.2H> IFPB_TXD7 11.4F< 13.2H> IFPB_TXD7* 11.4F< 13.2H> IFPCD_I OVDD 10.2B 10.3B IFPCD_PLLVDD 10.1B 10.2B IFPC_AUX 10.1F<> 11.2F<> IFPC_AUX* 10.1F<> 11.2F<> IFPC_L0 10.2F< 11.3F< IFPC_L0* 10.2F< 11.3F< IFPC_L1 10.2F<		

A		B		C	D	E	F	G	H
1	SNN_FBB1_NC_A11	6. 3D	SNN_MI_OBD<2>	14. 3G					
	SNN_FBB1_NC_T1	6. 3D	SNN_MI_OBD<3>	14. 3G					
	SNN_FBB1_NC_T11	6. 3D	SNN_MI_OBD<4>	14. 3G					
	SNN_FBB1_ODT1	6. 2D	SNN_MI_OBD<5>	14. 3G					
	SNN_FBB1_Z01	6. 2D	SNN_MI_OBD<6>	14. 3G					
	SNN_FBB2_CE1	7. 2B	SNN_MI_OBD<7>	14. 3G					
	SNN_FBB2_CS1	7. 2B	SNN_MI_OBD<8>	14. 3G					
	SNN_FBB2_NC_A1	7. 3B	SNN_MI_OBD<9>	14. 3G					
	SNN_FBB2_NC_A11	7. 3B	SNN_MI_OBD<10>	14. 4G					
	SNN_FBB2_NC_T1	7. 3B	SNN_MI_OBD<11>	14. 4G					
2	SNN_FBB2_NC_T11	7. 3B	SNN_MI_OBD<12>	14. 4G					
	SNN_FBB2_ODT1	7. 2B	SNN_MI_OBD<13>	14. 4G					
	SNN_FBB2_Z01	7. 2B	SNN_MI_OBD<14>	14. 4G					
	SNN_FBB3_CE1	7. 2E	SNN_MI_OB_CLK1 N	14. 4G					
	SNN_FBB3_CS1	7. 2E	SNN_MI_OB_CLKOUT	14. 4G					
	SNN_FBB3_NC_A1	7. 3E	SNN_MI_OB_CLKOUT*	14. 4G					
	SNN_FBB3_NC_A11	7. 3E	SNN_MI_OB_CTL3	14. 4G					
	SNN_FBB3_NC_T1	7. 3E	SNN_MI_OB_DE	14. 4G					
	SNN_FBB3_NC_T11	7. 3E	SNN_MI_OB_HSYNC	14. 4G					
	SNN_FBB3_ODT1	7. 2E	SNN_MI_OB_VREF	14. 4E					
3	SNN_FBB3_Z01	7. 2E	SNN_MI_OB_VSYNC	14. 4G					
	SNN_FBB_CMD<1>	3. 3G	SNN_MXM_OEM38	11. 1C					
	SNN_FBB_CMD<17>	3. 3G	SNN_MXM_OEM39	11. 1C					
	SNN_FBB_CMD<31>	3. 4G	SNN_MXM_OEM40	11. 1C					
	SNN_FBB_WDS0	3. 4E	SNN_MXM_OEM41	11. 1C					
	SNN_FBB_WDS0*	3. 4E	SNN_MXM_OEM42	11. 1C					
	SNN_FBB_WDS1	3. 4E	SNN_MXM_OEM43	11. 2C					
	SNN_FBB_WDS1*	3. 4E	SNN_MXM_OEM45	11. 2C					
	SNN_FBB_WDS2	3. 4E	SNN_MXM_WAKE	11. 3C					
	SNN_FBB_WDS2*	3. 4E	SNN_PEX_RFU1	2. 5F					
4	SNN_FBB_WDS3	3. 4E	SNN_PST1_NVVDD_I SEN	17. 2A					
	SNN_FBB_WDS3*	3. 4E	_N						
	SNN_FBVDDQ_PHASE	17. 2A	SNN_PST1_NVVDD_I SEN	17. 1A					
	SNN_FB_VREF	3. 5B	_P						
	SNN_FB_VREF_TP	17. 2B	SNN_PS_PEXVDD_NC	16. 5A					
	SNN_GPI 010_FBVREF_	12. 3D	SNN_PS_PEX_I SEN_P	17. 2A					
	SW		SNN_RFU_C5	13. 4C					
	SNN_GPI 013_FBVDDQ_	12. 3D	SNN_RFU_J25	13. 3A					
	VI D		SNN_RFU_J26	13. 3A					
	SNN_GPI 014	12. 3D	SNN_RSVD_0	11. 4C					
5	SNN_GPI 020	12. 4D	SNN_RSVD_1	11. 4C					
	SNN_GPI 022	12. 4D	SNN_RSVD_2	11. 4C					
	SNN_GPI 024	12. 4D	SNN_RSVD_3	11. 4C					
	SNN_GPU_NC1	2. 2F	SNN_RSVD_9	11. 4C					
	SNN_GPU_NC2	2. 2F	SNN_RSVD_10	11. 4C					
	SNN_GPU_NC3	2. 2F	SNN_RSVD_11	11. 4C					
	SNN_GPU_NC4	2. 2F	SNN_RSVD_12	11. 4C					
	SNN_GPU_NC5	2. 2F	SNN_RSVD_13	11. 4C					
	SNN_GPU_NC6	2. 2F	SNN_RSVD_14	11. 4C					
	SNN_GPU_NC7	2. 2F	SNN_RSVD_15	11. 4C					
6	SNN_GPU_NC8	2. 2F	SNN_RSVD_17	11. 4C					
	SNN_GPU_NC9	2. 2F	SNN_RSVD_19	11. 4C					
	SNN_GPU_NC10	2. 3F	SNN_RSVD_20	11. 4C					
	SNN_GPU_NC11	2. 3F	SNN_RSVD_22	11. 4C					
	SNN_GPU_NC12	2. 3F	SNN_RSVD_23	11. 5C					
	SNN_GPU_NC13	2. 3F	SNN_SPDI F	13. 4C					
	SNN_GPU_NC14	2. 3F	STRAPO	11. 4B> 13. 4C< 17. 1C<					
	SNN_GPU_NC15	2. 3F	STRAPO_R	11. 4C					
	SNN_GPU_NC16	2. 3F	STRAP1	13. 4C< 17. 1C< 17. 4B>					
	SNN_GPU_NC17	2. 3F	STRAP2	11. 4B> 13. 4C< 17. 1C<					
7	SNN_GPU_NC18	2. 3F	STRAP2_R	11. 4C					
	SNN_GPU_NC19	2. 3F	STRAP_REF0	13. 4A					
	SNN_GPU_NC20	2. 3F	STRAP_REF1	13. 4A					
	SNN_GPU_NC21	2. 3F	THERM	12. 3C					
	SNN_GPU_NC22	2. 3F	THERM*	12. 3C					
	SNN_GPU_NC23	2. 3F	THERM_ALERT_R*	12. 2C					
	SNN_GPU_NC24	2. 3F	THERM_SCL	12. 2B					
	SNN_GPU_NC25	2. 3F	THERM_SDA	12. 2B					
	SNN_GPU_NC26	2. 3F	THERM_VDD	12. 2C					
	SNN_HDMI_CEC	13. 4A	XTALI N	9. 4C					
8	SNN_HDMI_CEC_C	11. 3C	XTALOUT	9. 4D					
	SNN_MI_OA_CAL_PD	14. 2E	XTALOUT_BUF	9. 4D					
	SNN_MI_OA_CAL_PU	14. 2E	XTAL_SS_I N	9. 4B					
	SNN_MI_OA_CLK1 N	14. 2G							
	SNN_MI_OA_CLKOUT	14. 2G							
	SNN_MI_OA_CLKOUT*	14. 2G							
	SNN_MI_OA_CTL3	14. 2G							
	SNN_MI_OA_D<0>	14. 1G							
	SNN_MI_OA_D<1>	14. 1G							
	SNN_MI_OA_D<2>	14. 1G							
9	SNN_MI_OA_D<3>	14. 1G							
	SNN_MI_OA_D<4>	14. 1G							
	SNN_MI_OA_D<5>	14. 1G							
	SNN_MI_OA_D<6>	14. 1G							
	SNN_MI_OA_D<7>	14. 1G							
	SNN_MI_OA_D<8>	14. 1G							
	SNN_MI_OA_D<9>	14. 2G							
	SNN_MI_OA_D<10>	14. 2G							
	SNN_MI_OA_D<11>	14. 2G							
	SNN_MI_OA_D<12>	14. 2G							
10	SNN_MI_OA_D<13>	14. 2G							
	SNN_MI_OA_D<14>	14. 2G							
	SNN_MI_OA_DE	14. 2G							
	SNN_MI_OA_HSYNC	14. 2G							
	SNN_MI_OA_VREF	14. 2E							
	SNN_MI_OA_VSYNC	14. 2G							
	SNN_MI_OBCAL_PD_VDD	14. 4E							
	Q								
	SNN_MI_OBCAL_PU_GND	14. 4E							
	SNN_MI_OBD<0>	14. 3G							
11	SNN_MI_OBD<1>	14. 3G							

A		B		C		D		E		F		G		H	
Title: Cref Part Report Design: p1077_a01 Date: May 21 21:03:21 2010		C99 [13. 2B] C501 [16. 2B] C502 [15. 2D] C503 [16. 2C] C504 [16. 2C] C505 [15. 5D] C506 [15. 2F] C507 [15. 2A] C508 [2. 2A] C509 [16. 2F] C510 [2. 2A] C511 [15. 2G] C512 [15. 2H] C513 [14. 5D] C514 [15. 2B] C515 [15. 2D] C516 [15. 3E] C517 [15. 3C] C518 [16. 1D] C519 [15. 2H] C520 [14. 5C] C521 [2. 2A] C522 [15. 2C] C523 [15. 2A] C524 [15. 1F] C525 [15. 1F] C526 [15. 1F] C527 [2. 2A] C528 [15. 3C] C529 [15. 2B] C530 [15. 4D] C531 [15. 1D] C532 [15. 1E] C533 [16. 4G] C534 [11. 4A] C535 [8. 2B] C536 [8. 2B] C537 [16. 4G] C538 [8. 1C] C539 [8. 2C] C540 [16. 1E] C541 [8. 1C] C542 [8. 2C] C543 [8. 1B] C544 [8. 1C] C545 [8. 2C] C546 [8. 1C] C547 [8. 2B] C548 [4. 3G] C549 [8. 2C] C550 [8. 1F] C551 [8. 1E] C552 [8. 1B] C553 [8. 1F] C554 [8. 1F] C555 [8. 1E] C556 [3. 1D] C557 [3. 1C] C558 [3. 1C] C559 [3. 5D] C560 [3. 1D] C561 [3. 5D] C562 [3. 1D] C563 [2. 1F] C564 [8. 1E] C565 [14. 5C] C566 [3. 1G] C567 [14. 4C] C568 [14. 4C] C569 [6. 3G] C570 [2. 1G] C571 [14. 4C] C572 [3. 1G] C573 [14. 4C] C574 [6. 3G] C575 [14. 4B] C576 [2. 1G] C577 [14. 4C] C578 [2. 1G] C579 [14. 5B] C580 [14. 4B] C581 [14. 5C] C582 [14. 4D] C583 [2. 1H] C584 [2. 1G] C585 [2. 1H] C586 [14. 3C] C587 [14. 4B] C588 [6. 3G] C589 [14. 3C] C590 [14. 4C] C591 [2. 1G] C592 [14. 3C] C593 [3. 1G] C594 [14. 3C] C595 [2. 2F] C596 [2. 1F] C597 [14. 4C] C598 [14. 3B] C599 [3. 1H] C600 [14. 4C]	C601 [14. 4C] C602 [9. 1B] C603 [2. 4G] C604 [14. 4C] C605 [14. 4D] C606 [2. 3F] C607 [9. 1B] C608 [2. 1G] C609 [6. 3G] C610 [8. 2F] C611 [2. 2G] C612 [10. 4B] C613 [2. 3F] C614 [9. 3A] C615 [8. 2E] C616 [8. 2E] C617 [10. 1B] C618 [14. 5C] C619 [2. 3G] C620 [14. 4C] C621 [9. 4B] C622 [13. 2D] C623 [3. 1G] C624 [10. 2B] C625 [13. 2C] C626 [13. 2C] C627 [10. 5B] C628 [10. 2B] C629 [13. 2C] C630 [13. 2C] C631 [13. 2C] C632 [10. 1B] C633 [2. 1H] C634 [8. 2E] C635 [10. 2B] C636 [8. 2F] C637 [8. 2F] C638 [8. 2E] C639 [2. 1H] C640 [16. 3D] C641 [10. 1A] C642 [2. 4H] C643 [9. 3B] C644 [10. 3B] C645 [9. 1A] C646 [9. 3B] C647 [13. 2C] C648 [13. 2D] C649 [9. 4B] C650 [9. 1A] C651 [13. 3D] C652 [2. 1A] C653 [12. 2D] C654 [14. 4D] C655 [14. 4C] C656 [2. 2G] C657 [15. 4C] C658 [2. 3G] C659 [2. 3G] CN1 [2. 3B] CN1 [11. 3E] CN501 [17. 2B] D1 [12. 1F] D501 [15. 1C] D502 [16. 1C] G1 [2. 3E] G1 [3. 3C 3. 3F] G1 [9. 1C 9. 3C 9. 4C] G1 [10. 4C 10. 3C 10. 2C] G1 [12. 3C] G1 [13. 4B 13. 2E] G1 [14. 4F 14. 2F 14. 3A 14. 2C] L1 [16. 4G] L2 [16. 2E] L3 [15. 2F] LB1 [3. 5E] LB2 [10. 4A] LB501 [13. 2C] LB502 [2. 4H] LB503 [10. 1A] LB504 [10. 2B] LB505 [9. 1A] LB506 [13. 2C] LB507 [9. 3A] M1 [7. 2F 7. 4B 7. 4C] M2 [7. 4D 7. 4E 7. 2C] M3 [5. 4C 5. 4B 5. 2F] M4 [5. 4E 5. 4D 5. 2C] M501 [4. 4C 4. 2E 4. 4D] M502 [4. 4B 4. 2C 4. 4E] M503 [6. 2C 6. 4B 6. 4E]	M504 [6. 2E 6. 4C 6. 4D] MEC1 [17. 4H 17. 5H 17. 4H 17. 4H] 01 [10. 5F] 02 [10. 4F] 03 [16. 4D] 04 [16. 3D] 05 [13. 2A] 06 [17. 4E] 07 [10. 2F] 08 [13. 2B] 09 [15. 4G] 010 [15. 5G] 011 [10. 3F] 012 [16. 1D] 013 [15. 2D] 014 [16. 2D] 015 [15. 2D] 016 [15. 2E] 0501 [15. 4E] 0502 [15. 4D] 0503 [11. 3A] 0504 [16. 5E] 0505 [11. 3A] 0506 [17. 4B] 0507 [15. 4D] R1 [10. 4F] R2 [10. 4F] R3 [12. 1G] R4 [10. 4E] R5 [12. 1G] R6 [10. 4E] R7 [16. 5C] R8 [16. 3D] R9 [16. 5C] R10 [17. 4E] R11 [17. 5F] R12 [16. 3D] R13 [6. 3F] R14 [17. 4B] R15 [14. 3E] R16 [17. 4E] R17 [17. 4B] R18 [14. 3E] R19 [10. 2F] R20 [10. 2F] R21 [13. 3B] R22 [10. 3F] R23 [6. 3F] R24 [7. 3E] R25 [2. 2C] R26 [10. 4B] R27 [17. 4E] R28 [3. 4G] R29 [13. 2B] R30 [10. 3F] R31 [15. 4G] R32 [15. 4G] R33 [6. 2F] R34 [6. 2G] R35 [7. 3B] R36 [2. 5G] R37 [6. 3C] R38 [6. 3B] R39 [6. 3C] R40 [5. 3B] R41 [4. 3F] R42 [3. 4D] R43 [4. 2G] R44 [4. 3B] R45 [4. 3C] R46 [4. 3F] R47 [5. 3E] R48 [4. 3C] R49 [16. 2E] R50 [16. 4F] R51 [16. 4F] R52 [16. 2B] R53 [16. 2D] R54 [15. 3F] R55 [16. 1B] R56 [15. 2F] R57 [16. 1G] R58 [15. 5D] R59 [16. 3G] R60 [16. 2F] R61 [15. 5C] R70 [13. 2B] R501 [16. 2C] R502 [15. 5D] R503 [15. 2F] R504 [15. 2D] R505 [16. 2B] R506 [16. 3F] R507 [16. 2A] R508 [15. 2F] R509 [15. 5E] R510 [16. 2F] R511 [15. 2B]	R512 [15. 2C] R513 [15. 3G] R514 [15. 4E] R515 [16. 2F] R516 [15. 2F] R517 [15. 5E] R518 [15. 2B] R519 [15. 4D] R520 [15. 3C] R521 [16. 1F] R522 [16. 1D] R523 [15. 3F] R524 [15. 3E] R525 [15. 3E] R526 [15. 3B] R527 [15. 2B] R528 [15. 2A] R529 [16. 5G] R530 [15. 4D] R531 [15. 4E] R532 [15. 4D] R533 [15. 4D] R534 [16. 4G] R535 [16. 4G] R536 [16. 5G] R537 [11. 4B] R538 [4. 3B] R539 [11. 3A] R540 [11. 3B] R541 [4. 3D] R542 [11. 3B] R543 [16. 4E] R544 [4. 2A] R545 [5. 2D] R546 [16. 4E] R547 [4. 2F] R548 [4. 2H] R549 [11. 3A] R550 [4. 2G] R551 [7. 1D] R552 [3. 5G] R553 [3. 4D] R554 [3. 5G] R555 [6. 2G] R556 [6. 2H] R557 [3. 5G] R558 [6. 3B] R559 [3. 4G] R560 [11. 2B] R561 [2. 5G] R562 [11. 4C] R563 [11. 2B] R564 [9. 2E] R565 [11. 2B] R566 [9. 2E] R567 [2. 1D] R568 [12. 4B] R569 [9. 2E] R570 [9. 1B] R571 [6. 3D] R572 [2. 1D] R573 [2. 1D] R574 [13. 2D] R575 [13. 4A] R576 [10. 2B] R577 [9. 3D] R578 [9. 3E] R579 [13. 4C] R580 [17. 1D] R581 [9. 3E] R582 [9. 3E] R583 [13. 4D] R584 [10. 1E] R585 [10. 1B] R586 [9. 3B] R587 [6. 2A] R588 [9. 4B] R589 [12. 3E] R590 [12. 3E] R591 [9. 1E] R592 [9. 1D] R593 [12. 4G] R594 [13. 4A] R595 [17. 1D] R596 [17. 1D] R597 [17. 4B] R598 [17. 1D] R599 [17. 1C] R600 [17. 1C] R601 [10. 1E] R602 [10. 2E] R603 [9. 1E] R604 [9. 4D] R605 [9. 1E] R606 [12. 3F] R607 [13. 3F] R608 [10. 2E] R609 [12. 1C] R610 [12. 2D] R611 [12. 1C] R612 [12. 2B]	R613 [12. 2D] R614 [12. 2C] R615 [12. 2C] R616 [12. 2B] R617 [17. 3D] R618 [12. 2B] R619 [13. 3C] R620 [12. 2D] R621 [12. 4F] R622 [17. 2D] R623 [17. 2D] R624 [17. 2C] R625 [10. 4E] R626 [10. 4E] R627 [12. 2D] R628 [12. 2B] R629 [12. 4G] R630 [10. 5F] R631 [12. 2D] R632 [17. 3C] R633 [10. 5F] R634 [17. 3D] R635 [12. 3E] R636 [12. 3E] R637 [15. 4C] R638 [15. 3C] R639 [15. 4C] R640 [2. 2G] R641 [2. 2G] R642 [15. 3D] R643 [12. 1B] R644 [12. 1B] R645 [16. 4H] R646 [11. 4C] R647 [11. 4C] R648 [11. 4C] RP1 [11. 4C 11. 4C 11. 4C 11. 4C] RP2 [6. 1G 6. 1G 6. 1G 6. 1G] RP3 [6. 1H 6. 1H 6. 1F 6. 1F] RP4 [6. 2F 6. 2F 6. 2G 6. 1G] RP5 [4. 1F 4. 1F 4. 2F 4. 1F] RP6 [4. 1G 4. 1G 4. 1F 4. 1F] RP7 [4. 2G 4. 1G 4. 1G 4. 1G] RP501 [4. 2H 4. 2H 4. 1F 4. 1F] RP502 [4. 1F 4. 1H 4. 1F 4. 1H] RP503 [4. 2H 4. 1H 4. 2F 4. 2F] RP504 [4. 1H 4. 2F 4. 1H 4. 2F] RP505 [4. 2H 4. 1H 4. 2H 4. 1H] RP506 [4. 2G 4. 2G 4. 1G 4. 1G] RP507 [4. 1F 4. 1H 4. 1F 4. 1H] RP508 [4. 2G 4. 2G 4. 1H 4. 1H] RP509 [4. 1G 4. 1G 4. 1G 4. 1G] RP510 [6. 1F 6. 2H 6. 1F 6. 1H] RP511 [6. 2F 6. 2F 6. 1H 6. 1H] RP512 [6. 1G 6. 1G 6. 1H 6. 1H] RP513 [6. 1G 6. 1G 6. 1F 6. 1F] RP514 [6. 1H 6. 2G 6. 2G 6. 1H] RP515 [6. 1F 6. 1F 6. 2H 6. 2H] RP516 [6. 2H 6. 2H 6. 1H 6. 1H] RP517 [6. 1G 6. 1G 6. 2F 6. 1F] RP518 [6. 1F 6. 2G 6. 2G 6. 1F] RS1 [17. 2A] U1 [12. 2C] U2 [13. 3D] U3 [12. 1G] U4 [16. 5B] U5 [16. 4F] U6 [16. 2C] U501 [15. 2C] Y1 [9. 5C]									
1		2		3		4		5							
ASSEMBLY		GF108 P1077 SKU2 1GB N11P-GS DDR3 8x 64Mx16													
PAGE DETAIL		<edit here to insert page detail>													
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.															
A		B		C		D		E		F		G		H	
NV_PN		602-11077-0002-100													
PCB REV		P1077-A01													
BOM REV		A													
		PAGE 20 OF 20													
		DATE 24-MAY-2010													