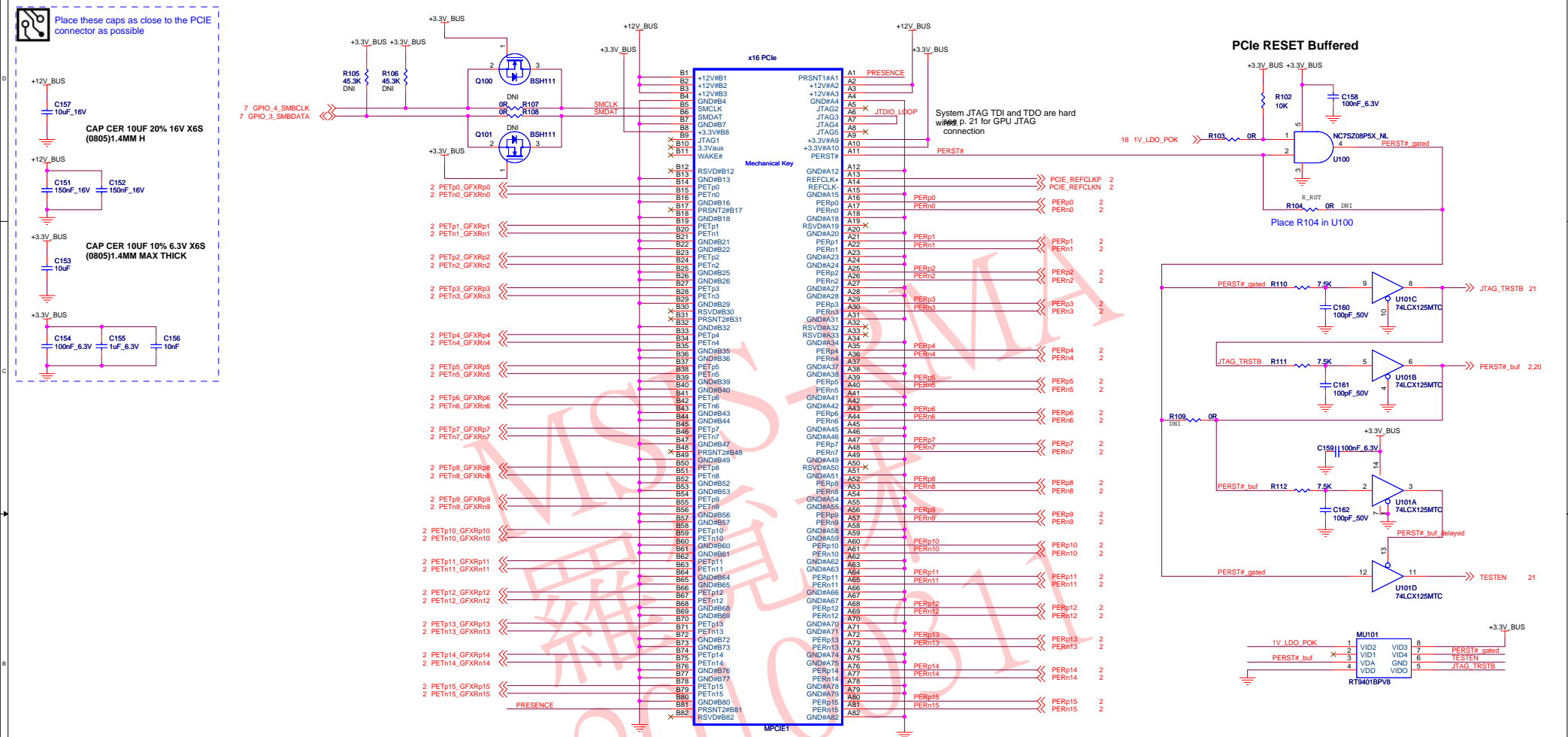




## PCI-EXPRESS EDGE CONNECTOR




SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

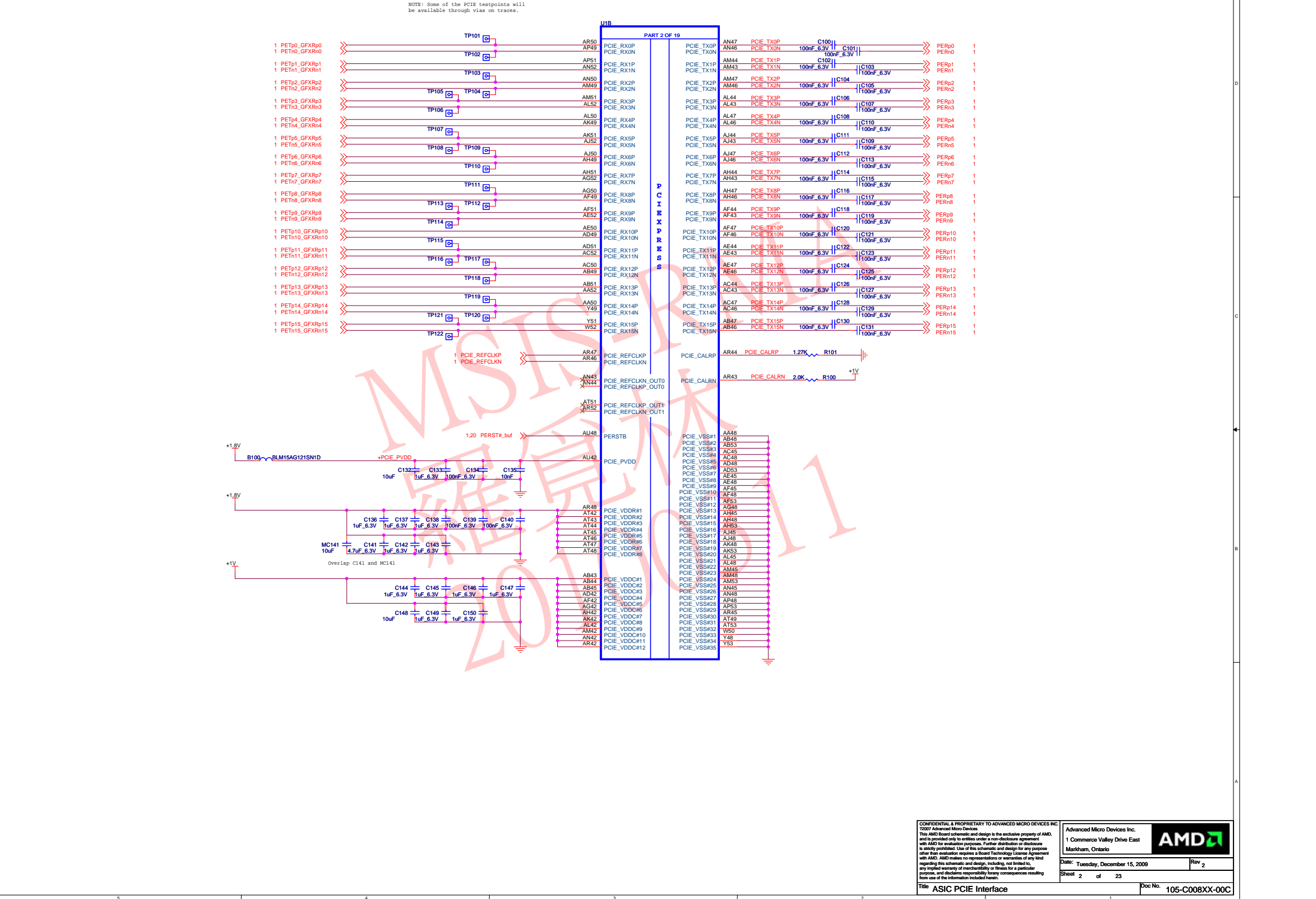
**CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.**  
**72007 Advanced Micro Devices**

This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

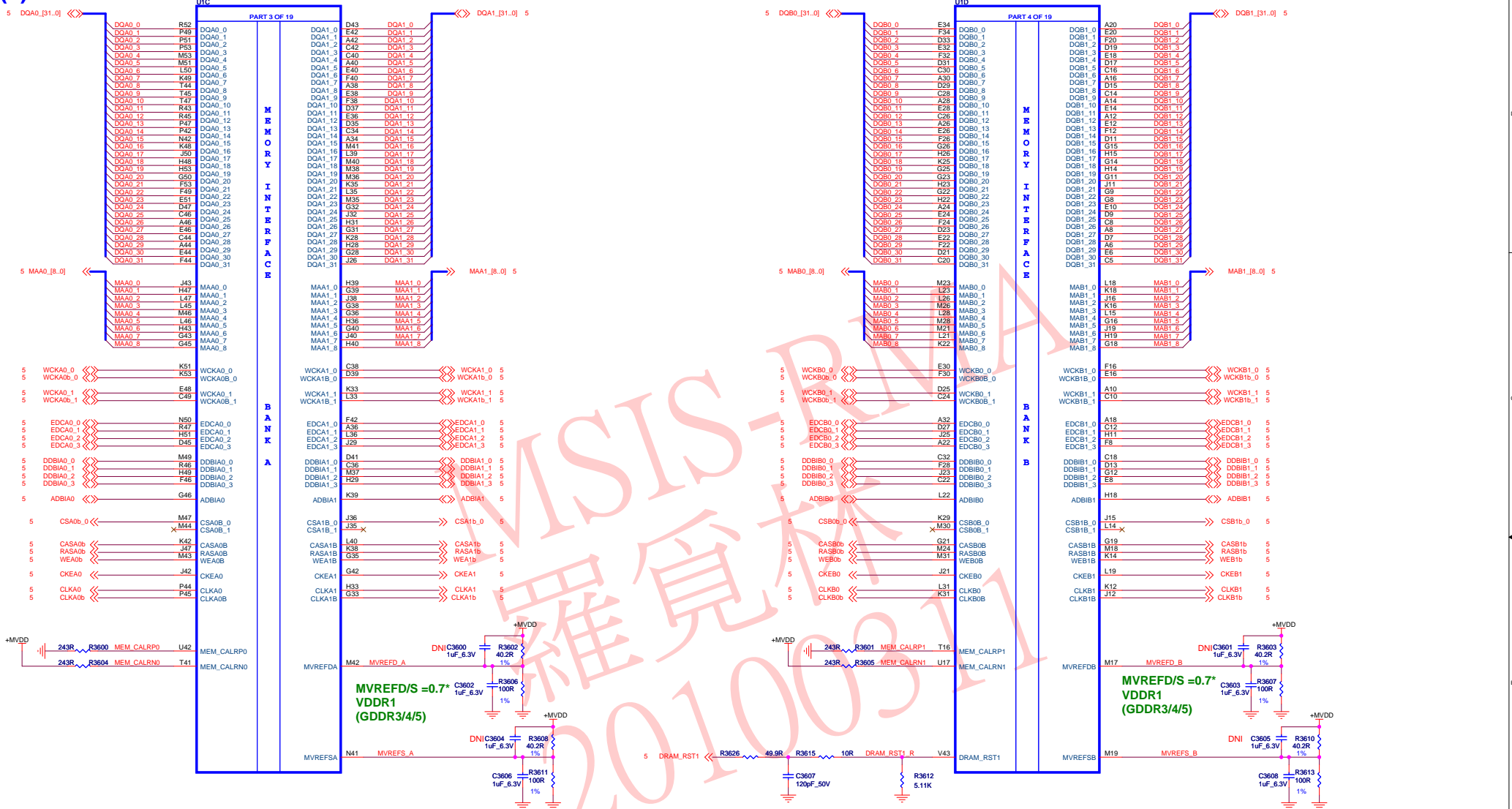
**Title: PCIE EDGE CONNECTOR**

<p>Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario</p>			
<p>Date: Tuesday, December 15, 2009</p>		<p>Rev 2</p>	
<p>Sheet 1 of 23</p>		<p>Doc No. 105-000018-000</p>	

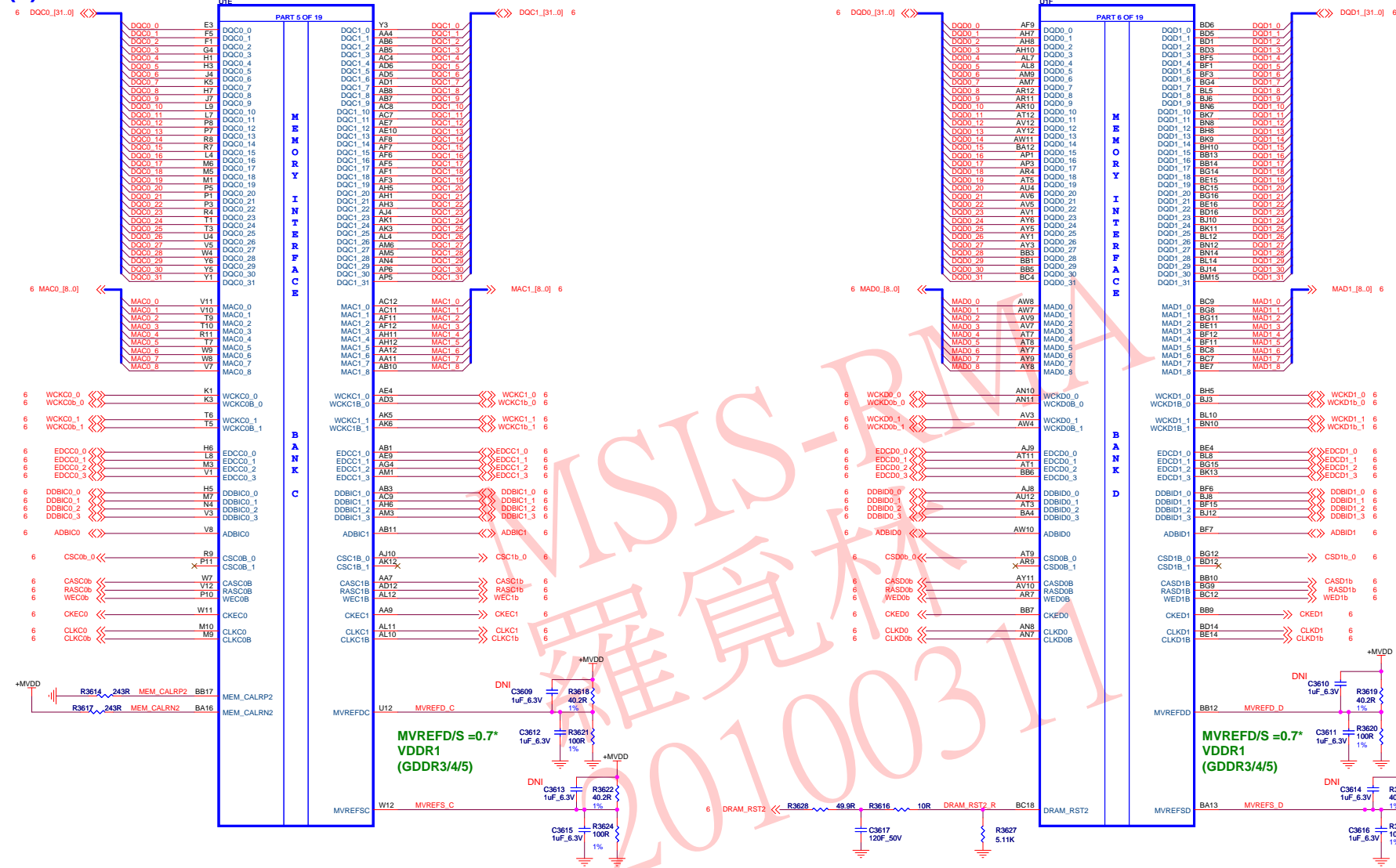
(2) CYPRESS PCIE Interface



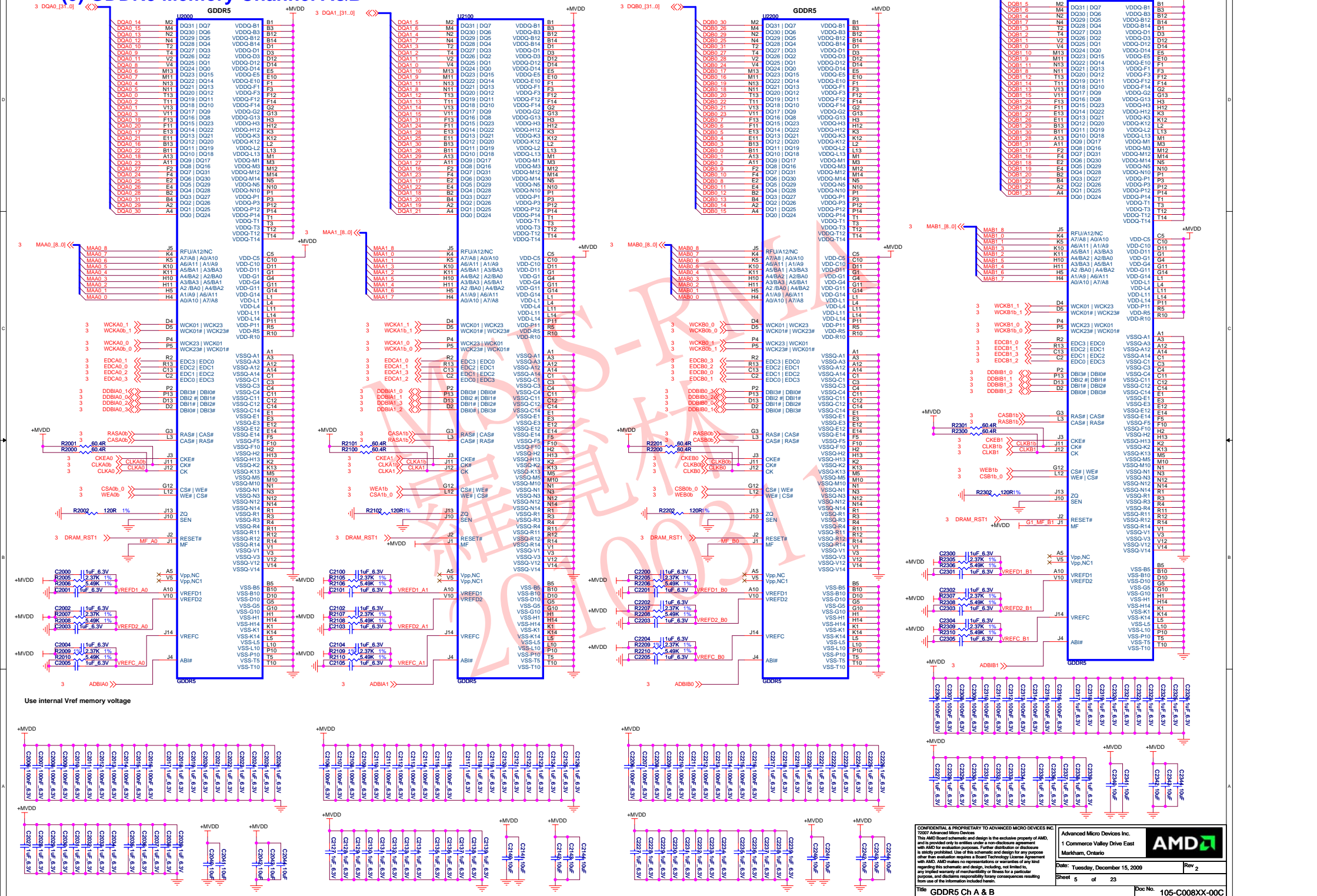
(3) CYPRESS MEM Interface Ch A&B



# (4) CYPRESS MEM Interface Ch C&D

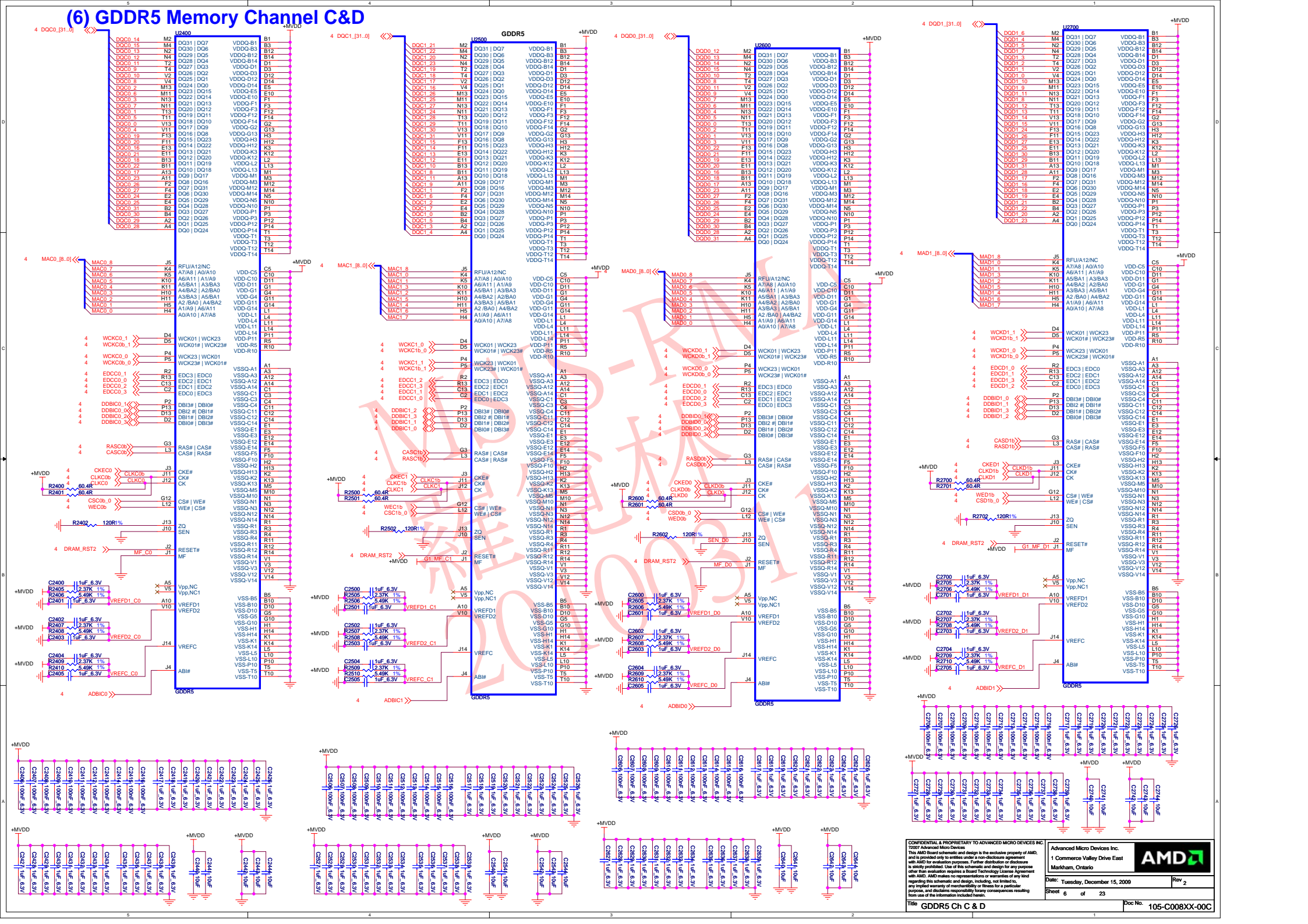


## (5) GDDR5 Memory Channel A&B





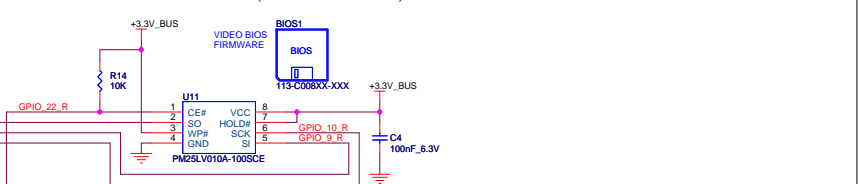
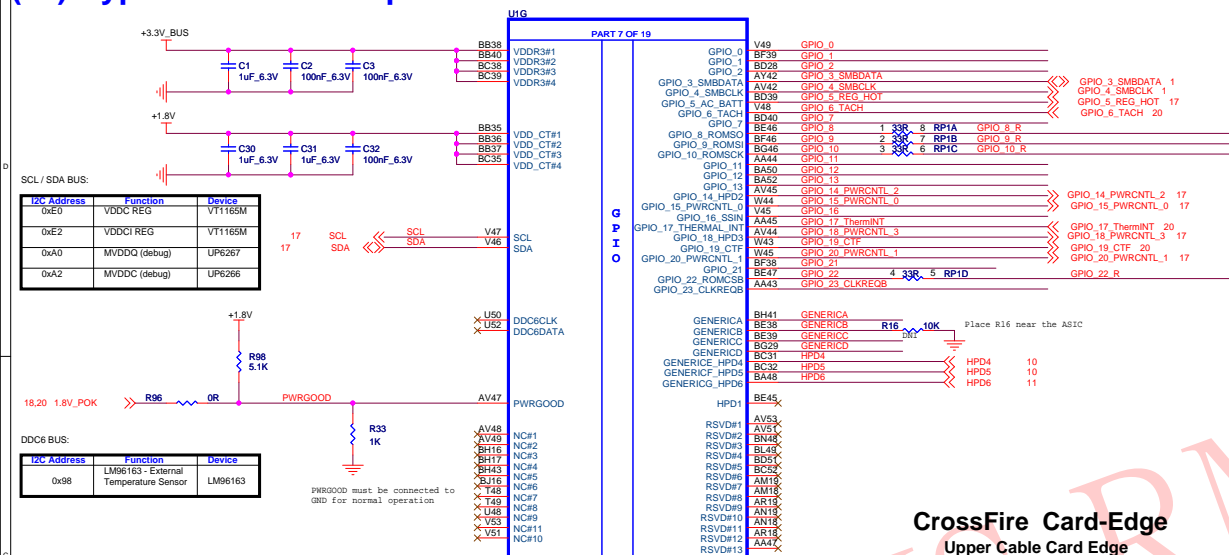
# (6) GDDR5 Memory Channel C&D



CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
2007 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

Advanced Micro Devices Inc.  
1 Commerce Valley Drive East  
Markham, Ontario  
Date: Tuesday, December 15, 2009  
Sheet 6 of 23  
Doc No. 105-C008XX-00C

(07) Cypress GPIOs Strap CF XTAL OSC

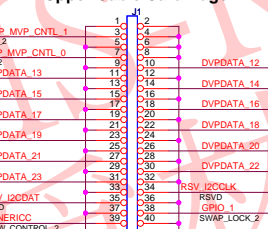


## PIN BASED STRAPS

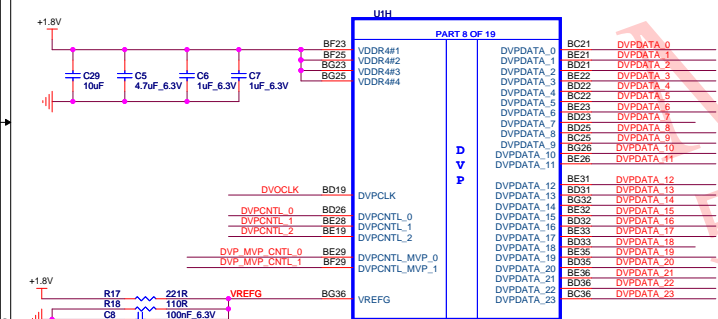
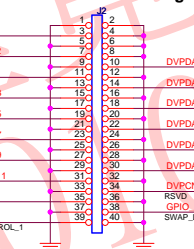



## CrossFire Card-Edge


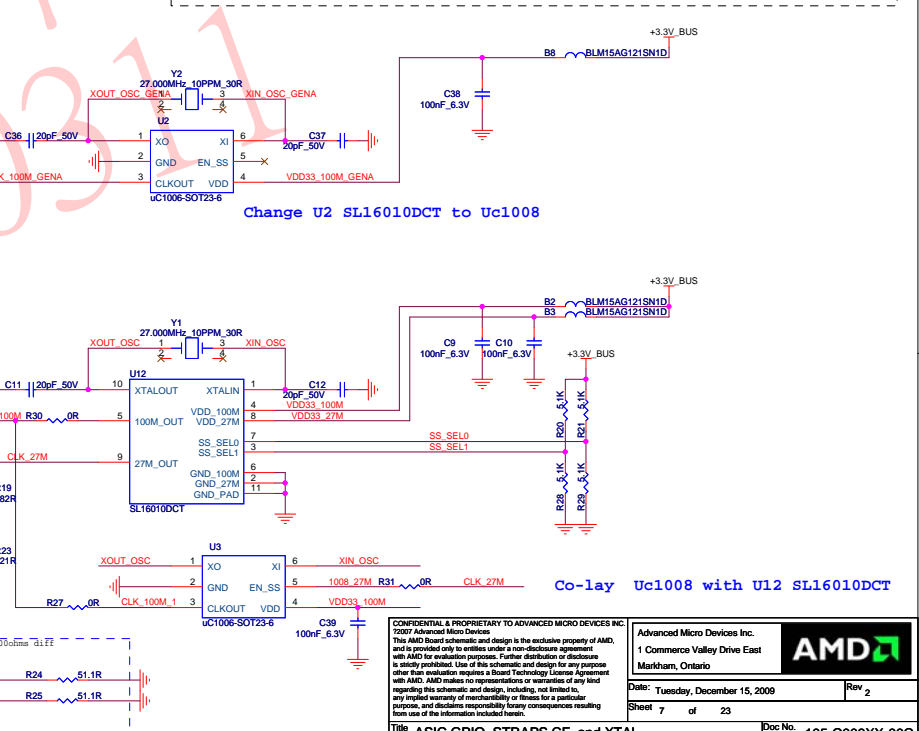
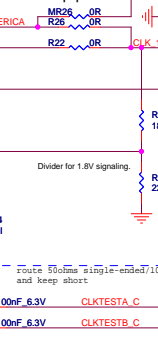
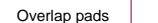
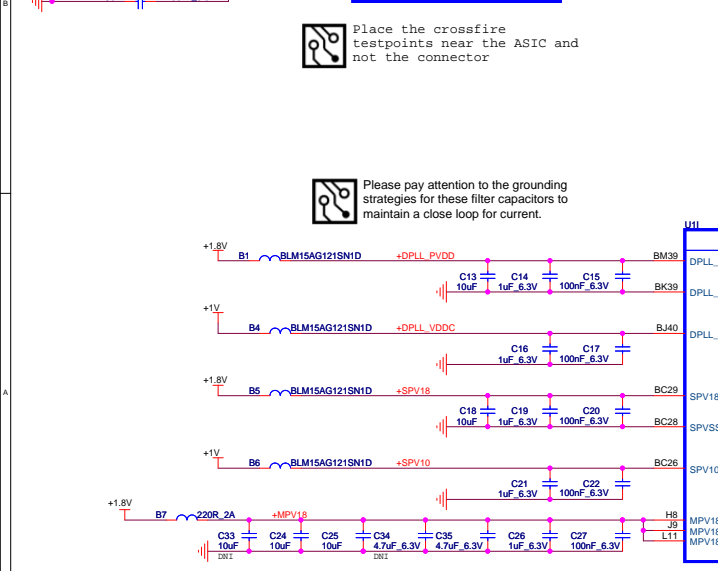
### Upper Cable Card Edge



### Lower Cable Card Edge




 Place the crossfire testpoints near the ASIC and not the connector

 Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

**THIS CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC. 72007 Advanced Micro Devices**

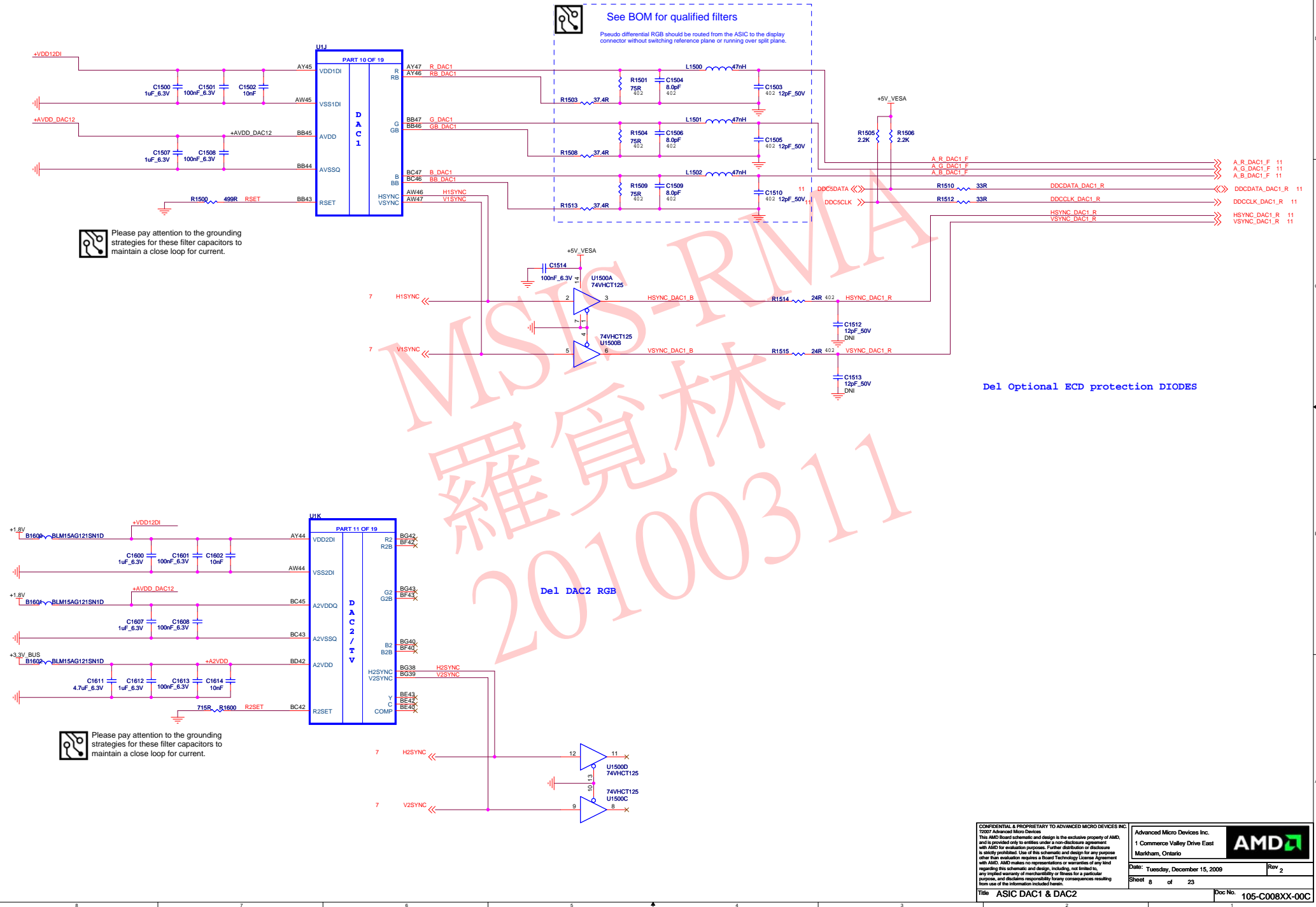
This document and the information contained herein is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Broad Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

**Title: ASIC DRIO, STRAPS OF**

Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario			
Date: Tuesday, December 15, 2009		Rev 2	
Sheet 7 of 23		Doc No. 105-0000000000	

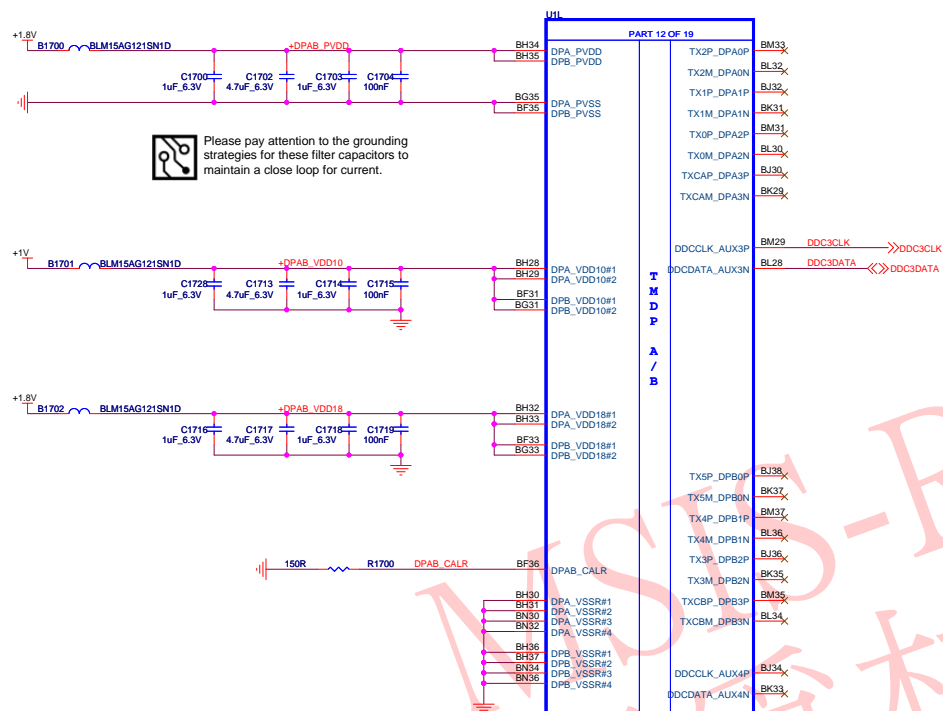
(08) CYPRESS DAC1 and DAC2

Del Optional ECD protection DIODES

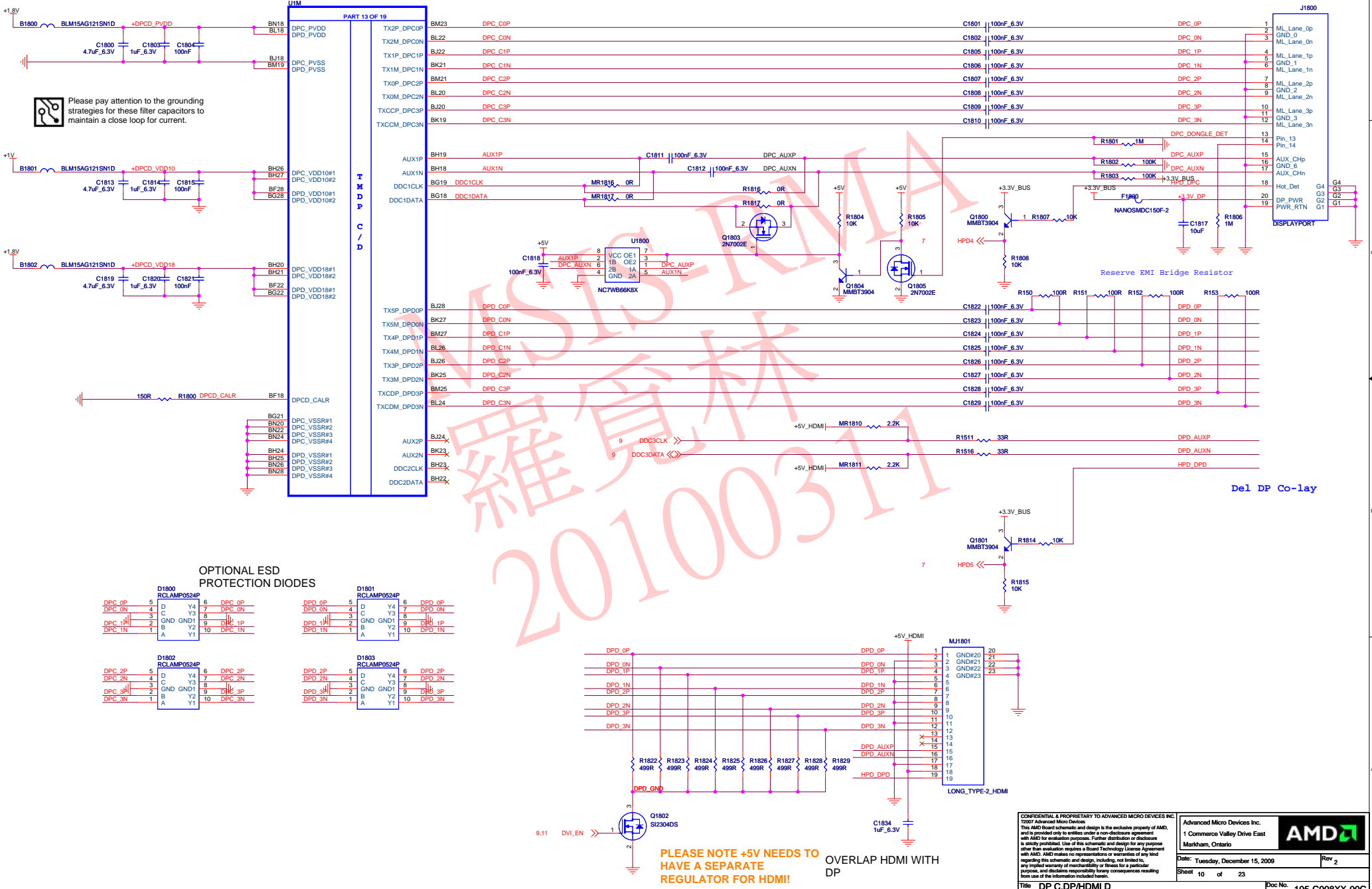




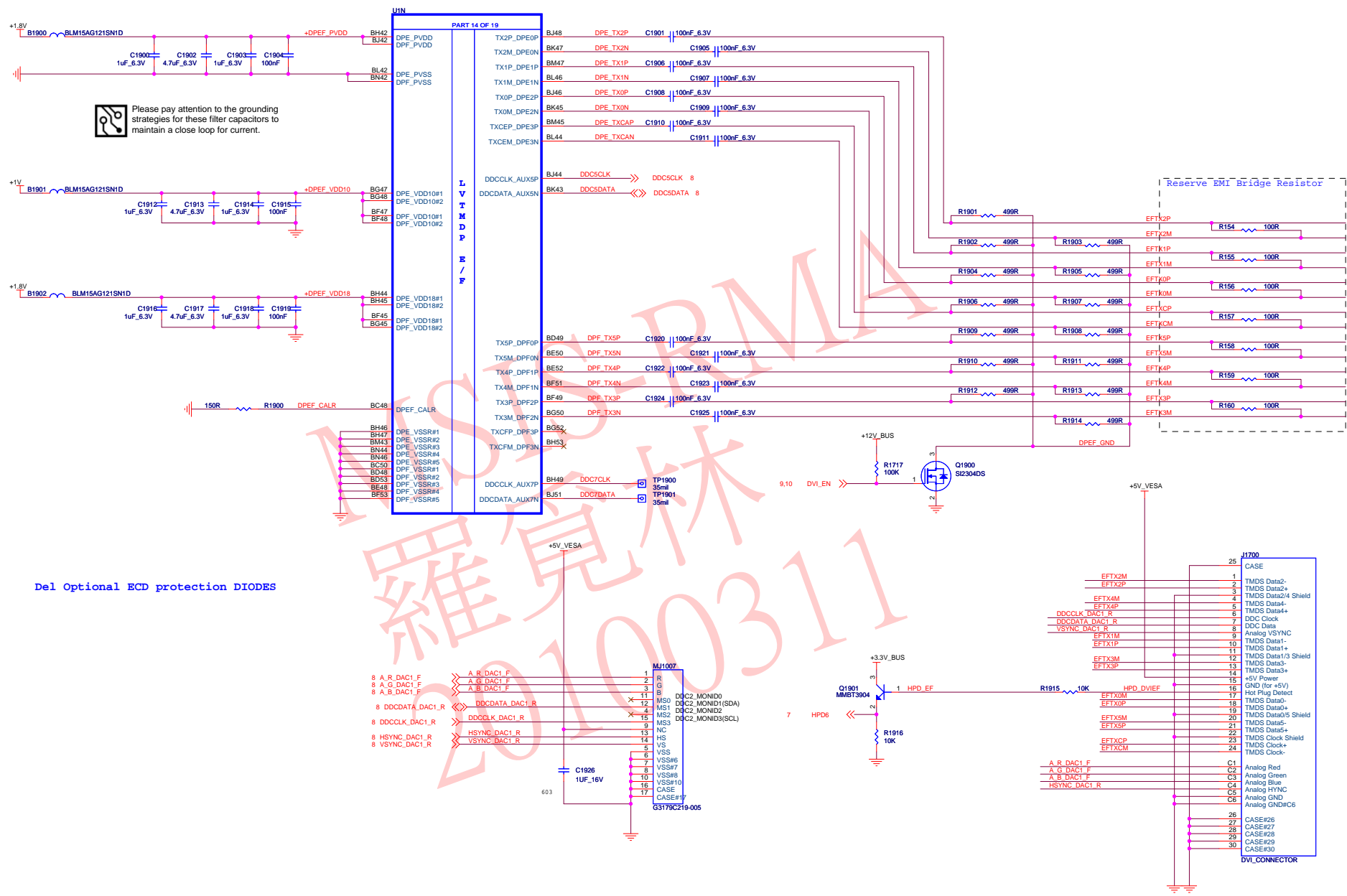
**(09) CYPRESS TMDS A&B**



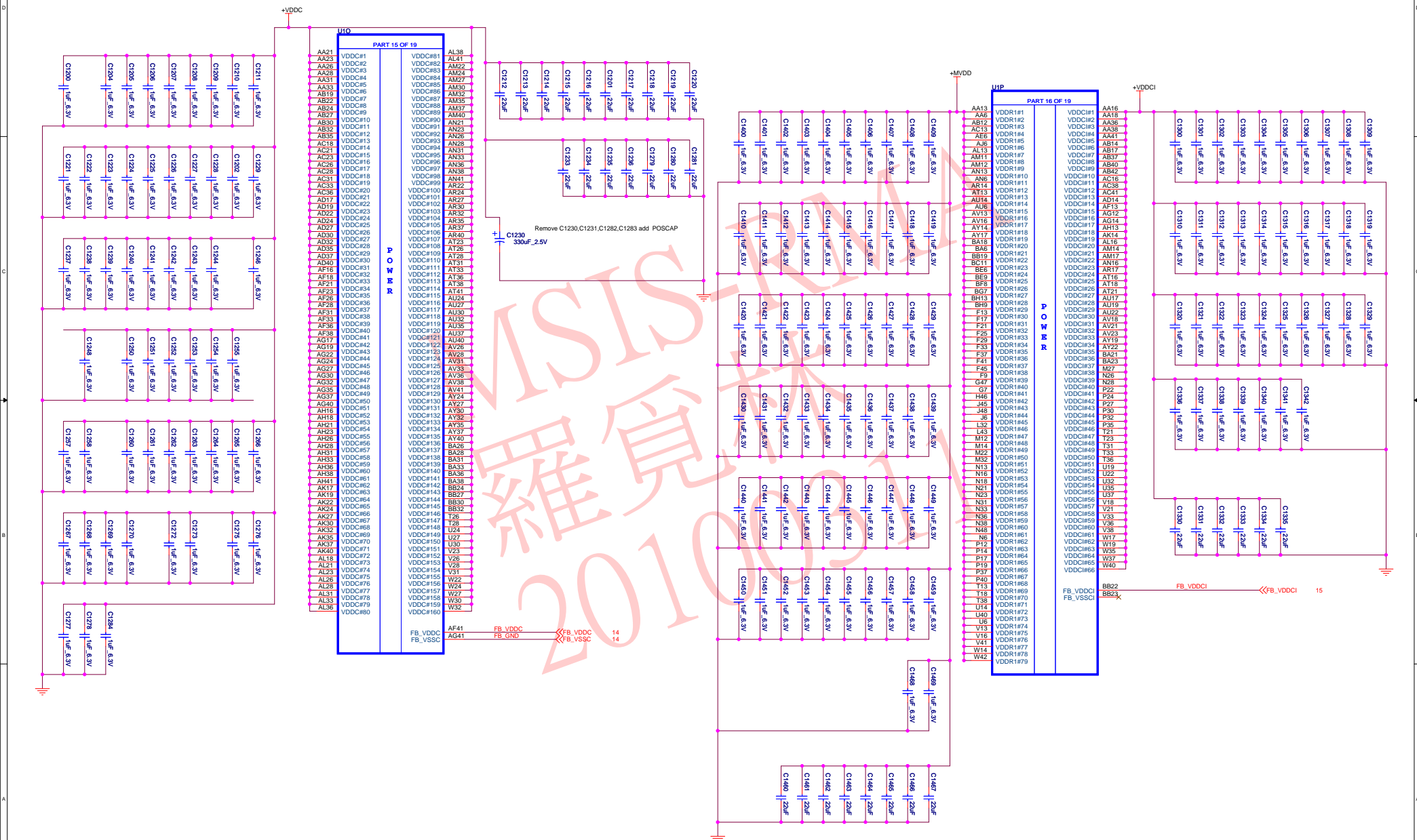
(10) CYPRESS Display Port/HDMI C&D



(11) CYPRESS LVTMDP E&F



## (12) CYPRESS Power

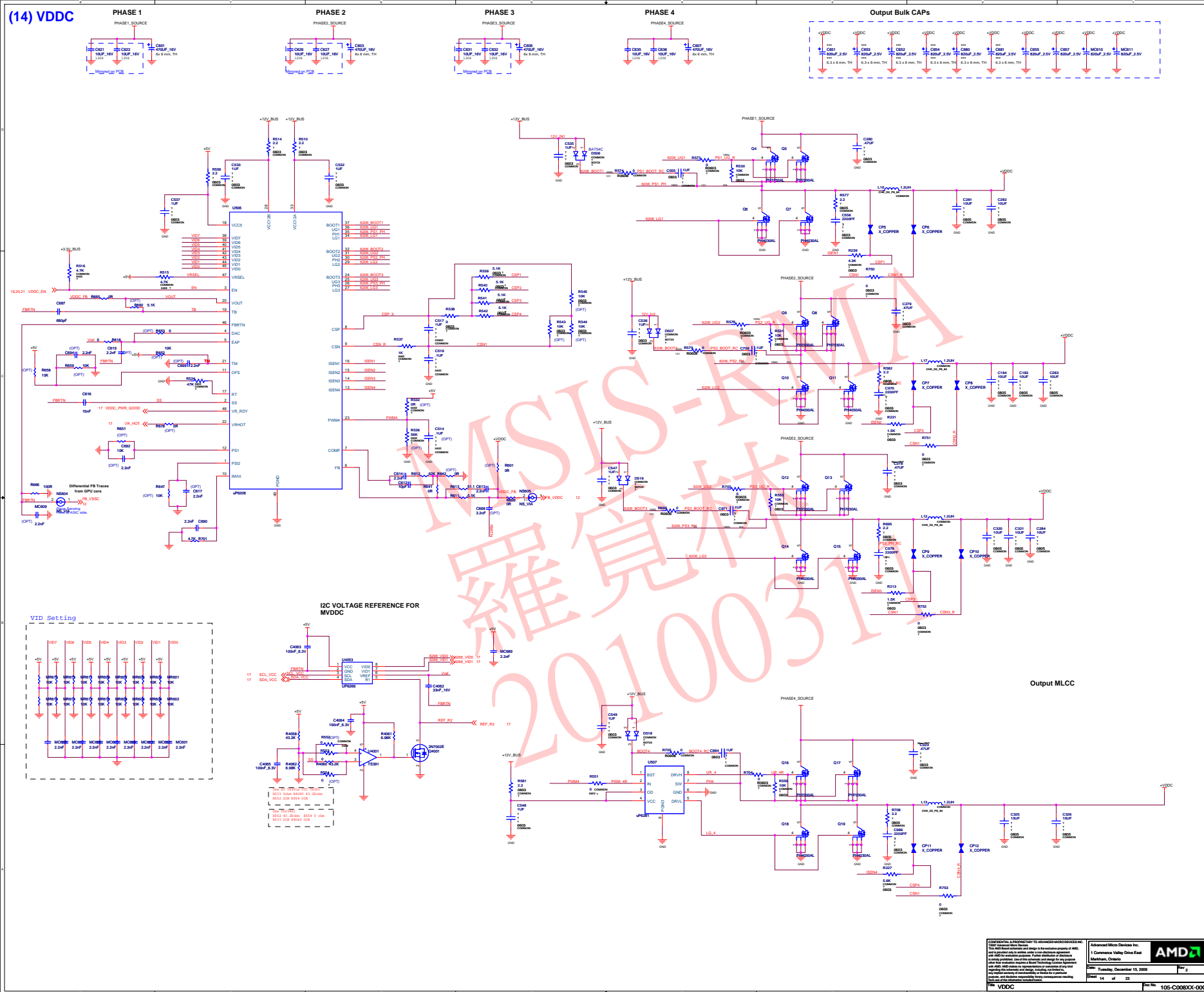


(13) CYPRESS GND

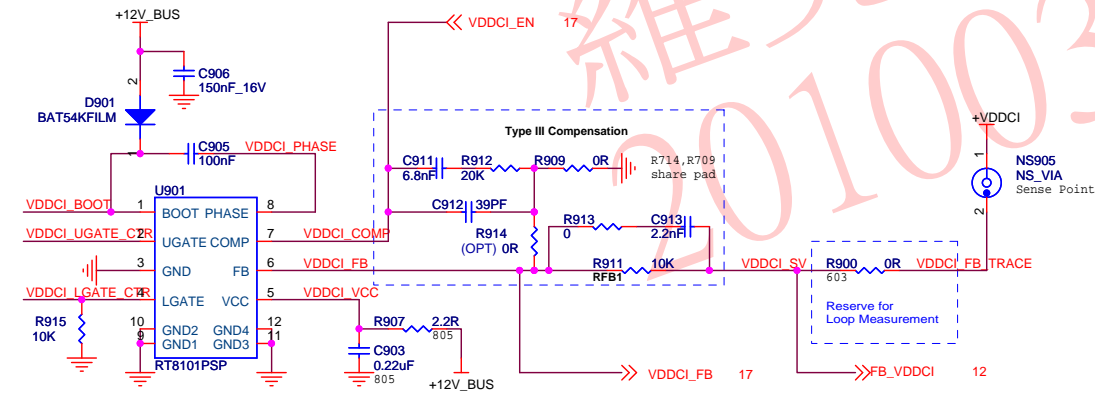
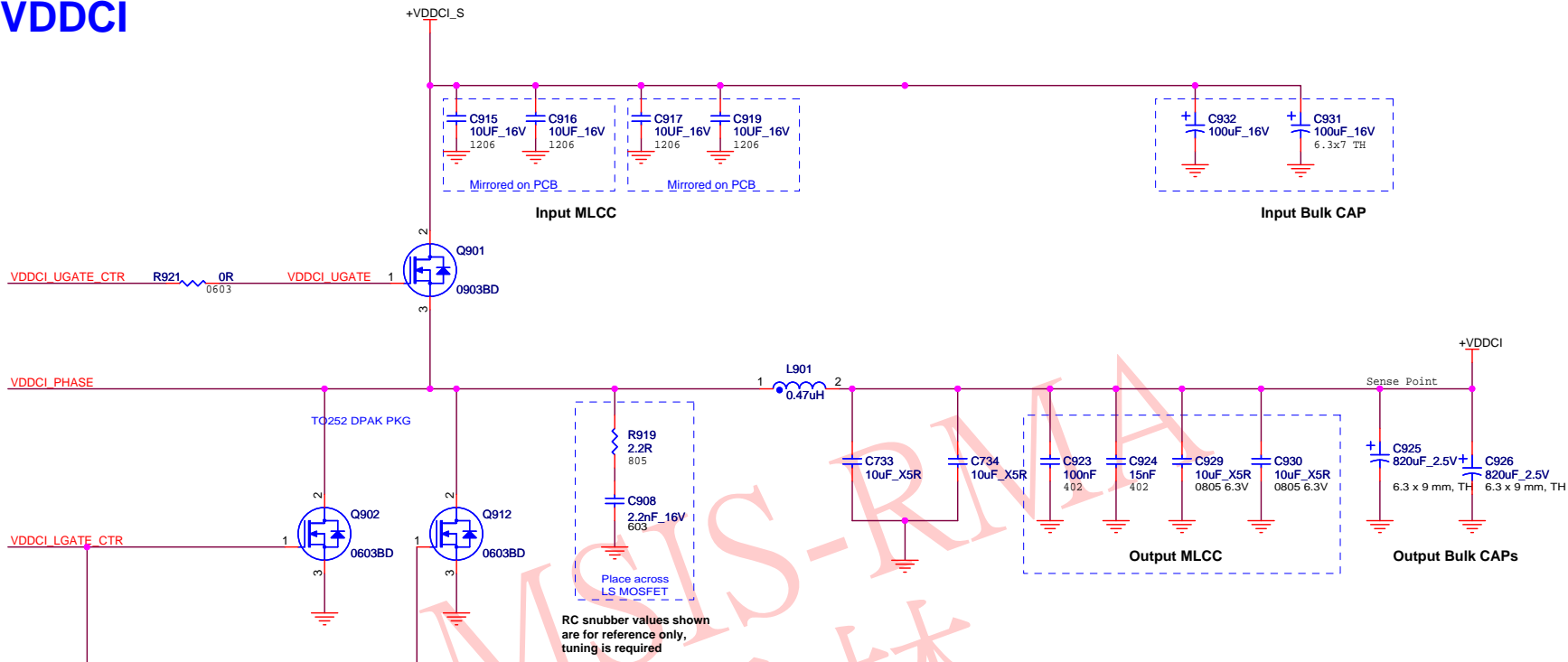
UIC			UIR		
PART 17 OF 19			PART 18 OF 19		
A46	VSS#1	AM0	BA17	VSS#251	L42
AA10	VSS#2	AM13	BA10	VSS#252	L48
AA14	VSS#3	AM16	BA2	VSS#253	L52
AA17	VSS#4	AM21	BA22	VSS#254	L5
AA19	VSS#5	AM23	BA21	VSS#255	VSS#379
AA2	VSS#6	AM26	BA27	VSS#256	M13
AA22	VSS#7	AM28	BA30	VSS#257	VSS#381
AA24	VSS#8	AM31	BA32	VSS#258	VSS#382
AA27	VSS#9	AM33	BA35	VSS#259	VSS#383
AA30	VSS#10	AM36	BA37	VSS#260	VSS#384
AA32	VSS#11	AM38	BA40	VSS#261	VSS#385
AA35	VSS#12	AM41	BA41	VSS#262	VSS#386
AA37	VSS#13	AM44	BA42	VSS#263	VSS#387
AA39	VSS#14	AM47	BA43	VSS#264	VSS#388
AA40	VSS#15	AM50	BA44	VSS#265	VSS#389
AA42	VSS#16	AM53	BA45	VSS#266	N2
AA4	VSS#17	AM56	BA46	VSS#267	VSS#391
AB13	VSS#18	AM59	BA47	VSS#268	N22
AB16	VSS#19	AM62	BA48	VSS#269	VSS#392
AB18	VSS#20	AM65	BA49	VSS#270	VSS#393
AB21	VSS#21	AM68	BA50	VSS#271	N30
AB23	VSS#22	AM71	BA51	VSS#272	N32
AB26	VSS#23	AM74	BA52	VSS#273	N35
AB28	VSS#24	AM77	BA53	VSS#274	VSS#397
AB31	VSS#25	AM80	BA54	VSS#275	N40
AB33	VSS#26	AM83	BA55	VSS#276	VSS#398
AB36	VSS#27	AM86	BA56	VSS#277	VSS#399
AB38	VSS#28	AM89	BA57	VSS#278	P13
AB41	VSS#29	AM92	BA58	VSS#279	VSS#401
AB43	VSS#30	AM95	BA59	VSS#280	P18
AB46	VSS#31	AM98	BA60	VSS#281	VSS#403
AB48	VSS#32	AM101	BA61	VSS#282	VSS#404
AB51	VSS#33	AM104	BA62	VSS#283	VSS#405
AB53	VSS#34	AM107	BA63	VSS#284	P28
AB56	VSS#35	AM110	BA64	VSS#285	VSS#406
AB58	VSS#36	AM113	BA65	VSS#286	VSS#407
AB61	VSS#37	AM116	BA66	VSS#287	VSS#408
AB63	VSS#38	AM119	BA67	VSS#288	P33
AB66	VSS#39	AM122	BA68	VSS#289	VSS#409
AB68	VSS#40	AM125	BA69	VSS#290	VSS#410
AB71	VSS#41	AM128	BA70	VSS#291	P41
AB73	VSS#42	AM131	BA71	VSS#292	VSS#412
AB76	VSS#43	AM134	BA72	VSS#293	P43
AB78	VSS#44	AM137	BA73	VSS#294	VSS#413
AB81	VSS#45	AM140	BA74	VSS#295	P45
AB83	VSS#46	AM143	BA75	VSS#296	VSS#414
AB86	VSS#47	AM146	BA76	VSS#297	P48
AB88	VSS#48	AM149	BA77	VSS#298	VSS#415
AB91	VSS#49	AM152	BA78	VSS#299	P5
AB93	VSS#50	AM155	BA79	VSS#300	VSS#422
AB96	VSS#51	AM158	BA80	VSS#301	R50
AB98	VSS#52	AM161	BA81	VSS#302	VSS#423
AB101	VSS#53	AM164	BA82	VSS#303	R5
AB103	VSS#54	AM167	BA83	VSS#304	VSS#425
AB106	VSS#55	AM170	BA84	VSS#305	VSS#426
AB108	VSS#56	AM173	BA85	VSS#306	VSS#427
AB111	VSS#57	AM176	BA86	VSS#307	VSS#428
AB113	VSS#58	AM179	BA87	VSS#308	T24
AB116	VSS#59	AM182	BA88	VSS#309	VSS#429
AB118	VSS#60	AM185	BA89	VSS#310	T27
AB121	VSS#61	AM188	BA90	VSS#311	VSS#431
AB123	VSS#62	AM191	BA91	VSS#312	T30
AB126	VSS#63	AM194	BA92	VSS#313	T32
AB128	VSS#64	AM197	BA93	VSS#314	VSS#433
AB131	VSS#65	AM200	BA94	VSS#315	T36
AB133	VSS#66	AM203	BA95	VSS#316	VSS#434
AB136	VSS#67	AM206	BA96	VSS#317	T40
AB138	VSS#68	AM209	BA97	VSS#318	VSS#435
AB141	VSS#69	AM212	BA98	VSS#319	T42
AB143	VSS#70	AM215	BA99	VSS#320	VSS#437
AB146	VSS#71	AM218	BA100	VSS#321	T43
AB148	VSS#72	AM221	BA101	VSS#322	VSS#438
AB151	VSS#73	AM224	BA102	VSS#323	VSS#439
AB153	VSS#74	AM227	BA103	VSS#324	T46
AB156	VSS#75	AM230	BA104	VSS#325	VSS#440
AB158	VSS#76	AM233	BA105	VSS#326	T53
AB161	VSS#77	AM236	BA106	VSS#327	VSS#441
AB163	VSS#78	AM239	BA107	VSS#328	VSS#442
AB166	VSS#79	AM242	BA108	VSS#329	T8
AB168	VSS#80	AM245	BA109	VSS#330	T13
AB171	VSS#81	AM248	BA110	VSS#331	VSS#443
AB173	VSS#82	AM251	BA111	VSS#332	VSS#444
AB176	VSS#83	AM254	BA112	VSS#333	VSS#445
AB178	VSS#84	AM257	BA113	VSS#334	VSS#446
AB181	VSS#85	AM260	BA114	VSS#335	VSS#447
AB183	VSS#86	AM263	BA115	VSS#336	VSS#448
AB186	VSS#87	AM266	BA116	VSS#337	VSS#449
AB188	VSS#88	AM269	BA117	VSS#338	VSS#450
AB191	VSS#89	AM272	BA118	VSS#339	VSS#451
AB193	VSS#90	AM275	BA119	VSS#340	VSS#452
AB196	VSS#91	AM278	BA120	VSS#341	VSS#453
AB198	VSS#92	AM281	BA121	VSS#342	VSS#454
AB201	VSS#93	AM284	BA122	VSS#343	VSS#455
AB203	VSS#94	AM287	BA123	VSS#344	VSS#456
AB206	VSS#95	AM290	BA124	VSS#345	VSS#457
AB208	VSS#96	AM293	BA125	VSS#346	VSS#458
AB211	VSS#97	AM296	BA126	VSS#347	VSS#459
AB213	VSS#98	AM299	BA127	VSS#348	VSS#460
AB216	VSS#99	AM302	BA128	VSS#349	VSS#461
AB218	VSS#100	AM305	BA129	VSS#350	VSS#462
AB221	VSS#101	AM308	BA130	VSS#351	VSS#463
AB223	VSS#102	AM311	BA131	VSS#352	VSS#464
AB226	VSS#103	AM314	BA132	VSS#353	VSS#465
AB228	VSS#104	AM317	BA133	VSS#354	VSS#466
AB231	VSS#105	AM320	BA134	VSS#355	VSS#467
AB233	VSS#106	AM323	BA135	VSS#356	VSS#468
AB236	VSS#107	AM326	BA136	VSS#357	VSS#469
AB238	VSS#108	AM329	BA137	VSS#358	VSS#470
AB241	VSS#109	AM332	BA138	VSS#359	VSS#471
AB243	VSS#110	AM335	BA139	VSS#360	VSS#472
AB246	VSS#111	AM338	BA140	VSS#361	VSS#473
AB248	VSS#112	AM341	BA141	VSS#362	VSS#474
AB251	VSS#113	AM344	BA142	VSS#363	VSS#475
AB253	VSS#114	AM347	BA143	VSS#364	VSS#476
AB256	VSS#115	AM350	BA144	VSS#365	VSS#477
AB258	VSS#116	AM353	BA145	VSS#366	VSS#478
AB261	VSS#117	AM356	BA146	VSS#367	VSS#479
AB263	VSS#118	AM359	BA147	VSS#368	VSS#480
AB266	VSS#119	AM362	BA148	VSS#369	VSS#481
AB268	VSS#120	AM365	BA149	VSS#370	VSS#482
AB271	VSS#121	AM368	BA150	VSS#371	VSS#483
AB273	VSS#122	AM371	BA151	VSS#372	VSS#484
AB276	VSS#123	AM374	BA152	VSS#373	VSS#485
AB278	VSS#124	AM377	BA153	VSS#374	VSS#486
AB281	VSS#125	AM380	BA154	VSS#375	VSS#487



# (14) VDDC

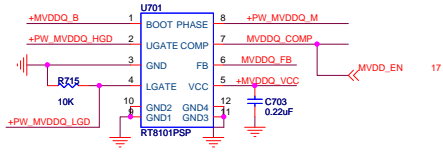


(15) VDDCI



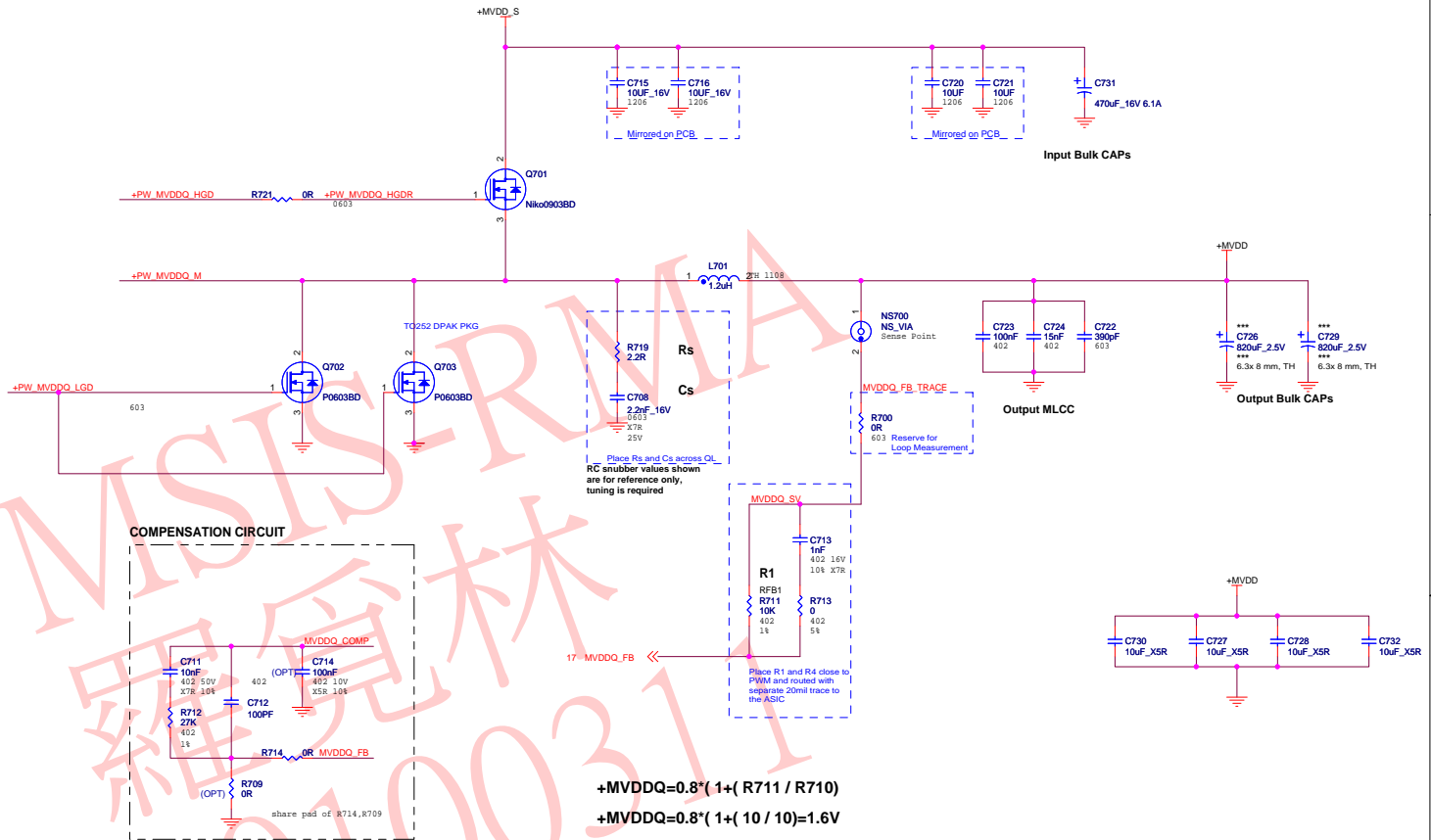


# (16) MVDDQ



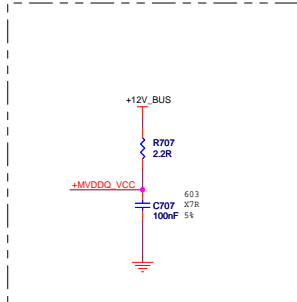
## Layout guideline

- 1-Position the controller (U703) such that LGate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces (PW\_MVDDQ\_LGD and PW\_MVDDQ\_HGD) as short and as wide as possible to reduce the trace inductance.
- 2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows:  
Vcc bypass cap is C703, and Boost cap is C705.
- 3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C711 and C712.

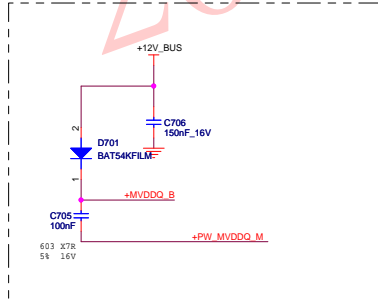


$$+MVDDQ = 0.8 * (1 + (R711 / R710))$$
$$+MVDDQ = 0.8 * (1 + (10 / 10)) = 1.6V$$

## FILTERED SMPS VCC



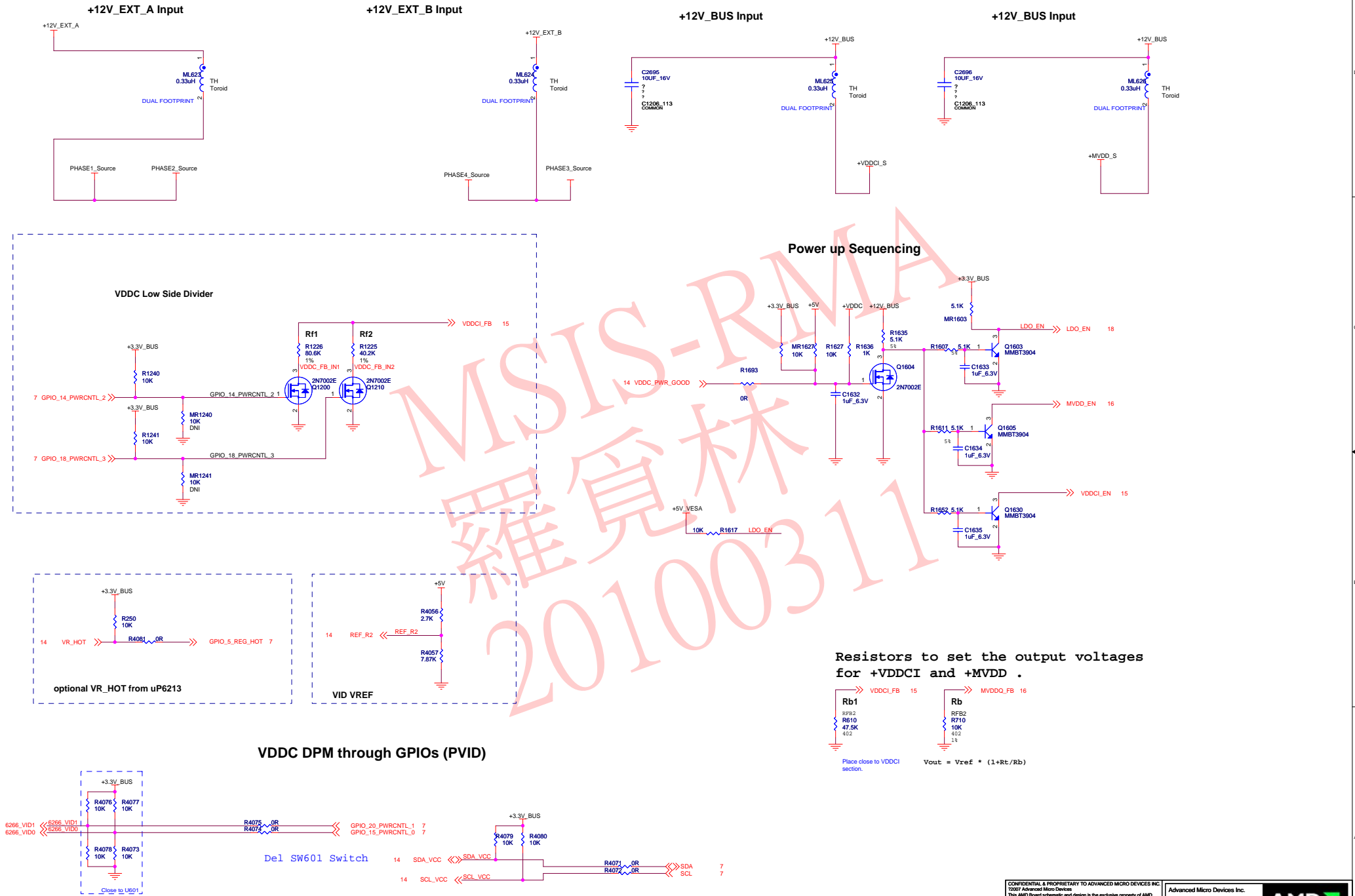
## BOOT CIRCUIT



CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
7207 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

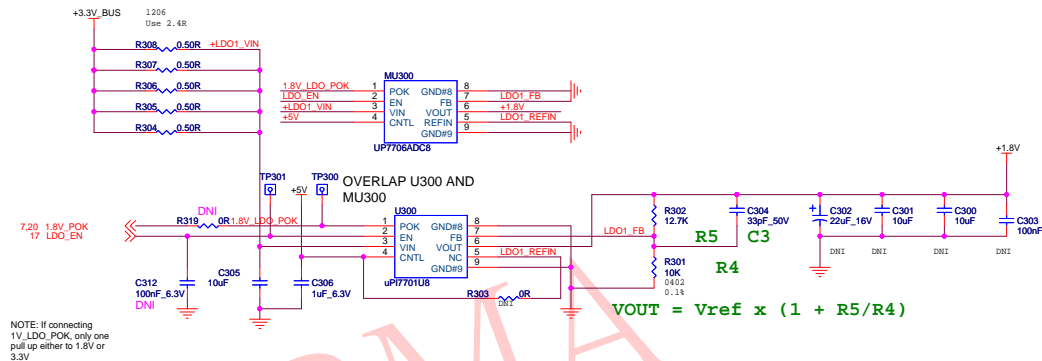
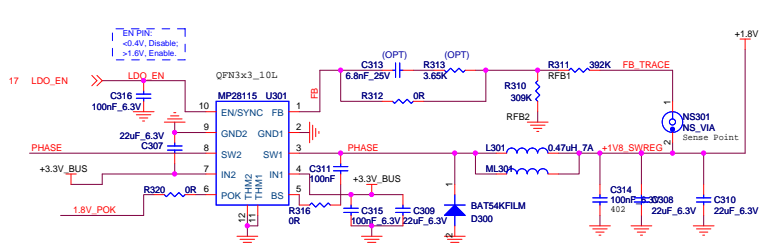
Advanced Micro Devices Inc.  
1 Commerce Valley Drive East  
Markham, Ontario  
Date: Tuesday, December 15, 2009  
Sheet 16 of 23  
Rev 2  
Doc No. 105-C008XX-00C

(17) CYPRESS VDDCI POWER PLAY



## (18) CYPRESS Small Rail Regulators

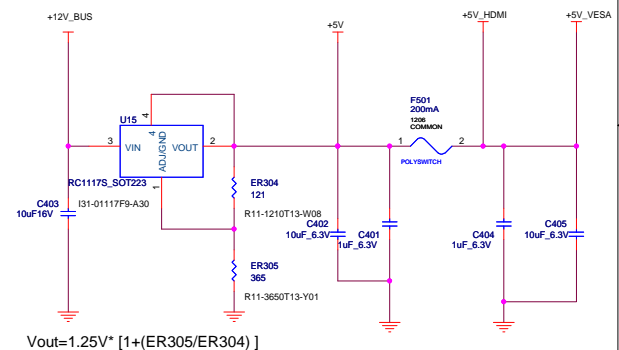
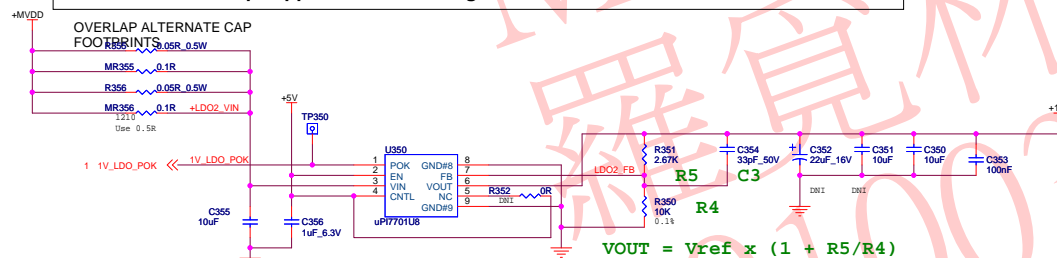
**LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX**  
**PCB: 50 to 70mm sq. copper area for cooling**



NOTE: If connecting 1V\_LDO\_POK, only one pull up either to 1.8V or 3.3V

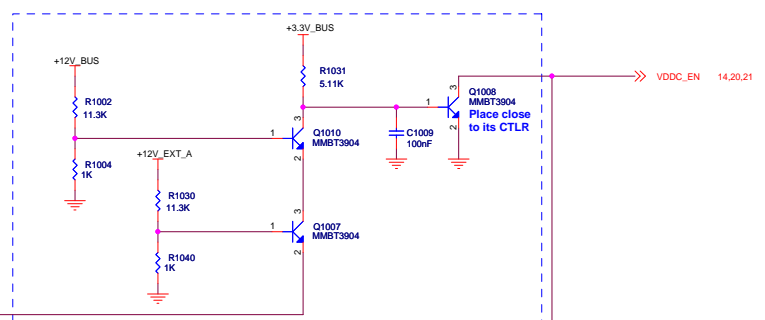
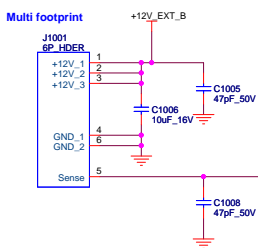
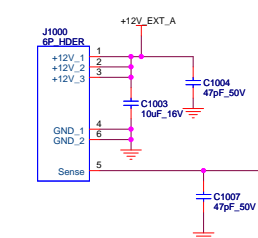
**optional 5V power for VDDC regulator;**

**LDO #2: Vin = +1.35V to 1.8VMAX    Vout = +1V +/- 2%    Iout = 1.7A (TBV) RMS MAX**  
**PCB: 50 to 70mm sq. copper area for cooling**

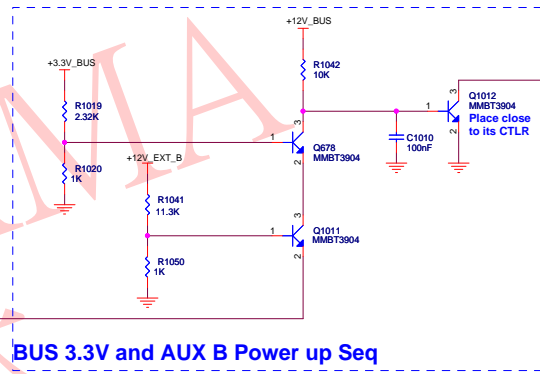




(19) CYPRESS POWER MGMNT

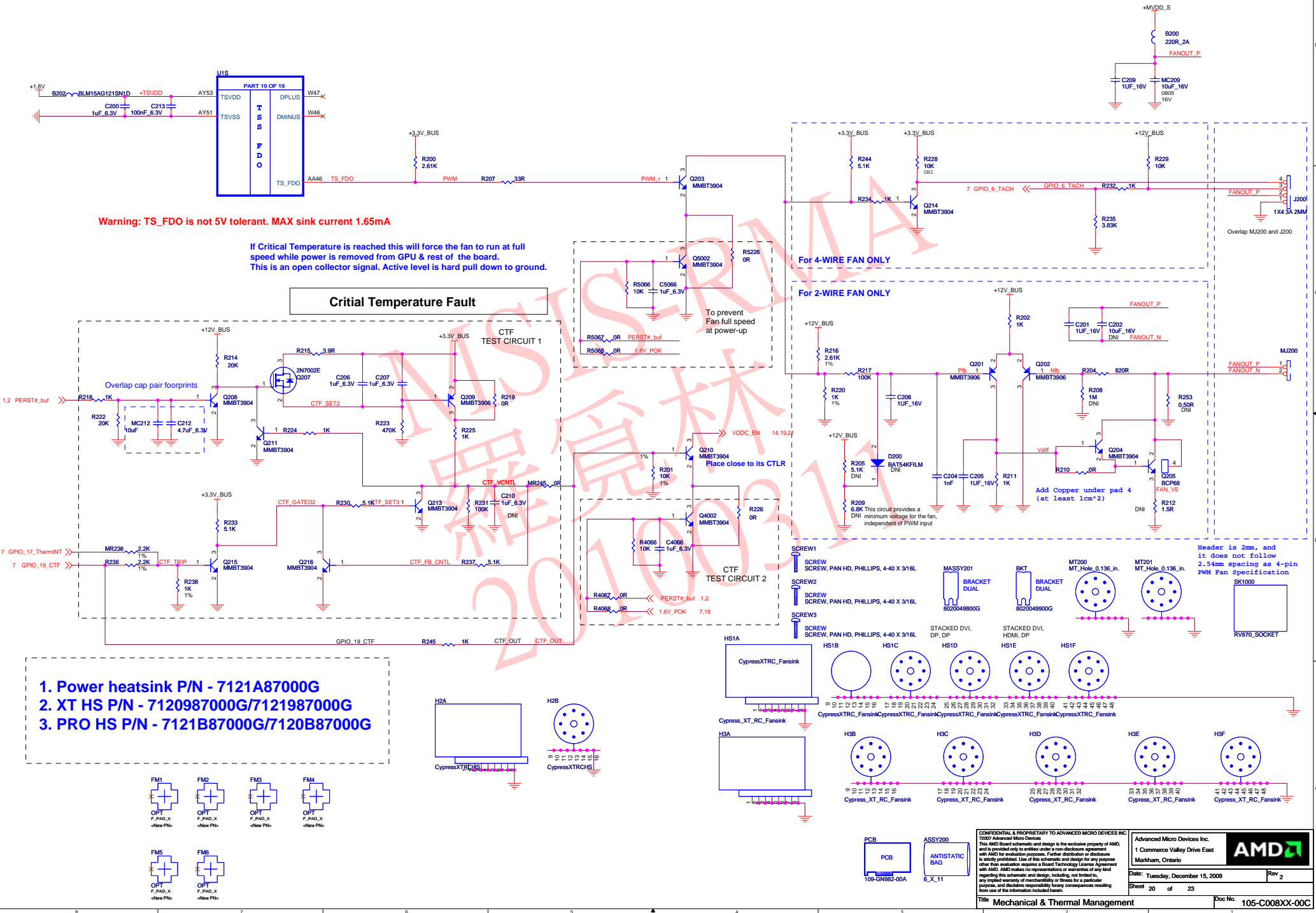


BUS 12V and AUX A Power up Seq

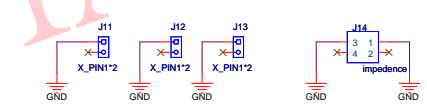
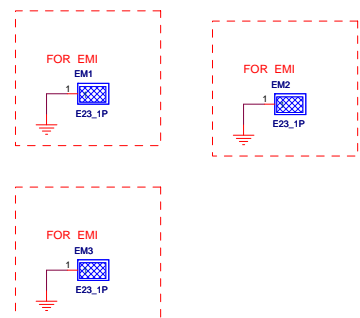
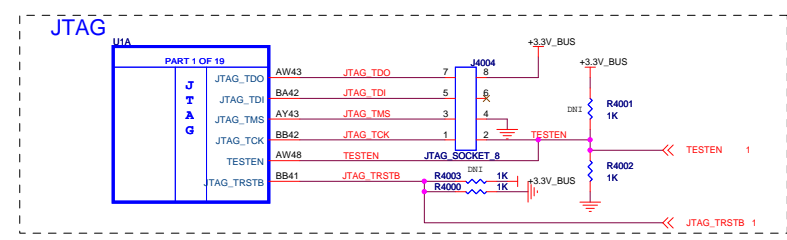


BUS 3.3V and AUX B Power up Seq

(20) CYPRESS Mechanical and Thermal Management



(21) CYPRESS Debug Circuits



Del PTC protect circuit.

MSIS-RMA  
羅覓林  
20100311





Title			Schematic No.	Date:
RH CYPRESS GDDR5 DP-HDMI-DVII-DVII			105-C008XX-00C	Tuesday, December 15, 2009
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.	
			Rev	2
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION	
0	00A	09/08/11		
1	00B	09/08/26		
2	00C	09/09/24	Initial release. Based on Cypress XT C001 00 PCB	
V209-0A		09/10/12	Based on Cypress XT C008 0C PCB 1. Page 7 Change U2 SL16010DCT to Uc1006 and Co-lay Uc1008 with U12 SL16010DCT 2. Page 8 Del DAC2 RGB 3. Page 9 Disable TMDP AB and disable DDC_AUX3,DDC_AUX4 4. Page 10 Del DP co-lay with HDMI 5. Page 11 Del Dual DVI Connector Change to Single DVI and Co-lay Slim D-Sub 6. Page 12 Remove C1230,C1231,C1282,C1283 add POSCAP 7. Page 14 Change VDDC PWM to Ux6206 8. Page 18 Change +5V circuit. 9. Page 21 Del PTC protect circuit. 10. Page 5,4 changing the DRAM reset circuit 11. Page 10 chang HDMI DDC to DDC3 12. Page 14 co-lay U4001 with TLV3401	
		09/11/2		

MSIS-RMA  
羅覓林  
20100311