

G94-P545-A01 - GDDR3, DVI/VGA + DVI/VGA + HDTV/SDTV-Out

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10545-0000-100	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SRU0100	600-10545-0100-100	G94-400 650MHz/1000MHz 512MB 16MA32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out (Bring Up SRU)
2	SRU0200	600-10545-0200-100	G94-400 650MHz/1000MHz 512MB 16MA32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
3	SRU0310	600-10545-0310-100	G94-300 600MHz/800MHz 512MB 16MA32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
4	SRU0320	600-10545-0320-100	G94-300 600MHz/800MHz 384MB 16MA32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
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V127-0A Base on P545

- 1.PAGE18: ADD Display port circuit
- 2.PAGE21: ADD GPIO circuit
- 3.PAGE 21: change SPDIF circuit
- 4.PAGE 27: remove PEX_VDD power switch circuit
- 5.PAGE 27: remove IFP_PLLVDD/2V5 power switch circuit cahnge APL5713 and APL5910 circuit
- 6.PAGE 28: remove FBVDDQ power switch circuit change APW7067N power circuit
- 7.PAGE 29: remove NVVDD VID circuit
- 8.PAGE 30: change NNVDD POWER APW7088 circuit
- 9.PAGE 16/17 : ADD EMI bridge R
- 10.PAGE 17 CO-LAYOUT HDIM CONNECT
- 11.PAGE 15 remove J2 D_SUB SLIM CONNECT
- 12.PAGE 29 ADD CH7322 circuit

V127-20 Base on V127-0A

- 1.PAGE30 .CO-LAYOUT RT9258 circuit

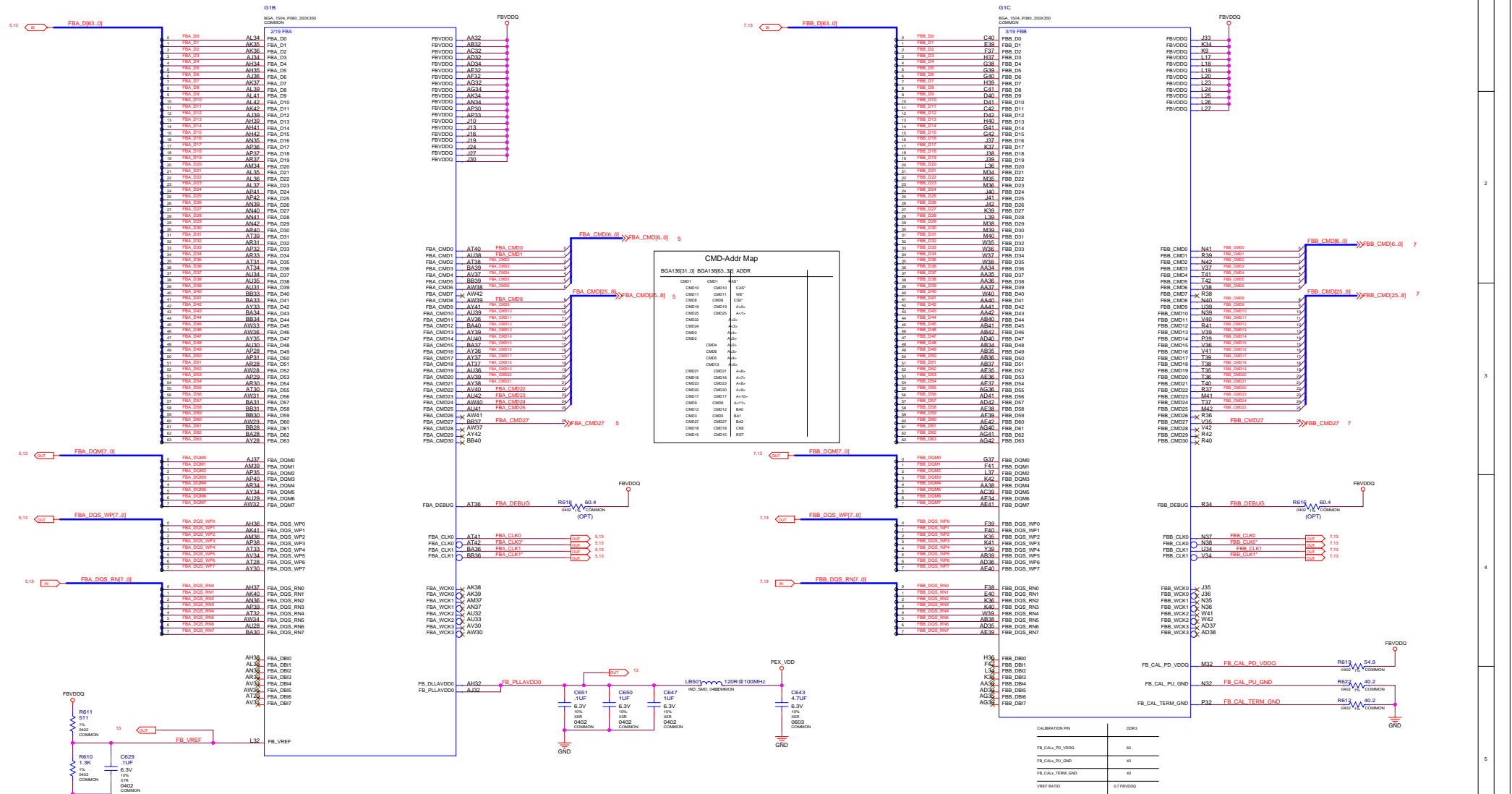
V127-0C Base on V127-20

- 1.PAGE18 remove Display port co-lay circuit
- 2.PAGE32 remove MEC8

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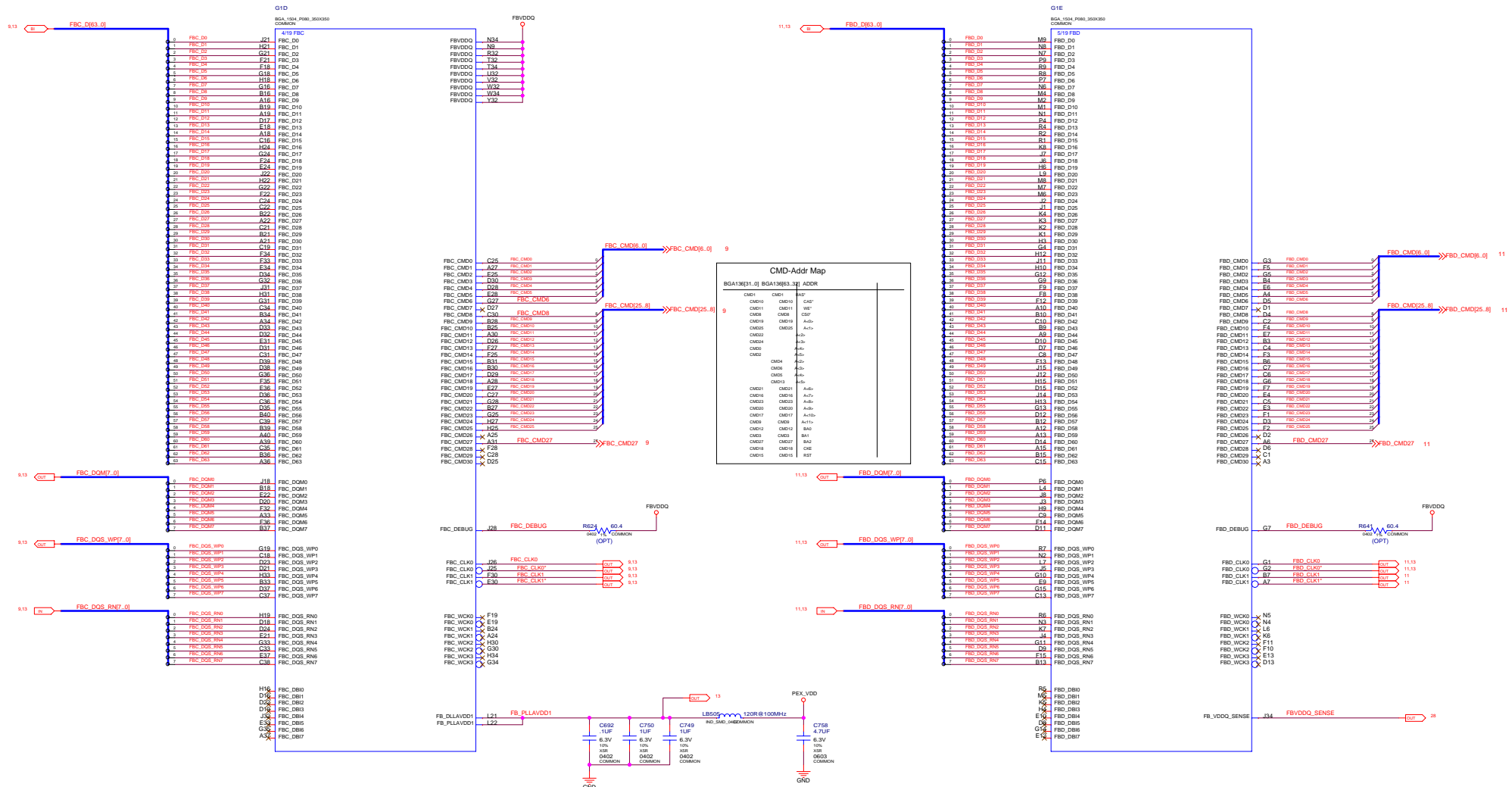
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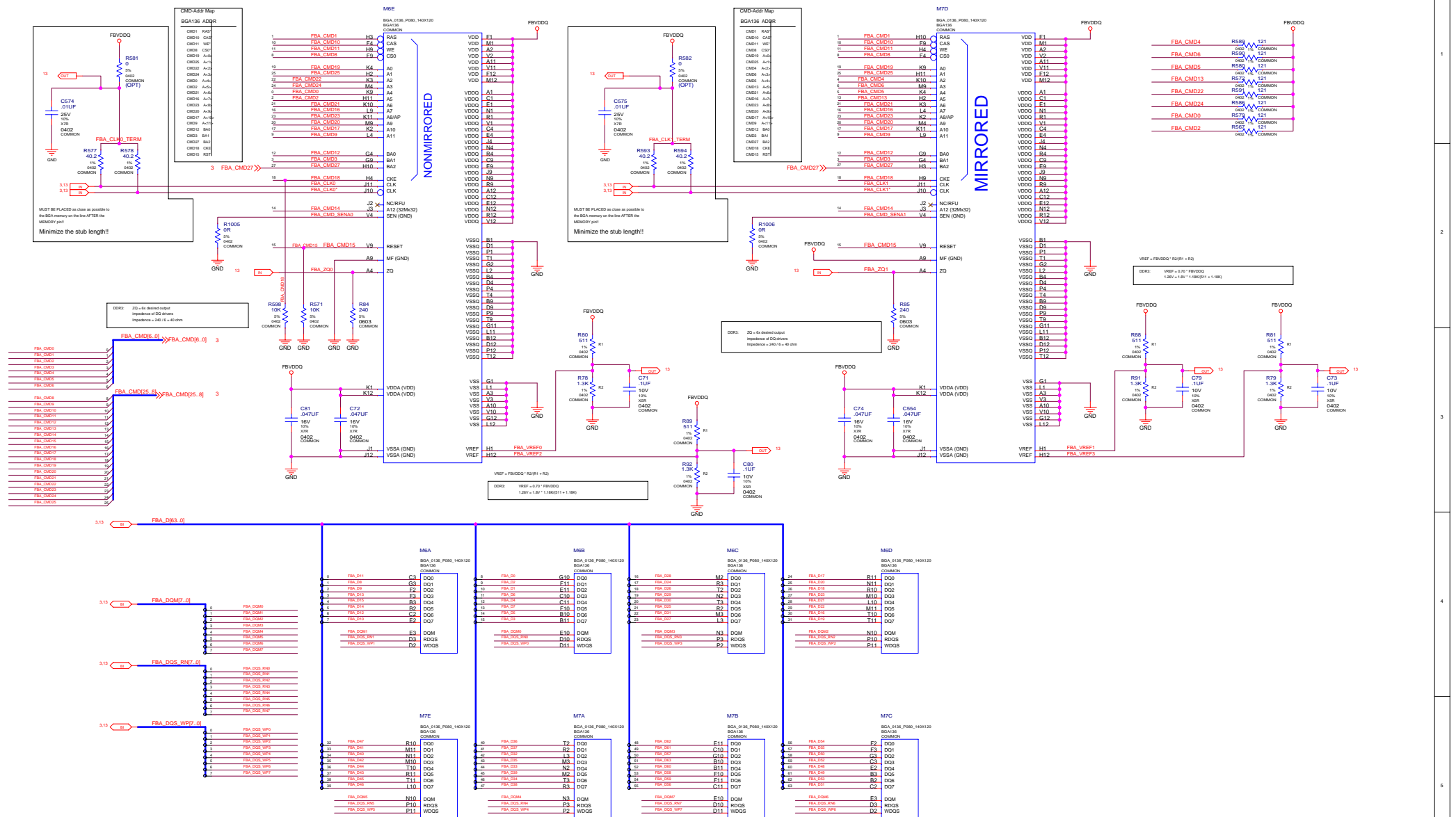


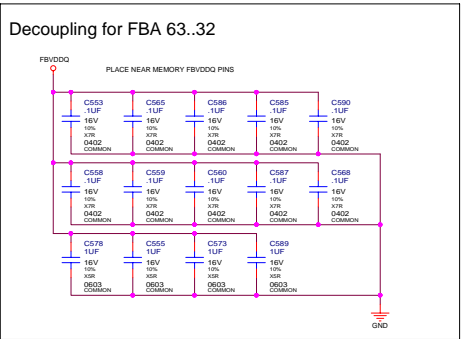
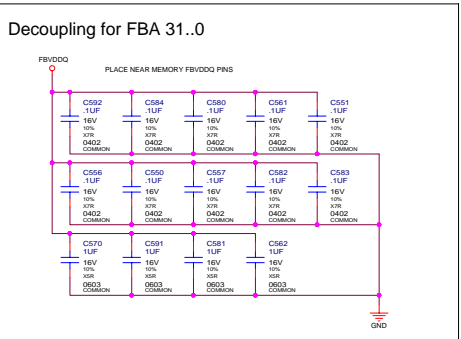
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MEMORY: GPU Partition A/B



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FBA Partition Decoupling

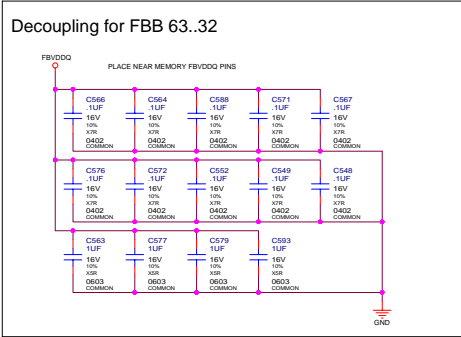
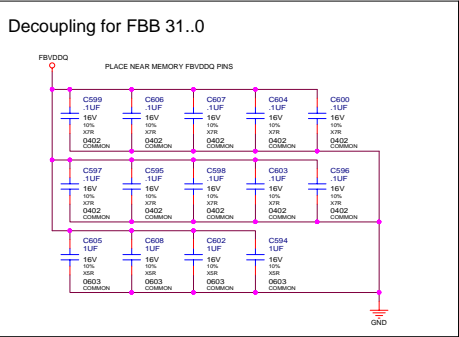


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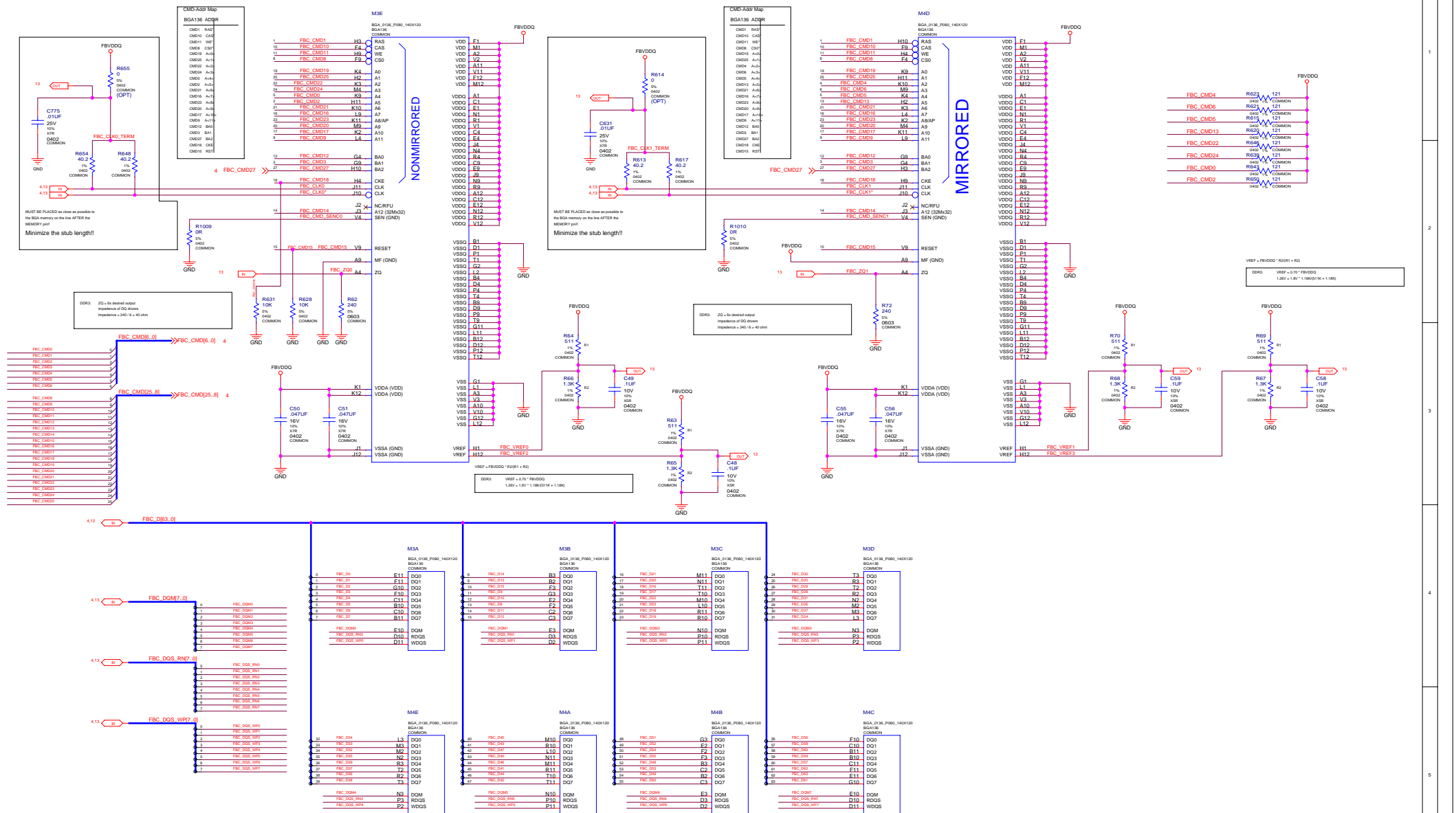
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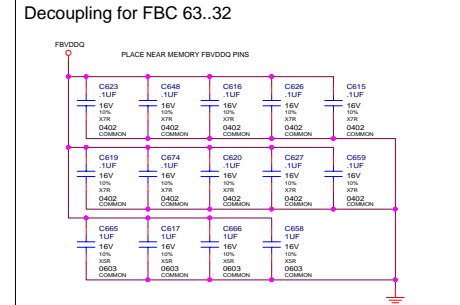
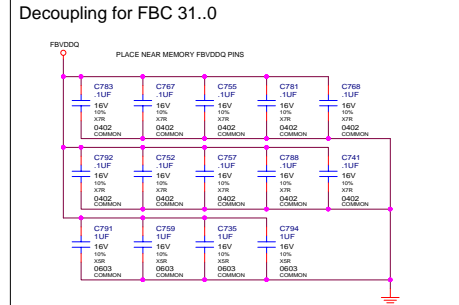
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PAGE DETAIL	FBC Partition Decoupling



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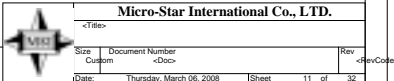
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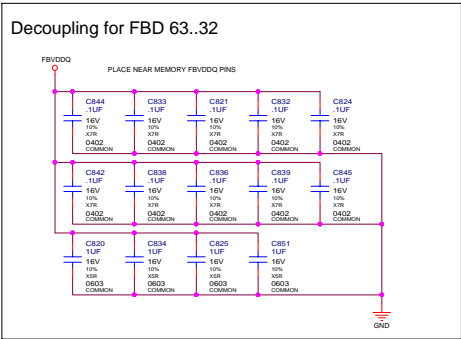
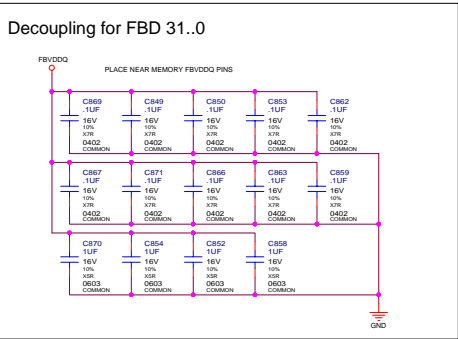
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FBD Partition Decoupling



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3.5	OUT FBA_CLK0	1	800FT	FBA_CLK0
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5	OUT FBA_CLK2_TERM	1	400MM	
3.5	OUT FBA_CLK1	1	800FT	FBA_CLK1
5	OUT FBA_CLK1*	1	800FT	FBA_CLK1
5	OUT FBA_CLK1_TERM	1	400MM	

	NET	NV_CRITICAL_NET	IMPEDANCE
3.5	QUT FSA DQS_WPT7 [G]	1	400M
	IN FSA DQS_WPT7 [G]	1	400M
	QUT FSA DQM7 [G]	1	400M
3.5	IN FSA DQS [G]	1	400M

	NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
3,7	OUT	FIBR_CLK0 1	50OH	FIBR_CLK0
3,7	OUT	FIBR_CLK0 1	50OH	FIBR_CLK0
7	OUT	FIBR_CLK0_TERM 1	ACDM	
	OUT	FIBR_CLK1 1	50OH	FIBR_CLK1
	OUT	FIBR_CLK1_TERM 1	50OH	FIBR_CLK1

	NET	NV_CRITICAL_NET	IMPEDANCE
3.7	OUT	FBS_DQ5_W0F7_0	1
3.7	IN	FBS_DQ5_W0F7_0	1
3.7	OUT	FBS_DQ6F7_0	1
3.7	IN	FBS_DQ6F7_0	1

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141	FB_VREF138	12MIL	1.50V	0.025
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143	FB_VREF140	12MIL	1.50V	0.025
144	FB_VREF141	12MIL	1.50V	0.025
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146	FB_VREF143	12MIL	1.50V	0.025
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	NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
4.0	OUT	FRC_CLK0	1	800T FRC_CLK0
4.0	OUT	FRC_CLK0*	1	800T* FRC_CLK0
9	OUT	FRC_CLK0_TERM	1	800RM
4.0	OUT	FRC_CLK1	1	800T FRC_CLK1
4.0	OUT	FRC_CLK1*	1	800T* FRC_CLK1
9	OUT	FRC_CLK1_TERM	1	800RM

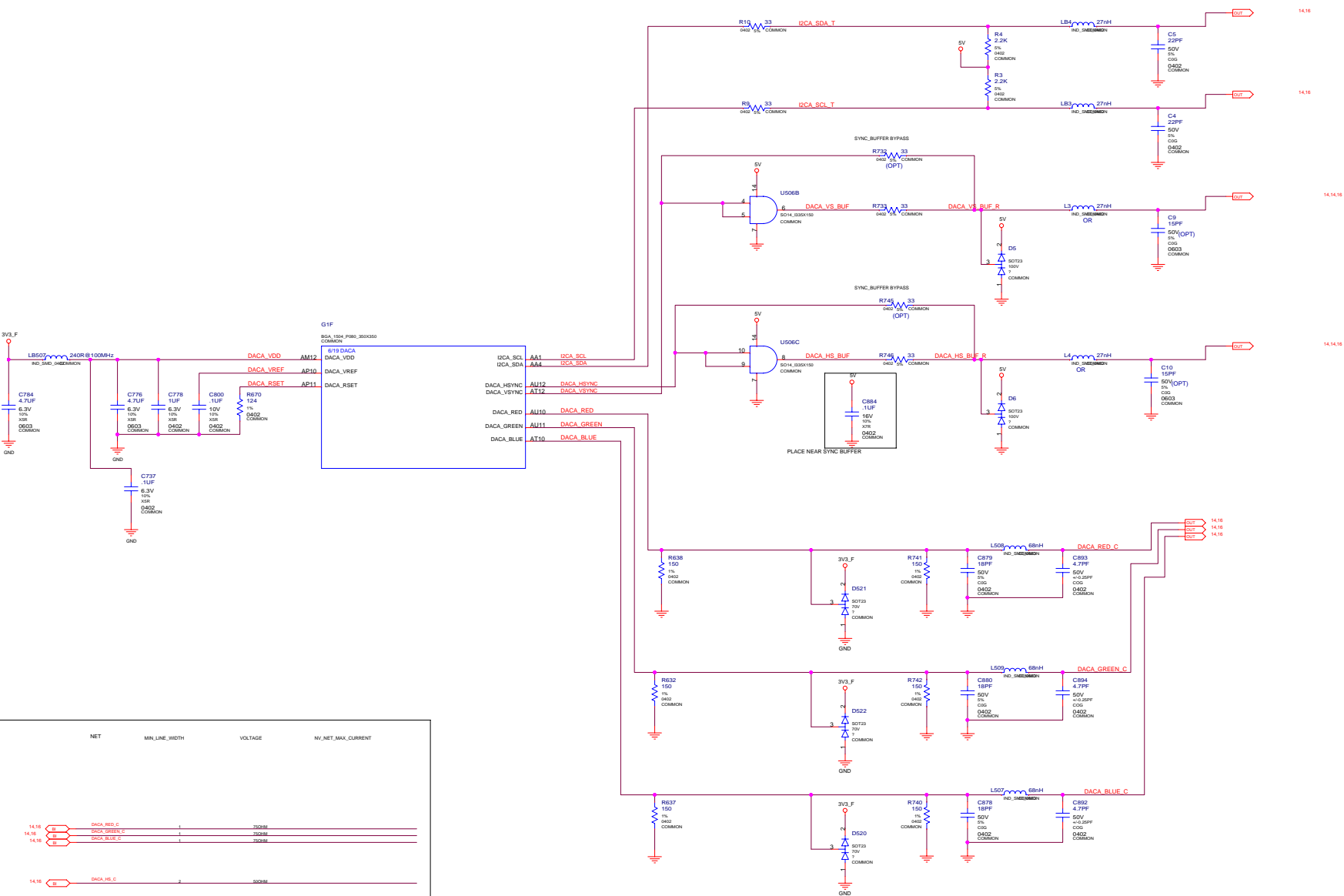
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4.9	Q27	FSC_Q05_WP07_0	1
4.9	IN	FSC_Q05_WP07_0	1
4.9	Q27	FSC_Q06_WP07_0	1
4.9	IN	FSC_Q06_WP07_0	1
4.9	Q27	FSC_Q08_0	1
4.9	IN	FSC_Q08_0	1

	NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
4:11	FBD_CLK0	1	ISDIT	FBD_CLK0
OUT	FBD_CLK0*	1	ISDIT	FBD_CLK0
11	FBD_CLK0_TERM	1	ISDIT	
OUT			ISDIT	
3:7,8	FBD_CLK1	1	ISDIT	FBD_CLK1
OUT	FBD_CLK1*	1	ISDIT	FBD_CLK1
7,8	FBD_CLK1_TERM	1	ISDIT	FBD_CLK1
OUT			ISDIT	

	NET	NV_CRITICAL_NET	IMPEDANCE
4.11	Q27	FSD_Q25_WPY[0]	1
4.11	IN	FSD_Q25_WPY[0]	1
4.11	Q27	FSD_Q26[7:0]	1
4.11	Q	FSD_Q26[7:0]	1

	NET	MIN_LEN_WIDTH	VOLTAGE	NET_NET_MAX_CURRENT
4	FB_PLA10D1	120k	1.5V	0.02A
9	FB_VREF0	120k	1.20V	0.02A
9	FB_VREF1	120k	1.20V	0.02A
9	FB_VREF2	120k	1.20V	0.02A
9	FB_VREF3	120k	1.20V	0.02A
9	FB_Z00	120k	1.20V	0.02A
9	FB_Z01	120k	1.20V	0.02A
11	FB_VREF0	120k	1.20V	0.02A
11	FB_VREF1	120k	1.20V	0.02A
11	FB_VREF2	120k	1.20V	0.02A
11	FB_VREF3	120k	1.20V	0.02A
11	FB_Z00	120k	1.20V	0.02A
11	FB_Z01	120k	1.20V	0.02A

DACA RGB-FILTER



NET	MIN_LINE_WIDTH	VOLTAGE	WIRE_CURRENT
14.16	1	3.3V	300MA
14.16	1	3.3V	300MA
14.16	1	3.3V	300MA
14.16	2	3.3V	300MA
14.16	2	3.3V	300MA

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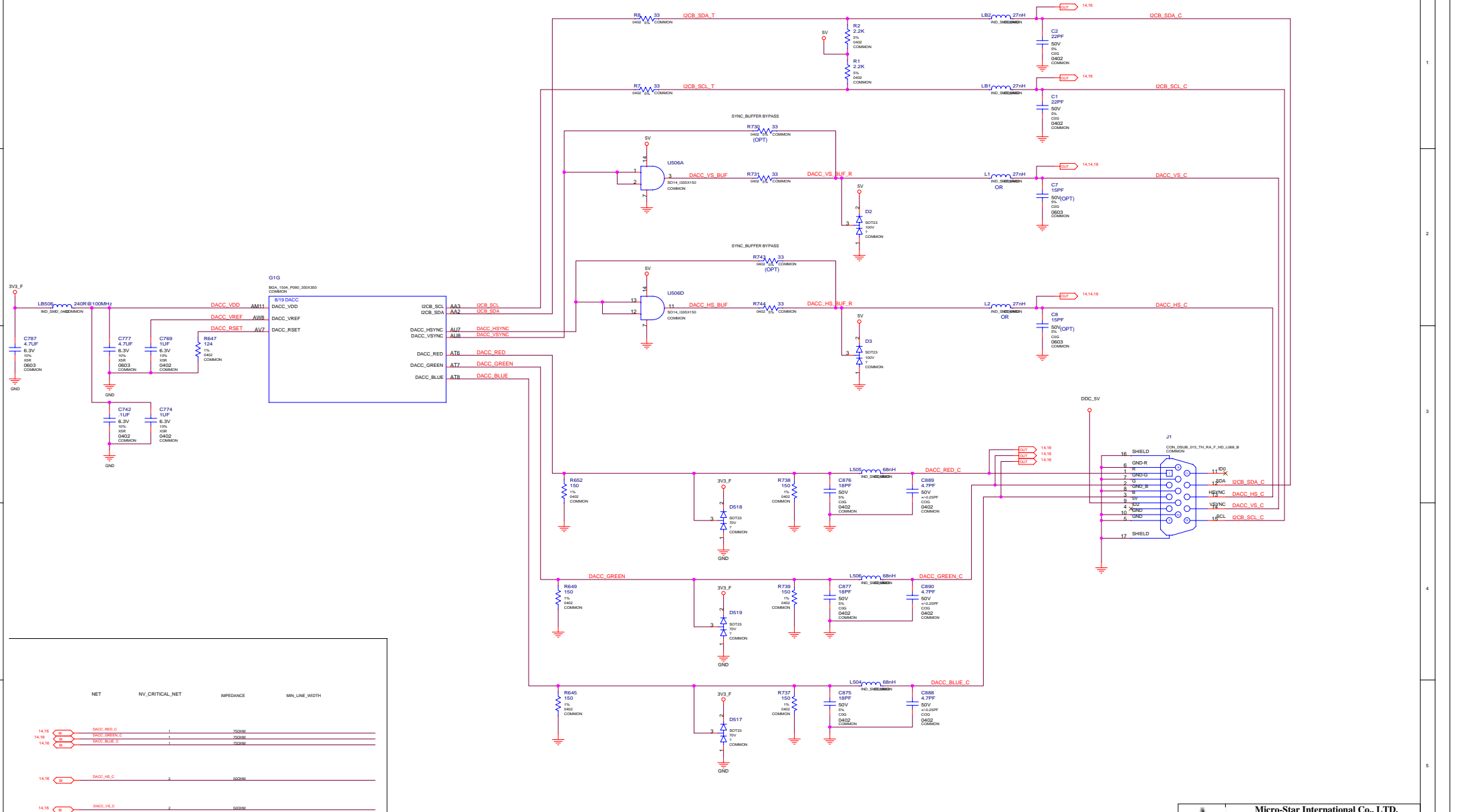
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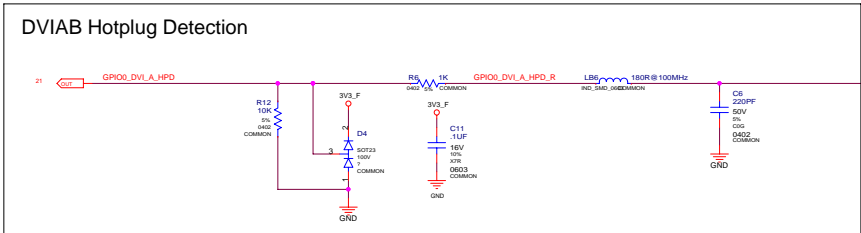
Micro-Star International Co., LTD.


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Date	Thursday, March 08, 2008	Sheet	14	of	32

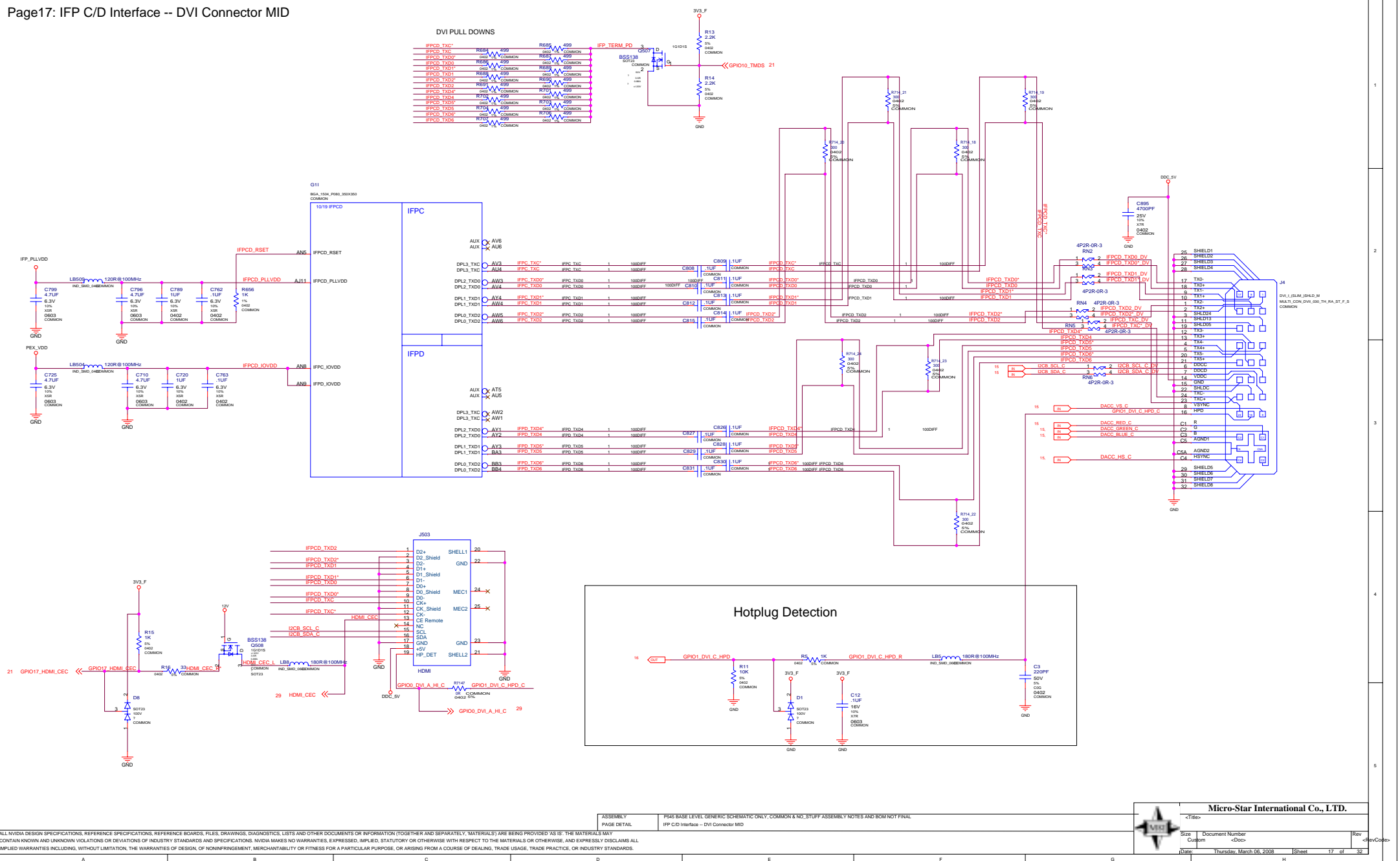
DACC RGB-FILTER



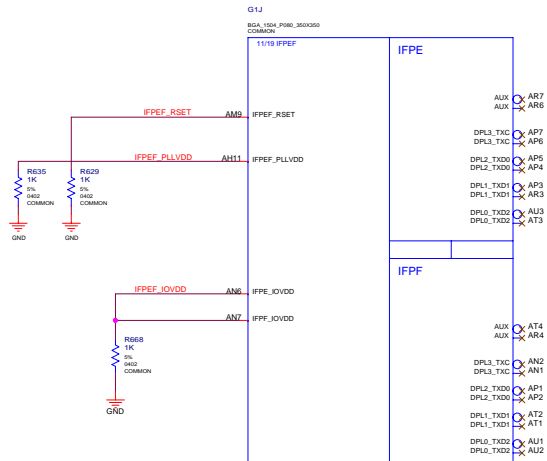
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Page18: IFP E/F Interface -- Unused
TMDS E : Display Port



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IFP E/F Interface -- Unused



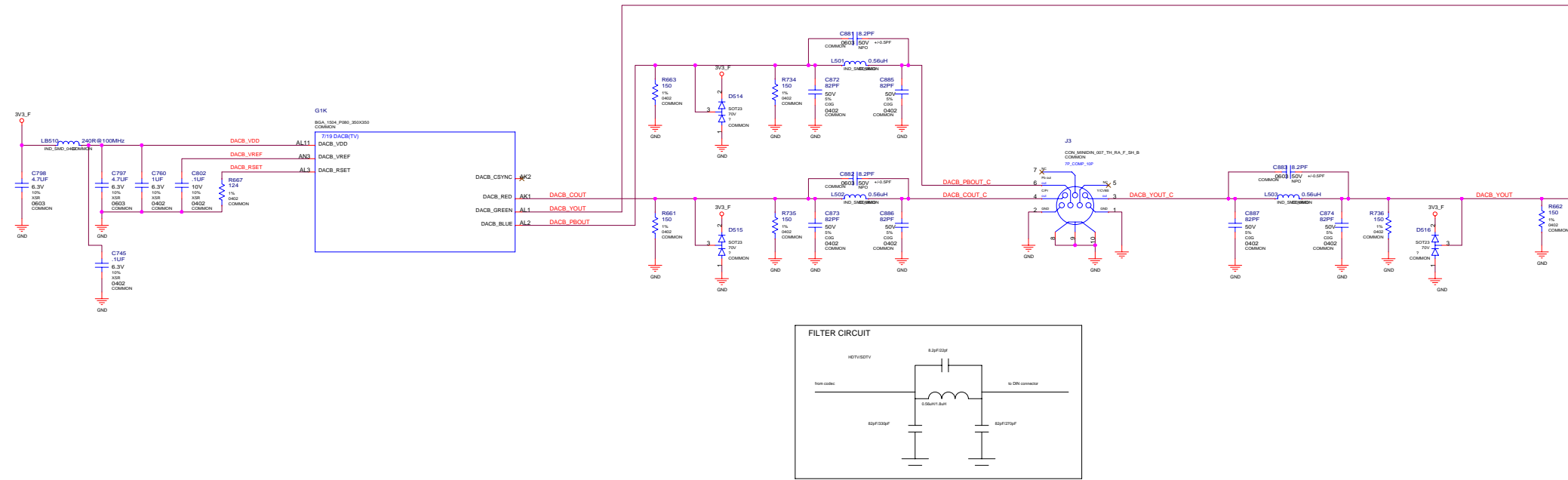
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Date Thursday, March 08, 2008 Sheet 18 of 32

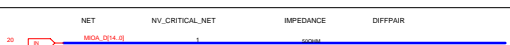
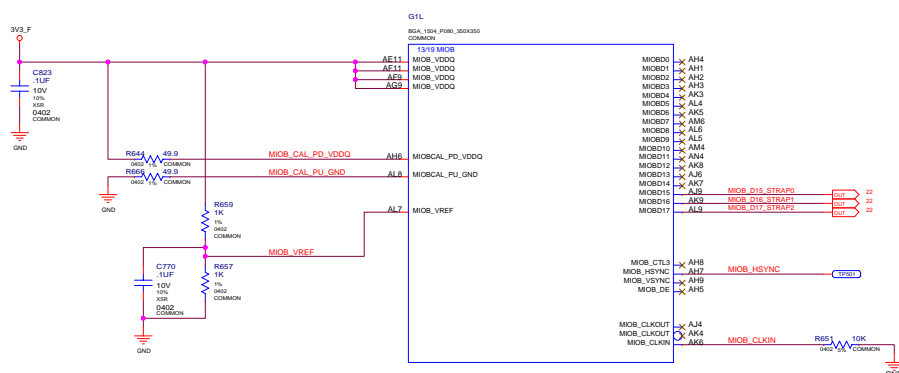
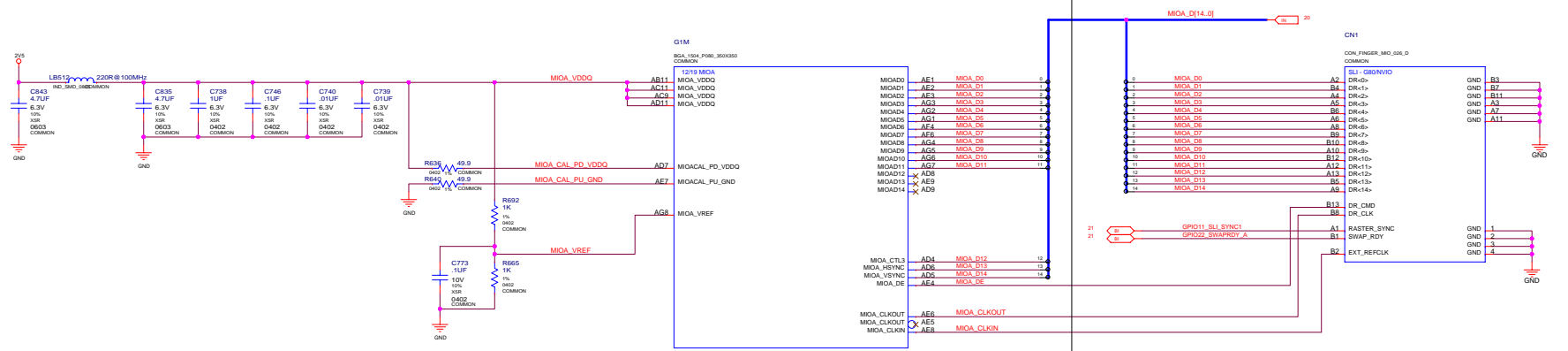
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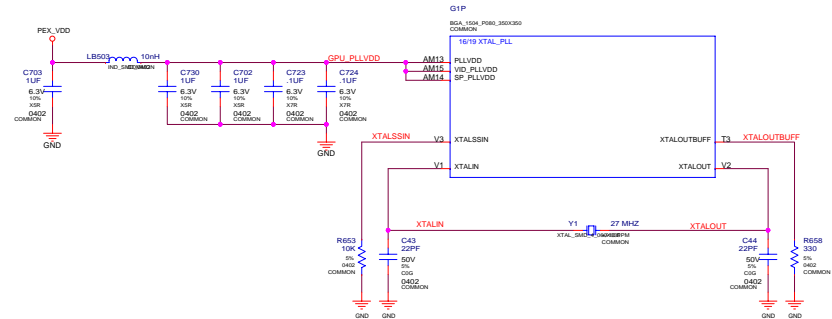
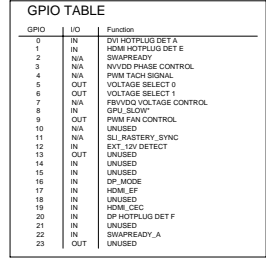


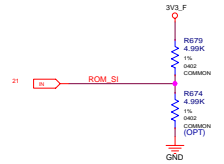
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ASSEMBLY PAGE DETAIL
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DACB and HDTV/SDTV-Out

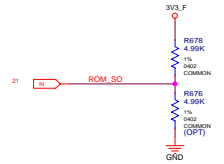
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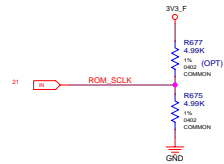




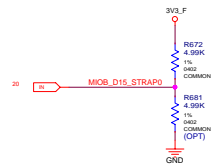
STRAP PIN	STRAP NAME
ROM_SI	PCI_DEVID_EXT



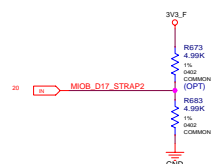
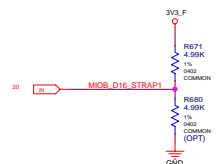
STRAP PIN	STRAP NAME
ROM_SO	SLOT_CLK_CFG



STRAP PIN	STRAP NAME
ROM_SCLK	PCI_DEVID[3]

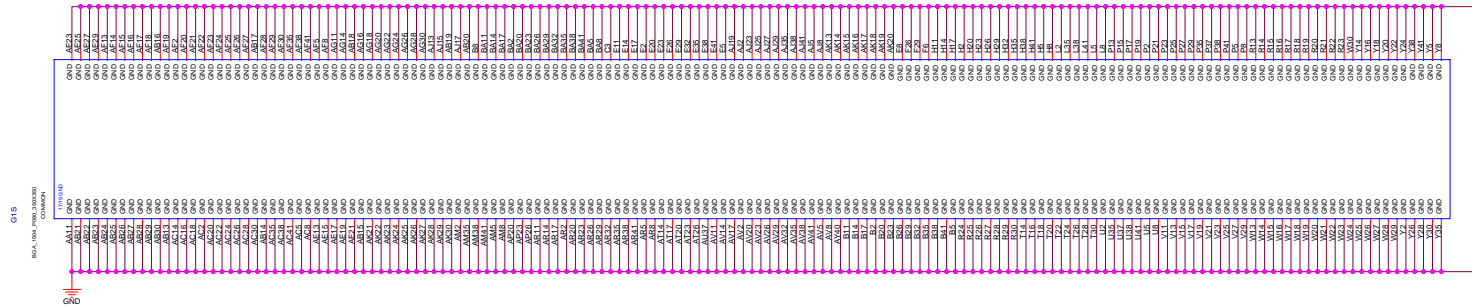


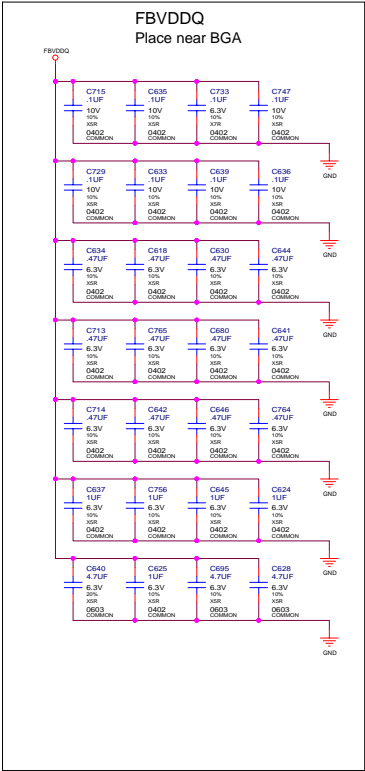
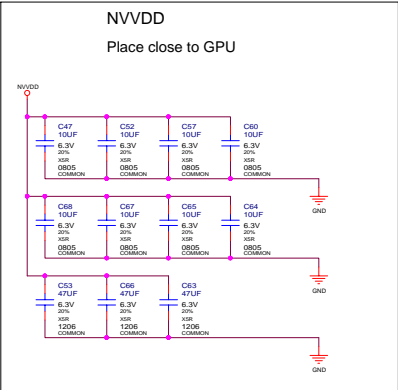
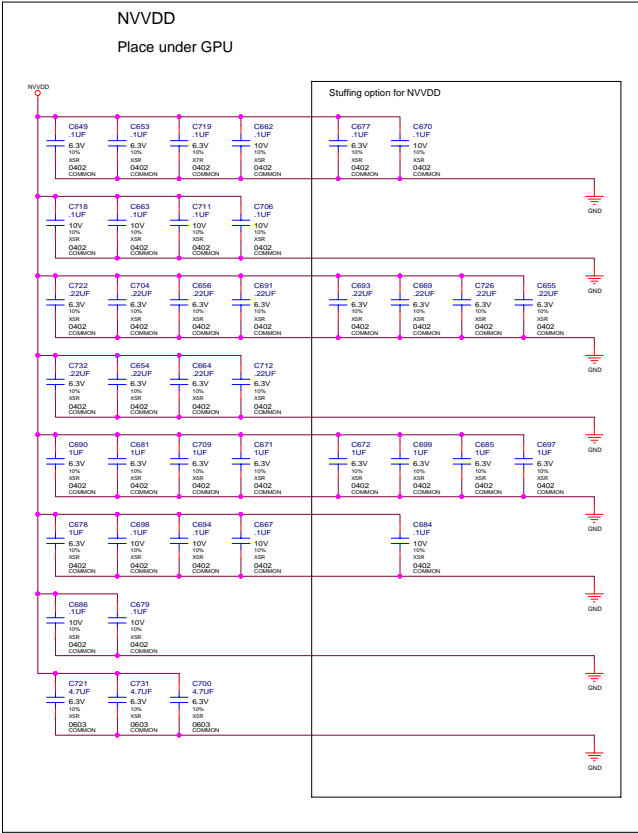
STRAP PIN	STRAP NAME			
STRAP0	RAMCFG0			
		* RAMCFG[2:0]		
		256MB (8Mx32)	512MB (16Mx32)	1024MB (32Mx32)
		101 --- 256-bit Qimonda 110 --- 256-bit Hynix 111 --- 256-bit Samsung	001 --- 256-bit Qimonda 010 --- 256-bit Hynix 011 --- 256-bit Samsung	101 --- 256-bit Hynix 110 --- 256-bit Hynix 111 --- 256-bit Samsung
		* VBIOS will be defined on a per SKU basis.		
STRAP PIN	STRAP NAME			
STRAP2	RAMCFG2			



3V3		GND	
5K		1	0

COMMON	
ACM4	NC
AC82	NC
AC83	NC
AC85	NC
AF56	NC
AF57	NC
AF58	NC
AG25	NC
AG26	NC
AM46	NC
AKC4	NC
AL32	NC
AL33	NC
AM59	NC
AM60	NC
AM53	NC
AM55	NC
AM6	NC
AP56	NC
AP58	NC
AT15	NC
AT17	NC
AT18	NC
AU12	NC
ALU8	NC
ALU9	NC
AV12	NC
AV18	NC
AV55	NC
E10	NC
E16	NC
F16	NC
F18	NC
F19	NC
G12	NC
G13	NC
G15	NC
G16	NC
G17	NC
H2	NC
H3	NC
J26	NC
J27	NC
J28	NC
L16	NC
L17	NC
L18	NC
L19	NC
M12	NC
M13	NC
P16	NC
P18	NC
R16	NC
R18	NC
TS1	NC
US1	NC
US2	NC
Y16	NC
Y18	NC
Y19	NC





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ASSEMBLY PAGE DETAIL
PS4 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO.31UFF ASSEMBLY NOTES AND BOM NOT FINAL
NVVDD and FBVDDQ Decoupling



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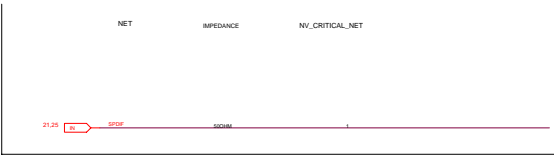
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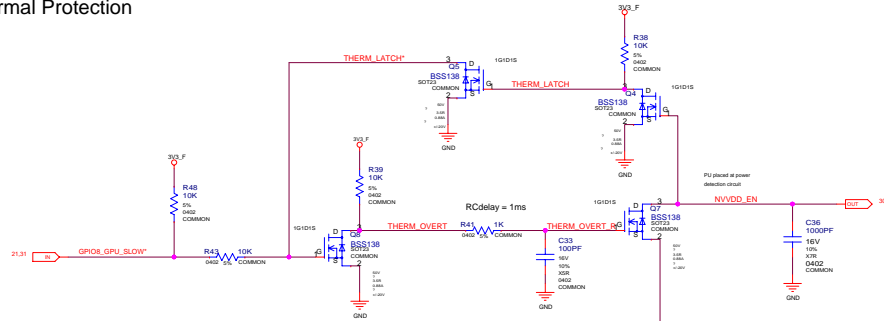
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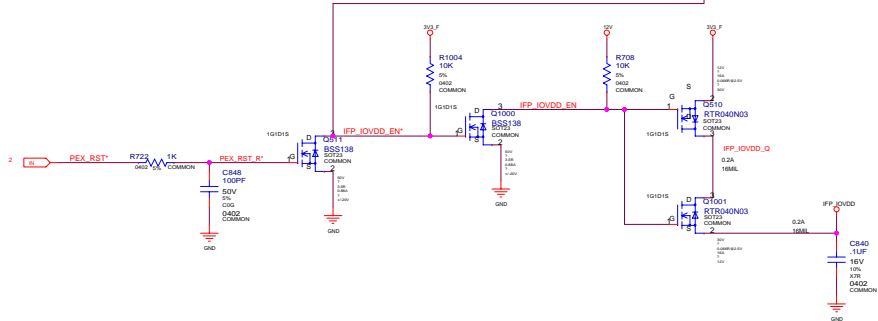


Thermal Protection

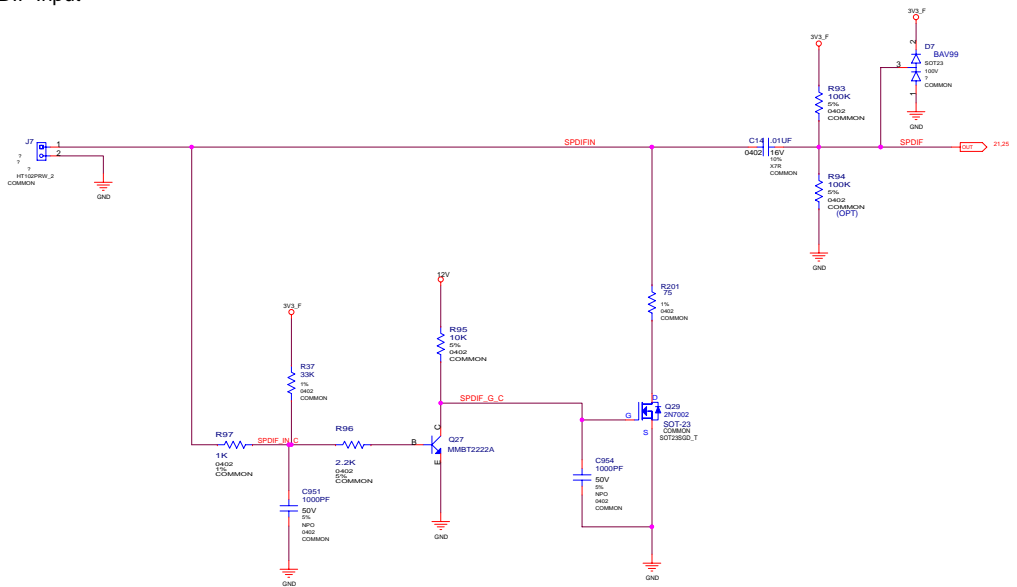


IFP_IOVDD Backdrive Prevention

Stuffing possibilities for thermal control and protection:

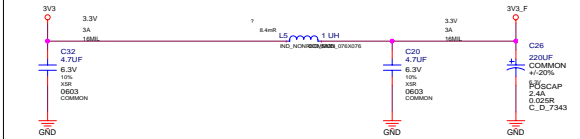


SPDIF Input



3V3 Power Supply Filter

3V3_F = 3.3V @ 2.5A



12V Power Supply Filter

12V_F = 12V @ 5.5A

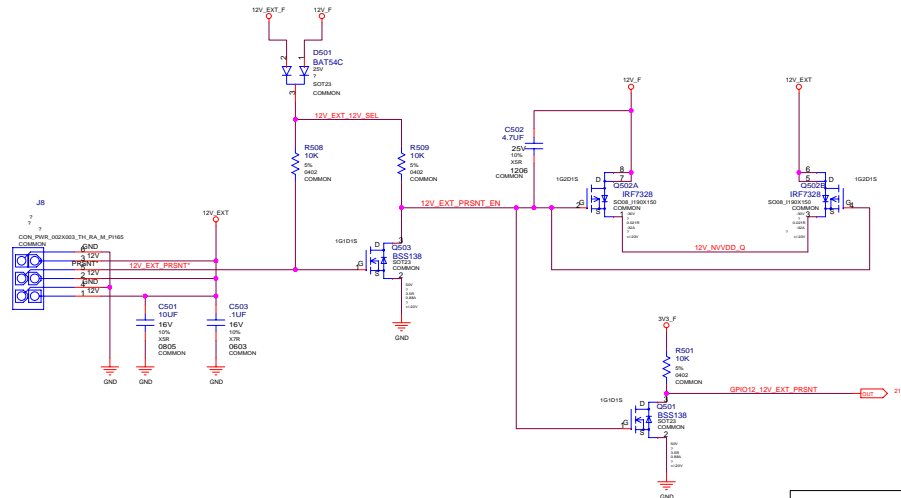


12V_EXT Power Supply Filter

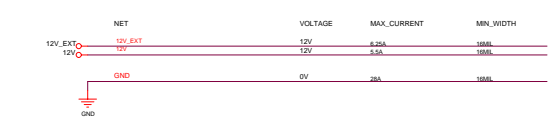
12V_EXT_F = 12V @ 6.25A

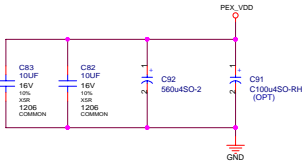


INPUT POWER SELECTION for NVVDD



GPIO12	
EMERGENCY MODE (12V_EXT present)	0
150W POWER MODE (12V_EXT NOT present)	1

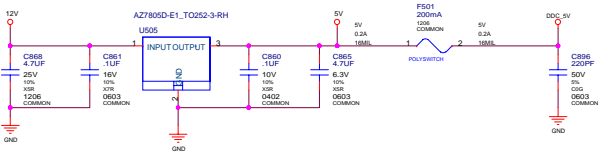




5V and DDC_5V Power Supply

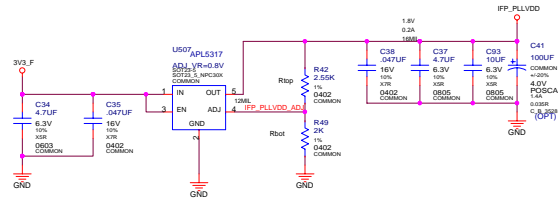
DDC_5V = 5V @ 200mA

LAYOUT NOTE: ADD MIN 200MM² COPPER AROUND THE DPAK FOR HEAT DISSIPATION



IFF_PLLVDD Power Supply

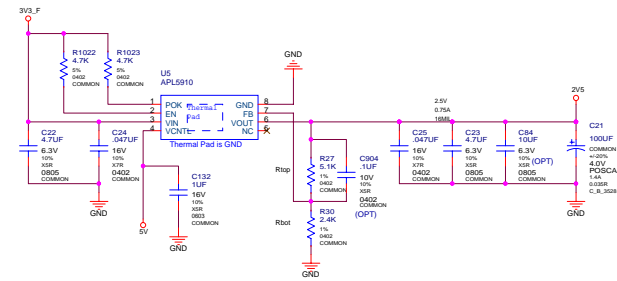
IFF_PLLVDD = 1.8V @ 200mA



$$IFF_PLLVDD = VREF * (1 + (Rtop / Rbot))$$
$$1.82V = 0.8V * (1 + (2.5K/2K))$$

2V5 Power Supply

2V5 = 2.5V @ 750mA



$$2V5 = VREF * (1 + (Rtop / Rbot))$$
$$2.5V = 0.8V * (1 + (5.1K/2.4K))$$

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ASSEMBLY PAGE DETAIL PSII BASE LEVEL GEN/RC SCHEMATIC ONLY; COMMON & NC SUFF ASSEMBLY NOTES AND BCM NOT FINAL PS II: PEX_VDD, IFF_PLLVDD, 2V5, 5V, and DDC_5V Power Supply



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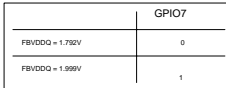
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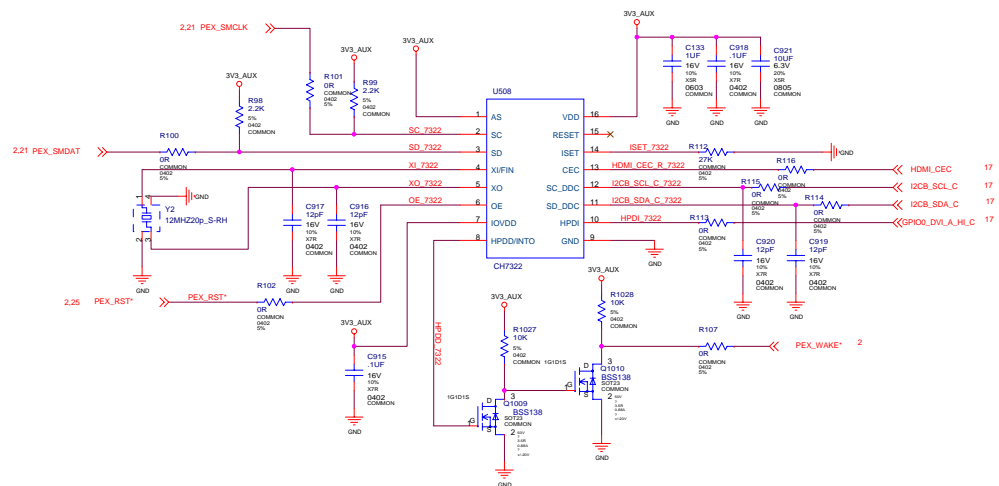
Date Thursday, March 08, 2008 Sheet 27 of 32

Rev

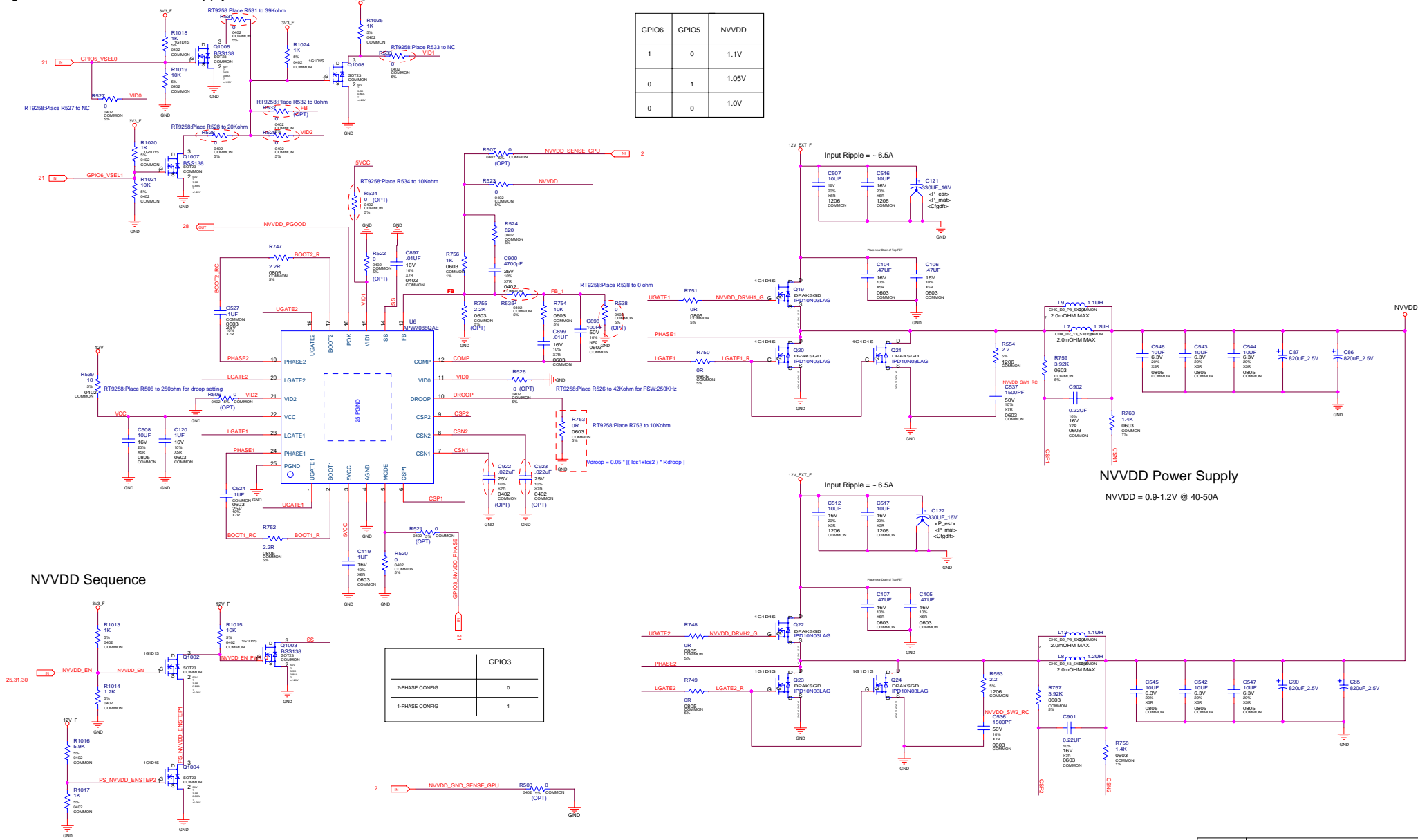
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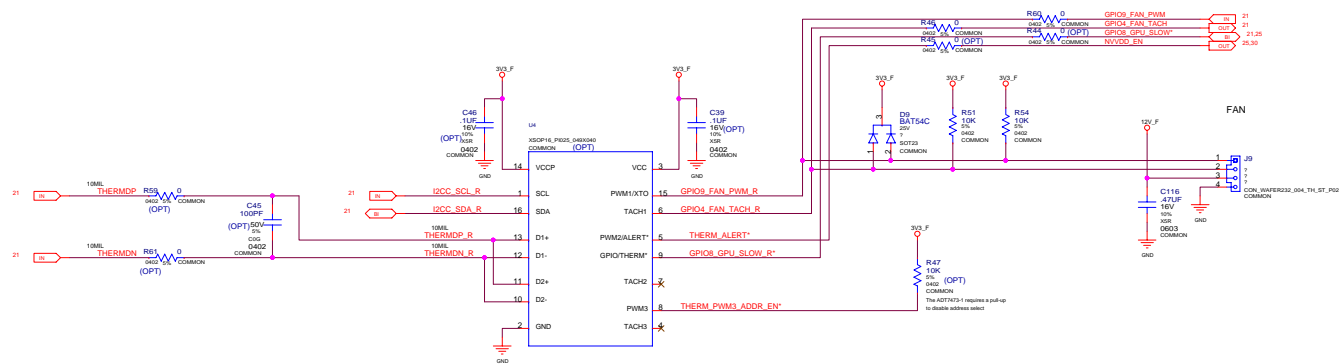
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	Date Thursday, March 06, 2008	Sheet 28 of 28	Page 28



NVDD Voltage Select											
NVDD range 0.80V-1.40V											
Register: ADDR08											
Control via NV_GPIOs NV_VSEL[1:0]											
VDD					NVDD						
6	5	4	3	10	Vout					G94	
0	1	1	0	0	0.80V					=> Default => Voltage1 => Voltage2	
0	1	1	0	1	0.85V						
0	1	1	0	0	0.90V						
0	1	1	0	1	0.95V						
0	1	1	1	0	1.00V						
0	1	1	1	1	1.05V						
0	1	0	0	0	1.10V						
0	1	0	1	1	1.15V						
0	0	1	0	0	1.20V						
0	0	1	0	1	1.25V						
0	0	1	0	0	1.30V						
0	0	1	1	1	1.35V						
0	0	1	1	0	1.40V						



ADT7473 External Fan/Thermal Control



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PAGE DETAIL	Thermal Diode and Fan Control



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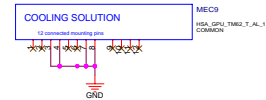
Sheet 31 of 3

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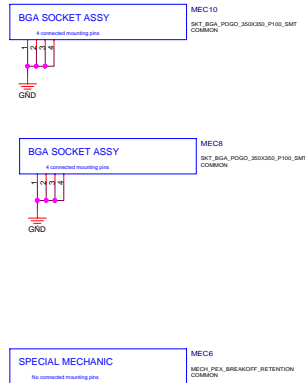
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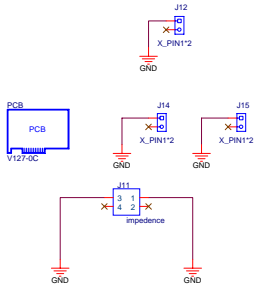
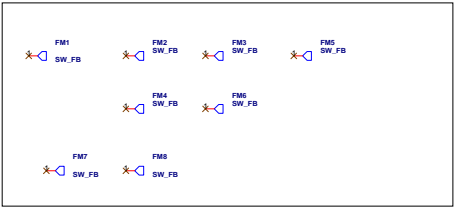
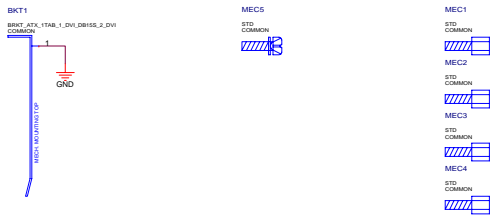
Thermal



Mechanical



Bracket



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