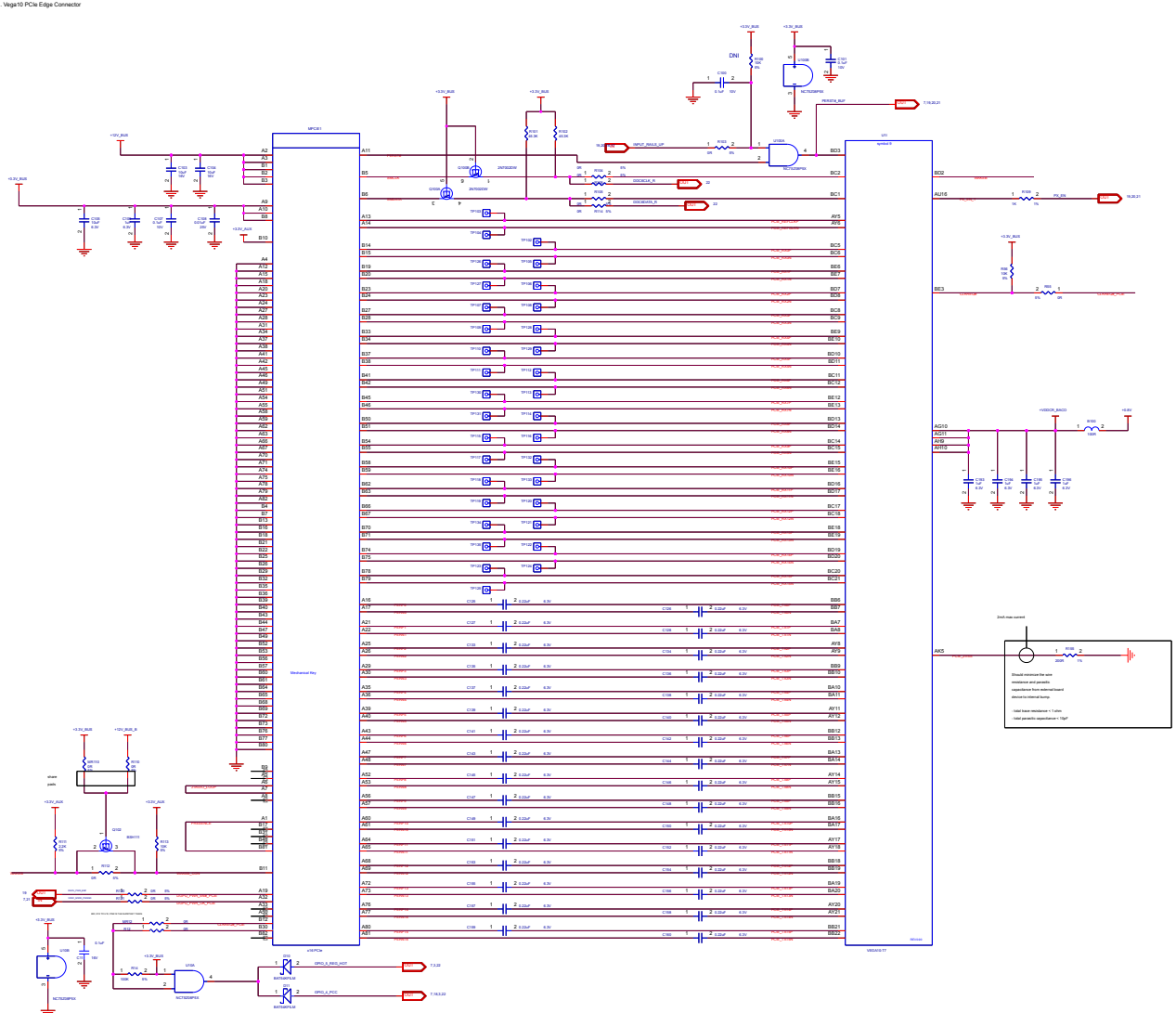

TABLE OF CONTENTS

SHEET NO.	SHEET NAME
1	Vega10 - PCIe Interface
2	Vega10 - Power / GND
3	Vega10 - GPIO, EXTRA
4	Vega10 - DFTIO, FREE, HPM_DAP, CRACKMON
5	Vega10 - TMDPAB 1xDP, 1xHDMI & +5V VESA
6	Vega10 - TMDPEF 2xDP
7	Control - VDDC / MVDD
8	Reg - VDDCR_SOC PHASES I and VII
9	Reg - VDDCR_SOC PHASES V and XI
10	Reg - VDDCR_SOC PHASES III and IX
11	Reg - VDDCR_SOC PHASES IV and X
12	Reg - VDDCR_SOC PHASES II and VIII
13	Reg - VDDCR_SOC PHASES VI and XII
14	Reg - VDDCR_IO
15	Reg - VDDCR_MEM and VPP
16	Reg - 0V8
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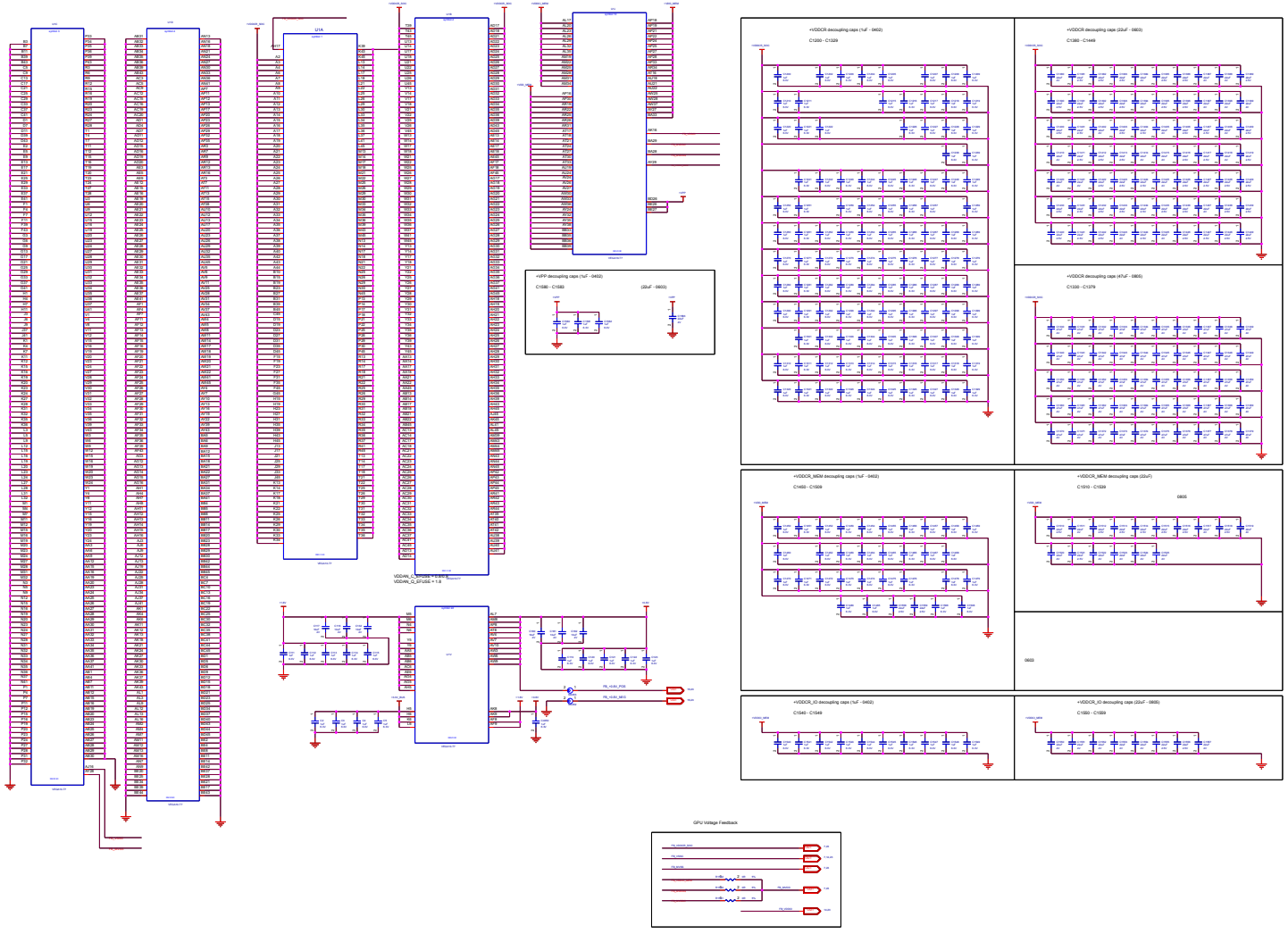
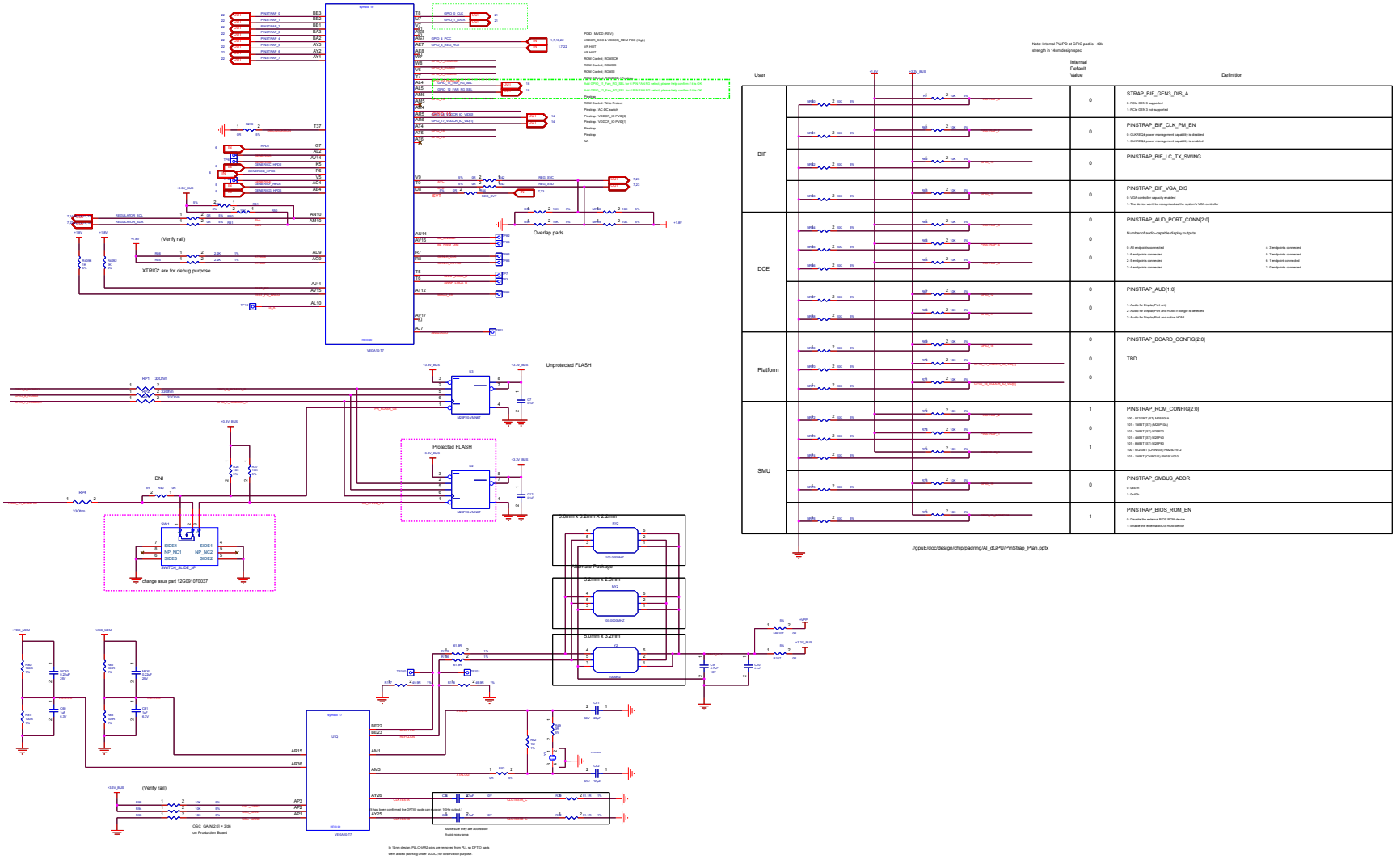
18	FCC - VDDC
19	POWER MANAGEMENT
20	THERMAL
21	GPUTACH & BACO LEDs
22	DEBUG
23	PI GLUE
24	BLOCK DIAGRAM
25	REVISION HISTORY


U21A
+VDDCR_SOC
+VDDCR_GFX
+VPP decoupling caps (1uF - 0402)
C1580 - C1583
(22uF - 0603)
+VDDCR decoupling caps (1uF - 0402)
C1200 - C1329
+VDDCR decoupling caps (22uF - 0603)
C1360 - C1449
+VDDCR decoupling caps (47uF - 0805)
C1330 - C1379
+VDDCR_MEM decoupling caps (1uF - 0402)
C1450 - C1509
+VDDCR_MEM decoupling caps (22uF)
C1510 - C1529
0805
0603
+VDDCR_IO decoupling caps (1uF - 0402)
C1540 - C1549
+VDDCR_IO decoupling caps (22uF - 0805)
C1550 - C1559
VDDAN_CT_SFUSE = 1.8
VDDMN_CL_SFUSE = 1.8
GPU Voltage Feedback

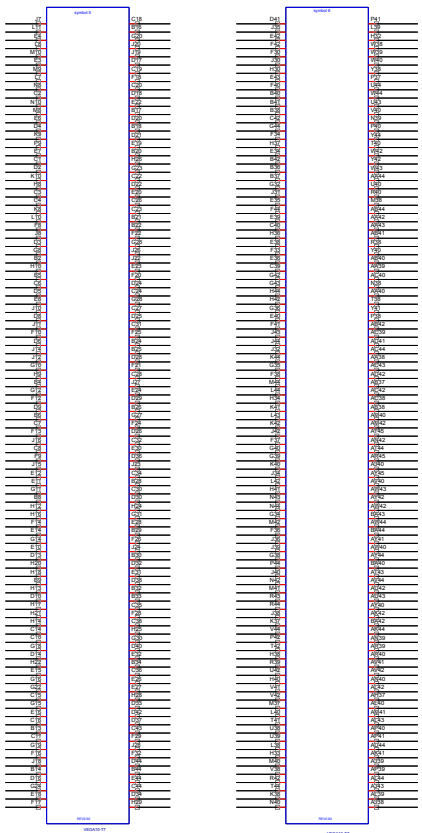


Note: Internal PU/PD at GPIO pad is ~40k
strength in 14nm design spec

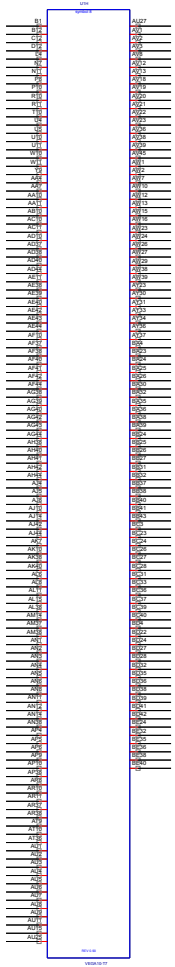
User		Internal Default Value	Definition
BIF		0	STRAP_BIF_GEN3_DIS_A 0: PCIe GEN3 supported 1: PCIe GEN3 not supported
		0	PINSTRAP_BIF_CLK_PM_EN 0: CLKPMG4 power management capability is disabled 1: CLKPMG4 power management capability is enabled
		0	PINSTRAP_BIF_LC_TX_SWING
		0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognized as the system's VGA controller
DCE		0 0 0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected
		0 0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for DisplayPort and native HDMI
Platform		0 0 0	PINSTRAP_BOARD_CONFIG[2:0] TBD
SMU		1 0 1	PINSTRAP_ROM_CONFIG[2:0] 100 : 512KBIT (ST) M25P05A 101 : 1MBIT (ST) M25P10A 110 : 2MBIT (ST) M25P20 101 : 4MBIT (ST) M25P40 111 : 8MBIT (ST) M25P80 100 : 512KBIT (CHINGIS) PM25LV512 101 : 1MBIT (CHINGIS) PM25LV010
		0	PINSTRAP_SMBUS_ADDR 0: 0x97h 1: 0xd0h
		1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device

//gpuEi/doc/design/chip/padring/AI_dGPU/PinStrap_Plan.pptx

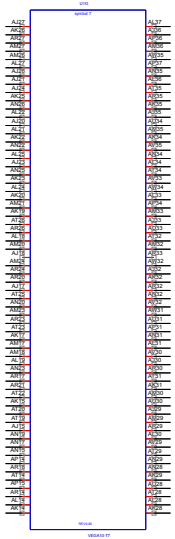
DFTIO



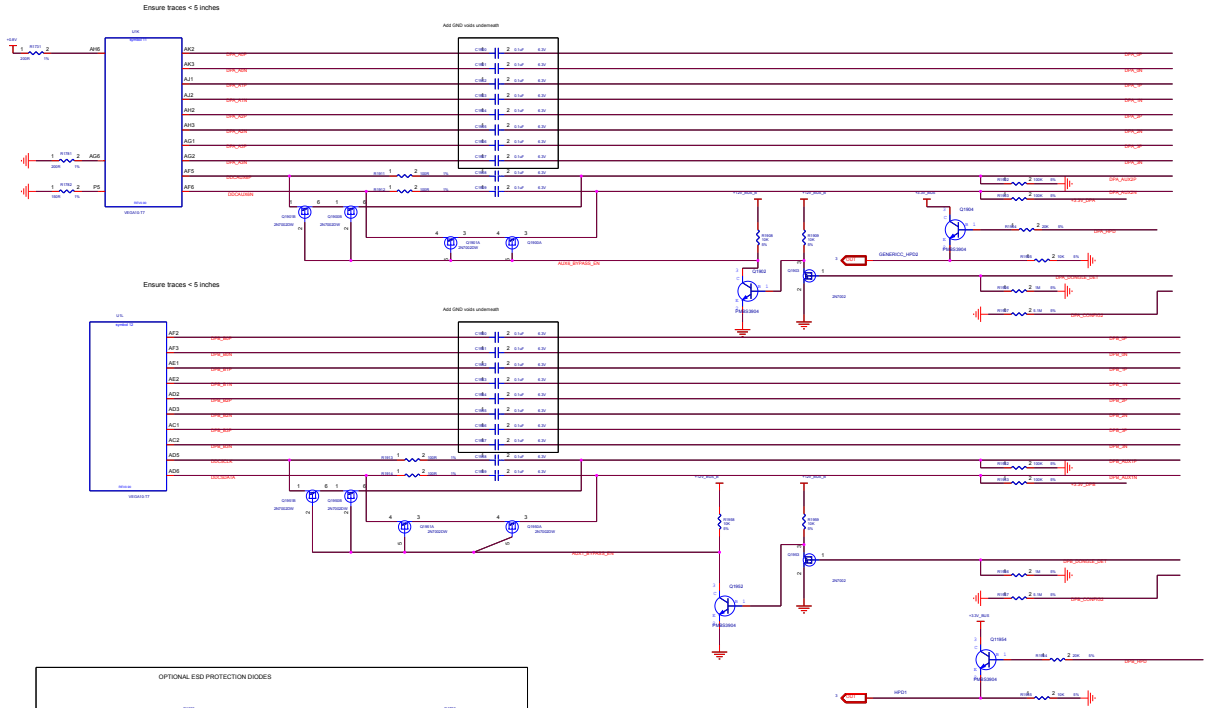
FREE

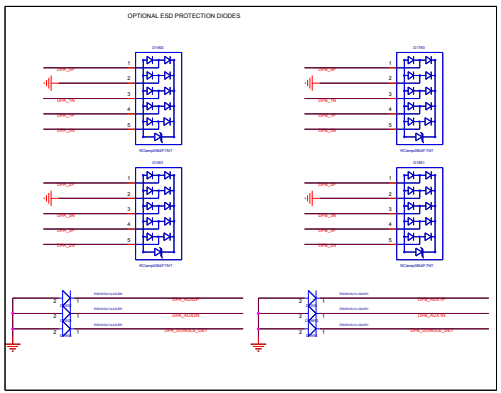


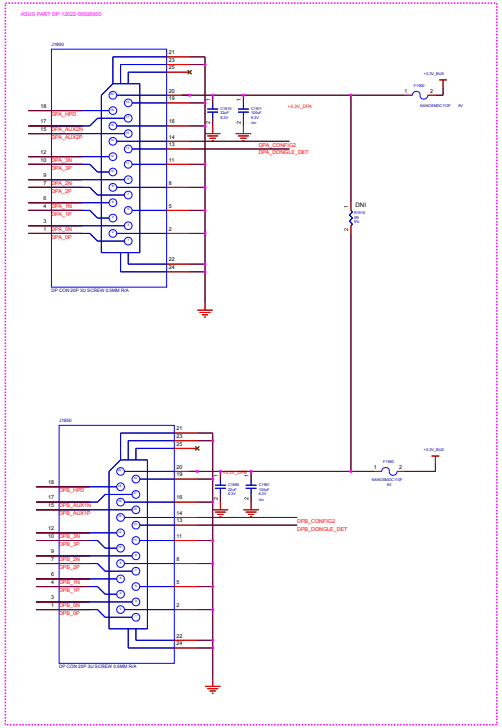
HBM_DAP



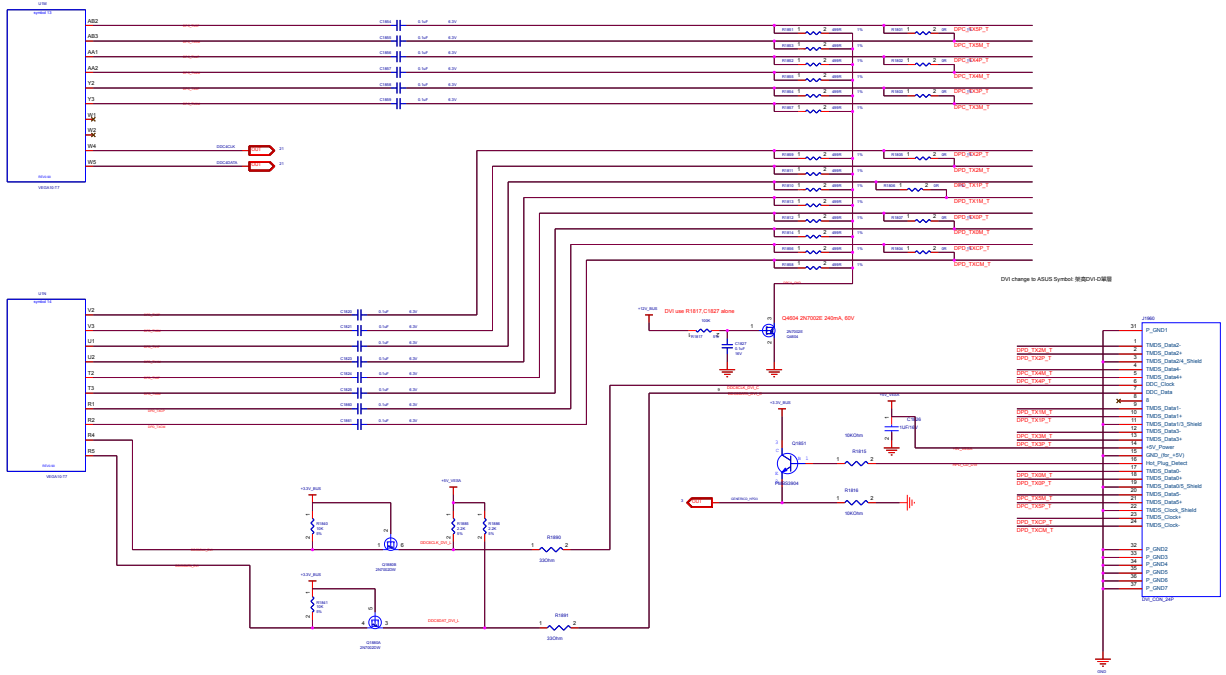
CRACKMON


Ensure traces < 5 inches
Add GND voids underneath
Ensure traces < 5 inches
Add GND voids underneath

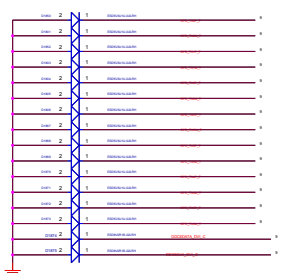

OPTIONAL ESD PROTECTION DIODES


ASUS PART DP-12022-000295600
DP CON 20P 3U SCREW 0.5MM R/A
DP CON 20P 3U SCREW 0.5MM R/A

(9) ELLESMERE TMDPAB dDVI



OPTIONAL ESD PROTECTION DIODES



Ensure traces < 5 inches MAX (if routed on same layer)

For differential routing on HDMI 2.0 connection, use dogbone shape antipads for the transitional vias of the same differential pair, and the distance from the via edge to the shape boundary should be

Add GND voids underneath

Void Covering Pad and body

for EMI

change asus part HDMI - 12G24110194

SJ1700

Ensure traces < 5 inches

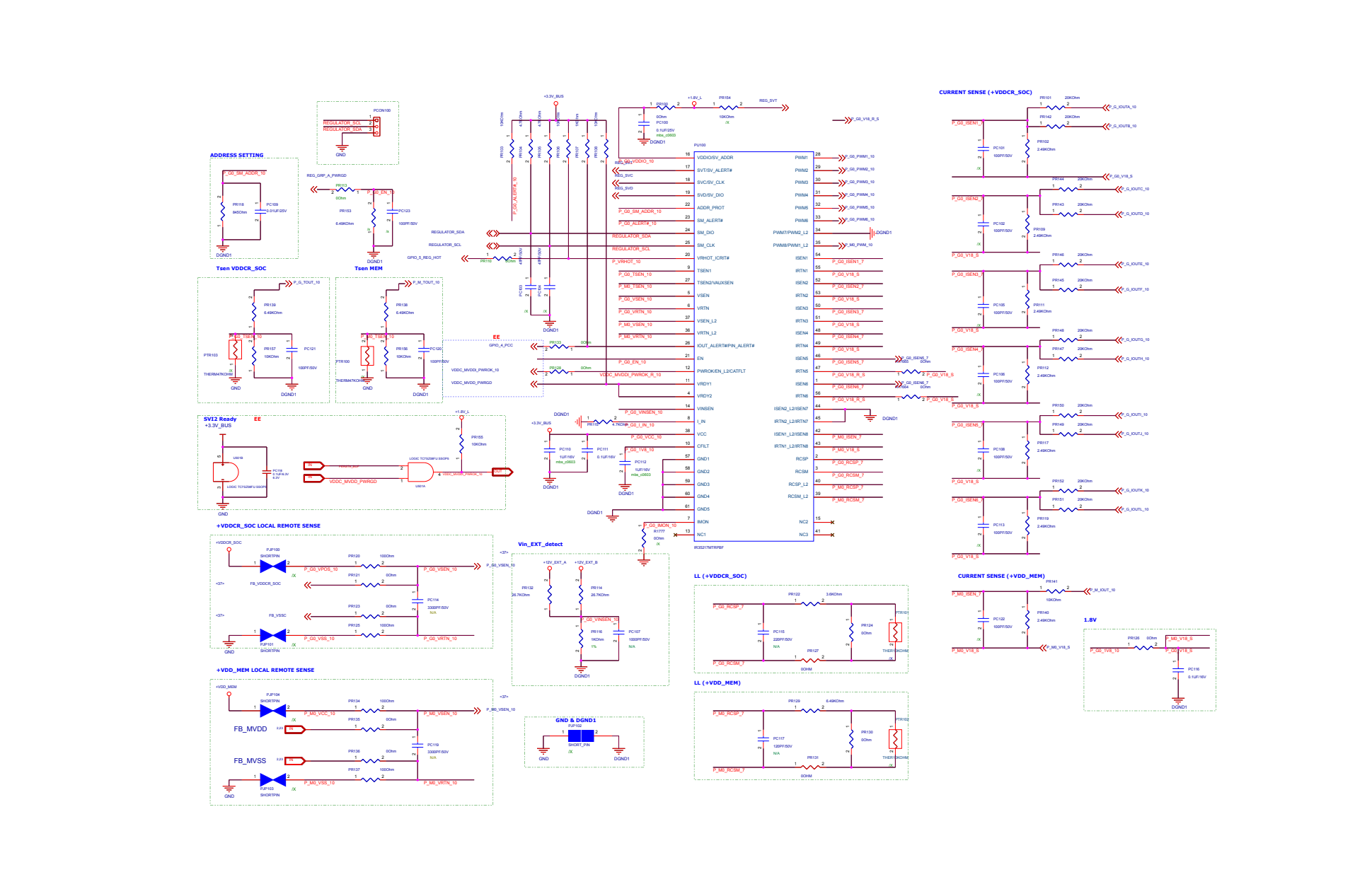
Add GND voids underneath

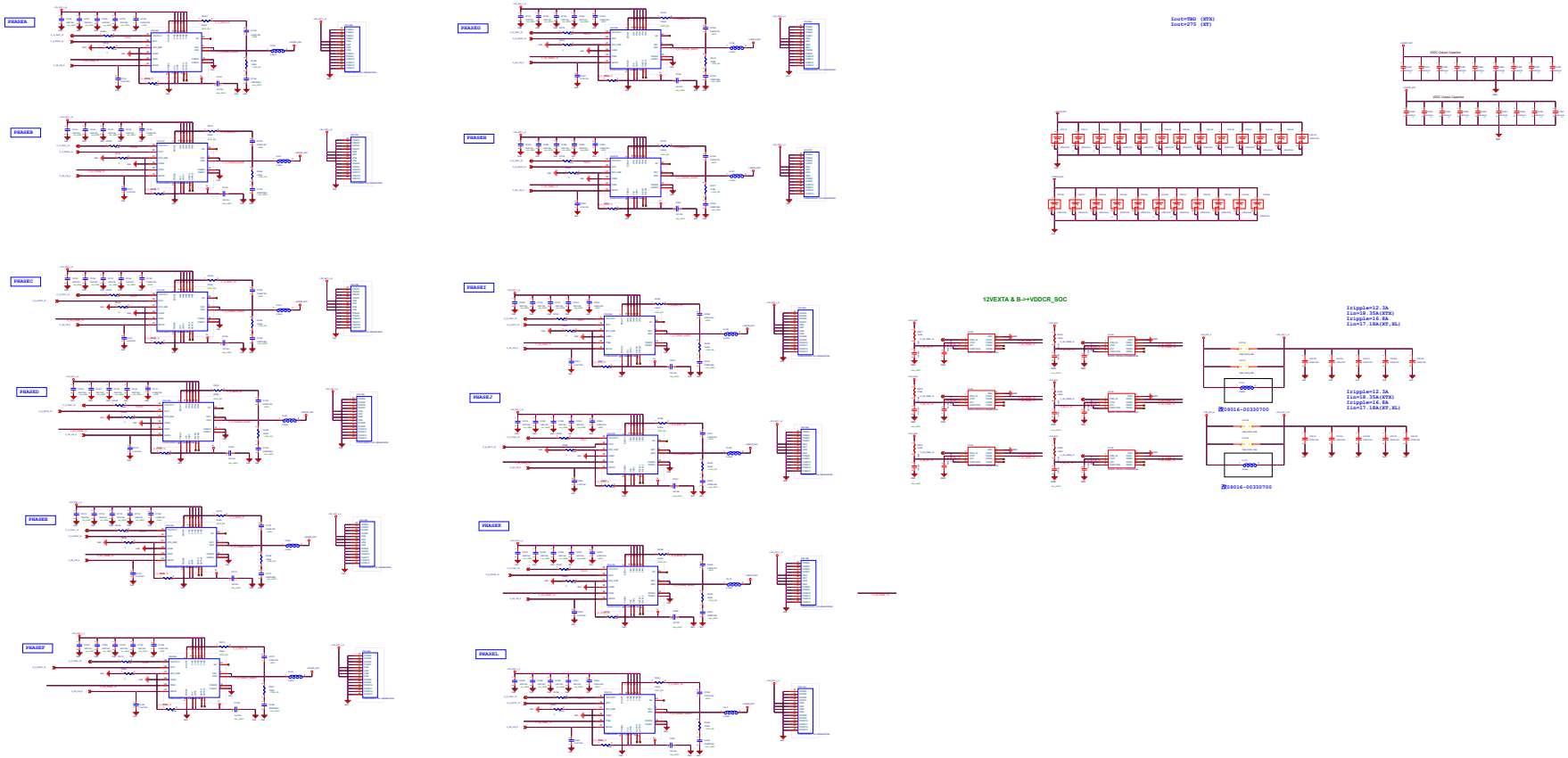
for EMI

SJ1700

OPTIONAL ESD PROTECTION DIODES

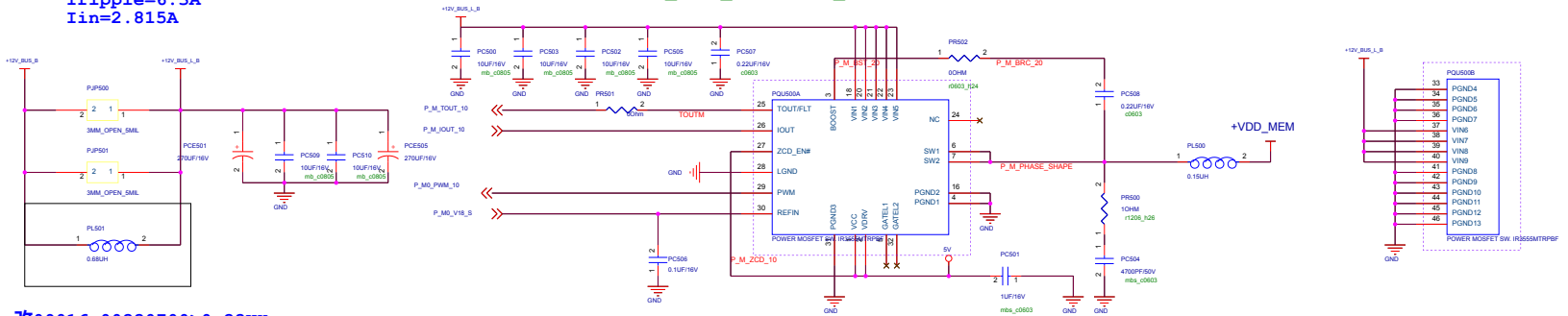
OPTIONAL ESD PROTECTION DIODES


ADDRESS SETTING
Tsen VDDCR_SOC
Tsen MEM
EE
SV12 Ready
+3.3V_BUS
+VDDCR_SOC LOCAL REMOTE SENSE
+VDD_MEM LOCAL REMOTE SENSE
Vin_EXT_detect
GND & DGND1
LL (+VDDCR_SOC)
LL (+VDD_MEM)
CURRENT SENSE (+VDDCR_SOC)
CURRENT SENSE (+VDD_MEM)
1.8V
PU100
IR35217MTRPBF
FB_MVDD
FB_MVSS
FB_VDDCR_SOC
FB_VSSC


PHASEA
PHASEB
PHASEC
PHASED
PHASEE
PHASEF
PHASE0
PHASE7
PHASE8
PHASE9
Iout=TBD (STX)
Iout=27S (XT)
12VEXTA & B->+VDDCR_SOC
Iripple=12.3A
Iin=18.35A(STX)
Iripple=16.8A
Iin=17.18A(XT,XL)
Iripple=12.3A
Iin=18.35A(STX)
Iripple=16.8A
Iin=17.18A(XT,XL)
109016-00330700
109016-00330700

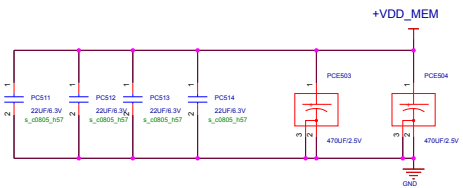
Iripple=6.3A
Iin=2.815A

+12V_BUS_B -> +VDD_MEM



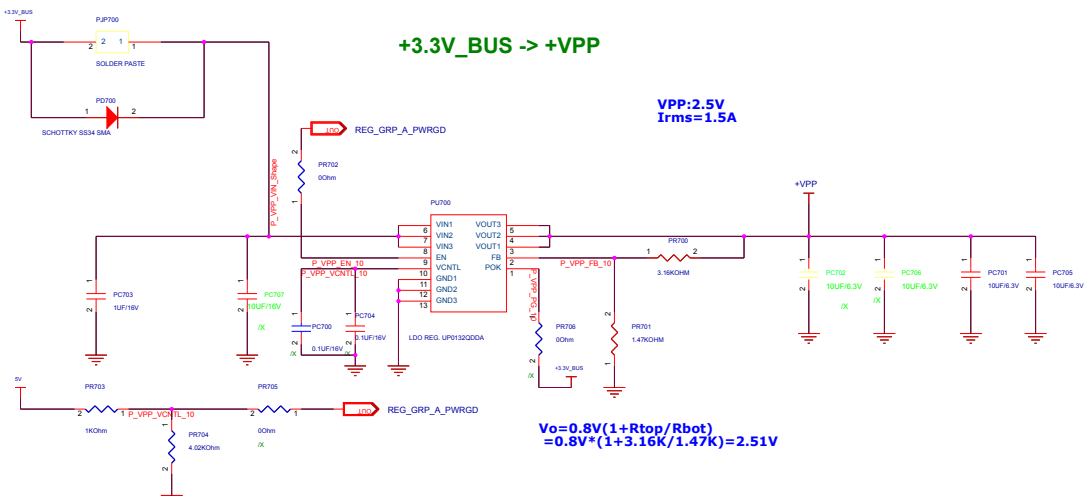
改09016-00330700>0.33UH

+VDD_MEM:1.35V
Iout=20A



+3.3V_BUS -> +VPP

VPP:2.5V
Irms=1.5A

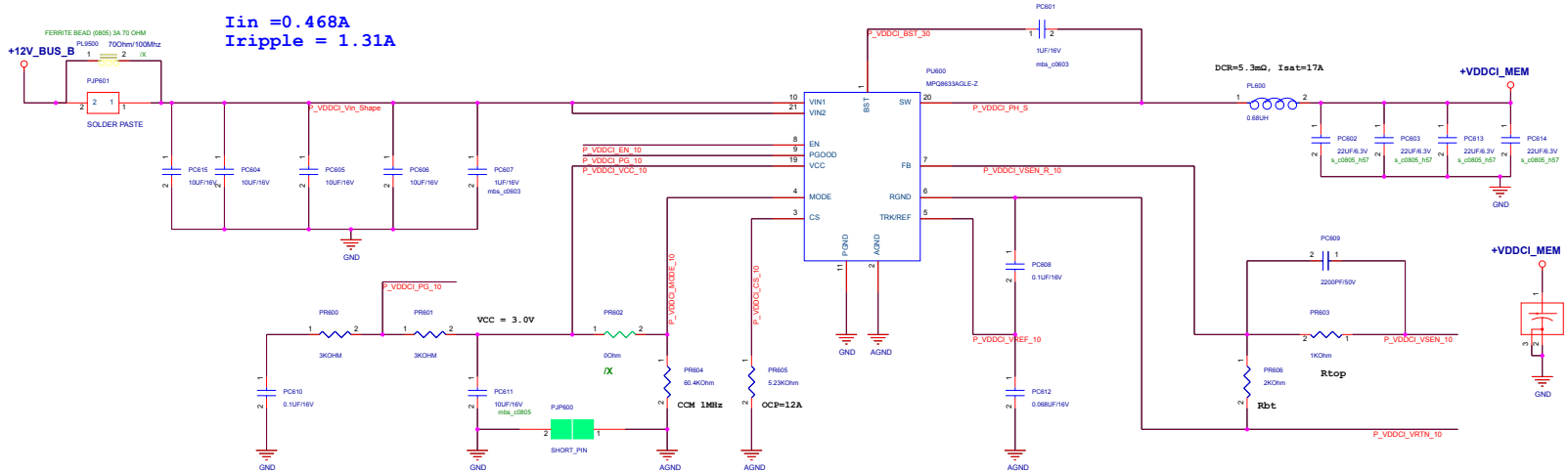


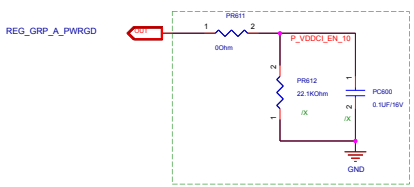
Vo=0.8V(1+Rtop/Rbot)
=0.8V*(1+3.16K/1.47K)=2.51V

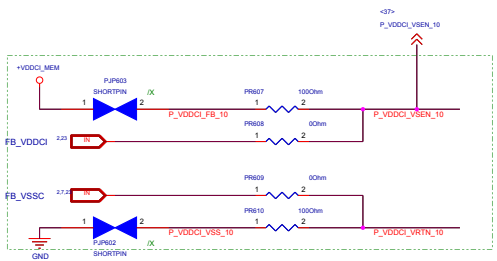
+12V_BUS_B -> +VDDCI_MEM

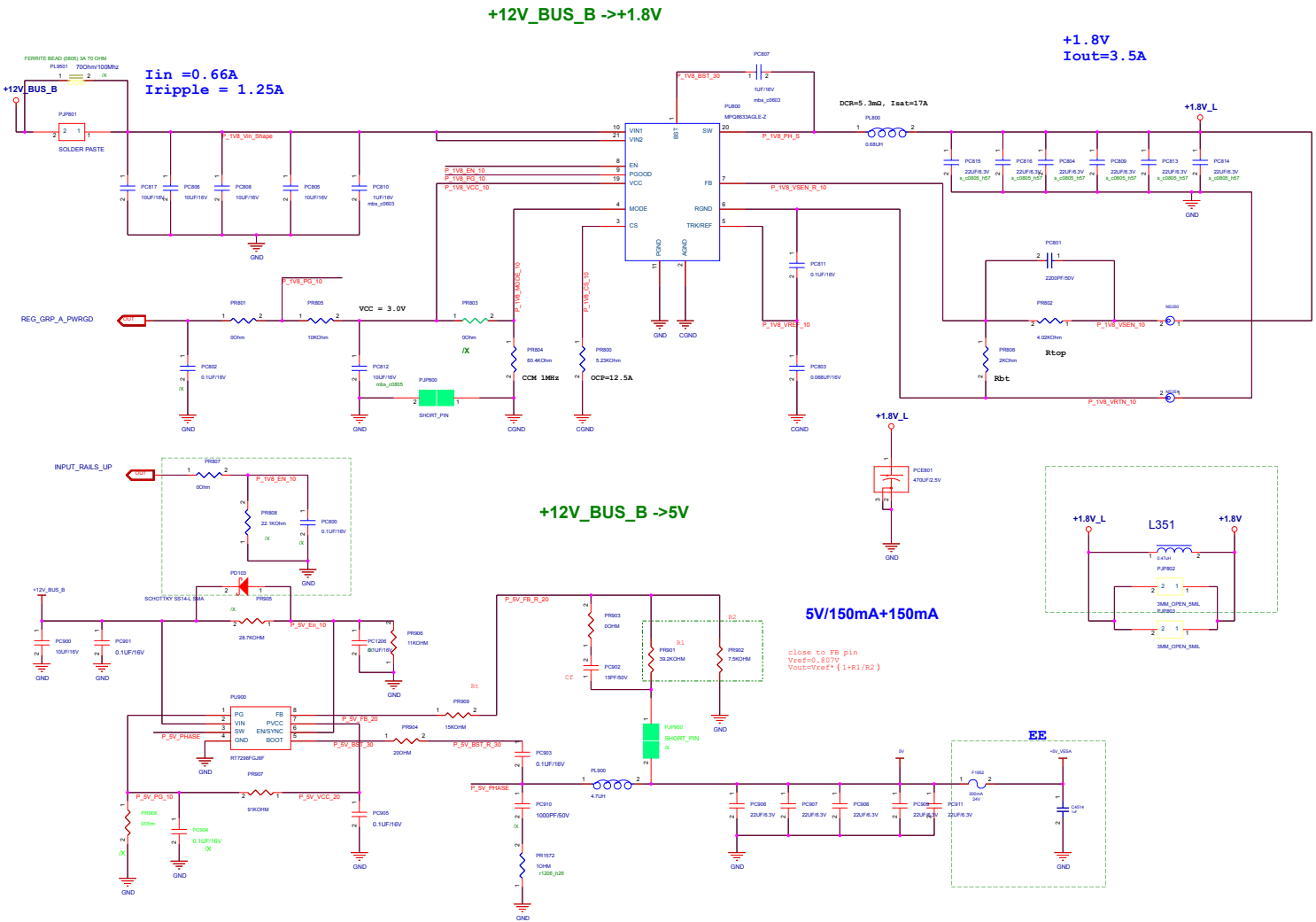
0.9V
Iout=5A

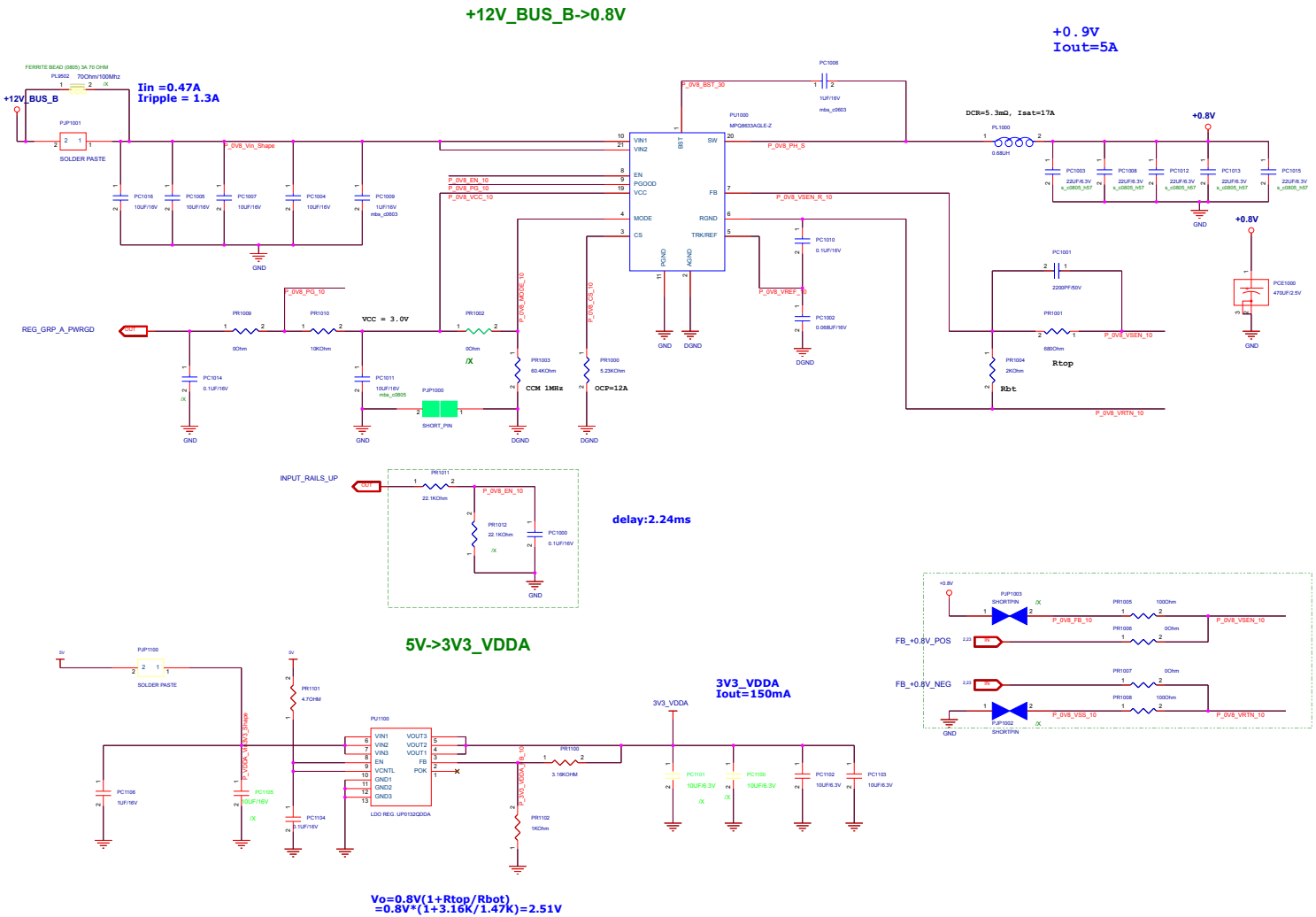
Iin =0.468A
Iripple = 1.31A



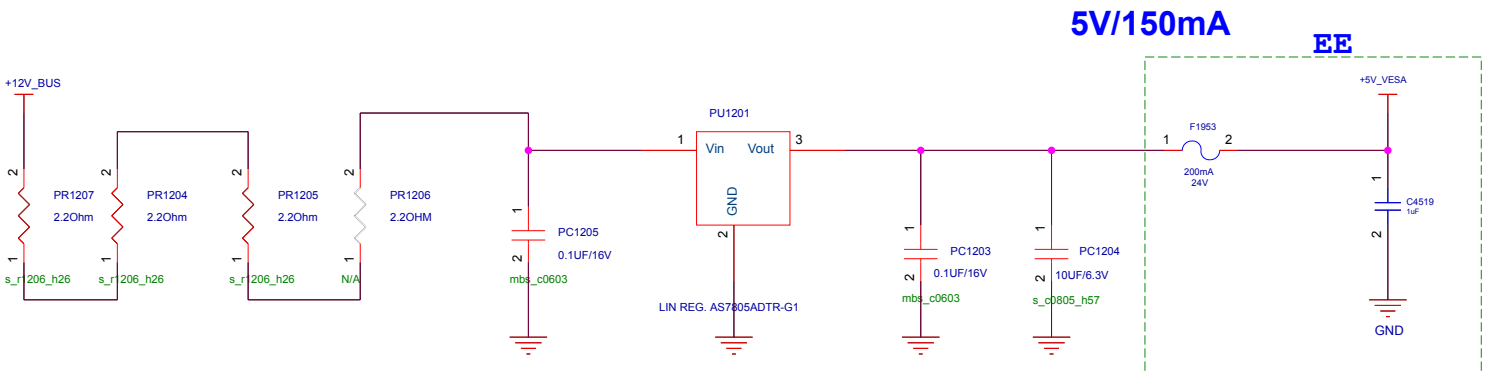


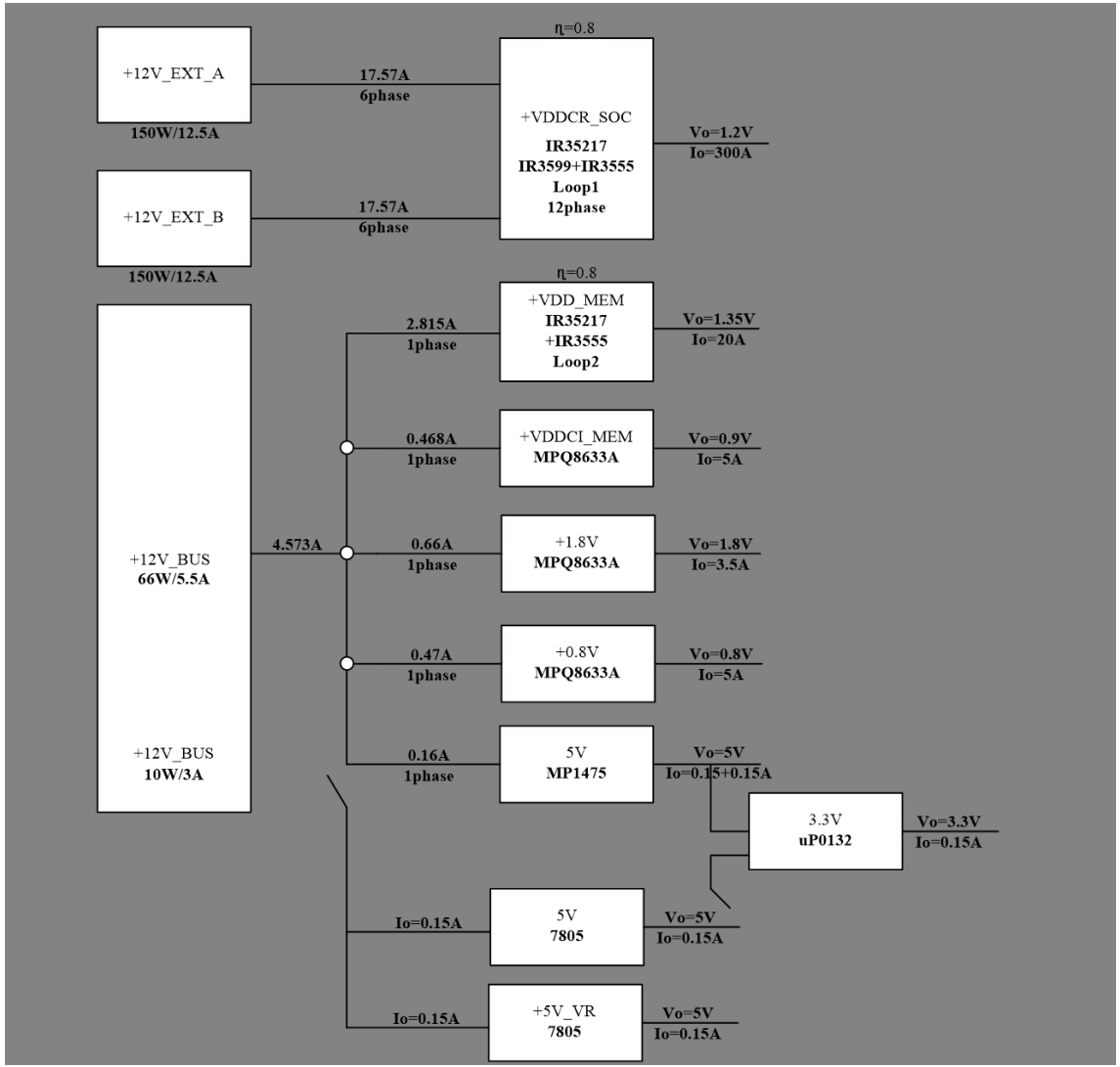


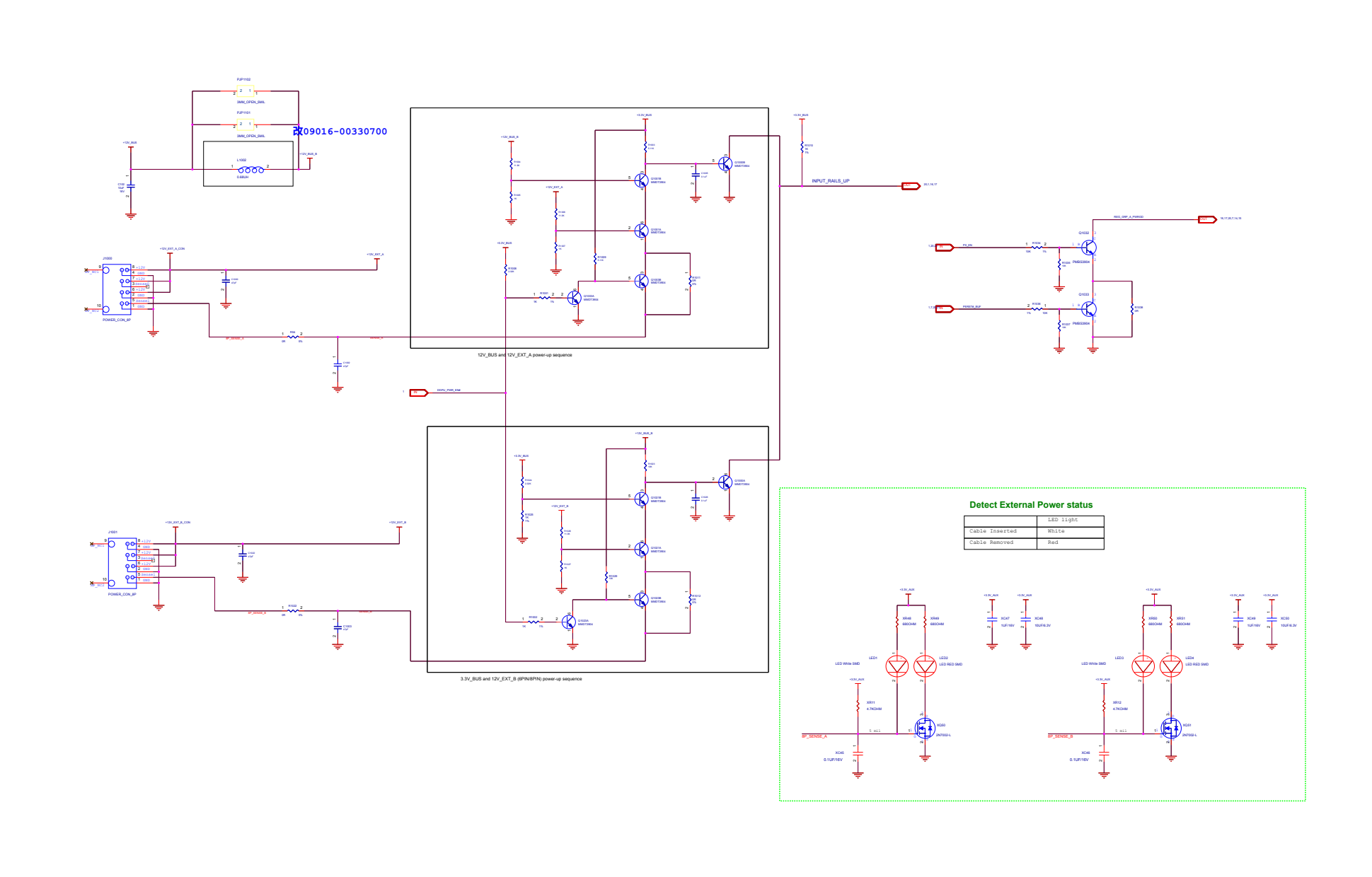

+12V_BUS_B ->+1.8V
+1.8V
Iout=3.5A
Iin =0.66A
Iripple = 1.25A
+12V_BUS_B
SOLDER PASTE
DCR=5.3mΩ, Isat=17A
+1.8V_L
REG_GRP_A_PWRGD
VCC = 3.0V
CCM 1MHz
OCP=12.5A
Rtop
Rbt
+12V_BUS_B ->5V
INPUT_RAILS_UP
5V/150mA+150mA
close to FB pin
Vref=0.807V
Vout=Vref*(1+R1/R2)
+1.8V_L
L351
+1.8V
EE

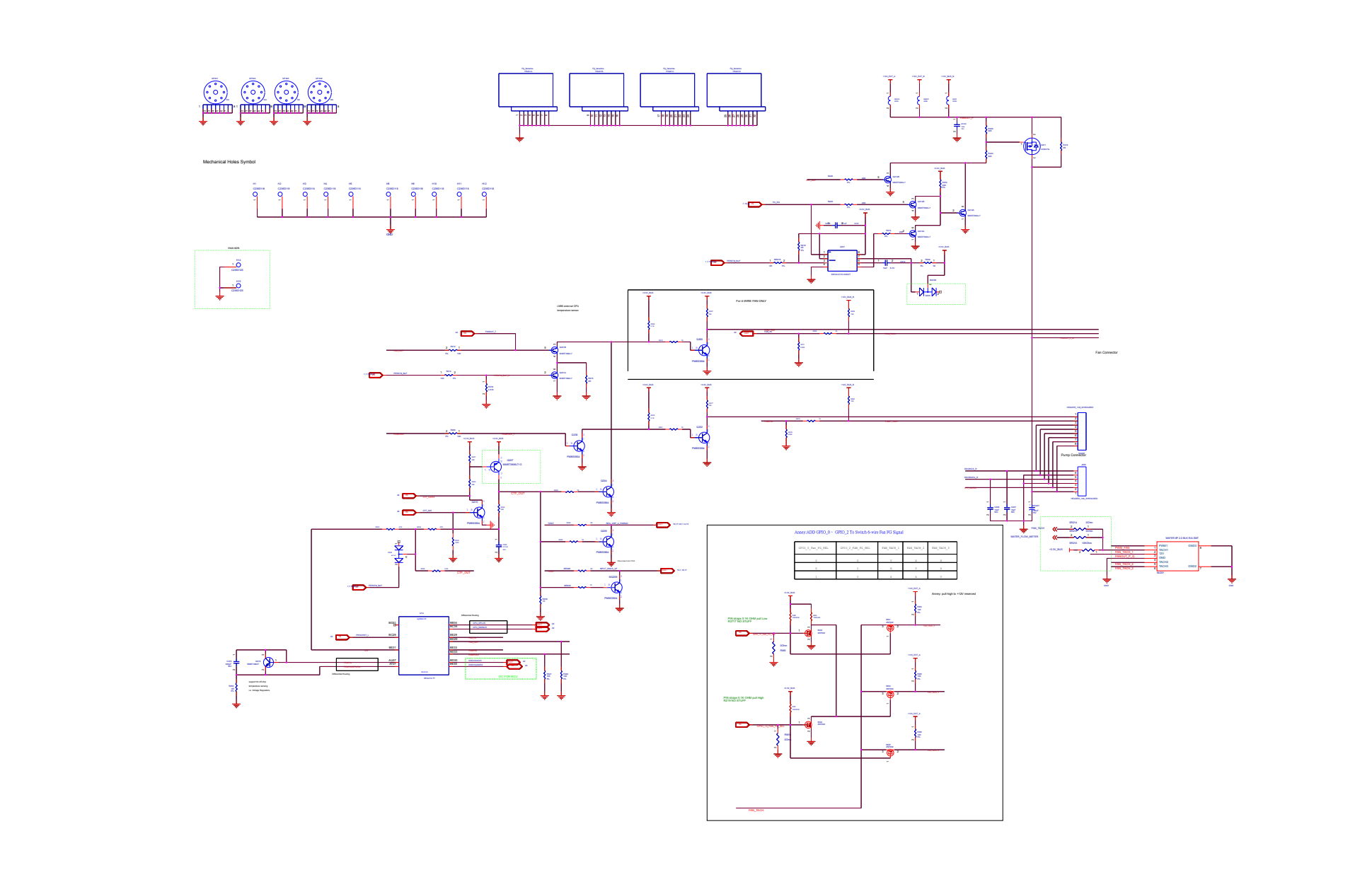

+12V_BUS_B->0.8V
+0.9V
Iout=5A
+12V_BUS_B
Iin =0.47A
Iripple = 1.3A
SOLDER PASTE
PJP1001
PU1000
MP28633AGLE-Z
VIN1
VIN2
BST
SW
EN
PGOOD
VCC
FB
MODE
RGND
CS
TRK/REF
PGND
AGND
DCR=5.3mΩ, Isat=17A
PL1000
0.68UH
+0.8V
GND
DGND
REG_GRP_A_PWRGD
VCC = 3.0V
CCM 1MHz
OCP=12A
Rtop
Rbt
SHORT_PIN
INPUT_RAILS_UP
delay:2.24ms
5V->3V3_VDDA
3V3_VDDA
Iout=150mA
LDO REG. UP0132QDDA
Vo=0.8V(1+Rtop/Rbot)
=0.8V*(1+3.16K/1.47K)=2.51V
FB_+0.8V_POS
FB_+0.8V_NEG
SHORTPIN

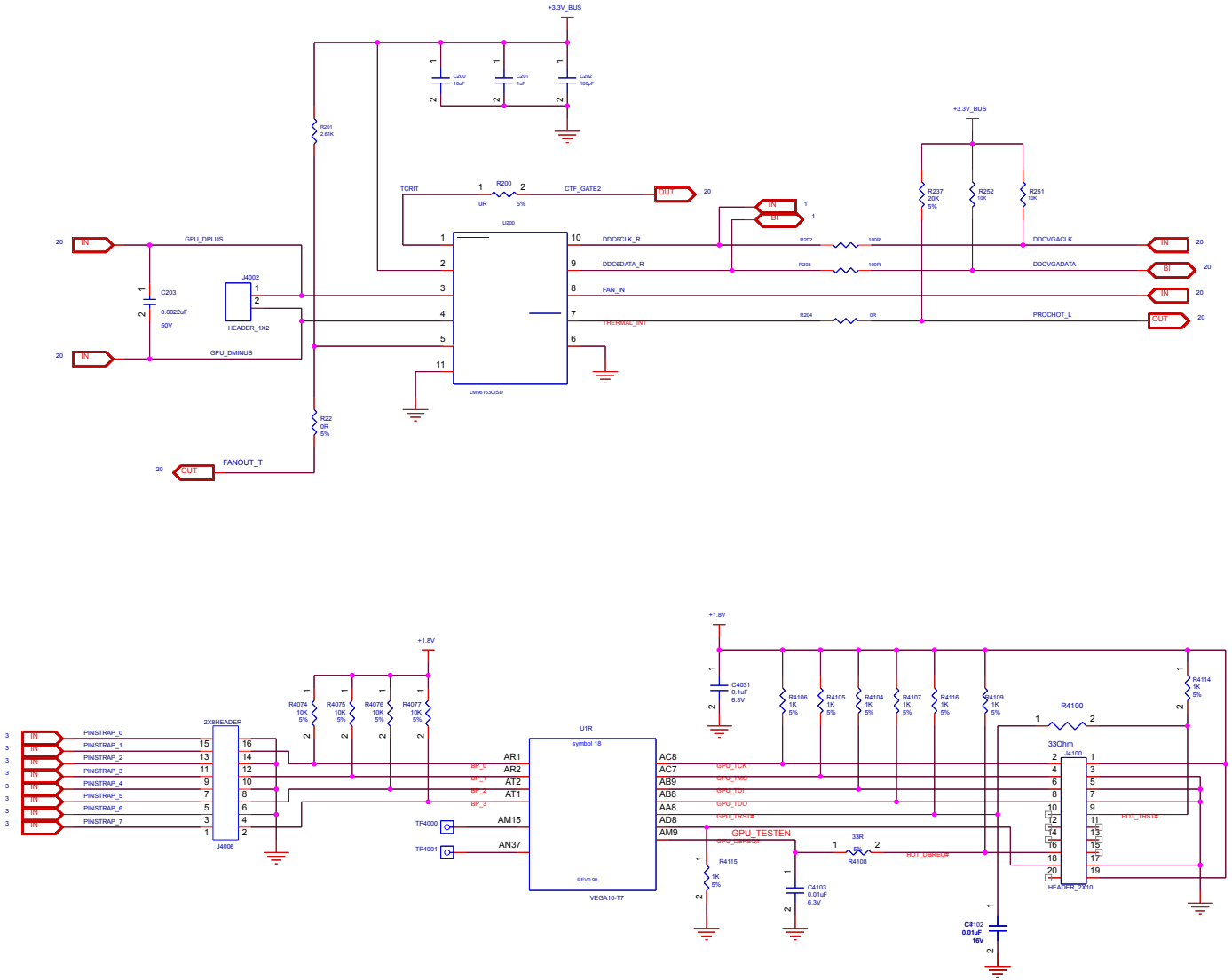
12V_BUS --> +5V


5V/150mA
EE
+12V_BUS
PR1207
2.2Ohm
s_r1206_h26
PR1204
2.2Ohm
s_r1206_h26
PR1205
2.2Ohm
s_r1206_h26
PR1206
2.2OHM
N/A
PC1205
0.1UF/16V
mbs_c0603
PU1201
Vin
Vout
GND
LIN REG. AS7805ADTR-G1
PC1203
0.1UF/16V
mbs_c0603
PC1204
10UF/6.3V
s_c0805_h57
F1953
200mA
24V
+5V_VESA
C4519
1uF
GND

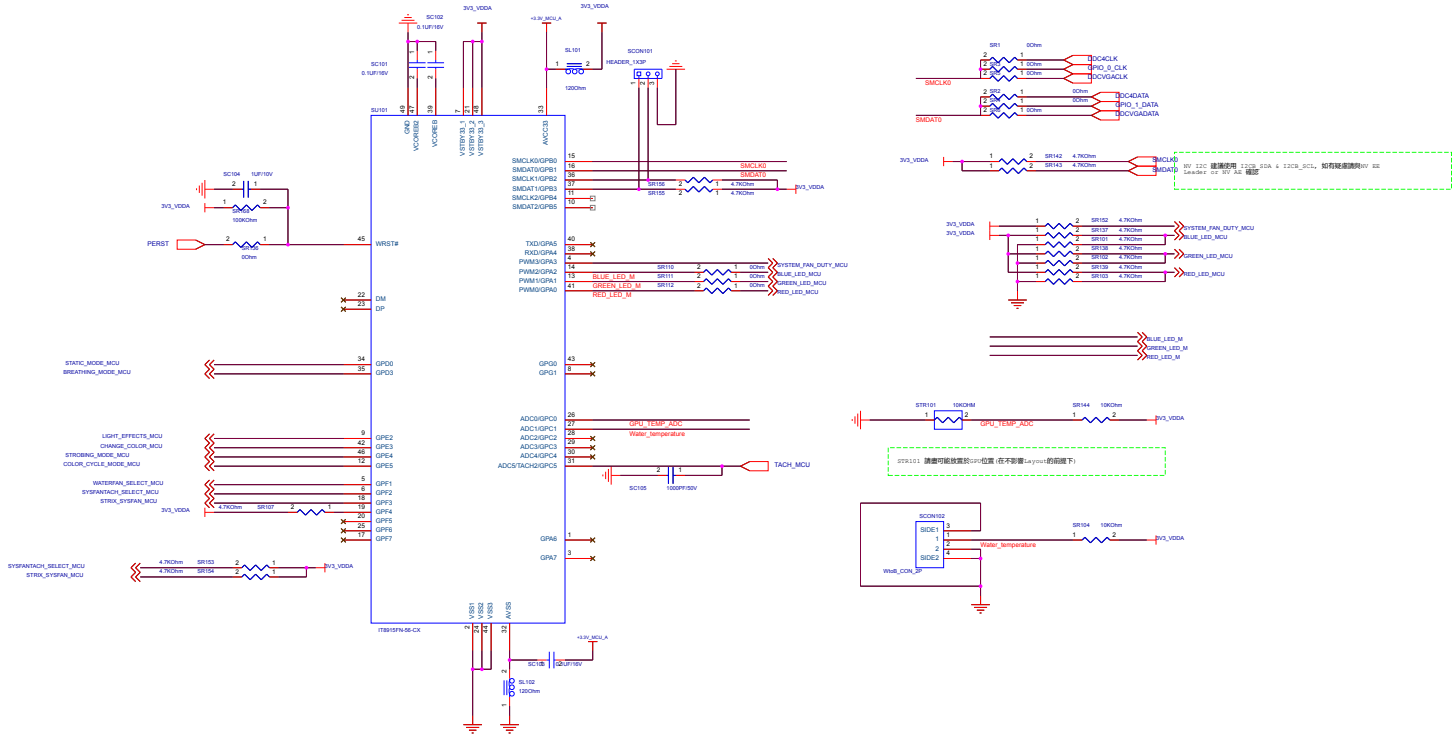

+12V_EXT_A
150W/12.5A
17.57A
6phase
η=0.8
+VDDCR_SOC
IR35217
IR3599+IR3555
Loop1
12phase
Vo=1.2V
Io=300A
+12V_EXT_B
150W/12.5A
17.57A
6phase
η=0.8
+VDD_MEM
IR35217
+IR3555
Loop2
2.815A
1phase
Vo=1.35V
Io=20A
+12V_BUS
66W/5.5A
4.573A
0.468A
1phase
+VDDCI_MEM
MPQ8633A
Vo=0.9V
Io=5A
0.66A
1phase
+1.8V
MPQ8633A
Vo=1.8V
Io=3.5A
0.47A
1phase
+0.8V
MPQ8633A
Vo=0.8V
Io=5A
+12V_BUS
10W/3A
0.16A
1phase
5V
MP1475
Vo=5V
Io=0.15+0.15A
3.3V
uP0132
Vo=3.3V
Io=0.15A
Io=0.15A
5V
7805
Vo=5V
Io=0.15A
Io=0.15A
+5V_VR
7805
Vo=5V
Io=0.15A


X09016-00330700
12V_BUS and 12V_EXT_A power-up sequence
3.3V_BUS and 12V_EXT_B (6PIN/8PIN) power-up sequence
INPUT_RAILS_UP
Detect External Power status
Cable Inserted
White
Cable Removed
Red


Mechanical Holes Symbol
Fan Connector
Pump Connector
Annex: ADD GPIO_0 ~ GPIO_2 To Switch 6-wire Pat PCI Signal
Annex: pull-high to +12V reserved

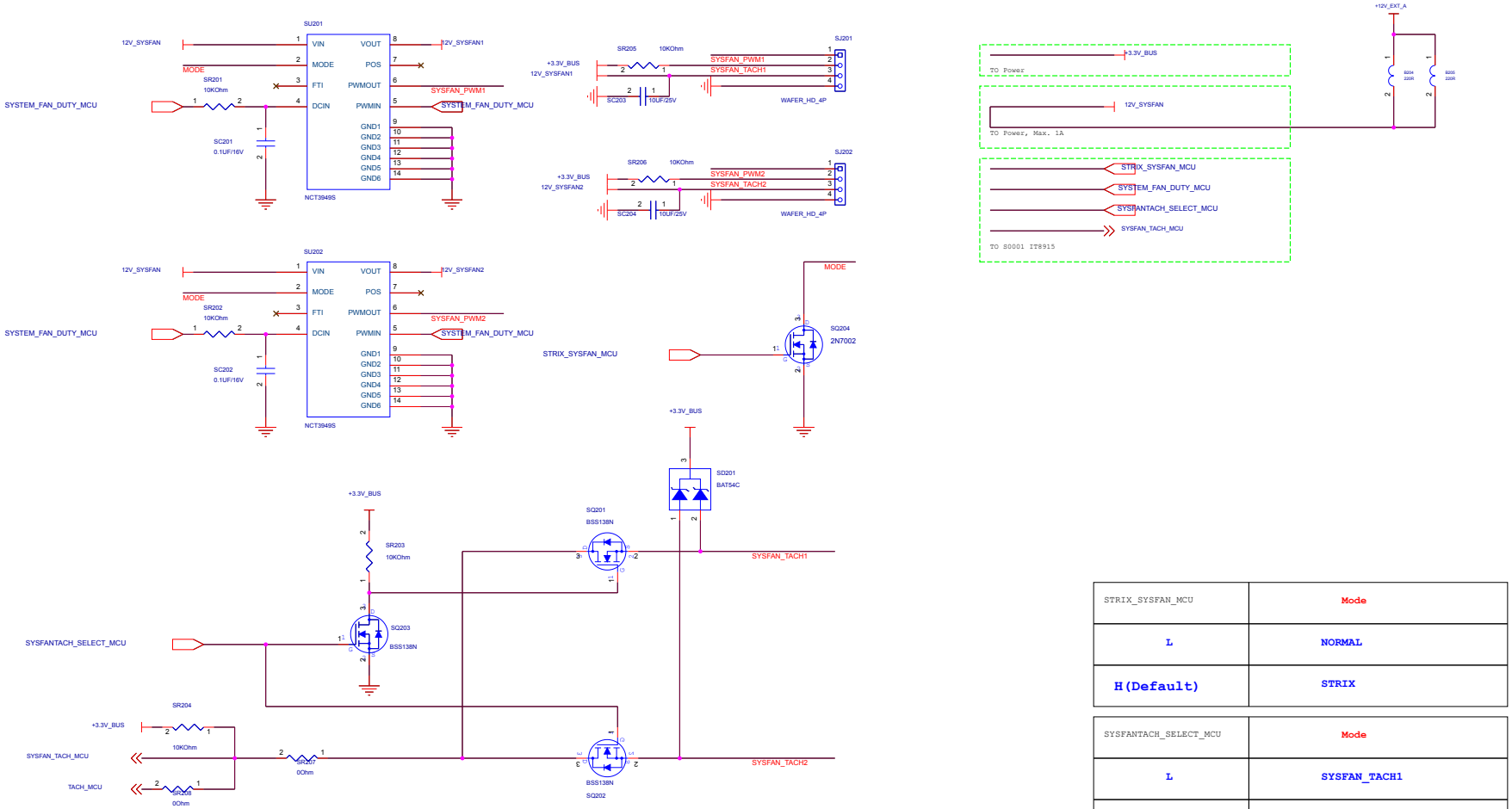


$CDS_IMAGE|clipboard_3.jpg|993|764



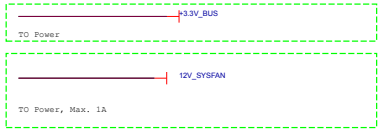
STRIX_SYSFAN_MCU	Mode
L	NORMAL
H(Default)	STRIX

SYSFANTACH_SELECT_MCU	Mode
L	SYSFAN_TACH1
H(Default)	SYSFAN_TACH2

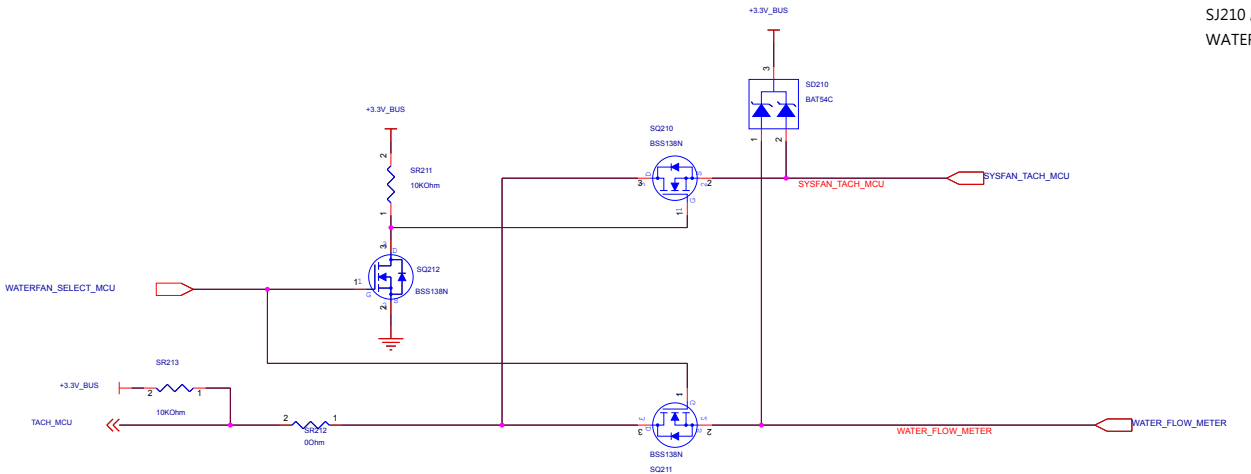


STRIX_SYSFAN_MCU	Mode
L	NORMAL
H(Default)	STRIX

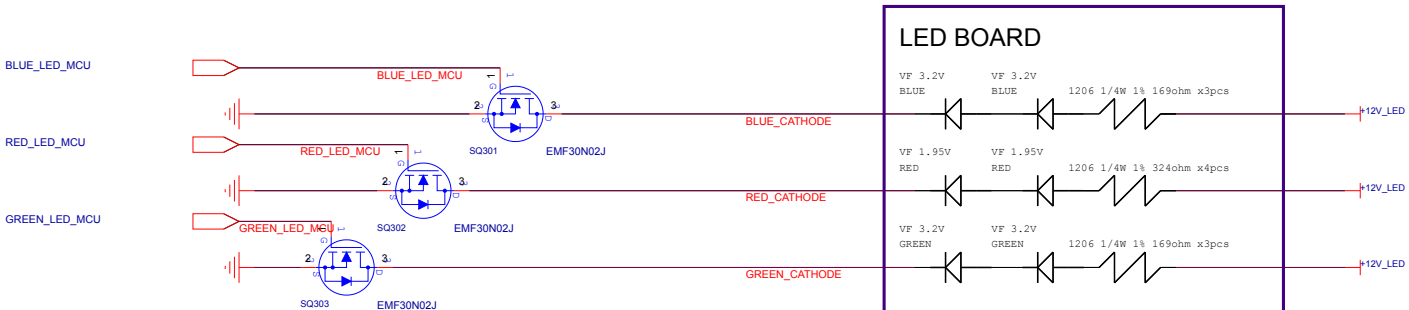
SYSFANTACH_SELECT_MCU	Mode
L	SYSFAN_TACH1
H(Default)	SYSFAN_TACH2

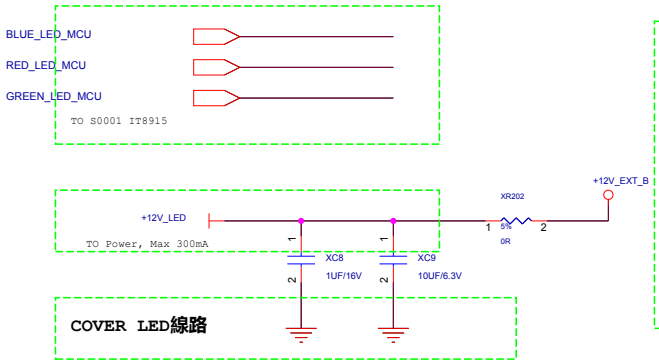


SJ210 可與VGA Card Fan Conn共用
SJ210 所使用之12V_SYSFAN 可更改為原設計VGA Card之12V
WATER_FLOW_METER若需變更Net Name須注意應拉到的Net



SYSFANTACH_SELECT_MCU	Mode
L	SYSFAN
H(Default)	WATER FLOW METER


BLUE_LED_MCU
RED_LED_MCU
GREEN_LED_MCU
BLUE_LED_MCU
RED_LED_MCU
GREEN_LED_MCU
SQ301
EMF30N02J
SQ302
EMF30N02J
SQ303
EMF30N02J
BLUE_CATHODE
RED_CATHODE
GREEN_CATHODE
LED BOARD
VF 3.2V
BLUE
VF 3.2V
BLUE
1206 1/4W 1% 169ohm x3pcs
+12V_LED
VF 1.95V
RED
VF 1.95V
RED
1206 1/4W 1% 324ohm x4pcs
+12V_LED
VF 3.2V
GREEN
VF 3.2V
GREEN
1206 1/4W 1% 169ohm x3pcs
+12V_LED


BLUE_LED_MCU
RED_LED_MCU
GREEN_LED_MCU
TO S0001 IT8915
+12V_LED
TO Power, Max 300mA
XR202
5%
0R
+12V_EXT_B
XC8
1UF/16V
XC9
10UF/6.3V
COVER LED線路

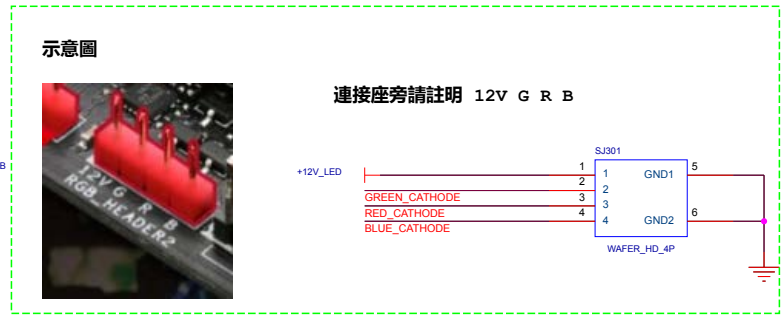
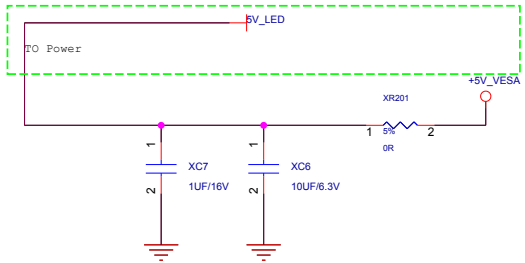
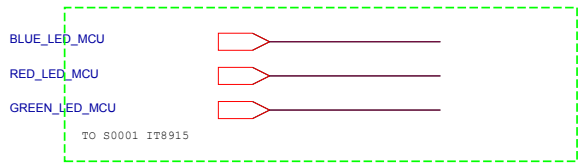
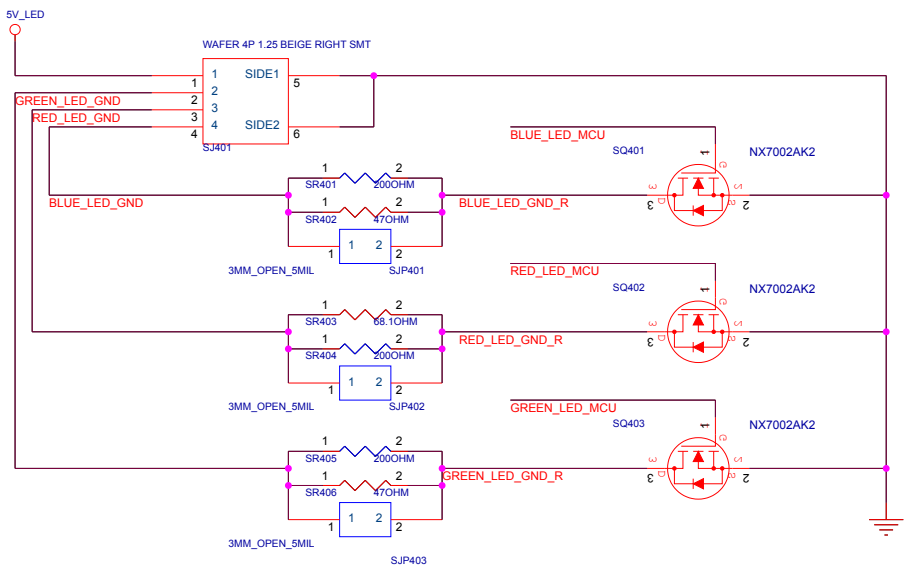


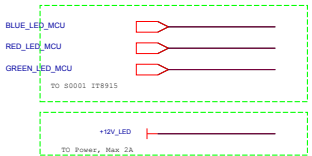
示意圖
連接座旁請註明 12V G R B
+12V_LED
SJ301
GREEN_CATHODE
RED_CATHODE
BLUE_CATHODE
GND1
GND2
WAFER_HD_4P

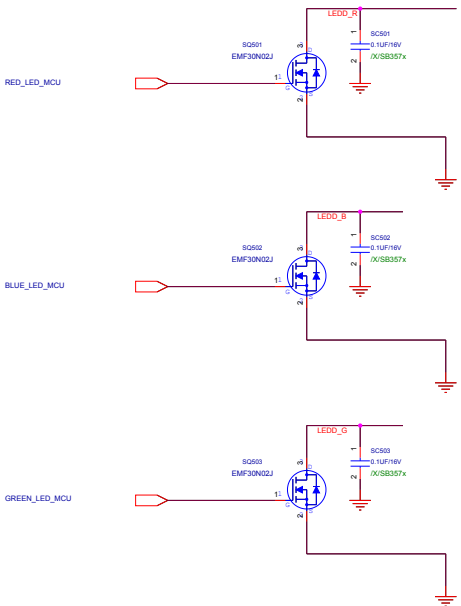
背板ROG LED線路


5V_LED
TO Power
+5V_VESA
XR201
5%
0R
XC7
1UF/16V
XC6
10UF/6.3V


BLUE_LED_MCU
RED_LED_MCU
GREEN_LED_MCU
TO S0001 IT8915


5V_LED
WAFER 4P 1.25 BEIGE RIGHT SMT
SIDE1
SIDE2
SJ401
GREEN_LED_GND
RED_LED_GND
BLUE_LED_GND
BLUE_LED_MCU
SQ401
NX7002AK2
SR401
200OHM
SR402
47OHM
3MM_OPEN_5MIL
SJP401
BLUE_LED_GND_R
RED_LED_MCU
SQ402
NX7002AK2
SR403
68.1OHM
SR404
200OHM
3MM_OPEN_5MIL
SJP402
RED_LED_GND_R
GREEN_LED_MCU
SQ403
NX7002AK2
SR405
200OHM
SR406
47OHM
3MM_OPEN_5MIL
SJP403
GREEN_LED_GND_R


BLUE_LED_MCU
RED_LED_MCU
GREEN_LED_MCU
TO SO001 IT8915
+12V_LED
TO Power, Max 2A


LEDD_R
SQ501
EMF30N02J
SC501
0.1UF/16V
/X/SB357x
RED_LED_MCU
LEDD_B
SQ502
EMF30N02J
SC502
0.1UF/16V
/X/SB357x
BLUE_LED_MCU
LEDD_G
SQ503
EMF30N02J
SC503
0.1UF/16V
/X/SB357x
GREEN_LED_MCU

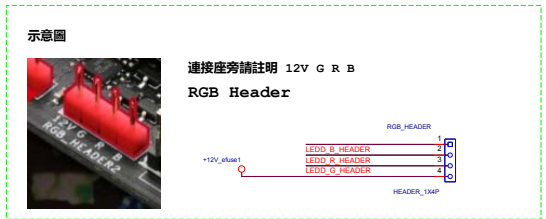
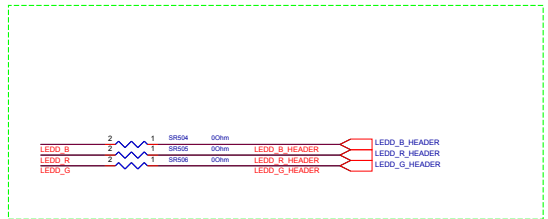
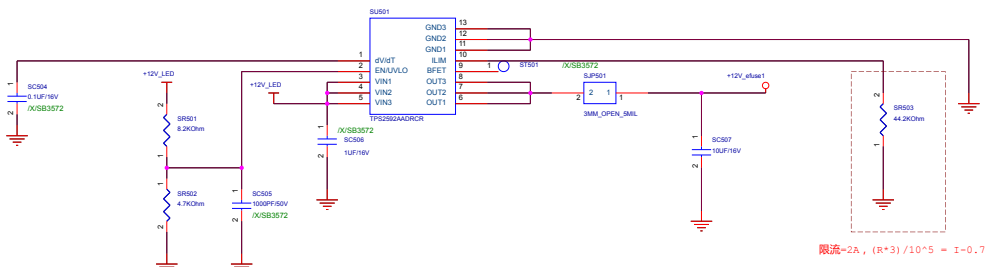
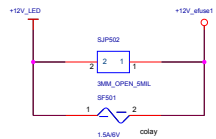
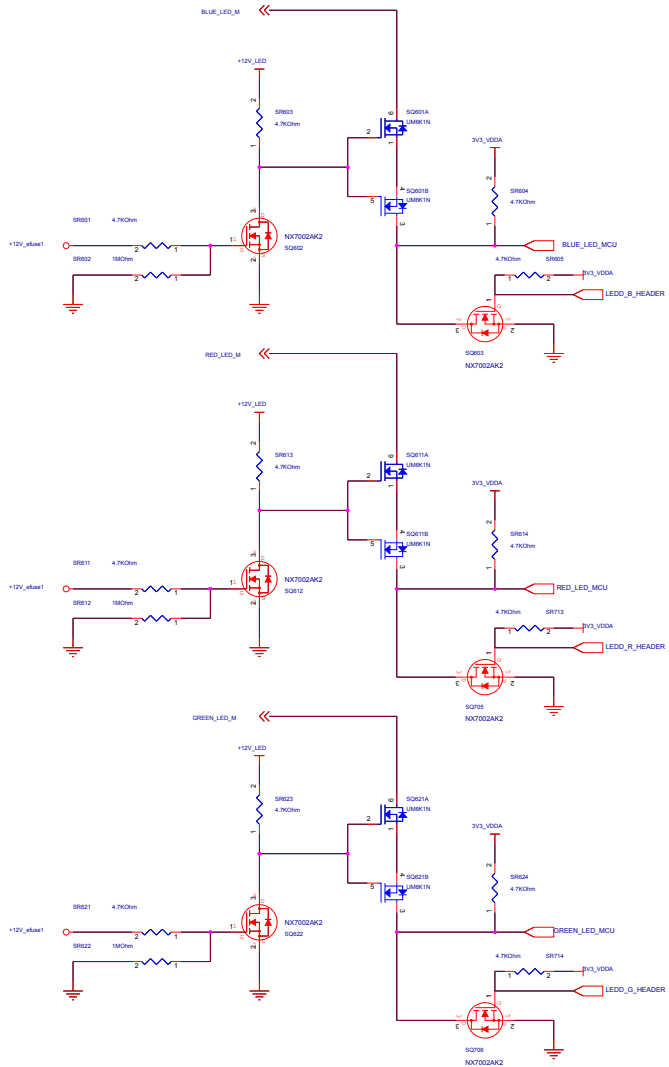


示意圖
連接座旁請註明 12V G R B
RGB Header
12V G R B
RGB_HEADER2
RGB_HEADER
+12V_efuse1
LEDD_B_HEADER
LEDD_R_HEADER
LEDD_G_HEADER
HEADER_1X4P

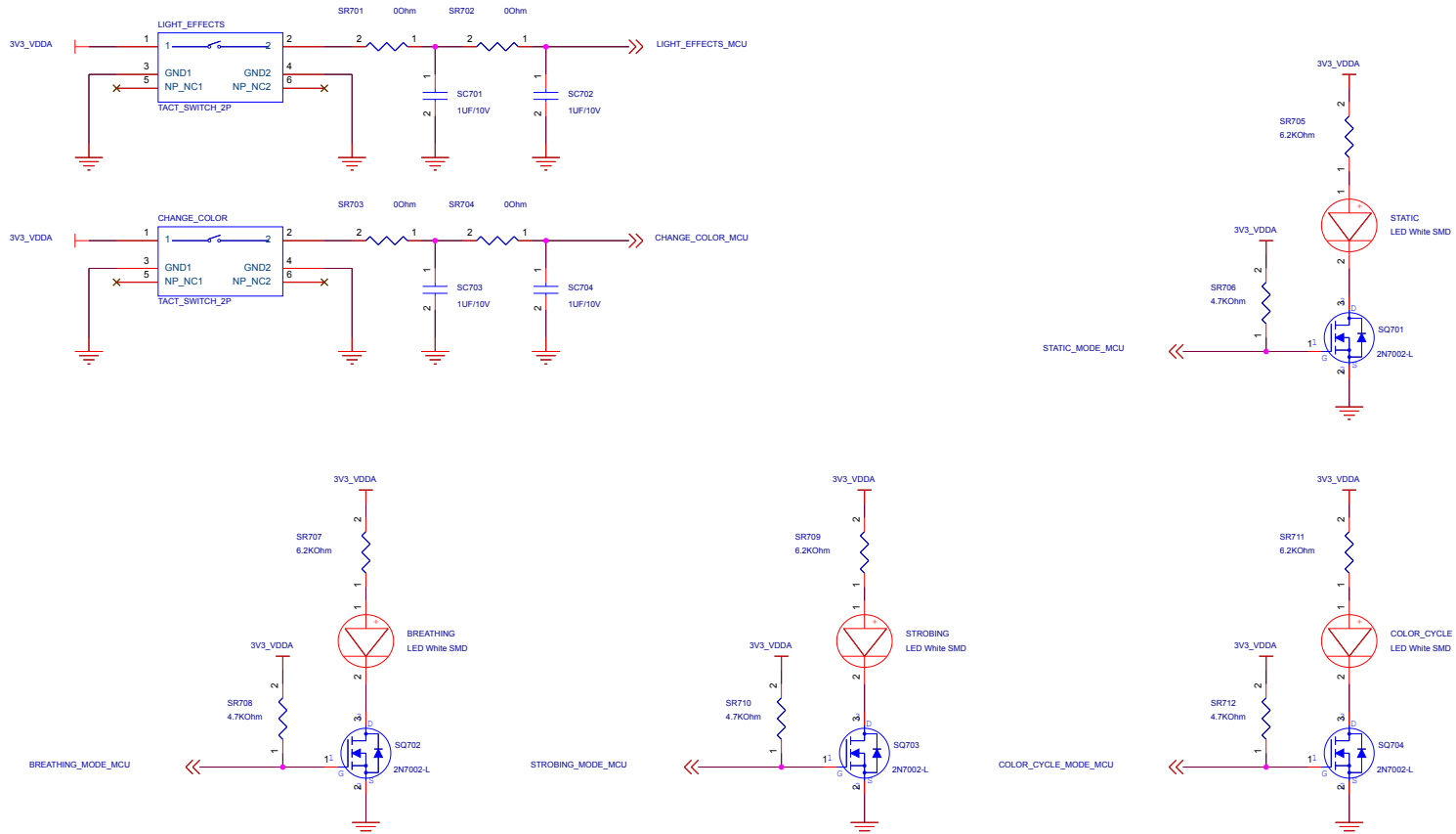

LEDD_B
LEDD_R
LEDD_G
SRS04
SRS05
SRS06
0Ohm
LEDD_B_HEADER
LEDD_R_HEADER
LEDD_G_HEADER


eFuse
SU501
TPS2592AADRCR
GND3
GND2
GND1
dV/dT
EN/UVLO
VIN1
VIN2
VIN3
ILIM
BFET
OUT3
OUT2
OUT1
ST501
/X/SB3572
SJP501
3MM_OPEN_5MIL
+12V_efuse1
SC504
0.1UF/16V
/X/SB3572
+12V_LED
SR501
8.2KOhm
SR502
4.7KOhm
SC505
1000PF/50V
/X/SB3572
SC506
1UF/16V
SC507
10UF/16V
SR503
44.2KOhm
限流=2A, (R*3)/10^5 = I=0.7

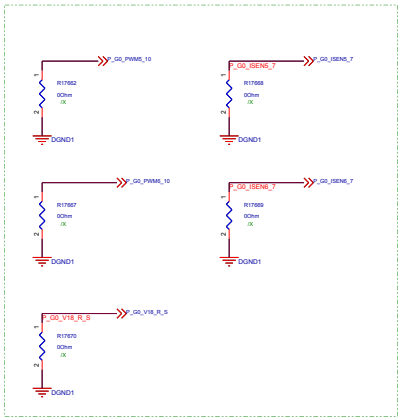

+12V_LED
+12V_efuse1
SJP502
3MM_OPEN_5MIL
SF501
1.5A/8V
colay



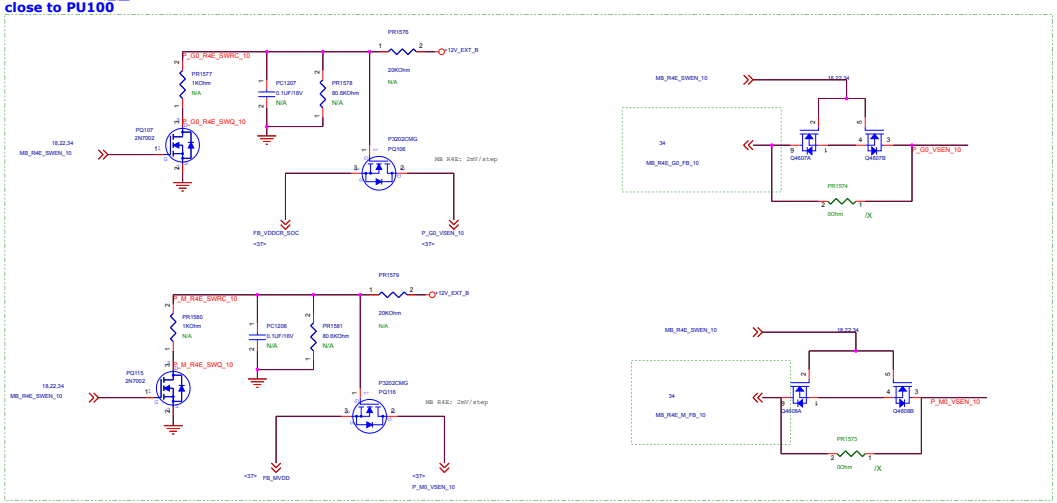
+12V_efuse1	LED
12V	HEADER CONTROL
X	MCU CONTROL


LIGHT_EFFECTS
3V3_VDDA
SR701 0Ohm
SR702 0Ohm
LIGHT_EFFECTS_MCU
GND1
GND2
NP_NC1
NP_NC2
TACT_SWITCH_2P
SC701
1UF/10V
SC702
1UF/10V
CHANGE_COLOR
SR703 0Ohm
SR704 0Ohm
CHANGE_COLOR_MCU
SC703
1UF/10V
SC704
1UF/10V
3V3_VDDA
SR705
6.2KOhm
STATIC
LED White SMD
SR706
4.7KOhm
STATIC_MODE_MCU
SQ701
2N7002-L
SR707
6.2KOhm
BREATHING
LED White SMD
SR708
4.7KOhm
BREATHING_MODE_MCU
SQ702
2N7002-L
SR709
6.2KOhm
STROBING
LED White SMD
SR710
4.7KOhm
STROBING_MODE_MCU
SQ703
2N7002-L
SR711
6.2KOhm
COLOR_CYCLE
LED White SMD
SR712
4.7KOhm
COLOR_CYCLE_MODE_MCU
SQ704
2N7002-L

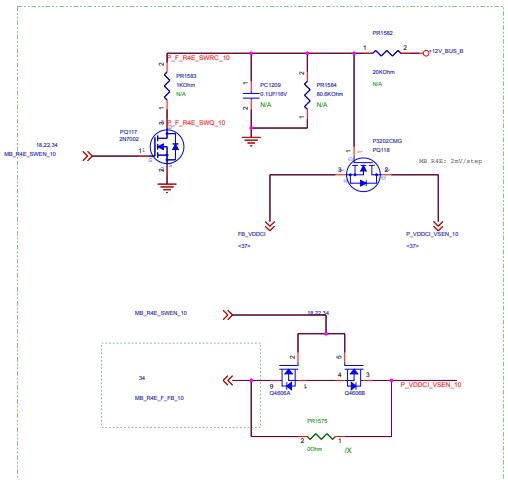
Down Phase



SOC & MVDD 超壓
close to PU100



VDDCI 超壓
close to PU600



MB R4E Enable