

# MS8849

ATI R300 9500Pro, 4MX32 BGA DDR, DVI-I, VIDEO IN, TV-OUT, AGP 8X

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FREQUENCY	MHZ
CORE	275
MEMORY	270

# MEMORY CHANNEL C D

DDR 8M X 16 (TSOP)

MEMORY TERMINATIONS C D

PRIMARY CRT LOGIC  
SHEET 15

VGA1 DB15 CONN  
SHT 16

INTEG TMDS LOGIC

DVI-I CONN  
SHT 16

THEATER VIDEO-IN CONN  
SHT 14

TVout LOGIC  
SHT 14

TVout CONN  
SHT 14

SECONDARY CRT LOGIC  
SHT 15

MEM A B  
MEM C D  
DAC1  
ROM  
R300  
SHT 3, 4, 5, 8, 9  
TMD5  
TVO  
DVO  
VIP  
DAC2  
AGP

STRAPS  
SHT 12

BIOS  
SHT 13

FAN  
SHT 13

EXTERNAL POWER  
SHT 6

POWER REGULATION  
SHT 6, 7

AGP BUS 2X/4X/8X  
SHT 2

VDDC VDDC18 VDD VTT VDDQ  
PVDD TPVDD MPVDD  
A2VDD Vref

+3.3V +5V +12V

AD31..0 CBE3..0 CPUCLK STOP# PAR REQ#  
IRDY# GNT# TRDY# DEVSEL# RESET#  
FRAME# CLK INTR SUSPEND# SERR#  
AGPREF SBA[7..0] ST2..0 SR\_STB SR\_STB#  
AD\_STB1 AD\_STB1# AD\_STB0 AD\_STB0# RBF#

MC/D[14..0]MDC/D[63..0]QSC/D[7..0]CS0C/D# D0MC/D[0..7]  
CASC/D#RASC/D# WEA/B# CKEC/DCLKC/D01 CLKC/D01#

R G B HSY VSY DDC1DATA DDC1CLK

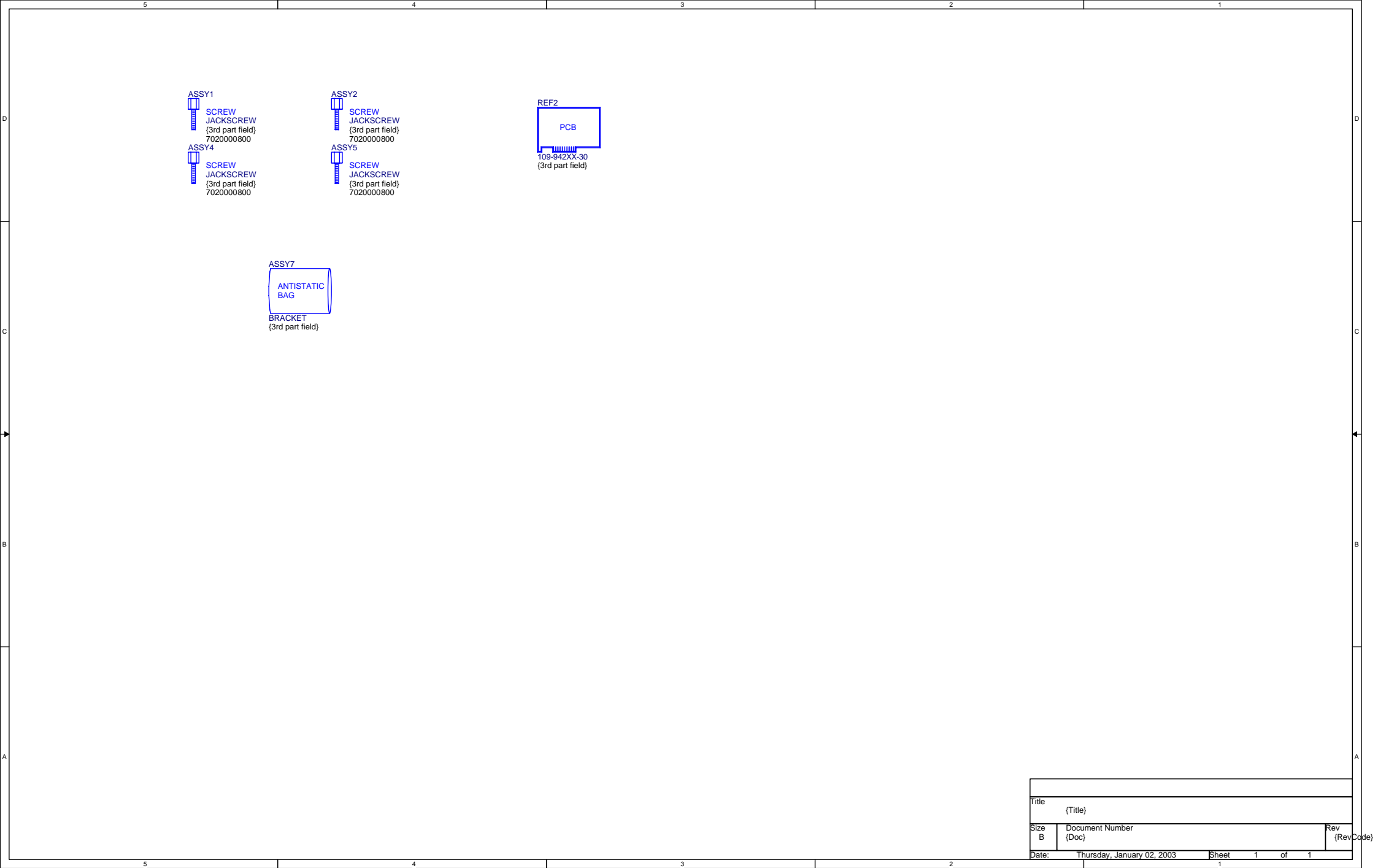
TMDS\_TX[C.2..0]N TMDS\_TX[C.2..0]P HPD, DDC2CLK DDC2DATA

DVO, VIP Host, VIP Data

Y/R C/G COMP/B H2SYNC CRT2DDCCDATA CRT2DDCCLK V2SYNC

GPI0

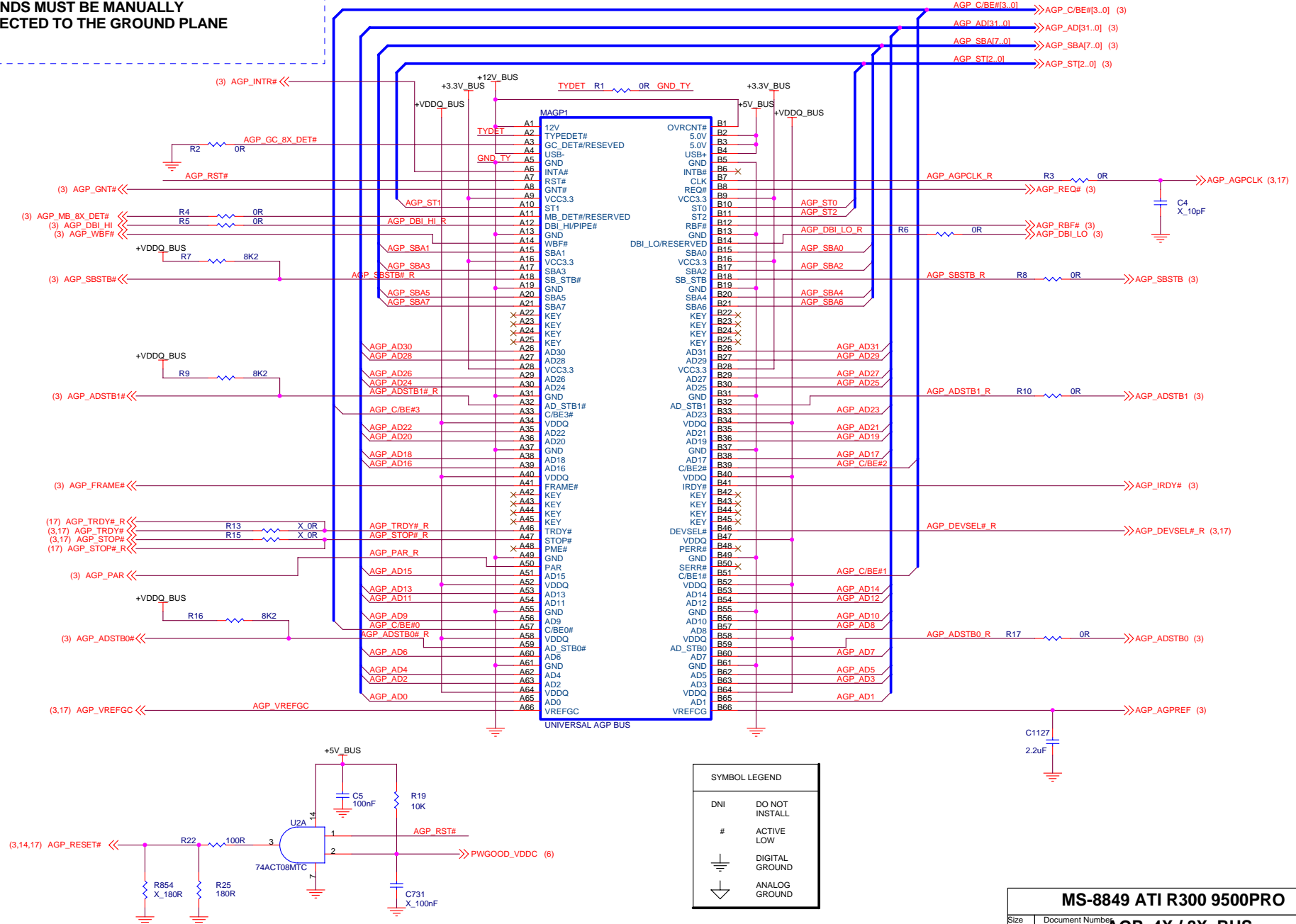
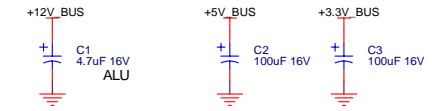
DEM U X  
SHT 14





Title		
(Title)		
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B	(Doc)	
Date:	Thursday, January 02, 2003	Rev (RevCode)
	Sheet	1 of 1

## 2X/4X/8X AGP BUS

**NOTE: THIS IS A DRAWING. THESE  
GROUNDS MUST BE MANUALLY  
CONNECTED TO THE GROUND PLANE**

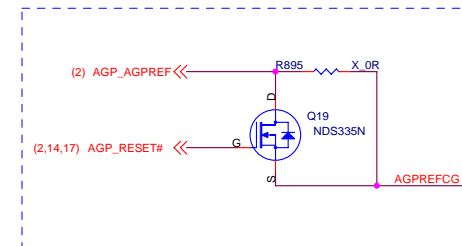
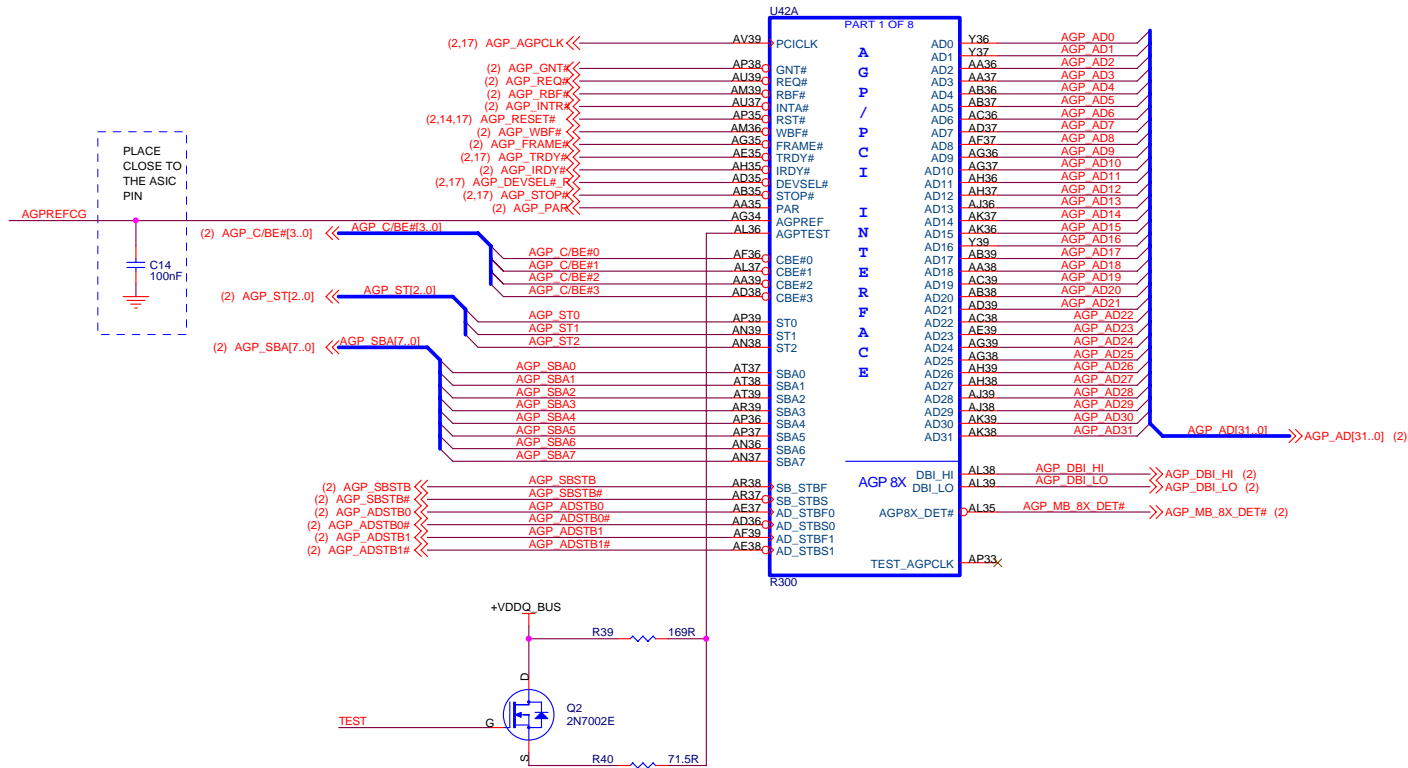


SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

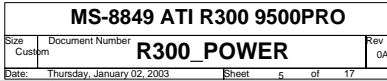
MS-8849 ATI R300 9500PRO

Number **AGP\_4X / 8X\_BUS**

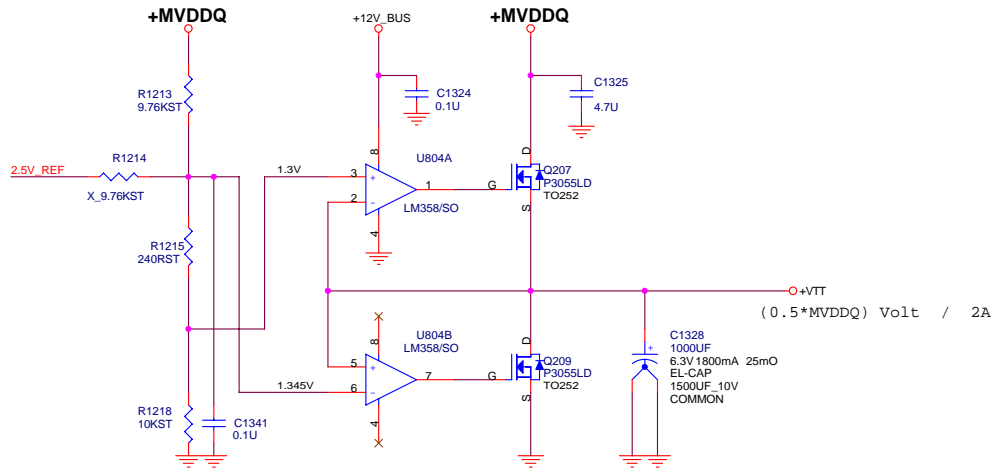
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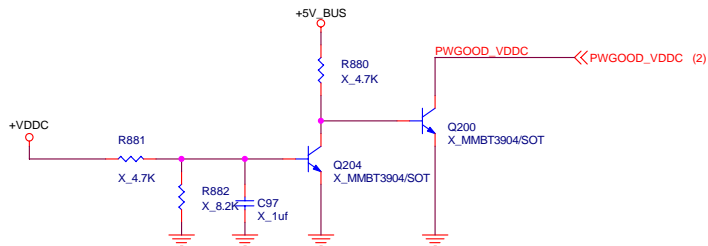




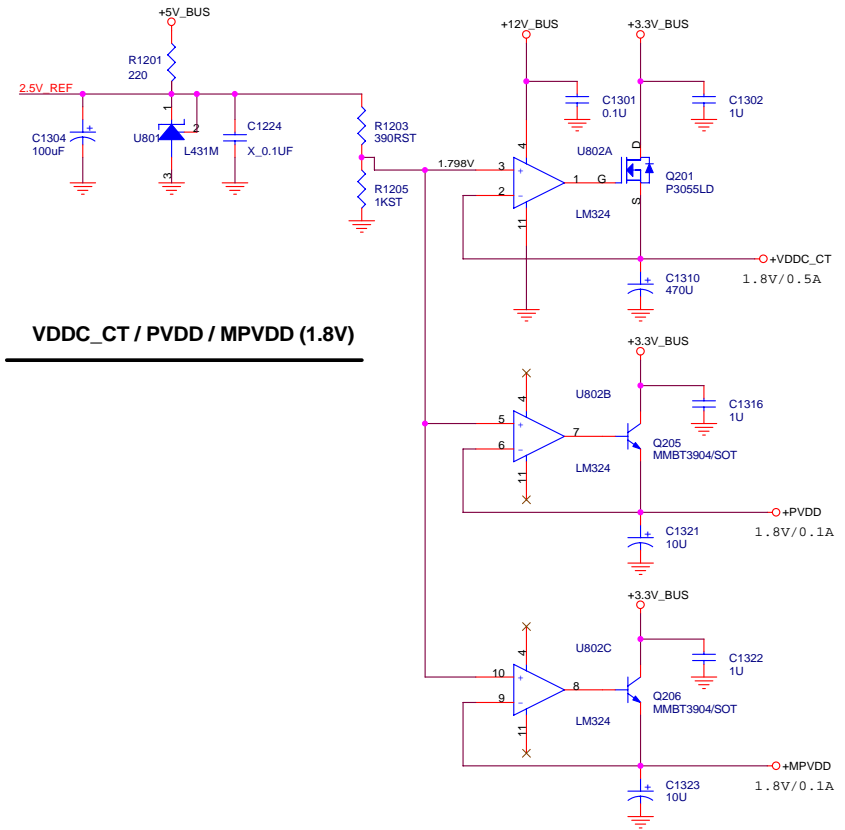
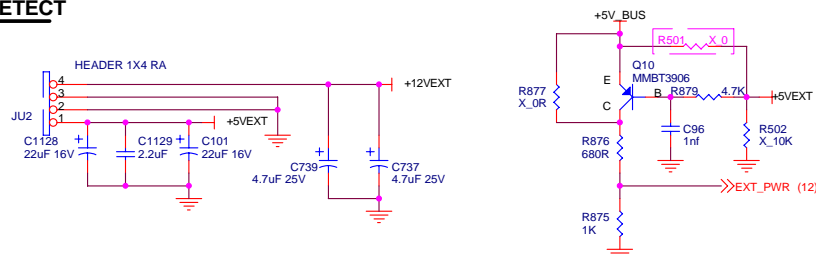
## VTT



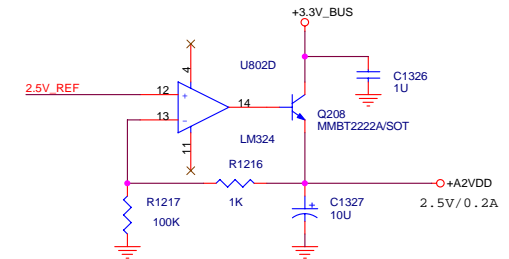
## POWER SEQUENCE



## EXTERNAL POWER DETECT



## A2VDD (2.5V)

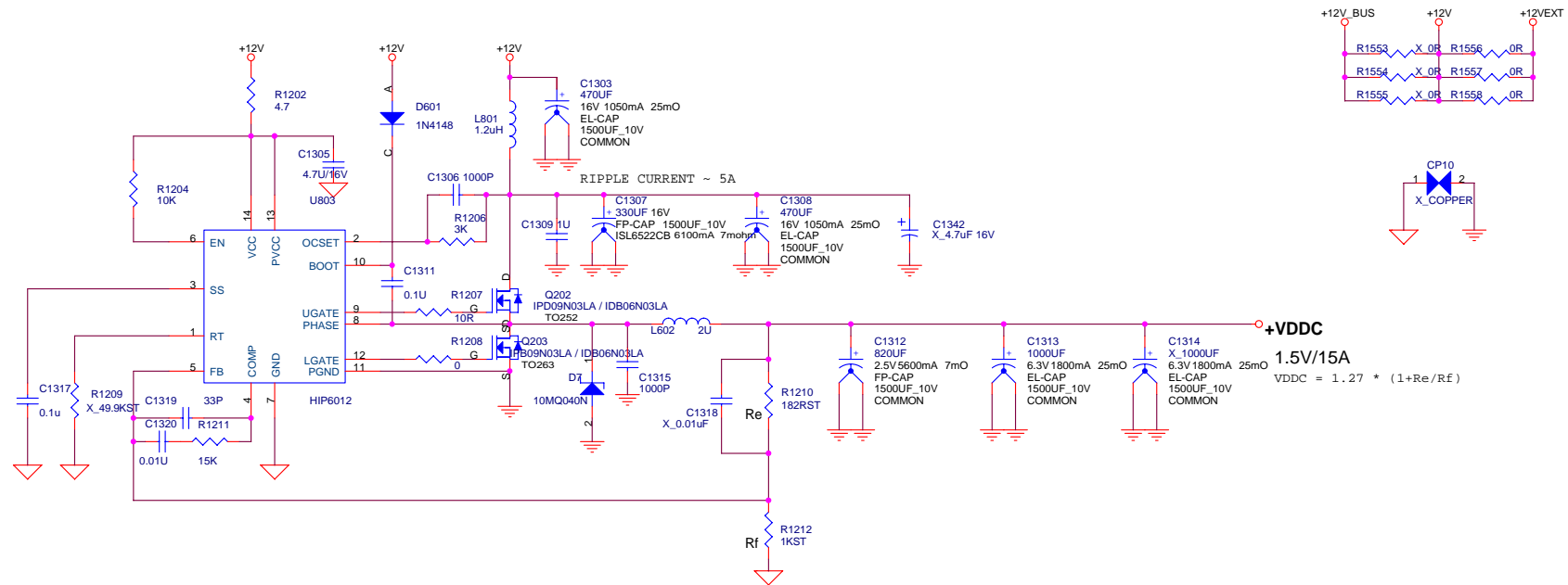


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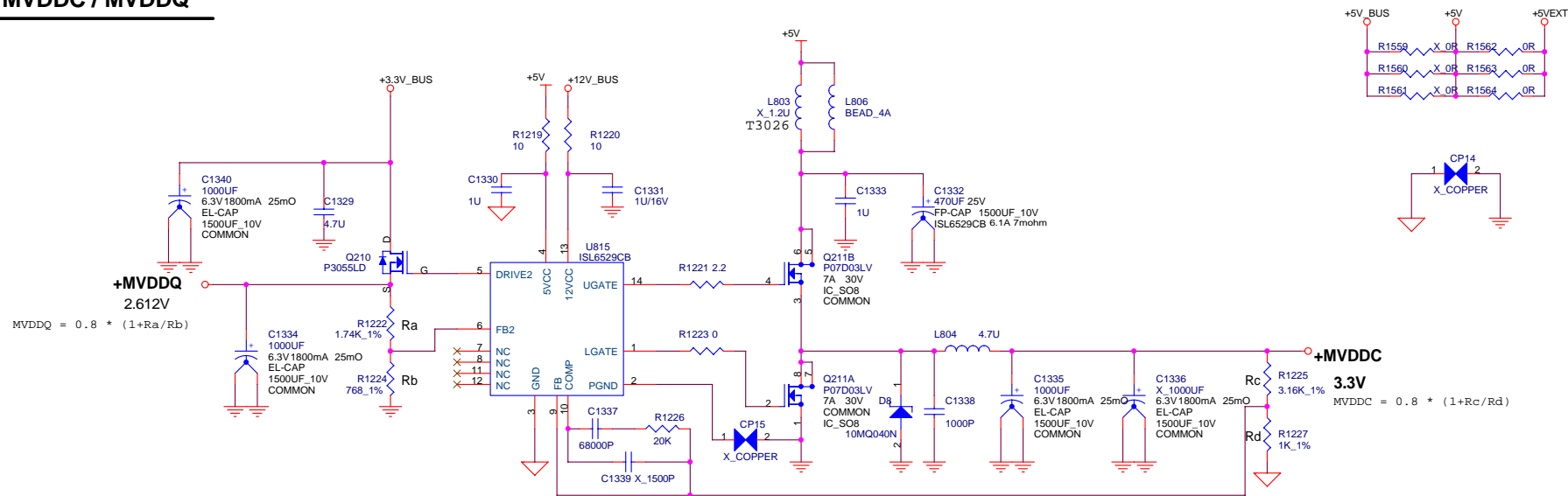
Size	Document Number	Rev
Custom	POWER REGULATOR 1	0A
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## VDDC



## MVDDC / MVDDQ

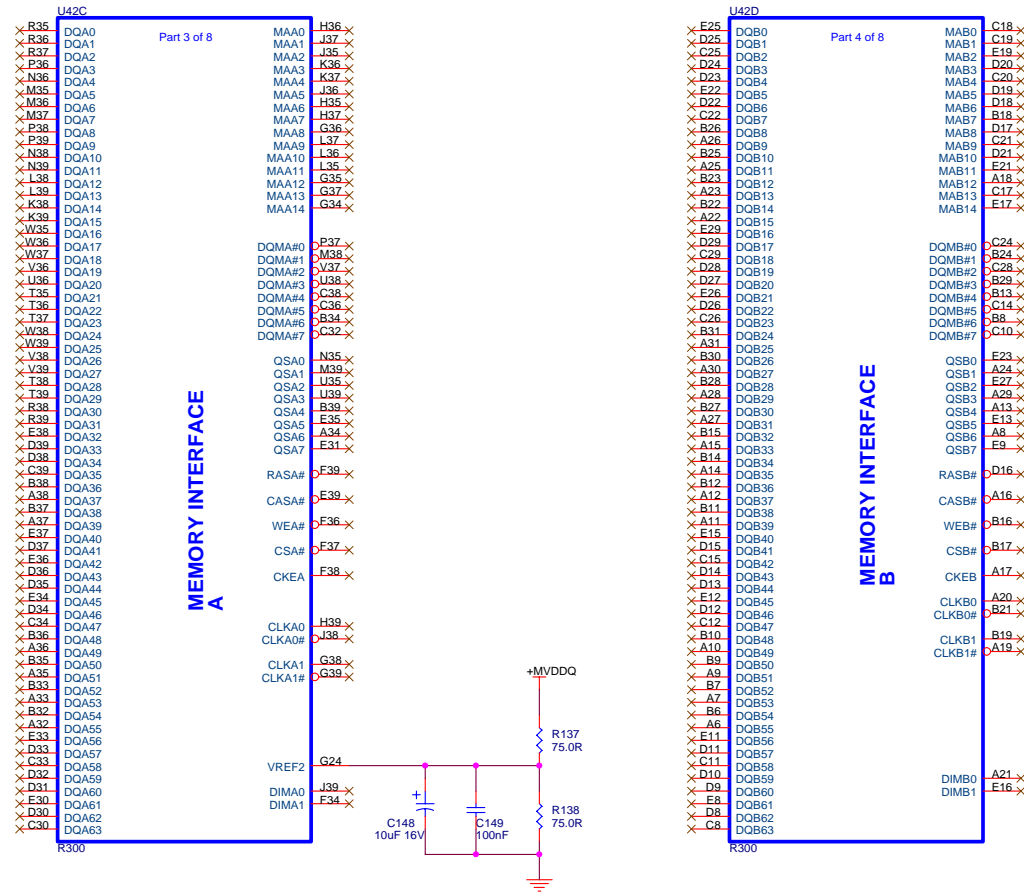


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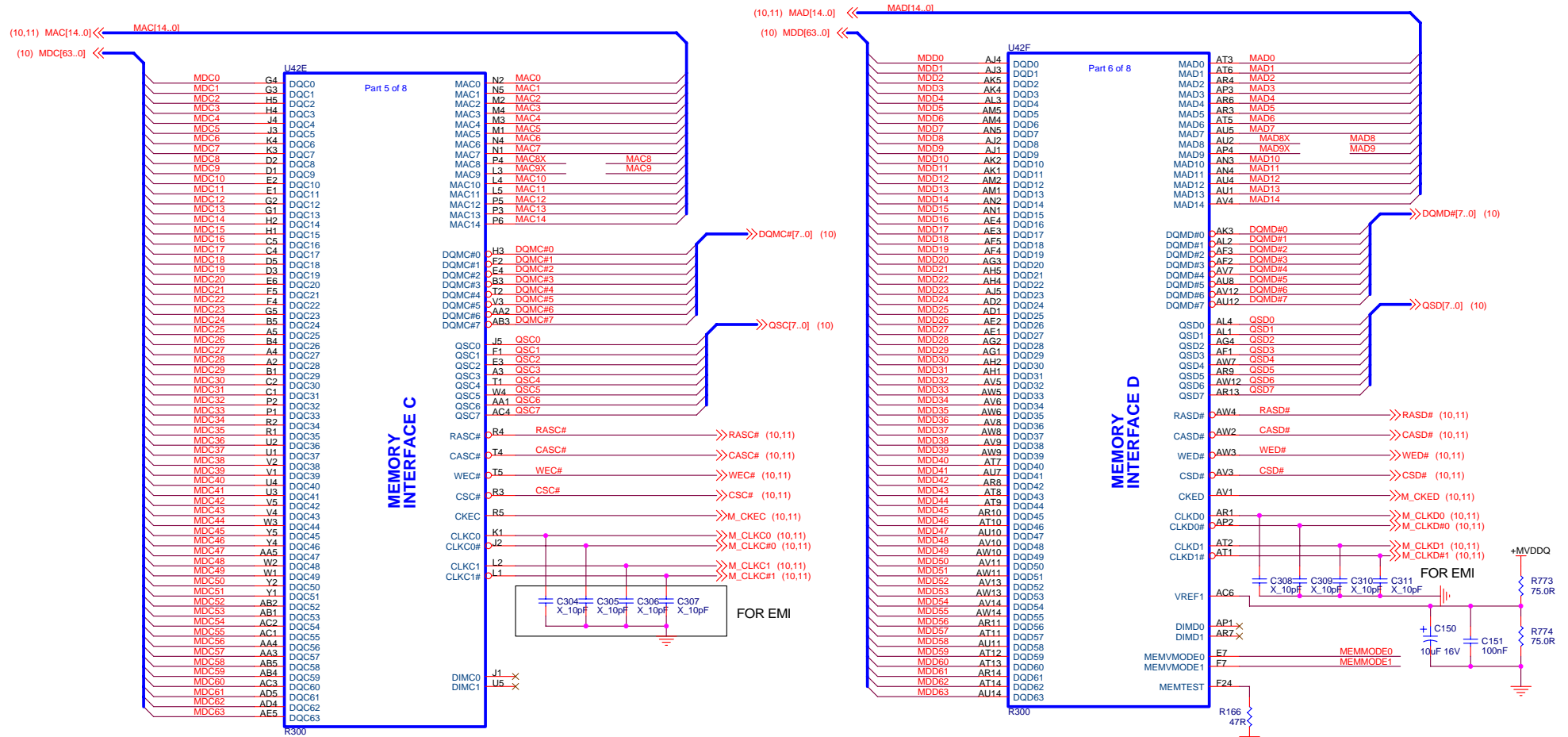
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Custom		0A
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POWER REGULATOR 2

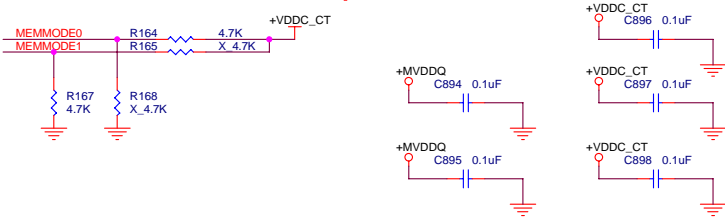
# R-300 MEMORY CHANNELS A and B

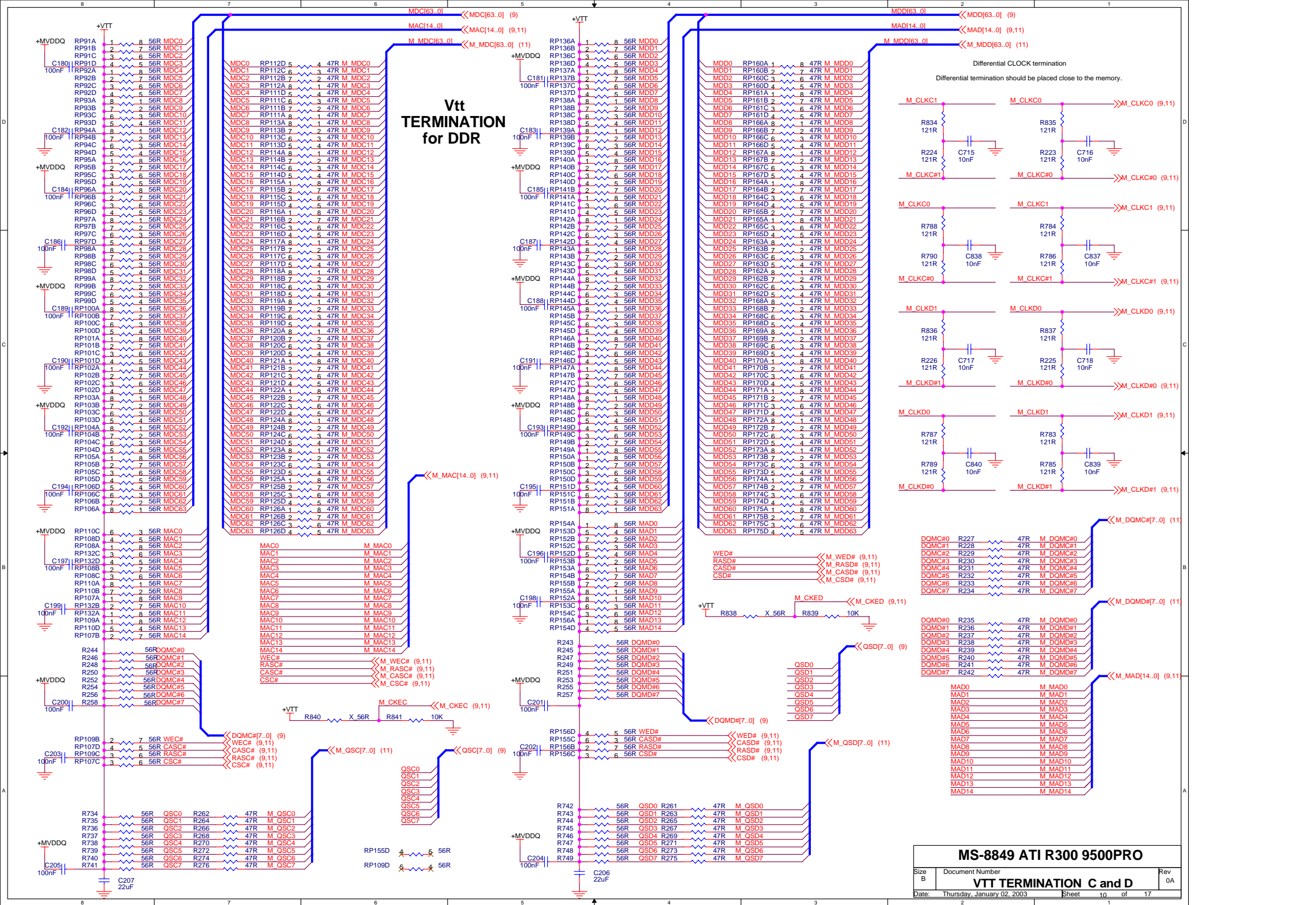


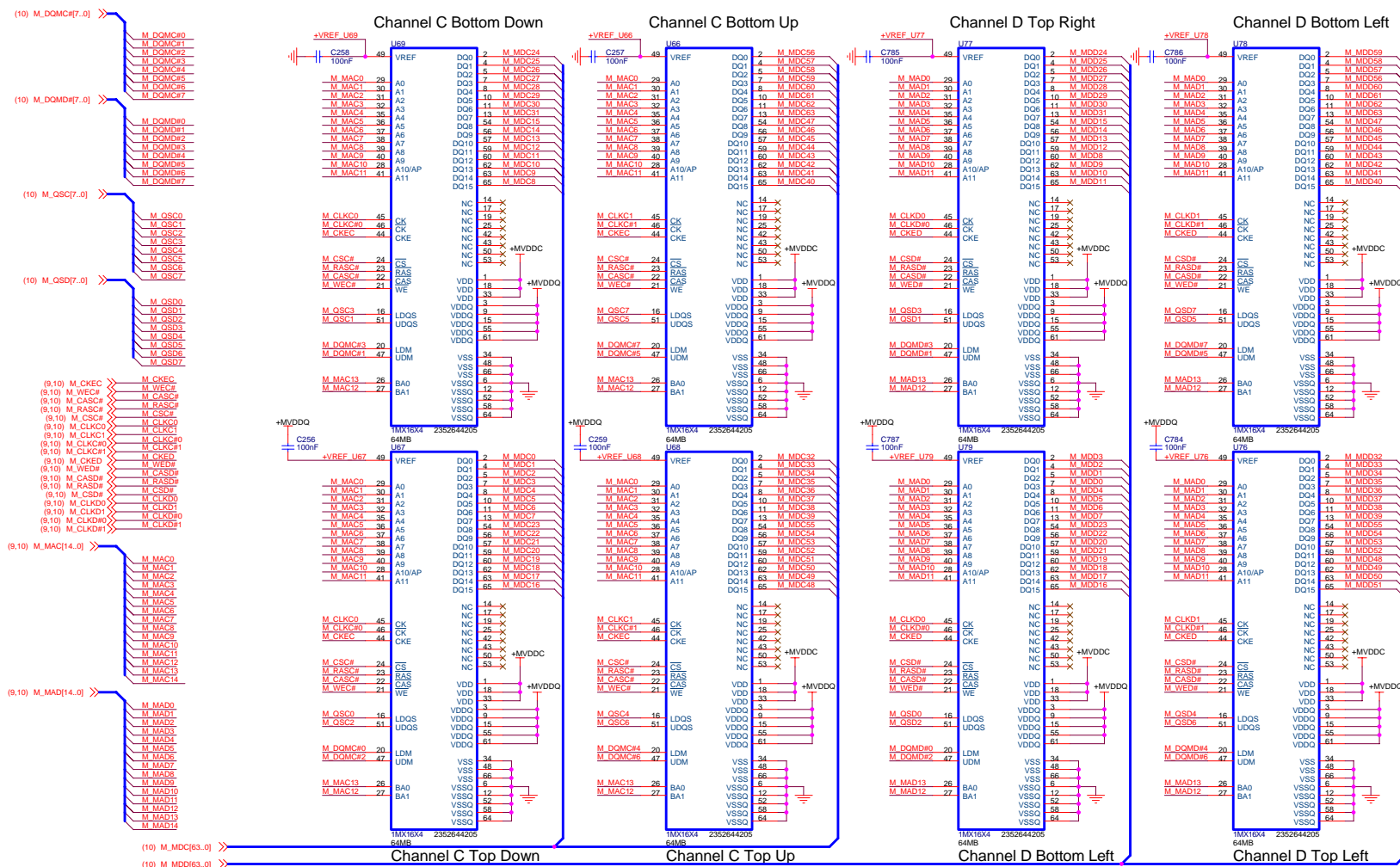
R-300  
MEMORY CHANNELS C and D



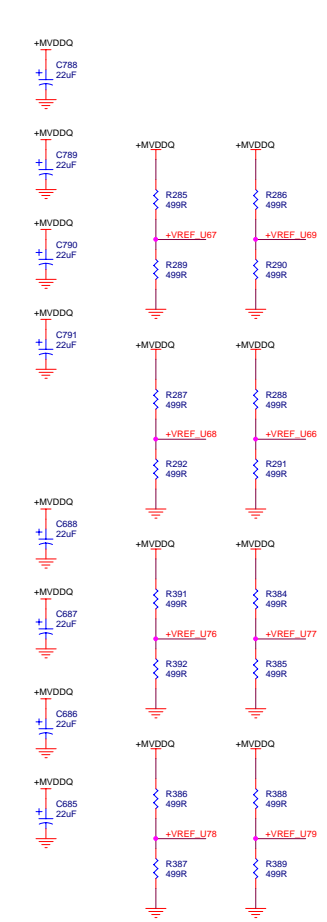
MEMVMODE[1:0]	MEMORY IO VOLTAGE
0 1	2.5V (DDR)
1 0	1.8V (DDR)
1 1	3.3V (SDR)



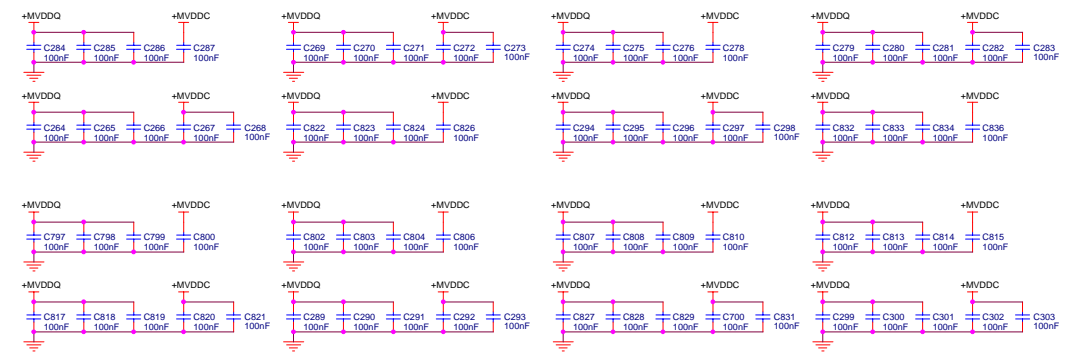




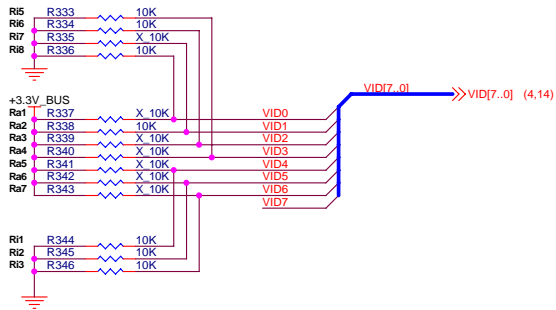
TSOP 8MX16 DDR



Note: These indications of the location of the memory for the solder side (bottom) are looking thru from the component side.



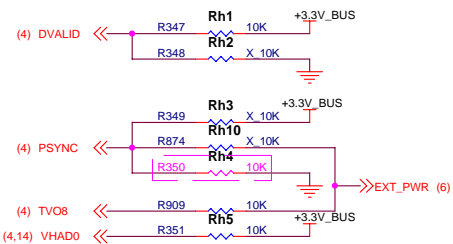
STRAPPING



AGPFBSKEW -- VID(1:0)				
Ra2	Ra1	Ri7	Ri8	
DNI	DNI	10K	10K	refclk slightly earlier than feedback (00)
DNI	10K	10K	DNI	refclk 1 tap later than feedback (01)
10K	DNI	DNI	10K	refclk 1 tap later than feedback DEFAULT (10)
10K	10K	DNI	DNI	refclk 2 taps earlier than feedback (11)

X0CLK_SKEW --VID(3:2)				
Ra4	Ra3	Ri5	Ri6	
DNI	DNI	10K	10K	x0clk to agpcik 0 tap delay DEFAULT
DNI	10K	10K	DNI	x0clk to agpcik 1 tap delay
10K	DNI	DNI	10K	x0clk to agpcik 2 taps delay
10K	10K	DNI	DNI	x0clk to agpcik 3 taps delay

BUSCFG -- VID(6:4)							
BUSTYPE_2 VID6		BUSTYPE_1 VID5		BUSTYPE_0 VID4			
Ra7	Ri3	Ra6	Ri2	Ra5	Ri1	AGP8X_DET = 0 (both GC and MB 8x capable)	
						DESCRIPTION	
DNI	10K	DNI	10K	DNI	10K	AGP 8X, 0.8V signaling PLL CLK, IDSEL = AD16	
DNI	10K	DNI	10K	10K	DNI	AGP 8X, 0.8V signaling PLL CLK, IDSEL = AD17	
DNI	10K	10K	DNI	10K	DNI	AGP 4X, 0.8V signaling PLL CLK, IDSEL = AD16	
DNI	10K	10K	DNI	10K	DNI	AGP 4X, 0.8V signaling PLL CLK, IDSEL = AD17	
						AGP8X_DET = 1 (either GC or MB not 8x capable)	
DNI	10K	DNI	10K	DNI	10K	AGP 4X, PLL CLK, IDSEL = AD16	
DNI	10K	DNI	10K	10K	DNI	AGP 4X, PLL CLK, IDSEL = AD17	
DNI	10K	10K	DNI	DNI	10K	AGP 1X/2X, PLL CLK, IDSEL = AD16	
DNI	10K	10K	DNI	DNI	10K	AGP 1X/2X, PLL CLK, IDSEL = AD17	
10K	DNI	DNI	10K	DNI	10K	PCI 66MHz, PLL CLK	
10K	DNI	DNI	10K	DNI	10K	PCI 33MHz, 3.3V, REF CLK	
10K	DNI	10K	DNI	DNI	10K	AGP 1X, REF CLK, IDSEL = AD16	
10K	DNI	10K	DNI	10K	DNI	AGP 1X, REF CLK, IDSEL = AD17	

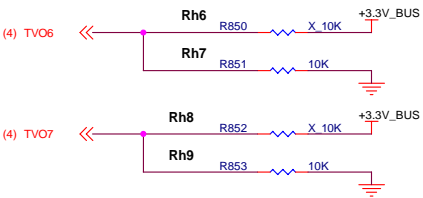


INSTALL	DEVICE ID
Rh1	NORMAL ID (default) Install it all the time when it is normal device ID
Rh2	Use workstation DEVICE_ID when WSEN = 1

INSTALL	DNI	ID_DISABLE
Rh4	Rh10	Normal operation
Rh3	Rh10	CHIP SHUTS DOWN
Rh10	Rh3 Rh4	Circuitry for external power detection. (DEFAULT)

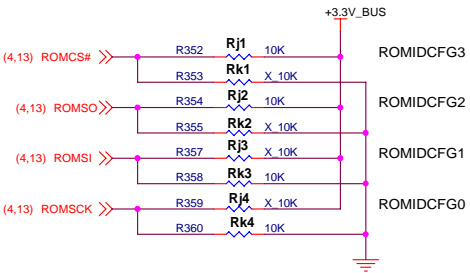
INSTALL	VIP DEVICE
Rh5	NO SLAVE VIP (DEFAULT) Install it when internal pull-up doesn't work
	SLAVE VIP --- VIP device will drive low when VIP is attached.

MEMORY TYPE STRAPS



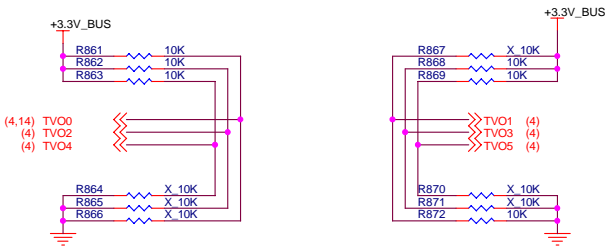
	TVO7	TVO6
SAM	0	0
INF	1	0
HYN	0	1
TBD	1	1

ST M25P05



Rj1	Rk1	Rj2	Rk2	Rj3	Rk3	Rj4	Rk4	ROMIDCFG[3:0]
DNI	10K	DNI	10K	DNI	10K	DNI	10K	No ROM, CHG ID = 00
DNI	10K	DNI	10K	10K	DNI	DNI	10K	No ROM, CHG ID = 01
DNI	10K	10K	DNI	DNI	10K	DNI	10K	No ROM, CHG ID = 10
DNI	10K	10K	DNI	10K	DNI	DNI	10K	No ROM, CHG ID = 11
10K	DNI	DNI	10K	DNI	10K	DNI	10K	Parallel ROM on TVO (default)
10K	DNI	DNI	10K	DNI	10K	10K	DNI	Serial AT25F1024, ID's from ROM
10K	DNI	DNI	10K	10K	DNI	DNI	10K	Serial AT45DB011, ID's from ROM
10K	DNI	DNI	10K	DNI	DNI	DNI	10K	Serial ST M25P10, ID's from ROM
10K	DNI	10K	DNI	DNI	10K	DNI	10K	Serial ST M25P05, ID's from ROM
10K	DNI	10K	DNI	DNI	10K	DNI	10K	Serial SST45LF010, ID's from ROM
10K	DNI	10K	DNI	10K	DNI	DNI	10K	Parallel ROM on DVO
10K	DNI	10K	DNI	10K	DNI	10K	DNI	Serial ISSI NX25F011B, ID's from ROM

TVO Straps



TVO1	
0	PAL
1	NTSC

TVO2	
0	YPrPb
1	SVHS/CVBS

TVO4	TMDS
0	NO
1	YES

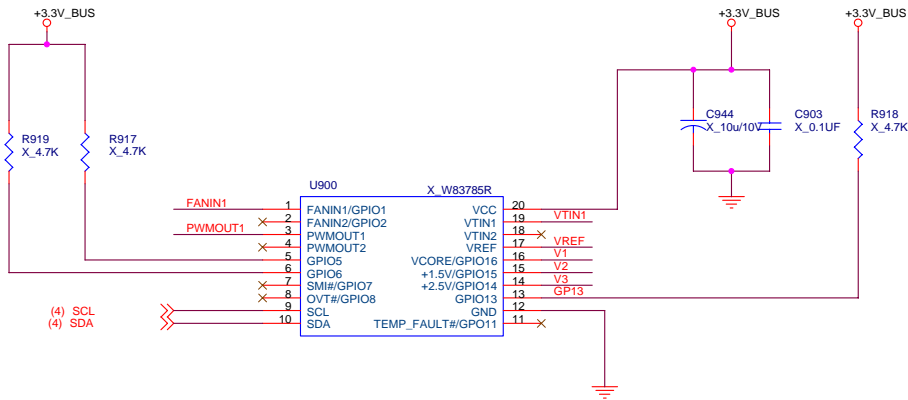
TVO0	TVO3	DAC2
0	0	OFF
0	1	TV-OUT
1	0	CRT
1	1	BOTH

TVO5	
0	NO VIDEO CAPATURE
1	RAGE THEATER 1 OR 2

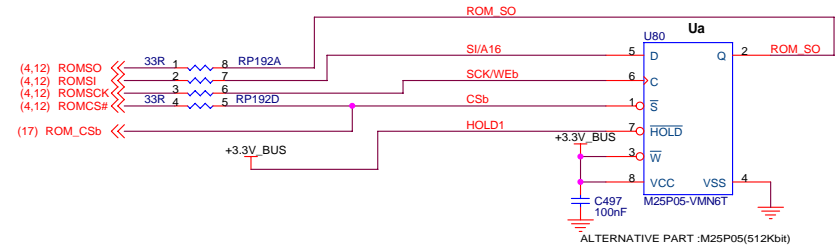
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B	STRAPPING	0A
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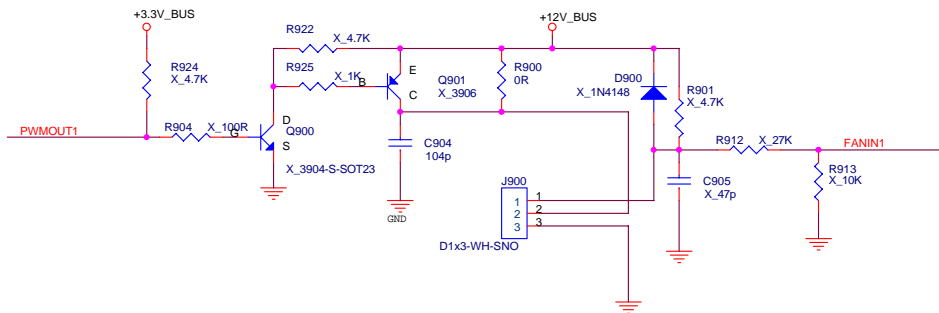
## HARDWARE MONITOR



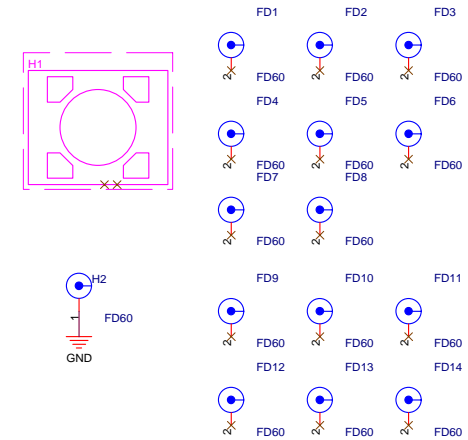
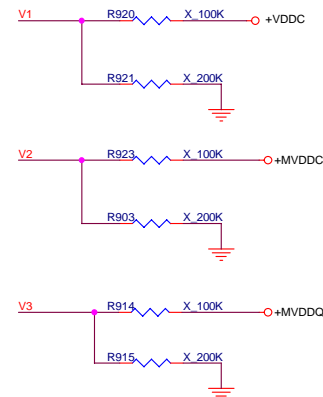
## SERIAL EEPROM 512K/1M



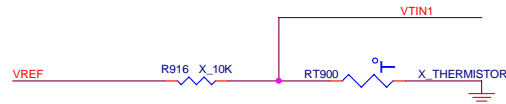
## FAN SPEED CONTROL



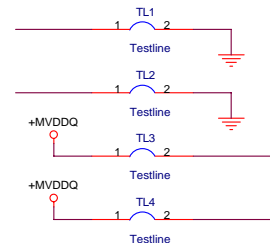
## VOLTAGE SENSING CIRCUIT



## TEMPERATURE SENSING CIRCUIT



## Impedence Test Line

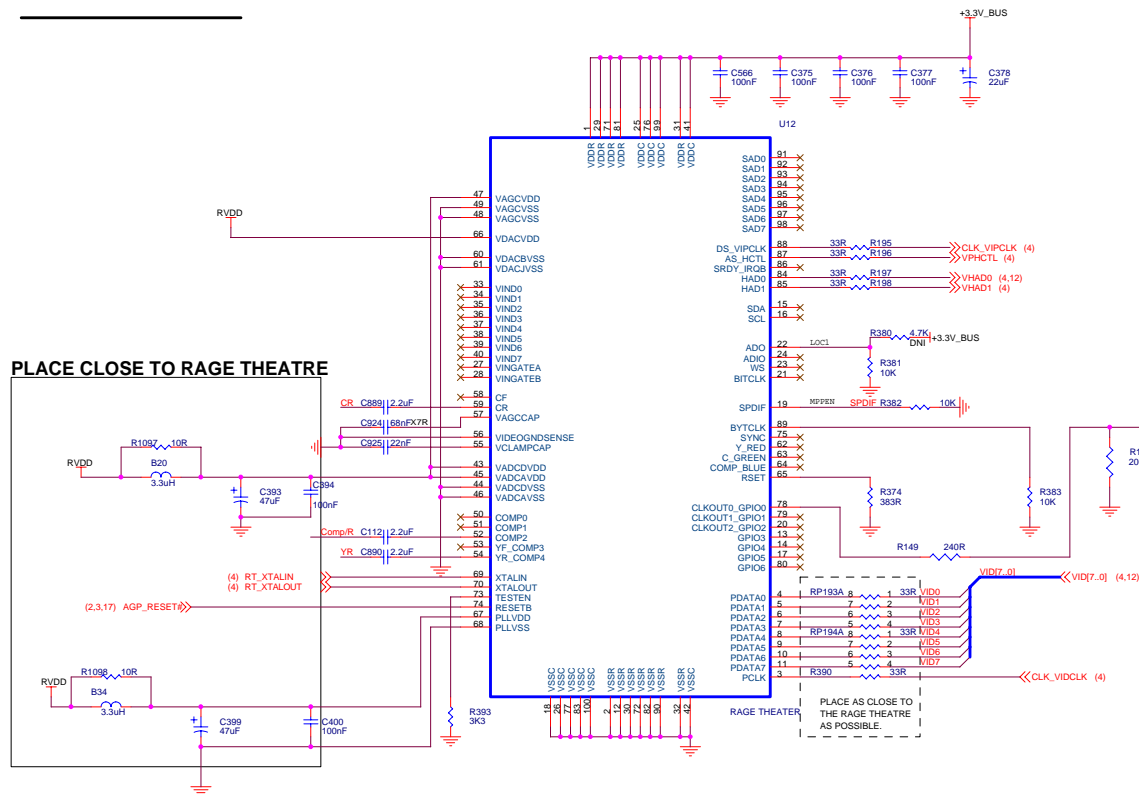


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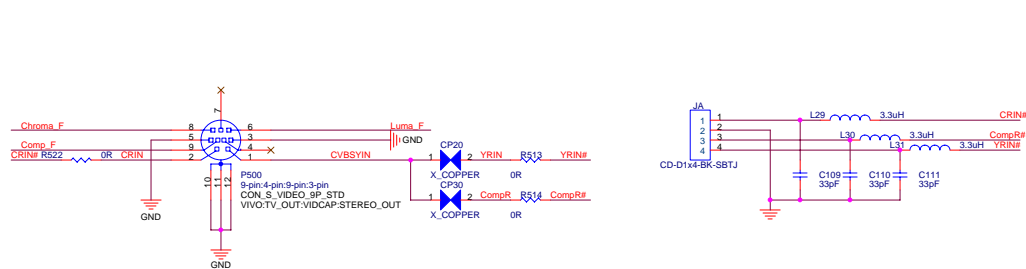
Size B	Document Number	Rev 0A
FAN SPEED CONTROL / BIOS		
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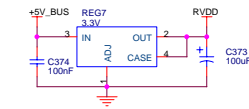
## THEATER & TV-OUT



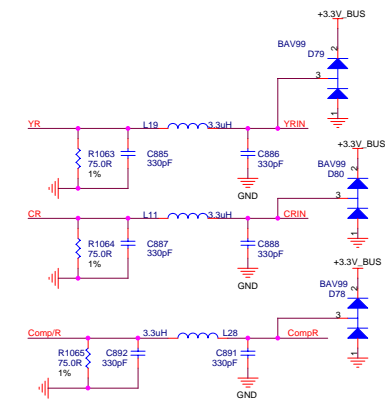
## VIVO CONNECTOR



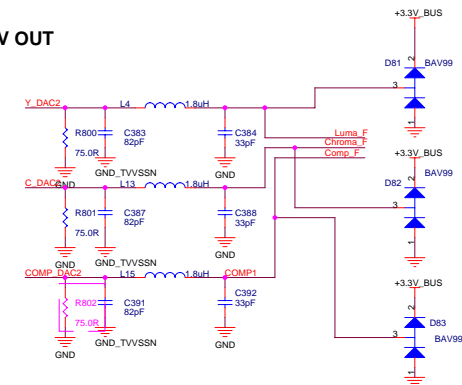
### Regulator for RVDD



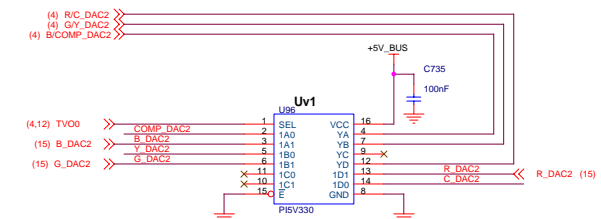
## VIDEO IN



## TV OUT

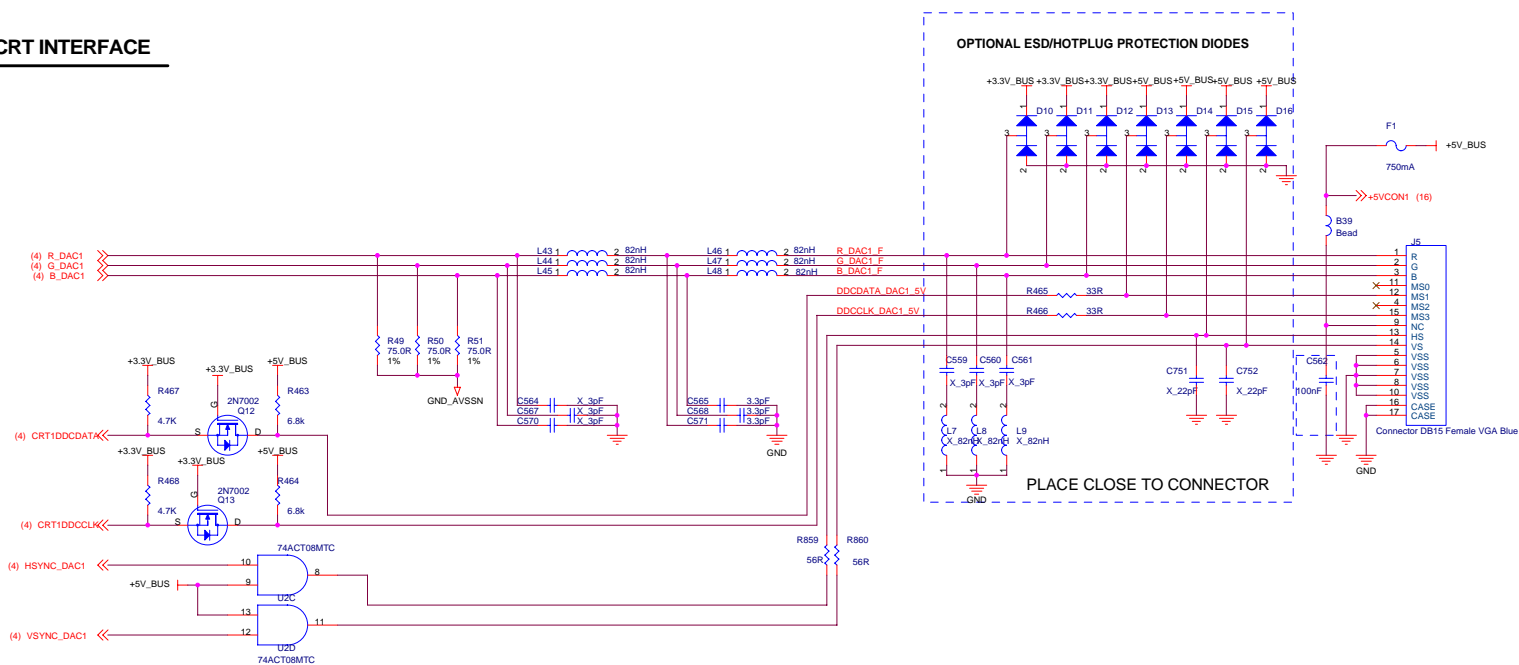


## DEMUX

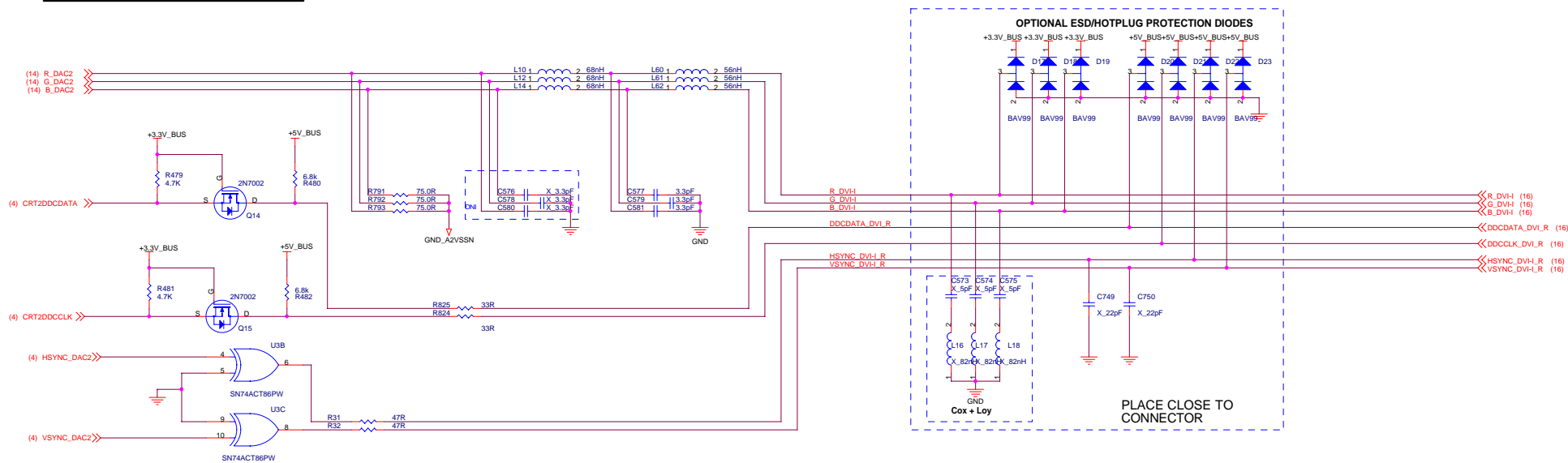




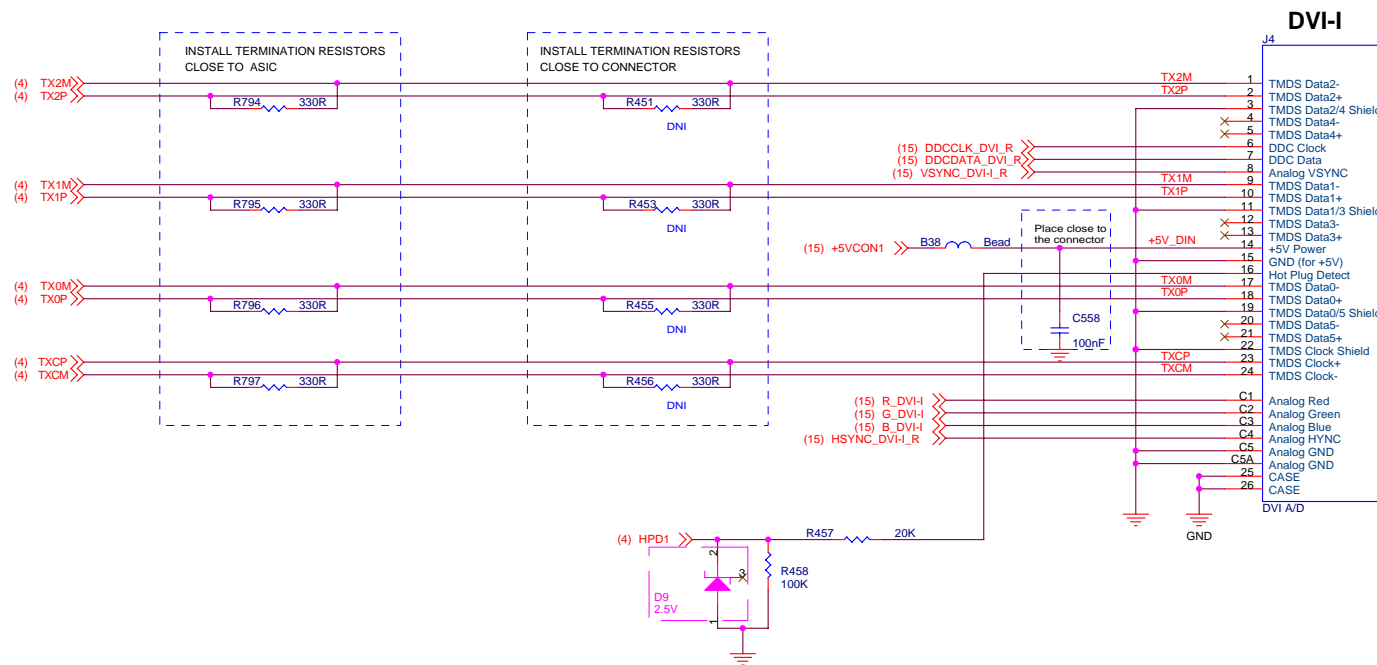
## PRIMARY CRT INTERFACE



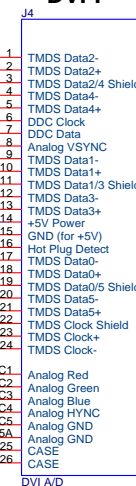
## SECONDARY CRT INTERFACE



# PRIMARY DVI-I CONNECTOR (DVI-I)



## DVI-I



# Hijack Circuit

