

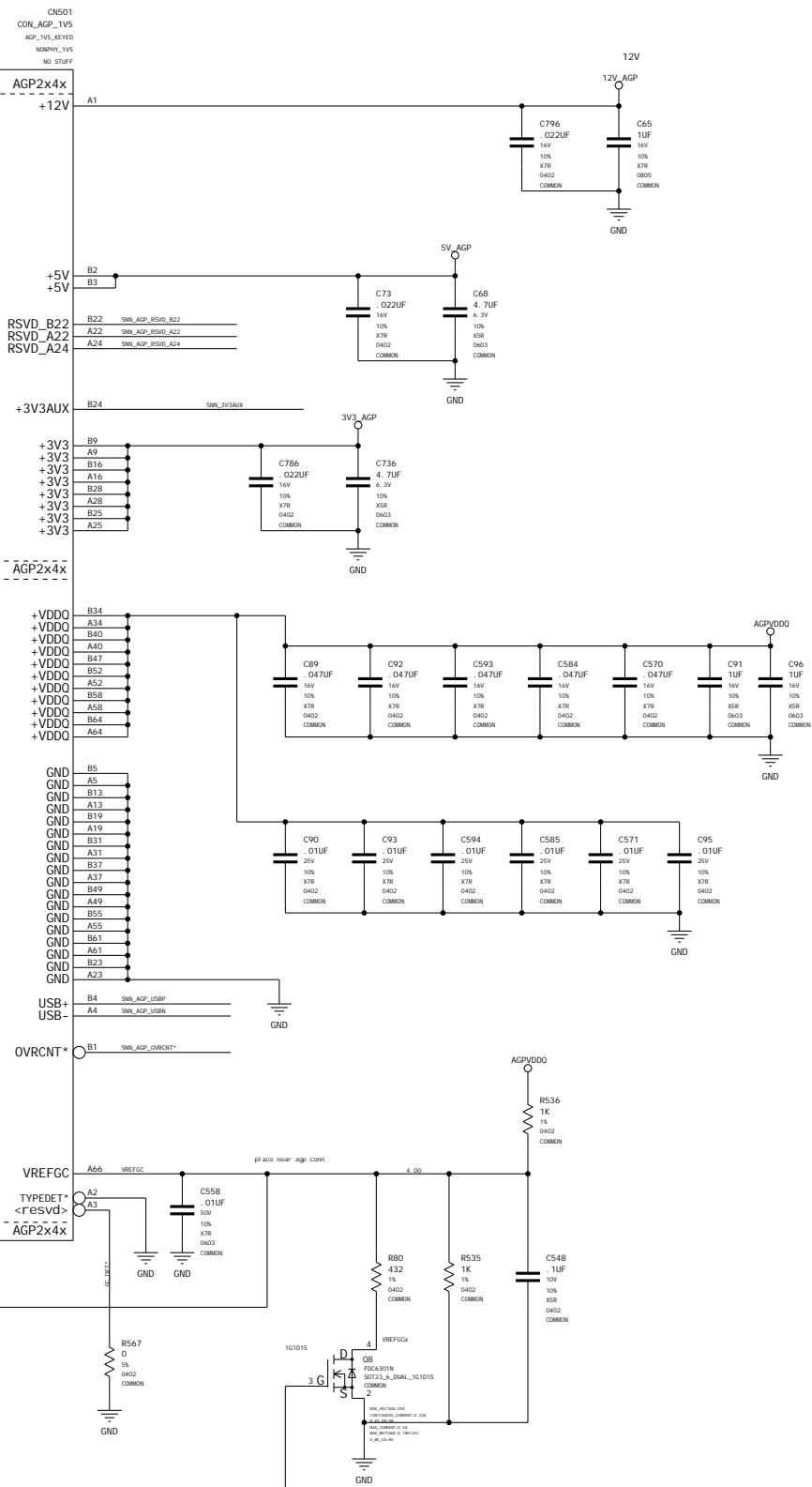
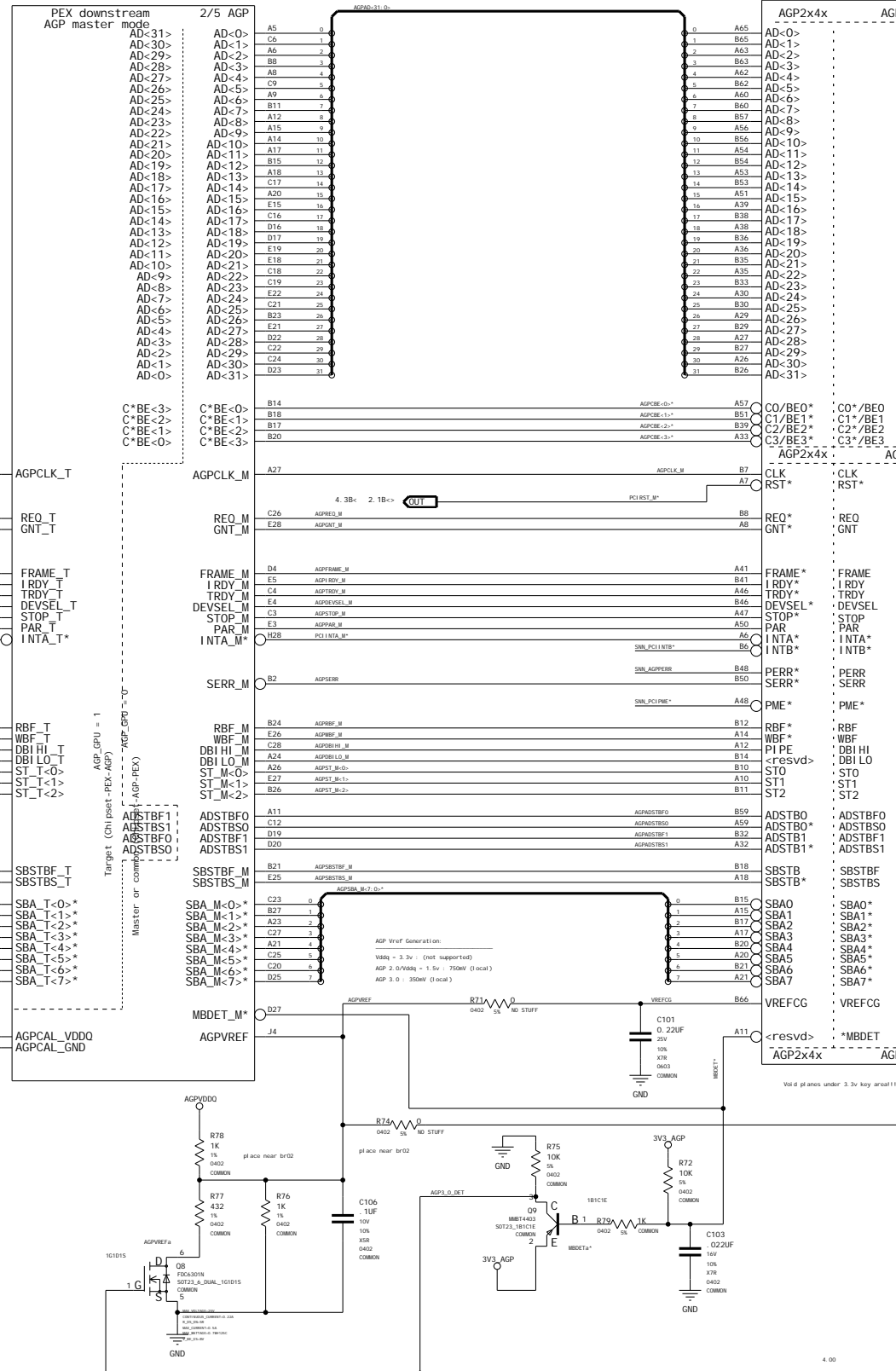
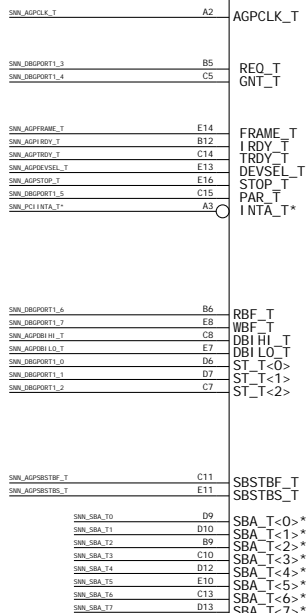
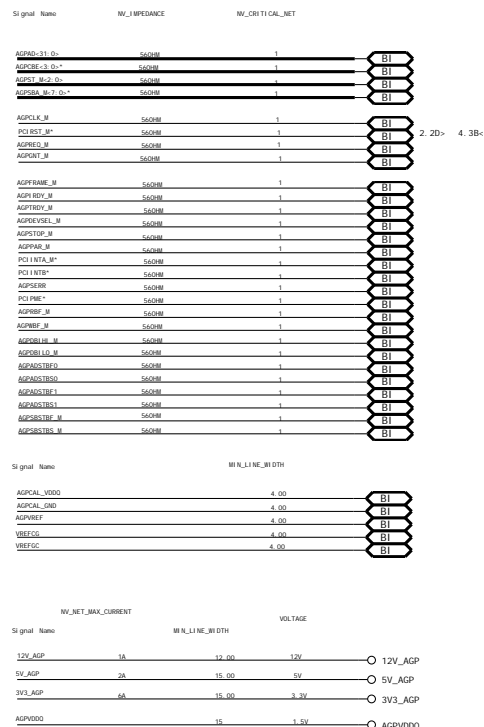
P508-A00 DESIGN - G73+BR02 AGP 256MB/128MB DDR2 Board

PAGE SUMMARY:

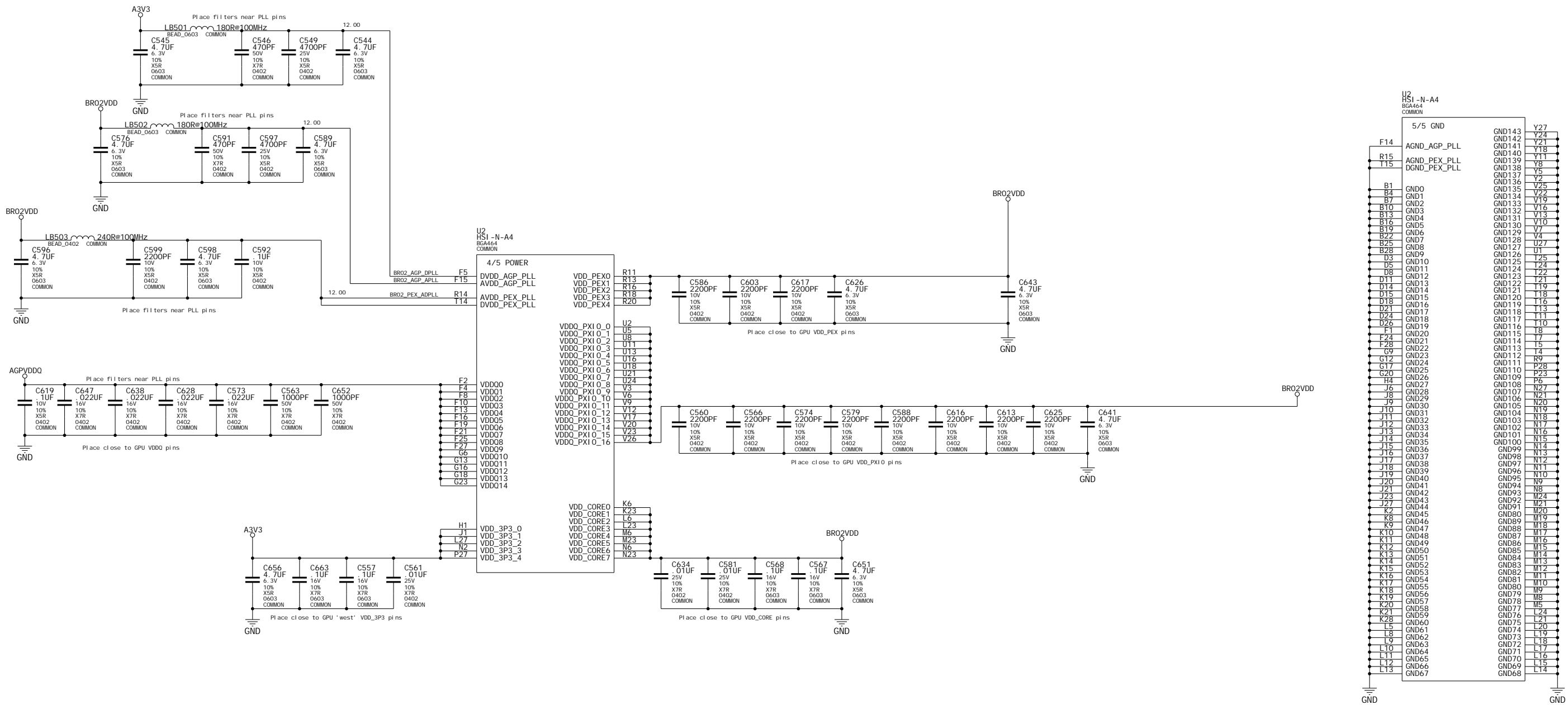
- Page1 : Page Summary and Revision History
- Page2 : AGP to BR02 Interface
- Page3 : BR02 PWR/GND/De-Coupling
- Page4 : BR02 JTAG / Straps / Misc.
- Page5 : BR02 PCI Express
- Page6 : G73 PCI Express Interface
- Page7 : GPU Frame Buffer A Interface
- Page8 : MEMORY 1st bank 0..31
- Page9 : MEMORY 1st bank 32..63
- Page10: GPU Frame Buffer C Interface
- Page11: MEMORY 2nd bank 0..31
- Page12: MEMORY 2nd bank 32..63
- Page13: Primary Display (DACA), Slim DB15
- Page14: Secondary Display (DACC), DB15
- Page15: INTERNAL TMDS .. LINK A,B SOUTH
- Page16: INTERNAL TMDS .. LINK C,D NO USE
- Page17: GPU-MIOB, MIOA
- Page18: DACB .. MiniDIN VIDEO IN/OUT CONNECTOR
- Page19: XTAL and GPU's GND
- Page20: GPIO, JTAG, BIOS, FAN CONTROL, EXTSENSE
- Page21: Straps & Mechanical
- Page22: Ext Power CON & SENCE Ckt, DDC5V, TMDSIOVDD, A3V3
- Page23: FBVDD/Q and BR02VDD, PEX1V2
- Page24: NVVDD (NVVDD and PEXVDD), A2V5

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10508-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	602-10508-0000-000	G73+BR02 AGP, 16Mx16 DDRII, 256MB/128-bit VGA + DVI-I + HDTV
2	SKU0001	602-10508-0001-000	G73-V+BR02 AGP, 16Mx16 DDRII, 256MB/128-bit VGA + DVI-I + HDTV
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4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

## 2. AGP to BR02 Interface



BRO2 PWR/GND/De-Coupl i ng



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BRO2 PWM/GND/De-Coupling

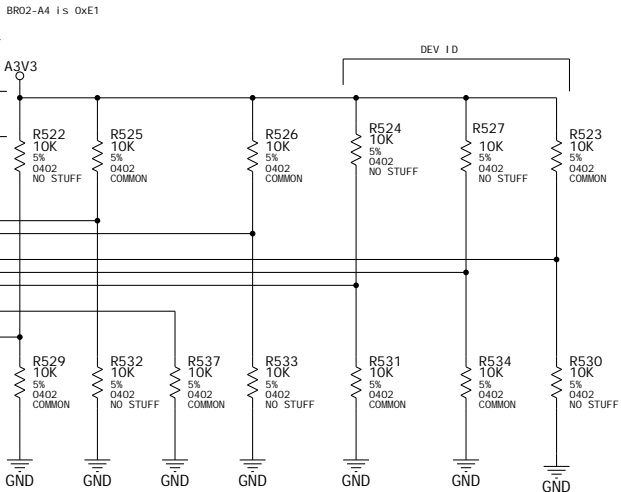
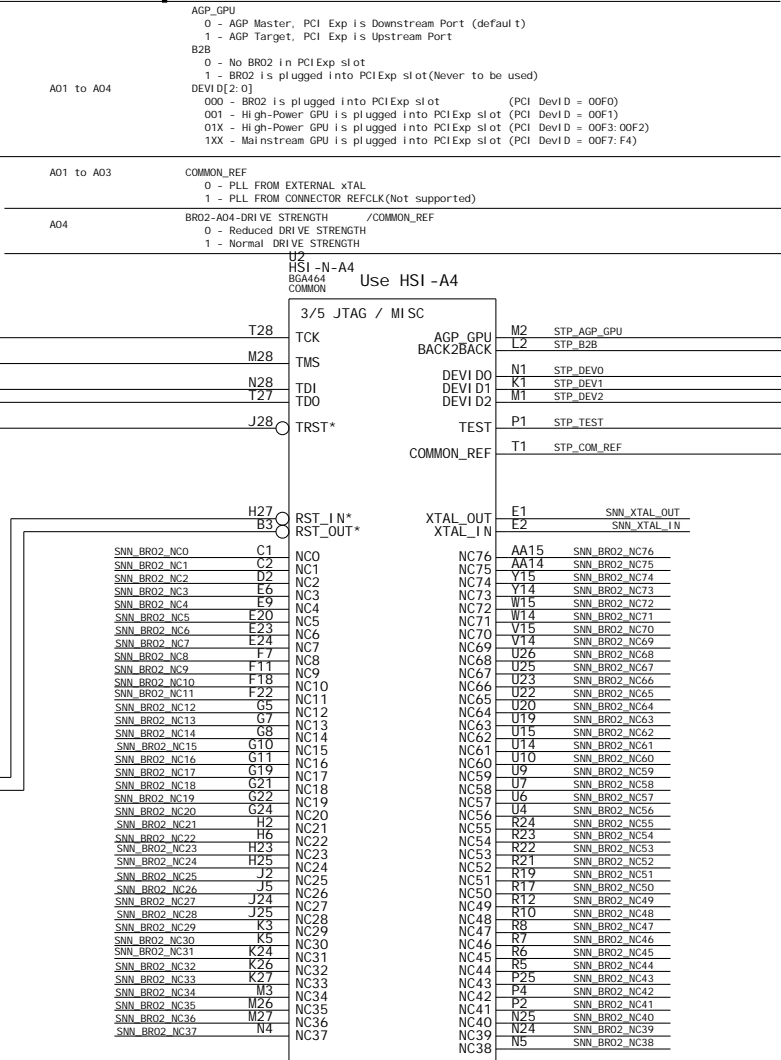
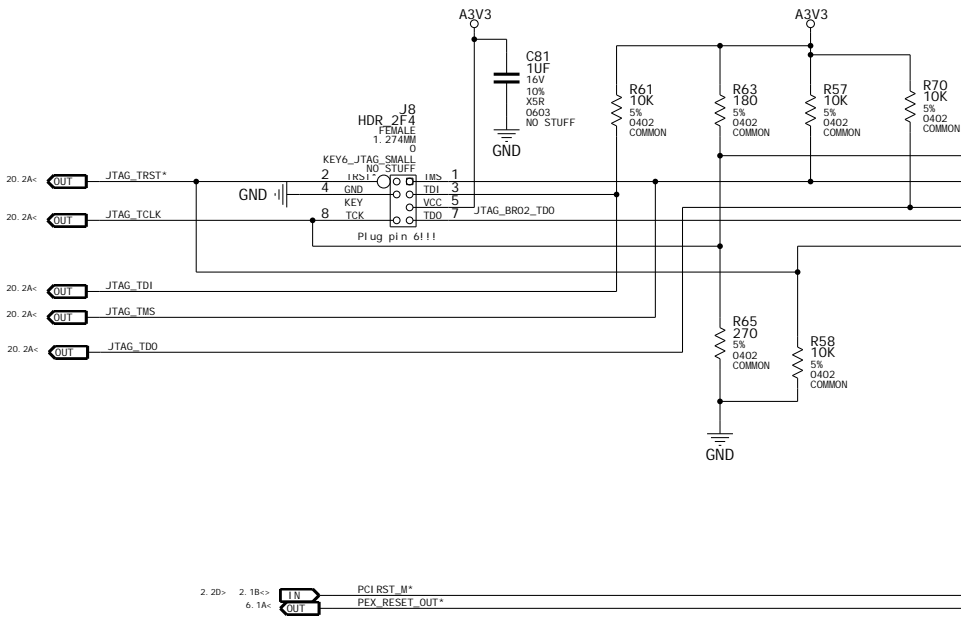
NV\_PN 602-10508-0000-000

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NAME	dhao	DATE	10-FEB-2006

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BR02 JTAG / Straps / Misc.

Straps:



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ID dest gn PAGE 4 OF 24  
NAME dhao DATE 10-FEB-2006

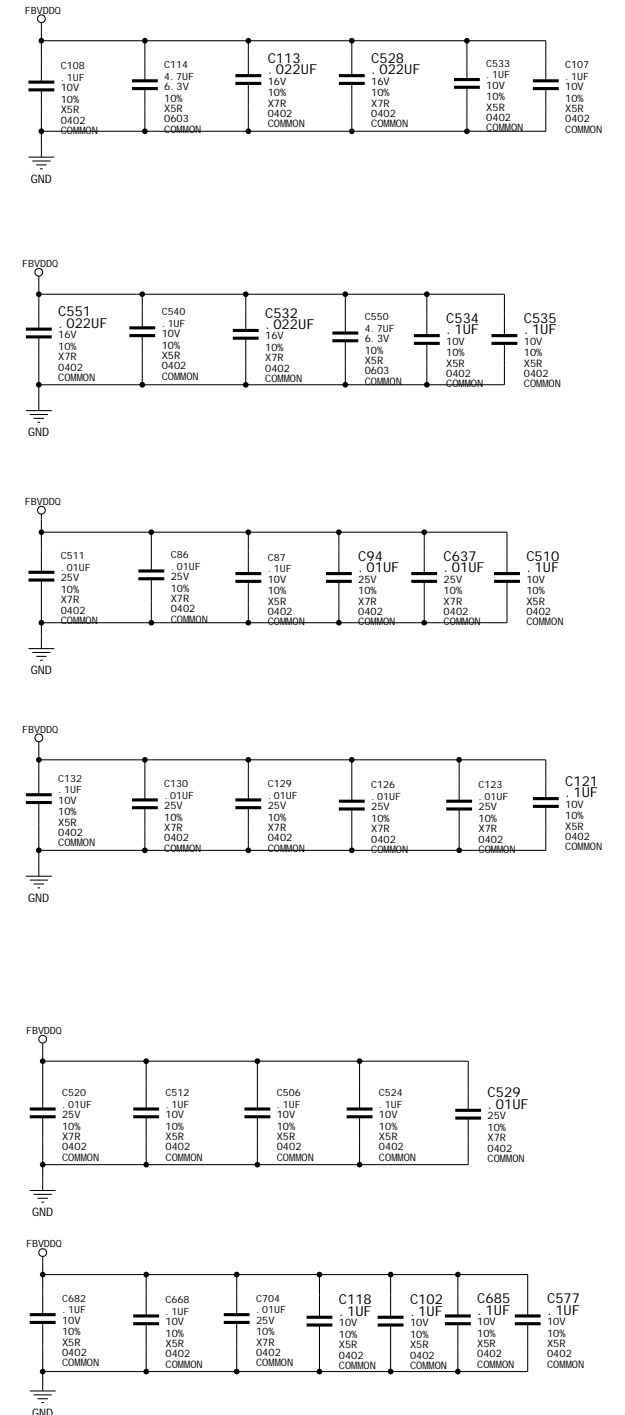
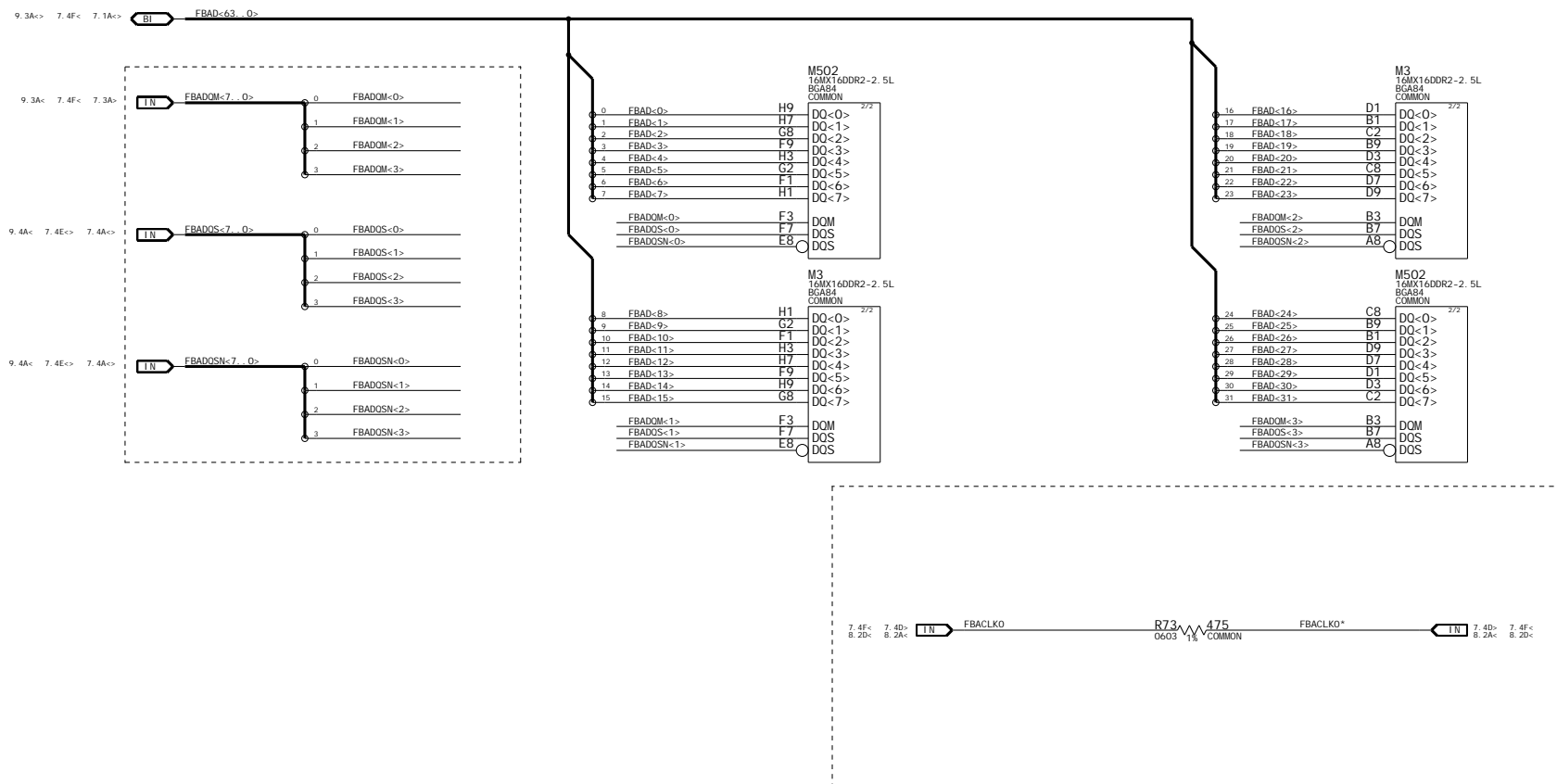
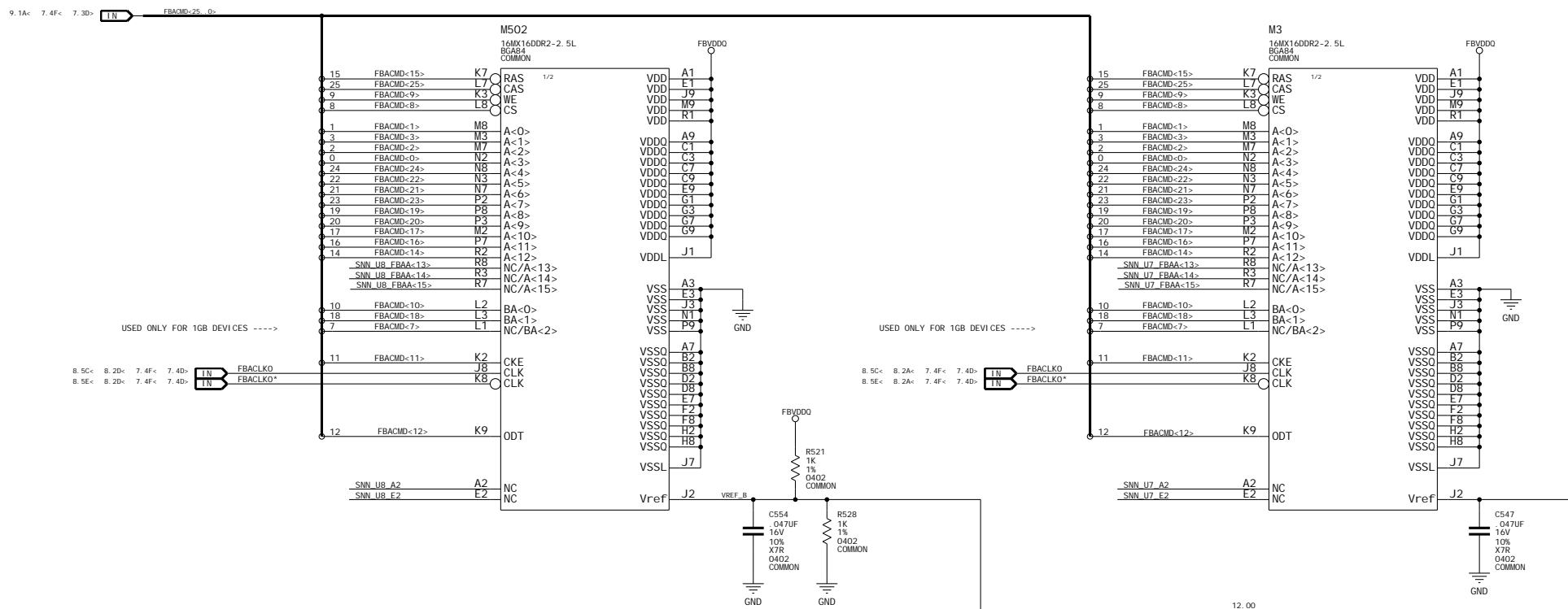
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2

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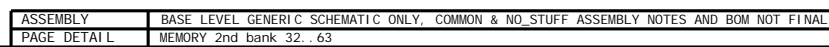
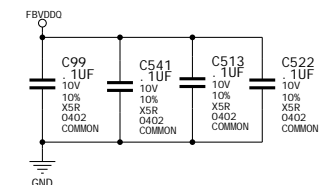
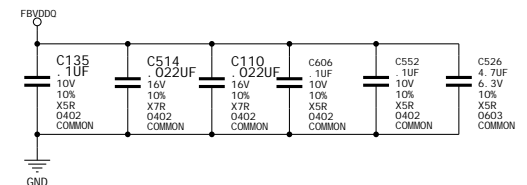
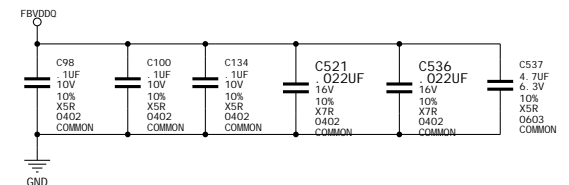



PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY





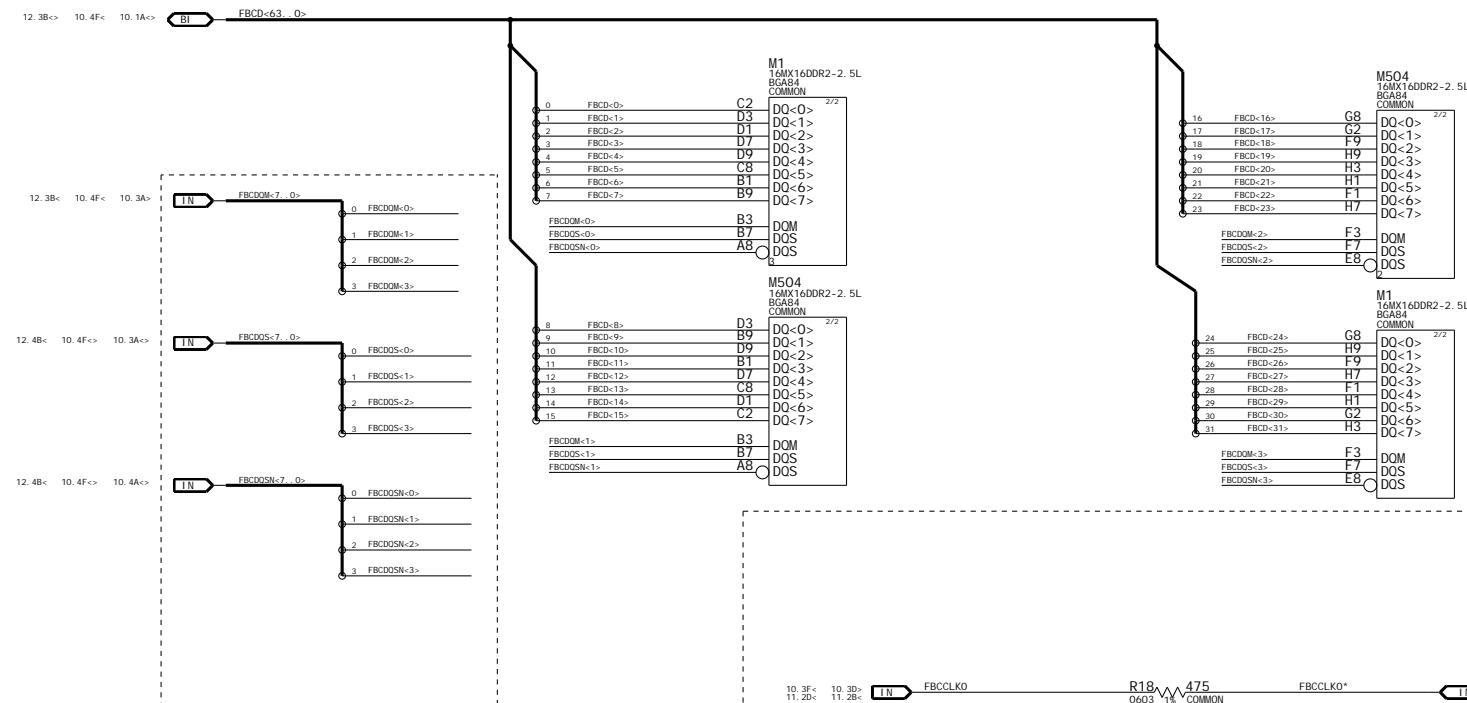
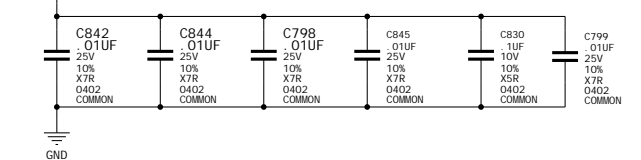
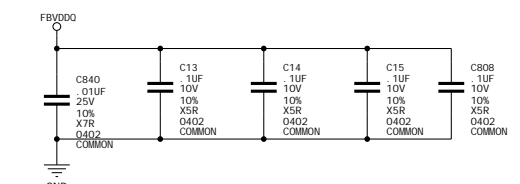
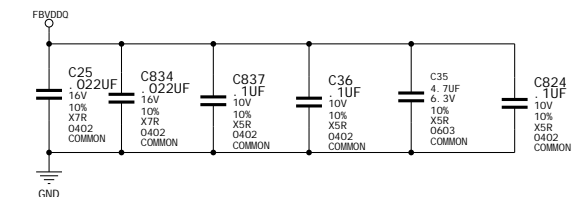
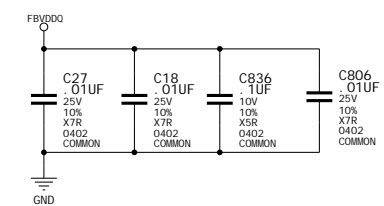
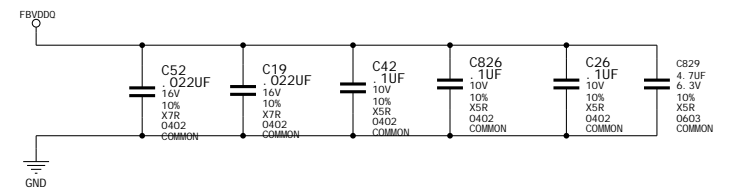
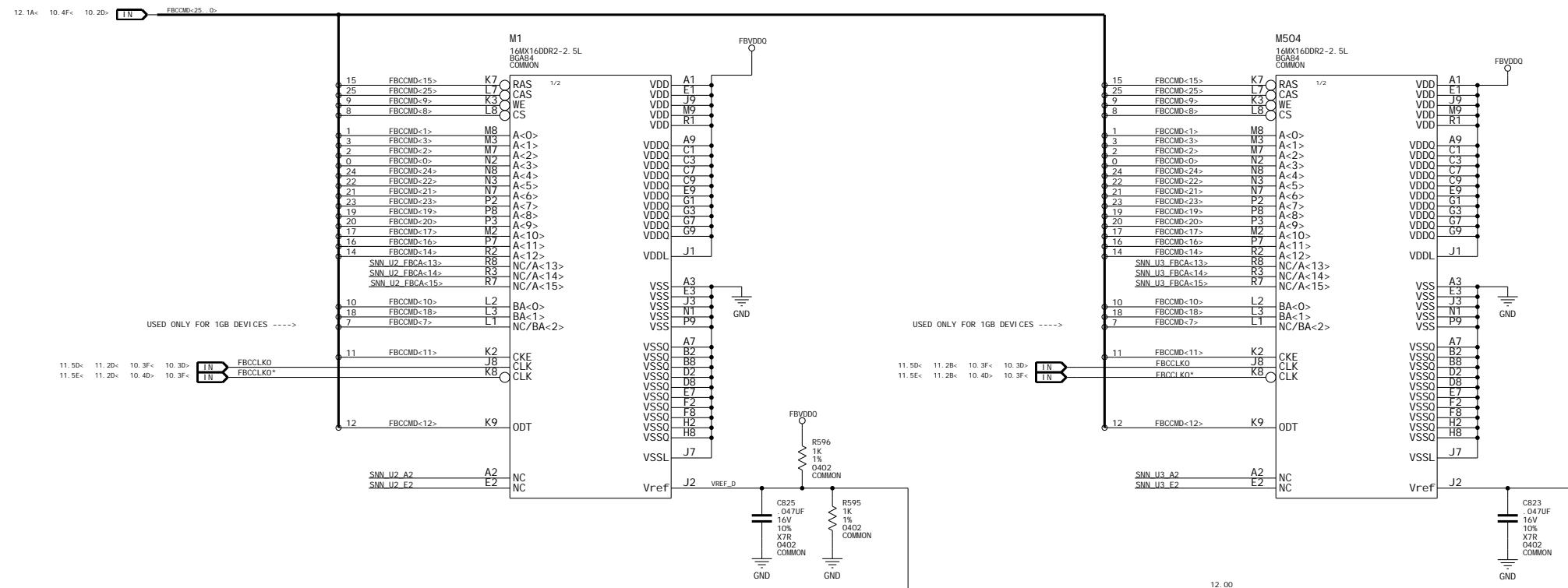
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<b>NV_PN</b>		<b>602-10508-0000-000</b>		
<b>ID</b>	<b>dest gn</b>	<b>PAGE</b>	<b>9 OF 24</b>	
<b>NAME</b>	<b>dhao</b>	<b>DATE</b>	<b>10-FEB-2006</b>	



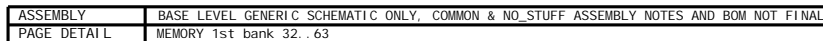
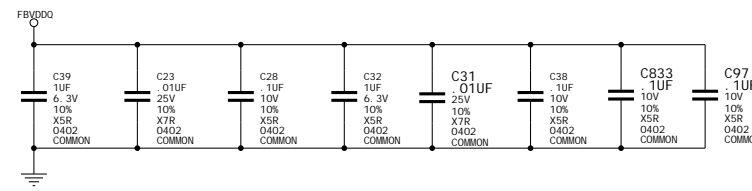
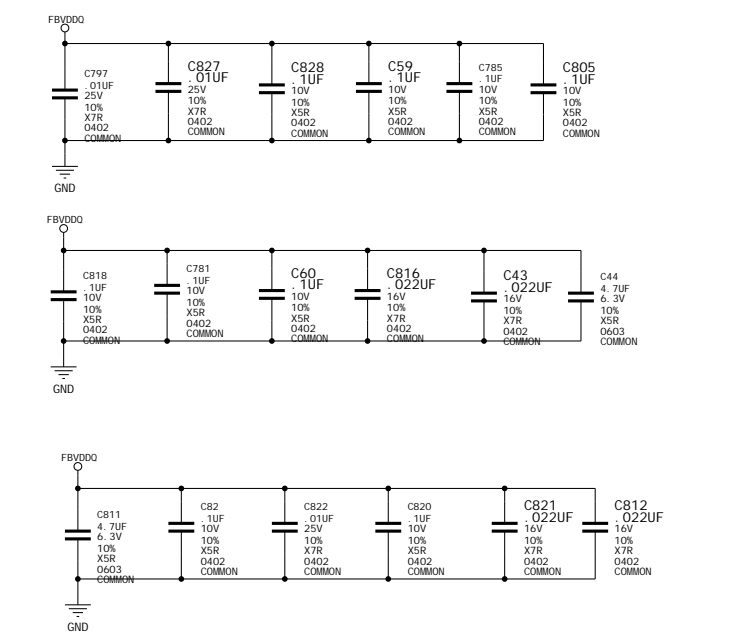
FBC MEMORY 2nd bank 0..31  
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY




ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY 2nd bank 0..31

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PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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# DACA NET RULES

NET NV\_CRI TICAL NV\_I MPEDANCE DI FFPAIR

DACA_RED	1	560HM
DACA_GREEN	1	560HM
DACA_BLUE	1	560HM

DACA_RED_C	1	560HM
DACA_GREEN_C	1	560HM
DACA_BLUE_C	1	560HM

DACA_HSYNC	2	500HM
DACA_VSYNC	2	500HM
AVB	2	500HM
AHB	2	500HM
DACA_HSYNC_BUF	2	500HM
DACA_VSYNC_BUF	2	500HM

DACA_HSYNC_C	2	500HM
DACA_VSYNC_C	2	500HM

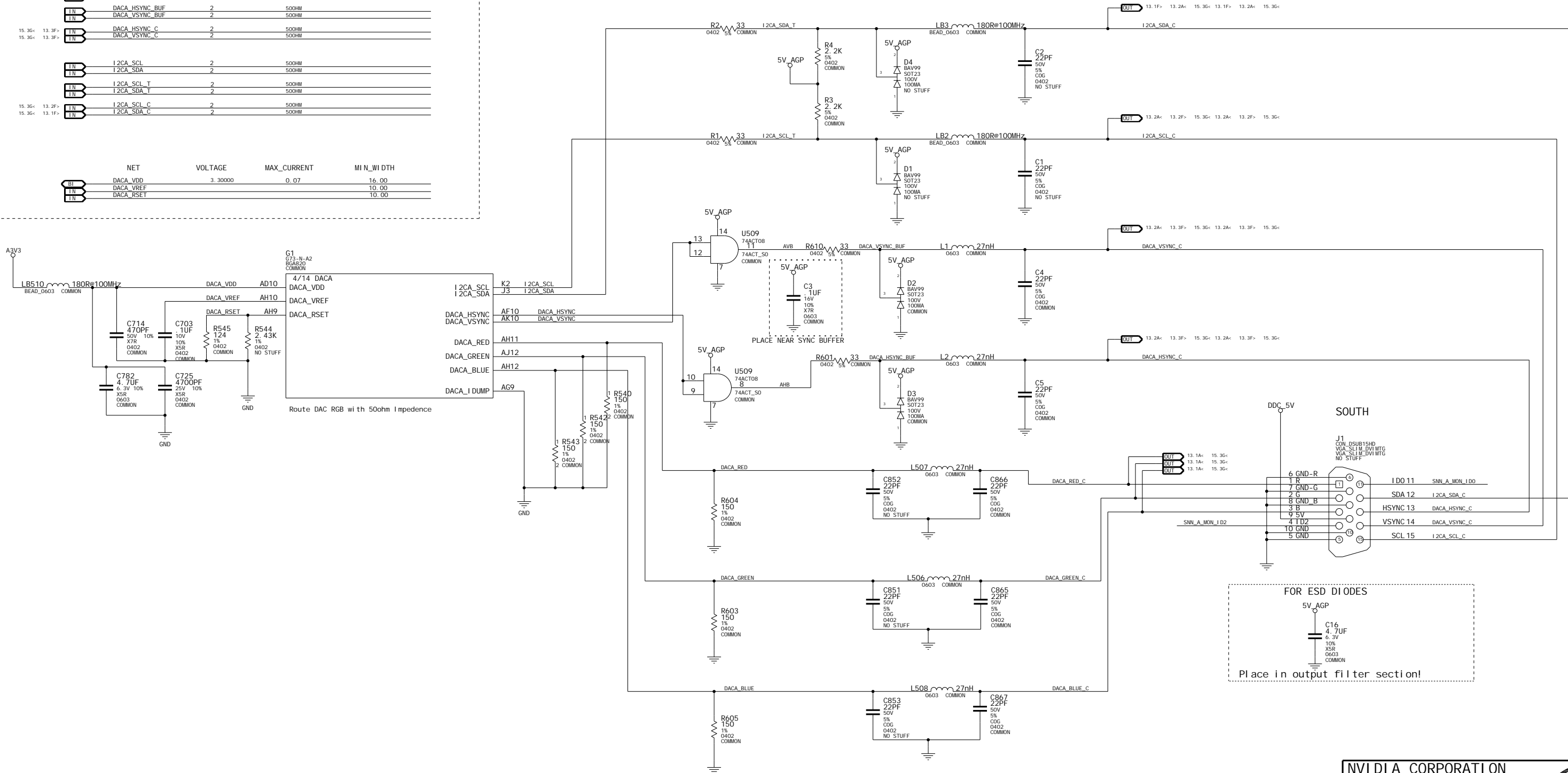
I2CA_SCL	2	500HM
I2CA_SDA	2	500HM
I2CA_SCL_T	2	500HM
I2CA_SDA_T	2	500HM

I2CA_SCL_C	2	500HM
I2CA_SDA_C	2	500HM

NET	VOLTAGE	MAX_CURRENT	MI N_WI DTH
DACA_VDD	3.30000	0.07	16.00
DACA_VREF			10.00
DACA_RSET			10.00

# Primary Display (DACA), Slim DB15

## DACA RGB-FILTER



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Secondary Display (DACC), Slim DB15

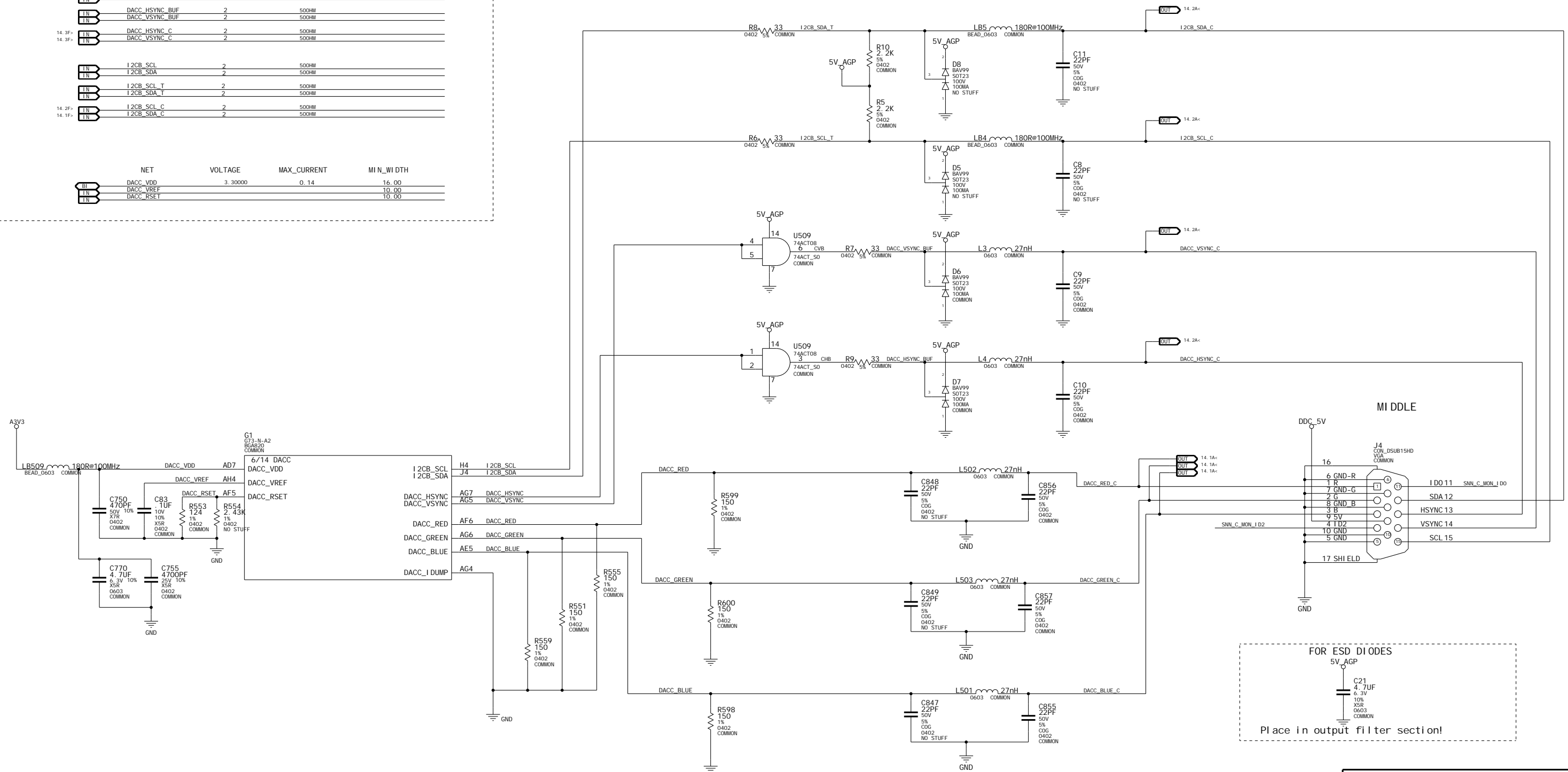
1W	DACC_RED	1	560HM
1W	DACC_GREEN	1	560HM
1W	DACC_BLUE	1	560HM
14 4G+	DACC_RED_C	1	560HM
14 4G+	DACC_GREEN_C	1	560HM
14 4G+	DACC_BLUE_C	1	560HM

14. 3F >	1B	DACC_HSYNC	2	500HM
	1B	DACC_VSYNC	2	500HM
	1B	CVB	2	500HM
	1B	CHB	2	500HM
	1B	DACC_HSYNC_BUF	2	500HM
	1B	DACC_VSYNC_BUF	2	500HM
	1B	DACC_HSYNC_C	2	500HM
	1B	DACC_VSYNC_C	2	500HM

14. 2F>	1N	I2CB_SCL_C	2	500HM
14. 1F>	1N	I2CB_SDA_C	2	500HM

	NET	VOLTAGE	MAX_CURRENT	MIN_WI_DTH
BI	DACC_VDD	3.30000	0.14	16.00
1N	DACC_VREF			10.00
1N	DACC_RST			10.00

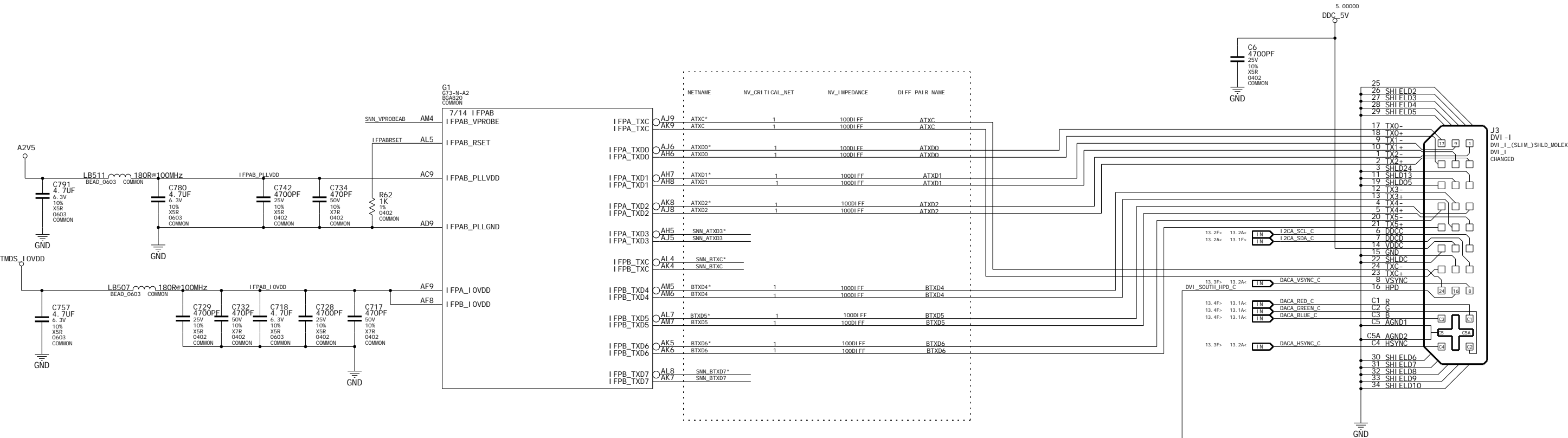
## DACC RGB-FILTER



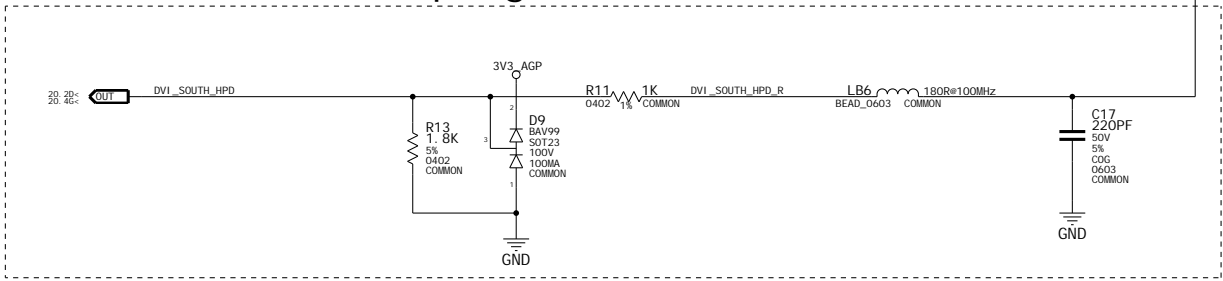
INTERNAL TMD5 .. LINK A & B

IFPAB NET RULES

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLLVDD	3.30000	0.04	16.00
IFPAB_I0VDD	3.30000	0.24	16.00
IFPAB_RSET			12.0



Hotplug Detection



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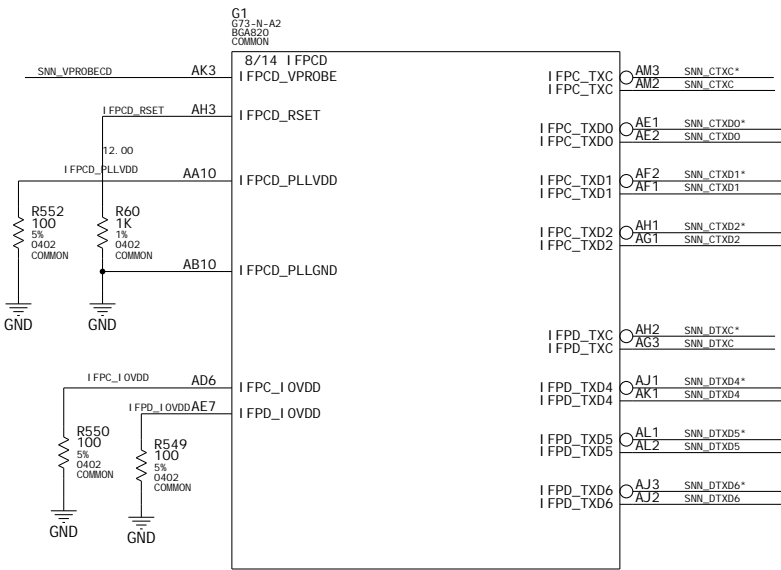


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NAME	dhao	DATE	10-FEB-2006

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INTERNAL TMD5 . . LINK C & D



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PAGE DETAIL INTERNAL TMD5 . . LINK C,D NO USE

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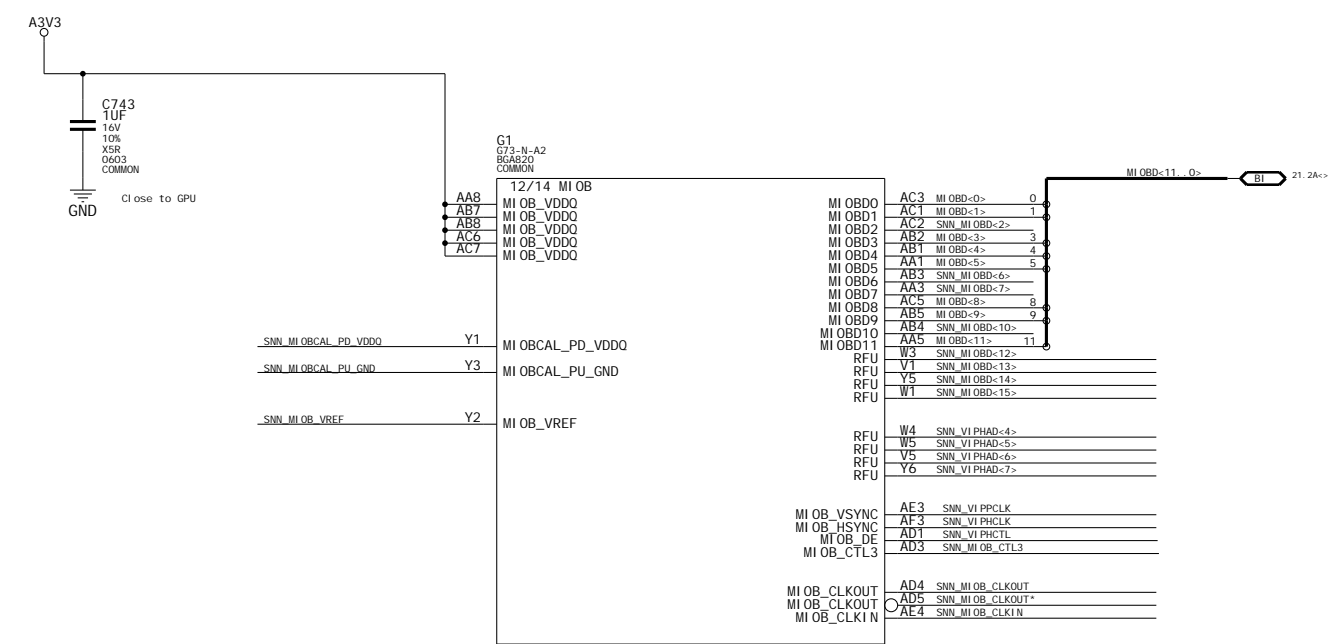
ID design PAGE 16 OF 24

NAME dhao DATE 10-FEB-2006

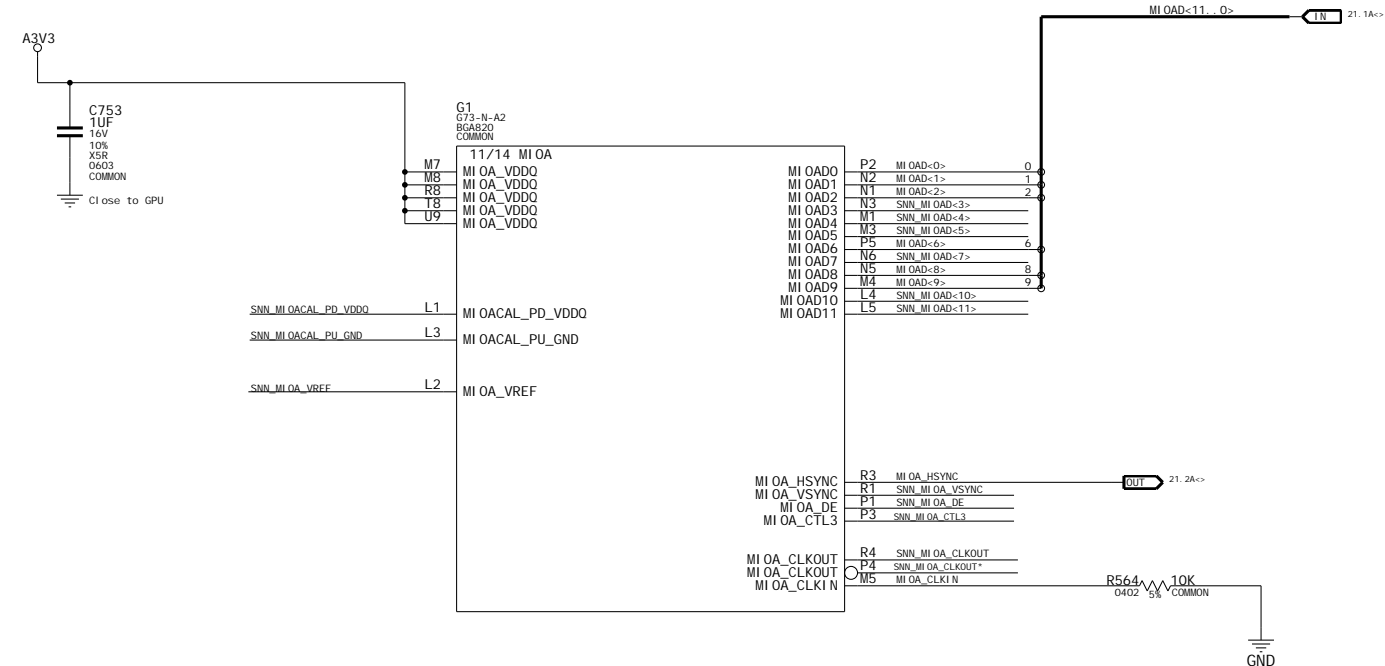
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G3 VI P/MI OB



G3 MI OA



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PAGE DETAIL	GPU-MI OB, MI OA

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NAME	dhao	DATE	10-FEB-2006

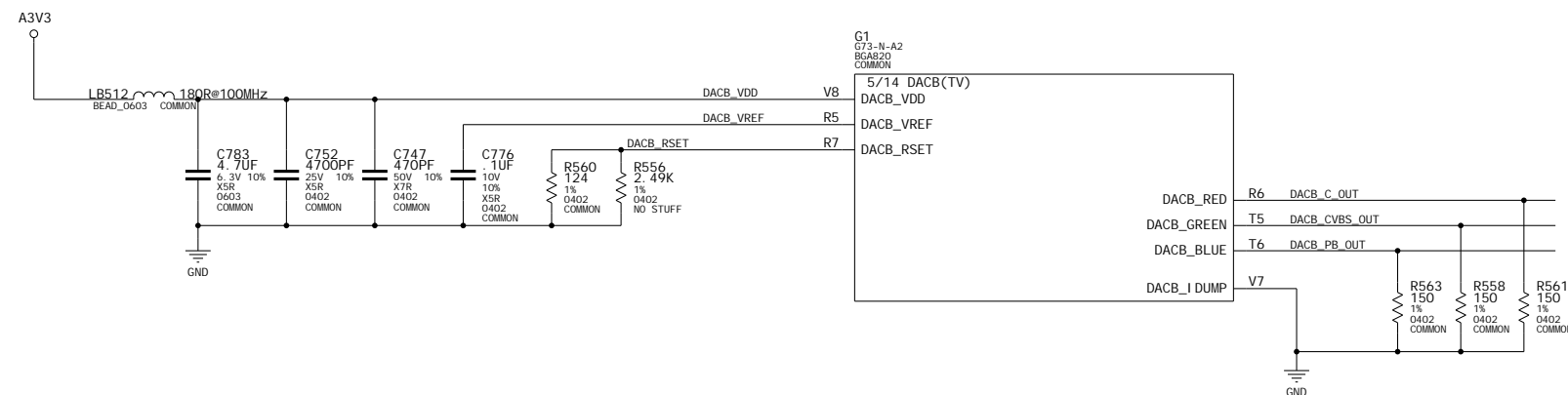
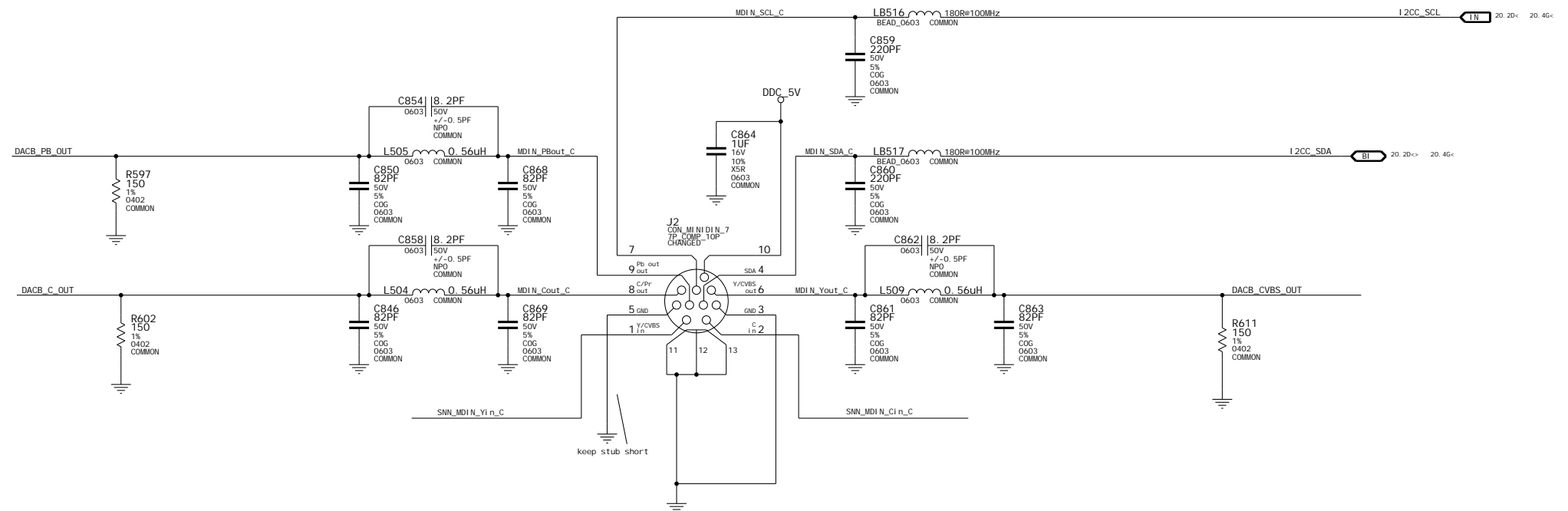
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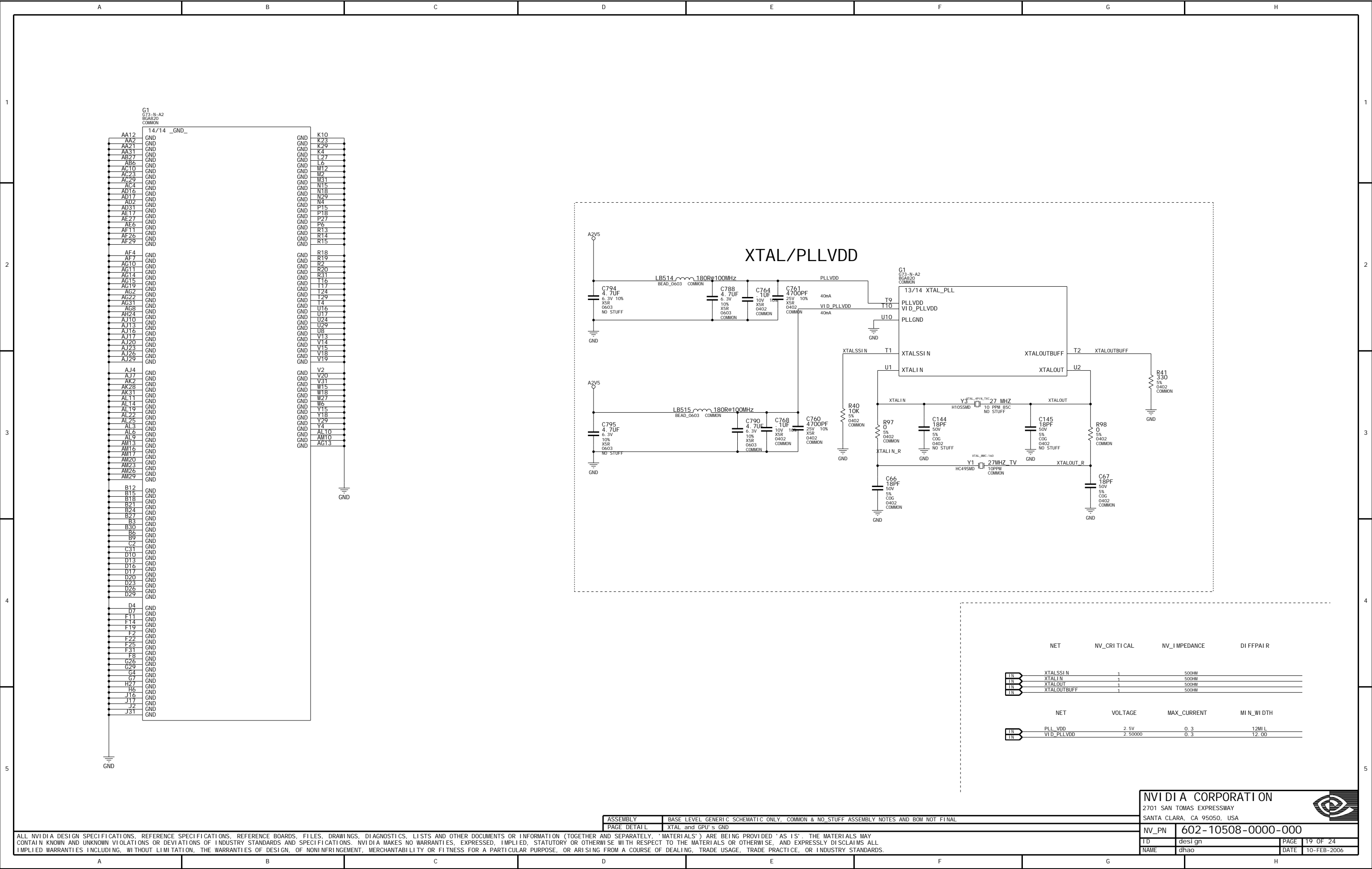
## DACB .. Mini DIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES

# DACB NET RULES

NET		NV_CRI T I CAL	NV_I MPEDANCE	DI FFPA I R
IN	DACB_C_OUT	1	560HM	
IN	MDI N_COUT_C	1	560HM	
IN	DACB_CVBS_OUT	1	560HM	
IN	MDI N_YOUT_C	1	560HM	
IN	DACB_PB_OUT	1	560HM	
IN	MDI N_PBOUT_C	1	560HM	

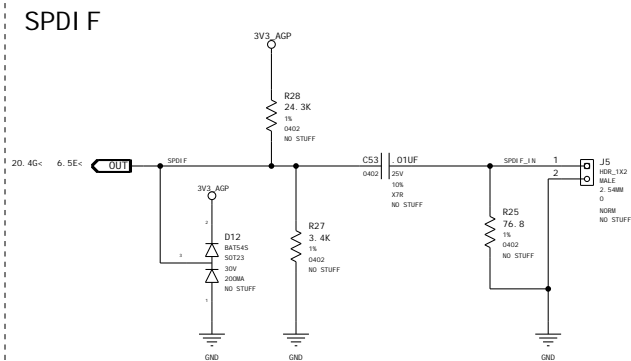
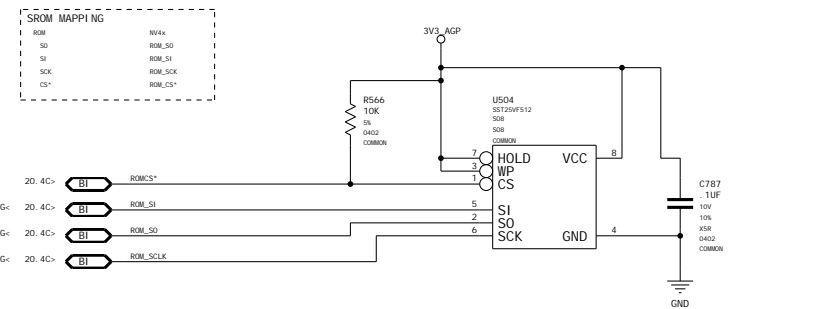
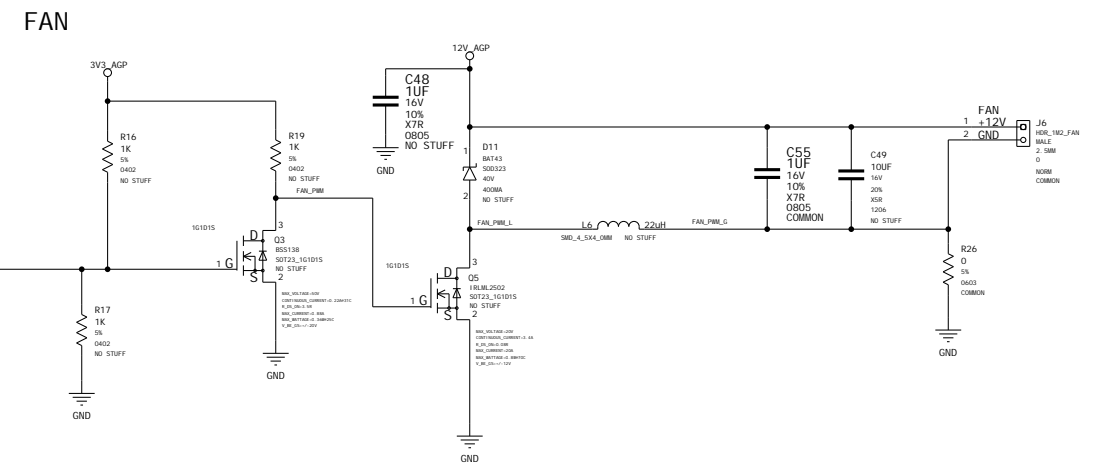
	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
1	MD1 N_SCL_C	2	500HM	
1	MD1 N_SDA_C	2	500HM	
1	DACB_VDD	3.30000	0.07	16.00
1	DACB_VREF			16.00
1	DACB_RSET			16.00





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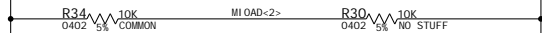
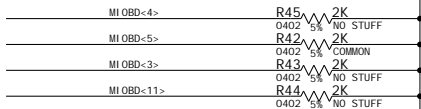
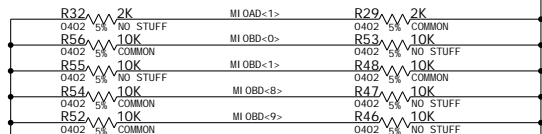
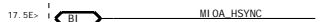
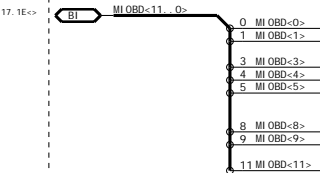
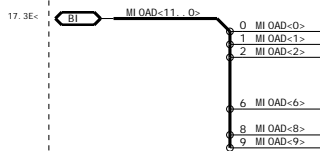
		NET	NV_CRTICAL	NV_IMPEDANCE	DIFFPAIR
20. 2D<	18. 1H<	120C_SCL	2	500W	
20. 2D<>	18. 2H<>	120C_SDA	2	500W	
		120C_SCL_G	2	500W	
		120C_SDA_G	2	500W	
		120H_SCL	2	500W	
		120H_SDA	2	500W	
20. 4C<	20. 3F<>	ROM_CS*	2	500W	
20. 4C<>	20. 3F<>	ROM_S0	2	500W	
20. 4C<>	20. 3F<>	ROM_S0	2	500W	
		ROM_SCLK	2	500W	
20. 2D<	15. 5D<	DW1_SOUTH_HPD	2	500W	
22. 2E<	20. 2D<	NVFAN	2	500W	
		SLOWDOWN*	2	500W	
20. 4D<	6. 5E<	SPDIF_E	1	500W	
		SPDIF_IN	1	500W	

BI OS, Straps, Mi sc

Straps

Assembly: BIOS

Mechanical parts



REG: NV\_PEXTDEV\_BOOT\_0

Bit	Signal	VALUE_ID	VALUES
00:	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED
01:	SUB_VENDOR	SUB_VENDOR	1 NORMAL 0 NO BIOS
02:	RAM_CFG_0	RAM_CFG[3:0]	1 read from BIOS 0000 8Mx16 DDR2 128BIT 0001 RFU 0010 16Mx16 DDR2 128BIT 0011 RFU 0100 RFU 0101 RFU 0110 RFU 0111 32Mx16 DDR2 128BIT
03:	RAM_CFG_1		
04:	RAM_CFG_2		
05:	RAM_CFG_3		
06:	CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz 01 14.31818 Mhz 10 27.000 Mhz 11 unknown
22:	CRYSTAL_1		
07:	TV_MODE_0	TV_MODE[1:0]	00 SECAM 01 NTSC 10 PAL 11 CRT
08:	TV_MODE_1		
09:	AGP8xEnabled	AGP_30_3x	0 AGP8x enabled 1 AGP8x disabled
10:	AGP_SBA	AGP_SBA[0]	0 SBA enabled 1 SBA disabled
11:	AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled
12:	PCI_DEVID_0	PCI_DEVID[3:0]	1 disabled 0000 0x140 ... 1111 0x014F 0000 (default 0x140) 0101 (0x145)
13:	PCI_DEVID_1		
20:	PCI_DEVID_2		
21:	PCI_DEVID_3		
14:	BUS_TYPE	BUS_TYPE[0]	0 PCI 1 AGP
15:	FP_FACE	FP_FACE[0]	0 24BIT 1 12BIT (DEFAULT)
23:	FB_0	FB[1:0]	00 64M 01 128M 10 256M (DEFAULT) 11 512M
24:	FB_1		
25:	BR	BR[0]	0 BRIDGE disabled 1 BRIDGE enabled
26:	BR_128M	BR bits are ignored if BRIDGE is disabled	
27:	BR_AGP		
28:	BR_10		
29:	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F 10 Serial_SST45VF 11 RFU
30:	ROM_TYPE_1		

16:	USER_0	STRAP_USER[3:0]	0000 (default)
17:	USER_1		
18:	USER_2		
19:	USER_3		

31: SLOT\_CLOCK\_CFG  
0 COMMON PCI E REF CLK enabled  
1 COMMON PCI E REF CLK disabled

REG: NV\_STRAP\_1

Bit	Signal	VALUE_ID	VALUES
11:	PEX_PLL_EN_TERM100		0 (default -- internal term on)
12:	3GI_0_PADCFG_LUT_ADR[0]		
13:	3GI_0_PADCFG_LUT_ADR[1]		
14:	3GI_0_PADCFG_LUT_ADR[2]		

155-00003-0000-000

SCREW HEX JACK 4-40 x 12.1MM STANDARD

MEC5

HEX JACK SCREW

STD COMMON

MEC3

HEX JACK SCREW

STD COMMON

MEC4

HEX JACK SCREW

STD COMMON

MEC2

HEX JACK SCREW

STD COMMON

151-10001-0006-001 --> DB15-DVI-MDIN  
151-10001-0006-002 --> DVI-DB15-MDIN

BK1

DVI 3152 DB1552 MDI N490\_TAB

ATX 1X TOP ALT2

COMMON

1

MECH. MOUNTING TOP

GND

MC1

PH 4-40X.1875 SCREW

STD COMMON

MEC1

TM1-2

GPU

COMMON

COOLING SOLUTION

No connected mounting pins

MEC6

110-20000-0021-000

NVIDIA CORPORATION

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SANTA CLARA, CA 95050, USA



NV\_PN 602-10508-0000-000

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NAME dhao DATE 10-FEB-2006

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## 1



## 3



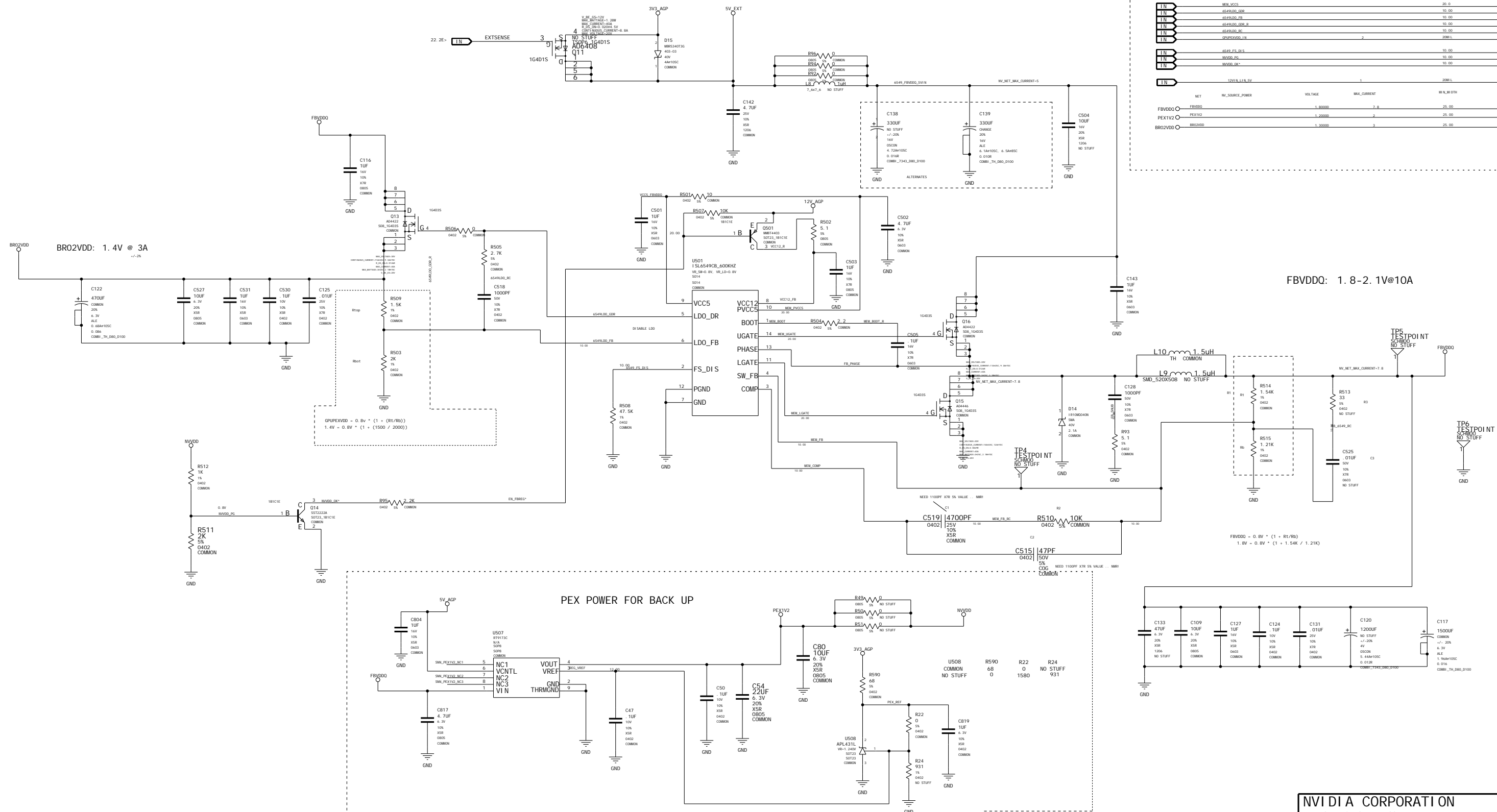
## F



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NAME	dhao	DATE	10-FEB-2006

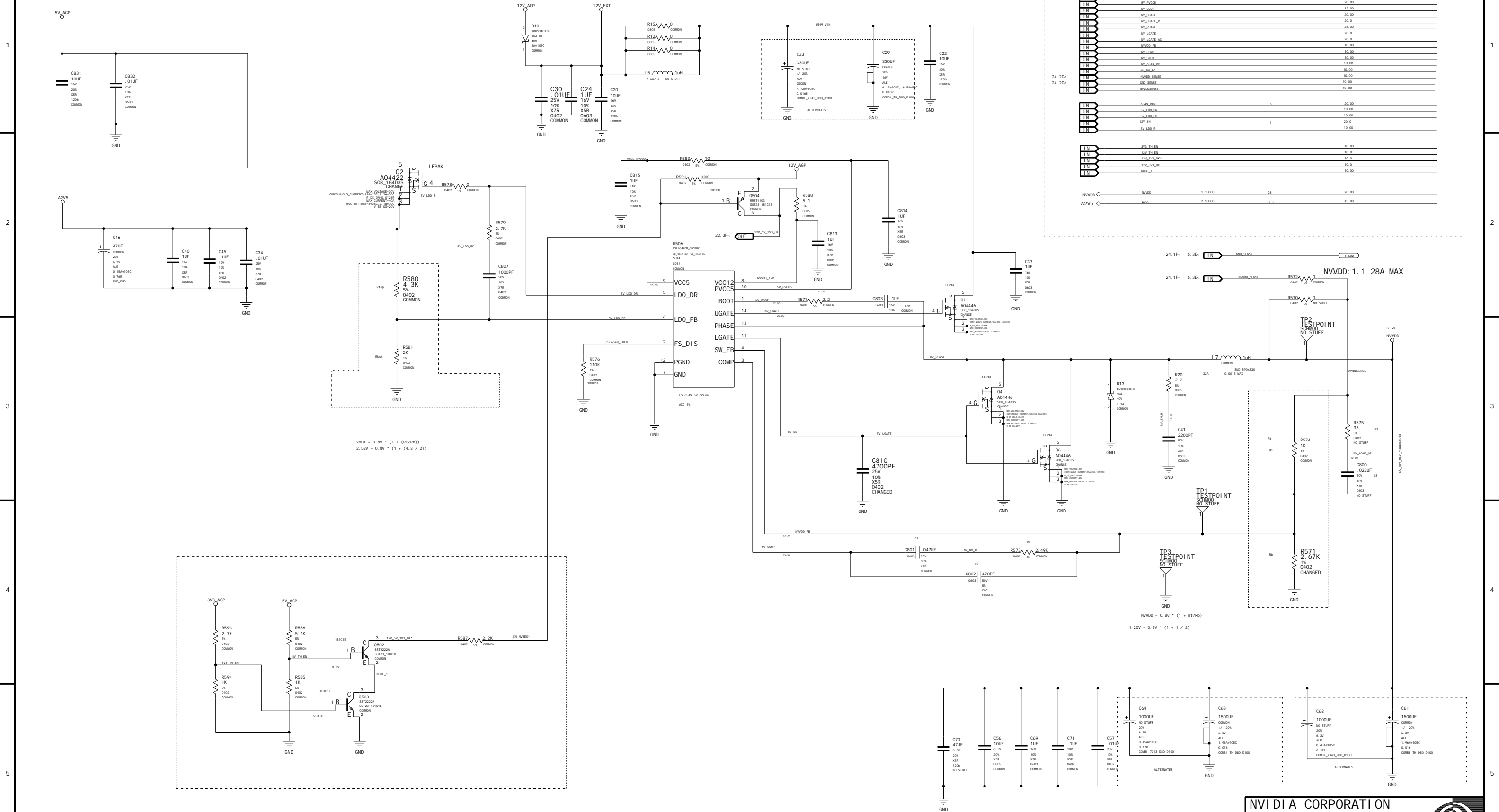
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## PowerSupply | SL6549 | FBVDDQ/BR02VDD/PEX1V2



NET		VOLTAGE	MAX_CURRENT	WLN_BW_DTH	
1N	NEW_PVCC5			20.00	
1N	NEW_BOOT			12.00	
1N	NEW_LGATE			20.00	
1N	NEW_LGATE_R			20.0	
1N	FB_25K5V	7.8		20.00	
1N	NEW_LGATE			20.00	
1N	FB_20K8V			10.00	
1N	NEW_FB			10.00	
1N	NEW_COP			10.00	
1N	FB_10K4V_3C			10.00	
1N	NEW_VCC5			20.0	
1N	6549D5_GDR			10.00	
1N	6549D5_ZR			10.00	
1N	6549D5_WB_R			10.00	
1N	6549D5_RP			10.00	
1N	6549D5_18	2		2000L	
1N	6549_FS_31.5			10.00	
1N	8005D_PG			10.00	
1N	8005D_DR*			10.00	
1N	12018_11N_5V		1	2000L	
NET	WLN_BW_DTH	WLN_BW_DTH	MAX_CURRENT	VOLTAGE	WLN_BW_DTH
FBVDD0	FBVDD0		1.80000	7.8	25.00
PEX1V2	PEX1V2		2.00000	2	25.00
BR0CVDD	BR0CVDD		1.30000	3	25.00

## Power Supply ... ISL6549 NVVDD, 5V



<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
<b>NV_PN</b> 602-10508-0000-000			
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<b>NAME</b>	<b>dhao</b>	<b>DATE</b>	10-FEB-2006

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