P690: GT218, DDR3 MEMORY 64MX16/32MX16

V183 1.2 pcb change list

Page 2：Add EC1802 for 12V_PEX use , G1.E15 pin NC

Page 3：Add R72

Page 5：ESD diose move to close connector side

Page 6：Del DAC B output

Page 7：Add EMI suggestion

Page 8：G1.H6 pin connector to GND

Page 9：G1.P6 D7 pin connector to GND

Page 10：Del JTAG、I2C SCH, U503 pin 3 connector to ROM_VCC

Page 12：Change FBVDDQ PWM sch , Add C99 for 3V3_PEX

Page 12：Change PEX_VDD、5V、3V3_FUSE sch

Page 13：Change NVVDD PWM sch

Page 13：Del PEX_PLL sch

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10690-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10690-0000-000	GT218-300, 550/1375/800, 512MB/64bit, 64Mx16 DDR3, DVI-DL+DP+VGA, DT
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P690 Overview

NVIDIA CORPORATION

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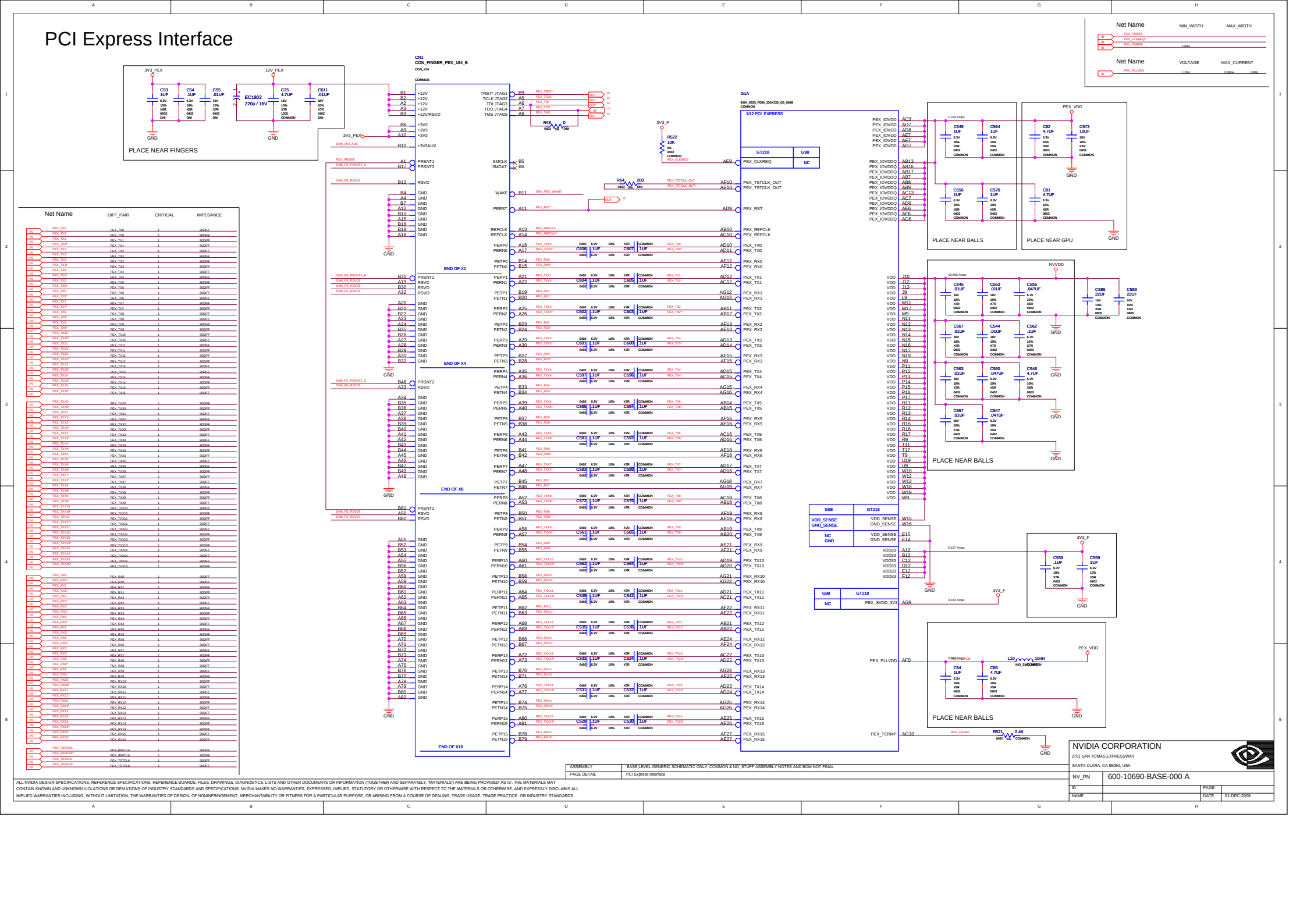
NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

PCI Express Interface



Net Name	DIFF_PAIR	CRITICAL	IMPEDANCE
PEX_TX0	PEX_TX0	1	90DIFF
PEX_TX0*	PEX_TX0	1	90DIFF
PEX_TX1	PEX_TX1	1	90DIFF
PEX_TX1*	PEX_TX1	1	90DIFF
PEX_TX2	PEX_TX2	1	90DIFF
PEX_TX2*	PEX_TX2	1	90DIFF
PEX_TX3	PEX_TX3	1	90DIFF
PEX_TX3*	PEX_TX3	1	90DIFF
PEX_TX4	PEX_TX4	1	90DIFF
PEX_TX4*	PEX_TX4	1	90DIFF
PEX_TX5	PEX_TX5	1	90DIFF
PEX_TX5*	PEX_TX5	1	90DIFF
PEX_TX6	PEX_TX6	1	90DIFF
PEX_TX6*	PEX_TX6	1	90DIFF
PEX_TX7	PEX_TX7	1	90DIFF
PEX_TX7*	PEX_TX7	1	90DIFF
PEX_TX8	PEX_TX8	1	90DIFF
PEX_TX8*	PEX_TX8	1	90DIFF
PEX_TX9	PEX_TX9	1	90DIFF
PEX_TX9*	PEX_TX9	1	90DIFF
PEX_TX10	PEX_TX10	1	90DIFF
PEX_TX10*	PEX_TX10	1	90DIFF
PEX_TX11	PEX_TX11	1	90DIFF
PEX_TX11*	PEX_TX11	1	90DIFF
PEX_TX12	PEX_TX12	1	90DIFF
PEX_TX12*	PEX_TX12	1	90DIFF
PEX_TX13	PEX_TX13	1	90DIFF
PEX_TX13*	PEX_TX13	1	90DIFF
PEX_TX14	PEX_TX14	1	90DIFF
PEX_TX14*	PEX_TX14	1	90DIFF
PEX_TX15	PEX_TX15	1	90DIFF
PEX_TX15*	PEX_TX15	1	90DIFF
PEX_TX0	PEX_TX0	1	90DIFF
PEX_TX0*	PEX_TX0	1	90DIFF
PEX_TX1	PEX_TX1	1	90DIFF
PEX_TX1*	PEX_TX1	1	90DIFF
PEX_TX2	PEX_TX2	1	90DIFF
PEX_TX2*	PEX_TX2	1	90DIFF
PEX_TX3	PEX_TX3	1	90DIFF
PEX_TX3*	PEX_TX3	1	90DIFF
PEX_TX4	PEX_TX4	1	90DIFF
PEX_TX4*	PEX_TX4	1	90DIFF
PEX_TX5	PEX_TX5	1	90DIFF
PEX_TX5*	PEX_TX5	1	90DIFF
PEX_TX6	PEX_TX6	1	90DIFF
PEX_TX6*	PEX_TX6	1	90DIFF
PEX_TX7	PEX_TX7	1	90DIFF
PEX_TX7*	PEX_TX7	1	90DIFF
PEX_TX8	PEX_TX8	1	90DIFF
PEX_TX8*	PEX_TX8	1	90DIFF
PEX_TX9	PEX_TX9	1	90DIFF
PEX_TX9*	PEX_TX9	1	90DIFF
PEX_TX10	PEX_TX10	1	90DIFF
PEX_TX10*	PEX_TX10	1	90DIFF
PEX_TX11	PEX_TX11	1	90DIFF
PEX_TX11*	PEX_TX11	1	90DIFF
PEX_TX12	PEX_TX12	1	90DIFF
PEX_TX12*	PEX_TX12	1	90DIFF
PEX_TX13	PEX_TX13	1	90DIFF
PEX_TX13*	PEX_TX13	1	90DIFF
PEX_TX14	PEX_TX14	1	90DIFF
PEX_TX14*	PEX_TX14	1	90DIFF
PEX_TX15	PEX_TX15	1	90DIFF
PEX_TX15*	PEX_TX15	1	90DIFF
PEX_RX0	PEX_RX0	1	90DIFF
PEX_RX0*	PEX_RX0	1	90DIFF
PEX_RX1	PEX_RX1	1	90DIFF
PEX_RX1*	PEX_RX1	1	90DIFF
PEX_RX2	PEX_RX2	1	90DIFF
PEX_RX2*	PEX_RX2	1	90DIFF
PEX_RX3	PEX_RX3	1	90DIFF
PEX_RX3*	PEX_RX3	1	90DIFF
PEX_RX4	PEX_RX4	1	90DIFF
PEX_RX4*	PEX_RX4	1	90DIFF
PEX_RX5	PEX_RX5	1	90DIFF
PEX_RX5*	PEX_RX5	1	90DIFF
PEX_RX6	PEX_RX6	1	90DIFF
PEX_RX6*	PEX_RX6	1	90DIFF
PEX_RX7	PEX_RX7	1	90DIFF
PEX_RX7*	PEX_RX7	1	90DIFF
PEX_RX8	PEX_RX8	1	90DIFF
PEX_RX8*	PEX_RX8	1	90DIFF
PEX_RX9	PEX_RX9	1	90DIFF
PEX_RX9*	PEX_RX9	1	90DIFF
PEX_RX10	PEX_RX10	1	90DIFF
PEX_RX10*	PEX_RX10	1	90DIFF
PEX_RX11	PEX_RX11	1	90DIFF
PEX_RX11*	PEX_RX11	1	90DIFF
PEX_RX12	PEX_RX12	1	90DIFF
PEX_RX12*	PEX_RX12	1	90DIFF
PEX_RX13	PEX_RX13	1	90DIFF
PEX_RX13*	PEX_RX13	1	90DIFF
PEX_RX14	PEX_RX14	1	90DIFF
PEX_RX14*	PEX_RX14	1	90DIFF
PEX_RX15	PEX_RX15	1	90DIFF
PEX_RX15*	PEX_RX15	1	90DIFF
PEX_REFCLK	PEX_REFCLK	1	90DIFF
PEX_REFCLK*	PEX_REFCLK	1	90DIFF
PEX_TSTCLK	PEX_TSTCLK	1	90DIFF
PEX_TSTCLK*	PEX_TSTCLK	1	90DIFF

Net Name	MIN_WIDTH	MAX_WIDTH
PEX_PRSNT		
PEX_CLKREQ*		
PEX_TERMP	12MIL	

Net Name	VOLTAGE	MAX_CURRENT
PEX_PLLVDD	1.05V	0.080A 12MIL

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express Interface

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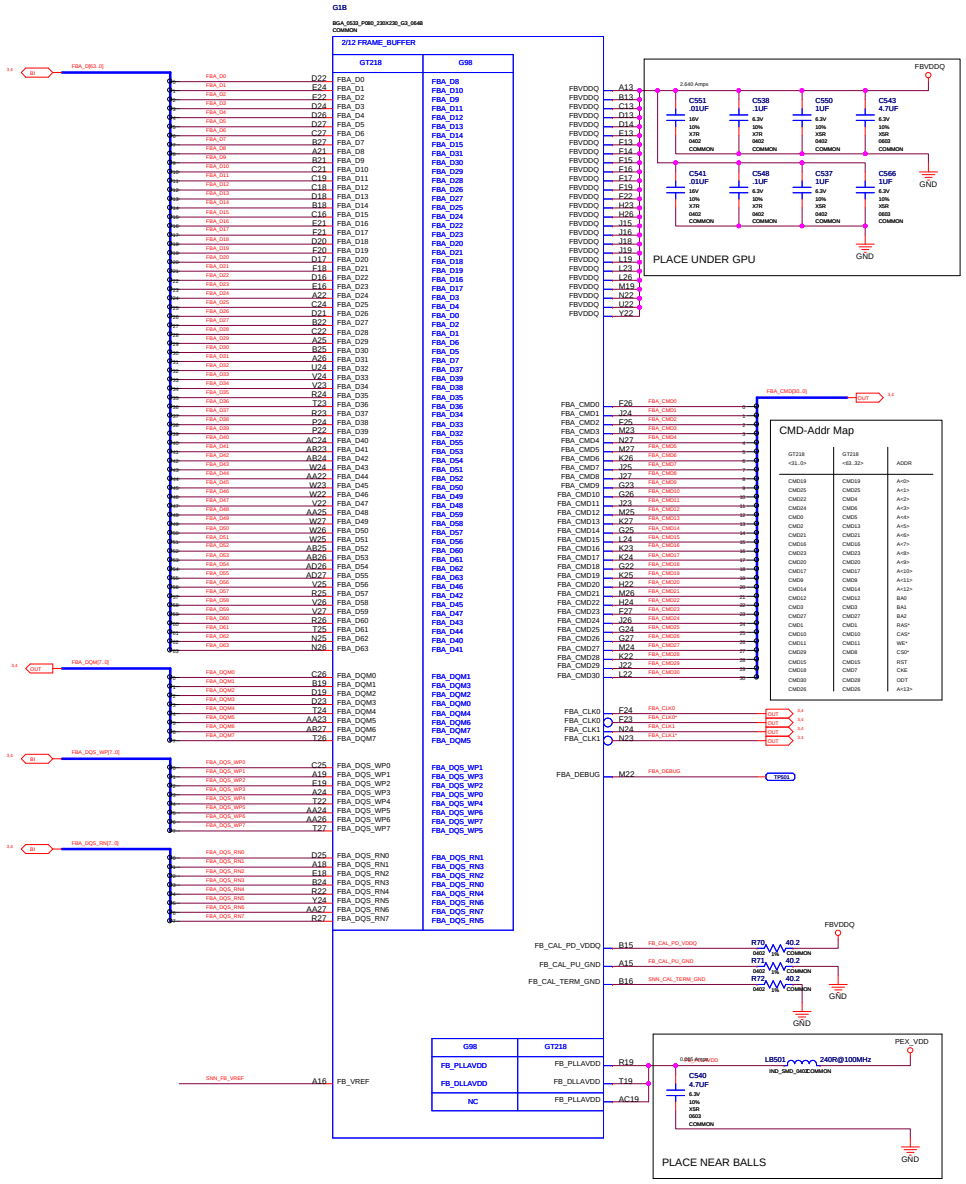
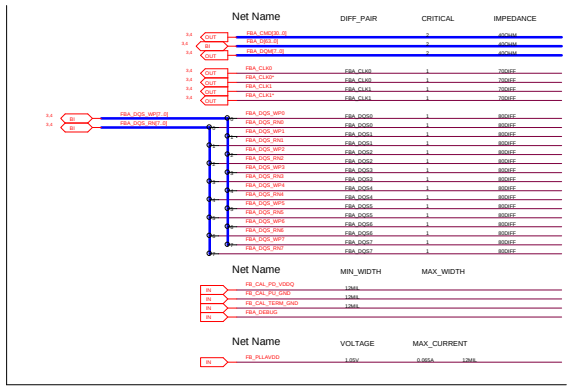
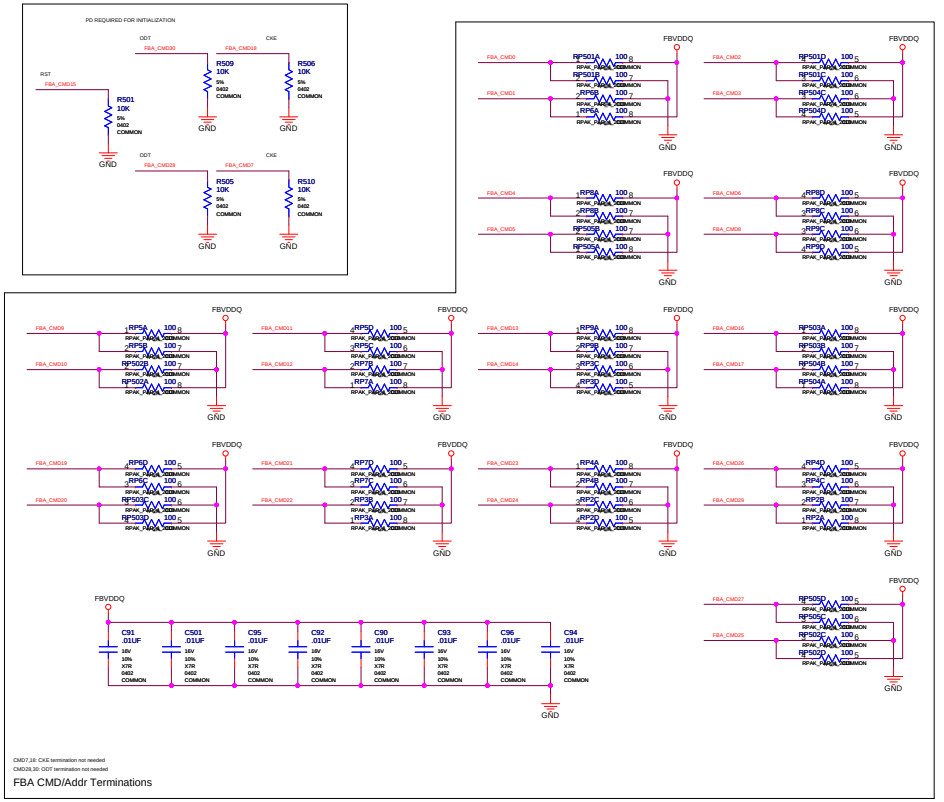
NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

Frame Buffer Interface







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Frame Buffer Interface

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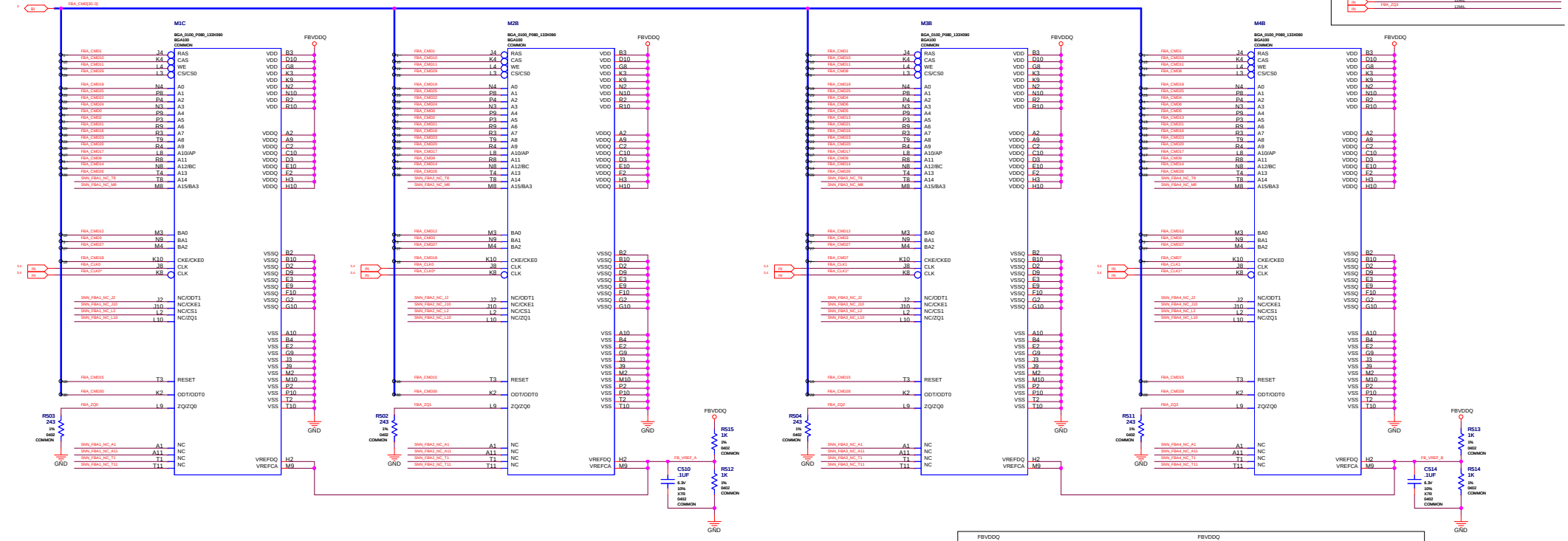
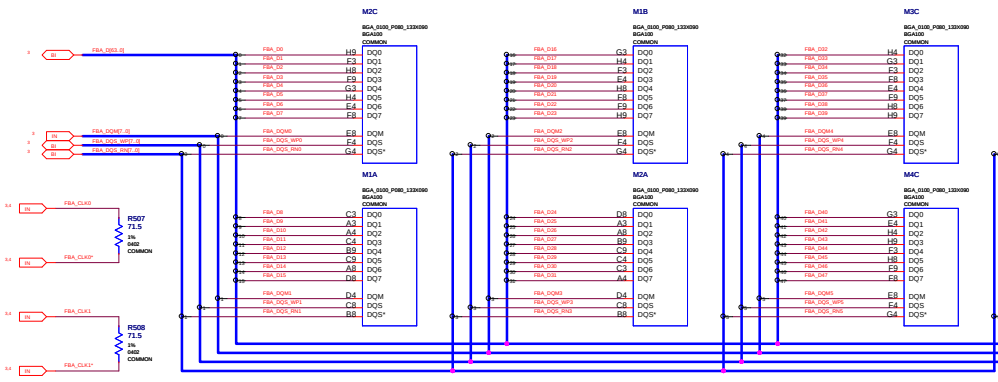
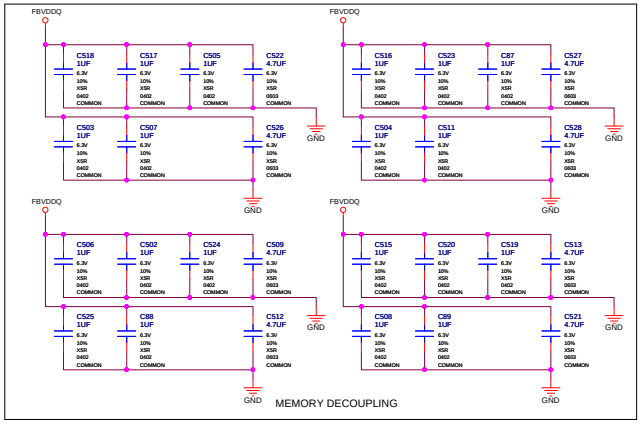
DDR3 Memories







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DDR3 Memories

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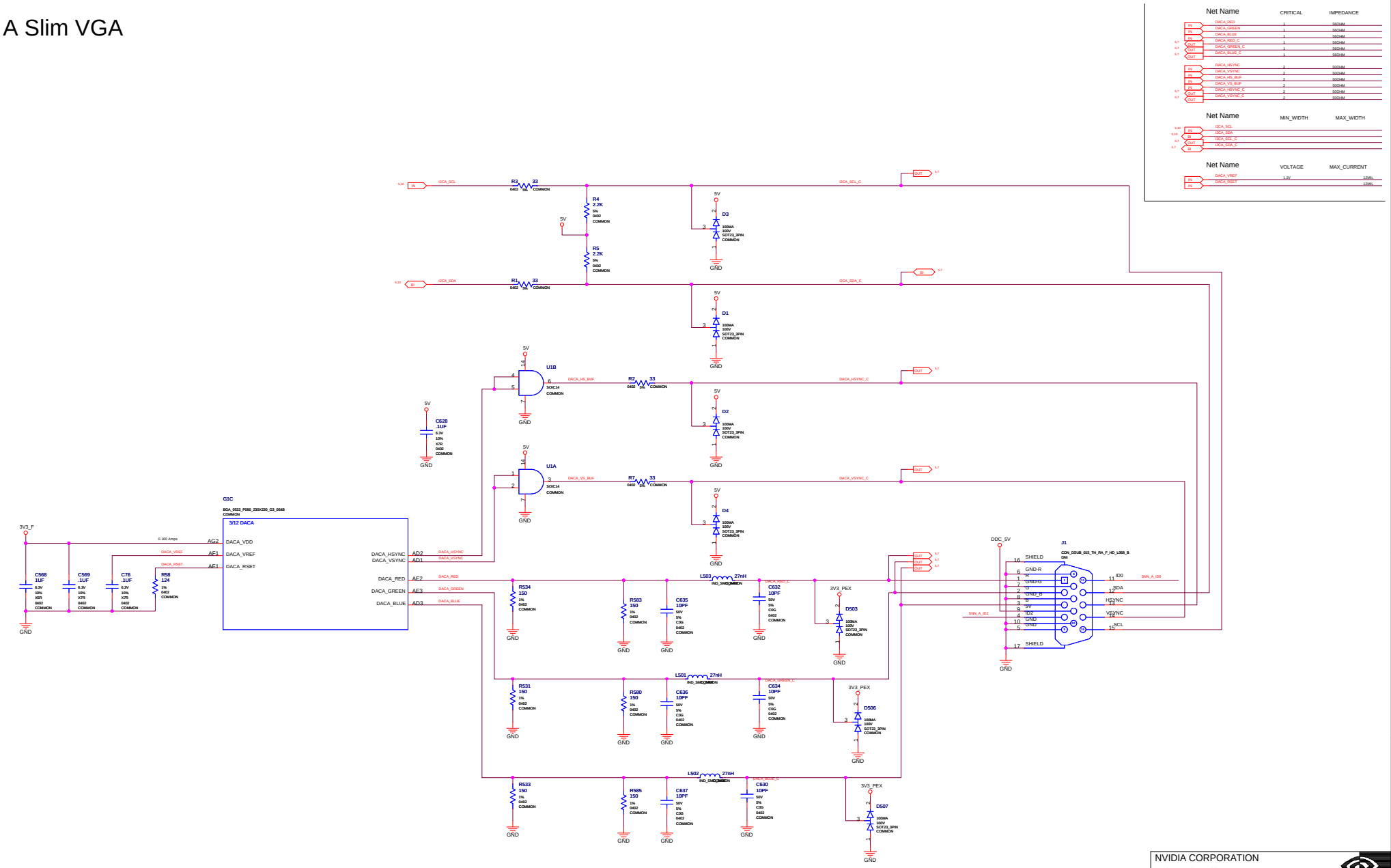
NAME		DATE	01-DEC-2008

DAC A Slim VGA



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DAC A Slim VGA

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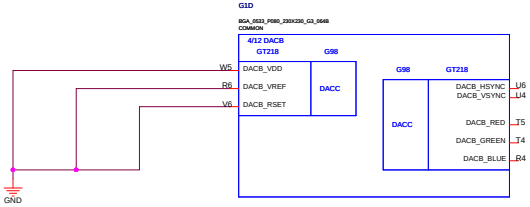
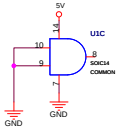
DAC B VGA Header

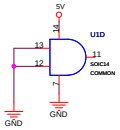
Net Name	CRITICAL	IMPEDANCE
DACB_RED	1	50OHM
DACB_GREEN	1	50OHM
DACB_BLUE	1	50OHM
DACB_RED_C	1	50OHM
DACB_GREEN_C	1	50OHM
DACB_BLUE_C	1	50OHM
DACB_HSYNC	2	50OHM
DACB_VSYNC	2	50OHM
DACB_HSYNC_C	2	50OHM
DACB_VSYNC_C	2	50OHM
DACB_HS_BUF	2	50OHM
DACB_VS_BUF	2	50OHM

Net Name	MIN_WIDTH	MAX_WIDTH
I2CB_SCL		
I2CB_SDA		
I2CB_SCL_C		
I2CB_SDA_C		

Net Name	VOLTAGE	MAX_CURRENT
DACB_VREF	1.2V	12MIL
DACB_RSET		12MIL







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DAC B VGA Header

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NV_PN	600-10690-BASE-000 A		
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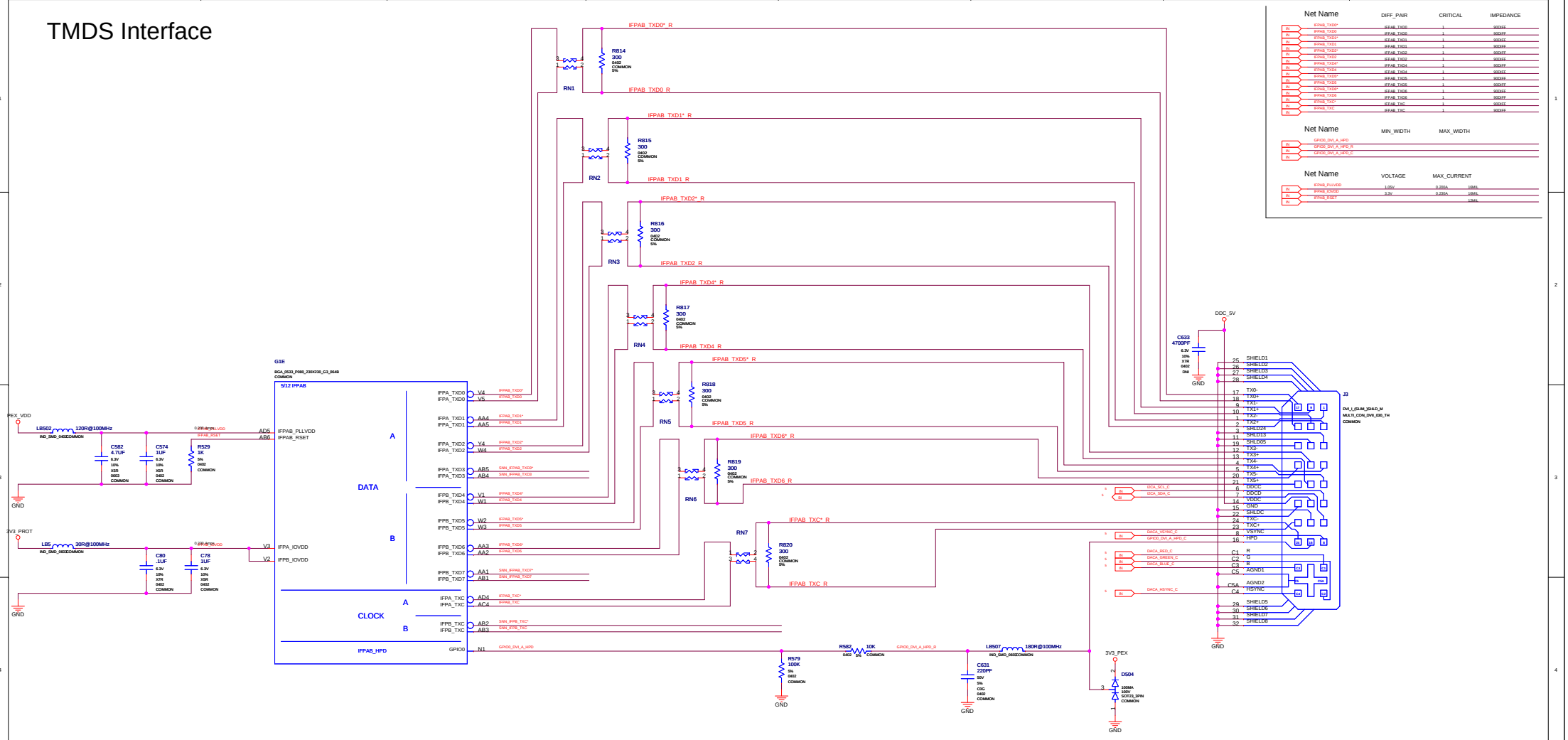
TMDS Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS Interface

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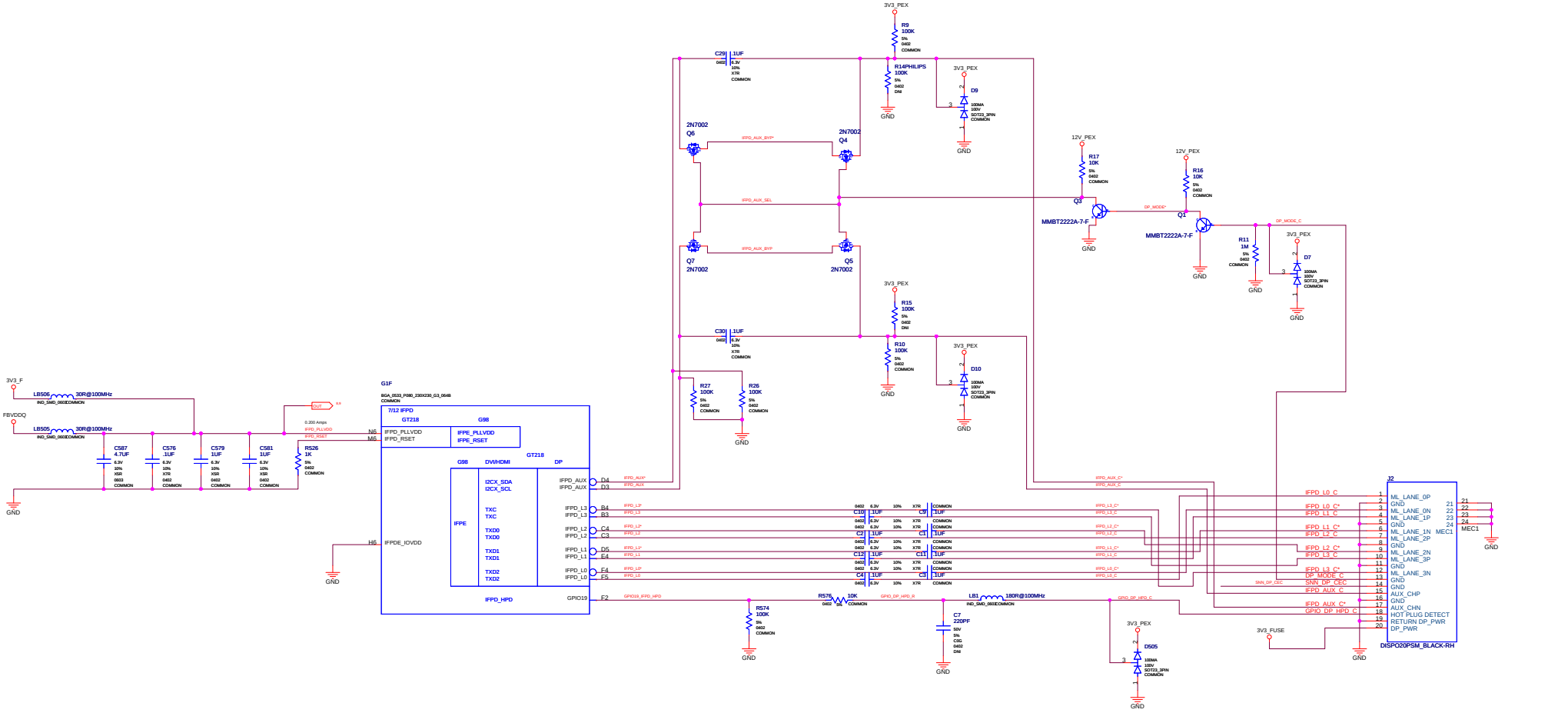
DisplayPort Connector



Net Name	MIN_WIDTH	MAX_WIDTH
GPIO_DP_HPD_C		
GPIO_DP_HPD_R		
GPIO19_IFPD_HPD		
IFPD_AUX_SEL		
DP_MODE*		
DP_MODE_C		

Net Name	VOLTAGE	MAX_CURRENT	
IFPD_PLLVDD	3.3V	0.200A	10MIL
IFPD_IOVDD	1.05V	0.250A	10MIL
IFPD_RSET			12MIL

Net Name	DIFF_PAIR	CRITICAL	IMPEDANCE
IFPD_AUX*	IFPD_AUX	1	90OHM
IFPD_AUX	IFPD_AUX	1	90OHM
IFPD_AUX_BYP*	IFPD_AUX_BYP	1	90OHM
IFPD_AUX_BYP	IFPD_AUX_BYP	1	90OHM
IFPD_AUX_C*	IFPD_AUX_C	1	90OHM
IFPD_AUX_C	IFPD_AUX_C	1	90OHM
IFPD_L3*	IFPD_L3	1	90OHM
IFPD_L3	IFPD_L3	1	90OHM
IFPD_L2*	IFPD_L2	1	90OHM
IFPD_L2	IFPD_L2	1	90OHM
IFPD_L1*	IFPD_L1	1	90OHM
IFPD_L1	IFPD_L1	1	90OHM
IFPD_L0*	IFPD_L0	1	90OHM
IFPD_L3_C*	IFPD_L3_C	1	90OHM
IFPD_L3_C	IFPD_L3_C	1	90OHM
IFPD_L2_C*	IFPD_L2_C	1	90OHM
IFPD_L2_C	IFPD_L2_C	1	90OHM
IFPD_L1_C*	IFPD_L1_C	1	90OHM
IFPD_L1_C	IFPD_L1_C	1	90OHM
IFPD_L0_C*	IFPD_L0_C	1	90OHM
IFPD_L0_C	IFPD_L0_C	1	90OHM

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DisplayPort Connector

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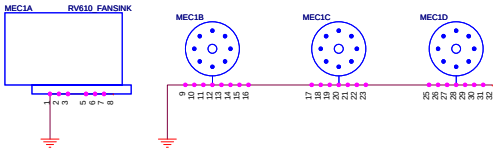
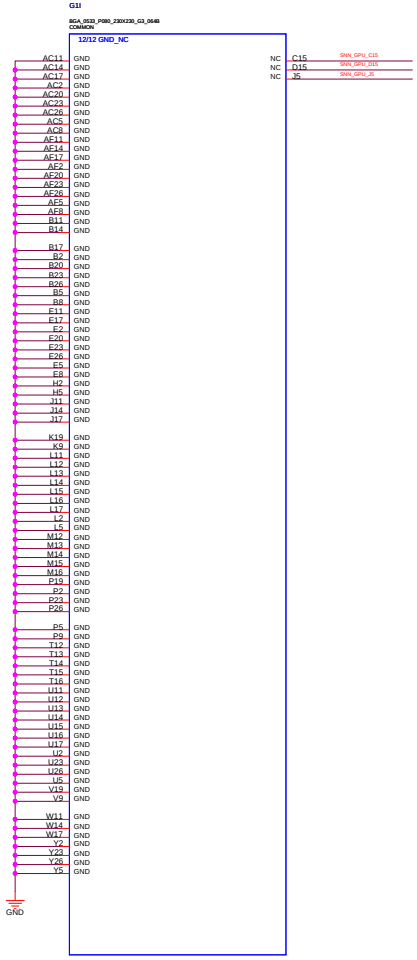
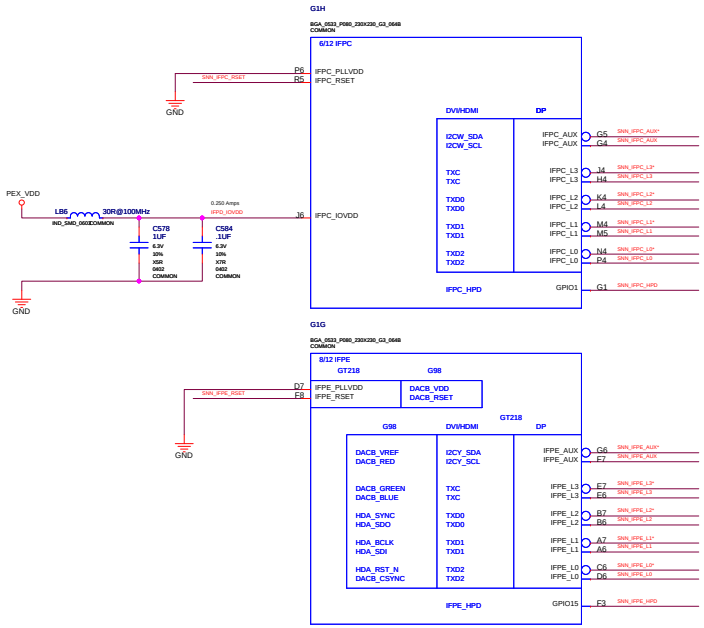
IFPC, IFPE Interface, Fan, Mechanical

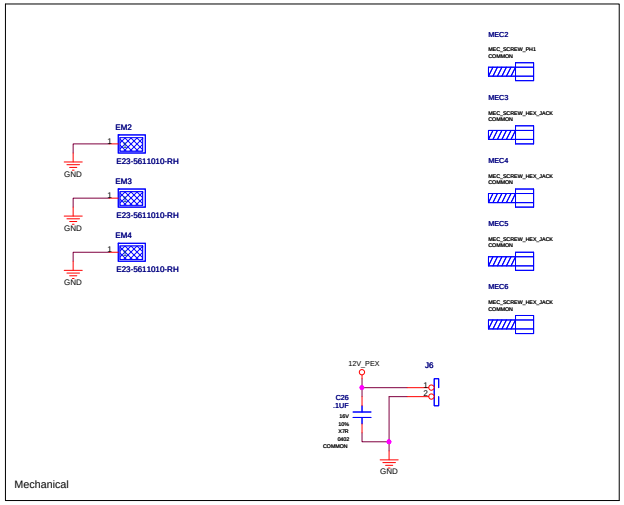
Net Name	VOLTAGE	MAX_CURRENT
IFPC_PLLVDD	3.3V	0.200A
IFPC_IOVDD	1.05V	16MIL

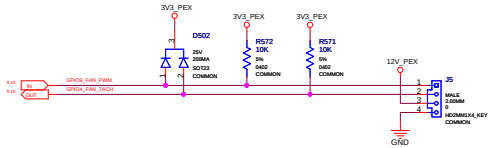
Net Name	MIN_WIDTH	MAX_WIDTH
GPIO9_FAN_TACH		
GPIO8_FAN_PWM		











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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPC, IFPE Interface, Fan, Mechanical

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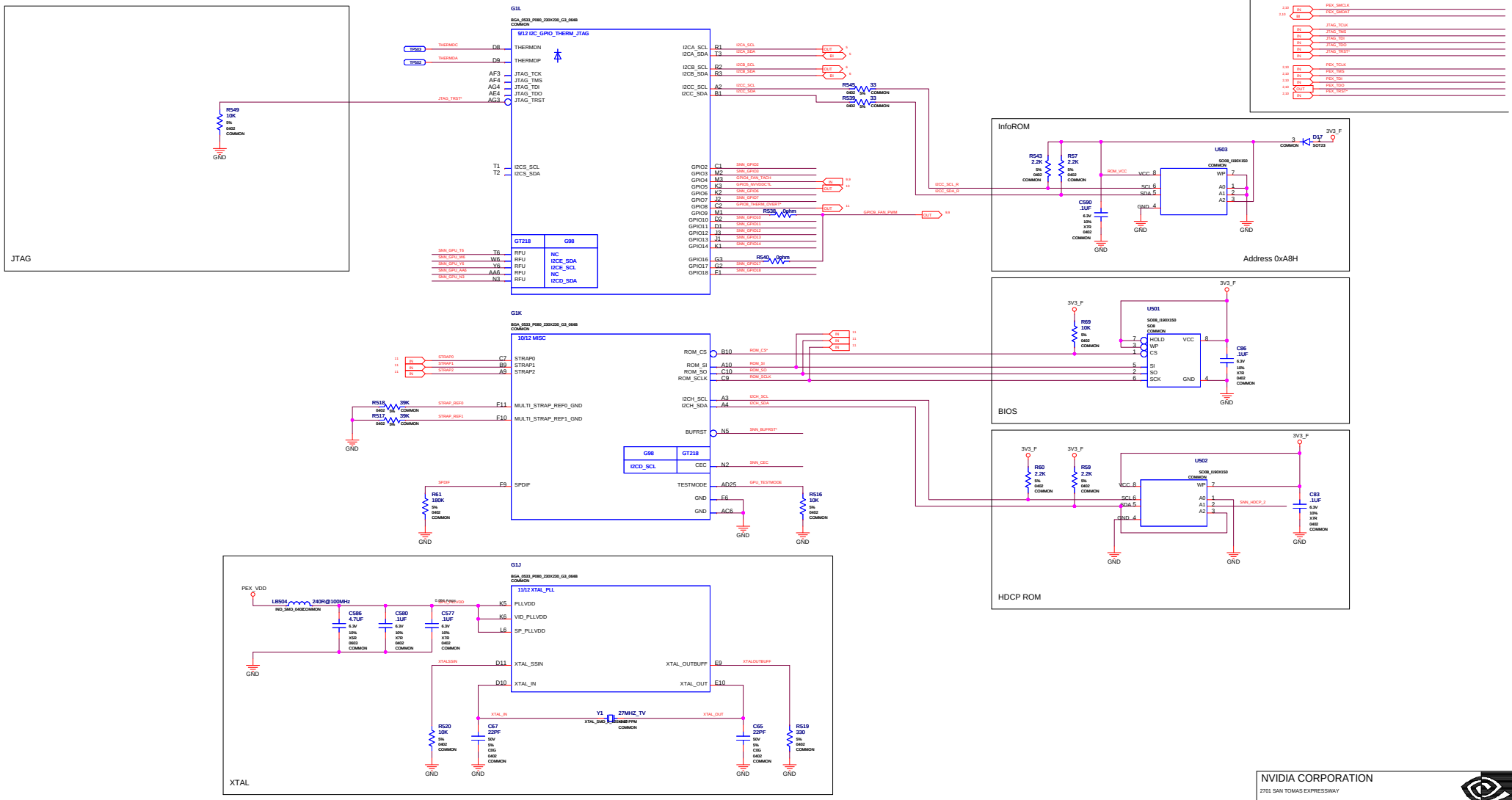
XTAL, ROM, SPDIF, JTAG



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, ROM, SPDIF, JTAG

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NV_PN	600-10690-BASE-000 A		
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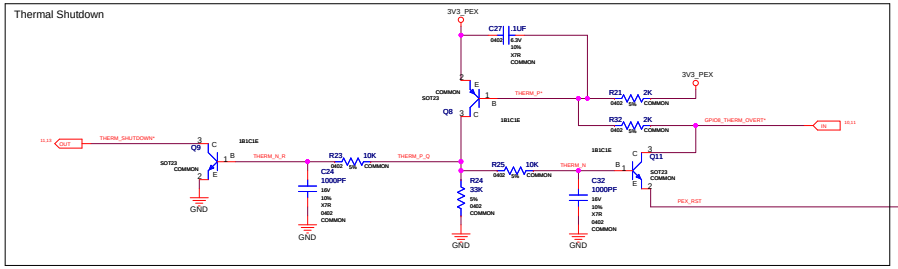
Thermal Protection, IFP_IOVDD, Straps

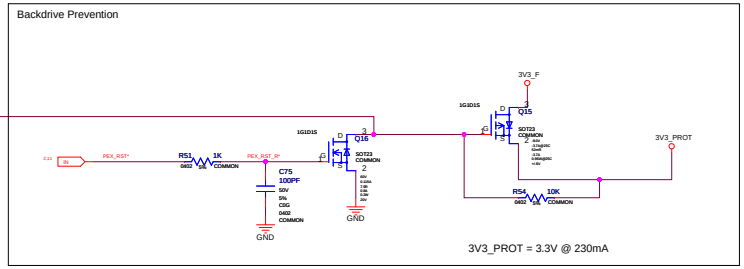
Net Name	MIN_WIDTH	MAX_WIDTH
PEX_RST		
PEX_RST_R*		
PEX_RST*		
GPIO8_THERM_OVERT*		
THERM_N_R		
THERM_P_Q		
THERM_P*		
THERM_N		
THERM_SHUTDOWN*		
ROM_SI		
ROM_SO		
ROM_SCLK		
STRAP2		
STRAP1		
STRAP0		

Net Name	VOLTAGE	MAX_CURRENT
3V3_PROT	3.3V	0.23A 169ML

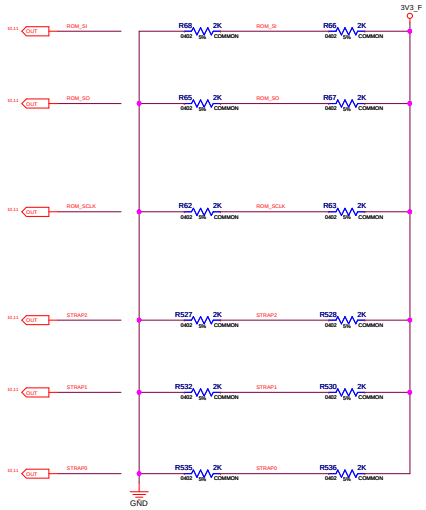
Thermal Shutdown



Backdrive Prevention



3V3_PROT = 3.3V @ 230mA



GT218 Straps MLS Mode

Bit	Signal	Values		
03:	RAMCFG[3]	0000	Elpida	
		0001	Samsung, Micron	
02:	RAMCFG[2]	0010	Qimonda	
		0011	Hynix	
01:	RAMCFG[1]	0100	Nanya	
00:	RAMCFG[0]			
03:	XCLK_417	0	277 (Default)	
02:	FB[0]	0	256M (Default)	
01:	SMB_ALT_ADDR	0	0x8E	
		1	0x8C	
00:	VGA_DEVICE	0	Class code 302	
		1	Class code 300	
03:	PCI_DEVID_EXT	0	GT218-300-A1	
02:	SUB_VENDOR	0	No BIOS	
		1	BIOS	
01:	SLOT_CLK_CFG	0	Disable	
		1	Enable	
00:	PEX_PLL_EN_TERM100	0	Disable	
		1	Enable	
03:	PCI_DEVID[3]	0000	GT218-300-A1	
02:	PCI_DEVID[2]			
01:	PCI_DEVID[1]			
00:	PCI_DEVID[0]			
03:	3GIO_PADCFG_LUT_ADR[3]	0000	DSKTOP_DEFAULT	1000 DSKTOP_HTHRS
		0001	MOBILE_DEFAULT	1001 MOBILE_HTHRS_NAMP
02:	3GIO_PADCFG_LUT_ADR[2]	0010	MOBILE_NTHRS_LLAMP	1010 MOBILE_HTHRS_LLAMP
		0011	MOBILE_NTHRS_LAMP	1011 MOBILE_HTHRS_LAMP
01:	3GIO_PADCFG_LUT_ADR[1]	0100	MOBILE_NTHRS_HAMP	1100 MOBILE_HTHRS_HAMP
		0101	MOBILE_NTHRS_HHAMP	1101 MOBILE_HTHRS_HHAMP
00:	3GIO_PADCFG_LUT_ADR[0]	0110	MOBILE_NTHRS_HHHAMP	1110 MOBILE_HTHRS_HHHAMP
		0111	MOBILE_NTHRS_HHHHAMP	1111 MOBILE_HTHRS_HHHHAMP
03:	USER[3]	0000	Default	
02:	USER[2]			
01:	USER[1]			
00:	USER[0]			

Multilevel Straps

5K to GND	0000
10K to GND	0001
15K to GND	0010
20K to GND	0011
25K to GND	0100
30K to GND	0101
35K to GND	0110
40K to GND	0111
5K to VCC	1000
10K to VCC	1001
15K to VCC	1010
20K to VCC	1011
25K to VCC	1100
30K to VCC	1101
35K to VCC	1110
40K to VCC	1111

GT218 Straps BU Mode

Bit	Signal	Values	
	PCI_DEVID_EXT	0	GT218-300-A1
	XCLK_417	0	277 (Default)
	3GIO_PADCFG_LUT_ADR[3]	0000	DSKTOP_DEFAULT
		0001	MOBILE_DEFAULT
		0010	MOBILE_NTHRS_LLAMP
		0011	MOBILE_NTHRS_LAMP
		0100	MOBILE_NTHRS_HAMP
		0101	MOBILE_NTHRS_HHAMP
		0110	MOBILE_NTHRS_HHHAMP
		0111	MOBILE_NTHRS_HHHHAMP
		1000	DSKTOP_HTHRS
		1001	MOBILE_HTHRS_NAMP
		1010	MOBILE_HTHRS_LLAMP
		1011	MOBILE_HTHRS_LAMP
	3GIO_PADCFG_LUT_ADR[2]	1100	MOBILE_HTHRS_HAMP
		1101	MOBILE_HTHRS_HHAMP
		1110	MOBILE_HTHRS_HHHAMP
		1111	MOBILE_HTHRS_HHHHAMP
	3GIO_PADCFG_LUT_ADR[1]		
	3GIO_PADCFG_LUT_ADR[0]		

GT218 Straps PM Mode

Bit	Signal	Values	
	PCI_DEVID_EXT	0	GT218-300-A1
	XCLK_417	0	277/277 OR 417/417
	PCI_DEVID[3]	0	GT218-300-A1
	RAMCFG[3]	0000	Elpida
		0001	Samsung, Micron
		0010	Qimonda
		0011	Hynix
		0100	Nanya
	RAMCFG[1]		
	RAMCFG[0]		

Mode	REF0/REF1
MLS	Stuff
BU	No stuff
PM	Stuff one

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Protection, IFP_IOVDD, Straps

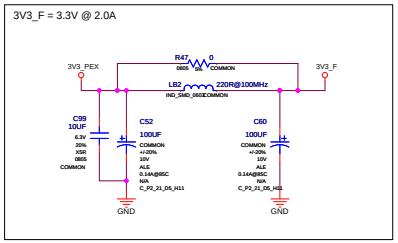
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

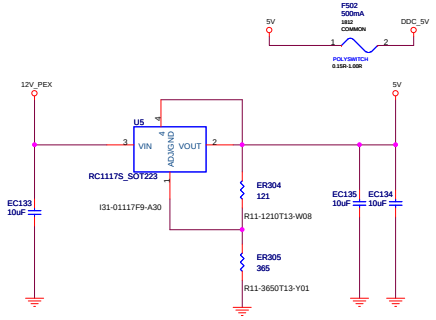
NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

Power Supply I: FBVDD/Q, PEX_VDD, 5V, 3V3_F

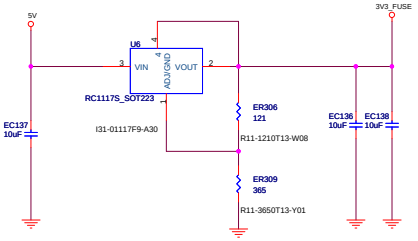
3V3_FUSE = 3.3V @ 500mA

3V3_F = 3.3V @ 2.0A

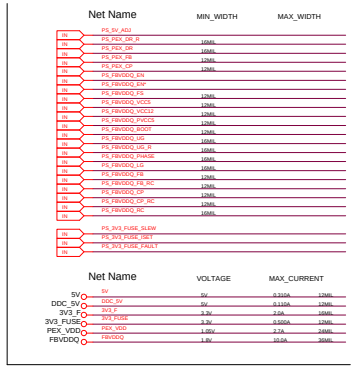


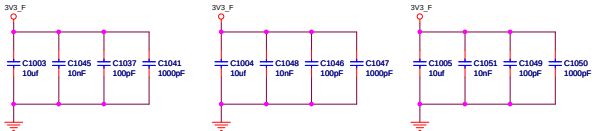


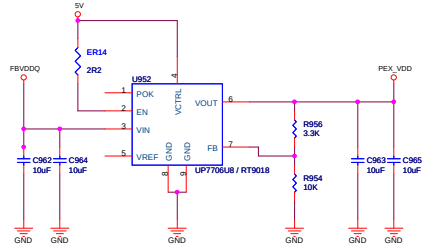
Vout=1.25V* [1+(ER305/ER304)]



Vout=1.25V* [1+(ER305/ER304)]

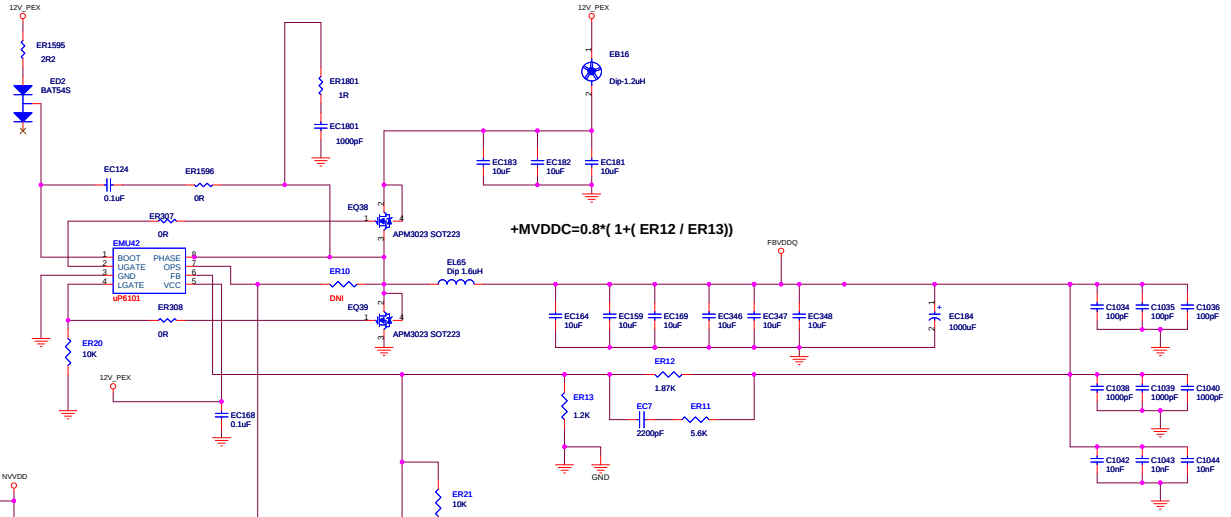




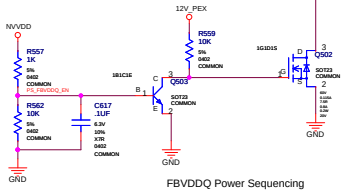


Vout=0.8V * (1+ R995 / R954)

PEX_VDD = 1.05V @ 2.7A



Memory Power Seq



FBVDDQ Power Sequencing

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply I: FBVDDQ, PEX_VDD, 5V, 3V3_F

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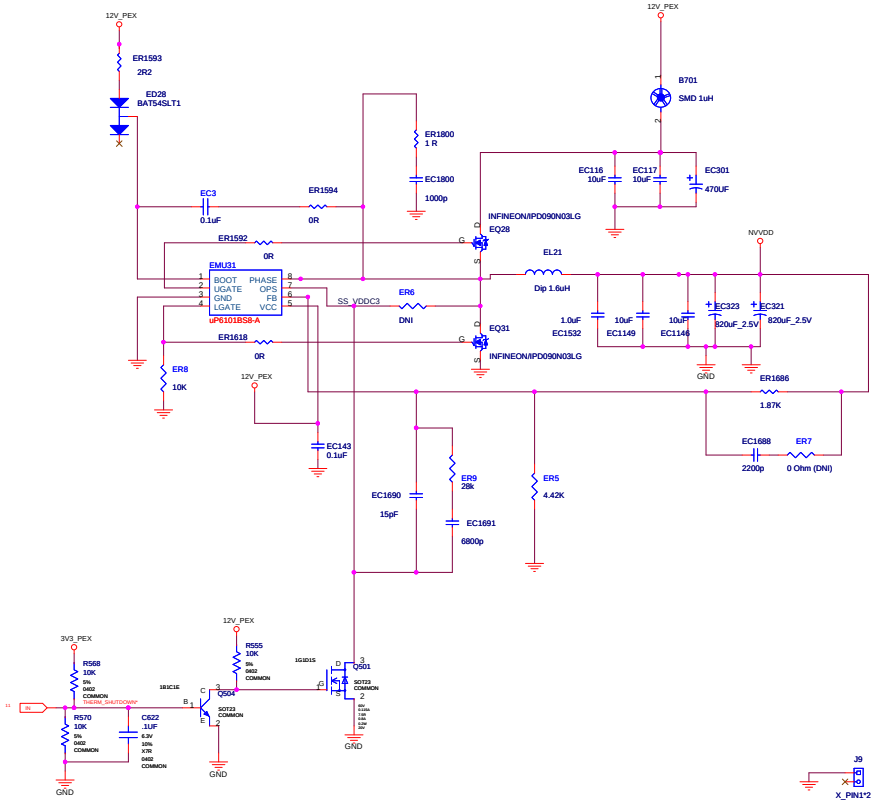
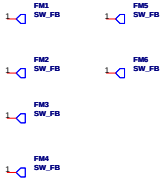
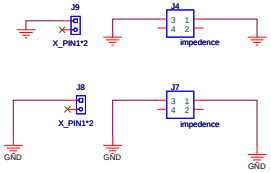
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

Power Supply II: PLLVDD, NVVDD







NVVDD = 0.9V @ 11.1A

NVVDD w/NVVDD=->PEX_VDD = 13.8A
NVVDD = 0.95V @ 12.3A
NVVDD w/NVVDD=->PEX_VDD = 15.0A
NVVDD = 1.0V @ 13.5A
NVVDD w/NVVDD=->PEX_VDD = 16.2A
NVVDD = 1.05V @ 14.8A
NVVDD w/NVVDD=->PEX_VDD = 17.5A

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply II: PLLVDD, NVVDD

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10690-BASE-000 A		
ID		PAGE	
NAME		DATE	01-DEC-2008

Title: Basenet Report
Design: design
Date: Dec 1 21:48:15 2008

Base nets and synonyms for
design_lib.DESIGN(@design_lib.design(sch
_1))
Base Signal Location([Zone][dir])

3V3_F 12.2H
3V3_FUSE 12.2H
3V3_PEX 13.2G
3V3_PROT 11.1H
5V 12.2H
12V_PEX 13.2G
DACA_BLUE 5.1G< 5.4C
DACA_BLUE_C 5.1G> 5.4F> 7.3F<
DACA_GREEN 5.1G< 5.4C
DACA_GREEN_C 5.1G> 5.4F> 7.3F<
DACA_HSYNC 5.1G< 5.4C
DACA_HSYNC_C 5.1G> 5.3F> 7.4F<
DACA_HS_BUF 5.1G< 5.3D
DACA_RED 5.1G< 5.4C
DACA_RED_C 5.1G> 5.4F> 7.3F<
DACA_RSET 5.2G< 5.4B
DACA_VREF 5.2G< 5.4B
DACA_VSYNC 5.1G< 5.4C
DACA_VSYNC_C 5.1G> 5.3F> 7.3F<
DACA_VS_BUF 5.1G< 5.3D
DACB_BLUE 6.1G< 6.4C
DACB_BLUE_C 6.1G< 6.5E
DACB_GREEN 6.1G< 6.4C
DACB_GREEN_C 6.1G< 6.4E
DACB_HSYNC 6.1G< 6.4C
DACB_HSYNC_C 6.1G< 6.3E
DACB_HS_BUF 6.1G< 6.3D
DACB_RED 6.1G< 6.4C
DACB_RED_C 6.1G< 6.4E
DACB_RSET 6.2G< 6.4B
DACB_VREF 6.2G< 6.4B
DACB_VSYNC 6.1G< 6.4C
DACB_VSYNC_C 6.1G< 6.3E
DACB_VS_BUF 6.1G< 6.3D
DDC_5V 12.2H
DP_MODE* 8.1F< 8.2F
DP_MODE_C 8.1F< 8.3G
FBA_CLK0 3.1G> 3.4D> 4.2A< 4.2B< 4.4A<
FBA_CLK0* 3.1G> 3.4D> 4.2A< 4.2B< 4.5A<
FBA_CLK1 3.1G> 3.4D> 4.2D< 4.2F< 4.5A<
FBA_CLK1* 3.1G> 3.4D> 4.2D< 4.2F< 4.5A<
FBA_CMD<0> 3.2C 3.2G 4.1A 4.1C
FBA_CMD<30..0> 3.1G> 3.2D> 4.1A<>
FBA_CMD<1> 3.2C 3.2G 4.1A 4.1C 4.1E 4.1F
FBA_CMD<2> 3.2C 3.2H 4.1A 4.1C
FBA_CMD<3> 3.2C 3.2H 4.2A 4.2C 4.2E 4.2F
FBA_CMD<4> 3.2C 3.3G 4.1E 4.1F
FBA_CMD<5> 3.3C 3.3G 4.1E 4.1F
FBA_CMD<6> 3.3C 3.3H 4.1E 4.1F
FBA_CMD<7> 3.3C 3.3F 4.2E 4.2F
FBA_CMD<8> 3.3C 3.3H 4.1E 4.1F
FBA_CMD<9> 3.3C 3.3E 4.2A 4.2C 4.2E 4.2F
FBA_CMD<10> 3.3C 3.3E 4.1A 4.1C 4.1E 4.1F
FBA_CMD<11> 3.3C 3.3F 4.1A 4.1C 4.1E 4.1F
FBA_CMD<12> 3.3C 3.3F 4.2A 4.2C 4.2E 4.2F
FBA_CMD<13> 3.3C 3.3G 4.1E 4.1F
FBA_CMD<14> 3.3C 3.3G 4.2A 4.2C 4.2E 4.2F
FBA_CMD<15> 3.2E 3.3C 4.3A 4.3C 4.3E 4.3F
FBA_CMD<16> 3.3C 3.3H 4.2A 4.2C 4.2E 4.2F
FBA_CMD<17> 3.3C 3.3H 4.2A 4.2C 4.2E 4.2F
FBA_CMD<18> 3.2F 3.3C 4.2A 4.2C
FBA_CMD<19> 3.3C 3.4E 4.1A 4.1C 4.1E 4.1F
FBA_CMD<20> 3.3C 3.4E 4.2A 4.2C 4.2E 4.2F
FBA_CMD<21> 3.3C 3.4F 4.2A 4.2C 4.2E 4.2F
FBA_CMD<22> 3.3C 3.4F 4.1A 4.1C
FBA_CMD<23> 3.3C 3.4G 4.2A 4.2C 4.2E 4.2F
FBA_CMD<24> 3.3C 3.4G 4.1A 4.1C
FBA_CMD<25> 3.3C 3.4H 4.1A 4.1C 4.1E 4.1F

FBA_CMD<26> 3.3C 3.4H 4.2A 4.2C 4.2E 4.2F
FBA_CMD<27> 3.3C 3.4H 4.2A 4.2C 4.2E 4.2F
FBA_CMD<28> 3.3C 3.3E 4.3E 4.3F
FBA_CMD<29> 3.3C 3.4H 4.1A 4.1C
FBA_CMD<30> 3.2E 3.3C 4.3A 4.3C
FBA_D<0> 3.1B 4.4B
FBA_D<63..0> 3.1A<> 3.1G<> 4.4A<>
FBA_D<1> 3.1B 4.4B
FBA_D<2> 3.1B 4.4B
FBA_D<3> 3.1B 4.4B
FBA_D<4> 3.1B 4.4B
FBA_D<5> 3.1B 4.4B
FBA_D<6> 3.1B 4.4B
FBA_D<7> 3.1B 4.4B
FBA_D<8> 3.1B 4.4B
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FBA_D<11> 3.2B 4.5B
FBA_D<12> 3.2B 4.5B
FBA_D<13> 3.2B 4.5B
FBA_D<14> 3.2B 4.5B
FBA_D<15> 3.2B 4.5B
FBA_D<16> 3.2B 4.4C
FBA_D<17> 3.2B 4.4C
FBA_D<18> 3.2B 4.4C
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FBA_D<21> 3.2B 4.4C
FBA_D<22> 3.2B 4.4C
FBA_D<23> 3.2B 4.4C
FBA_D<24> 3.2B 4.4C
FBA_D<25> 3.2B 4.5C
FBA_D<26> 3.2B 4.5C
FBA_D<27> 3.2B 4.5C
FBA_D<28> 3.2B 4.5C
FBA_D<29> 3.2B 4.5C
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FBA_D<31> 3.2B 4.5C
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FBA_D<34> 3.2B 4.4D
FBA_D<35> 3.2B 4.4D
FBA_D<36> 3.2B 4.4D
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FBA_D<39> 3.2B 4.4D
FBA_D<40> 3.2B 4.4D
FBA_D<41> 3.3B 4.5D
FBA_D<42> 3.3B 4.5D
FBA_D<43> 3.3B 4.5D
FBA_D<44> 3.3B 4.5D
FBA_D<45> 3.3B 4.5D
FBA_D<46> 3.3B 4.5D
FBA_D<47> 3.3B 4.5D
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FBA_D<54> 3.3B 4.4E
FBA_D<55> 3.3B 4.4E
FBA_D<56> 3.3B 4.4E
FBA_D<57> 3.3B 4.5E
FBA_D<58> 3.3B 4.5E
FBA_D<59> 3.3B 4.5E
FBA_D<60> 3.3B 4.5E
FBA_D<61> 3.3B 4.5E
FBA_D<62> 3.3B 4.5E
FBA_D<63> 3.3B 4.5E
FBA_DEBUG 3.2G< 3.4C
FBA_DQM<0> 3.3B 4.4B
FBA_DQM<7..0> 3.1G> 3.3A> 4.4A<
FBA_DQM<1> 3.3B 4.5B
FBA_DQM<2> 3.3B 4.4C
FBA_DQM<3> 3.3B 4.5C
FBA_DQM<4> 3.3B 4.4D
FBA_DQM<5> 3.4B 4.5D
FBA_DQM<6> 3.4B 4.4E
FBA_DQM<7> 3.4B 4.5E
FBA_DQS_RN<0> 3.1G 3.4B 4.4B
FBA_DQS_RN<7..0> 3.1G<> 3.4A<> 4.4A<>
FBA_DQS_RN<1> 3.1G 3.4B 4.5B
FBA_DQS_RN<2> 3.1G 3.4B 4.4C
FBA_DQS_RN<3> 3.1G 3.4B 4.5C
FBA_DQS_RN<4> 3.1G 3.4B 4.4D
FBA_DQS_RN<5> 3.1G 3.4B 4.5D
FBA_DQS_RN<6> 3.1G 3.4B 4.4E
FBA_DQS_RN<7> 3.1G 3.4B 4.5E
FBA_DQS_WP<0> 3.1G 3.4B 4.4B
FBA_DQS_WP<7..0> 3.1G<> 3.4A<> 4.4A<>
FBA_DQS_WP<1> 3.1G 3.4B 4.5B
FBA_DQS_WP<2> 3.1G 3.4B 4.4C
FBA_DQS_WP<3> 3.1G 3.4B 4.5C

FBA_DQS_WP<4> 3.1G 3.4B 4.4D
FBA_DQS_WP<5> 3.1G 3.4B 4.5D
FBA_DQS_WP<6> 3.1G 3.4B 4.4E
FBA_DQS_WP<7> 3.1G 3.4B 4.5E
FBA_DQS_WP<7..0> 3.1G 3.4B 4.5E
FBA_ZQ0 4.1G< 4.3A
FBA_ZQ1 4.1G< 4.3C
FBA_ZQ2 4.1G< 4.3E
FBA_ZQ3 4.1G< 4.3F
FBVDDQ 12.2H
FB_CAL_PD_VDDQ 3.2G< 3.4C
FB_CAL_PU_GND 3.2G< 3.4C
FB_CAL_TERM_GND 3.2G<
FB_PLLAVDD 3.2G< 3.5C
FB_VREF_A 4.1G< 4.3D
FB_VREF_A_Q 4.1G<
FB_VREF_B 4.1G< 4.3H
FB_VREF_B_Q 4.1G<
GPIO0_DVI_A_HPD 7.1G< 7.4D
GPIO0_DVI_A_HPD_C 7.1G< 7.3F
GPIO0_DVI_A_HPD_R 7.1G< 7.4E
GPIO4_FAN_TACH 9.1G< 9.4D> 10.2E<
GPIO5_NVVDDCTL 10.2E> 13.1G< 13.5D<
GPIO5_NVVDDCTL_R 13.4E
GPIO8_THERM_OVERT* 10.2E> 11.1G< 11.2D<
GPIO9_FAN_PWM 9.1G> 9.4D< 10.2E>
GPIO19_IFPD_HPD 8.1F< 8.4D
GPIO_DP_HPD_C 8.1F< 8.4F
GPIO_DP_HPD_R 8.1F< 8.4E
GPU_PLLVDD 10.1F< 10.4C
GPU_TESTMODE 10.1G< 10.4E
I2CA_SCL 5.1G< 5.2C< 10.2E>
I2CA_SCL_C 5.1F> 5.1G> 7.3F<
I2CA_SDA 5.1G<> 5.2C<> 10.2E<>
I2CA_SDA_C 5.1G<> 5.2F<> 7.3F<>
I2CB_SCL 6.1G< 6.2C< 10.2E>
I2CB_SCL_C 6.1G< 6.2E
I2CB_SDA 6.1G<> 6.2C<> 10.2E<>
I2CB_SDA_C 6.1G< 6.2E
I2CC_SCL 10.1G< 10.2E
I2CC_SCL_R 10.1G< 10.2F
I2CC_SDA 10.1G< 10.2E
I2CC_SDA_R 10.1G< 10.2F
I2CH_SCL 10.1G< 10.3E
I2CH_SDA 10.1G< 10.3E
I2CS_SCL 10.1G< 10.2C
I2CS_SDA 10.1G< 10.2C
IFPAB_IOVDD 7.2G< 7.3C
IFPAB_PLLVDD 7.2G< 7.3C
IFPAB_RSET 7.2G< 7.3C
IFPAB_TXC 7.1G< 7.4D
IFPAB_TXC* 7.1G< 7.4D
IFPAB_TXD0 7.1G< 7.3D
IFPAB_TXD0* 7.1G< 7.3D
IFPAB_TXD1 7.1G< 7.3D
IFPAB_TXD1* 7.1G< 7.3D
IFPAB_TXD2 7.1G< 7.3D
IFPAB_TXD2* 7.1G< 7.3D
IFPAB_TXD4 7.1G< 7.3D
IFPAB_TXD4* 7.1G< 7.3D
IFPAB_TXD5 7.1G< 7.3D
IFPAB_TXD5* 7.1G< 7.3D
IFPAB_TXD6 7.1G< 7.3D
IFPAB_TXD6* 7.1G< 7.3D
IFPC_IOVDD 9.1G< 9.3B
IFPC_PLLVDD 9.1G< 9.2B
IFPD_AUX 8.1G< 8.4D
IFPD_AUX* 8.1G< 8.4D
IFPD_AUX_BYP 8.1G< 8.3D
IFPD_AUX_BYP* 8.1G< 8.2D
IFPD_AUX_C 8.1G< 8.4F
IFPD_AUX_C* 8.1G< 8.4F
IFPD_AUX_SEL 8.1F< 8.2D
IFPD_IOVDD 8.1F> 8.4C> 9.3A<
IFPD_L0 8.1G< 8.4D
IFPD_L0* 8.1G< 8.4D
IFPD_L0_C 8.1G< 8.4F
IFPD_L0_C* 8.1G< 8.4F
IFPD_L1 8.1G< 8.4D
IFPD_L1* 8.1G< 8.4D
IFPD_L1_C 8.1G< 8.4F
IFPD_L1_C* 8.1G< 8.4F
IFPD_L2 8.1G< 8.4D
IFPD_L2* 8.1G< 8.4D
IFPD_L2_C 8.1G< 8.4F
IFPD_L2_C* 8.1G< 8.4F
IFPD_L3 8.1G< 8.4D
IFPD_L3* 8.1G< 8.4D
IFPD_L3_C 8.1G< 8.4F
IFPD_L3_C* 8.1G< 8.4F
IFPD_PLLVDD 8.1F> 8.3C> 9.2A<
IFPD_RSET 8.1F< 8.4B
JTAG_TCLK 10.1G< 10.2C
JTAG_TDI 10.1G< 10.2C
JTAG_TDO 10.2C 10.2G<
JTAG_TMS 10.1G< 10.2C
JTAG_TRST* 10.2C 10.2G<

NVVDD 13.2G
NVVDD_SENSE 2.4G> 13.1G< 13.4G<
NVVDD_SENSE_R 13.1G> 13.4F
PEX_CLKREQ* 2.1E 2.1G<
PEX_PLL 13.2G
PEX_PLLVDD 2.1G< 2.5F
PEX_PRSNT 2.1C 2.1G<
PEX_REFCLK 2.2D 2.5A<
PEX_REFCLK* 2.2D 2.5A<
PEX_RST 11.1G< 11.3C
PEX_RST* 2.2D> 11.1G< 11.2E<
PEX_RST_R* 11.1G< 11.2F
PEX_RX0 2.2D 2.4A<
PEX_RX0* 2.2D 2.4A<
PEX_RX1 2.2D 2.4A<
PEX_RX1* 2.2D 2.4A<
PEX_RX2 2.2D 2.4A<
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PEX_RX13 2.5A< 2.5D
PEX_RX13* 2.5A< 2.5D
PEX_RX14 2.5A< 2.5D
PEX_RX14* 2.5A< 2.5D
PEX_RX15 2.5A< 2.5D
PEX_RX15* 2.5A< 2.5D
PEX_SMCLK 2.1D> 10.1G< 10.3B< 10.3B->
PEX_SMDAT 2.2D<> 10.1G<>
PEX_TCLK 2.1D> 10.2A< 10.2G<
PEX_TDI 2.1D> 10.2A< 10.2G<
PEX_TDO 2.1D< 10.2A> 10.2G>
PEX_TERMP 2.1G< 2.5F
PEX_TMS 2.1D> 10.2A< 10.2G<
PEX_TRST* 2.1D> 10.2A< 10.2G<
PEX_TSTCLK 2.5A<
PEX_TSTCLK* 2.5A<
PEX_TSTCLK_OUT 2.2E
PEX_TSTCLK_OUT* 2.2E
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PEX_TX1* 2.2A< 2.2E
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PEX_TX4* 2.2A< 2.3E
PEX_TX5 2.2A< 2.3E
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PEX_TX7 2.2A< 2.3E
PEX_TX7* 2.2A< 2.3E
PEX_TX8 2.2A< 2.4E
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PEX_TX9 2.3A< 2.4E
PEX_TX9* 2.3A< 2.4E
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PEX_TXI2* 2.2D 2.3A<
PEX_TXI3 2.3A< 2.3D

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PEX_TXX4 2.3A< 2.3D
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PEX_TXX5* 2.3A< 2.3D
PEX_TXX6 2.3A< 2.3D
PEX_TXX6* 2.3A< 2.3D
PEX_TXX7 2.3A< 2.3D
PEX_TXX7* 2.3D 2.4A<
PEX_TXX8 2.4A< 2.4D
PEX_TXX8* 2.4A< 2.4D
PEX_TXX9 2.4A< 2.4D
PEX_TXX9* 2.4A< 2.4D
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PEX_TXX11 2.4A< 2.4D
PEX_TXX11* 2.4A< 2.4D
PEX_TXX12 2.4A< 2.4D
PEX_TXX12* 2.4A< 2.4D
PEX_TXX13 2.4A< 2.5D
PEX_TXX13* 2.4A< 2.5D
PEX_TXX14 2.4A< 2.5D
PEX_TXX14* 2.4A< 2.5D
PEX_TXX15 2.4A< 2.5D
PEX_TXX15* 2.4A< 2.5D
PEX_VDD 12.2H
PS_3V3_FUSE_FAULT 12.1G< 12.3F
PS_3V3_FUSE_ISET 12.1G< 12.3F
PS_3V3_FUSE_SLEW 12.1G< 12.3F
PS_5V_ADJ 12.1G< 12.2B
PS_FBVDDQ_BOOT 12.1G< 12.3E
PS_FBVDDQ_CP 12.1G< 12.4E
PS_FBVDDQ_CP_RC 12.1G< 12.4E
PS_FBVDDQ_EN 12.1G< 12.5C
PS_FBVDDQ_EN* 12.1G< 12.5C
PS_FBVDDQ_FB 12.1G< 12.4E
PS_FBVDDQ_FB_RC 12.1G< 12.4G
PS_FBVDDQ_FS 12.1G< 12.4D
PS_FBVDDQ_LG 12.1G< 12.4E
PS_FBVDDQ_PHASE 12.1G< 12.4E
PS_FBVDDQ_PVCCS 12.1G< 12.3E
PS_FBVDDQ_RC 12.1G< 12.4G
PS_FBVDDQ_UG 12.1G< 12.4E
PS_FBVDDQ_UG_R 12.1G< 12.3F
PS_FBVDDQ_VCC5 12.1G< 12.3D
PS_FBVDDQ_VCC12 12.1G< 12.3E
PS_NVDD_BOOT 13.1G< 13.3C
PS_NVDD_CP 13.1G< 13.3C
PS_NVDD_CP_RC 13.1G< 13.4D
PS_NVDD_EN* 13.1G< 13.4B
PS_NVDD_FB 13.1G< 13.3C
PS_NVDD_FB_RC 13.1G< 13.4F
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PS_NVDD_LDO 13.1G< 13.3C
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PS_PEX_FB 12.1G< 12.4D
PS_PEX_PLL_ADJ 13.1E 13.2G<
ROM_CS* 10.1G< 10.3E
ROM_SCLK 10.3E< 11.1G> 11.4A> 11.4B
ROM_SI 10.3E< 11.1G> 11.3A> 11.3B
ROM_SO 10.3E< 11.1G> 11.3A> 11.3B
ROM_VCC 10.2F
SNN_3V3_AUX 2.1C
SNN_AOZ_7 12.3G
SNN_A_ID0 5.4G
SNN_A_ID2 5.4F
SNN_BUFRST* 10.3E
SNN_CAL_TERM_GND 3.4C
SNN_CEC 10.4E
SNN_DP_CEC 8.4G
SNN_FBA1_NC_A1 4.3A
SNN_FBA1_NC_A11 4.3A
SNN_FBA1_NC_J2 4.2A
SNN_FBA1_NC_J10 4.2A
SNN_FBA1_NC_L2 4.2A
SNN_FBA1_NC_L10 4.2A
SNN_FBA1_NC_M8 4.2A
SNN_FBA1_NC_T1 4.3A
SNN_FBA1_NC_T11 4.3A
SNN_FBA2_NC_A1 4.3C
SNN_FBA2_NC_J2 4.2C
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SNN_FBA3_NC_J10 4.2E
SNN_FBA3_NC_L2 4.2E
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SNN_FBA3_NC_T1 4.3E
SNN_FBA3_NC_T8 4.2E
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SNN_FBA4_NC_A1 4.3F
SNN_FBA4_NC_A11 4.3F
SNN_FBA4_NC_J2 4.2F
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SNN_FBA4_NC_T8 4.2F
SNN_FBA4_NC_T11 4.3F
SNN_FB_VREF 3.5B
SNN_GPIO2 10.2E
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SNN_GPIO7 10.2E
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SNN_GPU_AA6 10.3C
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SNN_GPU_D15 9.2H
SNN_GPU_J5 9.2H
SNN_GPU_N3 10.3C
SNN_GPU_T6 10.3C
SNN_GPU_W6 10.3C
SNN_GPU_Y6 10.3C
SNN_HDCP_2 10.4G
SNN_IFPAB_TXD3 7.3D
SNN_IFPAB_TXD3* 7.3D
SNN_IFPAB_TXD7 7.4D
SNN_IFPAB_TXD7* 7.3D
SNN_IFPB_TXC 7.4D
SNN_IFPB_TXC* 7.4D
SNN_IFPC_AUX 9.3C
SNN_IFPC_AUX* 9.2C
SNN_IFPC_HPD 9.3C
SNN_IFPC_L0 9.3C
SNN_IFPC_L0* 9.3C
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SNN_IFPC_L3 9.3C
SNN_IFPC_L3* 9.3C
SNN_IFPC_RSET 9.2B
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SNN_IFPE_L0 9.4C
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SNN_IFPE_L1* 9.4C
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SNN_IFPE_L2* 9.4C
SNN_IFPE_L3 9.4C
SNN_IFPE_L3* 9.4C
SNN_IFPE_RSET 9.3B
SNN_PEX_WAKE* 2.2D
SNN_PE_PRSNT2_A 2.1C
SNN_PE_PRSNT2_B 2.2C
SNN_PE_PRSNT2_C 2.3C
SNN_PE_RSVD1 2.2C
SNN_PE_RSVD2 2.2C
SNN_PE_RSVD3 2.2C
SNN_PE_RSVD4 2.2C
SNN_PE_RSVD5 2.3C
SNN_PE_RSVD6 2.4C
SNN_PE_RSVD7 2.4C
SPDIF 10.1G< 10.4C
STRAP0 10.3C< 11.1G> 11.5A> 11.5B
STRAP1 10.3C< 11.1G> 11.4A> 11.4B
STRAP2 10.3C< 11.1G> 11.4A> 11.4B
STRAP_REF0 10.1G< 10.3C
STRAP_REF1 10.1G< 10.3C
THERMDA 10.1G< 10.2C
THERMDC 10.1C 10.1G<
THERM_N 11.1G< 11.2C
THERM_N_R 11.1G< 11.2B
THERM_P* 11.1G< 11.2C
THERM_P_Q 11.1G< 11.2B
THERM_SHUTDOWN* 11.1G> 11.2A> 13.4A<
XTALOUTBUFF 10.1F< 10.5E
XTALSSIN 10.1F< 10.5C
XTAL_IN 10.1F< 10.5C
XTAL_OUT 10.1F< 10.5D

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