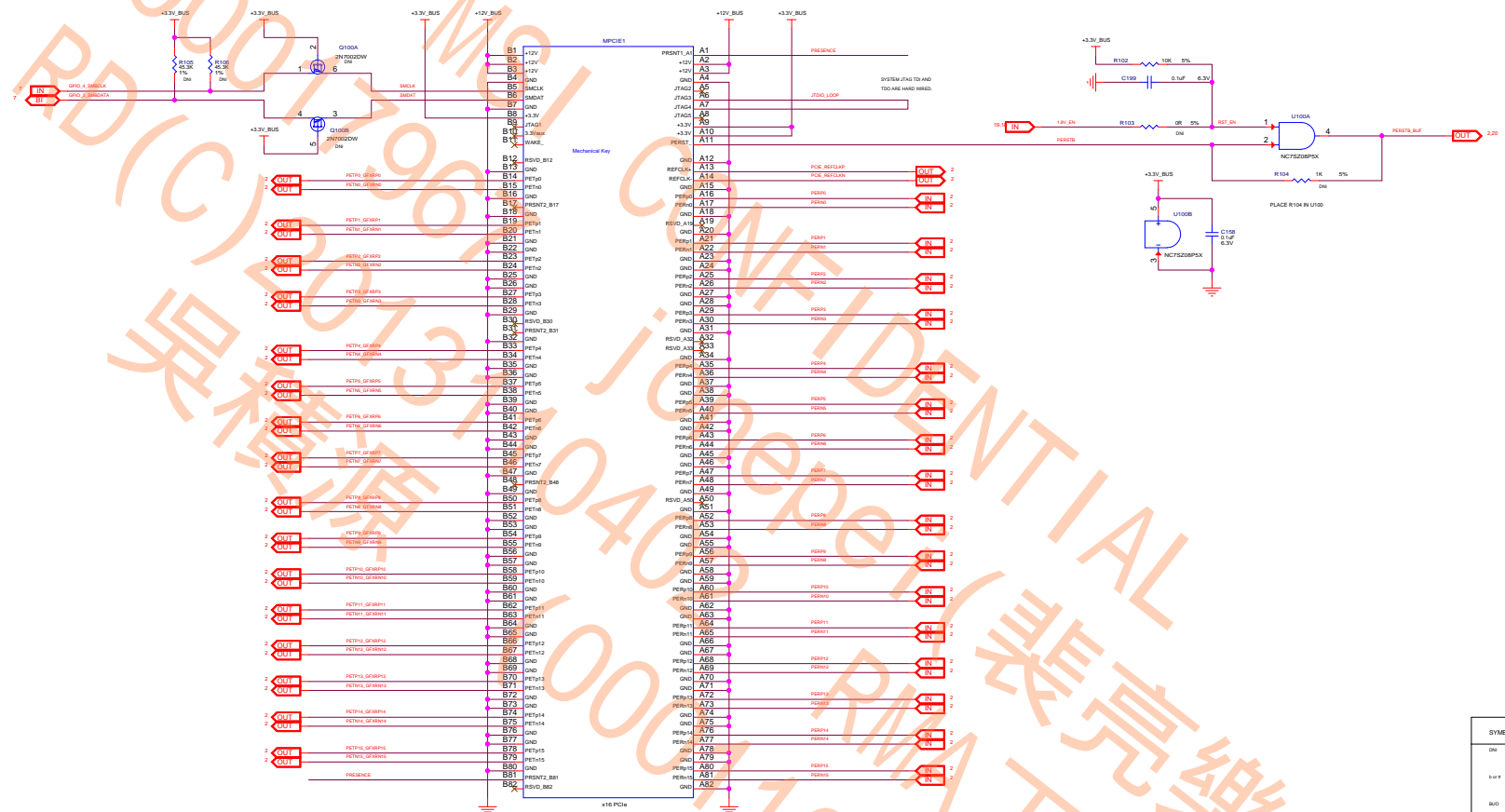
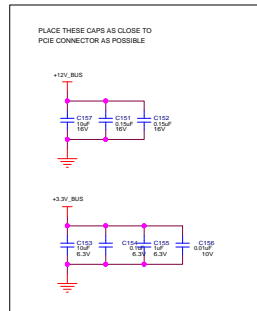


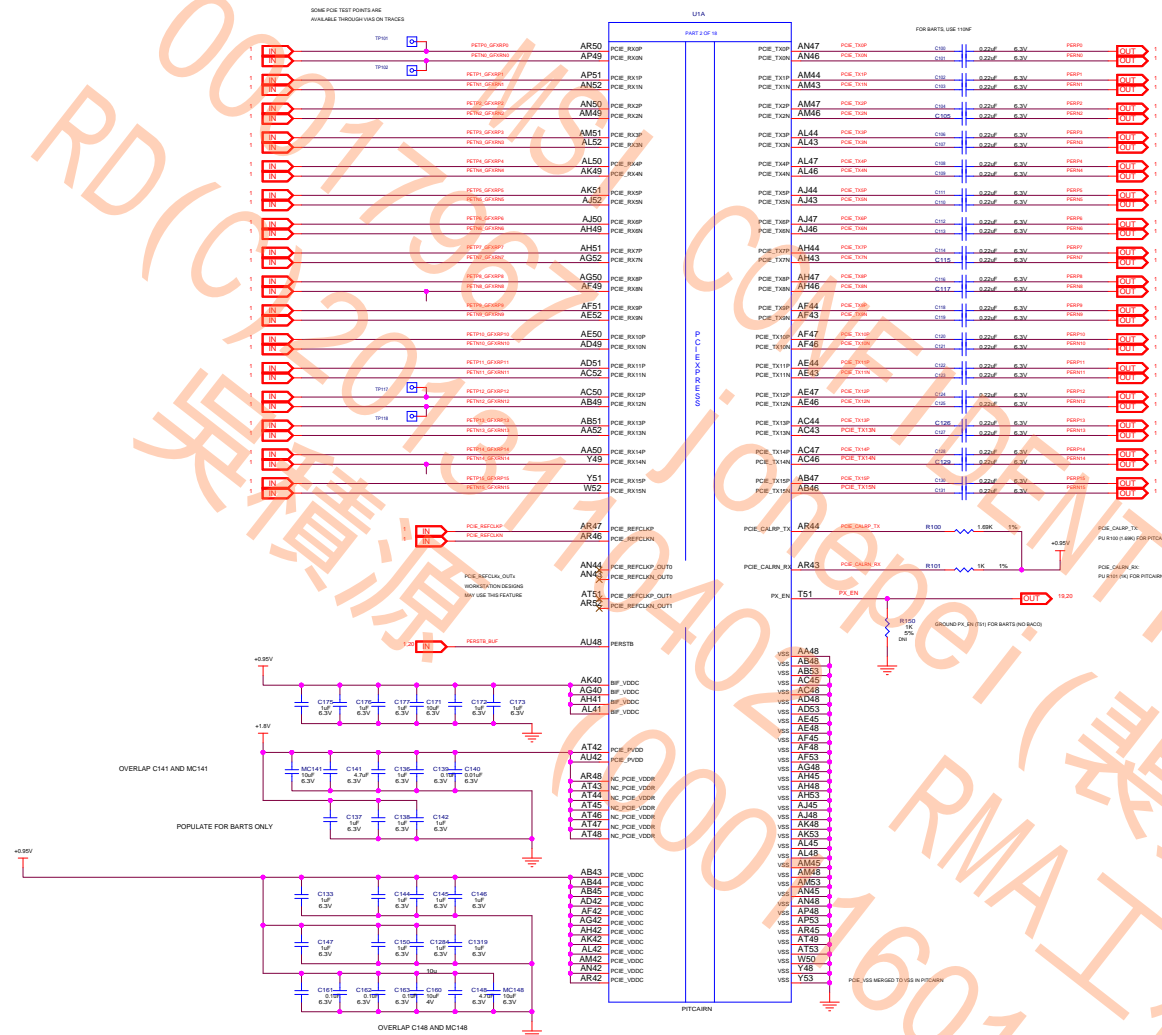


### (1) PCI-EXPRESS EDGE CONNECTOR

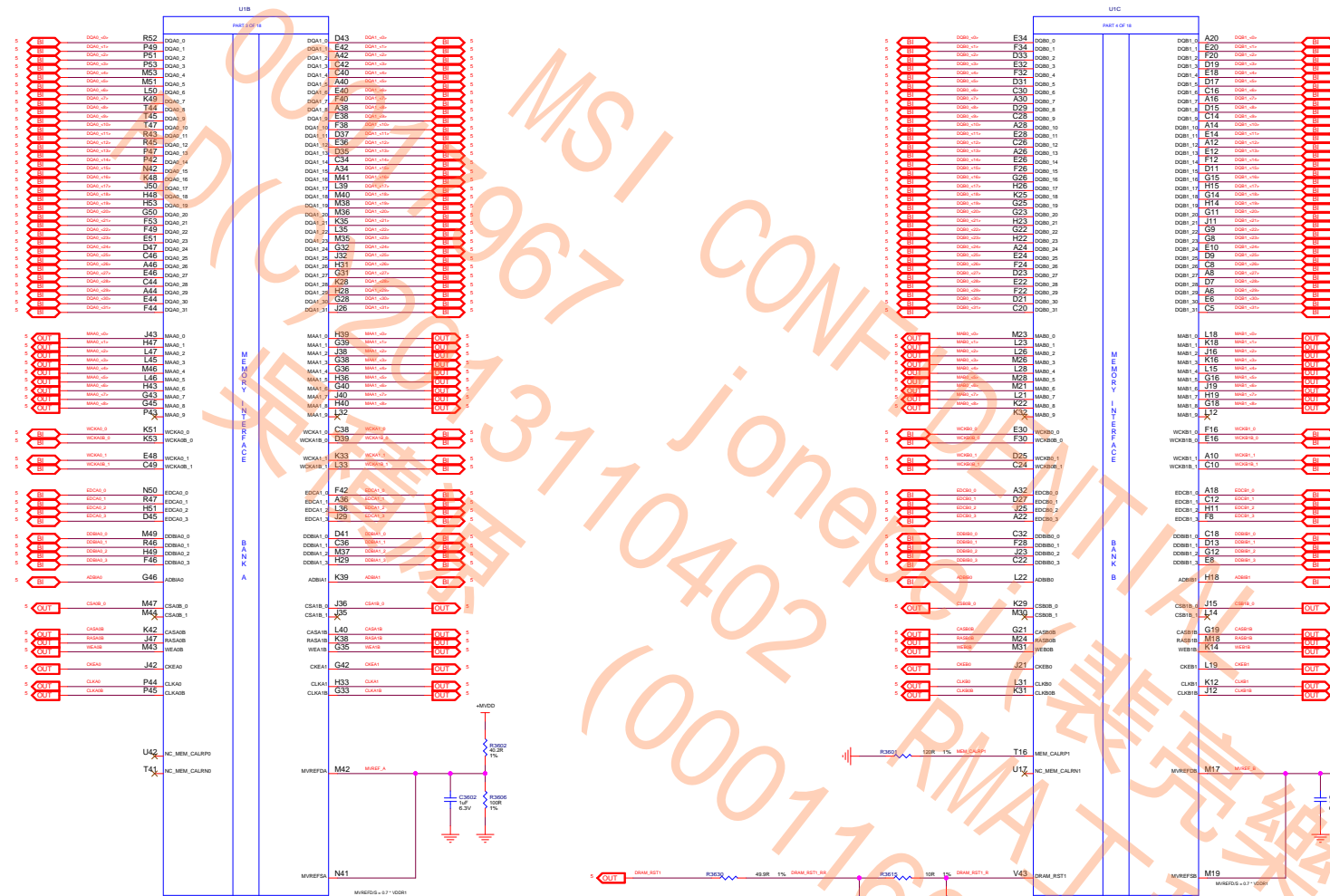


SYMBOL LEGEND	
ONE	DO NOT INSTALL
5-10 IF	ACTIVE LOW
BUD	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

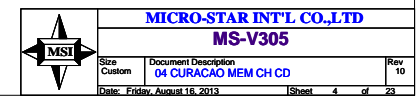
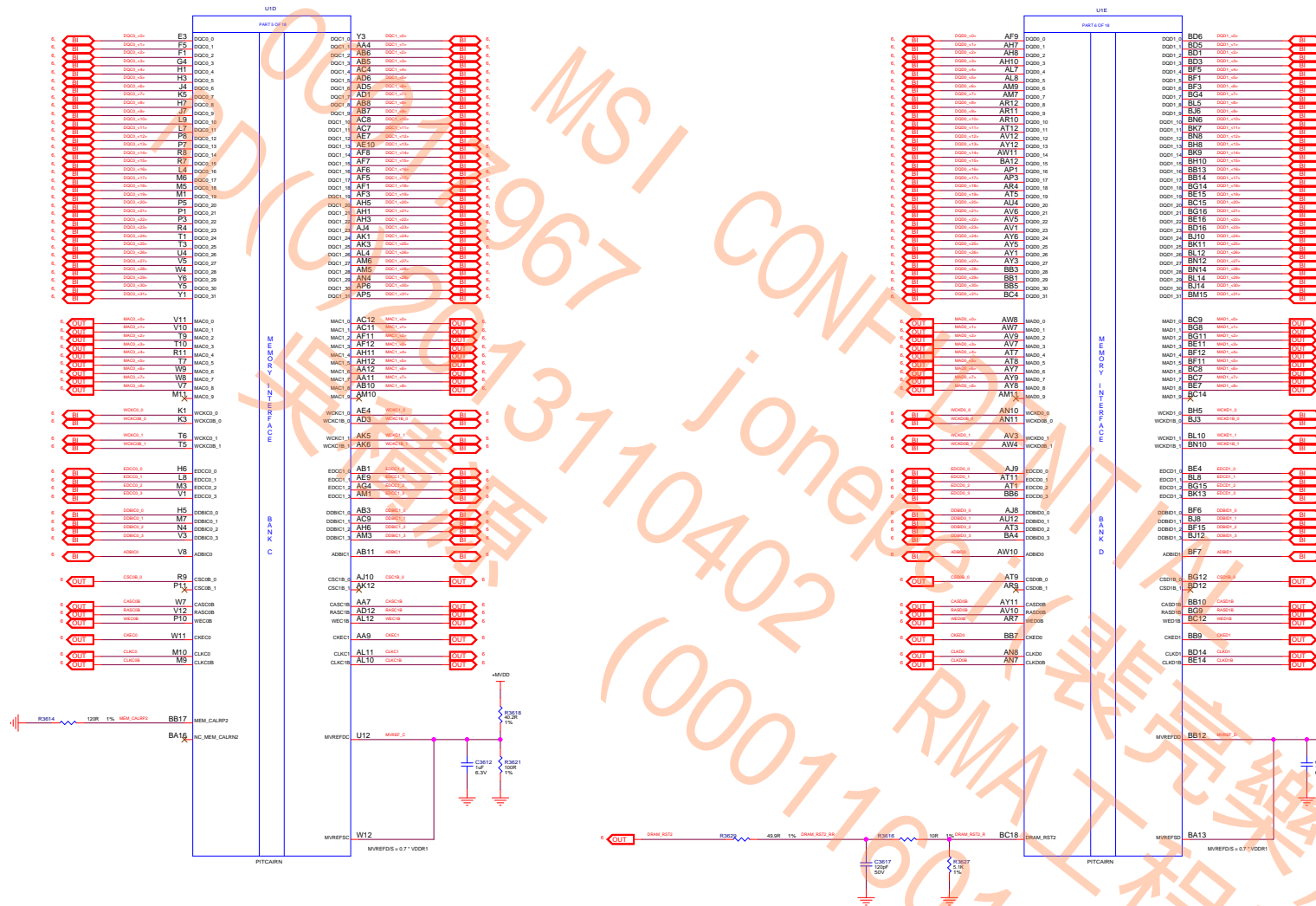
## (2) CURACAO PCIE INTERFACE



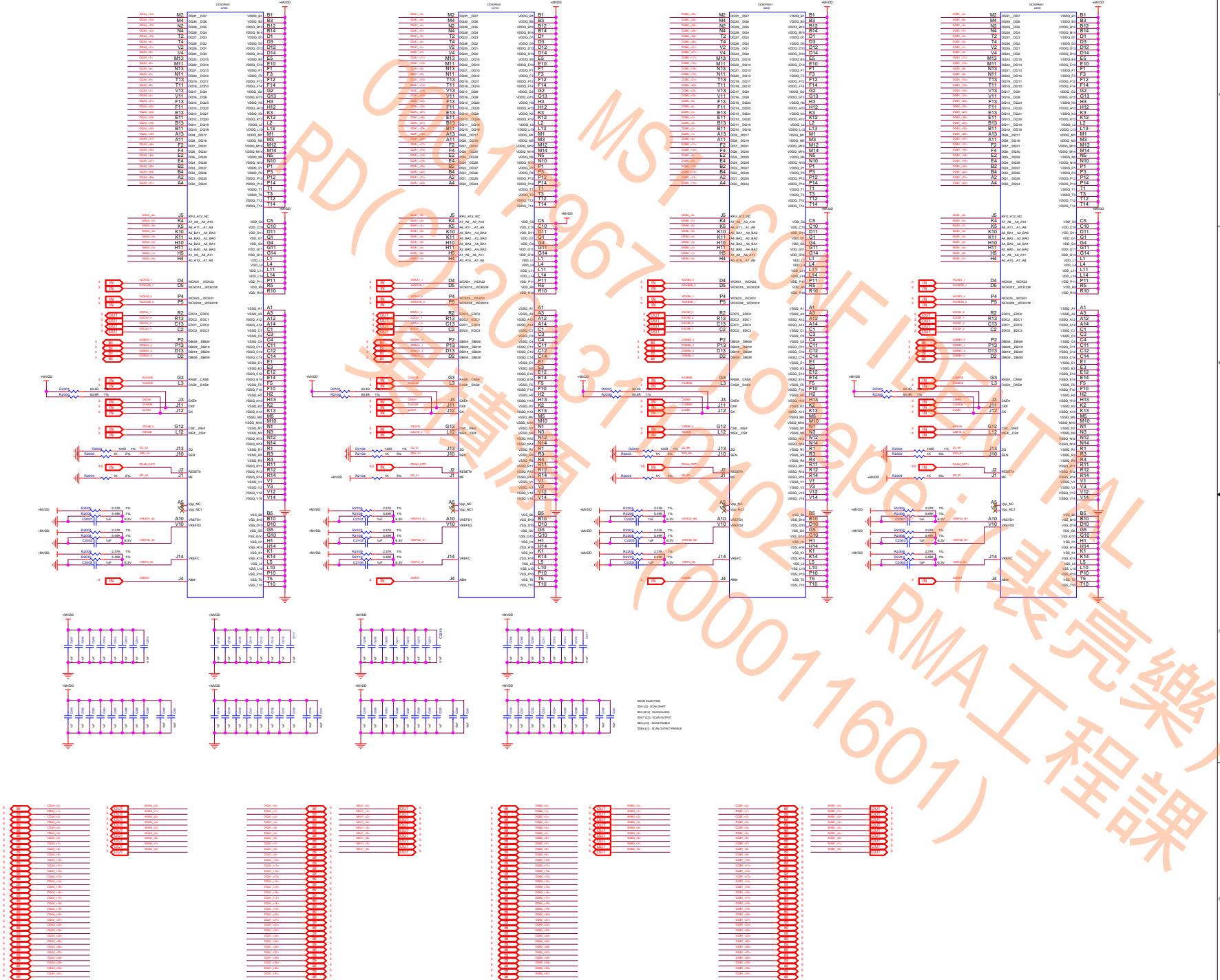
(3) CURACAO MEM INTERFACE CH A/B



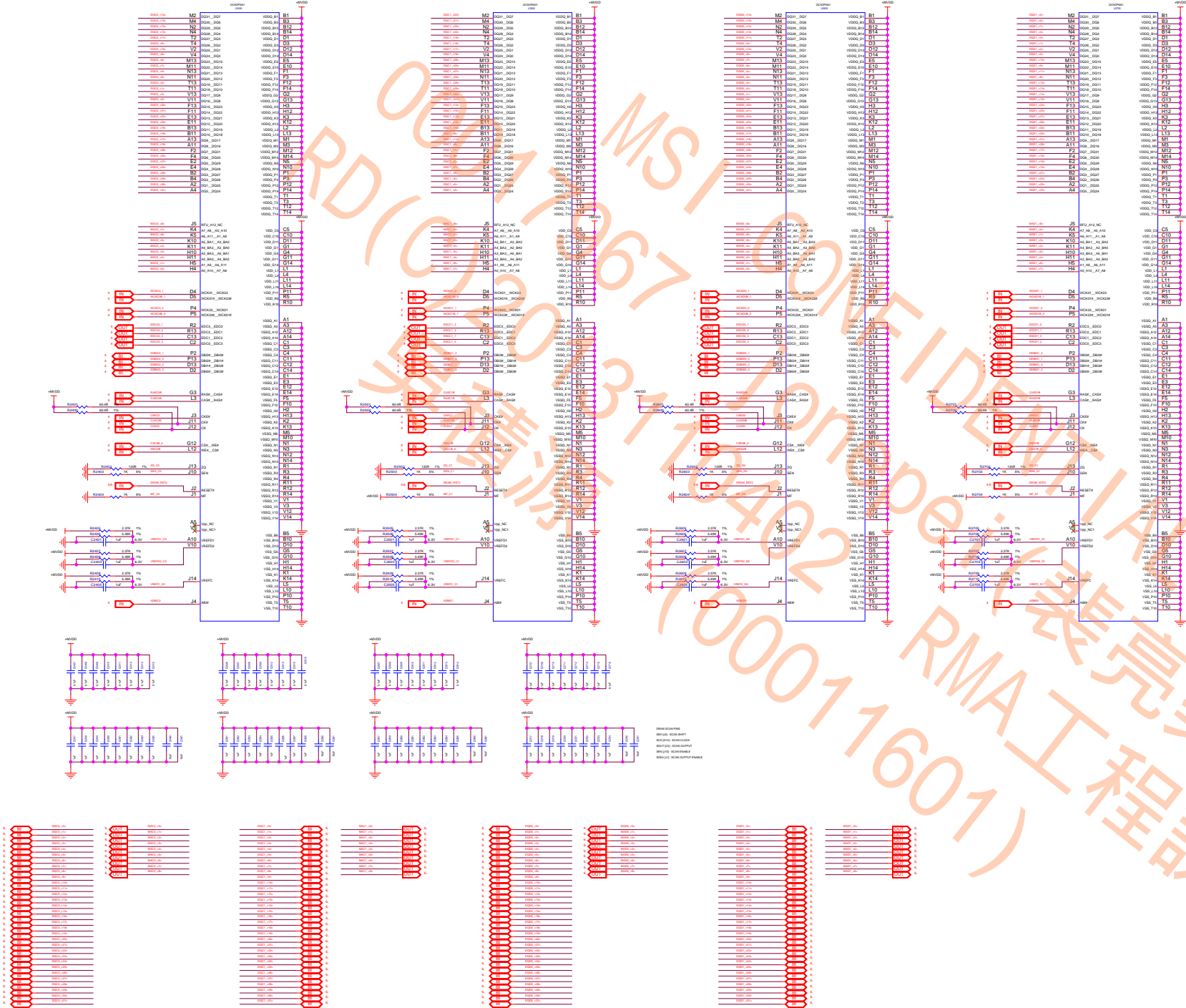
## (4) CURACAO MEM INTERFACE CH C/D



(5) GDDR5 MEMORY CH A/B

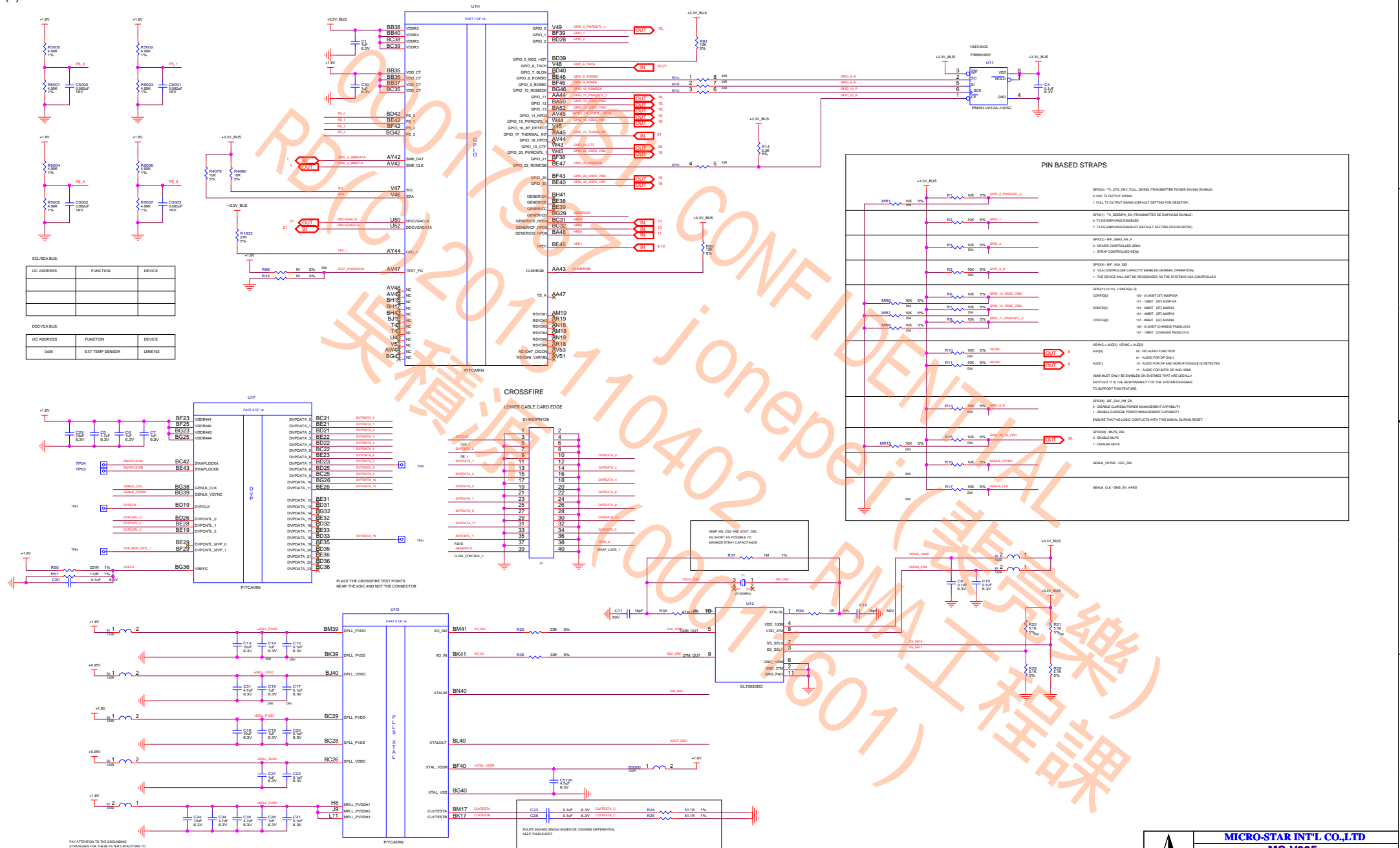


(6) GDDR5 MEMORY CH C/D

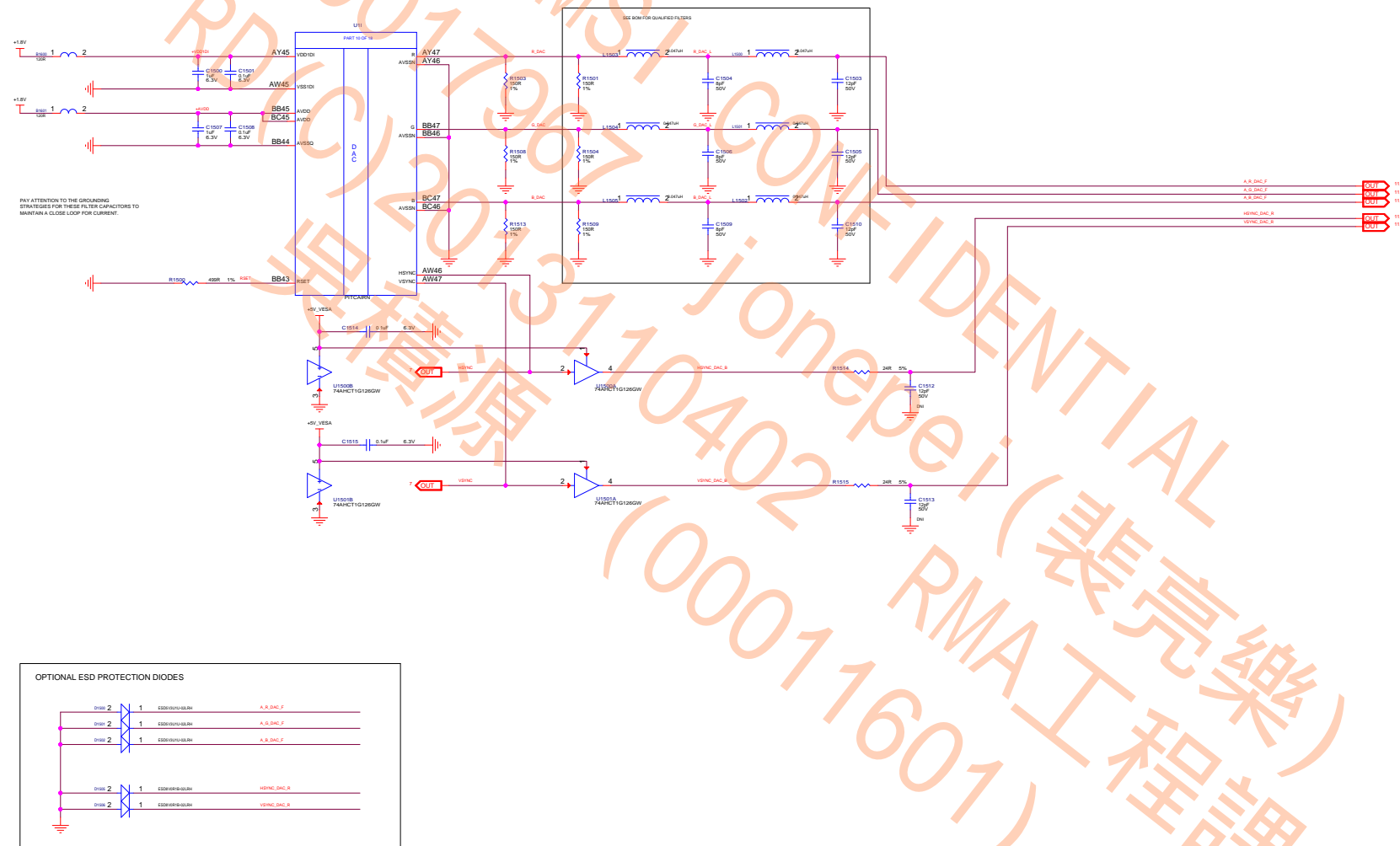




## (7) CURACAO GPIO STRAP CF XTAL

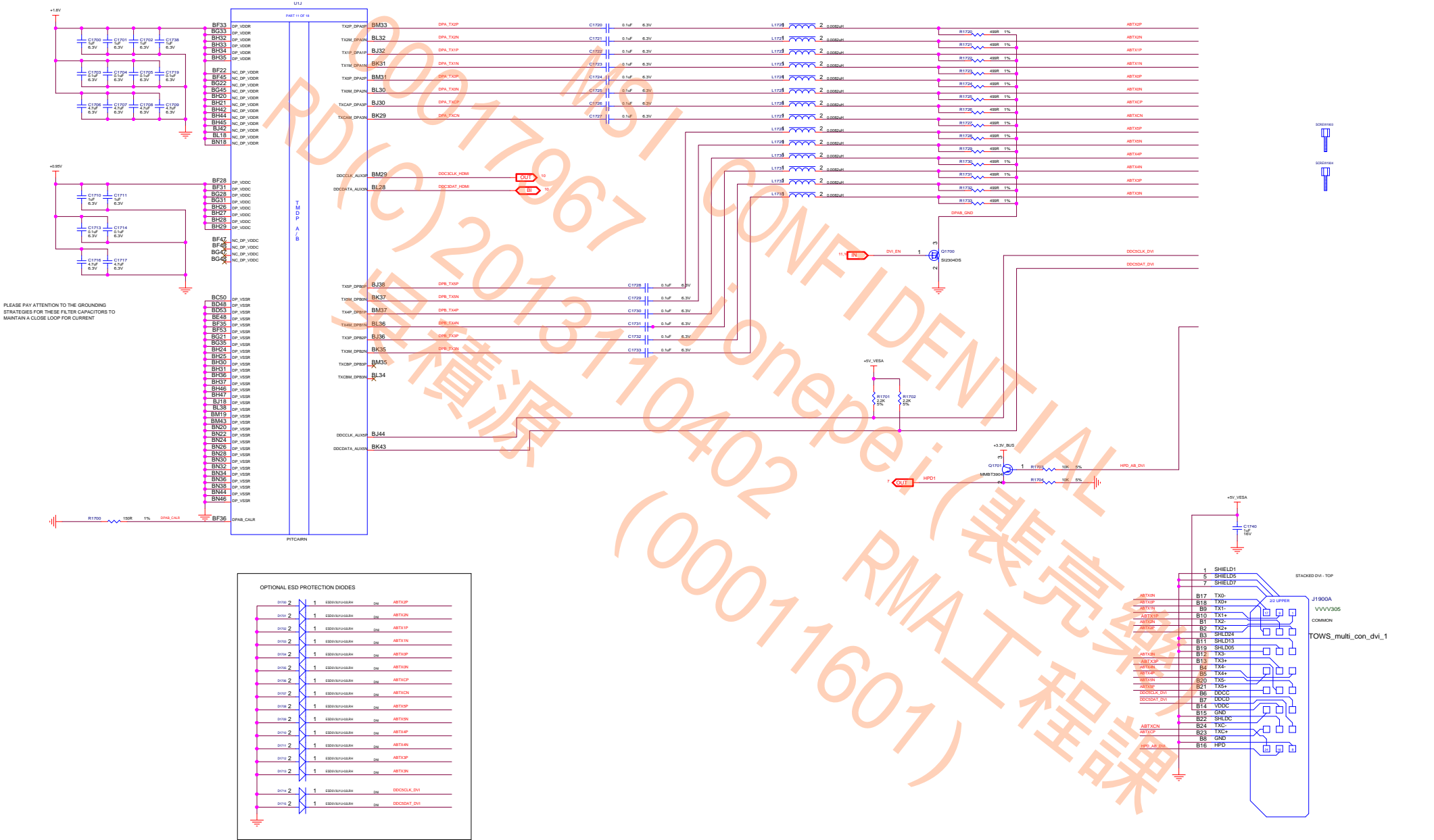


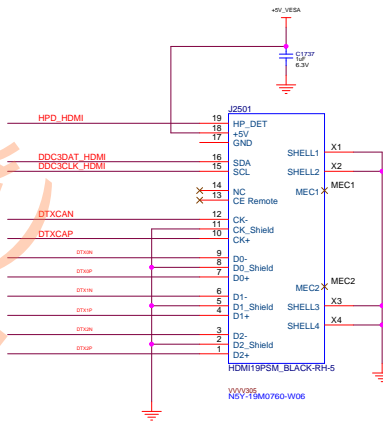
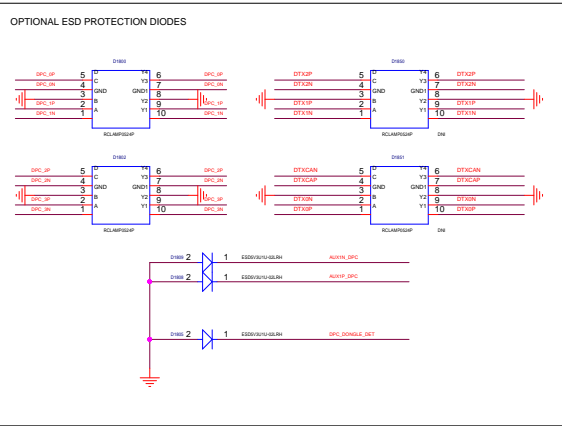
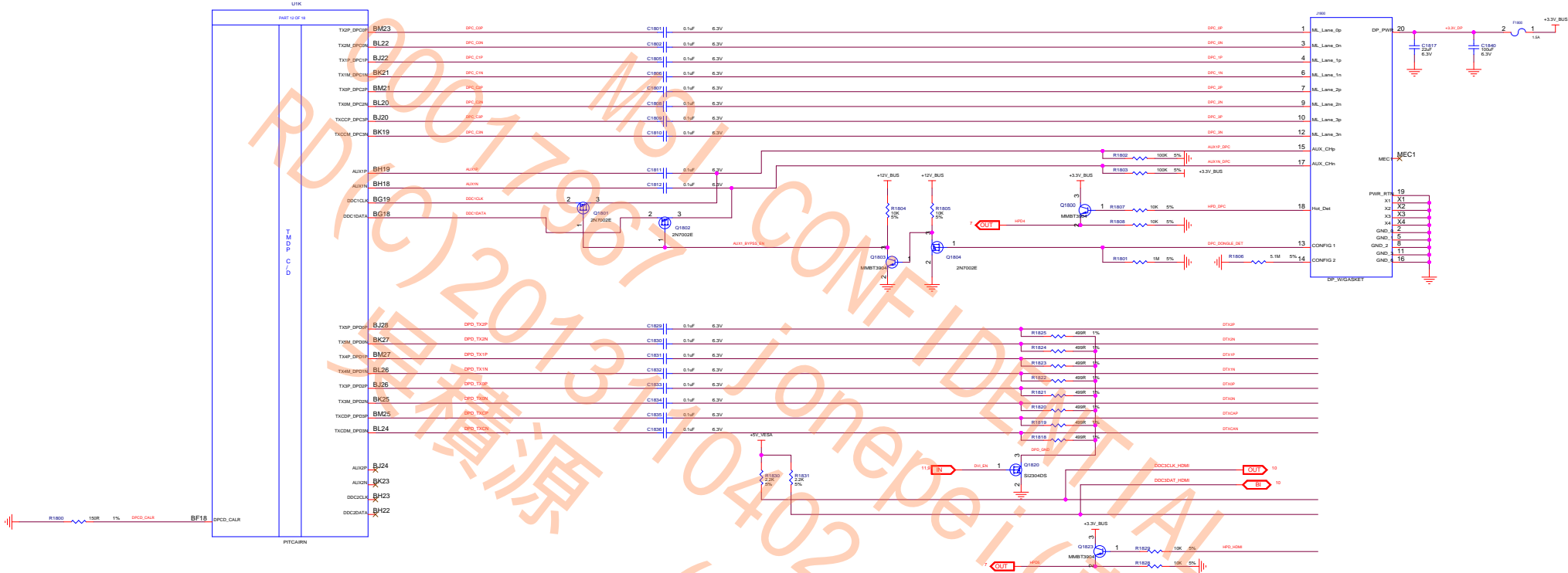
(8) CURACAO DAC1 LOCK

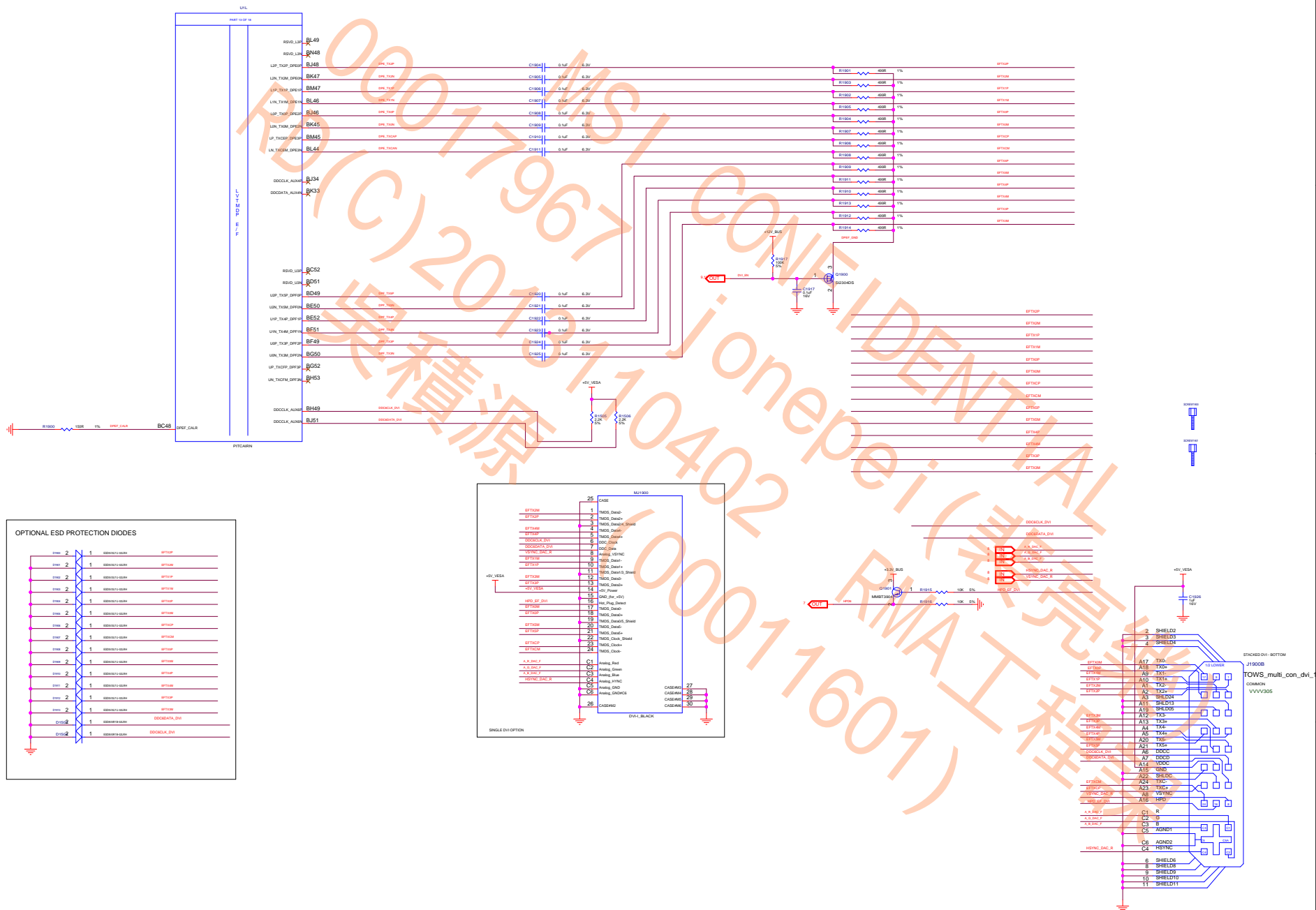




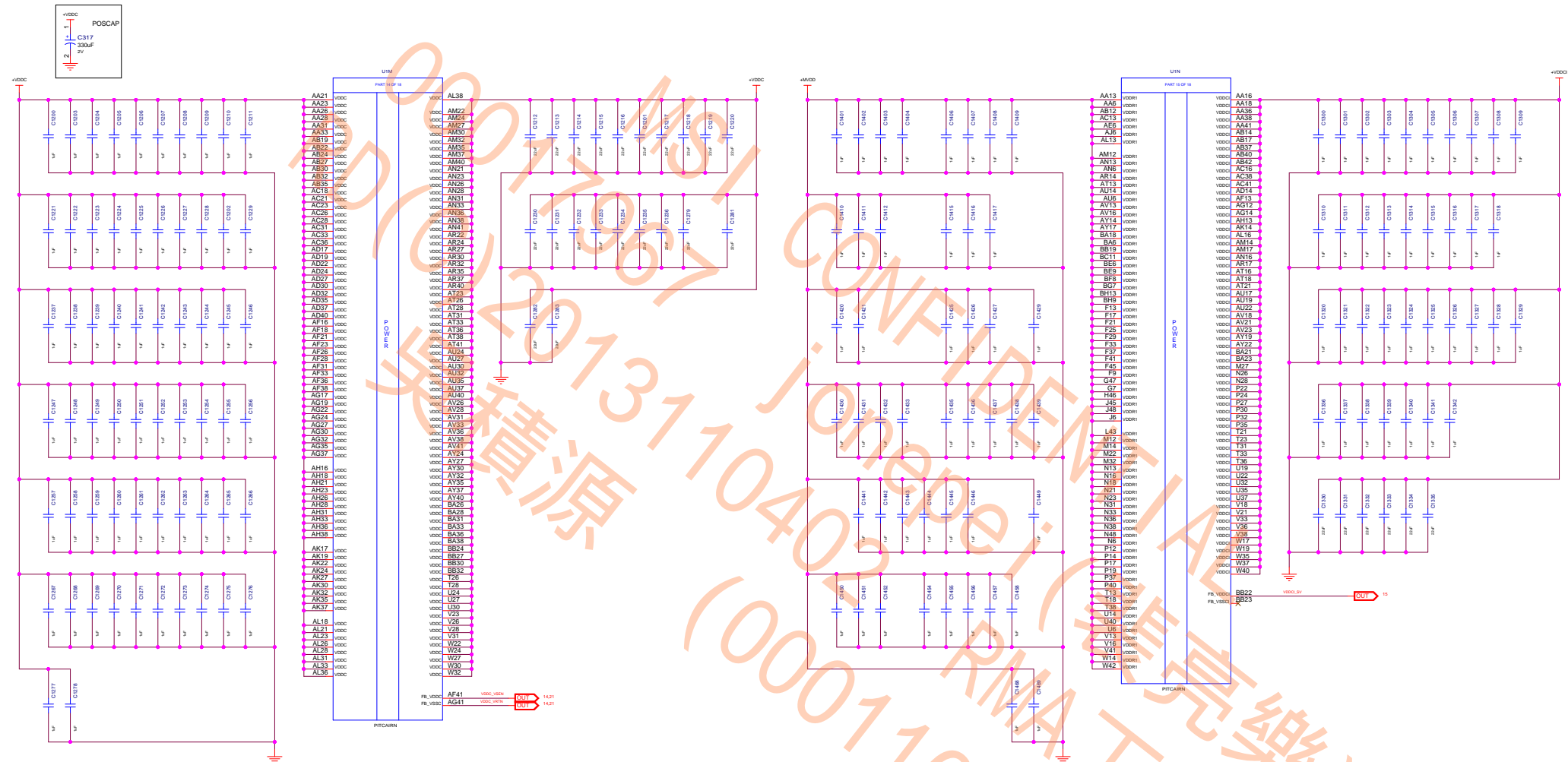
(9) CURACAO TMDP A/B







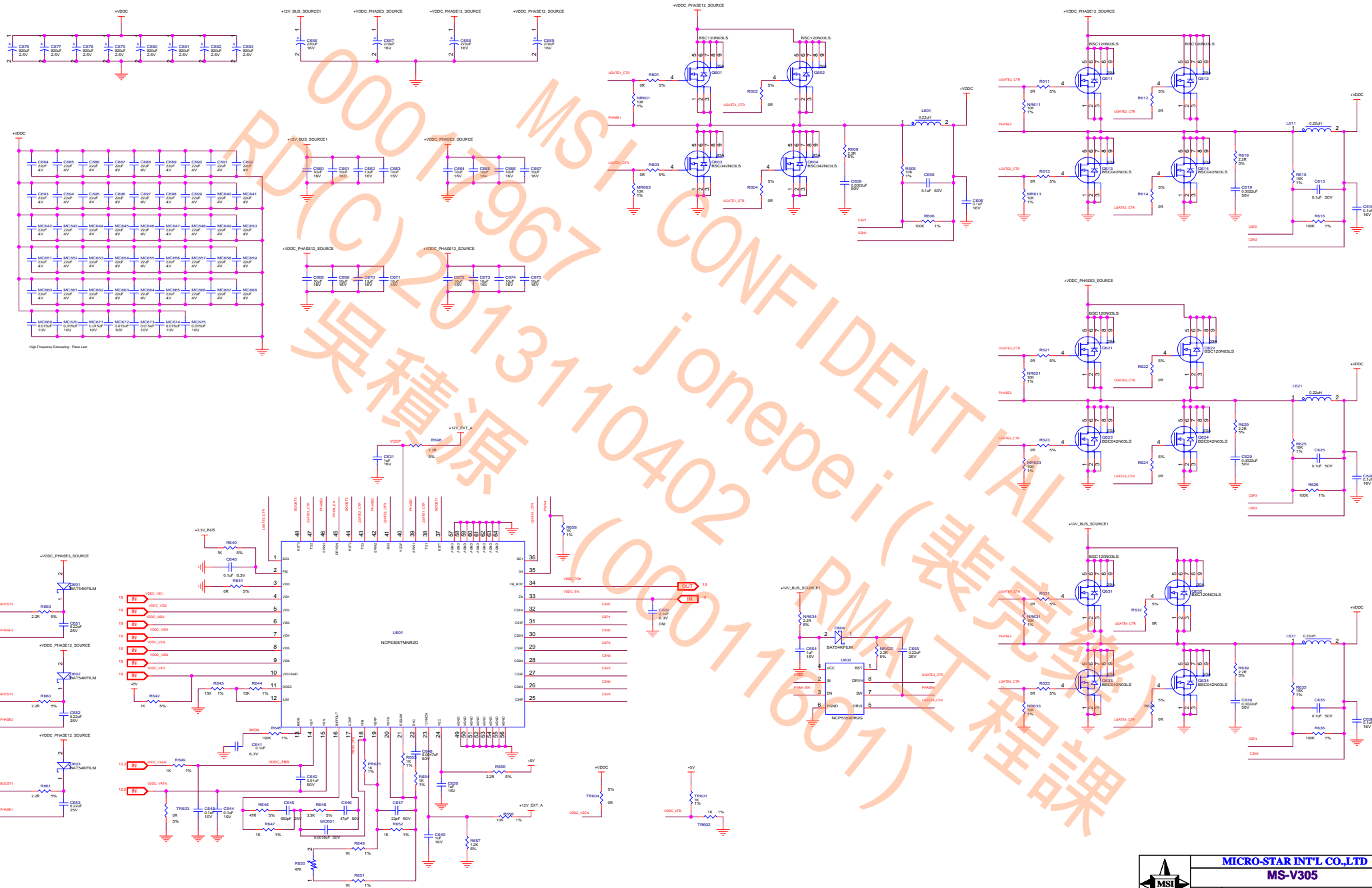
(12) CURACAO POWER

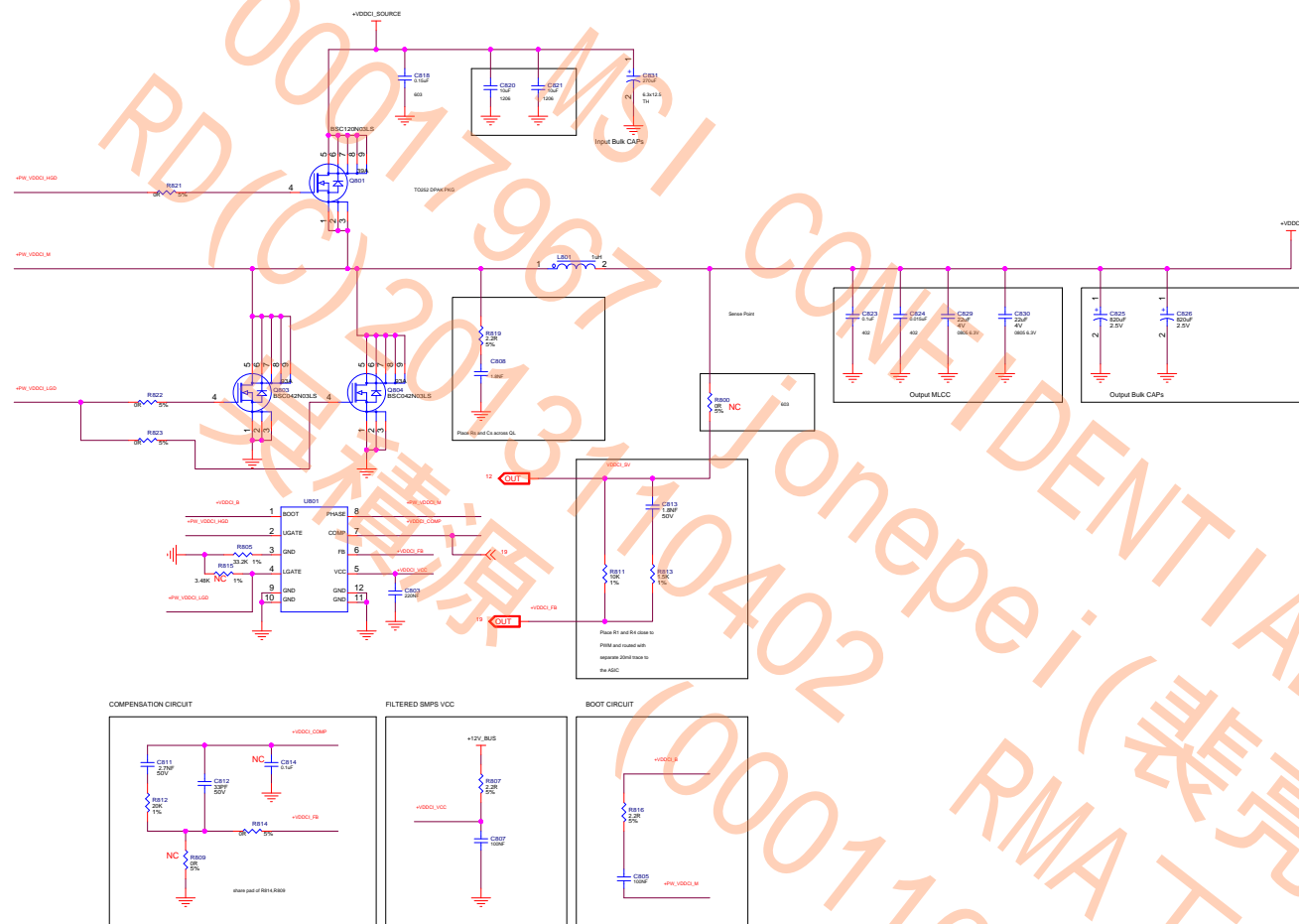


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P007 10-02-18		P007 10-02-18			
A48	V05	BA17	V05	L42	V05
A110	V05	BA19	V05	L25	V05
A115	V05	BA20	V05	L6	V05
A17	V05	BA21	V05		
A22	V05	BA22	V05		
A27	V05	BA23	V05		
A24	V05	BA24	V05		
A27	V05	BA25	V05		
A30	V05	BA26	V05		
A32	V05	BA27	V05		
A33	V05	BA28	V05		
A33	V05	BA29	V05		
A33	V05	BA30	V05		
A33	V05	BA31	V05		
A33	V05	BA32	V05		
A33	V05	BA33	V05		
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A33	V05	BA35	V05		
A33	V05	BA36	V05		
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A33	V05	BA42	V05		
A33	V05	BA43	V05		
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A33	V05	BA45	V05		
A33	V05	BA46	V05		
A33	V05	BA47	V05		
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A33	V05	BA49	V05		
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A33	V05	BA55	V05		
A33	V05	BA56	V05		
A33	V05	BA57	V05		
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A33	V05	BA60	V05		
A33	V05	BA61	V05		
A33	V05	BA62	V05		
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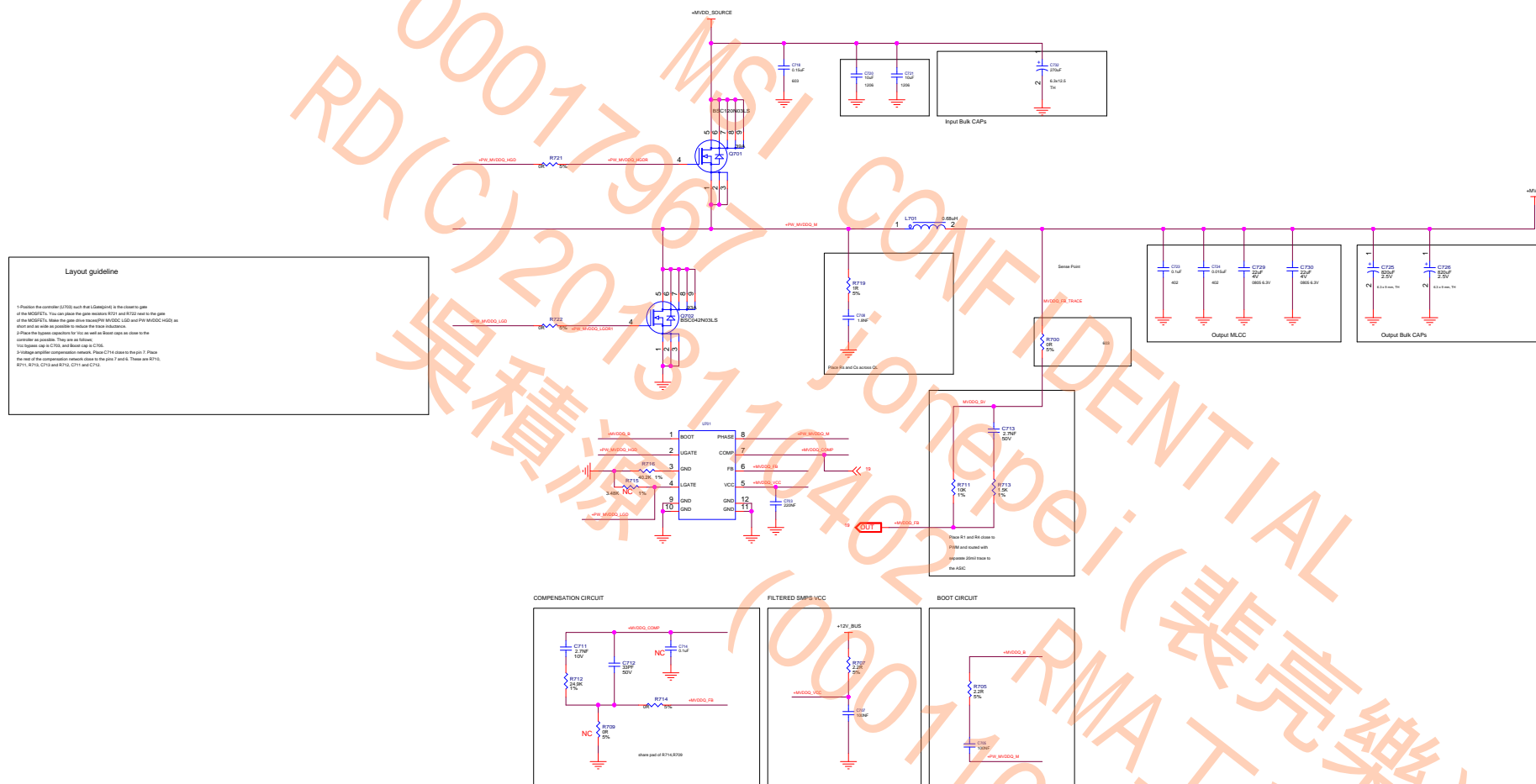


Size Custom	Document Description <b>13 CURACAO GND</b>	Rev 10
Date: Friday, August 16, 2013		Sheet 13 of 23

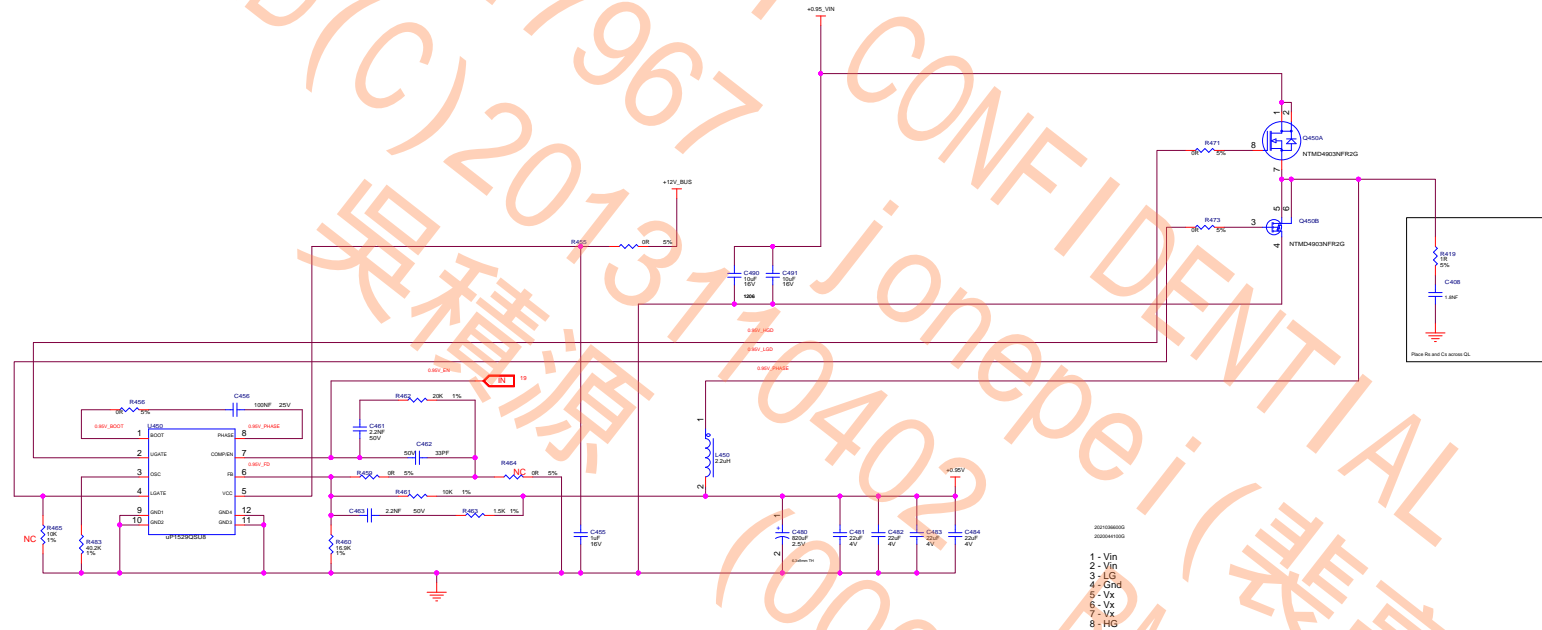








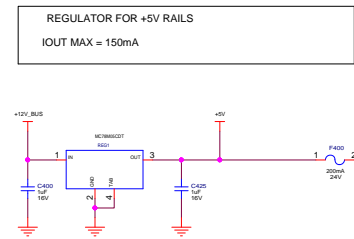
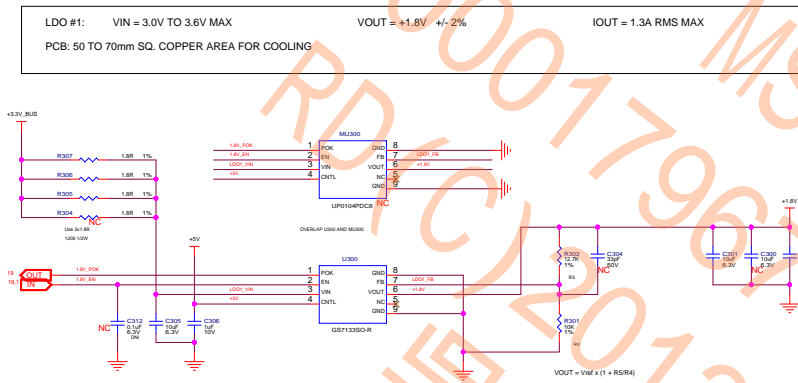
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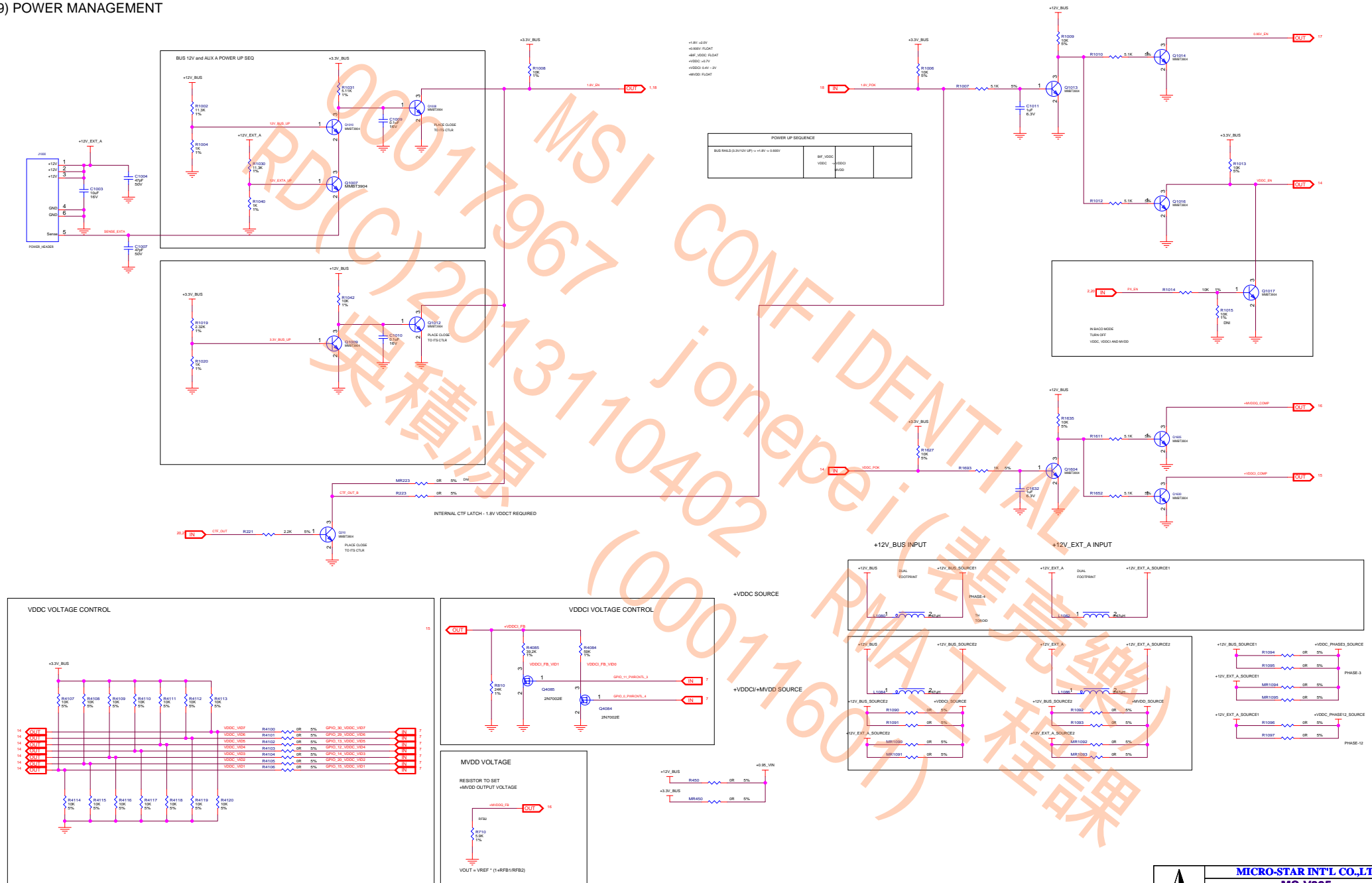
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2 - Vir  
3 - LG  
4 - Gr  
5 - Vx  
6 - Vx  
7 - Vx  
8 - HC

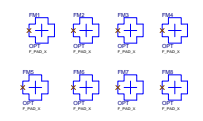


(18) SMALL RAIL REGULATORS



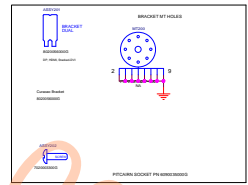
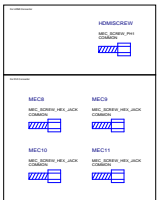
(19) POWER MANAGEMENT



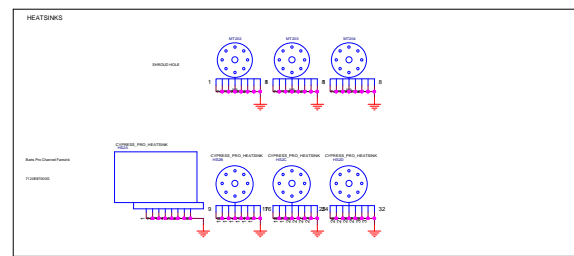
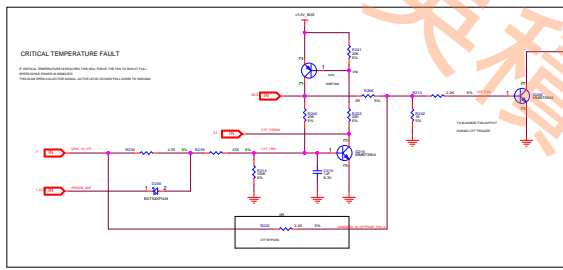
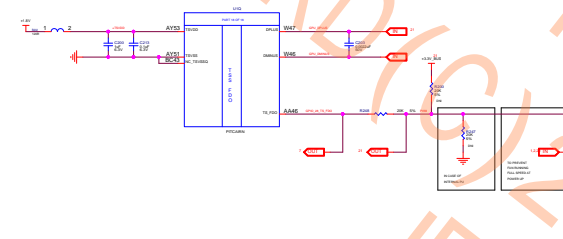


HDMI  
MS-001  
Y01-RHDM03-000  
V000000

SPECIAL MECHANIC  
STRUCTURE STACK

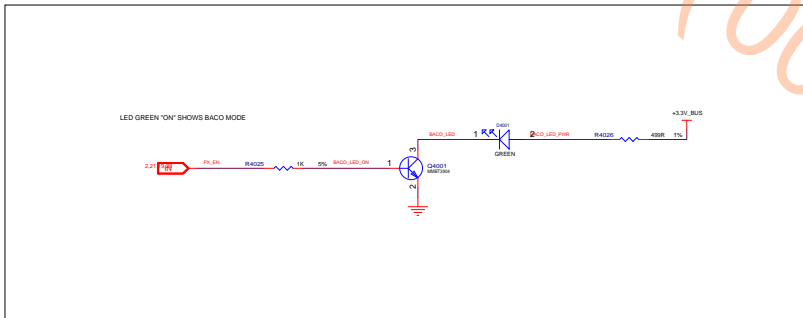
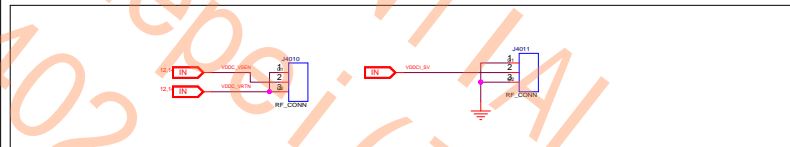
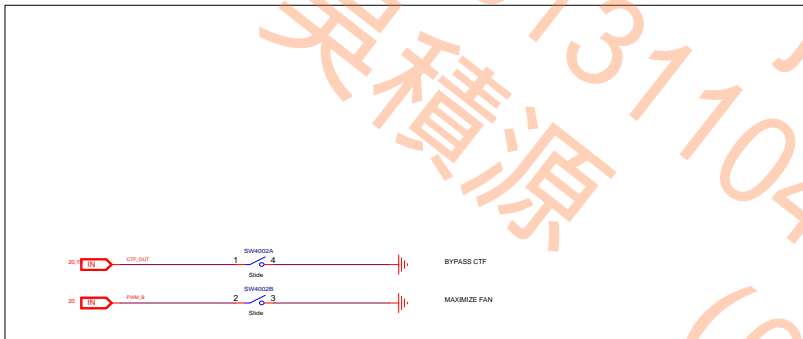
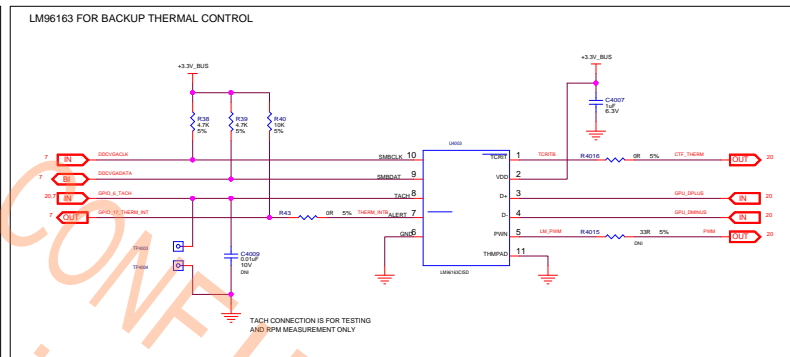
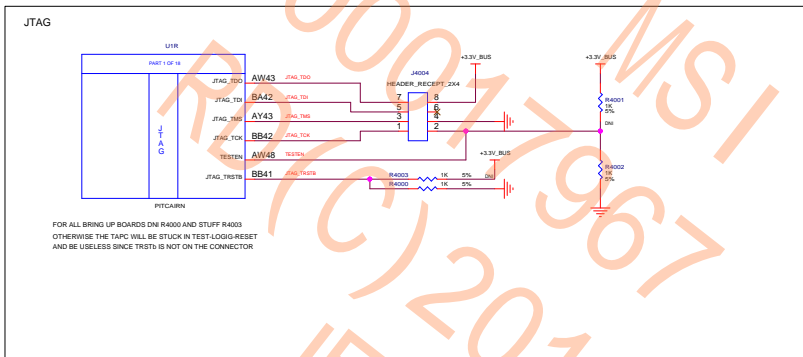


## (20) MECHANICAL AND THERMAL MANAGEMENT



<b>D1</b>	<b>DIFFERENTIAL IMPEDANCE</b> 85 ohms +/- 10% Trace Width: 0.13 mm Spacing: 0.14 mm On Layers: 1,6 Referenced To: 2,5 Note: DP, PCIe	<b>D3</b>	<b>DIFFERENTIAL IMPEDANCE</b> 80 ohms +/- 10% Trace Width: 0.13 mm Spacing: 0.18 mm On Layers: 1,6 Referenced To: 2,5 Note: MEM_CLK	<b>M1</b>	<b>MICROSTRIP IMPEDANCE</b> 50 ohms +/- 10% Trace Width: 0.102 mm On Layers: 1,6 Referenced To: 2,5 Note: DQ0, CLKTEST, RGB	<b>M2</b>	<b>MICROSTRIP IMPEDANCE</b> 45 ohms +/- 5 ohms Trace Width: 0.13 mm On Layers: 1,6 Referenced To: 2,5 Note: MEM
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8		7		6		5		4		3		2		1	
AMD				TITLE: <TITLE>		DOCUMENT NUMBER: 105_0630XX_01		DATE: Wed Jul 24 07:55:42 2013		SHEET NUMBER: 23 OF 23		REV: <REV>			
REVISION HISTORY				ENGINEER: <ENGINEER>		NOTES:		NOTE		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. This AMD Based schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of non-infringement or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.		<ADDR1> <ADDR2> <ADDR3>			
SCH Rev		PCB Rev		Date		REVISION DESCRIPTION									
0		000		20130724											
1		000		20130724		No schematic change. Just add mouse bit hole on PCB									
2		00		20130724		No schematic change.									

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(00011601)