P71, NV17, 4Mx16 SDR, 64MB, RGB, TV-out, video capture, AGP4X

PCI DEVICE ID 0X0=0X171 FOR NV17-128D.

HISTORY:

X00: Adapted from P70, with memory from P60

X24: 1) Added FB clock terminators.

X26: 1) Changed LFH to new pinout.

X30: 1) Removed cap on FBACKE.
2) Changed FB clock terminators to 0402 packages.

X42: 1) Swapped power supply FETs

X45: 1) Added R606 in 12V supply to U600

X46: 1) Changed AGPSTOP pullup to 3.3V
2) Added linear regulator (U602) for frame buffer rail

X50: 1) Changed from integrated to discrete video filters

X51: 1) Removed linear regulator (U602) for frame buffer rail
2) Many BOM edits to reflect new BOM generation scheme

X52: 1) New heatsink part number.
2) Change all FB clock terminators to 200 ohms (R210-R217)

X54: 1) NVPN edits to synchronize schematic with Agile BOM.

```
This schematic is not the source for
the netlist - the A01 netlist was used
for the A04 PCB.  This schematic should
be used to go forward if A05 is
necessary.  It has the correct AGPSTOP
pullup voltage, as well as many BOM
edits for the new BOM generation
scheme.
```

PAGE OVERVIEW

Stuff Option	Meaning
COMMON	Common to all assemblies
NO STUFF	Not normally present in any assembly
VIDCAP	Video Capture
RGB_PROT	RGB Protection diodes on primary DAC outputs
LFH	Second DAC channel goes to LFH connector
TV	Second DAC channel goes to S Video connector as TV out
1117	Fixed 1117 linear regulator for A3.3V
1117_ADJ	Adjustable 1117 linear regulator for A3.3V
NO_1117	Take A3.3V from system 3.3V
64B5N	64 Bit, 5 nS frame buffer
64B6N	64 Bit, 6 nS frame buffer
128B5N	128 Bit, 5 nS frame buffer
128B6N	128 Bit, 6 nS frame buffer
DESK	Desktop system
WKST	Workstation system
WKSTL	Workstation Lite system
MEM33	Frame buffer voltage is AGP 3.3V
MEM30	Frame buffer voltage is independently regulated

140-10071-0000-xxx
602-10071-0000-xxx

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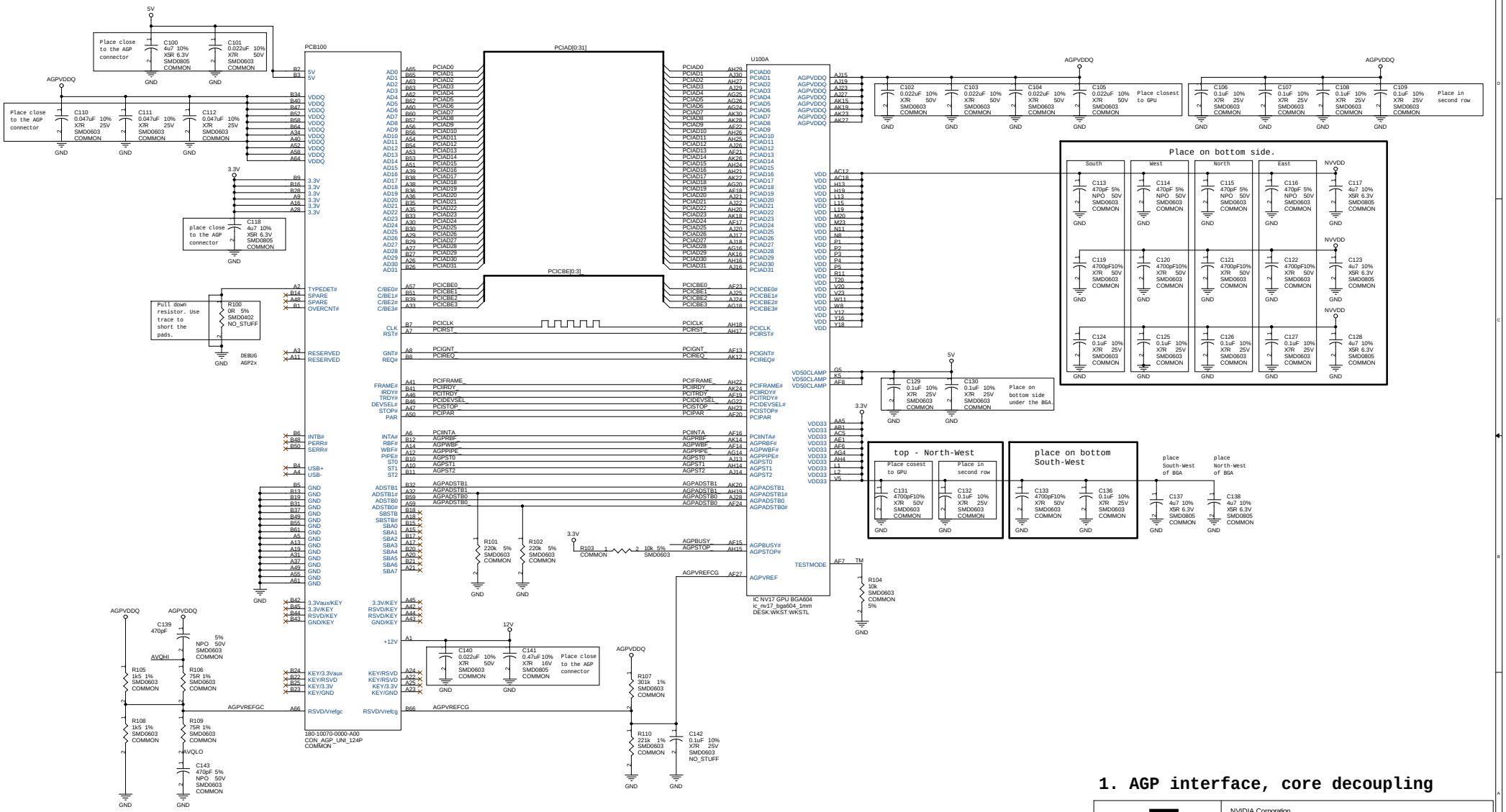
Size	CAGE Code	DWG NO	Rev
Custom			

Thursday, January 10, 2002 | Scale | Sheet 1 of 11



1. AGP interface, core decoupling

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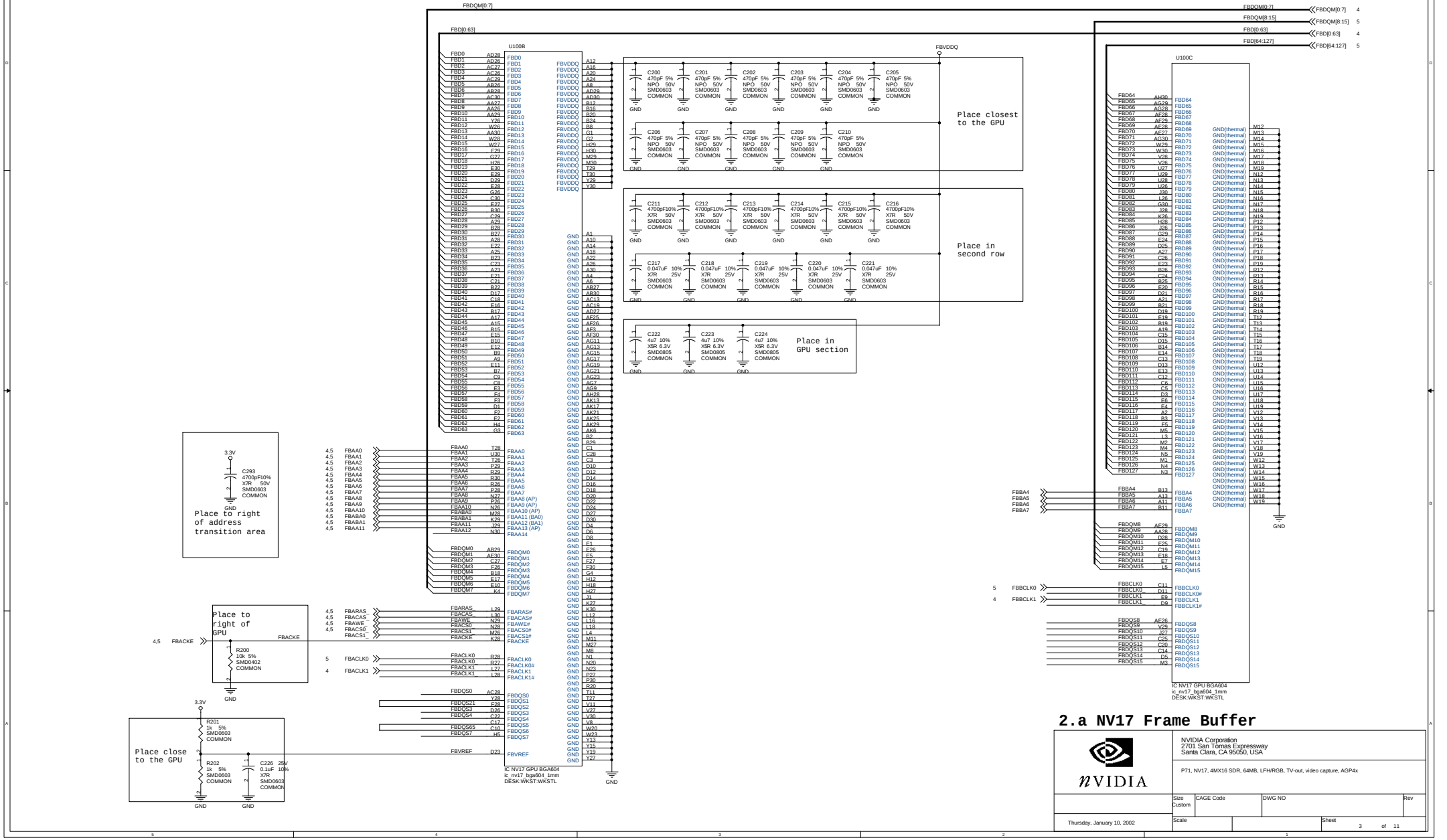
Custom			

Thursday, January 10, 2002 — Scale — Sheet 2 of 11


FBDQM[0:7]
FBD[0:63]
U100B
FBVDDQ
Place closest to the GPU
Place in second row
Place in GPU section
C200 470pF 5% NPO 50V SMD0603 COMMON
C201 470pF 5% NPO 50V SMD0603 COMMON
C202 470pF 5% NPO 50V SMD0603 COMMON
C203 470pF 5% NPO 50V SMD0603 COMMON
C204 470pF 5% NPO 50V SMD0603 COMMON
C205 470pF 5% NPO 50V SMD0603 COMMON
C206 470pF 5% NPO 50V SMD0603 COMMON
C207 470pF 5% NPO 50V SMD0603 COMMON
C208 470pF 5% NPO 50V SMD0603 COMMON
C209 470pF 5% NPO 50V SMD0603 COMMON
C210 470pF 5% NPO 50V SMD0603 COMMON
C211 4700pF10% X7R 50V SMD0603 COMMON
C212 4700pF10% X7R 50V SMD0603 COMMON
C213 4700pF10% X7R 50V SMD0603 COMMON
C214 4700pF10% X7R 50V SMD0603 COMMON
C215 4700pF10% X7R 50V SMD0603 COMMON
C216 4700pF10% X7R 50V SMD0603 COMMON
C217 0.047uF 10% X7R 25V SMD0603 COMMON
C218 0.047uF 10% X7R 25V SMD0603 COMMON
C219 0.047uF 10% X7R 25V SMD0603 COMMON
C220 0.047uF 10% X7R 25V SMD0603 COMMON
C221 0.047uF 10% X7R 25V SMD0603 COMMON
C222 4u7 10% X5R 6.3V SMD0805 COMMON
C223 4u7 10% X5R 6.3V SMD0805 COMMON
C224 4u7 10% X5R 6.3V SMD0805 COMMON
GND
3.3V
C293 4700pF10% X7R 50V SMD0603 COMMON
Place to right of address transition area
FBAA0
FBAA1
FBAA2
FBAA3
FBAA4
FBAA5
FBAA6
FBAA7
FBAA8
FBAA9
FBAA10
FBABA0
FBABA1
FBAA11
FBAA12
FBDQM0
FBDQM1
FBDQM2
FBDQM3
FBDQM4
FBDQM5
FBDQM6
FBDQM7
Place to right of GPU
FBACKE
R200 10k 5% SMD0402 COMMON
FBARAS_
FBACAS_
FBAWE_
FBACS0_
FBACS1_
FBACLK0
FBACLK1
FBDQS0
FBDQS21
FBDQS3
FBDQS4
FBDQS65
FBDQS7
FBVREF
Place close to the GPU
R201 1k 5% SMD0603 COMMON
R202 1k 5% SMD0603 COMMON
C226 25V 0.1uF 10% X7R SMD0603 COMMON
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WKST:WKSTL
U100C
FBD64
FBD65
FBD66
FBD67
FBD68
FBD69
FBD70
FBD71
FBD72
FBD73
FBD74
FBD75
FBD76
FBD77
FBD78
FBD79
FBD80
FBD81
FBD82
FBD83
FBD84
FBD85
FBD86
FBD87
FBD88
FBD89
FBD90
FBD91
FBD92
FBD93
FBD94
FBD95
FBD96
FBD97
FBD98
FBD99
FBD100
FBD101
FBD102
FBD103
FBD104
FBD105
FBD106
FBD107
FBD108
FBD109
FBD110
FBD111
FBD112
FBD113
FBD114
FBD115
FBD116
FBD117
FBD118
FBD119
FBD120
FBD121
FBD122
FBD123
FBD124
FBD125
FBD126
FBD127
GND(thermal)
FBBA4
FBBA5
FBBA6
FBBA7
FBDQM8
FBDQM9
FBDQM10
FBDQM11
FBDQM12
FBDQM13
FBDQM14
FBDQM15
FBBCLK0
FBBCLK0#
FBBCLK1
FBBCLK1#
FBDQS8
FBDQS9
FBDQS10
FBDQS11
FBDQS12
FBDQS13
FBDQS14
FBDQS15
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WKST:WKSTL
FBDQM[0:7]
FBDQM[8:15]
FBD[0:63]
FBD[64:127]
2.a NV17 Frame Buffer
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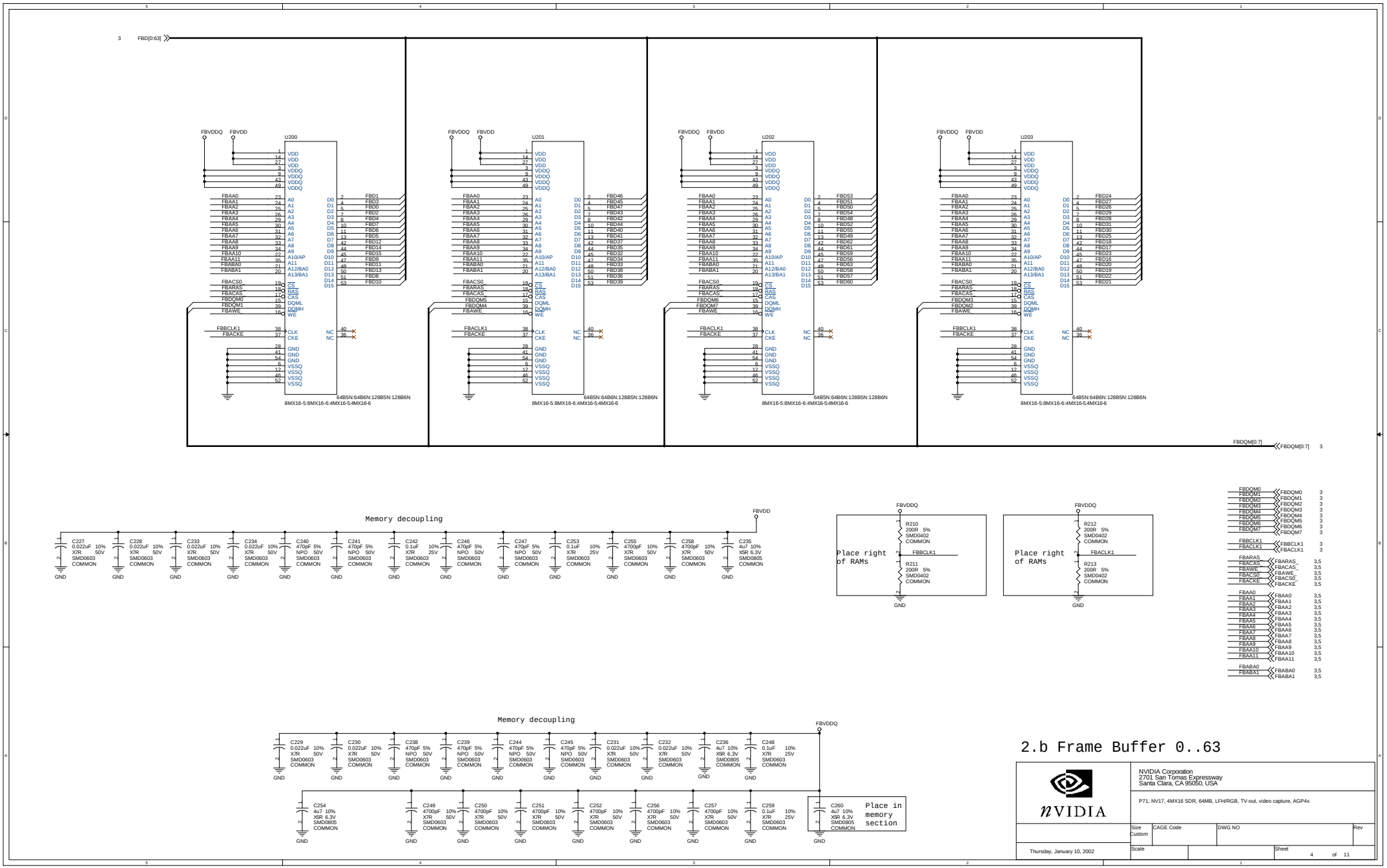
Size Custom
CAGE Code
DWG NO
Rev
Thursday, January 10, 2002
Scale
Sheet 3 of 11


FBD[0:63]
U200
U201
U202
U203
FBVDDQ
FBVDD
64B5N:64B6N:128B5N:128B6N
8MX16-5:8MX16-6:4MX16-5:4MX16-6
FBDQM[0:7]
Memory decoupling
Place right of RAMs
Place in memory section
2.b Frame Buffer 0..63
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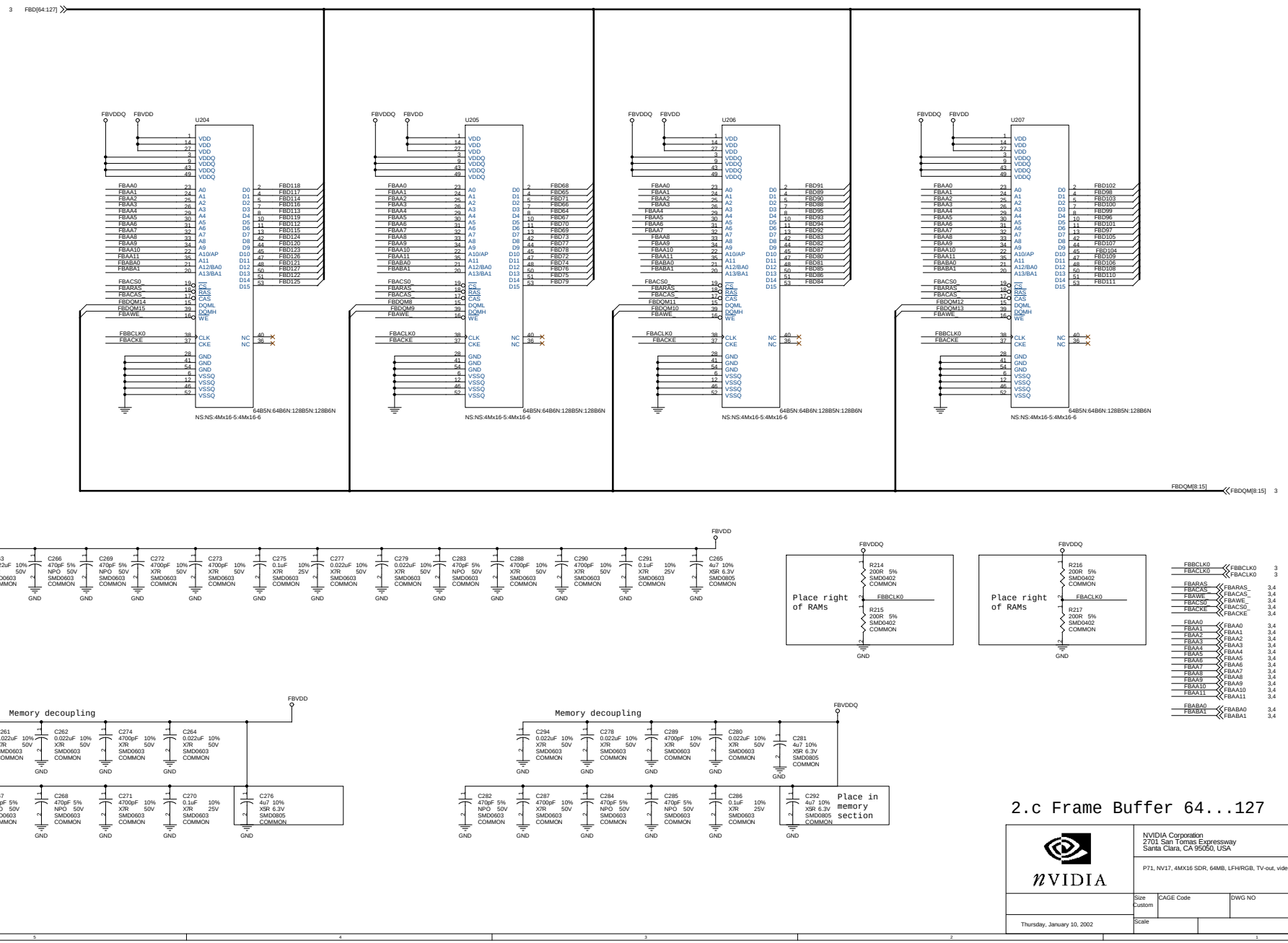
Thursday, January 10, 2002
Sheet 4 of 11



2.c Frame Buffer 64...127

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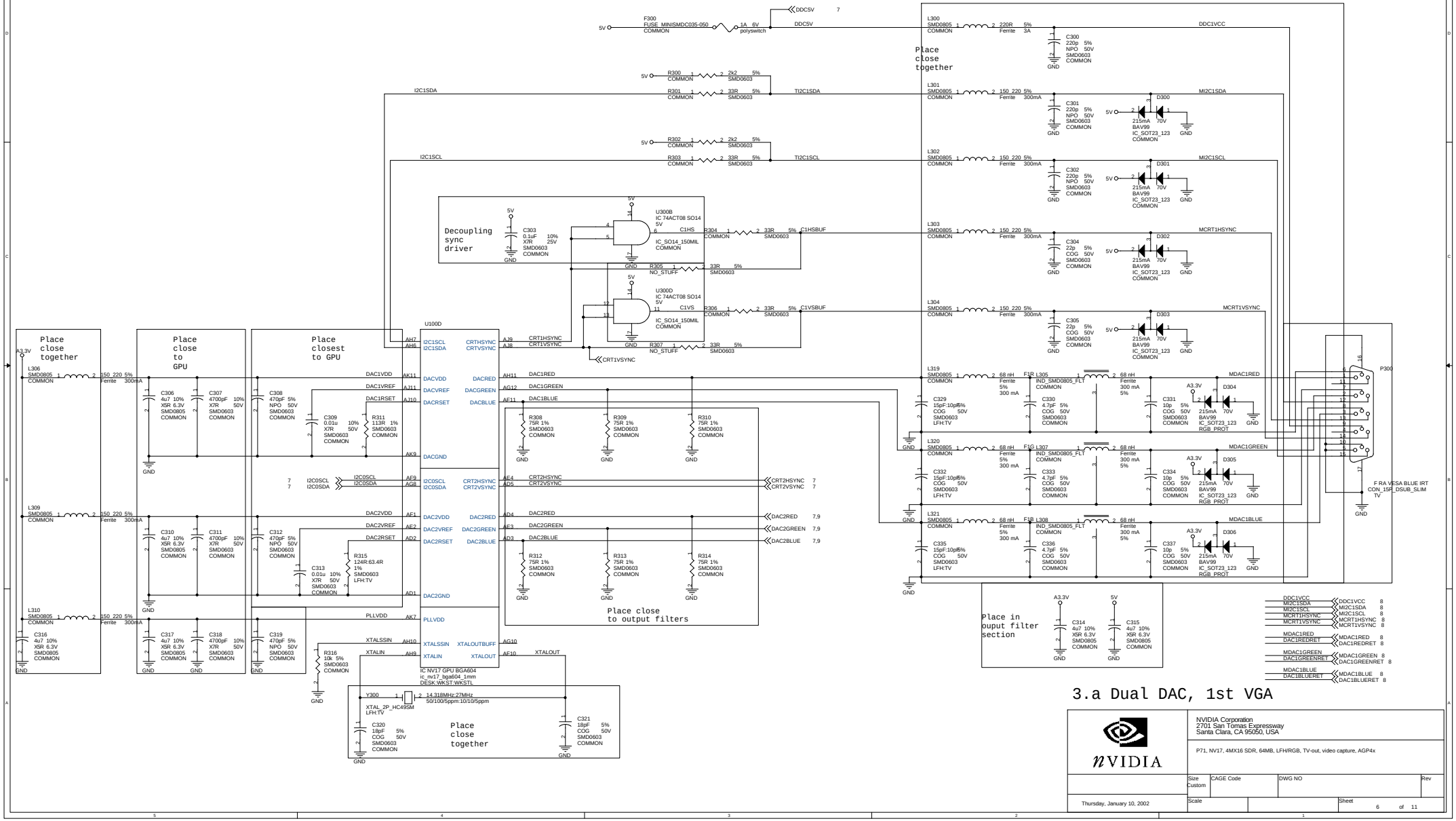
Thursday, January 10, 2002 — Scale — Sheet 5 of 11


Decoupling sync driver
Place close together
Place close to GPU
Place closest to GPU
Place close to output filters
Place close together
Place in ouput filter section
U100D
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WKST:WKSTL
U300B IC 74ACT08 SO14
U300D IC 74ACT08 SO14
IC_SO14_150MIL
F300 FUSE_MINISMDC035-050
1A 6V polyswitch
P300
F RA VESA BLUE IRT CON_15P_DSUB_SLIM
TV
3.a Dual DAC, 1st VGA
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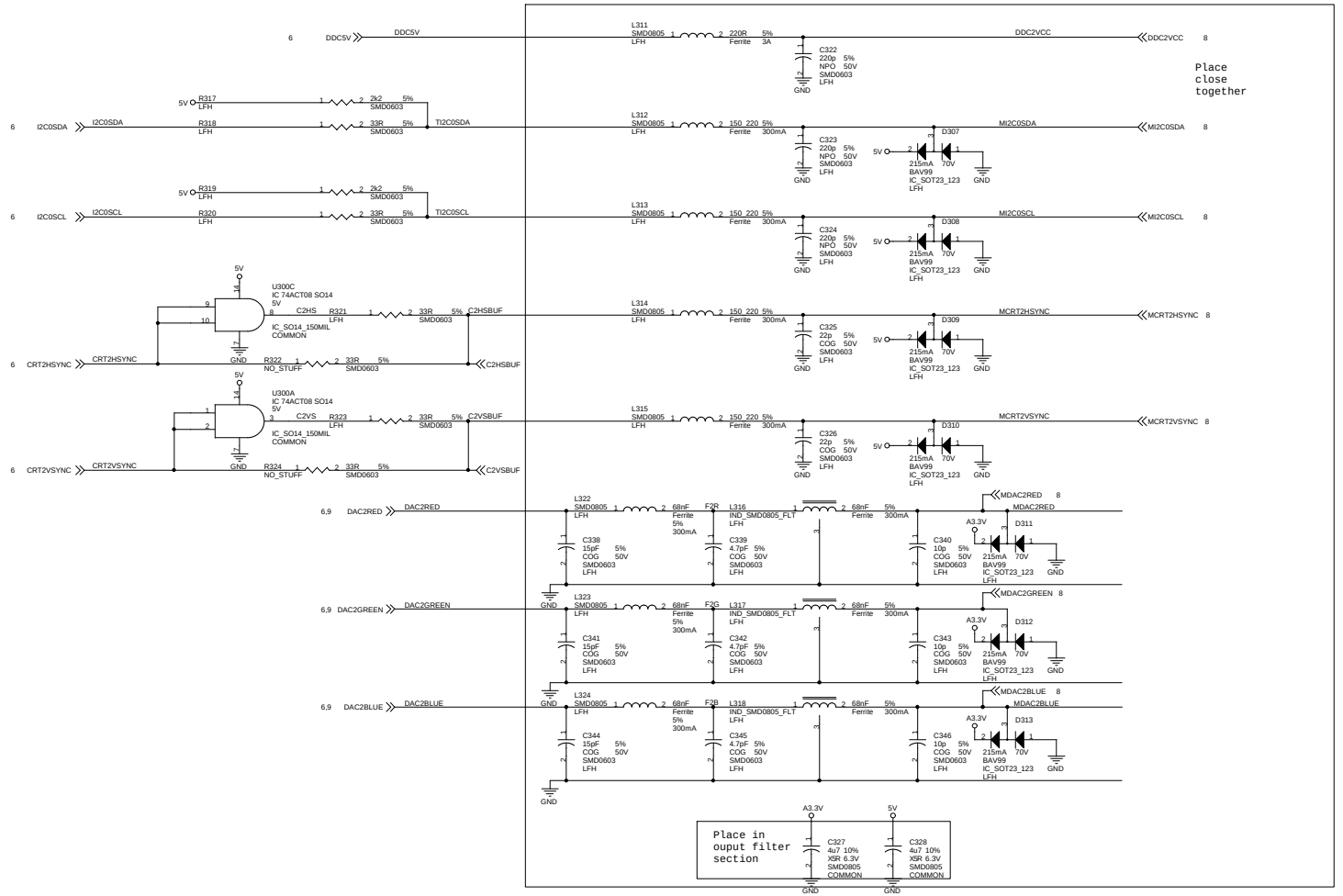
Thursday, January 10, 2002
Sheet 6 of 11



3.b Dual DAC, 2nd VGA

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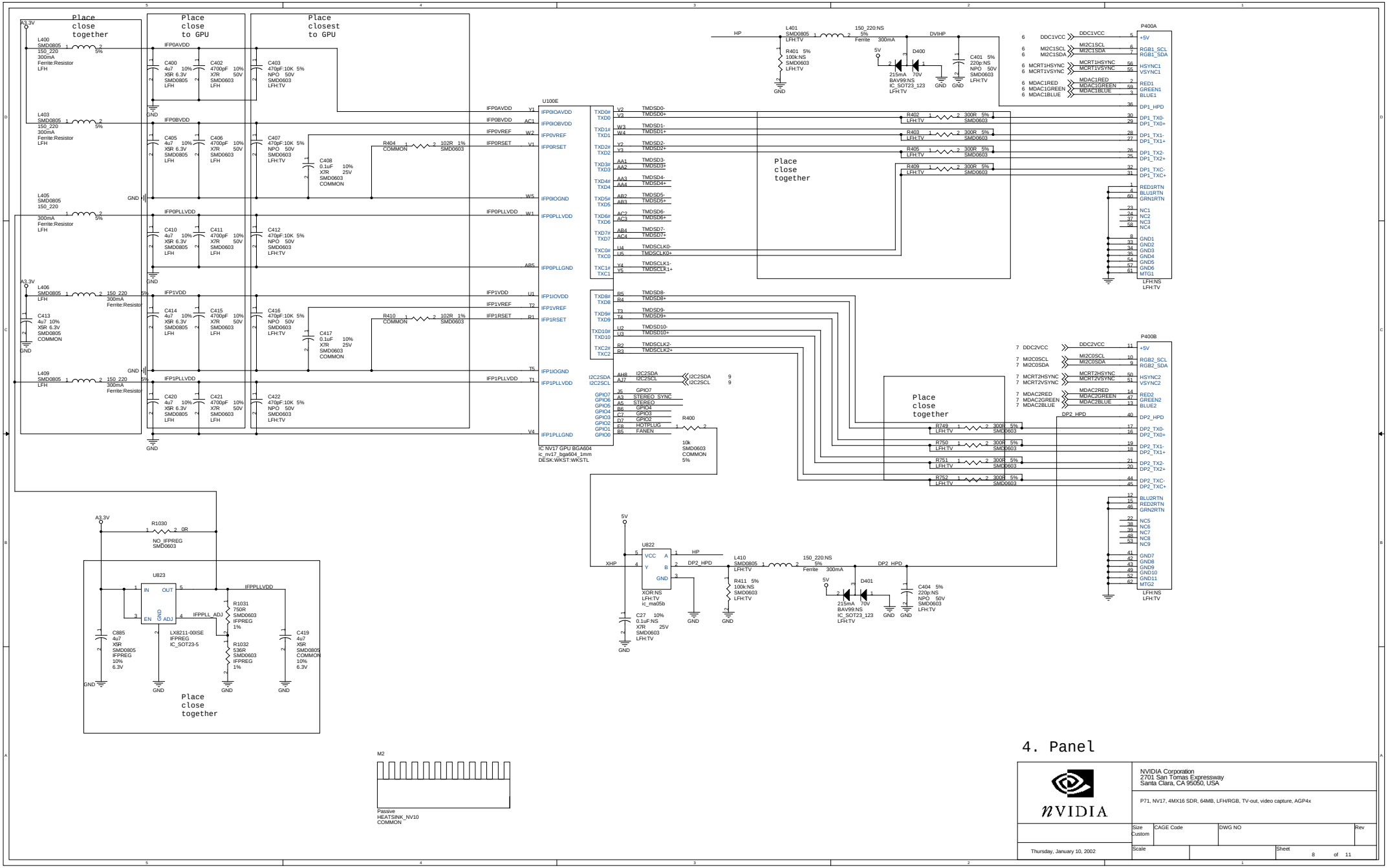
Custom			

Thursday, January 10, 2002

Scale

Sheet 7 of 11



4. Panel

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Thursday, January 10, 2002

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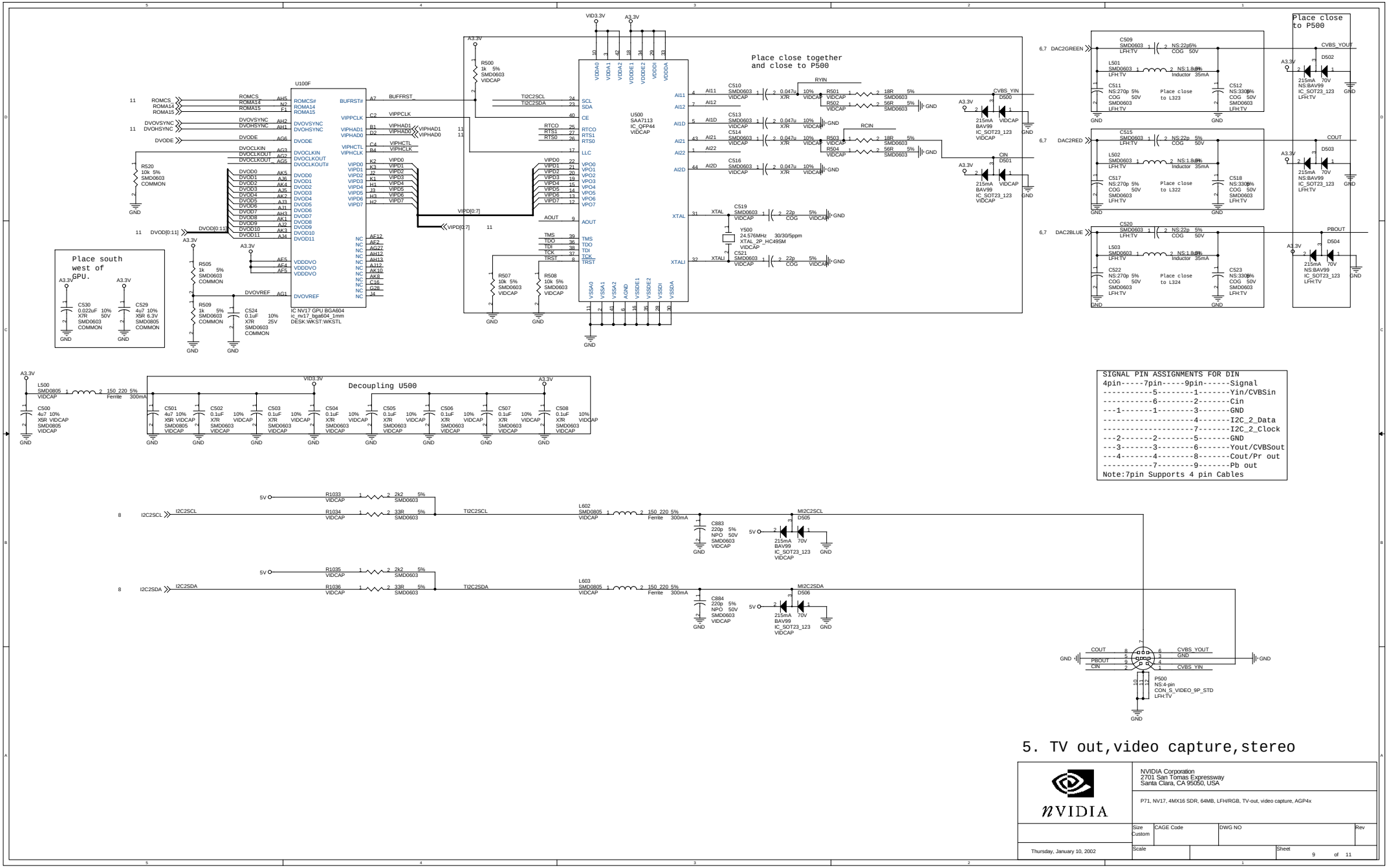
Sheet 8 of 11


U100F
ROMCS
ROMA13
ROMA15
DVOVSYNC
DVOHSYNC
DVODE
DVOCLKIN
DVOCLKOUT
DVOCLKOUT#
DVOD0
DVOD1
DVOD2
DVOD3
DVOD4
DVOD5
DVOD6
DVOD7
DVOD8
DVOD9
DVOD10
DVOD11
DVOVREF
BUFRST#
VIPPCLK
VIPHAD1
VIPHAD0
VIPHCTL
VIPHCLK
VIPD0
VIPD1
VIPD2
VIPD3
VIPD4
VIPD5
VIPD6
VIPD7
VDDVO
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WK:ST:WKSTL
U500
SAA7113
IC_QFP44
VIDCAP
Place close together
and close to P500
Place south
west of
GPU.
Decoupling U500
SIGNAL PIN ASSIGNMENTS FOR DIN
4pin-----7pin-----9pin-----Signal
----------5--------1-------Yin/CVBSin
----------6--------2-------Cin
---1-------1--------3-------GND
--------------------4-------I2C_2_Data
--------------------7-------I2C_2_Clock
---2-------2--------5-------GND
---3-------3--------6-------Yout/CVBSout
---4-------4--------8-------Cout/Pr out
----------7--------9-------Pb out
Note:7pin Supports 4 pin Cables
P500
NS:4-pin
CON_S_VIDEO_9P_STD
LFH:TV
5. TV out,video capture,stereo
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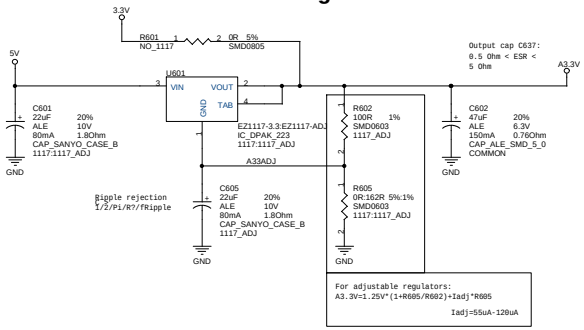
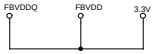
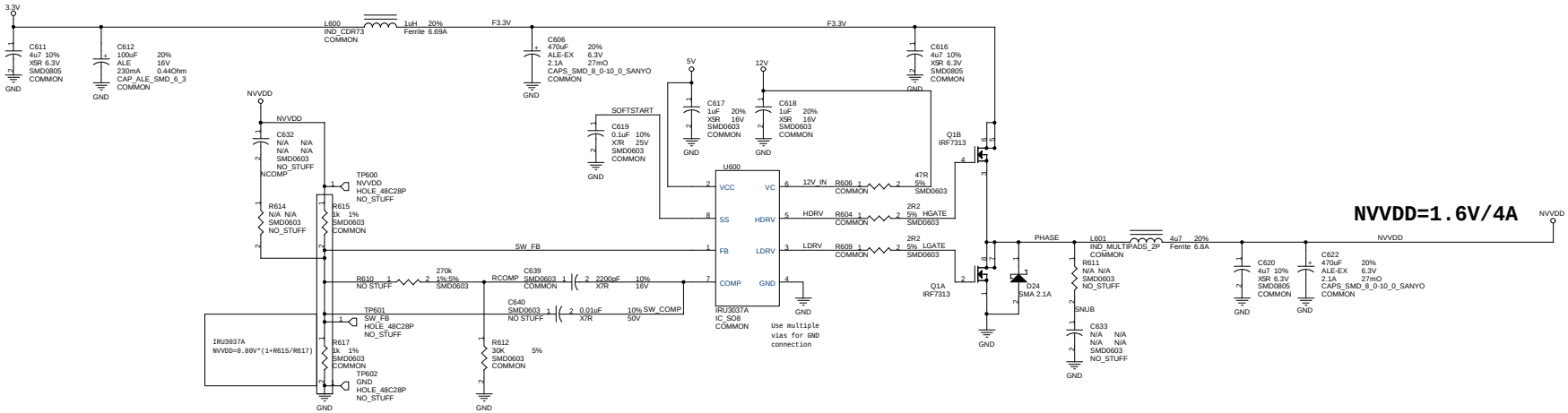
Thursday, January 10, 2002
Sheet 9 of 11

Analog 3.3V







6. Power supply

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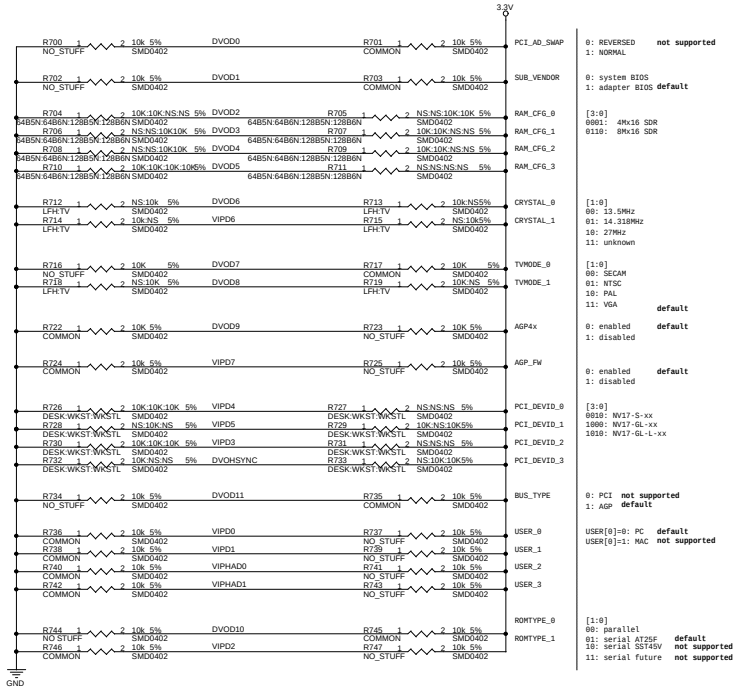
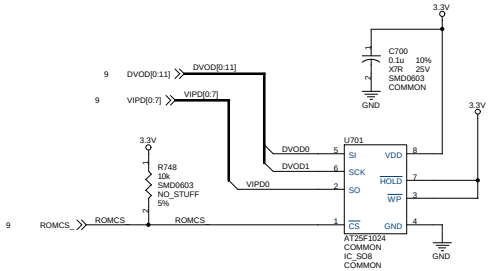
	Size Custom	CAGE Code	DWG NO	Rev
Thursday, January 10, 2002	Scale		Sheet 10 of 11	





7. BIOS, Strapping

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Thursday, January 10, 2002

Scale

Sheet 11 of 11