PG161-A00

TU106 6GB GDDR6, 192b, X16
DVI-D/DP + DP + HDMI

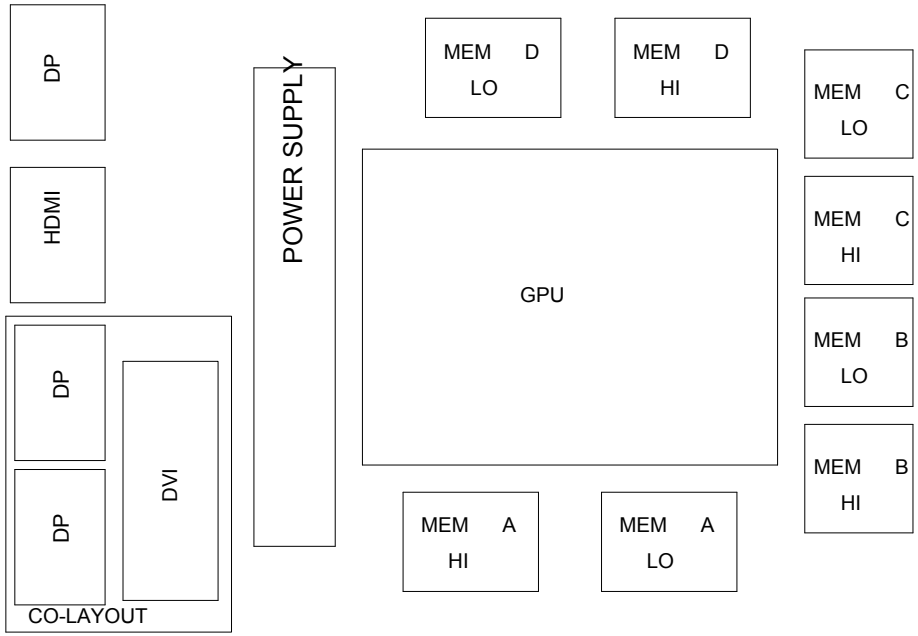
TABLE OF CONTENTS

V375-20
1. 移除 CO-LAY
2. Core Power: uP9512SQKI (QFN 4x4) + (NCP302045 x 4)
   Memory Power: I32-S725602-N03 + (UBIQ 3103+3107*2)
3. P.34 add R779
4. P.30 & 44 移除PS_FBVDD_BUFF換頁符號
   換 FBVDD controller ，換成1PHASE 上1下2
5. P.52 add HDMI & DVI 螺絲
6. IO 換常用料，footprint 不變

V379-10
線路：
1. 基於V375-1.2刪除GDDR6貼PG165 SKU0 GDDR5線路，
   拉GPIO10做VREF。
2. DRAM Power MOSFET改成Dual-N MOSFET。
物料：
1. 基於V375-58S DRAM PWM換成NIKO / GS7222
   並調成GDDR5電壓準位，相數2改1。
2. Core Power相數4改3。
3. OVR-M換UPI / US5650。

MICRO-STAR INT'L CO.,LTD
MS-V379
Size: Custom | Document Description: Page1: Table of Contents | Rev: 1.0
Date: Monday, January 14, 2019 | Sheet 1 of 53

Page2: Block Diagram



Power Supply:

- Power Supply NVVDD-PH6
- Power Supply NVVDD-PH5
- Power Supply NVVDD-PH4
- Power Supply NVVDD-PH3
- Power Supply NVVDD-PH2
- Power Supply NVVDD-PH1
- Power Supply FBVDDQ-PH2
- Power Supply FBVDDQ-PH1
- Power Supply 5V
- PEX_VDD
- 1V8
- Fan
- DP_PWR

EXT_12V 2x4 PWR

PEX_12V Finger

3V3 Finger

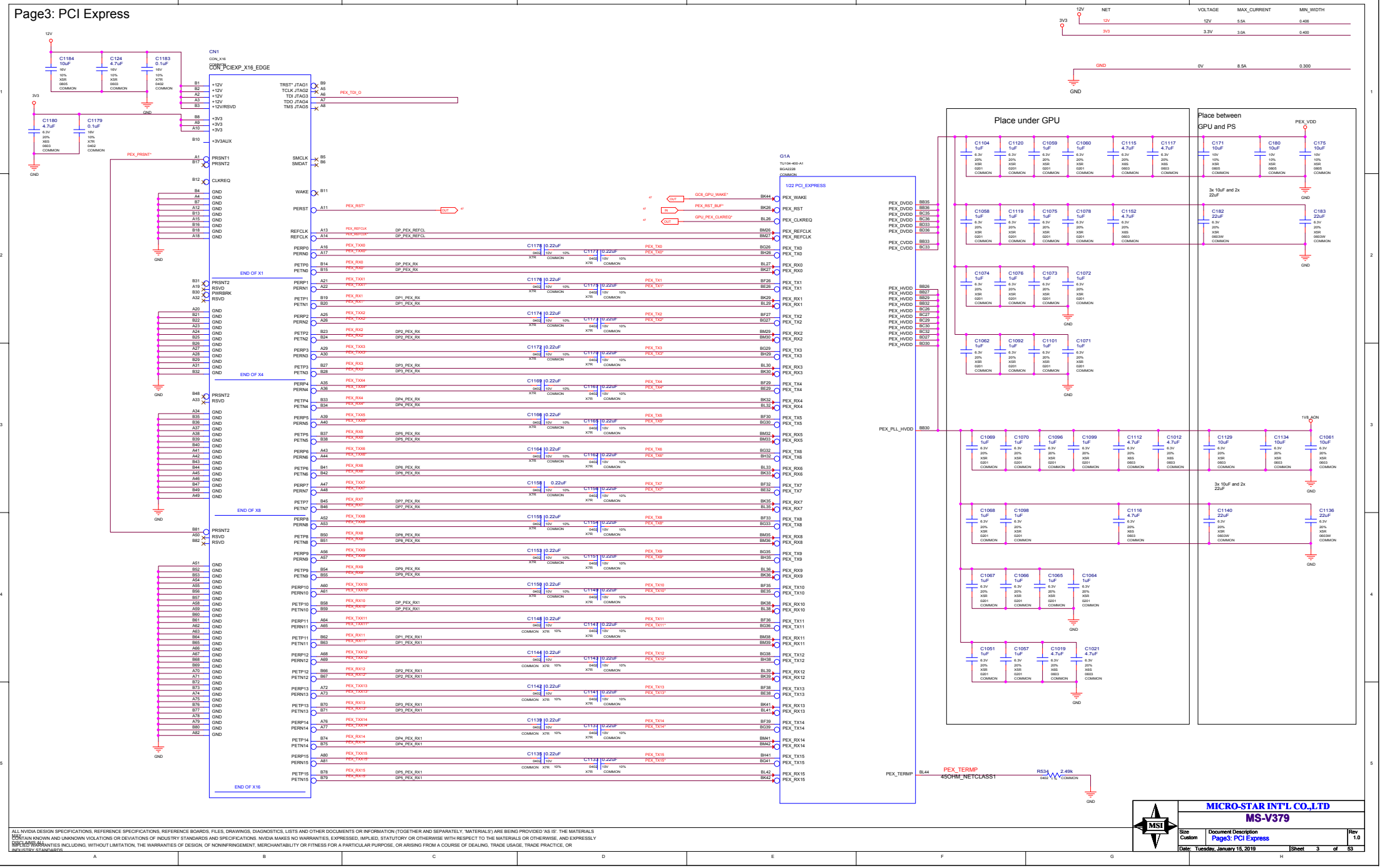
MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page2: Block Diagram	1.0

Date: Monday, January 14, 2019 Sheet 2 of 53

Page3: PCI Express



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.406
3V3	3.3V	3.0A	0.400
GND	0V	8.5A	0.300

MICRO-STAR INT'L CO.,LTD

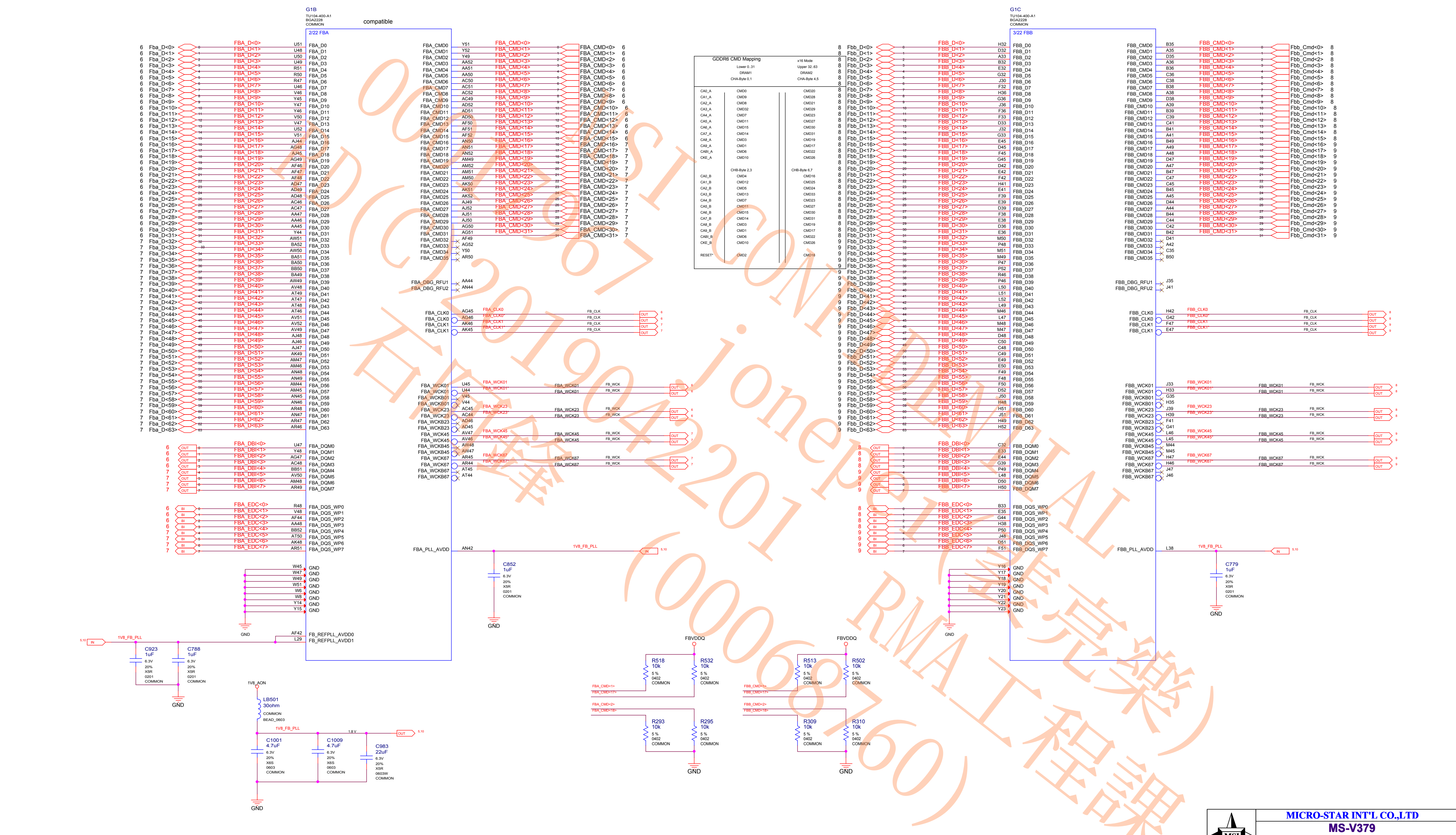
MS-V379

Size	Document Description	Rev
Custom	Page3: PCI Express	1.0
Date: Tuesday, January 15, 2019	Sheet 3 of 53	

NO PEX GEN4 SUPPORT

DELETE RC TERMINATIONS

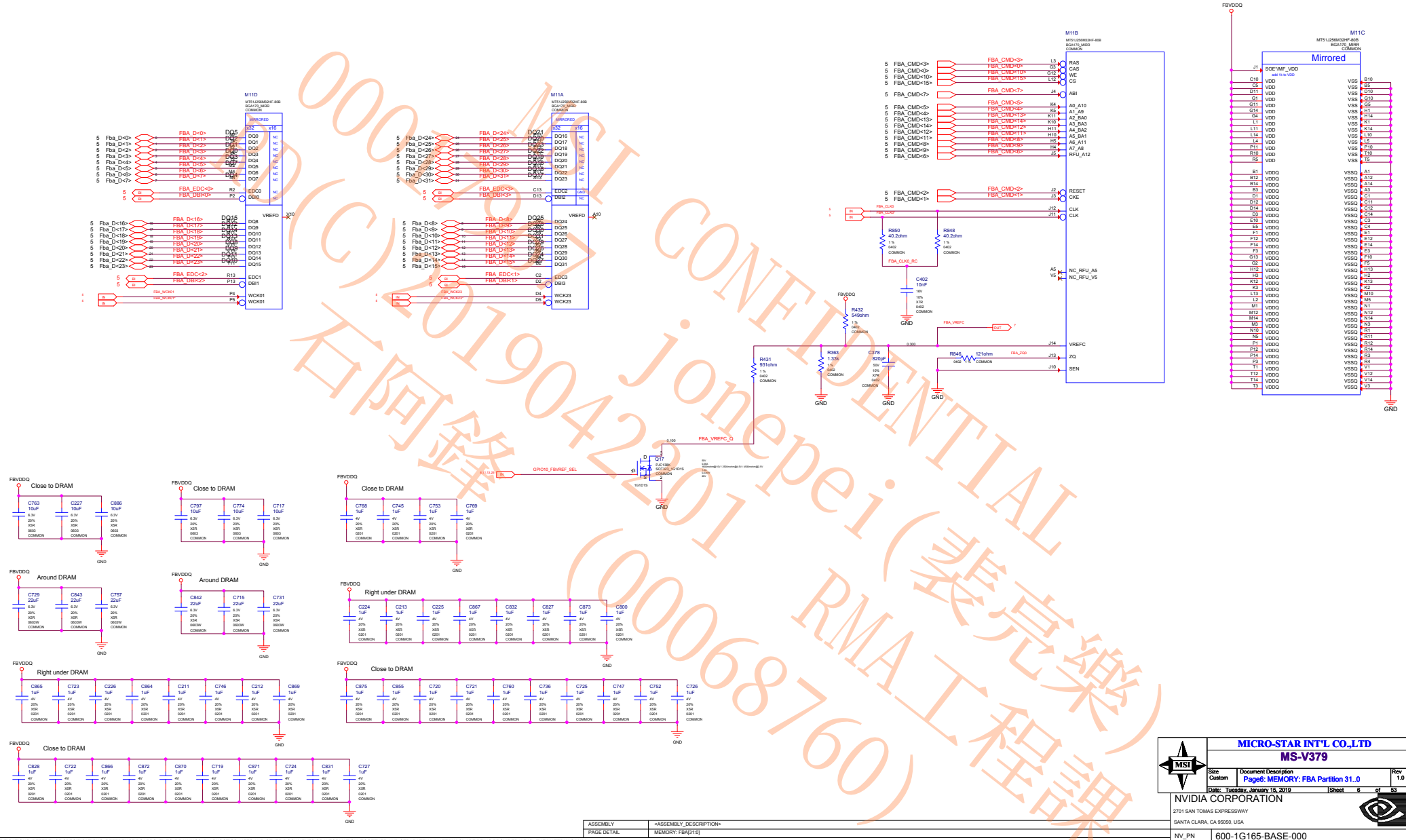
Page5: MEMORY: GPU Partition A/B



MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page5: MEMORY: GPU Partition A/B	1.0



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	'MEMORY: FBA[31:0]

MICRO-STAR INT'L CO.,LTD

MS-V379

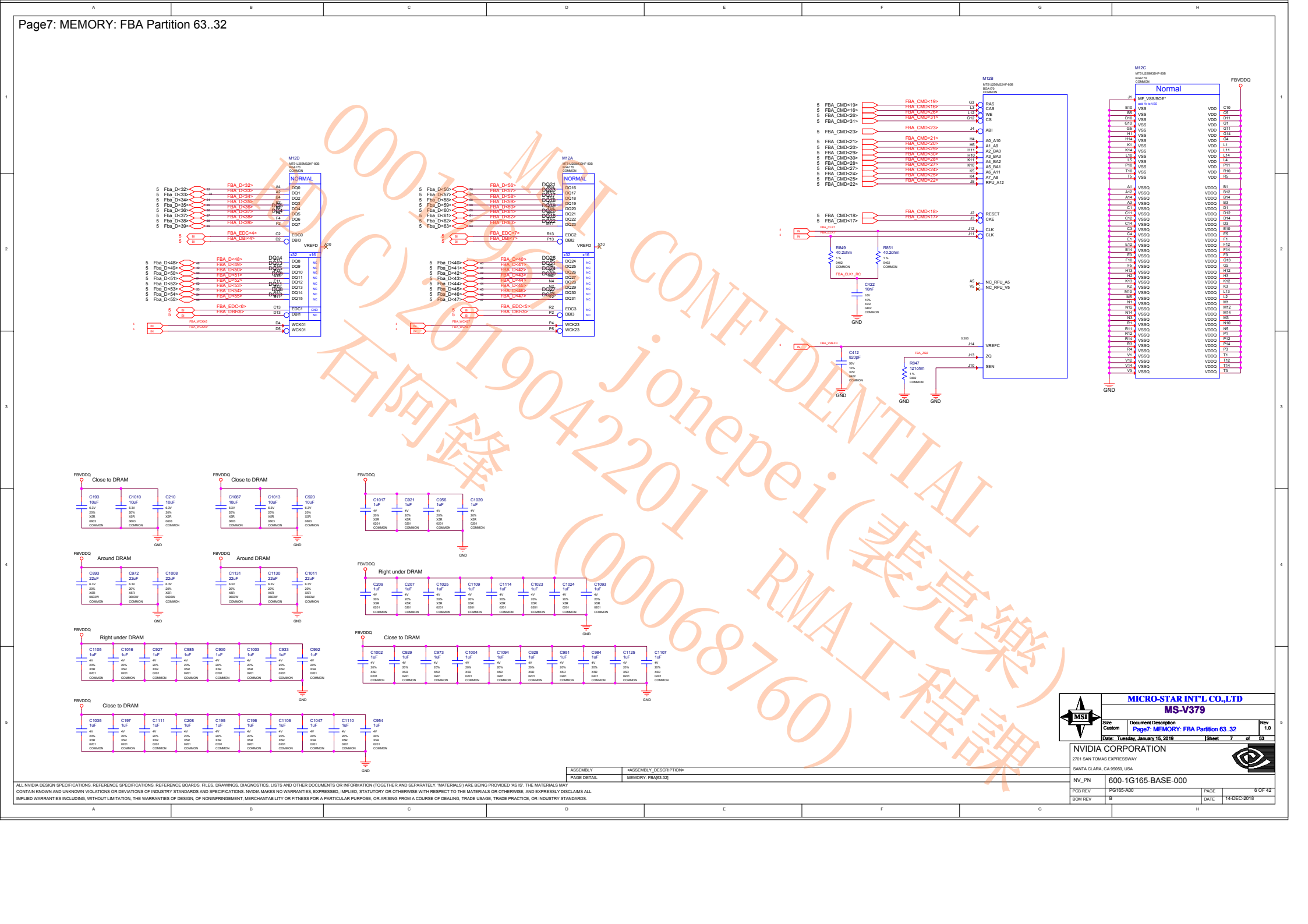
Size	Document Description	Rev
Custom	Page6: MEMORY: FBA Partition 31..0	1.0

Date: Tuesday, January 15, 2019 | Sheet 6 of 53

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G165-BASE-000		
PCB REV	PG165-A00	PAGE	5 OF 42
BOM REV	B	DATE	14-DEC-2018

Page7: MEMORY: FBA Partition 63..32



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBA[63:32]

MICRO-STAR INT'L CO.,LTD

MS-V379

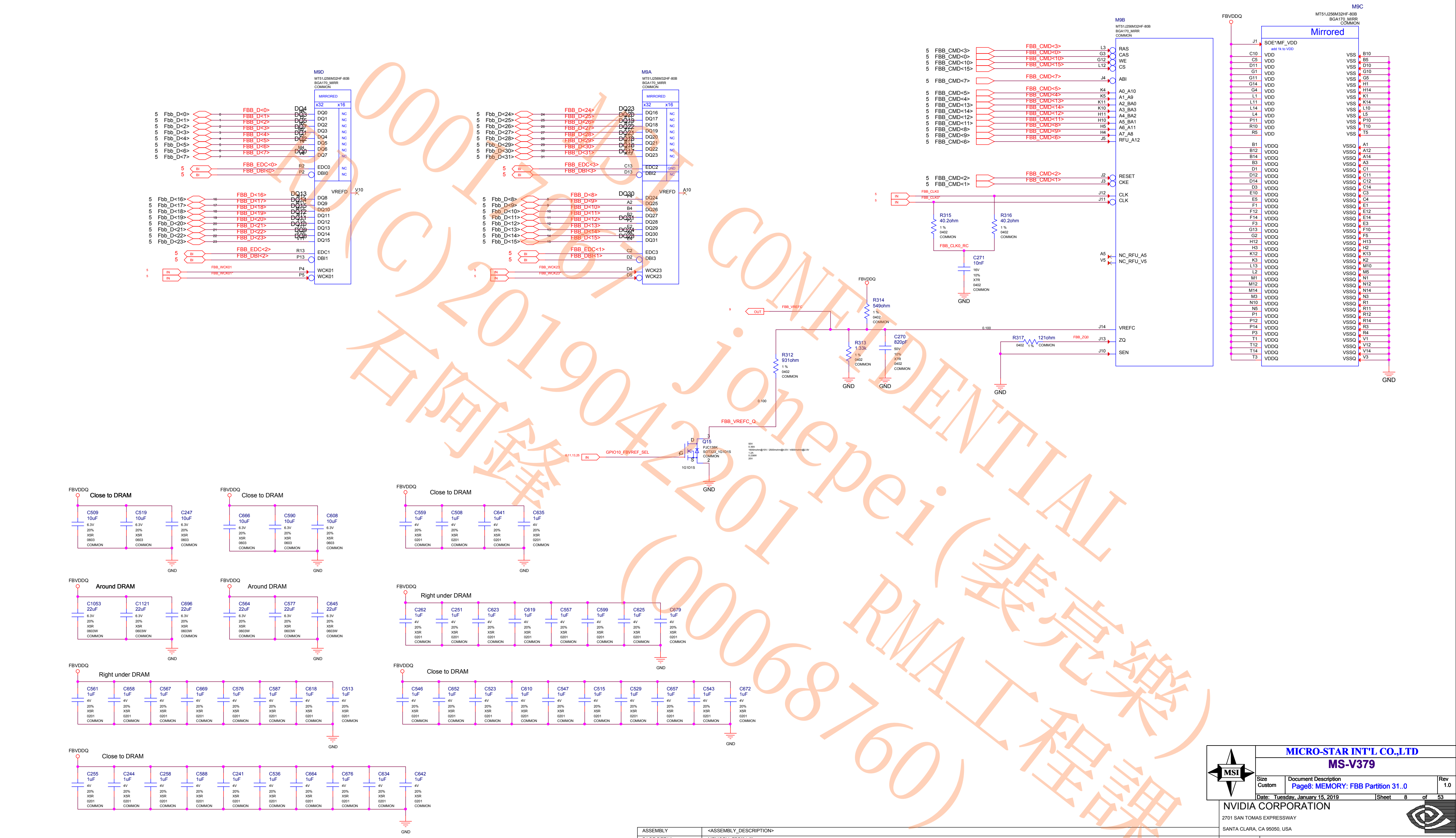
Size	Document Description	Rev
Custom	Page7: MEMORY: FBA Partition 63..32	1.0

Date: Tuesday, January 15, 2019 | Sheet 7 of 63

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G165-BASE-000		
PCB REV	PG165-A00	PAGE	6 OF 42
BOM REV	B	DATE	14-DEC-2018

Page8: MEMORY: FBB Partition 31..0



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB[31:0]

MICRO-STAR INT'L CO.,LTD

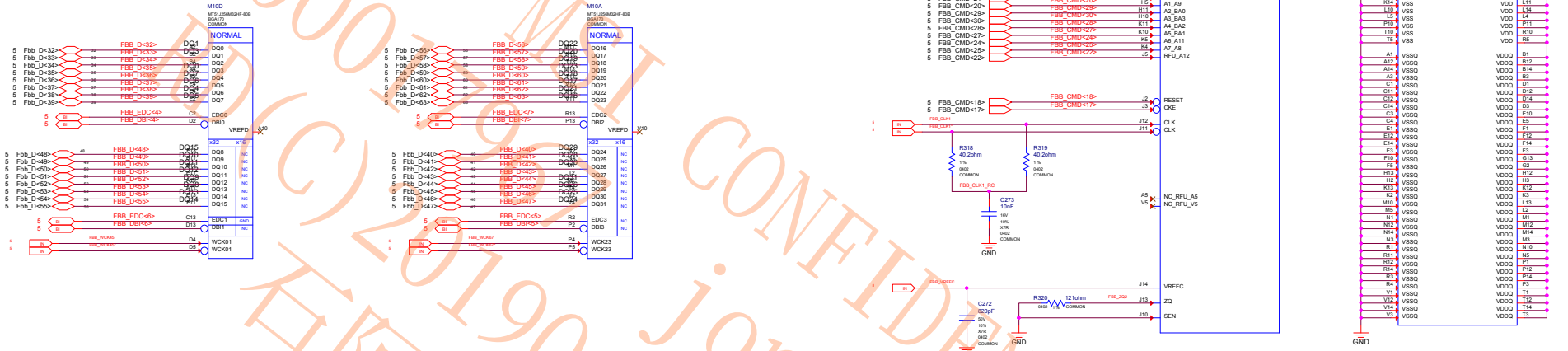
MS-V379

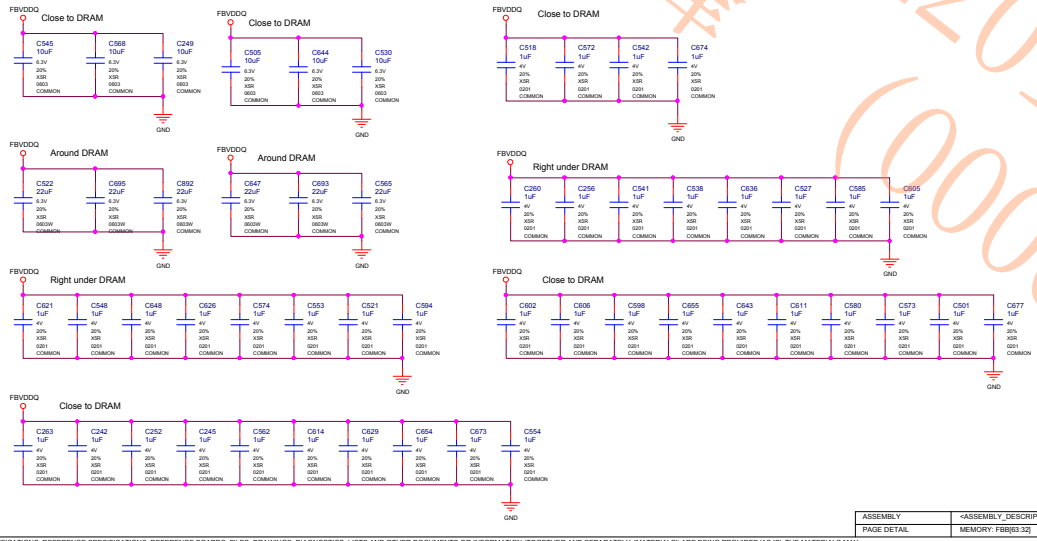
Size	Document Description	Rev
Custom	Page8: MEMORY: FBB Partition 31..0	1.0
Date: Tuesday, January 15, 2019	Sheet 8 of 53	

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G165-BASE-000		
PCB REV	PG165-A00	PAGE	7 OF 42
BOM REV	B	DATE	14-DEC-2018

Page9: MEMORY: FBB Partition 63..32





ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB[63:32]

MICRO-STAR INT'L CO.,LTD

MS-V379

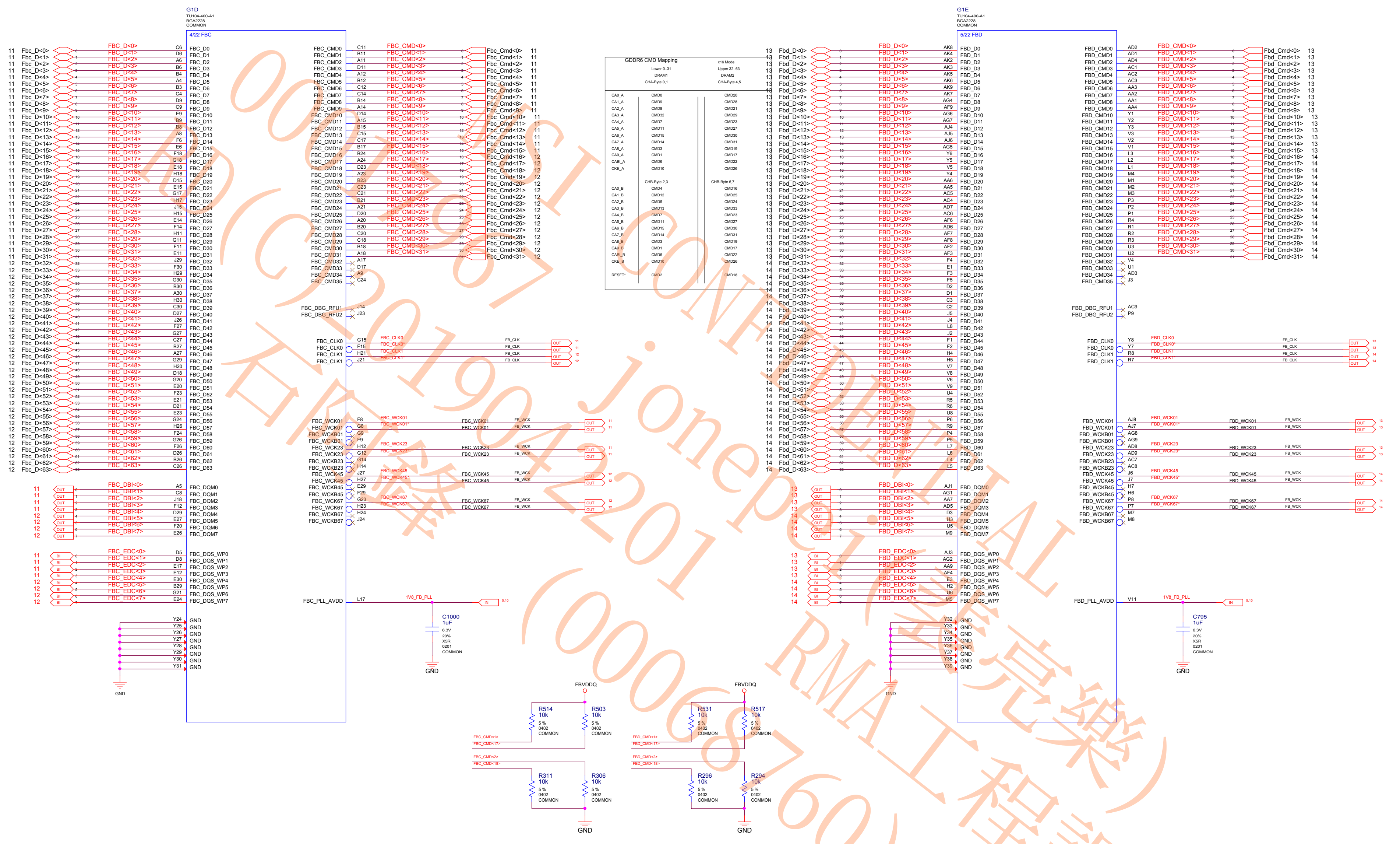
Size	Document Description	Rev
Custom	Page9: MEMORY: FBB Partition 63..32	1.0

Date: Tuesday, January 15, 2019 Sheet 9 of 53

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G165-BASE-000		
PCB REV	PG165-A00	PAGE	8 OF 42
BOM REV	B	DATE	14-DEC-2018

Page10: MEMORY: GPU Partition C/D



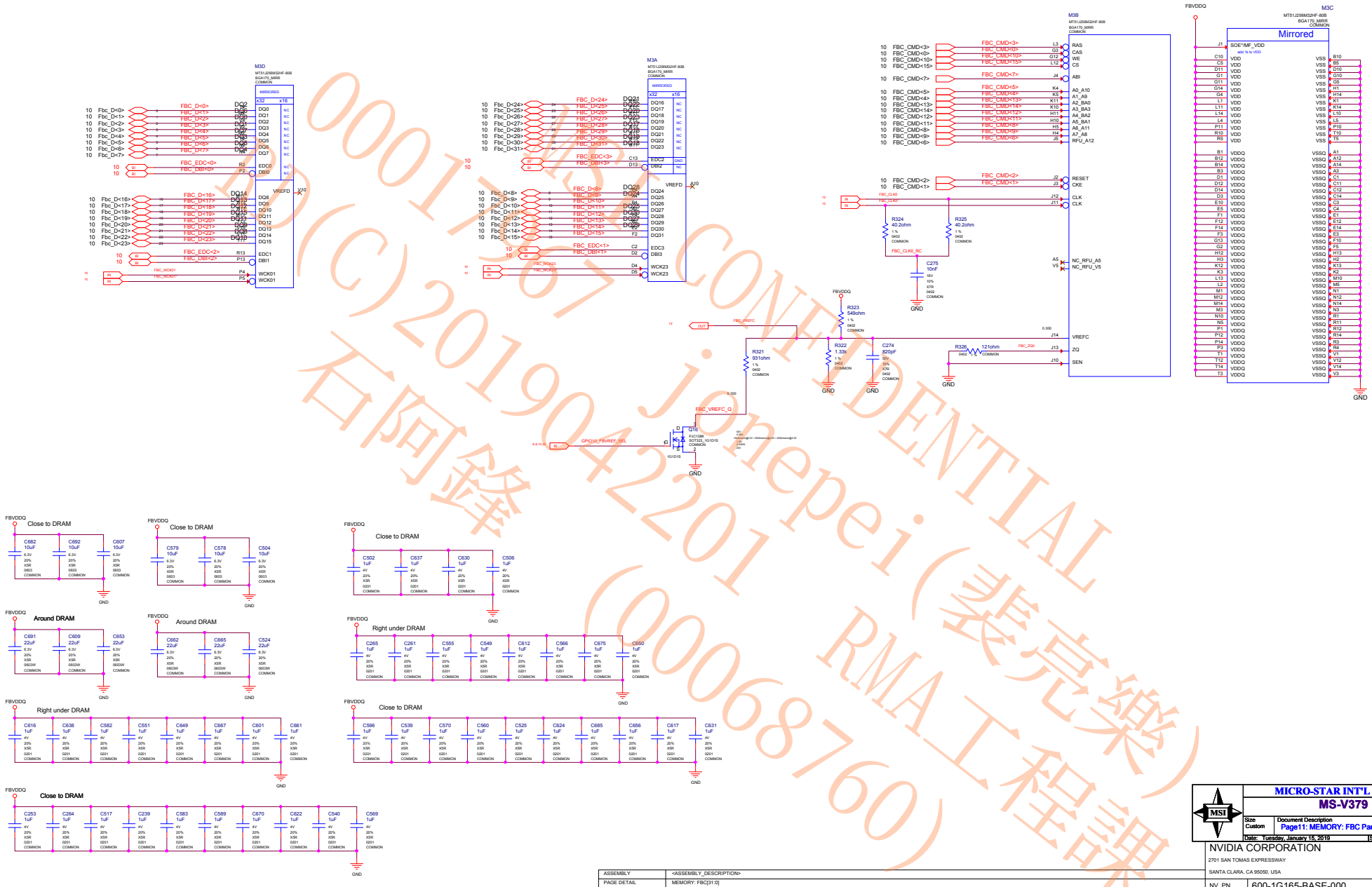
MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page10: MEMORY: GPU Partition C/D	1.0

Date: Tuesday, January 15, 2019 | Sheet 10 of 53

Page11: MEMORY: FBC Partition 31..0



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBC[31:0]

MICRO-STAR INT'L CO.,LTD

MS-V379

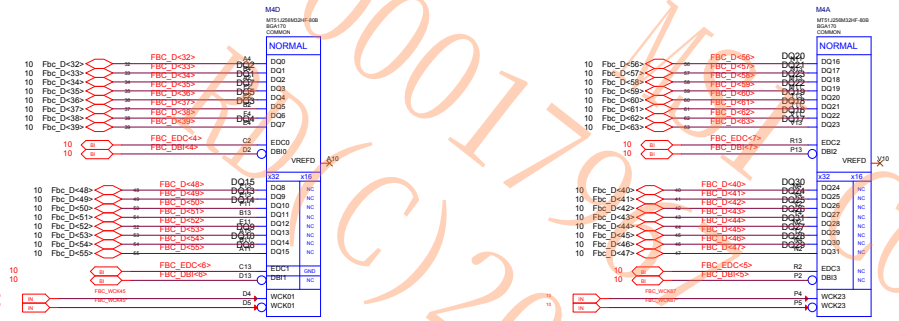
Size	Document Description	Rev
Custom	Page11: MEMORY: FBC Partition 31..0	1.0

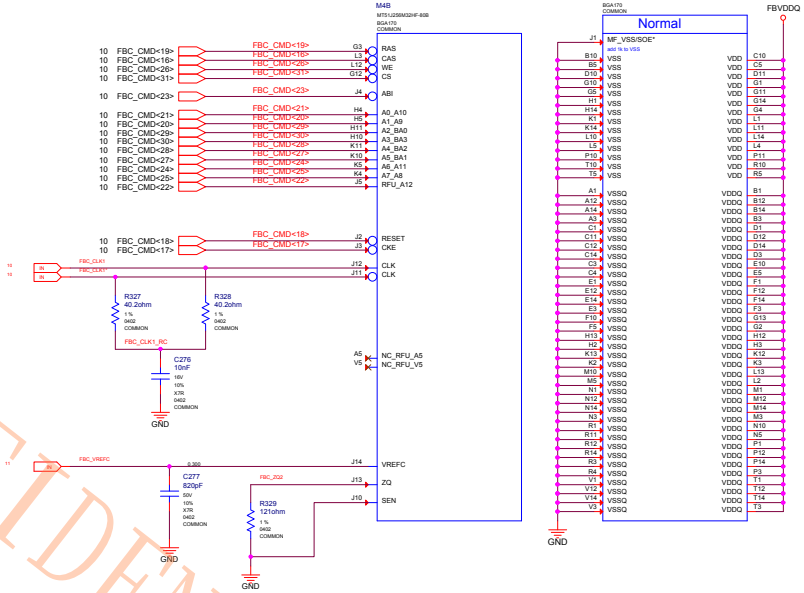
Date: Tuesday, January 15, 2019 | Sheet 11 of 53

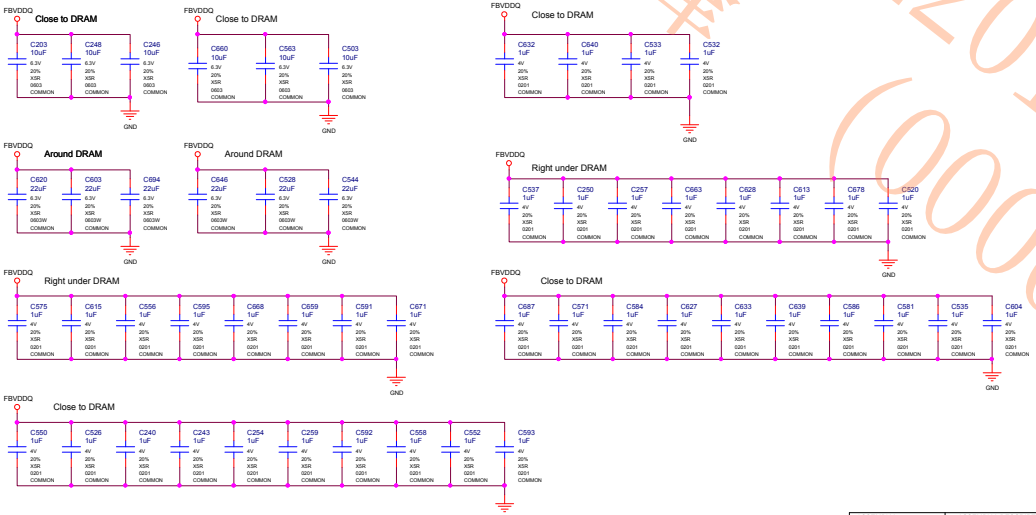
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G165-BASE-000		
PCB REV	PG165-A00	PAGE	10 OF 42
BOM REV	B	DATE	14-DEC-2018

Page12: MEMORY: FBC Partition 63..32







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBC[63:32]

MICRO-STAR INT'L CO.,LTD

MS-V379

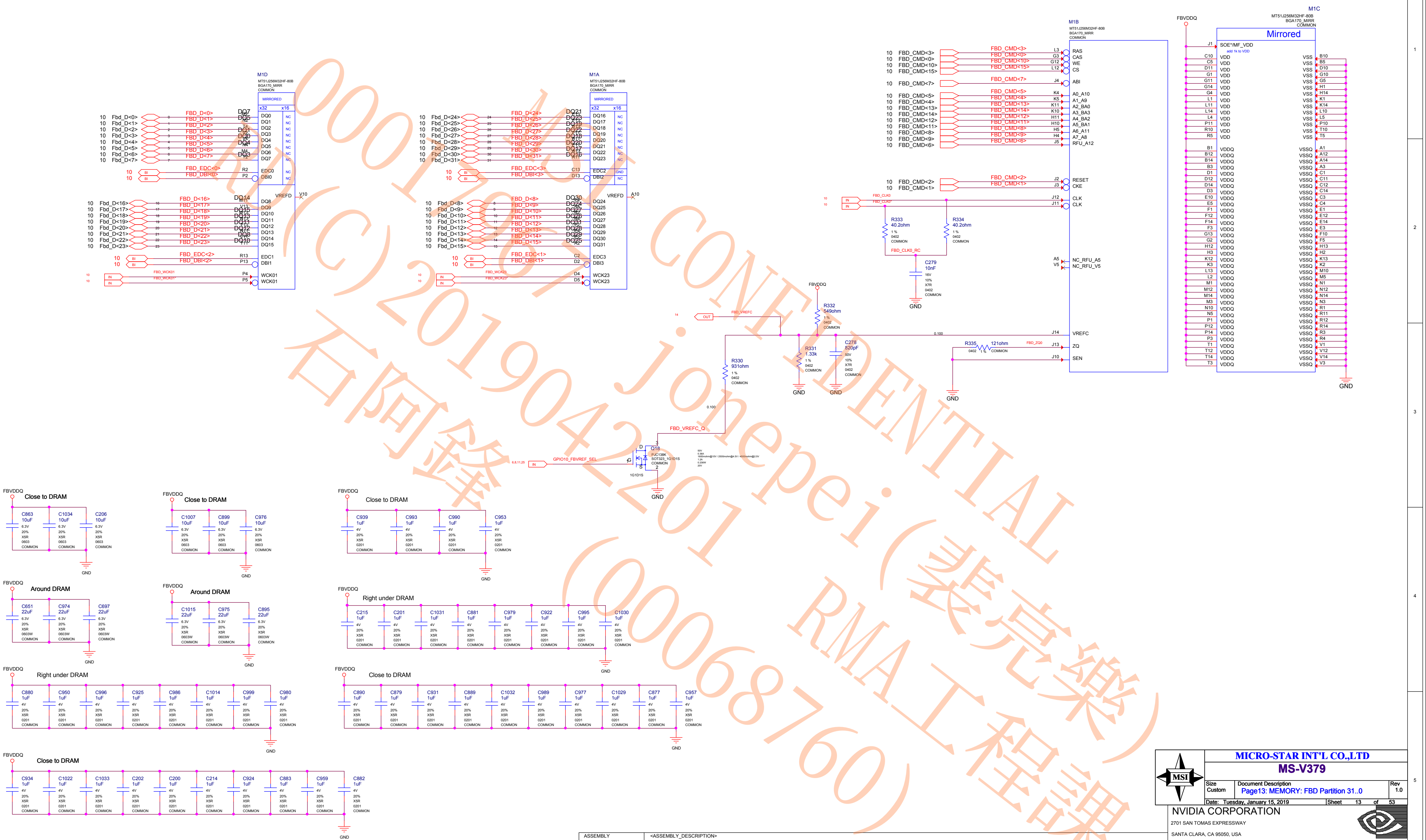
Size	Document Description	Rev
Custom	Page12: MEMORY: FBC Partition 63..32	1.0

Date: Tuesday, January 15, 2019 Sheet 12 of 53

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G165-BASE-000		
PCB REV	PG165-A00	PAGE	11 OF 42
BOM REV	B	DATE	14-DEC-2018

Page13: MEMORY: FBD Partition 31..0



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBD[31:0]

MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page13: MEMORY: FBD Partition 31..0	1.0

Date: Tuesday, January 15, 2019 | Sheet 13 of 53

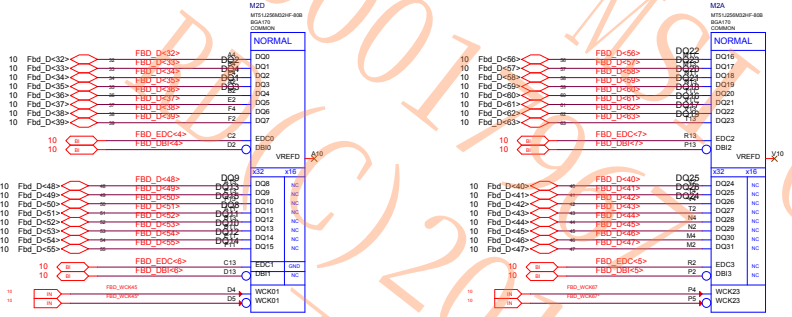
NVIDIA CORPORATION

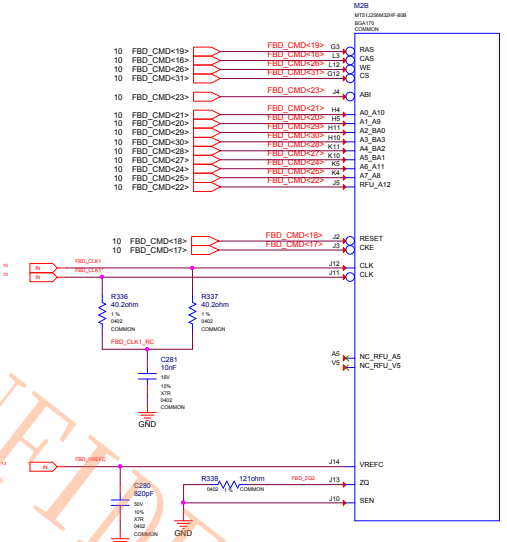
2701 SAN TOMAS EXPRESSWAY

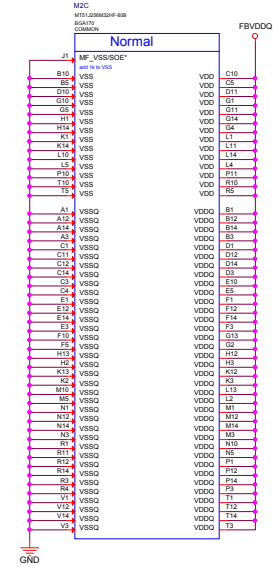
SANTA CLARA, CA 95050, USA

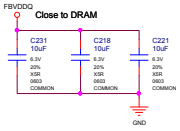
NV_PN	600-1G165-BASE-000		
PCB REV	PG165-A00	PAGE	12 OF 42
BOM REV	B	DATE	14-DEC-2018

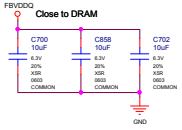
Page14: MEMORY: FBD Partition 63..32

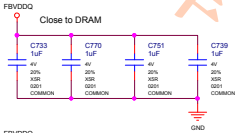


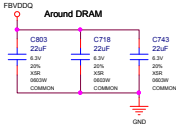


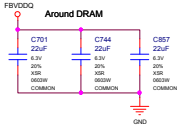


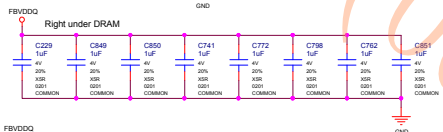


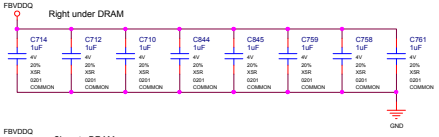


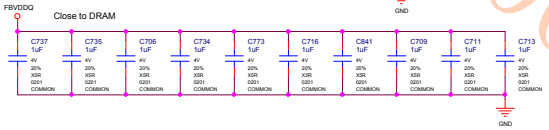


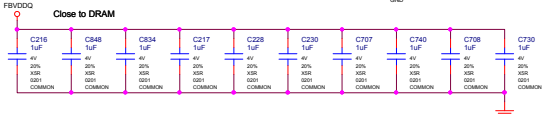












ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBD[63:32]

MICRO-STAR INT'L CO.,LTD

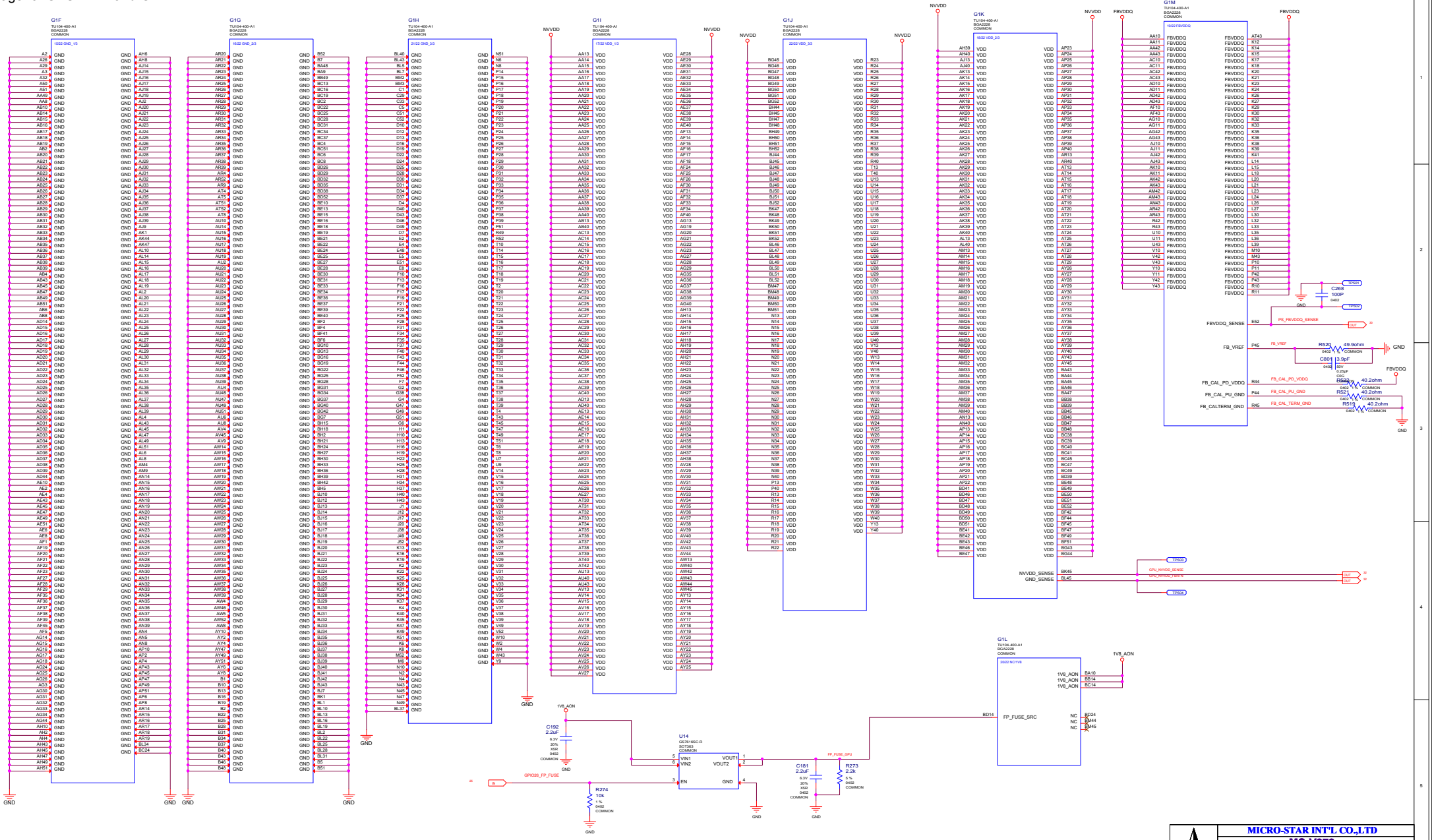
MS-V379

Size	Document Description	Rev
Custom	Page14: MEMORY: FBD Partition 63..32	1.0
Date: Tuesday, January 15, 2019	Sheet 14 of 53	

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G165-BASE-000		
PCB REV	PG165-A00	PAGE	13 OF 42
BOM REV	B	DATE	14-DEC-2018

Page15: GPU PWR and GND



MICRO-STAR INT'L CO.,LTD

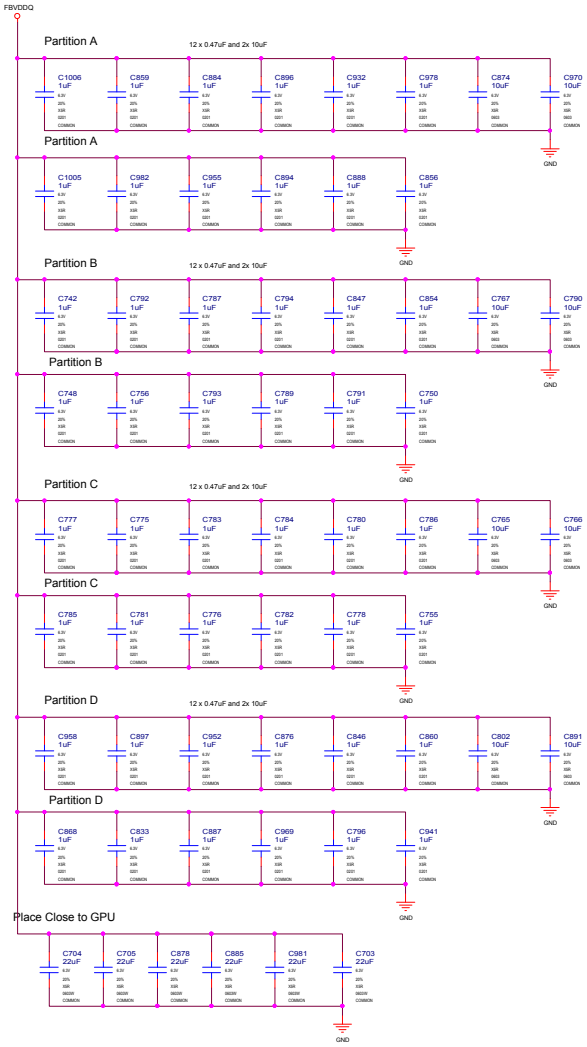
MS-V379

Size	Document Description	Rev
Custom	Page15: GPU PWR and GND	1.0

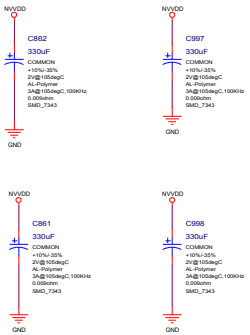
Date: Tuesday, January 15, 2019 | Sheet 15 of 53

Page16: GPU Decoupling 1

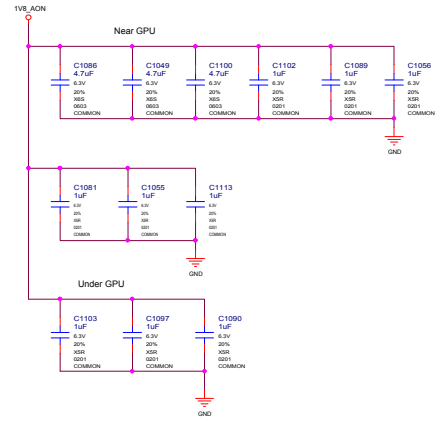
FBVDDQ



NVVDD



1V8_AON



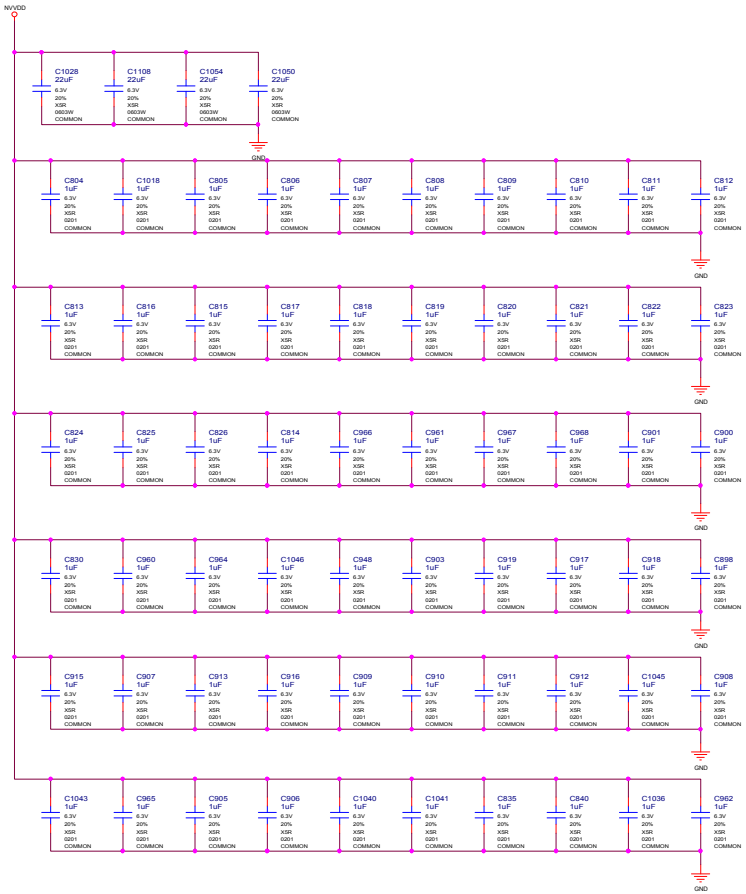
MICRO-STAR INT'L CO.,LTD

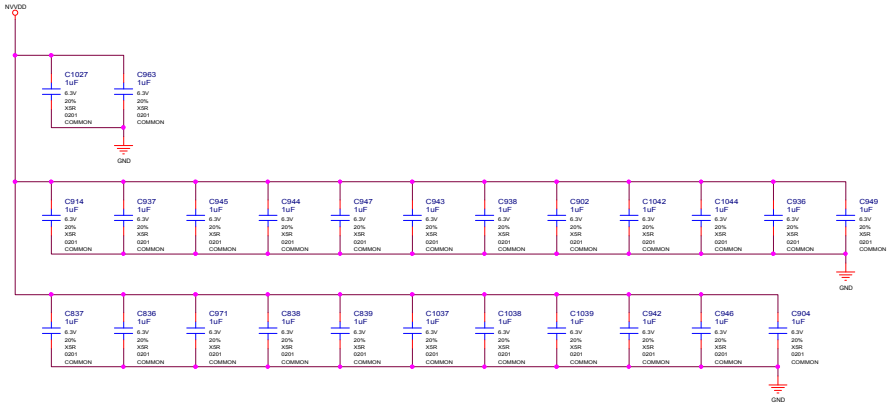
MS-V379

Size	Document Description	Rev
Custom	Page16: GPU Decoupling 1	1.0
Date: Tuesday, January 15, 2019	Sheet 16 of 53	

Page17: GPU Decoupling 2

NVVDD





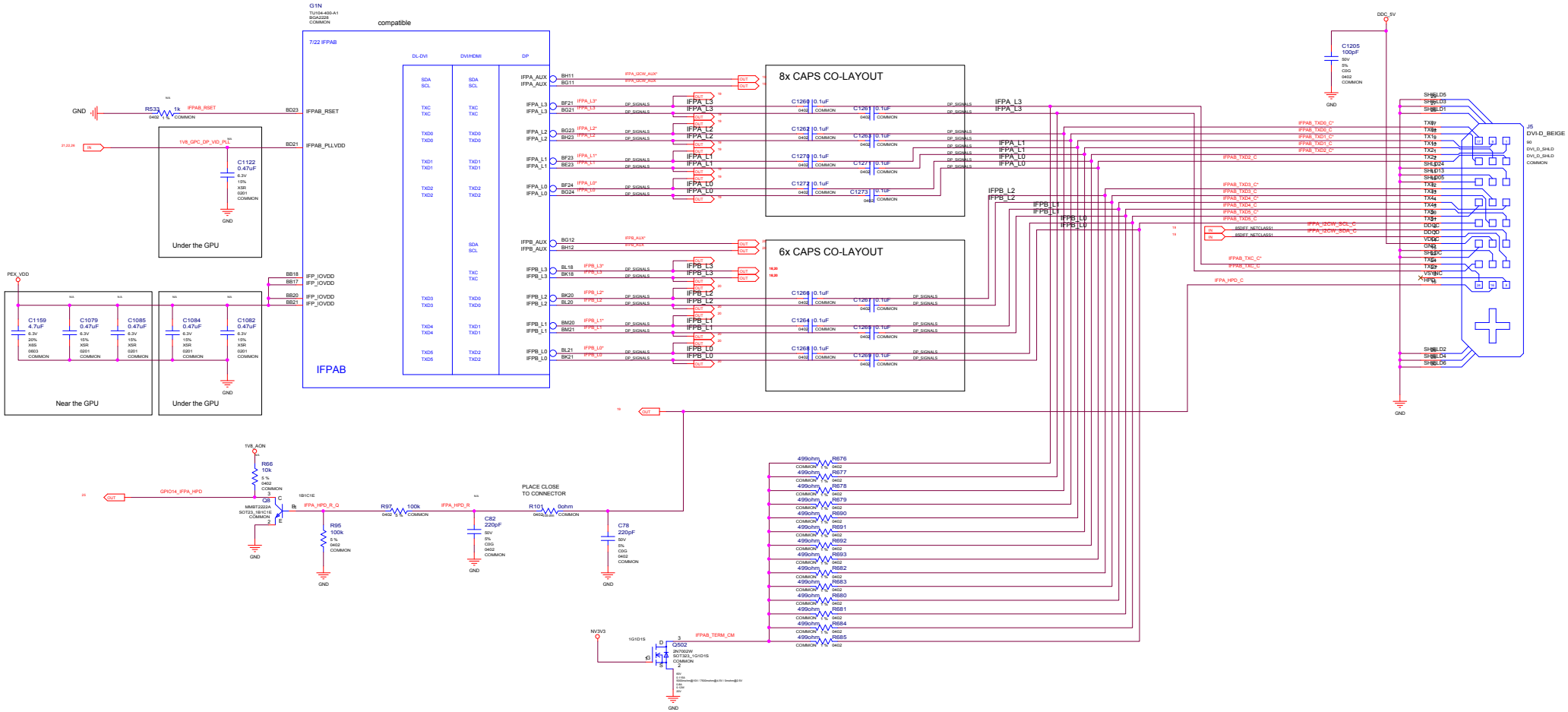
MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page17: GPU Decoupling 2	1.0

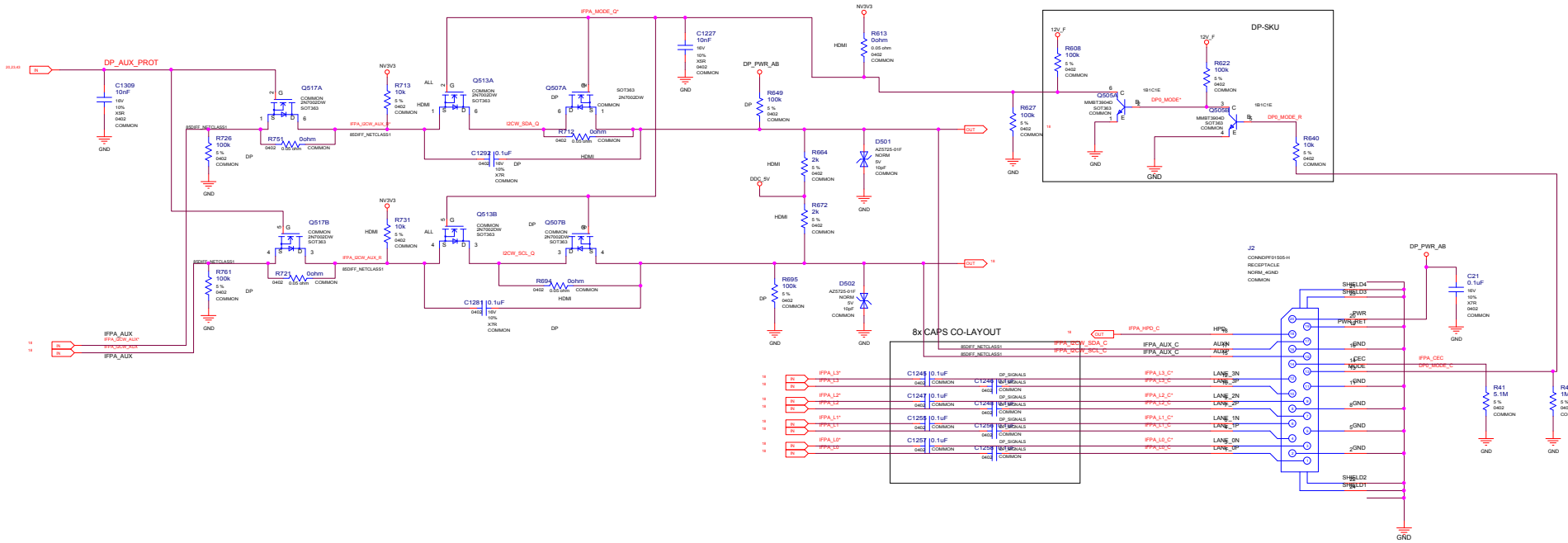
Date: Tuesday, January 15, 2019 Sheet 17 of 53

IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



MICRO-STAR INT'L CO.,LTD
MS-V379

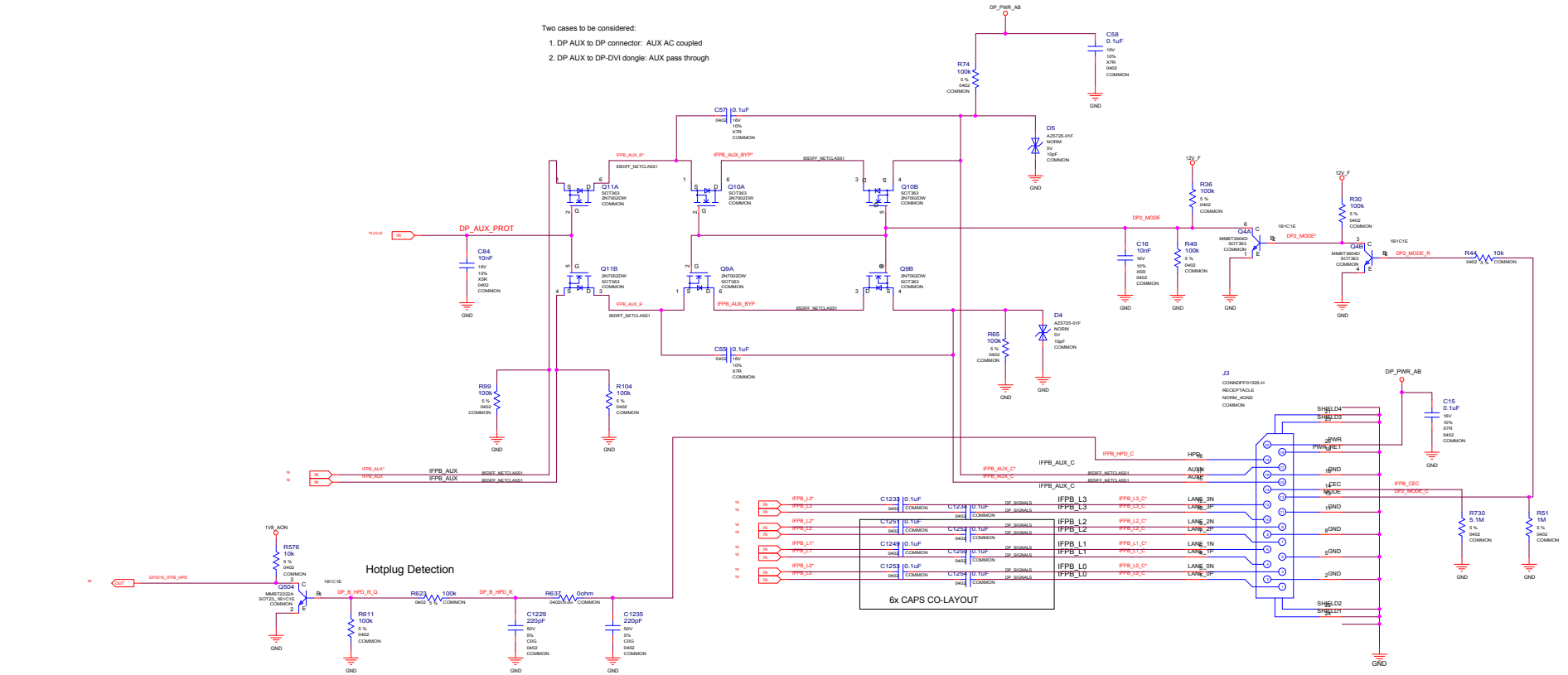
Size	Document Description	Rev
Custom	Page18: IFPAB DVI-D-DL	1.0
Date: Tuesday, January 15, 2019	Sheet 18 of 53	



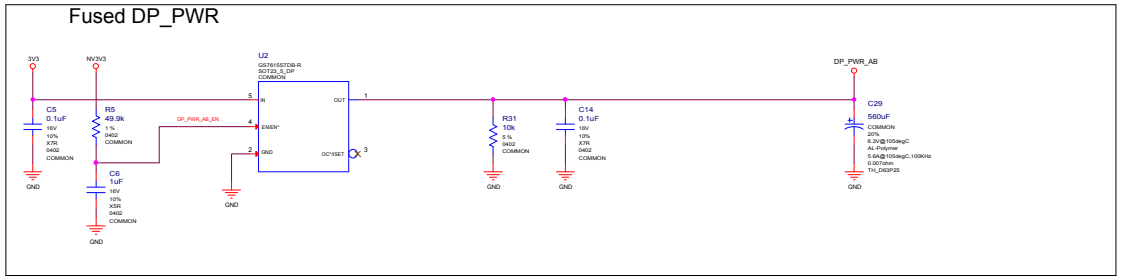
IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

MICRO-STAR INT'L CO.,LTD			
MS-V379			
Size: Custom	Document Description: Page19: IFPA DP		Rev: 1.0
Date: Tuesday, January 15, 2019		Sheet 19 of 53	

IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL



Fused DP_PWR



MSI

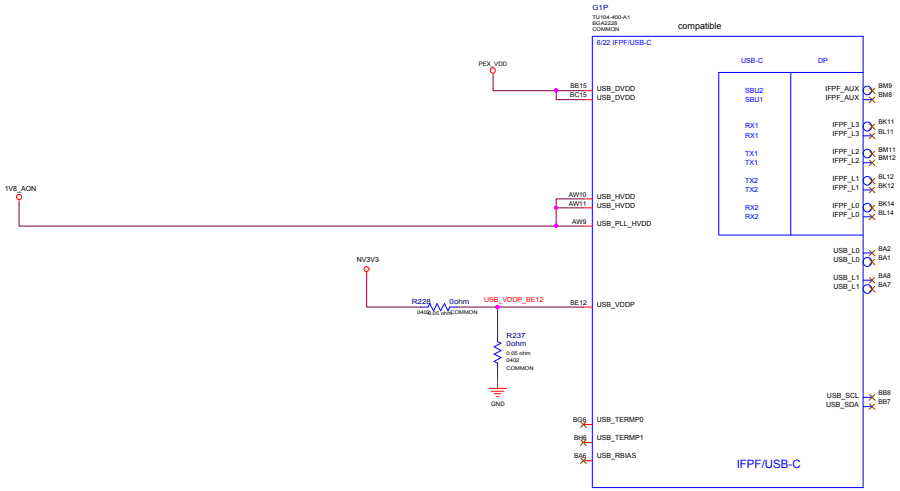
MICRO-STAR INT'L CO.,LTD

MS-V379

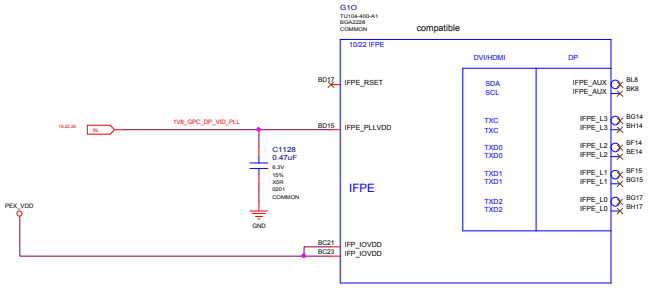
Size	Document Description	Rev
Custom	Page20: IFPB DP	1.0

Date: Tuesday, January 15, 2019 Sheet 20 of 53

Page21: IFPE & IFPF USB-C NC



IFPF NC



IFPE NC

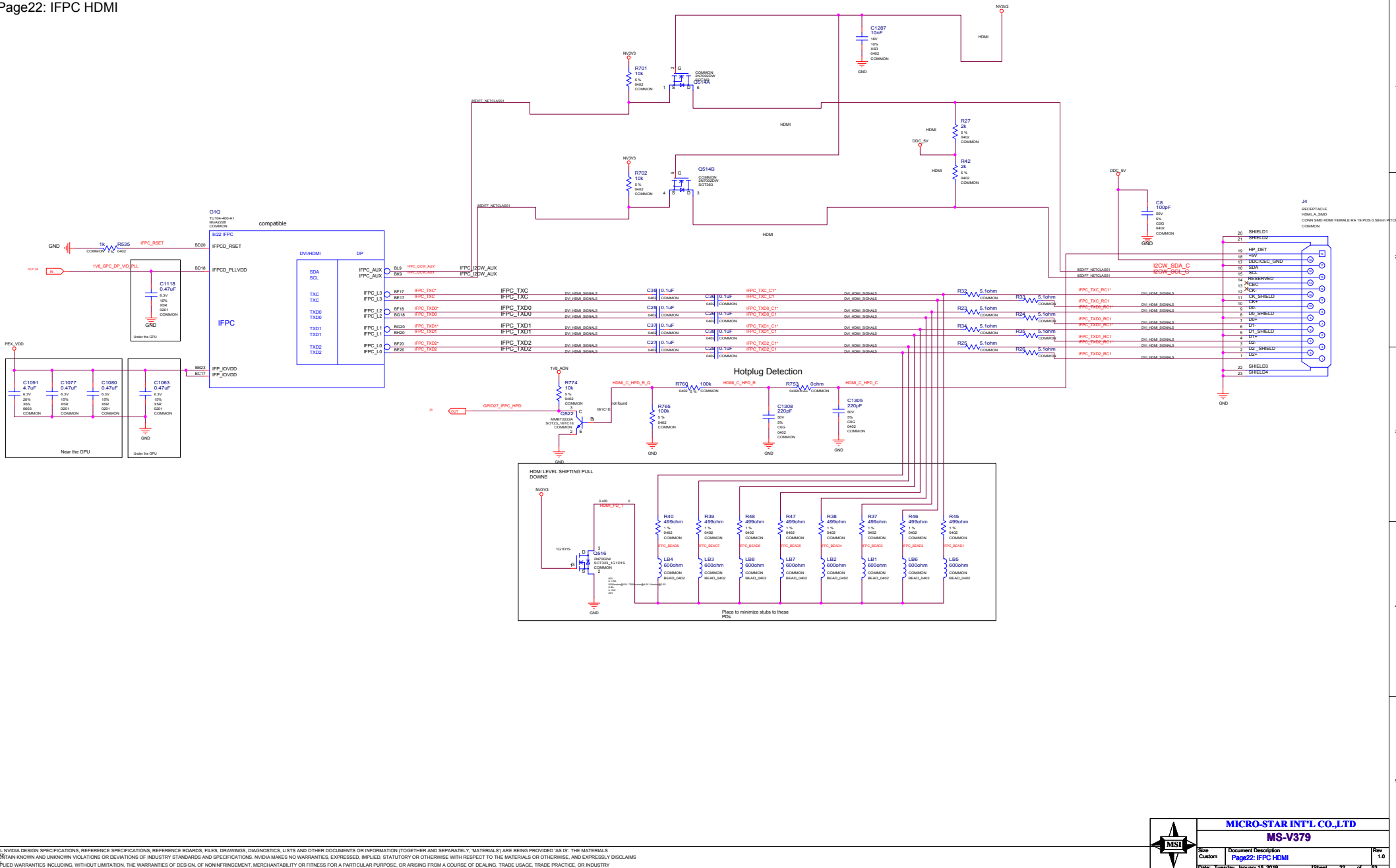
IO: IFPE & IFPF USBC NC

MICRO-STAR INT'L CO.,LTD
MS-V379

Size	Document Description	Rev
Custom	Page21: IFPE & IFPF USB-C NC	1.0
Date: Tuesday, January 15, 2019	Sheet 21 of 53	

21-OCT-2018

Page22: IFPC HDMI



MICRO-STAR INT'L CO.,LTD

MS-V379

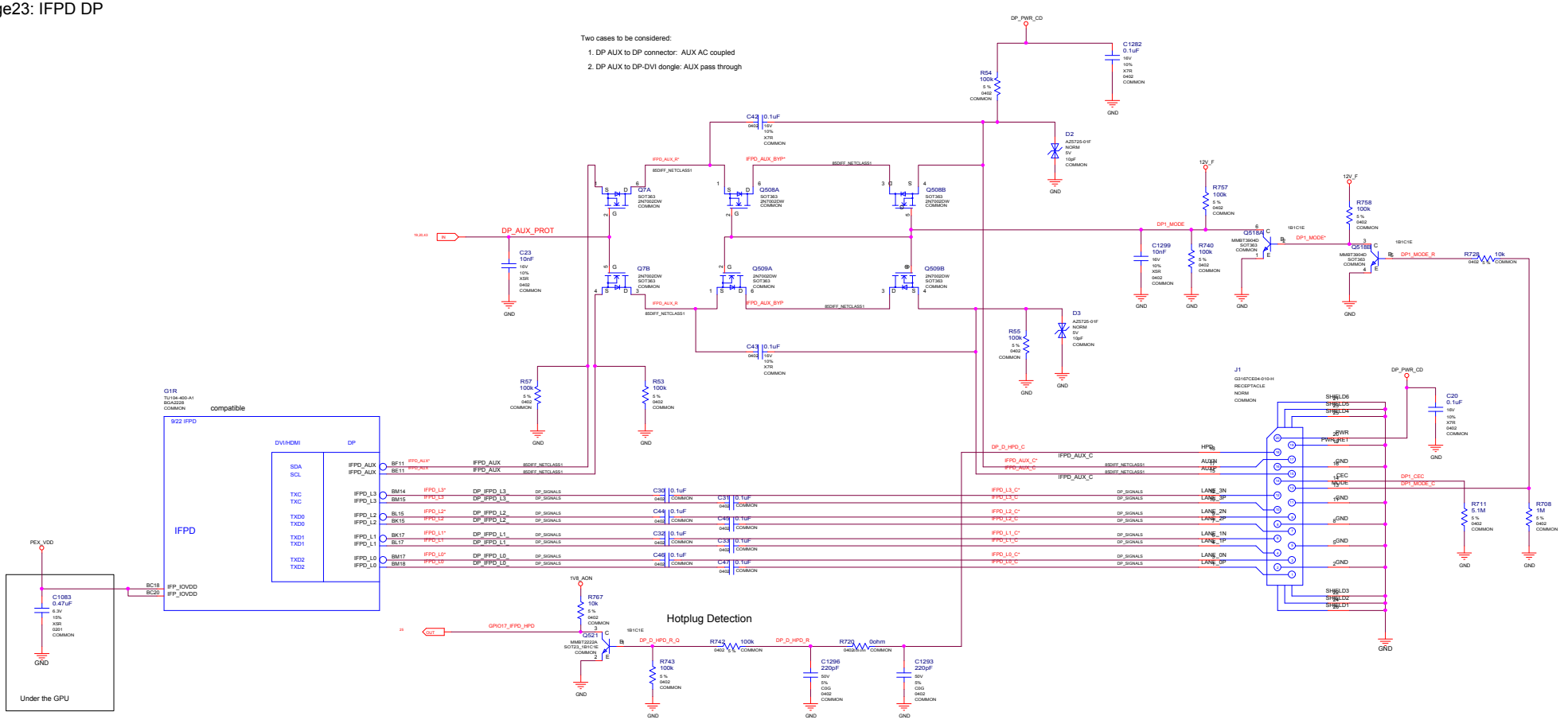
Size	Document Description	Rev
Custom	Page22: IFPC HDMI	1.0

Date: Tuesday, January 15, 2019 Sheet 22 of 53

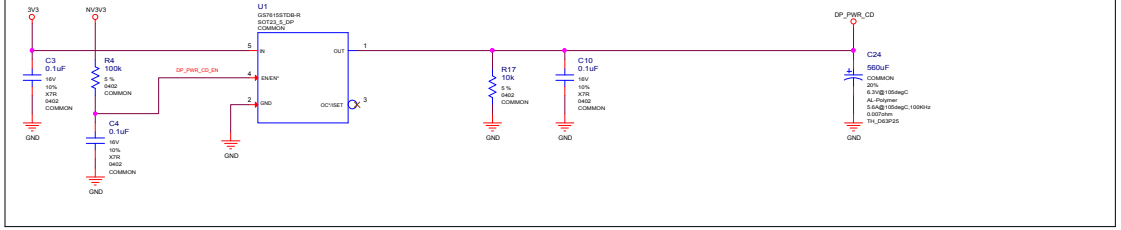
Page23: IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR



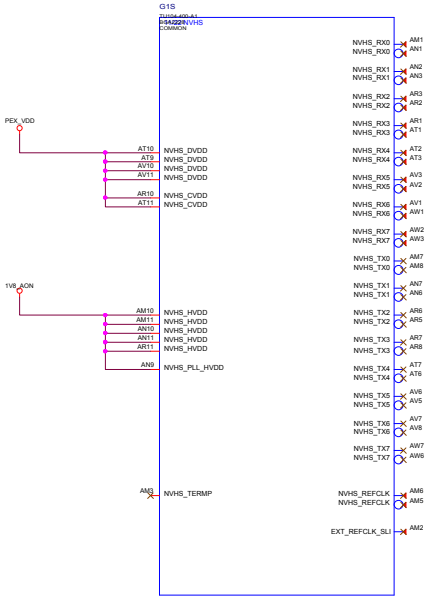
MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page23: IFPD DP	1.0

Date: Tuesday, January 15, 2019 Sheet 23 of 53

Page24: NVHS Interface and Frame Lock



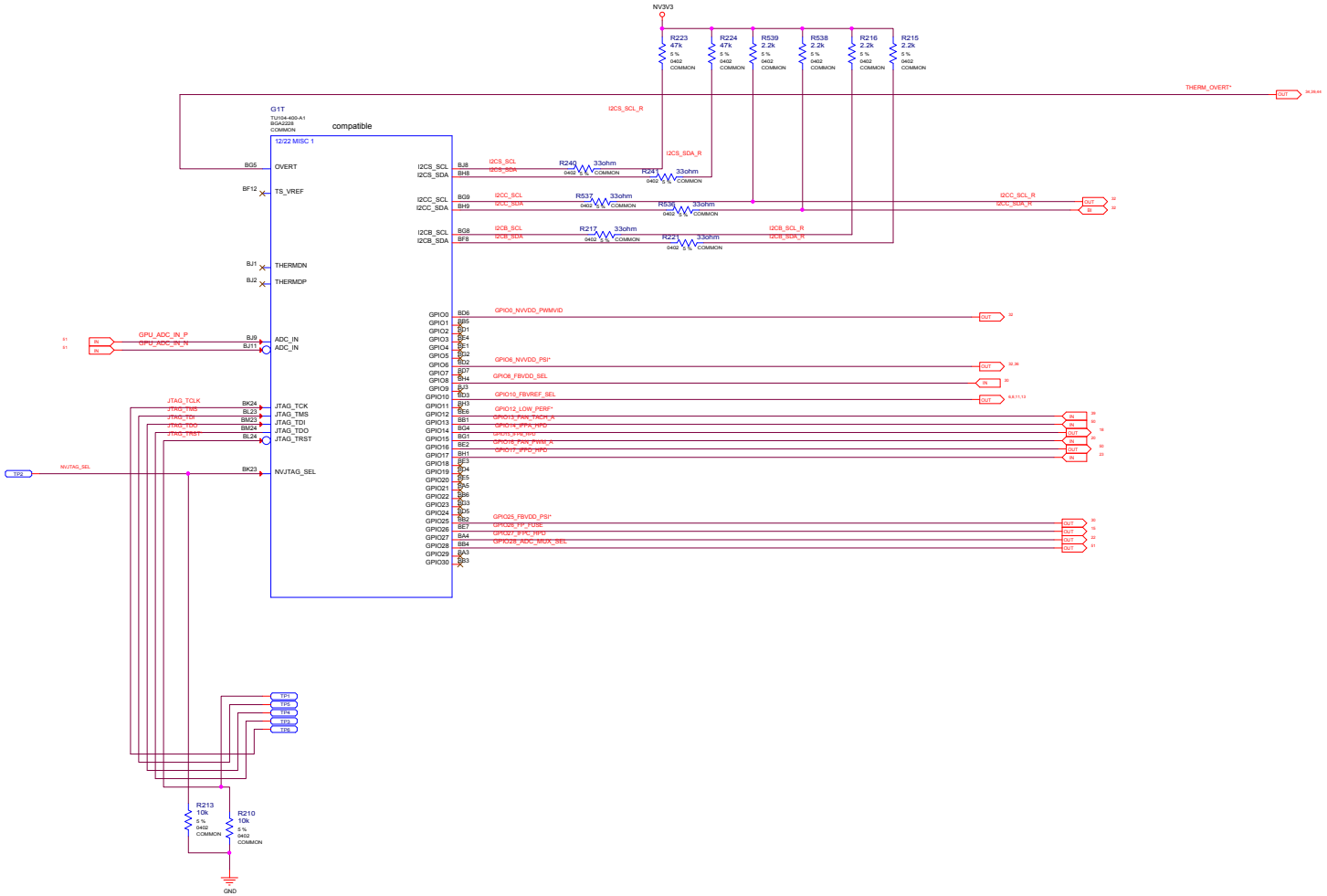
MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page24: NVHS Interface and Frame Lock	1.0

Date: Tuesday, January 15, 2019 | Sheet 24 of 53

Page25: MISC1: Fan, Thermal, JTAG, GPIO



MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page25: MISC1: Fan, Thermal, JTAG, GPIO	1.0

Date: Tuesday, January 15, 2019 Sheet 25 of 53

Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

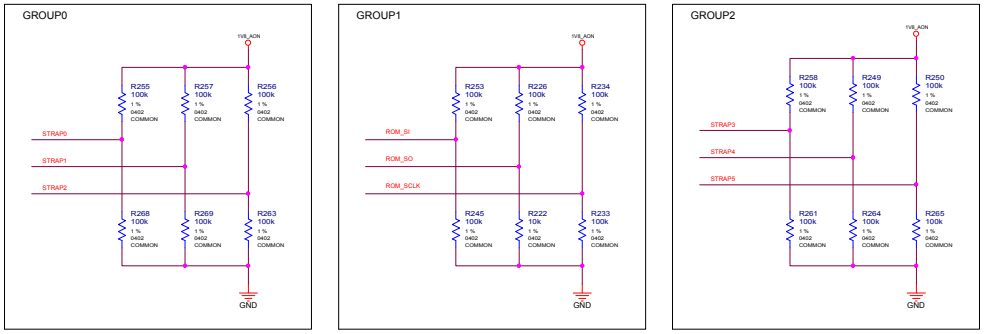
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

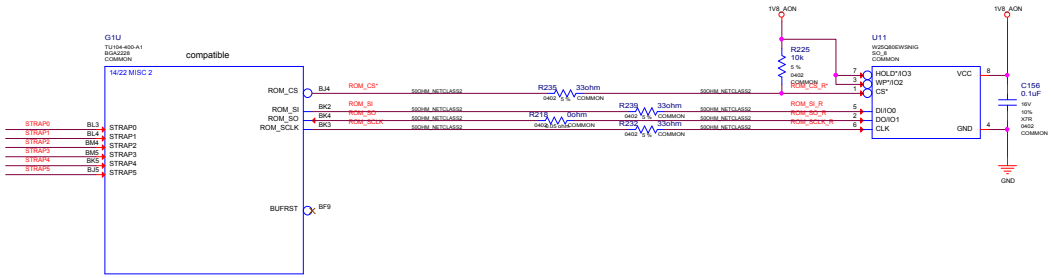
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

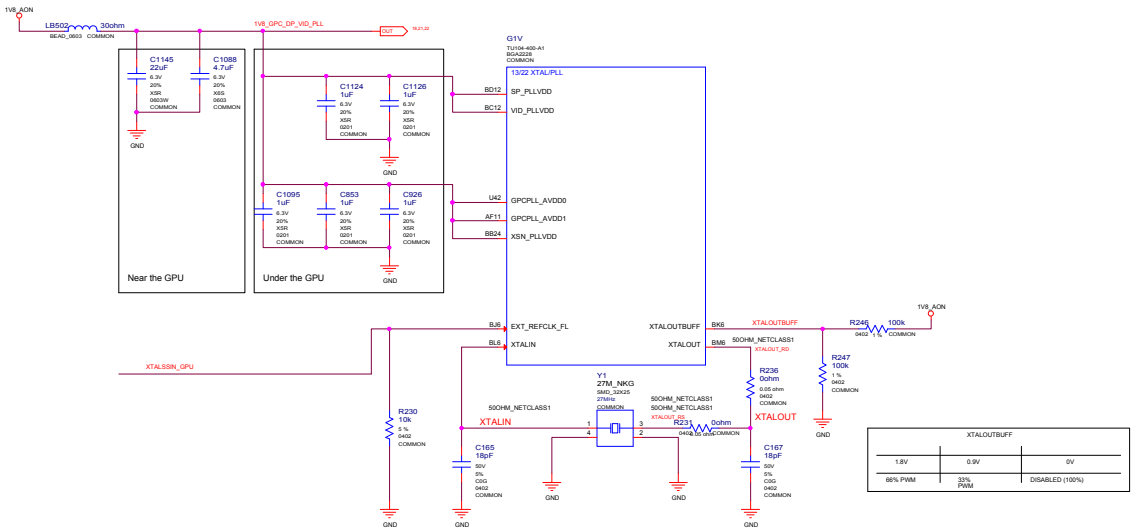
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



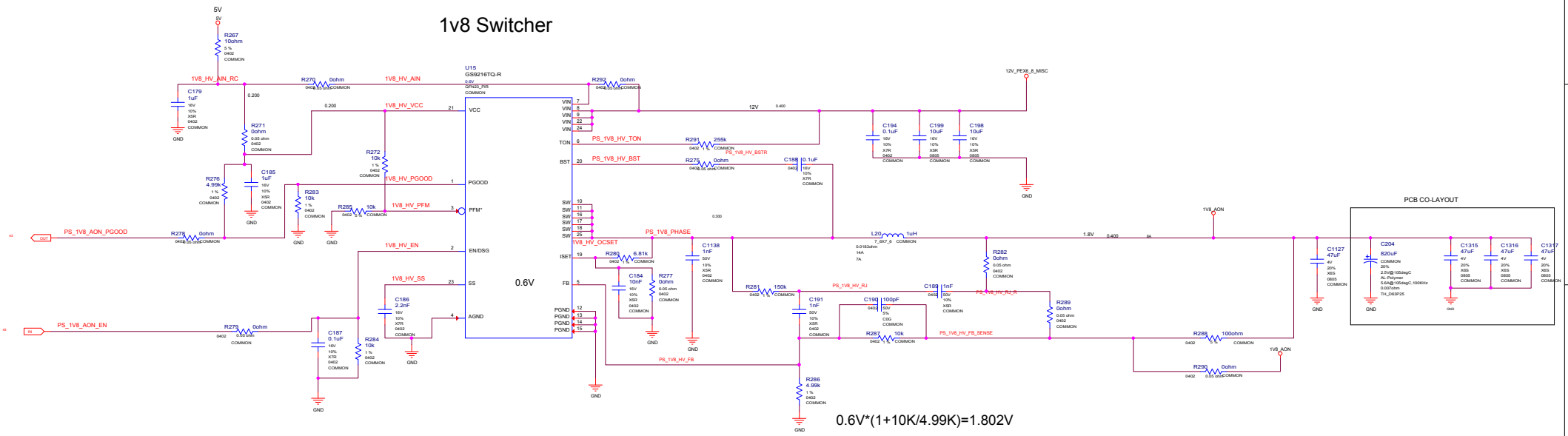




MICRO-STAR INT'L CO.,LTD
MS-V379

Size	Document Description	Rev
Custom	Page26: MISC2: ROM, XTAL, Straps	1.0
Date: Tuesday, January 15, 2019	Sheet 26 of 53	

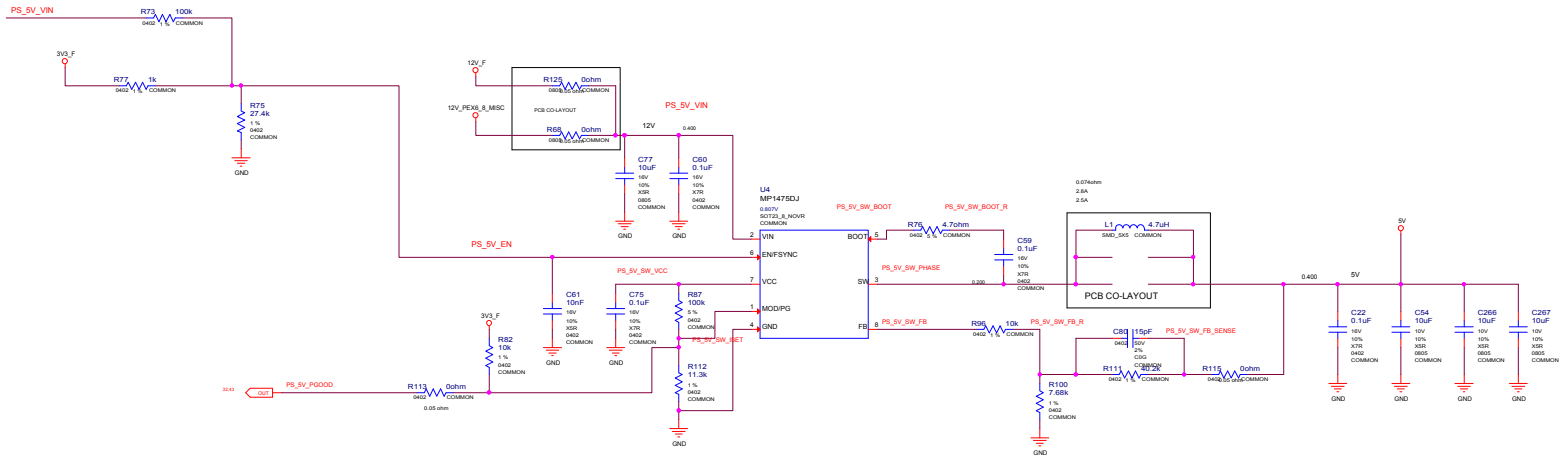
Page27: PS: 1V8_AON



MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page27: PS: 1V8_AON	1.0
Date: Tuesday, January 15, 2019	Sheet 27 of 53	



0.8V*(1+40.2K/7.68K)=4.9875V

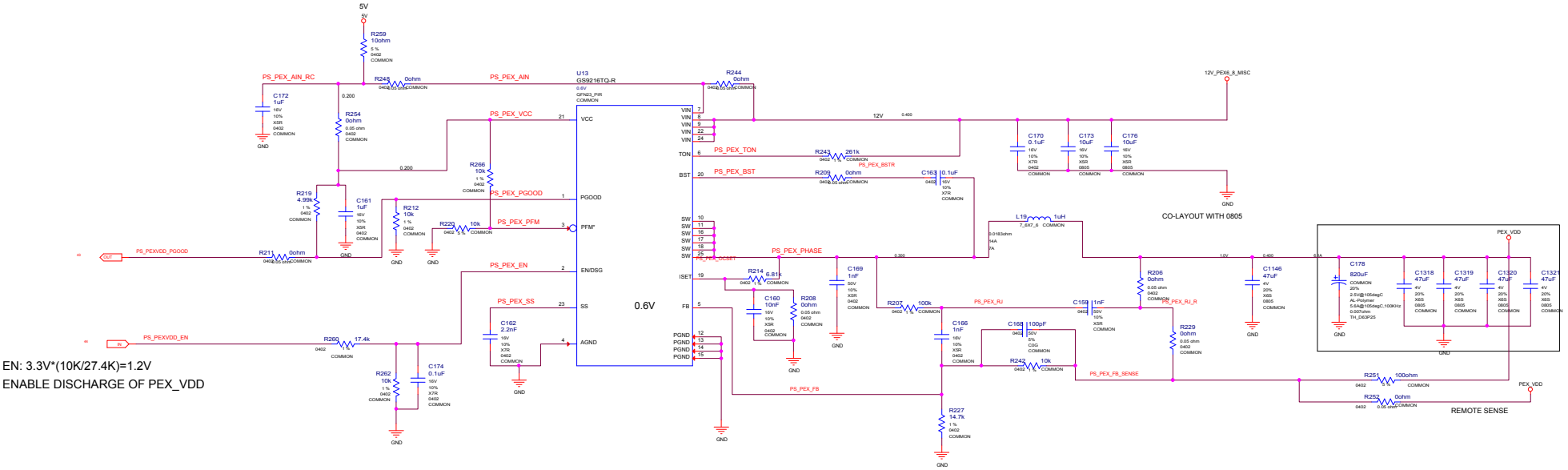
MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page28: PS: 5V	1.0

Date: Tuesday, January 15, 2019 Sheet 28 of 53

PEX Switcher



EN: 3.3V*(10K/27.4K)=1.2V

ENABLE DISCHARGE OF PEX_VDD

0.6V*(1+10K/14.7K)=1.008V

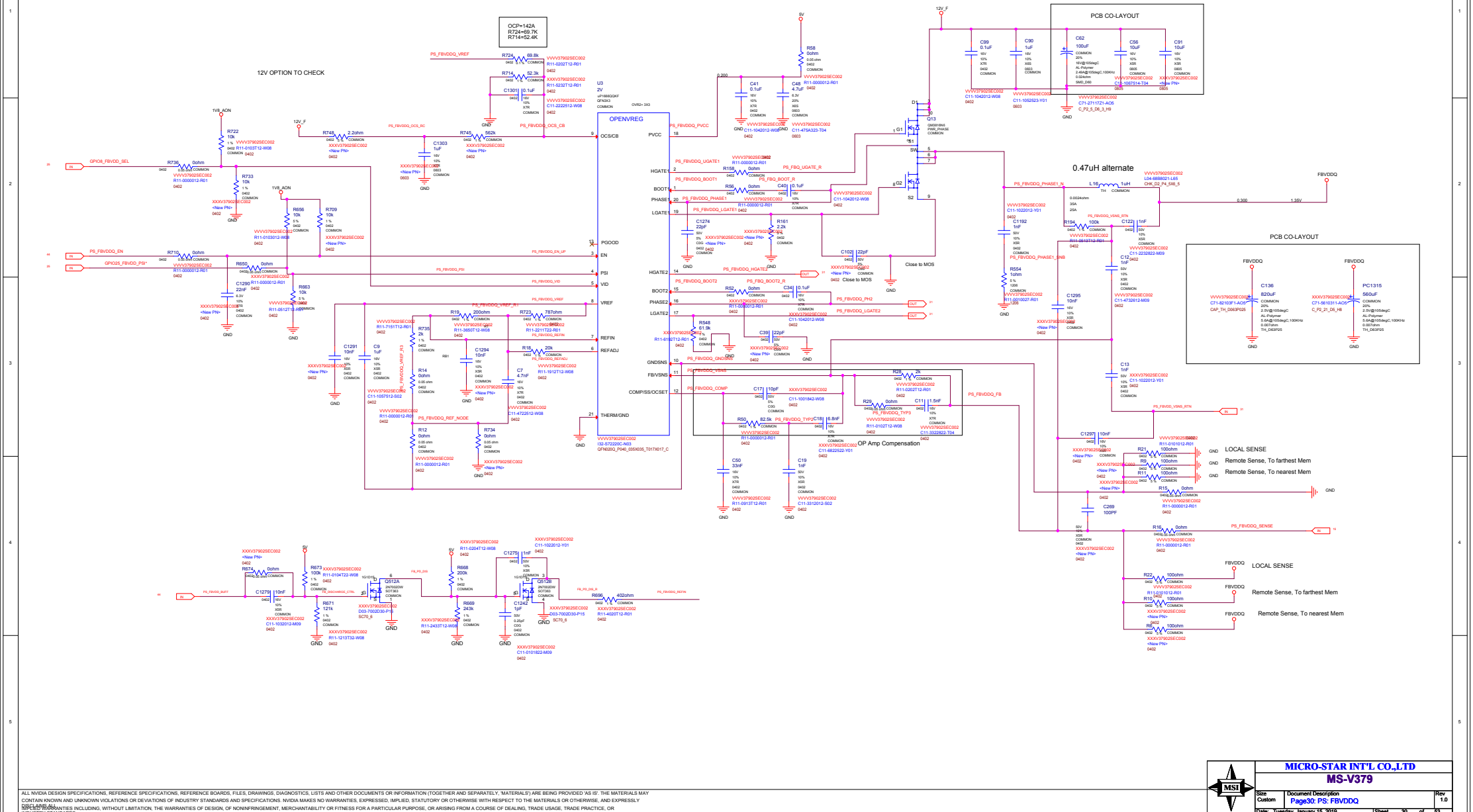
MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page29: PS: PEXVDD	1.0

Date: Tuesday, January 15, 2019 Sheet 29 of 53

Page30: PS: FBVDDQ



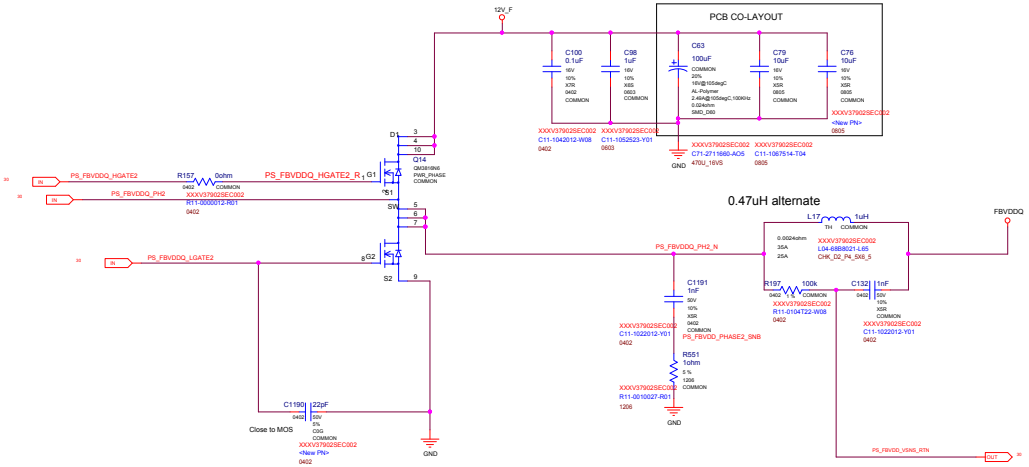
MICRO-STAR INT'L CO.,LTD

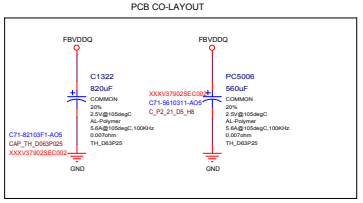
MS-V379

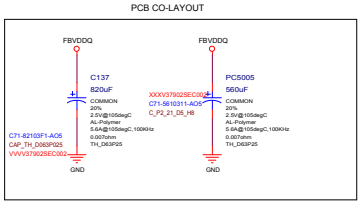
Size	Document Description	Rev
Custom	Page30: PS: FBVDDQ	1.0

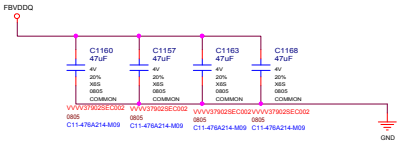
Date: Tuesday, January 15, 2019 Sheet 30 of 53

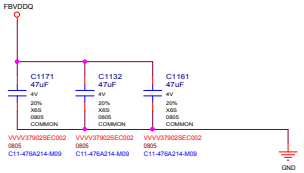
Page31: PS: FBVDDQ PH2











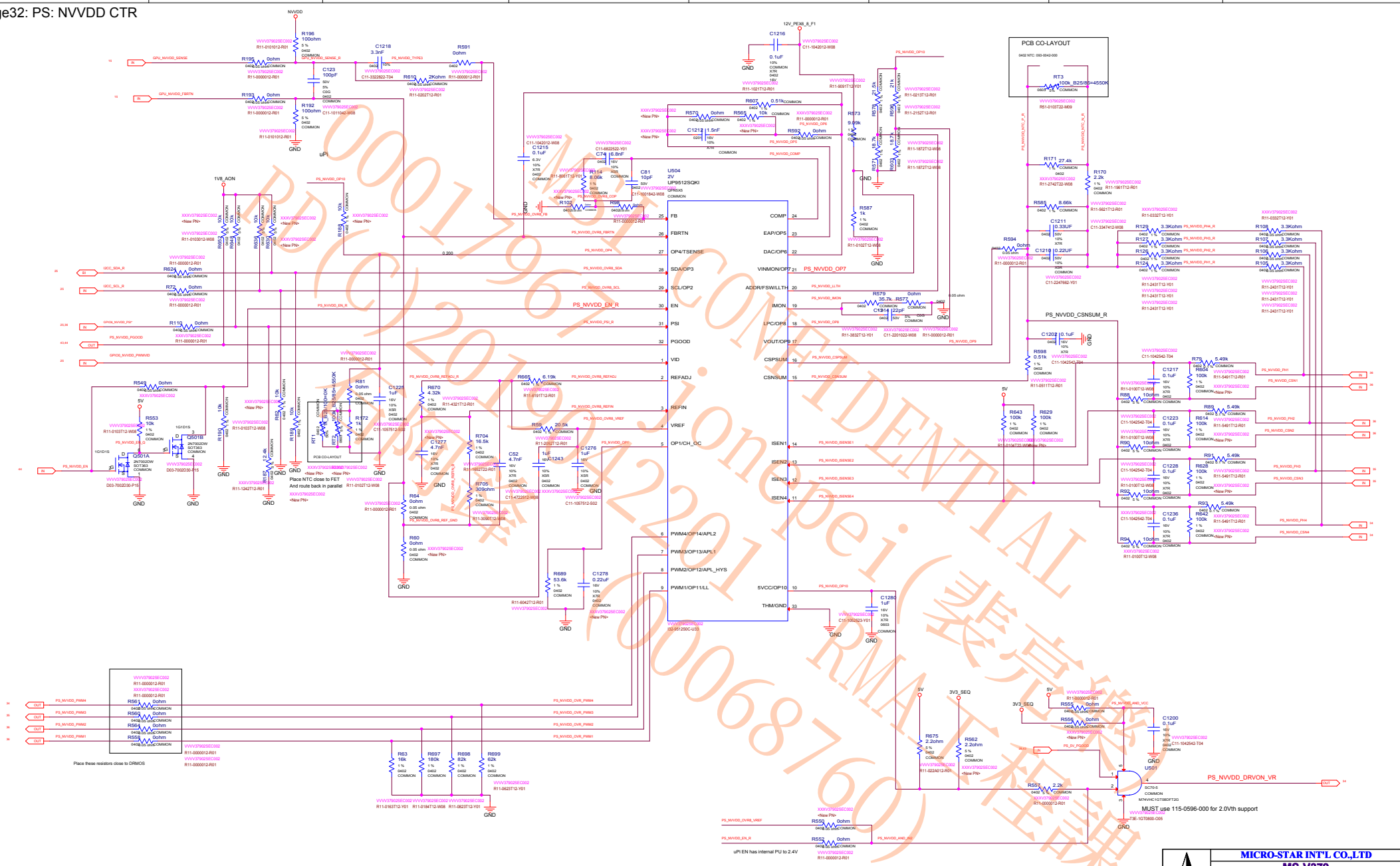
MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page31: PS: FBVDDQ PH2	1.0

Date: Tuesday, January 15, 2019 Sheet 31 of 53

Page32: PS: NVVDD CTR



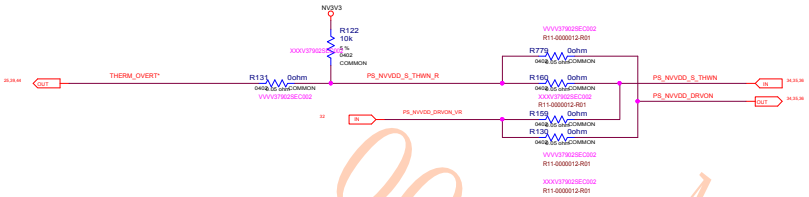
MICRO-STAR INT'L CO.,LTD

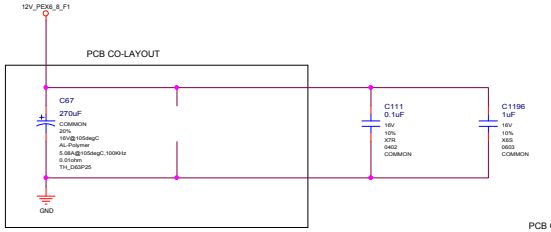
MS-V379

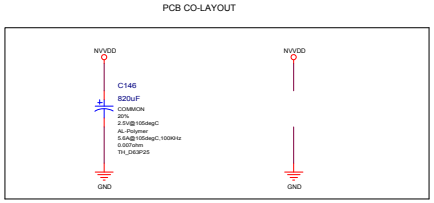
Size	Document Description	Rev
Custom	Page32: PS: NVVDD CTR	1.0
Date: Tuesday, January 15, 2019	Sheet 32 of 53	

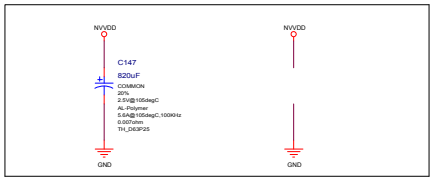
DROP OVR3i SOLUTION

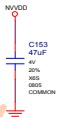
Page34: PS: NVVDD PH6&4

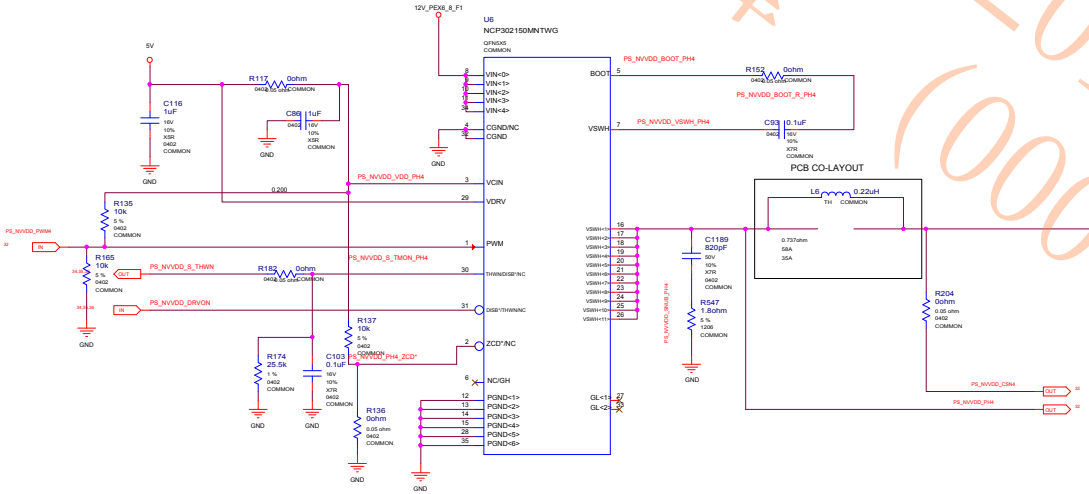


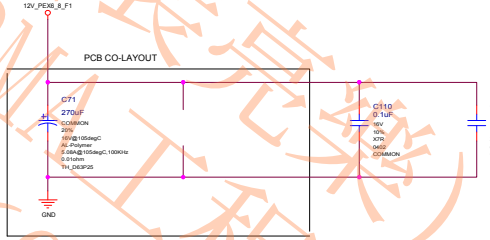












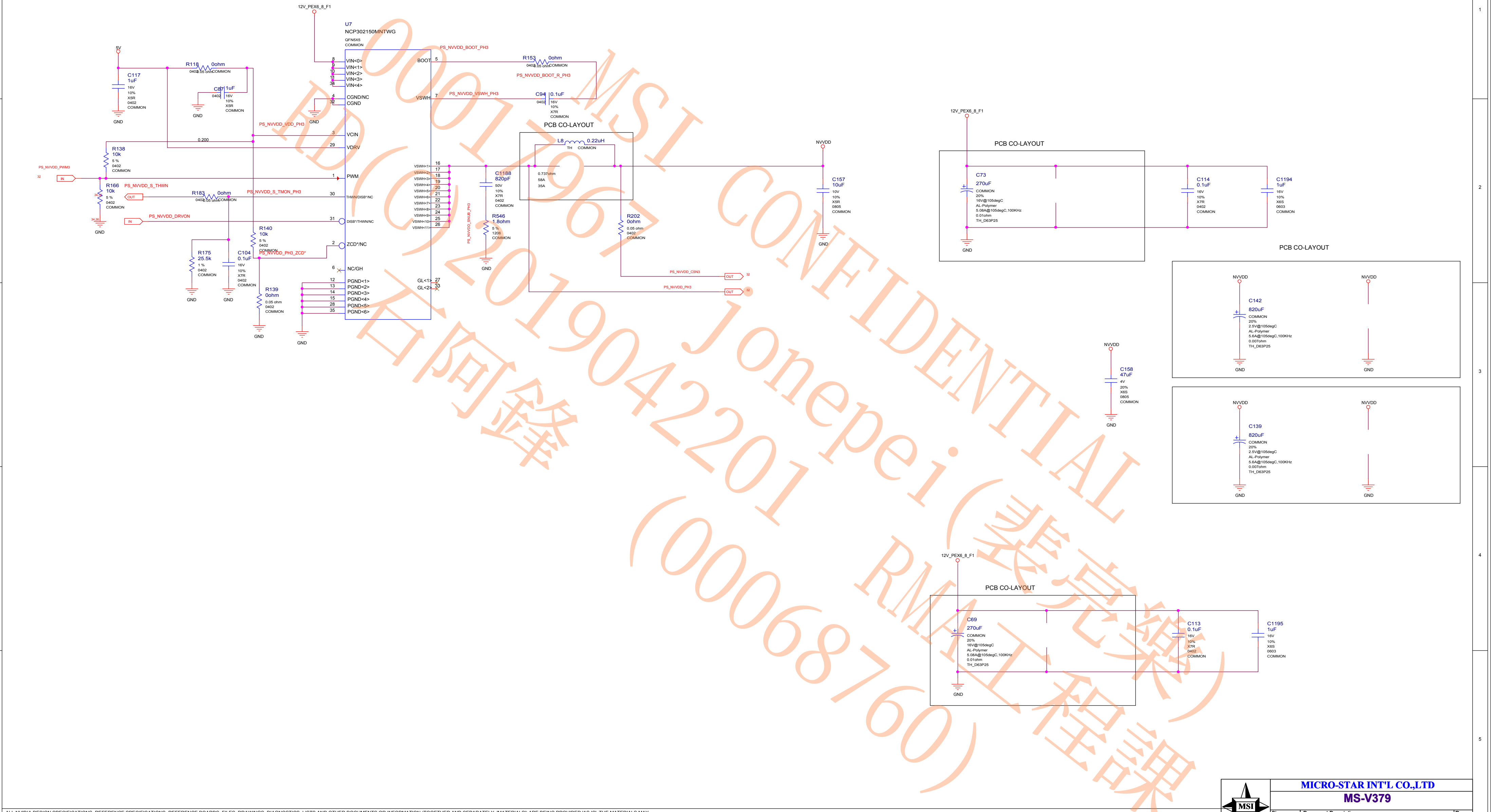
MICRO-STAR INT'L CO.,LTD

MS-V379

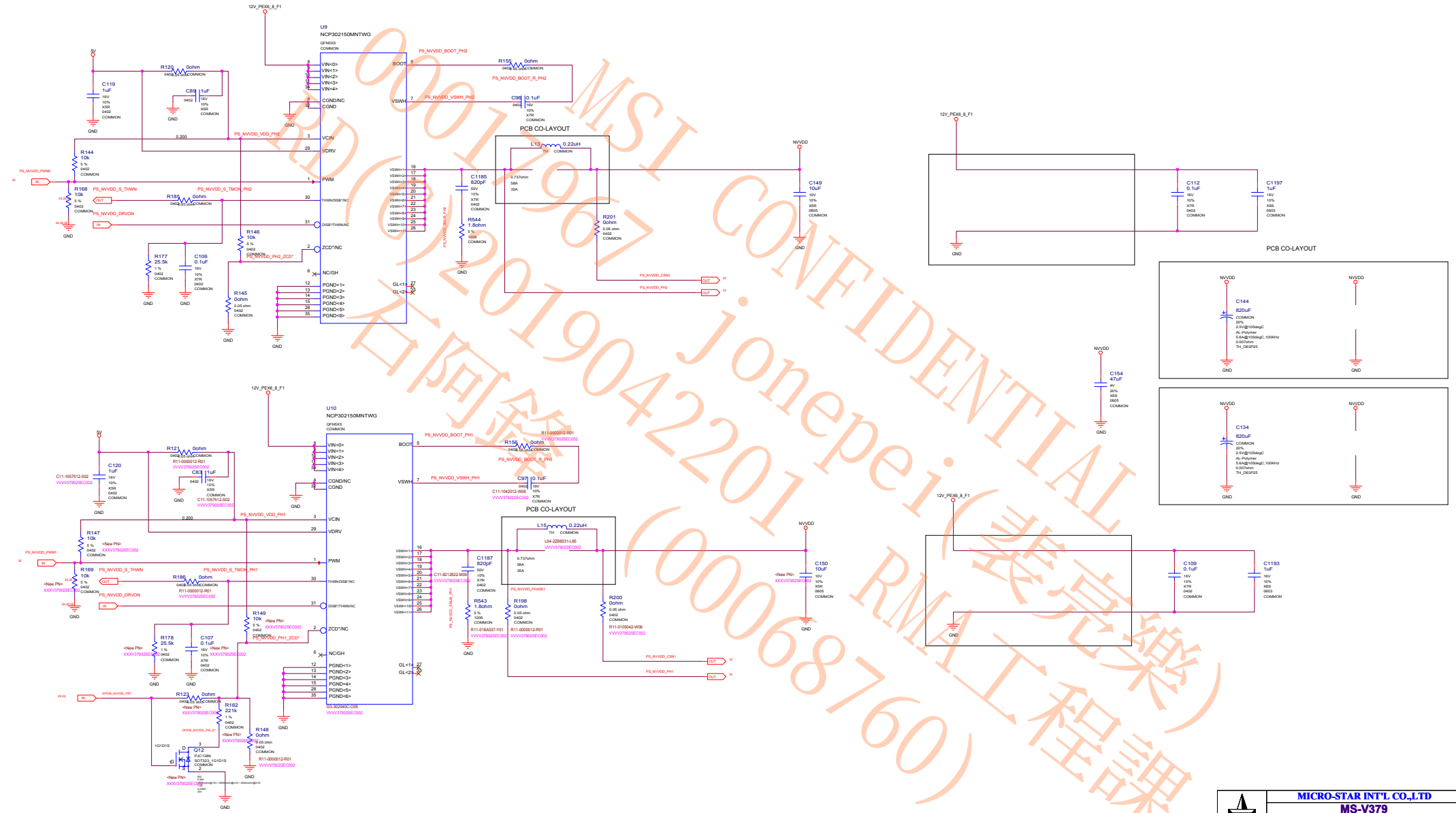
Size: Custom | Document Description: Page34: PS: NVVDD PH6&4 | Rev: 1.0

Date: Tuesday, January 15, 2019 | Sheet 34 of 53

Page35: PS: NVVDD PH3&5



Page36: PS: NVVDD PH2&1



MICRO-STAR INT'L CO.,LTD

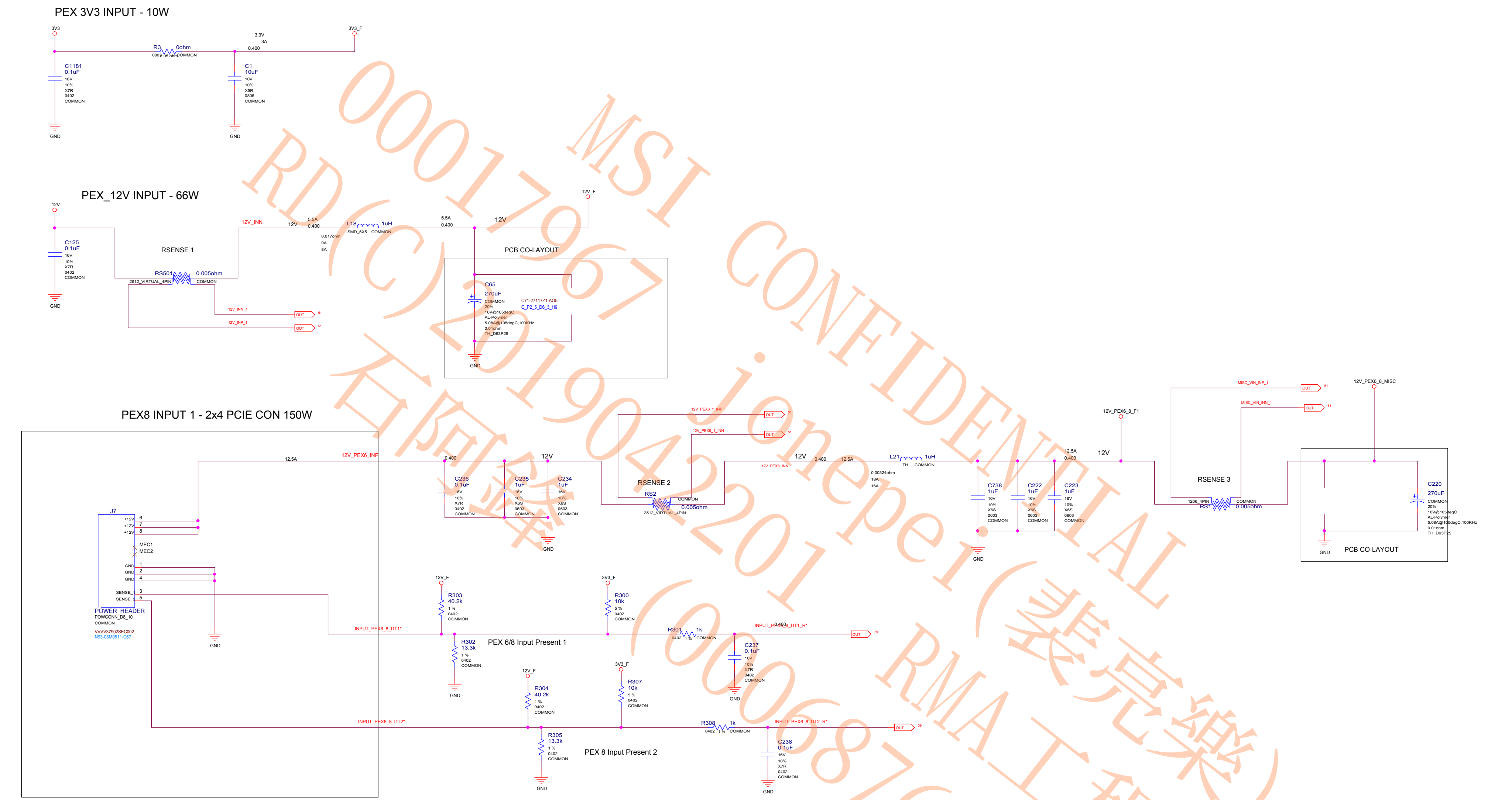
MS-V379

Size	Document Description	Rev
Custom	Page36: PS: NVVDD PH2&1	1.0

Date: Tuesday, January 15, 2019 Sheet 36 of 53

DELETE RAIL BALANCE CIRCUIT

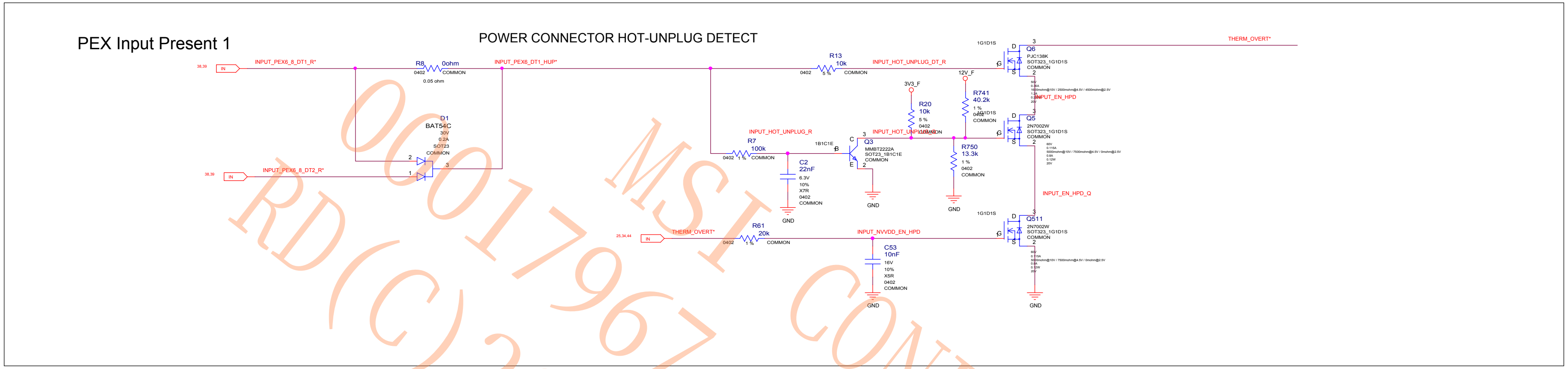
Page38: PS: Inputs, Filtering, and Monitoring

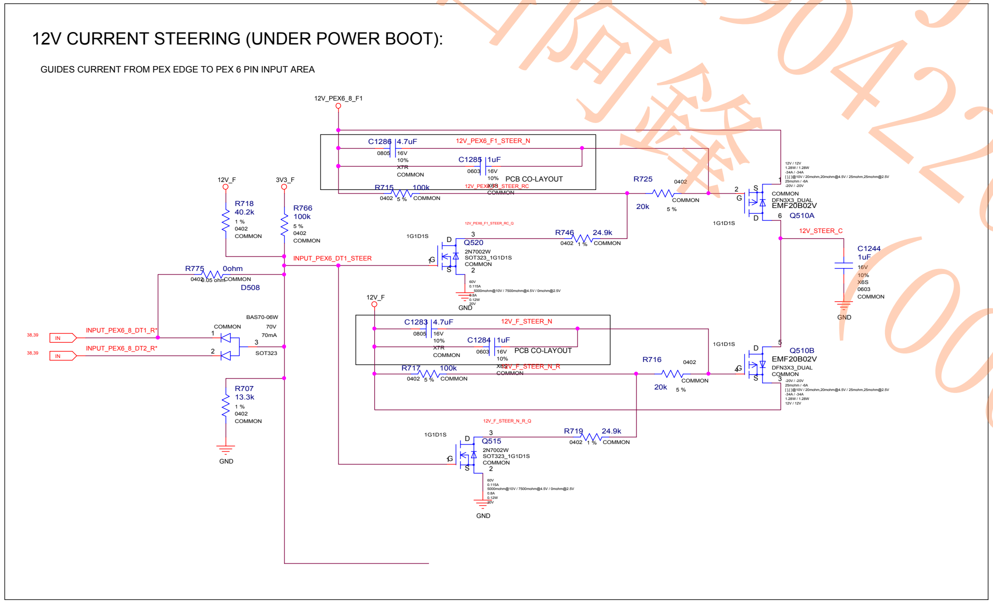


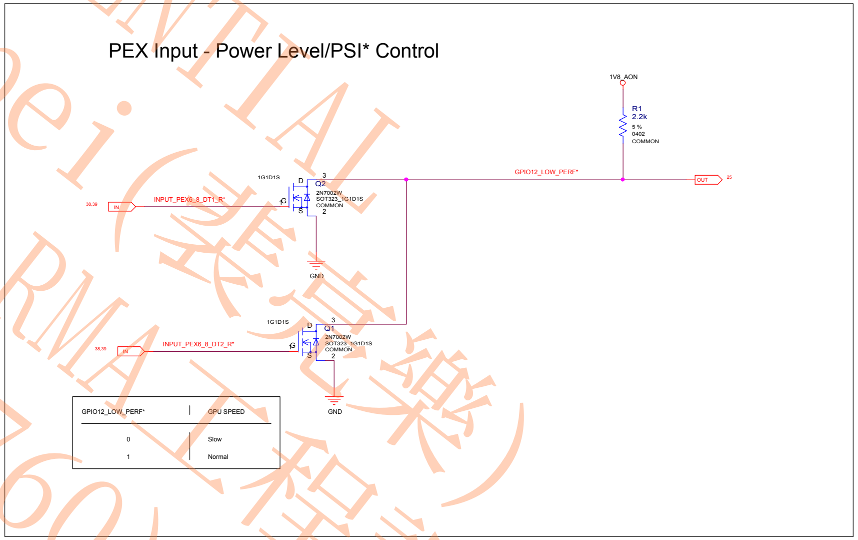
MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page38: PS: Inputs, Filtering, and Monitoring	1.0







GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

Page40: BUCKBOOST

MICRO-STAR INT'L CO.,LTD			
MS-V379			
Size: Custom	Document Description: Page40: BUCKBOOST		Rev: 1.0
Date: Monday, January 14, 2019		Sheet 40 of 53	

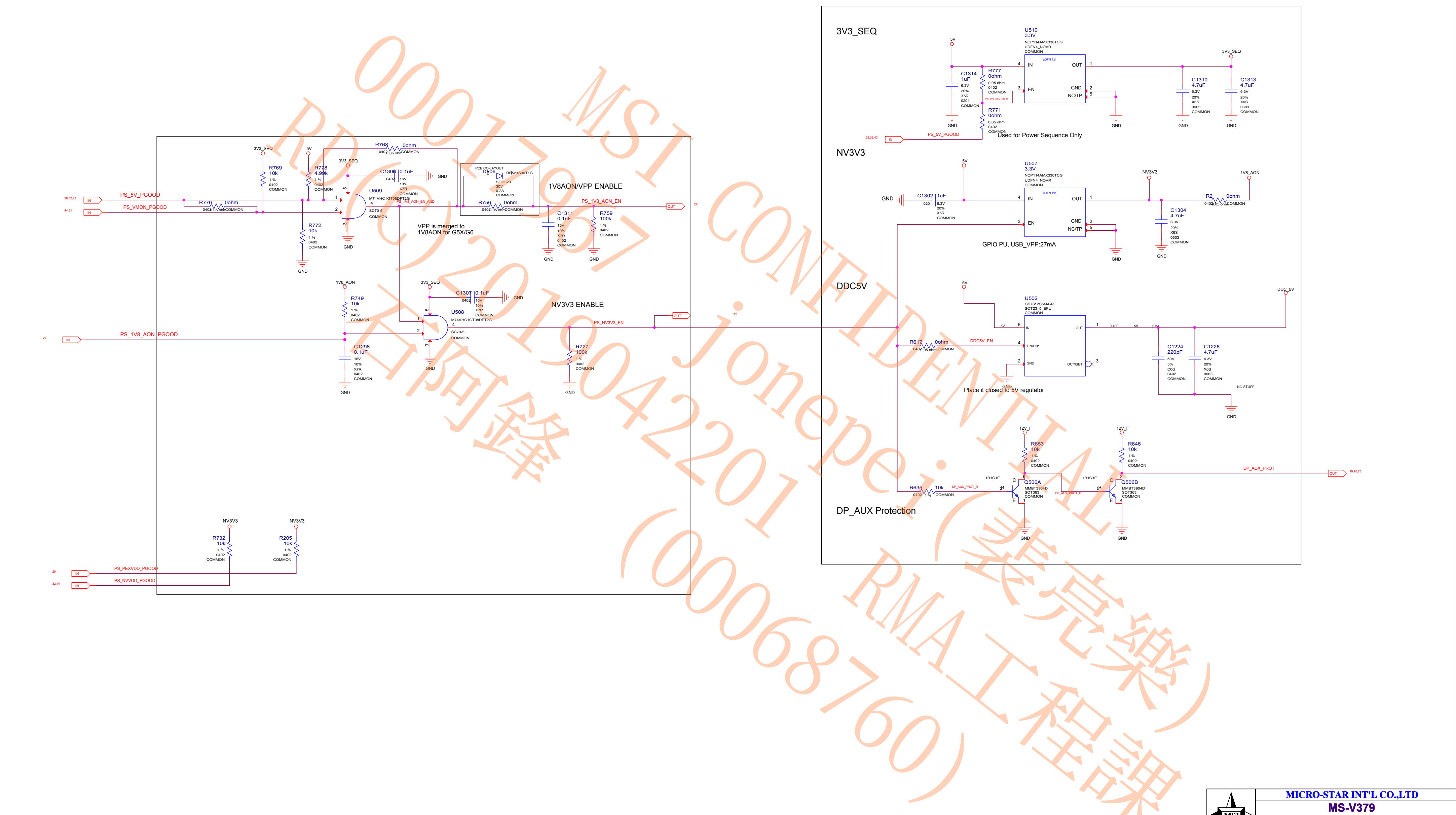
Page41: PPC

MICRO-STAR INT'L CO.,LTD			
MS-V379			
Size: Custom	Document Description: Page41: PPC		Rev: 1.0
Date: Monday, January 14, 2019		Sheet 41 of 53	

Page42: 12V & 3V3_A SWITCHER

MSI	MICRO-STAR INT'L CO.,LTD		
	MS-V379		
Size: Custom	Document Description: Page42: 12V & 3V3_A SWITCHER		Rev: 1.0
Date: Monday, January 14, 2019	Sheet 42 of 53		

Page43: SEQ:5V,1V8,NV3V3 ENABLE



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

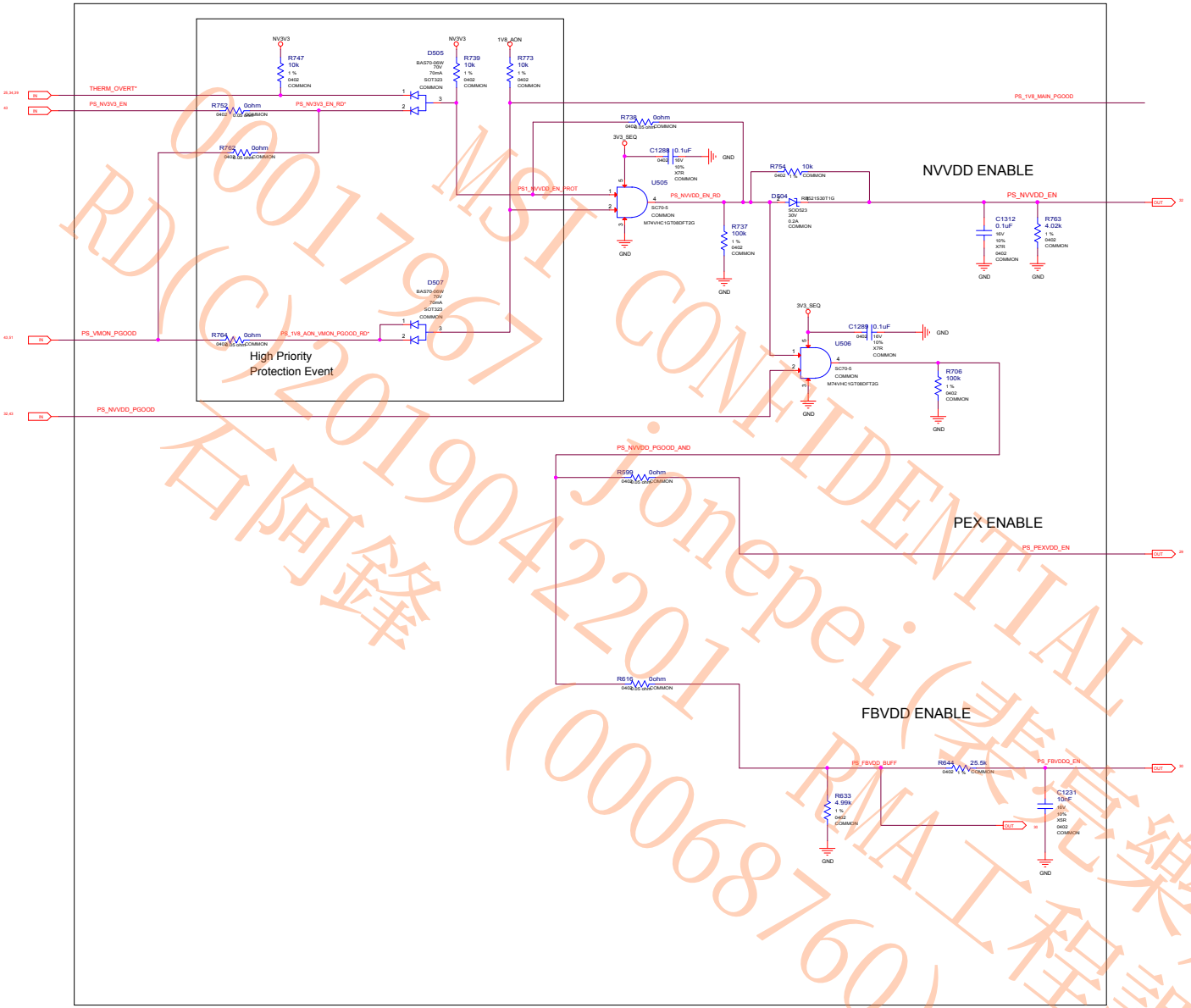
MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page43: SEQ:5V,1V8,NV3V3 ENABLE	1.0

Date: Tuesday, January 15, 2019 Sheet 43 of 53

Page44: SEQ:NV,PEX,FB ENABLE



MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page44: SEQ:NV,PEX,FB ENABLE	1.0

Date: Tuesday, January 15, 2019 | Sheet 44 of 53

Page45: SEQUENCE:Voltage Monitor

MICRO-STAR INT'L CO.,LTD			
MS-V379			
Size: Custom	Document Description: Page45: SEQUENCE:Voltage Monitor		Rev: 1.0
Date: Monday, January 14, 2019	Sheet 45 of 53		

Page46: SEQUENCE:Discharge

MICRO-STAR INT'L CO.,LTD			
MS-V379			
Size: Custom	Document Description: Page46: SEQUENCE:Discharge		Rev: 1.0
Date: Monday, January 14, 2019	Sheet 46 of 53		

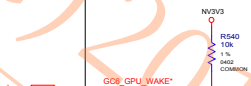
Page47: SEQUENCE:MISC

PEX_CLKREQ*

PU ON GPU SIDE

NC ON GOLD FINGER SIDE

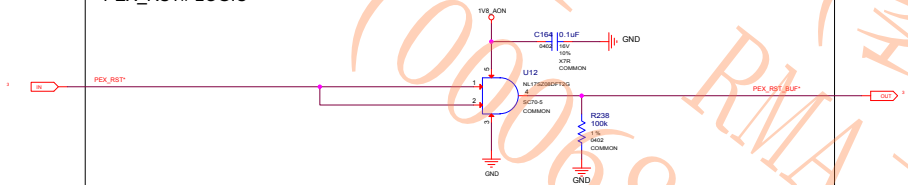
GPU_WAKE*



PU ON GPU SIDE

NC ON GOLD FINGER SIDE

PEX_RST# LOGIC



MICRO-STAR INT'L CO.,LTD		
MS-V379		
Size: Custom	Document Description: Page47: SEQUENCE:MISC	Rev: 1.0
Date: Tuesday, January 15, 2019	Sheet 47 of 53	

Page48: LOGO LED

MICRO-STAR INT'L CO.,LTD			
MS-V379			
Size: Custom	Document Description: Page48: LOGO LED		Rev: 1.0
Date: Monday, January 14, 2019		Sheet 48 of 53	

Page49: LED DRIVER & Boost

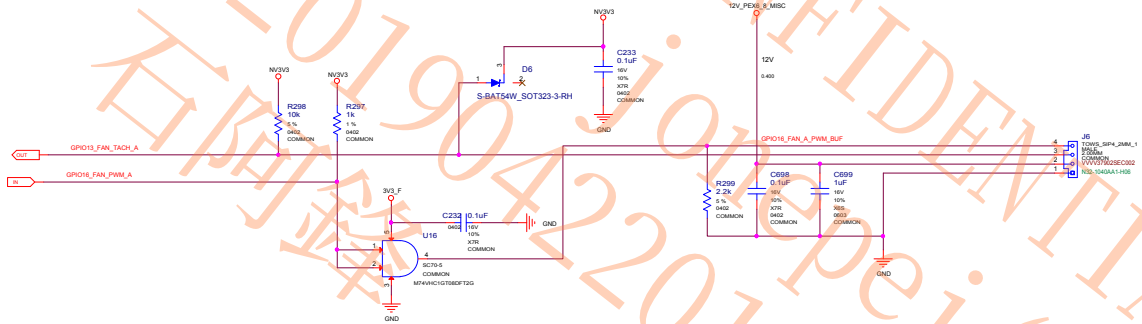
MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	Page49: LED DRIVER & Boost	1.0

Date: Monday, January 14, 2019 Sheet 49 of 53

Page50: FAN

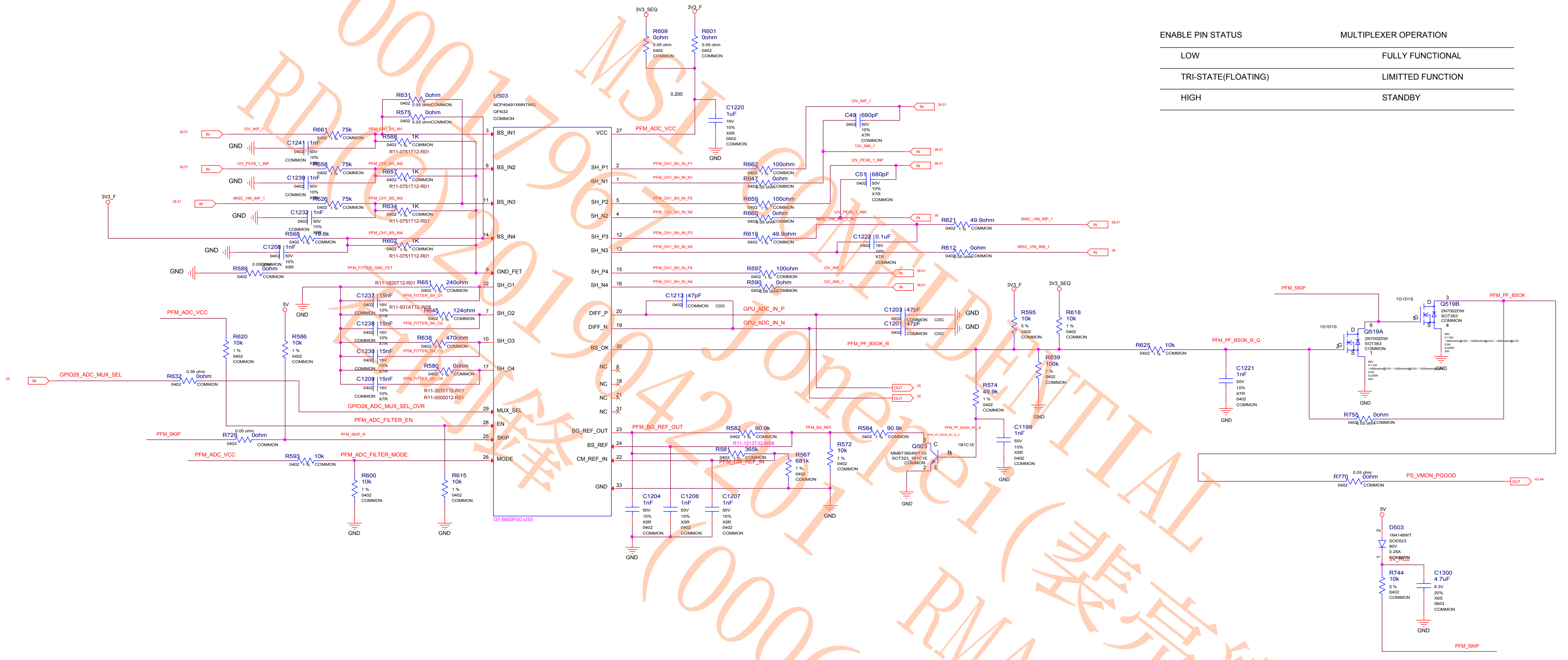


MICRO-STAR INT'L CO.,LTD			
MS-V379			
Size: Custom	Document Description: Page50: FAN		Rev: 1.0
Date: Tuesday, January 15, 2019		Sheet 50 of 53	

Page51: PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY

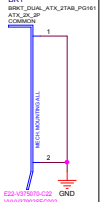


MICRO-STAR INT'L CO.,LTD
MS-V379
Size: Custom | Document Description: Page51: PWR SENSE | Rev 1.0
Date: Tuesday, January 15, 2019 | Sheet 51 of 53

Page52: MECH

Bracket:

BK1
BRKT_DUAL_ATX_2TAB_PG161
ATX_2K_2F
COMMON



E22-V379079-C20
VVVV379025EC002

FAN:

FAN1
STIFFNER
NO PINS
VVVV379025EC002
E32-0406580-A87

BACK STIFFENER:

BS1
STIFFNER
NO PINS
VVVV379025EC002
E99-0000179-G93

MOSFET Heatsink:

HS1
STIFFNER
NO PINS
VVVV379025EC002
E31-0506180-A87

DUST COVER:

PCIE1
STIFFNER
NO PINS
VVVV379025EC002
E24-V330020-P09

for PTA ERP:

HDMICOVER1
STIFFNER
NO PINS
XXXV379025EC002
E24-V330030-P09

DPCOVER1
STIFFNER
NO PINS
XXXV379025EC002
E24-V330010-P09

DPCOVER2
STIFFNER
NO PINS
XXXV379025EC002
E24-V330010-P09

DPCOVER3
STIFFNER
NO PINS
XXXV379025EC002
E24-V330010-P09

Bracket Screw:

BKTSCREW1
SCREW
VVVV379025EC002
E41-1304010-H75

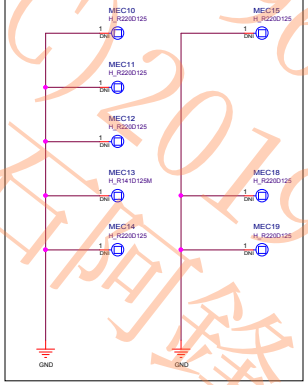
BKTSCREW2
SCREW
VVVV379025EC002
E41-1304010-H75

DPSCREW1
SCREW
VVVV379025EC002
E43-1203051-P65

DPSCREW2
SCREW
VVVV379025EC002
E43-1203051-P65

DPSCREW3
SCREW
VVVV379025EC002
E43-1203051-P65

Mechanical Holes Symbol:



BOARD STIFFENER
4 connected mounting pins
MEC501
GPU_STIFFENER_PG161
4PIN
COMMON
GND

J18
impedence
L4_D_0.088MM/0.1MM 80 OHM +/-10%

J17
X_PIN1*2
L4_S_0.116MM/45 OHM +/-10%

J19
impedence
L3_D_0.083MM/0.121MM 85 OHM +/-10%

J16
X_PIN1*2
L3_S_0.089MM/50 OHM +/-10%

FM1 FM2 FM3 FM4
FM5 FM6 FM7 FM8
OPT
F_PAD_X

PCB
PCB
109-GN982-00A
COMMON
VVVV379025EC002
P06-0V37910-E48

HDMI_FEE
HDMI
HDMI_FEE
COMMON
VVVV379025EC002
Y01-RHDM003-000

MICRO-STAR INT'L CO.,LTD
MS-V379

Size	Document Description	Rev
Custom	Page52: MECH	1.0

Date: Tuesday, January 15, 2019 Sheet 52 of 53

Page53: PTC

MICRO-STAR INT'L CO.,LTD			
MS-V379			
Size: Custom	Document Description: Page53: PTC		Rev: 1.0
Date: Monday, January 14, 2019		Sheet 53 of 53	