電子類元件 零件承認書文件 CHECK LIST

零件廠商： ON Semiconductor **零件名稱：PWM NCP5901BMNTBG ON**

零件 Part Number：NCP5901BMNTBG

項次	文件項目	YES	NO	Page
	Data Sheet 檢核項目			
1	DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**)	V		4-13
2	零件 Making 文字面說明	V		14
3	零件 Part Number 說明	V		15
4	零件 Qualification Test Report	V		16-19
5	料件包裝方式及包裝 Label 之零件 Part number 說明	V		20-30
6	UL Safety Report (If Request)		V	
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間,焊接/過爐次數與曲線圖)。**註 3**	V		31-32
8	零件樣品 20PCS(Chipset 等高單價，至少 1PCS)	V		
9	**主動電子零件承認基本調查表。註 4**	V		2
10	以上資料電子檔爲 PDF 檔，且是同 1 個 File			
	GPMS 綠色產品管理系統-物料管制文件檢核清單			
物料管制文件 1	GPMS 綠色產品管理系統：零件照片			
物料管制文件 2	GPMS 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 5**			
物料管制文件 3	GPMS 綠色產品管理系統：零件承認樣品送樣單			
物料管制文件 4	GPMS 綠色產品管理系統：Data Sheet			
	GPMS 綠色產品管理系統-MCD 表格			
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)			
	其他文件 (僅適用電阻、電容類之系列元件)			
附件 1	危害物質測試報告 Test Report of Hazardous Substances。**註 6**			
附件 2	元件調查表 Component Composition Table			

※ 1. Page 欄：請填入該文件於承認書中之頁碼

※ 2. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷爲雷射或油墨等

※ 3. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)

※ **4. 主動電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G***

※ 5. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”

※ 6. 危害物質測試報告 Test Report of Hazardous Substances：泛指爲具有 ISO/IEC 17025 國際認證之實驗室資格單位

所出具之測試報告

主動電子零件承認基本調查表

一、晶圓廠						
項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包	持有股份
1	ON Semiconductor	USA	Confidential	Confidential	Self	100%
2						
3						

二、封裝廠					
項次	工廠名稱	生產產地	投產比率(%)	自有/外包	持有股份
1	Confidential	Confidential	Confidential	Confidential	Confidential
2					
3					

三、產能				
項次	產能廠區	良率 (%)	總產能(月/PCS)	可供技嘉產能(月/PCS)
1	Confidential	Confidential	Confidential	Confidential
2				
3				
四、交貨 Lead Time				

五、料件銷售客戶/比率			
項次	客戶	出貨量/比率	導入時間
1			
2			
3			
4			

※ 1. 晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動) 時，請主動通知技嘉研發管理與 CE 單位，並更新文件 2. 以上資訊欄位若有不足，可自行增加行數

承　認　書

APPROVAL SHEET

客　戶　名　稱　　技嘉科技股份有限公司

品　　名　**NCP5901BMNTBG**
(10TA1-605901-20R)

廠　　商　**Yosun Industrial Corp.** 友尚股份有限公司

台北總公司	上海代表處	蘇州代表處
2-2659-8168	21-5836-5838	51-2809-4171

業務工程師　　張孝安

承　認　日　期	廠　商　簽　章	客　戶　承　認　章
	友尚股份有限公司 台灣區總代理 TEL:26598168 台北市內湖區堤頂大道二段480號9樓	

NCP5901B

VR12 Compatible Synchronous Buck MOSFET Drivers

The NCP5901B is a high performance dual MOSFET gate driver optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. It can drive up to 3 nF load with a 25 ns propagation delay and 20 ns transition time.

Adaptive anti−cross−conduction and power saving operation circuit can provide a low switching loss and high efficiency solution for notebook and desktop systems. Bidirectional EN pin can provide a fault signal to controller when the gate driver fault detect under OVP, UVLO occur. Also, an under−voltage lockout function guarantees the outputs are low when supply voltage is low.

Features

- Faster Rise and Fall Times
- Adaptive Anti−Cross−Conduction Circuit
- Integrated Bootstrap Diode
- Pre OV function
- ZCD Detect
- Floating Top Driver Accommodates Boost Voltages of up to 35 V
- Output Disable Control Turns Off Both MOSFETs
- Under−voltage Lockout
- Power Saving Operation Under Light Load Conditions
- Direct Interface to NCP6151 and Other Compatible PWM Controllers
- Thermally Enhanced Package
- These are Pb−Free Devices

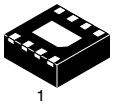
Typical Applications

- Power Solutions for Desktop Systems

ON Semiconductor®

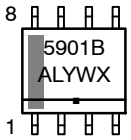
http://onsemi.com

SOIC−8 NB
D SUFFIX
CASE 751

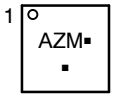


DFN8
MN SUFFIX
CASE 506AA

MARKING DIAGRAMS



5901B = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

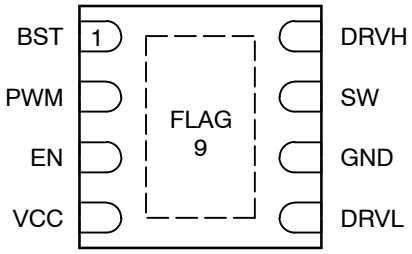


AZ = Specific Device Code
M = Date Code
▪ = Pb−Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NCP5901BMNTBG	DFN8 (Pb−Free)	3000 / Tape & Reel
NCP5901BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



(Top View)

Figure 1. Pin Diagram

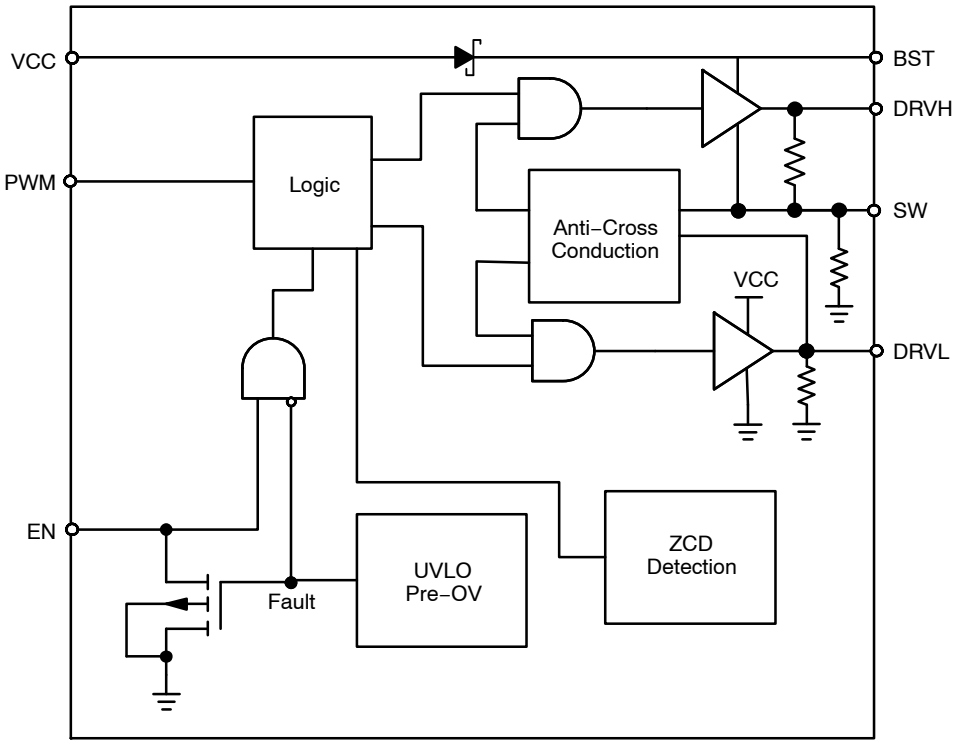


Figure 2. Block Diagram

Table 1. Pin Descriptions

Pin No.	Symbol	Description
1	BST	Floating bootstrap supply pin for high side gate driver. Connect the bootstrap capacitor between this pin and the SW pin.
2	PWM	Control input. The PWM signal has three distinctive states: Low = Low Side FET Enabled, Mid = Diode Emulation Enabled, High = High Side FET Enabled.
3	EN	Logic input. A logic high to enable the part and a logic low to disable the part.
4	VCC	Power supply input. Connect a bypass capacitor (0.1 μF) from this pin to ground.
5	DRVL	Low side gate drive output. Connect to the gate of low side MOSFET.
6	GND	Bias and reference ground. All signals are referenced to this node (QFN Flag).
7	SW	Switch node. Connect this pin to the source of the high side MOSFET and drain of the low side MOSFET.
8	DRVH	High side gate drive output. Connect to the gate of high side MOSFET.
9	FLAG	Thermal flag. There is no electrical connection to the IC. Connect to ground plane.

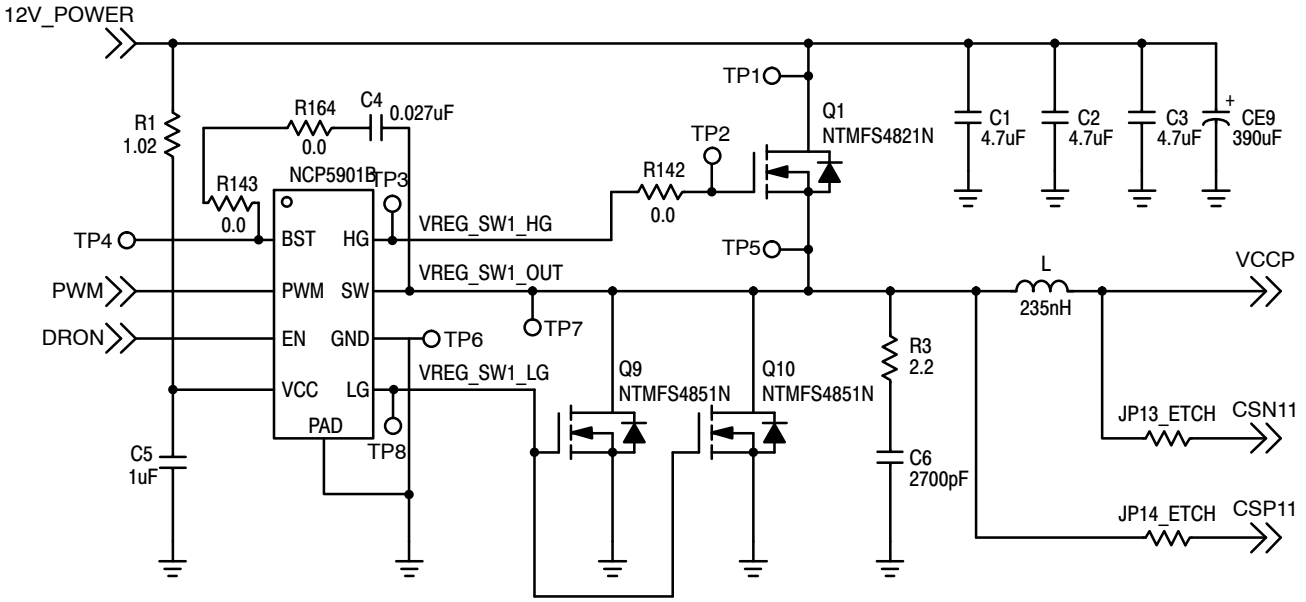


Figure 3. Application Circuit

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}
VCC	Main Supply Voltage Input	15 V	−0.3 V
BST	Bootstrap Supply Voltage	35 V wrt/ GND 40 V ≤ 50 ns wrt/ GND 15 V wrt/ SW	−0.3 V wrt/SW
SW	Switching Node (Bootstrap Supply Return)	35 V 40 V ≤ 50 ns	−5 V −10 V (200 ns)
DRVH	High Side Driver Output	BST+0.3 V	−0.3 V wrt/SW −2 V (<200 ns) wrt/SW
DRVL	Low Side Driver Output	VCC+0.3 V	−0.3 V DC −5 V (<200 ns)
PWM	DRVH and DRVL Control Input	6.5 V	−0.3 V
EN	Enable Pin	6.5 V	−0.3 V
GND	Ground	0 V	0 V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. THERMAL INFORMATION (All signals referenced to AGND unless noted otherwise)

Symbol	Parameter		Value	Unit
$R_{\theta JA}$	Thermal Characteristic	SOIC Package (Note 1) DFN Package (Note 1)	123 74	°C/W
T_J	Operating Junction Temperature Range (Note 2)		0 to 150	°C
T_A	Operating Ambient Temperature Range		−10 to +125	°C
T_{STG}	Maximum Storage Temperature Range		−55 to +150	°C
MSL	Moisture Sensitivity Level	SOIC Package DFN Package	1 1	

***** The maximum package power dissipation must be observed.
1. I in^2 Cu, 1 oz thickness.
2. Operation at −40°C to −10°C guaranteed by design, not production tested.

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −10°C < T_A < +125°C; 4.5 V < V_{CC} < 13.2 V, 4.5 V < BST−SWN < 13.2 V, 4.5 V < BST < 30 V, 0 V < SWN < 21 V)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
SUPPLY VOLTAGE					
VCC Operation Voltage		4.5		13.2	V
Power ON Reset Threshold			2.75	3.2	V
UNDERVOLTAGE LOCKOUT					
VCC Start Threshold		3.8	4.35	4.5	V
VCC UVLO Hysteresis		150	200	250	mV
Output Overvoltage Trip Threshold at Startup	Power Startup time, VCC > POR	2.1	2.25	2.4	V
SUPPLY CURRENT					
Normal Mode	Icc + Ibst, EN = 5 V, PWM = OSC, Fsw = 100 KHz, Cload = 3 nF for DRVH, 3 nF for DRVL		12.2		mA
Standby Current	Icc + Ibst, EN = GND		0.5	1.9	mA
Standby Current	I_{CC} + I_{BST}, EN = HIGH, PWM = LOW, No loading on DRVH & DRVL		2.1		mA
Standby Current	I_{CC} + I_{BST}, EN = HIGH, PWM = HIGH, No loading on DRVH & DRVL		2.2		mA
BOOTSTRAP DIODE					
Forward Voltage	V_{CC} = 12 V, forward bias current = 2 mA	0.1	0.4	0.6	V
PWM INPUT					
PWM Input High		3.4			V
PWM Mid−State		1.3		2.7	V
PWM Input Low				0.7	V
ZCD Blanking Timer			250		ns
HIGH SIDE DRIVER (VCC = 12 V)					
Output Impedance, Sourcing Current	VBST − VSW = 12 V		2.0	3.5	Ω
Output Impedance, Sinking Current	VBST − VSW = 12 V		1.0	2.0	Ω
DRVH Rise Time tr_{DRVH}	V_{VCC} = 12 V, 3 nF load, VBST−VSW = 12 V		16	30	ns
DRVH Fall Time tf_{DRVH}	V_{VCC} = 12 V, 3 nF load, VBST−VSW = 12 V		11	25	ns
DRVH Turn−Off Propagation Delay $tpdh_{DRVH}$	C_{LOAD} = 3 nF	8.0		30	ns
DRVH Turn−On Propagation Delay $tpdl_{DRVH}$	C_{LOAD} = 3 nF			30	ns
SW Pull Down Resistance	SW to PGND		45		kΩ
DRVH Pull Down Resistance	DRVH to SW, BST−SW = 0 V		45		kΩ
HIGH SIDE DRIVER (VCC = 5 V)					
Output Impedance, Sourcing Current	VBST − VSW = 5 V		4.5		Ω
Output Impedance, Sinking Current	VBST − VSW = 5 V		2.9		Ω
DRVH Rise Time tr_{DRVH}	V_{VCC} = 5 V, 3 nF load, VBST − VSW = 5 V		30		ns
DRVH Fall Time tf_{DRVH}	V_{VCC} = 5 V, 3 nF load, VBST − VSW = 5 V		27		ns
DRVH Turn−Off Propagation Delay $tpdh_{DRVH}$	C_{LOAD} = 3 nF		20		ns
DRVH Turn−On Propagation Delay $tpdl_{DRVH}$	C_{LOAD} = 3 nF		27		ns
SW Pull Down Resistance	SW to PGND		45		kΩ

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −10°C < T_A < +125°C; 4.5 V < V_{CC} < 13.2 V, 4.5 V < BST−SWN < 13.2 V, 4.5 V < BST < 30 V, 0 V < SWN < 21 V)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
HIGH SIDE DRIVER (VCC = 5 V)					
DRVH Pull Down Resistance	DRVH to SW, BST−SW = 0 V		45		kΩ
LOW SIDE DRIVER (VCC = 12 V)					
Output Impedance, Sourcing Current			2.0	3.5	Ω
Output Impedance, Sinking Current			0.8	1.8	Ω
DRVL Rise Time tr_{DRVL}	C_{LOAD} = 3 nF		16	35	ns
DRVL Fall Time tf_{DRVL}	C_{LOAD} = 3 nF		11	20	ns
DRVL Turn−Off Propagation Delay $tpdl_{DRVL}$	C_{LOAD} = 3 nF			35	ns
DRVL Turn−On Propagation Delay $tpdh_{DRVL}$	C_{LOAD} = 3 nF	8.0		30	ns
DRVL Pull Down Resistance	DRVL to PGND, VCC = PGND		45		kΩ
LOW SIDE DRIVER (VCC = 5 V)					
Output Impedance, Sourcing Current			4.5		Ω
Output Impedance, Sinking Current			2.4		Ω
DRVL Rise Time tr_{DRVL}	C_{LOAD} = 3 nF		30		ns
DRVL Fall Time tf_{DRVL}	C_{LOAD} = 3 nF		22		ns
DRVL Turn−Off Propagation Delay $tpdl_{DRVL}$	C_{LOAD} = 3 nF		27		ns
DRVL Turn−On Propagation Delay $tpdh_{DRVL}$	C_{LOAD} = 3 nF		12		ns
DRVL Pull Down Resistance	DRVL to PGND, VCC = PGND		45		kΩ
EN INPUT					
Input Voltage High		2.0			V
Input Voltage Low				1.0	V
Hysteresis			500		mV
Normal Mode Bias Current		−1		1	μA
Enable Pin Sink Current		4		30	mA
Propagation Delay Time			20	40	ns
SW Node					
SW Node Leakage Current				20	μA
Zero Cross Detection Threshold Voltage	SW to −20 mV, ramp slowly until BG goes off (Start in DCM mode) (Note 3)		−6		mV

Table 5. DECODER TRUTH TABLE

PWM INPUT	ZCD	DRVL	DRVH
PWM High	ZCD Reset	Low	High
PWM Mid	Positive current through the inductor	High	Low
PWM Mid	Zero current through the inductor	Low	Low
PWM Low	ZCD Reset	High	Low

3. Guaranteed by design; not production tested.

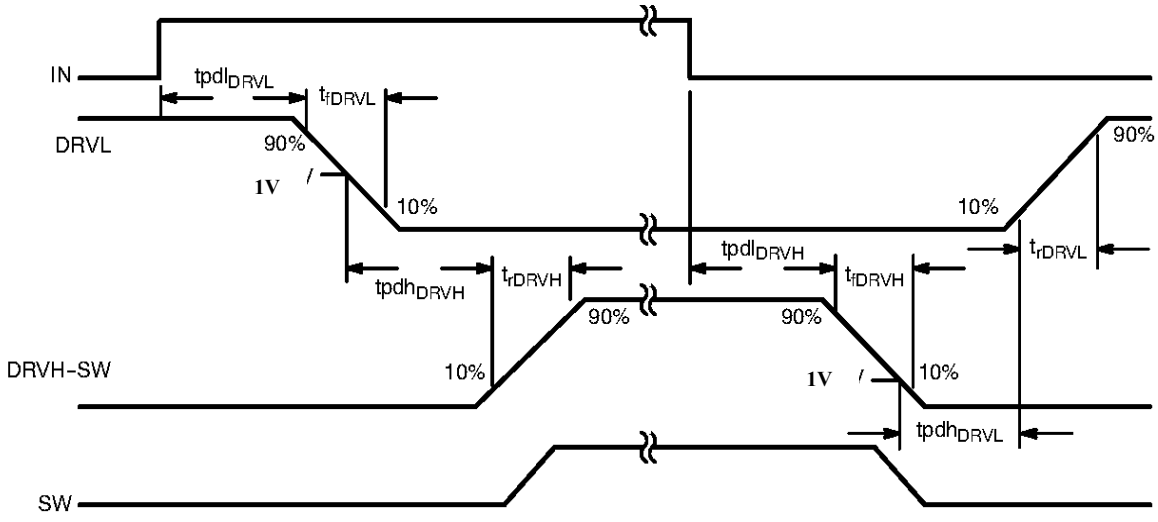


Figure 4.

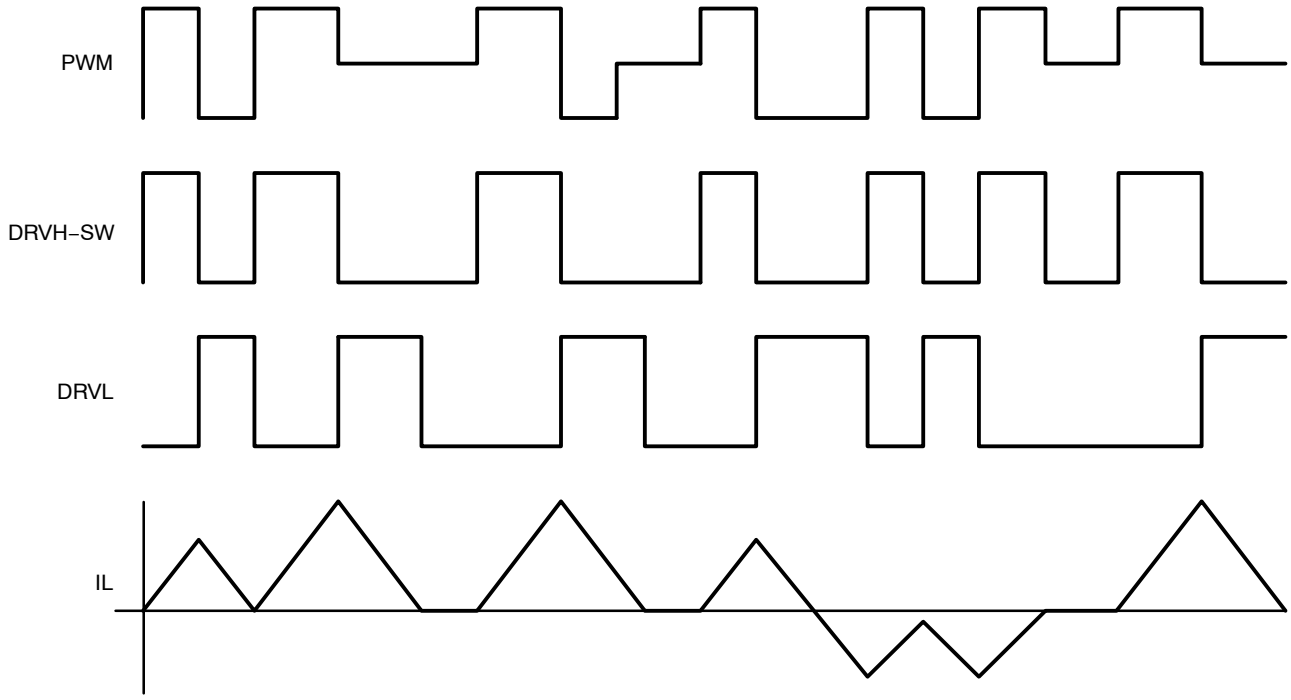


Figure 5. Timing Diagram

APPLICATIONS INFORMATION

The NCP5901B gate driver is a single phase MOSFET driver designed for driving N−channel MOSFETs in a synchronous buck converter topology. The NCP5901B is designed to work with ON Semiconductor's NCP6131 multi−phase controller. This gate driver is optimized for desktop applications.

Undervoltage Lockout

The DRVH and DRVL are held low until V_{CC} reaches 4.5 V during startup. The PWM signals will control the gate status when V_{CC} threshold is exceeded. If V_{CC} decreases to 250 mV below the threshold, the output gate will be forced low until input voltage V_{CC} rises above the startup threshold.

Power−On Reset

Power−On Reset feature is used to protect a gate driver avoid abnormal status driving the startup condition. When the initial soft−start voltage is higher than 2.75 V, the gate driver will monitor the switching node SW pin. If SW pin high than 2.25 V, bottom gate will be force to high for discharge the output capacitor. The fault mode will be latch and EN pin will force to be low, unless the driver is recycle. When input voltage is higher than 4.5 V, and EN goes high, the gate driver will normal operation, top gate driver DRVH and bottom gate driver will follow the PWM signal decode to a status.

Bi−directional EN Signal

Fault modes such as Power−On Reset and Undervoltage Lockout will de−assert the EN pin, which will pull down the DRON pin of controller as well. Thus the controller will be shut down consequently.

PWM Input and Zero Cross Detect (ZCD)

The PWM input, along with EN and ZCD, control the state of DRVH and DRVL.

When PWM is set high, DRVH will be set high after the adaptive non−overlap delay. When PWM is set low, DRVL will be set high after the adaptive non−overlap delay.

When the PWM is set to the mid state, DRVH will be set low, and after the adaptive non−overlap delay, DRVL will be set high. DRVL remains high during the ZCD blanking time. When the timer is expired, the SW pin will be monitored for zero cross detection. After the detection, the DRVL will be set low.

Adaptive Nonoverlap

The nonoverlap dead time control is used to avoid the shoot through damage the power MOSFETs. When the PWM signal pull high, DRVL will go low after a propagation delay, the controller will monitors the switching node (SWN) pin voltage and the gate voltage of the MOSFET to know the status of the MOSFET. When the low side MOSFET status is off an internal timer will delay turn on of the high−side MOSFET. When the PWM pull low, gate DRVH will go low after the propagation delay (tpd $_{DRVH}$).

The time to turn off the high side MOSFET is depending on the total gate charge of the high−side MOSFET. A timer will be triggered once the high side MOSFET is turn off to delay the turn on the low−side MOSFET.

Low−Side Driver Timeout

In normal operation, the DRVH signal tracks the PWM signal and turns off the Q1 high−side switch with a few 10 ns delay ($t_{pdlDRVH}$) following the falling edge of the input signal. When Q1is turned off, DRVL is allowed to go high, Q2 turns on, and the SW node voltage collapses to zero. But in a fault condition such as a high−side Q1 switch drain−source short circuit, the SW node cannot fall to zero, even when DRVH goes low. This driver has a timer circuit to address this scenario. Every time the PWM goes low, a DRVL on−time delay timer is triggered.

If the SW node voltage does not trigger a low−side turn−on, the DRVL on−time delay circuit does it instead, when it times out with $t_{SW(TO)}$ delay. If Q1 is still turned on, that is, its drain is shorted to the source, Q2 turns on and creates a direct short circuit across the VDCIN voltage rail. The crowbar action causes the fuse in the VDCIN current path to open. The opening of the fuse saves the load (CPU) from potential damage that the high−side switch short circuit could have caused.

Layout Guidelines

Layout for DC−DC converter is very important. The bootstrap and V_{CC} bypass capacitors should be placed as close as to the driver IC.

Connect GND pin to local ground plane. The ground plane can provide a good return path for gate drives and reduce the ground noise. The thermal slug should be tied to the ground plane for good heat dissipation. To minimize the ground loop for low side MOSFET, the driver GND pin should be close to the low−side MOSFET source pin. The gate drive trace should be routed to minimize the length, the minimum width is 20 mils.

Gate Driver Power Loss Calculation

The gate driver power loss consists of the gate drive loss and quiescent power loss.

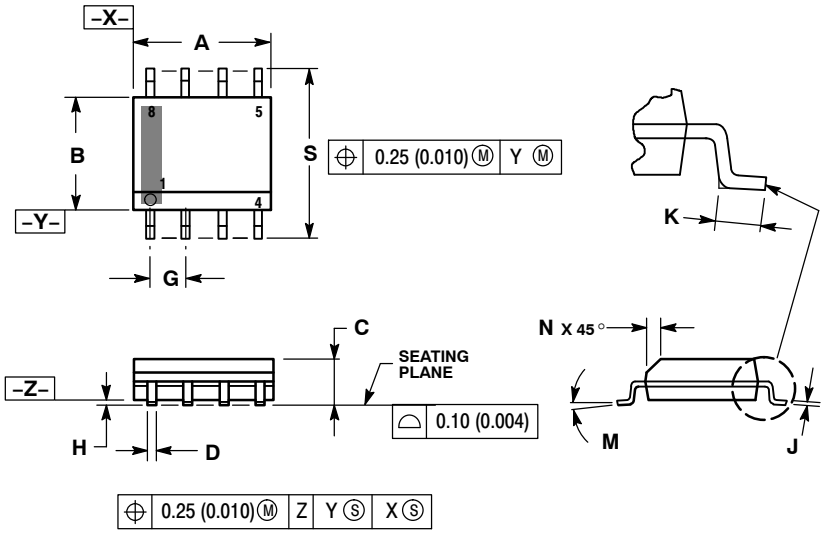
The equation below can be used to calculate the power dissipation of the gate driver. Where Q_{GMF} is the total gate charge for each main MOSFET and Q_{GSF} is the total gate charge for each synchronous MOSFET.

$$P_{DRV} = [\frac{f_{SW}}{2 \times n} \times (n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF}) + I_{CC}] \times V_{CC}$$

Also shown is the standby dissipation factor ($I_{CC} \cdot V_{CC}$) of the driver.

PACKAGE DIMENSIONS

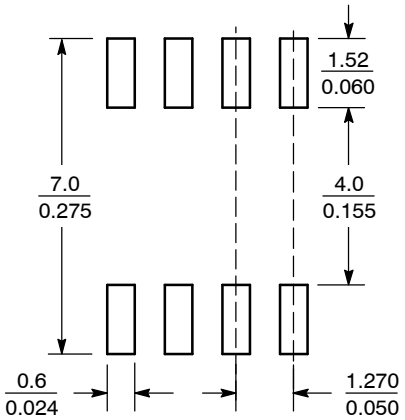
SOIC−8 NB
CASE 751−07
ISSUE AJ



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

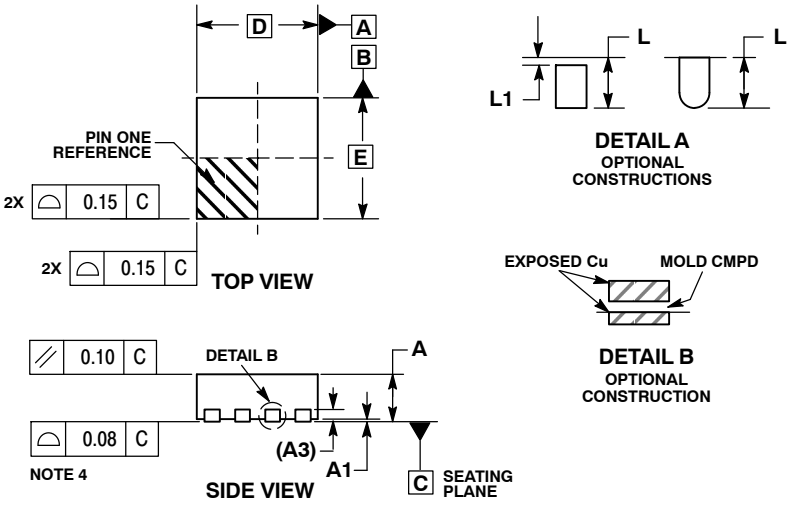


SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

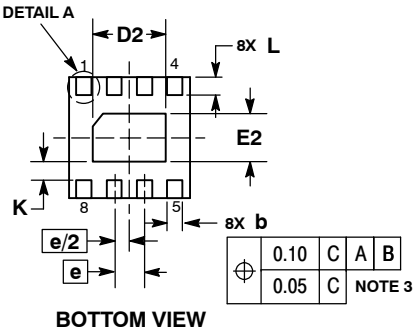
PACKAGE DIMENSIONS

DFN8 2x2
CASE 506AA−01
ISSUE E

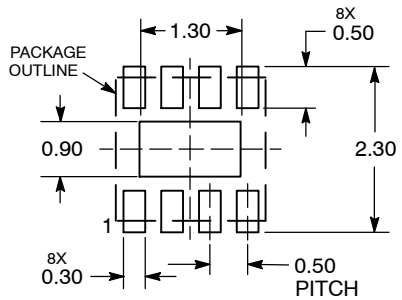


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	−−−	0.10



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

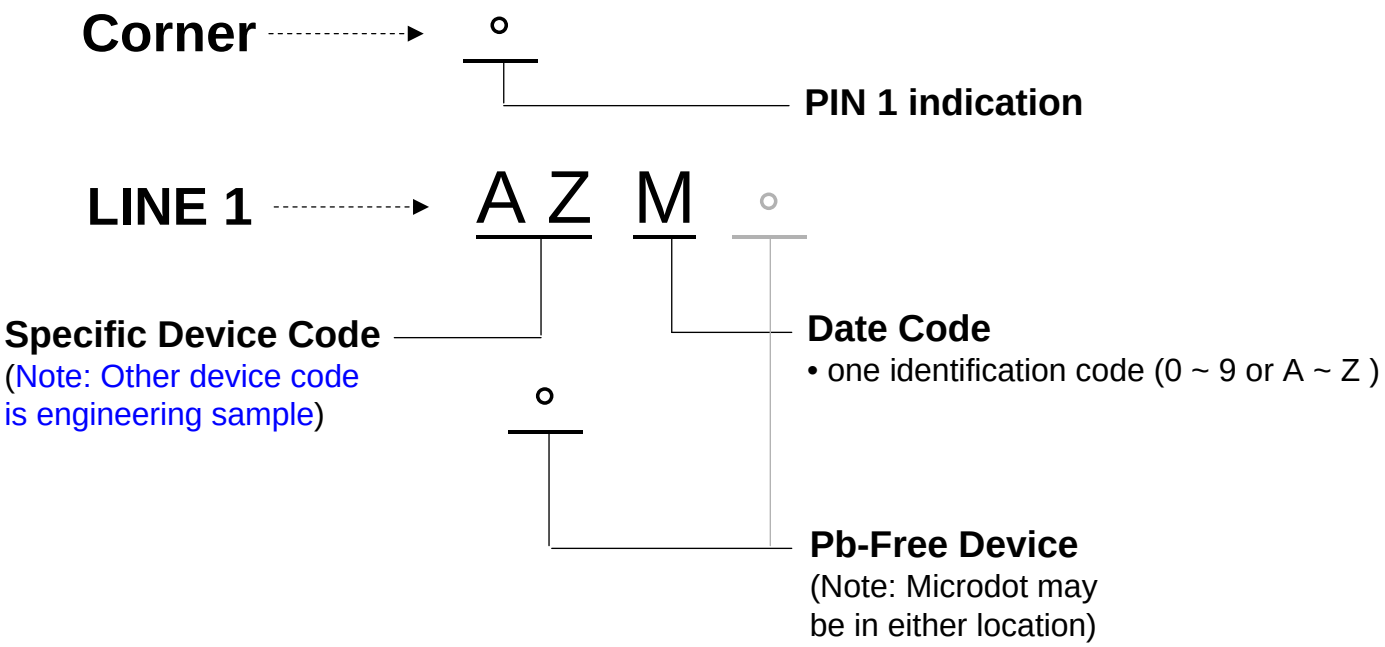
Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your loca
Sales Representative

Package information

Product	Status	Pb-free	Description	Package		MSL*	Container	
				Type	Case Outline		Type	Qty.
NCP5901BDR2G	Active	Pb	VR12 Compatible Synchronous Buck MOSFET Drivers	SOIC-8	751-07	1	Tape and Reel	2500
NCP5901BMNTBG	Active	Pb	VR12 Compatible Synchronous Buck MOSFET Drivers	DFN-8	506AA	1	Tape and Reel	3000

Marking Description



Naming Convention

N C P 5901B MN TB G

Product Class
- N = Standard
- S = Special/Custom
- X = Pilot Production
- P = Engineering Prototypes

Product Group
- C = Analog Integrated Circuits

Product Family/Performance Index
- L = Lighting
- N = Advanced Interface
- P = Power Management
- S = Signal
- T = Thermal Management
- V = Vehicular (Automotive)

Stem Number
Assigned by Marketing
(2 to 6 alpha/ numeric digits)

Temp Range/Output Type Designator Assigned by Marketing
Ex:
- A = Enhanced
- B = Extended

Package Designator
- C = CHIP
- D = SOIC Narrow Body
- DA = TSSOP with 0.5 mm lead pitch
- DB = TSSOP with 0.65 mm lead pitch
- DM = Micro
- DS = D2PAK
- DT = DPAK
- DW = SOIC Wide Body
- F = PowerFLEX
- FB = TQFP
- FC = bump Flip−Chip
- FN = PLCC
- FT = LQFT
- H = Flip−Chip
- MN = QFN/DFN/LLGA >0.8 mm thick
- MT = QFN/DFN/LLGA 0.6 to 0.8 mm thick
- MU = QFN/DFN/LLGA <0.6 mm thick

Tape/Reel Designator
- TB = Tape & Reel

Pb−Free Designator
- G = Lead−Free

NCP5901/01B, SOIC-8 NB and 2x2x1mm DFN-8 New Product Reliability Report

Date: 29 Oct 2010 **PCN: N/A** **Rev. O**

Executive Summary:

This report summarizes the result of the reliability tests performed on the NCP5901/01B, which is using the ONBCD25 wafer process and housing in SOIC-8 NB and 2x2x1mm DFN-8, 0.5P packages at OSPI and SBN respectively. Based on the reliability test results as documented in this report, the NCP5901/01B is qualified for consumer grade and rated at MSL 1@260ºC in both packages.

Introduction:

The NCP5901/01B is a high performance Dual MOSFET Gate Driver for driving N-channel MOSFETs in a synchronous buck converter topology. Internal bootstrap diode is included in NCP5901B. The ONBCD25 is a qualified wafer technology and the SOIC-8 NB & 2x2x0.9mm DFN-8 are qualified packages at OSPI and SBN respectively. With the generic die and package reliability data is available, this device will be qualified with 1 wafer lot sample for HTOL test, in addition with ESD, LU and Tri-temp. Electrical Characterization. As the die to flag (DTF) ratio in SOIC-8 NB package is just 35.8%, additional package reliability test is required to verify the changes.

Device Description:

Device	NCP5901/01BDR2G NCP5901/01BMNTBG	**Wafer Fab Site**	Gresham	Oregon, USA
Package	SOIC-8 NB DFN-8, 2x2x1mm, 0.5P	**Assembly Site**	OSPI SBN	Carmona, Philippines Seremban, Malaysia
MSL Level	MSL 1 @260°C	**Final Test Site**	OSPI SBN	Carmona, Philippines Seremban, Malaysia
Wafer Technology	ONBCD25, 3LM			
Final Lead Finish	Matte Sn	**Package Code**	0081 (SOIC-8 NB) 0380 (2x2 DFN-8)	

Related Reliability Qualification Data and Reports:

- QR-2009-11 – Gresham ONBCD25 Wafer process Qualification Reliability Report
- QR-2009-20 – NCP3420/5359A Gresham ONBCD25 in SBN & UTL DFN Reliability Report
- C100524-011 – NCP5901 SOIC-8NB SAT Report
- 10-NCP5901-E13 ESD/LU Report

Qualification Results and Analysis:

#	Test	Name	Test Conditions	End Point Req's	Test Results	Lot A (rej/ ss)	Lot B (rej/ ss)	Lot C (rej/ ss)	Remark
NCP5901 – SOIC-8NB & 2x2 DFN-8									
1	Prep	Sample preparation and initial part testing	various	---	Initial Electrical	Done	Done	Done	
2	HTOL	High Temp Op Life	TA = 125°C	c = 0, Room	**504hrs**	0/80			**SOIC-8 NB**
					1008 hrs	0/80			
3	PC	Moisture Preconditioning	MSL 1 @ 260°C	c = 0, Room	After PC	0/240	0/160	0/160	
4	AC-PC	Precond. Autoclave	TA = 121°C, RH = 100%, PSIG = 15	c = 0, Room	**96 hrs**	0/80			**SOIC-8 NB**
5	TC-PC	Precond. Temp Cycle	-65/+150°C air to air	c = 0, Room	250 cycs	0/80	0/80	0/80	**SOIC-8 NB**
					500 cycs	0/80	0/80	0/80	
6	TC-PC	Precond. Temp Cycle	-65/+150°C air to air	c = 0, Room	250 cycs	0/80	0/80	0/80	**2x2 DFN-8**
					500 cycs	0/80	0/80	0/80	
7	ED	Electrical Distribution	Per ON Datasheet Critical Parameter	Room, Hot, Cold **Cpk ≥ 1.67**	Results	Pass	Pass	Pass	**SOIC-8 NB**
NCP5901B									
1	HTOL	High Temp Op Life	TA = 125°C	c = 0, Room	**168hrs**	0/80			**SOIC-8 NB** Wafer Lot# GAL47926.7 Assembly Lot#PH1029104A
2	ESD	Electro-static Discharge	Human Body Model (HBM)	Room	Results	+/-500V			Class 1B
			Machine Model (MM)	Room	Results	+/-50V			Class A
3	LU	Latch-up	JESD 78	Room	**+/-100mA**	0/6			LU test on EN pin is limited to I-test@+/- 10mA.[1]
4	ED	Electrical Distribution	Per ON Datasheet Critical Parameter	Room, Hot, Cold **Cpk ≥ 1.67**	Results	Pass			

Table 1: Reliability Evaluation Results for NCP5901/01B, maskset Y07M, in SOIC-8 NB and 2x2 DFN-8, 0.5P package Qualification Points in BOLD

Note : #1 The NCP5901 EN pin is driven on our NCP6151 controller's DRON logic output pin. That pin has less than 5mA output current capability due to its internal design (2kΩ resistance in series with 5V output). Therefore, the LU I-test@100mA will damage the EN pin open drain NMOS. Per designer's comment, the NCP5901 EN pin is designed to handle about 13mA of current. Bench evaluation shown 70mA was required to damage the EN pin with identical failure mode as LU I-test@100mA.

Conclusion:

Based on the reliability test results documented in this report, the NCP5901/01B, maskset Y07M, in SOIC-8 NB and 2x2x1mm DFN-8, 0.5P package, meets or exceeds ON Semiconductor's requirements for product reliability, as set forth in "Product Reliability Qualification Process" specification 12MSB17722C. This device is qualified for consumer grade and rated at MSL 1@260ºC.

Written By : Nicky Siu, Reliability Engineer — 29 OCT 2010

Approved By : Stephen Ng, Quality Manager — Stephen Ng, 29 Oct 2010

Revision	Description of Revision	Who	Date
O	Initial release	Nicky Siu	29 Oct 2010

Appendix:

Test Descriptions and Conditions:

HTOL Op Life

HIGH TEMPERATURE OPERATING LIFE JESD22 A108
The purpose of this test is to evaluate the bulk stability of the die and to generate defects resulting from manufacturing aberrations that are manifested as time and stress-dependent failures.
Test Conditions: TA = 125 or 150°C
Common Failure Modes: Parametric shifts and catastrophic
Common Failure Mechanisms: Foreign material, crack die, bulk die, metallization, wire and die bond defects.

PC MSL 1 PC

MOISTURE LEVEL PRECONDITIONING J-Std-020B JA113
The tests are performed to simulate the board mounting process where parts are subjected to a high temperature for a short duration. These tests detect mold compound delamination from the die and leadframe. The failure mechanisms are corrosion, fractured wire bonds and passivation cracks.
Test Conditions: 24hrs Bake@125+5/-0°C + 168hrs 85/85 +3X IR Reflow@260 °C +1X Flux Immersion + DI Rinse (JEDEC)

AC-PC Autoclave-PC

AUTOCLAVE+MOISTURE LEVEL PRECONDITIONING JESD22 A102
Autoclave is an environmental test which measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Autoclave is an accelerated and destructive test.
Test Conditions: Ta=121 °C, RH=100%, P=15 psig
Common Failure Modes: Parametric shifts, high leakage and / or catastrophic
Common Failure Mechanisms: Die corrosion or contaminants such as foreign material on or within the package material. Poor package sealing.

TC-PC Temperature Cycle-PC

TEMPERATURE CYCLING + MOISTURE LEVEL PRECOND. JESD22 A104
The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperatures and transitions between temperature extremes. This testing will also expose excessive thermal mismatch between materials.
Test Conditions: Ta= -65 °C to 150 °C, air to air
Common Failure Modes: Parametric shifts and catastrophic
Common Failure Mechanisms: Wire bond, cracked or lifted die and package failure.

ESD ESD

ELECTROSTATIC DISCHARGE JESD22 A114, A115
The purpose of this test is to measure the relative ability of the part to withstand accidental electrostatic discharge. Both the Human Body Model and the Machine Model are used in testing. Devices are divided into groups and tested at specified increments across the ESD test range (per JEDEC). Data is recorded and devices are rated at the highest level at which they passed. If devices show no failures at the max increment, they are rated as being greater than (>) that voltage. If devices fail at some lower increment, they are rated as being equal (=) to that voltage.

LU Latch-up

Latch-up JESD78A
A state in which a low-impedance path, resulting from an overstress that triggers a parasitic thyristor structure, persists after removal or cessation of the triggering condition. Latch-up testing is extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures. Latch-up is not related to a specific mechanism but is an electrical failure characteristic that occurs when a device is subjected to this test method.

ED Electrical Distribution

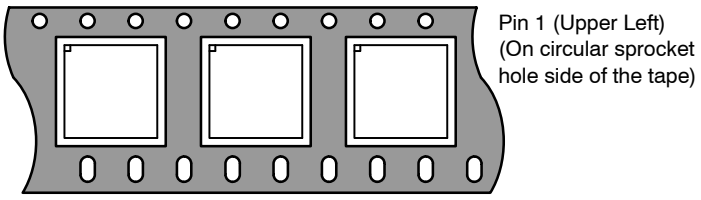
ELECTRICAL DISTRIBUTION (PARAMETRIC VERIFICATION)
This is performed to insure that all units meet or exceed the electrical requirements per datasheet.

Product Orientation (continued)

Direction of Feed

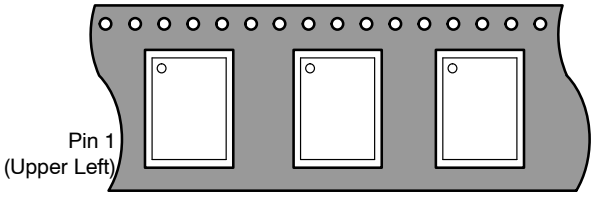
Leadless Packages

Figure 33. FCBGA (BGA)



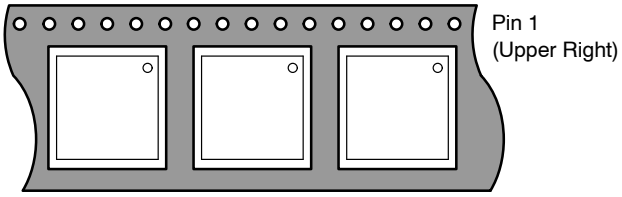
TA, TW

Figure 34. DFN/QFN



TA, TW

Figure 35. DFN/QFN (LPCC)



TB, TX

Package	Pre Jan 2007	Post Jan 2007
DFN / QFN Square (LPCC)	T1	TB, TX
	T4	TB, TX
	R2	TB, TX
DFN / QFN Rectangular (LPCC)	T1	TA, TW
	R2	TA, TW
DFN / QFN	T2	TA, TW
	R2	TA, TW
FCBGA / BGA	R2	TA, TW

Leadless Package Pin 1 Orientation for Tape and Reel (QFN, DFN, FCBGA, BGA, LPCC)

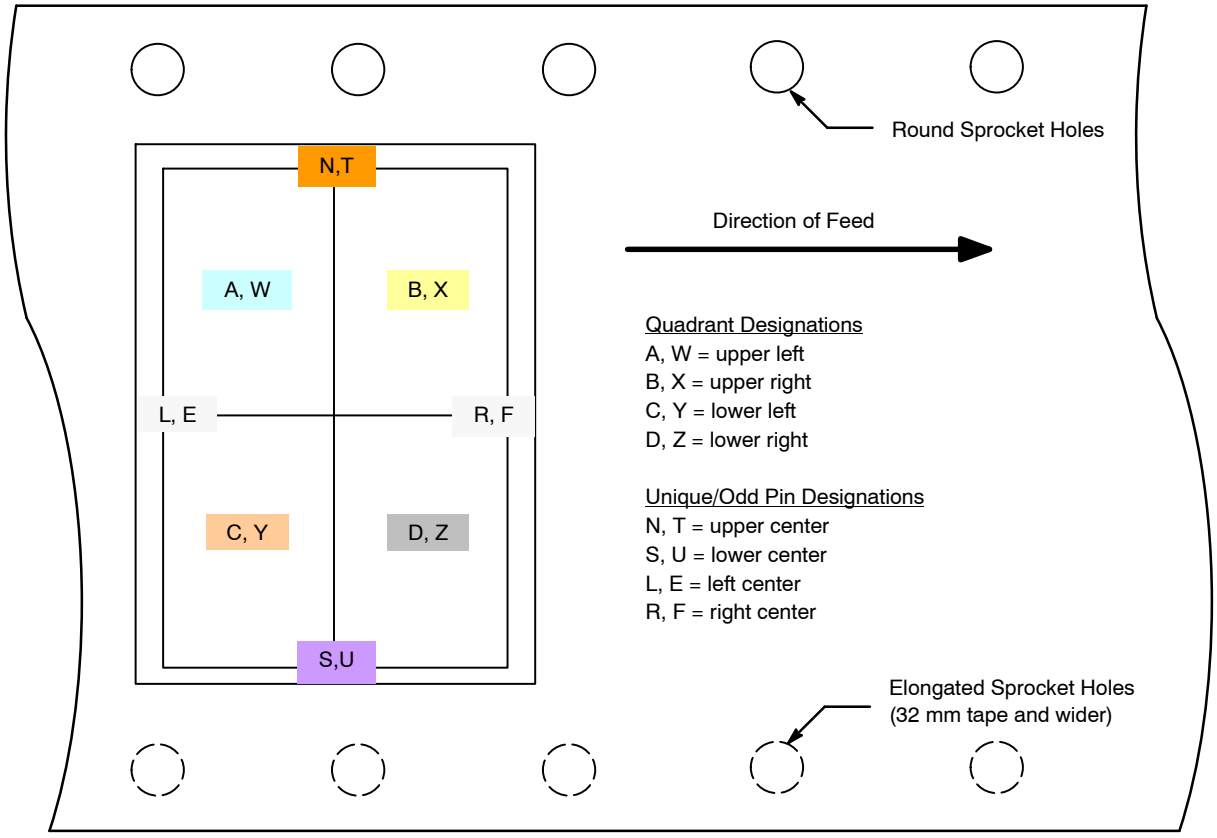
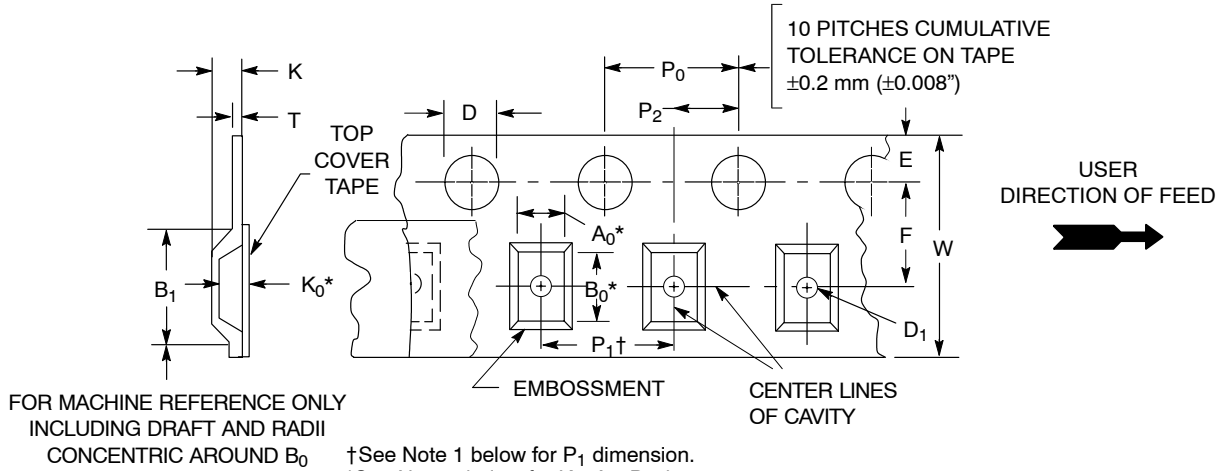


Figure 36. Leadless Package Pin 1 Orientation for Tape and Reel (Effective January 2007)

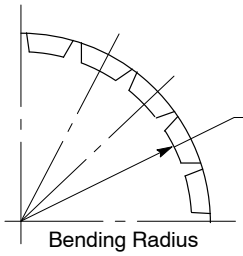
Part Number Suffix				
Shipping Type*	**Pin1 Location**	**Blank or Pb−Free**	**Remark:**	**Reel Size (mm) diameter**
T	A	G	Quadrant 1−upper left	177
T	B	G	Quadrant 2−−upper right	178
T	C	G	Quadrant 3−−lower left	178
T	D	G	Quadrant 4−−lower right	178
T	W	G	Quadrant 1−upper left	330
T	X	G	Quadrant 2−−upper right	330
T	Y	G	Quadrant 3−−lower left	330
T	Z	G	Quadrant 4−−lower right	330
T	N	G	North (upper center)	178
T	S	G	South (lower center)	178
T	T	G	Top (upper center)	330
T	U	G	Under (lower center)	330
T	L	G	Left center	178
T	R	G	Right center	178
T	E	G	Left center	330
T	F	G	Right center	330

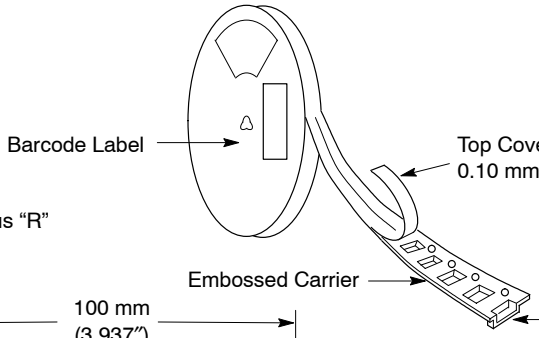
*T = Tape

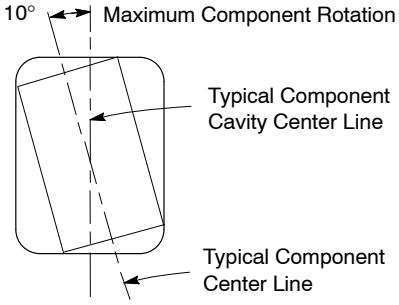
Embossed Tape and Reel Data Carrier Tape Specifications

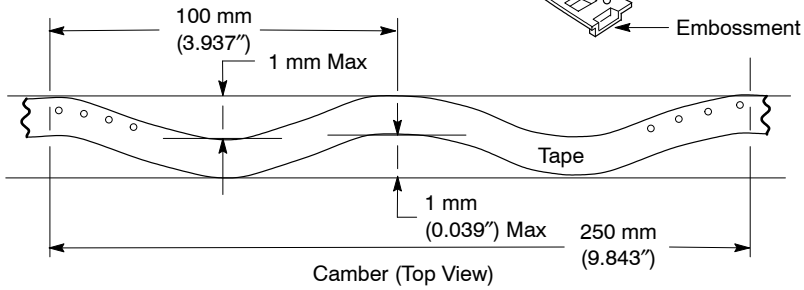


†See Note 1 below for P_1 dimension.
*See Note 2 below for K_0, A_0, B_0 dimensions.









Camber (Top View)
Allowable Camber To Be 1 mm/100 mm Nonaccumulative Over 250 mm

DIMENSIONS

Tape Size (W)	B_1 Max (Note 1)	D	D_1	E	F	K	P_0	P_2	R Min	T Max	W Max
8 mm	4.55 mm (0.179″)	1.5 + 0.1 mm − 0.0 (0.059 + 0.004″ − 0.0)	1.0 Min (0.039″) or 0.5 mm Min (0.020″)	1.75 ± 0.1 mm (0.069 ± 0.004″)	3.5 ± 0.05 mm (0.138 ± 0.002″)	2.4 mm Max (0.094″)	4.0 ± 0.1 mm (0.157 ± 0.004″)	2.0 ± 0.1 mm (0.079 ± 0.002″)	25 mm (0.98″)	0.6 mm (0.024″)	8.3 mm (0.327″)
12 mm	8.2 mm (0.323″)		1.5 mm Min (0.060″)		5.5 ± 0.05 mm (0.217 ± 0.002″)	6.4 mm Max (0.252″)			30 mm (1.18″)		12 ± 0.30 mm (0.470 ± 0.012″)
16 mm	12.1 mm (0.476″)				7.5 ± 0.10 mm (0.295 ± 0.004″)	7.9 mm Max (0.311″)					16.3 mm (0.642″)
24 mm	20.1 mm (0.791)				11.5 ± 0.1 mm (0.453 ± 0.004″)	11.9 mm Max (0.468″)					24.3 mm (0.957″)

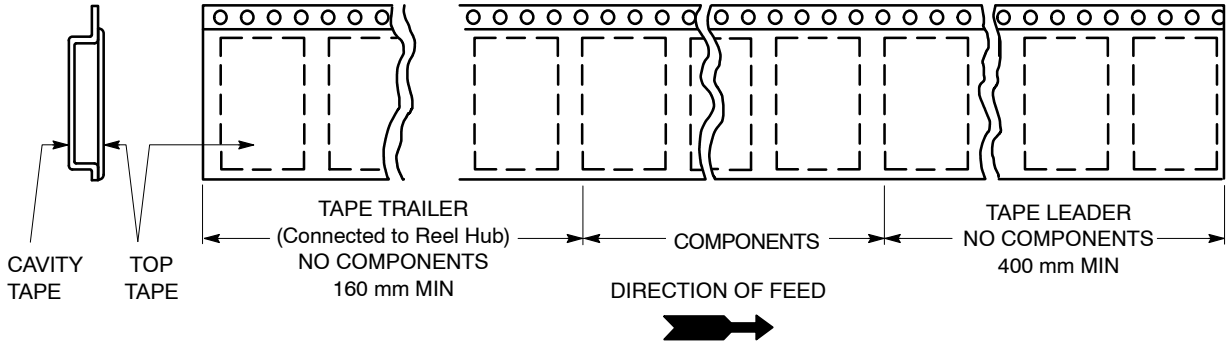
Metric dimensions govern − English are in parentheses for reference only.

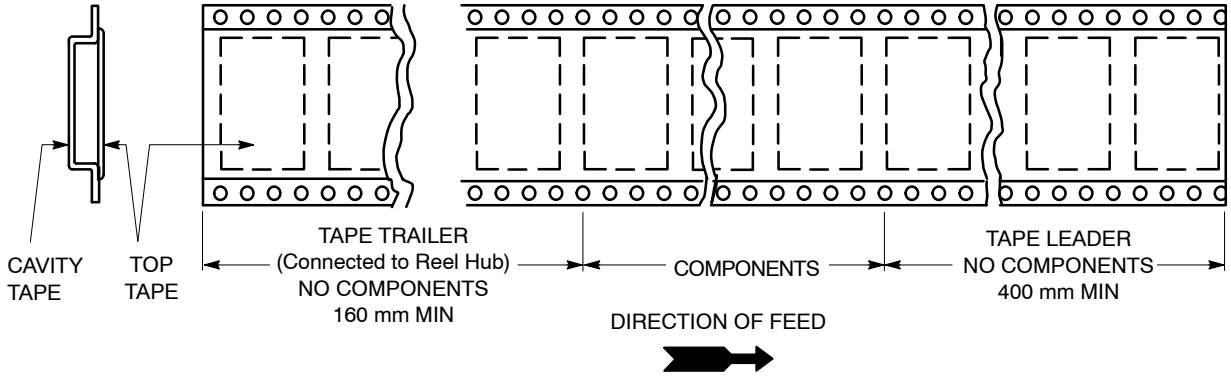
1. Pitch information (dimension P_1) is contained in the embossed tape and reel ordering information beginning on Page 7.
2. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity.

Tape Ends for Finished Goods

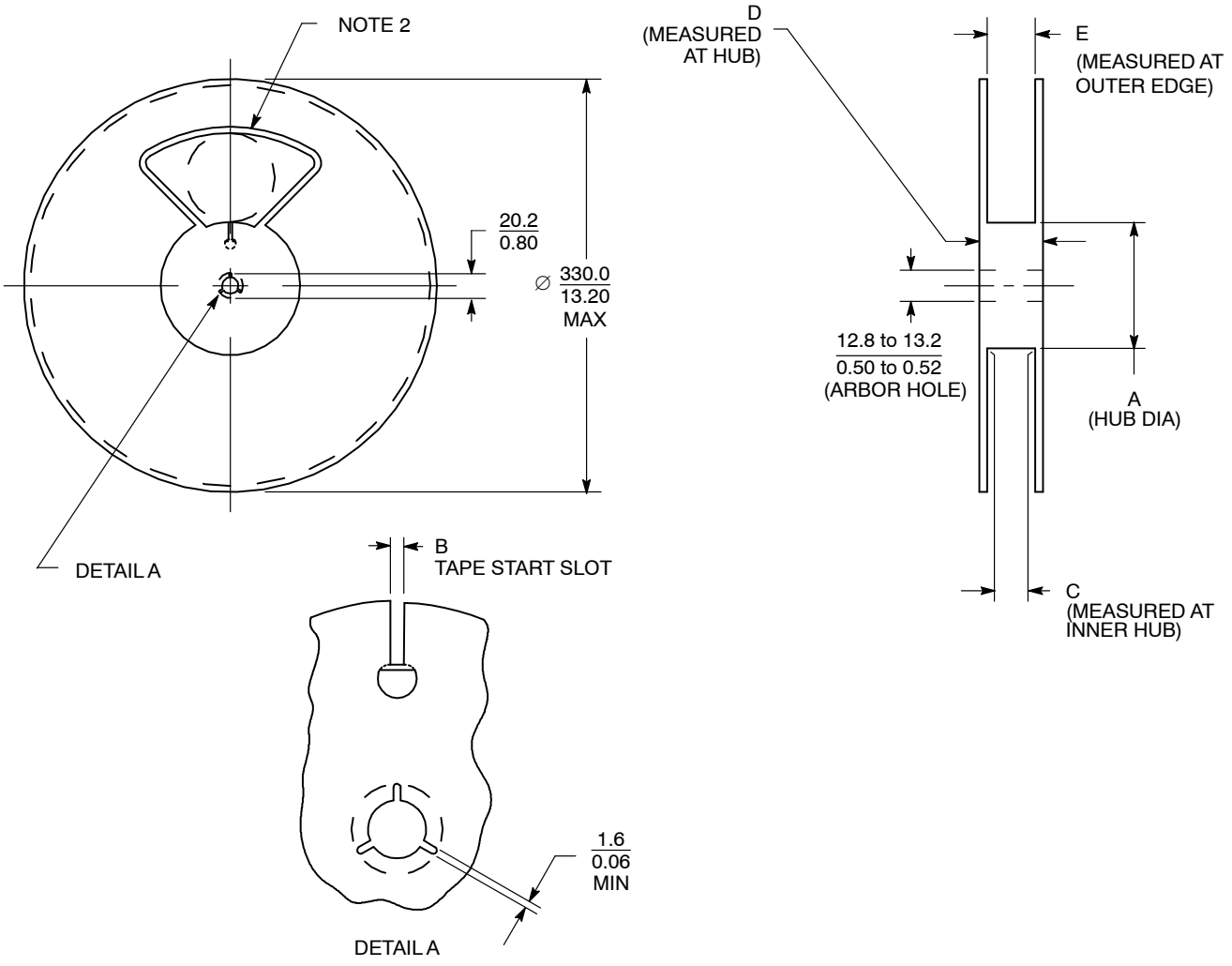
Leader and Trailer

The TRAILER is a minimum of 160 mm in length and it consists of empty cavities with sealed cover tape.
The LEADER is a minimum of 400 mm in length and it consists of empty cavities with sealed cover tape.





Reel Dimensions



Reel Diameter	Tape Size	A mm (inches)		B mm (inches)		C mm (inches)		D	E
		Min	Max	Min	Max	Min	Max	(Max)	(Max)
178.0 (7.01)	16.0 (0.63)		50.0 (1.97)	6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)	178.0 (7.01)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	56.0 (2.20)	150.0 (5.91)		10.0 (0.39)	11.0 (0.43)	56.4 (2.22)	58.4 (2.30)	62.4 (2.46)	59.4 (2.34)
330.0 (12.99)	44.0 (1.73)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	44.4 (1.75)	46.4 (1.83)	62.4 (2.46)	47.4 (1.87)
330.0 (12.99)	32.0 (1.26)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	32.4 (1.28)	34.4 (1.35)	38.4 (1.51)	35.4 (1.39)
330.0 (12.99)	24.0 (0.94)	60.0 (2.36)		9.5 (0.37)	10.5 (0.41)	24.4 (0.96)	26.4 (1.04)	30.4 (1.51)	27.4 (1.08)
330.0 (12.99)	16.0 (0.63)			6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)			4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.01)	12.0 (0.47)	50.0 (1.97)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.47)	10.9 (0.43)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)

Reel Dimensions (continued)

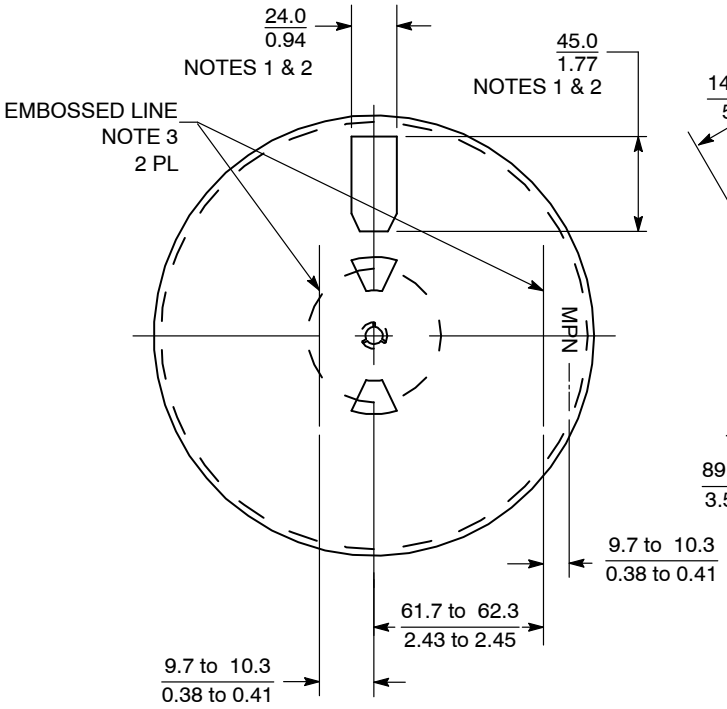


Figure 37. Front View of 178 mm (7.0 in) Reel

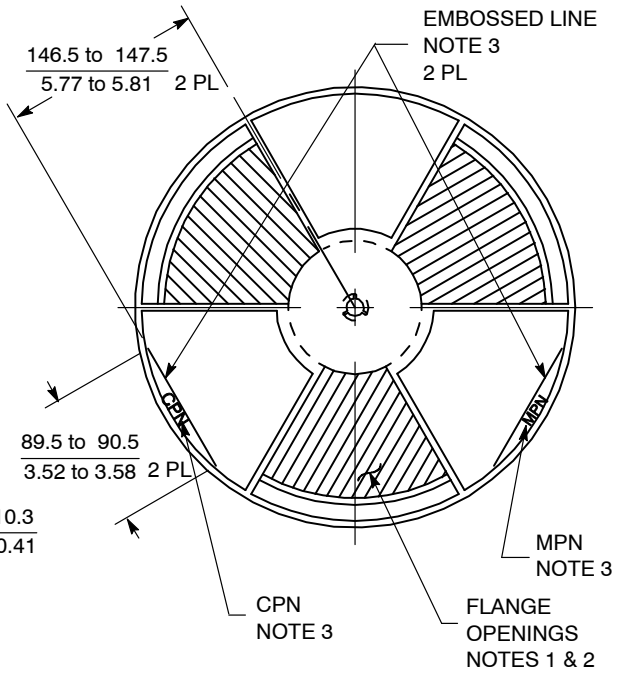


Figure 38. Front View of 330 mm (12.99 in) Reel

NOTES:

1. LABEL PLACEMENT AREA:
   - All reels must have flat area on the front flange of the reel that will fit two 41.3 mm (1.65 in) by 125 mm (4.90 in) ON Semiconductor barcode labels.
   - If there are any flange openings on the front side of the 178 mm (7.00 in) reel they must be designed in locations so that two of the 41.3 mm (1.65 in) ON Semiconductor barcode labels can be applied parallel to each other as in Figure 37.
   - If there are any flange opening on the front flange of the 330 mm (13.0 in) reel they must be designed in locations so that two of the 41.3 mm (1.65 in) by 125 mm (4.90 in) ON Semiconductor barcode labels can be applied parallel to each other as in Figure 38.
2. FLANGE OPENINGS
   - Flange opening on the front and the back of the reel are a supplier option but must meet all of the requirements in Note 1. The preferred size for the 176 mm (7.0 in) reel is shown in Figure 37.
   - The tape loading opening must be as in Detail A.
3. GRAPHICS:
   - The letters MPN and CPN are a option. The size and thickness of the letters are the manufacturer's option and are not to be used for inspection criteria.
   - The embossed lines on the reel are a option. If the lines are used they must be located as in Figure 37 and 38. They must be a minimum 38 mm (1.50 in) long. The thickness is a manufacturer's option and not to be used for inspection criteria.

Reel Labeling

Place the reel on an ESD protective surface so that the round sprocket holes are on the bottom. The direction of travel when unwound should be from the top right quadrant. See illustration below.

REEL WINDING DIRECTION

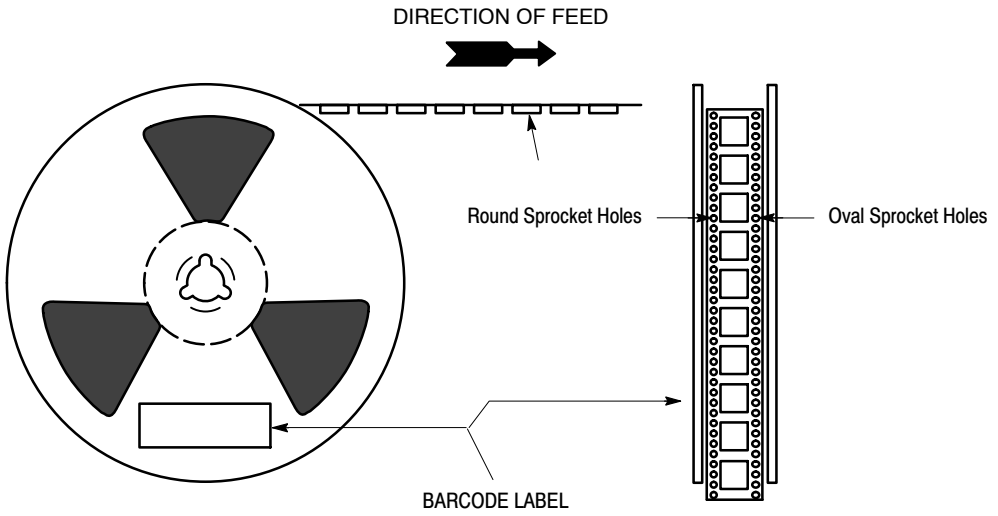


Figure 39. Round and Oval Sprocket Holes Used with 32 mm, 42 mm, 44 mm and 52 mm Tape (holes on both sides)

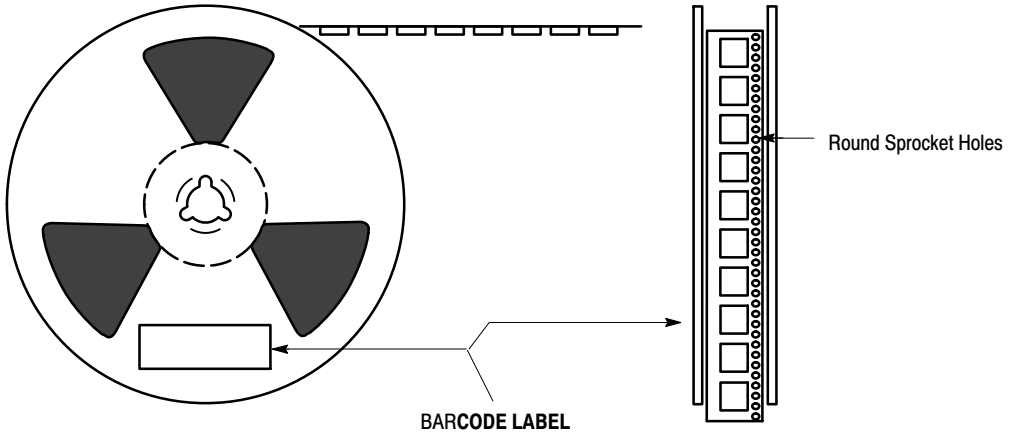
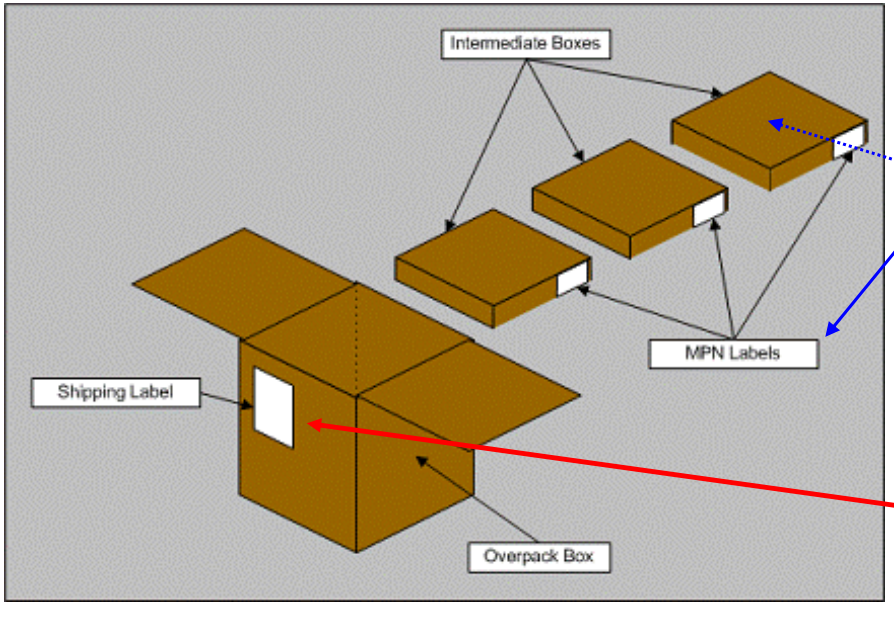


Figure 40. Round Sprocket Holes Used with 8 mm, 12 mm,16 mm and 24 mm Tape (holes on one side only)

Packaging Scheme

Packaging and Graphics

Shipments from ON Semiconductor will follow the company's standard packaging process. The "Overpack" box may contain multiple "Intermediate" boxes of a single product. For each line item on an order that is shipped, there will be at least one Overpack Box [more if the quantity of Intermediate Boxes exceeds the capacity of the overpack box]. Any Overpack Box will contain one and only one part number, but may contain varying lots and date codes based on the content of the Intermediate Boxes.



HF symbols on Reels, Dry bag, Intermediate boxes MPN label.

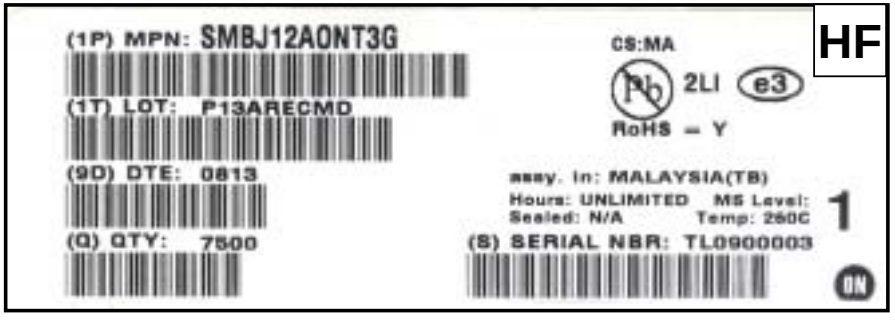
HF symbols on the "Overpack" Box – Shipping labels

MPN Label with halide-free text

Interim short term 'HF' on the labels for Halogen Free products: Reels, dry bag & intermediate box MPN labels.

Sample MPN label printed

Sample MPN label with HF Sticker



Started the rollout of labeling in February and expected the completion for all Halogen free product by end Q2'09 or sooner.

MPN Label with halide-free text

Long Term 'HF' on the labels for Halogen Free products: Reels, dry bag & intermediate box MPN labels automatically printed based on the product attribute. Target auto-print solution to be ready by Q3'09

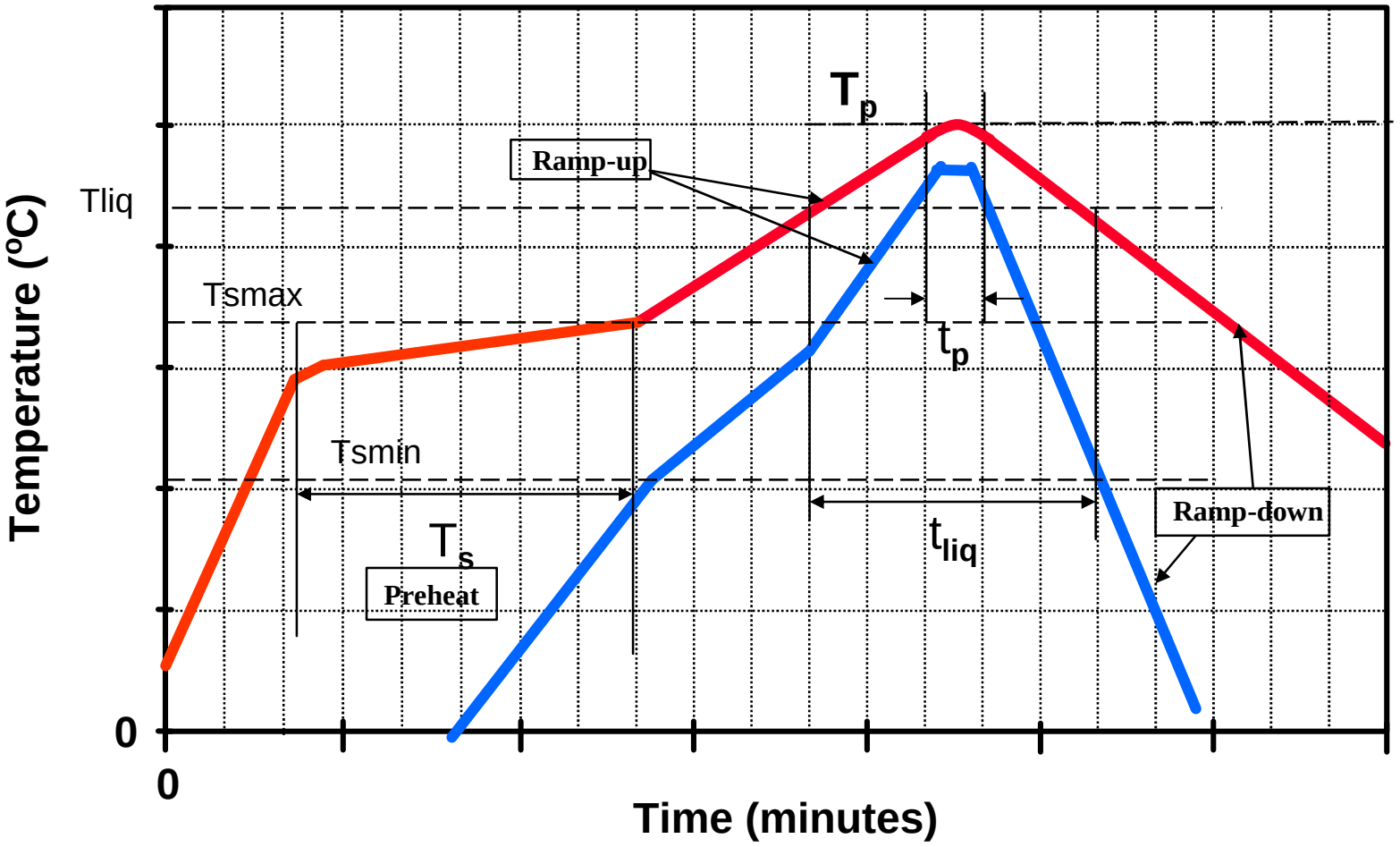
Sample MPN label printed

'HF' label on the shipping label for the 'Overpack' boxes is being define.

Shipping Label.

- HF: Halogen Free Indicator
- Located with other environmental indicators
- Approximate font size is 1 cm x 1 cm.
- Standard shipping label size is: 4.5 inches x 6.5 inches.

Standard Pb-Free Plating Reflow Profile



Reflow Profile For Lead-Free ONSEMI vs JEDEC

Profile Feature	JEDEC Pb-Free Profiles		ON Semi Pb-Free Profiles	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (Tliq to Tp)	3ºC/ second max		1.68ºC/ second	
Preheat - Temperature Min(Tsmin) - Temperature Max(Tsmax) - Time(min to max) (ts)	 150ºC 200ºC 60-180 seconds		 150ºC 180ºC 200 seconds max	
Tsmax to Tliq - Ramp-up Rate	3ºC/ second max		2.8ºC/second	
Time maintained above: - Temperature(Tliq) - Time(tliq)	 217ºC 60-150 seconds		 217ºC 90 seconds	
Peak Temperature(Tp)	245 +0/-5ºC	250 +0/-5ºC	260-265ºC	
Time within 5ºC of actual Peak Temperature(tp)	10-30 seconds	20-40 seconds	20 seconds	
Ramp-down Rate	6ºC/second max		1.2ºC/second	
Time 25ºC to Peak Temperature	8 minute max		5.2 -6 minutes	

- Large Body : Pkg Volume> 350 mm³; Small Body: Pkg Volume < 350 mm³
- 90% of ON Semi Packages < 350 mm³ in Volume