1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J71S | MLB_A

LAST_MODIFIED=Mon Aug 15 10:34:44 2016

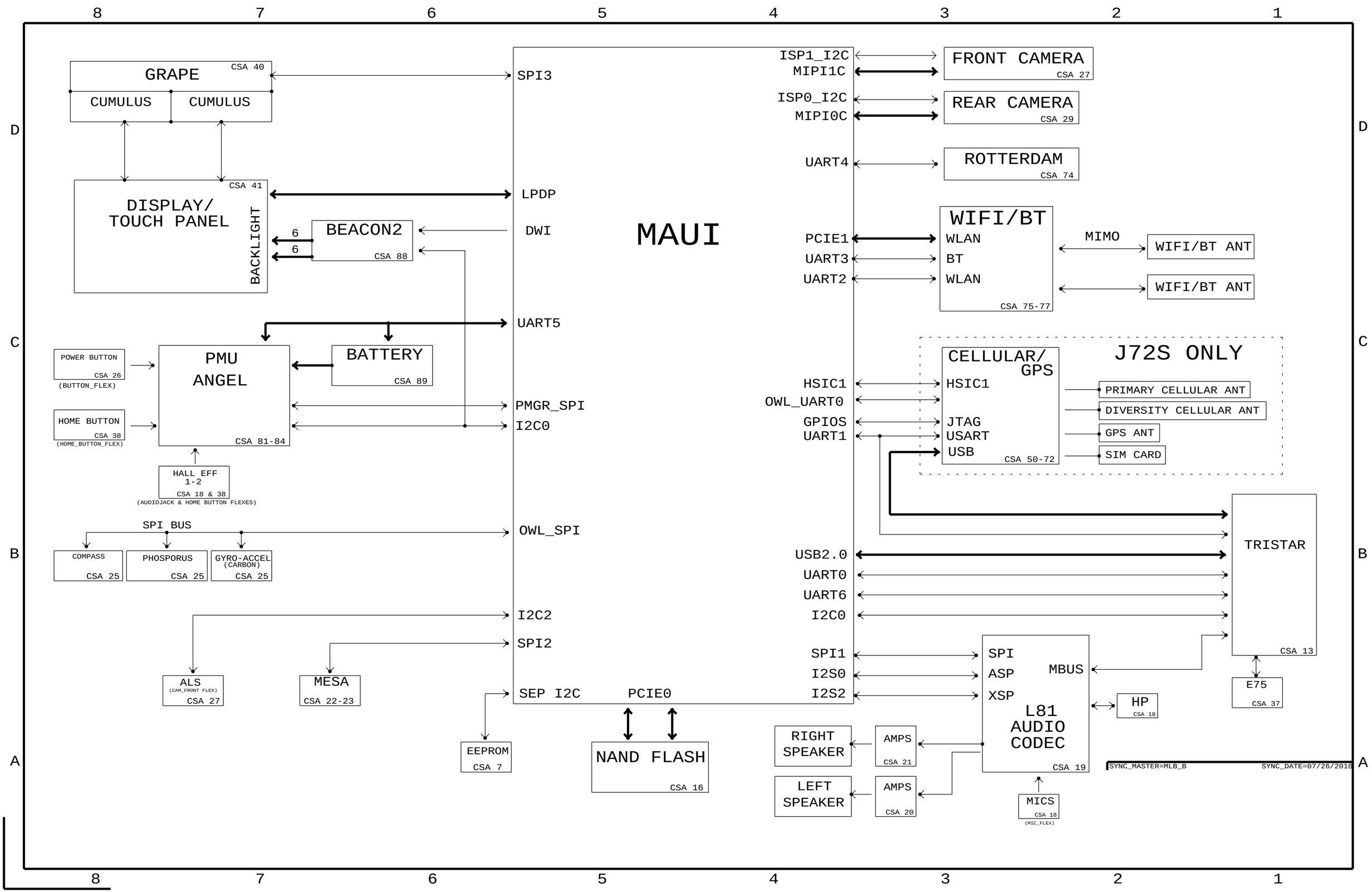
REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
2	0006866932	ENGINEERING RELEASED	2016-08-19

SCH AND BOARD PART NUMBERS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-01800	1	SCHEM,MLB_A,YN,J71S	SCH1	
820-00725	1	PCBF,MLB_A,YN,J71S	PCB1	

CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

DRAWING


8
7
6
5
4
3
2
1
D
C
B
A
GRAPE
CSA 40
CUMULUS
CUMULUS
DISPLAY/
TOUCH PANEL
CSA 41
BACKLIGHT
BEACON2
CSA 88
6
6
POWER BUTTON
CSA 26
(BUTTON_FLEX)
HOME BUTTON
CSA 38
(HOME_BUTTON_FLEX)
PMU
ANGEL
CSA 81-84
BATTERY
CSA 89
HALL EFF
1-2
CSA 18 & 38
(AUDIOJACK & HOME BUTTON FLEXES)
SPI BUS
COMPASS
CSA 25
PHOSPORUS
CSA 25
GYRO-ACCEL
(CARBON)
CSA 25
ALS
(CAM_FRONT FLEX)
CSA 27
MESA
CSA 22-23
EEPROM
CSA 7
NAND FLASH
CSA 16
SPI3
LPDP
DWI
UART5
PMGR_SPI
I2C0
OWL_SPI
I2C2
SPI2
SEP I2C
PCIE0
MAUI
ISP1_I2C
MIPI1C
FRONT CAMERA
CSA 27
ISP0_I2C
MIPI0C
REAR CAMERA
CSA 29
UART4
ROTTERDAM
CSA 74
WIFI/BT
PCIE1
WLAN
UART3
BT
UART2
WLAN
CSA 75-77
MIMO
WIFI/BT ANT
WIFI/BT ANT
J72S ONLY
CELLULAR/
GPS
HSIC1
OWL_UART0
GPIOS
UART1
HSIC1
JTAG
USART
USB
CSA 50-72
PRIMARY CELLULAR ANT
DIVERSITY CELLULAR ANT
GPS ANT
SIM CARD
TRISTAR
CSA 13
USB2.0
UART0
UART6
I2C0
SPI1
I2S0
I2S2
SPI
ASP
XSP
MBUS
L81
AUDIO
CODEC
CSA 19
HP
CSA 18
E75
CSA 37
RIGHT
SPEAKER
LEFT
SPEAKER
AMPS
CSA 21
AMPS
CSA 20
MICS
CSA 18
(MIC_FLEX)
SYNC_MASTER=MLB_B
SYNC_DATE=07/26/2016

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

SOC

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
MICRON	339S00097	1	POP,MAUI+2GB 25NM DDR,C0,M,DEV,FCMSP12G0	U0600	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
339S00096	339S00097		U0600	H DRAM - 25NM	NOT POR
339S00236	339S00097		U0600	H DRAM - 21NM	
339S00098	339S00097		U0600	S DRAM	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00007	155S0667			L2710,L2711,L2910,L2911,L2912,L2913,L2920

FLASH CONFIGURATIONS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
TOSHIBA	335S00235	1	NAND,1Z,32GBM,S3E,128GB,T,ULGA70	U1600	CRITICAL	32GB	2DP, GEN3, 1Z, SHIELDED
TOSHIBA	335S00174	1	NAND,1Z,128GBT,S3E,128G,T,ULGA70	U1600	CRITICAL	128GB	8DP, GEN3, 1Z

	PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
HYNIX	335S00160	335S00235		U1600	HYNIX 32G	4DP, GEN3, 1Z
HYNIX	335S00158	335S00174		U1600	HYNIX 128G	8DP, GEN3, 1Z

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
138S00032	138S0831		C0610,C0800,...	2.2UF 0201	RDAR #22885449
138S00006	138S0835		C0900,C0980,...	4.3UF	RDAR #22886293
138S00005	138S00003		C0160,C0161,...	15UF	RDAR #22886824
138S00056	138S1100		C1301,C1302,...	10UF	RDAR #22886497
138S0945	138S0739		C1760,...	1UF	
138S0706	138S0739		C1760,...	1UF	
376S00071	376S00073		Q0504		RDAR #23304176
376S00072	376S1211		Q0550		RDAR #22886067
335S00066	335S0946		U0701		RDAR #23002476
376S0948	376S00076		Q0900		
128S00062	128S00069		C81C0-C2	150UF	DESMOND EMAIL 3/17/16 5:05PM
132S0400	132S0436		C2521,C2525	0.22UF	RDAR #23002122
131S0641	131S00011		C4181,C8811,...	56PF	RDAR #23321717
197S0369	197S0392		Y8300	32.768K XTAL	RDAR #24177192
155S00097	155S0664		FL2780,...	FILTER_2P	RDAR #23399925
155S00017	155S0755		FL4190	FERRITE BEAD	RDAR #23169091
155S00016	155S0686		L1800,...	FILTER_2P	
155S0773	155S0453		FL2290-92,95-96	FILTER_2P	
155S00200	155S0610		FL2580,...	FILTER_2P	
138S0864	138S0709		C8547,...	4.7UF	RDAR #23320528
138S0875	138S0678		C81A0,...	10UF	
132S00005	132S0316		C0630,...	0.1UF	
353S01007	353S01039		NFCSW_RF	ON SEMI, LOAD SW	NFCSW_RF

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-09298	1	FENCE,AP,MLB,YY,J71S	PD_FENCE_AP	CRITICAL	
806-09240	1	SHIELD,GRAPE,MLB,YY,J71S	PD_SHIELD_GRAPE	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	EEEE FOR 639-02482 (GOOD)	H8N9	CRITICAL	EEEE_J71S_GD
825-7639	1	EEEE FOR 639-02483 (BETTER)	H8NC	CRITICAL	EEEE_J71S_BTR
825-7639	1	EEEE FOR 639-02484 (BEST)	H8ND	CRITICAL	EEEE_J71S_BST
825-7639	1	EEEE FOR 639-02485 (ULTIMATE)	H8NF	CRITICAL	EEEE_J71S_ULT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0631	1	RES,MF,100 OHM,1%,1/32W,01005	R0921	CRITICAL	MAUI
118S00009	1	RES,MF,3.01 KOHM,1%,1/32W,01005	R0921	CRITICAL	MALTA
118S0652	1	RES,MF,49.9 OHM,1/32W,01005	R0821	CRITICAL	MAUI
118S0631	1	RES,MF,100 OHM,1%,1/32W,01005	R0821	CRITICAL	MALTA
117S0161	1	RES,MF,0 OHM,1/32W,01005	R0651	CRITICAL	MAUI
118S00025	1	RES,MF,330 OHM,1%,1/32W,01005	R0651	CRITICAL	MALTA

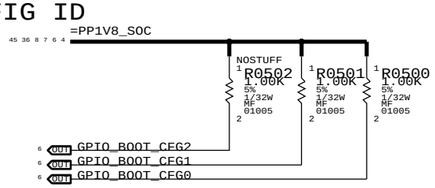
PHOSPHORUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00044	1	BMP282	U2580	CRITICAL	PHOS1_BMP282
338S00188	1	BMP284	U2580	CRITICAL	PHOS2_BMP284

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S00113	338S00044		U2780	BOSCH BMP282UBC

BOSCH BMP282BC

BOOT CONFIG ID



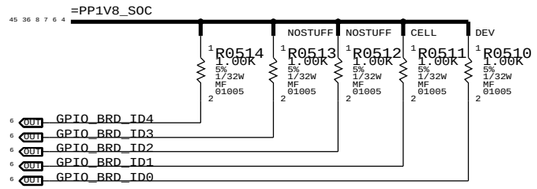
BOOT_CFG[2:0]	MODE
000	SPI0
001	SPI0 TEST MODE
010	NVME0 X2 MODE
011	NVME0 X2 TEST MODE
100	NVME0 X1 MODE
101	NVME0 X1 TEST MODE
110	SLOW SPI0 TEST MODE
111	FAST SPI0 TEST MODE

CURRENT SETTING --->

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID



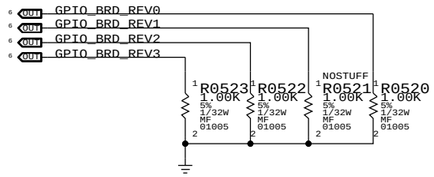
BRD_ID[4-0]	
10000	J71S AP (WIFI)
10001	J71S DEV
10010	J72S AP (CELL)
10011	J72S DEV

RDAR//PROBLEM/25022353

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION



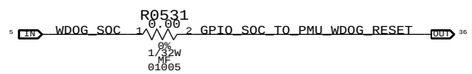
BRD_REV[3-0]		
0000	PROTO	(DEV, LOCAL P0 MLB_B REV 1)
0001	PROTO	(REWORKED DEV, MLB_B REV >1, MLB_A >=1)
0010	EVT	
0011	DVT	
0100	PVT	

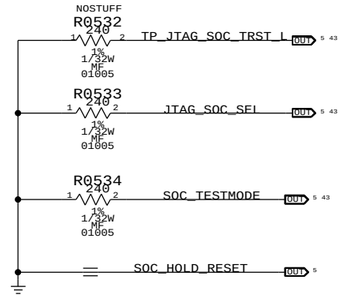
PHOSPHORUS 1
PHOSPHORUS 2 W/O IRQ
PHOSPHORUS 2 WITH IRQ --->

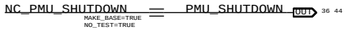
S/W READ FLOW

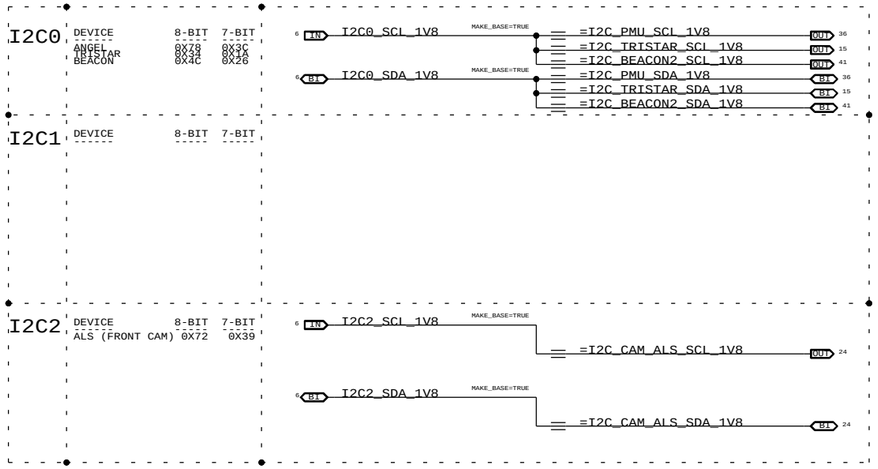
1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

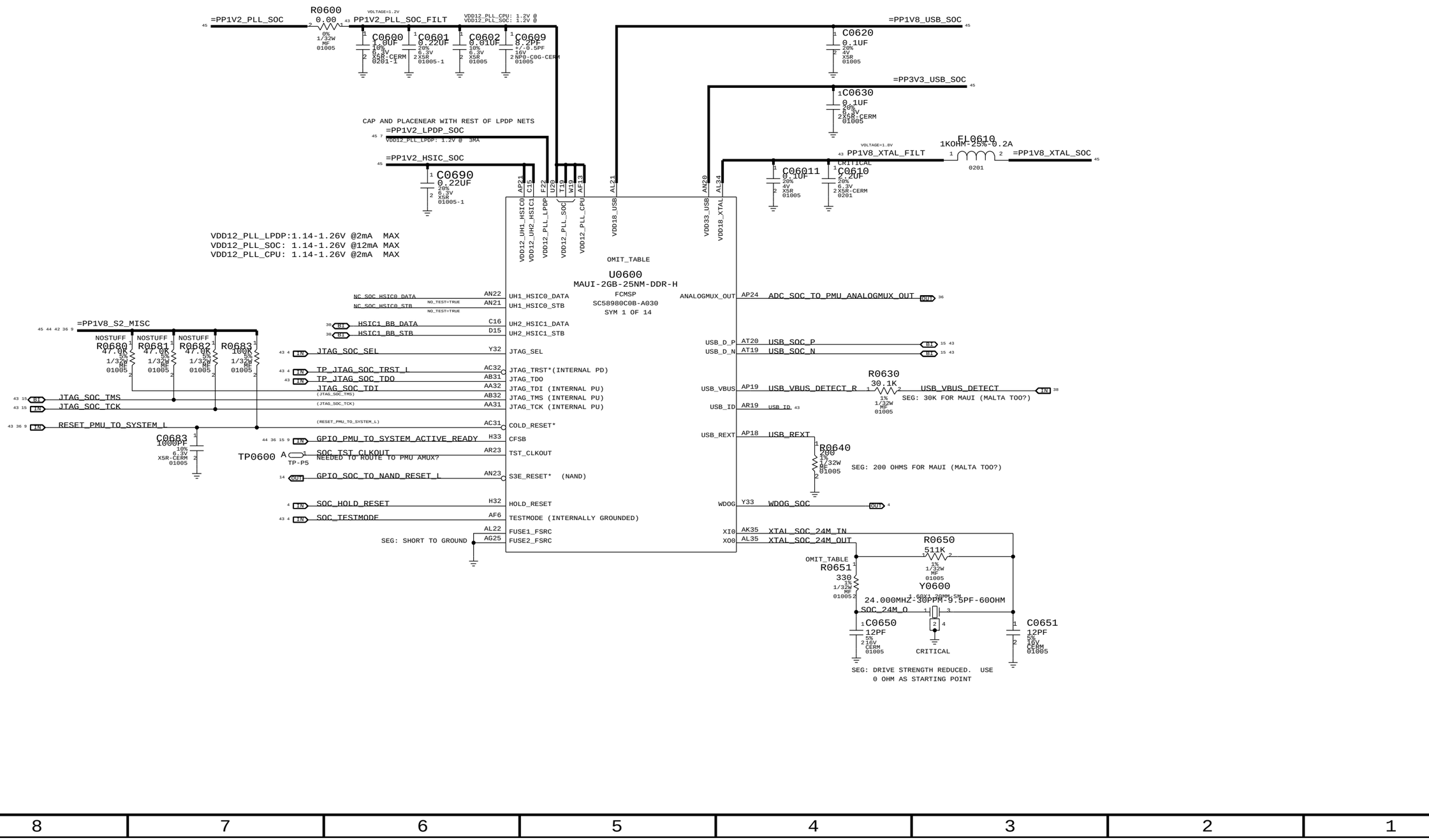
NOTE: CAN BE SHORTED ACROSS IF SPACE IS NEEDED

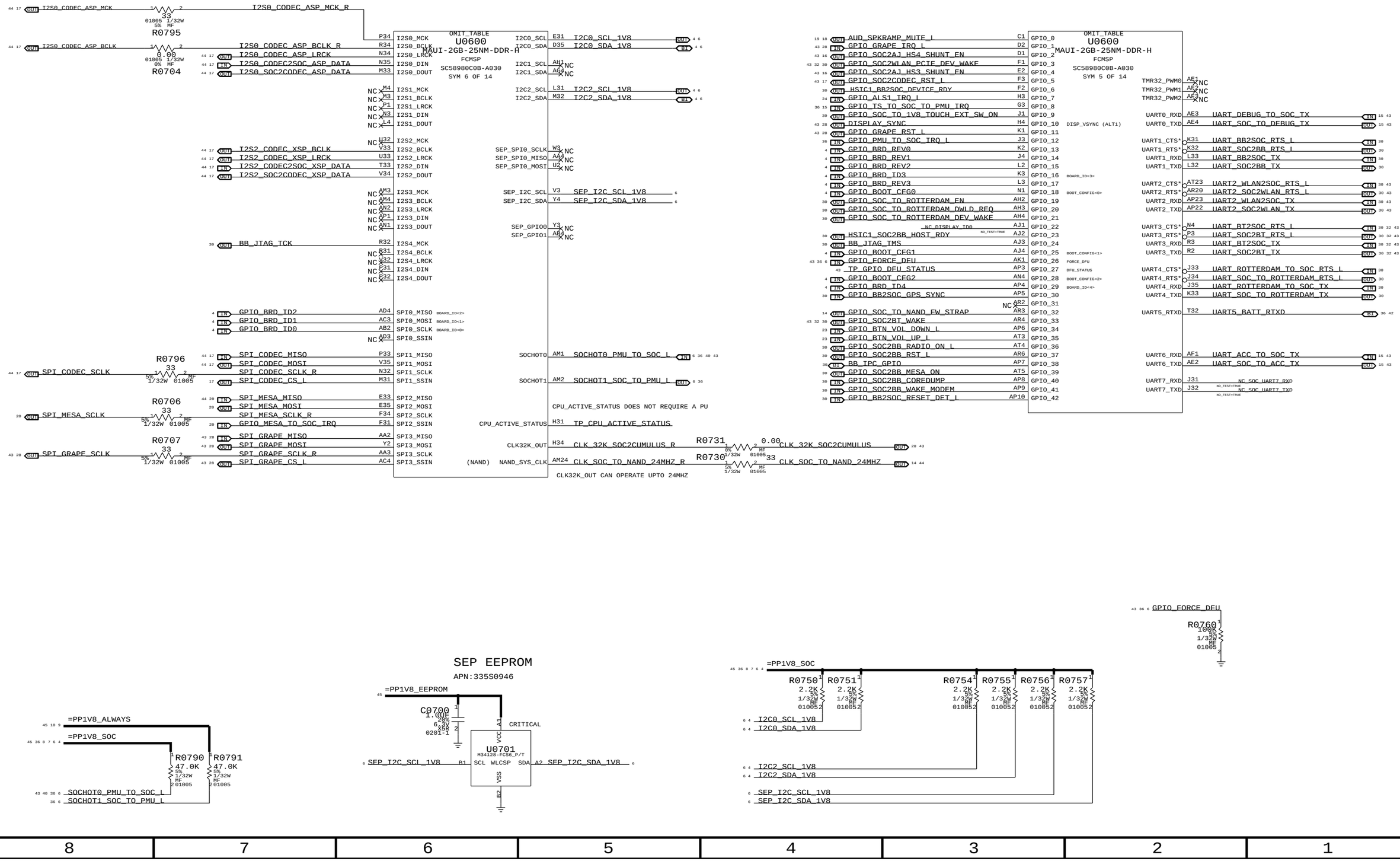


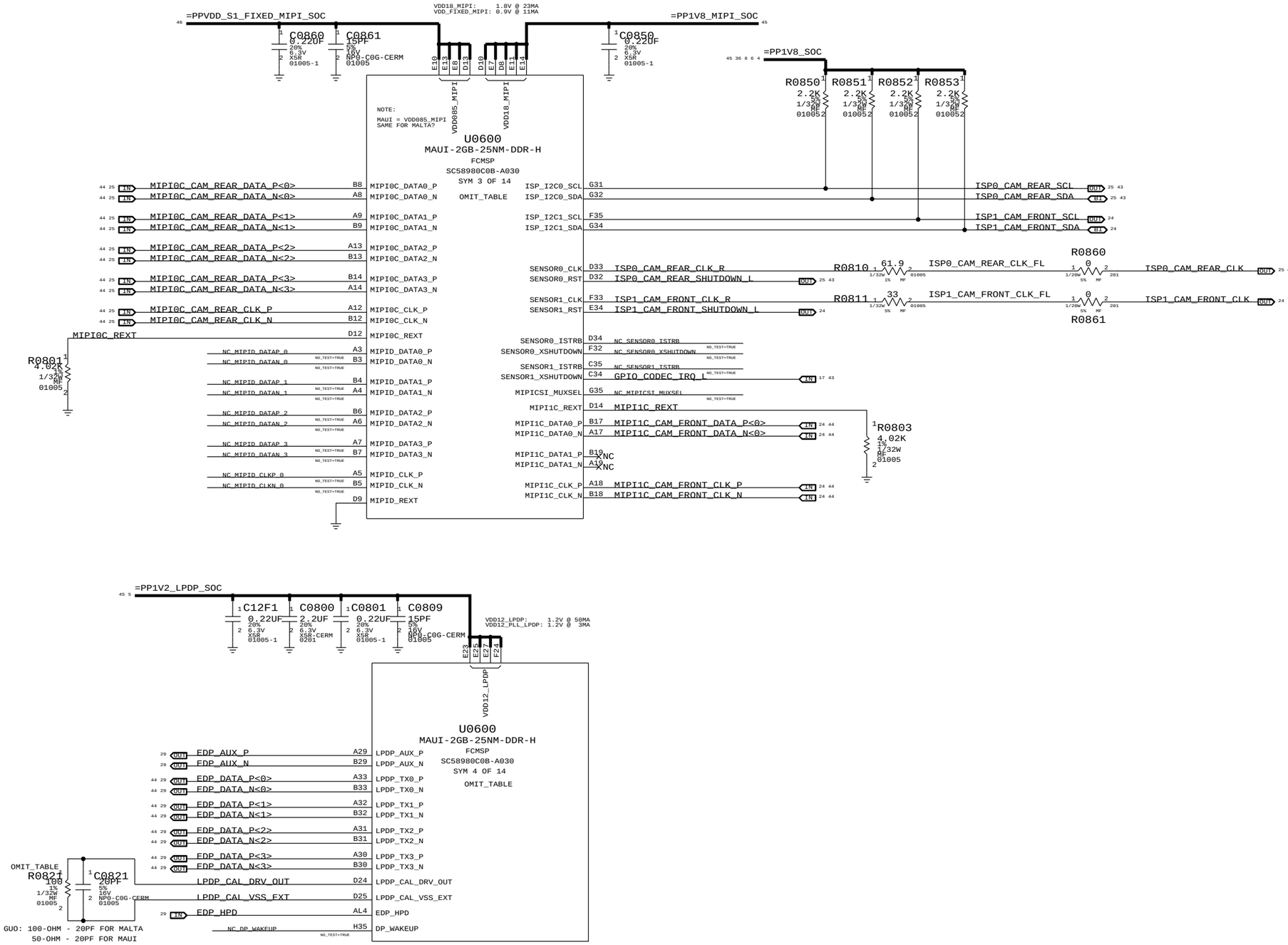







R0600
0.00
=PP1V2_PLL_SOC
PP1V2_PLL_SOC_FILT
VDD12_PLL_CPU: 1.2V @
VDD12_PLL_SOC: 1.2V @
C0600 1.0UF
C0601 0.22UF
C0602 0.01UF
C0609 8.2PF
CAP AND PLACENEAR WITH REST OF LPDP NETS
=PP1V2_LPDP_SOC
VDD12_PLL_LPDP: 1.2V @ 3MA
=PP1V2_HSIC_SOC
C0690 0.22UF
VDD12_PLL_LPDP:1.14-1.26V @2mA MAX
VDD12_PLL_SOC: 1.14-1.26V @12mA MAX
VDD12_PLL_CPU: 1.14-1.26V @2mA MAX
=PP1V8_USB_SOC
C0620 0.1UF
=PP3V3_USB_SOC
C0630 0.1UF
FL0610
1KOHM-25%-0.2A
=PP1V8_XTAL_SOC
PP1V8_XTAL_FILT
C0611 0.1UF
C0610 2.2UF
OMIT_TABLE
U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980C0B-A030
SYM 1 OF 14
VDD12_UH1_HSIC0
VDD12_UH2_HSIC1
VDD12_PLL_LPDP
VDD12_PLL_SOC
VDD12_PLL_CPU
VDD18_USB
VDD33_USB
VDD18_XTAL
NC_SOC_HSIC0_DATA
NC_SOC_HSIC0_STB
UH1_HSIC0_DATA
UH1_HSIC0_STB
ANALOGMUX_OUT
ADC_SOC_TO_PMU_ANALOGMUX_OUT
=PP1V8_S2_MISC
R0680 47.0K
R0681 47.0K
R0682 47.0K
R0683 100K
HSIC1_BB_DATA
HSIC1_BB_STB
UH2_HSIC1_DATA
UH2_HSIC1_STB
JTAG_SOC_SEL
TP_JTAG_SOC_TRST_L
TP_JTAG_SOC_TDO
JTAG_SOC_TDI
JTAG_SOC_TMS
JTAG_SOC_TCK
JTAG_TRST*(INTERNAL PD)
JTAG_TDO
JTAG_TDI (INTERNAL PU)
JTAG_TMS (INTERNAL PU)
JTAG_TCK (INTERNAL PU)
USB_D_P
USB_D_N
USB_SOC_P
USB_SOC_N
R0630 30.1K
USB_VBUS
USB_VBUS_DETECT_R
USB_VBUS_DETECT
SEG: 30K FOR MAUI (MALTA TOO?)
USB_ID
R0640 200
SEG: 200 OHMS FOR MAUI (MALTA TOO?)
RESET_PMU_TO_SYSTEM_L
C0683 1000PF
GPIO_PMU_TO_SYSTEM_ACTIVE_READY
SOC_TST_CLKOUT
TP0600
NEEDED TO ROUTE TO PMU AMUX?
GPIO_SOC_TO_NAND_RESET_L
CFSB
TST_CLKOUT
S3E_RESET* (NAND)
SOC_HOLD_RESET
SOC_TESTMODE
HOLD_RESET
TESTMODE (INTERNALLY GROUNDED)
FUSE1_FSRC
FUSE2_FSRC
SEG: SHORT TO GROUND
WDOG
WDOG_SOC
XI0
XO0
XTAL_SOC_24M_IN
XTAL_SOC_24M_OUT
R0650 511K
R0651 330
Y0600
24.000MHZ-30PPM-9.5PF-60OHM
SOC_24M_O
C0650 12PF
C0651 12PF
CRITICAL
SEG: DRIVE STRENGTH REDUCED. USE
0 OHM AS STARTING POINT


I2S0_CODEC_ASP_MCK
I2S0_CODEC_ASP_MCK_R
R0795
33
I2S0_CODEC_ASP_BCLK
I2S0_CODEC_ASP_BCLK_R
R0704
0.00
I2S0_CODEC_ASP_LRCK
I2S0_CODEC2SOC_ASP_DATA
I2S0_SOC2CODEC_ASP_DATA
OMIT_TABLE
U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980C0B-A030
SYM 6 OF 14
I2S0_MCK
I2S0_BCLK
I2S0_LRCK
I2S0_DIN
I2S0_DOUT
I2S1_MCK
I2S1_BCLK
I2S1_LRCK
I2S1_DIN
I2S1_DOUT
I2S2_MCK
I2S2_BCLK
I2S2_LRCK
I2S2_DIN
I2S2_DOUT
I2S3_MCK
I2S3_BCLK
I2S3_LRCK
I2S3_DIN
I2S3_DOUT
I2S2_CODEC_XSP_BCLK
I2S2_CODEC_XSP_LRCK
I2S2_CODEC2SOC_XSP_DATA
I2S2_SOC2CODEC_XSP_DATA
BB_JTAG_TCK
I2S4_MCK
I2S4_BCLK
I2S4_LRCK
I2S4_DIN
I2S4_DOUT
I2C0_SCL
I2C0_SDA
I2C0_SCL_1V8
I2C0_SDA_1V8
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA
I2C2_SCL_1V8
I2C2_SDA_1V8
SEP_SPI0_SCLK
SEP_SPI0_MISO
SEP_SPI0_MOSI
SEP_I2C_SCL
SEP_I2C_SDA
SEP_I2C_SCL_1V8
SEP_I2C_SDA_1V8
SEP_GPIO0
SEP_GPIO1
GPIO_BRD_ID2
GPIO_BRD_ID1
GPIO_BRD_ID0
SPI0_MISO
SPI0_MOSI
SPI0_SCLK
SPI0_SSIN
SPI_CODEC_MISO
SPI_CODEC_MOSI
SPI_CODEC_SCLK
SPI_CODEC_SCLK_R
SPI_CODEC_CS_L
SPI1_MISO
SPI1_MOSI
SPI1_SCLK
SPI1_SSIN
R0796
33
R0706
33
SPI_MESA_MISO
SPI_MESA_MOSI
SPI_MESA_SCLK
SPI_MESA_SCLK_R
GPIO_MESA_TO_SOC_IRQ
SPI2_MISO
SPI2_MOSI
SPI2_SCLK
SPI2_SSIN
R0707
33
SPI_GRAPE_MISO
SPI_GRAPE_MOSI
SPI_GRAPE_SCLK
SPI_GRAPE_SCLK_R
SPI_GRAPE_CS_L
SPI3_MISO
SPI3_MOSI
SPI3_SCLK
SPI3_SSIN
SOCHOT0
SOCHOT1
SOCHOT0_PMU_TO_SOC_L
SOCHOT1_SOC_TO_PMU_L
CPU_ACTIVE_STATUS DOES NOT REQUIRE A PU
CPU_ACTIVE_STATUS
TP_CPU_ACTIVE_STATUS
CLK32K_OUT
CLK_32K_SOC2CUMULUS_R
CLK_32K_SOC2CUMULUS
R0731
0.00
(NAND)
NAND_SYS_CLK
CLK_SOC_TO_NAND_24MHZ_R
R0730
33
CLK_SOC_TO_NAND_24MHZ
CLK32K_OUT CAN OPERATE UPTO 24MHZ
AUD_SPKRAMP_MUTE_L
GPIO_GRAPE_IRQ_L
GPIO_SOC2AJ_HS4_SHUNT_EN
GPIO_SOC2WLAN_PCIE_DEV_WAKE
GPIO_SOC2AJ_HS3_SHUNT_EN
GPIO_SOC2CODEC_RST_L
HSIC1_RB2SOC_DEVICE_RDY
GPIO_ALS1_IRQ_L
GPIO_TS_TO_SOC_TO_PMU_IRQ
GPIO_SOC_TO_1V8_TOUCH_EXT_SW_ON
DISPLAY_SYNC
GPIO_GRAPE_RST_L
GPIO_PMU_TO_SOC_IRQ_L
GPIO_BRD_REV0
GPIO_BRD_REV1
GPIO_BRD_REV2
GPIO_BRD_ID3
GPIO_BRD_REV3
GPIO_BOOT_CFG0
GPIO_SOC_TO_ROTTERDAM_EN
GPIO_SOC_TO_ROTTERDAM_DWLD_REQ
GPIO_SOC_TO_ROTTERDAM_DEV_WAKE
NC_DISPLAY_TD0
HSIC1_SOC2BB_HOST_RDY
BB_JTAG_TMS
GPIO_BOOT_CFG1
GPIO_FORCE_DFU
TP_GPIO_DFU_STATUS
GPIO_BOOT_CFG2
GPIO_BRD_ID4
GPIO_BB2SOC_GPS_SYNC
GPIO_SOC_TO_NAND_FW_STRAP
GPIO_SOC2BT_WAKE
GPIO_BTN_VOL_DOWN_L
GPIO_BTN_VOL_UP_L
GPIO_SOC2BB_RADIO_ON_L
GPIO_SOC2BB_RST_L
BB_TPC_GPIO
GPIO_SOC2BB_MESA_ON
GPIO_SOC2BB_COREDUMP
GPIO_SOC2BB_WAKE_MODEM
GPIO_BB2SOC_RESET_DET_L
OMIT_TABLE
U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980C0B-A030
SYM 5 OF 14
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_15
GPIO_16
GPIO_17
GPIO_18
GPIO_19
GPIO_20
GPIO_21
GPIO_22
GPIO_23
GPIO_24
GPIO_25
GPIO_26
GPIO_27
GPIO_28
GPIO_29
GPIO_30
GPIO_31
GPIO_32
GPIO_33
GPIO_34
GPIO_35
GPIO_36
GPIO_37
GPIO_38
GPIO_39
GPIO_40
GPIO_41
GPIO_42
DISP_VSYNC (ALT1)
BOARD_ID<3>
BOOT_CONFIG<0>
BOOT_CONFIG<1>
FORCE_DFU
DFU_STATUS
BOOT_CONFIG<2>
BOARD_ID<4>
TMR32_PWM0
TMR32_PWM1
TMR32_PWM2
UART0_RXD
UART0_TXD
UART1_CTS*
UART1_RTS*
UART1_RXD
UART1_TXD
UART2_CTS*
UART2_RTS*
UART2_RXD
UART2_TXD
UART3_CTS*
UART3_RTS*
UART3_RXD
UART3_TXD
UART4_CTS*
UART4_RTS*
UART4_RXD
UART4_TXD
UART5_RTXD
UART6_RXD
UART6_TXD
UART7_RXD
UART7_TXD
UART_DEBUG_TO_SOC_TX
UART_SOC_TO_DEBUG_TX
UART_BB2SOC_RTS_L
UART_SOC2BB_RTS_L
UART_BB2SOC_TX
UART_SOC2BB_TX
UART2_WLAN2SOC_RTS_L
UART2_SOC2WLAN_RTS_L
UART2_WLAN2SOC_TX
UART2_SOC2WLAN_TX
UART_BT2SOC_RTS_L
UART_SOC2BT_RTS_L
UART_BT2SOC_TX
UART_SOC2BT_TX
UART_ROTTERDAM_TO_SOC_RTS_L
UART_SOC_TO_ROTTERDAM_RTS_L
UART_ROTTERDAM_TO_SOC_TX
UART_SOC_TO_ROTTERDAM_TX
UART5_BATT_RTXD
UART_ACC_TO_SOC_TX
UART_SOC_TO_ACC_TX
NC_SOC_UART7_RXD
NC_SOC_UART7_TXD
NO_TEST=TRUE
=PP1V8_ALWAYS
=PP1V8_SOC
R0790
47.0K
R0791
47.0K
SOCHOT0_PMU_TO_SOC_L
SOCHOT1_SOC_TO_PMU_L
SEP EEPROM
APN:335S0946
=PP1V8_EEPROM
C0700
1.00UF
CRITICAL
U0701
M34128-FCS6_P/T
SCL WLCSP SDA
VCC
VSS
A1
A2
B1
B2
=PP1V8_SOC
R0750
R0751
R0754
R0755
R0756
R0757
2.2K
I2C0_SCL_1V8
I2C0_SDA_1V8
I2C2_SCL_1V8
I2C2_SDA_1V8
SEP_I2C_SCL_1V8
SEP_I2C_SDA_1V8
GPIO_FORCE_DFU
R0760
100K


=PPVDD_S1_FIXED_MIPI_SOC
VDD18_MIPI: 1.8V @ 23MA
VDD_FIXED_MIPI: 0.9V @ 11MA
=PP1V8_MIPI_SOC
C0860 0.22UF 20% 6.3V X5R 01005-1
C0861 15PF 5% 16V NP0-C0G-CERM 01005
C0850 0.22UF 20% 6.3V X5R 01005-1
=PP1V8_SOC
R0850 2.2K 1/32W MF 01005
R0851 2.2K 1/32W MF 01005
R0852 2.2K 1/32W MF 01005
R0853 2.2K 1/32W MF 01005
VDD085_MIPI
VDD18_MIPI
NOTE:
MAUI = VDD085_MIPI
SAME FOR MALTA?
U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980C0B-A030
SYM 3 OF 14
OMIT_TABLE
MIPI0C_CAM_REAR_DATA_P<0>
MIPI0C_CAM_REAR_DATA_N<0>
MIPI0C_CAM_REAR_DATA_P<1>
MIPI0C_CAM_REAR_DATA_N<1>
MIPI0C_CAM_REAR_DATA_P<2>
MIPI0C_CAM_REAR_DATA_N<2>
MIPI0C_CAM_REAR_DATA_P<3>
MIPI0C_CAM_REAR_DATA_N<3>
MIPI0C_CAM_REAR_CLK_P
MIPI0C_CAM_REAR_CLK_N
MIPI0C_REXT
R0801 4.02K 1% 1/32W MF 01005
ISP_I2C0_SCL
ISP_I2C0_SDA
ISP_I2C1_SCL
ISP_I2C1_SDA
ISP0_CAM_REAR_SCL
ISP0_CAM_REAR_SDA
ISP1_CAM_FRONT_SCL
ISP1_CAM_FRONT_SDA
SENSOR0_CLK
SENSOR0_RST
SENSOR1_CLK
SENSOR1_RST
ISP0_CAM_REAR_CLK_R
ISP0_CAM_REAR_SHUTDOWN_L
ISP1_CAM_FRONT_CLK_R
ISP1_CAM_FRONT_SHUTDOWN_L
R0810 61.9 1% 1/32W MF 01005
R0811 33 5% 1/32W MF 01005
R0860 0 5% 1/20W MF 201
R0861 0 5% 1/20W MF 201
ISP0_CAM_REAR_CLK_FL
ISP1_CAM_FRONT_CLK_FL
ISP0_CAM_REAR_CLK
ISP1_CAM_FRONT_CLK
SENSOR0_ISTRB
SENSOR0_XSHUTDOWN
SENSOR1_ISTRB
SENSOR1_XSHUTDOWN
MIPICSI_MUXSEL
MIPI1C_REXT
GPIO_CODEC_IRQ_L
MIPI1C_DATA0_P
MIPI1C_DATA0_N
MIPI1C_DATA1_P
MIPI1C_DATA1_N
MIPI1C_CLK_P
MIPI1C_CLK_N
MIPI1C_CAM_FRONT_DATA_P<0>
MIPI1C_CAM_FRONT_DATA_N<0>
MIPI1C_CAM_FRONT_CLK_P
MIPI1C_CAM_FRONT_CLK_N
R0803 4.02K 1% 1/32W MF 01005
MIPID_DATA0_P
MIPID_DATA0_N
MIPID_DATA1_P
MIPID_DATA1_N
MIPID_DATA2_P
MIPID_DATA2_N
MIPID_DATA3_P
MIPID_DATA3_N
MIPID_CLK_P
MIPID_CLK_N
MIPID_REXT
=PP1V2_LPDP_SOC
C12F1 0.22UF 20% 6.3V X5R 01005-1
C0800 2.2UF 20% 6.3V X5R-CERM 0201
C0801 0.22UF 20% 6.3V X5R 01005-1
C0809 15PF 5% 16V NP0-C0G-CERM 01005
VDD12_LPDP: 1.2V @ 50MA
VDD12_PLL_LPDP: 1.2V @ 3MA
VDD12_LPDP
U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980C0B-A030
SYM 4 OF 14
OMIT_TABLE
EDP_AUX_P
EDP_AUX_N
EDP_DATA_P<0>
EDP_DATA_N<0>
EDP_DATA_P<1>
EDP_DATA_N<1>
EDP_DATA_P<2>
EDP_DATA_N<2>
EDP_DATA_P<3>
EDP_DATA_N<3>
LPDP_CAL_DRV_OUT
LPDP_CAL_VSS_EXT
EDP_HPD
DP_WAKEUP
R0821 100 1% 1/32W MF 01005
C0821 20PF 5% 16V NP0-C0G-CERM 01005
OMIT_TABLE
EDWIN GUO: 100-OHM - 20PF FOR MALTA
50-OHM - 20PF FOR MAUI

NOTE: CAN DECAPS BE REDUCED?
N71 = 2.2UF, 1.0UF, 0.1UF

XW0900
SHORT-10L-0.1MM-SM

=PP1V2_PCIE_SOC

PPVDD12_PCIE_TXPLL
VOLTAGE=1.2V

VDD12_PCIE: 1.2V @ 115MA
VDD12_PCIE_REFBUF: 1.2V @ 50MA
VDD_FIXED_PCIE: 0.9V @ TBD

=PPVDD_S1_FIXED_PCIE_SOC

C0900 4.3UF 20% 4V CERM 0402 CRITICAL
C0901 1UF 20% 4V CERM 0402 CRITICAL
C0905 0.01UF 10% 6.3V X5R 01005
C0909 15PF 5% 16V NP0-C0G-CERM 01005
C0902 1.0UF 20% 6.3V X5R 0201-1
C0960 0.1UF 20% 6.3V X5R-CERM 01005
C0961 0.1UF 20% 6.3V X5R-CERM 01005
C0980 4.3UF 20% 4V CERM 0402 CRITICAL
C0981 4.3UF 20% 4V CERM 0402 CRITICAL
C0985 1UF 20% 4V CERM 0402 CRITICAL
C0986 1UF 20% 4V CERM 0402 CRITICAL
C0990 0.01UF 10% 6.3V X5R 01005
C0999 15PF 5% 16V NP0-C0G-CERM 01005

SOC_PCIE_EXT_C
AP29 PCIE_EXT_C

VDD12_PCIE
VDD12_PCIE_TXPLL
VDD12_PCIE_REFBUF
VDD085_PCIE

OMIT_TABLE
U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980C0B-A030
SYM 2 OF 14

NAND

PORT 0

PCIE_NAND_TO_SOC_TX_P<0>	AM30	PCIE_RX0_P
PCIE_NAND_TO_SOC_TX_N<0>	AN30	PCIE_RX0_N
PCIE_SOC_TO_NAND_TX_P<0> (C0930 0.1UF CRITICAL)	PCIE_SOC_TO_NAND_TX_C_P<0>	AT32 PCIE_TX0_P
PCIE_SOC_TO_NAND_TX_N<0> (C0931 0.1UF CRITICAL)	PCIE_SOC_TO_NAND_TX_C_N<0>	AR32 PCIE_TX0_N
PCIE_NAND_TO_SOC_TX_P<1>	AM28	PCIE_RX1_P
PCIE_NAND_TO_SOC_TX_N<1>	AN28	PCIE_RX1_N
PCIE_SOC_TO_NAND_TX_P<1> (C0932 0.1UF CRITICAL)	PCIE_SOC_TO_NAND_TX_C_P<1>	AT31 PCIE_TX1_P
PCIE_SOC_TO_NAND_TX_N<1> (C0933 0.1UF CRITICAL)	PCIE_SOC_TO_NAND_TX_C_N<1>	AR31 PCIE_TX1_N

WLAN/BT

PORT 1

PCIE1_WLAN2SOC_RX_P	AM27	PCIE_RX2_P
PCIE1_WLAN2SOC_RX_N	AN27	PCIE_RX2_N
PCIE1_SOC2WLAN_TX_P (C0940 0.1UF)	PCIE_SOC_TO_WLAN_TX_C_P	AT28 PCIE_TX2_P
PCIE1_SOC2WLAN_TX_N (C0941 0.1UF)	PCIE_SOC_TO_WLAN_TX_C_N	AR28 PCIE_TX2_N

PORT 2

NC	AM26	PCIE_RX3_P
NC	AN26	PCIE_RX3_N
NC	AT26	PCIE_TX3_P
NC	AR26	PCIE_TX3_N

PORT 3

NC_SOC_PCIE_RXP_4 (NO_TEST=TRUE)	AM25	PCIE_RX4_P
NC_SOC_PCIE_RXN_4 (NO_TEST=TRUE)	AN25	PCIE_RX4_N
NC_SOC_PCIE_TXP_4 (NO_TEST=TRUE)	AR24	PCIE_TX4_P
NC_SOC_PCIE_TXN_4 (NO_TEST=TRUE)	AT24	PCIE_TX4_N

PCIE_REF_CLK0_P	AN35	PCIE_SOC_TO_NAND_REFCLK_P (OUT)
PCIE_REF_CLK0_N	AP35	PCIE_SOC_TO_NAND_REFCLK_N (OUT)
PCIE_REF_CLK1_P	AN34	PCIE1_SOC2WLAN_REFCLK_P (OUT)
PCIE_REF_CLK1_N	AP34	PCIE1_SOC2WLAN_REFCLK_N (OUT)
PCIE_REF_CLK2_P	AM32	XNC
PCIE_REF_CLK2_N	AN32	XNC
PCIE_REF_CLK3_P	AM31	NC_SOC_PCIE_REF_CLKP_3 (NO_TEST=TRUE)
PCIE_REF_CLK3_N	AN31	NC_SOC_PCIE_REF_CLKN_3 (NO_TEST=TRUE)

(NAND) PCIE_CLKREQ0*	AT11	PCIE_NAND_TO_SOC_CLKREQ_L (IN)
PCIE_CLKREQ1*	AP12	PCIE1_WLAN2SOC_CLKREQ_L (IN)
PCIE_CLKREQ2*	AR12	XNC
PCIE_CLKREQ3*	AT12	NC_SOC_PCIE_CLKREQ3_L (NO_TEST=TRUE)

(NAND) PCIE_PERST0*	AR10	PCIE_SOC_TO_NAND_RESET_L (OUT)
PCIE_PERST1*	AT10	PCIE1_SOC2WLAN_RST_L (OUT)
PCIE_PERST2*	AP11	XNC
PCIE_PERST3*	AR11	NC_SOC_PCIE_PERST3_L (NO_TEST=TRUE)

PCIE_EXT_REF_CLK_P	AR33	
PCIE_EXT_REF_CLK_N	AT33	
PCIE_RX_TX_BYPASS_CLK_P	AT29	
PCIE_RX_TX_BYPASS_CLK_N	AR29	

PCIE_RCAL_P	AT30	PCIE_RCAL_P
PCIE_RCAL_N	AR30	PCIE_RCAL_N

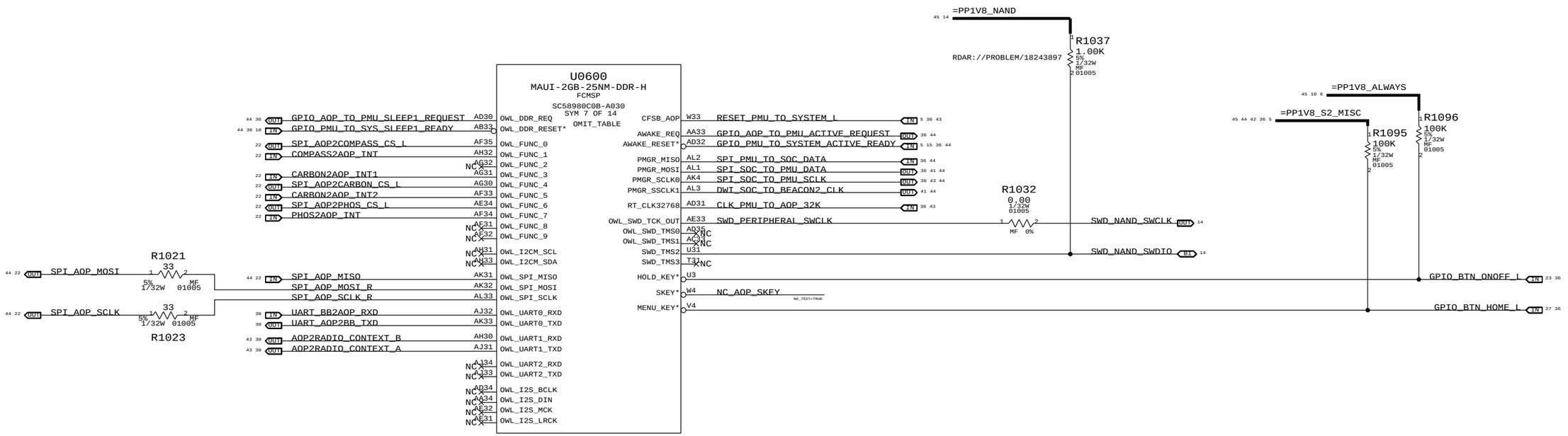
OMIT_TABLE R0921 3.01K 1% 1/32W MF 01005
MAUI C0921 100PF 5% 16V NP0-C0G 01005

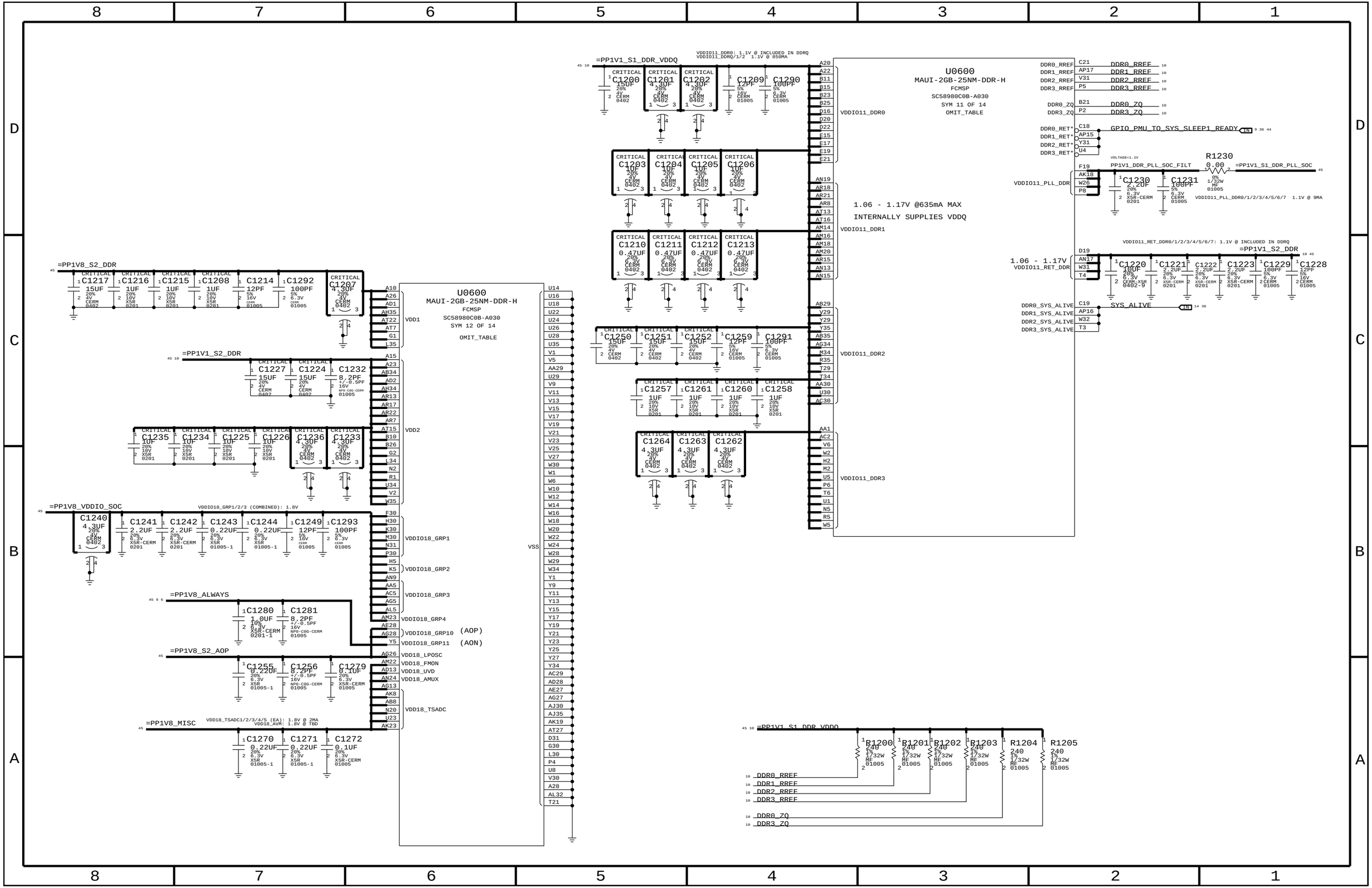
=PP1V8_SOC

R0930 47.0K 5% 1/32W MF 201005
R0940 47.0K 5% 1/32W MF 201005

PCIE_NAND_TO_SOC_CLKREQ_L
PCIE1_NAND_TO_SOC_CLKREQ_L
PCIE_SOC_TO_NAND_RESET_L
PCIE1_SOC2WLAN_RST_L

R0941 100K 5% 1/32W MF 201005
R0931 100K 5% 1/32W MF 201005


U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980C0B-A030
SYM 7 OF 14
OMIT_TABLE
GPIO_AOP_TO_PMU_SLEEP1_REQUEST
GPIO_PMU_TO_SYS_SLEEP1_READY
SPI_AOP2COMPASS_CS_L
COMPASS2AOP_INT
CARBON2AOP_INT1
SPI_AOP2CARBON_CS_L
CARBON2AOP_INT2
SPI_AOP2PHOS_CS_L
PHOS2AOP_INT
SPI_AOP_MOSI
SPI_AOP_MISO
SPI_AOP_MOST_R
SPI_AOP_SCLK_R
SPI_AOP_SCLK
UART_BB2AOP_RXD
UART_AOP2BB_TXD
AOP2RADIO_CONTEXT_B
AOP2RADIO_CONTEXT_A
R1021
33
5%
1/32W
MF
01005
R1023
OWL_DDR_REQ
OWL_DDR_RESET*
OWL_FUNC_0
OWL_FUNC_1
OWL_FUNC_2
OWL_FUNC_3
OWL_FUNC_4
OWL_FUNC_5
OWL_FUNC_6
OWL_FUNC_7
OWL_FUNC_8
OWL_FUNC_9
OWL_I2CM_SCL
OWL_I2CM_SDA
OWL_SPI_MISO
OWL_SPI_MOSI
OWL_SPI_SCLK
OWL_UART0_RXD
OWL_UART0_TXD
OWL_UART1_RXD
OWL_UART1_TXD
OWL_UART2_RXD
OWL_UART2_TXD
OWL_I2S_BCLK
OWL_I2S_DIN
OWL_I2S_MCK
OWL_I2S_LRCK
CFSB_AOP
AWAKE_REQ
AWAKE_RESET*
PMGR_MISO
PMGR_MOSI
PMGR_SCLK0
PMGR_SSCLK1
RT_CLK32768
OWL_SWD_TCK_OUT
OWL_SWD_TMS0
OWL_SWD_TMS1
SWD_TMS2
SWD_TMS3
HOLD_KEY*
SKEY*
MENU_KEY*
RESET_PMU_TO_SYSTEM_L
GPIO_AOP_TO_PMU_ACTIVE_REQUEST
GPIO_PMU_TO_SYSTEM_ACTIVE_READY
SPI_PMU_TO_SOC_DATA
SPI_SOC_TO_PMU_DATA
SPI_SOC_TO_PMU_SCLK
DWI_SOC_TO_BEACON2_CLK
CLK_PMU_TO_AOP_32K
SWD_PERIPHERAL_SWCLK
NC_AOP_SKEY
NO_TEST=TRUE
NC
=PP1V8_NAND
R1037
1.00K
RDAR://PROBLEM/18243897
R1032
0.00
SWD_NAND_SWCLK
SWD_NAND_SWDIO
=PP1V8_ALWAYS
=PP1V8_S2_MISC
R1095
100K
R1096
GPIO_BTN_ONOFF_L
GPIO_BTN_HOME_L


=PP1V1_S1_DDR_VDDQ
VDDIO11_DDR0: 1.1V @ INCLUDED IN DDRQ
VDDIO11_DDRQ/1/2 1.1V @ 850MA
C1200 15UF
C1201 4.3UF
C1202 4.3UF
C1209 12PF
C1290 100PF
C1203 10F
C1204 10F
C1205 1UF
C1206 1UF
C1210 0.47UF
C1211 0.47UF
C1212 0.47UF
C1213 0.47UF
C1250 15UF
C1251 15UF
C1252 15UF
C1259 12PF
C1291 100PF
C1257 1UF
C1261 1UF
C1260 1UF
C1258 1UF
C1264 4.3UF
C1263 4.3UF
C1262 4.3UF
U0600
MAUI-2GB-25NM-DDR-H
FCMSP
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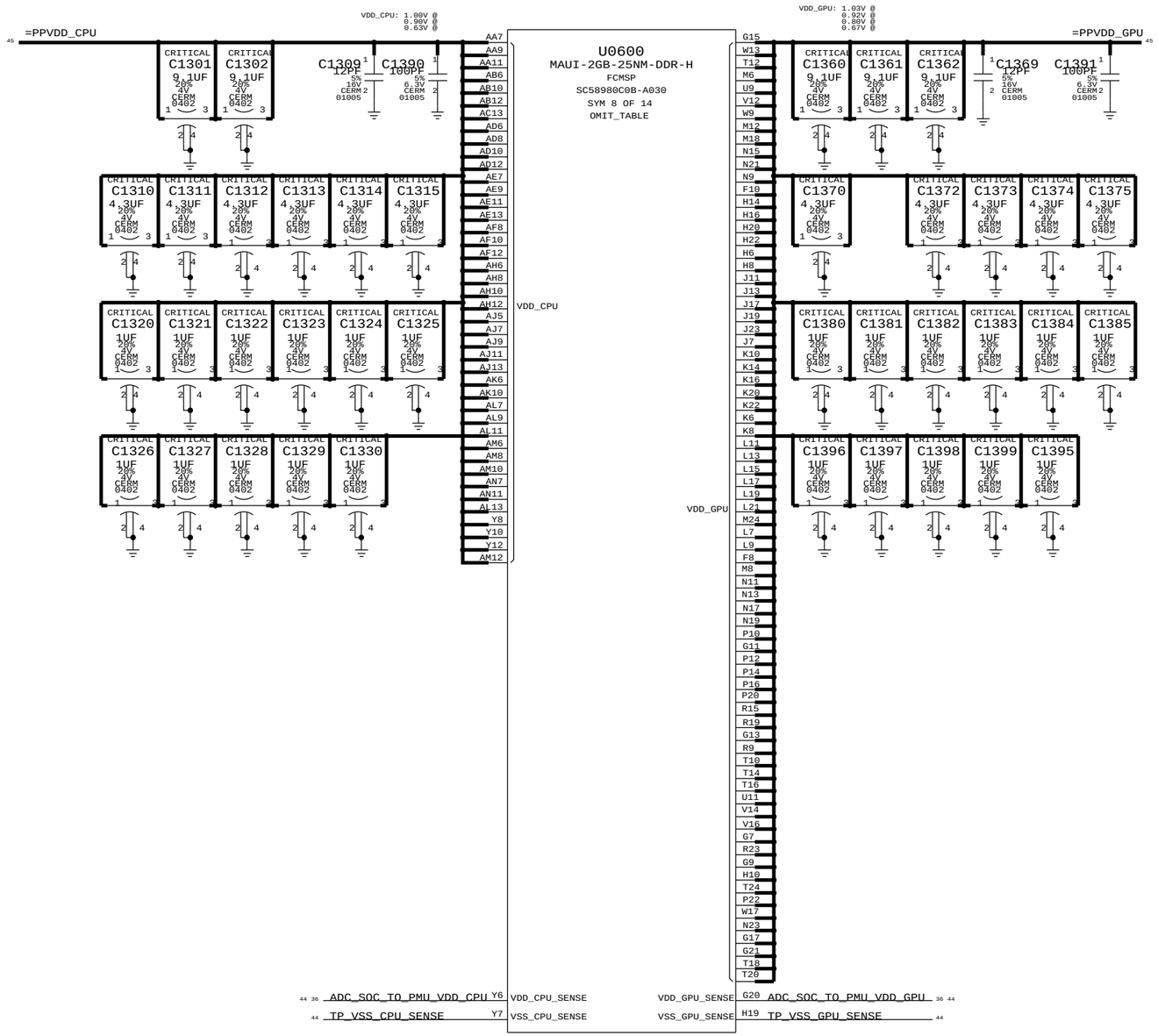
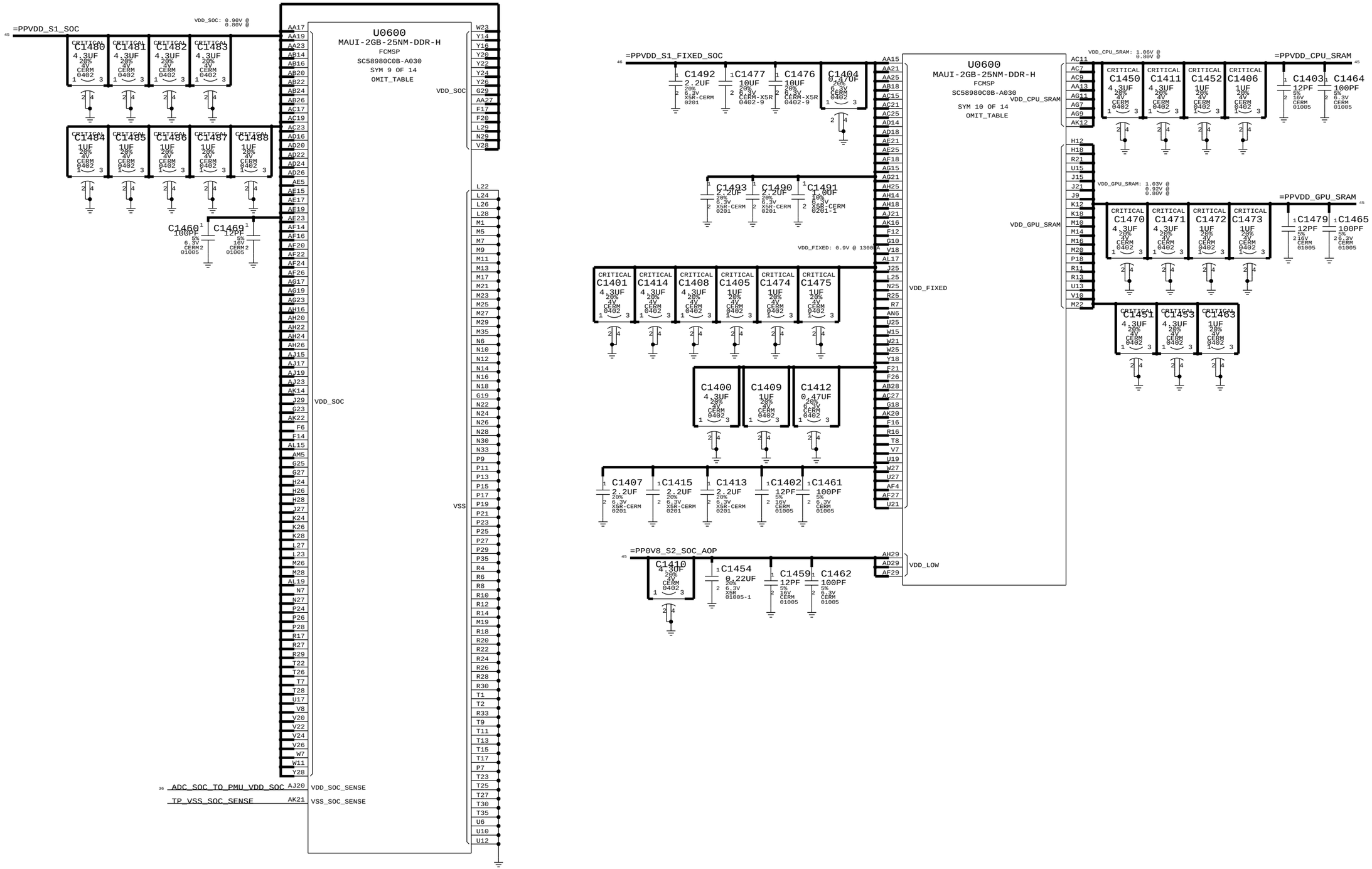
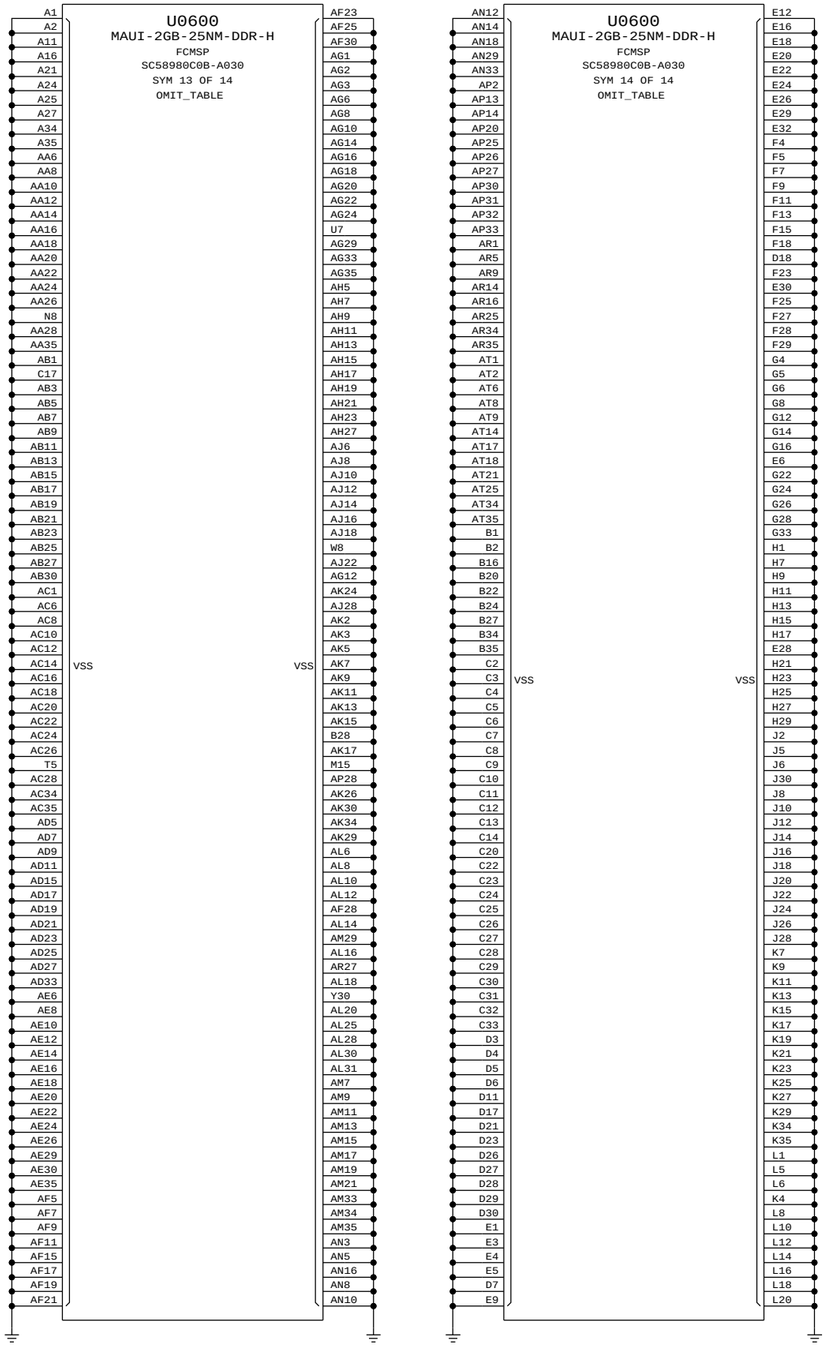
SYM 11 OF 14
OMIT_TABLE
VDDIO11_DDR0
VDDIO11_DDR1
VDDIO11_DDR2
VDDIO11_DDR3
1.06 - 1.17V @635mA MAX
INTERNALLY SUPPLIES VDDQ
DDR0_RREF
DDR1_RREF
DDR2_RREF
DDR3_RREF
DDR0_ZQ
DDR3_ZQ
GPIO_PMU_TO_SYS_SLEEP1_READY
R1230 0.00
=PP1V1_S1_DDR_PLL_SOC
VDDIO11_PLL_DDR
PP1V1_DDR_PLL_SOC_FILT
C1230 2.2UF
C1231 100PF
VDDIO11_PLL_DDR0/1/2/3/4/5/6/7 1.1V @ 9MA
VDDIO11_RET_DDR0/1/2/3/4/5/6/7: 1.1V @ INCLUDED IN DDRQ
1.06 - 1.17V
VDDIO11_RET_DDR
=PP1V1_S2_DDR
C1220 10UF
C1221 2.2UF
C1222 2.2UF
C1223 2.2UF
C1229 100PF
C1228 12PF
DDR0_SYS_ALIVE
DDR1_SYS_ALIVE
DDR2_SYS_ALIVE
DDR3_SYS_ALIVE
SYS_ALIVE
=PP1V8_S2_DDR
C1217 15UF
C1216 1UF
C1215 1UF
C1208 1UF
C1214 12PF
C1292 100PF
C1207 4.3UF
VDD1
=PP1V1_S2_DDR
C1227 15UF
C1224 15UF
C1232 8.2PF
C1235 1UF
C1234 1UF
C1225 1UF
C1226 1UF
C1236 4.3UF
C1233 4.3UF
VDD2
=PP1V8_VDDIO_SOC
VDDIO18_GRP1/2/3 (COMBINED): 1.8V
C1240 4.3UF
C1241 2.2UF
C1242 2.2UF
C1243 0.22UF
C1244 0.22UF
C1249 12PF
C1293 100PF
VDDIO18_GRP1
VDDIO18_GRP2
VDDIO18_GRP3
=PP1V8_ALWAYS
C1280 1.0UF
C1281 8.2PF
VDDIO18_GRP4
VDDIO18_GRP10 (AOP)
VDDIO18_GRP11 (AON)
=PP1V8_S2_AOP
C1255 0.22UF
C1256 8.2PF
C1279 0.1UF
VDD18_LPOSC
VDD18_FMON
VDD18_UVD
VDD18_AMUX
=PP1V8_MISC
VDD18_TSADC1/2/3/4/5 (EA): 1.8V @ 2MA
VDD18_AVM: 1.8V @ TBD
C1270 0.22UF
C1271 0.22UF
C1272 0.1UF
VDD18_TSADC
VSS
=PP1V1_S1_DDR_VDDQ
R1200 240
R1201 240
R1202 240
R1203 240
R1204 240
R1205 240
DDR0_RREF
DDR1_RREF
DDR2_RREF
DDR3_RREF
DDR0_ZQ
DDR3_ZQ

MALTA - POWER SUPPLIES




=PPVDD_S1_SOC
VDD_SOC: 0.90V @ 0.80V @
C1480 4.3UF
C1481 4.3UF
C1482 4.3UF
C1483 4.3UF
C1484 1UF
C1485 1UF
C1486 1UF
C1487 1UF
C1488 1UF
C1460 100PF
C1469 12PF
U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980C0B-A030
SYM 9 OF 14
OMIT_TABLE
VDD_SOC
VSS
ADC_SOC_TO_PMU_VDD_SOC
TP_VSS_SOC_SENSE
VDD_SOC_SENSE
VSS_SOC_SENSE
=PPVDD_S1_FIXED_SOC
C1492 2.2UF
C1477 10UF
C1476 10UF
C1404 0.47UF
C1493 2.2UF
C1490 2.2UF
C1491 1.00UF
VDD_FIXED: 0.9V @ 1300mA
C1401 4.3UF
C1414 4.3UF
C1408 4.3UF
C1405 1UF
C1474 1UF
C1475 1UF
C1400 4.3UF
C1409 1UF
C1412 0.47UF
C1407 2.2UF
C1415 2.2UF
C1413 2.2UF
C1402 12PF
C1461 100PF
VDD_FIXED
VDD_CPU_SRAM
VDD_GPU_SRAM
VDD_LOW
=PP0V8_S2_SOC_AOP
C1410 4.3UF
C1454 0.22UF
C1459 12PF
C1462 100PF
VDD_CPU_SRAM: 1.06V @ 0.80V @
=PPVDD_CPU_SRAM
C1450 4.3UF
C1411 4.3UF
C1452 1UF
C1406 1UF
C1403 12PF
C1464 100PF
VDD_GPU_SRAM: 1.03V @ 0.92V @ 0.86V @
=PPVDD_GPU_SRAM
C1470 4.3UF
C1471 4.3UF
C1472 1UF
C1473 1UF
C1479 12PF
C1465 100PF
C1451 4.3UF
C1453 4.3UF
C1463 1UF


U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980C0B-A030
SYM 13 OF 14
OMIT_TABLE
A1
A2
A11
A16
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A27
A34
A35
AA6
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AA18
AA20
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AA24
AA26
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AA35
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C17
AB3
AB5
AB7
AB9
AB11
AB13
AB15
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AB23
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AB27
AB30
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AF5
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U7
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AJ6
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AK17
M15
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AK26
AK30
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AK29
AL6
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AN5
AN16
AN8
AN10
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U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980C0B-A030
SYM 14 OF 14
OMIT_TABLE
AN12
AN14
AN18
AN29
AN33
AP2
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AP30
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VSS
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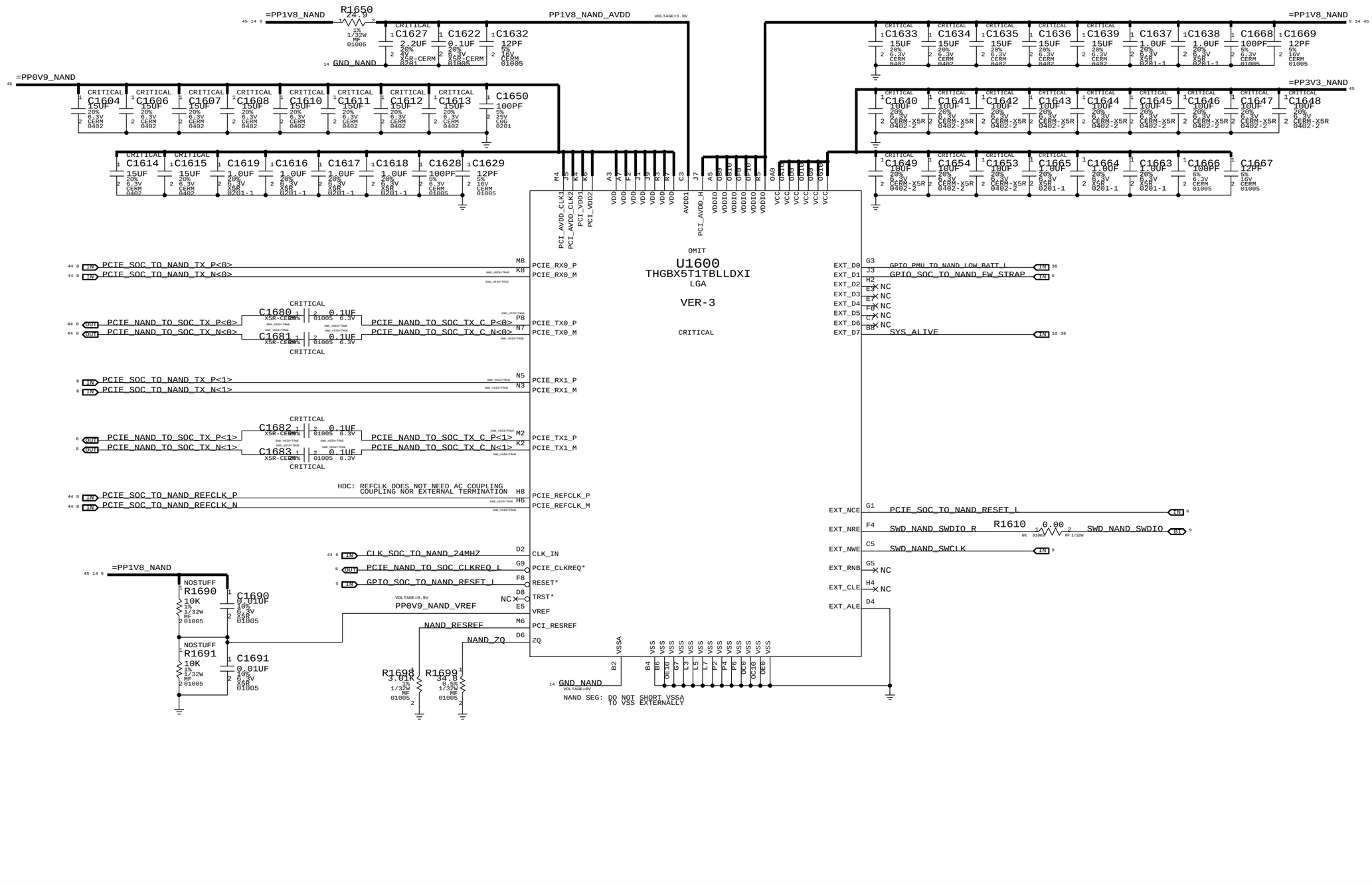
VSS


=PP1V8_NAND
R1650
24.9
1%
1/32W
MF
01005
PP1V8_NAND_AVDD
VOLTAGE=1.8V
GND_NAND
C1627
2.2UF
C1622
0.1UF
C1632
12PF
=PP0V9_NAND
C1650
100PF
=PP3V3_NAND
C1669
U1600
THGBX5T1TBLLDXI
LGA
VER-3
OMIT
CRITICAL
PCIE_SOC_TO_NAND_TX_P<0>
PCIE_SOC_TO_NAND_TX_N<0>
PCIE_NAND_TO_SOC_TX_P<0>
PCIE_NAND_TO_SOC_TX_N<0>
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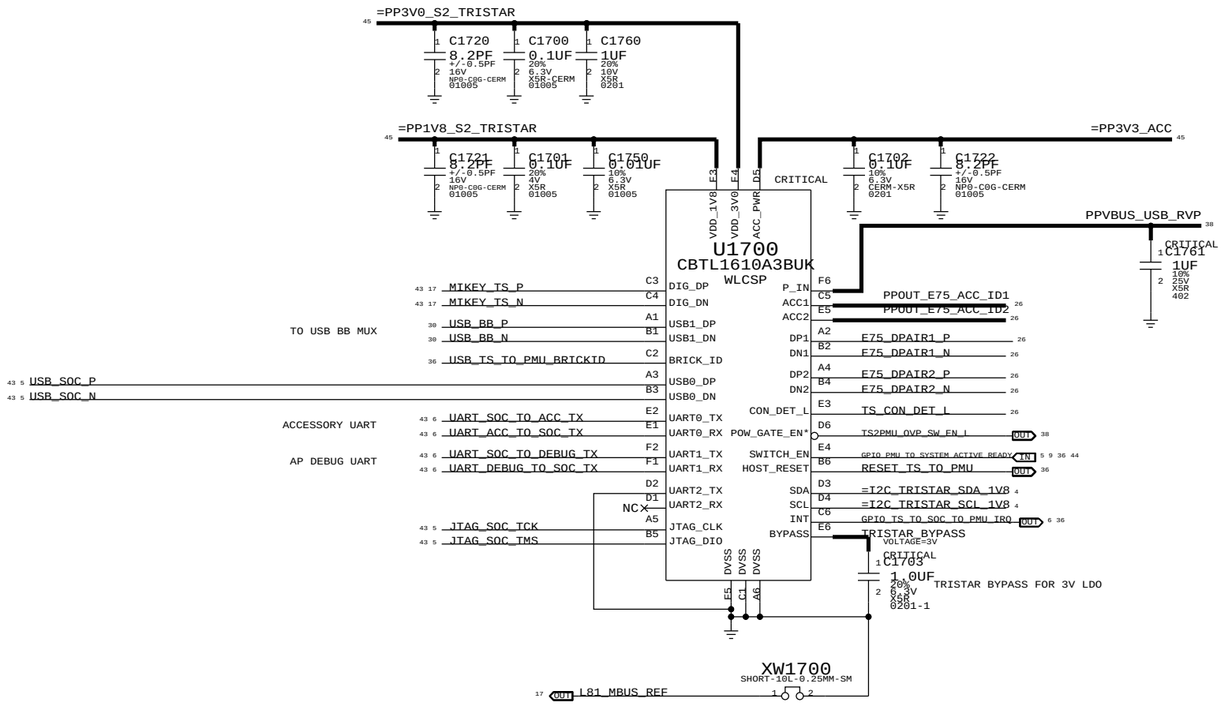
PCIE_NAND_TO_SOC_TX_P<1>
PCIE_NAND_TO_SOC_TX_N<1>
PCIE_SOC_TO_NAND_REFCLK_P
PCIE_SOC_TO_NAND_REFCLK_N
HDC: REFCLK DOES NOT NEED AC COUPLING
COUPLING NOR EXTERNAL TERMINATION
CLK_SOC_TO_NAND_24MHZ
PCIE_NAND_TO_SOC_CLKREQ_L
GPIO_SOC_TO_NAND_RESET_L
PP0V9_NAND_VREF
NAND_RESREF
NAND_ZQ
NAND SEG: DO NOT SHORT VSSA
TO VSS EXTERNALLY
GPIO_PMU_TO_NAND_LOW_BATT_L
GPIO_SOC_TO_NAND_FW_STRAP
SYS_ALIVE
PCIE_SOC_TO_NAND_RESET_L
SWD_NAND_SWDIO_R
R1610
0.00
SWD_NAND_SWDIO
SWD_NAND_SWCLK

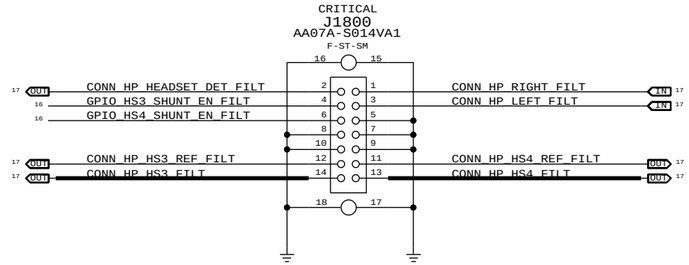
TRISTAR

343S0605 = TRISTAR 2, A3
343S0658 = TRISTAR 2, A1
339S0055 = TRISTAR 2, I6
343S0659 = TRISTAR 2, A0
343S0614 = TRISTAR 1
NOTE: A2 ONLY USED ON IPHONES

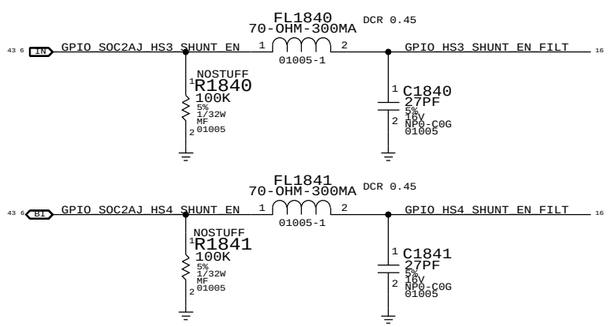


HP JACK B2B CONNECTOR

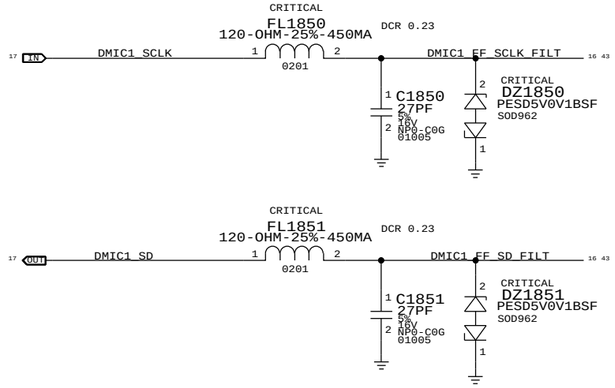
J1800 MATCHES AUDIO_JACK_FLEX_3.0.0 1/9/13
MLB: 516S1084
FLEX: 516S1085



SHUNT FILTERS



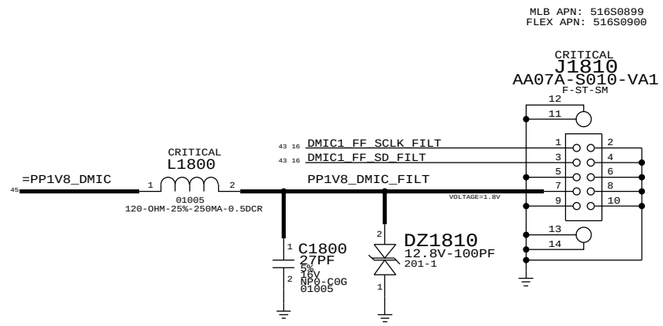
DMIC FILTERS



MICROPHONE FLEX B2B CONNECTOR

J1810 MATCHES MIC_FLEX_2.0.0 1/7/13

MLB APN: 516S0899
FLEX APN: 516S0900



SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0077	377S0111			

DZ1850,DZ1851

NOTE:
U1900 DECAPS CHANGED ON 5/24/12 PER RADAR #11485846

MIKEY BUS FILTER

TO TRISTAR

TO HEADPHONE JACK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S1213	338S1116		U1900	RADAR:13373870 SSMC FAB

SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

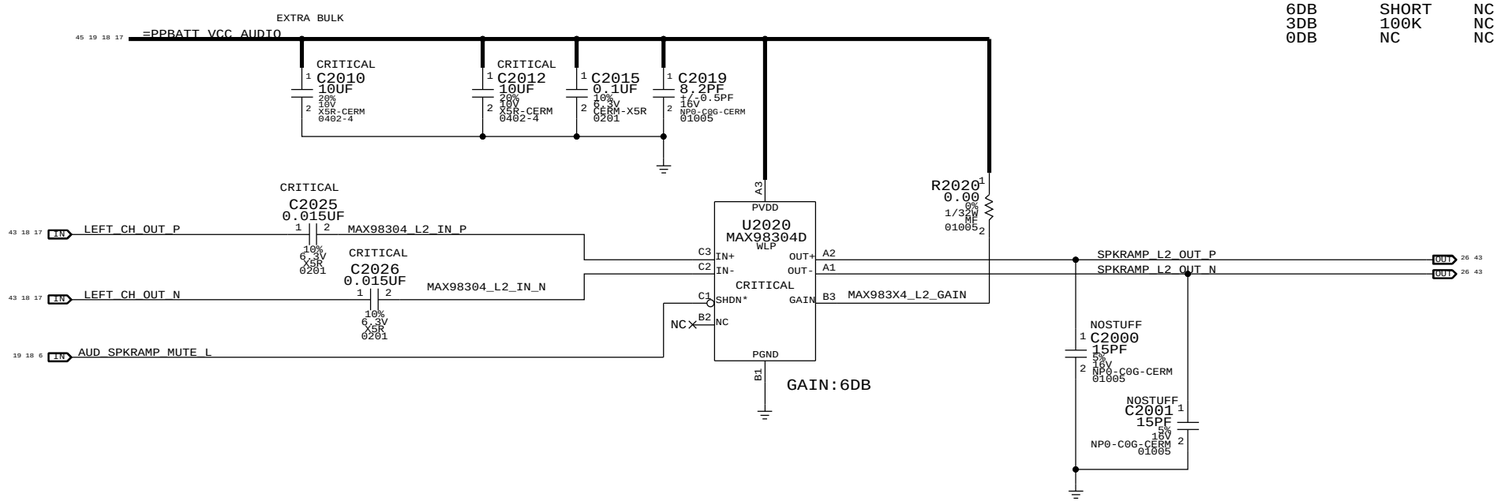
SPEAKER AMPLIFIER

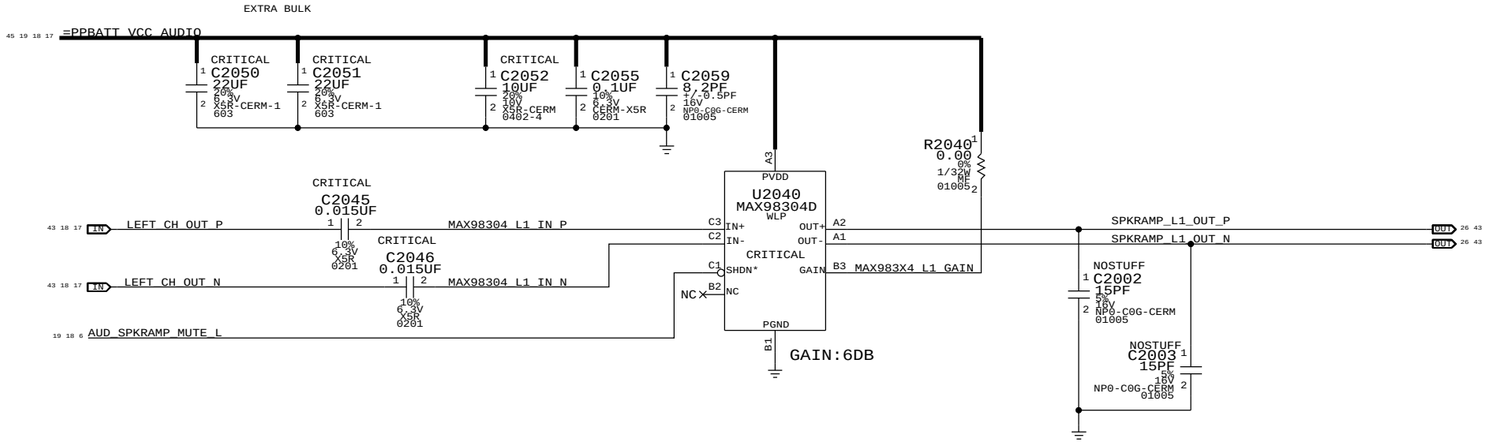
APN:353S3445

TURN ON TIME: 3.5MS

75HZ +/- XXX% TURN ON DELAY: ?MS

GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC



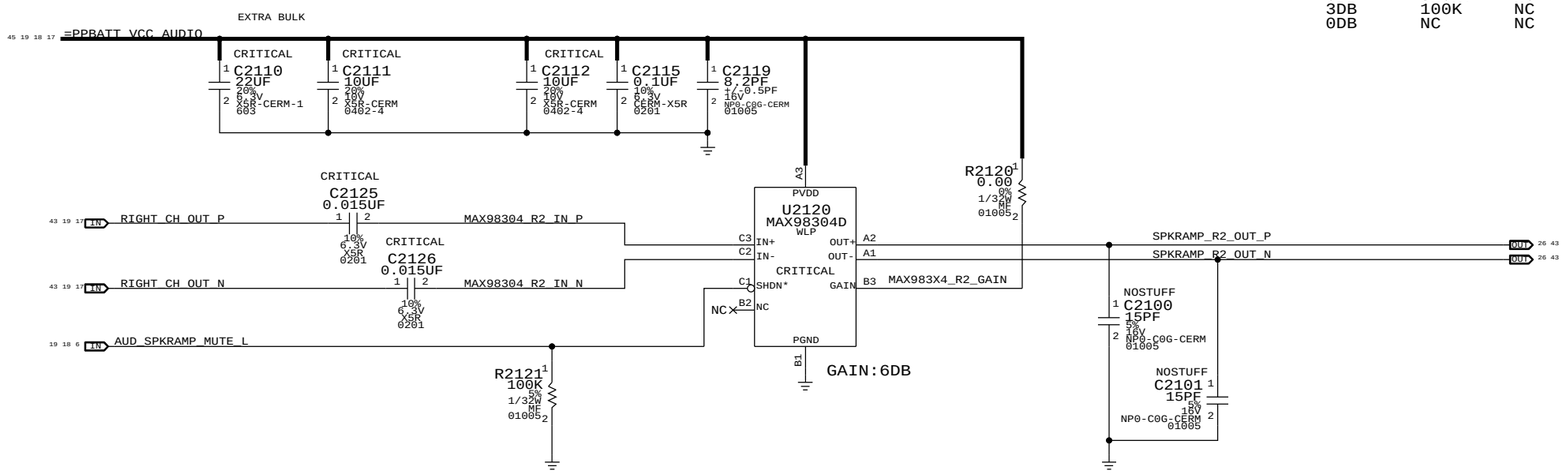


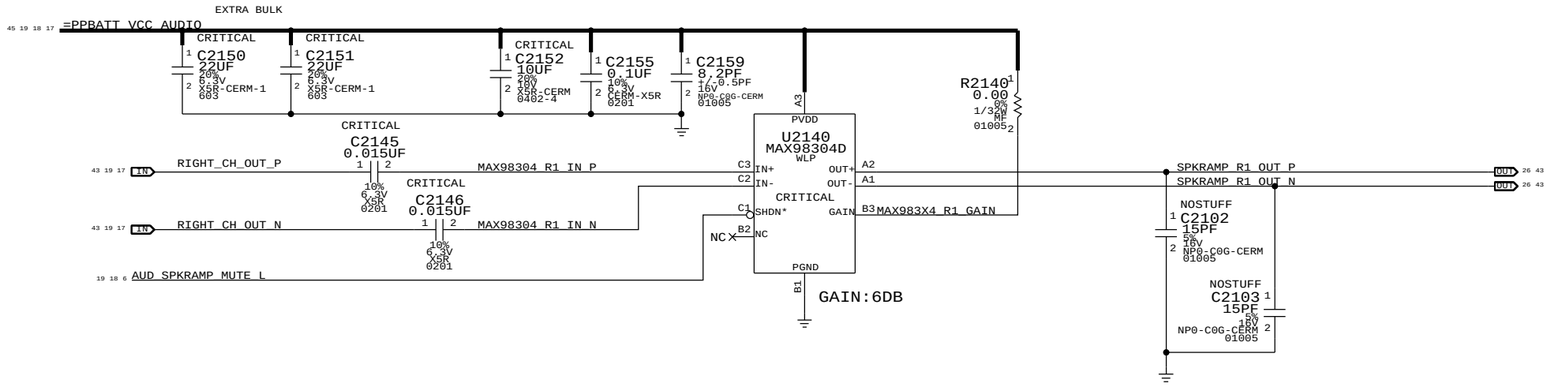
SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

SPEAKER AMPLIFIER

APN:353S3445
TURN ON TIME: 3.5MS
75HZ +/- XXX% TURN ON DELAY: ?MS

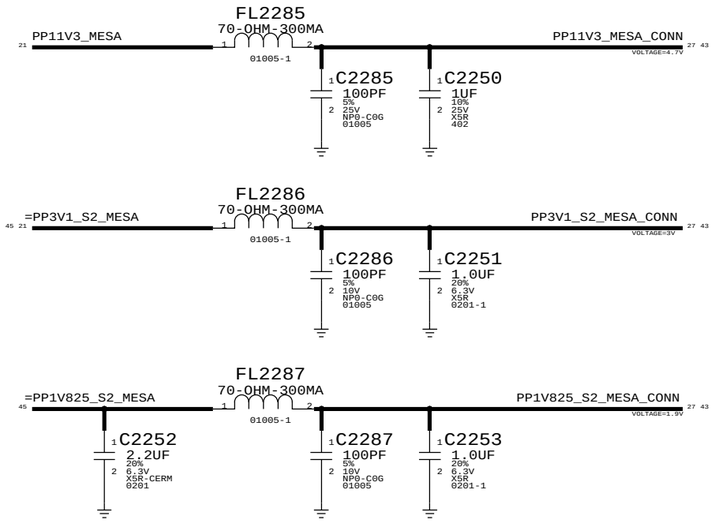
GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC

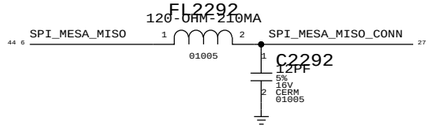


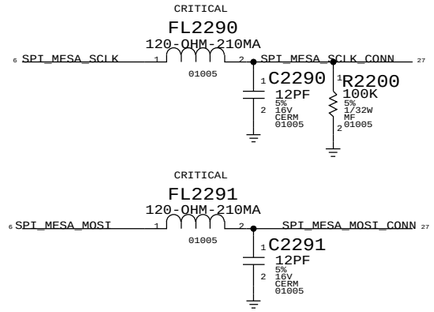


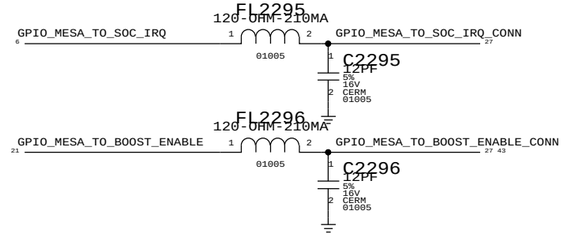
SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

MESA SUPPORT







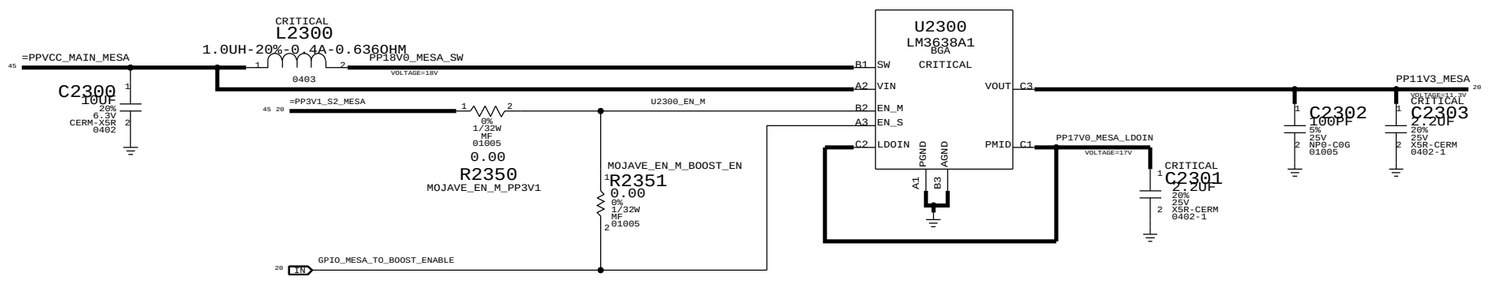


SYNC_MASTER=MLB_B

SYNC_DATE=07/26/2016

MOJAVE (BOOST)

APN: 353S4207
VENDOR: TI

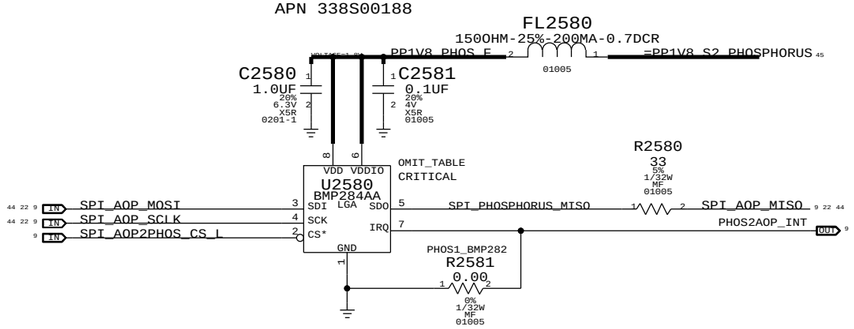


SYNC_MASTER=MLB_B

SYNC_DATE=07/26/2016

PHOSPHORUS

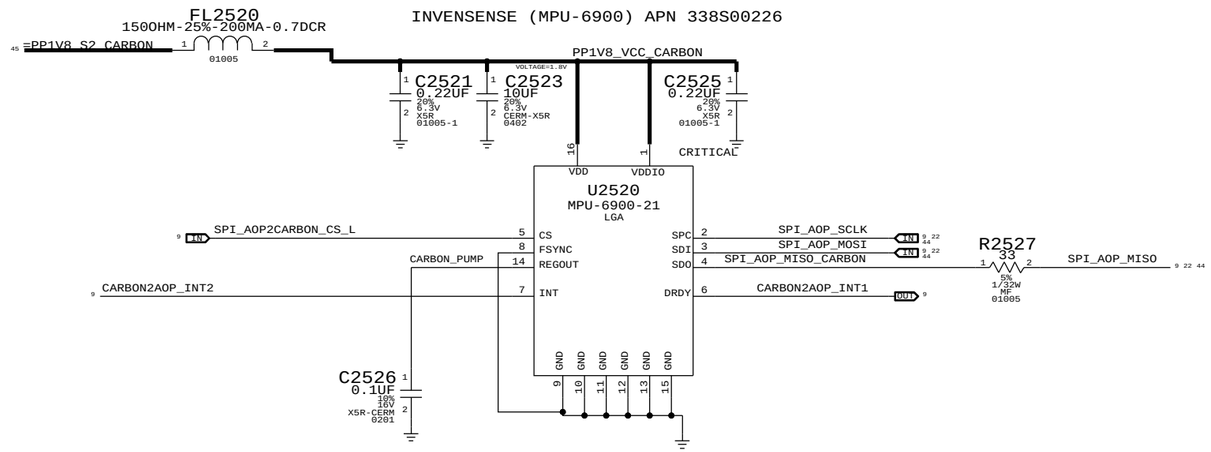
APN 338S00188



CARBON

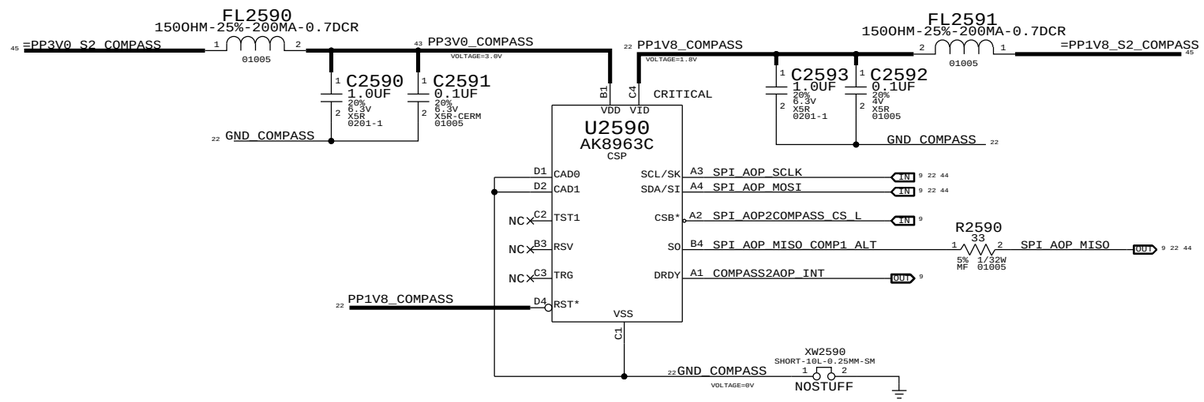
(ACCEL-GYRO COMBO)

INVENSENSE (MPU-6900) APN 338S00226



COMPASS

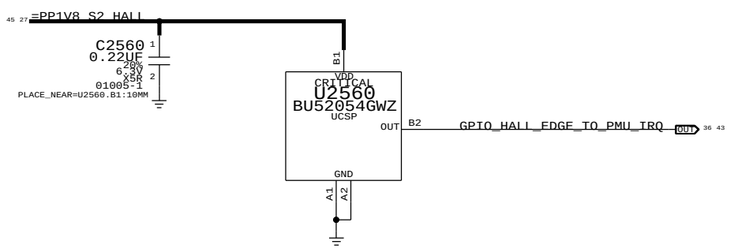
APN 338S1014 - AKM



HALL EFFECT

BIPOLAR ONE OUTPUT APN 353S3687

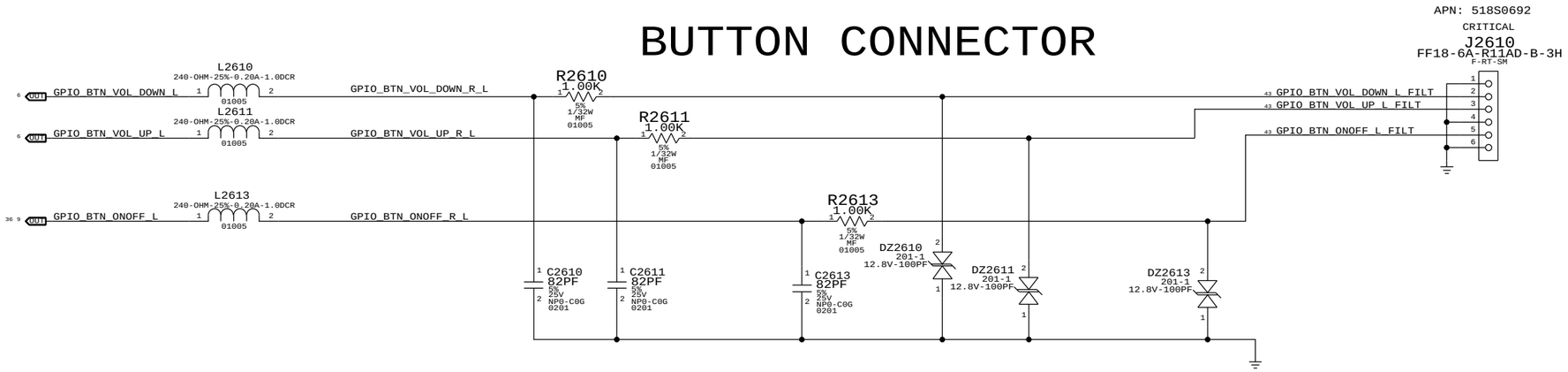
C-PANEL HALL EFFECT SENSOR
(B-PANEL HALL EFFECT SENSOR ON HB)



SYNC_MASTER=MLB_B

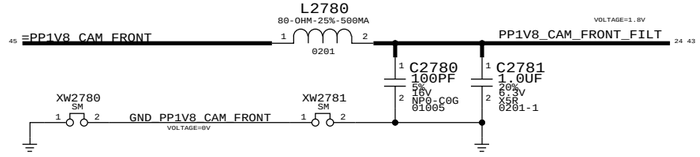
SYNC_DATE=07/26/2016

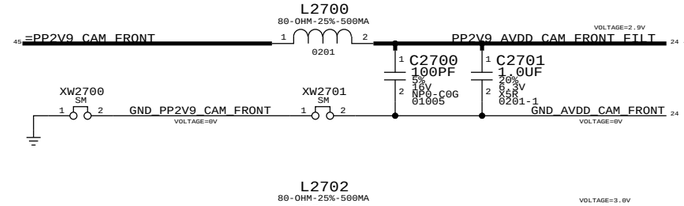
BUTTON CONNECTOR

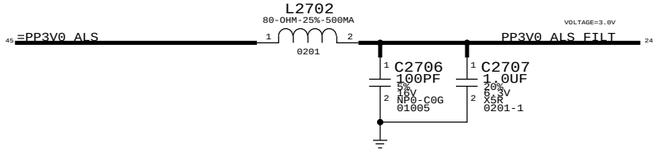


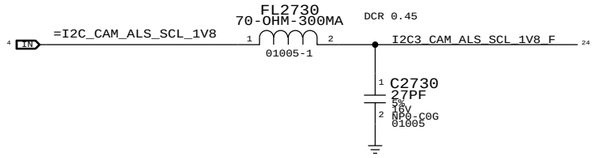
SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

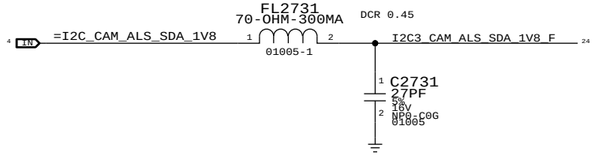
FRONT CAMERA CONNECTOR

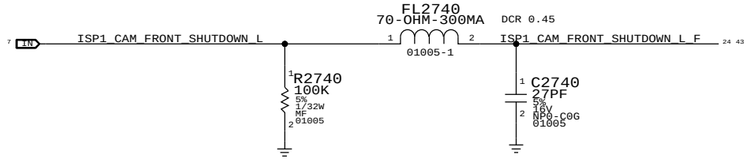


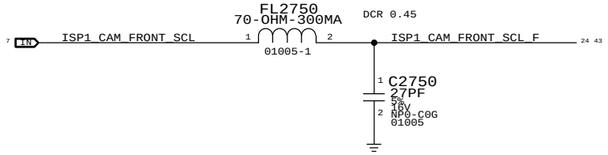


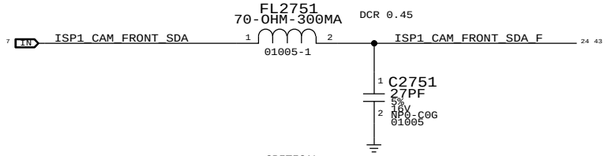


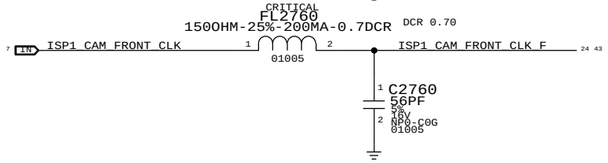






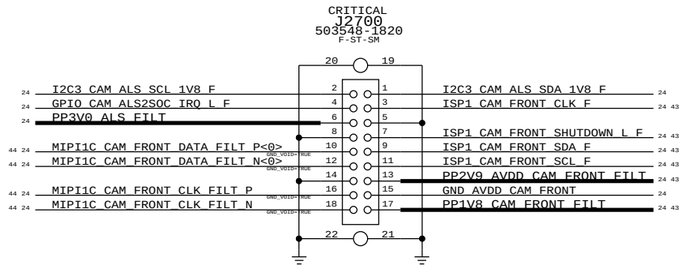


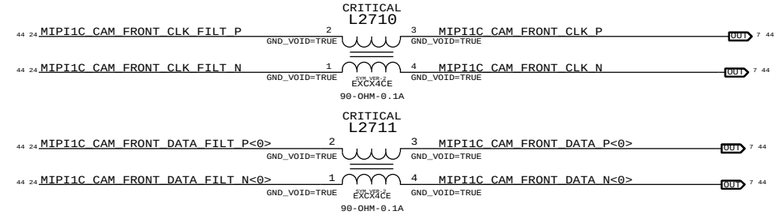




J65 CAMERA CONNECTOR

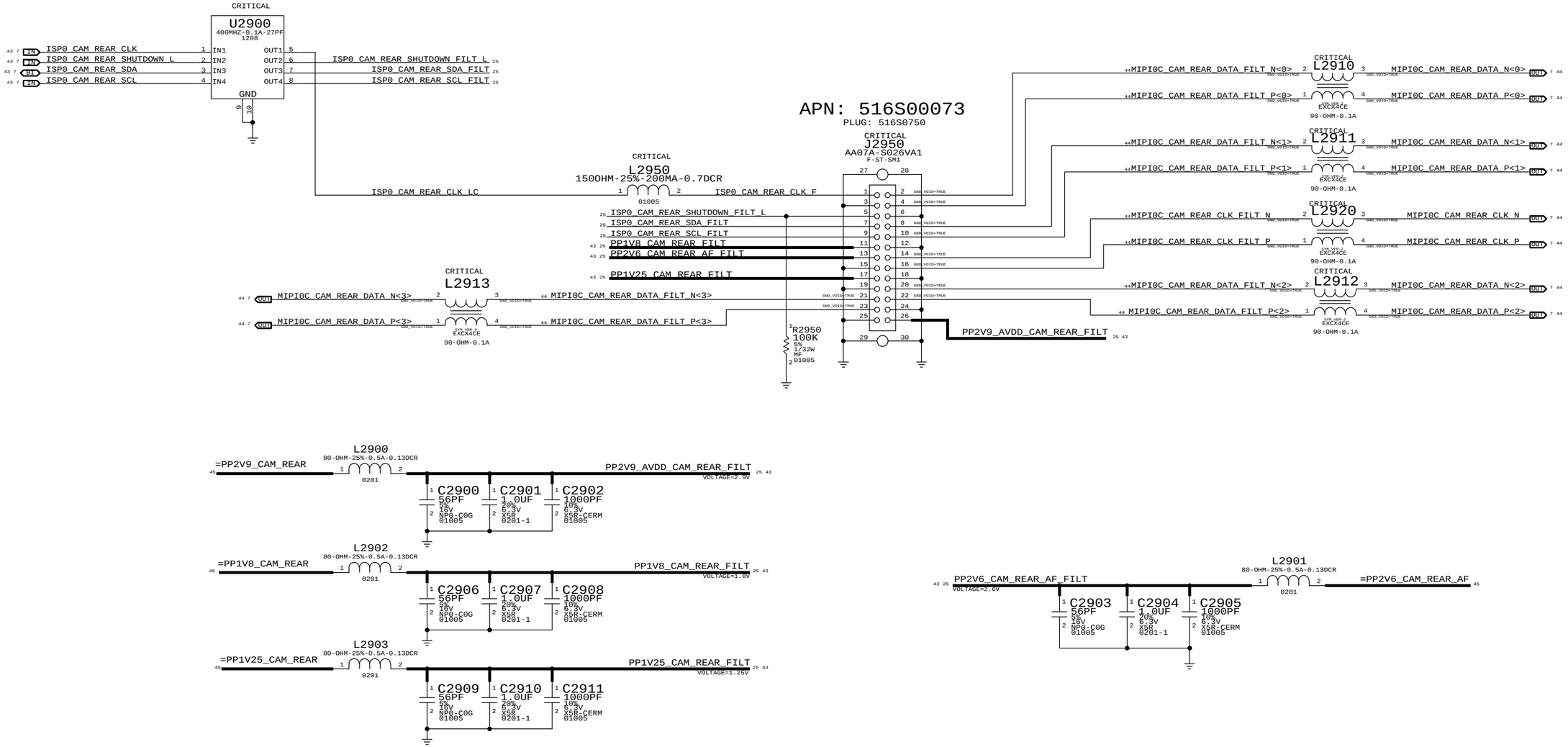
APN:MLB 516S0876
APN:FLEX 516S0869





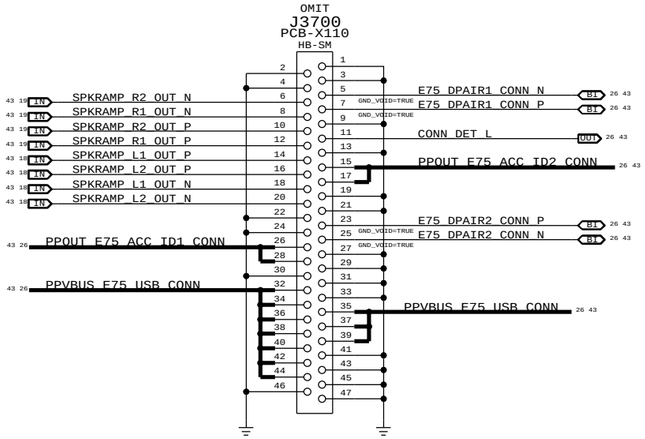
SYNC_MASTER=MLB_B
SYNC_DATE=07/26/2016

REAR CAMERA CONNECTOR

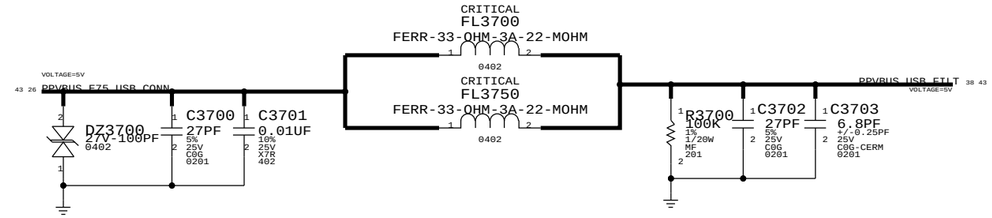


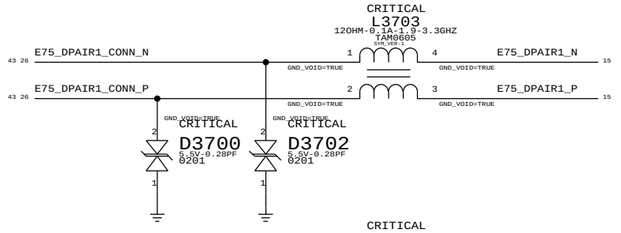
IO FLEX HOTBAR PADS

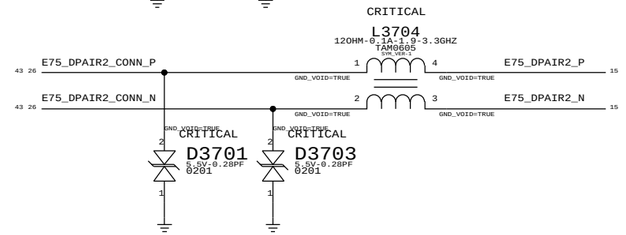
MLB 998-5877
FLEX 998-5876

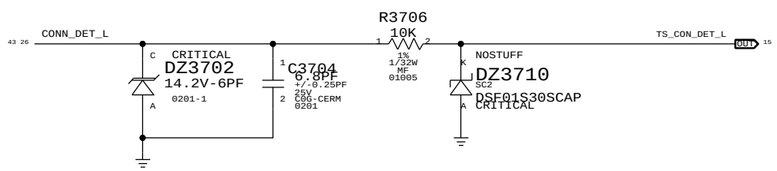


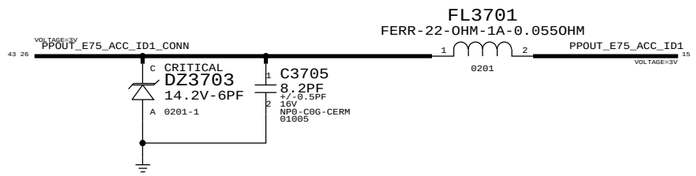
PINOUT MATCHES IO_FLEX 4.2.0 3/12/13

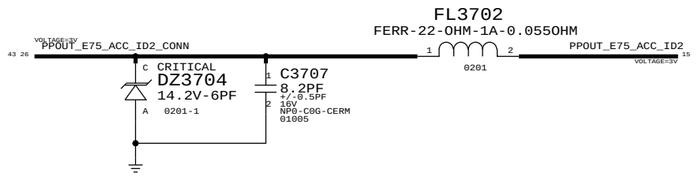






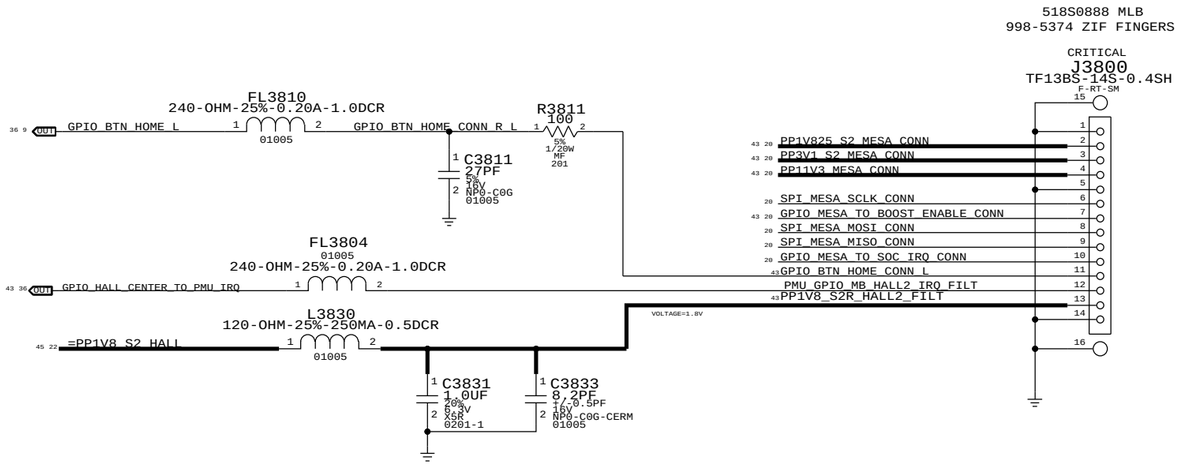






SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

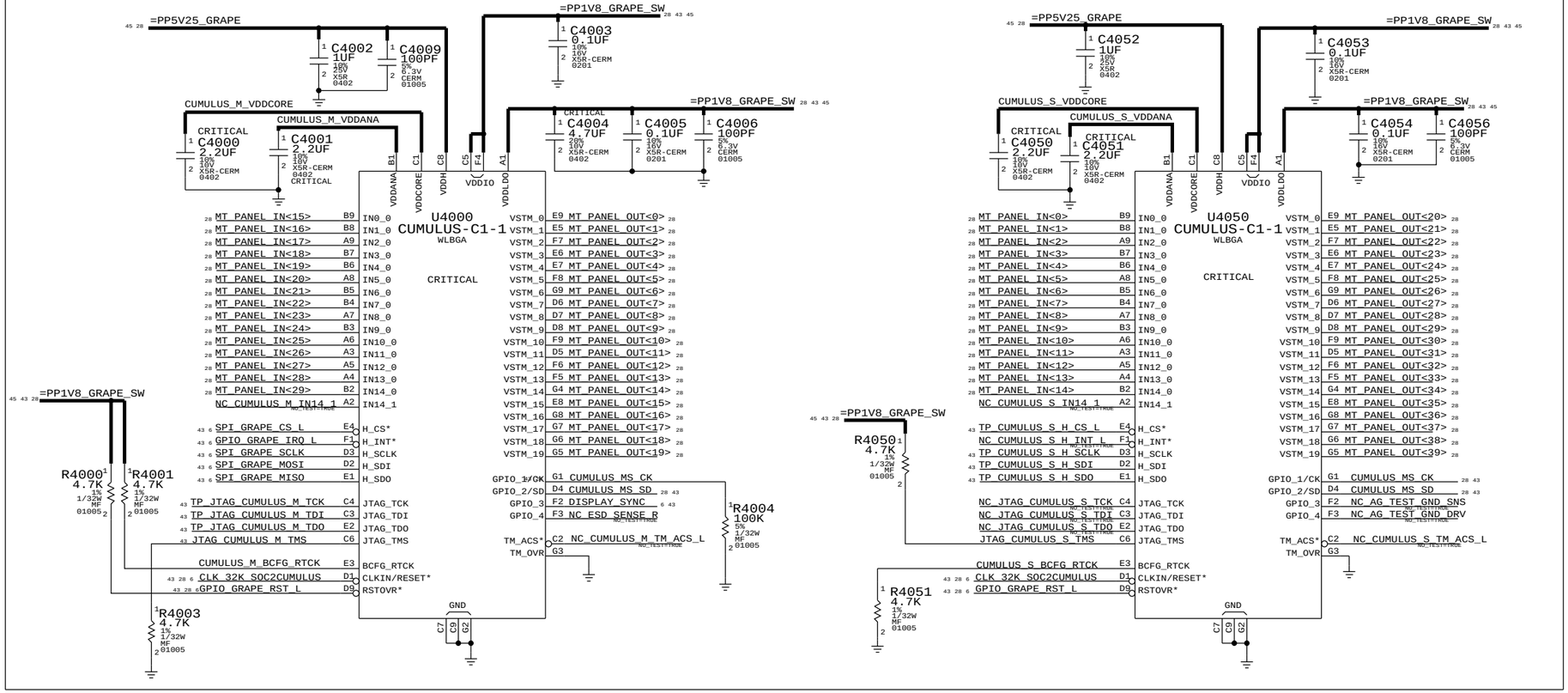
HALL-SENSOR-HOME-BUTTON-MESA FLEX CONN



SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

CUMULUS C1 (CSP) IN MASTER-SLAVE CONFIG

MASTER CUMULUS



SLAVE CUMULUS

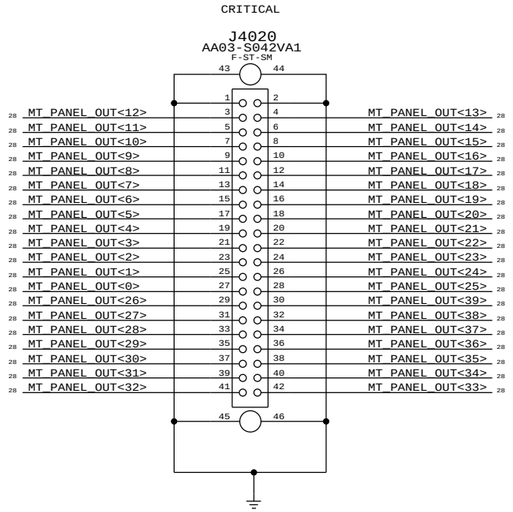
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0641	138S0700			RDAR://PROBLEM/13183483

C4000,C4001,C4050,C4051

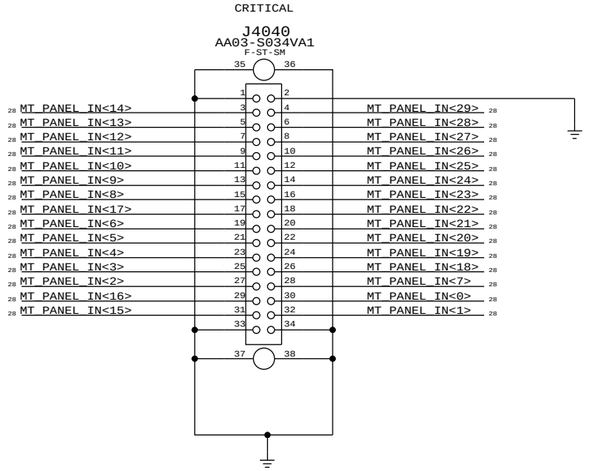
DIGITAL TESTPOINTS

GPIO_GRAPE_IRQ_L	TP_JTAG_CUMULUS_M_TCK
GPIO_GRAPE_RST_L	TP_JTAG_CUMULUS_M_TDI
CLK_32K_SOC2CUMULUS	JTAG_CUMULUS_M_TMS
SPI1_GRAPE_MOSI	TP_JTAG_CUMULUS_M_TDO
SPI1_GRAPE_MISO	DISPLAY_SYNC
SPI1_GRAPE_SCLK	CUMULUS_MS_CK
SPI1_GRAPE_CS_L	CUMULUS_MS_SD
TP_CUMULUS_S_H_CS_L	TP_CUMULUS_S_H_SDI
TP_CUMULUS_S_H_SCLK	TP_CUMULUS_S_H_SDO

PINOUT MATCHES GRAPE_FLEX_DRIVE_ALT 0.1.0 1/8/13

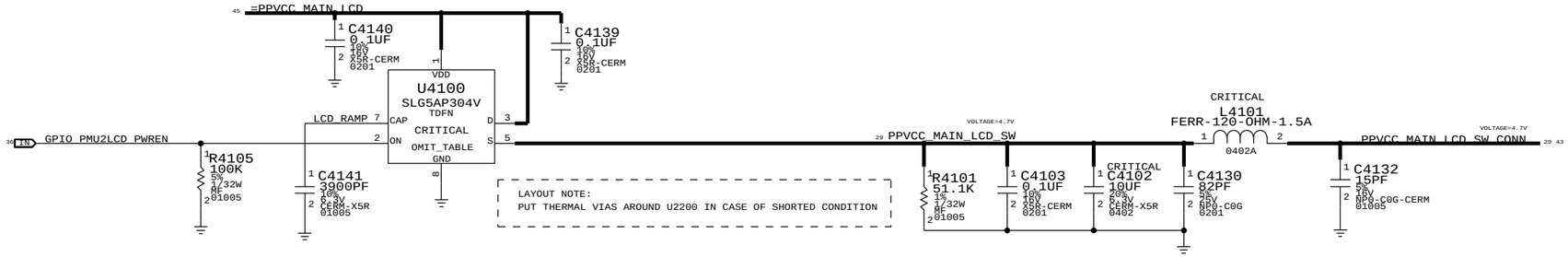


PINOUT MATCHES GRAPE_FLEX_SENSE_ALT 0.1.0 1/8/13

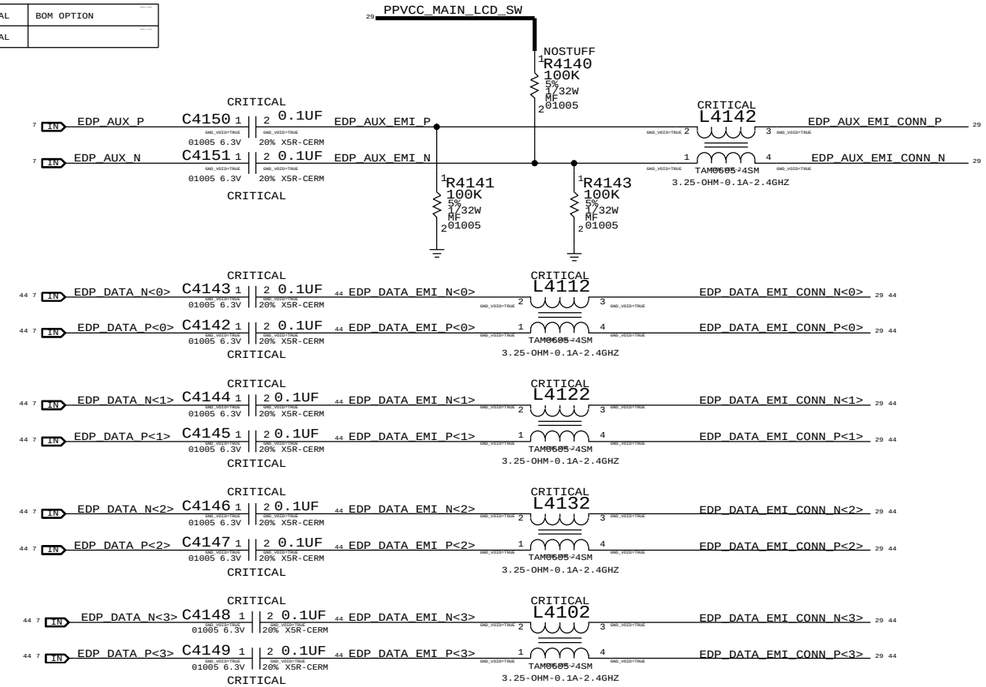


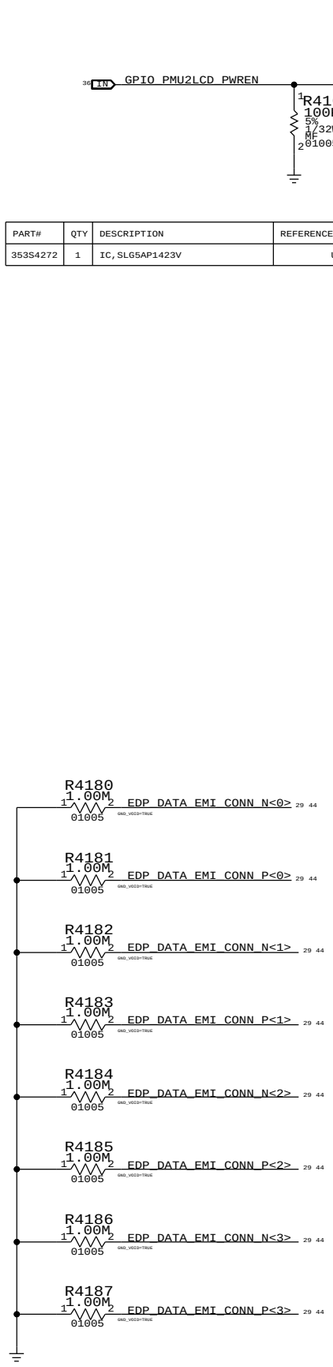
SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

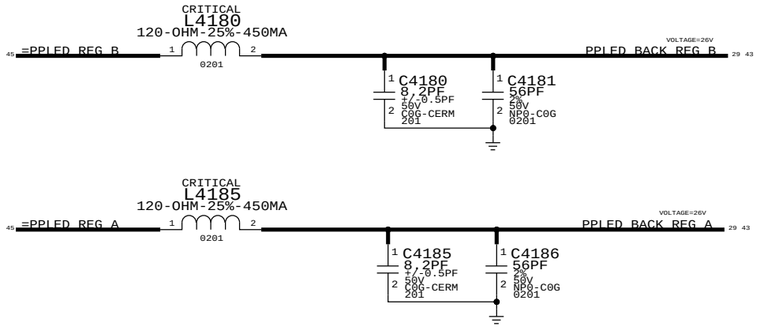
EDP CONNECTOR SUPPORT

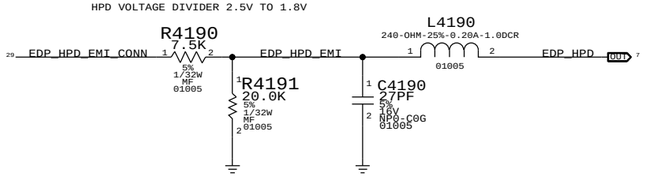


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4272	1	IC,SLG5AP1423V	U4100	CRITICAL	



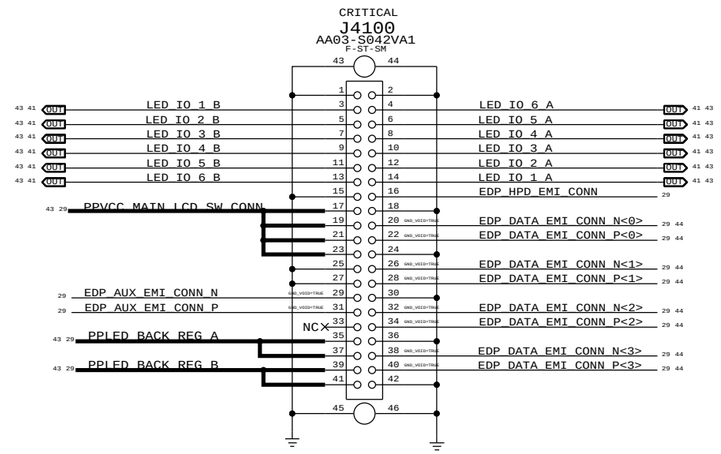






EDP CONNECTOR

PINOUT MATCHES DISPLAY_EDP_FLEX 1.0.0 1/7/13



SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

BB

6 GPIO_SOC2BB_RADIO_ON_L — NC_RADIO_ON_L
6 GPIO_SOC2BB_RST_L — NC_BB_RST_L
6 GPIO_SOC2BB_WAKE_MODEM — NC_AP_WAKE_MODEM
6 GPIO_SOC2BB_COREDUMP — NC_BB_CORE_DUMP
6 HSIC1_SOC2BB_HOST_RDY — NC_BB_HOST_RDY

6 BB_IPC_GPIO — NC_BB_IPC_GPIO
6 HSIC1_BB2SOC_DEVICE_RDY — NC_BB_DEVICE_RDY

6 GPIO_BB2SOC_GPS_SYNC — NC_BB_GPS_SYNC
6 GPIO_BB2SOC_RESET_DET_L — NC_BB_RESET_DET_L

RESET_PMU_TO_SYSTEM_L = RESET_1V8_L

6 UART_SOC2BB_RTS_L — NC_BB_UART_CTS_L
6 UART_BB2SOC_RTS_L — NC_BB_UART_RTS_L
6 UART_SOC2BB_TX — NC_BB_UART_RXD
6 UART_BB2SOC_TX — NC_BB_UART_TXD

5 HSIC1_BB_DATA — NC_50_BB_HSIC_DATA
5 HSIC1_BB_STB — NC_50_BB_HSIC_STROBE

15 USB_BB_P — NC_90_BB_USB_P
15 USB_BB_N — NC_90_BB_USB_N

PMU_GPIO_PMU2BBPMU_RST_L = RF_PMIC_RESET_L

36 PMU_GPIO_BB2PMU_HOST_WAKE — NC_BB_WAKE_HOST
36 PMU_GPIO_BB_VBUS_DET — NC_BB_USB_VBUS

9 UART_AOP2BB_TXD — NC_BB_OTHER_RXD
9 UART_BB2AOP_RXD — NC_BB_OTHER_TXD

NC_BB2SOC_GSM_BURST = GPIO_BB_TO_STROBE_GSM_BURST_IND

6 GPIO_SOC2BB_MESA_ON — NC_AP_TO_BB_MESA_ON

6 BB_JTAG_TCK — NC_BB_JTAG_TCK
6 BB_JTAG_TMS — NC_BB_JTAG_TMS

=PPBATT_VCC_BB = PP_BATT_VCC

36 PA_NTC_P — NC_BB_NTC

WLAN

45 32 30 =PPVCC_MAIN_WLAN — =PPVCC_MAIN_WLAN 30 32 45
45 =PP3V3_S2_WIFI — =PP_3V3_S2_WIFI 32
45 =PP1V8_S2_WIFI — =PP_1V8_S2R_VDDIO_WLAN_BT 32

36 PMU_GPIO_WLAN_REG_ON — GPIO_PMU2WLAN_REG_ON 32 43
36 PMU_GPIO_WLAN_HOST_WAKE — GPIO_WLAN2PMU_HOST_WAKE 32 43
43 32 30 6 GPIO_SOC2WLAN_PCIE_DEV_WAKE — GPIO_SOC2WLAN_PCIE_DEV_WAKE 6 30 32 43
36 PMU_GPIO_CLK_32K_WLAN — CLK_PMU2WLAN_32K 32 43

NC_UART_BB2WLAN_COEX_RX — UART_BB2WLAN_COEX_TX (IN) 32
NC_UART_WLAN2BB_COEX_TX — UART_WLAN2BB_COEX_TX (OUT) 32
43 9 AOP2RADIO_CONTEXT_A — CONTEXTA_JTAG_TDI (OUT) 32
43 9 AOP2RADIO_CONTEXT_B — CONTEXTB_JTAG_TDO (OUT) 32

43 6 UART2_SOC2WLAN_TX — UART_SOC2WLAN_TX 32
43 6 UART2_SOC2WLAN_RTS_L — UART_SOC2WLAN_RTS_L 32
43 6 UART2_WLAN2SOC_TX — UART_WLAN2SOC_TX 32
43 6 UART2_WLAN2SOC_RTS_L — UART_WLAN2SOC_RTS_L 32

CKPLUS_WAIVE=SINGLE_NODENET
FUNC_TEST=TRUE
53 TESTPOINT_JTAG_WLAN_TCK — JTAG_WLAN_TCK 32
49 TP_JTAG_WLAN_TMS — JTAG_WLAN_TMS 32
49 TP_JTAG_WLAN_TRST — JTAG_WLAN_TRST 32

44 8 PCIE1_SOC2WLAN_REFCLK_P — PCIE_SOC2WLAN_CLK_P 32
44 8 PCIE1_SOC2WLAN_REFCLK_N — PCIE_SOC2WLAN_CLK_N 32
43 8 PCIE1_SOC2WLAN_TX_P — PCIE_SOC2WLAN_TX_P 32
43 8 PCIE1_SOC2WLAN_TX_N — PCIE_SOC2WLAN_TX_N 32
30 PCIE_WLAN2SOC_TX_C_P — PCIE_WLAN2SOC_TX_P 32
30 PCIE_WLAN2SOC_TX_C_N — PCIE_WLAN2SOC_TX_N 32
43 8 PCIE1_WLAN2SOC_CLKREQ_L — PCIE_WLAN2SOC_CLKREQ_L 32
43 8 PCIE1_SOC2WLAN_RST_L — PCIE_SOC2WLAN_PERST_L 32

36 PMU_GPIO_BT_HOST_WAKE — GPIO_BT2PMU_HOST_WAKE 32 43
36 PMU_GPIO_BT_REG_ON — GPIO_PMU2BT_REG_ON 32 43
43 32 30 6 GPIO_SOC2BT_WAKE — GPIO_SOC2BT_WAKE 6 30 32 43

43 32 30 6 UART_SOC2BT_TX — UART_SOC2BT_TX 6 30 32 43
43 32 30 6 UART_SOC2BT_RTS_L — UART_SOC2BT_RTS_L 6 30 32 43
43 32 30 6 UART_BT2SOC_TX — UART_BT2SOC_TX 6 30 32 43
43 32 30 6 UART_BT2SOC_RTS_L — UART_BT2SOC_RTS_L 6 30 32 43

NC_BT_EXT_CLK — BT_EXT_CLK (OUT) 32
NC_BT_EXT_SYNC — BT_EXT_SYNC (OUT) 32

43 8 PCIE1_WLAN2SOC_RX_P — C9160 0.1UF 20% X5R-CERM 6.3V 01005 — PCIE_WLAN2SOC_TX_C_P 30
43 8 PCIE1_WLAN2SOC_RX_N — C9161 0.1UF 20% X5R-CERM 6.3V 01005 — PCIE_WLAN2SOC_TX_C_N 30

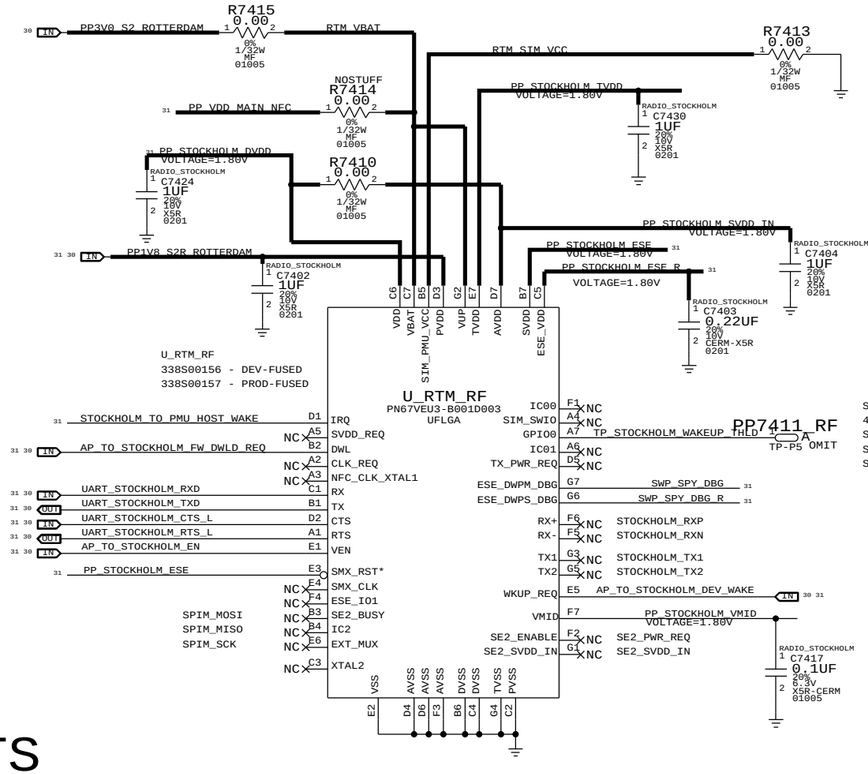
ROTTERDAM

45 43 34 PP3V3_S2 — PP3V0_S2_ROTTERDAM 31
49 =PP1V8_S2_ROTTERDAM — PP1V8_S2R_ROTTERDAM 31

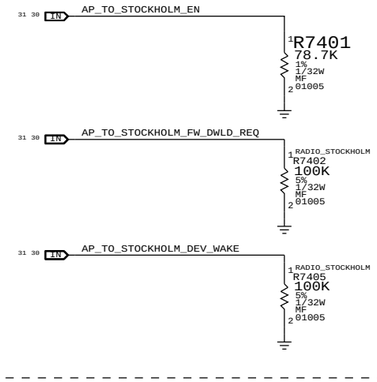
6 GPIO_SOC_TO_ROTTERDAM_EN — AP_TO_STOCKHOLM_EN 31
6 UART_ROTTERDAM_TO_SOC_RTS_L — UART_STOCKHOLM_RTS_L 31
6 UART_SOC_TO_ROTTERDAM_RTS_L — UART_STOCKHOLM_CTS_L 31
6 UART_ROTTERDAM_TO_SOC_TX — UART_STOCKHOLM_TXD 31
6 UART_SOC_TO_ROTTERDAM_TX — UART_STOCKHOLM_RXD 31
6 GPIO_SOC_TO_ROTTERDAM_DWLD_REQ — AP_TO_STOCKHOLM_FW_DWLD_REQ 31
6 GPIO_SOC_TO_ROTTERDAM_DEV_WAKE — AP_TO_STOCKHOLM_DEV_WAKE 31

SYNC_MASTER=N/A SYNC_DATE=04/11/2011

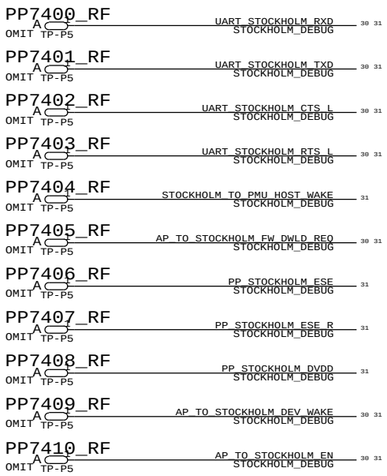
RTM/SECURE ELEMENT



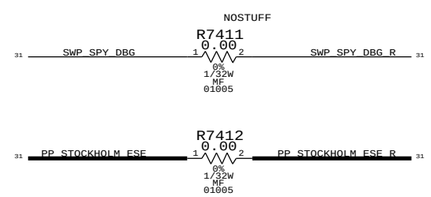
SUPPORT PULLS



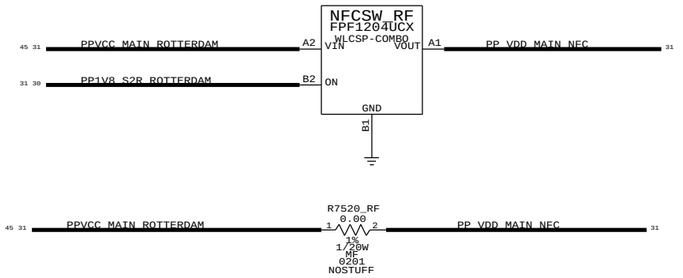
TEST POINTS



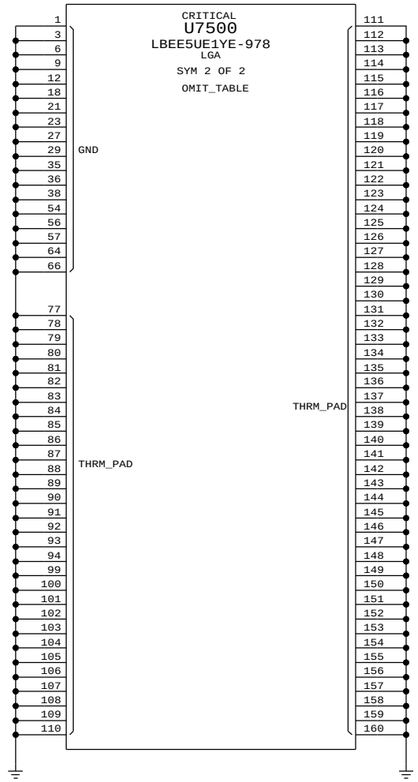
IMPORTANT DEBUG FEATURES

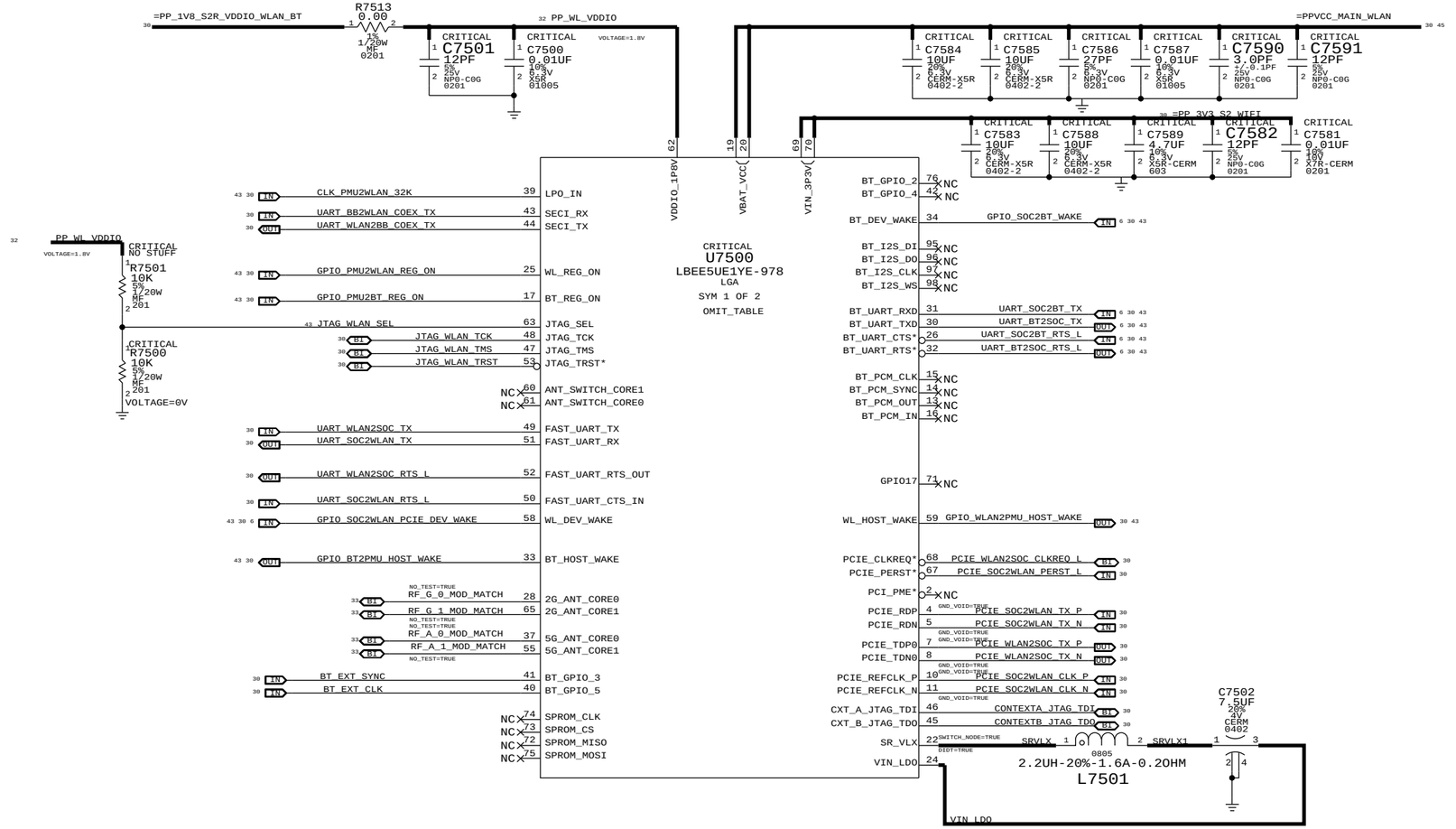


NFC LOAD SWITCH



WIFI/BT: J71S/72S: YEBISU MODULE, POWER, I/O





MODULE: USI ALTERNATES FOR MUR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00246	339S00248		U7500	USI ALT FOR MUR
339S00247	339S00249		U7500	CIDRE USI ALT FOR MUR

MODULE: BOM OPTION FOR CIDRE IN MLB_A, NOT IN MLB_B

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00248	1	YEBISU MURATA ES2	U7500	CRITICAL	MLB_B
339S00249	1	YEBISU CIDRE MURATA ES2	U7500	CRITICAL	MLB_A

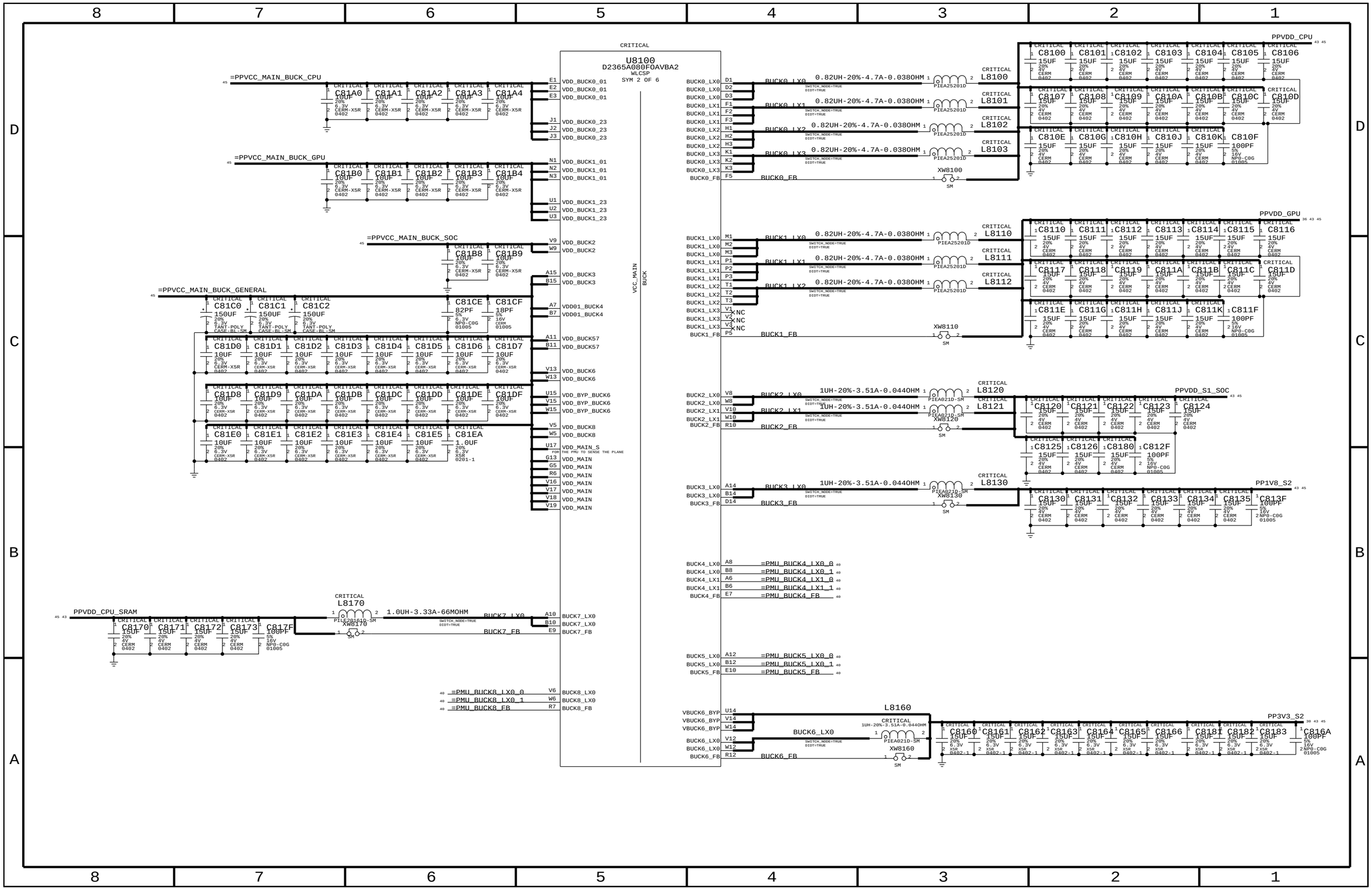
LAST UPDATED: 05/09/2016

SYNC_MASTER=J71S_WIFI_MLB SYNC_DATE=08/15/2016

WIFI/BT: J71S (WIFI/BT ONLY) RF FRONT END

LAST UPDATED: 08/12/2016

SYNC_MASTER=J71S_WIFI_MLB SYNC_DATE=08/15/2016


U8100
D2365A080F0AVBA2
WLCSP
SYM 2 OF 6
VCC_MAIN BUCK
=PPVCC_MAIN_BUCK_CPU
=PPVCC_MAIN_BUCK_GPU
=PPVCC_MAIN_BUCK_SOC
=PPVCC_MAIN_BUCK_GENERAL
PPVDD_CPU_SRAM
PPVDD_CPU
PPVDD_GPU
PPVDD_S1_SOC
PP1V8_S2
PP3V3_S2
0.82UH-20%-4.7A-0.038OHM
1UH-20%-3.51A-0.044OHM
1.0UH-3.33A-66MOHM
PIEA25201D
PIEA021D-SM
PILC20101D-SM
XW8100
XW8110
XW8120
XW8130
XW8160
XW8170
SM
SWITCH_NODE=TRUE
DIDT=TRUE
FOR THE PMU TO SENSE THE PLANE
CRITICAL
=PMU_BUCK4_LX0_0
=PMU_BUCK4_LX0_1
=PMU_BUCK4_LX1_0
=PMU_BUCK4_LX1_1
=PMU_BUCK4_FB
=PMU_BUCK5_LX0_0
=PMU_BUCK5_LX0_1
=PMU_BUCK5_FB
=PMU_BUCK8_LX0_0
=PMU_BUCK8_LX0_1
=PMU_BUCK8_FB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0703	138S0648		C8233	AND 7 MORE REFDES

CRITICAL

U8100
D2365A080FOAVBA2
WLCSP
SYM 6 OF 6

C1	VSS(VSS_BUCK0_0)	VSS	M19
C2	VSS(VSS_BUCK0_0)	VSS	L5
C3	VSS(VSS_BUCK0_0)	VSS	E11
G1	VSS(VSS_BUCK0_12)	VSS	E12
G2	VSS(VSS_BUCK0_12)	VSS	E6
G3	VSS(VSS_BUCK0_12)	VSS	F10
L1	VSS(VSS_BUCK01)	VSS	F11
L2	VSS(VSS_BUCK01)	VSS	F12
L3	VSS(VSS_BUCK01)	VSS	G16
R1	VSS(VSS_BUCK1_12)	VSS	G18
R2	VSS(VSS_BUCK1_12)	VSS	H13
R3	VSS(VSS_BUCK1_12)	VSS	H14
W1	VSS(VSS_BUCK1_3)	VSS	H18
W2	VSS(VSS_BUCK1_3)	VSS	P19
W3	VSS(VSS_BUCK1_3)	VSS	J11
V11	VSS(VSS0_BUCK26)	VSS	J12
W11	VSS(VSS0_BUCK26)	VSS	J14
V7	VSS(VSS_BUCK28)	VSS	J19
W7	VSS(VSS_BUCK28)	VSS	K11
A13	VSS(VSS0_BUCK35)	VSS	K12
B13	VSS(VSS0_BUCK35)	VSS	K13
A9	VSS(VSS0_BUCK47)	VSS	K14
B9	VSS(VSS0_BUCK47)	VSS	K15
A5	VSS(VSS1_BUCK4)	VSS	L11
B5	VSS(VSS1_BUCK4)	VSS	L14
B16	VSS_LCM_SW	VSS	L15
		VSS	M11
		VSS	M14
		VSS	M15
		VSS	N10
		VSS	N11
		VSS	N14
		VSS	P10
		VSS	P11
		VSS	R8
		VSS	U19
		VSS	V4
		VSS	W4
		VSS	L4
		VSS	C17
C10	VSS_NC		
C11	VSS_NC		
C12	VSS_NC		
C13	VSS_NC	VSS_NC	M4
C5	VSS_NC	VSS_NC	N16
C6	VSS_NC	VSS_NC	N4
C7	VSS_NC		
C8	VSS_NC	VSS_NC	P4
C9	VSS_NC	VSS_NC	R4
D10	VSS_NC	VSS_NC	T4
D11	VSS_NC	VSS_NC	U10
D12	VSS_NC	VSS_NC	U11
C14	VSS_NC	VSS_NC	U12
D4	VSS_NC	VSS_NC	U13
F4	VSS_NC	VSS_NC	U4
G4	VSS_NC	VSS_NC	U5
H4	VSS_NC	VSS_NC	U6
J4	VSS_NC	VSS_NC	U7
K4	VSS_NC	VSS_NC	U8
		VSS_NC	U9

VOLTAGE=0V

CRITICAL

U8100
D2365A080FOAVBA2
WLCSP
SYM 3 OF 6

LDO INPUT

LDO OUTPUT

SWITCHED INPUT

SWITCHED OUTPUT

LDO INPUTS

=PPVCC_MAIN_INTERNAL_LDOS

45 =PP1V8_S2_INTERNAL_LDOS

C8290 1UF 10% 6.3V CERM 402 (1)(2)
C8291 1UF 10% 6.3V CERM2 402 (1)(2)

E14 VDD_LDO1
E13 VDD_LDO2
D18 VDD_LDO34
F18 VDD_LDO5
J18 VDD_LDO6
J15 VDD_LDO7
G14 VDD_LDO8
F16 VDD_LDO9
B18 VDD_LDO10
B19 VDD_LDO10
F17 VDD_LDO11
J16 VDD_LDO13
D19 VDD_LDO14
F19 VDD_LDO15
F14 VDD_LDO16

45 =PP1V1_S2_INTERNAL_LDOS

C8292 1UF 10% 6.3V CERM 402 (1)(2)

45 =PP1V8_S2_INTERNAL_SW

C8293 1.0UF 20% 6.3V X5R 0201-1 (1)(2)
C8295 1.0UF 20% 6.3V X5R2 0201-1 (1)(2)

A2 VBUCK3
A3 VBUCK3

45 =PP1V1_S2_INTERNAL_SW

C8294 1.0UF 20% 6.3V X5R 0201-1 (1)(2)

B4 VBUCK4

PMU_VPUMP

C8299 0.1UF 10% 6.3V X5R2 0201 (1)(2)

B1 VPUMP
B2 VPUMP

LDO OUTPUTS

VLDO1 E15 (650MA; 2.5-3.3V) PP3V0_S2_TRISTAR 43 45
VLDO2 F13 (100MA; 1.7-3.6V) 43 45

CRITICAL C8204 10UF 20% 6.3V CERM-X5R 0402-9 (1)(2)
CRITICAL C8200 2.2UF 10% 6.3V X5R 402 (1)(2)

PP1V7_VA_VCP
ACTIVE - BYPASS MODE (1.8V)
HIBERNATE - LDO MODE (1.7V)

(50MA; 2.5-3.3V) VLDO3 C18 XNC
VLDO4 D17 (50MA; 2.5-3.3V) PP3V0_ALS 43 45

CRITICAL C8212 2.2UF 10% 6.3V X5R 402 (1)(2)

(1000MA; 2.5-3.6V) VLDO5 E18 XNC
VLDO6 J17 (1000MA; 2.5-3.6V) PP3V3_ACC 43 45

CRITICAL C8220 10UF 20% 6.3V CERM-X5R 0402 (1)(2)

VLDO7 H15 (300MA; 2.5-3.3V) PP3V0_S2_MISC 43 45
VLDO8 G15 (300MA; 2.5-3.3V) PP3V1_S2_MESA 45

CRITICAL C8228 10UF 20% 6.3V CERM-X5R 0402-9 (1)(2)
CRITICAL C8224 10UF 20% 6.3V CERM-X5R 0402-9 (1)(2)

VLDO9 E16 (200MA; 1.7-3.6V) PP1V25_REAR_CAM 45
VLDO10 A17 (1200MA; 1.7-3.6V) 43 45
VLDO10 A18
VLDO10 A19 PP0V9_NAND

CRITICAL C8236 10UF 20% 6.3V CERM-X5R 0402-9 (1)(2)
CRITICAL C8233 4.7UF 20% 6.3V X5R 402 (1)(2)
C8232 100PF 5% 16V NP0-C0G 01005 (1)(2)

VLDO11 E17 (200MA; 1.7-3.6V) PP2V6_CAM_AF 45
VLDO13 H16 (200MA; 1.7-3.6V) PP2V9_CAM 43 45

CRITICAL C8244 10UF 20% 6.3V CERM-X5R 0402-9 (1)(2)
CRITICAL C8240 10UF 20% 6.3V CERM-X5R 0402-9 (1)(2)

VLDO14 C19 (200MA; 0.9-1.6V) PP1V2_SOC 43 45
VLDO15 E19 (400MA; 0.9-1.6V) PP0V8_S2_SOC_AOP 43 45

CRITICAL C8252 1UF 20% 6.3V X5R 0201 (1)(2)
CRITICAL C8248 2.2UF 10% 6.3V X5R 402 (1)(2)

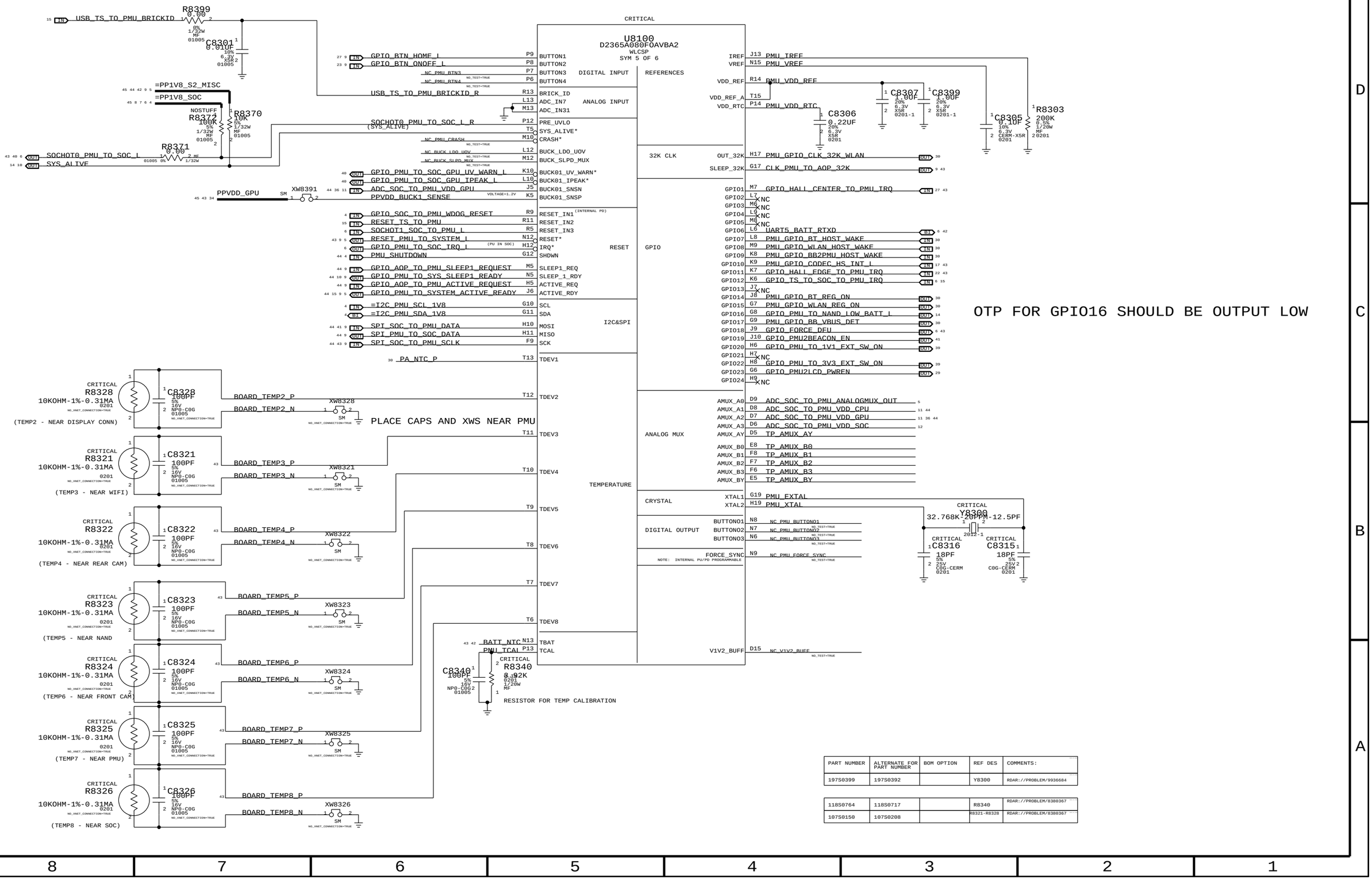
VLDO16 F15 (450MA; 1.7-3.6V) PP1V825_S2_MESA 45
ON_BUF R15 (450MA; 1.7-3.6V) PP1V8_ALWAYS 43 45

CRITICAL C8260 0.22UF 20% 6.3V X5R 0201 (1)(2)
CRITICAL C8256 4.7UF 20% 6.3V X5R 402 (1)(2)

BUCK3_SW1 A1
BUCK3_SW1 E4 PP1V8_SW1 43 45
BUCK3_SW2 A4 XNC
BUCK3_SW3 B3 PP1V8_S2_SW3 43 45

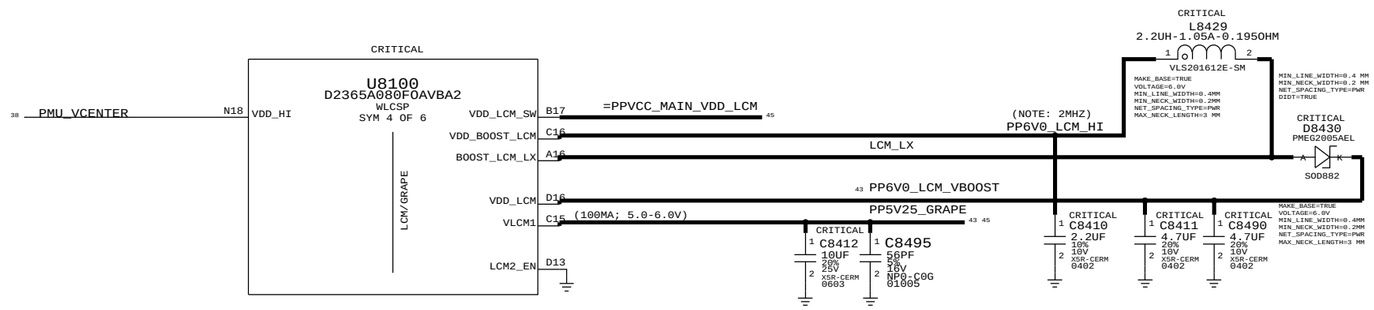
C8278 1.0UF 20% 6.3V X5R 0201-1 (1)(2)
C8270 1UF 10% 6.3V CERM 402 (1)(2)

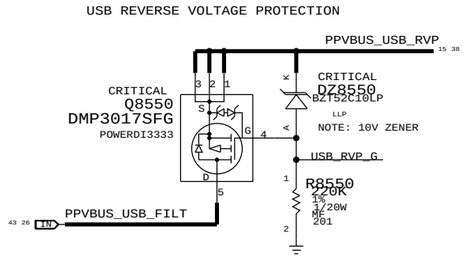
BUCK4_SW2 C4 XNC

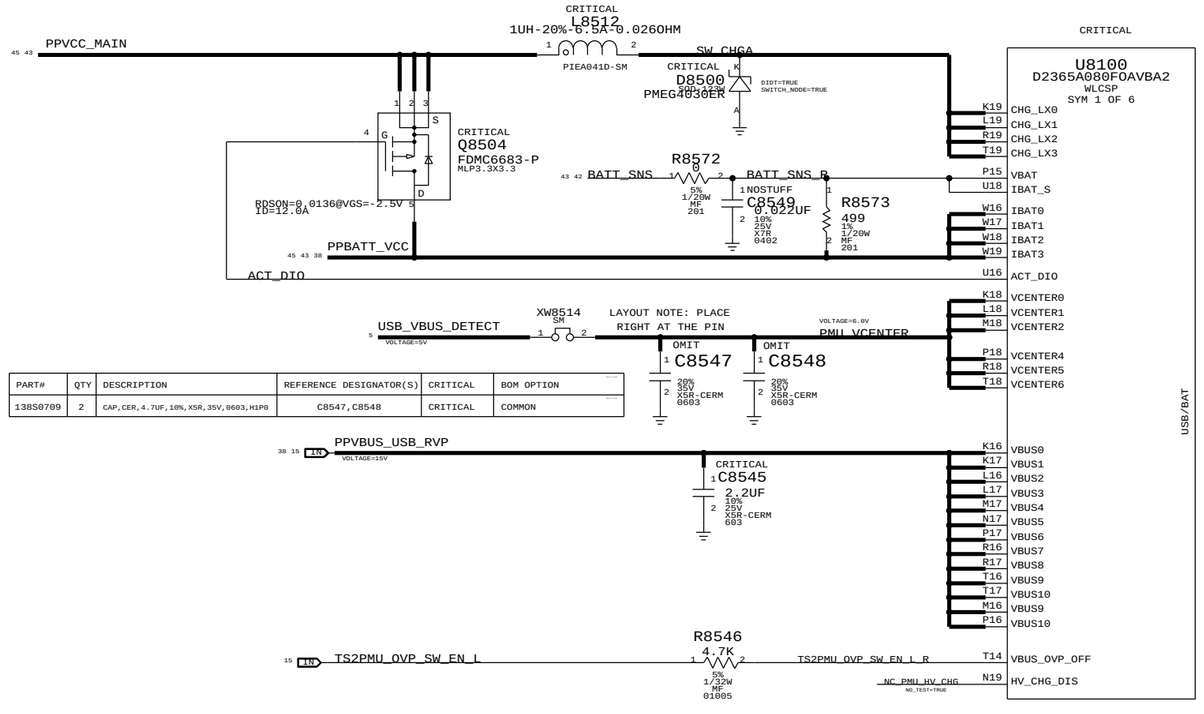


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392		Y8300	RDAR://PROBLEM/9936684

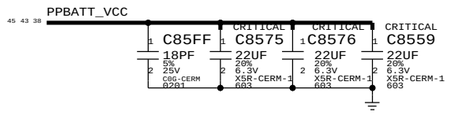
118S0764	118S0717		R8340	RDAR://PROBLEM/8380367
107S0150	107S0208		R8321-R8328	RDAR://PROBLEM/8380367


CRITICAL
U8100
D2365A080F0AVBA2
WLCSP
SYM 4 OF 6
LCM/GRAPE
38 PMU_VCENTER
N18 VDD_HI
VDD_LCM_SW B17
VDD_BOOST_LCM C16
BOOST_LCM_LX A16
VDD_LCM D16
VLCM1 C15
LCM2_EN D13
=PPVCC_MAIN_VDD_LCM 45
LCM_LX
(NOTE: 2MHZ)
PP6V0_LCM_HI
43 PP6V0_LCM_VBOOST
PP5V25_GRAPE
(100MA; 5.0-6.0V)
43 45
CRITICAL
L8429
2.2UH-1.05A-0.195OHM
VLS201612E-SM
MAKE_BASE=TRUE
VOLTAGE=6.0V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
DIDT=TRUE
CRITICAL
D8430
PMEG2005AEL
SOD882
CRITICAL
C8412
10UF
20%
25V
X5R-CERM
0603
CRITICAL
C8495
56PF
5%
16V
NP0-C0G
01005
CRITICAL
C8410
2.2UF
10%
10V
X5R-CERM
0402
CRITICAL
C8411
4.7UF
20%
10V
X5R-CERM
0402
CRITICAL
C8490
4.7UF
20%
10V
X5R-CERM
0402
MAKE_BASE=TRUE
VOLTAGE=6.0V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

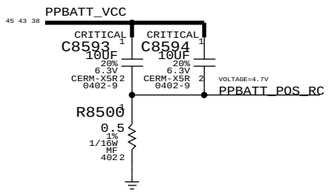


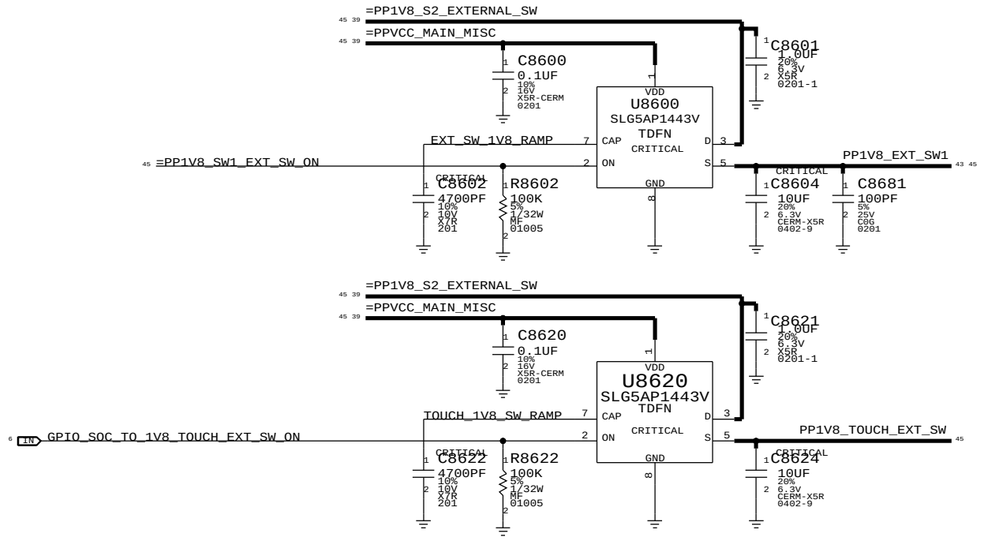


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0709	2	CAP,CER,4.7UF,10%,X5R,35V,0603,H1P0	C8547,C8548	CRITICAL	COMMON

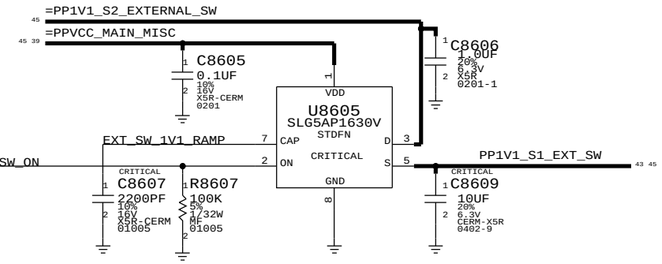


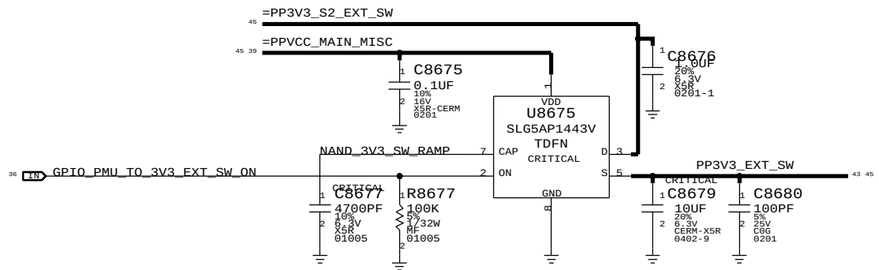
NOTE: FOR NO BATTERY SITUATION

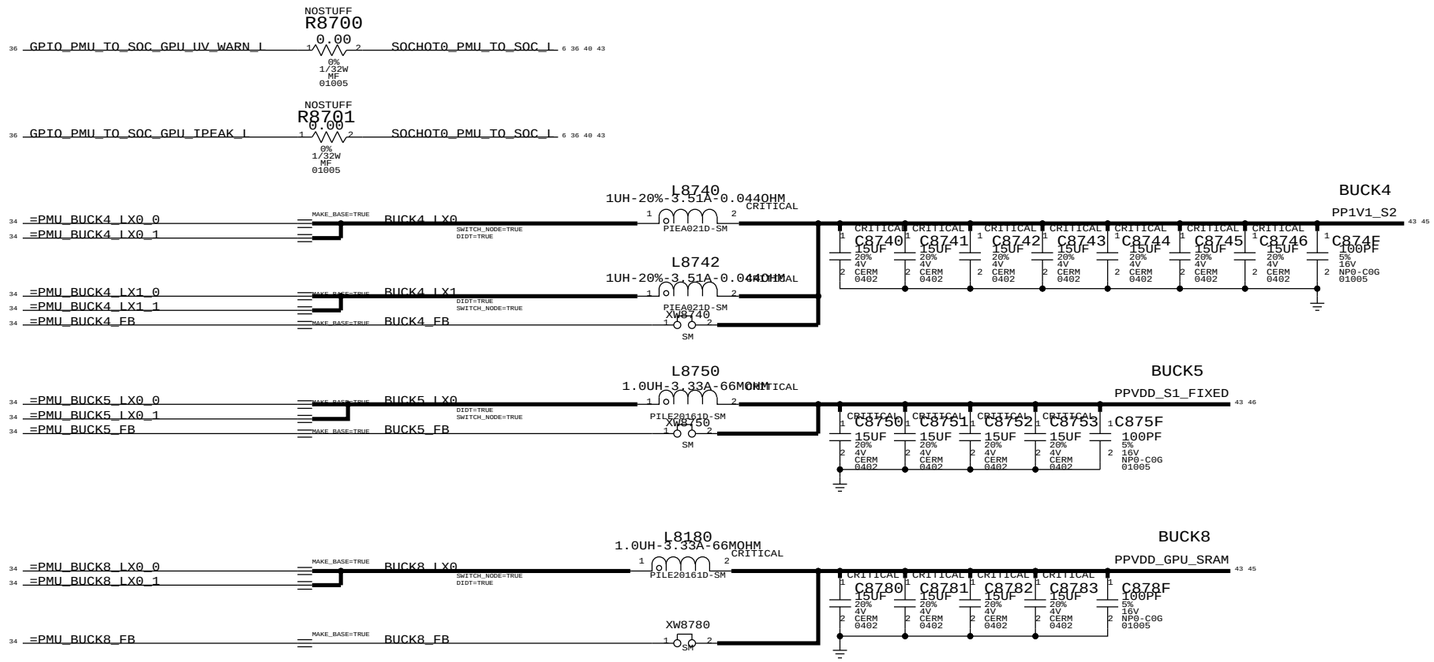



=PP1V8_S2_EXTERNAL_SW
=PPVCC_MAIN_MISC
C8600
0.1UF
10%
16V
X5R-CERM
0201
C8601
1.0UF
20%
6.3V
X5R
0201-1
U8600
SLG5AP1443V
TDFN
CRITICAL
VDD
CAP
ON
GND
D
S
=PP1V8_SW1_EXT_SW_ON
EXT_SW_1V8_RAMP
PP1V8_EXT_SW1
C8602
4700PF
10%
10V
X7R
201
R8602
100K
5%
1/32W
MF
01005
C8604
10UF
20%
6.3V
CERM-X5R
0402-9
C8681
100PF
5%
25V
C0G
0201

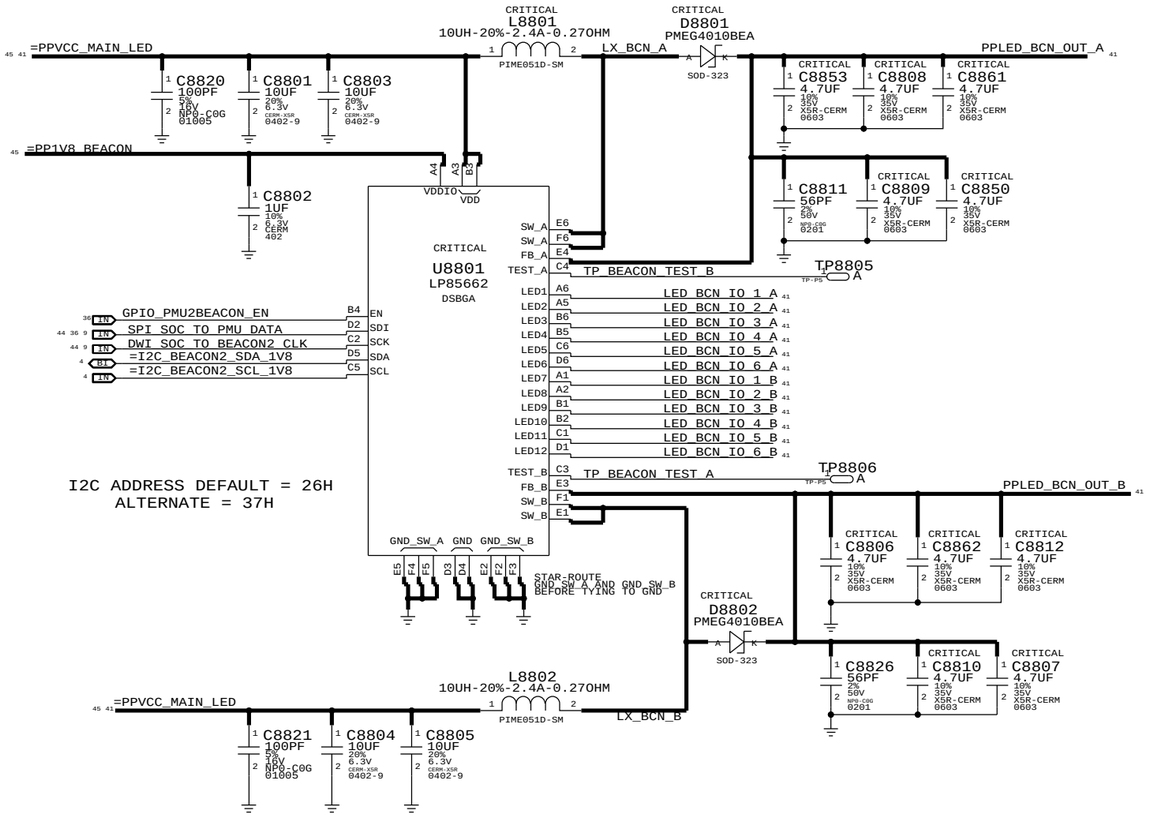
=PP1V8_S2_EXTERNAL_SW
=PPVCC_MAIN_MISC
C8620
0.1UF
10%
16V
X5R-CERM
0201
C8621
1.0UF
20%
6.3V
X5R
0201-1
U8620
SLG5AP1443V
TDFN
CRITICAL
VDD
CAP
ON
GND
D
S
GPIO_SOC_TO_1V8_TOUCH_EXT_SW_ON
TOUCH_1V8_SW_RAMP
PP1V8_TOUCH_EXT_SW
C8622
4700PF
10%
10V
X7R
201
R8622
100K
5%
1/32W
MF
01005
C8624
10UF
20%
6.3V
CERM-X5R
0402-9

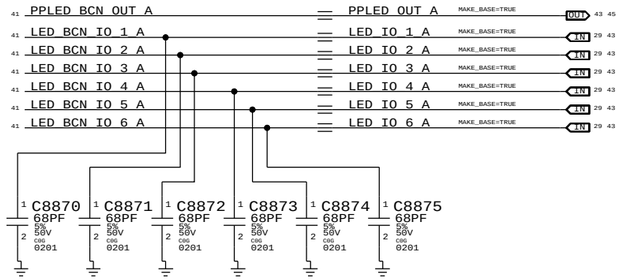

=PP1V1_S2_EXTERNAL_SW
=PPVCC_MAIN_MISC
C8605
0.1UF
10%
16V
X5R-CERM
0201
C8606
1.0UF
20%
6.3V
X5R
0201-1
U8605
SLG5AP1630V
STDFN
CRITICAL
VDD
CAP
ON
GND
D
S
GPIO_PMU_TO_1V1_EXT_SW_ON
EXT_SW_1V1_RAMP
PP1V1_S1_EXT_SW
C8607
2200PF
10%
16V
X5R-CERM
01005
R8607
100K
5%
1/32W
MF
01005
C8609
10UF
20%
6.3V
CERM-X5R
0402-9


=PP3V3_S2_EXT_SW
=PPVCC_MAIN_MISC
C8675
0.1UF
10%
16V
X5R-CERM
0201
C8676
1.0UF
20%
6.3V
X5R
0201-1
U8675
SLG5AP1443V
TDFN
CRITICAL
VDD
CAP
ON
GND
D
S
GPIO_PMU_TO_3V3_EXT_SW_ON
NAND_3V3_SW_RAMP
PP3V3_EXT_SW
C8677
4700PF
10%
6.3V
X5R
01005
R8677
100K
5%
1/32W
MF
01005
C8679
10UF
20%
6.3V
CERM-X5R
0402-9
C8680
100PF
5%
25V
C0G
0201


NOSTUFF
R8700
0.00
0%
1/32W
MF
01005
GPIO_PMU_TO_SOC_GPU_UV_WARN_L
SOCHOT0_PMU_TO_SOC_L
NOSTUFF
R8701
0.00
0%
1/32W
MF
01005
GPIO_PMU_TO_SOC_GPU_IPEAK_L
SOCHOT0_PMU_TO_SOC_L
L8740
1UH-20%-3.51A-0.044OHM
CRITICAL
PIEA021D-SM
=PMU_BUCK4_LX0_0
=PMU_BUCK4_LX0_1
BUCK4_LX0
MAKE_BASE=TRUE
SWITCH_NODE=TRUE
DIDT=TRUE
L8742
1UH-20%-3.51A-0.044OHM
CRITICAL
PIEA021D-SM
=PMU_BUCK4_LX1_0
=PMU_BUCK4_LX1_1
BUCK4_LX1
XW8740
SM
=PMU_BUCK4_FB
BUCK4_FB
BUCK4
PP1V1_S2
C8740 15UF 20% 4V CERM 0402
C8741 15UF 20% 4V CERM 0402
C8742 15UF 20% 4V CERM 0402
C8743 15UF 20% 4V CERM 0402
C8744 15UF 20% 4V CERM 0402
C8745 15UF 20% 4V CERM 0402
C8746 15UF 20% 4V CERM 0402
C874E 100PF 5% 16V NP0-C0G 01005
L8750
1.0UH-3.33A-66MOHM
CRITICAL
PILE20161D-SM
=PMU_BUCK5_LX0_0
=PMU_BUCK5_LX0_1
BUCK5_LX0
XW8750
SM
=PMU_BUCK5_FB
BUCK5_FB
BUCK5
PPVDD_S1_FIXED
C8750 15UF 20% 4V CERM 0402
C8751 15UF 20% 4V CERM 0402
C8752 15UF 20% 4V CERM 0402
C8753 15UF 20% 4V CERM 0402
C875F 100PF 5% 16V NP0-C0G 01005
L8180
1.0UH-3.33A-66MOHM
CRITICAL
PILE20161D-SM
=PMU_BUCK8_LX0_0
=PMU_BUCK8_LX0_1
BUCK8_LX0
XW8780
SM
=PMU_BUCK8_FB
BUCK8_FB
BUCK8
PPVDD_GPU_SRAM
C8780 15UF 20% 4V CERM 0402
C8781 15UF 20% 4V CERM 0402
C8782 15UF 20% 4V CERM 0402
C8783 15UF 20% 4V CERM 0402
C878F 100PF 5% 16V NP0-C0G 01005

BEACON 2

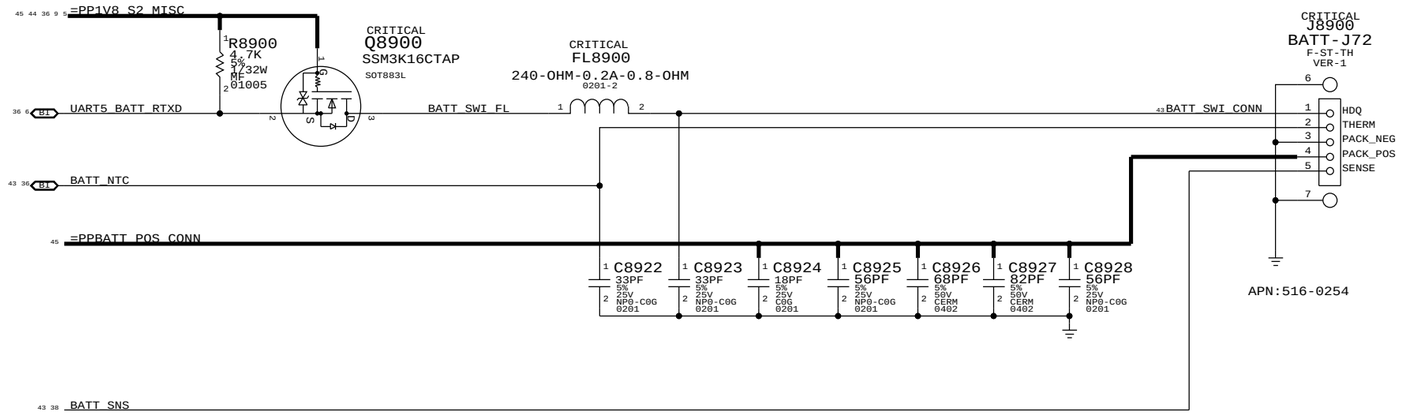




SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

DIODE ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0730	371S0490			DIODES DIODE ALTERNATE



SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

AUDIO

TP9300 GPIO_CODEC_IRQ_L 7 17
TP931B GPIO_SOC2CODEC_RST_L 6 17
TP93N1 GPIO_SOC2AJ_HS4_SHUNT_EN 6 16
TP93N3 GPIO_SOC2AJ_HS3_SHUNT_EN 6 16
TP9304 PMU_GPIO_CODEC_HS_INT_L 17 36
TP9320 CODEC_HP_DET_R 17
TP9321 CODEC_HP_HS3 17
TP9322 CODEC_HP_HS3_REF 17
TP9323 CODEC_HP_HS4 17
TP9324 CODEC_HP_HS4_REF 17
TP9325 CODEC_HP_LEFT 17
TP9326 CODEC_HP_RIGHT 17
TP9337 GND_AUDIO_CODEC 17
TP93MC DMIC1_FF_SCLK_FILT 16
TP9309 DMIC1_FF_SD_FILT 16
TP931C MIKEY_TS_N 15 17
TP931D MIKEY_TS_P 15 17
TP93H5 SPKRAMP_L1_OUT_N 18 26
TP93H6 SPKRAMP_L1_OUT_P 18 26
TP9370 SPKRAMP_L2_OUT_N 18 26
TP9371 SPKRAMP_L2_OUT_P 18 26
TP93H7 SPKRAMP_R1_OUT_N 19 26
TP93H8 SPKRAMP_R1_OUT_P 19 26
TP93MA SPKRAMP_R2_OUT_N 19 26
TP93MB SPKRAMP_R2_OUT_P 19 26
TP9393 PP1V7_VA_VCP 35 45
TP93MD LEFT_CH_OUT_N 17 18
TP93HF LEFT_CH_OUT_P 17 18
TP93H9 RIGHT_CH_OUT_N 17 19
TP93HA RIGHT_CH_OUT_P 17 19
TP93HB AIN3N 17

BUTTONS

TP9338 GPIO_BTN_HOME_CONN_L 27
TP9339 GPIO_BTN_ONOFF_L_FILT 23
TP9341 GPIO_BTN_VOL_DOWN_L_FILT 23
TP9342 GPIO_BTN_VOL_UP_L_FILT 23

CAMERAS

TP93JA PP2V9_CAM 35 45
TP930A PP2V9_AVDD_CAM_FRONT_FILT 24
TP93J3 PP2V9_AVDD_CAM_REAR_FILT 25
TP93B1 PP2V6_CAM_REAR_AF_FILT 25
TP93A7 PP1V8_SW1 35 45
TP9301 PP1V8_CAM_FRONT_FILT 24
TP93NB PP1V8_CAM_REAR_FILT 25
TP93JC PP1V25_CAM_REAR_FILT 25
TP9380 ISP0_CAM_REAR_CLK 7 25
TP9353 ISP0_CAM_REAR_SCL 7 25
TP9354 ISP0_CAM_REAR_SDA 7 25
TP9355 ISP0_CAM_REAR_SHUTDOWN_L 7 25
TP93JB ISP1_CAM_FRONT_CLK_F 24
TP93JE ISP1_CAM_FRONT_SCL_F 24
TP93JF ISP1_CAM_FRONT_SDA_F 24
TP93HE ISP1_CAM_FRONT_SHUTDOWN_L_F 24

DISPLAY

TP9372 LED_IO_1_A 29 41
TP9373 LED_IO_2_A 29 41
TP9374 LED_IO_3_A 29 41
TP9375 LED_IO_4_A 29 41
TP9376 LED_IO_5_A 29 41
TP9377 LED_IO_6_A 29 41
TP9378 LED_IO_1_B 29 41
TP9379 LED_IO_2_B 29 41
TP937A LED_IO_3_B 29 41
TP937B LED_IO_4_B 29 41
TP937C LED_IO_5_B 29 41
TP9370 LED_IO_6_B 29 41
TP9305 PPLED_OUT_A 41 45
TP93JD PPLED_OUT_B 41 45
TP93DB PPLED_BACK_REG_B 29
TP93D0 PPLED_BACK_REG_A 29

POWER

TP9391 PP0V8_S2_SOC_AOP 35 45
TP9389 PP1V1_S2 40 45
TP9396 PP1V1_S1_EXT_SW 39 45
TP9388 PP1V2_SOC 35 45
TP93A3 PP1V2_PLL_SOC_FILT 5
TP9395 PP1V8_ALWAYS 35 45
TP93A8 PP1V8_EXT_SW1 39 45
TP93A4 PP1V8_S2 34 45
TP93A6 PP1V8_S2_SW3 35 45
TP93A2 =PP1V8_GRAPE_SW 28 45
TP93A9 PP1V8_XTAL_FILT 5
TP93C0 PP3V0_S2_MISC 35 45
TP93C1 PP3V0_S2_TRISTAR 35 45
TP93C3 PP3V3_ACC 35 45
TP93C4 PP3V3_S2 30 34 45
TP93C5 PP3V3_EXT_SW 39 45
TP93C6 PP5V25_GRAPE 37 45
TP93C8 PP6V0_LCM_VBOOST 37
TP93D5 PPVCC_MAIN 38 45
TP93D6 PPVCC_MAIN_LCD_SW_CONN 29
TP93D7 PPVDD_CPU 34 45
TP93D8 PPVDD_GPU 34 36 45
TP93D9 PPVDD_S1_SOC 34 45
TP93C9 PPBATT_VCC 38 43 45
TP93CA PPBATT_VCC 38 43 45
TP93CB PPBATT_VCC 38 43 45
TP93CC PPBATT_VCC 38 43 45
TP93CD PPBATT_VCC 38 43 45
TP93CE PPBATT_VCC 38 43 45
TP9340
TP9336
TP9392
TP9394
TP9306
TP9397
TP9398
TP9399
TP939A
TP939B
TP93N7 PPVDD_CPU_SRAM 34 45
TP93N8 PPVDD_GPU_SRAM 40 45
TP93N9 PPVDD_S1_FIXED 40 46
TP93NA PP0V9_NAND 35 45
TP93NE BATT_SWI_CONN 42
TP93NF BATT_SNS 38 42

SENSORS

TP93J9 PP3V0_ALS 35 45
TP937E PP1V8_PHOS_F 22
TP937F PP1V825_S2_MESA_CONN 20 27
TP931E PP3V1_S2_MESA_CONN 20 27
TP931F PP11V3_MESA_CONN 20 27
TP93N4 GPIO_MESA_TO_BOOST_ENABLE_CONN 20 27
TP93N6 PP3V0_COMPASS 22
TP93N5 PP1V8_S2R_HALL2_FILT 27
TP930C GPIO_HALL_CENTER_TO_PMU_IRQ 27 36
TP93N2 GPIO_HALL_EDGE_TO_PMU_IRQ 22 36

THERMAL

TP9303 BATT_NTC 36 42
TP9312 BOARD_TEMP3_P 36
TP9313 BOARD_TEMP4_P 36
TP9314 BOARD_TEMP5_P 36
TP9315 BOARD_TEMP6_P 36
TP9316 BOARD_TEMP7_P 36
TP9317 BOARD_TEMP8_P 36

SOC

TP93G9 SOC_TESTMODE 4 5
TP9311 TP_JTAG_SOC_TDO 5
NEAR U0600 NEAR U1700 TP93I4 UART_DEBUG_TO_SOC_TX 6 15
NEAR U0600 NEAR U1700 TP93I5 UART_SOC_TO_DEBUG_TX 6 15
NEAR U0600 NEAR U1700 TP93I8 UART_ACC_TO_SOC_TX 6 15
NEAR U0600 NEAR U1700 TP9319 UART_SOC_TO_ACC_TX 6 15
TP93J0 USB_SOC_N 5 15
TP9311 USB_SOC_P 5 15
TP9360 JTAG_SOC_SEL 4 5
TP9361 JTAG_SOC_TCK 5 15
TP9362 JTAG_SOC_TDI 5
TP9363 JTAG_SOC_TMS 5 15
TP9364 TP_JTAG_SOC_TRST_L 4 5
TP9334 USB_ID 5
TP9343 GPIO_FORCE_DFU 6 36
TP93G6 RESET_PMU_TO_SYSTEM_L 5 9 36
NEAR U0600 TP9384 CLK_PMU_TO_AOP_32K 9 36
NEAR U8100 TP9329 P4MM SM PP 1 SPI_SOC_TO_PMU_SCLK 9 36 44
TP93NC SOCHOT0_PMU_TO_SOC_L 6 36 40
TP93ND TP_GPIO_DFU_STATUS 6

E75

TP93M0 CONN_DET_L 26
TP93D1 PPOUT_E75_ACC_ID1_CONN 26
TP93D2 PPOUT_E75_ACC_ID2_CONN 26
TP93D4 PPVBUS_USB_FILT 26 38
TP93DA PPVBUS_E75_USB_CONN 26 43
DELETE ONE IF CAN'T PLACE
TP93DC PPVBUS_E75_USB_CONN 26 43
TP93DD PPVBUS_E75_USB_CONN 26 43
TP93DE PPVBUS_E75_USB_CONN 26 43
TP9330 E75_DPAIR1_CONN_N 26
TP9331 E75_DPAIR1_CONN_P 26
TP9332 E75_DPAIR2_CONN_N 26
TP9333 E75_DPAIR2_CONN_P 26

TOUCH

TP9328 DISPLAY_SYNC 6 28
TP9344 GPIO_GRAPE_IRQ_L 6 28
NEAR U4050 TP9318 CLK_32K_SOC2CUMULUS 6 28
TP9345 GPIO_GRAPE_RST_L 6 28
TP9306 TP_CUMULUS_S_H_CS_L 28
TP9307 TP_CUMULUS_S_H_SCLK 28
TP9308 TP_CUMULUS_S_H_SDI 28
TP930B TP_CUMULUS_S_H_SDO 28
TP930E CUMULUS_MS_CK 28
TP930F CUMULUS_MS_SD 28
TP9310 TP_JTAG_CUMULUS_M_TCK 28
TP9311 TP_JTAG_CUMULUS_M_TDI 28
TP9319 TP_JTAG_CUMULUS_M_TDO 28
TP931A JTAG_CUMULUS_M_TMS 28
NEAR U4000 NEAR U0600 TP93H1 SPI_GRAPE_CS_L 6 28
NEAR U0600 TP93H2 SPI_GRAPE_MISO 6 28
NEAR U4000 TP93H3 SPI_GRAPE_MOSI 6 28
NEAR U4000 TP93H4 SPI_GRAPE_SCLK 6 28

RF TEST POINTS

BB_SIM_CLK TP93B9
BB_SIM_DATA TP93E7
BB_SIM_DETECT TP93E8
BB_SIM_RESET TP9302
PP_LDO5 TP93F3
UART_BB2SOC_TX TP931G
UART_SOC2BB_TX TP931F
BB_UART_RTS_L TP93FC
BB_UART_CTS_L TP93FB
BB_OTTHER_TXD TP93FA
BB_OTHER_RXD TP93F9
UART_BB2WLAN_COES_RX TP93L6
UART_WLAN2BB_COEX_TX TP93L1
AP_WAKE_MODEM TP93F0
BB_GPS_SYNC TP93F7
BB_USB_VBUS TP93E2
BB_CORE_DUMP TP93F6
RF_PMIC_RESET_L TP93F5
RADIO_ON_L TP93F4
BB_RESET_DET_L TP93E3
PP_LDO13 TP93ME

TP5000
TP5001
TP5002
TP5004
TP5005
TP5010
TP5015
TP5021 PPBATT_VCC 38 43 45
TP5025
TP5026
TP5028
TP5029
TP5007

WIFI TEST POINTS

NEAR U7500 TP93K0 PCIE1_SOC2WLAN_TX_P 8 30
NEAR U7500 TP93K1 PCIE1_SOC2WLAN_TX_N 8 30
NEAR U0600 TP93K2 PCIE1_WLAN2SOC_RX_P 8 30
NEAR U0600 TP93K3 PCIE1_WLAN2SOC_RX_N 8 30
TP93M4 CLK_PMU2WLAN_32K 30 32 43
NEAR U7500 TP93K5 UART2_SOC2WLAN_TX 6 30
NEAR U0600 TP93K6 UART2_WLAN2SOC_TX 6 30
NEAR U0600 TP93K8 UART2_WLAN2SOC_RTS_L 6 30
TP93K9 GPIO_PMU2WLAN_REG_ON 30 32
TP93KA GPIO_PMU2BT_REG_ON 30 32
TP93KC GPIO_SOC2WLAN_PCIE_DEV_WAKE 6 30 32
NEAR U7500 TP93KD UART2_SOC2WLAN_RTS_L 6 30
TP93KE TP_JTAG_WLAN_TMS 30
TP93KF TP_JTAG_WLAN_TRST 30
TP93L2 GPIO_BT2PMU_HOST_WAKE 30 32
TP93L3 GPIO_SOC2BT_WAKE 6 30 32
NEAR U7500 TP93L4 UART_SOC2BT_TX 6 30 32
NEAR U0600 TP93L5 UART_BT2SOC_TX 6 30 32
NEAR U7500 TP93L6 UART_SOC2BT_RTS_L 6 30 32
NEAR U0600 TP93L7 UART_BT2SOC_RTS_L 6 30 32
TP9365 JTAG_WLAN_SEL 32
TP93LC AOP2RADIO_CONTEXT_A 9 30
TP93LD AOP2RADIO_CONTEXT_B 9 30
TP93LE GPIO_WLAN2PMU_HOST_WAKE 30 32
TP93M1 PCIE1_WLAN2SOC_CLKREQ_L 8 30
TP93M0 PCIE1_SOC2WLAN_RST_L 8 30
TP93M3 TESTPOINT_JTAG_WLAN_TCK 30

TP -> PP

TP93K4 P4MM SM PP 1 CLK_PMU2WLAN_32K 30 32 43

STANDOFF P/N 860-1596

STD9302
STDOFF-3.3X1.8R1.02H-SM
1 BATTERY

860-1595

STD9300
STDOFF-3.3X1.8R1.17H-SM-1
1 GRAPE

STD9301
STDOFF-3.3X1.8R1.17H-SM-1
1 DISPLAY

STD9303
STDOFF-3.3X1.8R1.17H-SM-1
1 BATTERY

STD9350
STDOFF-3.3X1.8R1.17H-SM-1
1 FRONT CAMERA

STD9360
STDOFF-3.3X1.8R1.17H-SM-1
1 BUTTON FLEX

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

SL9303
TH-NSP
1
SL-1.1X0.4-1.4X0.7

SYNC_MASTER=J85 MLB_C SYNC_DATE=12/03/12

EE CHARACTERIZATION PP

NAND

	PP9400 P4MM SM	1	PCIE_SOC_TO_NAND_TX_P<0>	8 14
	PP9401 P4MM SM	1	PCIE_SOC_TO_NAND_TX_N<0>	8 14
PLACE NEAR U1600	PP9402 P4MM SM	1	PCIE_SOC_TO_NAND_REFCLK_P	8 14
	PP9403 P4MM SM	1	PCIE_SOC_TO_NAND_REFCLK_N	8 14
	PP9434 P4MM SM	1	CLK_SOC_TO_NAND_24MHZ	6 14
PLACE NEAR U0600	PP9404 P4MM SM	1	PCIE_NAND_TO_SOC_TX_P<0>	8 14
	PP9405 P4MM SM	1	PCIE_NAND_TO_SOC_TX_N<0>	8 14

PMU/BEACON2 SPI/DWI

PLACE NEAR U8100	PP9407 P4MM SM	1	SPI_SOC_TO_PMU_DATA	9 36 41 44
PLACE NEAR U8801	PP9408 P4MM SM	1	DWI_SOC_TO_BEACON2_CLK	9 41
	PP9409 P4MM SM	1	SPI_SOC_TO_PMU_DATA	9 36 41 44
PLACE NEAR U0600	PP940A P4MM SM	1	SPI_SOC_TO_PMU_SCLK	9 36 43
	PP940B P4MM SM	1	SPI_PMU_TO_SOC_DATA	9 36
	PP9440 P4MM SM	1	PMU_SHUTDOWN	4 36
	PP9441 P4MM SM	1	GPIO_AOP_TO_PMU_SLEEP1_REQUEST	9 36
	PP9442 P4MM SM	1	GPIO_PMU_TO_SYS_SLEEP1_READY	9 10 36
	PP9443 P4MM SM	1	GPIO_AOP_TO_PMU_ACTIVE_REQUEST	9 36
	PP9444 P4MM SM	1	GPIO_PMU_TO_SYSTEM_ACTIVE_READY	5 9 15 36

AUDIO

PLACE NEAR U1900	PP9421 P4MM SM	1	I2S0_CODEC_ASP_MCK	6 17
PLACE NEAR U1900	PP9422 P4MM SM	1	I2S0_CODEC_ASP_BCLK	6 17
PLACE NEAR U1900	PP9423 P4MM SM	1	I2S0_CODEC_ASP_LRCK	6 17
PLACE NEAR U1900	PP9424 P4MM SM	1	I2S0_SOC2CODEC_ASP_DATA	6 17
PLACE NEAR U0600	PP9425 P4MM SM	1	I2S0_CODEC2SOC_ASP_DATA	6 17
PLACE NEAR U1900	PP9426 P4MM SM	1	SPI_CODEC_SCLK	6 17
PLACE NEAR U1900	PP9427 P4MM SM	1	SPI_CODEC_MOSI	6 17
PLACE NEAR U0600	PP9428 P4MM SM	1	SPI_CODEC_MISO	6 17
PLACE NEAR U1900	PP9460 P4MM SM	1	I2S2_CODEC_XSP_BCLK	6 17
PLACE NEAR U1900	PP9461 P4MM SM	1	I2S2_CODEC_XSP_LRCK	6 17
PLACE NEAR U1900	PP9462 P4MM SM	1	I2S2_SOC2CODEC_XSP_DATA	6 17
PLACE NEAR U0600	PP9463 P4MM SM	1	I2S2_CODEC2SOC_XSP_DATA	6 17

SENSORS

PLACE NEAR U2590	PP9429 P4MM SM	1	SPI_AOP_SCLK	9 22 44
PLACE NEAR U2590	PP9430 P4MM SM	1	SPI_AOP_MOSI	9 22 44
PLACE NEAR U2580	PP9431 P4MM SM	1	SPI_AOP_SCLK	9 22 44
PLACE NEAR U2580	PP9432 P4MM SM	1	SPI_AOP_MOSI	9 22 44
PLACE NEAR U0600	PP9433 P4MM SM	1	SPI_AOP_MISO	9 22

MESA SPI

PLACE NEAR U0600	PP940C P4MM SM	1	SPI_MESA_MISO	6 20

CAMERA - FRONT

	PP940D P4MM SM	1	MIPI1C_CAM_FRONT_CLK_P	7 24 44
	PP940E P4MM SM	1	MIPI1C_CAM_FRONT_CLK_N	7 24 44
PLACE NEAR U0600				
	PP940F P4MM SM	1	MIPI1C_CAM_FRONT_DATA_P<0>	7 24 44
	PP9410 P4MM SM	1	MIPI1C_CAM_FRONT_DATA_N<0>	7 24 44

CAMERA - REAR

	PP9411 P4MM SM	1	MIPI0C_CAM_REAR_CLK_P	7 25 44
	PP9412 P4MM SM	1	MIPI0C_CAM_REAR_CLK_N	7 25 44
PLACE NEAR U0600				
	PP9413 P4MM SM	1	MIPI0C_CAM_REAR_DATA_P<0>	7 25 44
	PP9414 P4MM SM	1	MIPI0C_CAM_REAR_DATA_N<0>	7 25 44

WIFI

PLACE NEAR U7500	PP9417 P4MM SM	1	PCIE1_SOC2WLAN_REFCLK_P	8 30
	PP9418 P4MM SM	1	PCIE1_SOC2WLAN_REFCLK_N	8 30

DEBUG

45 42 36 9 5 =PP1V8_S2_MISC — TP9402 1 A TP-P55 — NEAR R0760 OR TP9343

SOC

	PP9450 P4MM SM	1	ADC_SOC_TO_PMU_VDD_CPU	11 36
	PP9451 P4MM SM	1	TP_VSS_CPU_SENSE	11
	PP9452 P4MM SM	1	ADC_SOC_TO_PMU_VDD_GPU	11 36
	PP9453 P4MM SM	1	TP_VSS_GPU_SENSE	11

HIGH SPEED, NO TEST

1341	MIPI0C_CAM_REAR_CLK_P	NO_TEST=TRUE	7 25 44
1405	MIPI0C_CAM_REAR_CLK_N	NO_TEST=TRUE	7 25 44
1339	MIPI0C_CAM_REAR_DATA_P<0..3>	NO_TEST=TRUE	7 25 44
1335	MIPI0C_CAM_REAR_DATA_N<0..3>	NO_TEST=TRUE	7 25 44
1842	MIPI0C_CAM_REAR_CLK_FILT_P	NO_TEST=TRUE	25
1844	MIPI0C_CAM_REAR_CLK_FILT_N	NO_TEST=TRUE	25
1845	MIPI0C_CAM_REAR_DATA_FILT_P<0..3>	NO_TEST=TRUE	25
1843	MIPI0C_CAM_REAR_DATA_FILT_N<0..3>	NO_TEST=TRUE	25
1411	MIPI1C_CAM_FRONT_CLK_P	NO_TEST=TRUE	7 24 44
1443	MIPI1C_CAM_FRONT_CLK_N	NO_TEST=TRUE	7 24 44
1358	MIPI1C_CAM_FRONT_DATA_P<0>	NO_TEST=TRUE	7 24 44
1445	MIPI1C_CAM_FRONT_DATA_N<0>	NO_TEST=TRUE	7 24 44
1417	MIPI1C_CAM_FRONT_CLK_FILT_P	NO_TEST=TRUE	24
1357	MIPI1C_CAM_FRONT_CLK_FILT_N	NO_TEST=TRUE	24
1353	MIPI1C_CAM_FRONT_DATA_FILT_P<0>	NO_TEST=TRUE	24
1351	MIPI1C_CAM_FRONT_DATA_FILT_N<0>	NO_TEST=TRUE	24
1387	EDP_DATA_P<0..3>	NO_TEST=TRUE	7 29
1385	EDP_DATA_N<0..3>	NO_TEST=TRUE	7 29
1383	EDP_DATA_EMI_P<0..3>	NO_TEST=TRUE	29
1381	EDP_DATA_EMI_N<0..3>	NO_TEST=TRUE	29
1389	EDP_DATA_EMI_CONN_P<0..3>	NO_TEST=TRUE	29
1387	EDP_DATA_EMI_CONN_N<0..3>	NO_TEST=TRUE	29

SYNC_MASTER=MLB_B SYNC_DATE=07/26/2016

POWER CONNECTIONS

BUCK0 (ACTIVE)

PPVDD_CPU — =PPVDD_CPU — 12400MA
MAKE_BASE=TRUE
VOLTAGE=1.6V

BUCK1 (SW CONTROL)

PPVDD_GPU — =PPVDD_GPU — 8300MA
MAKE_BASE=TRUE
VOLTAGE=0.8V

BUCK2 (SLEEP1)

PPVDD_S1_SOC — =PPVDD_S1_SOC — 1524MA
MAKE_BASE=TRUE
VOLTAGE=0.9V

BUCK3 (SLEEP2)

PP1V8_S2 — =PP1V8_S2_DDR — 100MA
MAKE_BASE=TRUE
VOLTAGE=1.8V
=PP1V8_S2_TRISTAR — 1MA
=PP1V8_S2_HALL — 1MA
=PP1V8_S2_MISC — 8MA
=PP1V8_S2_EXTERNAL_SW — 36.4MA
=PP1V8_S2_INTERNAL_SW — 430MA
=PP1V8_S2_INTERNAL_LDOS — 60MA
=PP1V8_S2_ROTTERDAM — 1MA
=PP1V8_S2_WIFI — 20MA
=PP1V8_S2_AUDIO — 25.5MA

BUCK3_SW

BUCK3_SW1 (ACTIVE)

PP1V8_SW1 — =PP1V8_AUDIO — 3MA
MAKE_BASE=TRUE
VOLTAGE=1.8V
=PP1V8_SW1_EXT_SW_ON — 0MA
=PP1V8_DMIC — 1MA
=PP1V8_CAM_FRONT — 1MA
=PP1V8_CAM_REAR

BUCK3_EXT_SW1 (ACTIVE)

PP1V8_EXT_SW1 — =PP1V8_VDDIO_SOC — 9MA
MAKE_BASE=TRUE
VOLTAGE=1.8V
=PP1V8_XTAL_SOC — 2MA
=PP1V8_MIPI_SOC — 8MA
=PP1V8_USB_SOC — 20MA
=PP1V8_NAND — 315MA
=PP1V8_EEPROM — 5MA
=PP1V8_SOC — 10MA
=PP1V8_MISC — 4MA
=PP1V8_BEACON — 10MA

BUCK3_SW3 (SLEEP2)

PP1V8_S2_SW3 — =PP1V8_S2_CARBON — 5MA
MAKE_BASE=TRUE
VOLTAGE=1.8V
=PP1V8_S2_PHOSPHORUS — 1.2MA
=PP1V8_S2_COMPASS — 16MA
=PP1V8_S2_AOP — 0.2MA
9MA

BUCK3 EXT SW TOUCH

PP1V8_TOUCH_EXT_SW — =PP1V8_GRAPE_SW
MAKE_BASE=TRUE
VOLTAGE=1.8V

BUCK4 (SLEEP2)

PP1V1_S2 — =PP1V1_S2_EXTERNAL_SW — 638MA
MAKE_BASE=TRUE
VOLTAGE=1.1V
=PP1V1_S2_INTERNAL_LDOS — 105.1MA
=PP1V1_S2_INTERNAL_SW — 0MA
=PP1V1_S2_DDR — 1300MA

BUCK4_EXT_SW (SLEEP1)

PP1V1_S1_EXT_SW — =PP1V1_S1_DDR_VDDQ — 635MA
MAKE_BASE=TRUE
VOLTAGE=1.1V
=PP1V1_S1_DDR_PLL_SOC — 3MA

BUCK5

BUCK 5 ALIASES ON NEXT PAGE (IF USED)

BUCK6 (SLEEP2)

PP3V3_S2 — =PP3V3_S2_WIFI — 1160MA
MAKE_BASE=TRUE
VOLTAGE=3.3V
=PP3V3_S2_EXT_SW

EXT SW (ACTIVE)

PP3V3_EXT_SW — =PP3V3_NAND — 1100MA
MAKE_BASE=TRUE
VOLTAGE=3.3V
=PP3V3_USB_SOC — 5MA

BUCK7 (ACTIVE)

PPVDD_CPU_SRAM — =PPVDD_CPU_SRAM — 354MA
MAKE_BASE=TRUE
VOLTAGE=1.06V

BUCK8 (SW CONTROL)

PPVDD_GPU_SRAM — =PPVDD_GPU_SRAM — 360MA
MAKE_BASE=TRUE
VOLTAGE=0.92V

LDO1 (SLEEP2)

PP3V0_S2_TRISTAR — =PP3V0_S2_TRISTAR — 3MA
MAKE_BASE=TRUE
VOLTAGE=3.0V

LDO2

PP1V7_VA_VCP — =PP1V7_VA_VCP — 10MA
MAKE_BASE=TRUE
VOLTAGE=1.7V

LDO3 (SPARE)

LDO4 (SW CONTROL)

PP3V0_ALS — =PP3V0_ALS — 1MA
MAKE_BASE=TRUE
VOLTAGE=3.0V

LDO5 (SPARE)

LDO6 (SW CONTROL)

PP3V3_ACC — =PP3V3_ACC — 1000MA
MAKE_BASE=TRUE
VOLTAGE=3.3V

LDO7 (SLEEP2)

PP3V0_S2_MISC — =PP3V0_S2_COMPASS — 15MA
MAKE_BASE=TRUE
VOLTAGE=3.0V

LDO8 (SLEEP2)

PP3V1_S2_MESA — =PP3V1_S2_MESA — 73MA
MAKE_BASE=TRUE
VOLTAGE=3.05V

LDO9 (SW CONTROL)

PP1V25_REAR_CAM — =PP1V25_CAM_REAR — 360MA
MAKE_BASE=TRUE
VOLTAGE=1.25V

LDO10 (ACTIVE)

PP0V9_NAND — =PP0V9_NAND — 1007MA
MAKE_BASE=TRUE
VOLTAGE=0.9V

LDO11 (ACTIVE)

PP2V6_CAM_AF — =PP2V6_CAM_REAR_AF — 80MA
MAKE_BASE=TRUE
VOLTAGE=2.6V

LDO13 (ACTIVE)

PP2V9_CAM — =PP2V9_CAM_REAR — 47MA
MAKE_BASE=TRUE
VOLTAGE=2.1V
=PP2V9_CAM_FRONT

LDO14 (ACTIVE)

PP1V2_SOC — =PP1V2_LPDP_SOC — 1MA
MAKE_BASE=TRUE
VOLTAGE=1.2V
=PP1V2_PLL_SOC — 22MA
=PP1V2_PCIE_SOC — 37MA
=PP1V2_HSIC_SOC

LDO15 (SLEEP2)

PP0V8_S2_SOC_AOP — =PP0V8_S2_SOC_AOP — 44MA
MAKE_BASE=TRUE
VOLTAGE=0.8V

LDO16 (SLEEP2)

PP1V825_S2_MESA — =PP1V825_S2_MESA — 1MA
MAKE_BASE=TRUE
VOLTAGE=1.9V

VLCM1

PP5V25_GRAPE — =PP5V25_GRAPE — 1MA
MAKE_BASE=TRUE
VOLTAGE=5.25V

CHARGER MAIN

PPVCC_MAIN — =PPVCC_MAIN_BUCK_CPU — 2930MA
MAKE_BASE=TRUE
VOLTAGE=4.5V
=PPVCC_MAIN_BUCK_GPU — 2741MA
=PPVCC_MAIN_BUCK_SOC — 449MA
=PPVCC_MAIN_BUCK_GENERAL — 1264MA
=PPVCC_MAIN_INTERNAL_LDOS — 237MA
=PPVCC_MAIN_LCD — 1371MA
=PPVCC_MAIN_LED — 5MA
=PPVCC_MAIN_MESA — 300MA
=PPVCC_MAIN_WLAN — 1000MA
=PPVCC_MAIN_VDD_LCM
=PPVCC_MAIN_MISC — 5MA
PPVCC_MAIN_ROTTERDAM

BATTERY

PPBATT_VCC — =PPBATT_POS_CONN — 2890MA
MAKE_BASE=TRUE
VOLTAGE=4.7V
=PPBATT_VCC_AUDIO — 3000MA

ON_BUF

PP1V8_ALWAYS — =PP1V8_ALWAYS
MAKE_BASE=TRUE
VOLTAGE=1.8V

BACKLIGHT BOOST

PPLED_OUT_A — =PPLED_REG_A — 150MA
MAKE_BASE=TRUE
VOLTAGE=26V
PPLED_OUT_B — =PPLED_REG_B
MAKE_BASE=TRUE
VOLTAGE=26V

BUCK5 (SLEEP1)