# P75, NV17-Pro, 4MX32 DDR BGA, 64MB, RGB, dual DVI-I, VGA TV-out, video capture, stereo, AGP4X

PCI DEVICE ID 0X0 see strapping options.

**HISTORY:**

```
A01-X00:
  started with P75-A00
  added the TV-out filter to the TV_OUT_CX assembly
  fixed strapping bugs for xtal and rom
  remove the Connexant TV encoder
  add serial termination for the DVO port

A01-X01:
  changed switcher input to 3.3V
  added 2.8V supply for IFPPLLVDD
A01-X02:
  added possible OCSet circuit to Semtech switcher (R640,R641,C640)
A01-X03:
  DVO pinswap
A01-X04:
  fixed 0603 caps on 0402 footprints
```

**PAGE OVERVIEW**


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**13 6.b Analog Power Supply, FBVDDQ**
**14 7 BIOS, Strapping**


| Stuffing Options | Meaning |
|---|---|
| COMMON | the common components |
| 1117 | stuff fixed 1117 linear regulator for analog 3.3V |
| 1117_ADJ | stuff adjustable 1117 linear regulator for analog 3.3V |
| NO_1117 | bypass the linear regulator for analog 3.3V |
| BP_FBVDDQ | bypass the linear regulator for FBVDDQ (=> FBVDDQ=FBVDD) |
| SET_FBVDDQ | set the FBVDDQ voltage (memory IO) |
| SET_FBVDD | set the FBVDD voltage (memory core) |
| SET_NVVDD | set the NVVDD voltage (GPU core) |
| BP_VDD33 | bypass the VDD33 voltage for the GPU |
| VDD33 | stuff the VDD33 regulator components |
| SET_VDD33 | set the VDD33 voltage |
| SC | stuff the Semtech switcher |
| SC1565 | stuff FBVDDQ voltage regulator SC1565 |
| IRU | stuff the IR switcher |
| IRU_VID | stuff the VID setting resistors of the IR switcher |
| IRU_POWSEQ | stuff the power sequencing circuit for the IR switcher |
| VIDCAP | stuff the video capture circuit with SAA7114 |
| TV_OUT_PH | stuff TV-out with the Philips encoder SAA7102 |
| VIVO | stuff video in/out with SAA7108 |
| VGA-B_PROT | stuff the protection diodes around DAC B |
| DVI-I-A_PROT | stuff the protection diodes around DVI-I A |
| VGA-B | stuff the VGA connector at DAC B |
| VGA-B-SYNCBUFF | stuff the sync buffer for DAC B/DVI-I-B |
| DVI-I-A-SYNCBUFF | stuff the sync buffer for DVI-I-A |
| NO_DVI-I-A-SYNCBUFF | bypass the sync buffer for DVI-I-A |
| NO_VGA-B-SYNCBUFF | bypass the sync buffer for DAC B/DVI-I-B |
| DVI-I-A | stuff the DVI-I at DAC A (and the SII164) |
| DVI-I-B | stuff the DVI-I at DAC B (and internal transmitter) |
| STEREOSYNC1 | stuff the stereo synchronisation for DAC A |
| STEREOSYNC2 | stuff the stereo synchronisation for DAC B |
| STEREOSYNCS | stuff the switchable stereo synchronisation |
| STEREO | stuff the stereo circuit |
| A_HPLUG | stuff the hot plug detection for DVI-I-A |
| B_HPLUG | stuff the hot plug detection for DVI-I-B |
| XOR_HPLUG | stuff the hot plug detection for DVI-I-A and B |
| VGA-TV-DVI | use the VGA-TV-DVI bracket |
| VGA-TV | use the VGA-TV bracket |
| VGA | use the VGA bracket |
| DVI-TV-DVI | use the DVI-TV-DVI bracket |
| PASSIVE_HS | use the passive heatsink |
| FAN | use the fan heatsink and stuff all associated components |
| TH_Control | stuff the thermal control circuit |
| MEMORY | the memory stuffing |
| MEM_STRAP_1111 | strap the memory to 1111 (= 4Mx32, 1DQS per 32bit) |
| MEM_STRAP_1101 | strap the memory to 1101 (= 4Mx32, 1DQS per 8bit) |
| NV17-Pro | stuff the NV17 Pro |
| NV17-P-GL | stuff the NV17 GL Pro |


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8867 base on MS-8863, NV17-Pro
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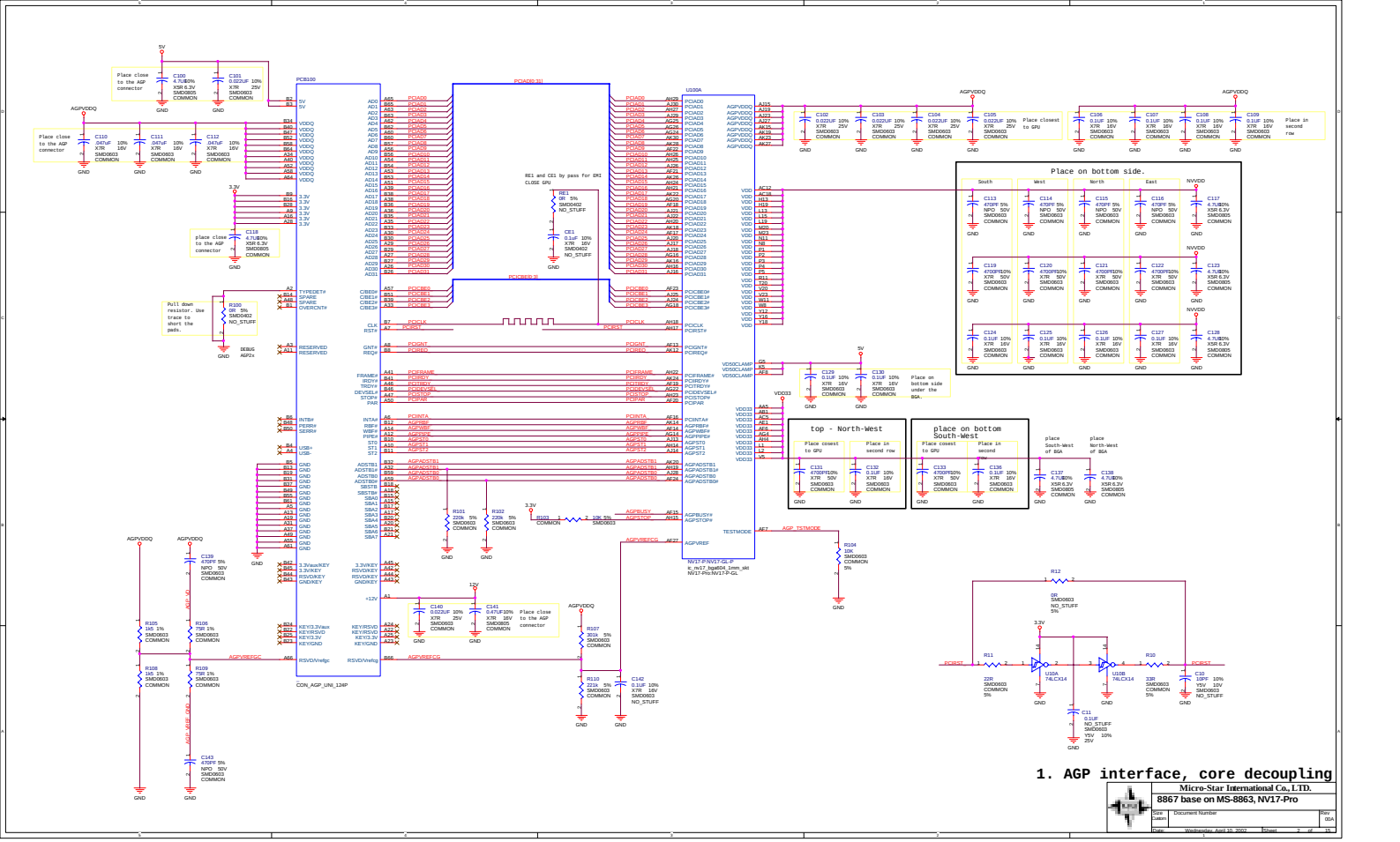
PCB100
U109A
CON_AGP_UNI_124P
NV17-P-NV17-GL-P
Place close to the AGP connector
Place closest to GPU
Place on bottom side.
Place on bottom South-West
top - North-West
Pull down resistor. Use trace to short the pads.
Place on bottom side under the BGA.
1. AGP interface, core decoupling

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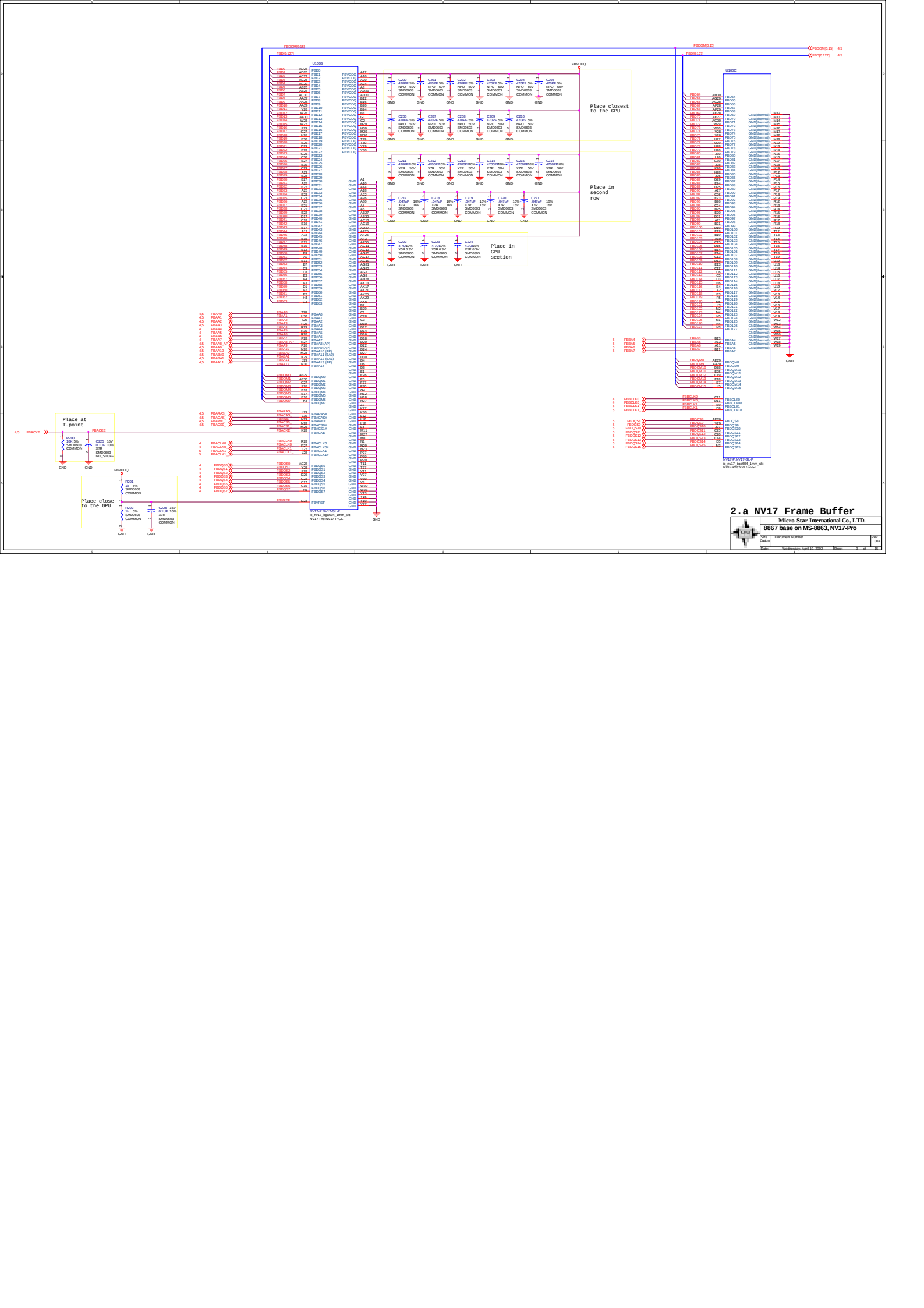
U100B
U100C
FBVDDQ
Place closest to the GPU
Place in second row
Place in GPU section
Place at T-point
Place close to the GPU
2.a NV17 Frame Buffer
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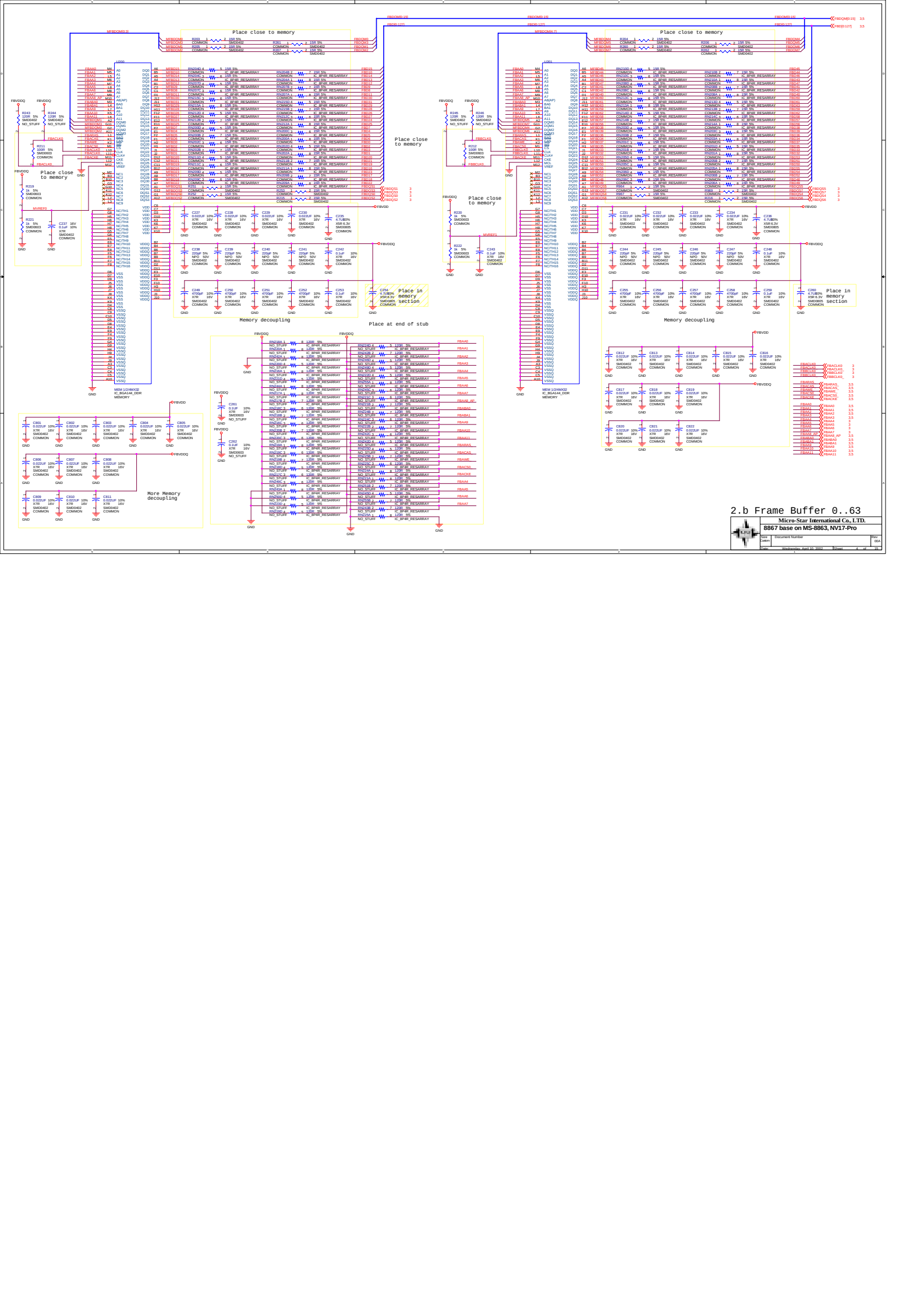
Place close to memory
Place close to memory
Place close to memory
Place close to memory
Place in memory section
Place in memory section
Memory decoupling
Memory decoupling
Place at end of stub
More Memory decoupling
MEM 1/2/4MX32 IC_BGA144_DDR MEMORY
MEM 1/2/4MX32 IC_BGA144_DDR MEMORY
2.b Frame Buffer 0..63
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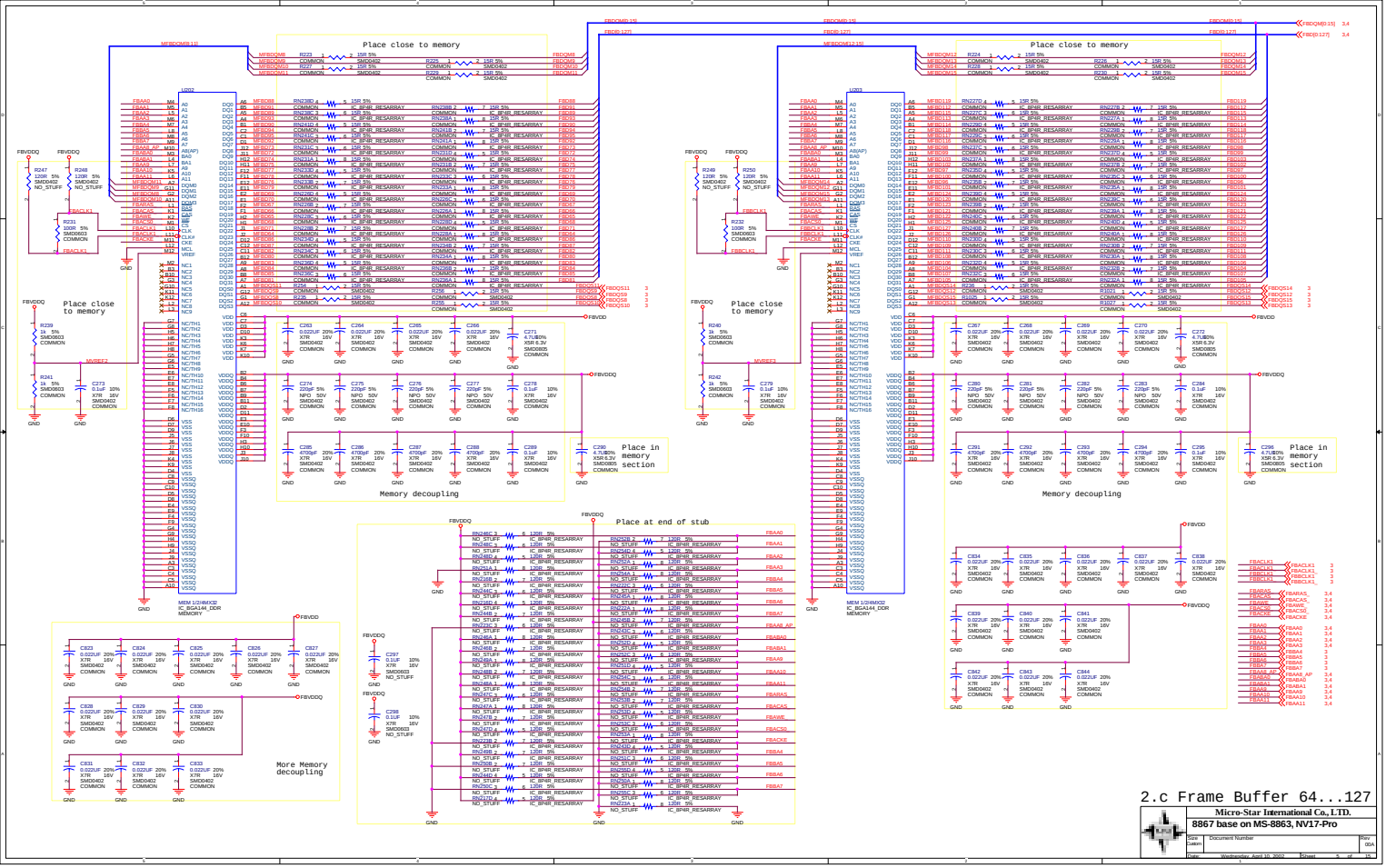
Place close to memory
Place close to memory
Place close to memory
Place close to memory
Memory decoupling
Memory decoupling
Place at end of stub
Place in memory section
Place in memory section
More Memory decoupling
MEM 1/2/4M/X32 IC_BGA144_DDR MEMORY
MEM 1/2/4M/X32 IC_BGA144_DDR MEMORY
2.c Frame Buffer 64...127
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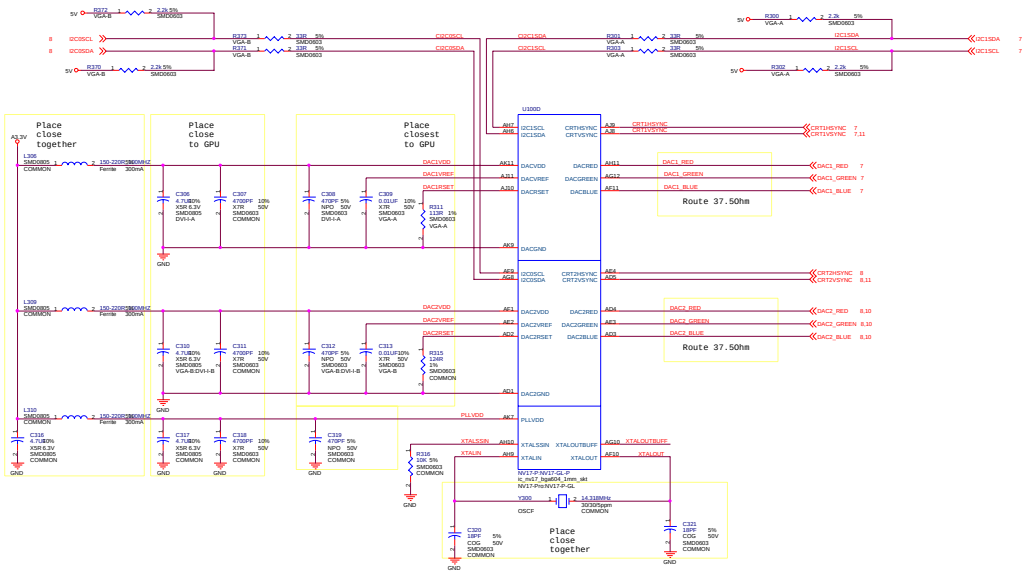
8867 base on MS-8863, NV17-Pro
Wednesday, April 10, 2002




3.a DACA,DACB,PLL,XTAL

| | |
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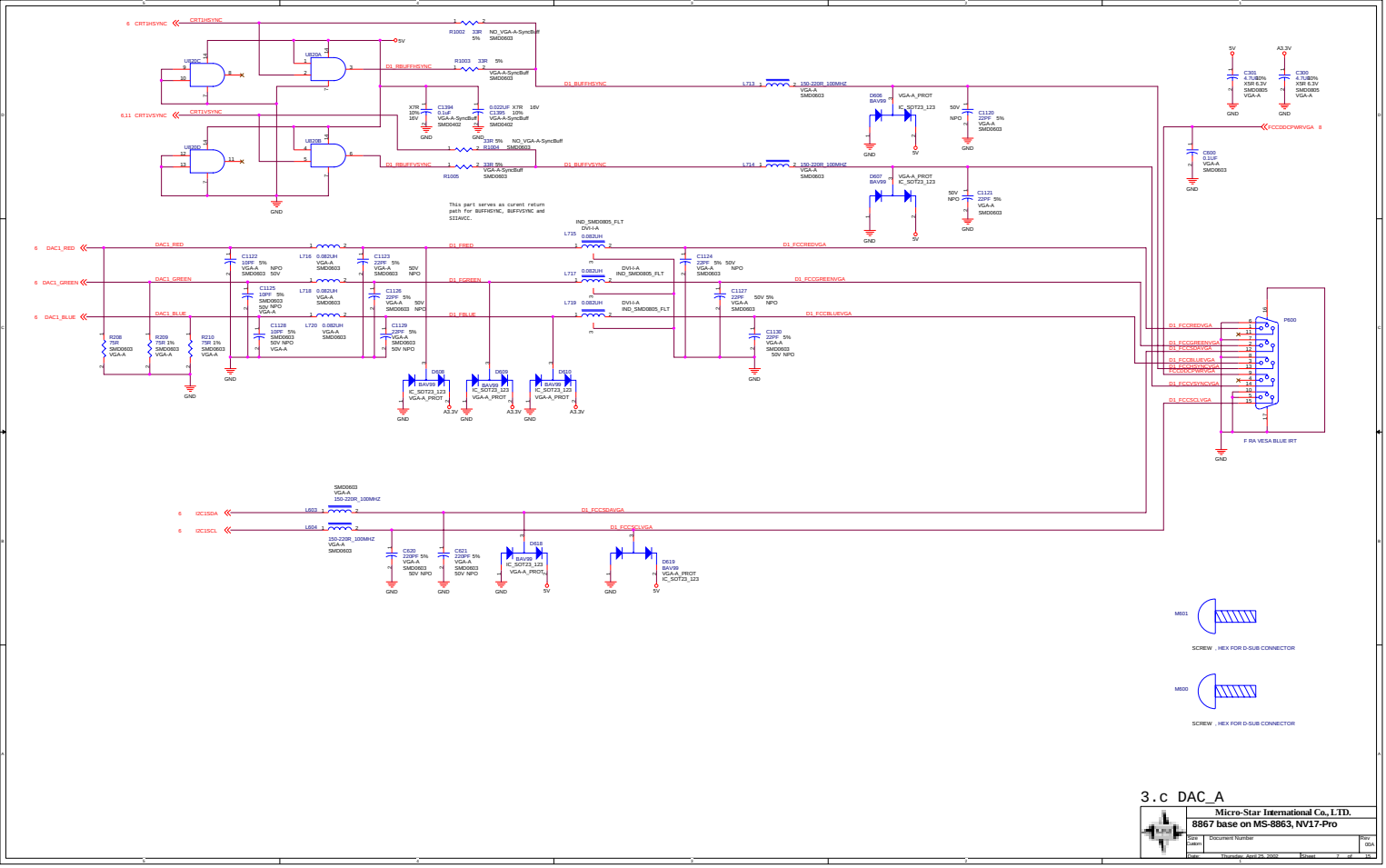


3.c DAC_A

| | |
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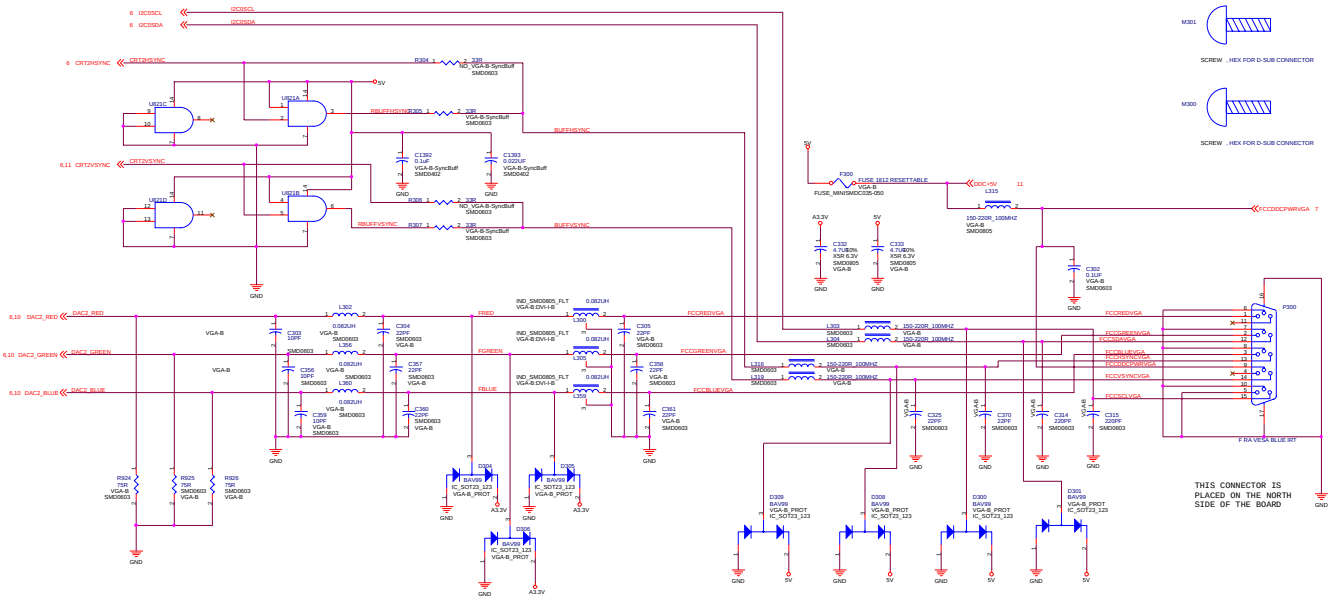


3.d DACB, 2nd VGA

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|---|---|
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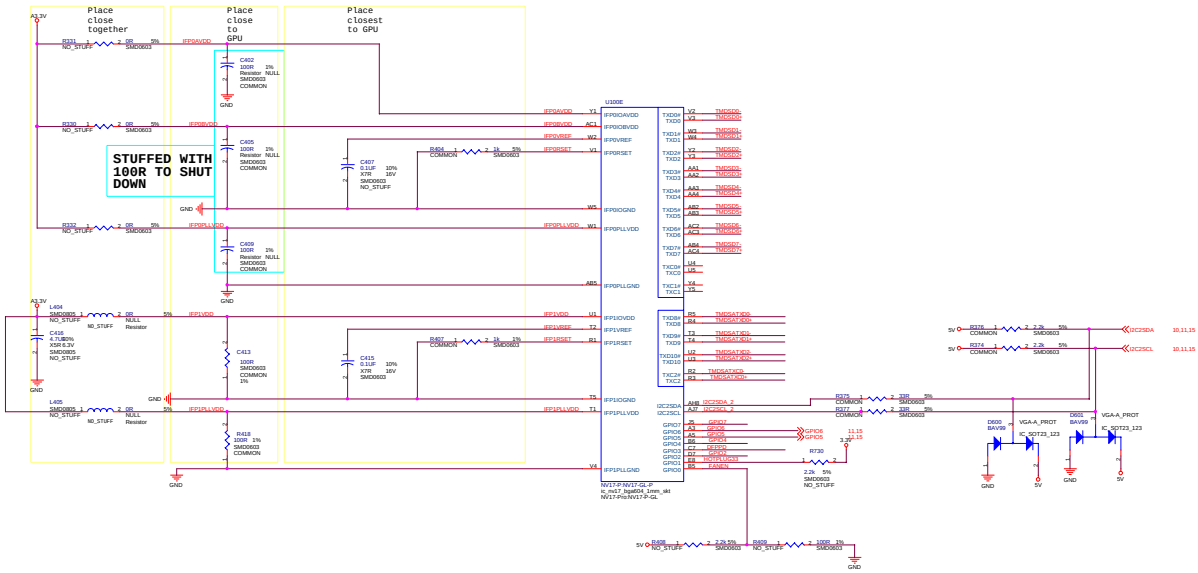


3.e Int Transmitter

| | |
|---|---|
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| 8867 base on MS-8863, NV17-Pro | |
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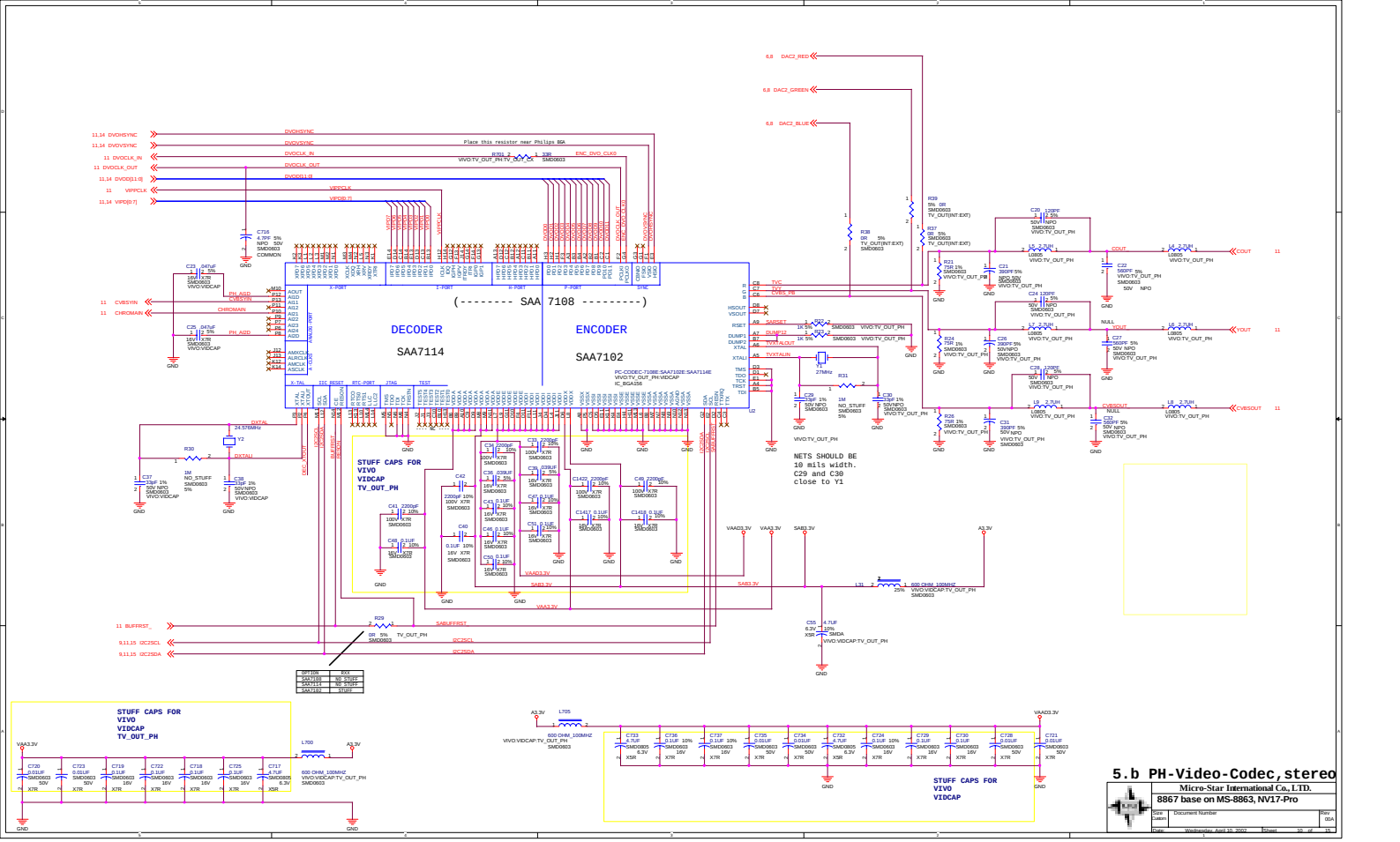
(-------- SAA 7108 ---------)
DECODER
SAA7114
ENCODER
SAA7102
X-PORT
I-PORT
H-PORT
P-PORT
STUFF CAPS FOR VIVO VIDCAP TV_OUT_PH
NETS SHOULD BE 10 mils width. C29 and C30 close to Y1
STUFF CAPS FOR VIVO VIDCAP TV_OUT_PH
STUFF CAPS FOR VIVO VIDCAP
5.b PH-Video-Codec,stereo
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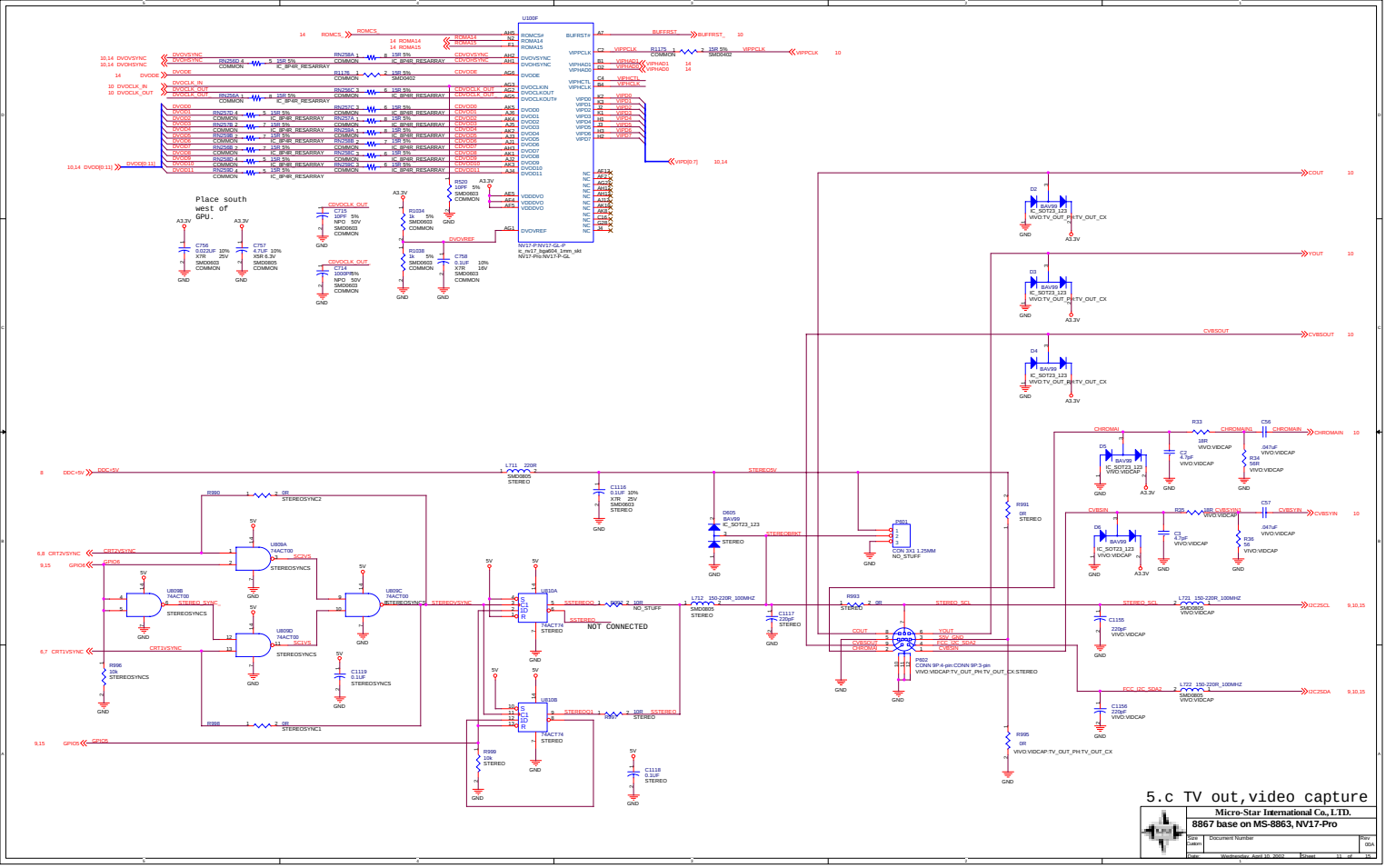
U1009
NV17-P:NV17-GL-P
Place south west of GPU.
NOT CONNECTED
5.c TV out,video capture
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Custom
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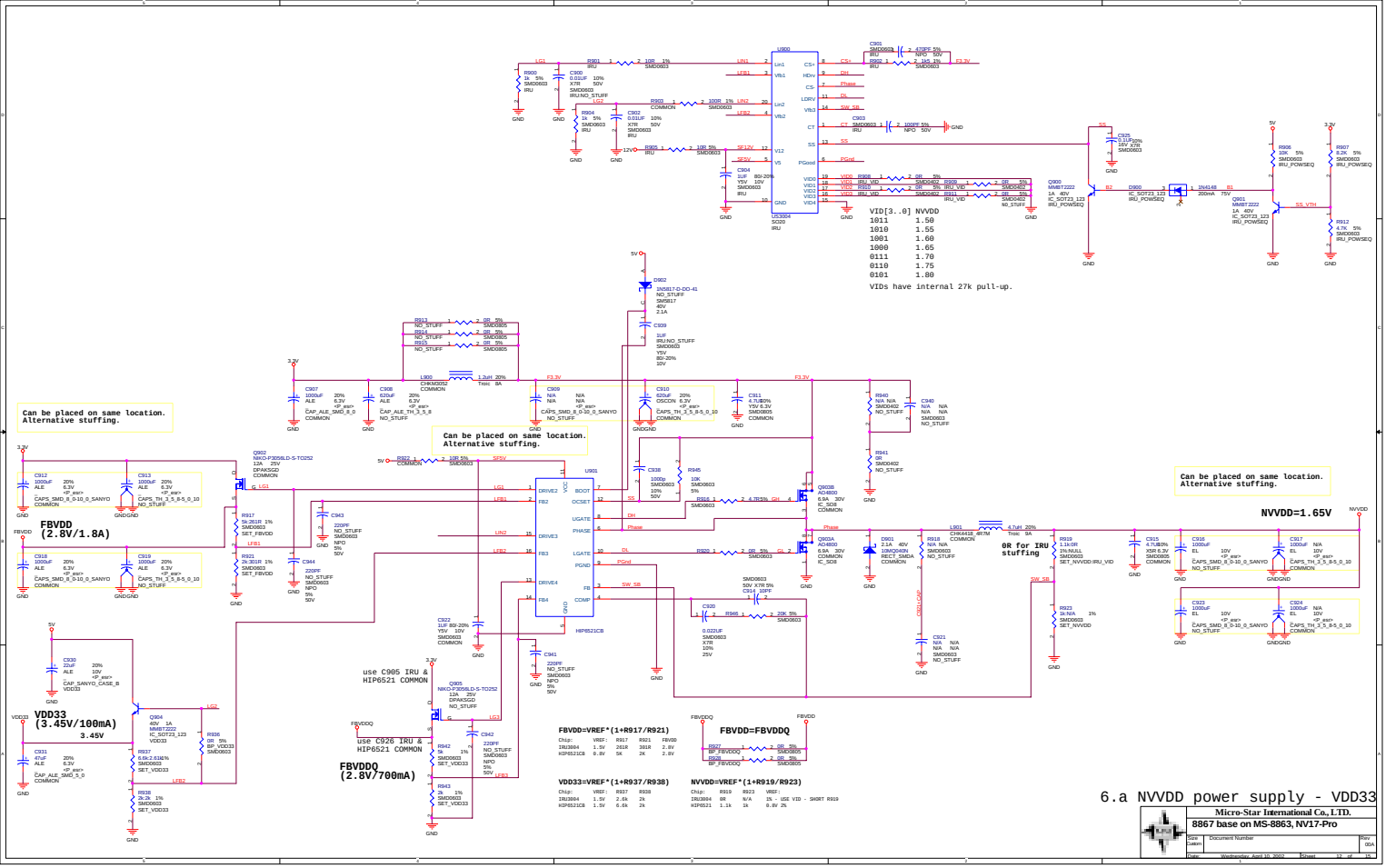


6.a NVVDD power supply - VDD33

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8867 base on MS-8863, NV17-Pro

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|---|---|---|
| Custom | | 00A |

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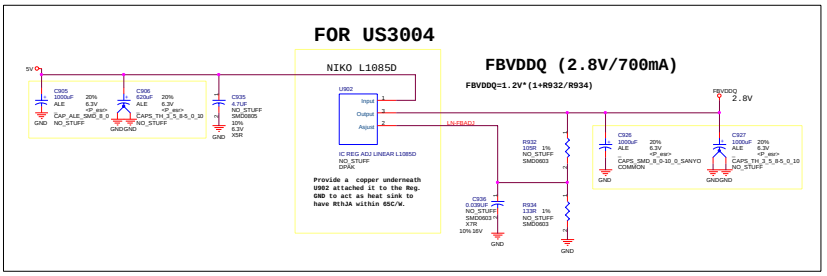


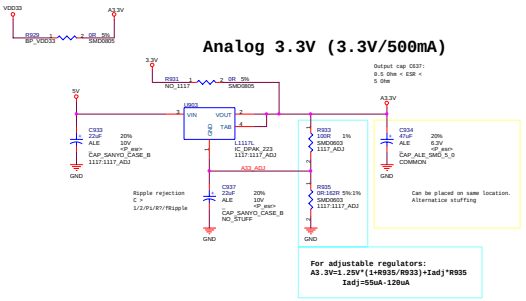


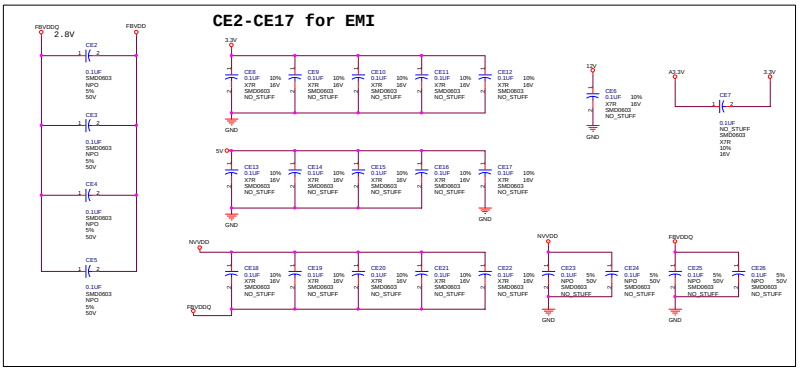


6.b Analog power supply, FBVDDQ

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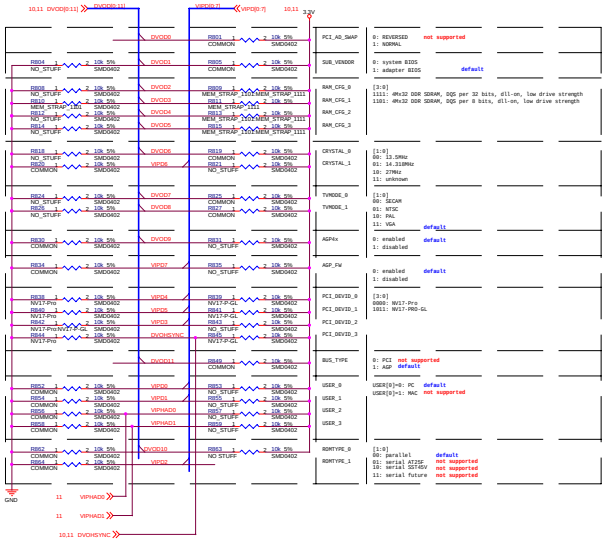
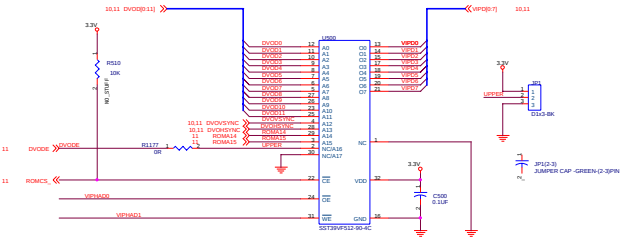
M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11

F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12

## Strapping




# 7. BIOS, Strapping

| | |
|---|---|
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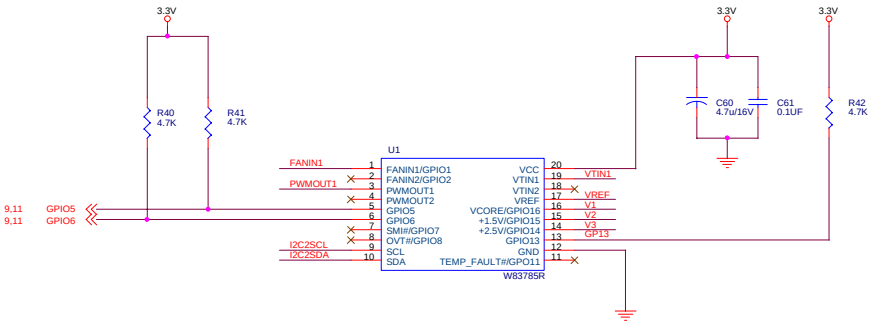
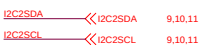
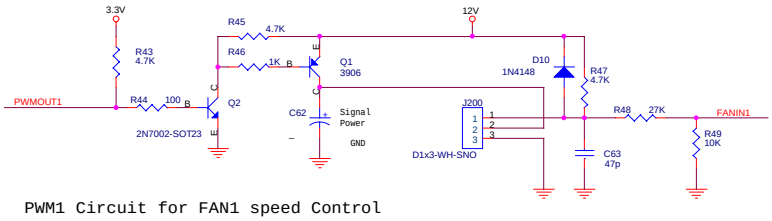
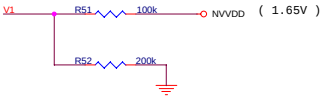


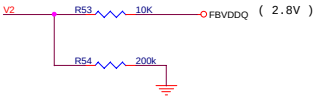



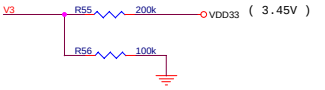




PWM1 Circuit for FAN1 speed Control

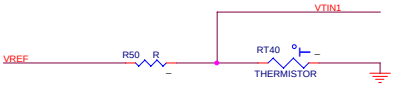
FOR 12V FAN




VOLTAGE SENSORING CIRCUIT




TEMPERATURE SENSORING CIRCUIT

| | | |
|---|---|---|
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