

30P126 - NV30 Production Board

30P126_A04 - NV30 FC BGA, 128MB DDR2 (4Mx32), VGA, External TMDS(Dual-Link)
Internal TV, Philips TV Capture, 2 Firewire Ports

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Calibration Resistors

AGPCALPD_VDDQ	- 50 Ohm to AGPVDDO (0.75v)
AGPCALPU_GND	- 50 Ohm to GND (0.75v)
FB_CAL_PD_VDDQ	- 30 Ohm to FBVDDQ (0.9v)
FB_CAL_GND	- 30 Ohm to GND (0.9v)
FB_CAL_CLK_VDD	- 55 Ohm to GND (1.2v)
FB_CAL_TERM_GND	- 50 Ohm to GND (0.45v) (or something close)
SAGPICALPD_VDDQ	- 50 Ohm to SAGP1VDDO (0.75v)
SAGPICALPD_VDDQ	- 50 Ohm to SAGP1VDDO (0.75v)
SAGPICALPU_GND	- 50 Ohm to GND (0.75v)
SAGPICALPU_GND	- 50 Ohm to GND (0.75v)
D1D2_CAL_PD_VDDQ	- 50 Ohm to VDDQ
D1D2_CAL_PD_GND	- 50 Ohm to GND

GPIO Assignments

Desktop	SKU	Type	Function
GPIO_0		IN	Not used
GPIO_1		OUT	Hot Plug/Unplug from DVI- Secondary -Bottom Fan PWM Control, LOW=FAN off, HIGH=FAN on LOAD_TEST (Quickswitch)
GPIO_2		IN	Not used
GPIO_3		OUT	Select NUUDD USEL0
GPIO_4		OUT	Select NUUDD USEL1
GPIO_5		OUT	SEL_2ND_DEV (Quickswitch)
GPIO_6		OUT	GPU_SLOW_MODE*(THERM_ALERT*) & EXSENSE
GPIO_7		OUT	External 12V sense (EXSENSE)
GPIO_8		IN	
GPIO_9		IN	

Connector I2C Assignments

Display Connector	NV30 Output	I2C Channel
VGA/DVI-I (south) DIN	DAC A + DVO A	A/B/C

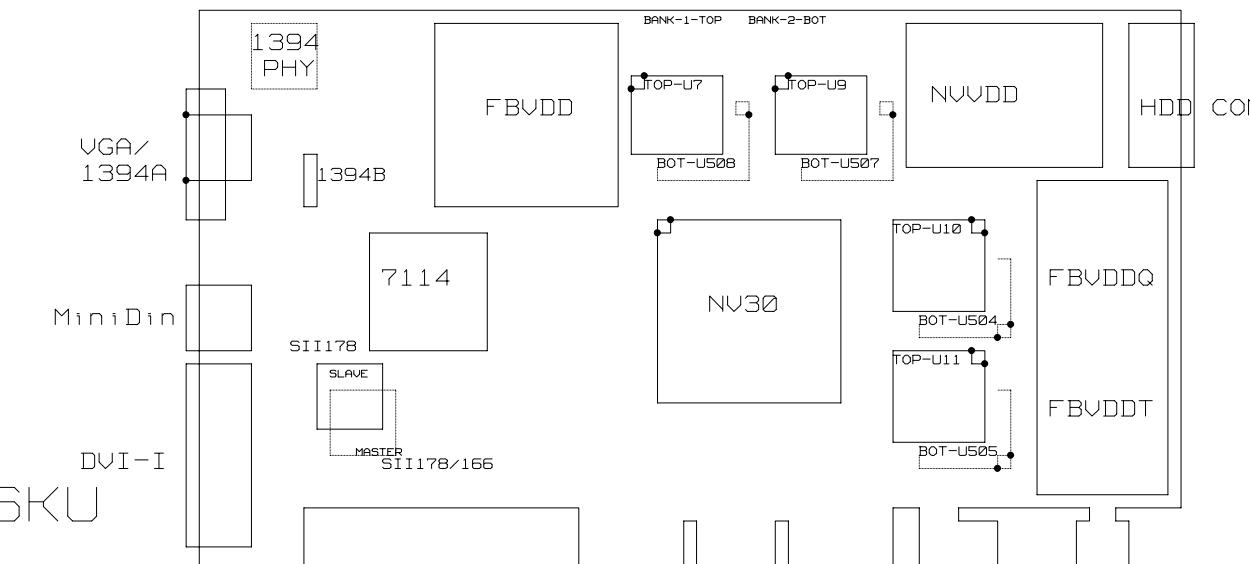
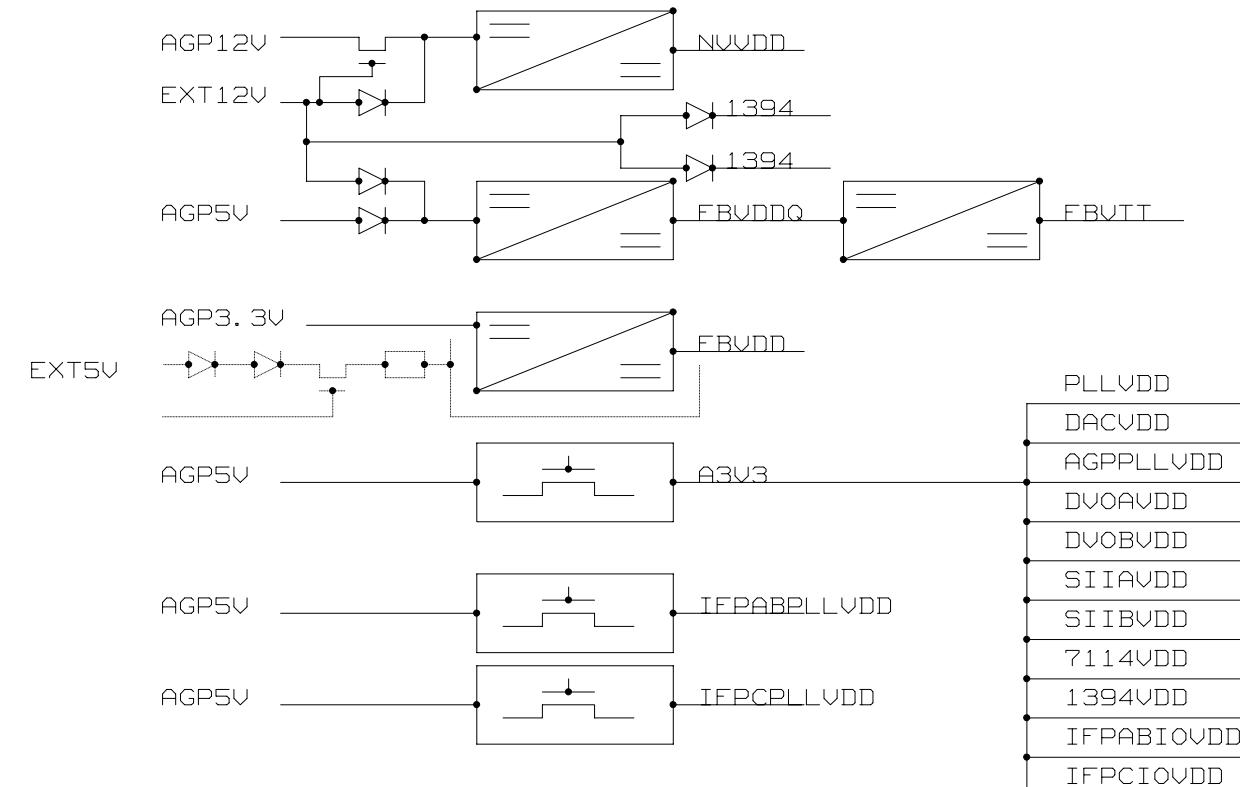
Dual DVI and TV out only SKU

* * * NOTE: * * *

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SKU SCHEMATICS ALONE WILL HAVE "NO STUFF" ASSEMBLY PROPERTY
Base SCH 602-10126-0000-004 SCH Ver: 03

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Power Topology



History: P126-A00

X01 - 8/08/02	- Created 30P126 from 30E121. Stopped work on E121 for now. - Stripped out unrequired components - Stripped out some extra FBVDD/FBVDDQ decoupling caps - Renamed Internal TMDS to TP...
X02 - 8/09/02	- Added Res on PCIINB - Removed Diffpair rules for Internal TMDS. Remember to put them back for E121. - Made some changes to fix our implementation of TMDS Backdrive
X03 - 8/12/02	- Replaced Fuse for NVUDD Power Supply - Added Second Package for PGOOD chip - Renamed nets for DIO0 to NTP - Added Pair for Bracket (Currently just a placeholder) - Added Diode and Diode Bypass for TMDS Backdrive - Fixed DVOB Strap bits - Removed TestPoints for NVUDD VID pins
X04 - 8/13/02	- Added NET_SPACING RULES for DAC - Removed FRMR_PME# trace - Adding Spacing Rules for PLLVDD - Fixed issues with remaining nets - Changed AGP_VDD to 5V instead of 3.3V (routing is better) - changed AGP_PLLVDD to use 3.3V instead of A3V3 (routing is better) - Removed A3V3 decoupling around DACA, replaced with single 5V decoupling cap - Removed two CGND to GND Resistors - Fixed problem with extra AND gate
X05 - 8/14/02	- Changed AGP_PLLVDD back to A3V3, pending further notice - Added Caps to 12V and FBVTT for the AGP section - Removed one cap from FBVDDQ - Changed Bracket to correct symbol 1. Added ISL6225 Enable pull up resistor and one decap. 2. Changed 6529-ISEN resistor to 2.2k 3. Changed pull down res to AGP12V FET to 0402 4. Changed 6529-Freq res to 49.9K 5. Added more NVUDDPS nets constraints, remote sense as diff pair. 6. Changed small cap voltages to min. 6225 7. Boot cap voltages change to 16V from 10V -OK 8. OCSET1 resistor changed from 49.9K to 49.9K 9. Added R option to use Inbuilt VDDQ/2 ref for VTT 10. Renamed nets as per function 11. Risen and Roc to be finalized.
X06 - 8/15/02	- Updated External Power Connector - Removed NV_PGOOD from FBVDD power supply ExtSense logic 1. Change to strong pull down for EXTSENSE, to 0402 from 0603 . 2. EXTSENSE buffer pull up to 0402 from 0603 3. Change EN_GPIUSLOW series resistor to 0R/0402 from 51R/0603. POWER_SUPPLY 1. Removed R151 0R/0402 on RESET_BUF* 2. Add note to place FRWRCLK, R68 close to PHY Power supply 1. 6529/6225 Voltage divider values for Vout changed/updated
X07 - 8/17/02	- Updated Power Supply_Select Options - Updated NVUDD Power Supply to use DPAK FETs - Moved C112 from 12V to 5V (Due to plan changes)
X08 - 8/20/02	- Cleaned up some of the Physical Rules - Updated with some symbols with Release candidates - NVUDD PS: Swapped PWM's for better routing 1. Cleaned up for assembly/n/a 2. Updated compensation values for NVUDD
X09 - 8/21/02	- Replaced Dual-FET on FBVDDQ to 2 Single S08 FETs 1. Update 6529 Compensation Values-C1,C3 need new P/N 2. Corrected 6225-FBVDDQ comp cap connection from Rbot to Rtop
X10 - 8/22/02	- 1. Update with new Roc, Risen for 6225, Update Comp values for 6529
X11 - 8/23/02	- Added NVUDD caps according to Ross's Power Analysis
X12 - 8/26/02	- Added FRWR_VDD to improve plane in 1394 section - Added more NVUDD caps - Added FBVDD Current Supplement Circuit
X13 - 8/28/02	1. Delete pullup(R268) to ISL6536 EN pin. Connect directly to 3V3 2. Clamp EXTSENSE to SV from 3V3. 3. NVUDD Comp note removed. 4. FBVDDQ Dual FET diode note removed 5. FBVDDQ voltage divider changed from 10K to 1.5K. 6. Added note for Shmoo 7. Added 0R for DDC_5V_R from DDC_5V 8. Changed 2nd from FAN1_CTRL to FAN2_CTRL. 9. Rename FAN1_CTRL to TP_GPIO0 10. Delete R248(LCD_BACKLIGHT) 11. Delete R248 on GPIO2 12. Delete R229 and LCD_POWER net 13. Rename VTG_RST to TP_GPIO4 14. Pull up R338 on EXTSENSE to SV instead of 3.3V 15. Change R16 from 0R to 47R 16. Change R338 Extsense pull up from 10 to 15K. 17. Delete LCD_POWER and R229 18. Delete R03 and R230 19. Delete R248_0R between VSEL0 and SEL_2nd_DEVICE 20. Delete R252_0R on VSEL0 and GPIO5, Delete GPIO5. 21. Add 0.1uF for SST flash. 22. Add * to default straps. 23. Add off page connection to strap signal nets. 24. Add a edge rate control cap for FANI_CTRL control signal 25. Thermal diode polarity reversed as per naming 26. DVDA and DVDB bus naming screwed in symbol, Partially corrected.
X14 - 8/29/02	1. Thermal diode polarity naming is wrong, change back connection. 2. Added notes for Fansink,screw back plate. 3. Change note for right default for FB size, Dual link TMDS 4. CGND_VGA_SLIM deleted and connected to CGND 5. MCHIP_RST changed to MCHIP_RST* 6. Changed Master/Slave strap resistors for SII178 7. DVDA/CLKOUT, DVDB/CLKOUTx to 0R from 33R 8. FBVDD 13 caps added 9. Updated block diagram for Ext 5V to 3.3V
X15 - 8/31/02	1. Added option to control all VIDx by VSEL0 and VSEL1. Added 5 0402 resistors 2. Deleted E121 Mobile FET used for GPU_SUS_STAT* 3. Renamed GPU_SUS_STAT* as GPIO6_VSEL1, VSEL0 as GPIO5_VSEL0
X16 - 9/3/02	1. Deleted R378 extra pullup to 2nd FAN drive, Add spacing rule for PWM signal

X17 9/4/02	1. Delete resistor option Vid4 for VSEL0, Vid0 for VSEL1, these are not practical options. 2. Change R154 to 0R Common from 20K, Nostuff. 3. Change Assembly for VIDx pull down resistors. 4. Change property to net Gate drive ckt of 6529, NV_UGATE1, NV_UGATE2, NV_UGATE1_R, NV_UGATE2_R, NV_LGATE1, NV_LGATE2, NV_LGATE1_R, NV_LGATE2_R from 16mil to 24mil trace. 5. Add a 0.22 and 0.02 resistor to internal FBVDD supplemental power using 6529_PGOOD. 6. Change property to nets Gate drive ckt of 6529, 6529_SW_DRH1, 6529_SW_DRLO1, 6529_SW_GH, 6529_SW_GL from 16mil to 24mil trace. 7. Modify Partnumber for EEPROM U23, U22 with preprogrammed. 8. Update Firewire Diffpair spacing rules
X18 9/5/02	1. DVI connector data lines corrected as per new Master/slave SII178. 2. Modified Supplemental power(3.3V) gate drive circuit, Added one Tr and 3 resistors. 3. Made all Refdes as Hard locations. 4. Added 4 1210 caps for FBVDD to be under Heat sink 5. Added 2 1210 caps for FBVTT.
X19 9/6/02	1. Added GPU Dev ID, changed default to 0x301.
X20 9/9/02	1. Changed in VGA1, from common GND to individual GND return nets
X21 9/10/02	1. Changed FP STRAP to 12bit for External Dual link also. 2. Changed Memory FBVDD, FBVDDQ Decap values as per SI-analysis decap layout(last 3 pages). 3. Changed EXSENSE pull down to 5.8K from 1K. This was causing IV potential divider
X22 9/10/02	1. Removed Vtt to Vref circuit for FB - Removed ISL3536 Alternate part (MSOP8 package) - Changed Capacitor Values for FBVDD and FBVDDQ to meet Ross's Power Integrity results(1st page)
X23 9/11/02	1. I2C_C was clamped wrongly to 3.3V, changed to 5V. 2. Changed Dual Link TMDS1SEL/RST# pin from SIIA_VCC to RESET_Buf*
X24 9/12/02	1. Temperature sensor is MAX6649(145C) instead of AD1032(125C) 2. Thermal diode symbol was wrong, corrected symbol and connections
X25 9/16/02	1. Moved X-Cap voltage from 5V to 12V, FBVTT to 3V3 for AGP traces
X26 9/17/02	1. Deleted X-Cap for AGP traces, the plane split was moved away. 2. Added 0402 series resistor to net GPIO2_FAN_CONTROL.
X27 9/19/02	- created CGND2 for Slim-VGA
X28 9/20/02	1. ISL5225 Boot diode pin 1&2 swaped during symbol updated, corrected now. - changed C694 from 0B05 to 0B03 so that the heatsink can fit without a cutout in that area
X29 9/21/02	- Added 1K Resistor to Quickswitch circuit
X30 9/22/02	- Made NTP net's on DVDB to TP (needed for ICT) - RESEQUENCED THE BOARD & SCHEMATICS RefDes
X31 10/01/02	1. Change C885 from No stuff to Common, value changed 0.1uF to smooth the Power good output. 2. Delete empty page #15.

History: P126-A01

X01 10/08/02	1. Add pullup and pulldn for Master SII178 to support SII164/166 in the same location 2. Dual Mode Strap for Slave SII187 was tied to SIIA_VCC(3.3V), now connected to SIIA_VCC(3.3V)
X02 10/09/02	1. Change AGP CAL PU/DN is changed from 56ohm to 50ohm parallel combination.
X03 10/10/02	1. Stuff AGUREFCG circuit and Change R594 from Nostuff 121K to stuff 158 K. Vref=350mV
X04 10/12/02	1. FBVTT cap values as per SI- C728, C729, C730, C731 from 1000F to 2.2nF C749, C773, C597, C585, C560, C521. 0.01uF(10nF) to 0.022uF(22nF) 2. Add more clarity to block diagram.

History: P126-A02

X00 10/14/02	- Created New project from A01. Add min PCICLK length Constraint.
X01 10/15/02	1. Update netnames for E-Tools
X02 10/20/02	- Change TMDS Termination from No-Stuff to Stuff (NUPN 195-23000-0003-000) - CB7 - 1UF 0B05 Cap on 12V AGP from 036-30105-0076-000 to 036-30105-0057-000
X03 10/24/02	1. Replaced various not for new design parts(147 error) 2. Connect un-used PG chip input to 3.3V rail as per Intersil recommendation - Add 12V pull up and pull down as per Intersil on power good chip o/p. To be used when no PG chip. - Add series termination res to FRWR interface.
X04 10/25/02	1. Add an adjustable LDO for DVDA_VDD rail to provide 3.0V from AGP3.3V rail 2. Add a decap for FB_CAL_CLK_GND, FB clock Bias pin. 3. Change R31 to 1K from 6.8K, R753 to 3.3K from 10K so the EXT_SENSE signal falls low quickly(< 650uS). 4. Add more notes for EXT_SENSE and GPU_SLOW_MODE signals usage for s/w.
X05 10/26/02	1. Change FB Vref voltage divider from using 120R to 1K.
X06 10/28/02	1. C658 was No stuff, change it to stuff, it is not under Heat sink. 2. Update Remote sense cap assy as per layout and bom.

History: P126-A03

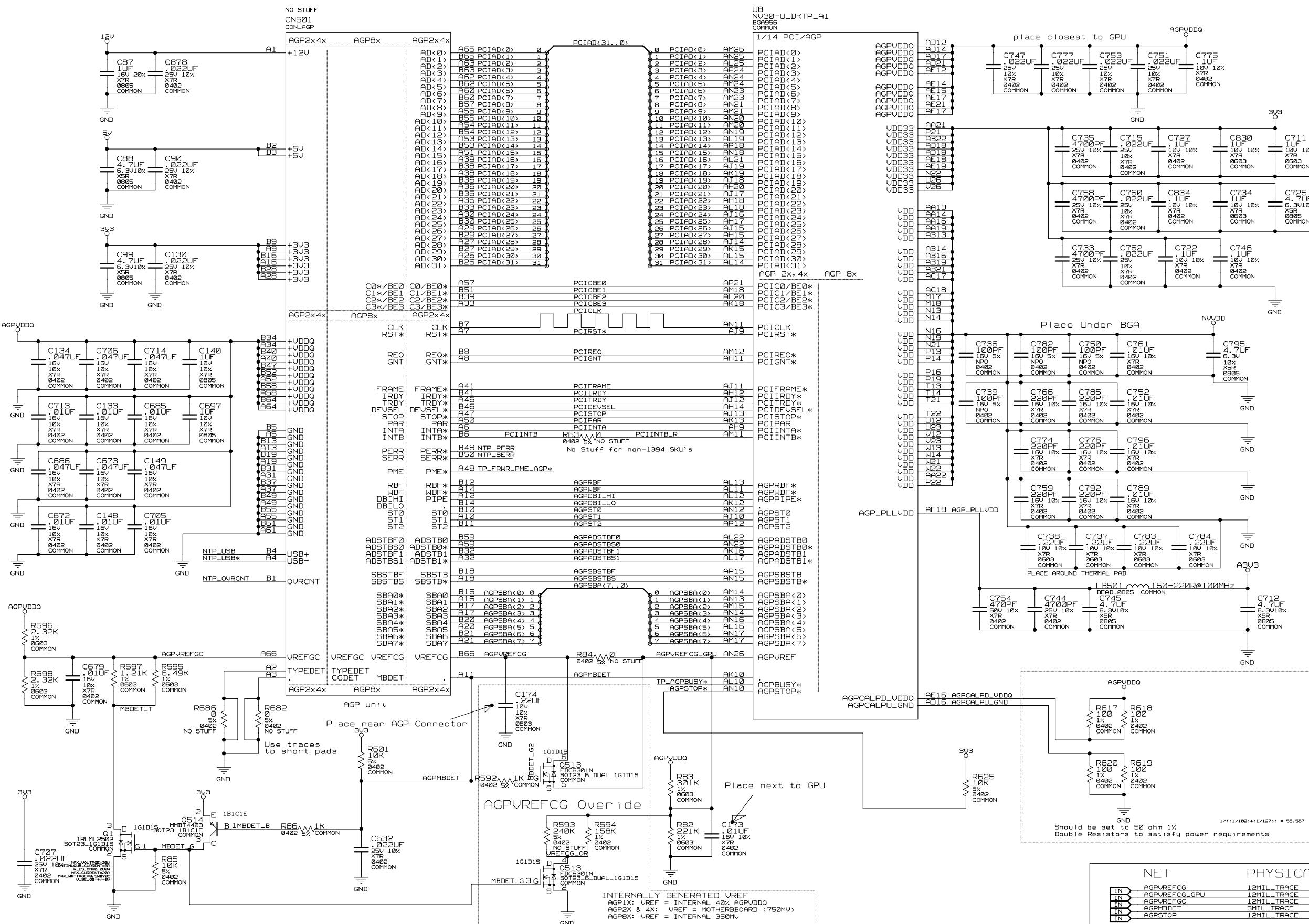
X01 10/30/02	1. Change C737, C738, C783, C784 to 0603 from 0402 2. PCB A02 was not gerberized correct, corrected PCB is A03. Rolling SCH for A04
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History: P126-A04

X00 11/04/02	1. Change U506 to 0.5% part
X01 11/05/02	1. Change NVUDD compensation to R608,R589,C598 to No stuff, C604 =0.1uF, R573 = 39K. 2. NVUDD, FBVDD Inductor of 3mohm type from 6mohm type. 3. Change FAN circuit CAPs to 0B05 from 0B03.
X02 11/07/02	1. Do changes for Barry III, FBAL-357ohm, Add 1pF cap for FBUREF. 2. No stuff CLK_Bias cap. DANGER.
X02 11/08/02	1. Add a diode in parallel to Q507, Change R536, FBVDDQ OCset to 56.1k from 95.K

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DETAIL	DRAWING DETAIL
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1. a. AGP 8X Interface



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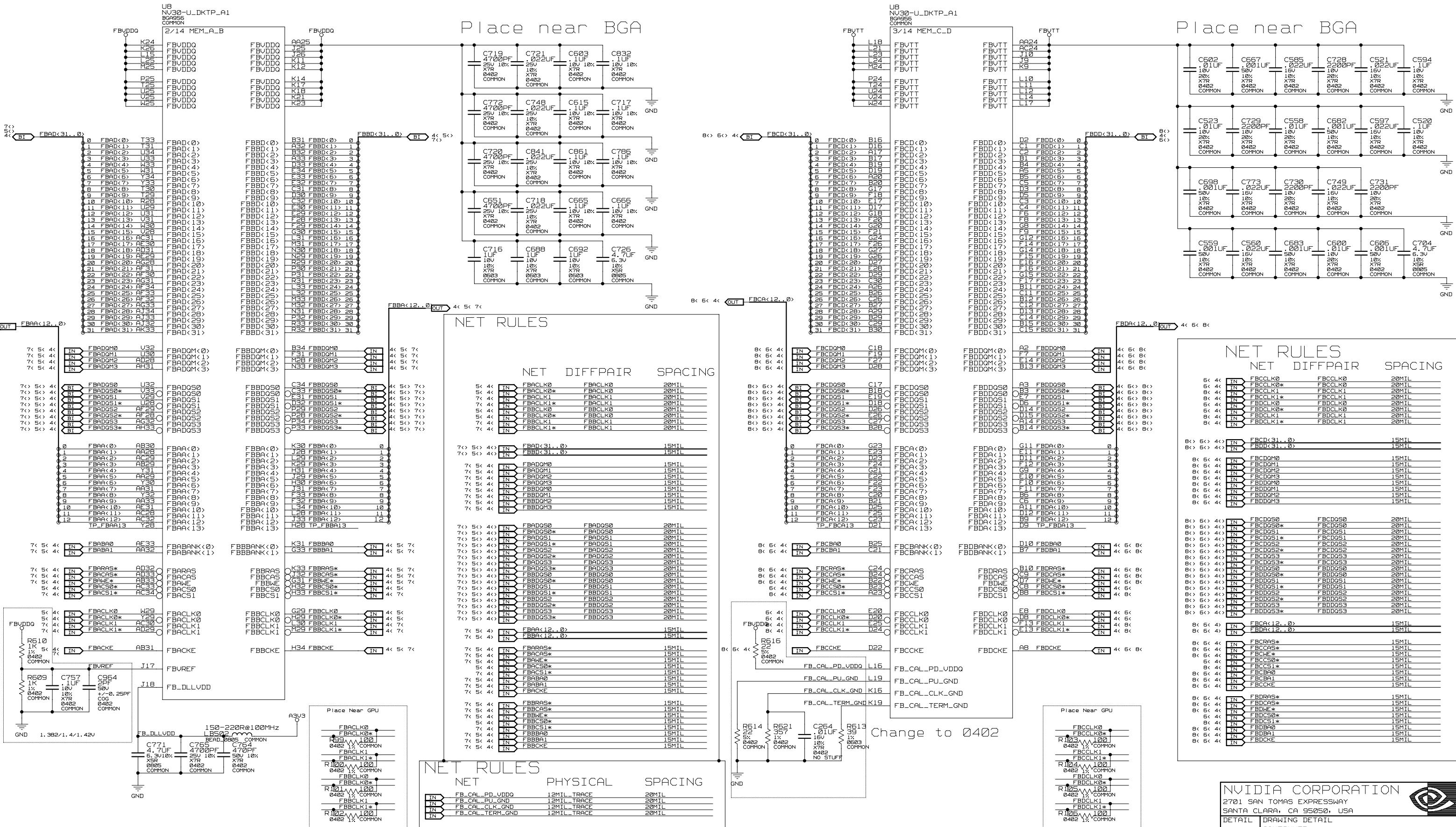
	NET	PHYSICAL
TN	AGPREF CG	12MIL_TRACE
TN	AGPREF CG_GPU	12MIL_TRACE
TN	AGPREF GC	12MIL_TRACE
TN	AGPMBDET	5MIL_TRACE
TN	AGPSTOP	12MIL_TRACE

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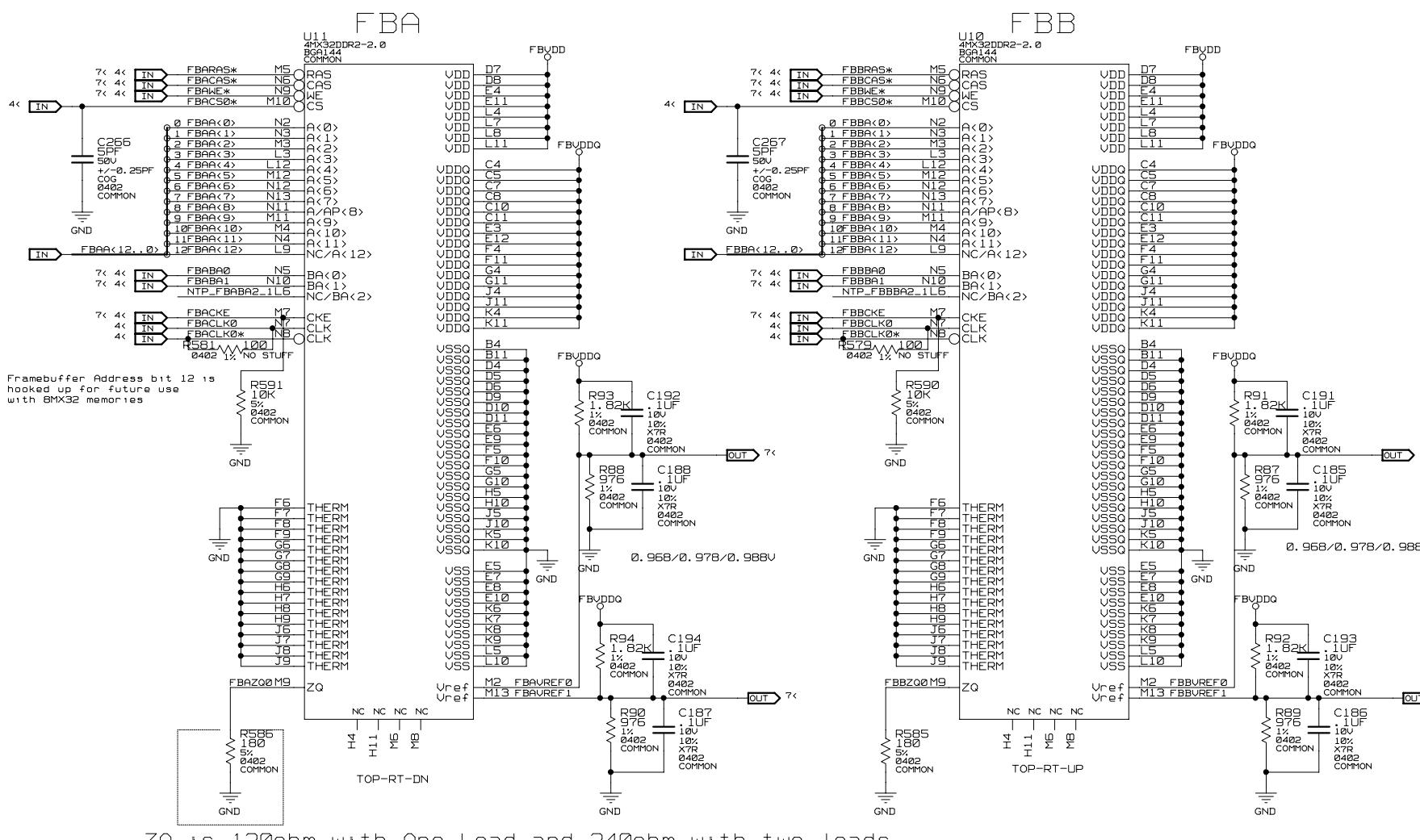
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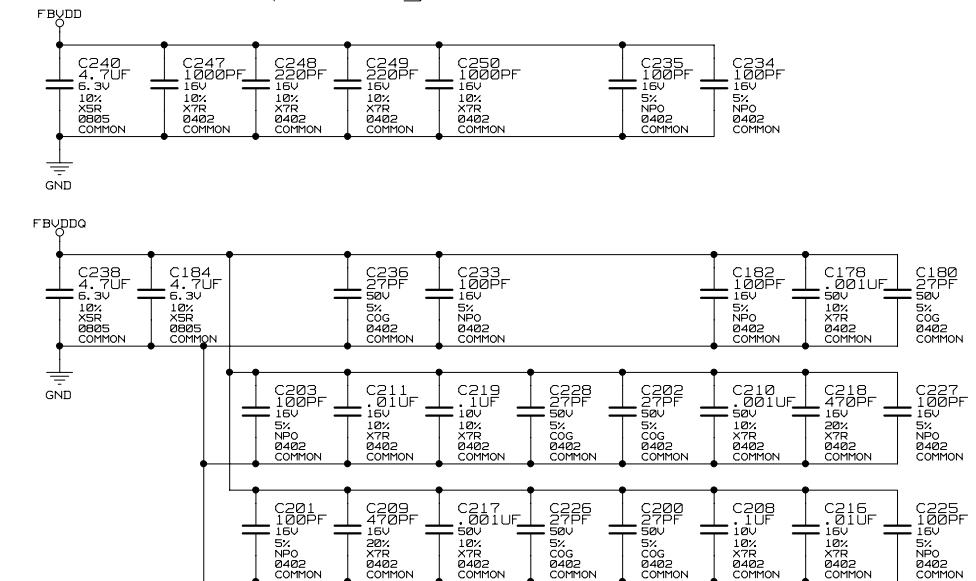
2. a. Memory



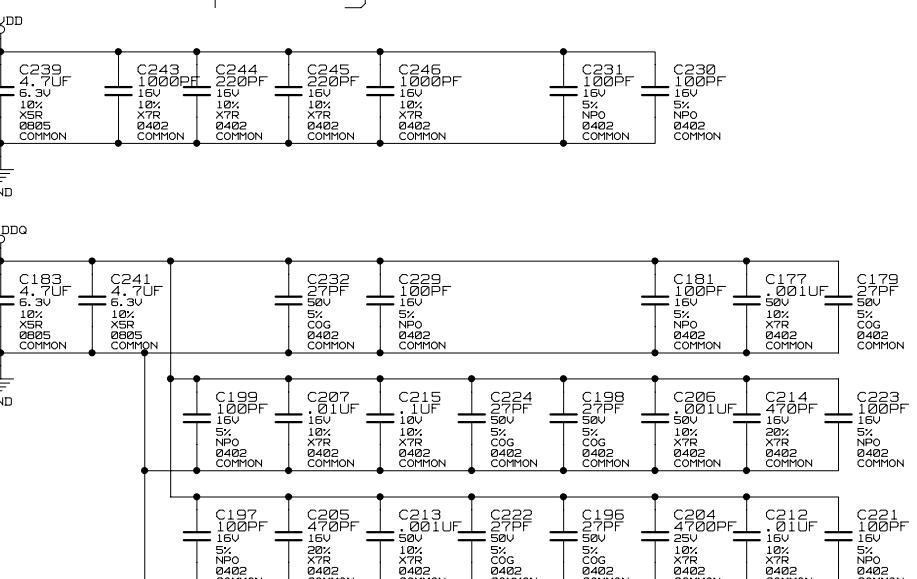
2.b. Memory: Bank 1: FBA & FBB



Decoupling for FBA

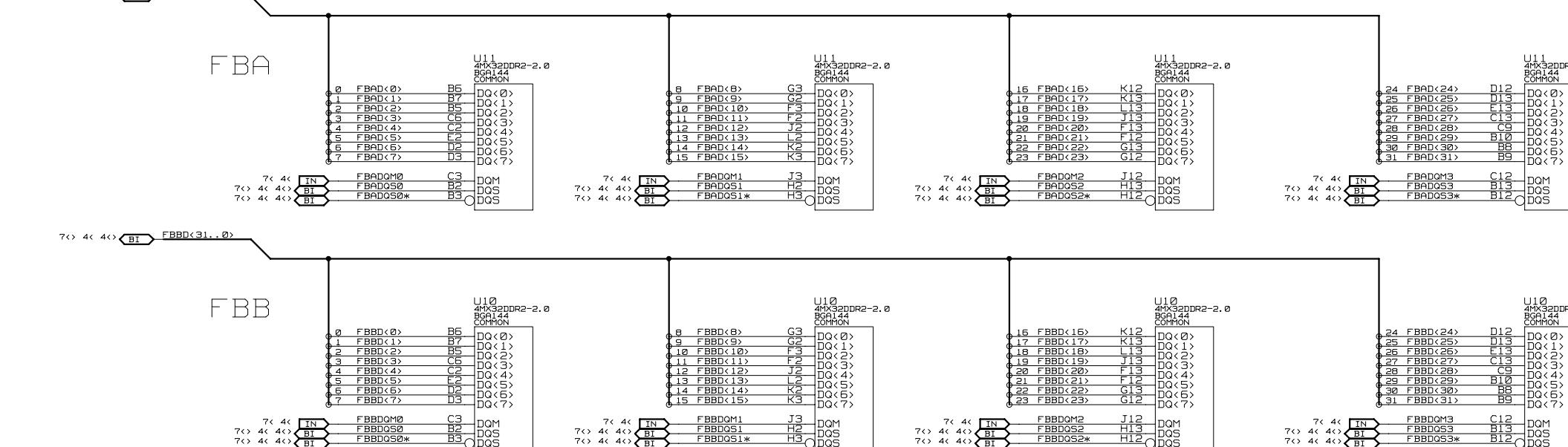


Decoupling for FBB



FBA

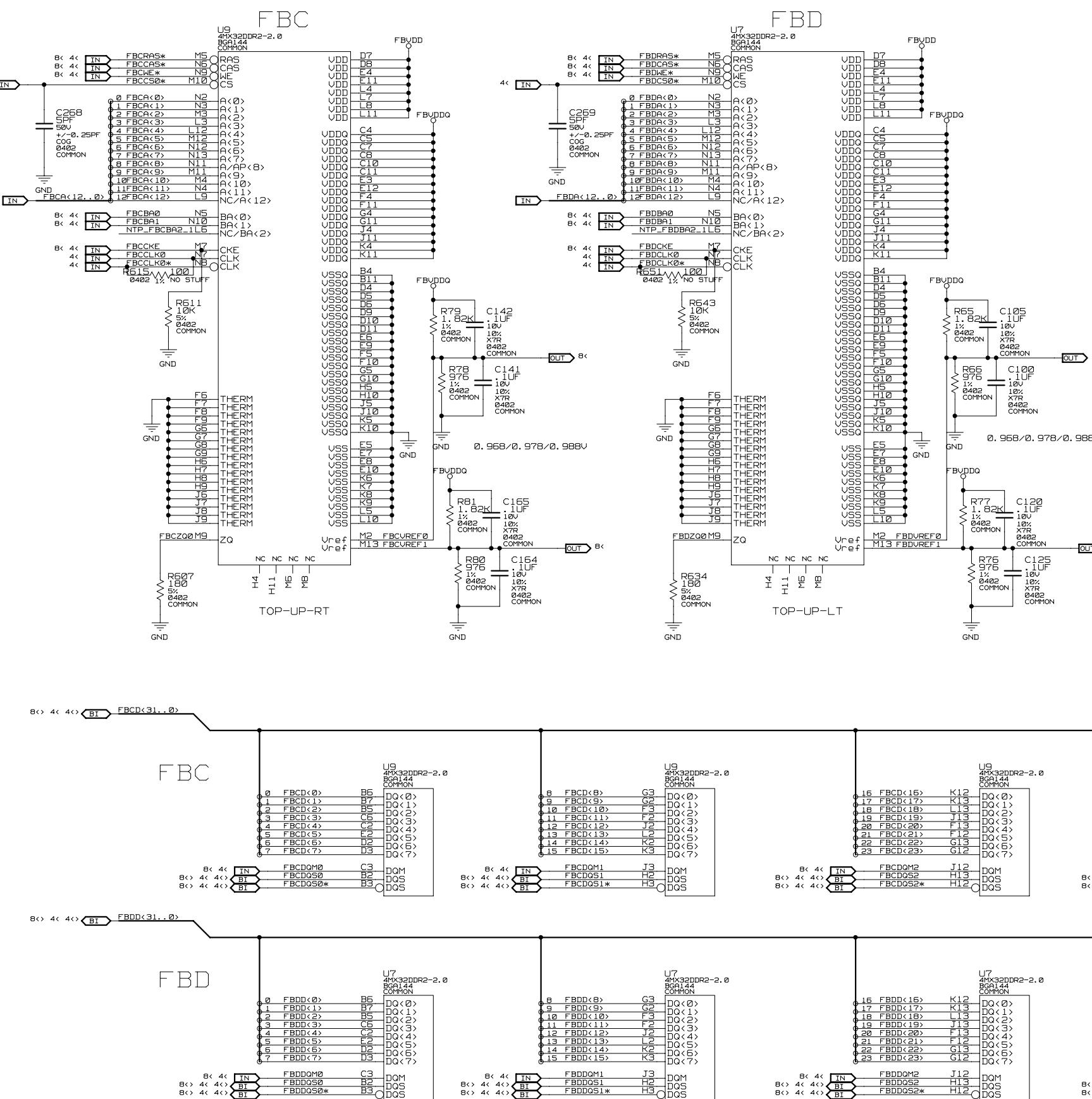
FBB



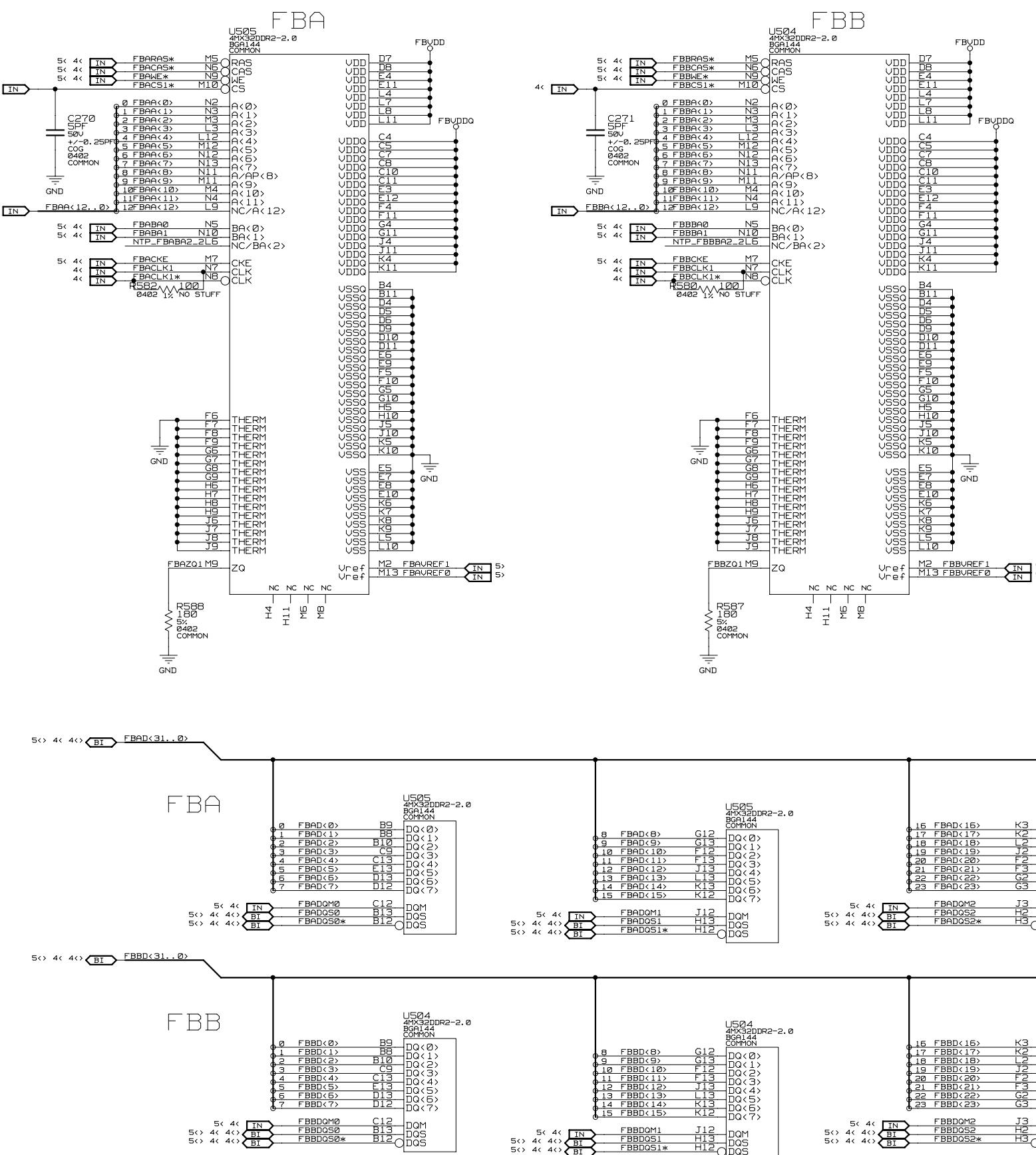
NET RULES
NET PHYSICAL

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DETAIL Memory Page 1
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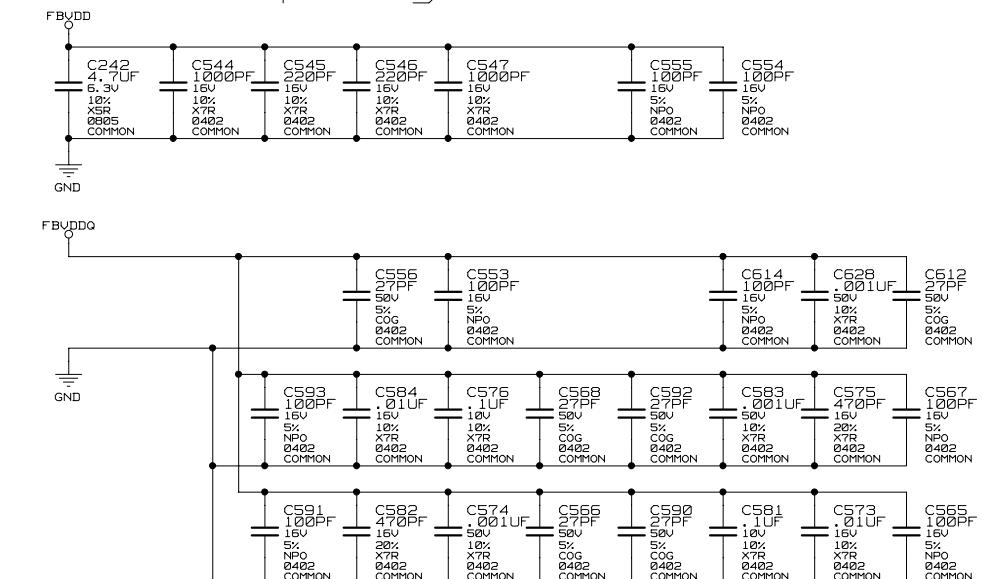
2. C. Memory: Bank 1: FBC & FBD



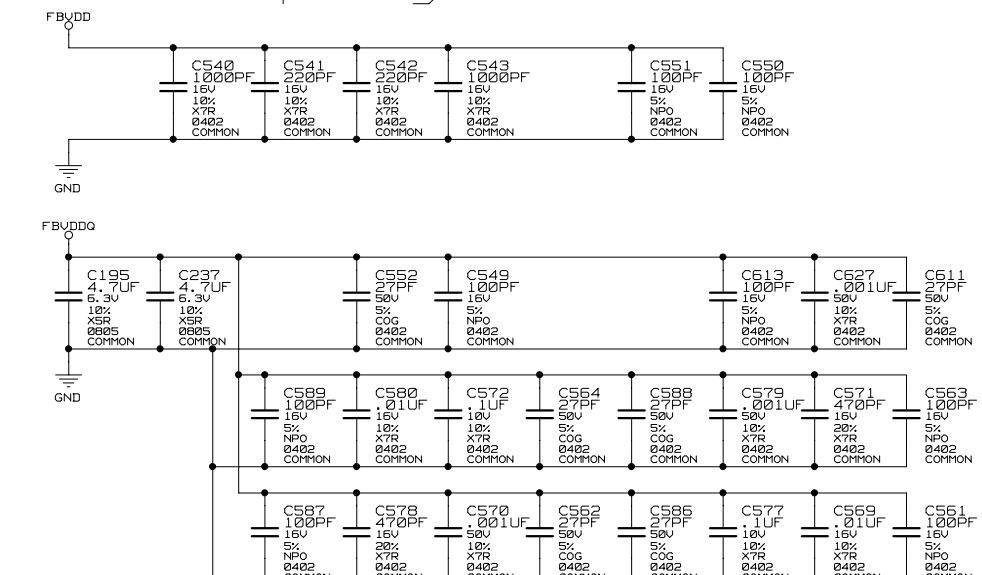
2. d. Memory: Bank2: FBA & FBB



Decoupling for FBA



Decoupling for FBB



NET RULES
NET PHYSICAL

[IN] FBAZQ1 12MIL-TRACE

[IN] FBBZQ1 12MIL-TRACE

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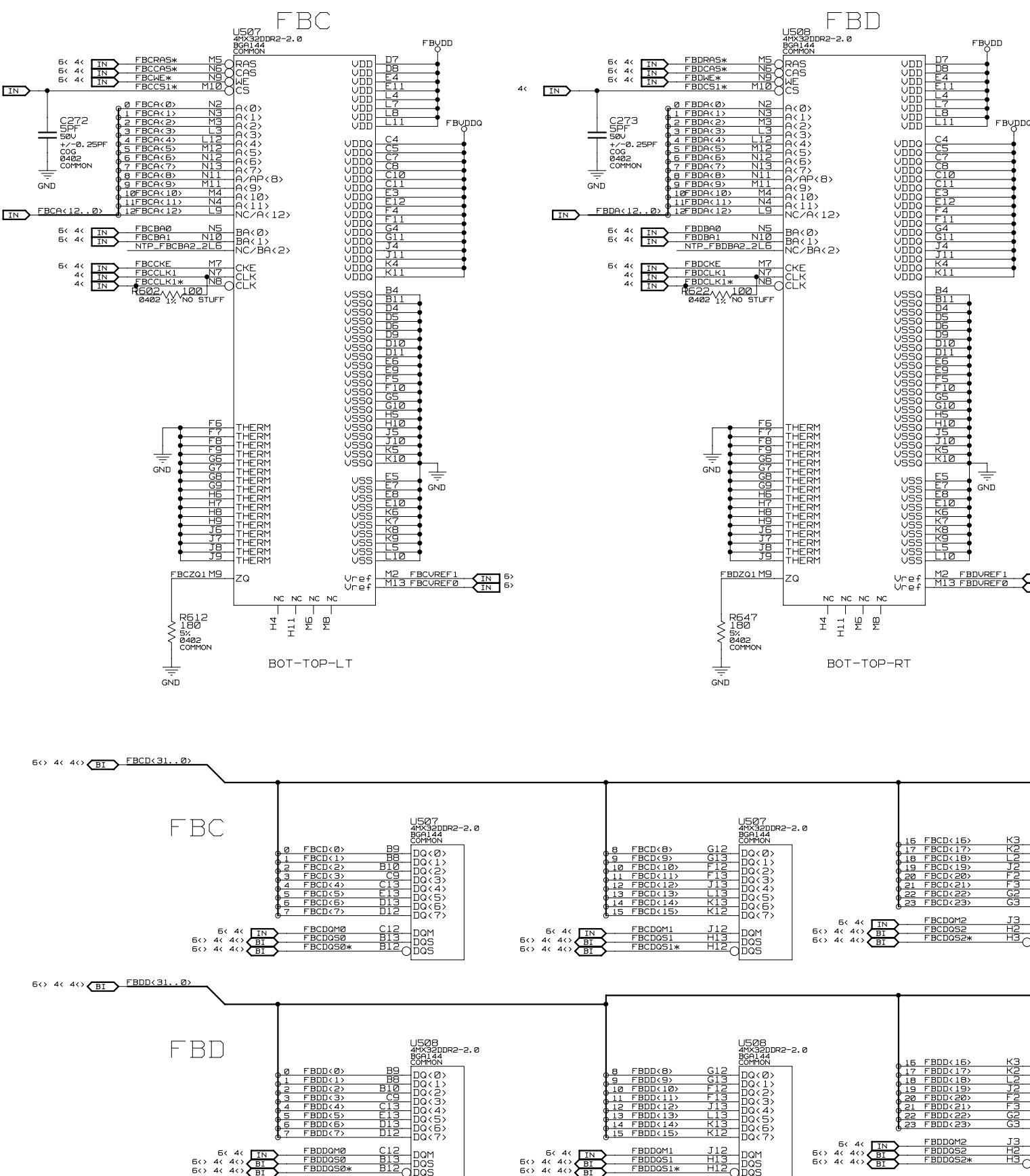
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DETAIL DRAWING DETAIL

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2. e. Memory: Bank2: FBC & FBD



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NET RULES
NET PHYSICAL

IN	FBCZQ1	12MIL-TRACE
IN	FBDZQ1	12MIL-TRACE

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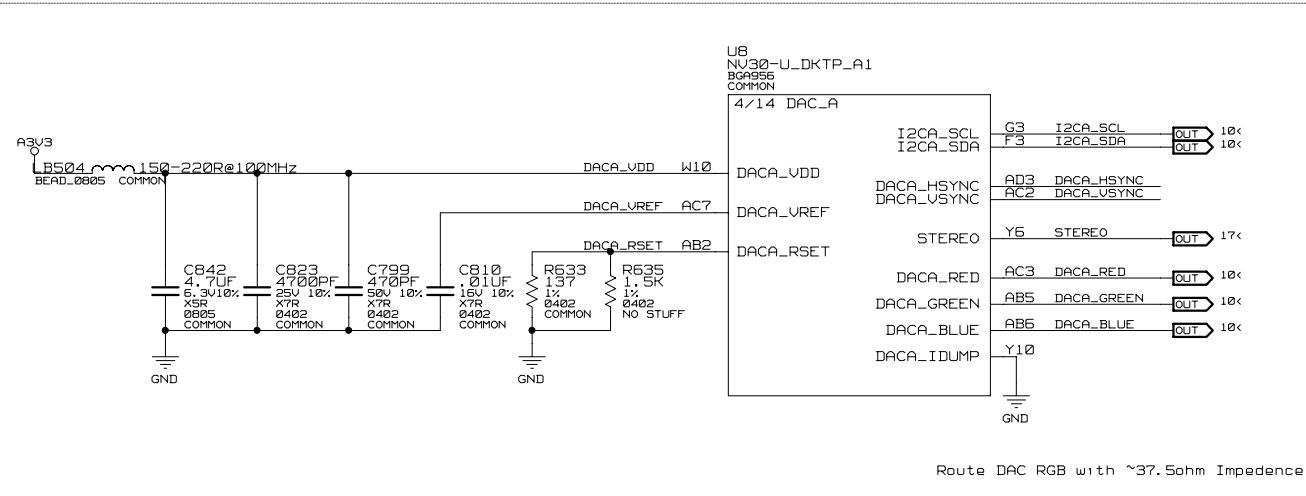
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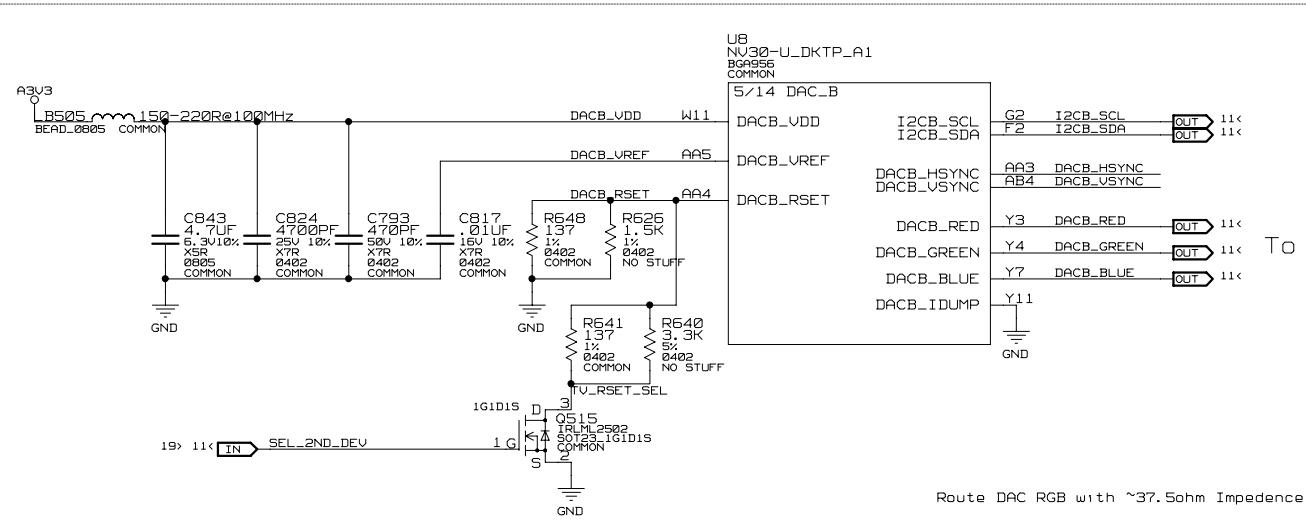


3.a. DAC and PLL

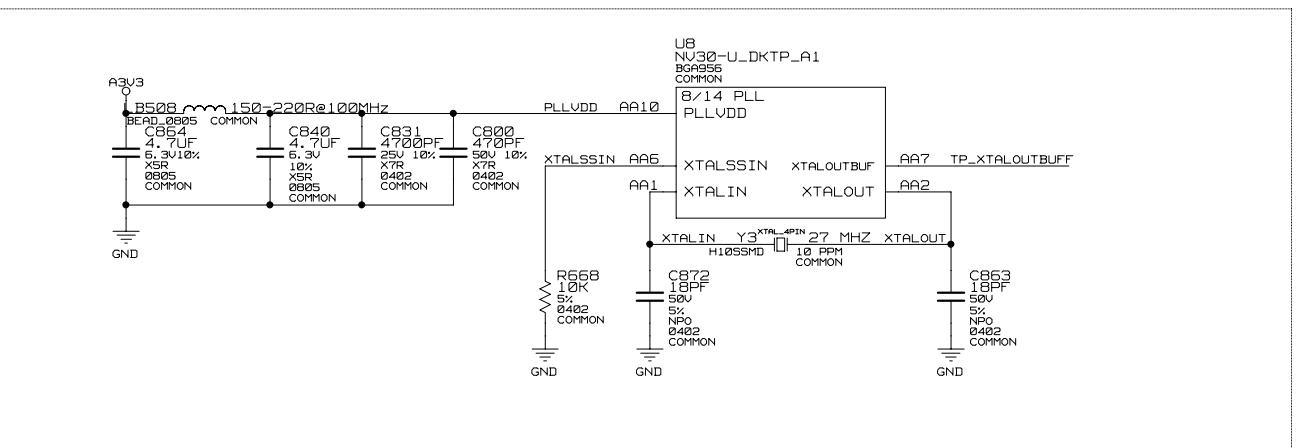
DACA



DACB

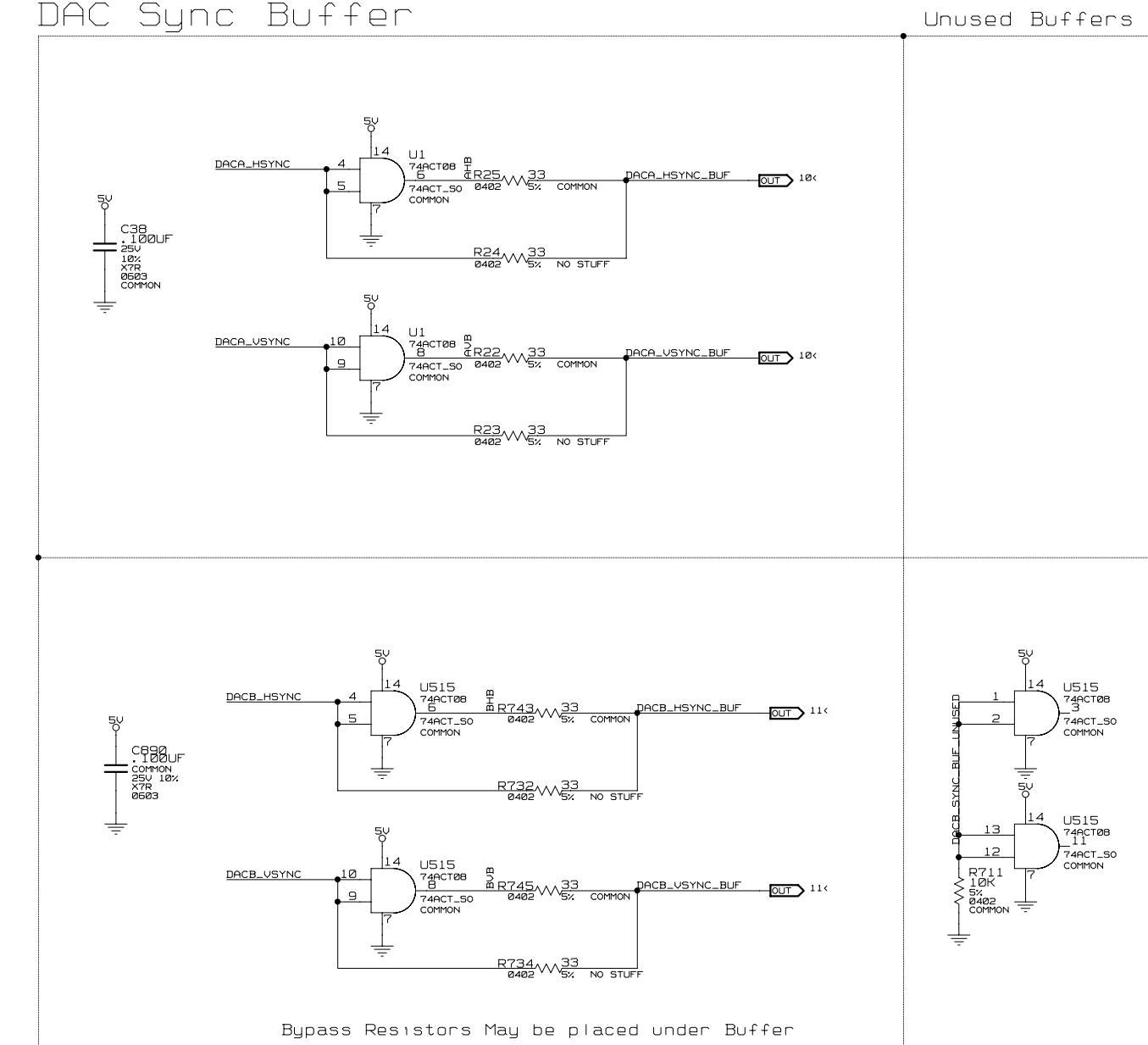


Xtal/PLLVDD



NET	PHYSICAL	VOLTAGE
XTALIN	18MIL_TRACE	
XTALOUT	18MIL_TRACE	
DACA_VDD	12MIL_TRACE	3.3V
DACA_VREF	5MIL_TRACE	
DACA_RSET	5MIL_TRACE	
DACB_VDD	12MIL_TRACE	3.3V
DACB_VREF	5MIL_TRACE	
DACB_RSET	5MIL_TRACE	
PLLVDD	12MIL_TRACE	3.3V

DAC Sync Buffer

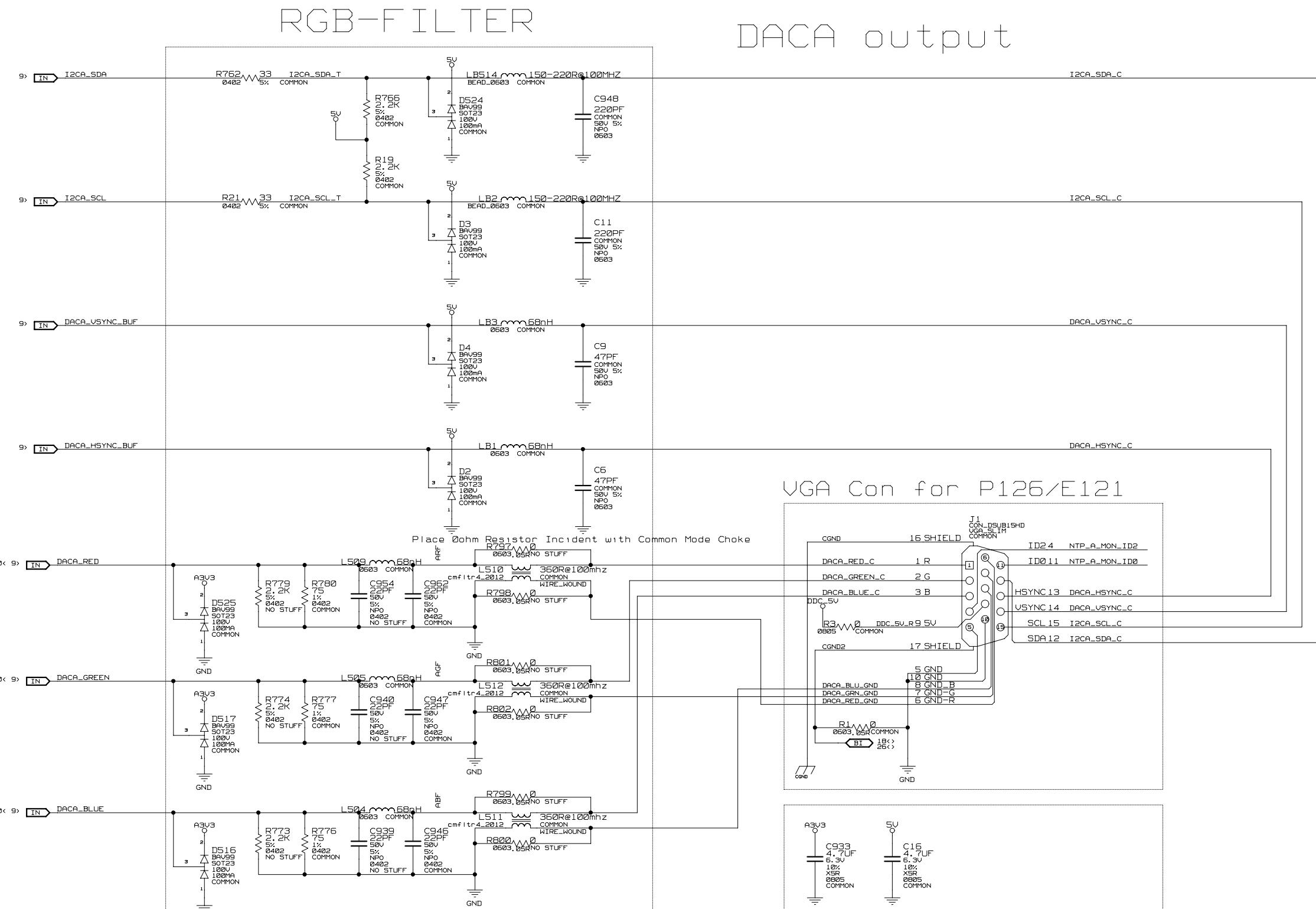


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3. b. DACA Output



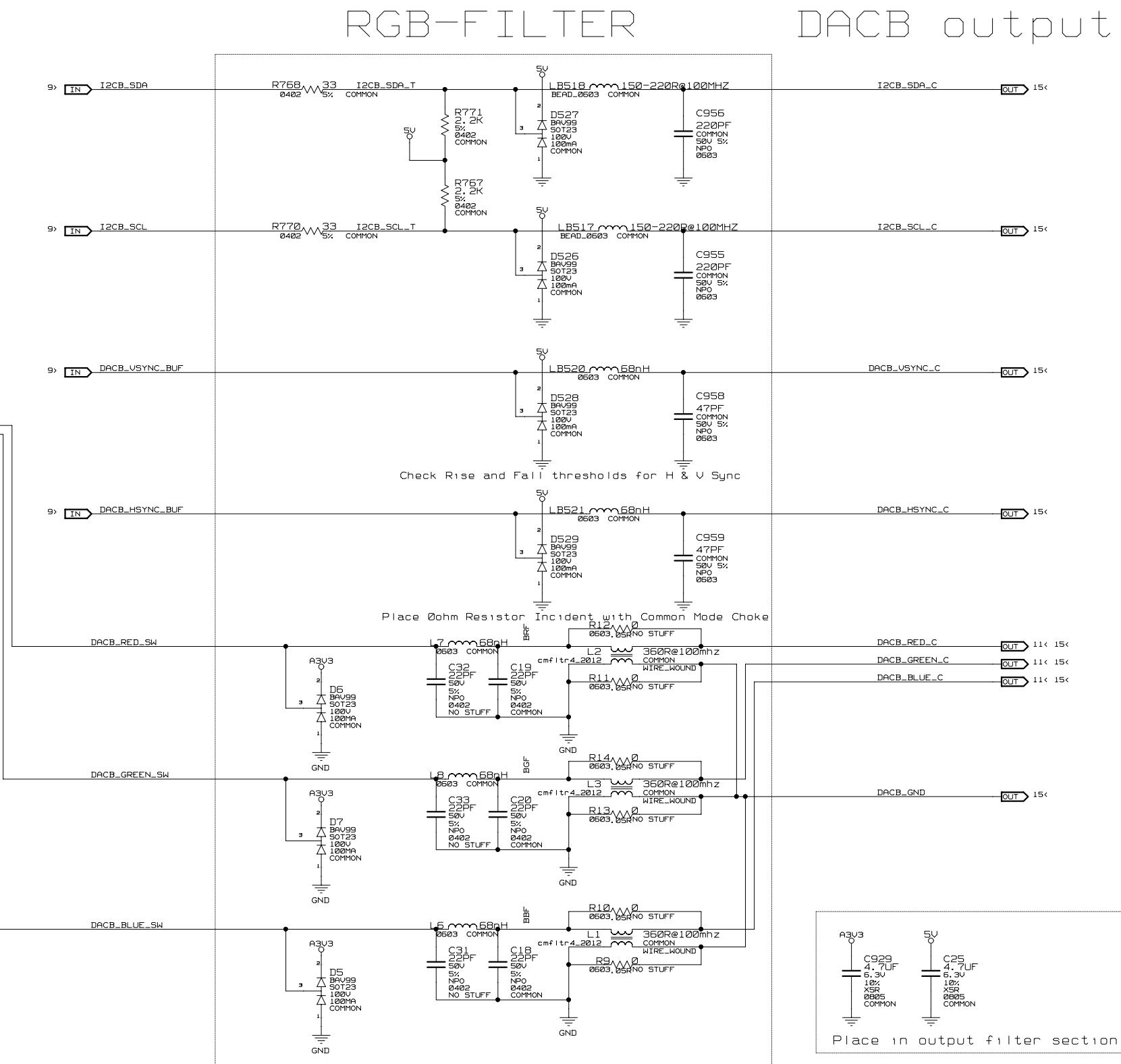
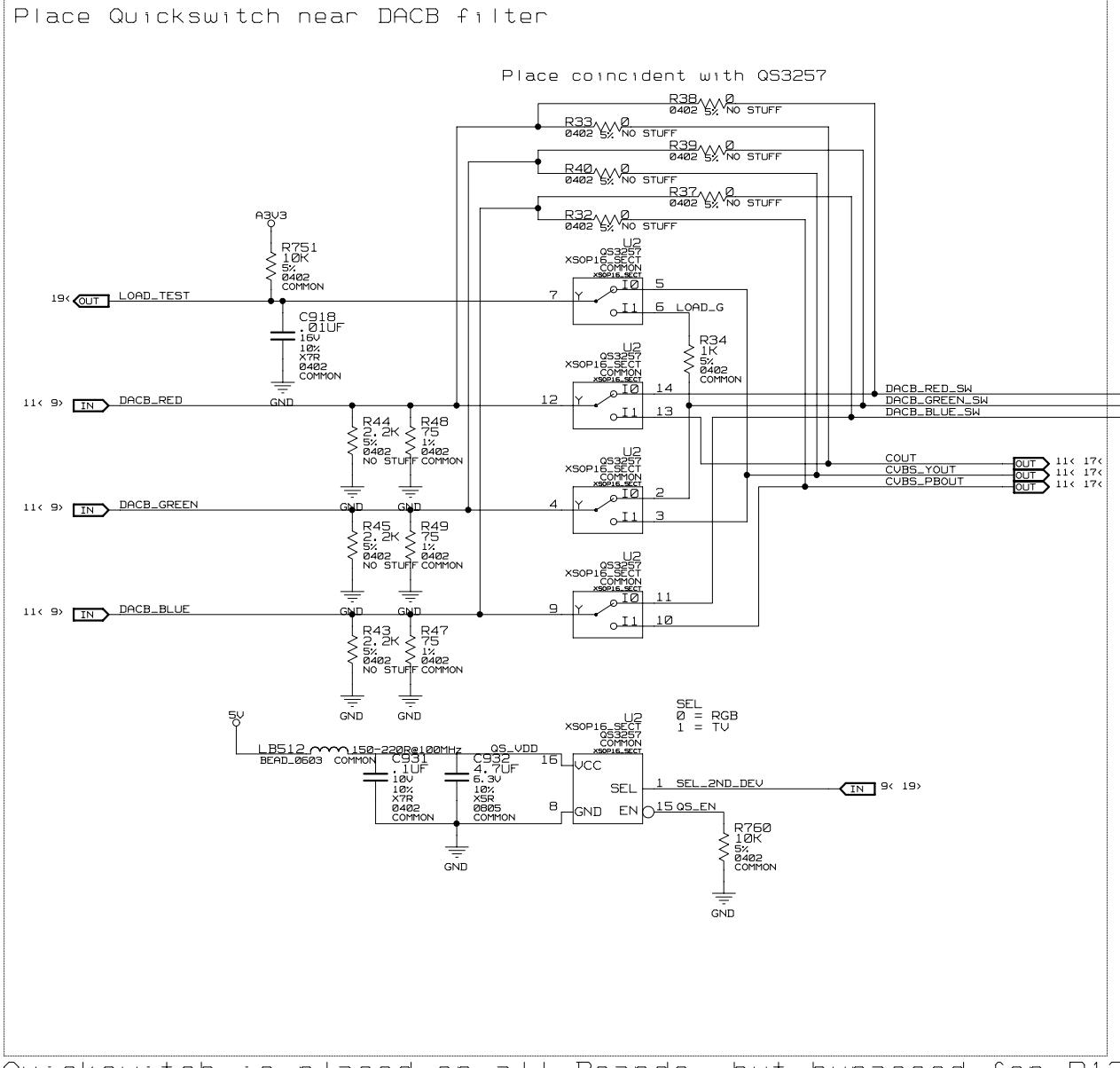
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NET SPACING	
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10< 9>	IN DACA_BLUE 20MIL
10< 9>	IN DACA_RED_C 20MIL
10< 9>	IN DACA_GREEN_C 20MIL
10< 9>	IN DACA_BLUE_C 20MIL

NET PHYSICAL	
IN	DACA_RED_GND 12MIL_TRACE
IN	DACA_GRN_GND 12MIL_TRACE
IN	DACA_BLU_GND 12MIL_TRACE

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3. c. DACB Output

Quickswitch for DACB



NET RULES

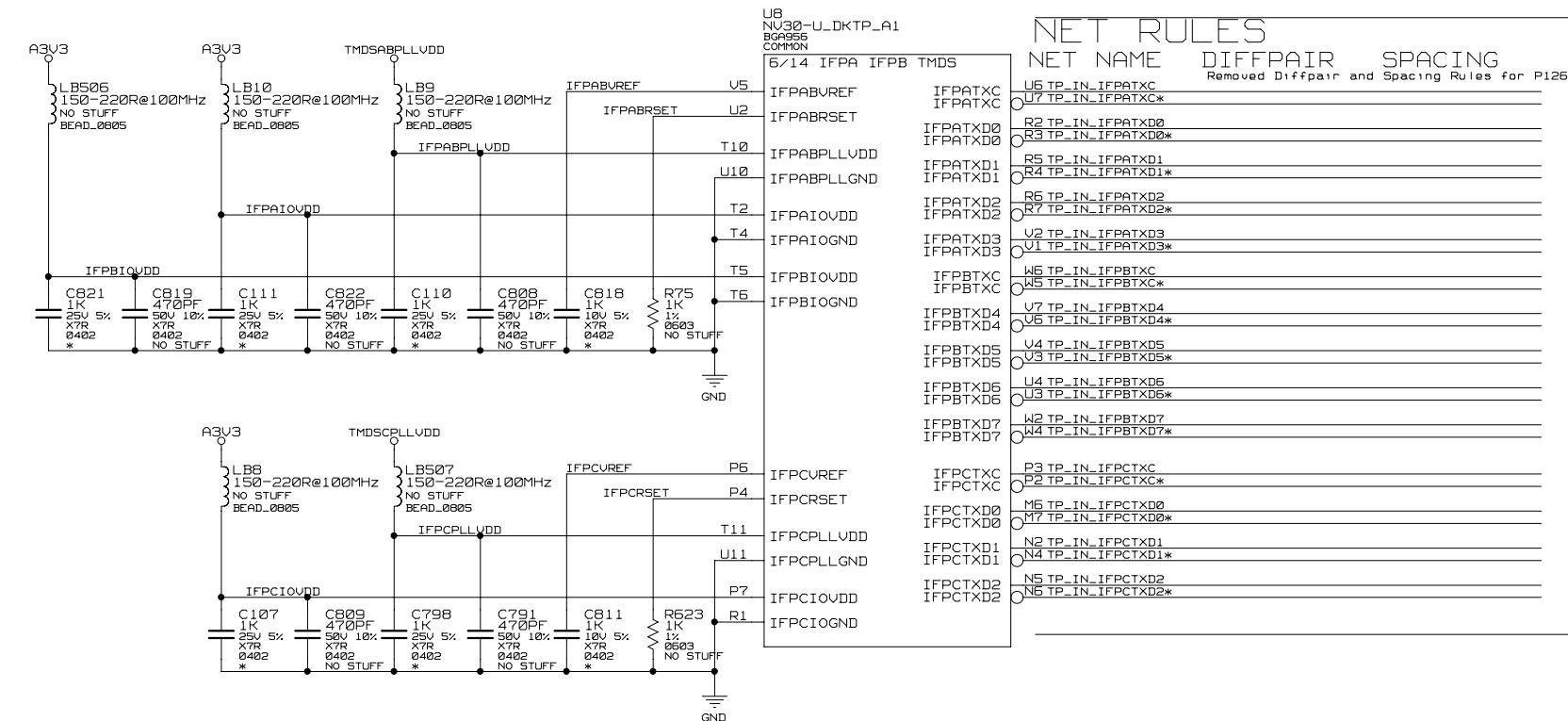
NET	SPACING
DACB_RED	20MIL
DACB_GREEN	20MIL
DACB_BLUE	20MIL
DACB_RED_SW	20MIL
DACB_GREEN_SW	20MIL
DACB_BLUE_SW	20MIL
DACB_RED_C	20MIL
DACB_GREEN_C	20MIL
DACB_BLUE_C	20MIL
COUT	20MIL
CVBS_YOUT	20MIL
CVBS_POUT	20MIL

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4. a. Internal TMDS



IFP Power should have alternate pull-down to GND when not used

NET RULES

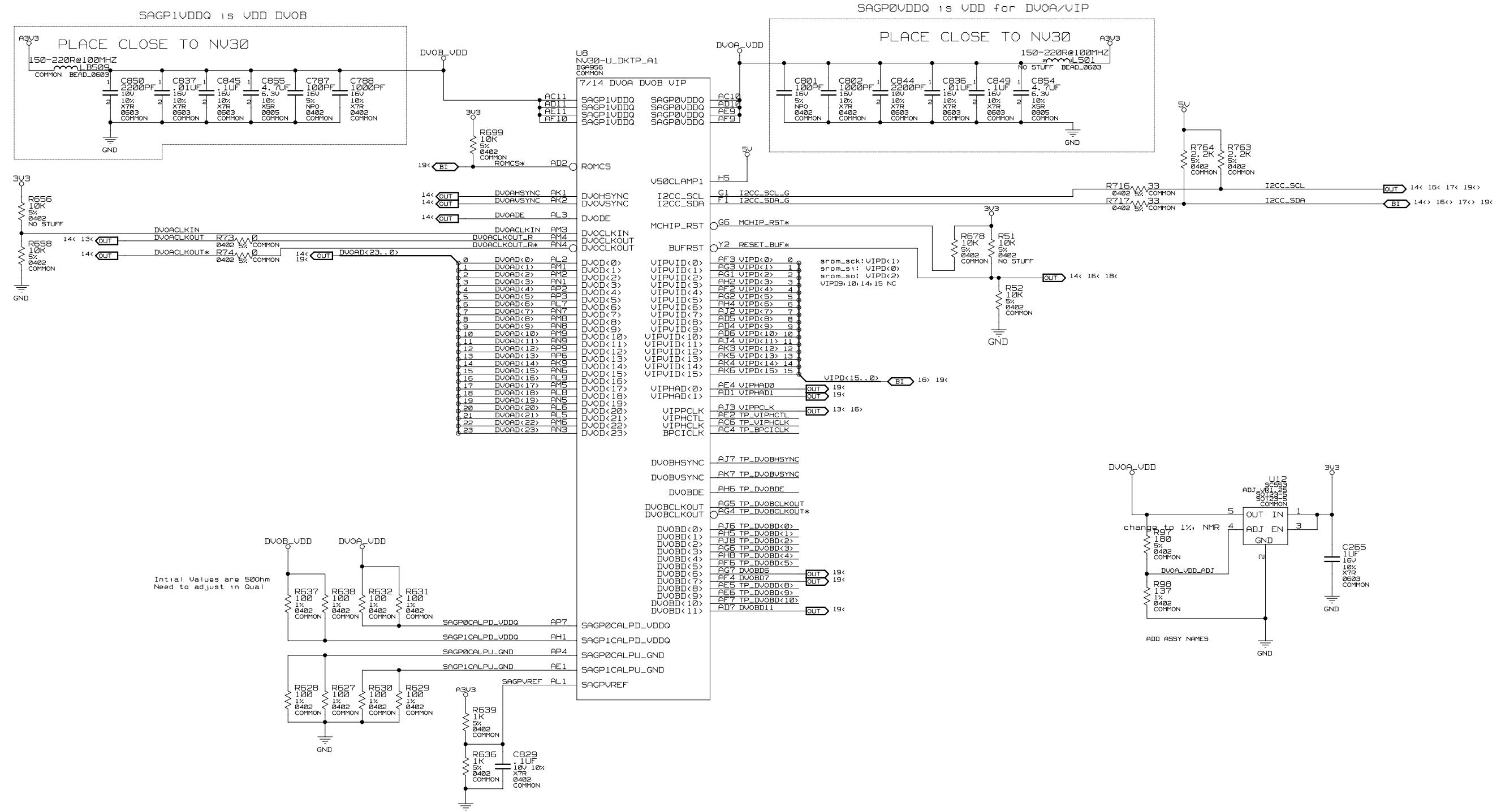
NET	PHYSICAL	VOLTAGE
IFPBPLLVDD	12MIL_TRACE	3.3V
IFPAIOVDD	12MIL_TRACE	3.3V
IFPABUREF	10MIL_TRACE	3.3V
IFPABRSET	10MIL_TRACE	3.3V
IFPBPLLVDD	12MIL_TRACE	3.3V
IFPCIOVDD	12MIL_TRACE	3.3V
IFPCUREF	10MIL_TRACE	3.3V
IFPCRSET	10MIL_TRACE	3.3V

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DETAIL	DRAWING DETAIL
CONTINUED...	

4. b. DVO/VIP Interface

NET RULES		PHYSICAL	SPACING
IN	SAGP1CALPD_VDDQ	12MIL_TRACE	20MIL
IN	SAGP1CALPD_VDDQ	12MIL_TRACE	20MIL
IN	SAGP1CALPU_GND	12MIL_TRACE	20MIL
IN	SAGP1CALPU_GND	12MIL_TRACE	20MIL
3	DVOACLKOUT		20MIL
4	DVOACLKOUT_R		20MIL
3	VIPCLK		20MIL
6			

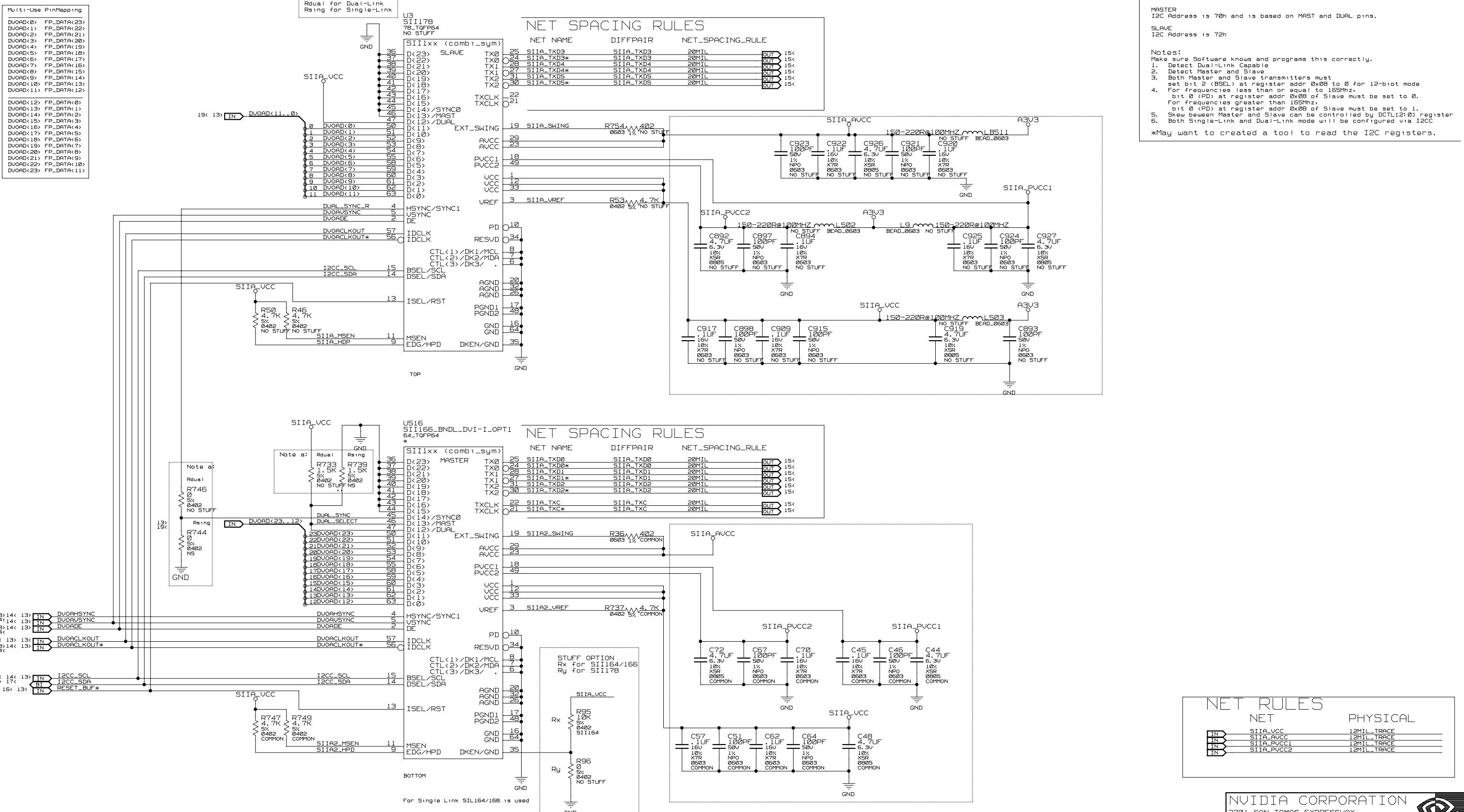


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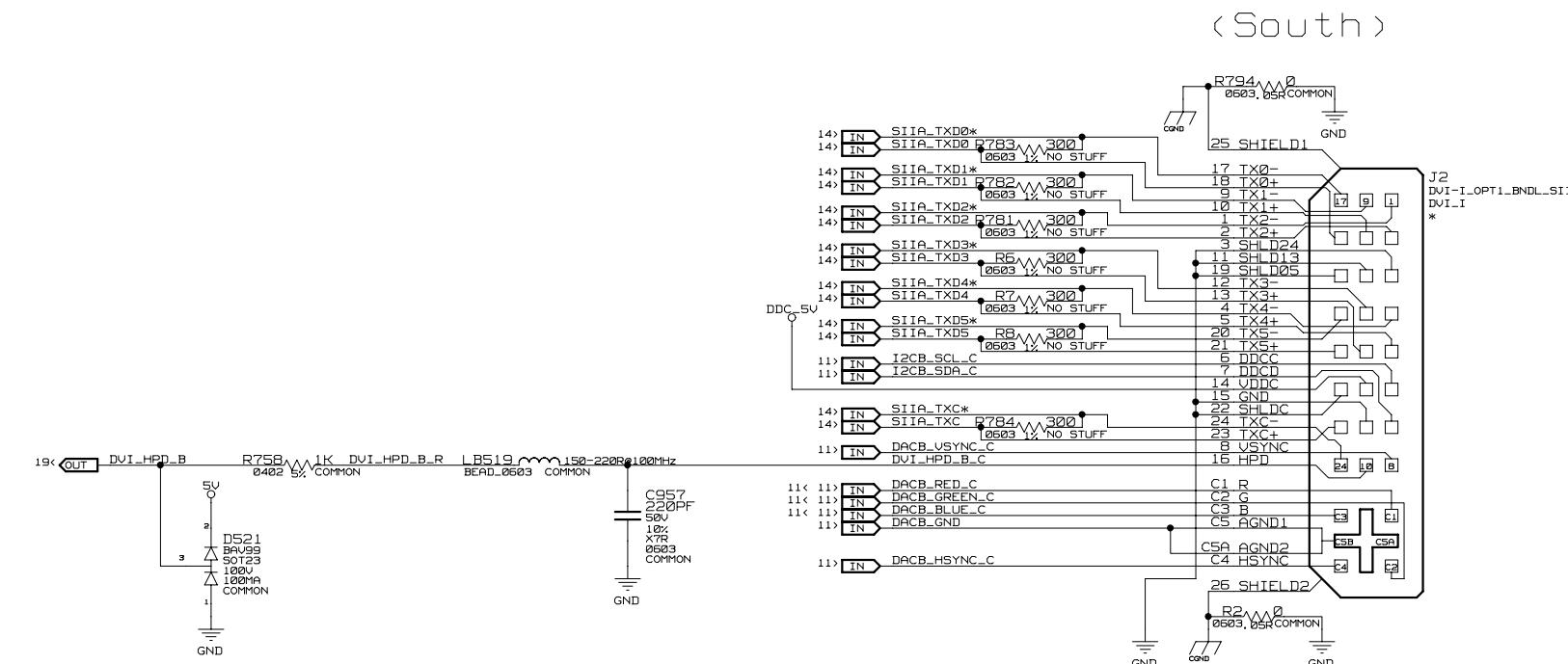
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DETAIL DRAWING DETAIL
CONTINUED...

4. C. DVOA: External Dual-Link Transmitter



4. e. DVI-I (TMDS) Connector



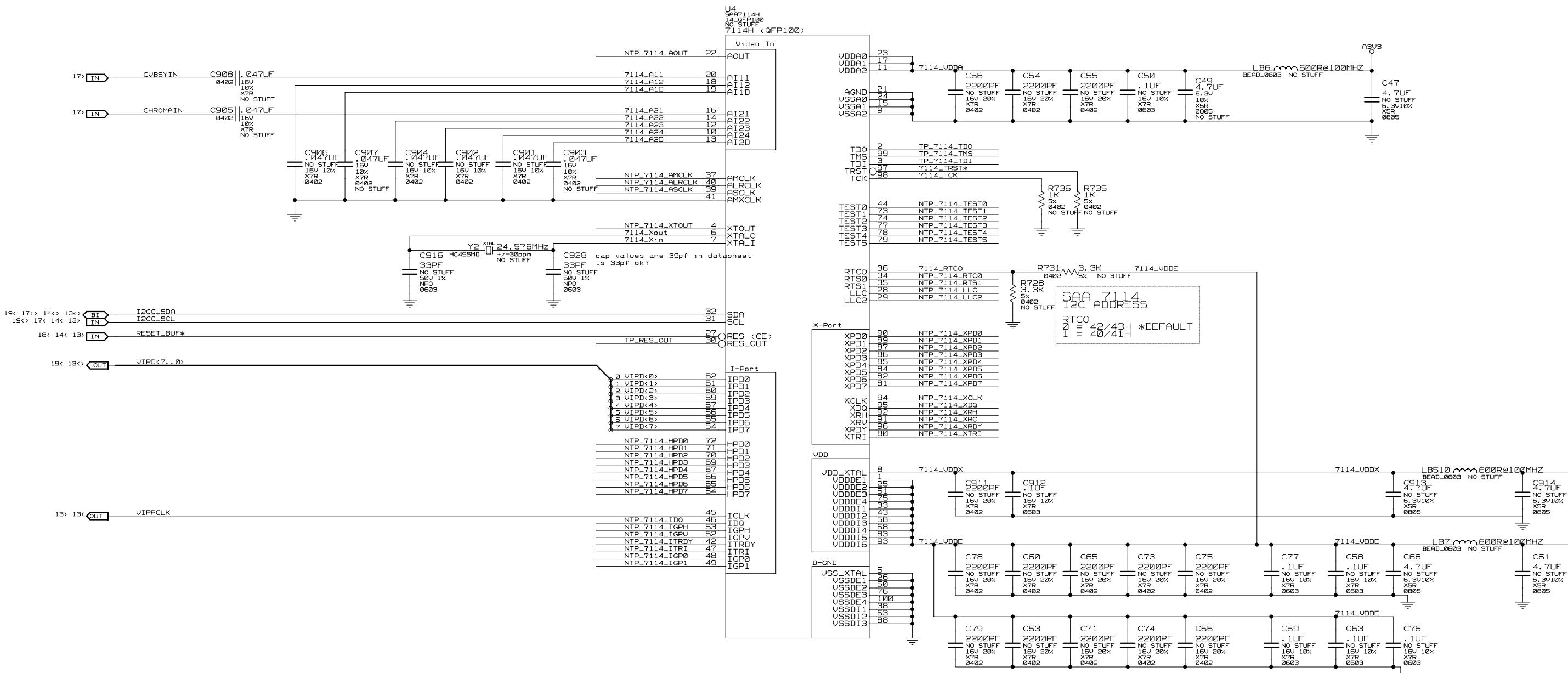
NV30 GPIO's are 5V Tolerant
So 10K/15K voltage divider is no required on HPD

5.a. Video Capture

NET RULES

NET	PHYSICAL	VOLTAGE
IN	12MIL_TRACE	3.3V
IN	12MIL_TRACE	2.8V
IN	12MIL_TRACE	3.3V

VIDEO CAPTURE



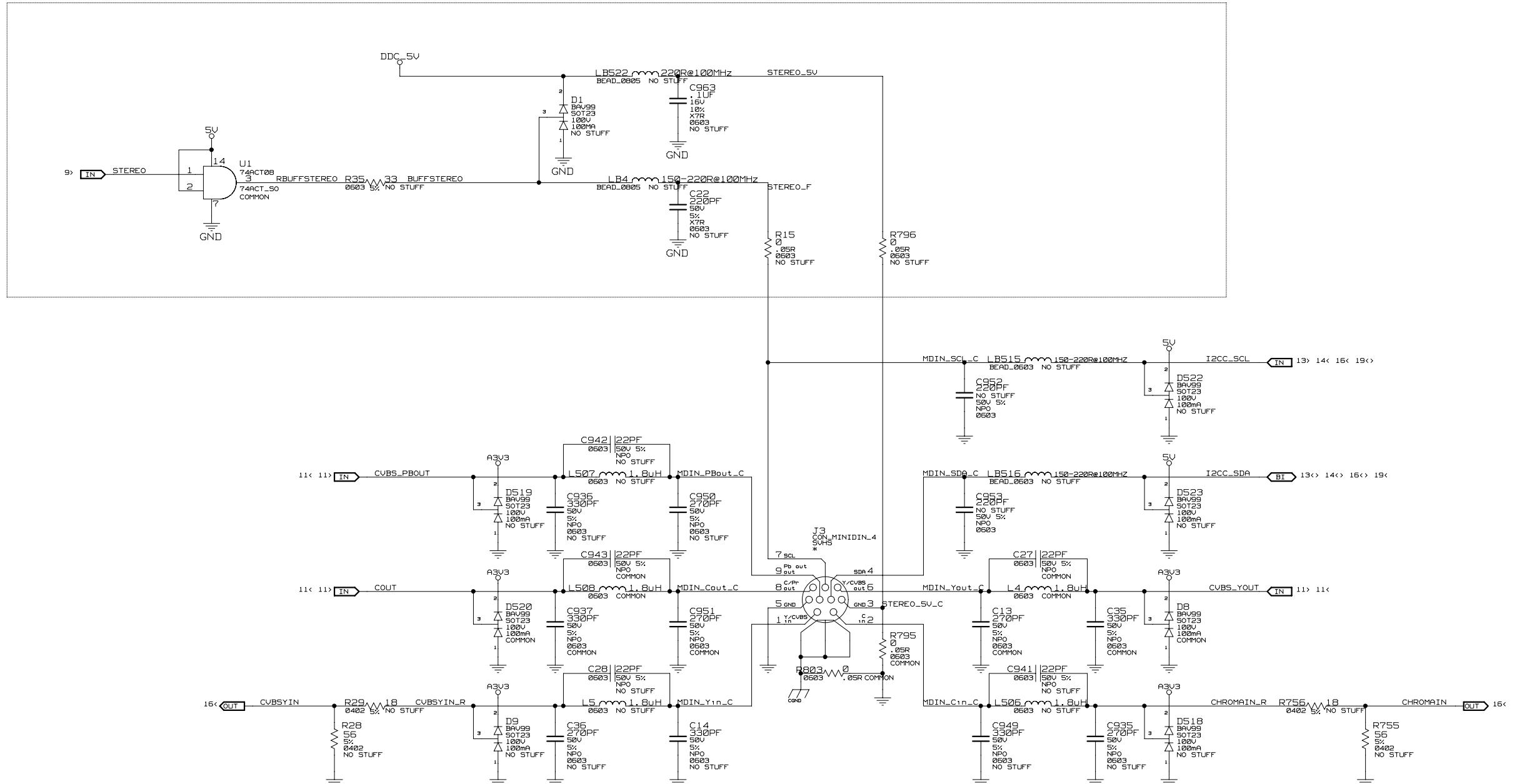
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DETAIL DRAWING DETAIL
CONTINUED...

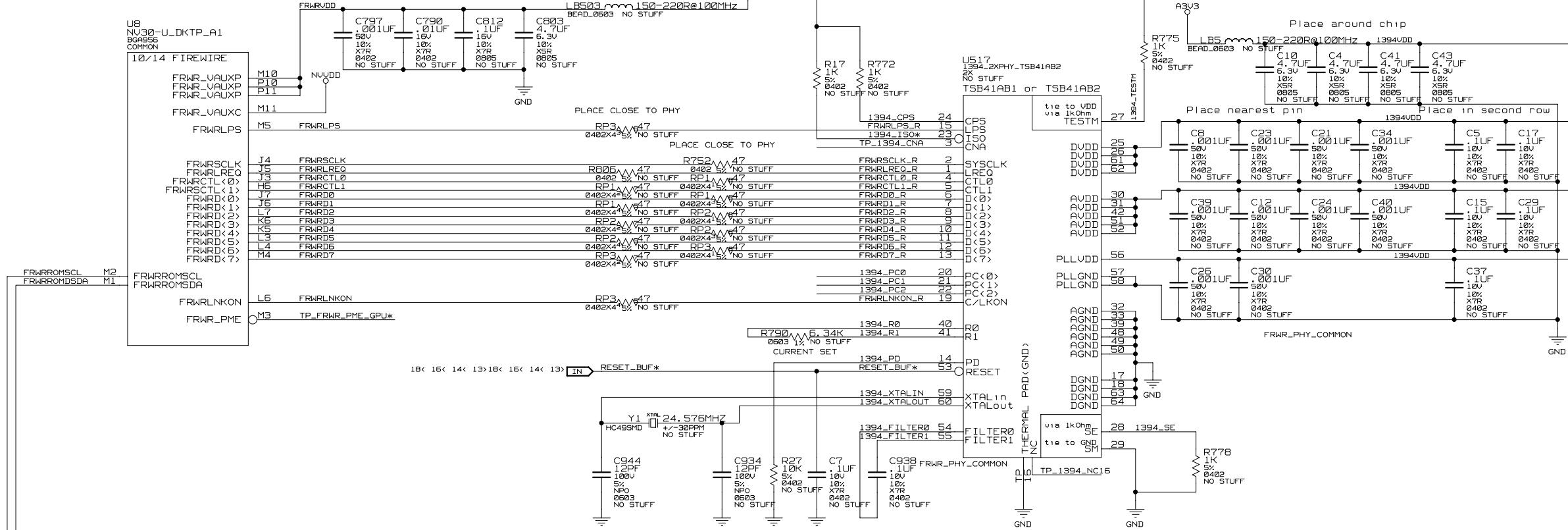
5. b. DIN Connector (TV, VIVO, STEREO)

STEREO 3D

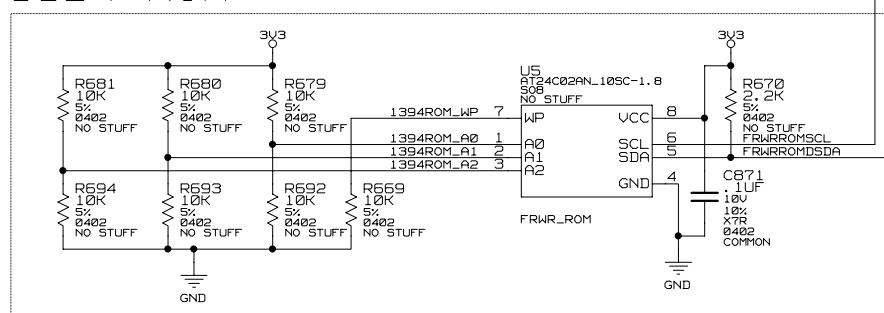


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DETAIL DRAWING DETAIL
CONTINUED..

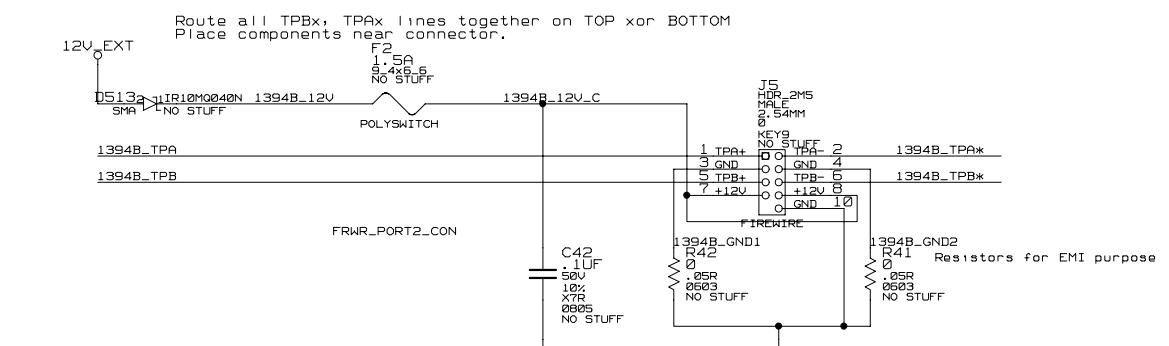
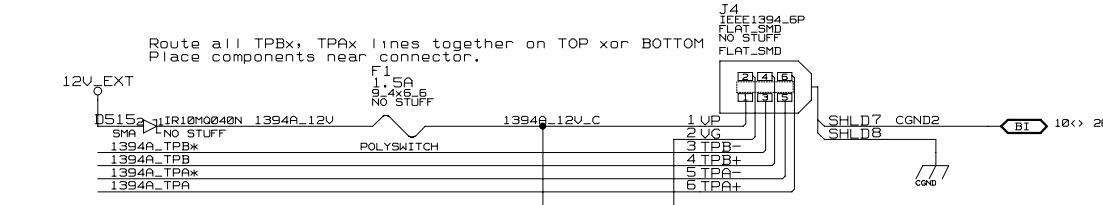
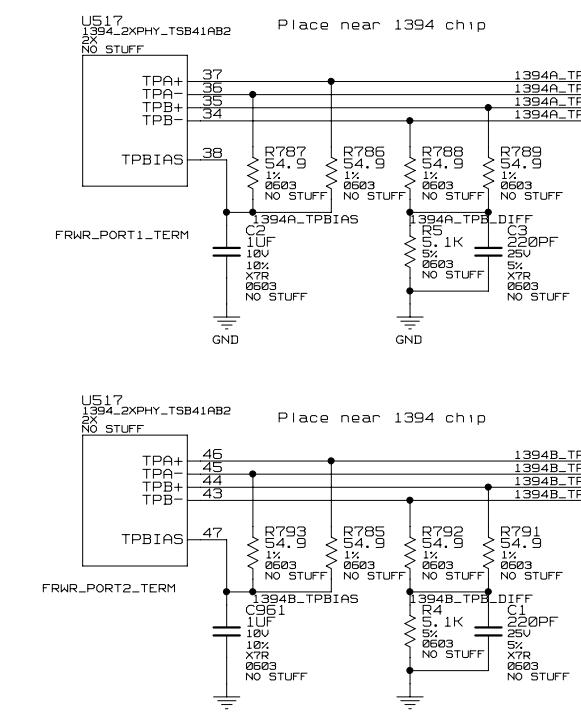
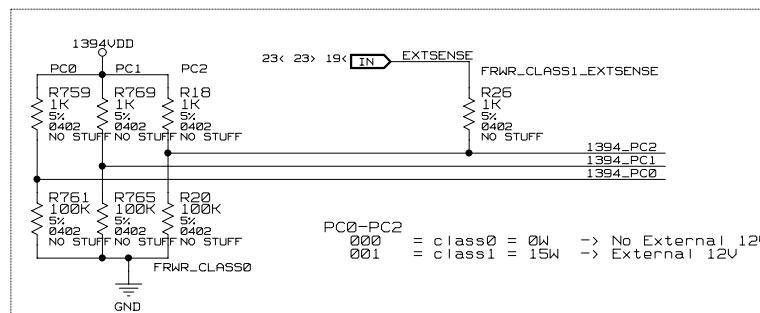
6.a. Firewire



1394 ROM



1394 Class Detect



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DETAIL DRAWING DETAIL
CONTINUED

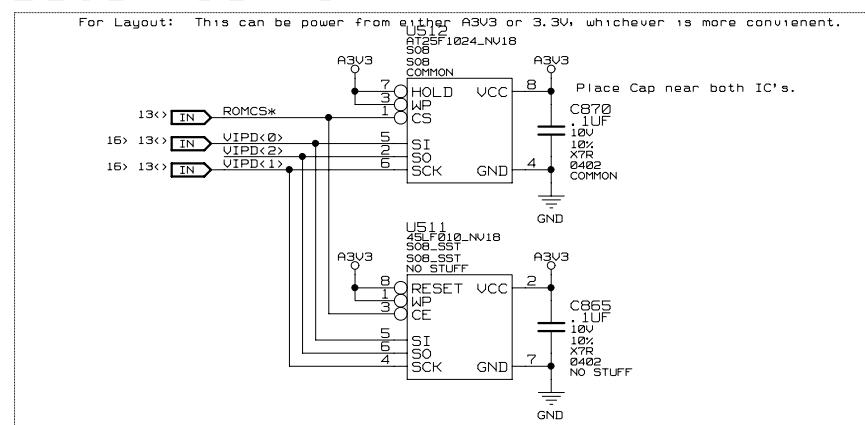
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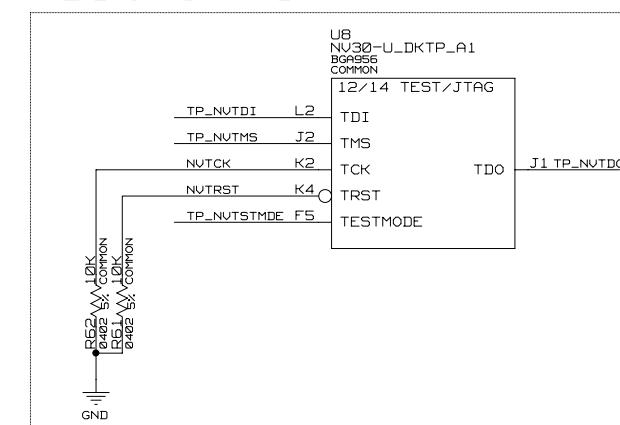
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7. a. BIOS, Straps, Misc

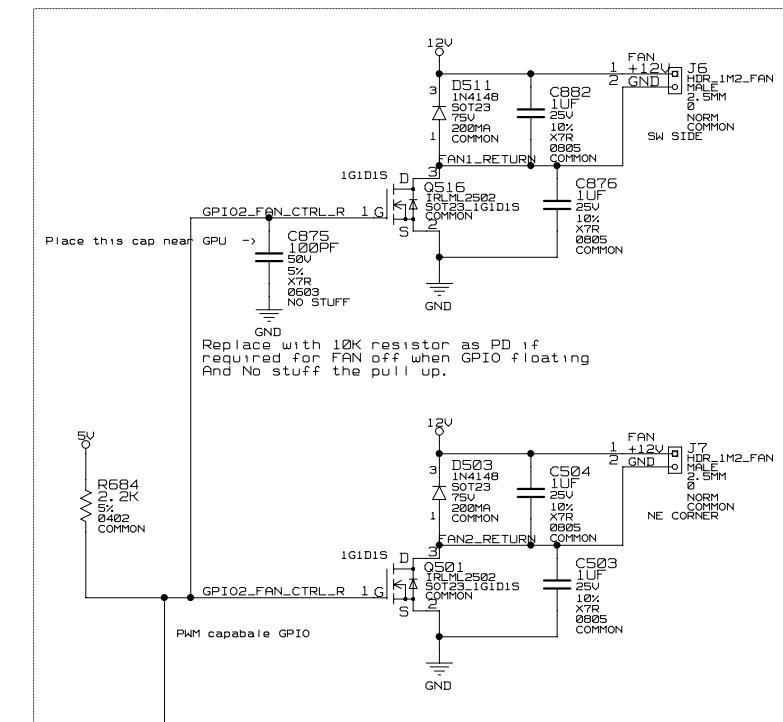
BIOS <serial>



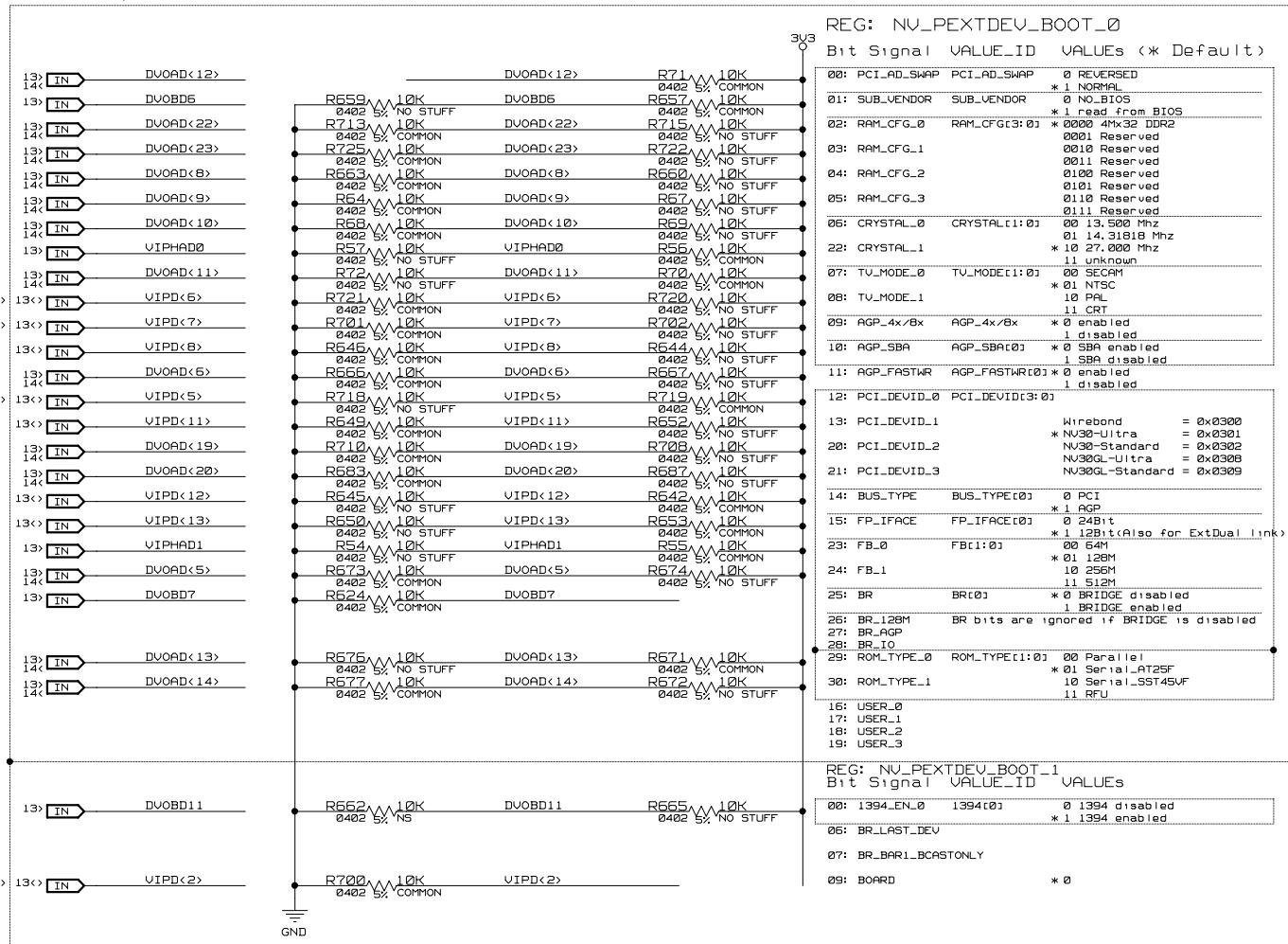
Test/JTAG



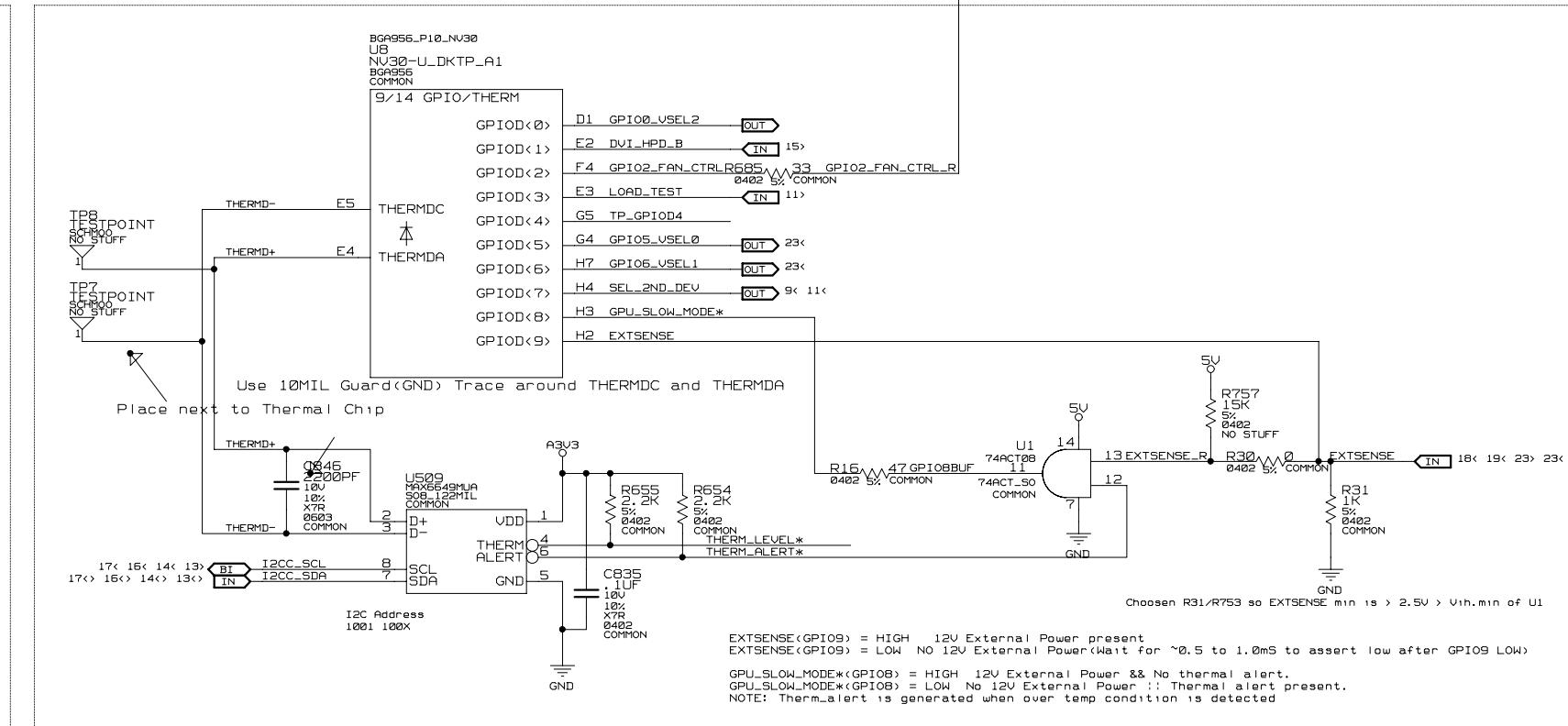
Fan1/Fan2



Straps



GPIO's, Fan Control, Thermal Sense & EXT Power Sense



NET RULES

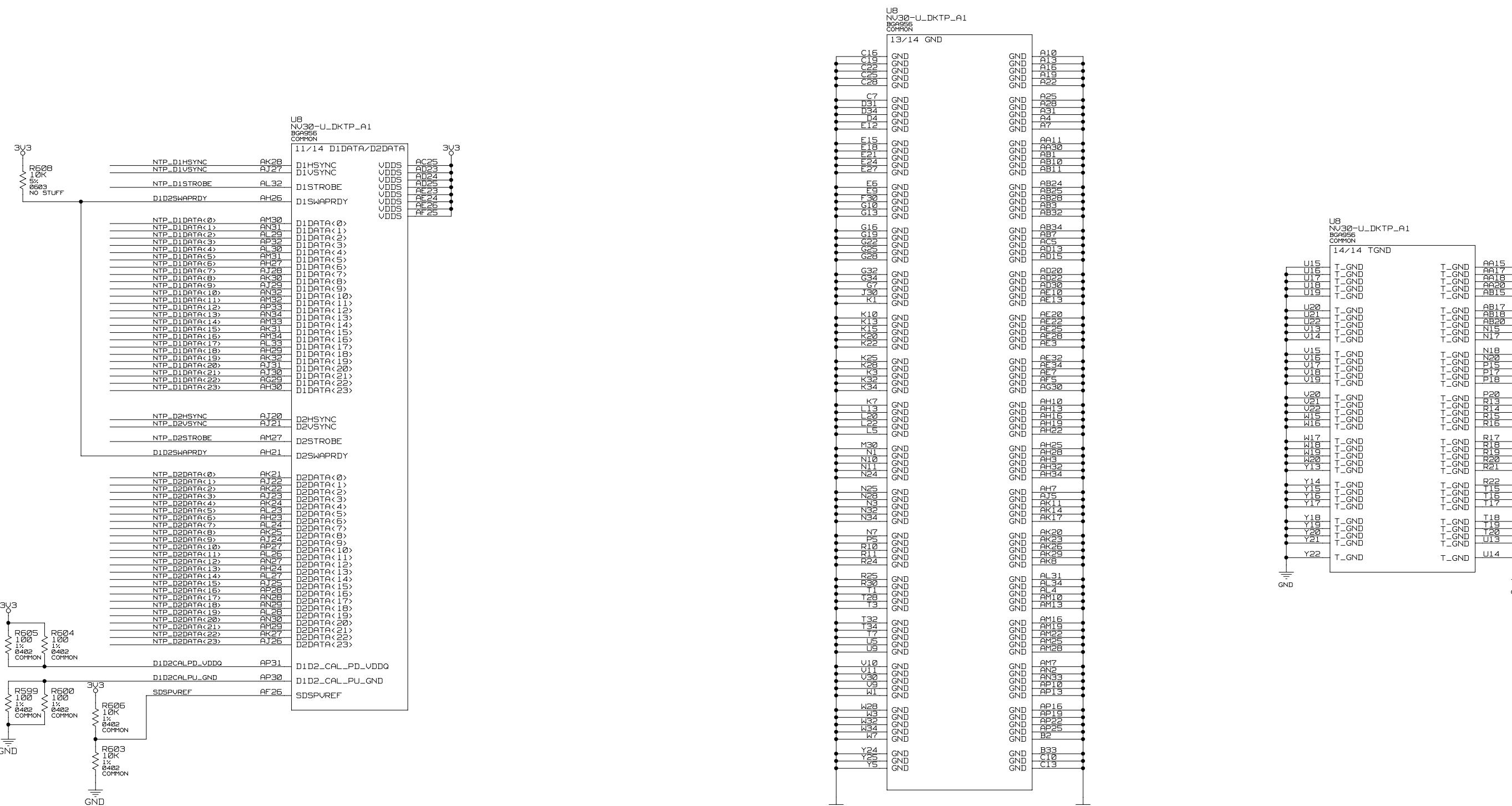
NET		PHYSICAL	
 IN	THERMDC	10MIL_TRACE	
 IN	THERMDA	10MIL_TRACE	
 IN	FAN1_RETURN	16MIL_TRACE	
 IN	FAN2_RETURN	16MIL_TRACE	
NET		SPACING	
 IN	GPIO2_FAN_CTRL	20MIL	
 IN	GPIO2_FAN_CTRL_R	20MIL	

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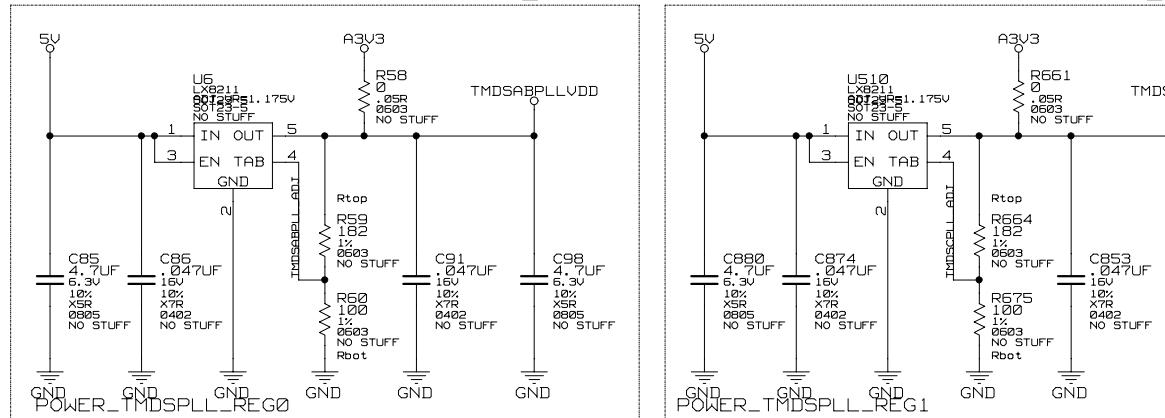
DETAIL DRAWING DETAIL
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8.a. GND, Thermal GND and Misc...



9.a. Power Supply I: TMDS/A3V3/FBVDD

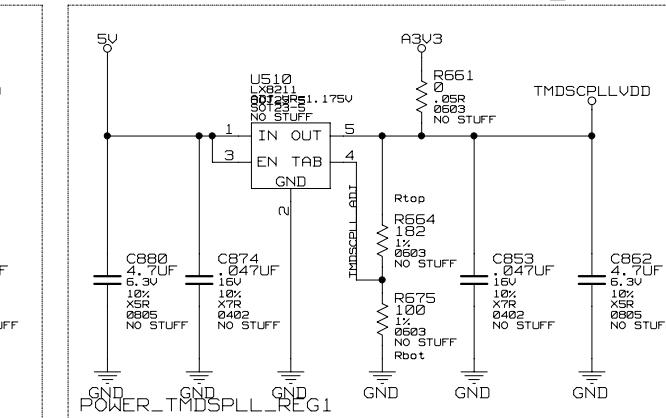
TMDS AB PLL Supply



$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

$$3.31V = 1.175V * (1 + (100/182))$$

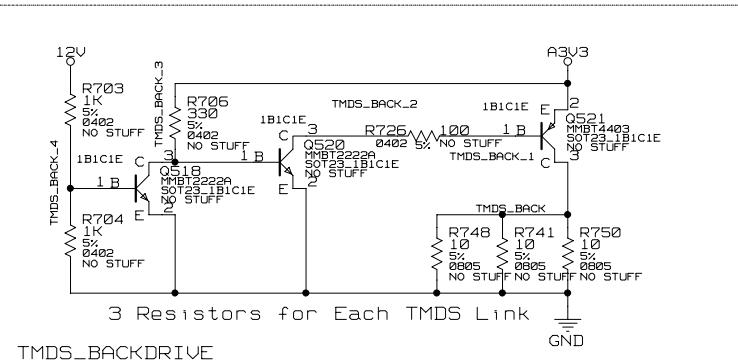
TMDS C PLL Supply



$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

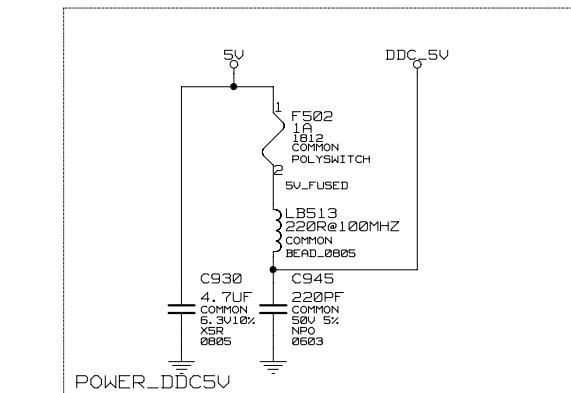
$$3.31V = 1.175V * (1 + (100/182))$$

TMDS backdrive prevention



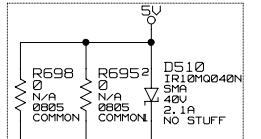
TMDS_BACK

DDC 5V

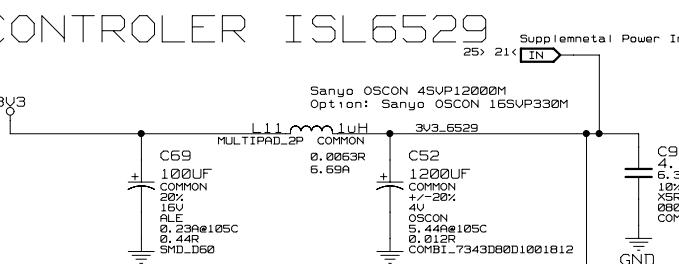


FBVDD-SWITCHER / A3V3-LDO CONTROLLER ISL6529

Diode Bypass when TMDS Backdrive is not stuffed

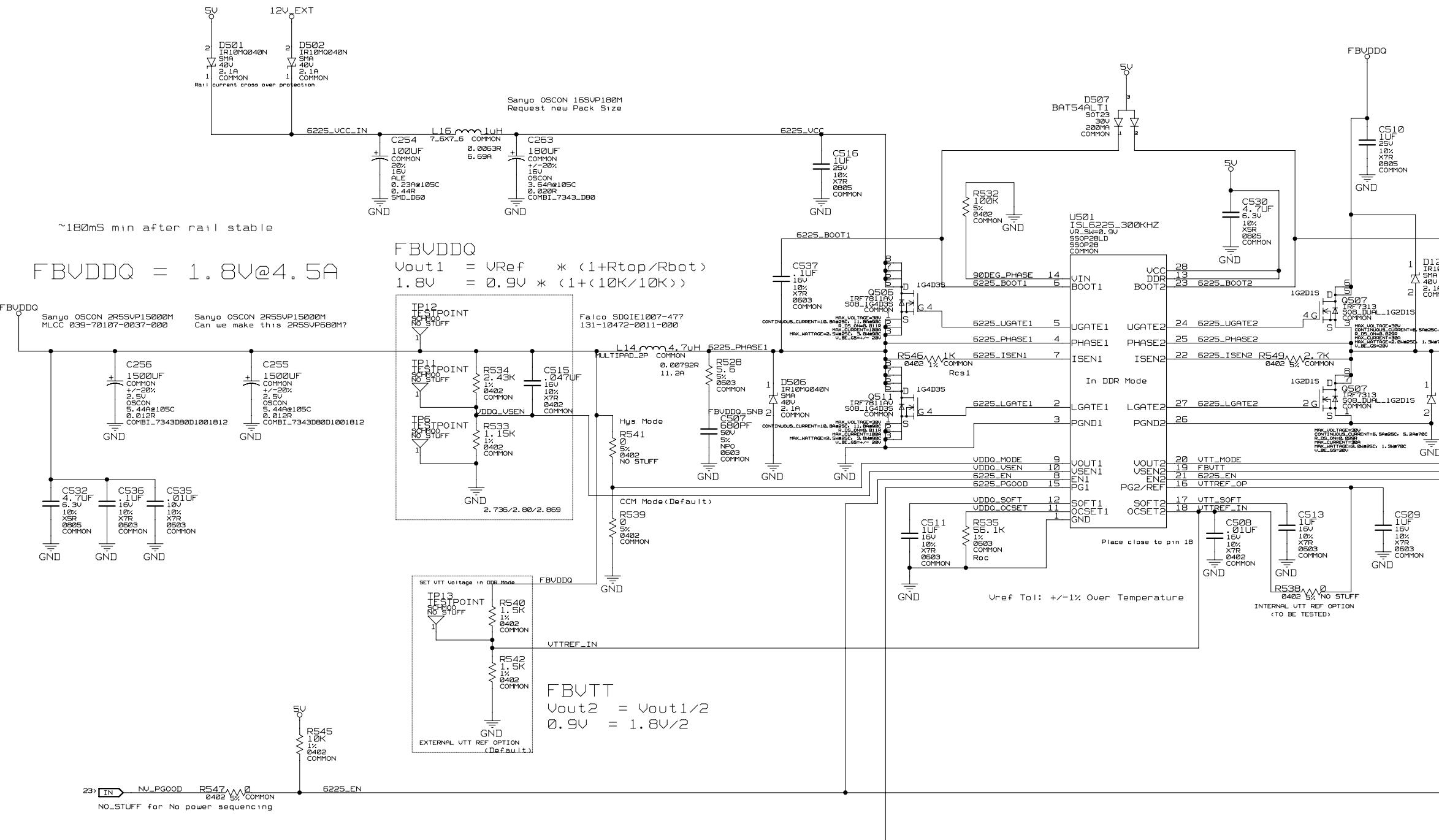


$$A3V3 = 3.3V @ 1.5A$$



9.b. Power Supply II: FBVDDQ/FBUTT

NOTE:
For 5V(AGP) operation the MCLK is limited and to be decided during qual.
With 12V_Ext<HDD Con>: There is no limit on max mclk freq.



NOTE

For Shmoo to change the o/p voltage adjust the FBVDDQ and VTT levels independently

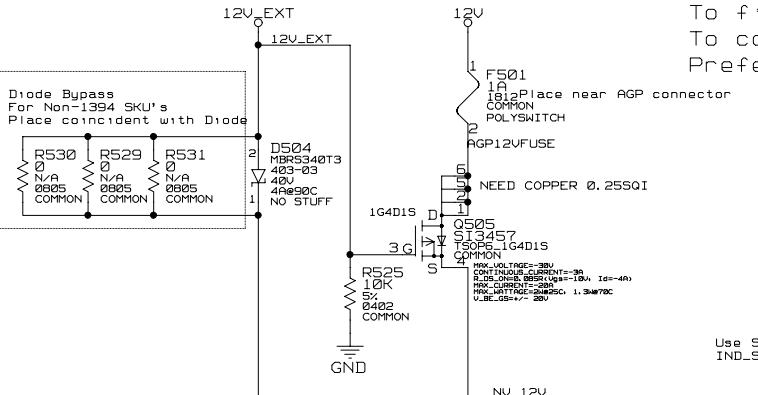
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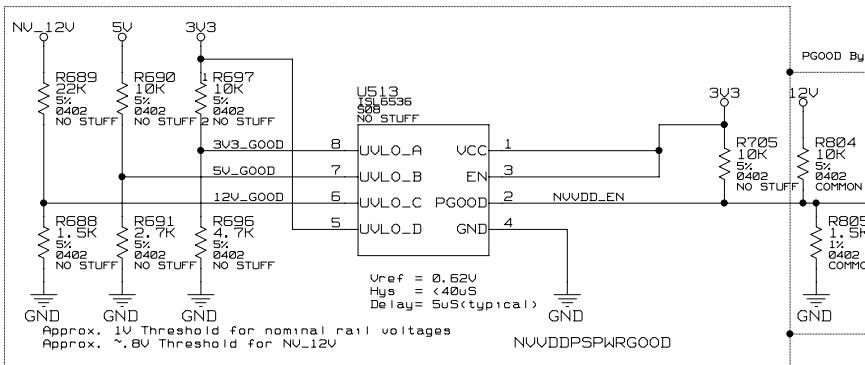
9. C. Power Supply III: NUVDD

$U_{ref,Tol} = \pm 1\%$ over Temperature
Dynamic VID o/p rate = $25mV/(2 * 1/freq)$
SoftStart-stable o/p Delay = $2048/freq$

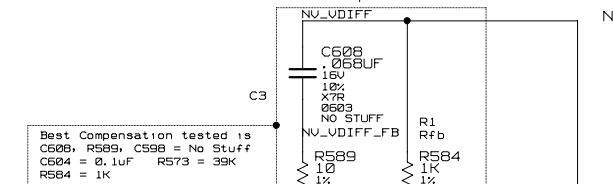


NOTE For shmoos NUVDD
To fine adjust within 25mV, Replace $R_{off} < 5K$
To coarse adjust, Change VIDx Pull Down resistors as per table
Prefer removing ALL VSEL0 and VSEL1 control resistors

Power Good



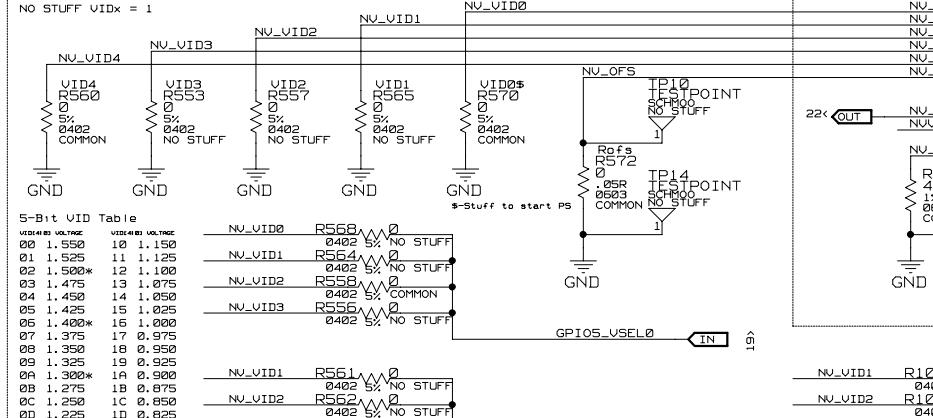
Comp Network



NUVDD Voltage Select

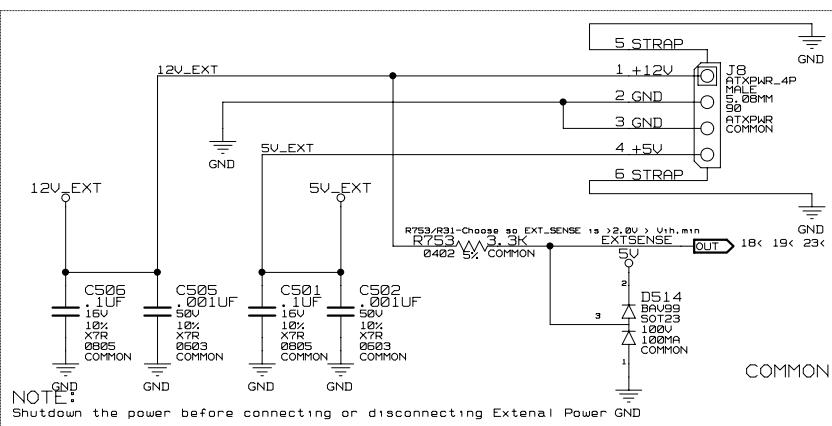
Regulator: ISL6569
GPIO5_VSEL0 and GPIO6_VSEL1 is mapped to VID[4:1] and is used to Control NUVDD
 $*VSEL_VID = V_{out} + (V_{offs} * 10)$
 $V_{out} = 1.5V + (V_{offs} * 10)$
 $V_{offs} = V_{offs} * 10$
 $20K = 0.20V * 10$

* GPIO's should tristate for logic 1
#Default on start up will be 1.2V
STUF OR VIDx = 0
NO STUFF VIDx = 1



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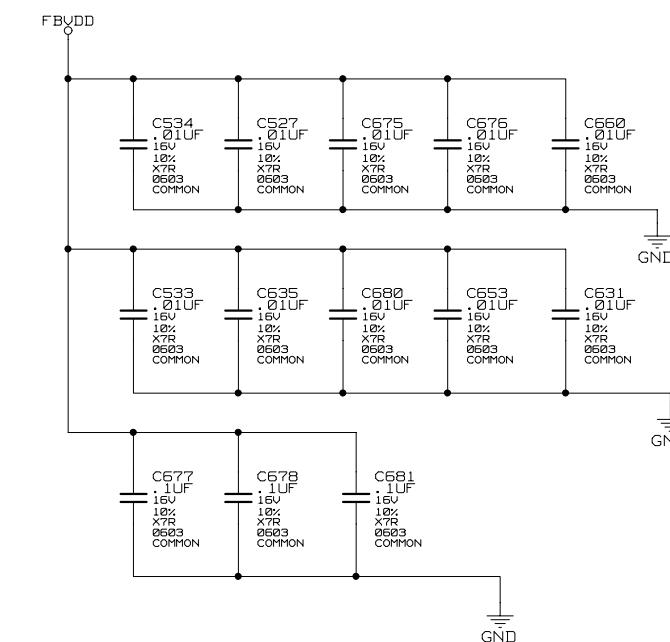
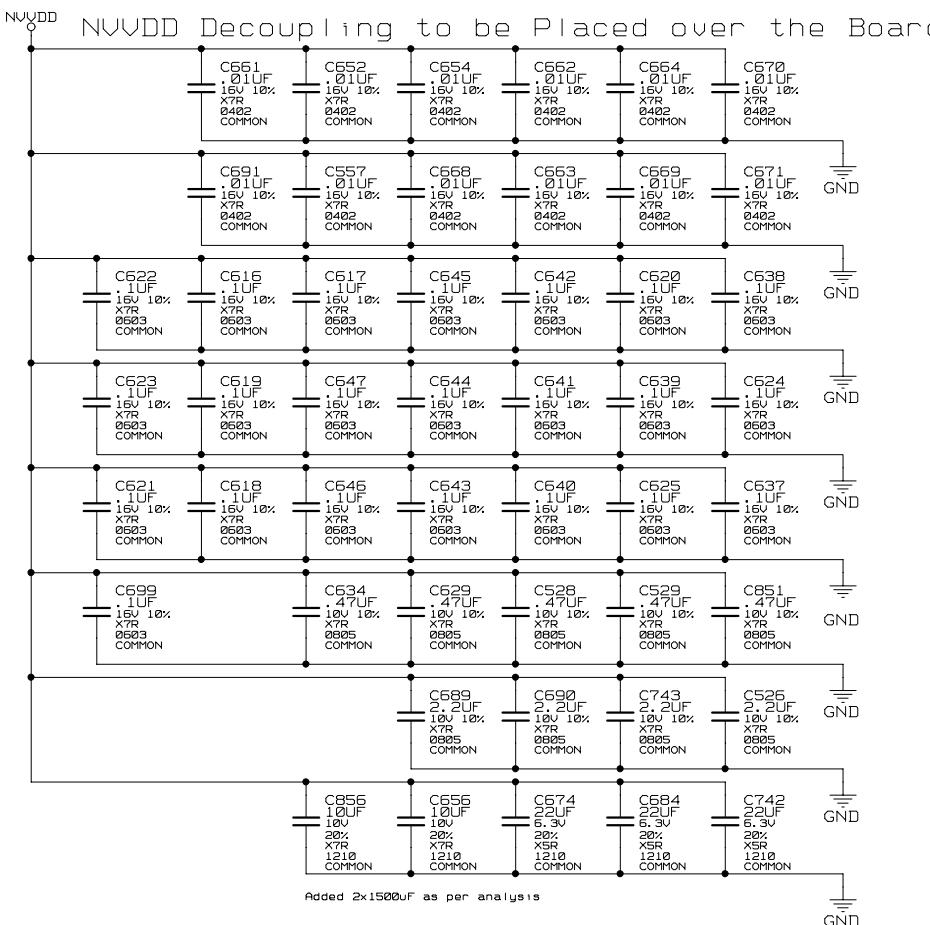
EXT POWER



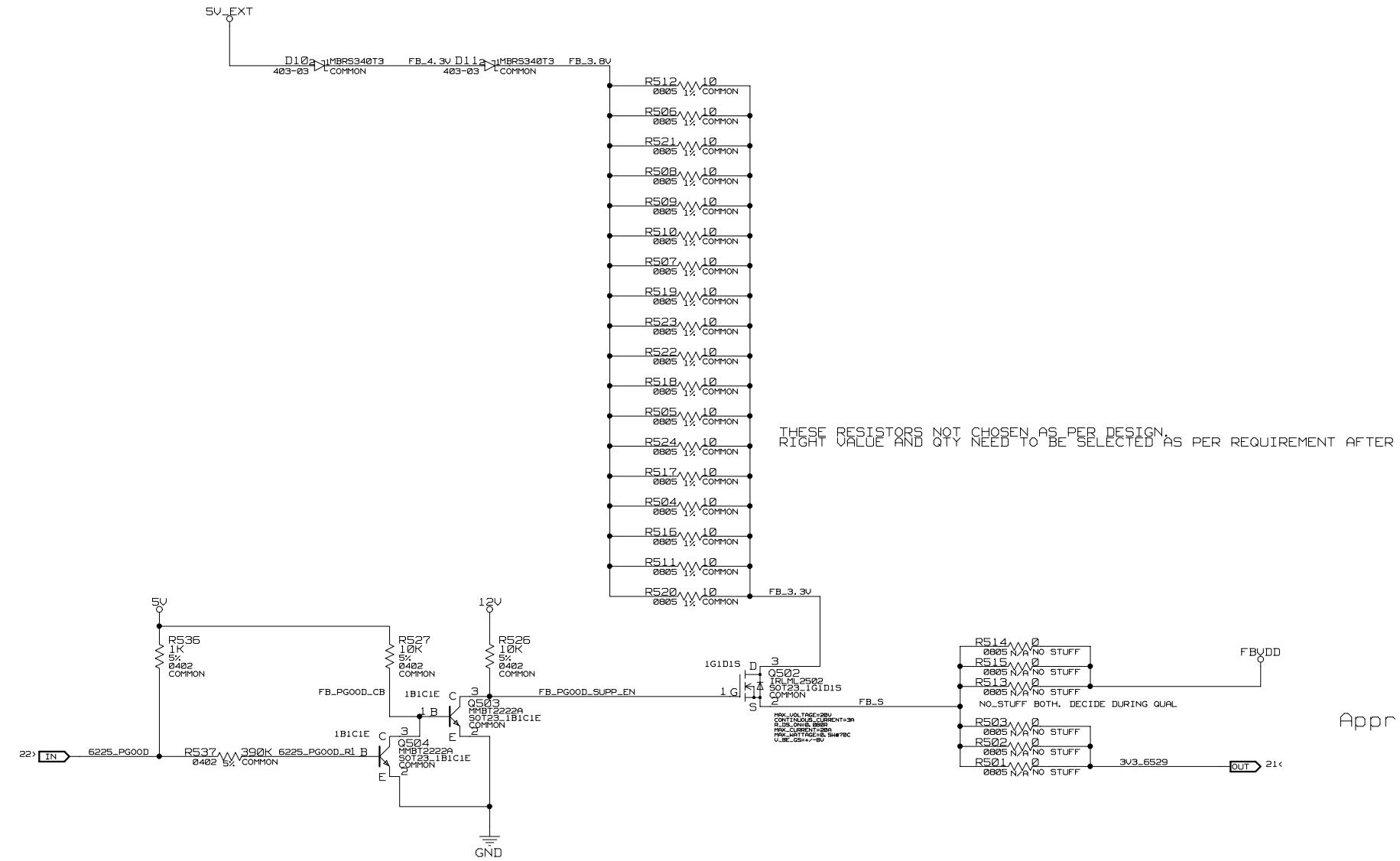
NOTE: Shutdown the power before connecting or disconnecting External Power GND

COMMON

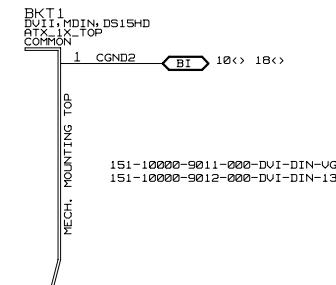
9. d. Memory Additional Decoupling



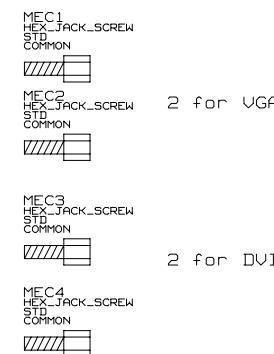
9. e. FBVDD/AGP3.3V Current Supplement



10. a. Mechanical



FANSINK SYMBOL AND PART NUMBER PENDING
BACK PLATE PART
SCREW PARTS- 155-00003-0000-000



*** Signal Cross-Reference for the entire design ***

3V3_6529 21< 25>
 SV_FUSED 21<
 SV_LDO_IN 21<
 12V_EXT 18<
 1394A_12U 18<
 1394A_12V_C 18<
 1394A_TPA 18<
 1394A_TPA* 18<
 1394A_TPBI 18<
 1394A_TPBI* 18<
 1394B_12U 18<
 1394B_12V_C 18<
 1394B_TPA 18<
 1394B_TPA* 18<
 1394B_TPBI 18<
 1394B_TPBI* 18<
 1394B_VDD 18<
 6225_BOOT1 22<
 6225_BOOT2 22<
 6225_ISEN1 22<
 6225_ISEN2 22<
 6225_LGATE1 22<
 6225_LGATE2 22<
 6225_PGOOD 22> 25<
 6225_PHASE1 22<
 6225_PHASE2 22<
 6225_UGATE1 22<
 6225_UGATE2 22<
 6225_VCC 22<
 6229_5V 21<
 6229_GND_FB 21<
 6229_LL_COMP 21<
 6229_LL_FB 21<
 6229_LL_GATE 21<
 6229_LL_GATE_R 21<
 6229_SW_12V 21<
 6229_SW_COMP 21<
 6229_SW_COMP3_FB 21<
 6229_SW_COMP_FB 21<
 6229_SW_DRH1 21<
 6229_SW_DRL0 21<
 6229_SW_FB 21<
 6229_SW_GH 21<
 6229_SW_GL 21<
 6229_SW_OUT 21<
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 FAN2_RETURN 19<
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 7114_VDDE 16<
 7114_VDDX 16<
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 AGPADSTBS1 3<
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 AGPDBILLO 3<
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 AGPSBA6 3<
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 AGPSBTF 3<
 AGPSBTBS 3<
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 AGPVREFCG_GPU 3<
 AGPUREFGC 3<
 AGPWBF 3<
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 CUBS_POUT 11< 17<
 CUBS_YOUT 11< 17<
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 D1D2CALPD_VDD1 26<
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*** Part Cross-Reference for the entire design ***	
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