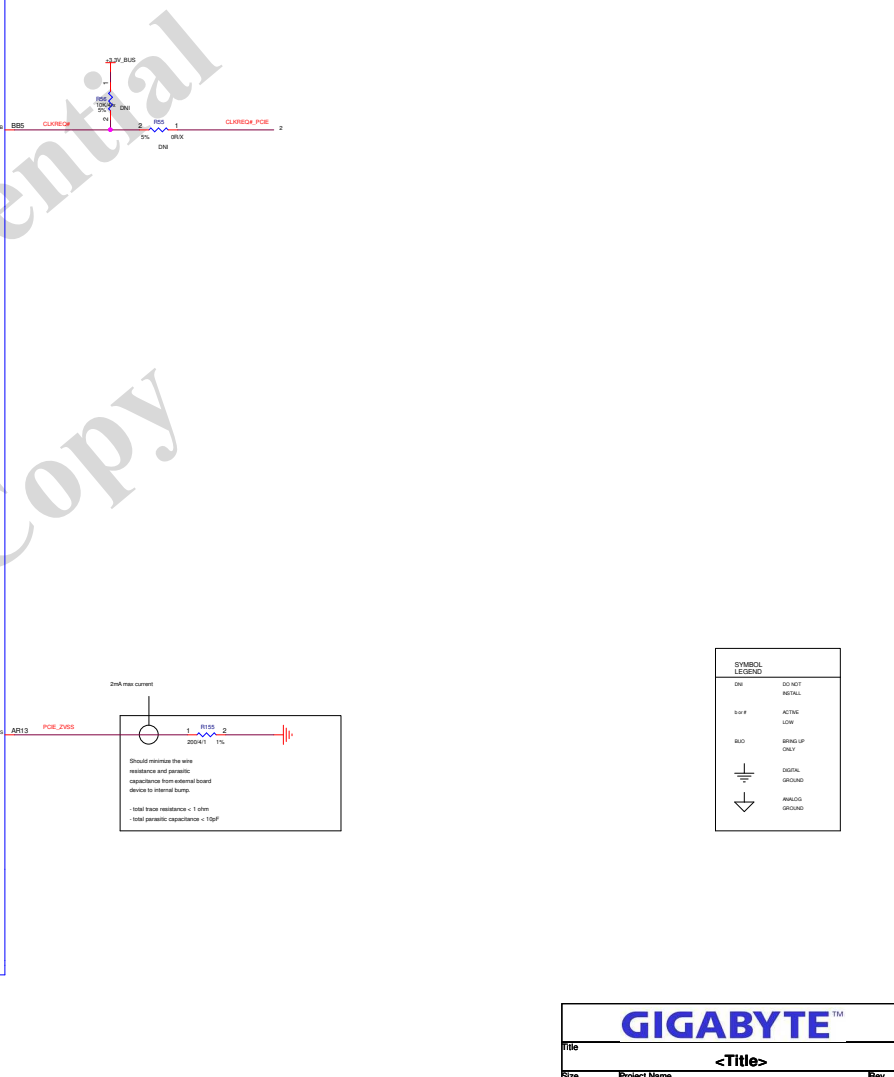
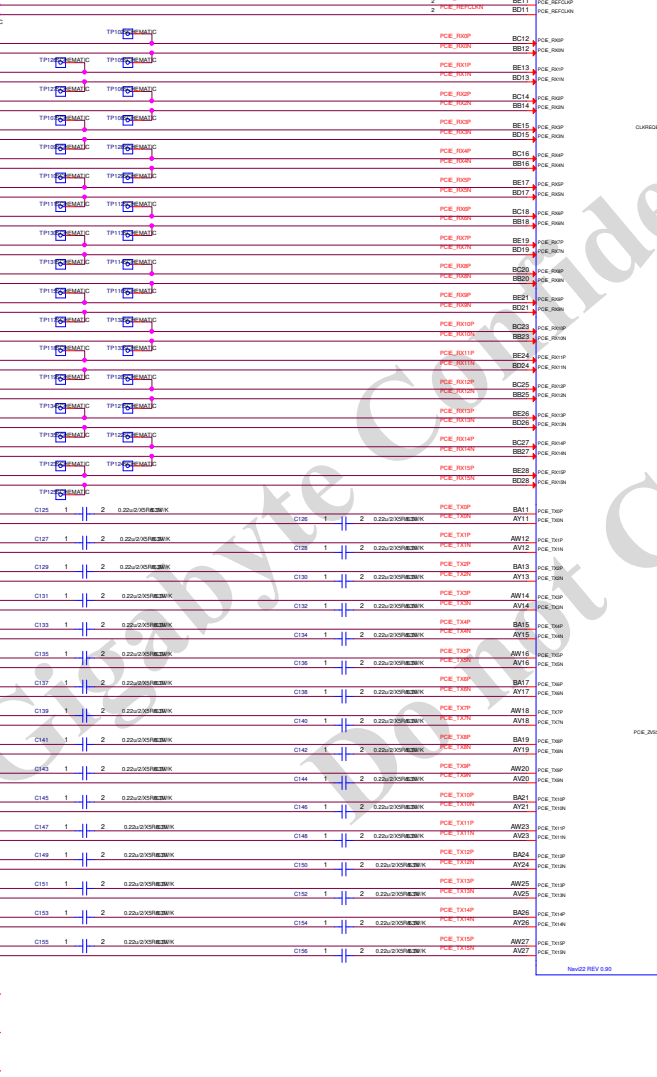
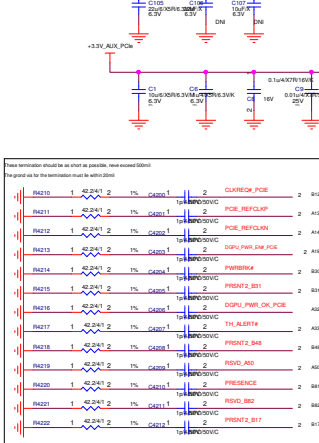
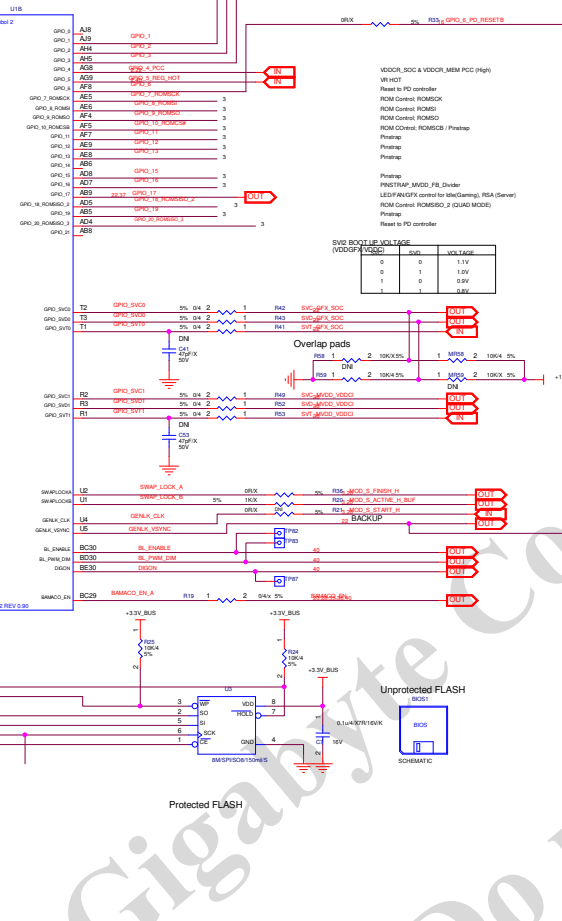


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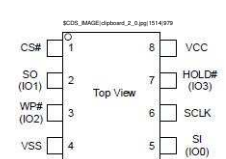
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2	NAVI22 PCIe Interface	27	VDDCR_SOC_PHASE 1 and 2
3	NAVI22 GPIOs	28	MVDD_VDDCI CONTROLLER
4	NAVI22 XTAL	29	REG MVDD
5	NAVI22 MEM CHAB	30	REG VDDCI
6	NAVI22 MEM CHCD	31	SMALL RAIL LDO
7	NAVI22 MEM CHEF	32	NAVI22 DECAPS
8	GDDR6 MEM CHAB	33	NAVI22 POWER
9	GDDR6 MEM CHCD	34	NAVI22 GND
10	GDDR6 MEM CHEF	35	POWER MANAGEMENT
11	NAVI22 TMDPAB - USB-C/DP	36	SVI2 & BAMAQD
12	NAVI22 TMDPCD - HDMI	37	MECHANICAL & THERMAL
13	NAVI22 TMDPEF - DP/DP	38	RADEON Lightbar
14	NAVI22 TMDPA	39	PI Debug
15	NAVI22 USB	40	DEBUG
16	PD Controller	41	BLOCK DIAGRAM
17	USB-C PORT 1 & DP	42	REVISION HISTORY
18	3.3V_AUX		
19	USB_5V_1.8V_0.75V		
20	MODS CONTROL & POWER		
21	REG_5V_BUCK		
22	VDDGFX_SOC CONTROLLER		
23	VDDCR_GFX PHASES 2 and 5		
24	VDDCR_GFX PHASES 1 and 4		
25	VDDCR_GFX PHASES 3 and 7		



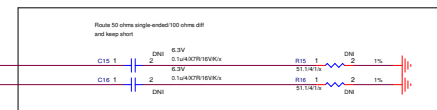
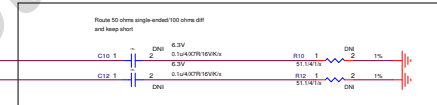
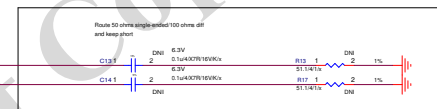
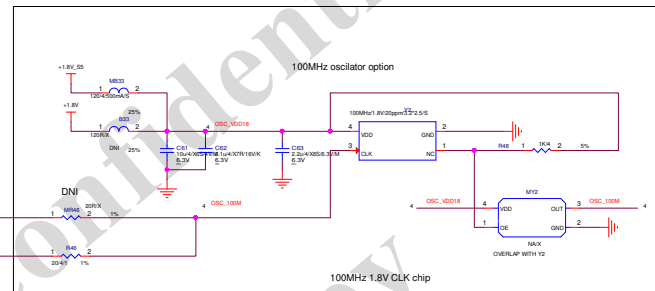
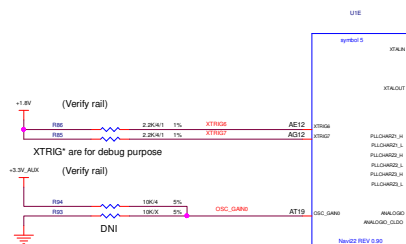
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Size	Project Name		Rev
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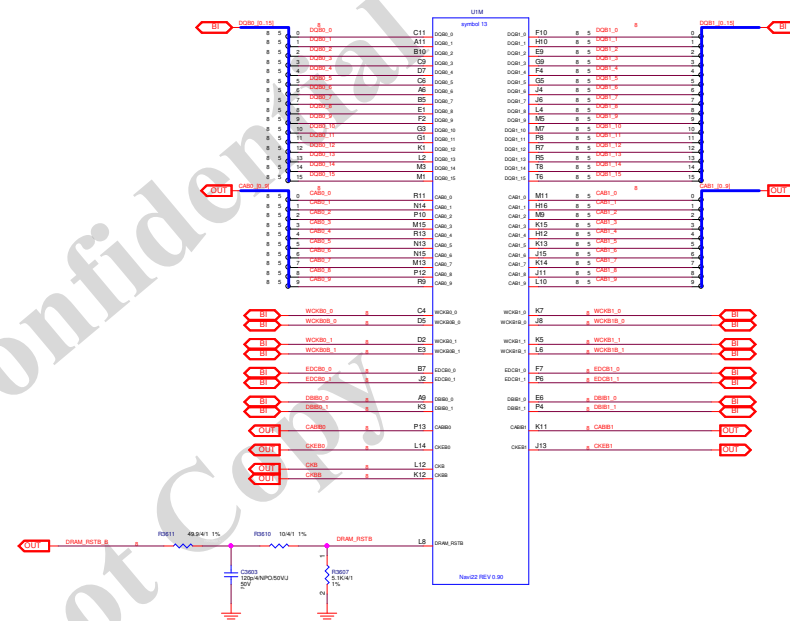
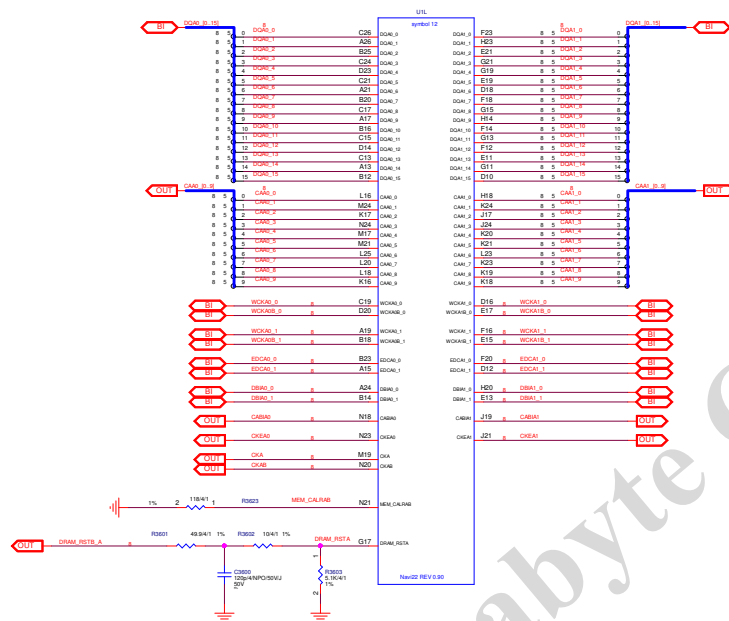


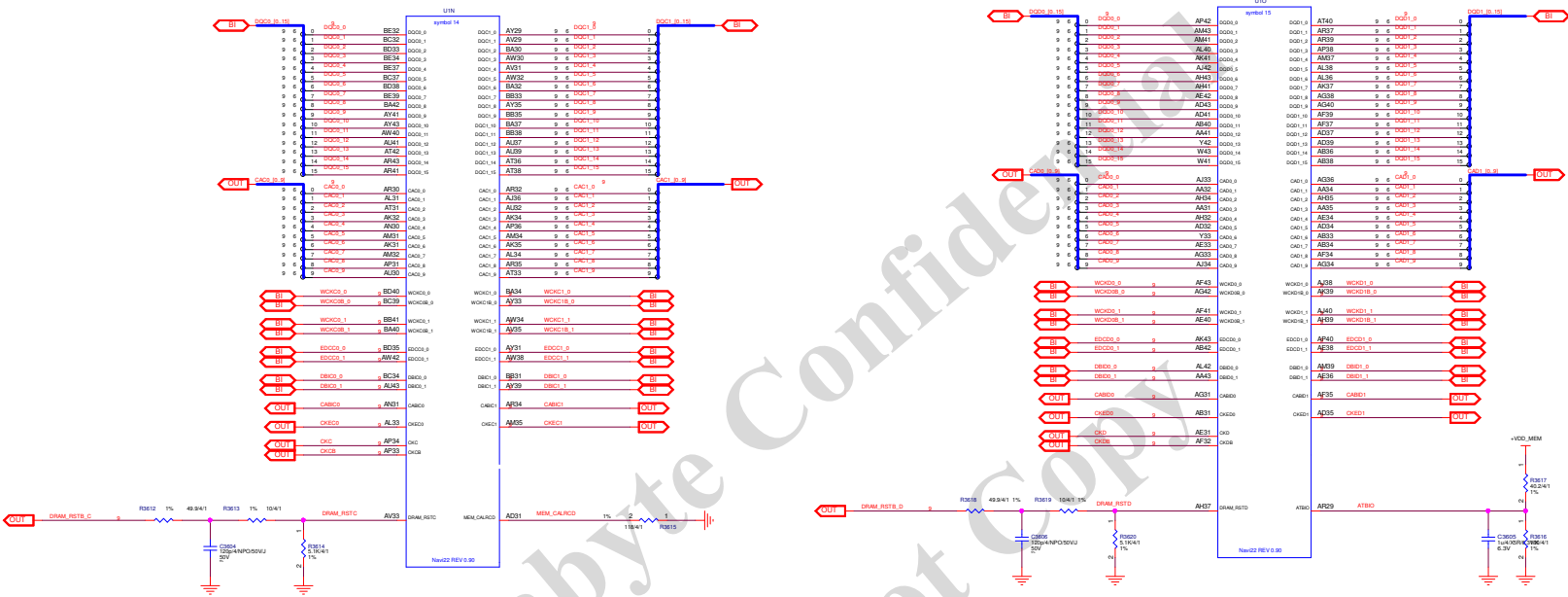
User	Internal Default Value	Definition
BIF		<p>STRAP_BIF_GEN4_DIS_A</p> <p>0: PCIe GEN4 supported 1: PCIe GEN4 not supported</p> <p>PINSTRAP_BIF_CLK_PM_EN</p> <p>0: CLAREDP power management capability is enabled 1: CLAREDP power management capability is disabled</p> <p>PINSTRAP_BIF_LC_TX_SWING</p> <p>0</p> <p>PINSTRAP_BIF_VGA_DIS</p> <p>0: VGA controller capacity enabled 1: The device won't be recognized as the system's VGA controller</p>
DCE		<p>PINSTRAP_AUD_PORT_CONN[2:0]</p> <p>Number of audio-capable display outputs</p> <p>0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected</p> <p>PINSTRAP_AUD[1:0]</p> <p>0</p> <p>1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if drcn is detected 3: Audio for DisplayPort and native HDMI</p>
Platform		<p>PINSTRAP_BOARD_CONFIG[2:0]</p> <p>LED/Fan/GFX control for site power</p> <p>PINSTRAP_MVDD_BOOT_VID_CONFIG</p> <p>0: Reflects current feedback divider 1: Ratio=1.1 with feedback divider installed</p>
SMU		<p>PINSTRAP_SMBUS_ADDR</p> <p>0: 0x11 1: 0x12</p>
		<p>PINSTRAP_ROM_CONFIG[2:0] 101</p>
DNI		<p>PINSTRAP_BIOS_ROM_EN</p> <p>0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device</p>

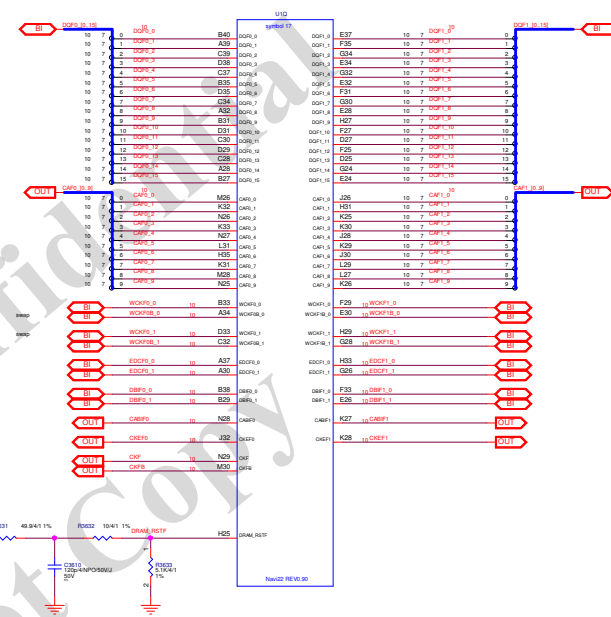
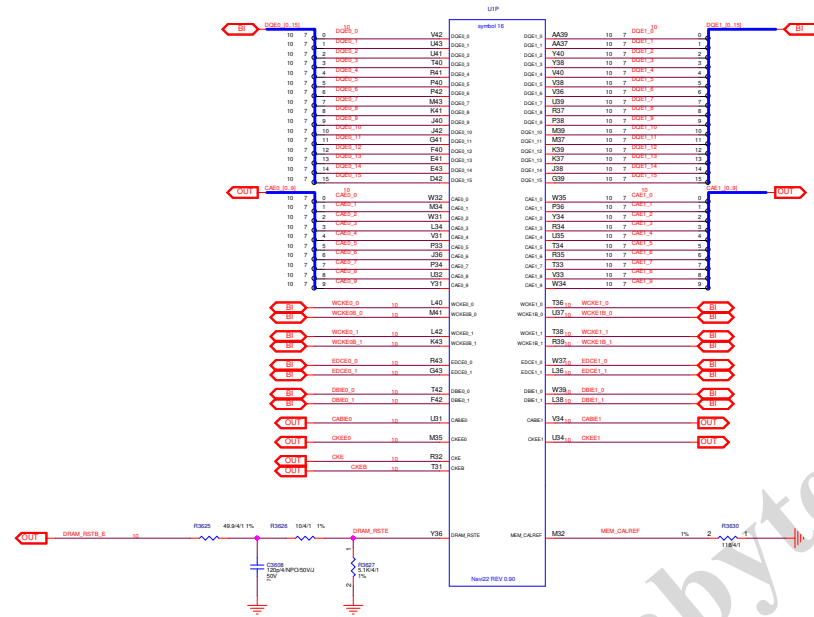


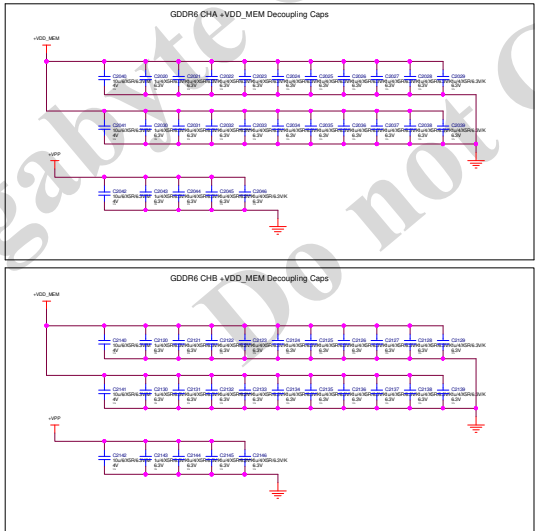
Default OSC_GAIN is 0x7. Pull-up OSC_GAIN0 to 3.3V_S5P
When 0x7, external clock chip connect to XTALOUT and leave XTALIN unconnected.

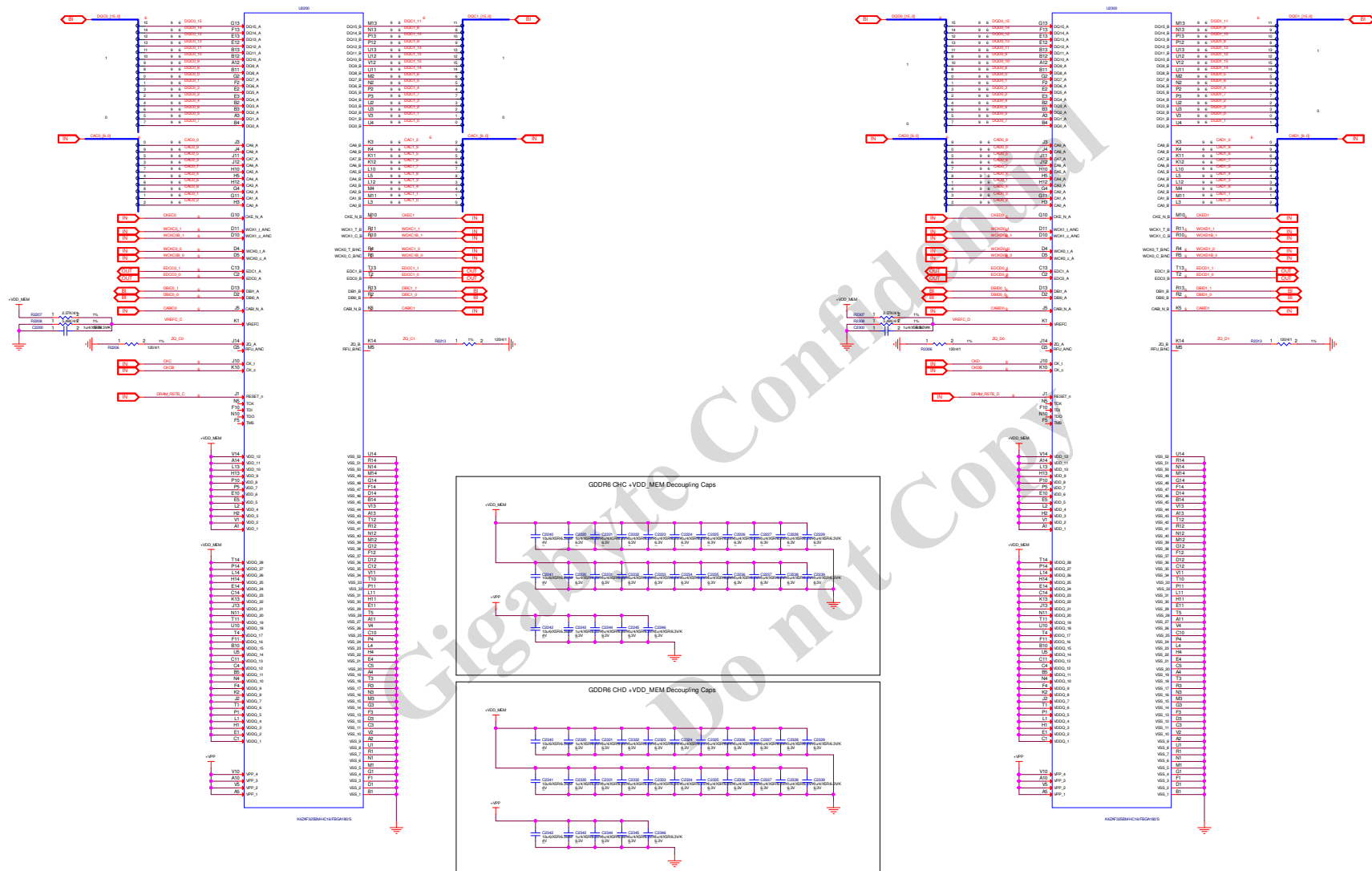


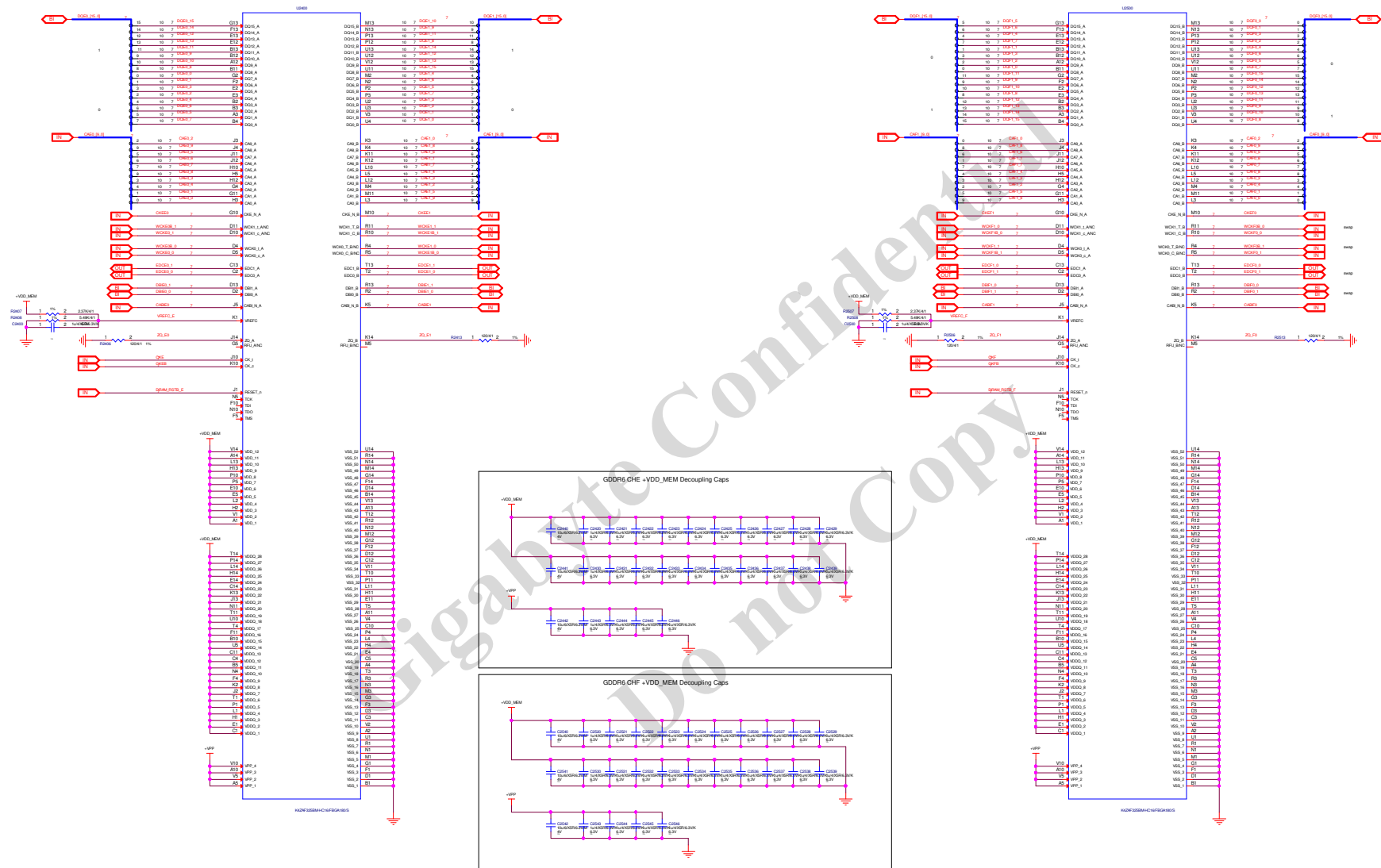


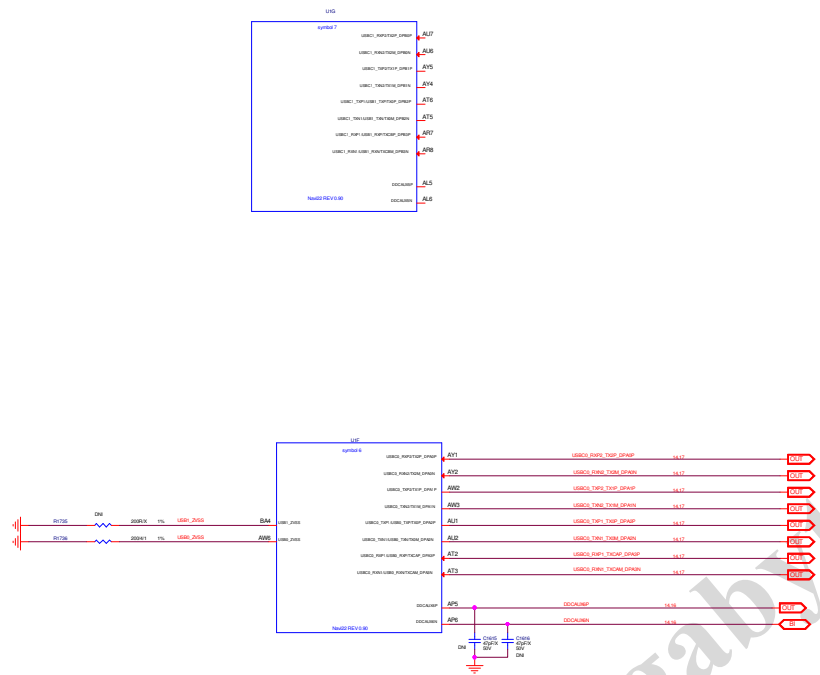


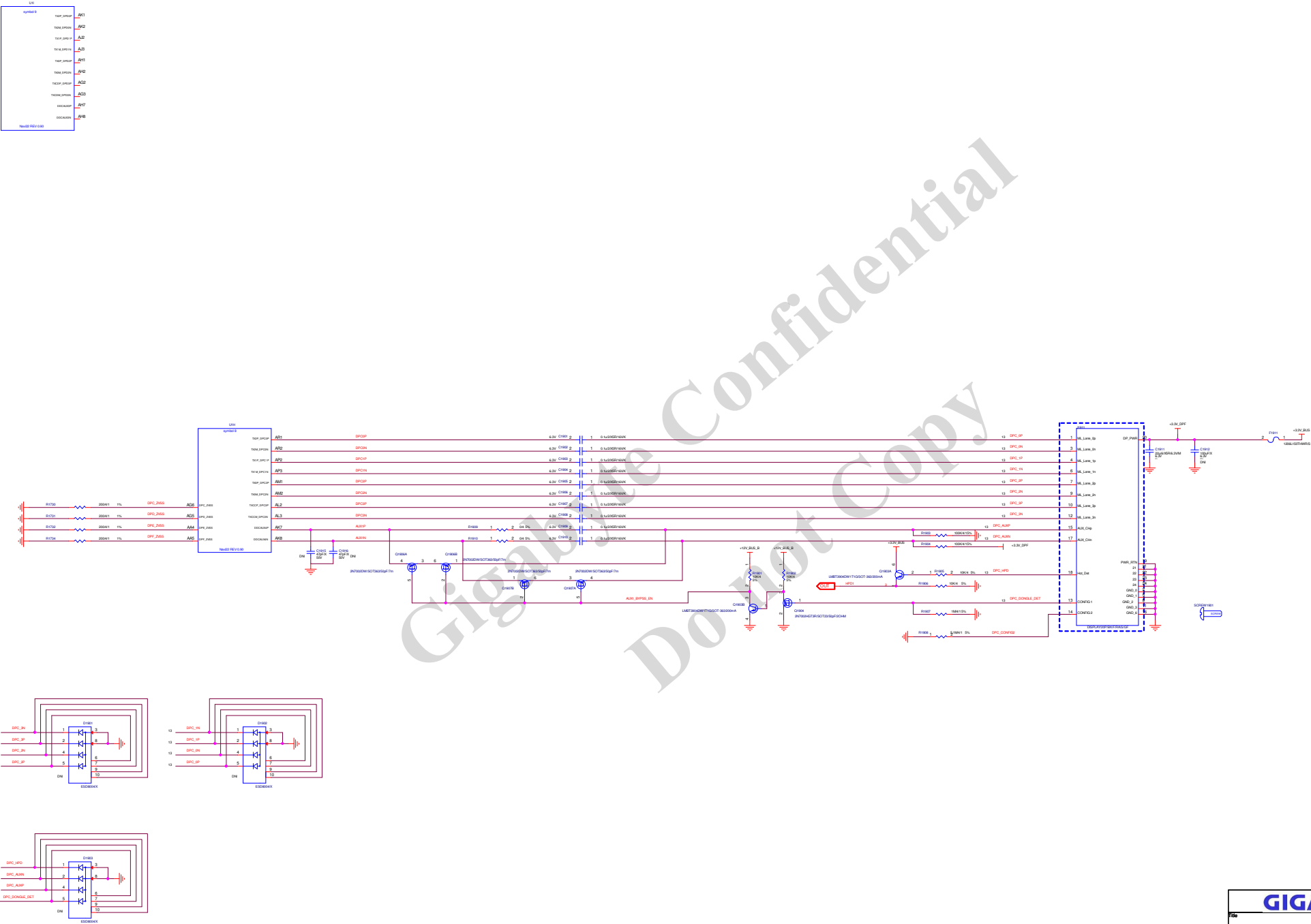


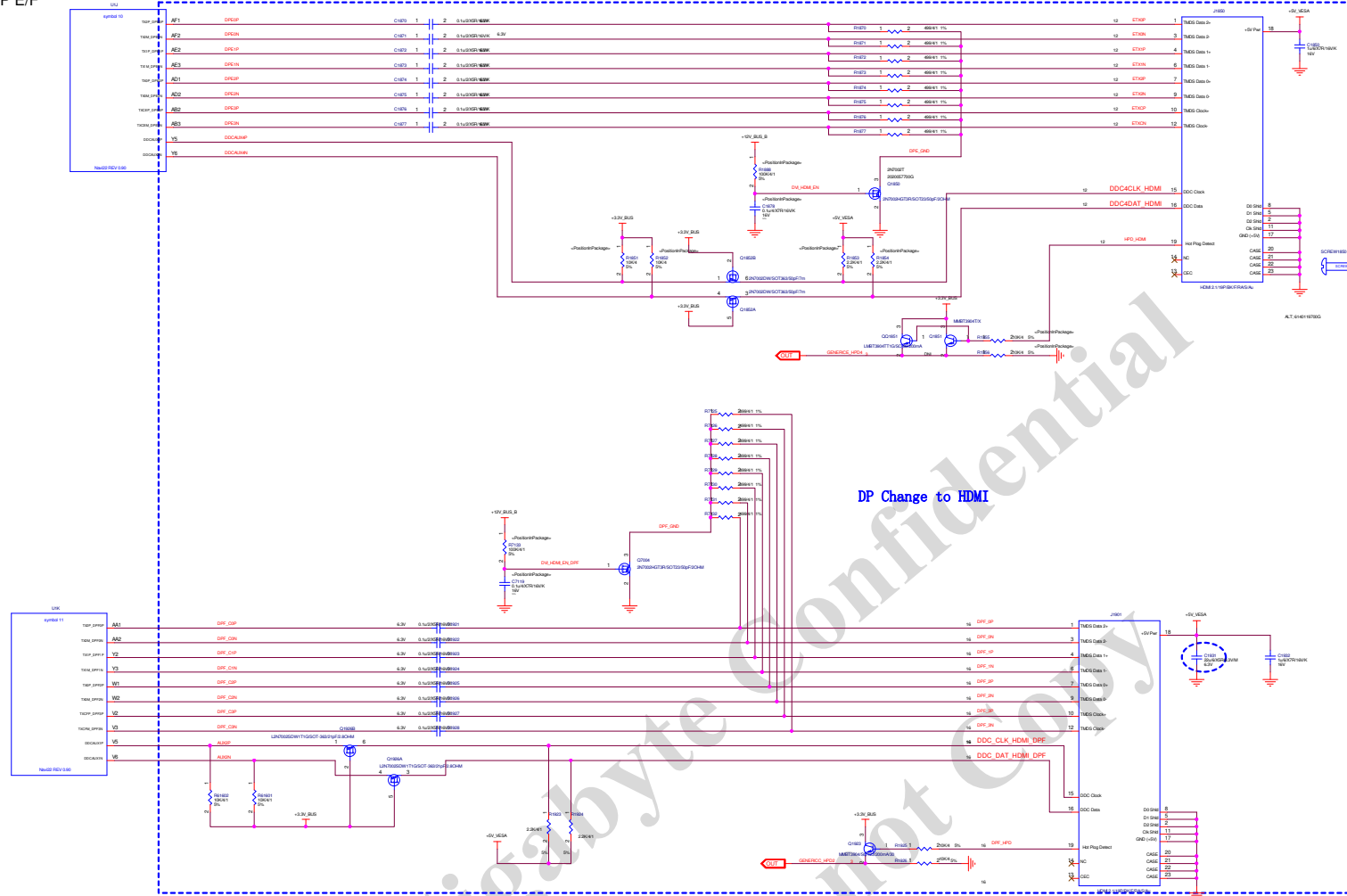




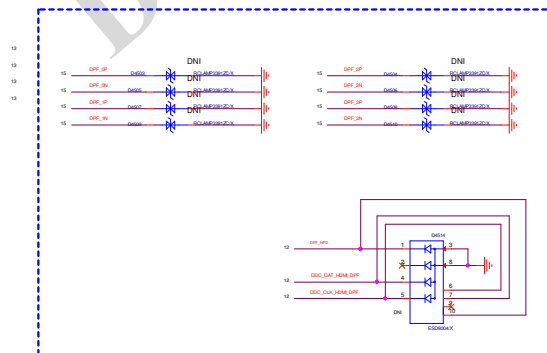
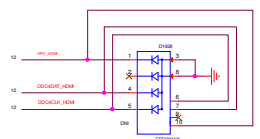








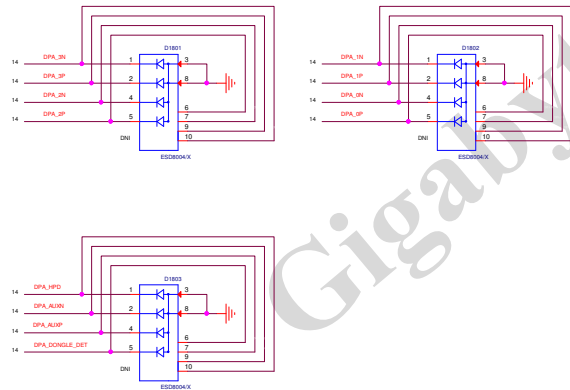
OPTIONAL ESD PROTECTION DIODES

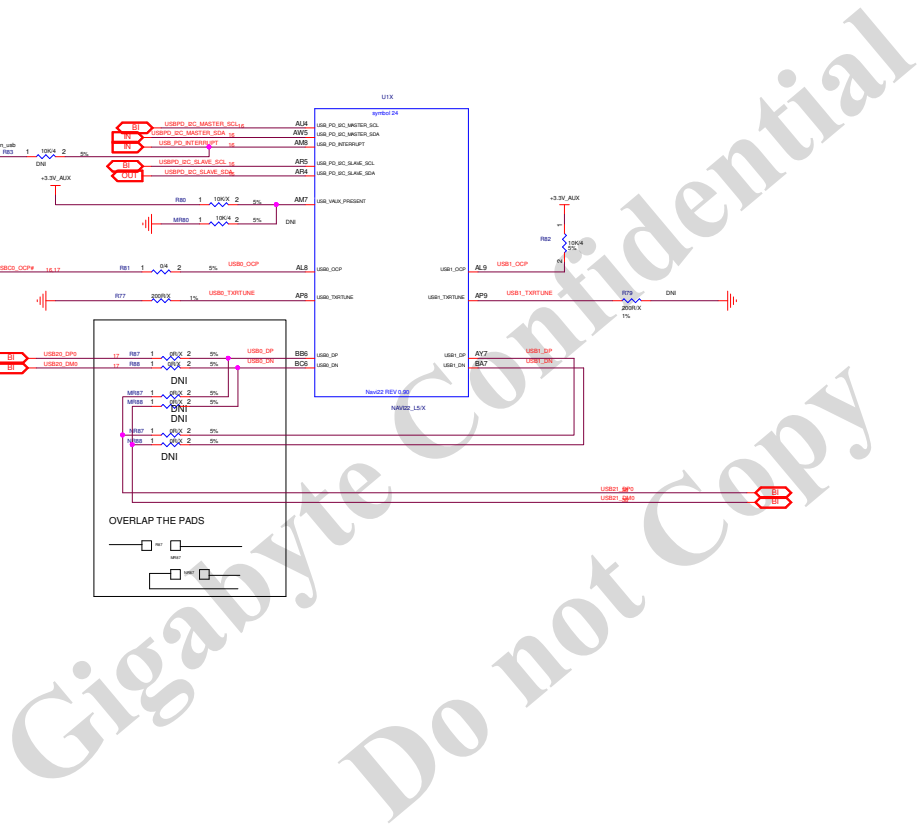


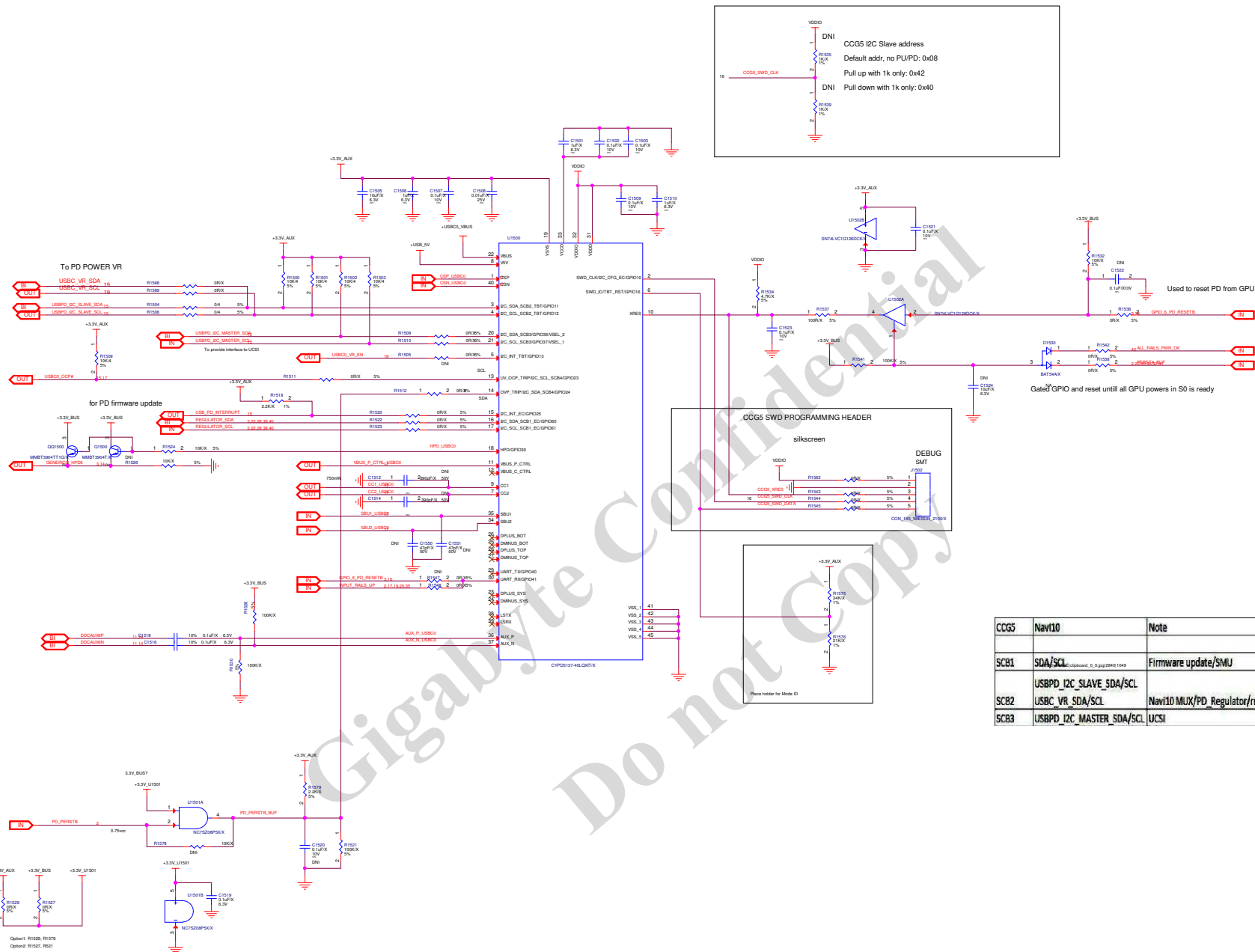
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GIGABYTE

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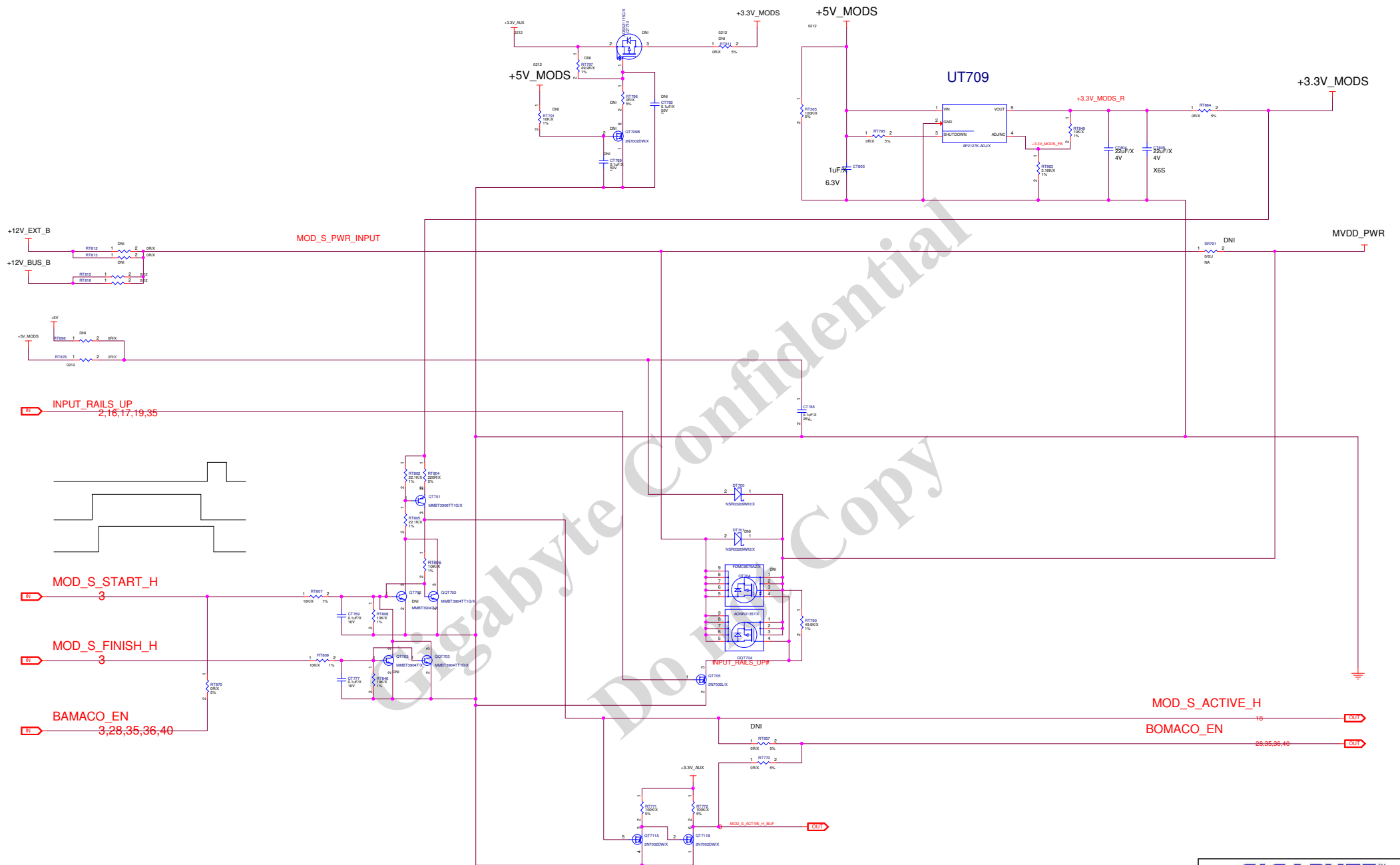


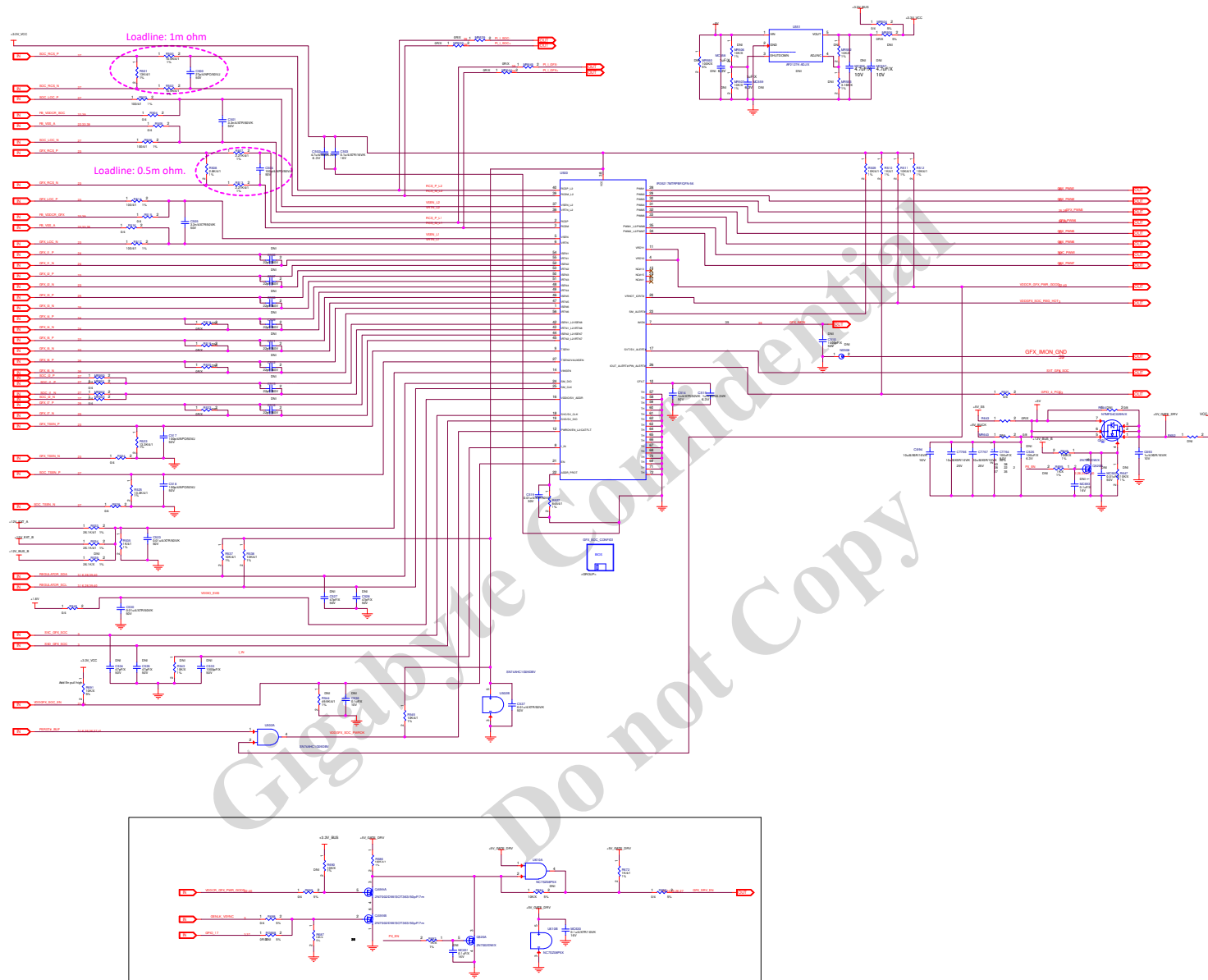


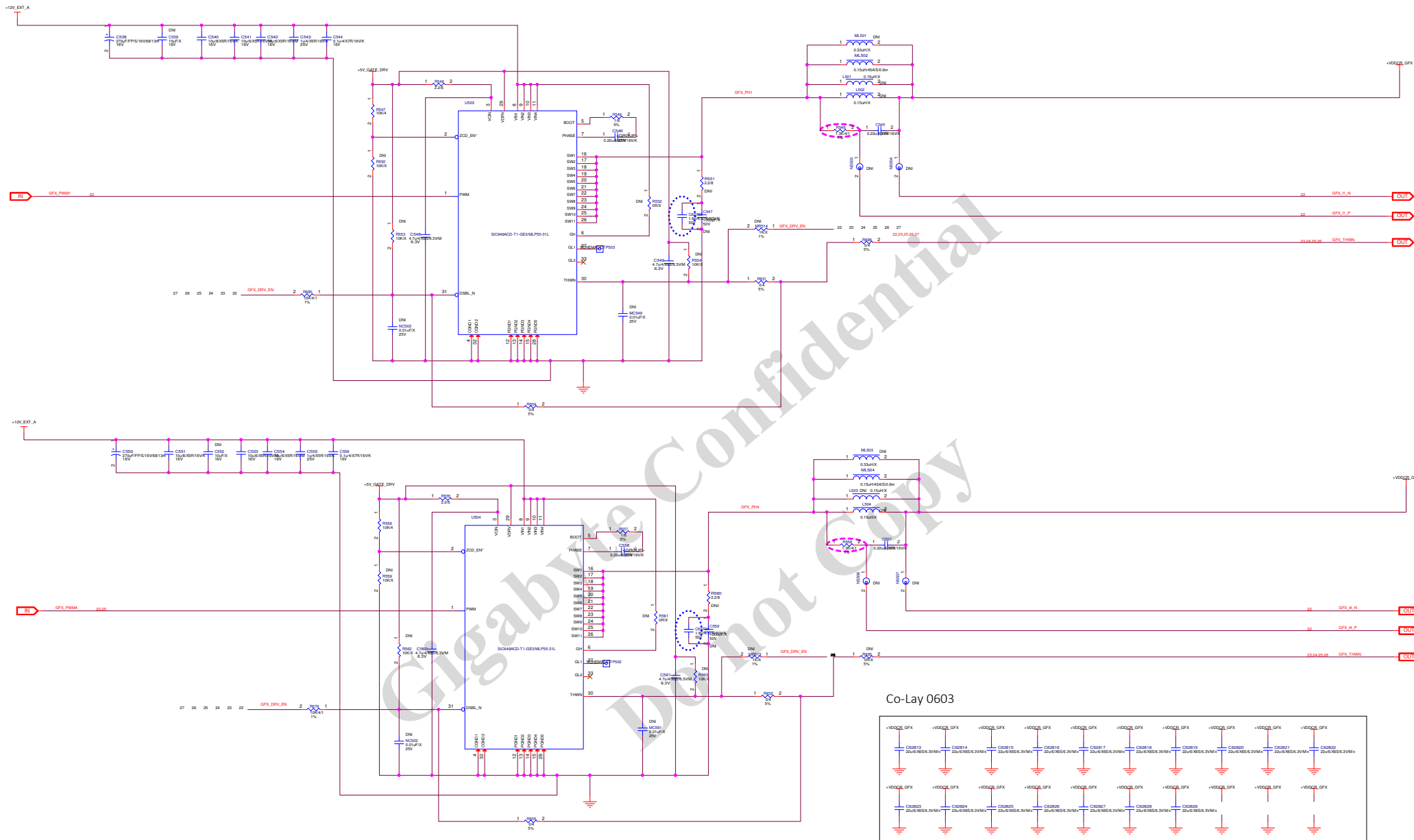


CCG5	Nav110	Note
SCB1	SDA/SCL <small>0x40000000 + 0x00000000 + 0x00000000 + 0x00000000</small>	Firmware update/SMU
SCB2	USBPD_I2C_SLAVE_SDA/SCL USBC_VR_SDA/SCL	Nav110 MUX/PD_Regulator/re-driver
SCB3	USBPD_I2C_MASTER_SDA/SCL	UCSI

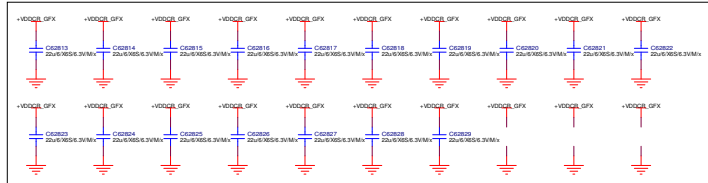


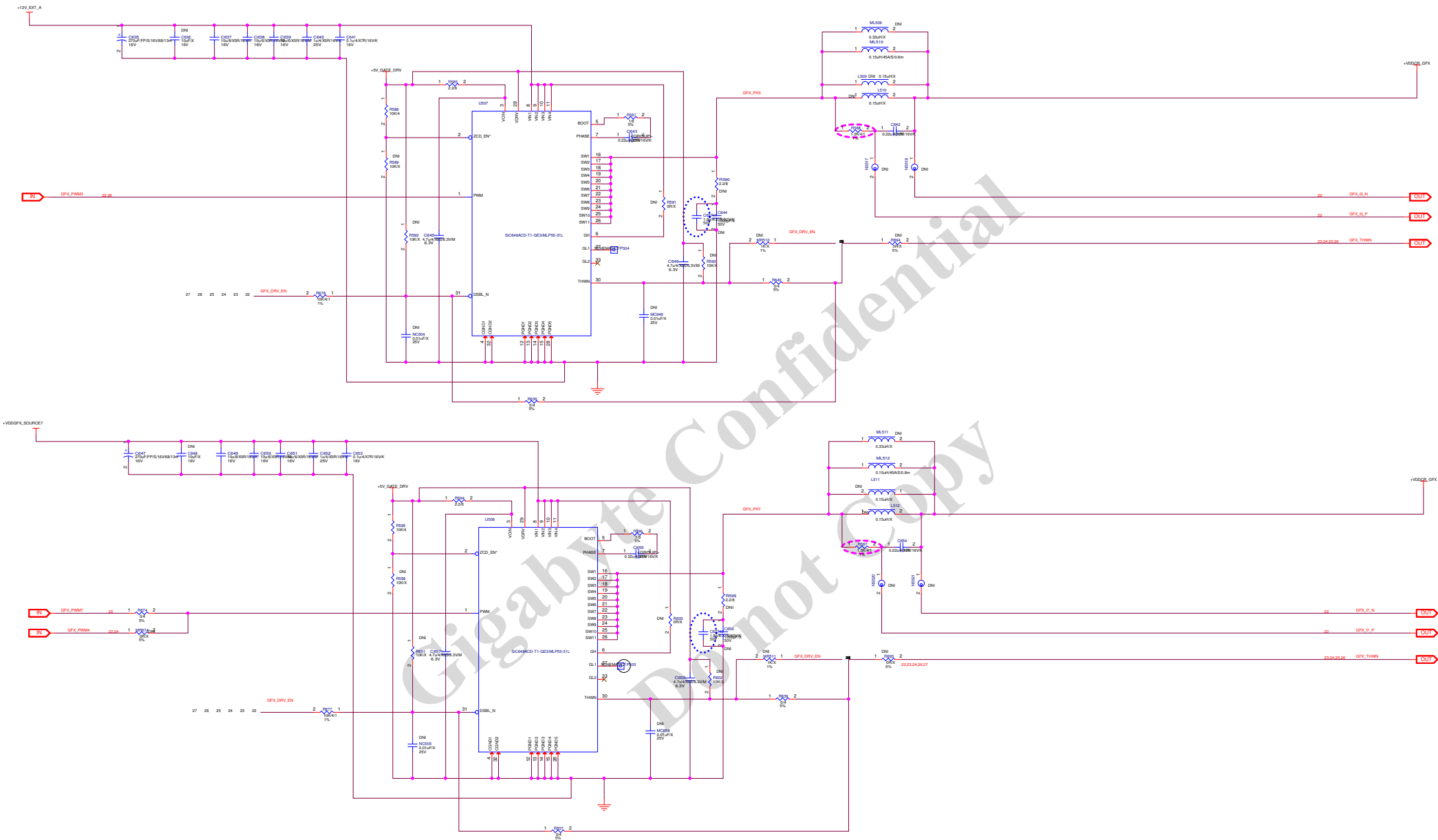


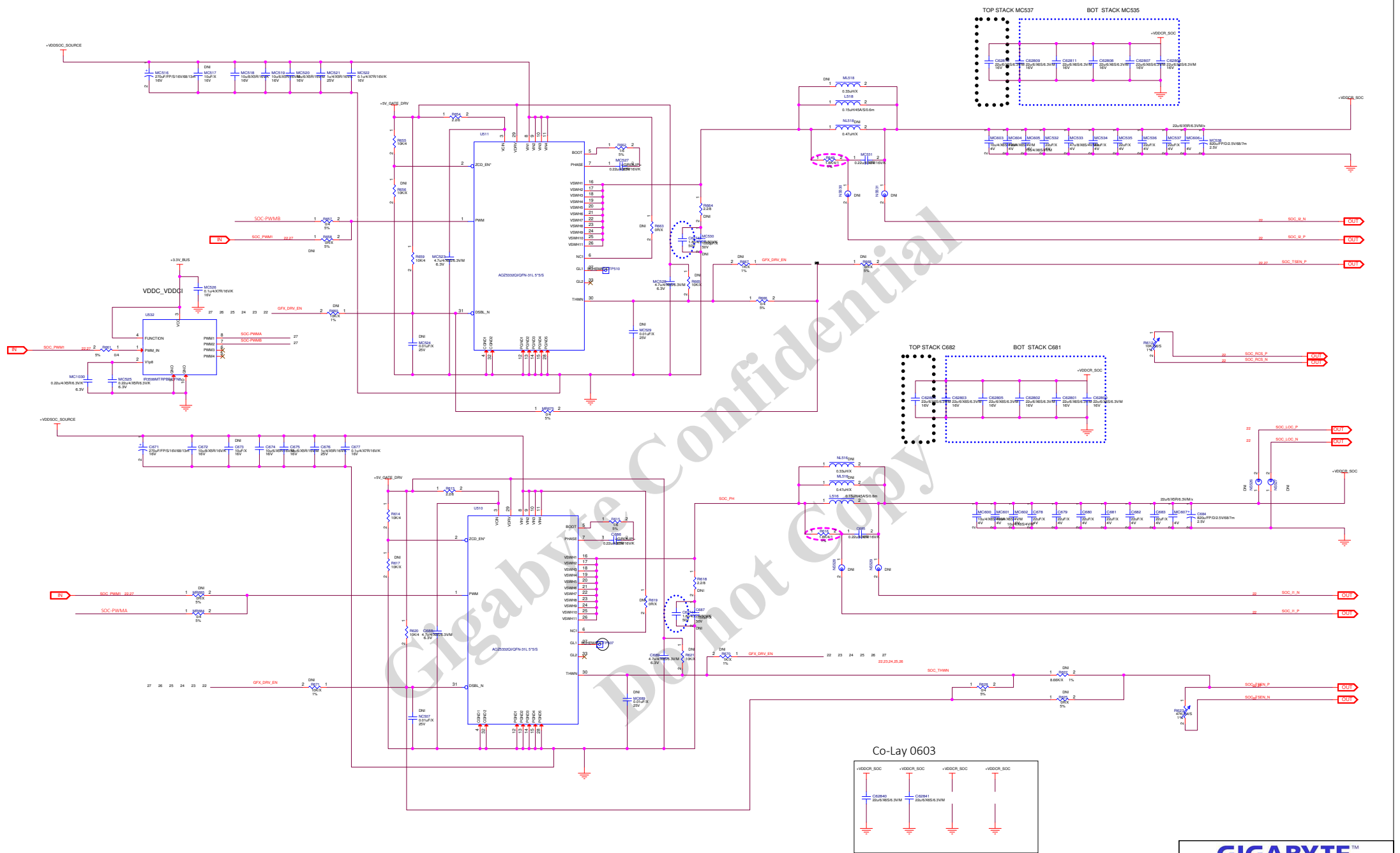


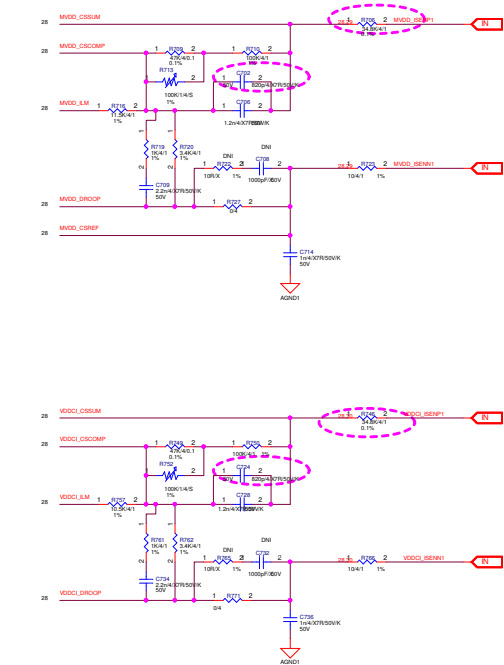
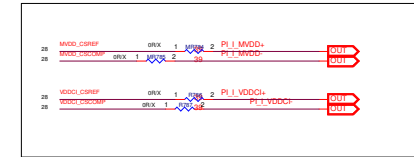
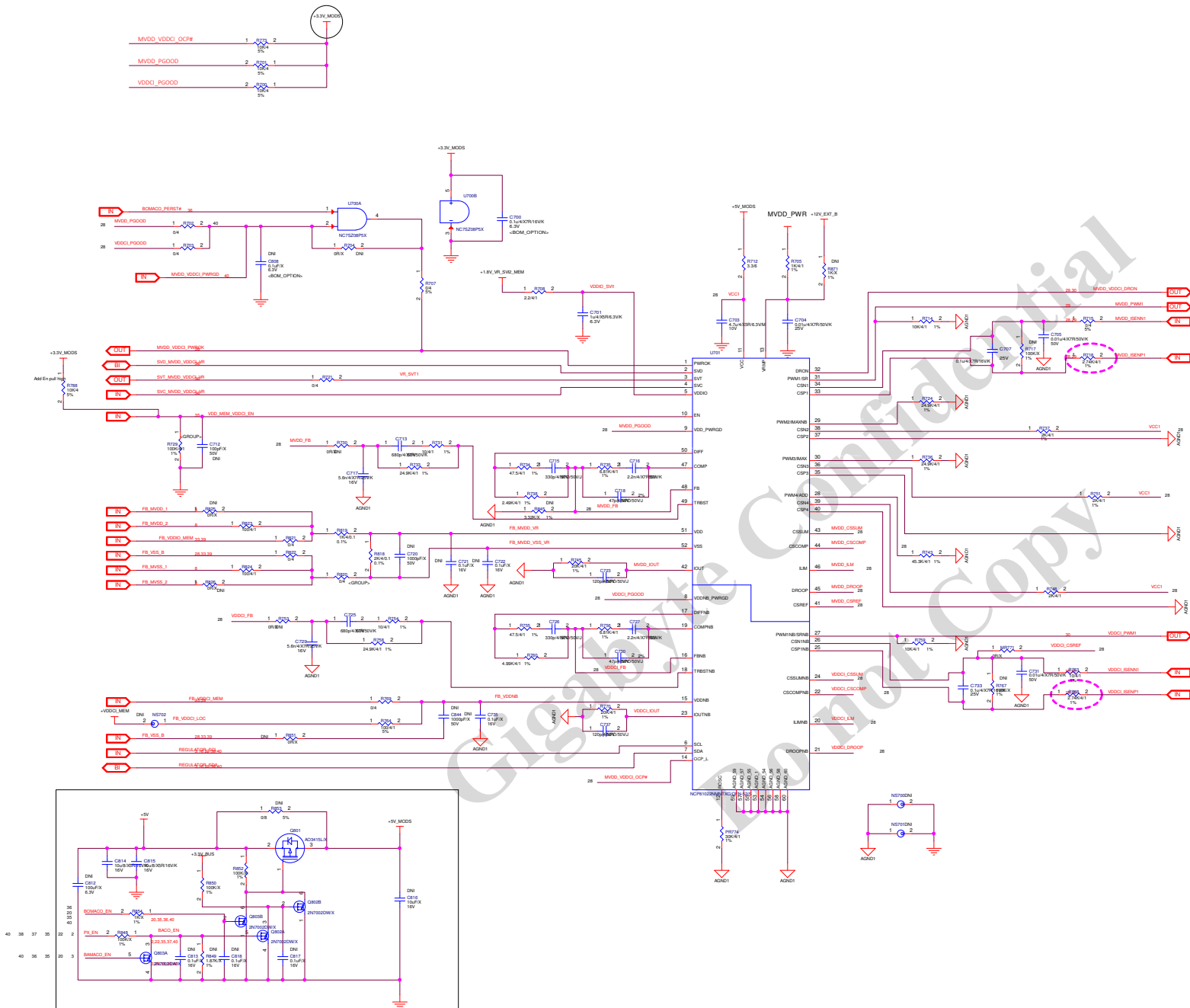


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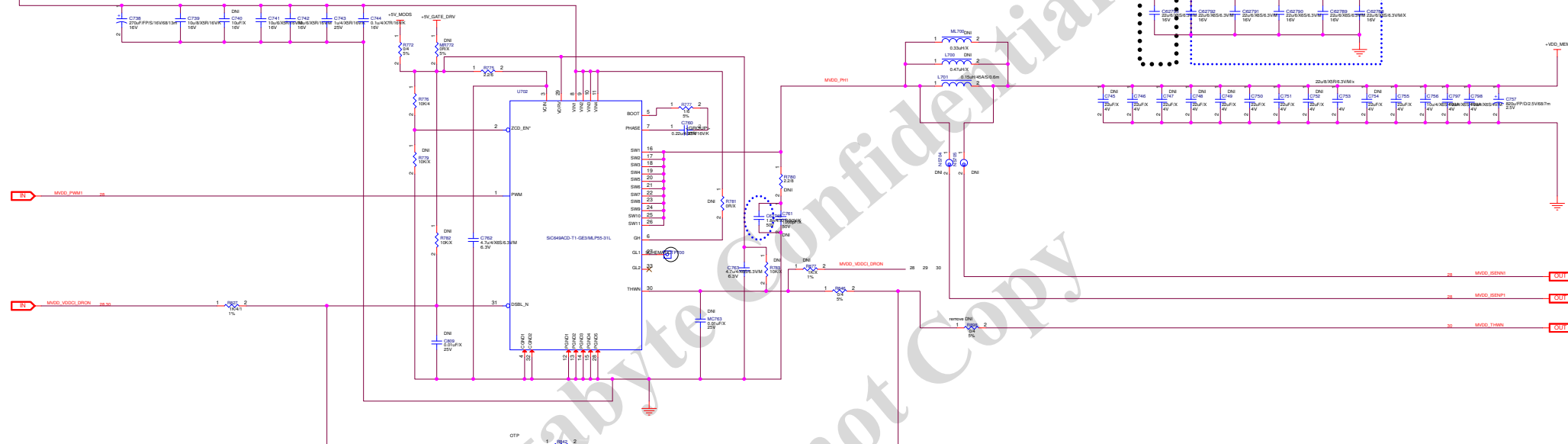




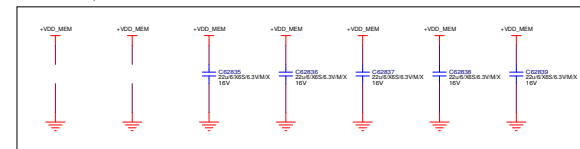




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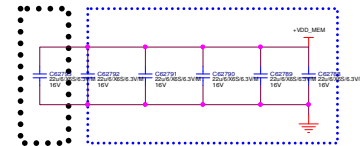


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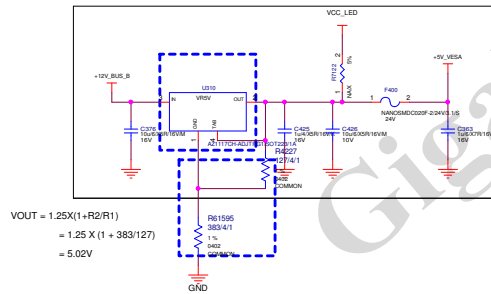
TOP STACK C753

BOT STACK C754

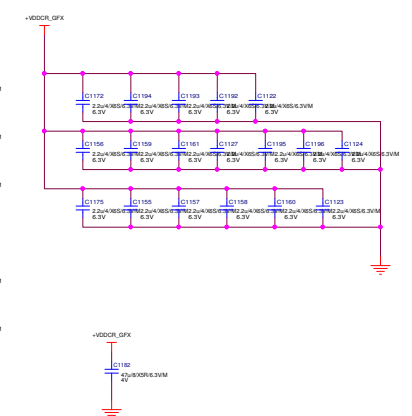
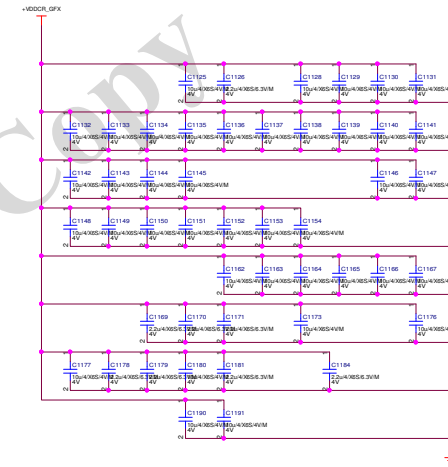
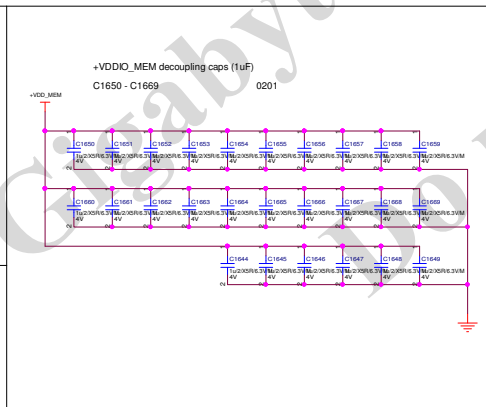
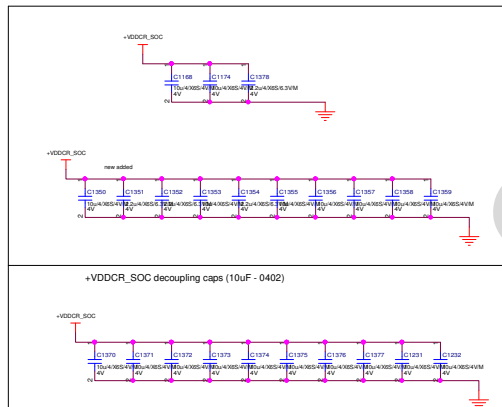
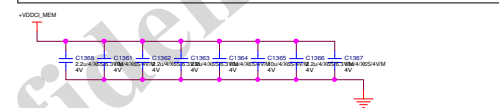
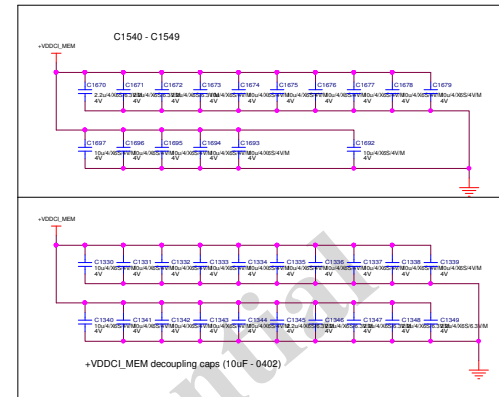
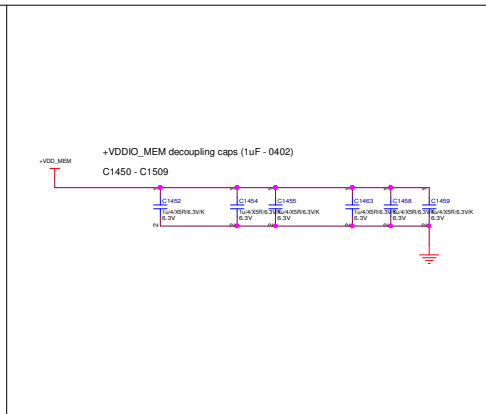
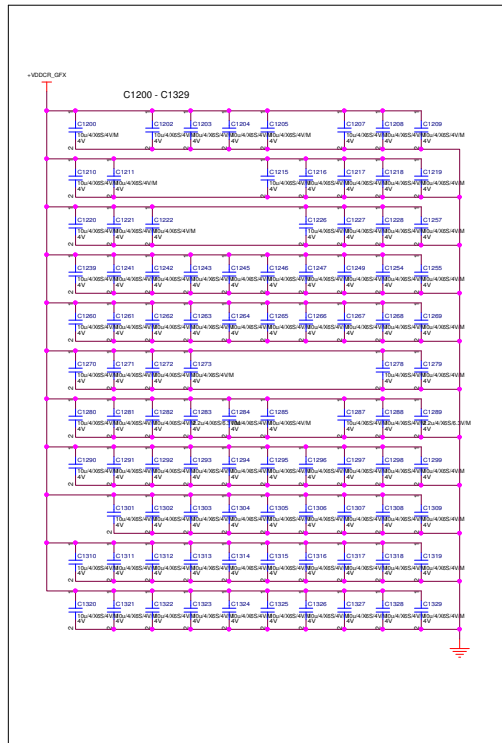


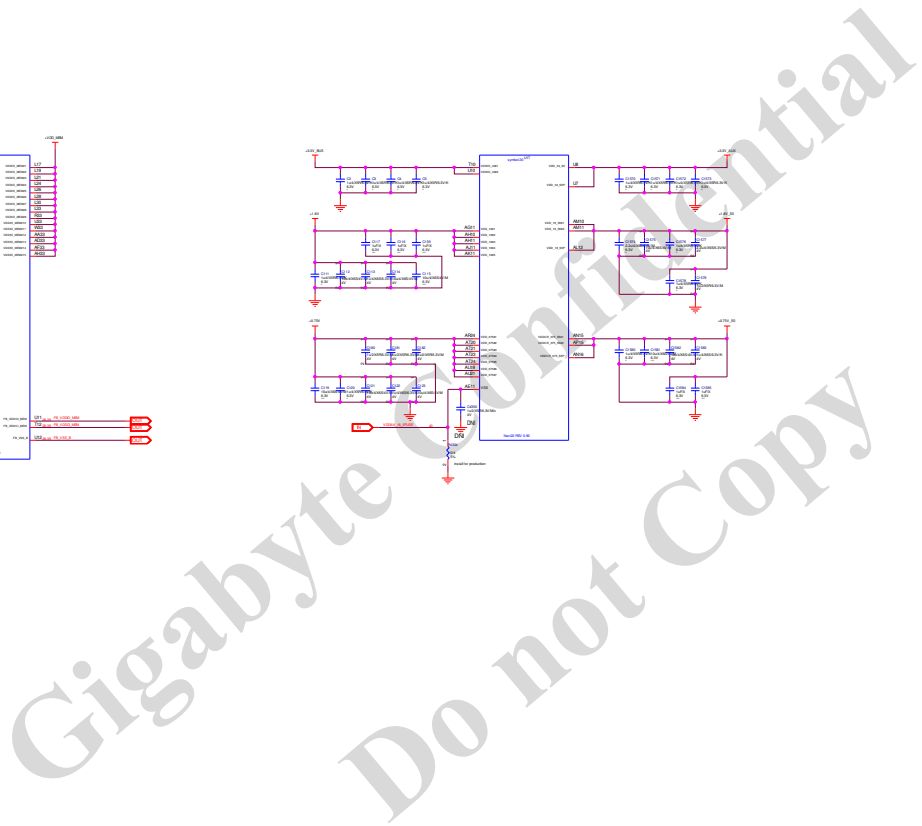
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Size	Project Name	Rev	
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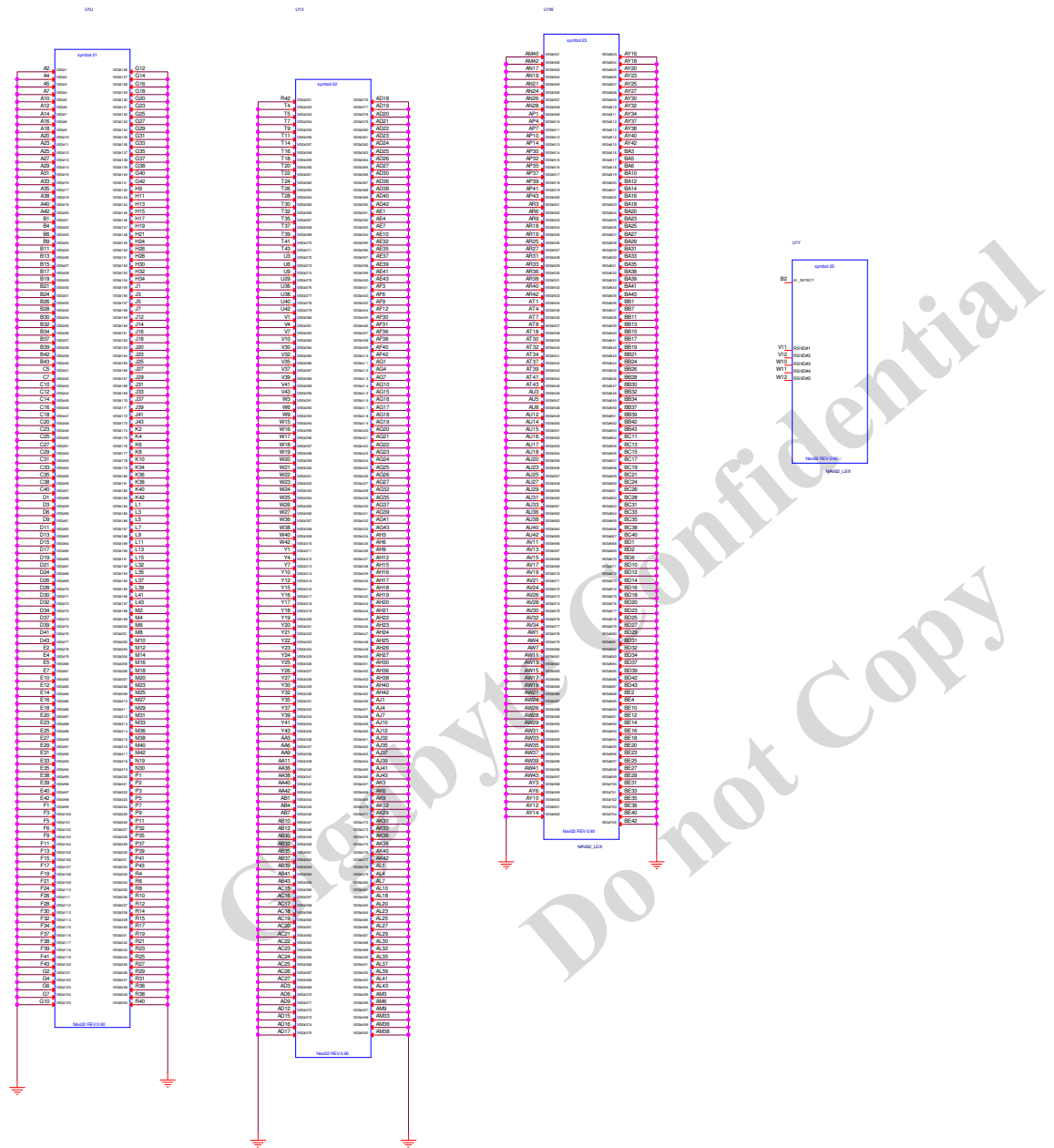
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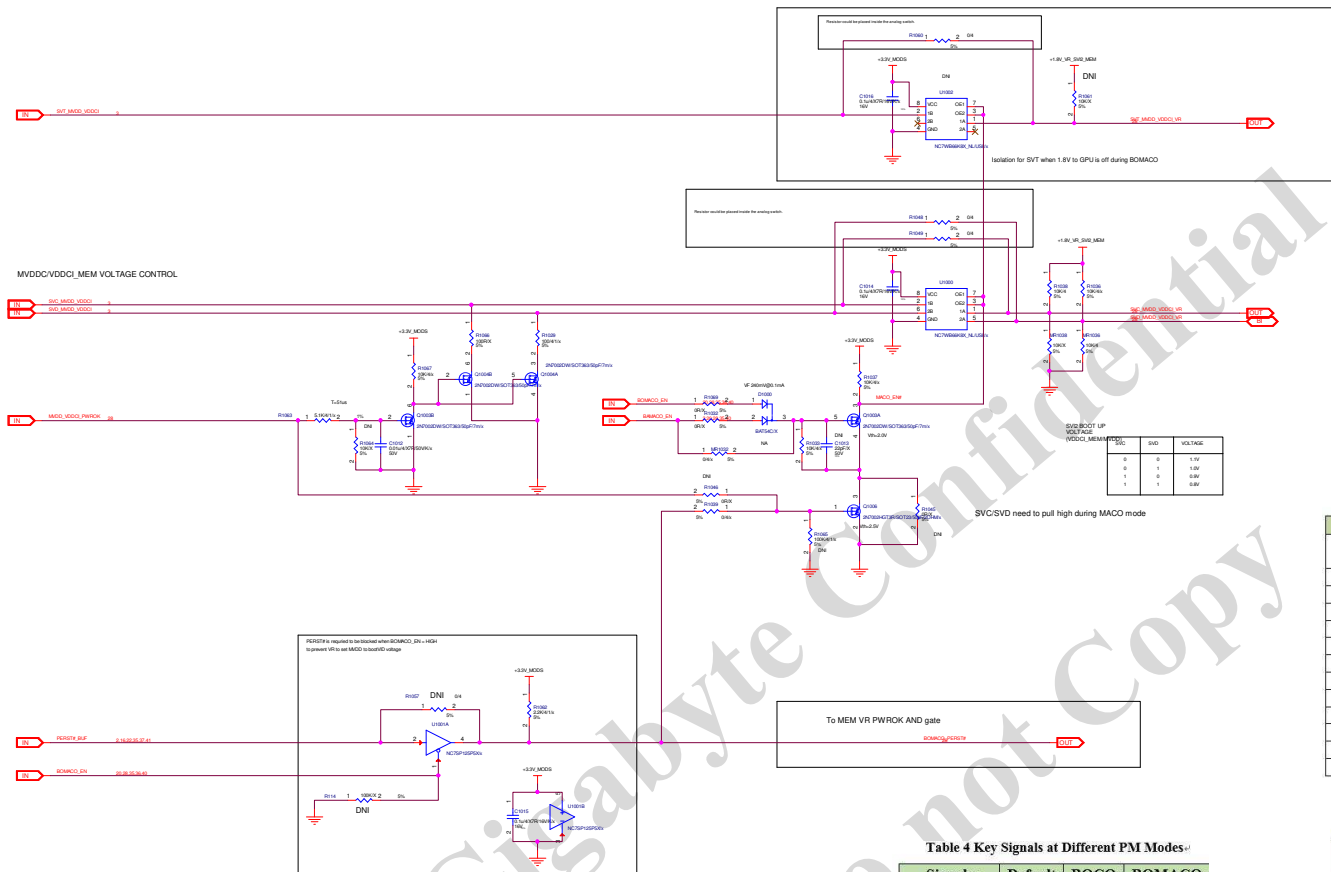


$$\begin{aligned} V_{OUT} &= 1.25X(1+R_2/R_1) \\ &= 1.25 \times (1 + 383/127) \\ &= 5.02V \end{aligned}$$









MODE	SW	VOLTRMS
0	0	1.8V
0	1	1.8V
1	0	1.8V
1	1	1.8V

Table 3 Power Rails Status at BOMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	ON
VDDIO_PCIE	PCIe PHY	ON
VDDAN_C	PHY	ON
VDDAN_18	PLL, PHY, etc	ON
VDDIO_18	1.8V GPIO, I2C, etc	ON
VDDIO_33	3.3V GPIO	ON
VDDAN_* EFUSE	EFUSE	ON
VDDCR_S5*	USB	ON

Table 3 Power Rails Status at BOMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status for BOMACO-A
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	OFF
VDDIO_PCIE	PCIe PHY	OFF
VDDAN_C	PHY	OFF
VDDAN_18	PLL, PHY, etc	OFF
VDDIO_18	1.8V GPIO, I2C, etc	OFF
VDDIO_33	3.3V GPIO	OFF
VDDAN_* EFUSE	EFUSE	OFF
VDDCR_S5*	USB	ON

Table 4 Key Signals at Different PM Modes

Signals	Default	BOCO	BOMACO
PX_EN	LOW	N/A	N/A
MACO_EN	N/A	N/A	N/A
PERSTb	HIGH	1->0->1	1->0->1
PWR_EN	HIGH	LOW	LOW
BOMACO_EN	LOW	LOW	HIGH

Table 5 Platform to Support BOMACO

BOMACO_EN	SVC PU/PD	SVD PU/PD
HIGH	PU	PU
LOW	bootVID	bootVID

GIGABYTE

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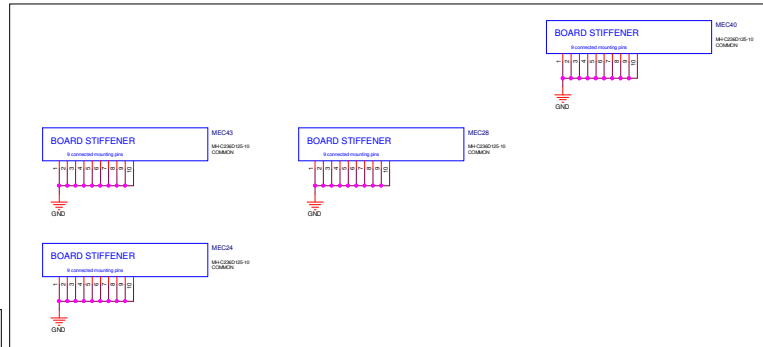
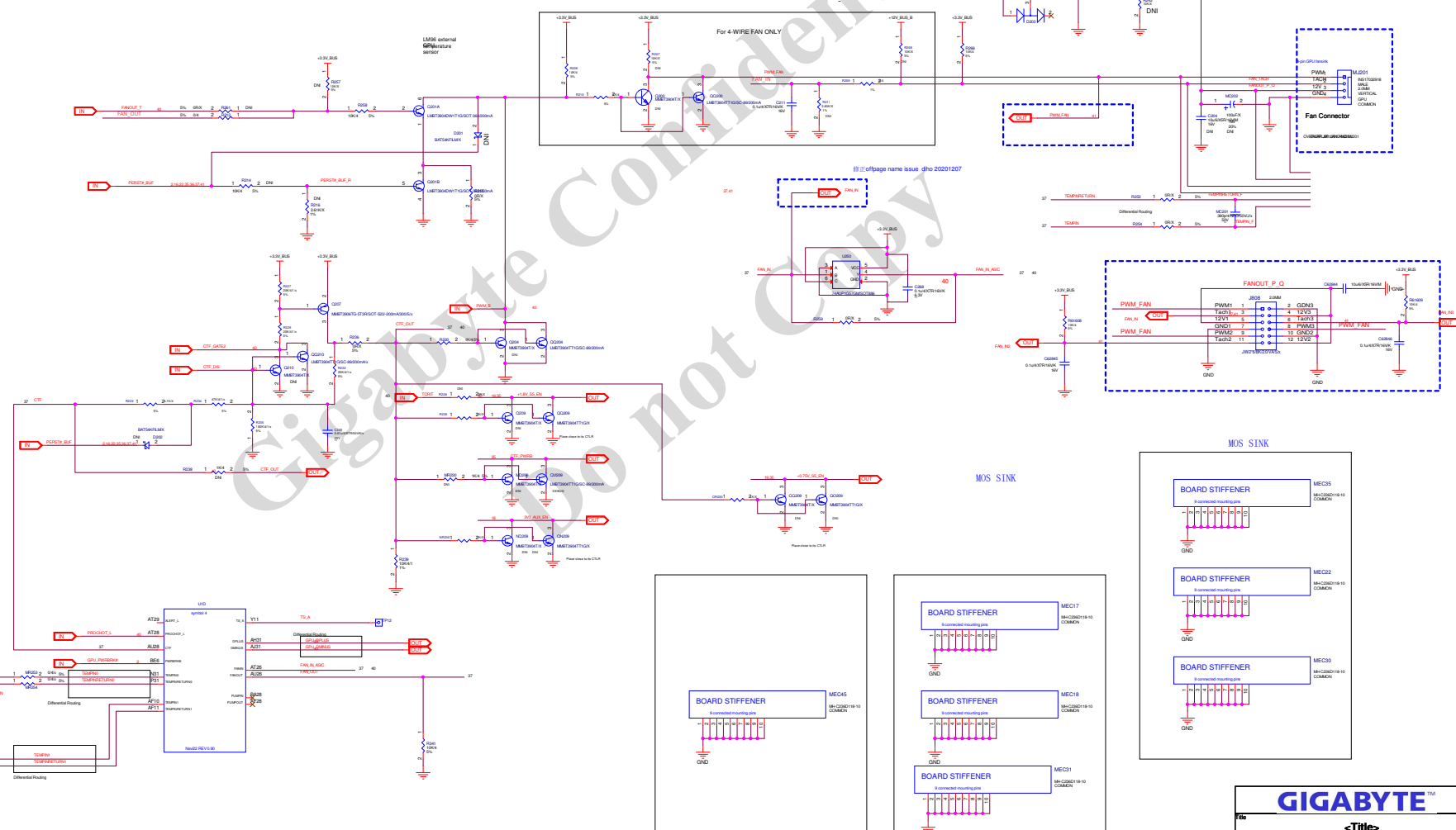


Figure 1 shows six board stiffener connection diagrams, each with a title box and a pin connection diagram. The diagrams are arranged in a 3x2 grid. Each diagram shows a 16-pin connector with pins 1-8 connected to a common ground and pins 9-16 connected to a common ground. The diagrams are labeled MEC37, MEC33, MEC36, MEC21, MEC28, and MEC39.

Model	Common
MEC37	MEC37(2)18-10 COMMON
MEC33	MEC33(2)18-10 COMMON
MEC36	MEC36(2)18-10 COMMON
MEC21	MEC21(2)18-10 COMMON
MEC28	MEC28(2)18-10 COMMON
MEC39	MEC39(2)18-10 COMMON



BOARD STIFFENER

in compressed mounting plate

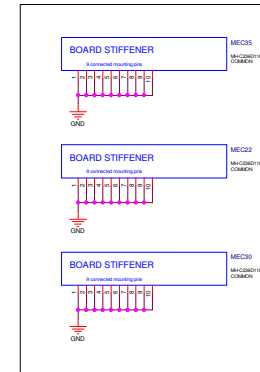
1 2 3 4 5 6 7 8

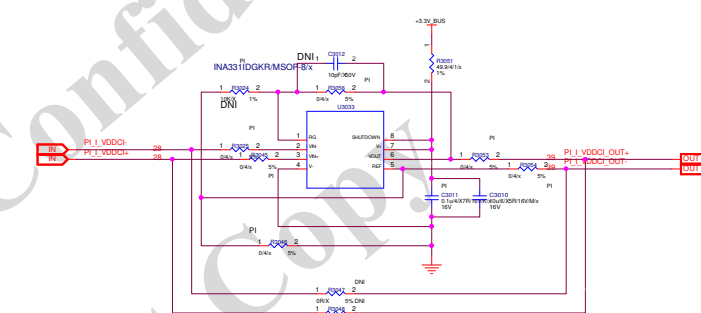
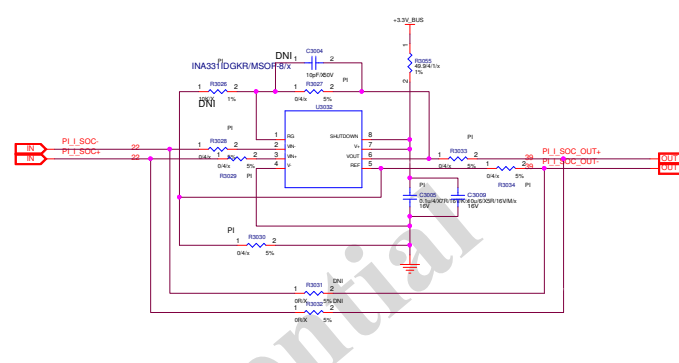
GND GND

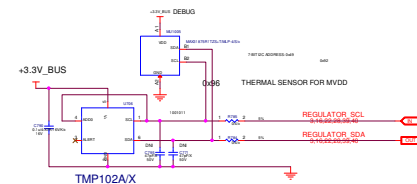
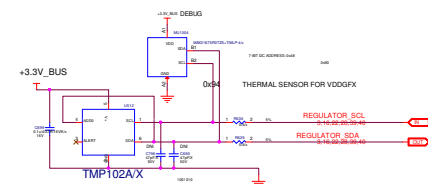
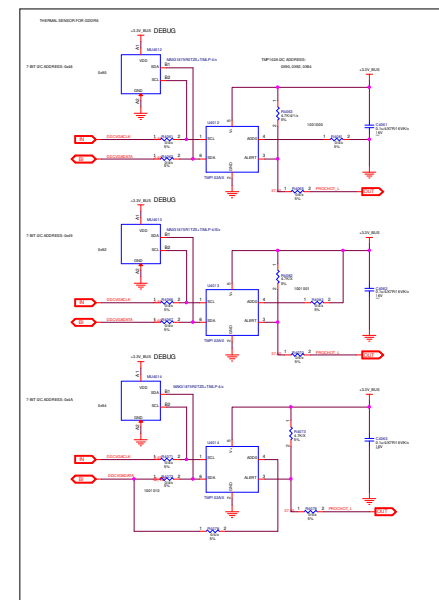
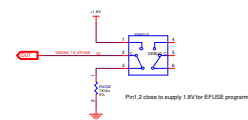
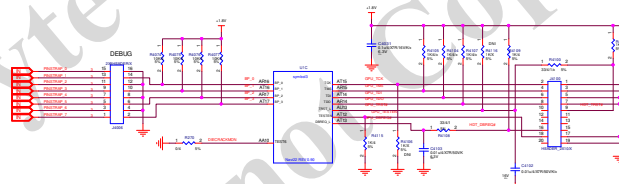
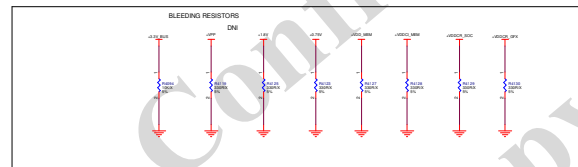
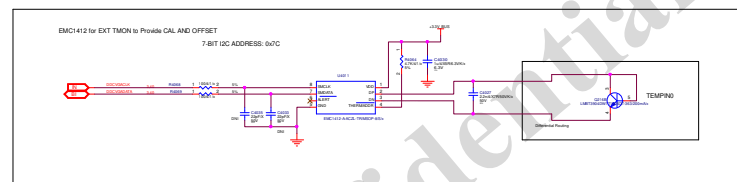
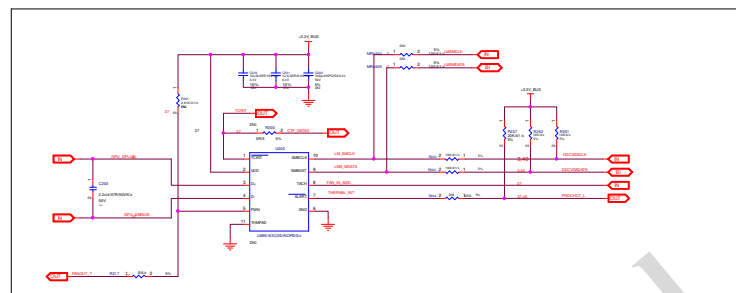
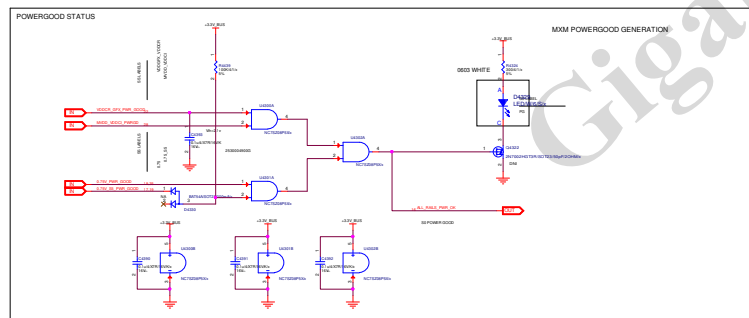
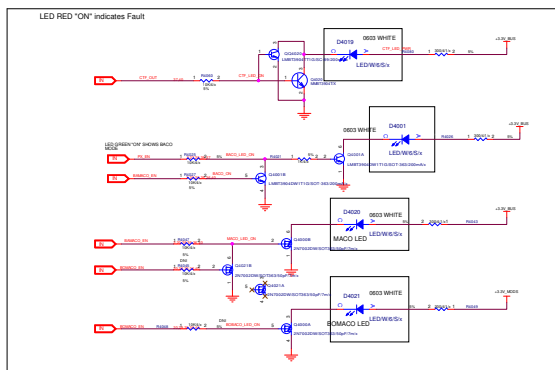
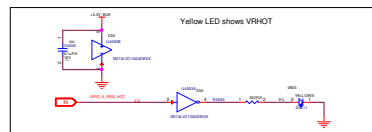
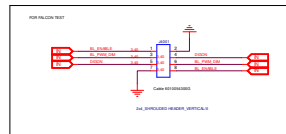
The diagrams illustrate common board stiffener mounting patterns for three different modules:

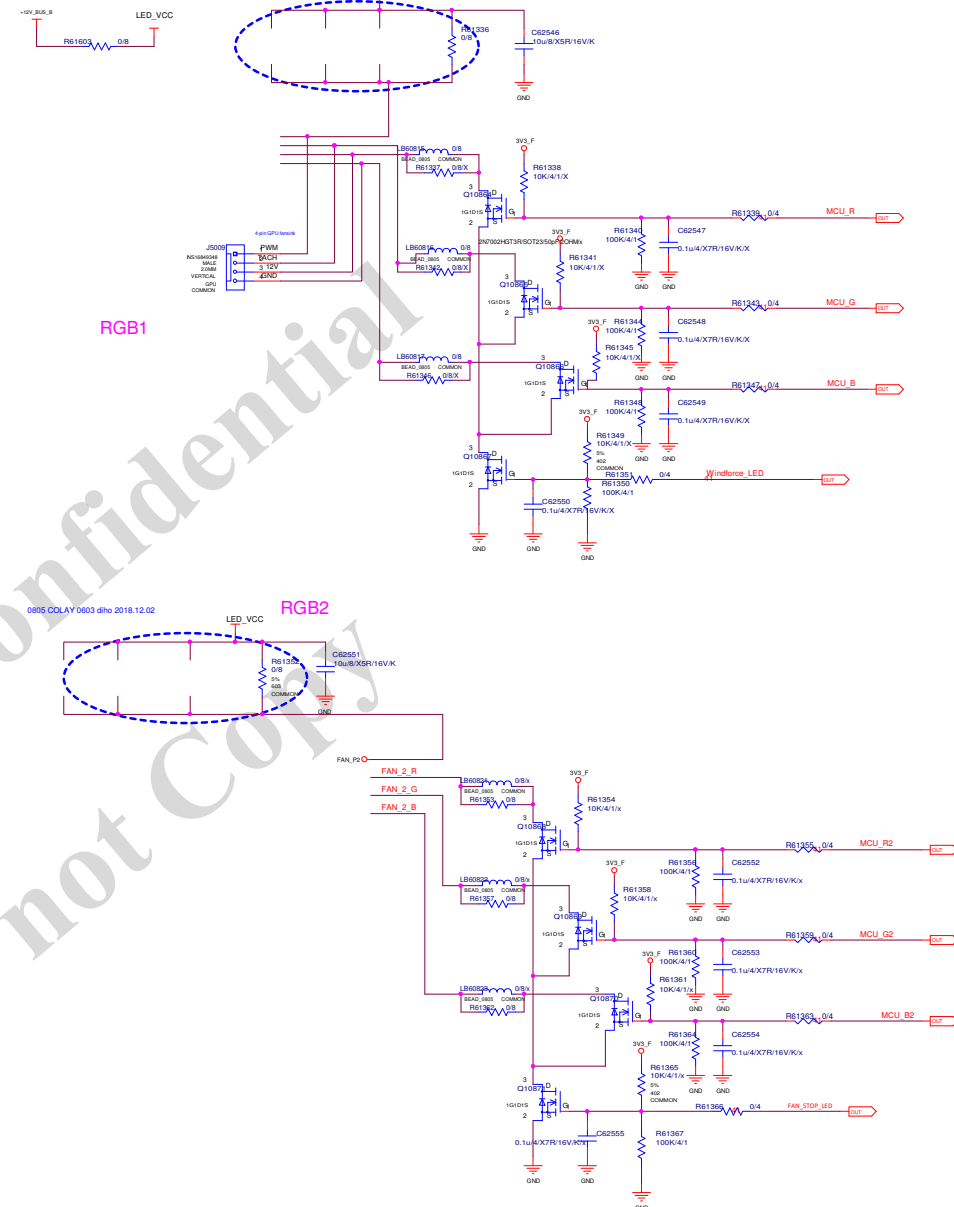
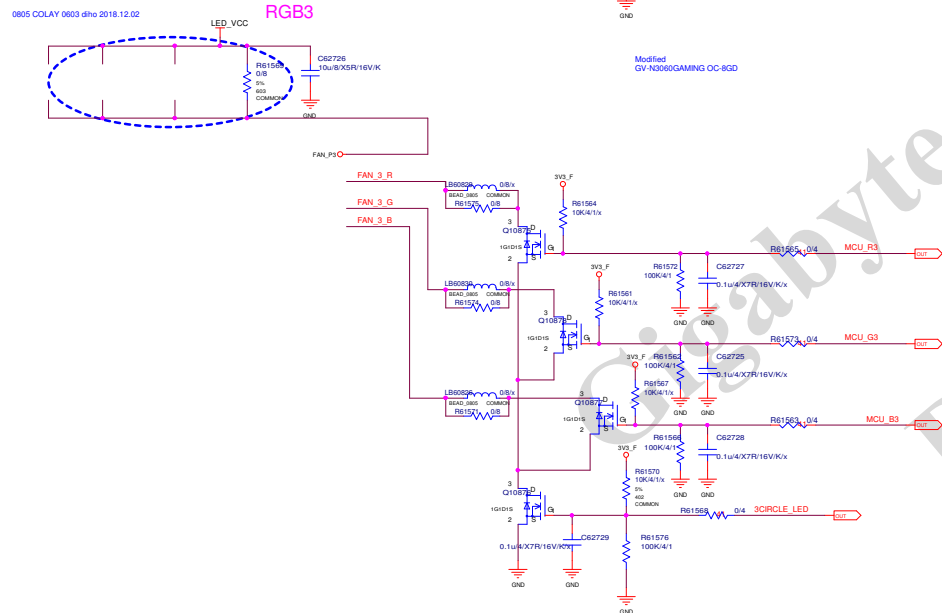
- MC17:** Board stiffener mounting pattern. The connector has 10 pins. Pins 1 through 9 are connected to a common ground (GND), and pin 10 is connected to a common signal line (COMMON).
- MC18:** Board stiffener mounting pattern. The connector has 10 pins. Pins 1 through 9 are connected to a common ground (GND), and pin 10 is connected to a common signal line (COMMON).
- MC31:** Board stiffener mounting pattern. The connector has 10 pins. Pins 1 through 9 are connected to a common ground (GND), and pin 10 is connected to a common signal line (COMMON).

MOS SINK









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