

PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI
Tall DVI-I + DP + DP + DP/HDMI + DP

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V320-2.0 change item:

- Page15:DVI add esd
- Page18:remove DP colay
- Page20:HDMI add esd
- Page21:4pin housing colay 6pin housing
- Page25:NVVDD enable phase4
- Page27:Add phase4
- Page29:remove colay NVVDD power solution
- Page30: 12V input bead change to choke
6pin power con colay 8pin con
remove 0603 MLCC colay
- Page32:stuff logo LED

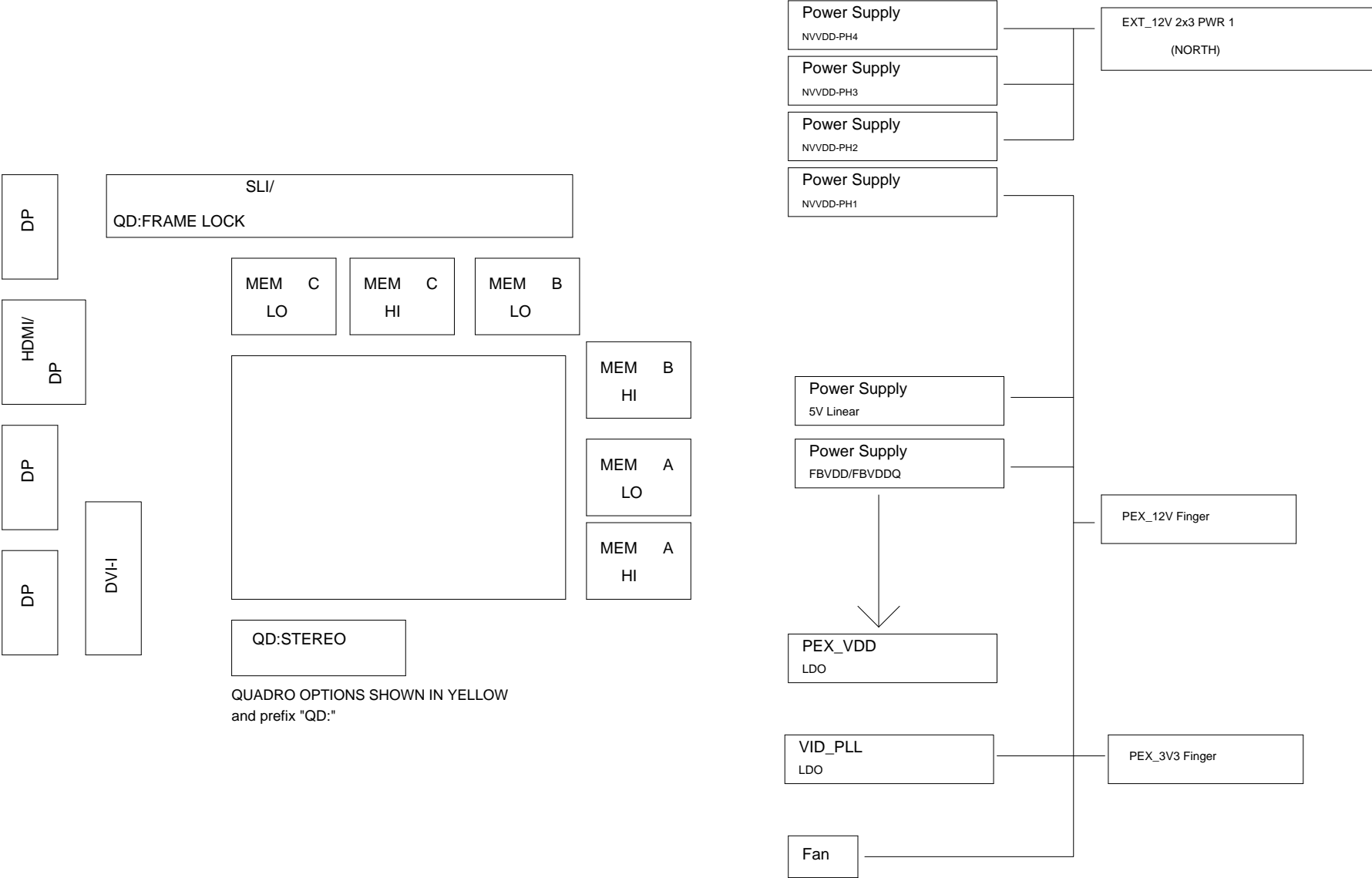
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MS-V320

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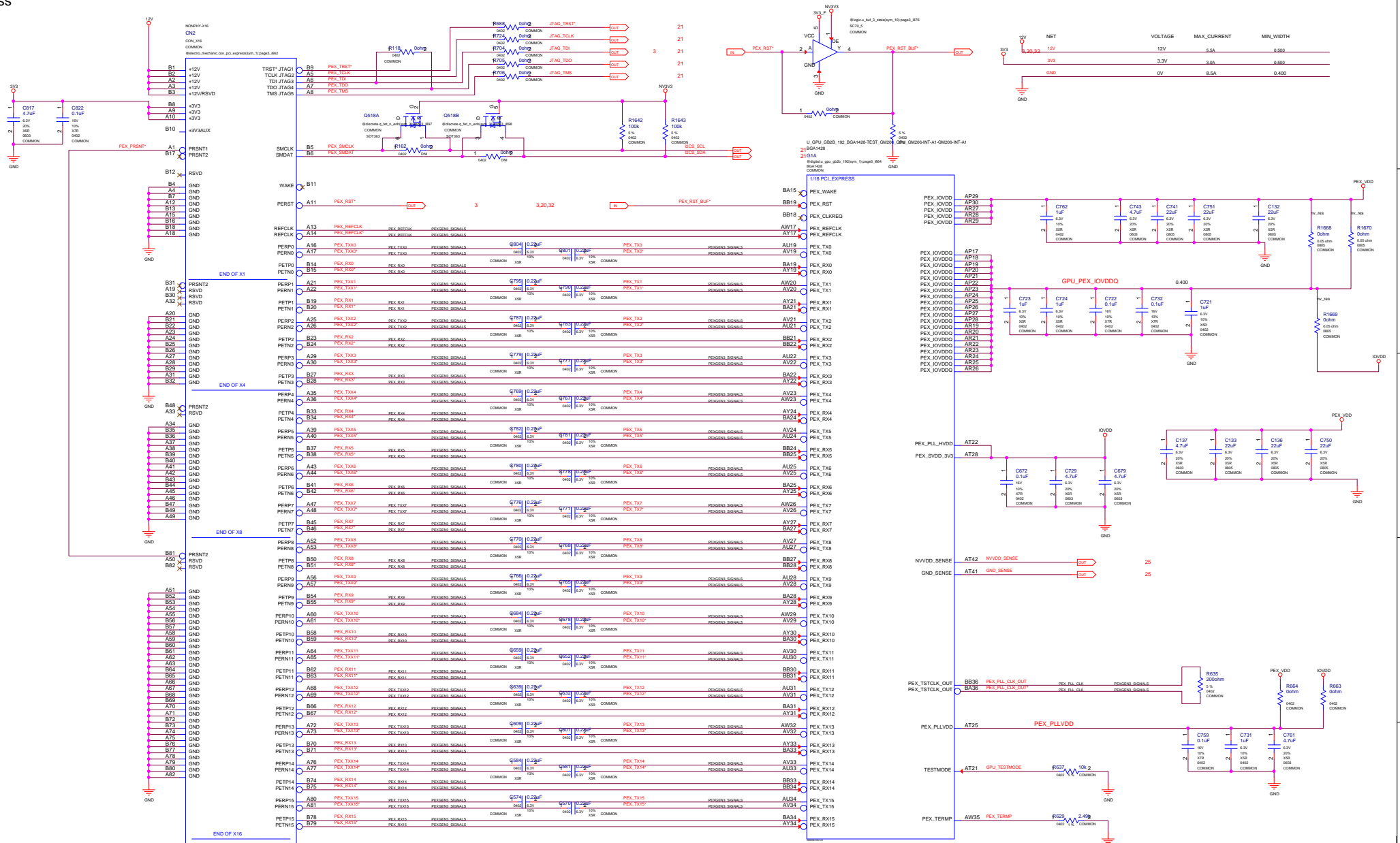
Block Diagram



QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

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PCI Express



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 Bga1426 - gpu_g82b_192pin_3 page 4 / 1905
 BGA1426

218 FBA

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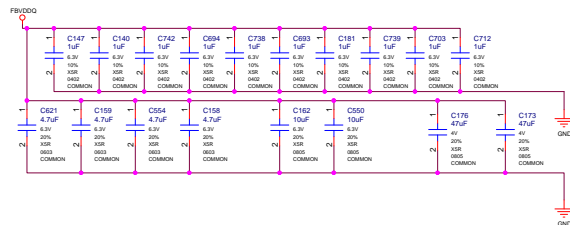
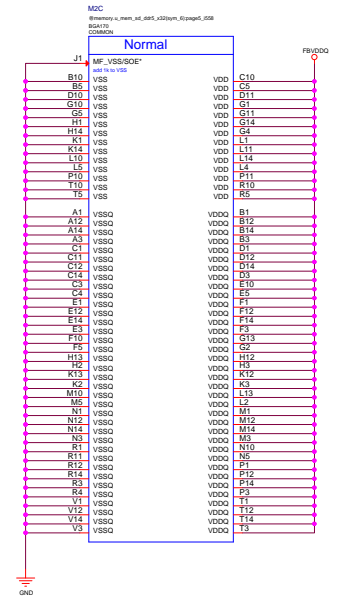
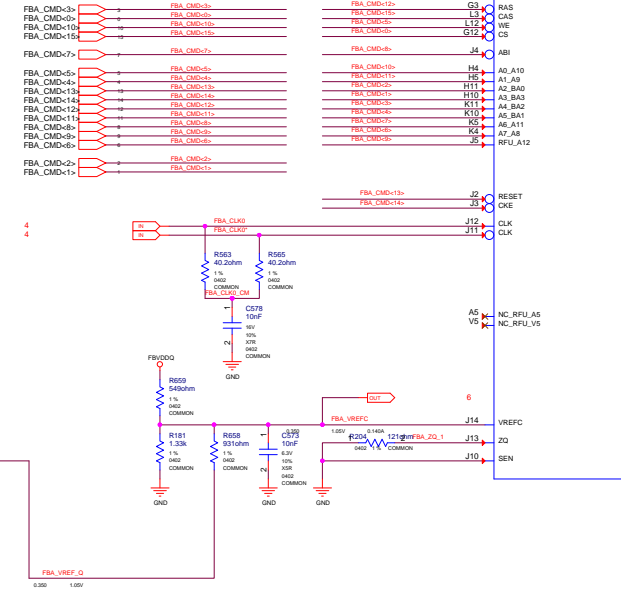
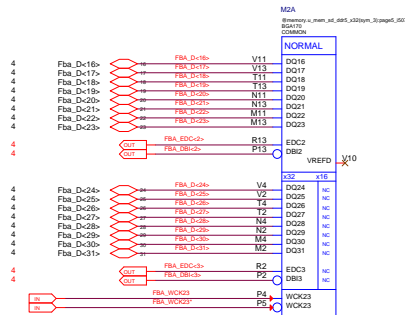
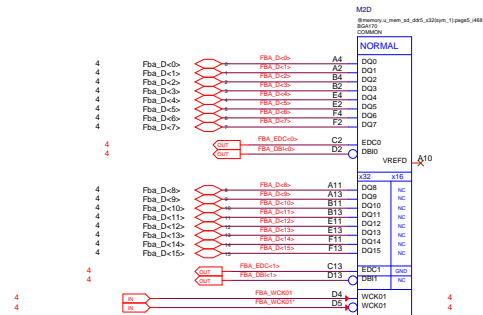
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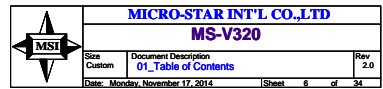
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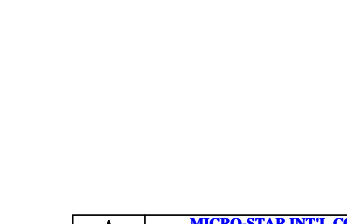
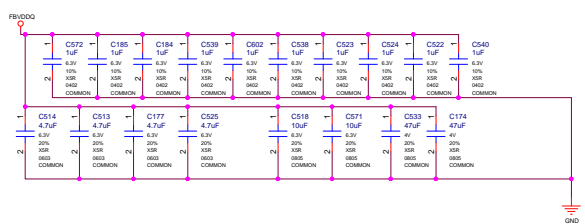
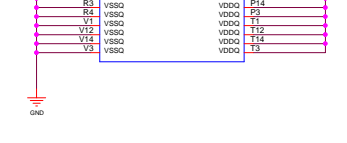
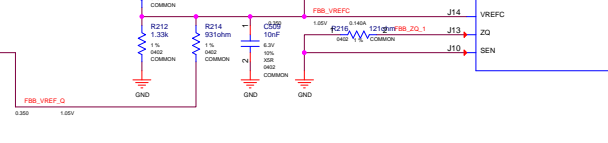
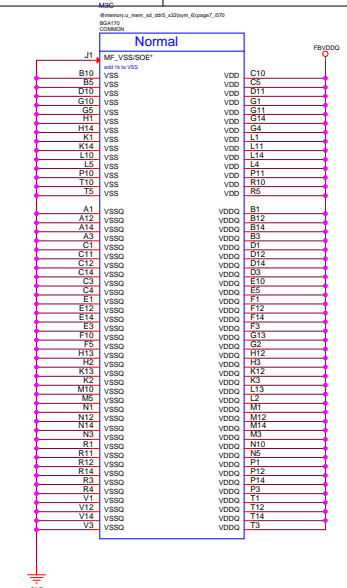
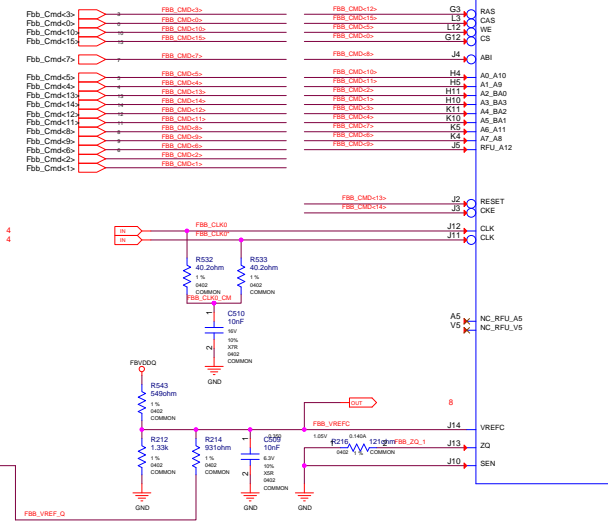
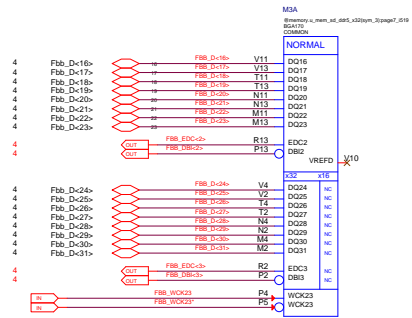
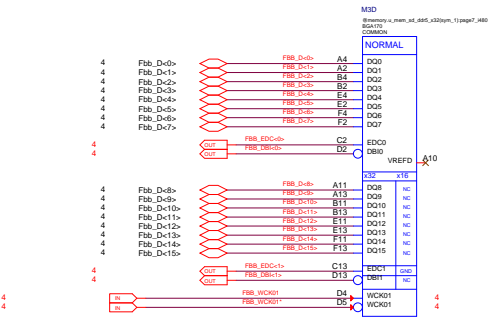
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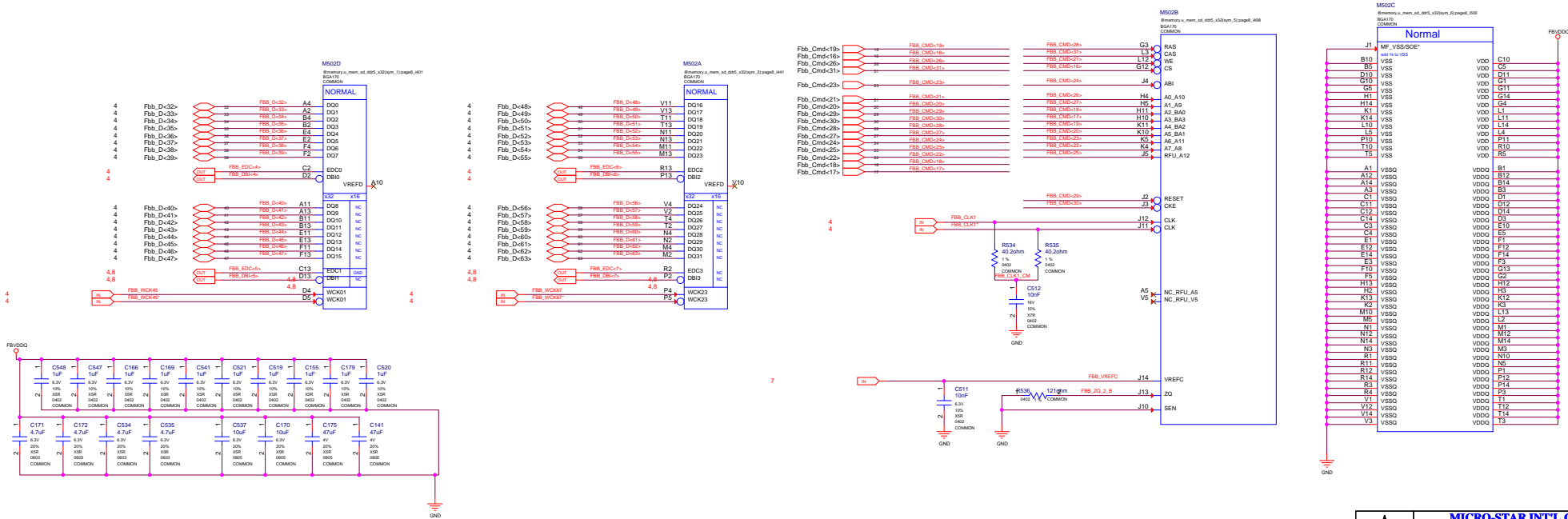
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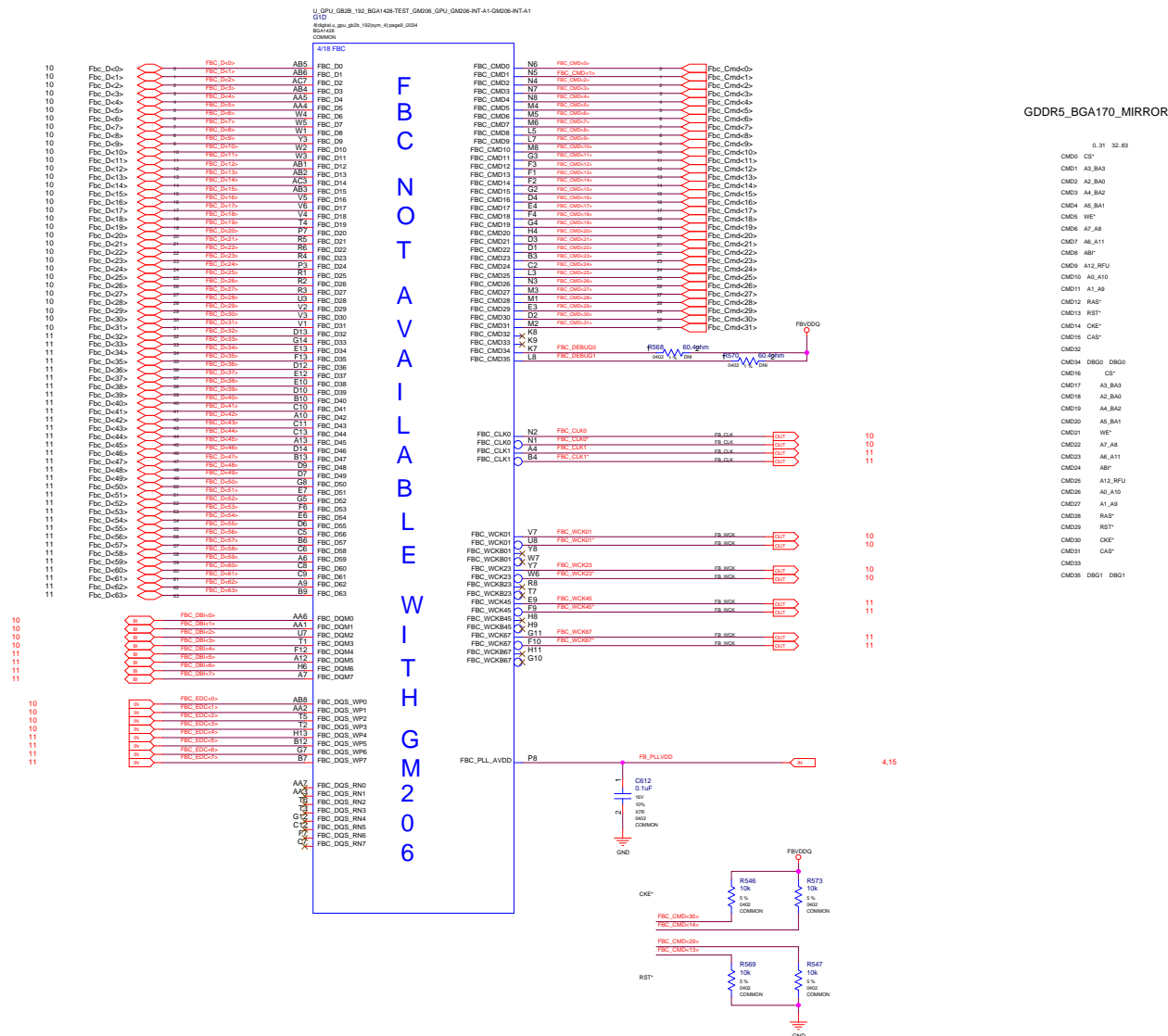


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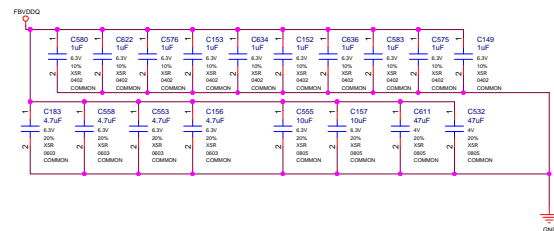
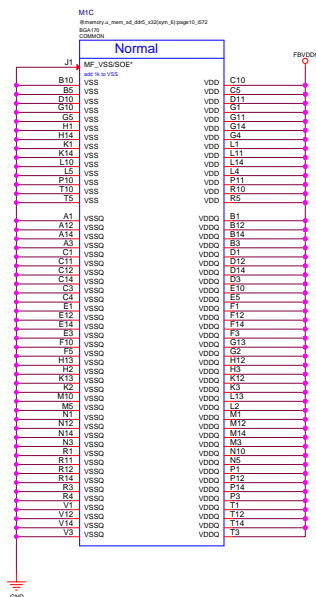
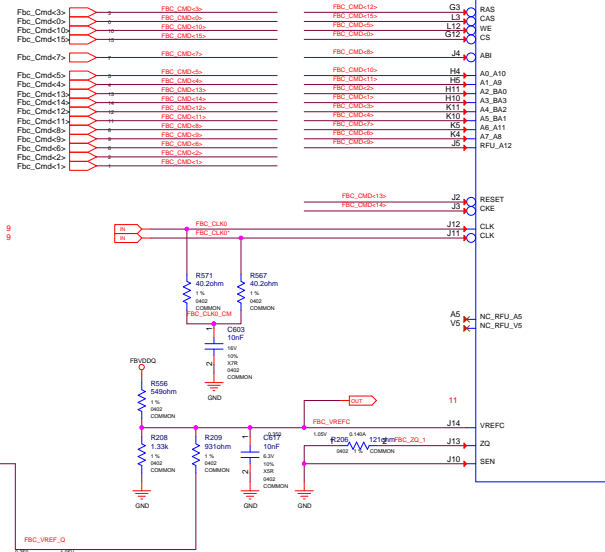
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CMD4	A5_BA1
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CMD7	A6_A11
CMD8	AB1*
CMD9	A12_RFU
CMD10	A2_A10
CMD11	A1_A9
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CMD13	RST*
CMD14	CKE*
CMD15	CAS*
CMD32	
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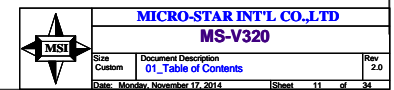
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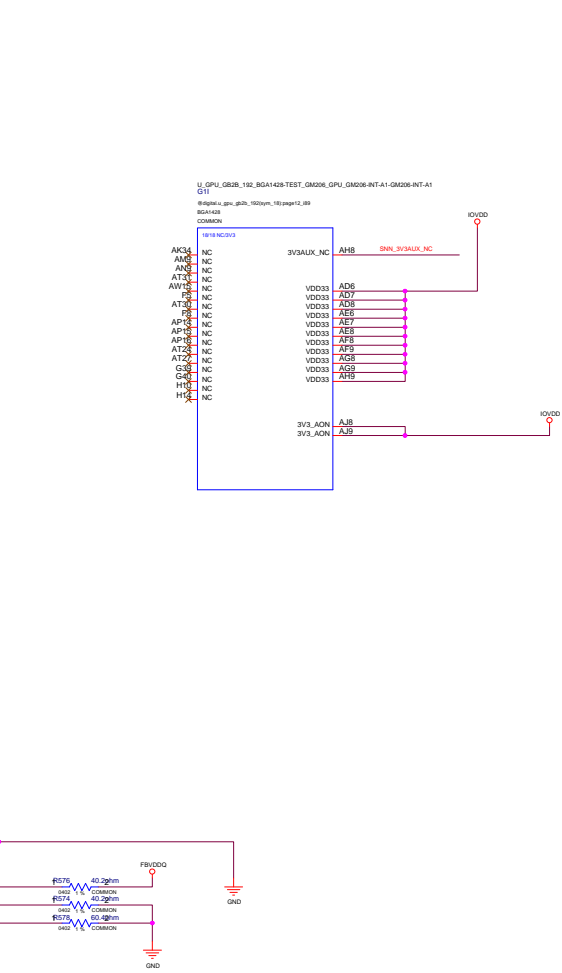
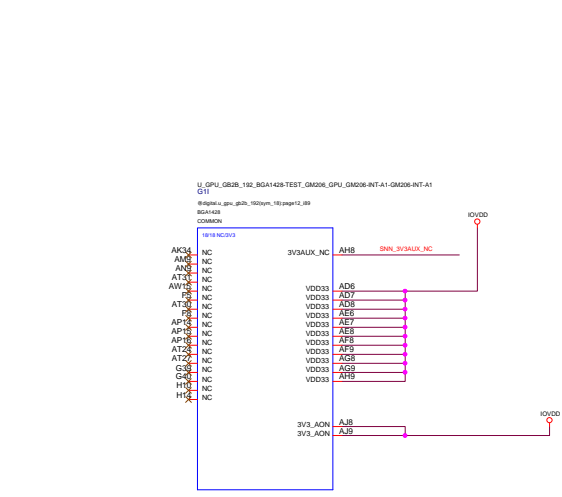
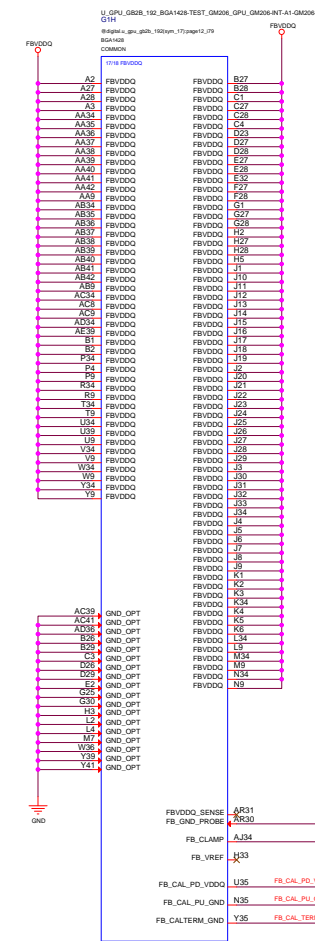
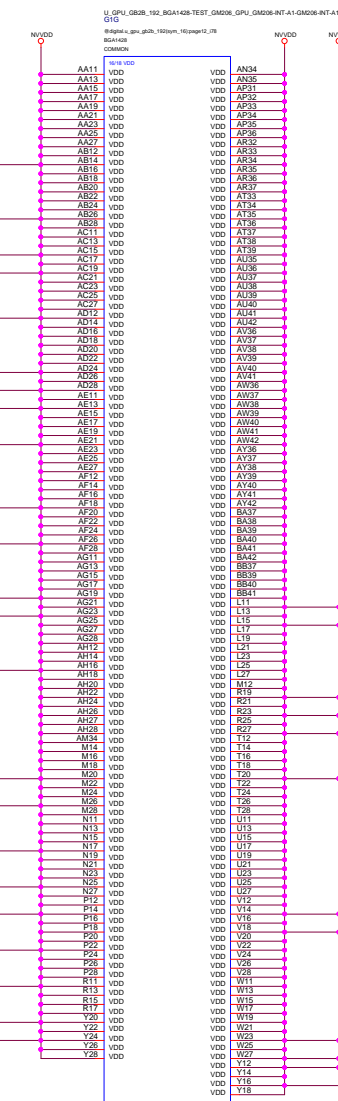
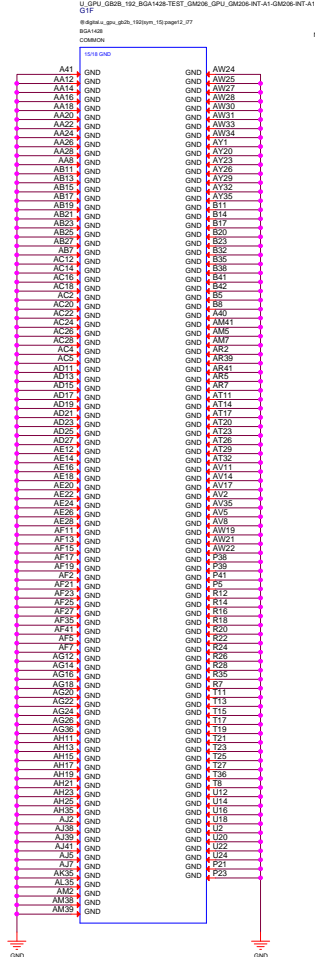
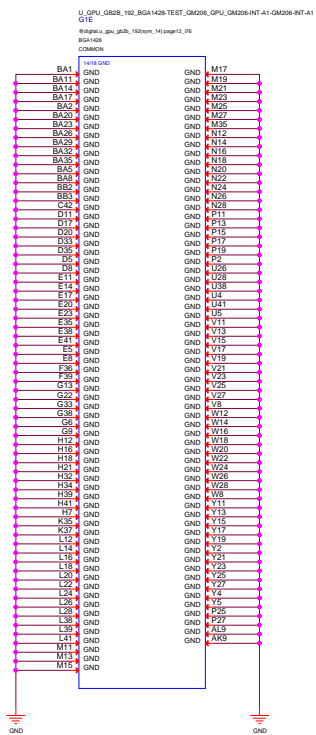
MEMORY: FBC Partition 31..0



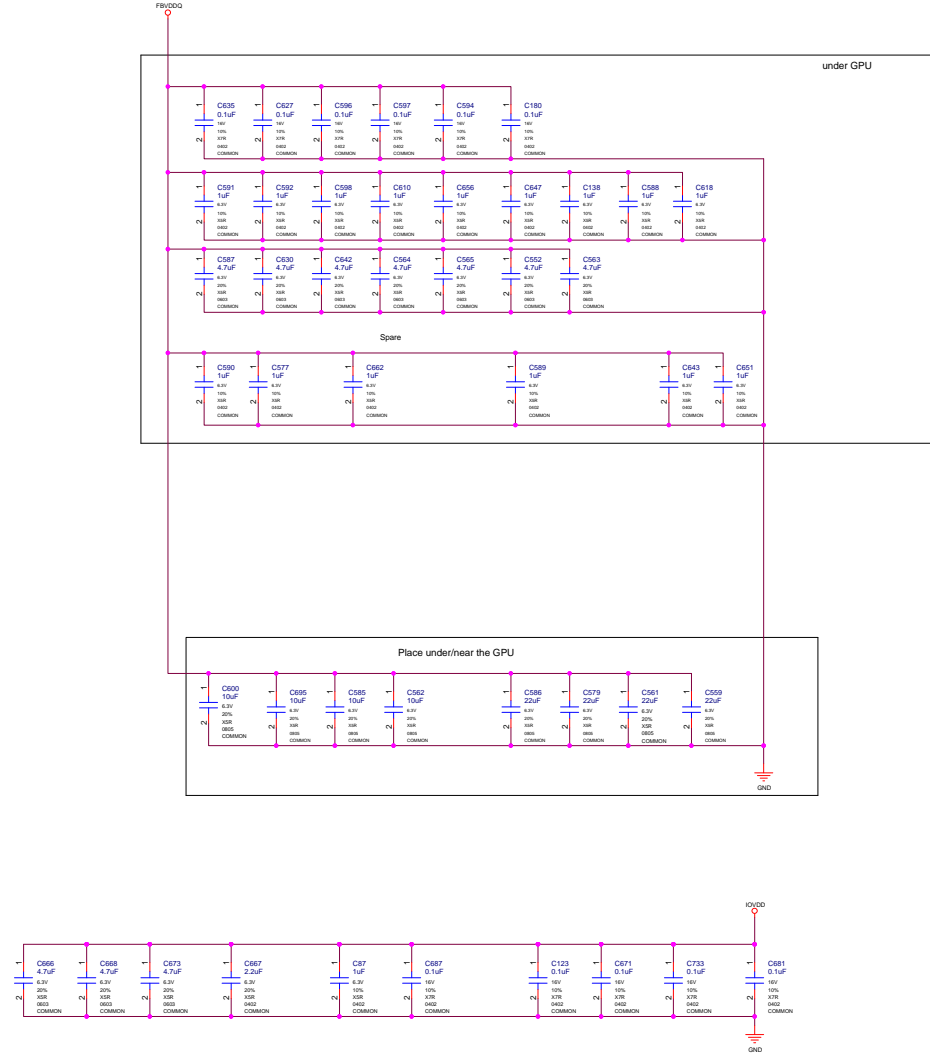
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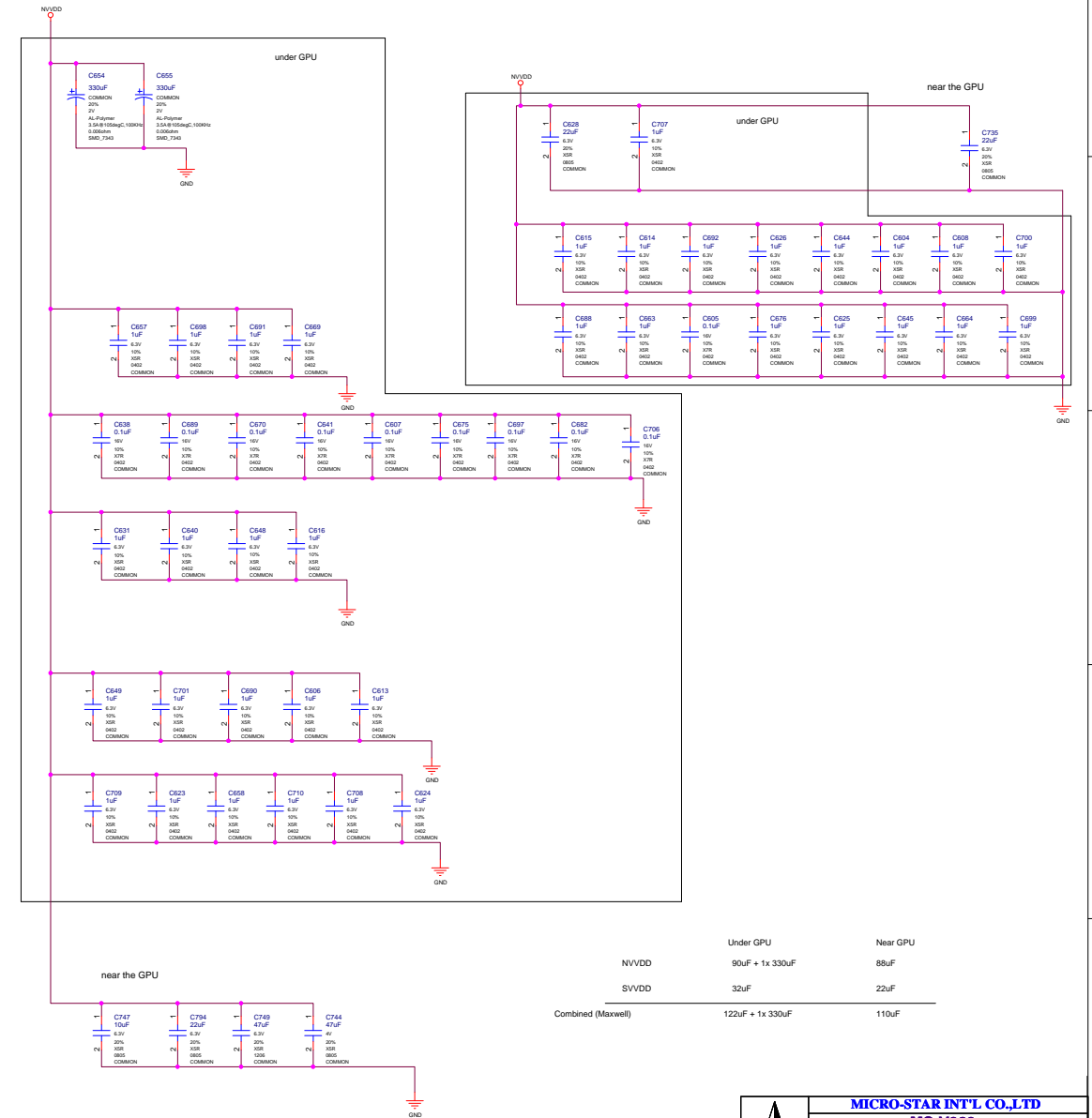
GPU PWR and GND



GPU Decoupling



NVVDD



	Under GPU	Near GPU
NVDD	90uF + 1x 330uF	88uF
SVDD	32uF	22uF
Combined (Maxwell)	122uF + 1x 330uF	110uF



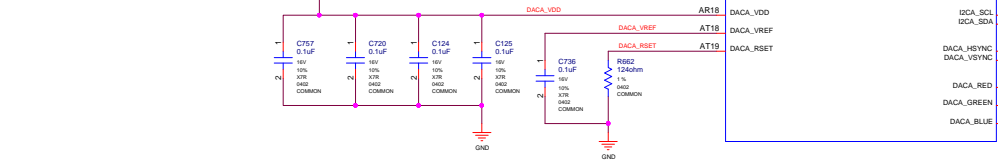
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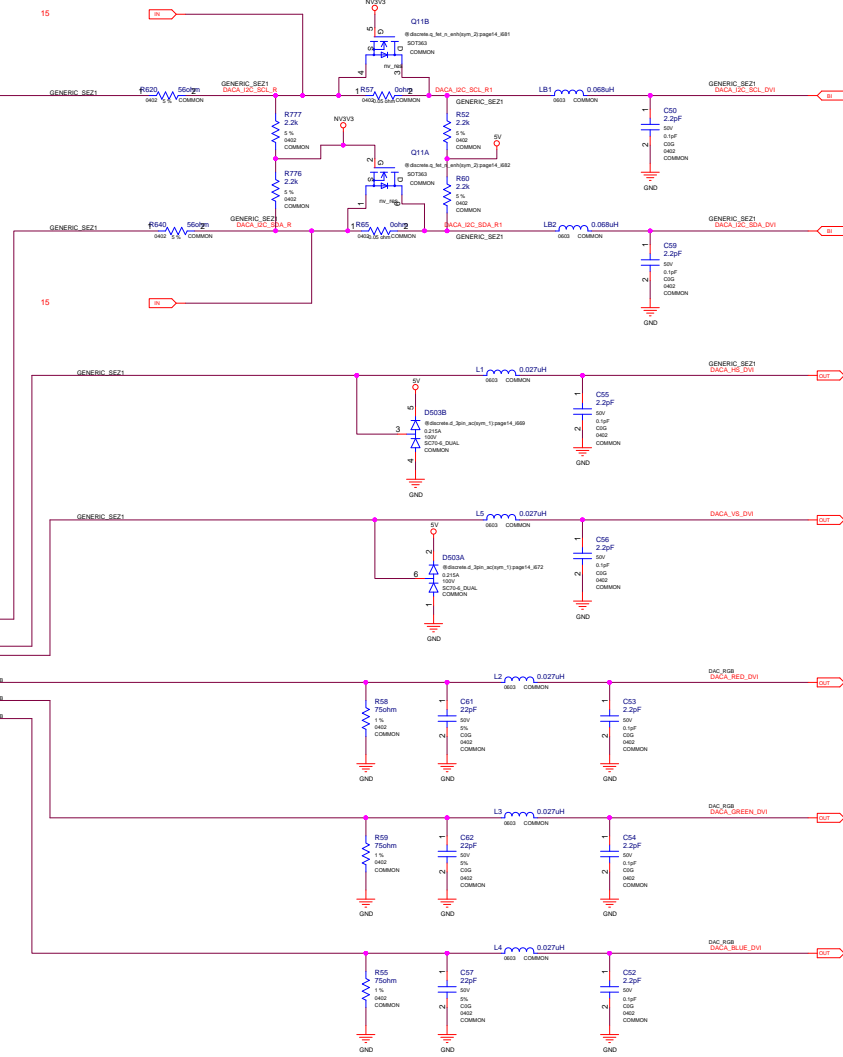
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DACA Interface

15,16,18,19



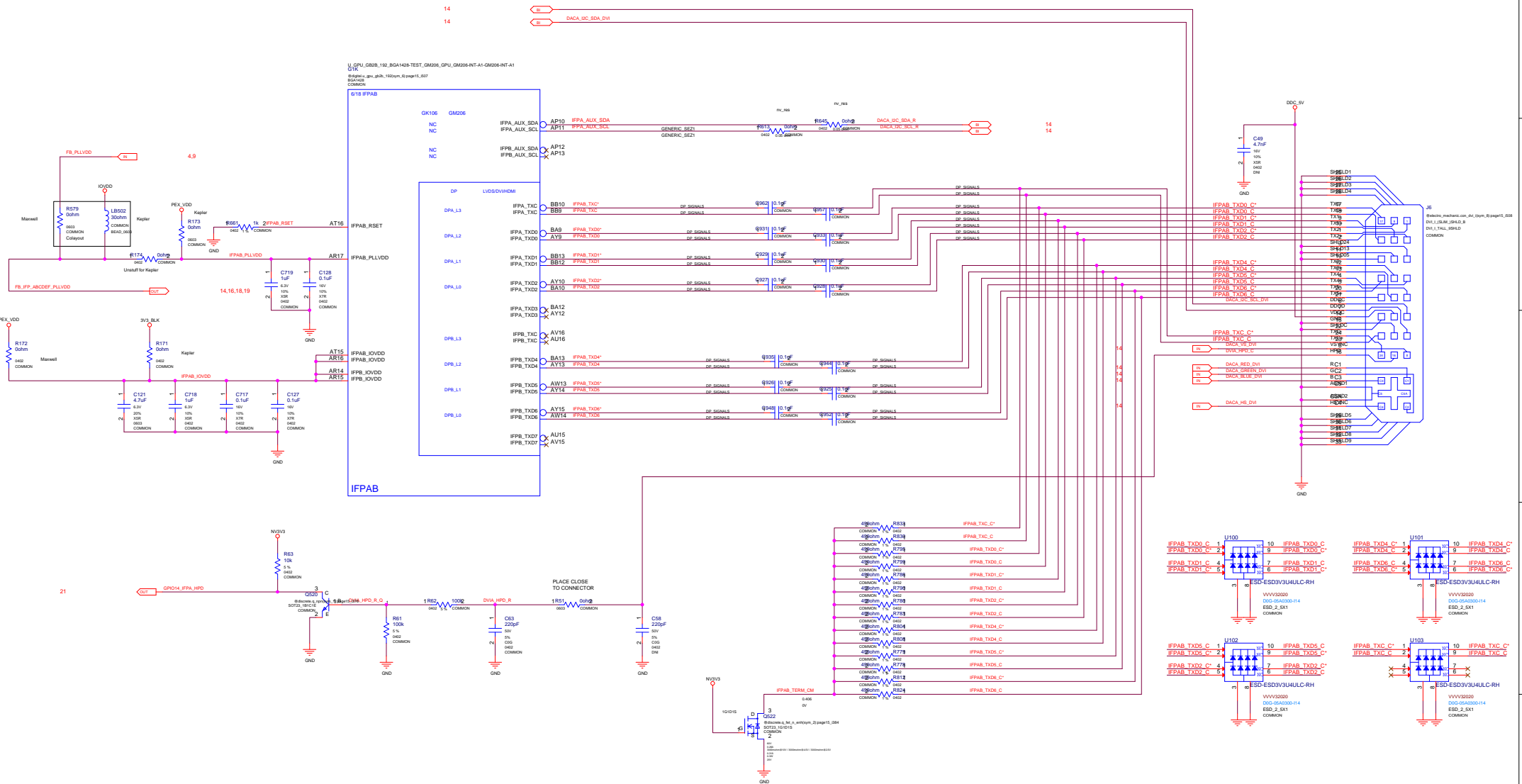
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DACA_SDA	AY5	DACA_DC_SDA
DACA_HEYNC	AU8	DACA_HEYNC
DACA_VSYNC	AY8	DACA_VSYNC
DACA_RED	BB16	DACA_RED
DACA_GREEN	BA16	DACA_GREEN
DACA_BLUE	BB15	DACA_BLUE



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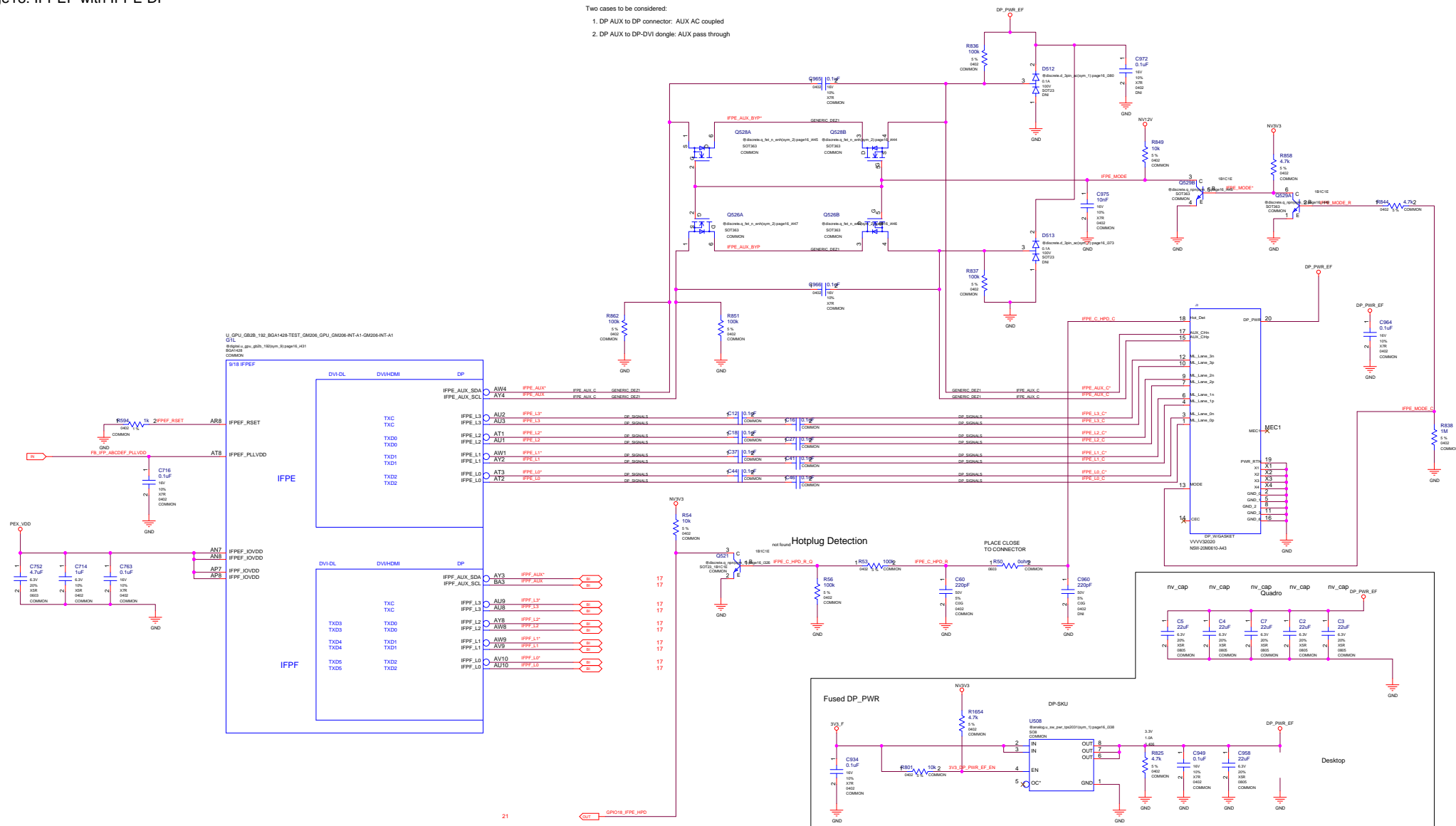
IFPAB DVI-I-DL



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Two cases to be considered:

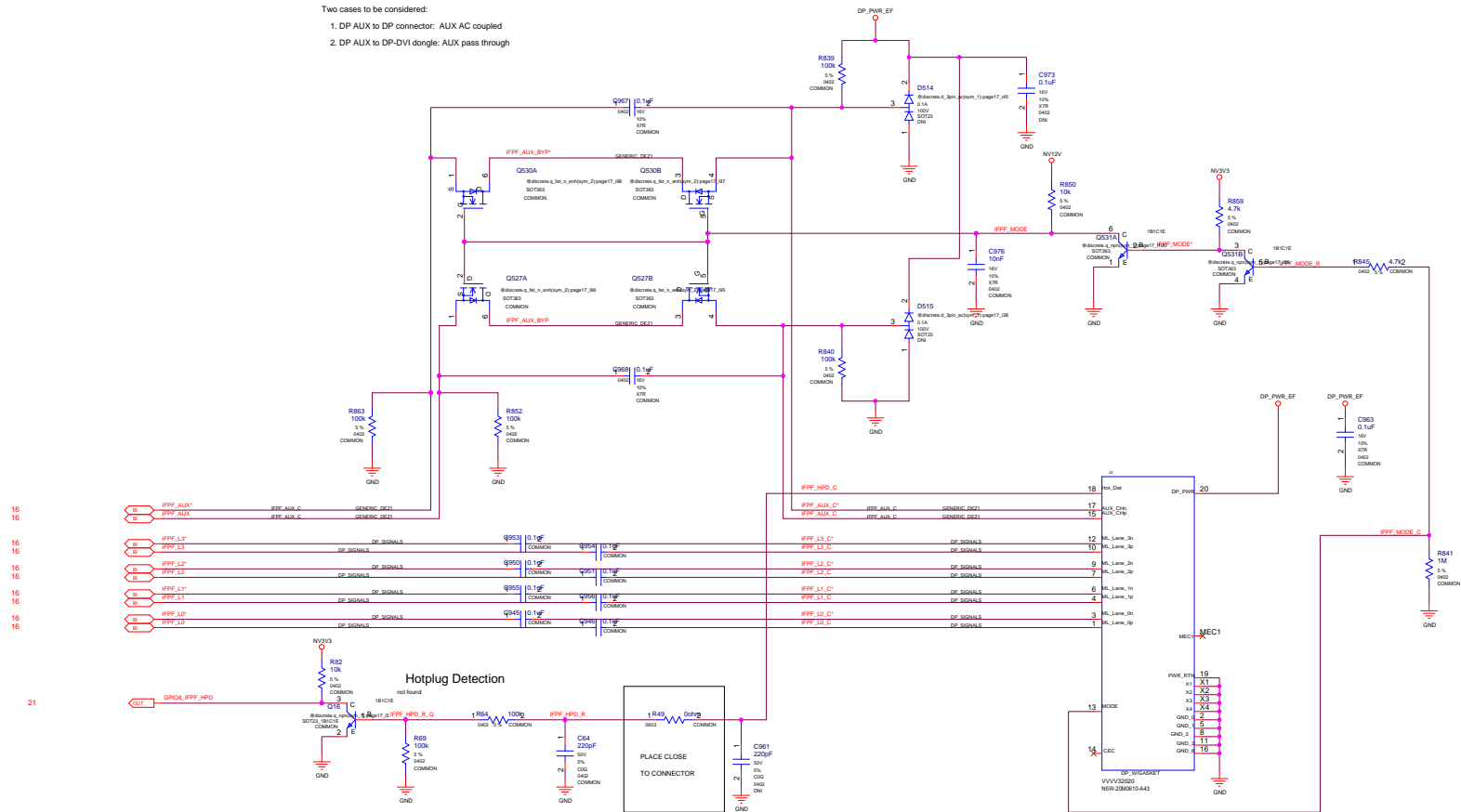
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



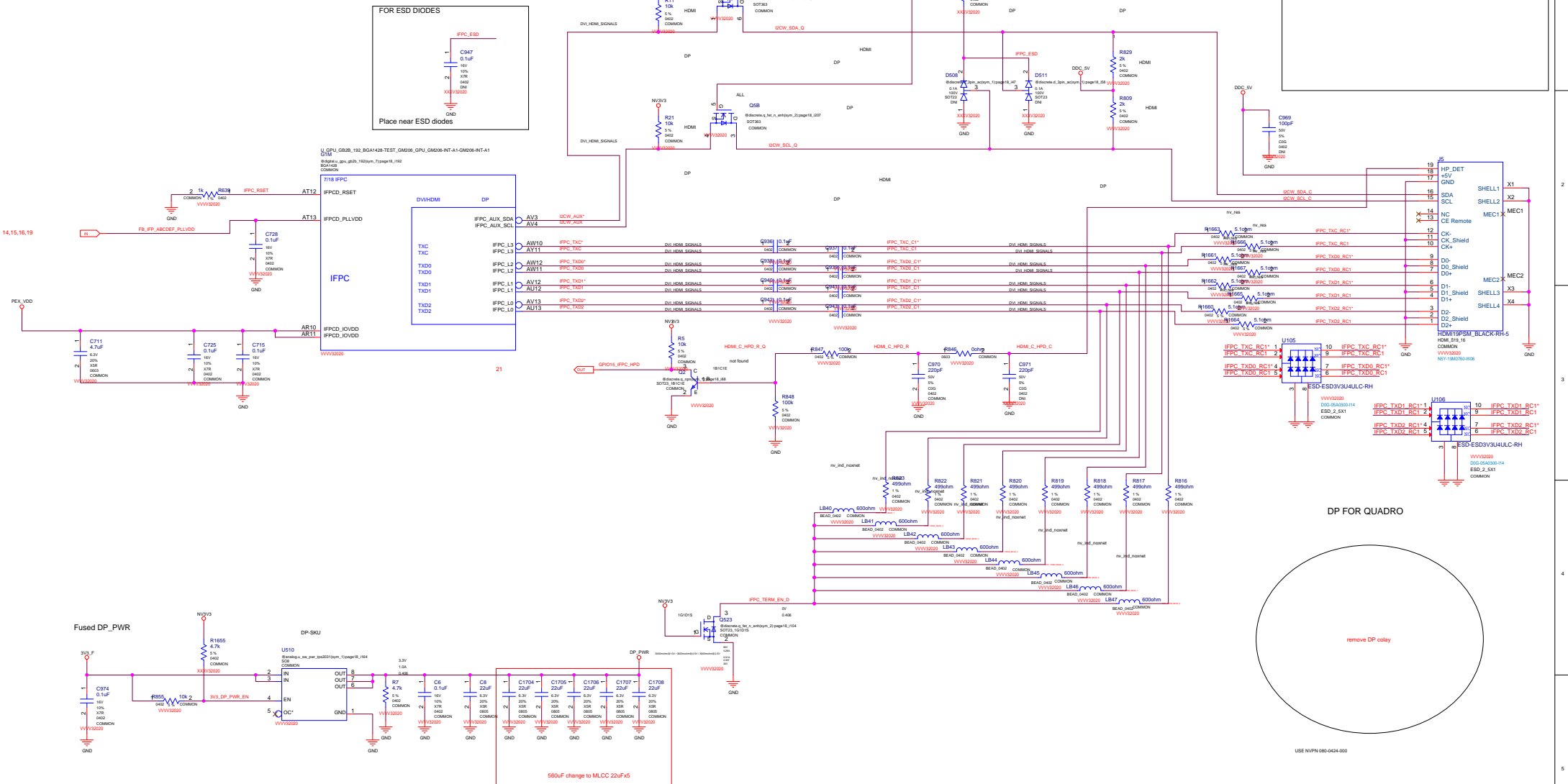
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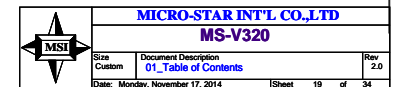
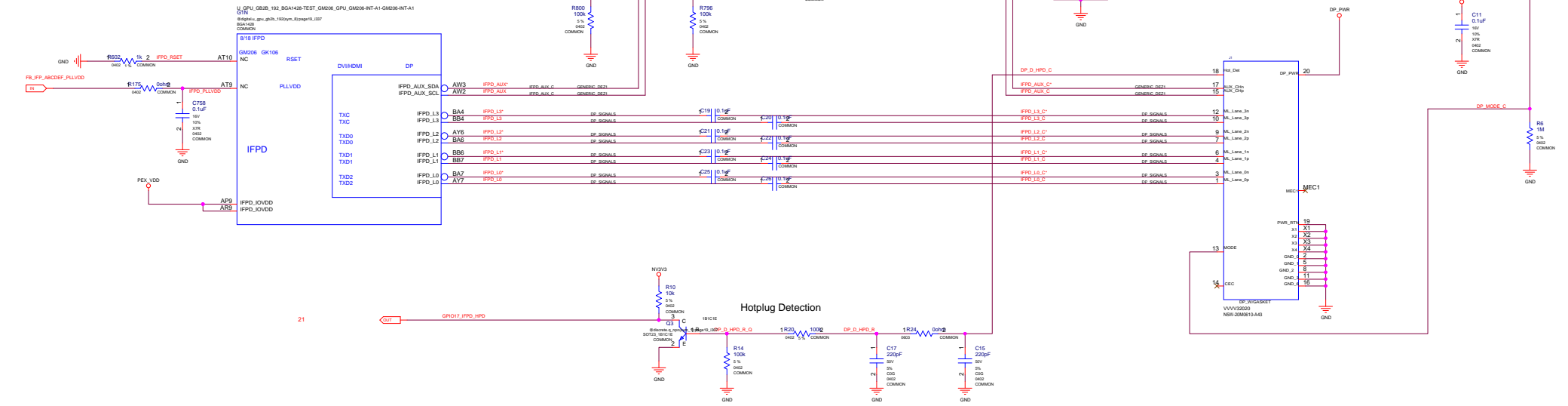
Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

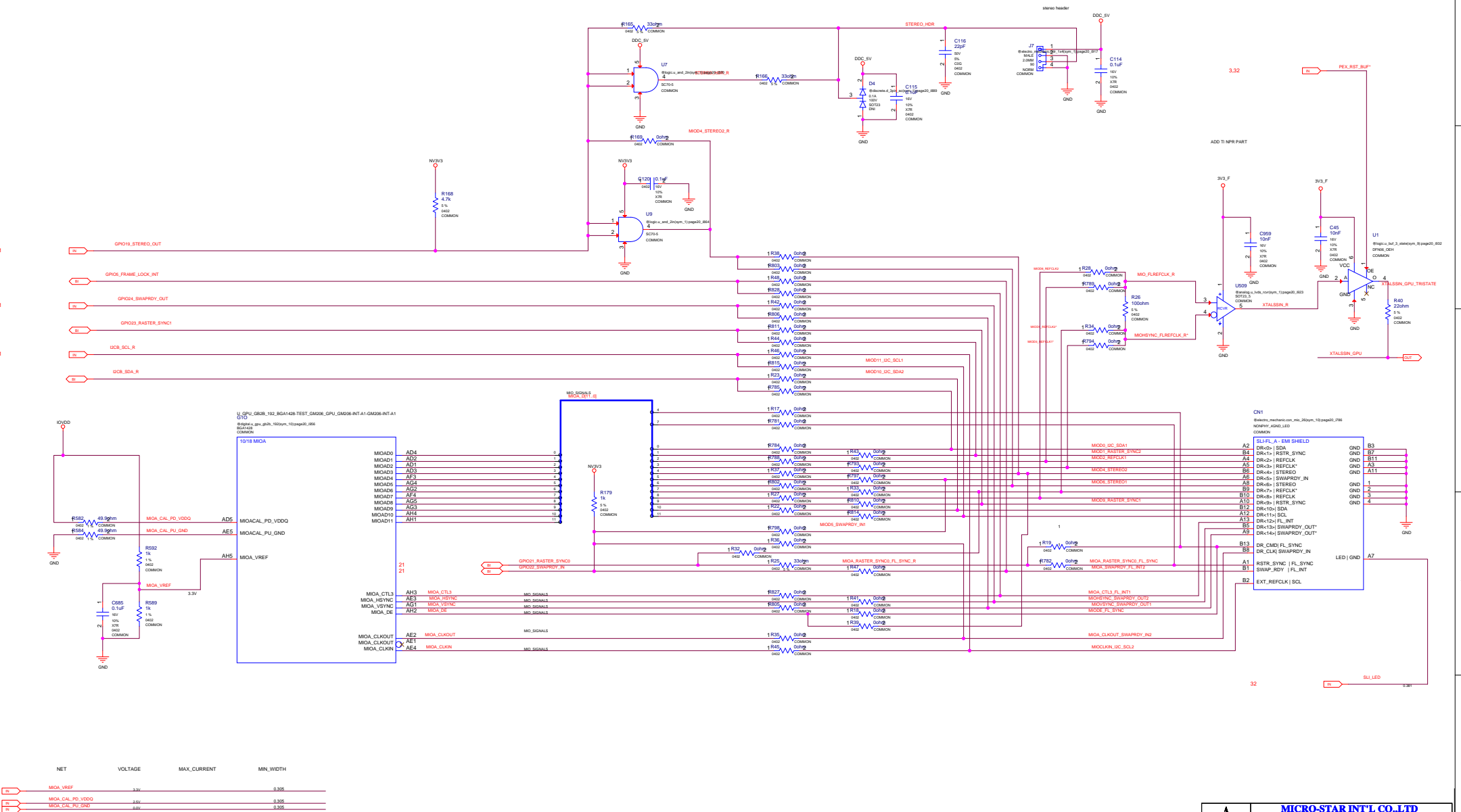


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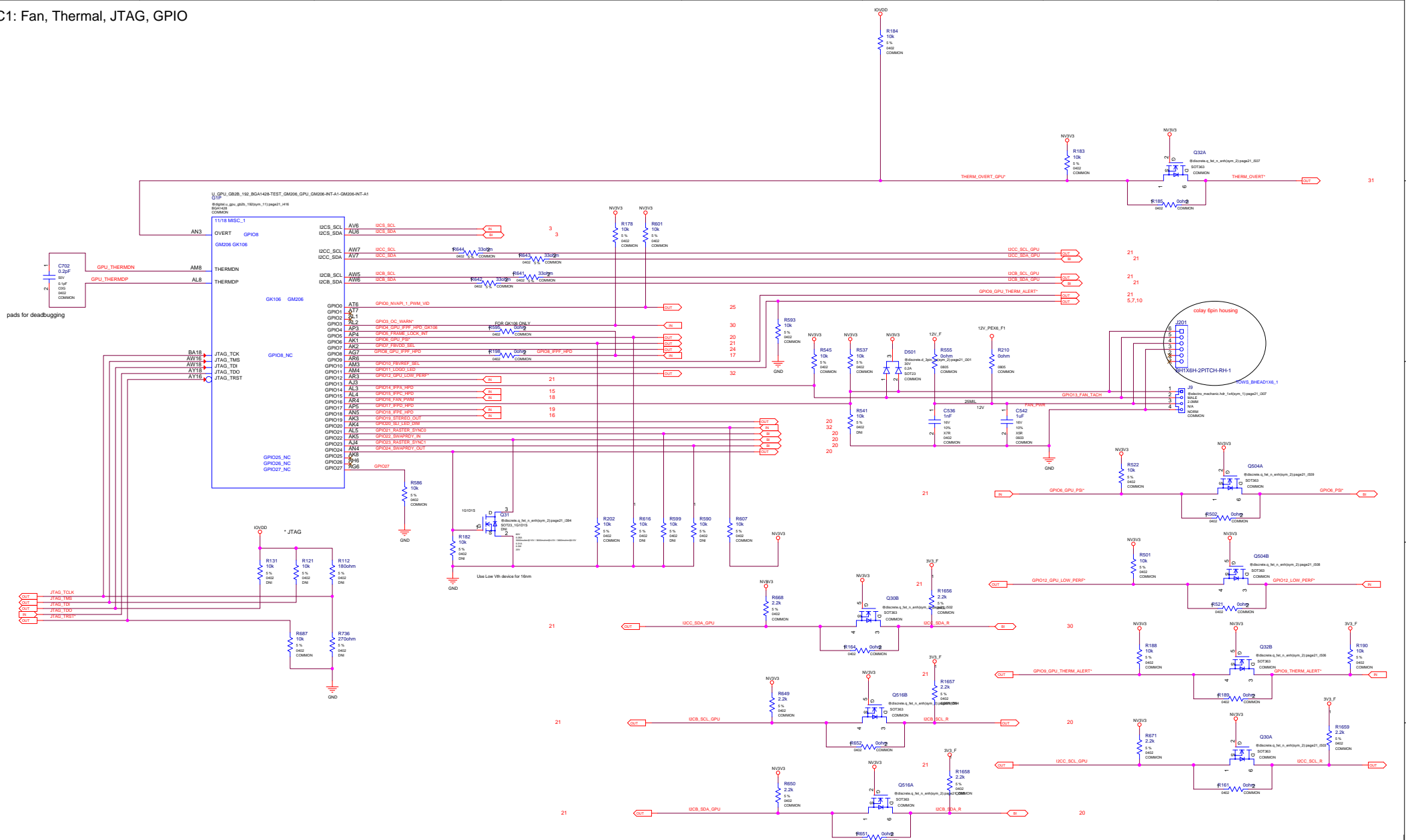


MIOA/SLI Interface



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MISC1: Fan, Thermal, JTAG, GPIO



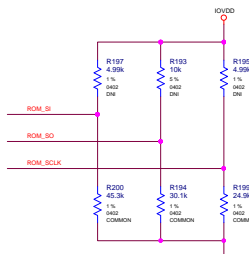
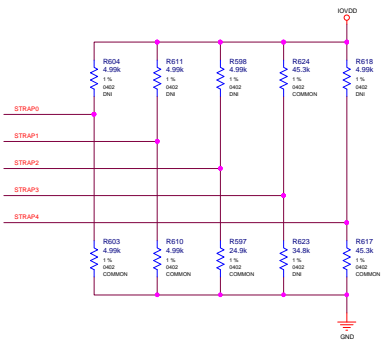
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MISC2: ROM, XTAL, Straps

	KEPLER	MAXWELL
STRAP0	USER_BIT [3:0]*	
STRAP1	3GIO_PADCFG_LUT_ADR*	
STRAP2	PCI_DEVID [3:0]*	
STRAP3	SOR_EXPOSED [3:0]*	
STRAP4	DP_PLL_VDD_33V*	
	PEX_MAX_SPEED*	
	PEX_SPD_CHANGE_GEN3*	
	*	
ROM_SI	RAMCFG[0]*	RAMCFG[0]*
	RAMCFG[1]*	RAMCFG[1]*
	RAMCFG[2]*	RAMCFG[2]*
	RAMCFG[3]*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	VGA_DEVICE*
	SMB_ALT_ADDR*	SMB_ALT_ADDR*
	FB[0]_APERTURE_SIZE*	PCIE_CFG*
	FB[1]_APERTURE_SIZE*	DEVID_SEL*
ROM_SCLK	PEX_PLL_EN_TERM100*	SOR0_EXPOSED*
	PCI_DEVID_EXT[5]*	SOR1_EXPOSED*
	SUB_VENDOR*	SOR2_EXPOSED*
	PCI_DEVID_EXT[4]*	SOR3_EXPOSED*

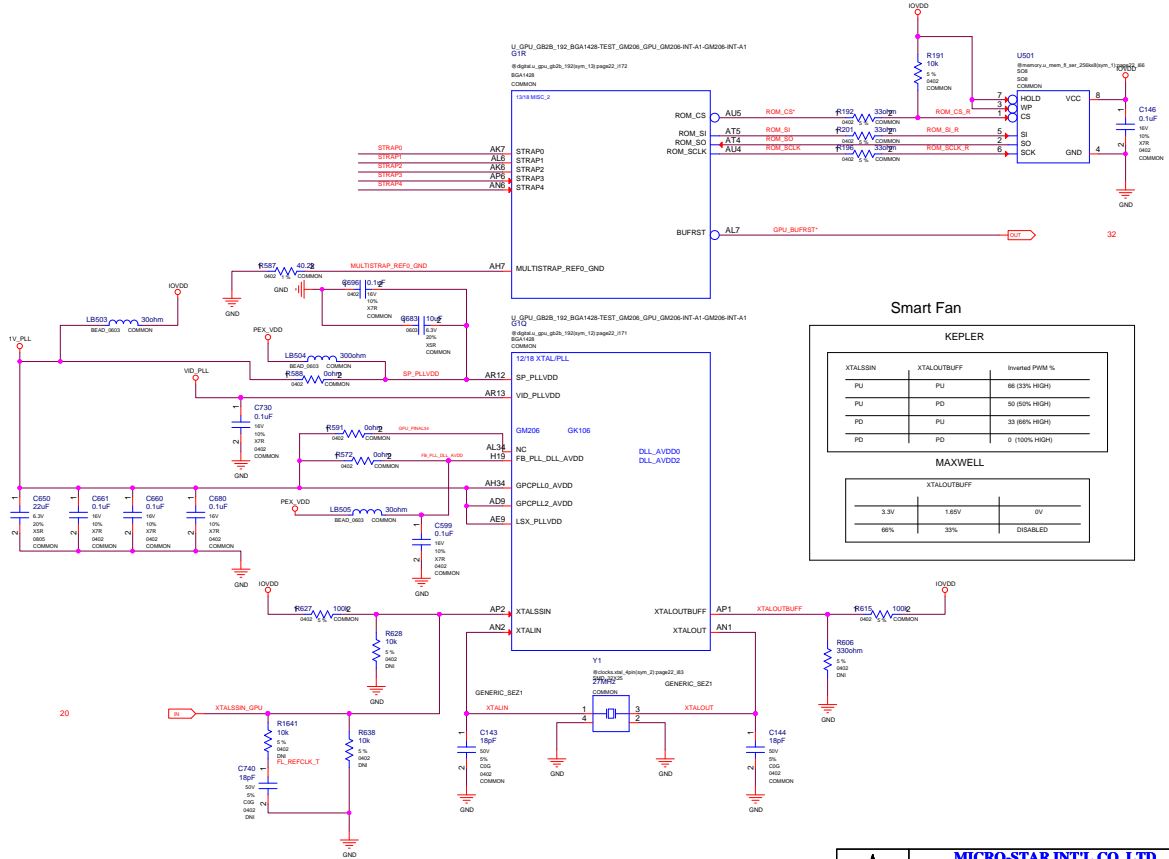
MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% to GND

MAXWELL		
3.3V	1.65V	0V
G06+ISLAND ENABLED	G06+ DEBUG MODE	G06+ ISLAND DISABLED



ROM_SI		
SAMSUNG	HYNIX	ELPIDA
45.3k	PD	30.1k PD

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111



Smart Fan		
KEPLER		
XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PD	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)
MAXWELL		
XTALOUTBUFF		
3.3V	1.65V	0V
66%	33%	DISABLED

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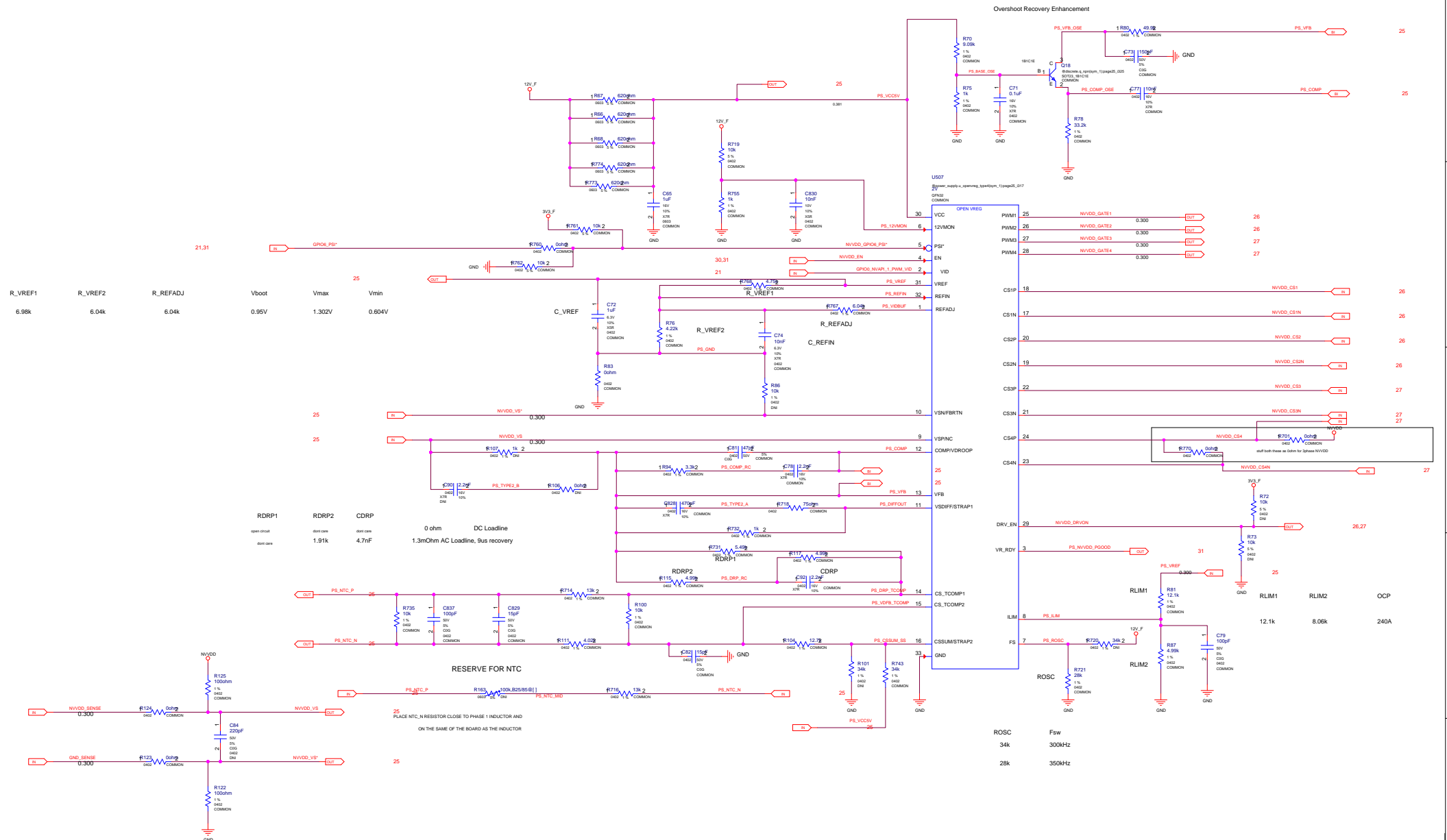
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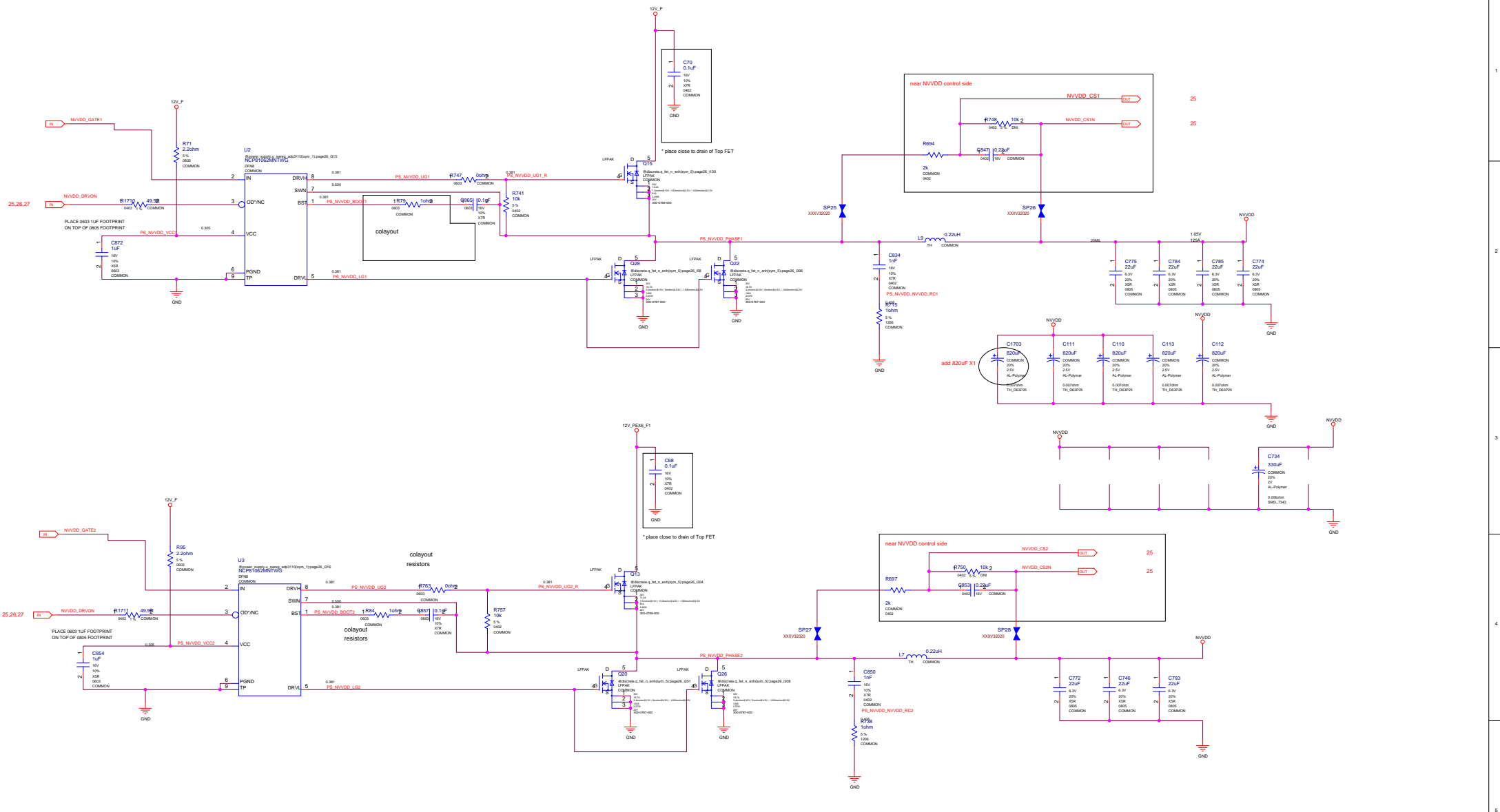
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PS: NVVDD Controller



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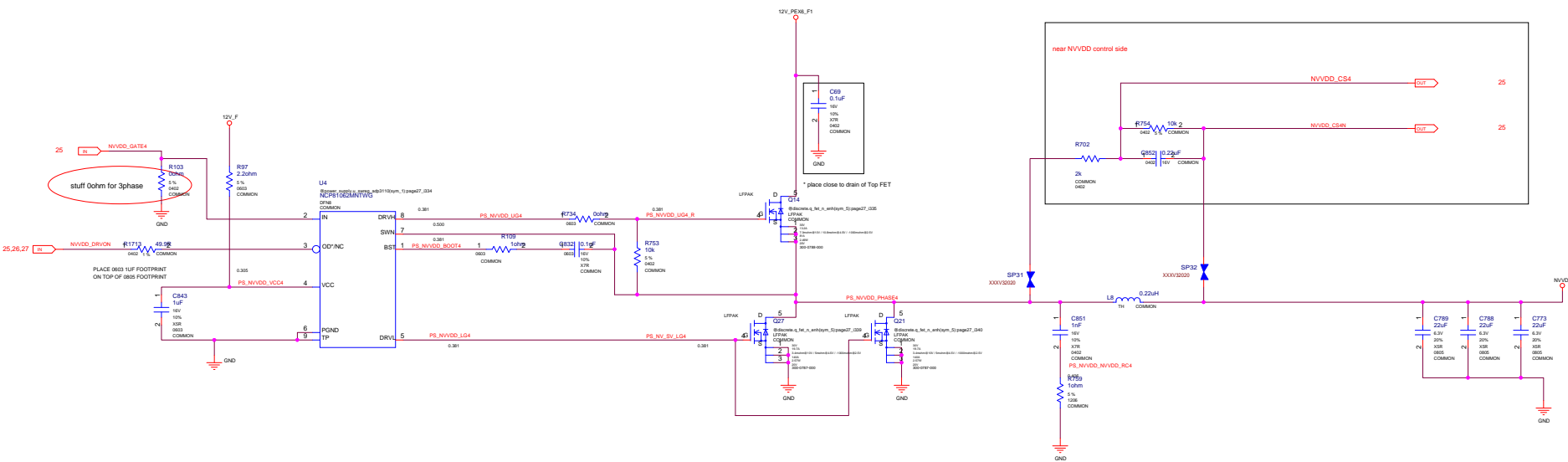
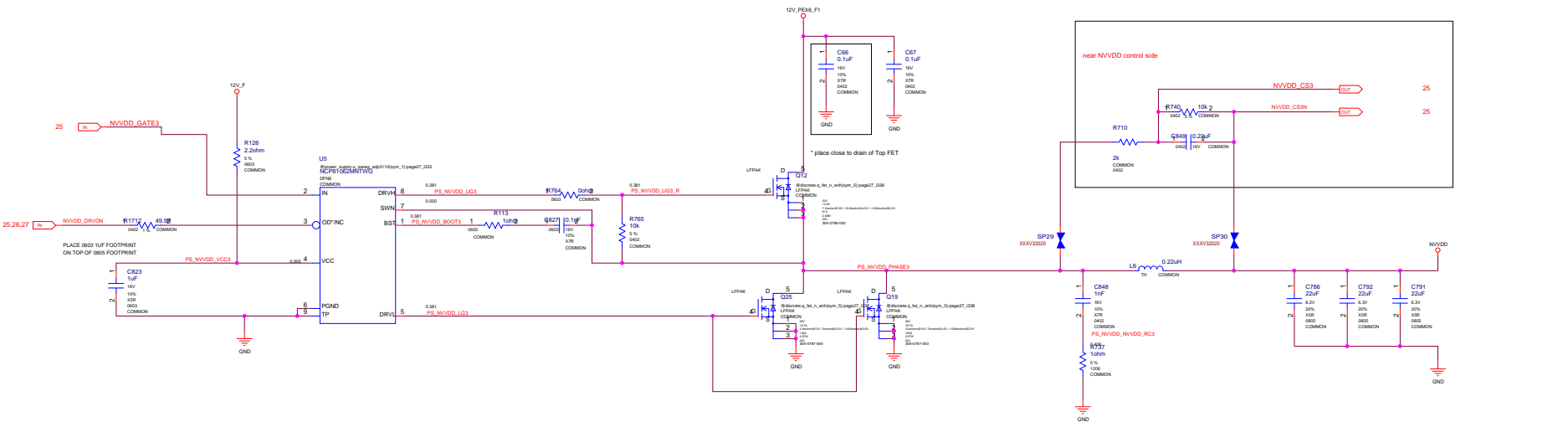
PS: NVVDD Phase 1,2



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PS: NVVDD Phase 3,4



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	A	B	C	D	E	F	G	H
1								
2								
3								
4								
5								

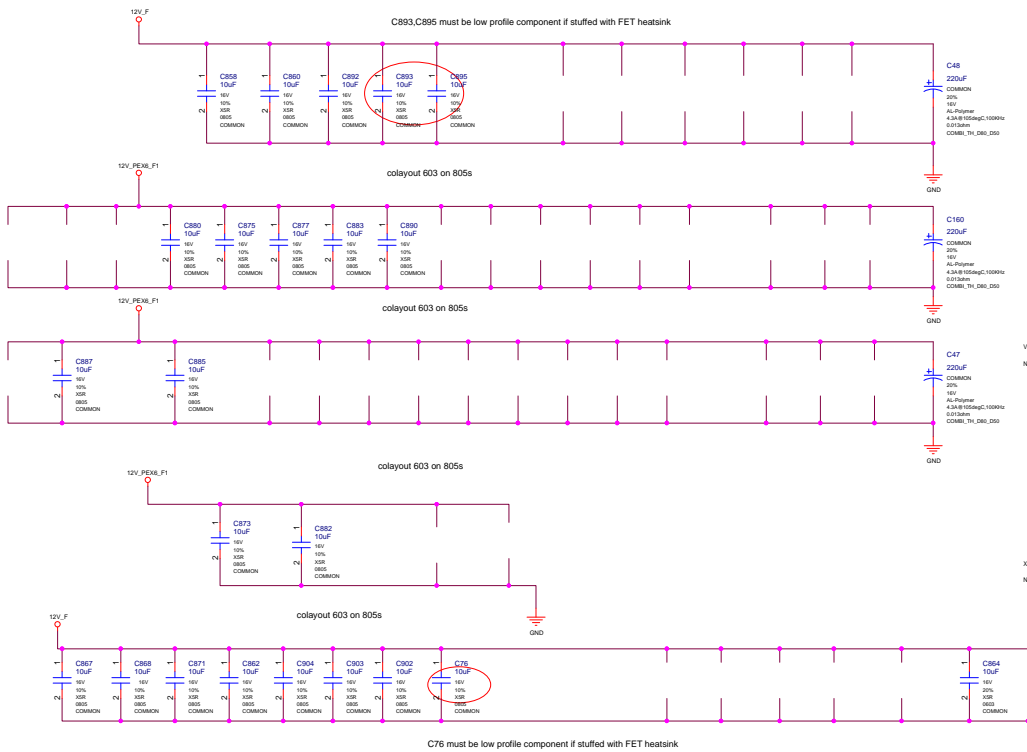
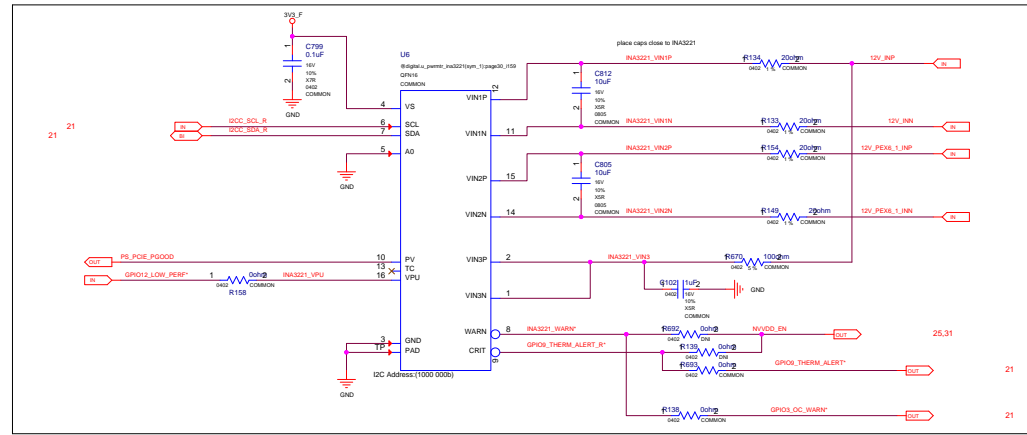
PS: NVVDD OVR2+1 POWER

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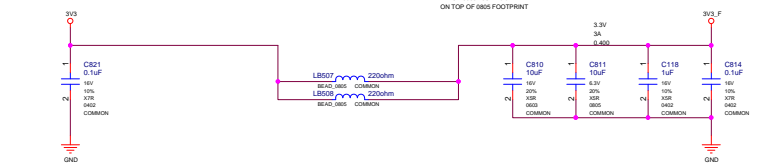
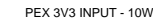


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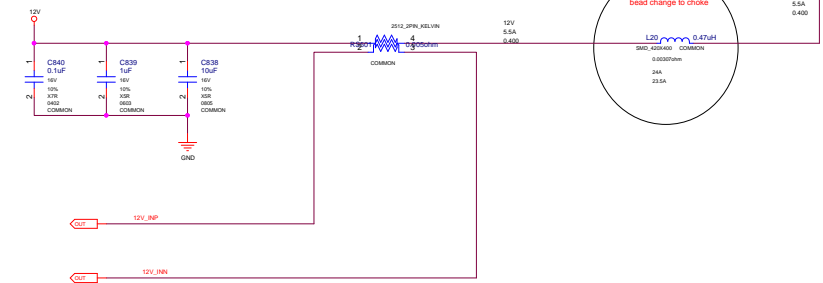
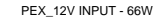
PS: Inputs, Filtering, and Monitoring



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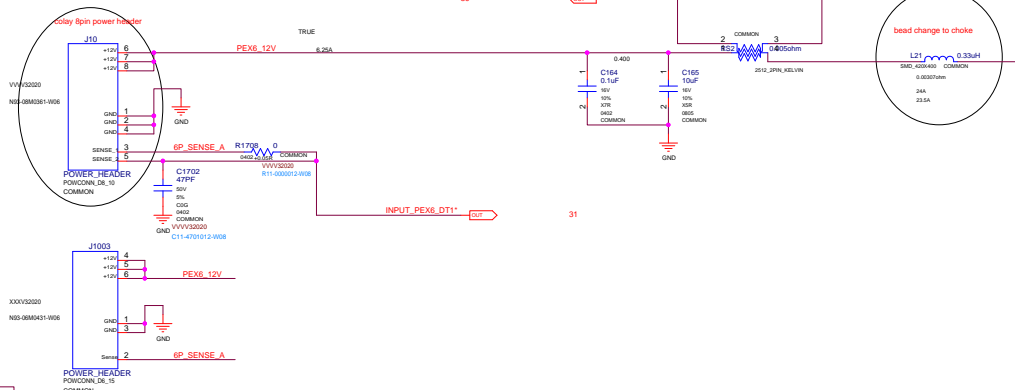
PLACE 0803 10UF FOOTPRINT
ON TOP OF 0805 FOOTPRINT



bead change to choke

PEX6 INPUT - 2x3 PCIE CON 75W

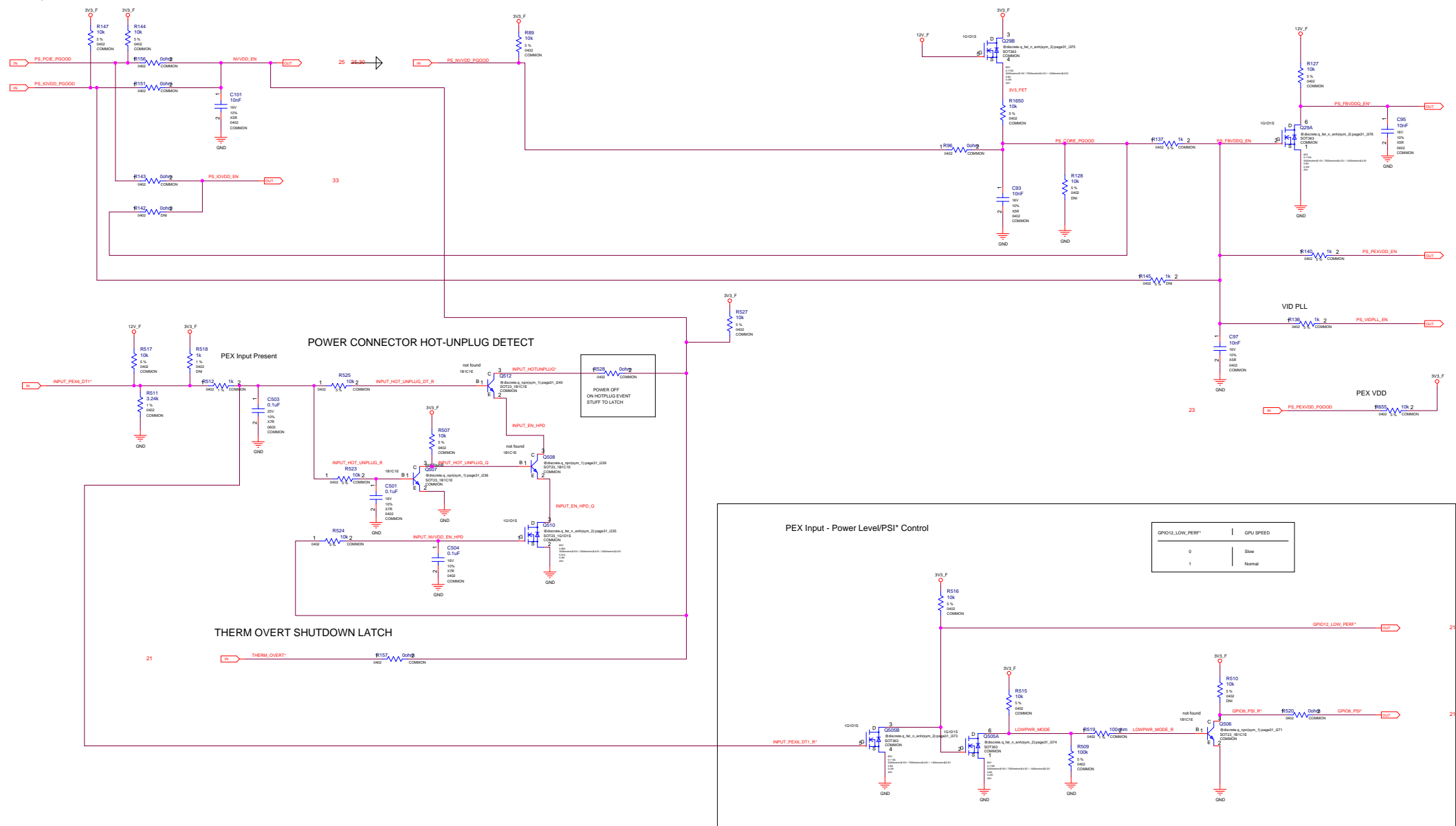
PLACE ON NORTH SIDE



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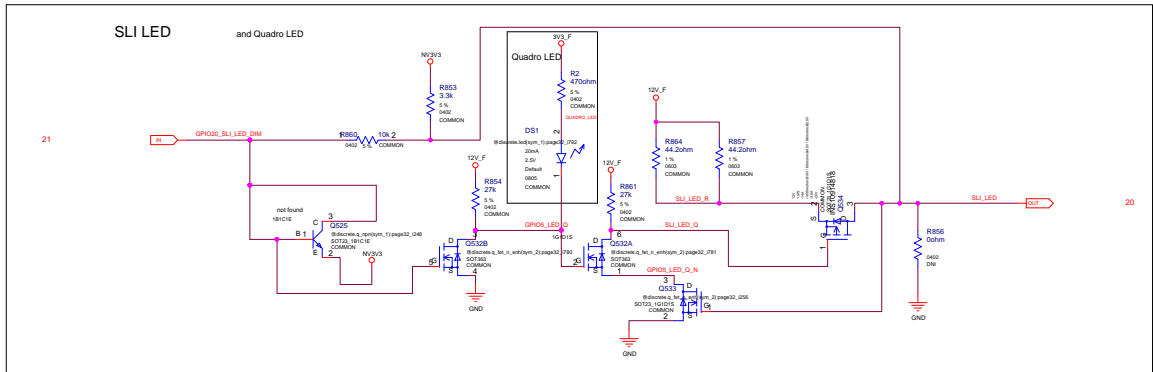
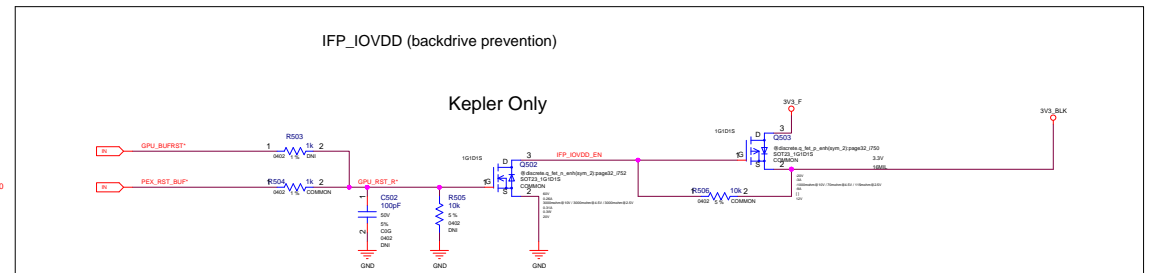
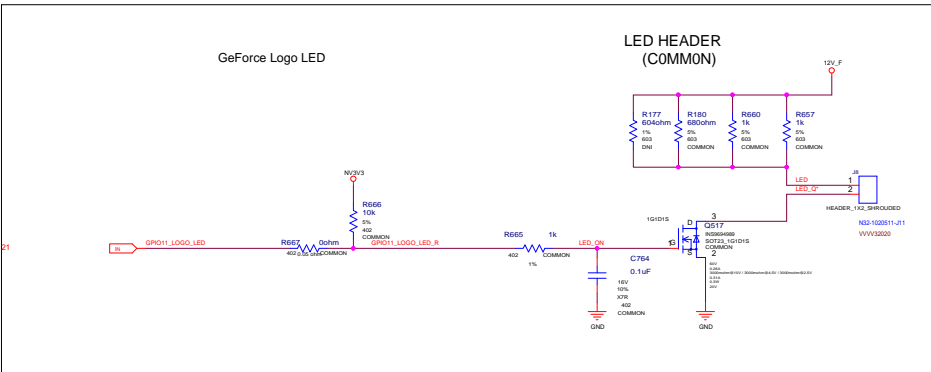
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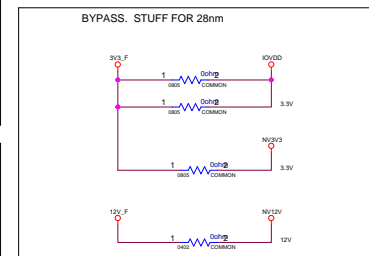
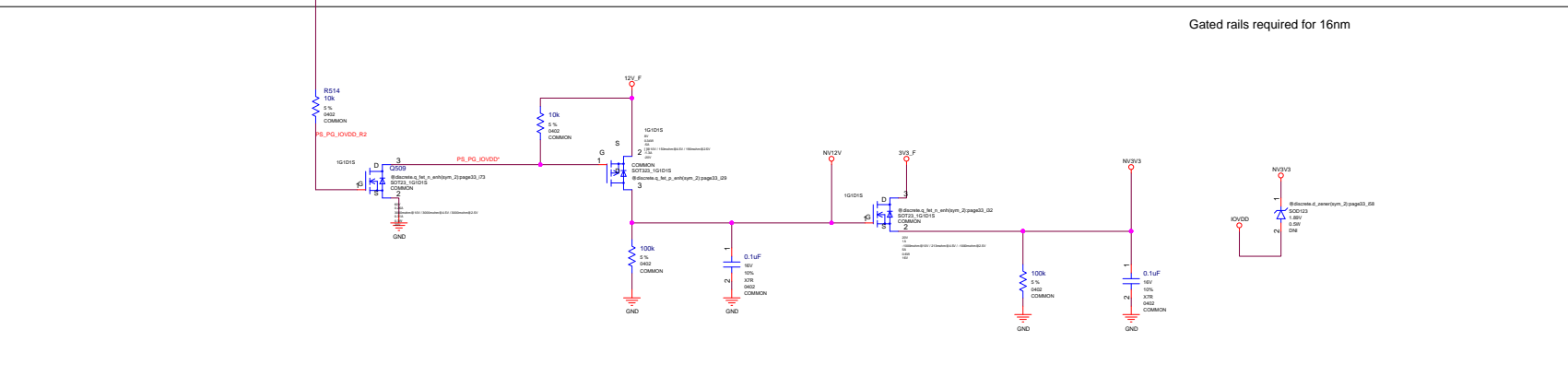
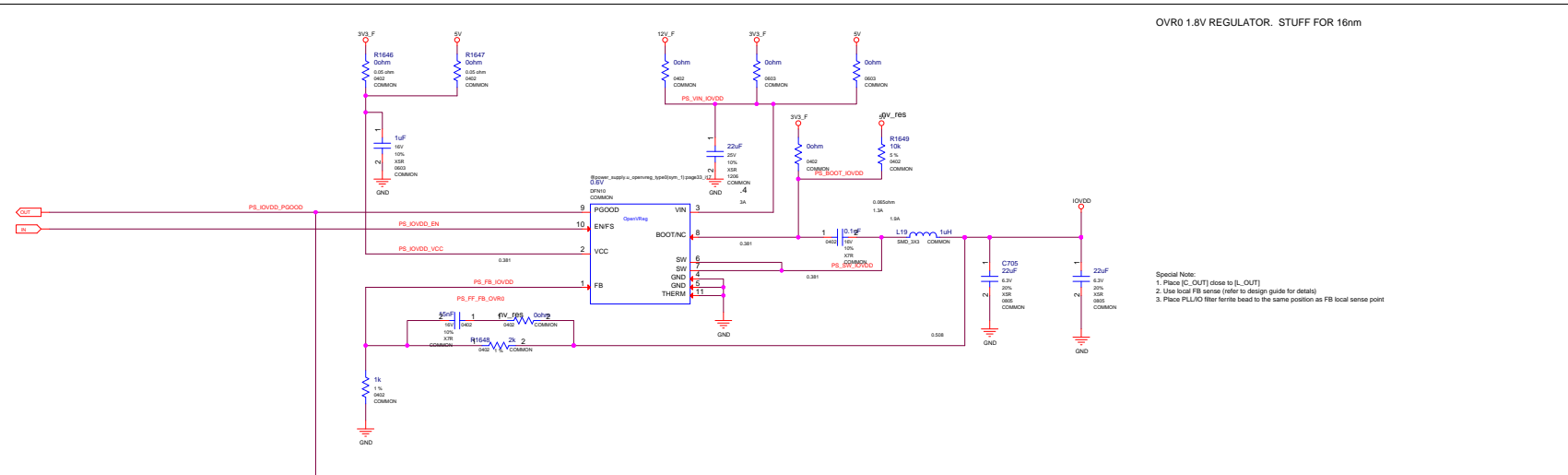
PS: Sequence and Shutdown



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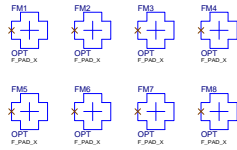
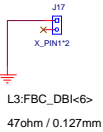
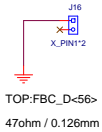
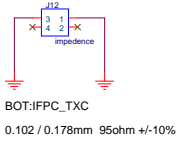
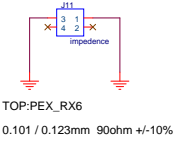
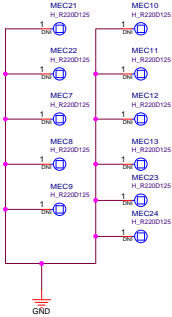
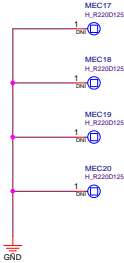
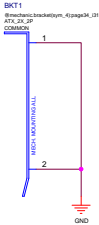
LEDs





Mechanical: Bracket/Thermal Solution

Brackets:



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