

# 30P126 - NV30 Production/BringUp Board

30P126\_A05 - NV30 FC BGA, 128MB DDR2 (4Mx32), VGA, External TMDS (Dual-Link)  
Internal TV, Philips VIDEO Capture, Option for Stereo.

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## Calibration Resistors

AGPCALPD_VDDQ	- 50 Ohm to AGPVDDQ (<0.75u)
AGPCALPD_GND	- 50 Ohm to GND (<0.75u)
FB_CAL_PD_VDDQ	- 47.5 Ohm to FBVDDQ (<0.75u)
FB_CAL_GND	- 47.5 Ohm to GND (<0.75u)
FB_CAL_TERM_GND	- 50 Ohm to GND (<1.2u)
FB_CAL_TERM_VDDQ	- 50 Ohm to FBVDDQ (<0.75u)
SAGP2CALPD_VDDQ	- 50 Ohm to SAGPVDDQ (<0.75u)
SAGP2CALPD_GND	- 50 Ohm to GND (<0.75u)
SAGP2CALPD_GND	- 50 Ohm to GND (<0.75u)
D1D2_CAL_PD_VDDQ	- 50 Ohm to VDDQ
D1D2_CAL_GND	- 50 Ohm to GND

## GPIO Assignments

GPIO	Type	Function
GPIO_0	IN	LOAD_TEST (Quickswitch)
GPIO_1	IN	Hot Plug/Unplug from DVI - Secondary - Bottom Fan PWM Control, LOW_FAN off, HIGH_FAN on
GPIO_2	OUT	Select NVUDD VSEL0
GPIO_3	OUT	Reserved
GPIO_4	OUT	Select NVUDD VSEL0
GPIO_5	OUT	Select NVUDD VSEL0
GPIO_6	OUT	Select NVUDD VSEL1
GPIO_7	OUT	SEL_2ND_DEV (Quickswitch)
GPIO_8	IN	GPU_SLOW_MODE# (THERM_ALERT# & EXSENSE)
GPIO_9	IN	Reserved

FAN will RUN when GPIO\_2 is tristated.

## Connector I2C Assignments

Display Connector	NV30 Output	I2C Channel
VGA DVI-I (south)	DAC A DAC B	B+DVO A B

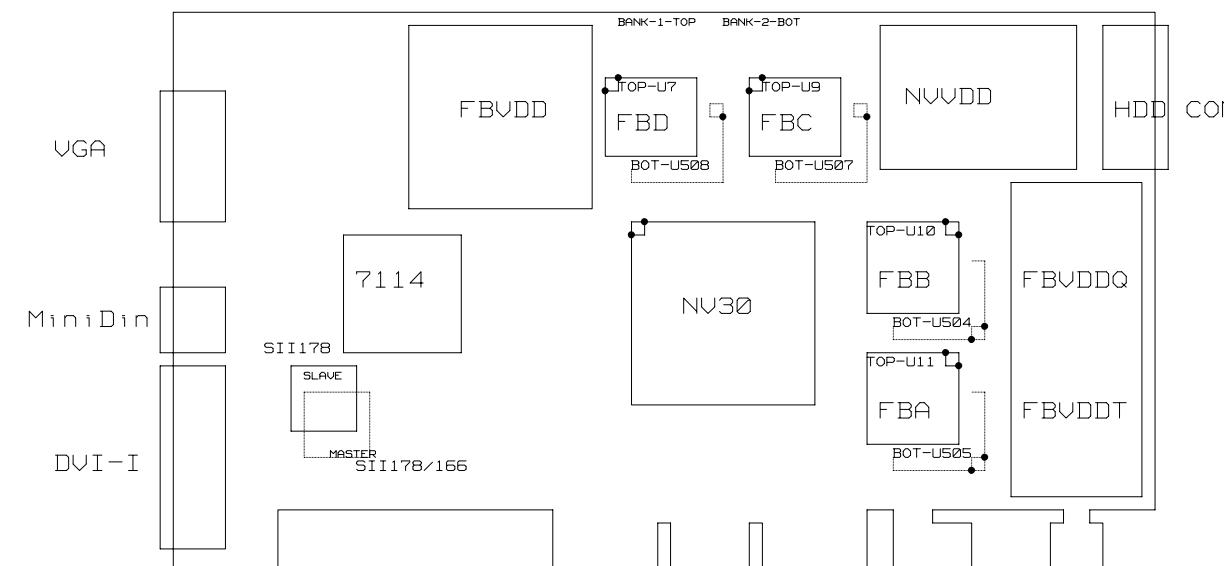
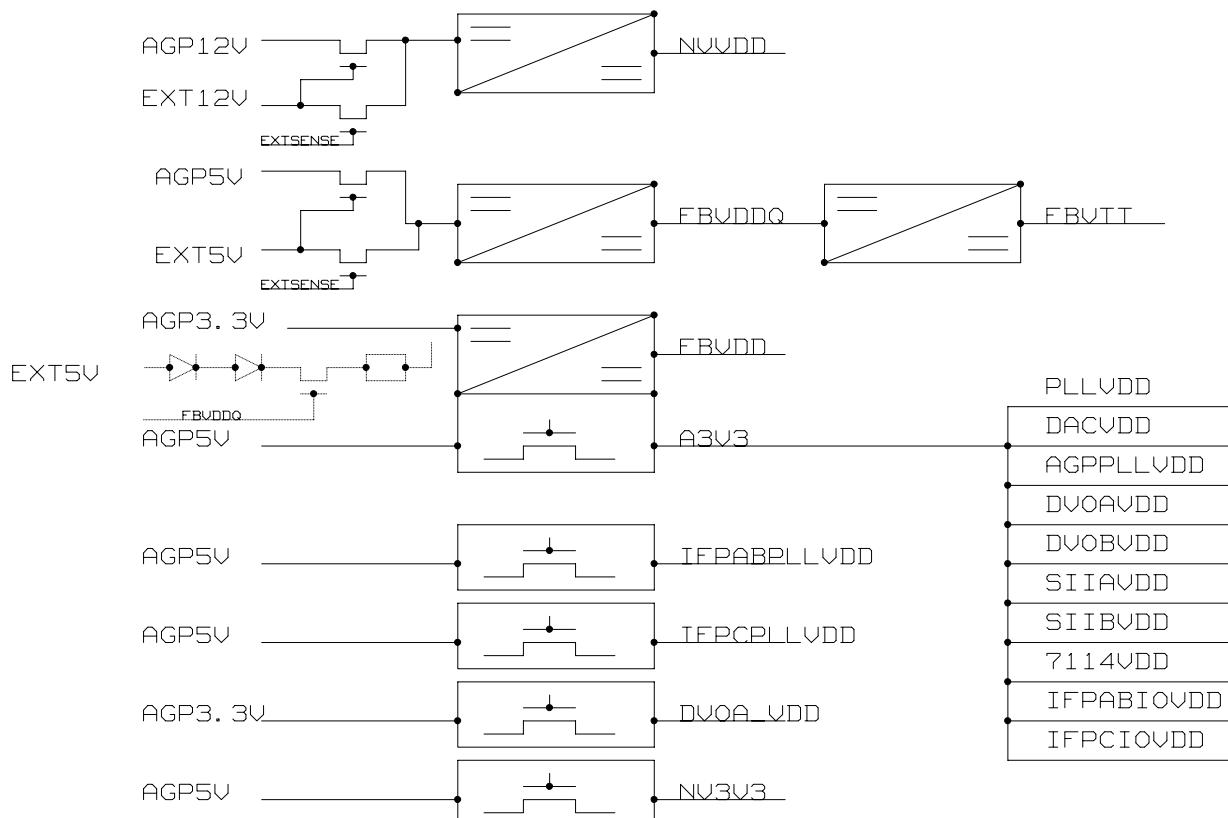
\* \* \* NOTE: \* \* \*

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SCH SCH 602-10126-0002-005

SCH Ver: 12

## Power Topology



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## History: P126-A00

PLEASE REFER PREVIOUS VERSION SCHEMATICS ( A04 )

## History: P126-A01

- X01 10/08/02 1. Add pullup and pulldn for Master S11178 to support S11164/166 in the same location  
2. Dual Mode Strap on Slave S11187 was tied to SIIA\_AVCC(3.3V). now connected to SIIA\_VCC(3.3V)
- X02 10/09/02 1. Change AGP CAL PU/DN is changed from 56ohm to 50ohm parallel combination.
- X03 10/10/02 1. Stuff AGUREFCG circuit and Change R594 from Nostuff 121K to stuff 158 K. Vref=350mV
- X04 10/12/02 1. FBUTT cap values as per SI- C728, C729, C730, C731 from 1000pF to 2.2nF  
C749, C773, C597, C585, C560, C521, 0.01uF<10nF> to 0.022uF<22nF>  
2. Add more clarity to block diagram.

## History: P126-A02

- X00 10/14/02 - Created New project from A01. Add min PCICLK length Constraint.
- X01 10/15/02 1. Update netnames for E-Tools
- X02 10/20/02 - Change TMDS Termination from No-Stuff to Stuff (NUPN 195-23000-0003-000)  
- C87 = 1uF 0805 Cap on 12V AGP from 036-30105-0076-000 to 036-30105-0057-000
- X03 10/24/02 1. Replaced various not for new design parts(147 error)  
2. Connect un used PG chip input to 3.3V rail as per Intersil recommendation  
- Add 12V pull up and pull down as per Intersil on power good chip o/p. To be used when no PG chip.  
- Add series termination res to FRWR interface.
- X04 10/25/02 1. Add anAdjustable LDO for DVDA\_VDD rail to provide 3.0V from AGP3.3V rail  
2. Add a decap for FB\_CAL\_CLK\_GND, FB clock Bias pin.  
3. Change R31 to 1K from 5.8K, R753 to 3.3K from 10K so the EXT\_SENSE signal falls low quickly(< 650uS).  
4. Add more notes for EXTSENSE and GPU\_SLOW\_MODE signals usage for s/w.
- X05 10/26/02 1. Change FB Vref voltage divider from using 120R to 1K.
- X06 10/28/02 1. C658 was No stuff, change it to stuff, it is not under Heat sink.  
2. Update Remote sense cap assy as per layout and bom.

## History: P126-A03

- X01 10/30/02 1. Change C737, C738, C783, C784 to 0603 from 0402  
2. PCB A02 was not gerberized correct, corrected PCB is A03. Rolling SCH for A04

## History: P126-A04

- X00 11/04/02 1. Change U506 to 0.5% part
- X01 11/05/02 1. Change NUVD compensation to R608, R589, C598 to No stuff, C604 = 0.1uF, R573 = 39K.  
2. NUVD, FBVDD Inductor of 3mhmm type from 6mhmm type.  
3. Change FAN circuit CAPs to 0805 from 0603.
- X02 11/07/02 1. Do changes for Barry III, FBCAL-357ohm, Add 1pF cap for FBUREF.  
2. No stuff CLK\_Bias cap. DANGER.
- X03 11/08/02 1. Add a diode in parallel to Q507, Cahnge R536, FBVDDQ OCset to 56.1k from 95.K
- X04 11/12/02 1. IFPRSET changed from 1K to 1.5K.  
2. CLK term at Memory cahnged to 225R, Zq for 128MB is 182R, 64MB is 90.9R, DAC Rest is 68R  
3. FBVDD logic FET is changed to higher current version.  
4. FB\_I2O CAL is 40R, CLK CAL is 549R for 226ohm source term, 357ohm for 100ohm CLK source term  
5. DVDA Reg Rtop=976ohm, Rbot 598R for standard values instead of 180R 5% and 137R 5%
- X05 11/21/02 1. Change Q511, for Idmax from 12A to 18A @ 25degC.

## History: P126-A05

- X00 11/22/02 1. Add pull down to TSTMODE pin, Add pull up to 6225-0deg Phase. Replace FBVDD fets to 20V Vgs from 12 Vgs  
2. Remove cap for FB\_CAL\_CLK\_GND, ADD cap for FBUREF to FBVDDQ, Add one more 1200uF CAP for FBVDD  
3. ISL6569 and FET drivers on same power plane, EXTSENSE moved to EXT\_SV, Add EZ1117 Reg for GPU 3v3
- X01 11/25/02 1. Remove Firewire section. Change R804<10K> from 5% to 1% R805 from 1.5K to 1.4K 1%. See notes.
- X02 11/26/02 1. Remove TAB bracket, Replace SlimVGA w/ standard VGA, Add pull down to hot plug ckt,  
2. Move FBVDDQ to EXT\_12V from EXT\_12V. Add gateing FETs instead of Diodes. Remove FRWRVDD, Inductor, 2caps  
3. For NUVD PS EXT\_12V is through a gating FET instead of Diode/No diode.  
4. Add discrete logic AND for EXTSENSE using Ext12V and Ext5V.  
5. Remove Supplemental power connection resistors to FBVDD rail, No CGND2  
6. Swapped LOAD\_TEST, GPIO3\_VSEL2 nets to GPU.  
7. Set Higher threshold to disconnect AGP rails when EXT rail is used by using Voltage divider
- X03 11/30/02 1. Move DVI\_HPD pull down before series resistor, otherwise it was forming a voltage divider..  
2. Delete Firewire enable strap(pull up).  
3. Add adjustment note for Q511, 3v3\_6529 to be 330Mohm, it is already 330mohm..  
4. Delete 8 nos. 0805 res on signal FB\_3.3V - Supplemental power ckt.  
5. Add Zener threshold detector for 12V ext detect  
6. Enable AGP-Rail FETs directly by EXT\_Rails. Body diode helps Rail transistions
- X04 12/02/02 1. CB30 and CB34 can not be connected to NV3V3, move to 3v3 as it was.
- X05 12/03/02 1. Move following from 3V3 to A3V3 for layout: R55, R56, U12, C265, R720, R719, R678.  
2. Move following from 3V3 to NV3V3 for layout: R608, R604, R605, R606.  
3. Change FBVDDQ PS input cap from 80mn to 100mn cap with > 4.0A ripple current
- X06 12/04/02 1. Update:Block diagram, Power topology, GPIO table, descriptions as per A05 baord  
2. R722 changed to A3V3 from 3V3  
3. The following changed from 3V3 to NV3V5: UB-D102 power pins, C701, R601, Q514  
4. New NET AGP\_12V\_OFF and 0402 cap and a resistor.  
5. New NET AGP\_5V\_OFF and 0402 cap and a resistor.  
6. Add GPIO control using FET, each fet controls only 3 VID pins
- X07 12/05/02 1. R705, R706 changed to 0402 from 0603. Added a cap to CGND to STEREO\_SV\_LC
- X08 12/05/02 1. R705, R706 changed to 0402 from 0603. Updated BRKT1
- X09 12/06/02 1. Updated GPIO Pages
- X10 12/08/02 1. Resequenced RefDes
- X10 12/09/02 1. Adjusted Resistor Values for External Sense Circuit  
2. Changed Upper FET of 6225 to IRF7822  
3. Removed 3 Resistors to bridge NL5 to 3V3\_6529 (not required after removing option to strap power to 3V3)
- X11 12/27/02 1. FAN circuit-Upper Cap changed to 0.01uF from 1uF, Lower caps No stuff, update variant for bracket.
- X12 12/30/02 to 01/14/03 1. NUVD Risen changed from 2.2K<13.8A/phase> to 2.32K 1%<13.8A/Phase> for better availability  
2. Update DAC Rsets/Terminations. Update NUVD default 1.2V, FBVDD=2.5V, MemCalib&Terms.  
3. Update 470uF/16V, 0.01uf/10V, 100pF/16V, Update Variant as per latest BOM.

FOR 128MB sku  
NUVD: 0.8 to 1.5V Default 1.2V  
NV3V3: 3.3V  
FBVDD: 2.5V  
FBVDD: 2.5V  
FBVDD: 2.5V  
GPU\_Uref: 0.5uF FBVDD  
MEM\_Uref: 1.08V  
CS\_Delay: 5pF +/-0.25pF has 4.7pF as alternate.  
Zq: 200R 1%  
CLK Term/Memory: 200R 1%  
FB\_CAL\_CLK(R620): 47.5R 1%  
FB\_CAL\_CLK(R620): 549R 1%  
FB\_CAL\_PU/PD(R621/623): 47.5 1%

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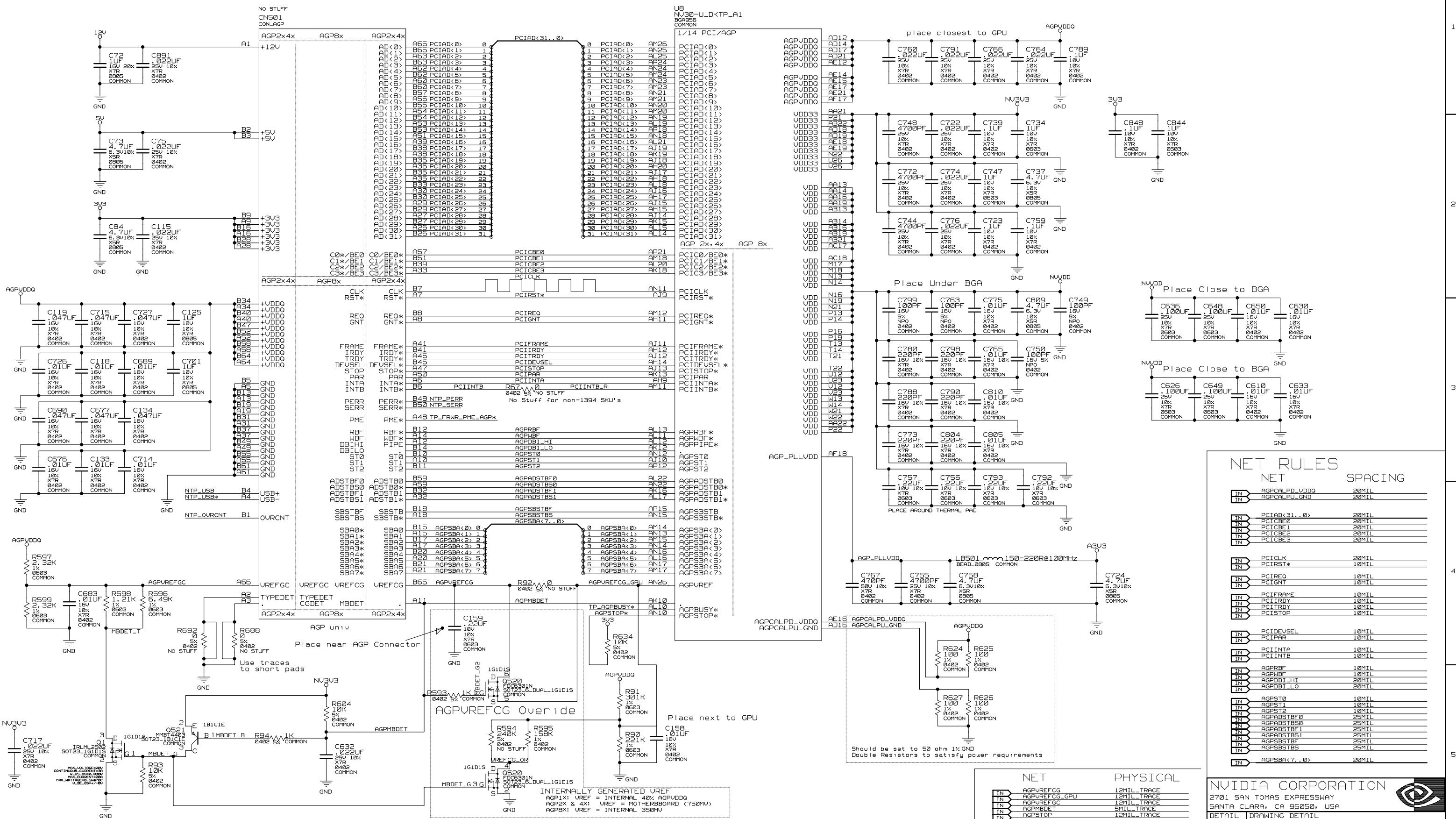
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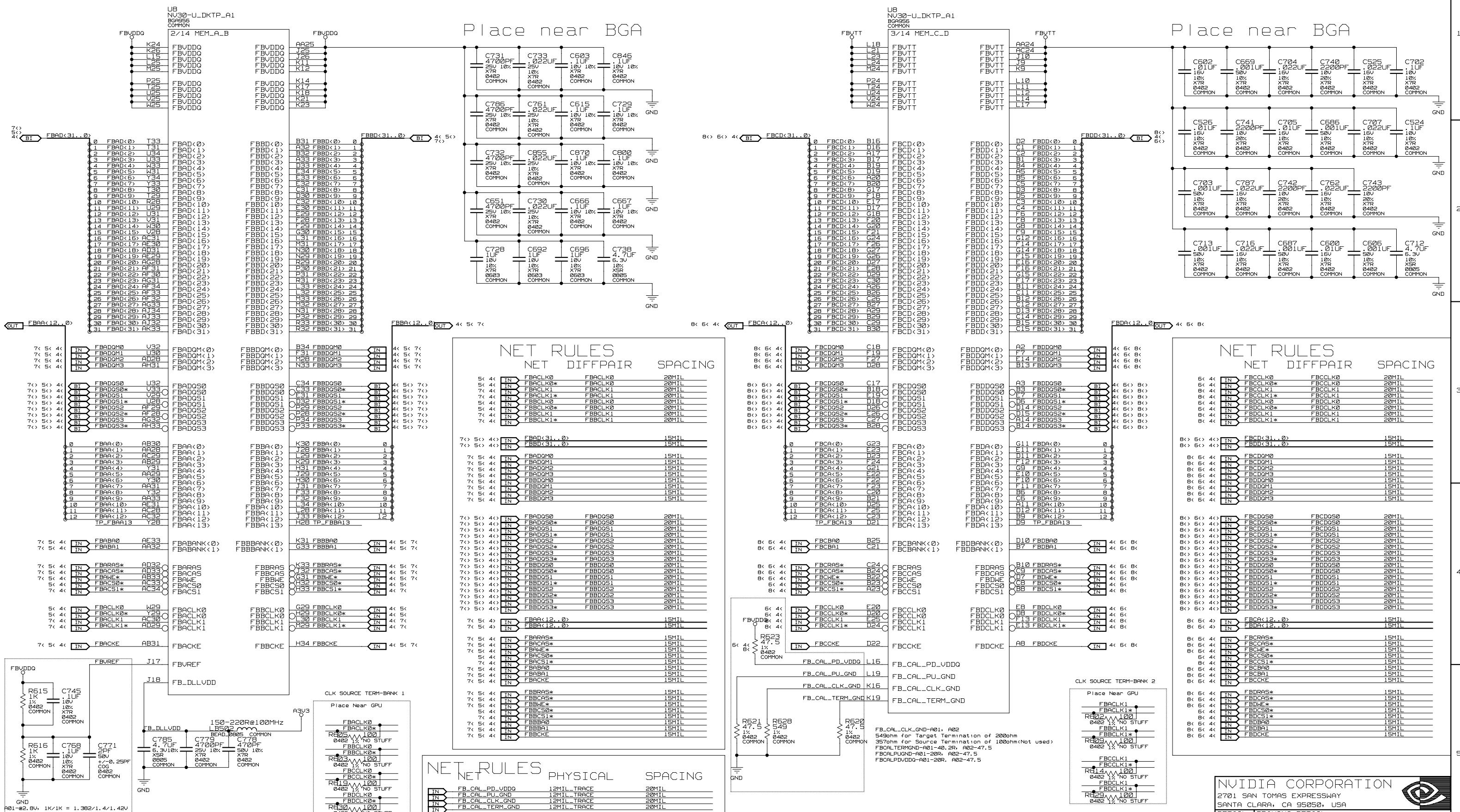
## 1. a. AGP 8X Interface



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## 2.a. Memory

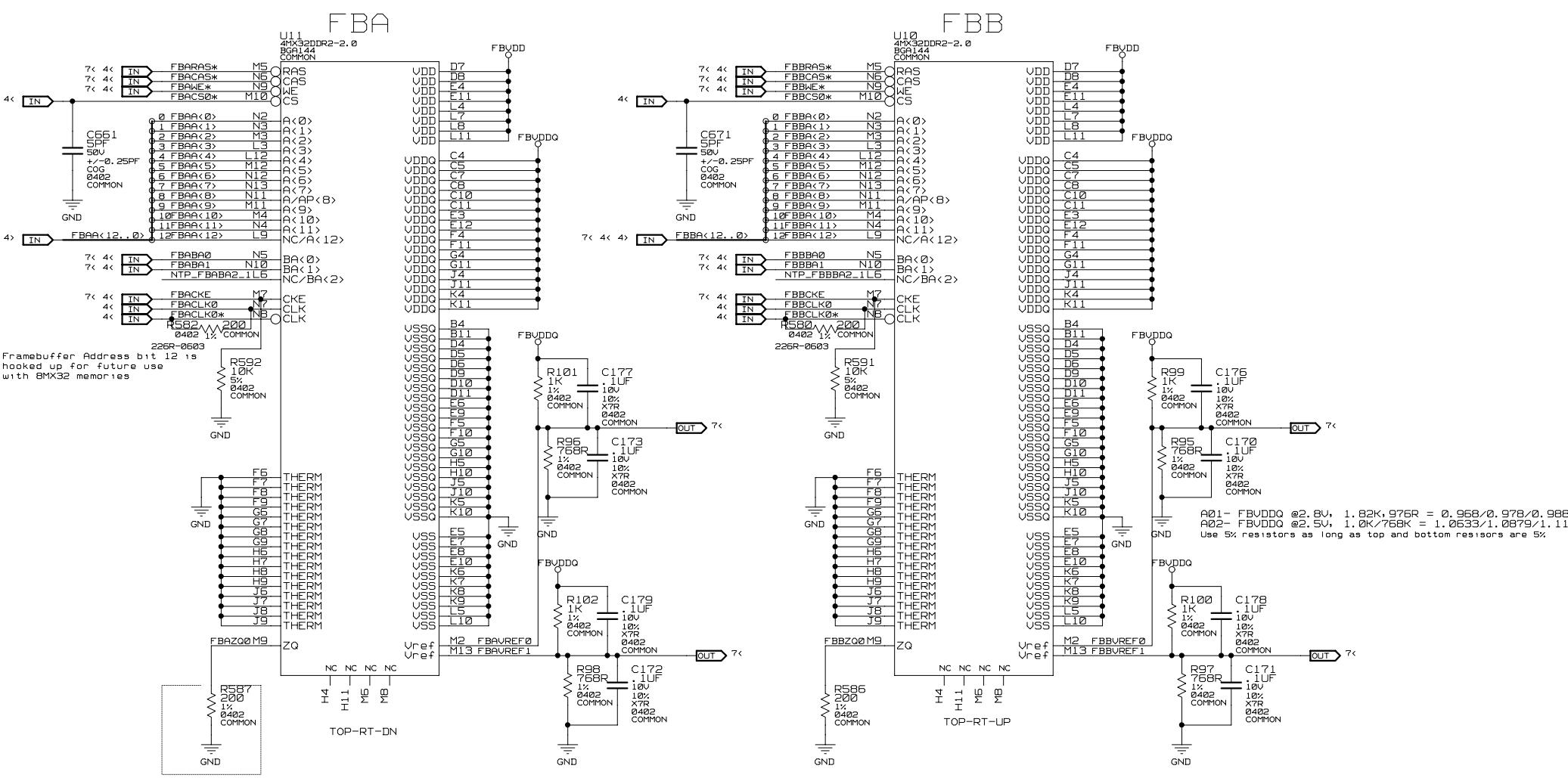


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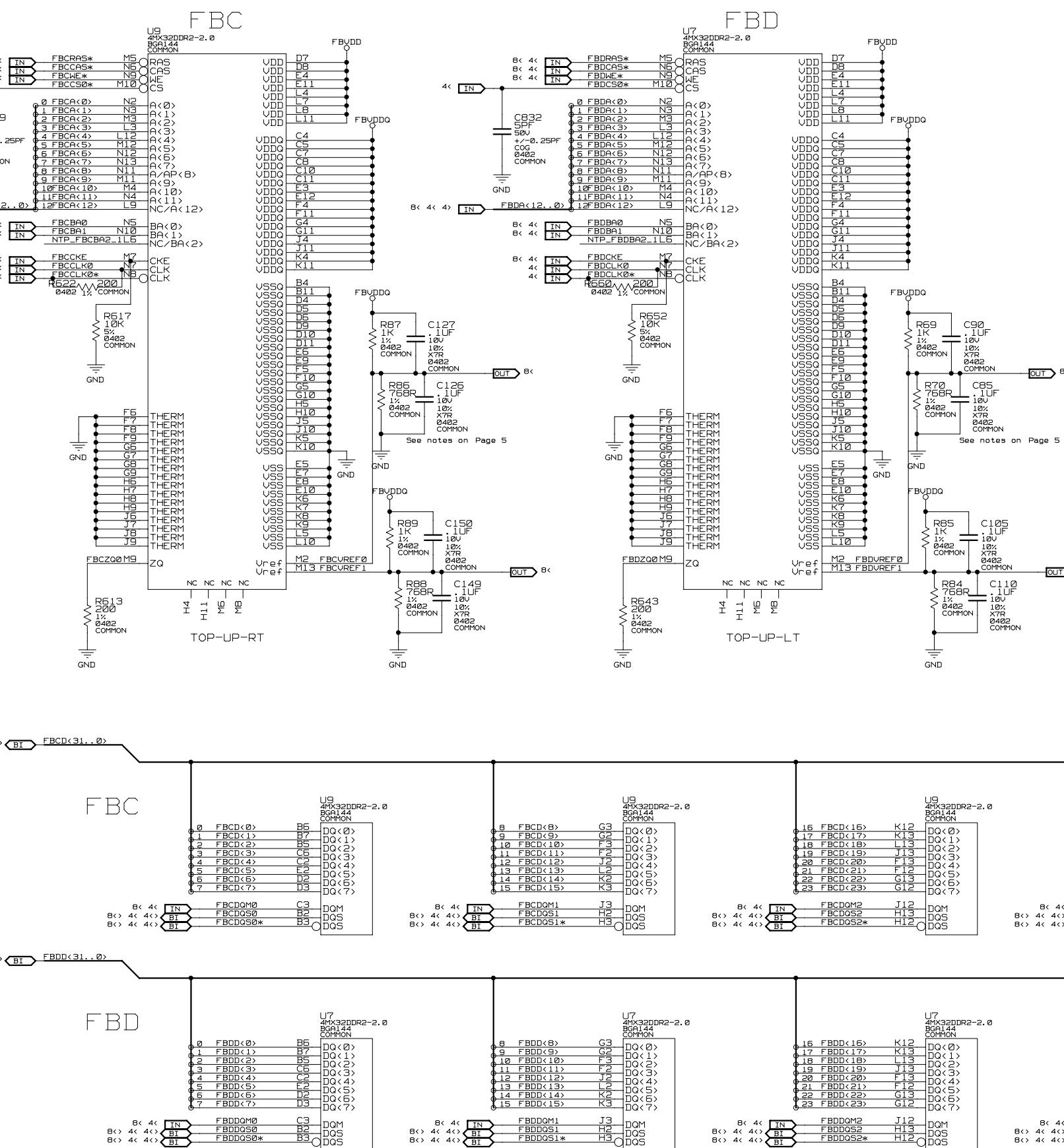
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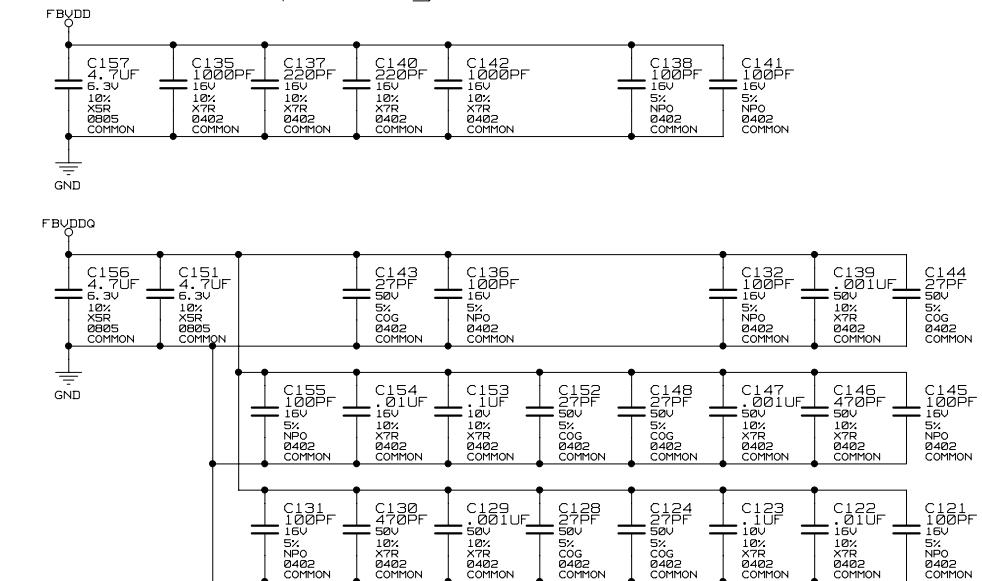
## 2.b. Memory: Bank 1: FBA & FBB



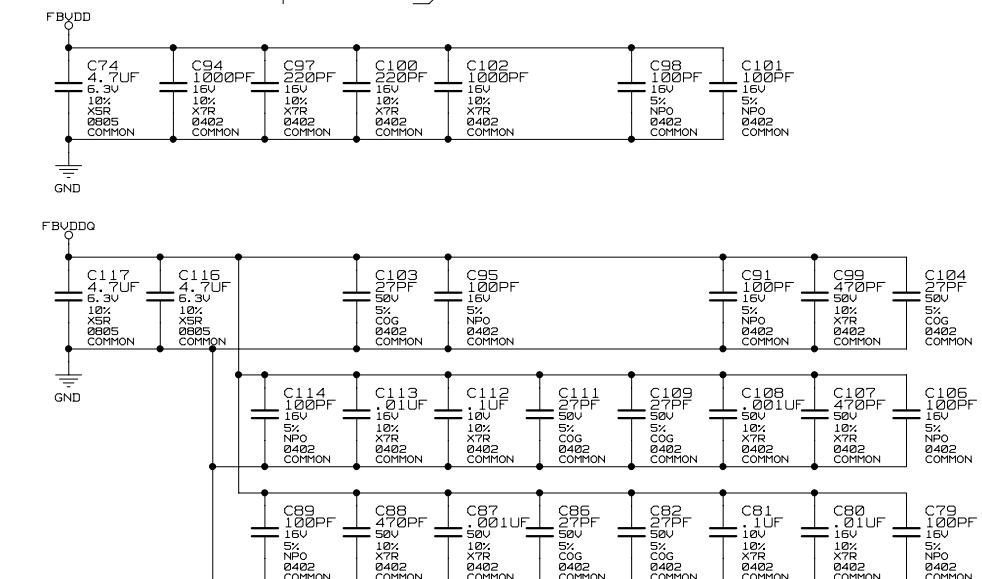
2. c. Memory: Bank 1: FBC & FBD



Decoupling for FBC



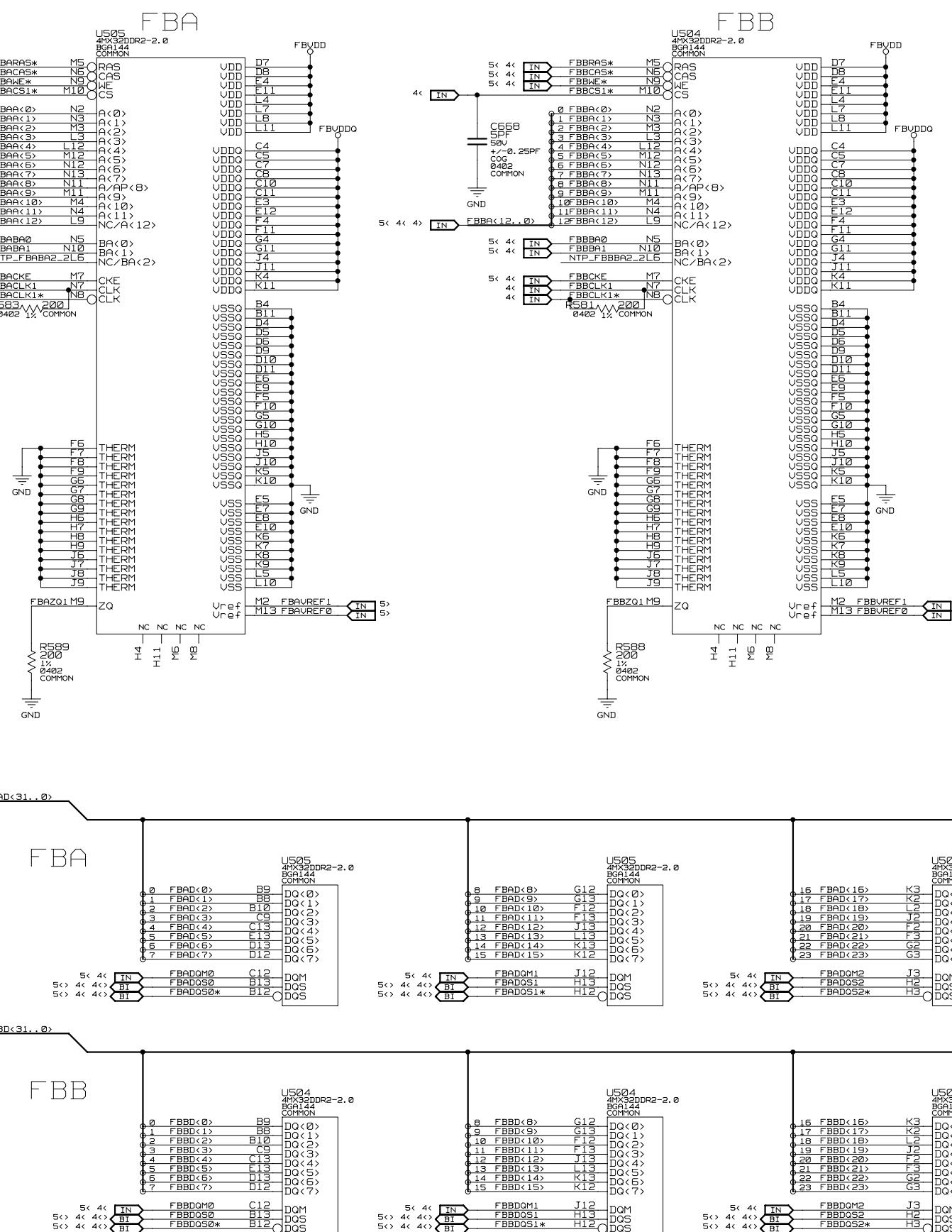
## Decoupling for FBD



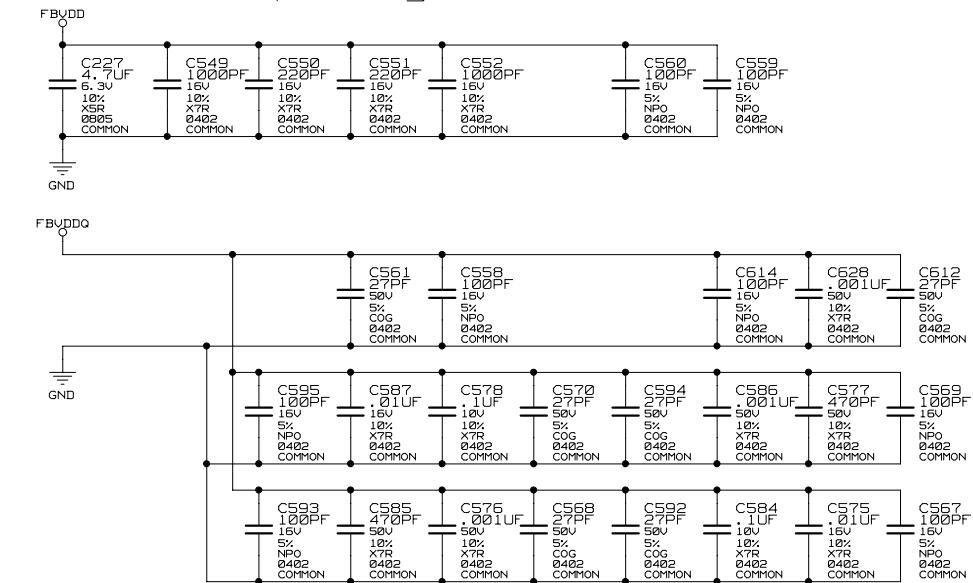
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NET RULES		PHYSICAL
NET		
	FBCZ00	12MIL_TRACE
	FBDZ00	12MIL_TRACE
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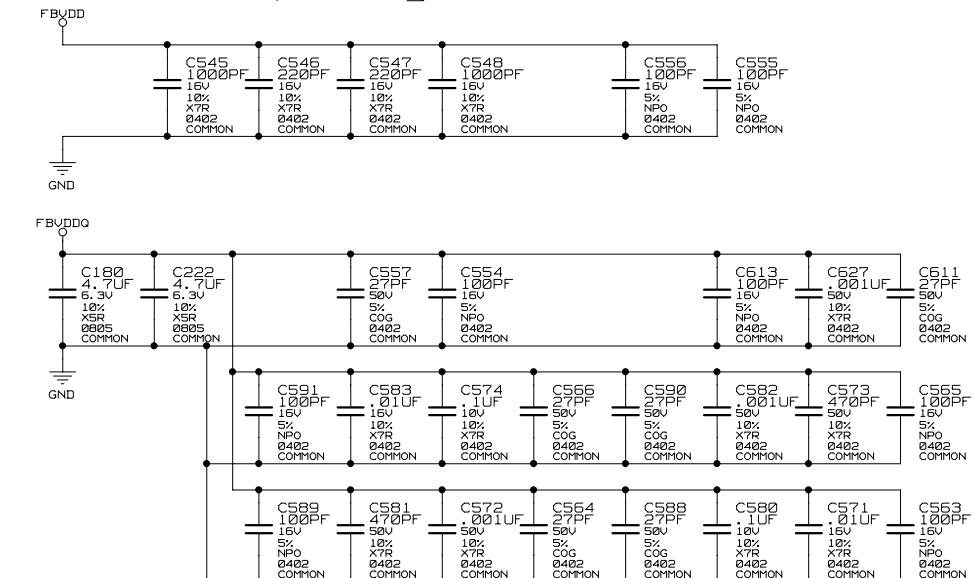
## 2. d. Memory: Bank2: FBA & FBB



## Decoupling for FBA



## Decoupling for FBB



NET RULES  
NET PHYSICAL

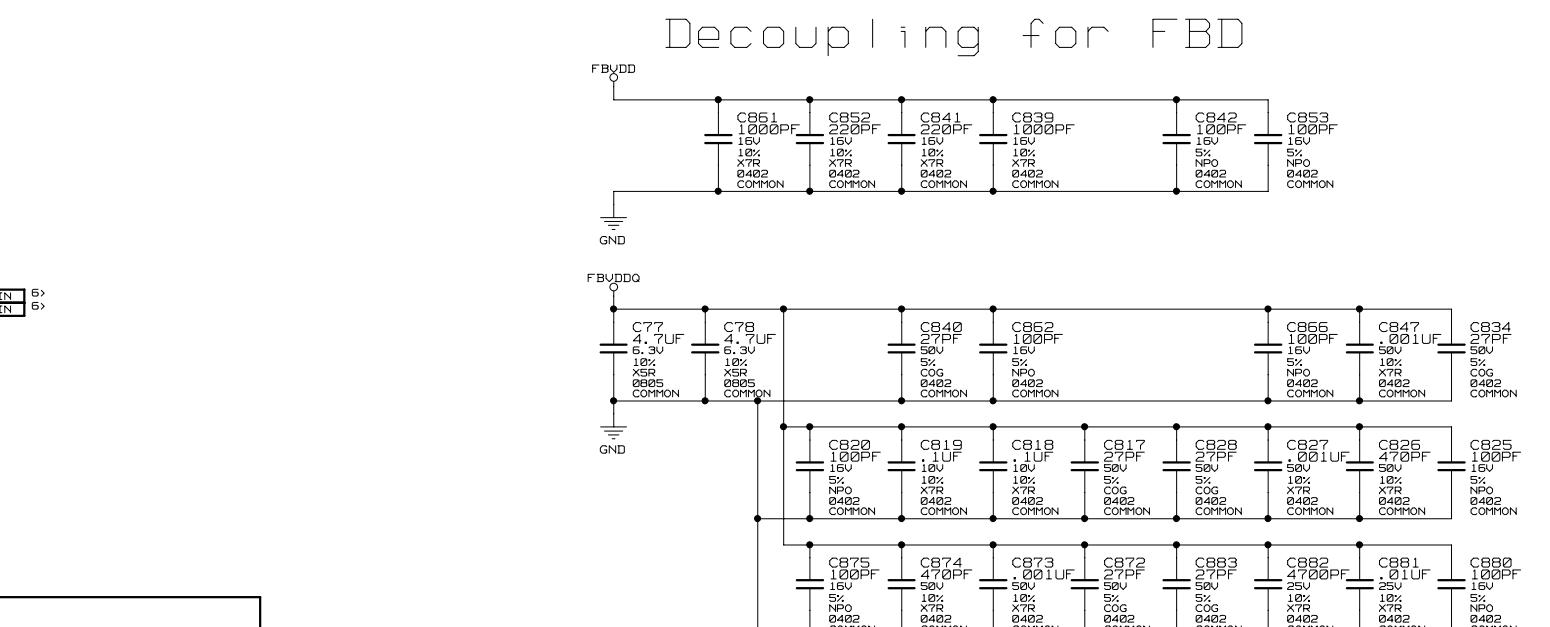
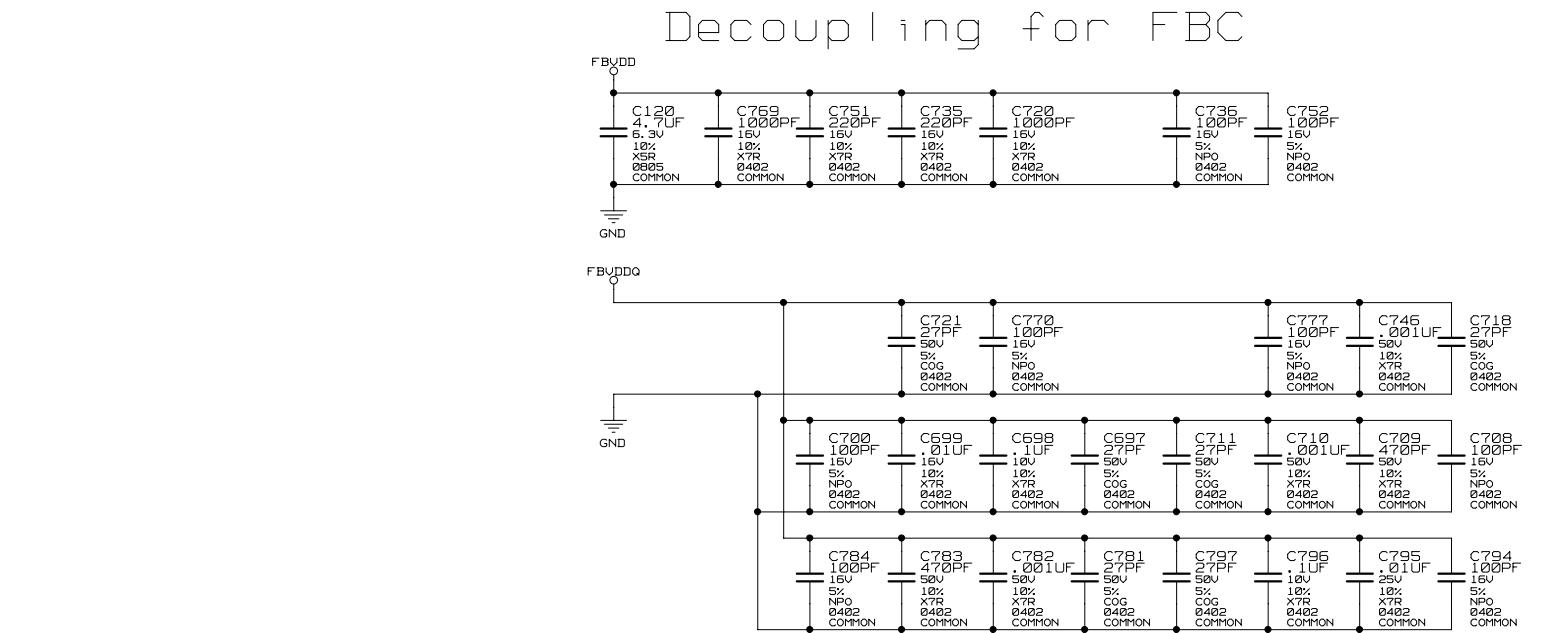
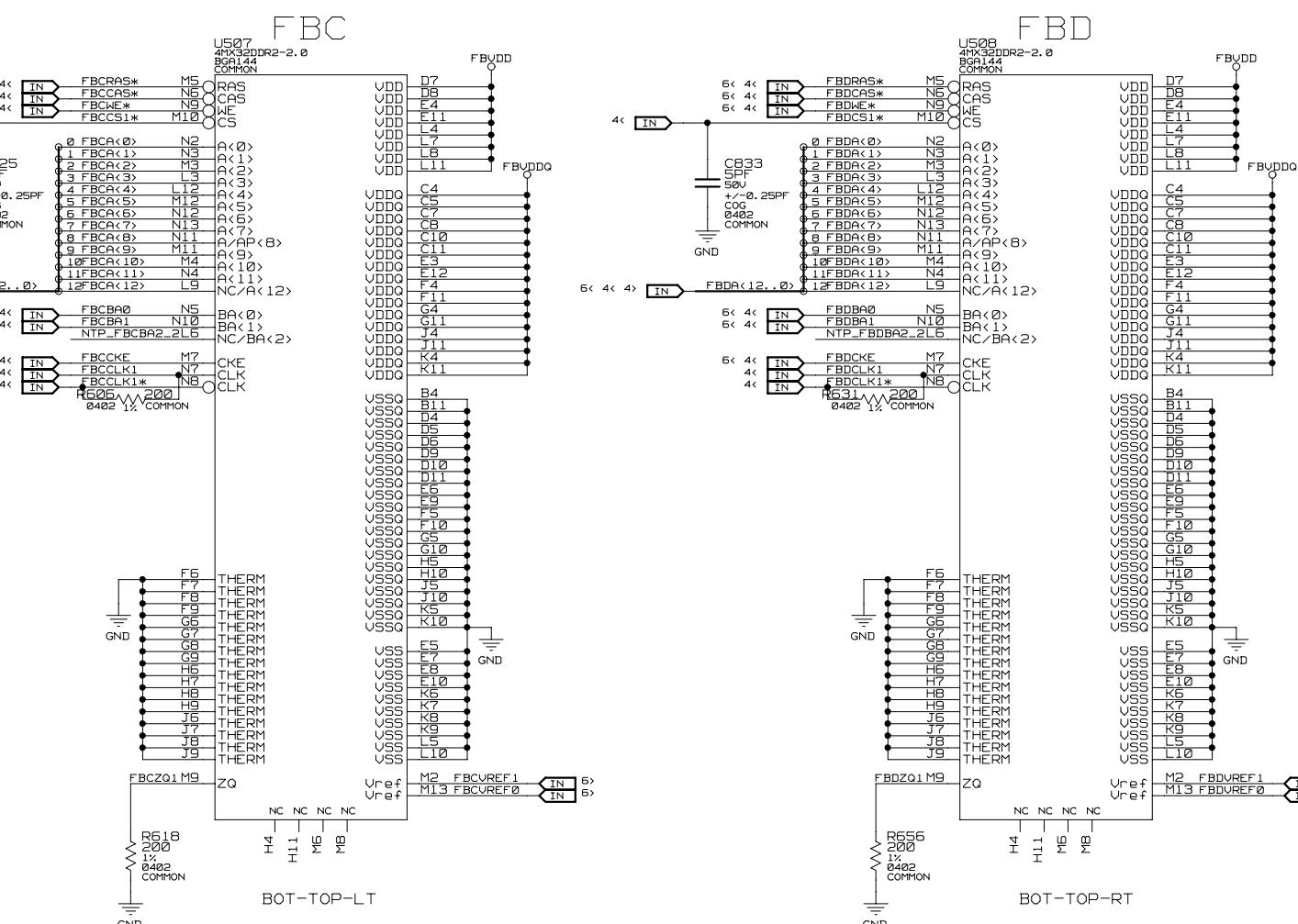
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[IN] FBZQ1 12MIL-TRACE

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2. e. Memory: Bank2: FBC & FBI

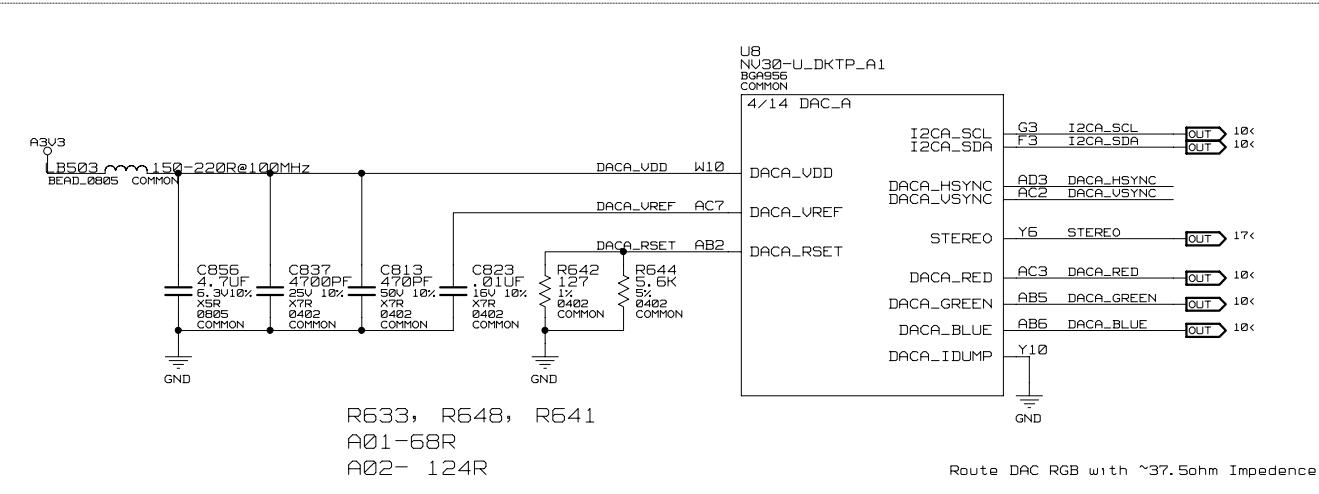


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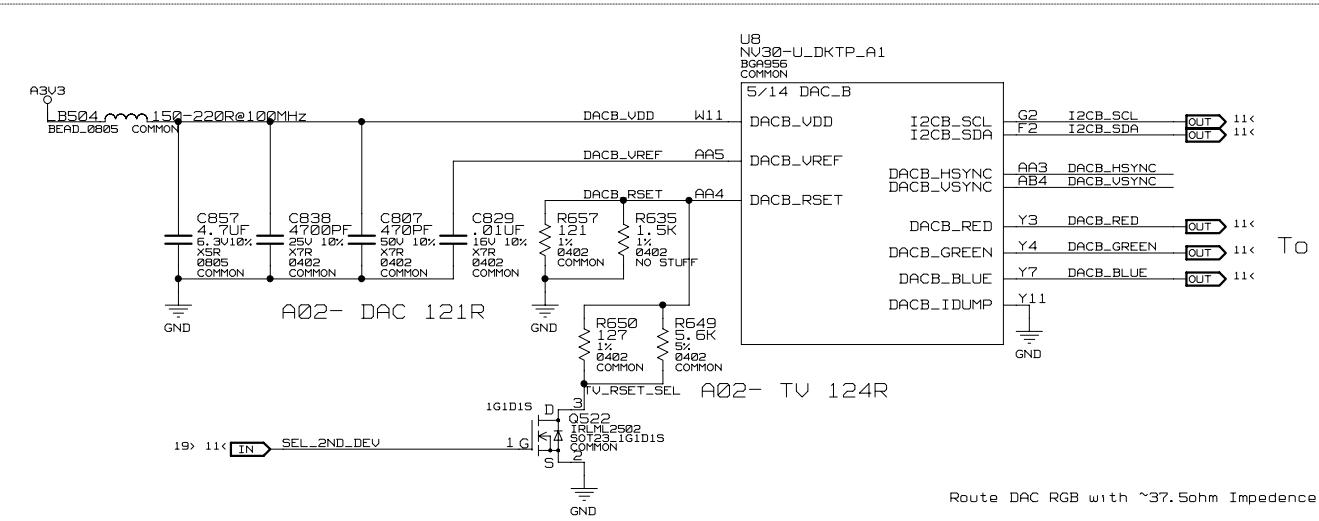
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### 3. a. DAC and PLL

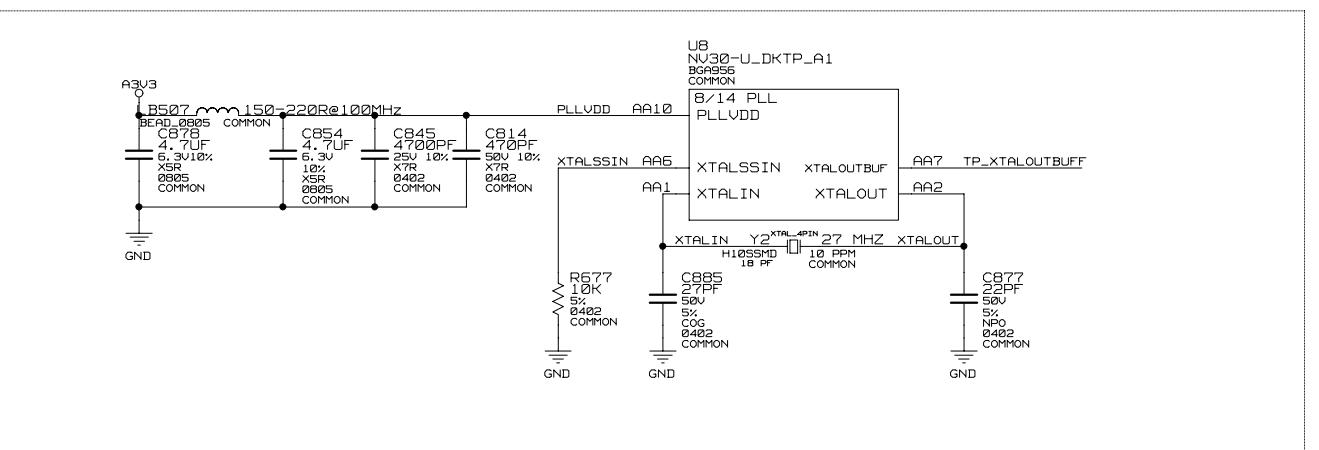
#### DACA



#### DACB

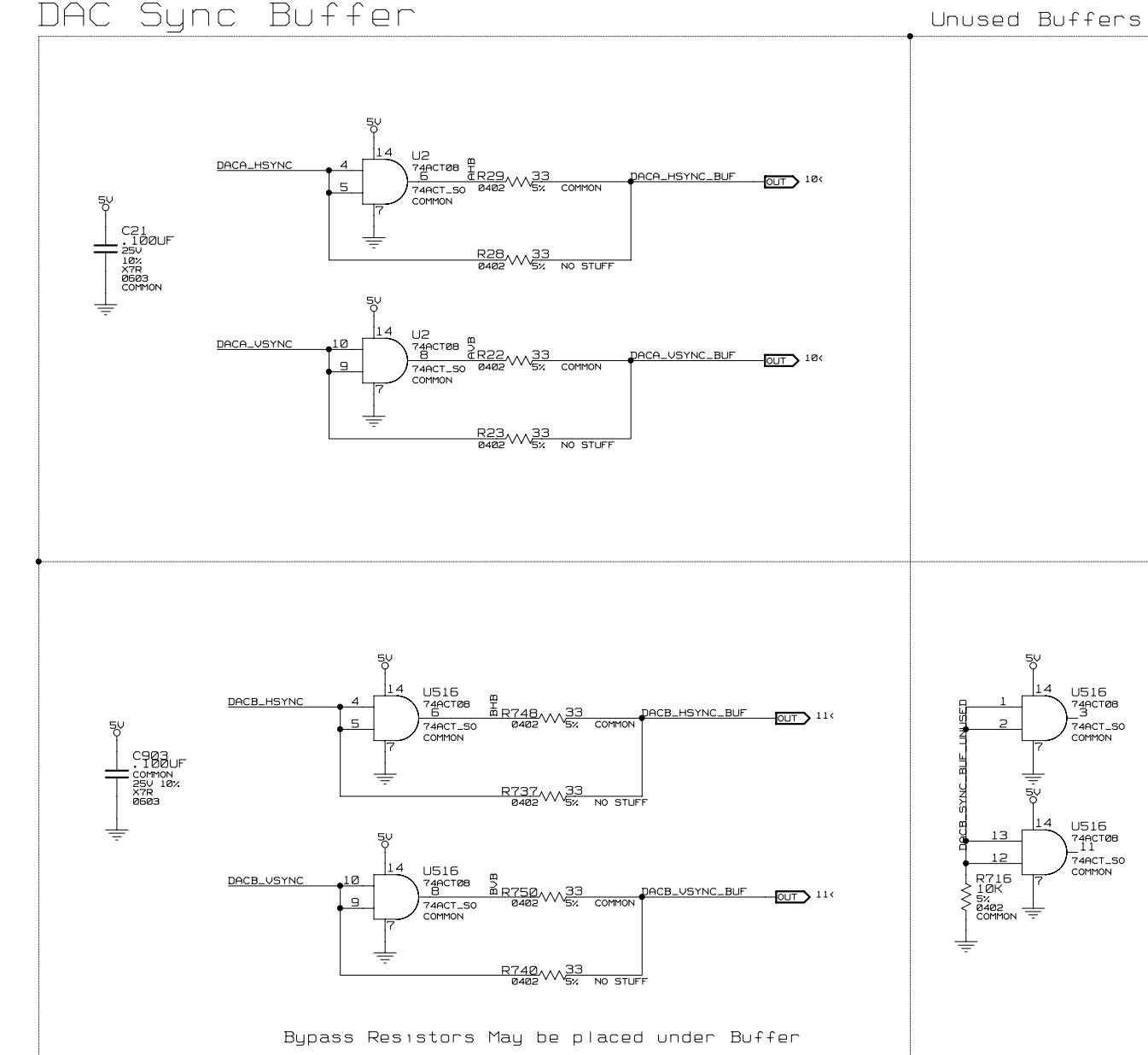


#### Xtal/PLLVDD



NET	PHYSICAL	VOLTAGE
XTAL_IN	18MIL_TRACE	
XTAL_OUT	18MIL_TRACE	
DACA_VDD	12MIL_TRACE	3.3V
DACA_VREF	5MIL_TRACE	
DACA_RSET	5MIL_TRACE	
DACB_VDD	12MIL_TRACE	3.3V
DACB_VREF	5MIL_TRACE	
DACB_RSET	5MIL_TRACE	
TV_RESET_SEL	5MIL_TRACE	
PLLVDD	12MIL_TRACE	3.3V

#### DAC Sync Buffer



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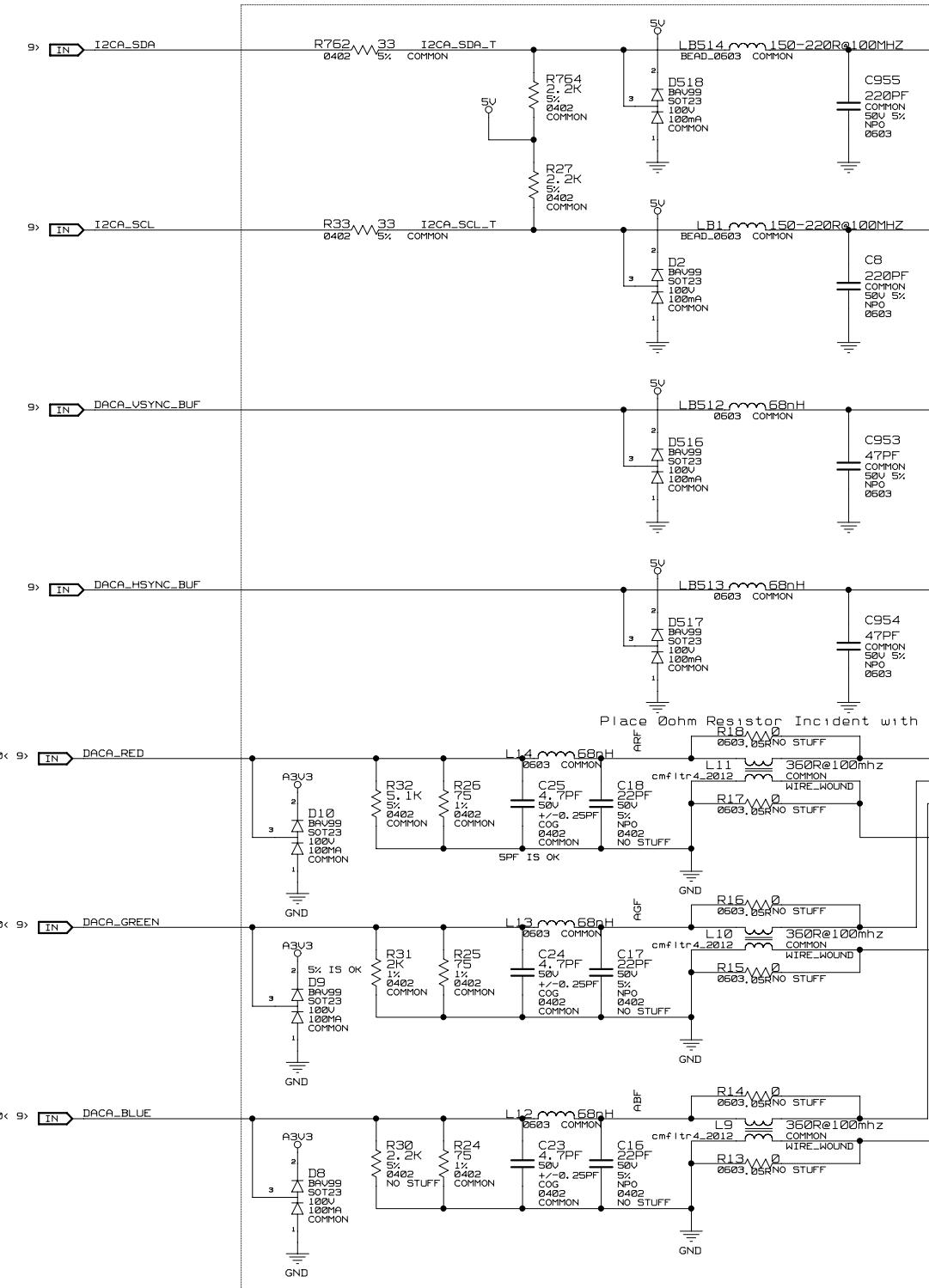
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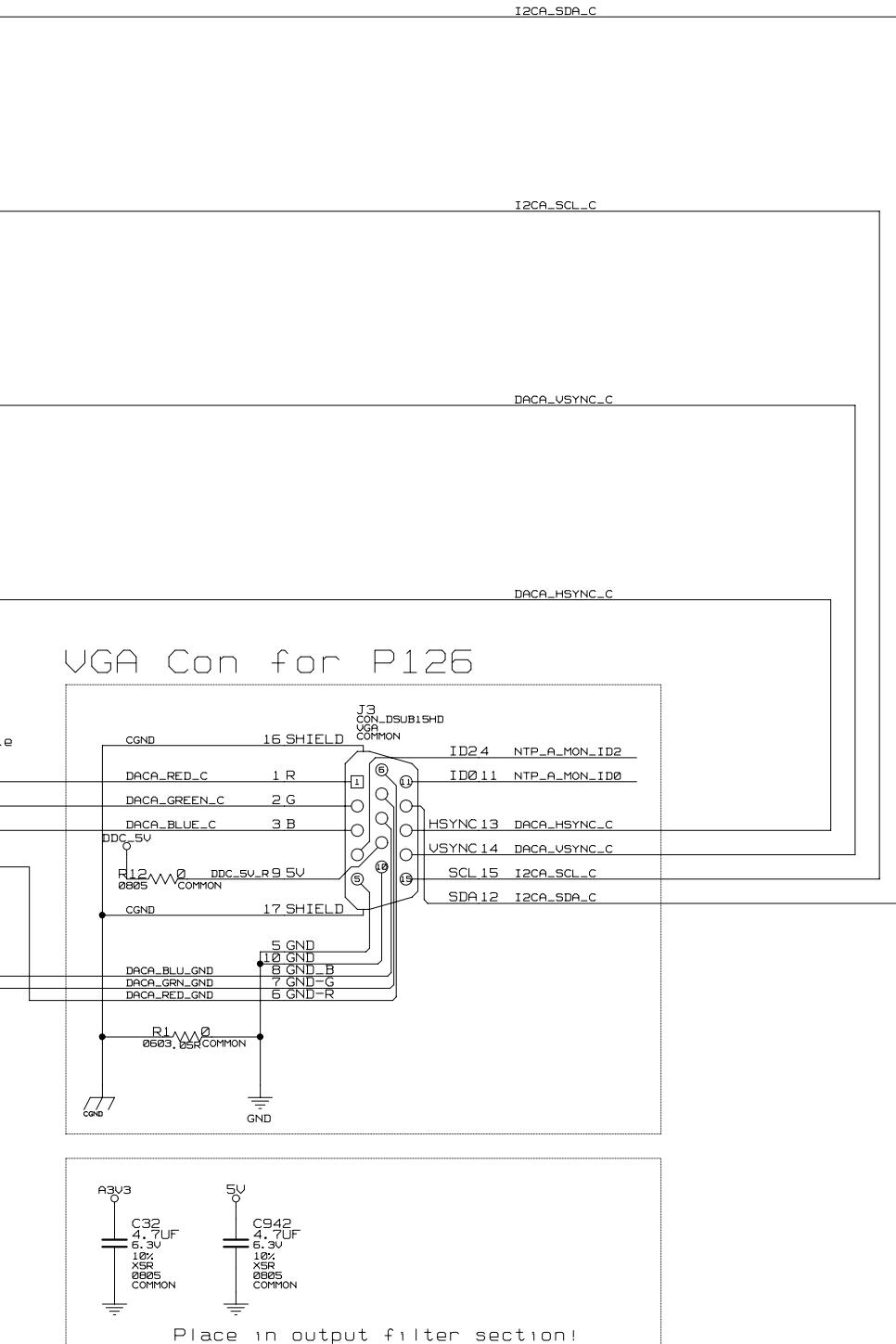
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### 3. b. DACA Output

#### RGB-FILTER



#### DACA output



#### NET RULES

NET	SPACING
DACA_RED	20MIL
DACA_GREEN	20MIL
DACA_BLUE	20MIL
DACA_RED_C	20MIL
DACA_GREEN_C	20MIL
DACA_BLUE_C	20MIL

NET	PHYSICAL
DACA_RED_GND	12MIL_TRACE
DACA_GRN_GND	12MIL_TRACE
DACA_BLU_GND	12MIL_TRACE

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DETAIL DRAWING DETAIL

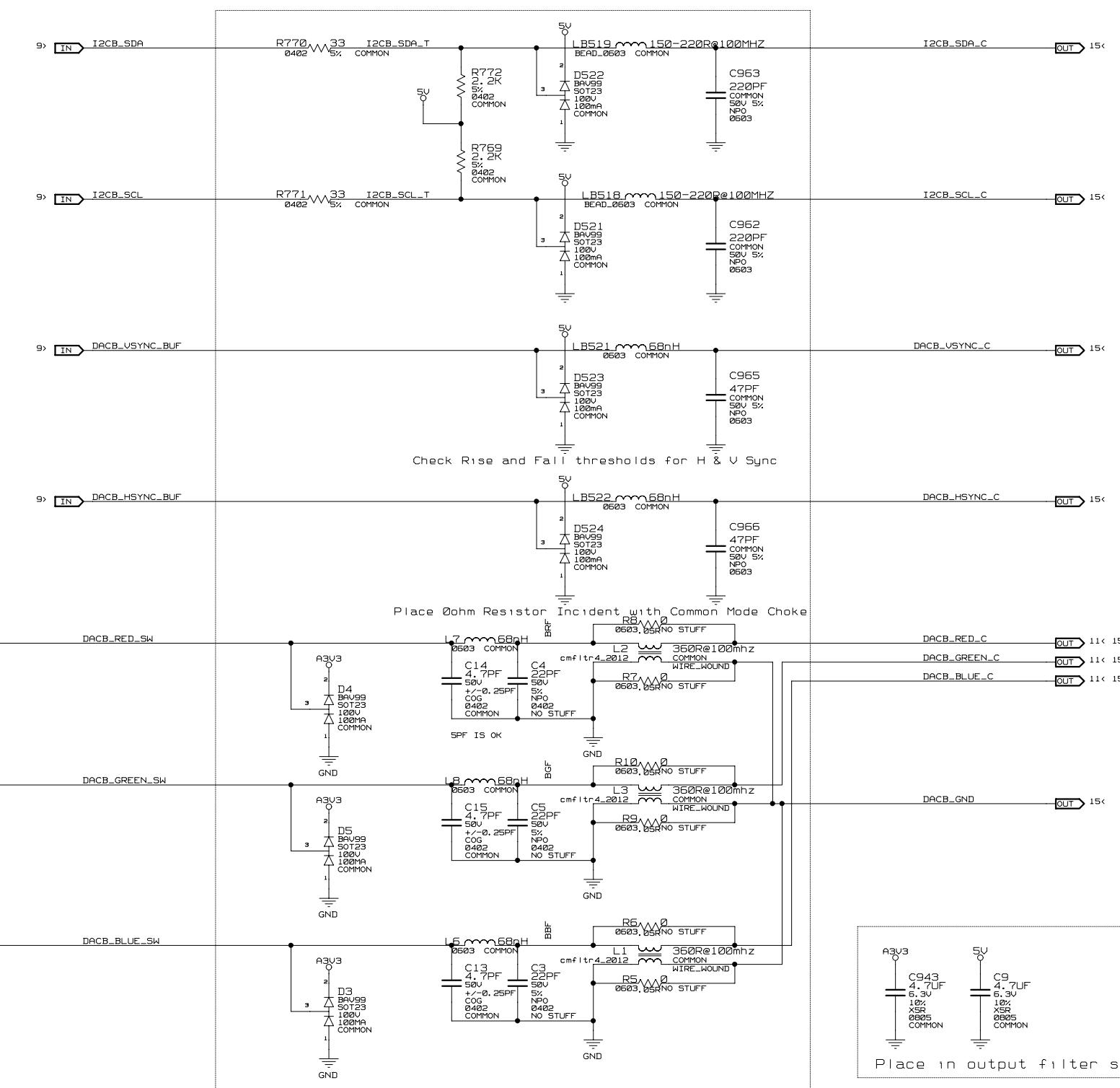
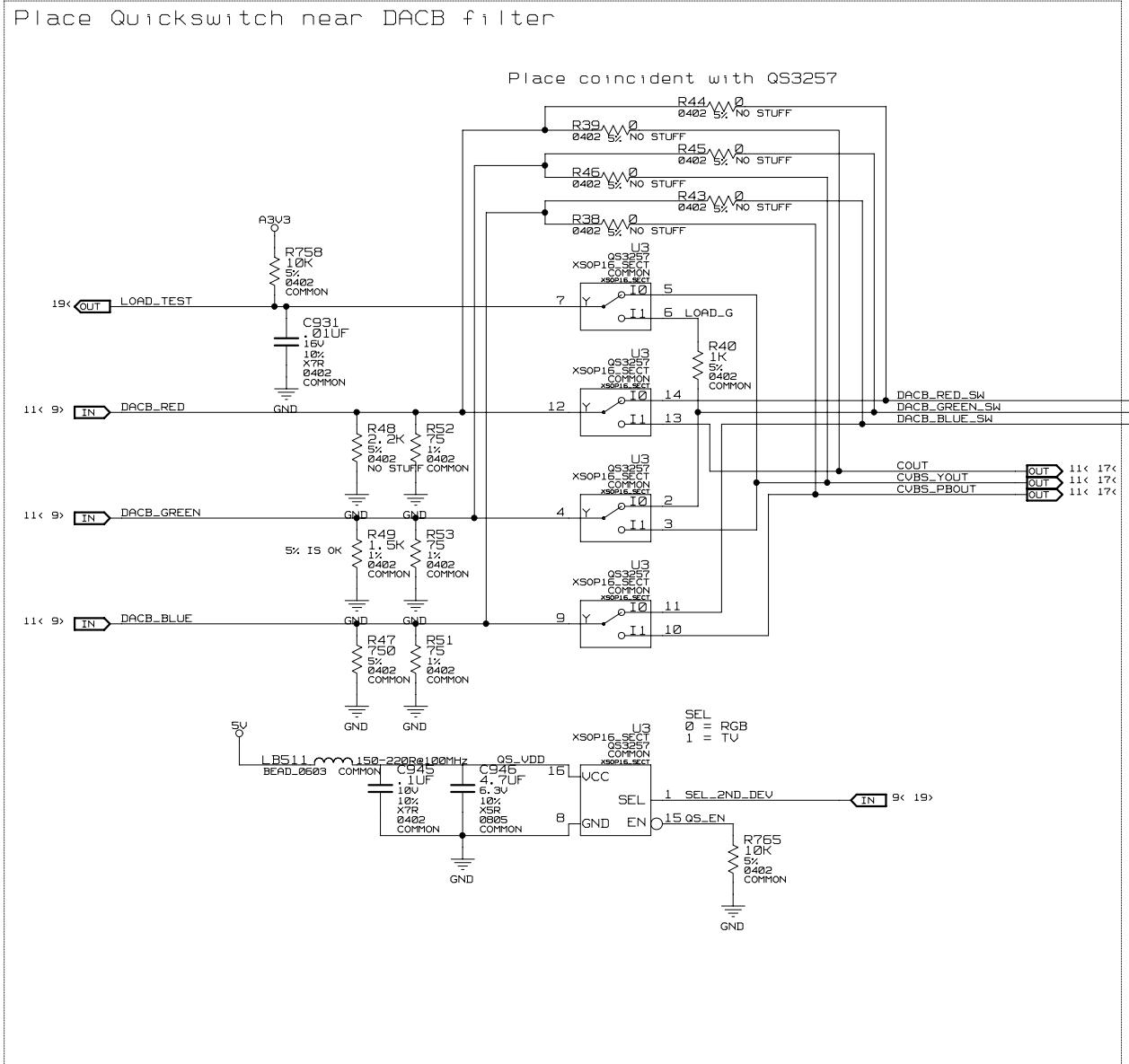
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ID p126\_a05\_sch PAGE 10 OF 32  
NAME 140-10126-000-005-X12 DATE JAN-14-2003

### 3. c. DACB Output

#### RGB-FILTER

#### DACB output

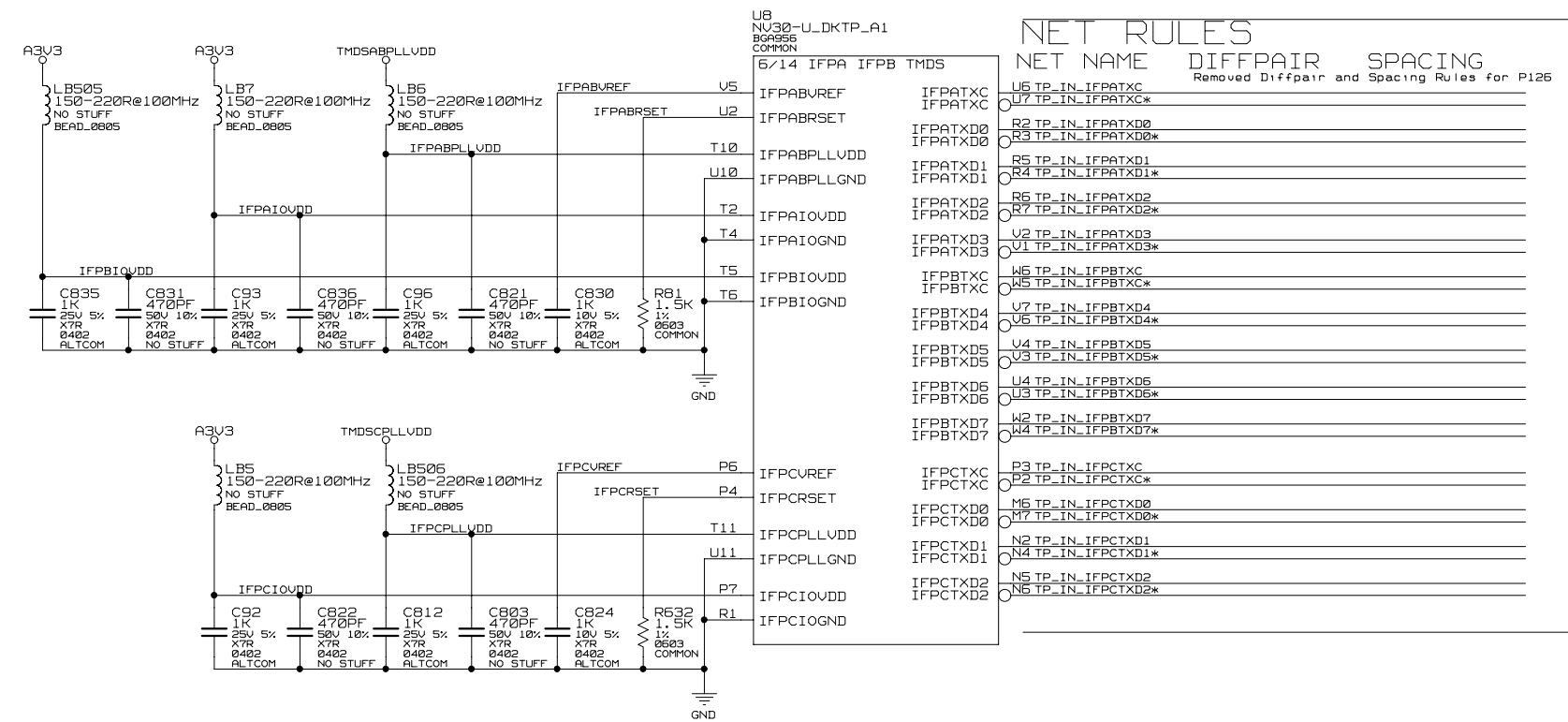
##### Quickswitch for DACB



NET RULES	
NET	SPACING
11< 9> IN DACB_RED	20MIL
11< 9> IN DACB_GREEN	20MIL
11< 9> IN DACB_BLUE	20MIL
11< 9> IN DACB_RED_SW	20MIL
11< 9> IN DACB_GREEN_SW	20MIL
11< 9> IN DACB_BLUE_SW	20MIL
15< 11> IN DACB_RED_C	20MIL
15< 11> IN DACB_GREEN_C	20MIL
15< 11> IN DACB_BLUE_C	20MIL
17< 11> OUT COUT	20MIL
17< 11> OUT CVBS_YOUT	20MIL
17< 11> OUT CVBS_POUT	20MIL
IN 05_UDD	12MIL_TRACE
IN 5V	

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## 4. a. Internal TMDS



IFP Power should have alternate pull-down to GND when not used

### NET RULES

NET	PHYSICAL	VOLTAGE
IFPABPLLVDD	12MIL_TRACE	3.3V
IFPABIOVDD	12MIL_TRACE	3.3V
IFPABUREF	10MIL_TRACE	3.3V
IFPABRSET	10MIL_TRACE	3.3V
IFPABPLLVDD	12MIL_TRACE	3.3V
IFPABIOVDD	12MIL_TRACE	3.3V
IFPCUREF	12MIL_TRACE	3.3V
IFPCRSET	10MIL_TRACE	3.3V

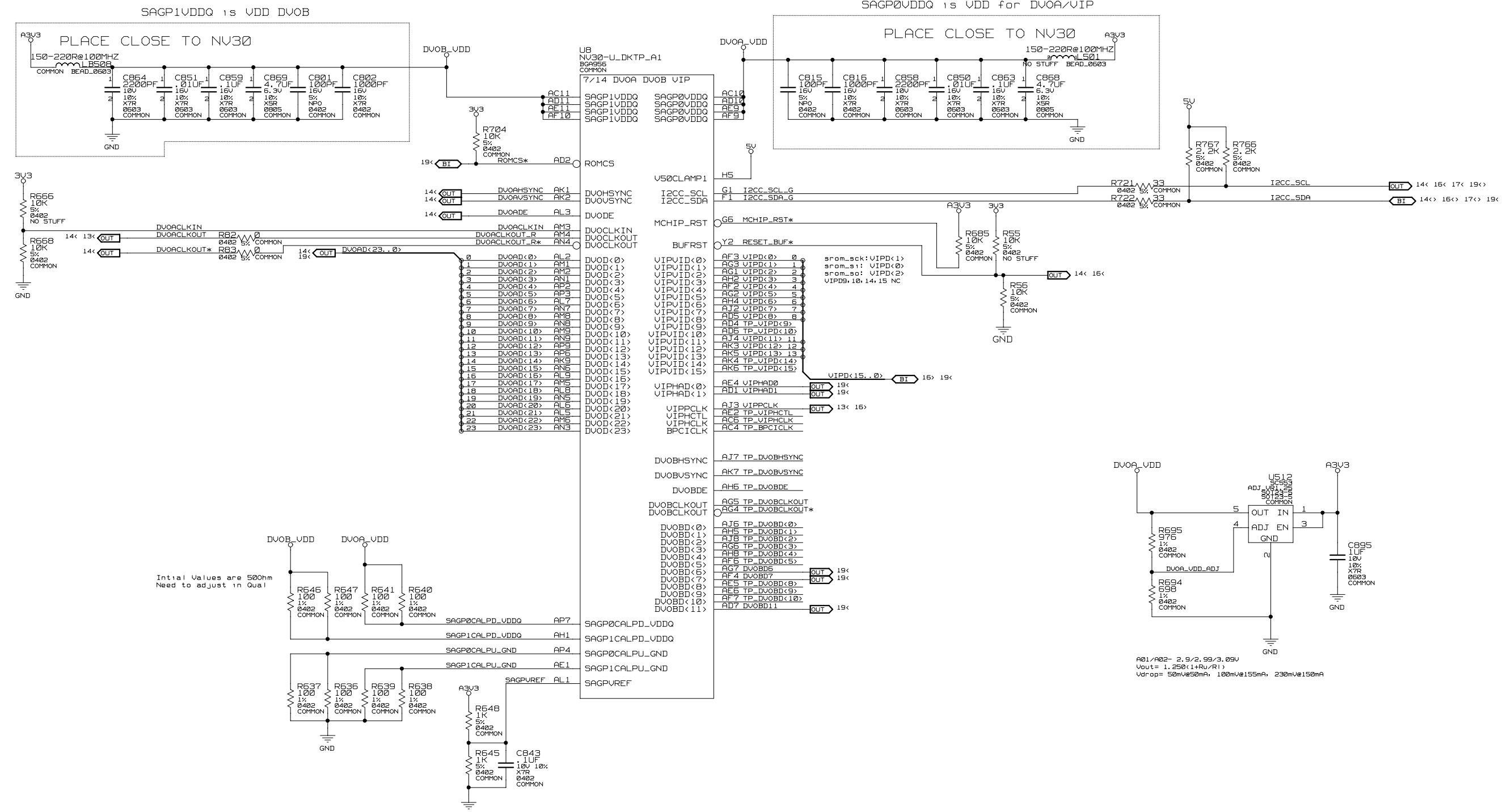
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DETAIL	DRAWING DETAIL
CONTINUED...	

# 4. b. DVO/VIP Interface

## NET RULES

NET	PHYSICAL	SPACING
SAGP0CALPD_VDDQ	12MIL_TRACE	20MIL
SAGP1CALPD_VDDQ	12MIL_TRACE	20MIL
SAGP0CALPU_GND	12MIL_TRACE	20MIL
SAGP1CALPU_GND	12MIL_TRACE	20MIL
DVOACLKOUT		20MIL
DVOACLKOUT_R		20MIL
VIPCLK		20MIL



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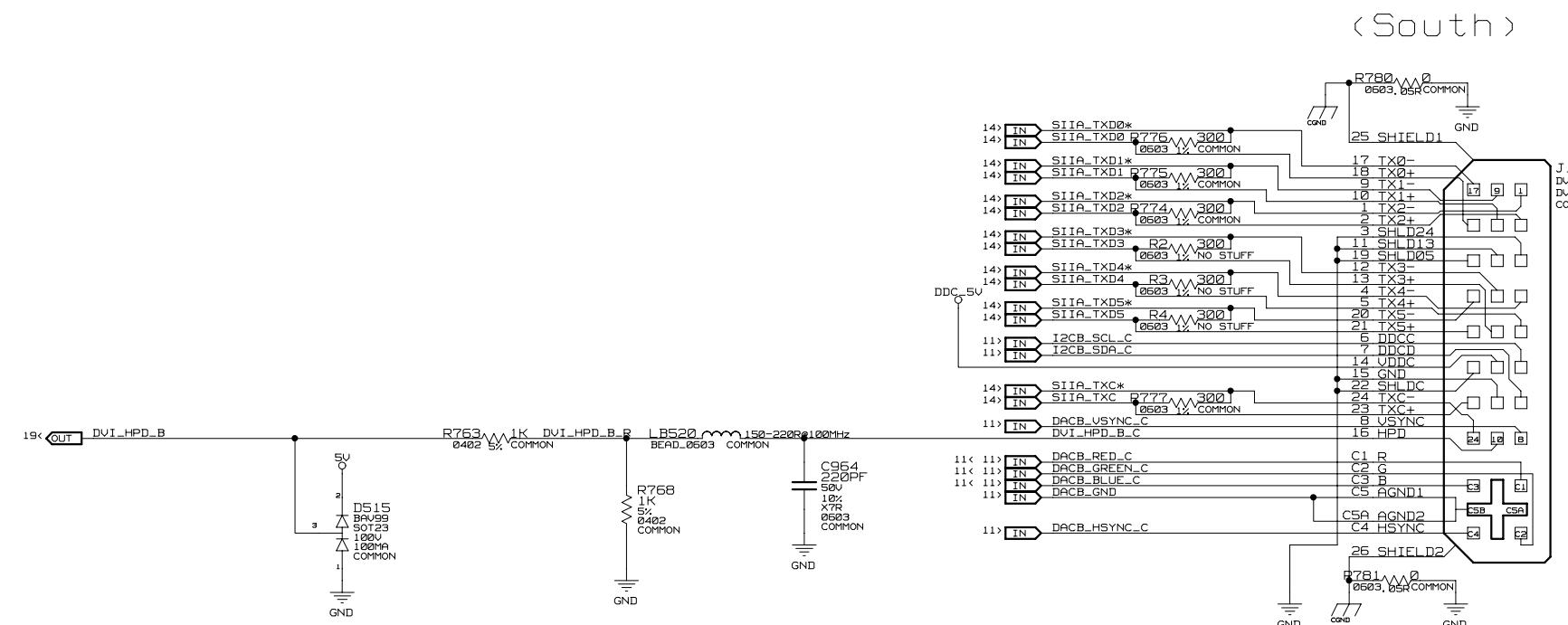
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## 4. e. DVI-I (TMDS) Connector



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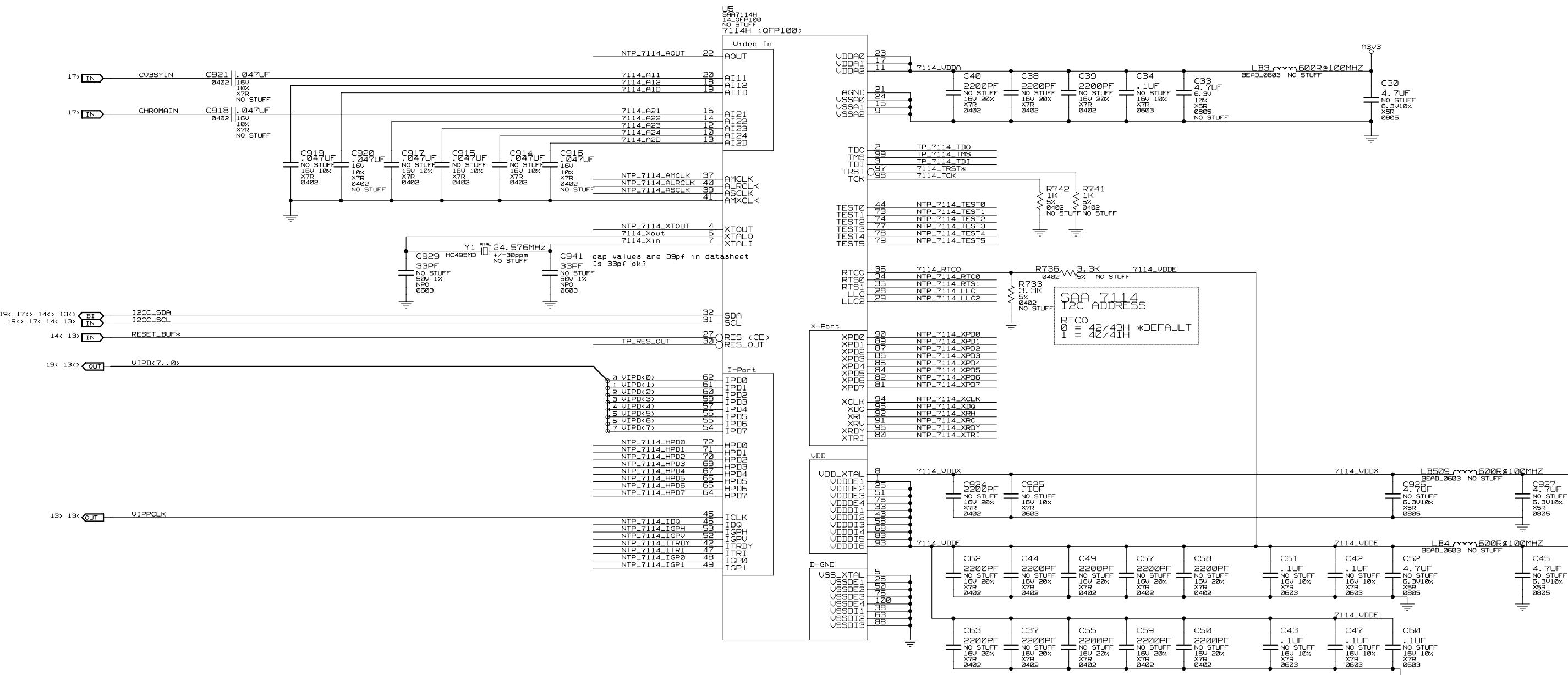
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DETAIL	DRAWING DETAIL
CONTINUED...	
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# 5.a. Video Capture

## NET RULES

NET	PHYSICAL	VOLTAGE
7114_VDDA	12MIL_TRACE	3.3V
7114_VDDX	12MIL_TRACE	2.8V
7114_VDDE	12MIL_TRACE	3.3V

## VIDEO CAPTURE



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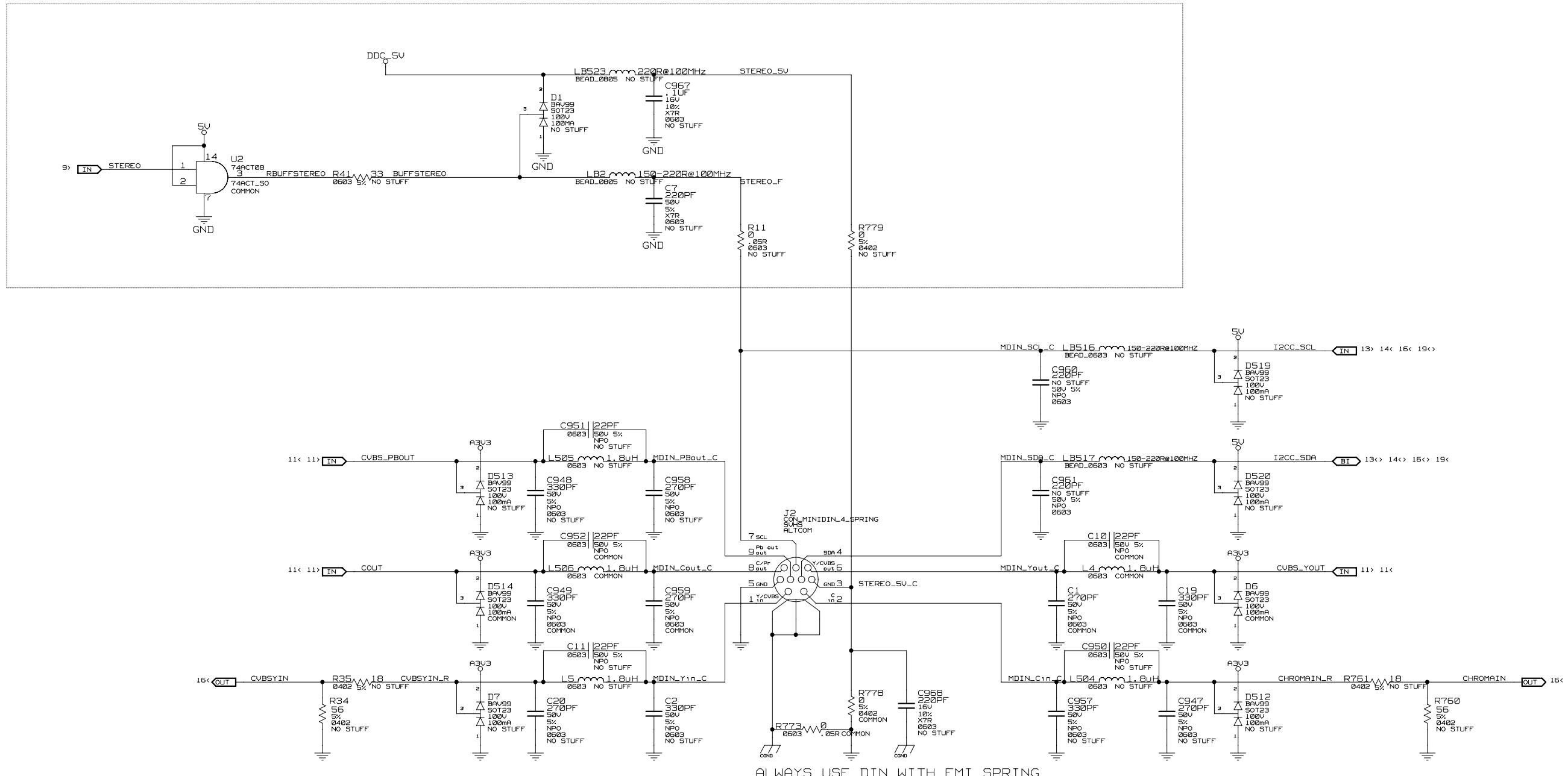
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# 5. b. DIN Connector (TV, VIVO, STEREO)

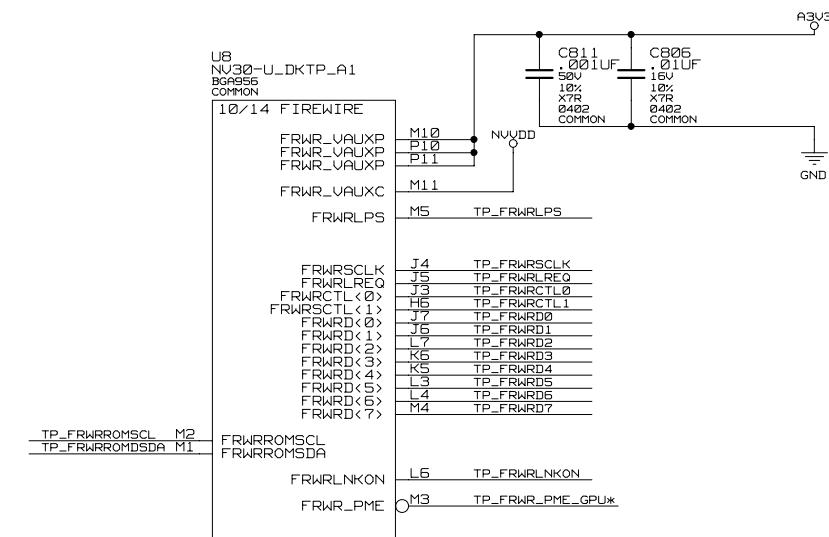
STEREO 3D



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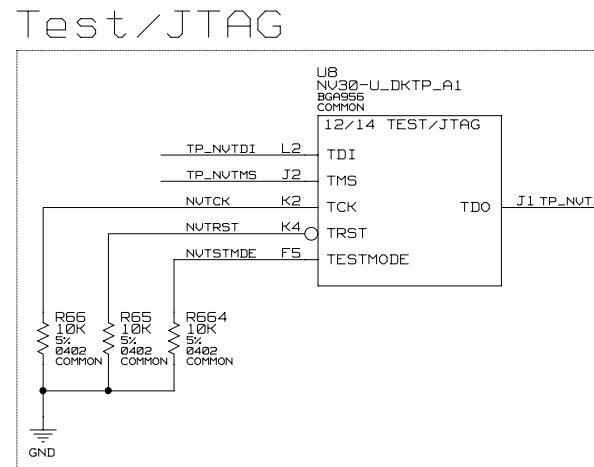
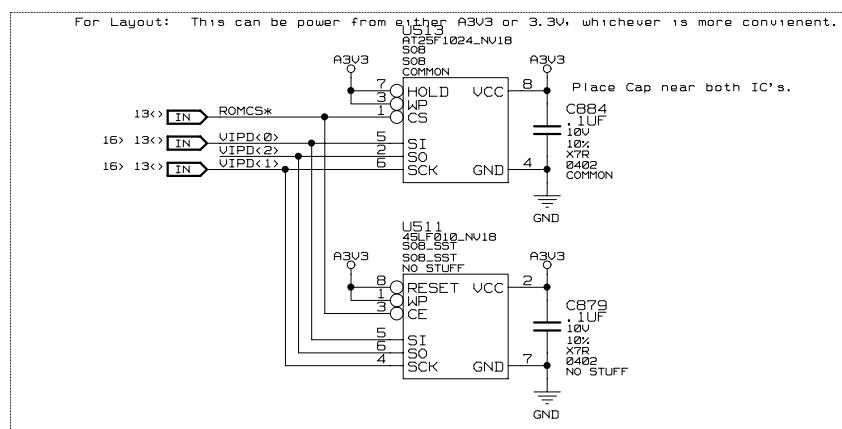
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## 6. a. Firewire

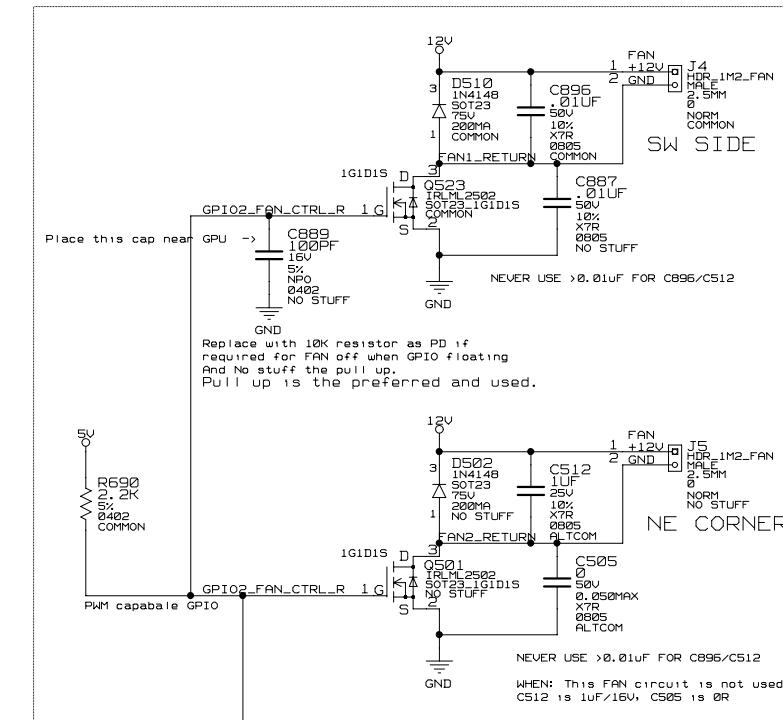


## 7. a. BIOS, Straps, Misc

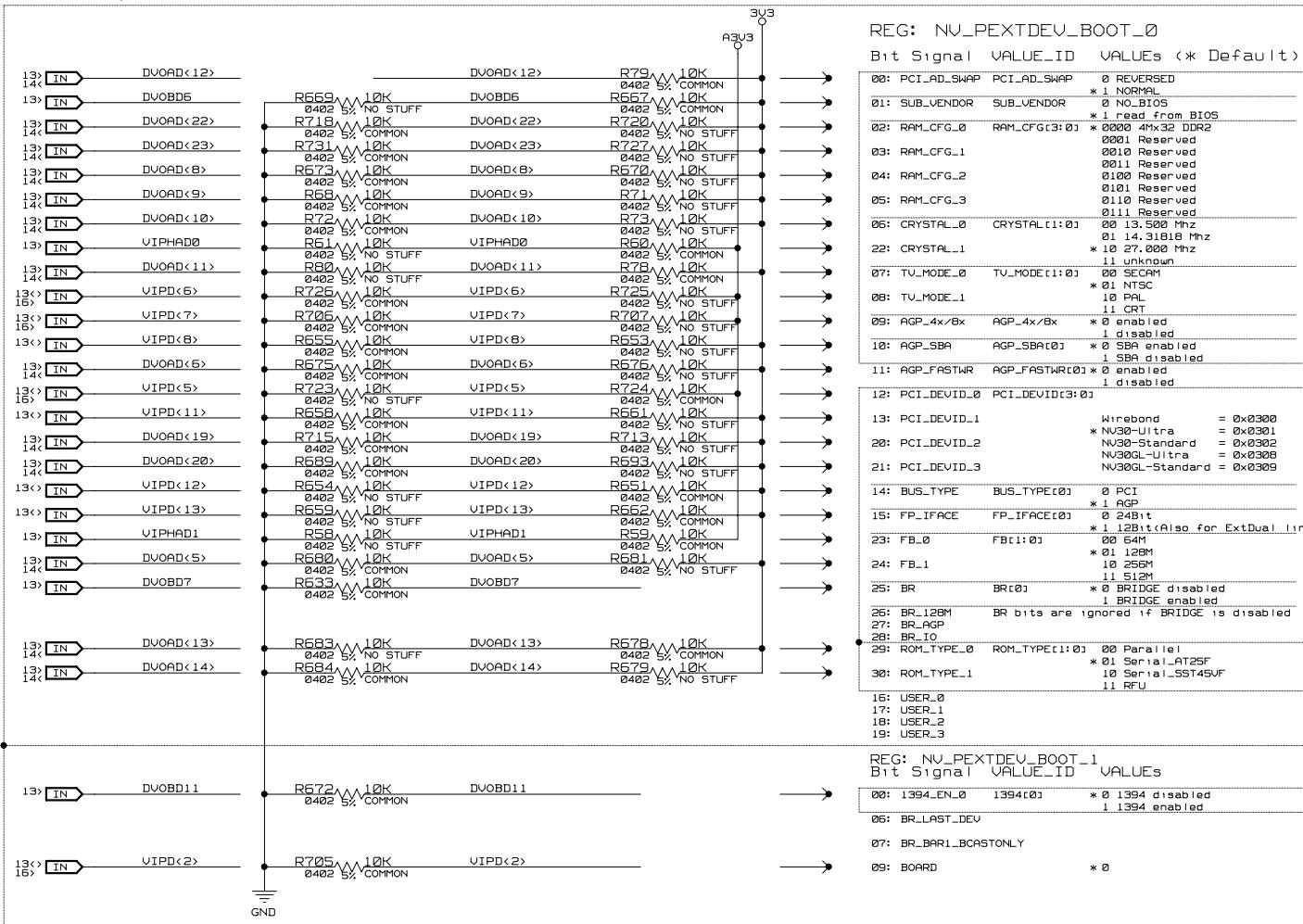
BIOS <serial>



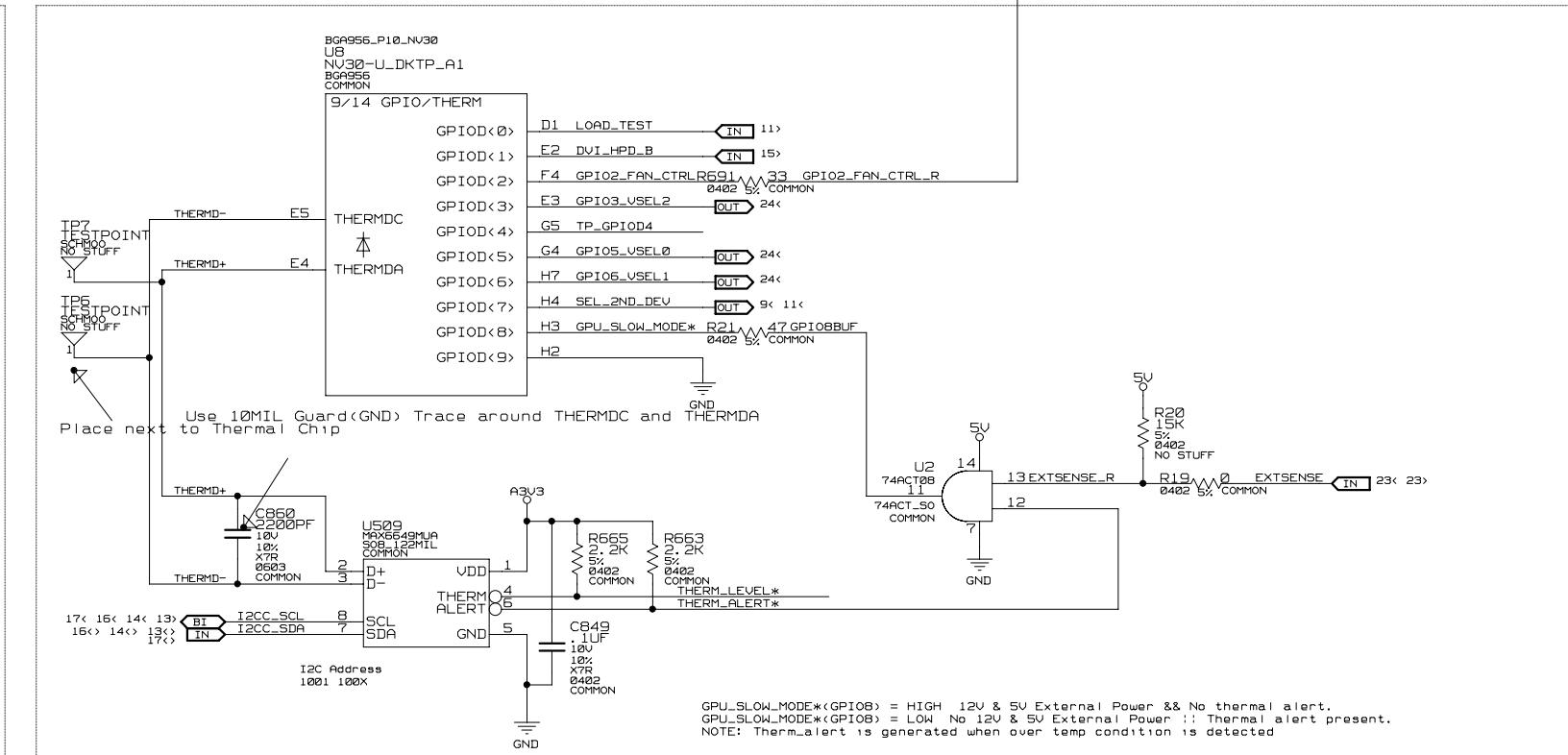
Fan1/Fan2



## Straps



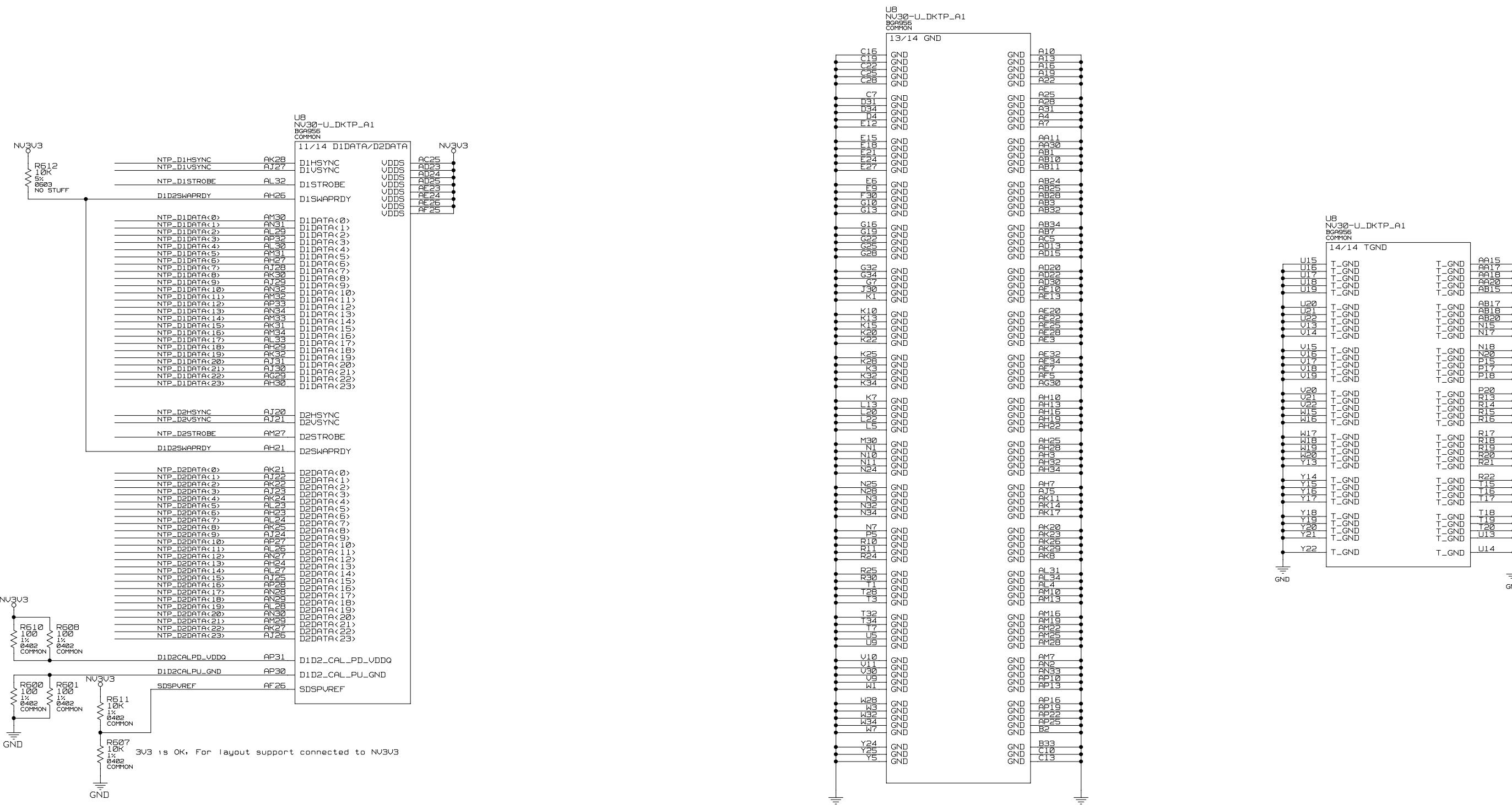
GPIO's, Fan Control, Thermal Sense & EXT Power Sense



NET RULES			
	NET	PHYSICAL	
IN	THERMDC	10MIL_TRACE	
IN	THERMDA	10MIL_TRACE	
IN	FAN1_RETURN	16MIL_TRACE	
IN	FAN2_RETURN	16MIL_TRACE	
NET		SPACING	
IN	GPIO2_FAN_CTRL	20MIL	
IN	GPIO2_FAN_CTRL_R	20MIL	

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## 8. a. GND, Thermal GND and Misc.



NET RULES		NET	PHYSICAL	SPACING
	D1D2CALPD_VDDQ		12MIL_TRACE	20MIL
	D1D2CALPU_GND		12MIL_TRACE	20MIL

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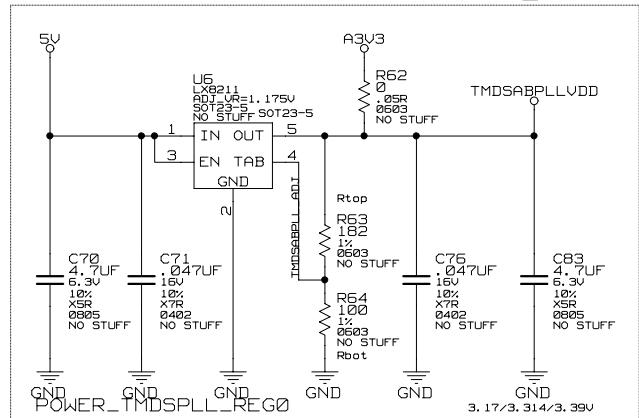
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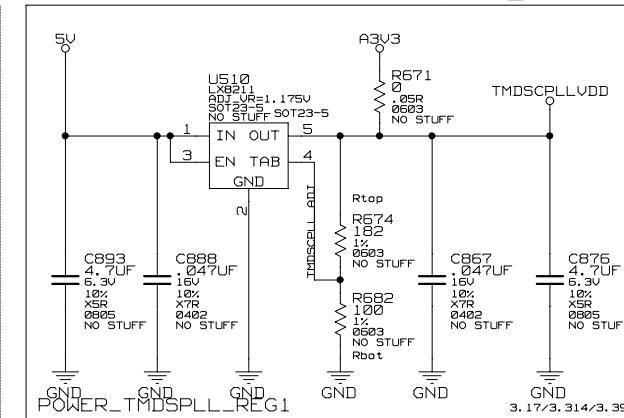


# 9.a. Power Supply I: TMDS/A3V3/FBVDD

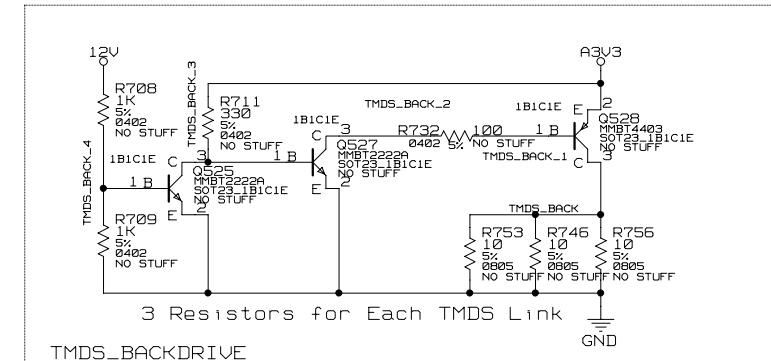
TMDS AB PLL Supply



TMDS C PLL Supply



TMDS backdrive prevention



## NET RULES

NET	PHYSICAL	VOLTAGE
A3V3_O	12MIL_TRACE	3.3V
FBUTT_O	FBUTT	12MIL_TRACE
FBUDDO_O	FBUDDO	12MIL_TRACE
FBUDD_O	FBUDD	12MIL_TRACE
NUVDD_O	NUVDD	12MIL_TRACE
5V_O	5V	12MIL_TRACE
12V_O	12V	12MIL_TRACE
3V3_O	3V3	12MIL_TRACE
AGPUDDO	GND	12MIL_TRACE
DDC_5V_O	DDC_5V	12MIL_TRACE
TMDSABPLLVDD_O	TMDSABPLLVDD	12MIL_TRACE
TMDSCLLVDD_O	TMDSCLLVDD	12MIL_TRACE
TMDSABPLL_ADJ_O	TMDSABPLL_ADJ	10MIL_TRACE
TMDSCLL_ADJ_O	TMDSCLL_ADJ	10MIL_TRACE
6529_SW_12V	10MIL_TRACE	12V
6529_SW	16MIL_TRACE	5V
3V3_6529	16MIL_TRACE	3.3V
6529_SW_COMP	10MIL_TRACE	3.3V
6529_SW_FB	10MIL_TRACE	2.5V
6529_SW_COMP3_FB	10MIL_TRACE	3.3V
6529_SW_SN	12MIL_TRACE	3.3V
6529_SW_DRHI	24MIL_TRACE	12V
6529_SW_DRLO	24MIL_TRACE	12V
6529_SW_GL	24MIL_TRACE	12V
6529_SW_GATE	16MIL_TRACE	5V
6529_SW_GATE_R	16MIL_TRACE	5V
6529_SW_LFB	10MIL_TRACE	2.5V
6529_GND_F	10MIL_TRACE	3.3V
SU_LDO_IN	16MIL_TRACE	5V
6529_L_COMP	10MIL_TRACE	3.3V
6529_L_F	10MIL_TRACE	3.3V
TMDS_BACK	12MIL_TRACE	3.3V
TMDS_BACK_1	12MIL_TRACE	3.3V
TMDS_BACK_2	12MIL_TRACE	3.3V
TMDS_BACK_3	12MIL_TRACE	3.3V
TMDS_BACK_4	12MIL_TRACE	3.3V

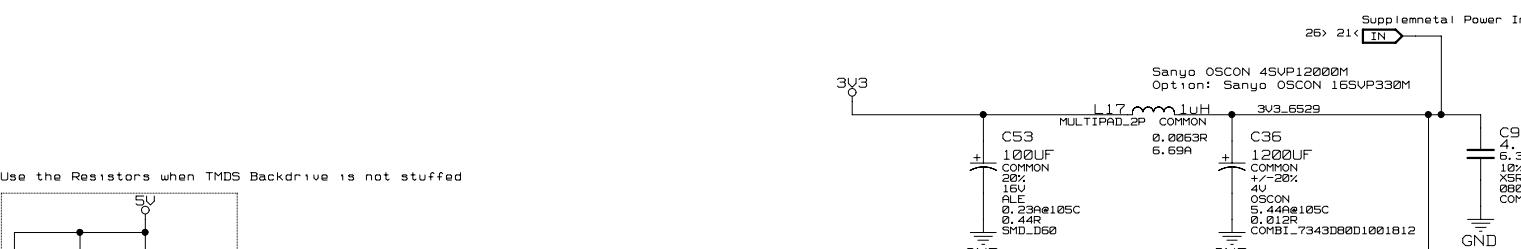
$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

$$3.31V = 1.175V * (1 + (100/182))$$

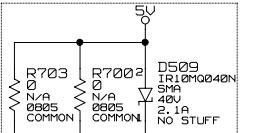
$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

$$3.31V = 1.175V * (1 + (100/182))$$

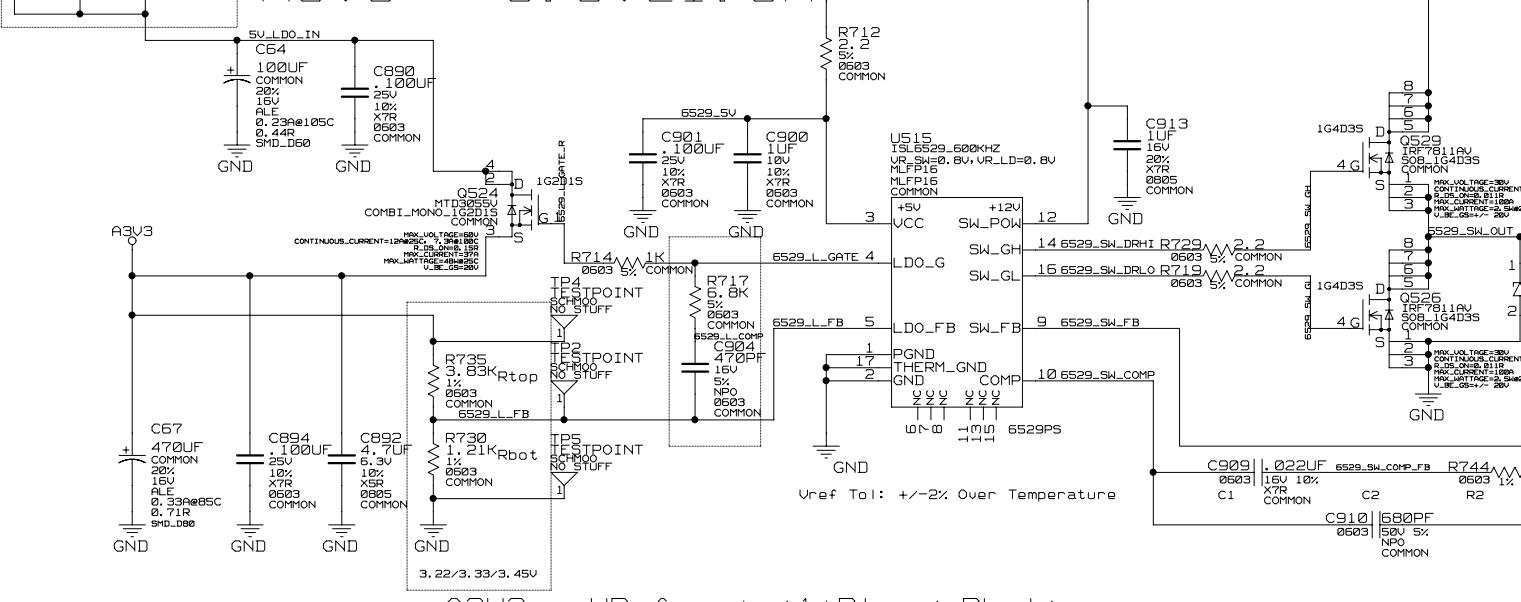
FBVDD-SWITCHER / A3V3-LDO CONTROLLER ISL6529



Use the Resistors when TMDS Backdrive is not stuffed



$$A3V3 = 3.3V @ 1.5A$$



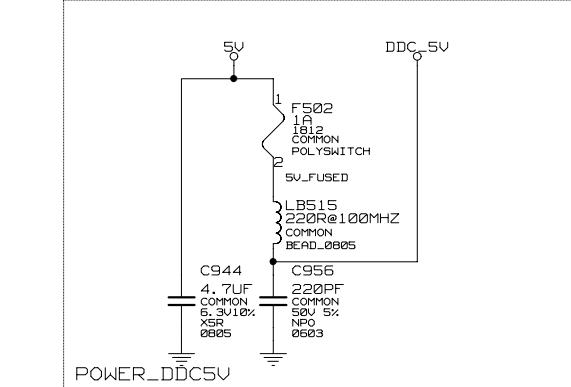
NOTE

SV external Supplemental power to 3.3V is for FBVDD. See other page  
For voltage Shmoo, the Rtop resistor value should not be changed more than 10%  
Please contact design team to check the compensation circuit analysis

$$A3V3 = V_{Ref} * (1 + R_{top}/R_{bot})$$

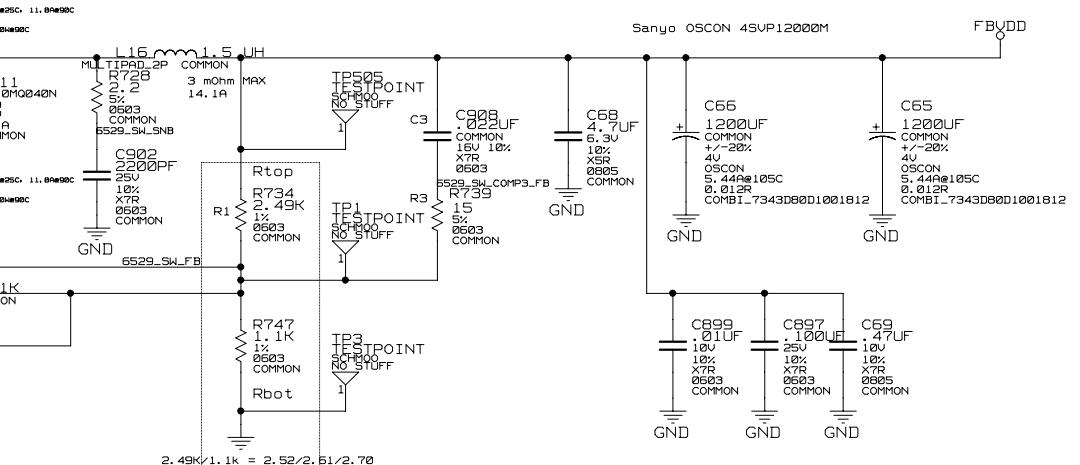
$$3.3V = 0.800V * (1 + 3.83k/1.21k)$$

DDC 5V



O/P is stable ~3ms min after rail stable

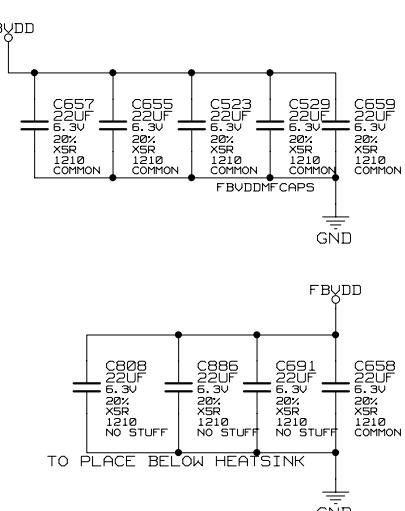
FBVDD = 2.5V@10A



$$FBVDD = V_{Ref} * (1 + R_{top}/R_{bot})$$

$$2.6V = 0.800V * (1 + 2.49k/1.1k)$$

SPREAD ADDITIONAL BULK OVER THE BOARD



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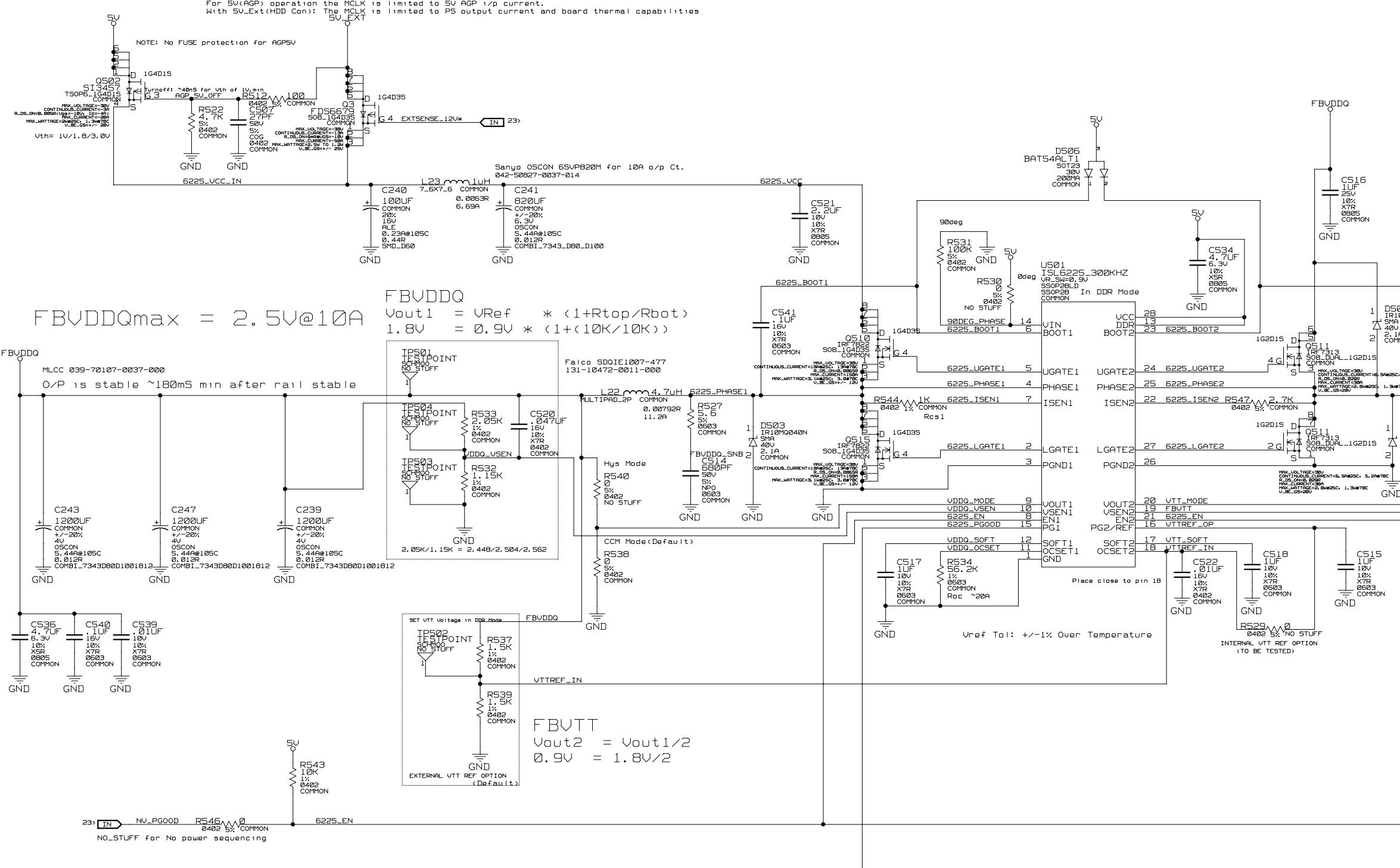
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# 9.b. Power Supply II: FBVDDQ/FBUTT

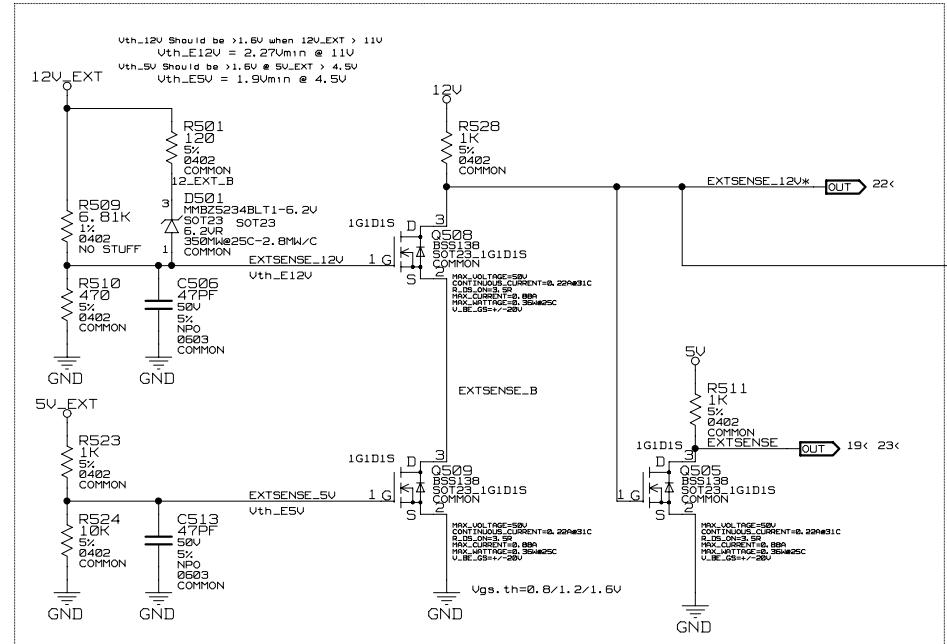
**NOTE:**  
For 5V(AGP) operation the MCLK is limited to 5V AGP 1/p current.  
With 5V\_Ext<HDD Con>: The MCLK is limited to PS output current and board thermal capabilities



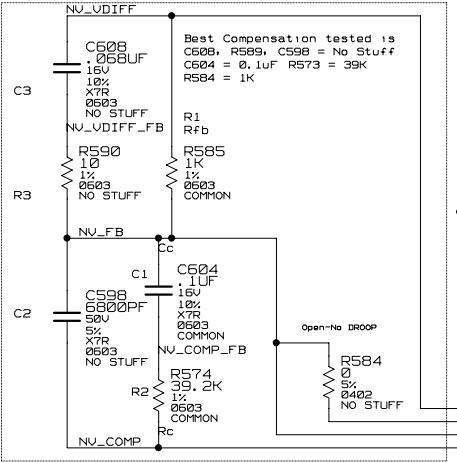
## 9. c. Power Supply III: NUVDD

For 12V(AGP) operation the NVCLK is limited to 12V AGP 1/p current.  
With 12V\_Ext(HDD Con): The NVCLK is limited PS output current and board thermal capability.

## External Power Sense

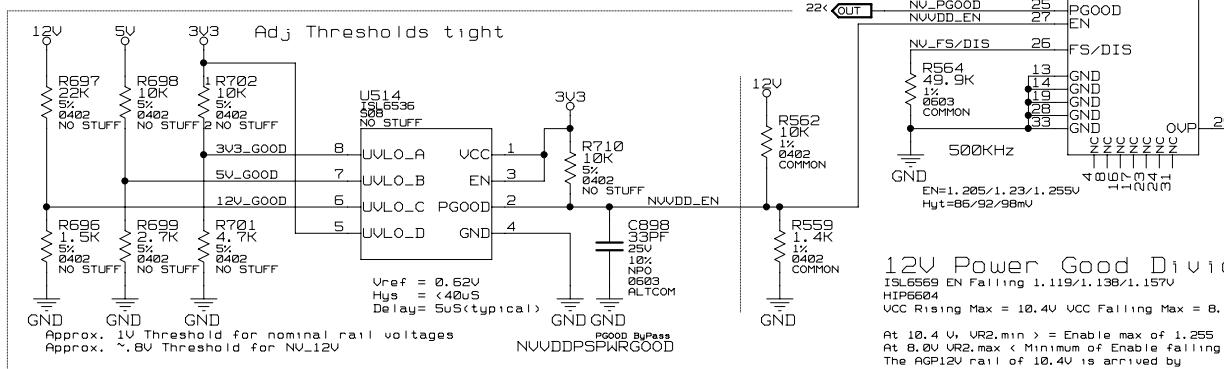


# Comp Network



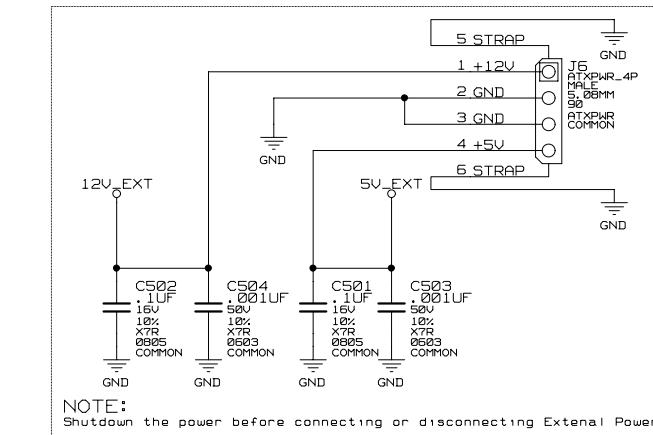
**NUVDD** Voltage Selection  
Dynamic VID over Temperature =  $\frac{25mV}{200} \times \frac{1}{Freq}$

Power Good



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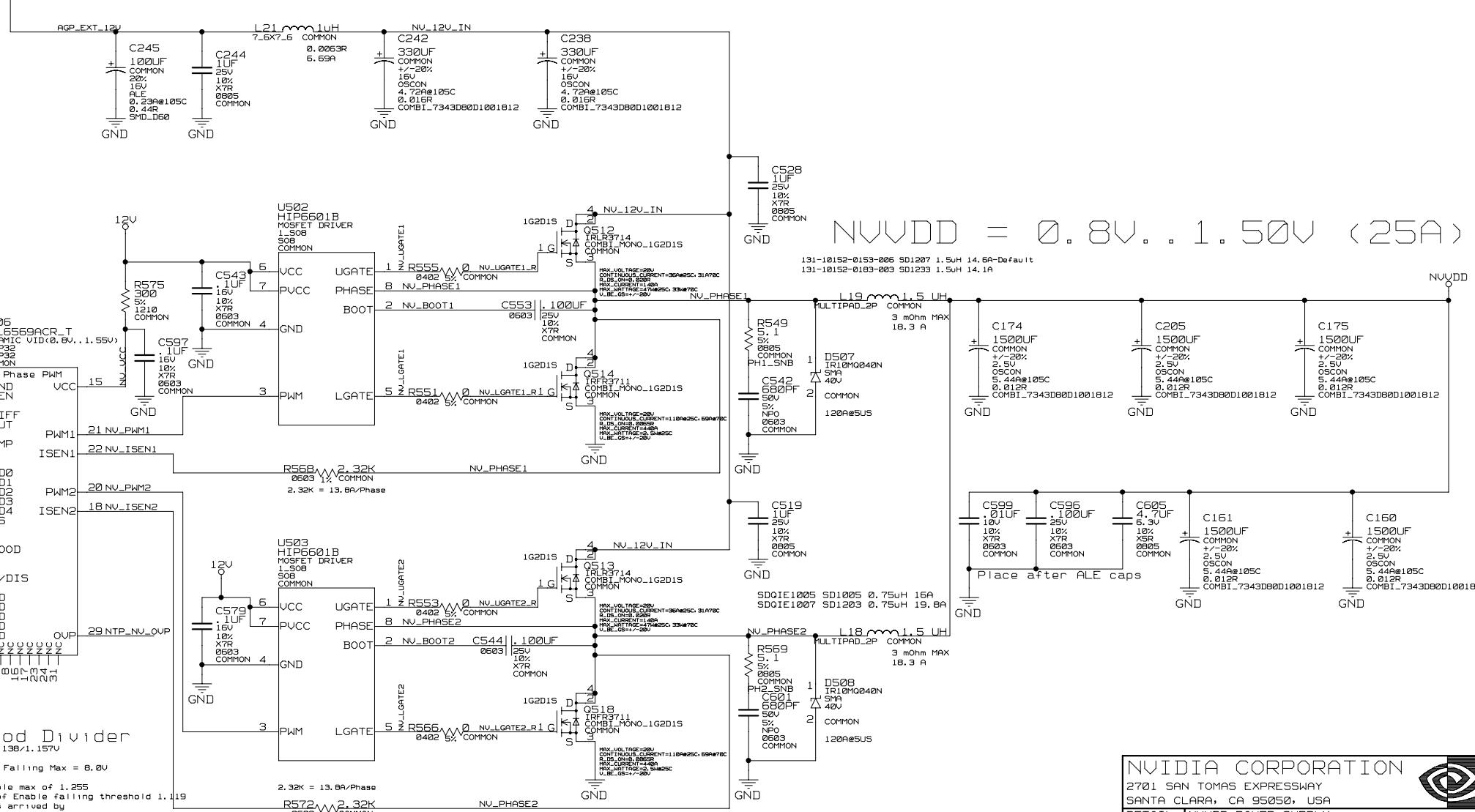
## External Power Connector



**NOTE:** Shutdown the power before connecting or disconnecting External Power

## NET RULES

NET	DIFFPAIR	PHYSICAL
NU_USEN	NU_Rem_Sense	10MIL_TRACE
NU_RGND	NU_Rem_Sense	10MIL_TRACE



<sup>N</sup> NUVDD = 0.8V..1.50V (25A)

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DETAIL		NOVOD POWER SUPPLY	
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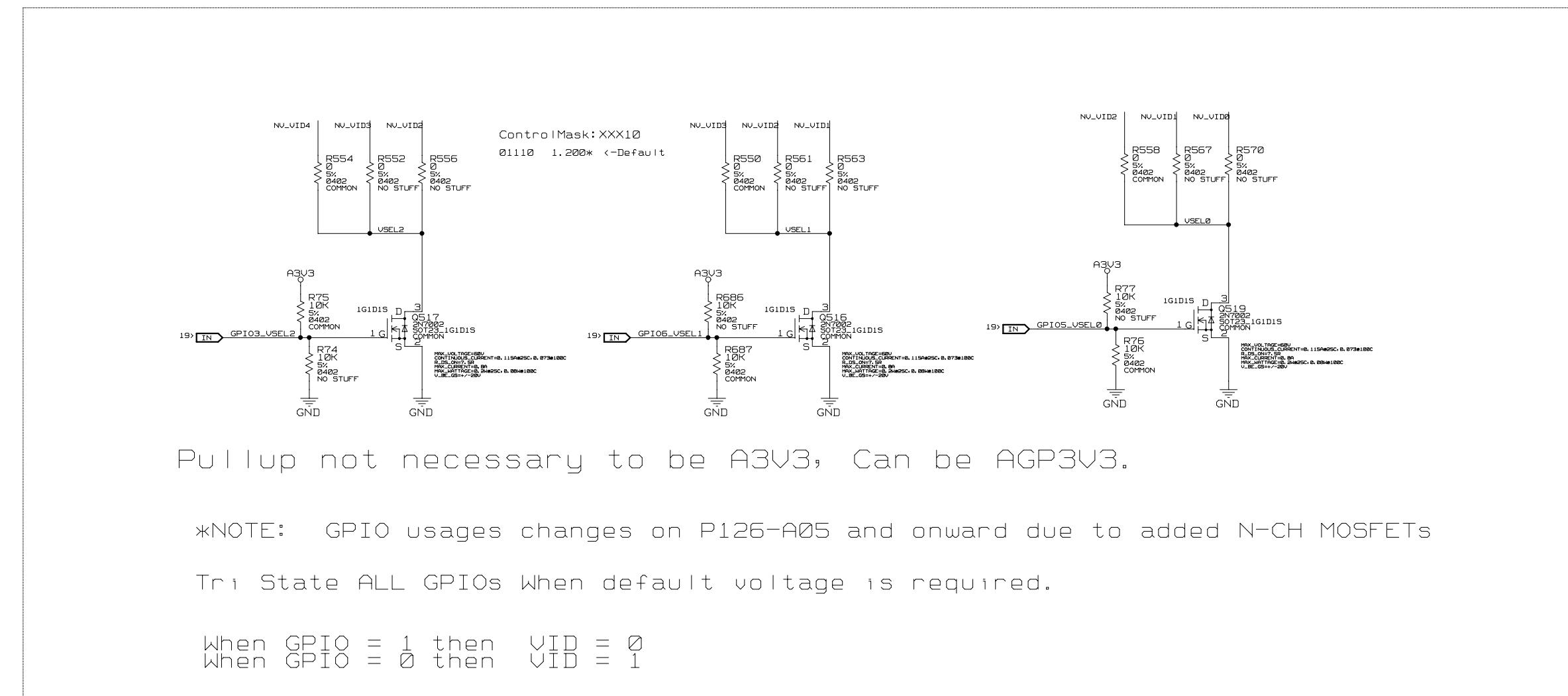
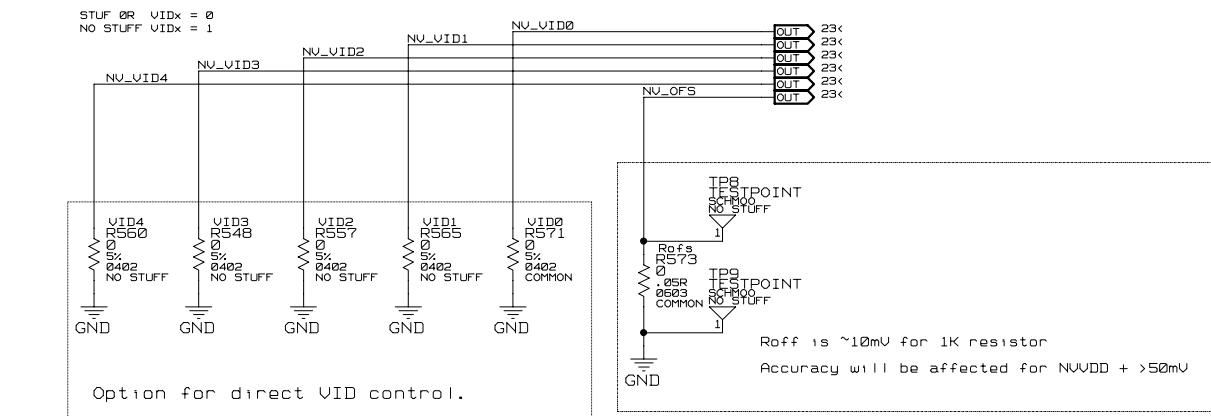
## 9. d. Power Supply III: NUVDD Voltage Select Options

ISL6569  
5-Bit VID Tab I

WID[4:0]	VOLTAGE	WID[4:0]	VOLTAGE	
00000	1.550	10000	1.150	
00001	1.525	10001	1.125	
00010	1.500*	10010	1.100*	
00011	1.475	10011	1.075	
00100	1.450	10100	1.050	
00101	1.425	10101	1.025	
00110	1.400*	10110	1.000*	
00111	1.375	10111	0.975	
01000	1.350	11000	0.950	
01001	1.325	11001	0.925	
01010	1.300*	11010	0.900*	
01011	1.275	11011	0.875	
01100	1.250	11100	0.850	
01101	1.225	11101	0.825	
Default->	01110	1.200*	11110	0.800*
	01111	1.175	11111	Shutdown

Table is with Roffset=  
# SELECTABLE

\* SELECTABLE



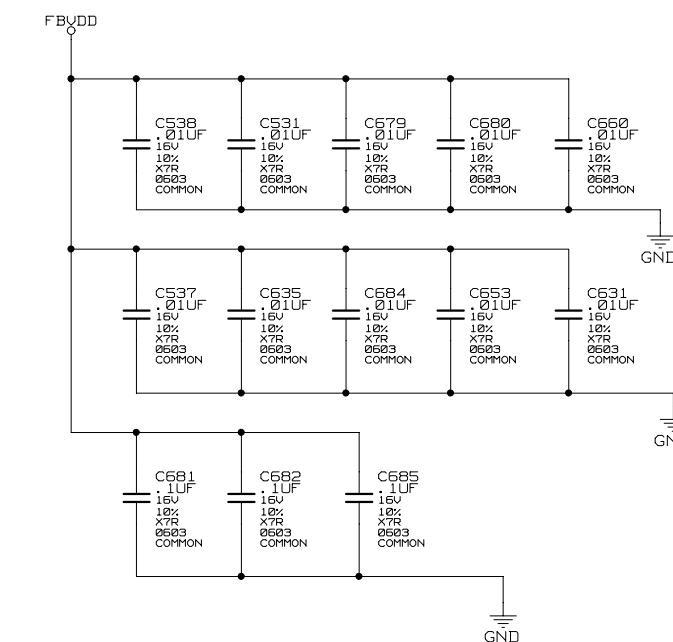
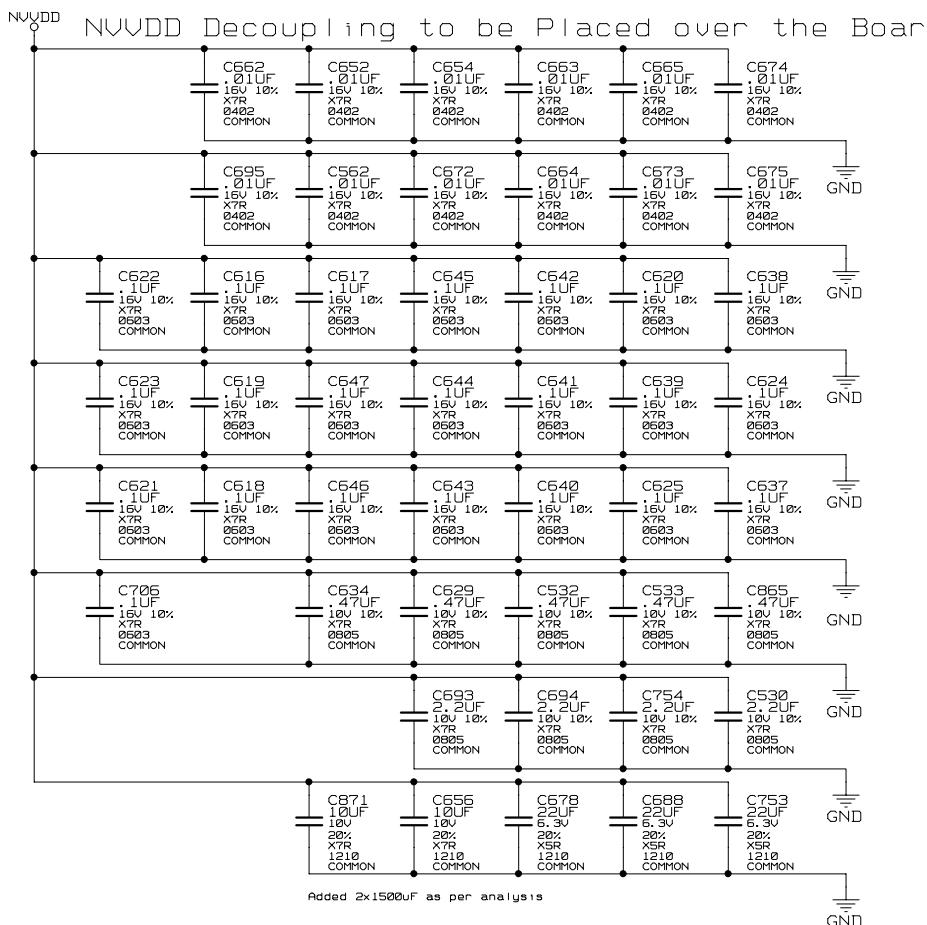
Pullup not necessary to be A3V3, Can be AGP3V3

\*NOTE: GPIO usages changes on P126-A05 and onward due to added N-CH MOSFETs

Tri State ALL GPIOs When default voltage is required

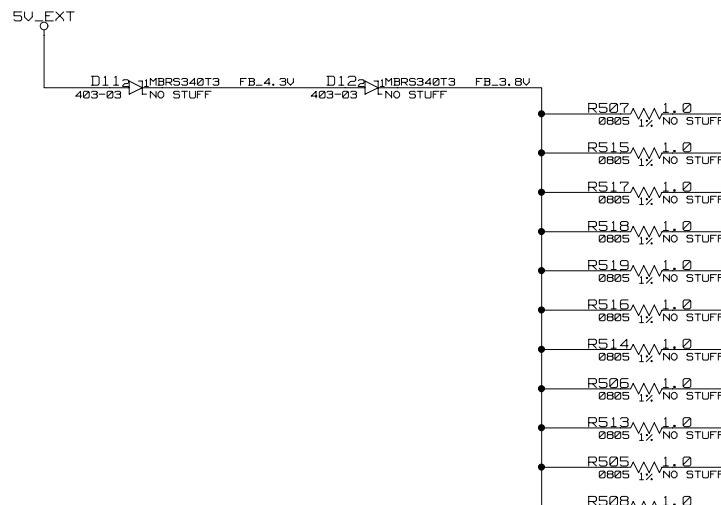
When GPIO = 1 then VID =

## 9. E. Additional Decoupling



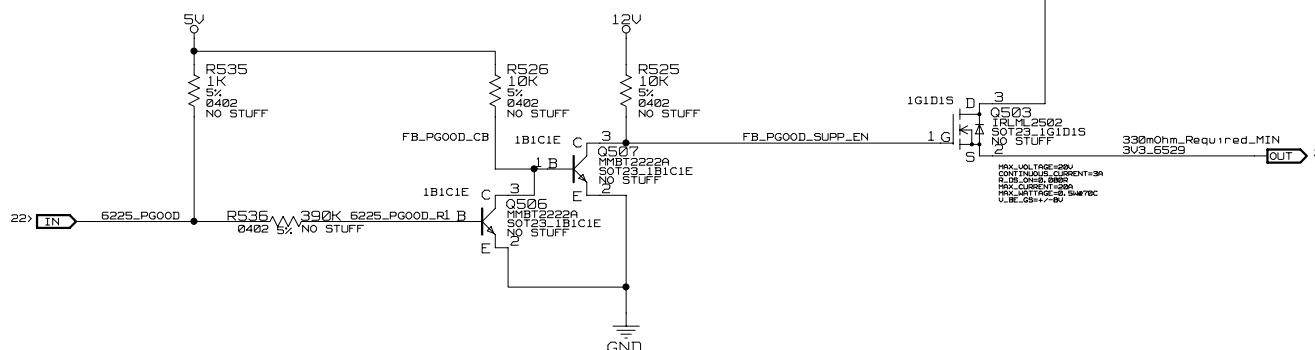
9. f. FBVDD Current Supplement & NV3V3

NEVER USE THIS CIRCUIT



NEED 1ohm, 10nos/0805  
NEED 330mOhm trace resistance

Approx 2A To be decided

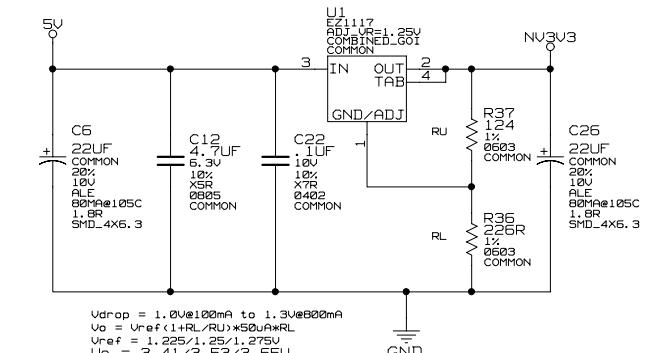


This circuit will be enabled after 180mS minimum after NUVDD.



For Better Drive Bias to Frame Buffer

3.5V, 500mA



$V_{drop} = 1.0V$  @  $100mA$  to  $1.3V$  @  $800mA$   
 $V_o = V_{ref} < 1 + RL/RU \cdot 50\mu A \cdot RL$   
 $V_{ref} = 1.225 / 1.25 / 1.275V$   
 $V_o = 3.41 / 3.53 / 3.65V$

## 10. a. Mechanical

1  
151-10000-0021-000-STDUVG-A-DIN-DVI  
151-10000-5004-000-DualWide-VGA-DIN-DVI2  
BKT1  
DS15HD, MDIN, DVI, NO TAB  
PART NO: BRKT\_DVI\_BDING\_CDB1S  
ALTCOM3  
MECH. MOUNT VGA CONNECTOR4  
FootPrint: BRKT\_DVI\_BDING\_CDB1S5  
FX FLOW(NUTM2) FANSINK ASSY KIT  
095-20000-0001-0003  
MEC1  
HEX-JACK SCREW  
STD COMMON  
  
MEC2  
HEX-JACK SCREW  
STD COMMON  
  
MEC3  
HEX-JACK SCREW  
STD COMMON  
  
MEC4  
HEX-JACK SCREW  
STD COMMON  
3  
2 for VGA  
2 for DVI-I4  
SCREW PARTS- 155-00003-0000-000

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NVIDIA CORPORATION  
2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA  
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DETAIL DRAWING DETAIL  
CONTINUED...

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NAME	140-10126-000-005-X12	DATE	JAN-14-2003

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1	SEL_2ND_DEV 9< 11< 19> SIIA_AVCC 14< SIIA_TXC 14> 15< SIIA_TXC* 14> 15< SIIA_TXD0 14> 15< SIIA_TXD0* 14> 15< SIIA_TXD1 14> 15< SIIA_TXD1* 14> 15< SIIA_TXD2 14> 15< SIIA_TXD2* 14> 15< SIIA_TXD3 14> 15< SIIA_TXD3* 14> 15< SIIA_TXD4 14> 15< SIIA_TXD4* 14> 15< SIIA_TXD5 14> 15< SIIA_TXD5* 14> 15< SIIA_VCC 14< STEREO 9> 17< THERM1A 19< THERM1C 19< TMDSBPLL_ADJ 21< TMDSCLL_ADJ 21< TMDS_BACK 21< TMDS_BACK_1 21< TMDS_BACK_2 21< TMDS_BACK_3 21< TMDS_BACK_4 21< TV_RSET_SEL 9< VDDQ_OSET 22< VDDQ_USEN 22< VIPD<0> 13<> 16> 19< VIPD<7..0> 13<> 16> 19< VIPD<15..0> 13<> 16> 19< VIPD<1> 13<> 16> 19< VIPD<2> 13<> 16> 19< VIPD<3> 13<> 16> VIPD<4> 13<> 16> VIPD<5> 13<> 16> 19< VIPD<6> 13<> 16> 19< VIPD<7> 13<> 16> 19< VIPD<8> 13<> 19< VIPD<11> 13<> 19< VIPD<12> 13<> 19< VIPD<13> 13<> 19< VIPHD0 13> 19< VIPHD1 13> 19< VIPPCLK 13> 13> 16> UTTREF_IN 22< UTT_SNB 22< XTALIN 9< XTALOUT 9<	1
2		2
3		3
4		4
5		5

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\*\*\* Part Cross-Reference for the entire design \*\*\*

BKT1 BRACKET 27  
 C1 C 17  
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 C3 C 11  
 C4 C 11  
 C5 C 11  
 C6 C\_POL 26  
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A B C D E F G H

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	C818 C 8	C931 C 11	L82 L 17	R49 R 11	R563 R 24
	C819 C 8	C932 C 14	L83 L 16	R50 R 14	R564 R 23
	C820 C 8	C933 C 14	L84 L 16	R51 R 11	R565 R 24
	C821 C 12	C934 C 14	L85 L 12	R52 R 11	R566 R 23
	C822 C 12	C935 C 14	L86 L 12	R53 R 11	R567 R 24
	C823 C 9	C936 C 14	L87 L 12	R54 R 14	R568 R 23
	C824 C 12	C937 C 14	L8801 L 3	R55 R 13	R569 R 23
	C825 C 8	C938 C 14	L8802 L 4	R56 R 13	R570 R 24
	C826 C 8	C939 C 14	L8803 L 9	R57 R 14	R571 R 24
	C827 C 8	C940 C 14	L8804 L 9	R58 R 19	R572 R 23
	C828 C 8	C941 C 16	L8805 L 12	R59 R 19	R573 R 24
	C829 C 9	C942 C 16	L8806 L 12	R60 R 19	R574 R 23
	C830 C 12	C943 C 11	L8807 L 9	R61 R 19	R575 R 23
	C831 C 12	C944 C 21	L8808 L 13	R62 R 21	R576 R 23
	C832 C 6	C945 C 11	L8809 L 16	R63 R 21	R577 R 23
	C833 C 8	C946 C 11	L8810 L 14	R64 R 21	R578 R 23
	C834 C 8	C947 C 17	L8811 L 11	R65 R 19	R579 R 23
	C835 C 12	C948 C 17	L8812 L 10	R66 R 19	R580 R 5
	C836 C 12	C949 C 17	L8813 L 10	R67 R 3	R581 R 7
	C837 C 9	C950 C 17	L8814 L 10	R68 R 19	R582 R 5
	C838 C 9	C951 C 17	L8815 L 21	R69 R 6	R583 R 7
	C839 C 8	C952 C 17	L8816 L 17	R70 R 6	R584 R 23
	C840 C 8	C953 C 18	L8817 L 17	R71 R 19	R585 R 23
	C841 C 8	C954 C 18	L8818 L 11	R72 R 19	R586 R 5
	C842 C 8	C955 C 18	L8819 L 11	R73 R 19	R587 R 5
	C843 C 13	C956 C 21	L8820 L 15	R74 R 24	R588 R 7
	C844 C 3	C957 C 17	L8821 L 11	R75 R 24	R589 R 7
	C845 C 9	C958 C 17	L8822 L 11	R76 R 24	R590 R 23
	C846 C 4	C959 C 17	L8823 L 17	R77 R 24	R591 R 5
	C847 C 8	C960 C 17	MEC1 MEC.SCREW 27	R78 R 19	R592 R 5
	C848 C 3	C961 C 17	MEC2 MEC.SCREW 27	R79 R 19	R593 R 3
	C849 C 19	C962 C 11	MEC3 MEC.SCREW 27	R80 R 19	R594 R 3
	C850 C 13	C963 C 11	MEC4 MEC.SCREW 27	R81 R 12	R595 R 3
	C851 C 13	C964 C 15	Q1 Q.FET_N.ENH 3	R82 R 13	R596 R 3
	C852 C 8	C965 C 11	Q2 Q.FET_P.ENH 23	R83 R 13	R597 R 3
	C853 C 8	C966 C 11	Q3 Q.FET_P.ENH 22	R84 R 6	R598 R 3
	C854 C 9	C967 C 17	Q501 Q.FET_N.ENH 19	R85 R 6	R599 R 3
	C855 C 4	C968 C 17	Q502 Q.FET_P.ENH 22	R86 R 6	R600 R 20
	C856 C 9	CN582 CON_AGP 3	Q503 Q.FET_N.ENH 26	R87 R 6	R601 R 20
	C857 C 9	D1 D_3PIN_LAC 17	Q504 Q.FET_P.ENH 23	R88 R 6	R602 R 4
	C858 C 13	D2 D_3PIN_LAC 10	Q505 Q.FET_N.ENH 23	R89 R 6	R603 R 4
	C859 C 13	D3 D_3PIN_LAC 11	Q506 Q.NPN 26	R90 R 3	R604 R 3
	C860 C 19	D4 D_3PIN_LAC 11	Q507 Q.NPN 26	R91 R 3	R605 R 4
	C861 C 8	D5 D_3PIN_LAC 11	Q508 Q.FET_N.ENH 23	R92 R 3	R606 R 8
	C862 C 8	D6 D_3PIN_LAC 17	Q509 Q.FET_N.ENH 23	R93 R 3	R607 R 20
	C863 C 13	D7 D_3PIN_LAC 17	Q510 Q.FET_N.ENH 22	R94 R 3	R608 R 20
	C864 C 13	D8 D_3PIN_LAC 10	Q511 Q.FET_N.ENH 22	R95 R 5	R609 R 4
	C865 C 25	D9 D_3PIN_LAC 10	Q512 Q.FET_N.ENH 23	R96 R 5	R610 R 20
	C866 C 8	D10 D_3PIN_LAC 10	Q513 Q.FET_N.ENH 23	R97 R 5	R611 R 20
	C867 C 21	D11 D_SCHOTTKY 26	Q514 Q.FET_N.ENH 23	R98 R 5	R612 R 20
	C868 C 13	D12 D_SCHOTTKY 26	Q515 Q.FET_N.ENH 22	R99 R 5	R613 R 5
	C869 C 13	D501 D_ZENER 23	Q516 Q.FET_N.ENH 24	R100 R 5	R614 R 4
	C870 C 4	D502 D 19	Q517 Q.FET_N.ENH 24	R101 R 5	R615 R 4
	C871 C 25	D503 D_SCHOTTKY 22	Q518 Q.FET_N.ENH 23	R102 R 5	R616 R 4
	C872 C 8	D504 D_SCHOTTKY 22	Q519 Q.FET_N.ENH 24	R501 R 23	R617 R 6
	C873 C 8	D505 D_SCHOTTKY 22	Q520 Q.FET_N.ENH 3	R502 R 26	R618 R 8
	C874 C 8	D506 D_3PIN_RA 22	Q521 Q.NPN 3	R503 R 26	R619 R 4
	C875 C 8	D507 D_SCHOTTKY 23	Q522 Q.FET_N.ENH 9	R504 R 26	R620 R 4
	C876 C 21	D508 D_SCHOTTKY 23	Q523 Q.FET_N.ENH 19	R505 R 26	R621 R 4
	C877 C 9	D509 D_SCHOTTKY 21	Q524 Q.FET_N.ENH 21	R506 R 23	R622 R 6
	C878 C 9	D510 D 19	Q525 Q.NPN 21	R507 R 23	R623 R 4
	C879 C 19	D511 D_SCHOTTKY 21	Q526 Q.FET_N.ENH 21	R508 R 23	R624 R 3
	C880 C 8	D512 D_3PIN_LAC 17	Q527 Q.NPN 21	R509 R 22	R625 R 3
	C881 C 8	D513 D_3PIN_LAC 17	Q528 Q.NPN 21	R510 R 26	R626 R 3
	C882 C 8	D514 D_3PIN_LAC 17	Q529 Q.FET_N.ENH 21	R511 R 26	R627 R 3
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	C884 C 19	D516 D_3PIN_LAC 10	R2 R 15	R513 R 26	R629 R 4
	C885 C 9	D517 D_3PIN_LAC 10	R3 R 15	R514 R 26	R630 R 4
	C886 C 21	D518 D_3PIN_LAC 10	R4 R 15	R515 R 26	R631 R 8
	C887 C 19	D519 D_3PIN_LAC 17	R5 R 11	R516 R 26	R632 R 12
	C888 C 21	D520 D_3PIN_LAC 17	R6 R 11	R517 R 26	R633 R 19
	C889 C 19	D521 D_3PIN_LAC 11	R7 R 11	R518 R 26	R634 R 3
	C890 C 21	D522 D_3PIN_LAC 11	R8 R 11	R519 R 26	R635 R 9
	C891 C 3	D523 D_3PIN_LAC 11	R9 R 11	R520 R 26	R636 R 13
	C892 C 21	D524 D_3PIN_LAC 11	R10 R 11	R521 R 23	R637 R 13
	C893 C 21	F501 F_POLYSW 23	R11 R 17	R522 R 23	R638 R 13
	C894 C 21	F502 F_POLYSW 21	R12 R 10	R523 R 26	R639 R 13
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	C897 C 21	J3 CON_DSUB15HD 10	R15 R 10	R526 R 29	R642 R 9
	C898 C 23	J4 HDR_1X2 19	R16 R 10	R527 R 22	R643 R 6
	C899 C 21	J5 HDR_1X2 19	R17 R 10	R528 R 23	R644 R 9
	C900 C 21	J6 HDR_1X4 23	R18 R 10	R529 R 22	R645 R 13
	C901 C 21	L1 L_CMF_4P 11	R19 R 19	R530 R 22	R646 R 13
	C902 C 21	L2 L_CMF_4P 11	R20 R 19	R531 R 22	R647 R 13
	C903 C 9	L3 L_CMF_4P 11	R21 R 19	R532 R 22	R648 R 13
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