PCI-EXPRESS EDGE CONNECTOR

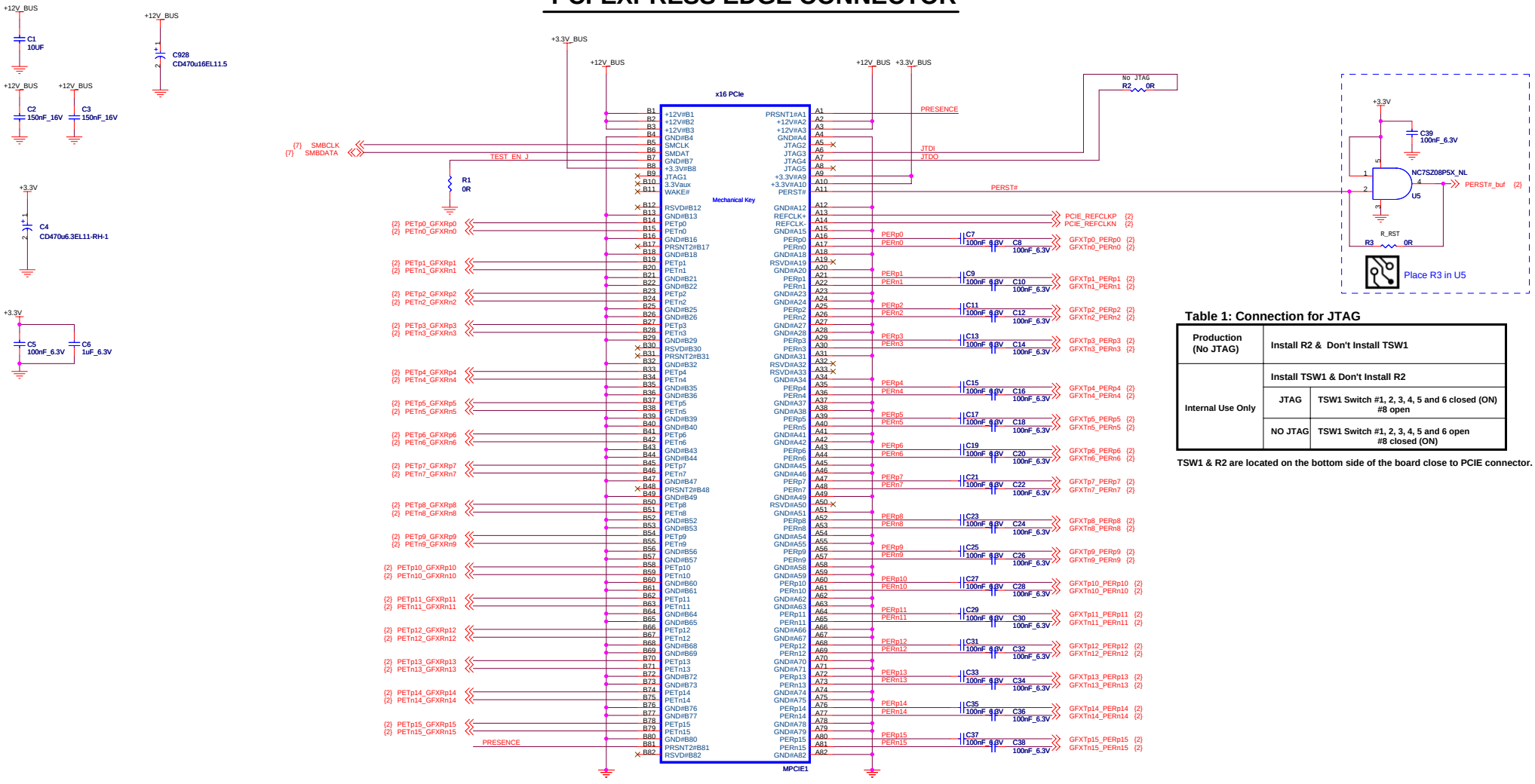

Table 1: Connection for JTAG

Production (No JTAG)	**Install R2 & Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 closed (ON)**

TSW1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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Title	RV635 GDDR3 - PCI-E Edge Connector
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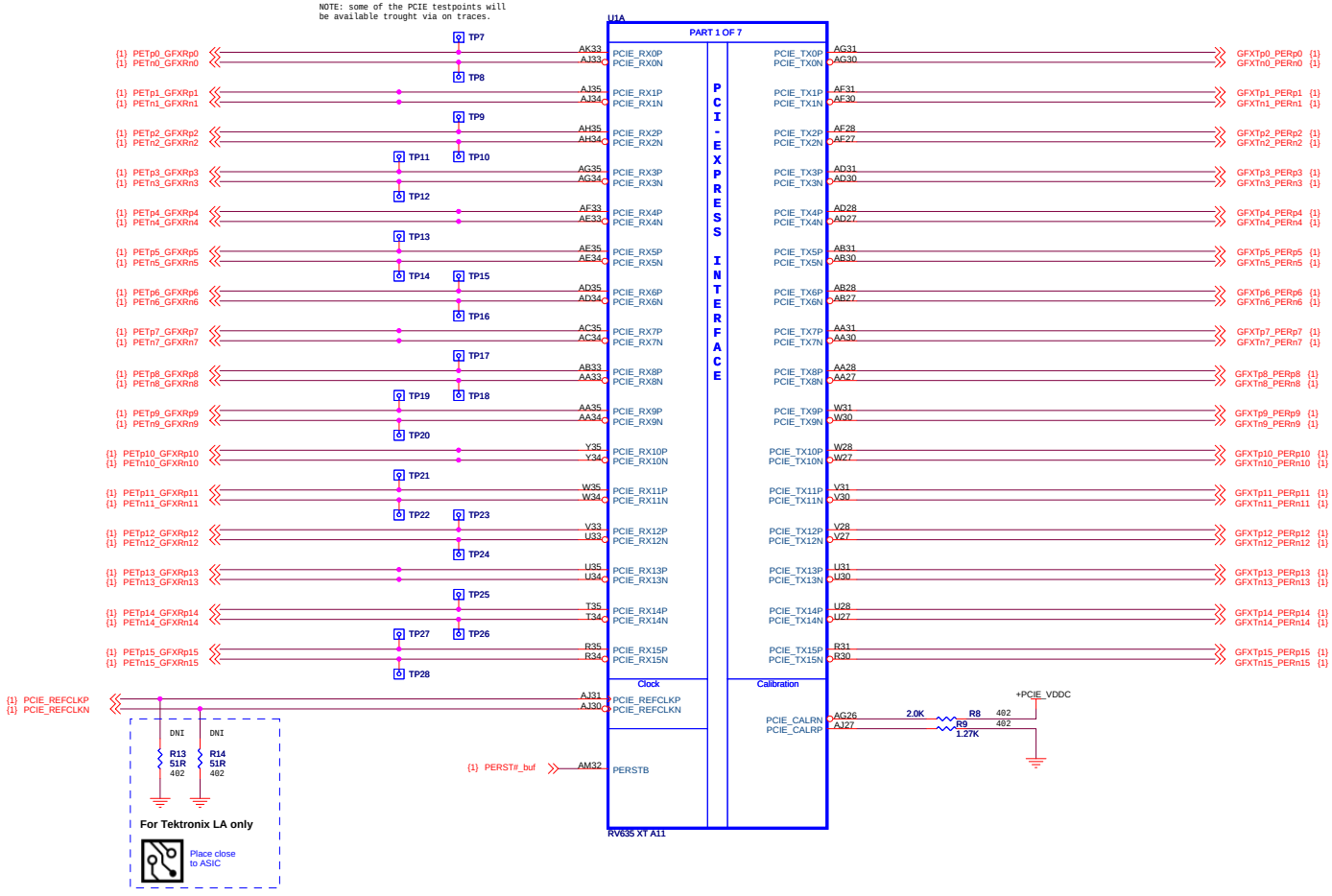

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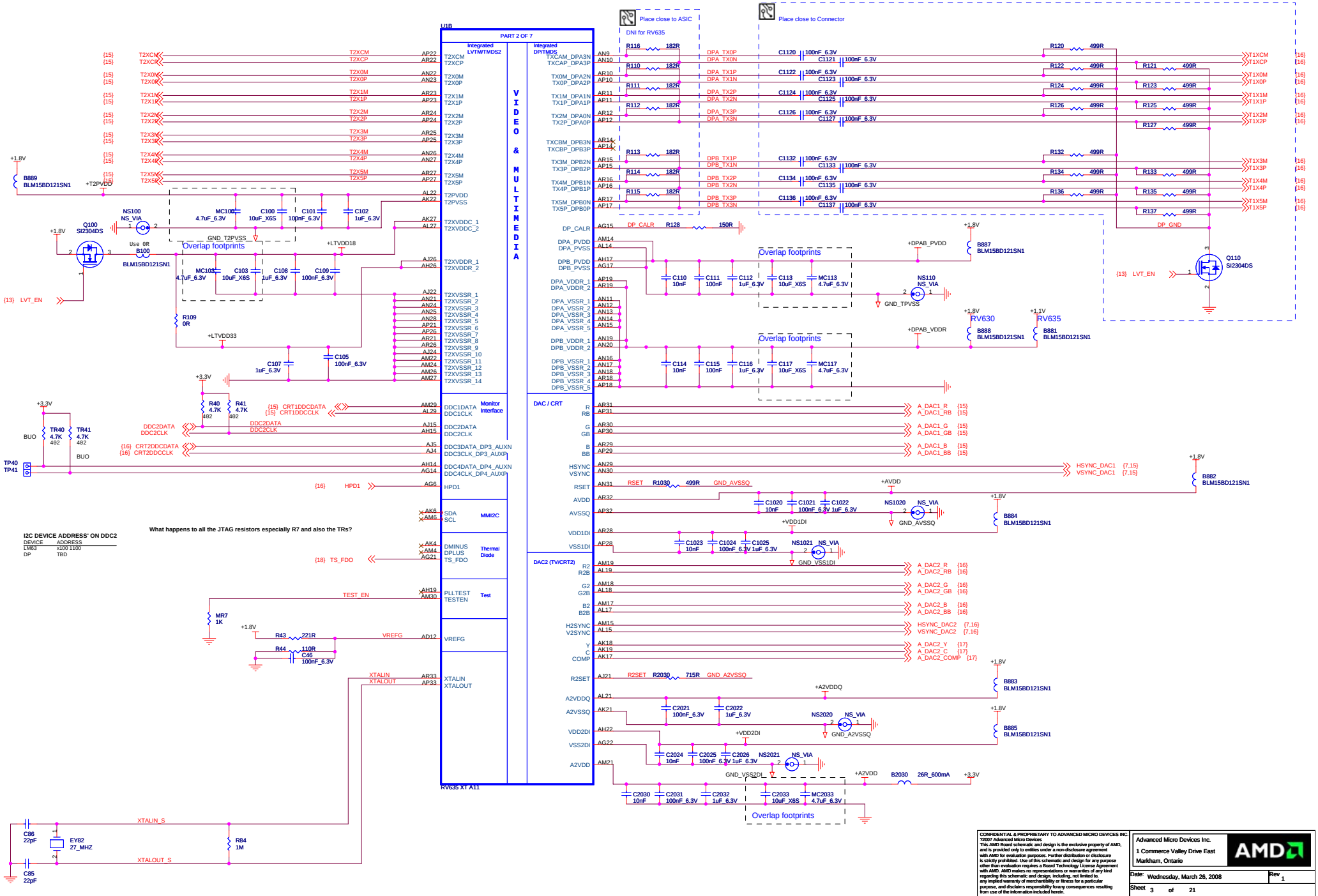
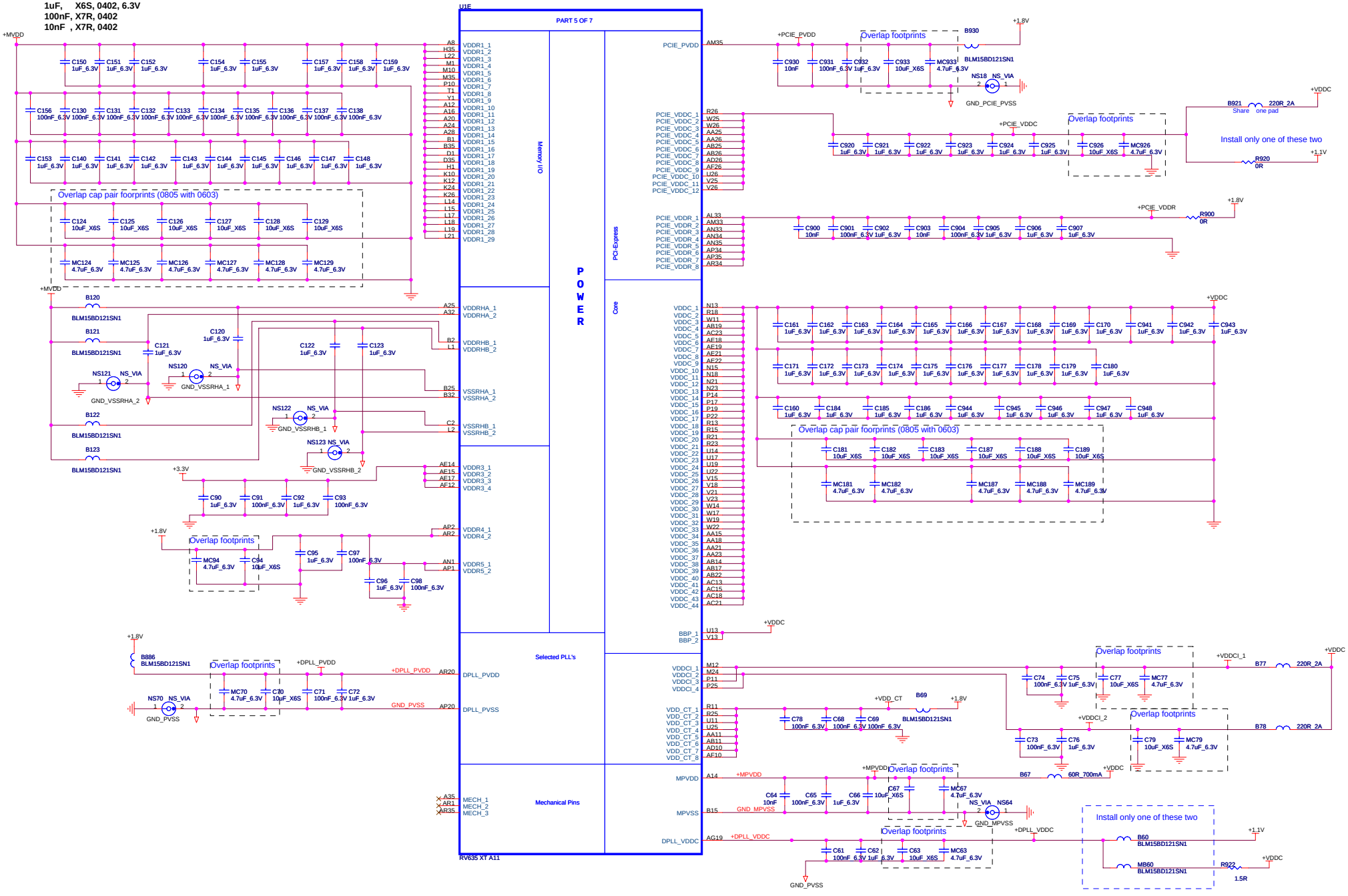
Title RV635 GDDR3 - ASIC PCIE_Interface

Doc No. 105-B380xx-00

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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Title	RV635 GDDR3 - ASIC Power
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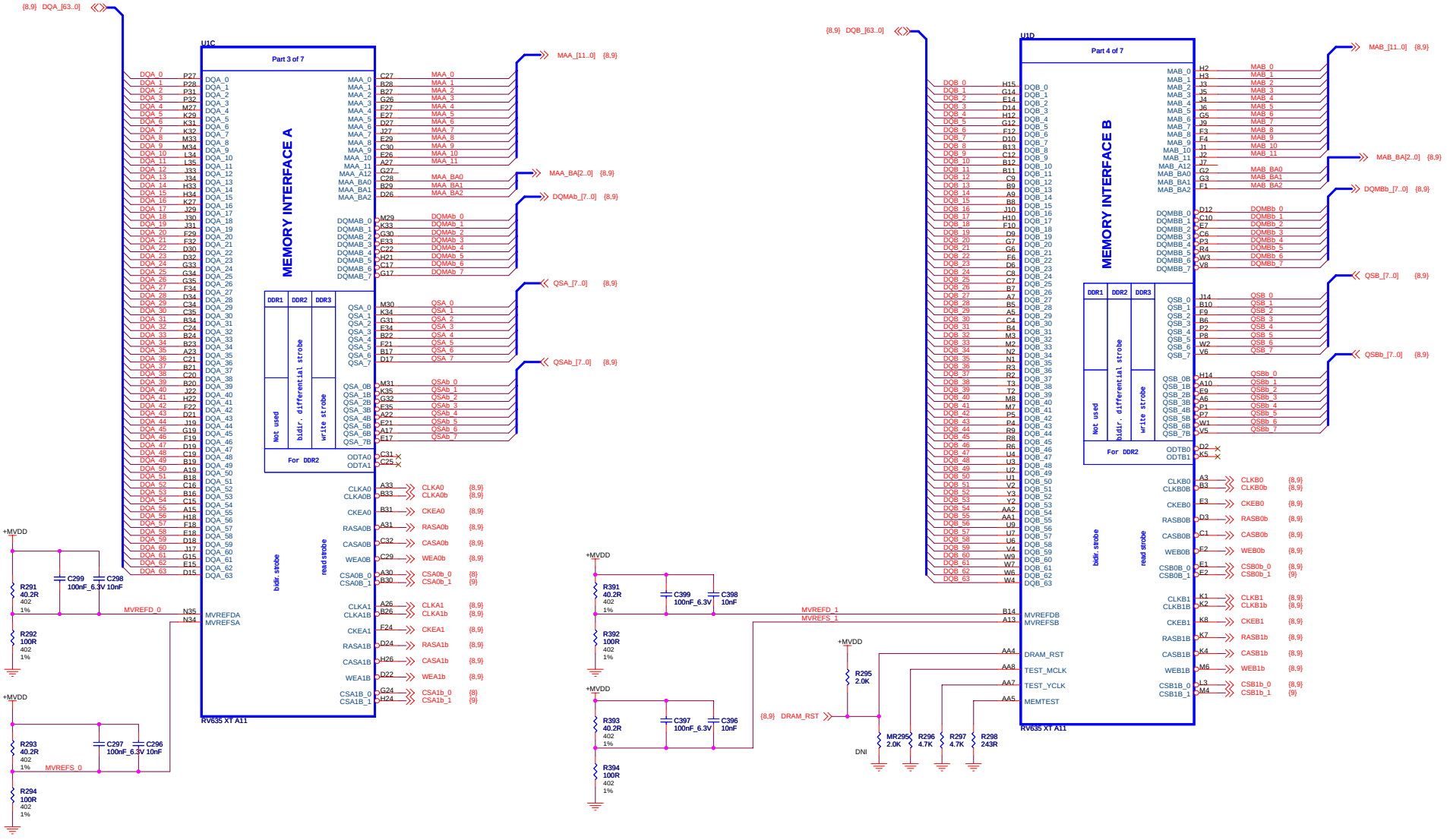

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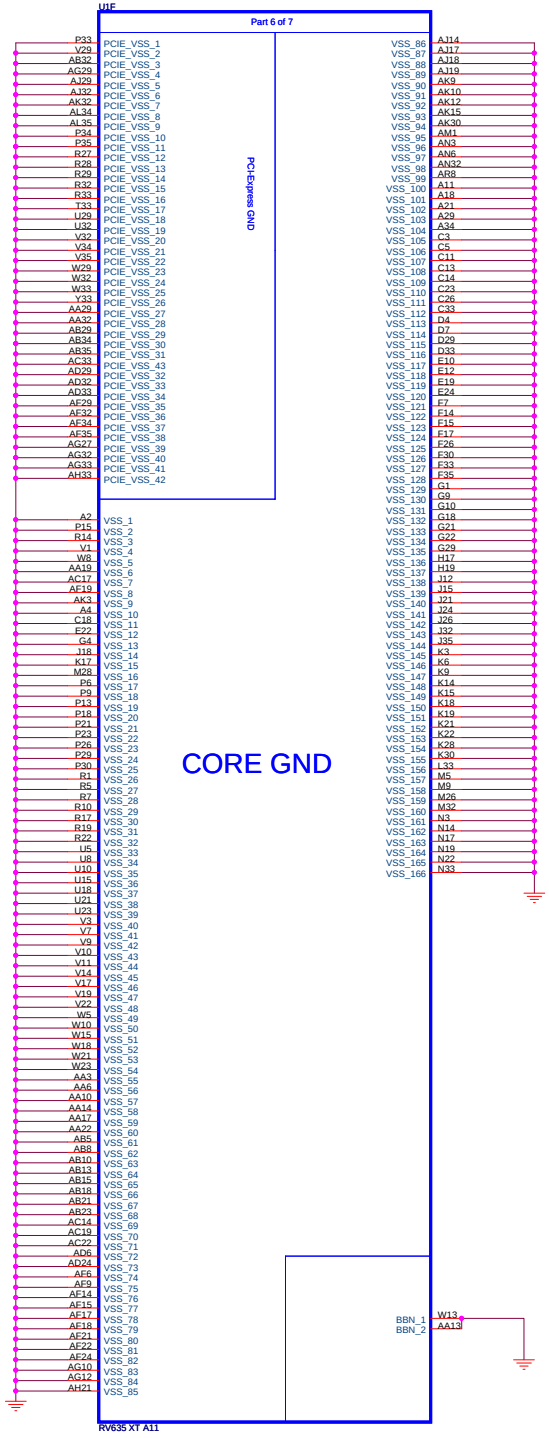
Title RV635 GDDR3 - ASIC Memory Interface (Channel A & B) Doc No. 105-B380xx-00



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Title RV635 GDDR3 - ASIC Grounds

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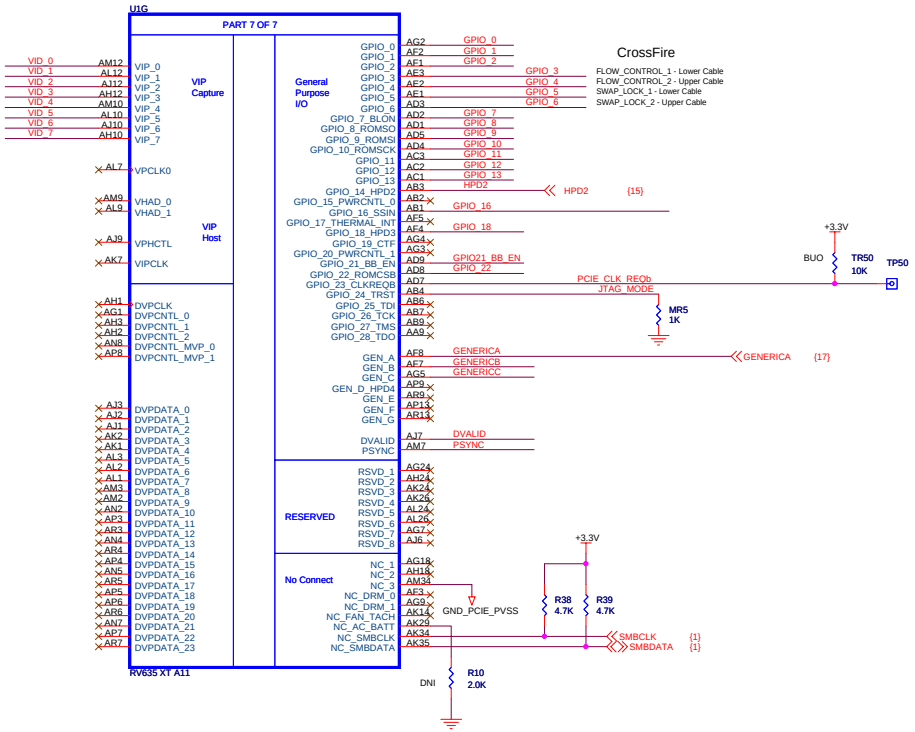

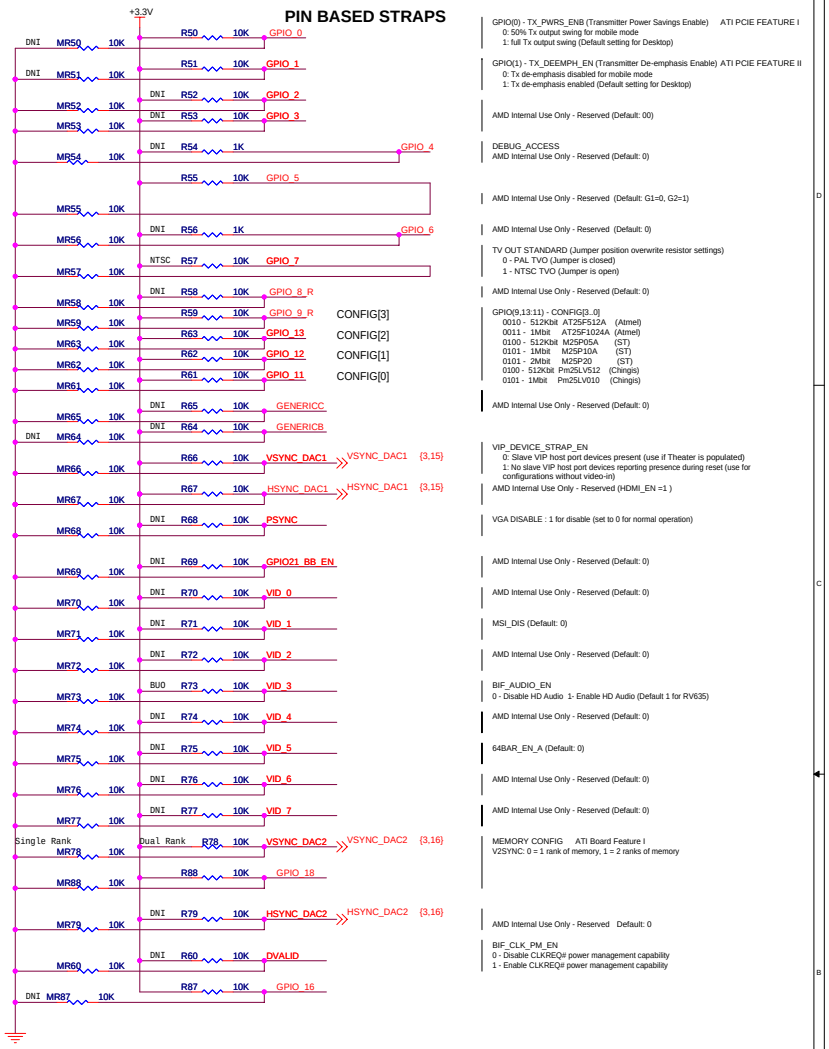

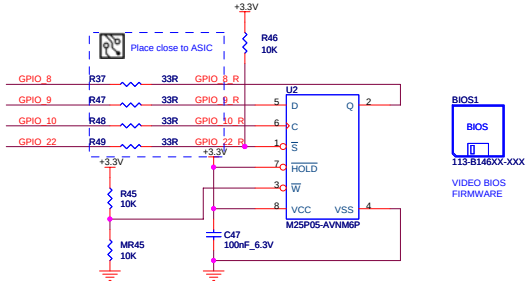

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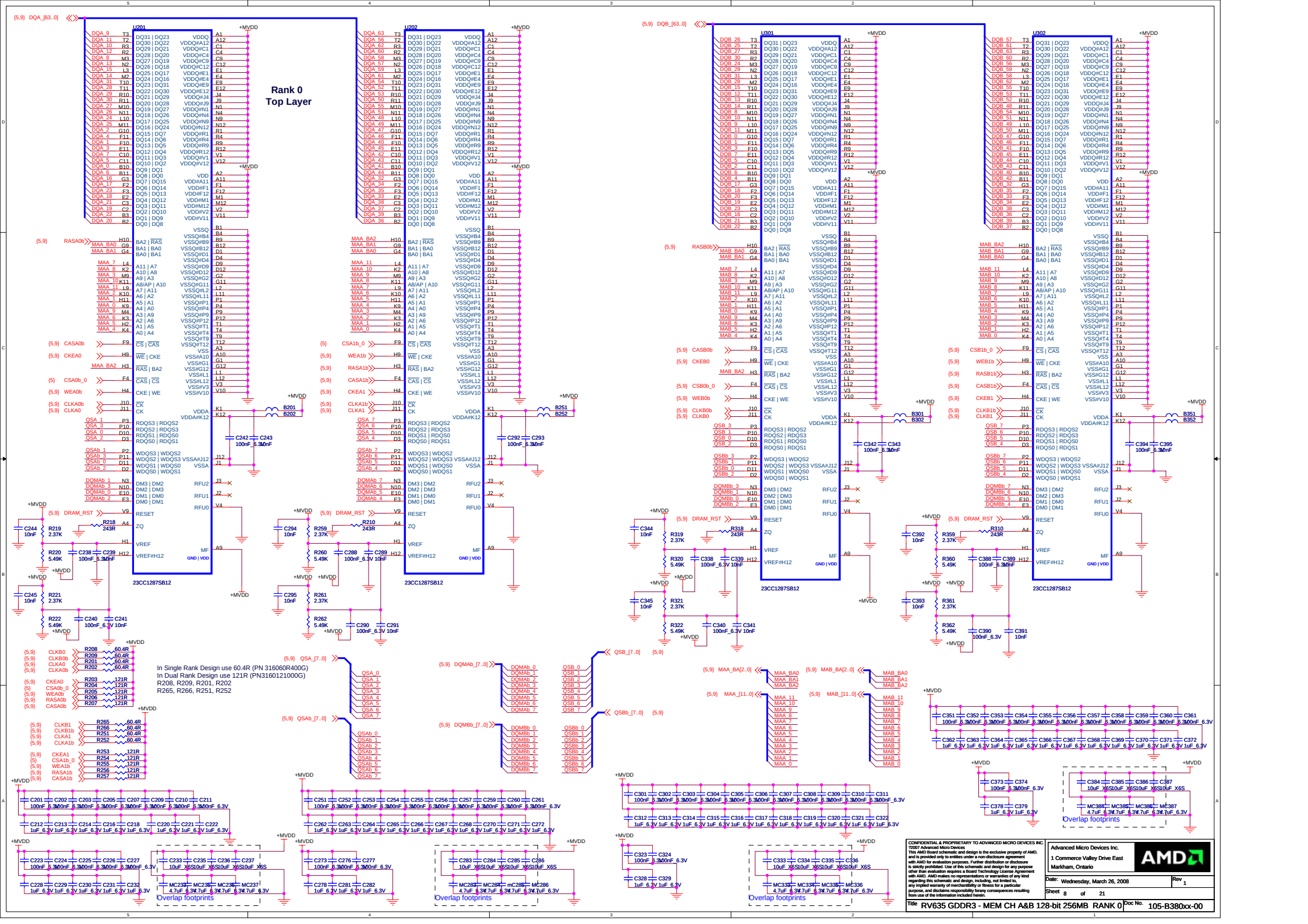
Title RV635 GDDR3 - ASIC DVO & GPIOs

Doc No. 105-B380xx-00


Rank 0
Top Layer
U201
U202
U301
U302
23CC1287SB12
In Single Rank Design use 60.4R (PN 316060R400G)
In Dual Rank Design use 121R (PN3160121000G)
R208, R209, R201, R202
R265, R266, R251, R252
Overlap footprints
Overlap footprints
Overlap footprints
Overlap footprints
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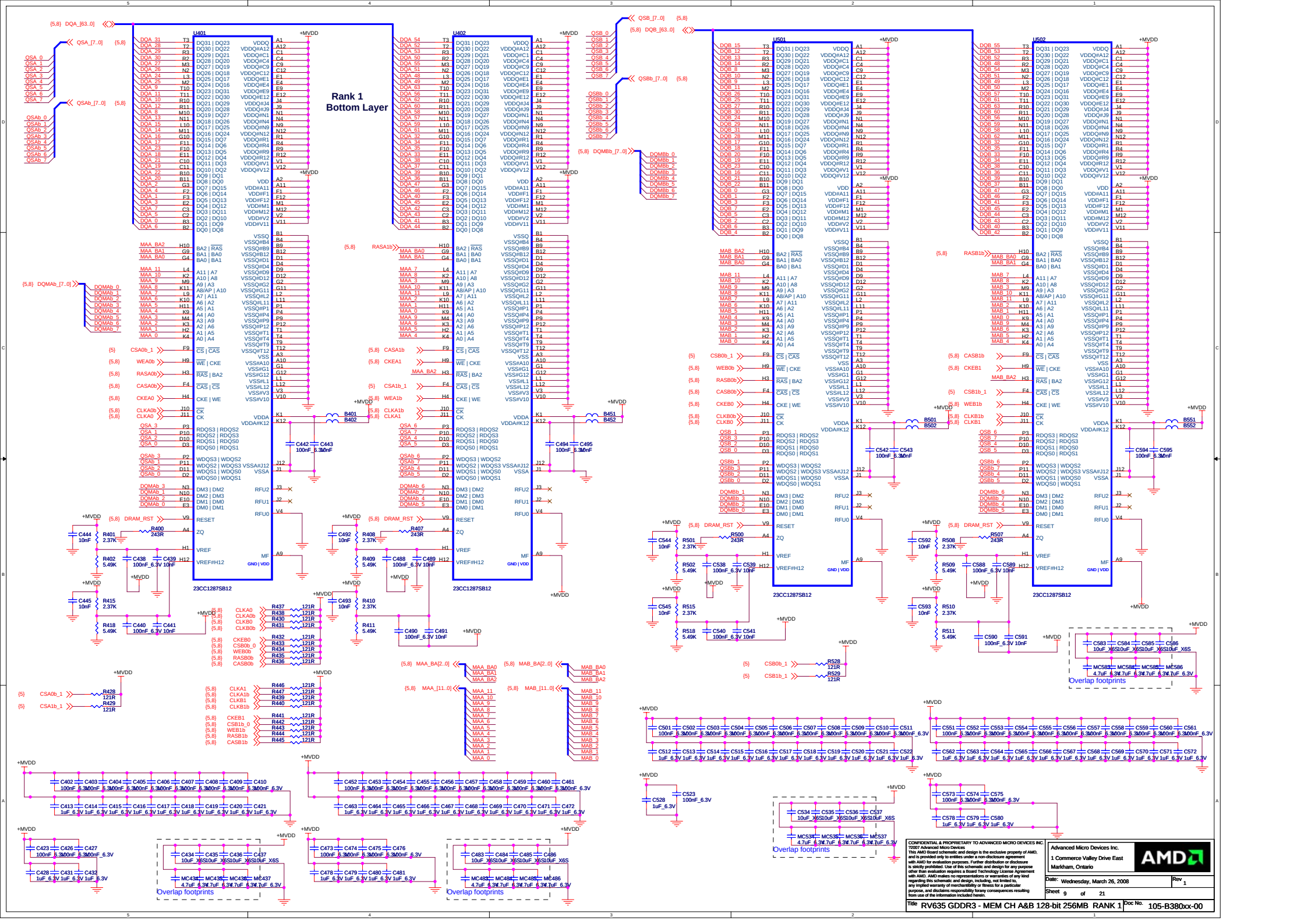
Title RV635 GDDR3 - MEM CH A&B 128-bit 256MB RANK 0
Doc No. 105-B380xx-00


Rank 1
Bottom Layer
U401
U402
U501
U502
23CC1287SB12
Overlap footprints
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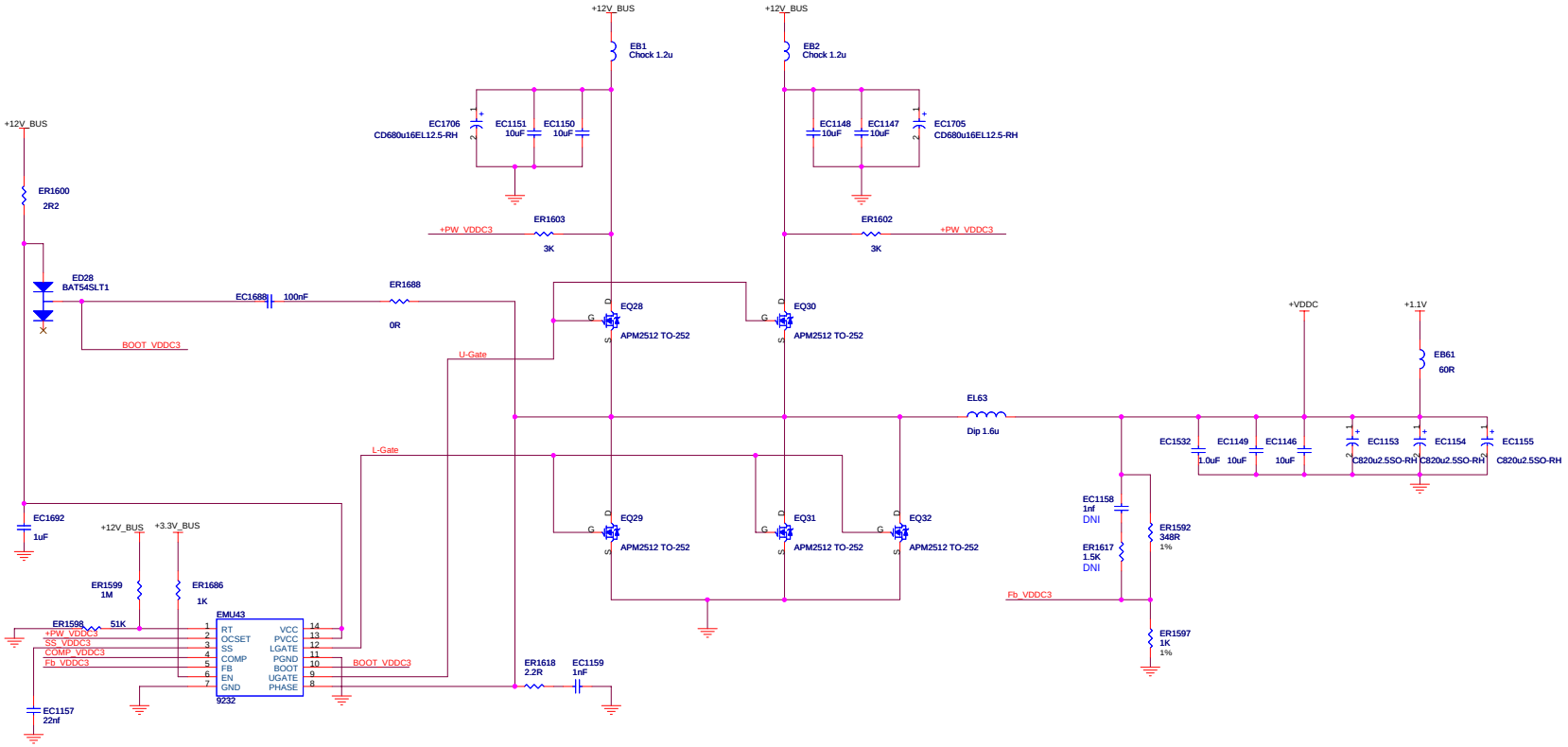
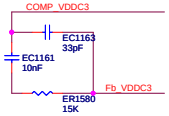
CORE REGULATOR VDDC



+VDDC=0.8*(1+(ER1592 / ER1597))

Compensation Circuit



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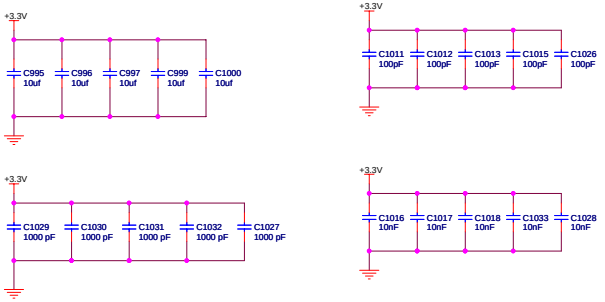
Title RV635 GDDR3 - VDDC SMPS 01

Doc No. 105-B380xx-00



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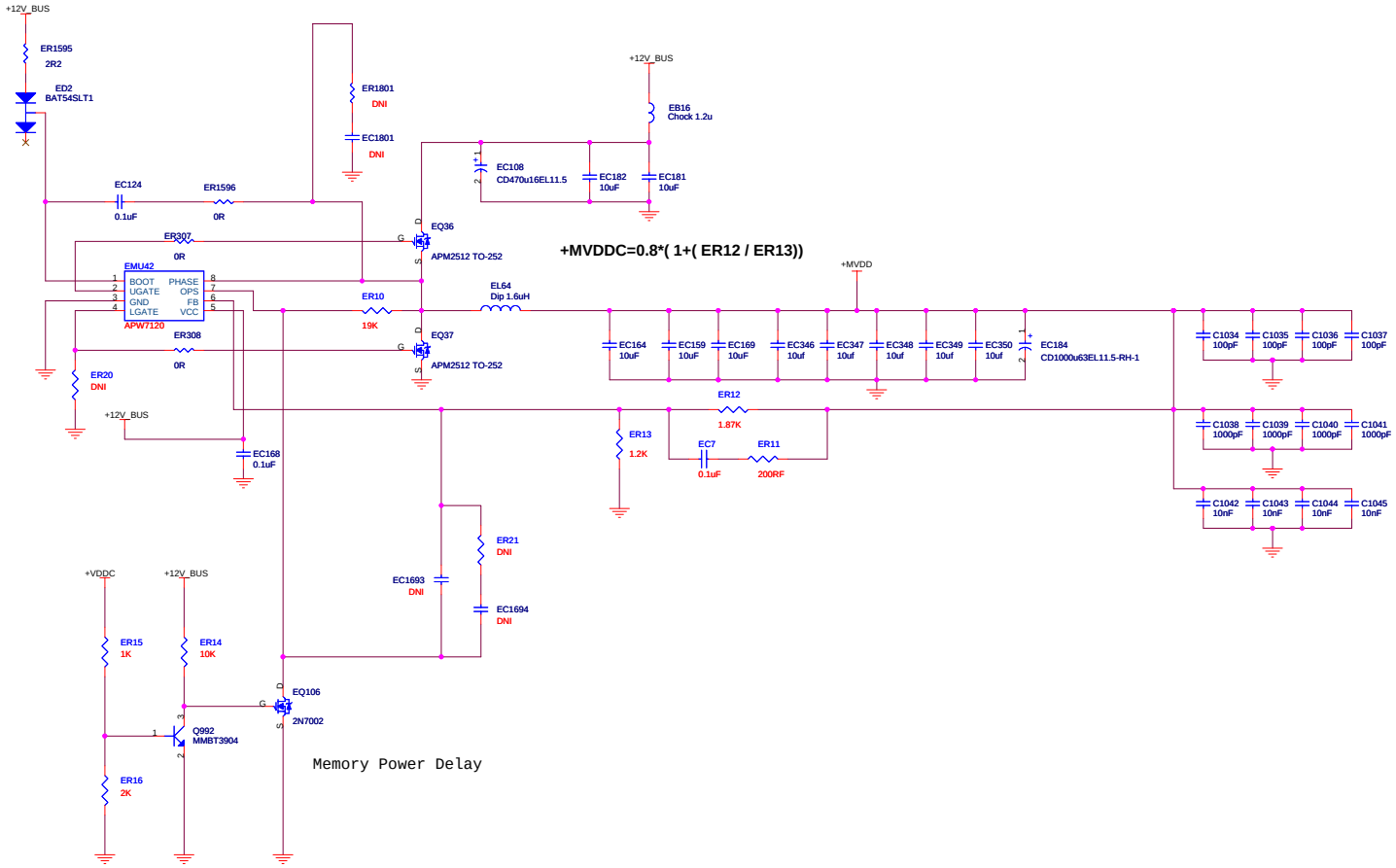
Title: RV635 GDDR3 - VDDC SMPS 02

Doc No. 105-B380xx-00



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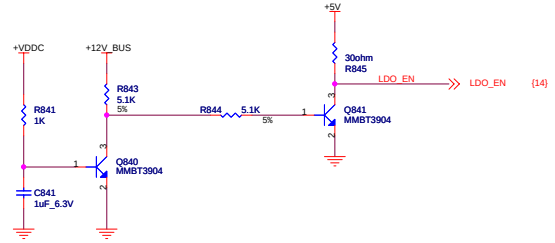
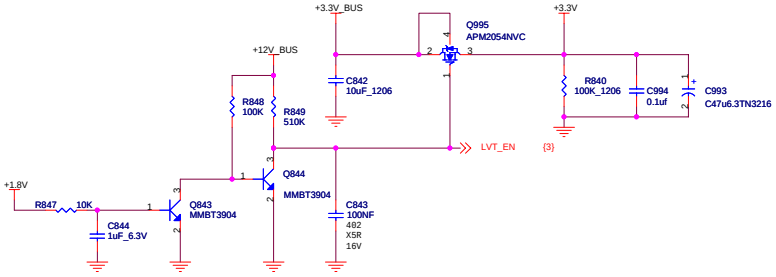
Title	RV635 GDDR3 - MVDD SMPS 01
Doc No.	105-B380xx-00

Power up Sequencing





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Title RV635 GDDR3 - Power Management

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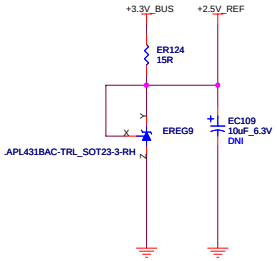
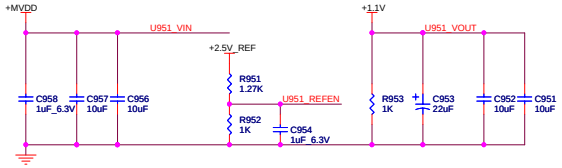
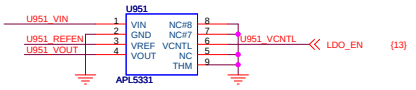
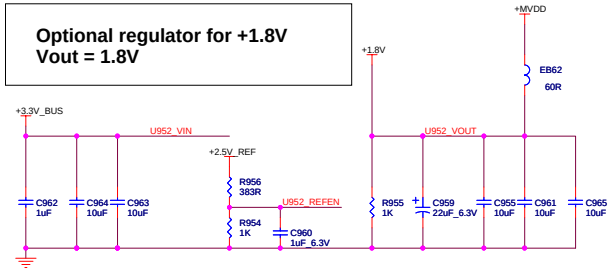


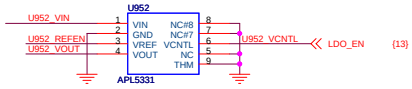
Optional regulator for +1.1V
Vout = 1.1V

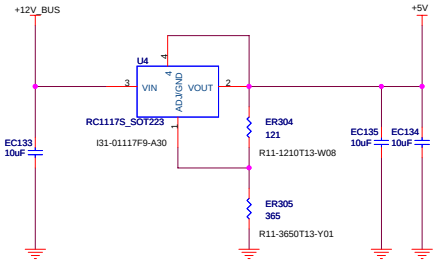




Optional regulator for +1.8V
Vout = 1.8V







Vout=1.25V* [1+(ER305/ER304)]

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Title RV635 GDDR3 - Linear Regulators

Doc No. 105-B380xx-00

See BOM for qualified filters

{3} A_DAC1_R — R1001 75R — C1004 8.0pF — L1001 47nH — A_R_DAC1_M — C1001 12pF_50V — L1004 36NH
{3} A_DAC1_RB — R1027 37.4R
{3} A_DAC1_G — R1002 75R — C1005 8.0pF — L1002 47nH — A_G_DAC1_M — C1002 12pF_50V — L1005 36NH
{3} A_DAC1_GB — R1028 37.4R
{3} A_DAC1_B — R1003 75R — C1006 8.0pF — L1003 47nH — A_B_DAC1_M — C1003 12pF_50V — L1006 36NH
{3} A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

+3.3V — BAT54SLT1 ED62 — BAT54SLT1 ED63 — BAT54SLT1 ED64 — +3.3V — +3.3V

+5V — EF1 1.5A — +5V_VESA

+5V — ED71 BAT54SLT1 — +5V — ED70 BAT54SLT1 — +5V — ED69 BAT54SLT1 — +5V — ED68 BAT54SLT1

C1010 104pF

MJ1001 G3179C219-005
1 R
2 G
3 B
11 MS0
12 MS1
4 MS2
15 MS3
9 NC
13 HS
14 VS
5 VSS
6 VSS#6
7 VSS#7
8 VSS#8
10 VSS#10
16 CASE
17 CASE#17

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

RV635: 10K pull up on 3.3V, 2.2K pull up on 5V
RV630: 24.3K pull up on 3.3V, 19.1K on 5V

+3.3V — R1004 10K — +5V — R1005 2.2K — Q1001 BSH111 — {3} CRT1DDCDATA — DDCDATA_DAC1_5V — R1006 33R — DDCDATA_DAC1_R

+3.3V — R1007 10K — +5V — R1008 2.2K — Q1002 BSH111 — {3} CRT1DDCCLK — DDCCLK_DAC1_5V — R1009 33R — DDCCLK_DAC1_R

+5V — C1999 100nF_6.3V
{3,7} HSYNC_DAC1 — U1999A SN74HCT125D — HSYNC_DAC1_B — R1010 10R — HSYNC_DAC1_R
{3,7} VSYNC_DAC1 — U1999B SN74HCT125D — VSYNC_DAC1_B — R1011 10R — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

R103 100R — T2X3P_R — T2X3M_R — REG1122 RCLAMP0524P
{3} T2X3M — R1018 0R
{3} T2X3P — R1019 0R
{3} T2X4M — R1014 0R
{3} T2X4P — R1015 0R
R104 100R

R102 100R — T2X2M_R — T2X2P_R — T2X4M_R — T2X4P_R — DDCCLK_DAC1_R — DDCDATA_DAC1_R — VSYNC_DAC1_R — T2X1M_R — T2X1P_R — T2X3M_R — T2X3P_R

REG1123 RCLAMP0524P
{3} T2X1M — R1016 0R
{3} T2X1P — R1017 0R
{3} T2X2M — R1012 0R
{3} T2X2P — R1013 0R
R101 100R

+3.3V — Q1021 MMBT3904 — R1022 10K — HPD_DVI2 — {7} HPD2 — R1023 10K

REG1124 RCLAMP0524P
{3} T2X5M — R1024 0R
{3} T2X5P — R1025 0R
R105 100R — T2X0M_R — T2X0P_R — T2X5M_R — T2X5P_R — T2XCP_R — T2XCM_R

REG1125 RCLAMP0524P
{3} T2X0P — R1021 0R
{3} T2X0M — R1020 0R
{3} T2XCP — R1026 0R
{3} T2XCM — R1031 0R
R100 100R

R106 100R — A_R_DAC1_F — A_G_DAC1_F — A_B_DAC1_F — HSYNC_DAC1_R

+5V_VESA — J1001 DVI_CONNECTOR
25 CASE
1 TMDS Data2-
2 TMDS Data2+
3 TMDS Data2/4 Shield
4 TMDS Data4-
5 TMDS Data4+
6 DDC Clock
7 DDC Data
8 Analog VSYNC
9 TMDS Data1-
10 TMDS Data1+
11 TMDS Data1/3 Shield
12 TMDS Data3-
13 TMDS Data3+
14 +5V Power
15 GND (for +5V)
16 Hot Plug Detect
17 TMDS Data0-
18 TMDS Data0+
19 TMDS Data0/5 Shield
20 TMDS Data5-
21 TMDS Data5+
22 TMDS Clock Shield
23 TMDS Clock+
24 TMDS Clock-
C1 Analog Red
C2 Analog Green
C3 Analog Blue
C4 Analog HYNC
C5 Analog GND
C6 Analog GND#C6
26 CASE#26
27 CASE#27
28 CASE#28
29 CASE#29
30 CASE#30

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See BOM for qualified filters

{3} A_DAC2_R
{3} A_DAC2_RB
{3} A_DAC2_G
{3} A_DAC2_GB
{3} A_DAC2_B
{3} A_DAC2_BB

R2001 75R 402
R2027 37.4R
R2002 75R 402
R2028 37.4R
R2003 75R 402
R2029 37.4R

C2004 8.0pF 402
C2001 402 12pF_50V
C2005 8.0pF 402
C2002 402 12pF_50V
C2006 8.0pF 402
C2003 402 12pF_50V

L2001 47nH
L2002 47nH
L2003 47nH

A_R_DAC2_M
A_G_DAC2_M
A_B_DAC2_M

L2004 36NH
L2005 36NH
L2006 36NH

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F

+3.3V
BAT54SLT1 ED67
BAT54SLT1 ED66
BAT54SLT1 ED65

+5V_VESA

MJ2001
1 R
2 G
3 B
11 MS0
12 MS1
4 MS2
15 MS3
9 NC
13 HS
14 VS
5 VSS
6 VSS#6
7 VSS#7
8 VSS#8
10 VSS#10
16 CASE
17 CASE#17
G3179C219-005

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R

+5V
ED75 BAT54SLT1
ED74 BAT54SLT1
ED73 BAT54SLT1
ED72 BAT54SLT1

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

{3} CRT2DDCDATA
{3} CRT2DDCCLK

DNI for RV635
R2004 24.3K
R2007 24.3K
BSH111 Q2001
BSH111 Q2002
R2040 0R
R2041 0R
DNI for RV630

R2005 2.2K 402 DDCDATA_DAC2_5V
R2008 2.2K 402 DDCCLK_DAC2_5V
R2006 33R 402 DDCDATA_DAC2_R
R2009 33R 402 DDCCLK_DAC2_R

RV635: no pull up on 3.3V, 2.2K pull up on 5V
RV630: 24.3K pull up on 3.3V, 19.1K on 5V

{3,7} HSYNC_DAC2
{3,7} VSYNC_DAC2

U1999C SN74HCT125D
SN74HCT125D U1999D

HSYNC_DAC2_B
VSYNC_DAC2_B
R2010 10R 402 HSYNC_DAC2_R
R2011 10R 402 VSYNC_DAC2_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

+3.3V
Q2021 MMBT3904
R2022 10K
HPD_DVI1
{3} HPD1
R2023 10K

+5V_VESA

J2001
25 CASE
1 TMDS Data2-
2 TMDS Data2+
3 TMDS Data2/4 Shield
4 TMDS Data4-
5 TMDS Data4+
6 DDC Clock
7 DDC Data
8 Analog VSYNC
9 TMDS Data1-
10 TMDS Data1+
11 TMDS Data1/3 Shield
12 TMDS Data3-
13 TMDS Data3+
14 +5V Power
15 GND (for +5V)
16 Hot Plug Detect
17 TMDS Data0-
18 TMDS Data0+
19 TMDS Data0/5 Shield
20 TMDS Data5-
21 TMDS Data5+
22 TMDS Clock Shield
23 TMDS Clock+
24 TMDS Clock-
C1 Analog Red
C2 Analog Green
C3 Analog Blue
C4 Analog HYNC
C5 Analog GND
C6 Analog GND#C6
26 CASE#26
27 CASE#27
28 CASE#28
29 CASE#29
30 CASE#30
DVI_CONNECTOR

{3} T1X2M
{3} T1X2P
{3} T1X4M
{3} T1X4P
DDCCLK_DAC2_R
DDCDATA_DAC2_R
VSYNC_DAC2_R
{3} T1X1M
{3} T1X1P
{3} T1X3M
{3} T1X3P
{3} T1X0M
{3} T1X0P
{3} T1X5M
{3} T1X5P
{3} T1XCP
{3} T1XCM
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
HSYNC_DAC2_R

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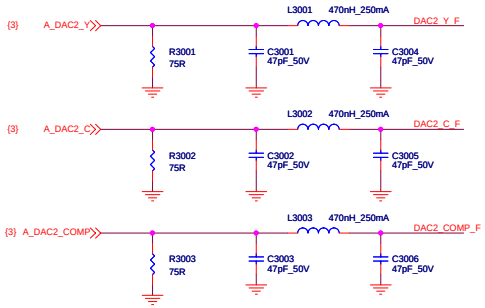
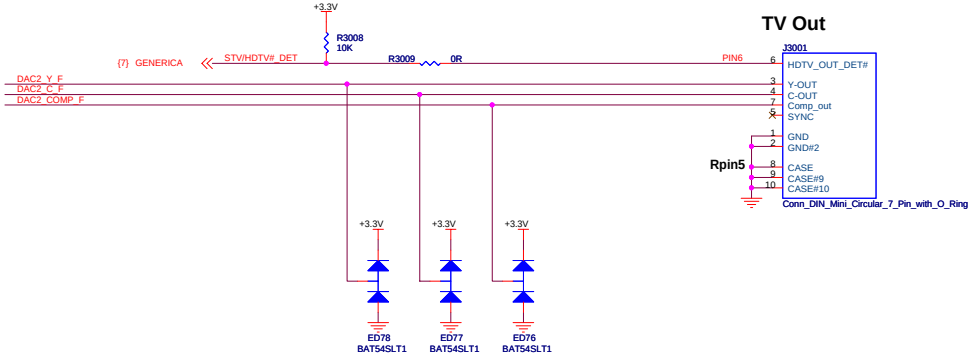
Sheet 16 of 21
Title RV635 GDDR3 - DAC2/TMDS1
Doc No. 105-B380xx-00





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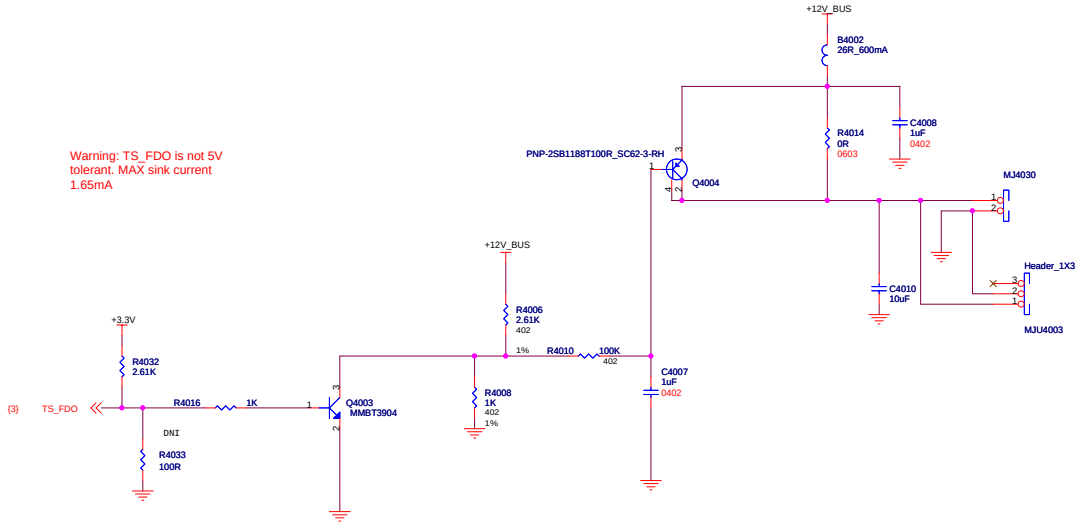
Title RV635 GDDR3 - TVO

Doc No. 105-B380xx-00



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Title: RV635 GDDR3 - Thermal Management | Doc No. 105-B380xx-00

DVI/DVI SCREWS with top tab

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

MT2
MT_Hole_0.136_in_6VIA

DNI

SK1
SOCKET_880

PCB1
PCB
109-B380xx-00

RV635 Socket

ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET
8020038600G

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

J5
X_PIN1*2

J4
X_PIN1*2

J10
X_PIN1*2

J3
3 1
4 2
impedence

J2
3 1
4 2
impedence

J1
3 1
4 2
impedence

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM4 SW_FB
FM5 SW_FB
FM6 SW_FB

FM7
X_SQUARE

FM8
X_SQUARE

U512
E23_1P

U513
E23_1P

U514
E23_1P

U515
E23_1P

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Title RV635 GDDR3 - Mechanical
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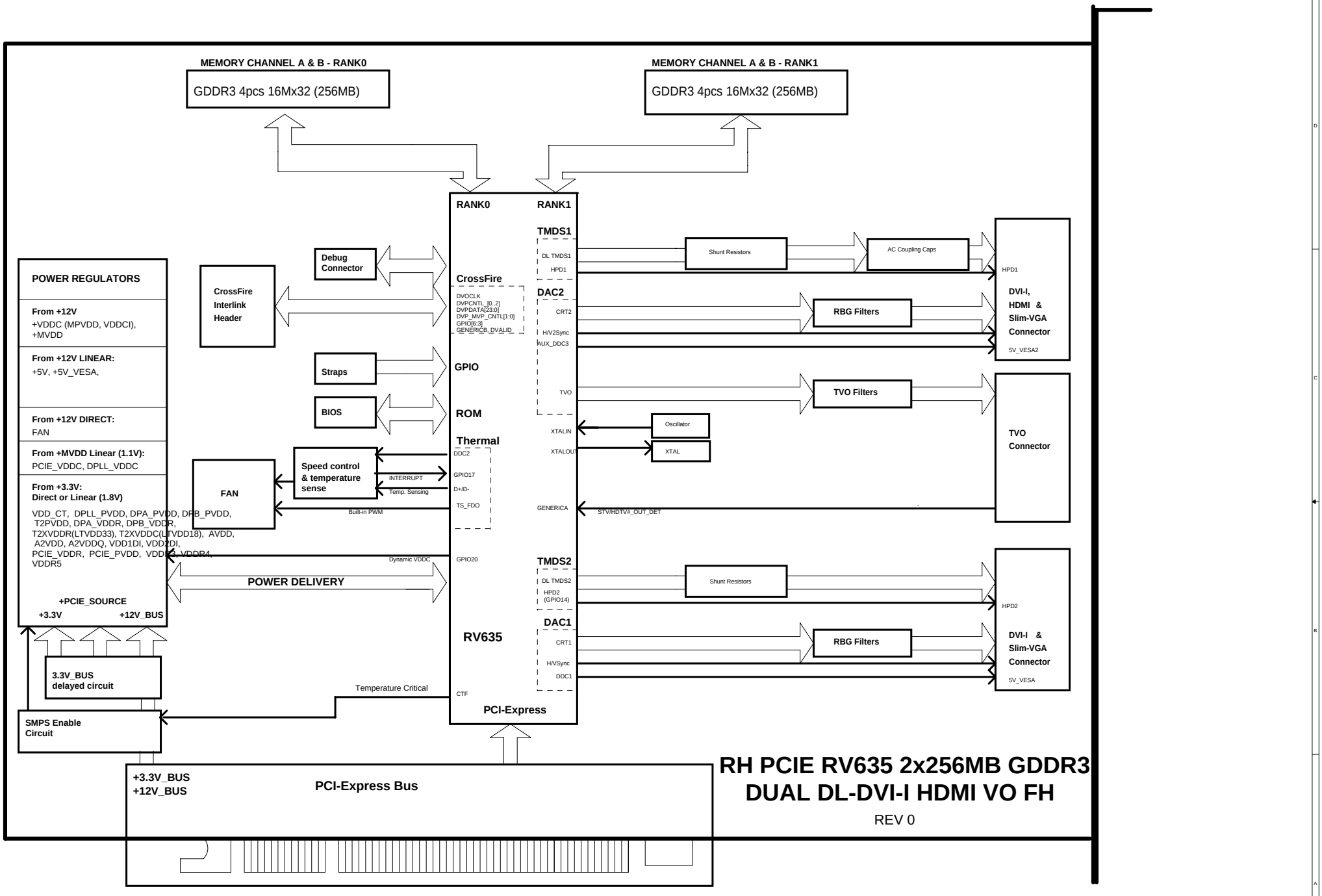
Title	Schematic No.	Date:
RH PCIE RV635 2x256MB GDDR3 DUAL DL-DVI-I DL-DVI-I VO FH	105-B380xx-00	Wednesday, March 26, 2008

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/13/07	Initial design for RV635 GDDR3
1	00	10/25/07	Release To Rev 00



RH PCIE RV635 2x256MB GDDR3 DUAL DL-DVI-I HDMI VO FH

REV 0

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Date: Wednesday, March 26, 2008	Rev 1
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Title RV635 GDDR3 - BLOCK DIAGRAM	Doc No. 105-B380xx-00