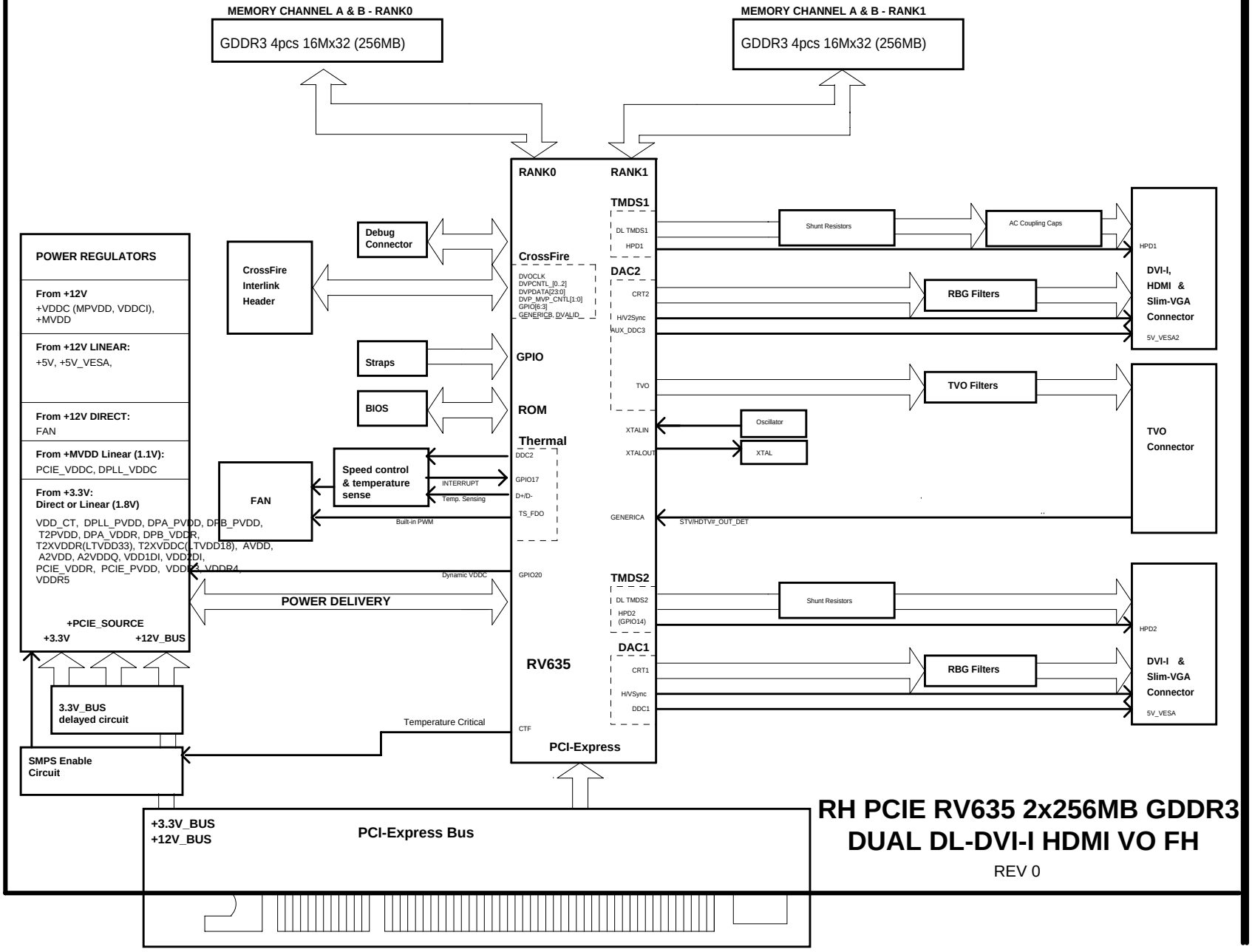
Title	Schematic No.	Date:
RH PCIE RV635 2x256MB GDDR3 DUAL DL-DVI-I DL-DVI-I VO FH	105-B380xx-00	Wednesday, October 31, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/13/07	Initial design for RV635 GDDR3
1	00	10/25/07	Release To Rev 00



RH PCIE RV635 2x256MB GDDR3
DUAL DL-DVI-I HDMI VO FH

REV 0

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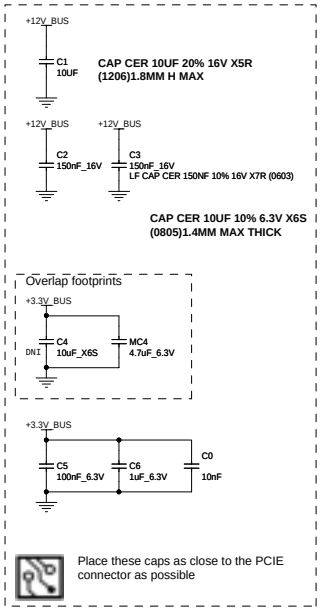
Sheet	21 of 21
Title	RV635 GDDR3 - BLOCK DIAGRAM
Doc No.	105-B380xx-00

PCI-EXPRESS EDGE CONNECTOR



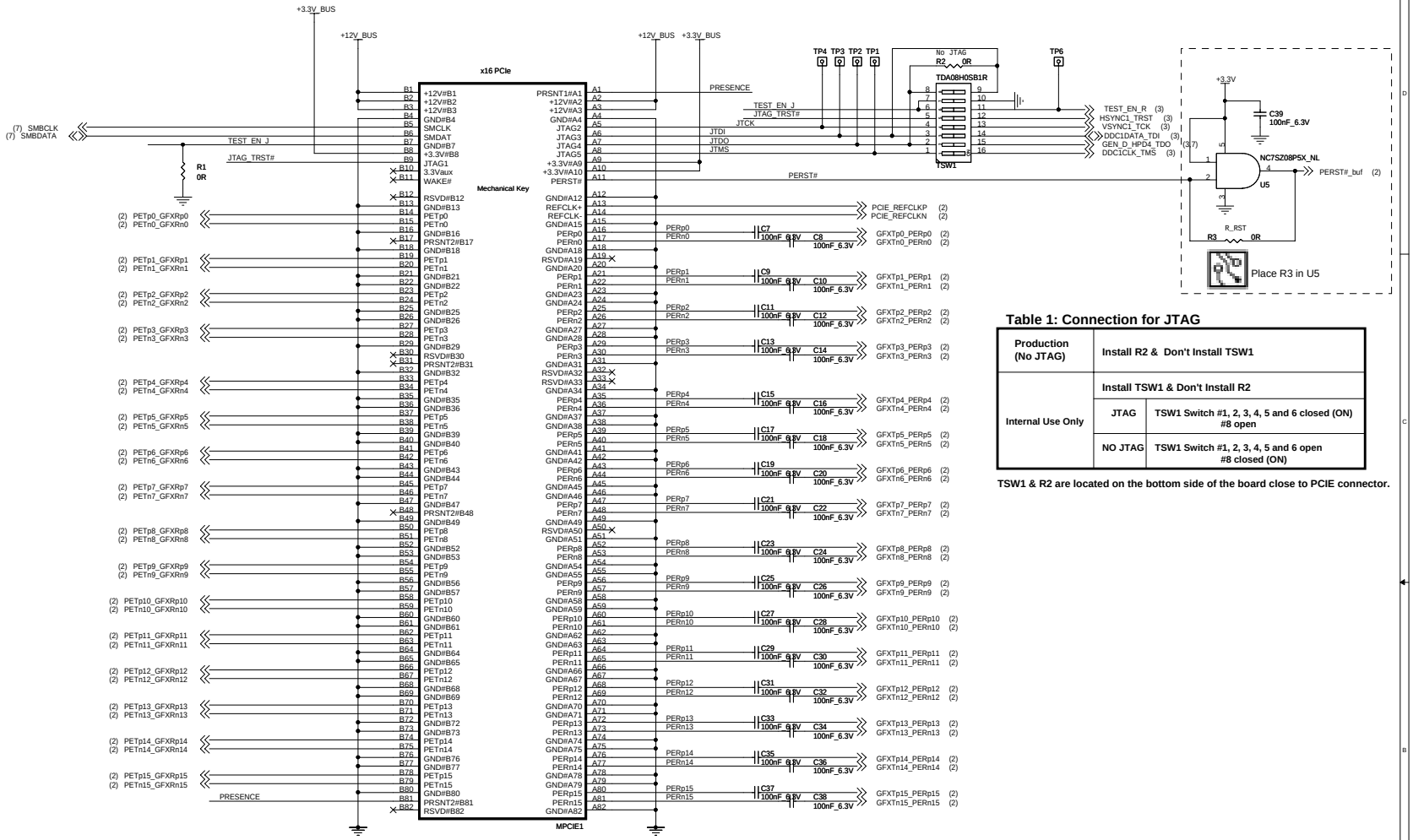


Table 1: Connection for JTAG

Production (No JTAG)	**Install R2 & Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 closed (ON)**

TSW1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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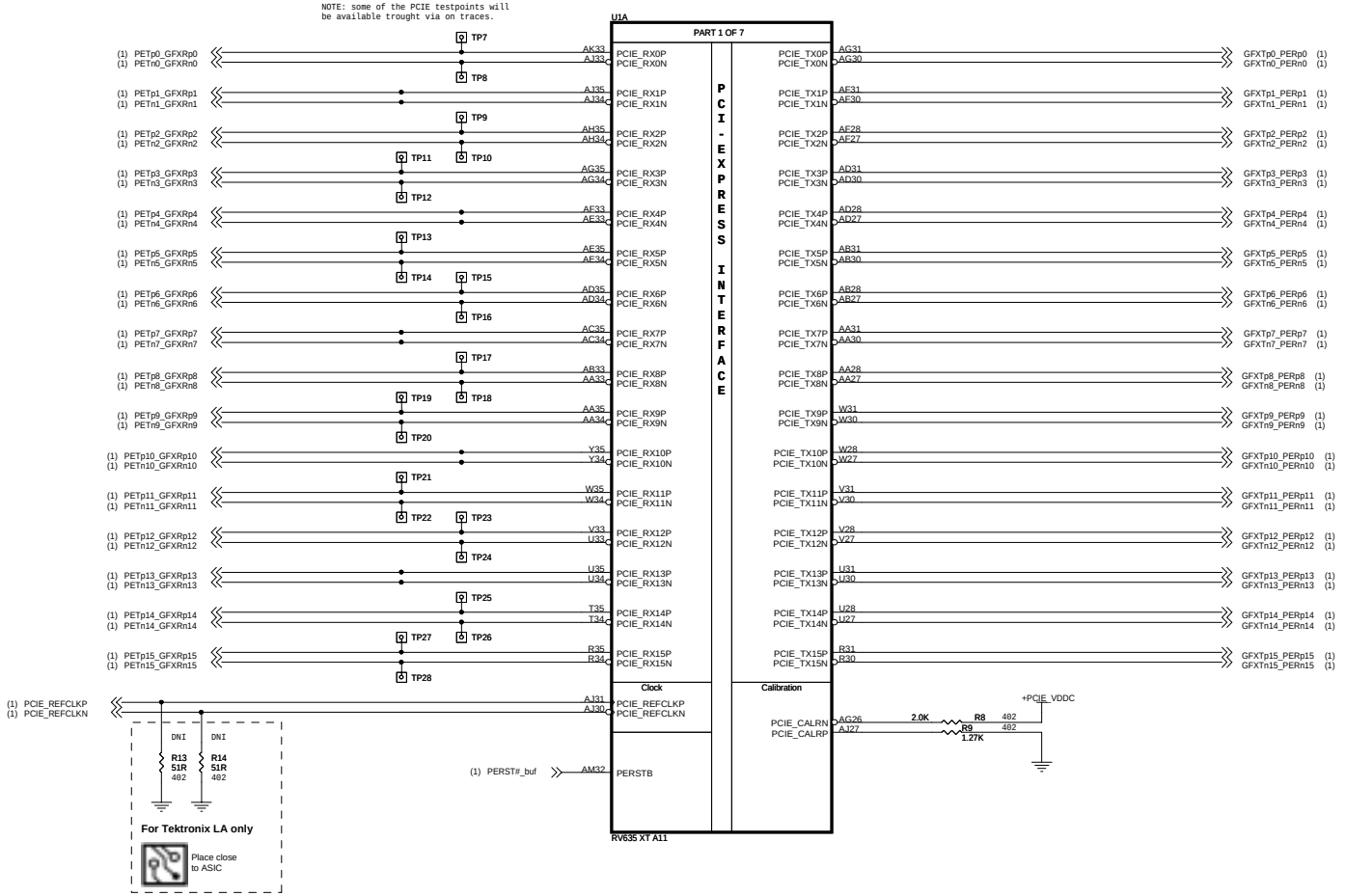
Title RV635 GDDR3 - PCI-E Edge Connector

Doc No. 105-B380xx-00



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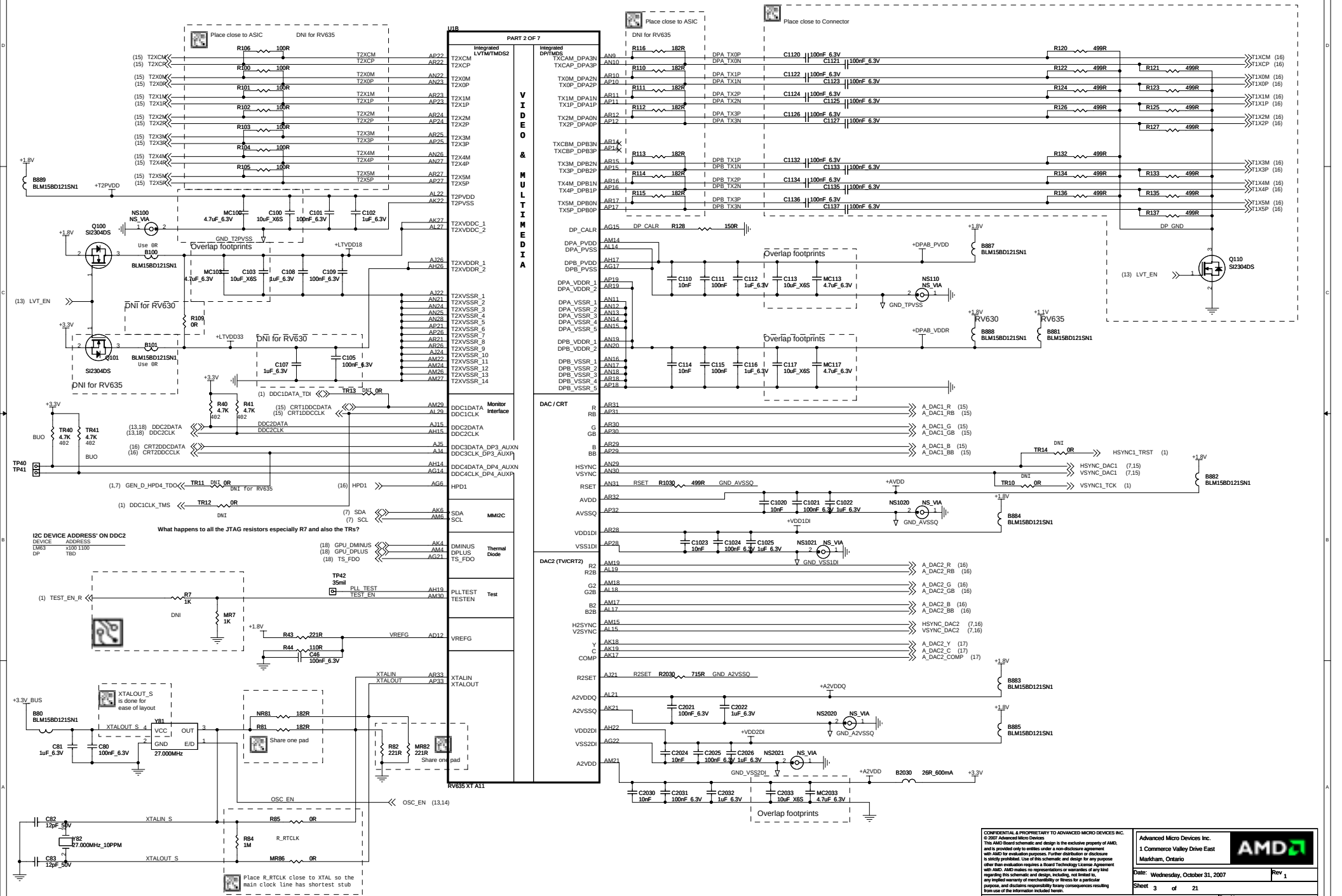
Title RV635 GDDR3 - ASIC PCIE_Interface

Doc No. 105-B380xx-00

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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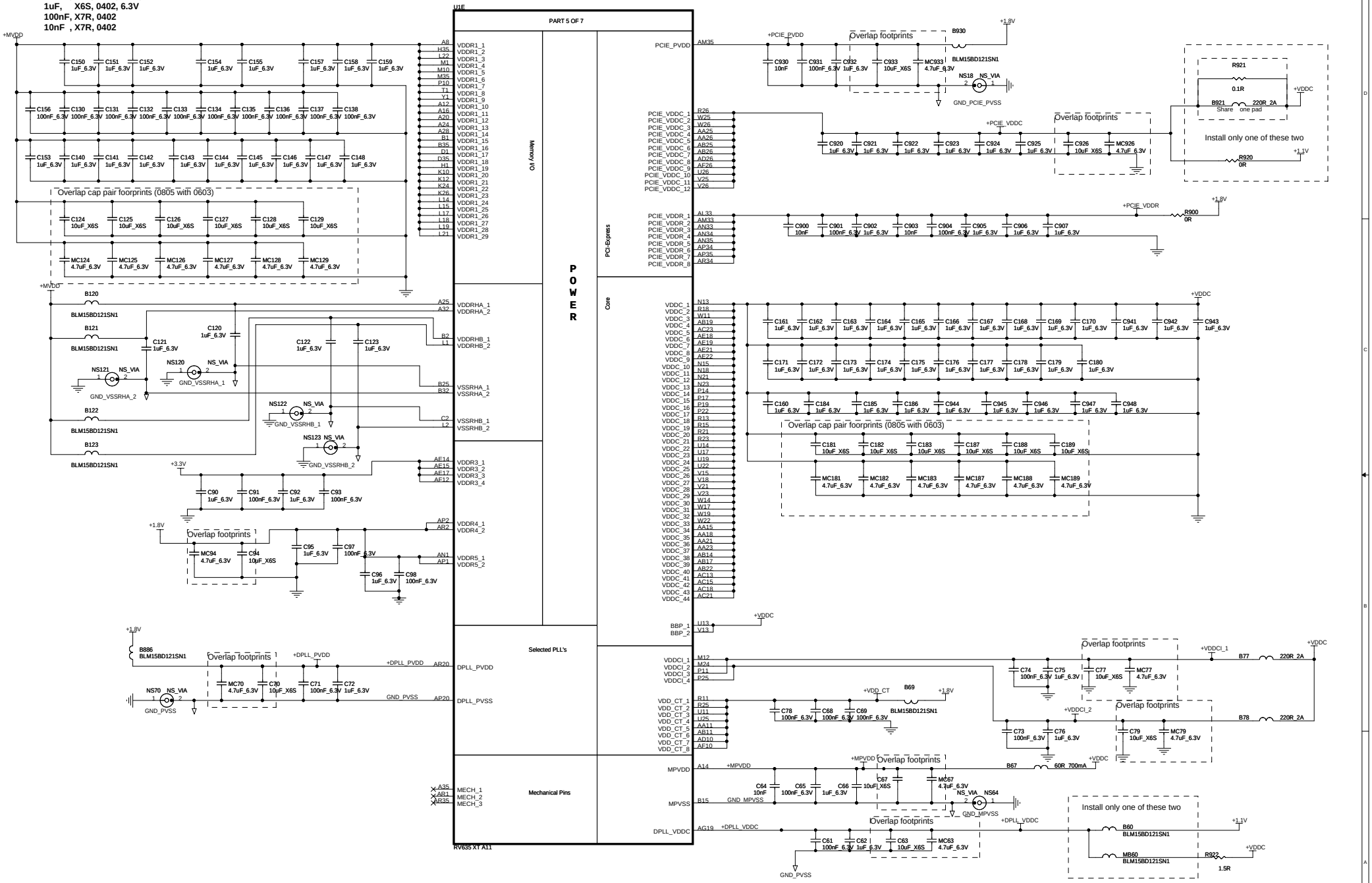
Title	RV635 GDDR3 - ASIC MAIN
Doc No.	105-B380xx-00

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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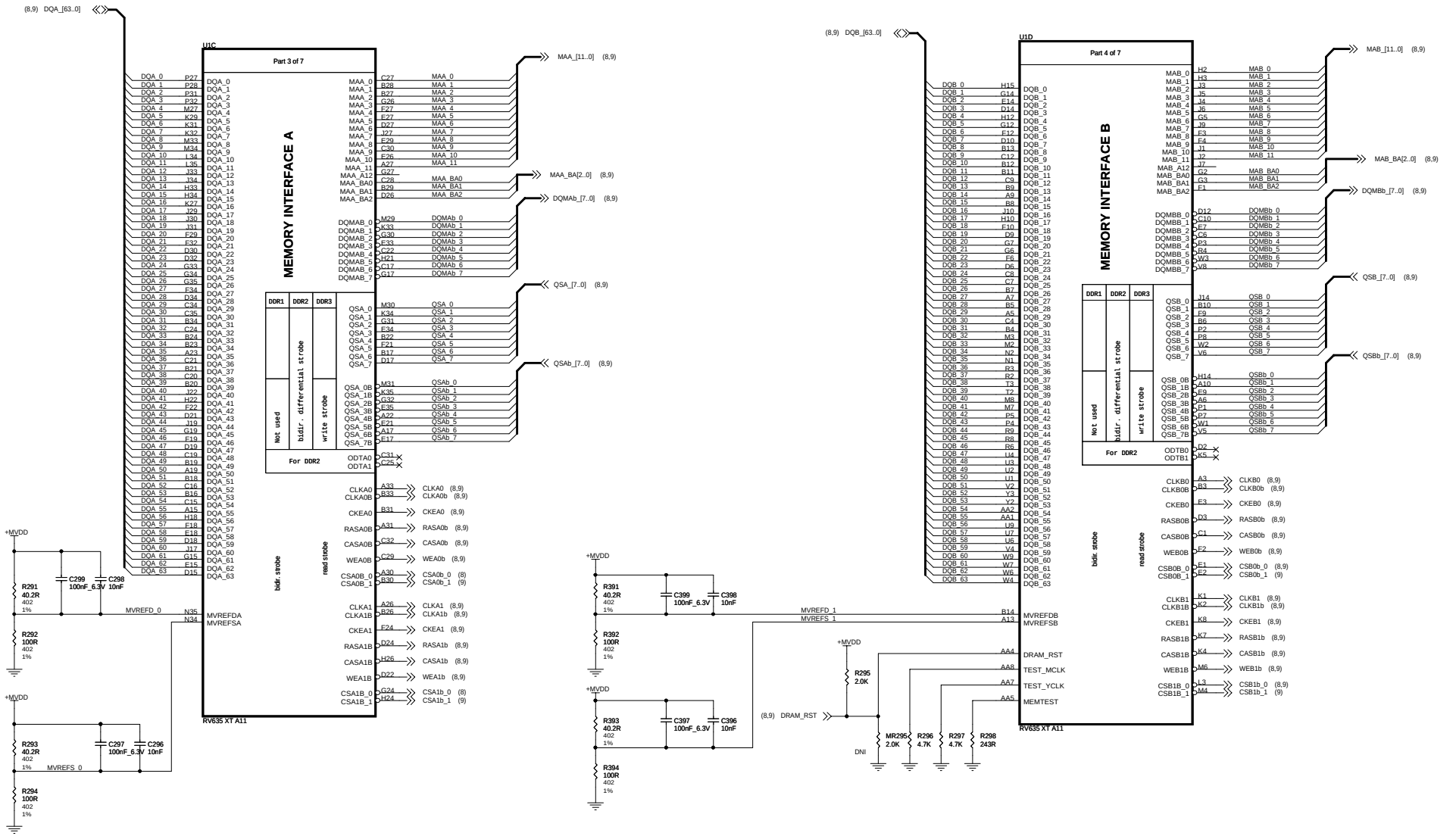
Title	RV635 GDDR3 - ASIC Power
Doc No.	105-B380xx-00



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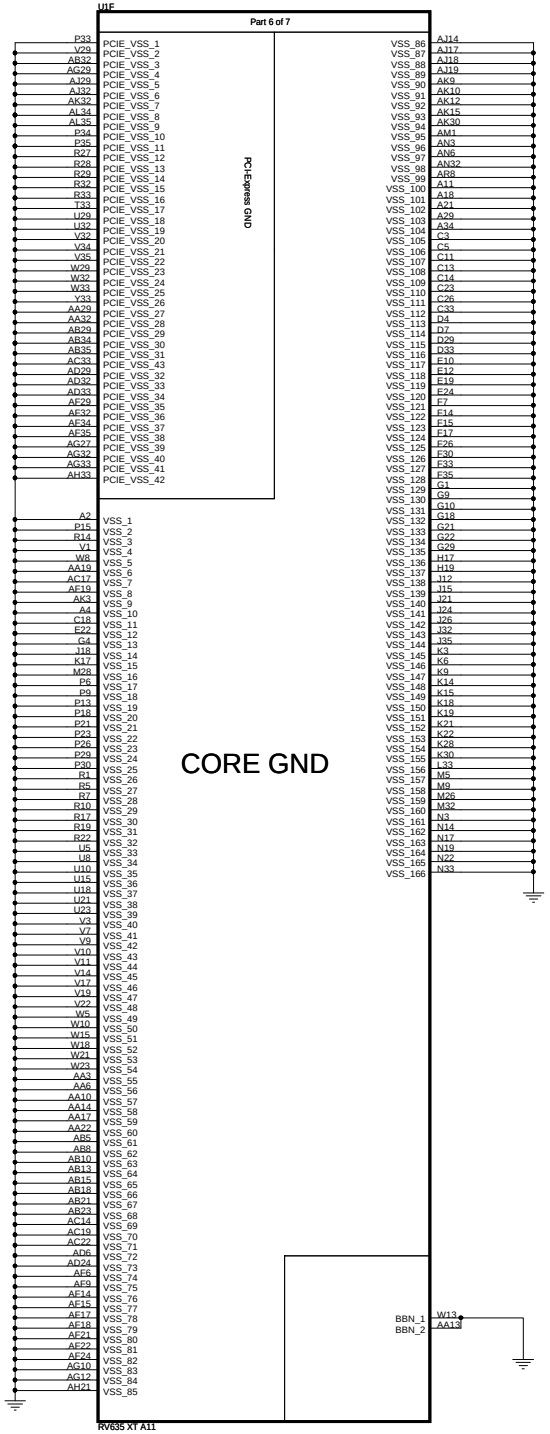
Title RV635 GDDR3 - ASIC Memory Interface (Channel A & B) Doc No. 105-B380xx-00



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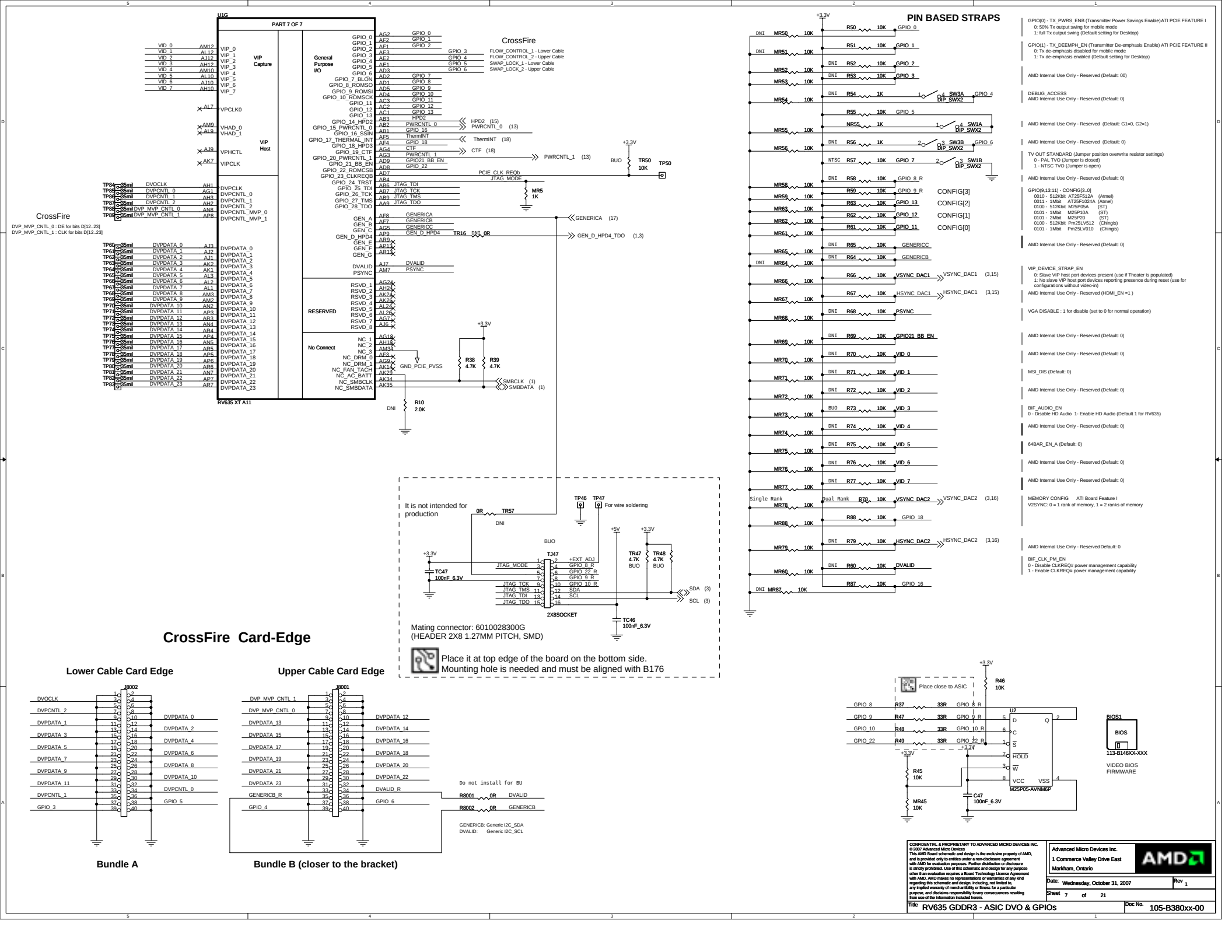
Title RV635 GDDR3 - ASIC Grounds

Doc No. 105-B380xx-00


U1G
PART 7 OF 7
RV635 XT A11
VIP Capture
VIP Host
General Purpose I/O
RESERVED
No Connect
CrossFire
PIN BASED STRAPS
CrossFire Card-Edge
Lower Cable Card Edge
Upper Cable Card Edge
Bundle A
Bundle B (closer to the bracket)
It is not intended for production
For wire soldering
Mating connector: 6010028300G
(HEADER 2X8 1.27MM PITCH, SMD)
Place it at top edge of the board on the bottom side.
Mounting hole is needed and must be aligned with B176
Place close to ASIC
BIOS1
113-B146XX-XXX
VIDEO BIOS FIRMWARE
M25P05-AVNM6P
Do not install for BU
GENERICB: Generic I2C_SDA
DVALID: Generic I2C_SCL
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Markham, Ontario
Date: Wednesday, October 31, 2007
Rev 1
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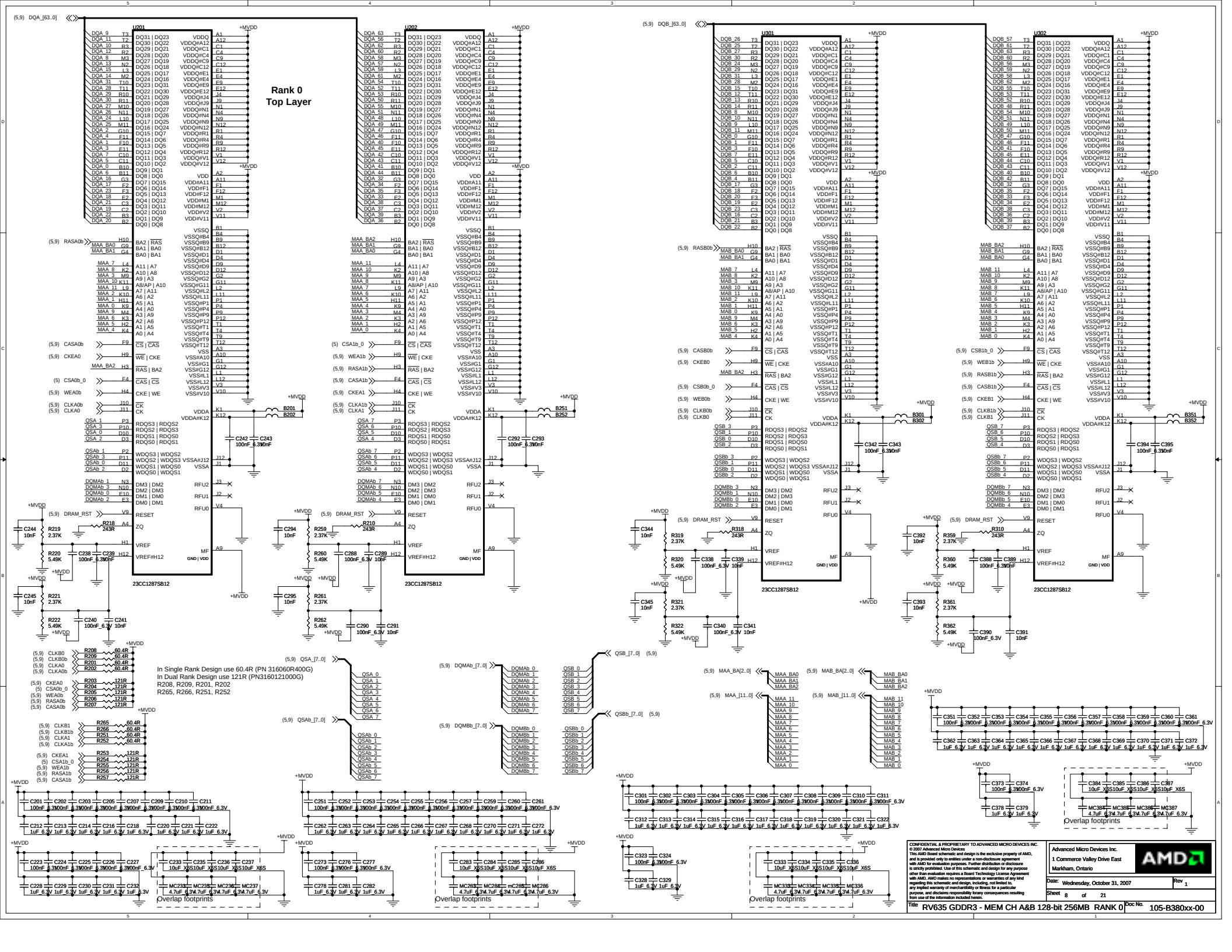
Title RV635 GDDR3 - ASIC DVO & GPIOs
Doc No. 105-B380xx-00


Rank 0
Top Layer
U201
U202
U301
U302
23CC1287SB12
In Single Rank Design use 60.4R (PN 316060R400G)
In Dual Rank Design use 121R (PN3160121000G)
R208, R209, R201, R202
R265, R266, R251, R252
Overlap footprints
Overlap footprints
Overlap footprints
Overlap footprints
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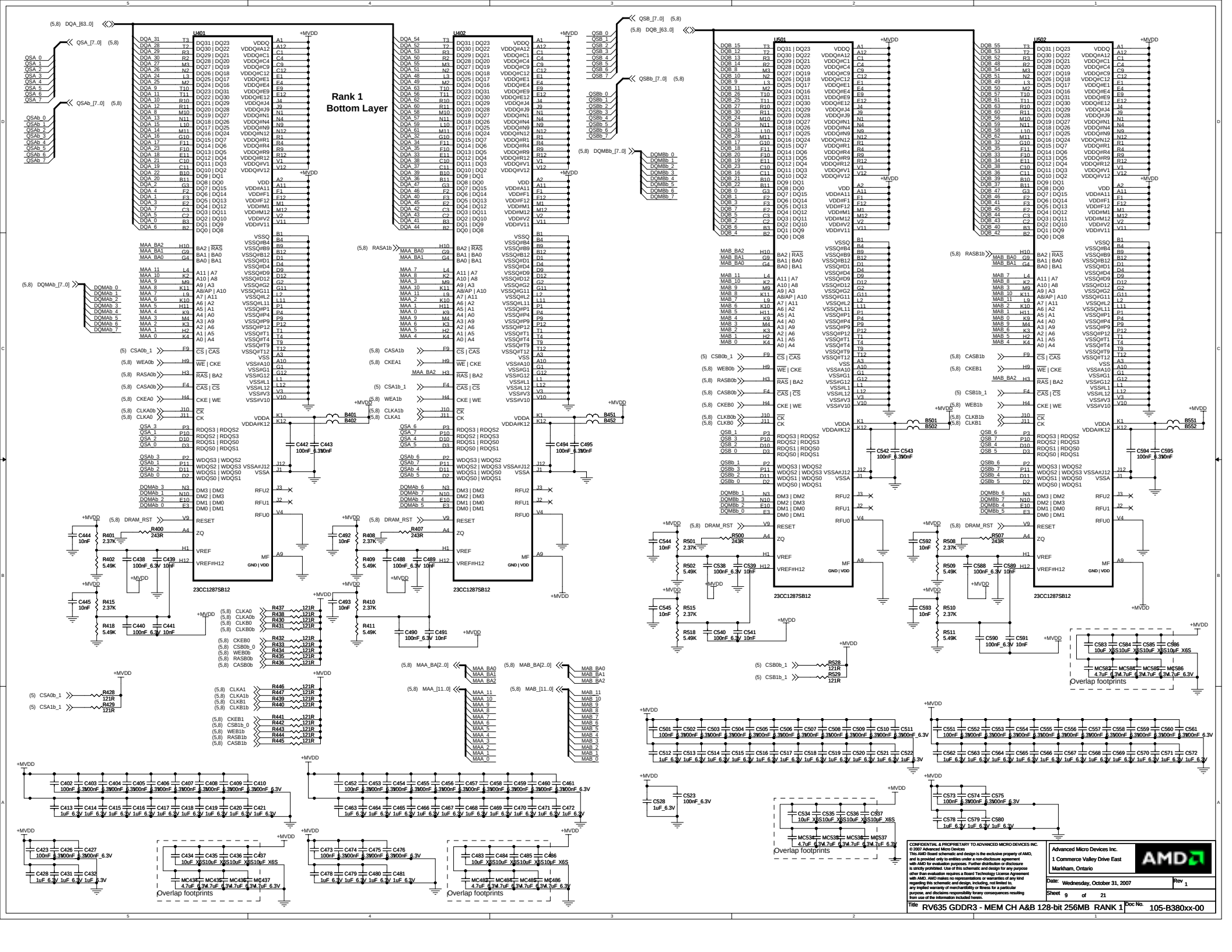
Title RV635 GDDR3 - MEM CH A&B 128-bit 256MB RANK 0
Doc No. 105-B380xx-00



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Title RV635 GDDR3 - MEM CH A&B 128-bit 256MB RANK 1
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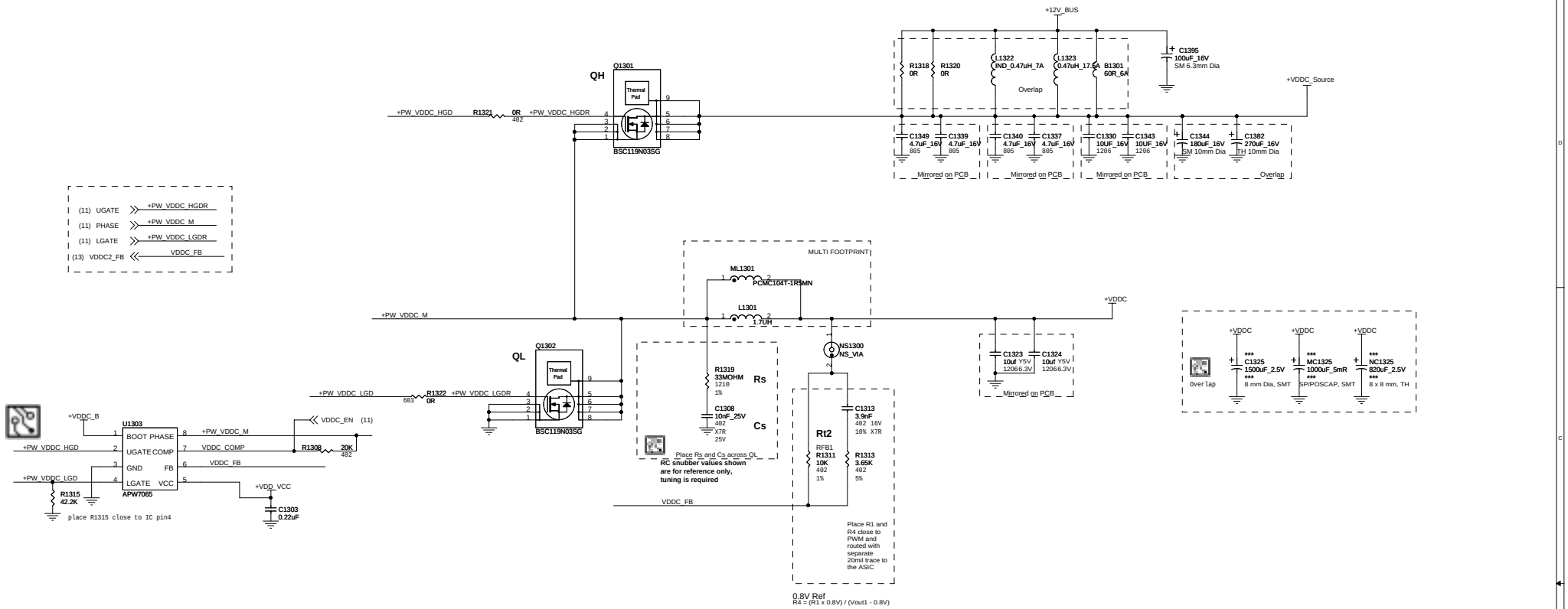
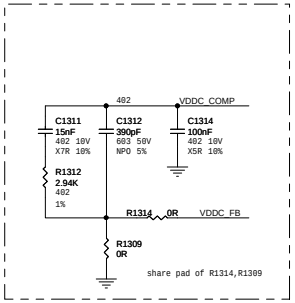
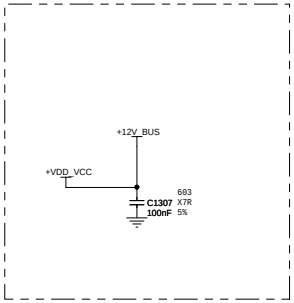


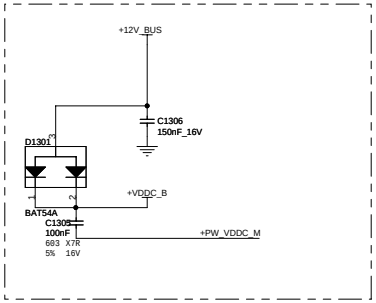
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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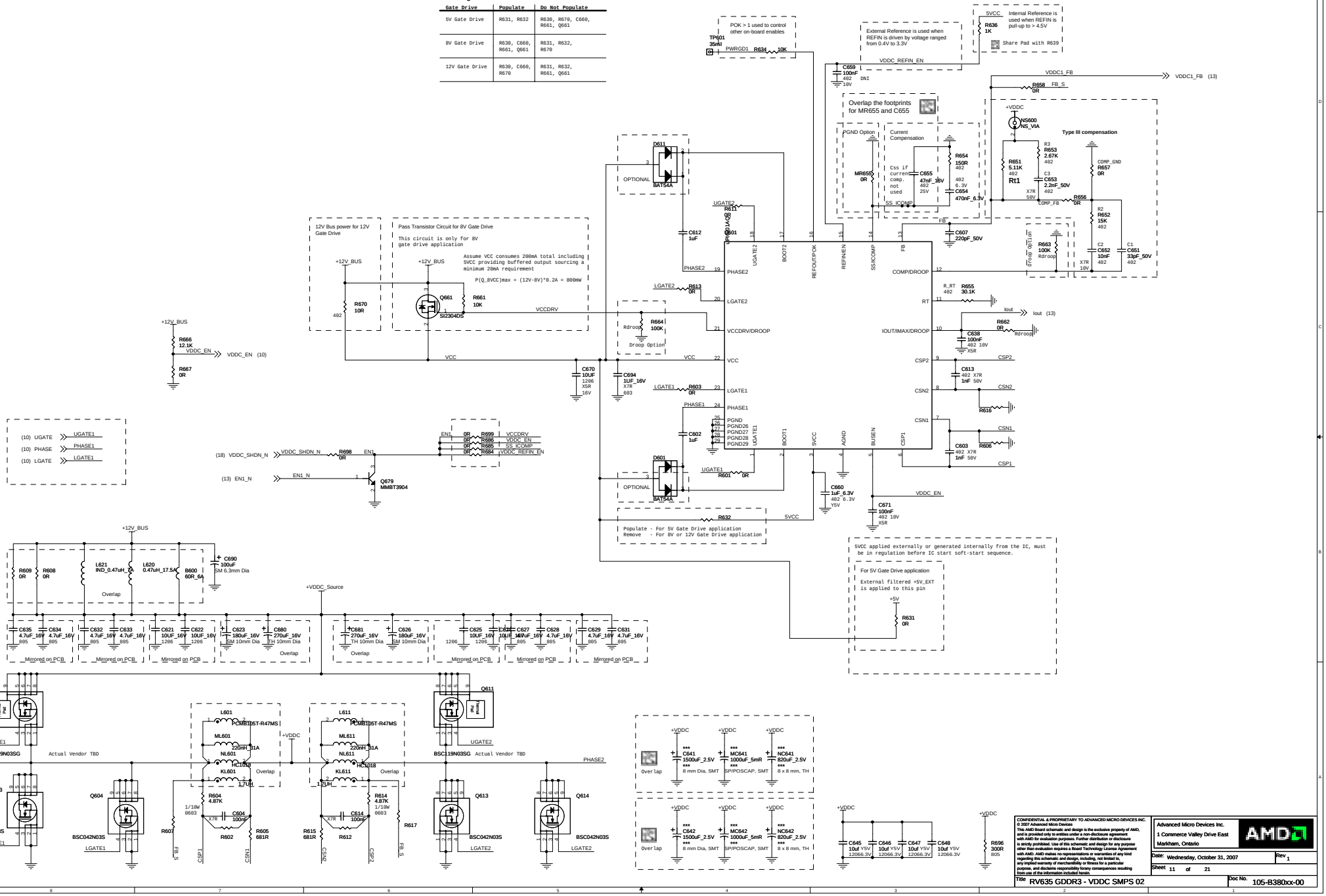
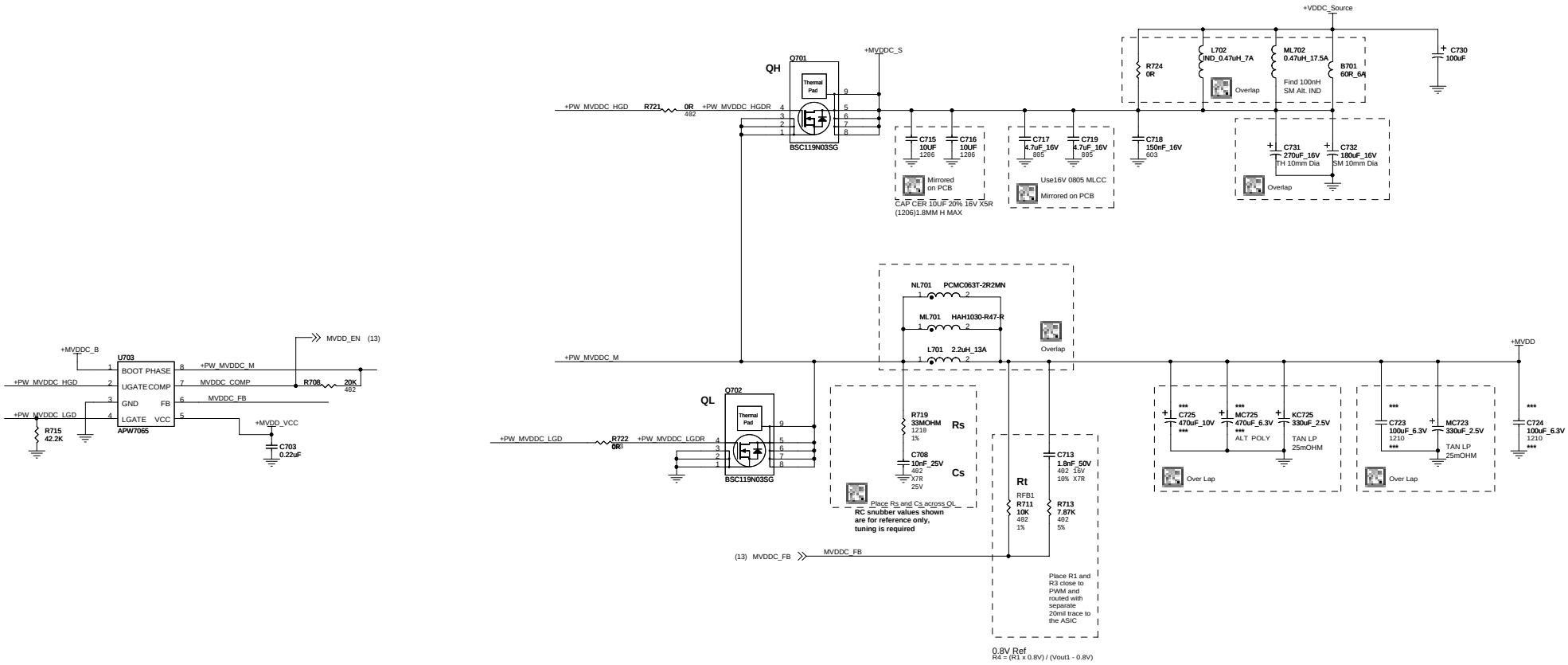
Title	RV635 GDDR3 - VDDC SMPS 01
Doc No.	105-B380xx-00

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661





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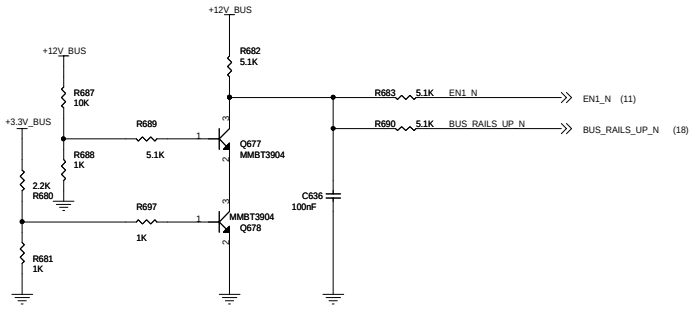
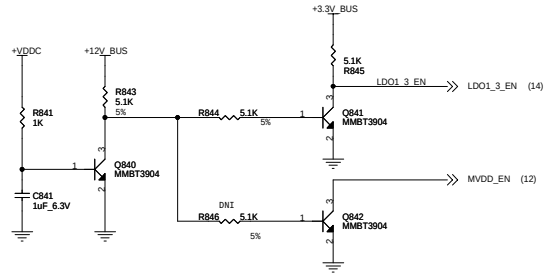
Title RV635 GDDR3 - MVDD SMPS 01

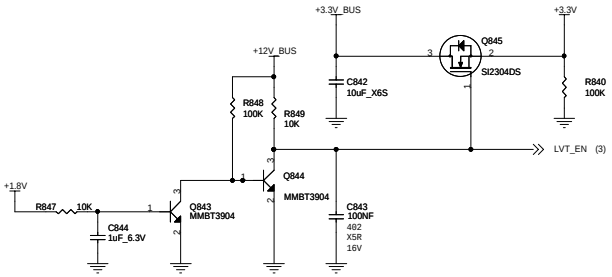
Doc No. 105-B380xx-00

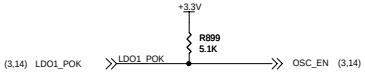
Power up Sequencing



VDDC Enable Circuit





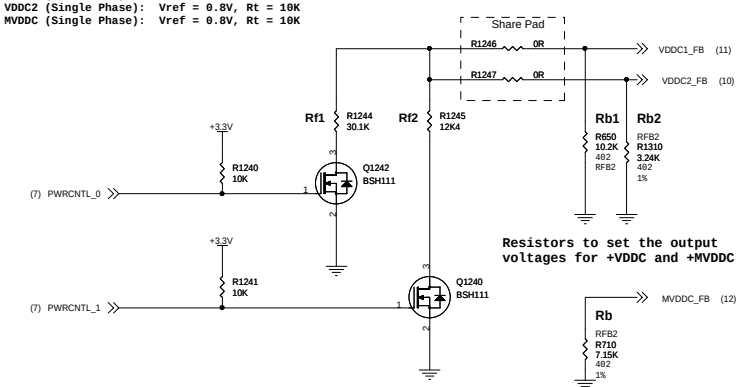


Power Play

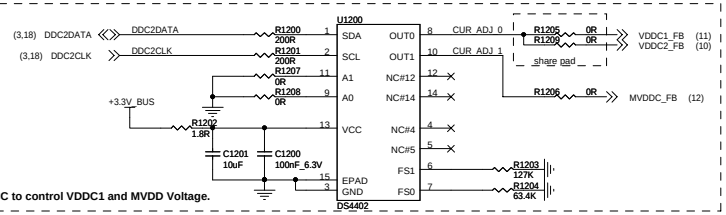
VDDC Voltage Settings Using GPIOs (for VDDC1 Dual Phase)

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1=42.2K Rf2=20.5K	Rf1= Rf2=	Rf1= Rf2=	
0	0	0.90V			
0	1	1.00V			
1	0	1.15V			
1	1	1.25V			Power-up Default

Vout = Vref * (1+Rt/Rb)
VDDC1 (Dual Phase): Vref = 0.6V, Rt = 5.11K
VDDC2 (Single Phase): Vref = 0.8V, Rt = 10K
MVDDC (Single Phase): Vref = 0.8V, Rt = 10K

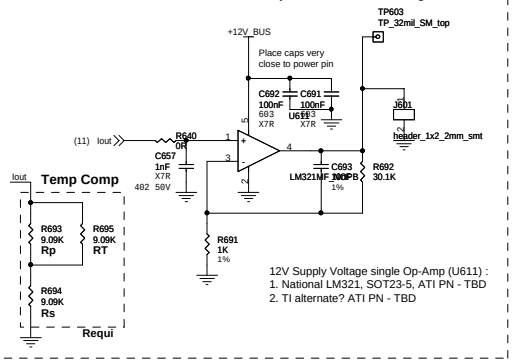


Resistors to set the output voltages for +VDDC and +MVDDC



DCC to control VDDC1 and MVDD Voltage.

Buffered VDDC Output Current Monitoring



12V Supply Voltage single Op-Amp (U611) :
1. National LM321, SOT23-5, ATI PN - TBD
2. TI alternate? ATI PN - TBD

132-
For Testing purposes only

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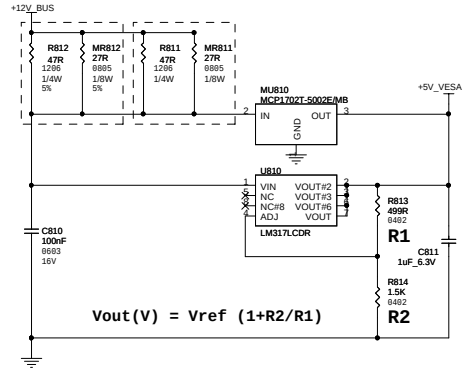
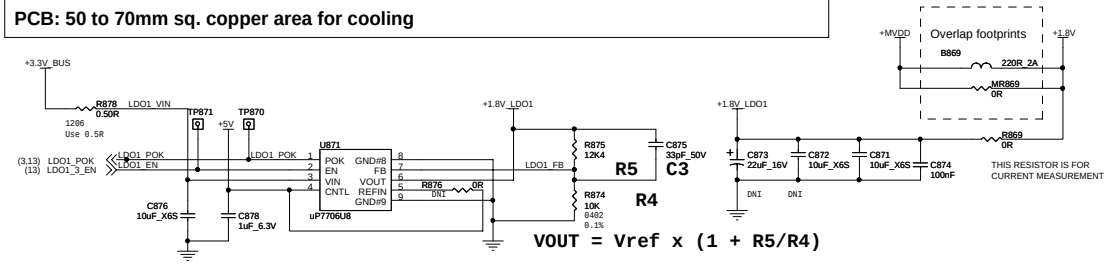
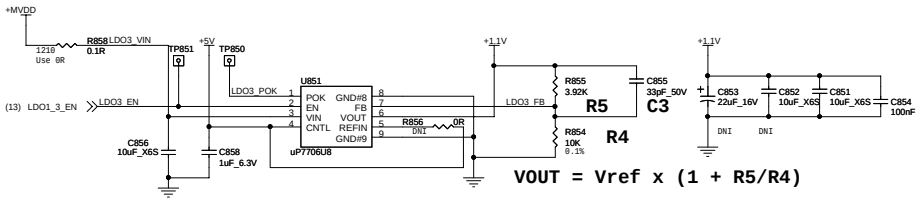
Regulators for +5V, +5V_VESA and +5V_VESA2

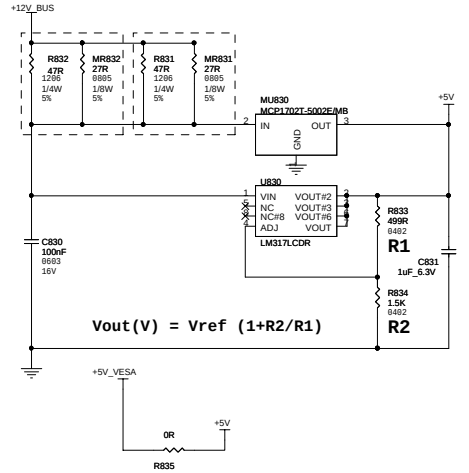


LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #3: Vin = +1.45V to 2.0VMAX Vout = +1.1V +/- 2% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling





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Title RV635 GDDR3 - Linear Regulators
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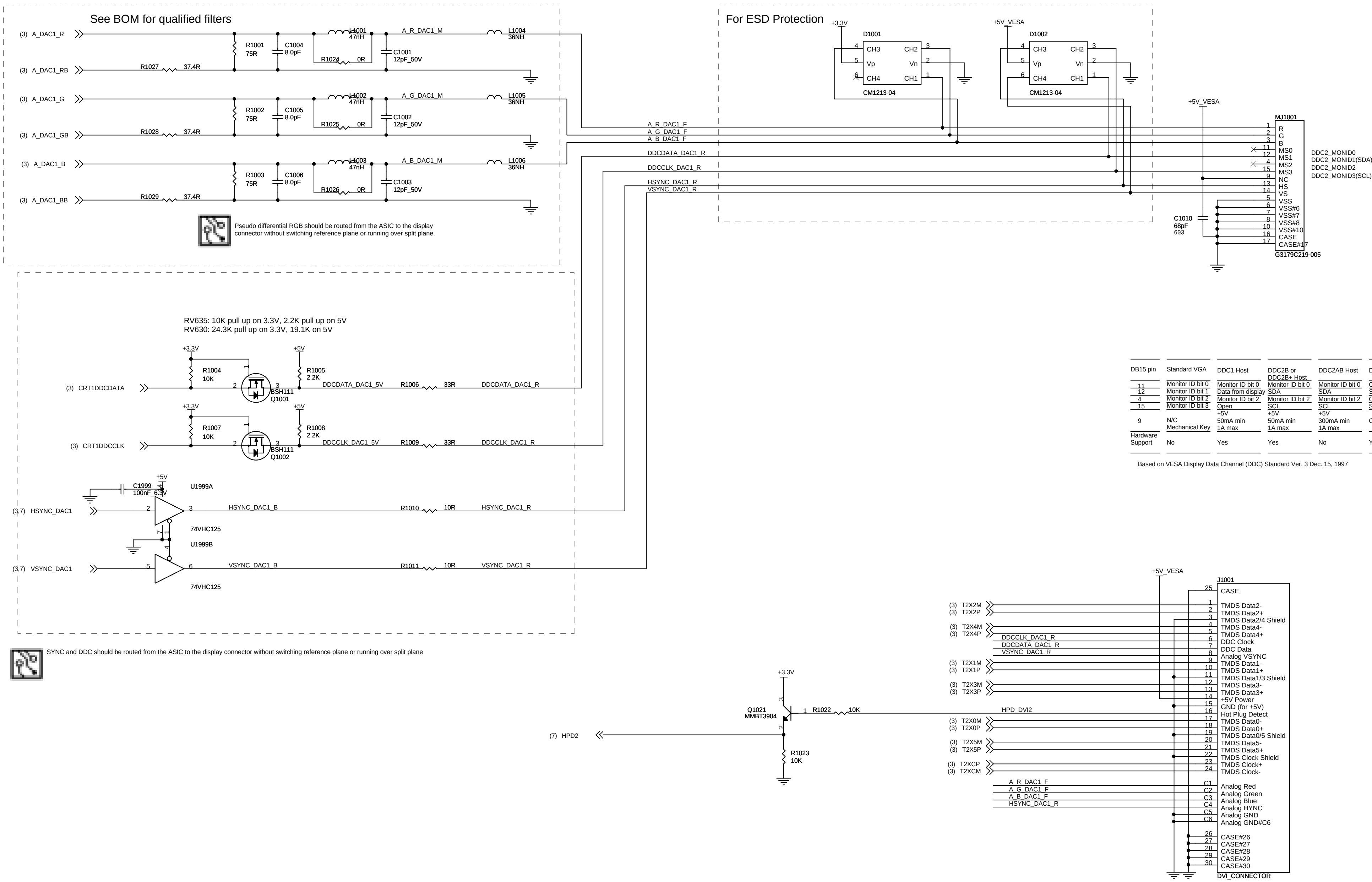
See BOM for qualified filters
For ESD Protection
(3) A_DAC1_R
(3) A_DAC1_RB
(3) A_DAC1_G
(3) A_DAC1_GB
(3) A_DAC1_B
(3) A_DAC1_BB
R1001 75R
C1004 8.0pF
L1001 47nH
R1024 0R
C1001 12pF_50V
A_R_DAC1_M
L1004 36NH
R1027 37.4R
R1002 75R
C1005 8.0pF
L1002 47nH
R1025 0R
C1002 12pF_50V
A_G_DAC1_M
L1005 36NH
R1028 37.4R
R1003 75R
C1006 8.0pF
L1003 47nH
R1026 0R
C1003 12pF_50V
A_B_DAC1_M
L1006 36NH
R1029 37.4R
Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.
+3.3V
D1001
CH3 CH2 Vp Vn CH4 CH1
CM1213-04
+5V_VESA
D1002
CM1213-04
A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R
+5V_VESA
MJ1001
R G B MS0 MS1 MS2 MS3 NC HS VS VSS VSS#6 VSS#7 VSS#8 VSS#10 CASE CASE#17
DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)
C1010 68pF 603
G3179C219-005
RV635: 10K pull up on 3.3V, 2.2K pull up on 5V
RV630: 24.3K pull up on 3.3V, 19.1K on 5V
(3) CRT1DDCDATA
R1004 10K
R1005 2.2K
BSH111 Q1001
DDCDATA_DAC1_5V
R1006 33R
DDCDATA_DAC1_R
(3) CRT1DDCCLK
R1007 10K
R1008 2.2K
BSH111 Q1002
DDCCLK_DAC1_5V
R1009 33R
DDCCLK_DAC1_R
C1999 100nF_6.3V
U1999A
(3,7) HSYNC_DAC1
HSYNC_DAC1_B
R1010 10R
HSYNC_DAC1_R
74VHC125
U1999B
(3,7) VSYNC_DAC1
VSYNC_DAC1_B
R1011 10R
VSYNC_DAC1_R
74VHC125
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane
+3.3V
Q1021 MMBT3904
R1022 10K
HPD_DVI2
(7) HPD2
R1023 10K
+5V_VESA
J1001
(3) T2X2M
(3) T2X2P
(3) T2X4M
(3) T2X4P
DDCCLK_DAC1_R
DDCDATA_DAC1_R
VSYNC_DAC1_R
(3) T2X1M
(3) T2X1P
(3) T2X3M
(3) T2X3P
(3) T2X0M
(3) T2X0P
(3) T2X5M
(3) T2X5P
(3) T2XCP
(3) T2XCM
A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
HSYNC_DAC1_R
CASE
TMDS Data2-
TMDS Data2+
TMDS Data2/4 Shield
TMDS Data4-
TMDS Data4+
DDC Clock
DDC Data
Analog VSYNC
TMDS Data1-
TMDS Data1+
TMDS Data1/3 Shield
TMDS Data3-
TMDS Data3+
+5V Power
GND (for +5V)
Hot Plug Detect
TMDS Data0-
TMDS Data0+
TMDS Data0/5 Shield
TMDS Data5-
TMDS Data5+
TMDS Clock Shield
TMDS Clock+
TMDS Clock-
Analog Red
Analog Green
Analog Blue
Analog HYNC
Analog GND
Analog GND#C6
CASE#26
CASE#27
CASE#28
CASE#29
CASE#30
DVI_CONNECTOR

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C Mechanical Key	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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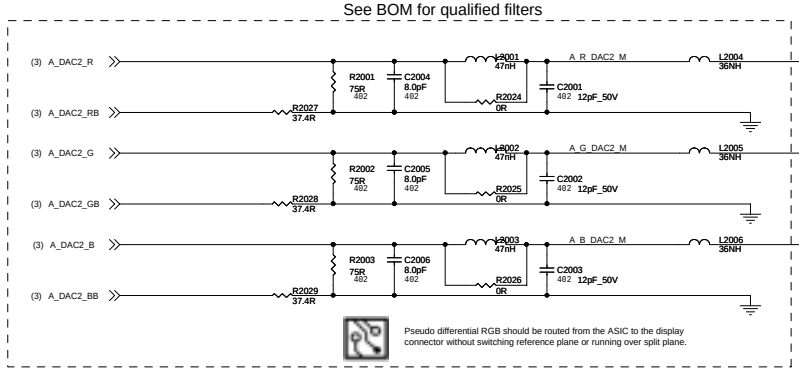
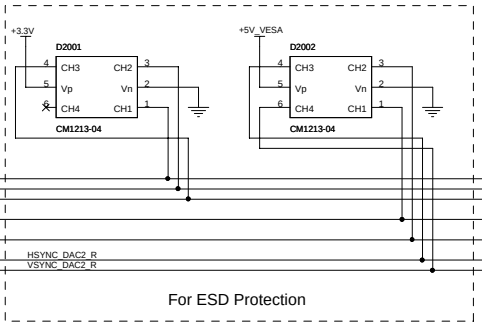
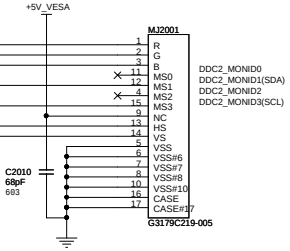
Title RV635 GDDR3 - DAC1&TMDS2 | Doc No. 105-B380xx-00

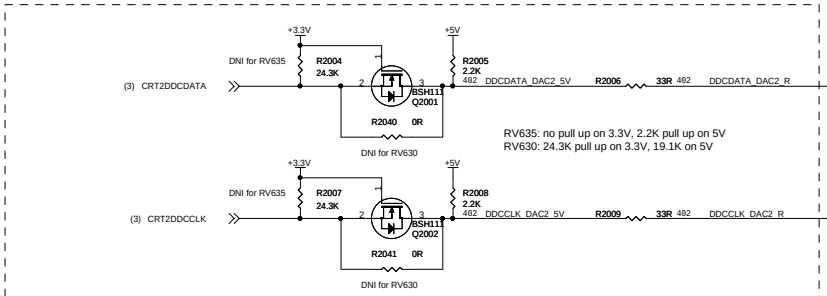
See BOM for qualified filters





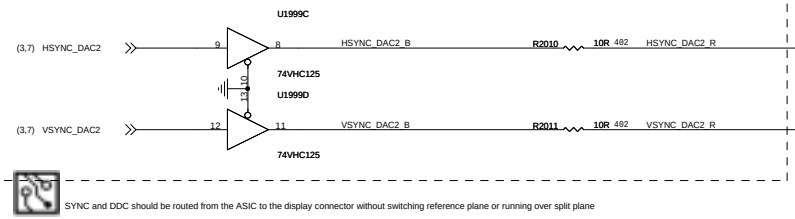


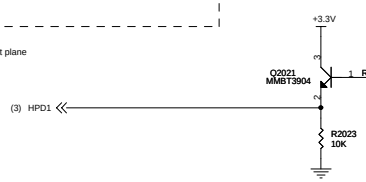
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R

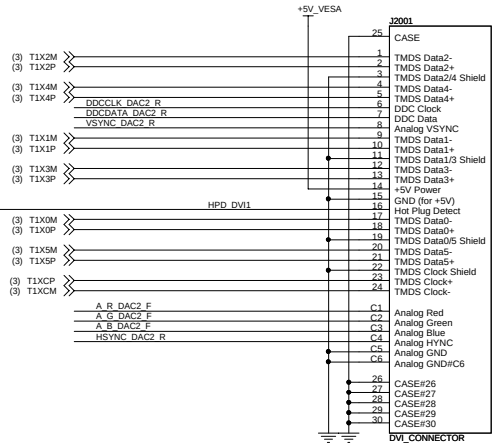


DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997







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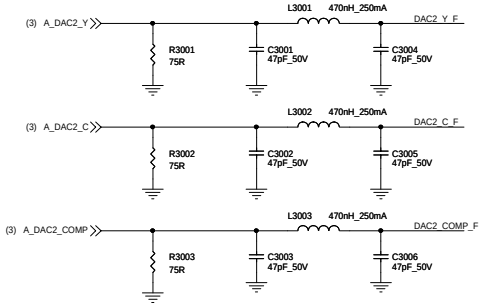

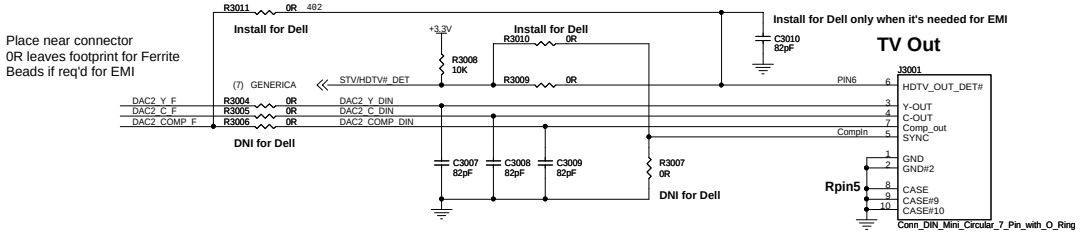

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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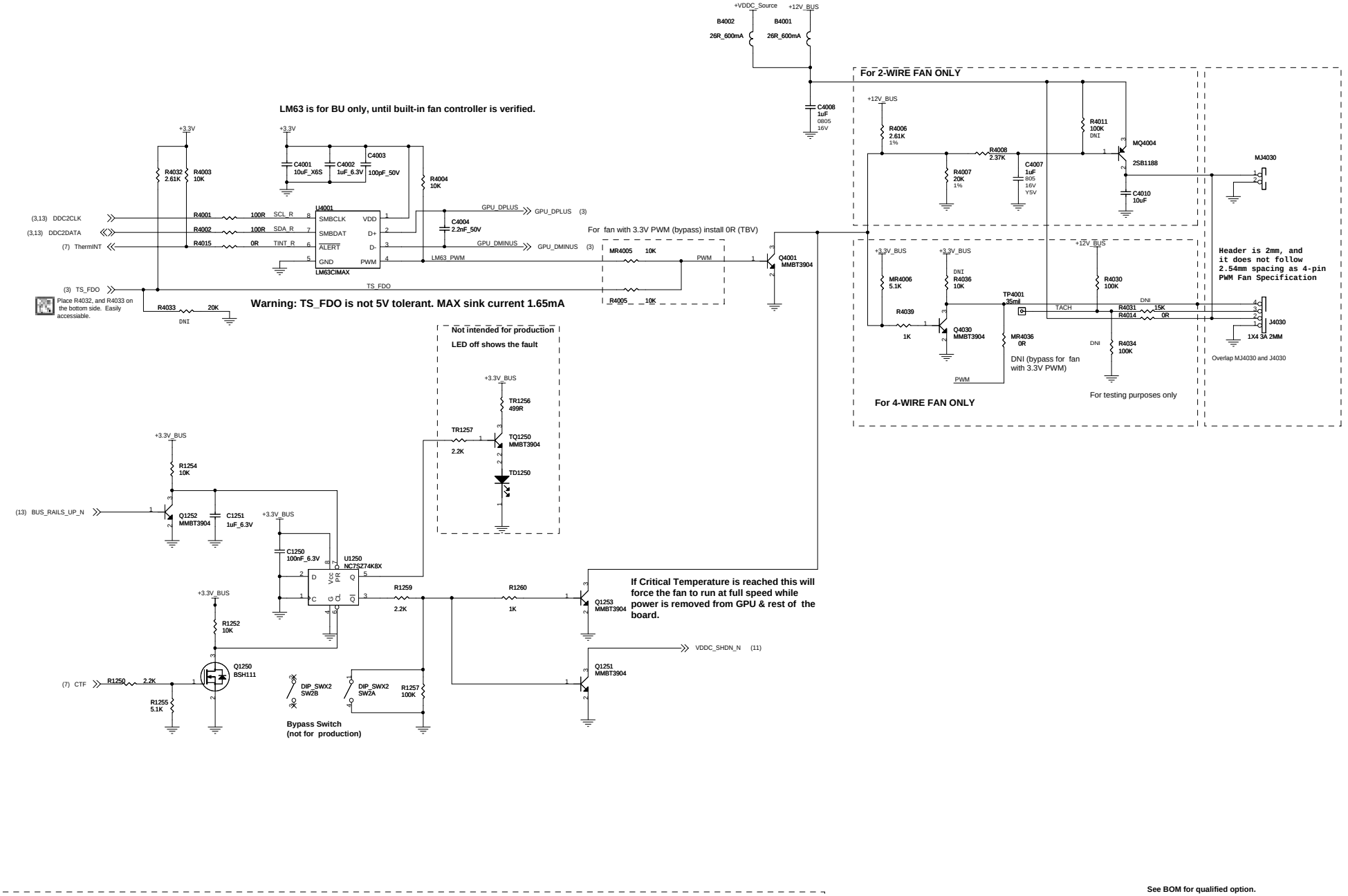

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DVI/DVI SCREWS with top tab

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

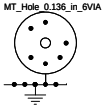
ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET
802038600G

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

MT2
MT_Hole_0.136_in_6VIA



DNI

SK1

SOCKET_880

RV635 Socket

PCB1

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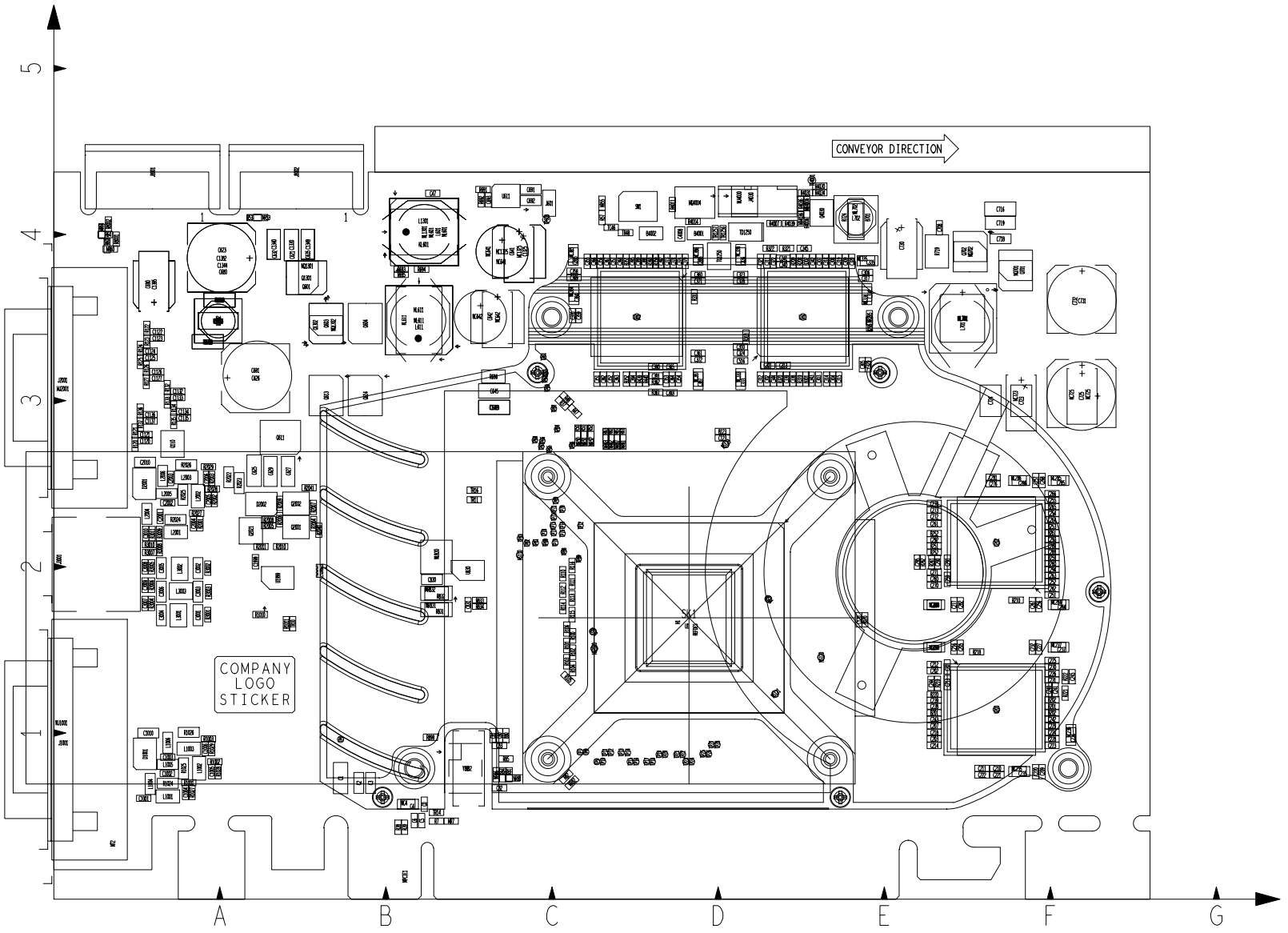

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ADVANCED MICRO DEVICES
PCBCAD GROUP

RH RV635 512MB DDR3 DL-DVI-I DL_DVI V0 FH 6"

P/N 109-B38031-00
OCT. 29 2007
SVETLANA OSTROVSKY / JASMINE

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SHEET 1 OF 2

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