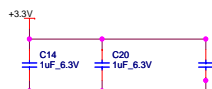
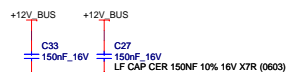
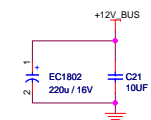
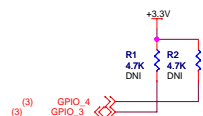


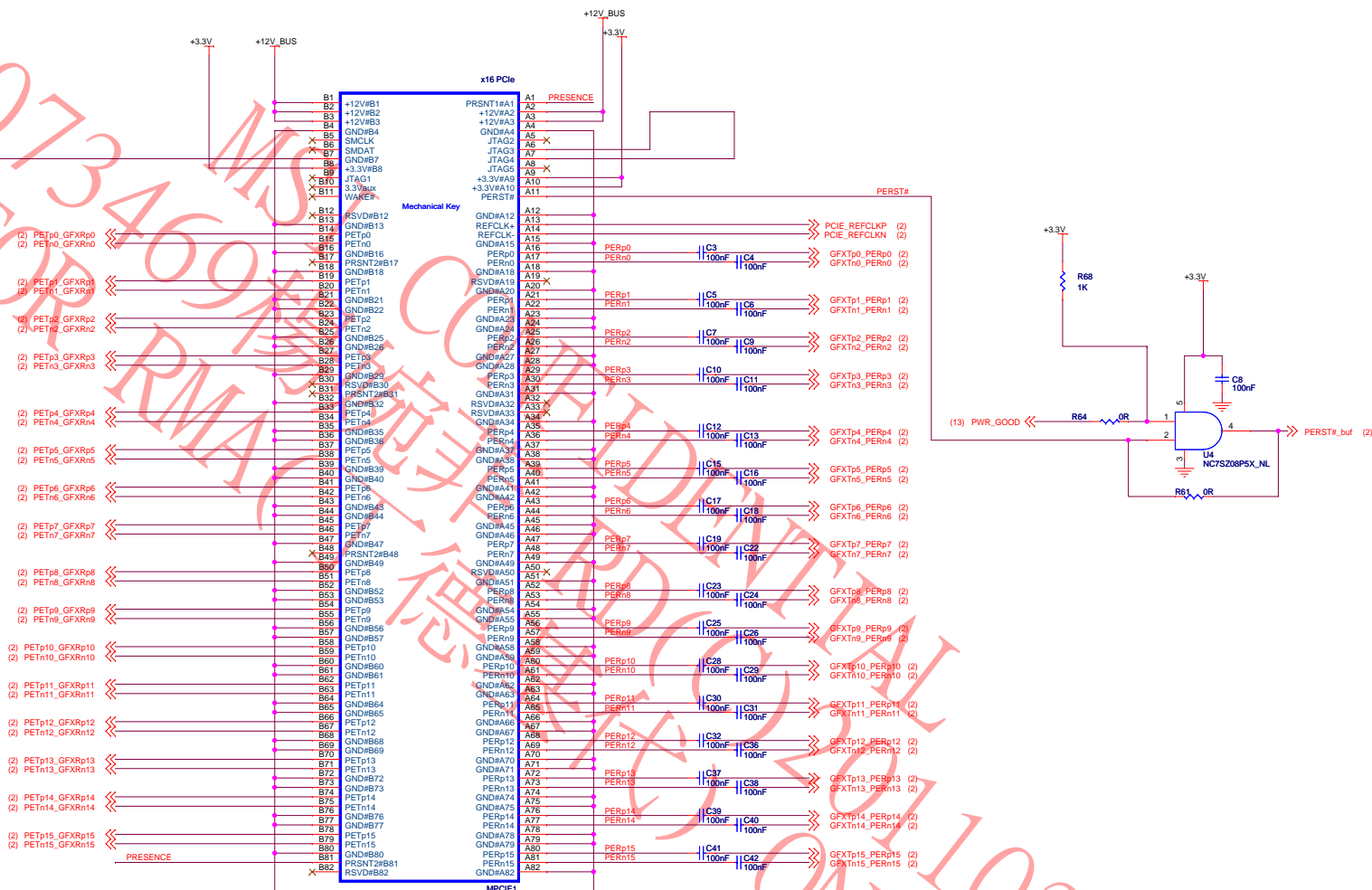
PCI-EXPRESS EDGE CONNECTOR



Place these caps last,
ideally as close to the bus
connector as possible

CAP CER 10UF 20% 16V
X5R (1206)1.6MM H MAX

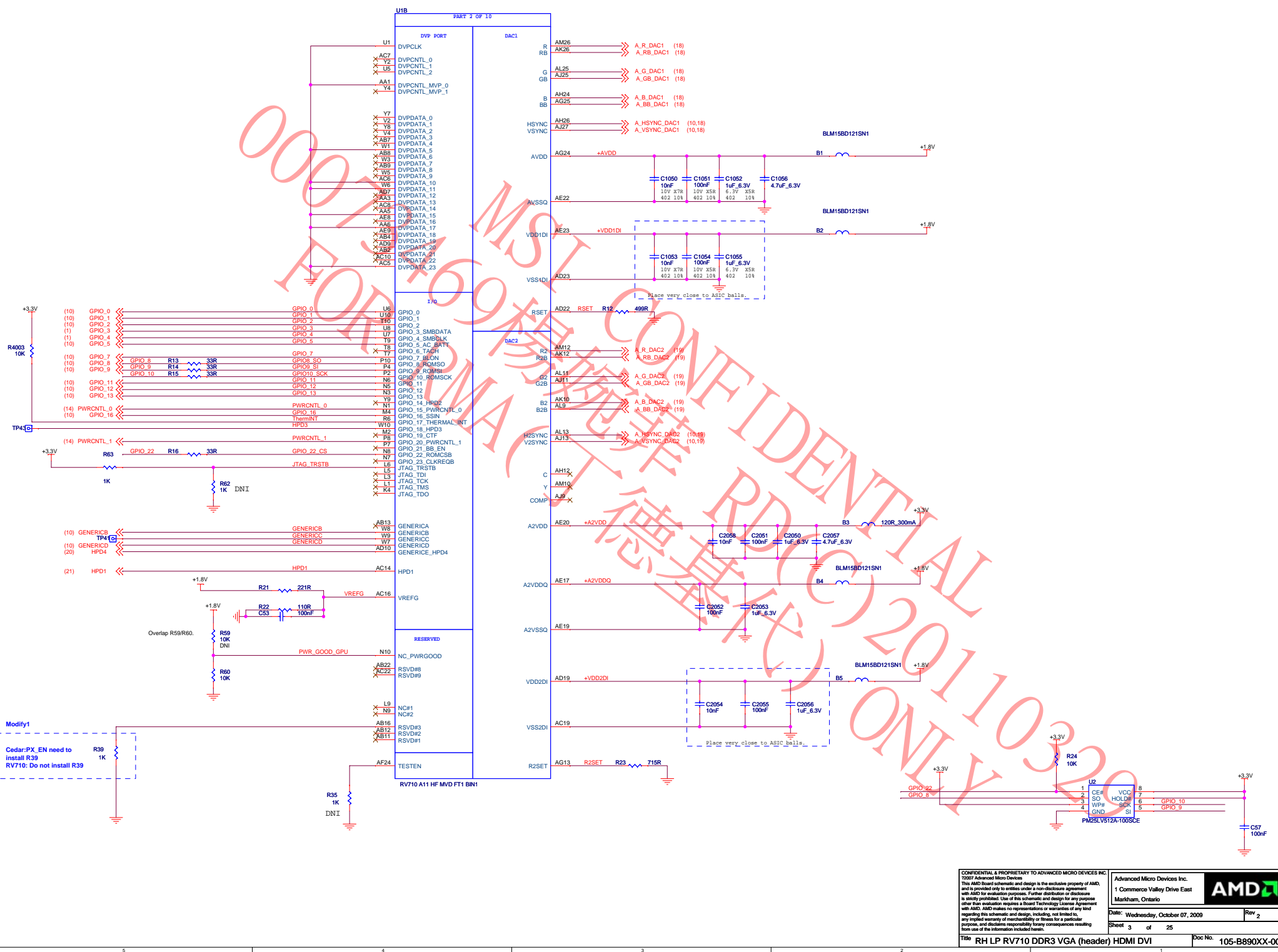
CAP CER 10UF 10% 6.3V X5R
(0805)1.6MM MAX THICK

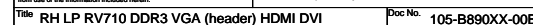


(2) RV710 PCIe Interface

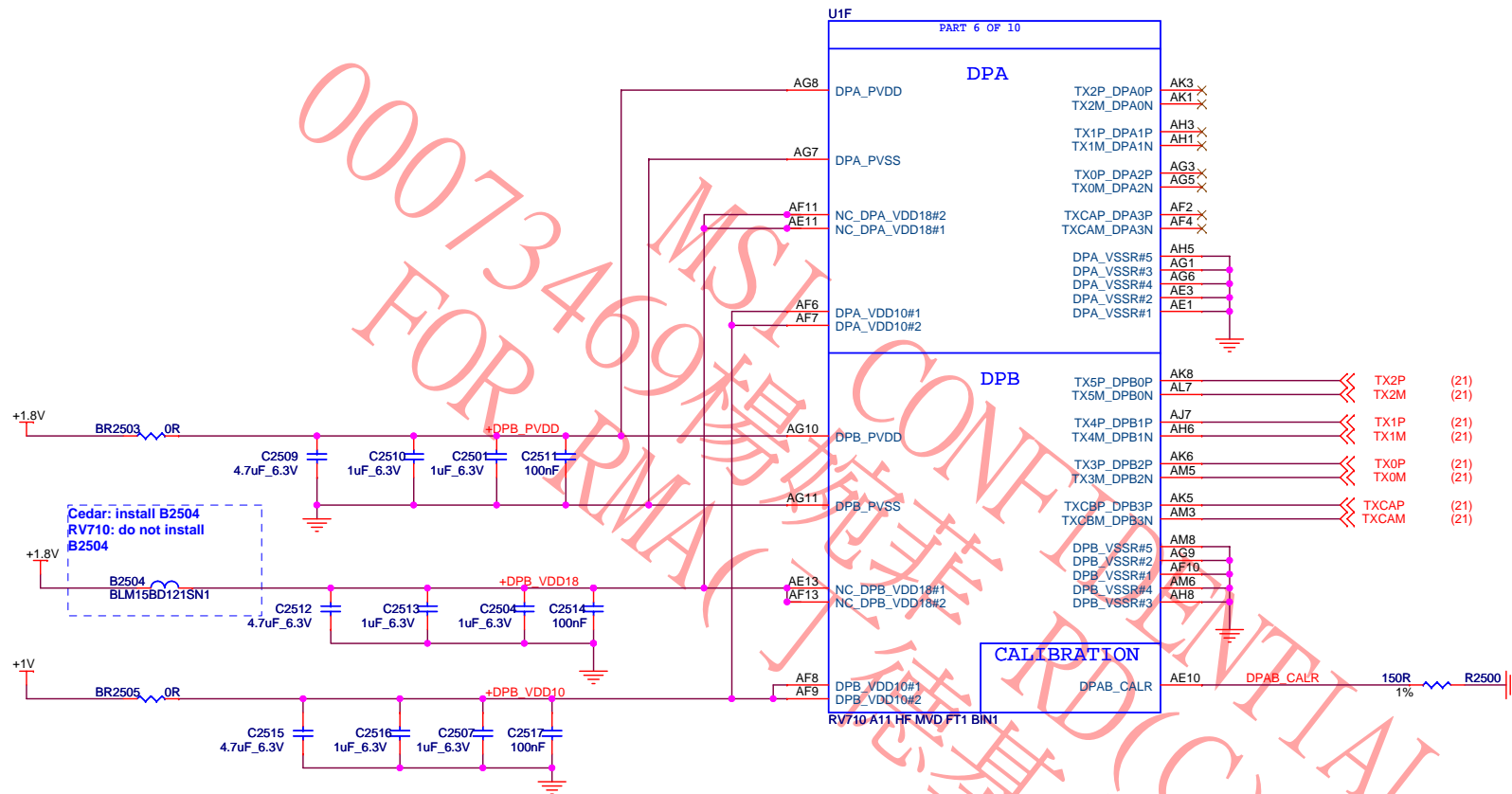


(3) RV710 Main





TMDP INTERFACE



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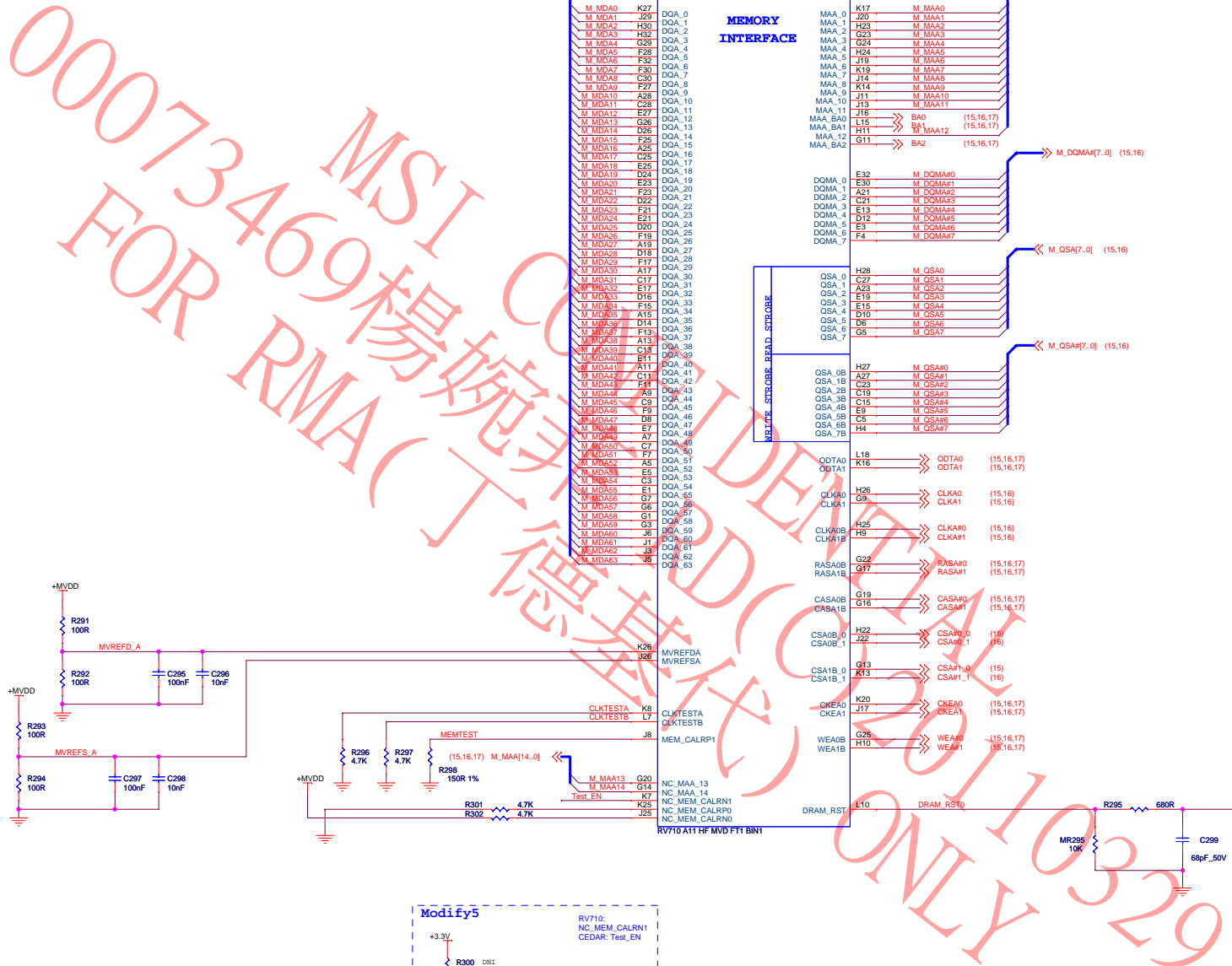
Title	RH LP RV710 DDR3 VGA (header) HDMI DVI
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Doc No.	105-B890XX-00B
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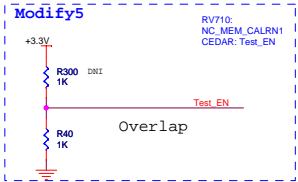


Doc No.	105-B890XX-00B
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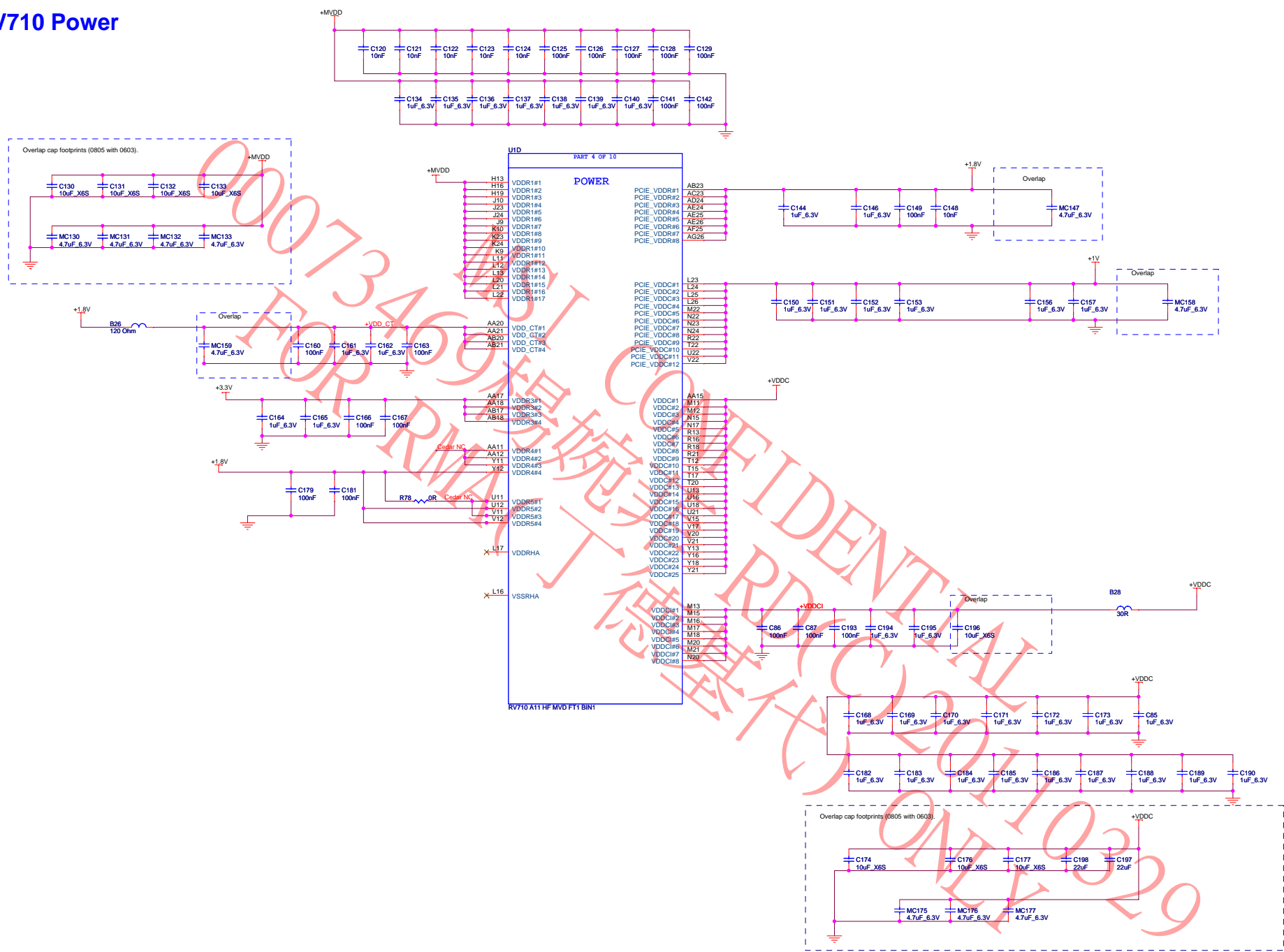
MEMORY INTERFACE



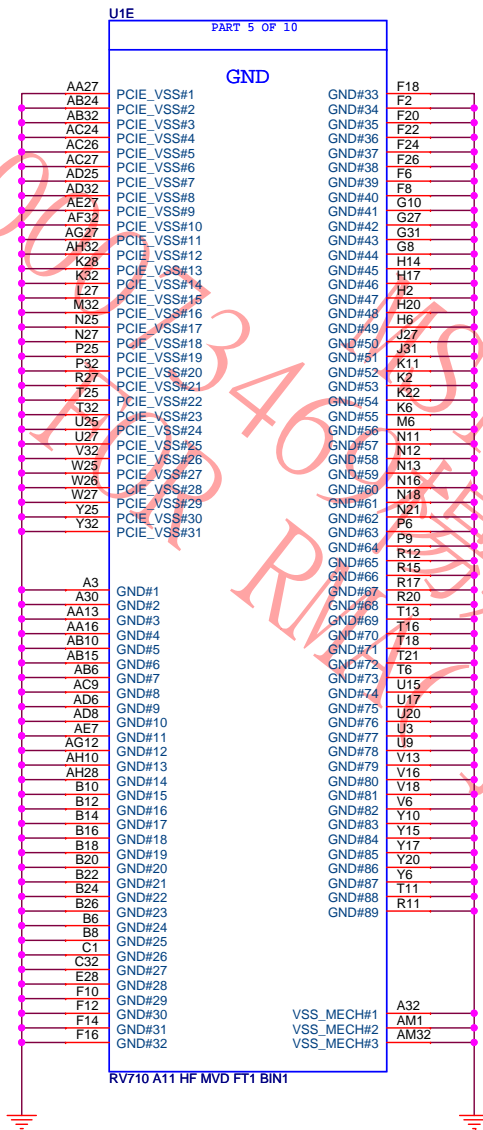
DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R



(08) RV710 Power



(09) RV710 GND

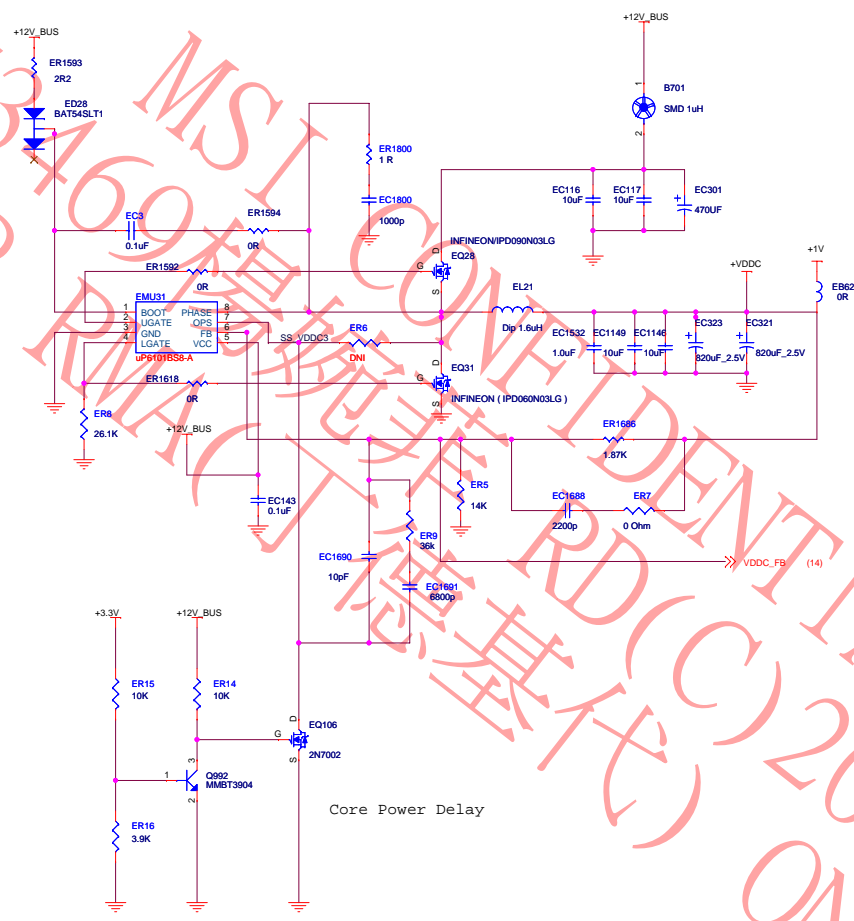


(10) RV710 STRAPS

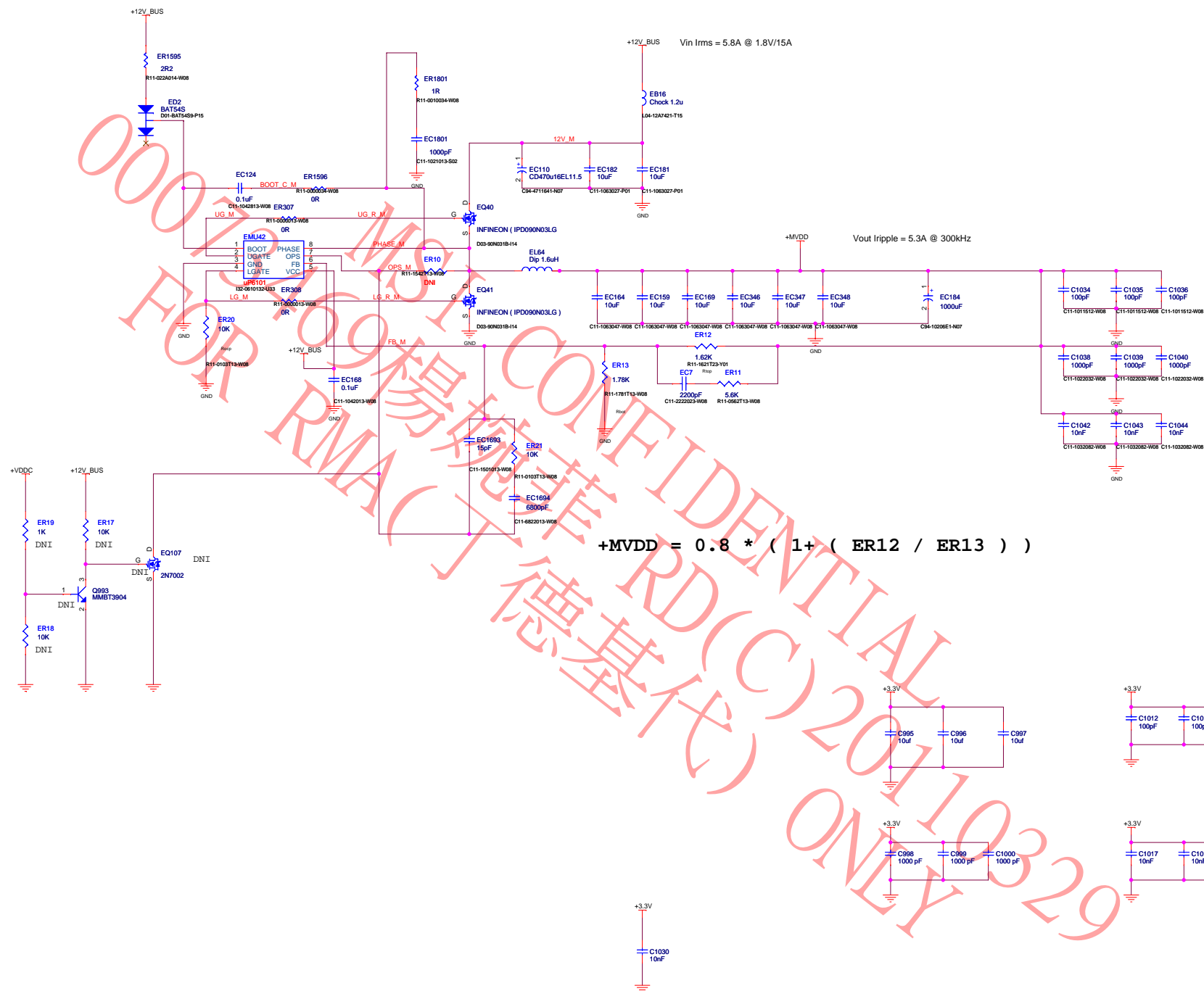
PIN BASED STRAPS



(11) VDDC

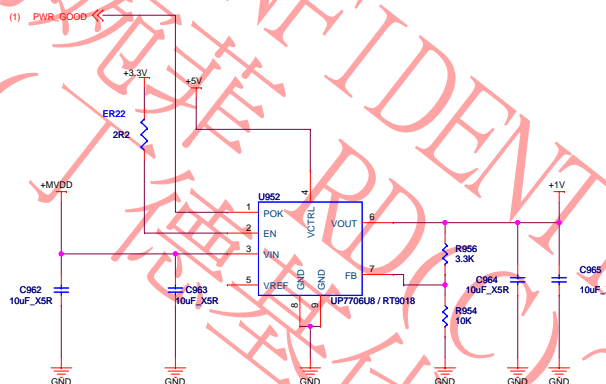
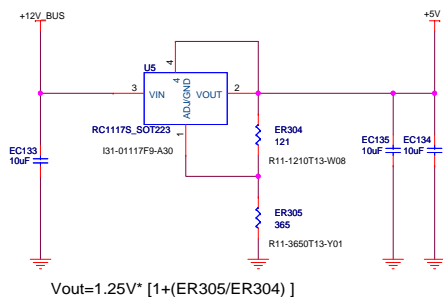
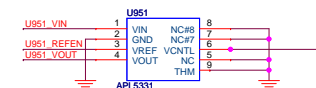
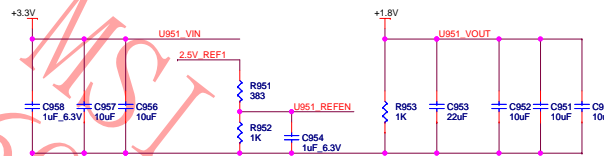
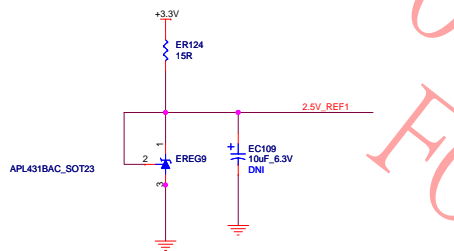


(12) MVDD



Memory Power Seq

(13) Linear Regulators



$$V_{out}=0.8V * (1+ R956 / R954)$$

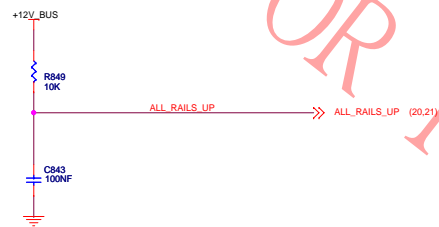
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(14) Power Management



Power Play

VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	RE1= RE2=	Output Voltage (V) RE1= RE2=	RE1= RE2=	
0	0				
0	1				
1	0				
1	1	1 0	1		Power-up Default

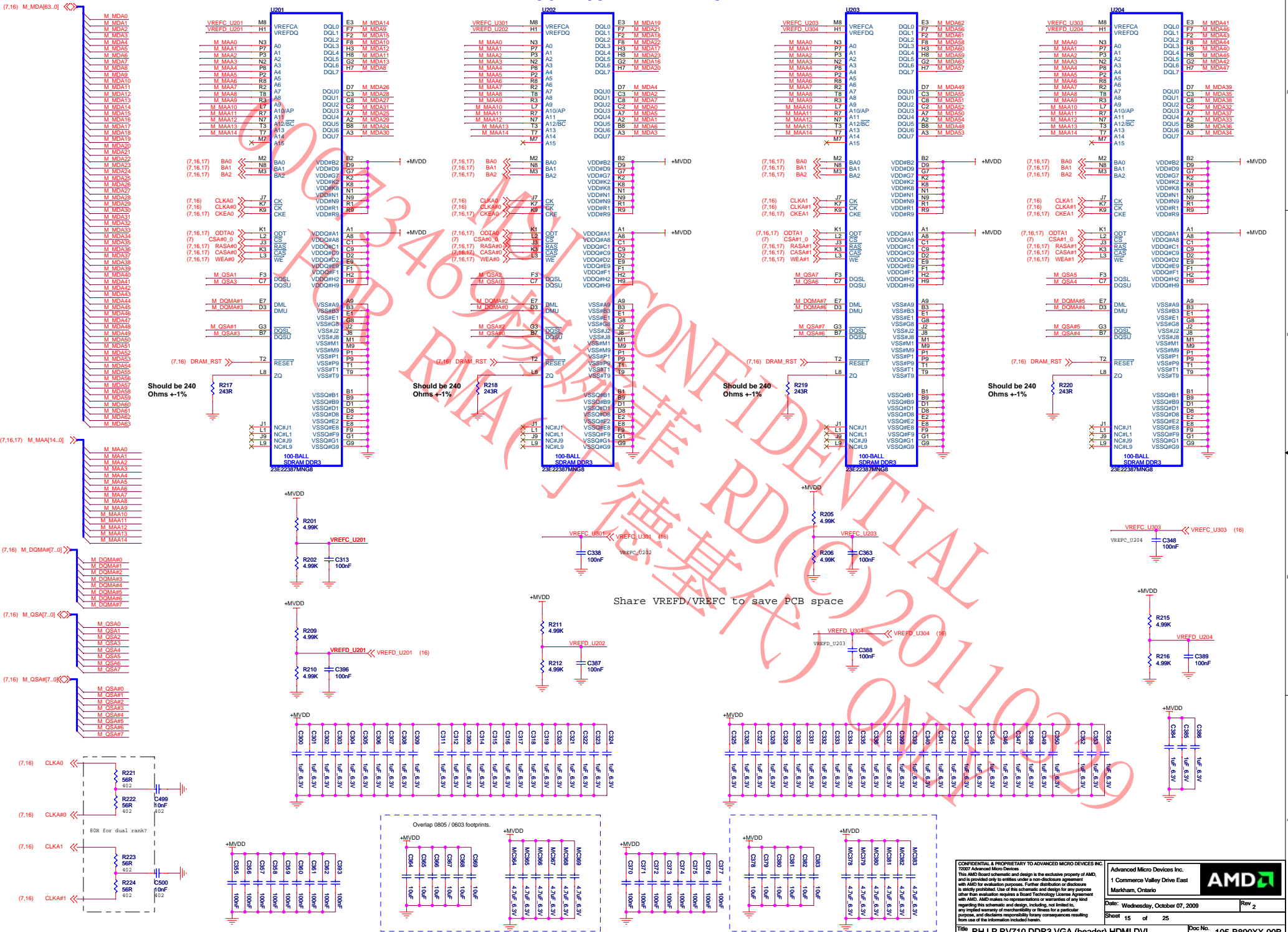
22.6K: 1.154V, PN: 31602262000
23.2K: 1.145V, PN: 31602322000
23.7K: 1.1376V, PN: 31602372000

MVDD Voltage Settings Using GPIOs

PWRCNTL_2 GPIO_6	RE1= RE2=	Output Voltage (V) RE1= RE2=	RE1= RE2=	
0				
1	1 0	1		Power-up Default

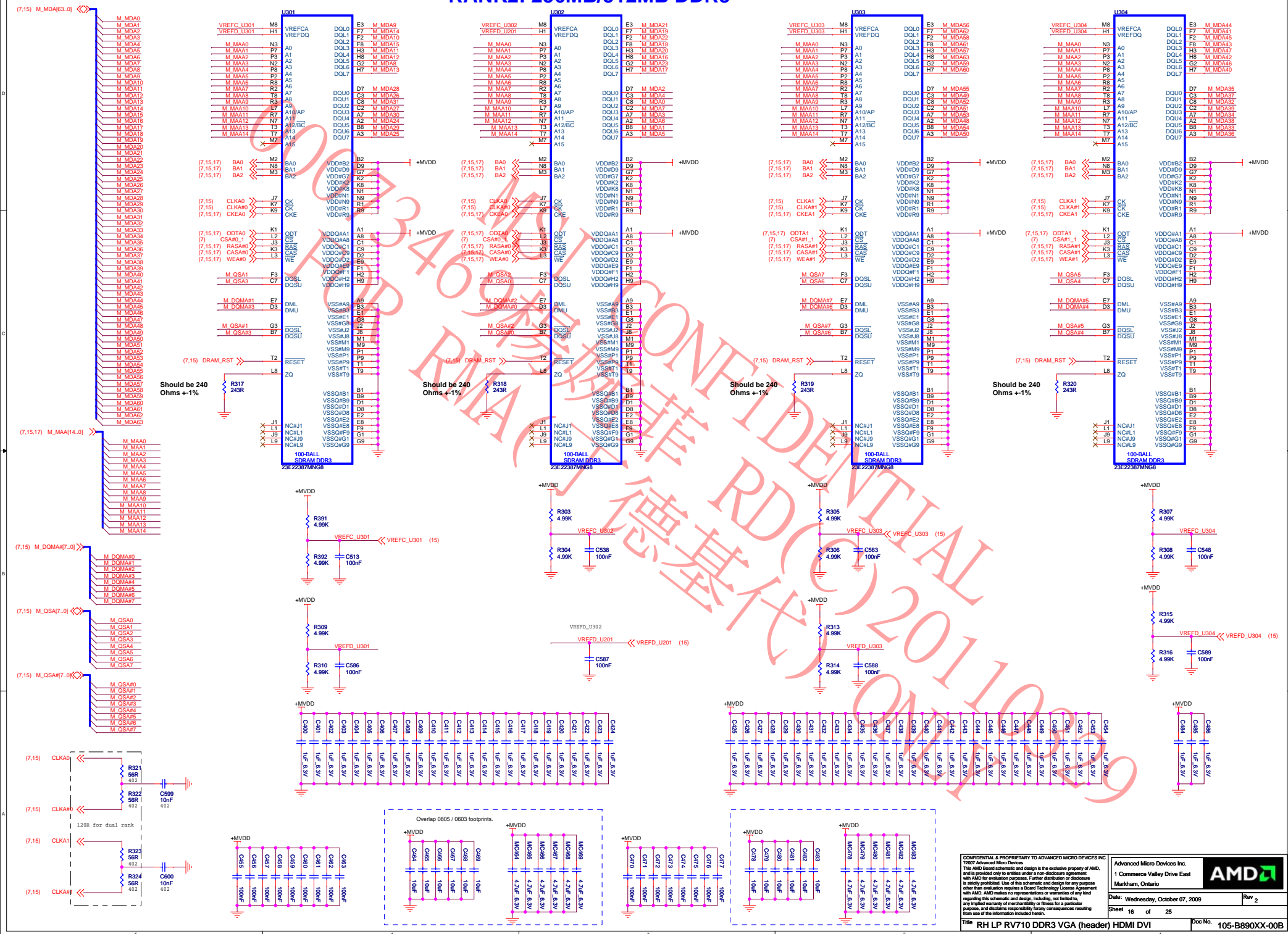
(15) DDR3 RANK1

RANK1: 256MB/512MB DDR3

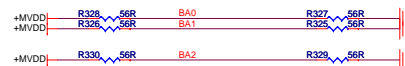
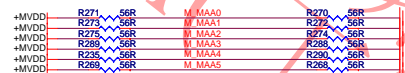
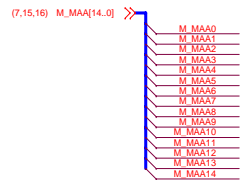


(16) DDR3 RANK2

RANK2: 256MB/512MB DDR3



(17) DDR3 Termination



(19) DAC2 OUTPUT

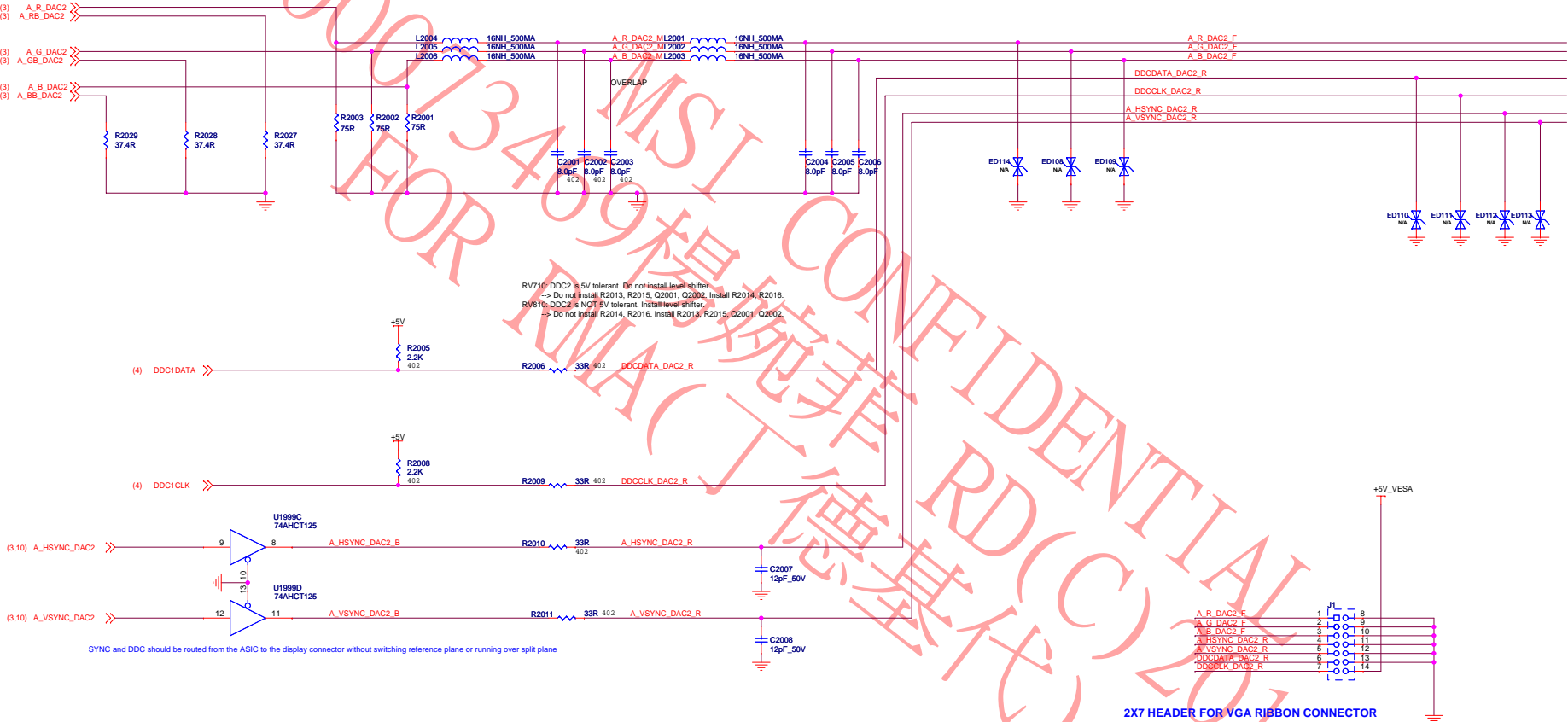
DAC 2 OUTPUT

Optional ESD Protection Diodes

Place near D2002, D2003, D2004, D2005

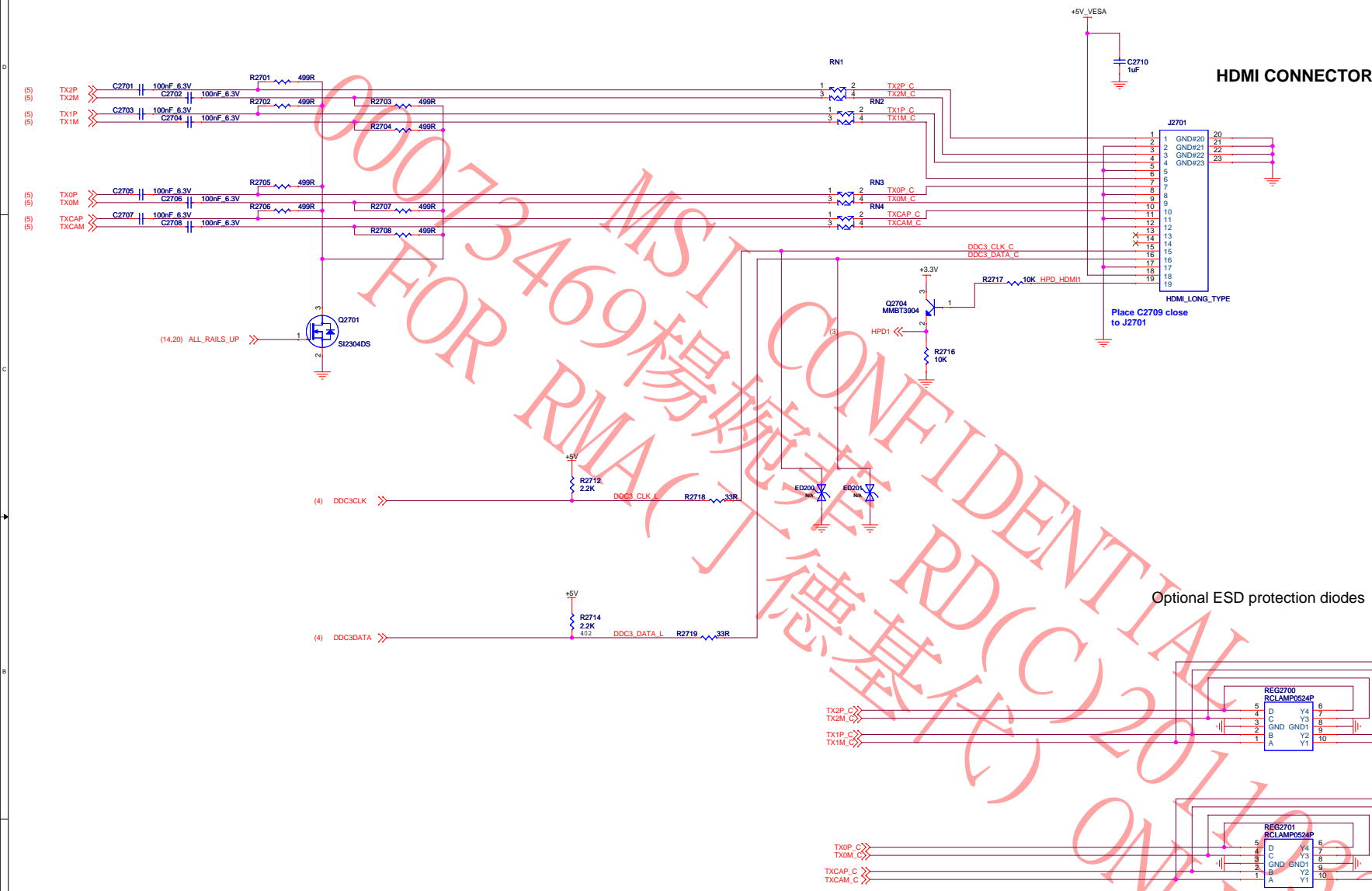


Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane



2X7 HEADER FOR VGA RIBBON CONNECTOR

TMDP-B OUTPUT



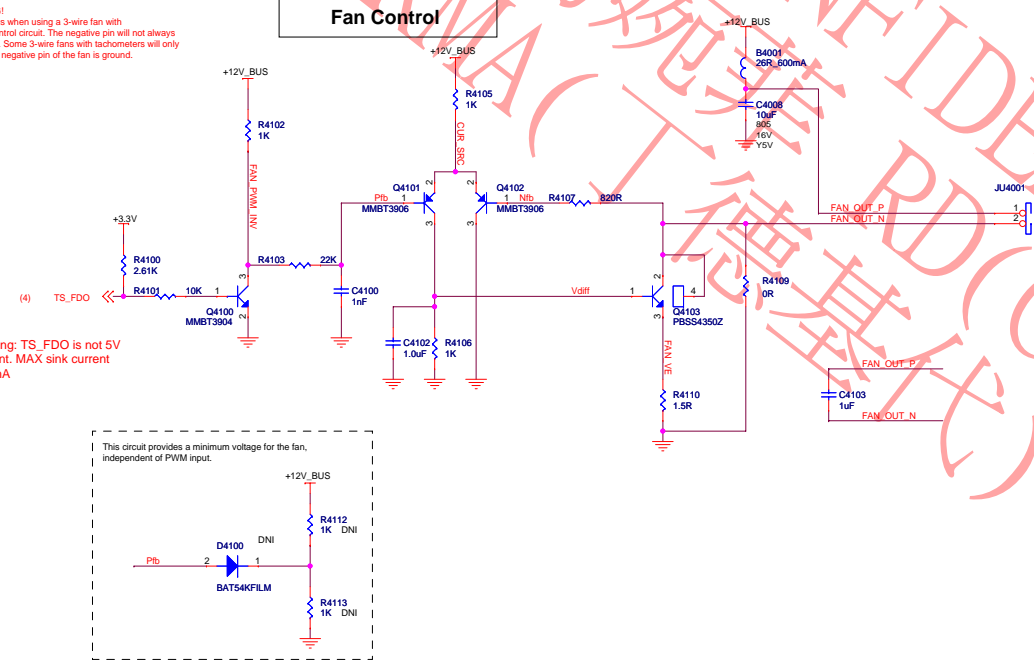
HDMI CONNECTOR

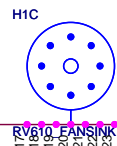
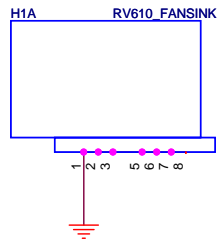
Optional ESD protection diodes

WARNING!
Be cautious when using a 3-wire fan with this fan control circuit. The negative pin will not always be ground. Some 3-wire fans with tachometers will only work if the negative pin of the fan is ground.

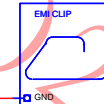
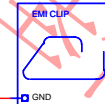
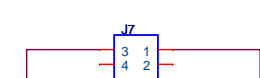
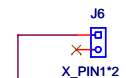
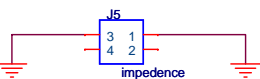
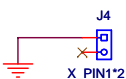
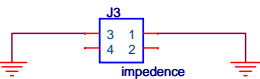
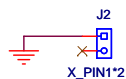
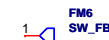
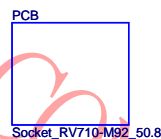
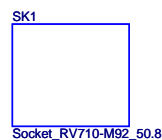
Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

Fan Control





7120036200G



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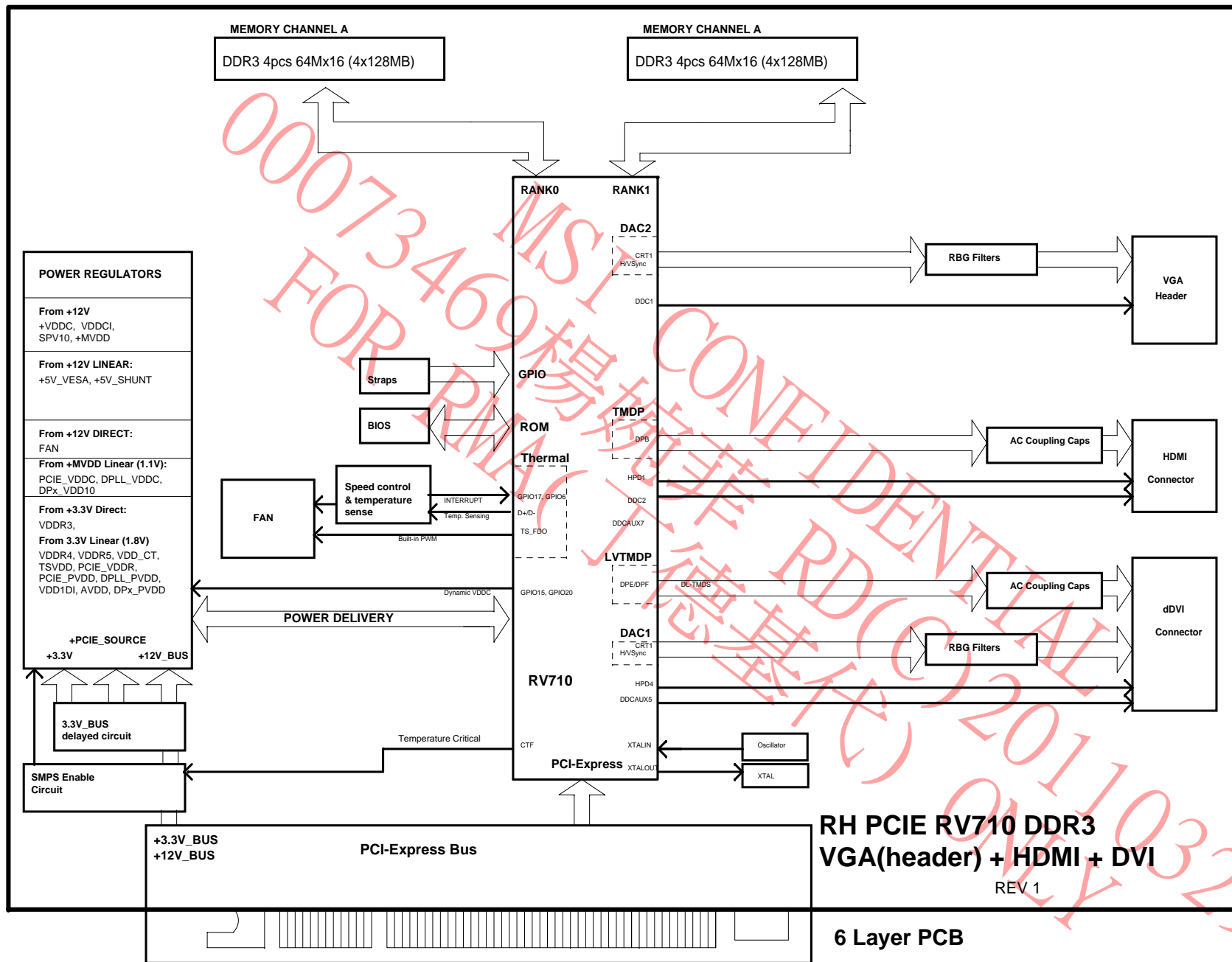
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Title RH LP RV710 DDR3 VGA (header) HDMI DVI Doc No. 105-B890XX-00B



**RH PCIE RV710 DDR3
VGA(header) + HDMI + DVI**
REV 1

6 Layer PCB

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Title RH LP RV710 DDR3 VGA (header) HDMI DVI Doc No. 105-B890XX-00B

<div>AMD</div>			Title		Schematic No.		Date:	
			RH LP RV710 DDR3 VGA (header) HDMI DVI		105-B890XX-00B		Wednesday, October 07, 2009	
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.					Rev 2
			RV710 ENGINEERING BOARD REVISION DESCRIPTION					
Sch Rev	PCB Rev	Date						
0	00A	2008.12.30	INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.					
1	00B	2009.01.22	Sch no change. just modify HDMI connnecro location on PCB					
			MSI CONFIDENTIAL FOR RMA (楊婉菲 RD(C) 20110329 ONLY) (丁德基代)					