MS8951 100

ATI RV360 R9600XT, TSOP 16MX16 *8 DDR, CRT, DVI-I , VIDEO IN, TV-OUT, AGP 8X

FREQUENCY	MHZ
CORE	500MHz
MEMORY	275MHz

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/25/03	PRELIMINARY BASED ON A035-10A - Redesign regulators - Add full-termination - Add variable speed controlled fan - Add RT1 and video in 9-in MiniDIN - Add oscillator - Replace all 100nF with 402 footprint
1	00B	09/02/03	- (LAYOUT) Move JU1/MJU1 away and move C321 and C322 up to avoid fan keep out violation - (04) Move VDDR4 ASIC pins to 3.3V_Bus - (05) Move +VDDC_S, +MVDDC_S after the bead - (05) Change Vin and Diode boost to +5V_BUS for VDDC
2	00B	10/31/03	ATi schematic review result: 1. Sheet4, R27 and R28 will provide the voltage as VDDC 2. Sheet7, make sure Q22 and Q24 can stand for the high current 3. Sheet8, keep the foot pin of the ALT. part in case there is problem. Add Samsung and Hynix memory setting suggestion 4.Sheet9, A2VDD, please make sure the MVDDQ setting is 2.5V before linking it. 5. Sheet10,11 Populate R751 to R758, R851 to R858 Change R759 to R766, R859 to R866 from 0R to 33R 6. Sheet15, DNI R605,R606,R607,Q25 and Q26. 7. Sheet18, DNI R927, R931, C900, Q41, Q42

<Variant Name>

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Size	Document Number	Rev
B	Cover_REV_HISTORY	00B

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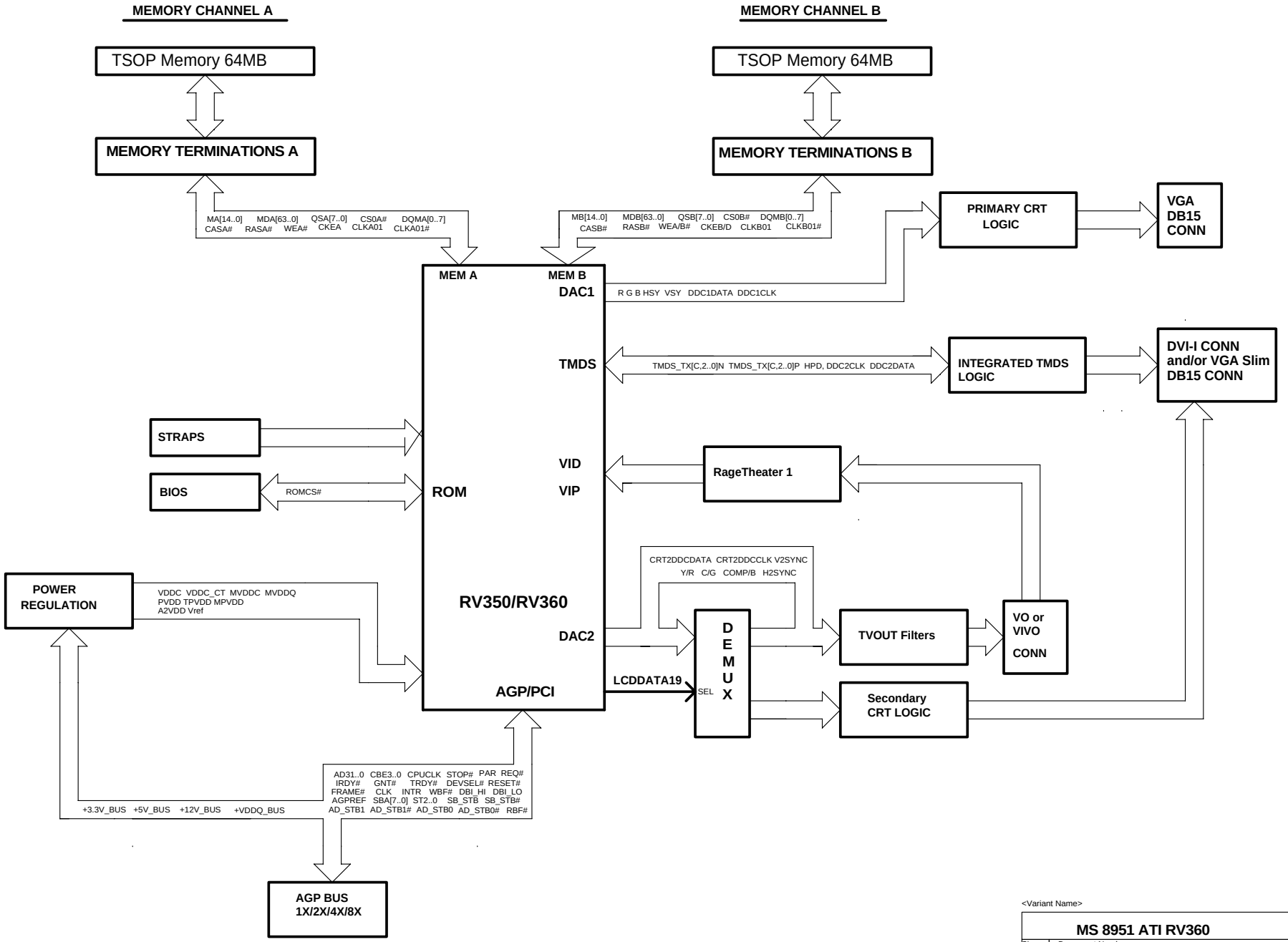

<Variant Name>

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Size	Document Number	Rev
B	**Block Diagram**	00B

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LAYOUT NOTE: SOME OF THE CAPS BELOW MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

+12V_BUS: C10 10uF_20V

+5V_BUS: C5 47uF_6.3V

+3.3V_BUS: C8 47uF_6.3V

+VDDQ_BUS: C2 100uF_6.3V >= 6.3V

Use 47uF Tant. 16V 20% D size (P/N 4230047600), 800mR Max. ESR and Max. ripple 430mA @ 100kHz
or
100uF, Alum. 6.3V 20% 6.3mm dia (P/N 4261010700), 440mR Max. ESR and Max. ripple 230mA @ 100kHz
or
47uF, Alum. 6.3V 20% 5mm dia (P/N 4262047600), 760mR Max. ESR and Max. ripple 150mA @ 100kHz

Place C2 on left side of AGP connector

4X/8X AGP BUS

GND_MPVSS GND_TPVSS GND_A2VSSN GND_AVSSQ GND_RSET
GND_AVSSN GND_PVSS GND_TXVSSR GND_A2VSSQ GND_R2SET

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

AGP_C/BE#[3..0] 4
AGP_AD[31..0] 4
AGP_SBA[7..0] 4
AGP_ST[2..0] 4

MAGP1

A1	12V	B1	OVRCNT#
A2	TYPEDET#	B2	5.0V
A3	GC_DET#/RESERVED	B3	5.0V#B3
A4	USB-	B4	USB+
A5	GND	B5	GND#B5
A6	INTA#	B6	INTB#
A7	RST#	B7	CLK
A8	GNT#	B8	REQ#
A9	VCC3.3	B9	VCC3.3#B9
A10	ST1	B10	ST0
A11	MB_DET#/RESERVED	B11	ST2
A12	DBI_HI/PIPE#	B12	RBF#
A13	GND#A13	B13	GND#B13
A14	WBF#	B14	DBI_LO/RESERVED
A15	SBA1	B15	SBA0
A16	VCC3.3#A16	B16	VCC3.3#B16
A17	SBA3	B17	SBA2
A18	SB_STB#	B18	SB_STB
A19	GND#A19	B19	GND#B19
A20	SBA5	B20	SBA4
A21	SBA7	B21	SBA6
A22	RESERVED	B22	RESERVED#B22
A23	GND#A23	B23	GND#B23
A24	RESERVED#A24	B24	3.3VAUX
A25	VCC3.3#A25	B25	VCC3.3#B25
A26	AD30	B26	AD31
A27	AD28	B27	AD29
A28	VCC3.3#A28	B28	VCC3.3#B28
A29	AD26	B29	AD27
A30	AD24	B30	AD25
A31	GND#A31	B31	GND#B31
A32	AD_STB1#	B32	AD_STB1
A33	C/BE3#	B33	AD23
A34	VDDQ1.5	B34	VDDQ1.5#B34
A35	AD22	B35	AD21
A36	AD20	B36	AD19
A37	GND#A37	B37	GND#B37
A38	AD18	B38	AD17
A39	AD16	B39	C/BE2#
A40	VDDQ1.5#A40	B40	VDDQ1.5#B40
A41	FRAME#	B41	IRDY#
A42	KEY	B42	KEY#B42
A43	KEY#A43	B43	KEY#B43
A44	KEY#A44	B44	KEY#B44
A45	KEY#A45	B45	KEY#B45
A46	TRDY#	B46	DEVSEL#
A47	STOP#	B47	VDDQ1.5#B47
A48	PME#	B48	PERR#
A49	GND#A49	B49	GND#B49
A50	PAR	B50	SERR#
A51	AD15	B51	C/BE1#
A52	VDDQ1.5#A52	B52	VDDQ1.5#B52
A53	AD13	B53	AD14
A54	AD11	B54	AD12
A55	GND#A55	B55	GND#B55
A56	AD9	B56	AD10
A57	C/BE0#	B57	AD8
A58	VDDQ1.5#A58	B58	VDDQ1.5#B58
A59	AD_STB0#	B59	AD_STB0
A60	AD6	B60	AD7
A61	GND#A61	B61	GND#B61
A62	AD4	B62	AD5
A63	AD2	B63	AD3
A64	VDDQ1.5#A64	B64	VDDQ1.5#B64
A65	AD0	B65	AD1
A66	VREFGC	B66	VREFCG

X_1.5V_AGP_BUS

AGP_TYPEDET# / AGP_GC_8X_DET#
4 AGP_INTR#
4,16 AGP_RESET#
4 AGP_GNT#
AGP_ST1
4 AGP_MB_8X_DET# — R4 0R 402 — AGP_MB_8X_DET#_R
4 AGP_DBI_HI — R7 0R 402 — AGP_DBI_HI_R
4 AGP_WBF#
AGP_SBA1
AGP_SBA3
4 AGP_SBSTB# — R1 0R 402
AGP_SBA5
AGP_SBA7
AGP_AD30
AGP_AD28
AGP_AD26
AGP_AD24
4 AGP_ADSTB1# — R5 0R 402
AGP_C/BE#3
AGP_AD22
AGP_AD20
AGP_AD18
AGP_AD16
4 AGP_FRAME#
4 AGP_TRDY#
4 AGP_STOP#
4 AGP_PAR
AGP_PAR_R
AGP_AD15
AGP_AD13
AGP_AD11
AGP_AD9
AGP_C/BE#0
4 AGP_ADSTB0# — R12 0R 402
AGP_AD6
AGP_AD4
AGP_AD2
AGP_AD0
AGP_VREFGC

AGP_ST0
AGP_ST2
AGP_SBA0
AGP_SBA2
AGP_SBA4
AGP_SBA6
AGP_AD31
AGP_AD29
AGP_AD27
AGP_AD25
AGP_AD23
AGP_AD21
AGP_AD19
AGP_AD17
AGP_C/BE#2
AGP_C/BE#1
AGP_AD14
AGP_AD12
AGP_AD10
AGP_AD8
AGP_AD7
AGP_AD5
AGP_AD3
AGP_AD1
AGP_AGPREF

AGP_DBI_LO_R — R8 0R 402 — AGP_RBF# 4, AGP_DBI_LO 4
AGP_SBSTB_R — R2 0R 402 — AGP_SBSTB 4
AGP_ADSTB1_R — R6 0R 402 — AGP_ADSTB1 4
AGP_ADSTB0_R — R13 0R 402 — AGP_ADSTB0 4

AGP_AGPCLK 4
AGP_REQ# 4
AGP_IRDY# 4
AGP_DEVSEL# 4

+12V_BUS +5V_BUS +3.3V_BUS
C21 100nF 402
C22 100nF 402
C23 100nF 402
Caps for EMI - install close to AGP connector

AGP_TYPEDET# — R19 5.1R
+12V, TYPEDET# short protection for OEM (5.1R)

AGP_GC_8X_DET# — R60 0R 402

UNIVERSAL VREFGC CIRCUIT (4X, 8X)

4 AGP_MB_8X_DET# — AGP_MB_8X_DET# — R17 47K 402 — Q12 BSN20 — R3 20K 402 — TEST
Q1 2N7002E — R20 324R — AGP_VREFGC
R21 147R
R24 100R 402
C6 10nF 402
Close to ASIC
May be placed far from connector -- place C3 FAR from connector, on left side!!
C3 100nF 402
U2 X_TC7SZ08FU
R23 X_1K 402

UNIVERSAL VREFCG CIRCUIT (4X, 8X)

AGP_AGPREF
TEST
Q5 2N7002E
R66 324R
R64 X_0R 402 DNI
R67 147R
AGP_AGPREFCG — AGP_AGPREFCG 4
R65 100R 402
C7 10nF 402
Close to ASIC

<Variant Name>

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Size	Document Number	Rev
Custom	AGP 4X/8X Bus	00B
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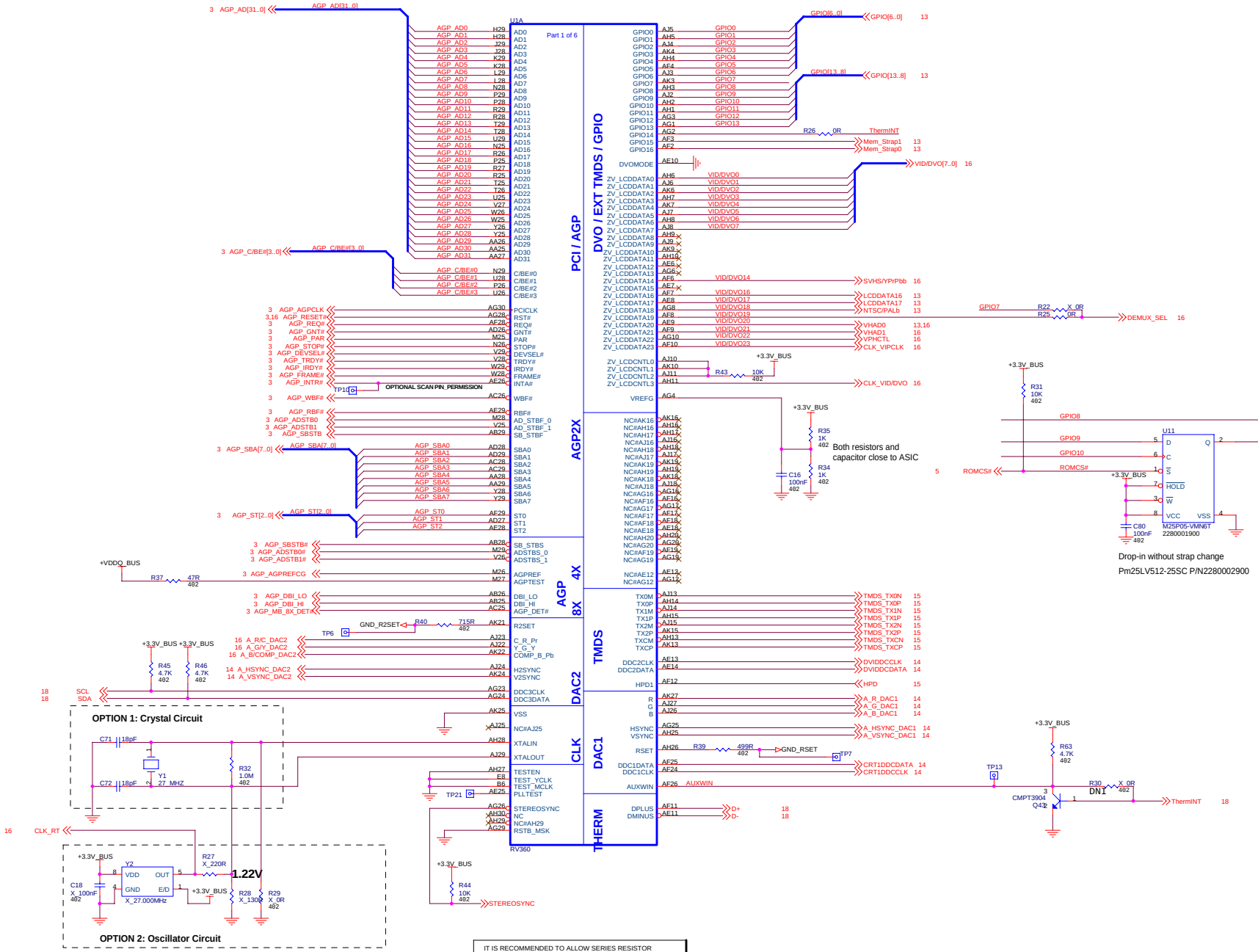
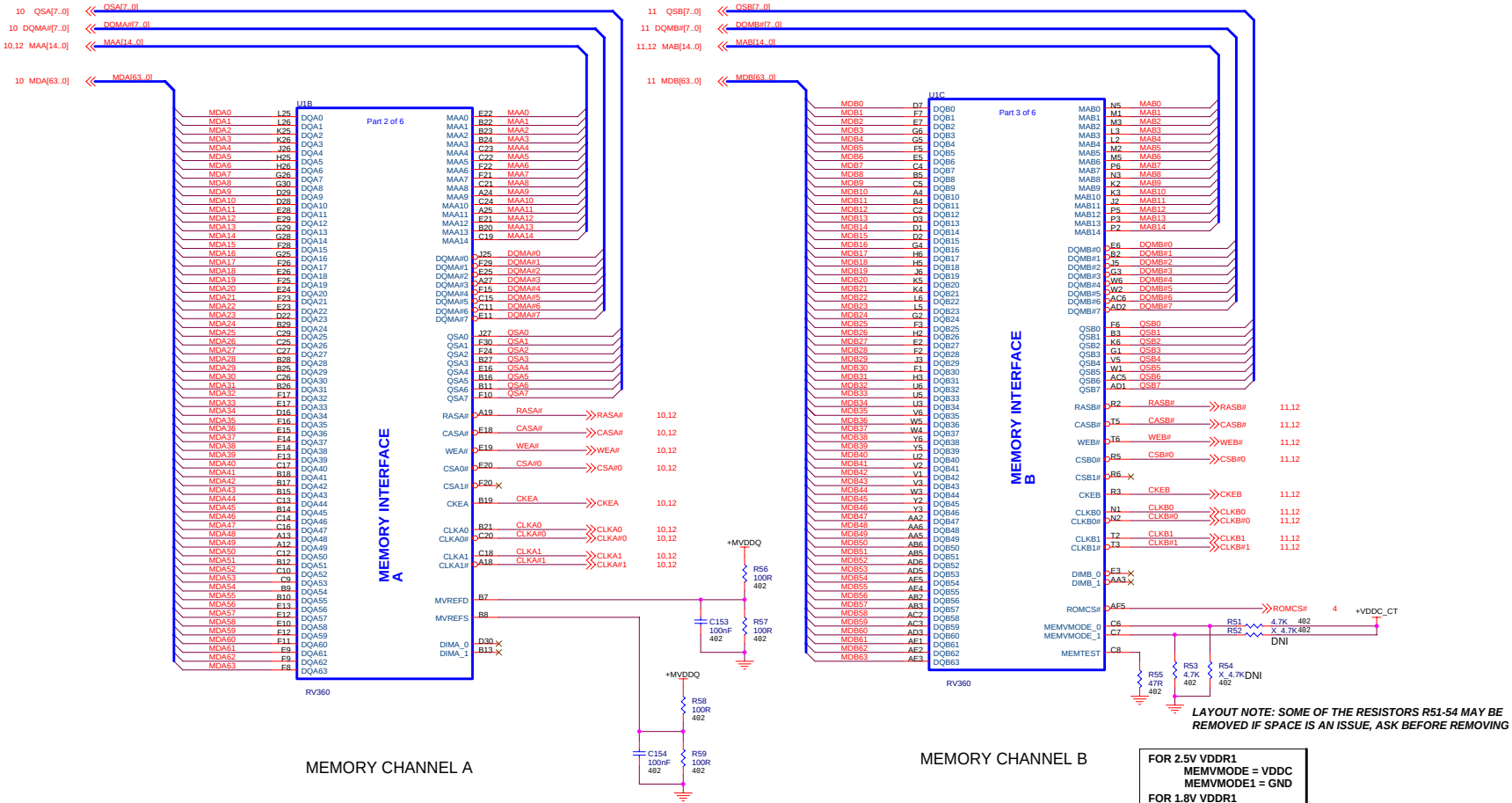

U1A
Part 1 of 6
PCI / AGP
DVO / EXT TMDS / GPIO
AGP2X
AGP 4X
8X
TMDS
DAC2
CLK
DAC1
THERM
RV360
OPTIONAL SCAN PIN_PERMISSION
Both resistors and capacitor close to ASIC
Drop-in without strap change
Pm25LV512-25SC P/N2280002900
OPTION 1: Crystal Circuit
OPTION 2: Oscillator Circuit
1.22V
IT IS RECOMMENDED TO ALLOW SERIES RESISTOR FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS TO ADDRESS ANY LAYOUT NOISE RELATED SIGNAL DAMPING REQUIREMENTS
1. Make sure R27 and R28 provide the voltage as VDDC
MS 8951 ATI RV360
RV360 core
Custom
Friday, June 04, 2004
Sheet 4 of 18



MEMORY CHANNEL A

MEMORY CHANNEL B

PLACE C351/152 VERY CLOSE TO ASIC

R56/57/58/59 CLOSE TO ASIC AS WELL

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

FOR 2.5V VDDR1
MEMVMODE = VDDC
MEMVMODE1 = GND
FOR 1.8V VDDR1
MEMVMODE = GND
MEMVMODE1 = VDDC
SEE DESIGN GUIDE

<Variant Name>

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Size	Document Number	Rev
Custom	**RV360 memory interface**	00B
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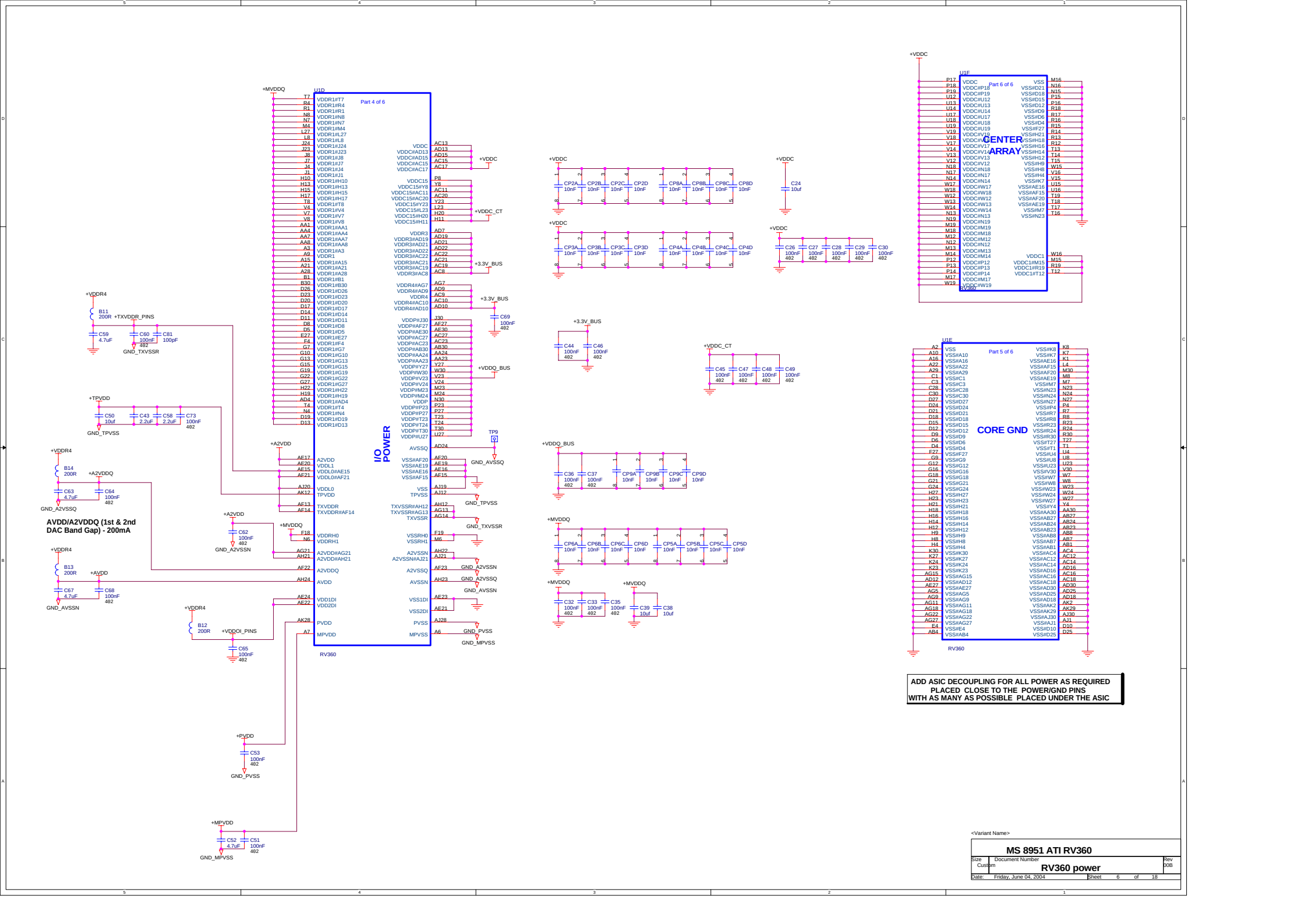
U1D
Part 4 of 6
I/O POWER
RV360
U1F
Part 6 of 6
CENTER ARRAY
U1E
Part 5 of 6
CORE GND
RV360
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
<Variant Name>
MS 8951 ATI RV360
Size Custom
Document Number
RV360 power
Rev 00B
Date: Friday, June 04, 2004
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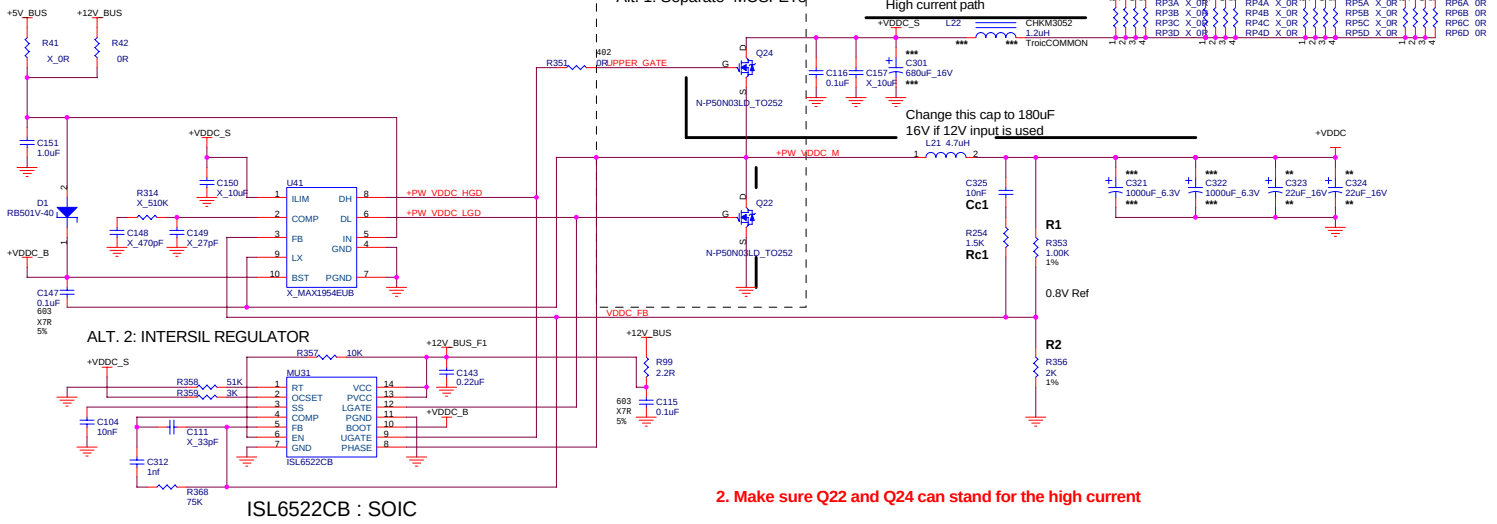
Regulator for VDDC (ASIC Core)

Vout = 1.2V
Iout = 7A MAX at 400MHz

ALT. 1: MAXIM REGULATOR



ALT. 2: INTERSIL REGULATOR

ISL6522CB : SOIC

2. Make sure Q22 and Q24 can stand for the high current

*** Indicate number of power via required for the connection

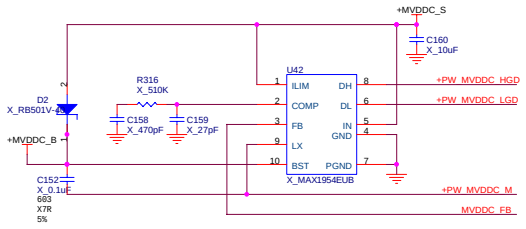
Part	NOTES
MAX1954	Do not install Cc1, Rc1
ISL6522	Install Cc1, Rc1

Part	Vout	R1	R2
MAX1954 ISL6522 0.8V Ref	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240110100
	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N
	1.62V	1.00K 1% ATI P/N 3240100100	976R 1% ATI P/N 3240976000
	2.5V	1.00K 1% ATI P/N 3240100100	475R 1% ATI P/N 3240475300
	3.3V TSOP Memory	1.00K 1% ATI P/N 3240100100	324R 1% ATI P/N 3240332000
	3.45V TSOP Memory	1.00K 1% ATI P/N 3240100100	301 1% ATI P/N 3240301000

Regulator for MVDDC (MEM Core)

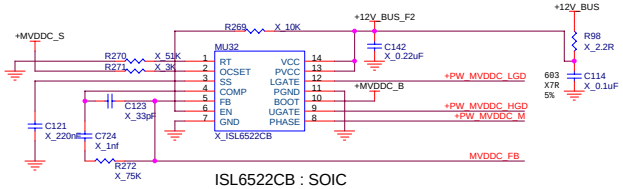
Vout = 2.5V ~ 2.6V
Iout = 2.96A (370mA x 8) MAX,
Burst Mode (300MHz rated)

ALT. 1: MAXIM REGULATOR

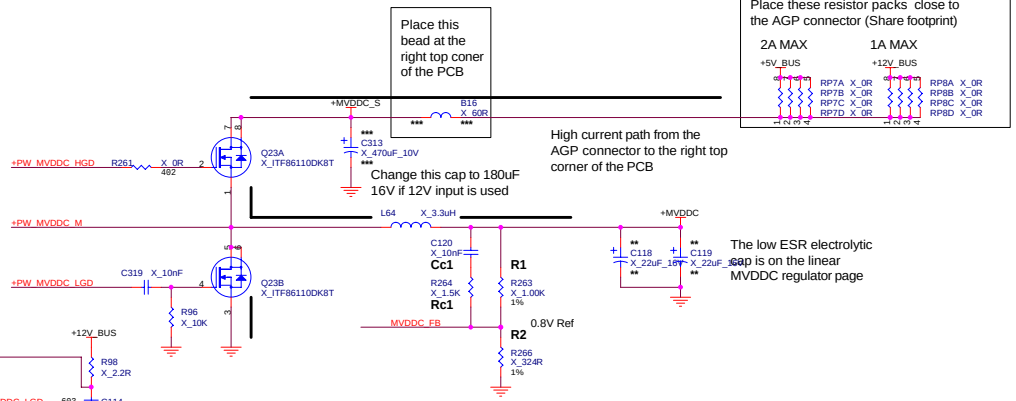


DO NOT USE MAXIM REGULATOR IF 12V INPUT IS USED!!!

ALT. 2: INTERSIL REGULATOR



ISL6522CB : SOIC



<Variant Name>

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Size: Custom | Document Number: REG Switcher (VDDC,MVDDC) | Rev: 1.0

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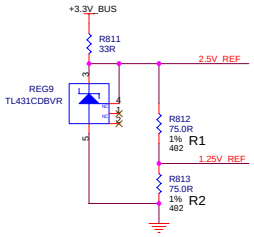
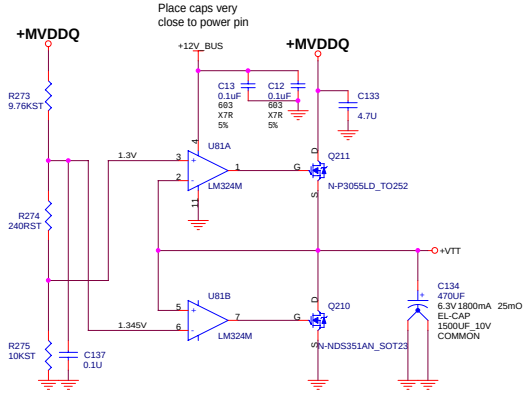


Voltage Req.	R1	R2
0.8V	150R P/N 3240150000	71.5R P/N 324075R500
1.25V	75R P/N 3240075000	75R P/N 3240075000
1.5V	49.9R P/N 3240049900	75R P/N 3240075000
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

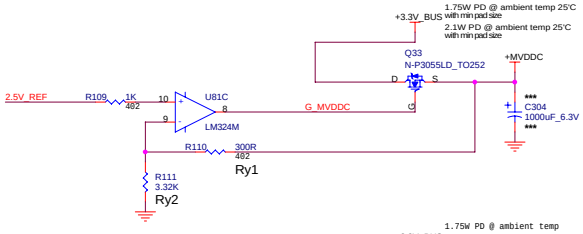
Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000	1.5K P/N 3240015200

Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.65V	200R P/N 3240200000	3.32K P/N 3240332100
2.5V	0R P/N 3230000000	DNI

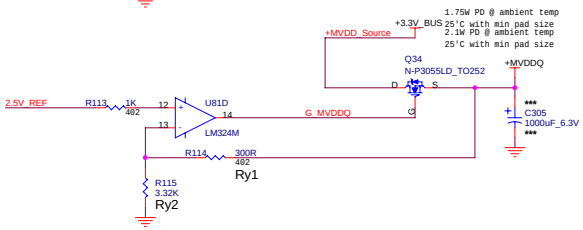
Regulator for +VTT (Termination)
Vout = 1.25V ~ 1.3V with +2.5V +MVDDQ
Iout = 1000mA MAX



Keep the foot pin of the ALT. part in case there is problem



2.5V
+MVDDC: 3A MAX (3W)
+MVDDC and +MVDDQ: 5.5A MAX (5.5W)
Use 2 squ. in Drain Pad Size



2.5V
1A MAX (2.5W)
Use 2 squ. in Drain Pad Size

+MVDDQ MOSFET can be removed and derive +MVDDQ form +MVDDC
Maximum current measurement must be obtained and MOSFET dissipation must be checked

3.

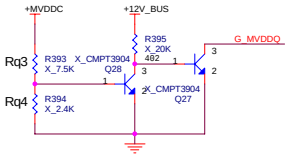
For Samsung K4D551638D-TC2A
+MVDDQ/+MVDDC = 2.8V
R111, R115 = 2.67K
R110, R114 = 324R

For Hynix 5DU561622CT-33
+MVDDQ/+MVDDC = 2.6V
R111, R115 = 3.74K
R110, R114 = 150R

Circuit to hold +MVDDQ low and wait for +MVDDC for proper memory power sequence

+MVDDC	Rq3	Rq4
3.45V	7.5K 3230075200	2.4K 3230024200
2.5V		

Assume Bmin of the transistors = 100 for the above values, if Bmin = 50 instead, then Rq3 and Rq4 should be decrease to half of the above values



<Variant Name>

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Size	Document Number	Rev
Custom	REG (Memory, VDDC_CT)	00B
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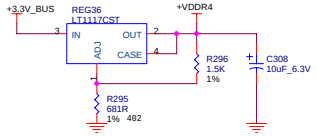
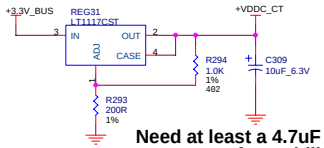
Alt. regulator for +VDDR4
Vout = 1.8V
Iout = 300mA MAX

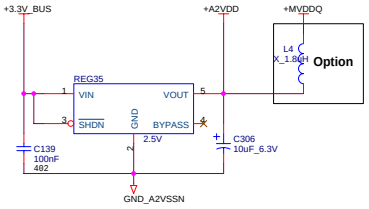


Alt regulator for +VDDC_CT
Vout = 1.5V
Iout = 500mA MAX



Need at least a 4.7uF output cap for stability

Alt. regulator for +A2VDD
Vout = 2.5V
Iout = 120mA MAX

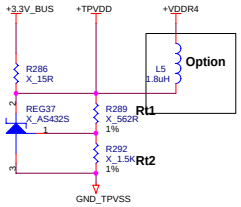


+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.

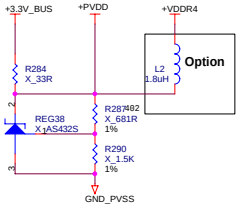
4. If +MVDDQ = 2.5V, then +A2VDD can link to this voltage

Alt. regulator for +TPVDD
Vout = 1.6V ~ 1.8V
Iout = 100mA MAX

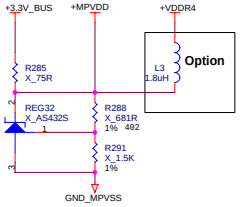
	Rt1		Rt2	
1.61V +0.01V/-0.01V	432R	3240432000	1.5K	3230015200
1.69V +0.01V/-0.01V	432R	3240432000	1.21K	3240121100
1.716V +0.01V/-0.01V	562R	3240562000	1.5K	3230015200
1.8175V +0.01V/-0.01V	681R	3240681000	1.5K	3230015200



Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



Alt regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX

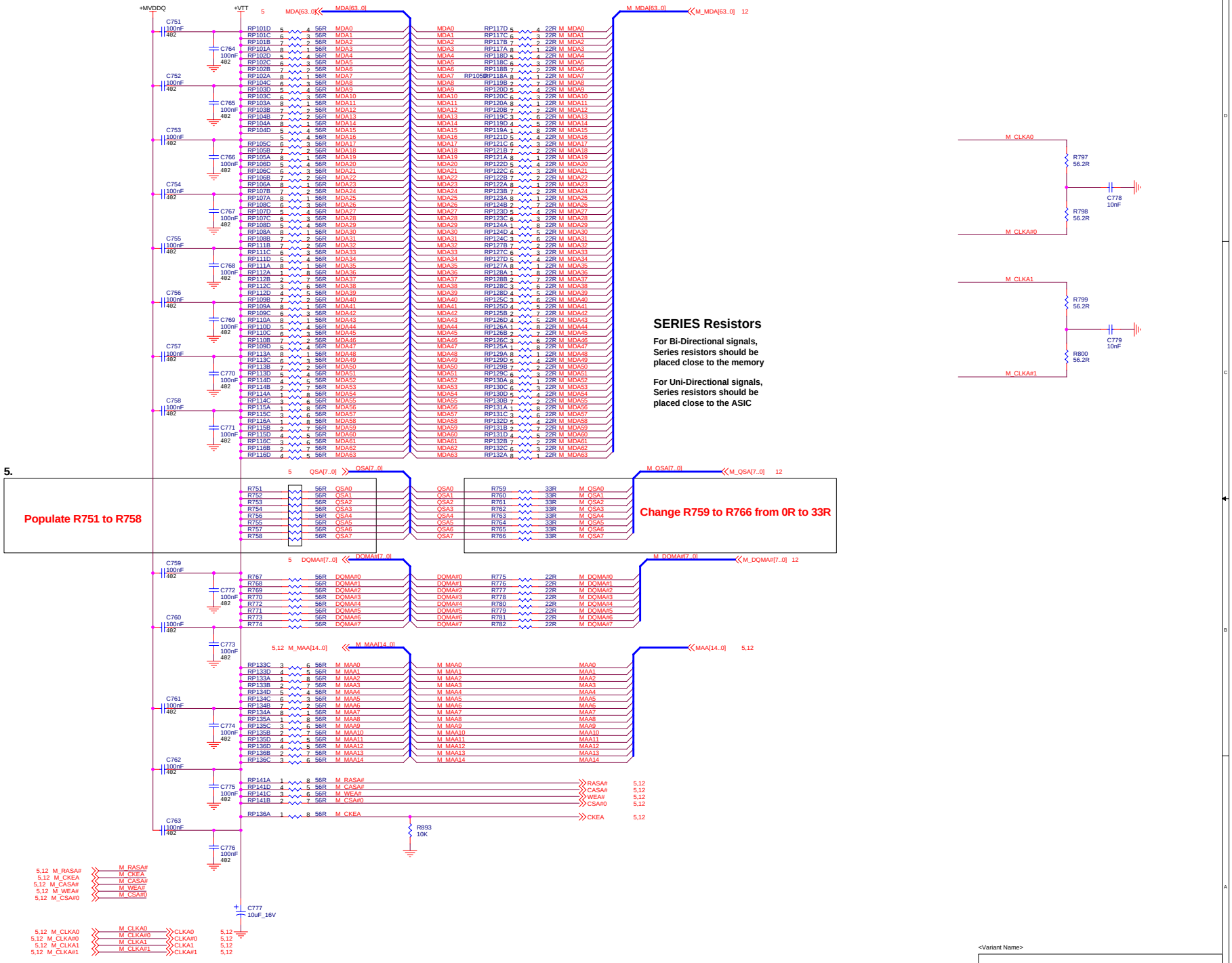


<Variant Name>

MS 8951 ATI RV360

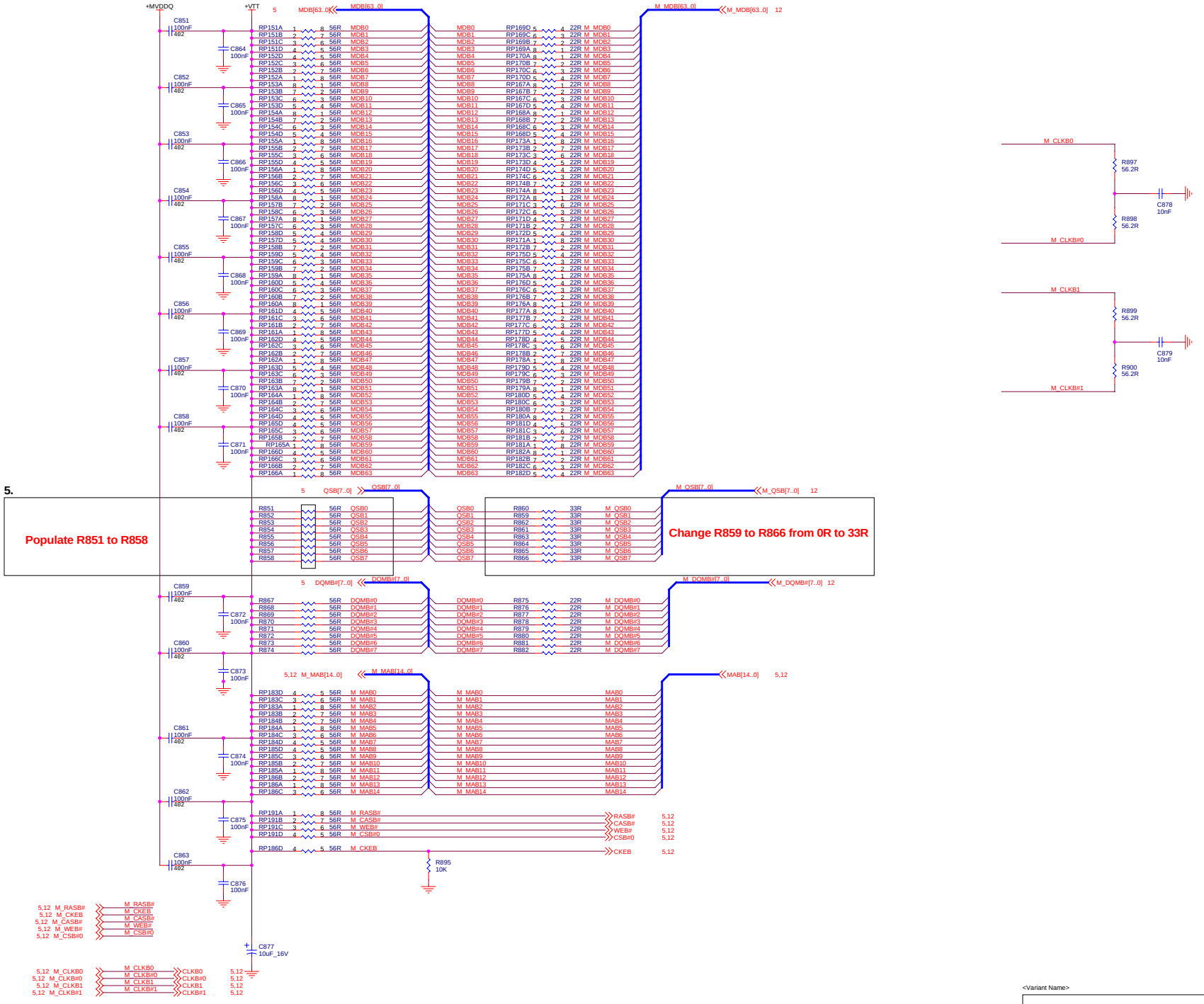
Size	Document Number	Rev
Custom	REG(others PLLs)	00B

Date: Friday, June 04, 2004 Sheet 9 of 19



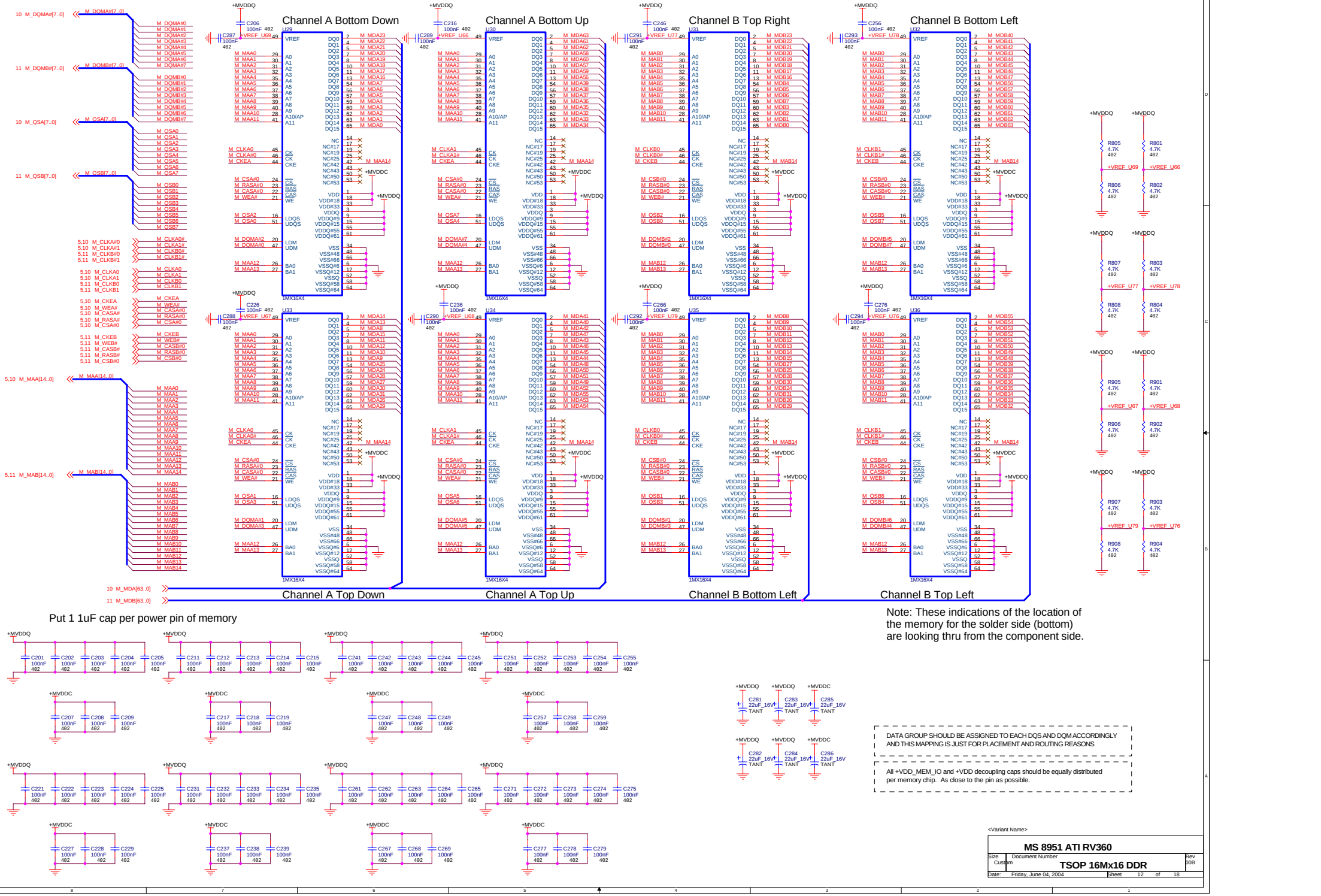
<Variant Name>

	MS 8951 ATI RV360	
Size C	Document Number VTT Termination CHA	Rev 00B
Date: Friday, June 04, 2004	Sheet 10 of 18	



<Variant Name>

MS 8951 ATI RV360		
Size C	Document Number VTT Termination CHB	Rev 00B
Date: Friday, June 04, 2004	Sheet 11 of 18	


Channel A Bottom Down
Channel A Bottom Up
Channel B Top Right
Channel B Bottom Left
Channel A Top Down
Channel A Top Up
Channel B Bottom Left
Channel B Top Left
Put 1 1uF cap per power pin of memory
Note: These indications of the location of the memory for the solder side (bottom) are looking thru from the component side.
DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS
All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.
<Variant Name>
MS 8951 ATI RV360
Size Custom
Document Number
TSOP 16Mx16 DDR
Rev 00B
Date: Friday, June 04, 2004
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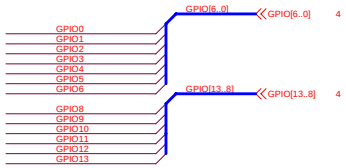
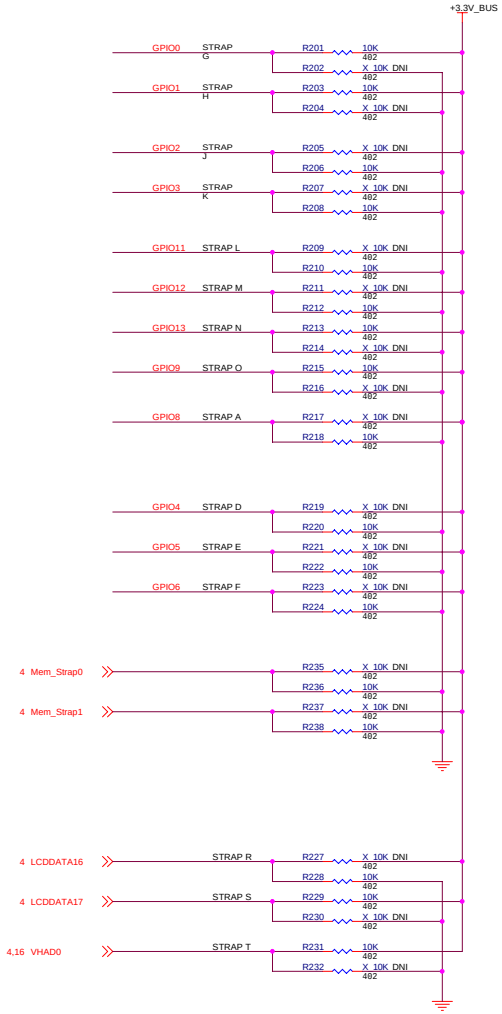
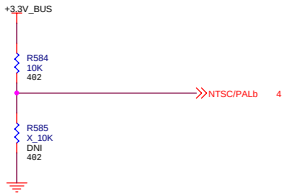
OPTION STRAPS





STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM **1011 - Serial M25P10 ROM (ST), chip IDis from ROM** 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1001
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000 (internal pull-down)
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select **00 - single function device.** 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	00
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED



DEMUX_SEL	LCDDATA19	On board pull-up and software controlled to select DAC2 driving CRT or TV for detection purpose 0 - DAC2 for TV 1 - DAC2 for CRT
NTSC/PALb	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)
SVHS/YPrPbb	LCDDATA14	Connected to Component TV-Out Detect pin Normally high, pulled low by Component TVO dongle 0 - Component/YPrPb (Resistor pull-down in dangle) 1 - SHVS/Composite (on board resistor pull-up)

<Variant Name>

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Size	Document Number	Rev
Custom	**Straps**	00B
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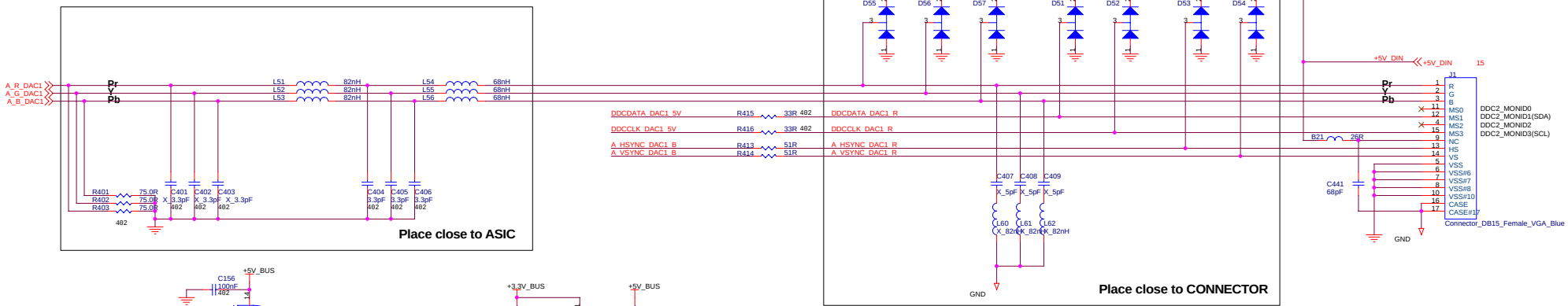
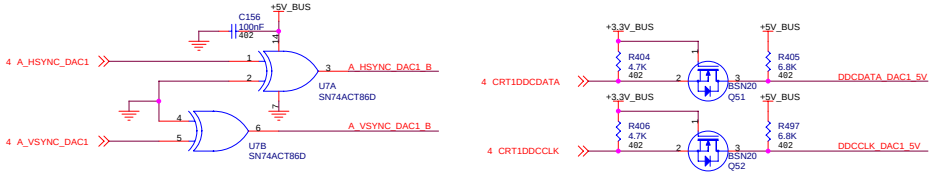
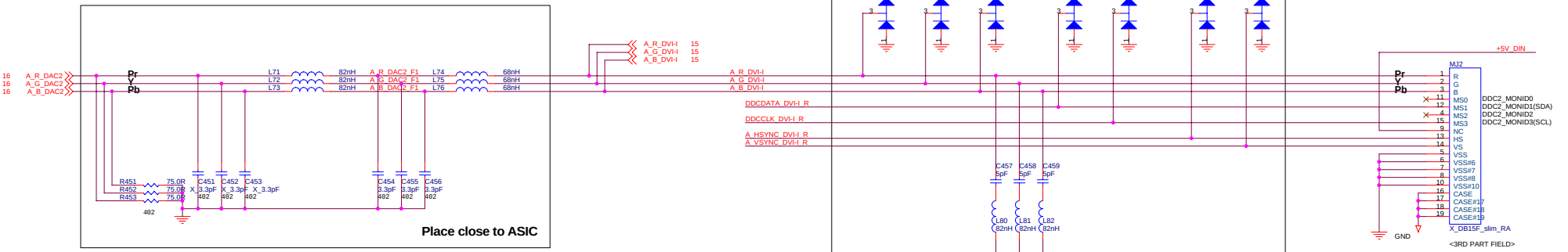
OPTIONAL ESD/HOTPLUG PROTECTION DIODES

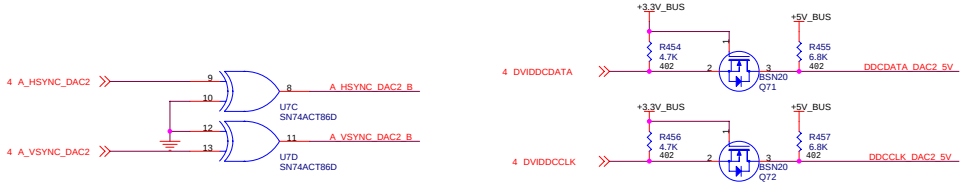
PRIMARY CRT



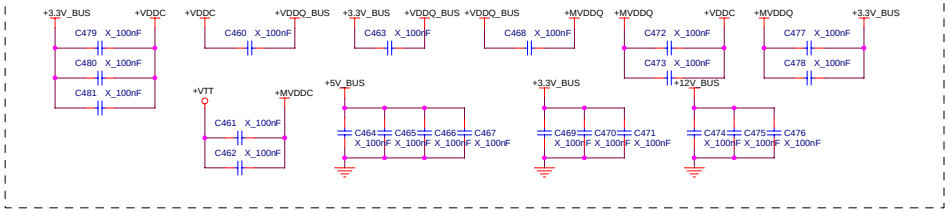


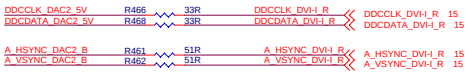
SECONDARY CRT





For EMI Cap





<Variant Name>

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Size: Custom	Document Number: DAC RGB Filters	Rev: 00B
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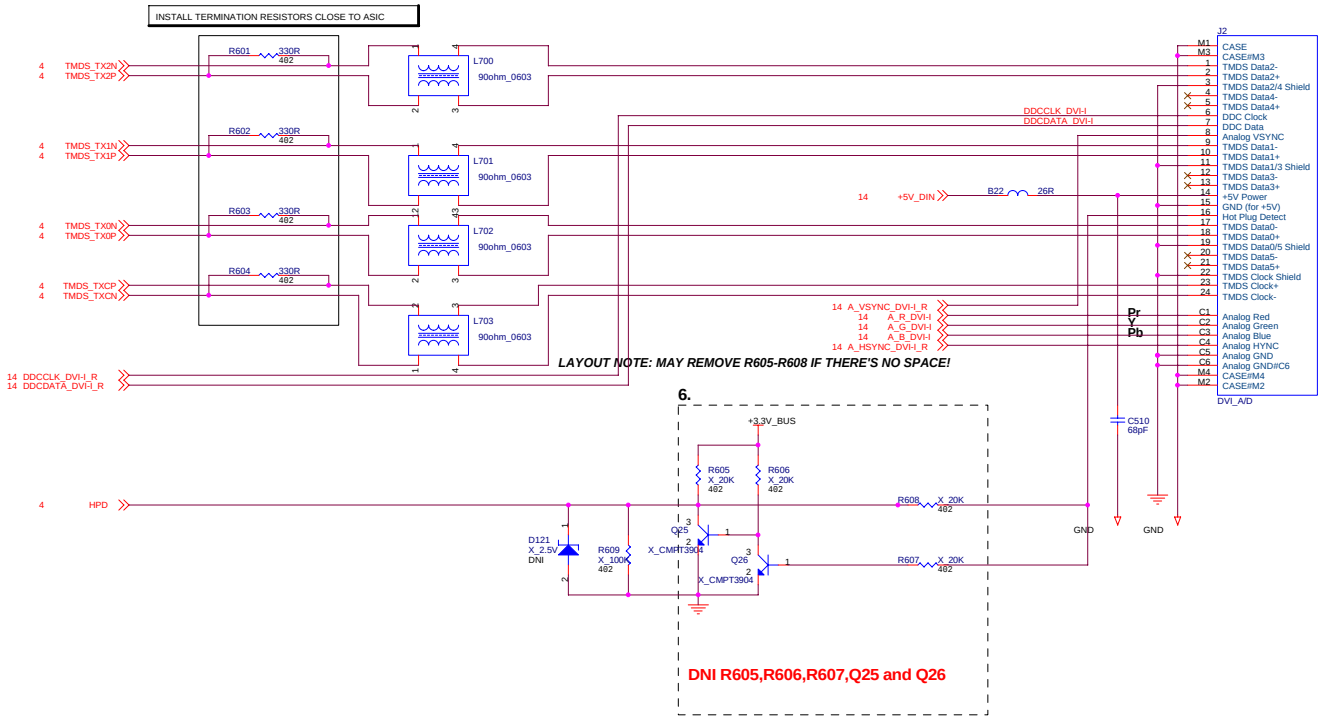
PRIMARY DVI-I CONNECTOR



<Variant Name>

MS 8951 ATI RV360		
Size: Custom	Document Number: TMDS & DVI-I	Rev: 00B
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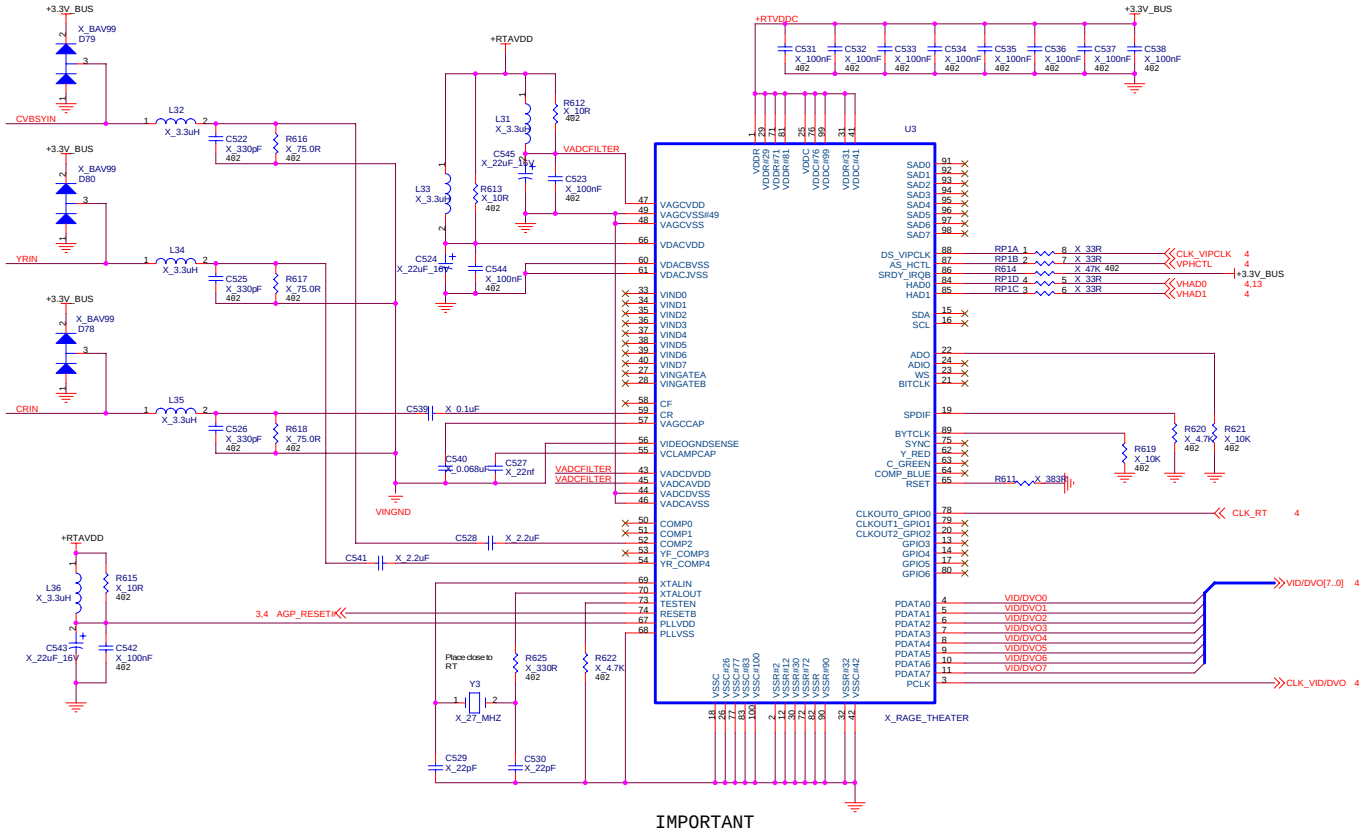


Layout Guide line of THEATER

#1 : C27 and C28 have to be placed as close as possible to the respective pins of Rage THEATER

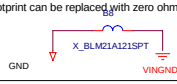
#2 : VINGND should be seperated from Digital or Chassis Ground and have no loops

#3 : VINGND should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

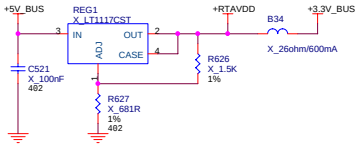
IMPORTANT

Put 2D line as close as possible to pin 56 of Rage Theater

Footprint can be replaced with zero ohm or other.

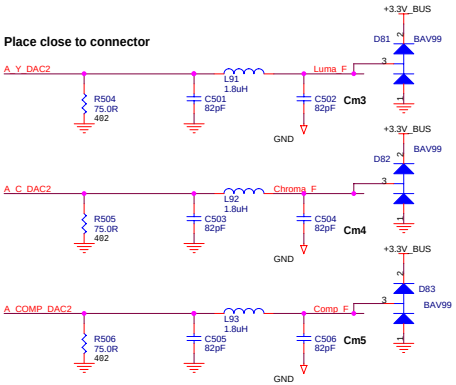


Regulator for RVDD

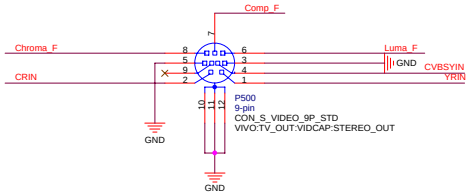


TV OUT

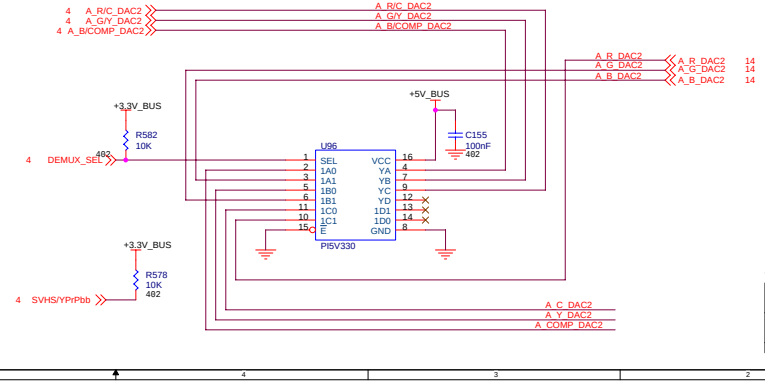
Place close to connector



VIVO CONNECTOR



DEMUX



<Variant Name>

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Size	Document Number	Rev
Custom	Rage Theater 1	00B
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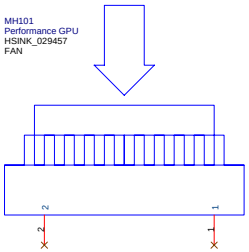
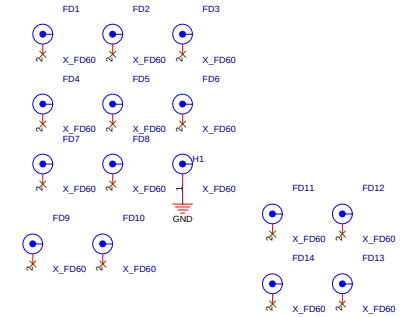
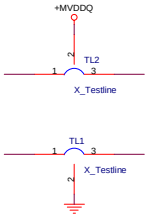
Heatsink







SCREW1
SCREW
JACKSCREW
<3rd part field>
7020000800

SCREW2
SCREW
JACKSCREW
<3rd part field>
7020000800

SCREW3
SCREW
JACKSCREW
<3rd part field>
7020000800

SCREW4
SCREW
JACKSCREW
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7020000800

PCB
PCB
109-942XX-30
<3rd part field>

Bracket
ANTISTATIC BAG
BRACKET
<3rd part field>

<Variant Name>

MS 8951 ATI RV360		
Size: Custom	Document Number: Heatsink & Mechanicals	Rev: 00B
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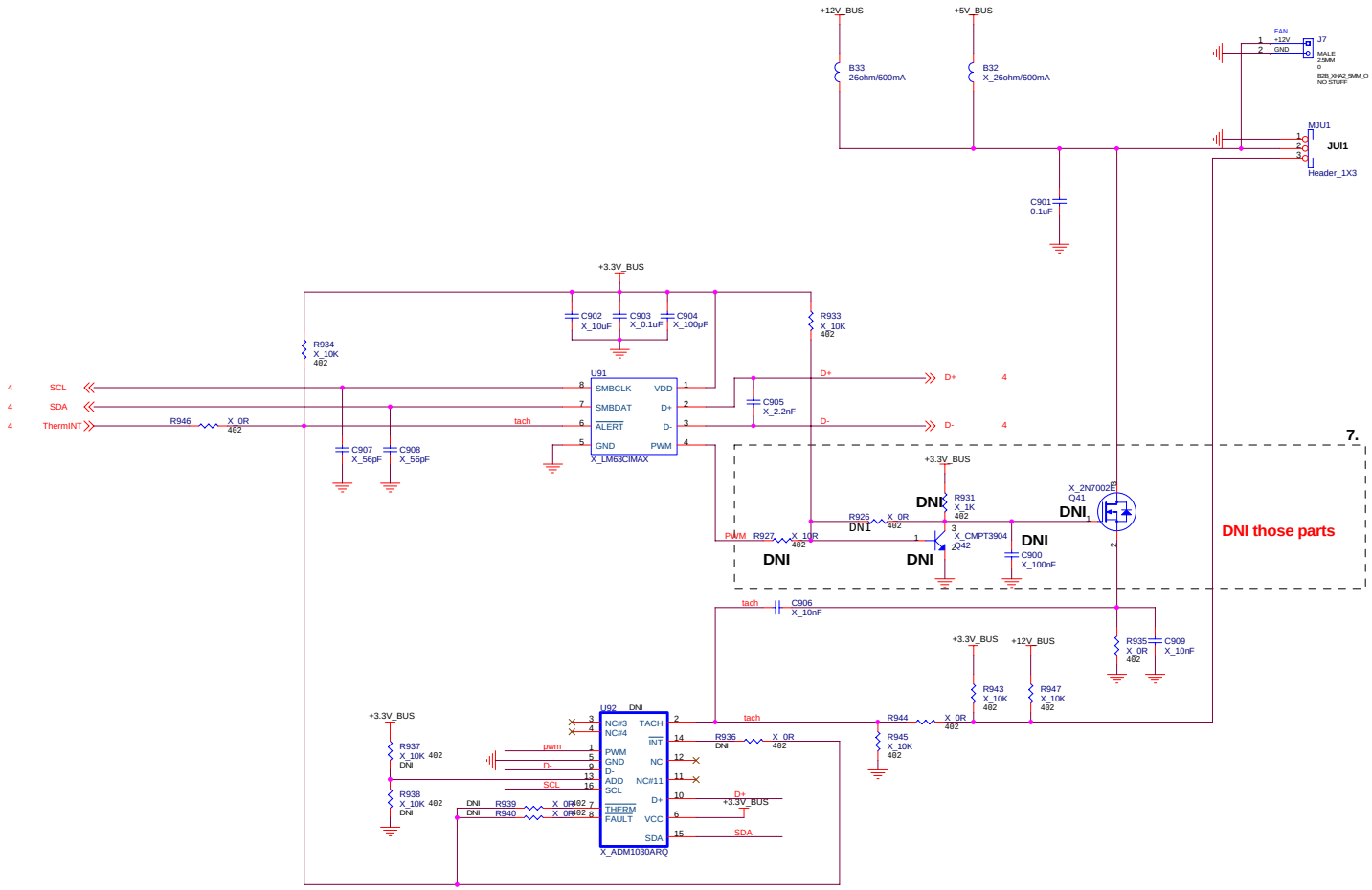
TEMPERATURE SENSE AND SPEED CONTROLLED FAN



<Variant Name>

MS 8951 ATI RV360		
Size: Custom	Document Number: Thermal Management	Rev: 00B
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