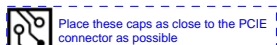




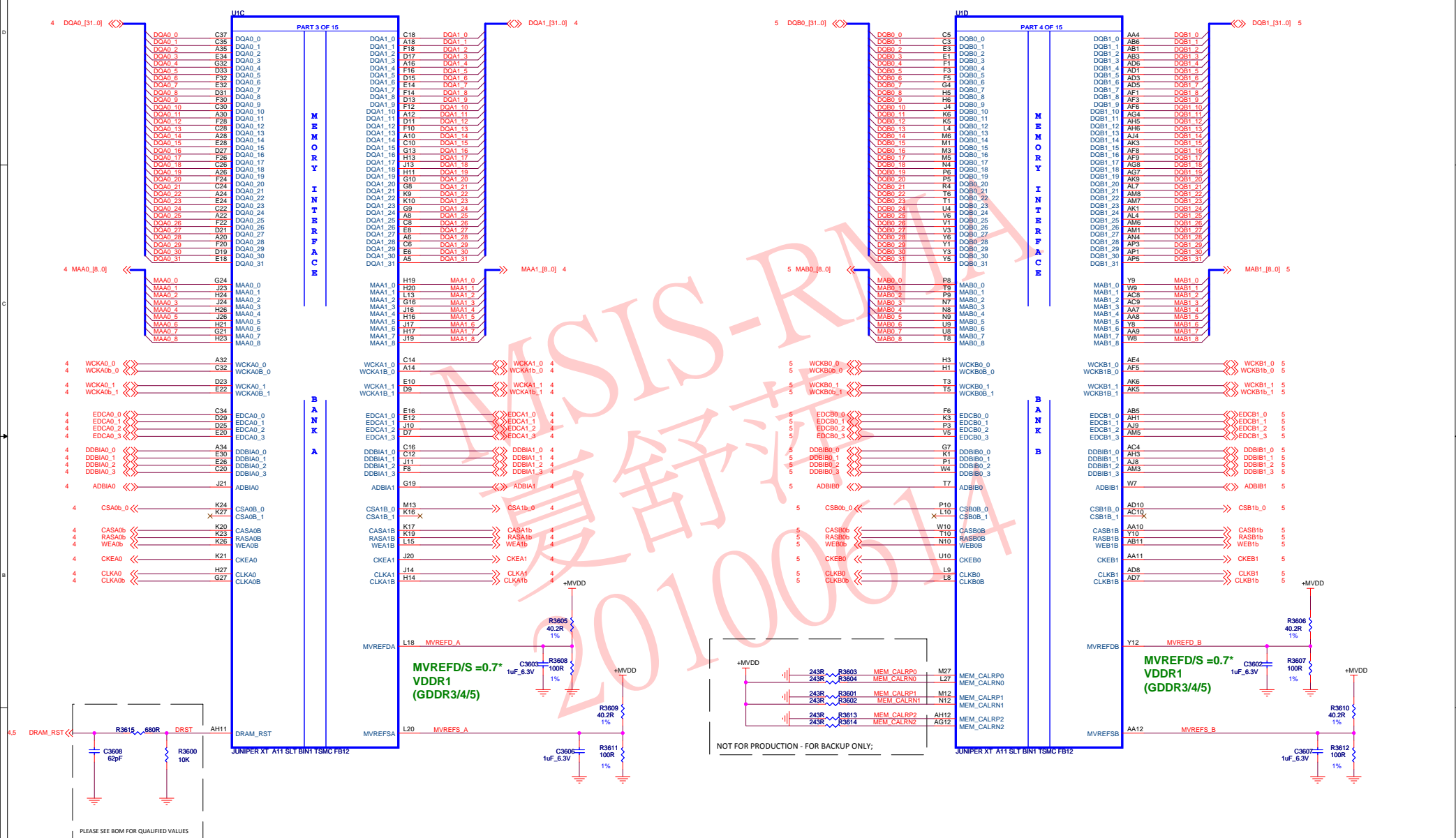
CORVETTE



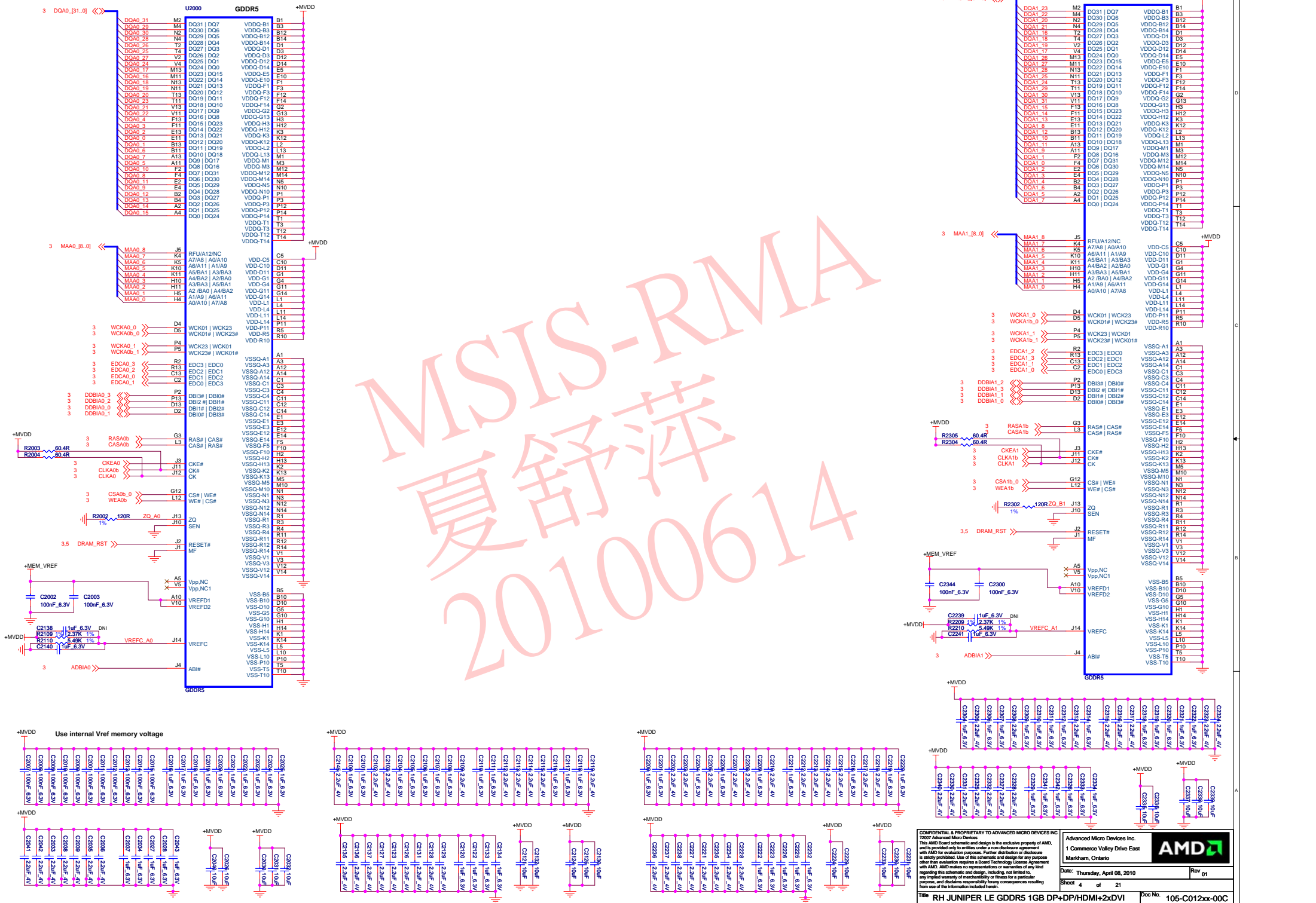
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

Doc No. 105-C012xx-00C

(3) JUNIPER MEM Interface Ch A&B



(4) GDDR5 x32 MEM Channel A

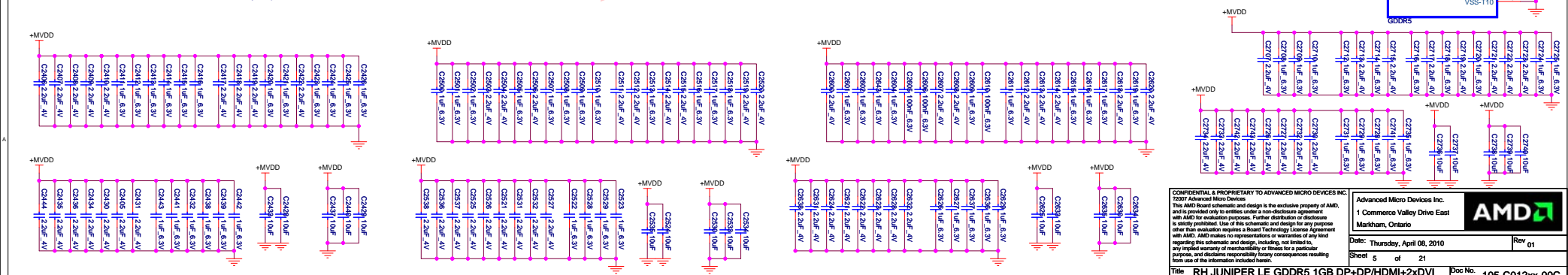
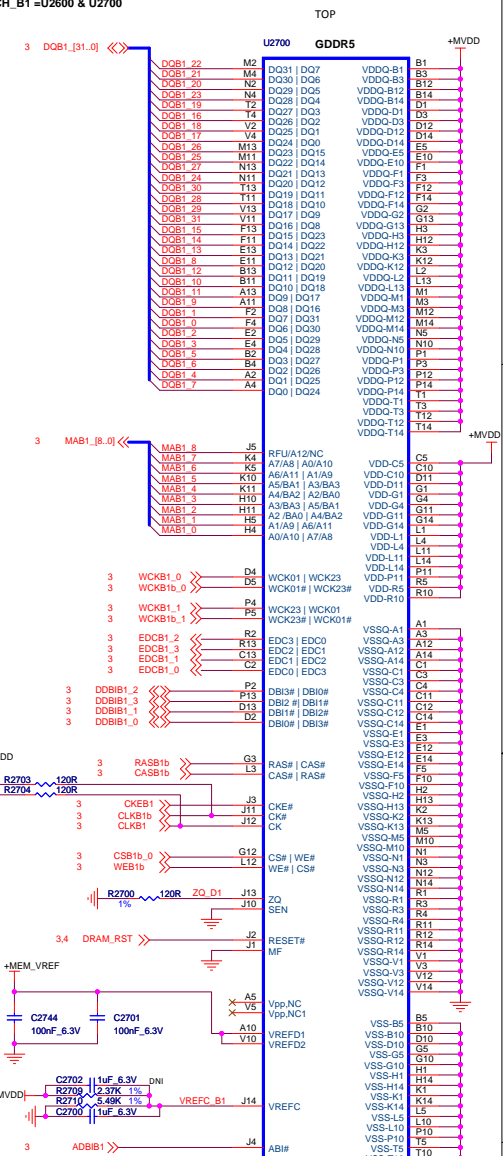
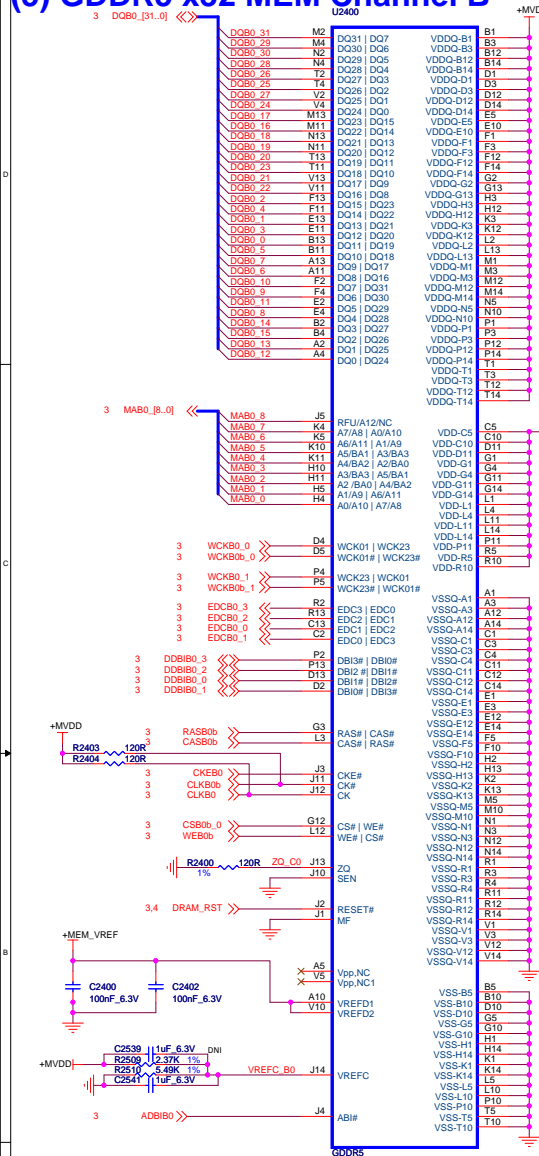


(5) GDDR5 x32 MEM Channel B

CH_B0 =U2400 & U2500


CH_B1 =U2600 & U2700

TOP

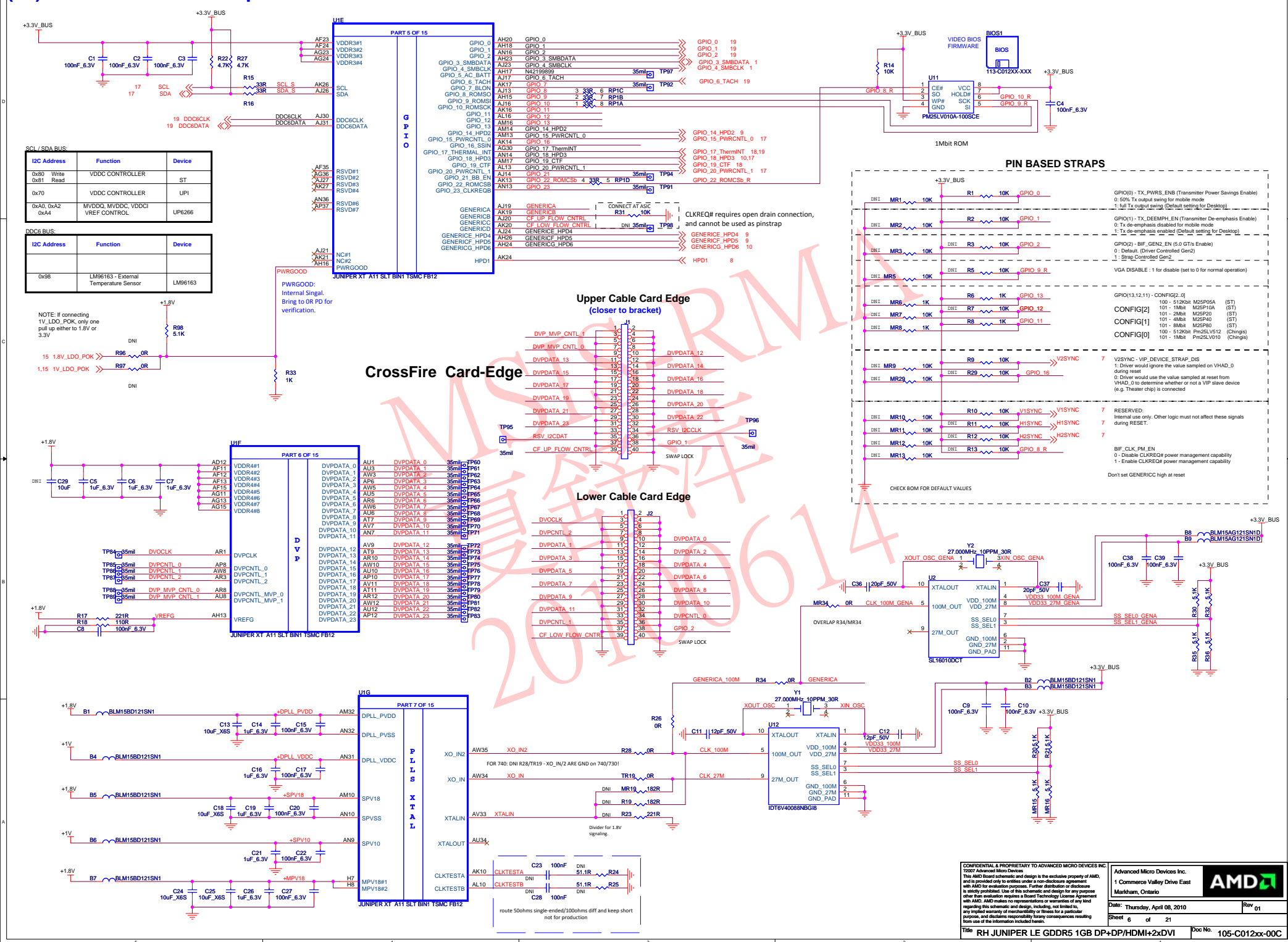


CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES
72007 Advanced Micro Devices

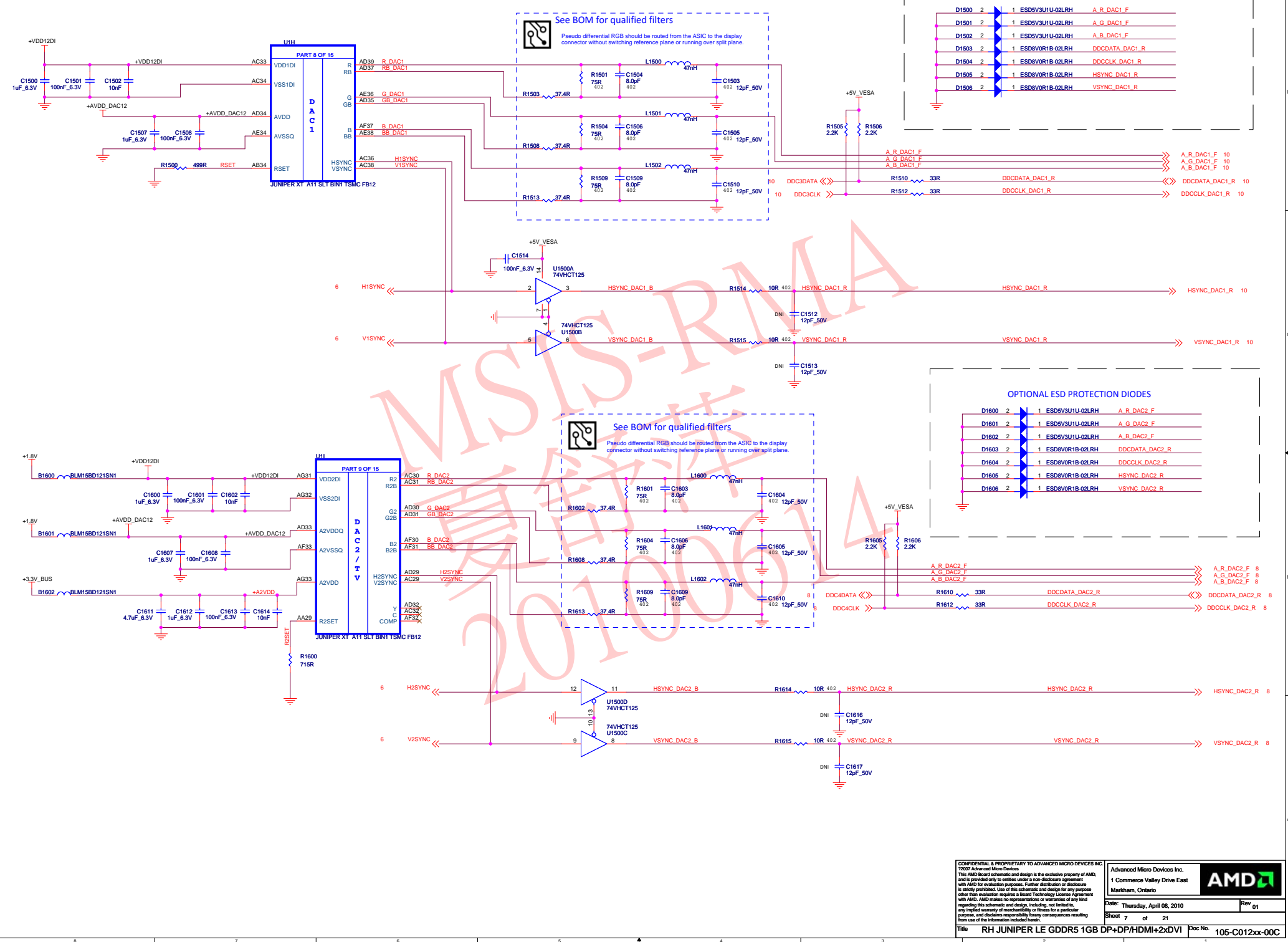
This AMD Board schematic and design is the exclusive property of AMD and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

INC. Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario			
Date: Thursday, April 08, 2010		Rev 01	
Sheet 5 of 21			

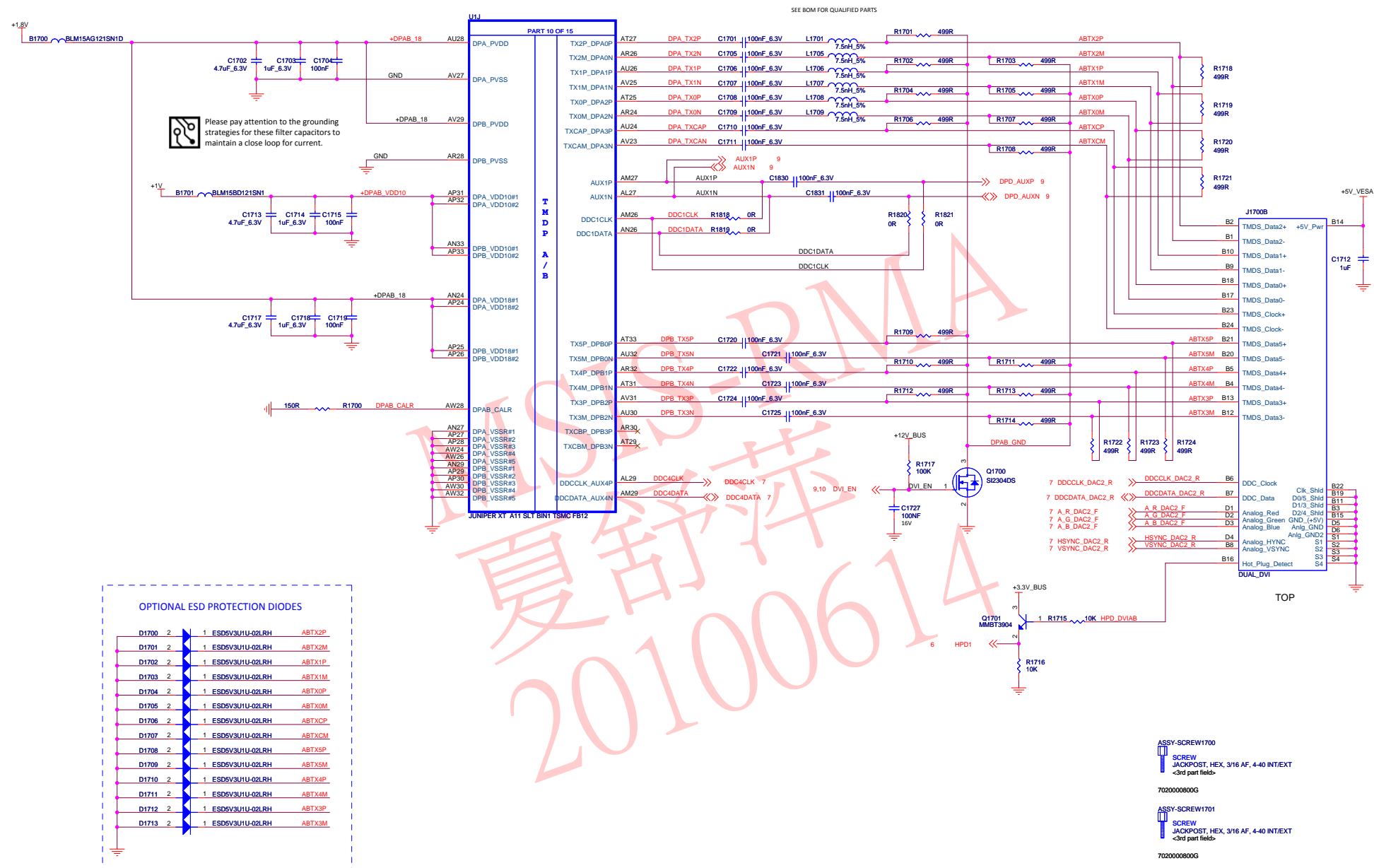
(06) JUNIPER GPIOs Strap CF XTAL OSC




(07) JUNIPER DAC1 and DAC2



(08) JUNIPER TMDP A&B dDVI-I TOP




ASSY-SCREW1700

 SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

7020000800G

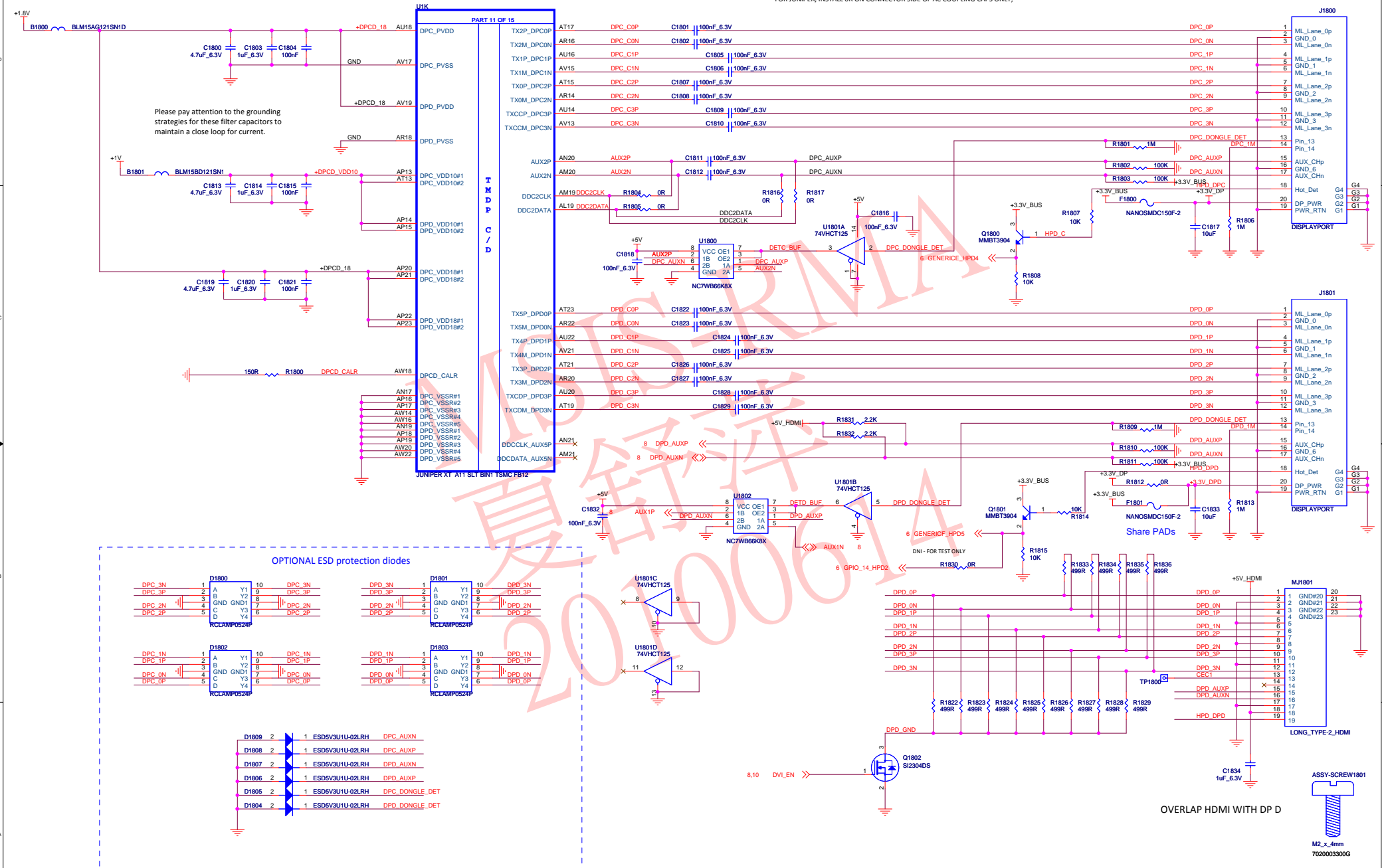
ASSY-SCREW1701

 SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

7020000800G

(09) JUNIPER Display Port C & Display Port/HDMI D

AUX/DDC:
FOR 740/730, INSTALL OR ON ASIC-SIDE OF AC COUPLING CAPS ONLY;
FOR JUNIPER, INSTALL OR ON CONNECTOR SIDE OF AC COUPLING CAPS ONLY;



CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.
72007 Advanced Micro Devices

This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims any and all liability for any consequences resulting from use of the information, including but not limited to, any damages, costs, or expenses, whether incurred or not, in connection with the use of the information.

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario



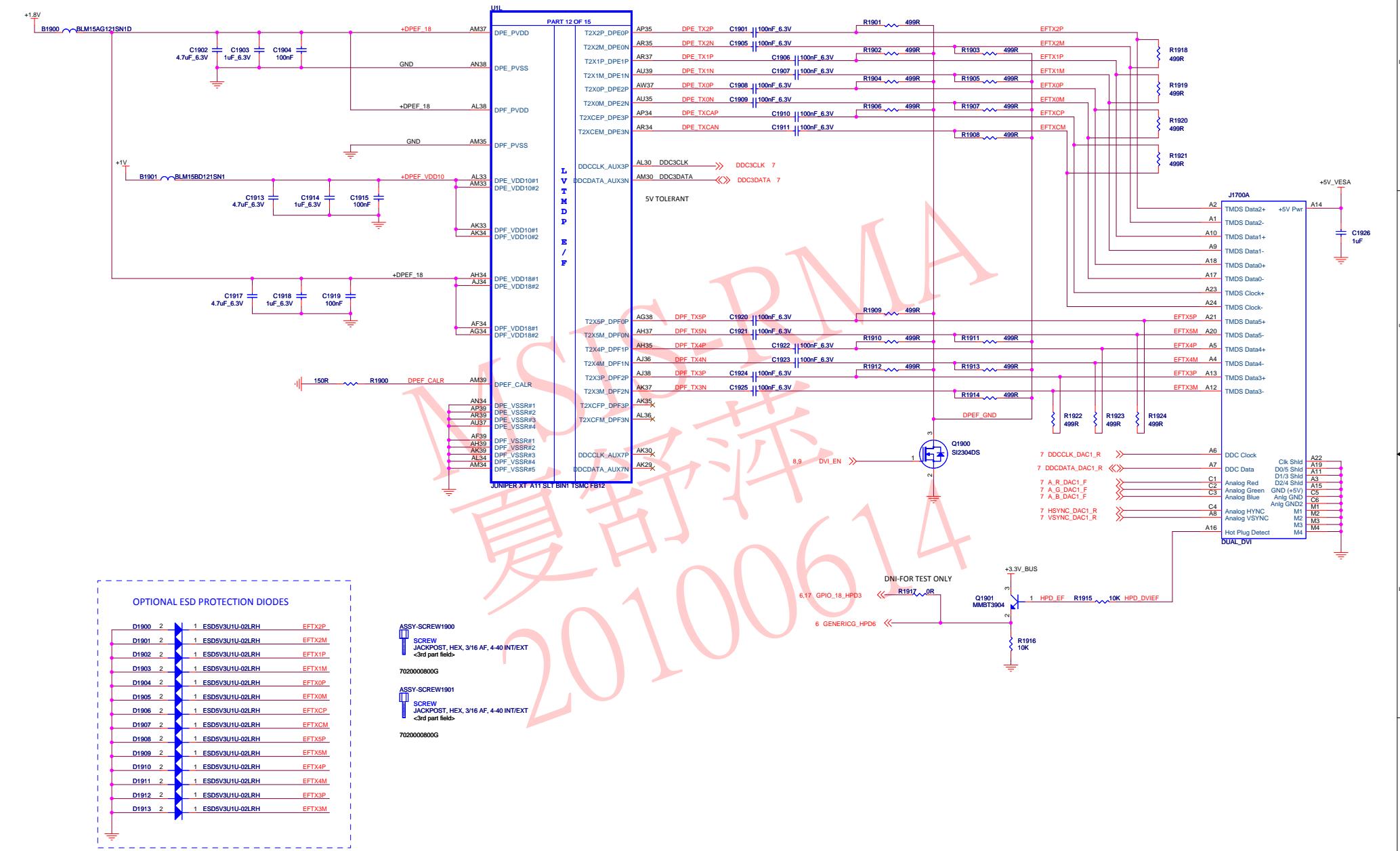
Date: Thursday, April 08, 2010

Sheet 9 of 21

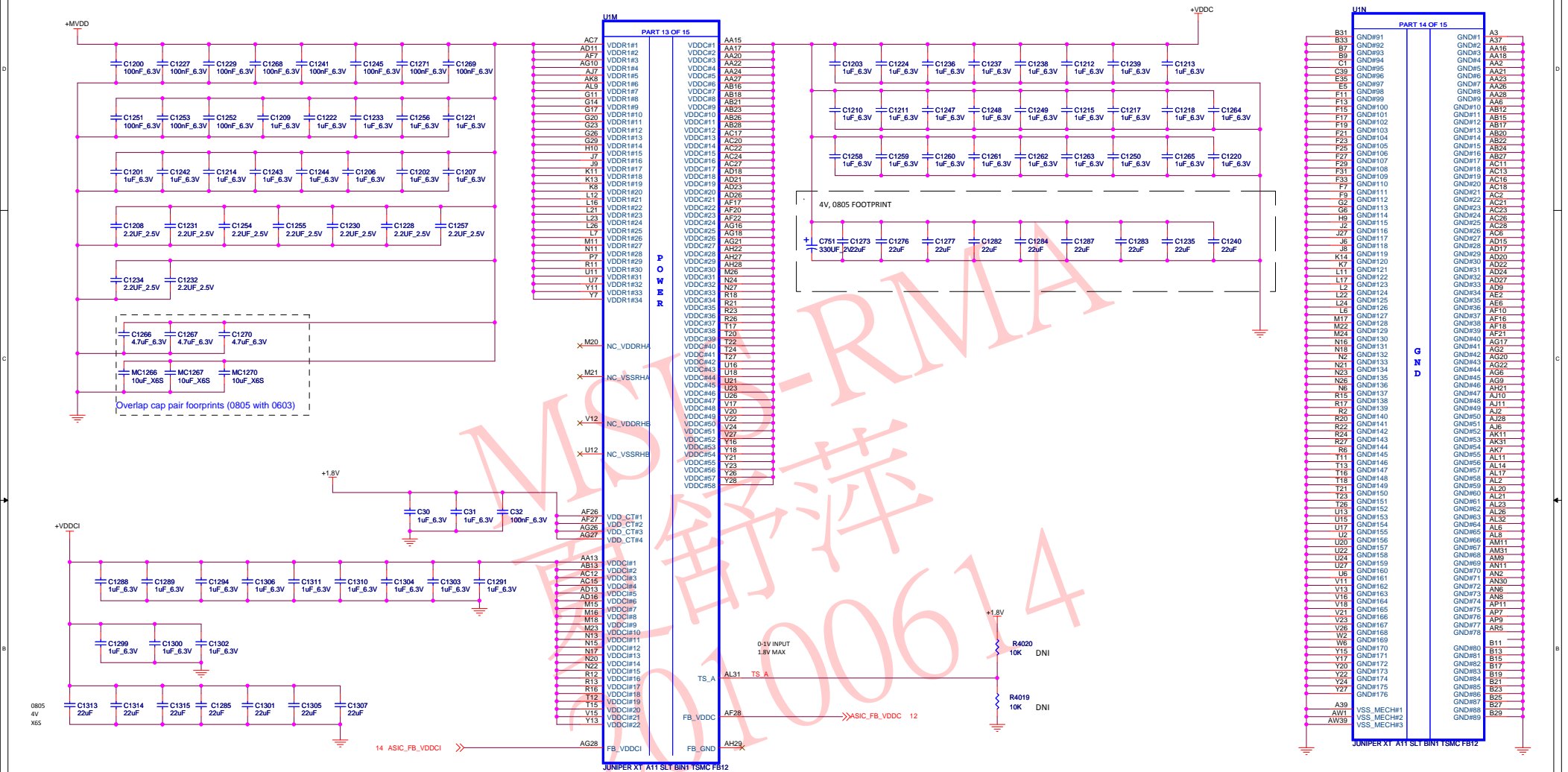
Rev 01

Title	BH JUNIPER LE GDDR5 1GB DP+DP/HDMI+2xDVI	Doc No.	105 C013 rev 00C
-------	--	---------	------------------

(10) JUNIPER LVTMDP E&F dDVI-I BOTTOM



(11) JUNIPER Power & GND



CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.
72007 Advanced Micro Devices

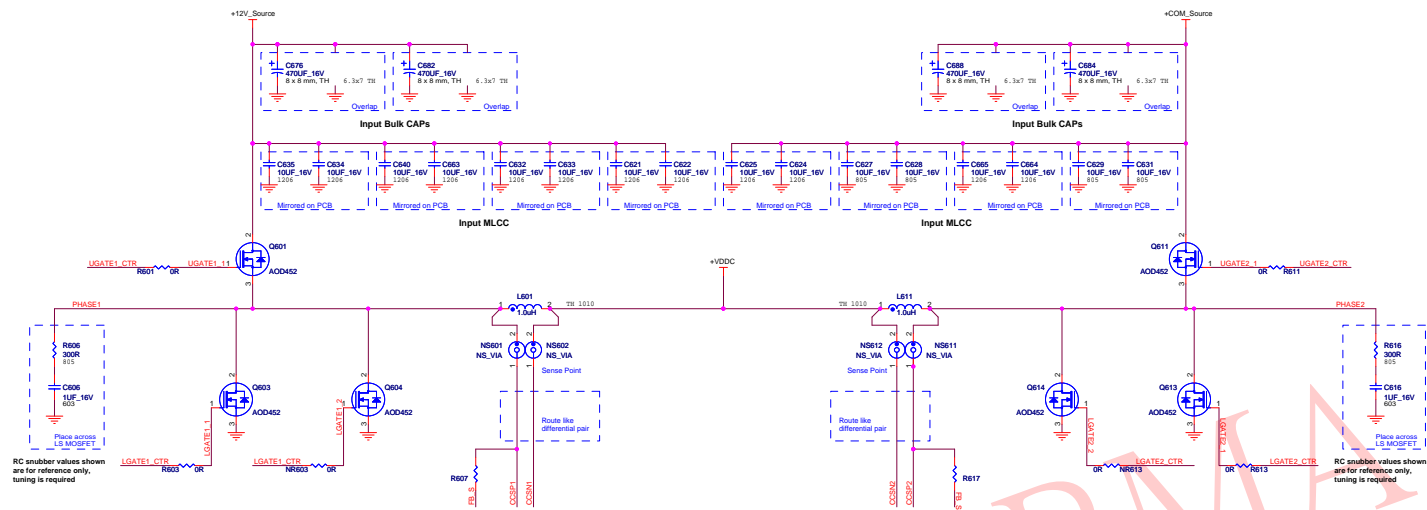
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario



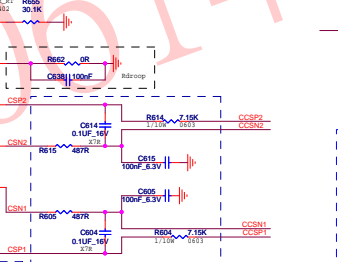
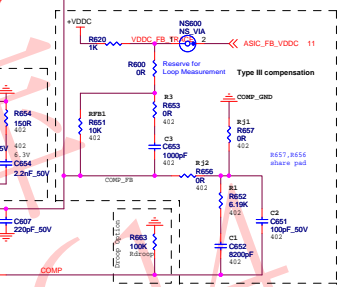
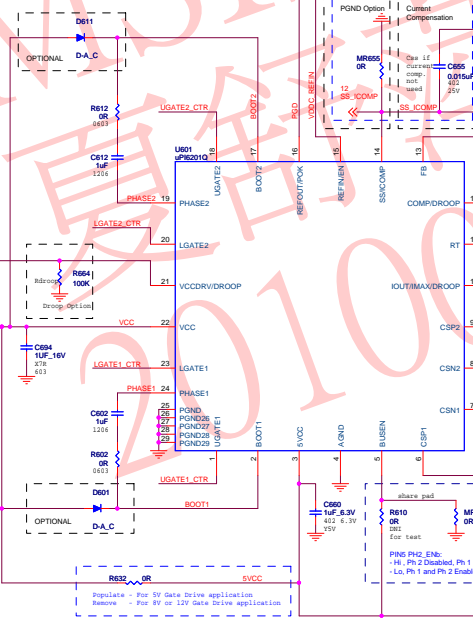
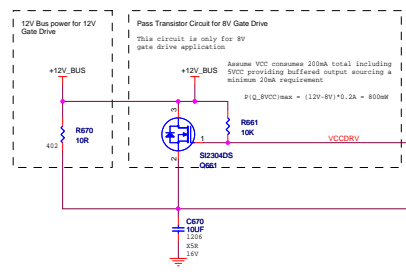
Date: Thursday, April 08, 2010	Rev 01
Sheet 11 of 21	

Title	RH JUNIPER LE GDDR5 1GB DP+DP/HDMI+2xDVI	Doc No.	105-C012xx-00C
-------	--	---------	----------------



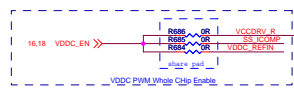
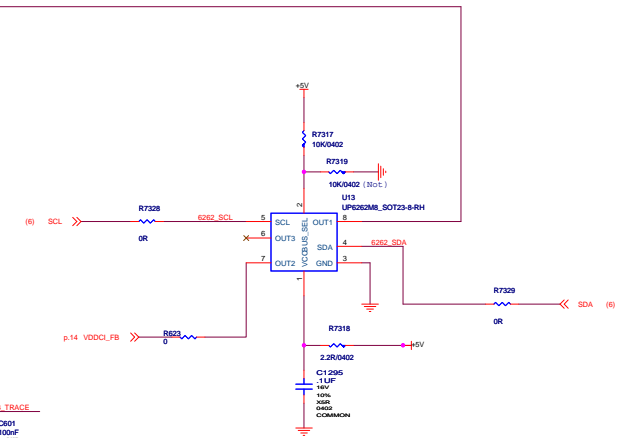
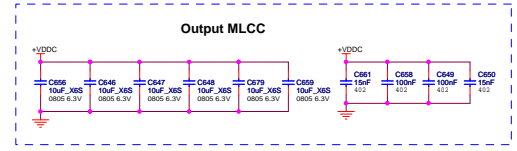
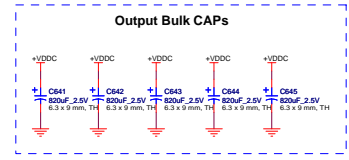
Choosing Different Gate Drive

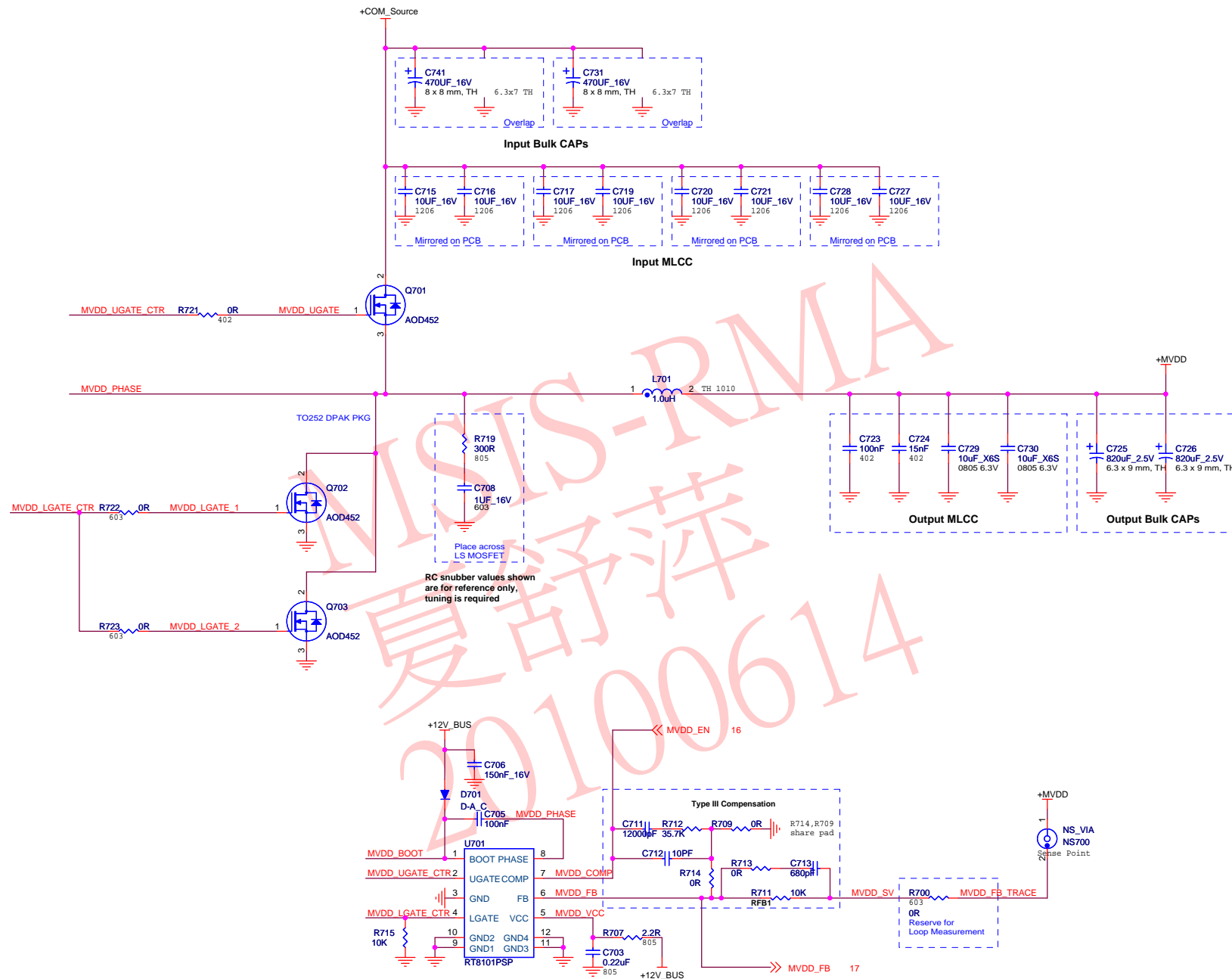
Gate Drive	Populate	Do Not Populate
5V Gate Drive	R831, R832	R830, R870, C860, R861, Q861
8V Gate Drive	R830, C860, R861, Q861	R831, R832, R870
12V Gate Drive	R830, C860, R870	R831, R832, R861, Q861



VDDC applied externally or generated internally from the IC, must be in regulation before IC start up/shut sequence.

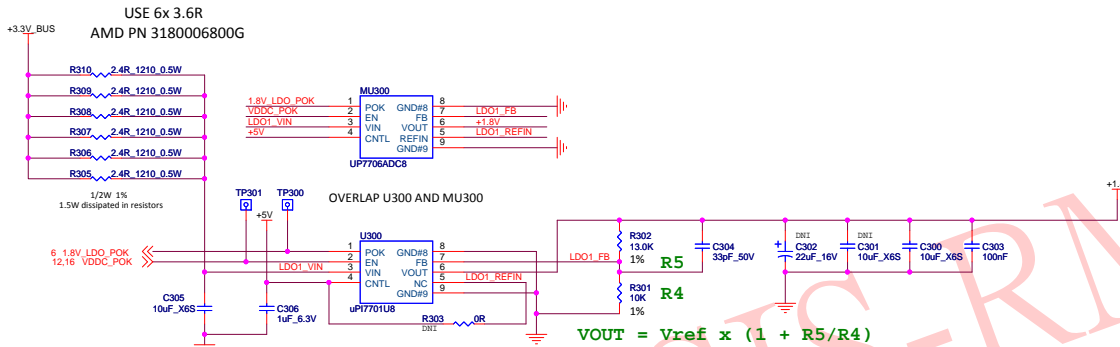
- For 5V Gate Drive application: External filtered +5V_EXT is applied to this pin.
- For 8V or 12V Gate Drive application: +VDDC is generated internally and this is an output with 20mA minimum current capability.



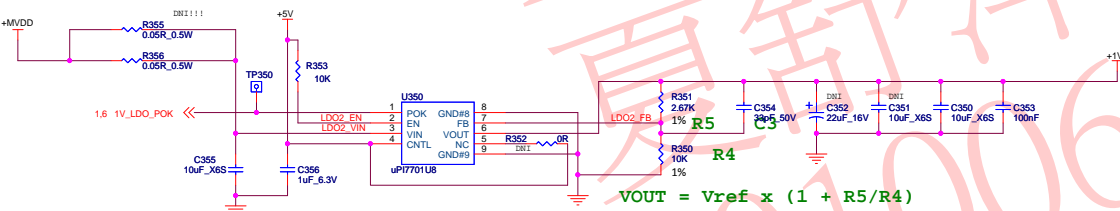


(15) Linear Regulators

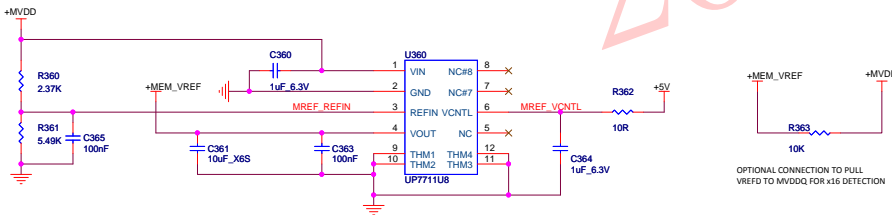
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



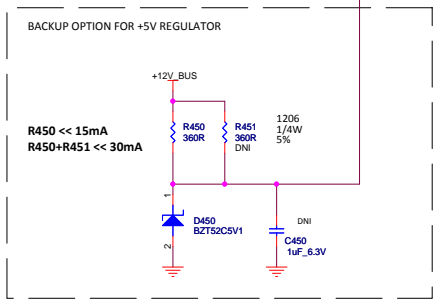
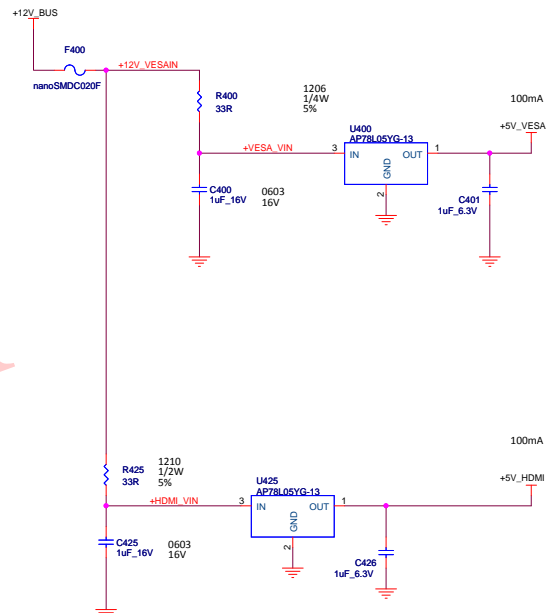
LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ

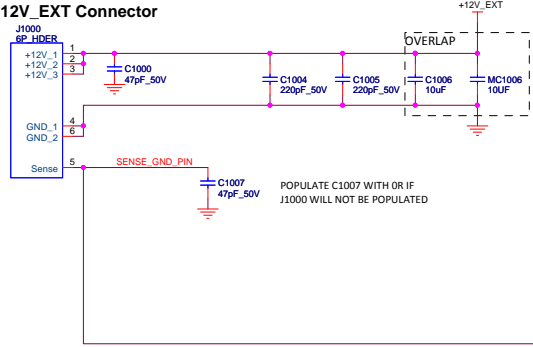


Regulators for +5V, +5V_VESA and +5V_HDMI



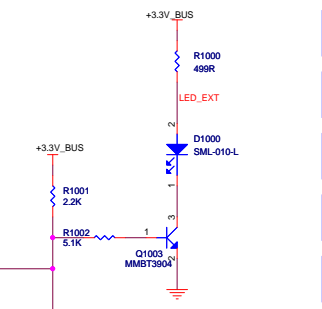
(16) Power Management - Power Gating and External Power Detect

12V_EXT Connector

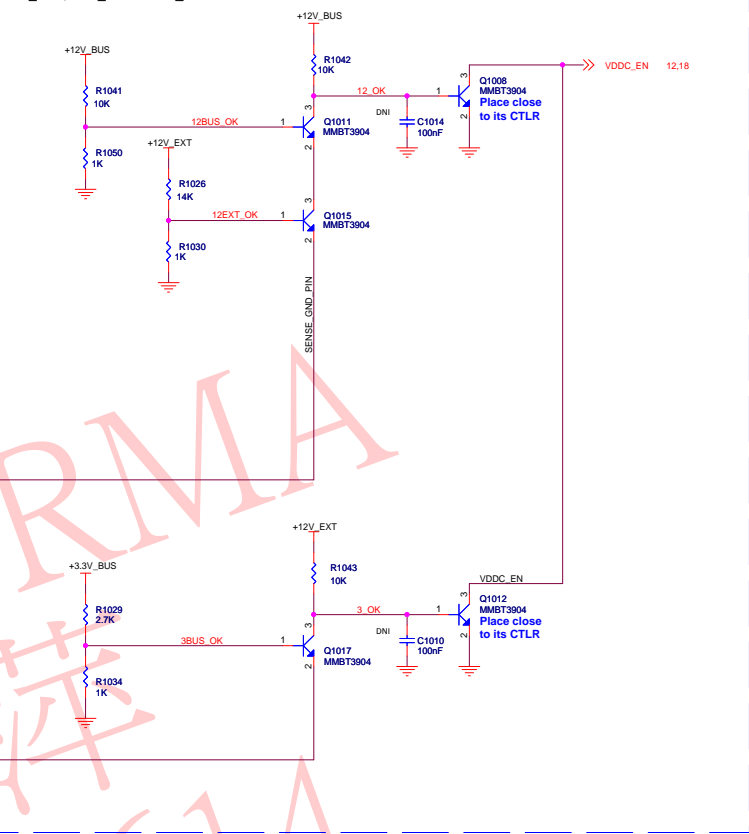


OPTIONAL LED

(LED " ON" indicates 12V_EXT power is not connected)
(client request only)

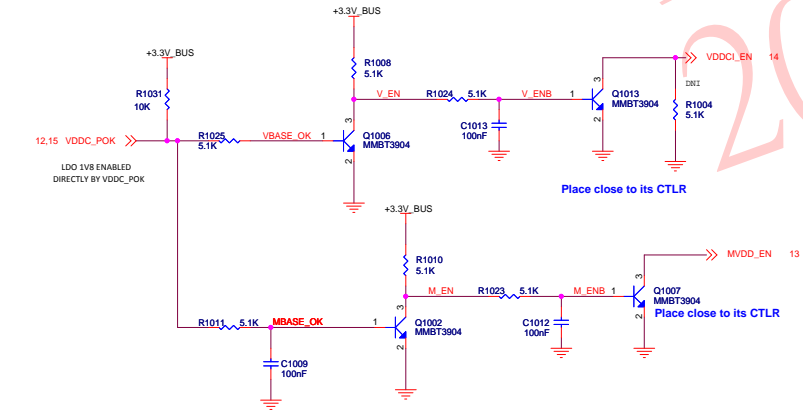


12V_BUS, 12V_EXT & 3V3_BUS POWER SEQUENCING

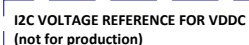
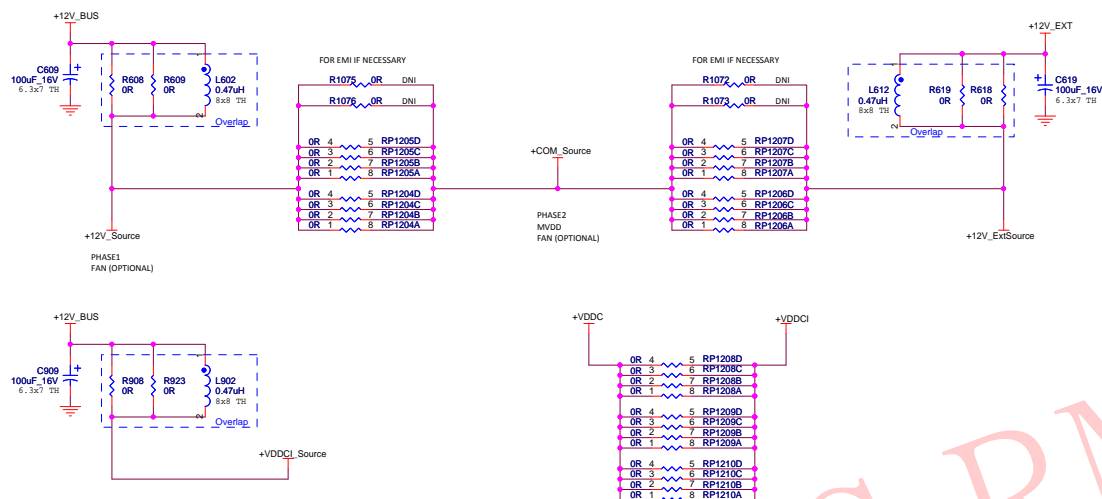


POWER SEQUENCING CIRCUIT

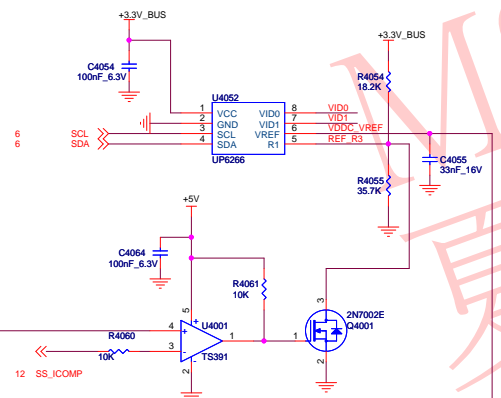
FOR MVDD & VDDCI
(ENABLES CANNOT BE SHARED SINCE IT IS ALSO THE COMPENSATION PIN OF THE SMPS REGULATOR)



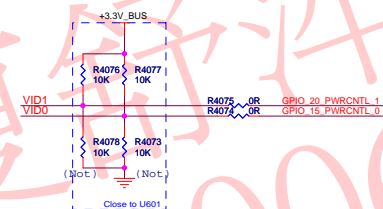
(18) Power Management 2



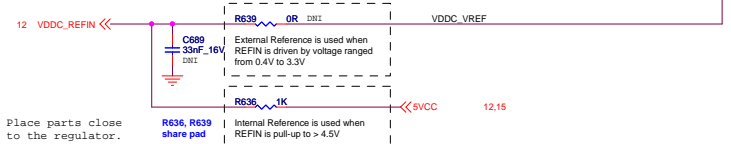
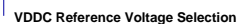
I2C ADDRESS:
A4



GPIO18	Voltage	
0	0.999V	Idle and Video mode
1	1.1V	Boot and 3D mode

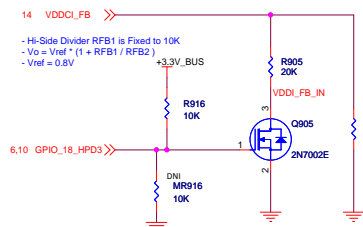
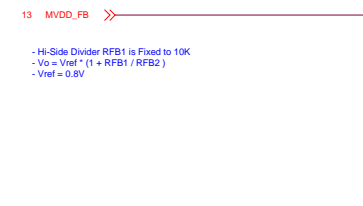
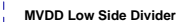


+VDDC Voltage			
GPIO20	GPIO15	Voltage	
0	0	0.955V	Idle mode
0	1	0.997V	
1	0	1.061V	Video mode
1	1	1.1V	Boot and 3D mode

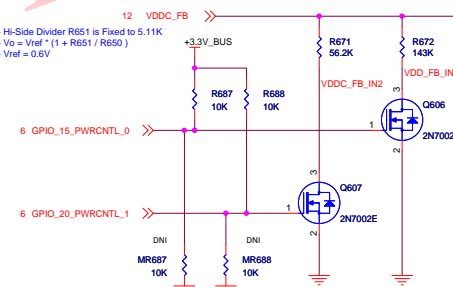


VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

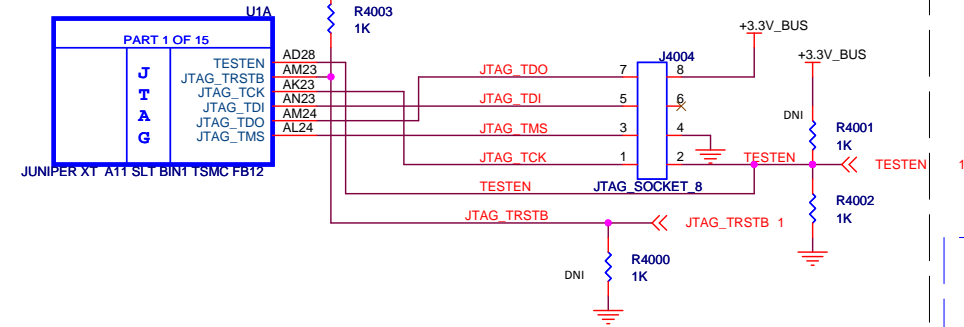


R650 must be populated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.

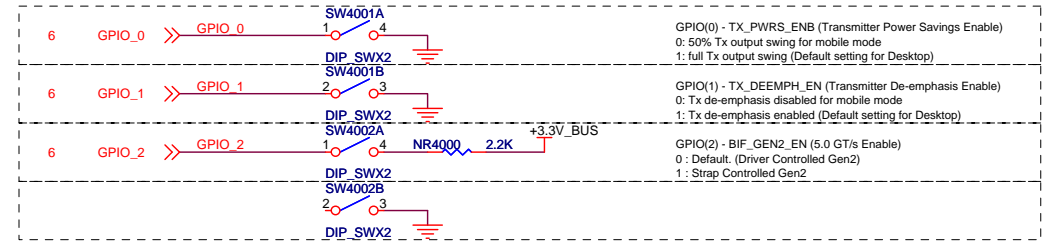


(19) Debug Circuits

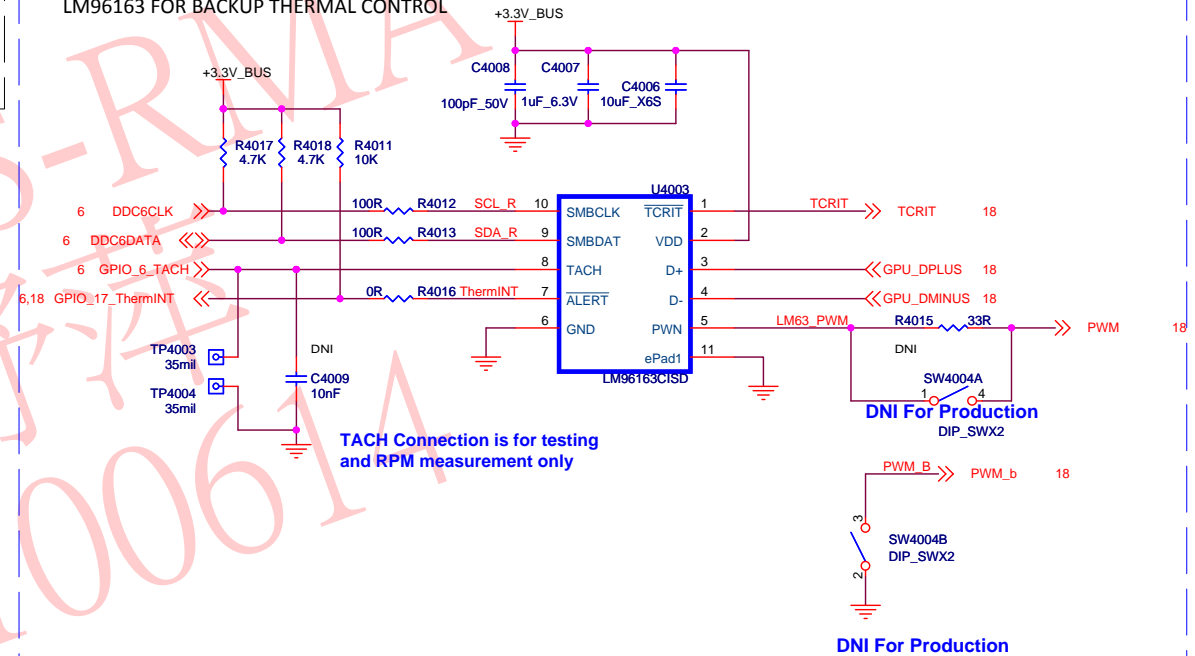
JTAG



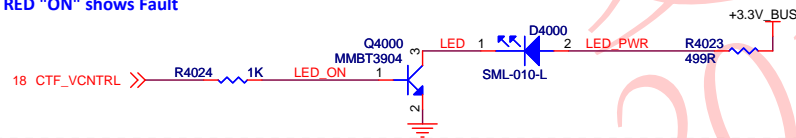
SWITCH CONNECTIONS TO PINSTRAPS



LM96163 FOR BACKUP THERMAL CONTROL



LED RED "ON" shows Fault



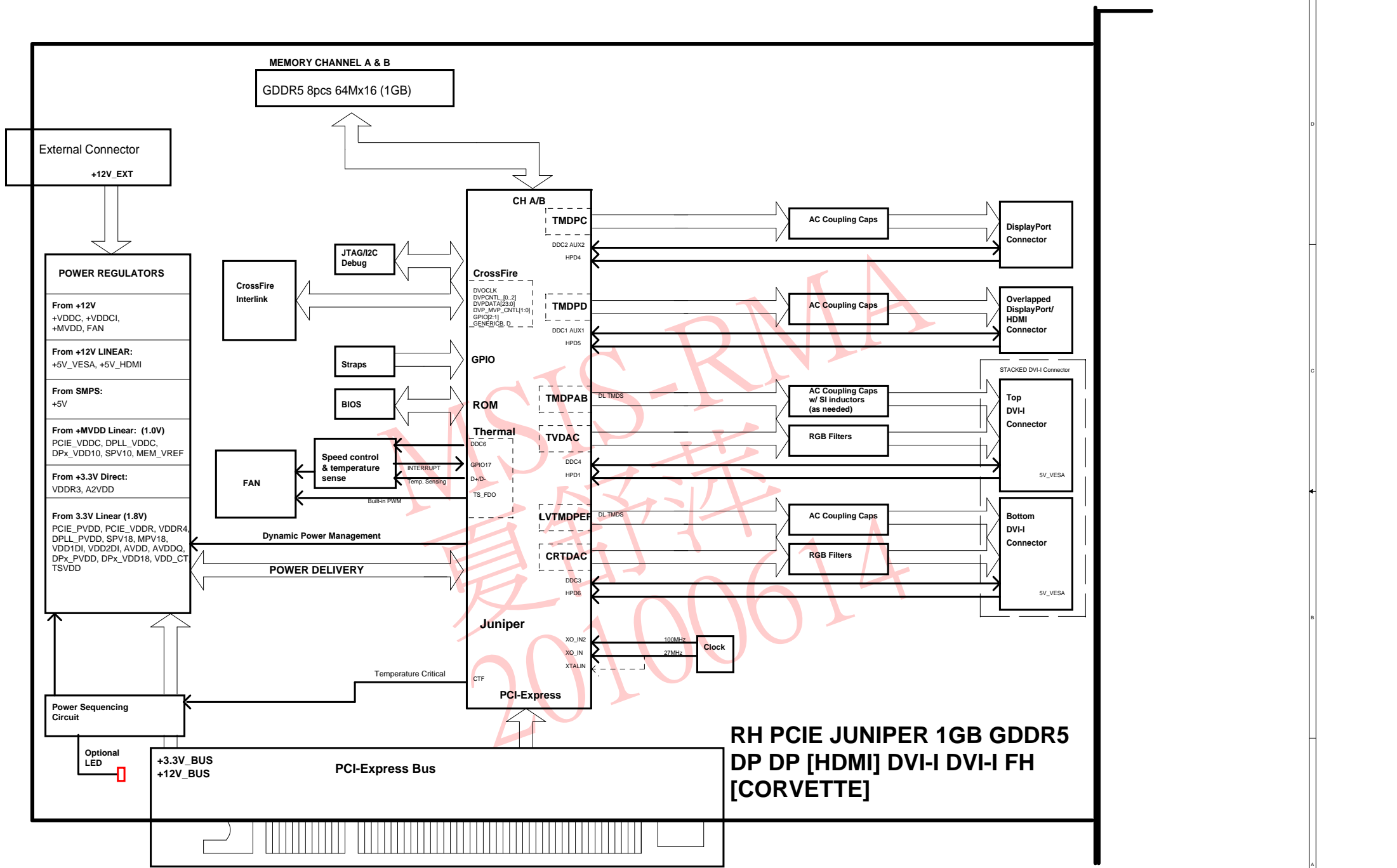
CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.
©2007 Advanced Micro Devices
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario



Date: Thursday, April 08, 2010 Rev 01
Sheet 19 of 21

Title RH JUNIPER LE GDDR5 1GB DP+DP/HDMI+2xDVI Doc No. 105-C012xx-00C



**RH PCIE JUNIPER 1GB GDDR5
DP DP [HDMI] DVI-I DVI-I FH
[CORVETTE]**

<div>AMD</div>			Title		Schematic No.		Date:				
			RH JUNIPER LE GDDR5 1GB DP+DP/HDMI+2xDVI		105-C012xx-00C		Tuesday, April 06, 2010				
			REVISION HISTORY						NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.		Rev 02
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION								
00	00A	2009/03/23	JUNIPER LE GDDR5 1GB - BASED ON C010 REV43;								
01	00B	2009/07/13									
02	00C	2009/09/09	Added PCIe Reset Circuitry								
	20	2010/04/01	Page 04 Removed U2100,U2200 ; U2000,U2300 set to x32 mode Page 05 Removed U2500,U2600 ; U2400,U2700 set to x32 mode Page 08 Add EMI bridge resister R1718~R1724 for DVI top Page 09 Add EMI bridge resister R1833~R1836 for HDMI Page 10 Add EMI bridge resister R1918~R1924 for DVI bot Page 11 Add POSCAP C751 Page 12 Add UP6262 VDDC adj circuit changed VDDC output choke footprint Page 13 changed MVDD output choke footprint Page 14 changed VDDCi output choke footprint Page 17 Add UP6266 VID circuit for VDDC adj Page 18 changed FAN connector to 4pin from 2pin								