

P1041-B01 GF104

GF104-300, 768MB/1536MB, GDDR5 192b 32M/64Mx32
DVI-I-DL, DVI-I-DL/DP, mHDMI

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變更記錄

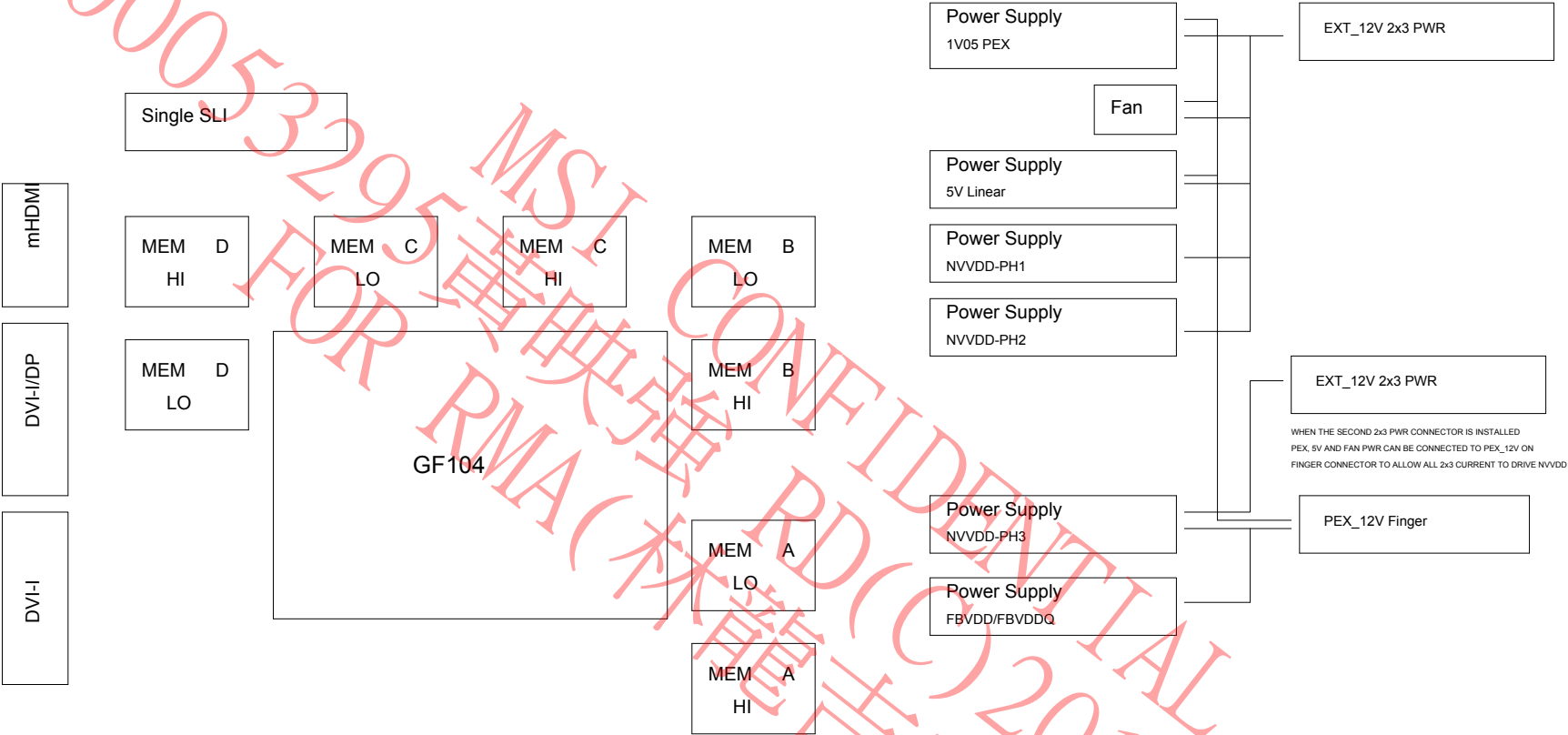
- P3 , C55 change to 1206 10u
- P4~P14 , add 跳頁<>’符號
- P14,刪除所有網絡線
- P17 , add 6262 IC
- P25,刪除原公版U2 & J501. 把I2CC接到6262IC
- P27,接PS1_1V05_FB到6262,U4 foot_print 改為十字的
- P28,改U8的FB接法，換L6為L04-22A8011-L65
- P29 , core部份PWM換UP6213+6284 , OFS電壓開關抬50mV 。 頻率def400KHz，開關抬到600KHz.
- P30-31，加driver IC 6284；去掉3顆input 電容；同時增加6個 LED燈，增加CP1~CP12；為精簡線路，刪除L mos端與 DRV1 0OHm電阻，刪除CSP，CSN 0Ω電阻；更換MOS & 電感；power前4相由PEX6_F1提供，后2相由PEX6_F2 提供；電容部份保留公版。
- P32,去除input 端12V 的LB電感
- P33,加防彎條mec100，加6個十字光學點，加NVVDD，FBVDD &pex_vdd的測試點, 增加阻抗條

REV	VARIANT	RVPM	ASSEMBLY
B	BASE	600-11041-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-11041-0000-300	P1041 GF104-300 768MB GDDR5 32Mx32 QV1+HDMI+HDMI Frame Buffer
2	SKU0010	600-11041-0010-300	P1041 GF104-300 1536MB GDDR5 32Mx32 QV1+HDMI+HDMI Frame Buffer
3	Q01	600-11041-0000-Q01	P1041 GF104-300 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
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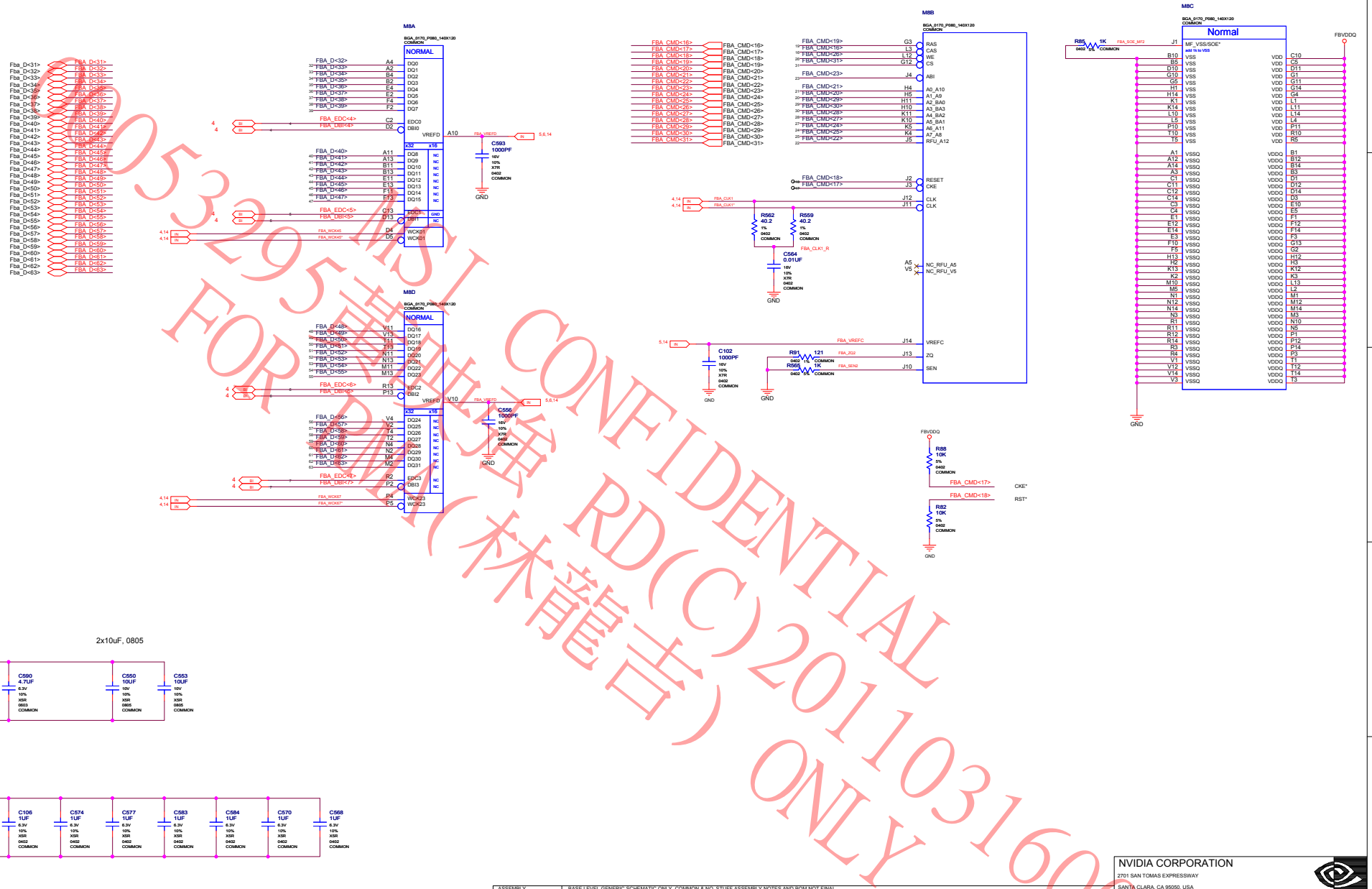
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GDERS CMD Mapping		
CMD	3.31	32.65
CM00	CM07	
CM01	CM07	
CM02	RS07	
CM03	RS07	
CM04	A0_A0	
CM05	A0_A10	
CM06	A02_RPU	
CM07	AB07	
CM08	AB_A11	
CM09	AB_A8	
CM10	AB07	
CM11	A0_BA0	
CM12	A0_BA0	
CM13	A0_BA0	
CM14	A0_BA0	
CM15	CM17	
CM16		CM07
CM17	CM07	
CM18	RS07	
CM19	RS07	
CM20	A0_A0	
CM21	A0_A10	
CM22	A02_RPU	
CM23	AB07	
CM24	AB_A11	
CM25	AB_A8	
CM26	AB07	
CM27	AB_BA0	
CM28	AB_BA0	
CM29	AB_BA0	
CM30	AB_BA0	
CM31	CM17	

** Vref switching options:

- internal Vref should be POR for VrefD
- potential for update



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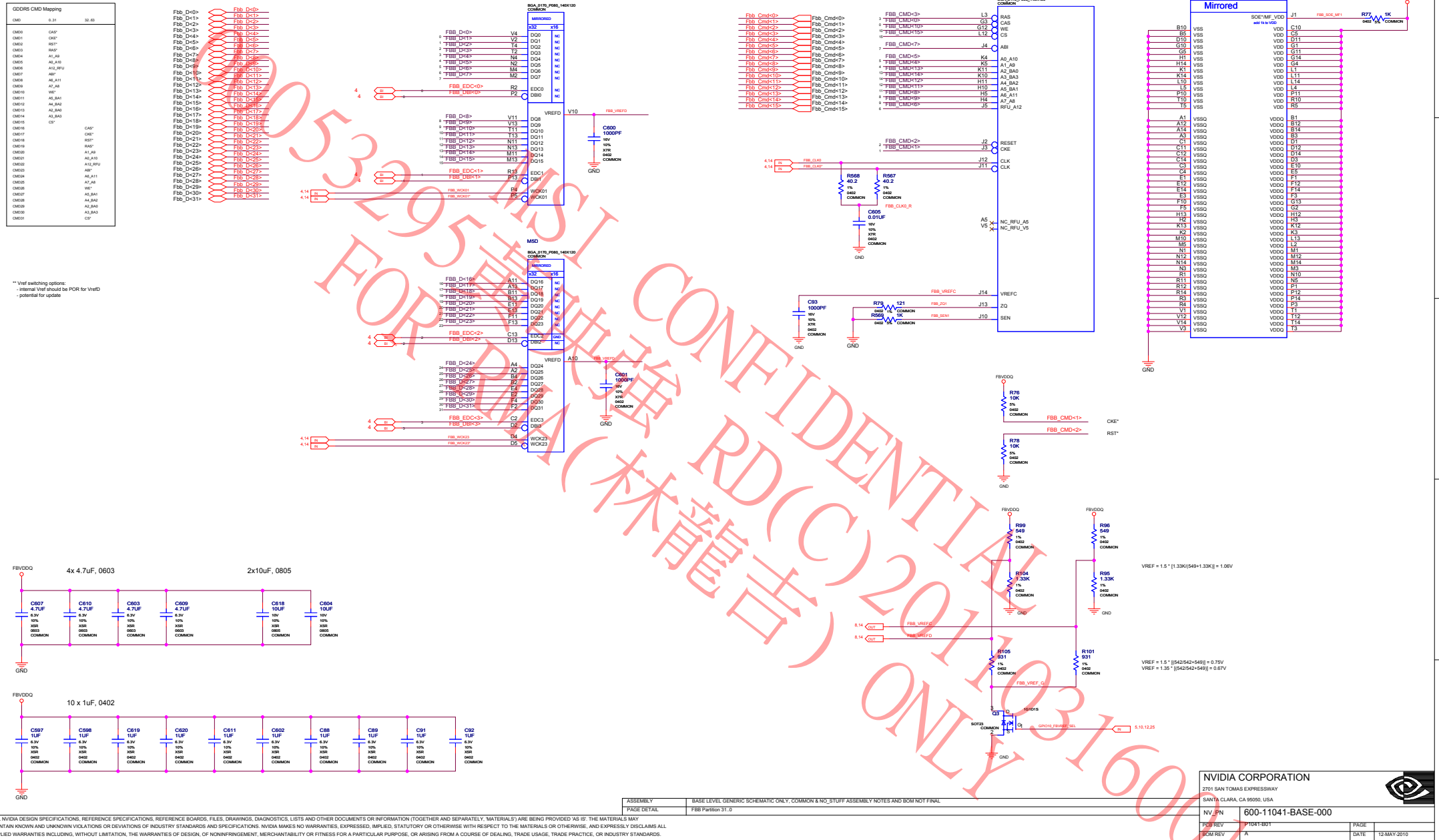
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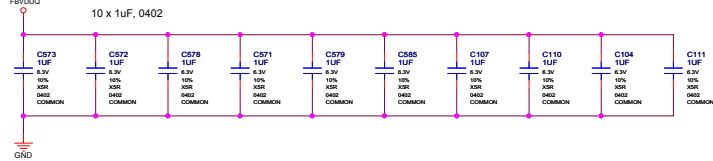
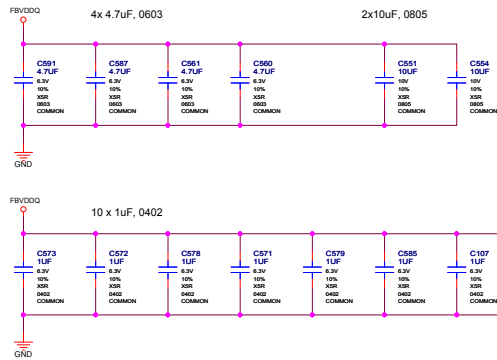
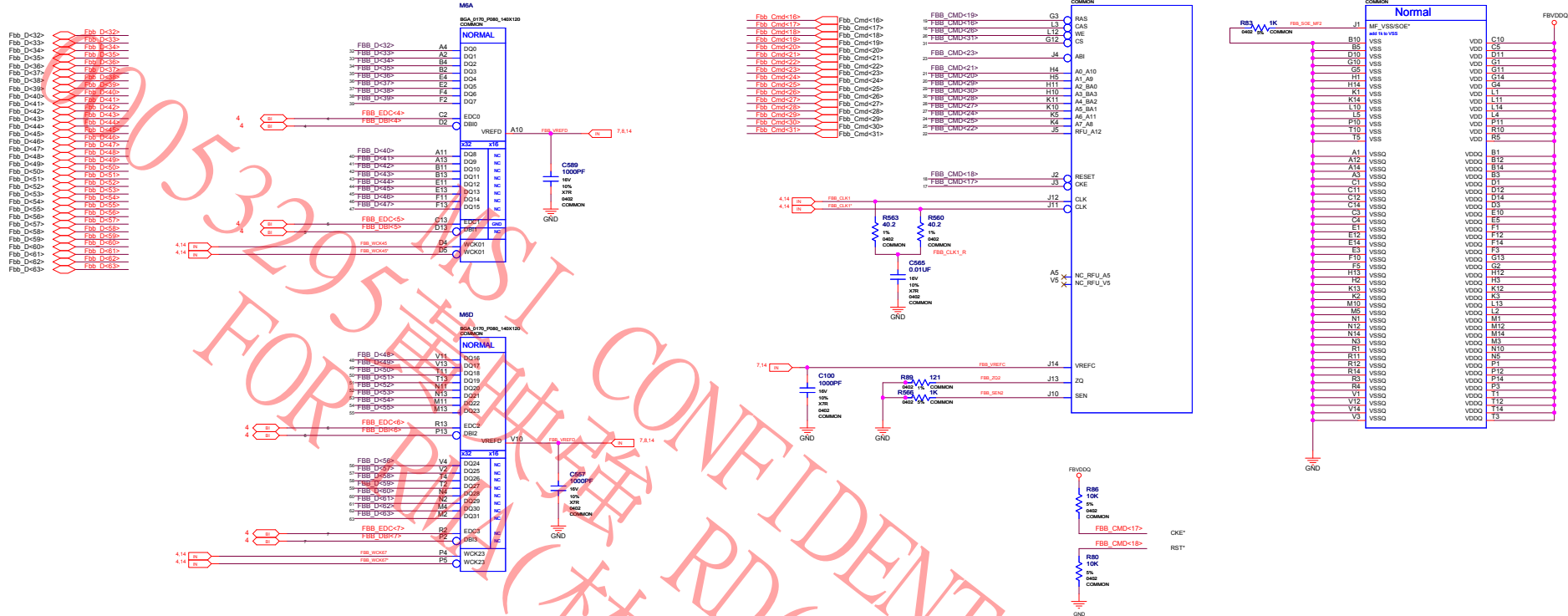
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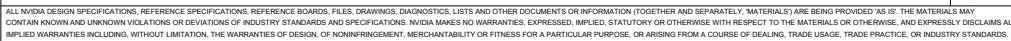


GDRES CMD Mapping		
Cmd	3-31	32-63
CM00	CM07	
CM01	CM07	
CM02	RS07	
CM03	CM07	
CM04	A0_A09	
CM05	A0_A10	
CM06	A02_RPU	
CM07	MEM	
CM08	A0_A11	
CM09	A7_A8	
CM010	MEM	
CM011	A0_BA0	
CM012	A0_BA2	
CM013	A2_BA0	
CM014	A0_BA3	
CM015	CM07	
CM016		CM07
CM017	CM07	
CM018	RS07	
CM019	RS07	
CM020	A0_A0	
CM021	A0_A10	
CM022	A02_RPU	
CM023	MEM	
CM024	A0_A11	
CM025	A7_A8	
CM026	MEM	
CM027	A0_BA0	
CM028	A0_BA2	
CM029	A0_BA0	
CM030	A0_BA3	
CM031	CM07	

** Vref switching options:

- internal Vref should be POR for VrefID
- potential for update





4x 4.7uF, D603

2x10uF, 0805

FBVDDQ

GND

C754 4.7uF 10% XSR 0805 COMMON

C746 4.7uF 10% XSR 0805 COMMON

C753 4.7uF 10% XSR 0805 COMMON

C741 4.7uF 10% XSR 0805 COMMON

C777 10uF 10% XSR 0805 COMMON

C740 10uF 10% XSR 0805 COMMON

FBVDDQ

GND

C739 10uF 10% XSR 0805 COMMON

C755 10uF 10% XSR 0805 COMMON

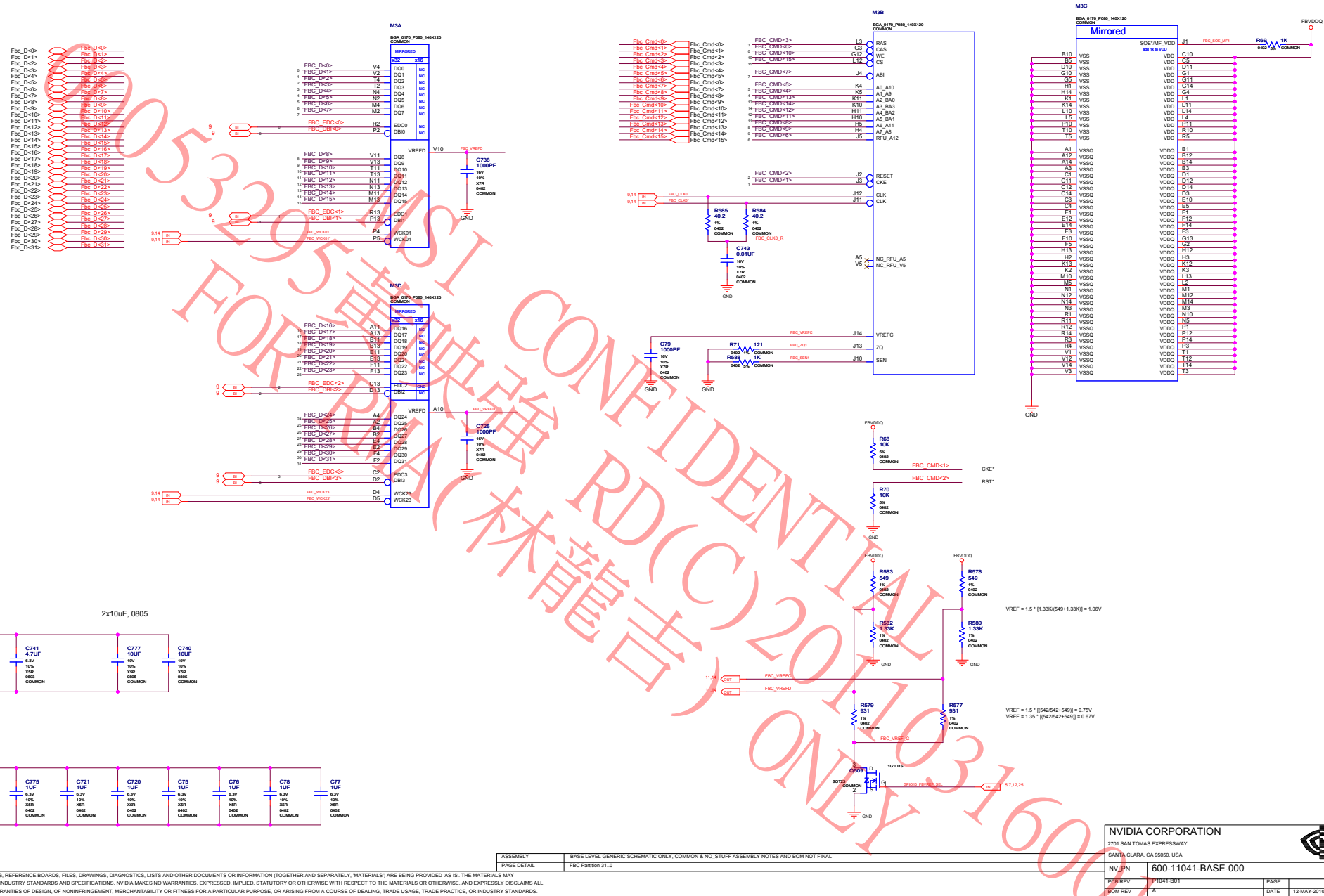
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C775 10uF 10% XSR 0805 COMMON

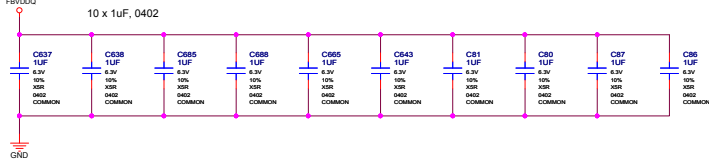
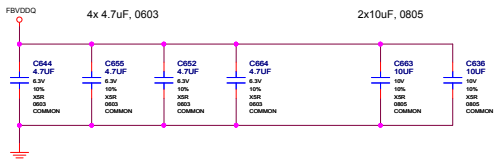
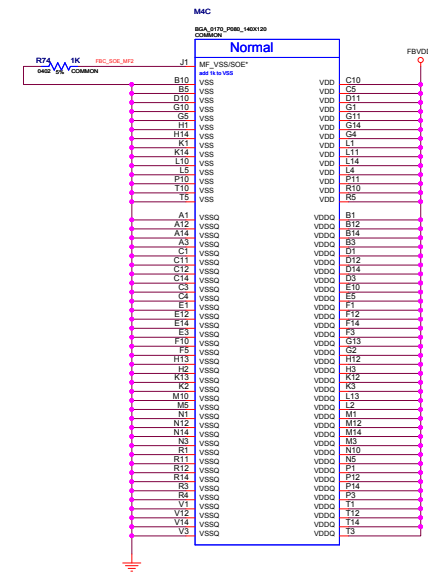
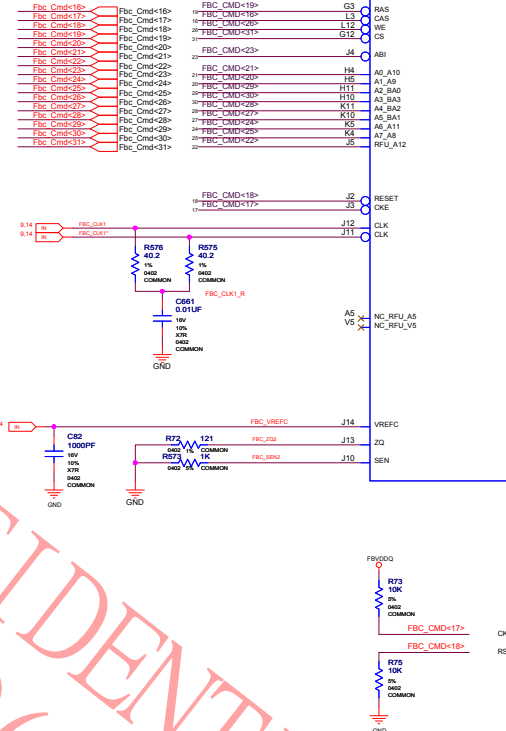
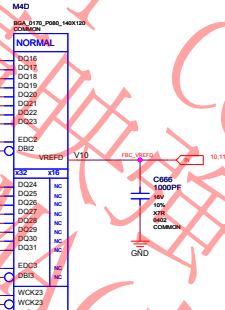
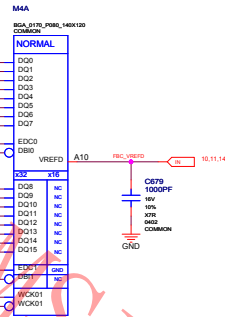
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C720 10uF 10% XSR 0805 COMMON

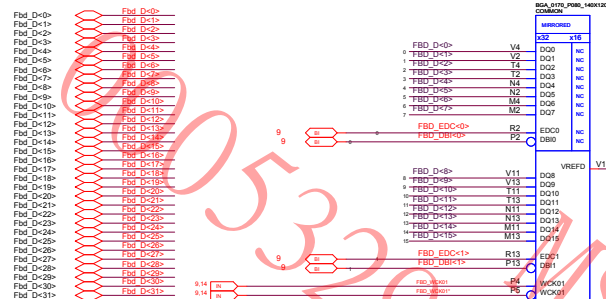
C75 10uF 10% XSR 0805 COMMON



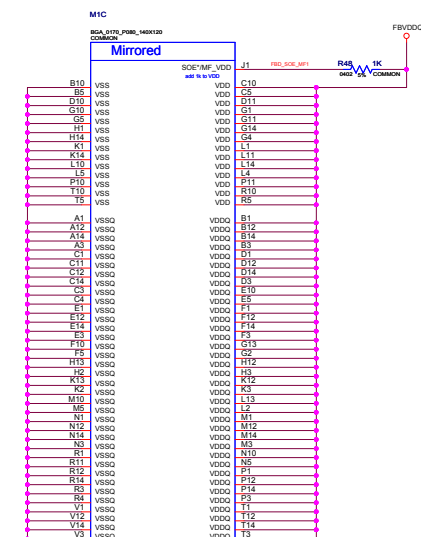
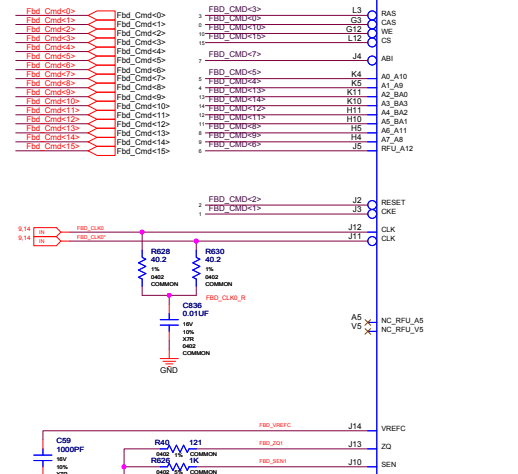
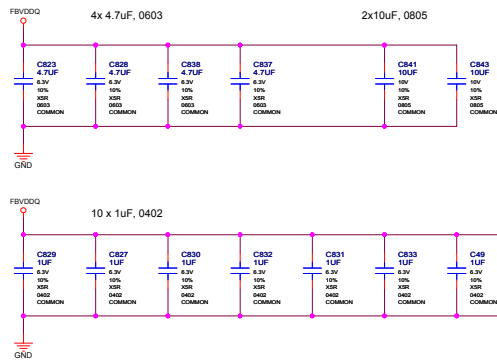
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GDORs CMD Mapping		
Cmd		32_63
CM00	CM07	
CM01	CM08	
CM02	CM09	
CM03	CM10	
CM04	CM11	
CM05	CM12	
CM06	CM13	
CM07	CM14	
CM08	CM15	
CM09	CM16	
CM10	CM17	
CM11	CM18	
CM12	CM19	
CM13	CM20	
CM14	CM21	
CM15	CM22	
CM16	CM23	
CM17	CM24	
CM18	CM25	
CM19	CM26	
CM20	CM27	
CM21	CM28	
CM22	CM29	
CM23	CM30	
CM24	CM31	



** Vref switching options:
- Internal Vref should be POR for VrefD
- potential for update



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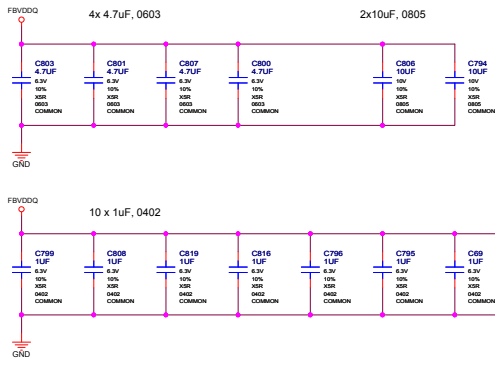
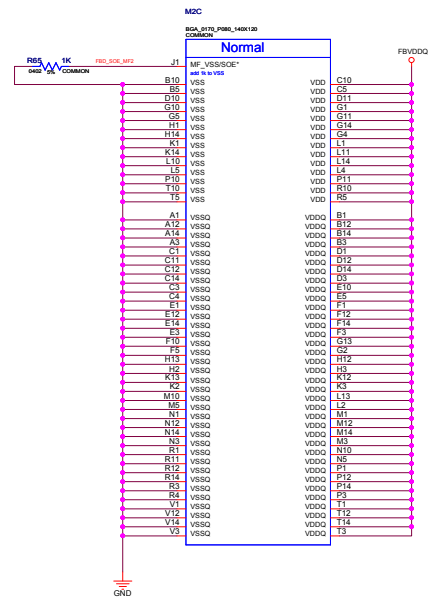
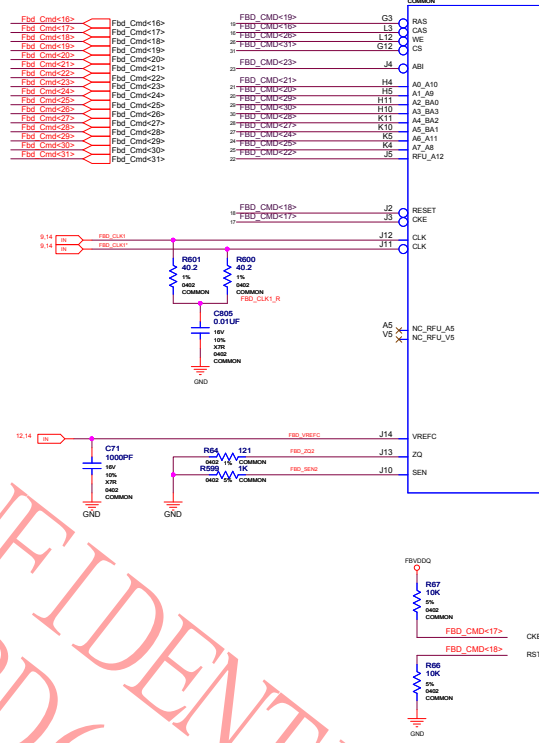
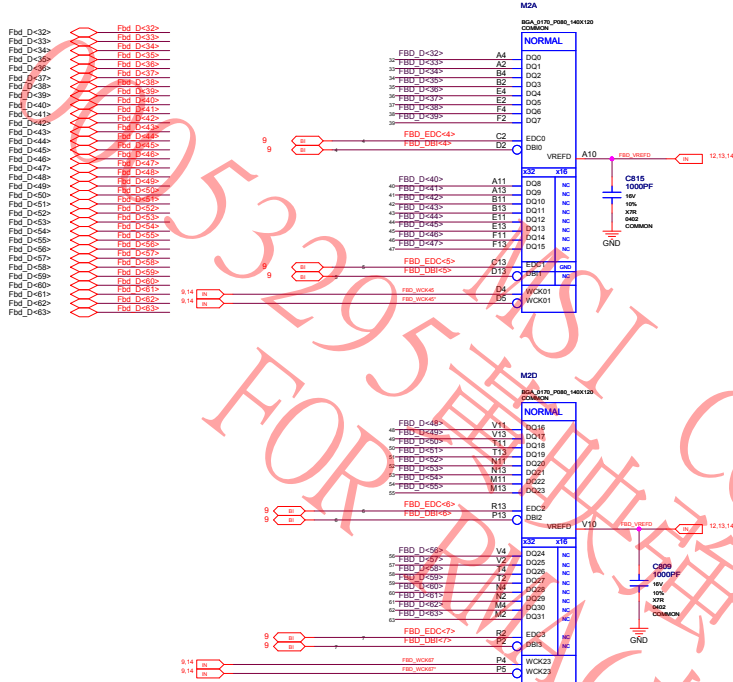
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GDORs CMD Mapping		
CMD	0..31	32..63
CM00	CAS*	
CM01	CAS*	
CM02	RST*	
CM03	RST*	
CM04	AL_A0	
CM05	AL_A10	
CM06	AL_A10	
CM07	AB*	
CM08	AL_A11	
CM09	AT_A0	
CM10	WE*	
CM11	AL_BA1	
CM12	AL_BA2	
CM13	AL_BA3	
CM14	AL_BA3	
CM15	CD*	
CM16	CAS*	
CM17	CAS*	
CM18	RST*	
CM19	RST*	
CM20	AL_A0	
CM21	AL_A10	
CM22	AL_A10	
CM23	AB*	
CM24	AL_A11	
CM25	AT_A0	
CM26	WE*	
CM27	AL_BA1	
CM28	AL_BA2	
CM29	AL_BA3	
CM30	AL_BA3	
CM31	CD*	

** Vref switching options:
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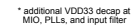
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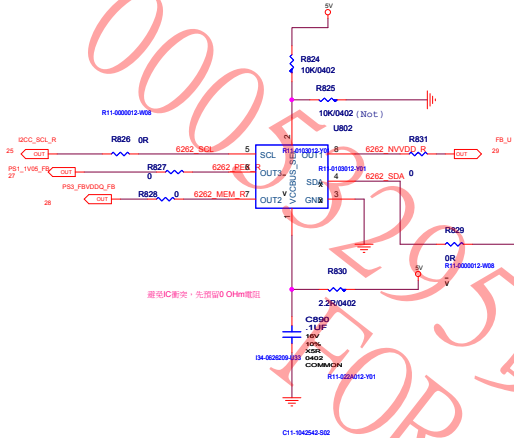
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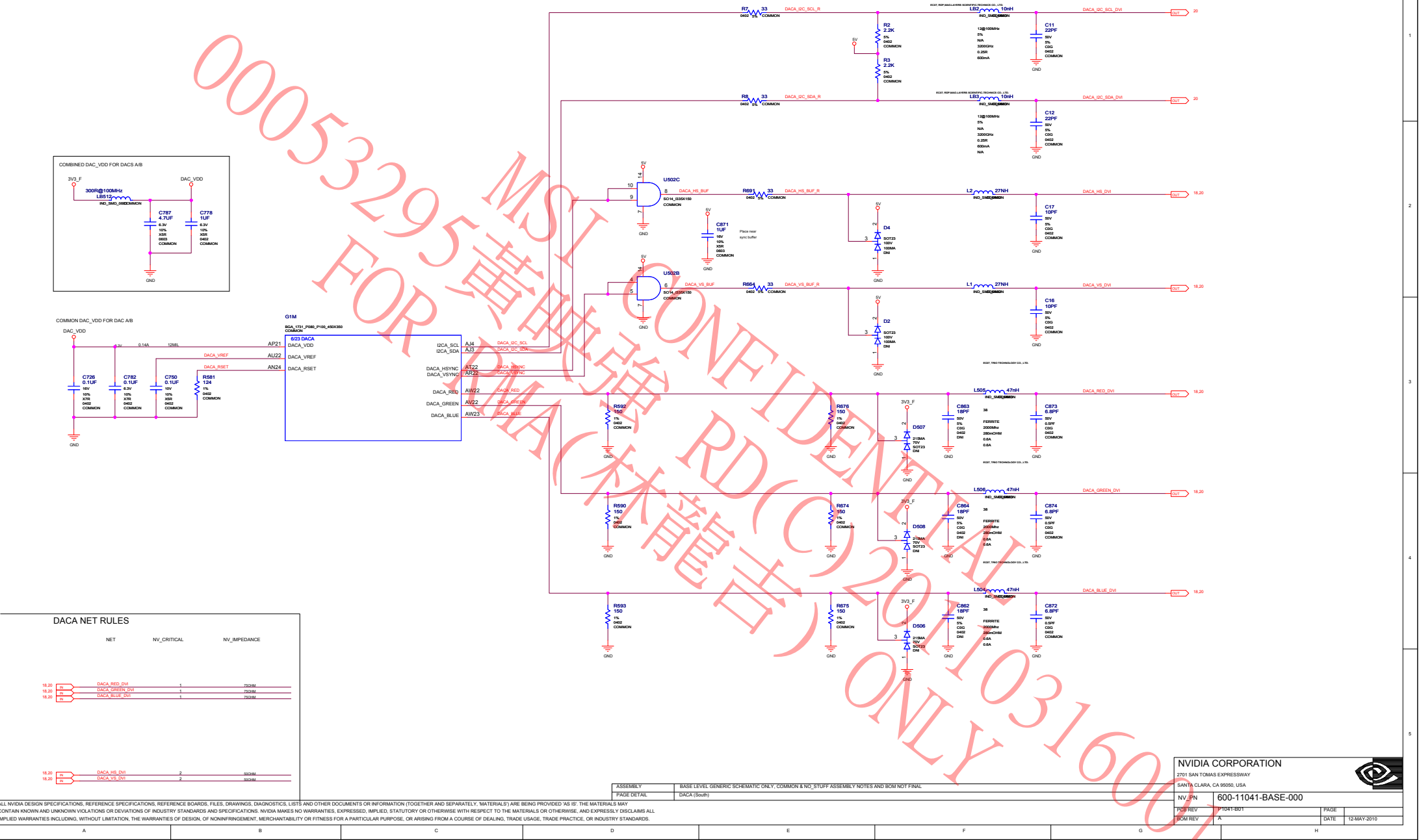
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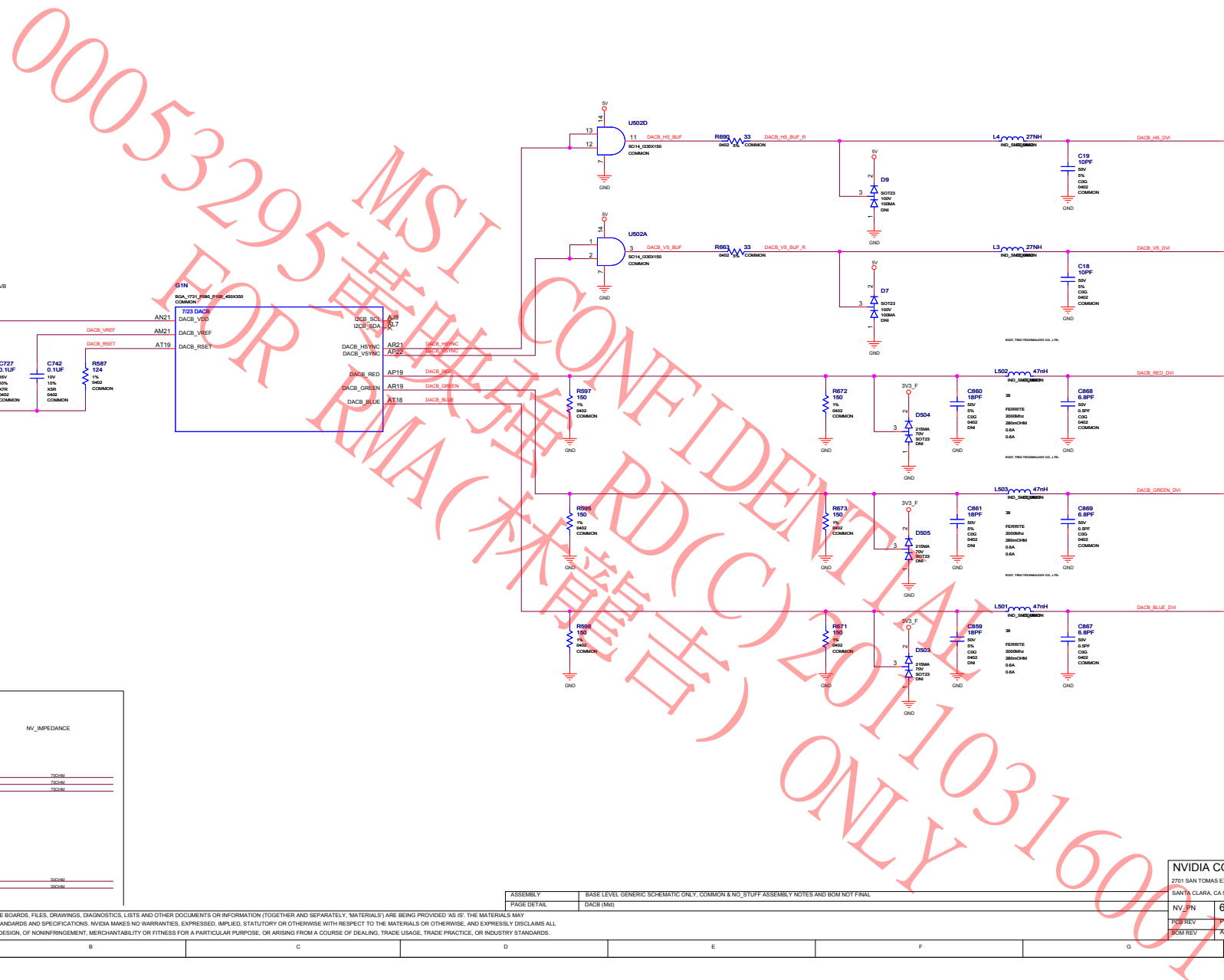


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100	1	1

19.21	IN	DACB_HS_DVI	2	5001BM
19.21	IN	DACB_VS_DVI	2	5001BM

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PAGE DETAIL	DACB (Mid)

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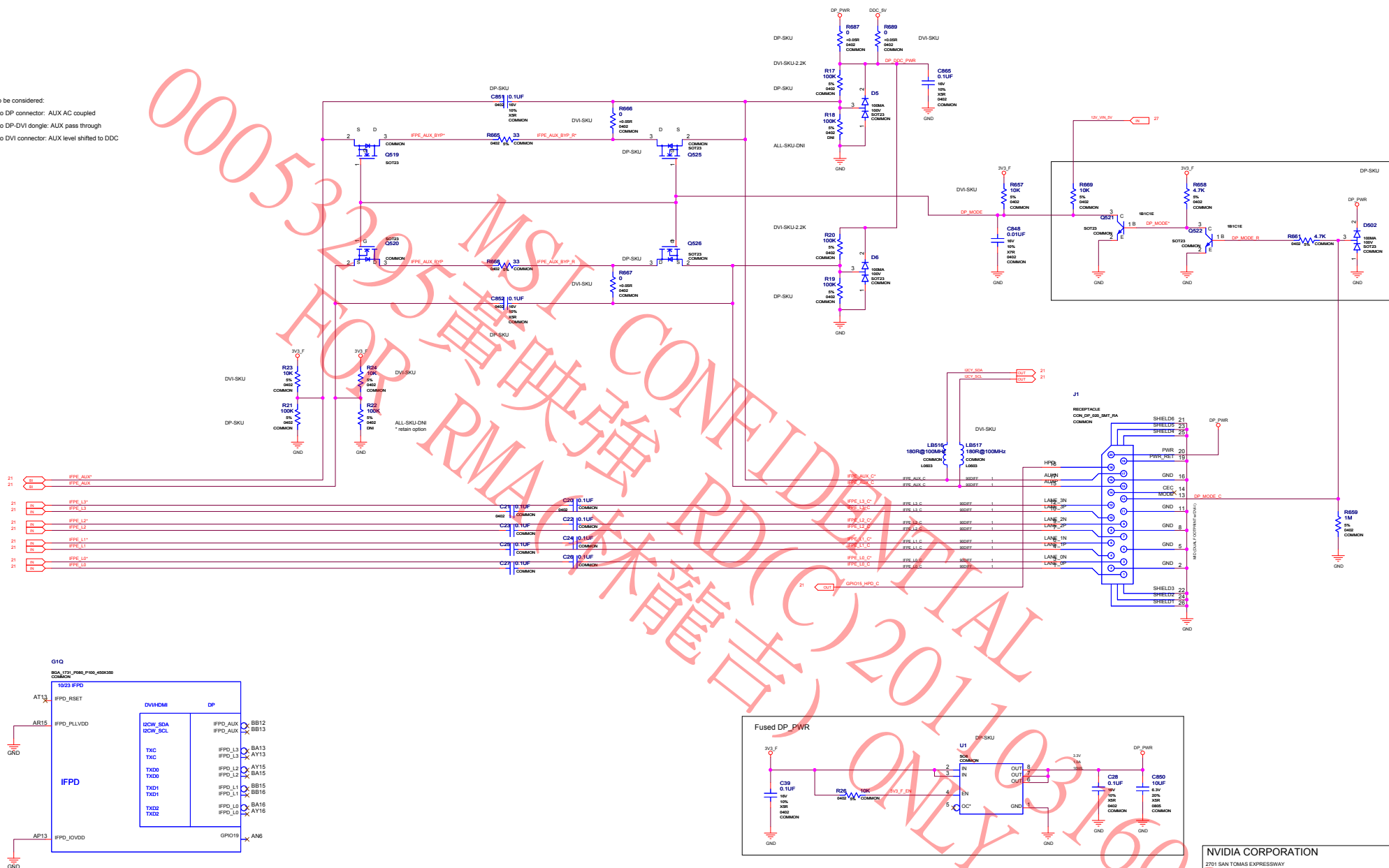
NV_PN	600-11041-BASE-000
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PCB REV	P1041-B01
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BOM REV	1
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	PAGE	
	DATE	12-MAY-2010

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through
3. DP AUX to DVI connector: AUX level shifted to DDC



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PAGE DETAIL	IFPEF DP (Mid)

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PCB REV	P1041-B01	PAGE	
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DATE	12-MAY-2010

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DATE	12-MAY-2010

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DATE	12-MAY-2010

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Page26: Misc: ROM, HDCP, XTAL, Straps

STRAP0	USER_BIT [3..0]	0000 => 5K PD	
STRAP1	3GIO_PADCFG_LUT_ADR	0000 => 5K PD	0000 Desktop
STRAP2	PCI_DEVID [3..0]	0010 For 0x0E22 => 15K PD 0100 For 0x0E24 => 25K PD	
ROM_SI	RAMCFG[0]	32Mx32 256-bit Samsung for SKU 0 1st memory 0011 PD 20K 32Mx32 256-bit Hynix for SKU 10 2nd memory 0010 PD 10K	
	RAMCFG[1]		
	RAMCFG[2]	32Mx32 192-bit Samsung for SKU 0 1st memory 1011 PD 20K 32Mx32 192-bit Hynix for SKU 0 2nd memory 1010 PD 10K	
	RAMCFG[3]		
ROM_SO	VGA_DEVICE	1	
	SMB_ALT_ADDR	0	10k PD
	FB[0]_BAR_SIZE	0	
ROM_SCLK	XCLK_417	0	
	PEX_PLL_EN_TERM100	1 ENABLED	
	SLOT_CLK_CFG	1 ENABLE	
	SUB_VENDOR	1 Dedicated BIOS	45K PD
	PCI_DEVID_EXT	0 0xC	

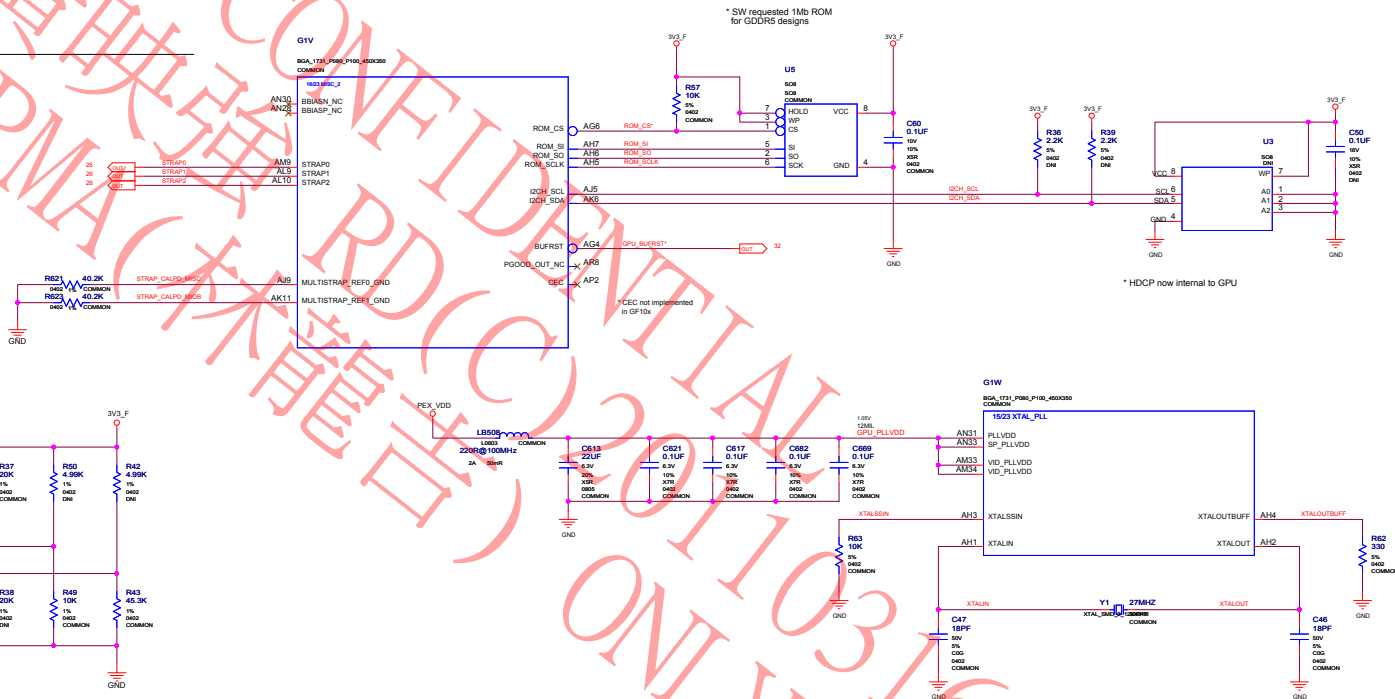
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3..0] Config Width	Vendor
0000	Reserved
0001	32Mx32 256-bit Qimonda
0010	32Mx32 256-bit Hynix
0011	32Mx32 256-bit Samsung
0100	Reserved
0101	64Mx32 256-bit Qimonda
0110	64Mx32 256-bit Hynix
0111	64Mx32 256-bit Samsung
1000	Reserved
1001	32Mx32 192-bit Qimonda
1010	32Mx32 192-bit Hynix
1011	32Mx32 192-bit Samsung
1100	Reserved
1101	64Mx32 192-bit Qimonda
1110	64Mx32 192-bit Hynix
1111	64Mx32 192-bit Samsung

MISC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE
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	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	45.2k 1% TO GND	NC
BINARY BRINGUP	NC	NC
MULTI-LEVEL	45.2k 1% TO GND	45.2k 1% TO GND



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PAGE DETAIL	Misc ROM, HDCP, XTAL, Straps

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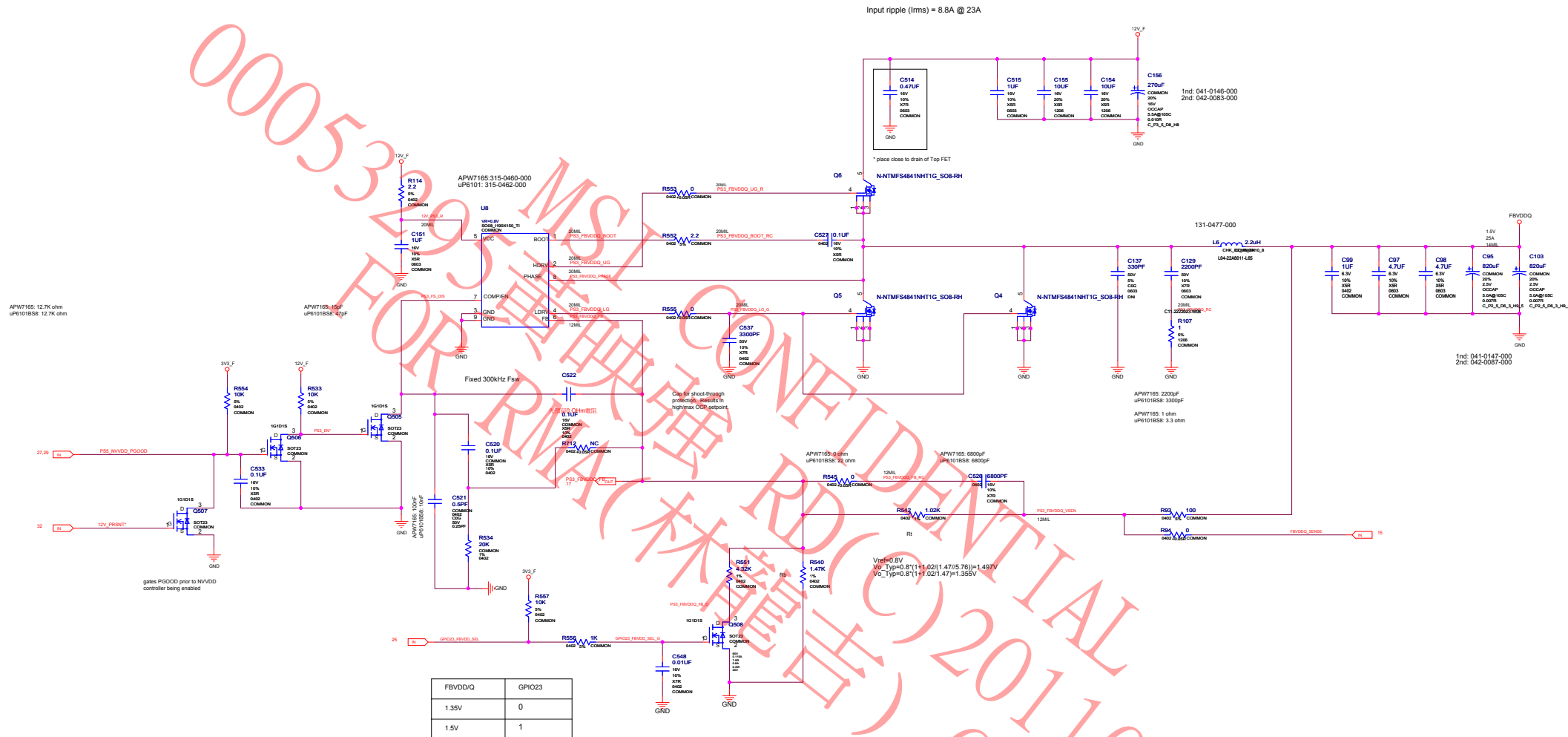
PCB REV P1041-B01

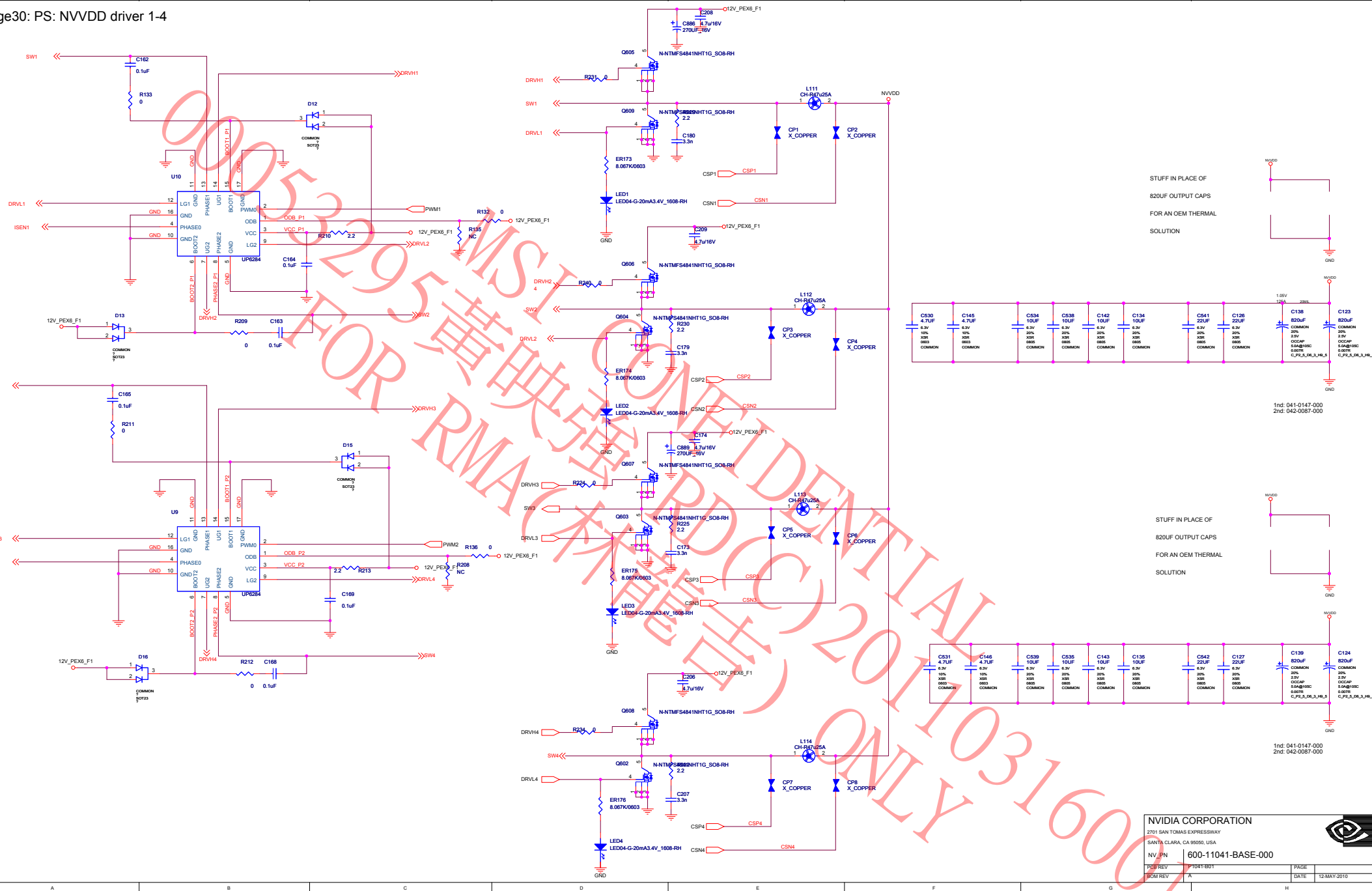
ROM REV A

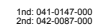
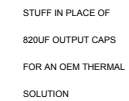
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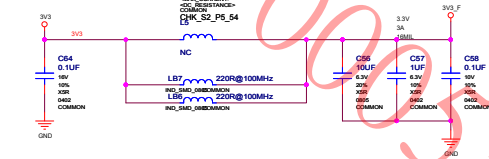
NV_PN	600-11041-BASE-000
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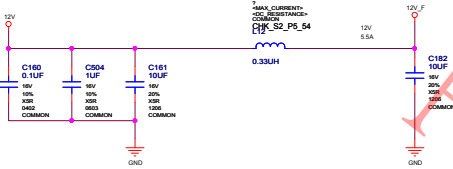
DATE	12-MAY-2010
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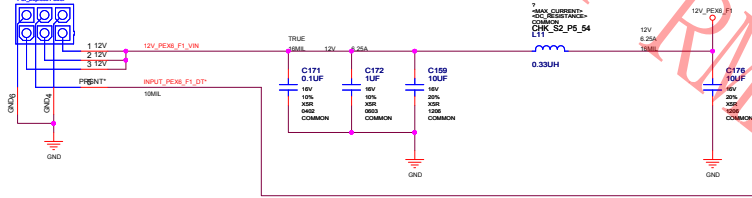
PEX 3V3 INPUT - 10W



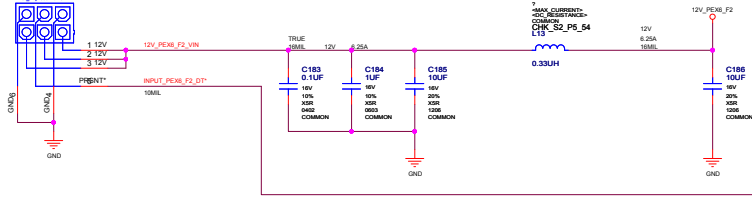
PEX_12V INPUT - 66W



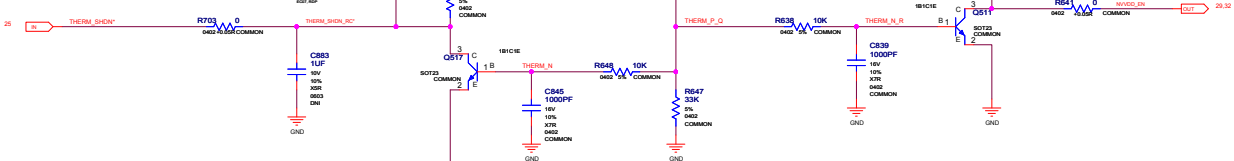
PEX6 INPUT 1 - 2x3 PCIE CON 75W
MUST BE ATTACHED AND POWERED TO START BOARD



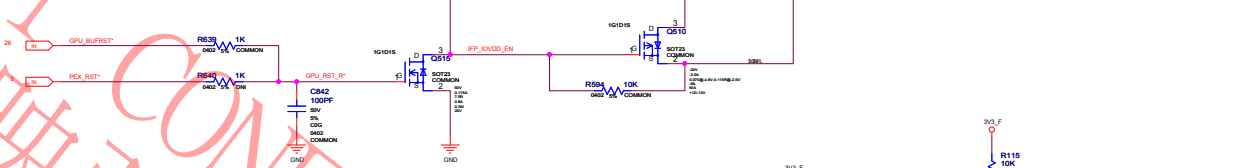
PEX6 INPUT 1 - 2x3 PCIE CON 75W
MUST BE ATTACHED AND POWERED TO START BOARD



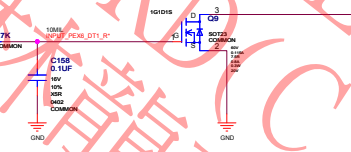
THERM OVERT SHUTDOWN LATCH



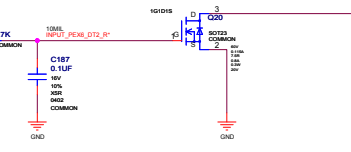
IFP_IOVDD (backdrive prevention)



PEX Input Present 1



PEX Input Present 1



Brackets:

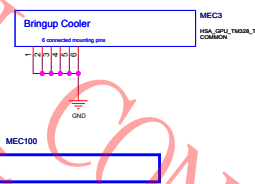
Bracket with DVI_DP_mHDMI: 151-10001-0355-071



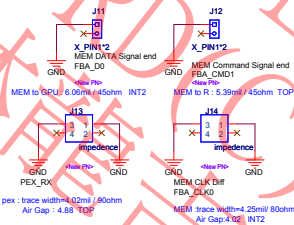
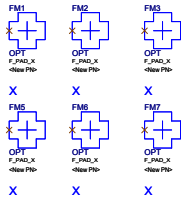
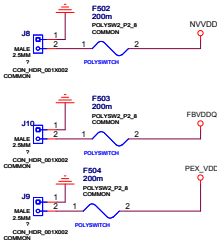
Bracket Screw



Cooler/GPU Stiffener



remove mec1



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PAGE DETAIL	Mechanical: Bracket/Thermal Solution

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NV_P/N	600-11041-BASE-000	PAGE	
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PAGE DETAIL	Blank

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