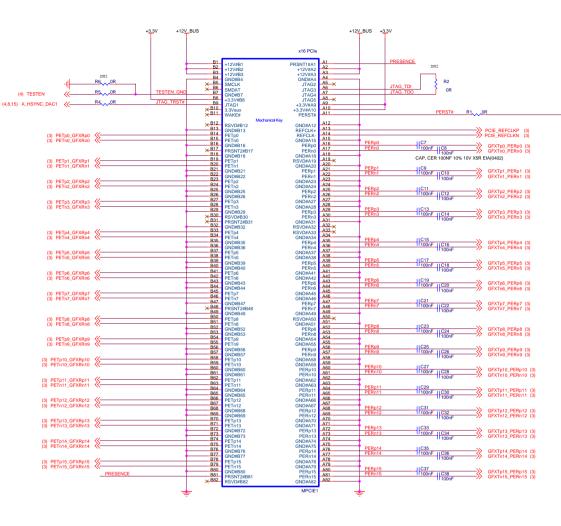


## PCI-EXPRESS EDGE CONNECTOR



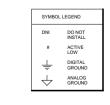
Power Sequence Circuit to ensure SMPS\_EN is released after +12V\_BUS and +3.3V\_BUS are both in regulation. Pull-up may or may not be required on SMPS\_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS\_EN will be helt low Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS\_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)
Typical trigger when +3.3V ramps above 2.2V (650mV)

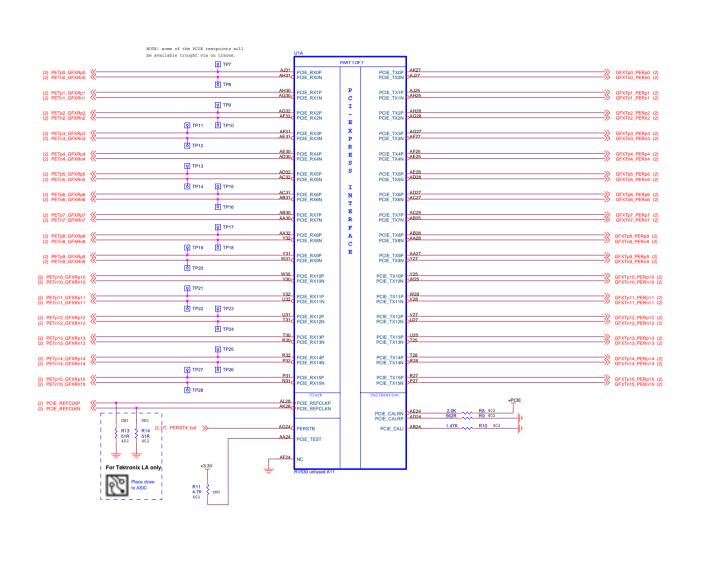
Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS\_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)
Typical trigger when +12V ramps above 10V (1.1V)

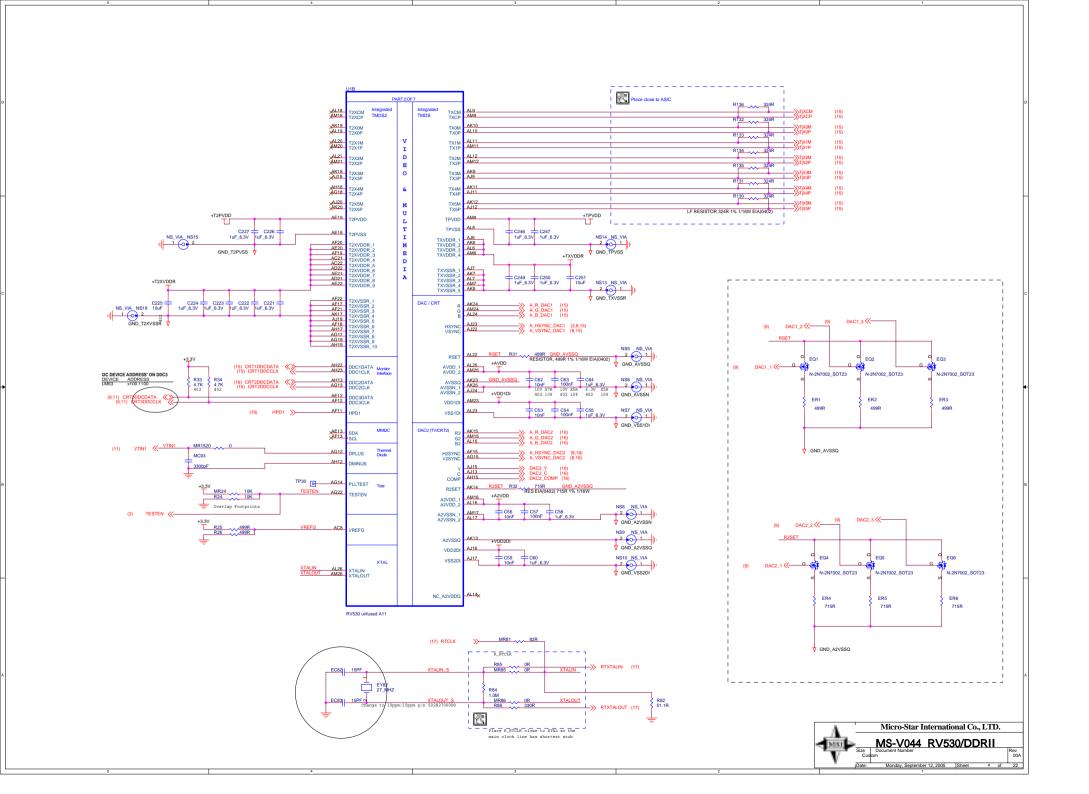


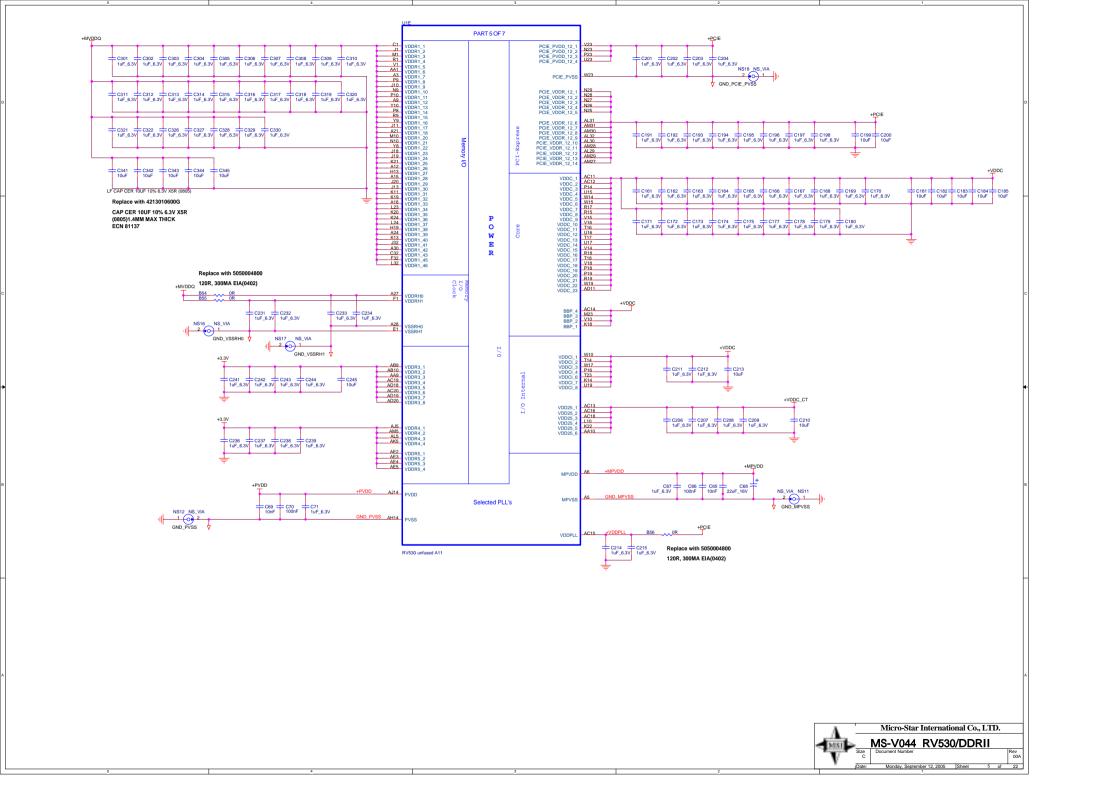
CAP CERAMIC 100NE 10% 10V X5R EIA(0402)



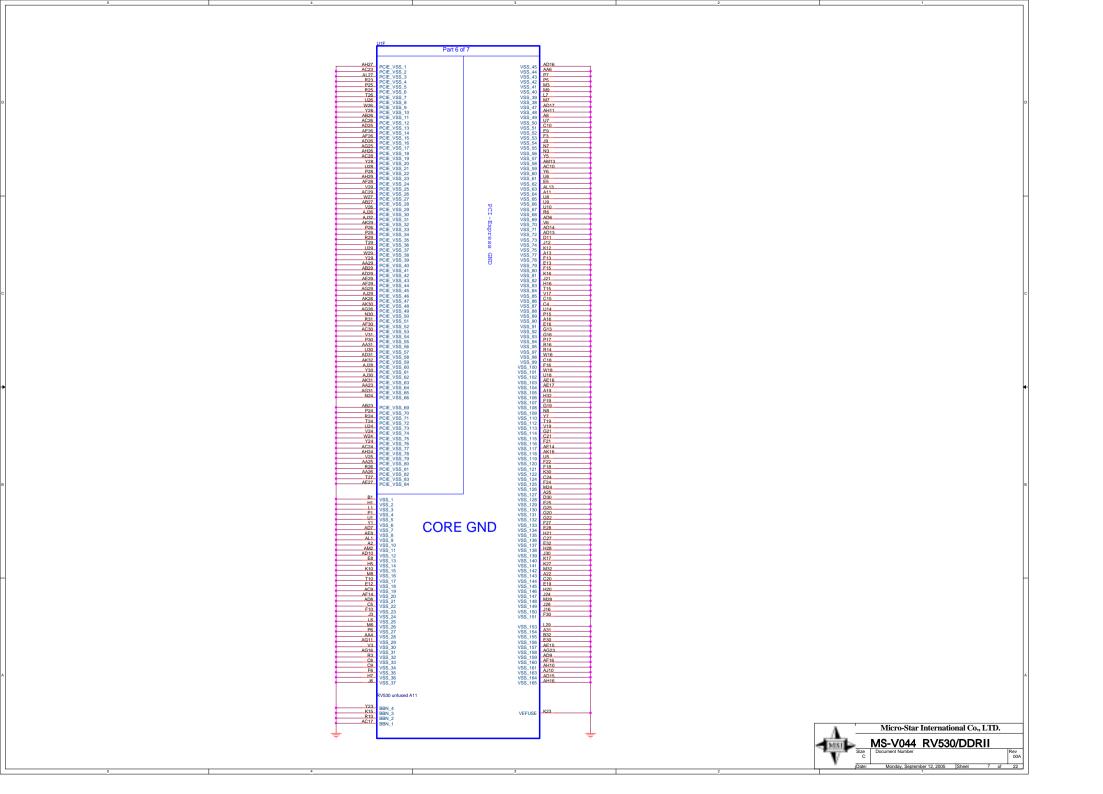


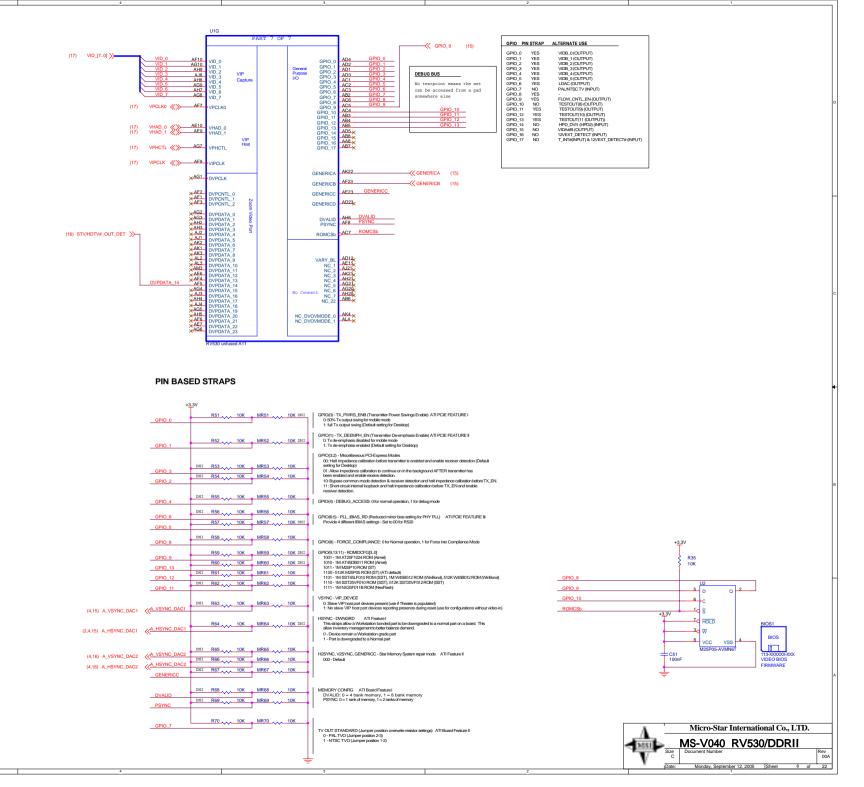
| Micro-Star International Co., LTD. | MS-V044 RV530/DDRII | Scc | Document Number | COA | Document Number | COA | Date: Monday, September 12, 2005 | Sheet | 3 of | 22

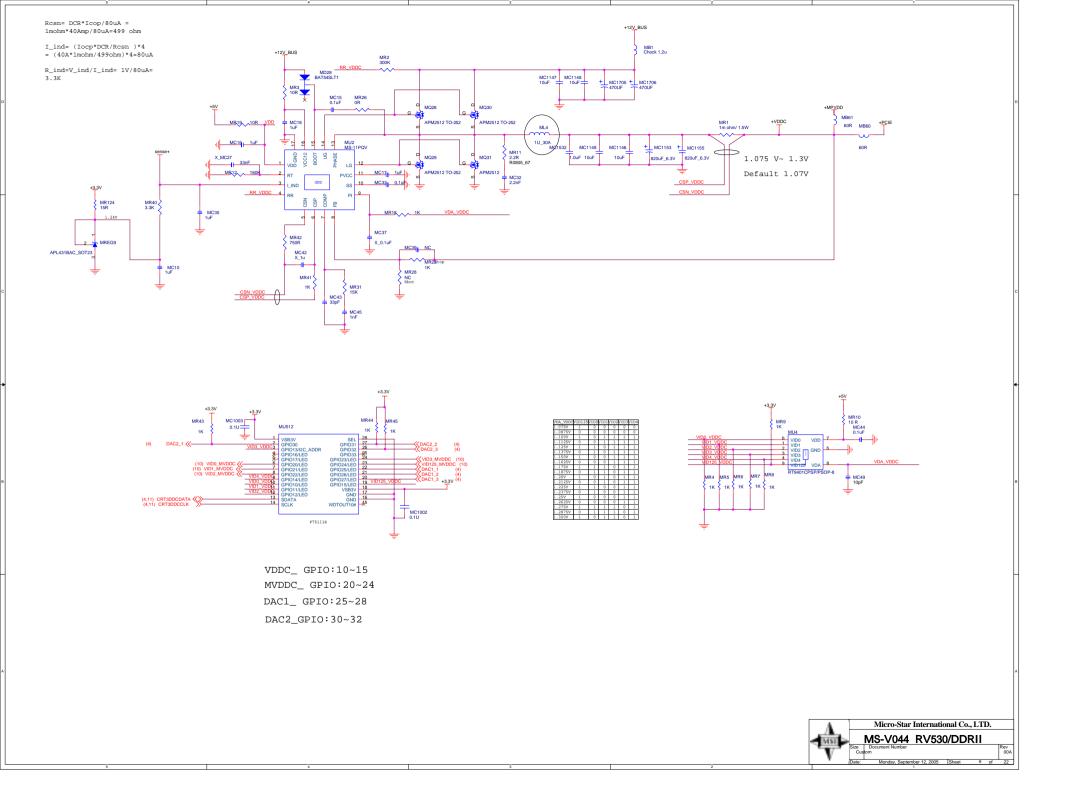


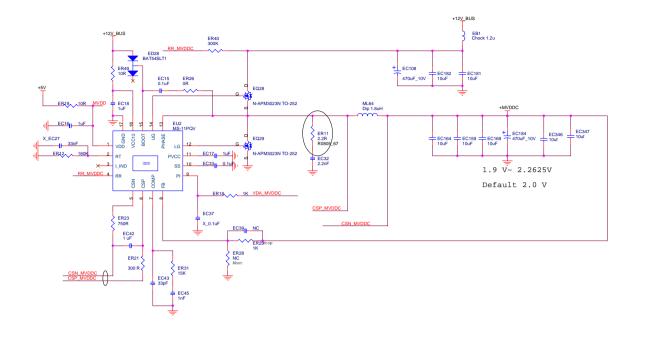


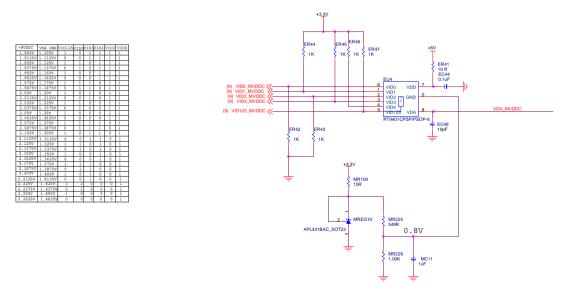
## RV530 MEMORY CHANNELS A and B Channel B Channel A (14) M\_MDB[63..0] «>> M\_MAB[12..0] (14) Part 4 of 7 (13) M\_MDA[63..0] «> →>> M\_MAA[12..0] (13) Part 3 of 7 MAA\_0 MAA\_1 MAA\_2 MAA\_3 MAA\_6 MAA\_6 MAA\_7 MAA\_1 MAA\_1 MAA\_1; MAA\_1; MAA\_1; MAA\_1; MEMORY INTERFACE A MEMORY INTERFACE B M\_MAA[15..14] (13) >>> M\_DQMA#[7..0] (13) DQMBb DQMBb DQMBb DQMBb DQMBb DQMBb DQMBb DQMBb DQMAb\_C DQMAb\_C DQMAb\_C DQMAb\_C DQMAb\_C DQMAb\_C DQMAb\_C ✓ M\_QSB[7..0] (14) ✓ M\_QSA[7..0] (13) QSB QSB QSB QSB QSB QSB QSB QSB QSA\_G QSA\_G QSA\_G QSA\_G QSA\_G QSA\_G QSB\_0B QSB\_1B QSB\_2B QSB\_3B QSB\_4B QSB\_5B QSB\_6B QSB\_7B QSA\_0B QSA\_1B QSA\_2B QSA\_3B QSA\_4B QSA\_5B QSA\_6B QSA\_7B ODTB0 ODTA0 ODTA0 ODTA0 For DDR2 C2 >>> CKEB0 CKEB0 CKEA0 B30 CKEA0 RASB0b RASA0b DB28 >>> RASA#0 (13) CASB0b DD3 CASB#0 CASA0b OC29 >>> CASA#0 (13) +MVDDQ WEB0b DB2 >> WEB#0 +MVDDQ (14) WEA0b DB31 >>> WEA#0 (13) CLKA1 CLKA1 (13) CLKA1b CLKA#1 (13) C351 = C352 100nF 10nF CKEB1 13 CKEB1 R162 100R 1% (14) CKEA1 C22 >>> CKEA1 (13) C355 C356 100nF 10nF RASB1b OJ2 >>> RASB#1 (14) DRAM RST RASA1b 0B24 >>> RASA#1 (13) CASB1b OL2 >>> CASB#1 (14) TEST MOLK CASA1b 0B22 >>> CASA#1 (13) WEB1b 0M2\_>> WEB#1 TEST\_YCLK WEA1b 0B21 >>> WEA#1 (13) DK2 X3 CSB#1\_0 (14) MEMTEST R172 R171 R170 4.7K 4.7K 4.7K R169 > 243R LF RES EIA(0402) 243R 1% 1/16W RESISTOR, 4.7K 5% 1/16W EIA(0402) Micro-Star International Co., LTD. MS-V044 RV530/DDRII Monday, September 12, 2005 Sheet 6 of 22



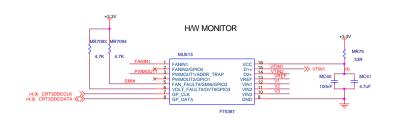


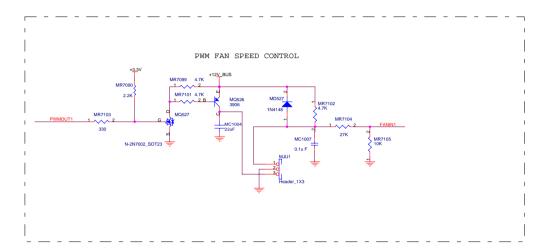


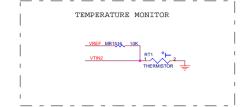


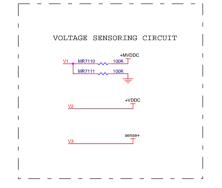




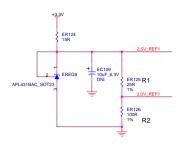


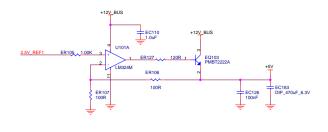


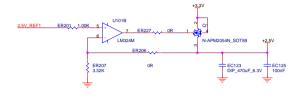


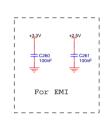






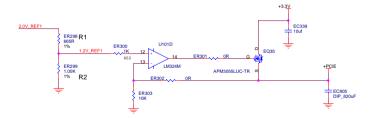










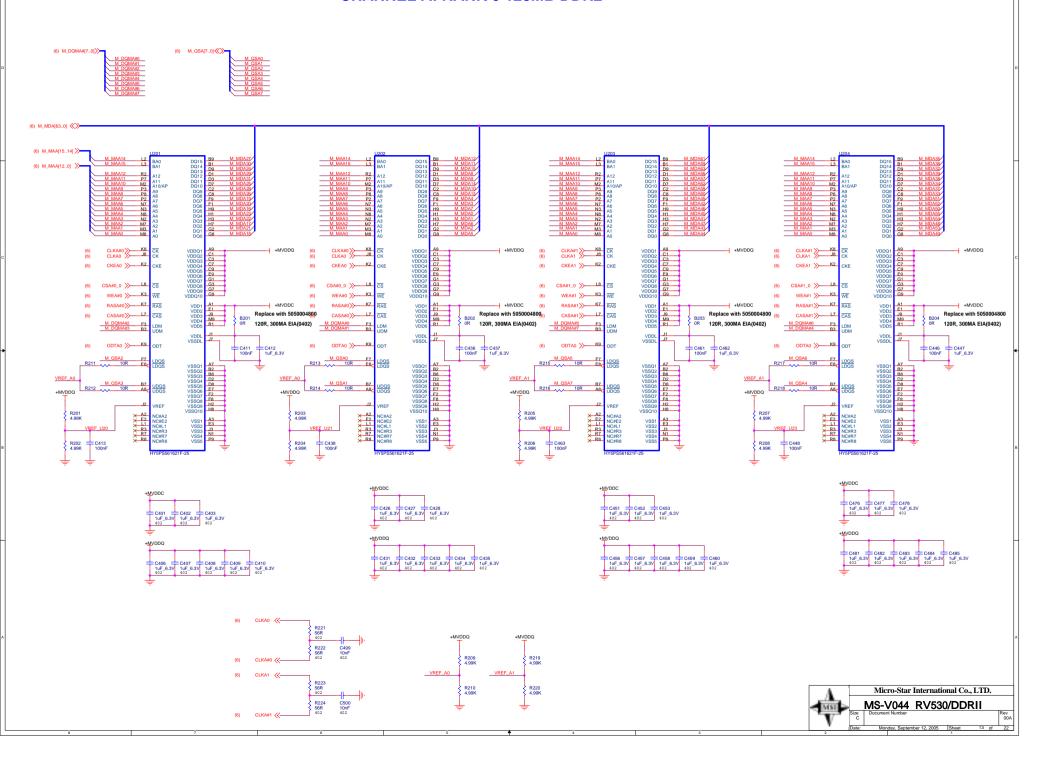


+2.5V +AVDD +AZVDD +VDD1DI +VDD2DI +PVDD +TPVDD +TXVDDR +TZPVDD +TZXVDDR +VDDC\_CT +VDDC\_CT + RAVDD +RAVDD +

Replace with 5050004800 120R, 300MA EIA(0402)

<u> </u>	Micro-Star International Co., LTD.		
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## **CHANNEL A: RANK 0 128MB DDR2**



## **CHANNEL B: RANK 0 128MB DDR2**

