The following grounds should be routed back to their respective regulators and then tied directly to the ground plane with one via: GND_PVSS, GND_MPVSS, GND_TPVSS, and GND_A2VSSN. The other ground pins (GND_AVSSN, GND_A2VSSQ, GND_RSET, GND_R2SET) should be tied to the ground plane directly through one via as close to the pins as possible without connecting to anything else. If space is an issue it is possible to use one via for two adjacent pins.

GND_R2SET GND_RSET

+VDDQ_BUS

Use 47uF Tant. 16V 20% D size (P/N 4230047600), 800mR Max. ESR and Max. ripple 430mA @ 100kHz
or
100uF, Alum. 6.3V 20% 6.3mm dia (P/N 4261010700), 440mR Max. ESR and Max. ripple 230mA @ 100kHz
or
47uF, Alum. 6.3V 20% 5mm dia (P/N 4262047600), 760mR Max. ESR and Max. ripple 150mA @ 100kHz

C2 100uF_6.3V
Biggest footprint

+5V_BUS +3.3V_BUS

C5 47uF_6.3V >=6.3V DNI
C8 47uF_6.3V >=6.3V

+12V_BUS

C10 place at the AGP connector
C10 10uF_20V
DNI

MAGP1

	A1	12V	OVRCNT#	B1	
AGP_TYPEDET#	A2	TYPEDET#	5.0V	B2	
AGP_GC_8X_DET#	A3	GC_DET#/RESERVED	5.0V#B3	B3	
	A4	USB-	USB+	B4	
	A5	GND	GND#B5	B5	
	A6	INTA#	INTB#	B6	
	A7	RST#	CLK	B7	
	A8	GNT#	REQ#	B8	
	A9	VCC3.3	VCC3.3#B9	B9	
AGP_ST1	A10	ST1	ST0	B10	AGP_ST0
	A11	MB_DET#/RESERVED	ST2	B11	AGP_ST2
	A12	DBI_HI/PIPE#	RBF#	B12	
	A13	GND#A13	GND#B13	B13	
AGP_SBA1	A14	WBF#	DBI_LO/RESERVED	B14	
	A15	SBA1	SBA0	B15	AGP_SBA0
AGP_SBA3	A16	VCC3.3#A16	VCC3.3#B16	B16	
	A17	SBA3	SBA2	B17	AGP_SBA2
	A18	SB_STB#	SB_STB	B18	
	A19	GND#A19	GND#B19	B19	
AGP_SBA5	A20	SBA5	SBA4	B20	AGP_SBA4
AGP_SBA7	A21	SBA7	SBA6	B21	AGP_SBA6
	A22	KEY	KEY#B22	B22	
	A23	KEY#A23	KEY#B23	B23	
	A24	KEY#A24	KEY#B24	B24	
	A25	KEY#A25	KEY#B25	B25	
AGP_AD30	A26	AD30	AD31	B26	AGP_AD31
AGP_AD28	A27	AD28	AD29	B27	AGP_AD29
	A28	VCC3.3#A28	VCC3.3#B28	B28	
AGP_AD26	A29	AD26	AD27	B29	AGP_AD27
AGP_AD24	A30	AD24	AD25	B30	AGP_AD25
	A31	GND#A31	GND#B31	B31	
AGP_C/BE#3	A32	AD_STB1#	AD_STB1	B32	
	A33	C/BE3#	AD23	B33	AGP_AD23
	A34	VDDQ	VDDQ#B34	B34	
AGP_AD22	A35	AD22	AD21	B35	AGP_AD21
AGP_AD20	A36	AD20	AD19	B36	AGP_AD19
	A37	GND#A37	GND#B37	B37	
AGP_AD18	A38	AD18	AD17	B38	AGP_AD17
AGP_AD16	A39	AD16	C/BE2#	B39	AGP_C/BE#2
	A40	VDDQ#A40	VDDQ#B40	B40	
	A41	FRAME#	IRDY#	B41	
	A42	KEY#A42	KEY#B42	B42	
	A43	KEY#A43	KEY#B43	B43	
	A44	KEY#A44	KEY#B44	B44	
	A45	KEY#A45	KEY#B45	B45	
	A46	TRDY#	DEVSEL#	B46	
	A47	STOP#	VDDQ#B47	B47	
	A48	PME#	PERR#	B48	
	A49	GND#A49	GND#B49	B49	
	A50	PAR	SERR#	B50	
AGP_AD15	A51	AD15	C/BE1#	B51	AGP_C/BE#1
	A52	VDDQ#A52	VDDQ#B52	B52	
AGP_AD13	A53	AD13	AD14	B53	AGP_AD14
AGP_AD11	A54	AD11	AD12	B54	AGP_AD12
	A55	GND#A55	GND#B55	B55	
AGP_AD9	A56	AD9	AD10	B56	AGP_AD10
AGP_C/BE#0	A57	C/BE0#	AD8	B57	AGP_AD8
	A58	VDDQ#A58	VDDQ#B58	B58	
AGP_AD6	A59	AD_STB0#	AD_STB0	B59	
	A60	AD6	AD7	B60	AGP_AD7
	A61	GND#A61	GND#B61	B61	
AGP_AD4	A62	AD4	AD5	B62	AGP_AD5
AGP_AD2	A63	AD2	AD3	B63	AGP_AD3
	A64	VDDQ#A64	VDDQ#B64	B64	
AGP_AD0	A65	AD0	AD1	B65	AGP_AD1
	A66	VREFGC	VREFCG	B66	AGP_AGPREF

UNIVERSAL_AGP_BUS

AGP_SBA[7..0]
AGP_ST[2..0]
AGP_C/BE#[3..0]
AGP_AD[31..0]

2 AGP_INTR#
2 AGP_GNT#
2 AGP_WBF#
2 AGP_SB_STB#
2 AGP_MB_8X_DET#
2 AGP_DBI_HI

R83 0R

+5V_BUS
C11 100nF X7R

R3 100R
2 AGP_RESET# AGP_RESET#
R4 180R
U6A SN74ACT86D
COMMON

2 AGP_AD_STB1#
2 AGP_FRAME#
2 AGP_TRDY#
2 AGP_STOP#
2 AGP_PAR
2 AGP_AD_STB0#

AGP_AGP/PCICLK 2
AGP_REQ# 2
AGP_RBF# 2
AGP_DBI_LO 2
R86 0R
AGP_SB_STB 2
AGP_AD_STB1 2
AGP_IRDY# 2
AGP_DEVSEL# 2
AGP_AD_STB0 2

AGP_TYPEDET#
R19 0R
For retail, 1K ohm pull-down causes AMD system detects AGP2X only
+12V_TYPEDET# short protection for OEM (1KR)

AGP_GC_8X_DET#
R81 0R

AGP_VREFGC

+3.3V_BUS
R90 47K
U6D SN74ACT86D
AGP_MB_8X_DET#
R91 1K
TEST

+VDDQ_BUS
2N7002E Q10
R92 147R

R_AGP8X must be 1% resistor to provide 350mV +/- 5% on Vref

R_AGP8X
R93 332R
R94 100R
C19 10nF

UNIVERSAL VREFGC CIRCUIT (2X, 4X, 8X)

+VDDQ_BUS
R88 137R 1%
Q9 2N7002E
R89 75.0R 1%
TEST
AGP_AGPTEST
AGP_AGPTEST 2

AGP_AGPREF R84 0R Keep stubs short
AGP_VREFGC R85 0R

R_AGP8X must be 1% resistor to provide 350mV +/- 5% on Vref

+VDDQ_BUS
2N7002E Q11
TEST
R_AGP8X
R96 332R
R95 147R
R97 100R
C21 10nF
AGP_AGPREFCG 2

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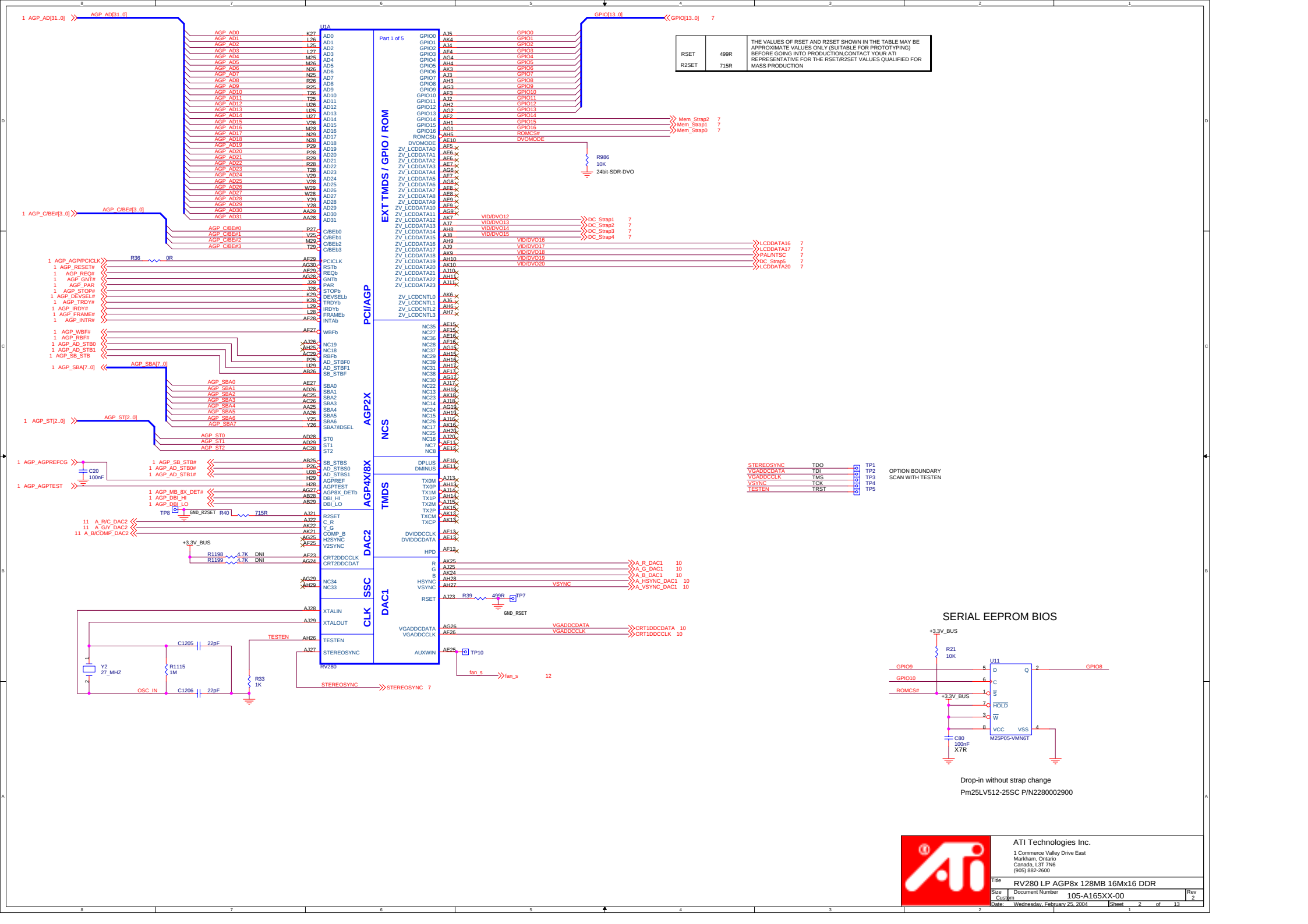
Title	RV280 LP AGP8x 128MB 16Mx16 DDR		
Size: Custom	Document Number: 105-A165XX-00		Rev: 2
Date: Wednesday, February 25, 2004	Sheet 1 of 13		


U1A
Part 1 of 5
EXT TMDS / GPIO / ROM
PCI/AGP
AGP2X
NCS
AGP4X/8X
TMDS
DAC2
SSC
CLK
DAC1
RSET R2SET THE VALUES OF RSET AND R2SET SHOWN IN THE TABLE MAY BE APPROXIMATE VALUES ONLY (SUITABLE FOR PROTOTYPING) BEFORE GOING INTO PRODUCTION,CONTACT YOUR ATI REPRESENTATIVE FOR THE RSET/R2SET VALUES QUALIFIED FOR MASS PRODUCTION
499R 715R
R986 10K 24bit-SDR-DVO
OPTION BOUNDARY SCAN WITH TESTEN
SERIAL EEPROM BIOS
Drop-in without strap change
Pm25LV512-25SC P/N2280002900
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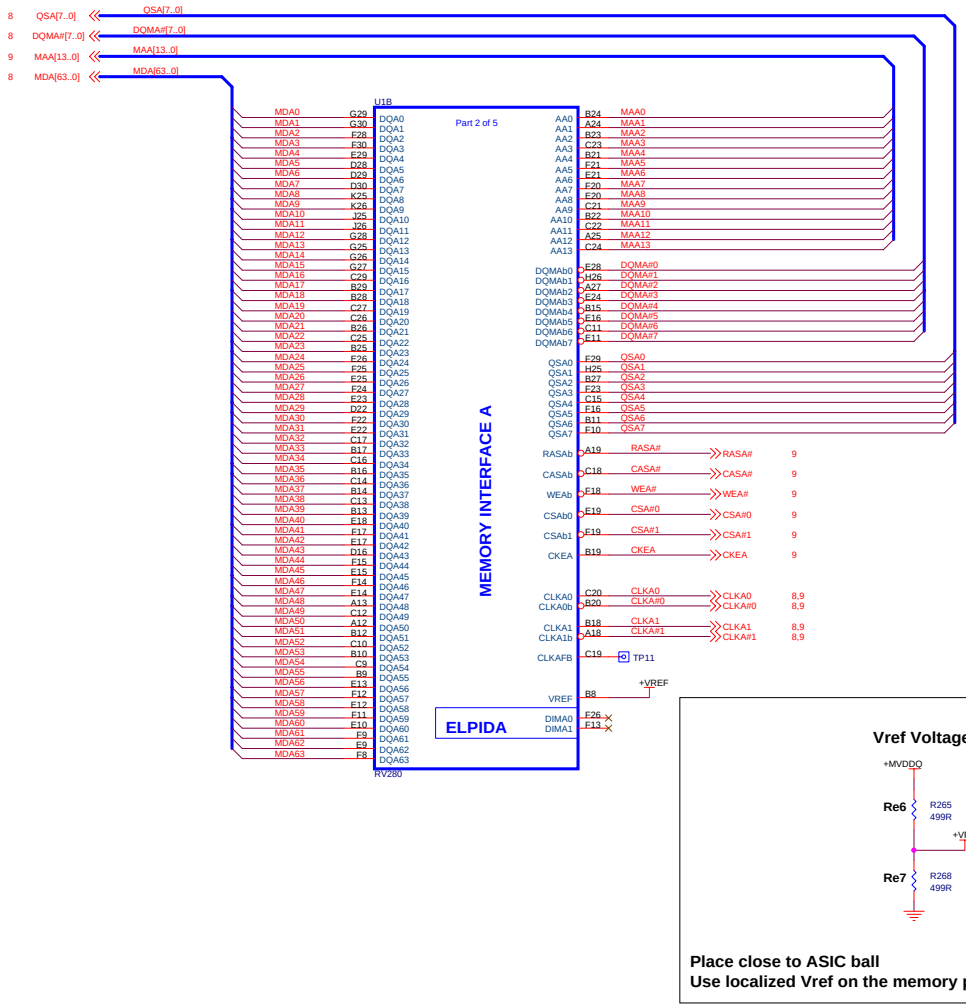
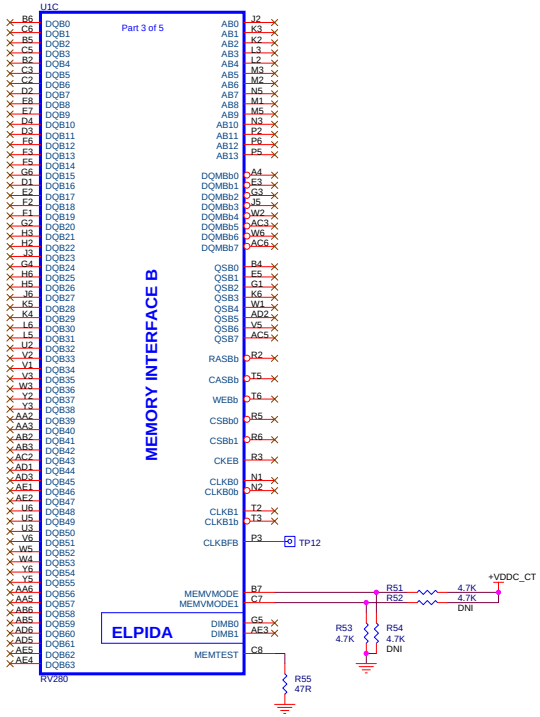
MEMORY CHANNEL A



Vref Voltage

Place close to ASIC ball
Use localized Vref on the memory page

MEMORY CHANNEL B



MEMVMODE[1:0]	MEMORY IO VOLTAGE	
0 1	2.5V (DDR)	Default
1 0	1.8V (DDR)	
1 1	3.3V (SDR)	

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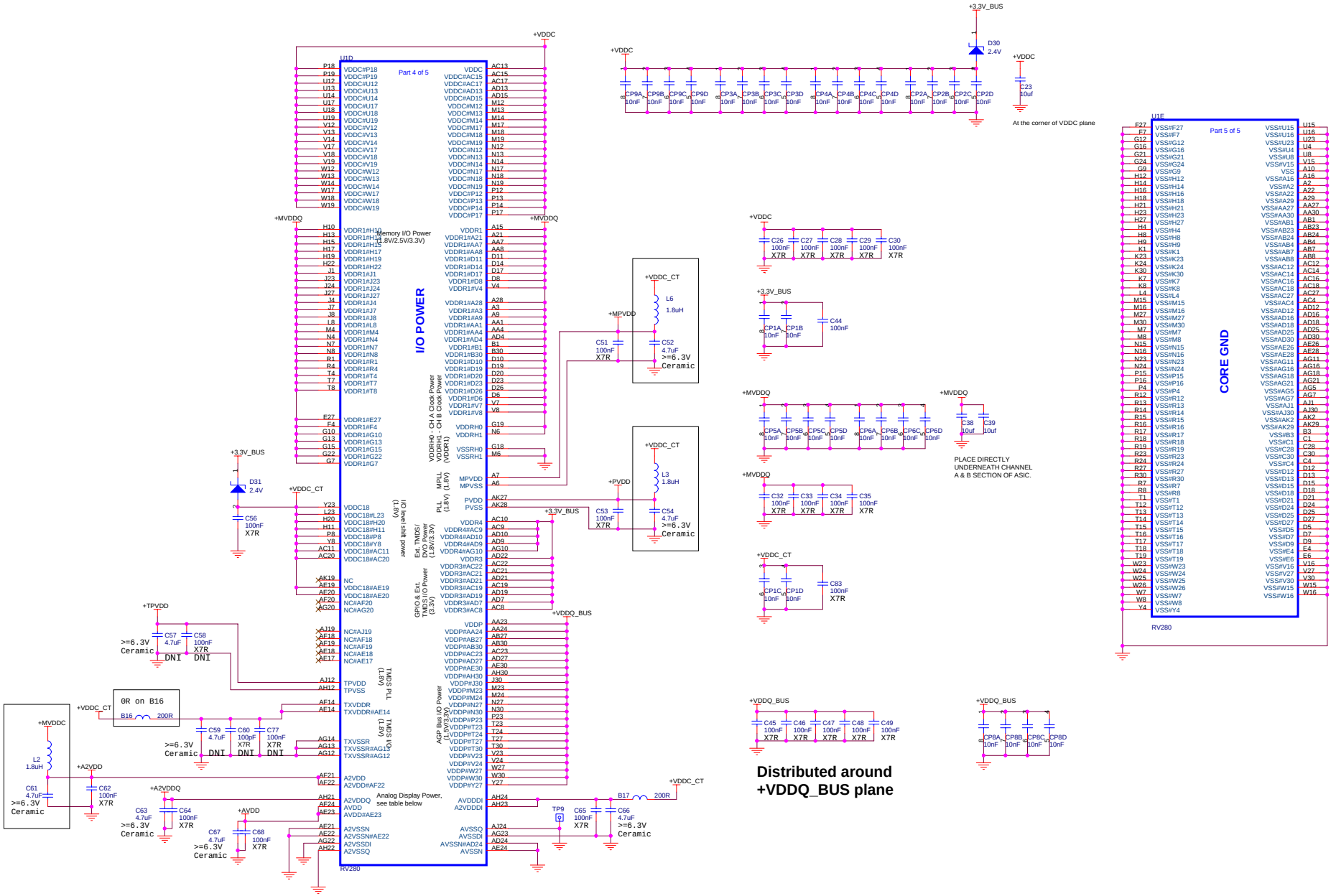

Pin Names	+AVDD	Matching Ground	+A2VDD	Matching Ground	+A2VDDQ	Matching Ground	+AVDDDI +A2VDDDI	Matching Ground
Voltage	1.8V		2.5V		1.8V		1.8V	
Usage	DAC1 VDD (80mA)	AVSSN (Noisy)	DAC2 VDD (120mA)	A2VSSN (Noisy)	DAC2 Band Gap Ref.	A2VSSQ (Quiet)	Digital Power for DAC1 and DAC2	AVSSDI A2VSSDI (Digital)
	DAC1 Band Gap Ref.	AVSSQ (Quiet)						
Board power and ground option(s)	AVDD sourced from VDDC_CT thru bead at least 15 mil trace and not longer than 1.5 inch. AVSSN and AVSSQ with single via to GND close to the pin.		(1) A2VDD regulated source and A2VSSN return path routed with at least 15 mil trace and not longer than 1.5 inch. AVSSN with single via to GND at the regulator. (2) Sourced from VDD thru bead instead of the regulator		Source from AVDD thru bead. A2VSSQ with sigle via to GND close to the pin.		Source from VDDC_CT thru bead	

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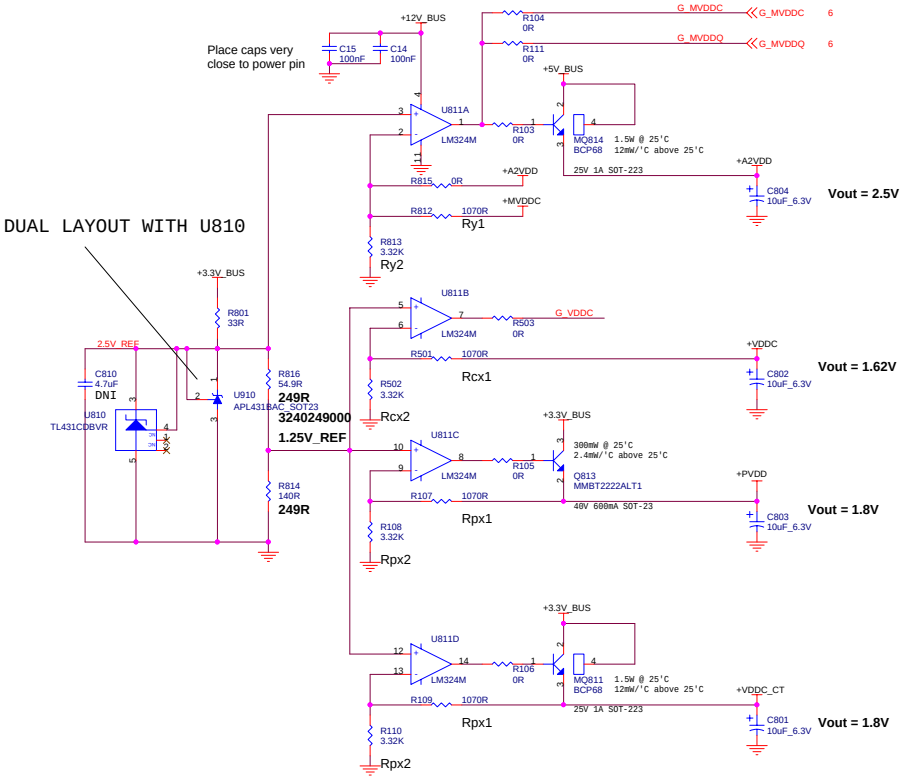


Regulator for VDDC_CT (Core Transform) and AVDD/A2VDDQ/AVDDDI/A2VDDDI TXVDDR, LVDDRx, MPVDD

Vin = 3.3V AGP
Vout = 1.8V
Iout = 350mA + 100mA + 50mA = 500mA MAX
Iout = 600mA MAX (with PVDD/TPVDD)

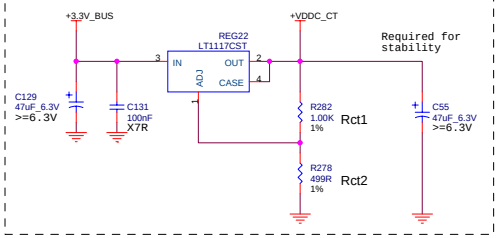
Regulator for PVDD (Core PLLs) and optional TPVDD (TMDS PLLs)

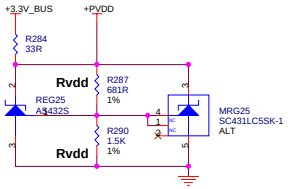
Vin = 3.3V AGP
Vout = +1.8V
Iout = 25mA MAX (PVDD only)
Iout = 30mA MAX (PVDD + TPVDD)

The value of resistor were chosen to reduce failure rate caused by possible defective regulators, i.e., 33R are used instead of 47R or 51R for more start up current. (3.465V - 1.8V) / 33R = 50.5mA

805 package resistor are required for sufficient power rating (0.1W rating). (3.465V - 1.8V) * 50.5mA = 0.085W; therefore, smaller resistor value would require 1206 package

	Rct1	Rct2
1.8V	1K 3240100100 603	422R 3240422000 603
1.9V		499R 3240499000 603

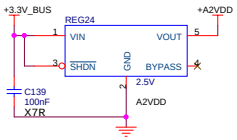




Regulator For A2VDD (2nd DACs)

Vin = +3.3V AGP
Vout = 2.5V
Iout = 150mA MAX

A2VDD might not be needed if VDD can provide stable 2.5V



TC1185

A2VDD and A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch. A2VSSN with signle via to GND at the regulator

	Range	Rpx1	Rpx2
1.8V	1.805V ~ 1.827V	1K 3240100100	2.21K 3240221100

Buffered Shount Regulator for VDDC

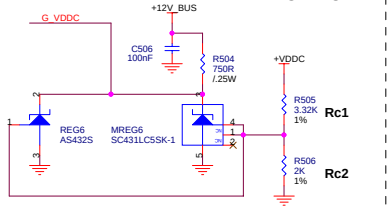
Vin = 3.3V
Vout = 1.62V or Adjustable
Iout = 3A MAX

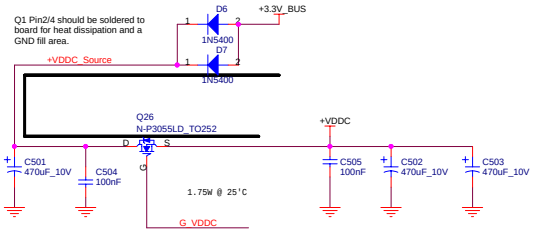
+VDDC	Range	Rcx1 Rc1	Rcx2 Rc2
1.62V	1.619V ~ 1.635V	1K 3240100100	3.32K 3240332100

These dummy resistors are placed under the diodes to avoid PCB heat damage due to hot diodes. layout engineer don't move these components' position

R554 0R R553 0R R552 0R R551 0R

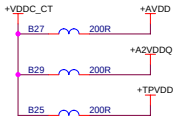
OPTIONAL





AVDD/A2VDDQ (1st DAC & 2nd DAC Band Gap)

TPVDD



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Buffered Shunt Regulator for MVDDQ & VDDR1
Vin = 3.3V AGP
Vout = 2.5V
Iout = 1200mA MAX
Iout = 1000mA Est. MAX

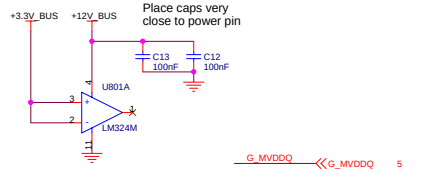
Type	Voltage Req.	Rq1	Rq2
Elpida	1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
	2.5V	1K 3240100100	1K 3240100100
	2.6V	4.75K 3240475100	4.32K 3240432100

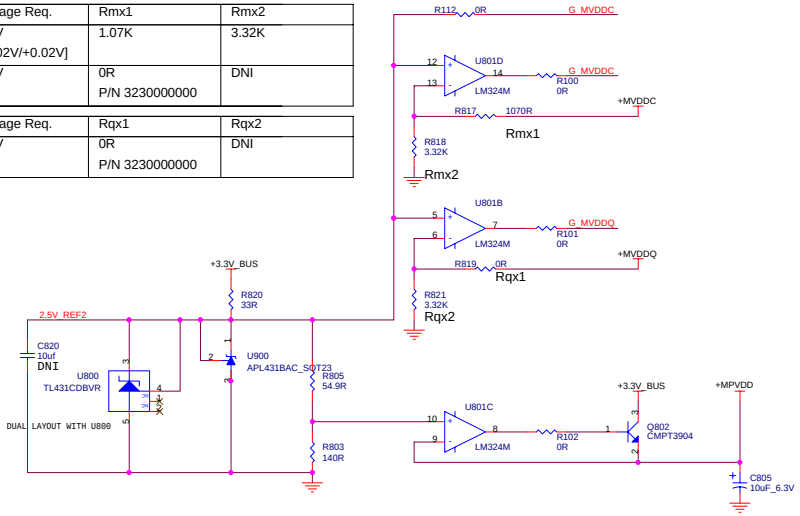
Buffered Shount Regulator for MVDDC
Vin = 5V
Vout = 3.3V
Iout = 1.4A MAX

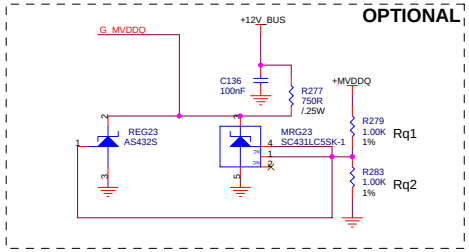
	Voltage Req.	Rm1	Rm2
Hynix	3.22V [-0.04V/+0.04V]	4.32K P/N 3240432100	2.74K P/N 3240274100
	3.34V [-0.04V/+0.04V]	4.32K P/N 3240432100	2.55K P/N 3240255100
	3.45V [-0.04V/+0.04V]	4.32K P/N 3240432100	2.43K P/N 3250243100
Sumsung	2.56V [-0.03V/+0.03V]	2.55K P/N 3240255100	2.43K P/N 3250243100

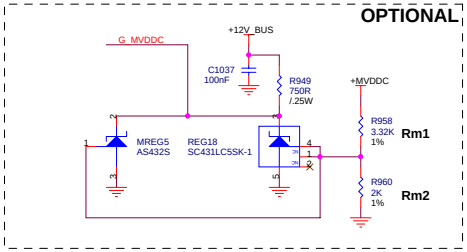
+MVDDC	Voltage Req.	Rmx1	Rmx2
	3.3V [-0.02V/+0.02V]	1.07K	3.32K
	2.5V	0R P/N 3230000000	DNI

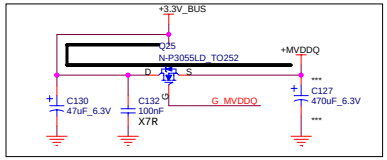
+MVDDQ	Voltage Req.	Rqx1	Rqx2
	2.5V	0R P/N 3230000000	DNI





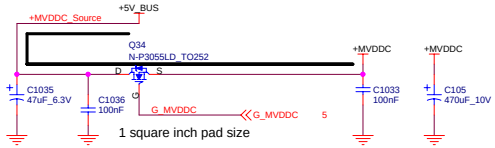




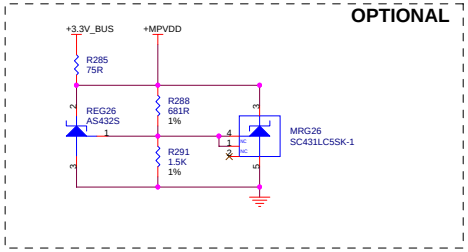


no stuff

Q34 Pin2/4 should be soldered to board for heat dissipation and a GND fill area.



Buffered Shount Regulator for MPVDD
Vin = 3.3V
Vout = 1.8V
Iout = 10mA MAX



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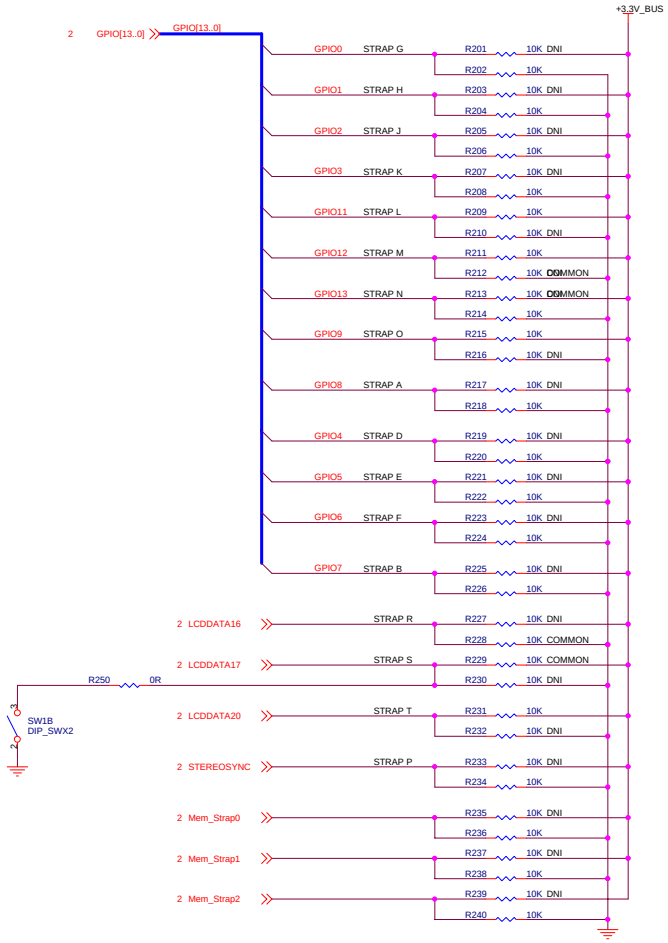
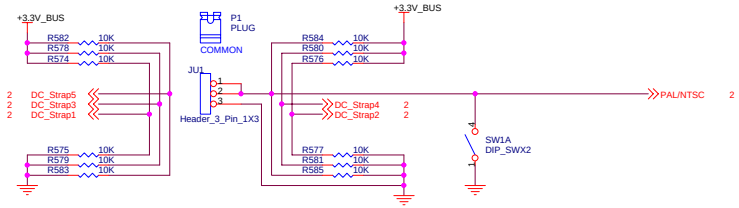


OPTION STRAPS

STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM **1011 - Serial M25P05/10 ROM (ST), chip IDis from ROM** 1100 - Reserved 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1100
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000 (internal pull-down)
VGA_DISABLE	GPIO(7)	**0 - VGA controller capabillity enabled.** 1 - The device will not be recognized as the systemis VGA controller.	0
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select 00 - single function device. 01 - two function device. No AGP in either function **10 - two function device. AGP only in function 0** 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	10
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. **0 - Slave VIP host port devices present** 1 - No slave VIP host port devices reporting presence during reset	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

Daughter Card Straps



STRAPS	PIN		DESCRIPTION
DC_STRAP1	LCDDATA12		Internal TMDS Enabled **0 - Disabled** 1 - Enabled
DC_STRAP2	LCDDATA13		Video Capture Enabled **0 - Disabled** 1 - Enabled
DC_STRAP4 DC_STRAP5	LCDDATA15	LCDDATA19	DAC2 Configuration
	0	0	DAC2 Off
	0	1	DAC2 On as CRT
	1	0	DAC2 On as TVOUT
	1	1	DAC2 On as TVOUT and CRT
DC_STRAP6	LCDDATA18		TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 -NTSC (on board resistor pull-up)

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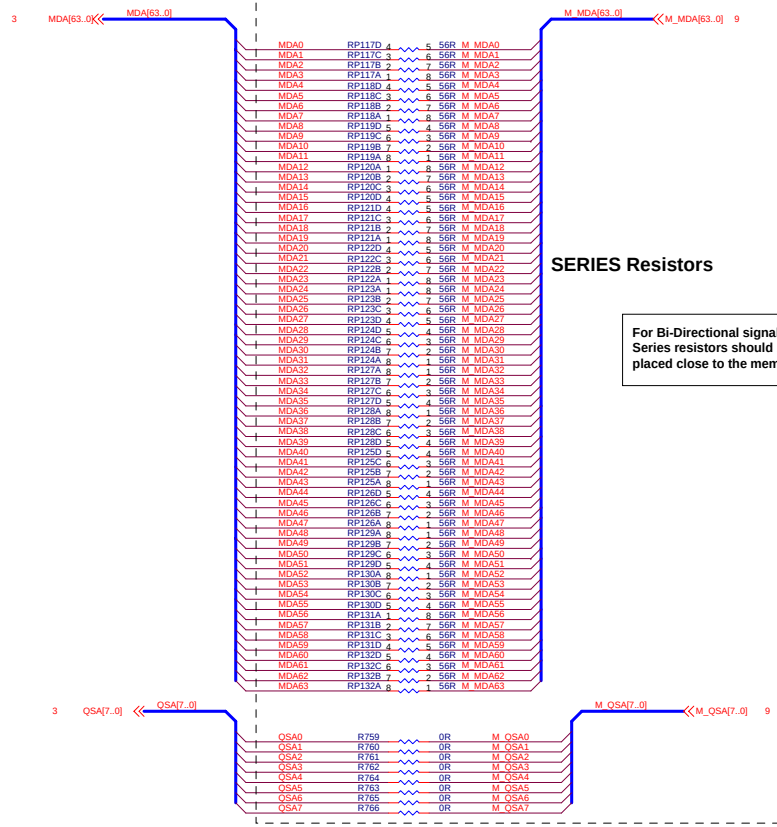
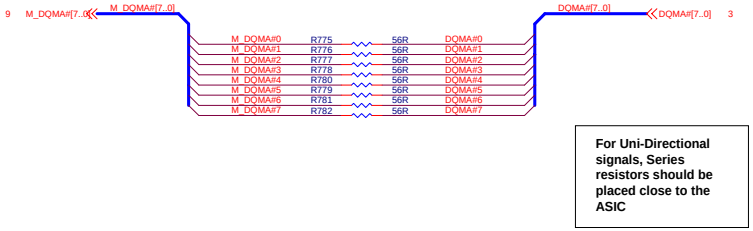
TERMINATION FOR MEMORY CHANNEL A



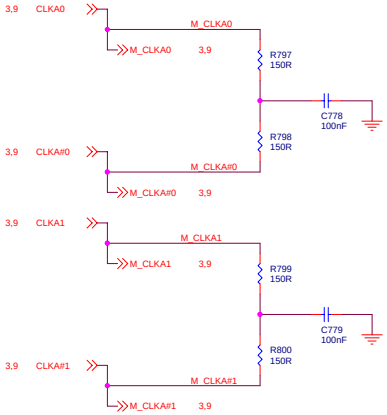
Proper Termination of QSA?



CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



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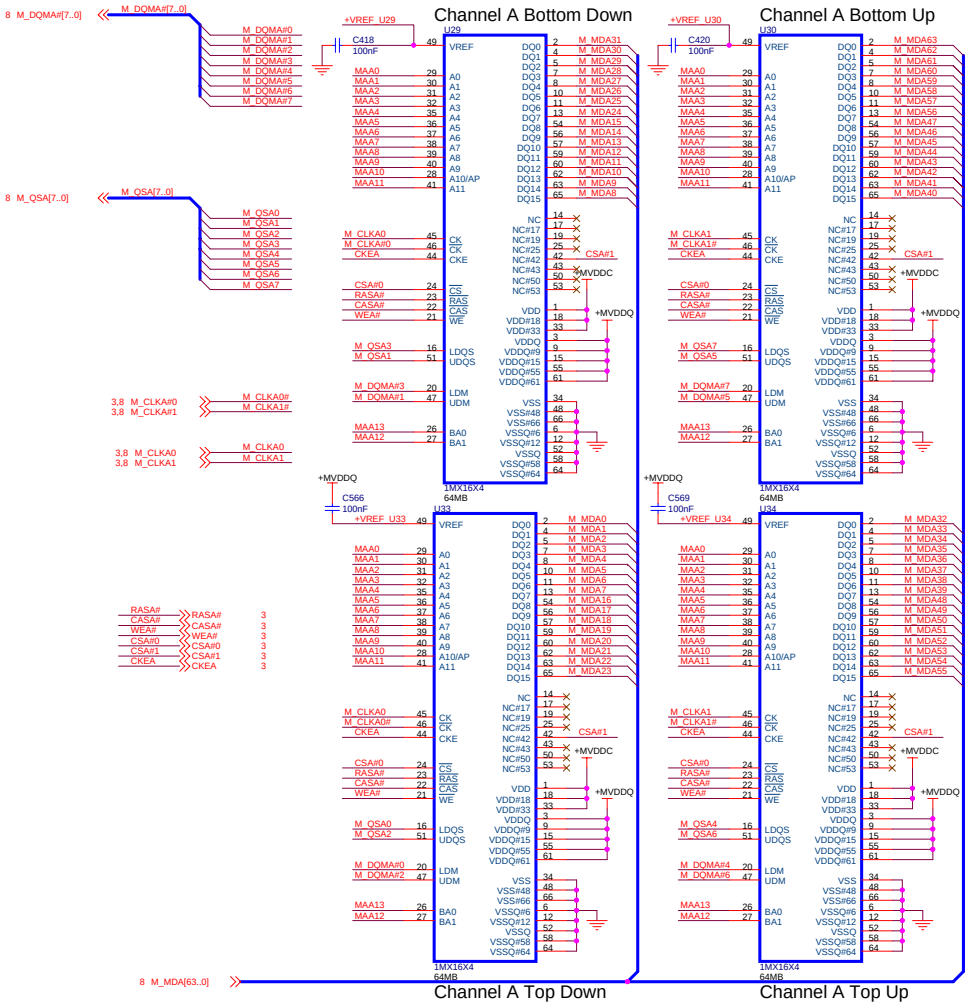
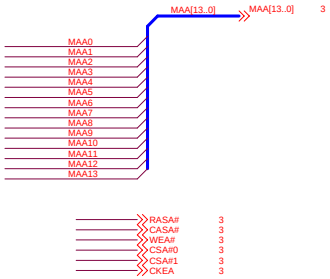
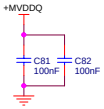
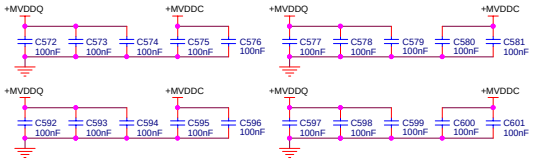


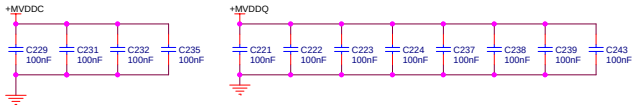


Put 1 1uF cap per power pin of memory



2 capacitors SHOULD BE PLACED CLOSE TO THE REFERENCE LAYER CHANGE OF CLOCKS FOR EMI REDUCE.





Part number for 8Mx16: 2354274204 (Samsung)

DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

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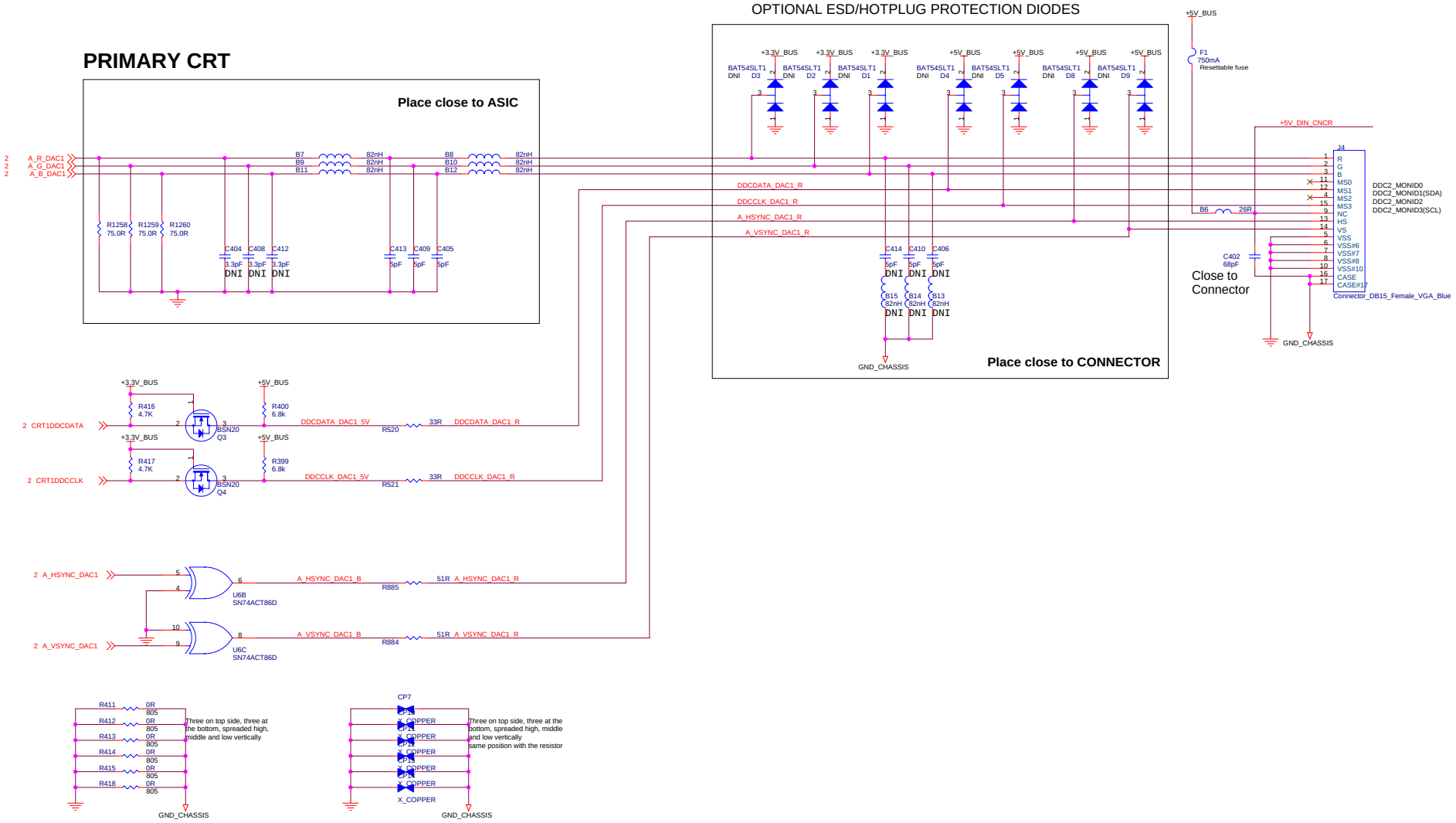

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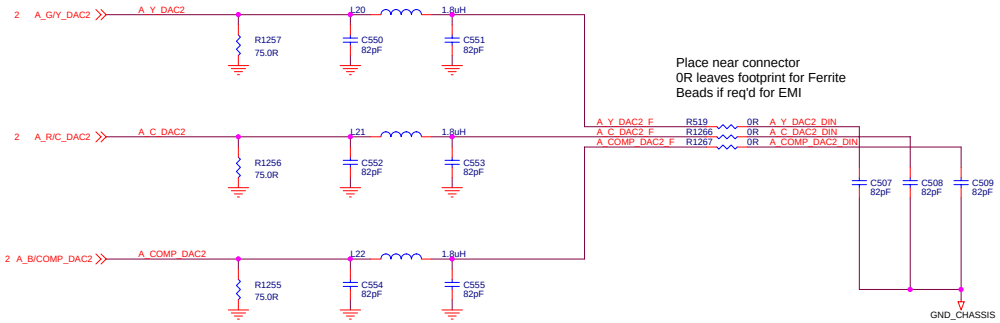
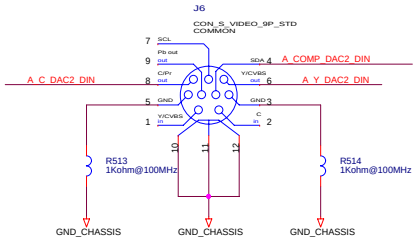
Place Resistors close to ASIC.





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CRT SCREWS

ASSY1

SCREW
JACKSCREW
ASSY

ASSY2

SCREW
JACKSCREW
ASSY

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM4 SW_FB
FM5 SW_FB
FM6 SW_FB
FM7 SW_FB
FM8 SW_FB

PCB

PCB

BKT1 NPTH126

COMMON

GND_CHASSIS

MECH MOUNTING TOP

BRACKET

Heatsink

MH101

HEATSINK

STD COMMON SCREW-1

MEC_SCREW

STD COMMON SCREW-2

MEC_SCREW

STD COMMON MEC5

MEC_SCREW

STD COMMON MEC6

MEC_SCREW

Dual layout with R3008

+3.3V_BUS

U902

PIN1

status

7SZ04P5X_SC70

Dual layout with R3004

+3.3V_BUS

U903

status

fan_s

7SZ04P5X_SC70

FAN Control

+5V_BUS

no stuff

R3007
2.1KR1%

+3.3V_BUS

R3010
4.7KR

R3004
0R

fan_s

fan_s

2

J900

FAN-
FAN+
PIN1

R3008
0R

status

BH1X3_white-2pitch

status
FAN+
FAN-

R3006
0R

+12V_BUS

R3005
4.02KR1%

R3009
0R no stuff

Q1

N-MMBT3904_SOT23
no stuff

C850
C0.1U50Y

GND

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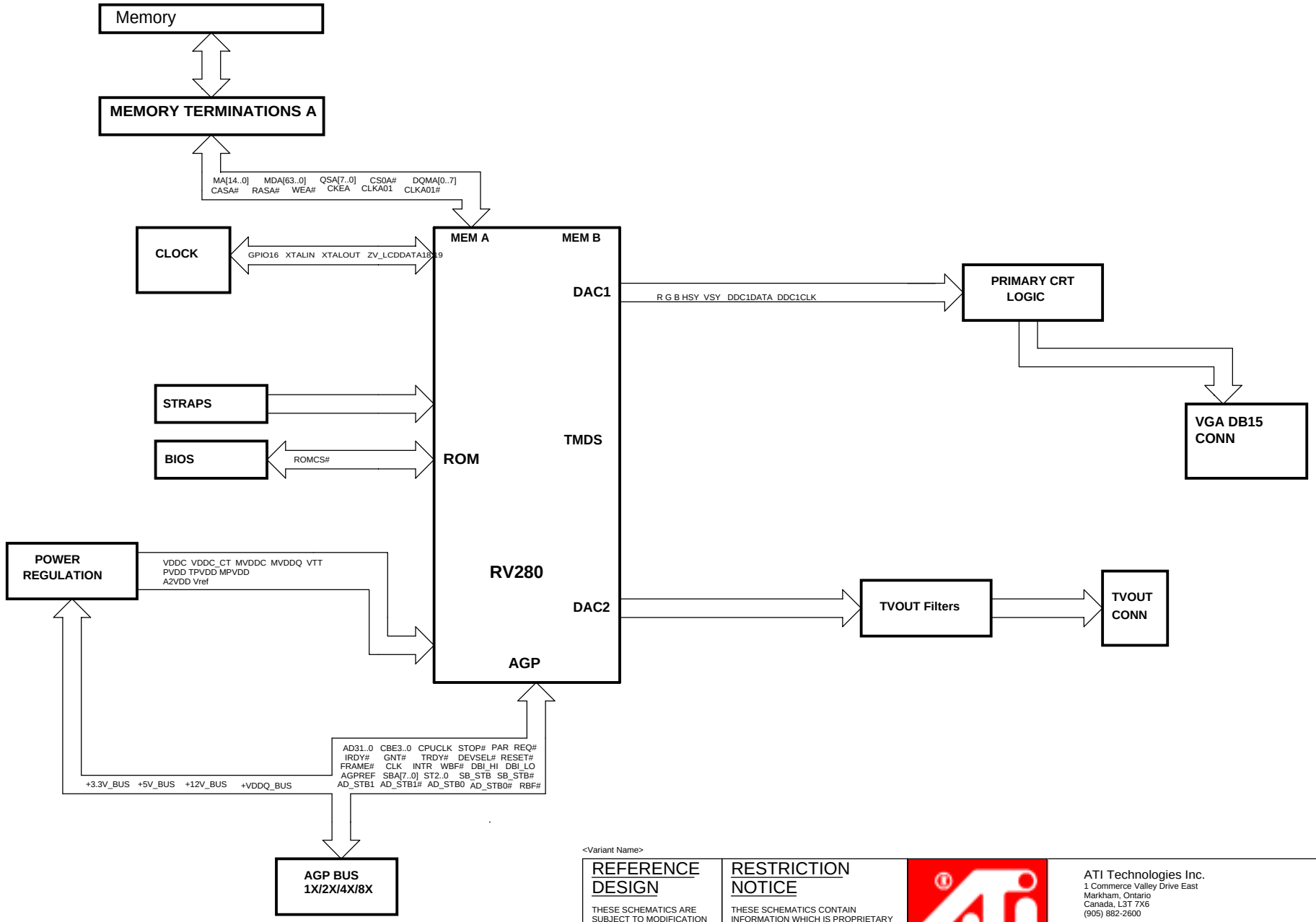
MEMORY CHANNEL A



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REFERENCE DESIGN

THESE SCHEMATICS ARE SUBJECT TO MODIFICATION AND DESIGN IMPROVEMENTS. PLEASE CONTACT ATI FIELD APPLICATION ENGINEERING BEFORE USING THE INFORMATION CONTAINED HEREIN.

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<variant Name>

Title	Schematic No.	Date:
RV280 LP AGP8x 128MB 16Mx16 DDR	105-A165XX-00	**Wednesday, February 25, 2004**

REVISION HISTORY

Rev 2

Sch Rev		Date	REVISION DESCRIPTION
0	00A	03/25/03	Based on 105-A062xx-00 schematic (pg2) Add pull-up on CS# for flashrom (pg5) Replace swiching VDDC regulator with Op-Amp regulator circuit (pg5) Add Op-Amp regulator circuit for low-cost design (pg6) Add Op-Amp regulator circuit for low-cost design (pg6) Remove C317 Thru-hole Alum. Cap for MVDDC (pg6) Add +3.3V_BUS directly to +MVDDC option (pg11) Modify VO connector filter chassis ground connections
		04/01/03	(pg5) Replace VDDC 470uF with thru-hole (pg6) Add thru-hole 470uF on +MVDDC for option
		04/10/03	(pg6) Remove C1, C17 and C1034
1	00B	05/14/03	(pg5) Remove Q811 and Q814 (pg6) Add C805 10uF tant. cap on +MPVDD (pg6) Add R112 to bypass opamp for +MVDDC (pg6) Remove diodes (D10 and D11) and resistors (R111, R1261, R1262, R1263 and R1264) for +MVDDC (pg5, 6) Add R104 to drive +MVDDC from alternate shunt reference (pg7) Add jumper J1 for PAL TVO default (Layout) Add silscreen for switch and jumper (Layout) Correct MiniDIN J6 footprint (Layout) Correct diode clearance for manufacturing request (Layout) Move sticker location
2	00	05/30/03	(pg9) Replace a 2-pin with a 3-pin jumper for NTSC/PAL section. (pg5) Add R812, R813 and R815 for +MVDDC voltage adjustment (Layout) Change footprint of P/N4238010600