P2030

GK106, 2GB GDDR5, 192b mixed mode x16, x32

Stacked DVI-I/DVI-D + HDMI/DP + DP

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SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-12030-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-12030-0000-000	GK106-400, 2048MB, GDDR5 192b Stacked DVI-I DL/DVI-D DL, HDMI, DP
2	SKU0010	600-12030-0010-000	GK106-250, 2048MB, GDDR5, 192b Stacked DVI-I DL/DVI-D, HDMI, DP
3	SKU0050	600-12030-0050-000	GK106-200, 2048MB, GDDR5, 128b Stacked DVI-I DL/DVI-D, HDMI, DP
4	SKU0500	600-52030-0500-000	GK106-875, 3072MB, GDDR5, 192b DVI-I, DP, DP Workstation
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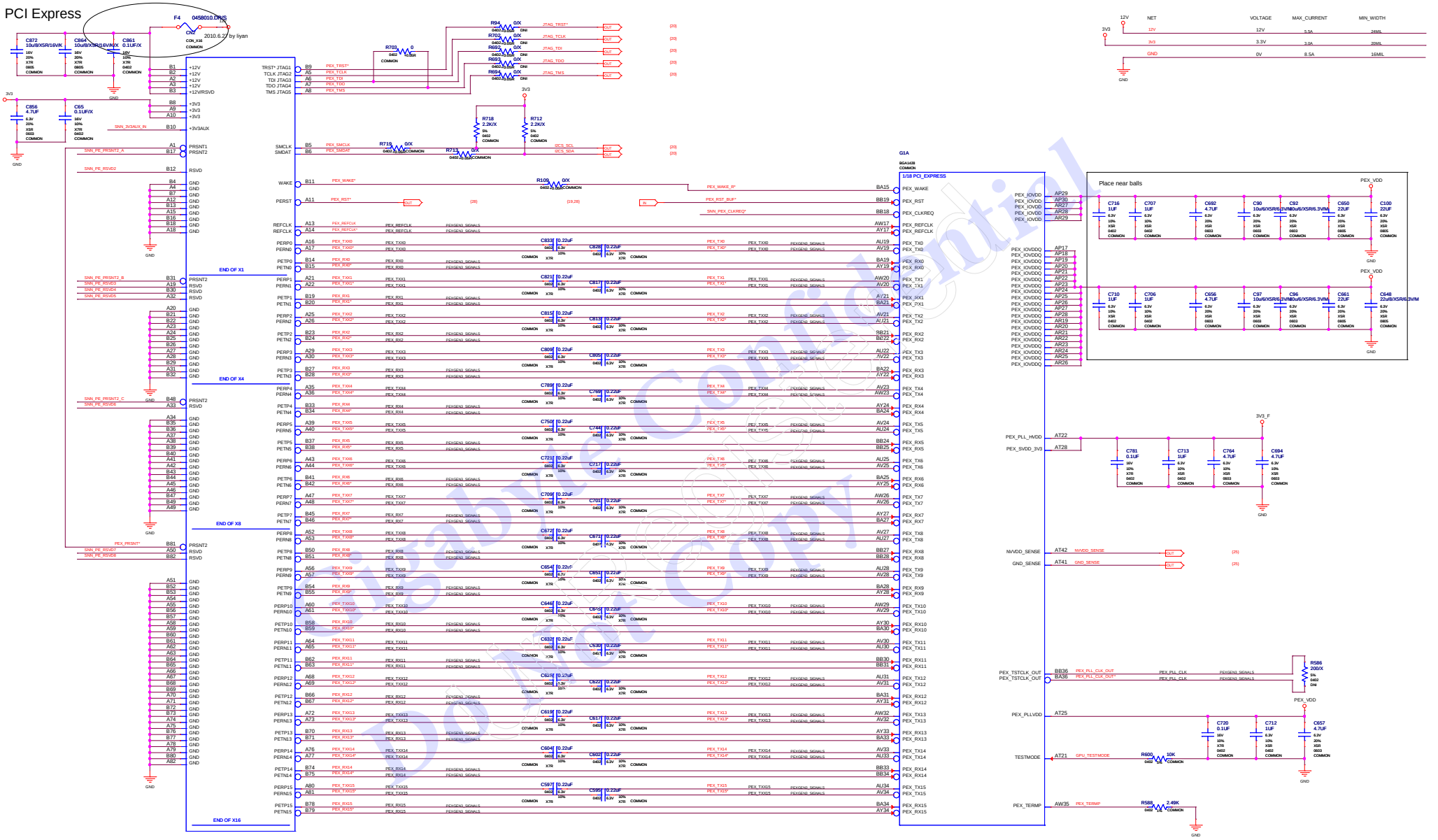
Title: Table of Contents			
Size: Custom	Document Number: GV-N660WF2-2GD		Rev: 1.0
Date: Wednesday, October 24, 2012	Sheet 1 of 31		



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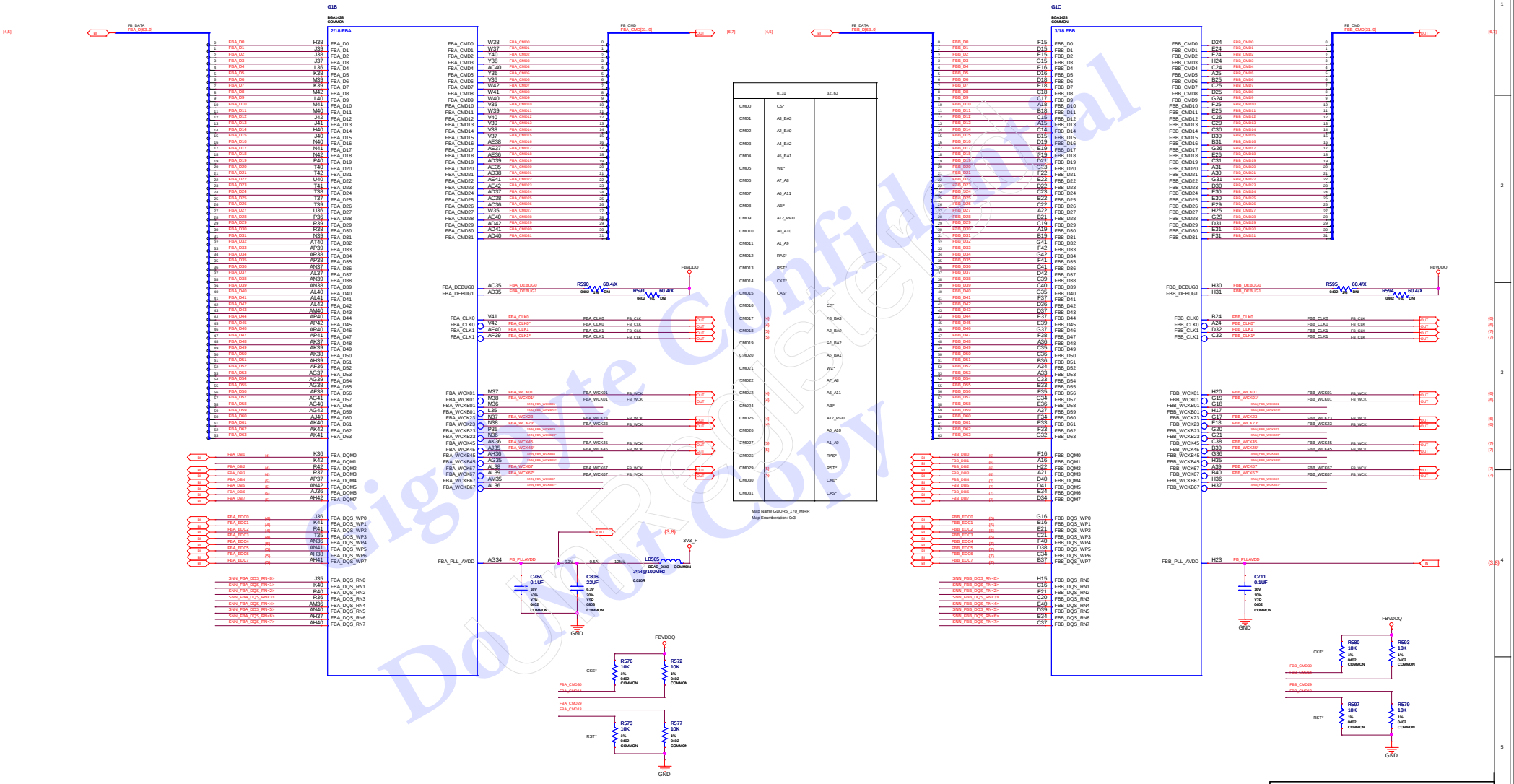
MEMORY: GPU Partition A/B



ASSEMBLY
PAGE DETAIL

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MEMORY: GPU Partition A/B

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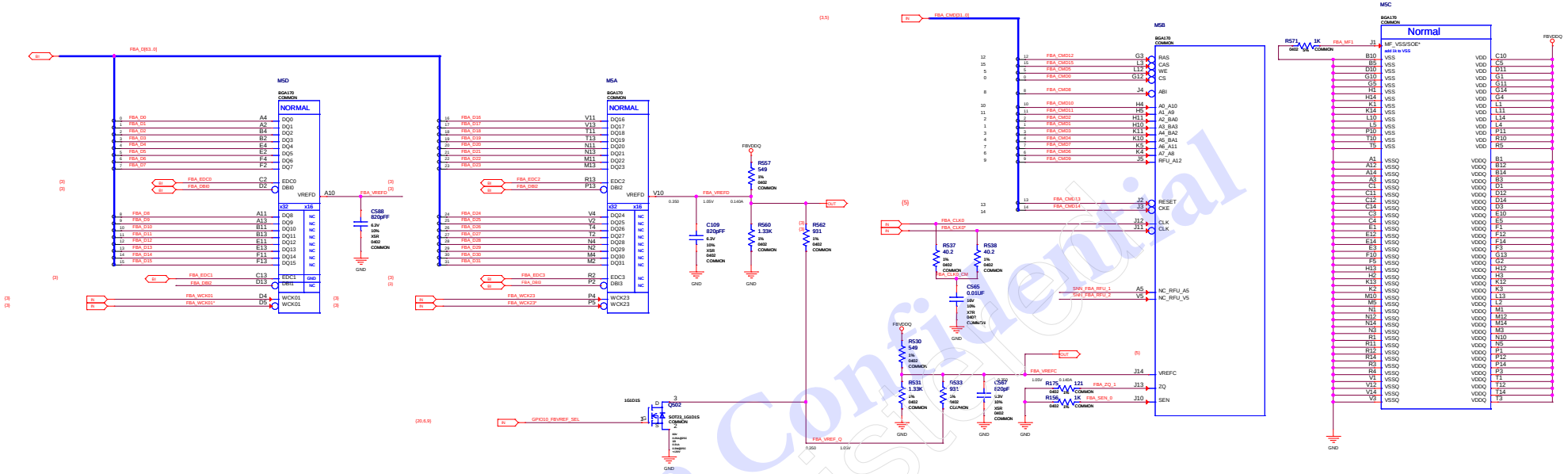
Size: Custom | Document Number: GV-N660WF2-2GD | Rev: 1.0

Date: Wednesday, October 24, 2012 | Sheet 3 of 31

MEMORY: FBA Partition 31..0



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PAGE DETAIL	MEMORY: FBA[31:0]

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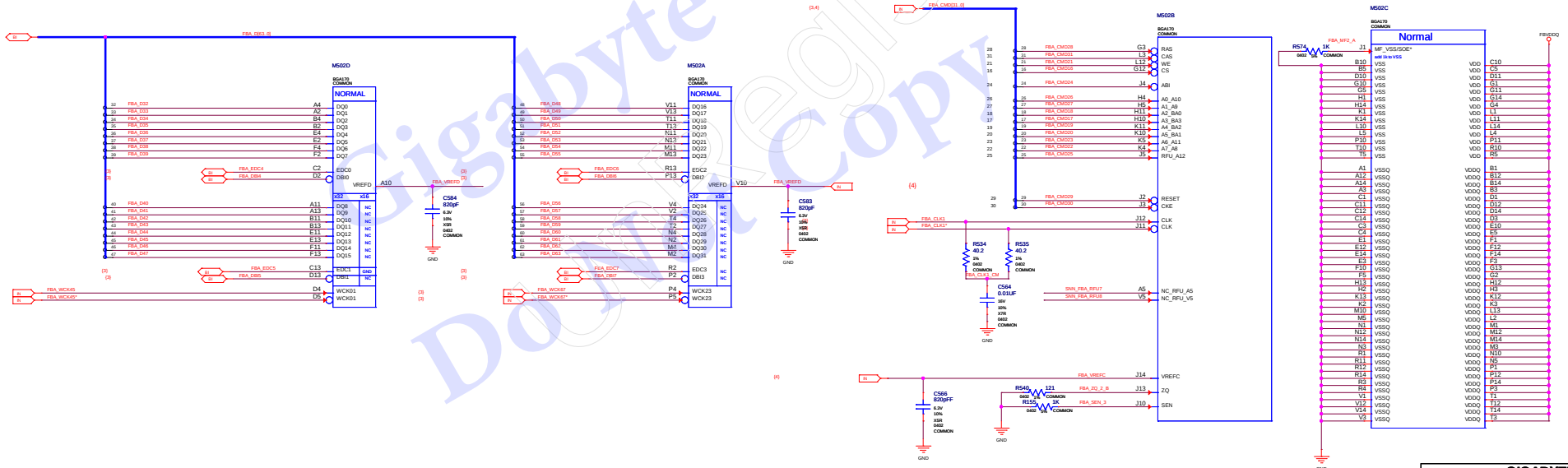

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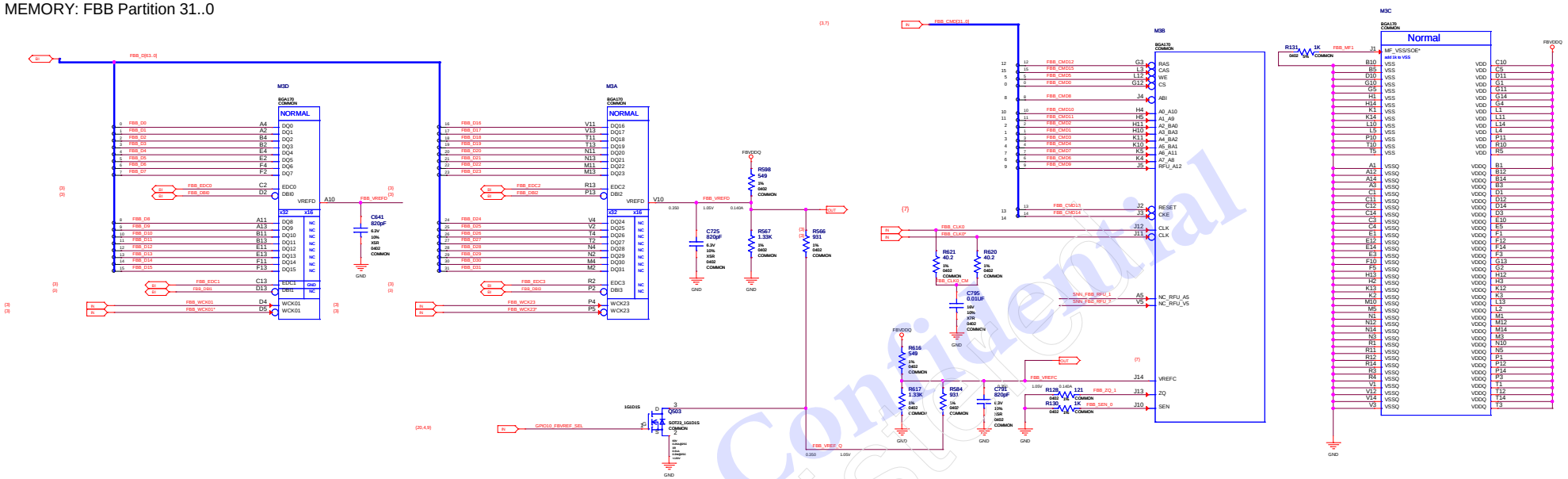

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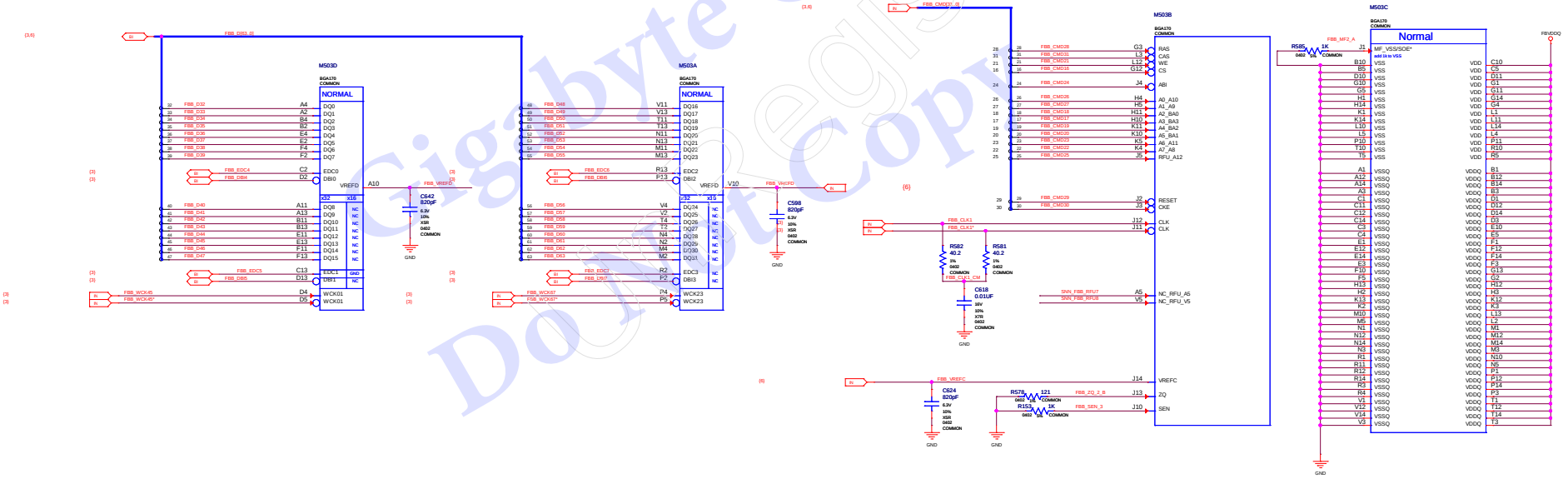

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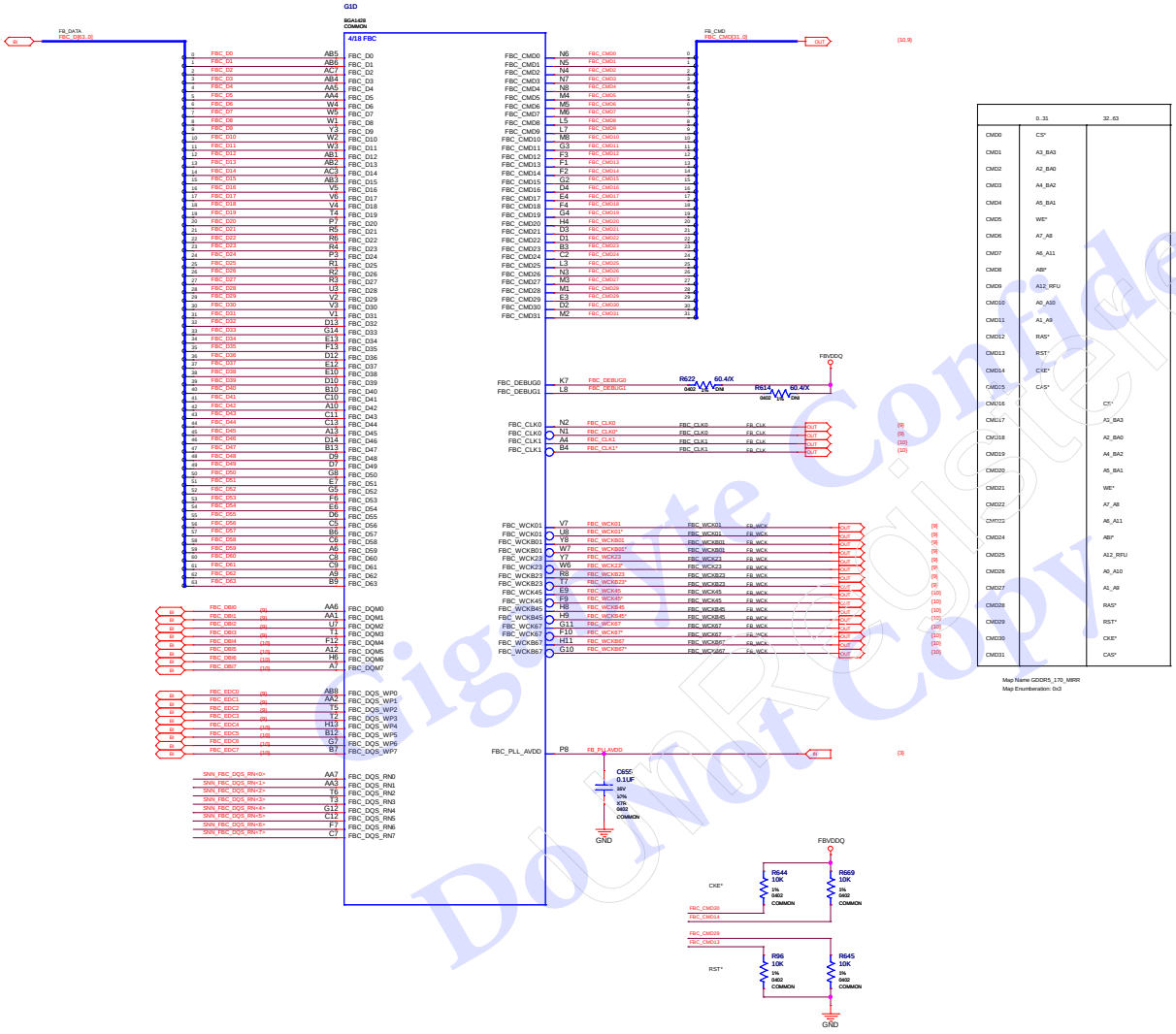

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MEMORY: GPU Partition C

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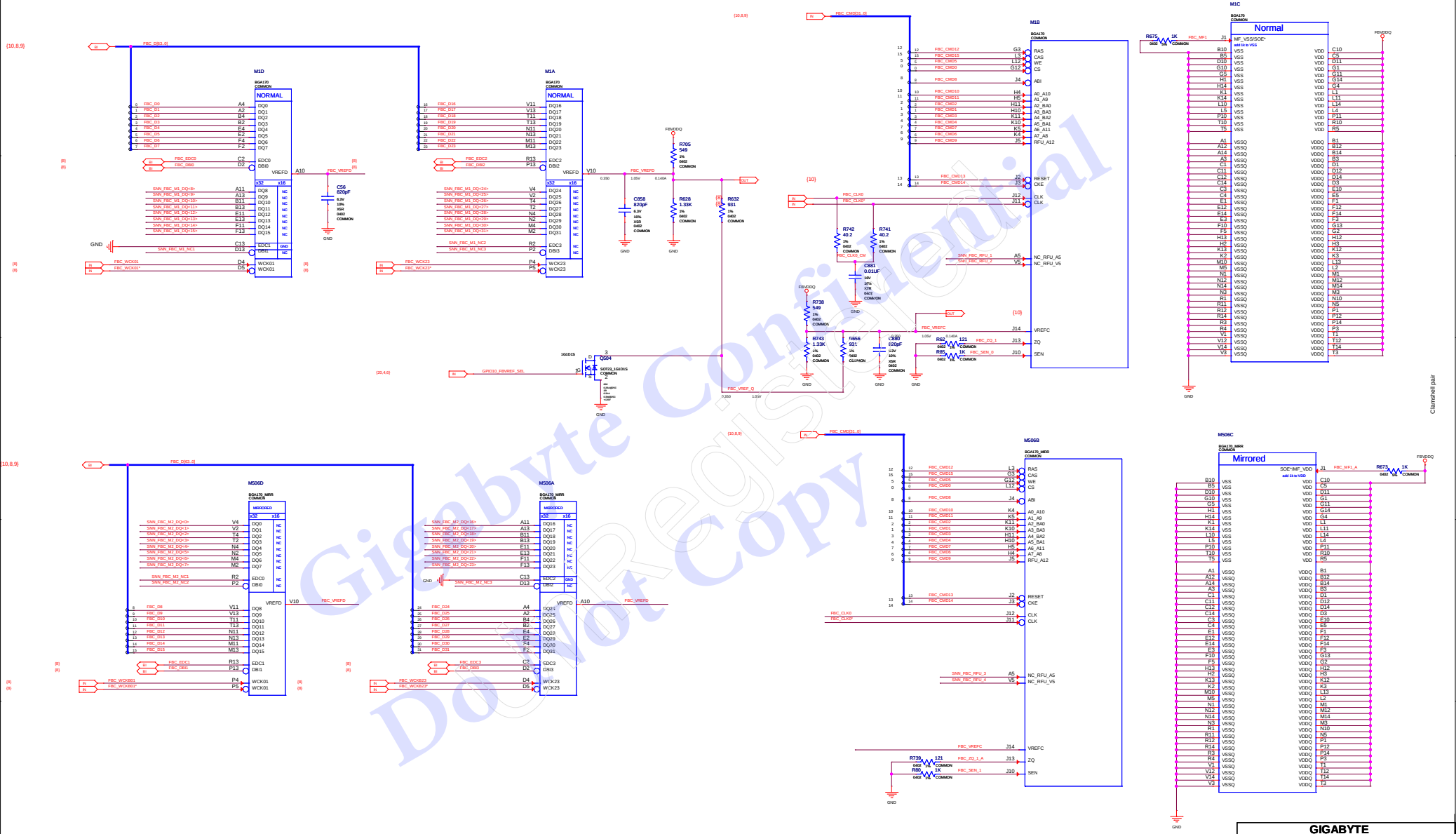

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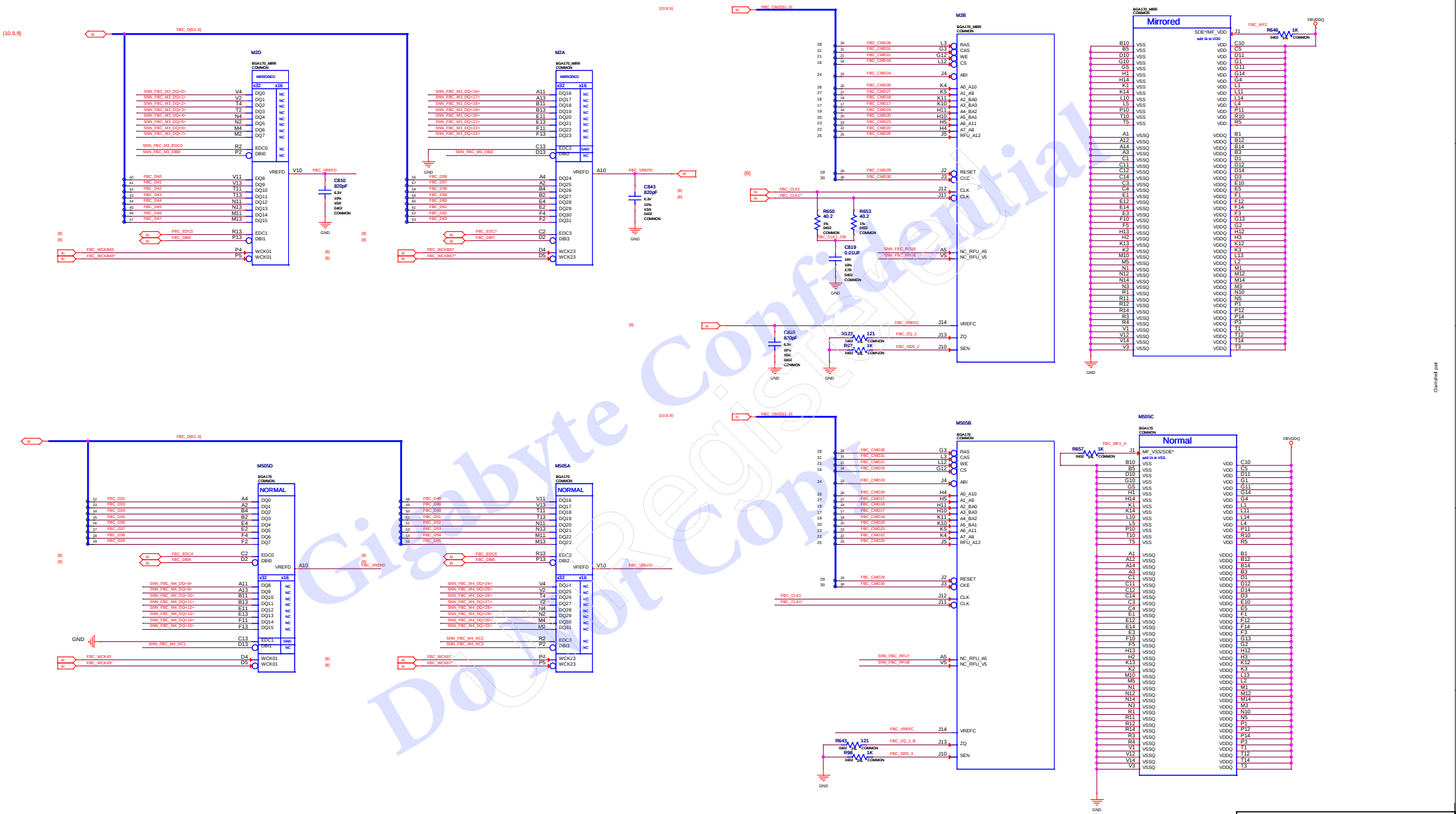

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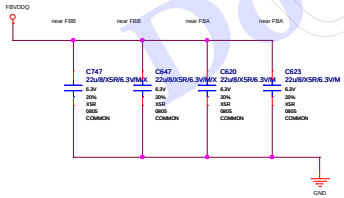
MEMORY: DECAP

FBA

FBB

FBC



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MEMORY: DECAP

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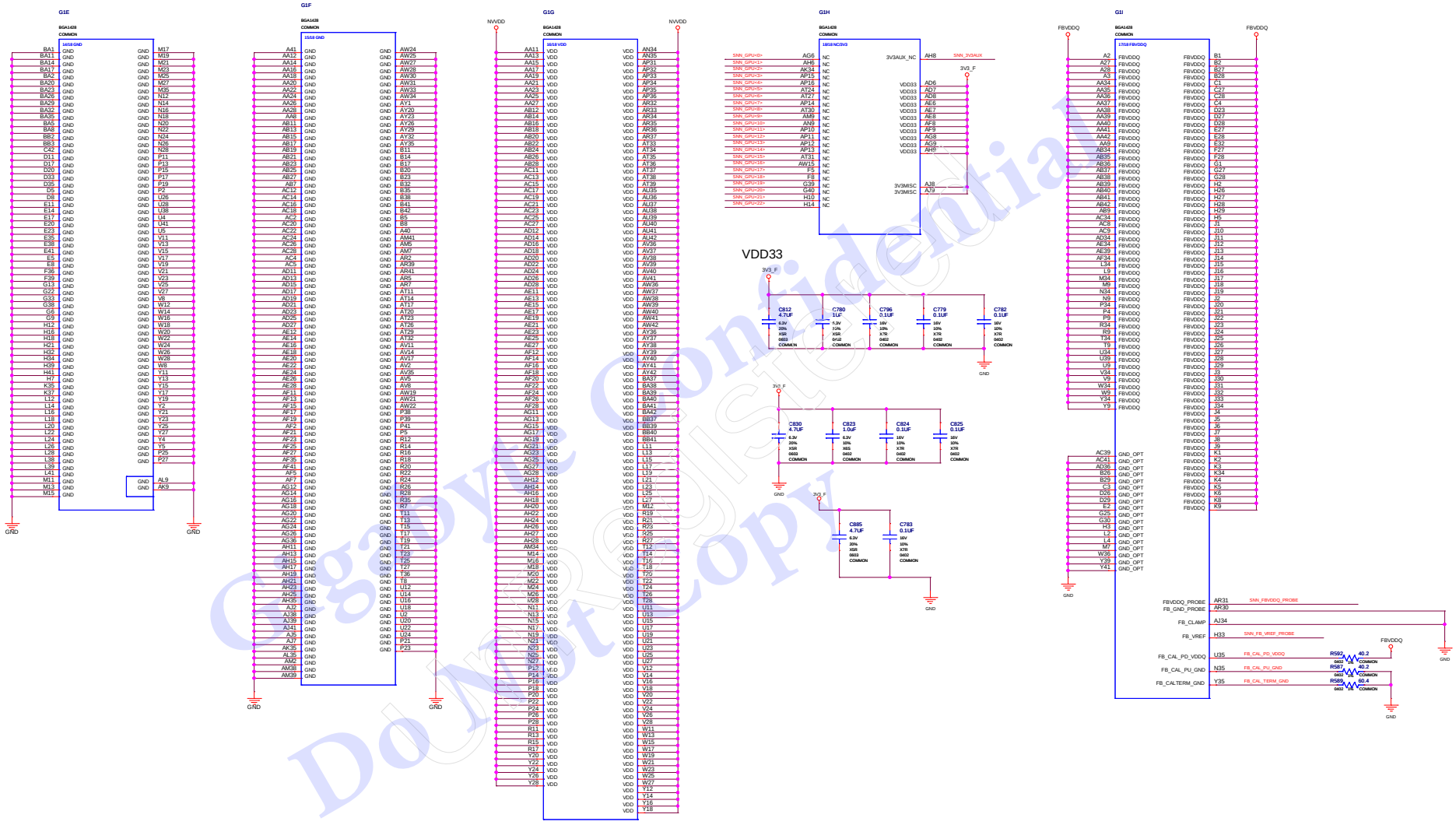
GPU PWR and GND



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PAGE DETAIL	GPU PWR and GND

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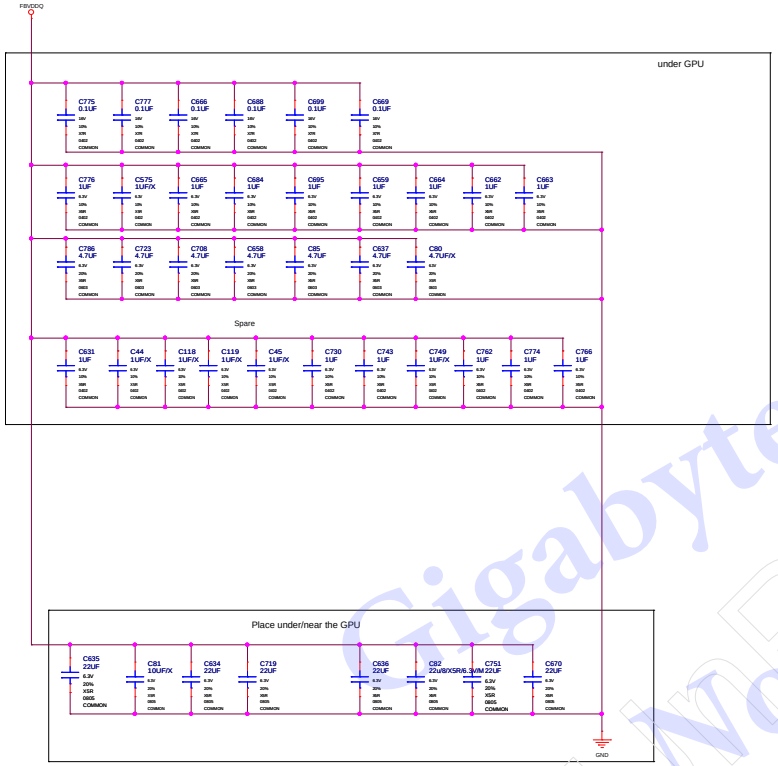
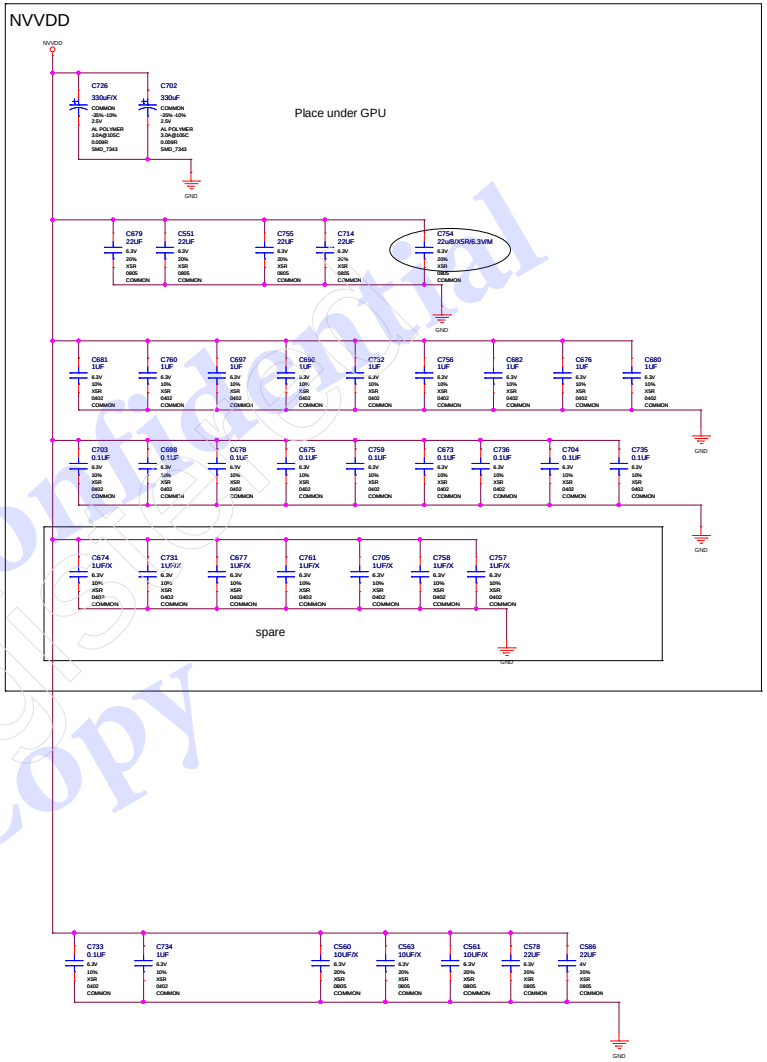
GPU Decoupling

FBVDDQ



NVVDD



	guidelines	actual
Under GPU	2x 330uF 9mOhm	1x 330uF 9mOhm
	1x 47uF 1206	1x 22uF 1206
	2x 22uF 805	4x 22uF 805
	2x 10uF 805	9x 1uF 402
	9x 1uF 402	9x 0.1uF 402
	9x 0.1uF 402	
		spare sites (not stuffed)
		1x 7343
		27x 402
near GPU	1x 47uF 1206	2x 22uF
	2x 22uF 805	
	2x 10uF 805	spare sites (not stuffed)
	2x 4.7uF 603	3x 805
	1x 1uF 402	
	1x 0.1uF 402	

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GPU Decoupling

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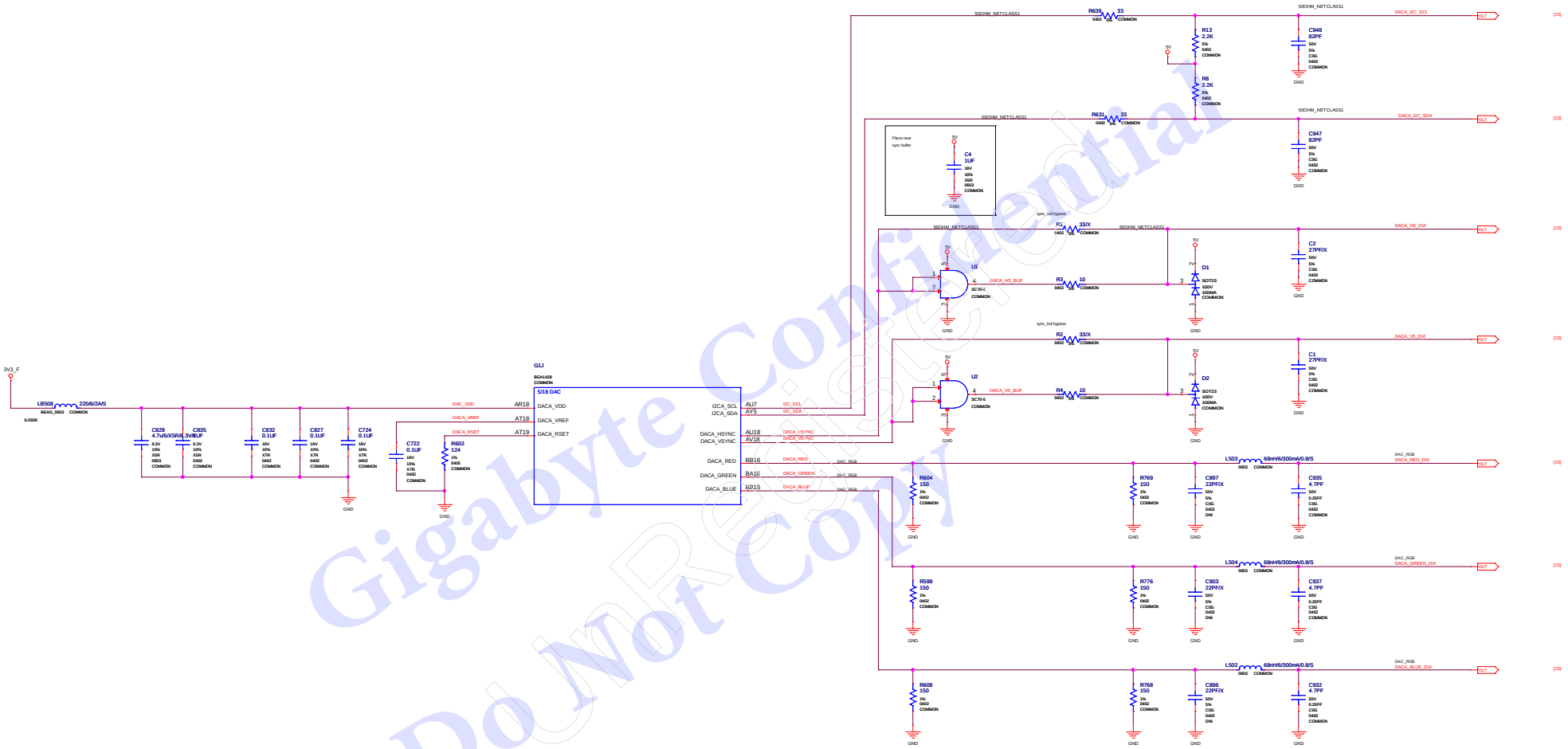
DACA Interface



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DAC_VDD	3.3V	0.25A	16MIL

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PAGE DETAIL

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DACA Interface

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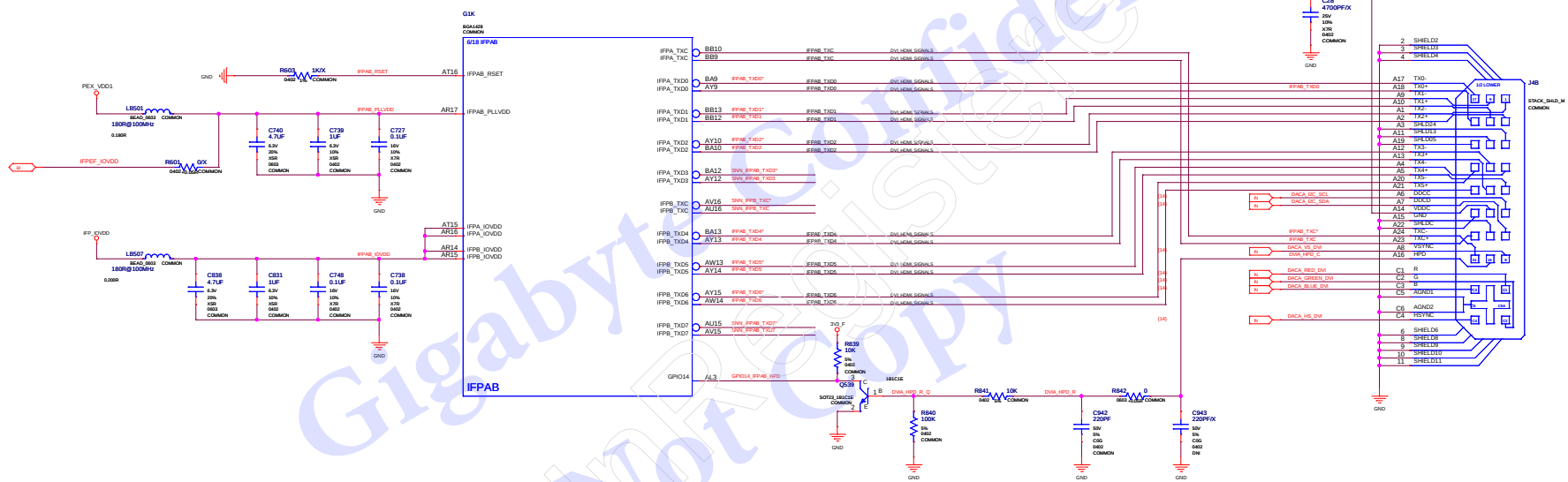
IFPAB DVI-I-DL



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IFPAB_IOVDD	3.3V	0.15A	0.406

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IFPAB DVI-I-DL

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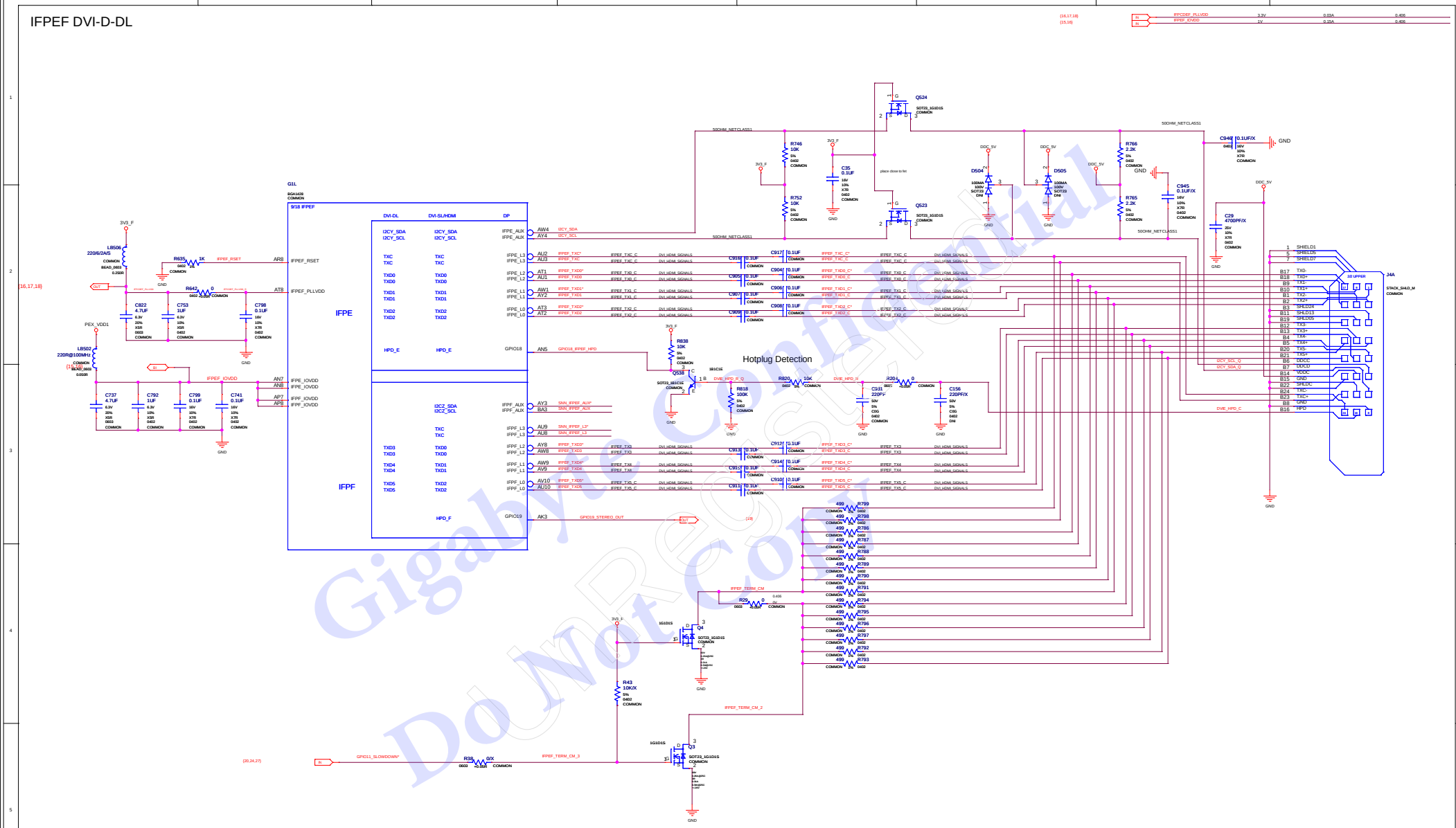
IFPEF DVI-D-DL



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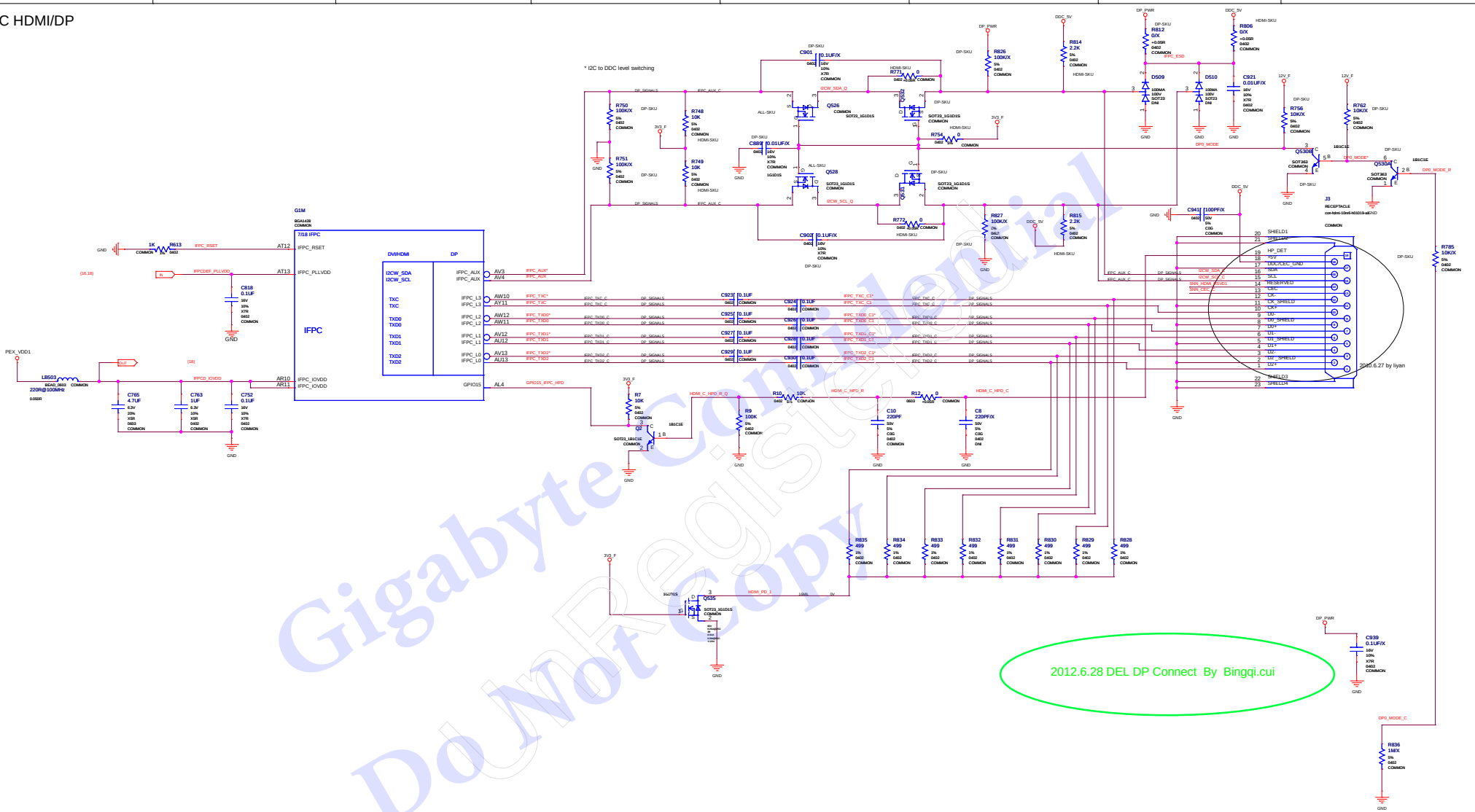
IFPC HDMI/DP



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ASSEMBLY
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BASE LEVEL GENERIC SCHEMATIC ONLY
IFPC HDMI/DP

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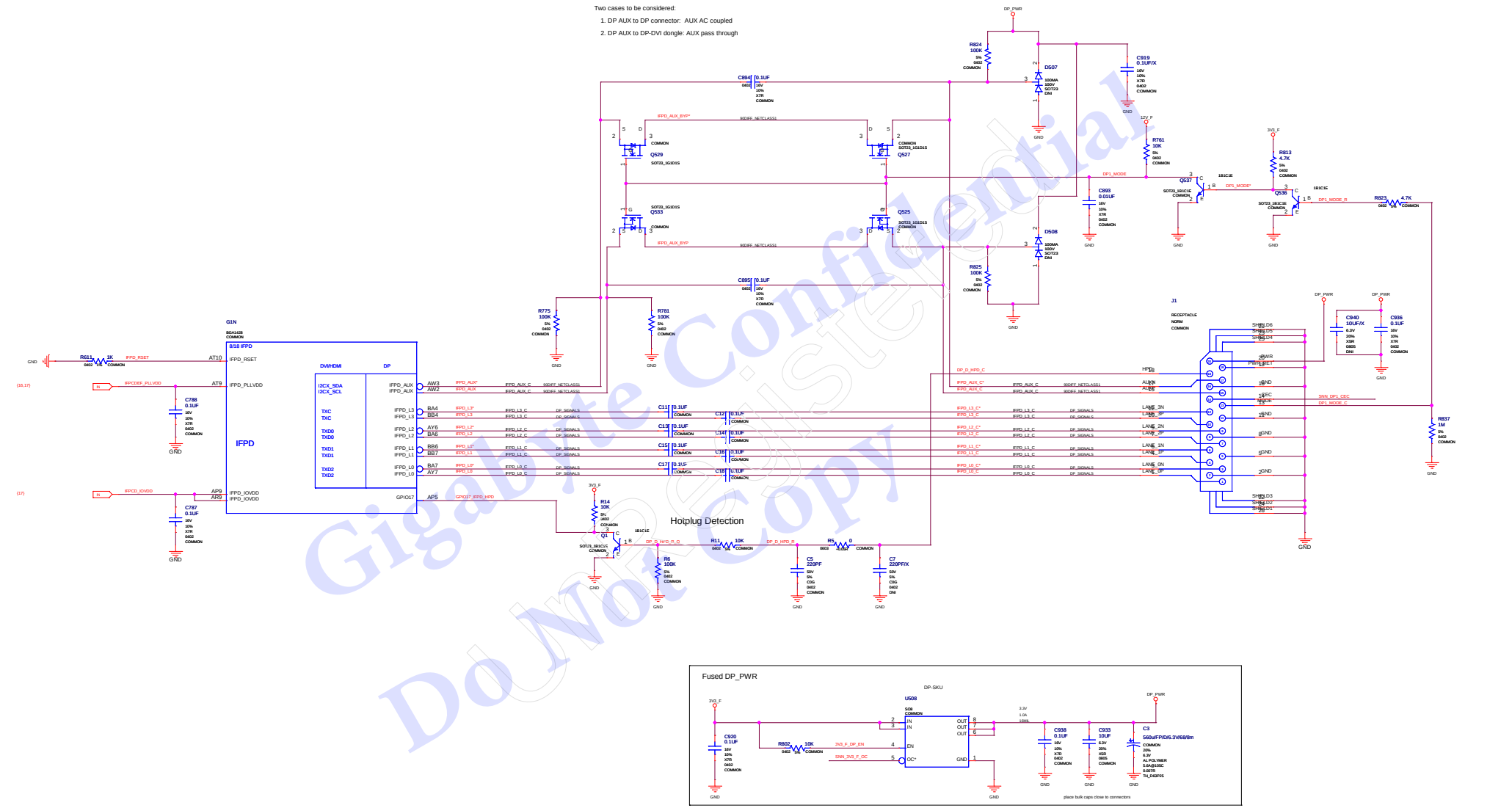
IFPD DP



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IFPD DP

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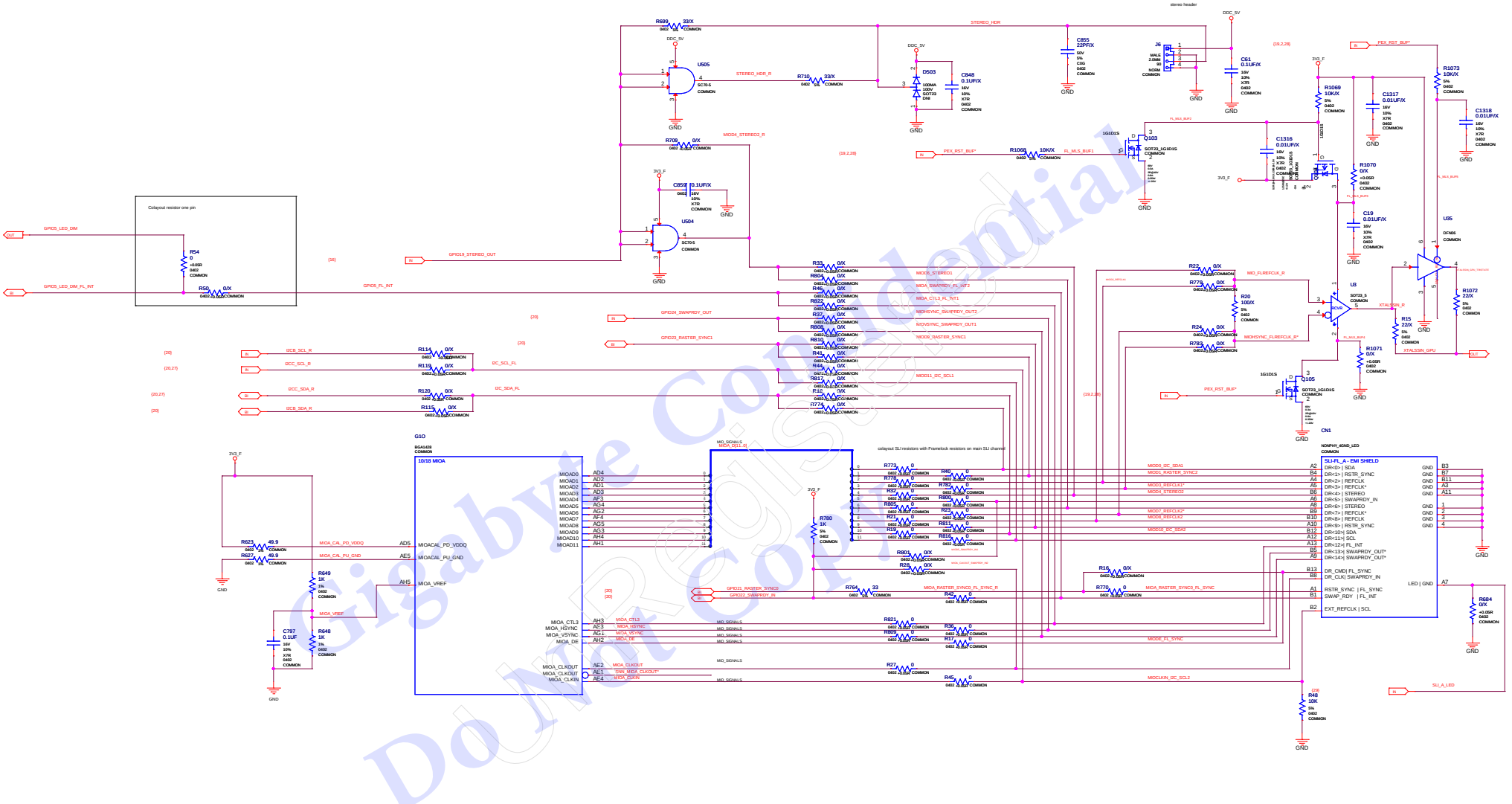
MIOA/SLI Interface



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	1.49V		0.305
MIOA_CAL_PD_VDDQ	2.5V		0.305
MIOA_CAL_PU_GND	0.0V		0.305

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MIOA/SLI/Stereo Hdr Interface

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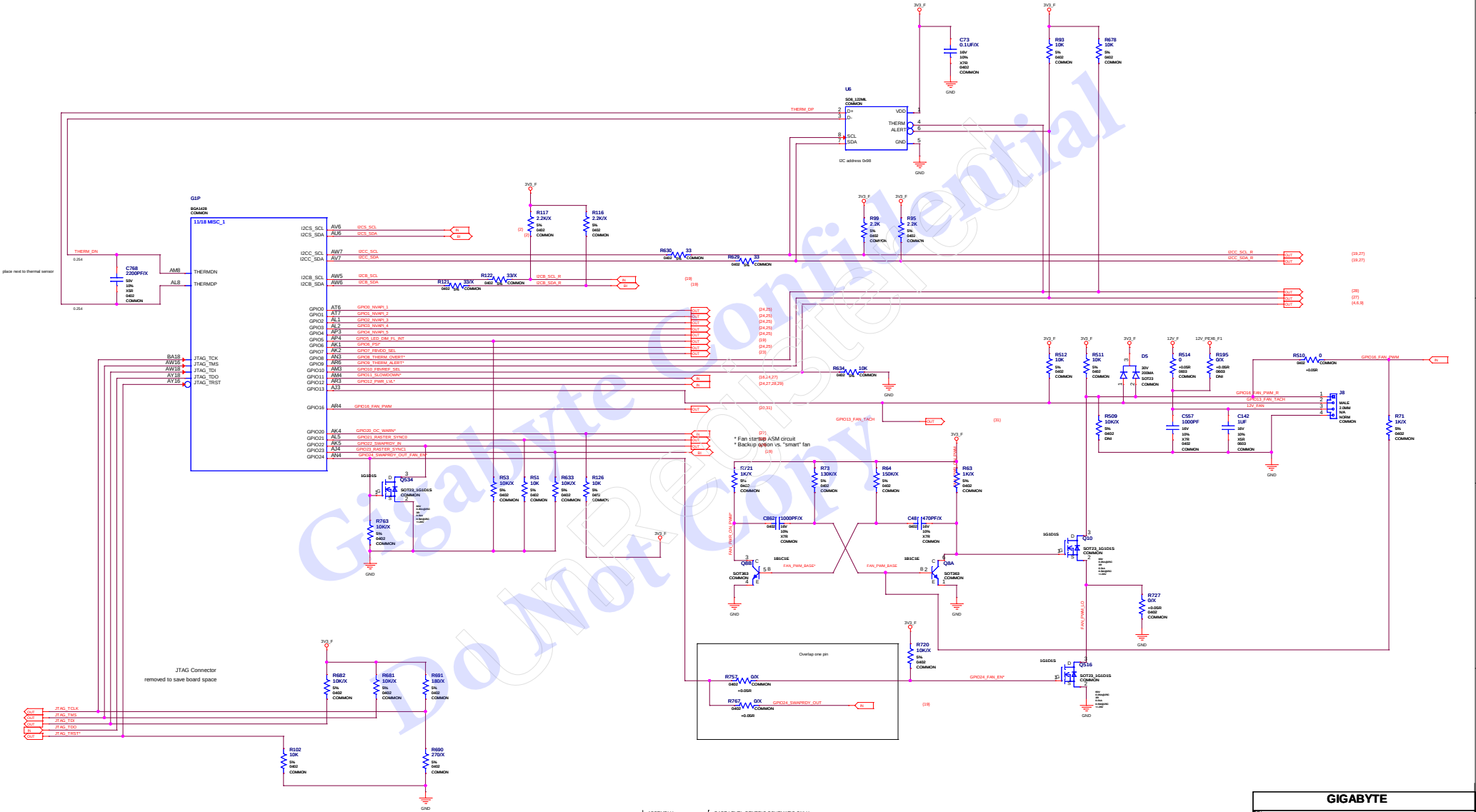
MISC1: Fan, Thermal, JTAG, GPIO



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BASE LEVEL GENERIC SCHEMATIC ONLY
MISC1: Fan, Thermal, JTAG, GPIO

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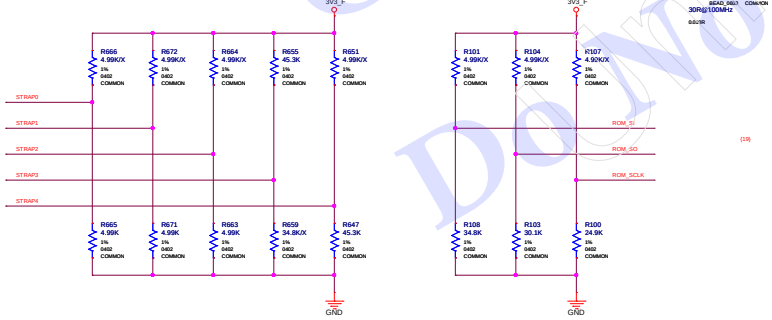
MISC2: ROM, XTAL, Straps

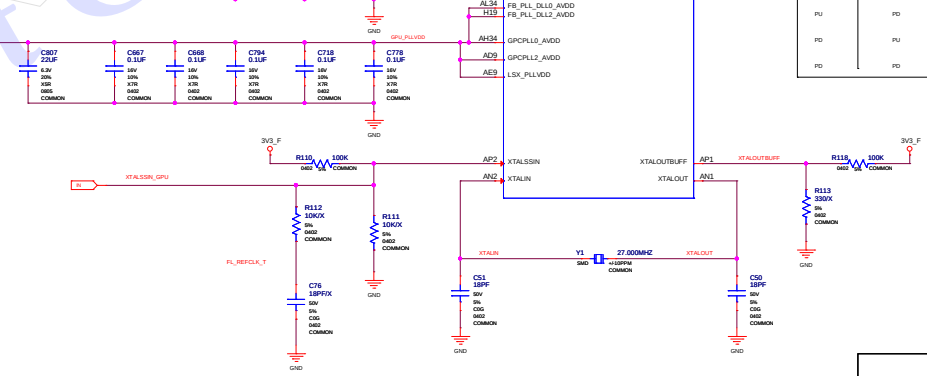
STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0000 - (0x11C0)* 0010 - (0x11C1)* 0050 - (0x11C4)* 0500 - (0x11FA)*	5K PD -400 GPU* 10K PD -250 GPU* 25K PD -225 GPU* 15K PU -875 GPU*

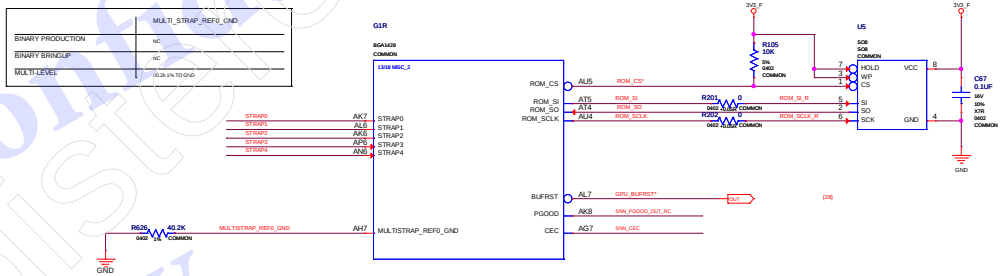
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

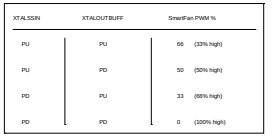
STRAP3	SOR_EXPOSED [3:0]*	1111*		45K PU*
STRAP4	*			
	PEX_SPD_CHANGE_GEN3*	1*	ENABLED*	45K PD*
	PEX_MAX_SPEED*	1*	FOR GEN2/3*	
	DP_PLL_VDD_33V*	1*	FOR 3_3V*	
ROM_SI	RAMCFG[3]*	0*		35K PD* 45K PD*
	RAMCFG[2]*	1*		
	RAMCFG[1]*	1*		
	RAMCFG[0]*	0*		
ROM_SO	FB[1]_APERTURE_SIZE*	0*	For 128MB*	30k PD*
	FB[0]_APERTURE_SIZE*	1*	For 128MB*	
	SMB_ALT_ADDR*	0*		
	VGA_DEVICE*	1*		
ROM_SCLK	PCI_DEVID_EXT[4]*	0*	For 0x11C0*	25K PD* 25K PD* 25K PD* 35K PU*
	SUB_VENDOR*	1*	Dedicated BIOS*	
	PCI_DEVID_EXT[5]*	0*	For 0x11C0*	
	PEX_PLL_EN_TERM100*	0*	ENABLED*	

BINARY PRODUCTION	MULTI_STRAP_REF0_GND
BINARY BRINGUP	NC
MULTI-LEVEL	NC 0.1k 1% TO GND









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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC2: ROM, XTAL, Straps

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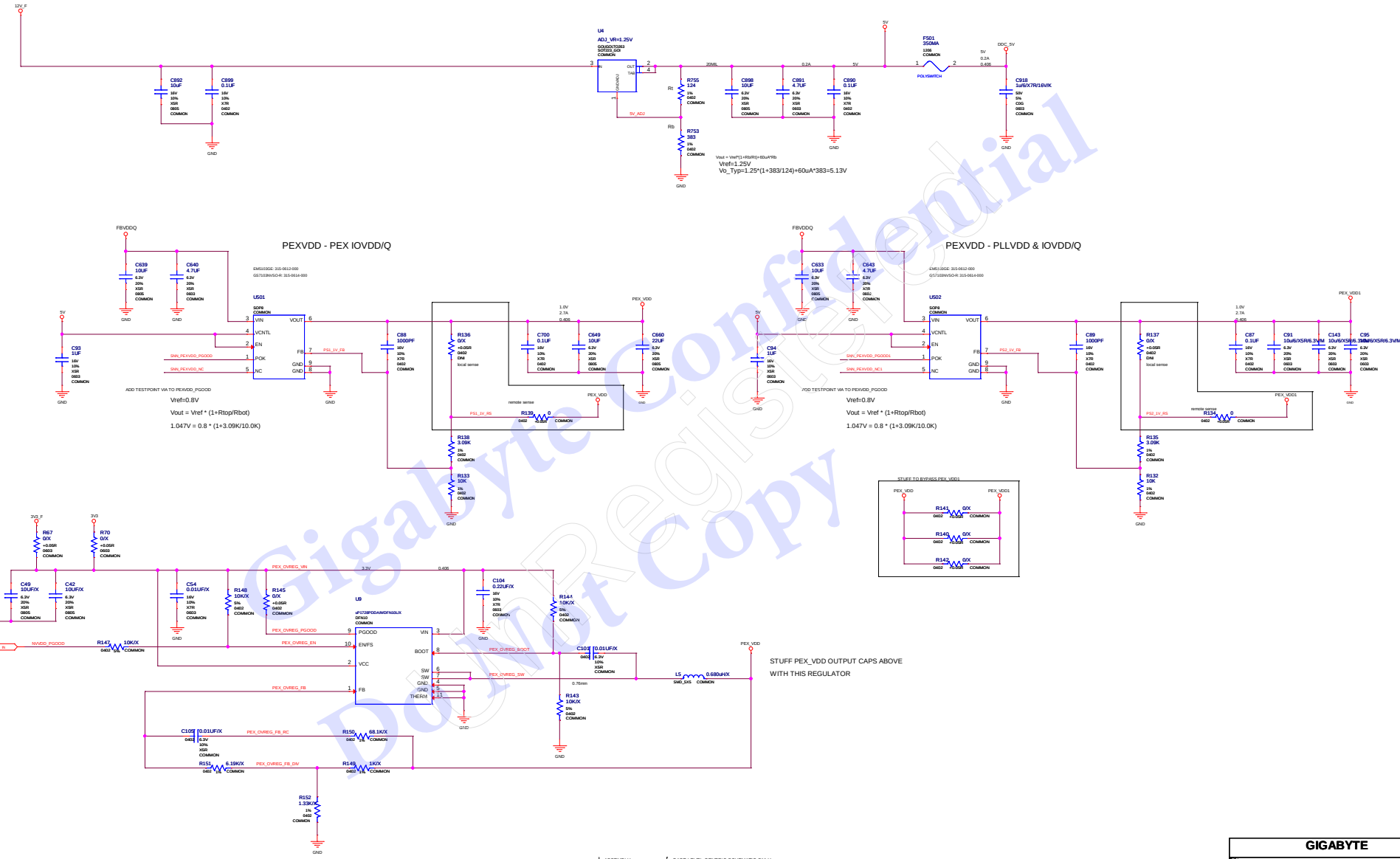
PS: 5V, PEX_VDD



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 5V, PEX_VDD

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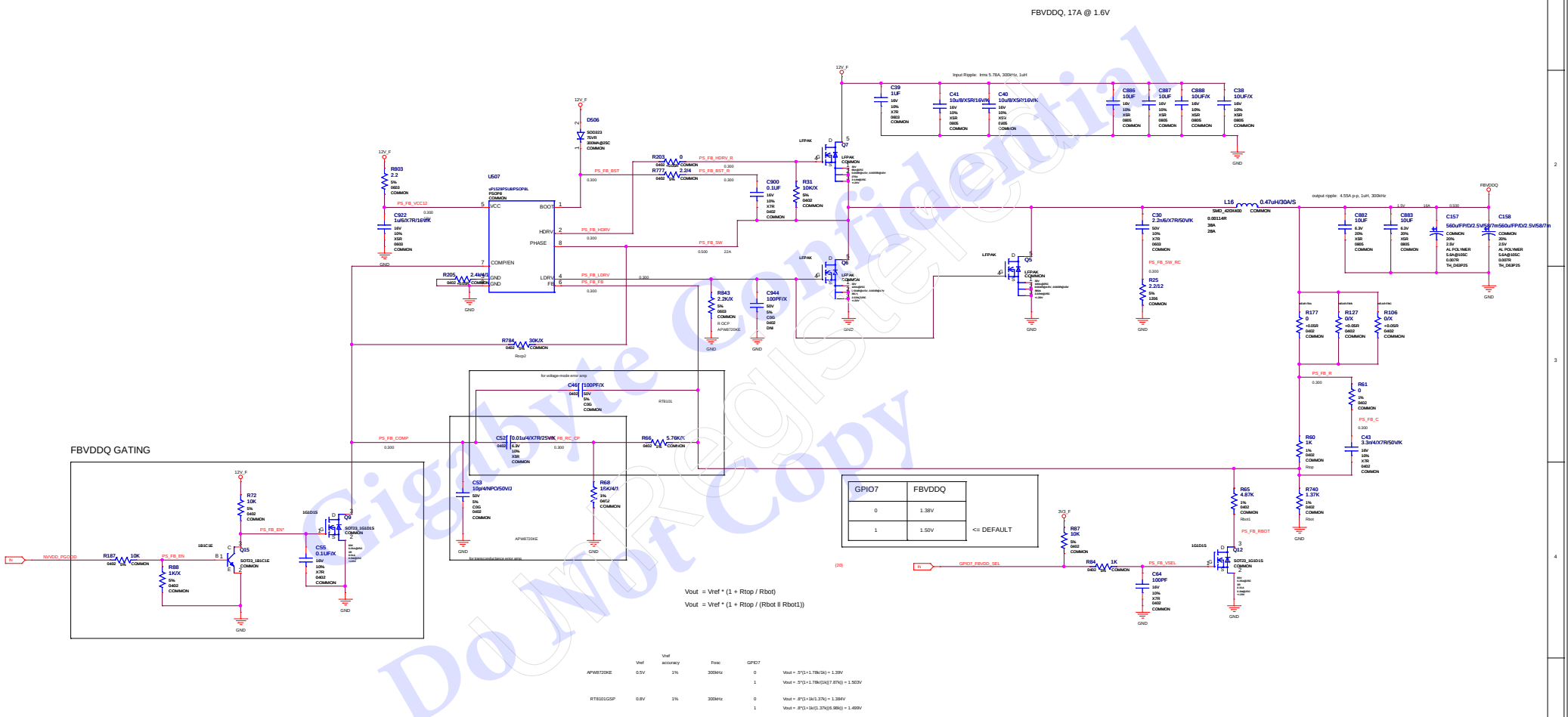
PS: FBVDDQ



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PAGE DETAIL

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PS: FBVDDQ

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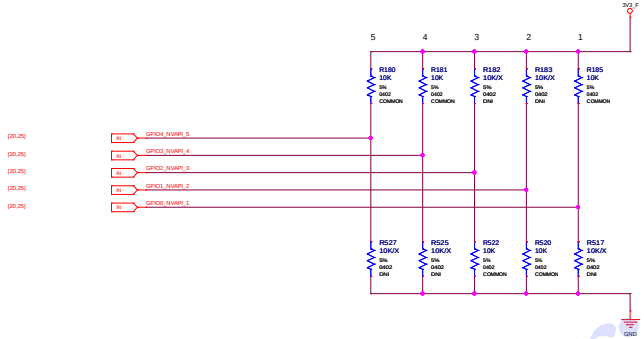
PS: NVVDD Controller, VID and PSI

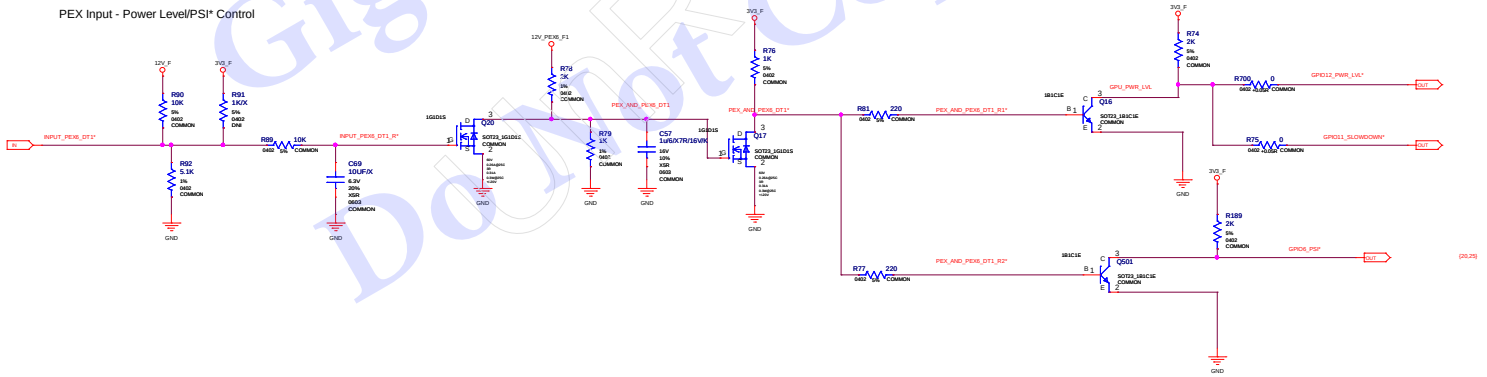
VID Table

GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V



GPIO12_PWR_LVL	GPU SPEED
0	Slow
1	Normal

PEX Input - Power Level/PSI* Control



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BASE LEVEL GENERIC SCHEMATIC ONLY
PS: NVVDD VID and PSI

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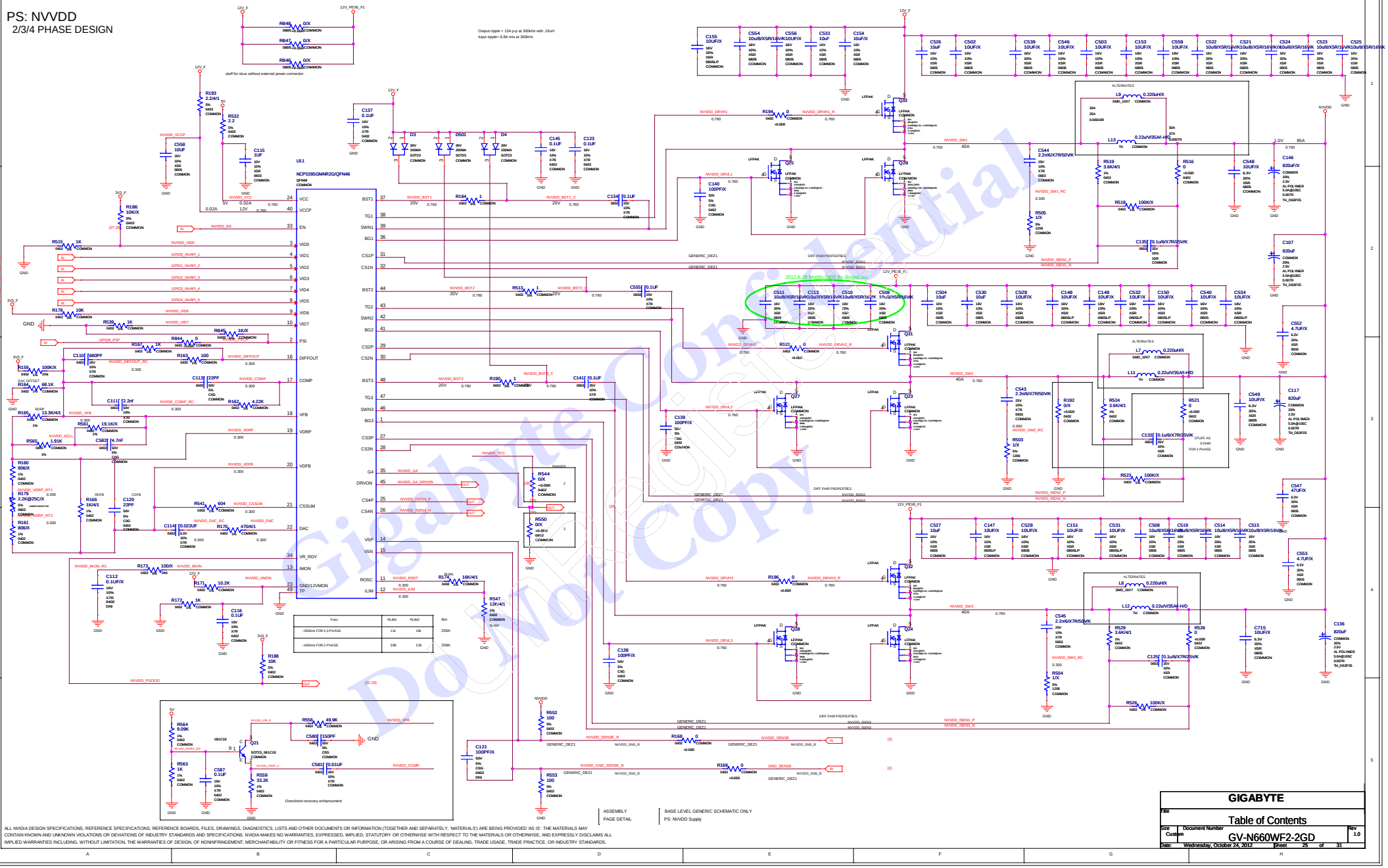
PS: NVVDD
2/3/4 PHASE DESIGN



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PS: NVDD Supply

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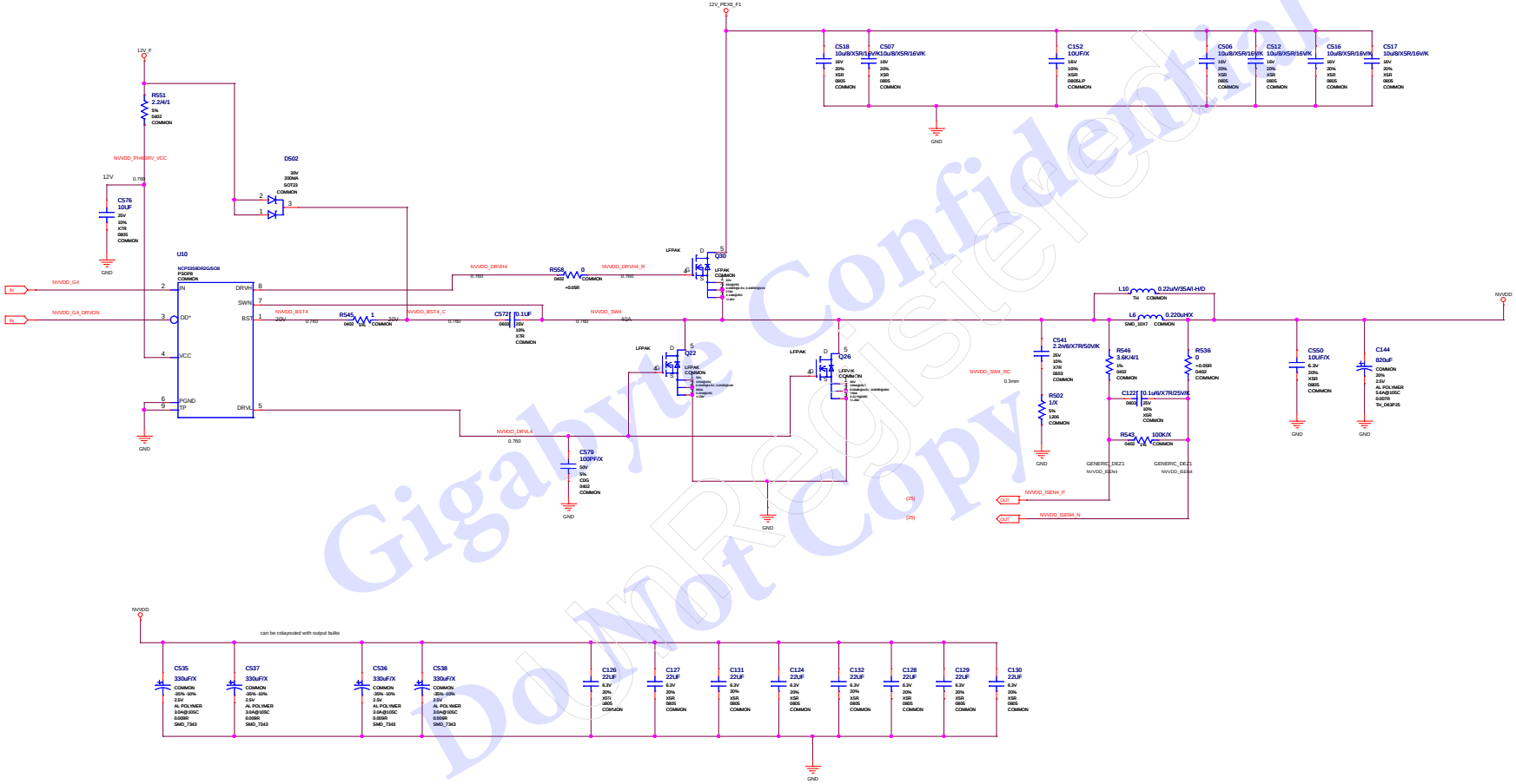

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PS: NVDD Phase4

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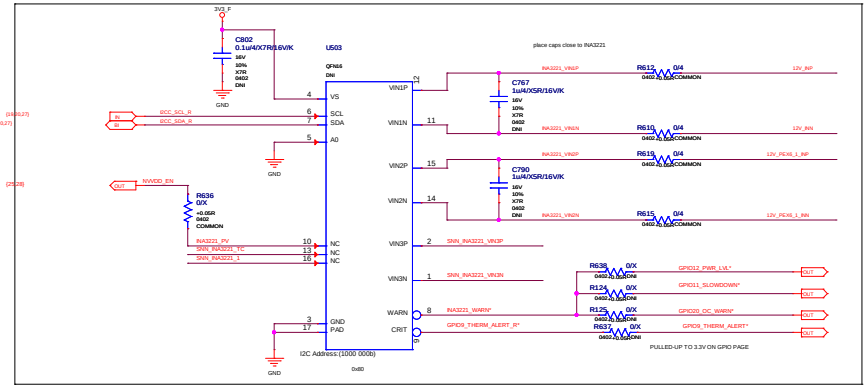
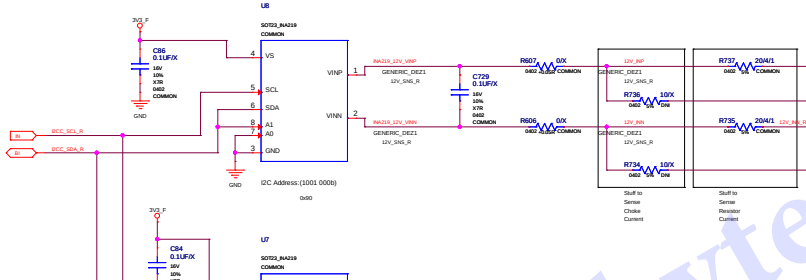
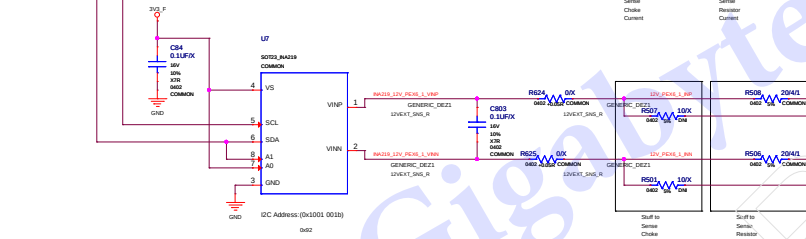
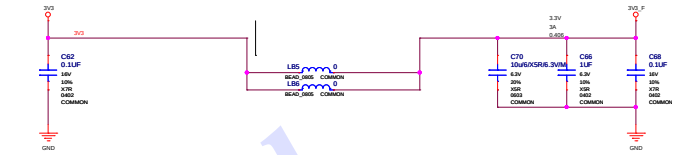
PS: Inputs, Filtering, and Monitoring



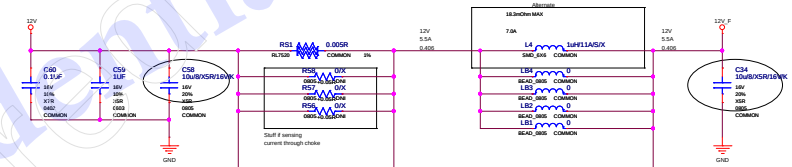




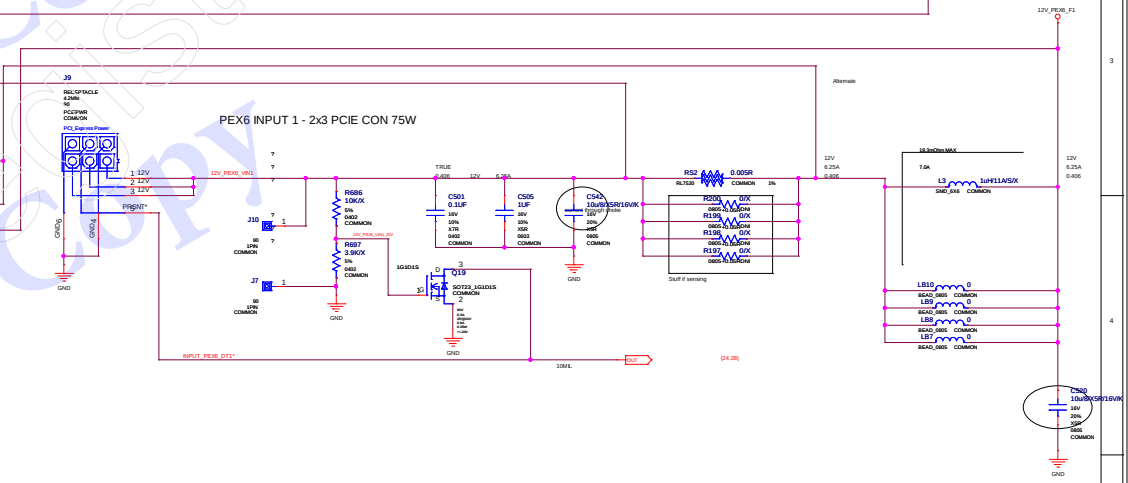
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



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PS: Inputs, Filtering, and Monitoring

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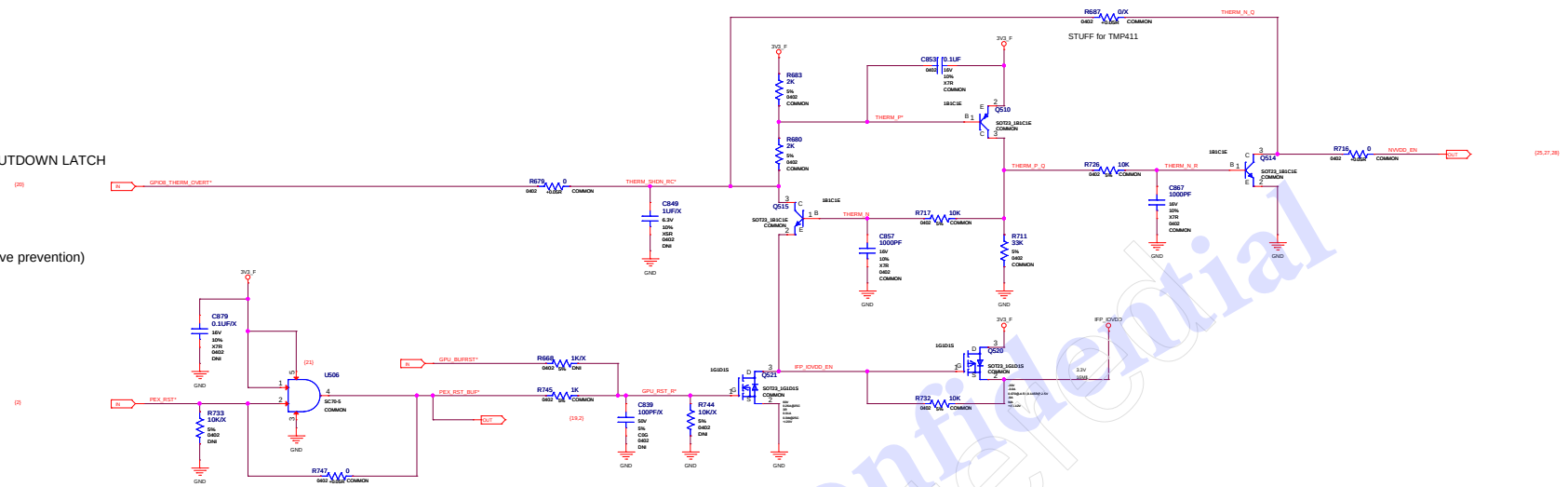
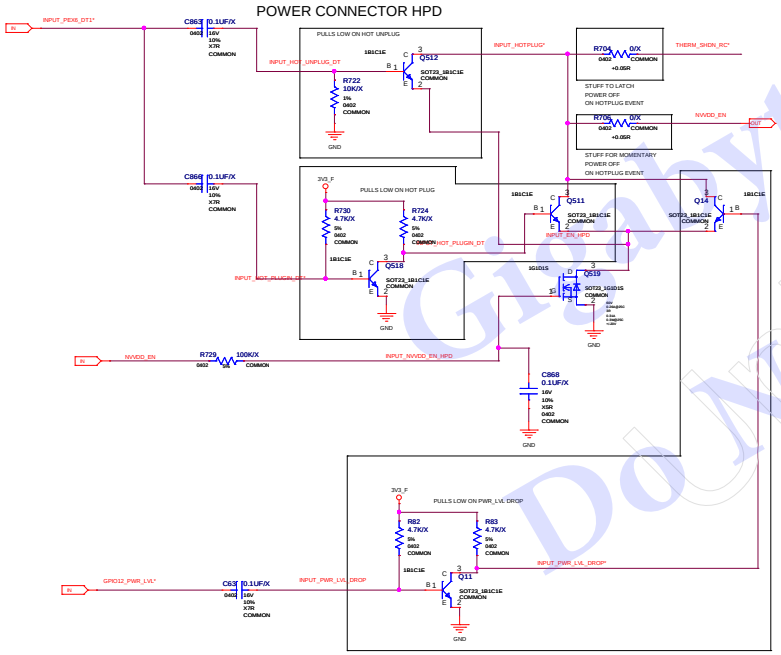
PS: Shutdown

THERM OVERT SHUTDOWN LATCH

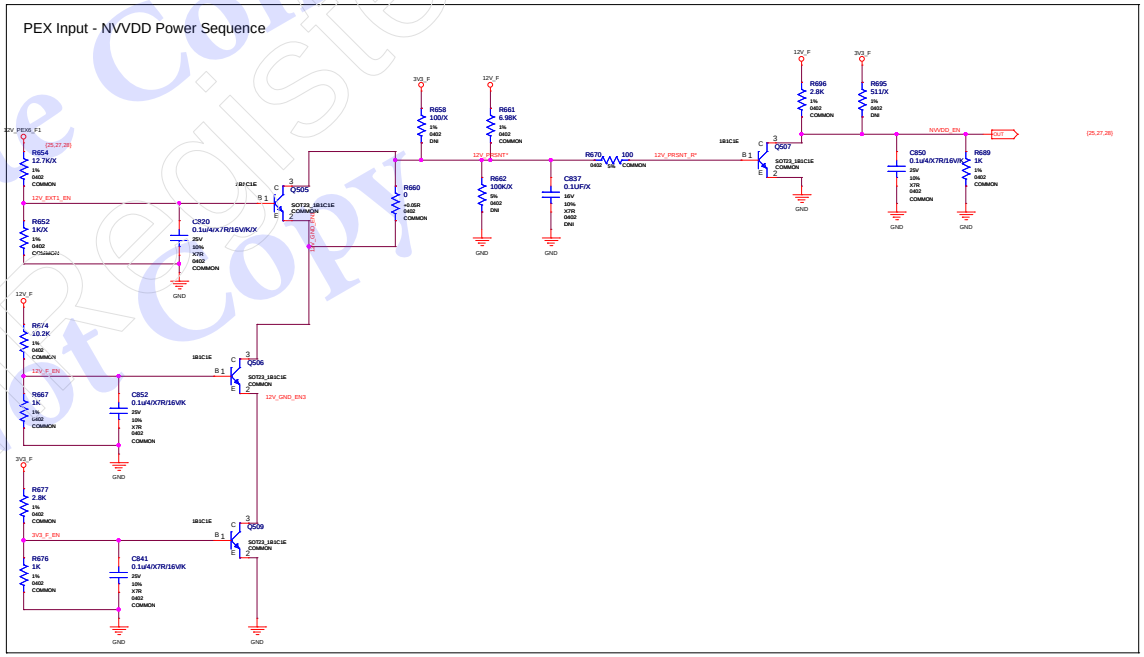
IFP_IOVDD (backdrive prevention)



POWER CONNECTOR HPD



PEX Input - NVVDD Power Sequence



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PS: Shutdown

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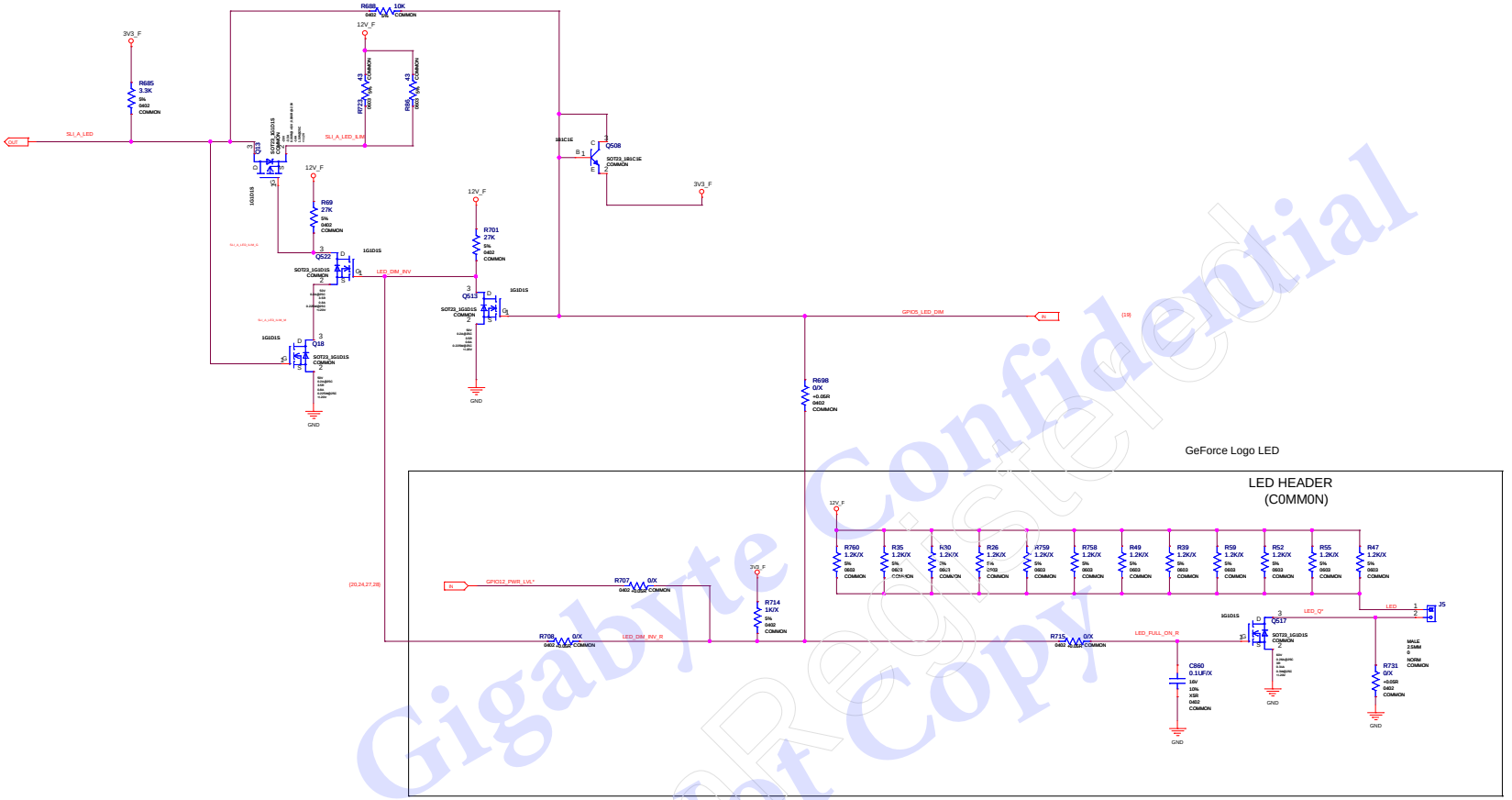
PS: Board LED



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PS: Board LED; Lighted SLI LED

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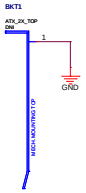
Mechanical: Bracket/Thermal Solution

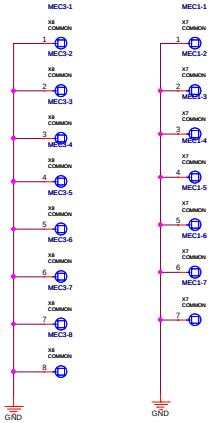
Bracket:



Bracket Screw

Hockey Stick

Mechanical Holes Symbol



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MECH: Bracket/Thermal

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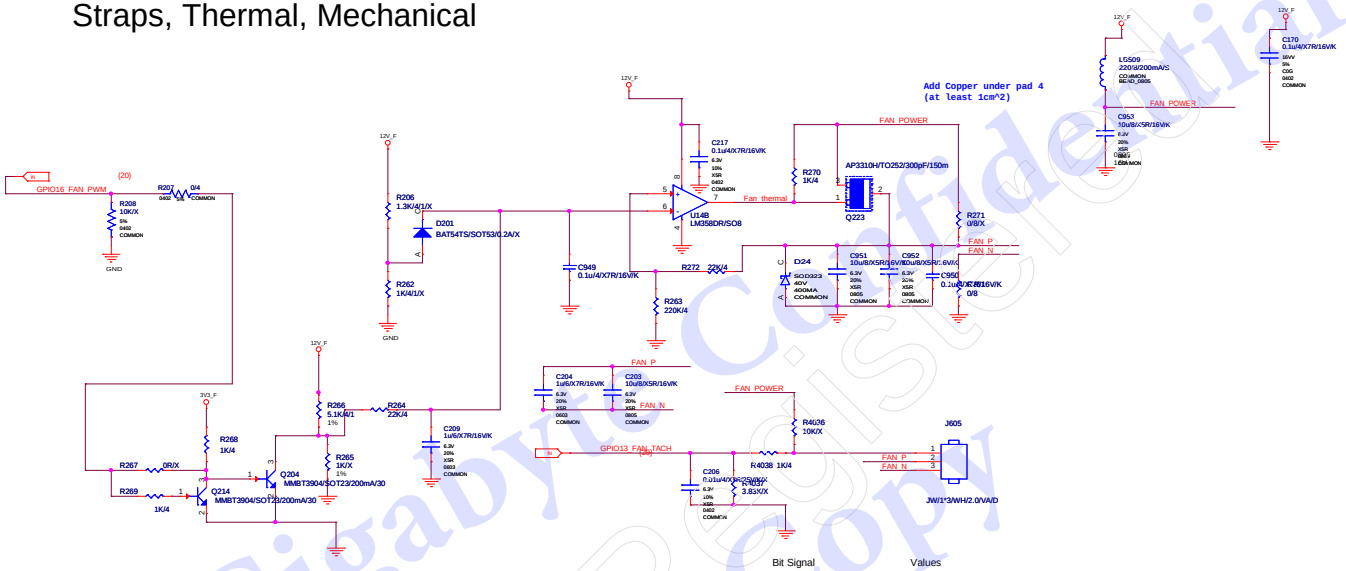
Straps, Thermal, Mechanical



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