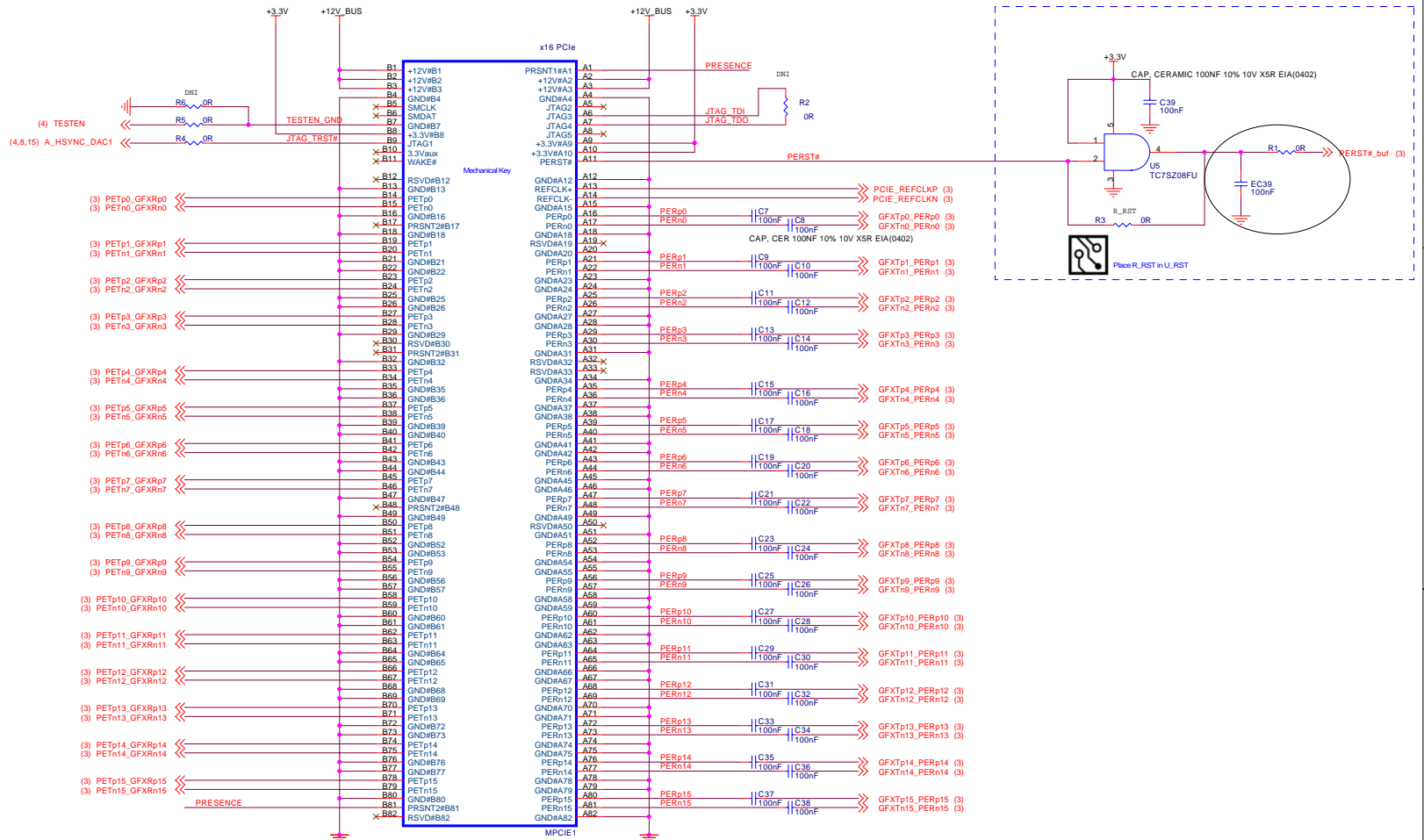
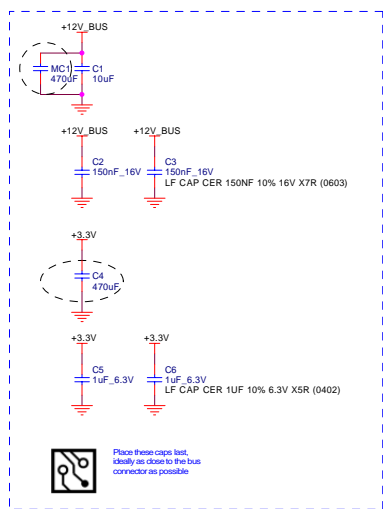
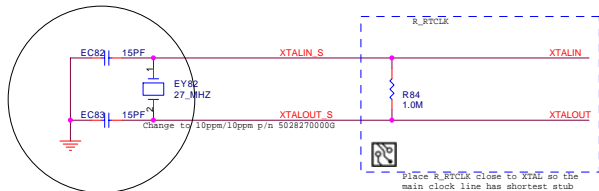
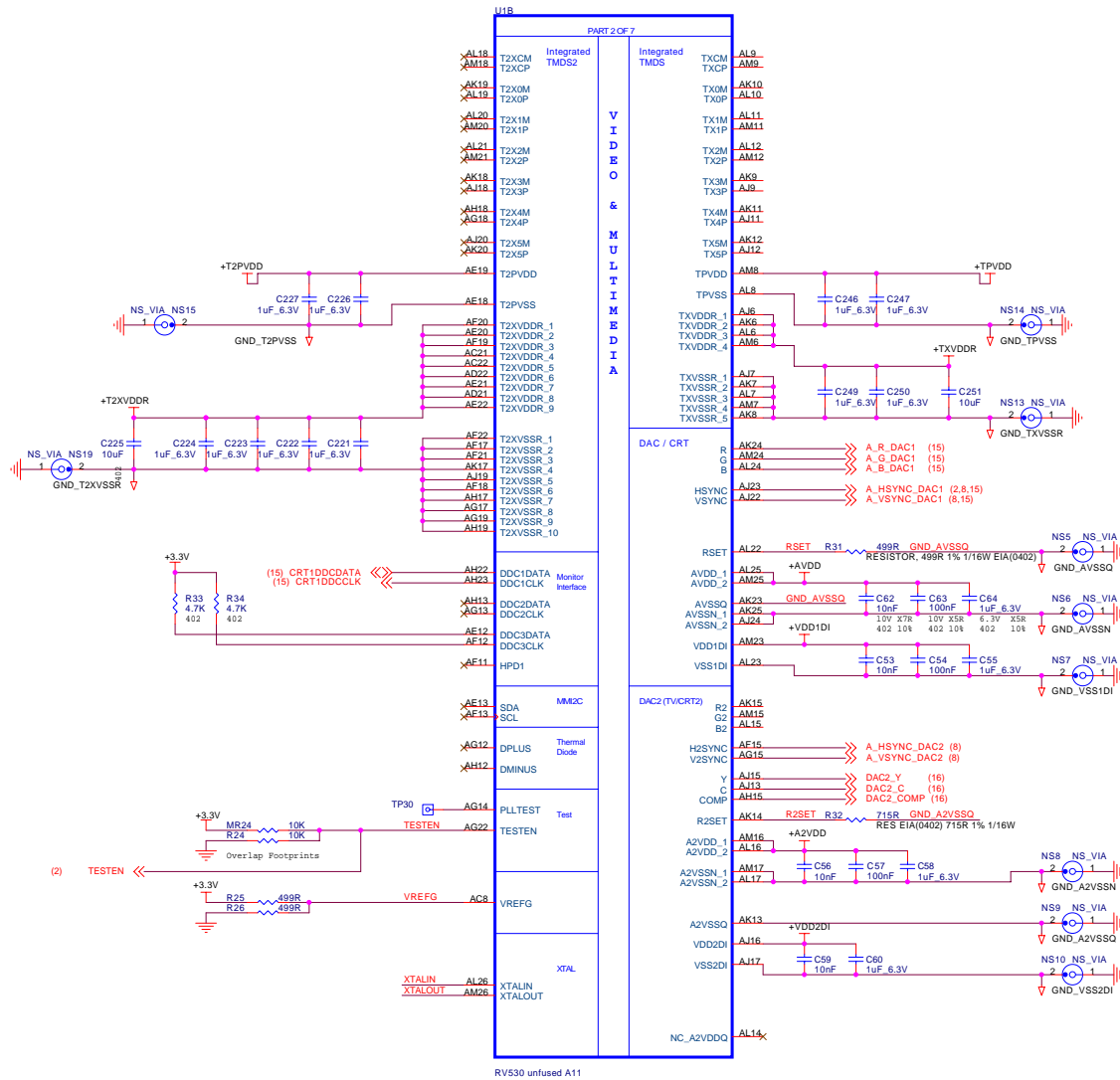
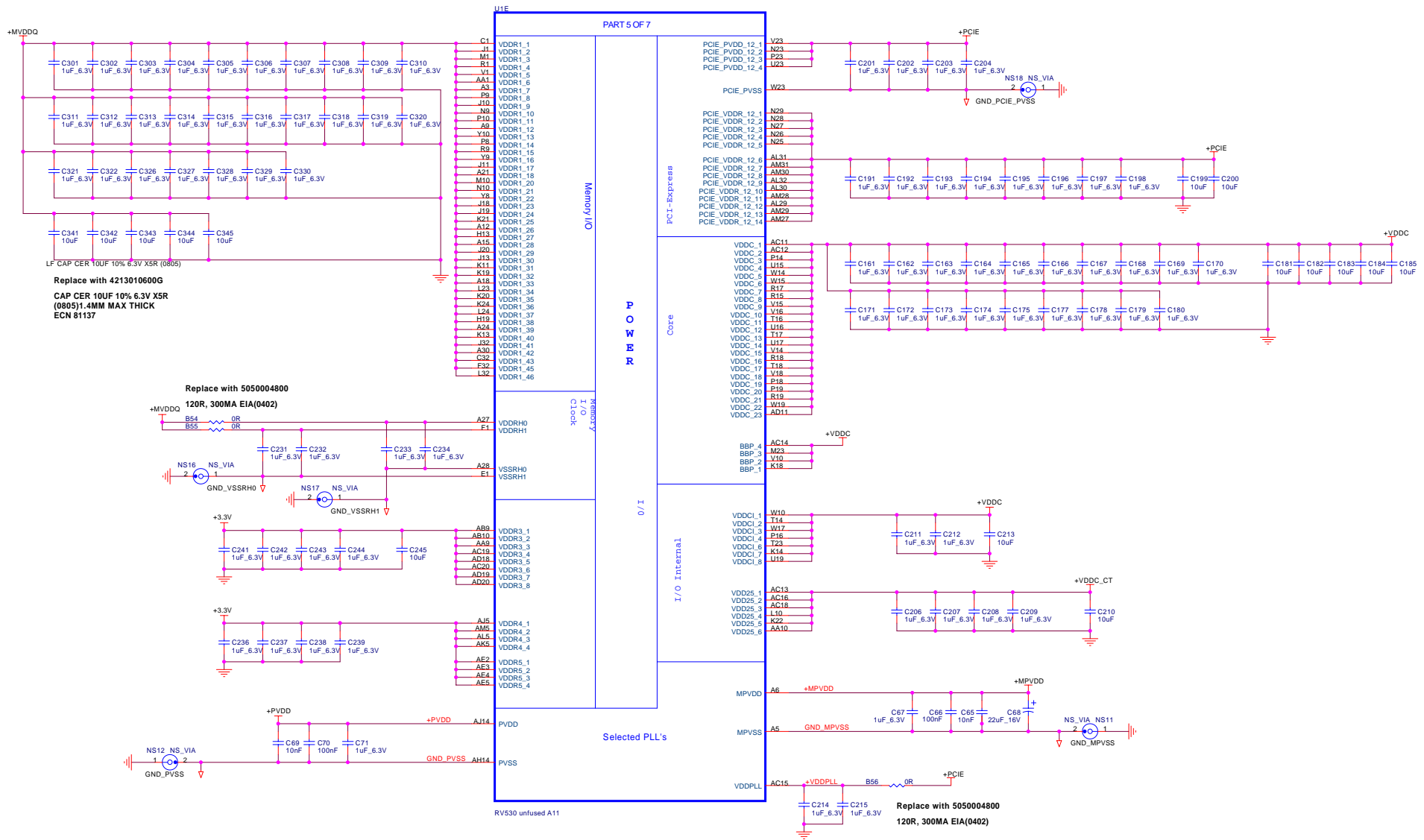


PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND





RV530 MEMORY CHANNELS A and B

Channel A

Channel B

MEMORY INTERFACE A

MEMORY INTERFACE B

RV530 unfused A11

RV530 unfused A11

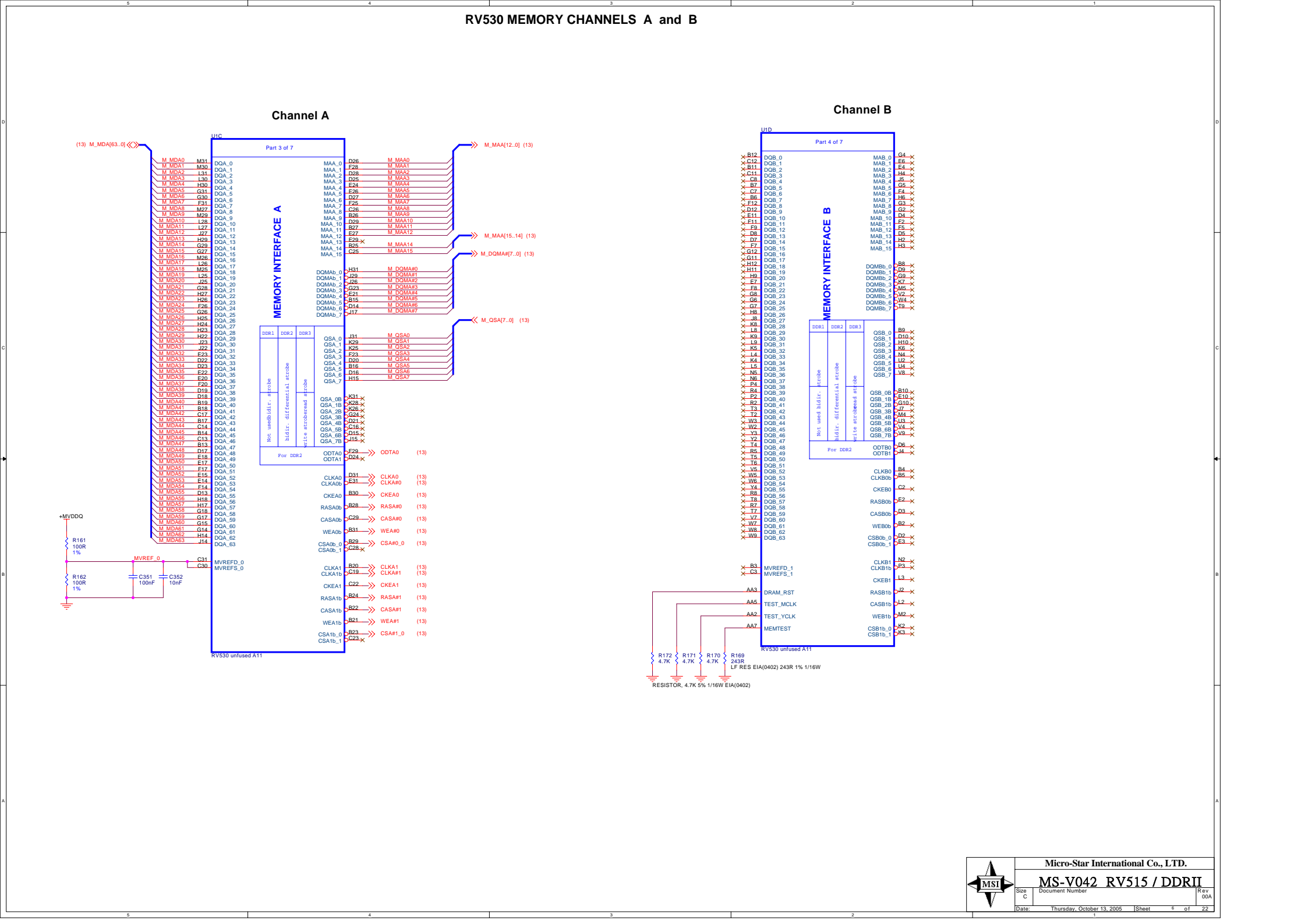
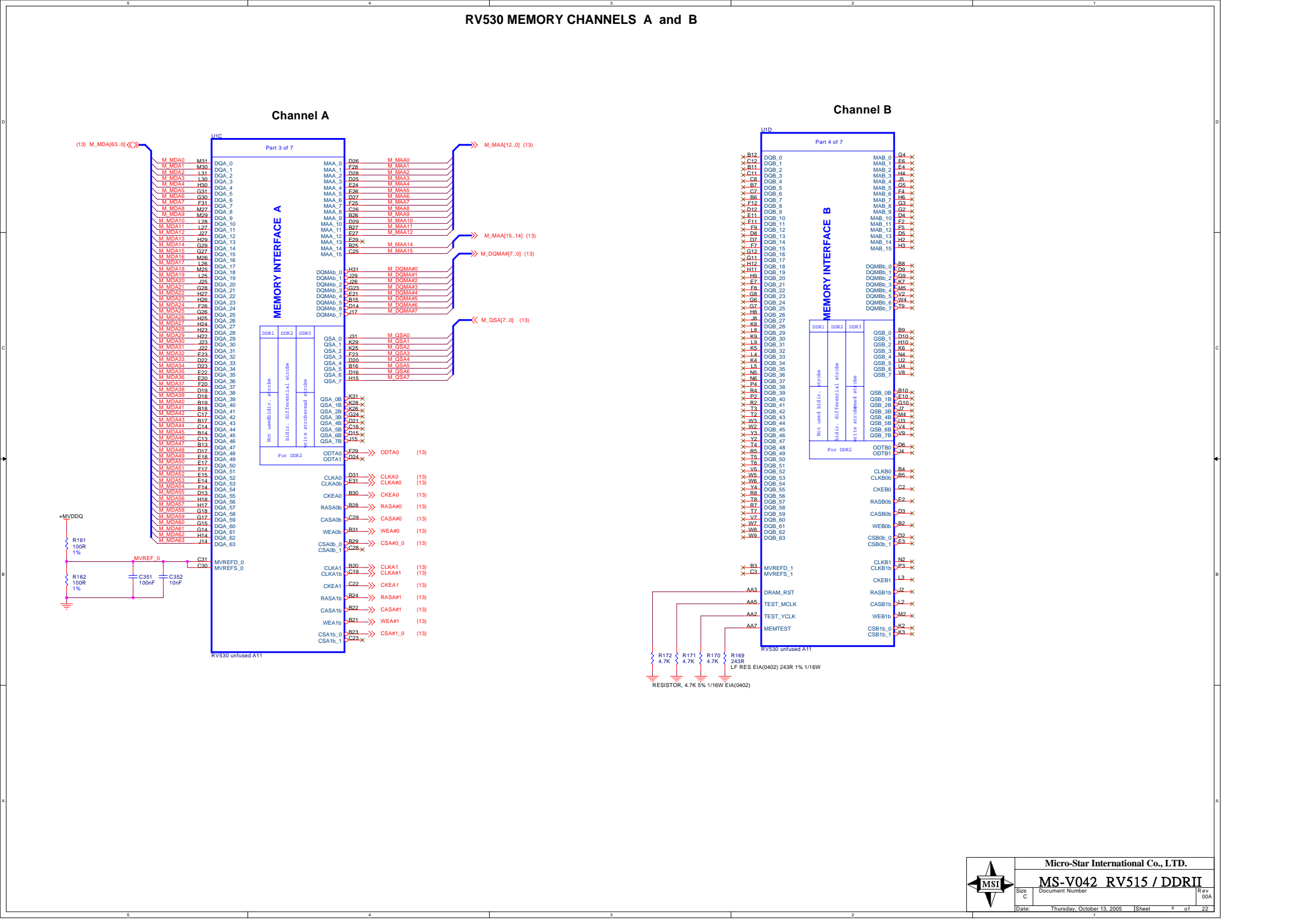
RESISTOR, 4.7K 5% 1/16W EIA(0402)

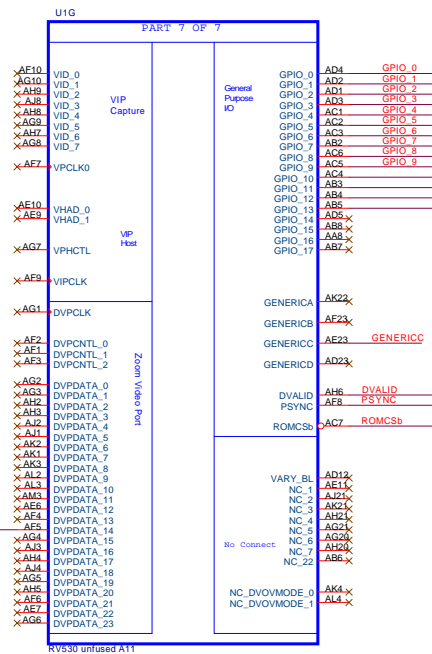
Micro-Star International Co., LTD.

MS-V042 RV515 / DDRII

Size C Document Number

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DEBUG BUS

No testpoint means the net can be accessed from a pad somewhere else

GPIO_10

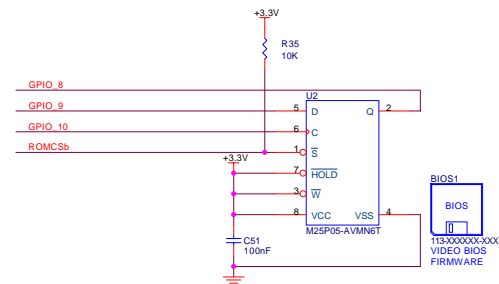
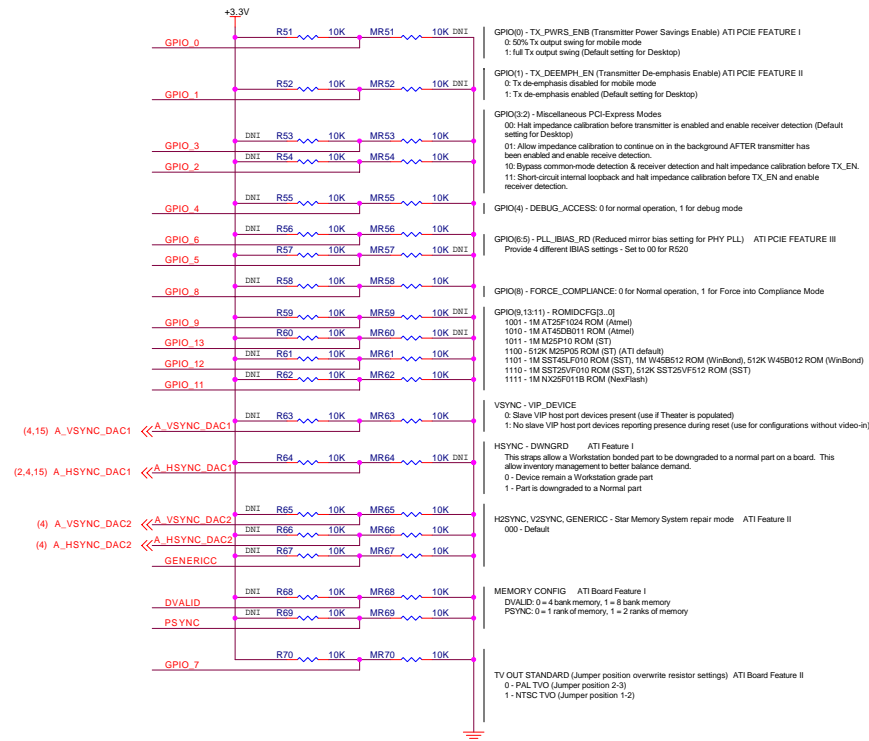
GPIO_11

GPIO_12

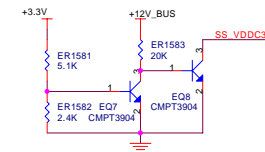
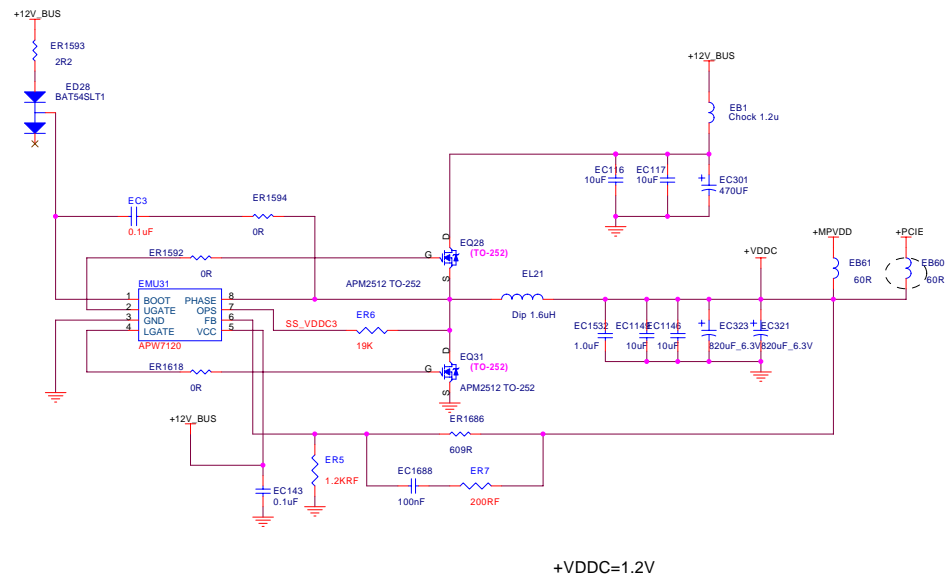
GPIO_13

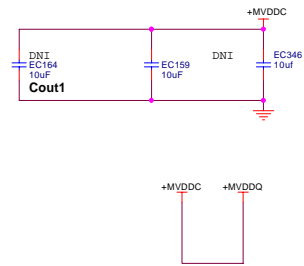
GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PALNTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11) (OUTPUT)
GPIO_14	NO	HPO_D(11) (HPO2) (INPUT)
GPIO_15	NO	VIDA/B (OUTPUT)
GPIO_16	NO	I2VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT# (INPUT) & I2VEXT_DETECT# (INPUT)

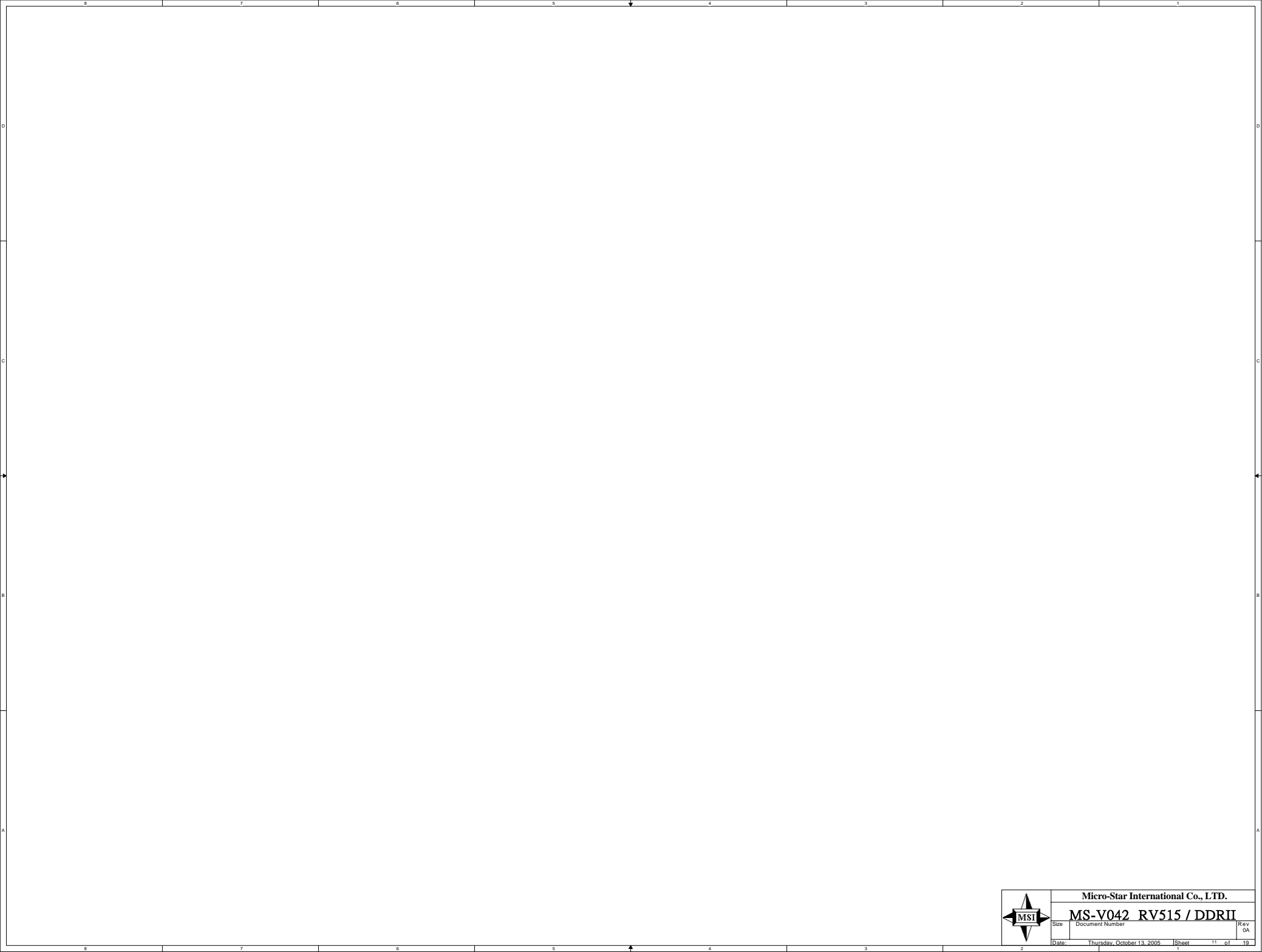
PIN BASED STRAPS



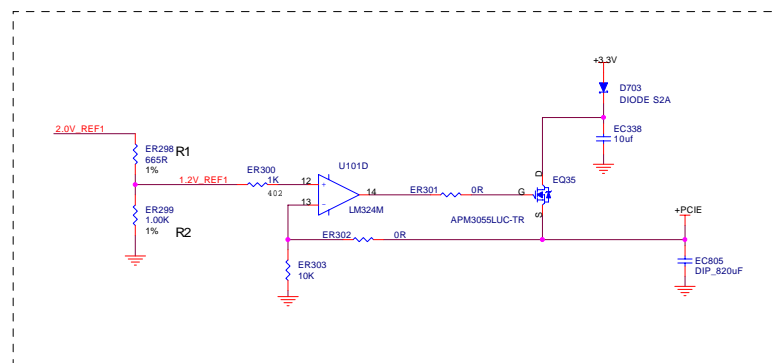
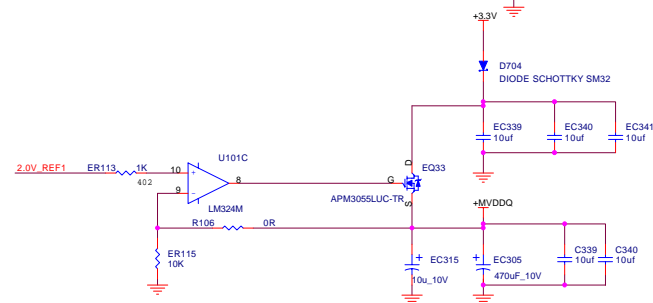
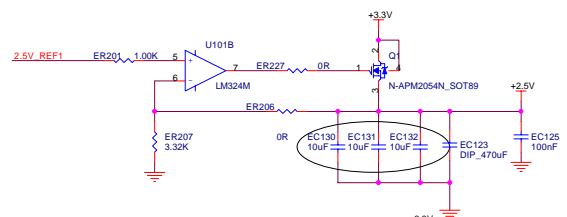
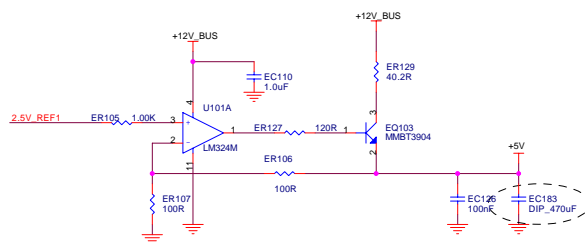
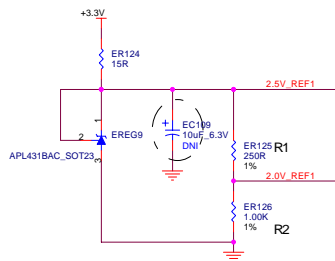
CORE REGULATOR +VDDC







Micro-Star International Co., LTD.			
MS-V042 RV515 / DDRII		Rev 0A	
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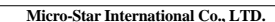


Replace with 5050004800
120R, 300MA EIA(0402)

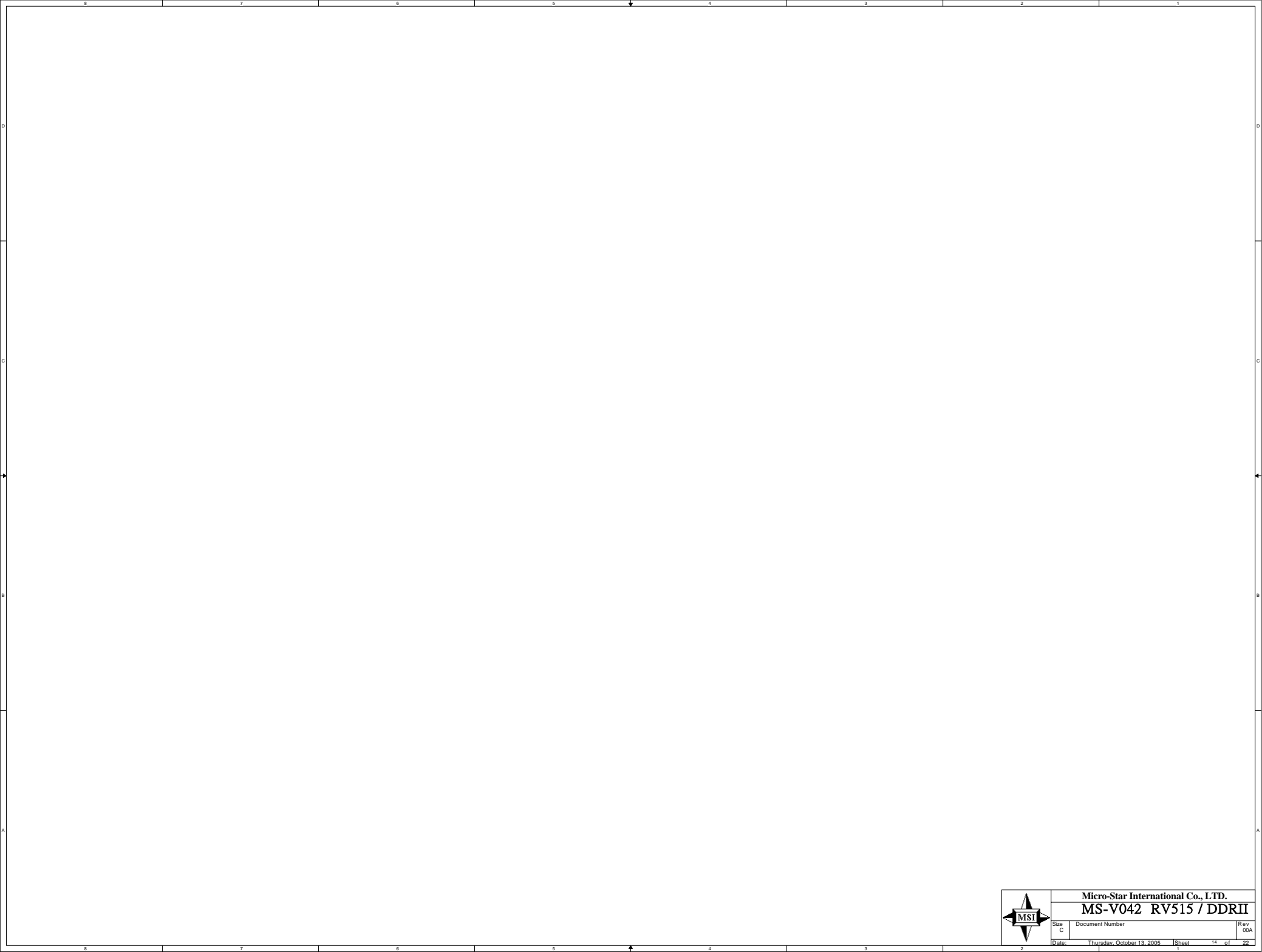


Micro-Star International Co., LTD.		
Size	Document Number	Rev
C	MS-V042 RV515 / DDRII	00A
Date:	Thursday, October 13, 2005	Sheet 12 of 22

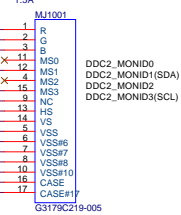
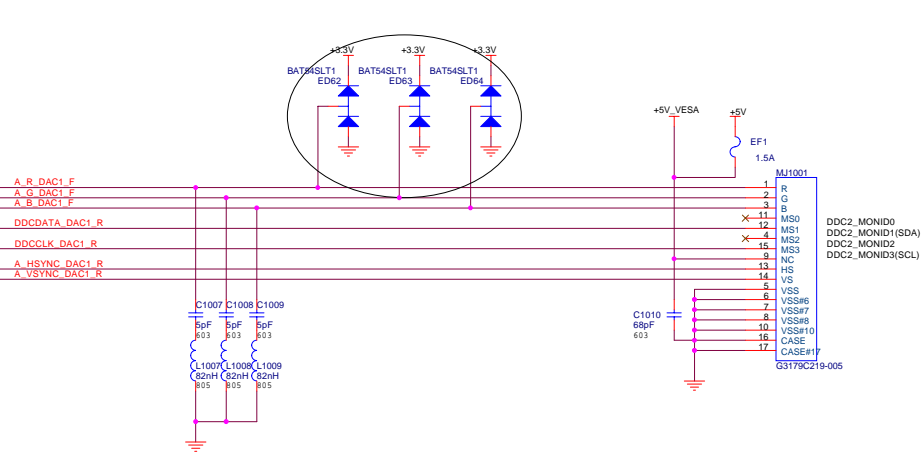
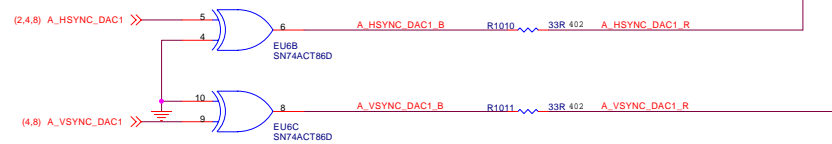
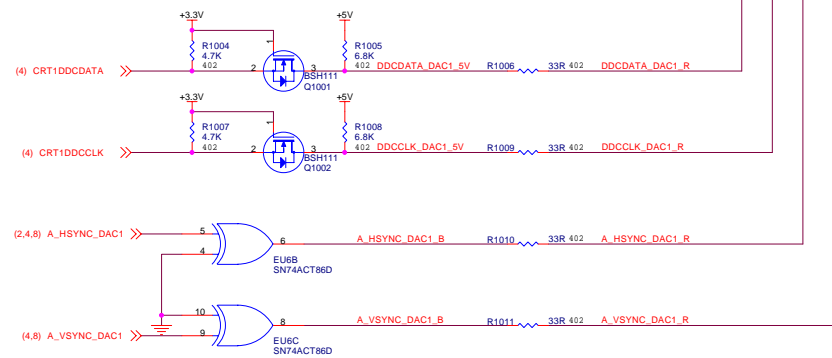
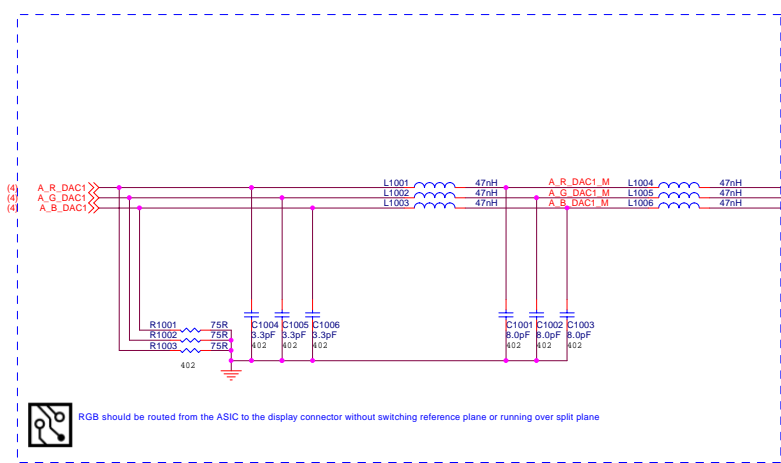
CHANNEL A: RANK 0 128MB DDR2

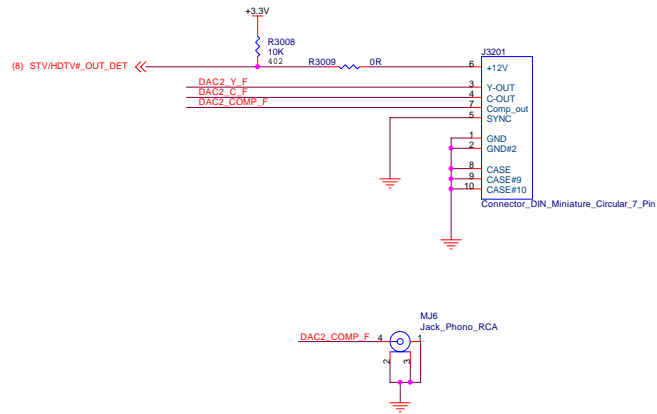
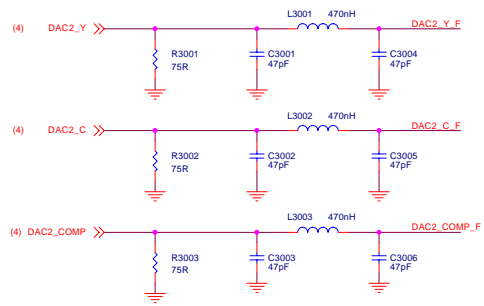
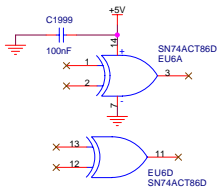


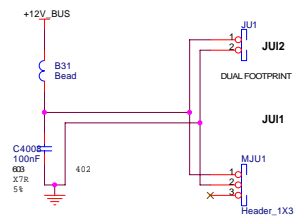
Size	Document Number	Rev
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MS-V042 RV515 / DDRII			
Size	Document Number		Rev
C			00A
Date:	Thursday, October 13, 2005	Sheet	14 of 22



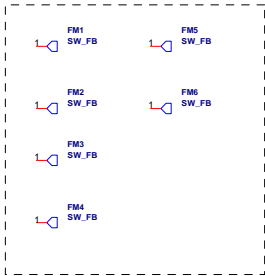
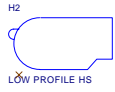
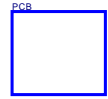
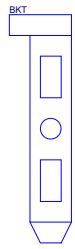




DVI/VGA SCREWS

SCREW1
SCREW
JACKSCREW
ASSY
7020000800

SCREW2
SCREW
JACKSCREW
ASSY
7020000800





Title

MS-V042 RV5xx DDR2 VGA TV LP

Schematic No.

MS-V042-10

Date:

Thursday, October 13, 2005

REVISION HISTORY

Rev 1

Sch Rev	PCB Rev	Date
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REVISION DESCRIPTION

0	0A	
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1	10	05/10/04
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1:Add Page1 12V 470uF CAP : MC1
2:Add Page1 +3.3V 470uF Cap : C4
3:Change Page1 R1 location and add EC39
4:Remove page4 DVI trace
5:Change pag12 EC805 footprint
6:Add Page12 +2.5V 10U Cap, EC130,EC131,EC132
7:Add Page12 PCIE PWR Solution
8:Change page12 EC123 footprint
9:Remove Page15 DVI function
10:Change Page15 CRT1 MJ1001 footprint