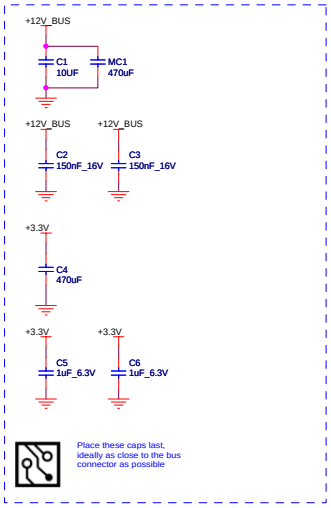
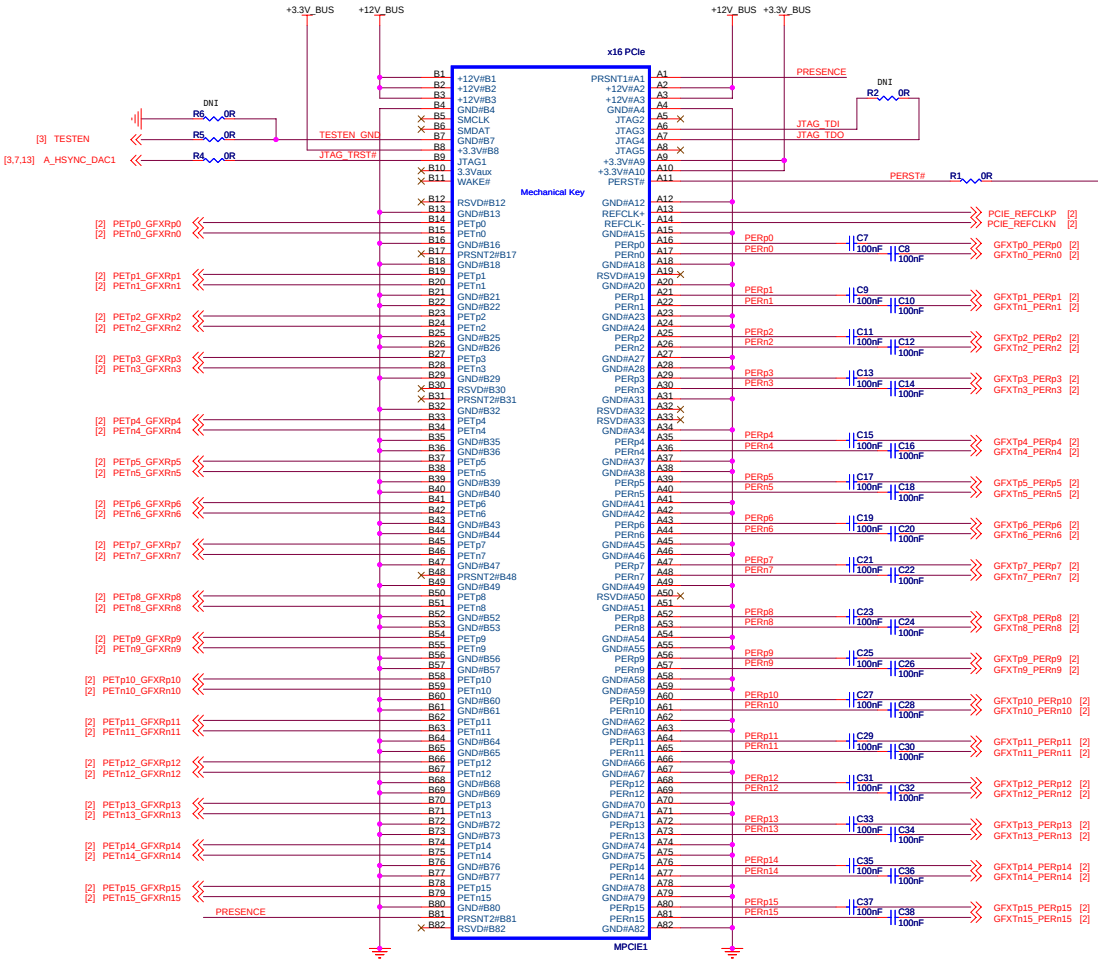
PCI-EXPRESS EDGE CONNECTOR





SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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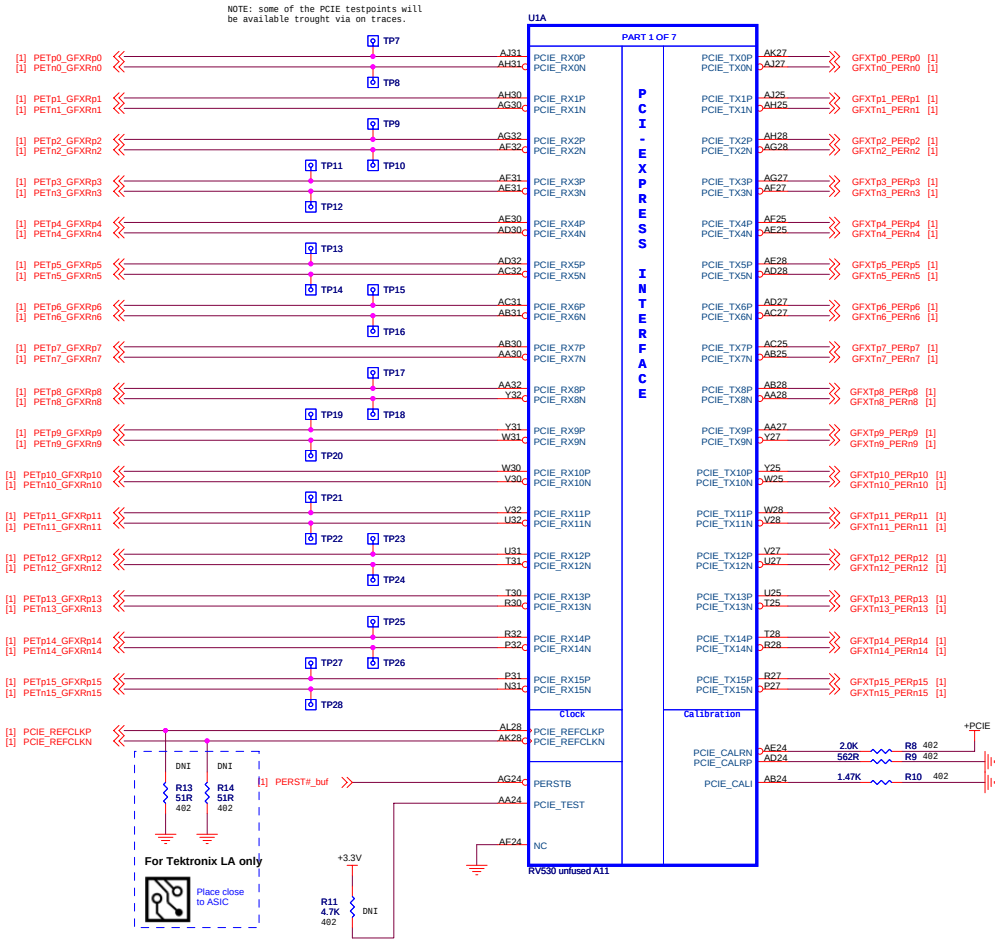

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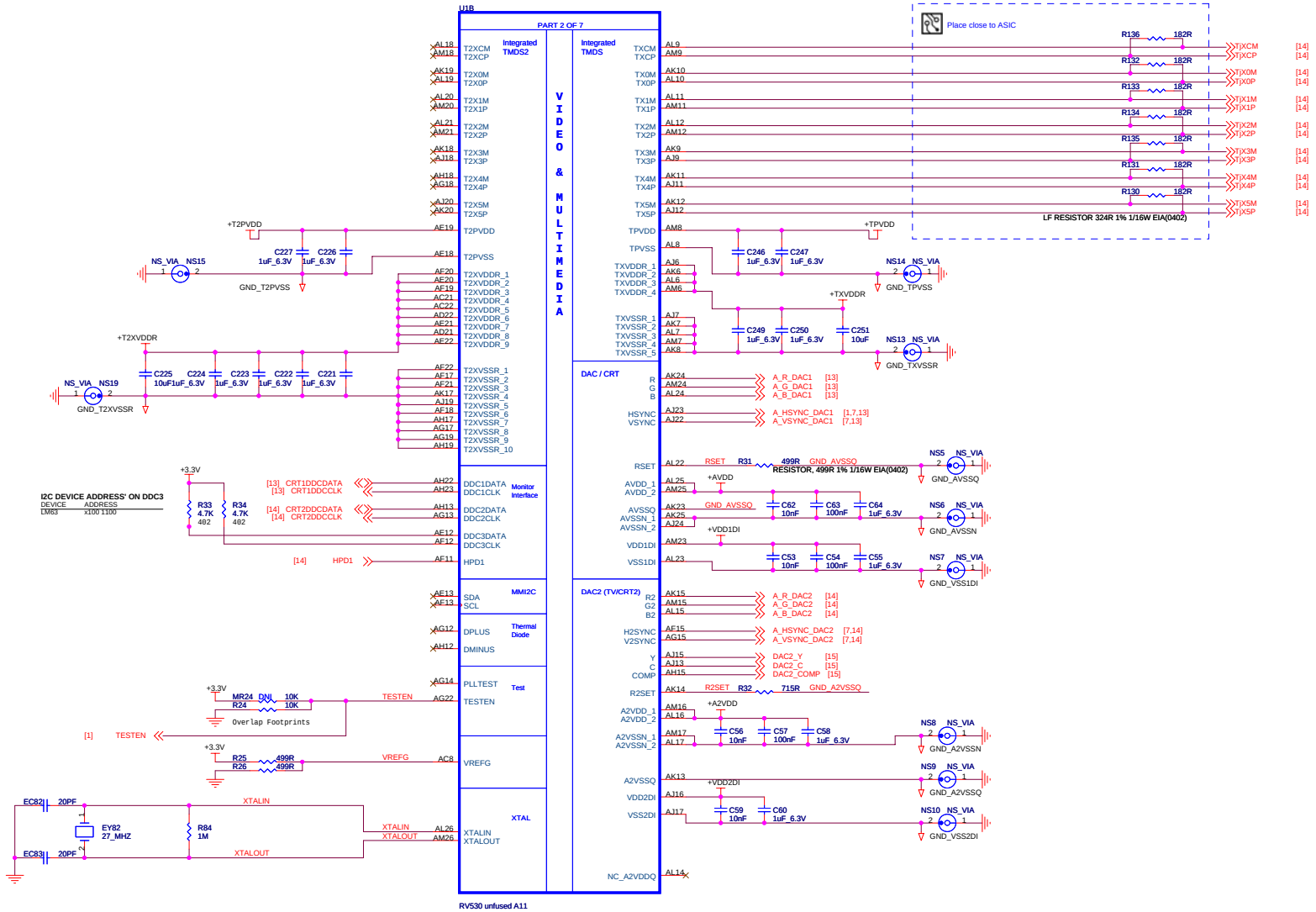

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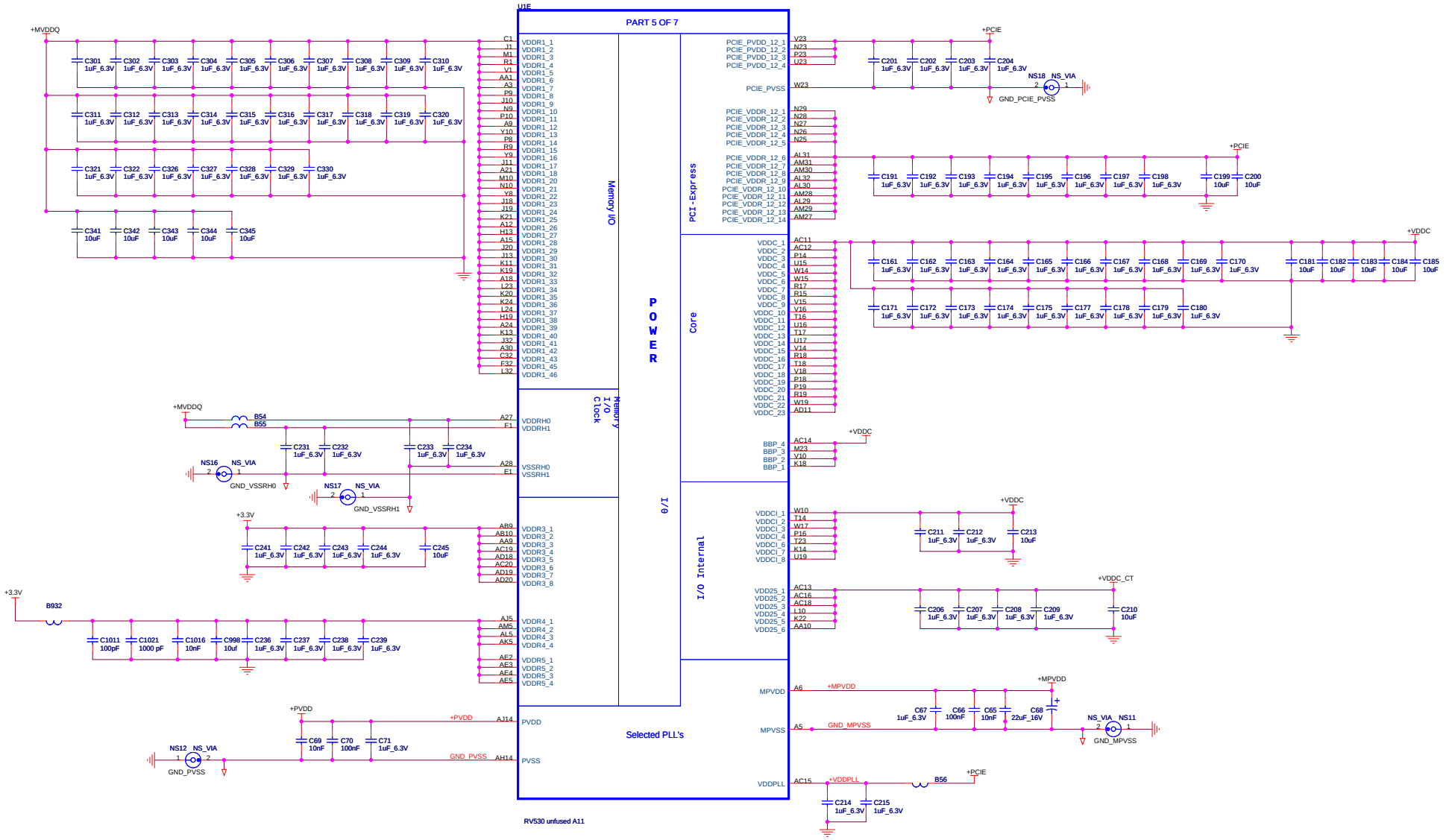

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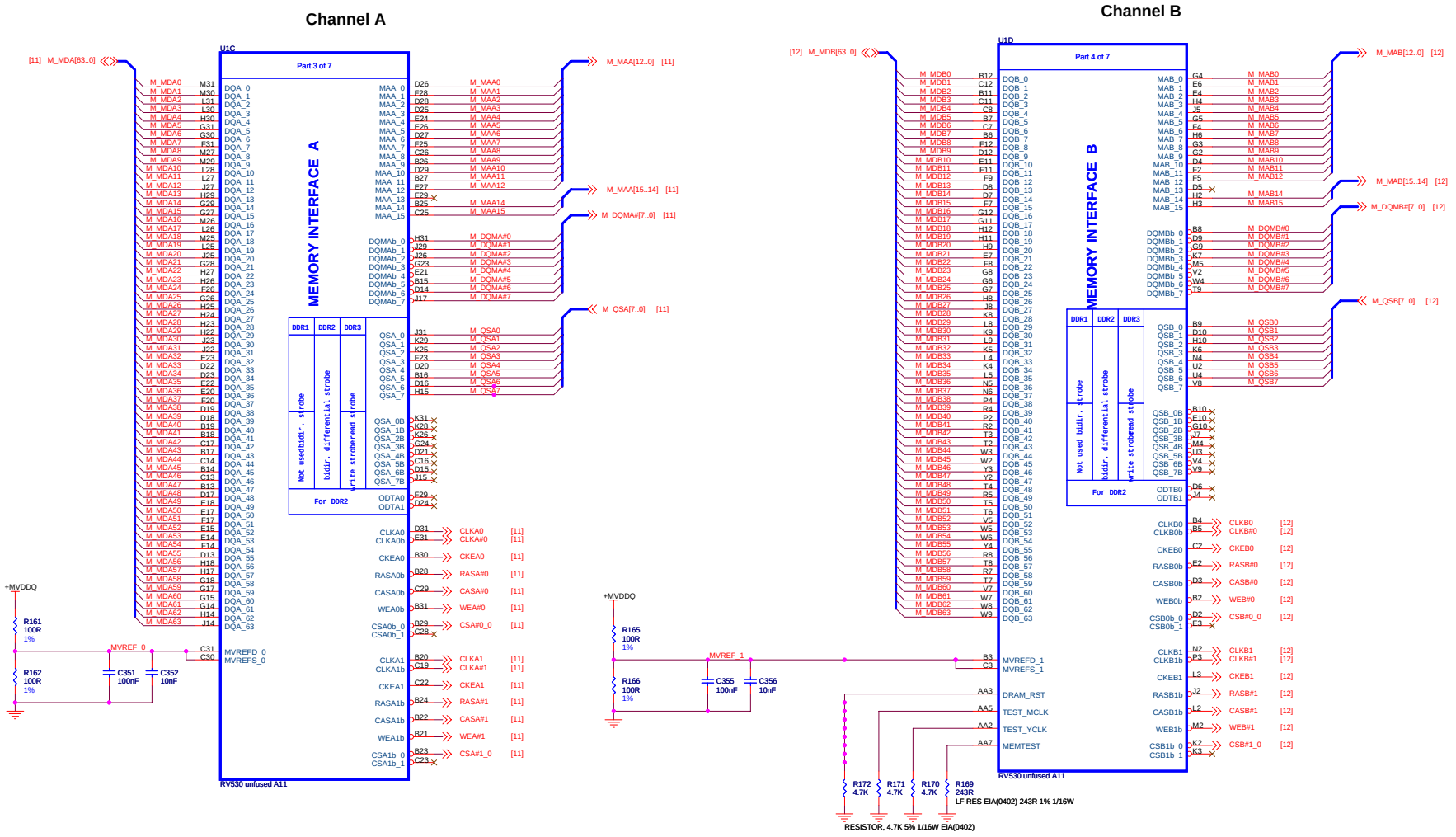
RV530 MEMORY CHANNELS A and B



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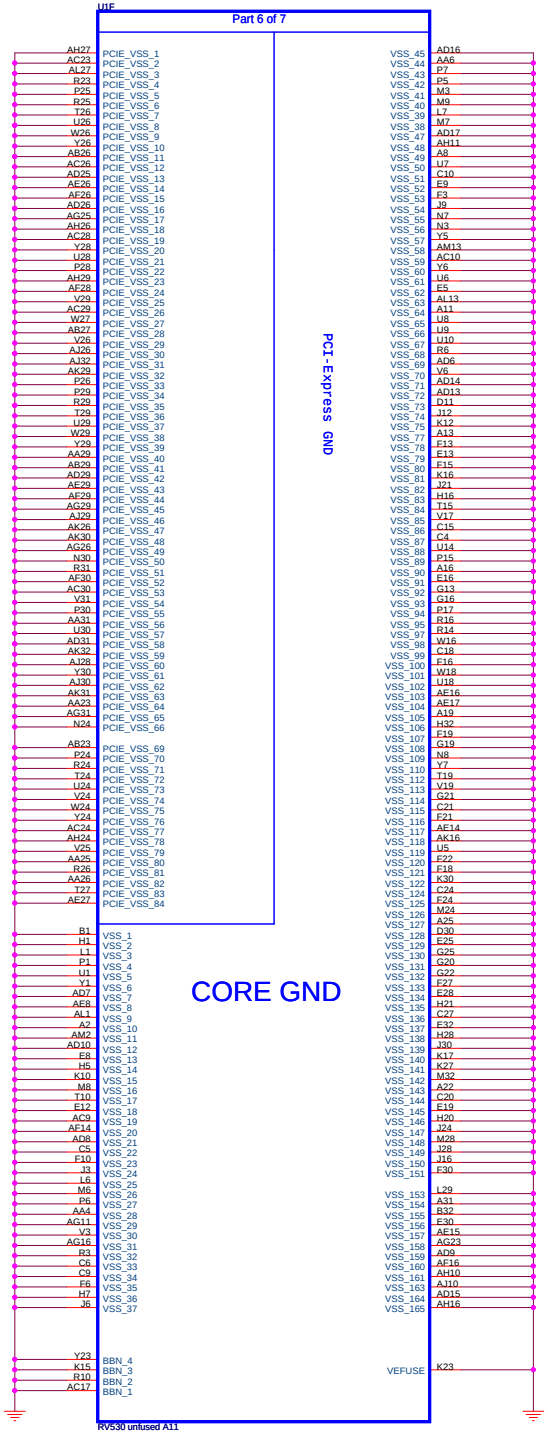

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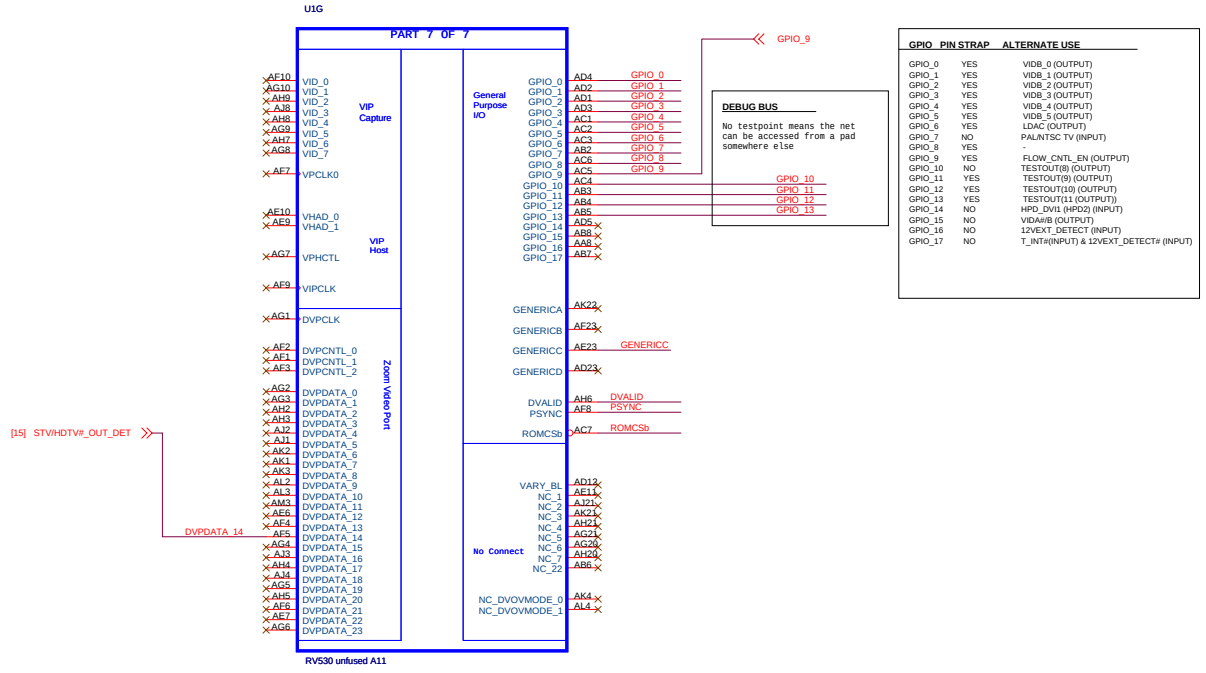
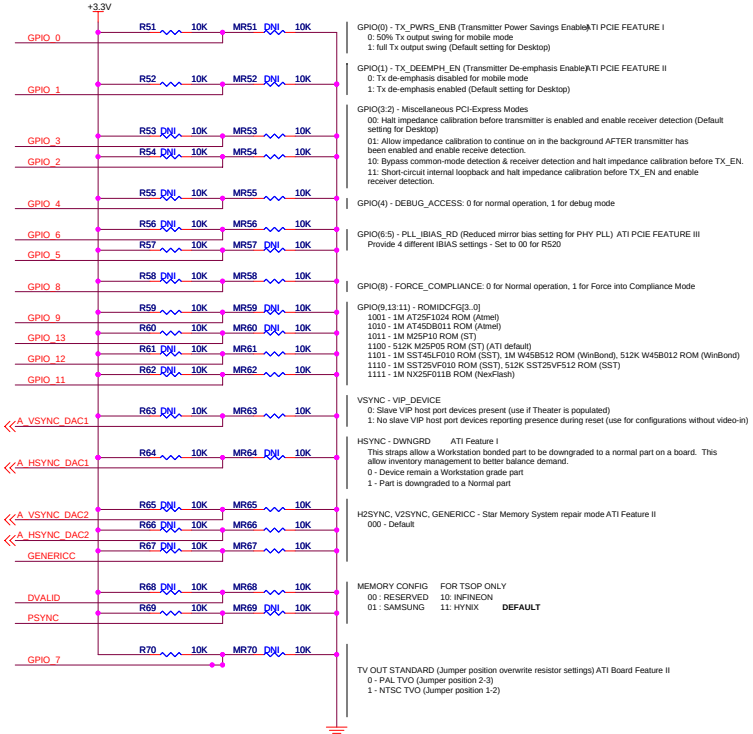


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDAKIB (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

PIN BASED STRAPS



GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - Miscellaneous PCI-Express Modes
00: Halt impedance calibration before transmitter is enabled and enable receiver detection (Default setting for Desktop)
01: Allow impedance calibration to continue on in the background AFTER transmitter has been enabled and enable receive detection.
10: Bypass common-mode detection & receiver detection and halt impedance calibration before TX_EN.
11: Short-circuit internal loopback and halt impedance calibration before TX_EN and enable receiver detection.

GPIO(4) - DEBUG_ACCESS: 0 for normal operation, 1 for debug mode

GPIO(6:5) - PLL_IBIAS_RD (Reduced mirror bias setting for PHY PLL) ATI PCIE FEATURE III
Provide 4 different IBIAS settings - Set to 00 for R520

GPIO(8) - FORCE_COMPLIANCE: 0 for Normal operation, 1 for Force into Compliance Mode

GPIO(9,13:11) - ROMIDCFG[3..0]
1001 - 1M AT25F1024 ROM (Atmel)
1010 - 1M AT45DB011 ROM (Atmel)
1011 - 1M M25P10 ROM (ST)
1100 - 512K M25P05 ROM (ST) (ATI default)
1101 - 1M SST45LF010 ROM (SST), 1M W45B512 ROM (WinBond), 512K W45B012 ROM (WinBond)
1110 - 1M SST25VF010 ROM (SST), 512K SST25VF512 ROM (SST)
1111 - 1M NX25F011B ROM (NexFlash)

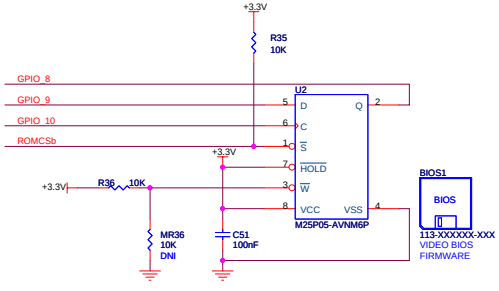
VSYNC - VIP_DEVICE
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - DWNGRD ATI Feature I
This straps allow a Workstation bonded part to be downgraded to a normal part on a board. This allow inventory management to better balance demand.
0 - Device remain a Workstation grade part
1 - Part is downgraded to a Normal part

H2SYNC, V2SYNC, GENERICC - Star Memory System repair mode ATI Feature II
000 - Default

MEMORY CONFIG FOR TSOP ONLY
00 : RESERVED 10: INFINEON
01 : SAMSUNG 11: HYNIX **DEFAULT**

TV OUT STANDARD (Jumper position overwrite resistor settings) ATI Board Feature II
0 - PAL TVO (Jumper position 2-3)
1 - NTSC TVO (Jumper position 1-2)



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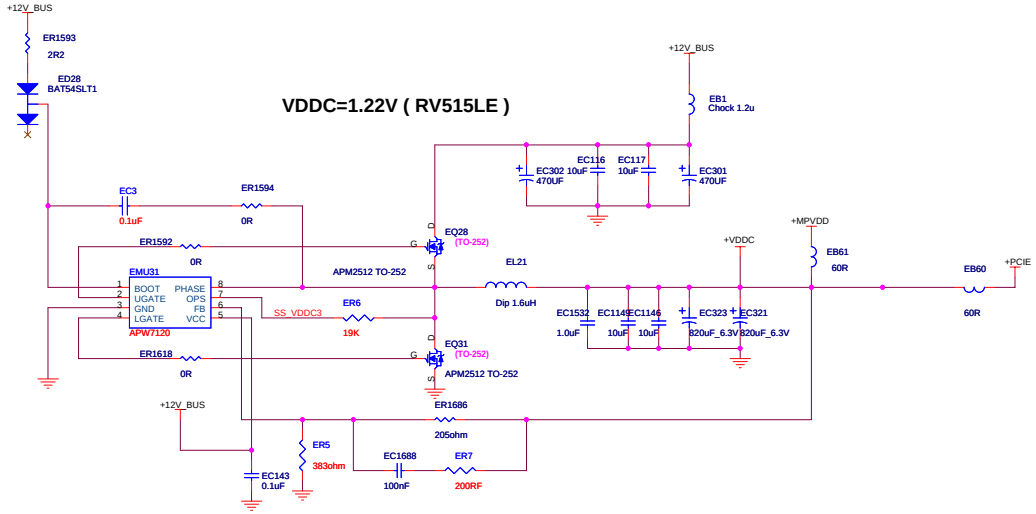
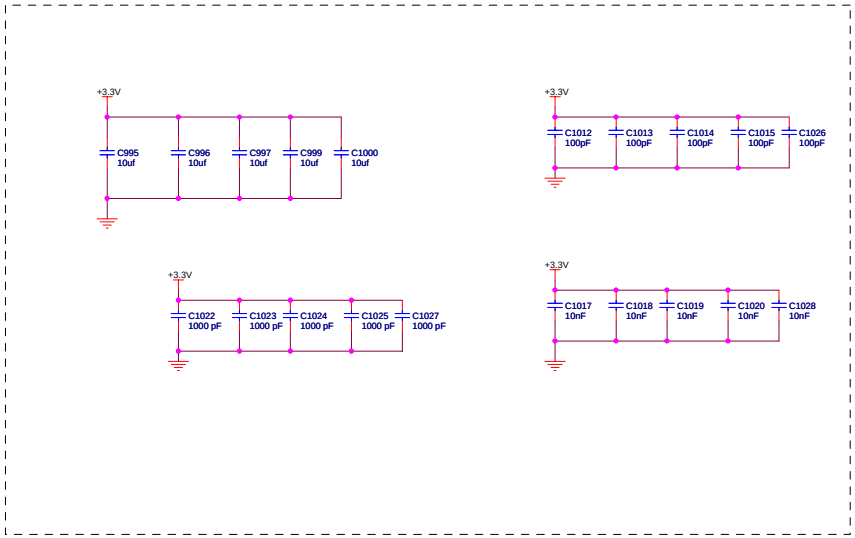
CORE REGULATOR +VDDC



VDDC=0.8 * [1 + (ER1686 / ER5)]



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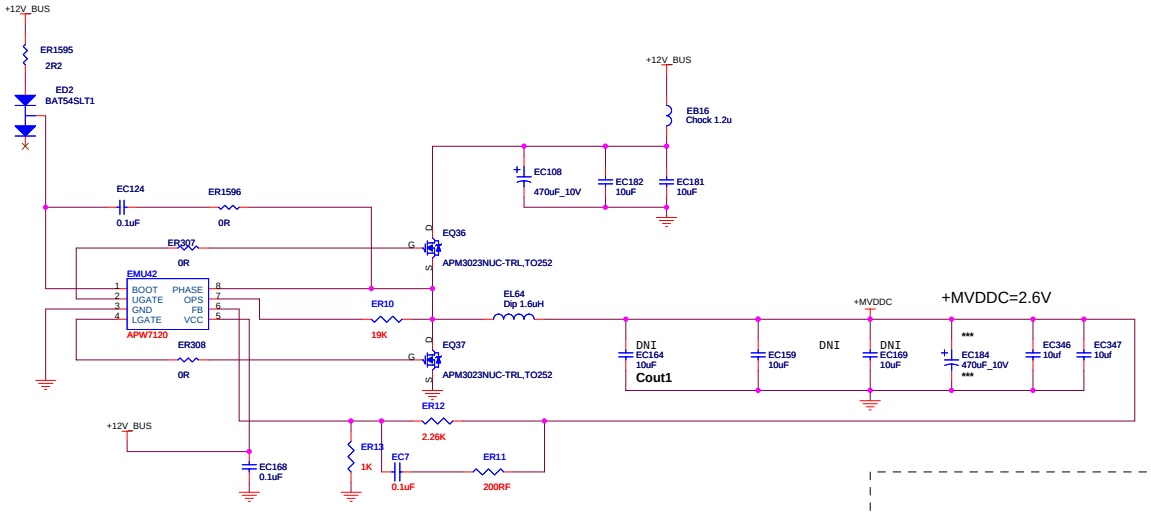
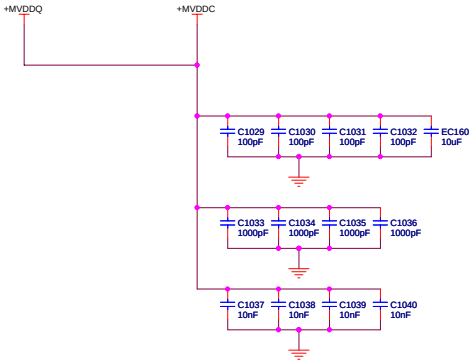
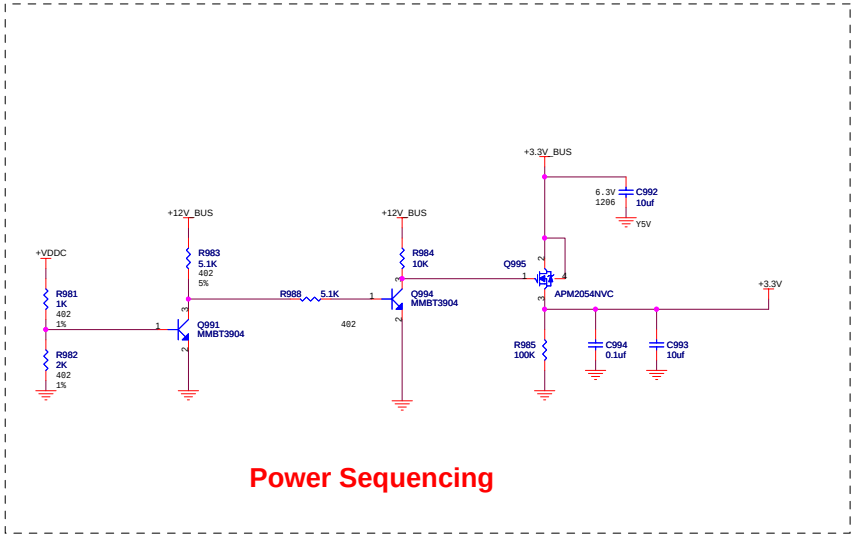


MVDDC=0.8 * [1 + (ER12 / ER13)]





Power Sequencing

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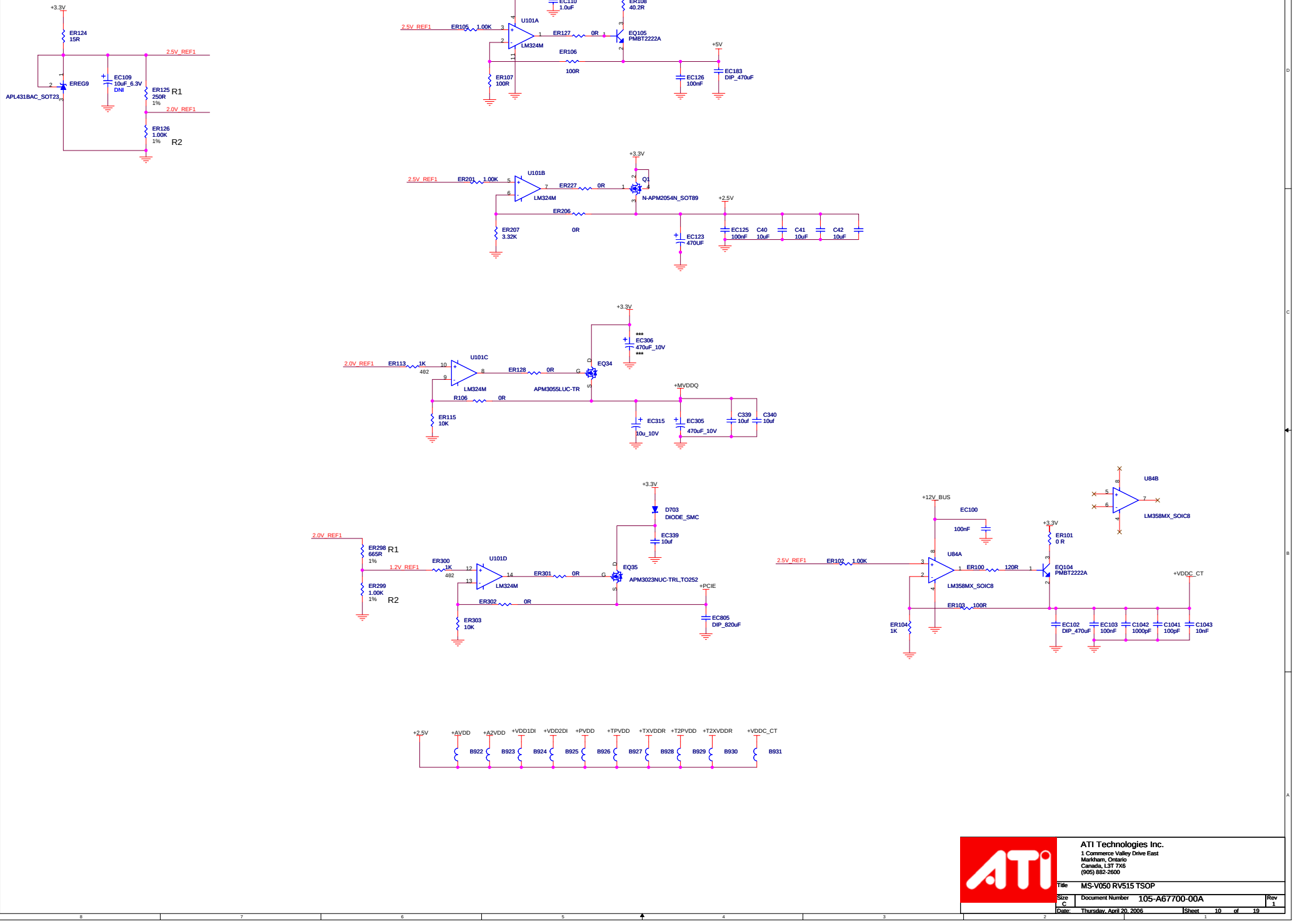

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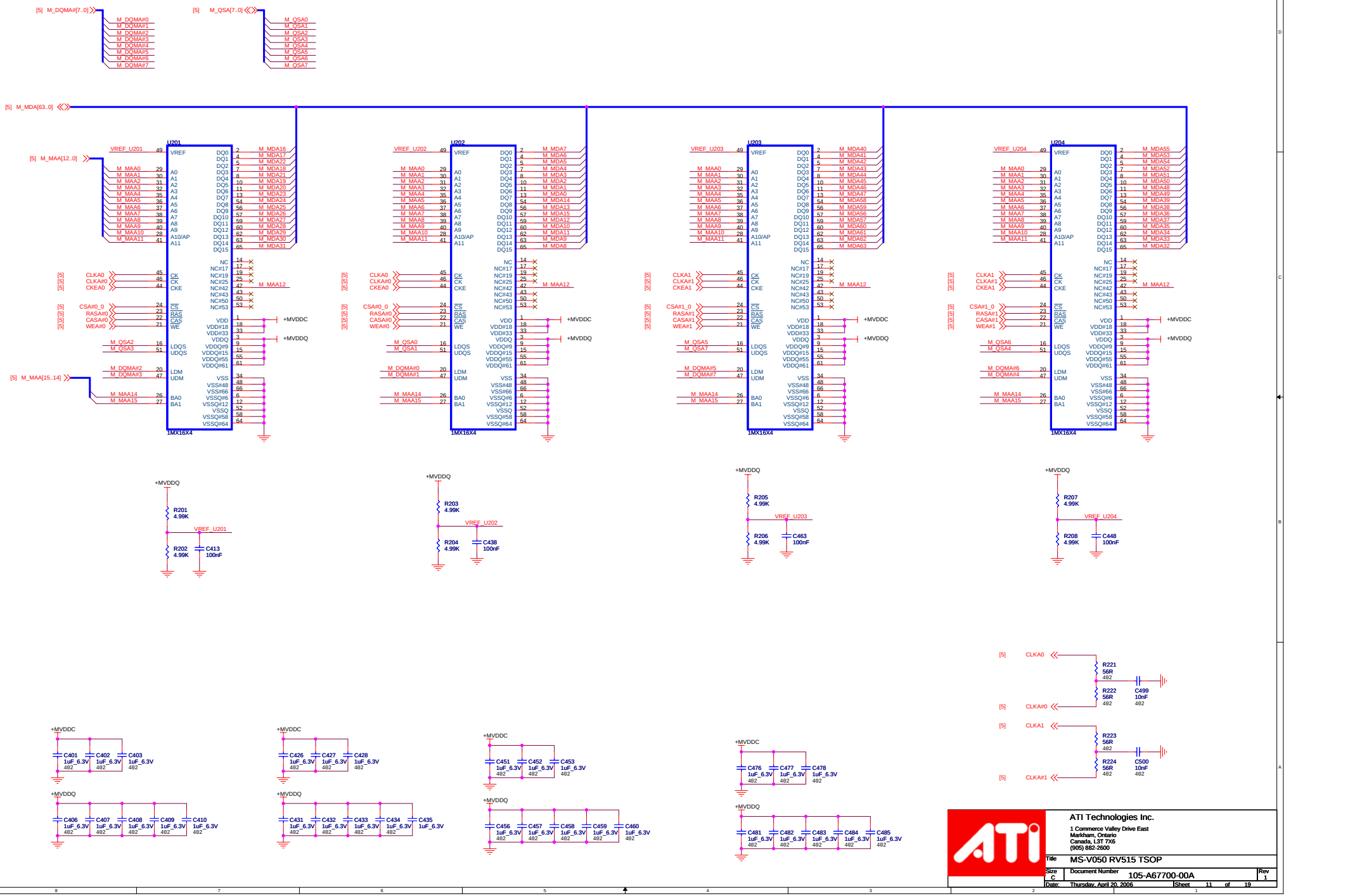
CHANNEL A: RANK 0 128/256MB DDR1



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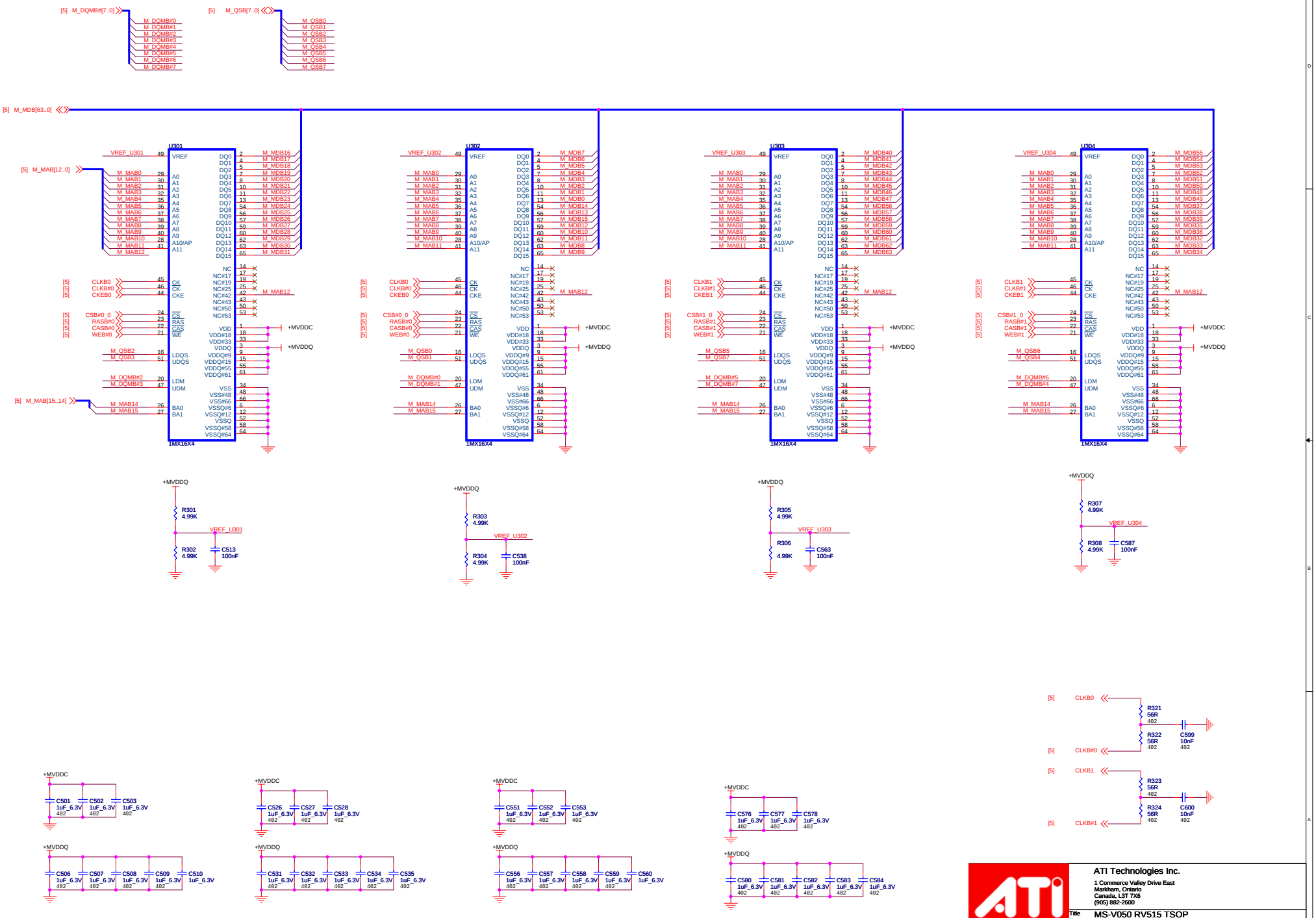
CHANNEL B: RANK 0 128/256MB DDR1



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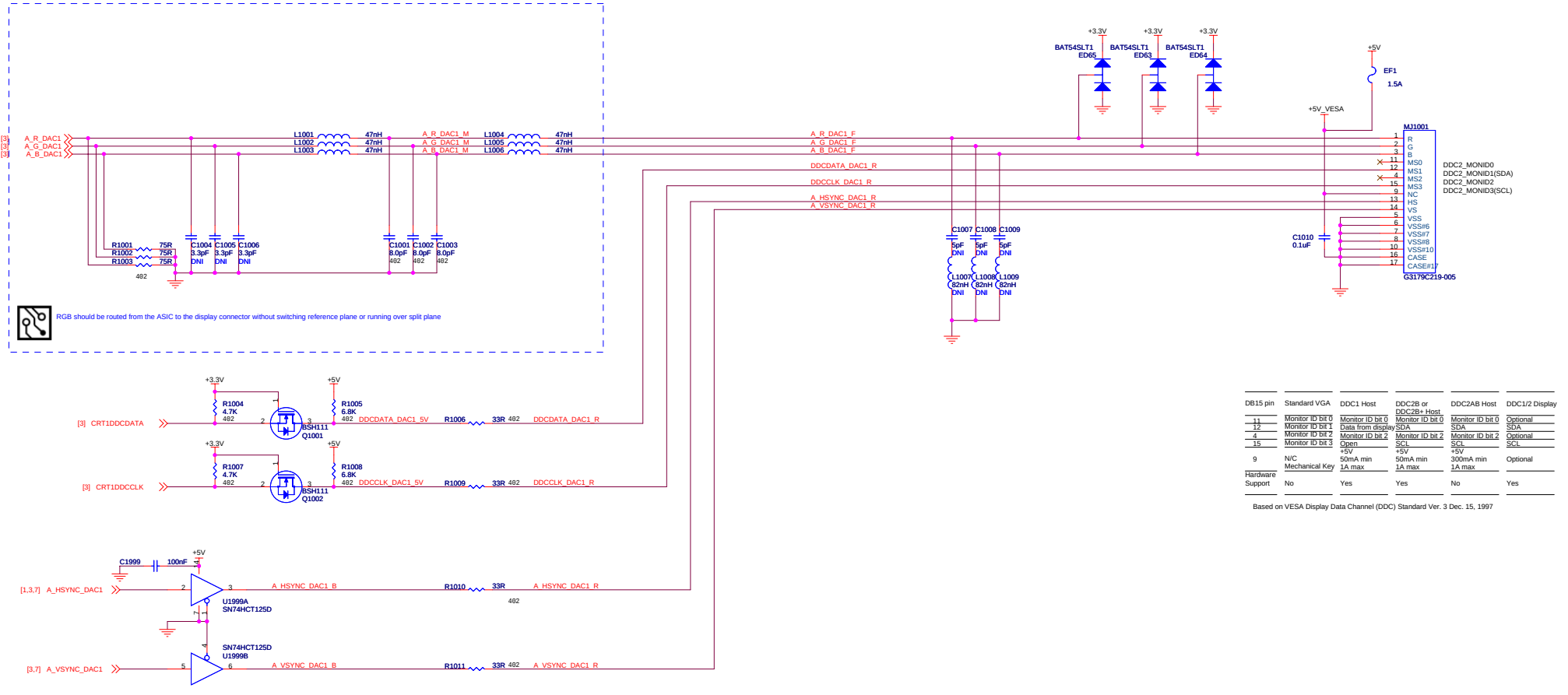

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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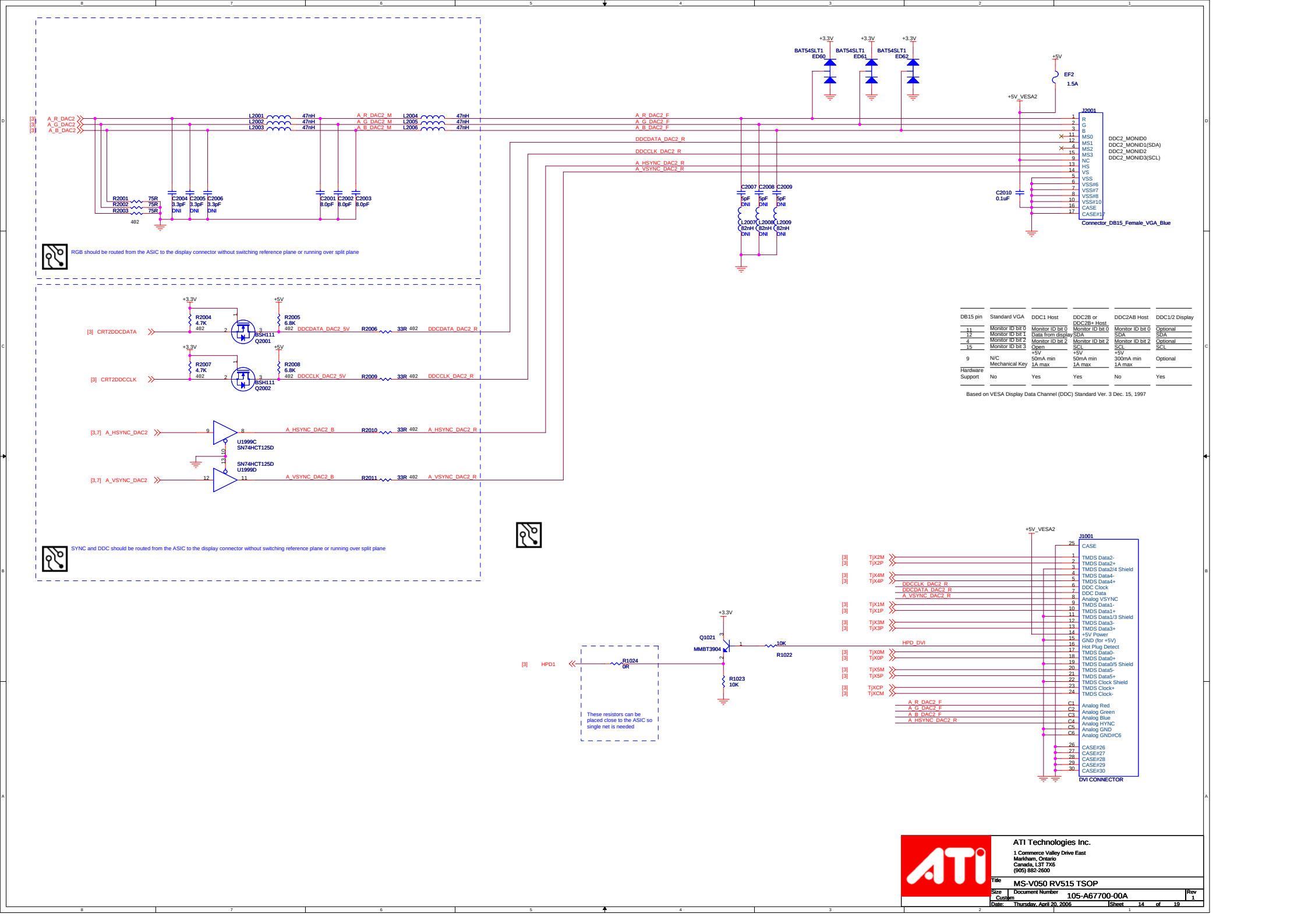

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

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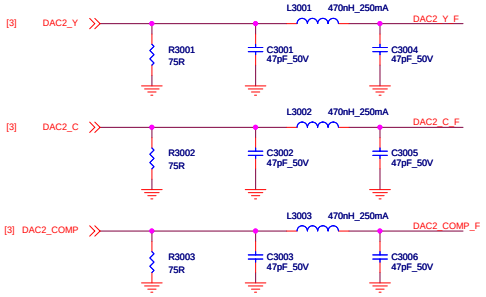
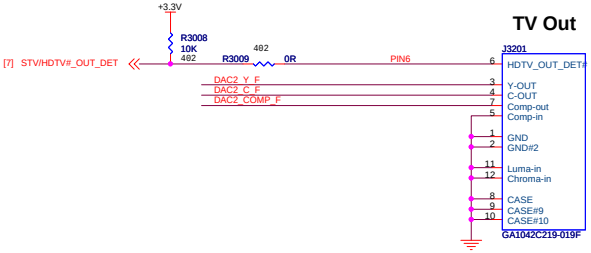


Place near connector
0R leaves footprint for Ferrite Beads if req'd for EMI



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

7 pin N56-07F0021-F02

9 pin N56-09F0031-F02

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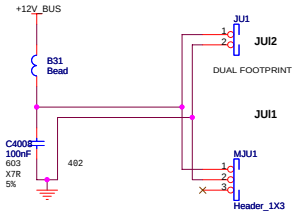

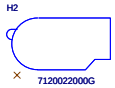

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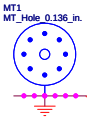

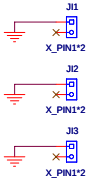

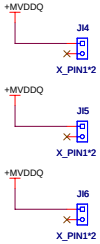

<Variant Name>

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<variant Name>

Title

RV515/530 ATX VGA DVI VIVO 256/512MB TSOP

Schematic No.

105-A67700-00A

Date:

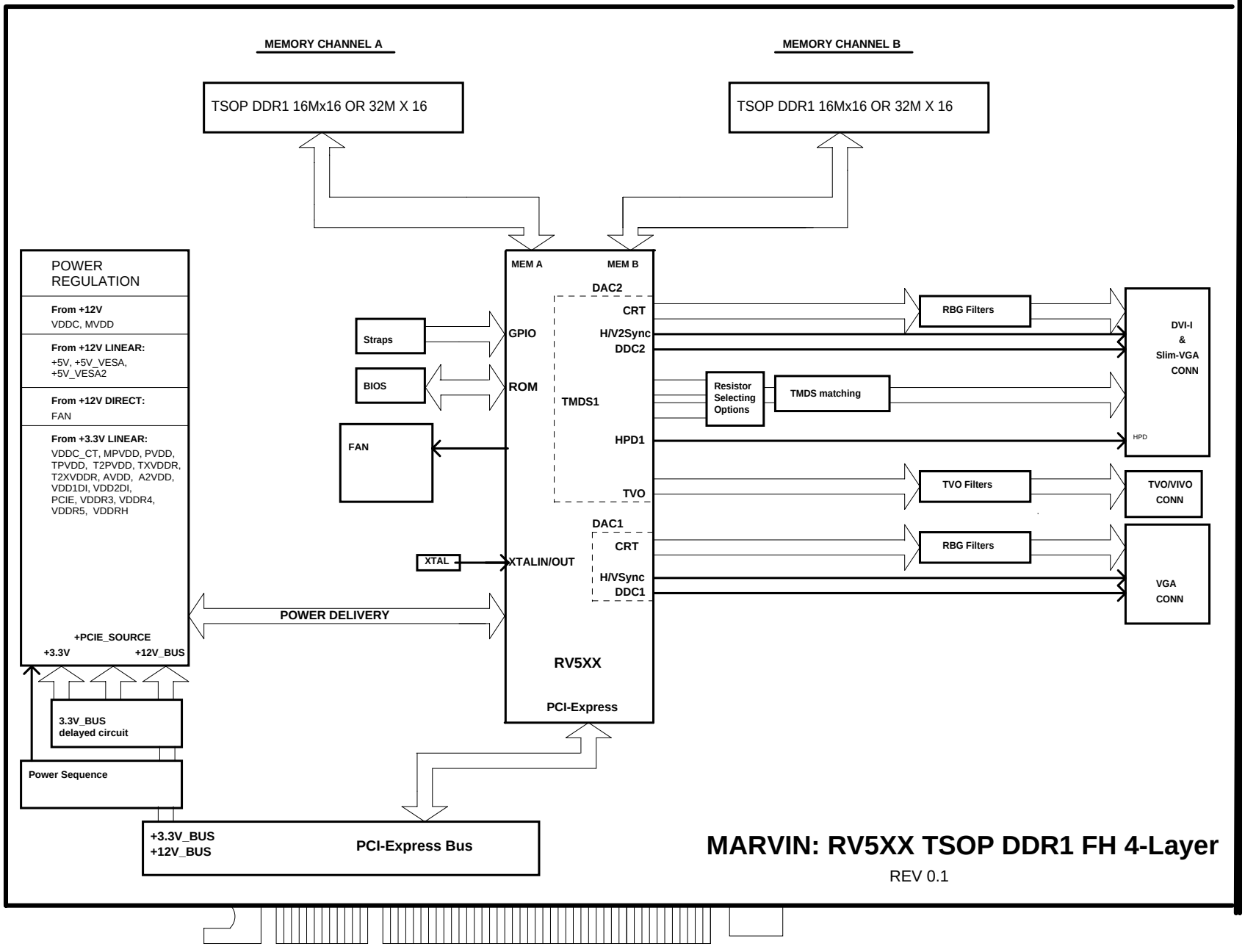
Thursday, April 20, 2006

REVISION HISTORY

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
		06/29/05	DERIVE FROM A666
0	00A	07/27/05	(pg 01) Correct clock circuitry to support RT (pg 08) Swap R603 and R604 to match layout for documentation purposes (pg 09) Swap R703 and R704 to match layout for documentation purposes (pg 10) Add MVDD linear regulator option (pg 11) Add R986, R987, R988; replace redundant power sequence circuit with +5V_EN and MVDD_EN (pg 11) Add MR911, R918 for +MPVDD for no-tracking option (pg 16) Change C3103 to 603 footprint, change RT to power from 3.3V_BUS to avoid leakage, remove redundant RT clock resistors

V050-12



MARVIN: RV5XX TSOP DDR1 FH 4-Layer

REV 0.1

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