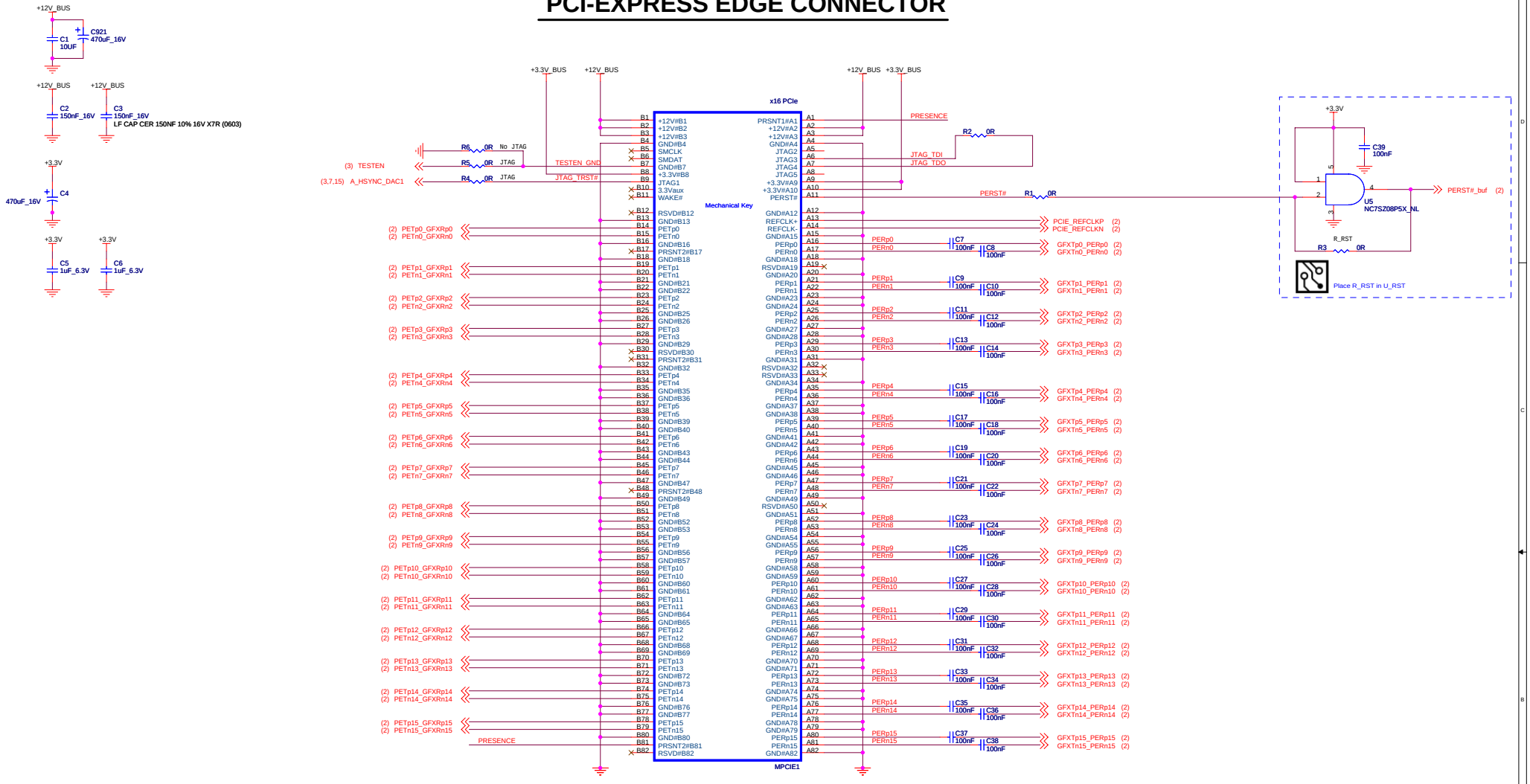
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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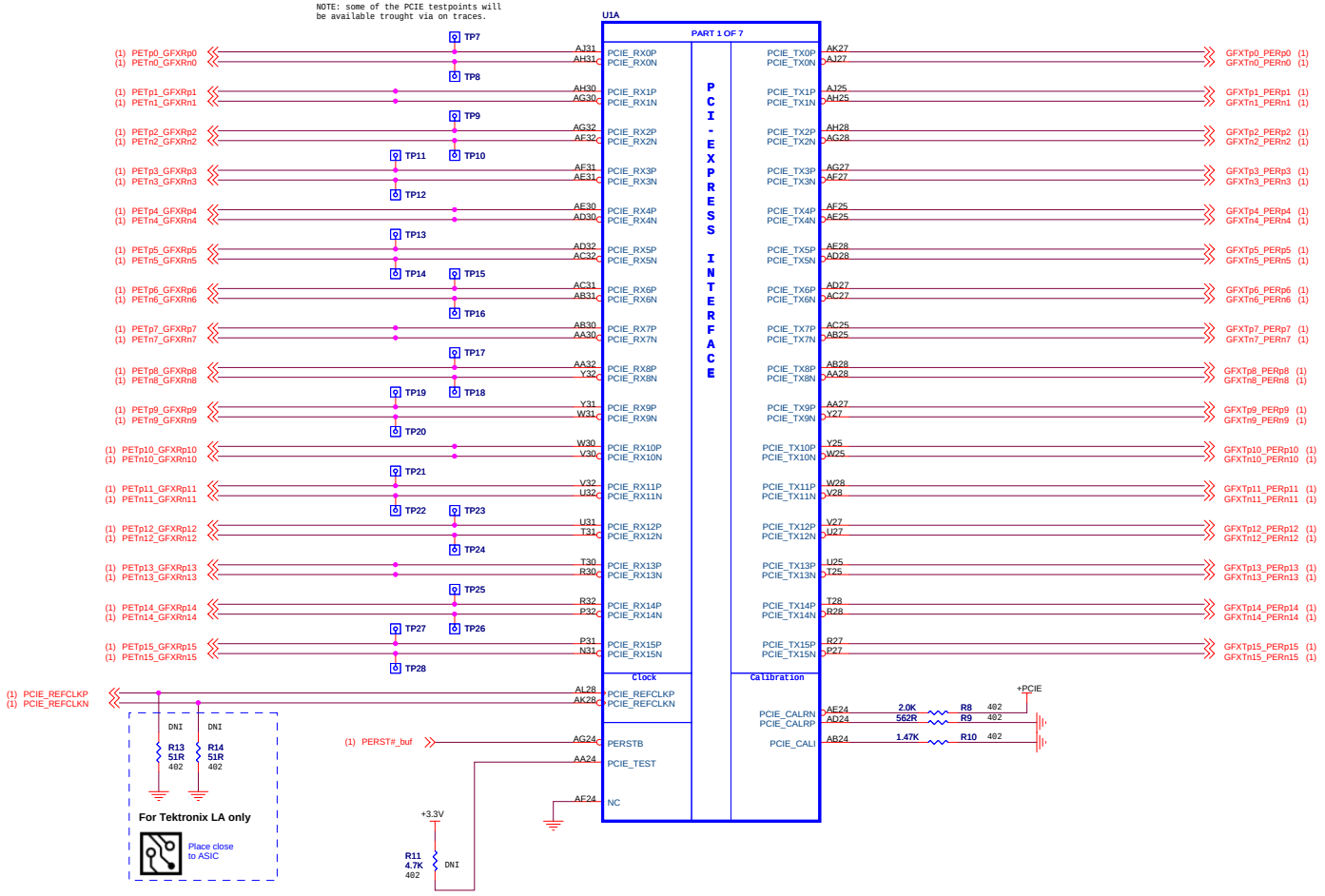

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Title: RH PCIE RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH

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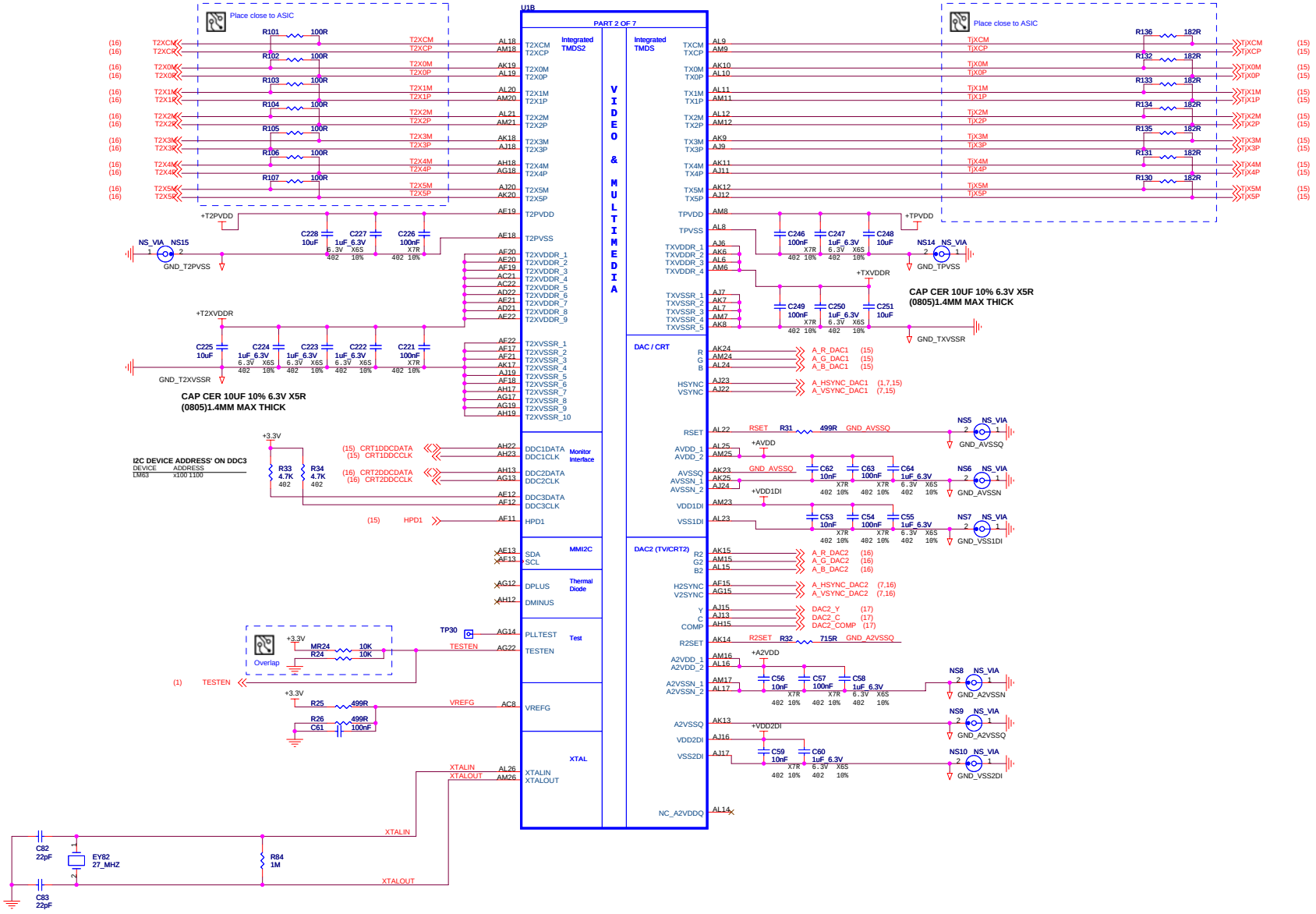
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X5R, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402



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Title RH PCIE RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH

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Recommended caps:
(see BOM for qualified values/vendors)
10uF , X5R, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402

U1E

PART 5 OF 7

POWER

Memory I/O

Memory I/O Clock

DVO I/O

PCI-Express

Core

I/O Internal

Selected PLL's

VDDR1_1 VDDR1_2 VDDR1_3 VDDR1_4 VDDR1_5 VDDR1_6 VDDR1_7 VDDR1_8 VDDR1_9 VDDR1_10 VDDR1_11 VDDR1_12 VDDR1_13 VDDR1_14 VDDR1_15 VDDR1_16 VDDR1_17 VDDR1_18 VDDR1_20 VDDR1_21 VDDR1_22 VDDR1_23 VDDR1_24 VDDR1_25 VDDR1_26 VDDR1_27 VDDR1_28 VDDR1_29 VDDR1_30 VDDR1_31 VDDR1_32 VDDR1_33 VDDR1_34 VDDR1_35 VDDR1_36 VDDR1_37 VDDR1_38 VDDR1_39 VDDR1_40 VDDR1_41 VDDR1_42 VDDR1_43 VDDR1_45 VDDR1_46

VDDRH0 VDDRH1 VSSRH0 VSSRH1

VDDR3_1 VDDR3_2 VDDR3_3 VDDR3_4 VDDR3_5 VDDR3_6 VDDR3_7 VDDR3_8

VDDR4_1 VDDR4_2 VDDR4_3 VDDR4_4 VDDR5_1 VDDR5_2 VDDR5_3 VDDR5_4

PVDD PVSS

PCIE_PVDD_12_1 PCIE_PVDD_12_2 PCIE_PVDD_12_3 PCIE_PVDD_12_4 PCIE_PVSS

PCIE_VDDR_12_1 PCIE_VDDR_12_2 PCIE_VDDR_12_3 PCIE_VDDR_12_4 PCIE_VDDR_12_5 PCIE_VDDR_12_6 PCIE_VDDR_12_7 PCIE_VDDR_12_8 PCIE_VDDR_12_9 PCIE_VDDR_12_10 PCIE_VDDR_12_11 PCIE_VDDR_12_12 PCIE_VDDR_12_13 PCIE_VDDR_12_14

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22 VDDC_23 VDDC_24 VDDC_25 VDDC_26 VDDC_27 VDDC_28 VDDC_29 VDDC_30 VDDC_31 VDDC_32 VDDC_33 VDDC_34 VDDC_35 VDDC_36 VDDC_37 VDDC_38 VDDC_39

VDDCI_1 VDDCI_2 VDDCI_3 VDDCI_4 VDDCI_6 VDDCI_7 VDDCI_8

VDD25_1 VDD25_2 VDD25_3 VDD25_4 VDD25_5 VDD25_6

MPVDD MPVSS

VDDPLL

+MVDD

C301 C302 C303 C304 C305 C306 C307 C308 C309 C310 1uF_6.3V

C311 C312 C313 C314 C315 C316 C317 C318 C319 C320 1uF_6.3V

C321 C322 C326 C327 C328 C329 C330 1uF_6.3V

C341 C342 C343 C344 C345 10uF

CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

+PCIE

C201 C202 C203 C204 1uF_6.3V

NS18 _NS_VIA

GND_PCIE_PVSS

C191 C192 C193 C194 C195 C196 C197 C198 1uF_6.3V

C199 C200 10uF

CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

+VDDC

C161 C162 C163 C164 C165 C166 C167 C168 C169 C170 1uF_6.3V

C181 C182 C183 10uF

C171 C172 C173 C174 C175 C176 C177 C178 C179 C180 1uF_6.3V

C151 C152 1uF_6.3V

CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

B54 BLM15BD121SN1
B55 BLM15BD121SN1

C231 C232 C233 C234 1uF_6.3V

NS16 NS_VIA

GND_VSSRH0

NS17 NS_VIA

GND_VSSRH1

+3.3V

C241 C242 C243 C244 1uF_6.3V

C245 10uF

CAP CER 10UF 10%
6.3V X5R (0805)1.4MM
MAX THICK

+VDDR_DVP

C236 C237 C238 C239 1uF_6.3V

+VDDC

C211 C212 C216 1uF_6.3V

C213 10uF

+VDDC_CT

C206 C207 C208 C209 1uF_6.3V

C210 10uF

+PVDD

C69 10nF

C70 100nF

C71 1uF_6.3V

NS12 _NS_VIA

GND_PVSS

+MPVDD

C67 1uF_6.3V

C66 100nF

C65 10nF

C68 22uF_16V

NS_VIA_NS11

GND_MPVSS

+VDDPLL

B56 BLM15BD121SN1

C214 1uF_6.3V

C215 1uF_6.3V

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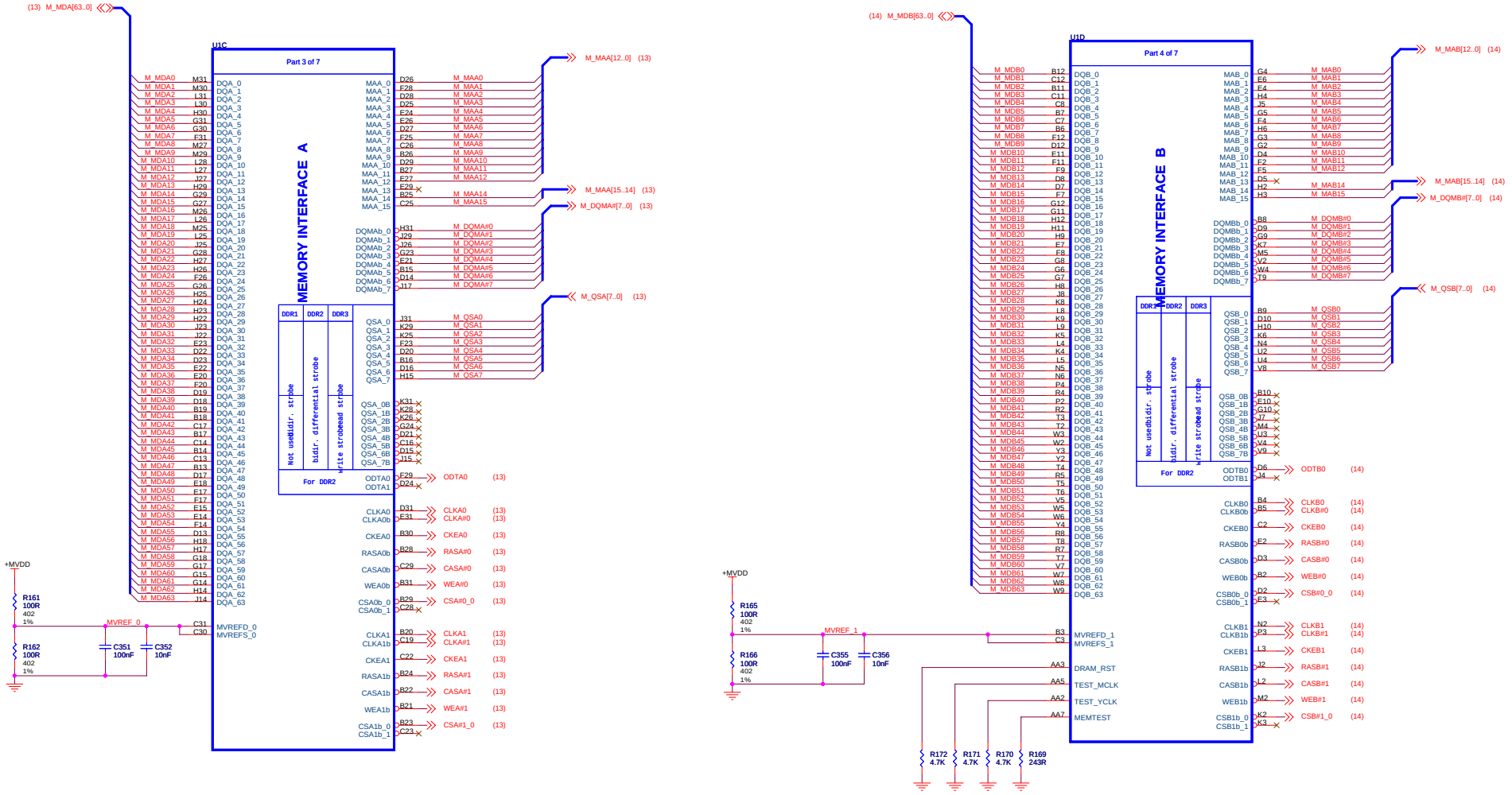

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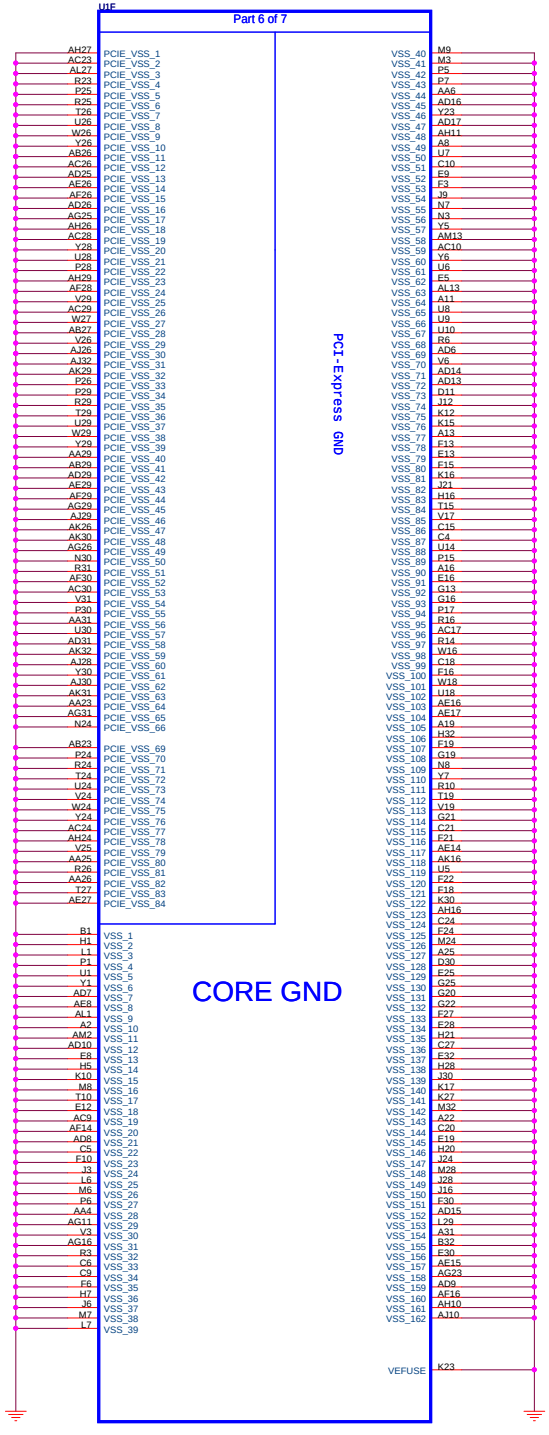

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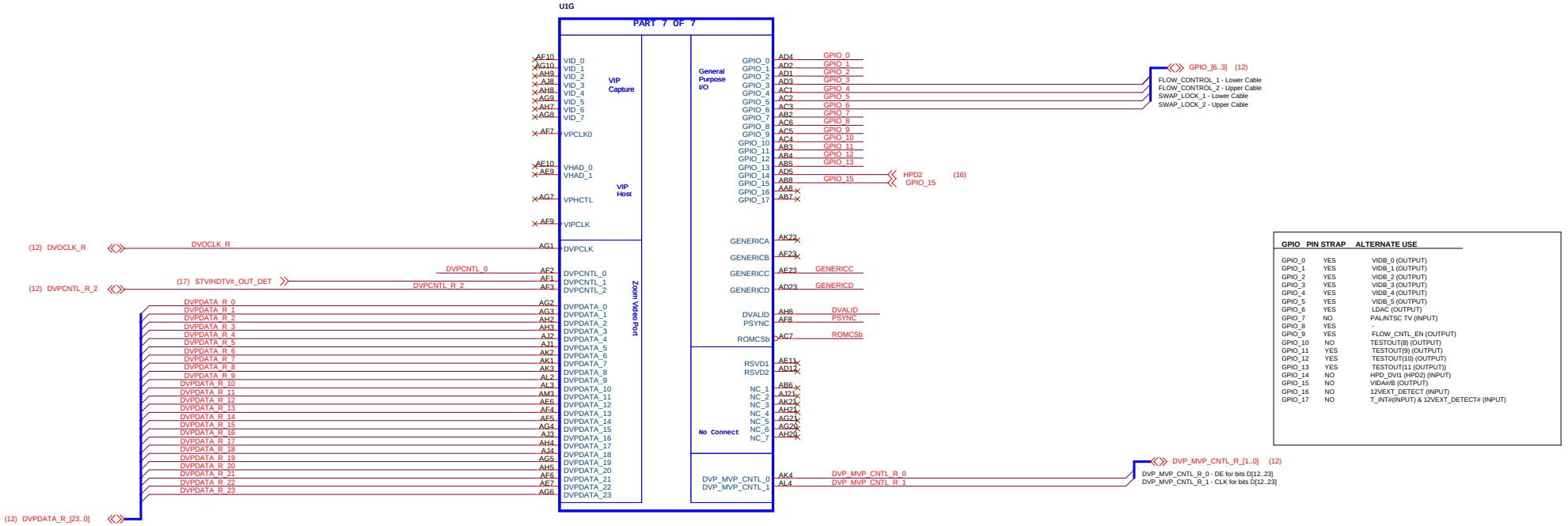
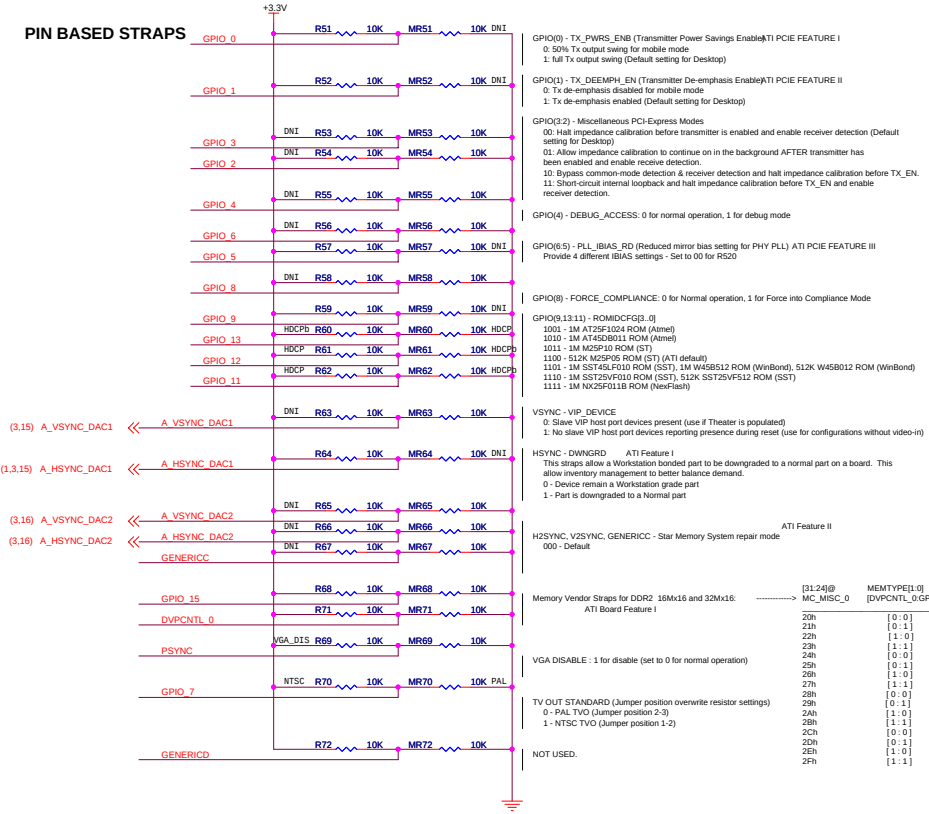
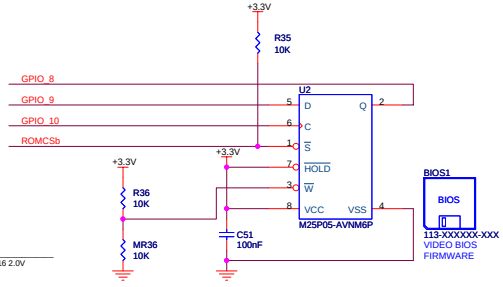


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDAii/B (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

PIN BASED STRAPS





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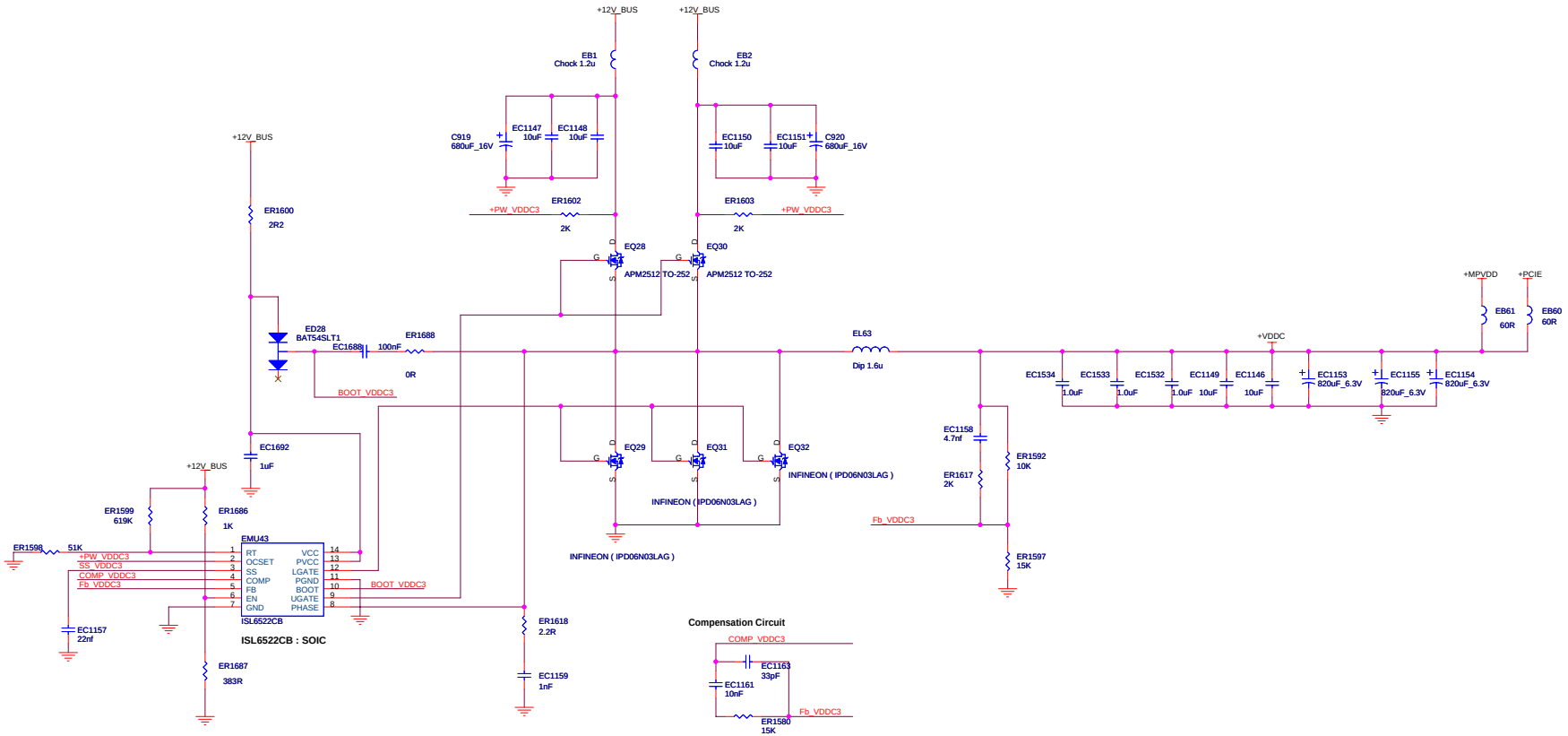

+VDDC=0.8*(1+(ER1592 / ER1597))

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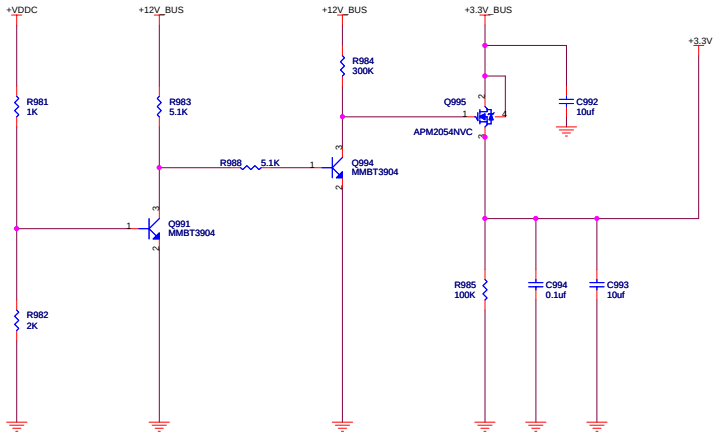

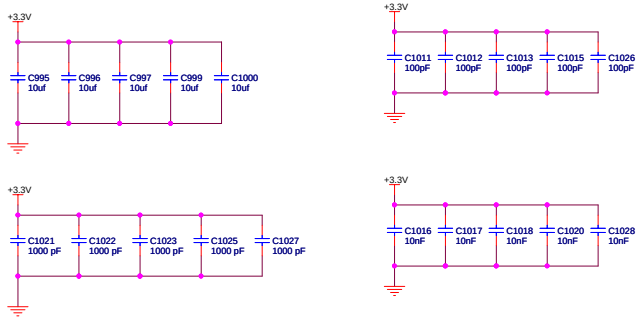

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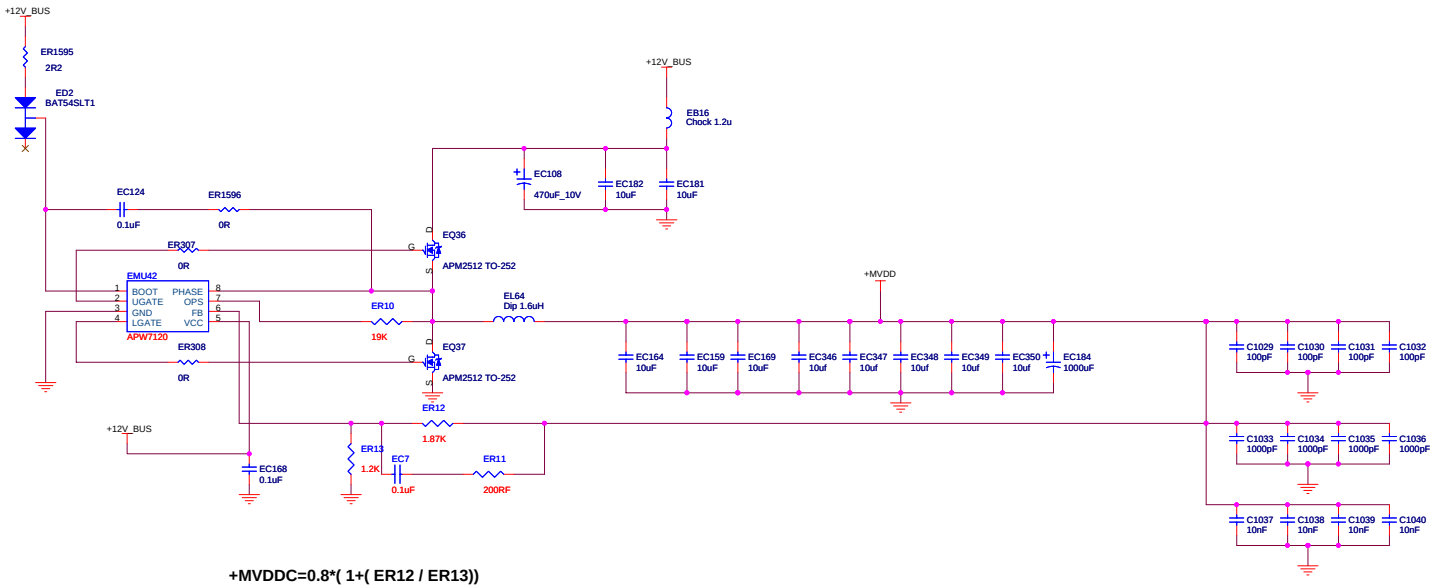

+MVDDC=0.8*(1+(ER12 / ER13))

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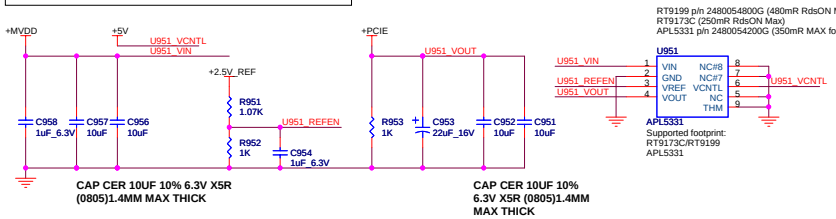
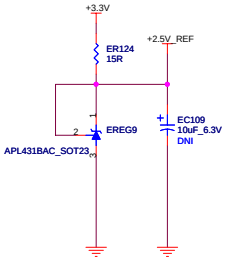
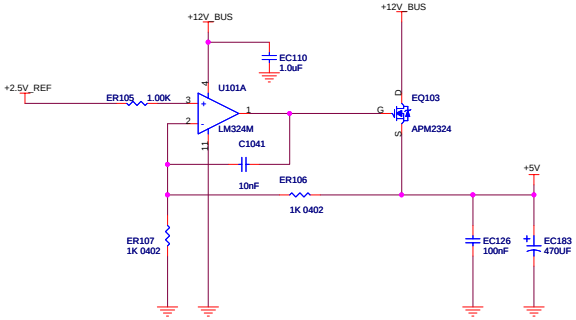
Optional regulator for +PCIE
Vout = 1.2V ~1.25V

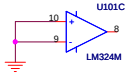


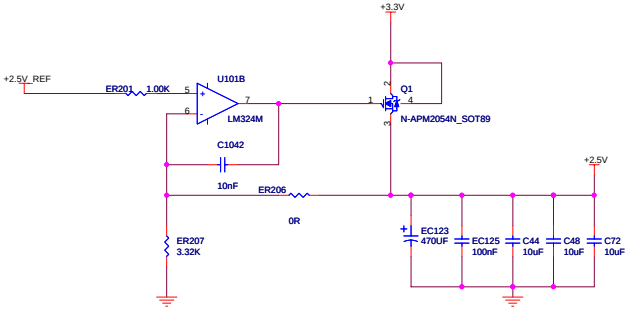
RT9199 p/n 2480054800G (480mR RdsON Max)
RT9173C (250mR RdsON Max)
APL5331 p/n 2480054200G (350mR MAX for 2A)

Supported footprint:
RT9173C/RT9199
APL5331

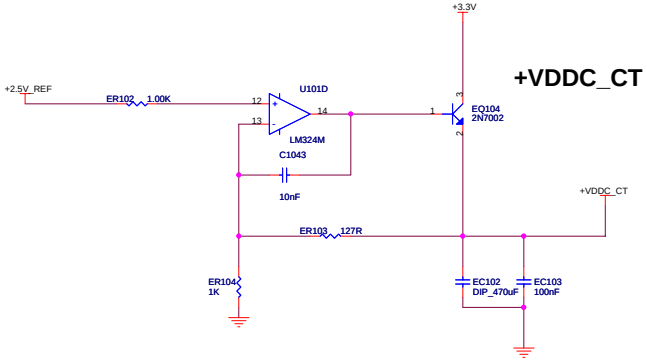


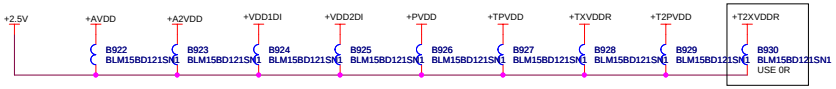






+VDDC_CT 2.8V





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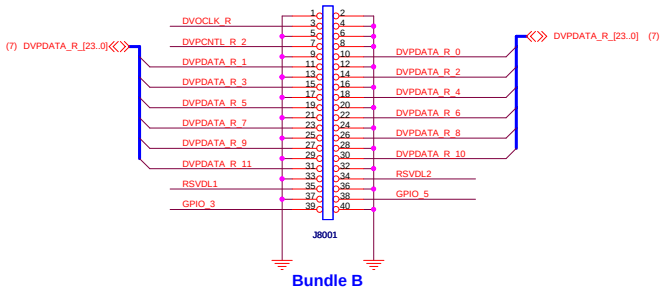
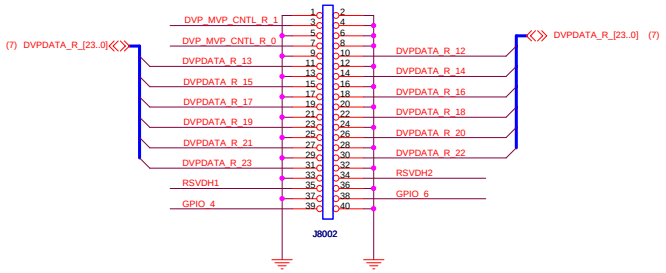
CrossFire Card-Edge

Lower Cable Card Edge

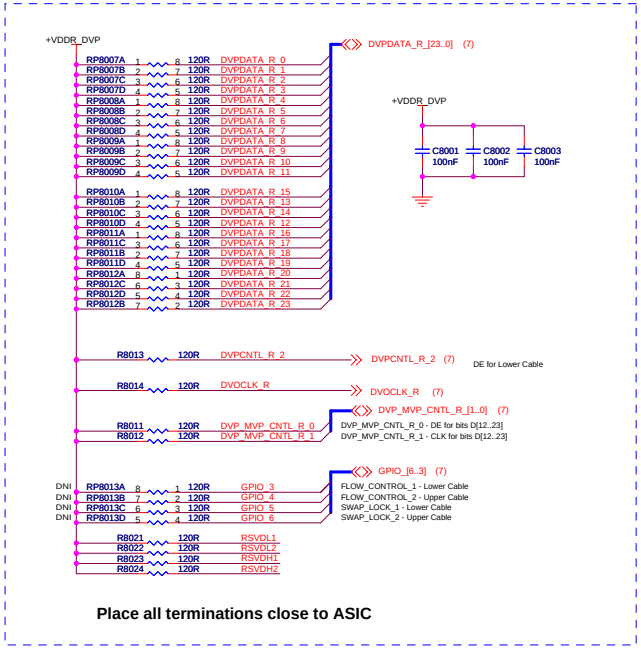


Bundle B

Upper Cable Card Edge



Bundle A



Place all terminations close to ASIC

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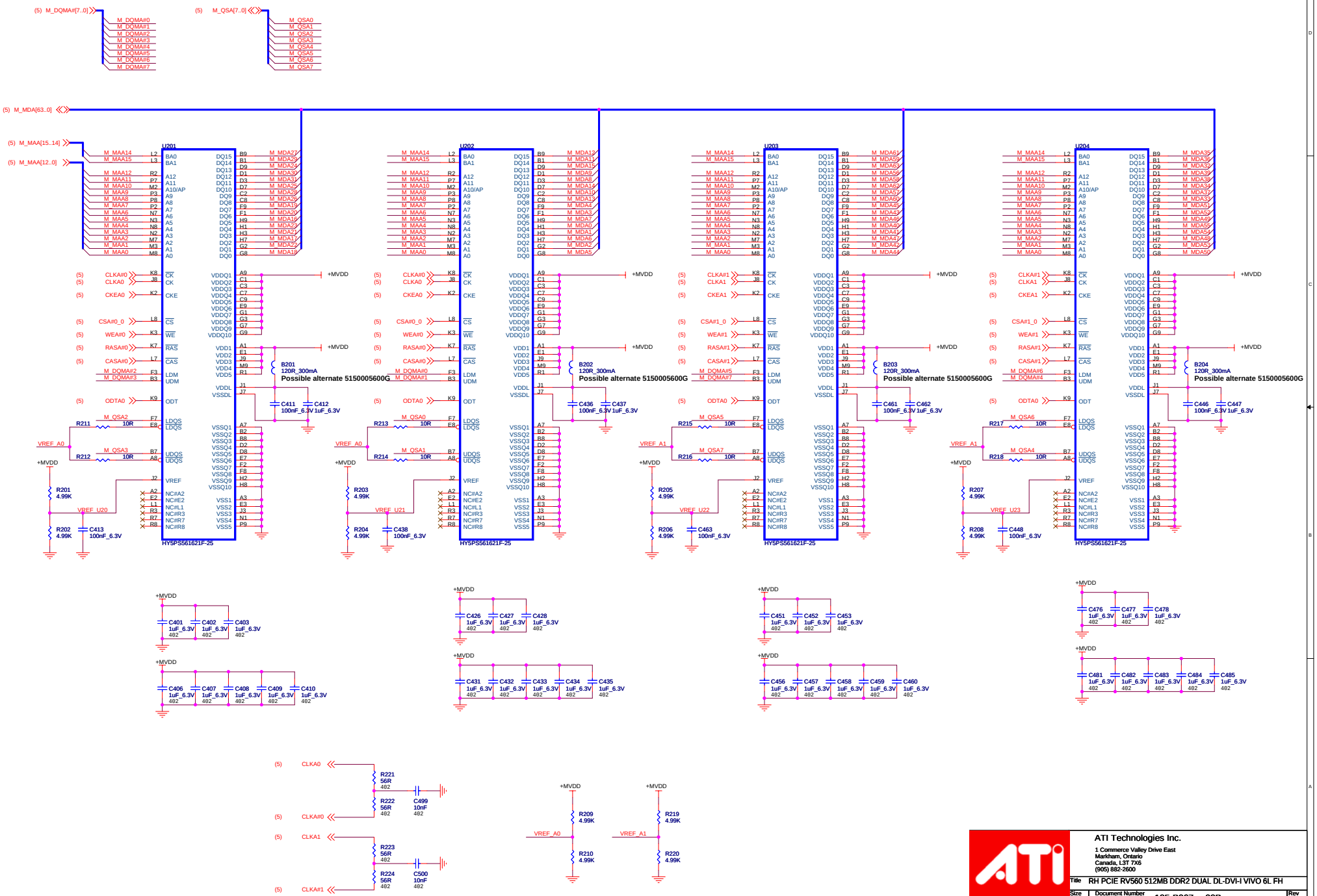
CHANNEL A: 128MB/256MB DDR2



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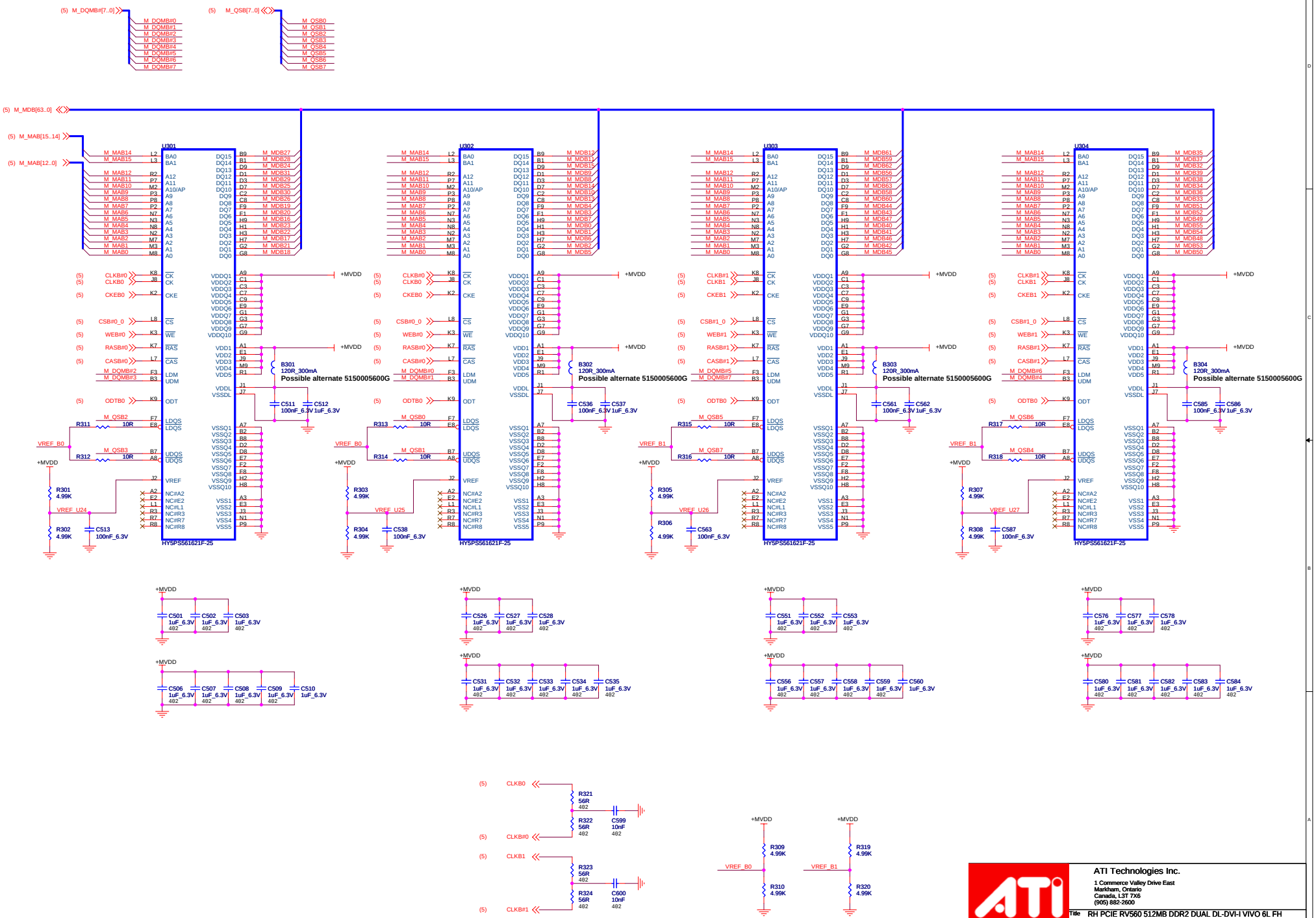
CHANNEL B: 128MB/256MB DDR2



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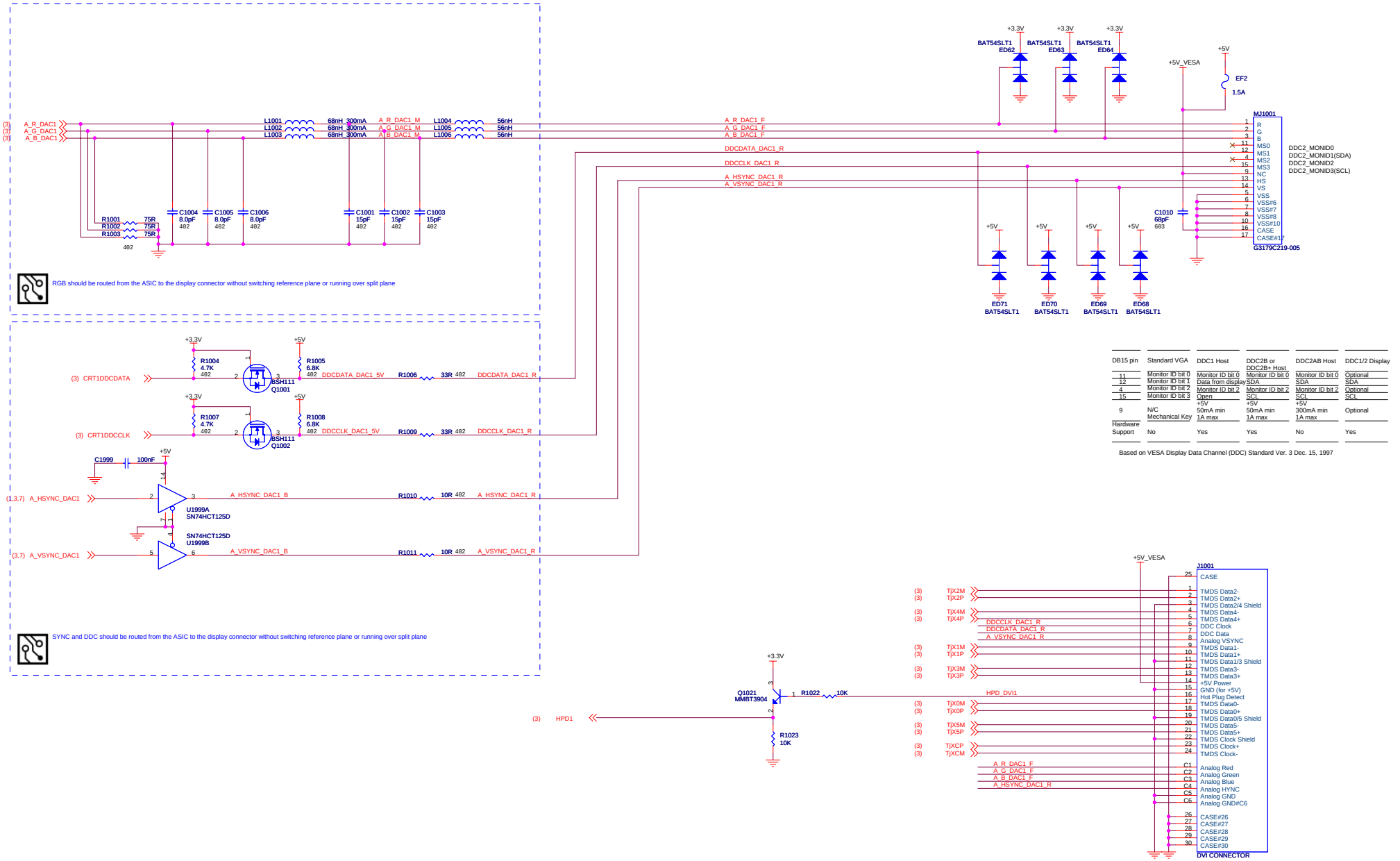

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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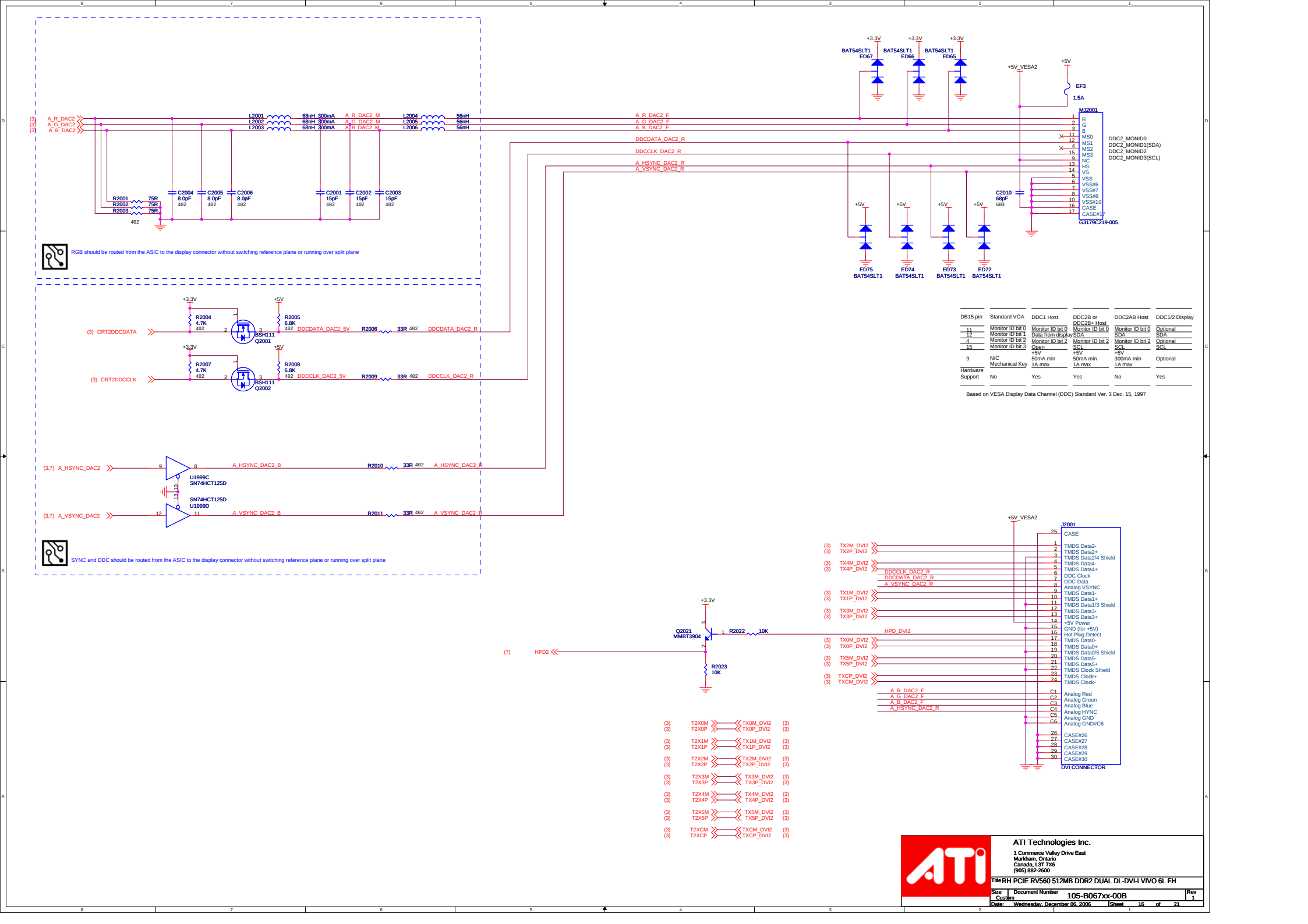

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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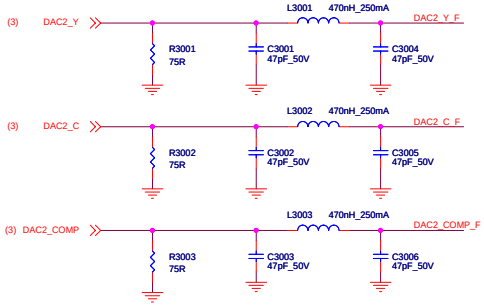

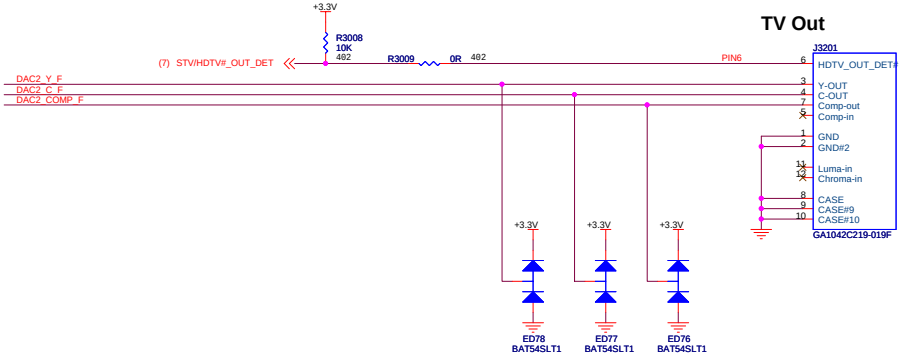

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Title RH PCIE RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH

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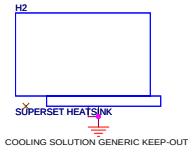
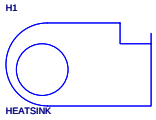
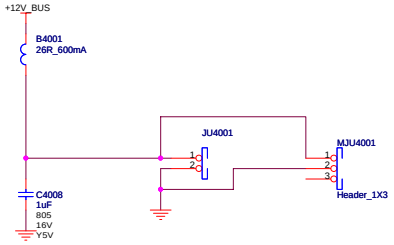
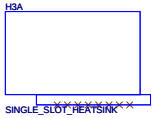


COOLING SOLUTION GENERIC KEEP-OUT







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DVI/DVI SCREWS with top tab

ASSY-SCREW1
SCREW
JACKSCREW
<3rd part field>
7020000800G

ASSY-SCREW2
SCREW
JACKSCREW
<3rd part field>
7020000800G

ASSY-SCREW3
SCREW
JACKSCREW
<3rd part field>
7020000800G

ASSY-SCREW4
SCREW
JACKSCREW
<3rd part field>
7020000800G

BKT1
BRACKET
8020042500G

ASSY1
ANTISTATIC
BAG
6_X_11

MVDD1
RV560 Socket

PCB1
PCB
109-B06731-00B

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM4 SW_FB
FM5 SW_FB
FM6 SW_FB

J1 X_PIN1*2
J2 X_PIN1*2
J3 X_PIN1*2
J4 X_PIN1*2
J5 X_PIN1*2
J6 X_PIN1*2
J7 X_PIN1*2
J8 X_PIN1*2
J9 X_PIN1*2

<Variant Name>

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<variant Name>

Title	Schematic No.	Date:
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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/07/25	Design based on 105/109-A880xx-00E Replacing GDDR3 memory config to DDR2 (pg 19) Removing +1.8V regulator - not required (pg 11) Removing linear regulator for +MVDD (not used) to facilitate PCB design
0	00B	06/08/11	Remove CrossFire support (pg 08) Renaming net label BUSEN to ENBUS

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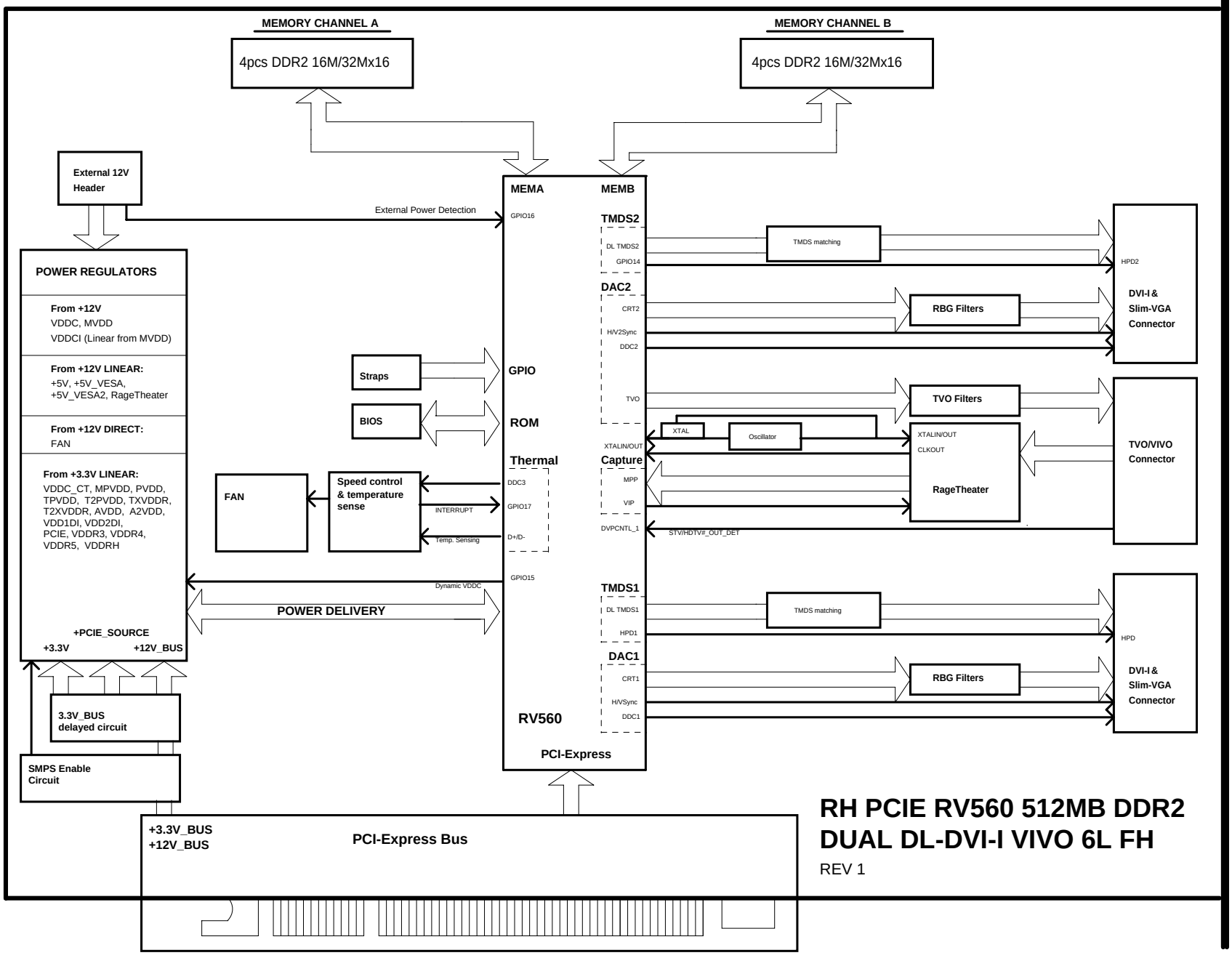

RH PCIE RV560 512MB DDR2 DUAL DL-DVI-I VIVO 6L FH

REV 1

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