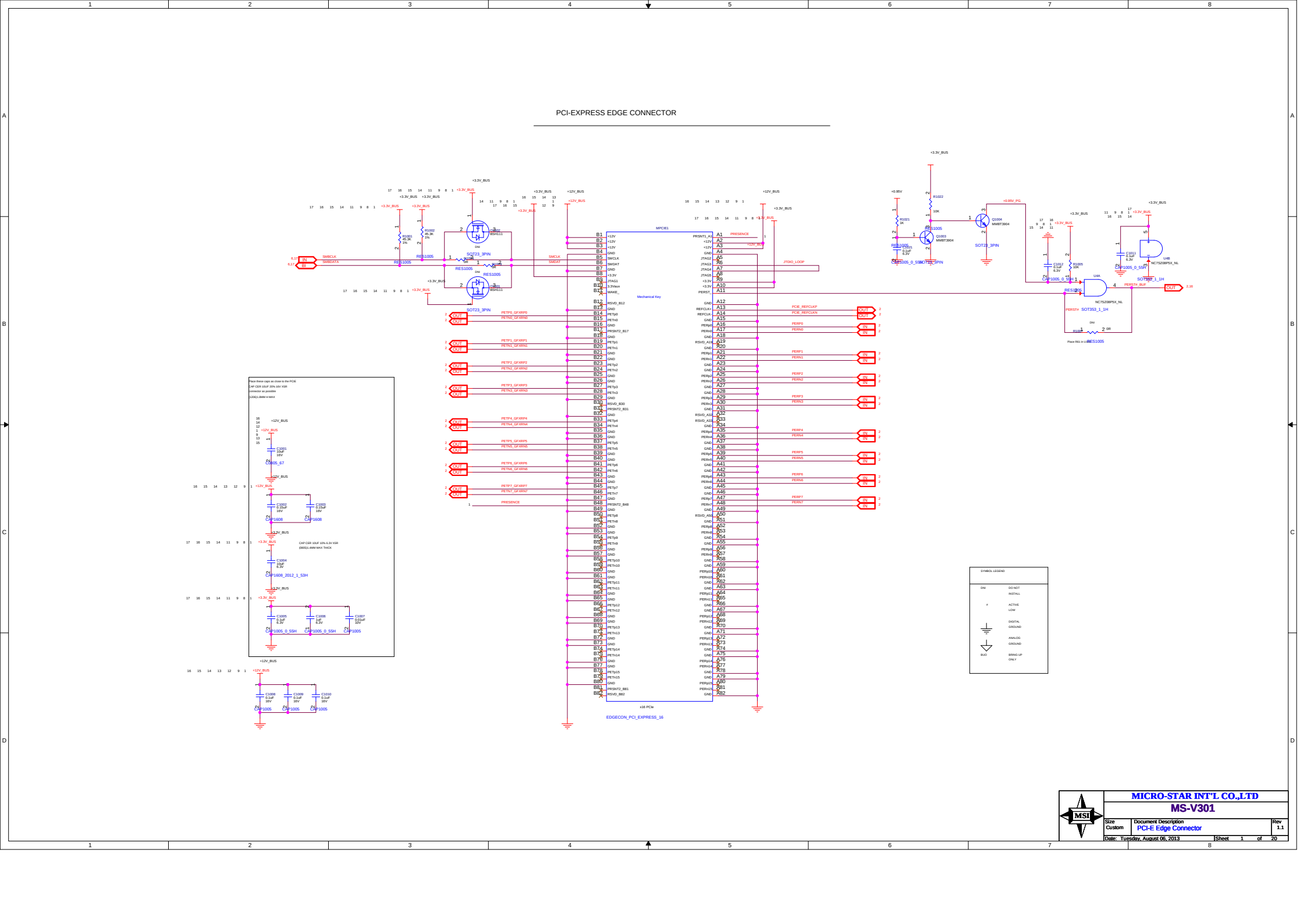
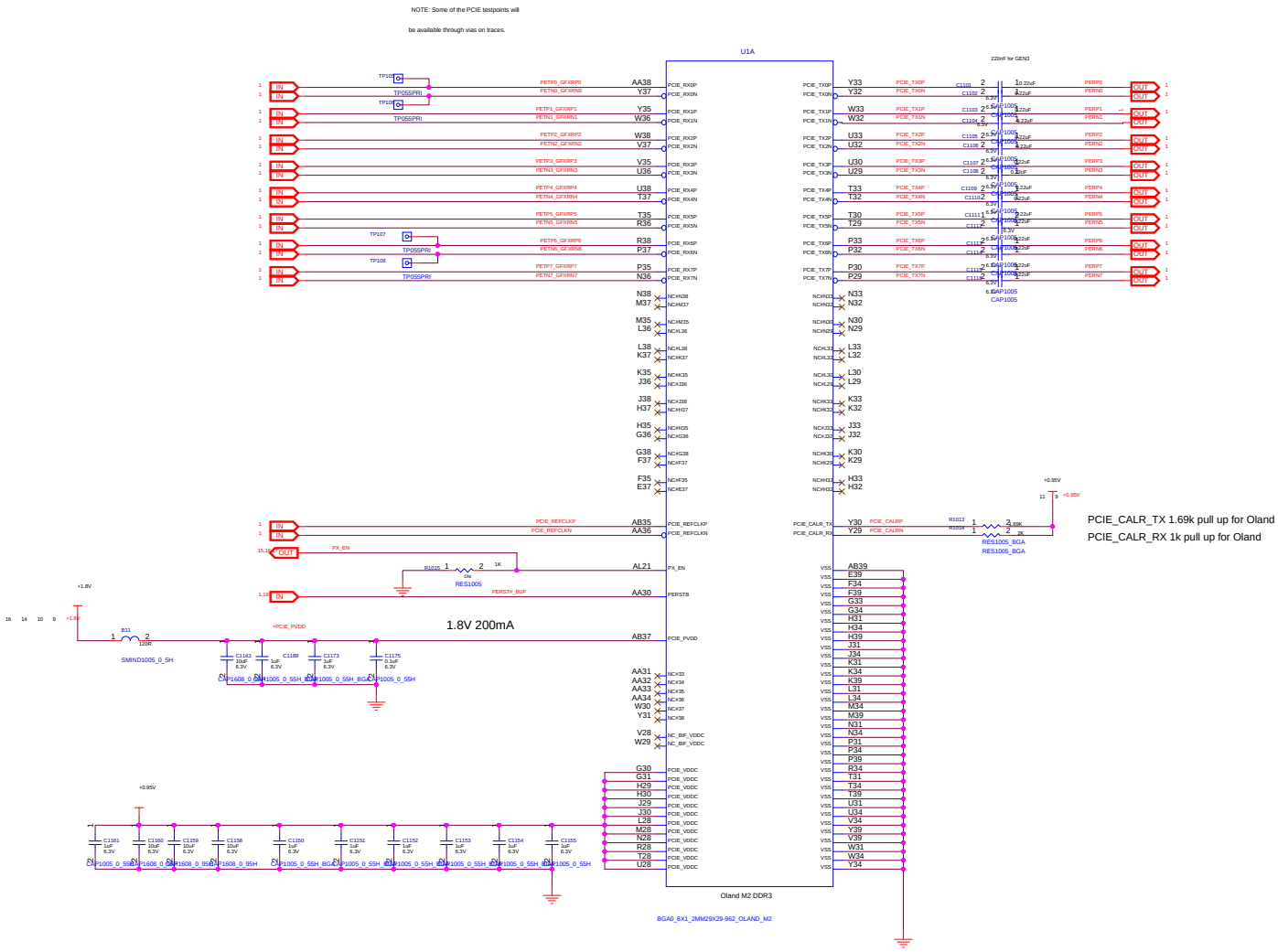
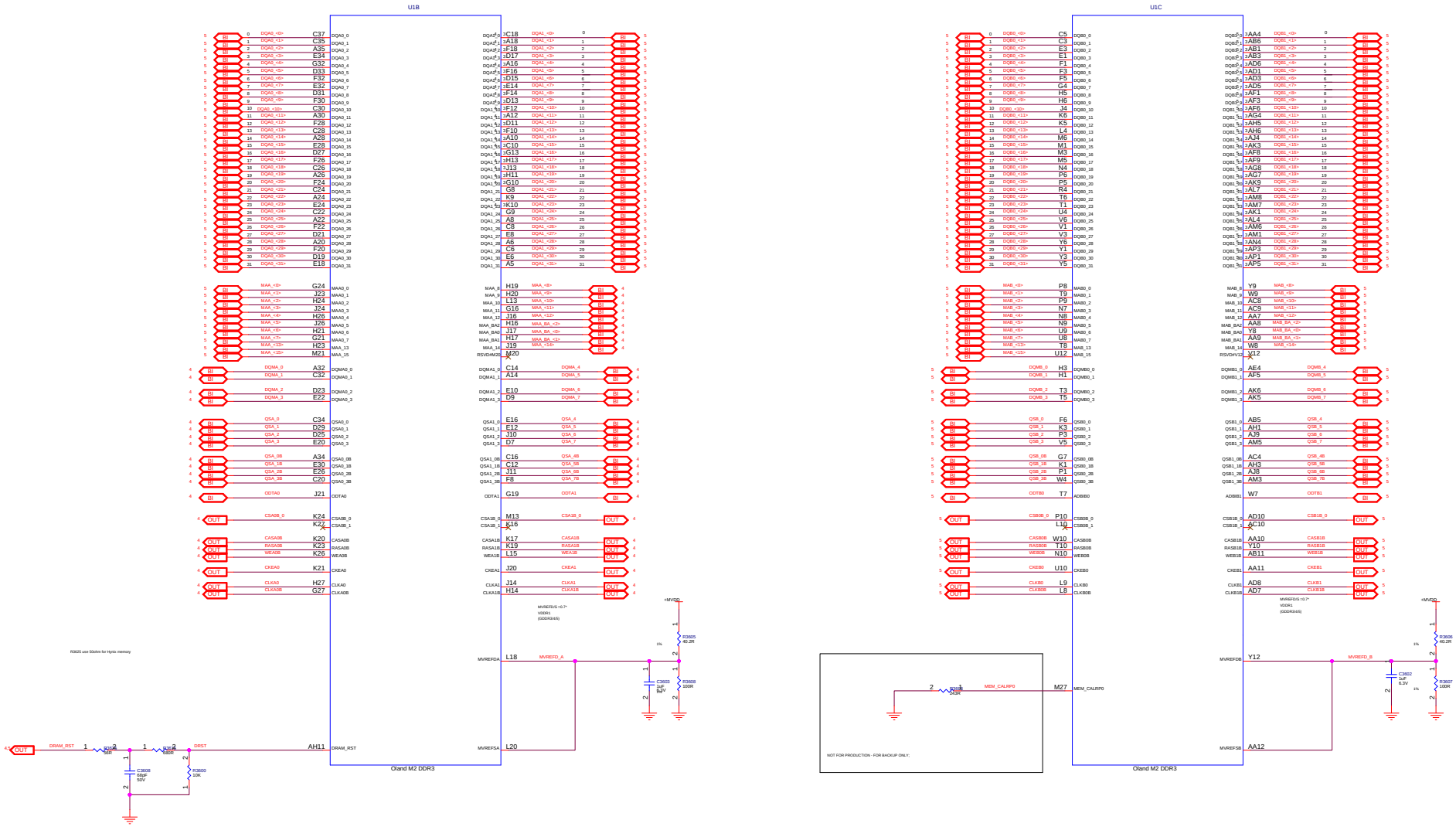

PCI-EXPRESS EDGE CONNECTOR
MPCIE1
Mechanical Key
EDGECON_PCI_EXPRESS_16
SMBCLK
SMBDATA
SMCLK
SMDAT
JTDIO_LOOP
PRESENCE
PCIE_REFCLKP
PCIE_REFCLKN
PERST#
PERST#_BUF
PETP0_GFXRP0
PETN0_GFXRN0
PETP1_GFXRP1
PETN1_GFXRN1
PETP2_GFXRP2
PETN2_GFXRN2
PETP3_GFXRP3
PETN3_GFXRN3
PETP4_GFXRP4
PETN4_GFXRN4
PETP5_GFXRP5
PETN5_GFXRN5
PETP6_GFXRP6
PETN6_GFXRN6
PETP7_GFXRP7
PETN7_GFXRN7
PERP0
PERN0
PERP1
PERN1
PERP2
PERN2
PERP3
PERN3
PERP4
PERN4
PERP5
PERN5
PERP6
PERN6
PERP7
PERN7
SYMBOL LEGEND
DO NOT INSTALL
ACTIVE LOW
DIGITAL GROUND
ANALOG GROUND
BRING UP ONLY
MICRO-STAR INT'L CO.,LTD
MS-V301
Size Custom
Document Description PCI-E Edge Connector
Rev 1.1
Date: Tuesday, August 06, 2013
Sheet 1 of 20

Oland XT M2 PCIe Interface



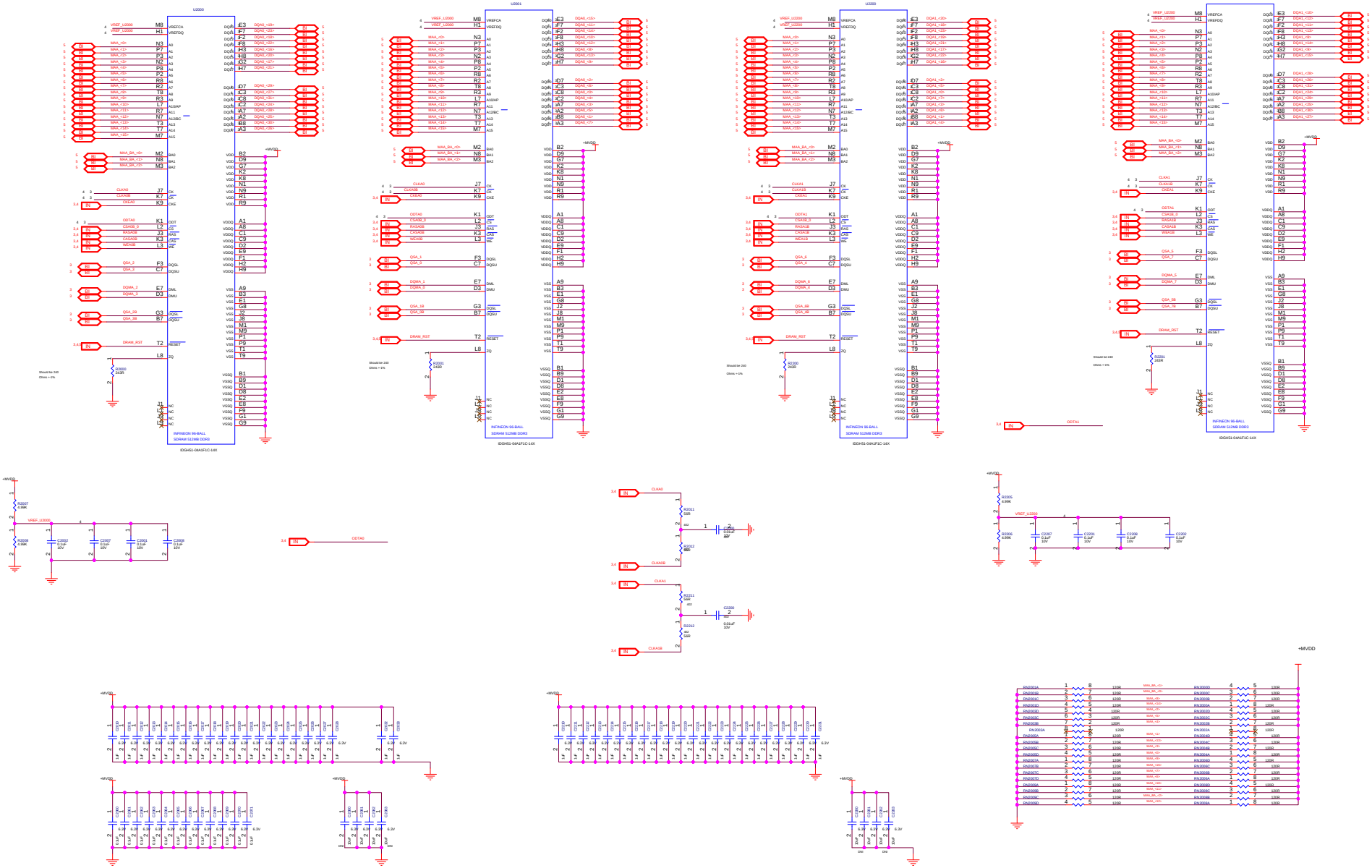
MICRO-STAR INT'L CO.,LTD	
MS-V301	
Size: Custom	Document Description: Oland PCIE Interface
Rev: 1.1	
Date: Tuesday, August 06, 2013	Sheet 2 of 20

(3)Oland XT MEM Interface Ch A&B



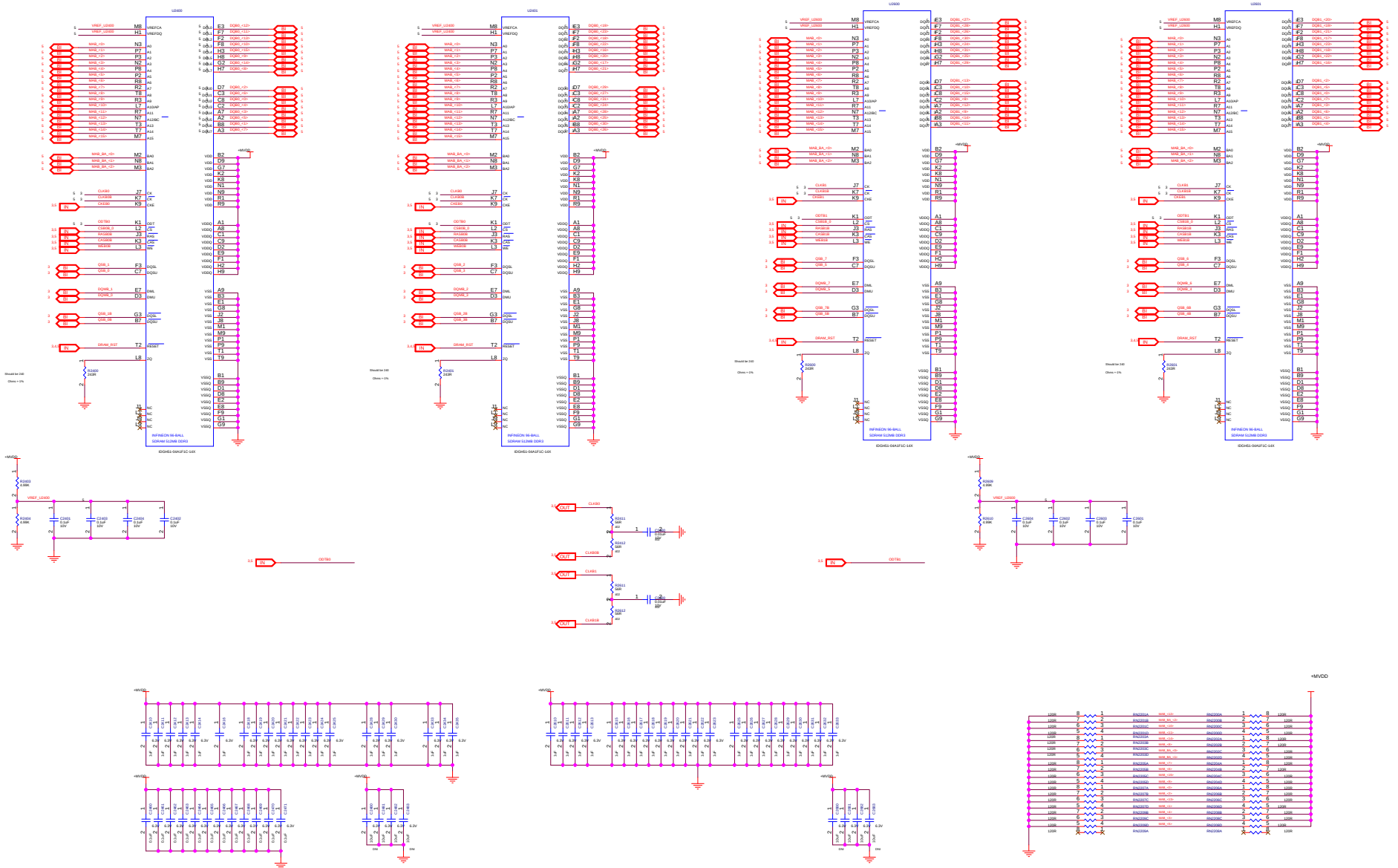
MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: Oland MEMORY INTERFACE	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 3 of 20	

(4) DDR3 Memory Channel A



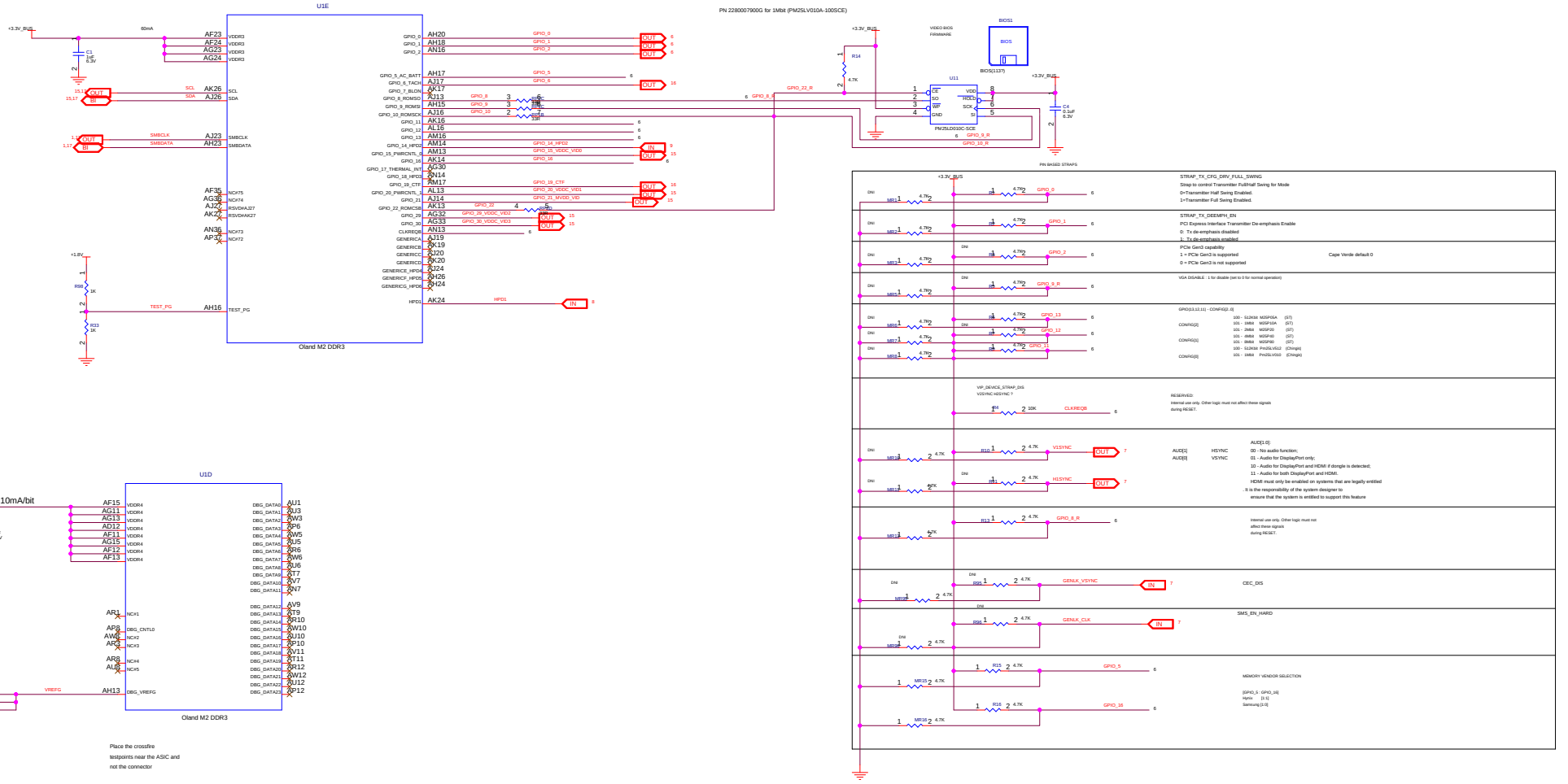
MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: DDR3 CHA	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 4 of 20	

(5) DDR3 Memory Channel B

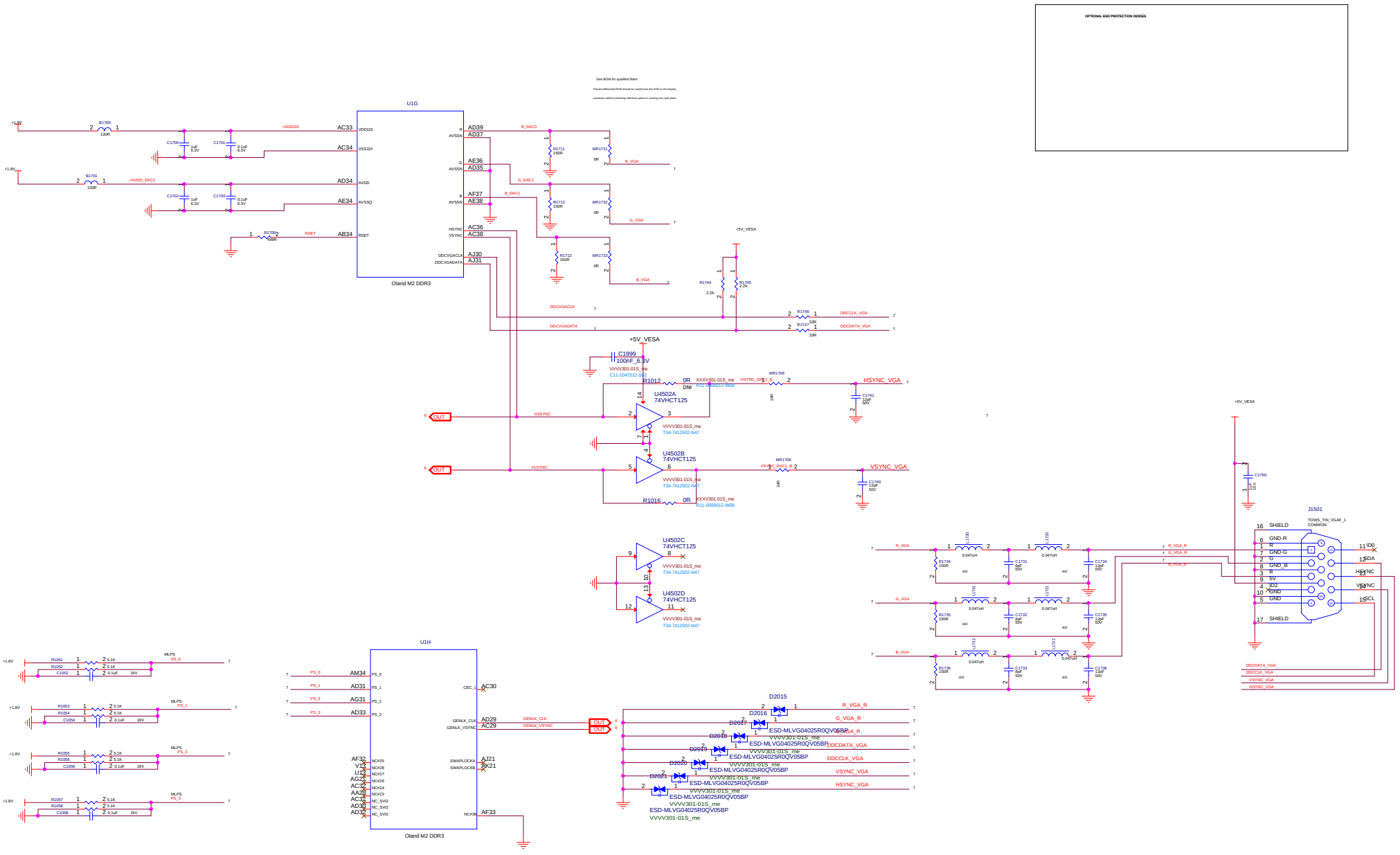


MICRO-STAR INT'L CO.,LTD			
MS-V301			
Size: Custom	Document Description: DDR3 CHB		Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 5 of 20		

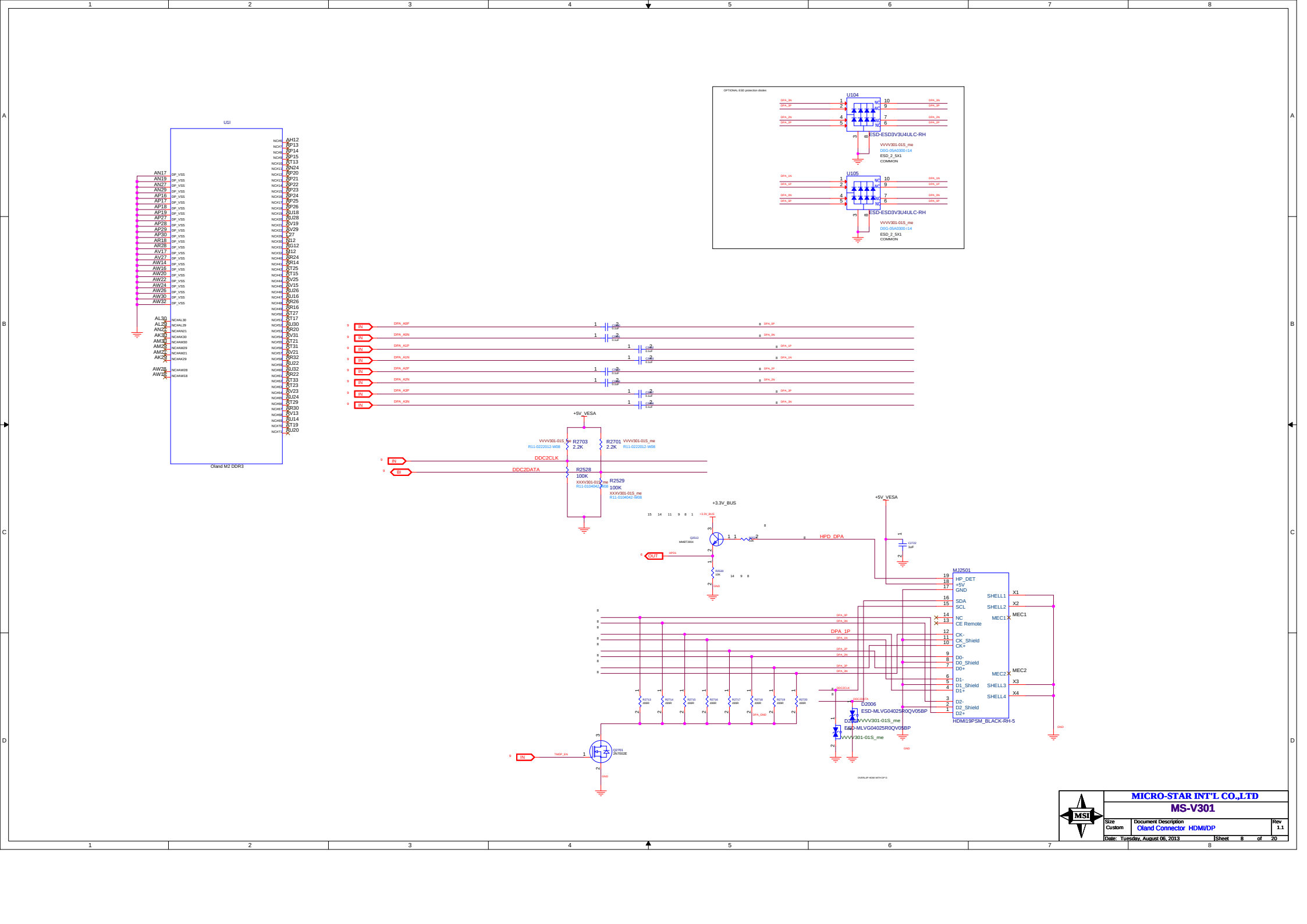
Oland XT M2 GPIOs Strap CF XTAL OSC

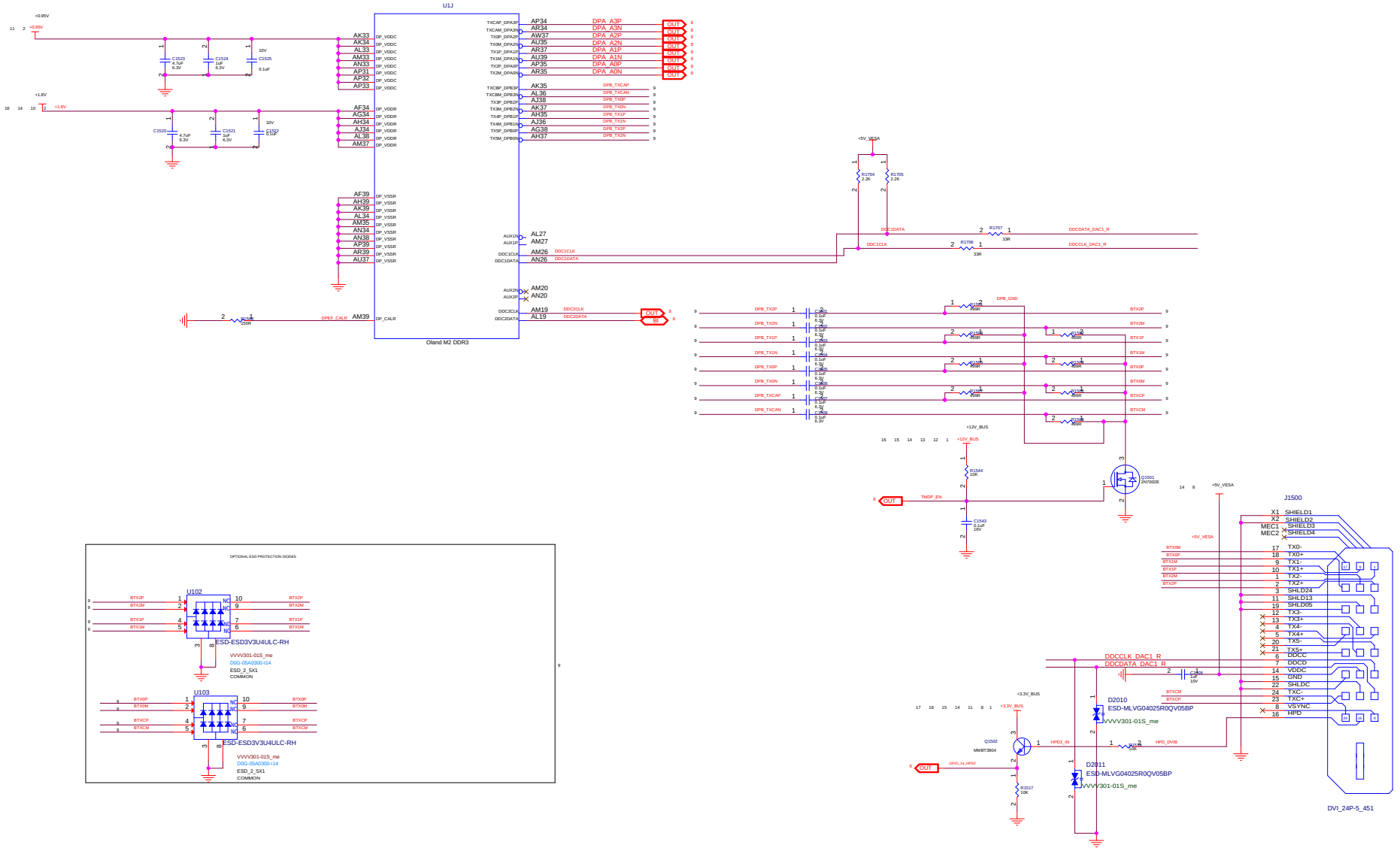


MICRO-STAR INT'L CO.,LTD	
MS-V301	
Size: Custom	Document Description: Oland GPIO STRAP PLL
Rev: 1.1	
Date: Tuesday, August 06, 2013	Sheet 6 of 20

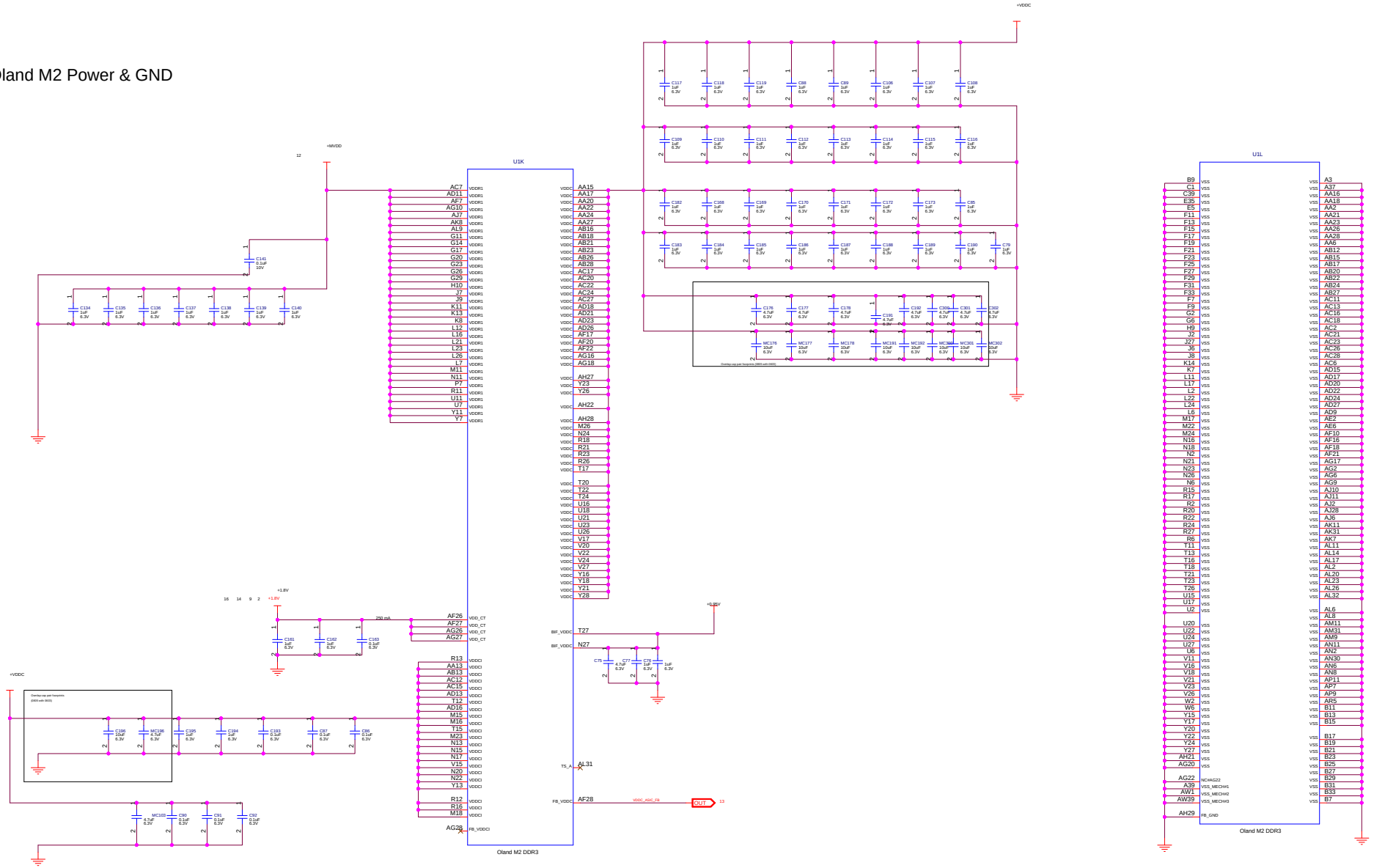


MICRO-STAR INT'L CO.,LTD	
MS-V301	
Size: Custom	Document Description: Oland DAC and MLPS
Rev: 1.1	
Date: Tuesday, August 06, 2013	Sheet 7 of 20

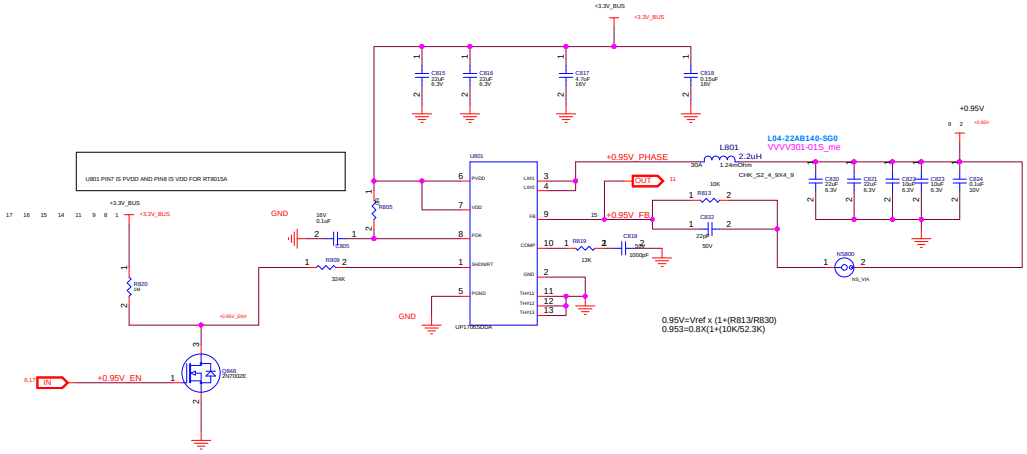

U1I
Oland M2 DDR3
OPTIONAL ESD protection diodes
U104
U105
ESD-ESD3V3U4ULC-RH
VVVV301-01S_me
DDG-05A0300-I14
ESD_2_SX1
COMMON
+5V_VESA
+3.3V_BUS
DDC2CLK
DDC2DATA
HPD_DPA
DPA_1P
MJ2501
HP_DET
+5V
GND
SDA
SCL
NC
CE Remote
CK-
CK_Shield
CK+
D0-
D0_Shield
D0+
D1-
D1_Shield
D1+
D2-
D2_Shield
D2+
SHELL1
SHELL2
SHELL3
SHELL4
MEC1
MEC2
HDMI19PSM_BLACK-RH-5
D2006
ESD-MLVG04025R0QV05BP
MICRO-STAR INT'L CO.,LTD
MS-V301
Size
Custom
Document Description
Oland Connector HDMI/DP
Rev
1.1
Date: Tuesday, August 06, 2013
Sheet 8 of 20


U1J
Oland M2 DDR3
J1500
DVI_24P-5_451
OPTIONAL ESD PROTECTION DIODES
U102
U103
ESD-ESD3V3U4ULC-RH
D2010
D2011
ESD-MLVG04025R0QV05BP
MICRO-STAR INT'L CO.,LTD
MS-V301
Oland TMDP sDVI
Tuesday, August 06, 2013

Oland M2 Power & GND

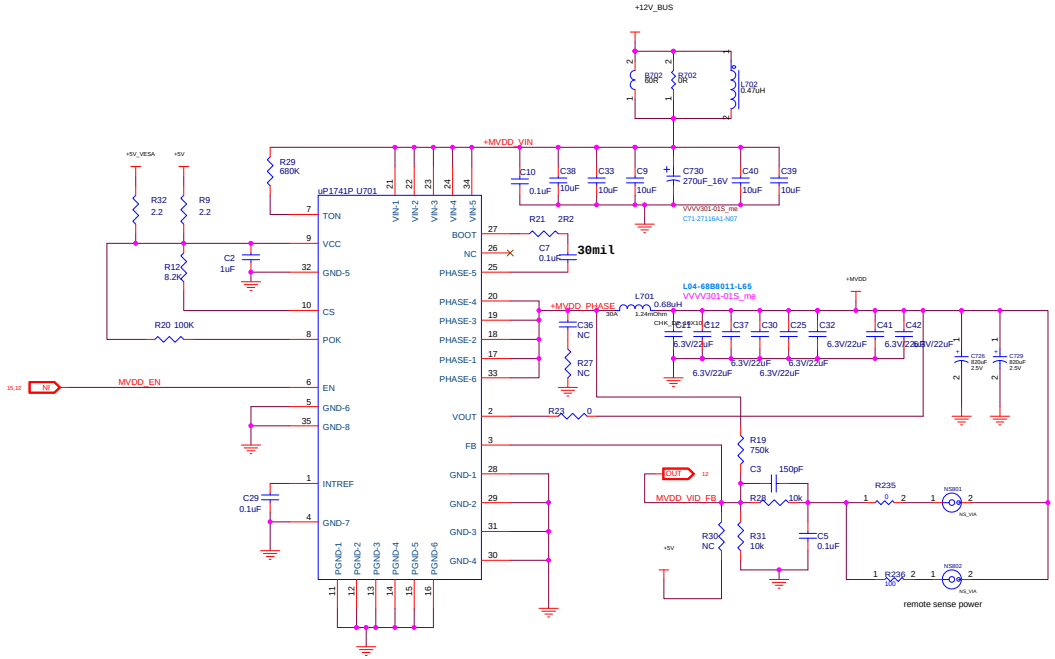


MICRO-STAR INT'L CO.,LTD			
MS-V301			
Size: Custom	Document Description: Oland Power&GND		Rev: 1.1
Date: Tuesday, August 06, 2013		Sheet 10 of 20	

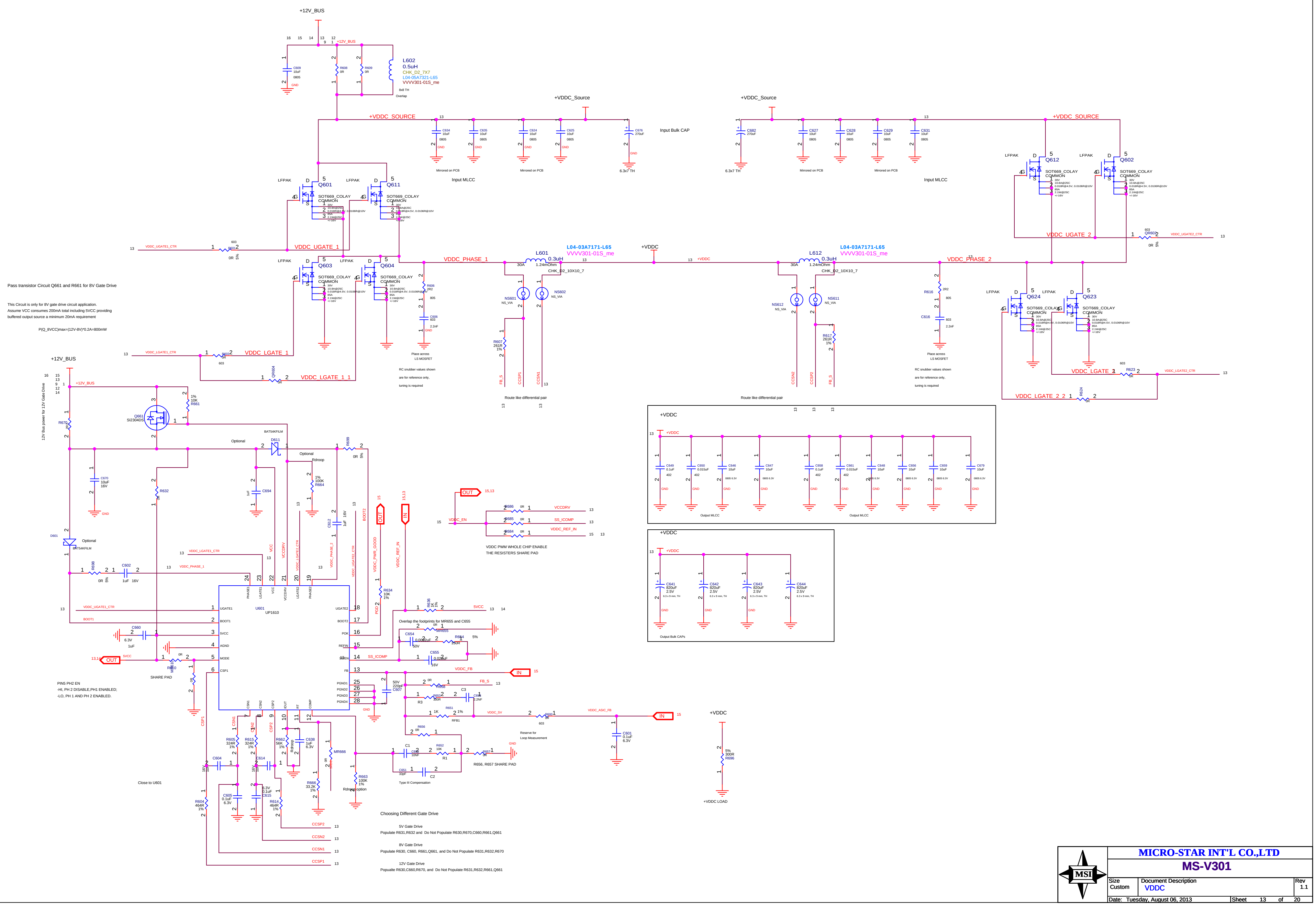


MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: 0.95V	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 11 of 20	

MVDD



MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: MVDD	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 12 of 20	



+12V_BUS
L602
0.5uH
CHK_D2_7X7
L04-05A7321-L65
VVVV301-01S_me
+VDDC_Source
+VDDC_SOURCE
Input Bulk CAP
Mirrored on PCB
Input MLCC
6.3x7 TH
Q601
Q611
Q603
Q604
Q612
Q602
Q624
Q623
SOT669_COLAY
COMMON
LFPAK
VDDC_UGATE_1
VDDC_UGATE_2
VDDC_PHASE_1
VDDC_PHASE_2
VDDC_LGATE_1
VDDC_LGATE_1_1
VDDC_LGATE_2_1
VDDC_LGATE_2_2
L601
0.3uH
1.24mOhm
CHK_D2_10X10_7
L04-03A7171-L65
VVVV301-01S_me
L612
+VDDC
Pass transistor Circuit Q661 and R661 for 8V Gate Drive
This Circuit is only for 8V gate drive circuit application.
Assume VCC consumes 200mA total including 5VCC providing
buffered output source a minimum 20mA requirement
P(Q_8VCC)max=(12V-8V)*0.2A=800mW
Place across
LS MOSFET
RC snubber values shown
are for reference only,
tuning is required
Route like differential pair
12V Bus power for 12V Gate Drive
Q661
SI2304DS
BAT54KFILM
Optional
Rdroop
Output MLCC
Output Bulk CAPs
VDDC PWM WHOLE CHIP ENABLE
THE RESISTERS SHARE PAD
U601
UP1610
SHARE PAD
PIN5 PH2 EN
-HI, PH 2 DISABLE,PH1 ENABLED;
-LO, PH 1 AND PH 2 ENABLED.
Overlap the footprints for MR655 and C655
Reserve for
Loop Measurement
R656, R657 SHARE PAD
Type III Compensation
Close to U601
Rdroop option
+VDDC LOAD
Choosing Different Gate Drive
5V Gate Drive
Populate R631,R632 and Do Not Populate R630,R670,C660,R661,Q661
8V Gate Drive
Populate R630, C660, R661,Q661, and Do Not Populate R631,R632,R670
12V Gate Drive
Populate R630,C660,R670, and Do Not Populate R631,R632,R661,Q661
MICRO-STAR INT'L CO.,LTD
MS-V301
Size
Custom
Document Description
VDDC
Rev
1.1
Date: Tuesday, August 06, 2013
Sheet 13 of 20

Linear Regulators

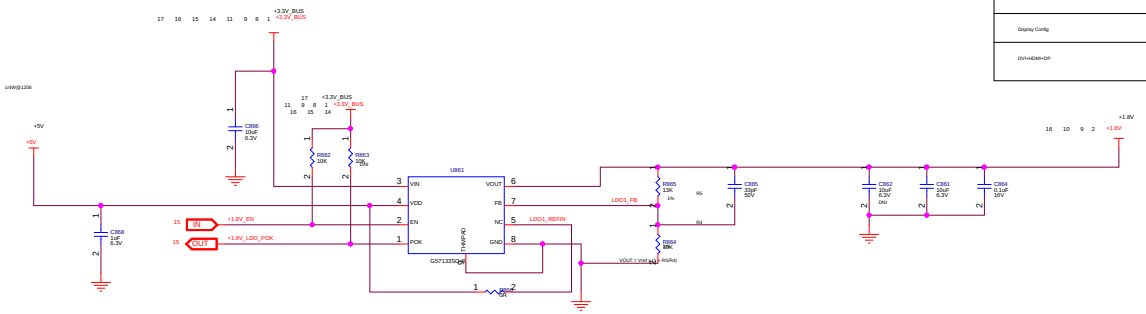
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX

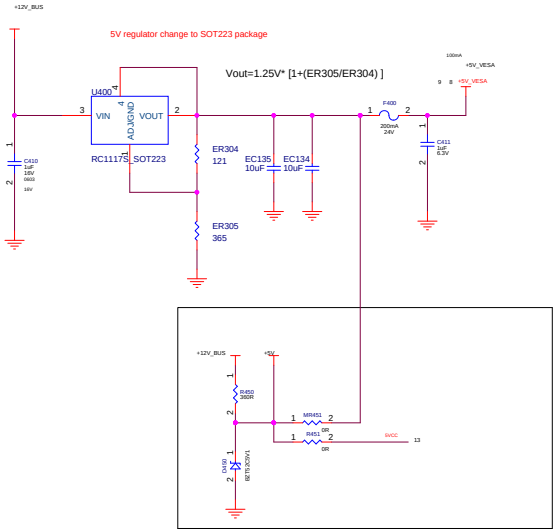
PCB: 50 to 70mm sq. copper area for cooling

Regulators for +5V, +5V_VESA and +5V_VESA2

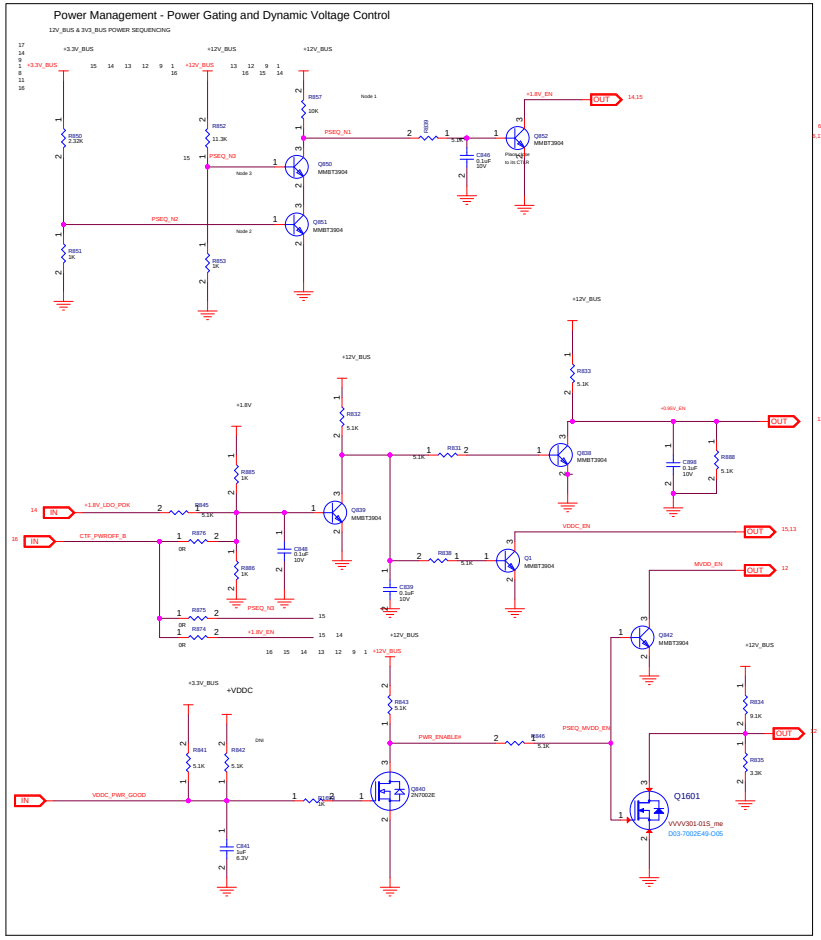
1.8V WORST-CASE REQUIREMENT

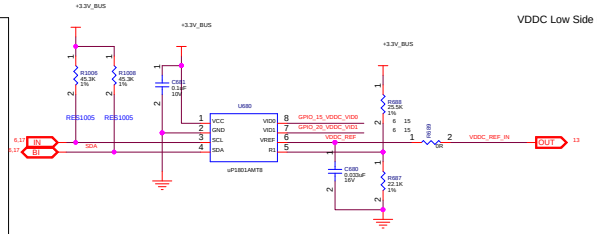
Display Config	Est. Current
DVI+HDMI+DP	1330mA



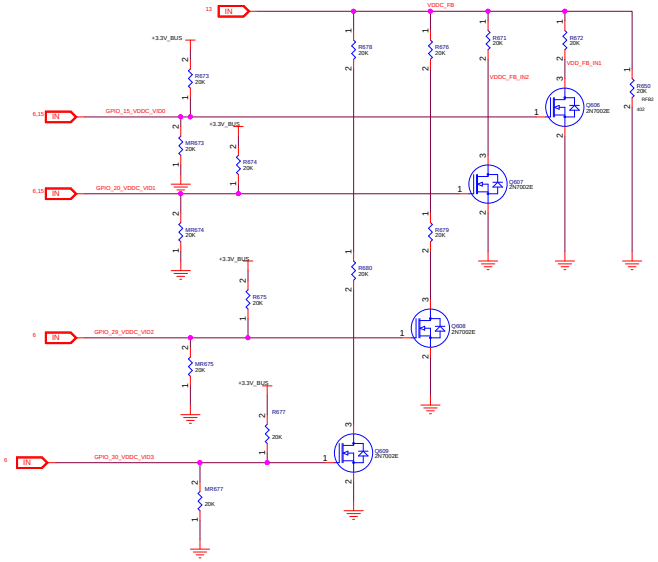


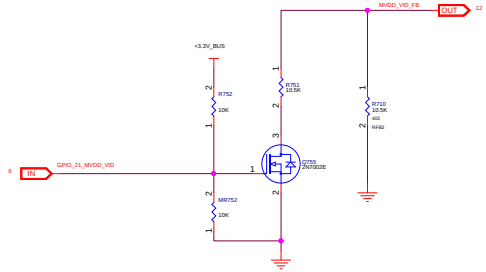
MICRO-STAR INT'L CO.,LTD			
MS-V301			
Size: Custom	Document Description: Linear Regulators		Rev: 1.1
Date: Tuesday, August 06, 2013		Sheet 14 of 20	

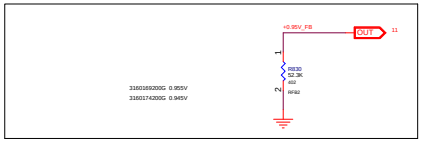




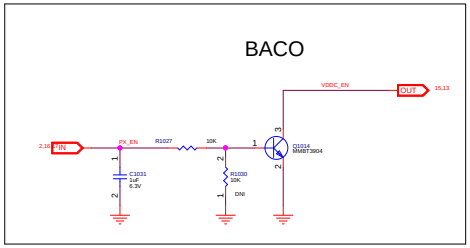
VDDC Low Side Divider







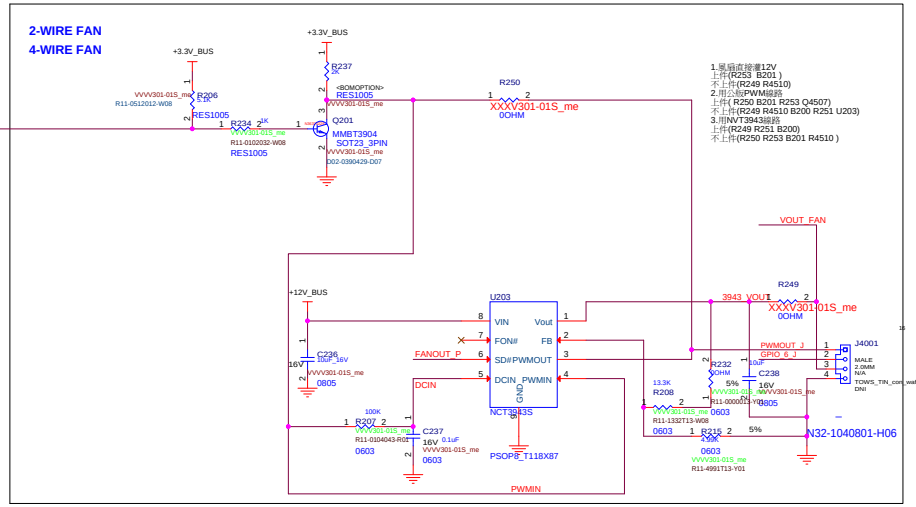
BACO

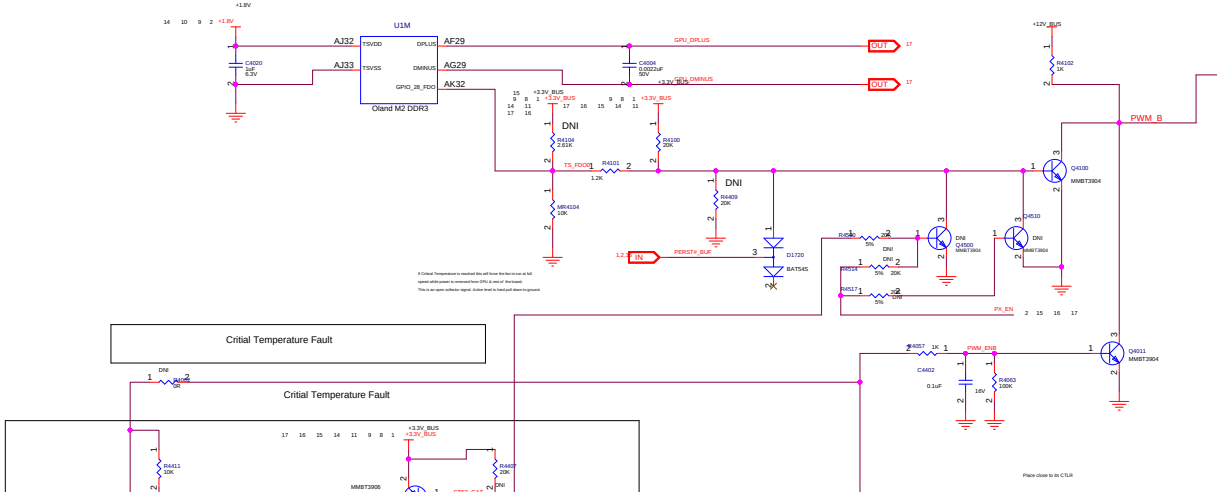


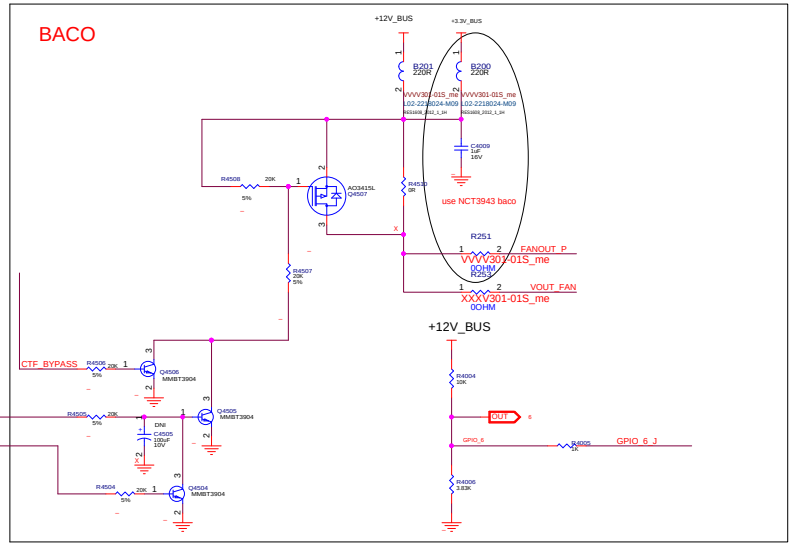
MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: PWR MGMT & SEQ	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 15 of 20	

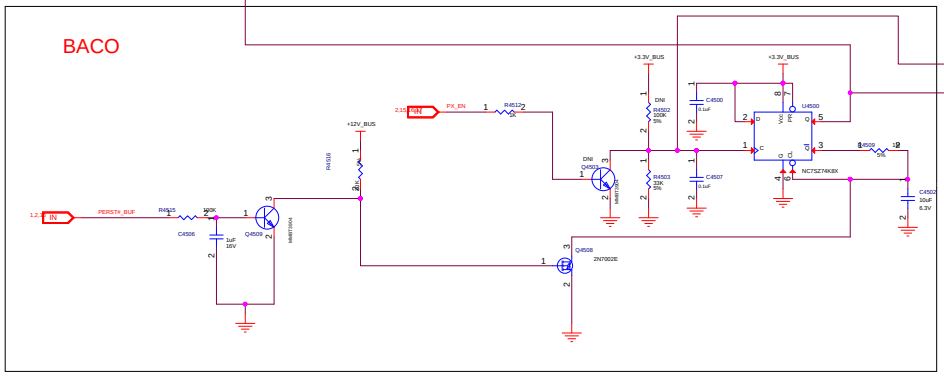
Mechanical and Thermal Management

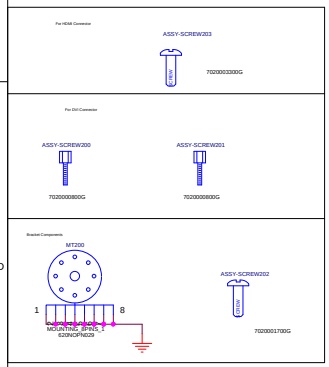
Fan Control (New)

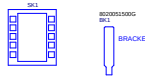






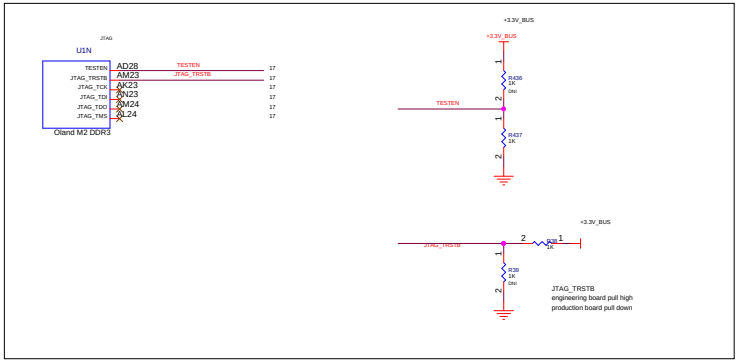






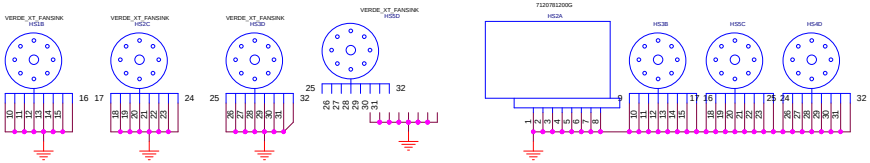
MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: Mech/Thermal Management	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 16 of 20	

(19) Debug Circuits

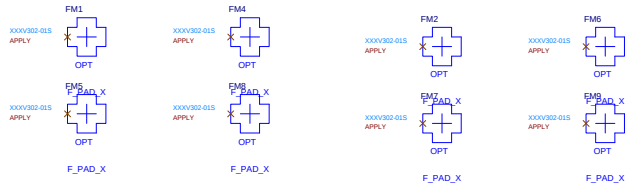


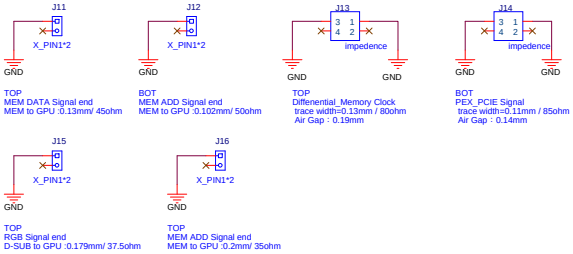
LM86163 FOR BACKUP THERMAL CONTROL

7121000100G



LED GREEN "ON" shows PX_EN

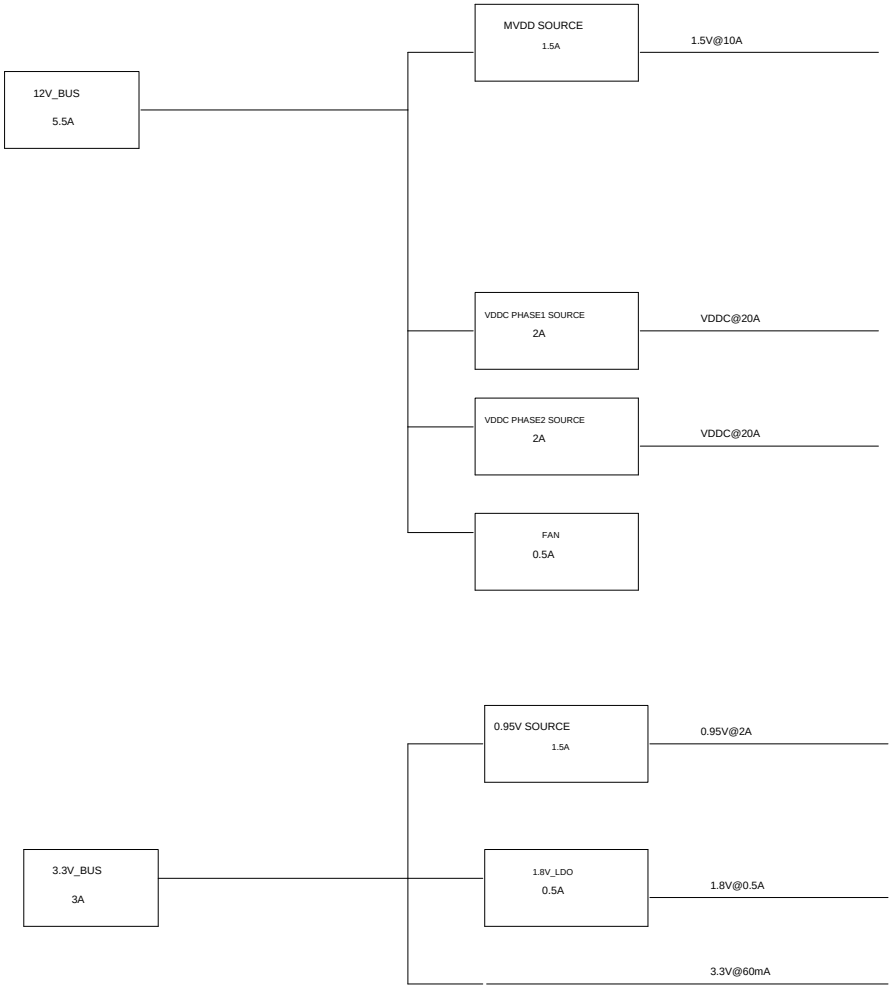




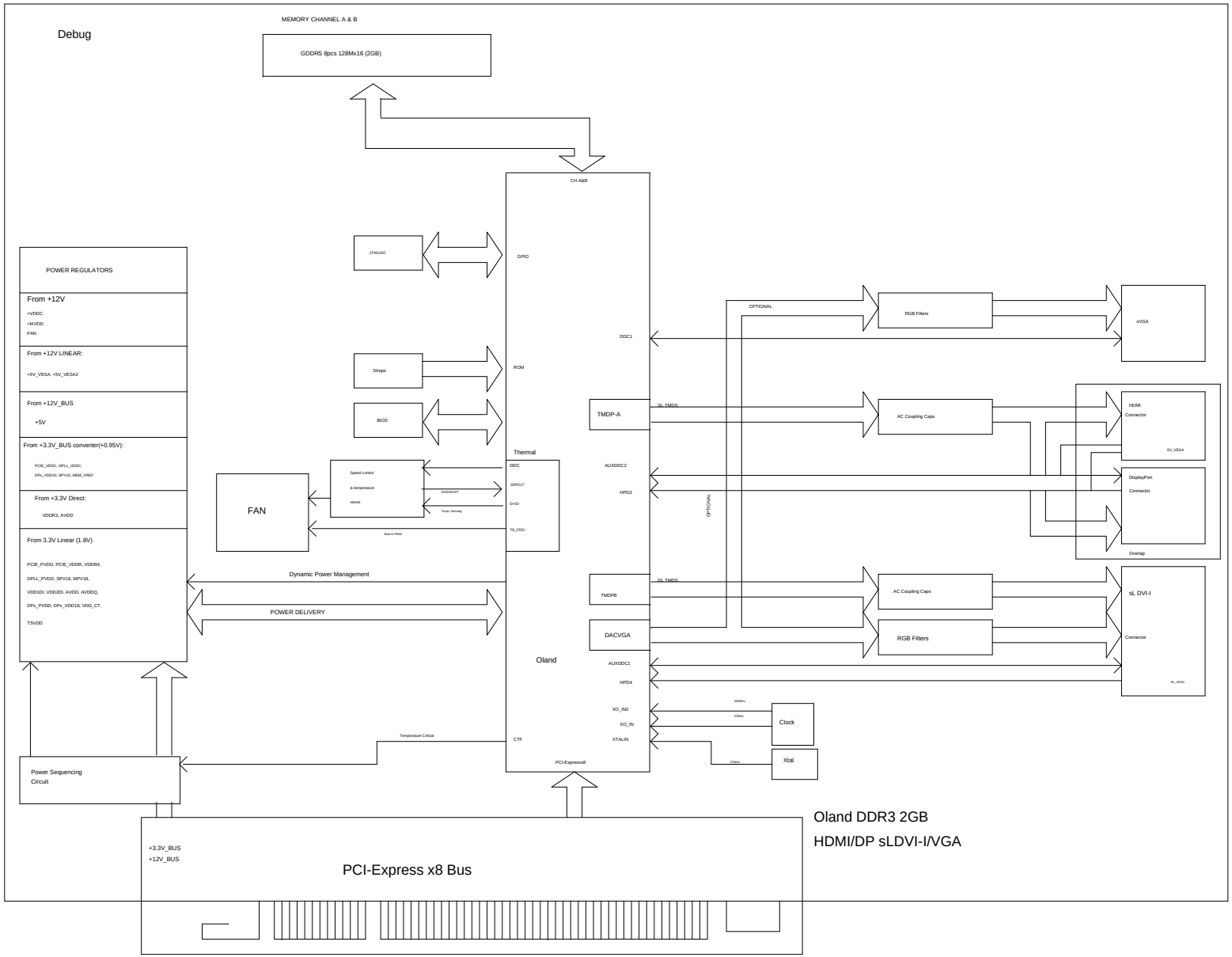
MICRO-STAR INT'L CO.,LTD	
MS-V301	
Size: Custom	Document Description: Debug Circuit
Rev: 1.1	
Date: Tuesday, August 06, 2013	Sheet 17 of 20

DVI-I	HPD2	DDC/AUX1
HDMI/DP	HPD1	DDC/AUX2

GPIO15	VDDC_VID0	
GPIO20	VDDC_VID1	
GPIO29	VDDC_VID2	
GPIO30	VDDC_VID3	
GPIO21	MVDD_VID	



MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: GPIO DDC HPD map	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 18 of 20	



MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 19 of 20	

TITLE	SCHEMATIC NO.	DATE
Oland xto DDR3 2GB SL_DVI-I+HDMI/DP+sVGA	105-C662XX-00	

REVISION HISTORY

NOTE:
THIS SCHEMATIC REPRESENTS THE PCB, IT DOES NOT REPRESENT ANY SPECIFIC SKU.
FOR STUFFING OPTIONS (COMPONENT VALUES, DNI PLEASE CONSULT THE PRODUCT SPECIFIC BOM.
PLEASE CONTACT AMD REPRESENTATIVE TO OBTAIN LASTEST BOM CLOSEST TO THE APPLICATION DESIRED.

REV P00

SCH REV	PCB REV	DATE	REVISION DESCRIPTION
00	00A	2012/08/20	Initial Oland XT schematic based on C552 C550&C469
00	00	2013/03/27	Upgrade PCB to 00 without Schematic change
01			
		2013/07/02	1. Page 03~05 : Add <> in memory DQA_ 2. Page 07: chagne connector to black type 3. Page 08: remove DP & add ESD 4. Page 09 : add ESD 5. Page 11 : U801 change to UP1706 6. Page 12 : U701 change to UP1741P 7. Page 13 : U601 change to UP1610 8. Page 15 : add MVDD_EN circuit , add SCL SDA pull high R 9. Page 16 : add NCT3943 in FAN control

MICRO-STAR INT'L CO.,LTD

MS-V301

Size	Document Description	Rev
Custom	History	1.1

Date: Tuesday, August 06, 2013 Sheet 20 of 20