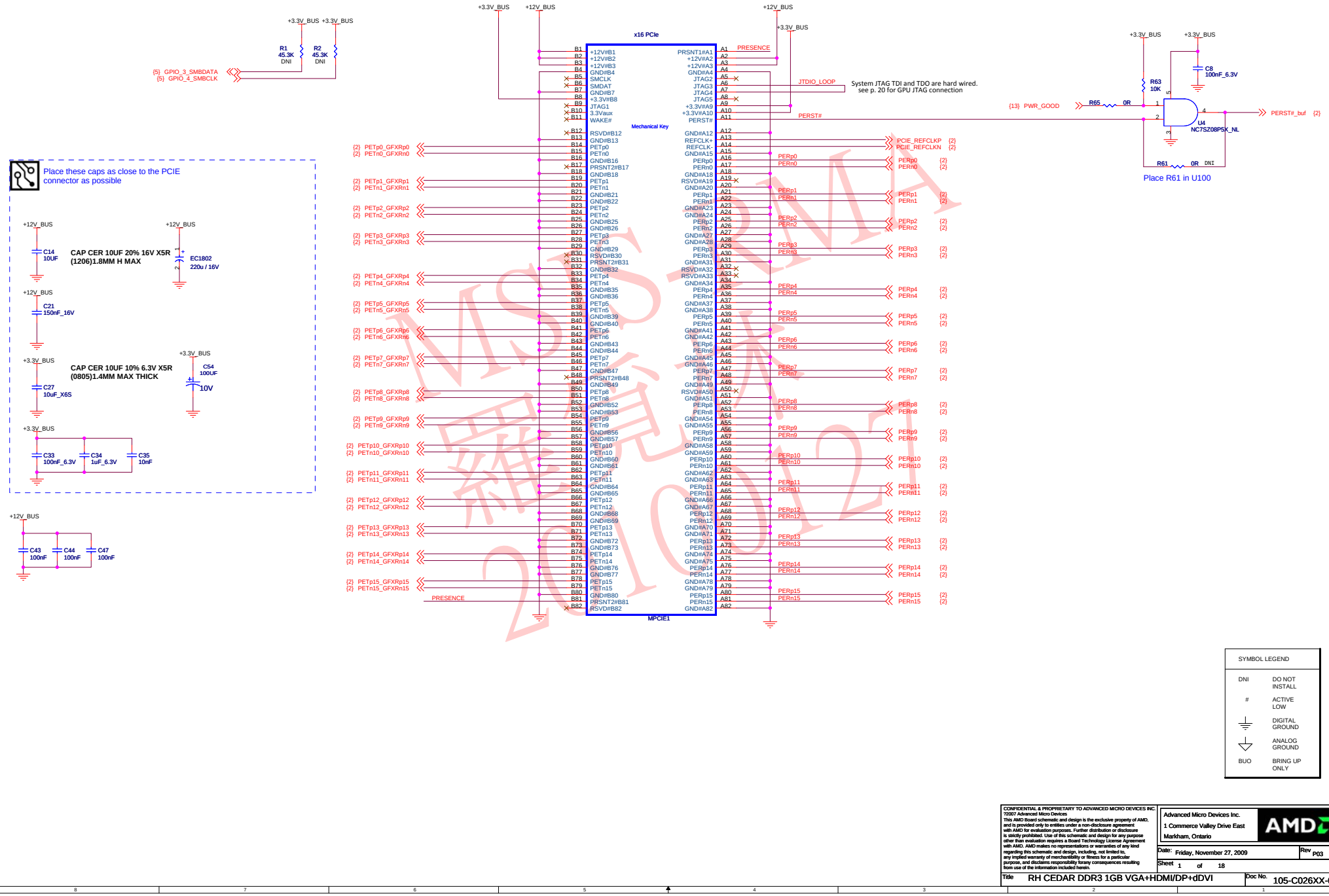
PCI-EXPRESS EDGE CONNECTOR

CEDAR BASS / PERCH



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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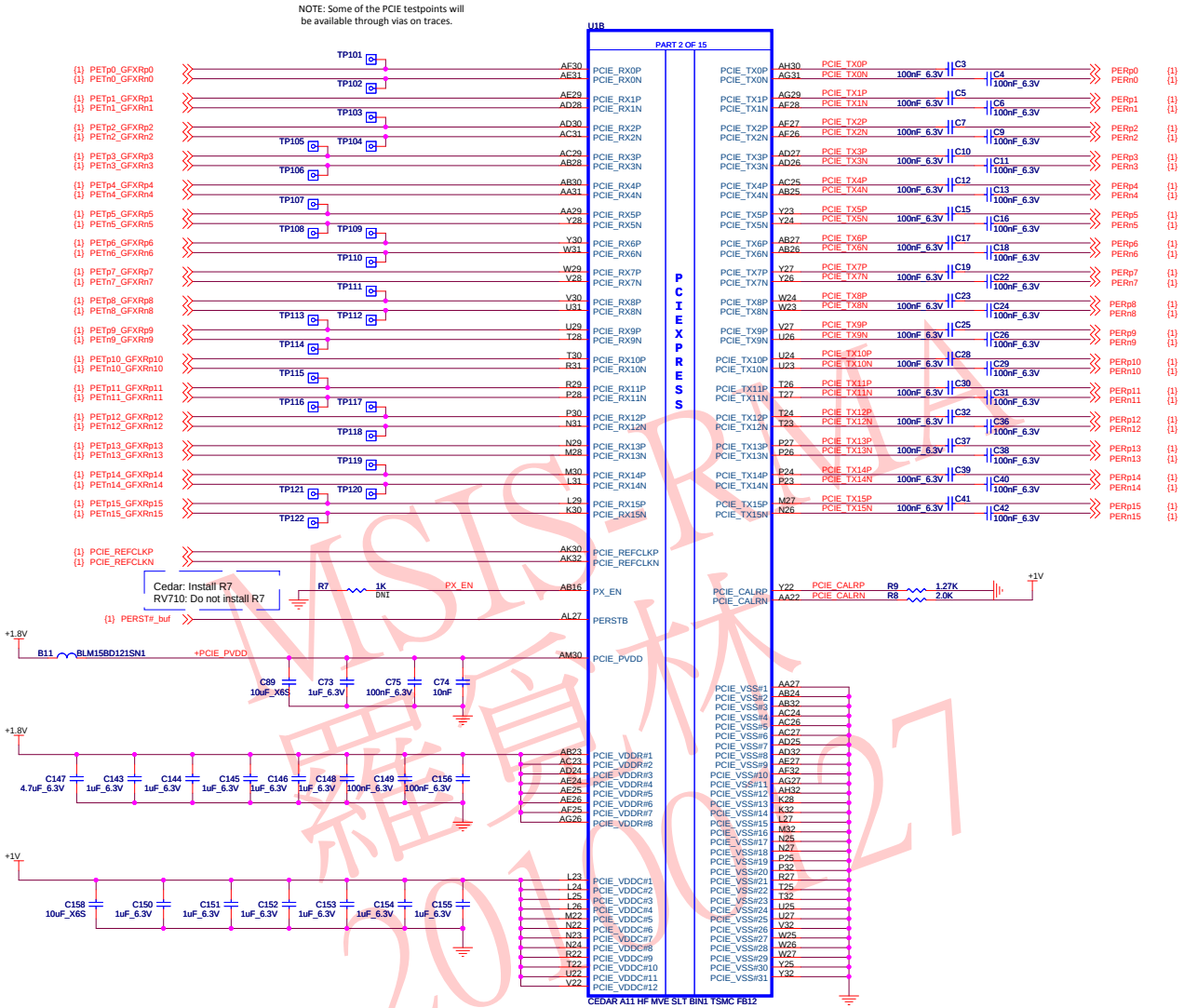
CEDAR PCIe Interface



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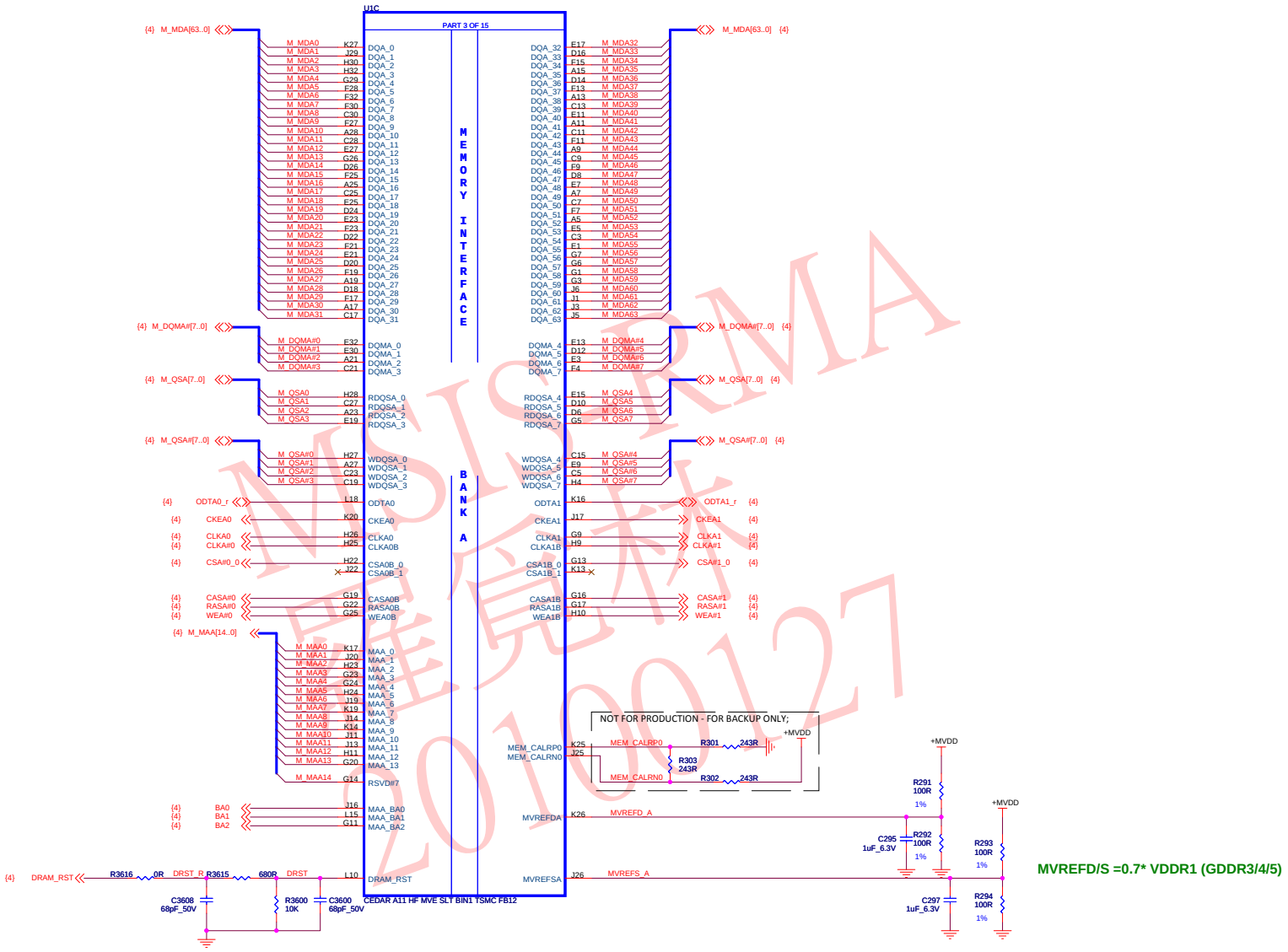
CEDAR MEM Interface Ch A&B



MVREFD/S =0.7* VDDR1 (GDDR3/4/5)

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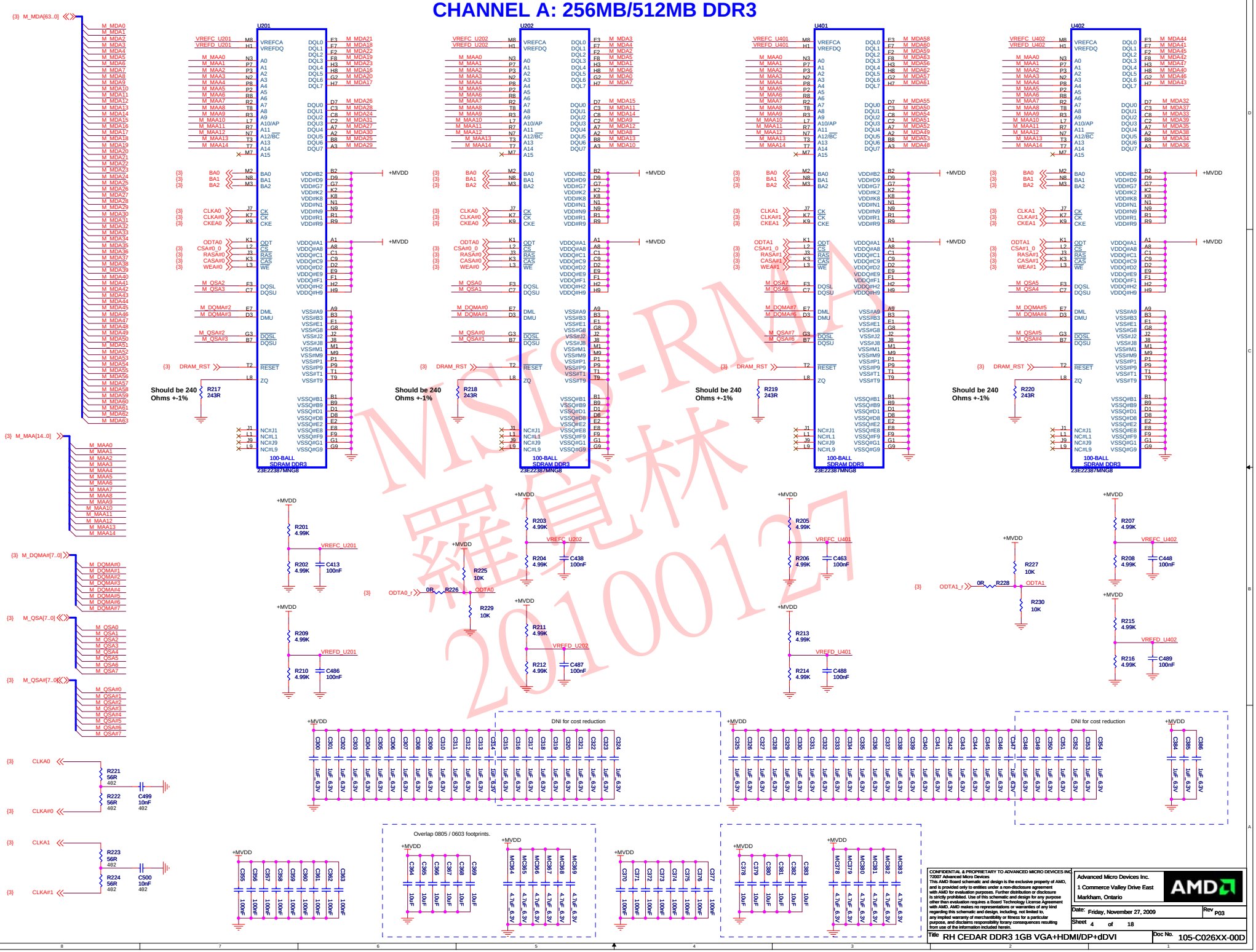
CHANNEL A: 256MB/512MB DDR3



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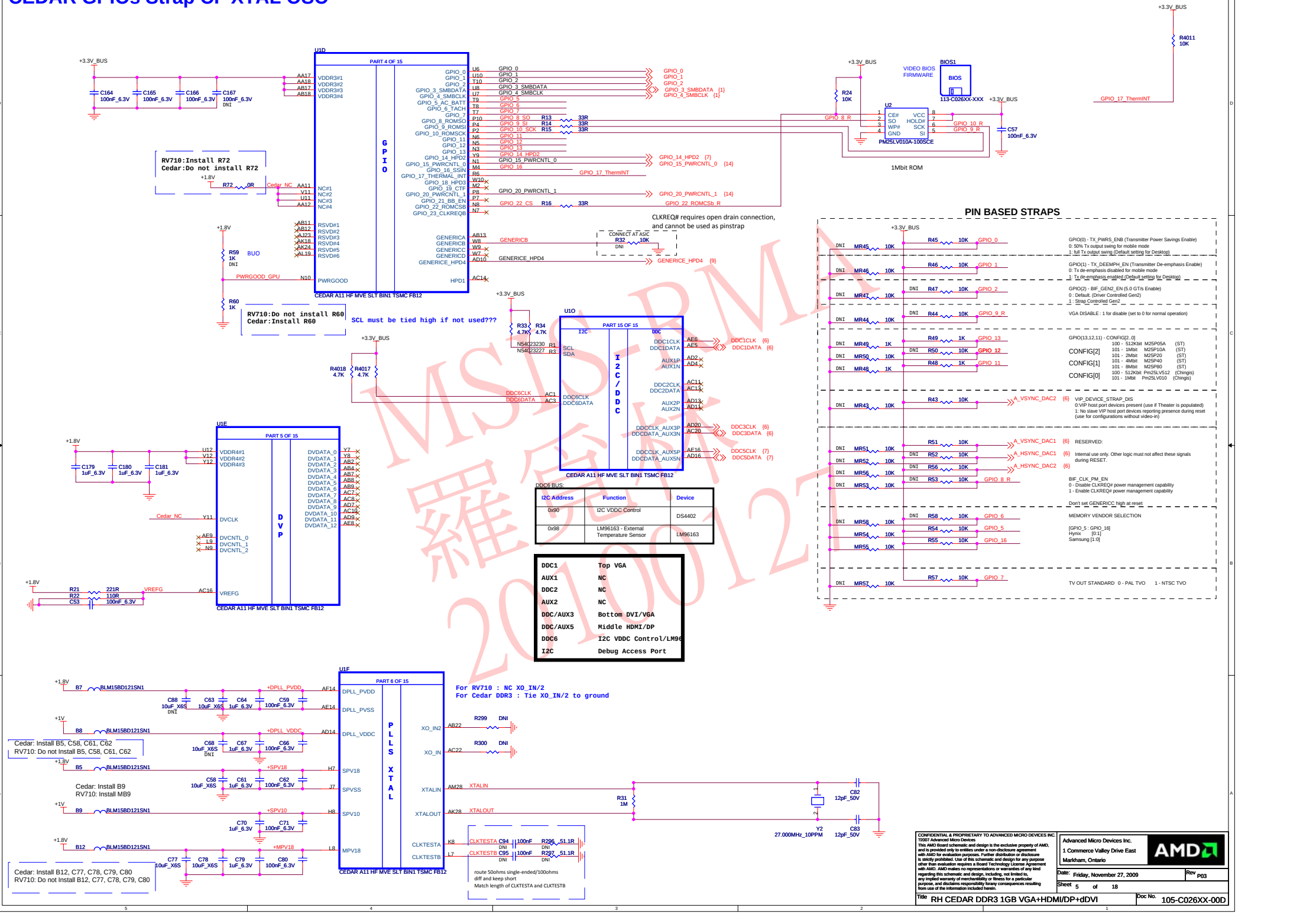
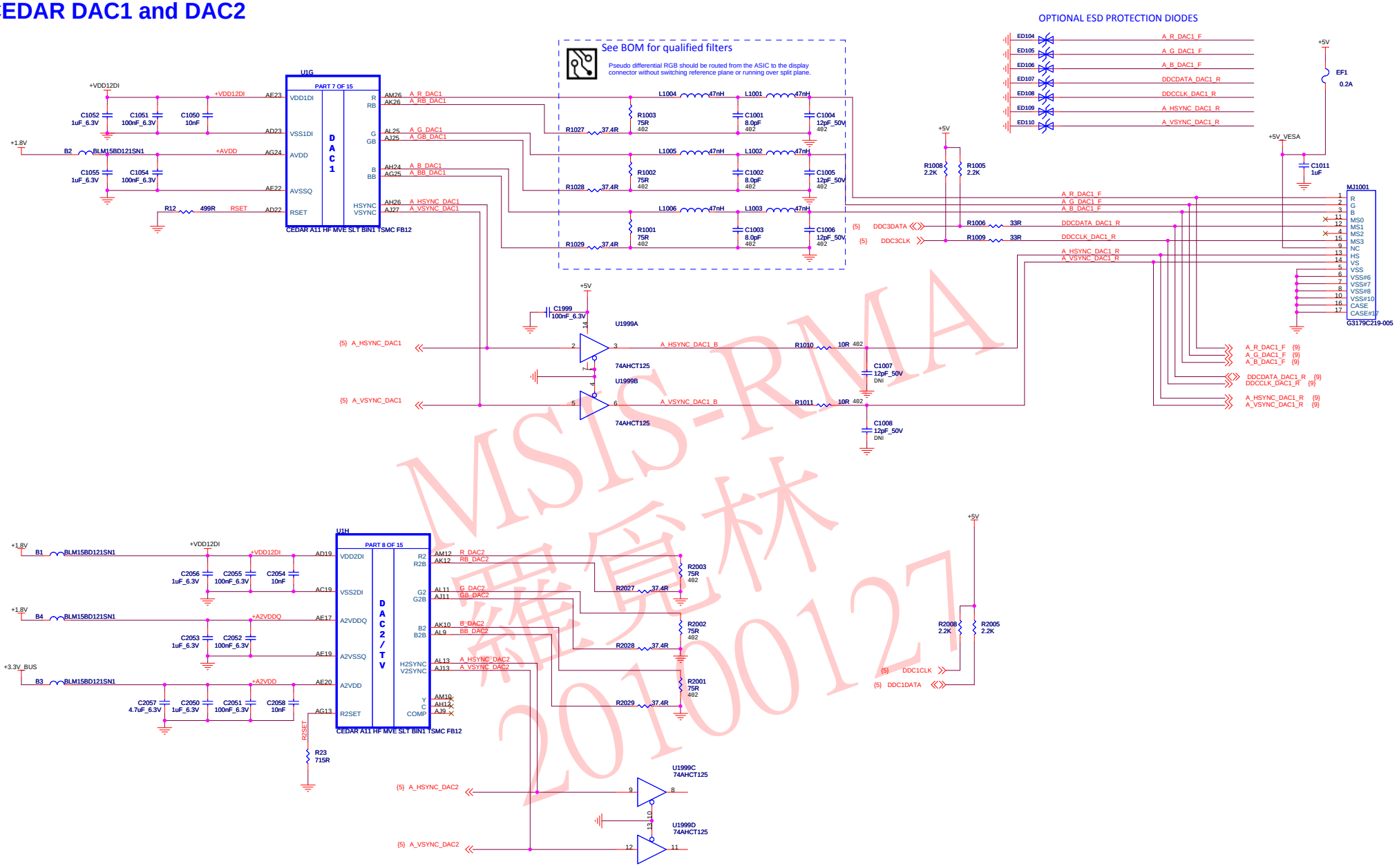
CEDAR GPIOs Strap CF XTAL OSC



CEDAR DAC1 and DAC2



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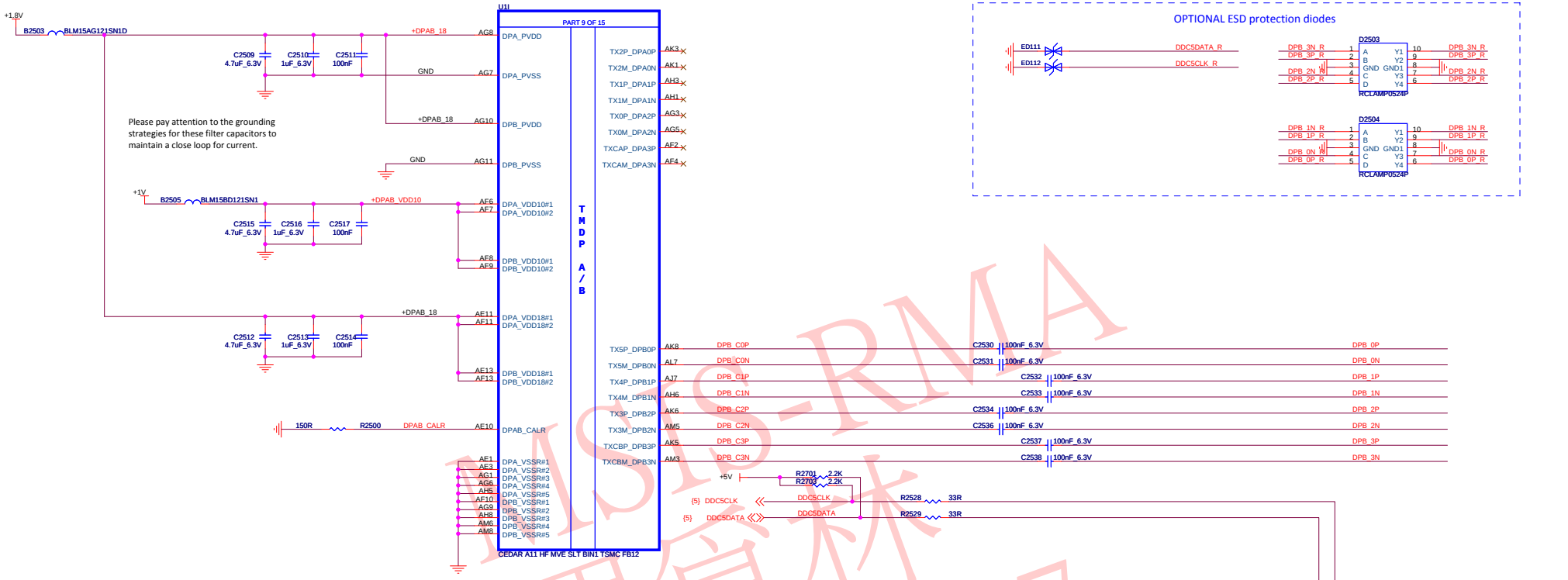
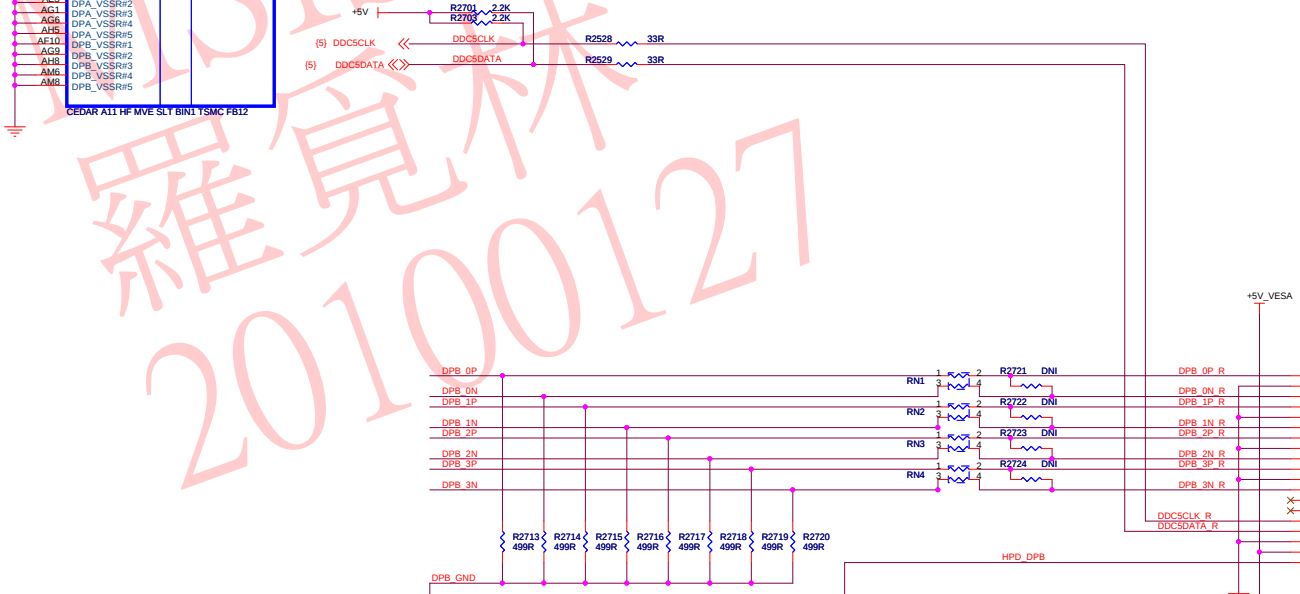
CEDAR TMDP A&B DP/HDMI OVERLAP





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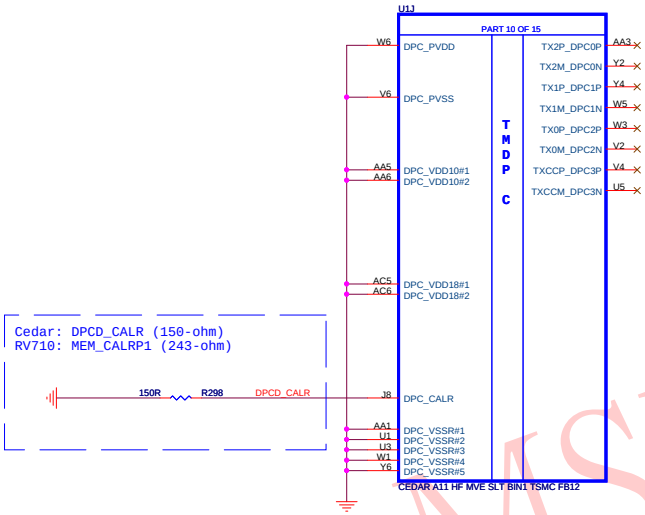
CEDAR Display Port C (Unused)



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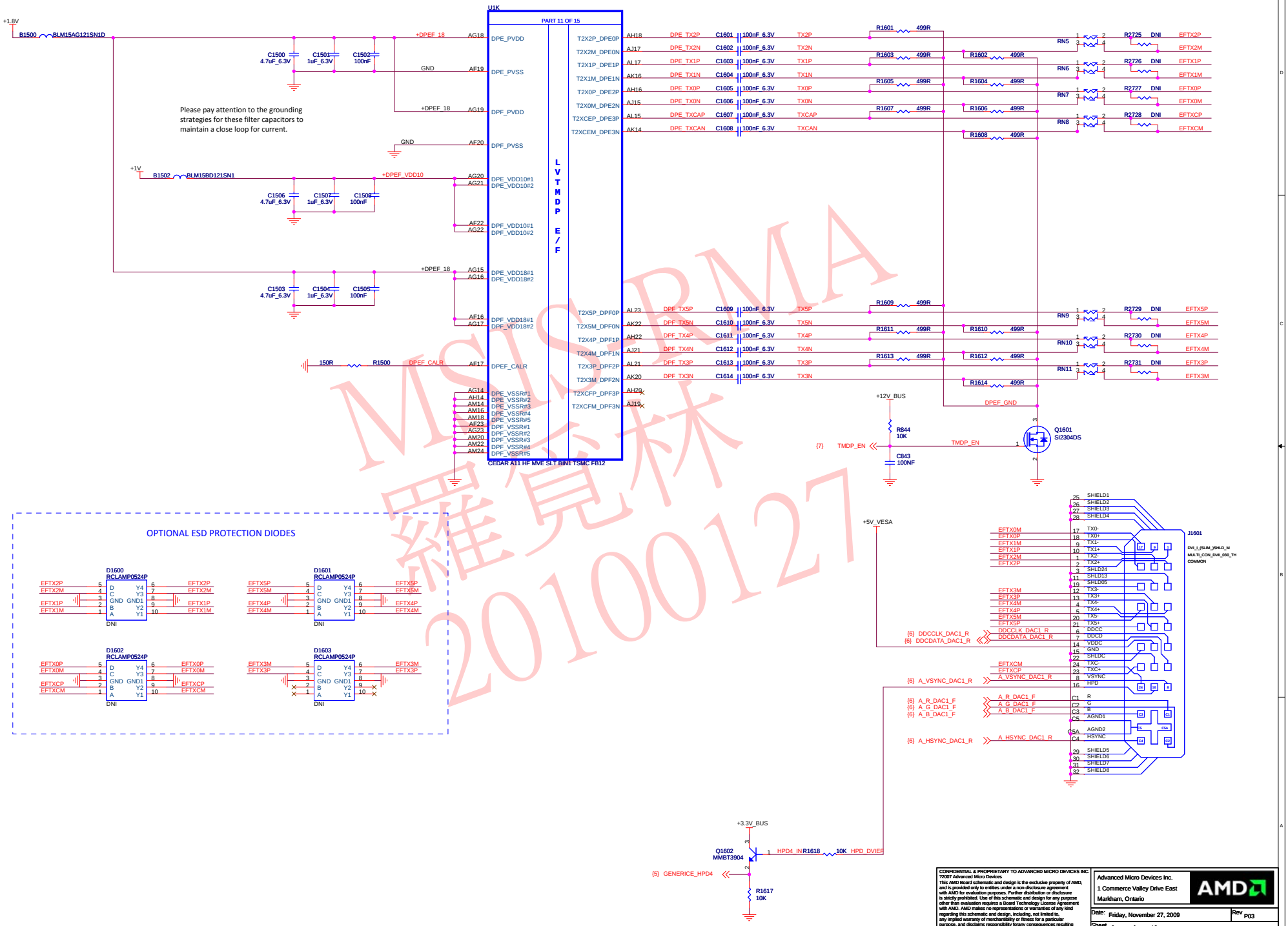
CEDAR LVTMDP E&F dDVI-I



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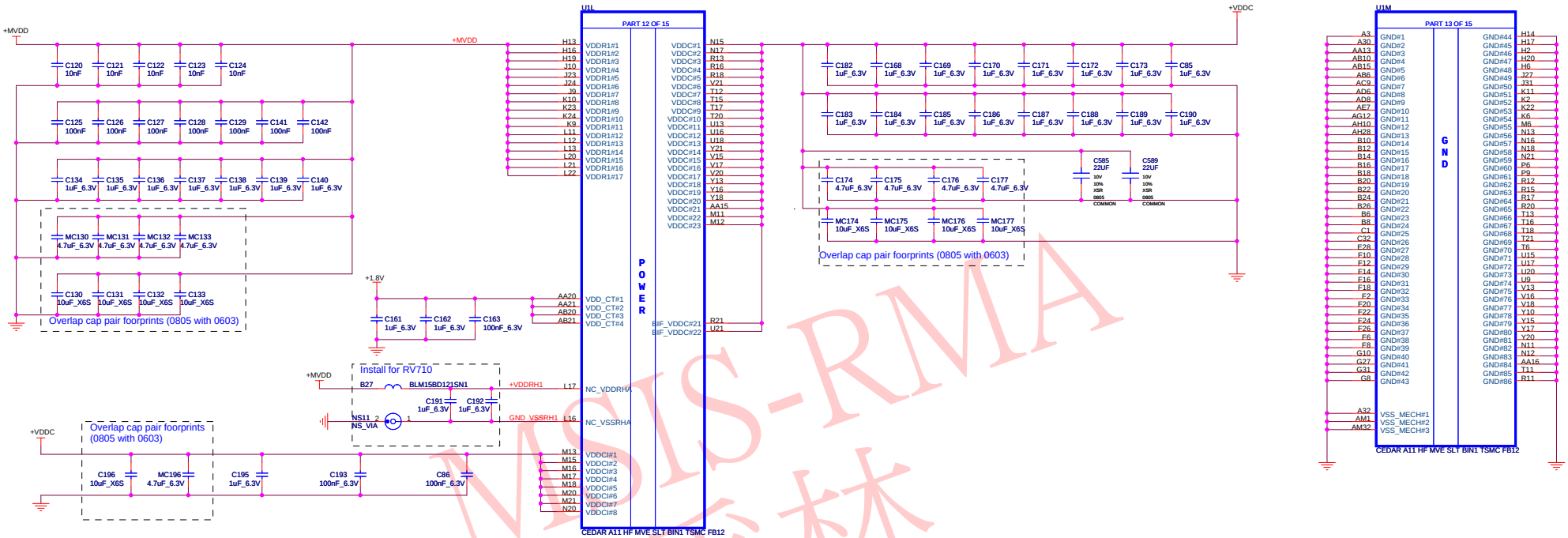
CEDAR Power & GND



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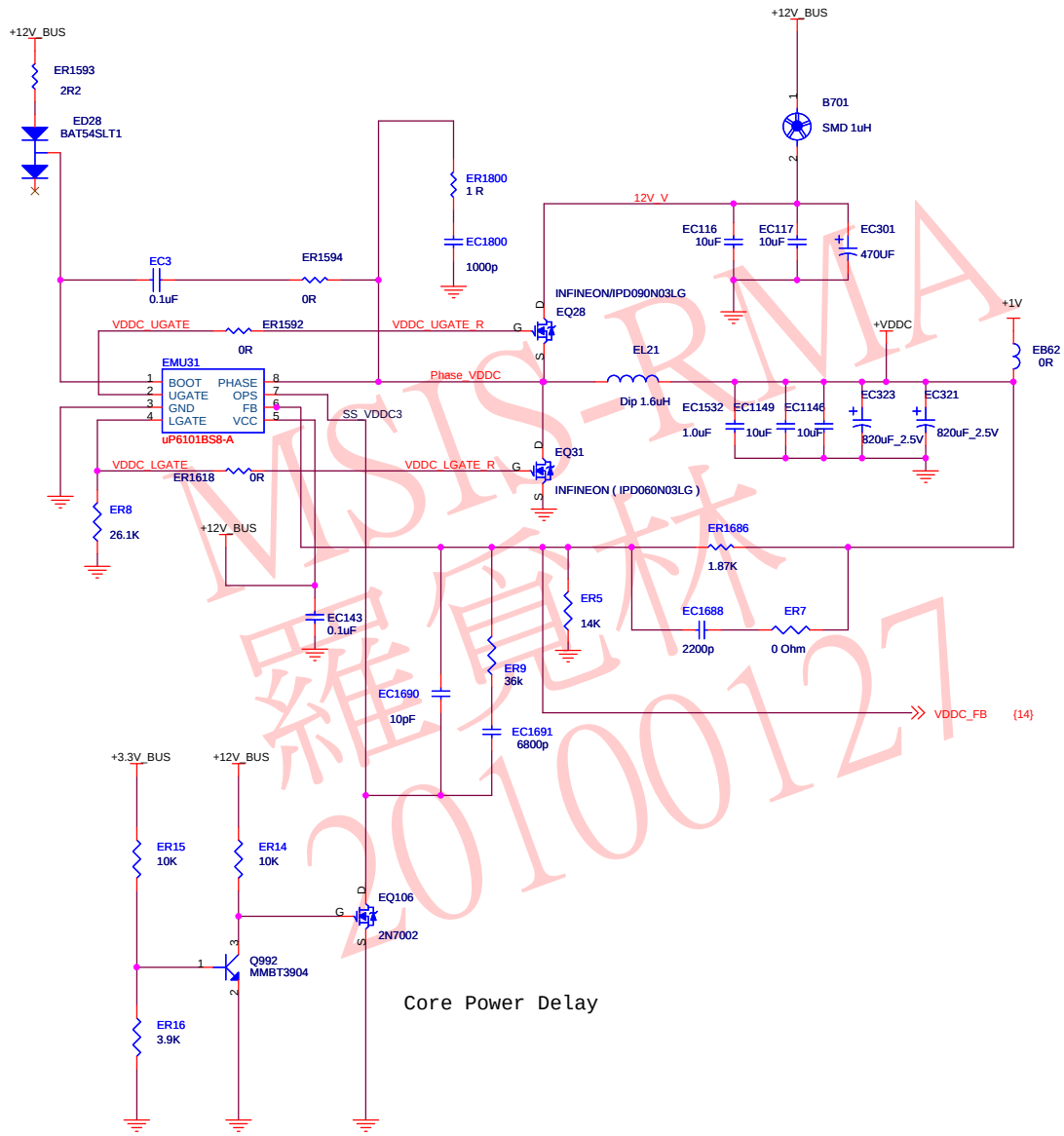

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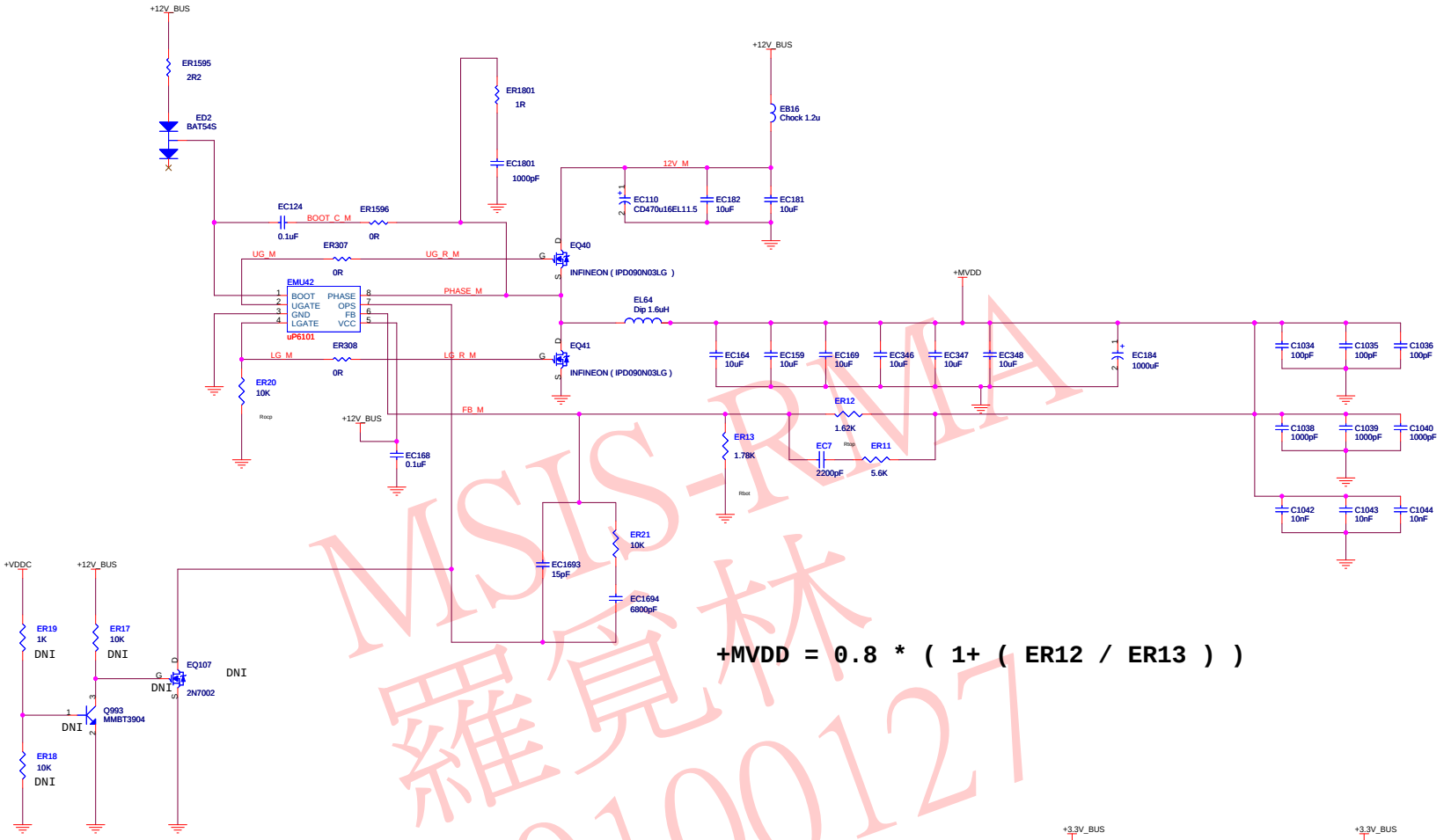

Memory Power Seq

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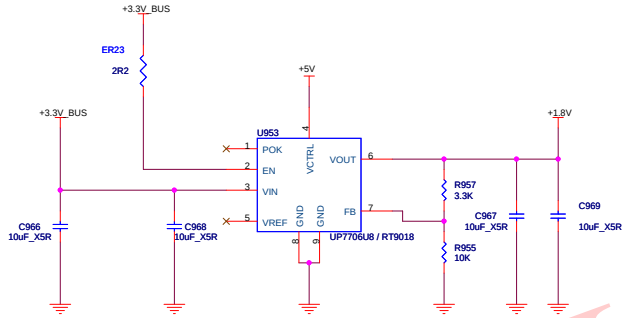
Linear Regulators

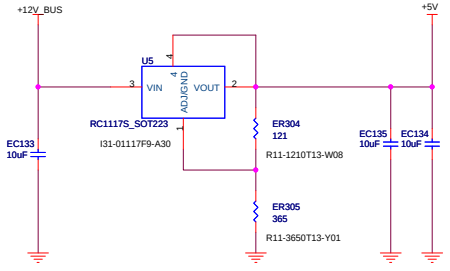
Regulators for +5V, +5V_VESA and +5V_VESA2

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

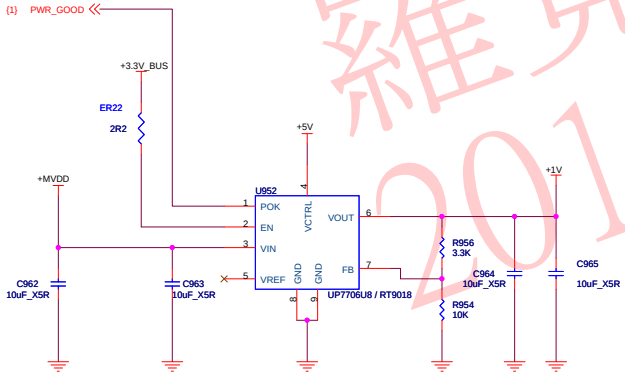
Vout=0.8V * (1+ R957 / R955)



Vout=1.25V* [1+(ER305/ER304)]

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA



Vout=0.8V * (1+ R956 / R954)

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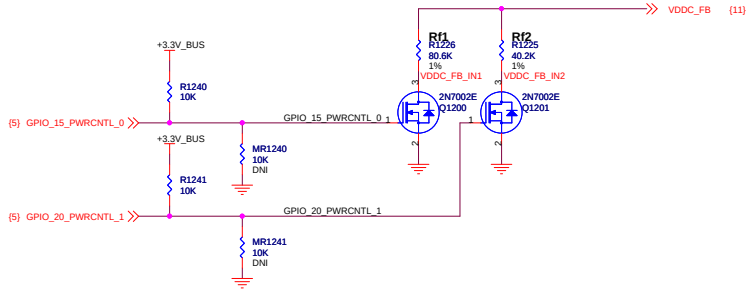
Power Management - Power Gating and Dynamic Voltage Control

VDDC Low Side Divider



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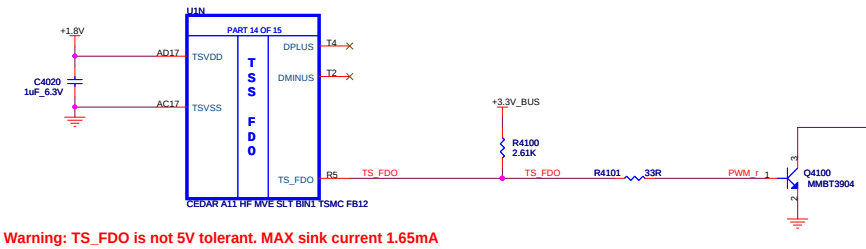
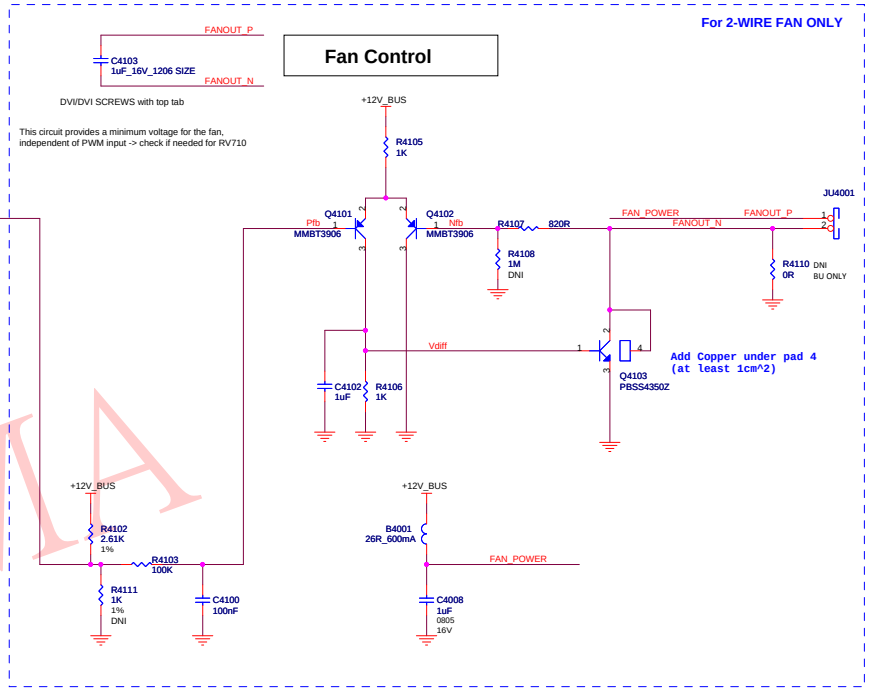
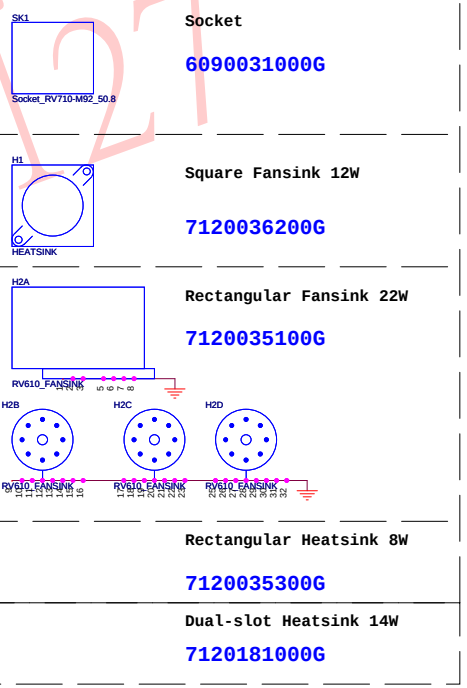
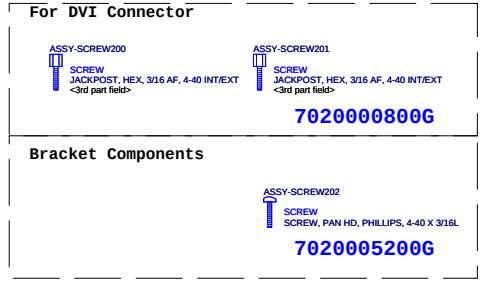
Mechanical and Thermal Management

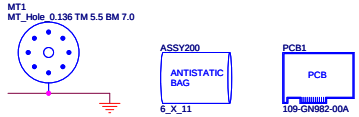


Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA









SKU		P/N	CONFIGURATION	Form Factor
	PERCH	80200513000G	DVI + DP + VGA	FH / SS
BASS		80200514000G	DVI +HDMI+ VGA	FH / SS
	PERCH	80200516000G	DVI + DP	LP / SS
BASS		80200516A0G	DVI +HDMI	LP / SS
	PERCH	80200517000G	DVI + DP + VGA	FH / DS
BASS		80200517A0G	DVI +HDMI+ VGA	FH / DS

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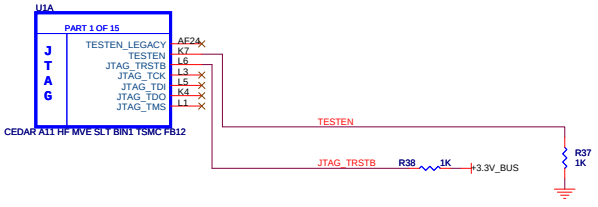
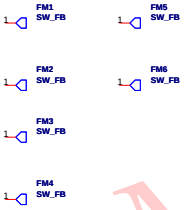
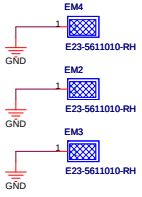
(19) Debug Circuits

JTAG





TOP Single end Address branch 50 ohm +/- 5 ohm 3.937 mils	Bottom Single end Memory data 45 ohm +/- 5 ohm 4.724 mils	TOP Different TMDS 100 ohm +/- 10 % 3.897 mils / 11.850 mils	Bottom Different PEX_PCIE 85 ohm +/- 10 % 4.921 mils / 6.889 mils



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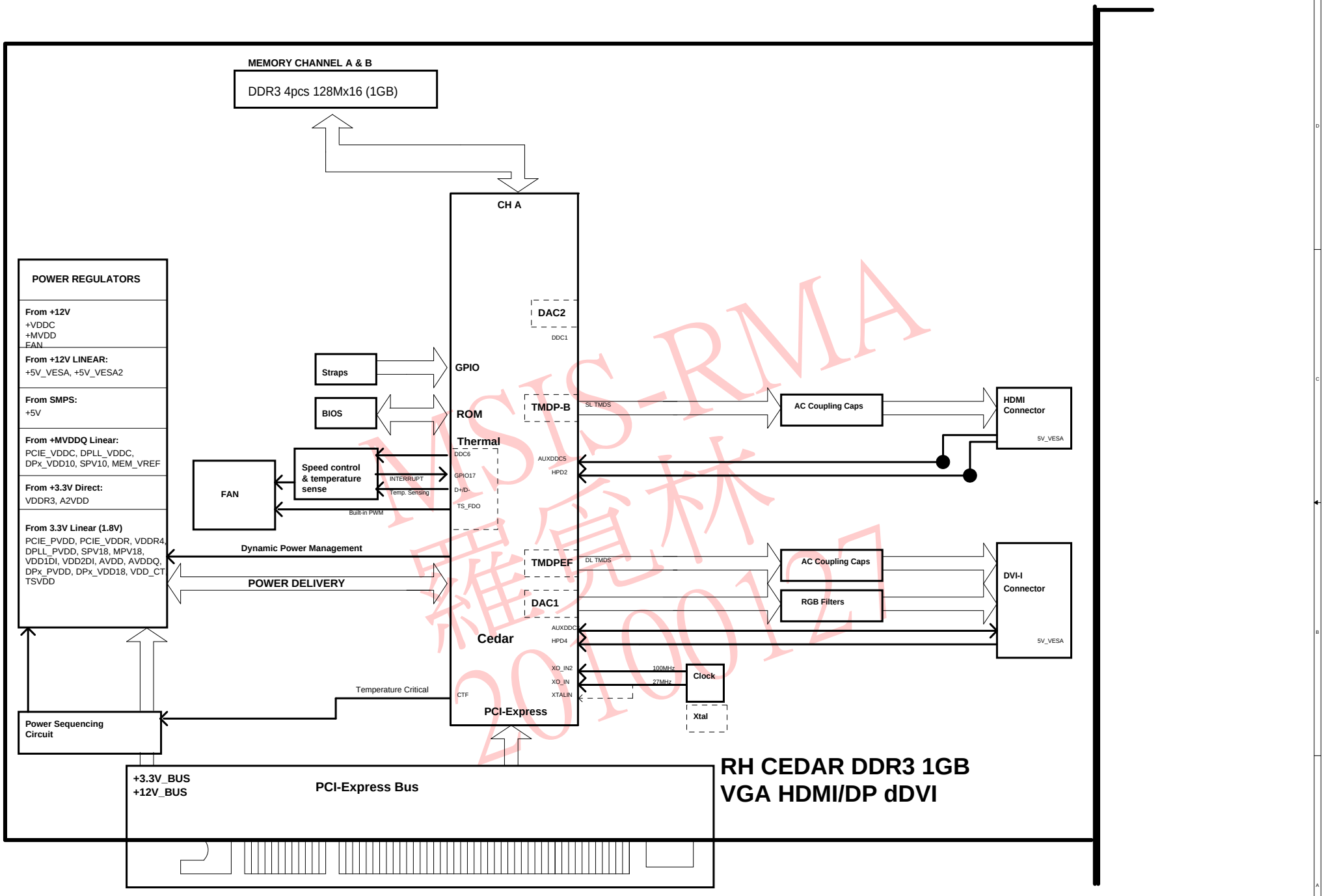

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Title	Schematic No.	Date:
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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev P03

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/03/23	
01	00B	2009/07/3	
02	00C	2009/08/12	Initial Cedar schematic
03	00D	2009/09/24	Change DDC line configuration