PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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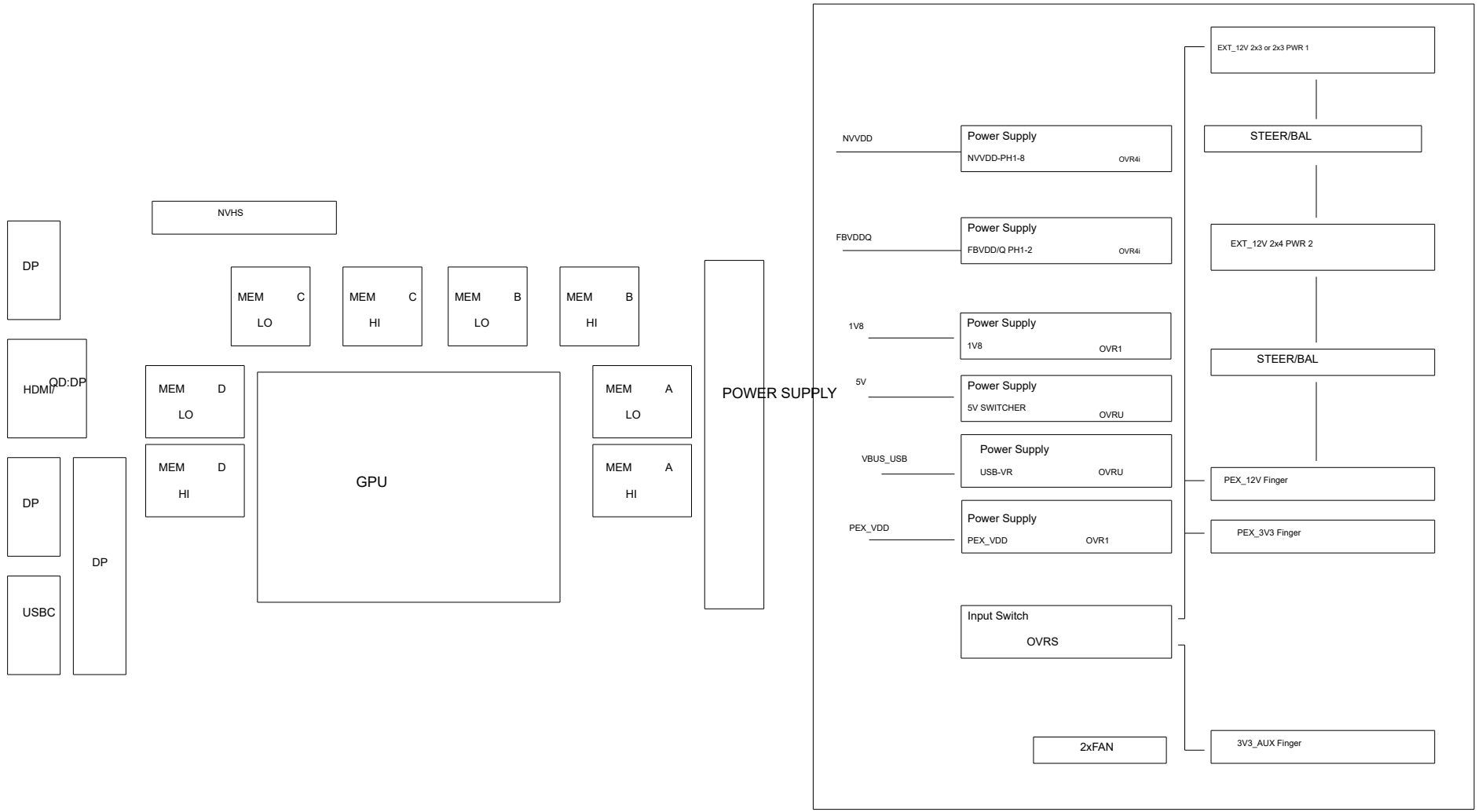

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Block Diagram

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NV_PN	600-1G180-BASE-200		
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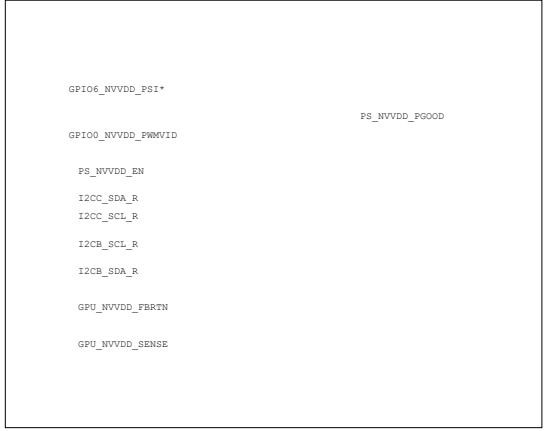
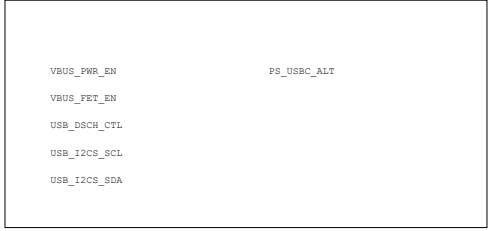
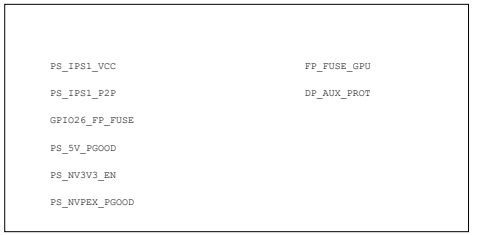
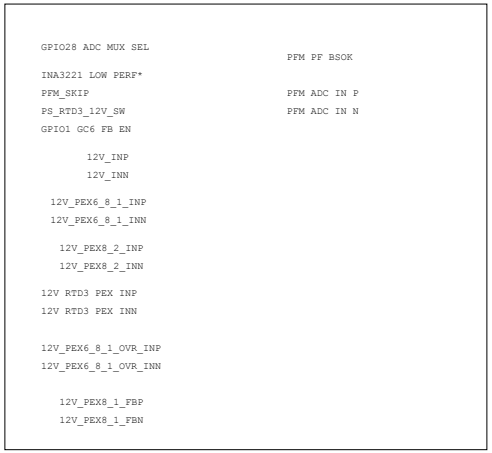
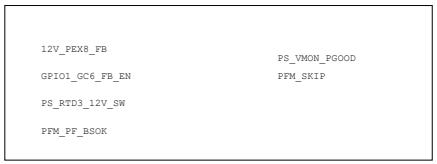
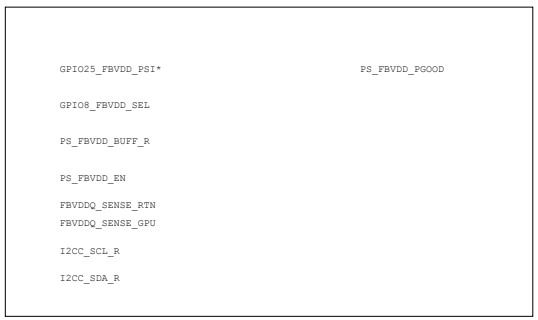

GPIO6_NVVDD_PSI*
PS_NVVDD_PGOOD
GPIO0_NVVDD_PWMVID
PS_NVVDD_EN
I2CC_SDA_R
I2CC_SCL_R
I2CB_SCL_R
I2CB_SDA_R
GPU_NVVDD_FBRTN
GPU_NVVDD_SENSE

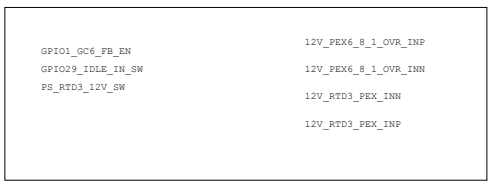

VBUS_PWR_EN
PS_USBC_ALT
VBUS_FET_EN
USB_DSCH_CTL
USB_I2CS_SCL
USB_I2CS_SDA

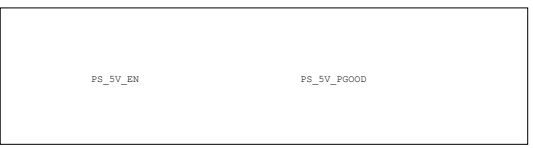

PS_IPS1_VCC
FP_FUSE_GPU
PS_IPS1_P2P
DP_AUX_PROT
GPIO26_FP_FUSE
PS_5V_PGOOD
PS_NV3V3_EN
PS_NVPEX_PGOOD

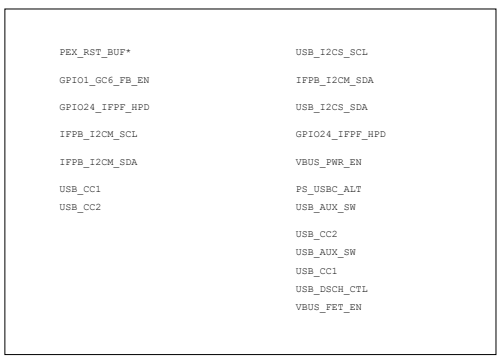

GPIO28 ADC MUX SEL
PFM PF BSOK
INA3221 LOW PERF*
PFM_SKIP
PFM ADC IN P
PS_RTD3_12V_SW
PFM ADC IN N
GPIO1 GC6 FB EN
12V_INP
12V_INN
12V_PEX6_8_1_INP
12V_PEX6_8_1_INN
12V_PEX8_2_INP
12V_PEX8_2_INN
12V RTD3 PEX INP
12V RTD3 PEX INN
12V_PEX6_8_1_OVR_INP
12V_PEX6_8_1_OVR_INN
12V_PEX8_1_FBP
12V_PEX8_1_FBN

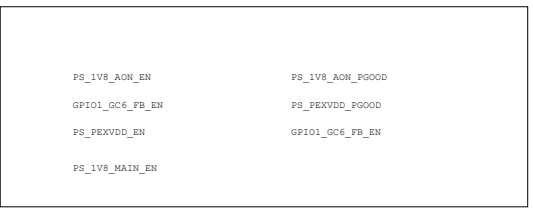

12V_PEX8_FB
PS_VMON_PGOOD
GPIO1_GC6_FB_EN
PFM_SKIP
PS_RTD3_12V_SW
PFM_PF_BSOK

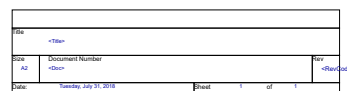

GPIO25_FBVDD_PSI*
PS_FBVDD_PGOOD
GPIO8_FBVDD_SEL
PS_FBVDD_BUFF_R
PS_FBVDD_EN
FBVDDQ_SENSE_RTN
FBVDDQ_SENSE_GPU
I2CC_SCL_R
I2CC_SDA_R


GPIO1_GC6_FB_EN
12V_PEX6_8_1_OVR_INP
GPIO29_IDLE_IN_SW
12V_PEX6_8_1_OVR_INN
PS_RTD3_12V_SW
12V_RTD3_PEX_INN
12V_RTD3_PEX_INP


PS_5V_EN
PS_5V_PGOOD


PEX_RST_BUF*
USB_I2CS_SCL
GPIO1_GC6_FB_EN
IFPB_I2CM_SDA
GPIO24_IFPF_HPD
USB_I2CS_SDA
IFPB_I2CM_SCL
GPIO24_IFPF_HPD
IFPB_I2CM_SDA
VBUS_PWR_EN
USB_CC1
PS_USBC_ALT
USB_CC2
USB_AUX_SW
USB_CC2
USB_AUX_SW
USB_CC1
USB_DSCH_CTL
VBUS_FET_EN


PS_1V8_AON_EN
PS_1V8_AON_PGOOD
GPIO1_GC6_FB_EN
PS_PEXVDD_PGOOD
PS_PEXVDD_EN
GPIO1_GC6_FB_EN
PS_1V8_MAIN_EN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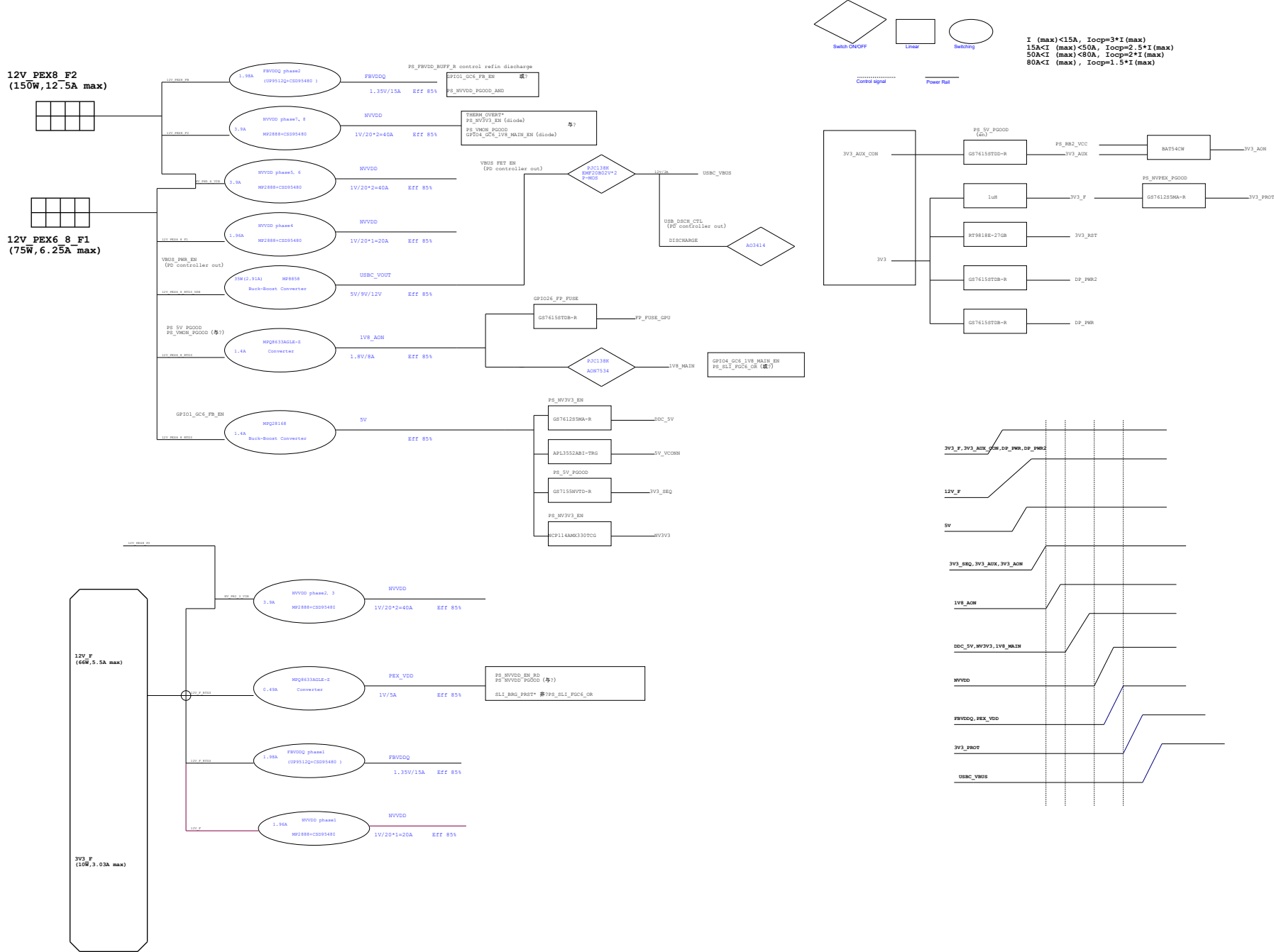
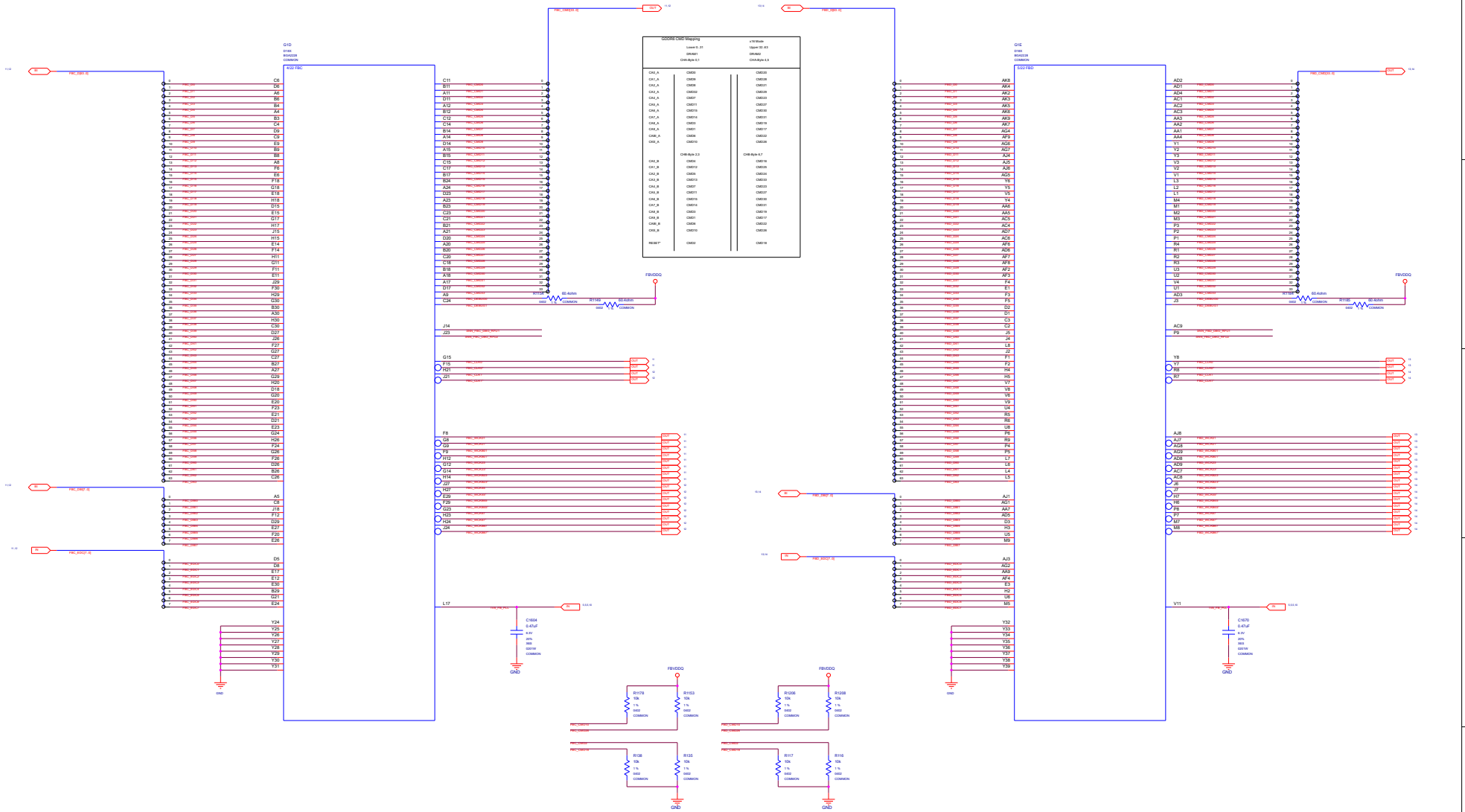

12V_PEX8_F2
(150W,12.5A max)
12V_PEX6_8_F1
(75W,6.25A max)
FBVDDQ phase2
(UP9512Q+CSD95480)
1.98A
FBVDDQ
1.35V/15A Eff 85%
PS_FBVDD_BUFF_R control refin discharge
GPIO1_GC6_FB_EN 或?
PS_NVVDD_PGOOD_AND
NVVDD phase7, 8
3.9A
MP2888+CSD95480
NVVDD
1V/20*2=40A Eff 85%
THERM_OVERT*
PS_NV3V3_EN (diode)
PS_VMON_PGOOD
GPIO4_GC6_1V8_MAIN_EN (diode)
与?
NVVDD phase5, 6
3.9A
MP2888+CSD95480
NVVDD
1V/20*2=40A Eff 85%
VBUS FET EN
(PD controller out)
PJC138K
EMF20B02V*2
P+MOS
12V_A
USBC_VBUS
USB_DSCH_CTL
(PD controller out)
DISCHARGE
AO3414
NVVDD phase4
1.96A
MP2888+CSD95480
NVVDD
1V/20*1=20A Eff 85%
VBUS_PWR_EN
(PD controller out)
35W(2.91A) MP8858
Buck-Boost Converter
USBC_VOUT
5V/9V/12V Eff 85%
GPIO26_FP_FUSE
GS7615STDB-R
FP_FUSE_GPU
PS_5V_PGOOD
PS_VMON_PGOOD (与?)
MPQ8633AGLE-Z
1.4A
Converter
1V8_AON
1.8V/8A Eff 85%
PJC138K
AON7534
1V8_MAIN
GPIO4_GC6_1V8_MAIN_EN
PS_SLI_PGC6_OR (或?)
GPIO1_GC6_FB_EN
MPQ2816
1.4A
Buck-Boost Converter
5V
Eff 85%
PS_NV3V3_EN
GS7612SSMA-R
ndc_5V
APL3552ABI-TRG
5V_VCONN
PS_5V_PGOOD
GS7155NVTD-R
3V3_SEQ
PS_NV3V3_EN
NCP114AMG330TCG
NV3V3
Switch ON/OFF
Linear
Switching
Control signal
Power Rail
I (max)<15A, Iocp=3*I(max)
15A<I (max)<50A, Iocp=2.5*I(max)
50A<I (max)<80A, Iocp=2*I(max)
80A<I (max), Iocp=1.5*I(max)
PS_5V_PGOOD
(en)
3V3_AUX_CON
GS7615STDD-R
PS_RR2_VCC
3V3_AUX
BAT54CW
3V3_AON
PS_NVPEX_PGOOD
1uH
3V3_F
GS7612SSMA-R
3V3_PROT
RT9818E-27GB
3V3_RST
GS7615STDB-R
DP_PWR2
3V3
GS7615STDB-R
DP_PWR
12V_F
(66W,5.5A max)
3V3_F
(10W,3.03A max)
NVVDD phase2, 3
3.9A
MP2888+CSD95480
NVVDD
1V/20*2=40A Eff 85%
MPQ8633AGLE-Z
0.49A
Converter
PEX_VDD
1V/5A Eff 85%
PS_NVVDD_EN_RD
PS_NVVDD_PGOOD (与?)
SLI_BRG_PRST* 非?PS_SLI_PGC6_OR
FBVDDQ phase1
(UP9512Q+CSD95480)
1.98A
FBVDDQ
1.35V/15A Eff 85%
NVVDD phase1
1.96A
MP2888+CSD95480
NVVDD
1V/20*1=20A Eff 85%
3V3_F,3V3_AUX_CON,DP_PWR,DP_PWR2
12V_F
5V
3V3_SEQ,3V3_AUX,3V3_AON
1V8_AON
DDC_5V,NV3V3,1V8_MAIN
NVVDD
FBVDDQ,PEX_VDD
3V3_PROT
USBC_VBUS

Page10: MEMORY: GPU Partition C/D



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: GPU Partition C/D

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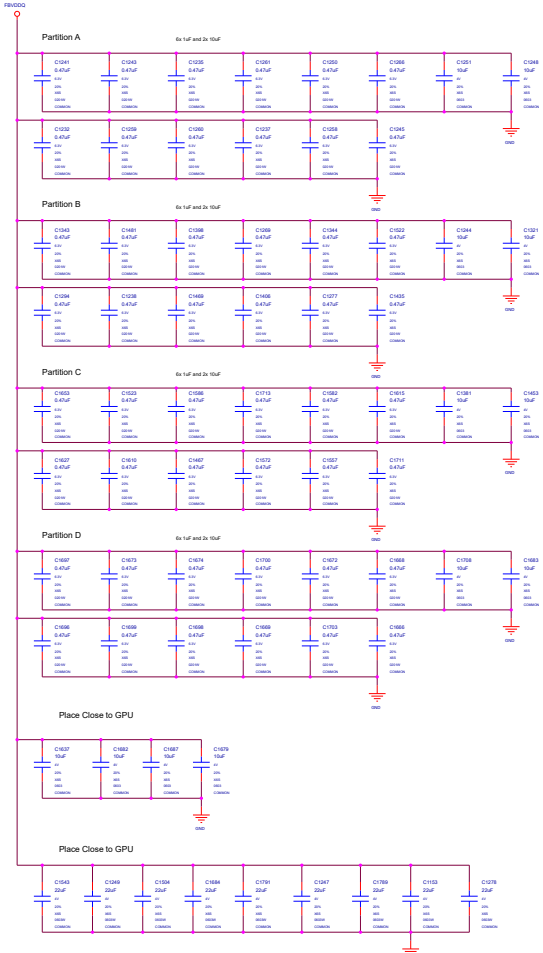
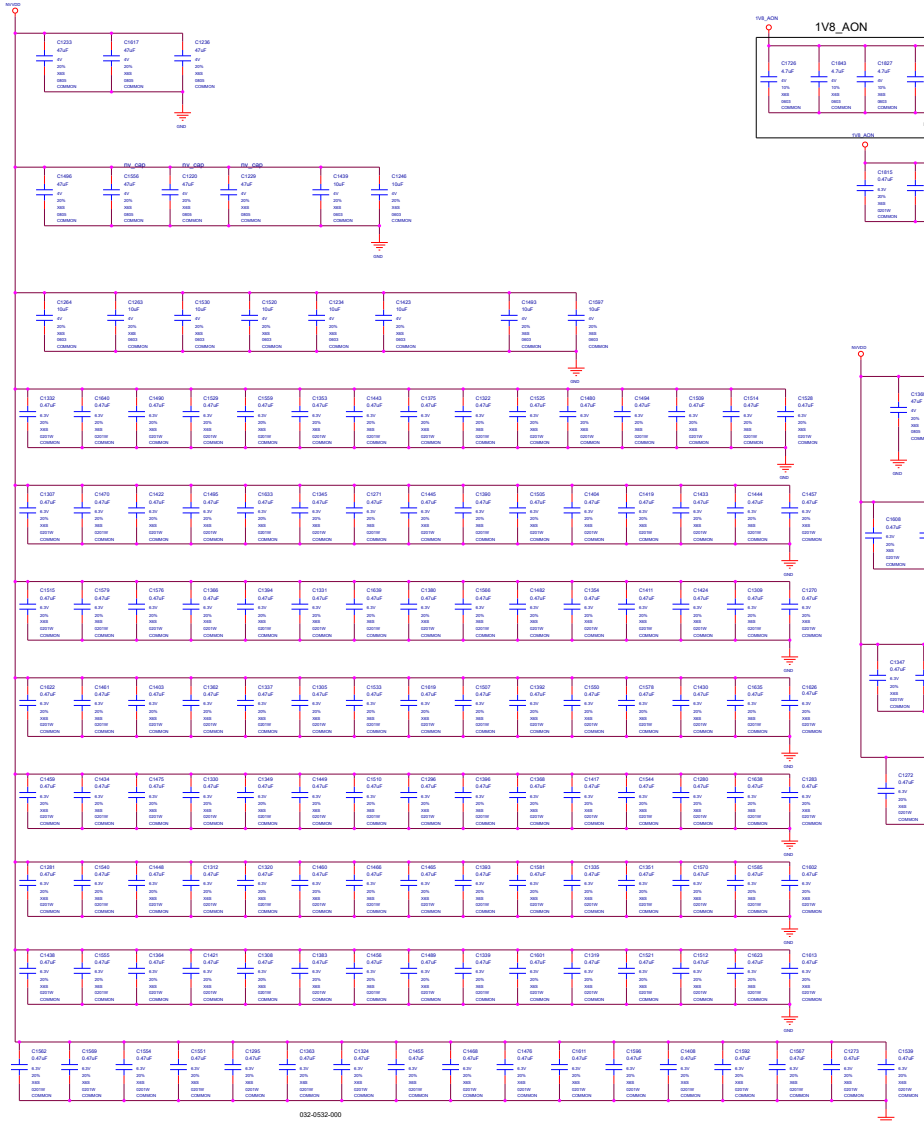
Page16: GPU Decoupling

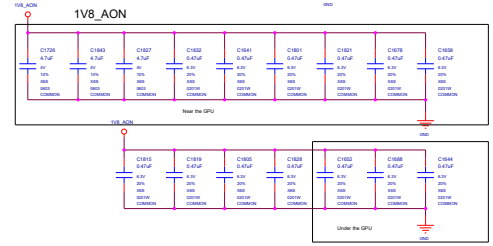
FBVDDQ



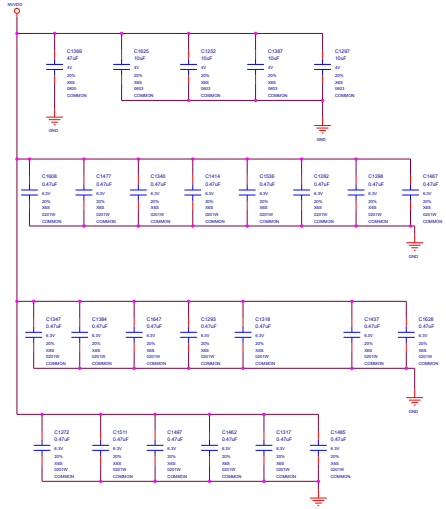
NVVDD



1V8_AON



NVVDD



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU Decoupling

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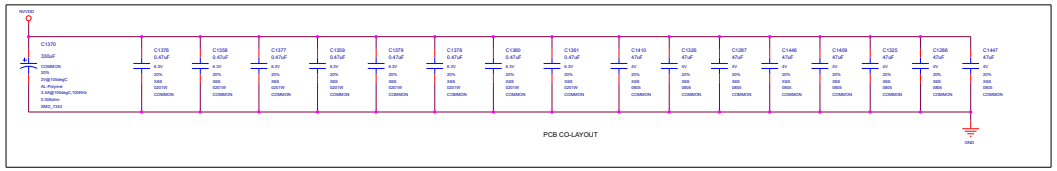
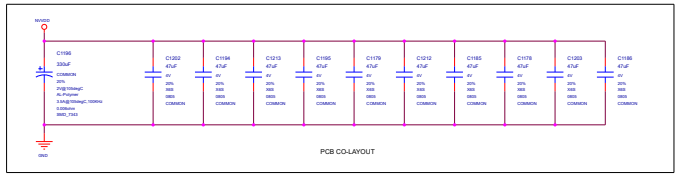
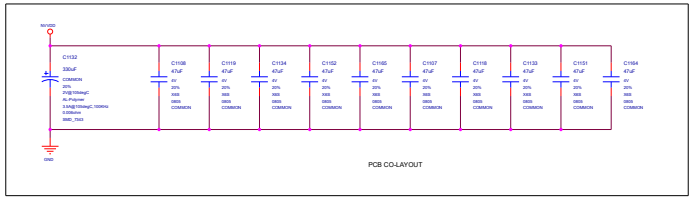
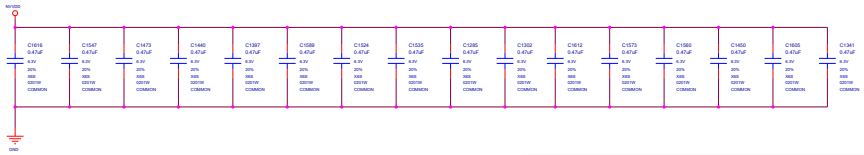
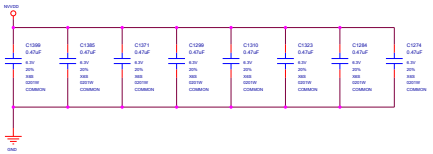
Page17: GPU Decoupling

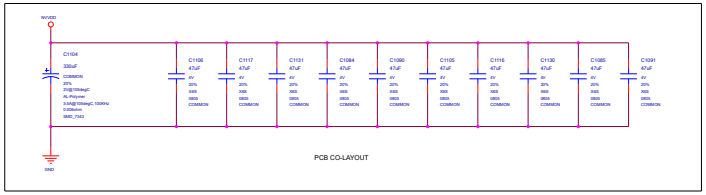


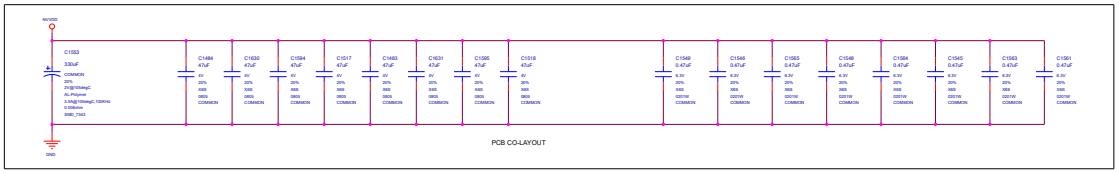












ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING

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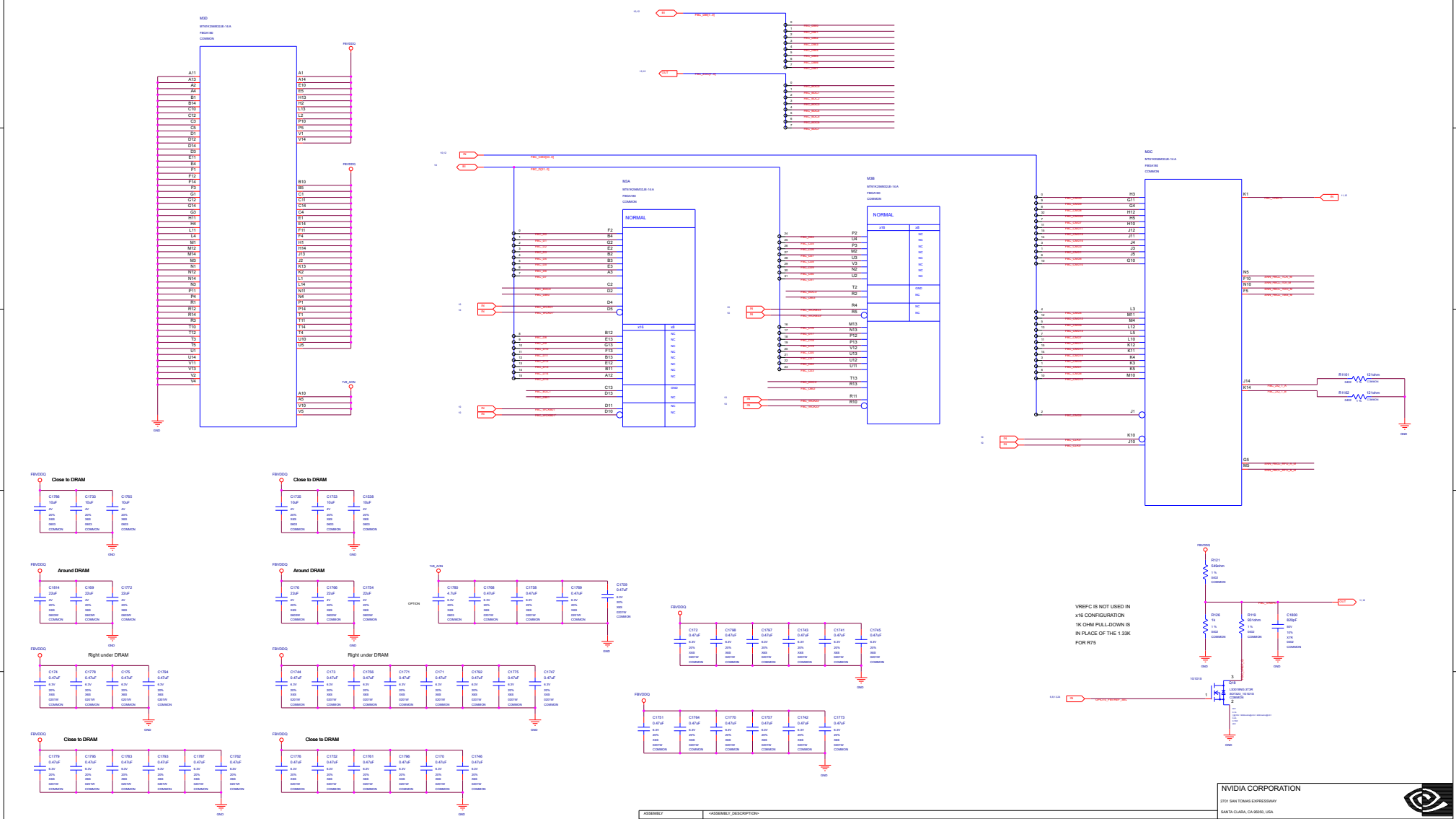

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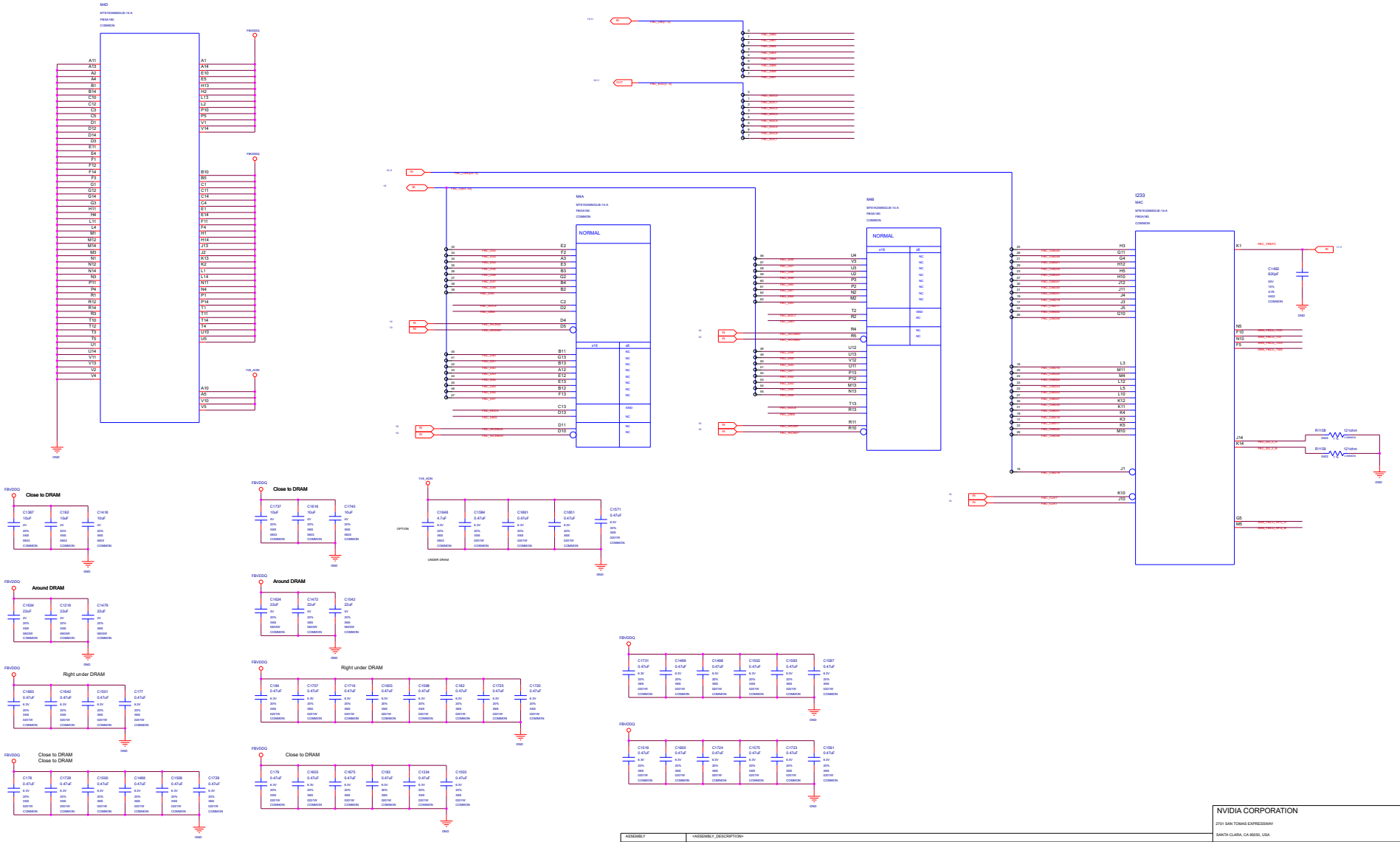

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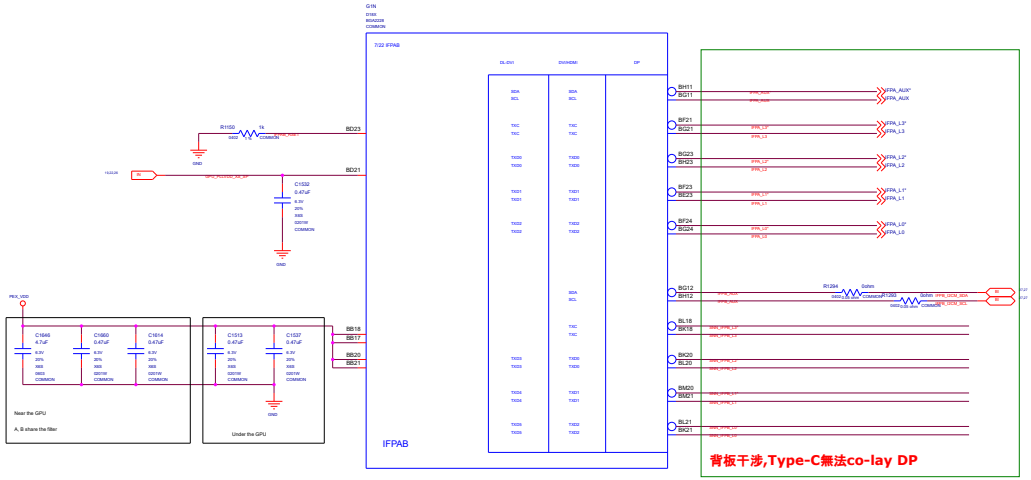

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NV_PN	600-1G180-BASE-200		
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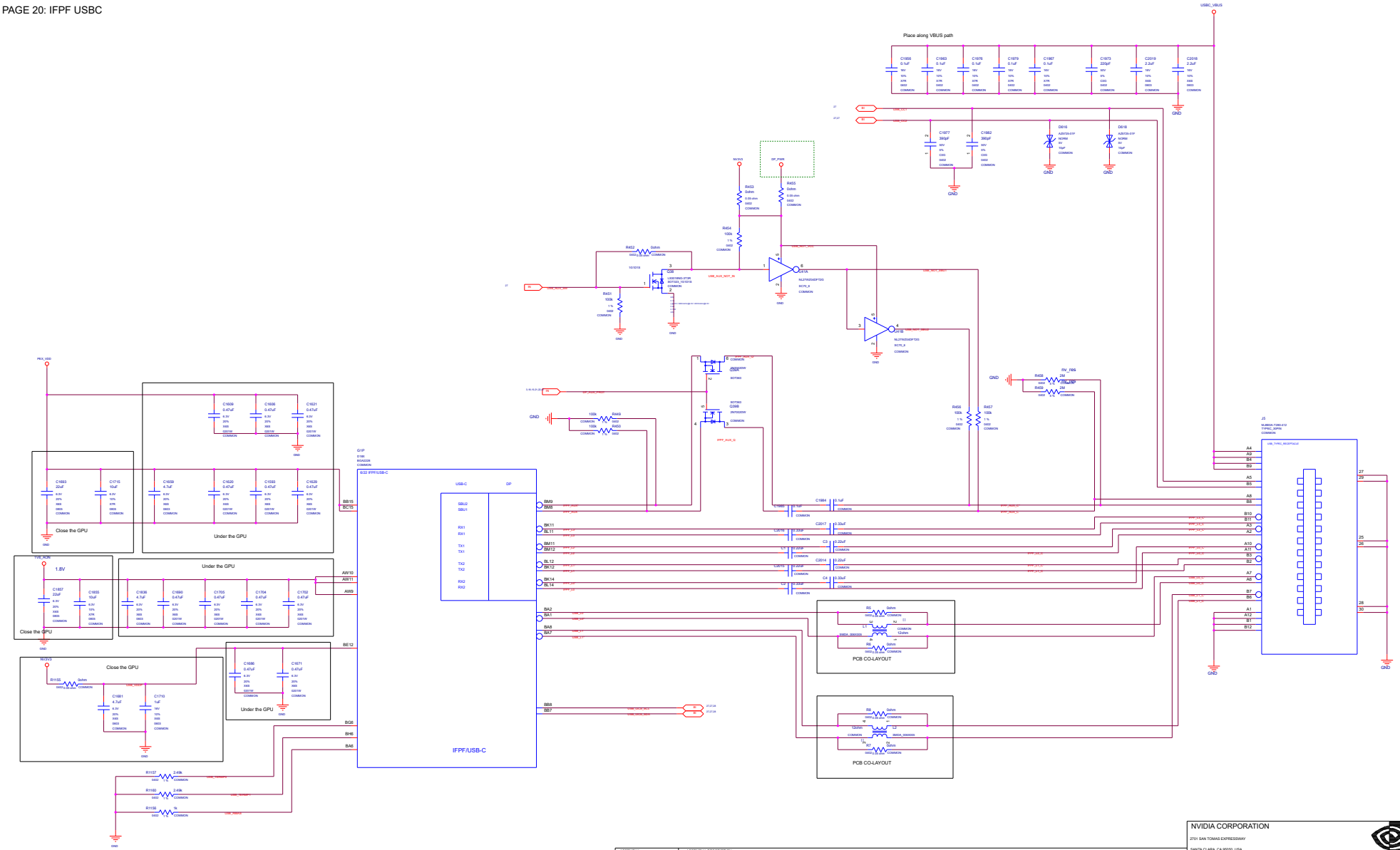

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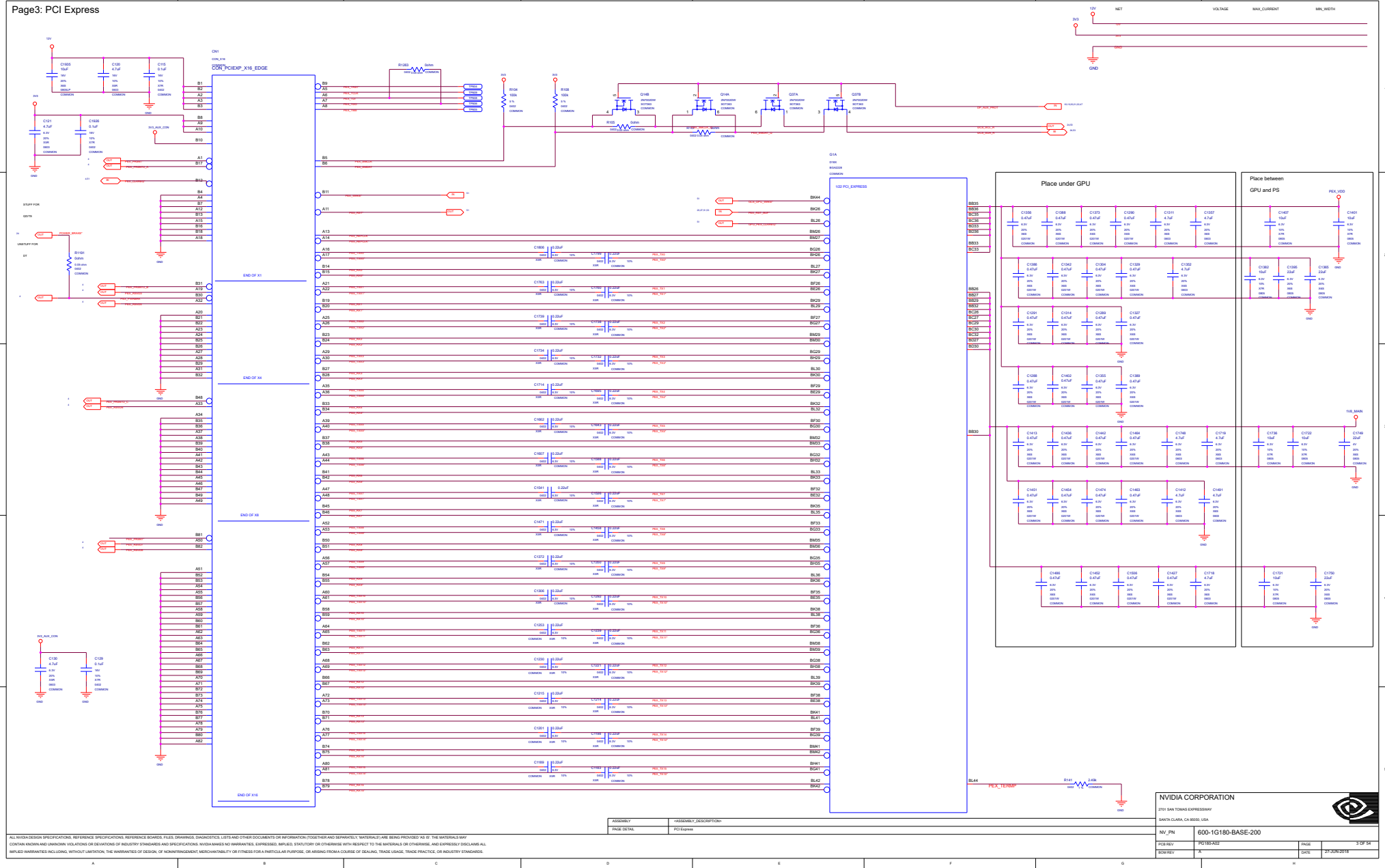
Page3: PCI Express



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NVIDIA CORPORATION
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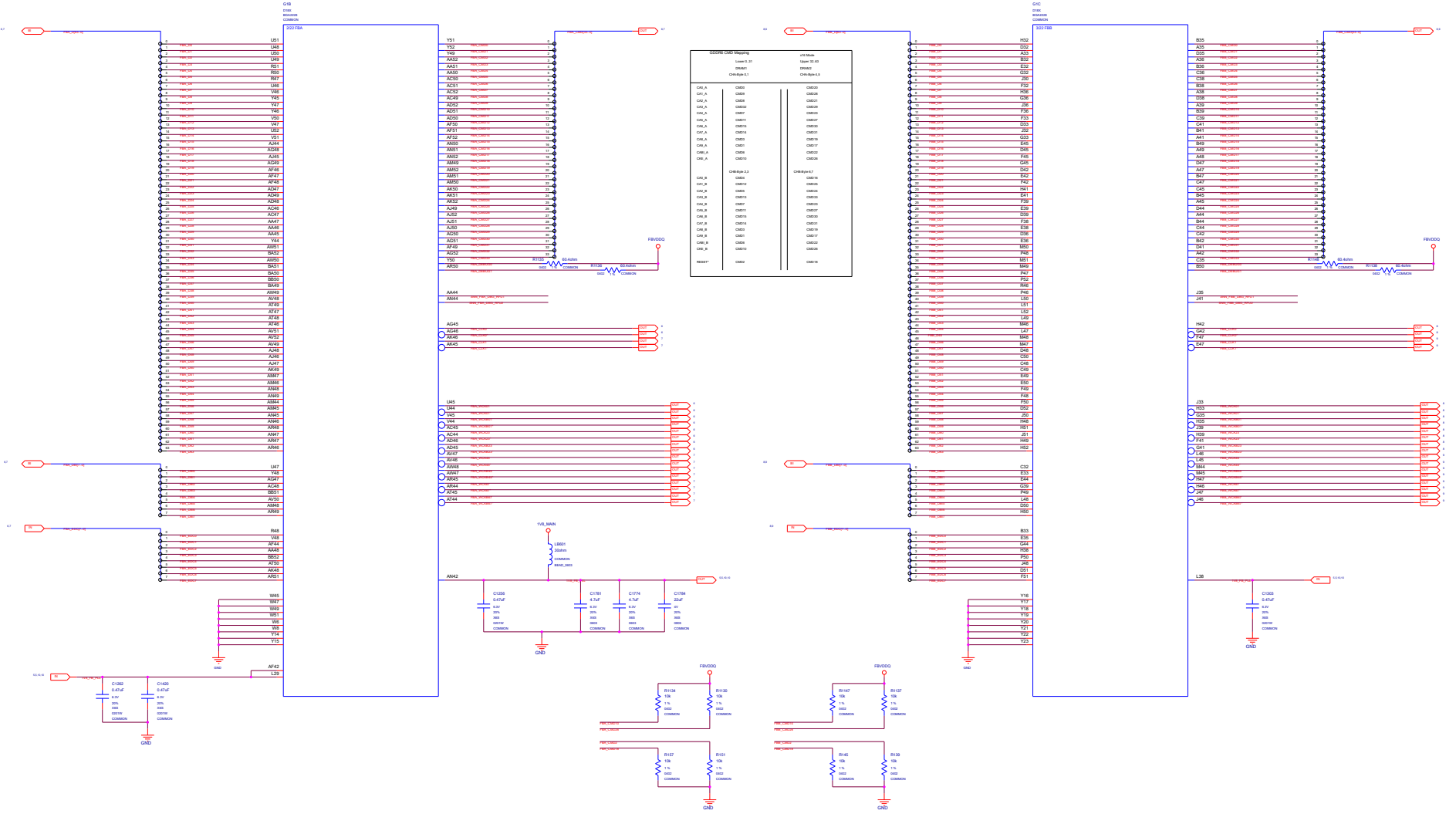
Page5: MEMORY: GPU Partition A/B



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: GPU Partition A/B

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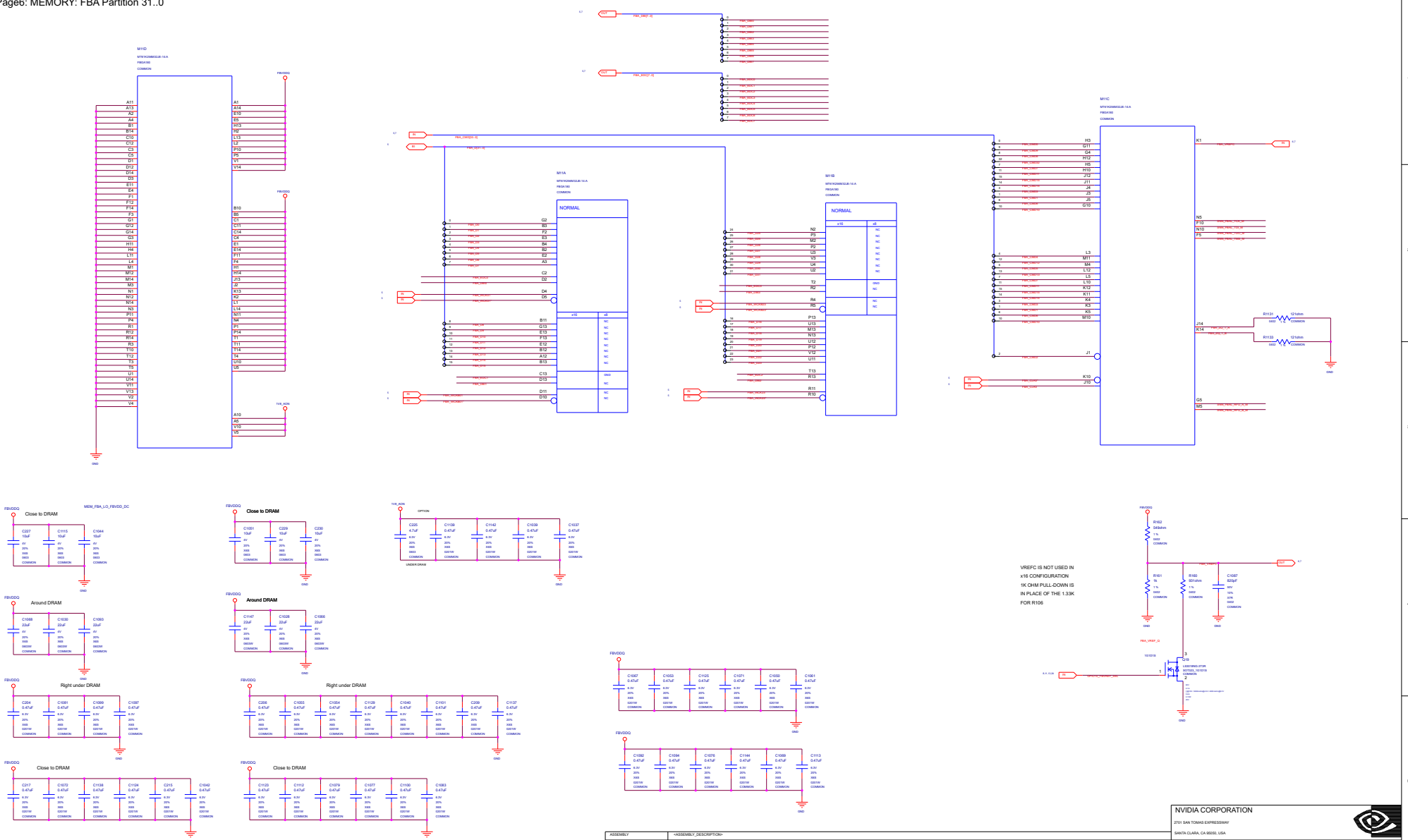
Page6: MEMORY: FBA Partition 31..0



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBA Partition 31..0

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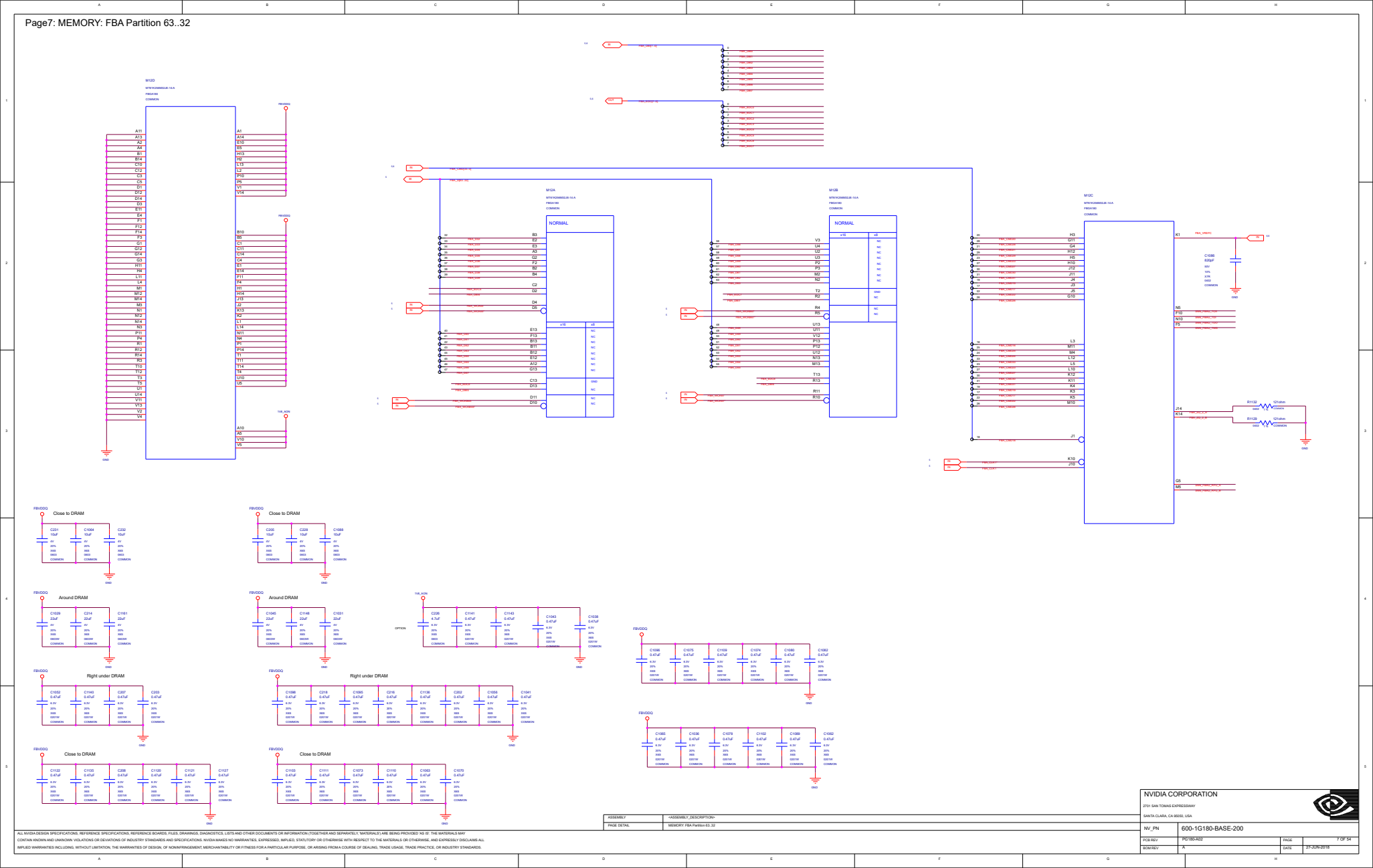
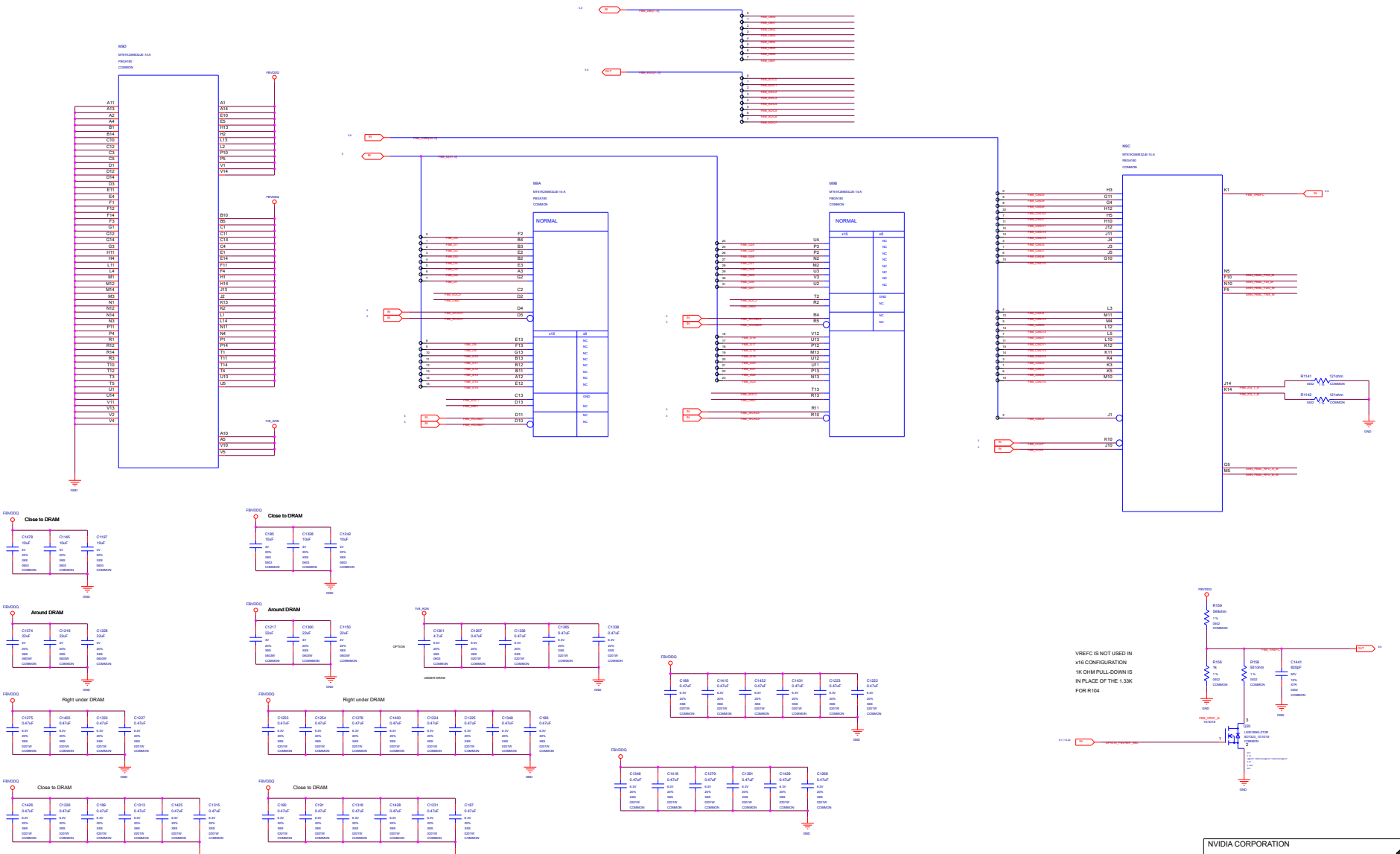
Page7: MEMORY: FBA Partition 63..32



Page8: MEMORY: FBB Partition 31..0



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB Partition 31..0

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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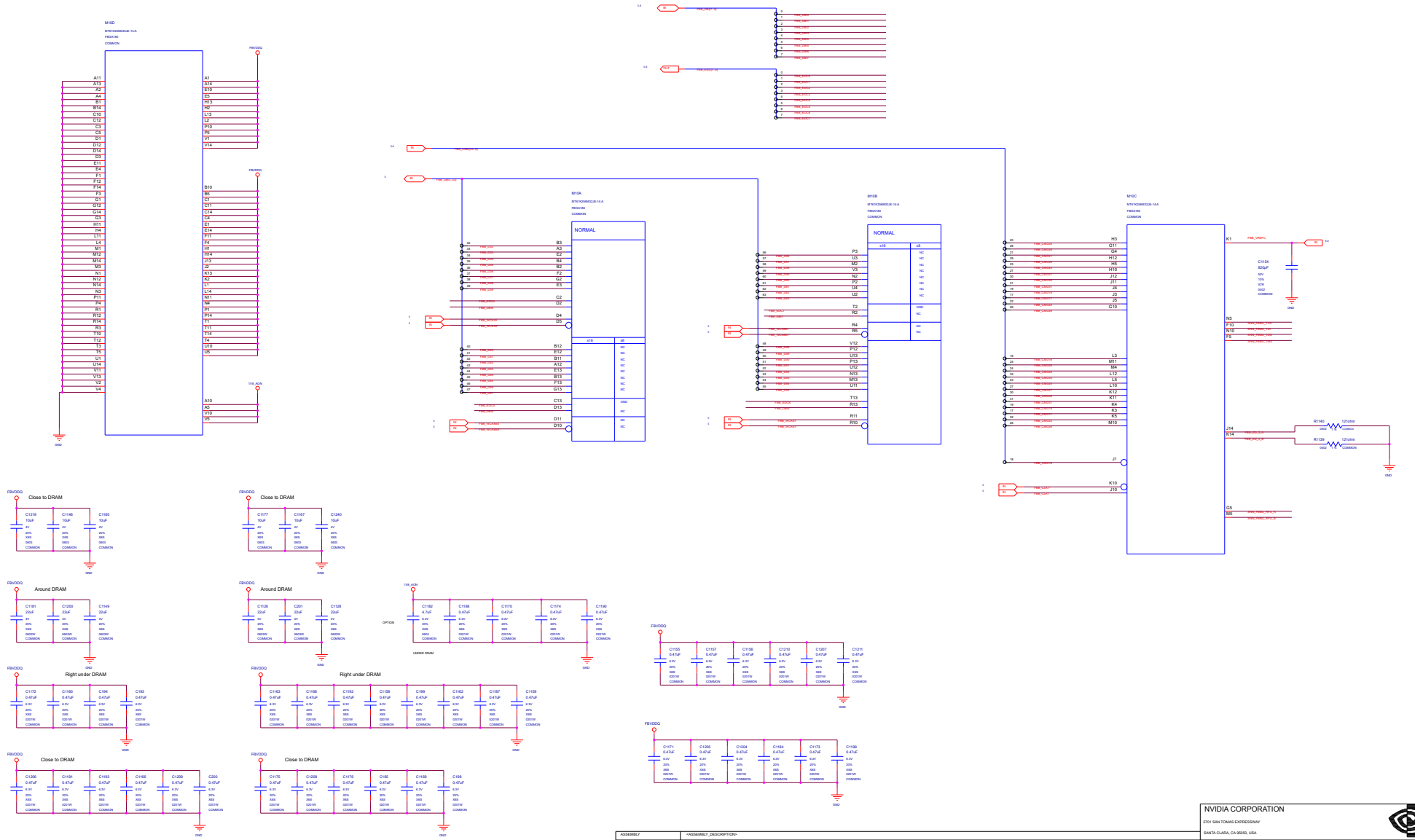
Page9: MEMORY: FBB Partition 63..32



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB Partition 63..32

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G180-BASE-200		
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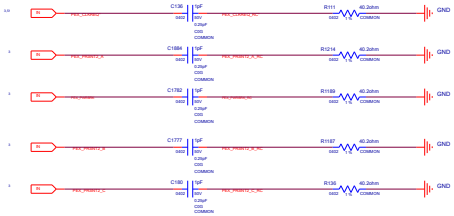
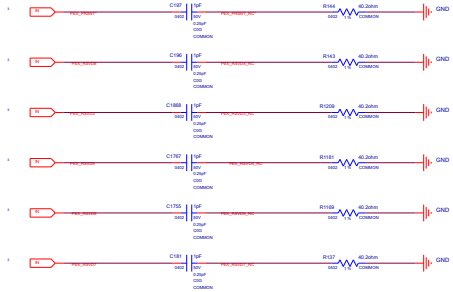
Page4: PCI Termination



PLACE CLOSE TO B81



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI Termination

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G180-BASE-200		
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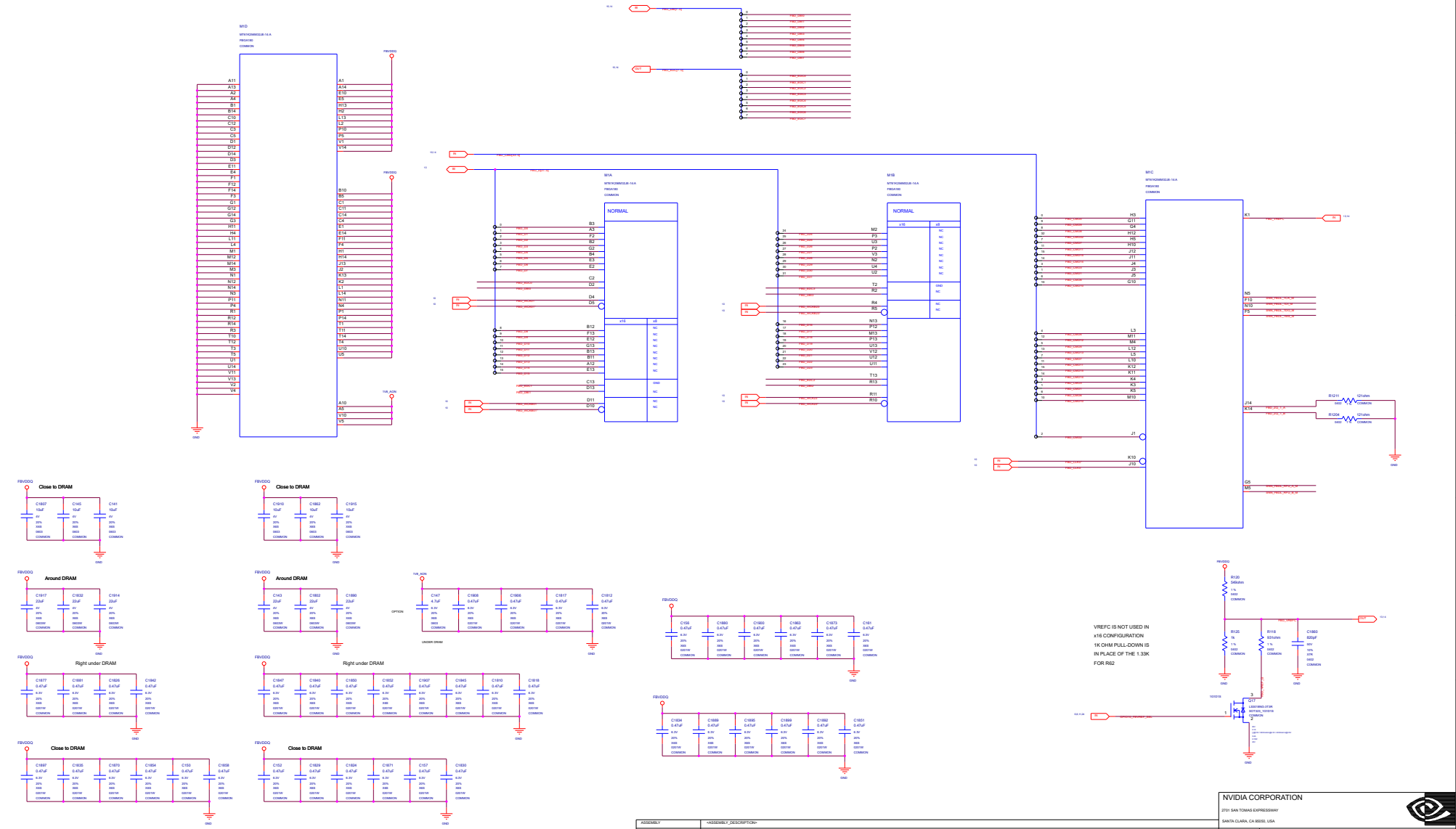
Page13: MEMORY: FBD Partition 31..0



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBD Partition 31..0

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
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NV_PN	600-1G180-BASE-200
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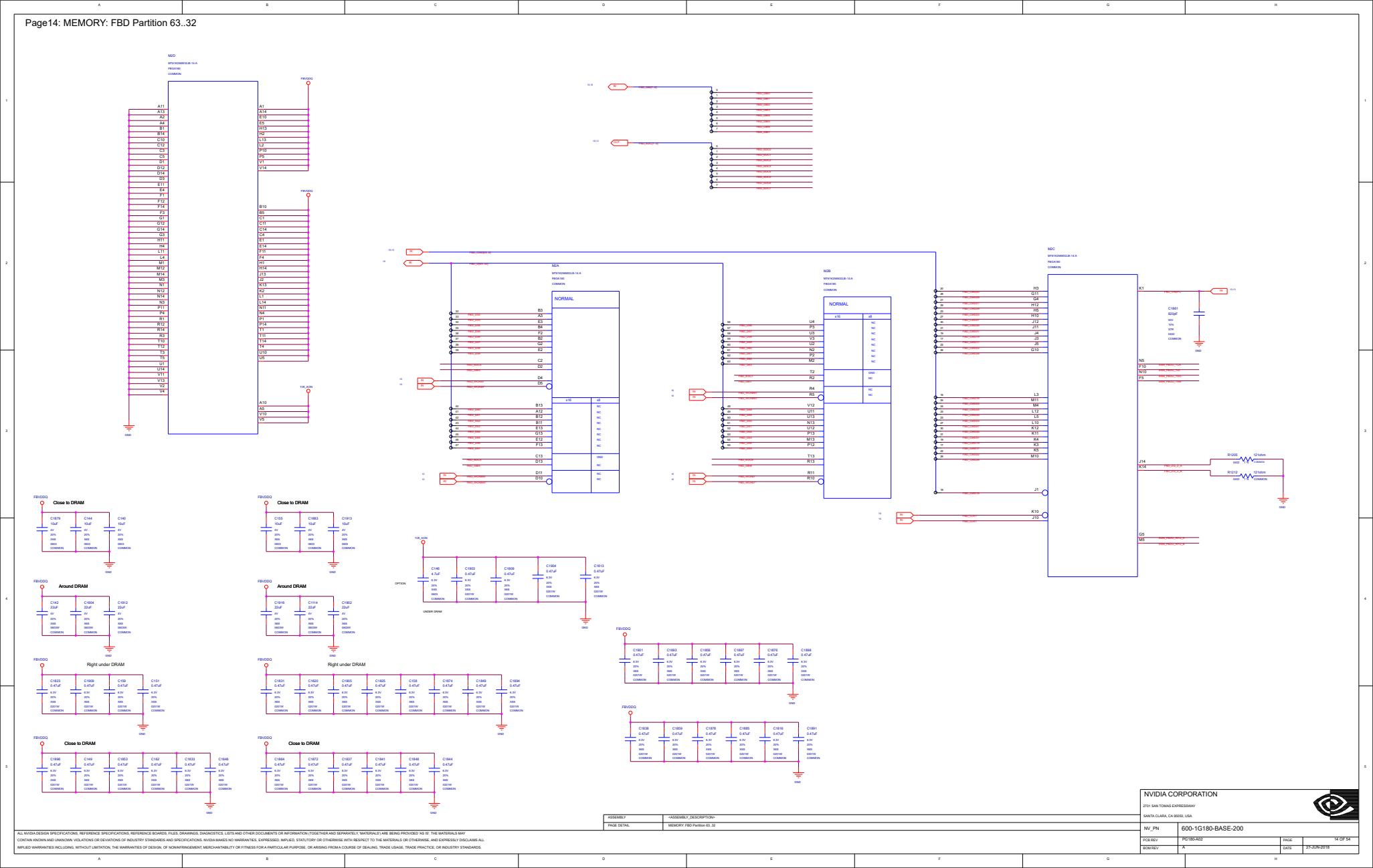
Page14: MEMORY: FBD Partition 63..32



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBD Partition 63..32

NVIDIA CORPORATION
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NV_PN	600-1G180-BASE-200		
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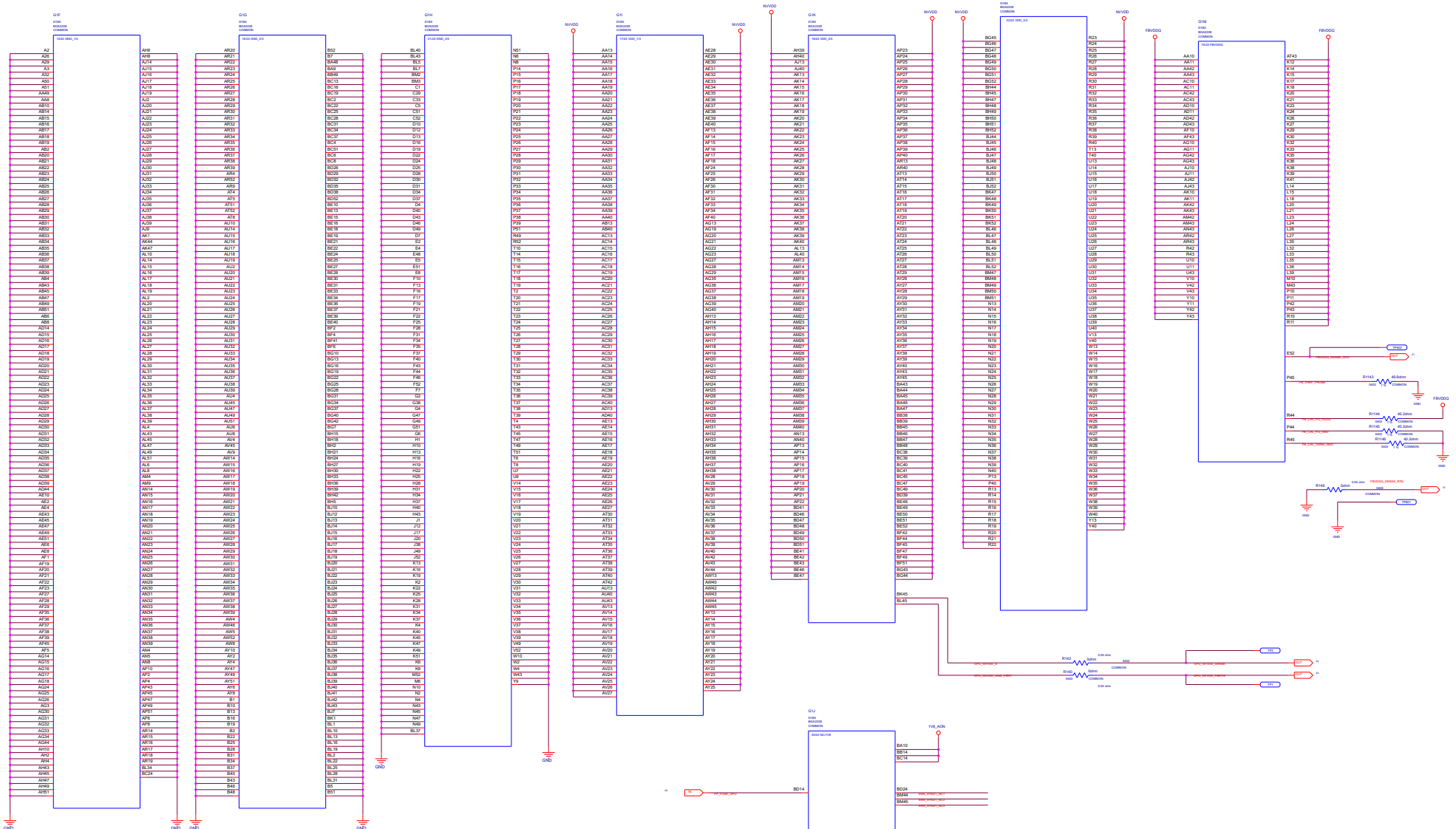
Page15: GPU PWR and GND



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR and GND

NVIDIA CORPORATION
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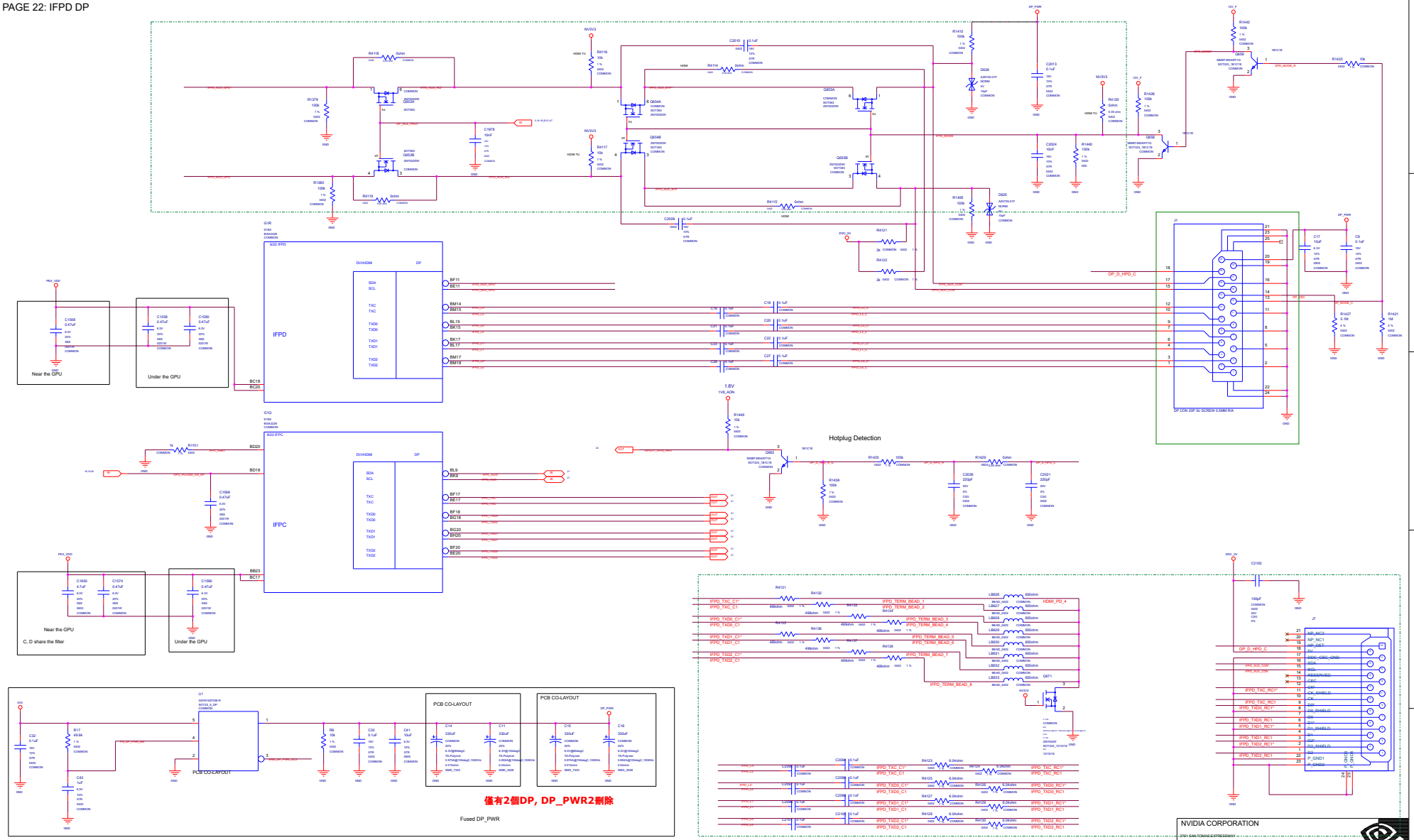
PAGE 22: IFPD DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPD DP

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
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NV_PN	600-1G180-BASE-200		
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PAGE 25: MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

DEFAULT

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

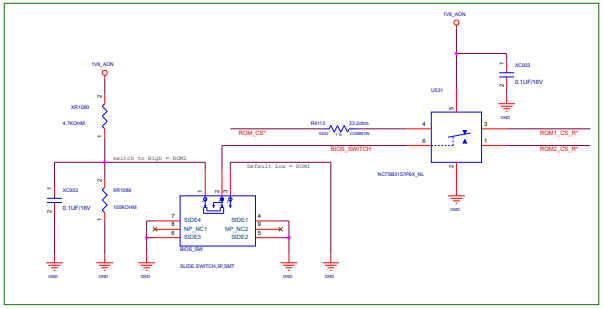
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

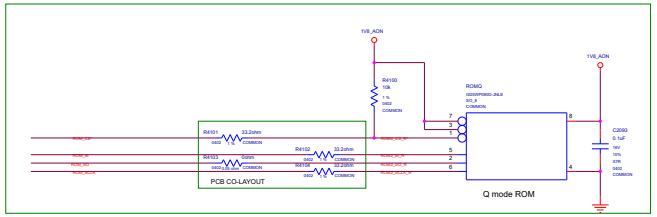
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

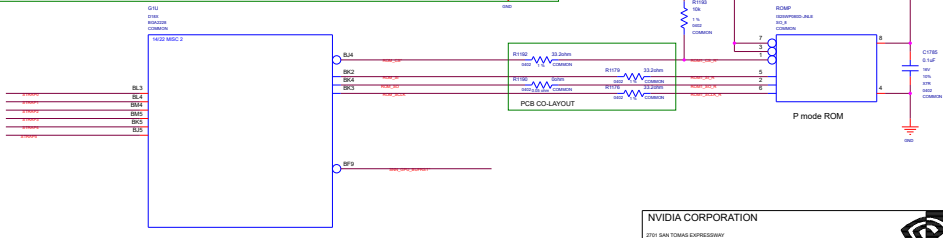
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

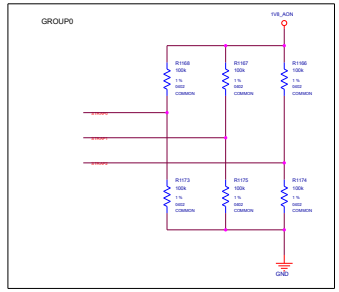
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

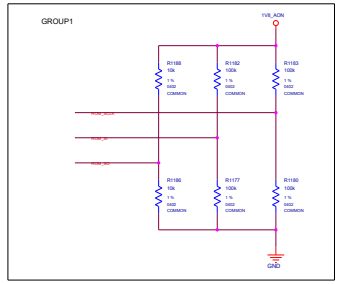
Default

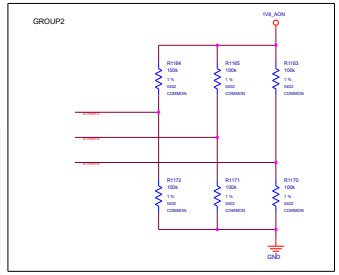












ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC3 ROM, STRAPS

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NV_PN	600-1G180-BASE-200		
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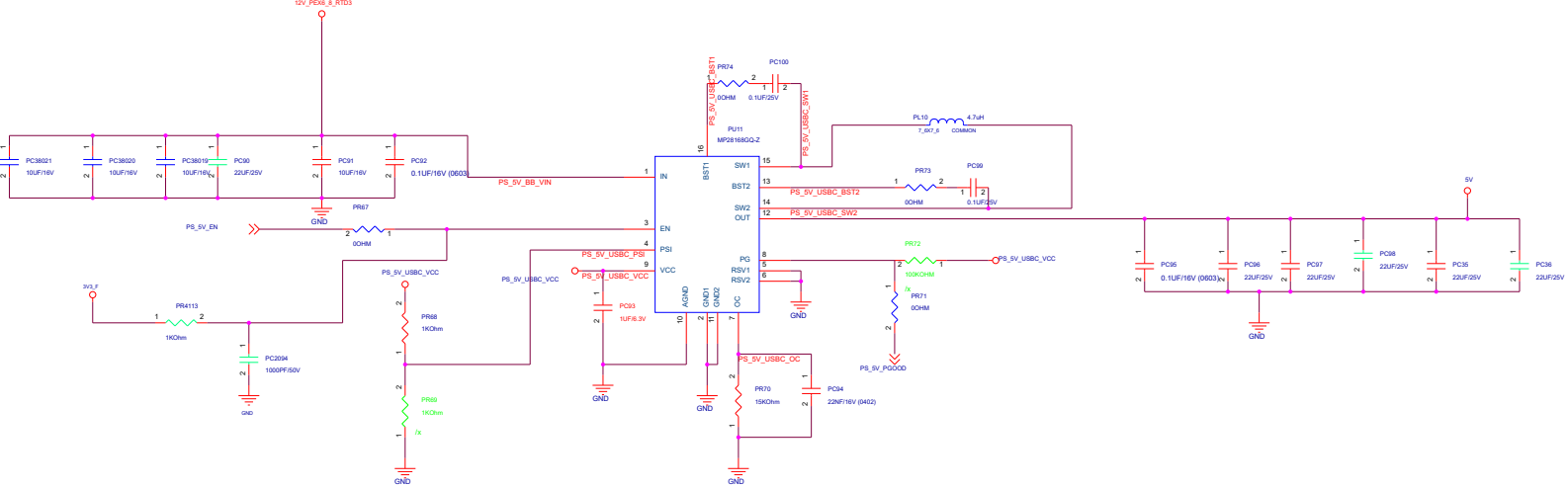
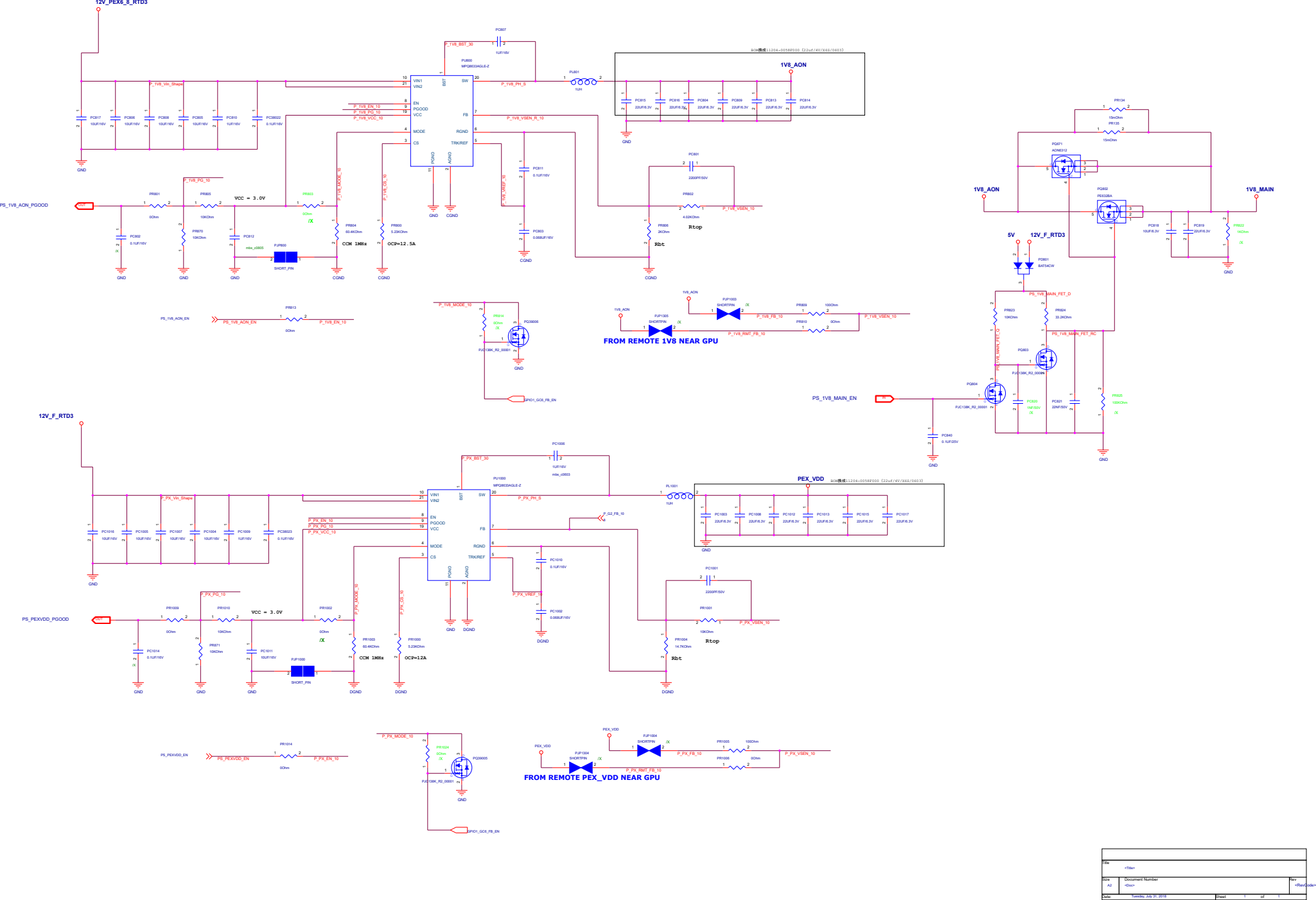
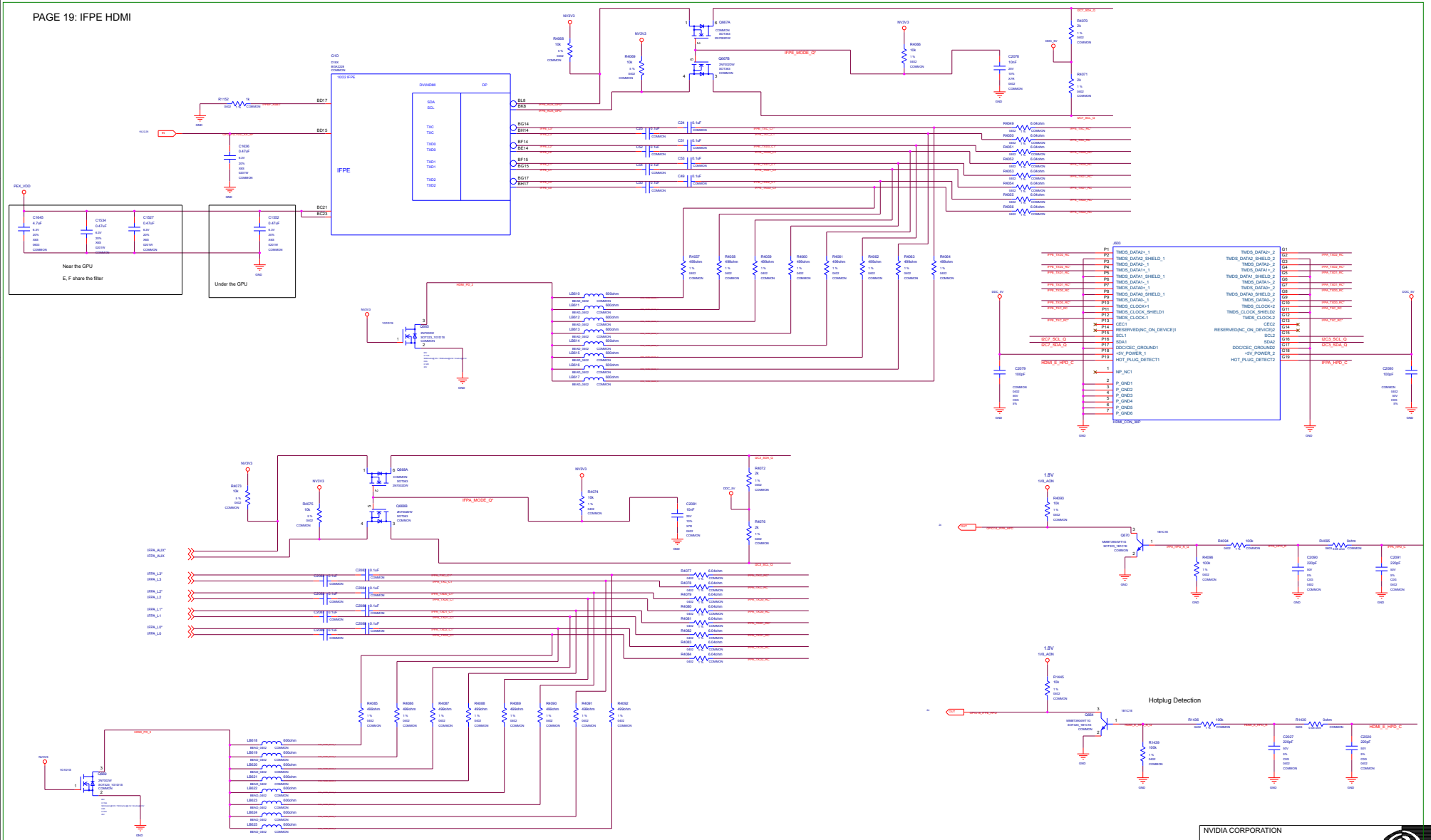


Title	<Title>	
Size: C	Document Number: <Doc>	Rev: <RevCode>
Date: Tuesday, July 31, 2018	Sheet 1 of 1	


12V_PEX6_8_RTD3
1V8_AON
1V8_MAIN
5V
12V_F_RTD3
PEX_VDD
PS_1V8_AON_PGOOD
PS_PEXVDD_PGOOD
PS_1V8_AON_EN
PS_PEXVDD_EN
PS_1V8_MAIN_EN
VCC = 3.0V
CCM 1MHz
OCP=12.5A
OCP=12A
Rtop
Rbt
FROM REMOTE 1V8 NEAR GPU
FROM REMOTE PEX_VDD NEAR GPU
SHORT_PIN
GPIO1_GC6_FB_EN

PAGE 19: IFPE HDMI



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPE DP

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
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NV_PN	600-1G180-BASE-200		
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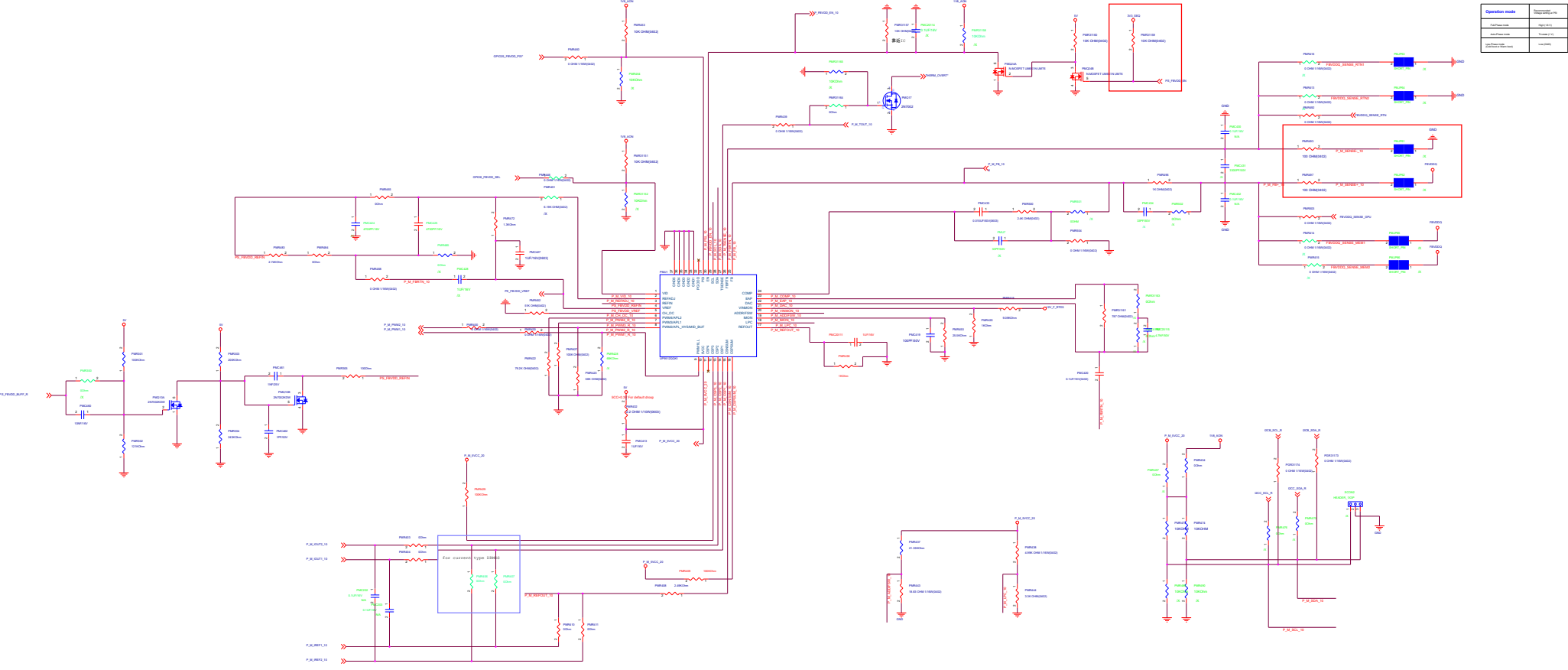
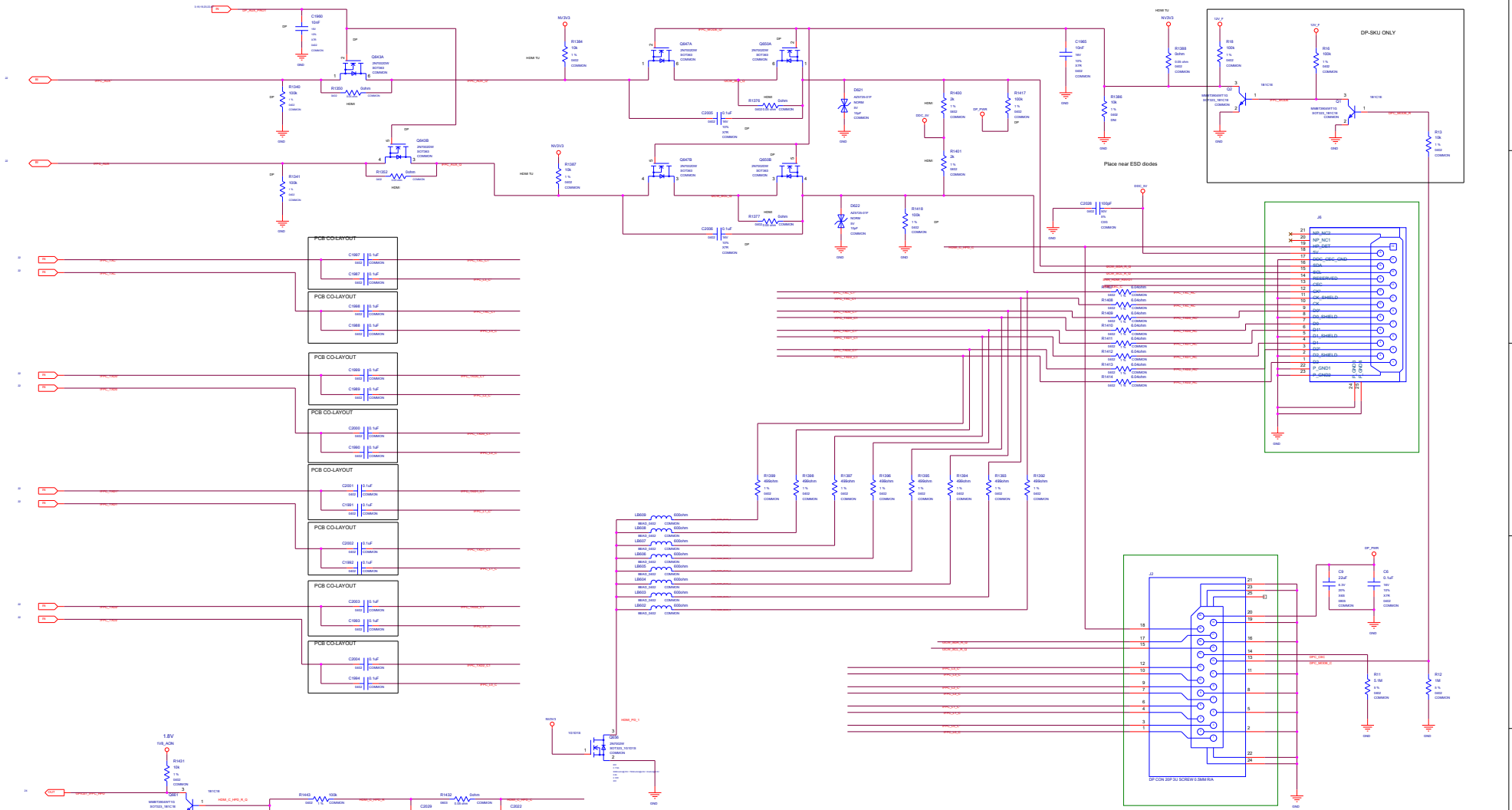


Operation mode	Function control (Voltage setting up 0.5V)
Full Phase mode	High (>2.1V)
Auto Phase mode	Tri-state (1~2)
Light Phase mode (Auto Phase + Skip mode)	Low (GND)

		R15 (09016-00360500) L=0.15uH DCR=0.82mohm	R30 (09016-00130800) L=0.30uH DCR=0.78mohm
RC match	Csum	0.1uF	0.1uF
	Rcsp	14.7K ohm	30k ohm
Total OCP (410A)	Rsum	0.5K ohm	0.5K ohm
	Isum	85.7uA	80uA
	Rimon	28K ohm (418A)	30K ohm (410A)
Loadline (0.3m ohm)	RLL	1.47K ohm	1.54K ohm
Loadline En threshold (101A En, 50A Dis)	Rtop	124K ohm	124K ohm
	Rbot	38.3K ohm	39K ohm



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPC HDMI 2.0/DP

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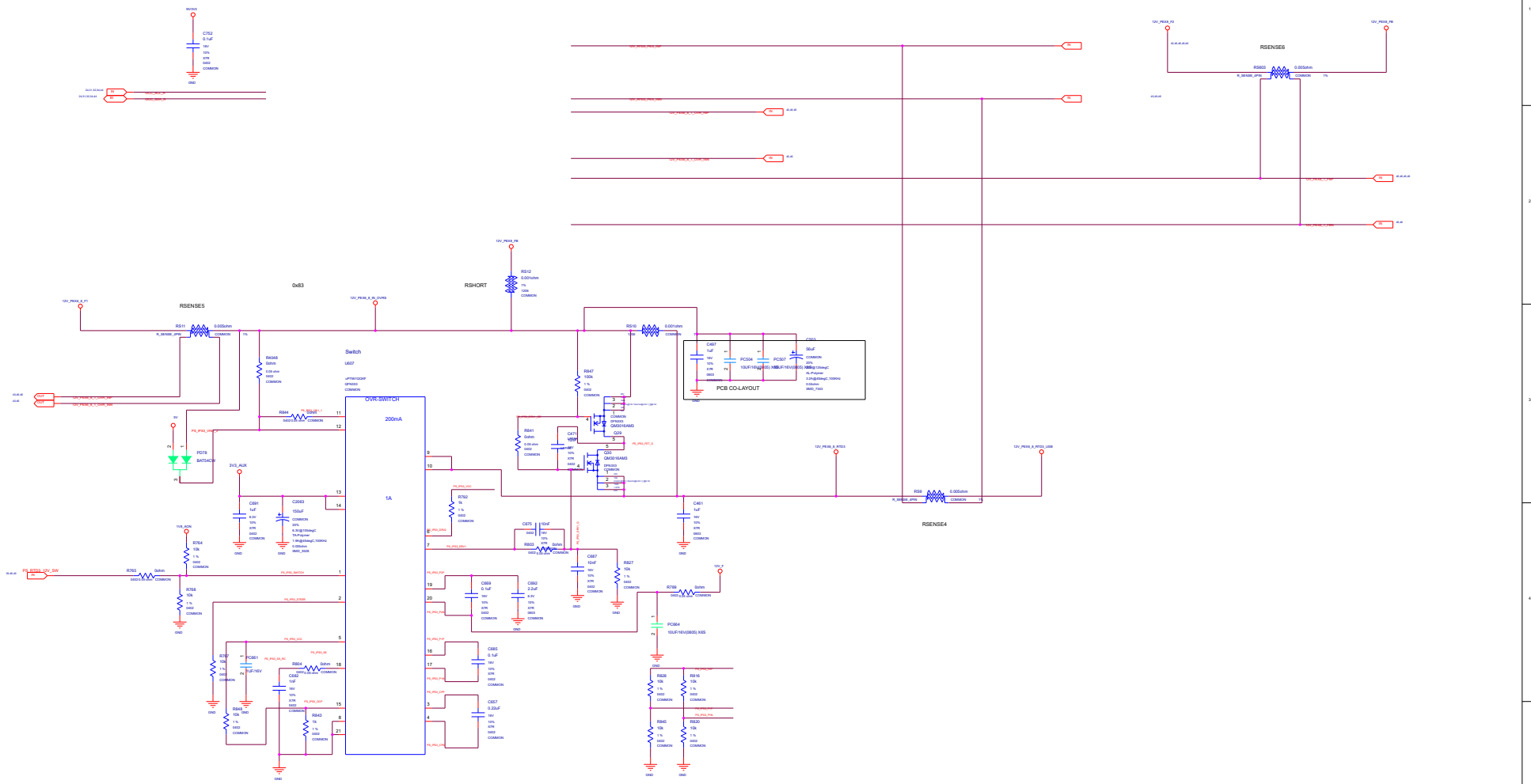
PAGE 40: PS: INPUT SWITCH RTD3 USB



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUT SWITCH RTD3 USB

NVIDIA CORPORATION
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NV_PN	600-1G180-BASE-200		
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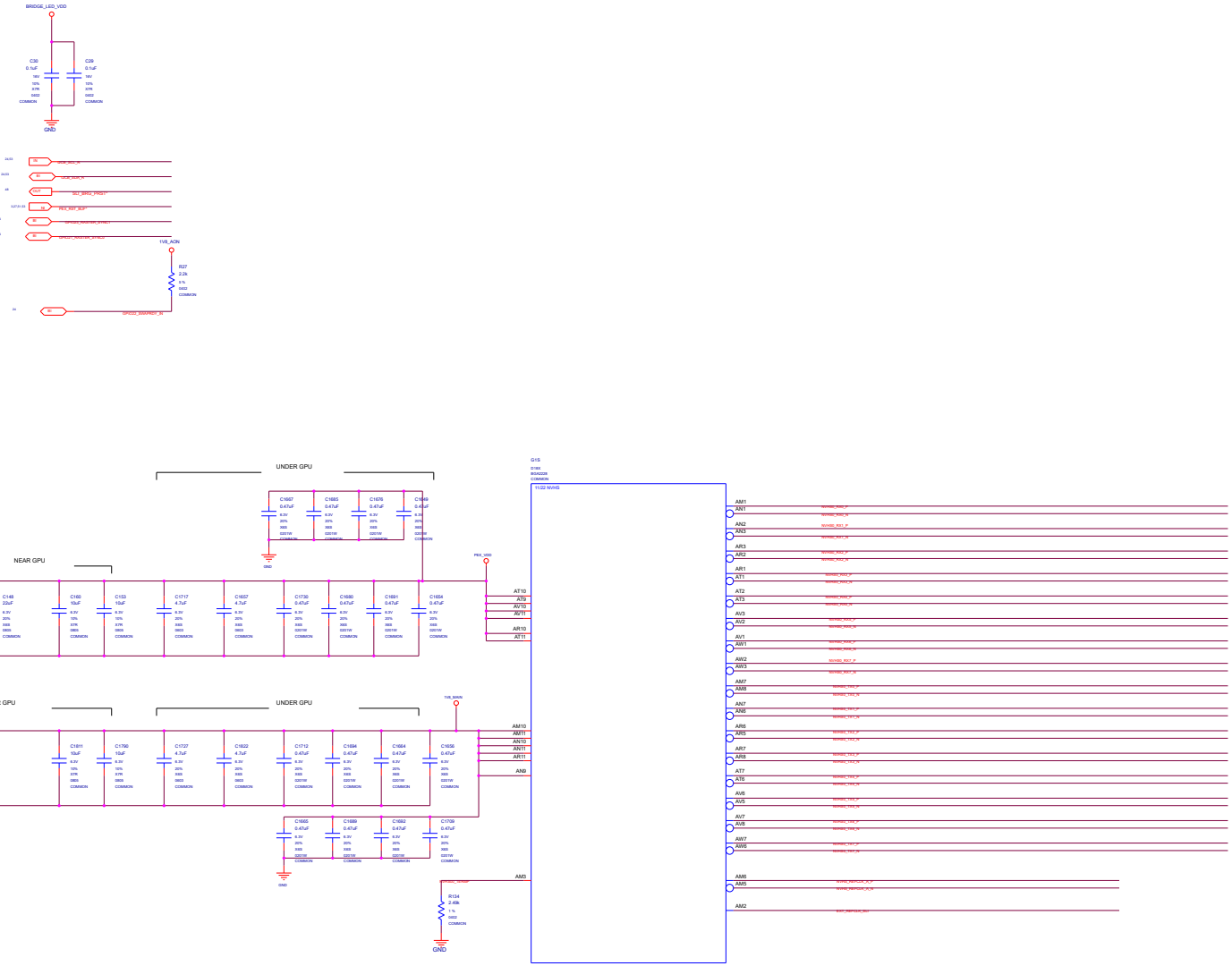
PAGE 23: NVHS Interface



delete NVLINK

delete NVLINK

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	NVHS INTERFACE

NVIDIA CORPORATION
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NV_PN	600-1G180-BASE-200		
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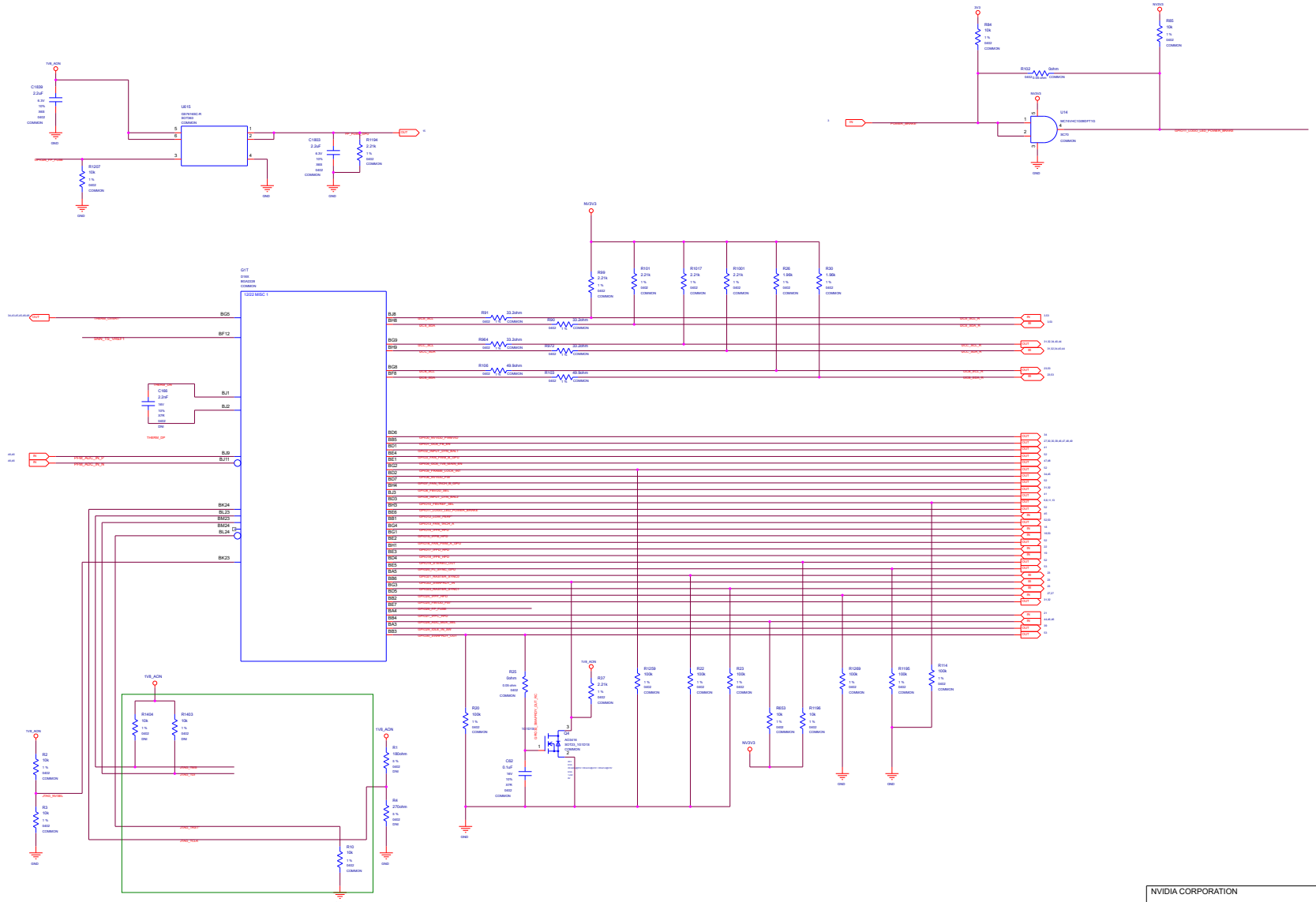

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: FAN,THERMAL,JTAG,GPIO,STEREO

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NV_PN	600-1G180-BASE-200		
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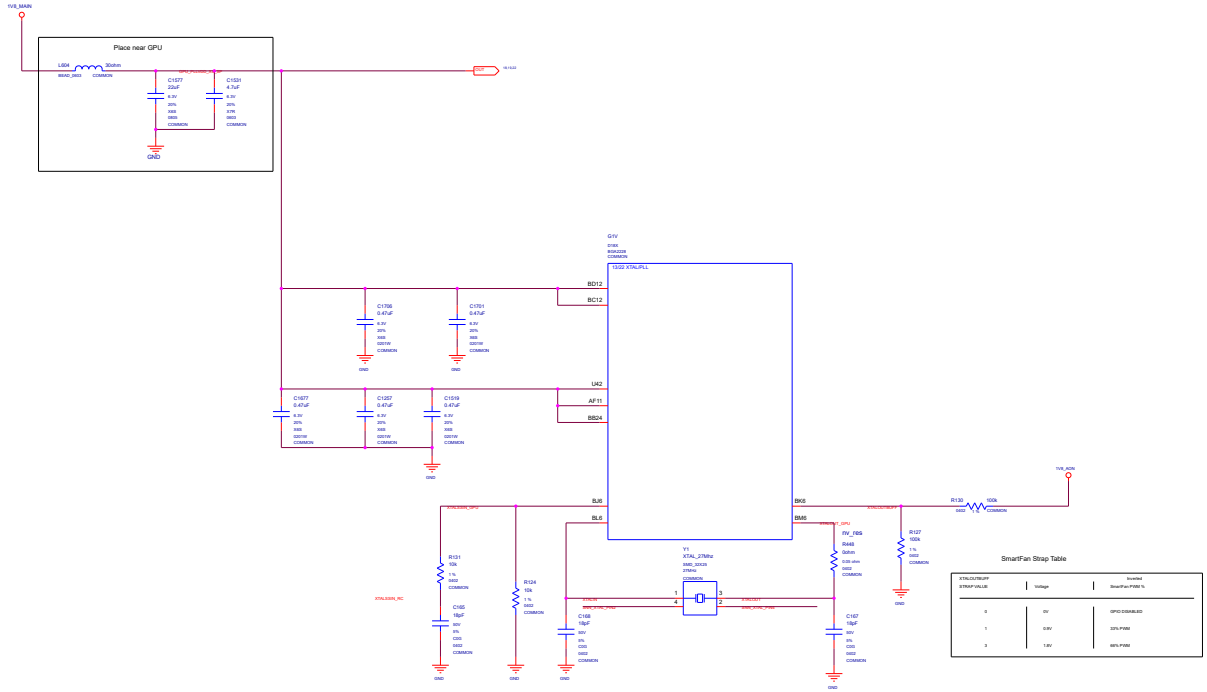
PAGE 26: MISC: XTAL. PLL



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: XTAL. PLL

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NV_PN	600-1G180-BASE-200		
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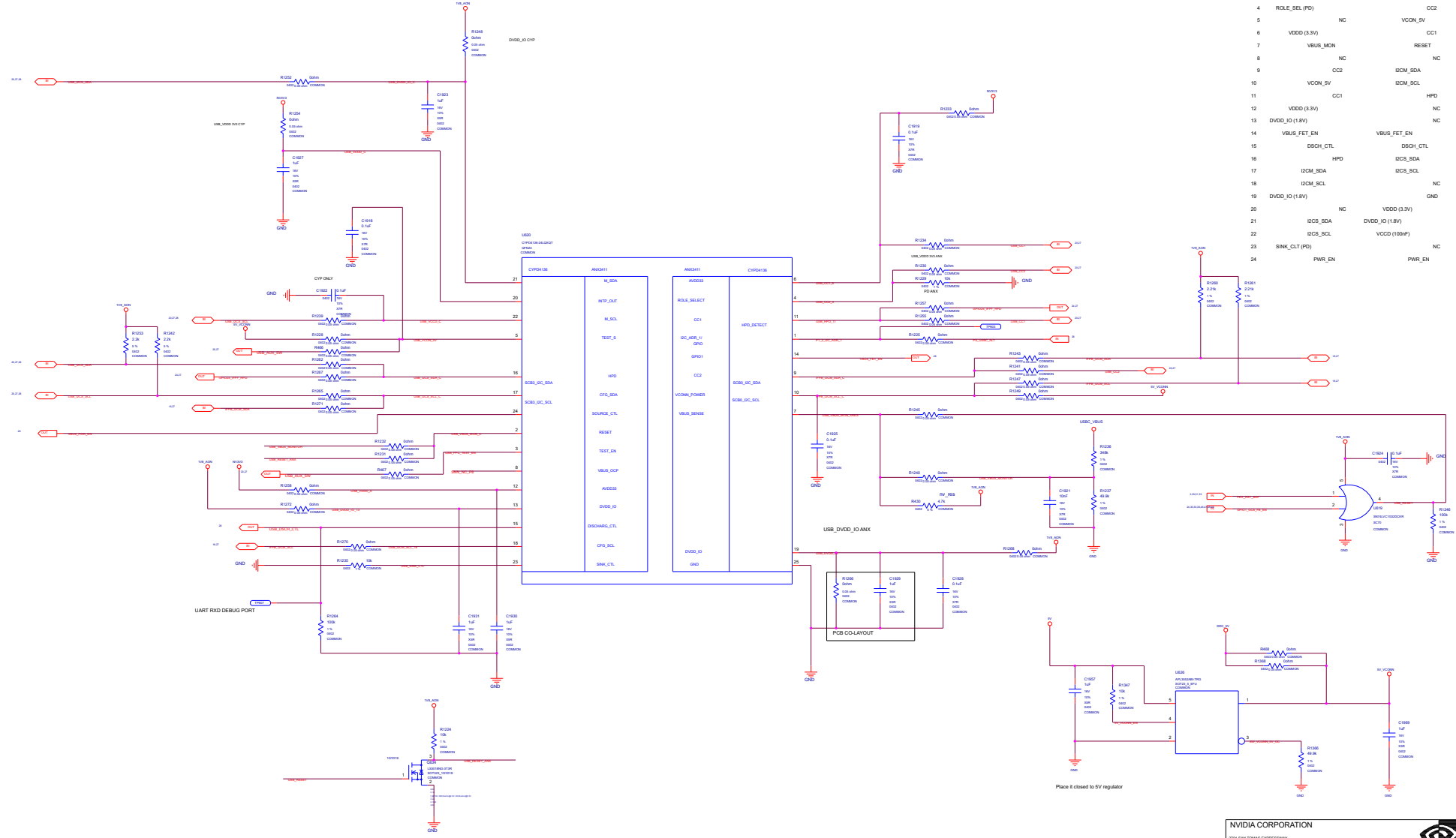
PAGE 27: MISC: USB PPC



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: USB PPC

NVIDIA CORPORATION
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NV_PN	600-1G180-BASE-200		
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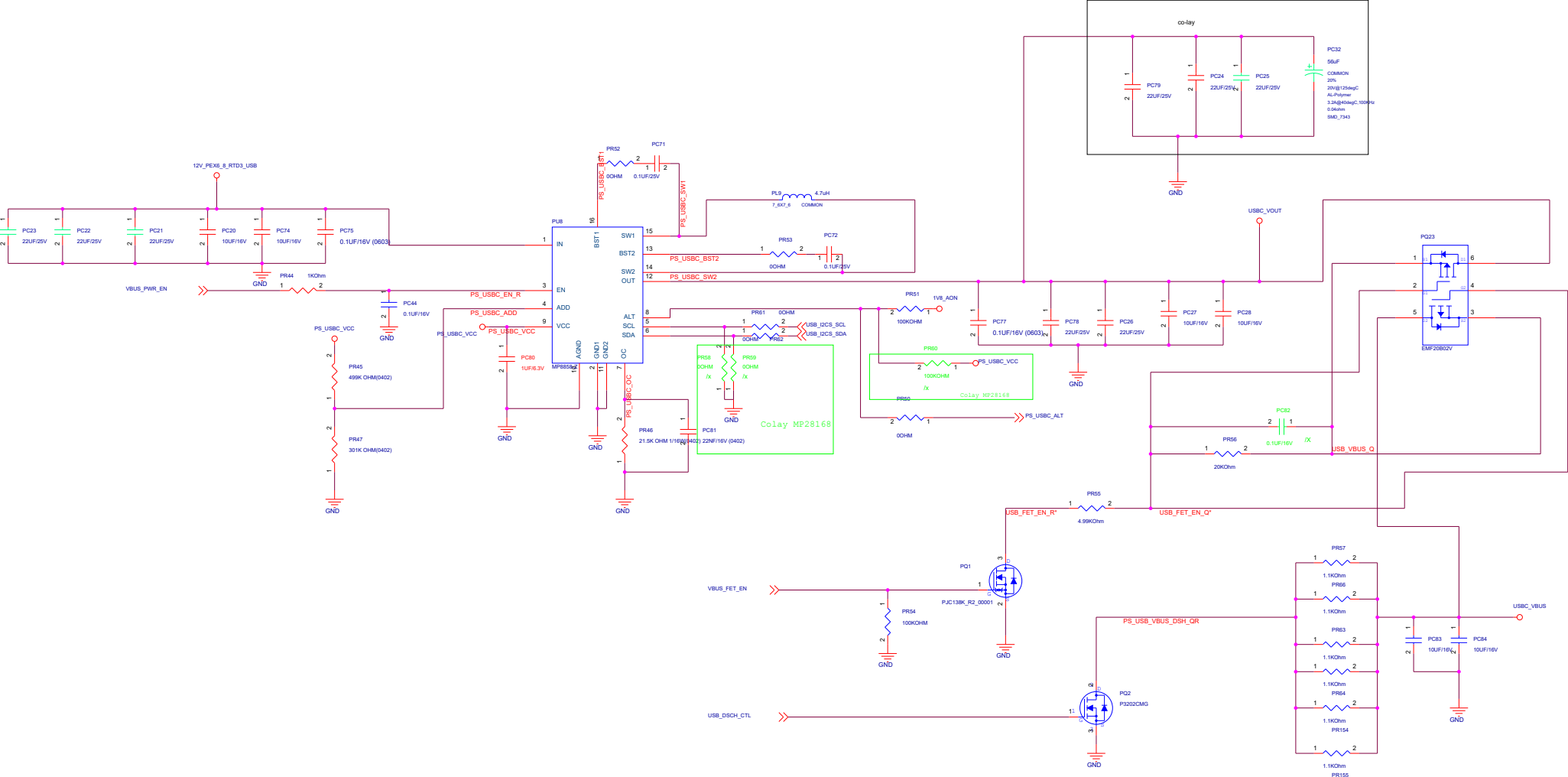
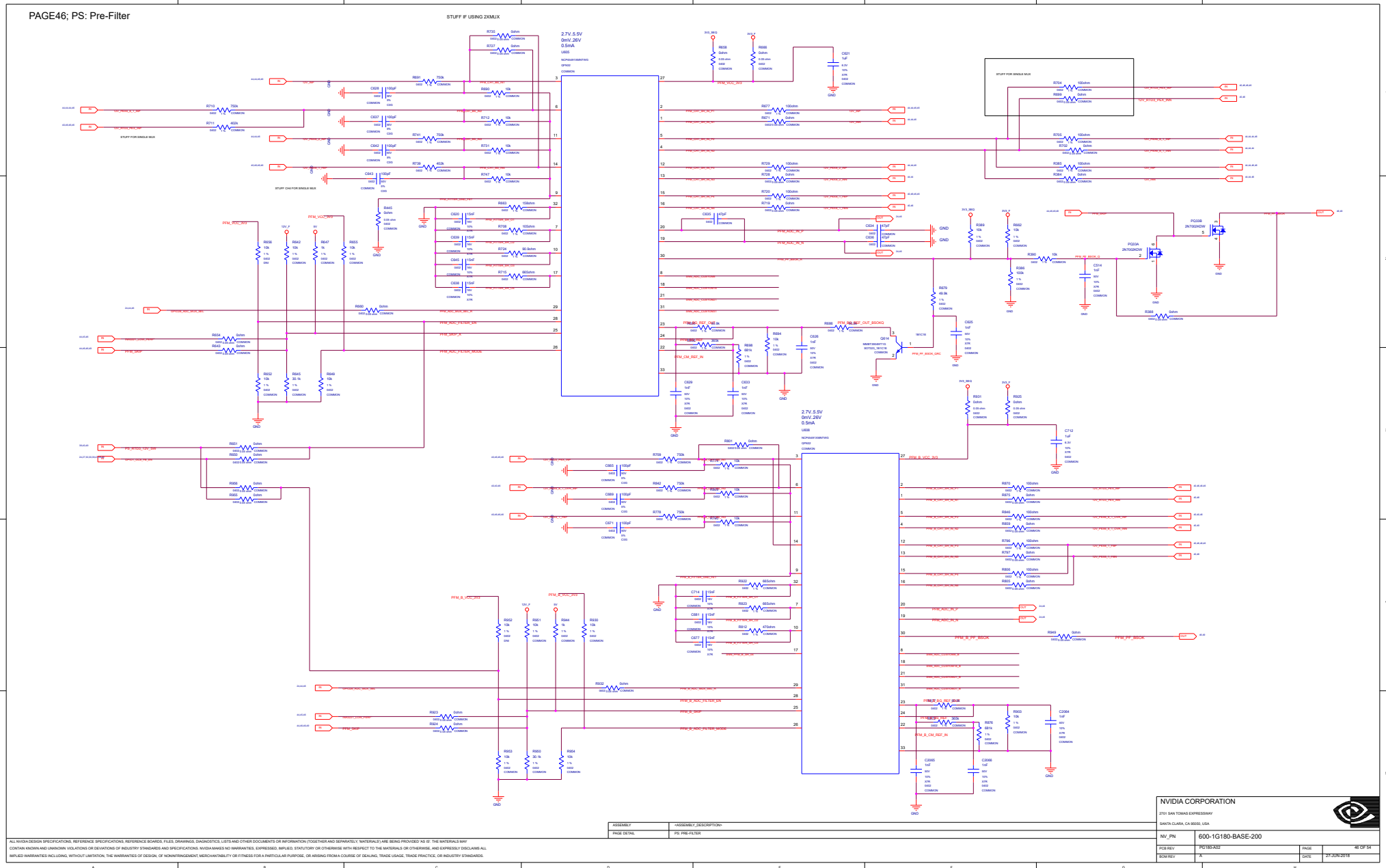

co-lay
PC32
56uF
COMMON
20%
20V@125degC
AL-Polymer
3.2A@40degC,100kHz
0.04ohm
SMD_7343
PC79
22UF/25V
PC24
22UF/25V
PC25
22UF/25V
GND
12V_PEX6_8_RTD3_USB
PC23
22UF/25V
PC22
22UF/25V
PC21
22UF/25V
PC20
10UF/16V
PC74
10UF/16V
PC75
0.1UF/16V (0603)
VBUS_PWR_EN
PR44
1KOhm
PC44
0.1UF/16V
PS_USBC_VCC
PR45
499K OHM(0402)
PR47
301K OHM(0402)
PS_USBC_EN_R
PS_USBC_ADD
PS_USBC_VCC
PC80
1UF/6.3V
PU8
MP8858GZ
IN
EN
ADD
VCC
AGND
GND1
GND2
BST1
SW1
BST2
SW2
OUT
ALT
SCL
SDA
OC
PR52
0OHM
PC71
0.1UF/25V
PS_USBC_BST1
PS_USBC_SW1
PL9
7_6X7_6
4.7uH
COMMON
PR53
0OHM
PC72
0.1UF/25V
PS_USBC_BST2
PS_USBC_SW2
PR61
0OHM
PR62
0OHM
USB_I2CS_SCL
USB_I2CS_SDA
PR58
0OHM
/x
PR59
0OHM
/x
Colay MP28168
PS_USBC_OC
PR46
21.5K OHM 1/16W (0402)
PC81
22NF/16V (0402)
PR51
1V8_AON
100KOHM
PR60
100KOHM
/x
PS_USBC_VCC
Colay MP28168
PR50
0OHM
PS_USBC_ALT
USBC_VOUT
PC77
0.1UF/16V (0603)
PC78
22UF/25V
PC26
22UF/25V
PC27
10UF/16V
PC28
10UF/16V
PQ23
EMF20B02V
PC82
0.1UF/16V
/X
PR56
20KOhm
USB_VBUS_Q
PR55
4.99KOhm
USB_FET_EN_R*
USB_FET_EN_Q*
PQ1
PJC138K_R2_00001
VBUS_FET_EN
PR54
100KOHM
PS_USB_VBUS_DSH_QR
PQ2
P3202CMG
USB_DSCH_CTL
PR57
1.1KOhm
PR66
1.1KOhm
PR63
1.1KOhm
PR64
1.1KOhm
PR154
1.1KOhm
PR155
1.1KOhm
USBC_VBUS
PC83
10UF/16V
PC84
10UF/16V


PAGE46; PS: Pre-Filter
STUFF IF USING 2XMUX
2.7V..5.5V
0mV..26V
0.5mA
U605
NCP45491SN90T3WG
DFN10
COMMON
2.7V..5.5V
0mV..26V
0.5mA
U606
NCP45491SN90T3WG
DFN10
COMMON
STUFF FOR SINGLE MUX
STUFF CNX FOR SINGLE MUX
GND
3V3_SEQ
3V3_P
2V5_P
12V_P
9V
PFM_VCC_3V3
PFM_B_VCC_3V3
PFM_VCC_2V5
PFM_B_VCC_2V5
PFM_VCC_12V
PFM_B_VCC_12V
PFM_PF_BSCK
PFM_B_PF_BSCK
PFM_PF_BSDI
PFM_B_PF_BSDI
PFM_PF_BSCK_G
PFM_B_PF_BSCK_G
PFM_PF_BSDI_G
PFM_B_PF_BSDI_G
PFM_ADC_FILTER_SIN
PFM_B_ADC_FILTER_SIN
PFM_ADC_FILTER_MODE
PFM_B_ADC_FILTER_MODE
PFM_CM_REF_IN
PFM_B_CM_REF_IN
PFM_PF_BSCK_QRC
PFM_B_PF_BSCK_QRC
PFM_PB_REF_OUT_BSCKQ
PFM_B_PB_REF_OUT_BSCKQ
PC33A
2N7002KDW
PC33B
2N7002KDW
NVIDIA CORPORATION
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NV_PN
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A
PAGE
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DATE
27-JUN-2018
ASSEMBLY
<ASSEMBLY_DESCRIPTION>
PAGE DETAIL
PS: PRE-FILTER
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY
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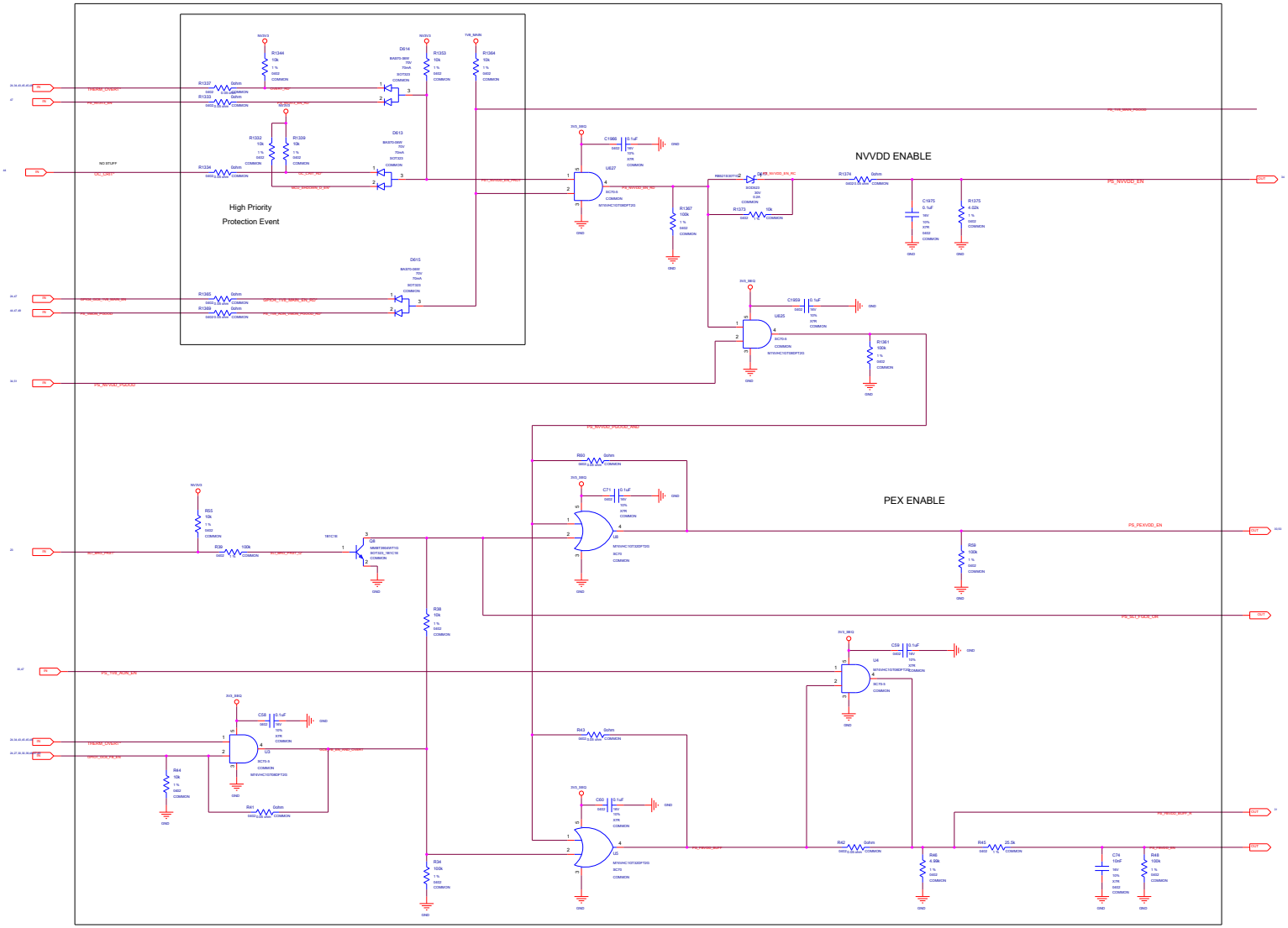

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQUENCE: NV, PEX, FB ENABLE

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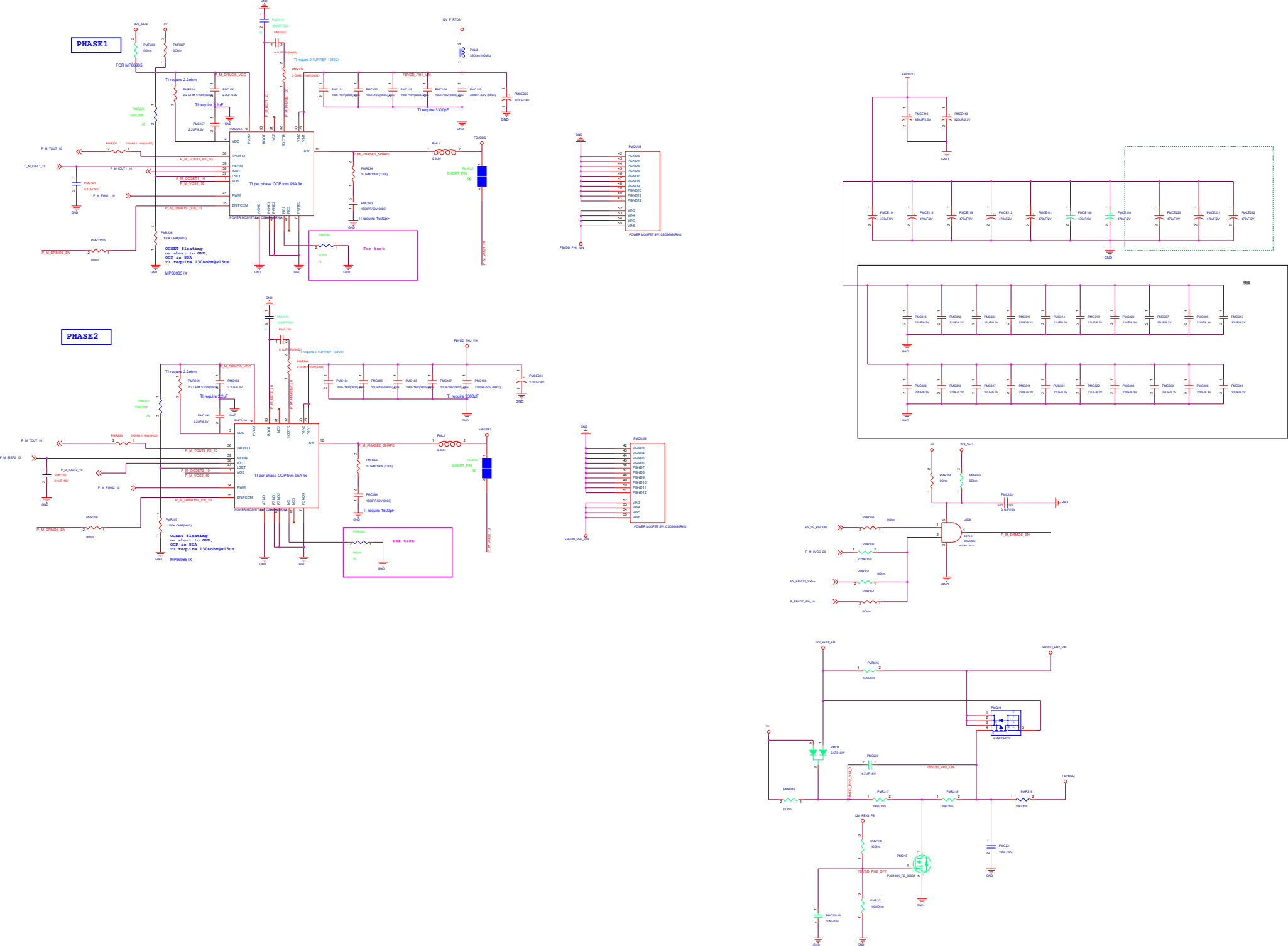
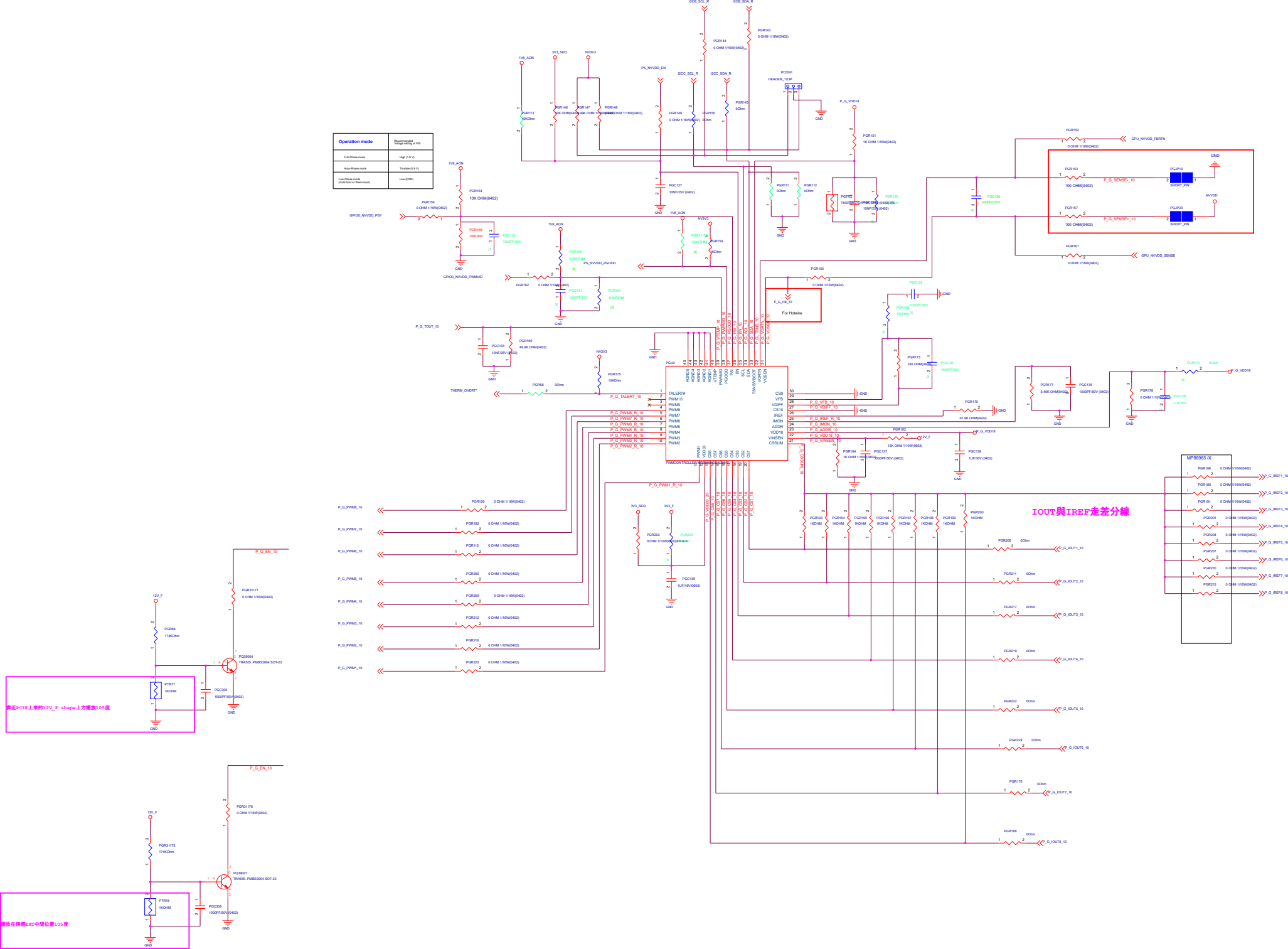

PHASE1
PHASE2
MP86985 /X
OCSET floating
or short to GND,
OCP is 80A
TI require 130Kohm@815uH
TI per phase OCP trim 95A fix
For test
TI require 2.2ohm
TI require 2.2uF
TI require 3300pF
TI require 1500pF
TI require 0.1UF/16V (0402)
FOR MP86985
SHORT_PIN
POWER MOSFET SW: CSD85480RRU


Operation mode
Recommended Voltage setting at PSI
Full-Phase mode
High (1.8 V)
Auto-Phase mode
Tri-state (0.9 V)
Low-Phase mode (Cold boot or Warm boot)
Low (GND)
IOUT與IREF走差分線
靠近PCIE上来的12V_F shape上方摆放105度
摆放在两個EXT中間位置105度

PAGE 54:MECHANICAL;BRACKET/THERMAL SOLUTION

Brackets:

Bracket Screw

1

MEC2
PH_M2.5X4.5X7.5MM_SCREW
PCD
COMMON

new LF screw = 556-0001-000.
ROHS screw = 556-0003-700.

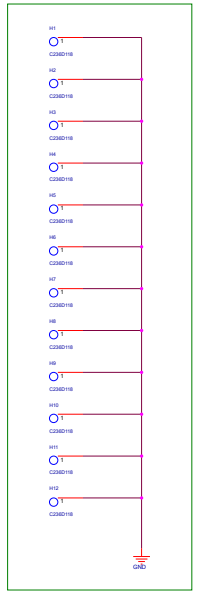
BOARD STIFFENER

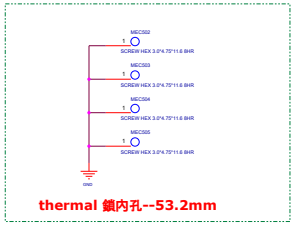
No connected mounting pins

MEC501
Back Cover
NOPIN
COMMON

STIFFENER

Mechanical Holes Symbol





GPU Socket Symbol

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Mechanical: Bracket/Thermal Solution

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SXXXX NOTE

2018/06/14

Power

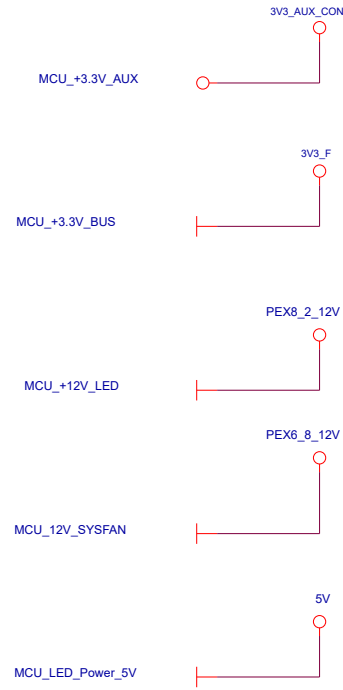
MCU_+3.3V_AUX — From PCIE 3V3_AUX (for ITE)

MCU_+3.3V_BUS — From BUS 3V3 (for ITE logic判斷)

MCU_+12V_LED — From BUS 12V (for Cover LED/RGB Header使用, Max 2.3A)

MCU_12V_SYSFAN — From 12V (for 外接式風扇使用, 任一組12V皆可)

MCU_LED_Power_5V — From 5V (for 背板LED)



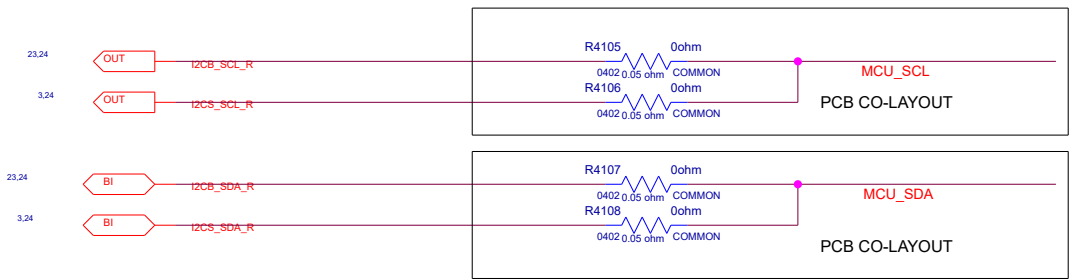
I2C

MCU_SCL
MCU_SDA

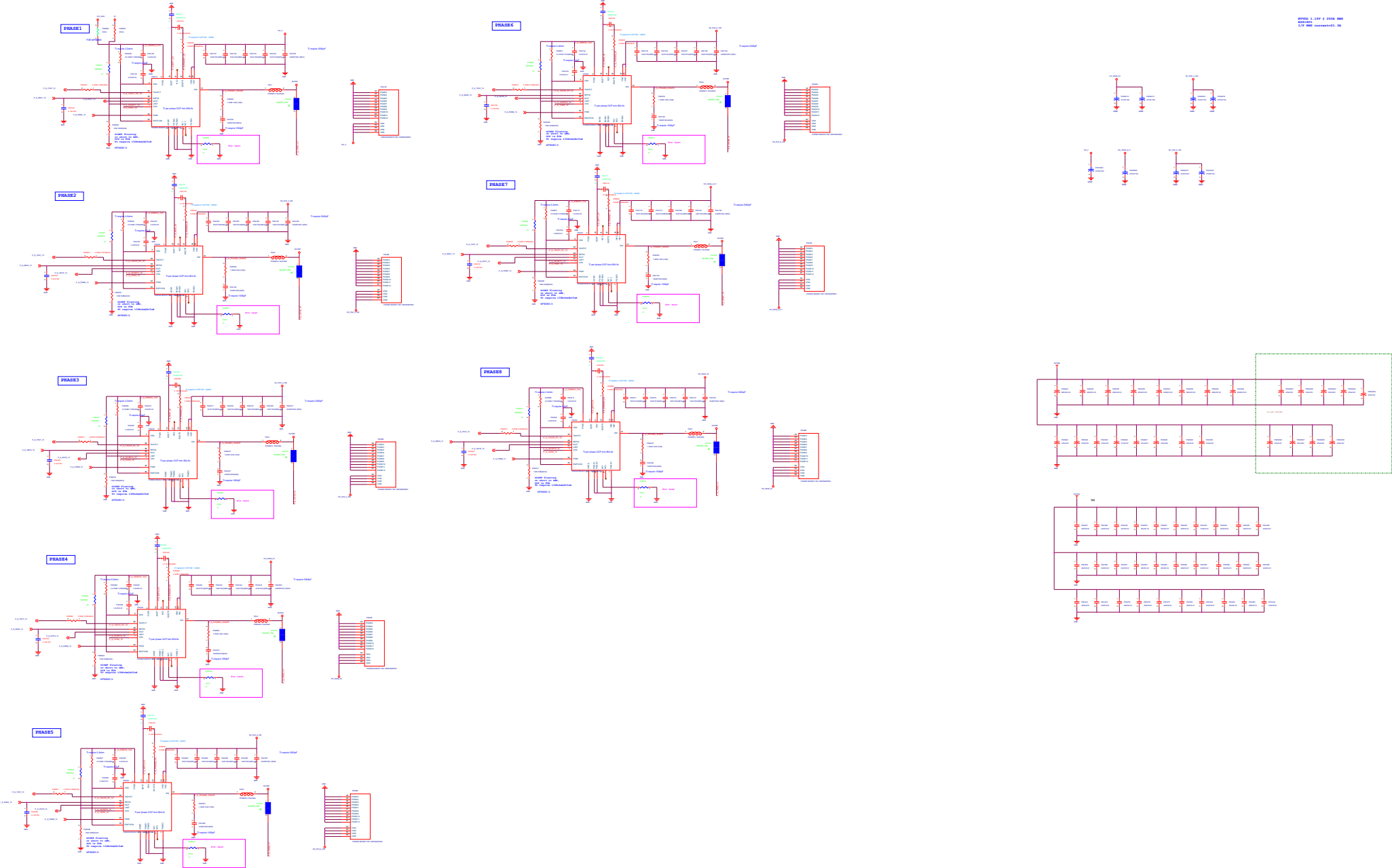
From GPU (for ITE / ENE)

NV I2C 建議使用 I2CB_SDA & I2CB_SCL

Layout前請再與AMD/NV EE Leader or AMD/NV AE 確認



S0000 MCU_POWER

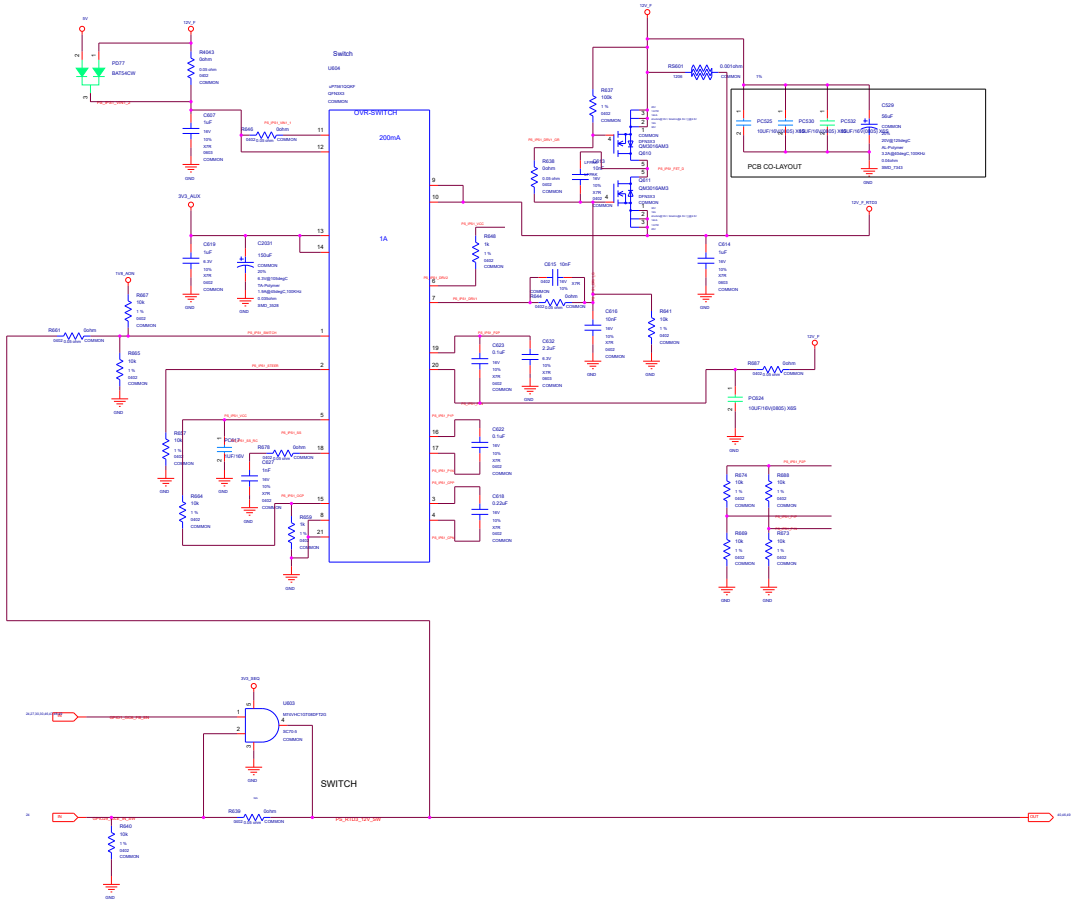

PHASE1
PHASE2
PHASE3
PHASE4
PHASE5
PHASE6
PHASE7
PHASE8
VDDQ 1.19V @ 20A MAX
RAM=8GB
I/F MAX channels=21.3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUT SWITCH RTD3

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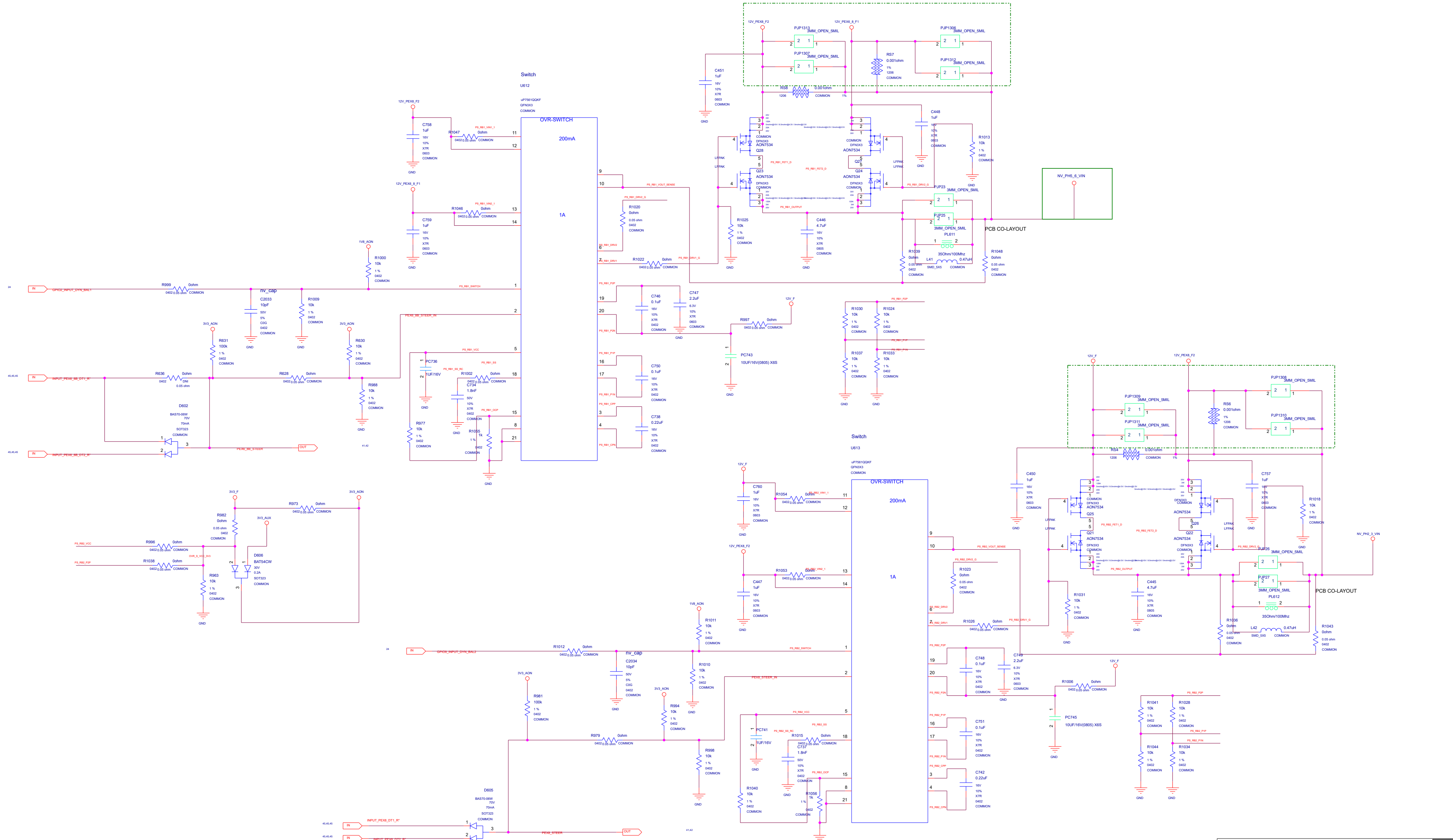
PAGE 41: PS: INPUT SWITCH Rail Balance



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUT SWITCH RAIL BALANCE

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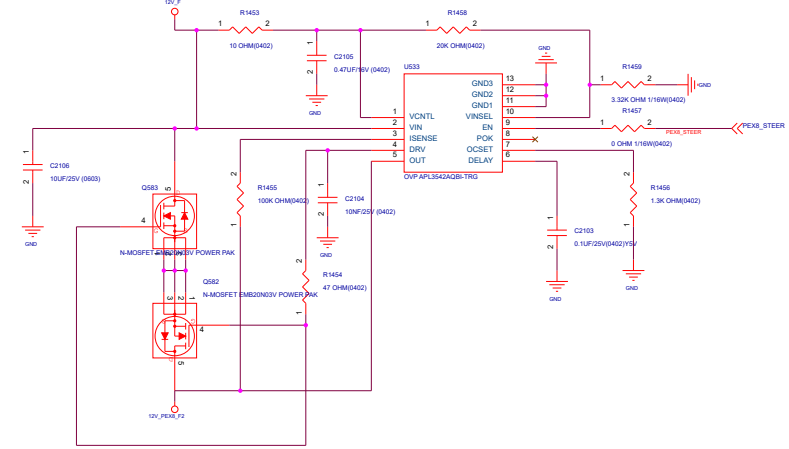
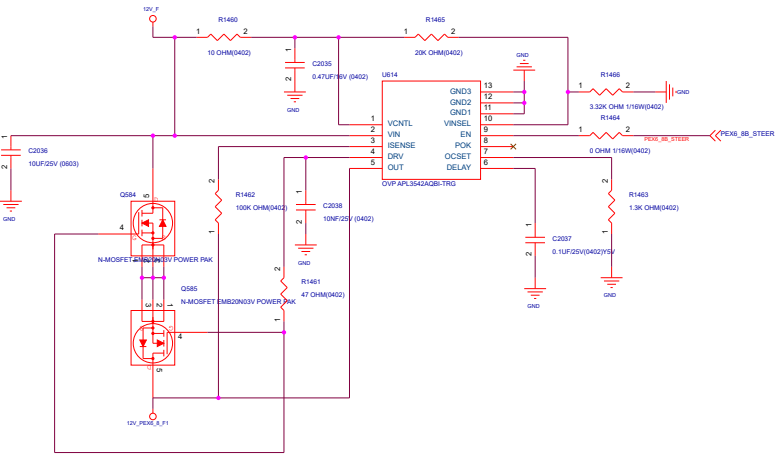
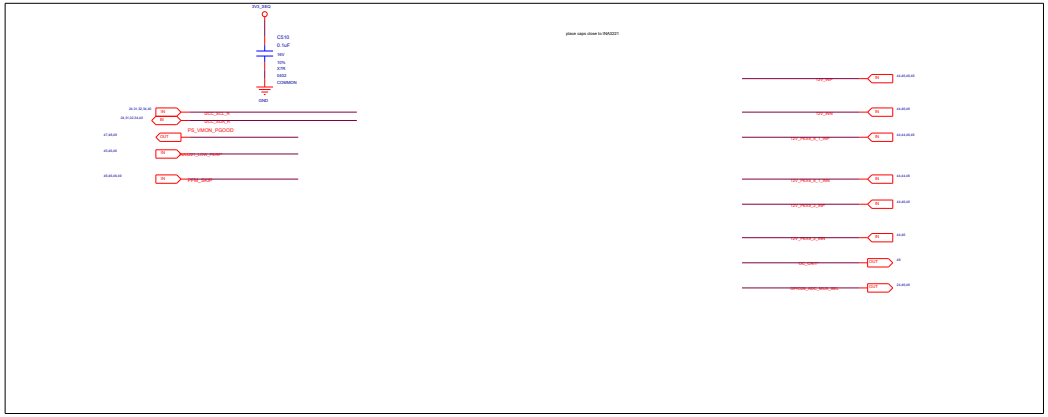


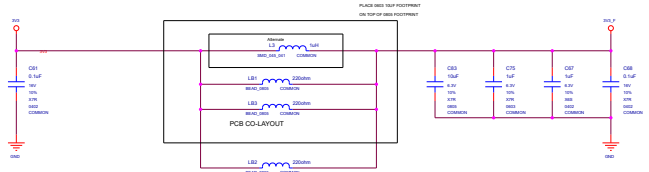


Title	<Title>	
Size: C	Document Number: <Doc>	Rev: <RevCode>
Date: Tuesday, July 31, 2018	Sheet 1 of 1	

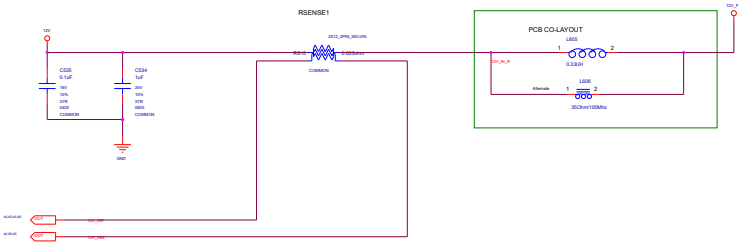
PAGE 44: PS: Inputs, Filtering, and Monitoring



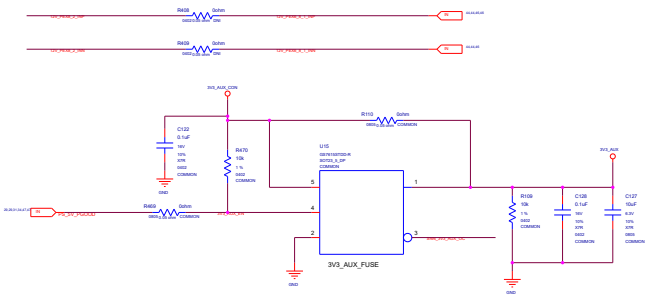
PEX 3V3 INPUT - 10W



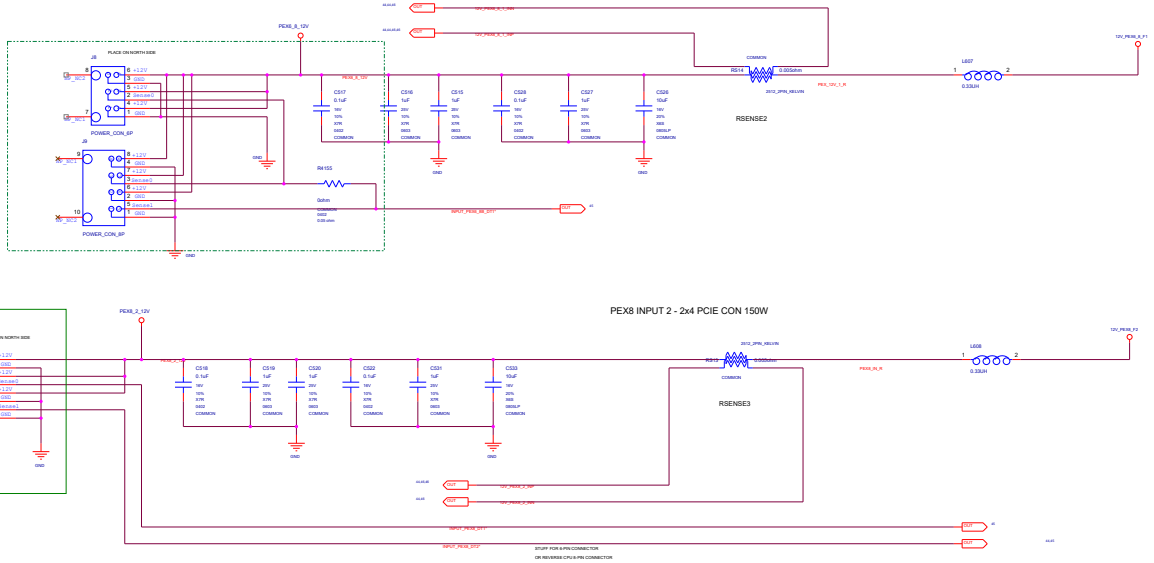
PEX_12V INPUT - 66W



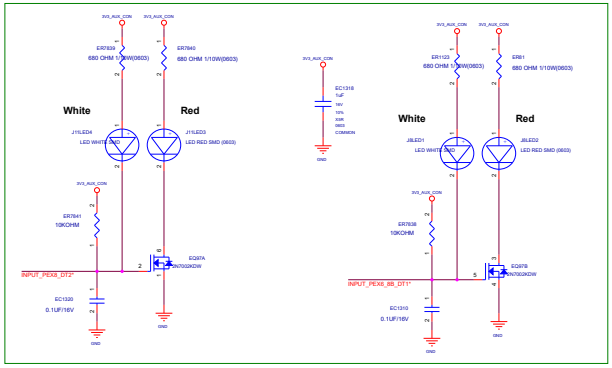
PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUTS, FILTERING AND MONITORING

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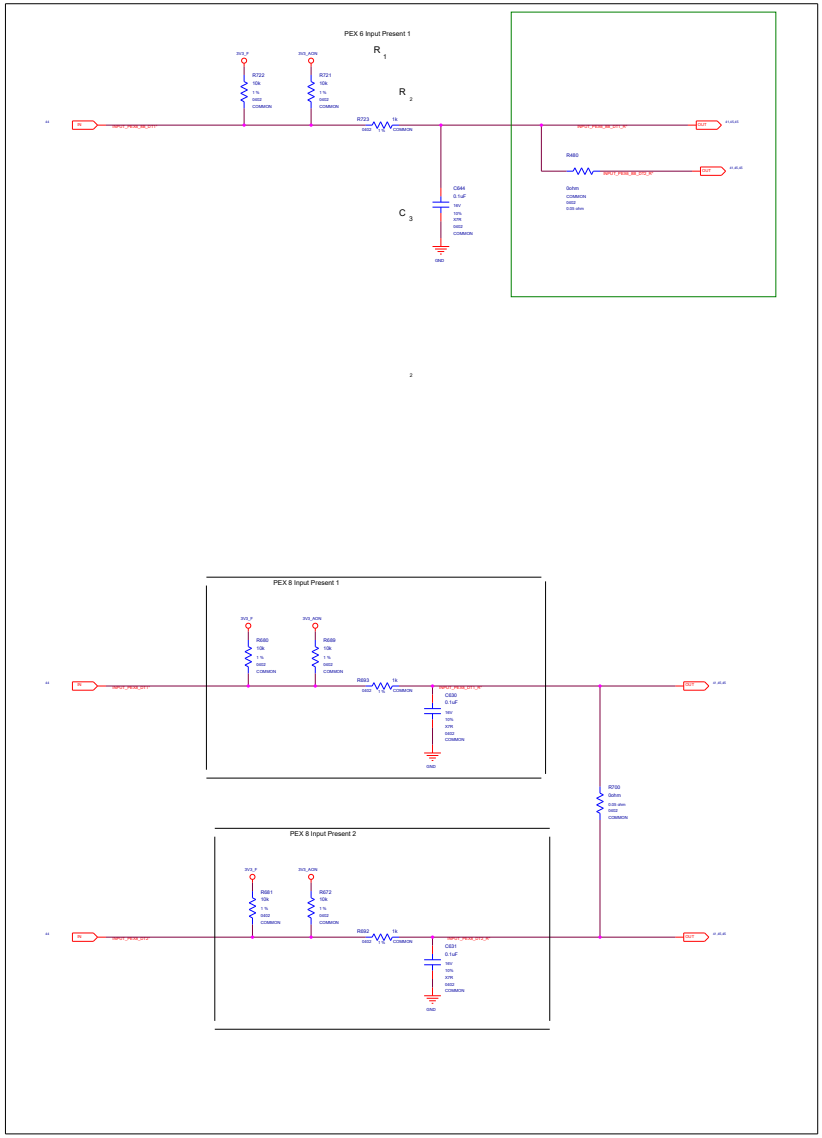
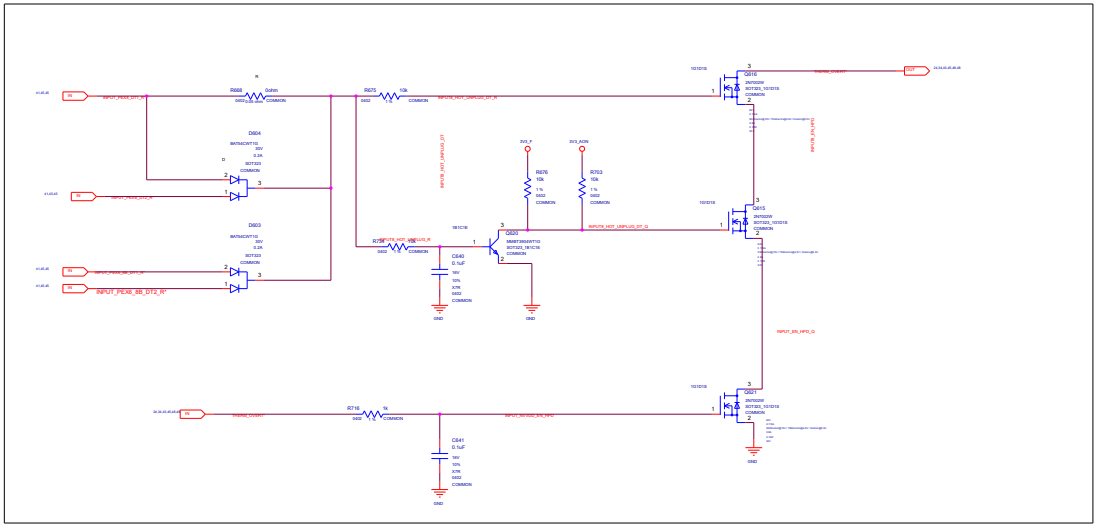
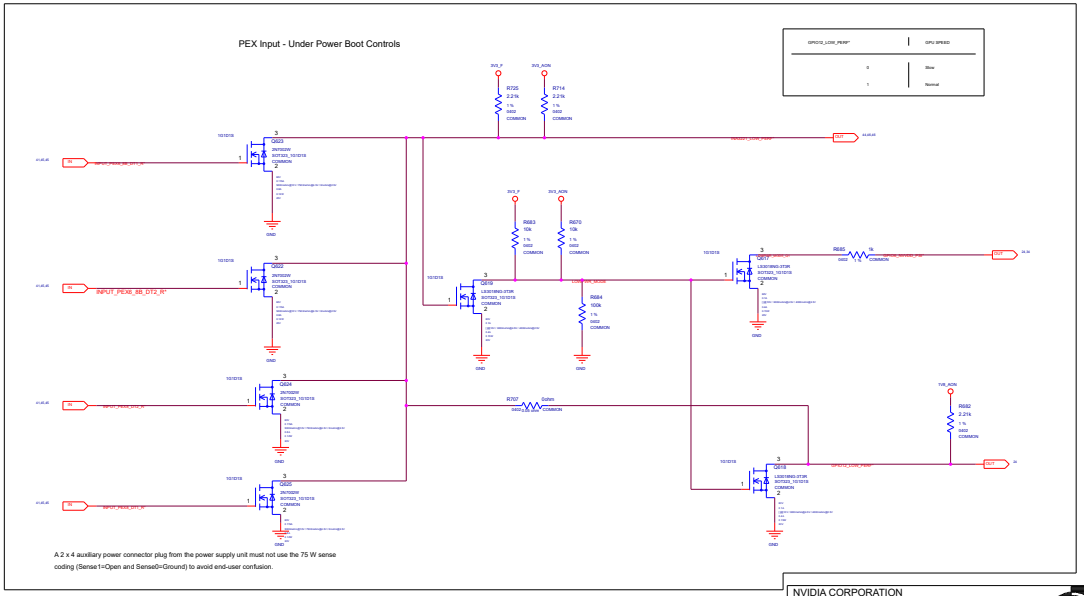
PAGE 45: PS: Hot Unplug Detect







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: CURRENT STEERING,HOT UNPLUG DETECT

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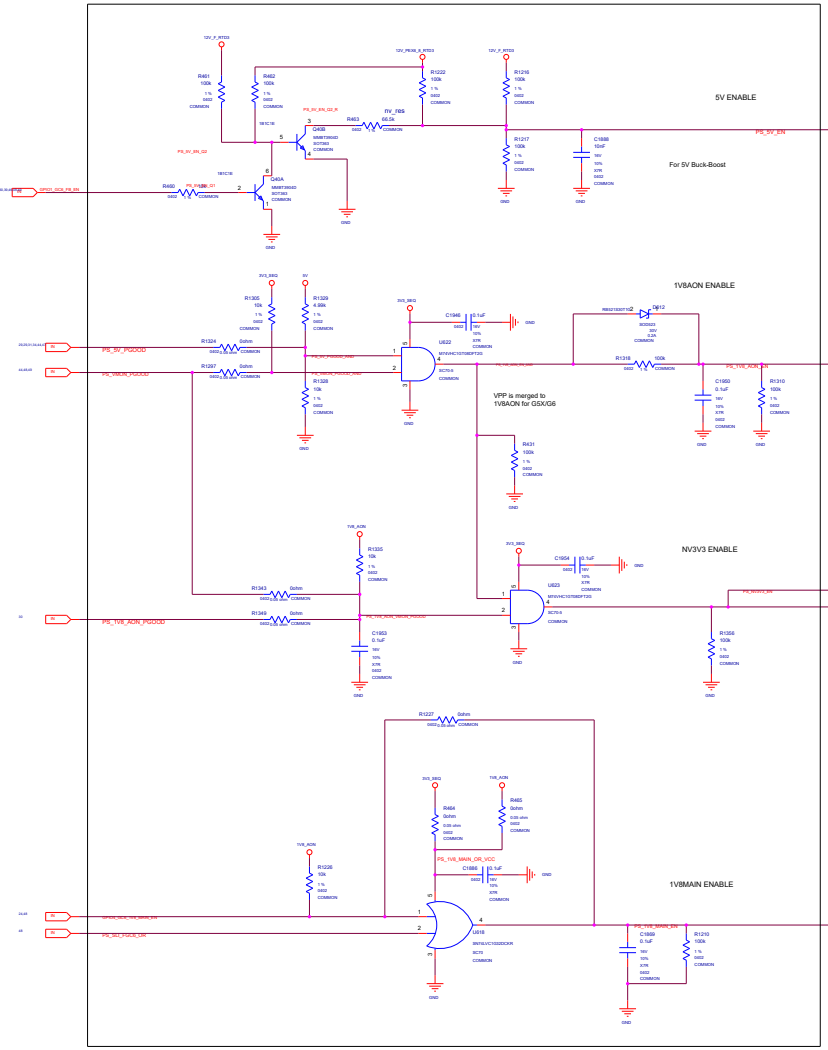
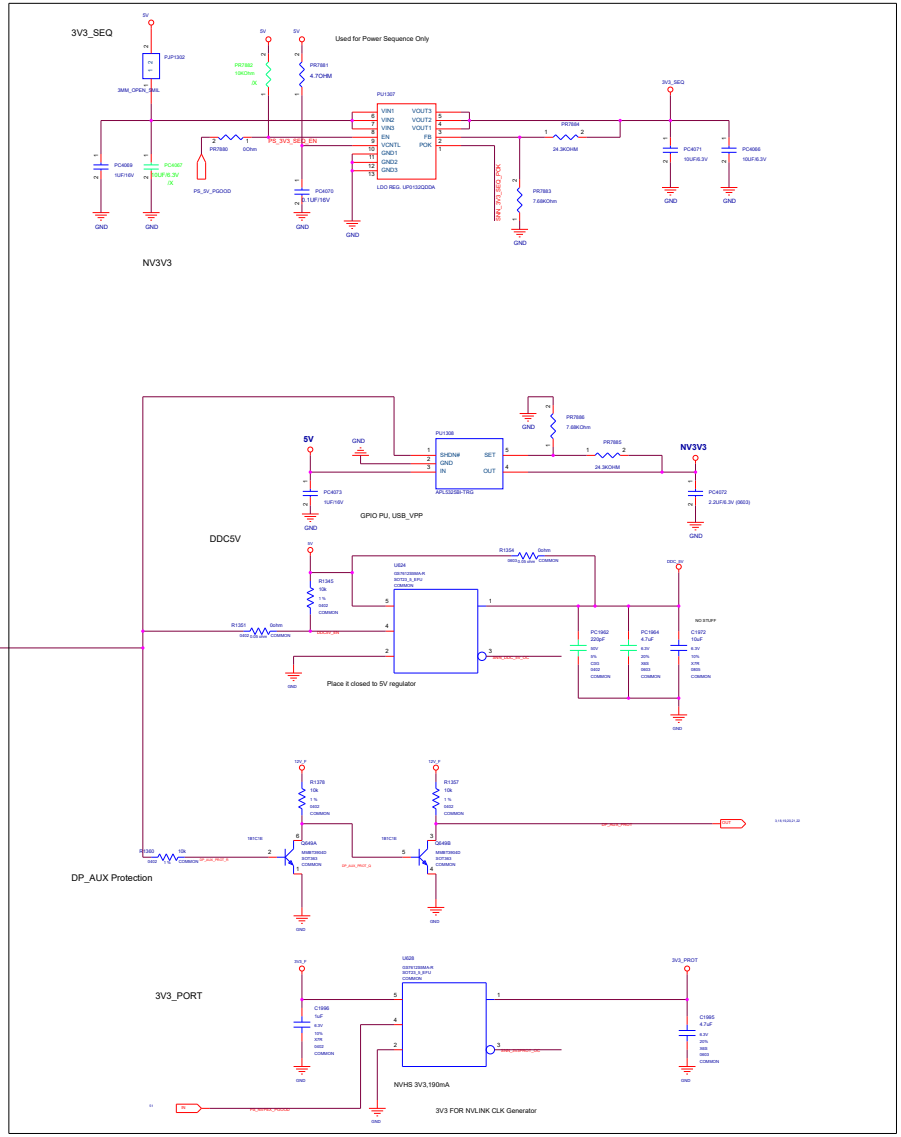
PAGE 47: SEQUENCE:5V,1V8,NV3V3 ENABLE





ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQUENCE: 5V, 1V8, NV3V3 ENABLE

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NV_PN	600-1G180-BASE-200		
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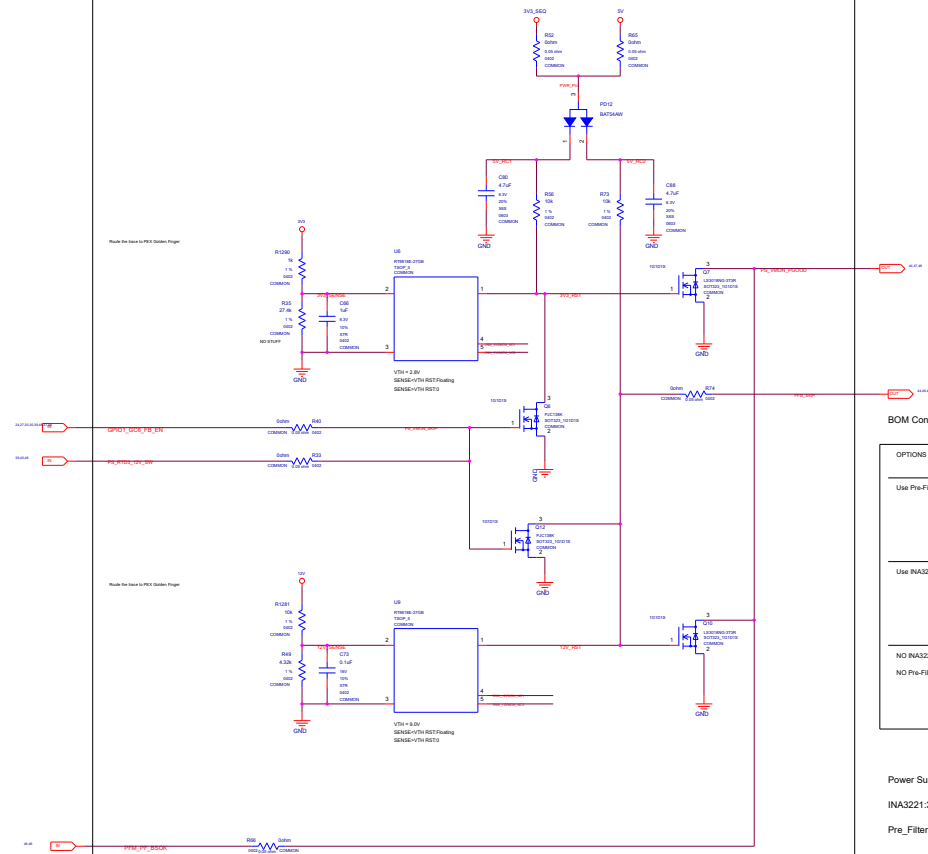
PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(Hi) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQUENCE: PCIE VOLTAGE MONITOR

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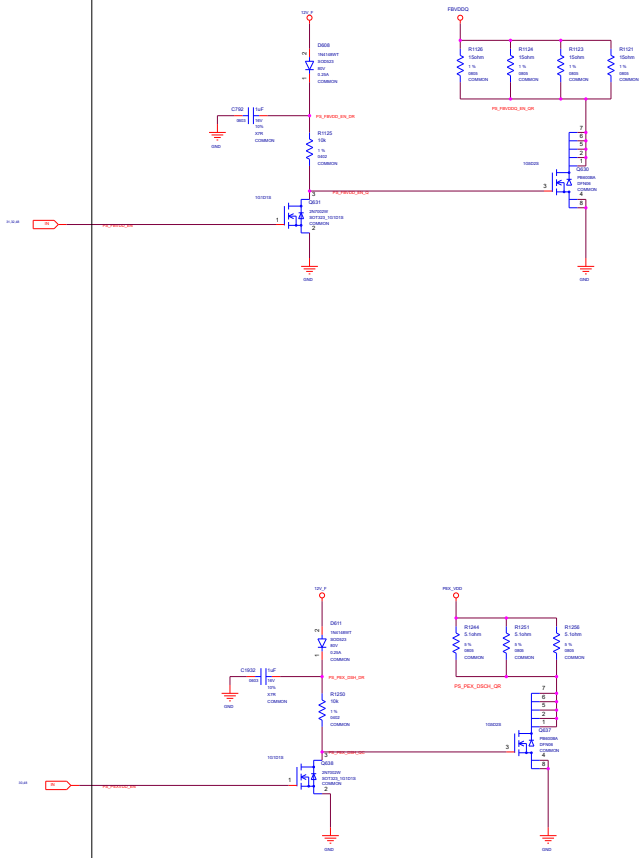
PAGE 50: SEQUENCE:DISCHARGE



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQUENCE: DISCHARGE

NVIDIA CORPORATION
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NV_PN	600-1G180-BASE-200		
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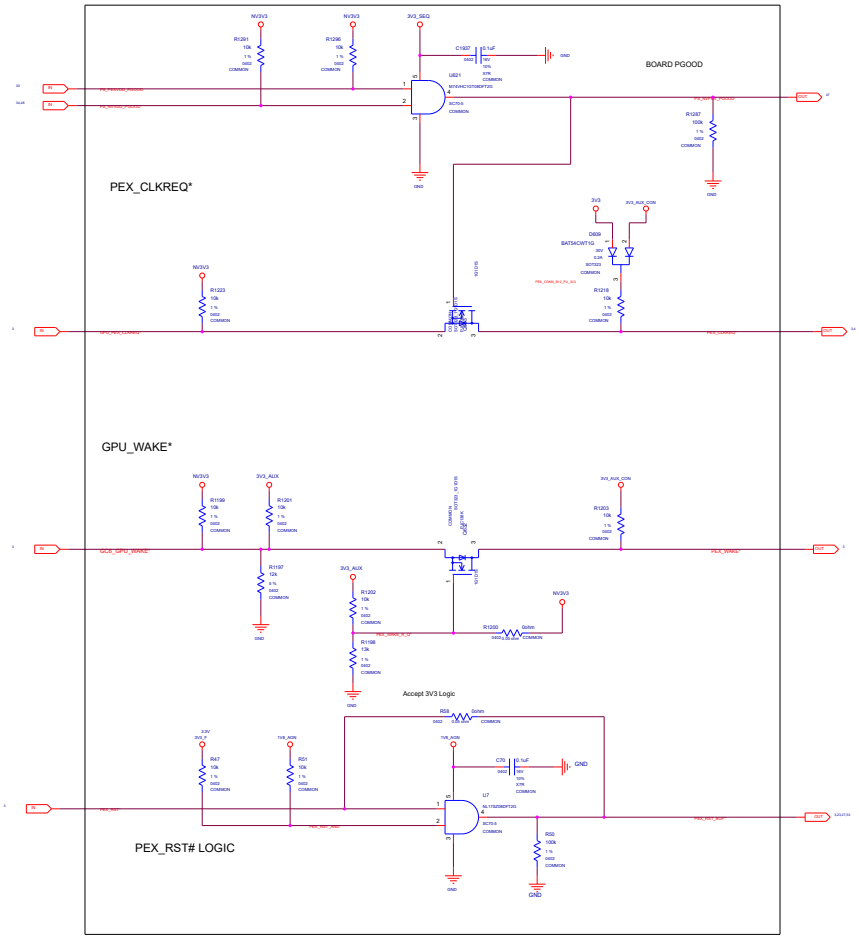
BOM REV	A	DATE	27-JUN-2018

PAGE 51: SEQUENCE:MISC



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQUENCE: MISC

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NV_PN	600-1G180-BASE-200		
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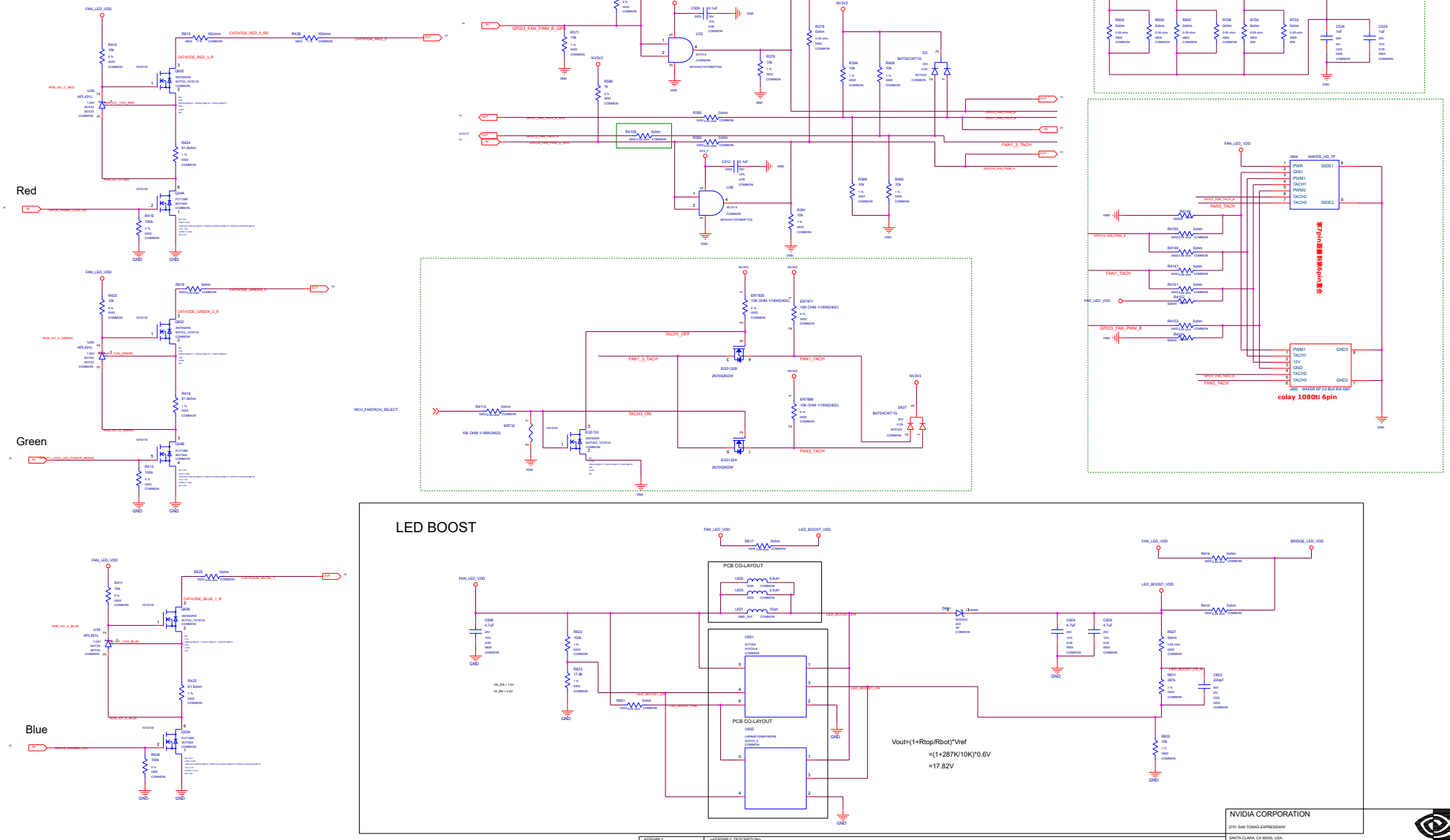
PAGE 52: LED & FAN HEADERS

Red

Green

Blue



LED BOOST

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	LED & FAN HEADERS

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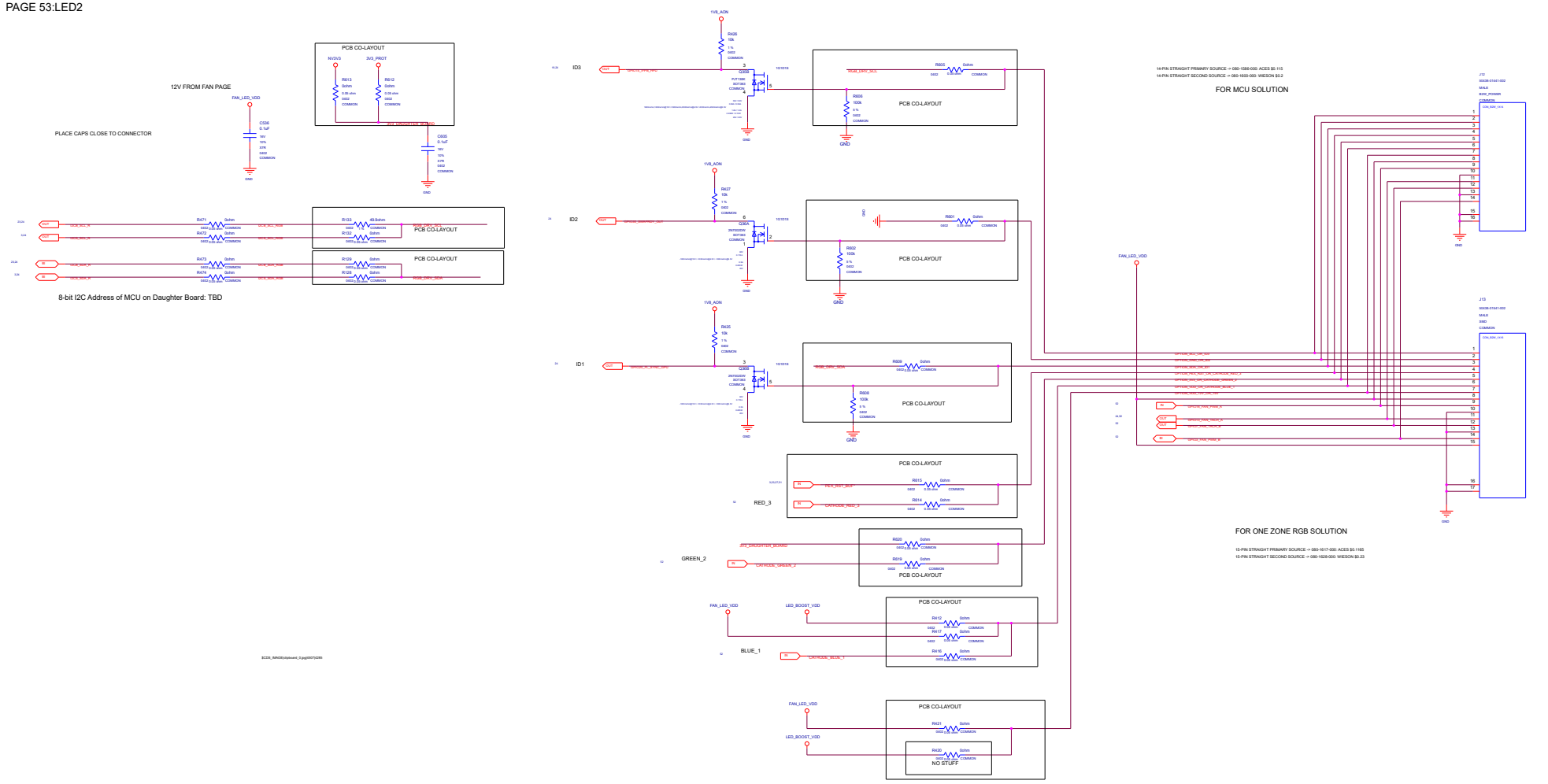
PAGE 53:LED2



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	LED 2

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ASUS VGA PCB Logo

LOGO1
CE
/X

LOGO2
VCCI
/X

LOGO3
EMI_D33005_H
/X

LOGO4
FCC
/X

LOGO5
RCM
/X

LOGO6
CAN ICES-3(B)/NMB-3(B)
/X

LOGO7
/X

LOGO8
UKRAINE

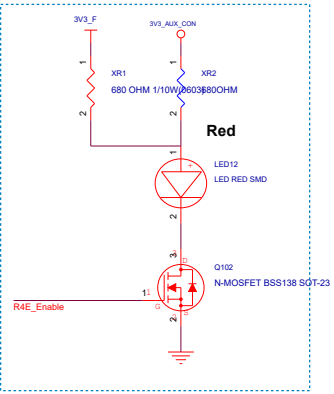
LOGO9
PCB MADE IN CHINA
/X

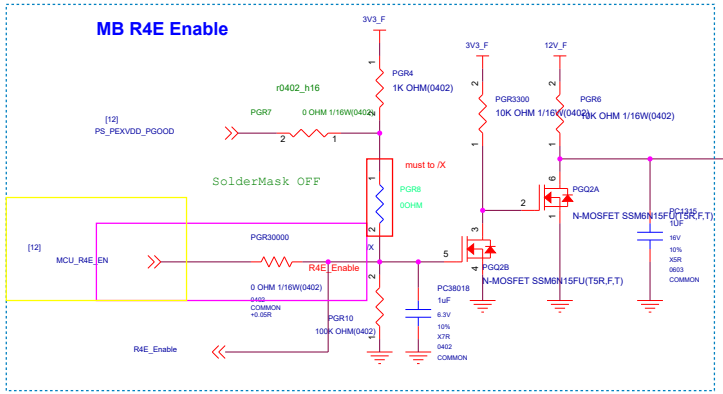
LOGO10
MARK_L
/X

LOGO11
WEEE_LOGO
/X

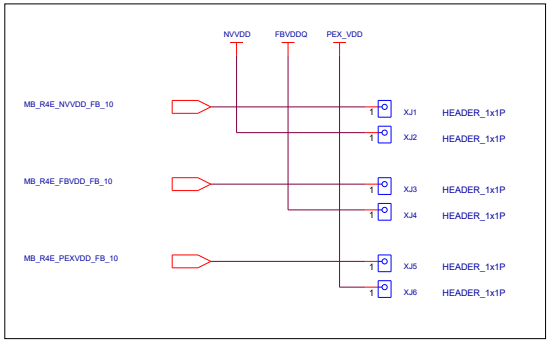
ASUSTEK COMPUTER INC	Title :	PCB Logo	
	Engineer:	Tomo	
Size	Project Name	ASUS VGA Logo	Rev 1.00
Date: Tuesday, July 31, 2018	Sheet 1 of 1		

觸發信號來源需要靠整塊板子最後的POWER RAIL來決定
. 我們會先上PEXVDD這路的PG信號
. 另外預留不上 PEXVDD1這路的PG信號。





MB VGA Hotwire

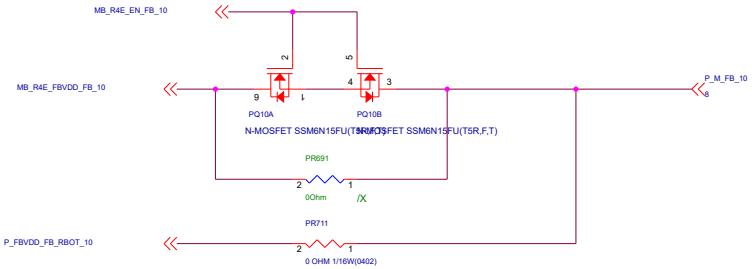


P-STATE VOLTAGES

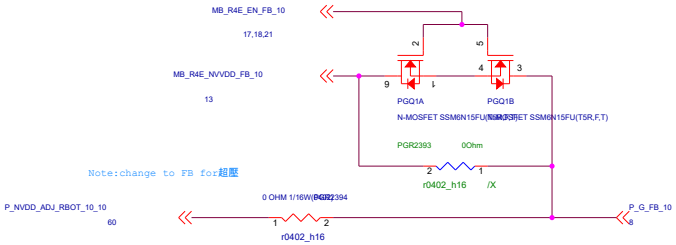
1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V

SOFT START (VR11)

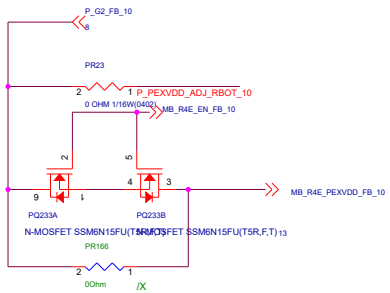
1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPIO tri-state
   VID[5:1]=11000 to set 0.9125V



For MB R4E的預留超壓電路

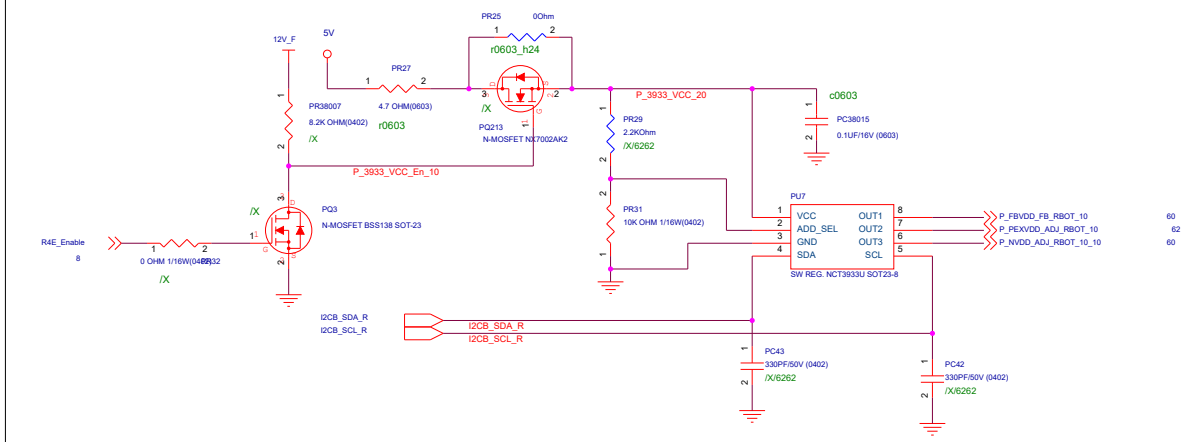


Note:change to LL for超壓(RESERVE)

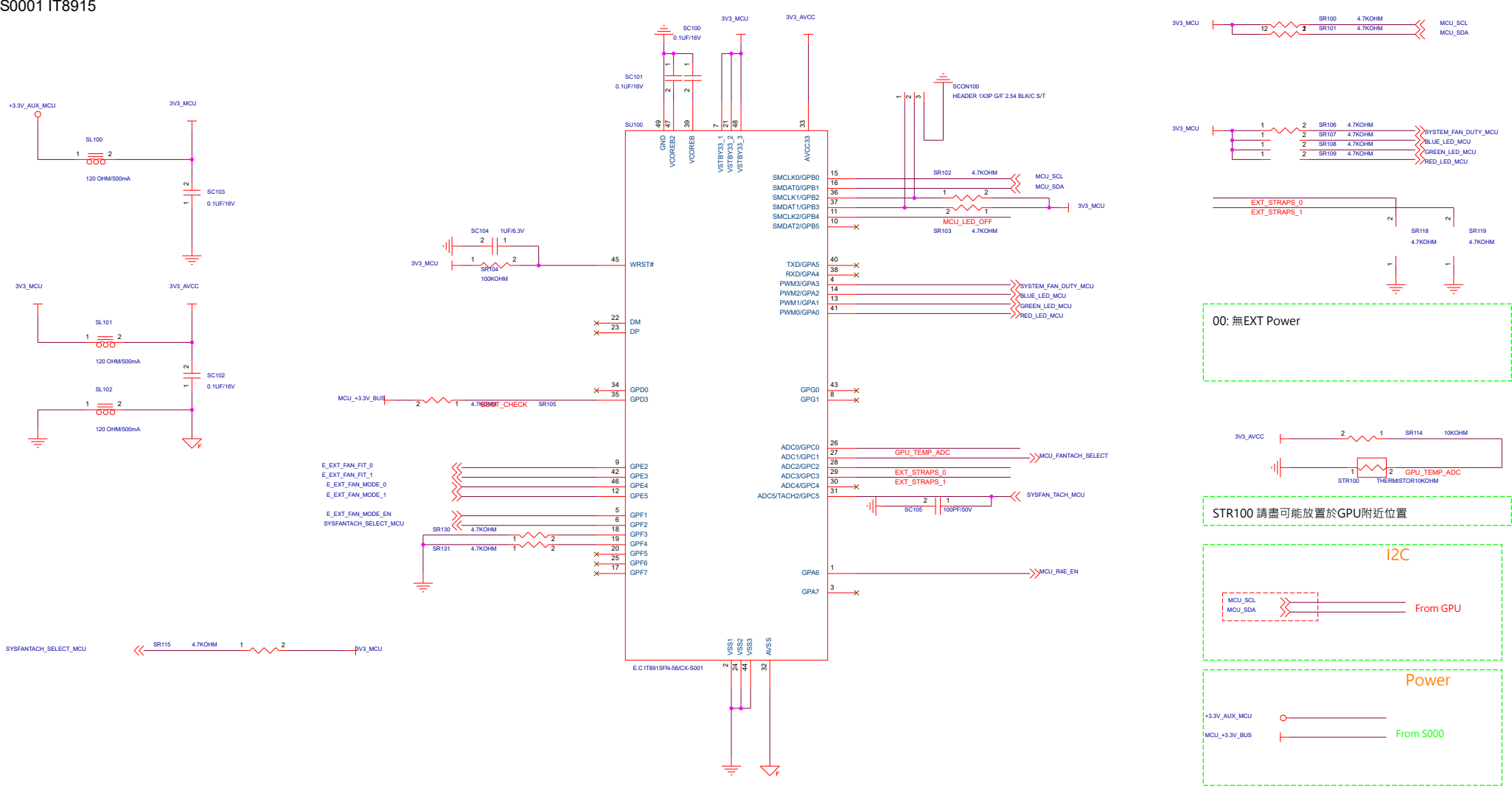


NCT3933U Over Voltage

Address : 0x2A



S0001 IT8915



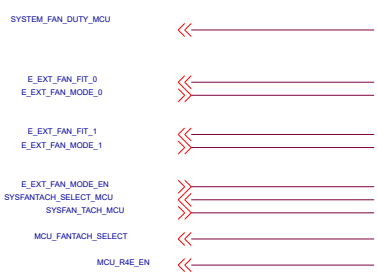
00: 無EXT Power

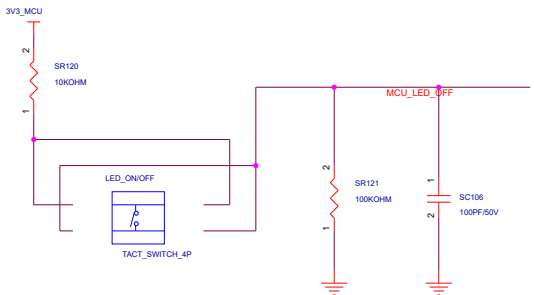
STR100 請盡可能放置於GPU附近位置

I2C

Power

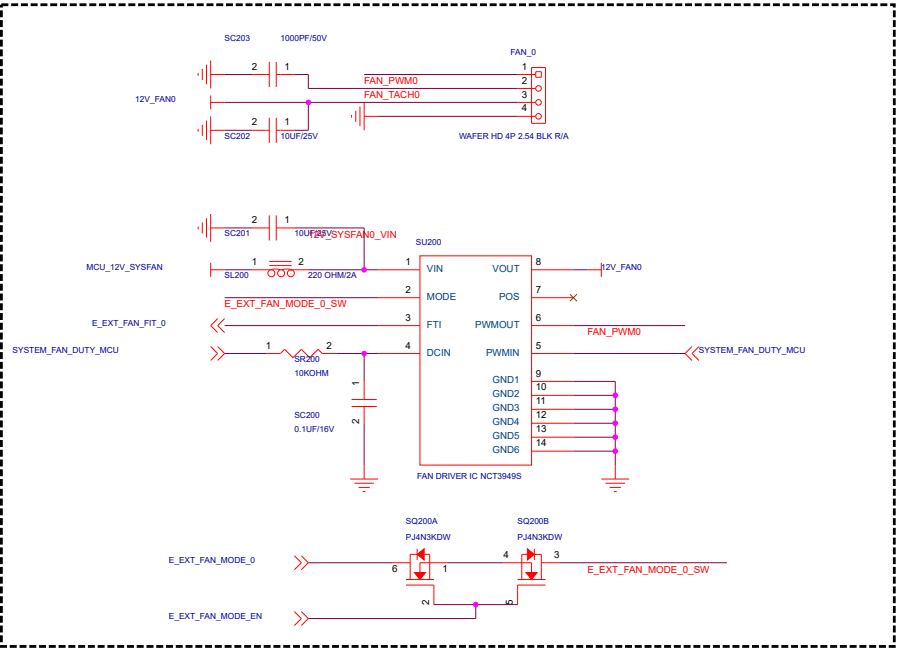
Fan Control II

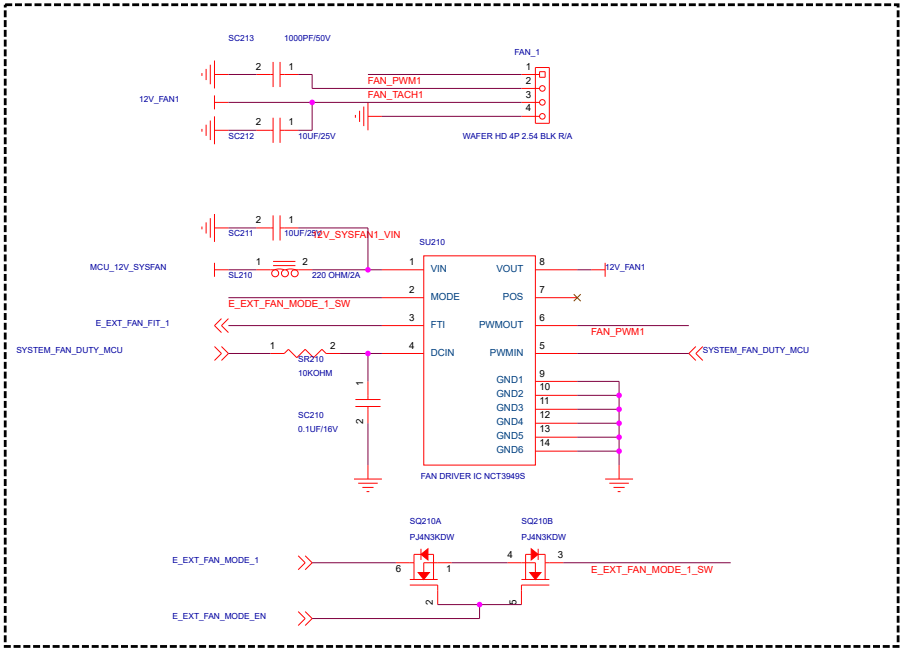


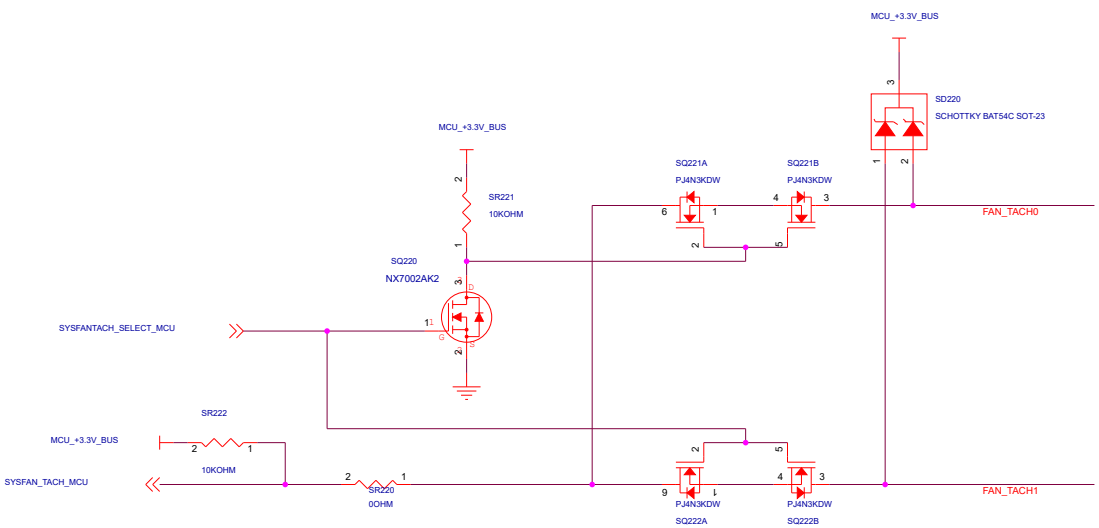


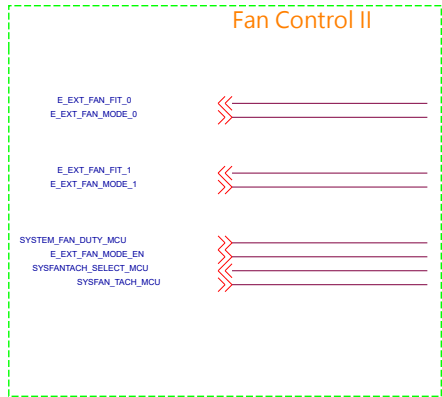
LED_ON/OFF請放置於BOT SIDE
相關位置請與ME/PM確認
須以上圖方式顯示明顯文字

S0002 SYSTEM FAN CONTROL

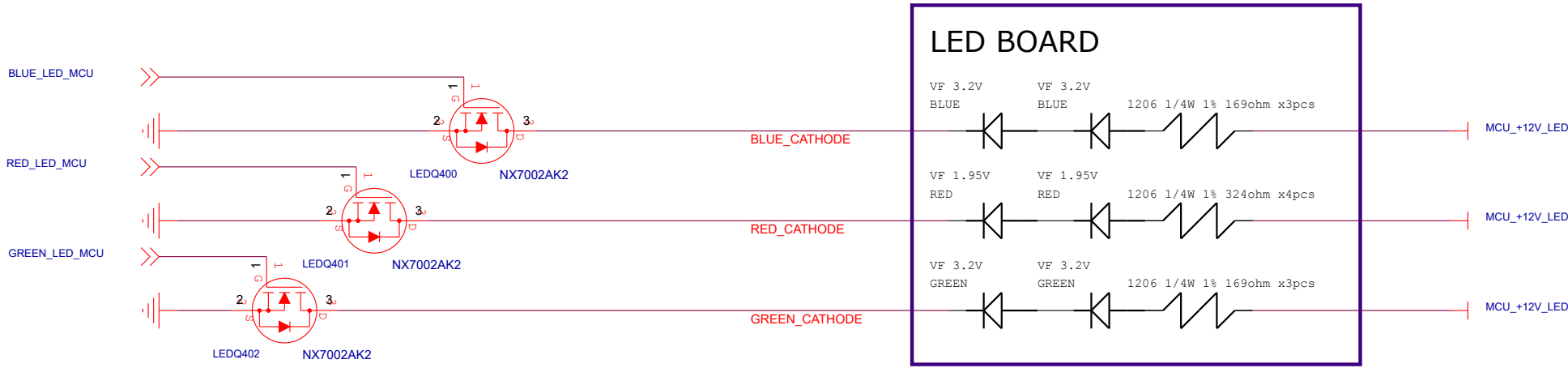


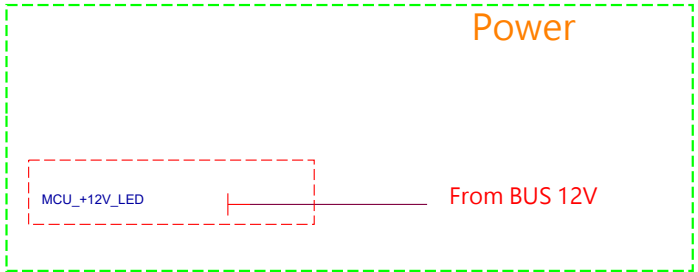


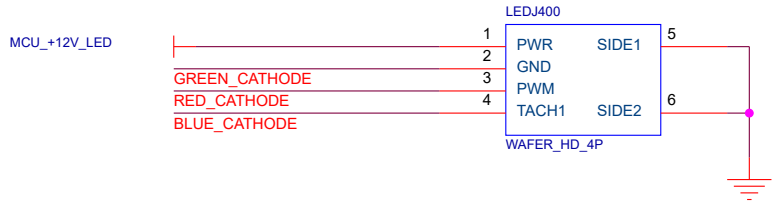




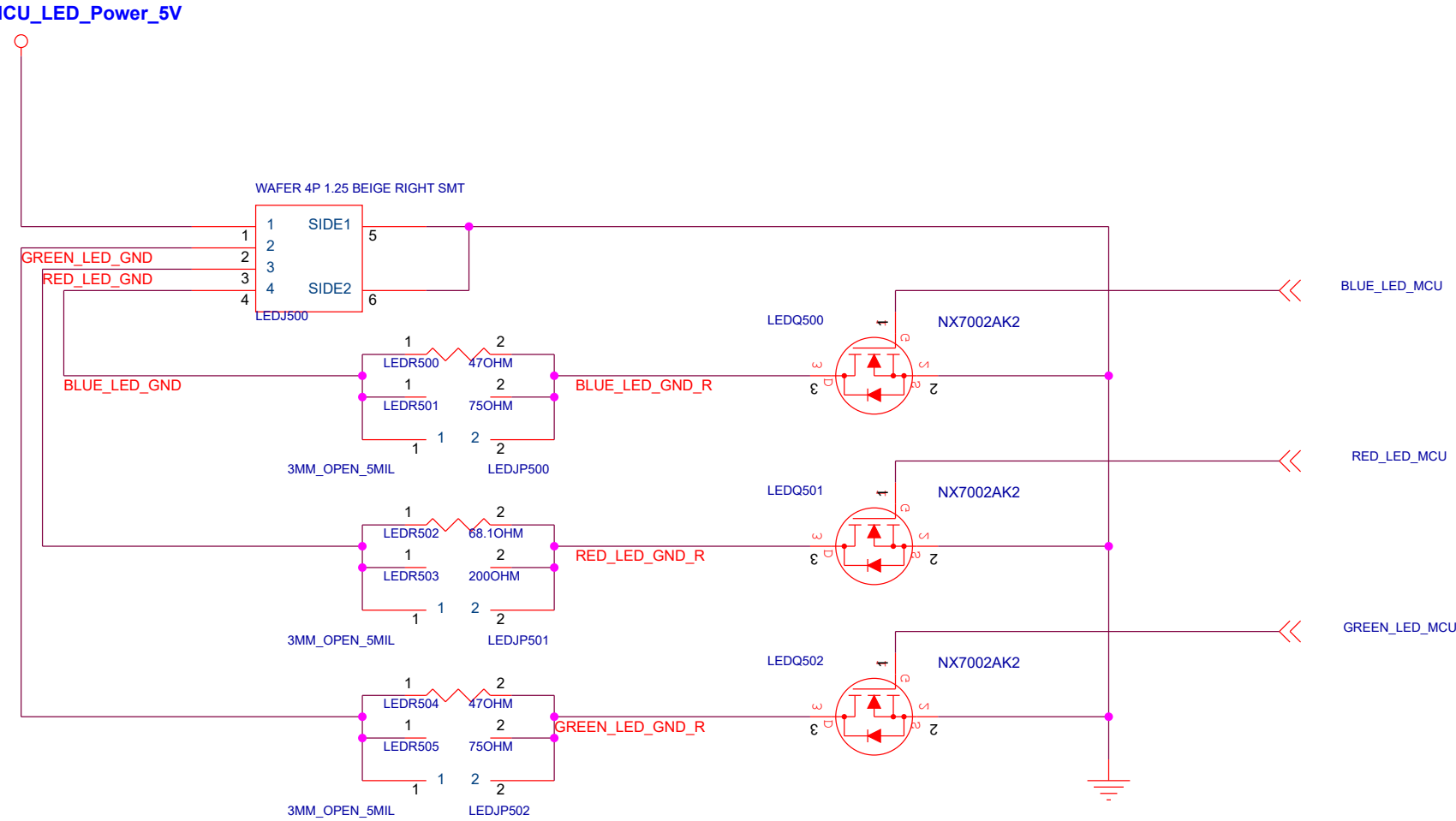
S0003 RGB LED







S0014 LIGHT BACK PLATE



Power

MCU_LED_Power_5V From S000

S0015 RGB HEADER

Power

MCU_+12V_LED

From BUS 12V

示意圖

連接座旁請註明 12V G R B

RGB Header

RGB_HEADER

+12V_efuse1

RGBHEADER_B

RGBHEADER_R

RGBHEADER_G

HEADER 1X4P G/F 2.54 RED R/A

RED_LED_MCU

RGBHEADER_R

LEDQ601

EMF30N02J

LEDC601

0.1UF/16V

/X/SB357x

BLUE_LED_MCU

RGBHEADER_B

LEDQ602

EMF30N02J

LEDC602

0.1UF/16V

/X/SB357x

GREEN_LED_MCU

RGBHEADER_G

LEDQ603

EMF30N02J

LEDC603

0.1UF/16V

/X/SB357x

eFuse

LEDU600

GND3 GND2 GND1 dV/dT ILIM EN/UVLO BFET VIN1 OUT3 VIN2 OUT2 VIN3 OUT1

OVP IC NCT3581Y-D

LEDC604

0.1UF/16V

/X/SB3572

MCU_+12V_LED

LEDR601

8.2KOHM

LEDR602

4.7KOHM

LEDC605

1000PF/16V

/X/SB3572

MCU_+12V_LED

/X/SB3572

LEDC606

1UF/16V

LEDT601

/X/SB3572

LEDJP600

SOLDER PASTE

+12V_efuse1

LEDC607

10UF/16V

LEDR603

82.5KOHM

限流=2A, (R*3)/10^5 = I-0.7