P1041-B01 GF104

GF104-300, 768MB/1536MB, GDDR5 192b 32M/64Mx32
DVI-I-DL, DVI-I-DL/DP, mHDMI

Table of Contents:

Page 1: Title
Page 2: Block Diagram
Page 3: PCI Express
Page 4: GPU Partition A/B
Page 5: FBA Partition 31..0
Page 6: FBA Partition 63..32
Page 7: FBB Partition 31..0
Page 8: FBB Partition 63..32
Page 9: GPU Partition C/D
Page 10: FBC Partition 31..0
Page 11: FBC Partition 63..32
Page 12: FBD Partition 31..0
Page 13: FBD Partition 63..32
Page 14: FB Net Properties(delete)
Page 15: GPU PWR and GND
Page 16: GPU Decoupling
Page 17: Blank
Page 18: DACA (South)
Page 19: DACB (Mid)
Page 20: IFPAB DVI-DL (South)
Page 21: IFPEF DVI-DL (Mid)
Page 22: IFPEF DP (Mid)
Page 23: IFPC mHDMI (North)
Page 24: Multi-use IO (MIO) Interface
Page 25: Misc: Fan, Thermal, JTAG, GPIO
Page 26: Misc: ROM, HDCP, XTAL, Straps
Page 27: PS: 5V, PEX_VDD
Page 28: PS: FBVDD/Q
Page 29: PS: NVVDD Controller
Page 30: PS: NVVDD Phase 1-2
Page 31: PS: NVVDD Phase 3-4
Page 32: PS: Inputs, Shutdown, IFP
Page 33: Mechanical: Bracket/Thermal Solution
Page 34: Blank

變更記錄

P3，C55 change to 1206 10u
P4~P14，add 跳頁&'<>'符號
P14,刪除所有網絡線
P17，add 6262 IC
P25,刪除原公版U2 & J501. 把I2CC接到6262IC
P27,接PS1_1V05_FB到6262,U4 foot_print 改爲十字的
P28,改U8的FB接法，換L6爲L04-22A8011-L65
P29，core部份PWM換UP6213+6284，OFS電壓開關抬50mV。頻率def400KHz，開關抬到600KHz.
P30-31，加driver IC 6284；去掉3顆input 電容；同時增加6個LED燈，增加CP1~CP12；爲精簡線路，刪除L mos端與DRVL 0OHm電阻，刪除CSP，CSN 0Ω電阻；更換MOS & 電感；power前4相由PEX6_F1提供，后2相由PEX6_F2提供；電容部份保留公版。
P32,去除input 端12V 的LB電感
P33,加防彎條mec100，加6個十字光學點，加NVVDD，FBVDD &pex_vdd的測試點, 增加阻抗條

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SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11041-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-11041-0000-300	P1041 GF104-300 768MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
2	SKU0010	600-11041-0010-300	P1041 GF104-350 1024MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
3	QS1	600-11041-0000-QS1	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
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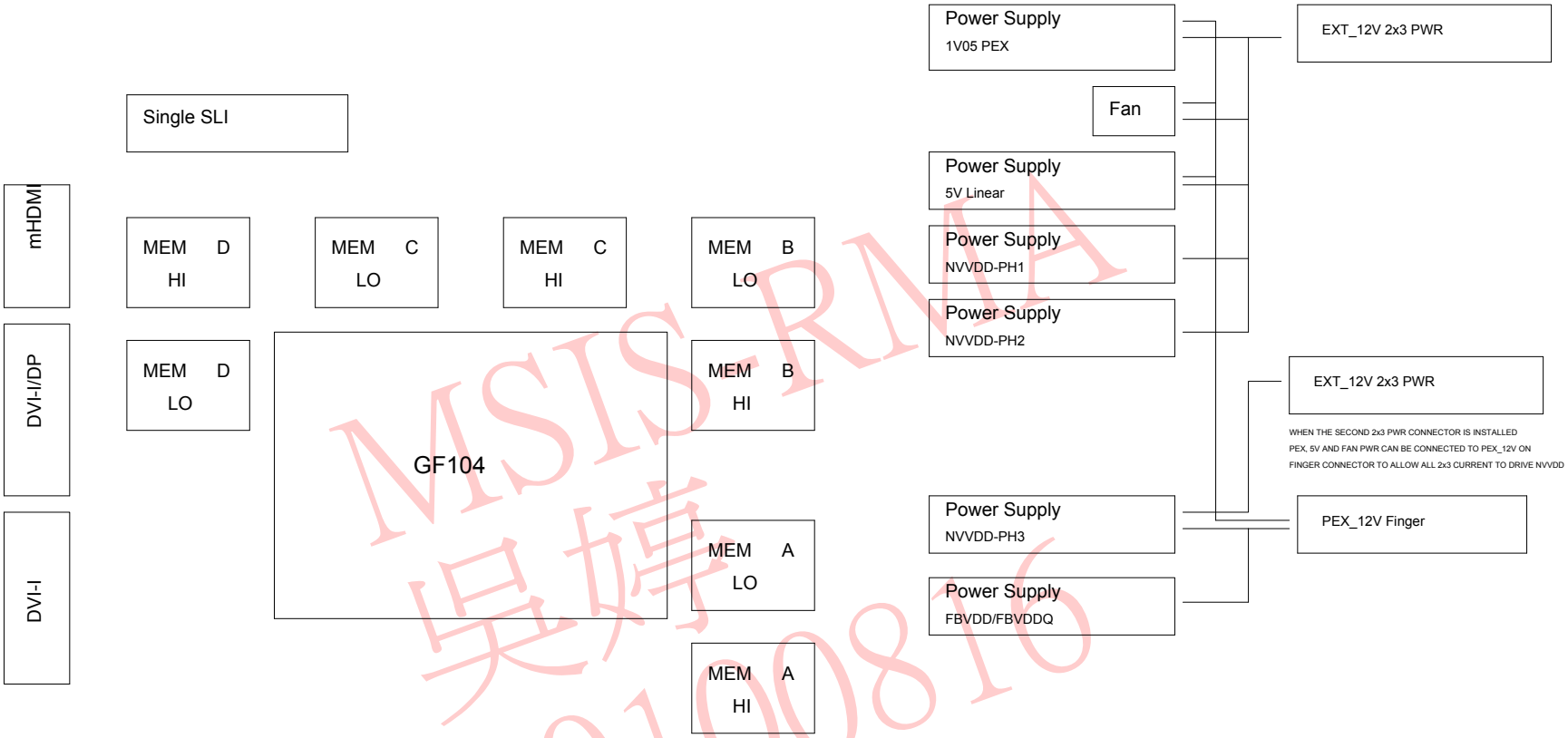
Page2: Block Diagram



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PAGE DETAIL	Block Diagram

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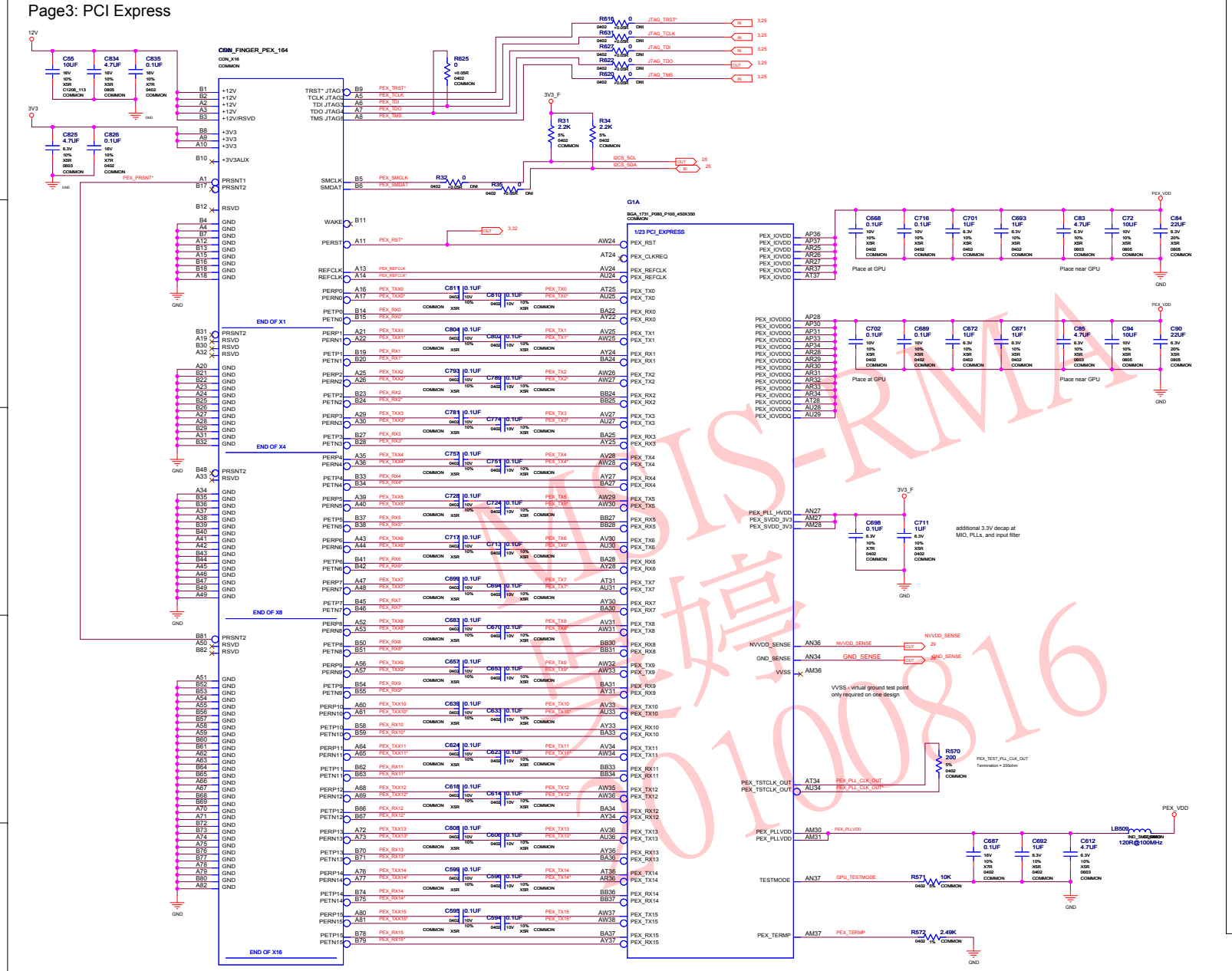
Page3: PCI Express



PEX NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	24MIL
3V3	3.3V	3.0A	20MIL
GND	0V	8.5A	16MIL

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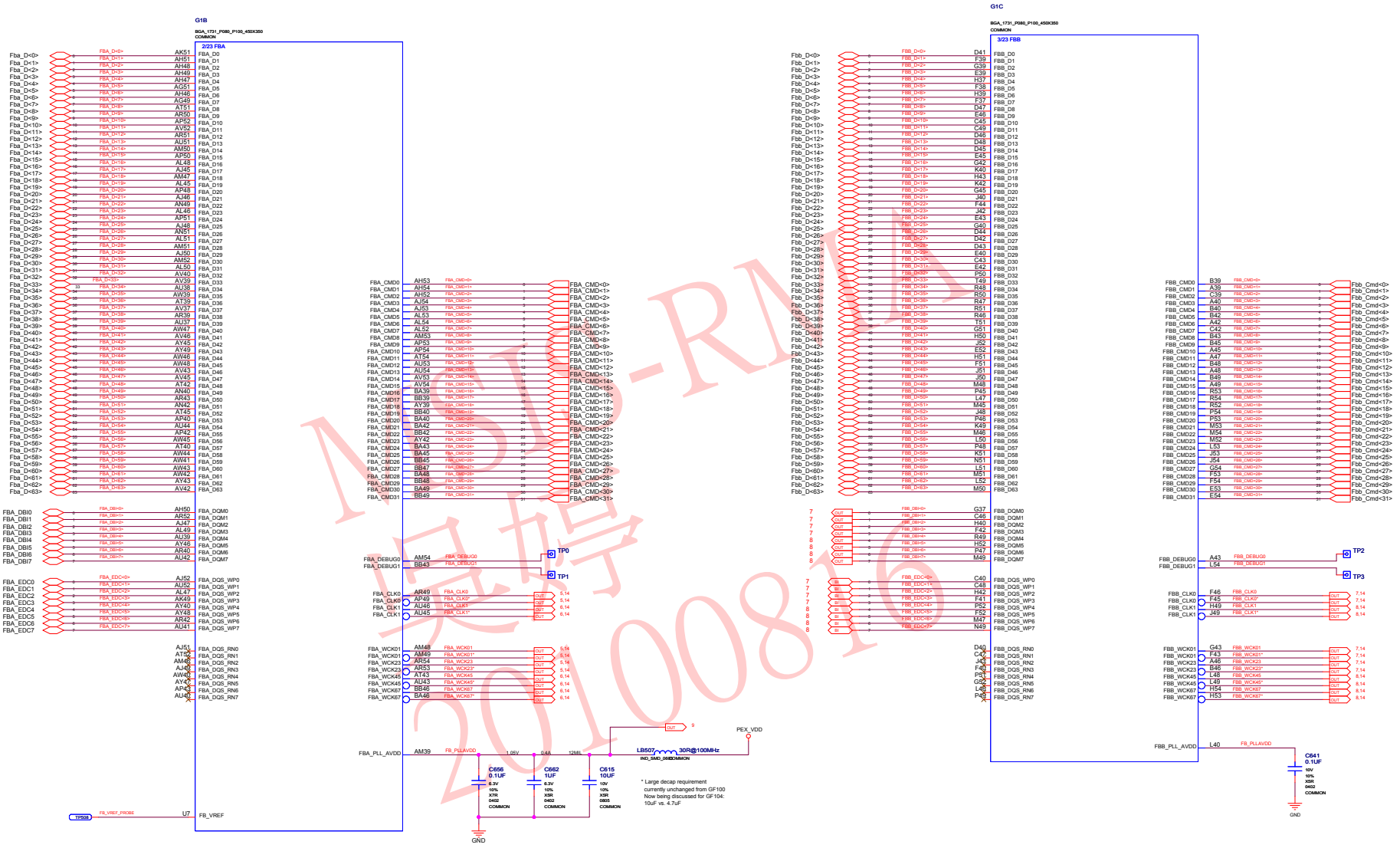
Page4: GPU Partition A/B



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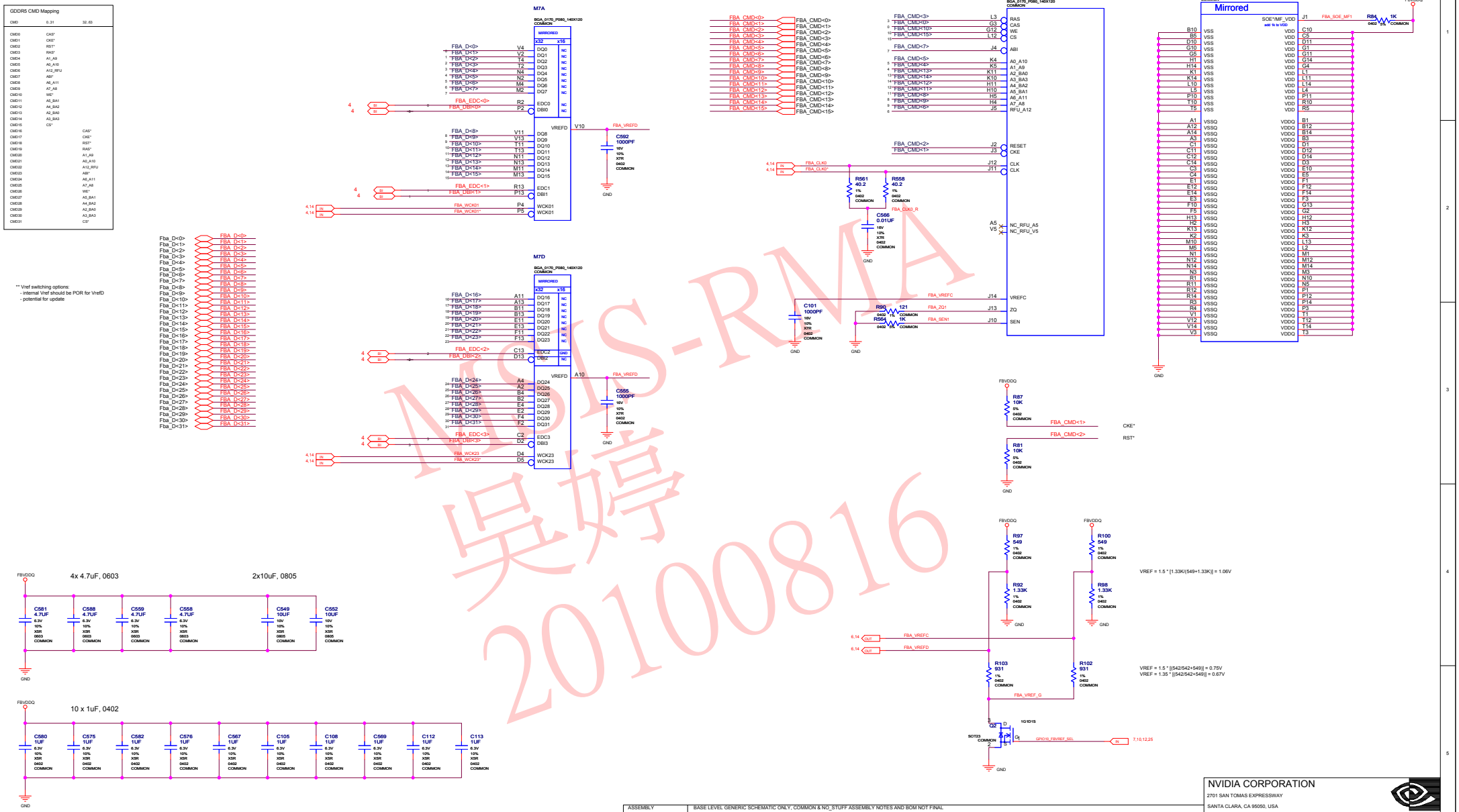
Page5: FBA Partition 31..0



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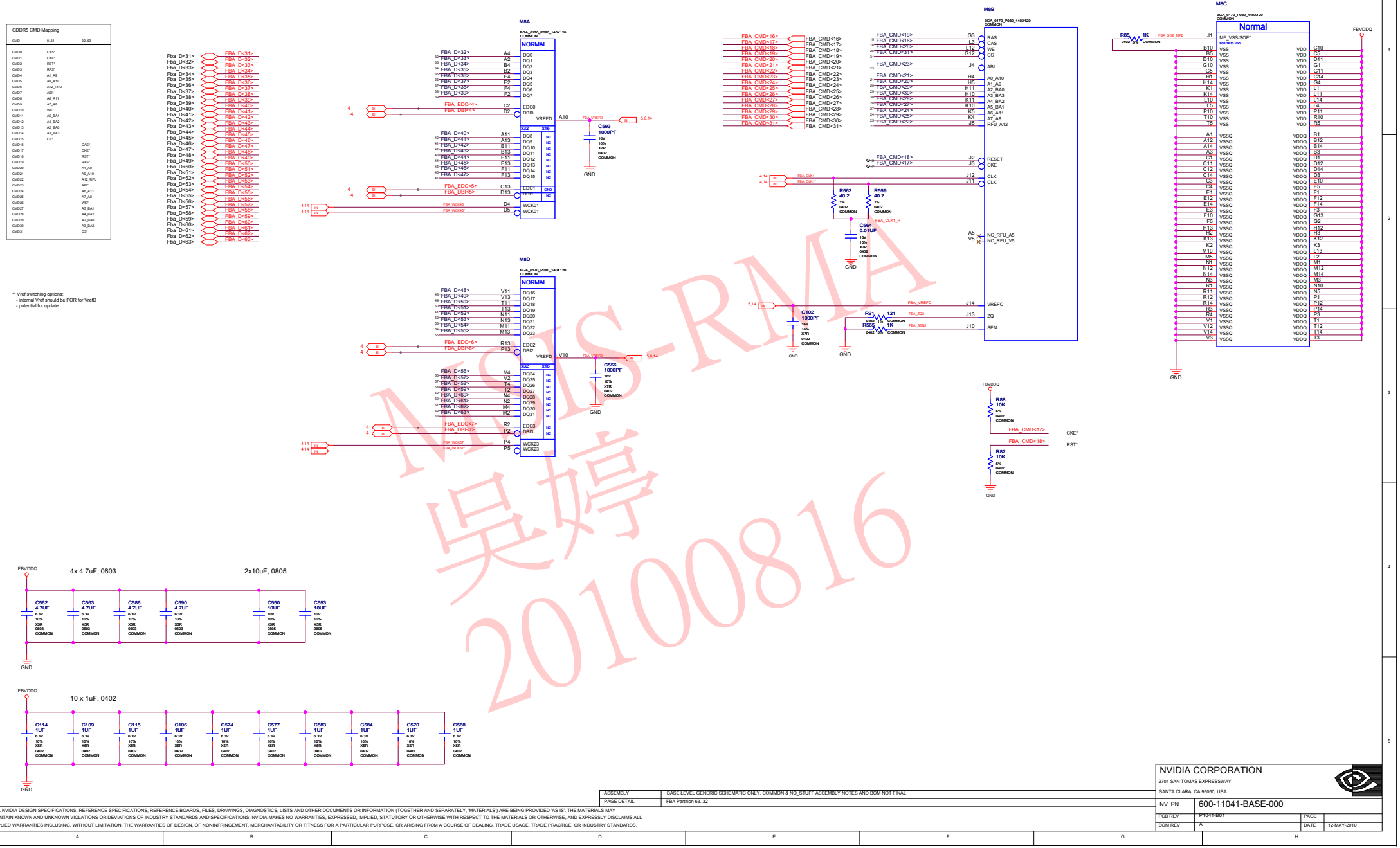
Page6: FBA Partition 63..32



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PAGE DETAIL	FBA Partition 63..32

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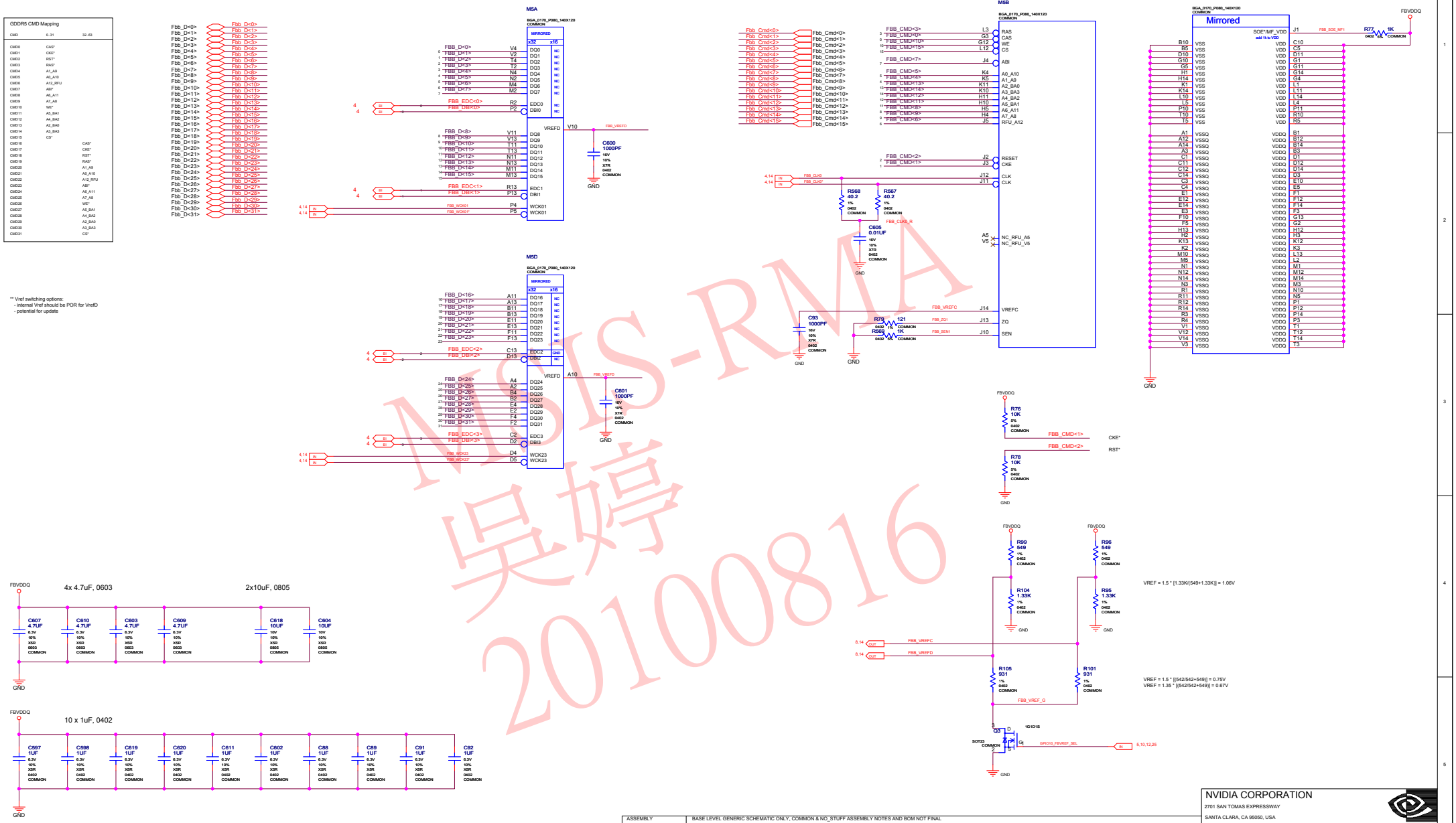
Page7: FBB Partition 31..0



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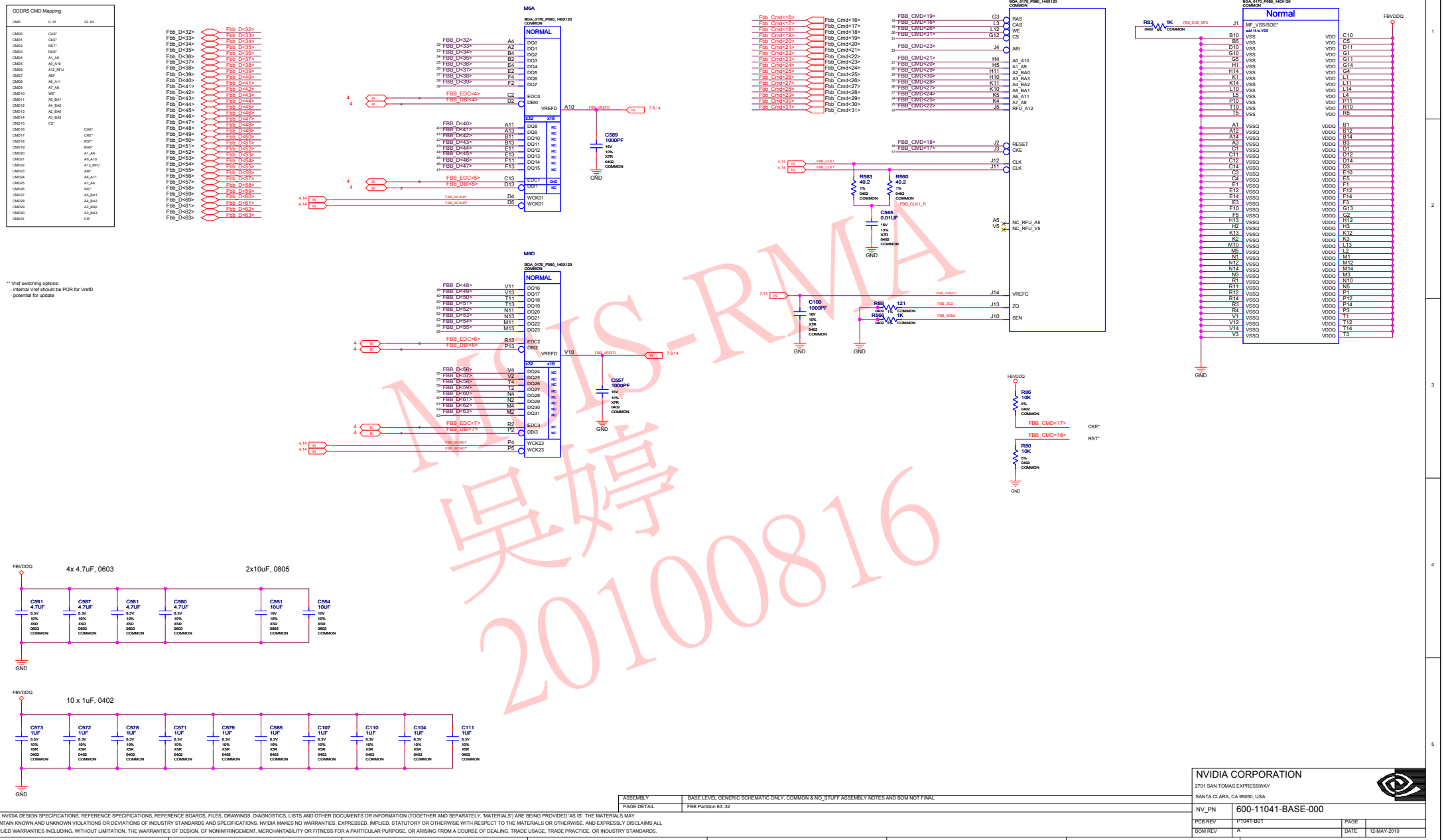
Page8: FBB Partition 63..32



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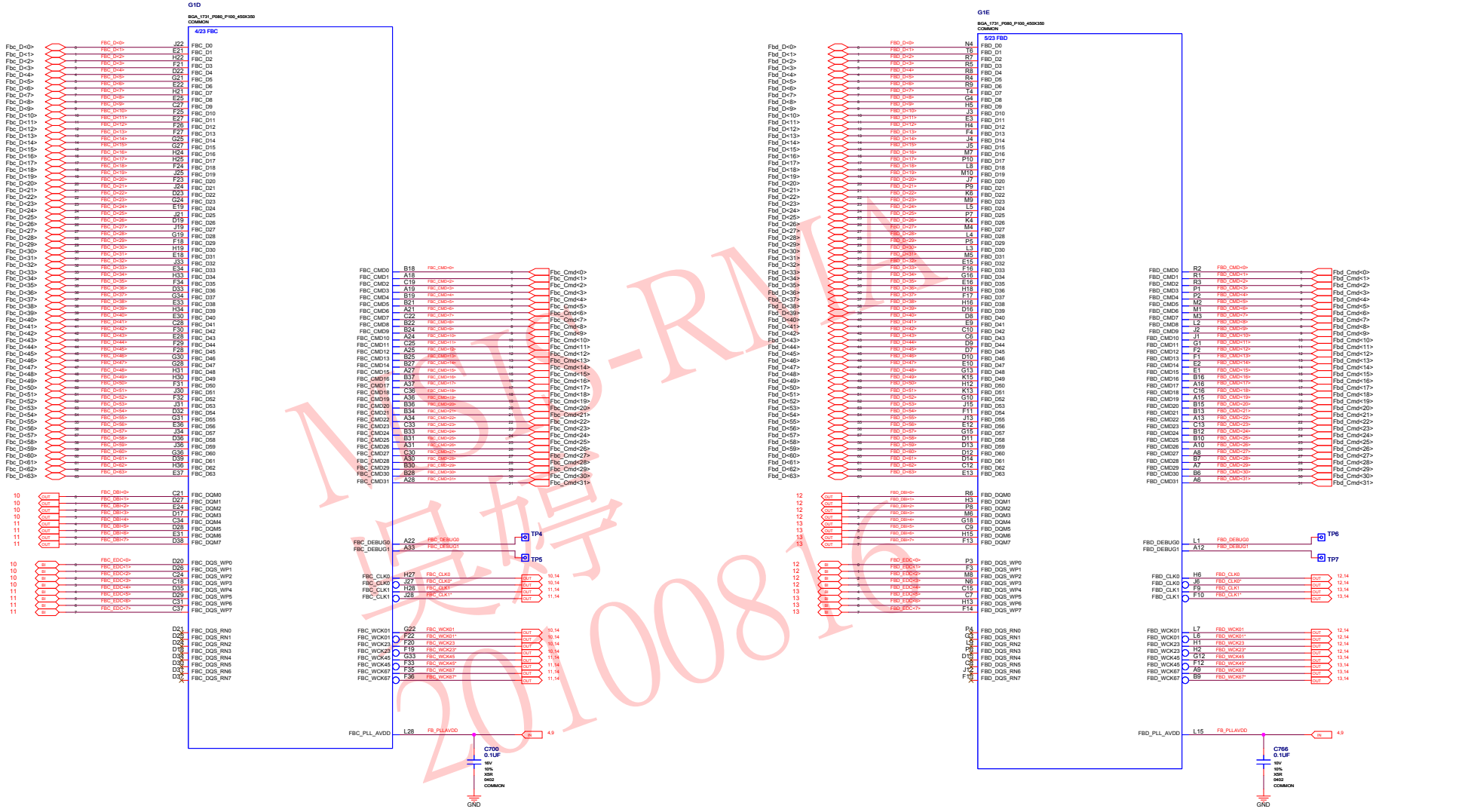
Page9: GPU Partition C/D



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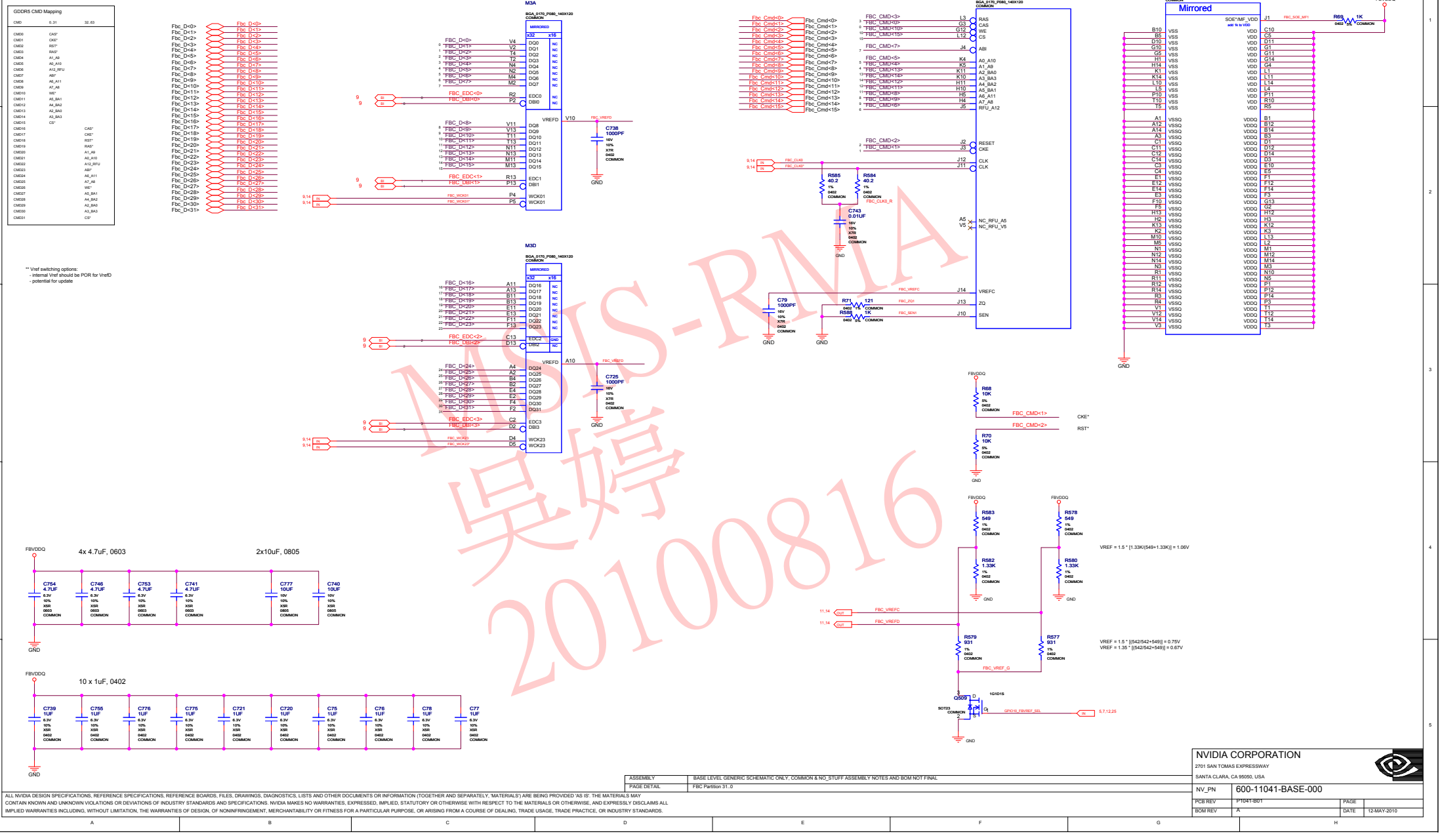
Page10: FBC Partition 31..0



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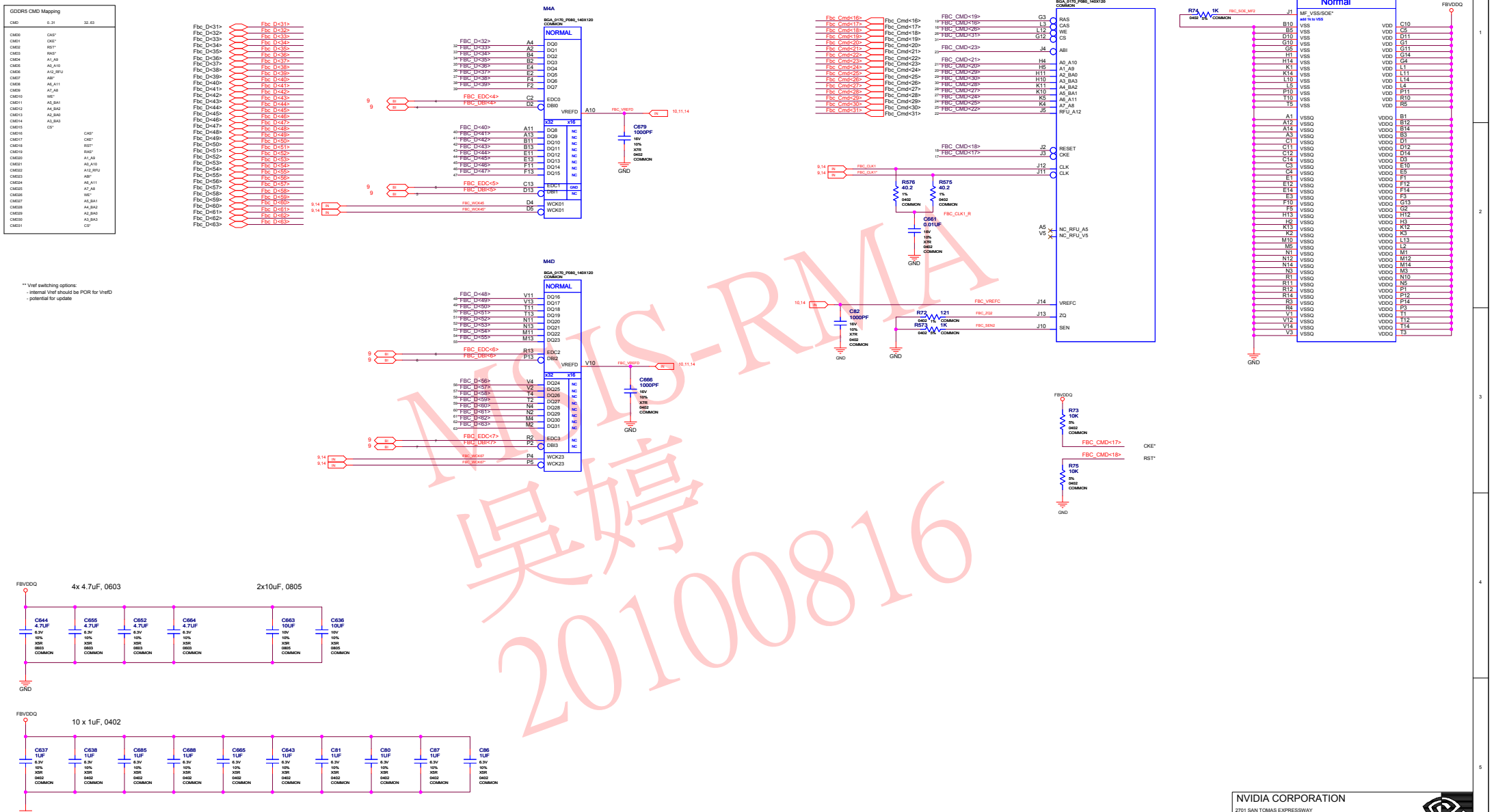
Page11: FBC Partition 63..32



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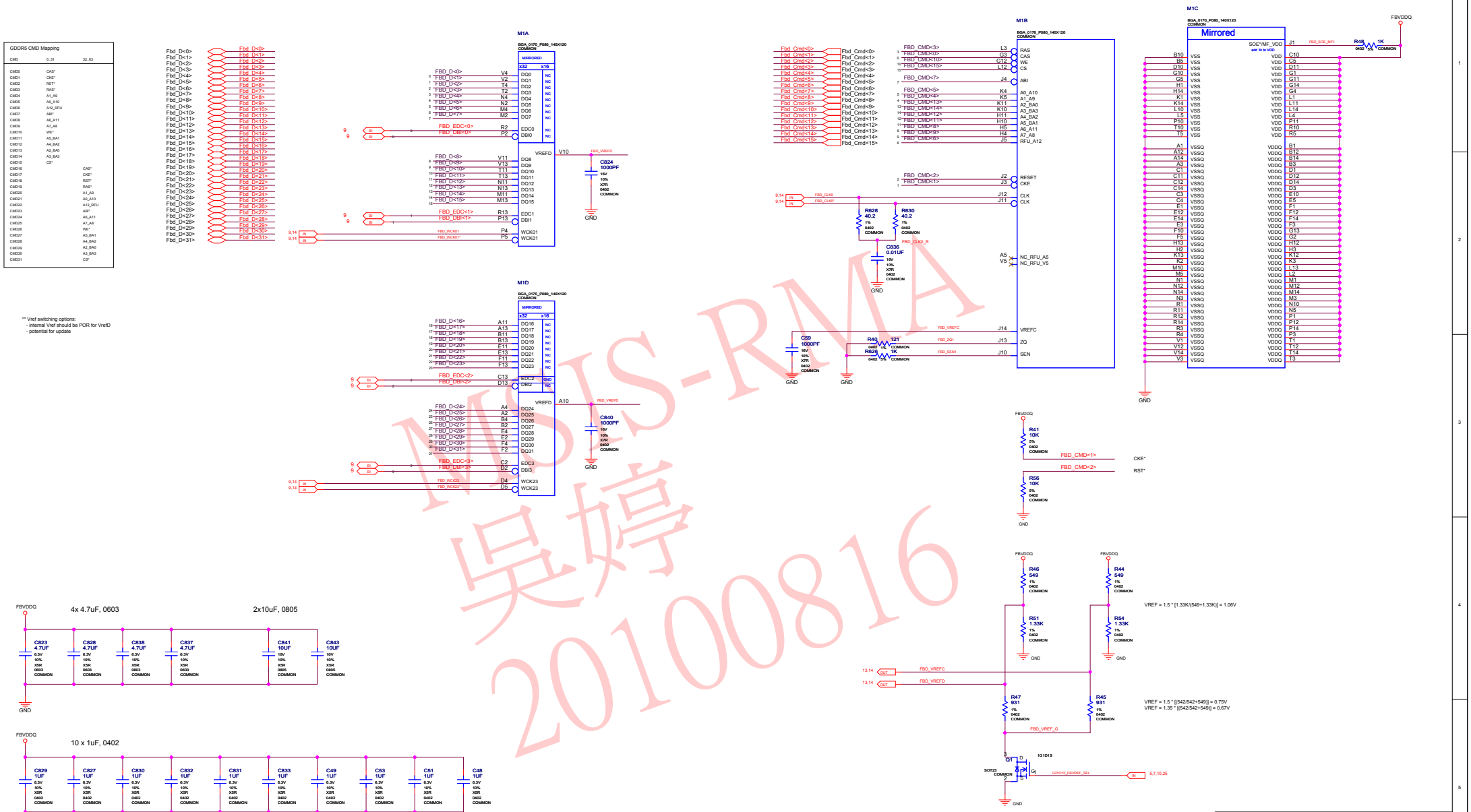
Page12: FBD Partition 31..0



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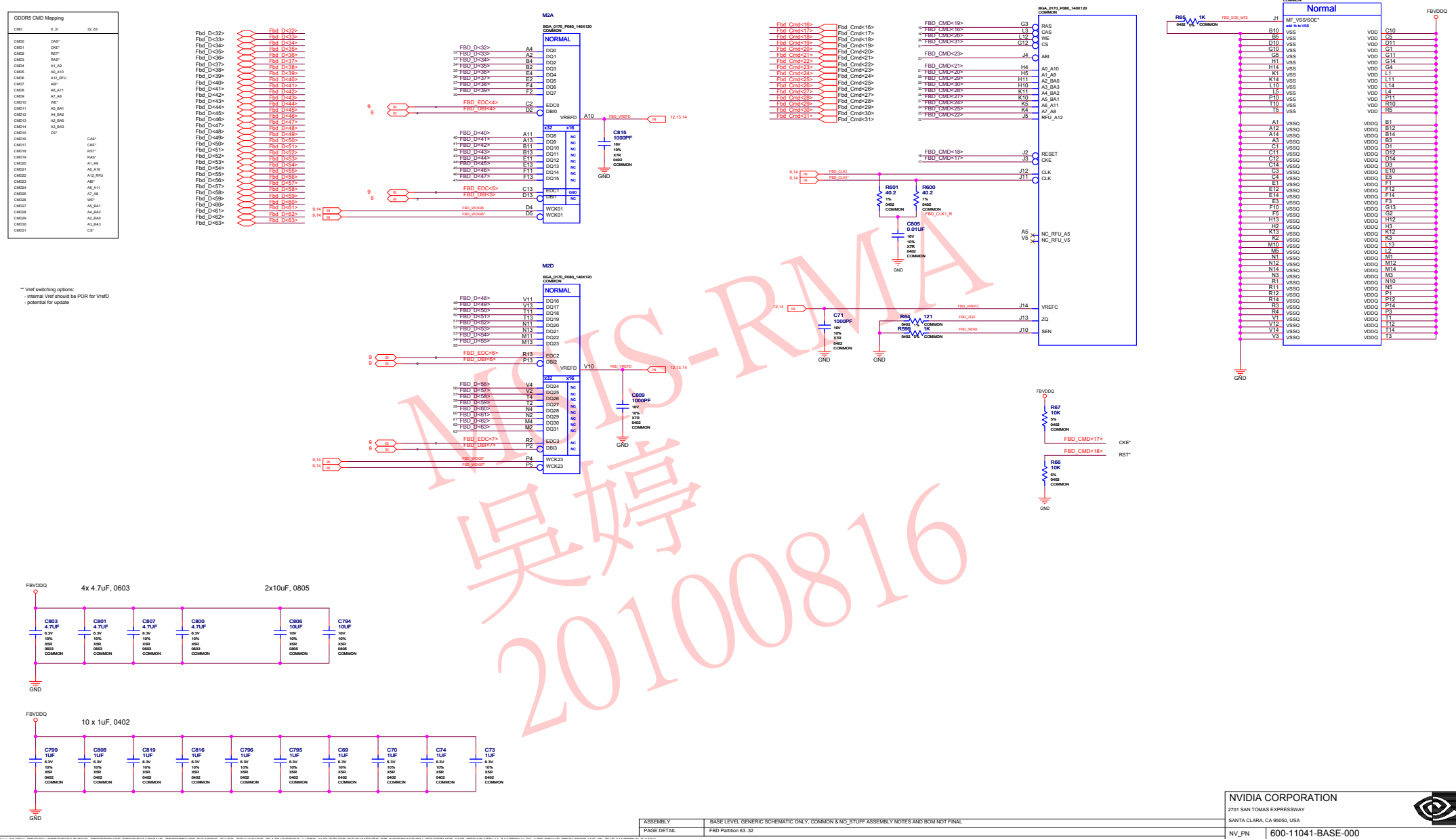
Page13: FBD Partition 63..32



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Page14: FB Net Properties

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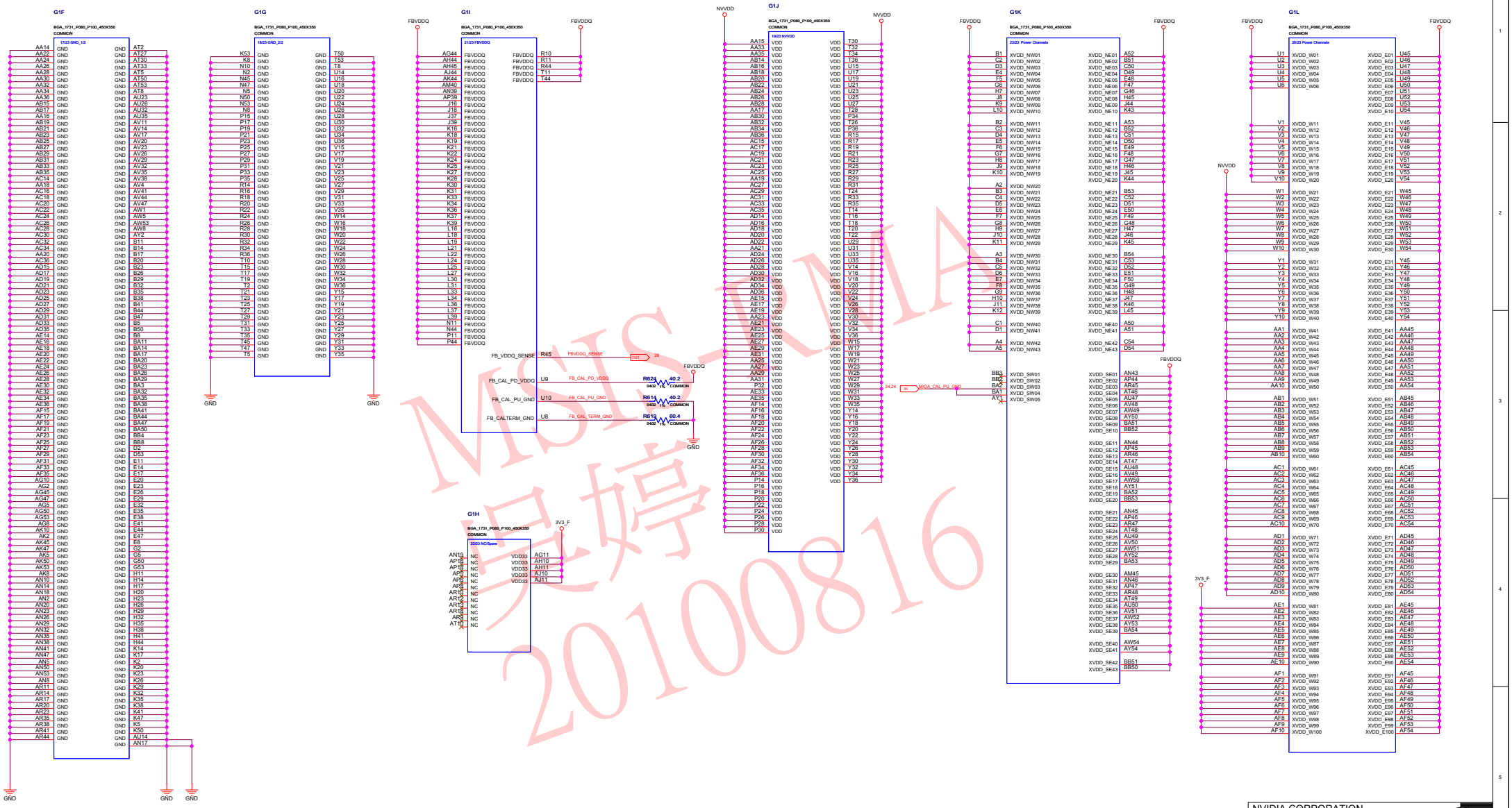
Page15: GPU PWR and GND

** Power channels are configurable.

XVDD_* pins are not connected on the substrate.

Therefore, XVDD_* pins can be assigned as needed.



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PAGE DETAIL	GPU PWR and GND

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BOM REV	A	DATE	12-MAY-2010

Page16: GPU Decoupling

FBVDDQ

FBVDDQ

Partition A

C629 0.1UF 16V 10% X5R 0402 COMMON
C640 0.47UF 6.3V 10% X5R 0402 COMMON
C632 1UF 6.3V 10% X5R 0402 COMMON
C625 1UF 6.3V 10% X5R 0402 COMMON
GND

1x 100nF, 470nF, 2x 1uF, 0402

Partition B

C654 0.1UF 16V 10% X5R 0402 COMMON
C667 0.47UF 6.3V 10% X5R 0402 COMMON
C628 1UF 6.3V 10% X5R 0402 COMMON
C626 1UF 6.3V 10% X5R 0402 COMMON
GND

1x 100nF, 470nF, 2x 1uF, 0402

Partition C

C722 0.1UF 16V 10% X5R 0402 COMMON
C696 0.47UF 6.3V 10% X5R 0402 COMMON
C712 1UF 6.3V 10% X5R 0402 COMMON
C684 1UF 6.3V 10% X5R 0402 COMMON
GND

1x 100nF, 470nF, 2x 1uF, 0402

Partition D

C748 0.1UF 16V 10% X5R 0402 COMMON
C737 0.47UF 6.3V 10% X5R 0402 COMMON
C784 1UF 6.3V 10% X5R 0402 COMMON
C785 1UF 6.3V 10% X5R 0402 COMMON
GND

1x 100nF, 470nF, 2x 1uF, 0402

8x 4.7uF, 0603 (Place Near GPU)

C627 4.7UF 6.3V 20% X5R 0603 COMMON
C779 4.7UF 6.3V 20% X5R 0603 COMMON
C634 4.7UF 6.3V 20% X5R 0603 COMMON
C630 4.7UF 6.3V 20% X5R 0603 COMMON
C67 4.7UF 6.3V 20% X5R 0603 COMMON
C631 4.7UF 6.3V 20% X5R 0603 COMMON
C63 4.7UF 6.3V 20% X5R 0603 COMMON
C96 4.7UF 6.3V 20% X5R 0603 COMMON
GND

4x 10uF, 0805 (Place Near GPU)

C66 10UF 6.3V 20% X5R 0805 COMMON
C116 10UF 6.3V 20% X5R 0805 COMMON
C118 10UF 6.3V 20% X5R 0805 COMMON
C42 10UF 6.3V 20% X5R 0805 COMMON
GND

4x 22uF, 0805 (Place Near GPU)

C119 22UF 6.3V 20% X5R 0805 COMMON
C43 22UF 6.3V 20% X5R 0805 COMMON
C52 22UF 6.3V 20% X5R 0805 COMMON
C117 22UF 6.3V 20% X5R 0805 COMMON
GND

VDD33

3V3_F

C790 4.7UF 10% X5R 0603 COMMON
C813 1UF 10% X5R 0402 COMMON
C814 0.1UF 10V 10% X5R 0402 COMMON
GND

* additional VDD33 decap at MIO, PLLs, and input filter

NVVDD

NVVDD

C759 0.047UF 16V 10% X7R 0402 COMMON
C651 0.047UF 16V 10% X7R 0402 COMMON
C765 0.047UF 16V 10% X7R 0402 COMMON
C645 0.047UF 16V 10% X7R 0402 COMMON
C736 0.047UF 16V 10% X7R 0402 COMMON
C673 0.047UF 16V 10% X7R 0402 COMMON
C729 0.047UF 16V 10% X7R 0402 COMMON
C709 0.047UF 16V 10% X7R 0402 COMMON
C681 0.047UF 16V 10% X7R 0402 COMMON
GND

9x 47nF, 0402

C761 0.1UF 16V 10% X5R 0402 COMMON
C762 0.1UF 16V 10% X5R 0402 COMMON
C647 0.1UF 16V 10% X5R 0402 COMMON
C648 0.1UF 16V 10% X5R 0402 COMMON
C708 0.1UF 16V 10% X5R 0402 COMMON
C676 0.1UF 16V 10% X5R 0402 COMMON
C732 0.1UF 16V 10% X5R 0402 COMMON
C710 0.1UF 16V 10% X5R 0402 COMMON
C706 0.1UF 16V 10% X5R 0402 COMMON
GND

9x 100nF, 0402

C755 0.22UF 6.3V 10% X5R 0402 COMMON
C754 0.22UF 6.3V 10% X5R 0402 COMMON
C674 0.22UF 6.3V 10% X5R 0402 COMMON
C660 0.22UF 6.3V 10% X5R 0402 COMMON
C703 0.22UF 6.3V 10% X5R 0402 COMMON
C735 0.22UF 6.3V 10% X5R 0402 COMMON
C730 0.22UF 6.3V 10% X5R 0402 COMMON
C707 0.22UF 6.3V 10% X5R 0402 COMMON
C690 0.22UF 6.3V 10% X5R 0402 COMMON
GND

9x 220nF, 0402

C763 1UF 6.3V 10% X5R 0402 COMMON
C649 1UF 6.3V 10% X5R 0402 COMMON
C760 1UF 6.3V 10% X5R 0402 COMMON
C734 1UF 6.3V 10% X5R 0402 COMMON
C731 1UF 6.3V 10% X5R 0402 COMMON
C704 1UF 6.3V 10% X5R 0402 COMMON
C646 1UF 6.3V 10% X5R 0402 COMMON
C678 1UF 6.3V 10% X5R 0402 COMMON
C675 1UF 6.3V 10% X5R 0402 COMMON
GND

9x 1uF, 0402

C642 4.7UF 6.3V 20% X5R 0603 COMMON
C677 4.7UF 6.3V 20% X5R 0603 COMMON
C733 4.7UF 6.3V 20% X5R 0603 COMMON
C768 4.7UF 6.3V 20% X5R 0603 COMMON
C622 4.7UF 6.3V 20% X5R 0603 COMMON
C791 4.7UF 6.3V 20% X5R 0603 COMMON
GND

6x 4.7uF, 0603

C744 10UF 6.3V 20% X5R 0805 COMMON
C745 10UF 6.3V 20% X5R 0805 COMMON
C659 10UF 6.3V 20% X5R 0805 COMMON
C660 10UF 6.3V 20% X5R 0805 COMMON
GND

4x 10uF, 0805

C749 22UF 6.3V 20% X5R 0805 COMMON
C715 22UF 6.3V 20% X5R 0805 COMMON
C697 22UF 6.3V 20% X5R 0805 COMMON
C658 22UF 6.3V 20% X5R 0805 COMMON
C718 22UF 6.3V 20% X5R 0805 COMMON
C690 22UF 6.3V 20% X5R 0805 COMMON
C719 22UF 6.3V 20% X5R 0805 COMMON
C691 22UF 6.3V 20% X5R 0805 COMMON
C635 22UF 6.3V 20% X5R 0805 COMMON
C780 22UF 6.3V 20% X5R 0805 COMMON
GND

10x 22uF, 0805

NVVDD

C877 470UF COMMON 20% 2V POSCAP 3A@105C 0.005R CAP_SMD_7343
C876 470UF DNI 20% 2V POSCAP 3A@105C 0.005R CAP_SMD_7343
C880 470UF COMMON 20% 2V POSCAP 3A@105C 0.005R CAP_SMD_7343
C879 470UF COMMON 20% 2V POSCAP 3A@105C 0.005R CAP_SMD_7343
C878 470UF DNI 20% 2V POSCAP 3A@105C 0.005R CAP_SMD_7343
GND

5x 470uF, 7342

NVVDD

C881 220UF COMMON +/-20% 2.5V POSCAP 1A@45C, 100 TO 500 KHZ 0.075 OHM CAP_SMD_3528
GND

2x 220uF, 3528

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PAGE DETAIL	GPU Decoupling

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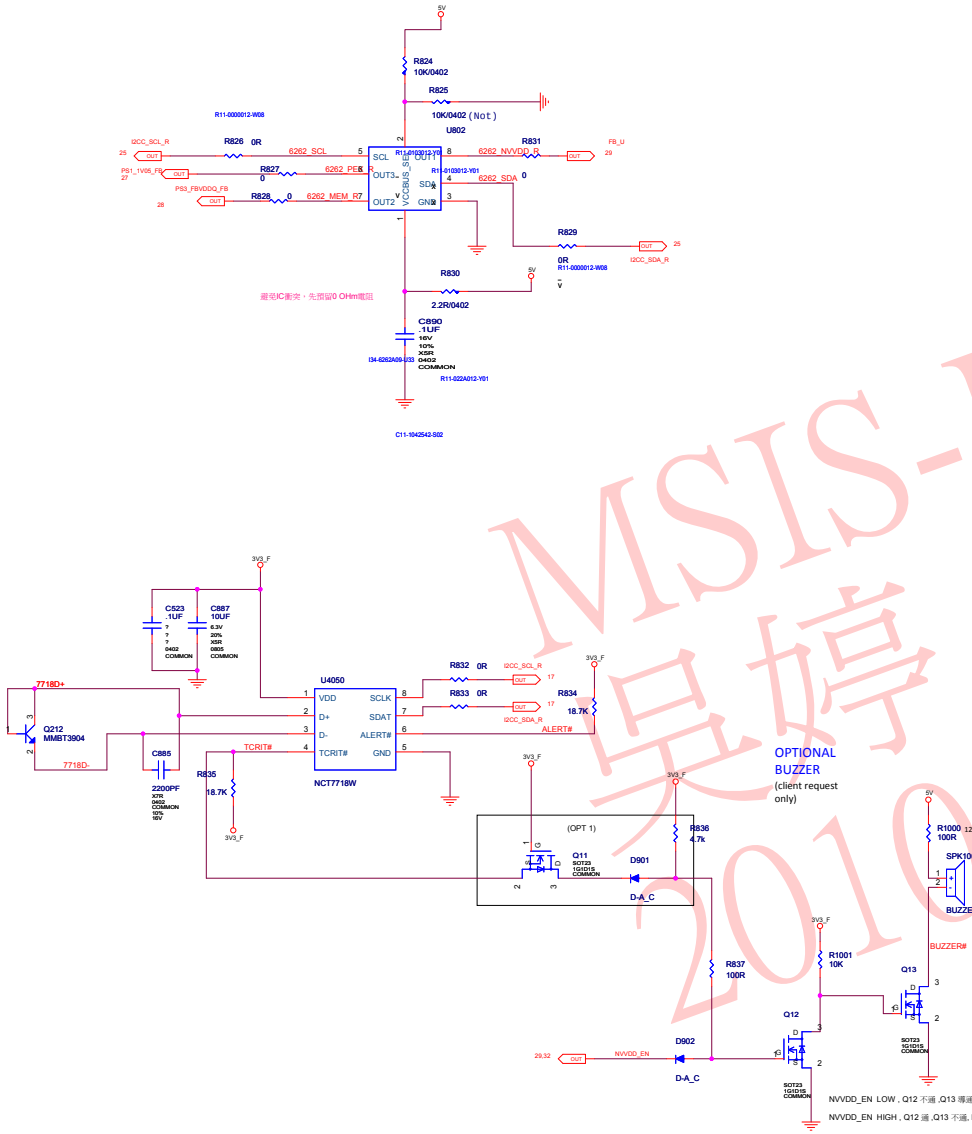
BOM REV	A	DATE	12-MAY-2010



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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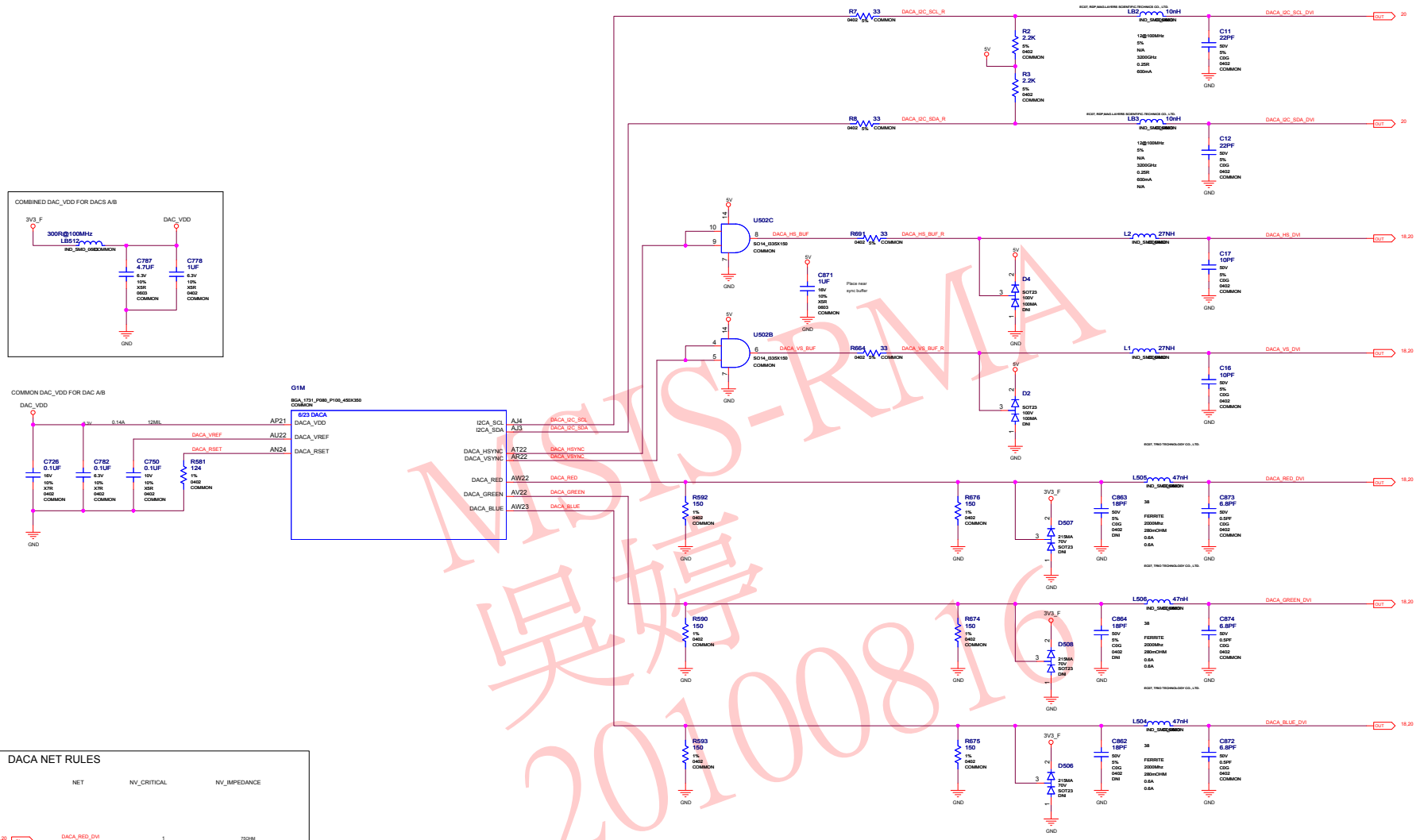
PCB REV	P1041-B01	PAGE	
BOM REV	A	DATE	12-MAY-2010

Page18: DACA (South)



DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE
DACA_RED_DVI	1	75OHM
DACA_GREEN_DVI	1	75OHM
DACA_BLUE_DVI	1	75OHM
DACA_HS_DVI	2	50OHM
DACA_VS_DVI	2	50OHM

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PAGE DETAIL	DACA (South)

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BOM REV	A	DATE	12-MAY-2010

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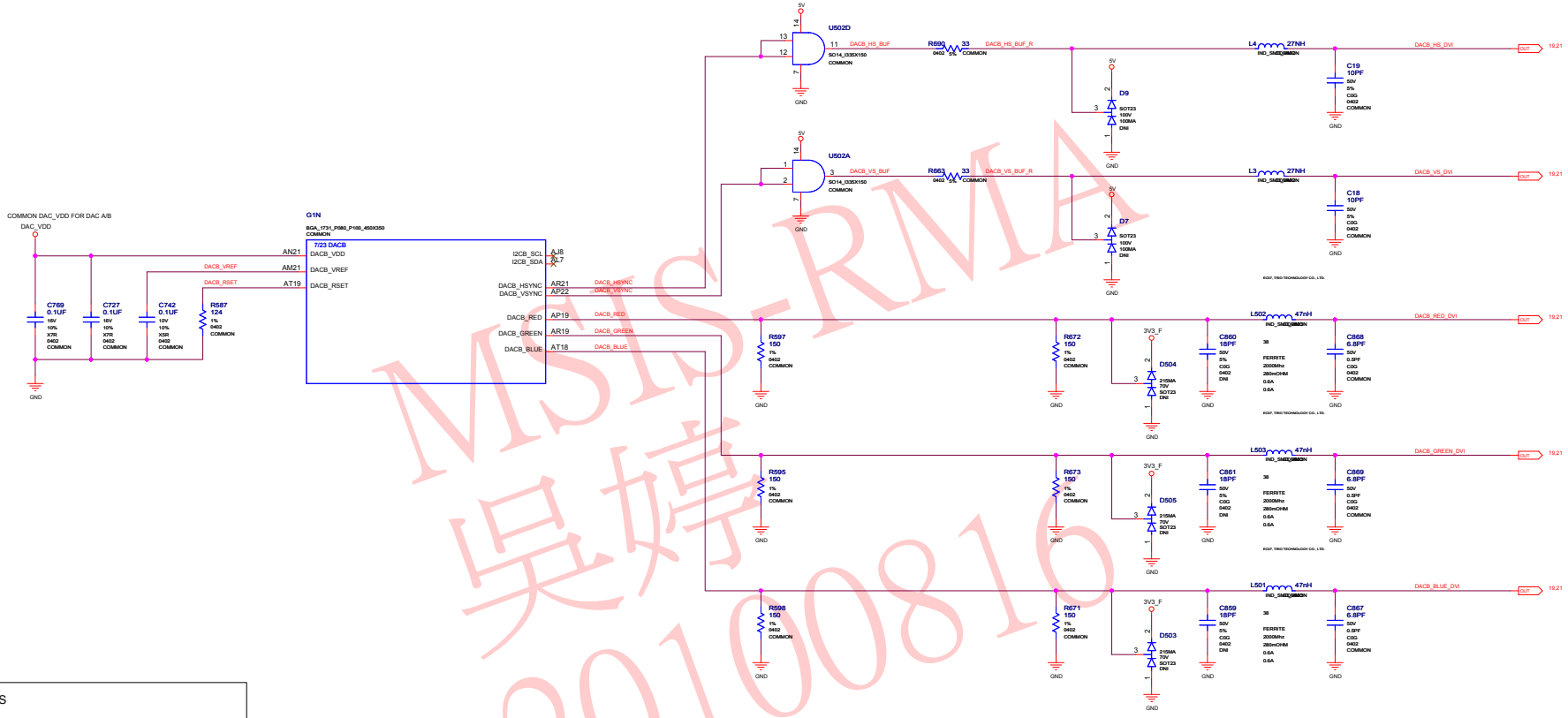
Page19: DACB (Mid)



DACB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE
DACB_RED_DVI	1	75OHM
DACB_GREEN_DVI	1	75OHM
DACB_BLUE_DVI	1	75OHM
DACB_HS_DVI	2	50OHM
DACB_VS_DVI	2	50OHM

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PAGE DETAIL	DACB (Mid)

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PCB REV	P1041-B01	PAGE	
BOM REV	A	DATE	12-MAY-2010

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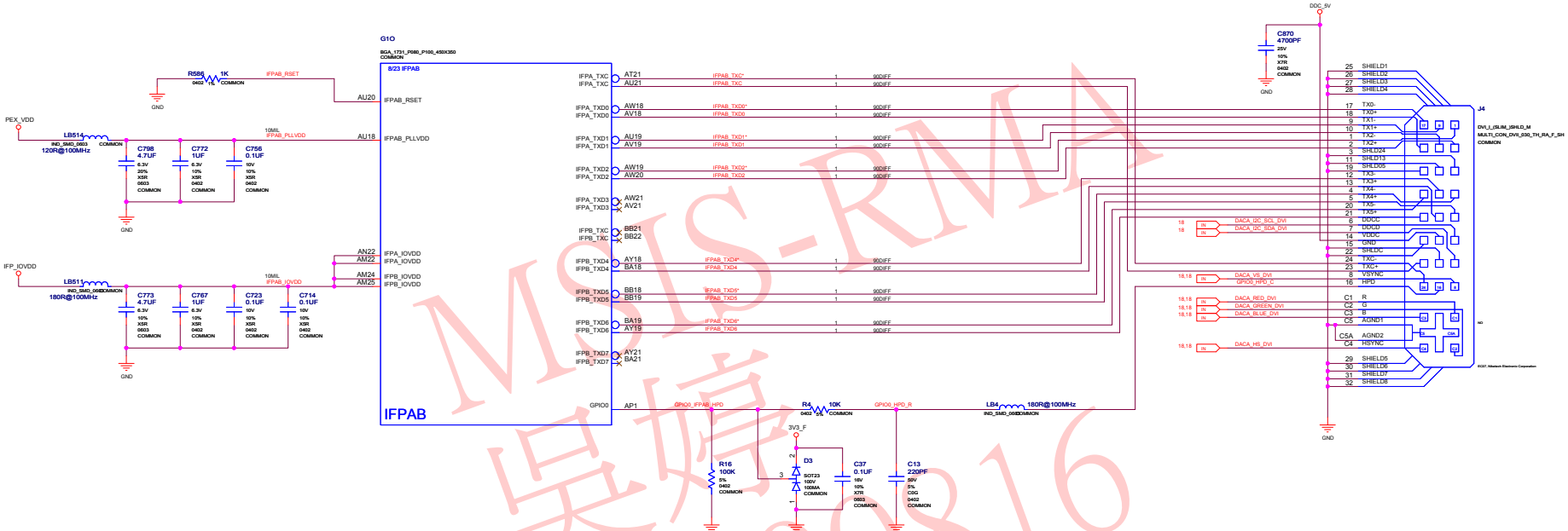
Page20: IFPAB DVI-I-DL (South)



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PAGE DETAIL	IFPAB DVI-DL (South)

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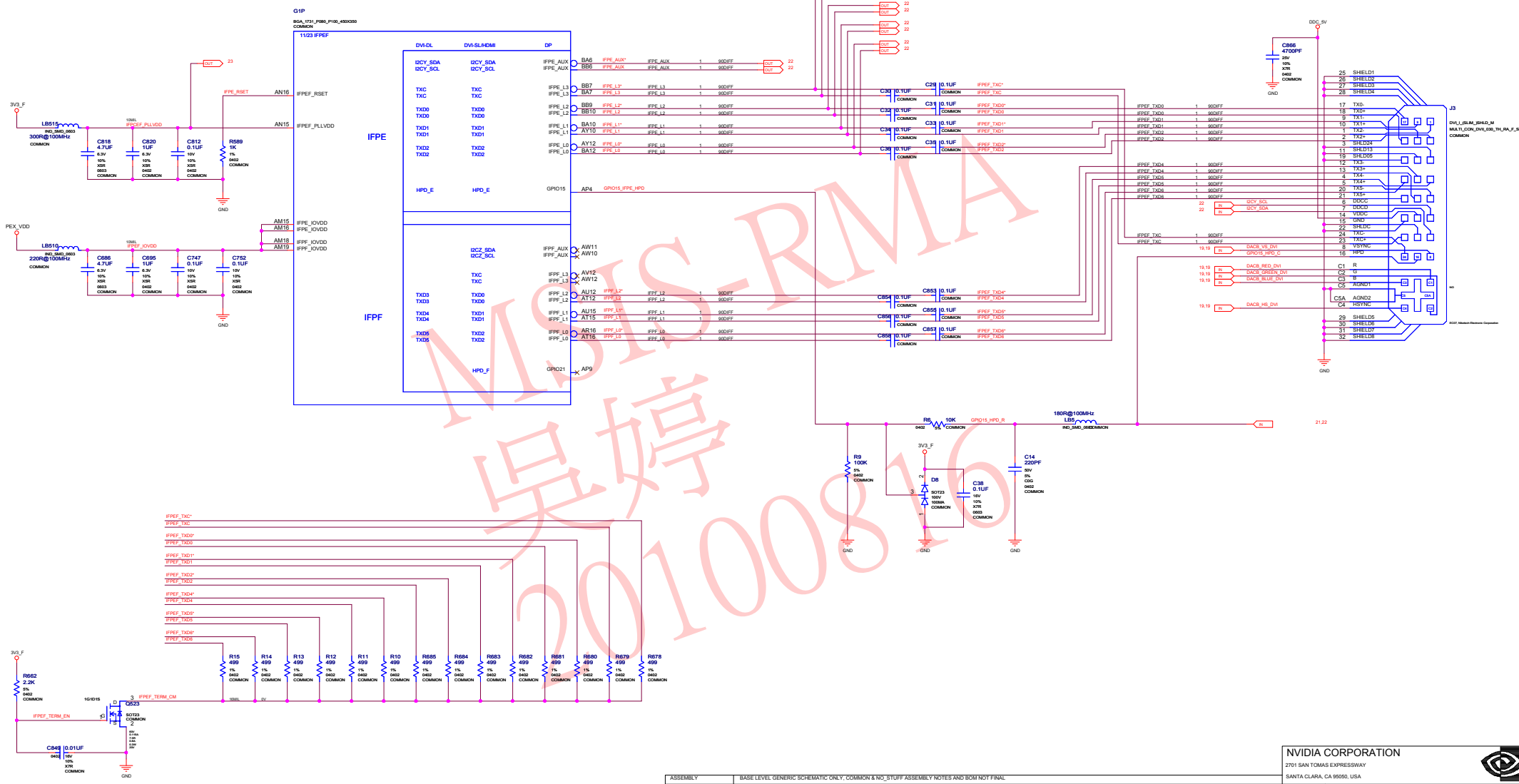
BOM REV	A	DATE	12-MAY-2010

Page21: IFPEF DVI-I-DL (Mid)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPEF DVI-DL (Mid)

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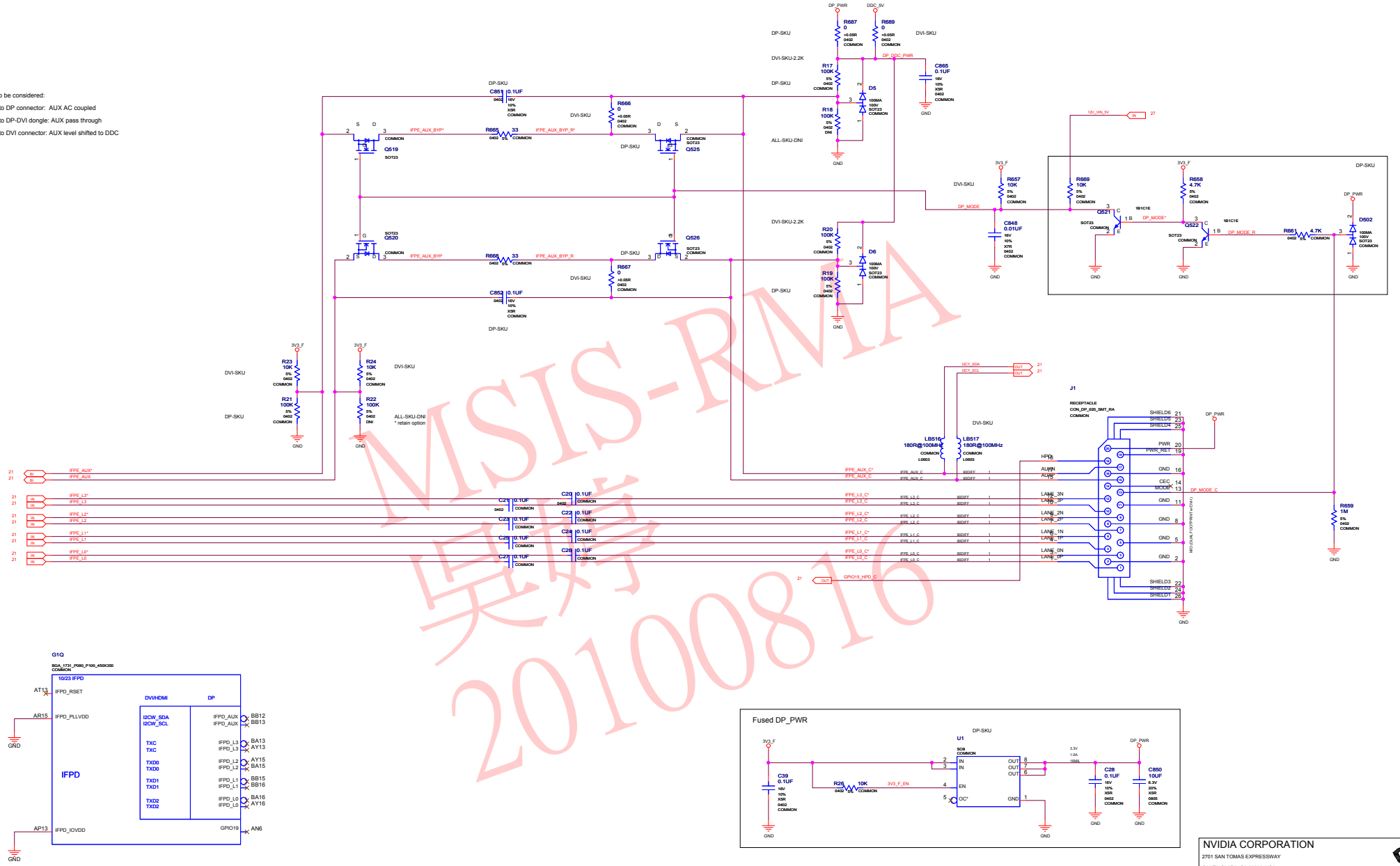
BOM REV	A	DATE	12-MAY-2010

Page22: IFPEF DP (Mid)

Three cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through
3. DP AUX to DVI connector: AUX level shifted to DDC



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPEF DP (Mid)

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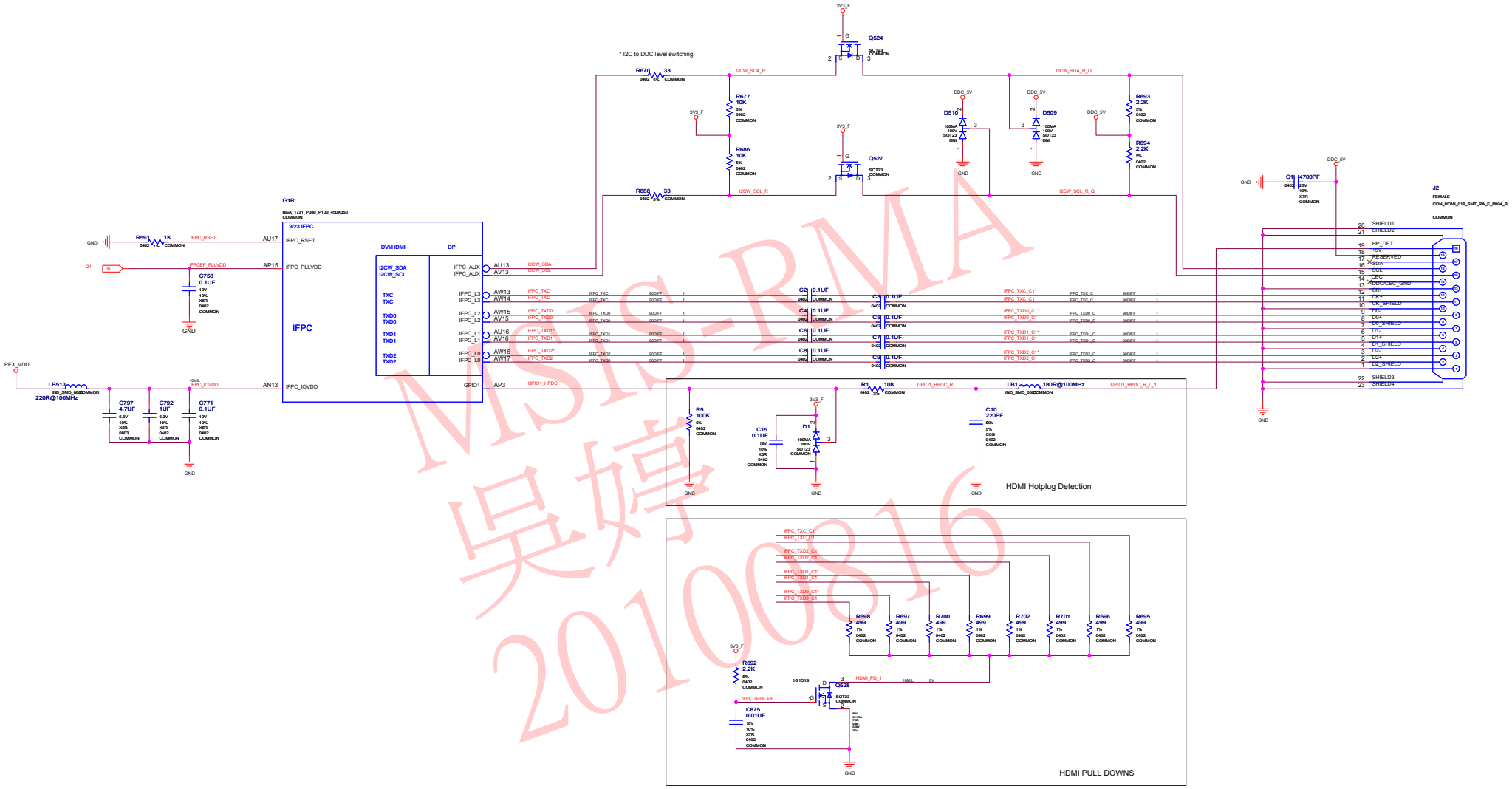
BOM REV	A	DATE	12-MAY-2010

Page23: IFPC mHDMI (North)



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPC mHDMI (North)

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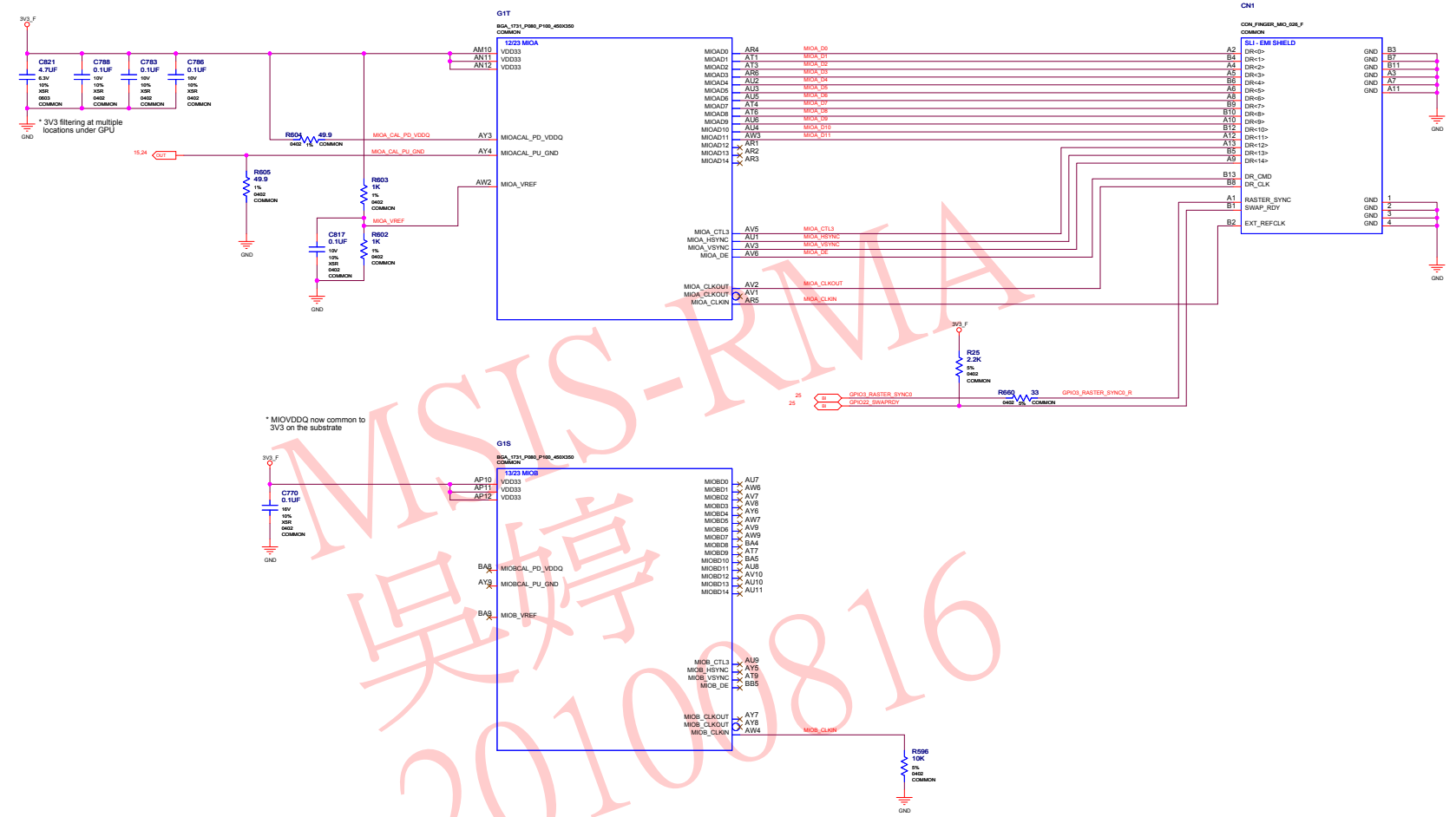
BOM REV	A	DATE	12-MAY-2010

Page24: Multi-use IO (MIO) Interface



MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR

NET	VOLTAGE	MIN_WIDTH
MIOA_CAL_PU_GND	0.6V	6MIL

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Multi-use IO (MIO) Interface

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PCB REV	P1041-B01	PAGE	
BOM REV	A	DATE	12-MAY-2010

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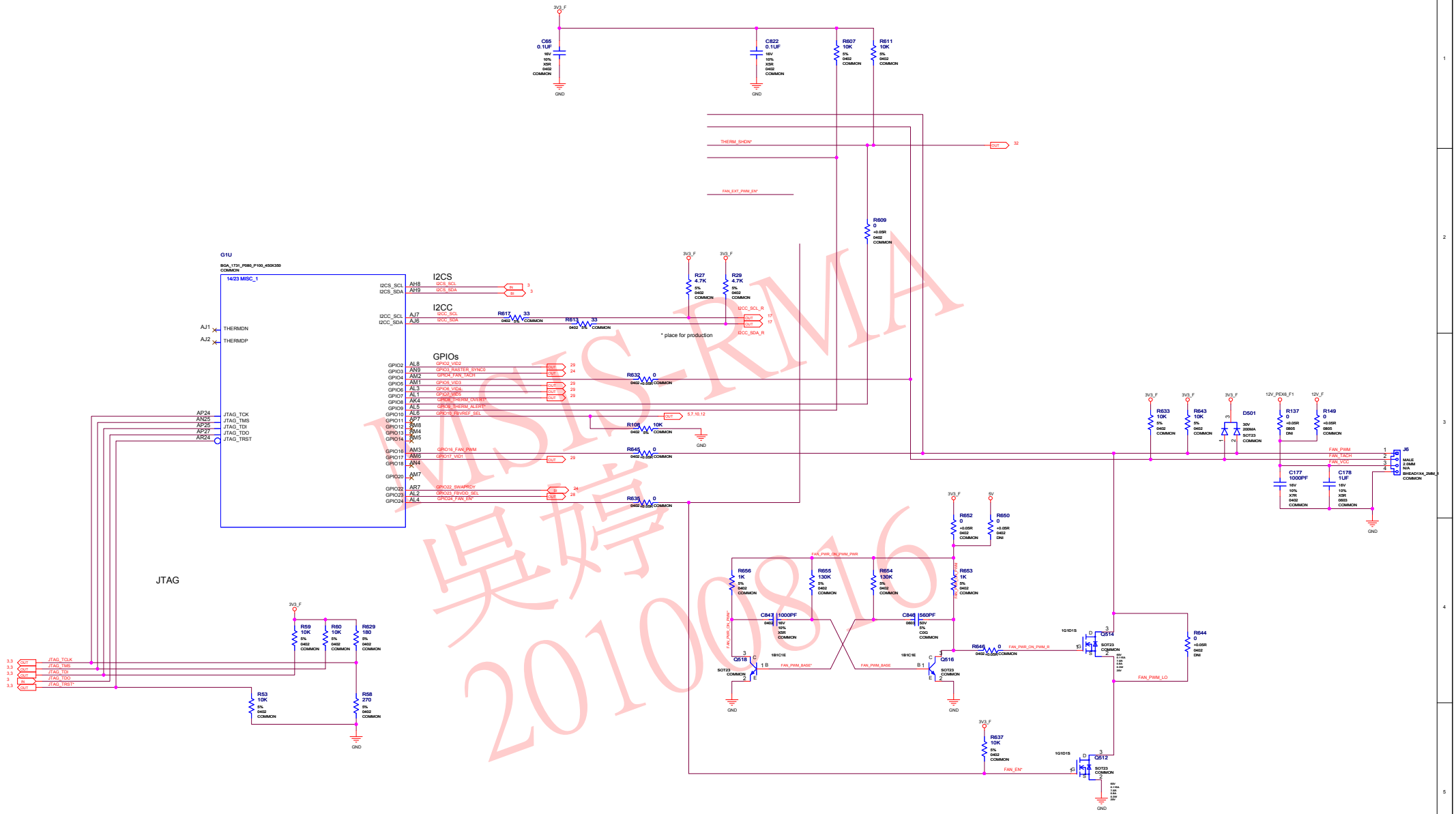
Page25: Misc: Fan, Thermal, JTAG, GPIO



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Misc: Fan, Thermal, JTAG, GPIO

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BOM REV	A	DATE	12-MAY-2010

Page26: Misc: ROM, HDCP, XTAL, Straps

STRAP0	USER_BIT [3..0]	0000:=> 5K PD	
STRAP1	3GIO_PADCFG_LUT_ADR	0000 :=>5K PD	0000 Desktop
		0010 For 0x0E22 :=> 15K PD	
STRAP2	PCI_DEVID [3:0]	0100 For 0x0E24 :=> 25K PD	
ROM_SI	RAMCFG[0]		
	RAMCFG[1]		
	RAMCFG[2]		
	RAMCFG[3]		
ROM_SO	VGA_DEVICE	1	
	SMB_ALT_ADDR	0	10k PD
	FB[0]_BAR_SIZE	0	
	XCLK_417	0	
ROM_SCLK	PEX_PLL_EN_TERM100	1 ENABLED	
	SLOT_CLK_CFG	1 ENABLE	
	SUB_VENDOR	1 Dedicated BIOS	45K PD
	PCI_DEVID_EXT	0 0xC	

32Mx32 256 bit Samsung for SKU 10 first memory
0011: PD 20K
32Mx32 256 bit Hynix for SKU 10 2'nd memory
0010: PD 15K

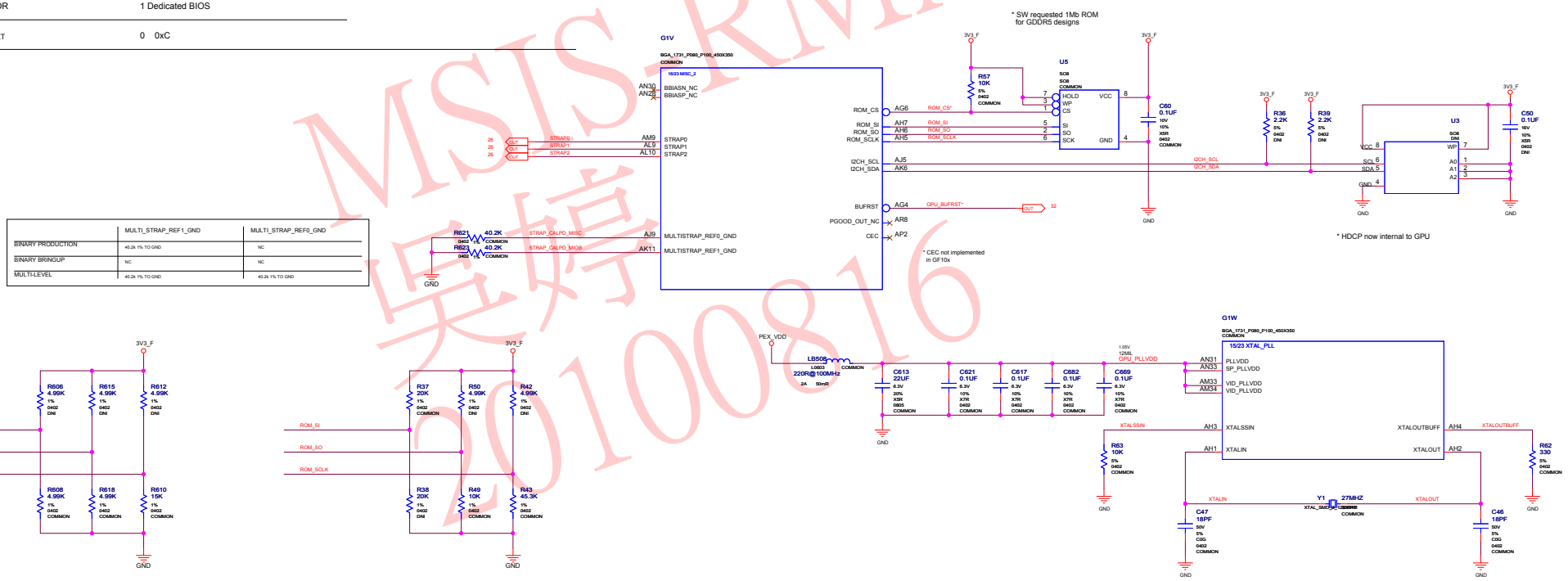
32Mx32 192 bit Samsung for SKU 0 first memory
1011: PU 20K
32Mx32 192 bit Hynix for SKU 0 2'nd memory
1010: PU 15K

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit	Qimonda
0010	32Mx32 256-bit	Hynix
0011	32Mx32 256-bit	Samsung
0100	Reserved	
0101	64Mx32 256-bit	Qimonda
0110	64Mx32 256-bit	Hynix
0111	64Mx32 256-bit	Samsung
1000	Reserved	
1001	32Mx32 192-bit	Qimonda
1010	32Mx32 192-bit	Hynix
1011	32Mx32 192-bit	Samsung
1100	Reserved	
1101	64Mx32 192-bit	Qimonda
1110	64Mx32 192-bit	Hynix
1111	64Mx32 192-bit	Samsung

MISC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Misc: ROM, HDCP, XTAL, Straps

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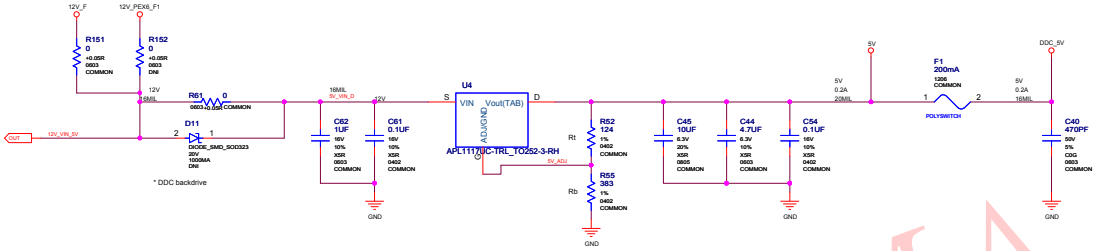
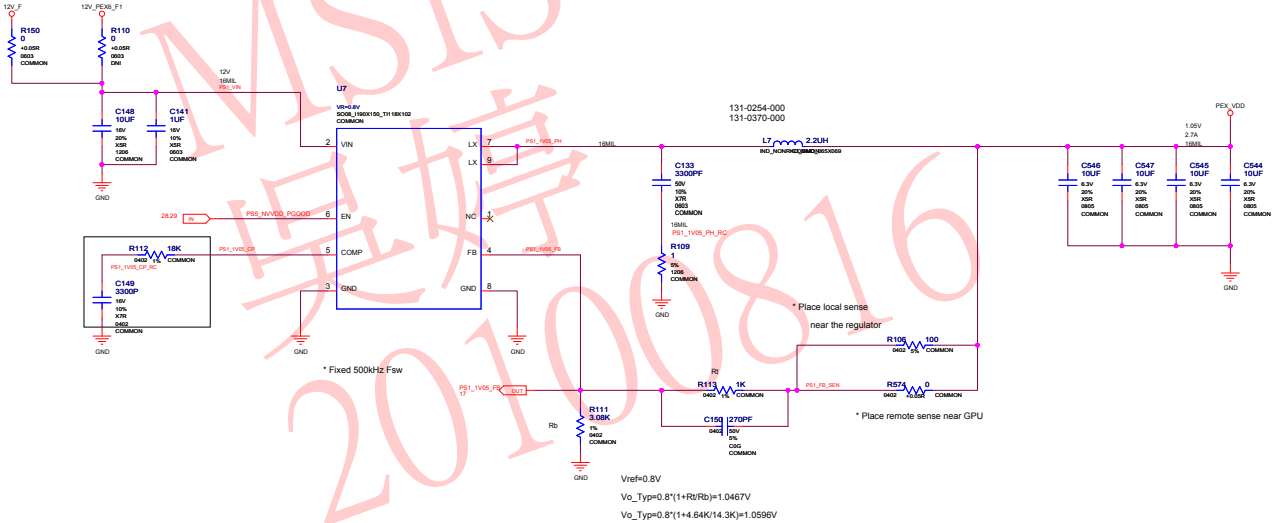
PCB REV	P1041-B01	PAGE	
BOM REV	A	DATE	12-MAY-2010

Page27: PS: 5V, PEX_VDD



Input ripple (Irms) = ~0.9A @ 2.7A



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PAGE DETAIL	PS: 5V, PEX_VDD

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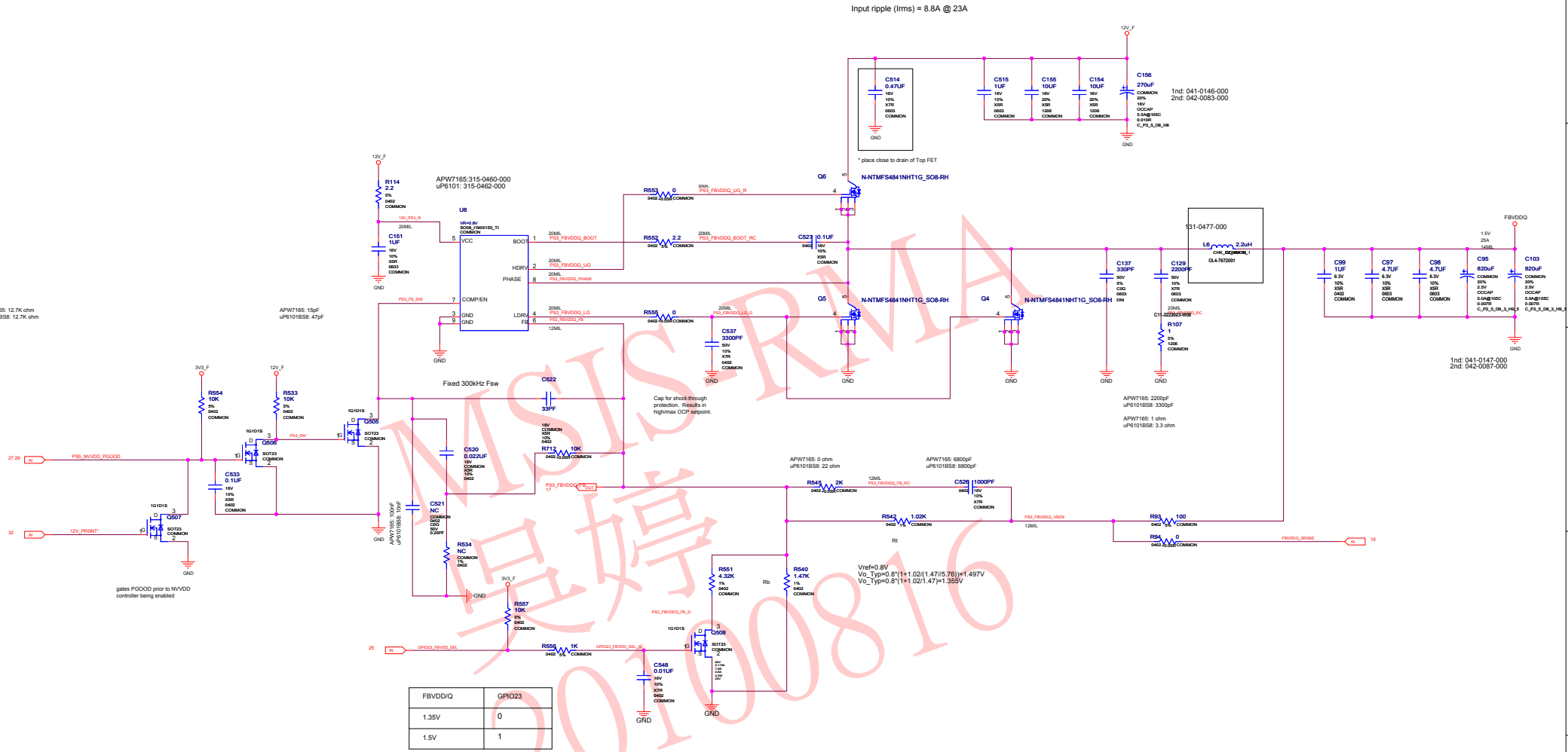
PCB REV	P1041-B01	PAGE	
BOM REV	A	DATE	12-MAY-2010

Page28: PS: FBVDD/Q



FBVDD/Q	GPIO23
1.35V	0
1.5V	1

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PAGE DETAIL	PS: FBVDD/Q

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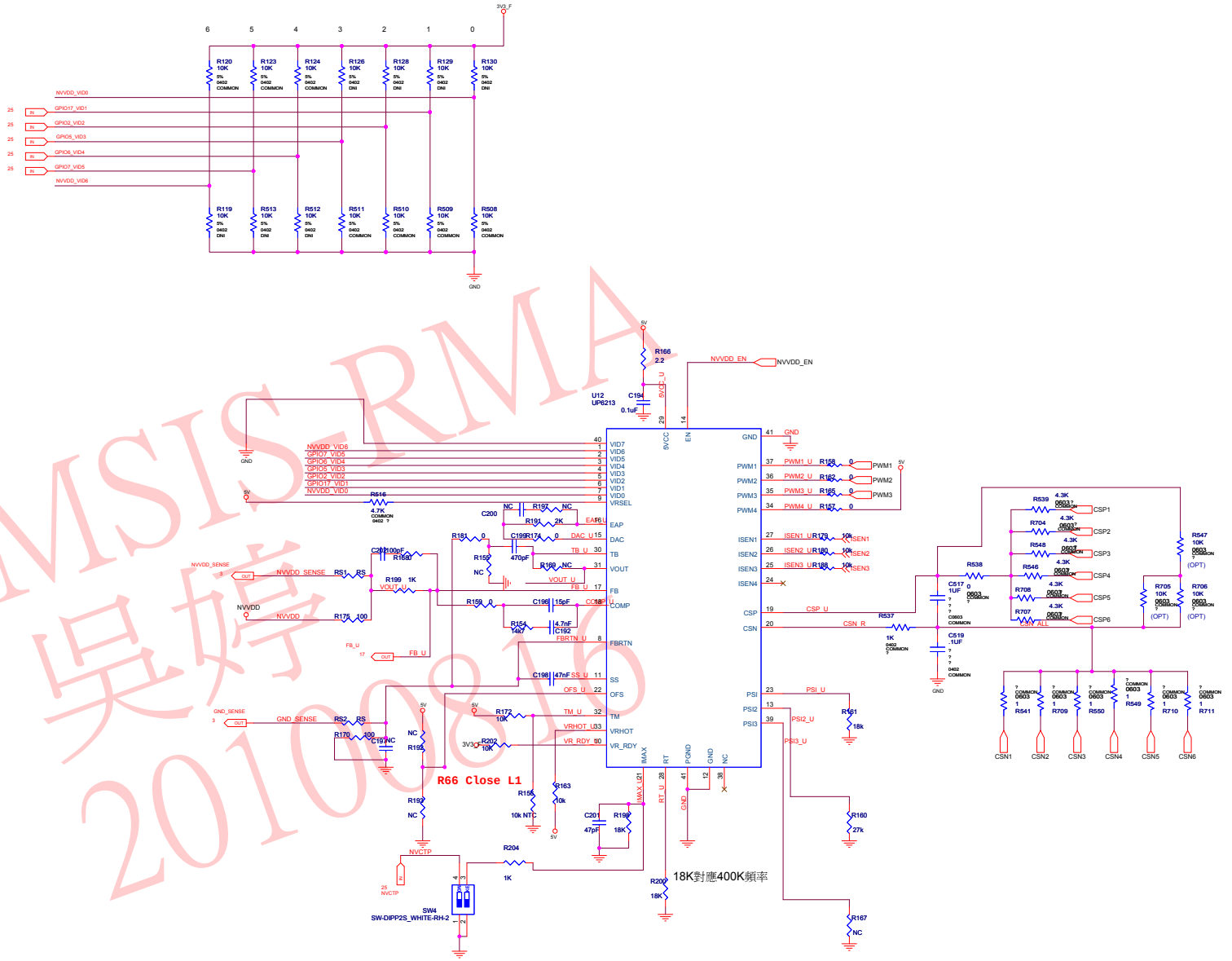
NV_PN	600-11041-BASE-000		
PCB REV	P1041-B01	PAGE	
BOM REV	A	DATE	12-MAY-2010

Page29: PS: NVVDD Controller

VID Table

GPIO7	GPIO6	GPIO5	GPIO2	GPIO17	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V



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PAGE DETAIL	PS: NVVDD Controller

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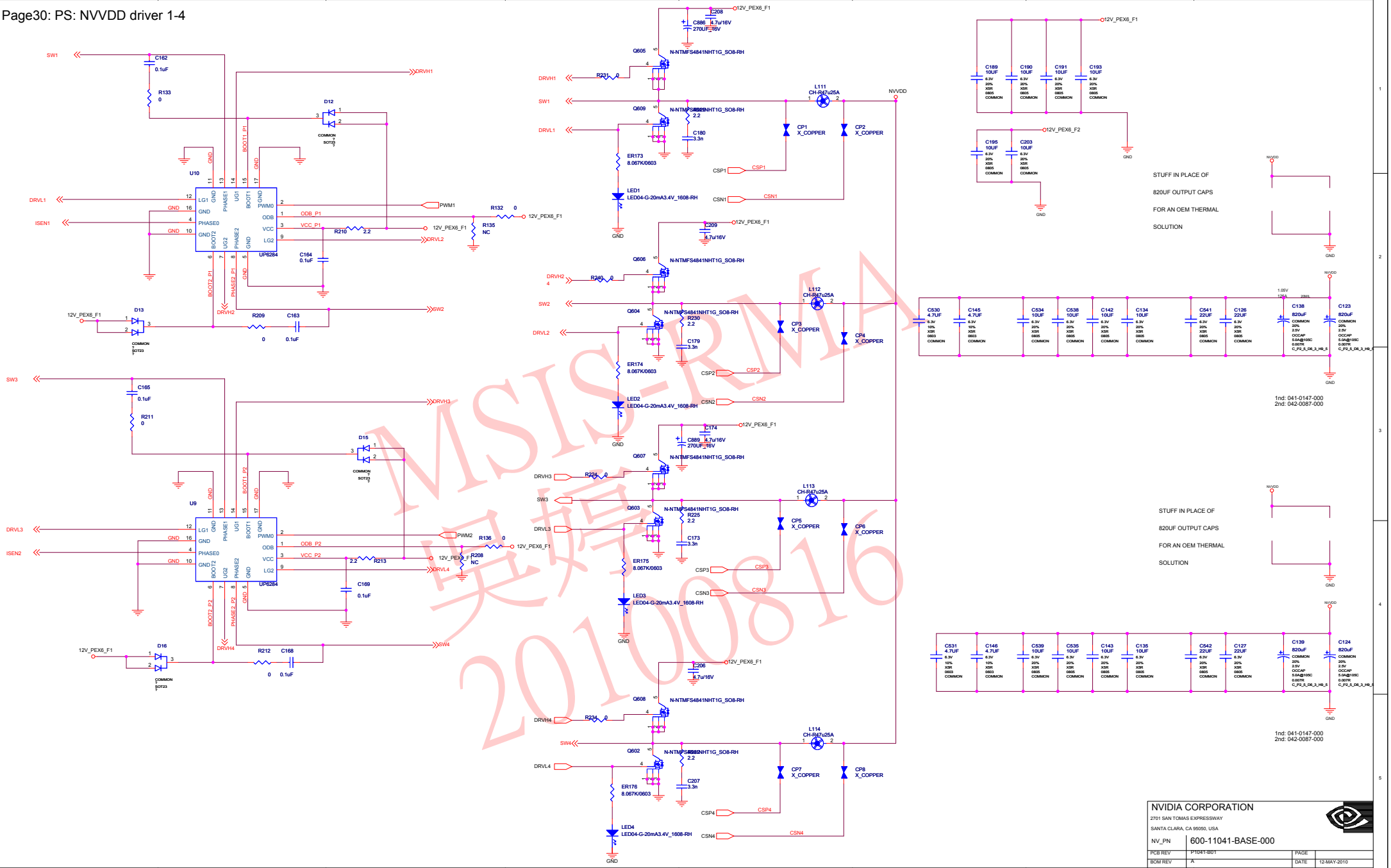
BOM REV	A	DATE:	12-MAY-2010

Page30: PS: NVVDD driver 1-4



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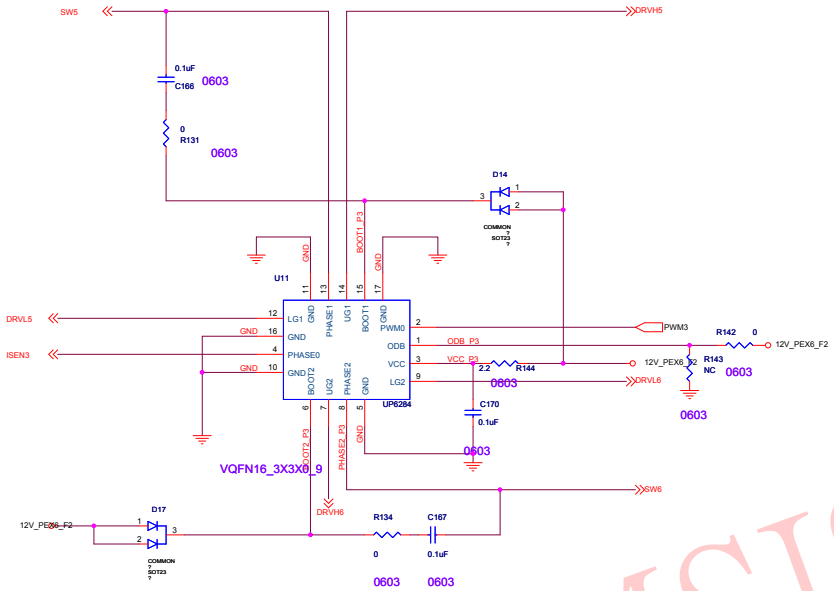
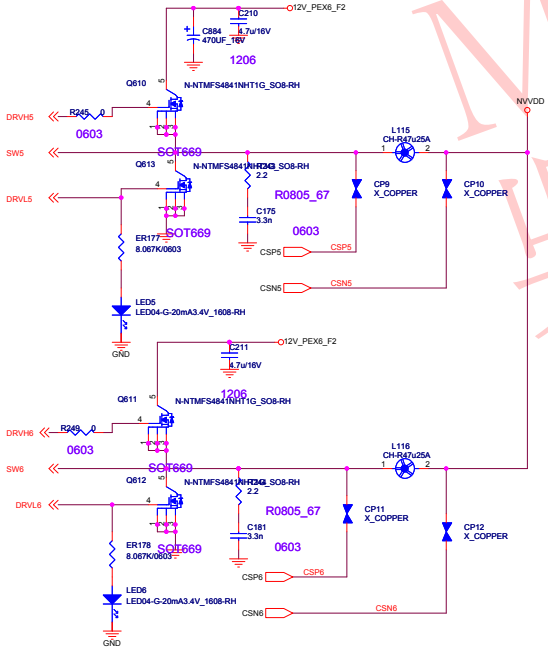
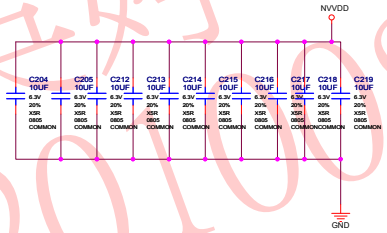
PAGE	
DATE	12-MAY-2010

Page31: PS: NVVDD driver 5-6





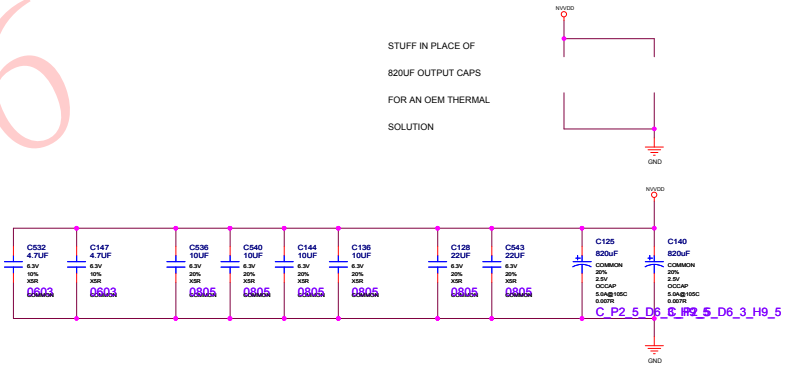


STUFF IN PLACE OF

820UF OUTPUT CAPS

FOR AN OEM THERMAL

SOLUTION



1nd: 041-0147-000
2nd: 042-0087-000

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PAGE DETAIL	PS: NVVDD Phase 3

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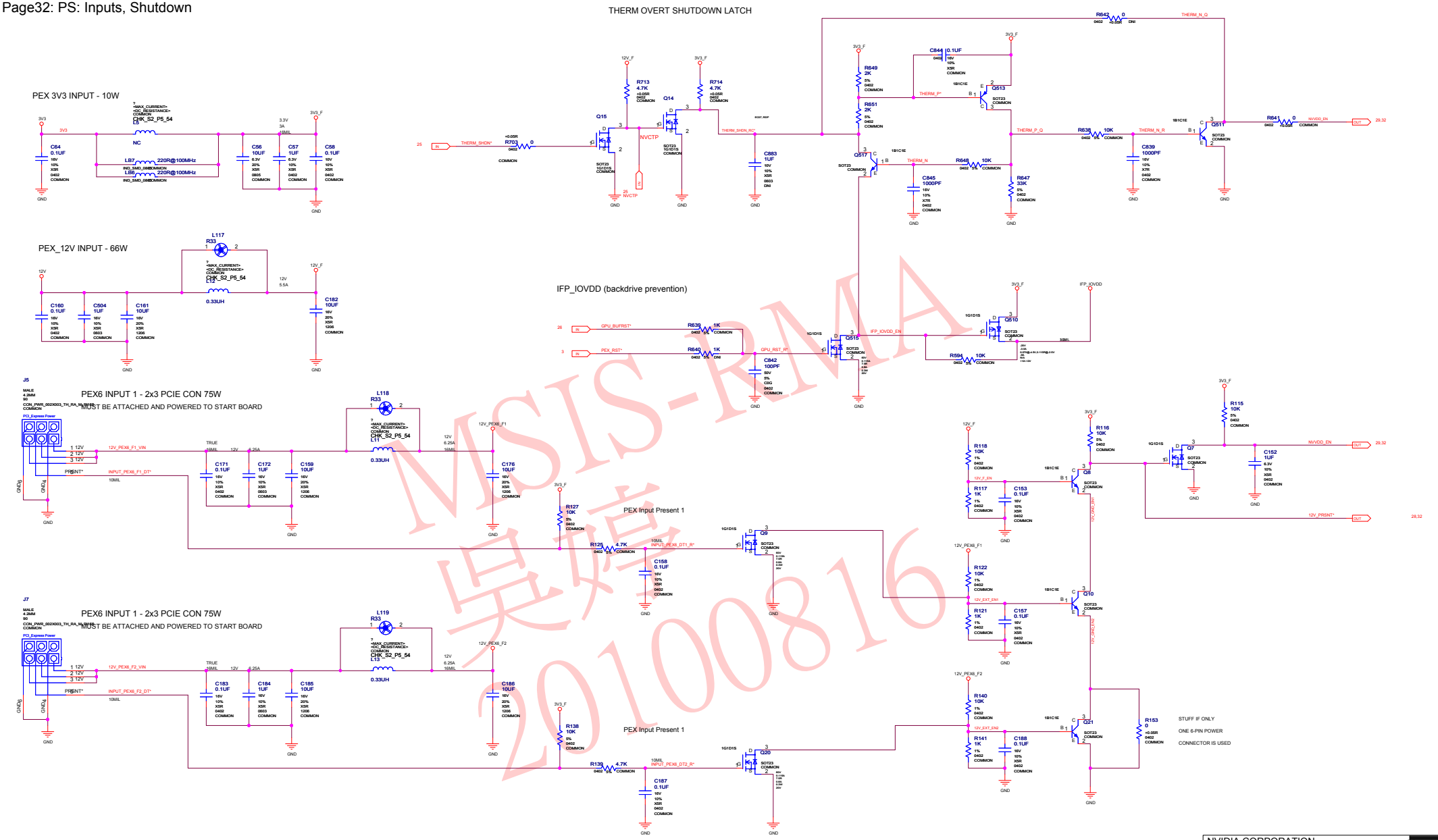
BOM REV	A	DATE	12-MAY-2010

Page32: PS: Inputs, Shutdown



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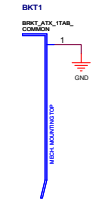
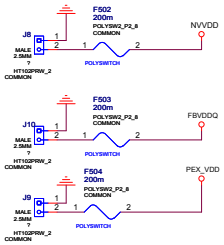
Page33: Mechanical: Bracket/Thermal Solution

Brackets:

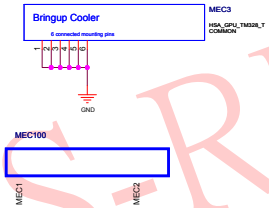
Bracket with DVI_DP_mHDMI : 151-10001-0355-071



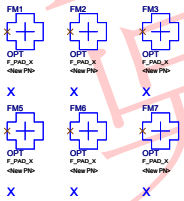


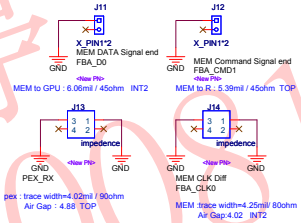
Bracket Screw

Cooler/GPU Stiffener



remove mec1





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PAGE DETAIL	Mechanical: Bracket/Thermal Solution

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BOM REV	A	DATE	12-MAY-2010