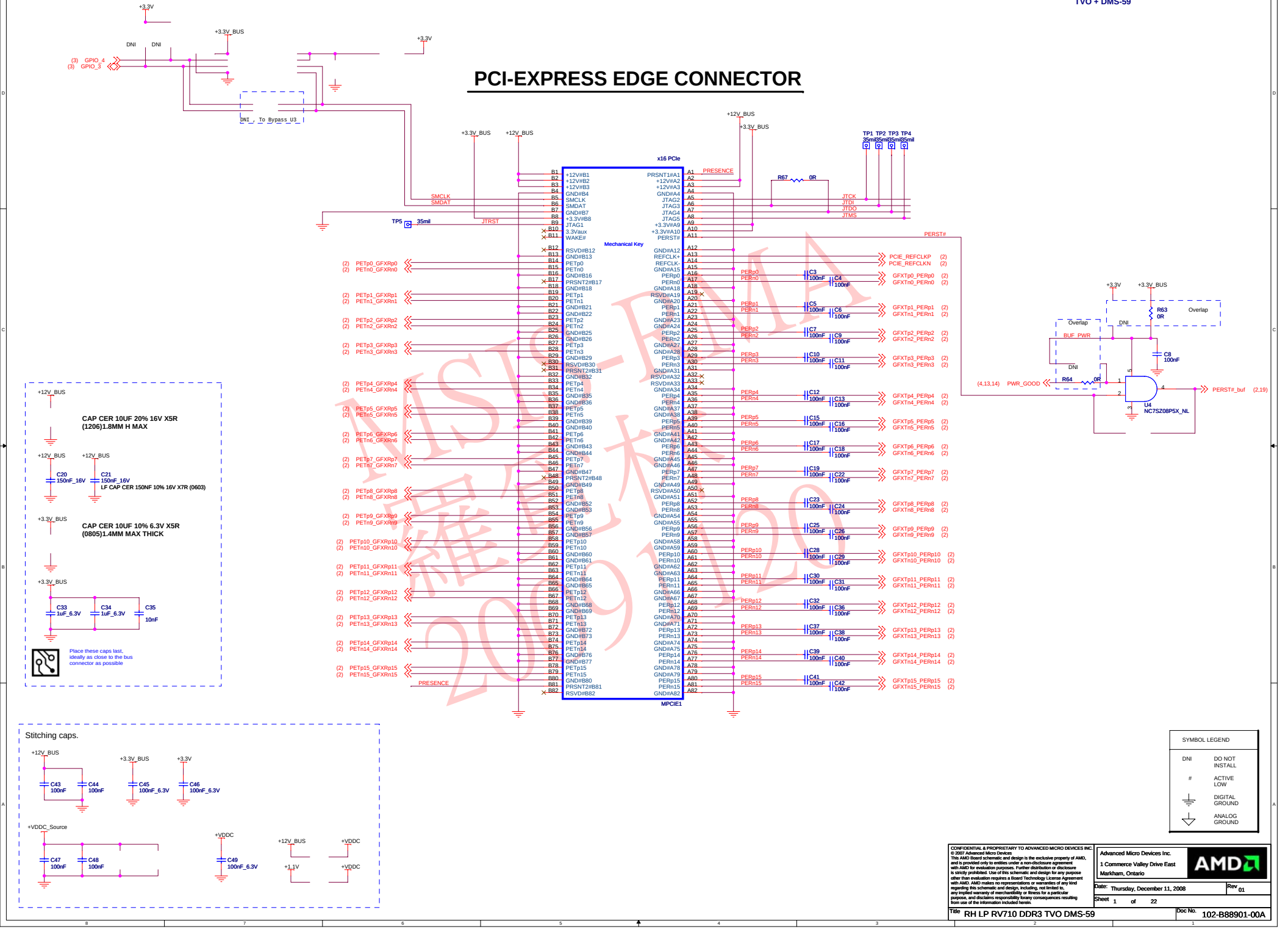
RV710

TVO + DMS-59

PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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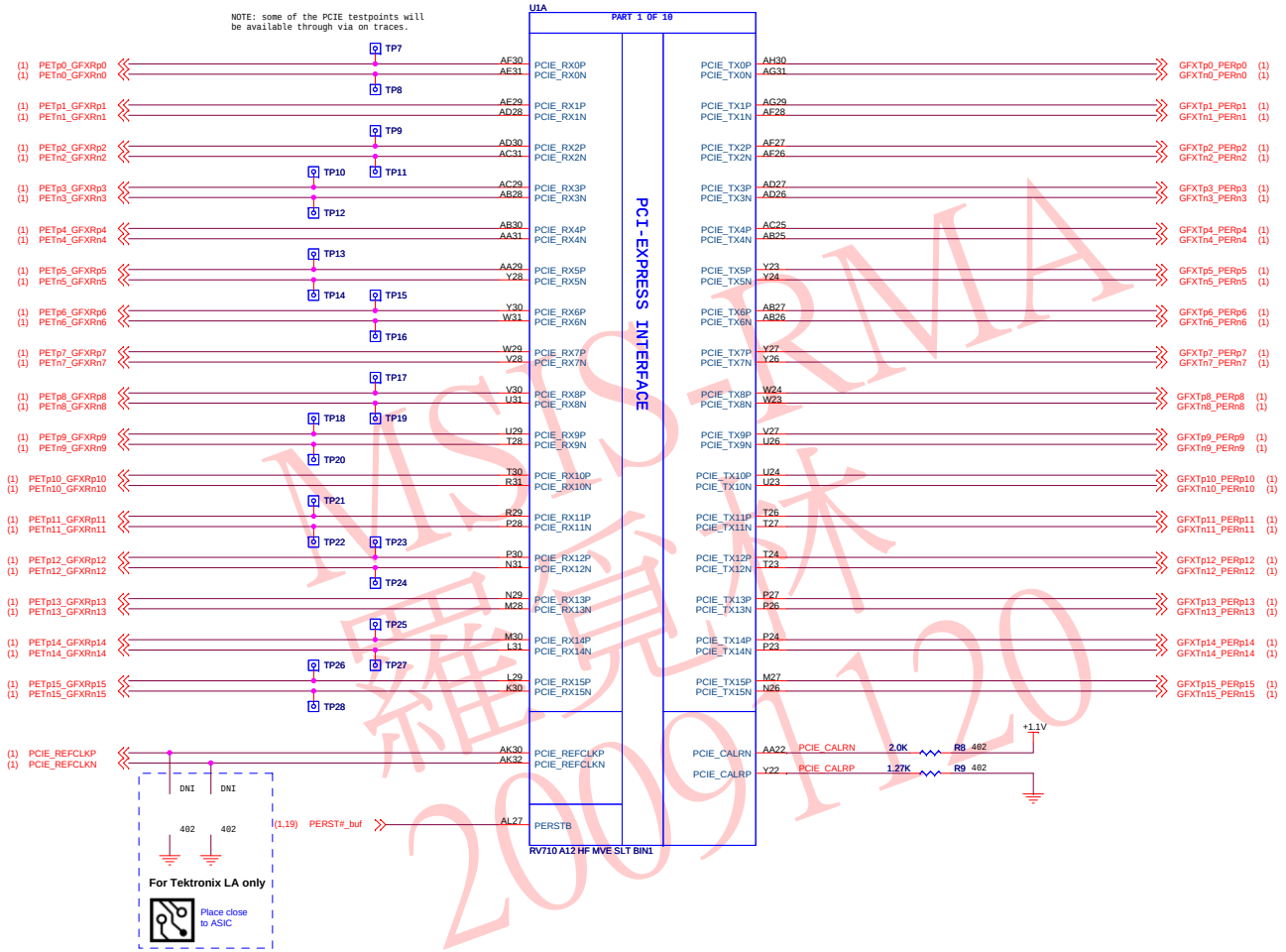

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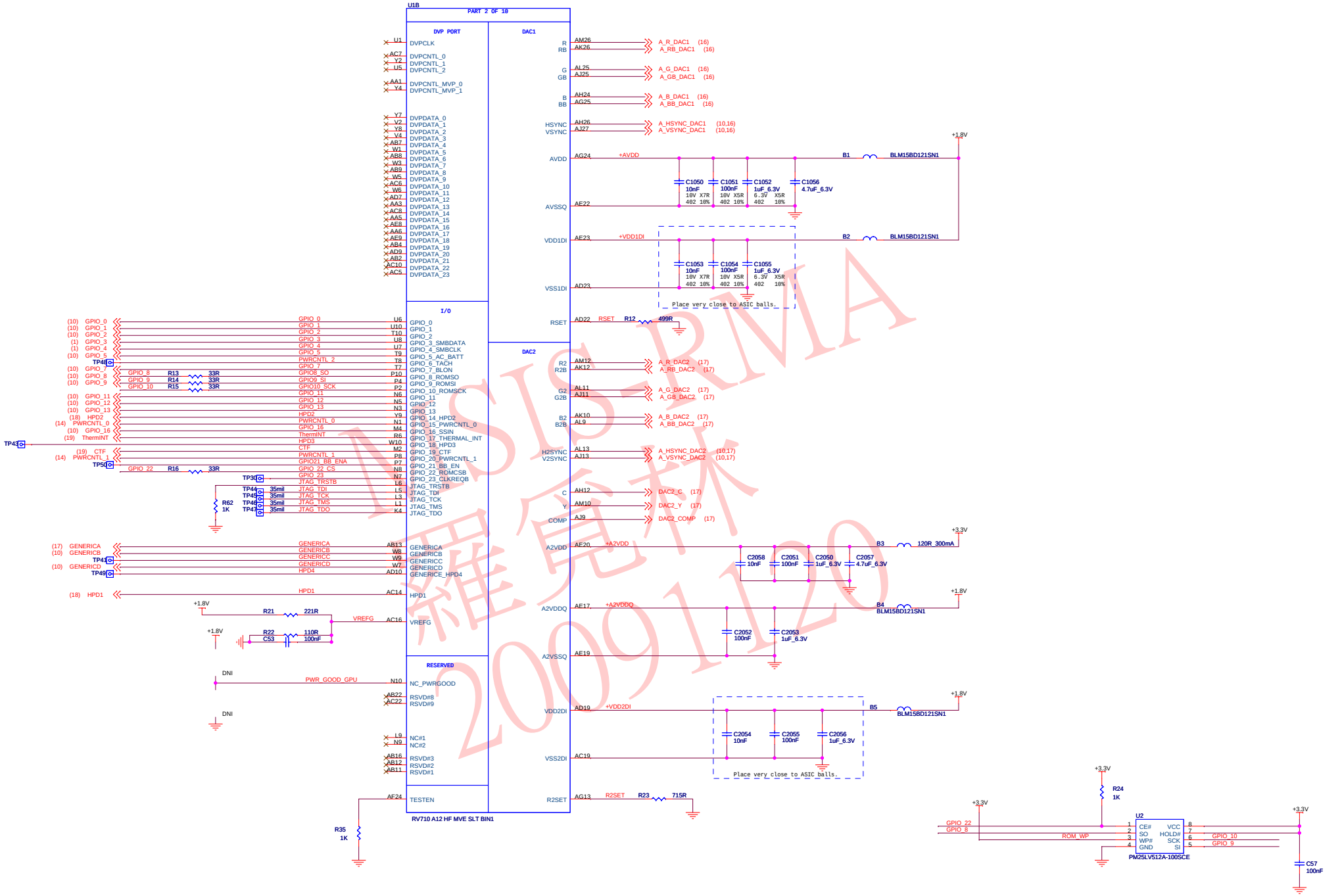

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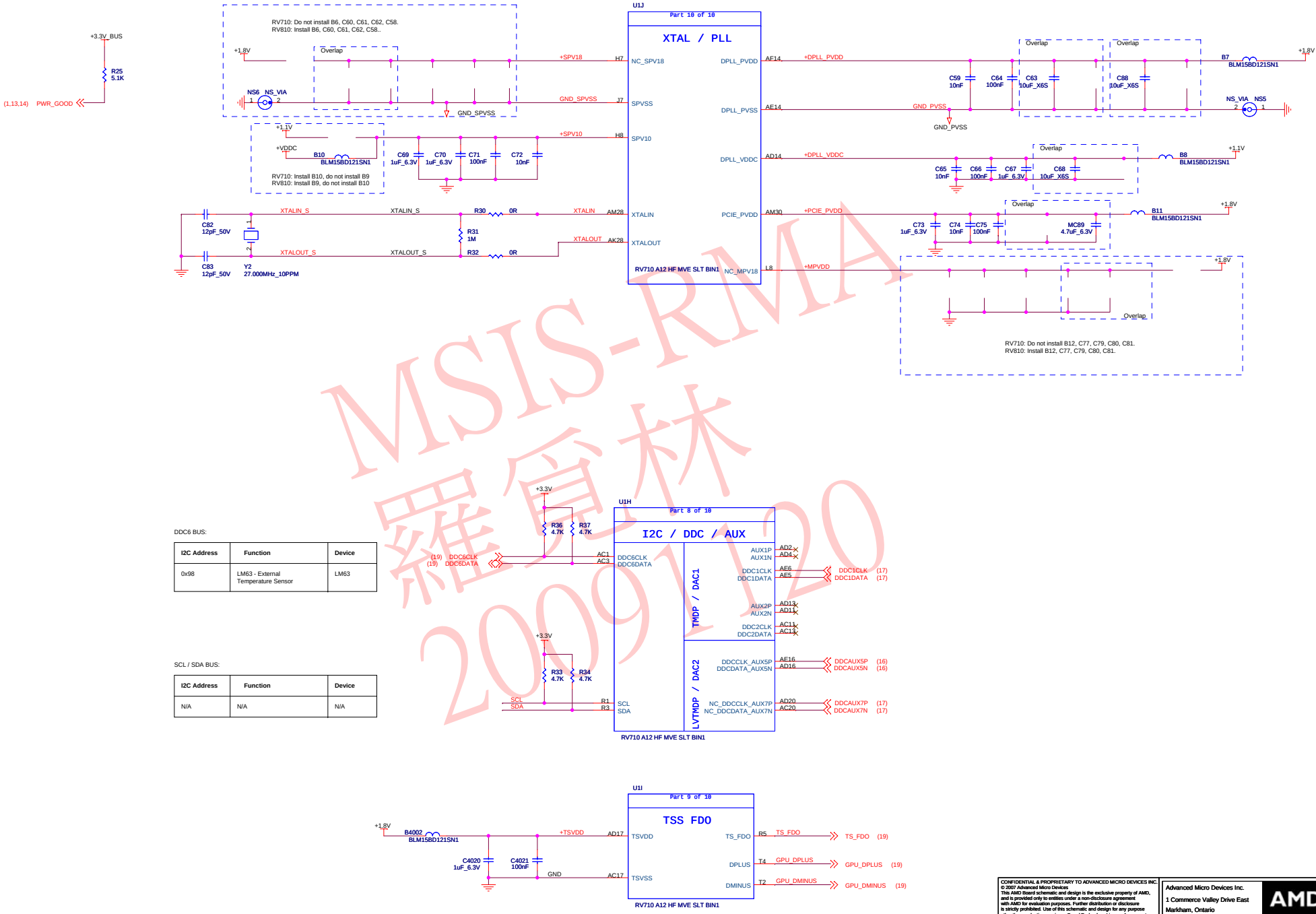

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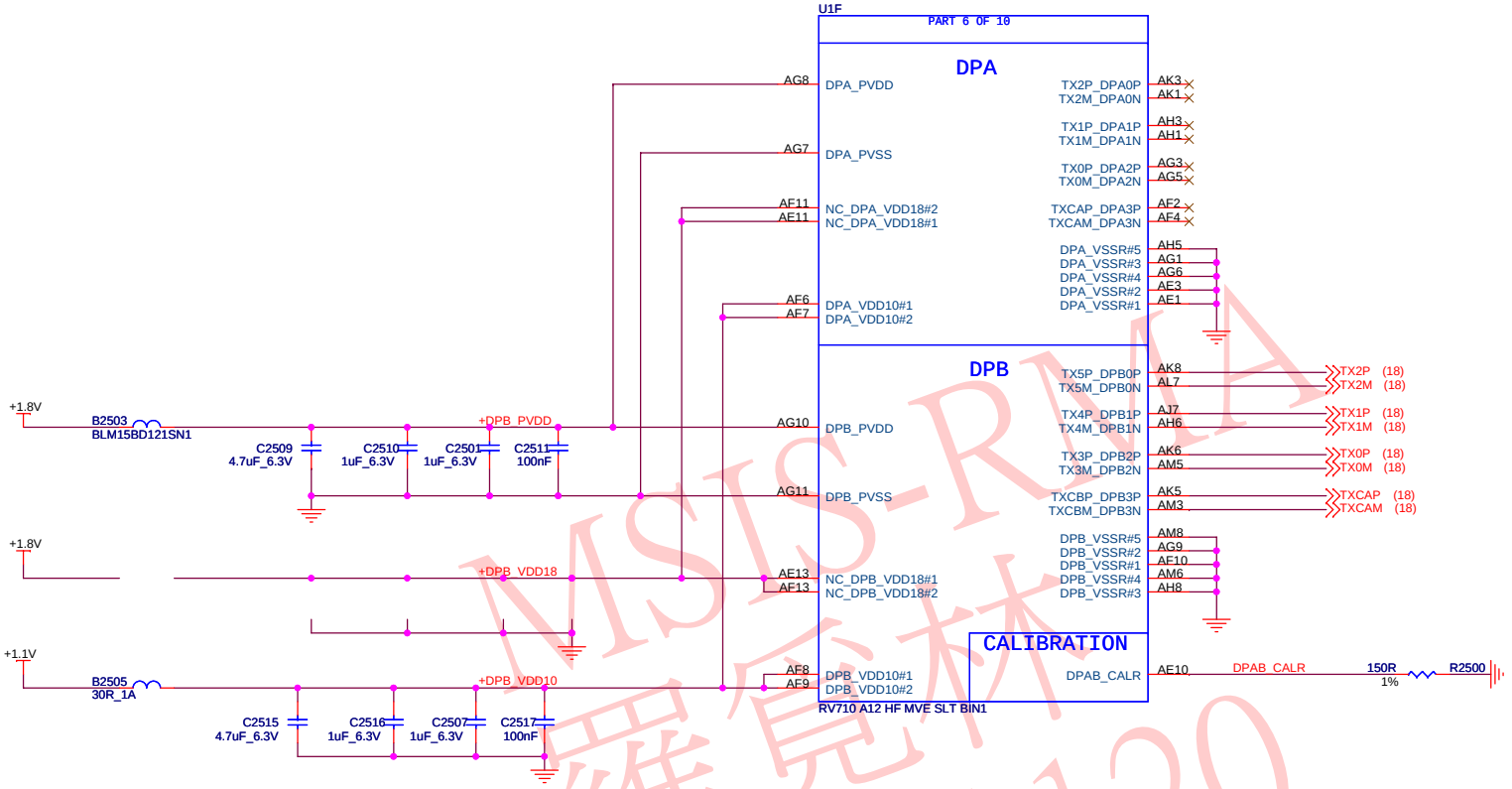
TMDP INTERFACE



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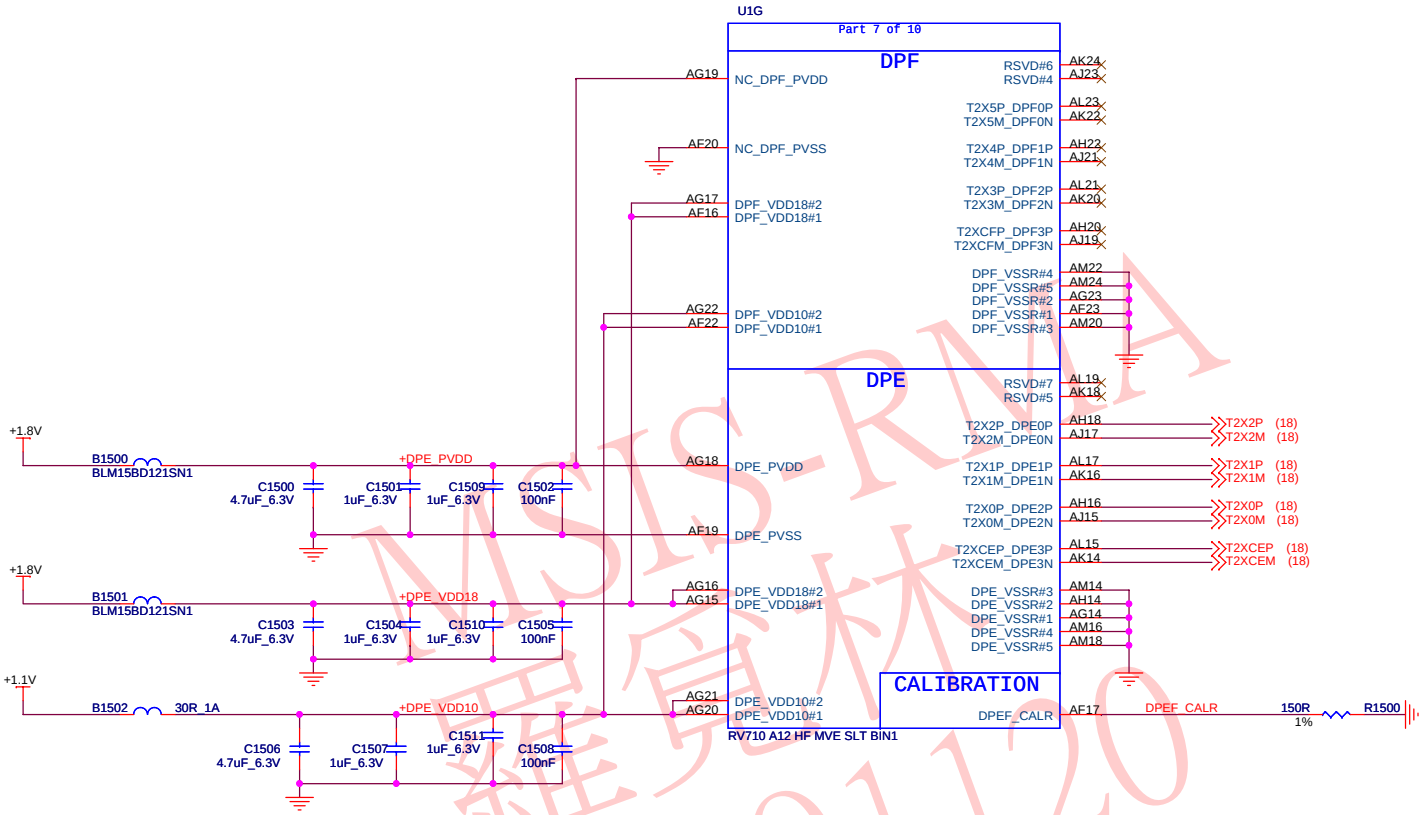
LVTMDP INTERFACE



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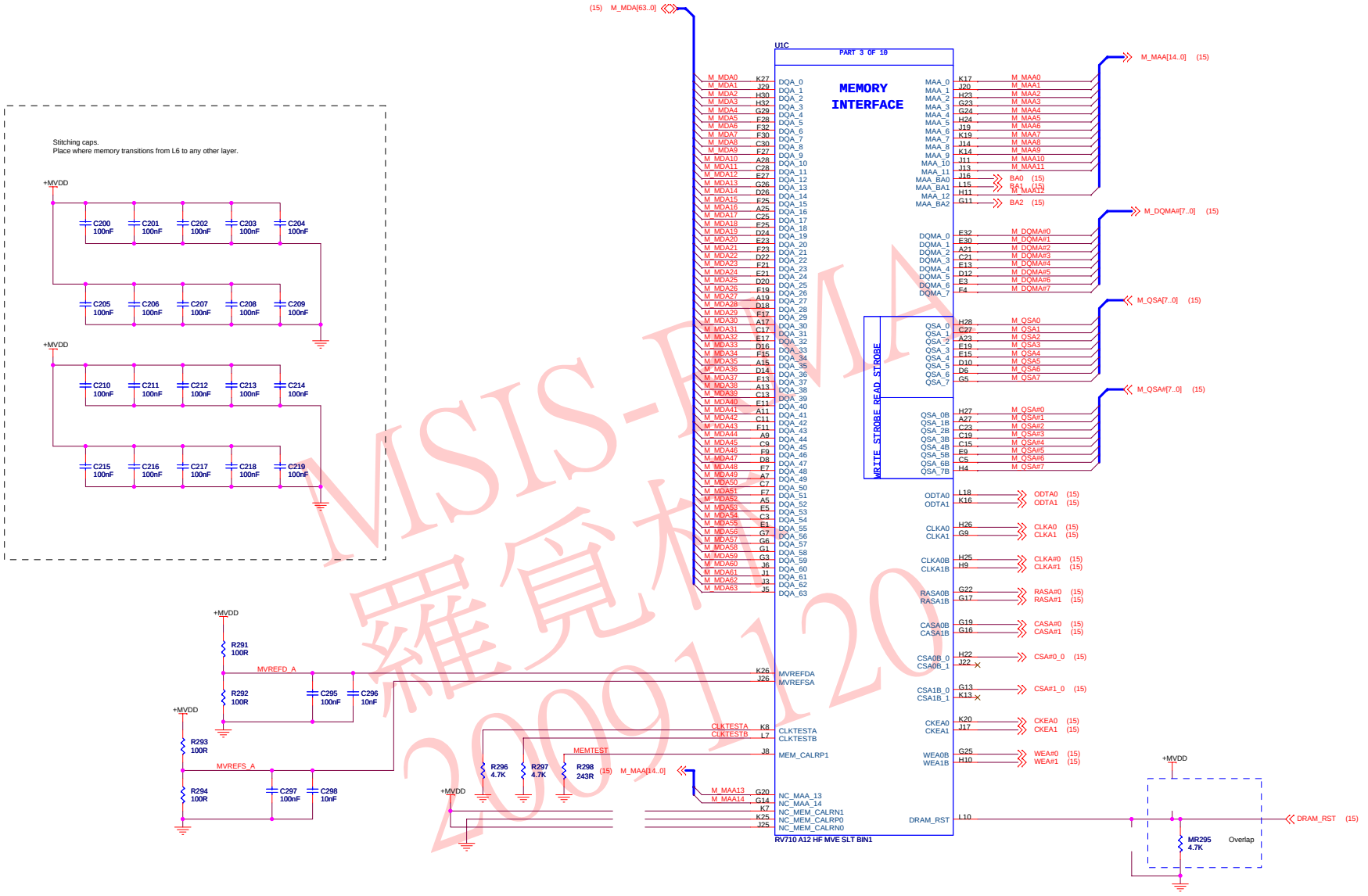
MEMORY INTERFACE



DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R

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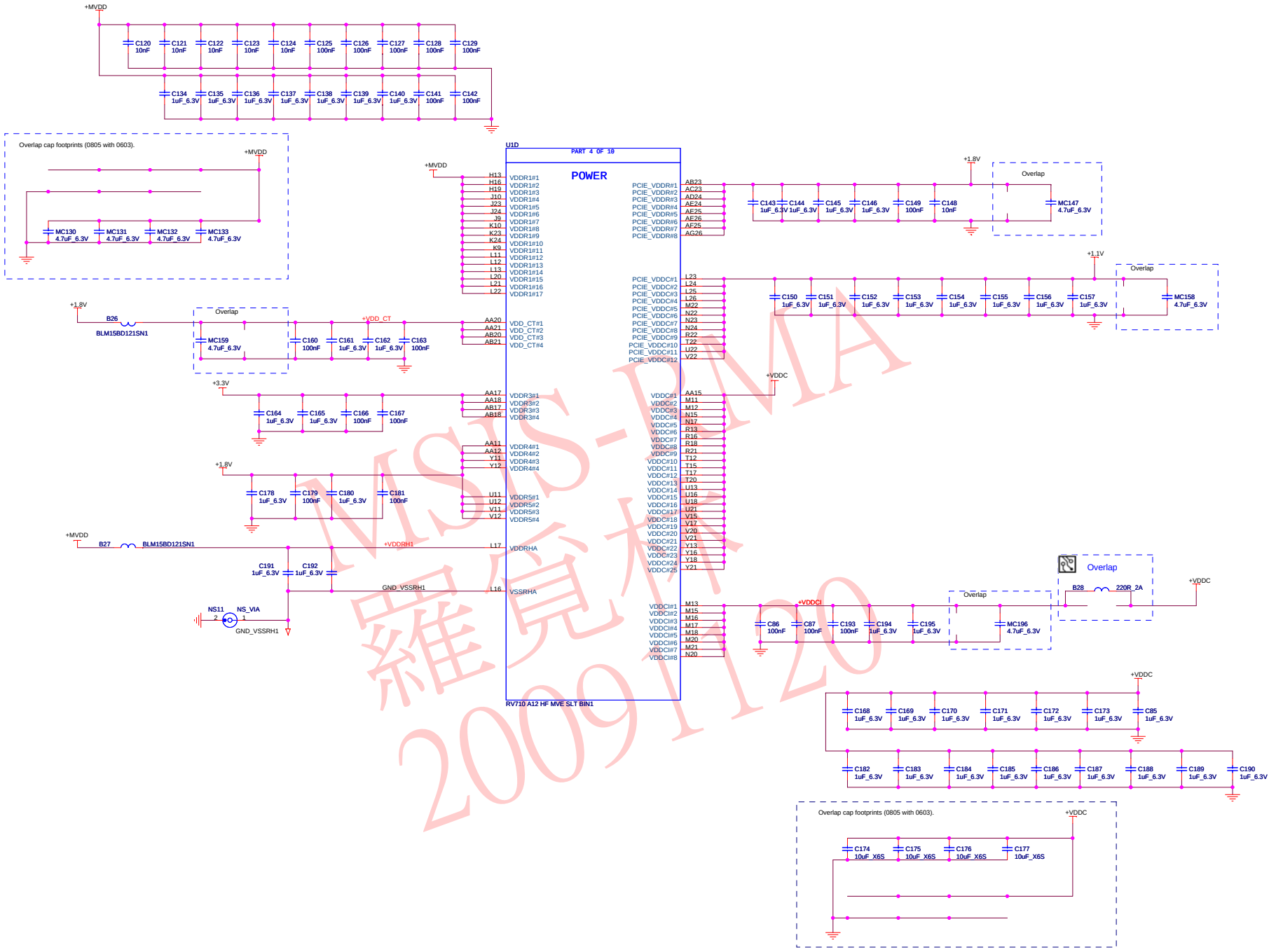

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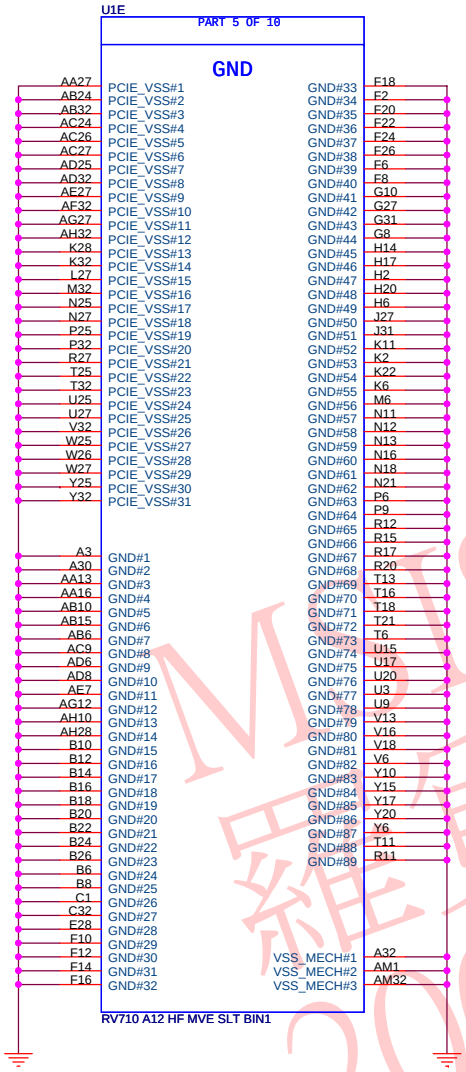

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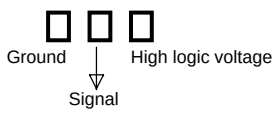
PIN BASED STRAPS

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout



PIN BASED STRAPS

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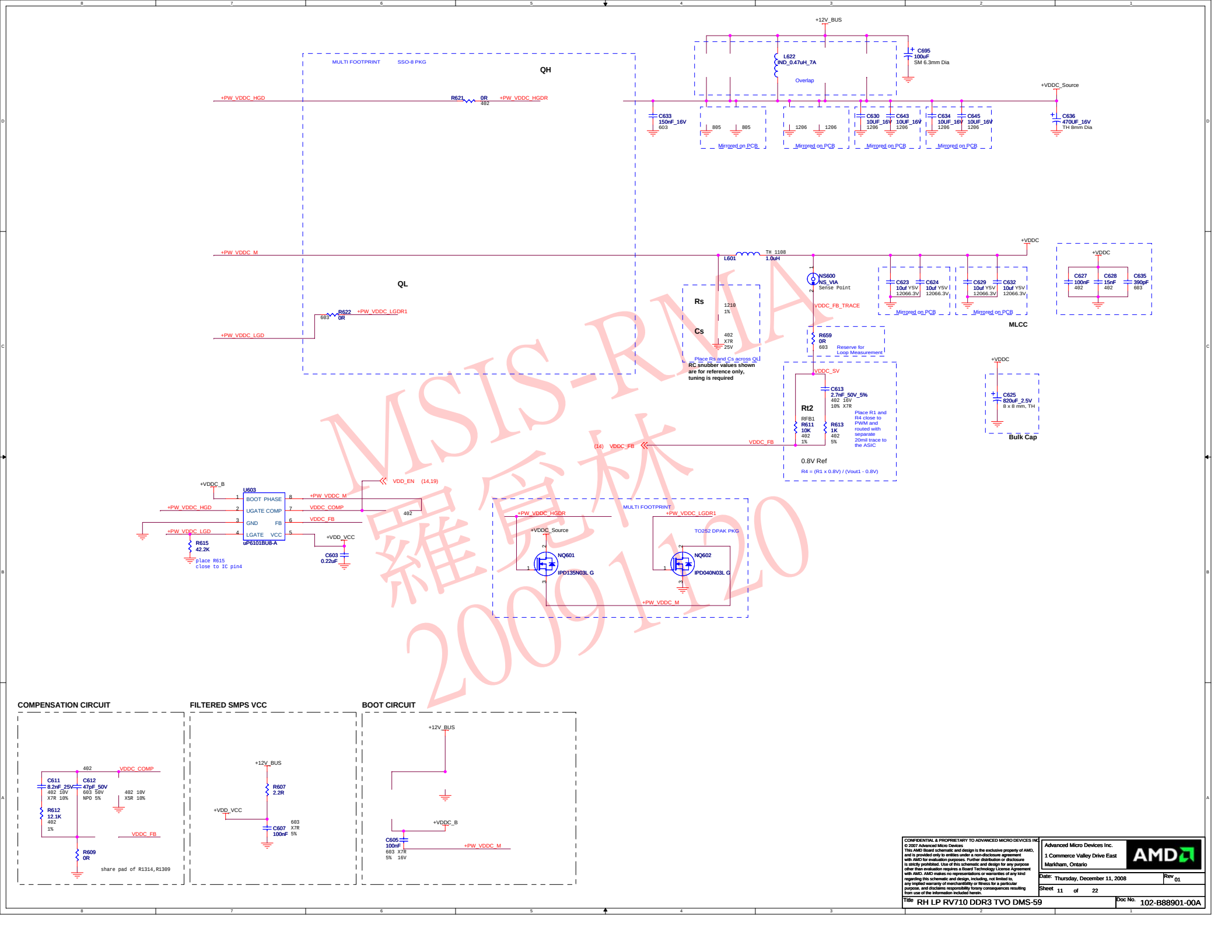

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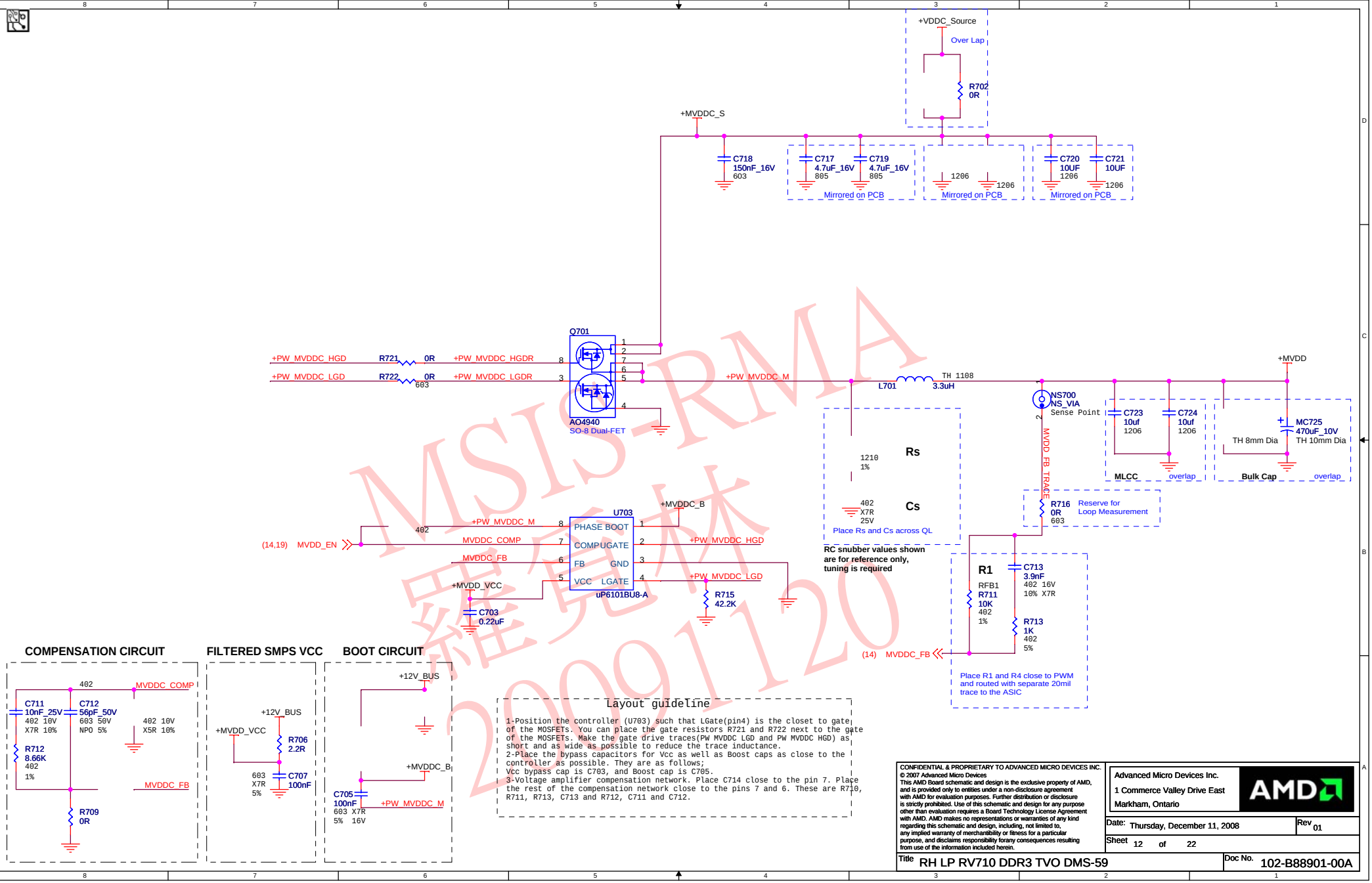
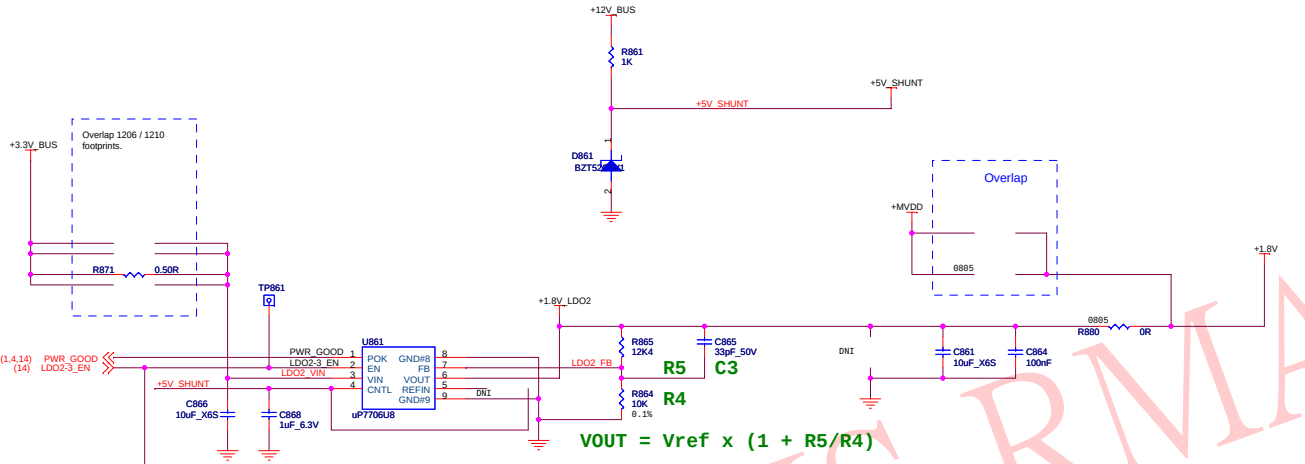
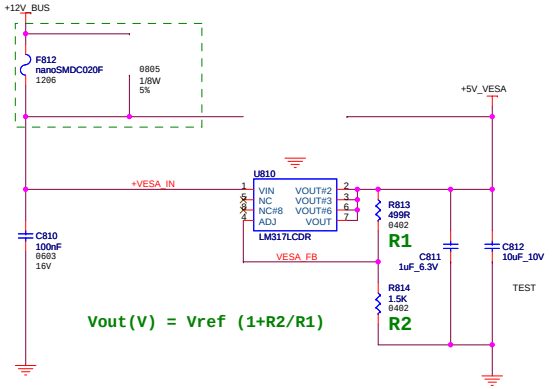


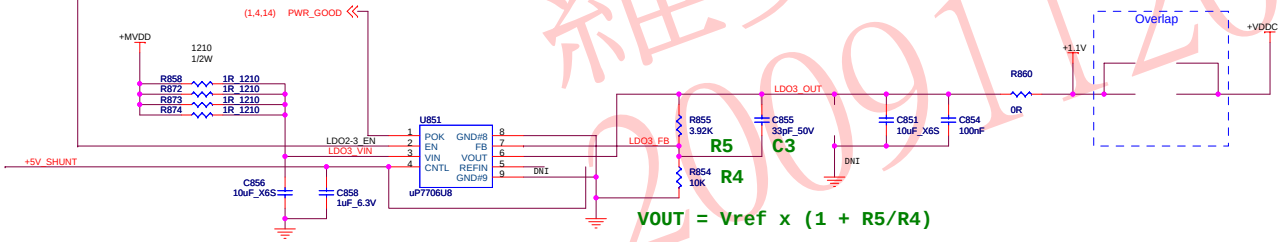
LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

Regulators for +5V_VESA





LDO #3: Vin = +1.4V to 2.087VMAX Vout = +1.1V +/- 2.5% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



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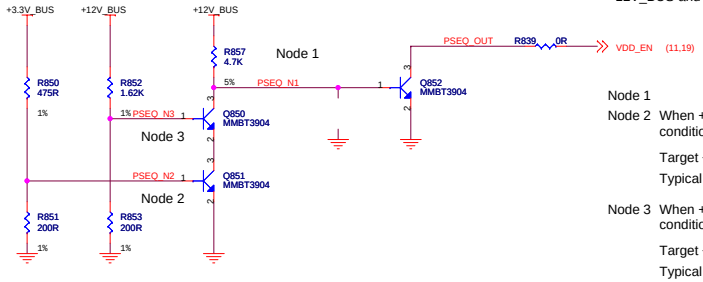
Power up/down Sequencing



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.

Node 1

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

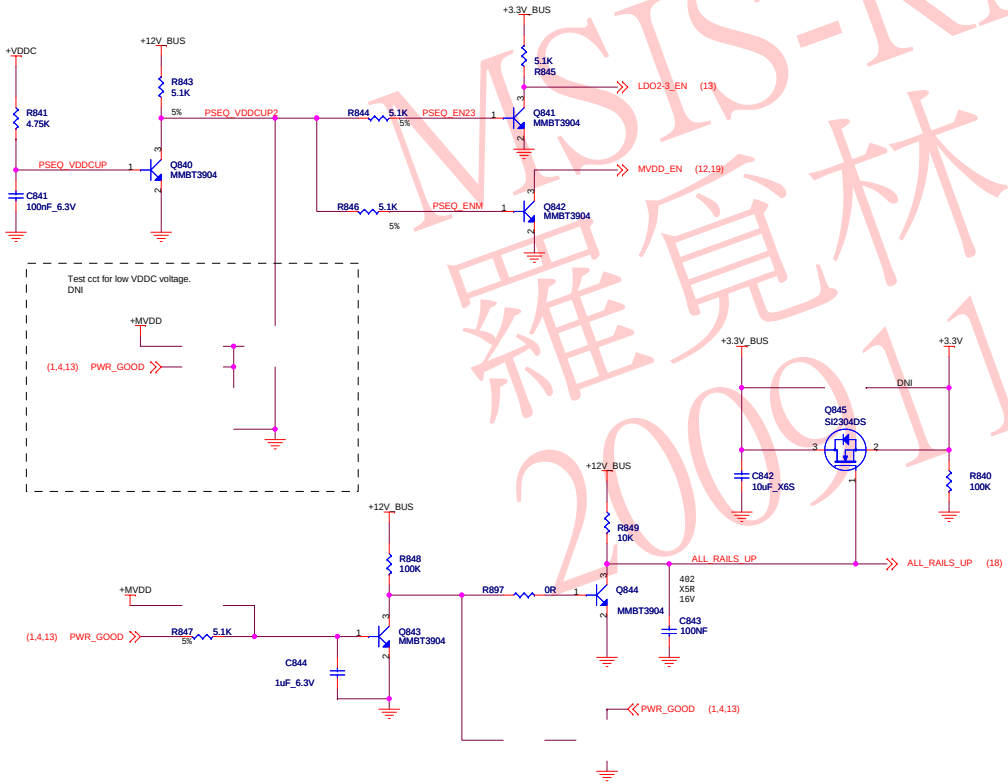
Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

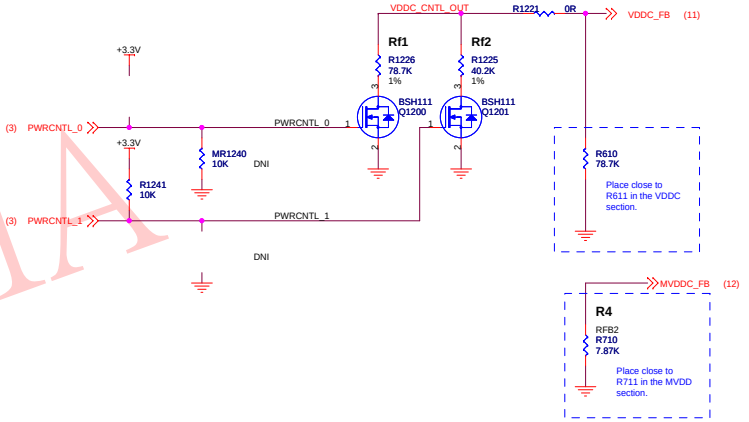
When +12V_BUS ramps above min Vbe, SMPS_EN will be held low



Power Play

VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0	0				
0	1				
1	0				
1	1	1 0	1		Power-up Default



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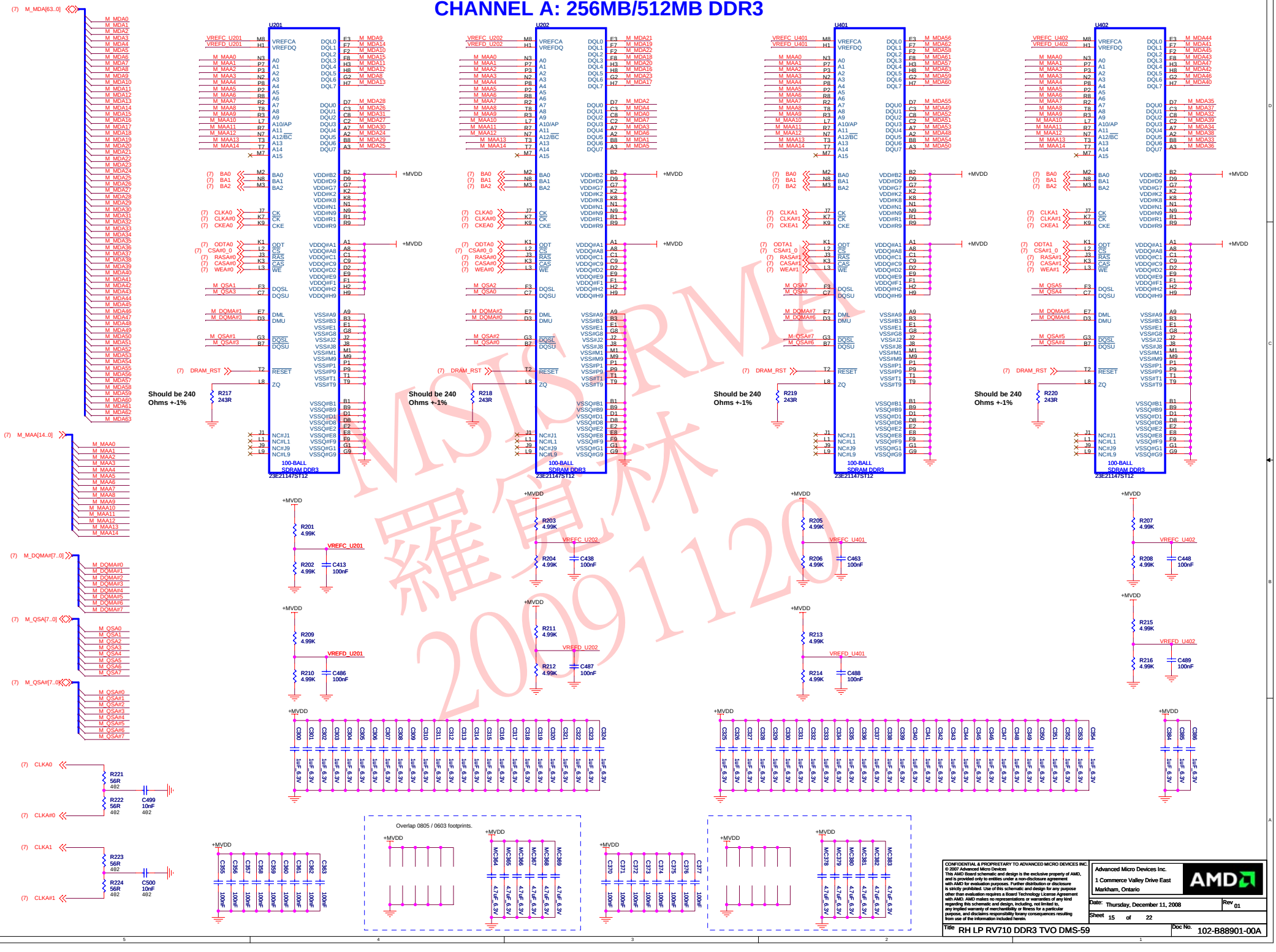
CHANNEL A: 256MB/512MB DDR3



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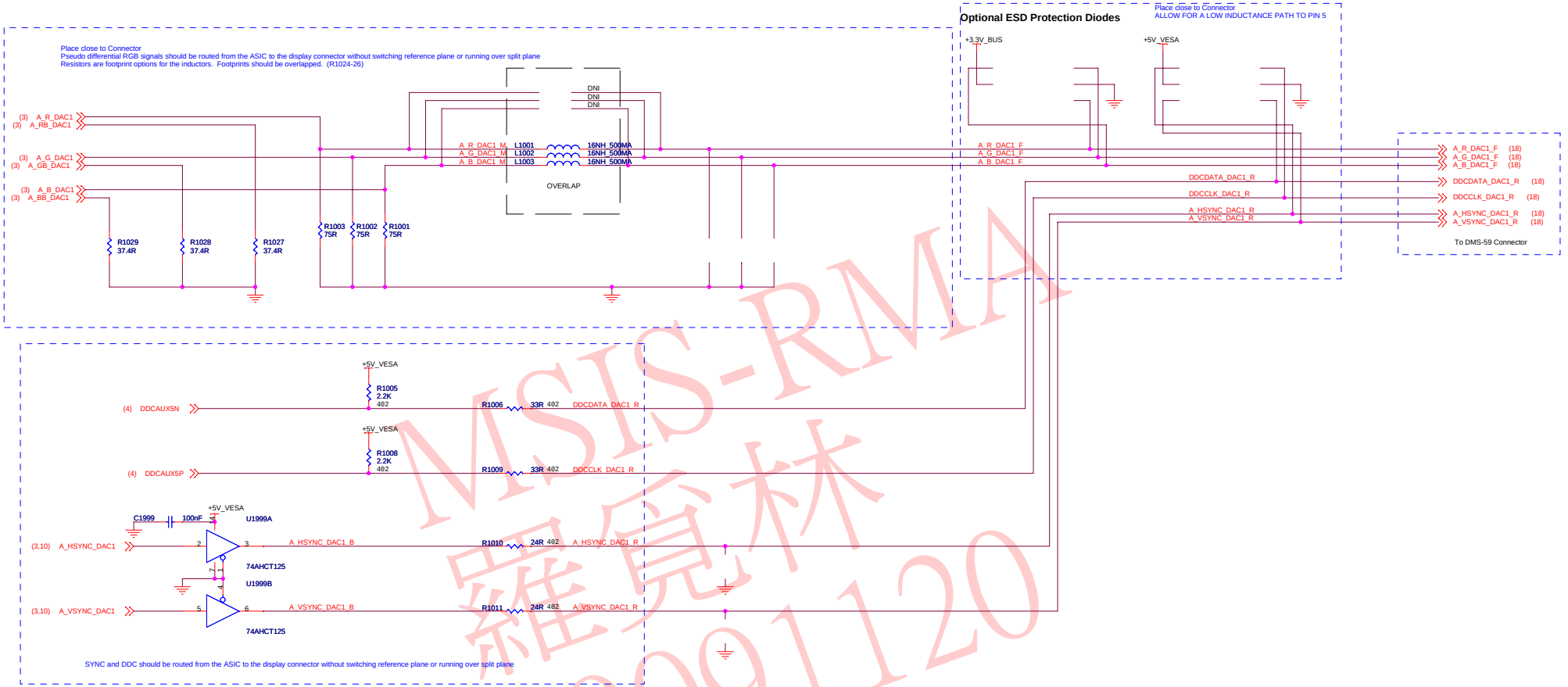
DAC 1 OUTPUT



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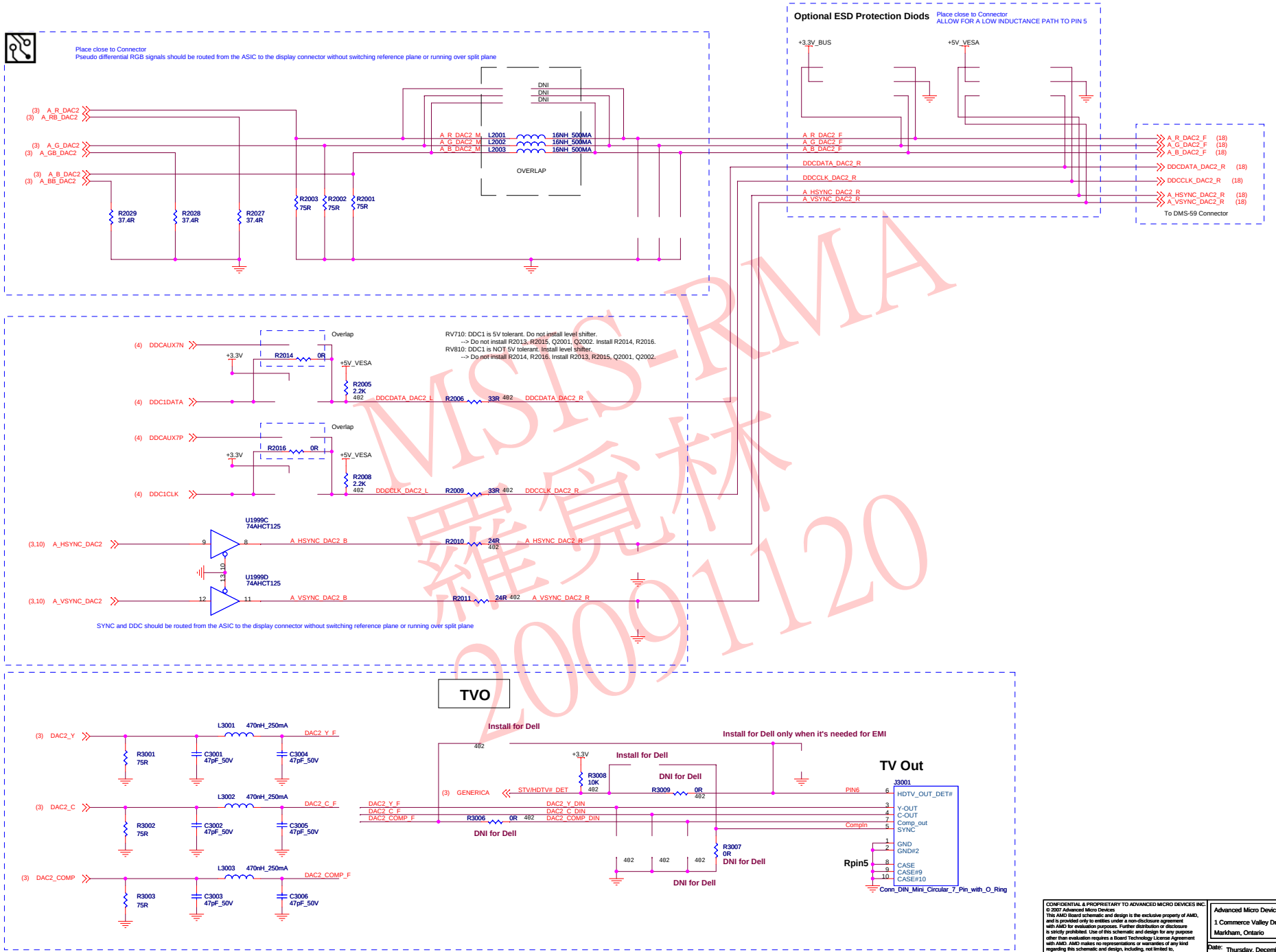
DAC 2 OUTPUT



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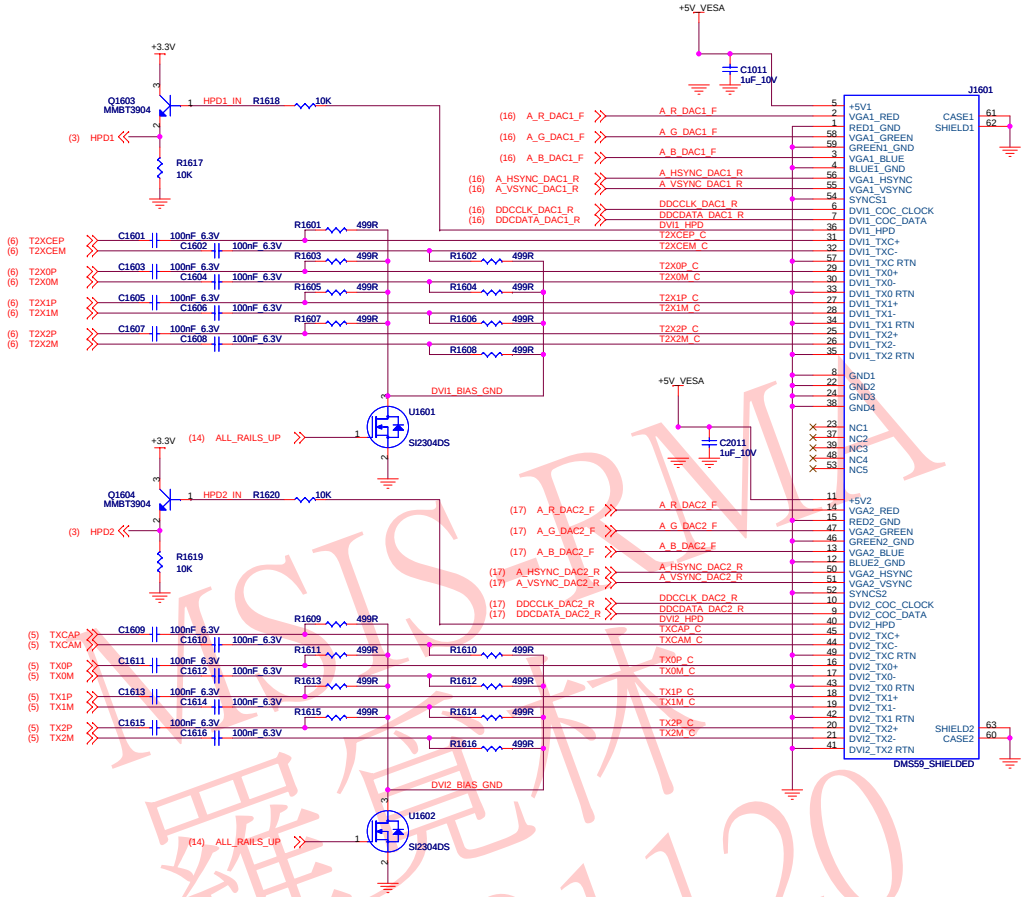
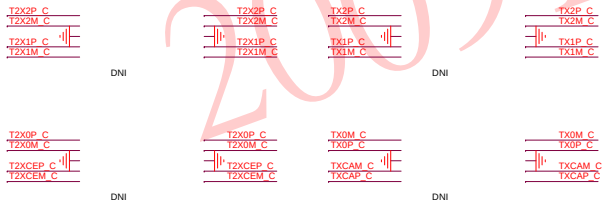
DMS-59 DPB / DPE OUTPUT



Optional ESD protection diodes



Connector 1	
Signals	Mapping
VGA:	DAC1
DVI:	Internal TMDP2
HPD:	HPD1
DDC:	DDC1
5V:	+5V_VESA

Connector 2	
Signals	Mapping
VGA:	DAC2 (TVDAC)
DVI:	Internal LVTMDS1
HPD:	HPD2
DDC:	DDC5
5V:	+5V_VESA

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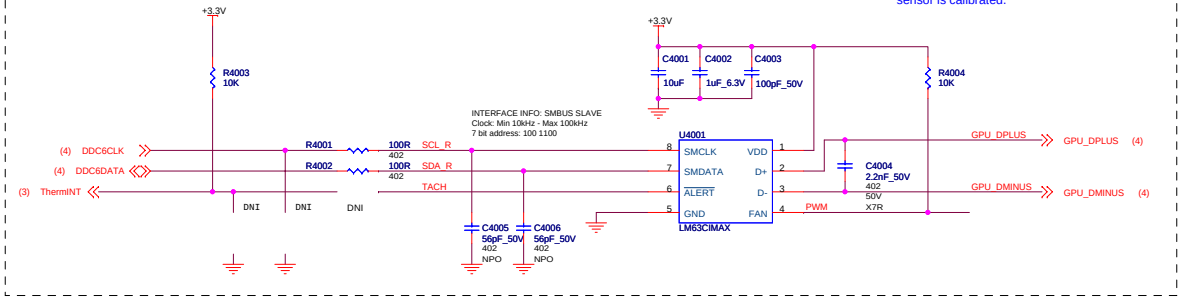
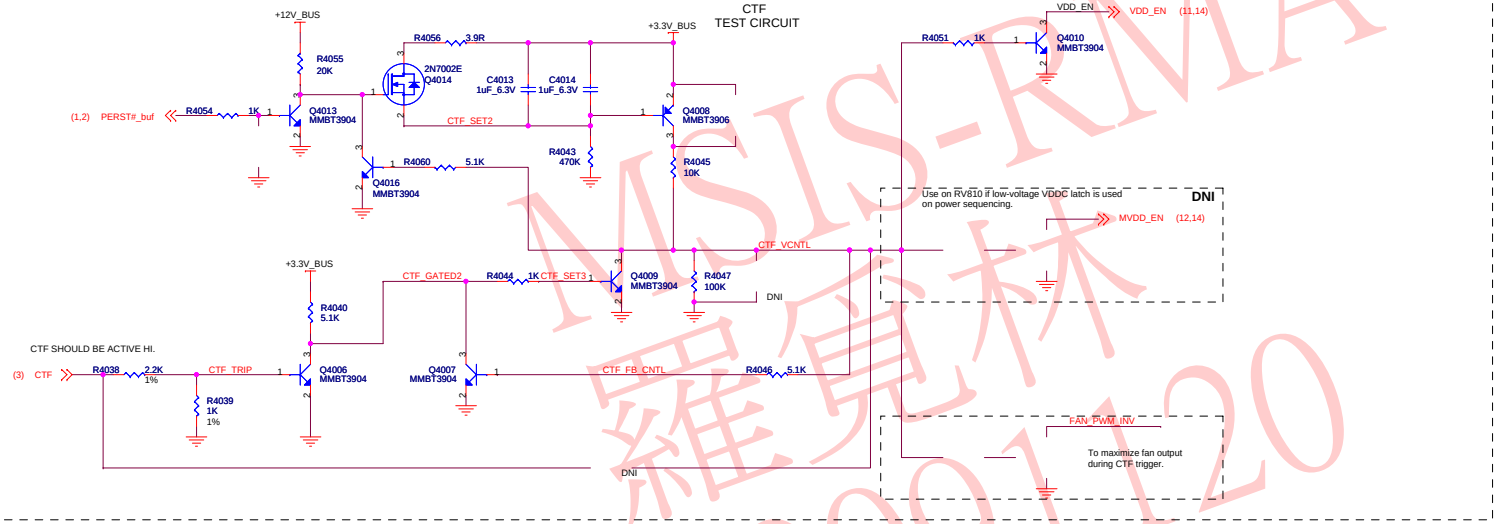
THERMAL MANAGEMENT

Remote Temperature Sensor

Remote diode temp sensor is for RV710 BU, until internal thermal sensor is calibrated.



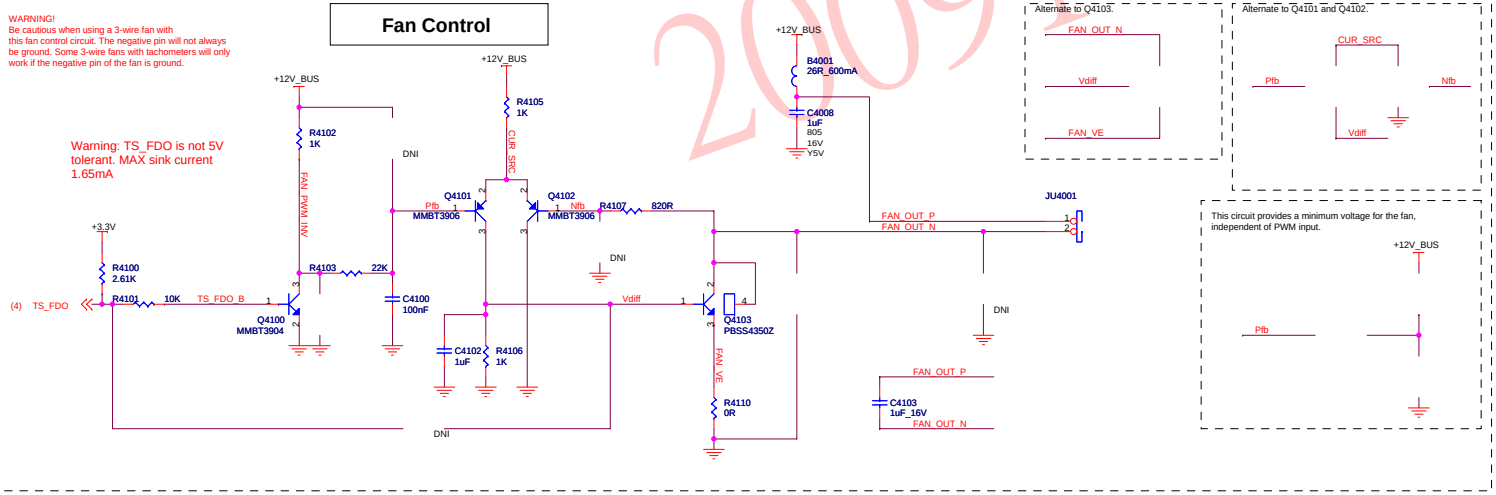
Critial Temperature Fault



Fan Control

WARNING!
Be cautious when using a 3-wire fan with this fan control circuit. The negative pin will not always be ground. Some 3-wire fans with tachometers will only work if the negative pin of the fan is ground.

Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA



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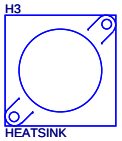

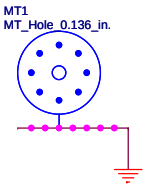

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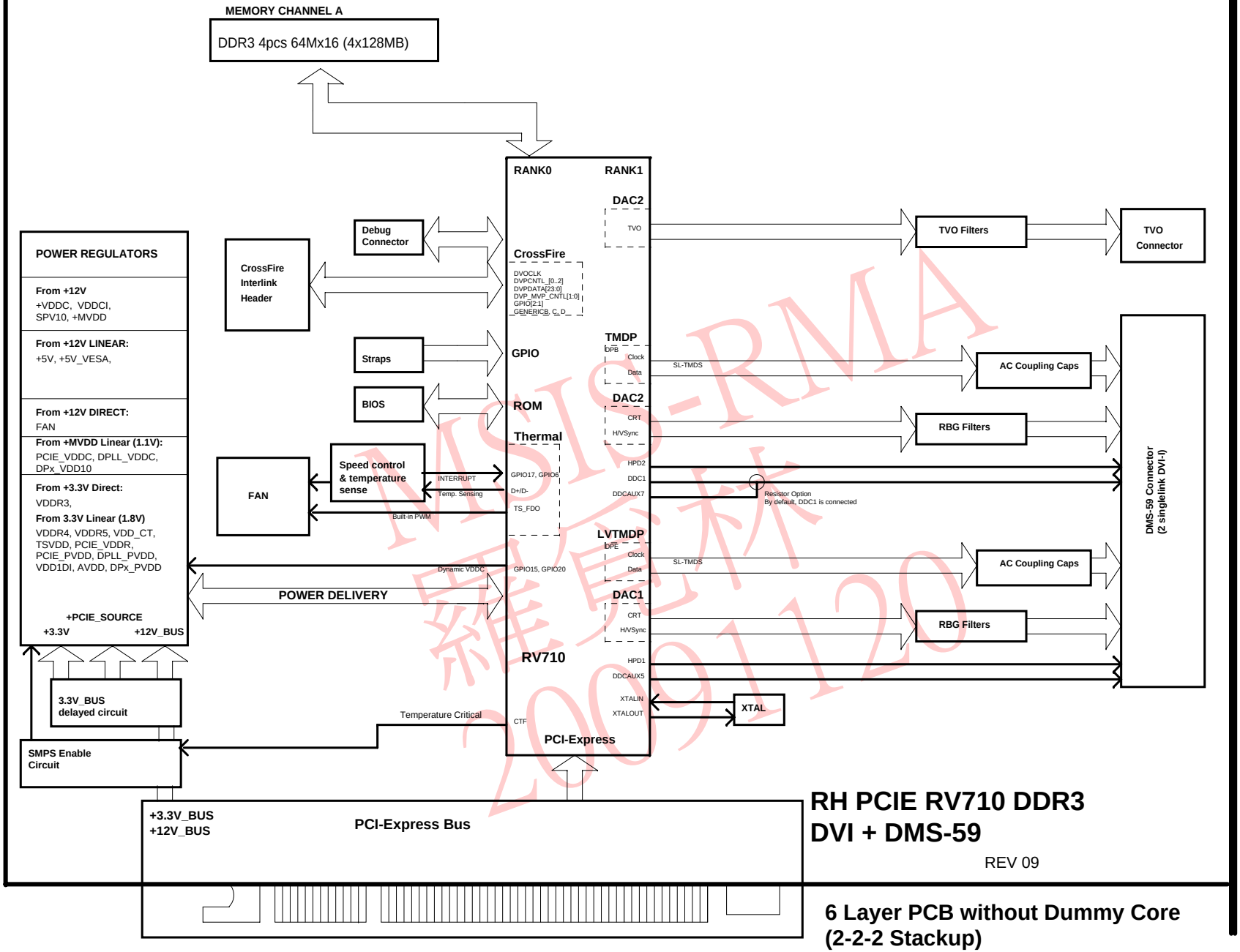

RH PCIE RV710 DDR3 DVI + DMS-59

REV 09

6 Layer PCB without Dummy Core (2-2-2 Stackup)

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Title	Schematic No.	Date:
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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 01

RV710

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
01	00A	2008.11.11	INITIAL RELEASE OF B889 BOARD. BASED ON B754 Rev 90.
02	00A	2008.11.12	ADD R67 AS OPTION TO SHORT JTAG IO
03	00A	2008.11.13	REMOVE MT2
04	00A	2008.11.19	REMOVE MVDD GPIO VOLTAGE CONTROL OPTION
05	00A	2008.11.19	REMOVE LED AND PWR_GOOD CONNECTIONS TO CTF CIRCUIT
06	00A	2008.11.19	REMOVE MC625, PL601, NL601, ML601, R58 AND PROVIDE OPTION TO SHORT CTF TO CTF_VCNTL BY R4062
07	00A	2008.11.24	CHANGE DAC INDUCTORS TO 0603 PART, REMOVE C1001-C1003 and C2001-C2003
08	00A	2008.11.25	REMOVE R26, CHANGE MVDD FET SYMBOL
09	00A	2008.12.01	CHANGE PIN ASSIGNMENT OF D2001 AND REG1603 FOR LAYOUT