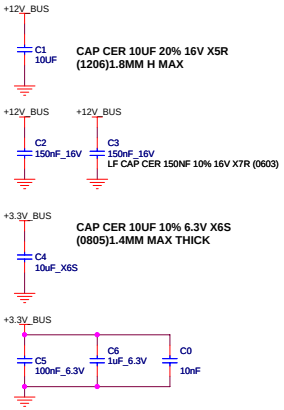
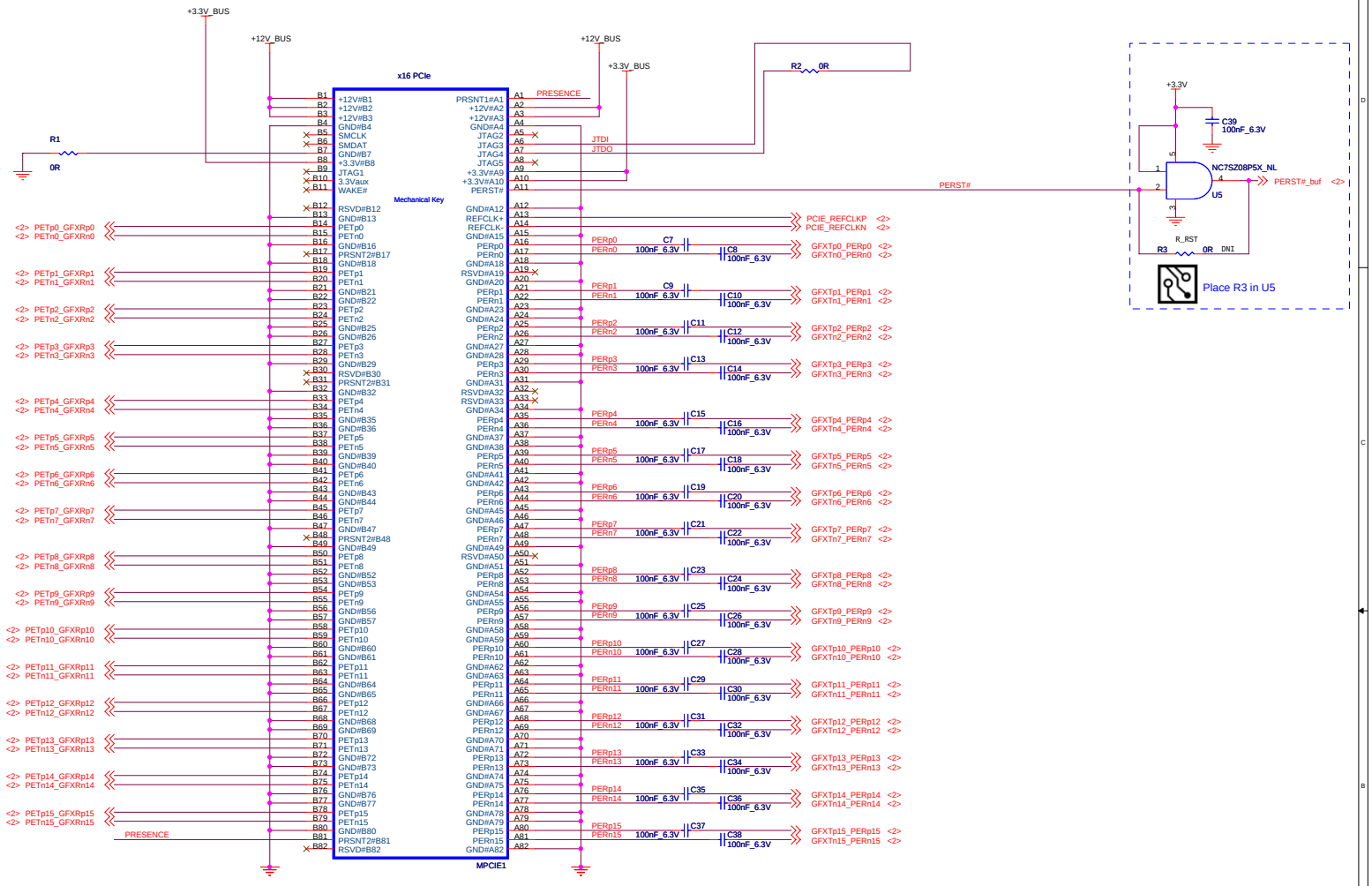
PCI-EXPRESS EDGE CONNECTOR



Place these caps as close to the PCIE connector as possible



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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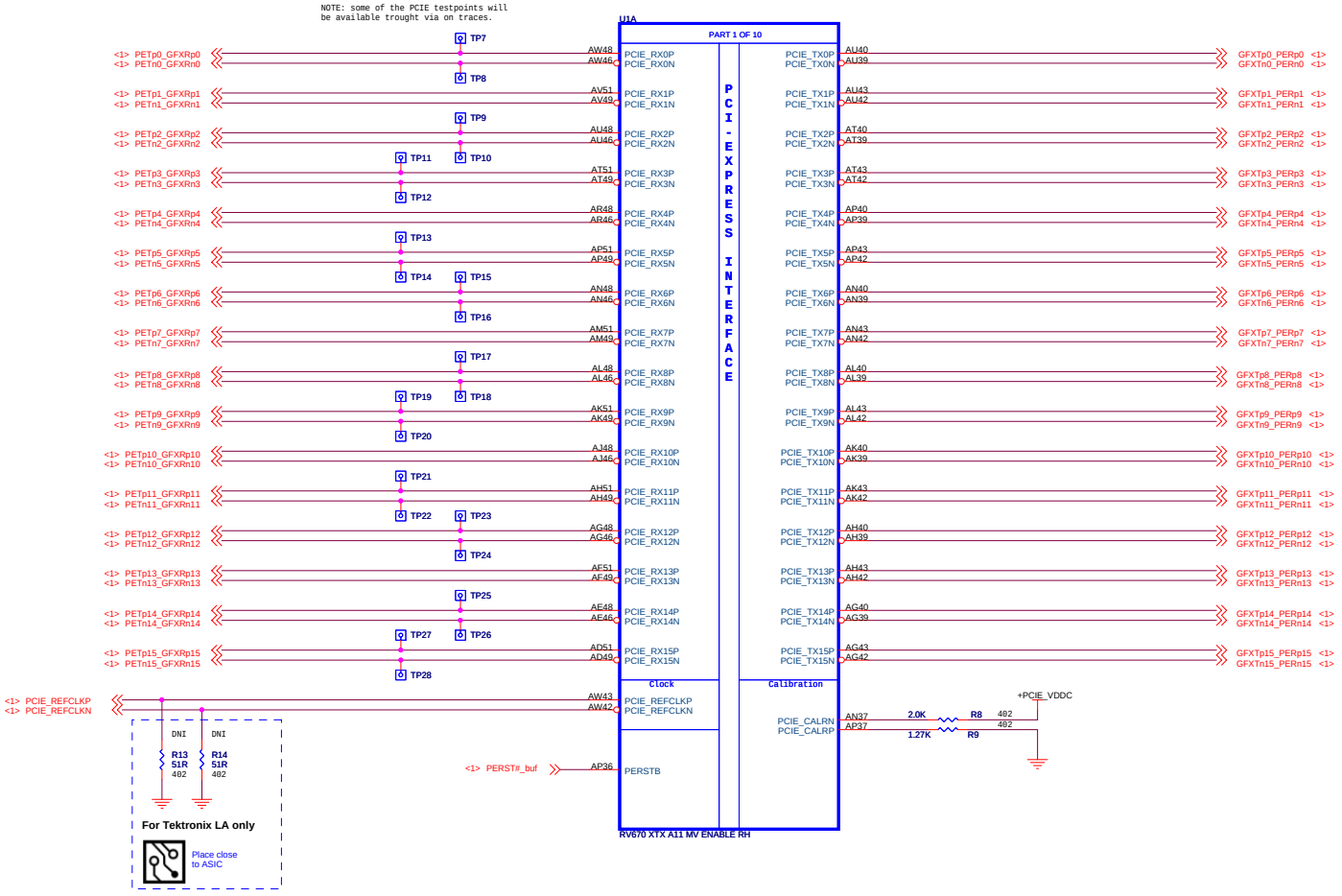
Title	RH RV670 - PCI-E Edge Connector
Doc No.	105-B340xx-00B



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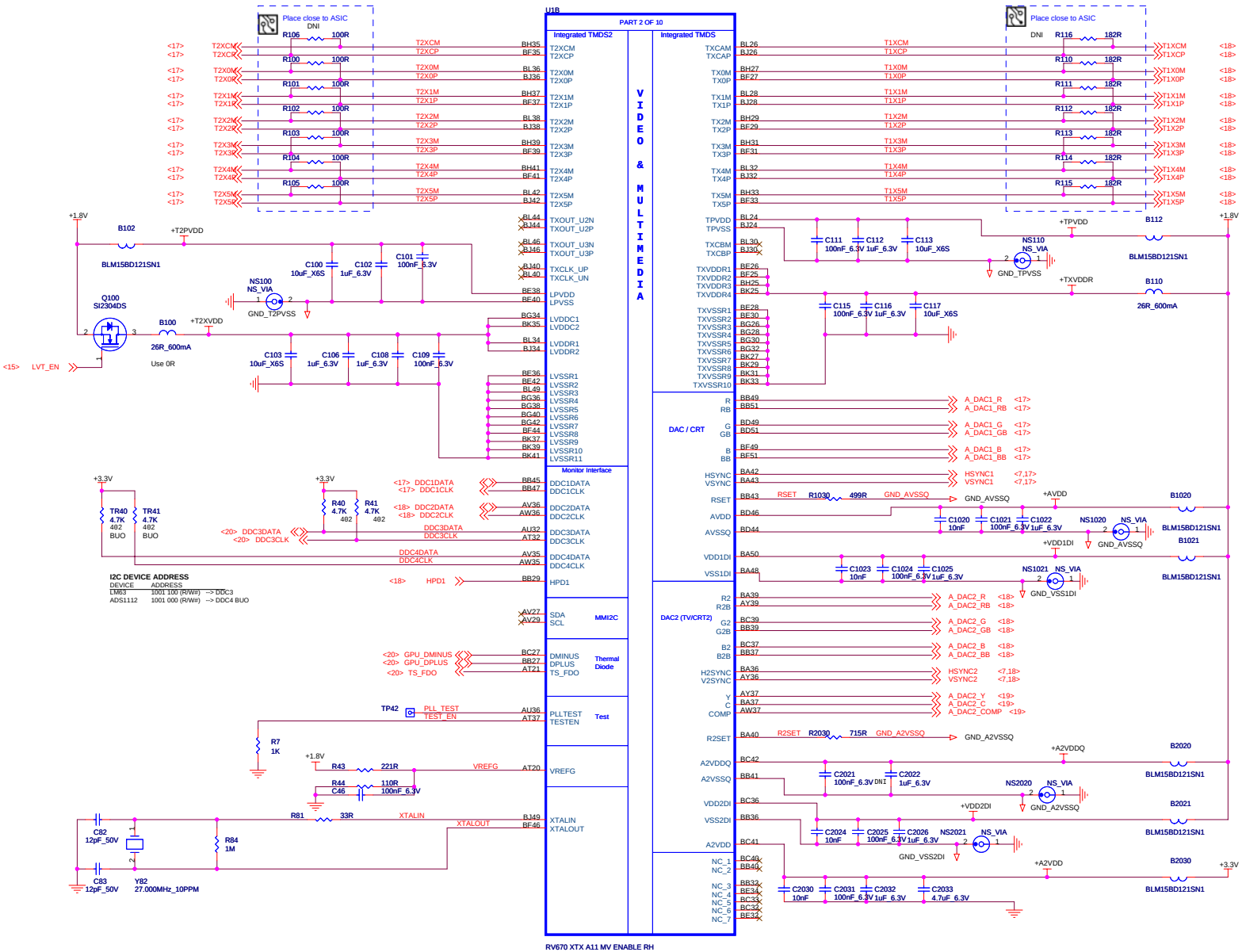
Title RH RV670 - ASIC PCIE_Interface

Doc No. 105-B340xx-00B

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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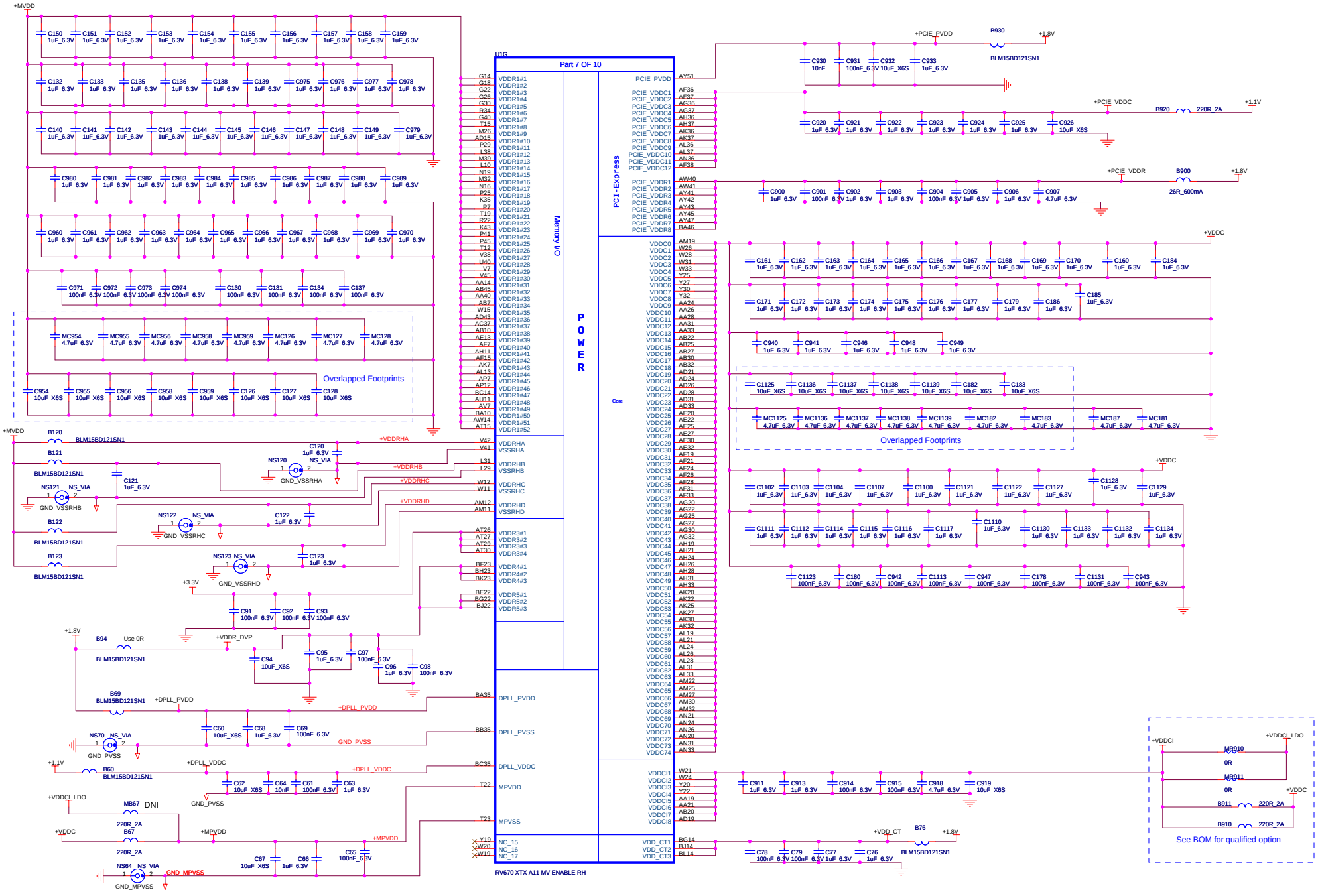
Title	RH RV670 - ASIC MAIN
Doc No.	105-B340xx-00B



Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402

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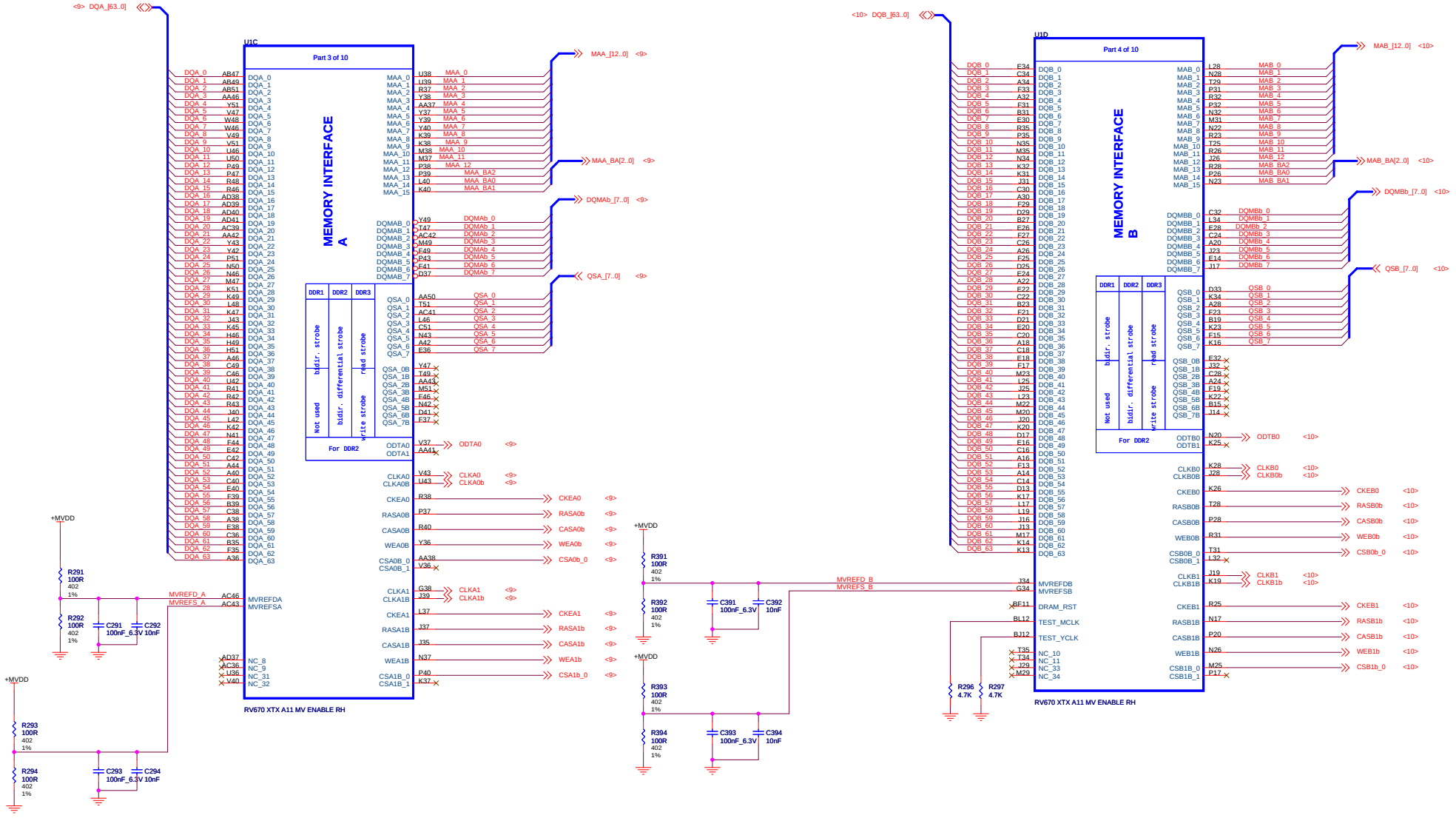
Sheet 4 of 23
Title RH RV670 - ASIC Power
Doc No. 105-B340xx-00B



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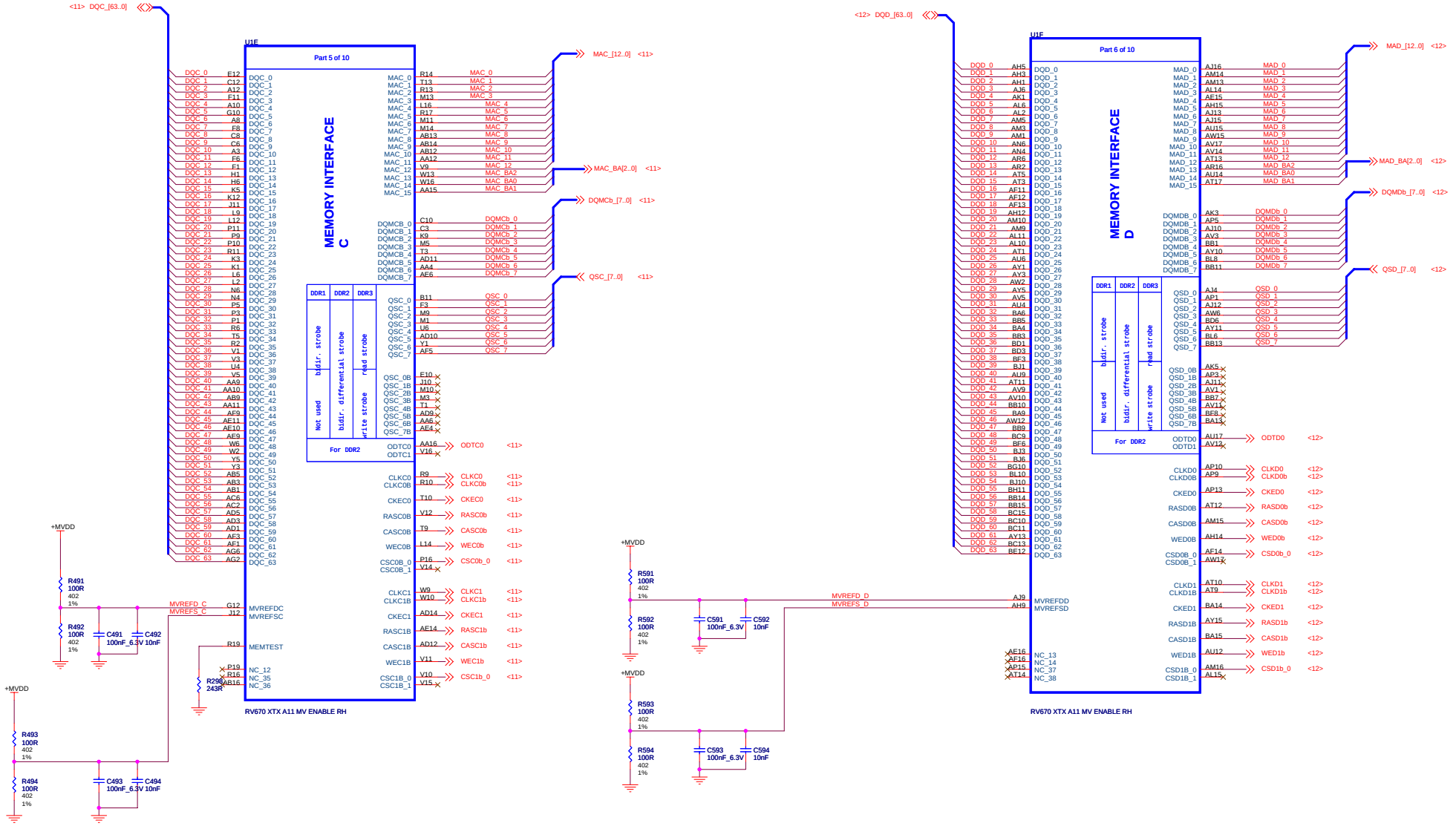
Title	RH RV670 - ASIC Memory Interface (Channel A & B)
Doc No.	105-B340xx-00B



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Title: RH RV670 - ASIC Memory Interface (Channel C & D)
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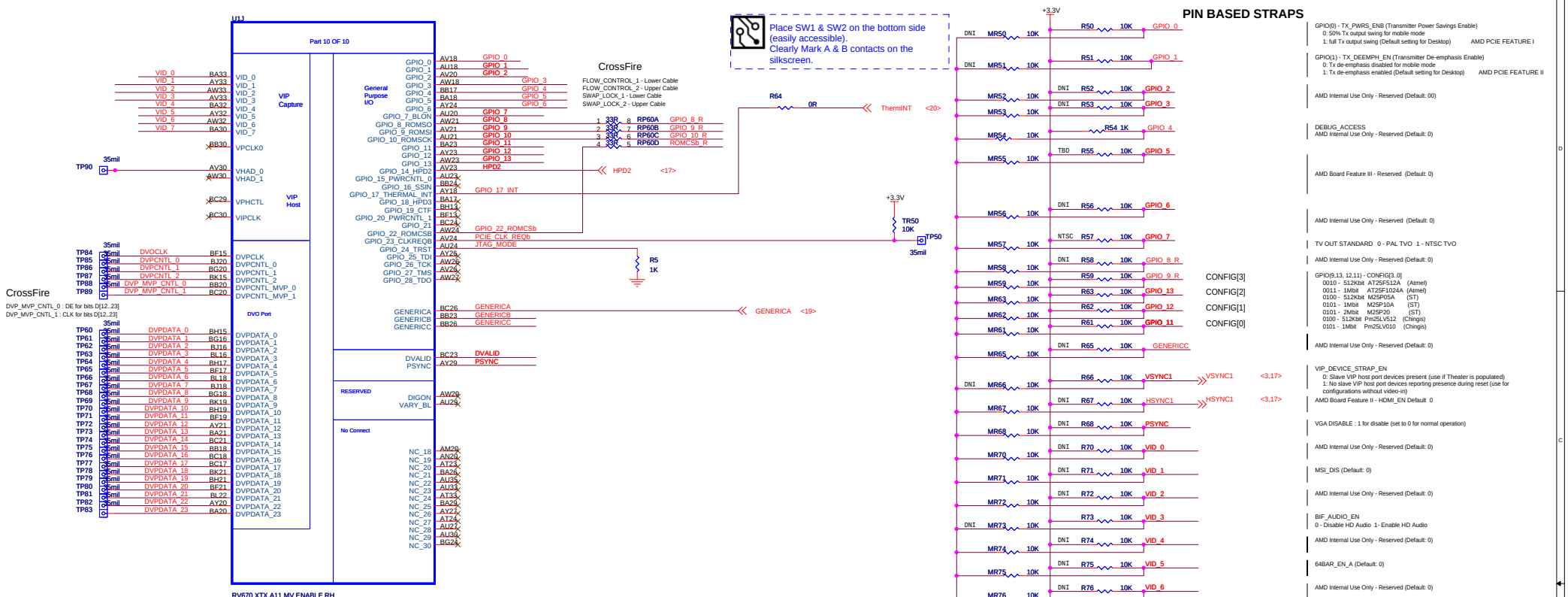
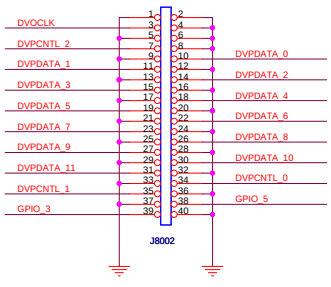
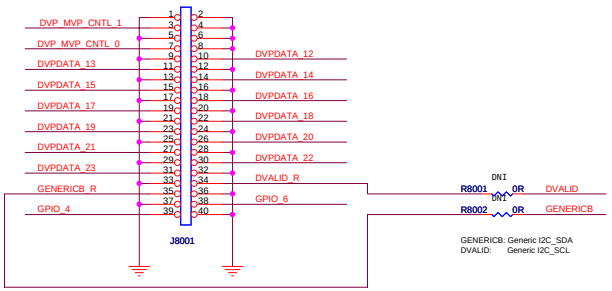


CrossFire Card-Edge

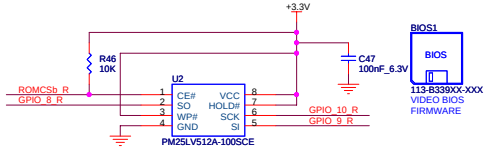
Lower Cable Card Edge



Upper Cable Card Edge



Bundle B **Bundle A (closer to the bracket)**



PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

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Title	RH RV670 - ASIC DVO, VIP & GPIOs
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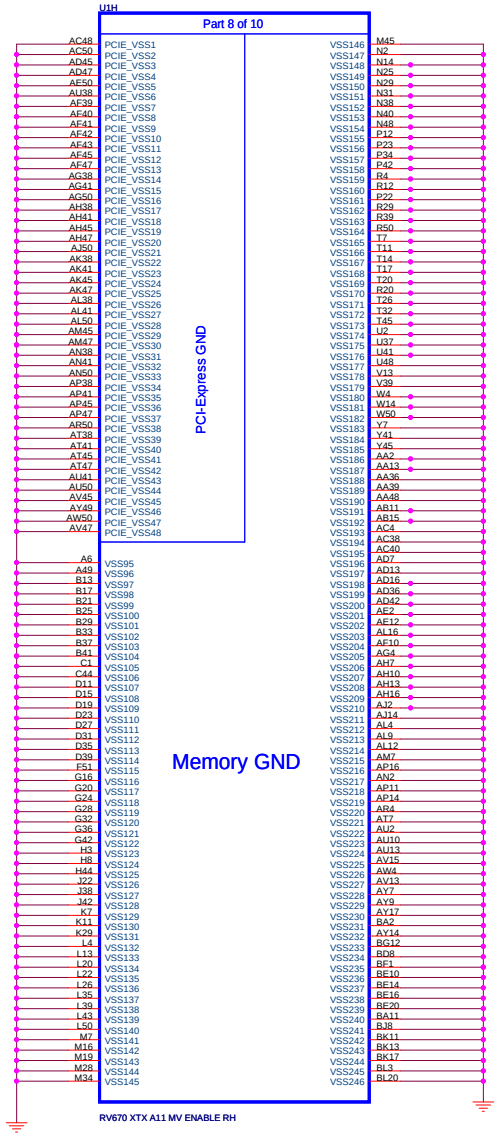

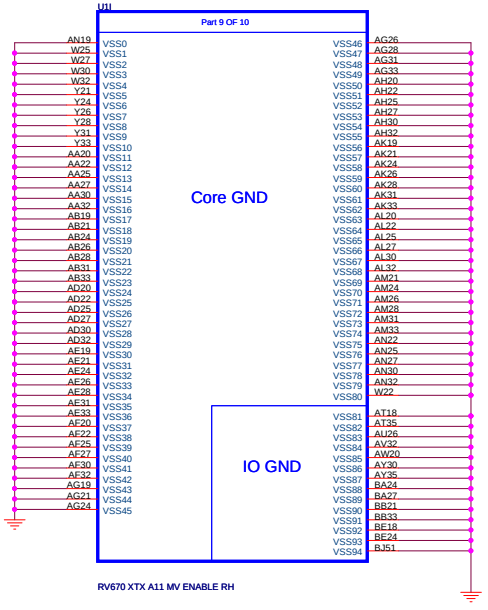

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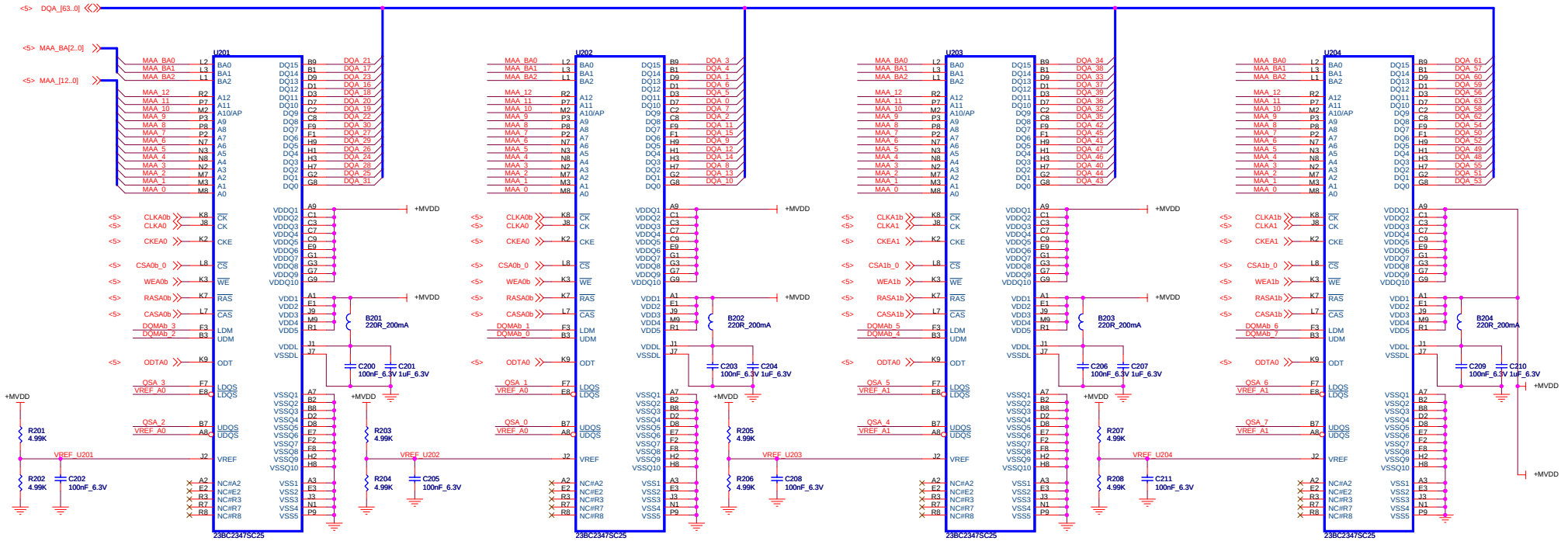
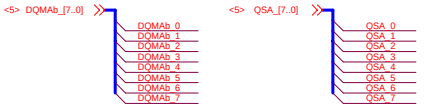
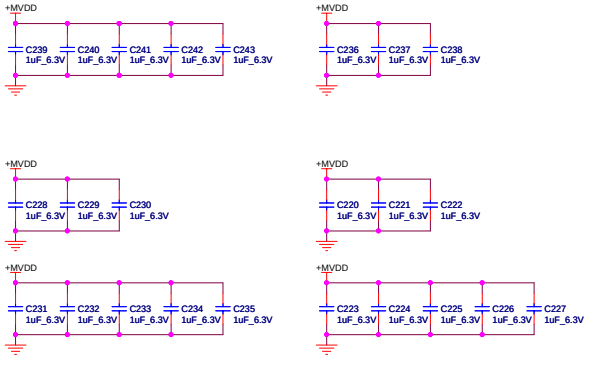
Title RH RV670 - ASIC Grounds

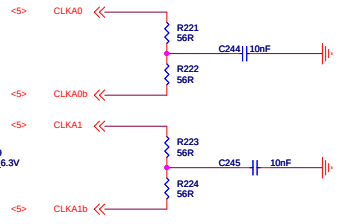
Doc No. 105-B340xx-00B

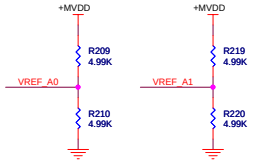
CHANNEL A: 128MB/256MB DDR2











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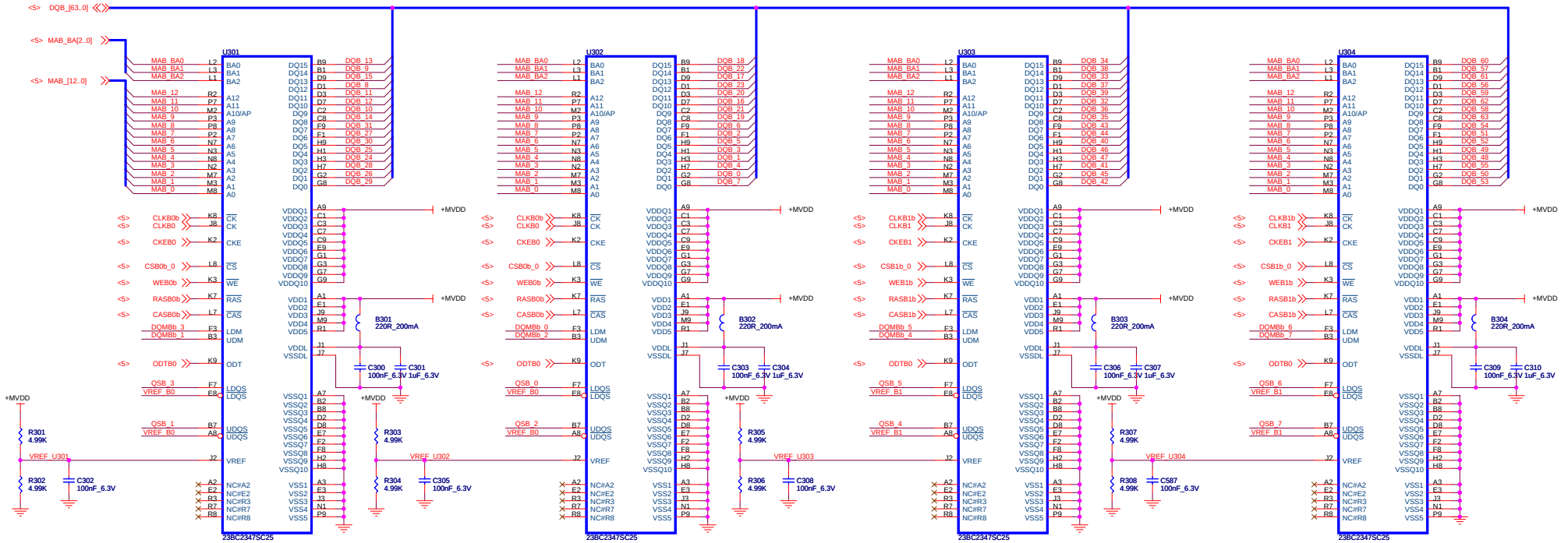
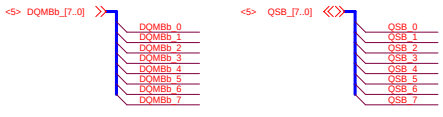
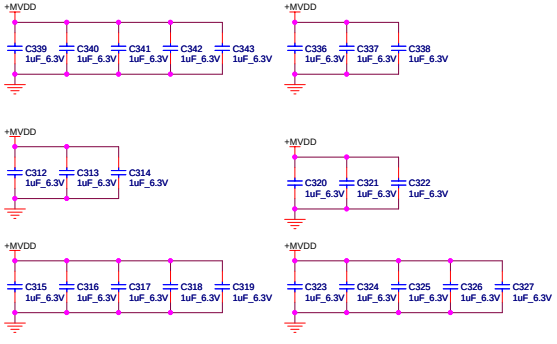
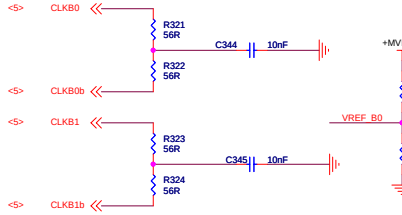
Title	RH RV670 - MEM GDDR3 CH A&B 128-bit 256MB
Doc No.	105-B340xx-00B

CHANNEL B: 128MB/256MB DDR2









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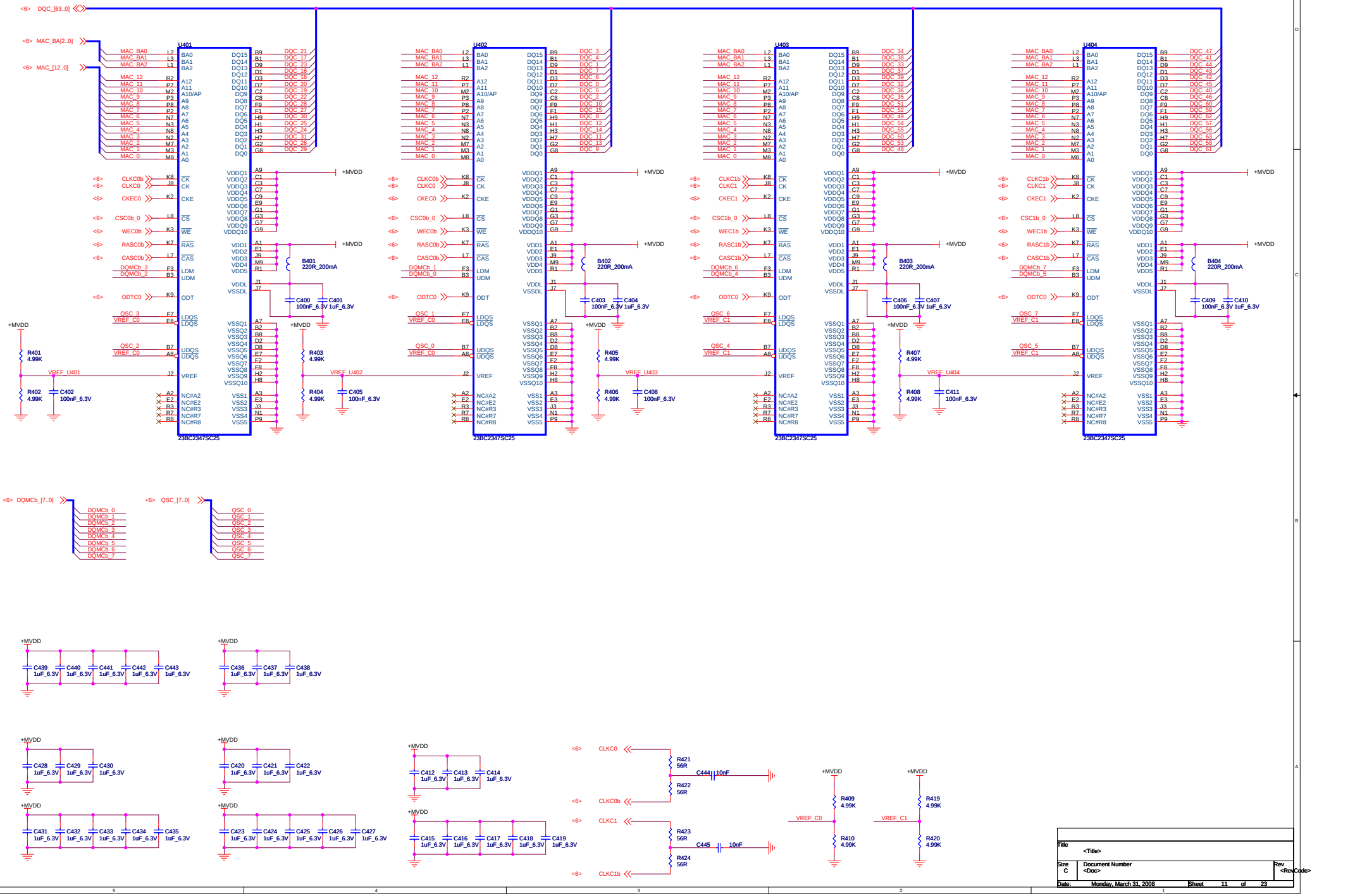
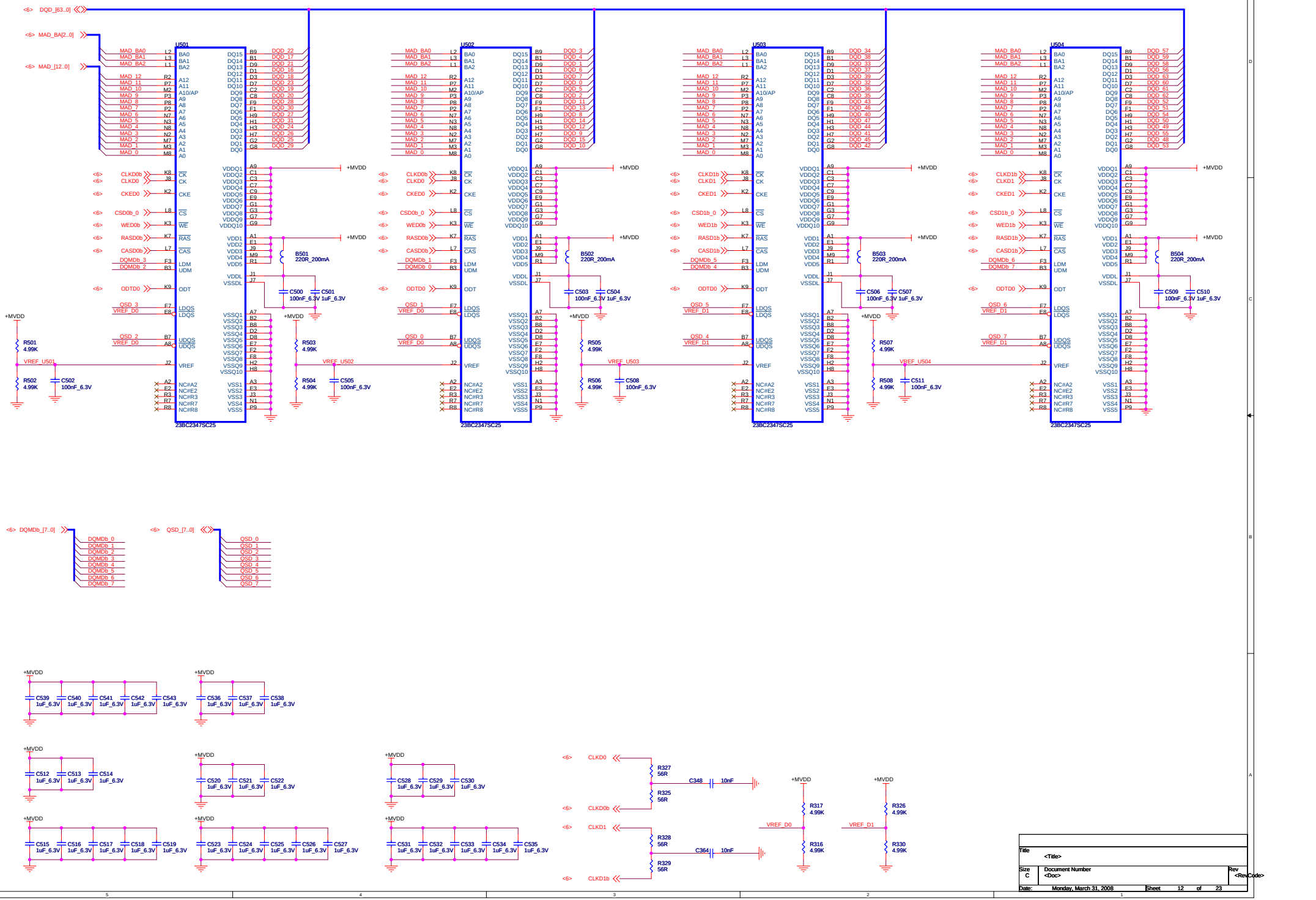
Sheet	10 of 23
Title	RH RV670 - MEM GDDR3 CH C&D 128-bit 256MB
Doc No.	105-B340xx-00B

CHANNEL C: 128MB/256MB DDR2



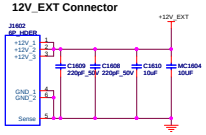
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Monday, March 31, 2008	Sheet 11 of 23	

CHANNEL D: 128MB/256MB DDR2

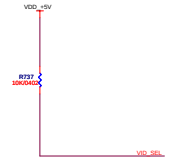


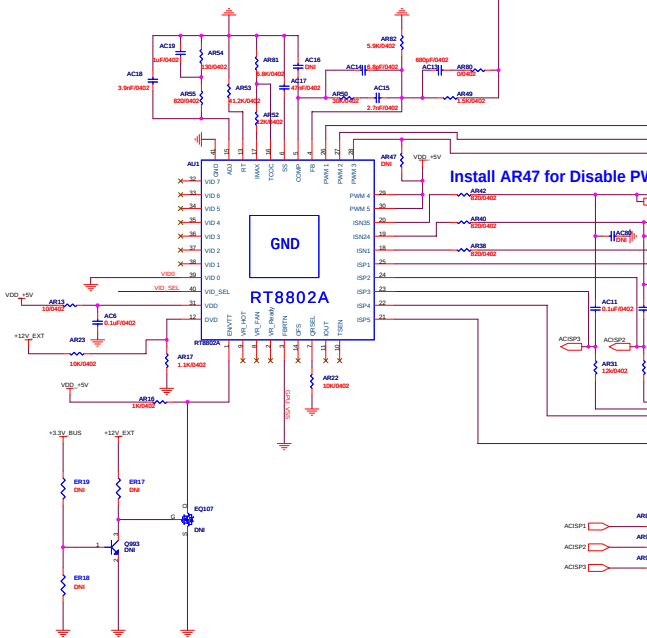
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Monday, March 31, 2008	Sheet 12 of 23	

12V_EXT Connector

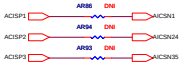


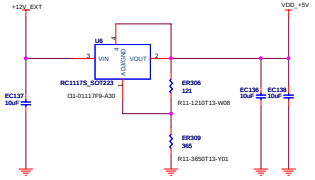
+VDDC=0.8 * (1+ (AR49 / AR82))



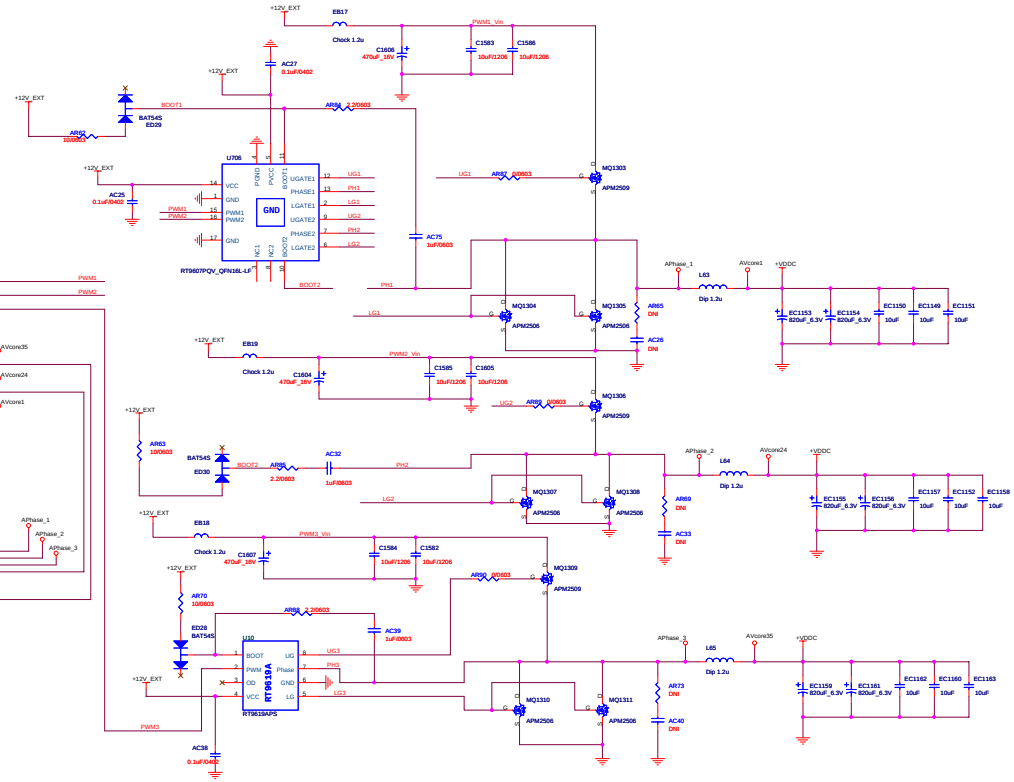


Install AR47 for Disable PWM3 function





Vout=1.25V* [1+(ER305/ER304)]



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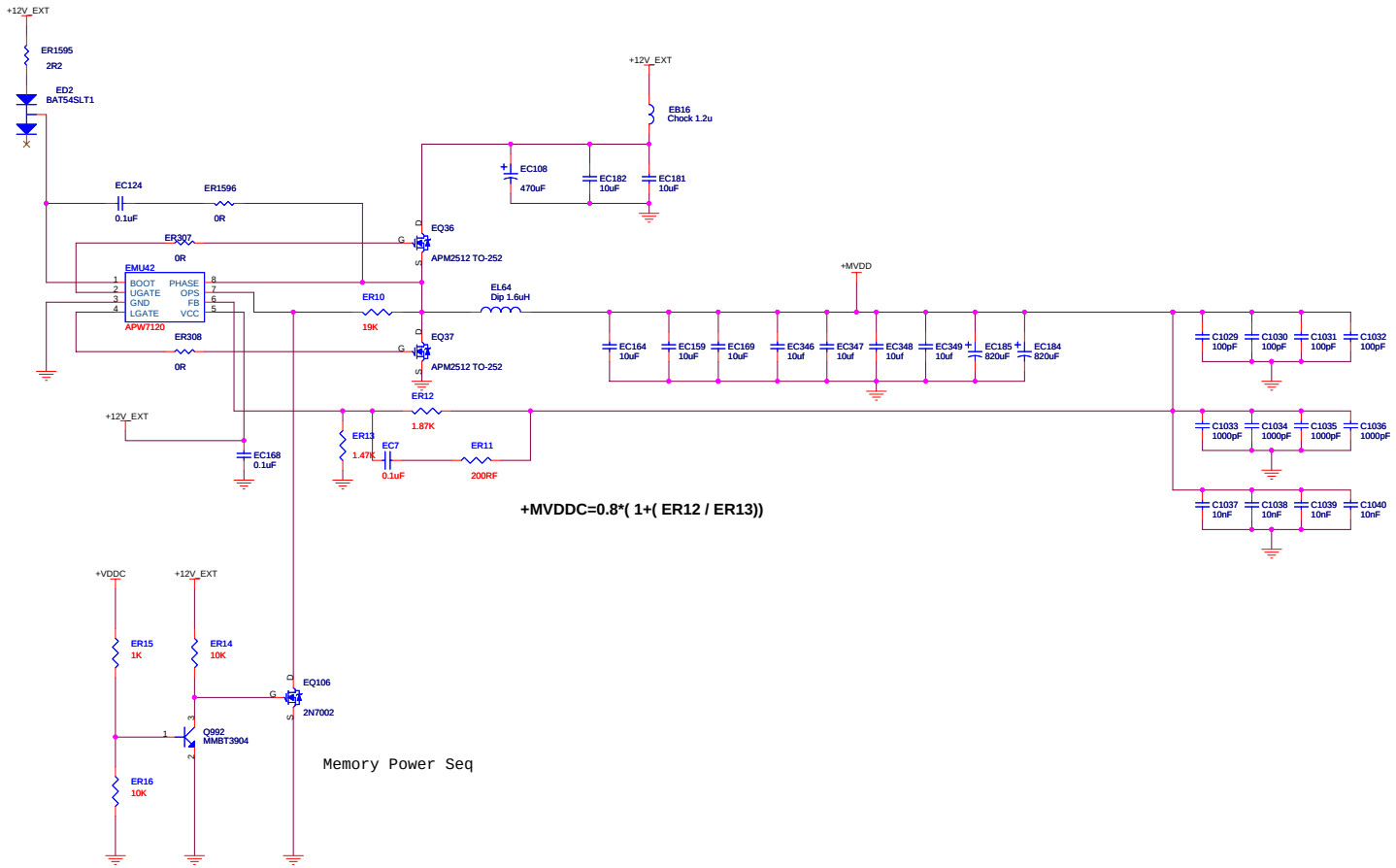
Title: RH RV670 - VDDC SMPS 03
Doc No.: 105-B340xx-008



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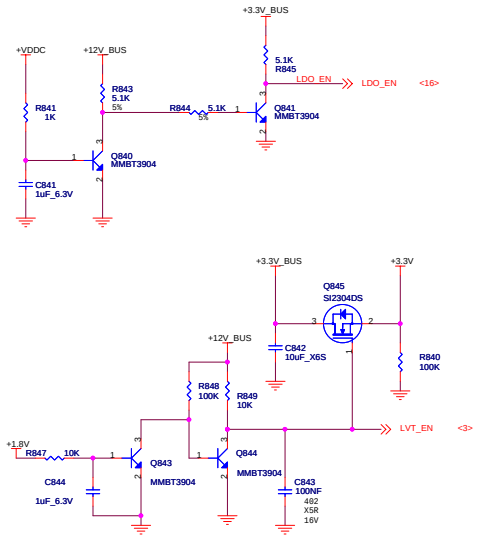
Title RH RV670 - MVDD SMPS 02

Doc No. 105-B340xx-00B

Power up Sequencing



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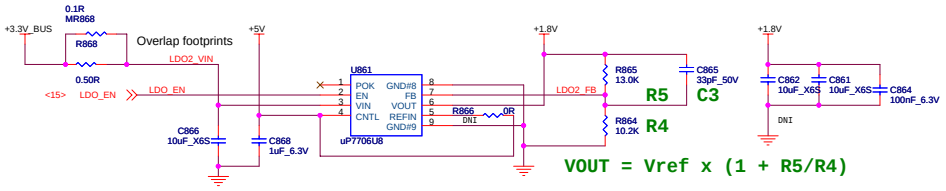
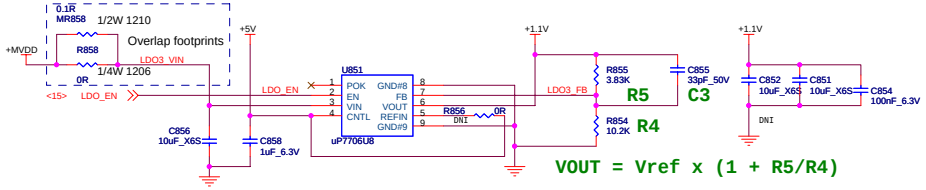
Title RH RV670 - Power Management	Doc No. 105-B340xx-00B

Regulators for +5V, +5V_VESA and +5V_VESA2

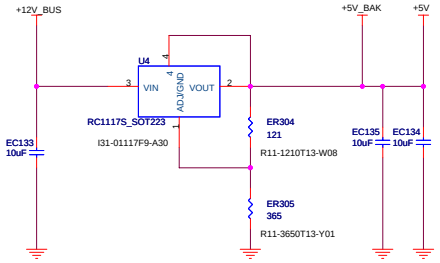
LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #3: Vin = +1.70V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

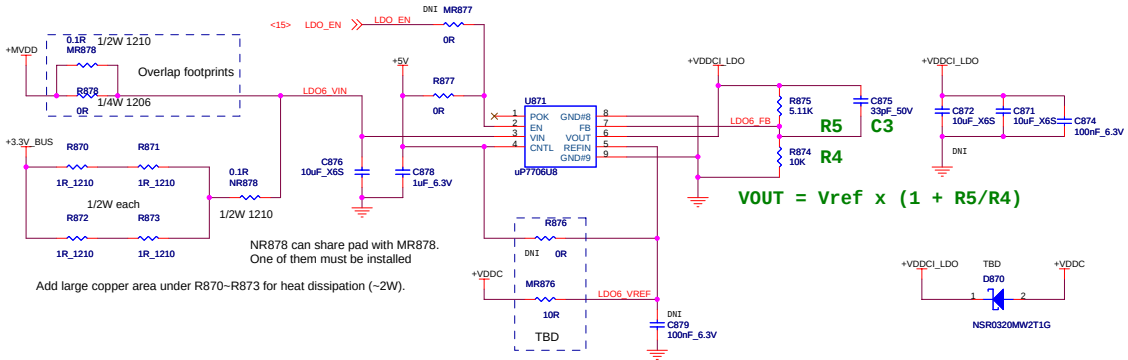


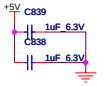
LDO #6: For fixed output voltage: Vin = +1.70V to 2.1V MAX Vout = +1.20V +/- 3% Iout = 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



Vout=1.25V* [1+(ER305/ER304)]

LDO #6: For tracking VDDC: Vin = TBD Vout = TBD Iout = 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling





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Sheet 16 of 23
Title RH RV670 - Linear Regulators
Doc No. 105-B340xx-00B

See BOM for qualified filters

<3> A_DAC1_R
<3> A_DAC1_RB
<3> A_DAC1_G
<3> A_DAC1_GB
<3> A_DAC1_B
<3> A_DAC1_BB

R1027 37.4R
R1028 37.4R
R1029 37.4R

R1001 75R 402
R1002 75R 402
R1003 75R 402

C1004 8.0pF 402
C1005 8.0pF 402
C1006 8.0pF 402

L1001 47nH
ML1001 36NH
C1001 12pF_50V 402

L1002 47nH
ML1002 36NH
C1002 12pF_50V 402

L1003 47nH
ML1003 36NH
C1003 12pF_50V 402

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

L100x and ML100x footprints are overlapped

For ESD Protection

D1001 CM1213-04
D1002 CM1213-04

+3.3V
+5V_VESA
+5V_VESA2
+5V
EF1 0.2A

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

C1010 104pF

MJ1001 G3179C219-005
R
G
B
MS0
MS1
MS2
MS3
NC
HS
VS
VSS
VSS#6
VSS#7
VSS#8
VSS#10
CASE
CASE#17

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

<3> DDC1DATA
<3> DDC1CLK

R1004 10K
R1007 10K
R1005 2.2K
R1008 2.2K

Q1001 BSH111
Q1002 BSH111

DDCDATA_DAC1_5V
DDCCLK_DAC1_5V

R1006 33R 402 DDCDATA_DAC1_R
R1009 33R 402 DDCCLK_DAC1_R

100nF_6.3V C1999

<3,7> HSYNC1
<3,7> VSYNC1

U1999A SN74HCT125D
U1999B SN74HCT125D

HSYNC_DAC1_B
VSYNC_DAC1_B

R1010 10R 402 HSYNC_DAC1_R
R1011 10R 402 VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

Q1021 MMBT3904
R1022 10K
R1023 10K
HPD_DVI2
<7> HPD2

J1001 DVI_CONNECTOR

<3> T2X2M	1	TMDS Data2-
<3> T2X2P	2	TMDS Data2+
	3	TMDS Data2/4 Shield
<3> T2X4M	4	TMDS Data4-
<3> T2X4P	5	TMDS Data4+
DDCCLK_DAC1_R	6	DDC Clock
DDCDATA_DAC1_R	7	DDC Data
VSYNC_DAC1_R	8	Analog VSYNC
<3> T2X1M	9	TMDS Data1-
<3> T2X1P	10	TMDS Data1+
	11	TMDS Data1/3 Shield
<3> T2X3M	12	TMDS Data3-
<3> T2X3P	13	TMDS Data3+
	14	+5V Power
	15	GND (for +5V)
	16	Hot Plug Detect
<3> T2X0M	17	TMDS Data0-
<3> T2X0P	18	TMDS Data0+
	19	TMDS Data0/5 Shield
<3> T2X5M	20	TMDS Data5-
<3> T2X5P	21	TMDS Data5+
	22	TMDS Clock Shield
<3> T2XCP	23	TMDS Clock+
<3> T2XCM	24	TMDS Clock-
A_R_DAC1_F	C1	Analog Red
A_G_DAC1_F	C2	Analog Green
A_B_DAC1_F	C3	Analog Blue
HSYNC_DAC1_R	C4	Analog HYNC
	C5	Analog GND
	C6	Analog GND#C6
	26	CASE#26
	27	CASE#27
	28	CASE#28
	29	CASE#29
	30	CASE#30
	25	CASE

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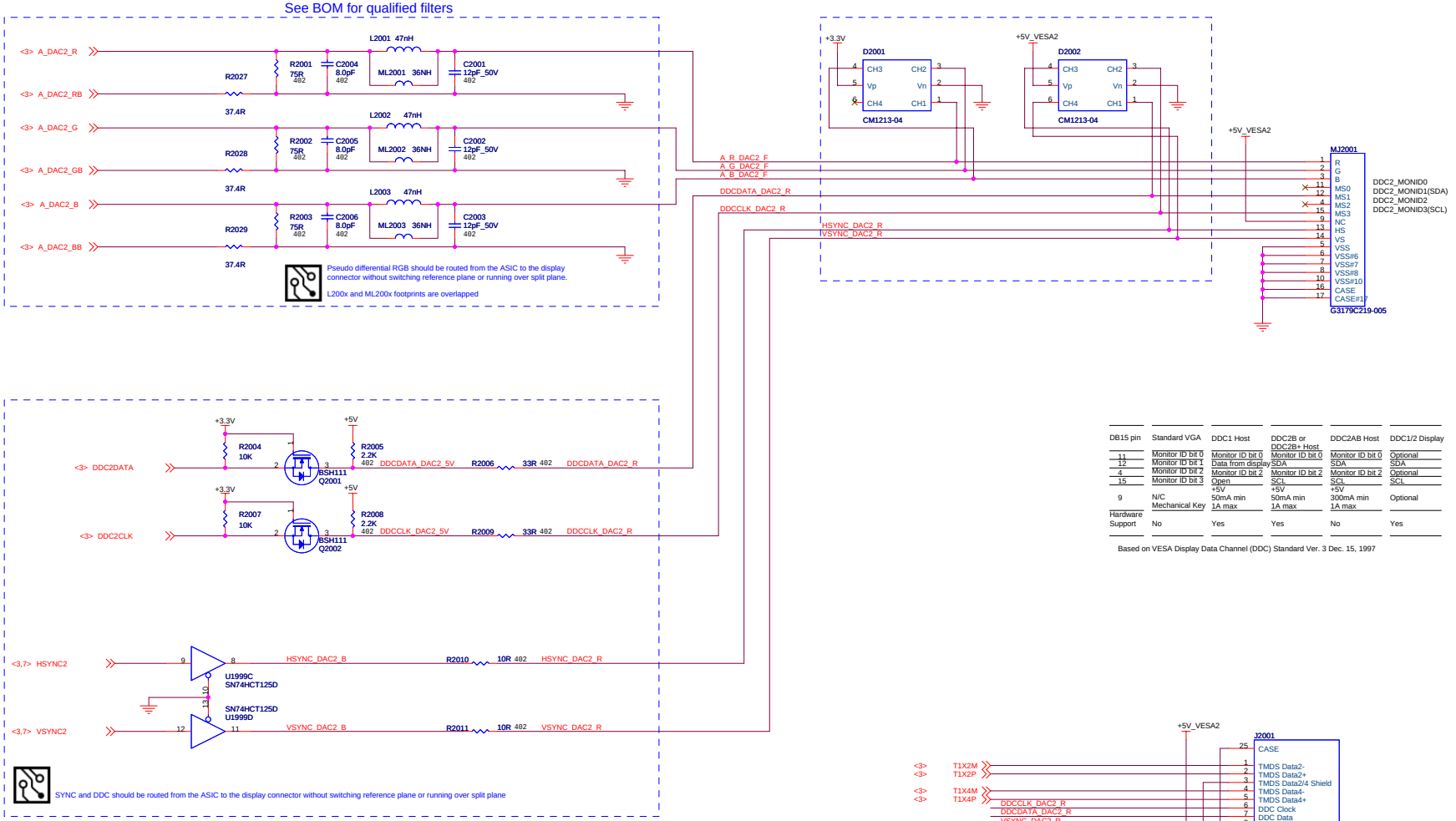
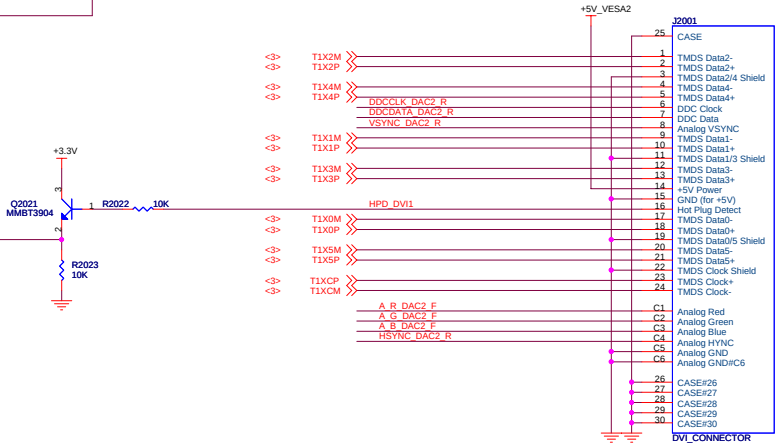
See BOM for qualified filters



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



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Title RH RV670 - DAC2/TMDS1

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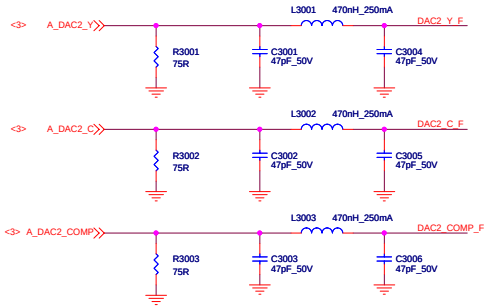

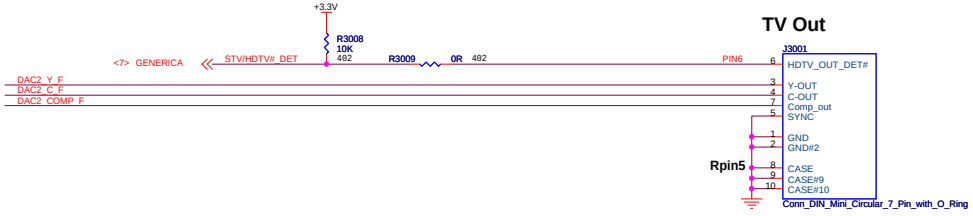

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Title RH RV670 - TV OUT

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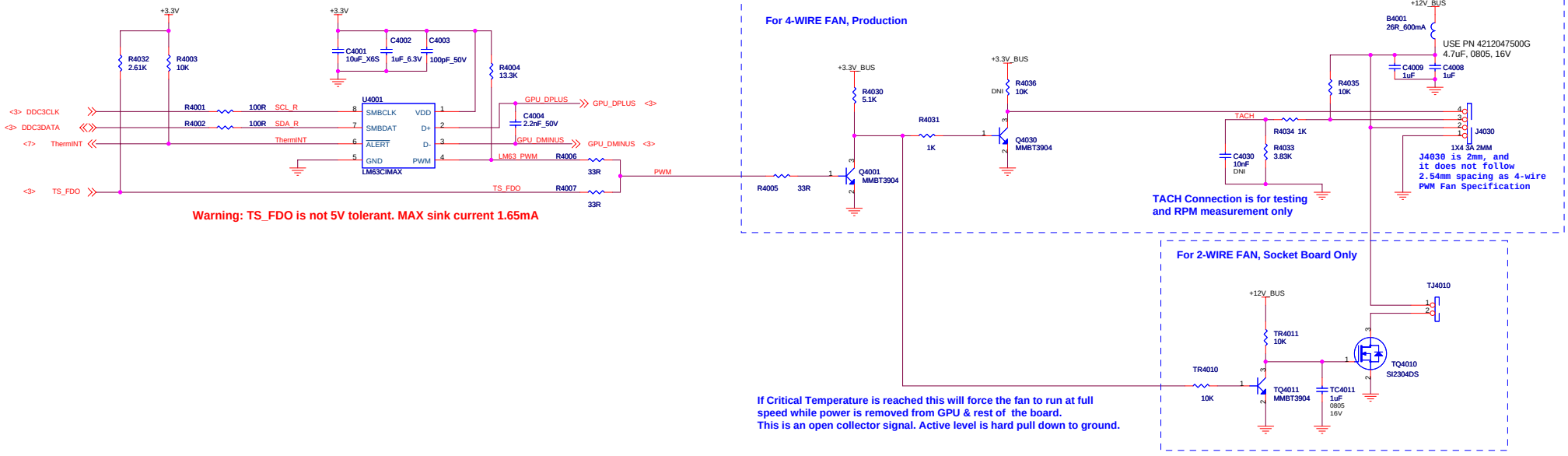

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Title RH RV670 - Thermal Management

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ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

MT1
MT_Hole_0.136 TM 5.5 BM 7.0

SK1
Socket_RV670/M88L

PCB1
PCB
109-B34031-00B

ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET
8020038600G

ASSY-SCREW5
SCREW
SCREW

BKT2
BRACKET
80200386B0G

BKT1: DVI - DIN -DVI
BKT2: DVI - DVI
ASSY-SCREW5 only for Slim-VGA with upper or lower tab bracket

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM4 SW_FB
FM5 SW_FB
FM6 SW_FB

J7 3 1 4 2 impedence
J4 3 1 4 2 impedence
J2 3 1 4 2 impedence
J1 3 1 4 2 impedence

J3 X_PIN1*2
J6 X_PIN1*2
J9 X_PIN1*2
J11 X_PIN1*2

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<variant_name>

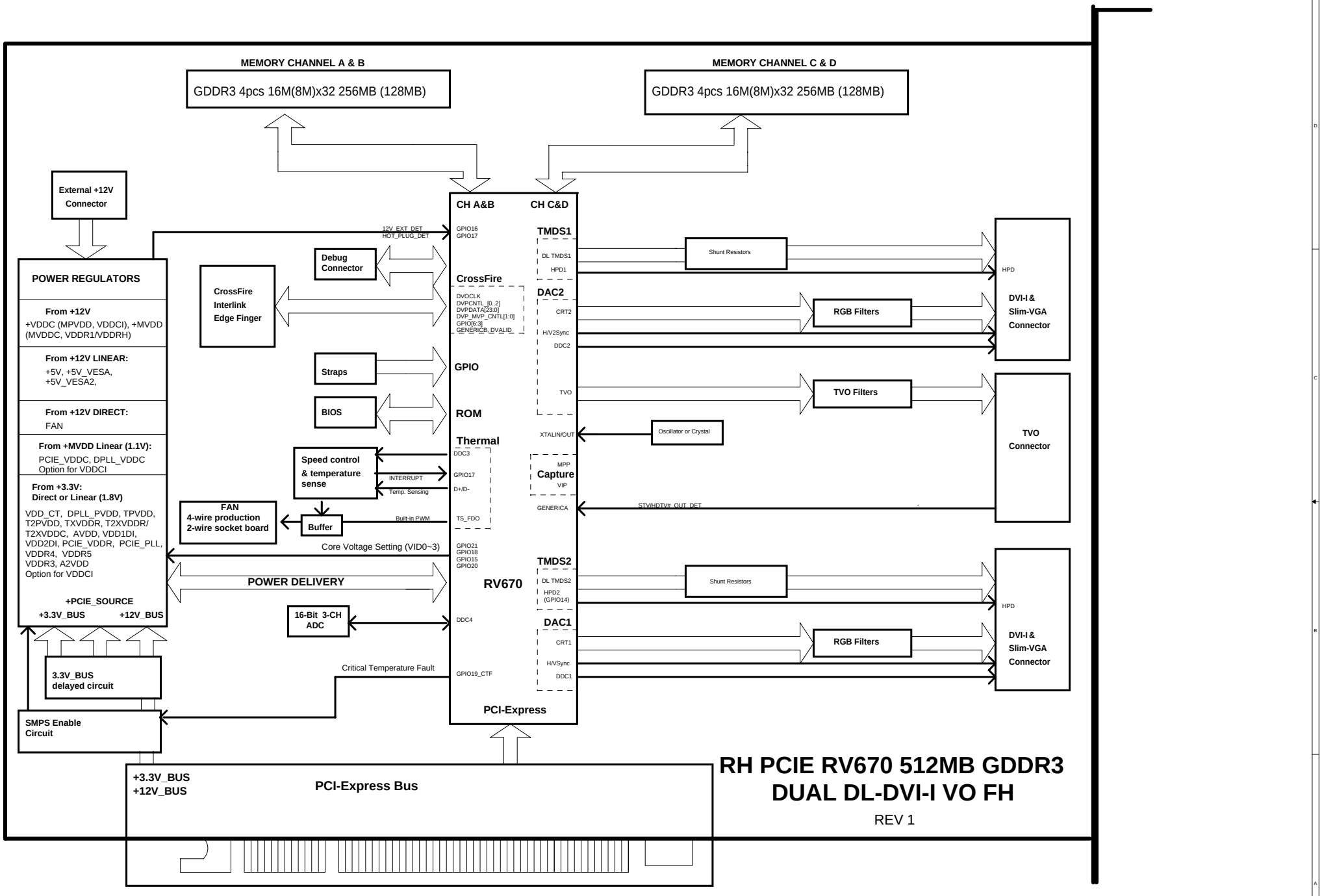
Title	Schematic No.	Date:
RH PCIE RV670 512MB GDDR3 DUAL DL-DVI-I VO FH	105-B340xx-00B	Thursday, March 13, 2008

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/05/11	Initial design for RV670 GDDR3 (Revival) based on B339
1	00B	07/08/1	(pg 1) Adding R1 and connecting switch #7 of TSW1. Some mother boards require B7 to be grounded. Table-1 updated accordingly (pg 7) Adding R64 and MR64 to select HOT_PLUG_DET or ThermINT as the interrupt source. (pg 13) Adding R1617, MR1617, R1616, Q1613, R1615, R1618, and R1619 as option to support hot plug detection of external cable. (pg 13) Adding R1282, MR1282, R1283, MR1283, R1284, MR1284, R1281, R1285, Q1280, and C1280 as option for thermal protection for VDDC SMPS MOSFETs (pg 13) Adding MC1603 (overlapped with C1603) (pg 14) Adding D870 as option for power up sequencing (pg 18) Adding heatsink symbol/footprint (Layout) Increasing spacing between DDC4DATA & DDC4CLK going to U1270 to reduce the crosstalk



RH PCIE RV670 512MB GDDR3
DUAL DL-DVI-I VO FH

REV 1

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Doc No.	105-B340xx-00B