

PG110-A00

GP108 64Bit GDDR5 X32

HDMI/DP + DVI-D/DP

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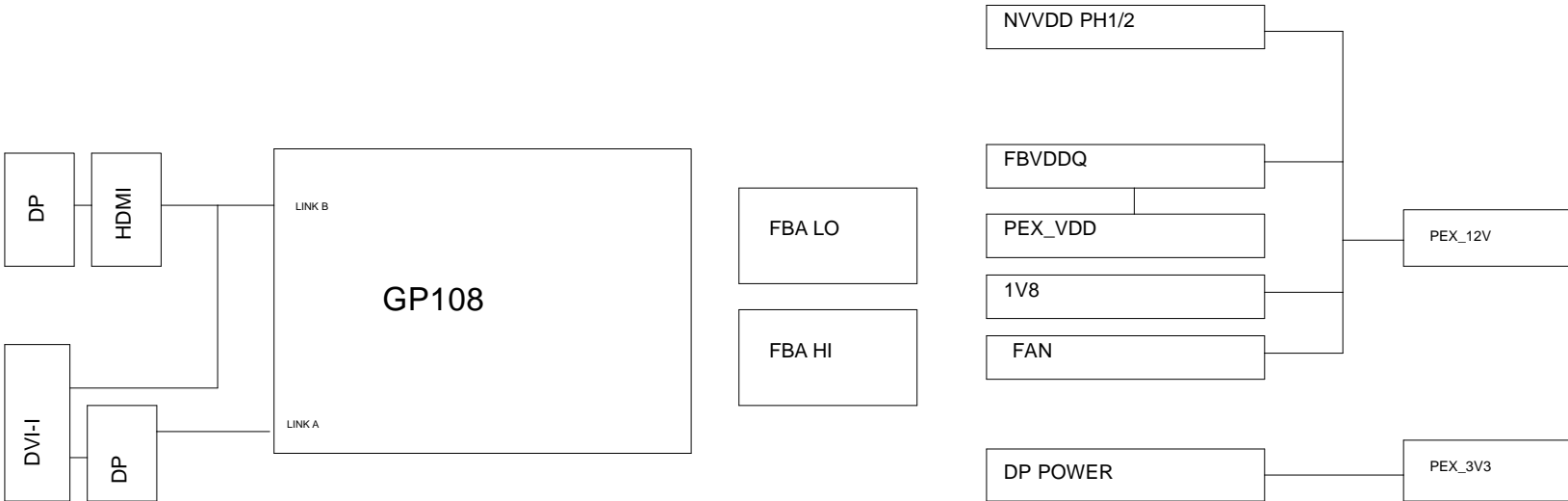
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Block Diagram

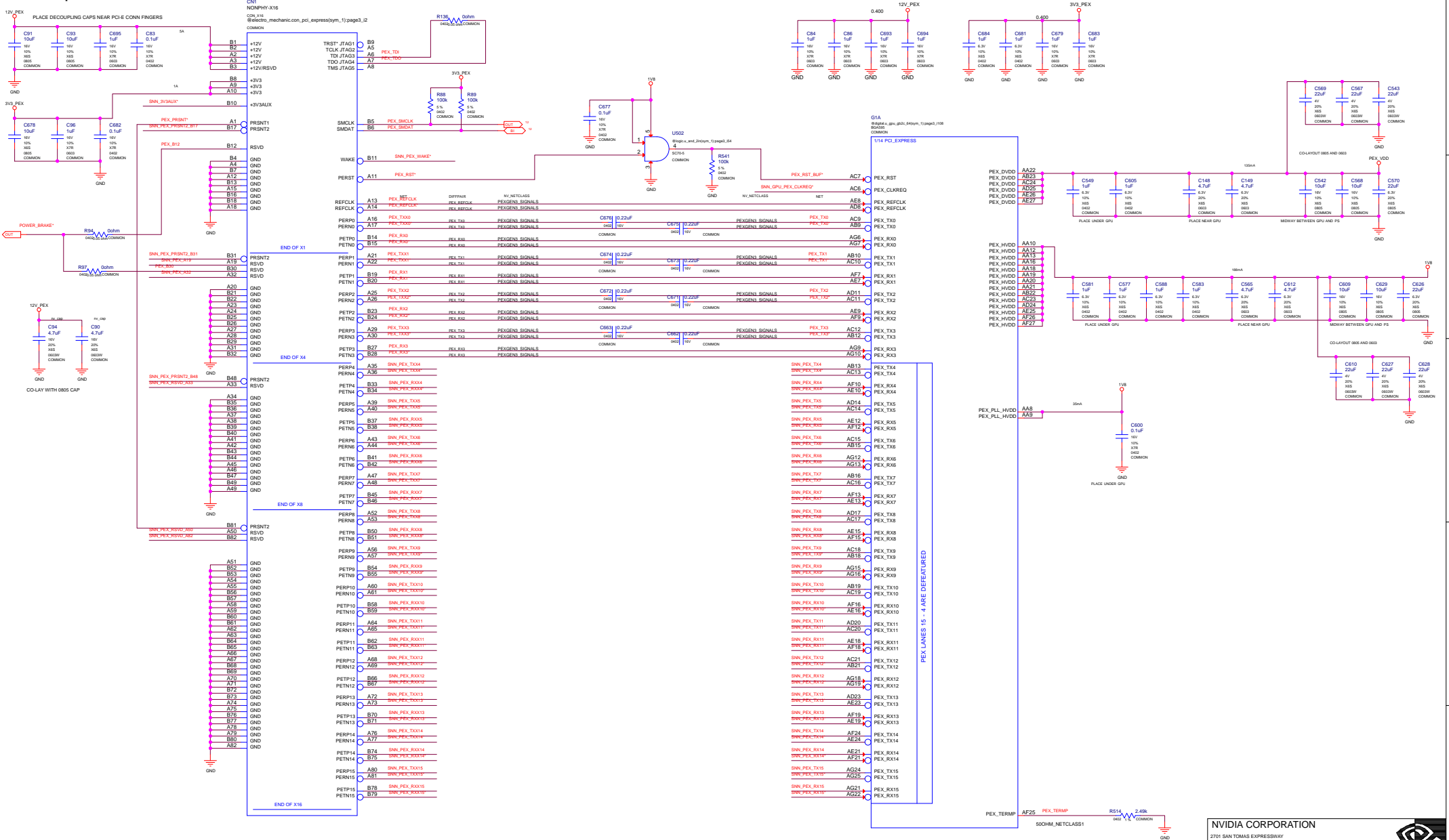



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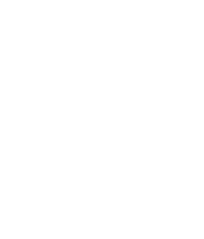
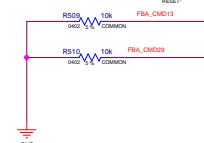
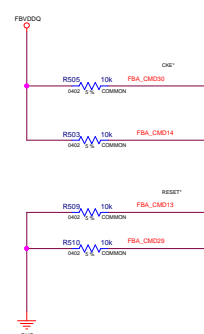
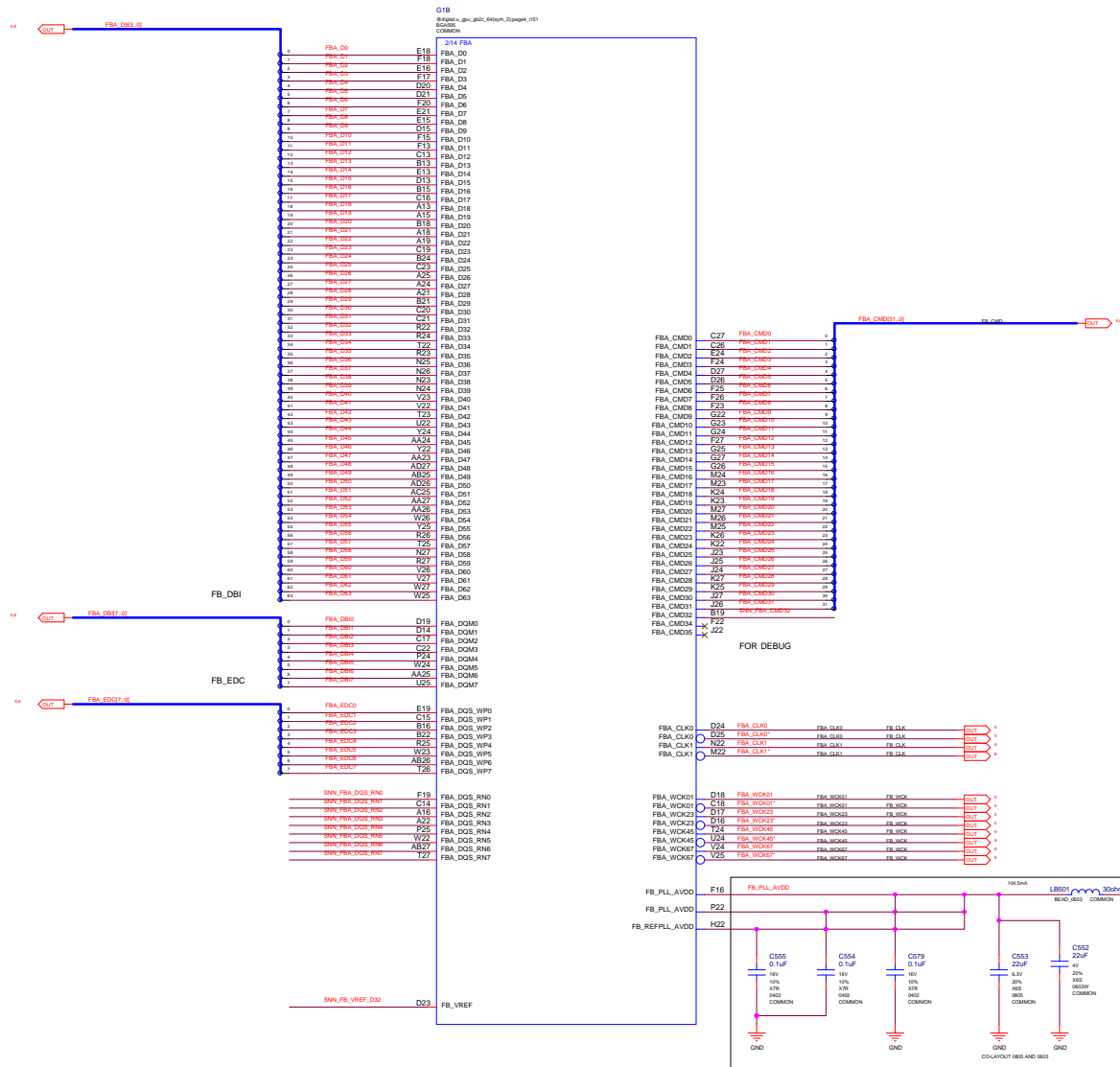
PCI Express



ASSEMBLY		ASSEMBLY DESCRIPTION:		SANTA CLARA, CA 95050, USA			
PAGE DETAIL		PCI Express					
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GPU Frame Buffer

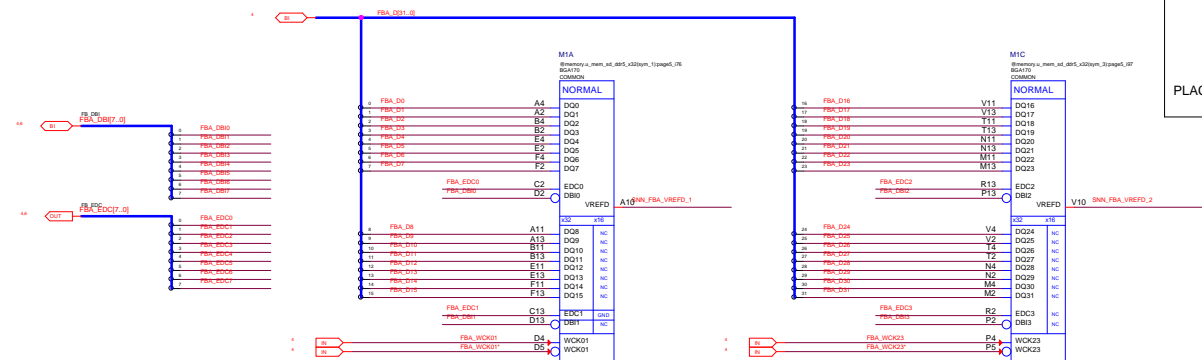
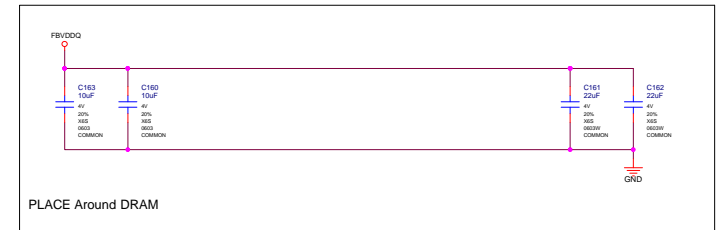
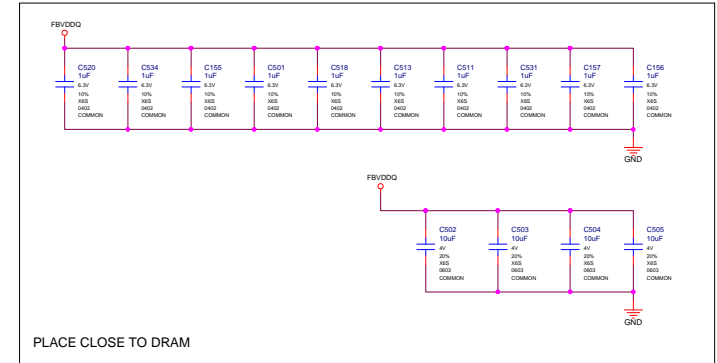
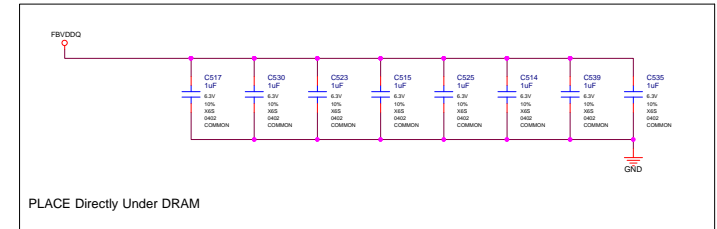
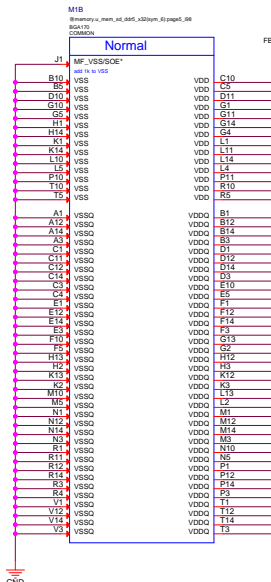
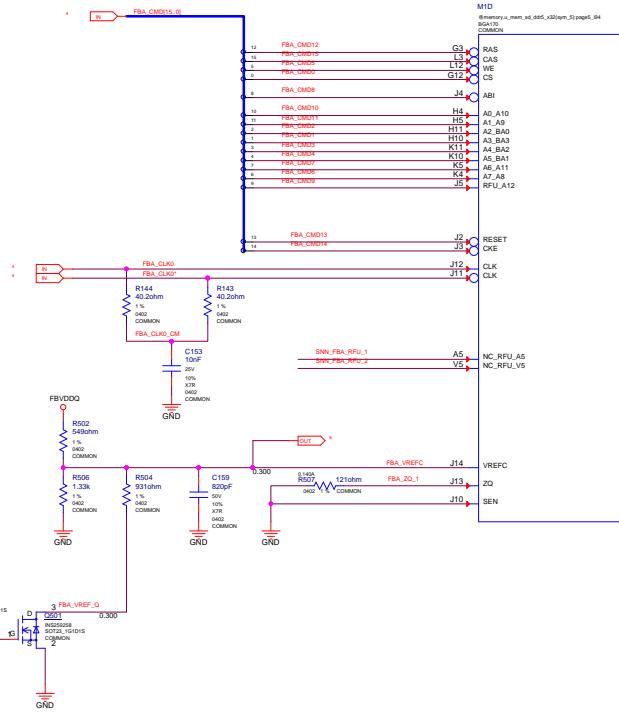


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FBA bits 31..00

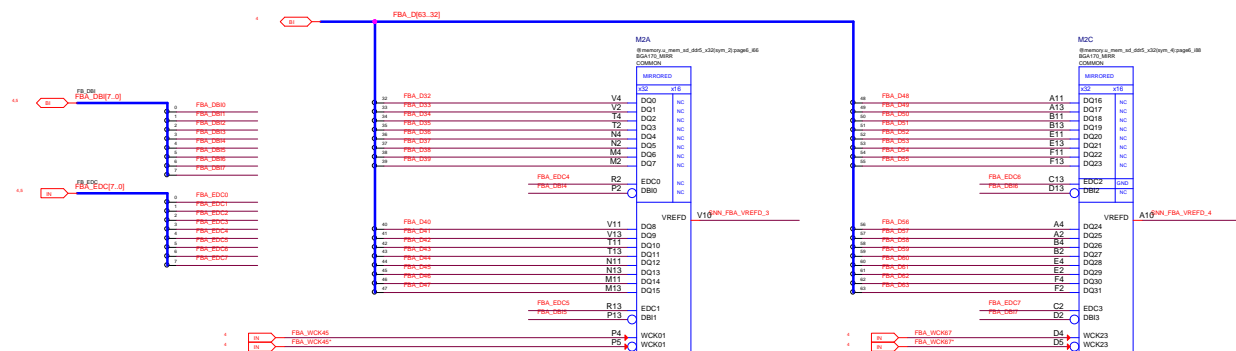
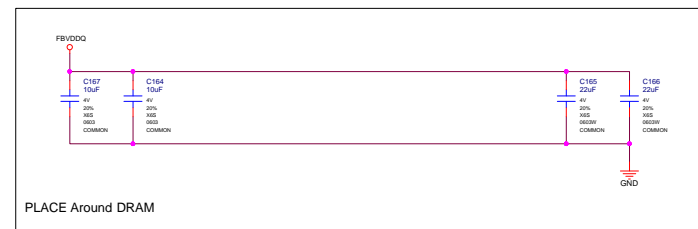
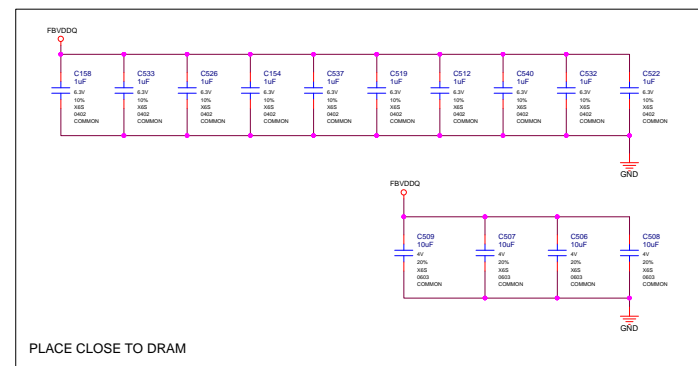
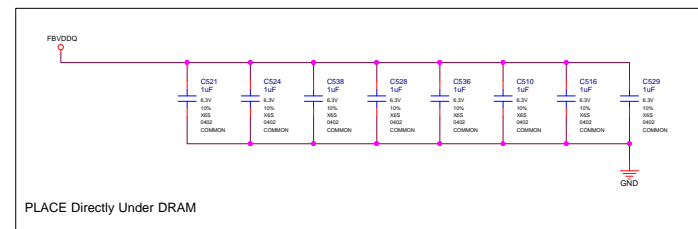
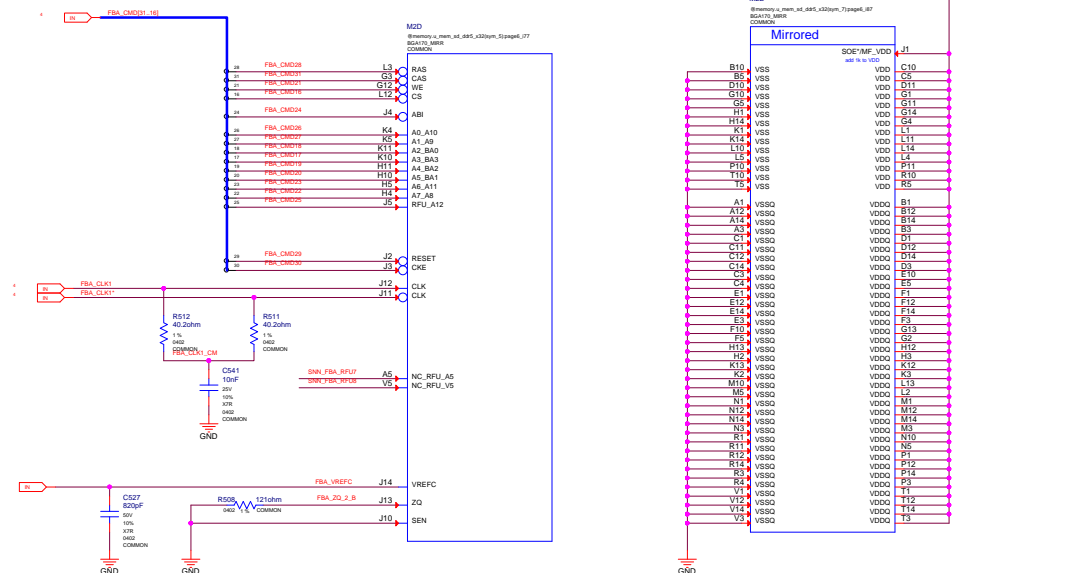
CMD	0.31	32..63
CMD0	CS*	
CMD1	A3, BA3	
CMD2	A2, BA2	
CMD3	AA, BA2	
CMD4	AS, BA1	
CMD5	WE*	
CMD6	A7, AS	
CMD7	AE, A11	
CMD8	AB*	
CMD9	A12, RFU	
CMD10	AO, A10	
CMD11	A10, A10	
CMD12	BA5*	
CMD13	RS1*	
CMD14	CA5*	
CMD15	CA5*	
CMD16		CS*
CMD17		A3, BA3
CMD18		A2, BA2
CMD19		A4, BA2
CMD20		AS, BA1
CMD21		WE*
CMD22		A7, AS
CMD23		AE, A11
CMD24		AB*
CMD25		A12, RFU
CMD26		AO, A10
CMD27		A10, A10
CMD28		A1, AS
CMD29		BA5*
CMD30		RS1*
CMD31		CA5*



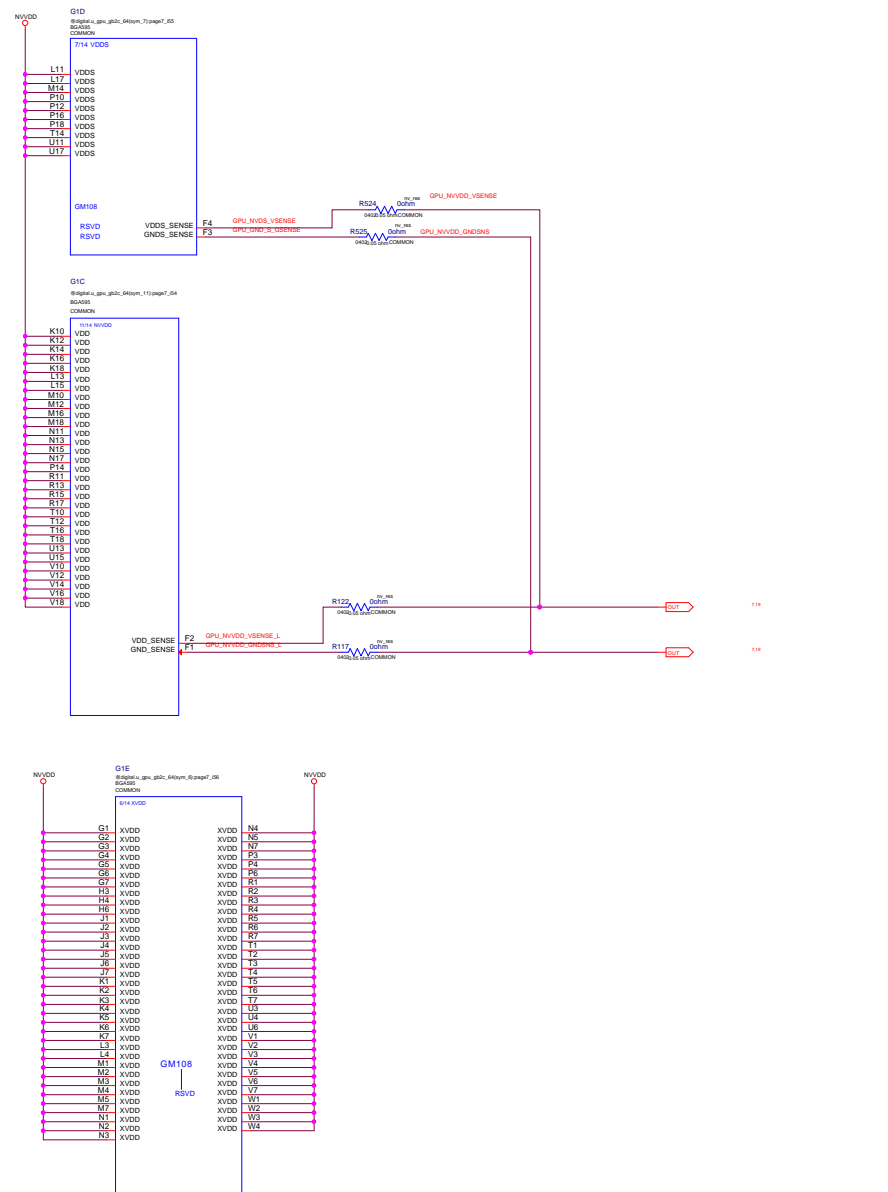
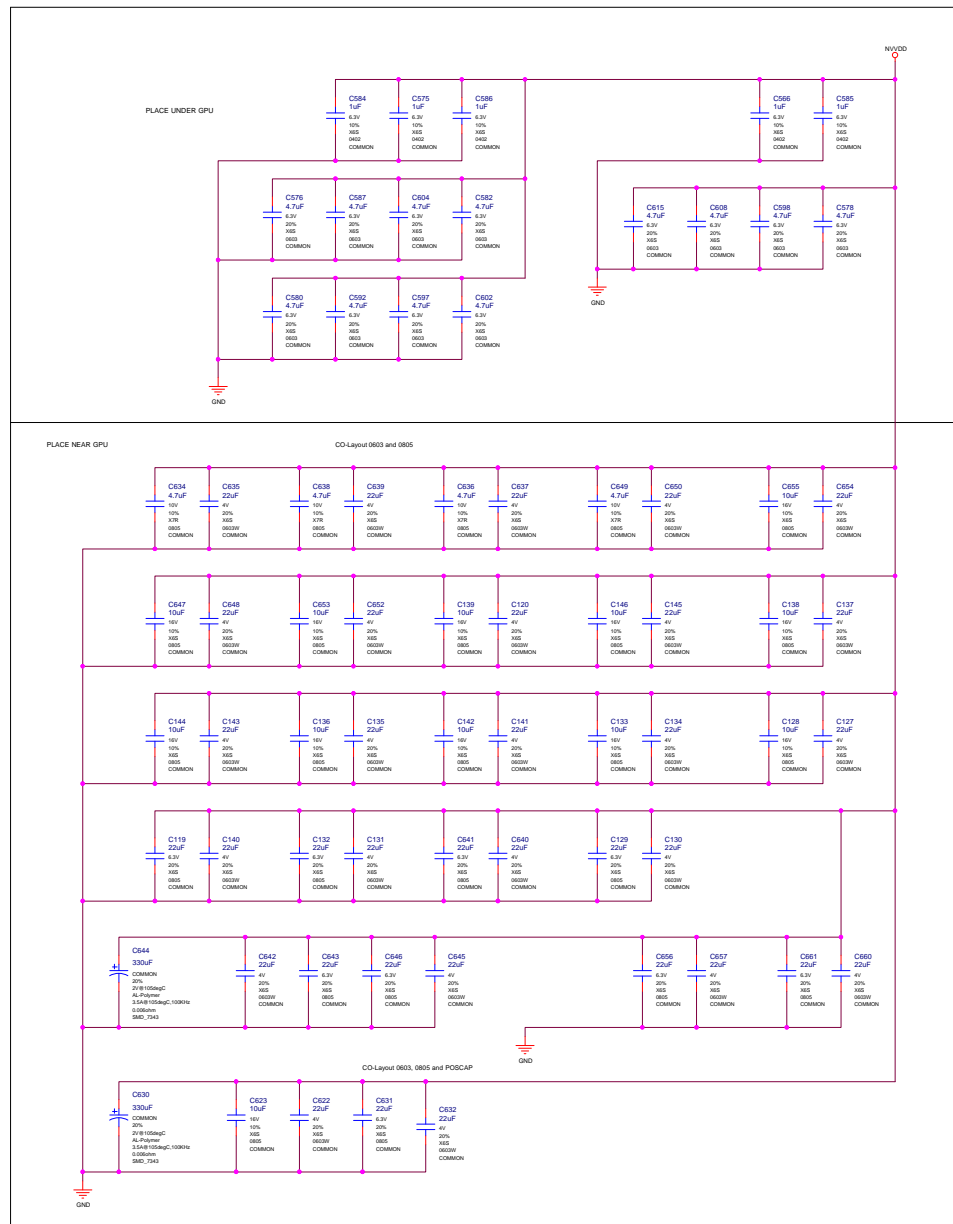
FBA bits 63..32

GDDR5_BGA170_MiRR

CMD	0.31	32.63
CM00	CS*	
CM01	A3, BA3	
CM02	A2, BA0	
CM03	A4, BA2	
CM04	AS, A1	
CM05	WE*	
CM06	A7, A8	
CM07	AB, A11	
CM08	AB*	
CM09	A12, RFU	
CM10	AJ, A10	
CM11	A1, A9	
CM12	RA*	
CM13	RST*	
CM14	CNE*	
CM15	CAS*	
CM16		CS*
CM17		A3, BA3
CM18		A2, BA0
CM19		A4, BA2
CM20		AS, A1
CM21		WE*
CM22		A7, A8
CM23		AB, A11
CM24		AB*
CM25		A12, RFU
CM26		AJ, A10
CM27		A1, A9
CM28		RA*
CM29		RST*
CM30		CNE*
CM31		CAS*



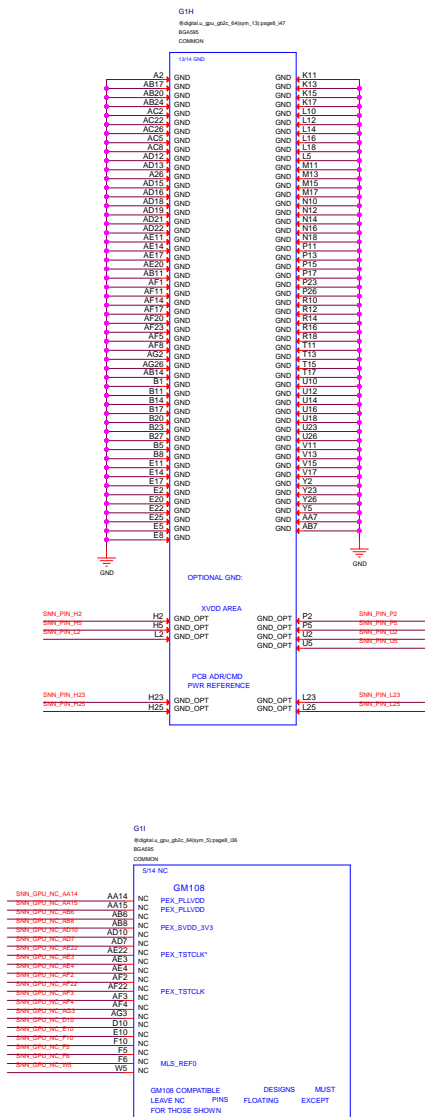
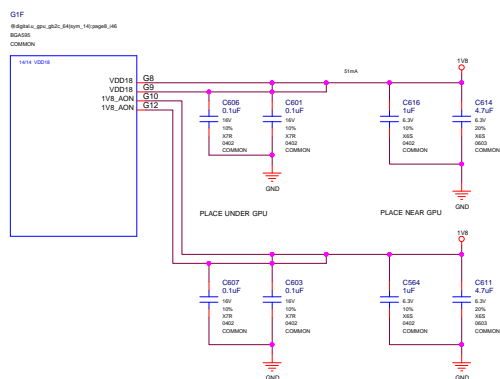
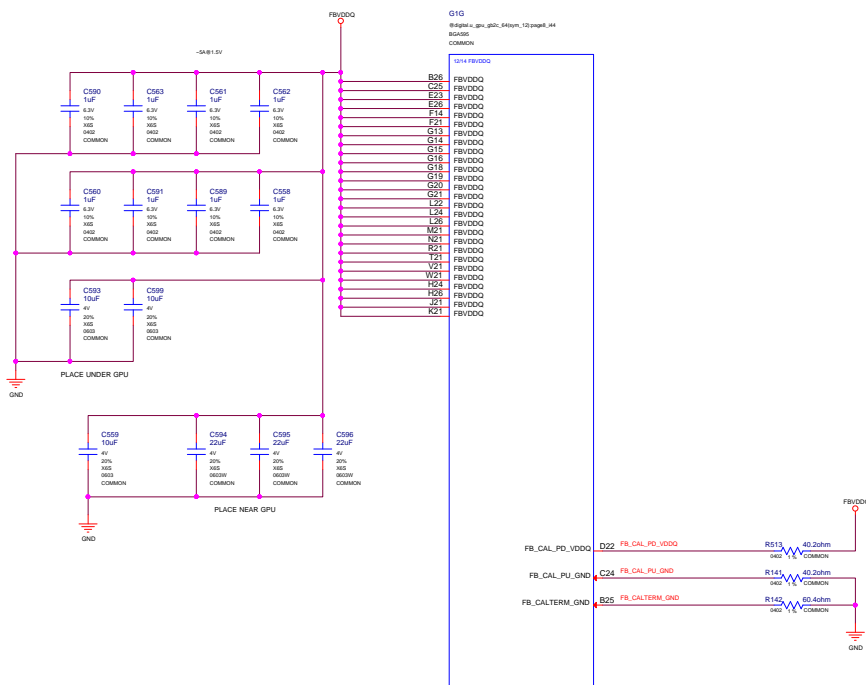
NVVVD Decoupling



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PAGE DETAIL
"ASSEMBLY DESCRIPTION"
NVVVD Decoupling

FBVDDQ and 1V8 Decoupling



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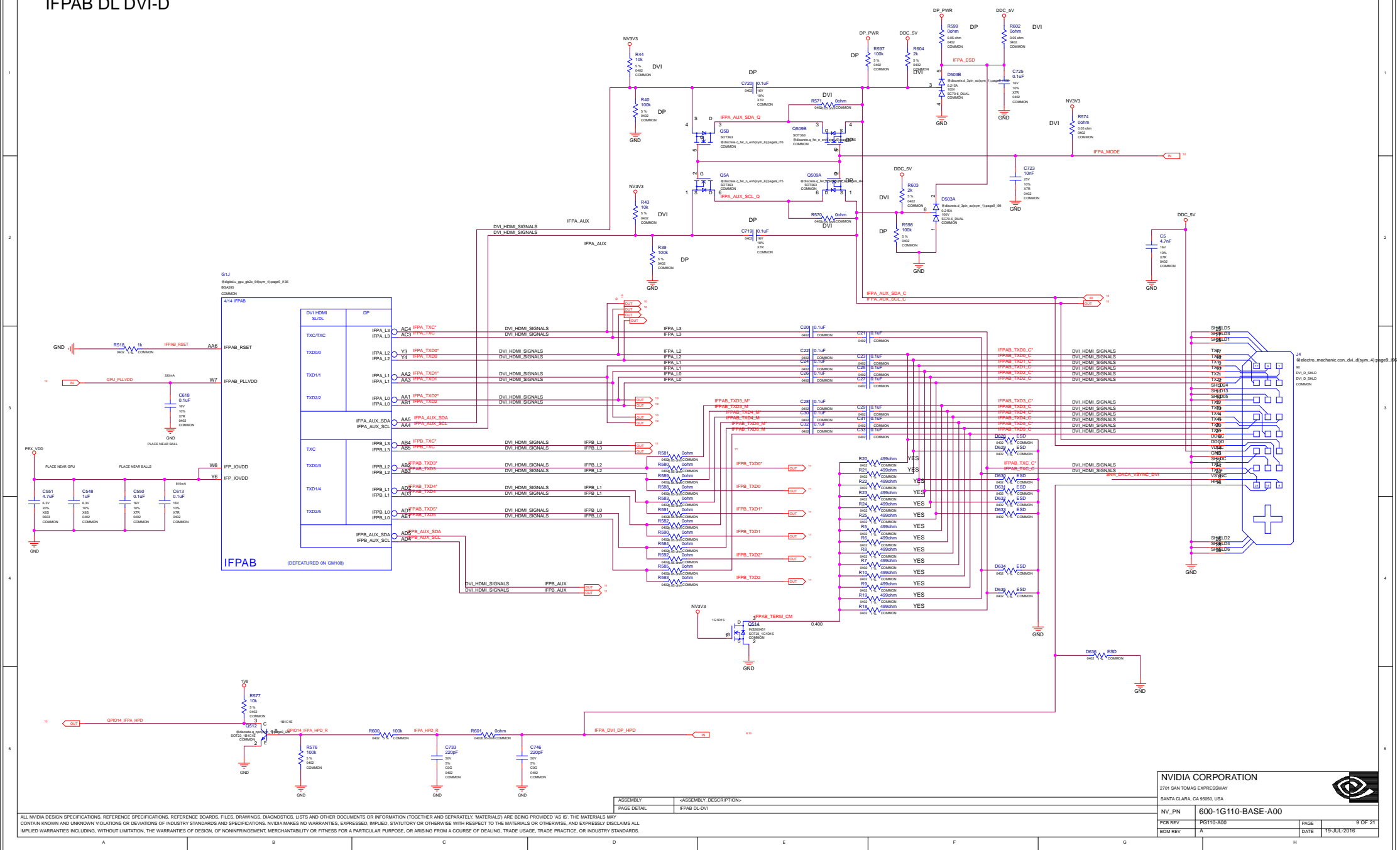


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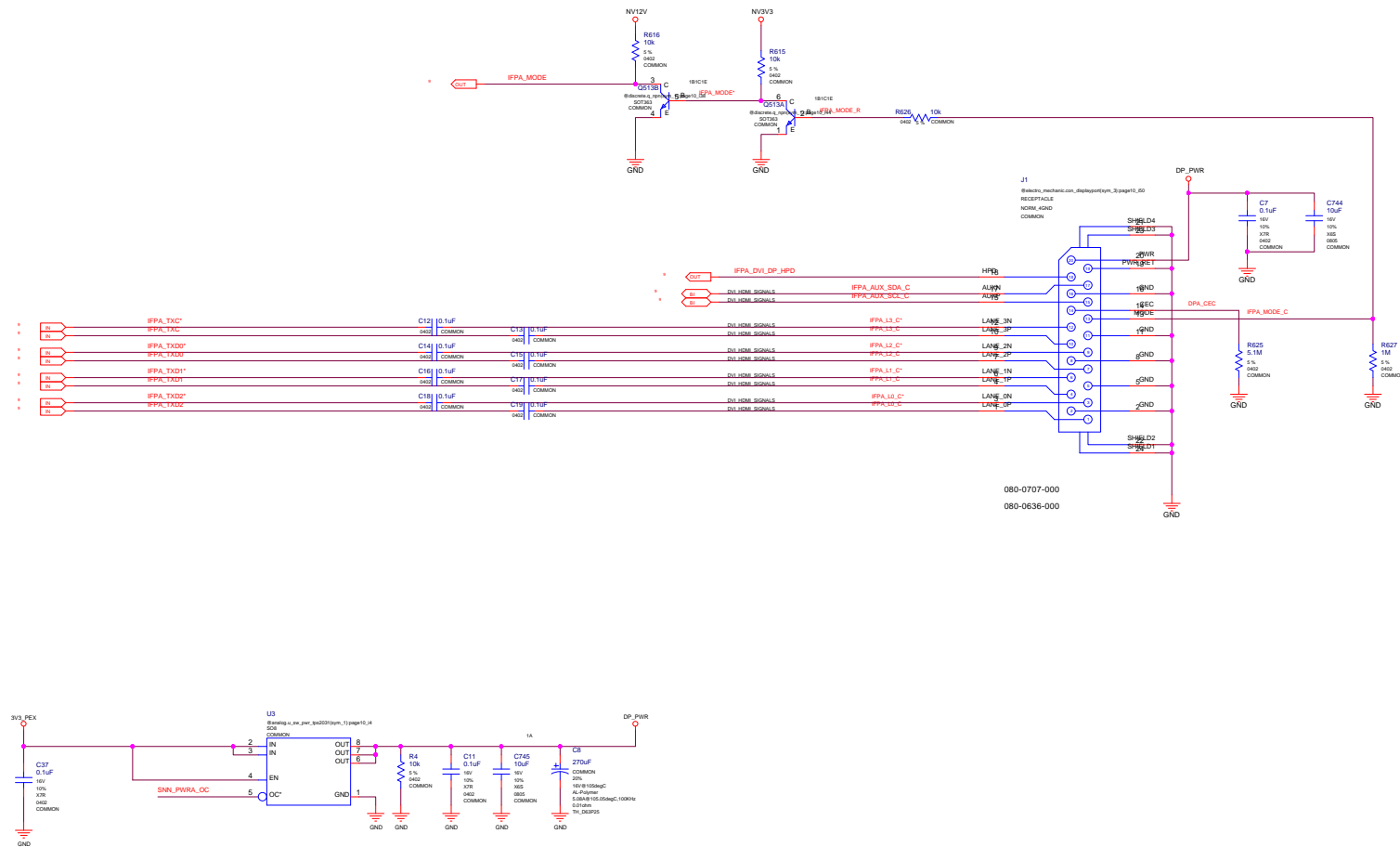
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IFPAB DL DVI-D



IFPA DP



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PAGE DETAIL	IFPA DP

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IFPB HDMI/DP

8.11
8.11
8.11
8.11
8.11
8.11

10 CUT

Hotplug Detection

ASSEMBLY	ASSEMBLY DESCRIPTION
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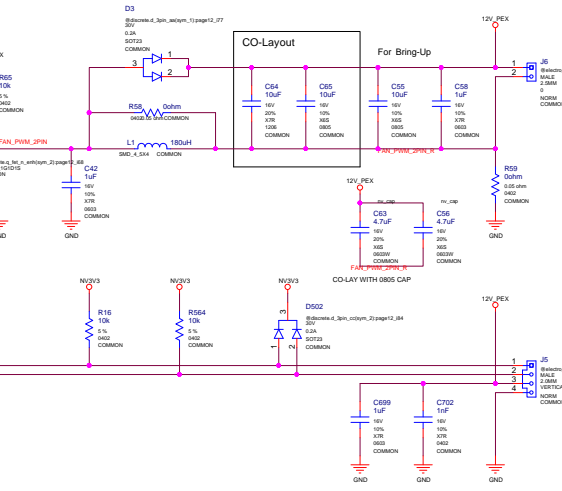
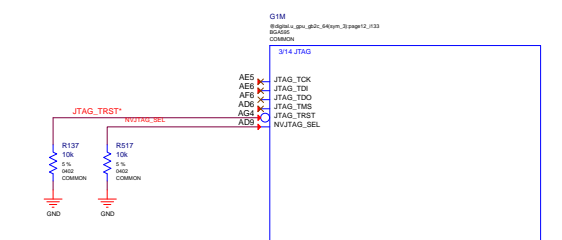
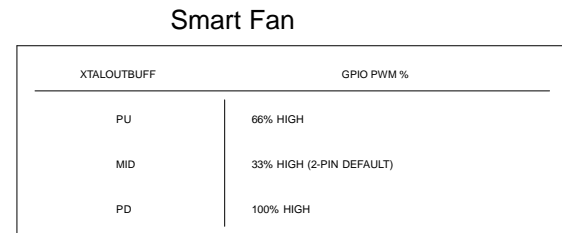
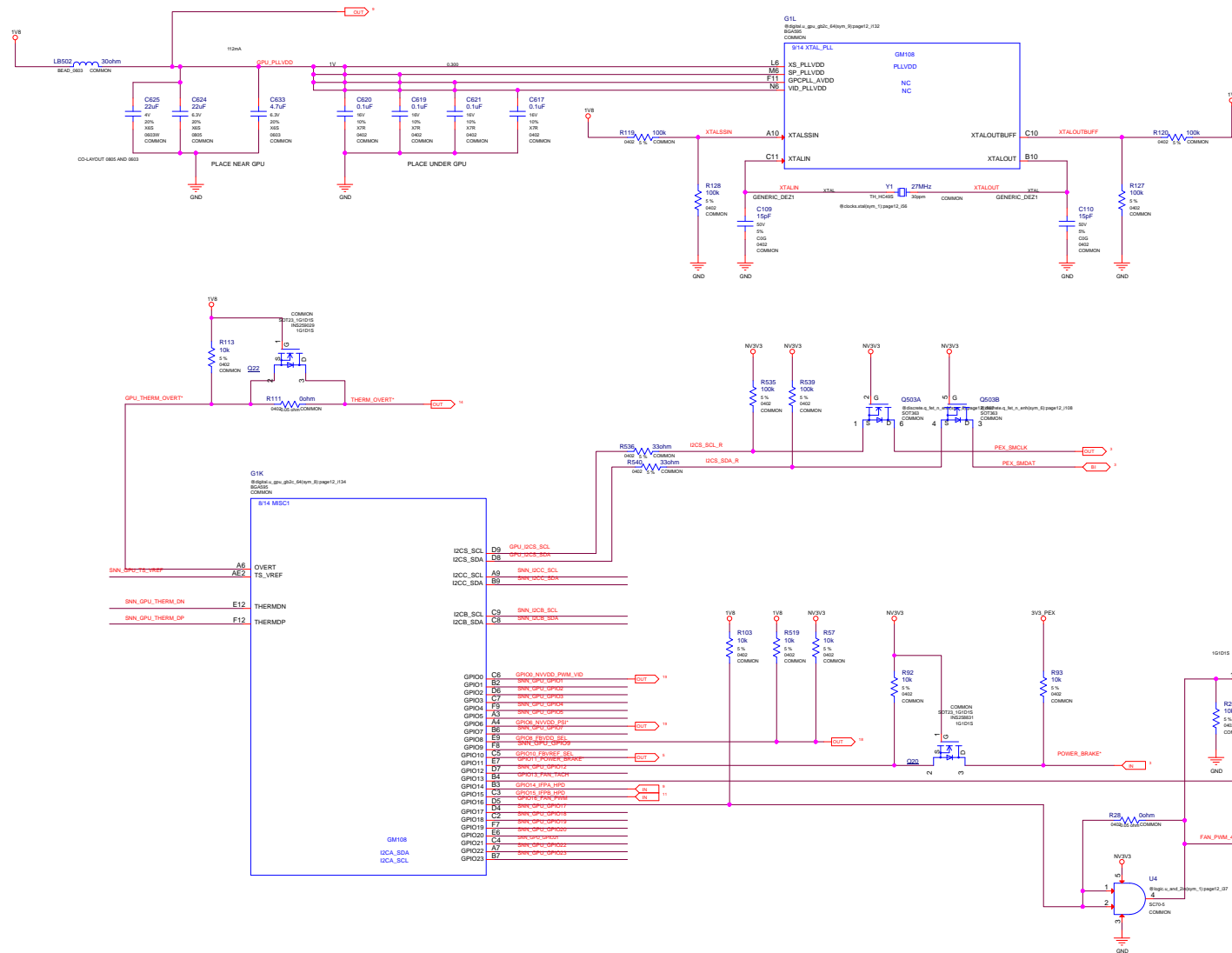
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A B C D E F G H

JTAG,GPIO&XTAL



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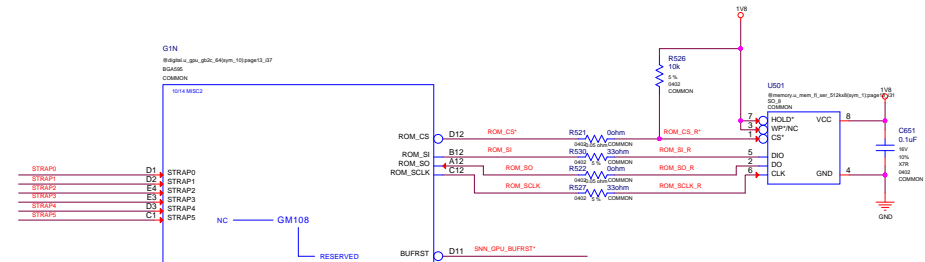
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ROM & STRAPS

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	DEFAULT
L	L	H	0001	
L	H	L	0010	
L	H	H	0011	
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	

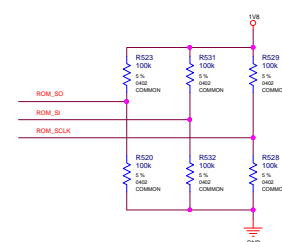
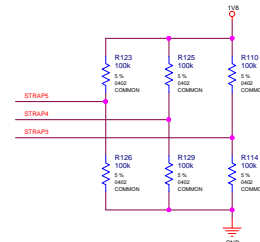
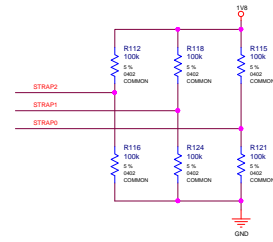
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
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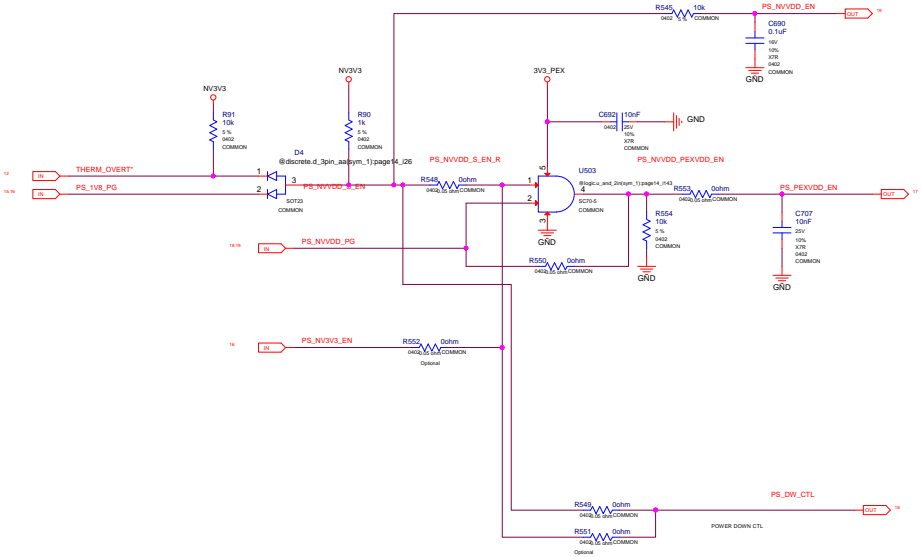
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Power Sequence




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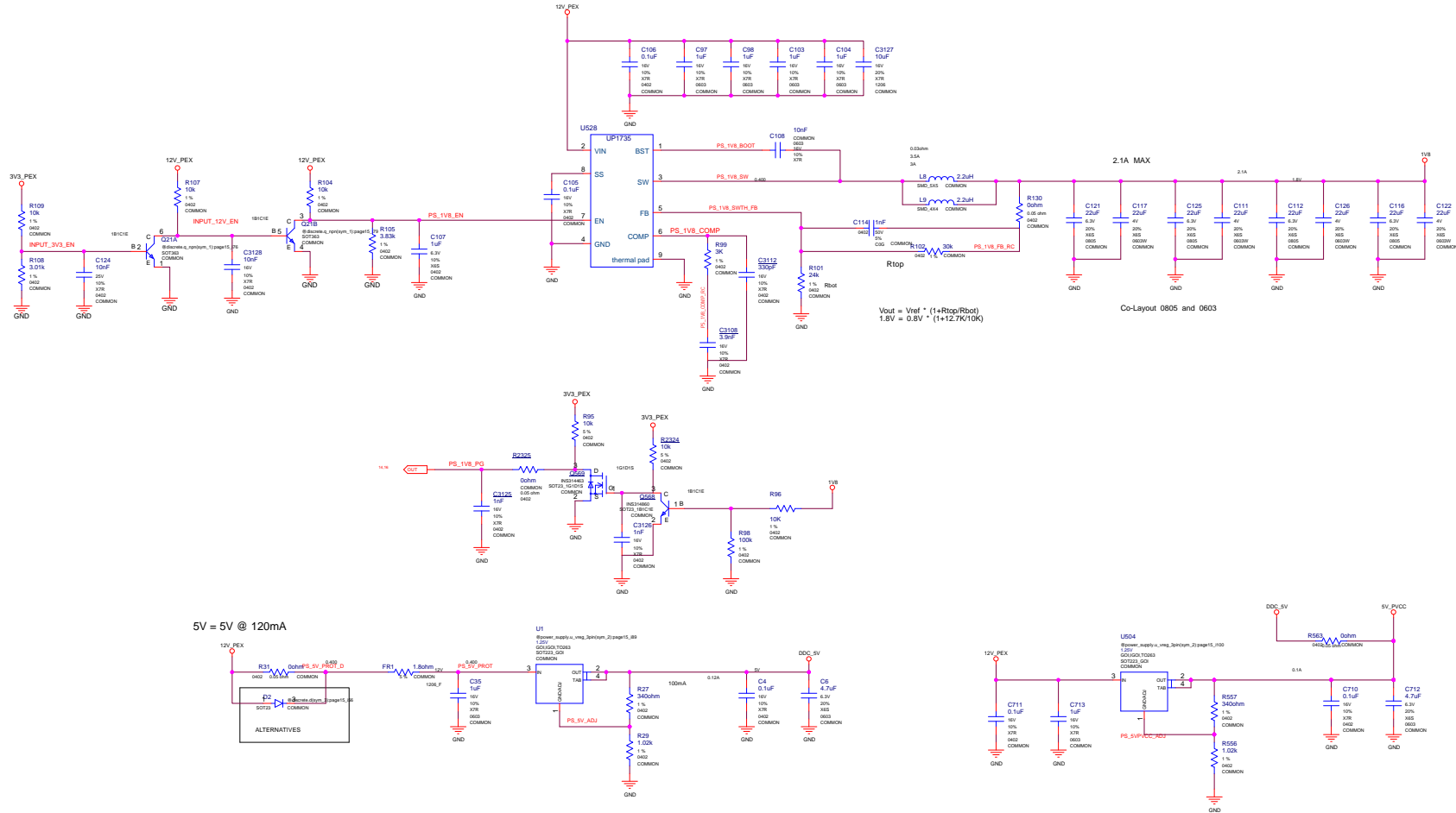
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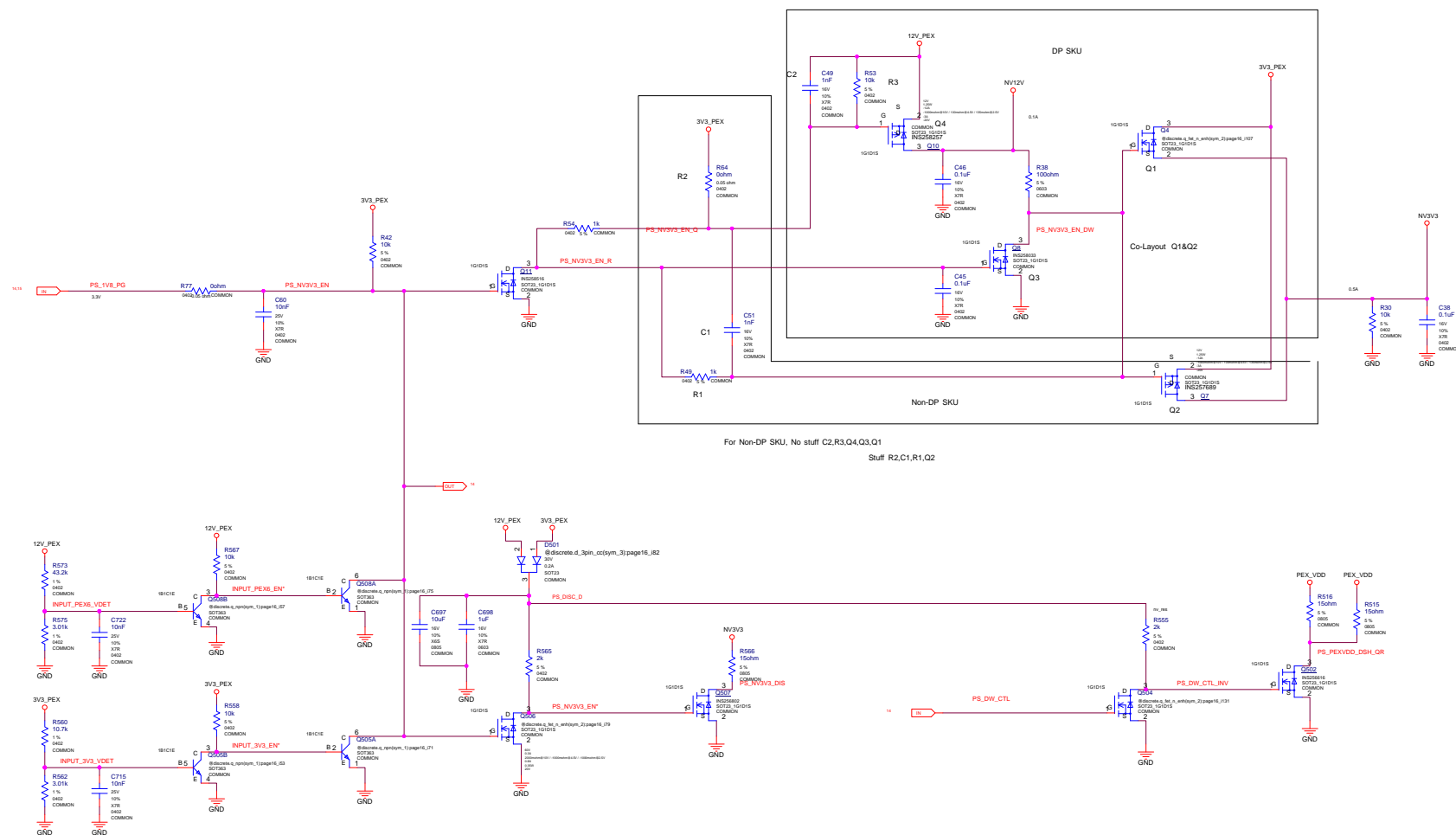


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POWER:1V8 & 5V



POWER: NV3V3, NV12V



For Non-DP SKU, No stuff C2,R3,Q4,Q3,Q1
Stuff R2,C1,R1,Q2

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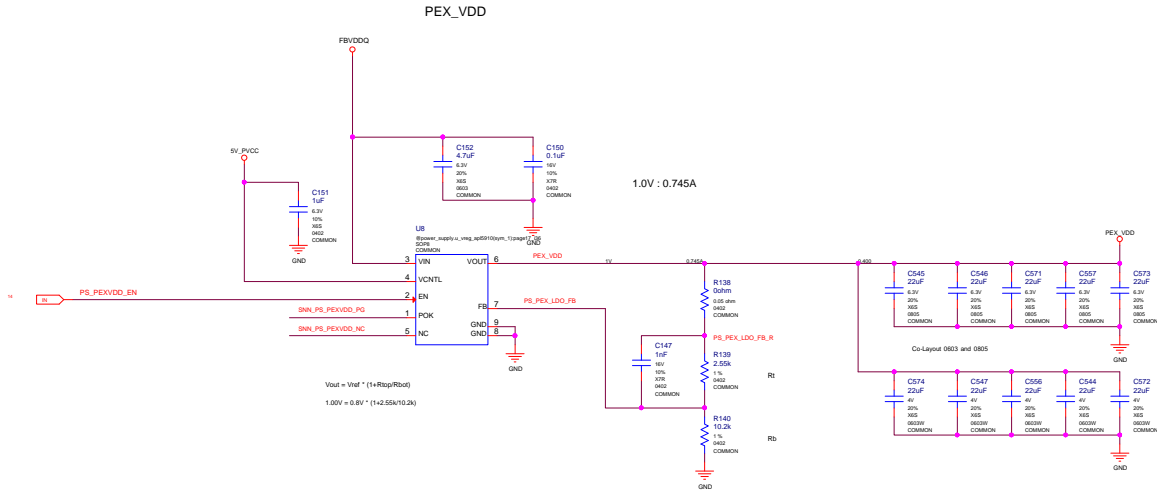
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POWER:PEX_VDD



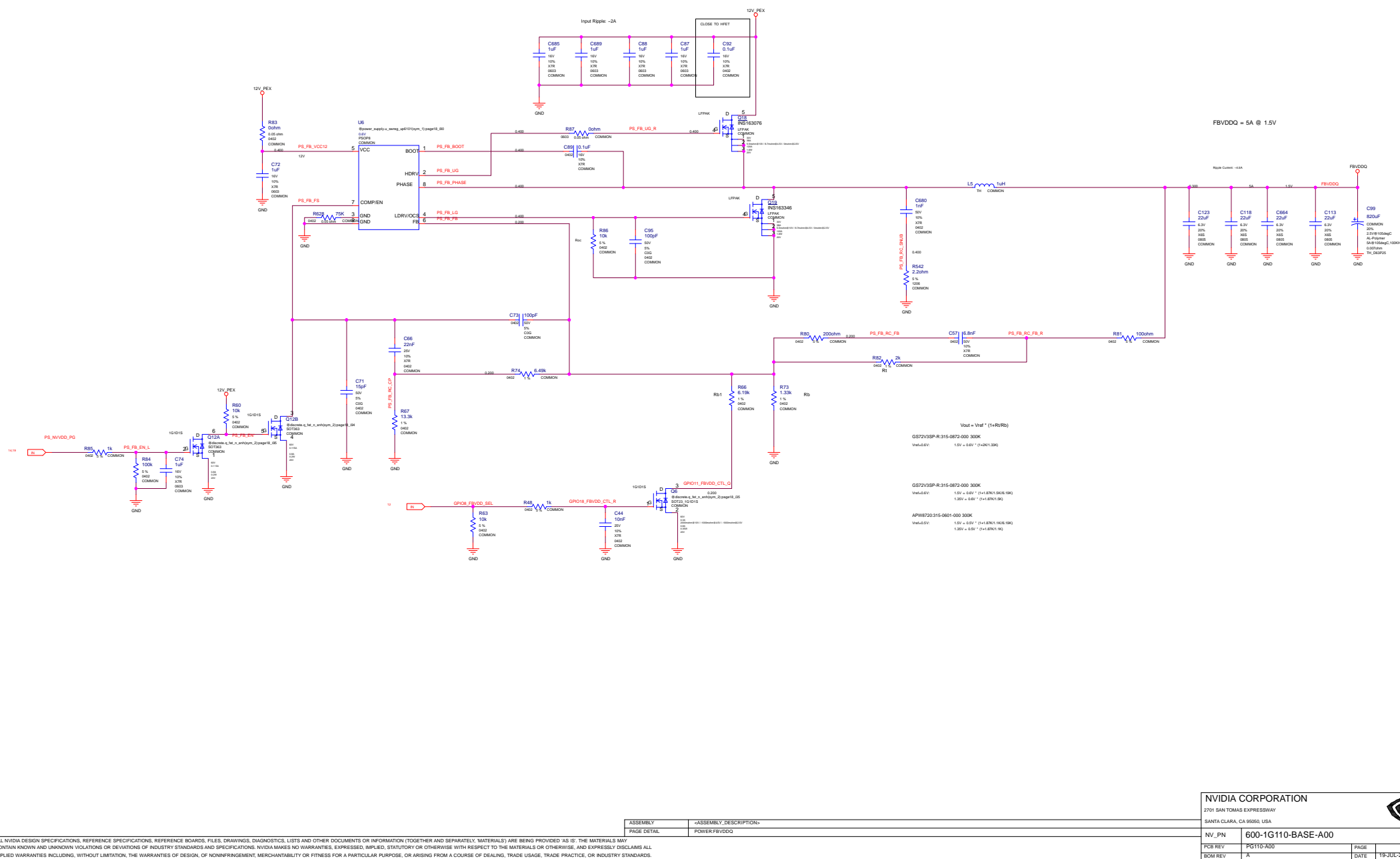
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POWER:FBVDDQ



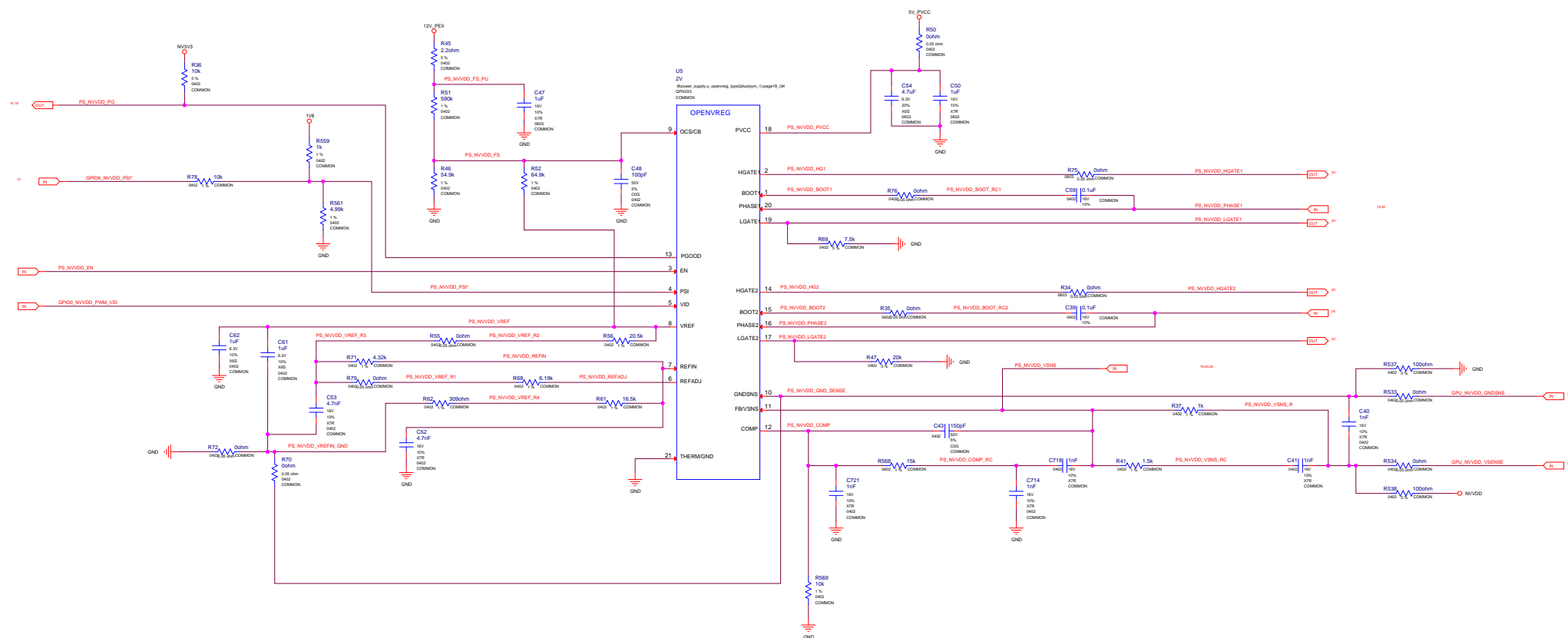
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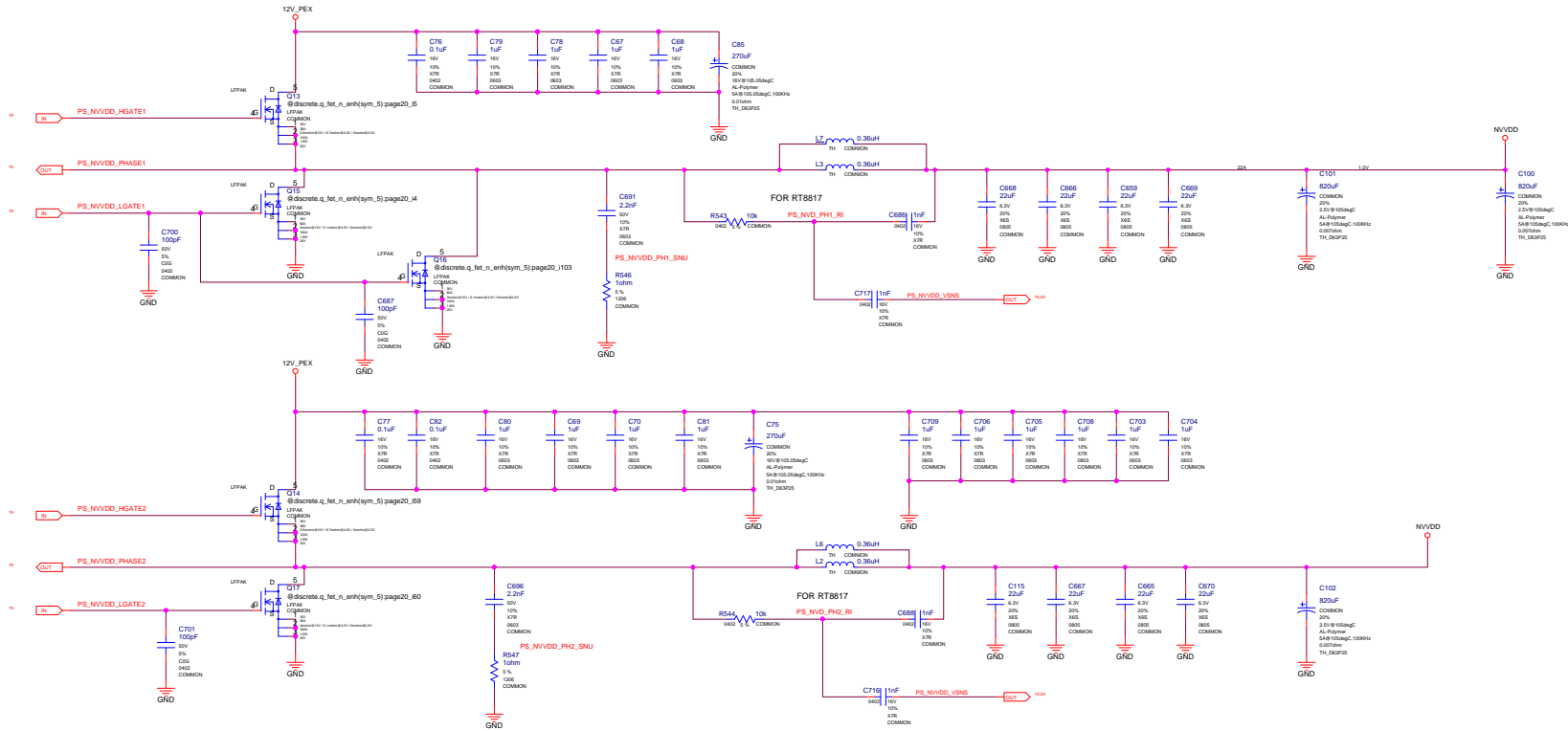


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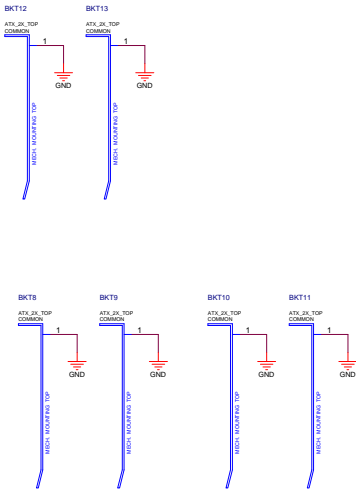
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Mechanical



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