

P229-B01  
DESIGN

PAGE SUMMARY:

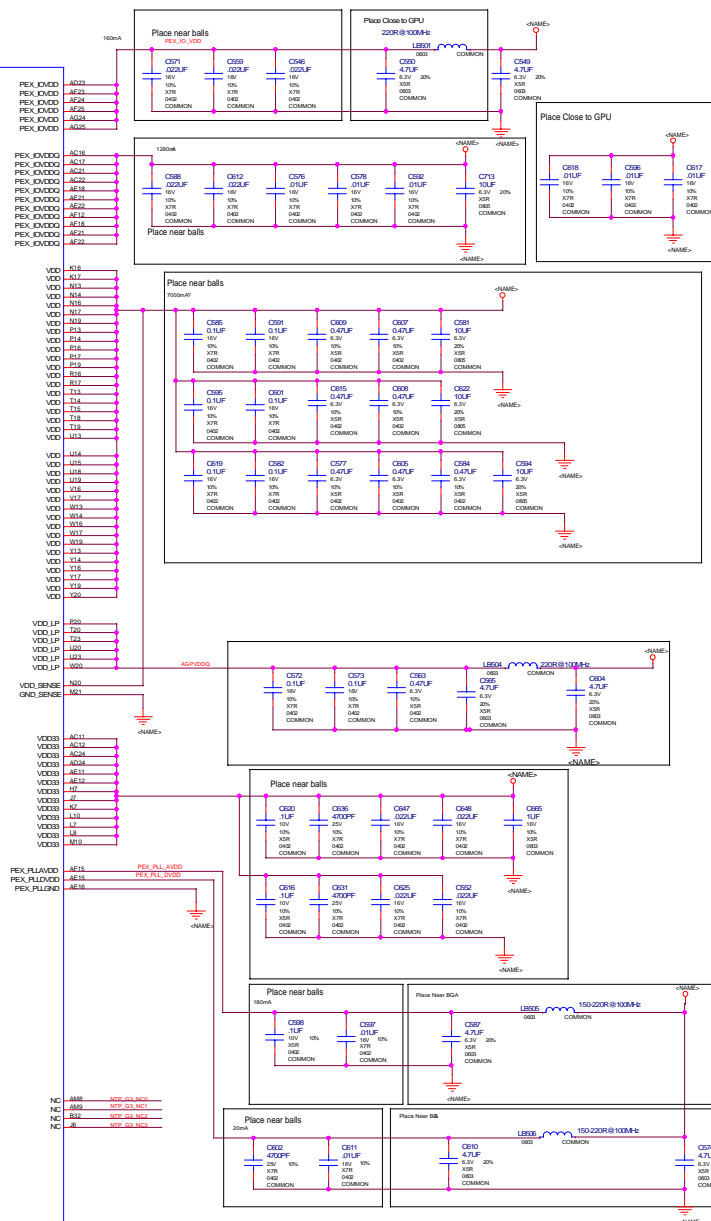
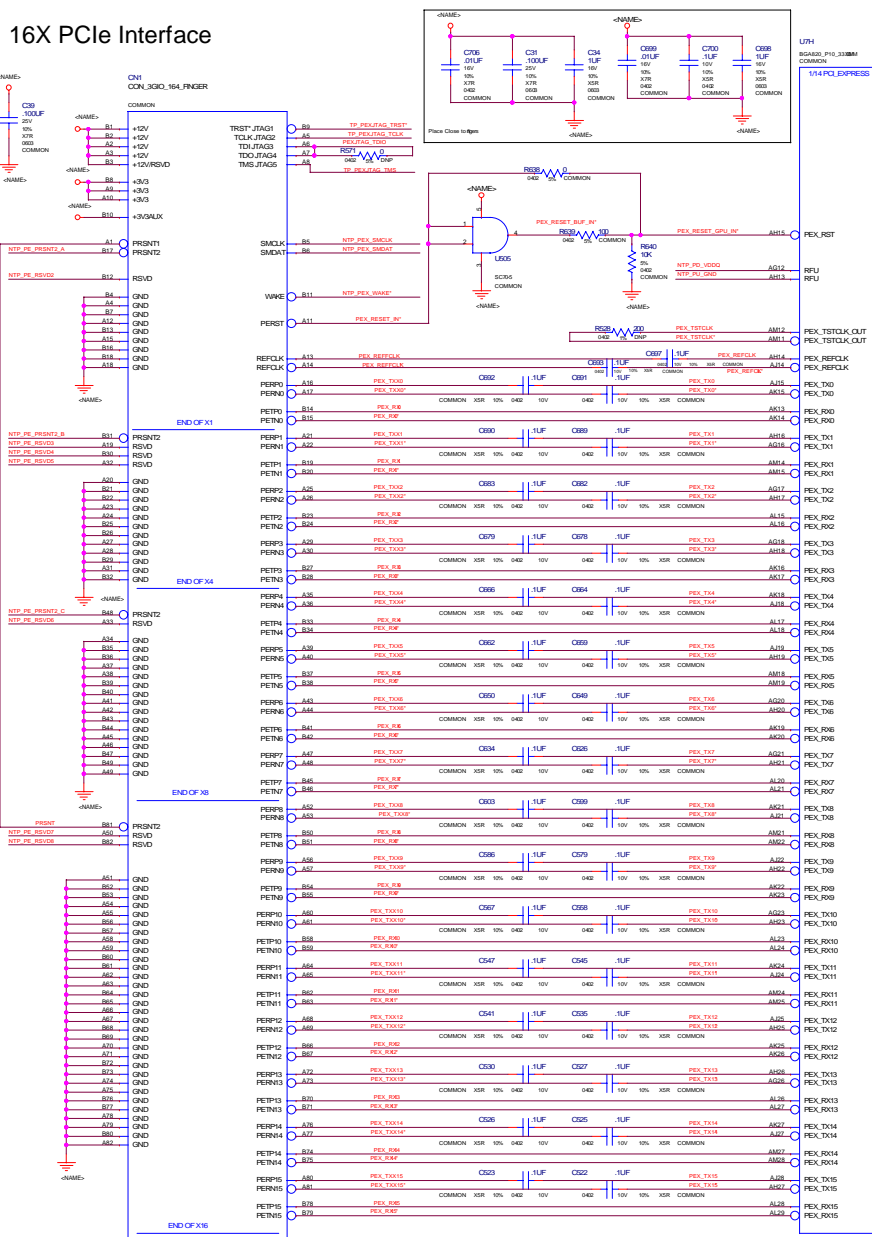
8981 Ver : 00A modify P229-B01 Summary

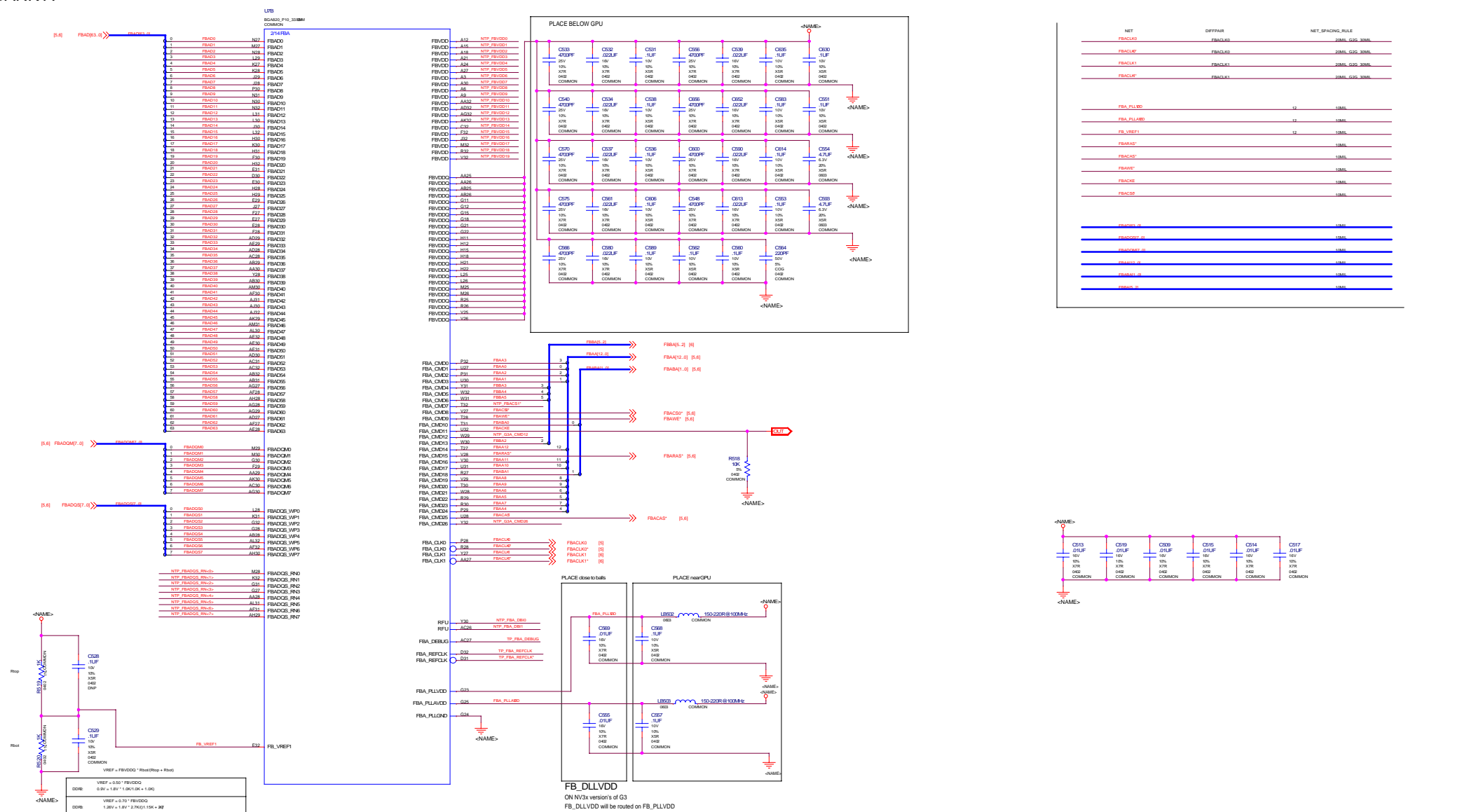
- Page 11. Add Video in connect to mini-din 10 pin & remove J5.
- Page 12. Add DVI-I common choke.
- Page 13. Connect net MIOBD 2 , MIOBD 6 & MIOBD 7 to BUS.
- Page 15. Modify Power ,PWM change to ISL6549.
- Page 16. Add Video function.

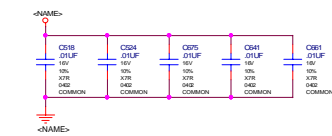
REVISION HISTORY:	
X1	Initial Release

REV	VARIANT	MFRN	ASSEMBLY
0	BASE	800-10229-8ASE-0CH	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON AND STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	rw43Mgskv29m1b	800-10229-0002-101	P229-B01 NVA3 GEN-DVA-HVGA-S-VIDEO 128MB 18M/16TSCP
2	rw43Mgskv29m1b	800-10229-0003-101	P229-B01 NVA3 GEN-DVA-HVGA-HDTV 128MB 18M/16TSCP
3	43gMgskv29m1b	800-10229-0005-101	P229-B01 NVA3-QL GEN-DVA-HVGA-HDTV 128MB 18M/16TSCP
4	rw43Mgskv29m1b	800-10229-0004-101	P229-B01 NVA3 GEN-DVA-HVGA-HDTV 256MB 18M/16TSCP
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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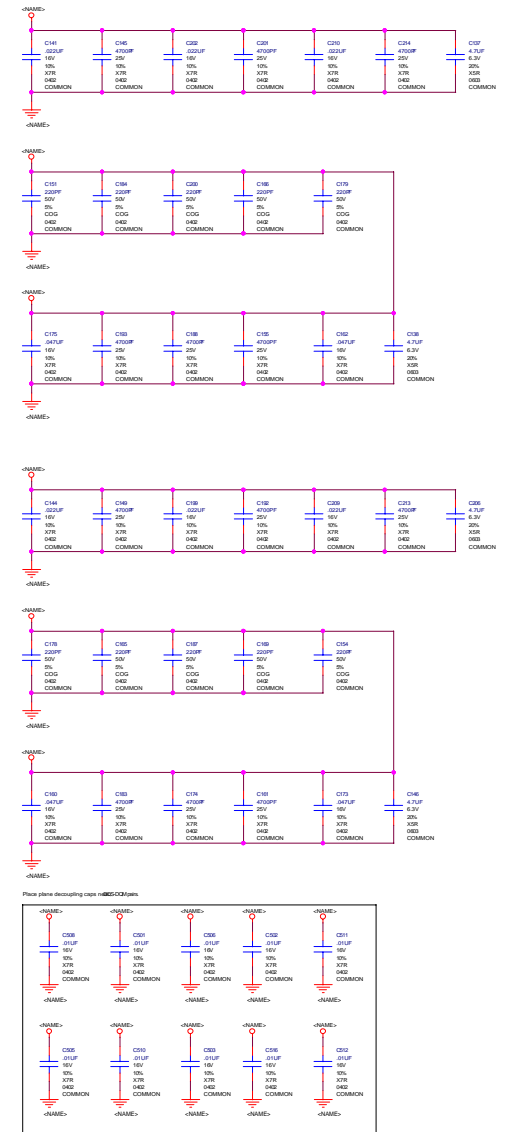
## 16X PCIe Interface

[illegible]

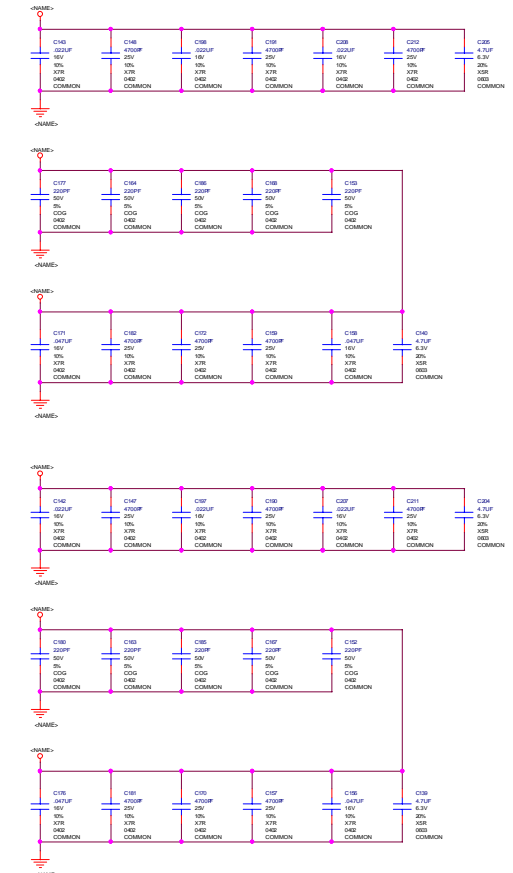




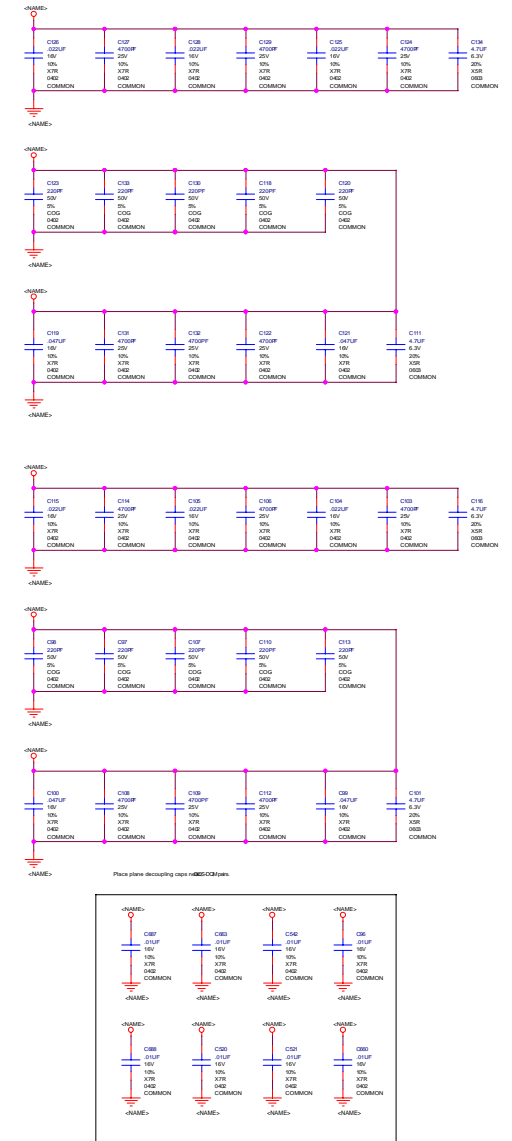
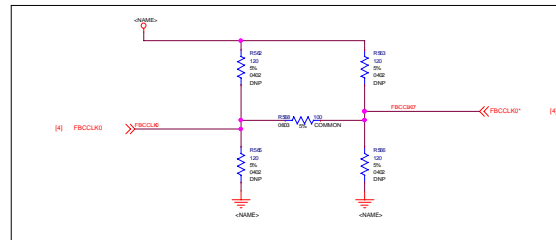
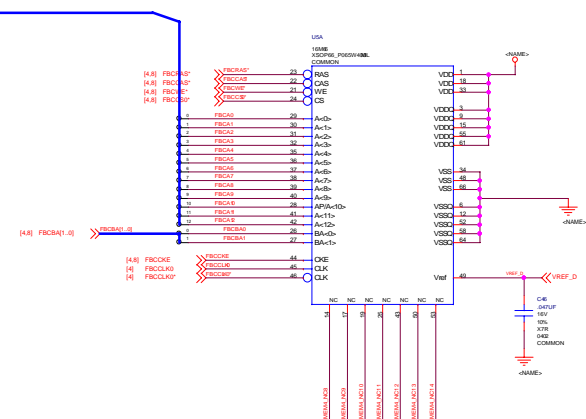
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



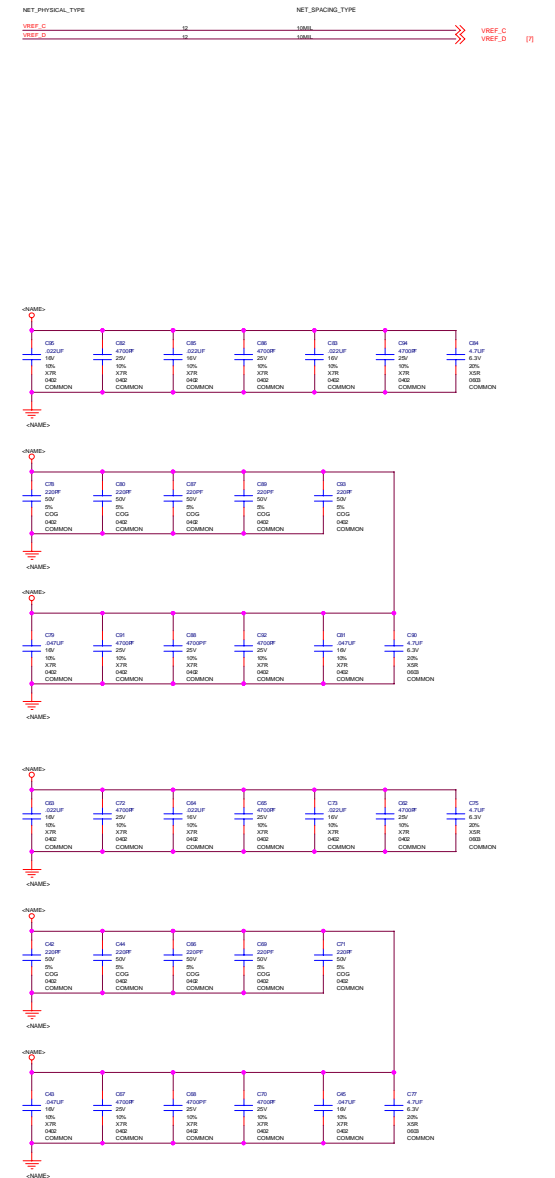
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

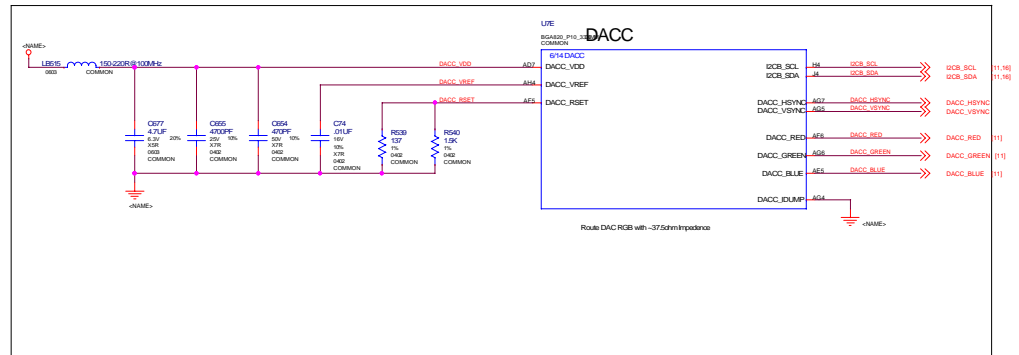
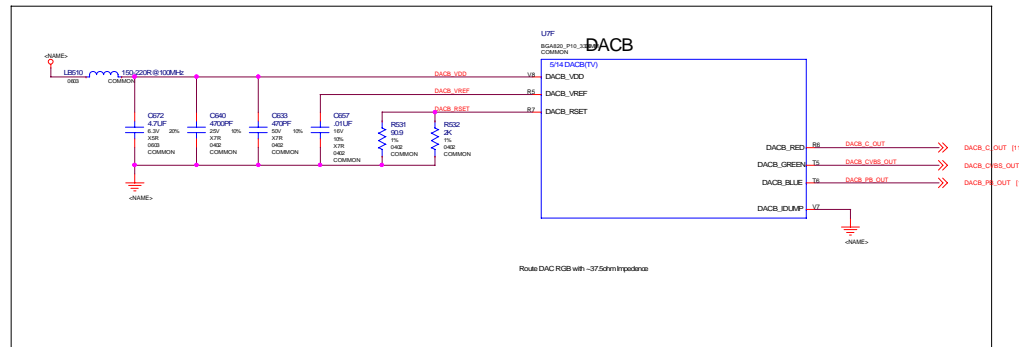
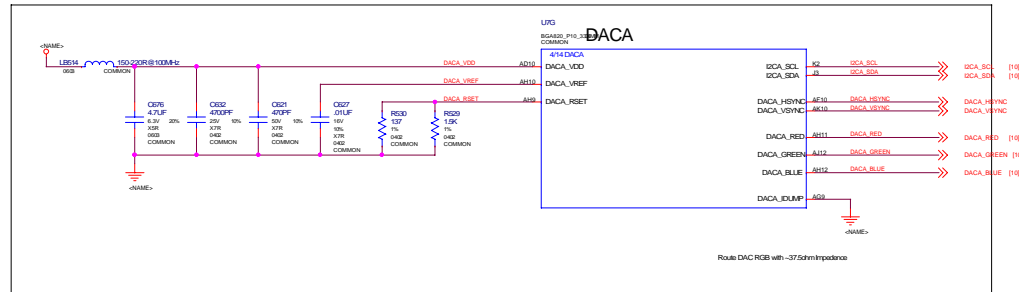
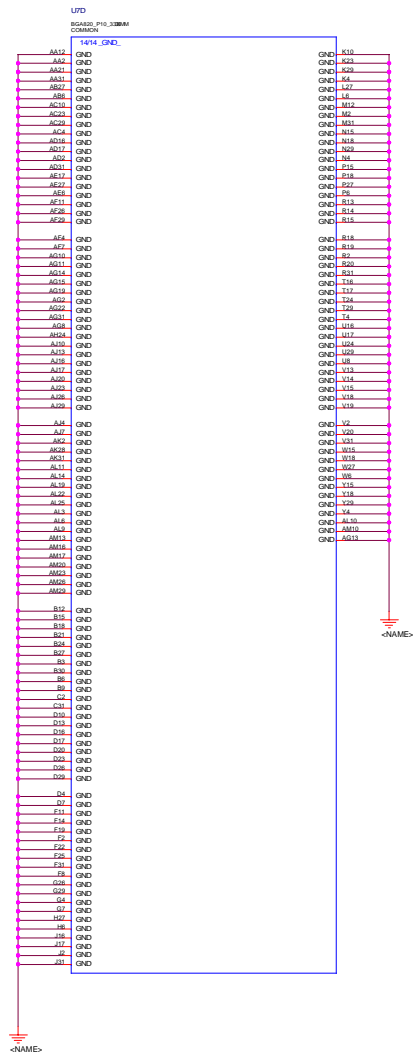


PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

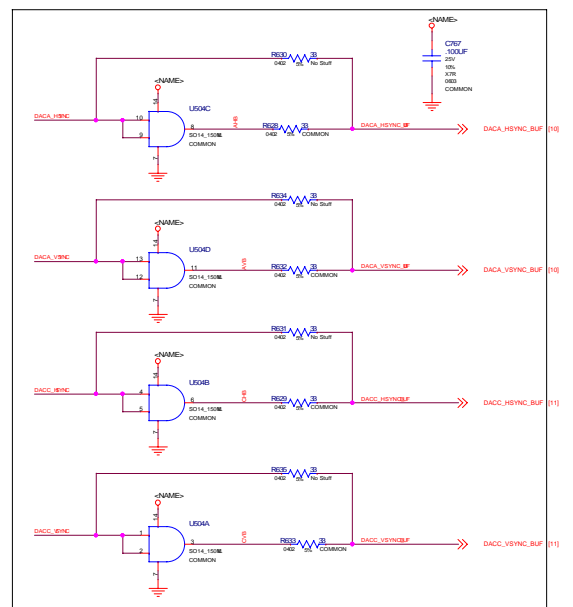




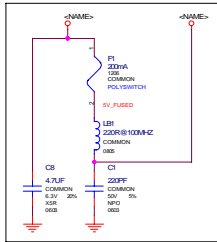
GND,DACA,DACB,DACC

[illegible]

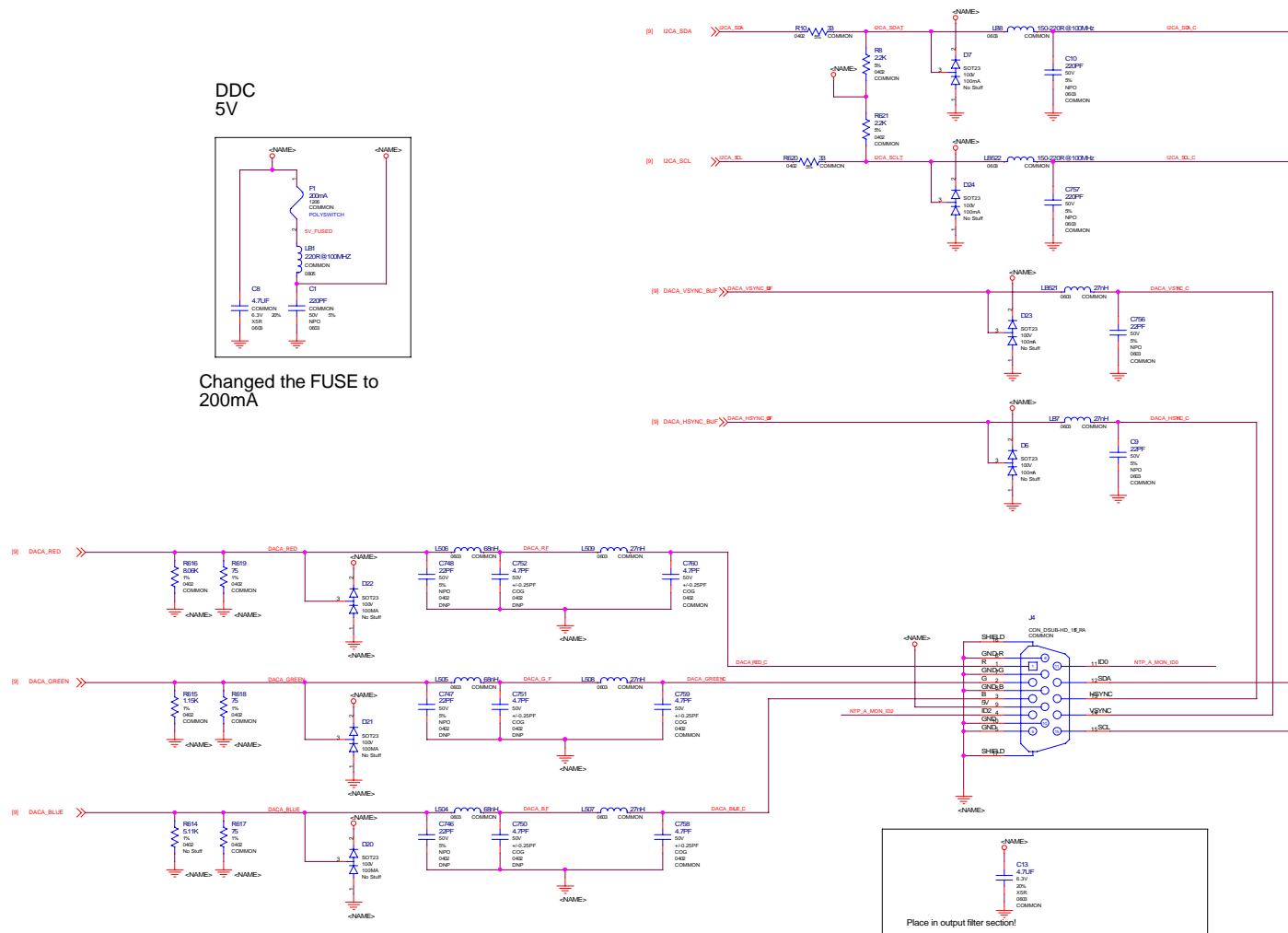
## DACA & DACC Sync Buffers



VGA  
DACA



Changed the FUSE to 200mA

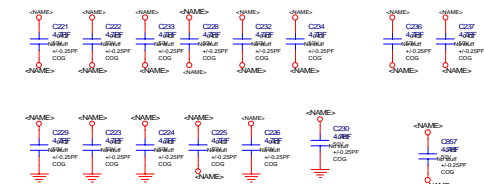
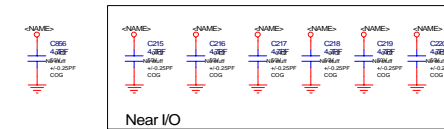


NET_NAME	NET_SPACING_RULE
DACA_R#	20MIL
DACA_G_P	20MIL
DACA_SF	20MIL
DACA_WD_C	20MIL
DACA_GFFINE	20MIL
DACA_RULE_C	20MIL
DACA_VTRM_C	10MIL
DACA_VTRM_C	10MIL

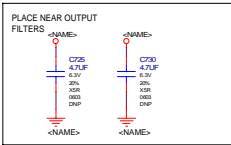
  

	MIN_LINE_WIDTH	VOLTAGE
RV_FUSED	50	5V
RV	50	5V
SDC RV	50	5V
RVN	50	3.3V
RVN	50	5V

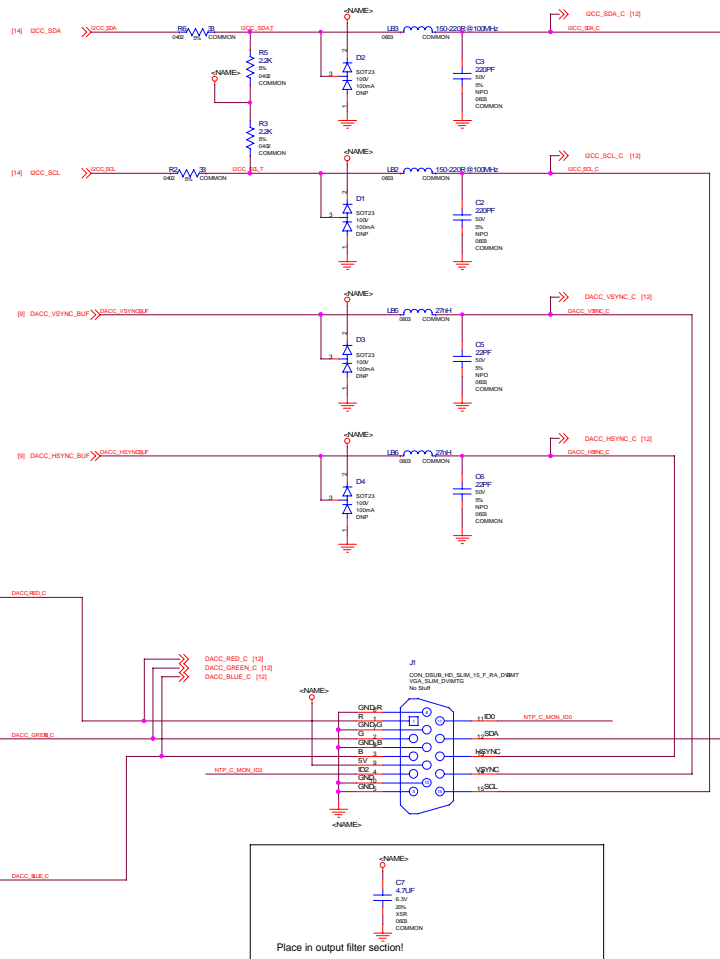
EMI Reserve Cap.



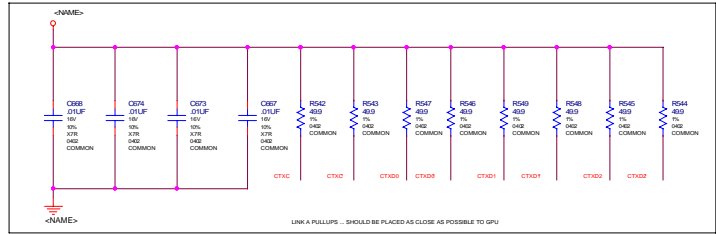
Place in output filter section!

VGA/TV  
DACB/C

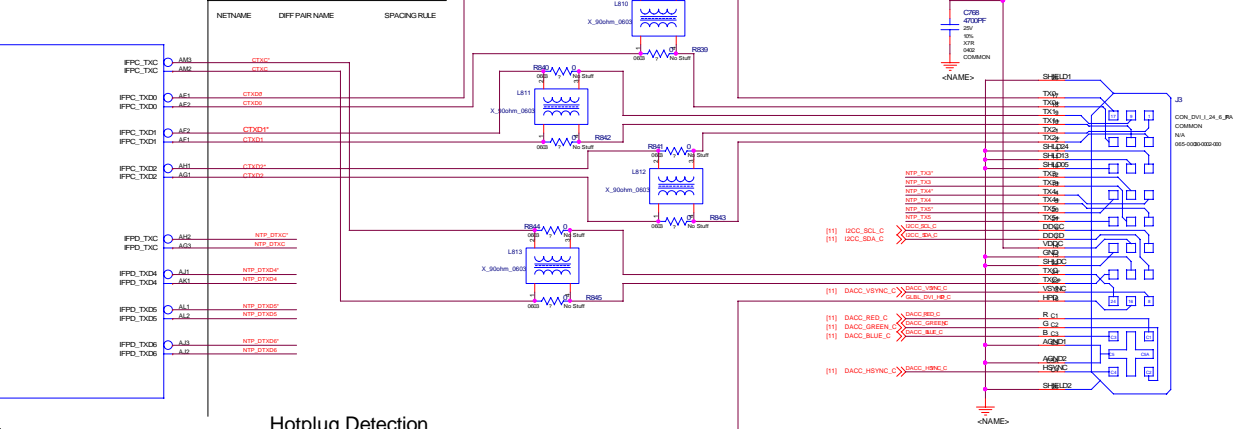
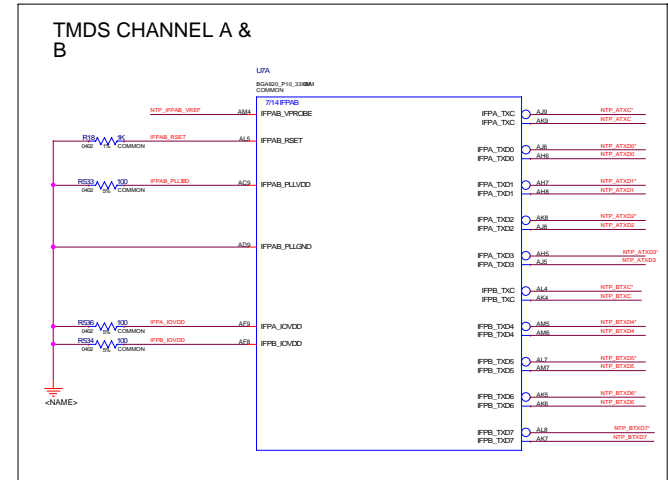
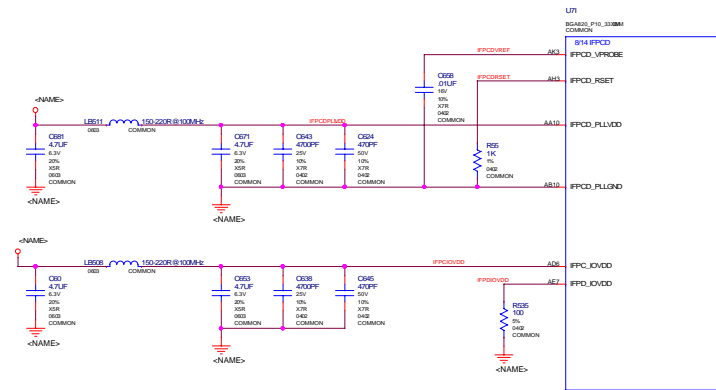
NET_NAME	NET_SPACING_TYPE
DACD_BF	2000L
DACD_G_F	2000L
DACD_SF	2000L
DACD_RED_G	2000L
DACD_GREENB	2000L
DACD_BLUE_G	2000L
DACD_RED_BW	2000L
DACD_GREEN_HQD	2000L
DACD_BLUE_BW	2000L
COU0	2000L
COU1	2000L
PROU0	2000L
DACD_GREEN_C	1000L
DACD_HQD_C	1000L
COU2_C	2000L
COU3_C	2000L
PROU2_C	2000L



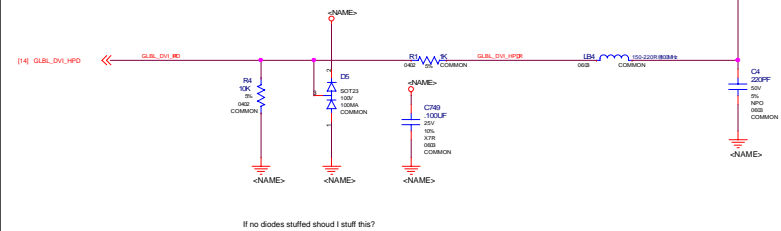
INTERNAL  
TMDS



INTERNAL TMDS ..LINK  
C/D



Hotplug Detection



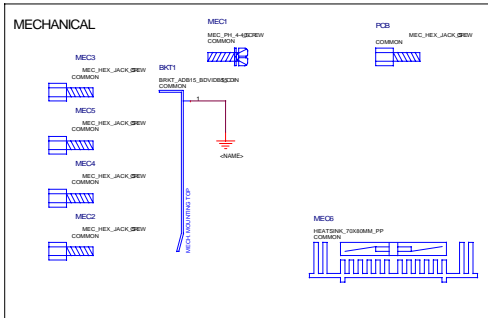
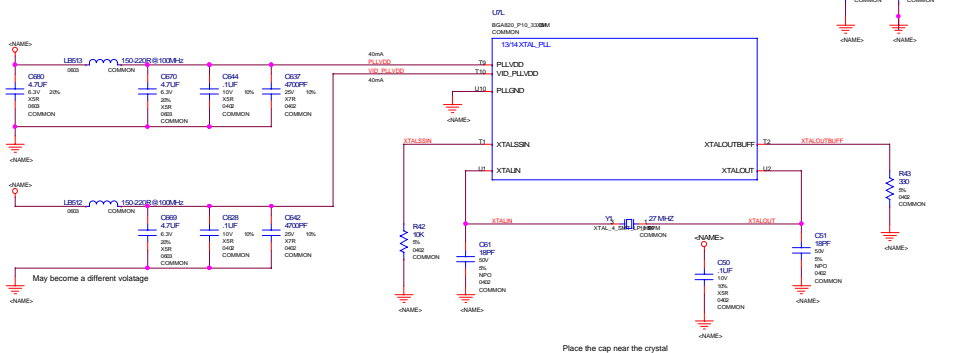
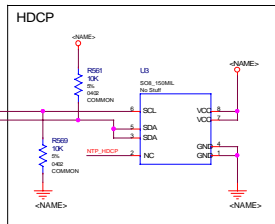
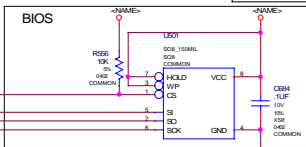
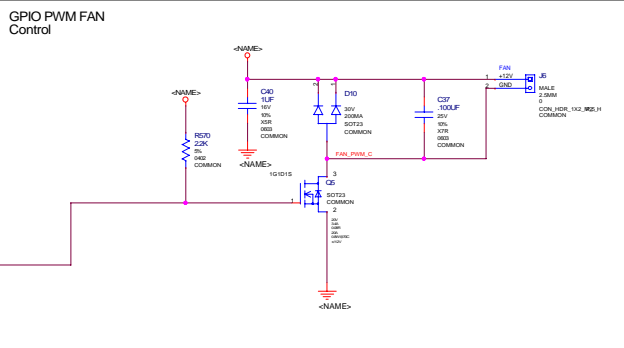
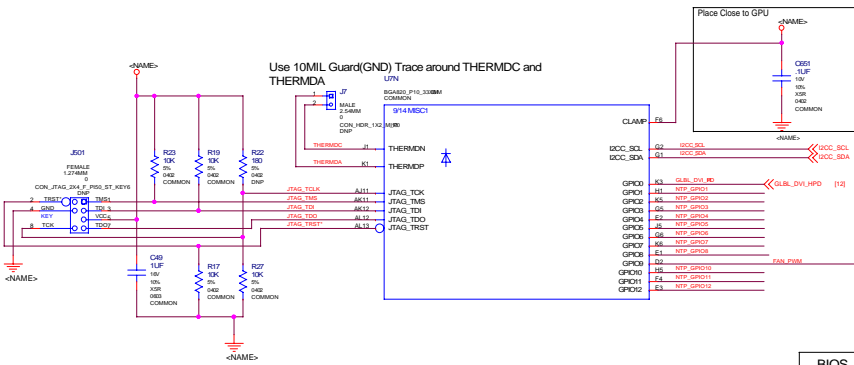
NET	MIN_LINE_WIDTH	VOLTAGE
IFPCDREF	10	3.3V
IFPCDREF	10	3.3V
IFPCDREF	10	3.3V
IFPCDREF	10	3.3V

NETNAME	DIFF PAIR NAME	SPACING RULE
CTXC	CTXC	200M_GDS_300M
CTXC	CTXC	200M_GDS_300M
CTXC	CTXC	200M_GDS_300M
CTXC	CTXC	200M_GDS_300M
CTXC	CTXC	200M_GDS_300M
CTXC	CTXC	200M_GDS_300M
CTXC	CTXC	200M_GDS_300M
CTXC	CTXC	200M_GDS_300M
CTXC	CTXC	200M_GDS_300M
CTXC	CTXC	200M_GDS_300M

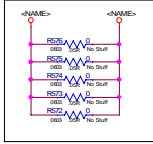


XTAL, GPIO,  
ROM

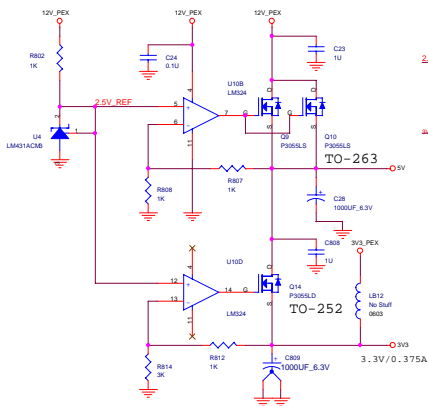
NET	MIN_LIN_WIDTH	NET_SPACING_RULE
XTALIN		200M
XTALOUT		200M
PLUVDD	12	100M
VDD_P1_VDD	12	100M
FAN_F10M		200M
FAN_F10M_B		200M
FAN_F10M_C		200M
TERMSVDD	12	
TERMSVDD	12	



1V2 NVVDD  
bypass

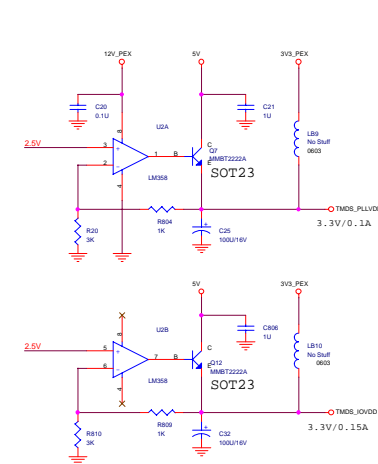


1.2V~1.4V/24A(ambient)  
 $NVDD = 0.8V * (1 + R_t/R_b)$

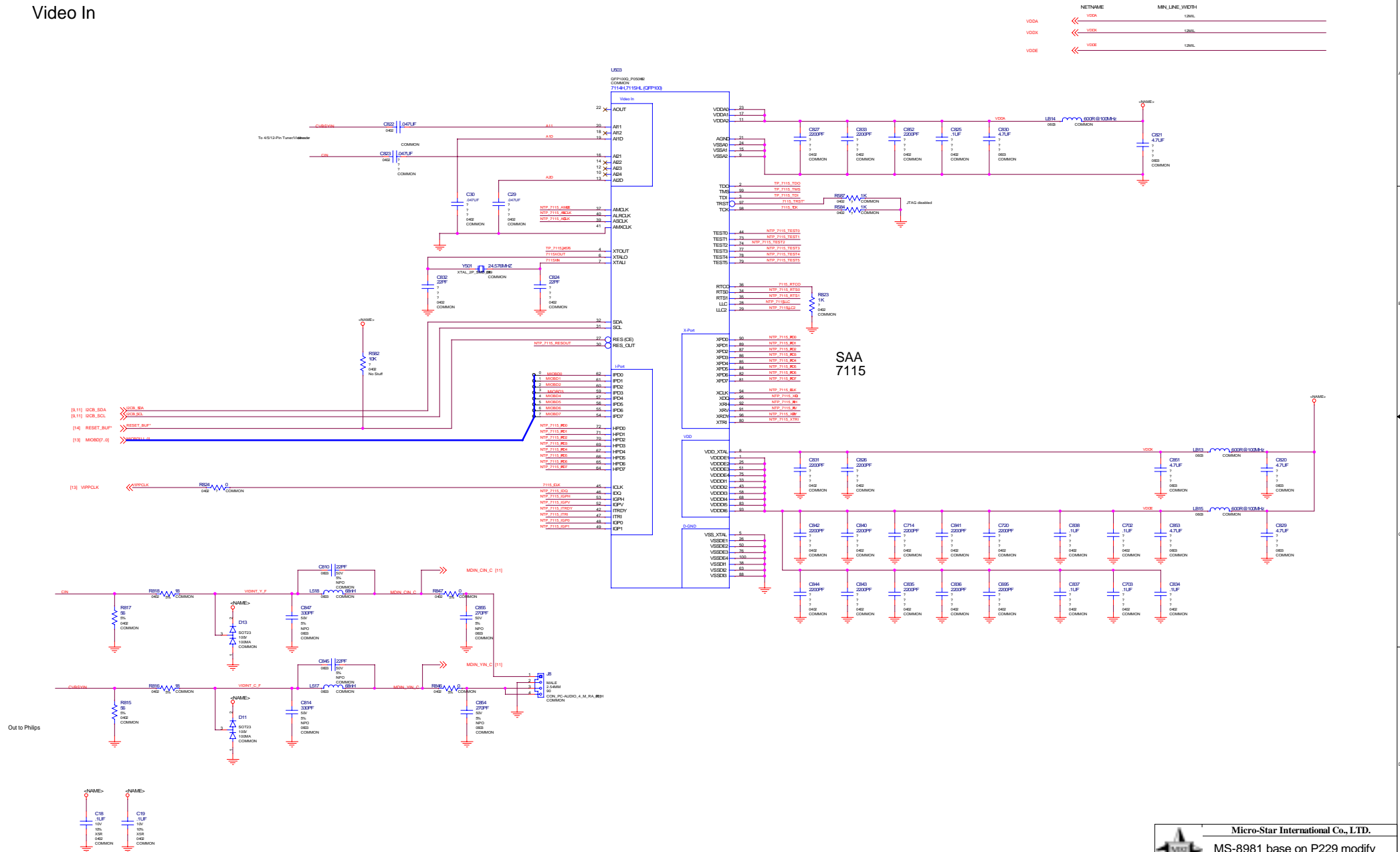
[illegible]

The schematic diagram illustrates the internal power management of the T0-252 IC, featuring two regulators:

- Top Regulator (2.5V REF to FB/VDDO):** This regulator takes a 2.5V REF input and provides a 2.5V output to the FB/VDDO pin. It consists of an LM524 op-amp buffer (U10A) and a P3055LD MOSFET (Q8). The feedback network includes a 1K resistor (R803) and a 100nF capacitor (C26). The MOSFET gate is driven by a 3V3\_PEX signal through a 100nF capacitor (C25). The MOSFET source is connected to ground, and the drain provides the 2.5V output.
- Bottom Regulator (3.3V VDD3):** This regulator takes a 2.5V REF input and provides a 3.3V output to the VDD3 pin. It also uses an LM524 op-amp buffer (U10C) and a P3055LD MOSFET (Q13). The feedback network includes a 3K resistor (R813) and a 100nF capacitor (C33). The MOSFET gate is driven by a 3V3\_PEX signal through a 100nF capacitor (C32). The MOSFET source is connected to ground, and the drain provides the 3.3V output.



Video In



Micro-Star International Co., LTD.

MS-8981 base on P229 modify

Video In

Tuesday, October 26, 2004

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