

P690: GT218, DDR3 MEMORY 64MX16/32MX16

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REV	VARIANT	NVPN	ASSEMBLY
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SANTA CLARA, CA 95050, USA

NV\_PN

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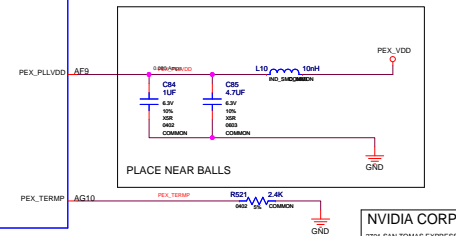
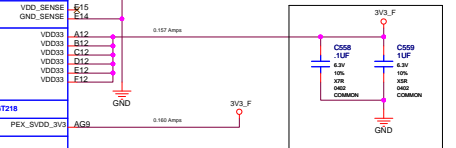
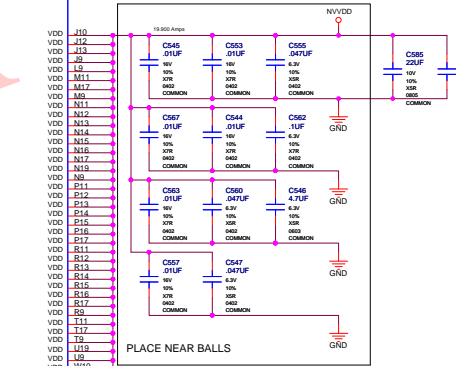
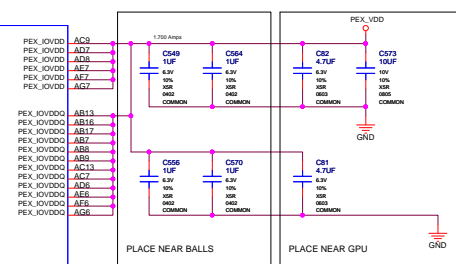
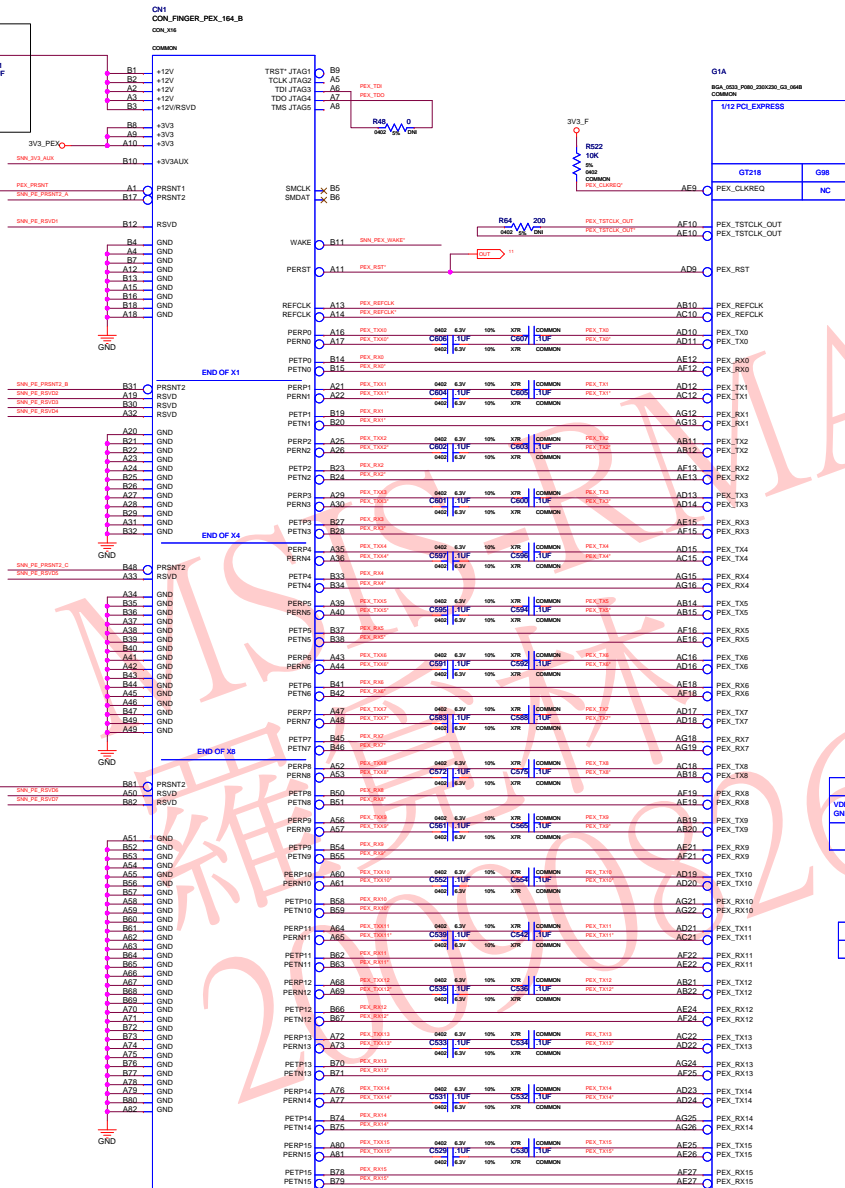
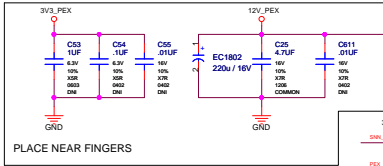
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## PCI Express Interface



**Net Name**

MIN\_WIDTH MAX\_WIDTH

IN PEX\_FRONT

IN PEX\_CENTER

IN PEX\_TEMP

IN PEX\_BACK

12MIL

**Net Name**

VOLTAGE MAX\_CURRENT

IN PEX\_PL1VDD

1.00V 0.050A 12MIL

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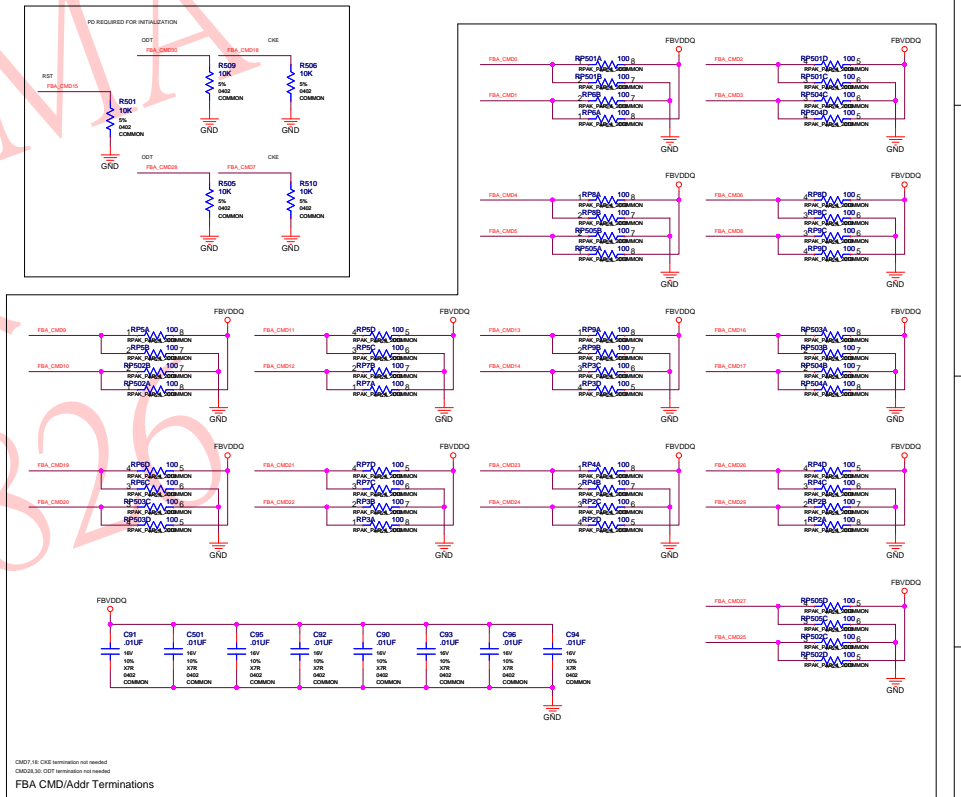
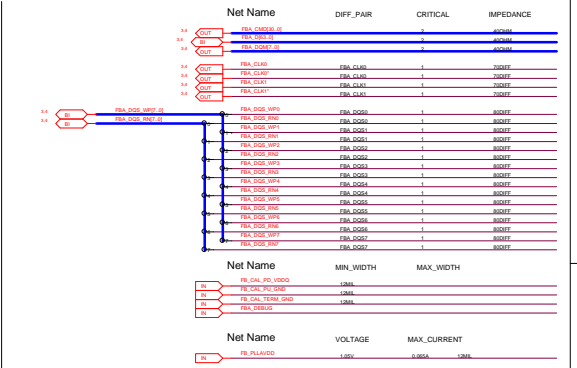
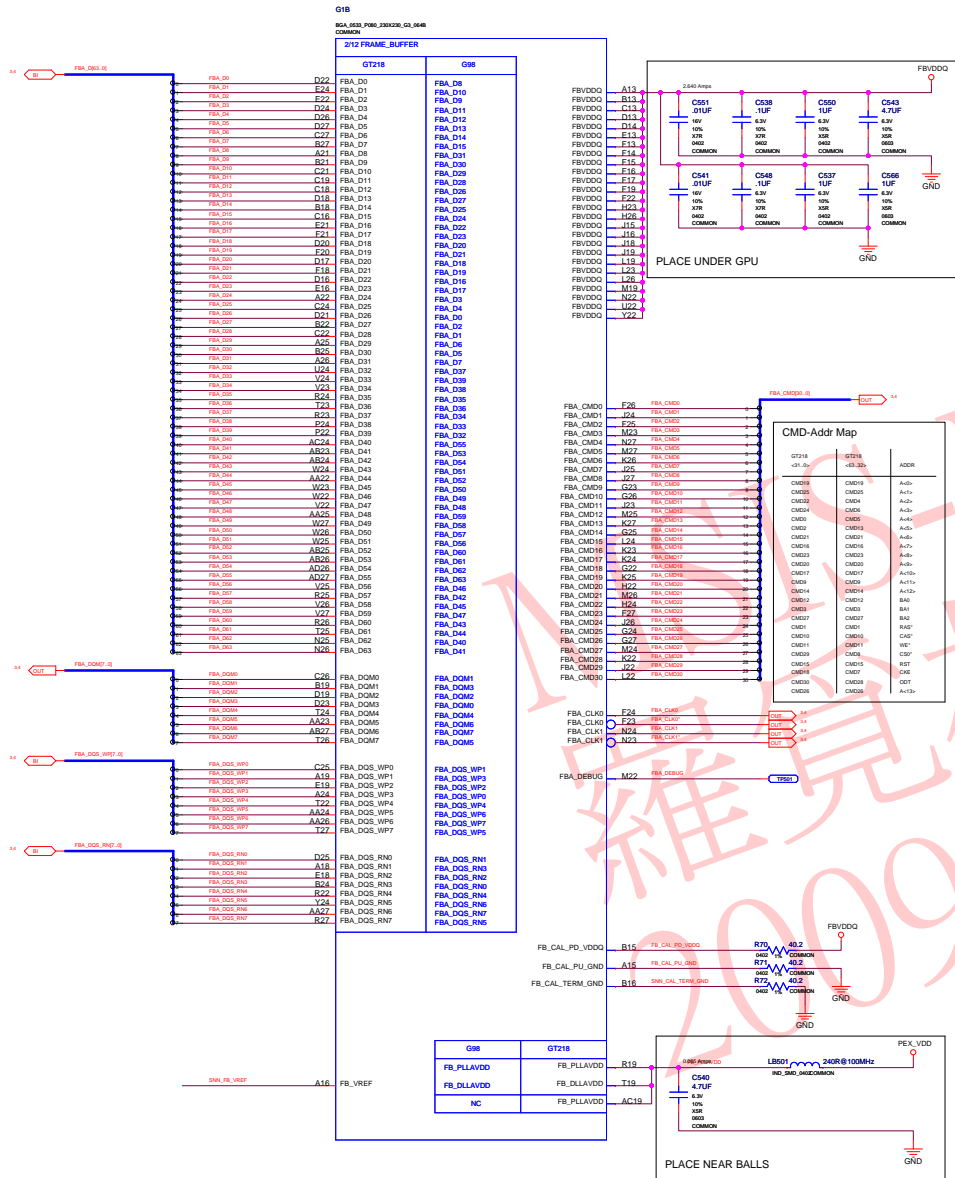
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PAGE DETAIL	PCI Express Interface

<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA	
NV_PN	600-10690-BASE-000 A



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# Frame Buffer Interface

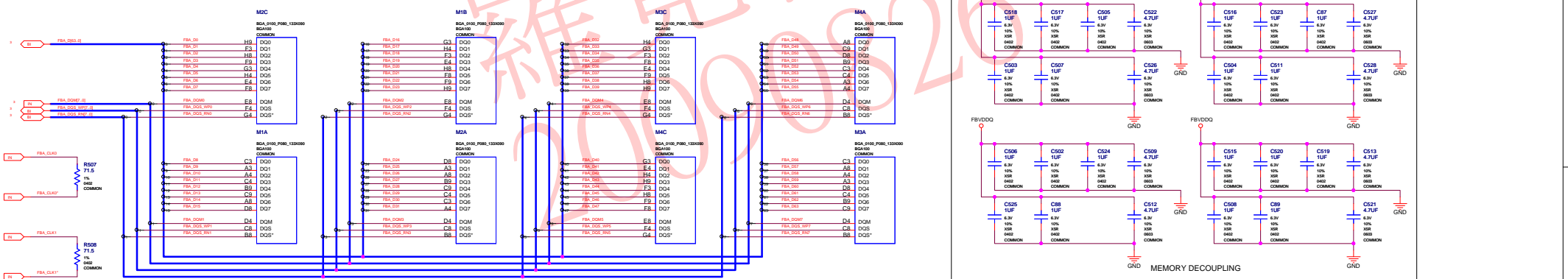
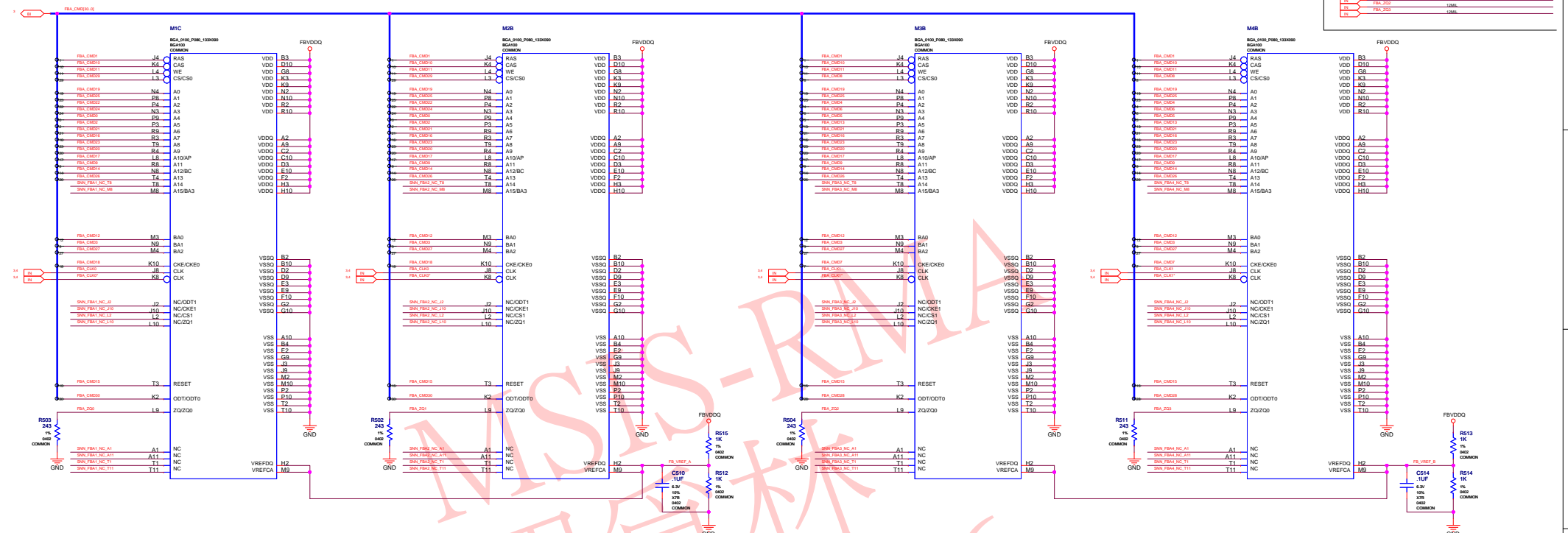


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Frame Buffer Interface

**FBA CMD/Addr Terminations**


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## DDR3 Memories



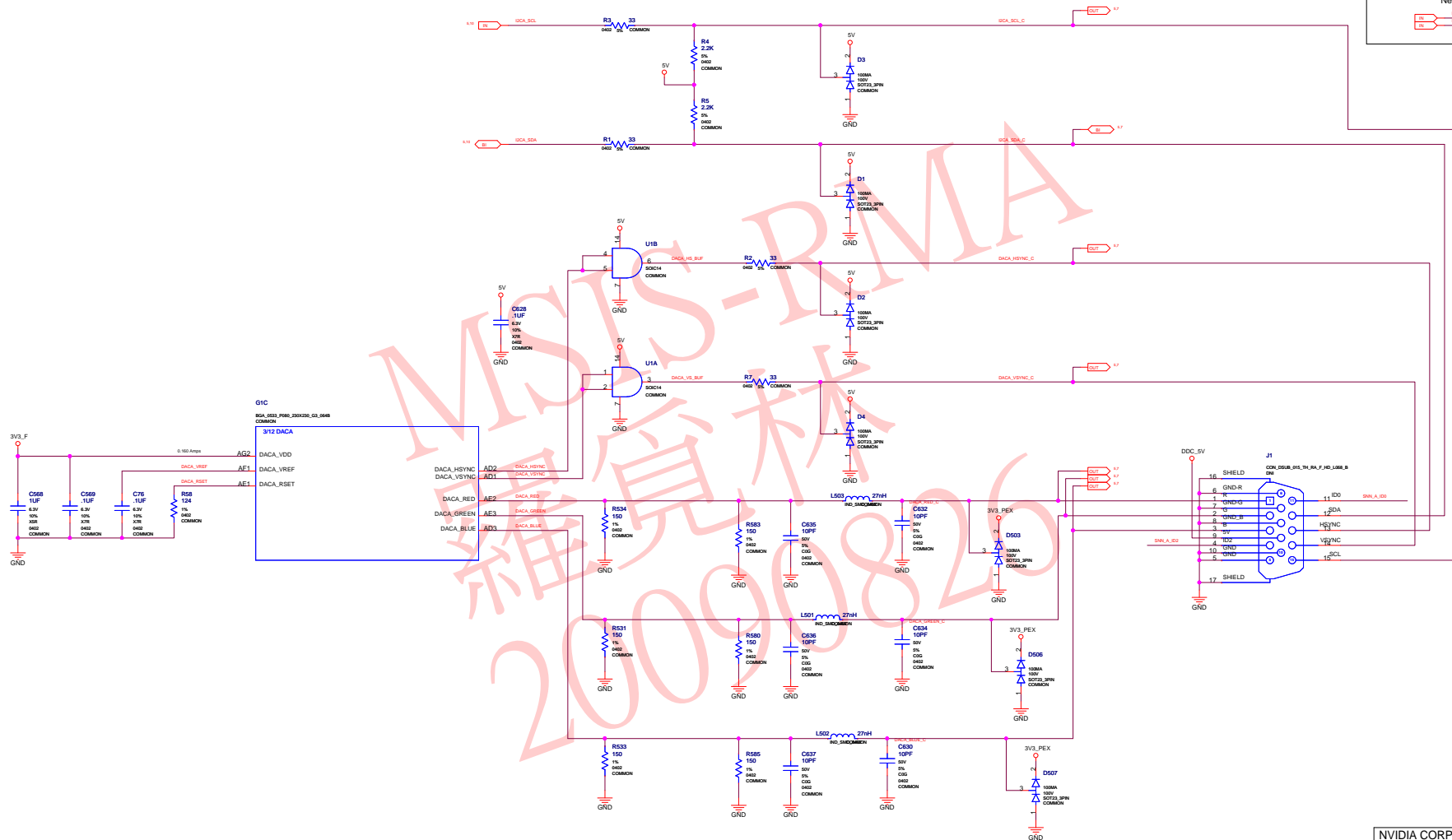
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IN	FBA_ZQ2	120u	
IN	FBA_ZQ3	120u	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DDR3 Memories

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## DAC A Slim VGA



Net Name		CRITICAL	IMPEDANCE
5.7	IN1 DQCA_RED	1	50OHM
	IN1 DQCA_GREEN	1	50OHM
	IN1 DQCA_BLUE	1	50OHM
	IN1 DQCA_RED_C	1	50OHM
	OUT1 DQCA_GREEN_C	1	50OHM
5.7	IN2 DQCA_YELLOW	2	50OHM
	IN2 DQCA_BLUE	2	50OHM
	IN2 DQCA_VIOLET	2	50OHM
	OUT2 DQCA_VIOLET_C	2	50OHM
	OUT2 DQCA_GREEN_C	2	50OHM
Net Name		MRL_WIDTH	MAX_WIDTH
5.10	IN1 DQCA_RED		
	IN1 DQCA_BLUE		
	OUT1 DQCA_RED_C		
5.7	IN2 DQCA_BLUE		
	IN2 DQCA_VIOLET		
	OUT2 DQCA_VIOLET_C		
Net Name		VOLTAGE	MAX_CURRENT
IN1	DQCA_VIOLET	1.2V	1.000A
	DQCA_RED		1.000A

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PAGE DETAIL	DAC A Sim VGA

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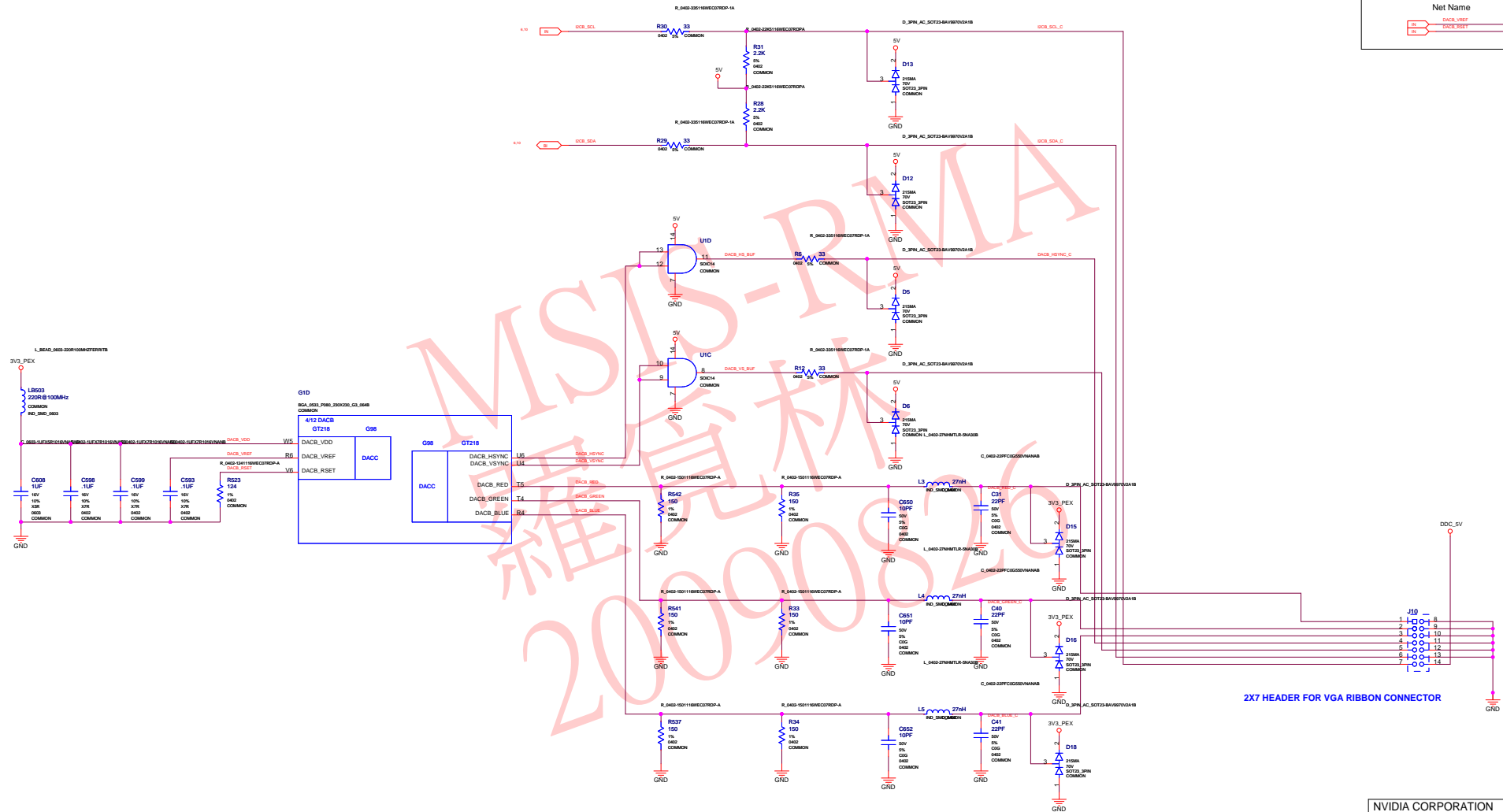
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## DAC B VGA Header



Net Name		CRITICAL	IMPEDANCE
IN	DACR_NEO	1	50ΩIN
IN	DACR_GREEN	1	50ΩIN
IN	DACR_BLUE	1	50ΩIN
IN	DACR_NEO_C	1	50ΩIN
IN	DACR_GREEN_C	1	50ΩIN
IN	DACR_BLUE_C	1	50ΩIN
IN	DACR_TVINIC	2	50ΩIN
IN	DACR_TVINIC_C	2	50ΩIN
IN	DACR_TVINIC_C	2	50ΩIN
IN	DACR_TVINIC_C	2	50ΩIN
IN	DACR_HS_BUF	2	50ΩIN
IN	DACR_HS_BUF	2	50ΩIN

Net Name		MIN_WIDTH	MAX_WIDTH
8,10	IN	UCB_SCL	
8,10	BI	UCB_SDA	
	IN	UCB_SCL_C	
	IN	UCB_SDA_C	

Net Name	VOLTAGE	MAX_CURRENT
IN	DACB_VREF	1.2V
IN	DACB_ASET	125mA

## 2X7 HEADER FOR VGA RIBBON CONNECTOR

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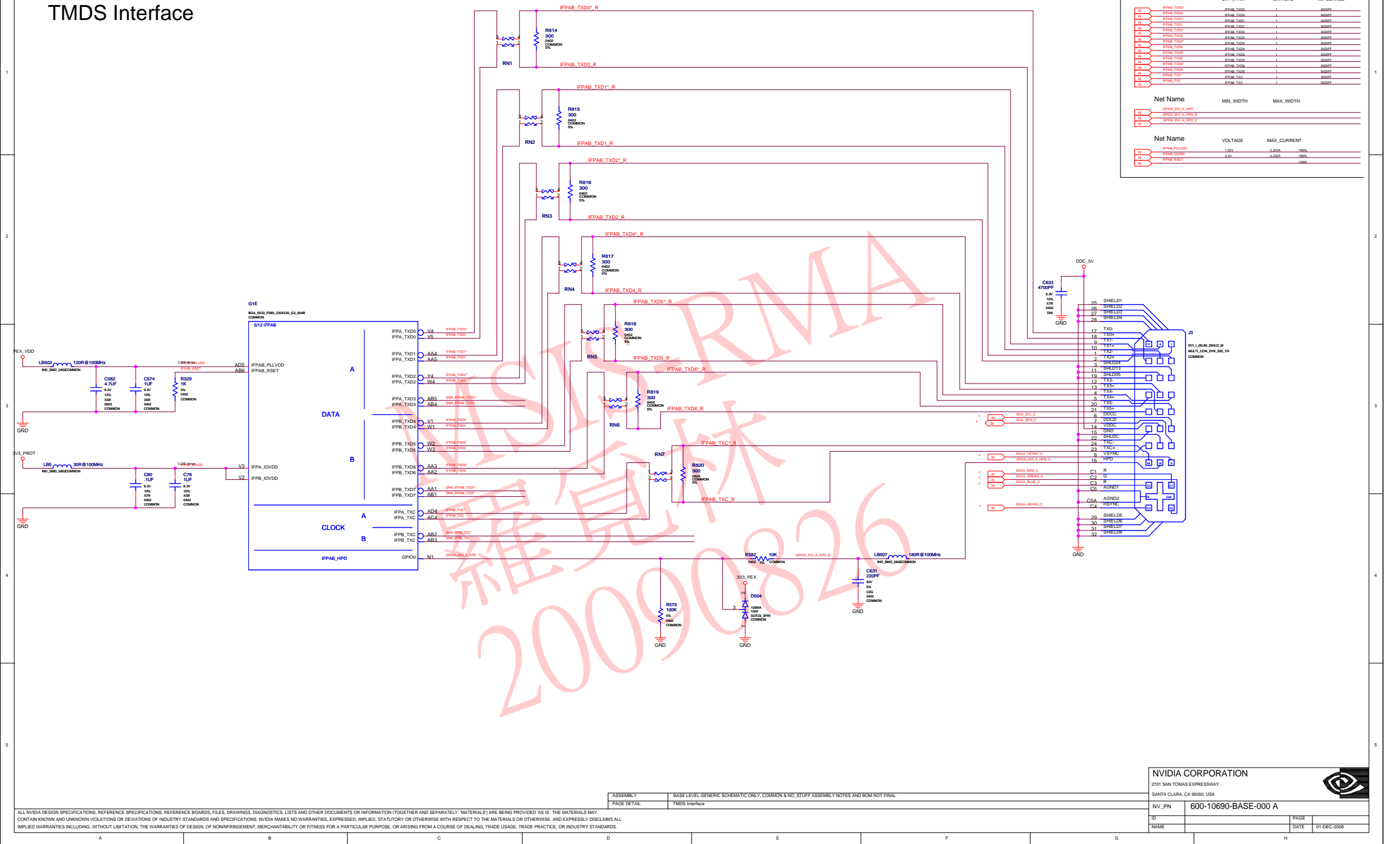
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NAME		DATE	01-DEC-2008

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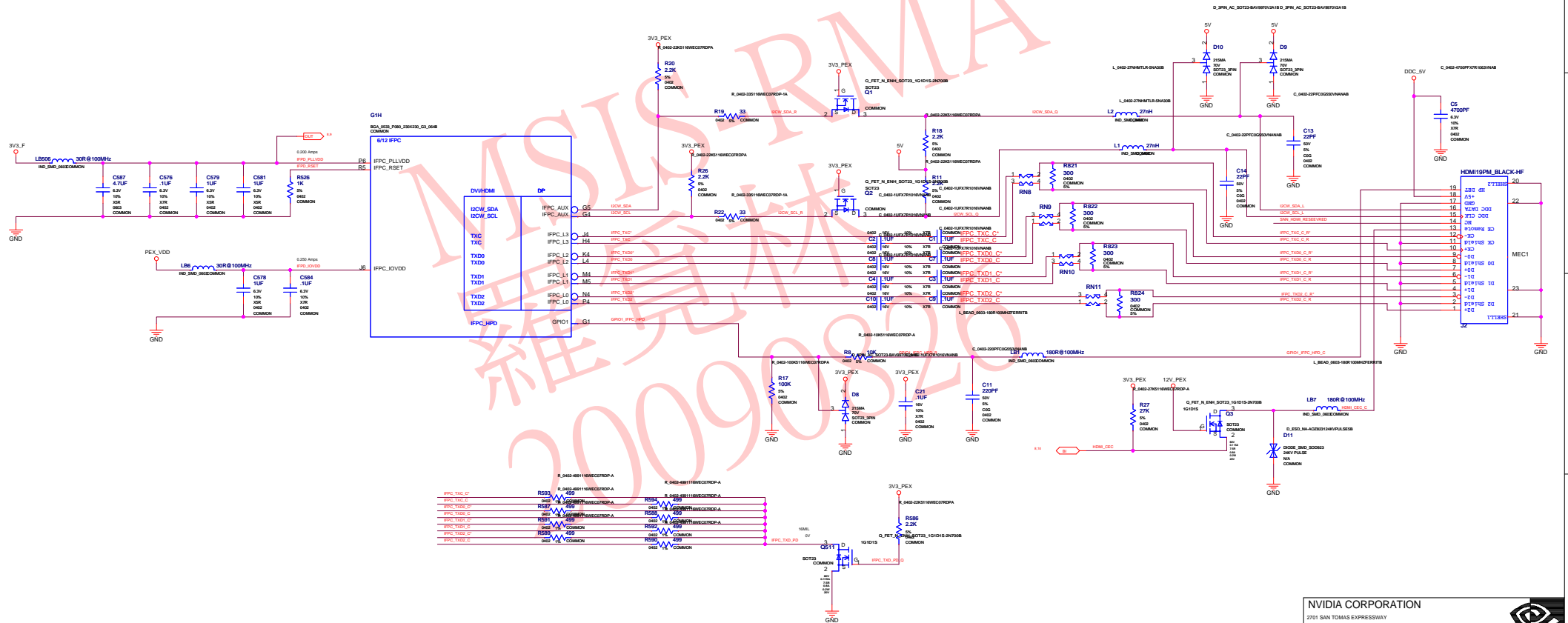
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PAGE DETAIL	DAC B VGA Header

## TMD5 Interface



## HDMI Connector

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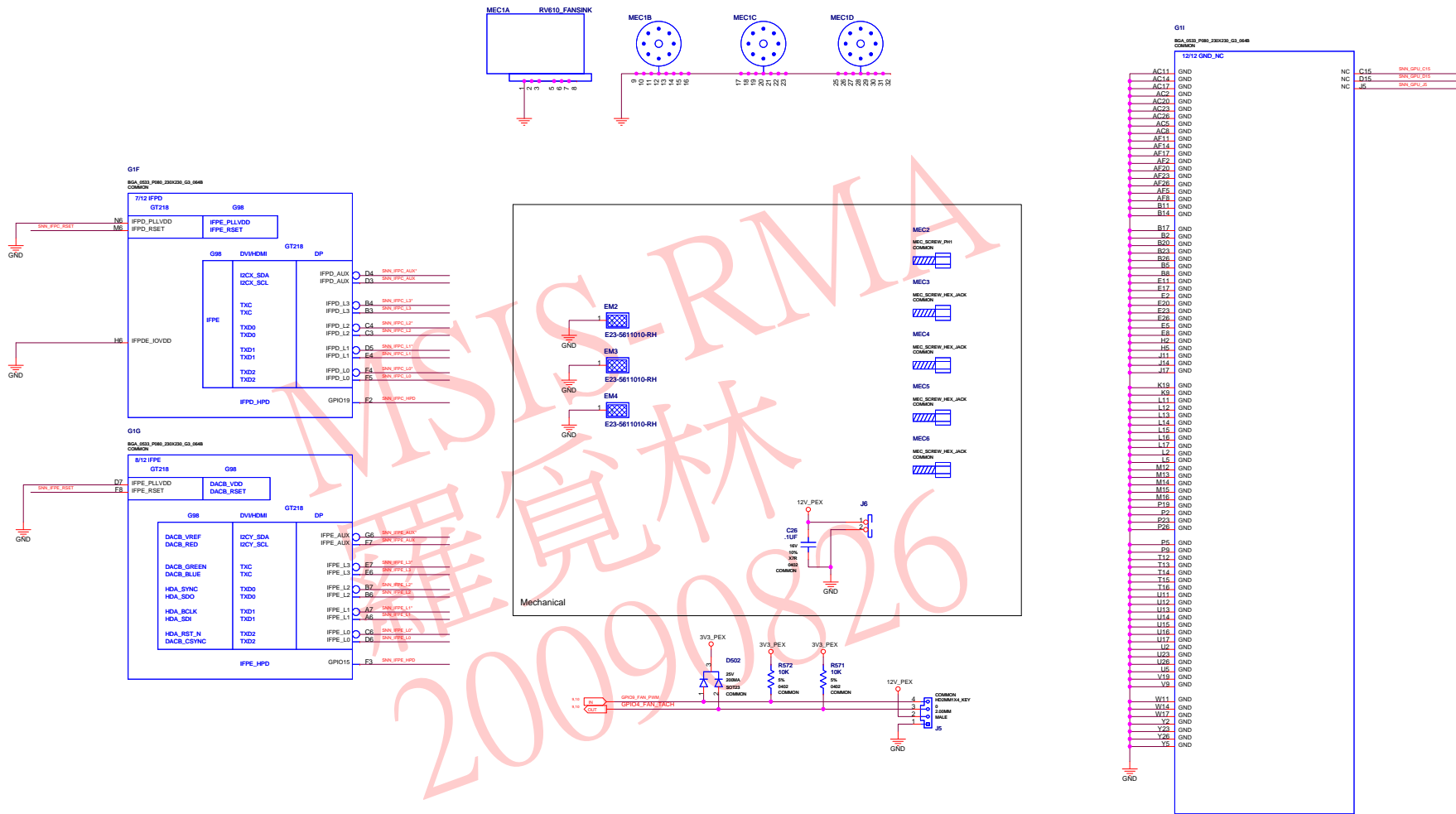
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IFPC, IFPE Interface, Fan, Mechanical

Net Name		VOLTAGE	MAX_CURRENT
IN	IFPC_PL1VDD	3.3V	0.200A
IN	IFPC_PL1VDD	1.05V	100mA

Net Name		MIN_WIDTH	MAX_WIDTH
IN	IFPC_FAN_TACH		
OUT	IFPC_FAN_PWM		



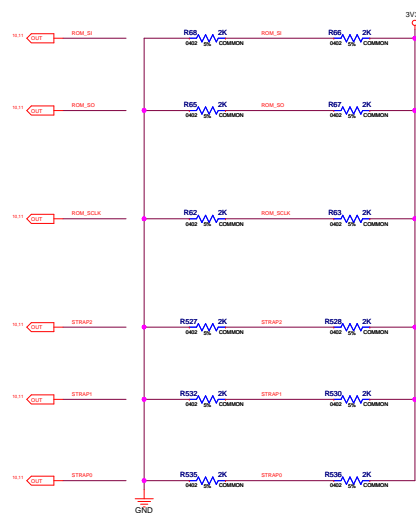
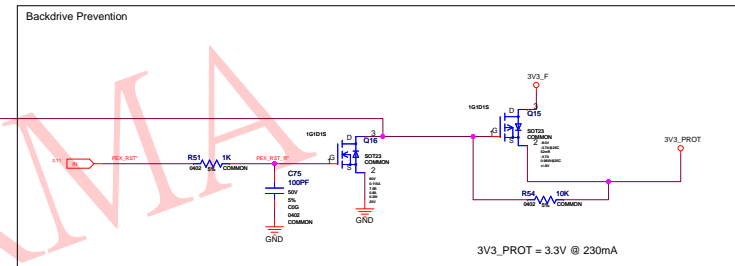
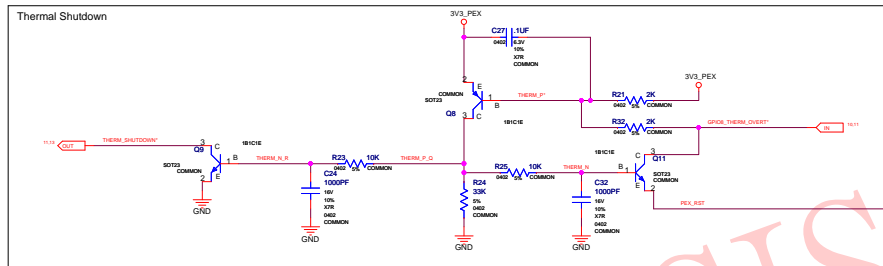
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PAGE DETAIL	IFPC, IFPE Interface, Fan, Mechanical



## Thermal Protection, IFP\_IOVDD, Straps



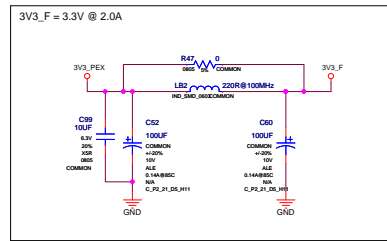
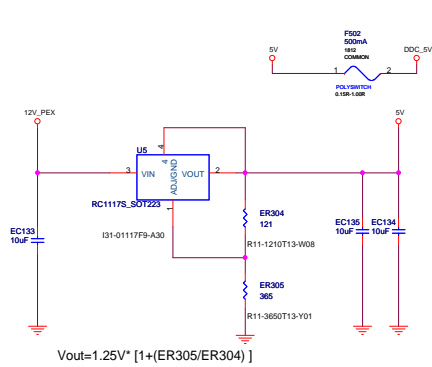
G7218 Straps		Values		Multilevel Straps	
01	RAMEQ[02]	0000	Enable		
		0001	Sampling Micro		
		0010	Overwrite		
01	RAMEQ[03]	0011	High		
		0000	Normal		
	RAMEQ[05]				
				5K to GND	0000
				10K to GND	0001
				15K to GND	0010
				20K to GND	0011
				25K to GND	0100
				30K to GND	0101
				35K to GND	0110
				40K to GND	0111
				5K to VCC	1000
				10K to VCC	1001
				15K to VCC	1010
				20K to VCC	1011
				25K to VCC	1100
				30K to VCC	1101
				35K to VCC	1110
				40K to VCC	1111
02	FC[0]	0	250M (Default)		
01	SMB_ALT_ADDR	0	0x6F		
		1	0x6C		
00	VGA_DEVICE	0	Onboard 800		
		1	Onboard 300		
01	PCI_DEVICE_EXT	0	07279-300-A1		
02	SUB_VENDOR	0	No BIOS		
		1	BIOS		
01	SLOT_GA_CFG	0	Disable		
		1	Enable		
00	PEX_PCI_EN_TERR100	0	Disable		
		1	Enable		
03	PCI_DEVICE1	0000	G7279-300-A1		
01	PCI_DEVICE2				
01	PCI_DEVICE3				
01	PCI_DEVICE4				
03	3XG_FADCFG_LUT_ADDR[0]	0000	DDI070_DEFAULT	1000	DDI070_3XGHSR
		0001	MOBILE_DEFAULT	1001	MOBILE_3XGHSR
		0010	MOBILE_3XGHSR_LAMP	1010	MOBILE_3XGHSR_LAMP
		0011	MOBILE_3XGHSR_LAMP	1011	MOBILE_3XGHSR_LAMP
		0100	MOBILE_3XGHSR	1100	MOBILE_3XGHSR
		0101	MOBILE_3XGHSR_3XGHSR	1101	MOBILE_3XGHSR_3XGHSR
		0110	MOBILE_3XGHSR_3XGHSR	1110	MOBILE_3XGHSR_3XGHSR
		0111	MOBILE_3XGHSR_3XGHSR	1111	MOBILE_3XGHSR_3XGHSR
02	USER[0]	0000	Default		
02	USER[1]				
02	USER[2]				
02	USER[3]				
02	USER[4]				
02	USER[5]				

BT218 Straps		
GU Mode		
Bit Signal	Values	
PCU_DEVICE_EXT	0	GT218-300A1
PCU_417	0	277 (Default)
SIGF_PANDFCG_LUT_ADDR0E	0000	OSSTOP_DEFAULT
	0001	MOBILE_DEFAULT
	0010	MOBILE_JITTER_LOOP
	0011	MOBILE_JITTER_LOOP
	0100	MOBILE_JITTER_LOOP
	0101	MOBILE_JITTER_LOOP
	0110	MOBILE_JITTER_LOOP
	0111	MOBILE_JITTER_LOOP
	1000	OSSTOP_JITTER
	1001	MOBILE_JITTER_LOOP
	1010	MOBILE_JITTER_LOOP
	1011	MOBILE_JITTER_LOOP
SIGF_PANDFCG_LUT_ADDR0F	1100	MOBILE_JITTER_LOOP
	1101	MOBILE_JITTER_LOOP
	1110	MOBILE_JITTER_LOOP
	1111	MOBILE_JITTER_LOOP
SIGF_PANDFCG_LUT_ADDR1E		
SIGF_PANDFCG_LUT_ADDR1F		

GT218 Straps PM Mode		
Bit Signal	Values	
POL_DEV[DEV_EXT]	0	GT218-900-A1
KICK_417	0	272727 OR 417417
POL_DEV[DEV2]	0	GT218-900-A1
RANCFG[2]	0000	Elipse
	0001	Samsung Micron
	0010	Onedrive
	0011	Hynix
	0100	Memops
RANCFG[1]		
RANCFG[0]		

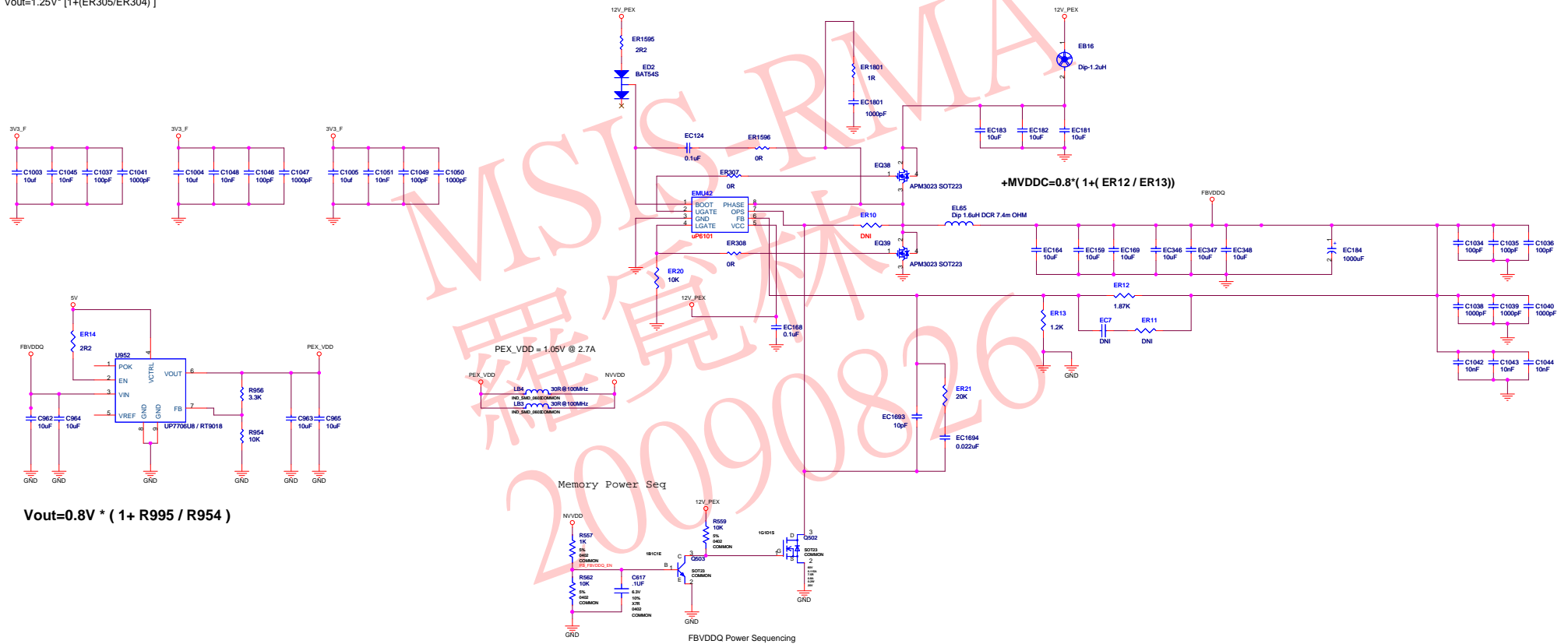
Mode	REFOREF1
ML5	Stall
ML3	No stall
PM	Stall one

Power Supply I: FBVDD/Q, PEX\_VDD, 5V, 3V3\_F



Net Name	MIN_WIDTH	MAX_WIDTH
PS_PU_ADU	10000	10000
PS_PU_PDR_B	10000	10000
PS_PU_PDR	10000	10000
PS_PU_PDR_F0	10000	10000
PS_PU_PDR_F1	10000	10000
PS_PU_PDR_F2	10000	10000
PS_PU_PDR_F3	10000	10000
PS_PU_PDR_F4	10000	10000
PS_PU_PDR_F5	10000	10000
PS_PU_PDR_F6	10000	10000
PS_PU_PDR_F7	10000	10000
PS_PU_PDR_F8	10000	10000
PS_PU_PDR_F9	10000	10000
PS_PU_PDR_F10	10000	10000
PS_PU_PDR_F11	10000	10000
PS_PU_PDR_F12	10000	10000
PS_PU_PDR_F13	10000	10000
PS_PU_PDR_F14	10000	10000
PS_PU_PDR_F15	10000	10000
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PS_PU_PDR_F17	10000	10000
PS_PU_PDR_F18	10000	10000
PS_PU_PDR_F19	10000	10000
PS_PU_PDR_F20	10000	10000
PS_PU_PDR_F21	10000	10000
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PS_PU_PDR_F322	10000	10000
PS_PU_PDR_F323	10000	10000
PS_PU_PDR_F324	10000	10000
PS_PU_PDR_F325</		

Net Name	VOLTAGE	MAX_CURRENT
5V	5V	
DDC_5V	5V	0.310A 120mV
DDC_5V	5V	0.1150A 120mV
3V3_F	3.3V	2.0A 160mV
3V3_FUSE	3.3V	0.5500A 120mV
PEX_VDD	1.05V	2.7A 240mV
FBVDDQ	1.8V	10.5A 300mV



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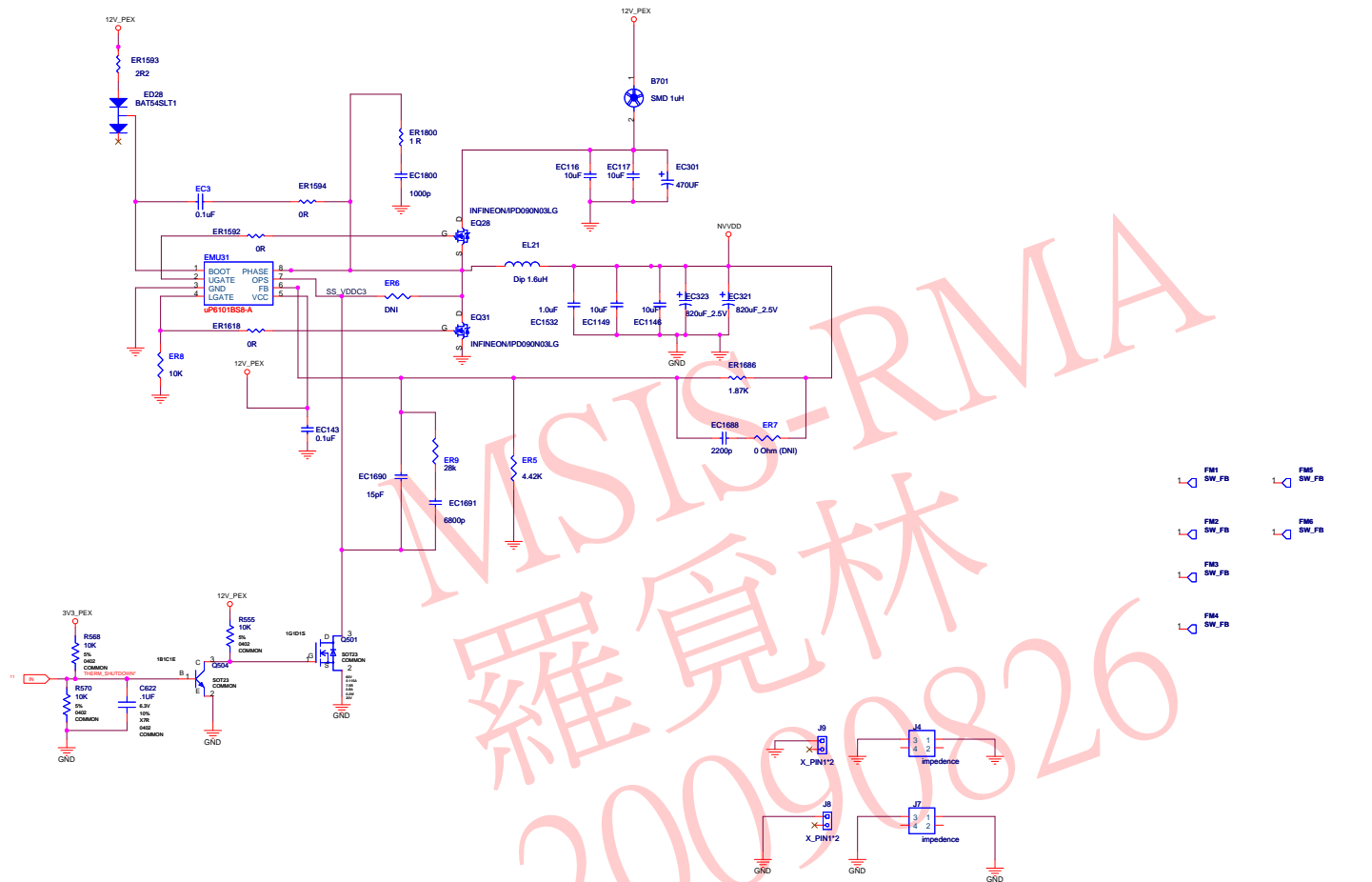
ID		PAGE	
NAME		DATE	01-DEC-2008

[illegible]

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply I: FBVDDIQ, PEX_VDD, 5V, 3V3_F

## Power Supply II: PLLVDD, NVVDD



NVVDD = 0.9V @ 11.1A

NVDD w/NVDDc->PEX\_VDD = 12.8A  
 NVDD = 0.95V @ 12.3A  
 NVDD w/NVDDc->PEX\_VDD = 15.0A  
 NVDD = 1.0V @ 13.5A  
 NVDD w/NVDDc->PEX\_VDD = 16.2A  
 NVDD = 1.05V @ 14.8A  
 NVDD w/NVDDc->PEX\_VDD = 17.5A

[illegible]

Net Name	VOLTAGE	MAX_CURRENT	POWER_NET
12V_PEX	12V	5.5A	TRUE
3V3_PEX	3.3V	3.0A	TRUE
NVDD	1.1V	17.5A	TRUE

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply II: PLLVDD, NVVDD

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A horizontal number line with several tick marks. A vertical line segment is drawn from the second tick mark to the fourth tick mark, labeled 'H' below it.

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