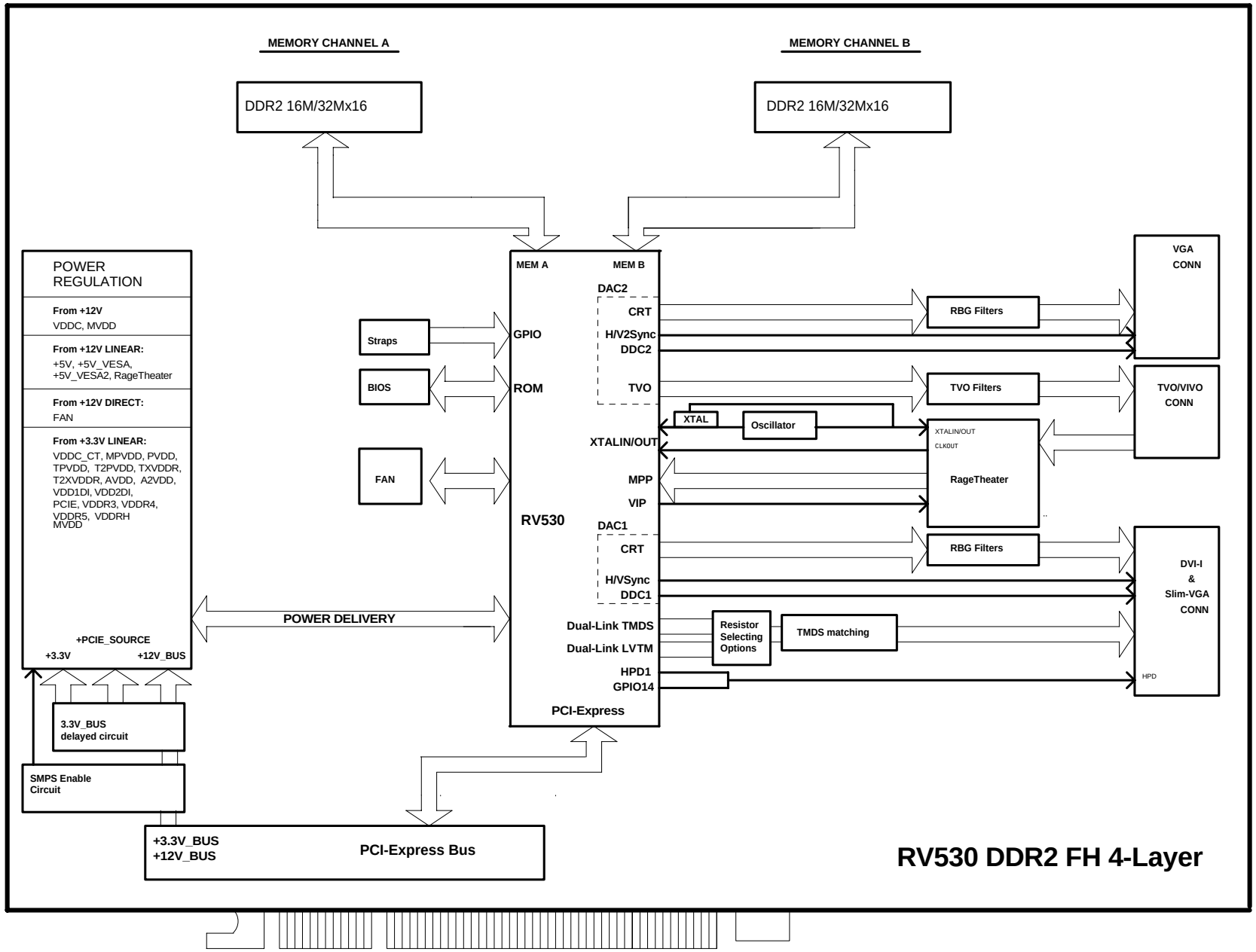

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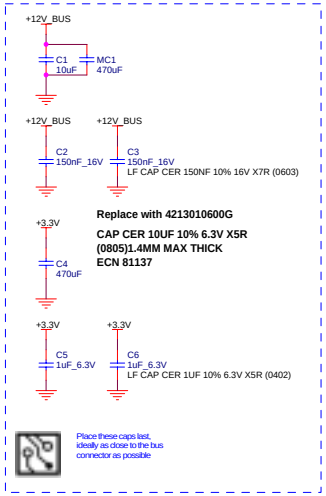
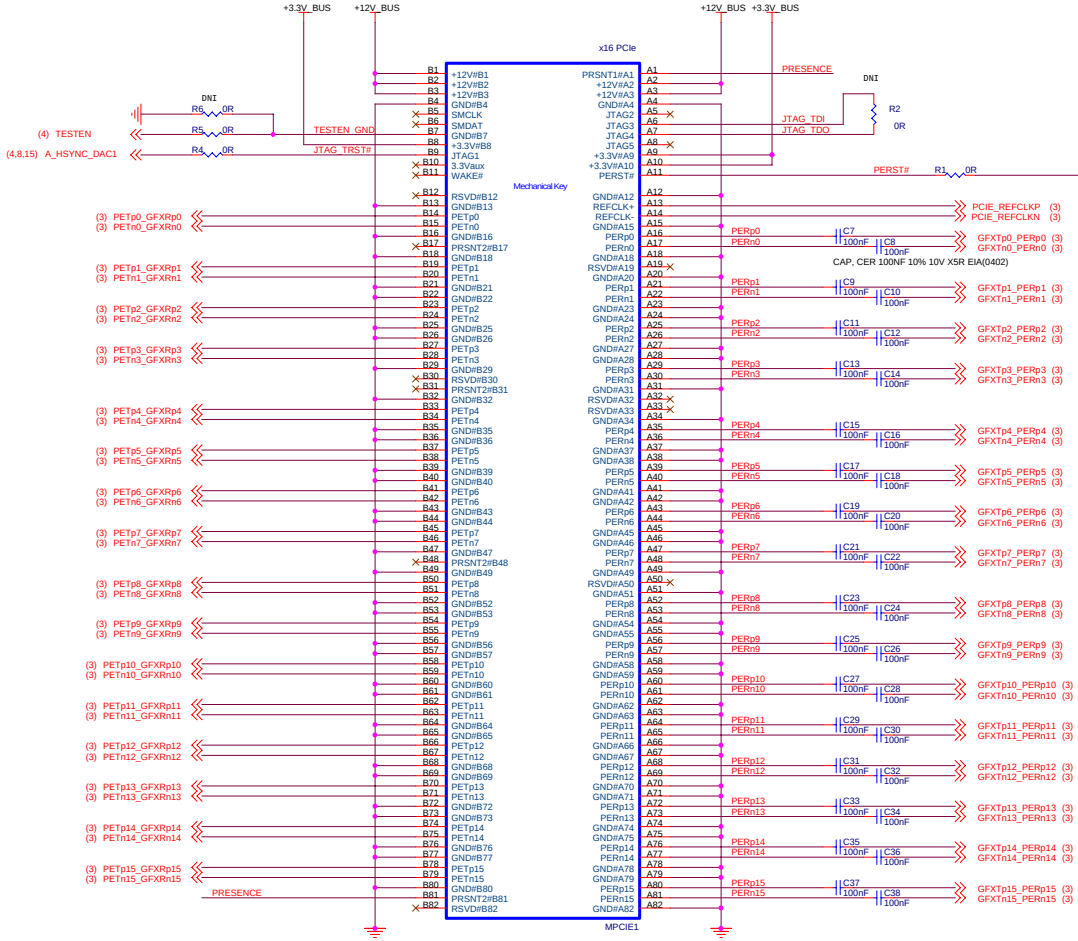
PCI-EXPRESS EDGE CONNECTOR





Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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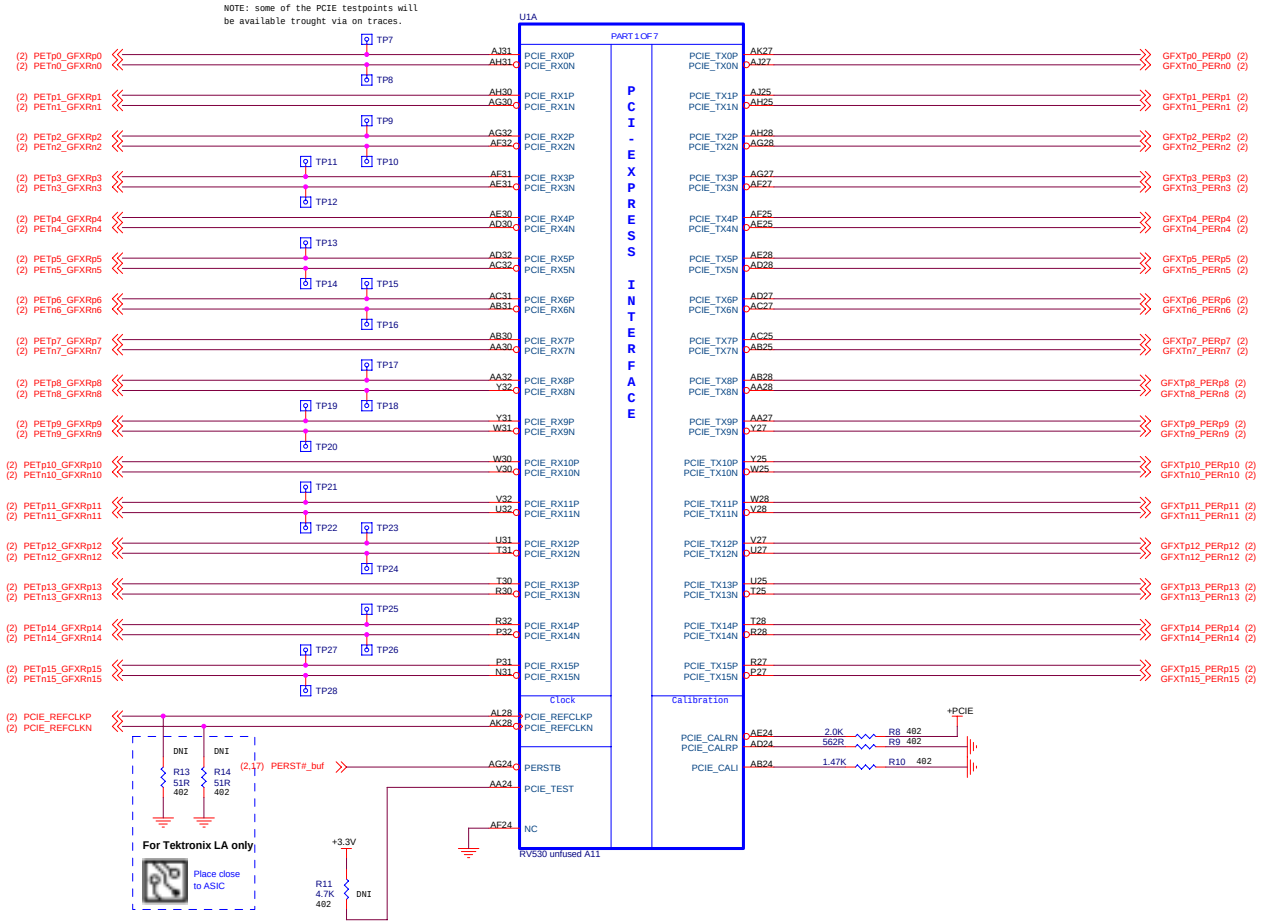

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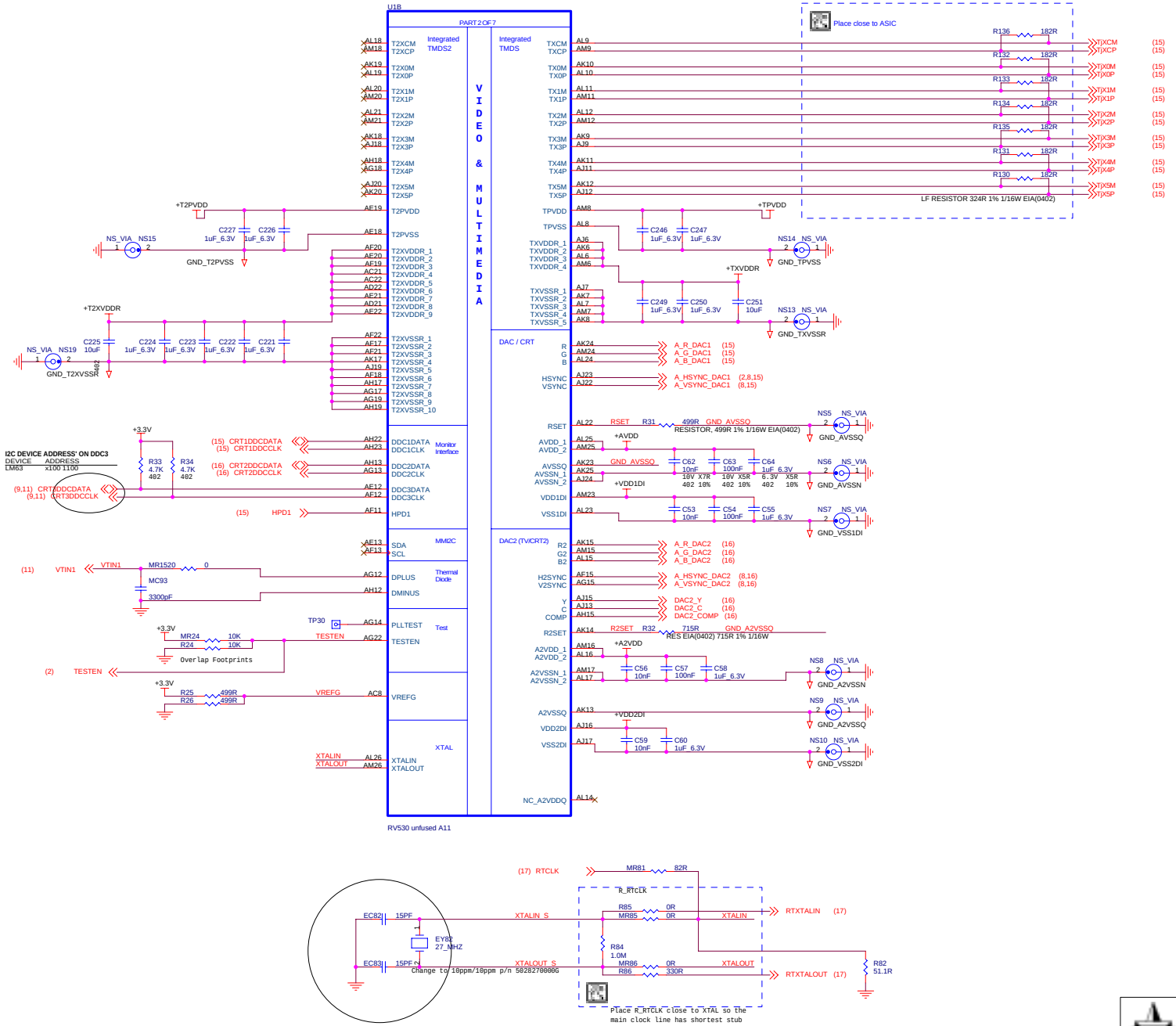

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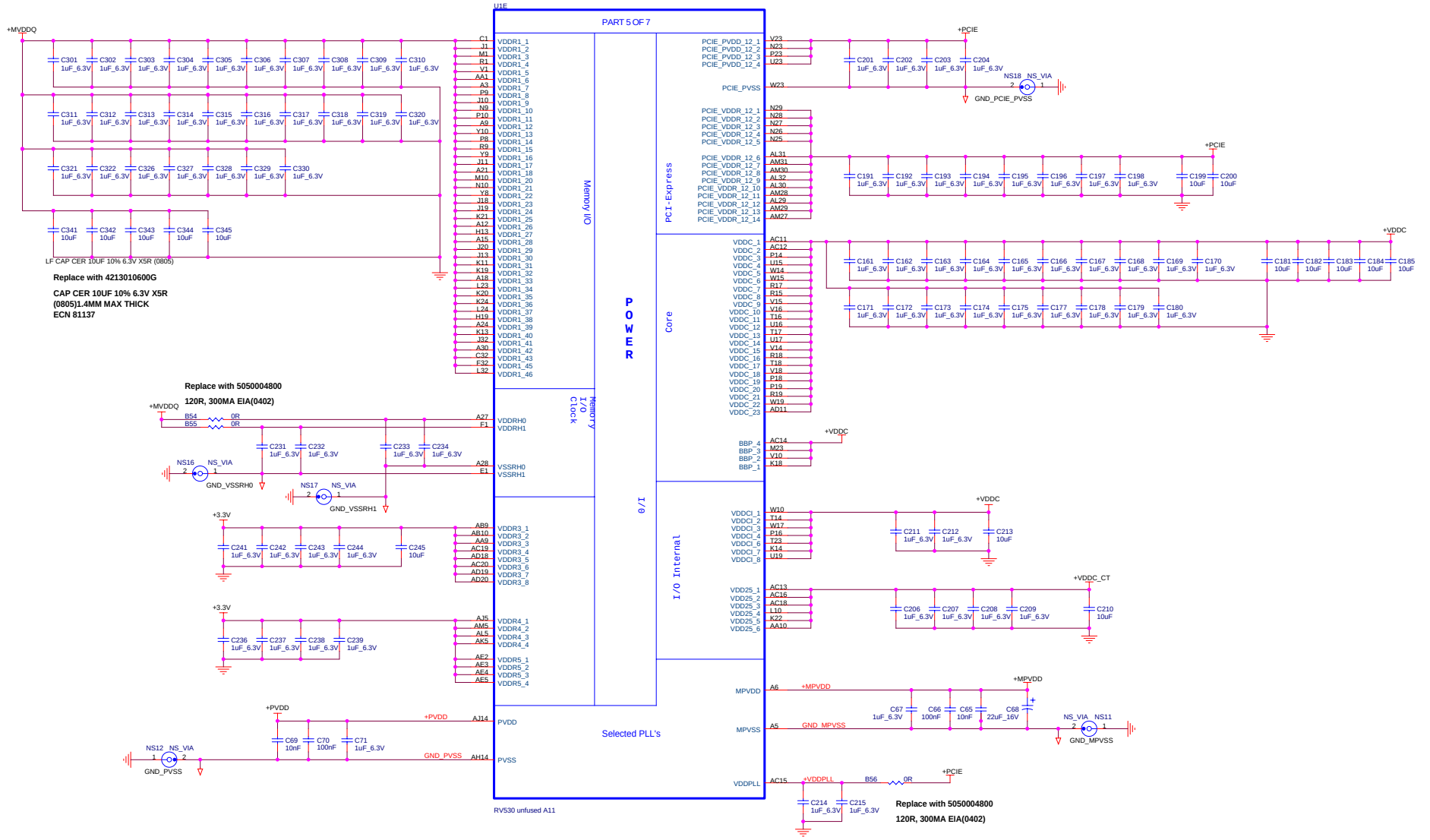
U1E
PART 5 OF 7
POWER
Memory I/O
PCI-Express
Core
I/O
Memory I/O Clock
I/O Internal
Selected PLL's
+MVDDQ
LF CAP CER 10UF 10% 6.3V X5R (0805)
Replace with 4213010600G
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK
ECN 81137
Replace with 5050004800
120R, 300MA EIA(0402)
+PCIE
+VDDC
+VDDC_CT
+3.3V
+PVDD
+MPVDD
+VDDPLL
GND_PCIE_PVSS
GND_VSSRH0
GND_VSSRH1
GND_PVSS
GND_MPVSS
RV530 unfused A11
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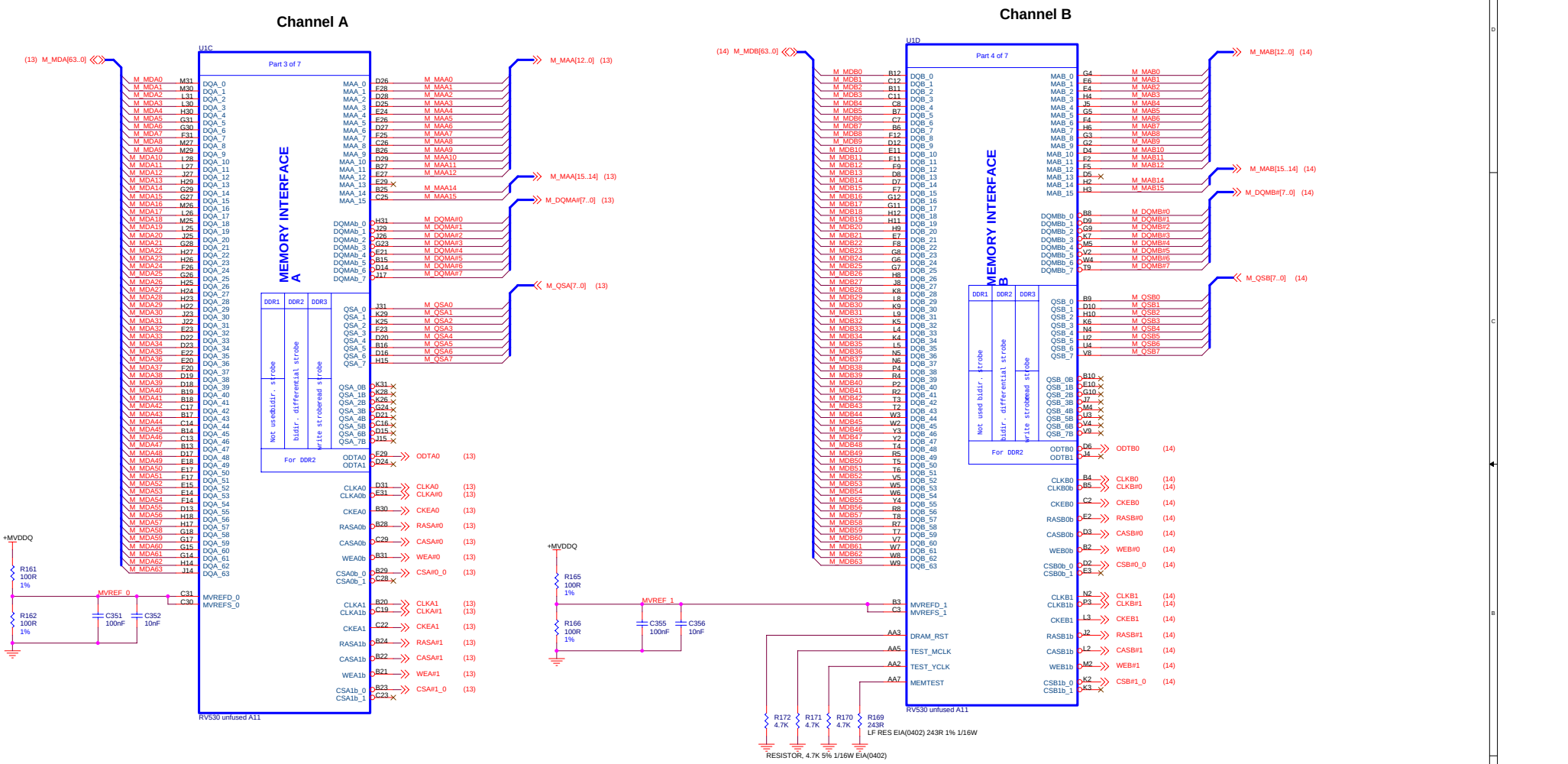
RV530 MEMORY CHANNELS A and B



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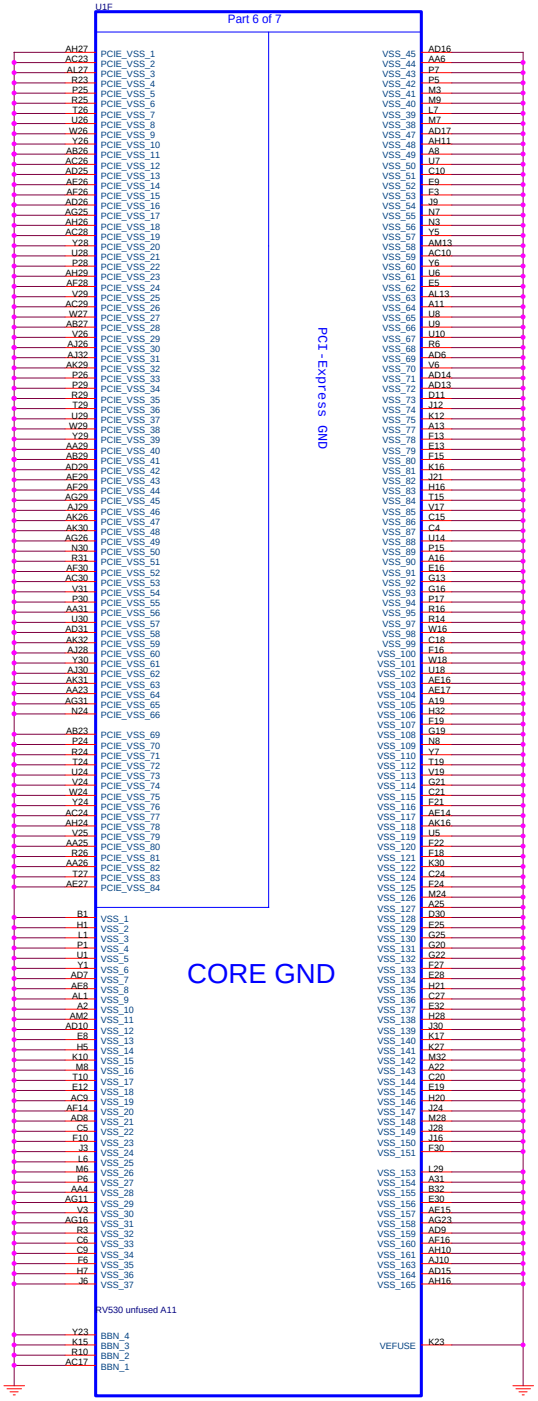

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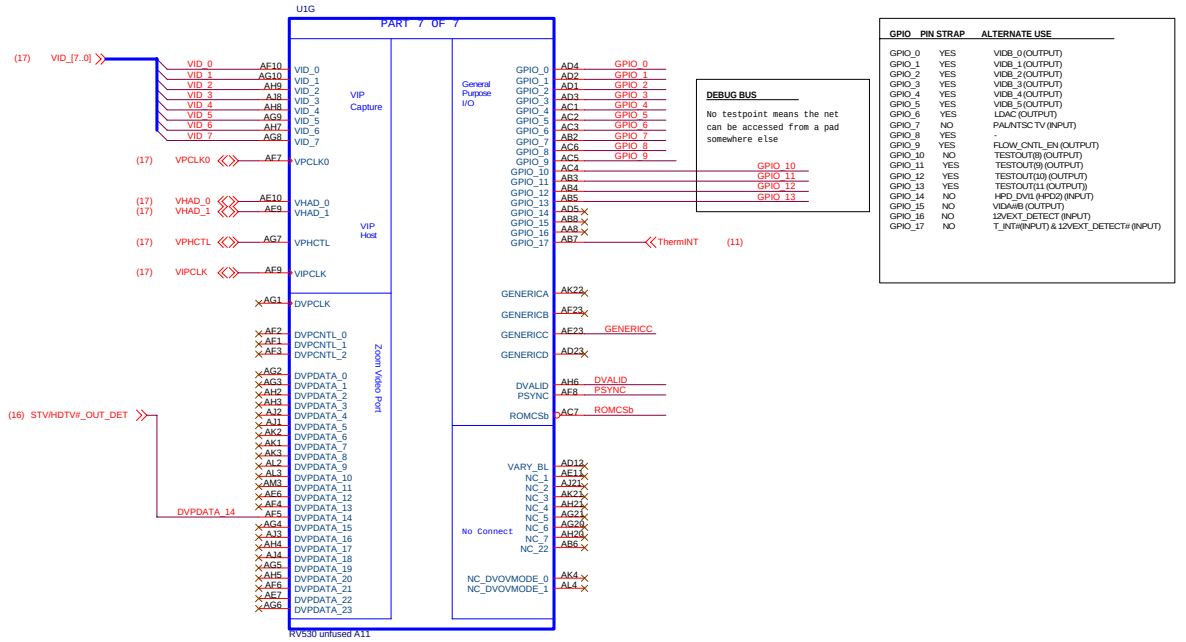
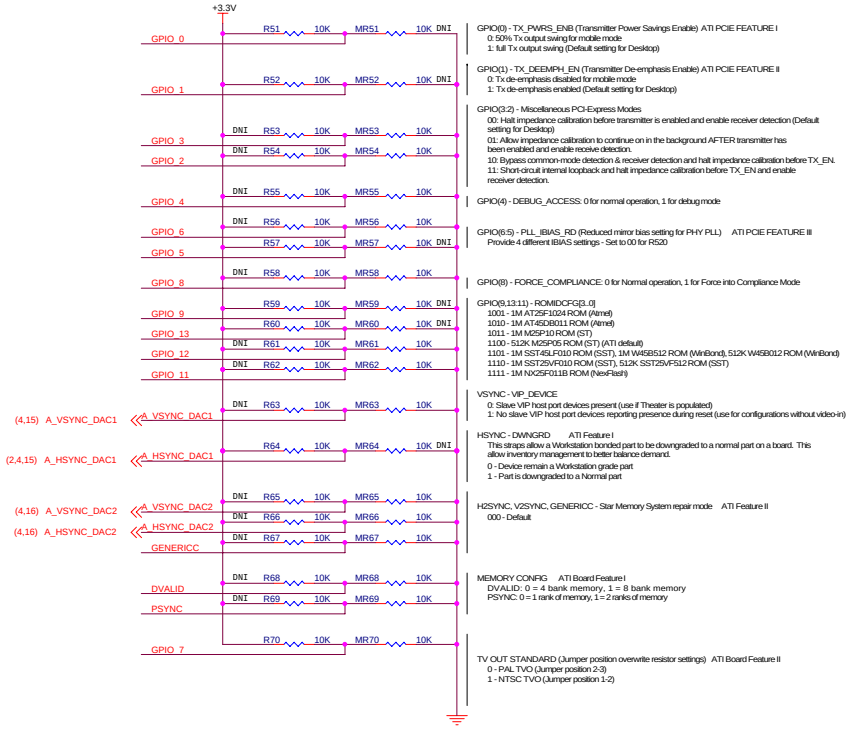
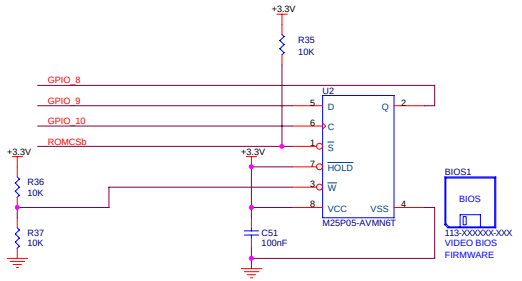


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDAalB (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

PIN BASED STRAPS





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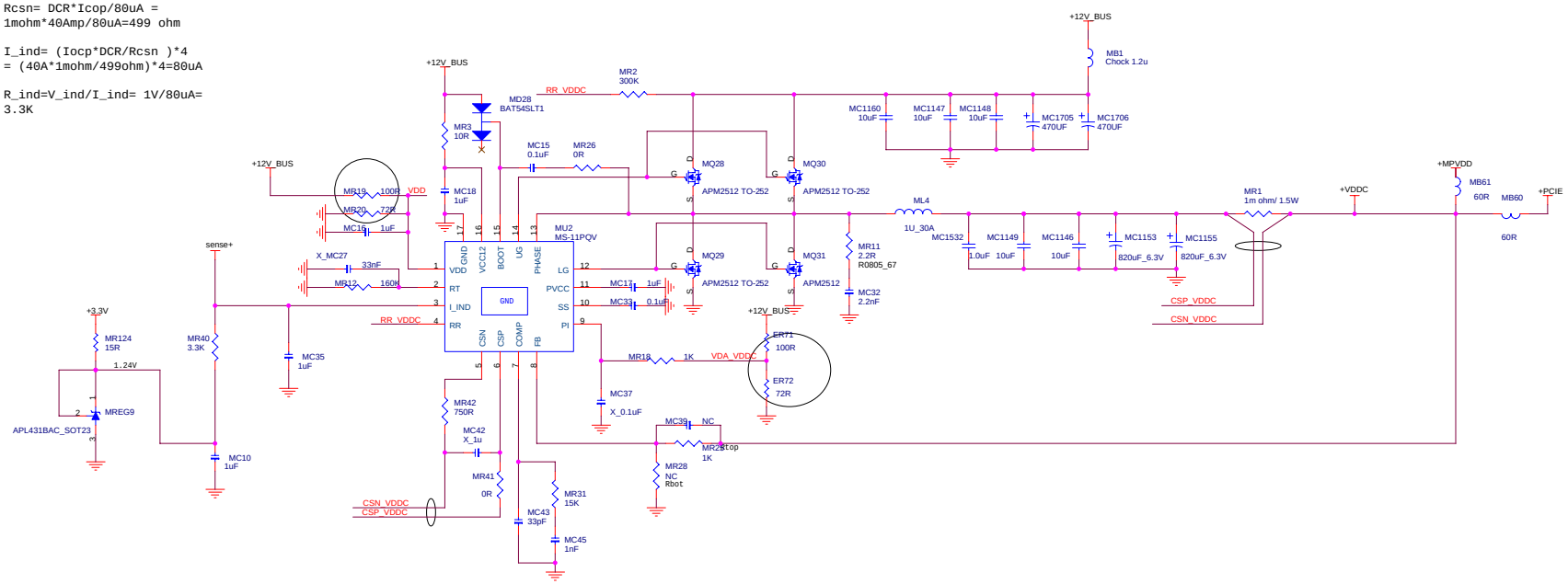
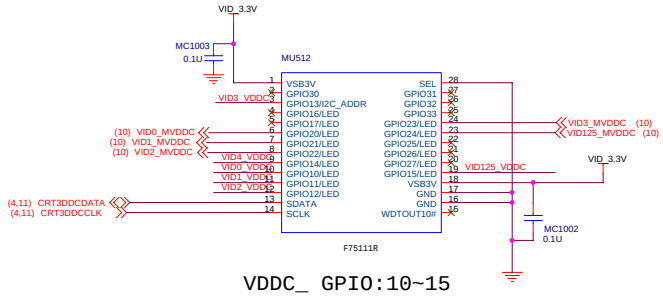
Rcsn= DCR*Icop/80uA =
1mohm*40Amp/80uA=499 ohm

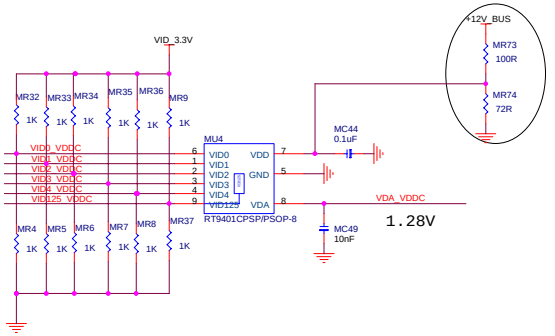
I_ind= (Iocp*DCR/Rcsn)*4
= (40A*1mohm/499ohm)*4=80uA

R_ind=V_ind/I_ind= 1V/80uA=
3.3K





VDA_VDDC	VID125	VID0	VID1	VID2	VID3	VID4
1.075V	1	0	0	0	0	0
1.0875V	0	0	0	0	0	0
1.100V	1	0	1	1	1	1
1.1125V	0	0	1	1	1	1
1.125V	1	1	0	1	1	1
1.1375V	0	1	0	1	1	1
1.150V	1	0	0	1	1	1
1.1625V	0	0	0	1	1	1
1.175V	1	1	1	0	1	1
1.1875V	0	1	1	0	1	1
1.20V	1	0	1	0	1	1
1.2125V	0	0	1	0	1	1
1.225V	1	1	0	0	1	1
1.2375V	0	1	0	0	1	1
1.25V	1	0	0	0	1	1
1.2625V	0	0	0	0	1	1
1.275V	1	1	1	1	0	1
1.2875V	0	1	1	1	0	1
1.300V	1	0	1	1	0	1

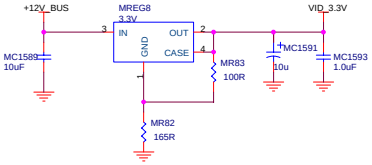


VDDC_ GPIO:10~15

MVDDC_ GPIO:20~24

DAC1_ GPIO:25~28

DAC2_GPIO:30~32



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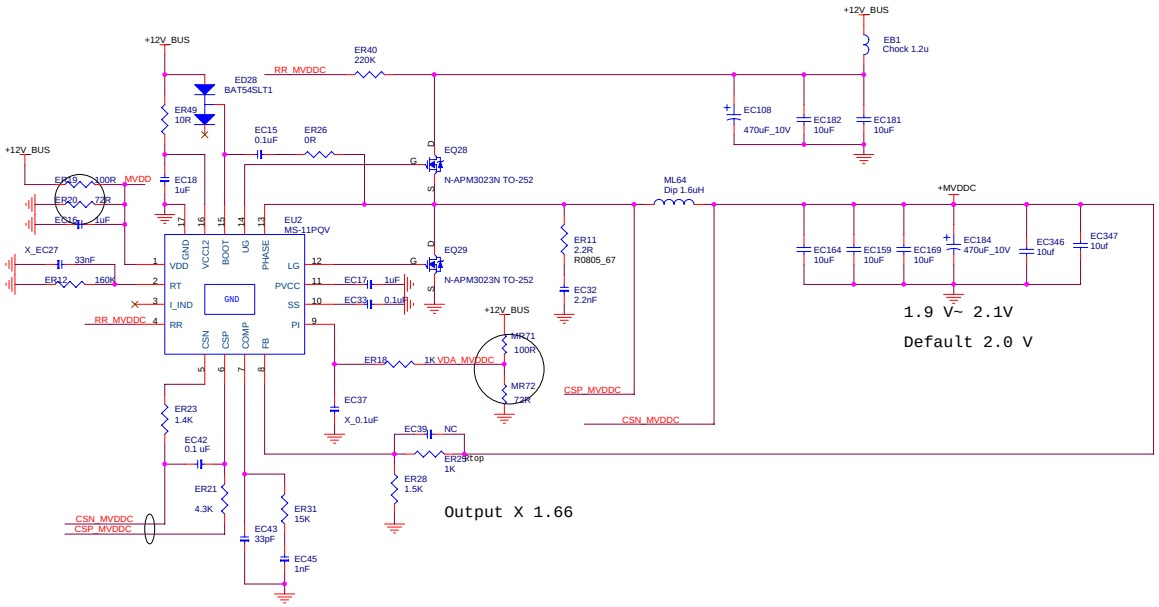

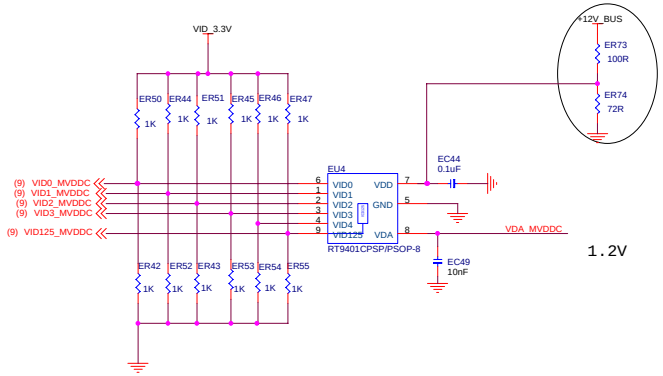

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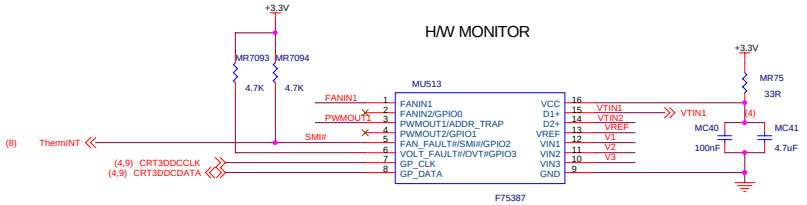
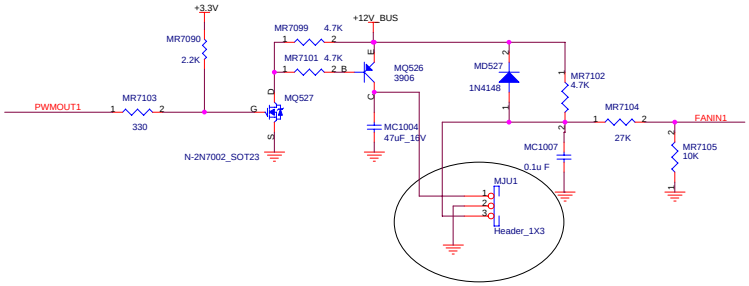
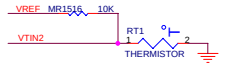
H/W MONITOR



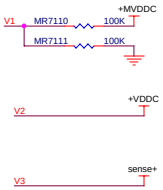
PWM FAN SPEED CONTROL

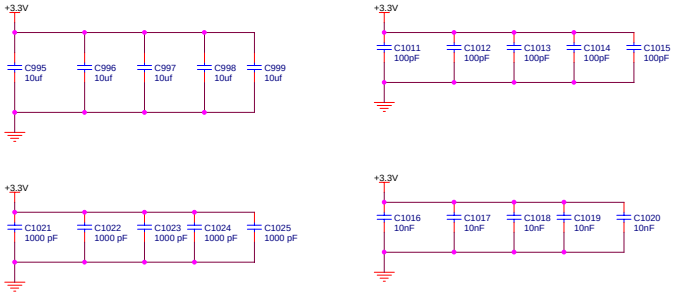


TEMPERATURE MONITOR



VOLTAGE SENSORING CIRCUIT





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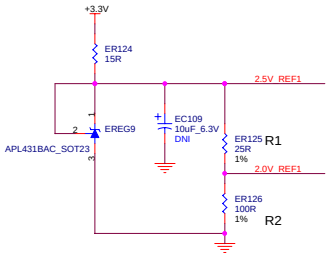
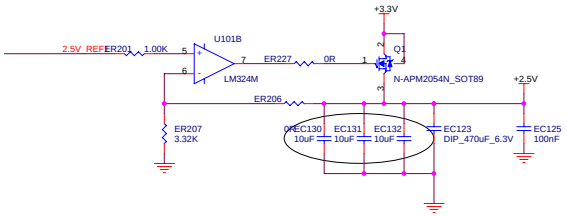
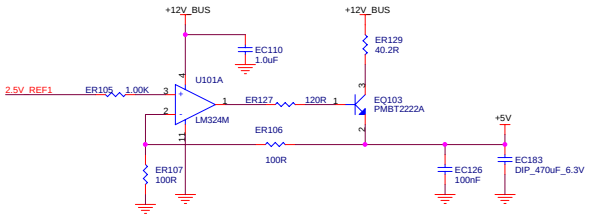
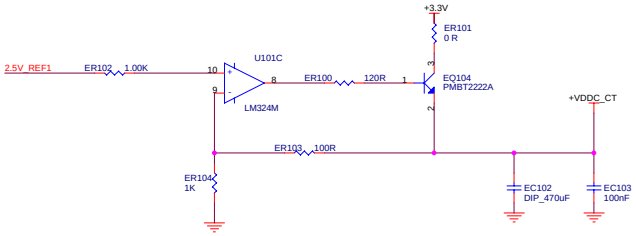
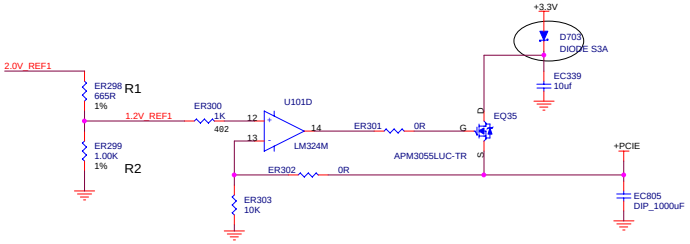
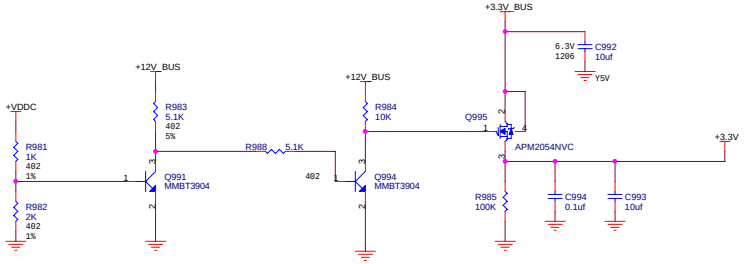




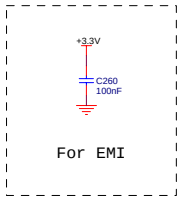


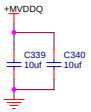


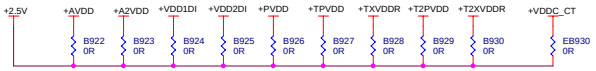




Power Sequence Circuit







Replace with 5050004800
120R, 300MA EIA(0402)

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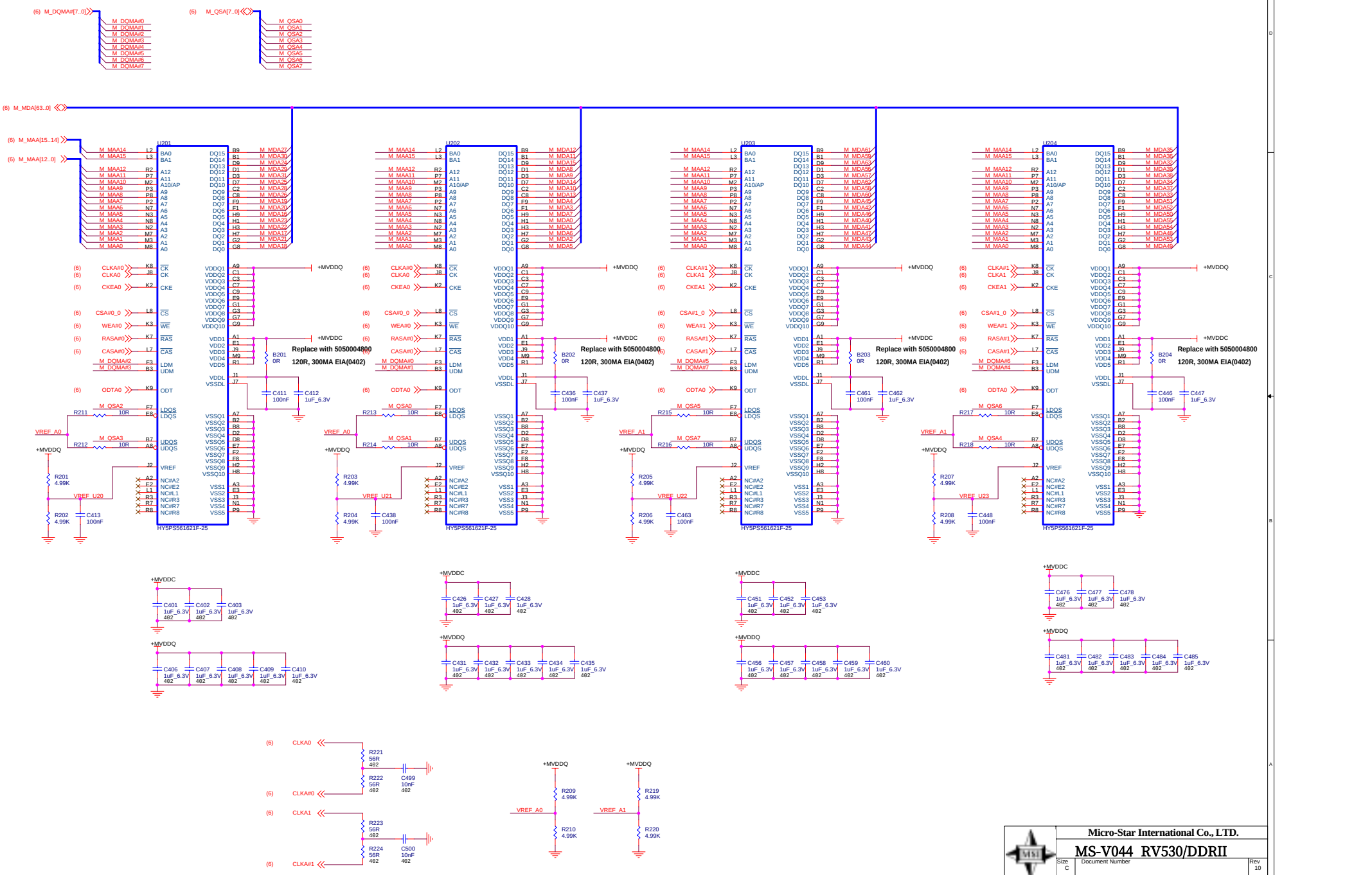
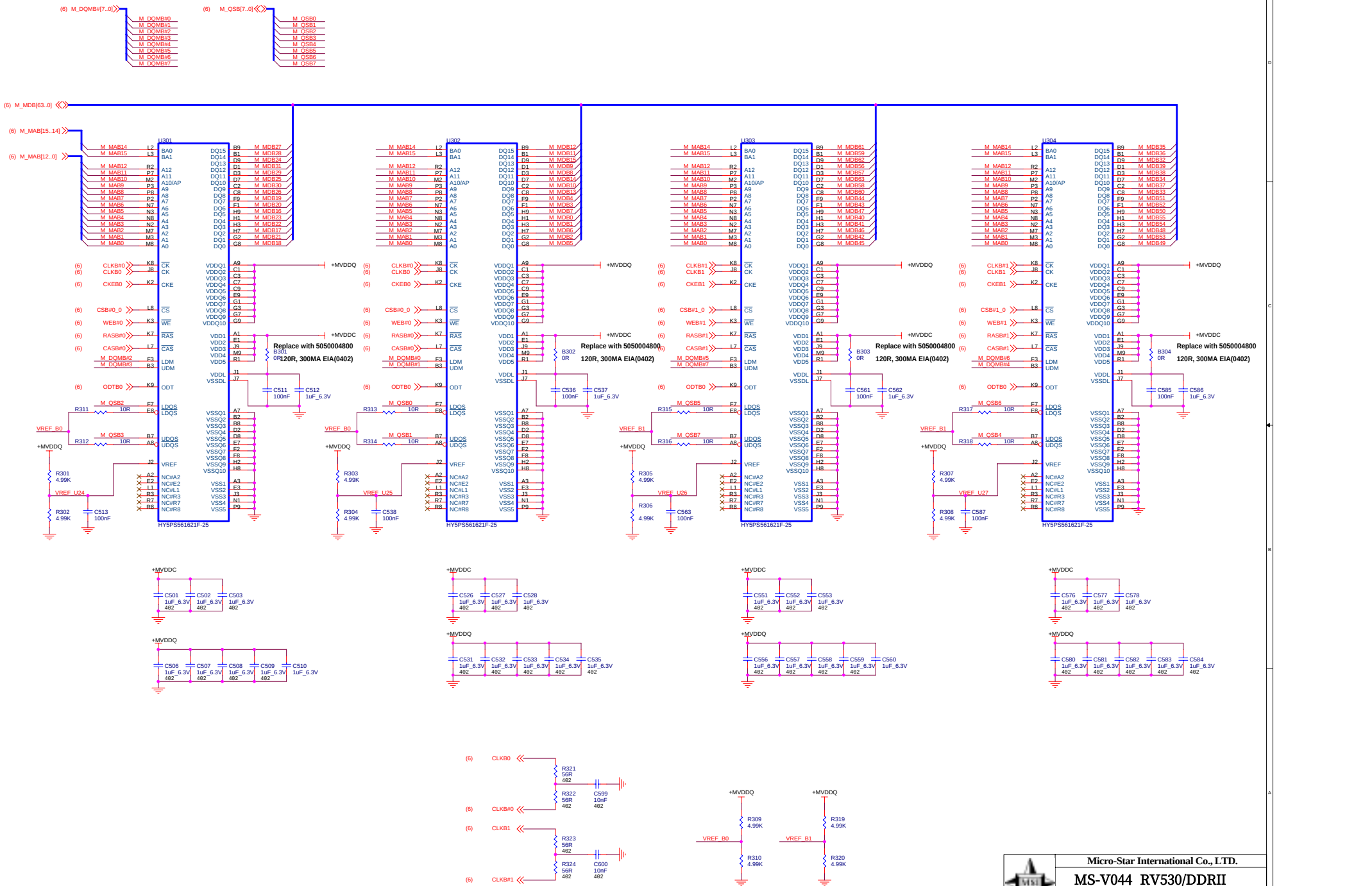
CHANNEL A: RANK 0 128MB DDR2



CHANNEL B: RANK 0 128MB DDR2



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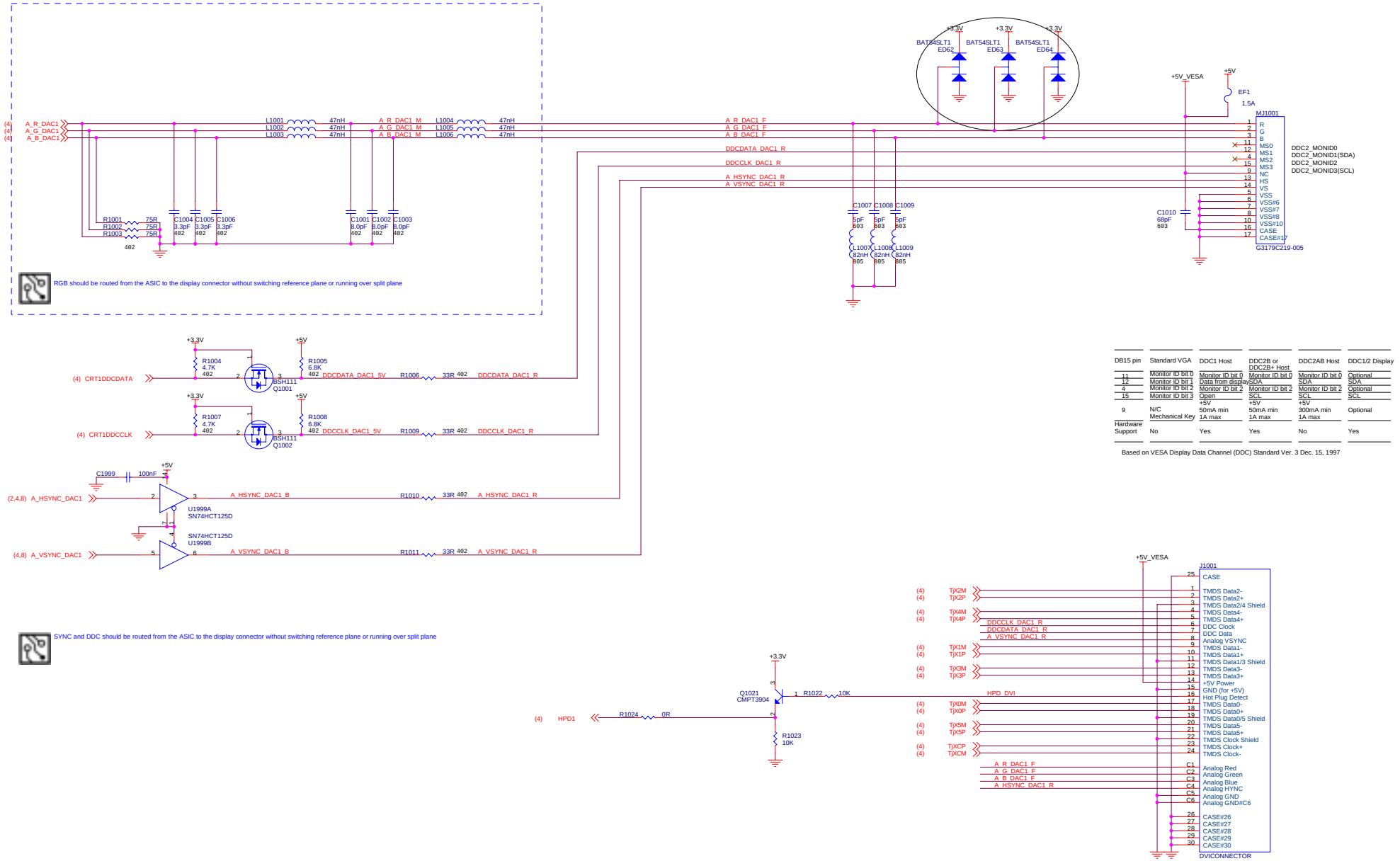

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C Mechanical Key	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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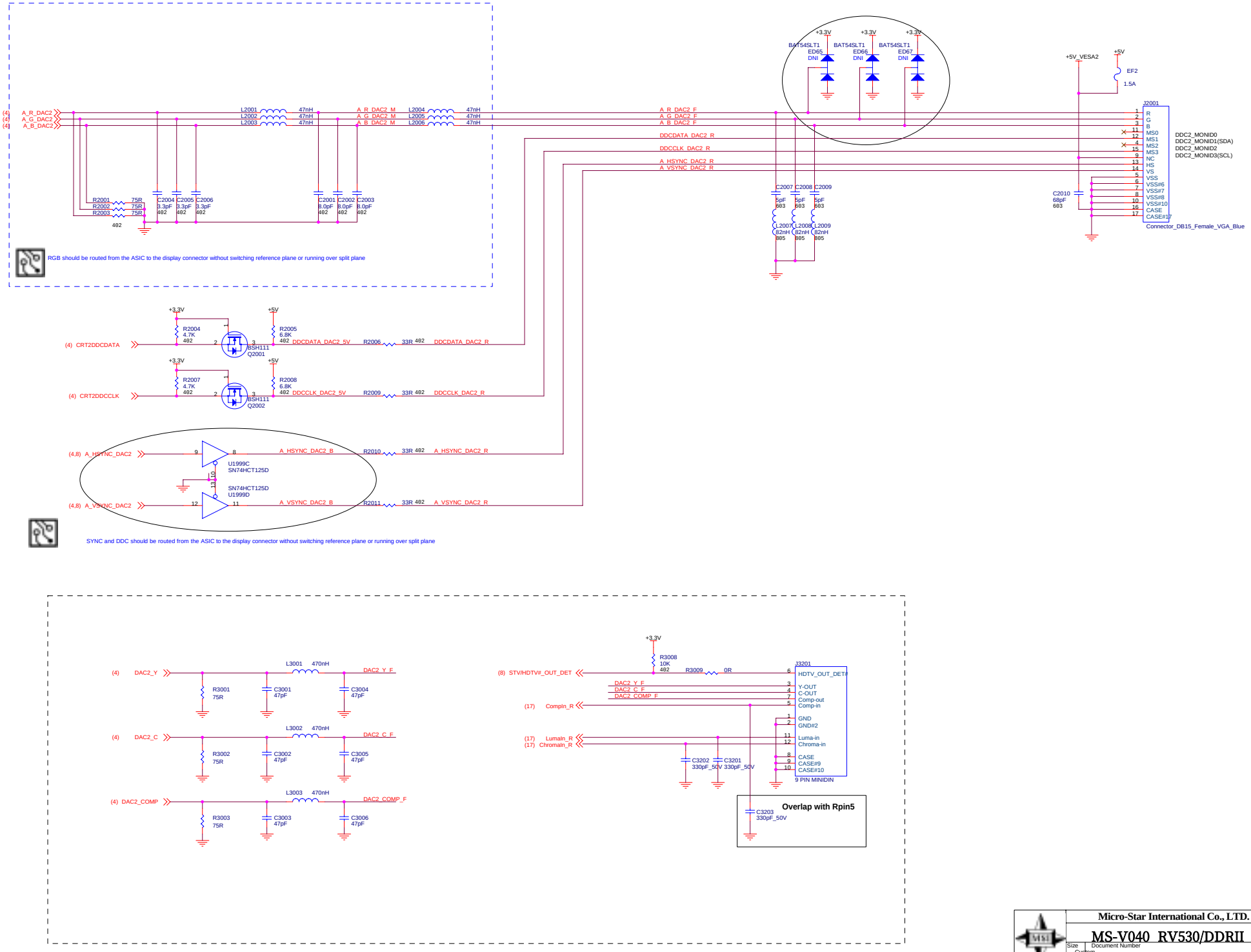

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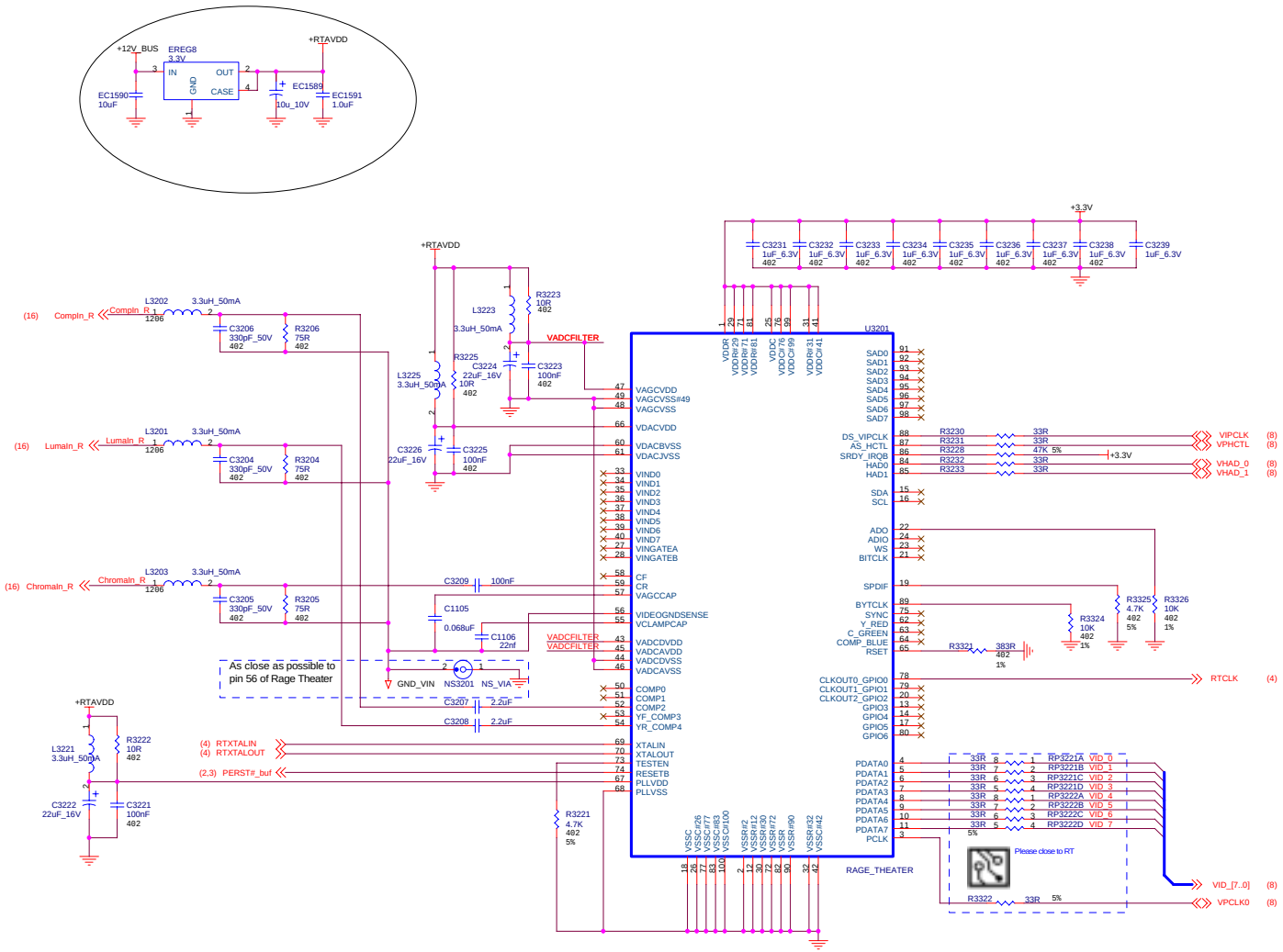

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DVI/VGA SCREWS

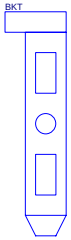
SCREW1
SCREW
JACKSCREW ASSY
7020000800

SCREW2
SCREW
JACKSCREW ASSY
7020000800

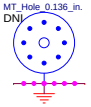
SCREW3
SCREW
JACKSCREW ASSY
7020000800

SCREW4
SCREW
JACKSCREW ASSY
7020000800

BKT



MT1
MT_Hole_0.136_in.
DNI



FM1 SW_FB
FM5 SW_FB
FM2 SW_FB
FM6 SW_FB
FM3 SW_FB
FM4 SW_FB

PCB

FAN

LOW PROFILE HS

+MVDDQ
J1 X_PIN1*2
J3 X_PIN1*2
J2 X_PIN1*2
J4 X_PIN1*2

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