

P2002

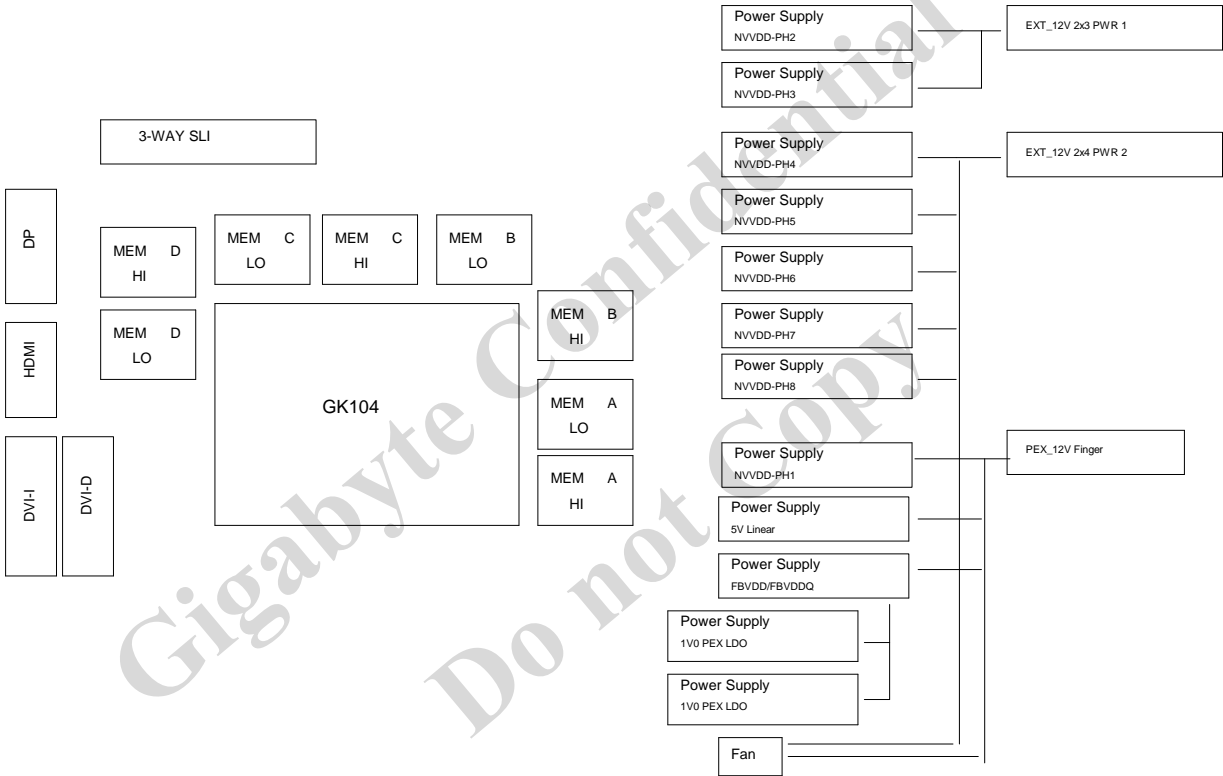
2GB GDDR5, 256b, 64Mx32

Stacked DVI-I/DVI-D + HDMI + DP

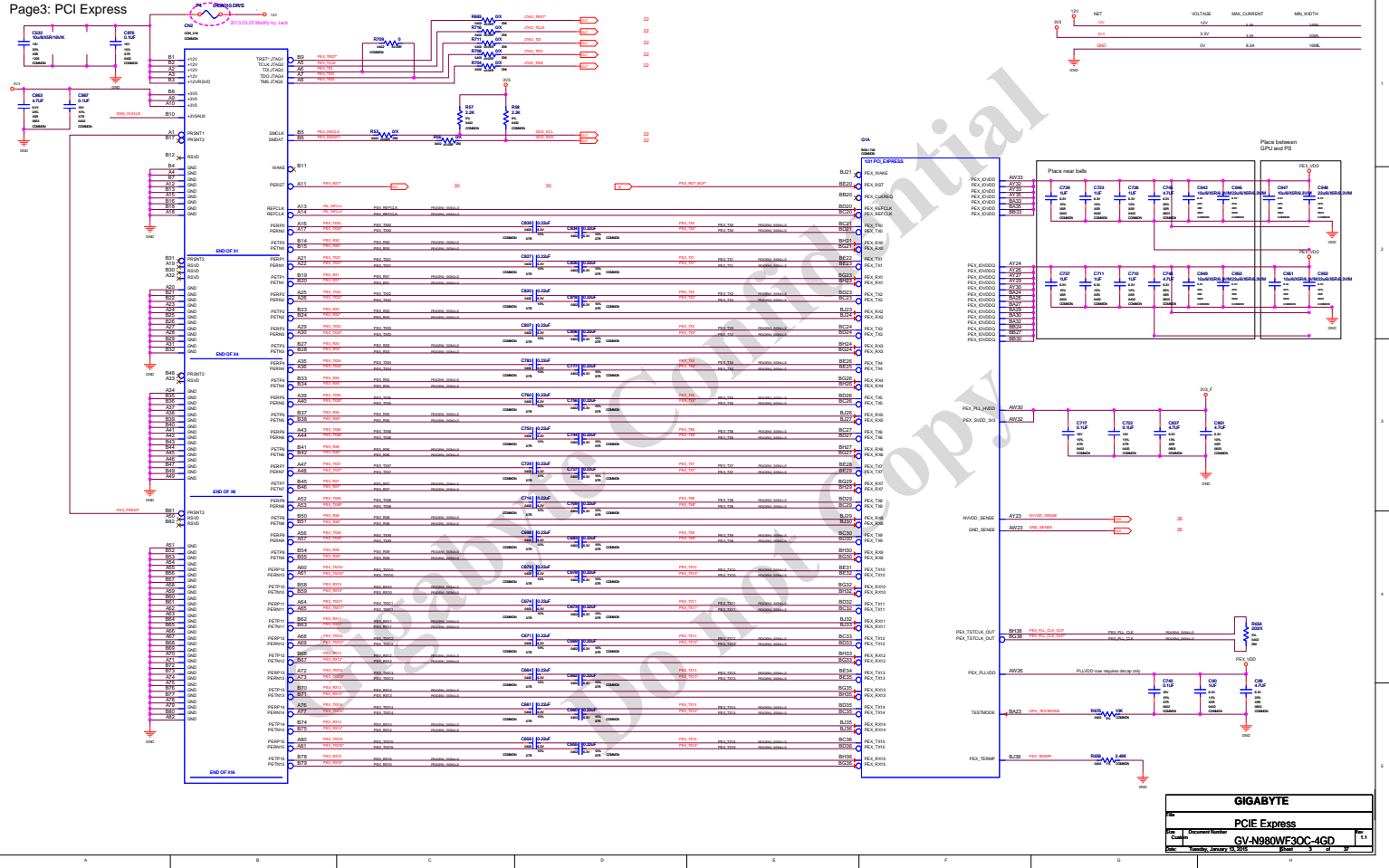
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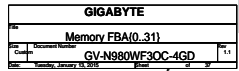
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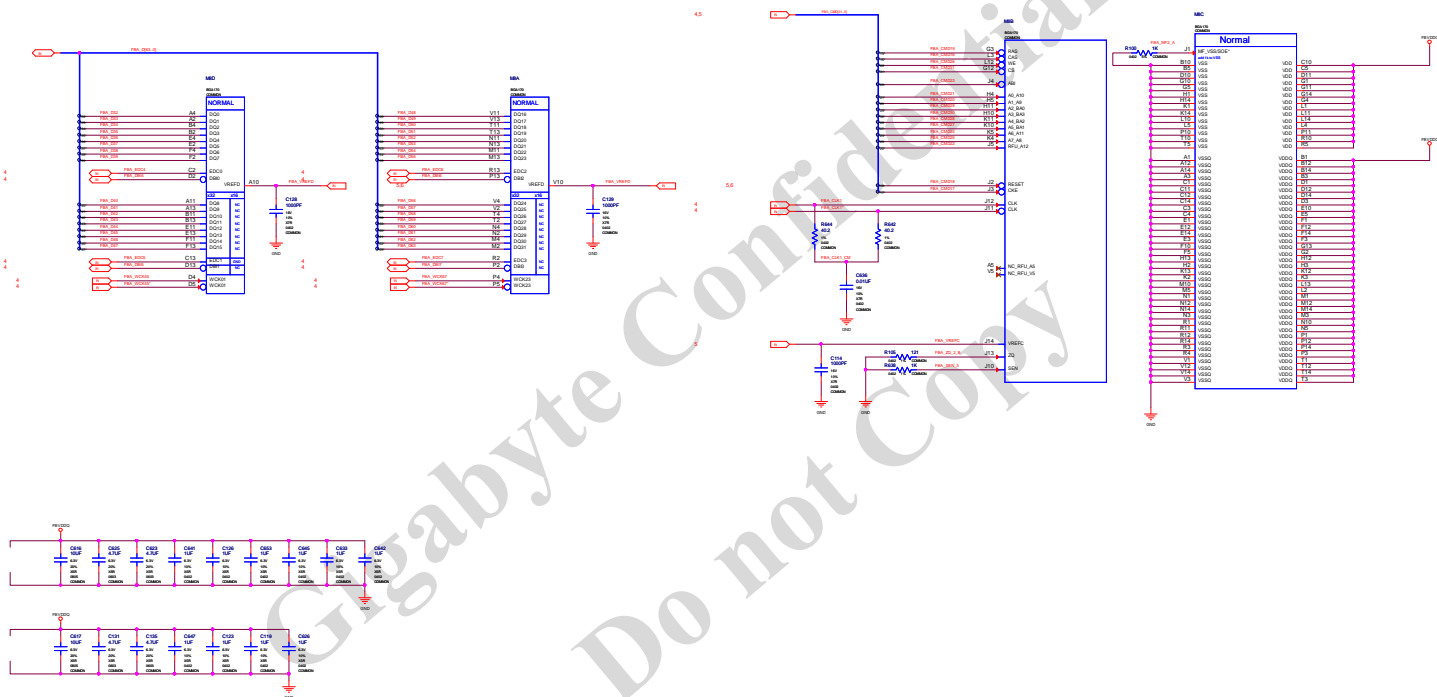


GIGABYTE			
Block of Diagram			
Doc No.	GV-N980WF3OC-4GD	Rev.	1.0
GIGABYTE Technology, Inc. 2012			





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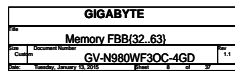


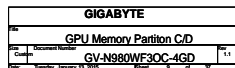
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ASSEMBLY
PAGE DETAIL

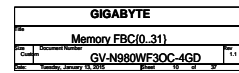
BASE LEVEL GENERIC SCHEMATIC ONLY
MEMORY (FBA(32..95))

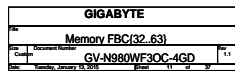
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Memory FBA(32..63)	
GV-N980WF30C-4GD	
1.1	



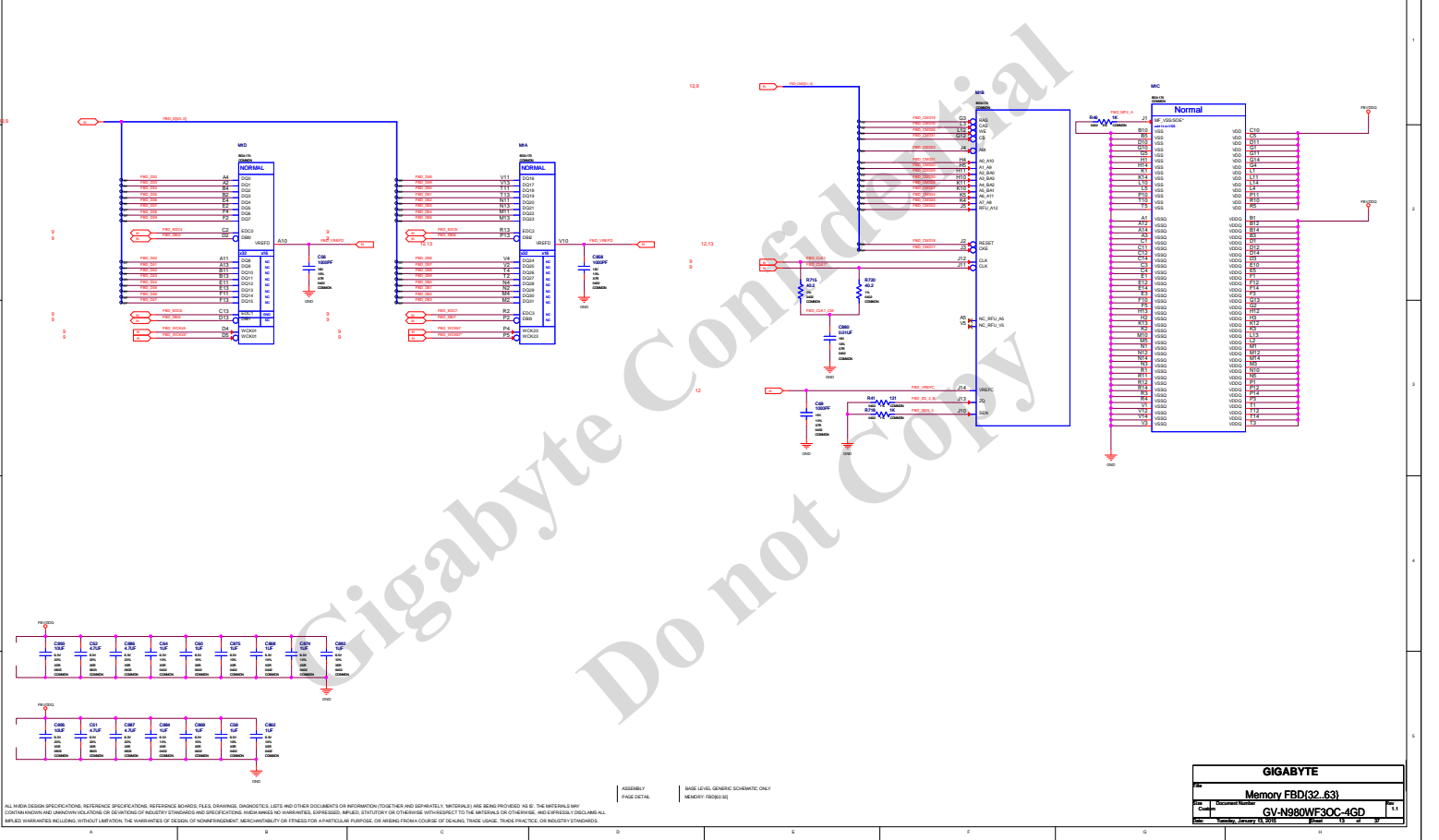


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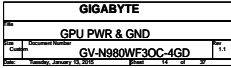




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ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY MEMORY (PROM 32)

GIGABYTE	
Memory FBD(32..63)	
GV-N980WF3OC-4GD	
GIGABYTE	



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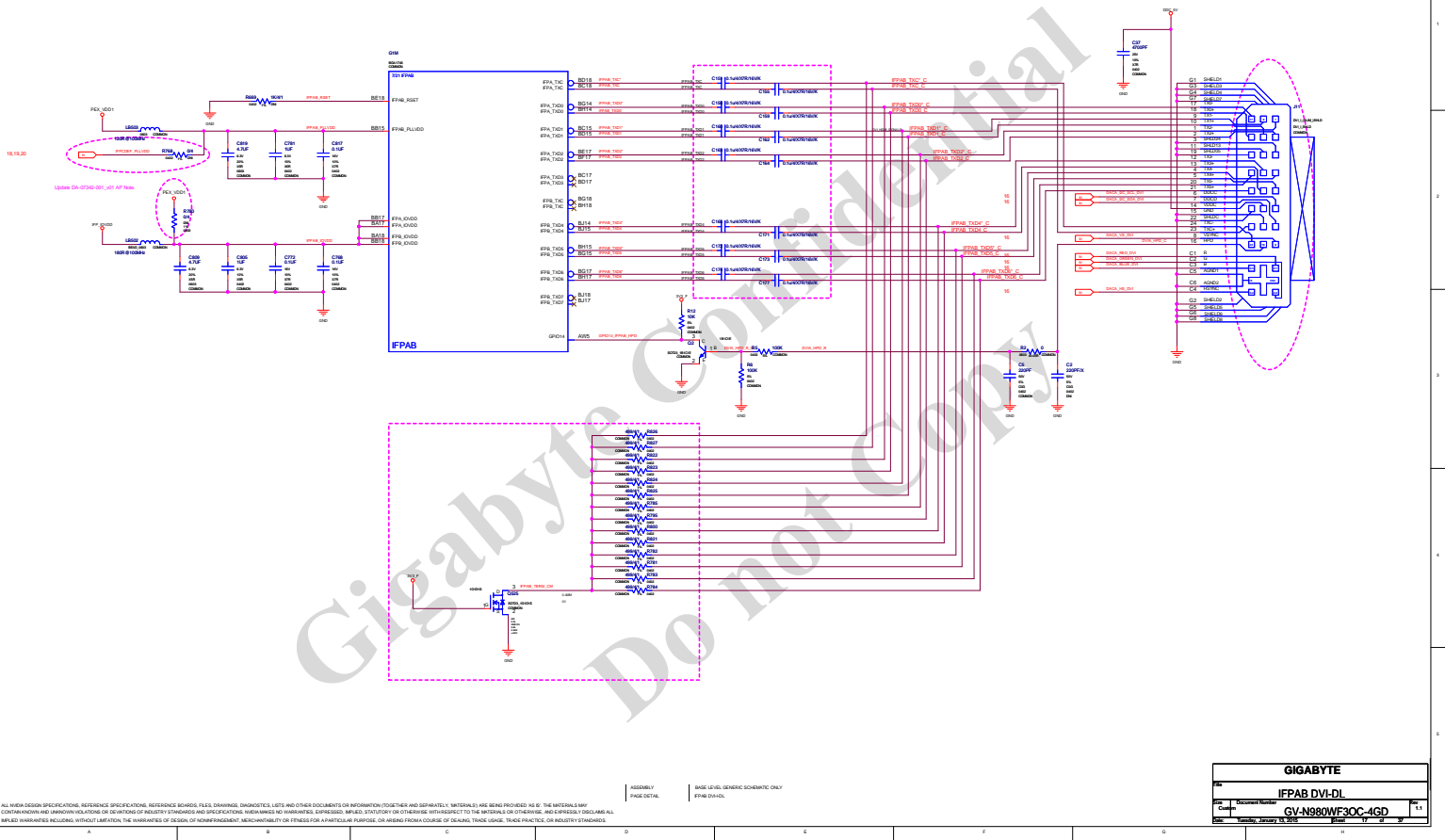
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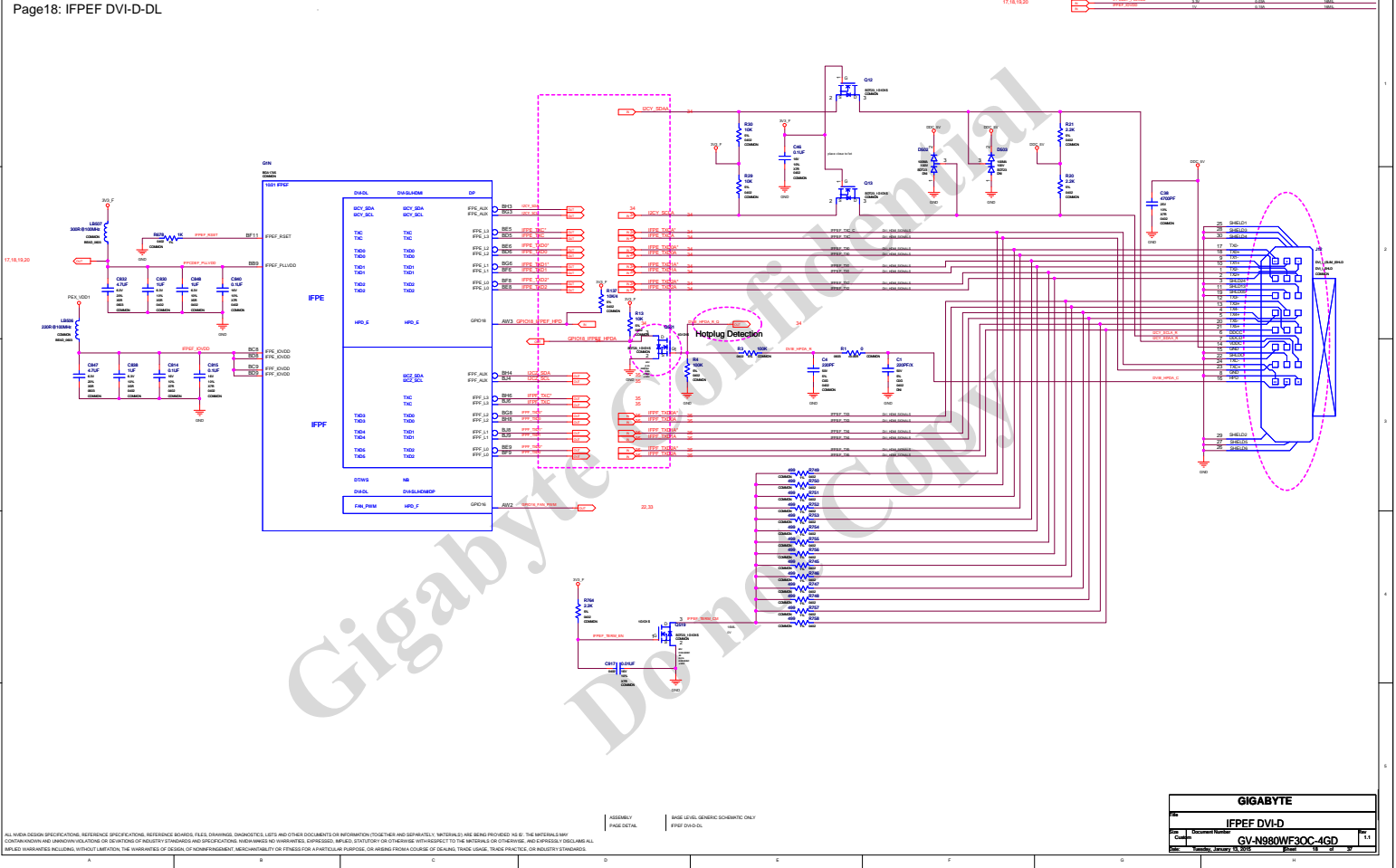
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ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
GPU Decoupling

GIGABYTE	
GPU Decoupling	
Document Number	GV-N980WF3OC-4GD
Revision	1.0



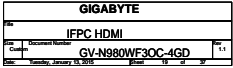


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ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
IPFEF DVI-D-DL

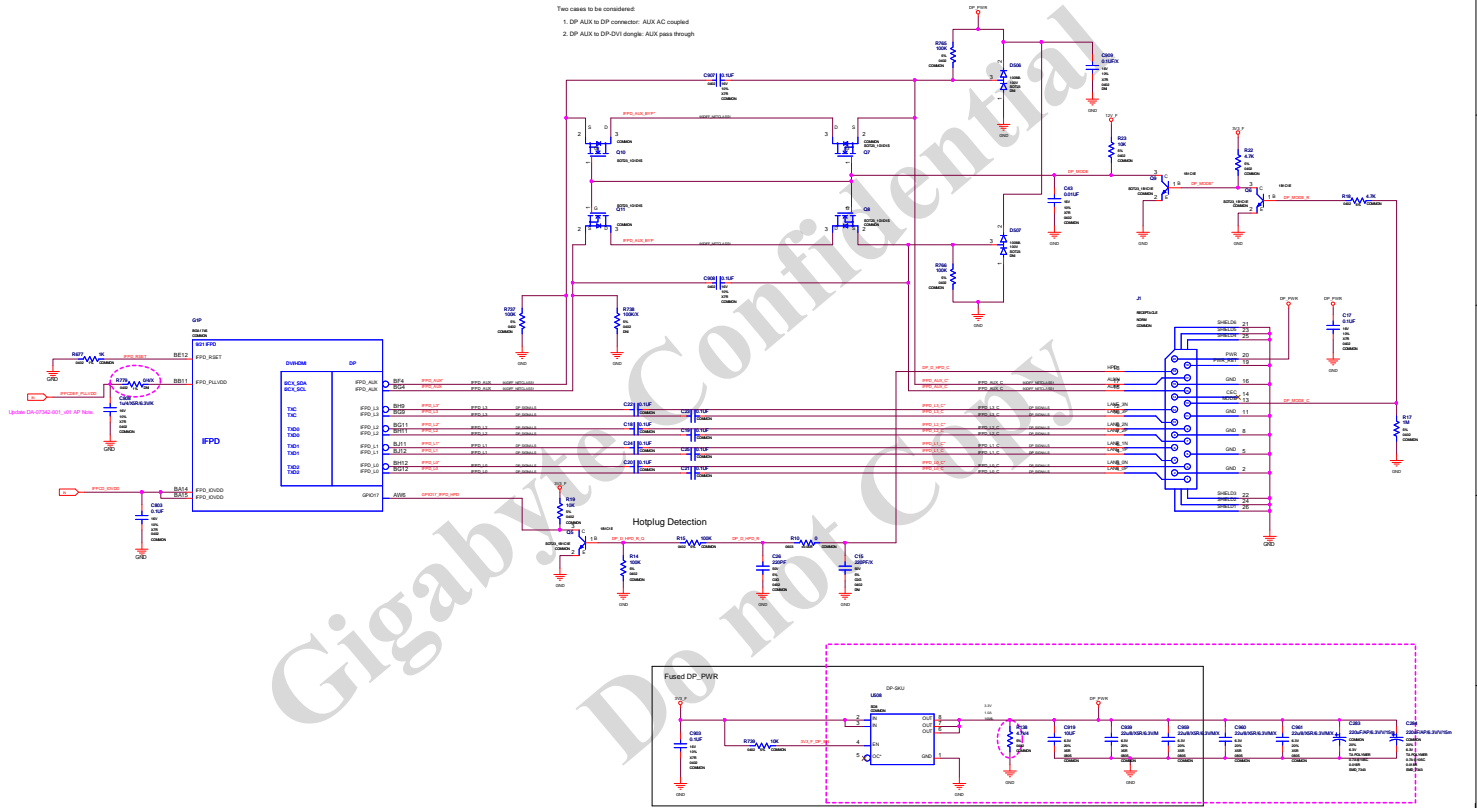
GIGABYTE	
IPFEF DVI-D	
GV-N980WF3OC-4GD	
1:1	



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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

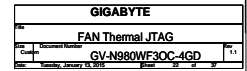


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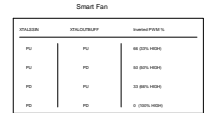
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	8FO-0P

GIGABYTE									
File									
IFPD DP									
Doc Comments		Document Number GV-N980WF30C-4GD						Rev 1.3	
Date		Tuesday, January 04, 2015		Sheet		20		of 30	



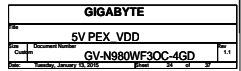


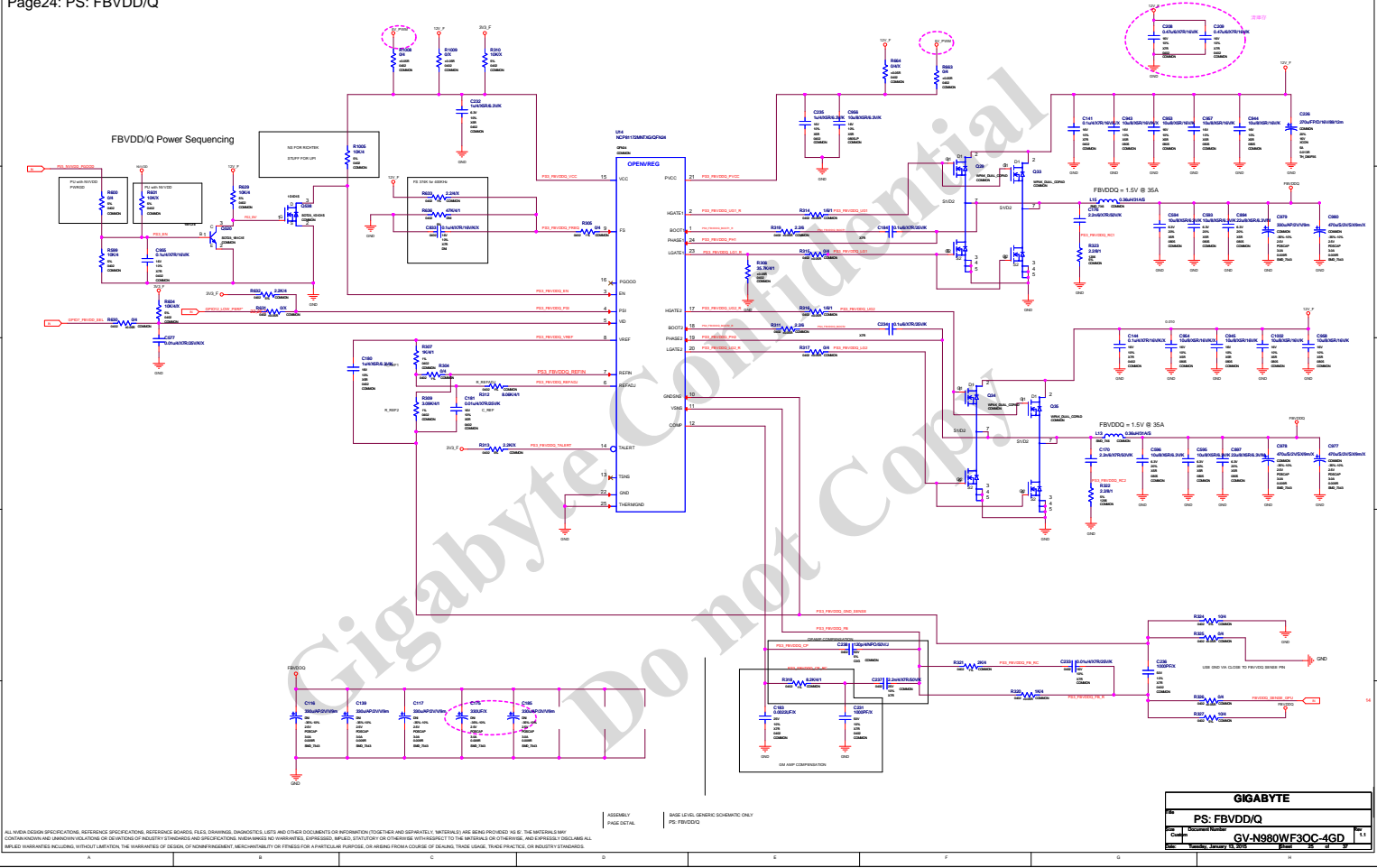
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0010 32Mx32 256-bit Hynix
0011 32Mx32 256-bit Samsung
0100 Reserved
0101 64Mx32 256-bit Ellpsida
0110 64Mx32 256-bit Hynix
0111 64Mx32 256-bit Samsung
1000 Reserved
1001 32Mx32 192-bit Ellpsida
1010 32Mx32 192-bit Hynix
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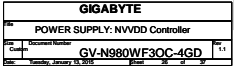


GIGABYTE			
File			
ROM Xtal Straps			
Size	Document Number		File
Custom	GV-N980WF3OC-4GD		1.1
Date:	Tuesday, January 13, 2015	Sheet	25 of 30

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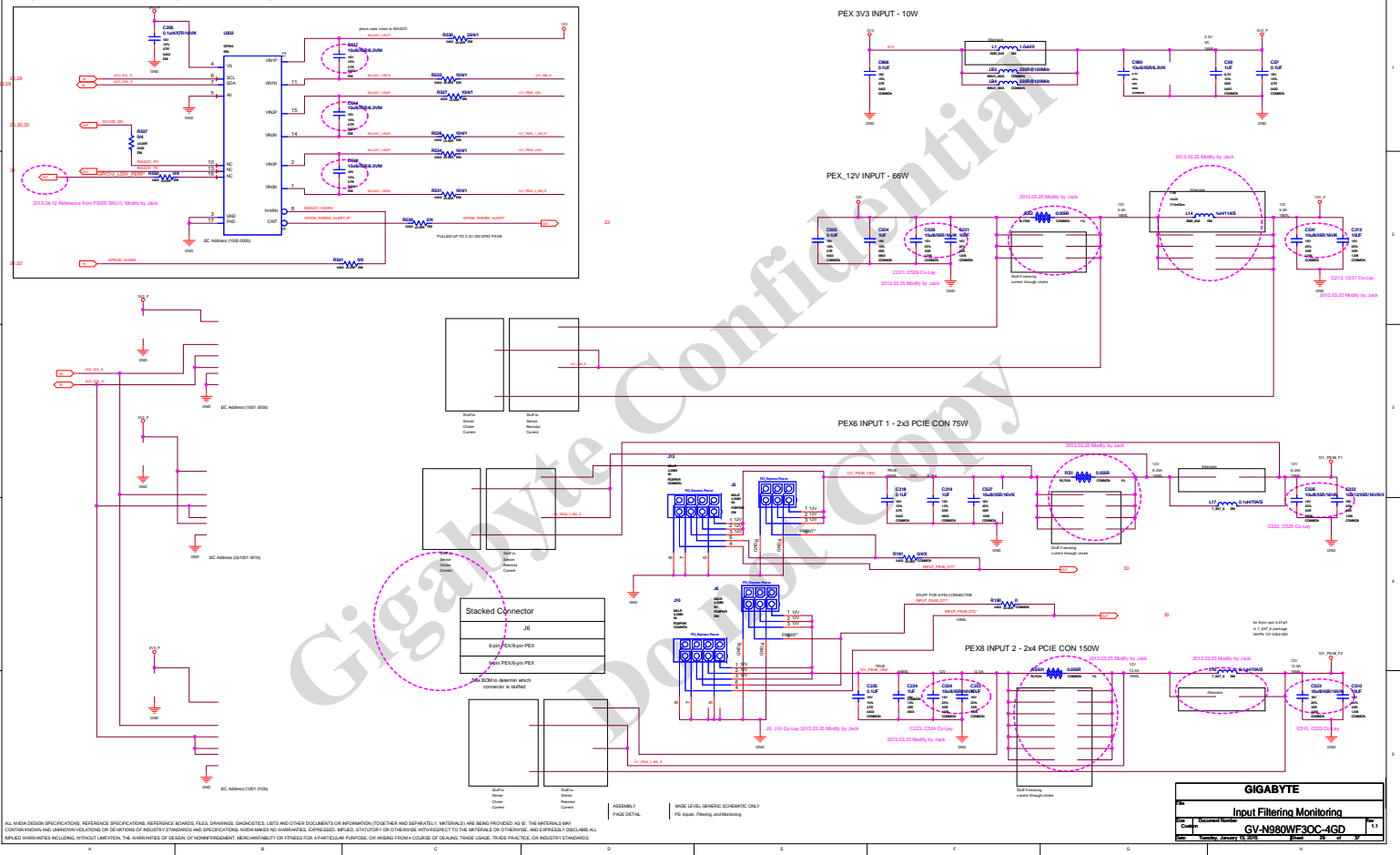


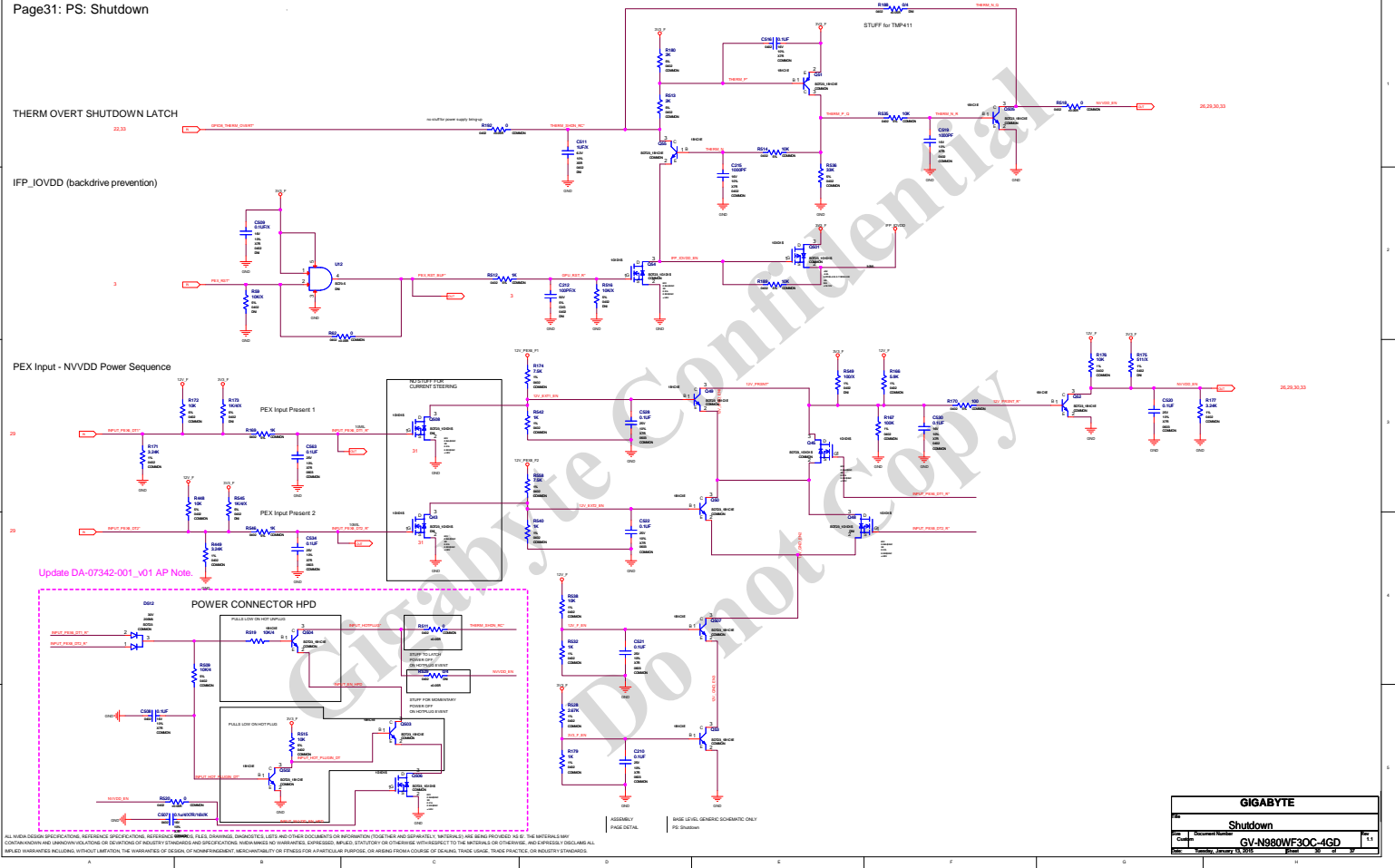




The schematic diagram shows a 10-bit SAR ADC circuit. It consists of six stages, each with a 330 pF capacitor (C156 to C160) and a 100 nA current source (C87 to C91). The stages are connected in series, with the output of one stage feeding into the next. The final output is connected to a 10-bit SAR ADC block.

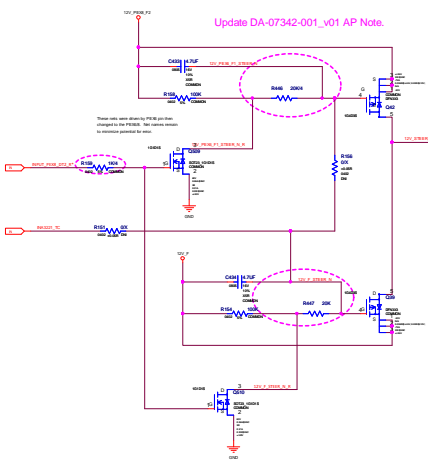
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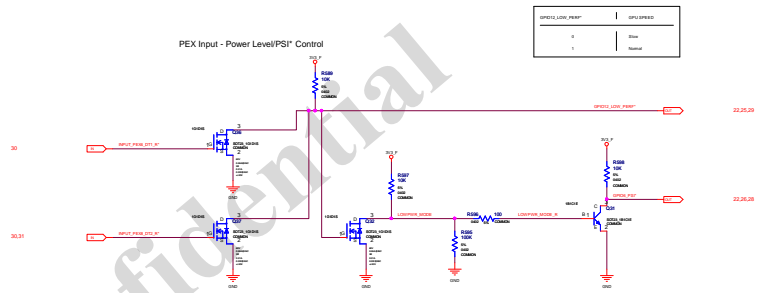


PEX Input - 12V Current Steering FETs

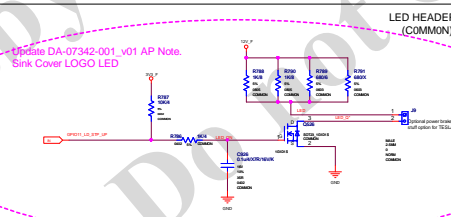
Update DA-07342-001_v01 AP Note.



PEX Input - Power Level/PSI* Control



GeForce Logo LED



LED HEADER (COMMON)

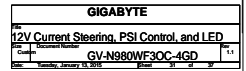
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2013.03.25 Modify by Jack

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ASSEMBLY PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY PS: 12V Current Steering FET Control and LED



Brackets:



MH-TC2368C350125-8

Bracket Screw



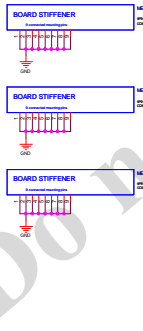
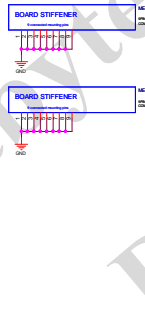
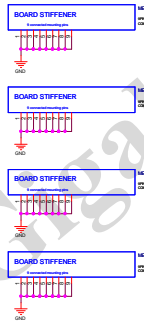
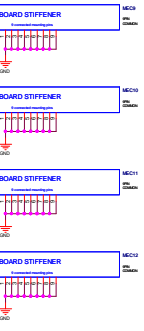
Hockey Stick



GPU Stiffener



Mechanical Holes Symbol



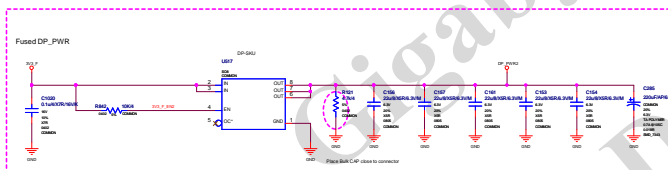
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ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY MH-TC2368C350125-8

GIGABYTE	
Thermal Bk	
GV-N980WF3OC-4GD	
1.1	

Two cases to be considered:

1. THE SEL TO HIGHT, CONNECT DVI WORK
2. THE SEL TO LOW, CONNECT VGA WORK



GIGABYTE	
File PS: NVDD Phase 1 & 3	
Docu- ment Number	GV-N980WF3OC-4GD
Ver- sion	1.00

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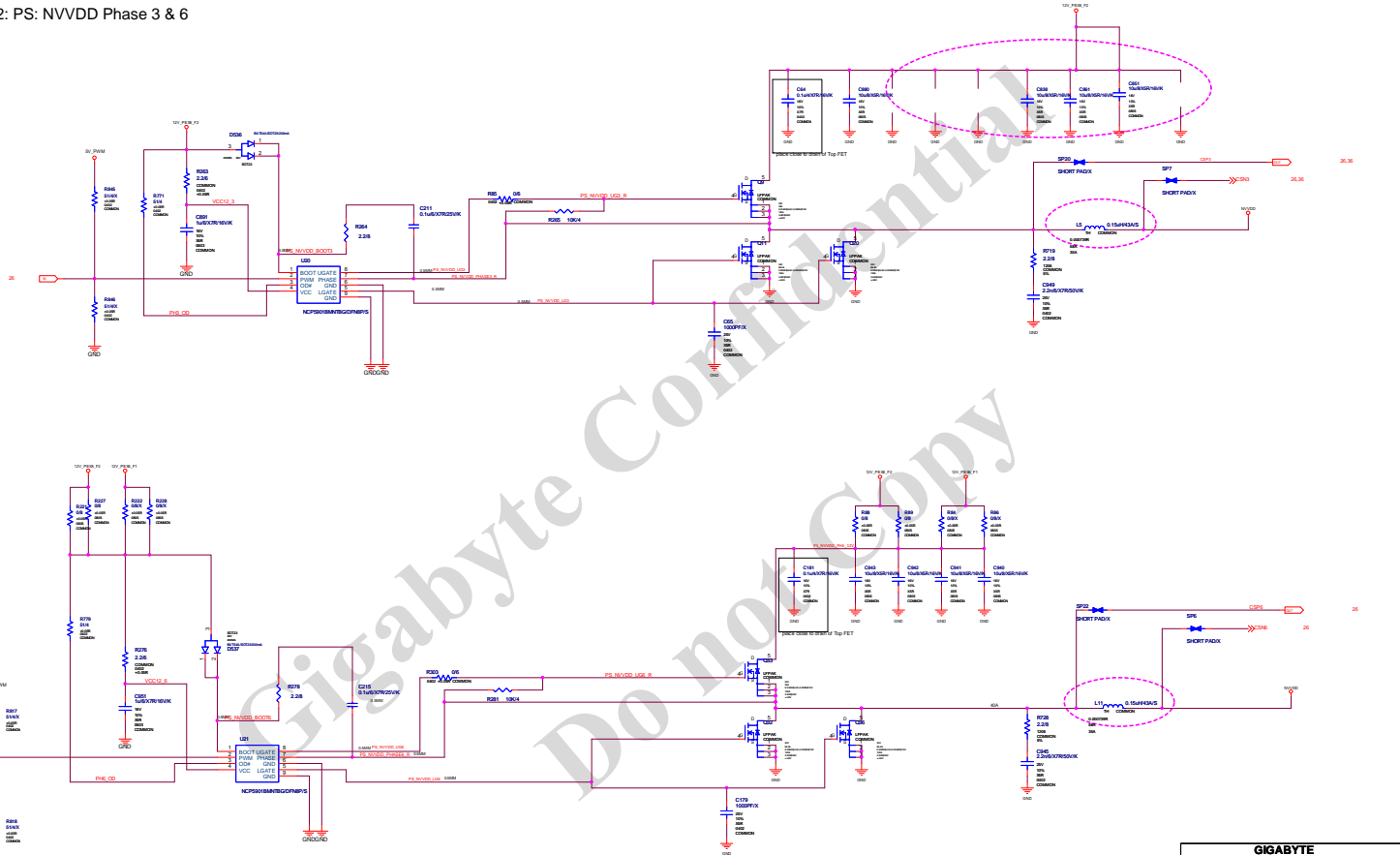


MLCC with 7343 Colay

Hotplug Detection

GIGABYTE	
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PS: NVDD Phase 1 & 3	
File Name	Document Number
	GV-N980WF3OC-4GD
File	1.1
Date	Tuesday, January 13, 2015
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GIGABYTE	
Part Number	PS: NVVDD Phase 3 & 6
Revision	1.0
Product Name	GV-N980WF3QC-4GD
File Name	PS: NVVDD Phase 3 & 6

