

NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X

PCI DEVICE ID 0X0=0X200 FOR NV20.

NVVD SET TO: 1.52V
FBVDD SET TO: 3.47V
FBVDDQ SET TO: 2.59V

HISTORY REVISION:

X00: Based on P50-A06
- See change list in 149- file.
- Set FBVDDQ=2.59V


P50-A07-X01:
- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

P50-A08:
X04: - Delay PLL_VDD to come up after NVVD.
X05: - Added 1UF across R257.
X06: - Removed X04-5 above, added a switcher generated PLL delay option.
- SSENNA cap for 2nd SW changed to 1UF.
- A05 SI, NVVD=1.52V

P50-A09:
X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.
X03: - Added option to pull up power good to 12V

ECO1235: - Changed R841 PU to 10K (from 4.7K)

ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction.
Replaced C303,306,309 with 75ohm and no stuffed R208-210.



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MS-8838 based on P50A09

Doc C

Document Number

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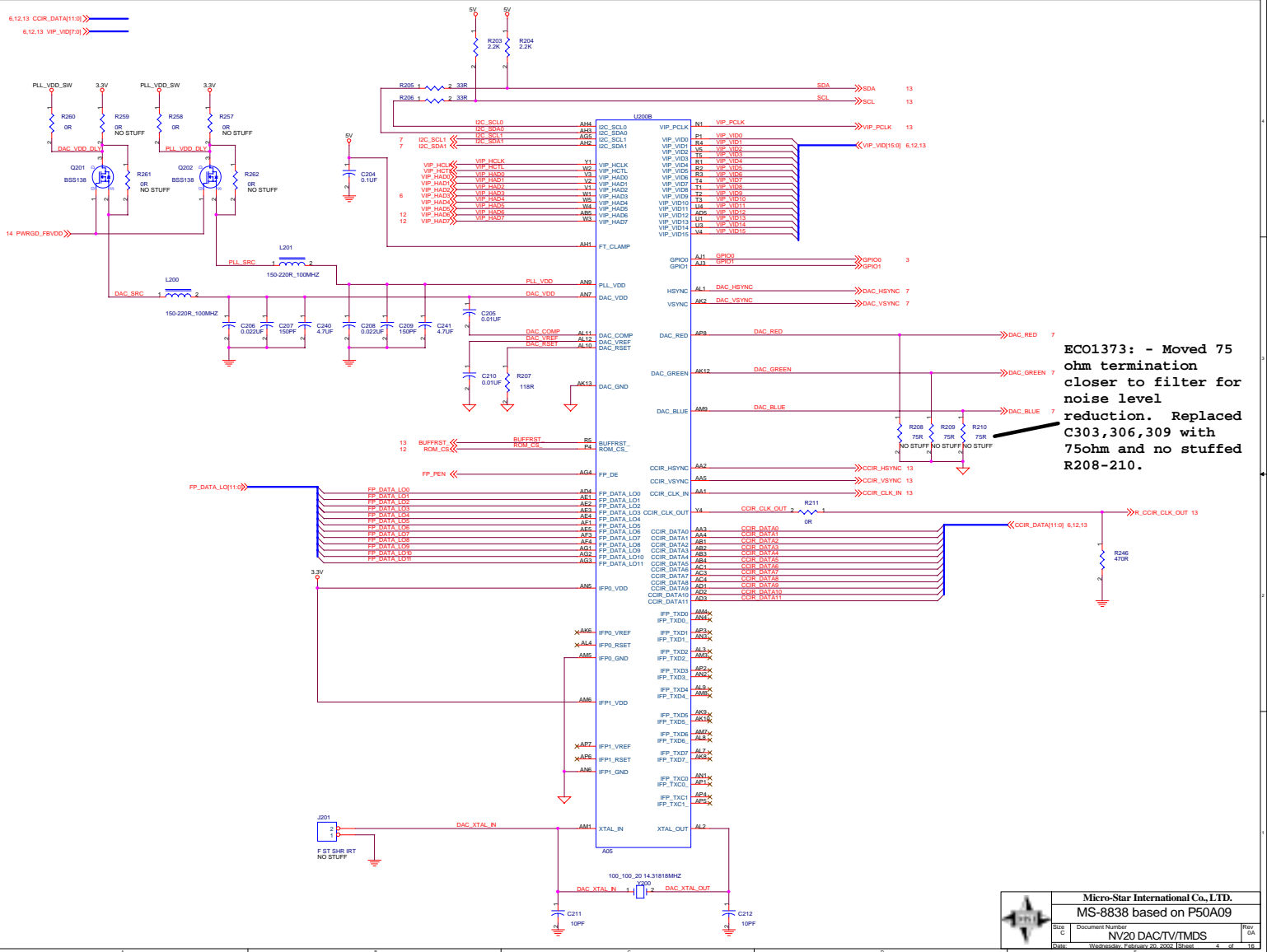
Rev 0A

Date

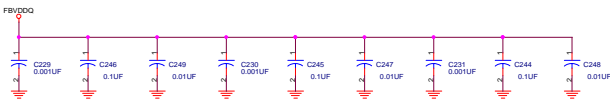
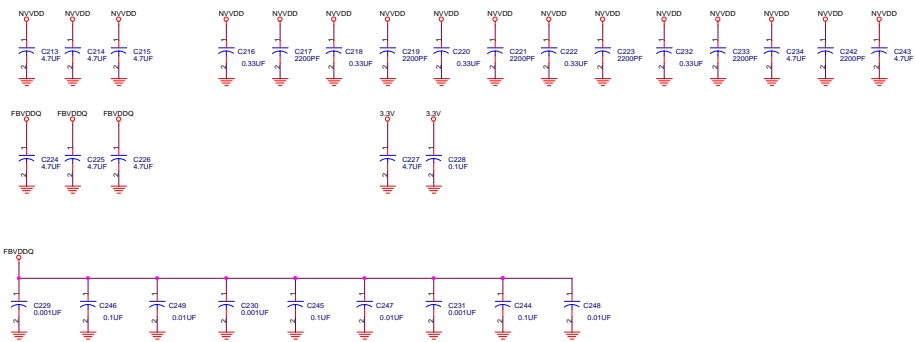
Wednesday, February 26, 2008 13:00

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6,12,13 COR_DATA[11:0] >>>
6,12,13 VIP_VID[7:0] >>>



Use thick (non-impedance controlled) traces on XTALIN/OUT

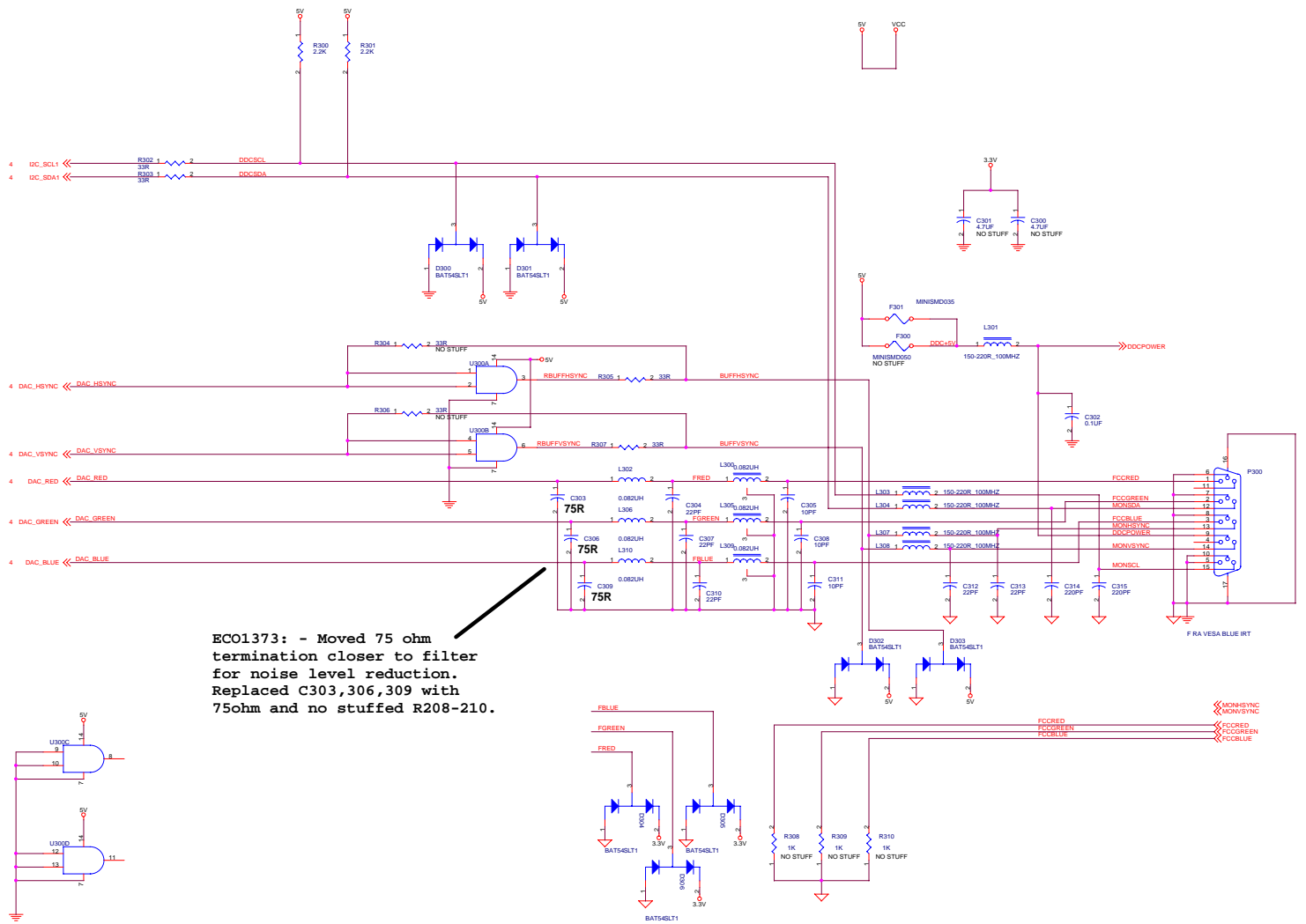


4.12.13 CCIR_DATA[11:0]
4.12.13 VIP_VID[15:0]
4 FP_DATA_LQ[11:0]

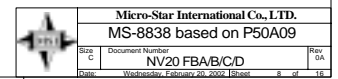
4 VIP_HAD0
4 VIP_HAD1
4 VIP_HAD2
4 VIP_HAD3
4 VIP_HAD4
4.12 VIP_HAD5
4.12 VIP_HAD6

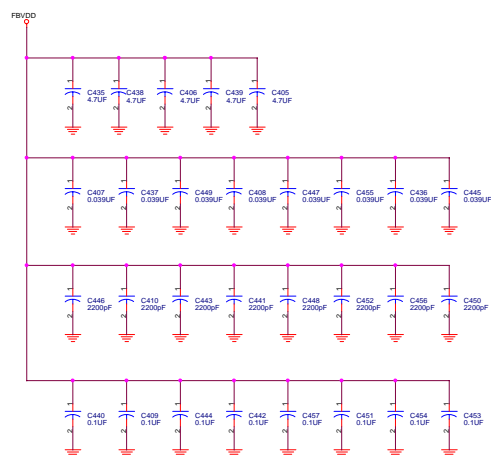
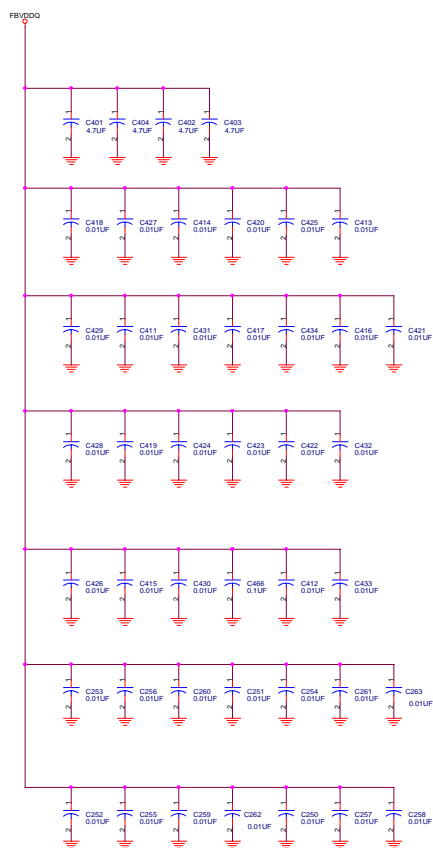


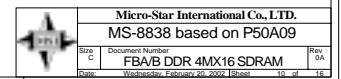
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EC01373: - Moved 75 ohm termination closer to filter for noise level reduction. Replaced C303,306,309 with 75ohm and no stuffed R208-210.



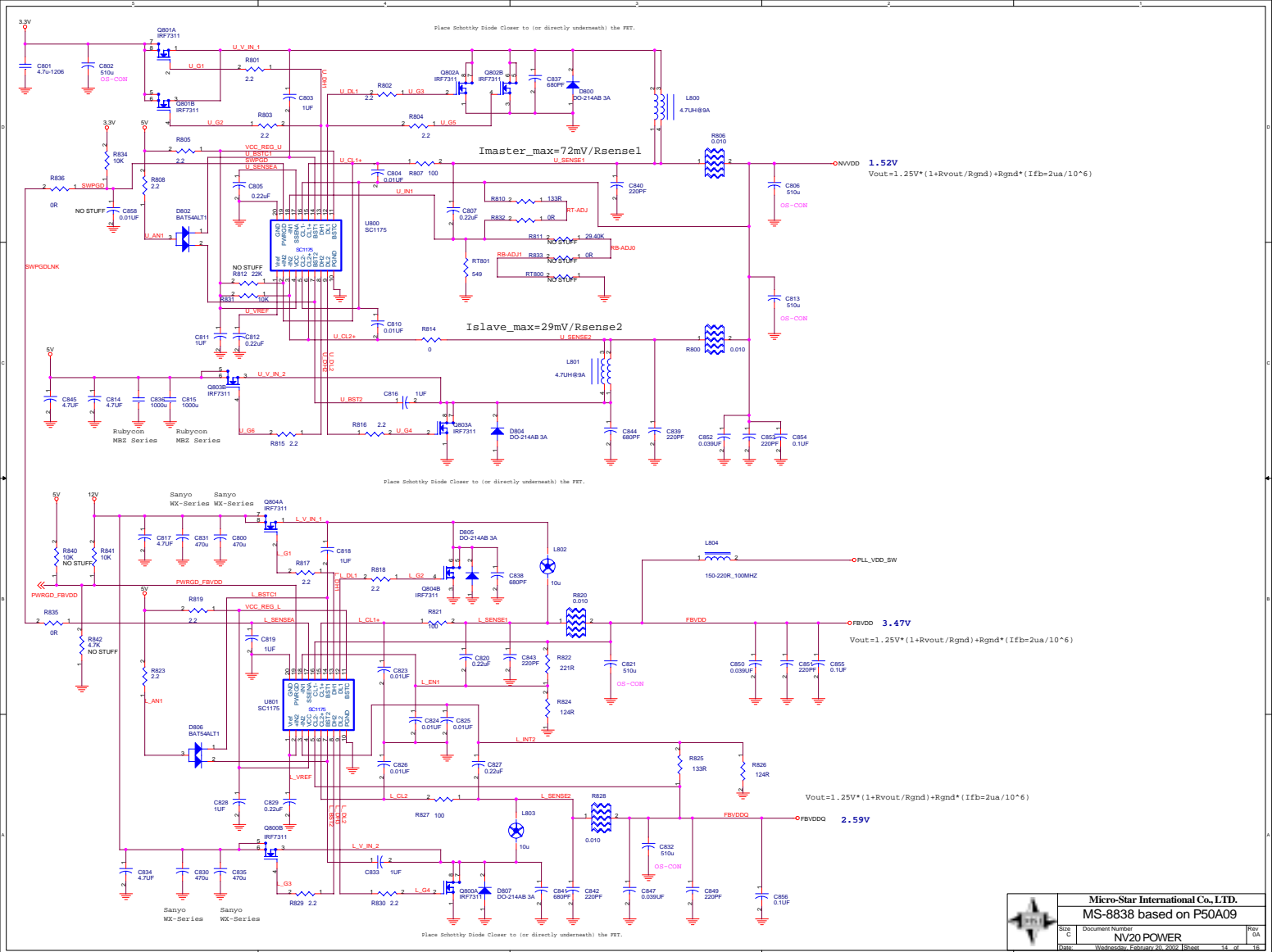






The schematic diagram illustrates the electrical connections between the CCIR camera module and the U500 module. The CCIR module's ROM_CS pin is connected to the U500's CE pin. The VIP_HAD7 and VIP_HAD6 pins of the CCIR module are connected to the U500's OE and WE pins, respectively. The U500 module's GND pin is connected to the common ground. The U500 module's VDD pin is connected to a 3.3V supply through a 0.1uF capacitor (C500). The U500 module's pins for VIP_VIDEO0 through VIP_VIDEO21 are connected to the CCIR module's pins for CCIR_DATA0 through CCIR_DATA7. The U500 module's pins for NC/A16 and NC/A17 are connected to the common ground. The U500 module's pins for NC/A16 and NC/A17 are connected to the common ground. The U500 module's pins for NC/A16 and NC/A17 are connected to the common ground.



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D									
C									
B									
A									

	5	4	3	2	1												
D	 P300-1 SCREW	 PCB 0.01UF															
	 P300-2 SCREW	 B-SCREW 0.01UF															
C	 HEATSINK HEATSINK																
	 BRACKET BRACKET																
B																	
A					<table><tr><td colspan="3">Title</td></tr><tr><td colspan="3">MS-8838 based on P50A09</td></tr><tr><td>Size A</td><td>Document Number <Doc></td><td>Rev 0A</td></tr><tr><td colspan="2">Date: Wednesday, February 20, 2002</td><td>Sheet 16 of 16</td></tr></table>	Title			MS-8838 based on P50A09			Size A	Document Number <Doc>	Rev 0A	Date: Wednesday, February 20, 2002		Sheet 16 of 16
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