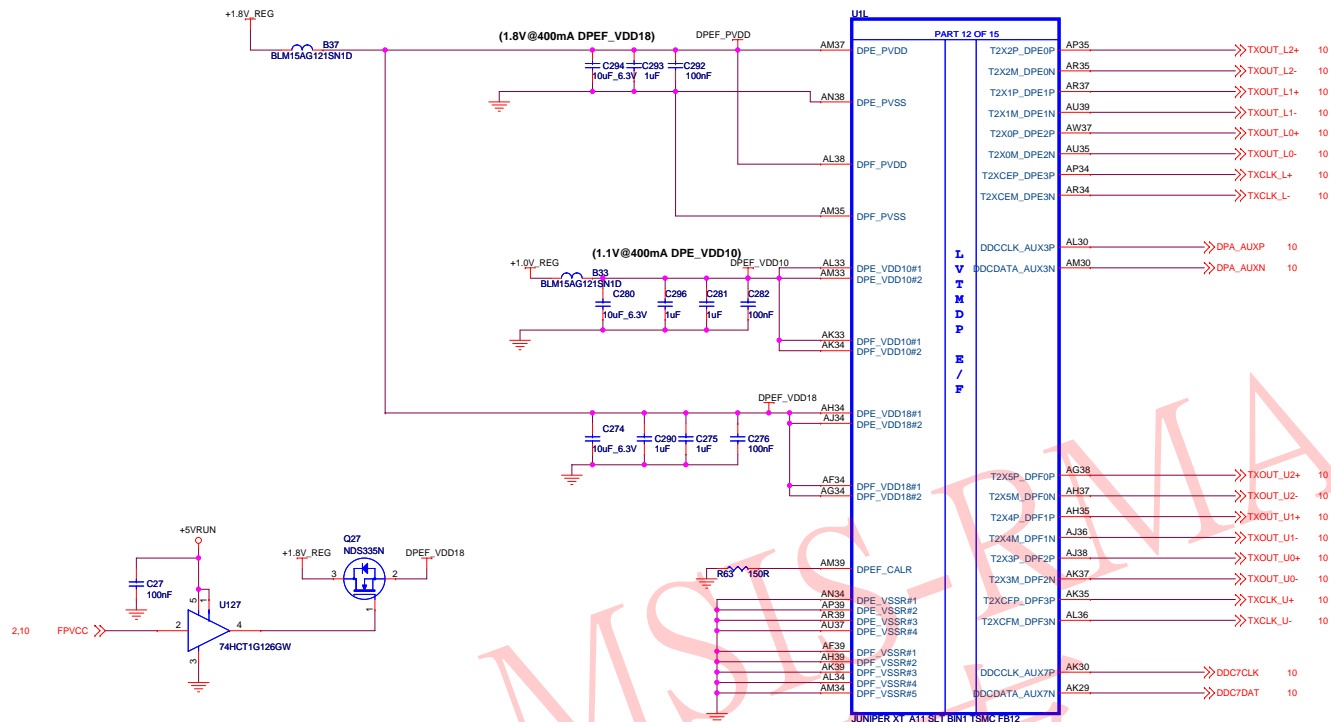


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 Markham, Ontario  
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 Title RH Redwood/ Broadway M2 package MXM3.0 DDR3  
 Doc No. 105-C076XX-00B



Rev 0



AP35 TXOUT\_L2+ 10

AR35 TXOUT\_L2- 10

AR37 TXOUT\_L1+ 10

AU39 TXOUT\_L1- 10

AW37 TXOUT\_L0+ 10

AU35 TXOUT\_L0- 10

AP34 TXCLK\_L+ 10

AR34 TXCLK\_L- 10

AL30 DPA\_AUXP 10

AM30 DPA\_AUXN 10

AG38 TXOUT\_U2+ 10

AH37 TXOUT\_U2- 10

AH35 TXOUT\_U1+ 10

AJ36 TXOUT\_U1- 10

AJ38 TXOUT\_U0+ 10

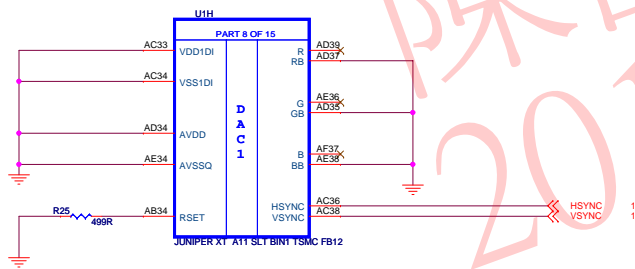
AK37 TXOUT\_U0- 10

AK35 TXCLK\_U+ 10

AL36 TXCLK\_U- 10

AK30 DDC7CLK 10

AK29 DDC7DAT 10



AC33 VDD1DI

AC34 VSS1DI

AD34 AVDD

AE34 AVSSQ

AB34 RSET

AD39 R

AD37 RB

AE36 G

AD35 GB

AF37 B

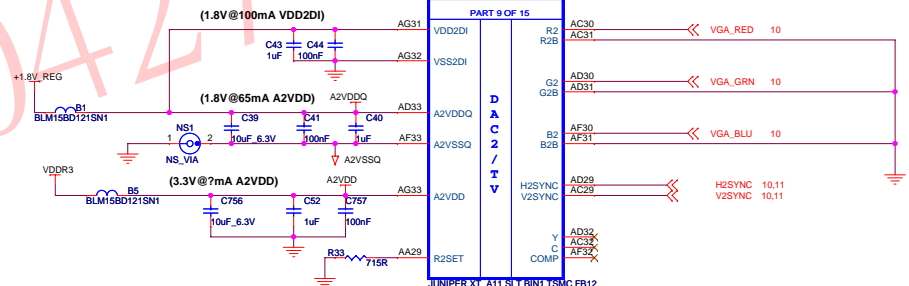
AE38 BB

AC36 HSYNC

AC38 VSYNC

11 HSYNC

11 VSYNC



AC30 VGA\_RED 10

R2B AC31

G2B AD30 VGA\_GRN 10

AD31

B2B AF30 VGA\_BLU 10

AF31

AD29 H2SYNC 10,11

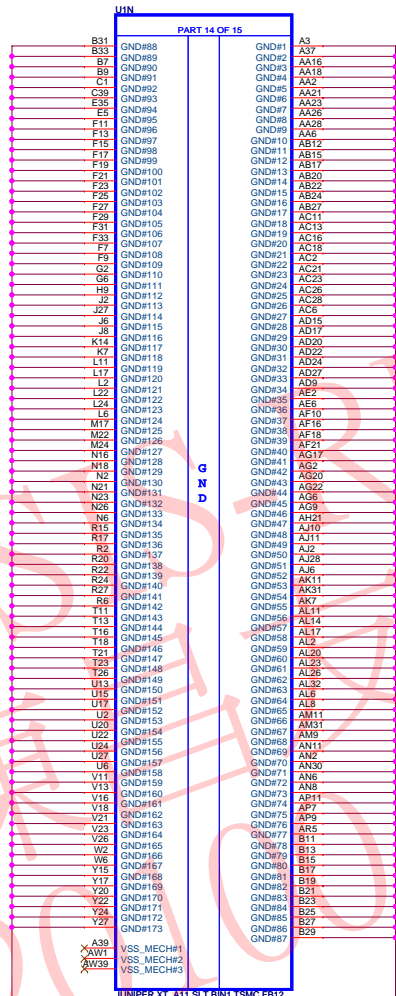
AC29 V2SYNC 10,11

AD32 Y

AC33 C

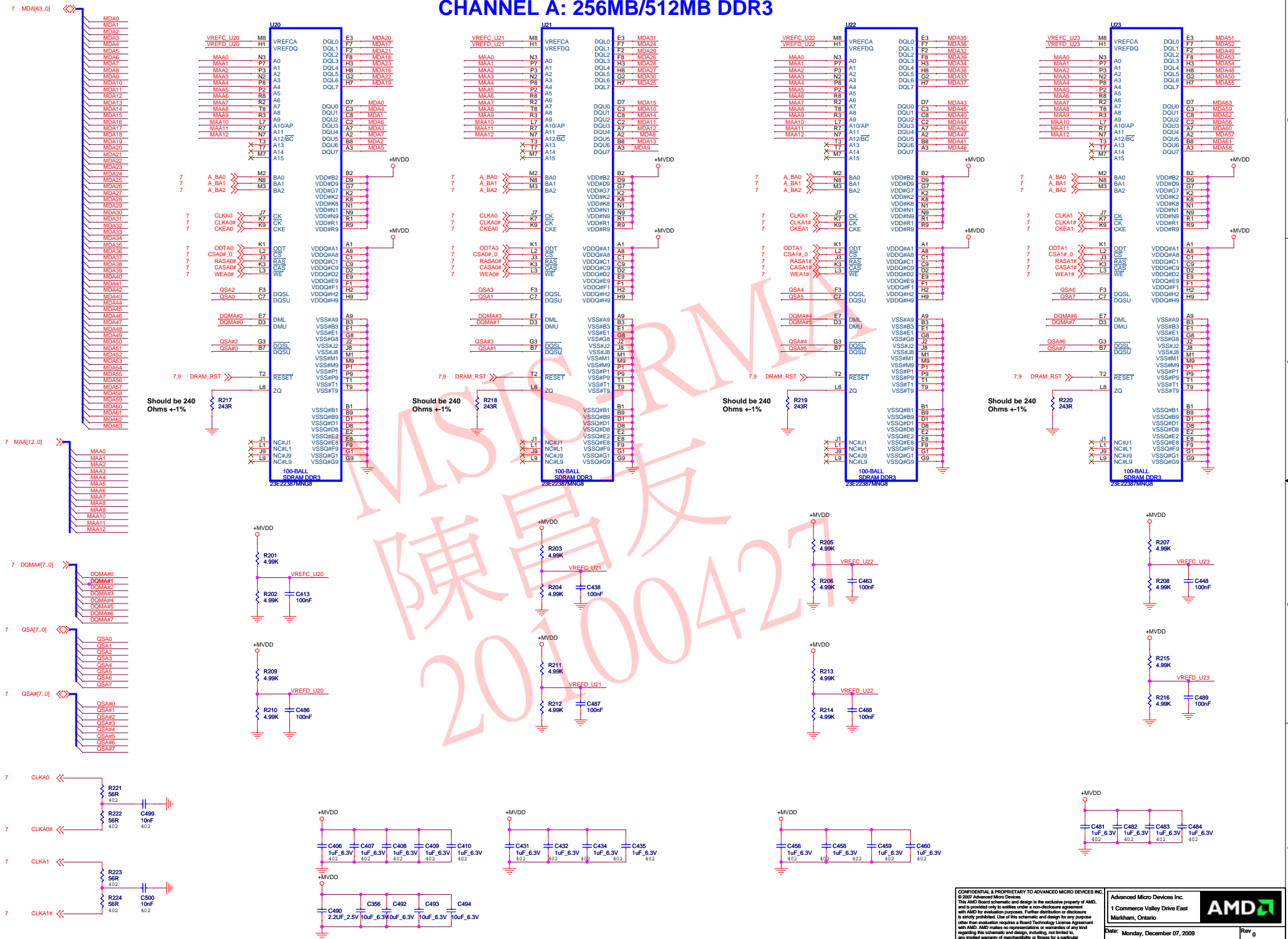
AF33 COMP








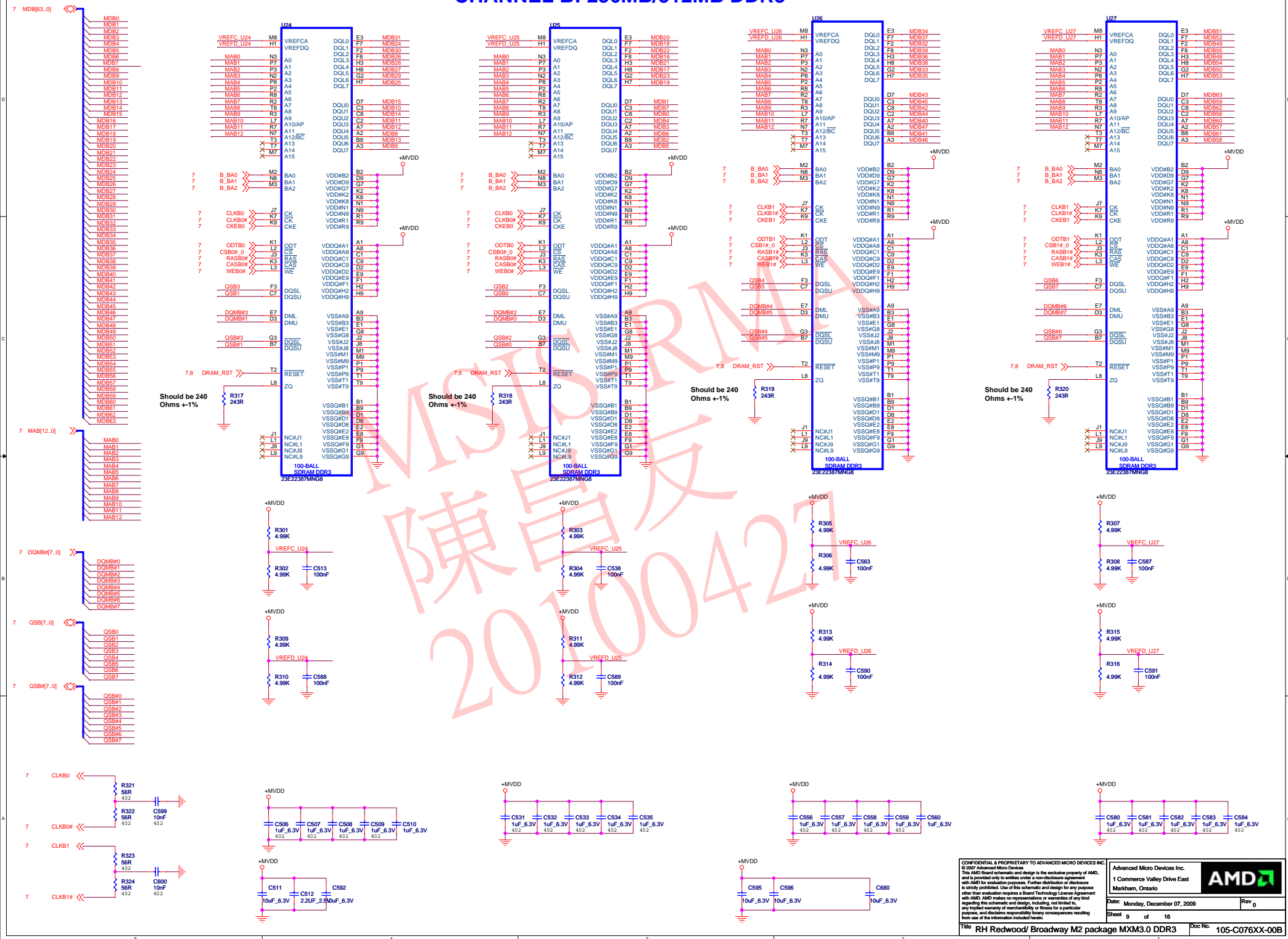
**CHANNEL A: 256MB/512MB DDR3**



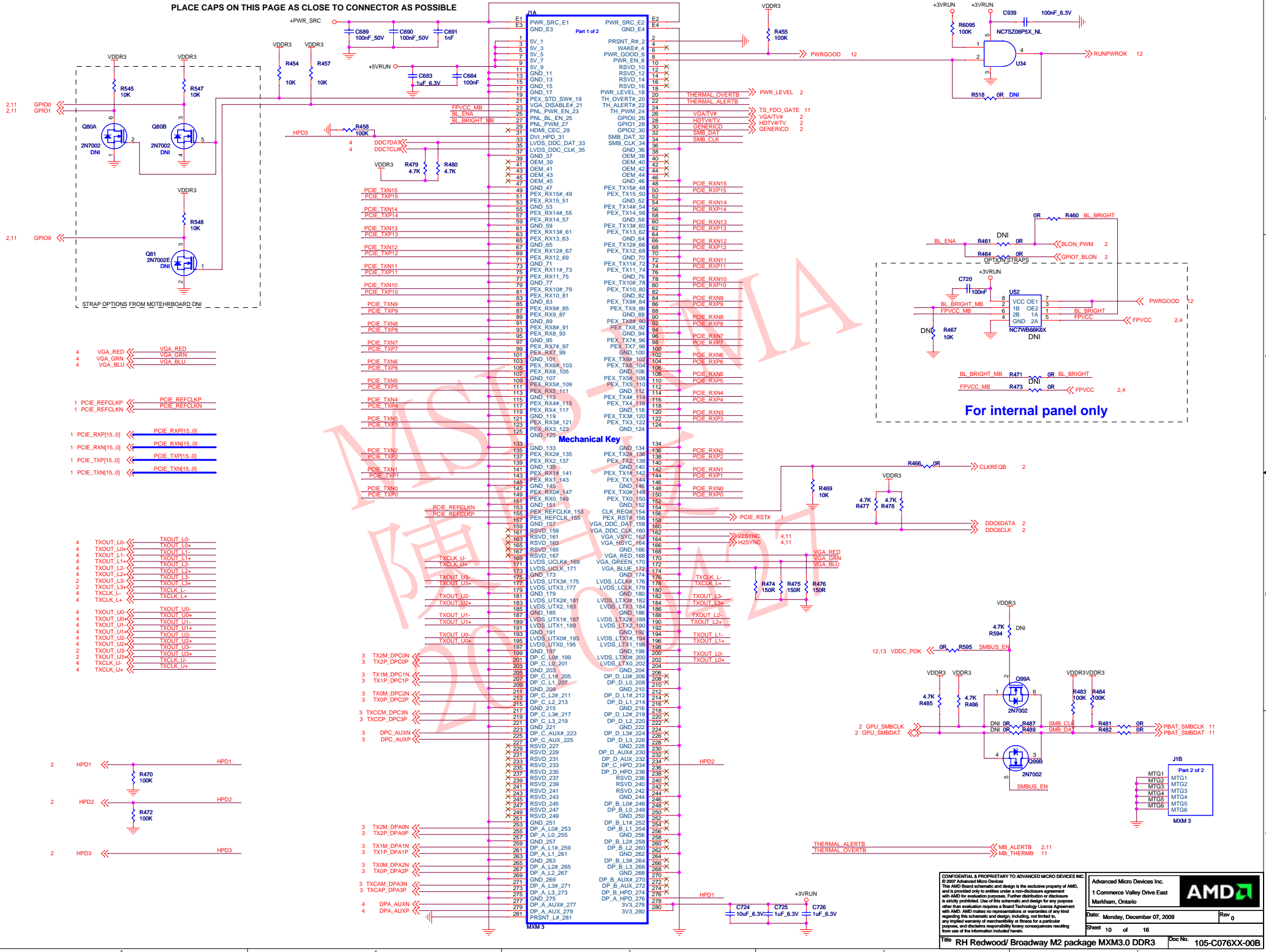
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		Date:	Monday, December 07, 2009	Rev#	0
		Sheet:	8	of	16
Title	RH Redwood/ Broadway M2 package MXM3.0 DDR3			Dwg No.	105-C076XX-00B




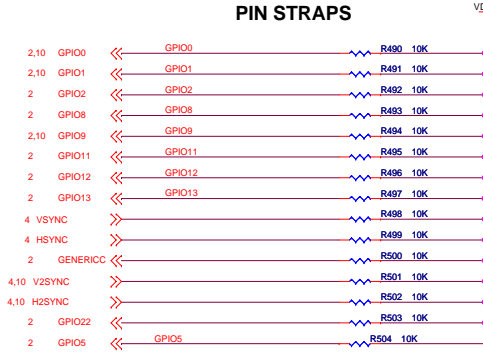
**CHANNEL B: 256MB/512MB DDR3**



PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE



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<p>Title RH Redwood/ Broadway M2 package MXM3.0 DDR3</p>	<div data-bbox="1789 1455 1992 1456"> <div>Sheet 10 of 16</div> <div>Doc No. 105-C076XX-00</div> </div>



<p><b>AMD RESERVED CONFIGURATION STRAPS</b></p> <p><b>ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</b></p>	
H2SYNC	GENERICC
<p><b>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</b></p>	
GPI0_28_TDO	GPI021_BB_EN

### Critical Temperature Fault

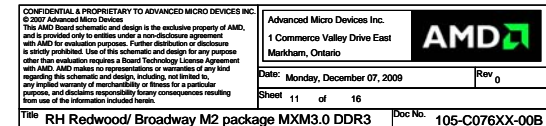
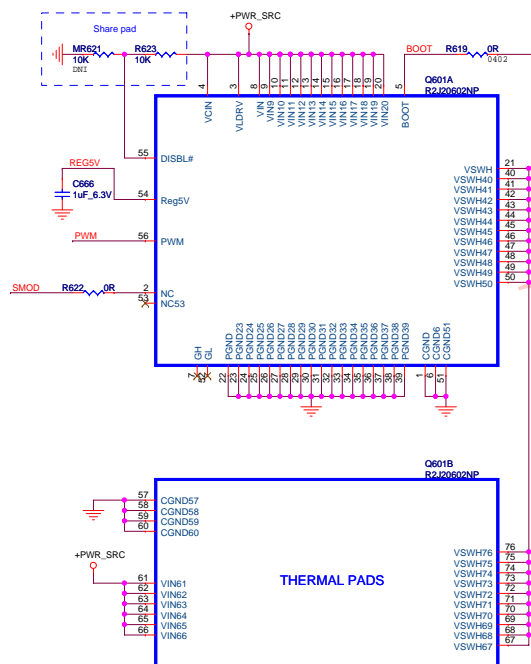
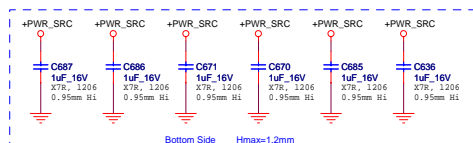


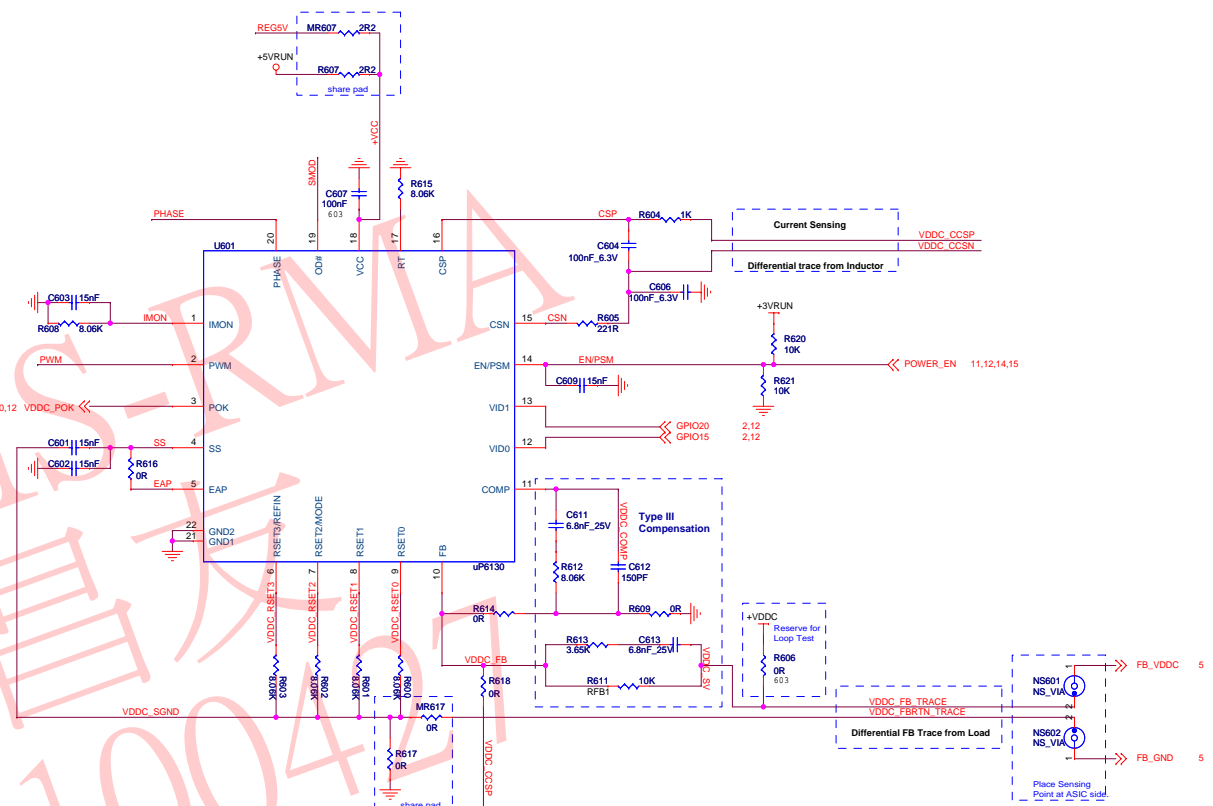
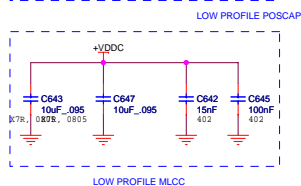


Figure 1 shows the top view of the PCB layout. It displays four capacitors (C657, C669, C638, C665) connected to the +PWR\_SRC pins. The capacitors are 2.2uF\_16V, X7R, 1206, 1.3mm HI. The layout is labeled 'Top Side' and 'Hmax=1.5mm'.



Pin Difference Between R2J2062NP and R2J2065NP		
	R2J2062NP	R2J2065NP
3	VLDRV	NC
8	VIN	NC
2	NC	LSDBL4
52	NC	TURN

Top Side Hmax=1.5mm



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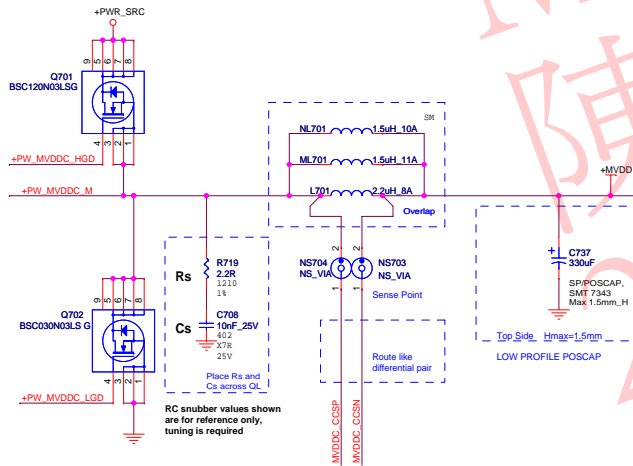
Rev

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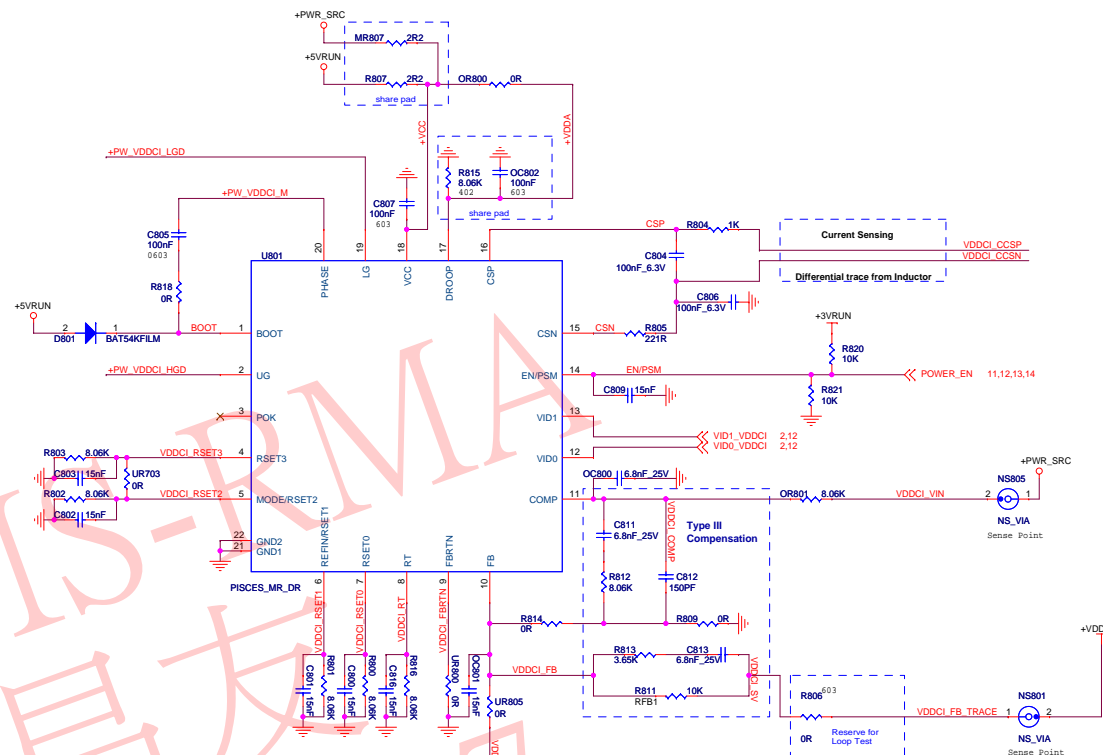
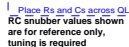
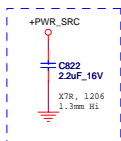
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<p><b>Title</b> RH Redwood/ Broadway M2 package MXM3.0 DDR3</p>	<p><b>Date:</b> Monday, December 07, 2009 <b>Rev</b> 0  <b>Sheet</b> 14 of 16  <b>Doc No.</b> 105-C076XX-00B</p>



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<p>Title: RH Redwood/ Broadway M2 package MXM3.0 DDR3</p>		<p>Doc No: 105-C076XX-00B</p>			

<div>AMD</div>			Title		Schematic No.		Date:	
			RH Redwood/ Broadway M2 package MXM3.0 DDR3		105-C076XX-00B		Monday, December 07, 2009	
			REVISION HISTORY		NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.			Rev 0
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION					
0	00A	09/27/09	Create new SCHs					
	00B	12/03/09	Added PWR_EN short to DrMOS Added DrMOS Thermal Pad					
			<div>MSIS-RMA</div> <div>陳昌友</div> <div>20100427</div>					