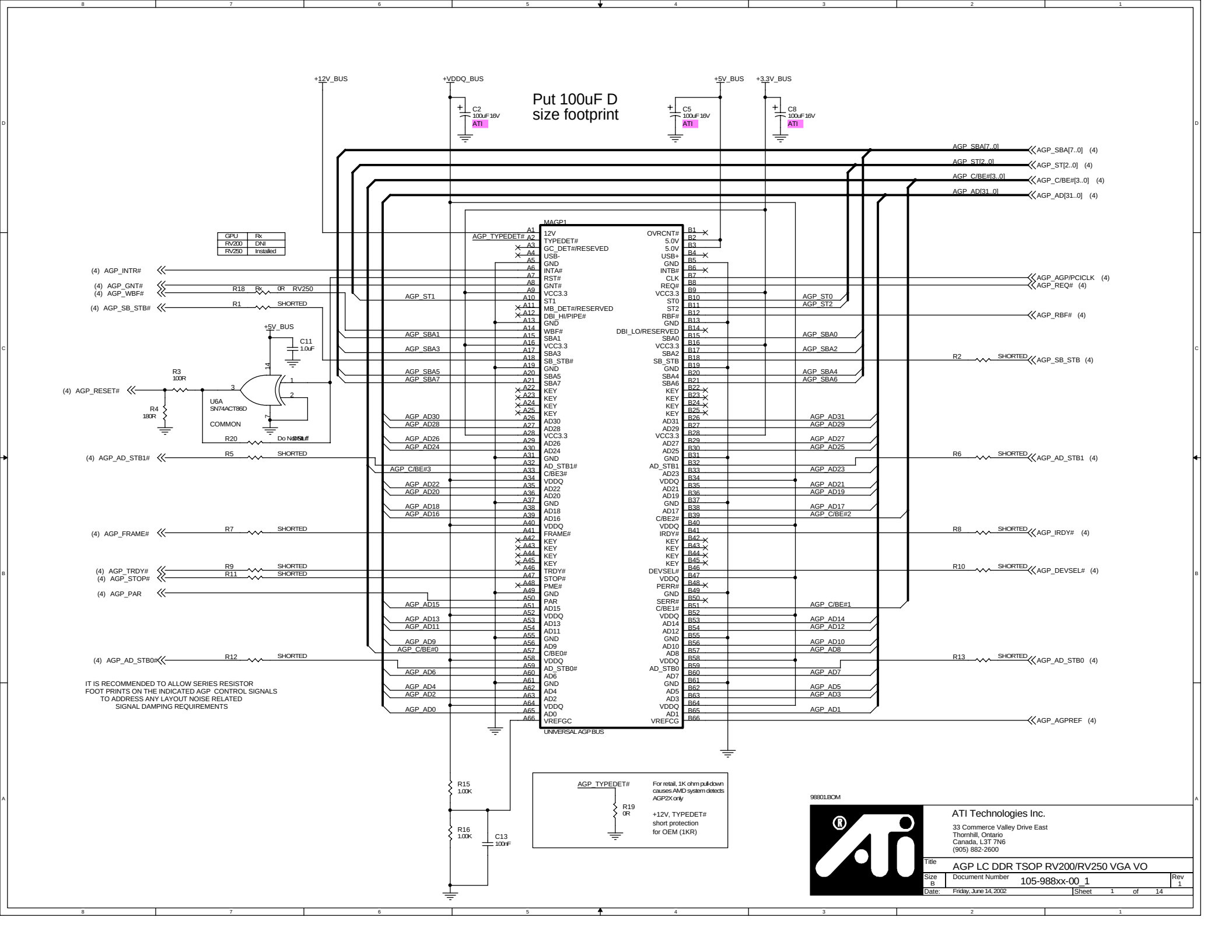
+12V_BUS
+VDDQ_BUS
+5V_BUS
+3.3V_BUS
Put 100uF D size footprint
C2 100uF 16V ATI
C5 100uF 16V ATI
C8 100uF 16V ATI
MAGP1
UNIVERSAL AGP BUS
AGP_SBA[7..0]
AGP_ST[2..0]
AGP_C/BE#[3..0]
AGP_AD[31..0]
AGP_AGP/PCICLK
AGP_REQ#
AGP_RBF#
AGP_SB_STB
AGP_AD_STB1
AGP_IRDY#
AGP_DEVSEL#
AGP_AD_STB0
AGP_AGPREF
AGP_TYPEDET#
R19 0R
For retail, 1K ohm pull-down causes AMD system detects AGP2X only
+12V, TYPEDET# short protection for OEM (1KR)
R15 1.00K
R16 1.00K
C13 100nF
GPU | Rx
RV200 | DNI
RV250 | Installed
R18 Rx 0R RV250
R1 SHORTED
C11 1.0uF
R3 100R
R4 180R
U6A SN74ACT86D
COMMON
R20 Do Not Stuff
R5 SHORTED
R2 SHORTED
R6 SHORTED
R7 SHORTED
R8 SHORTED
R9 SHORTED
R11 SHORTED
R10 SHORTED
R12 SHORTED
R13 SHORTED
IT IS RECOMMENDED TO ALLOW SERIES RESISTOR FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS TO ADDRESS ANY LAYOUT NOISE RELATED SIGNAL DAMPING REQUIREMENTS
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ATI Technologies Inc.
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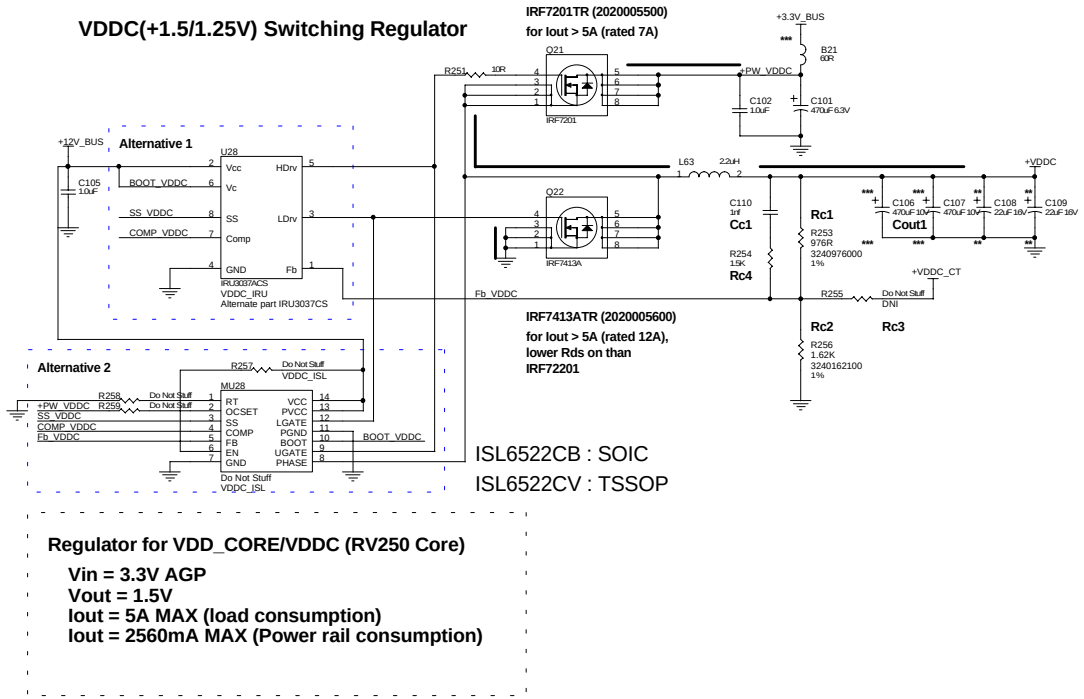
VDDC(+1.5/1.25V) Switching Regulator



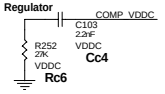
Regulator for VDD_CORE/VDDC (RV250 Core)

Vin = 3.3V AGP
Vout = 1.5V
Iout = 5A MAX (load consumption)
Iout = 2560mA MAX (Power rail consumption)

Compensation Options for VDDC Regulator

Alt. Compensation 1

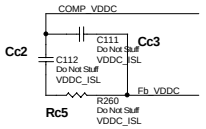
This compensation circuit is simplified and will only work with the IRU3037(A) Regulator



Common

Alt. Compensation 2

This is required for the ISL6522CB regulator, and provides maximum regulation speed for IRU3037 Regultor



Note: Alternative Compensation Circuit 2 will only work if Rc1 is a 1k Ohm Resistor. Alternative Compensation Circuit 1 has no requirements for the divider circuit.

Cout1 470uF thru hole capacitor (P/N 4051047700) has 30mR ESR where as 470uF SMT (P/N 4262047700) capacitor has 150mR ESR. For current below 4.5A, 1 thru 470uF is enough.

******* Indicates number of vias required for the connection

Part	INSTALL	Compensation Circuit	DO NOT INSTALL
IRU3037 IRU3037A	Alternative1	Common, and Either Alt. Compensation 1, or Alt. Compensation 2	Cc4, Rc6 Alternative 2
ISL6522CB	Alternative2	Common and Alt. Compensation 2	Alternative1

Table for IRU3037 and IRU3037A with Alt. Compensation Circuit 1

Part		Rc1	Rc2	Rc3
IRU3037	0.9V	887R 1%	DNI	1.40K 1%
	1.2V	110R 1%	DNI	1.21K 1%
	1.25V	1.00K 1%	DNI	DNI
	1.4V	511R 1%	6.49K 1%	DNI
	1.5V	1.33K 1% 511R 1%	6.49k 1% 2.43K 1%	DNI DNI
IRU3037A	0.9V	1.00K 1%	8.06K 1%	DNI
	1.2V	1.00K 1%	2.00K 1%	DNI
	1.25V	976R 1% 1.00K 1%	1.62K 1% 1.78K 1%	DNI DNI
	1.5V	1.00K 1%	1.15k 1%	DNI

Table for IRU3037, IRU3037A and ISL6522 with Alt. Compensation Circuit 2

Part		Rc1	Rc2	Rc3
IRU3037	0.9V	1.00K 1%	DNI	1.56K 1%
	1.2V	1.00K 1%	DNI	11K 1%
	1.25V	1.00K 1%	DNI	DNI
	1.5V	1.00K 1%	4.99K 1%	DNI
IRU3037A ISL6522C	0.9V	1.00K 1%	8.06K 1%	DNI
	1.2V	1.00K 1%	2.00K 1%	DNI
	1.25V	1.00K 1%	1.78K 1%	DNI
	1.5V	1.00K 1%	1.15k 1%	DNI

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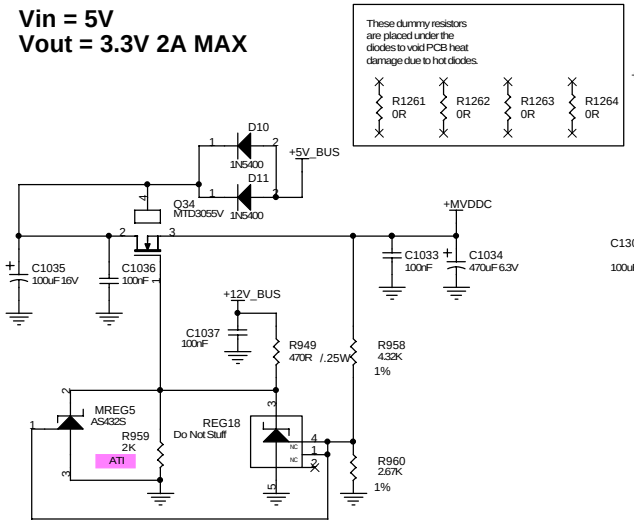
Regulator for VDD_CORE/VDDC

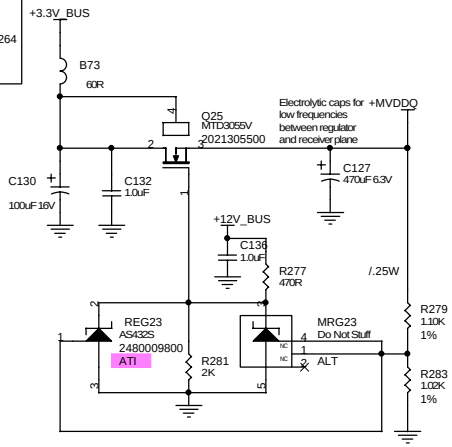
Vin = 5V
Vout = 3.3V 2A MAX



Regulator for MVDDQ (MEM IO)

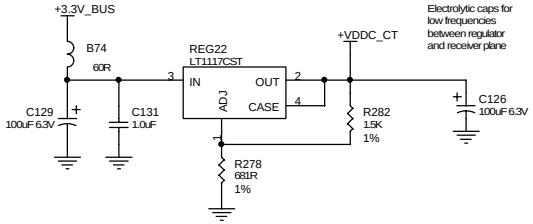
Vin = 3.3V

Vout = 2.5V 1A MAX

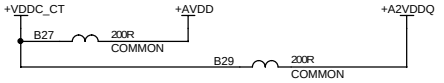


Regulator for VDDC_CT (Core Transform) and AVDD/A2VDDQ/AVDDDI/A2VDDDI TXVDDR, LVDDRx

Vin = 3.3V **Vout = 1.85V 0.8A MAX**

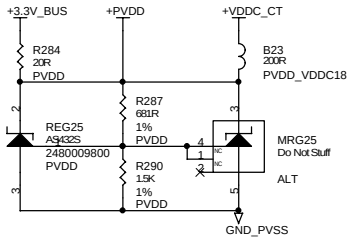


AVDD/A2VDDQ (1st DAC & 2nd DAC Band Gap)



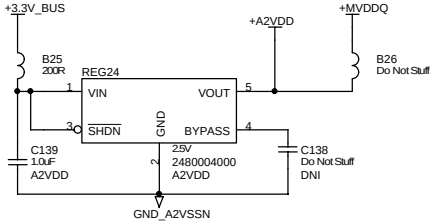
Regulator for PVDD (R200 PLLs) and optional TPVDD (TMDS PLLs)

Vin = 3.3V
Vout = 1.8V 75mA MAX



Regulator For A2VDD (2nd DACs)

Vin = 3.3V
Vout = 2.5V
Iout = 120mA MAX



A2VDD and A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch. A2VSSN with single via to GND at the regulator

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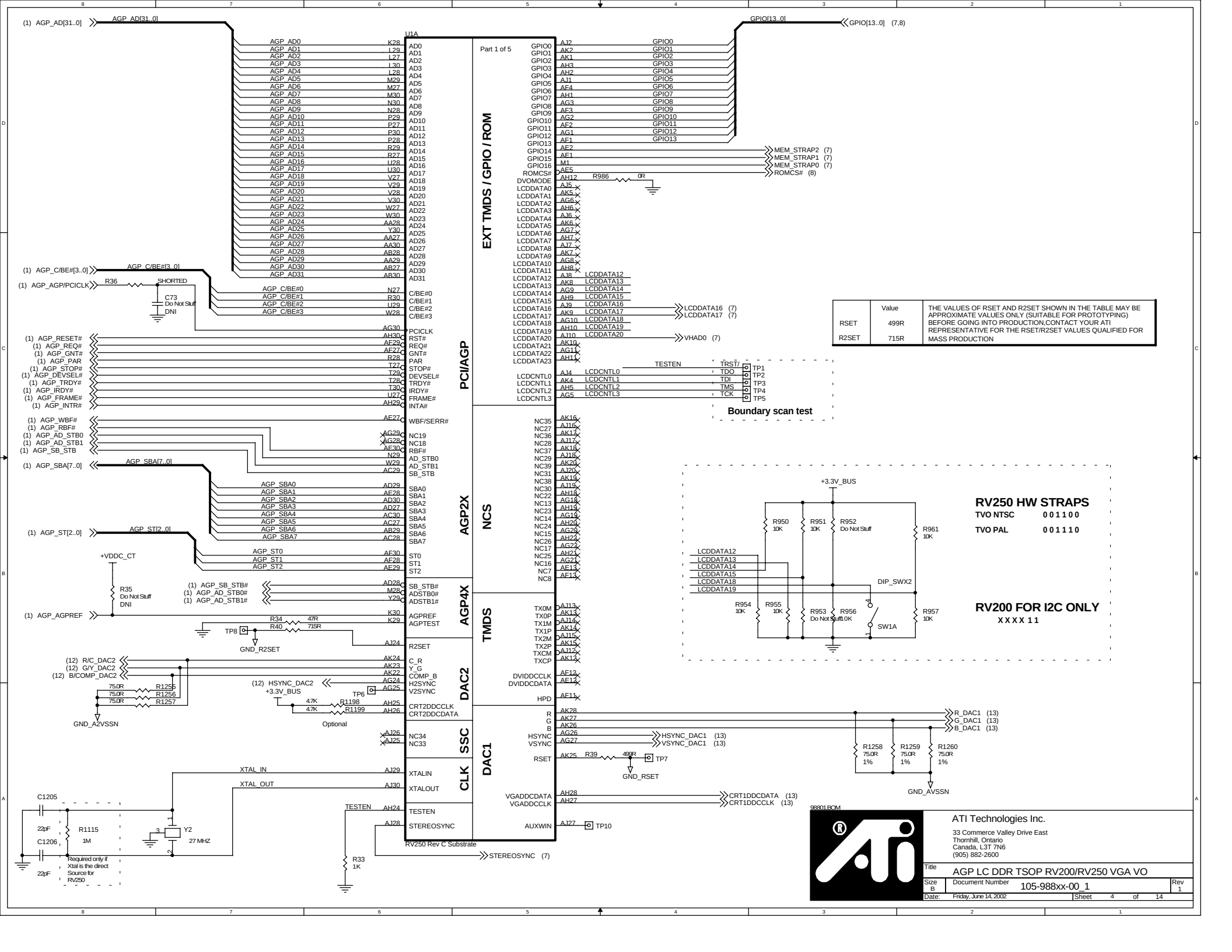

	Value	
RSET	499R	THE VALUES OF RSET AND R2SET SHOWN IN THE TABLE MAY BE APPROXIMATE VALUES ONLY (SUITABLE FOR PROTOTYPING) BEFORE GOING INTO PRODUCTION,CONTACT YOUR ATI REPRESENTATIVE FOR THE RSET/R2SET VALUES QUALIFIED FOR MASS PRODUCTION
R2SET	715R	

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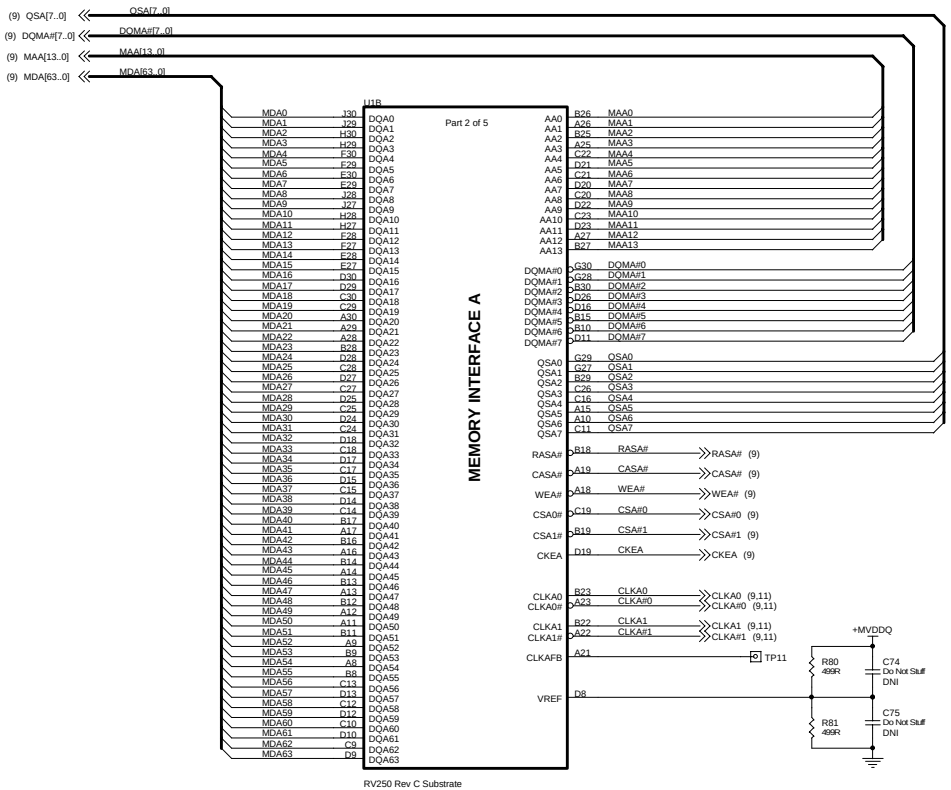
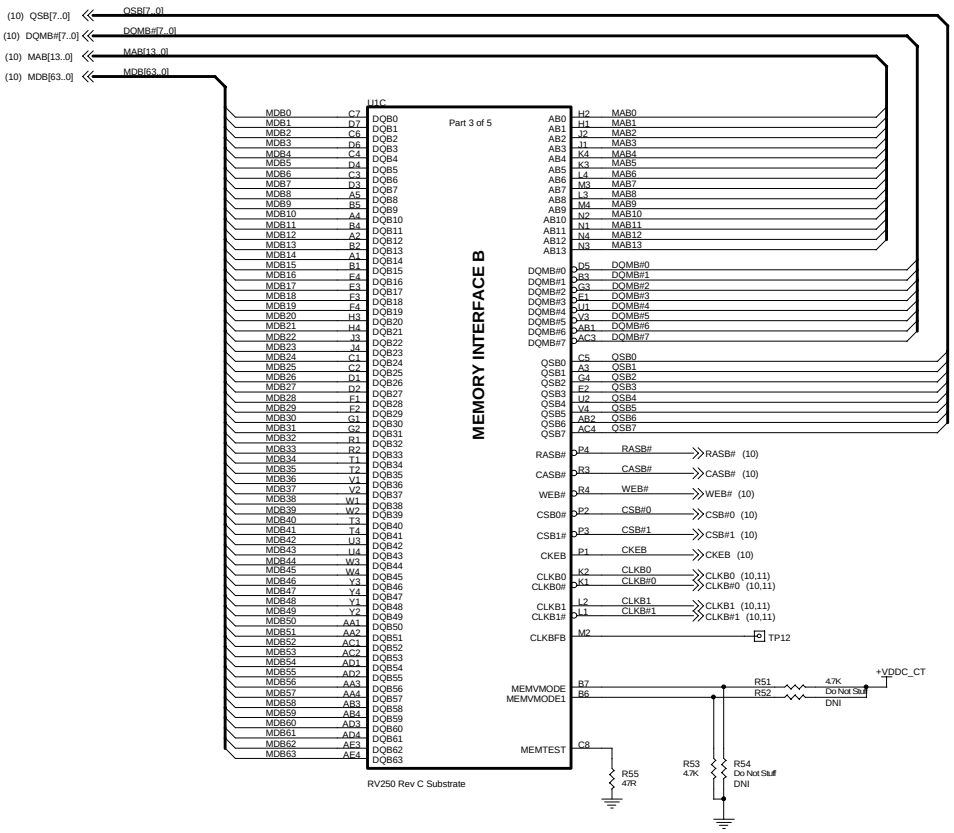
MEMORY CHANNEL A



MEMORY CHANNEL B



MEMVMODE[1:0]	MEMORY IO VOLTAGE	
0	2.5V (DDR)	Default
1		
1 0	1.8V (DDR)	
1 1	3.3V (SDR)	

All references to SDR Memory in this schematic are for legacy support of the RV200 chip.

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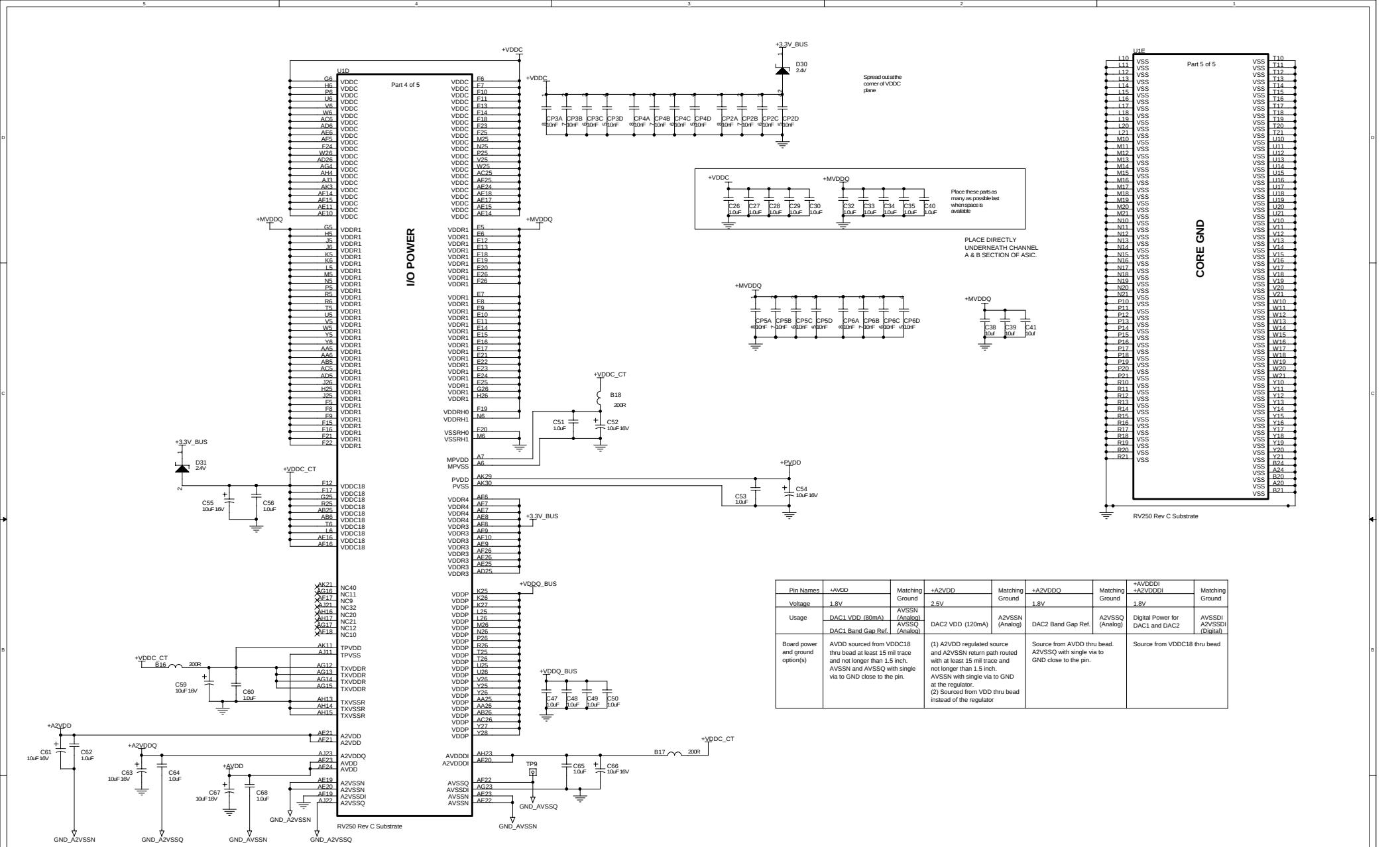

Pin Names	+AVDD	Matching Ground	+A2VDD	Matching Ground	+A2VDDQ	Matching Ground	+AVDDI +A2VDDDI	Matching Ground
Voltage	1.8V		2.5V		1.8V		1.8V	
Usage	DAC1 VDD (80mA)	AVSSN (Analog)	DAC2 VDD (120mA)	A2VSSN (Analog)	DAC2 Band Gap Ref.	A2VSSQ (Analog)	Digital Power for DAC1 and DAC2	AVSSDI A2VSSDI (Digital)
	DAC1 Band Gap Ref.	AVSSQ (Analog)						
Board power and ground option(s)	AVDD sourced from VDDC18 thru bead at least 15 mil trace and not longer than 1.5 inch. AVSSN and AVSSQ with single via to GND close to the pin.		(1) A2VDD regulated source and A2VSSN return path routed with at least 15 mil trace and not longer than 1.5 inch. AVSSN with single via to GND at the regulator. (2) Sourced from VDD thru bead instead of the regulator		Source from AVDD thru bead. A2VSSQ with single via to GND close to the pin.		Source from VDDC18 thru bead	

These are not electrically connected on the schematic. Consult the design guide for proper routing of grounds.

The following grounds should be routed back to their respective regulators and then tied directly to the ground plane with one via: GND_PVSS, GND_MPVSS, GND_TPVSS, and GND_A2VSSN. The other ground pins (GND_AVSSN, GND_A2VSSQ, GND_RSET, GND_R2SET) should be tied to the ground plane directly through one via as close to the pins as possible without connecting to anything else. If space is an issue it is possible to use one via for two adjacent pins.

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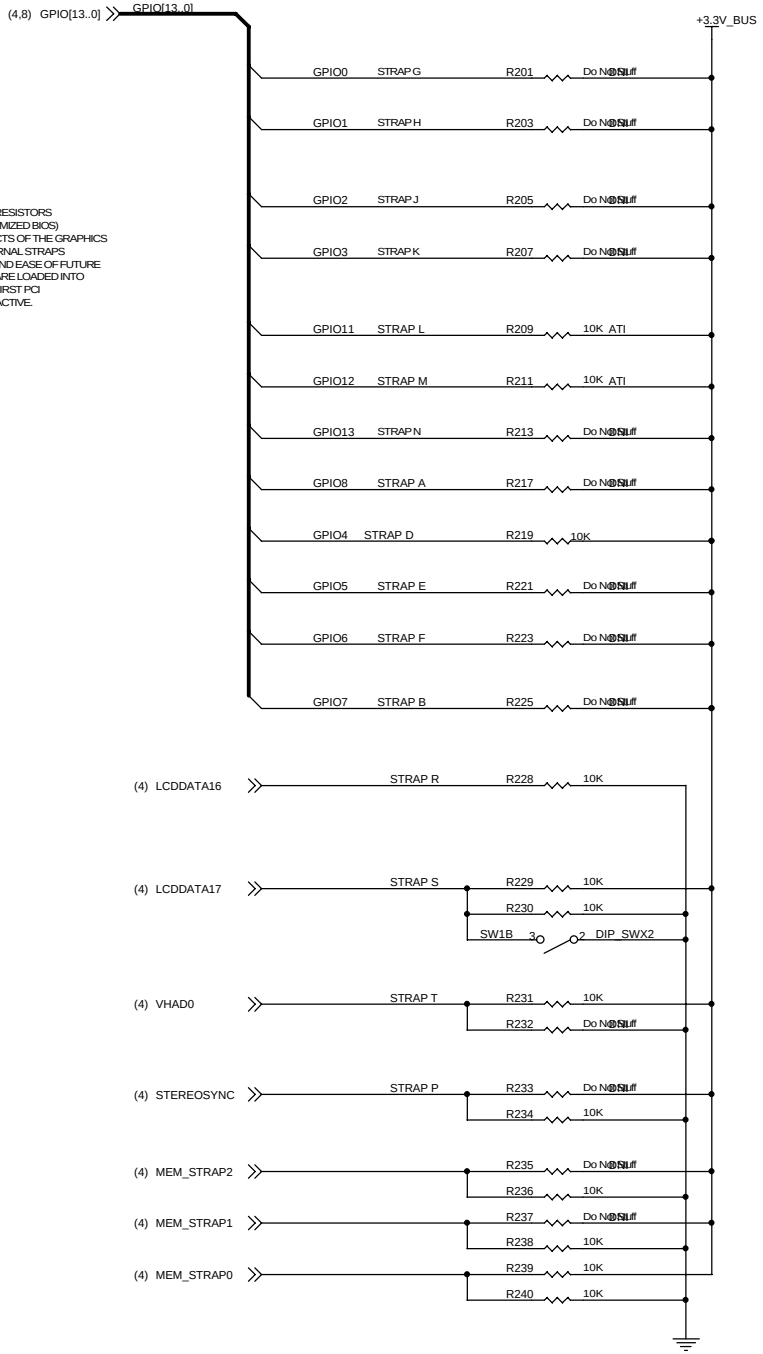
OPTION STRAPS



NOTE: THE RV250
SUPPORTS THE USE OF STRAP RESISTORS
(AS AN ALTERNATIVE TO CUSTOMIZED BIOS)
TO CONFIGURE CERTAIN ASPECTS OF THE GRAPHICS
SUBSYSTEM. THE USE OF EXTERNAL STRAPS
PROVIDES ADDED FLEXIBILITY AND EASE OF FUTURE
UPGRADE. STRAPPED VALUES ARE LOADED INTO
INTERNAL REGISTERS ON THE FIRST PCI
COMMAND AFTER RESET# IS INACTIVE.

NOTE:
THE I/O BUFFERS HAVE WEAK PULLDOWN RESISTORS, IT IS
RECOMMENDED TO RE-INFORCE THESE PULLDOWNS WITH
STRAPS TO GROUND VIA 10K RESISTORS
THIS DICTATES THE FOLLOWING STRAP

CONFIGURATION:
STRAP TO VCC VIA 10K RESISTOR.
STRAP TO GROUND VIA 10K RESISTOR.
THIS PROVIDES THE LOGIC LEVELS SHOWN:
'0' WHEN 10K RESISTOR TO GROUND INSTALLED
'1' WHEN 10K RESISTOR TO +3.3V_BUS INSTALLED.

TO BE CHECKED

STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM **1011 - Serial M25P10 ROM (ST), chip IDis from ROM** 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1001
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000 (internal pull-down)
VGA_DISABLE	GPIO(7)	**0 - VGA controller capabillity enableed.** 1 - The device will not be recognized as the systemis VGA controller.	0
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select **00 - single function device.** 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	00
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

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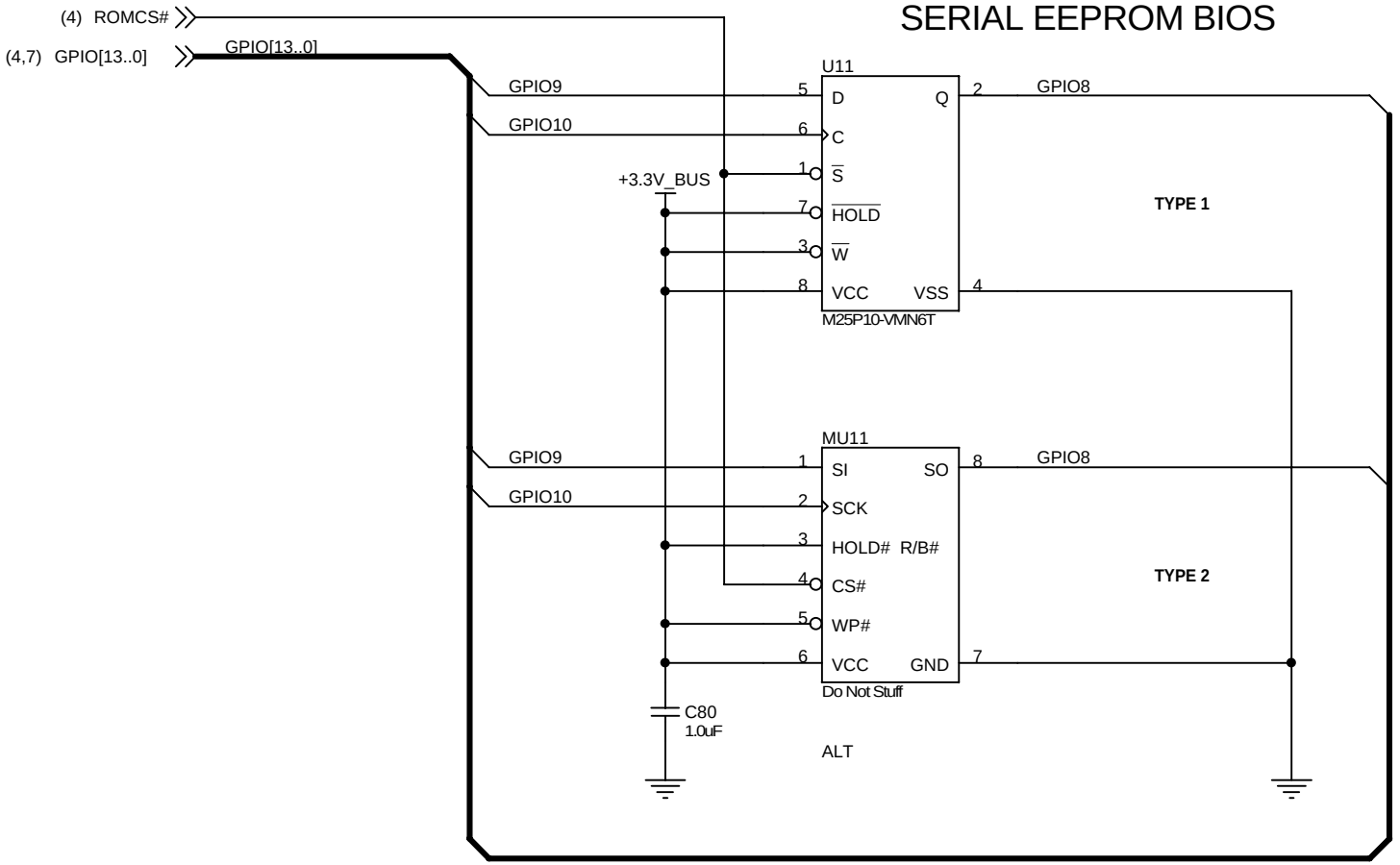
SERIAL EEPROM BIOS



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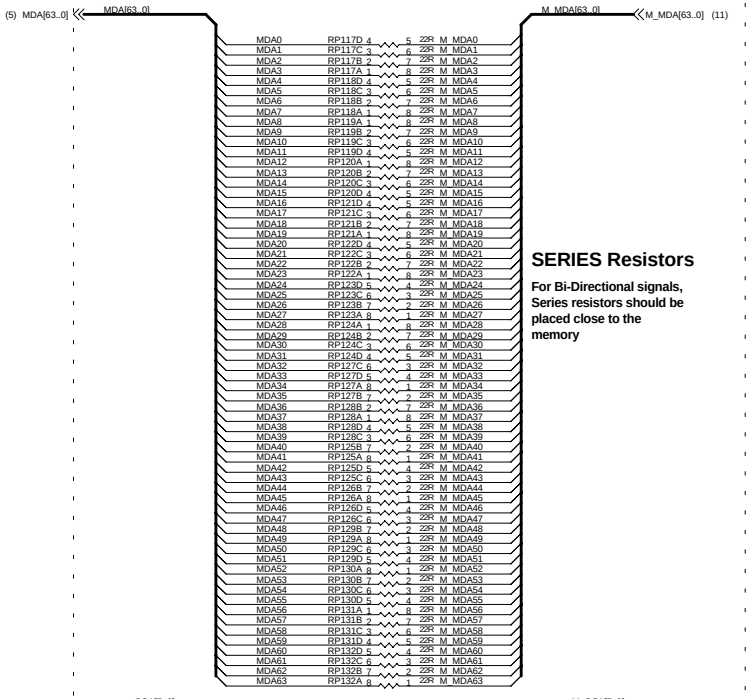
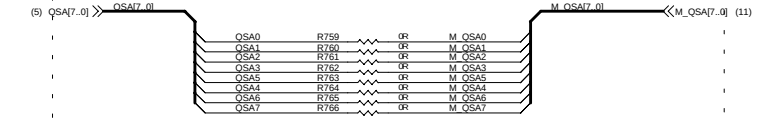
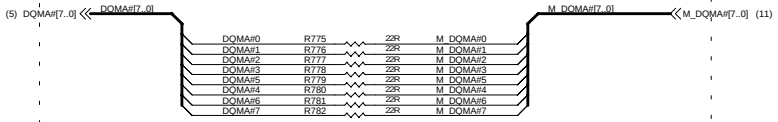
TERMINATION FOR MEMORY CHANNEL A

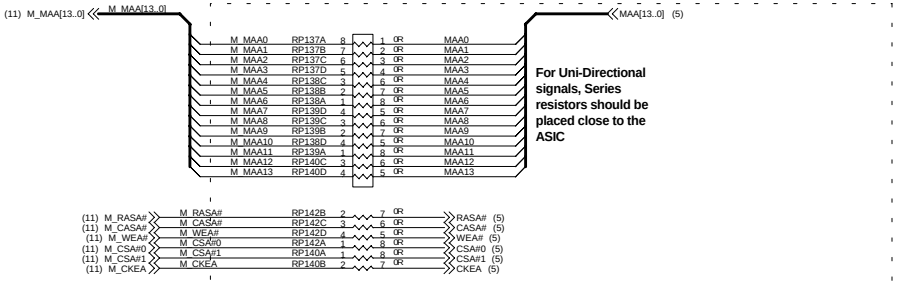


SERIES Resistors

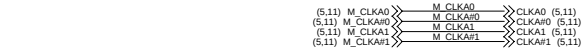
For Bi-Directional signals, Series resistors should be placed close to the memory







For Uni-Directional signals, Series resistors should be placed close to the ASIC

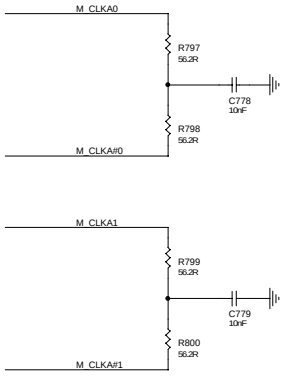


Differential CLOCK termination

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

CLOCK terminations

These resistors and caps must be placed to minimize any stubs. These must also be placed close to the memory



Clocks can be terminated in several ways. This circuitry shows complementary termination for Differential Clocks in conjunction with standard memory interface terminations (Series or Parallel). If Series termiation is used, 121 Ohms Resistance between the differential lines is recommended (eg: R1168=121 Ohms, R1169=0 Ohms, C1221 DNI)..

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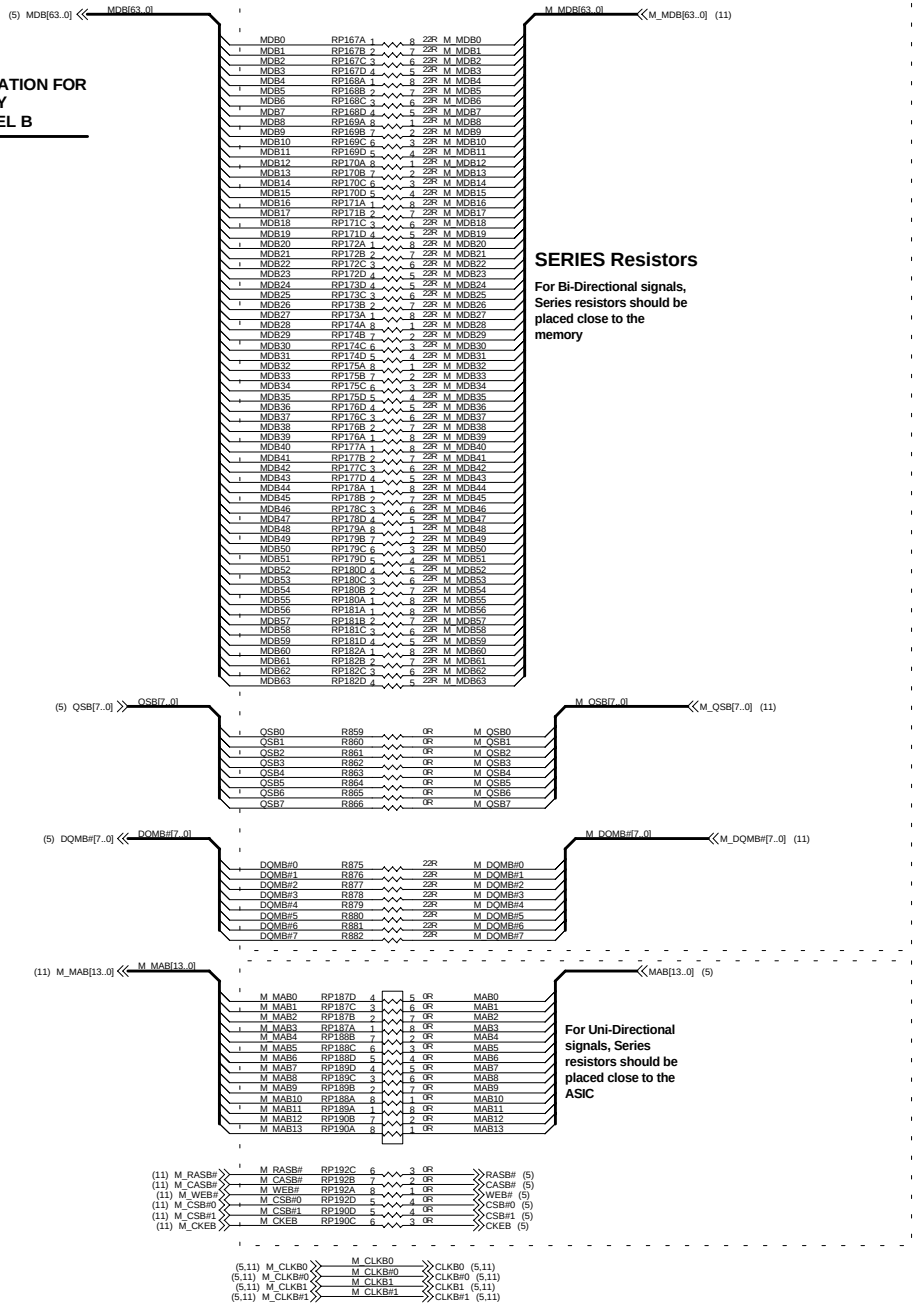
TERMINATION FOR MEMORY CHANNEL B



SERIES Resistors

For Bi-Directional signals, Series resistors should be placed close to the memory

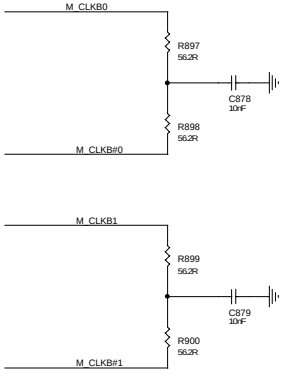
For Uni-Directional signals, Series resistors should be placed close to the ASIC

Differential CLOCK termination

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

CLOCK terminations

These resistors and caps must be placed to minimize any stubs. These must also be placed close to the memory



Clocks can be terminated in several ways. This circuitry shows complementary termination for Differential Clocks in conjunction with standard memory interface terminations (Series or Parallel). If Series termiation is used, 121 Ohms Resistance between the differential lines is recommended (eg: R1168=121 Ohms, R1169=0 Ohms, C1221 DNI)..

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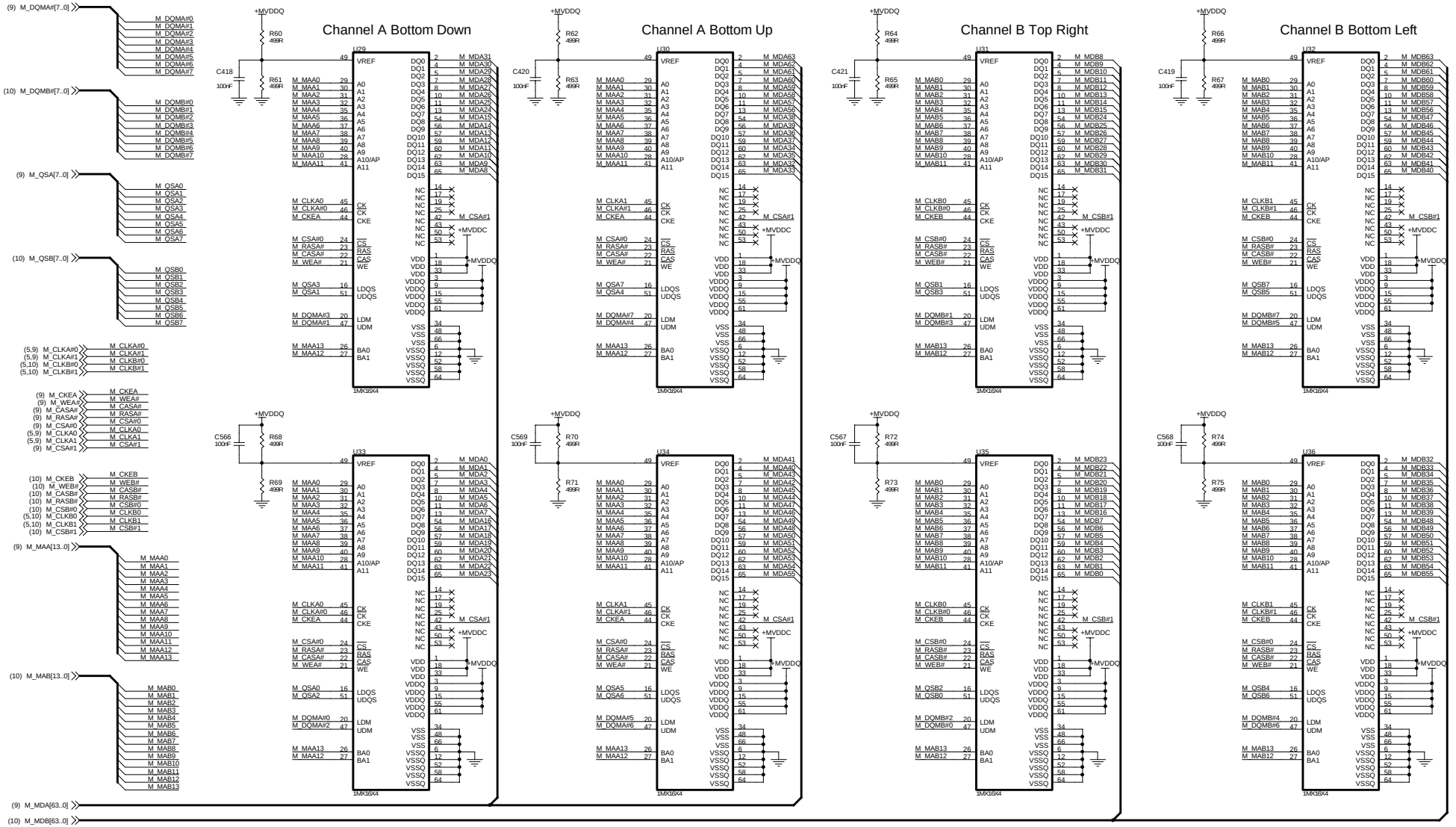
64MBytes DDR SDRAM 64Mbit 1Mx16x4



C81, C82 SHOULD BE PLACED CLOSE TO THE REFERENCE LAYER CHANGE OF CLOCKS FOR EMI REDUCE.

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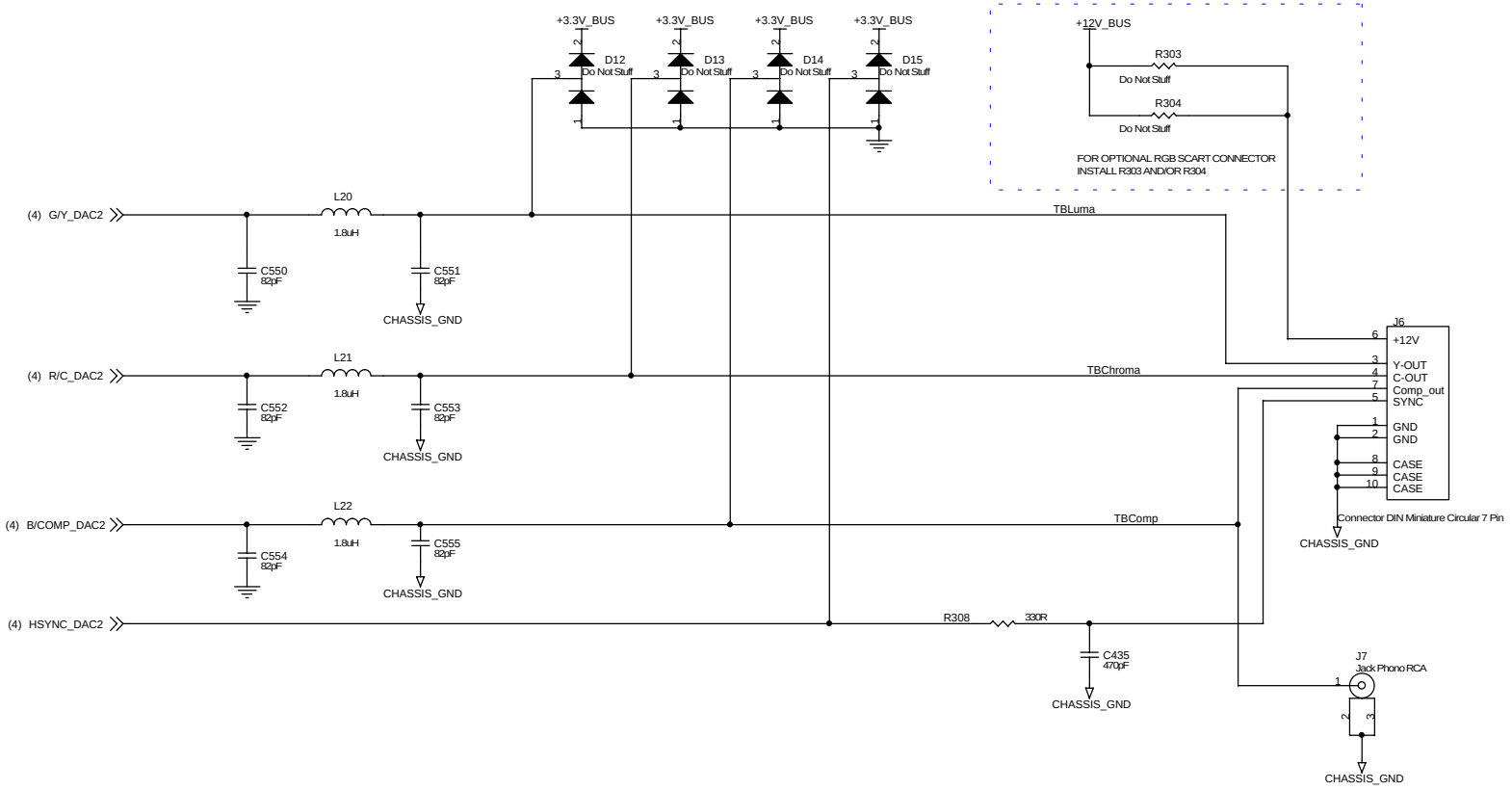
TV-OUT



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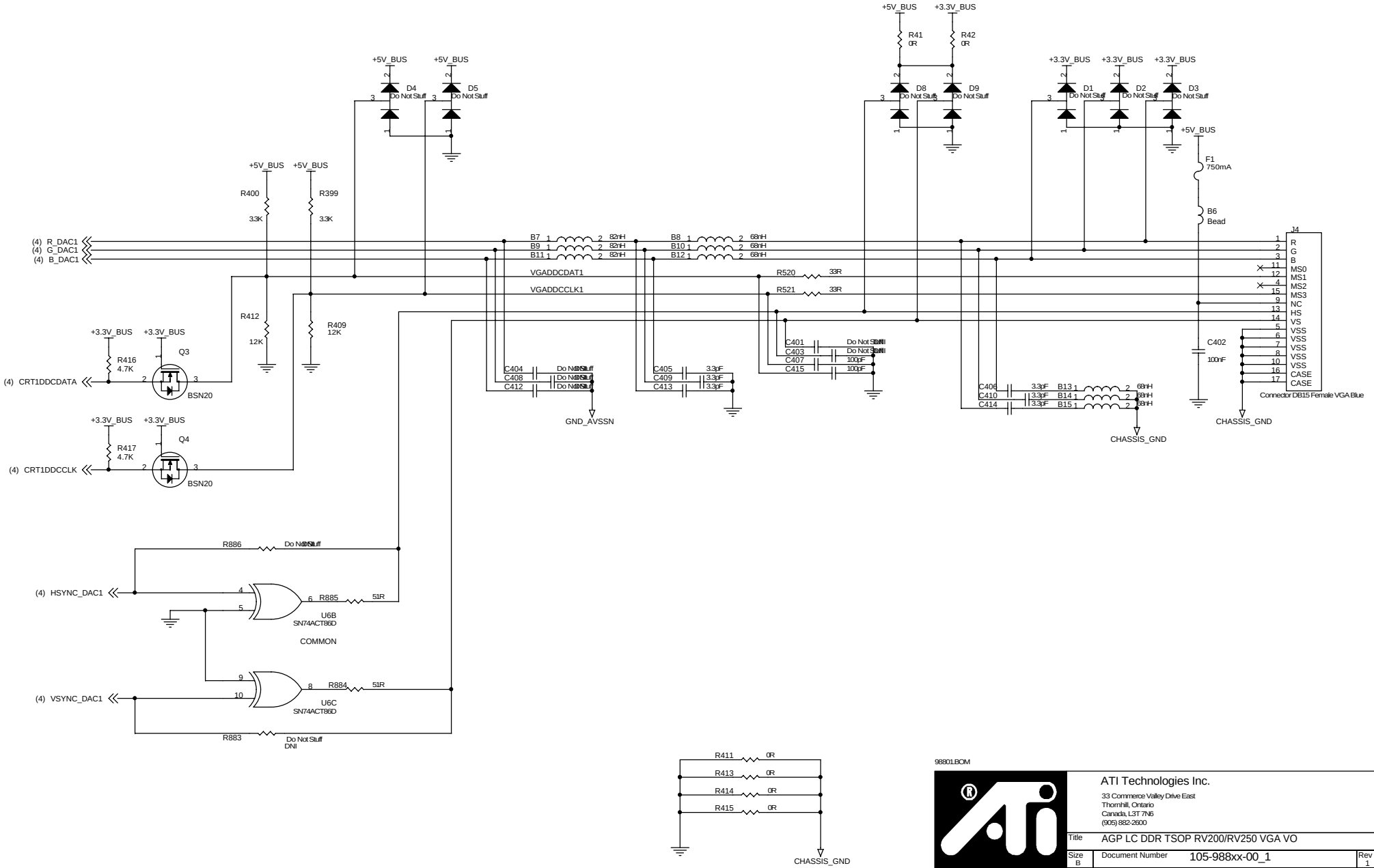
CRT INTERFACE



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CRT SCREWS

ASSY2

SCREW
JACKSCREW

ASSY3

SCREW
JACKSCREW

BRACKET SCREWS

REF1

SCHEMATIC

105-988xx-00

REF2

PCB

109-988xx-00

MISC. BOARD PARTS

ASSY1

BLANK
LABEL

1.50W X 0.50H

ASSY8

ANTISTATIC
BAG

6 X 11

H1

HEATSINK

ASSY4

BRACKET

VID OUT, VGA, 297

ASSY6

BRACKET

VGA, 305

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REVISION HISTORY

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	A	04/04/02	PROTOTYPE I.i TSOP MEMORY VERSION.
1	00	06/10/02	1.) ADD MEM_STRAP2 STRAP 2.) ADD R229 PULUP STRAP FOR MULT FUNCTION AND DIP SWICHER 3.) ADD PAL/ NTSC SELECT DIP SWITCHER PRODUCTION RELEASE