PG611 A00

12GB GDDR5X, 384b, 256Mx32
TALL DVI-D + DP + DP + HDMI/DP + DP

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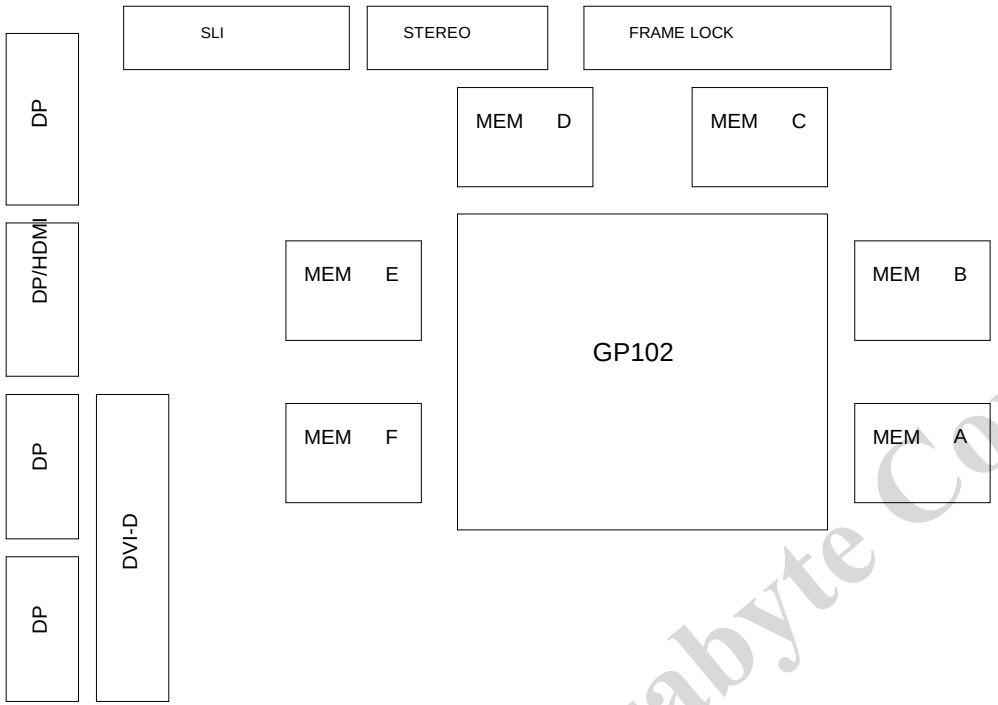

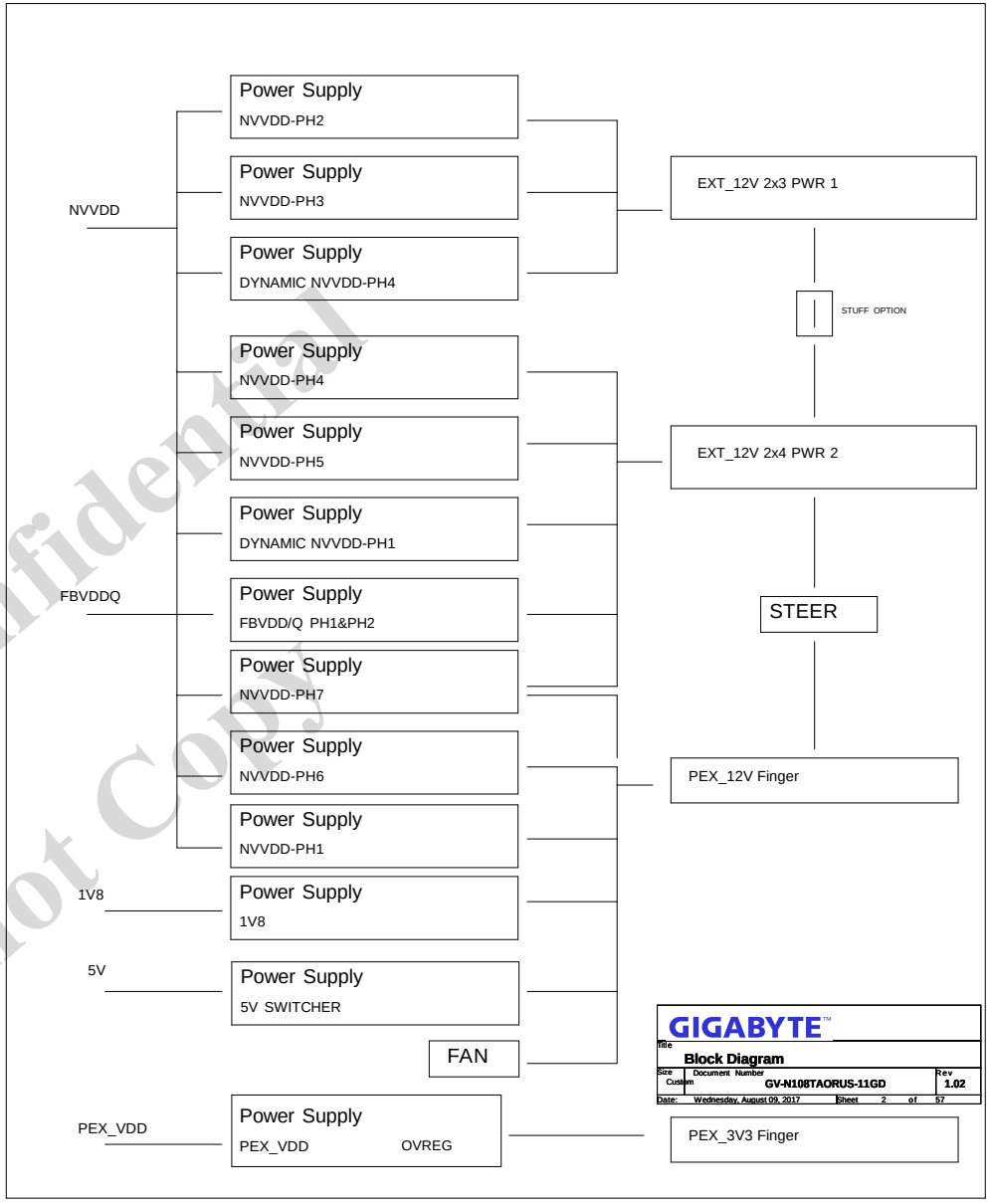

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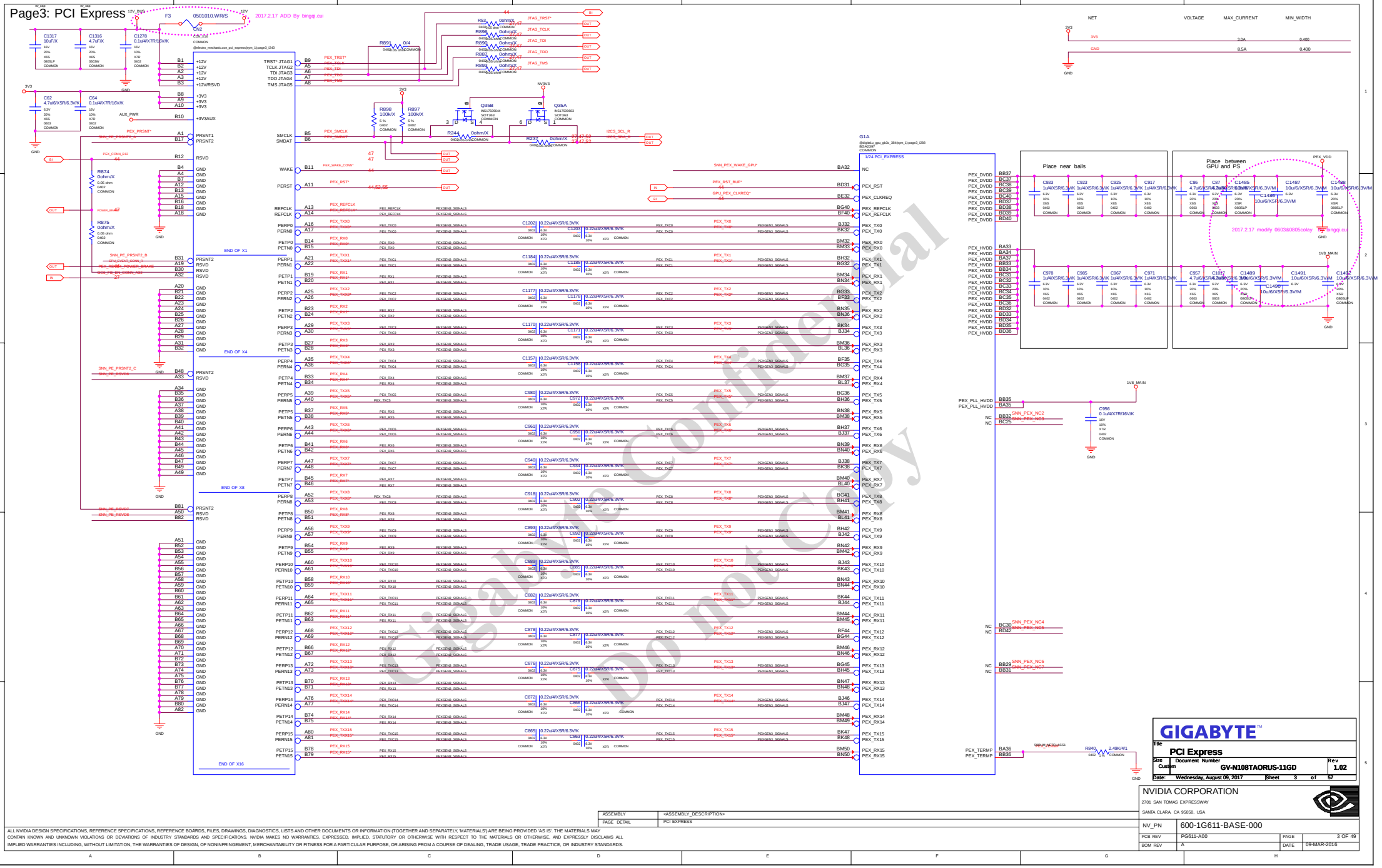

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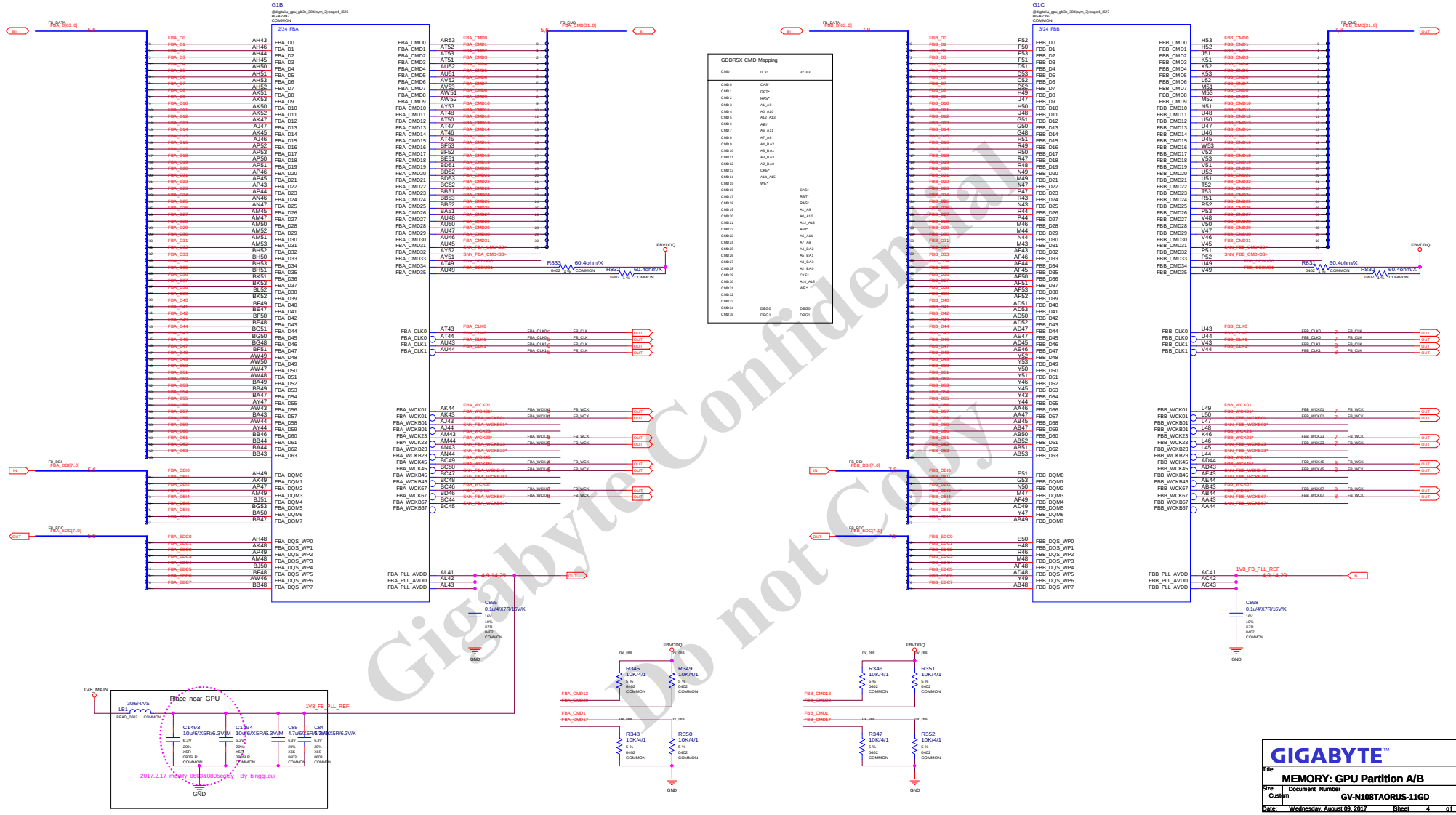

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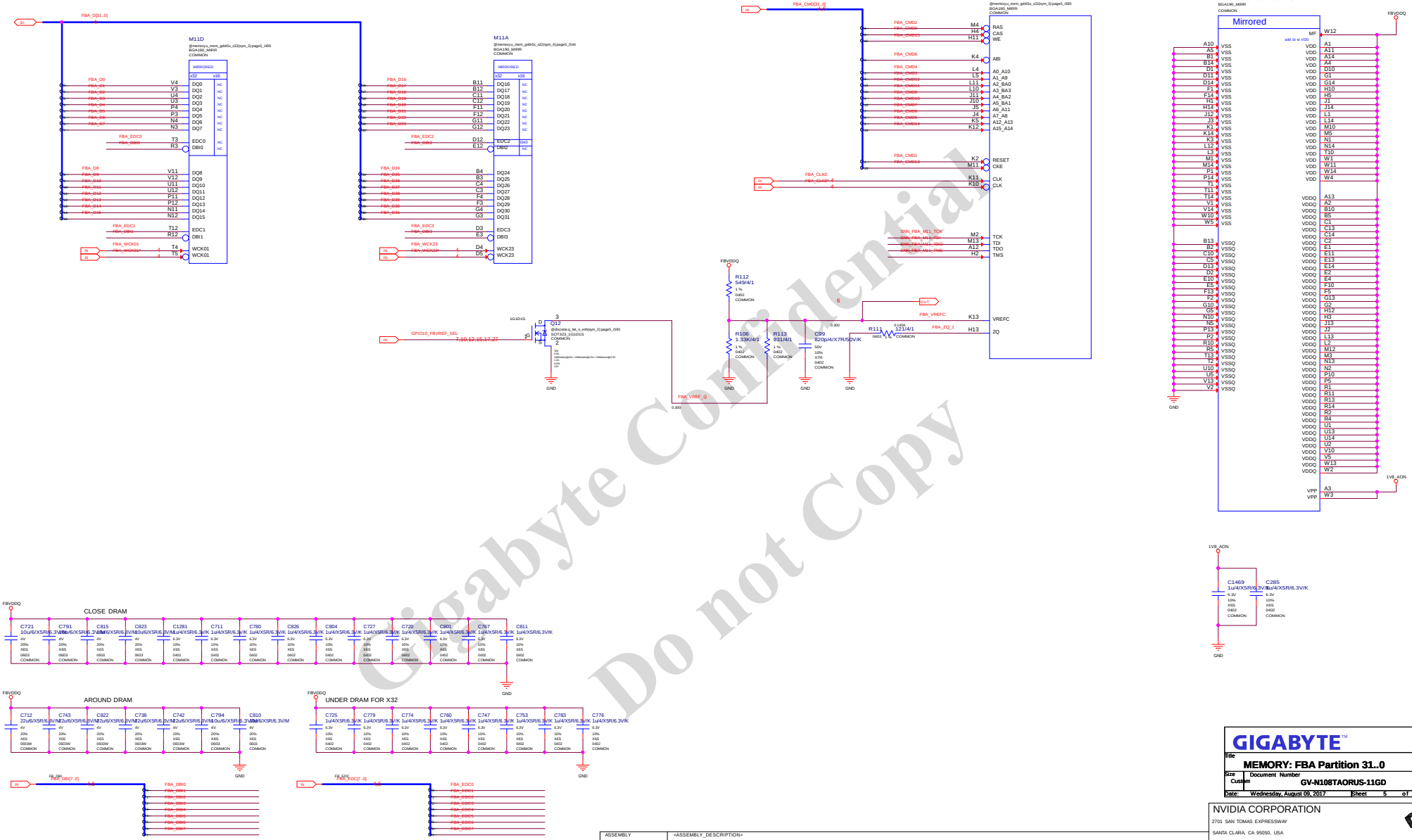

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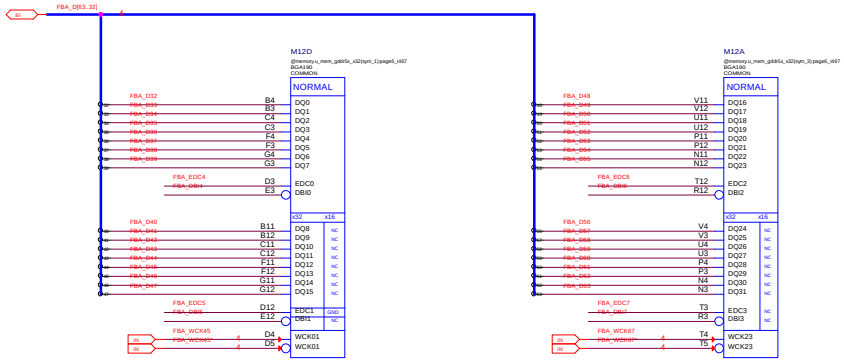

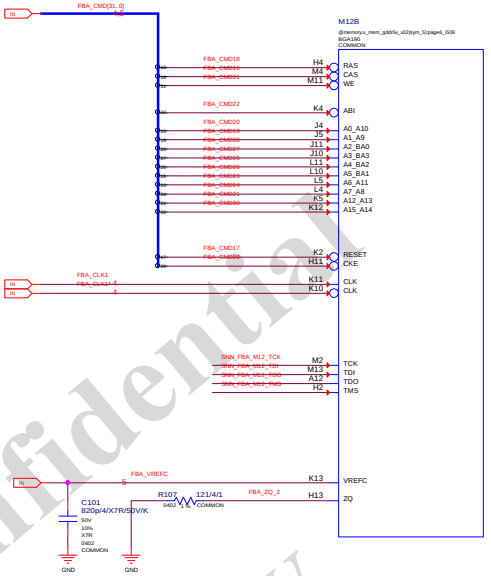

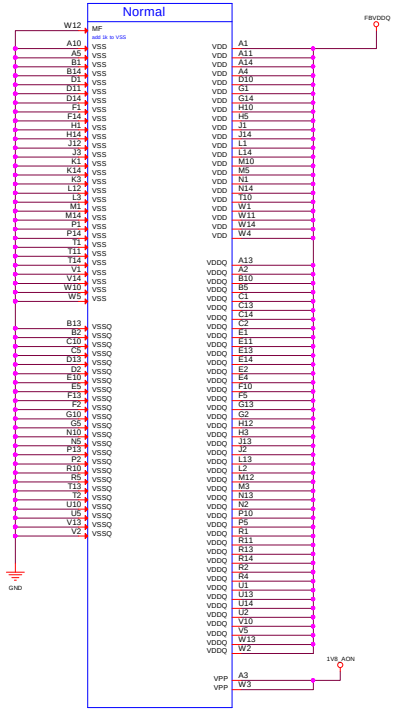

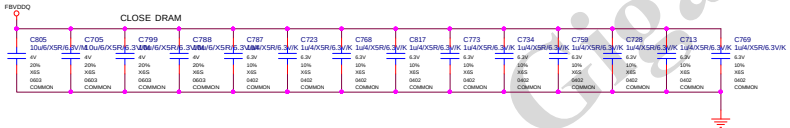

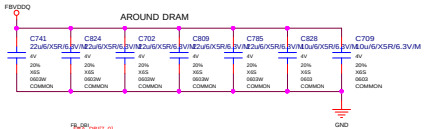

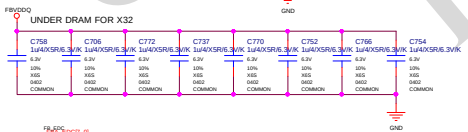

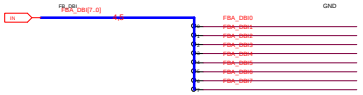

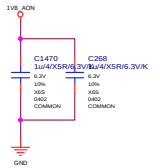

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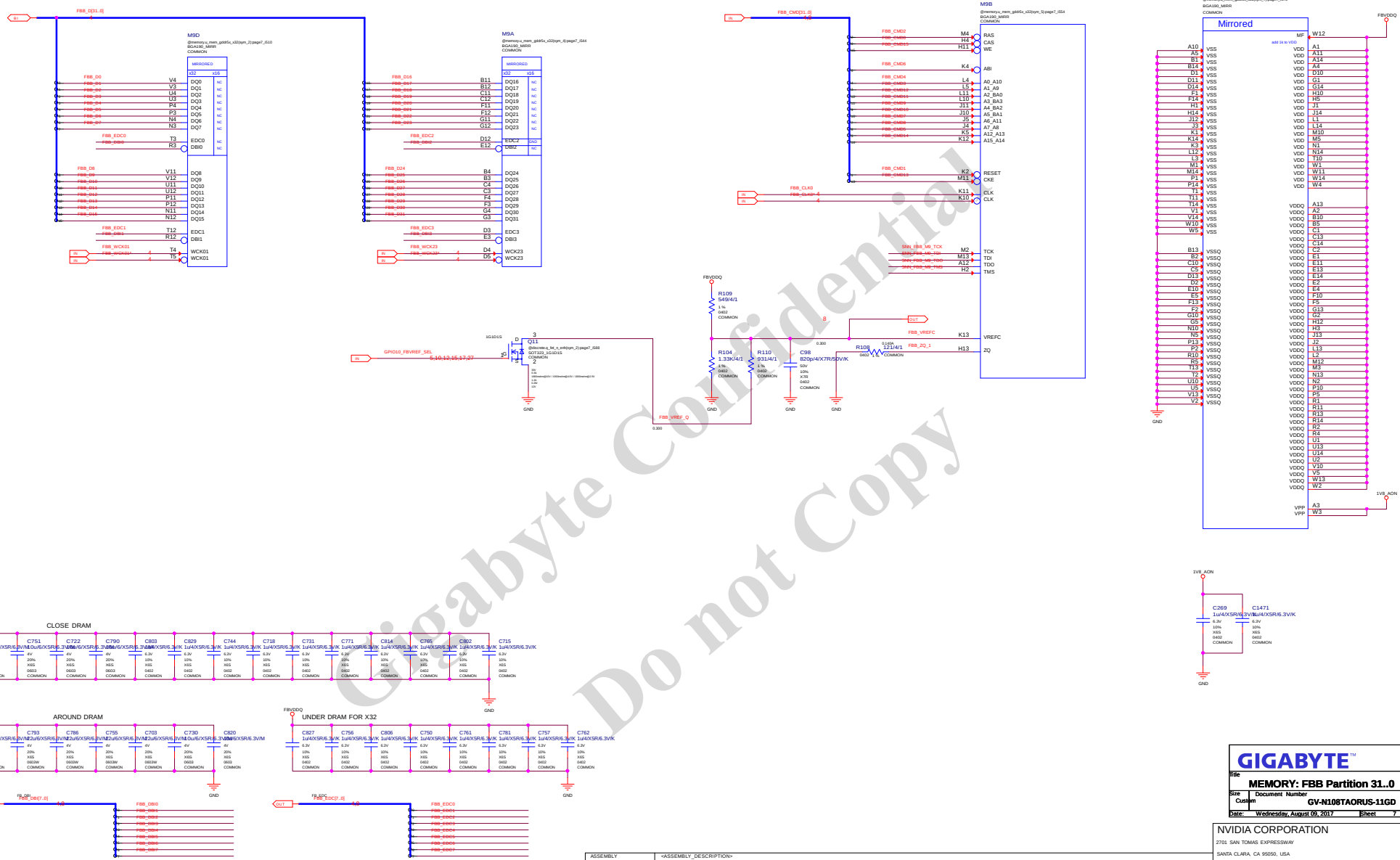

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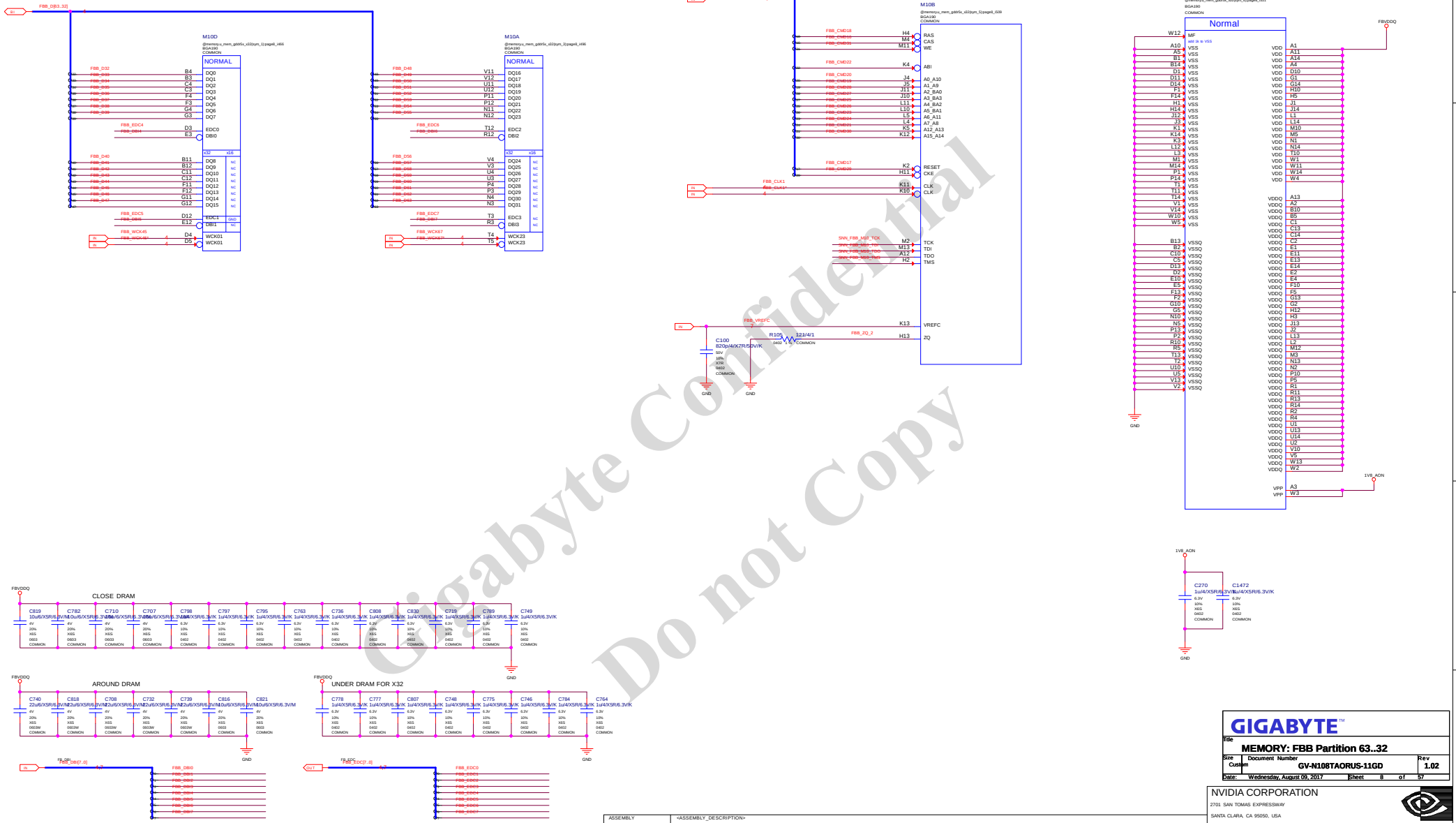

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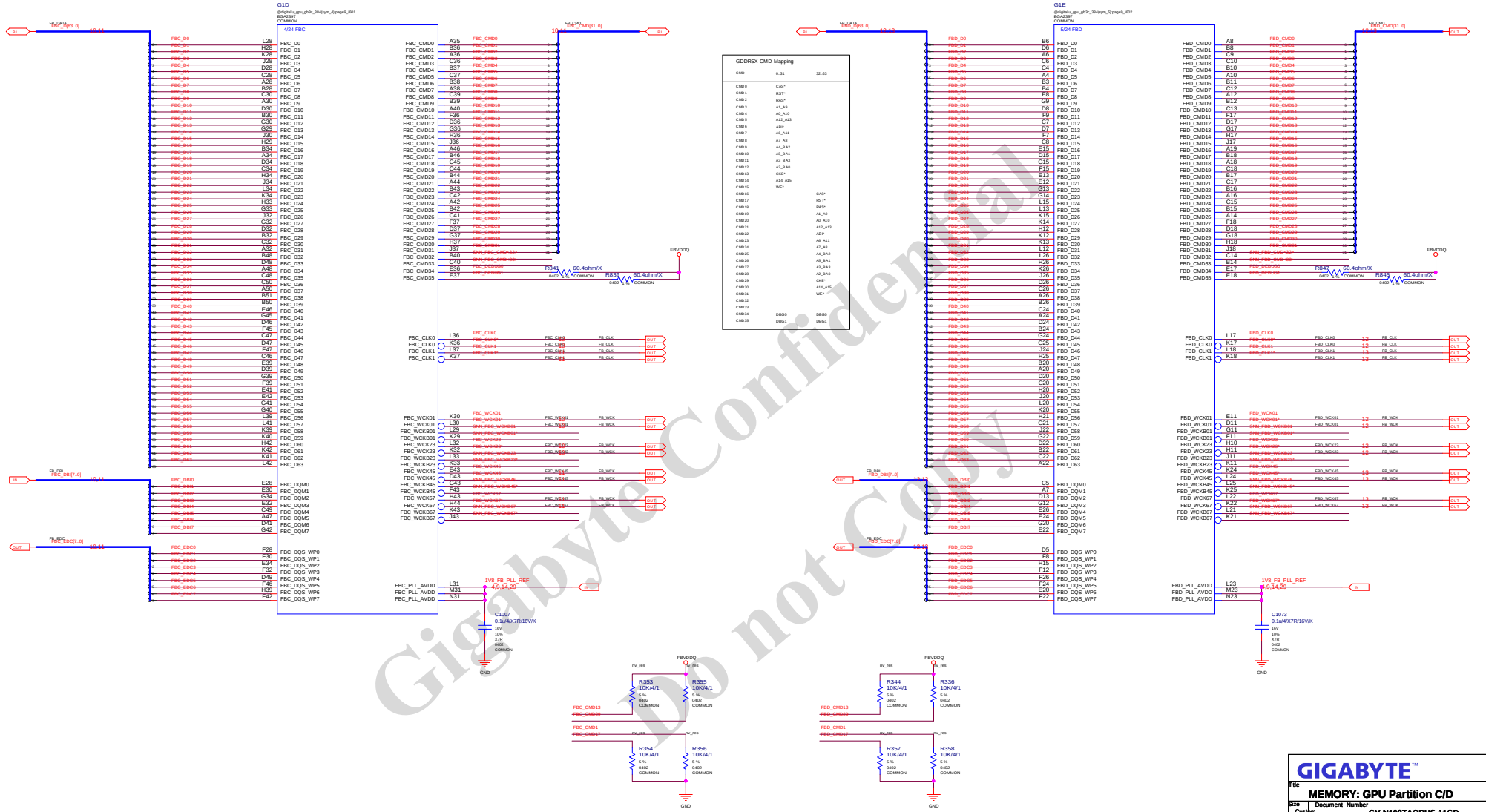

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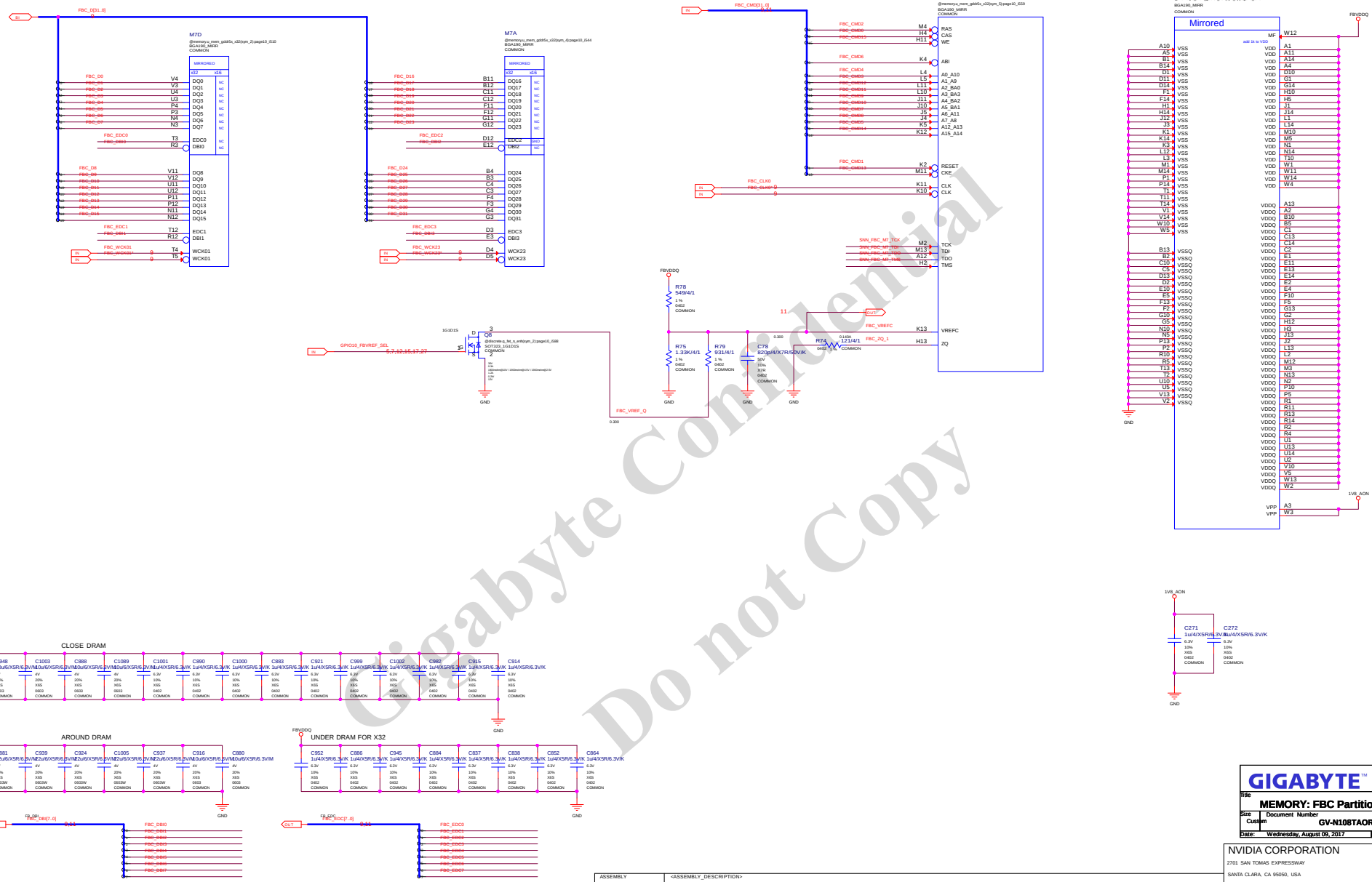

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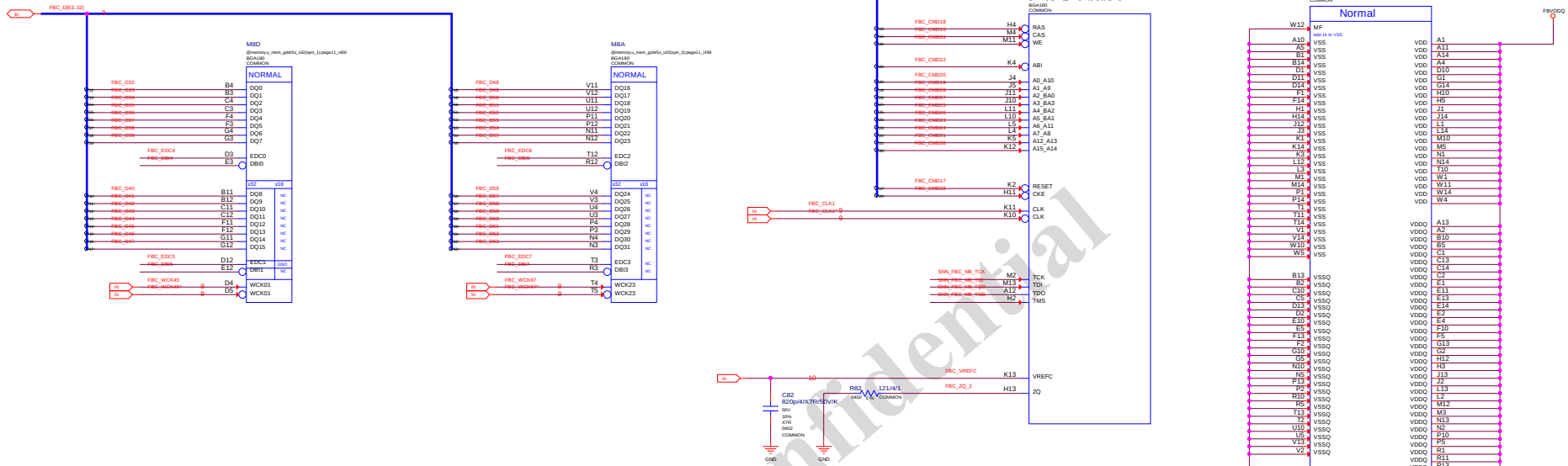

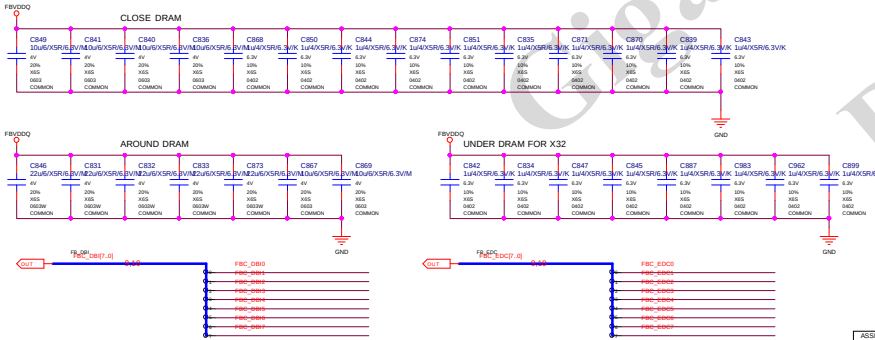

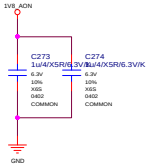

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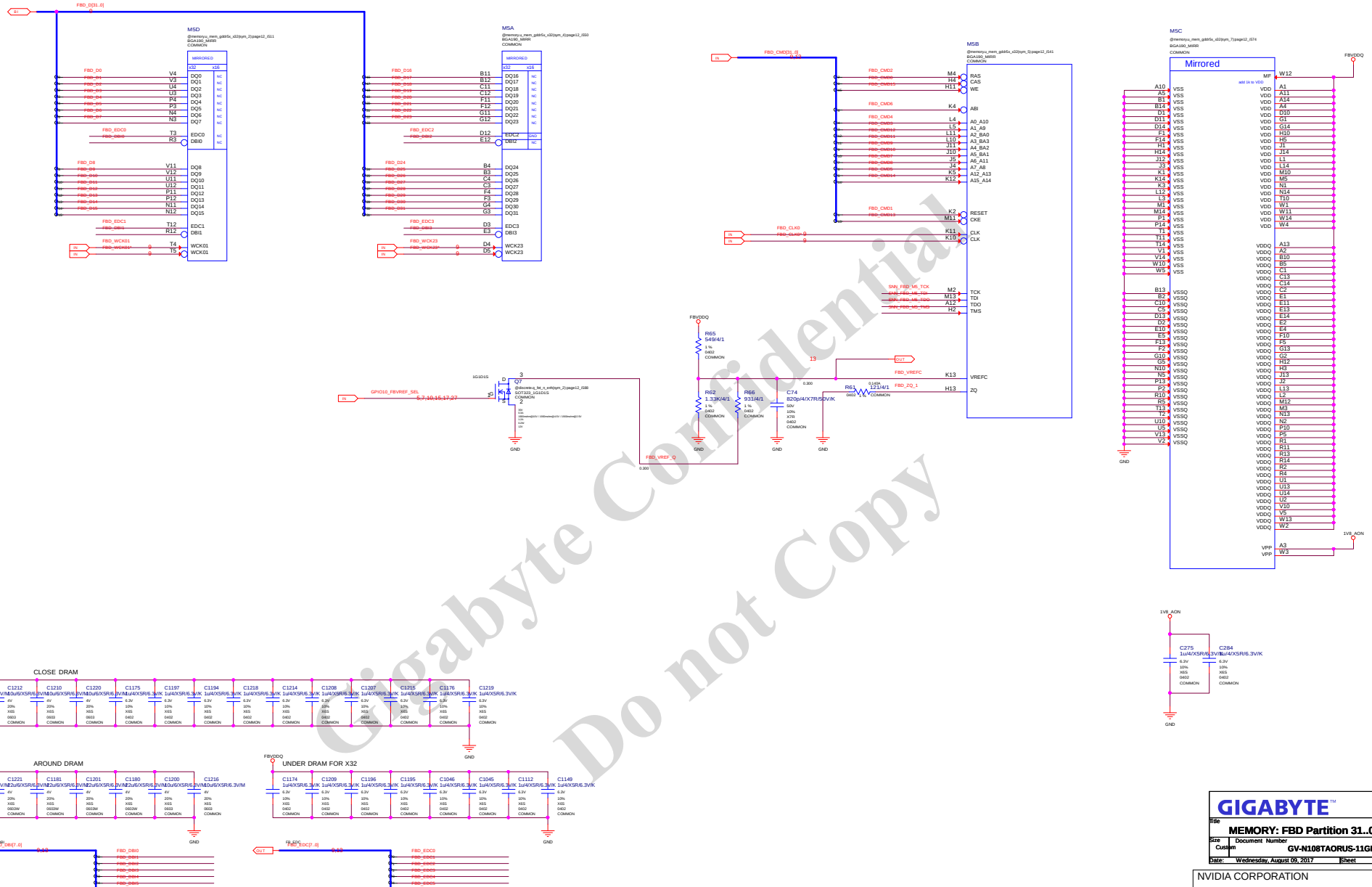

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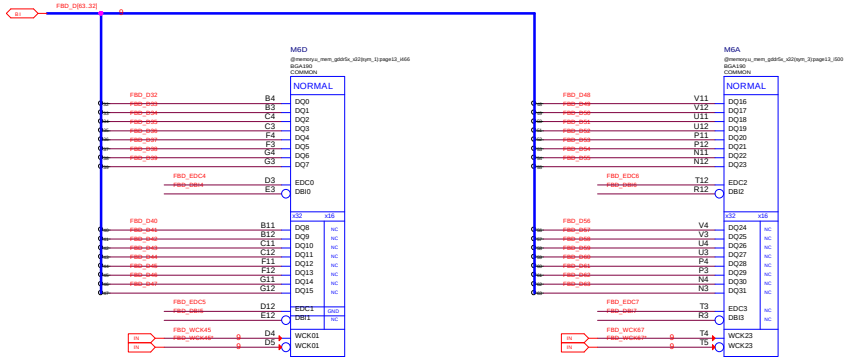

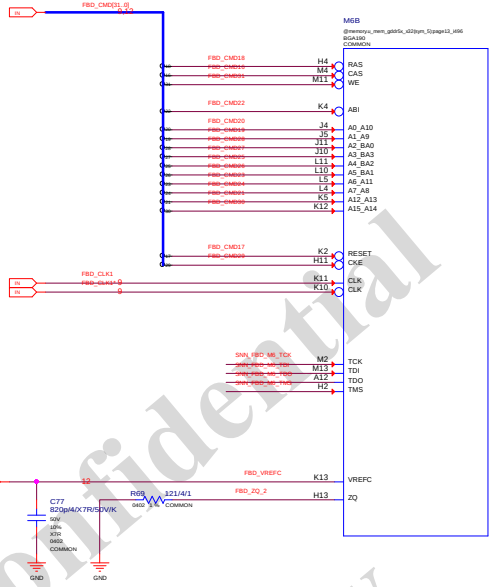

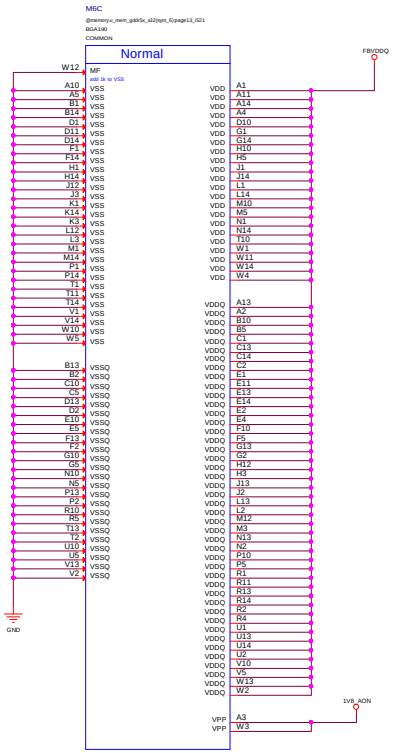

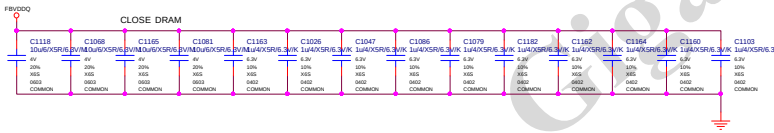

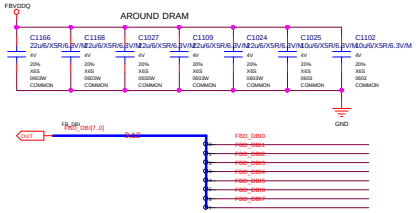

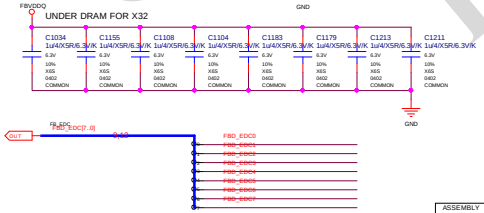

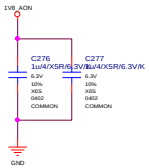

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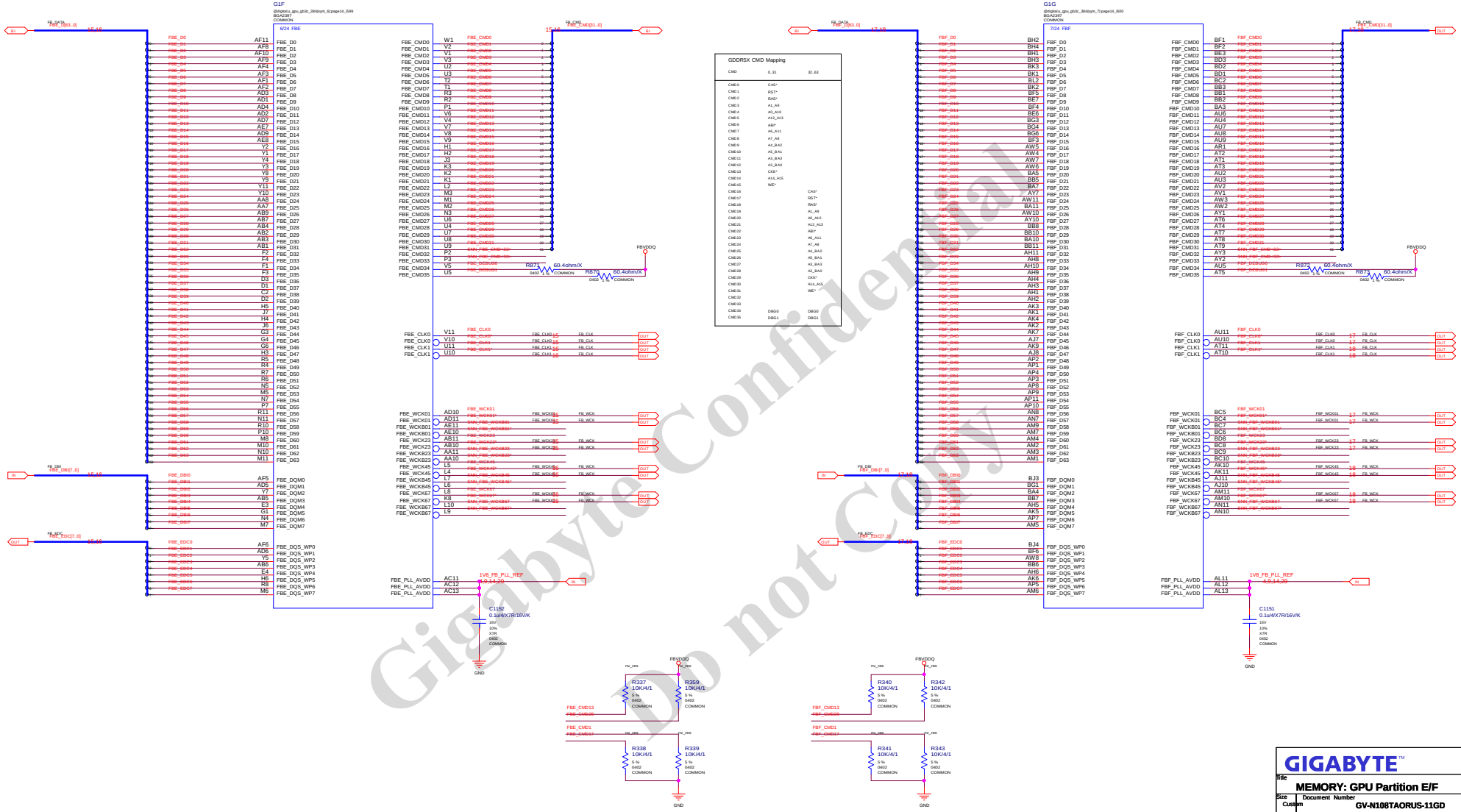

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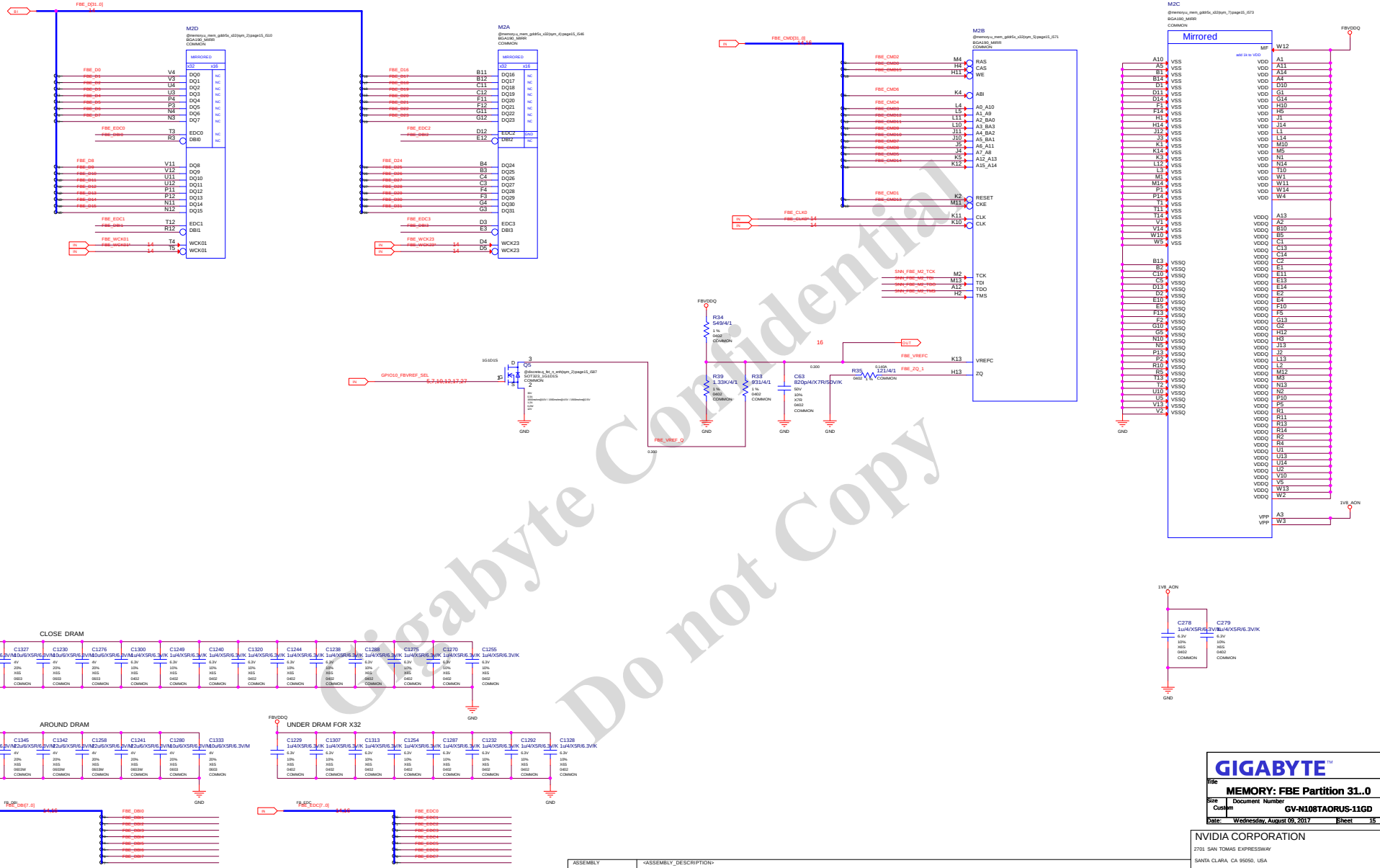

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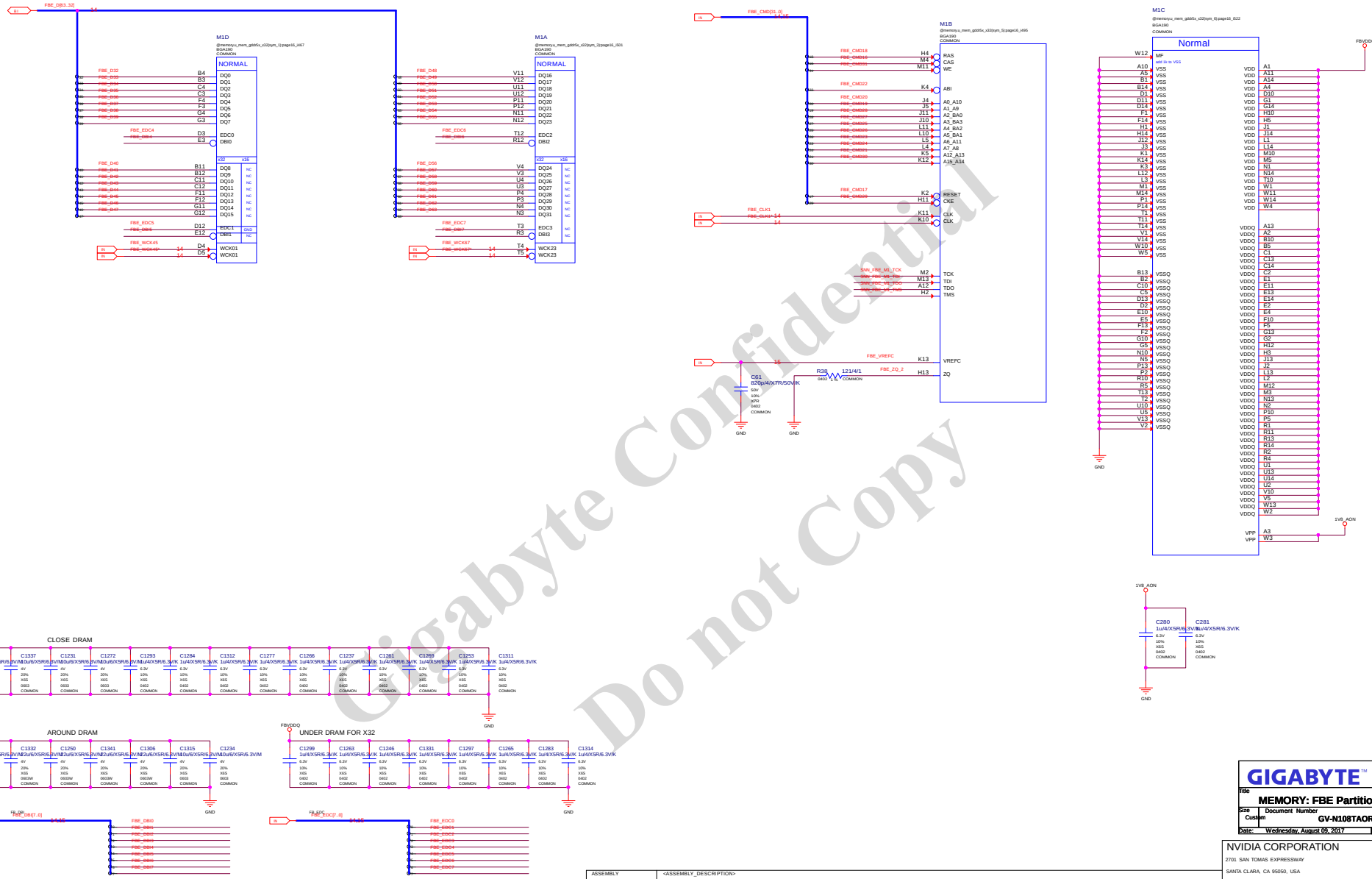

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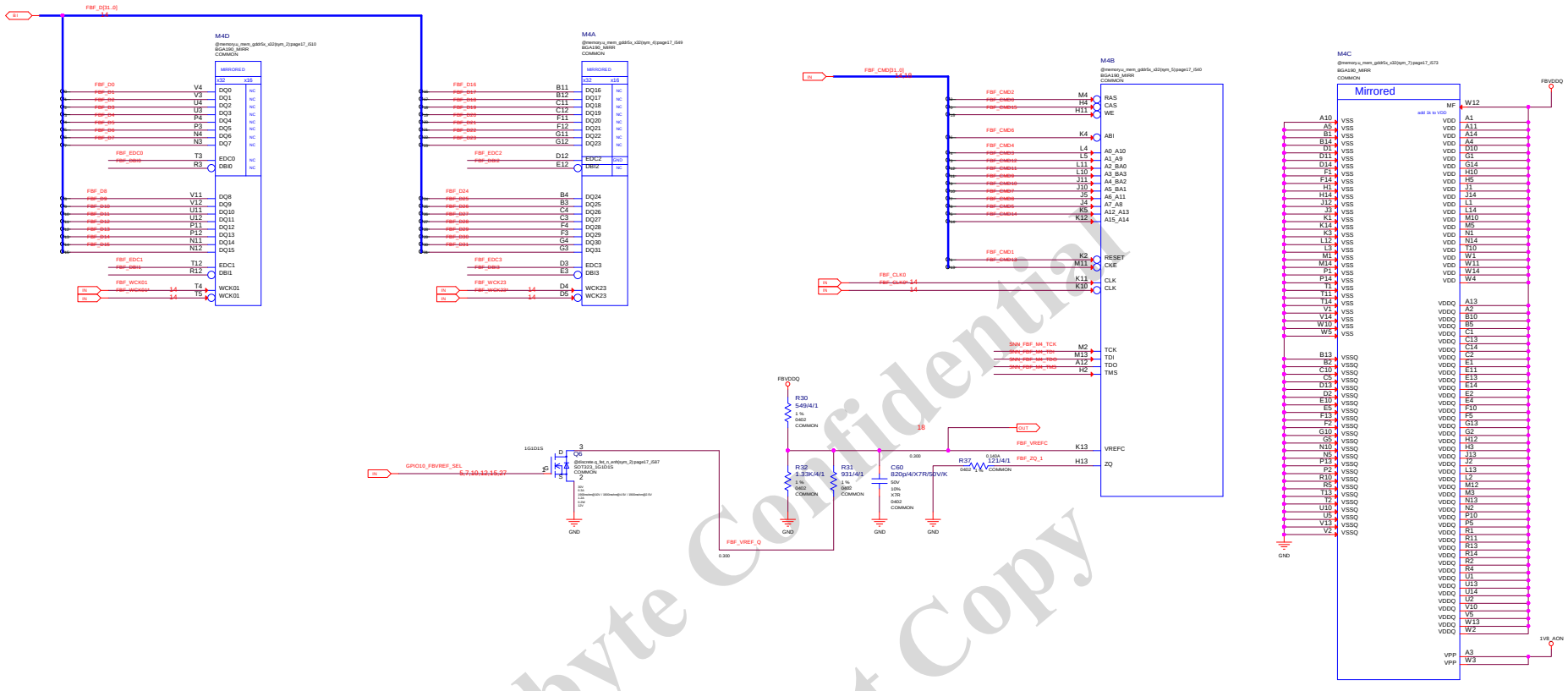

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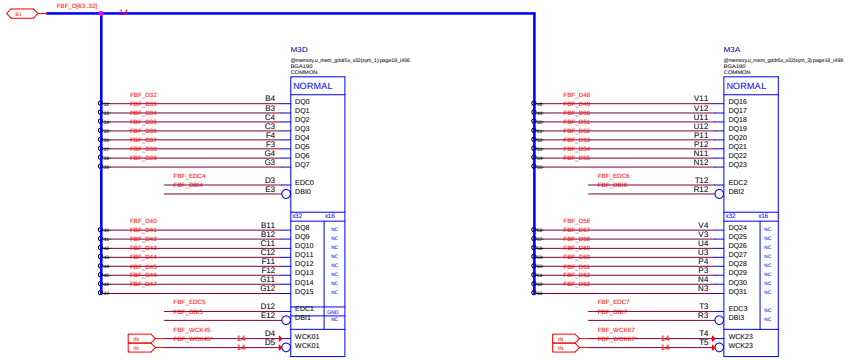

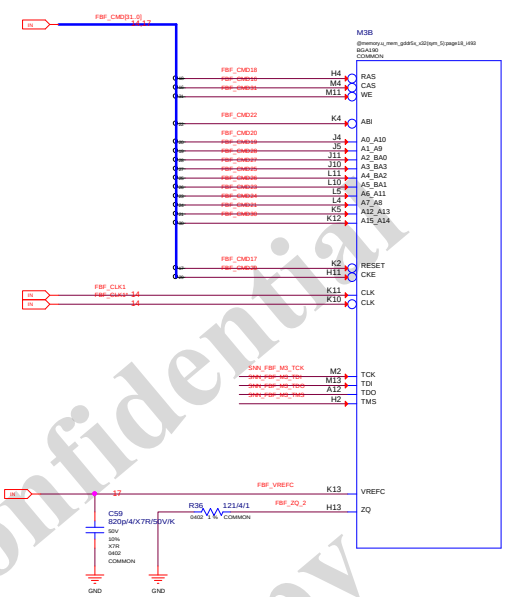

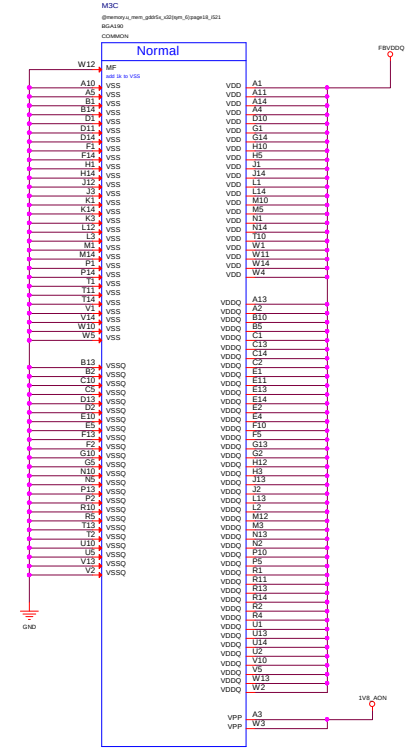

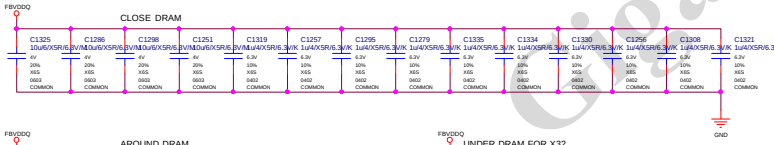

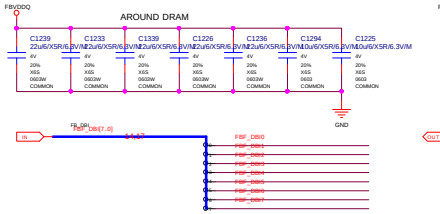

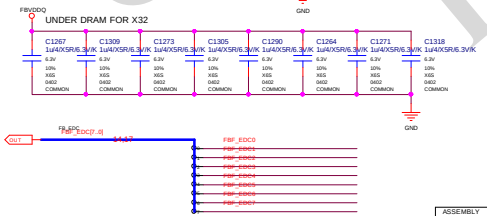

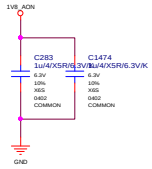

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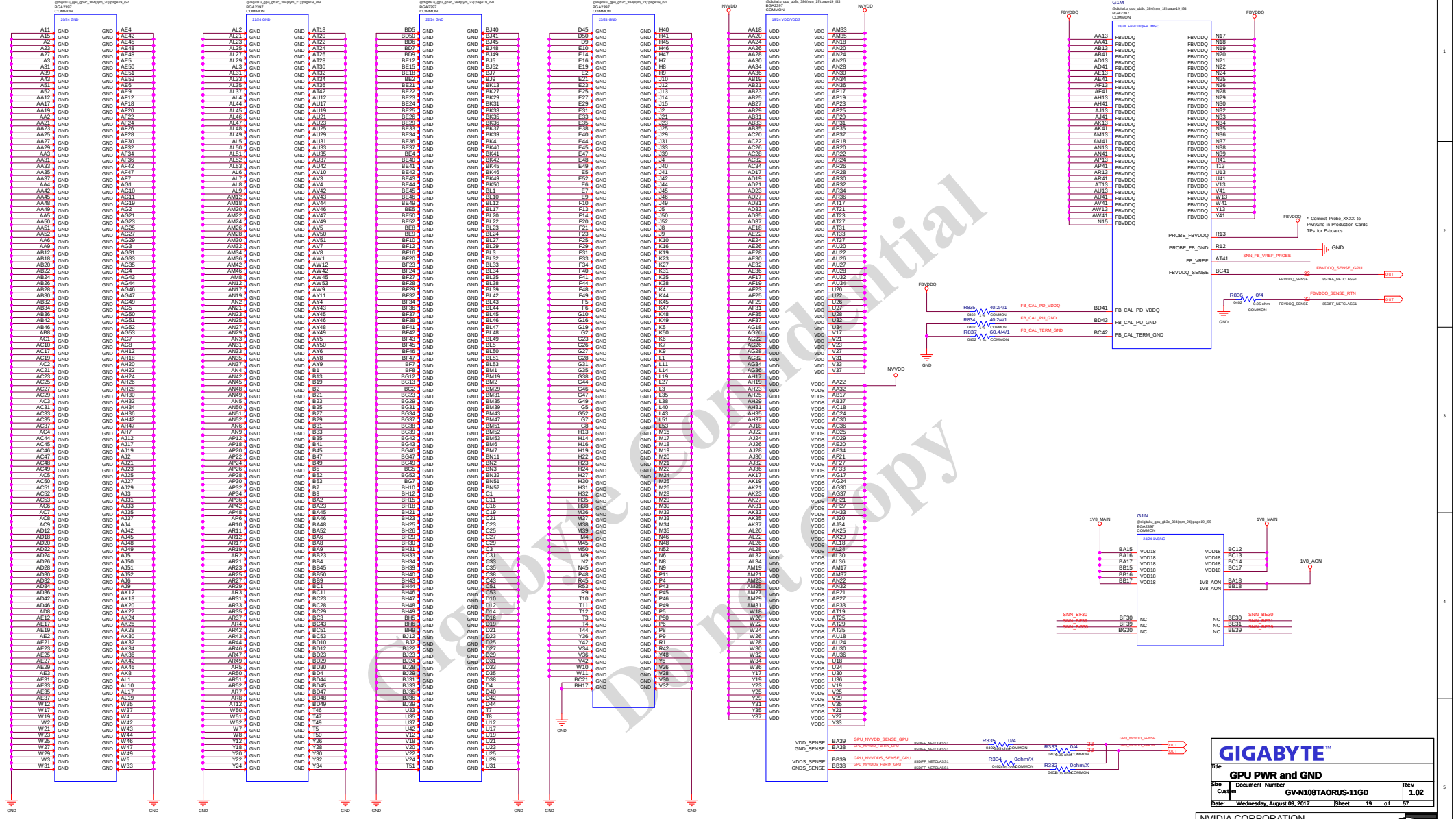
Page19: GPU PWR and GND



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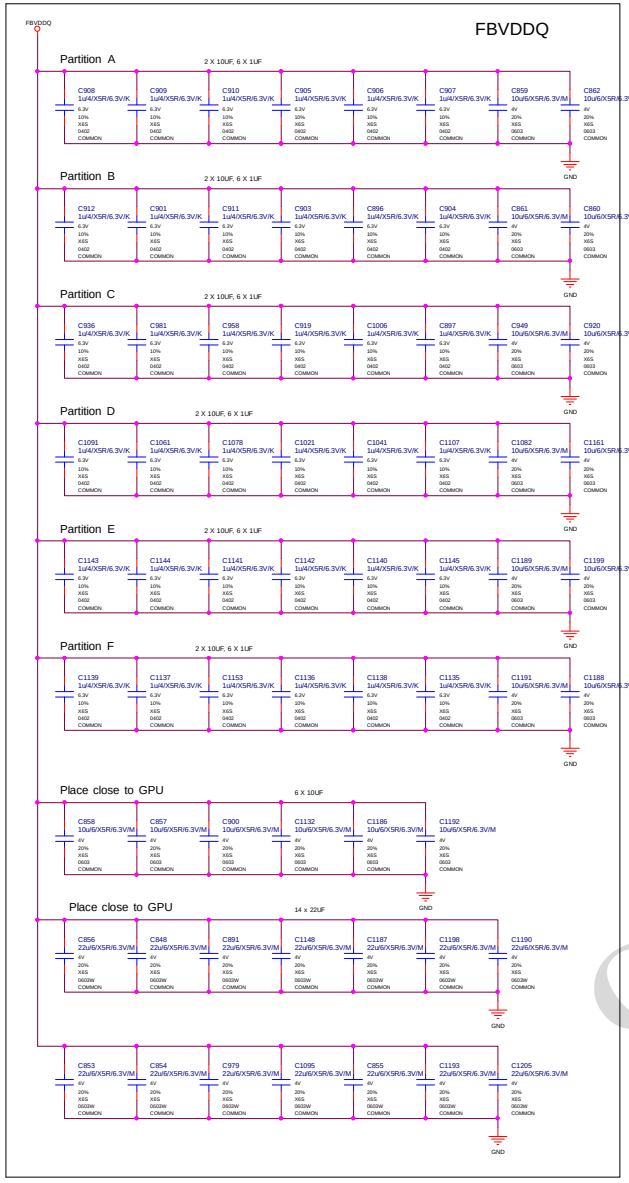
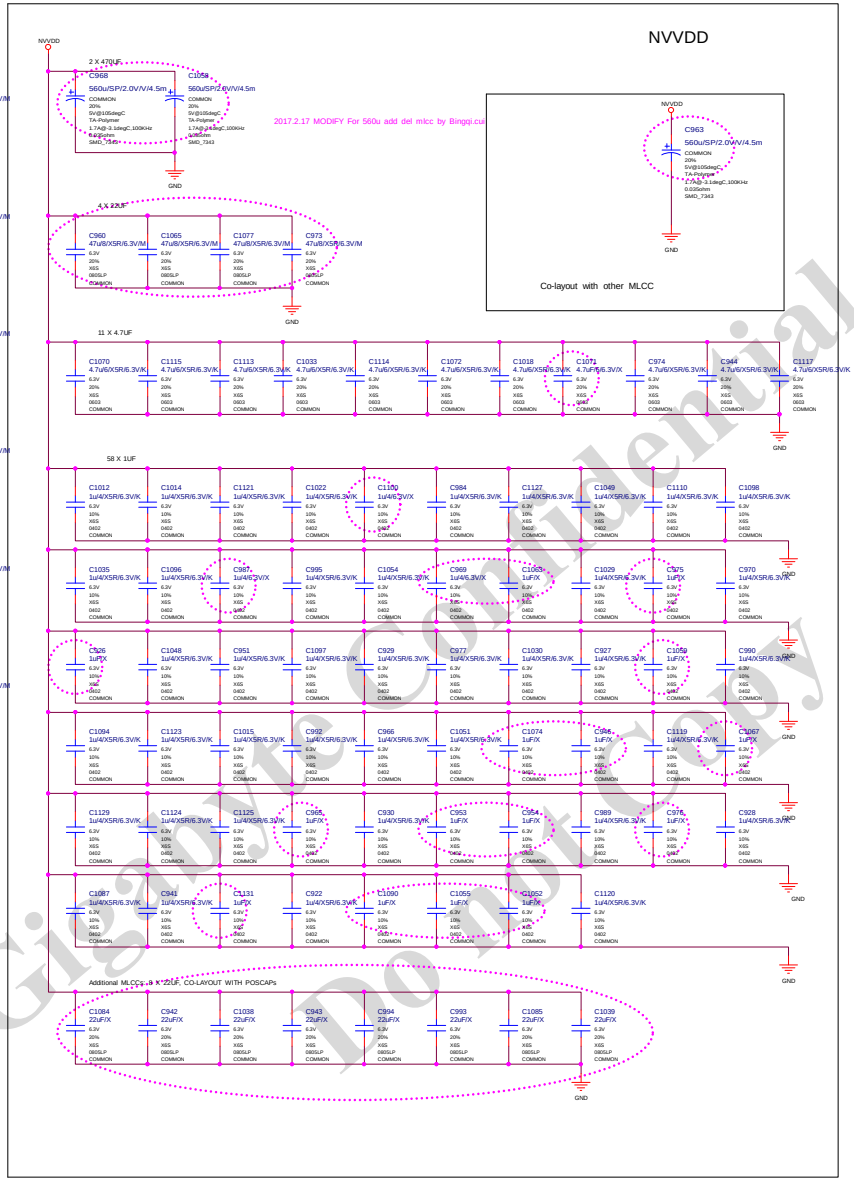
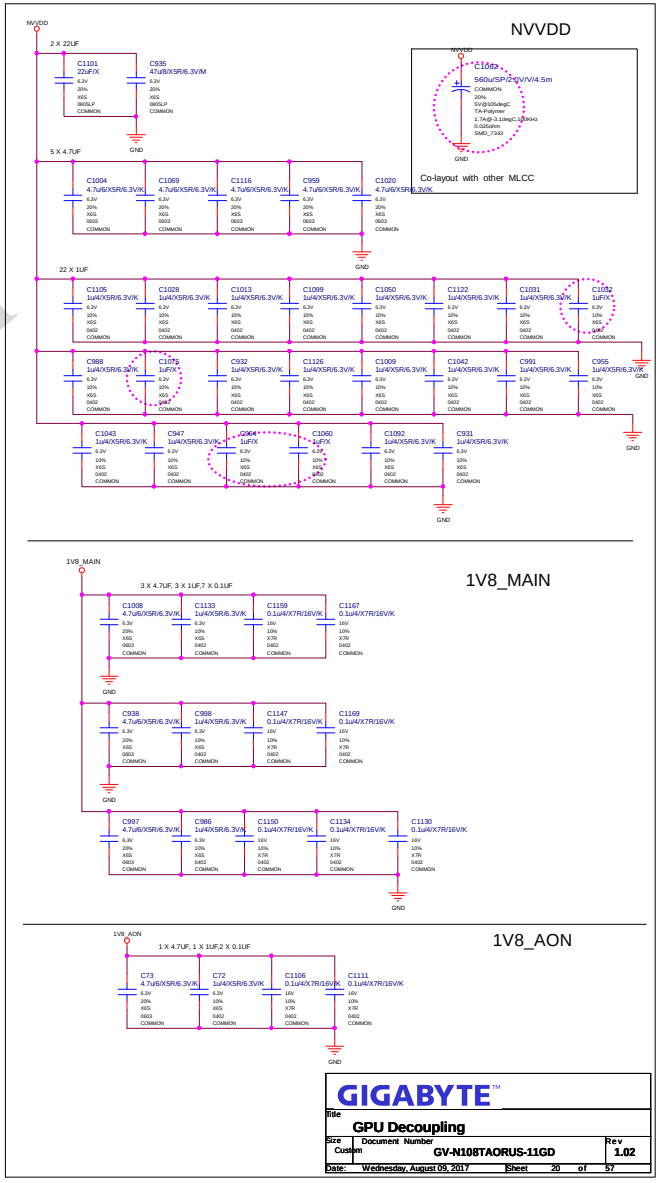
Page20: GPU Decoupling







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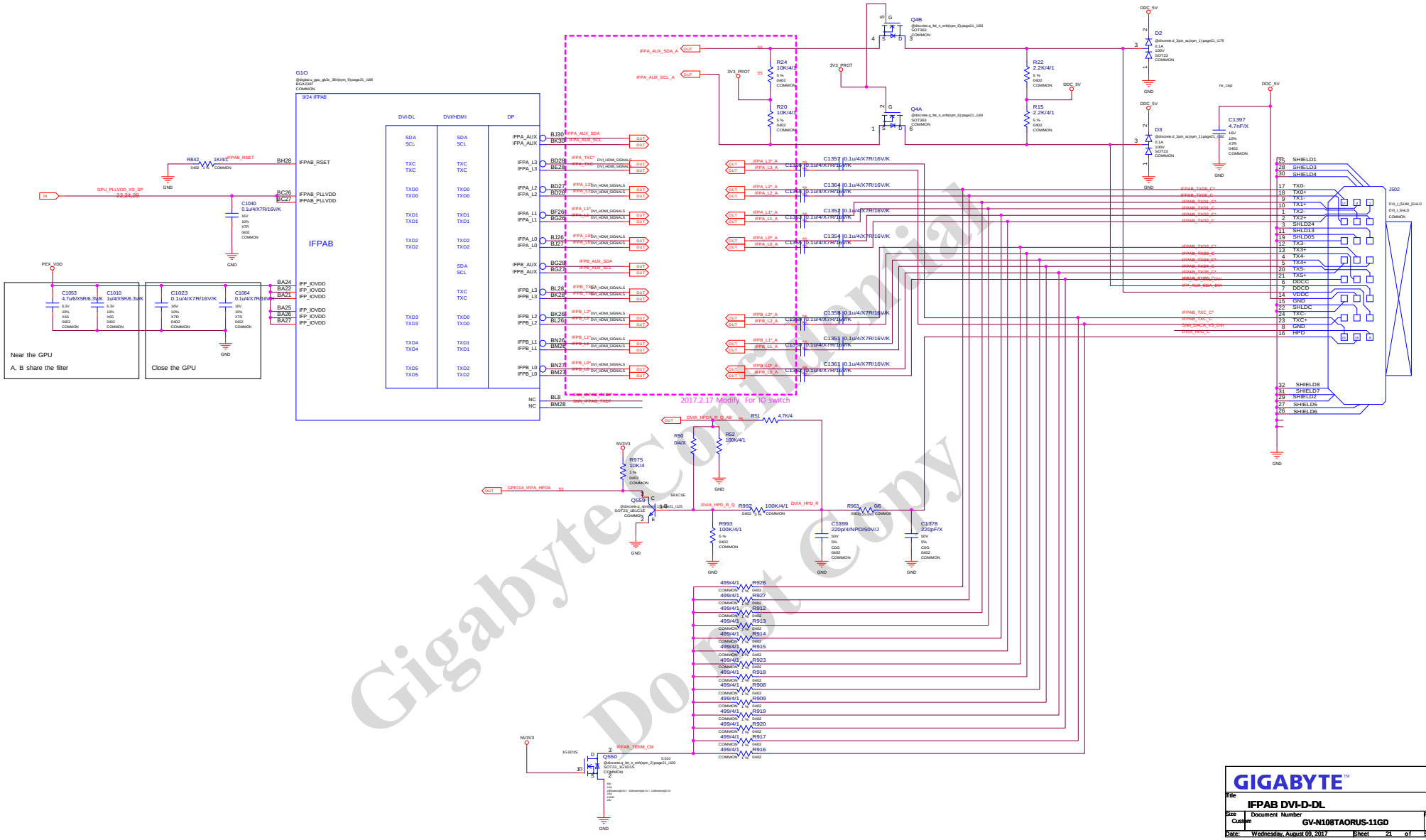

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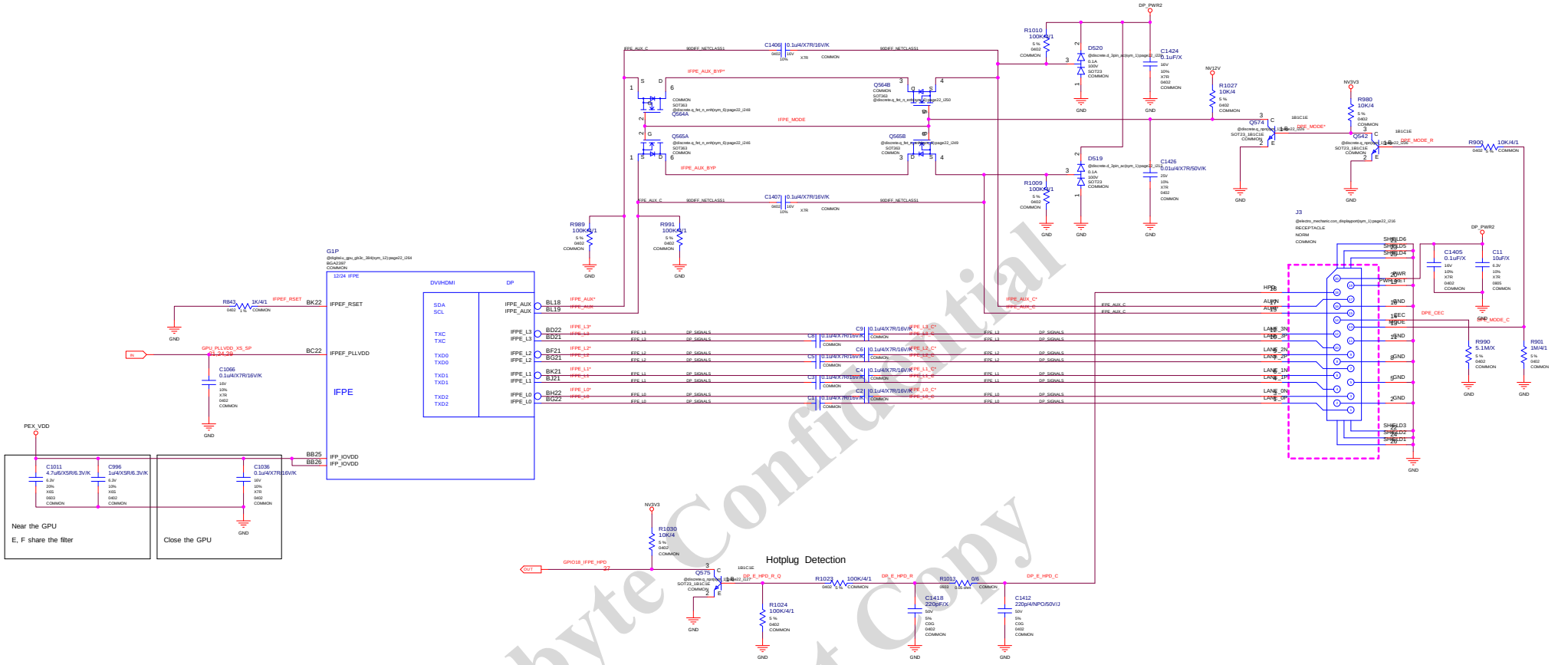

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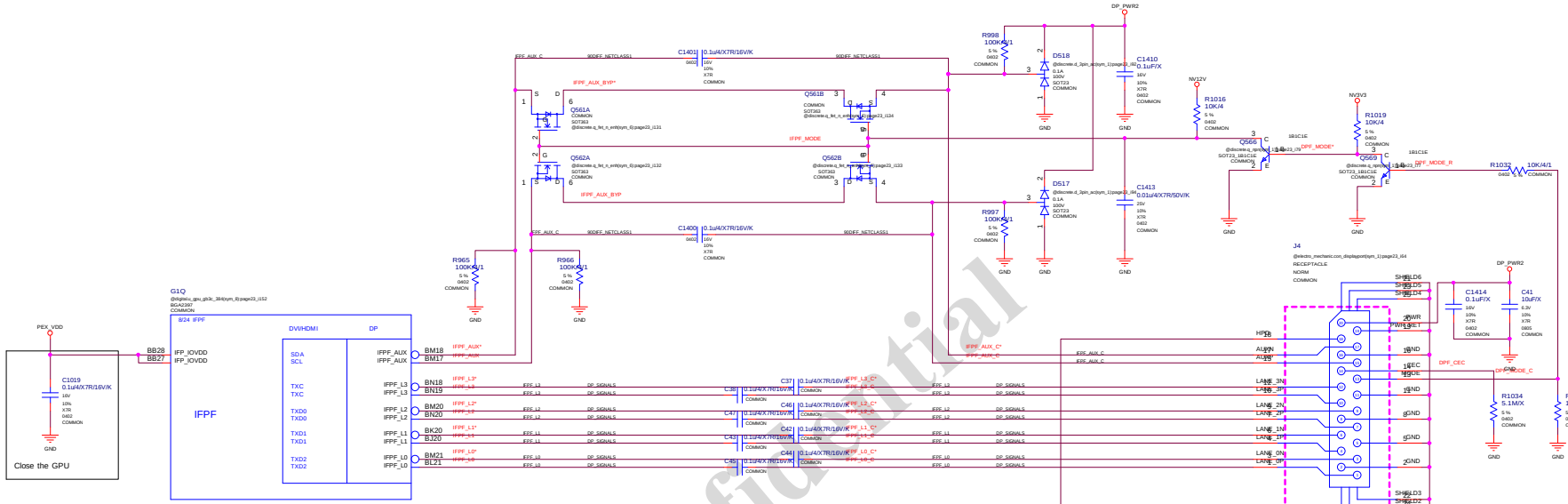

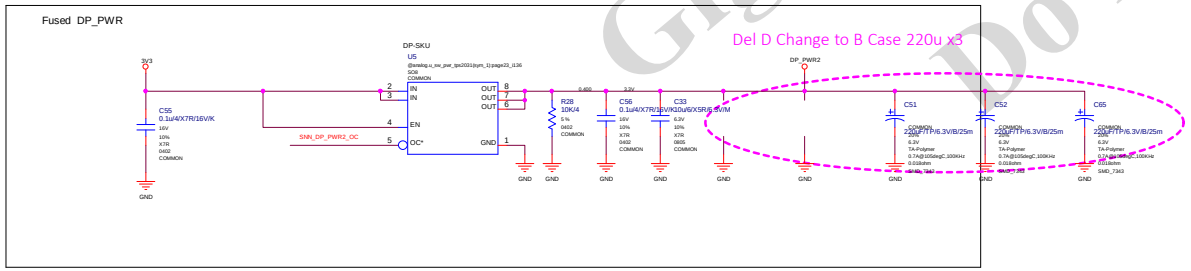

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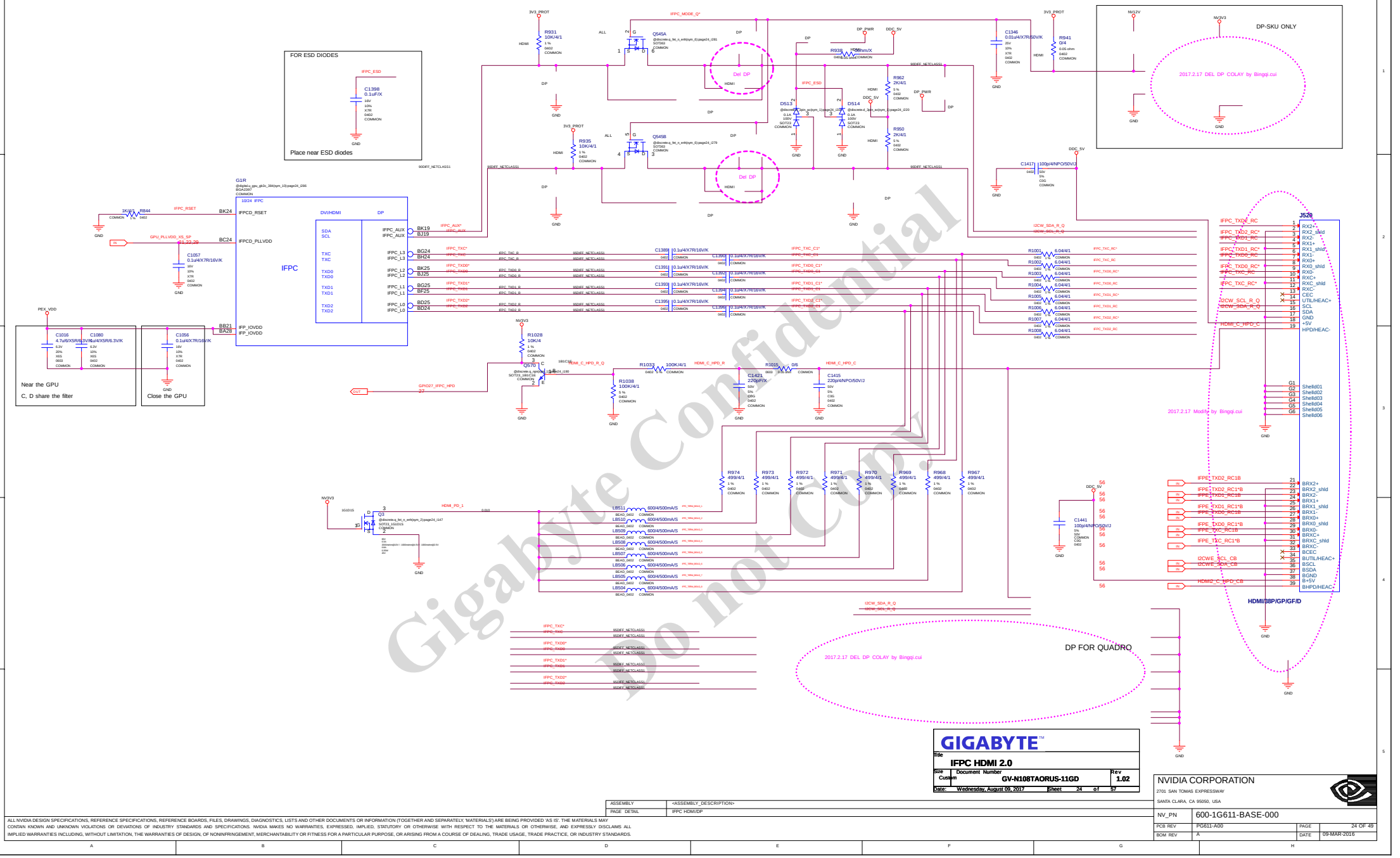
Page24: IFPC HDMI 2.0/DP



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PAGE_DETAIL	IFPC HDMI/DP

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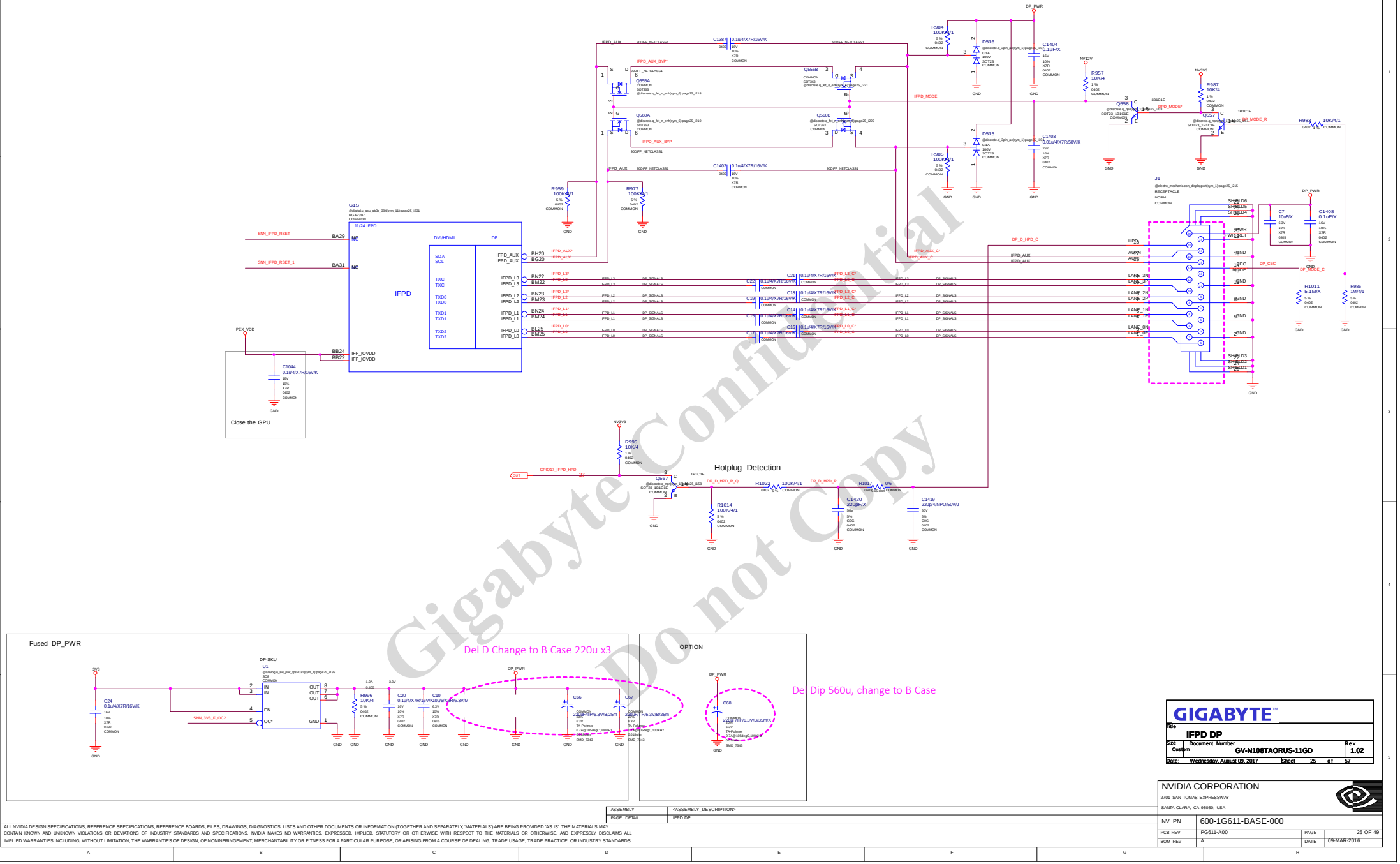

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPD DP

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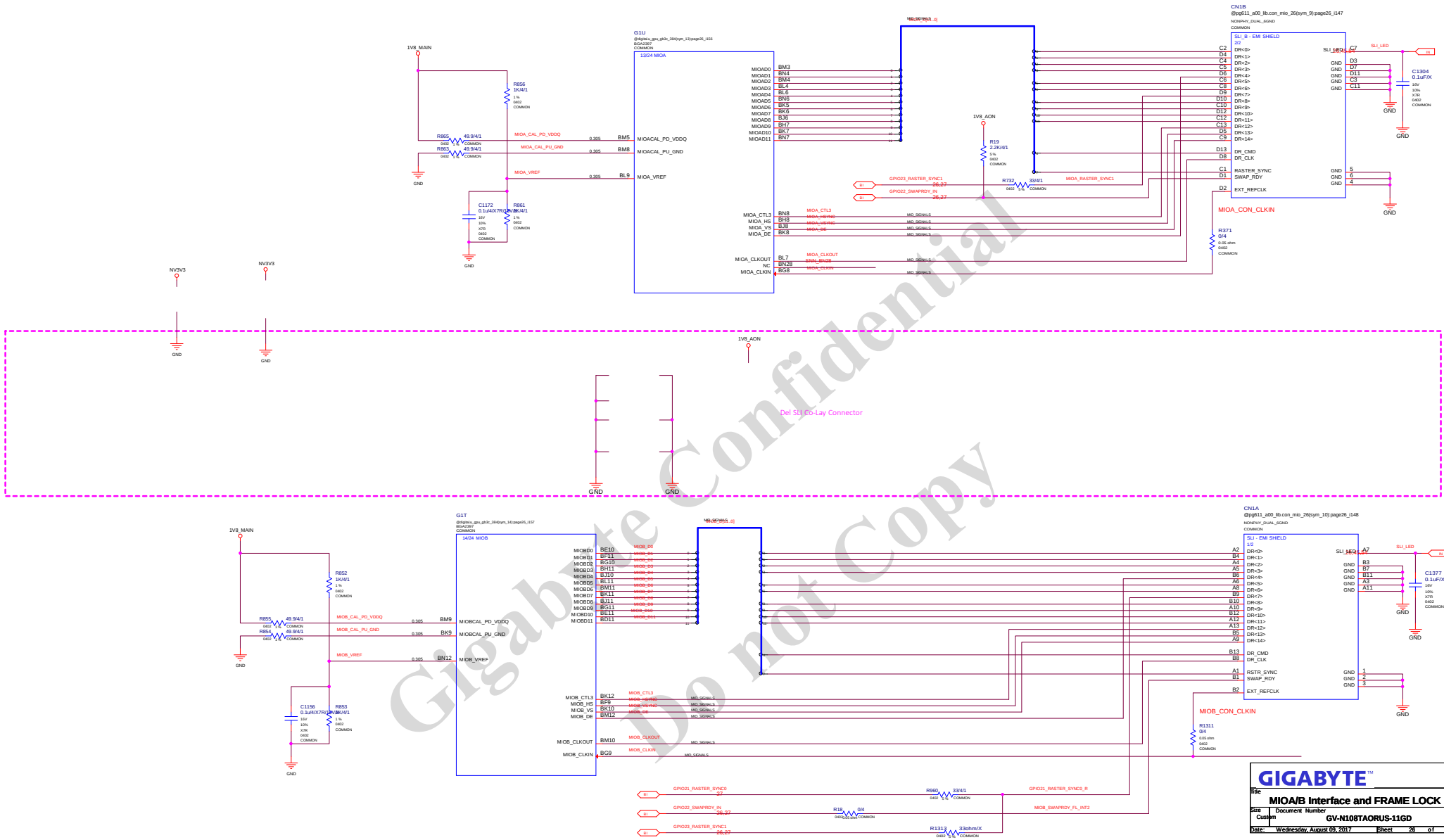
Page26: MIOA/B Interface and FRAME LOCK



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MIOA/B INTERFACE & FRAME LOCK

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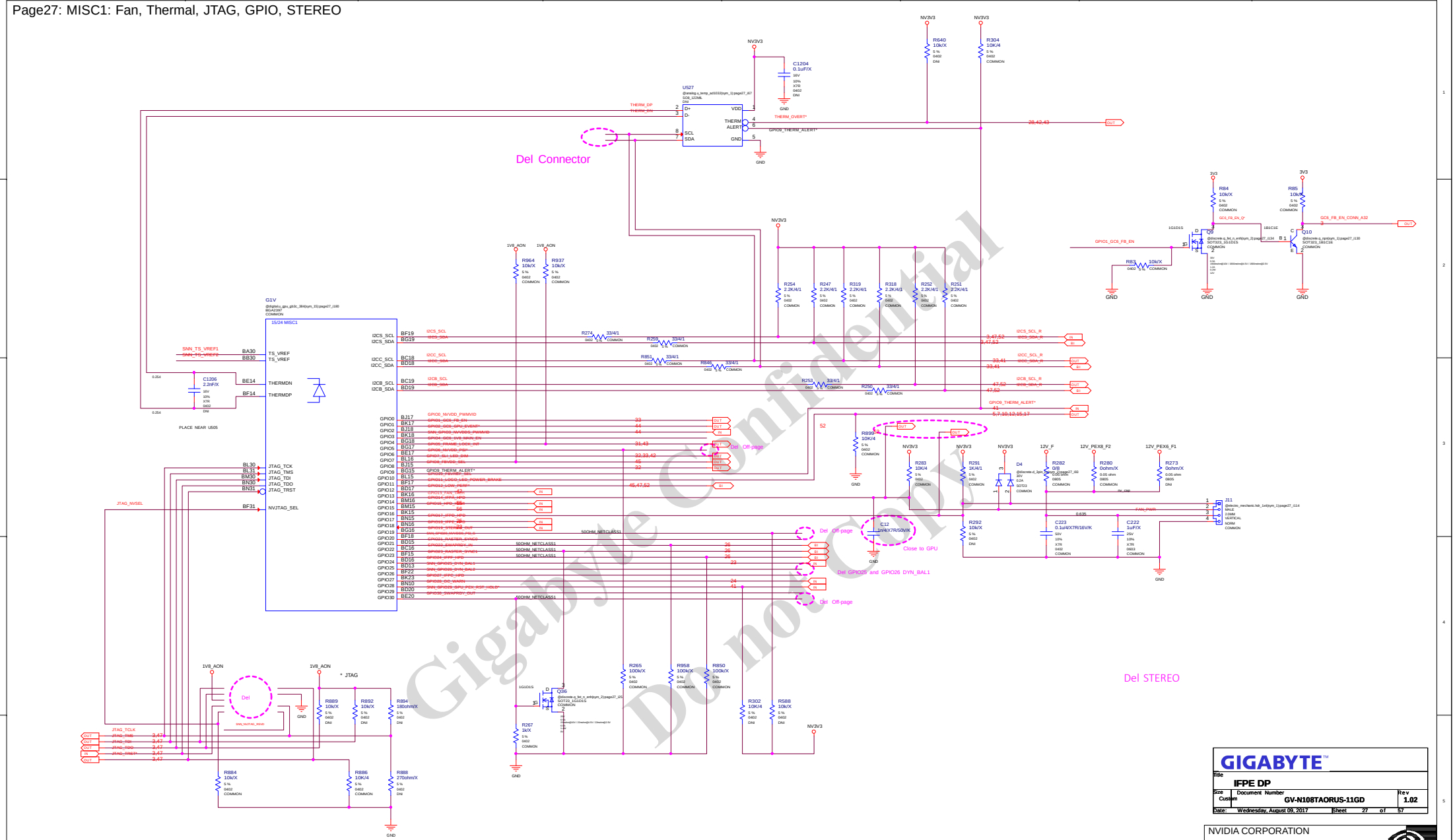
Page27: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: FAN, THERMAL, JTAG, GPIO, STEREO

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Page28: MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

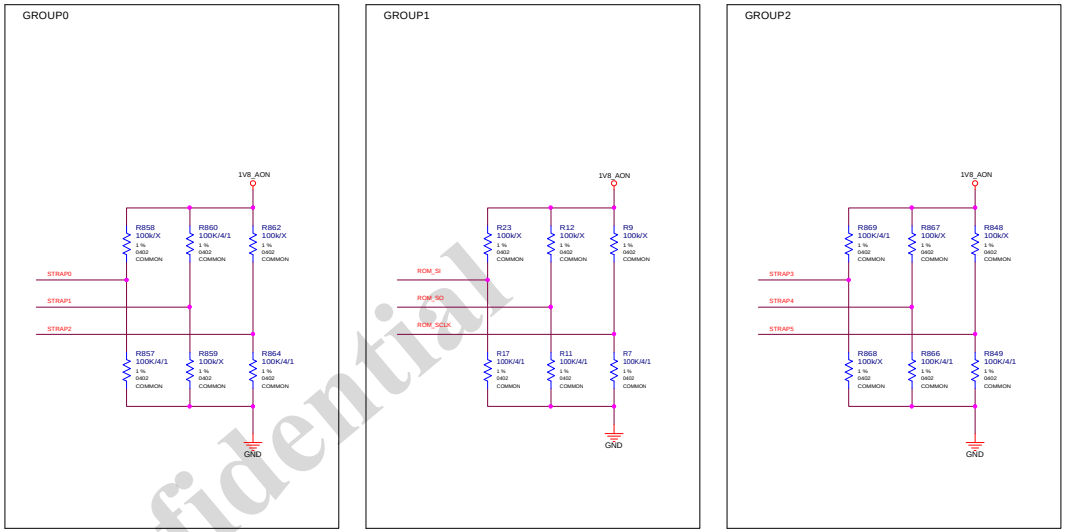
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

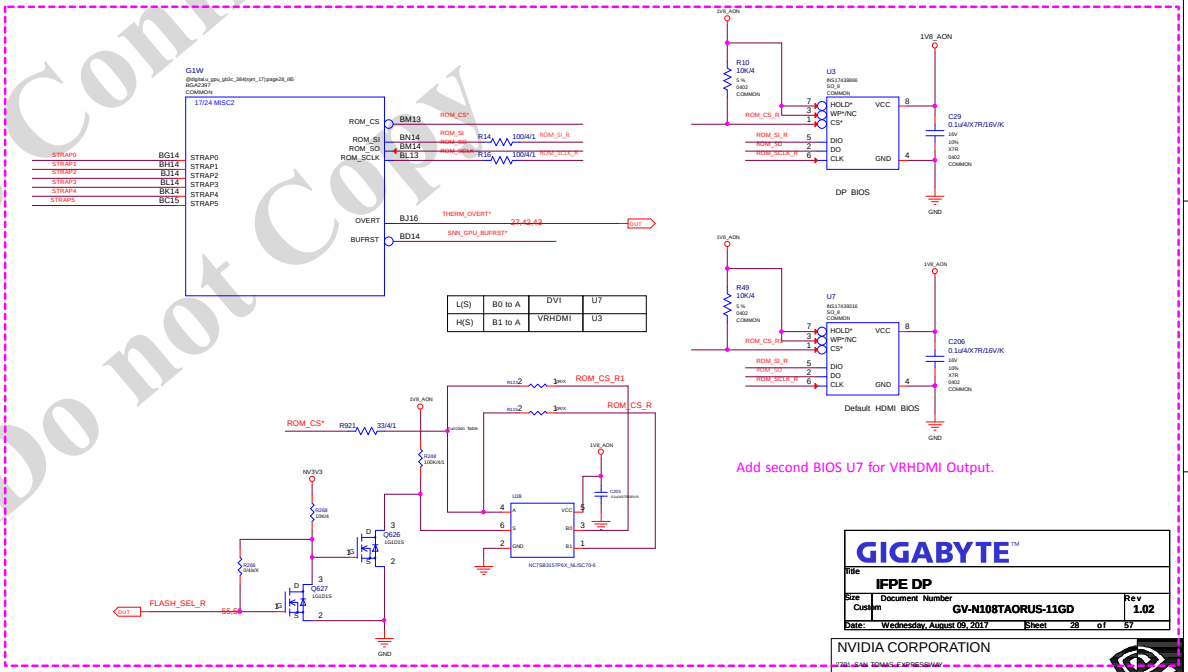
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: ROM, STRAPS

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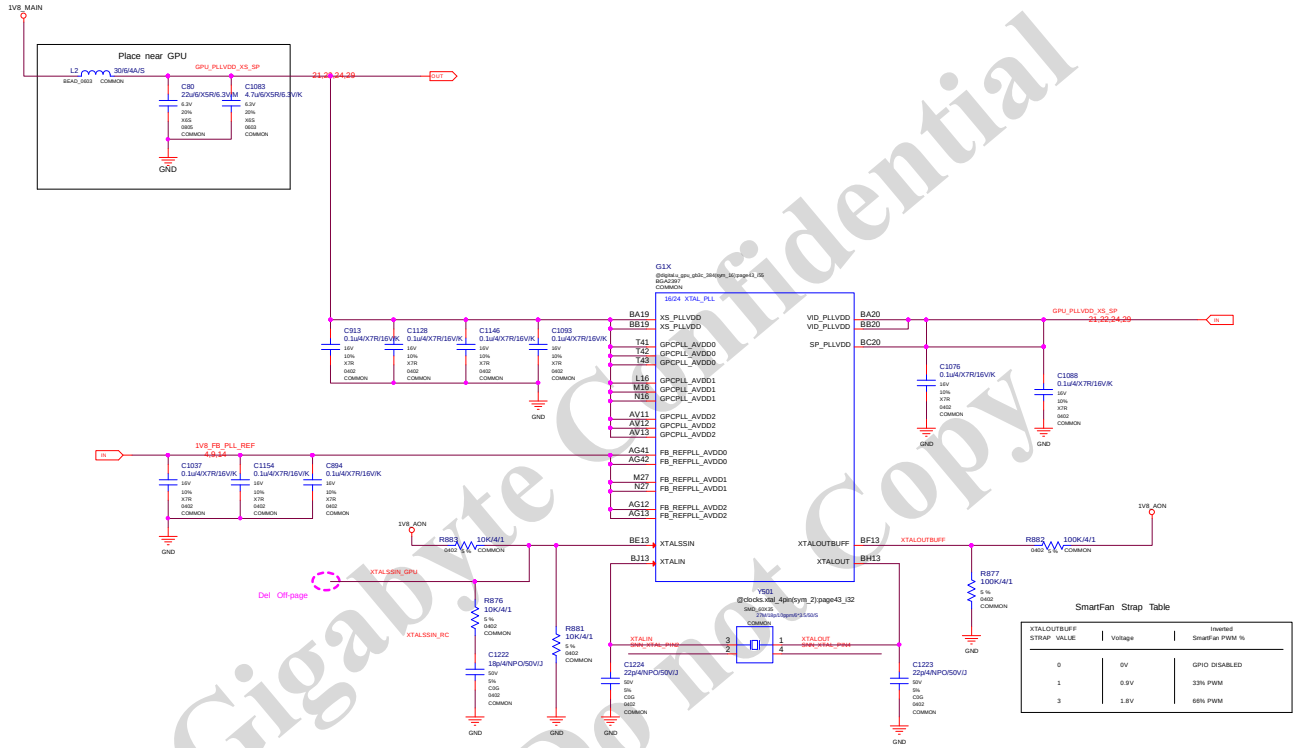

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: XTAL. PLL

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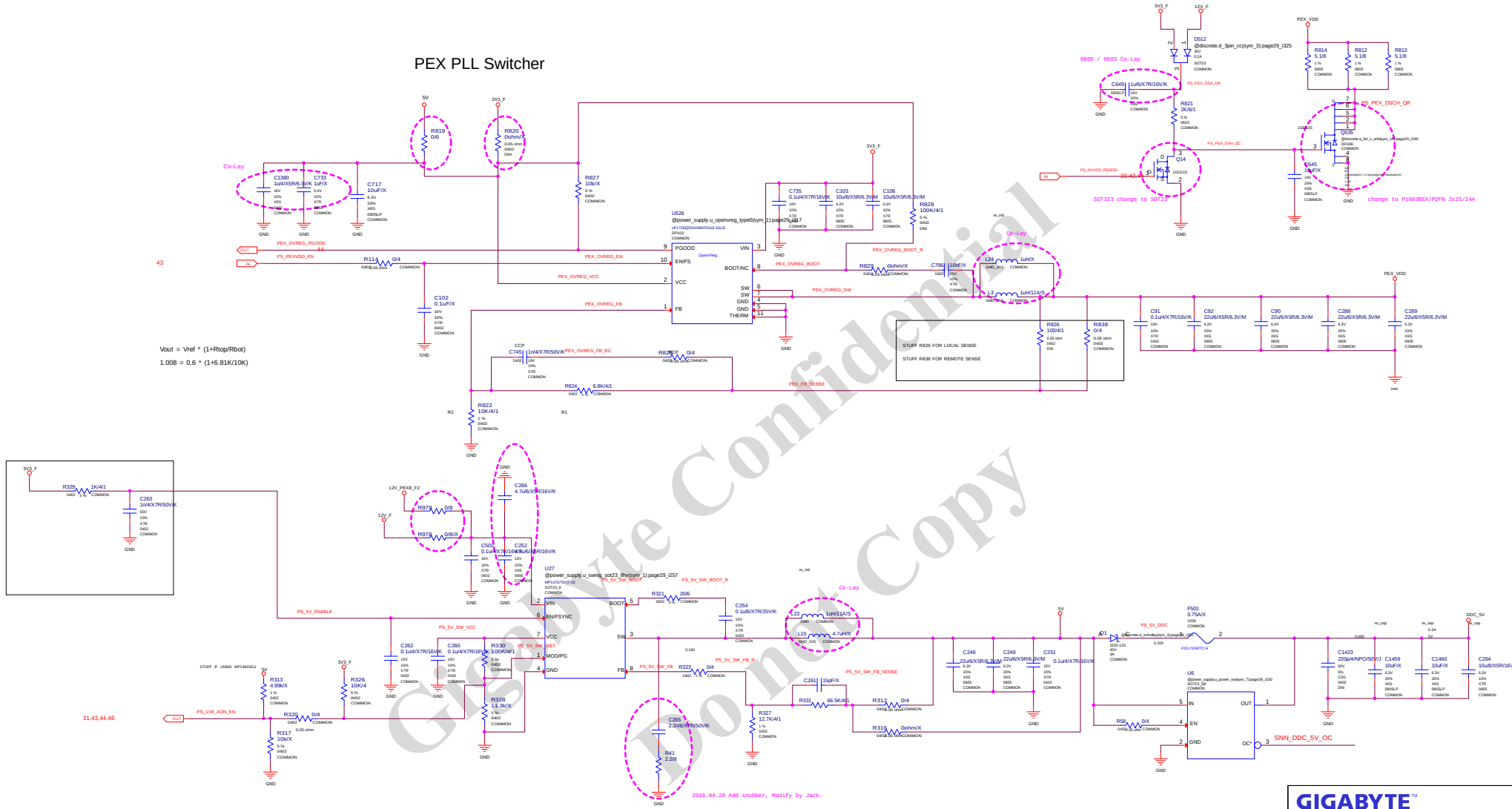

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 5V, PEXVDD

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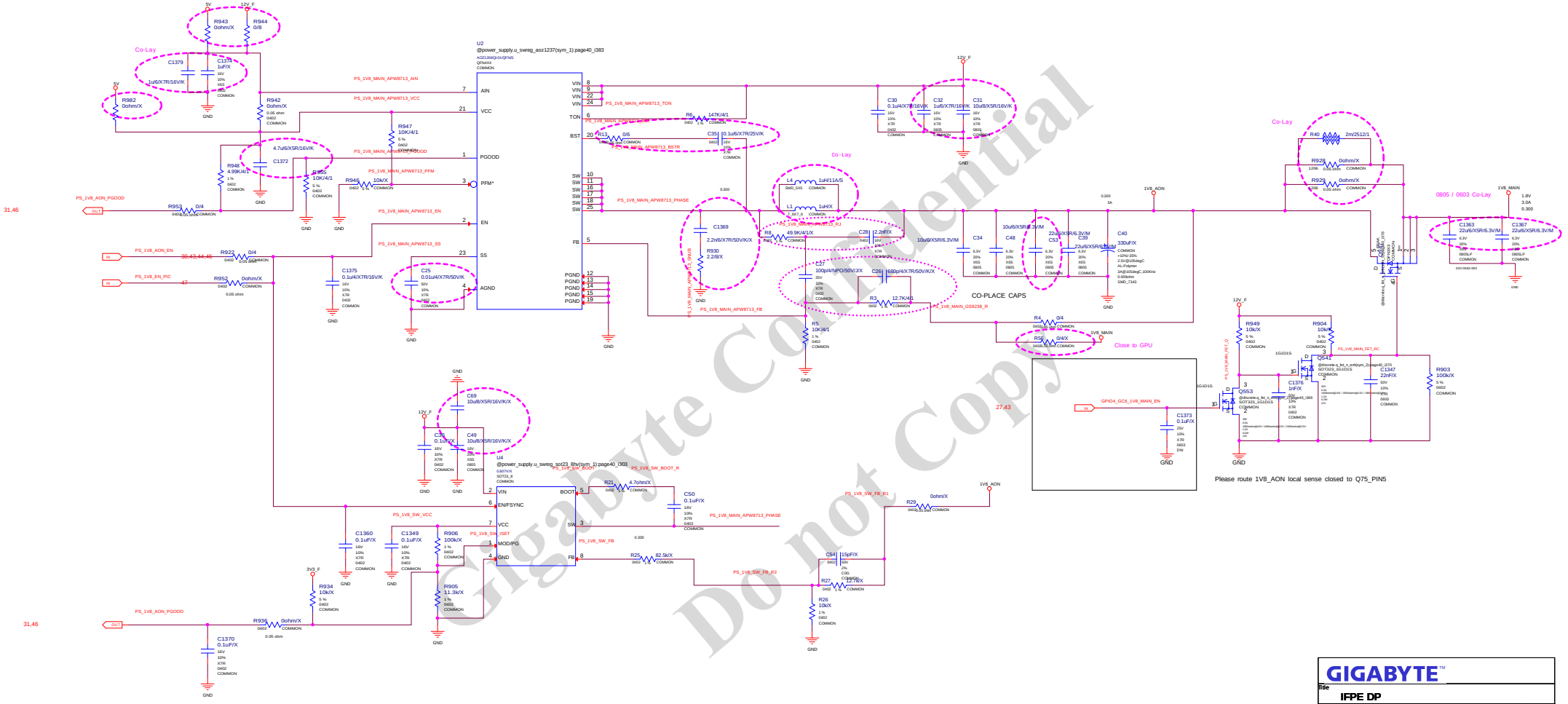

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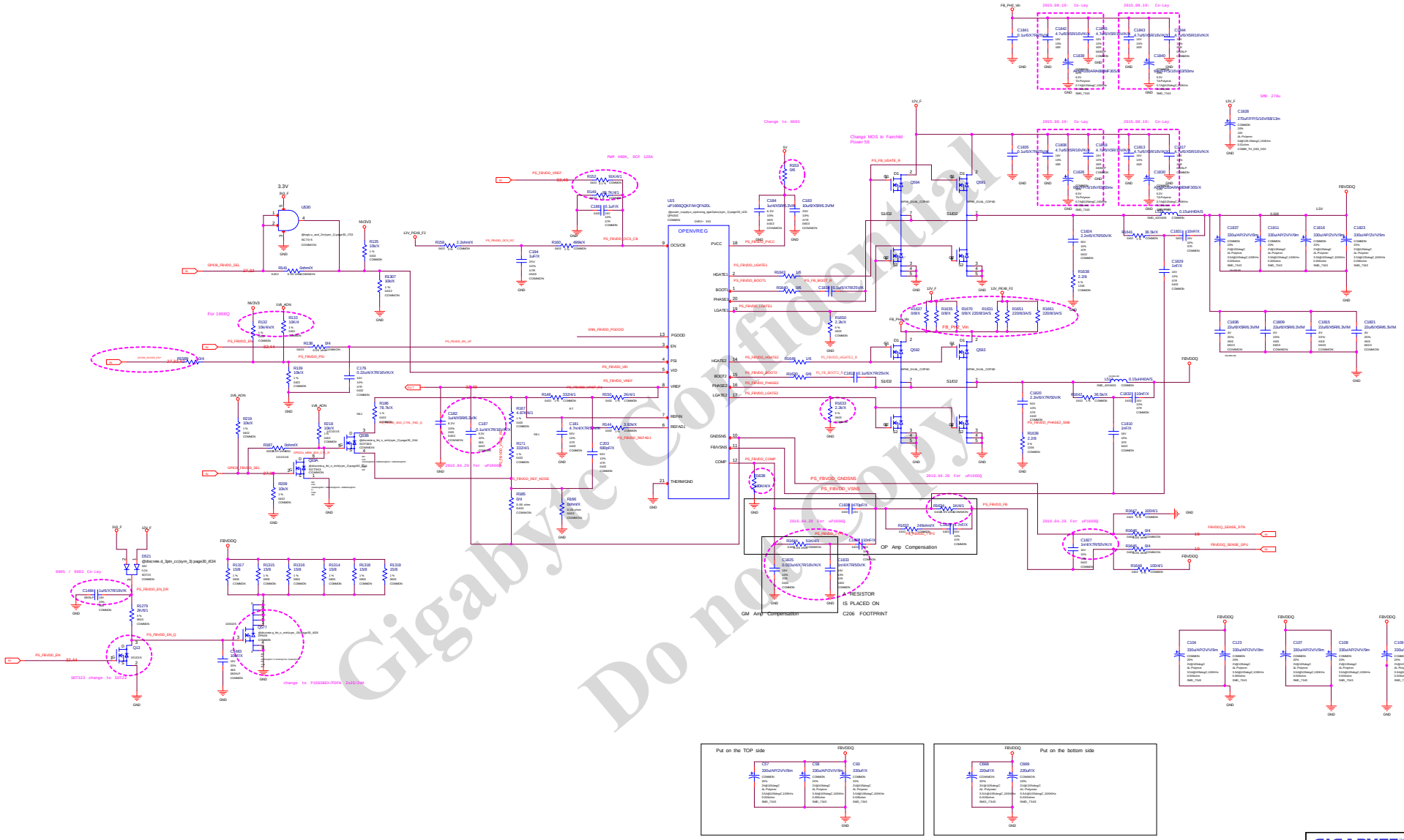

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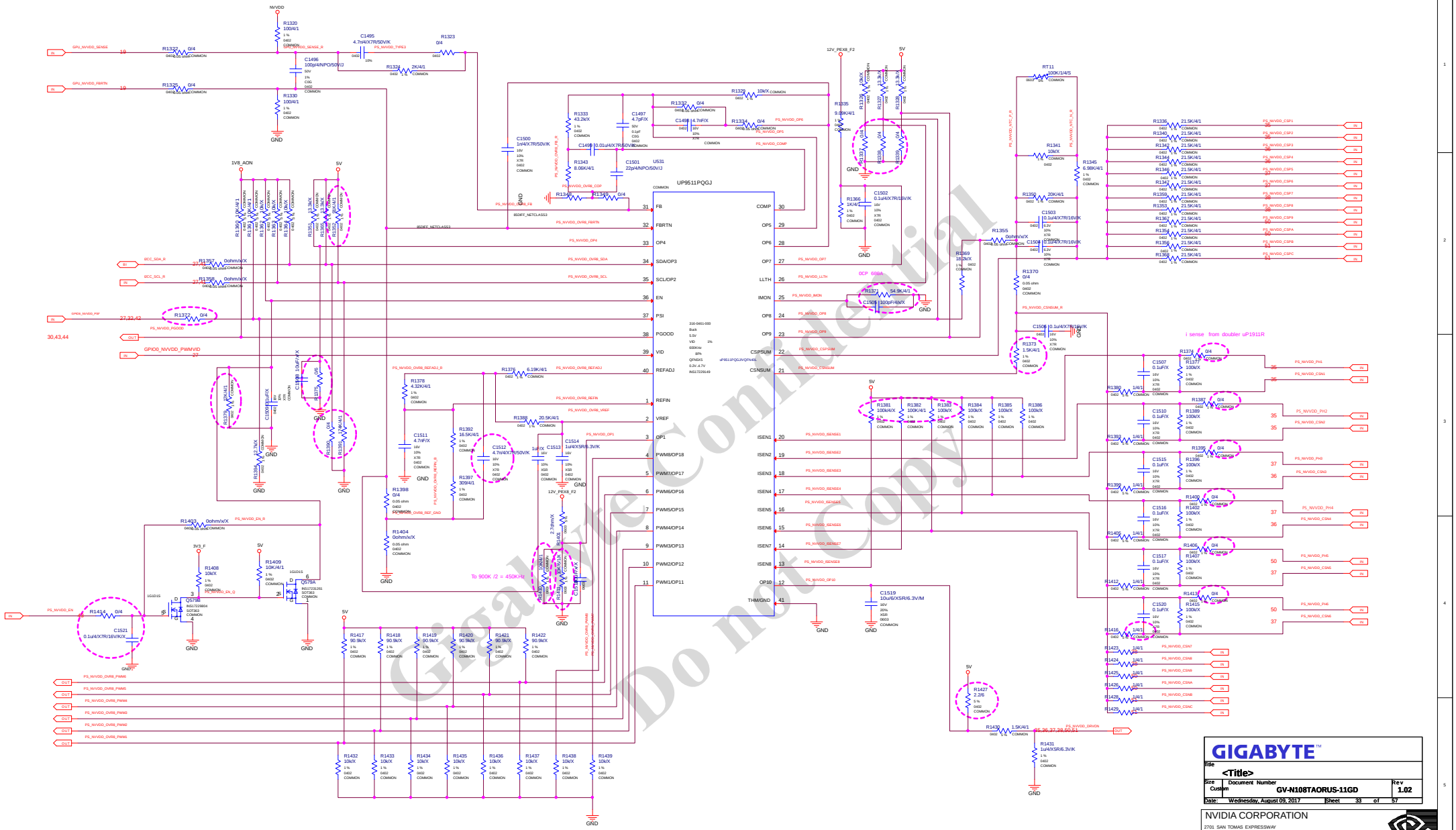
Page27: PS: NVVDD_OVR8



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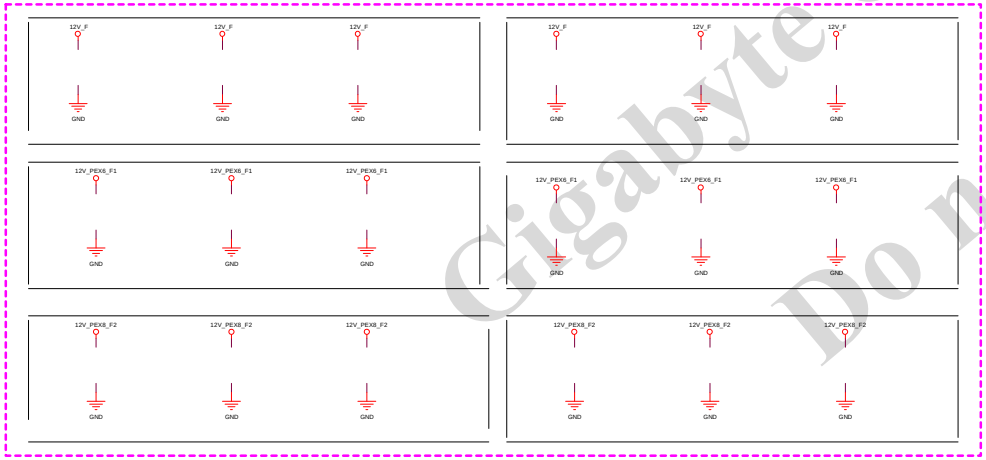
Del PWM MODULE

CO-LAYOUT: CHOOSE ONE ONLY



Del P-Board CAP

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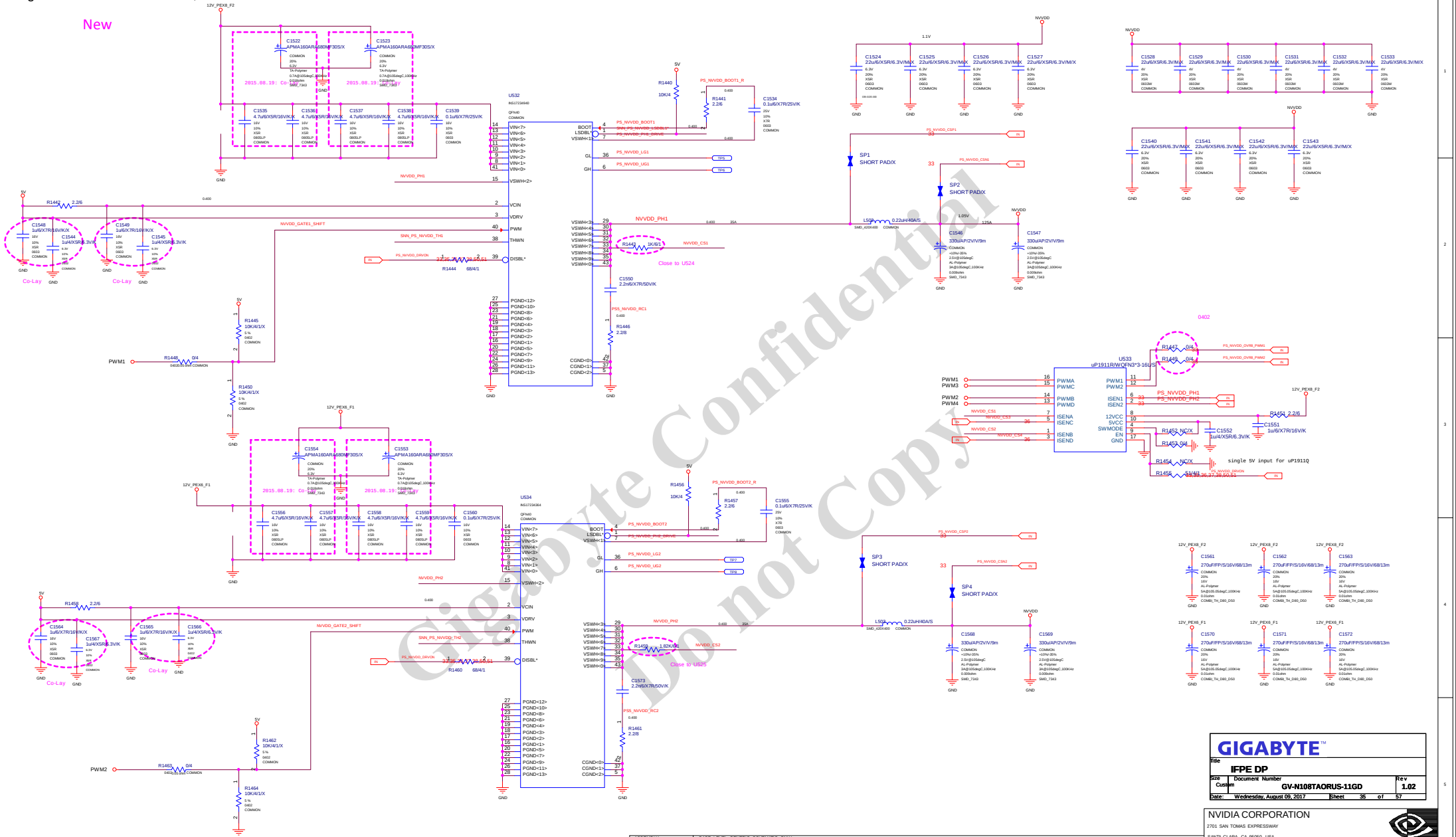
Page32: PS: NVVDD Phase 1,2

New



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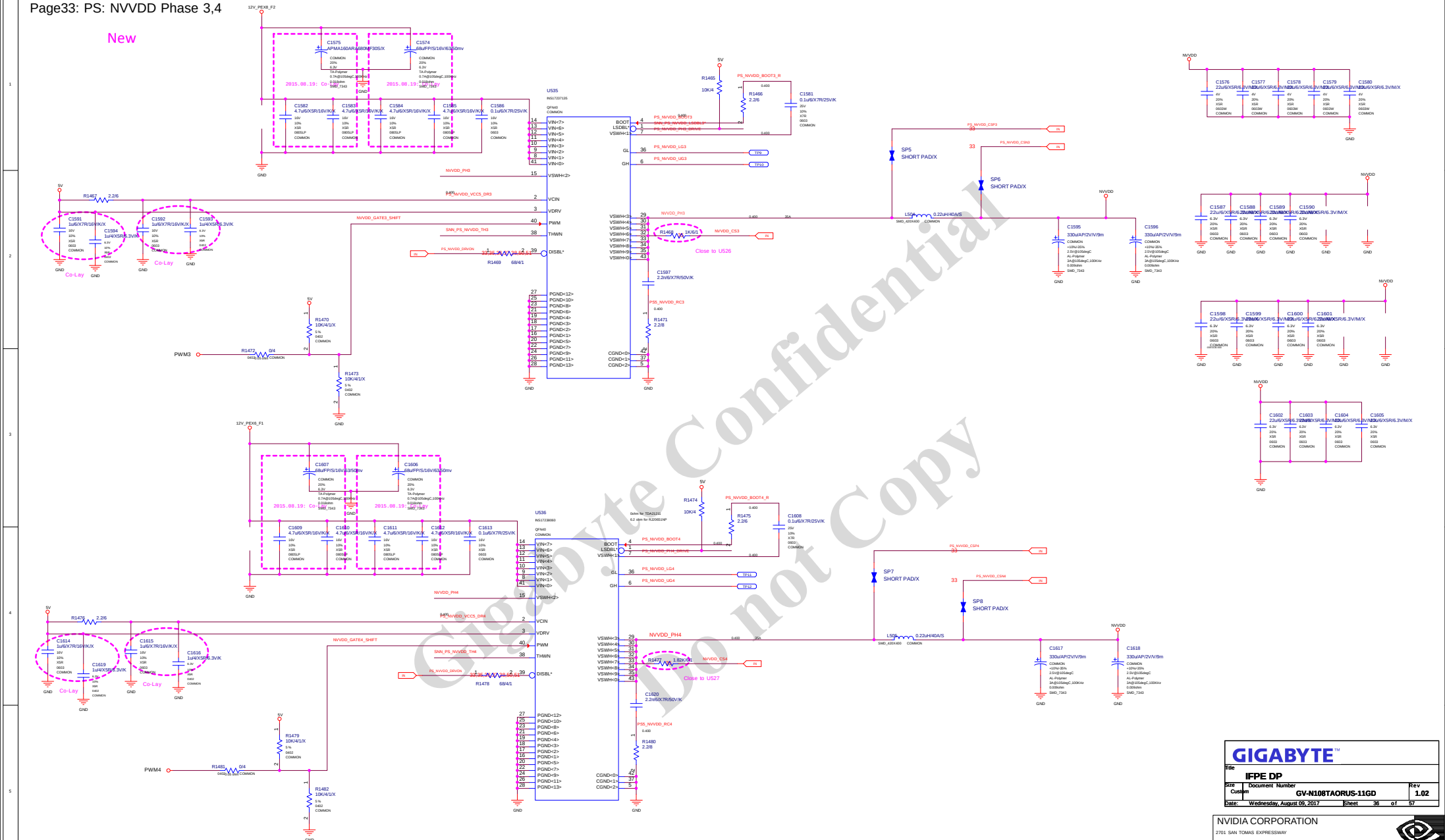
Page33: PS: NVVDD Phase 3,4

New



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Page34: PS: NVVDD Phase 5,6

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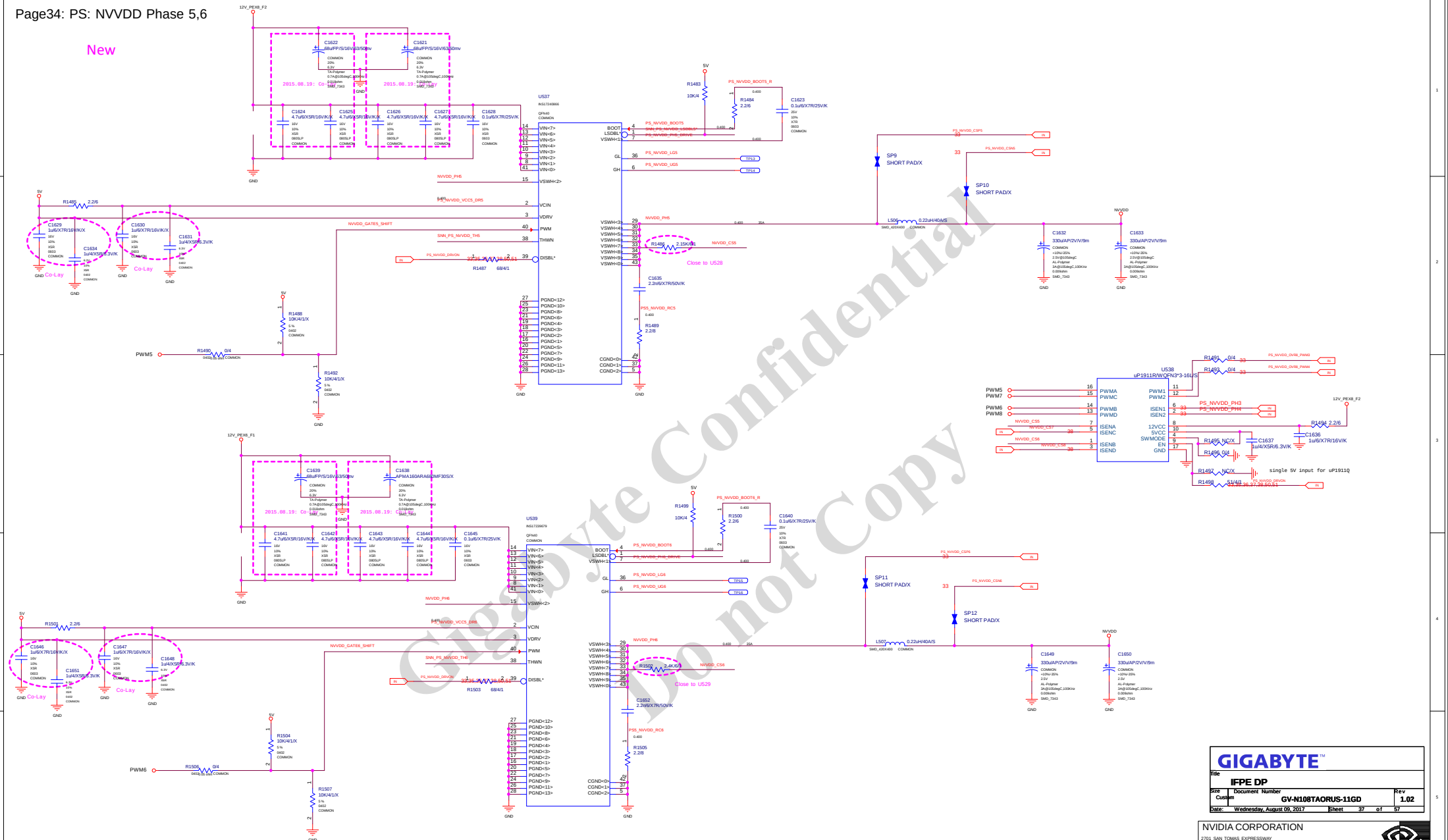

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 5,6

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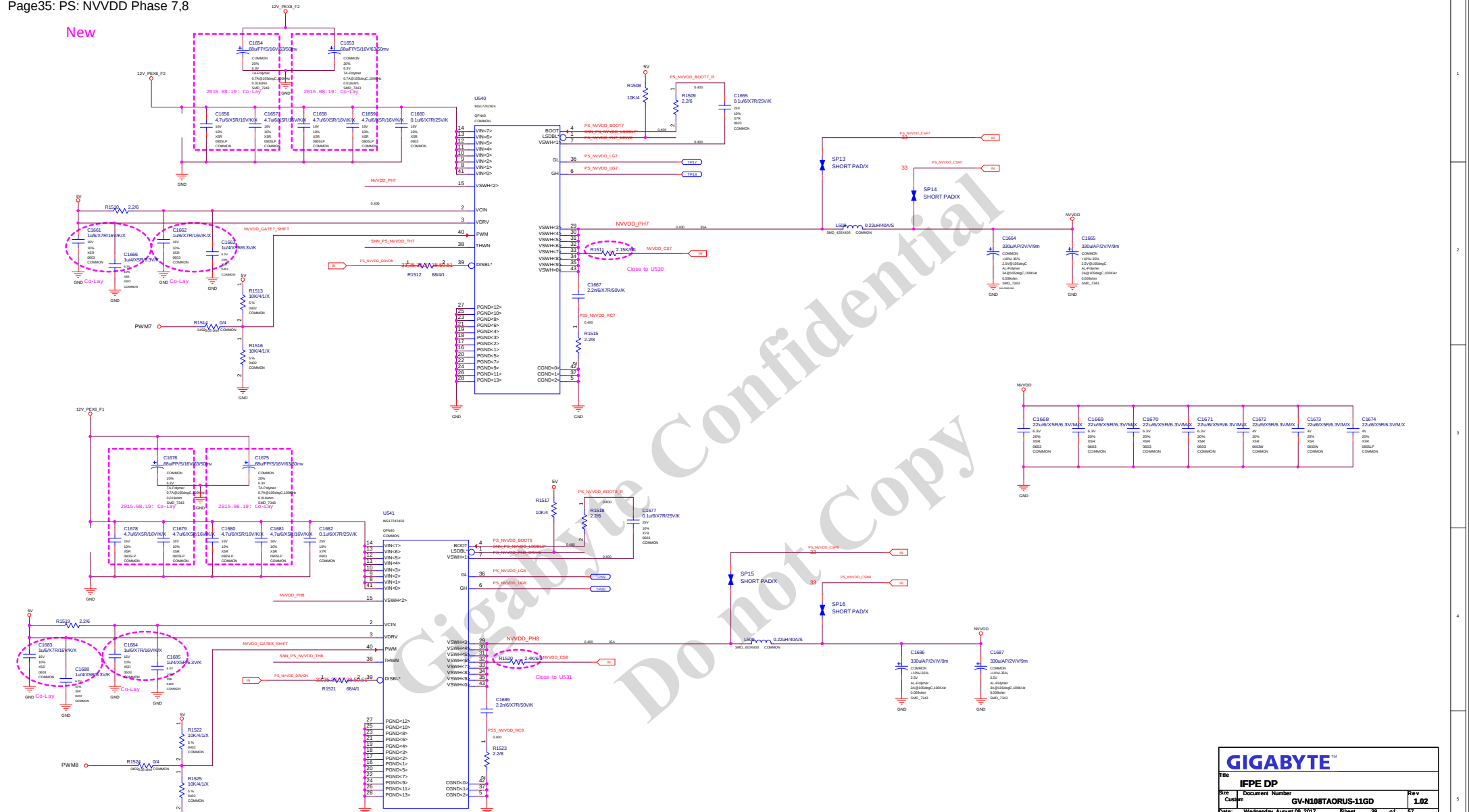
Page35: PS: NVVDD Phase 7,8

New



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CO-LAYOUT: CHOOSE UA OR UB

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVDD Dynamic Switch Phases

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Page39: PS: Dynamic Power Balance Phases

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Dynamic power balance phase

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Page40: PS: Dynamic Power Balance Logic

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>		
PAGE DETAIL	PS: Dynamic power balance logic		
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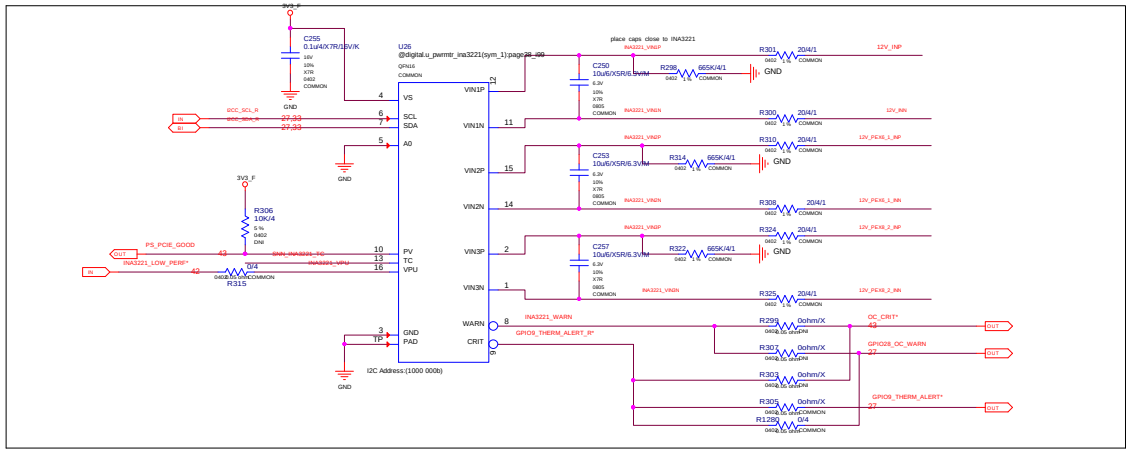
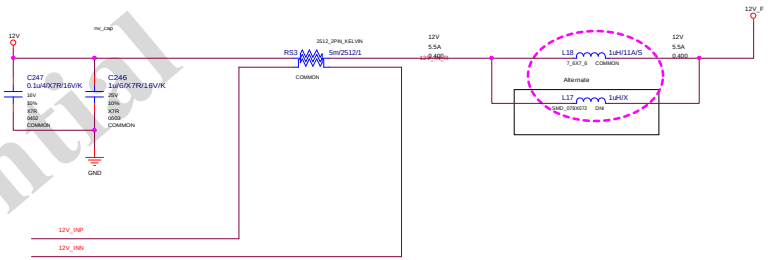
Page41: PS: Inputs, Filtering, and Monitoring

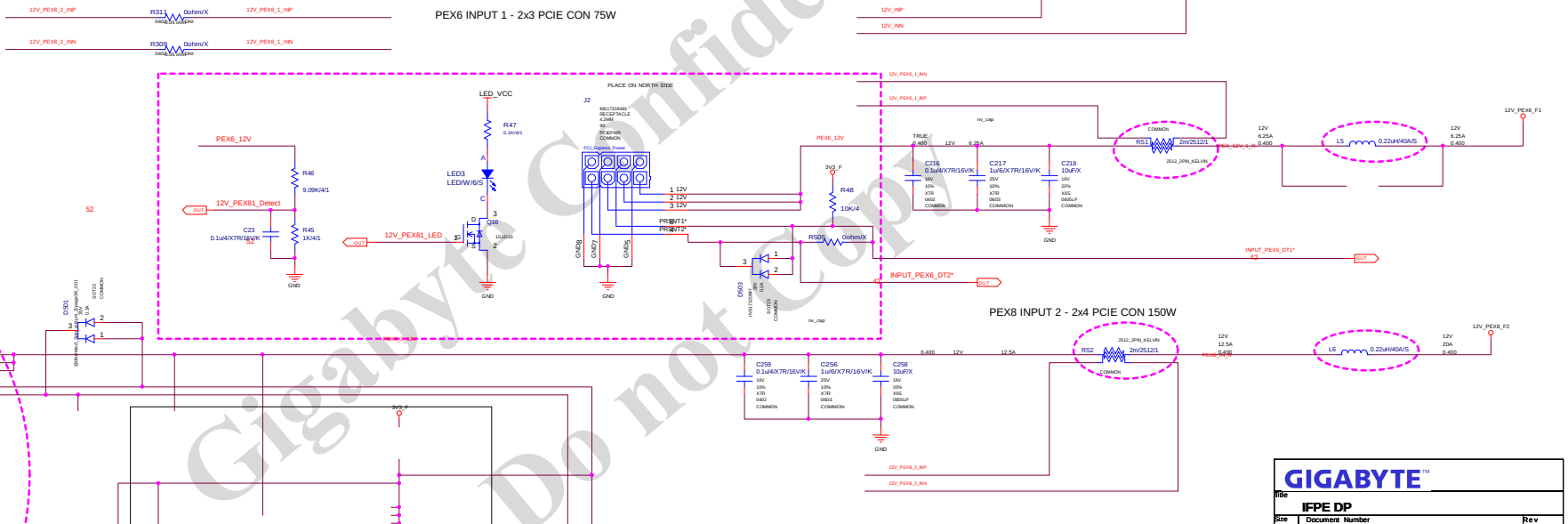


PEX 3V3 INPUT - 10W

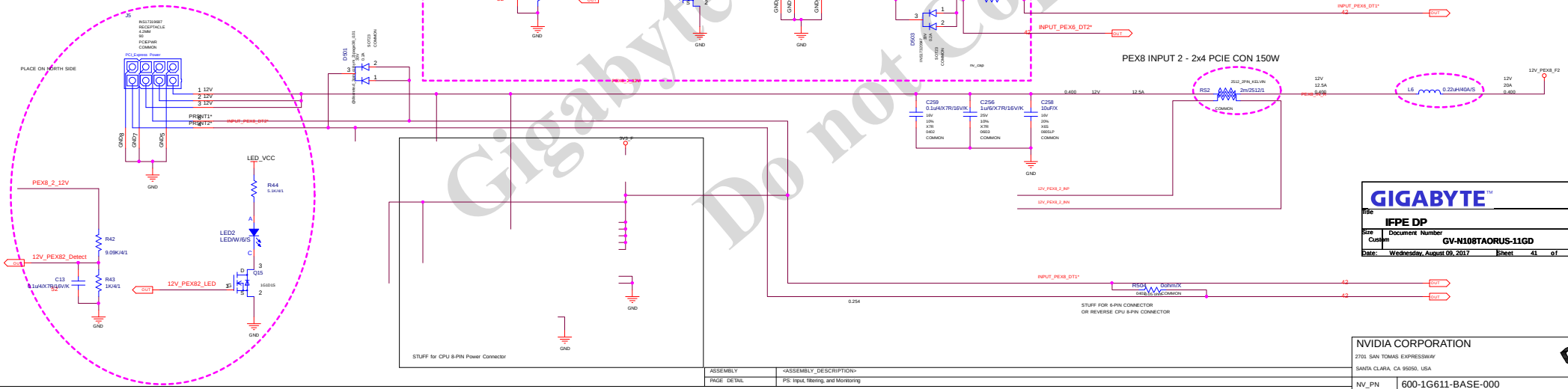
PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Input, filtering, and Monitoring

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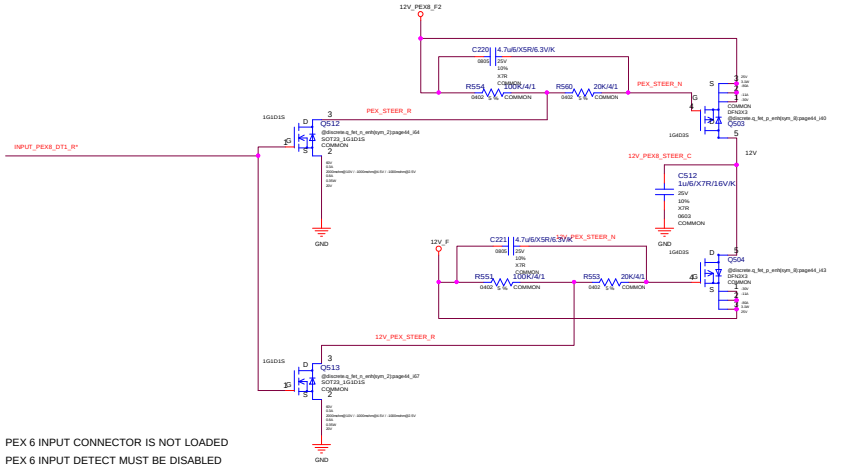
Page42: PS: 12V Current Steering & Hot Unplug Detect

QUADRO/TESLA:

12V CURRENT STEERING (UNDER POWER BOOT):

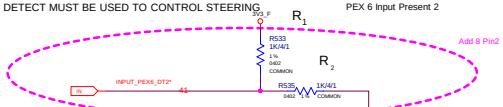
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



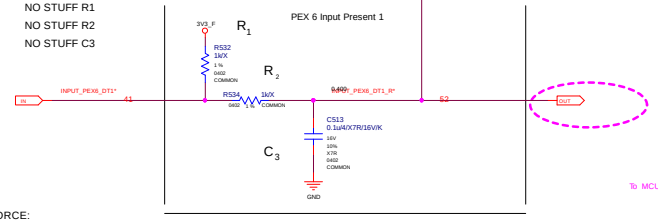
PEX 6 INPUT CONNECTOR IS NOT LOADED
PEX 6 INPUT DETECT MUST BE DISABLED
PEX 8 INPUT DETECT MUST BE USED TO CONTROL STEERING

PEX 6 Input Present 2



NO STUFF R1
NO STUFF R2
NO STUFF C3

PEX 6 Input Present 1



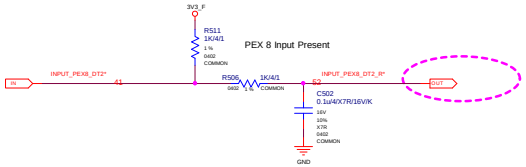
GeFORCE:

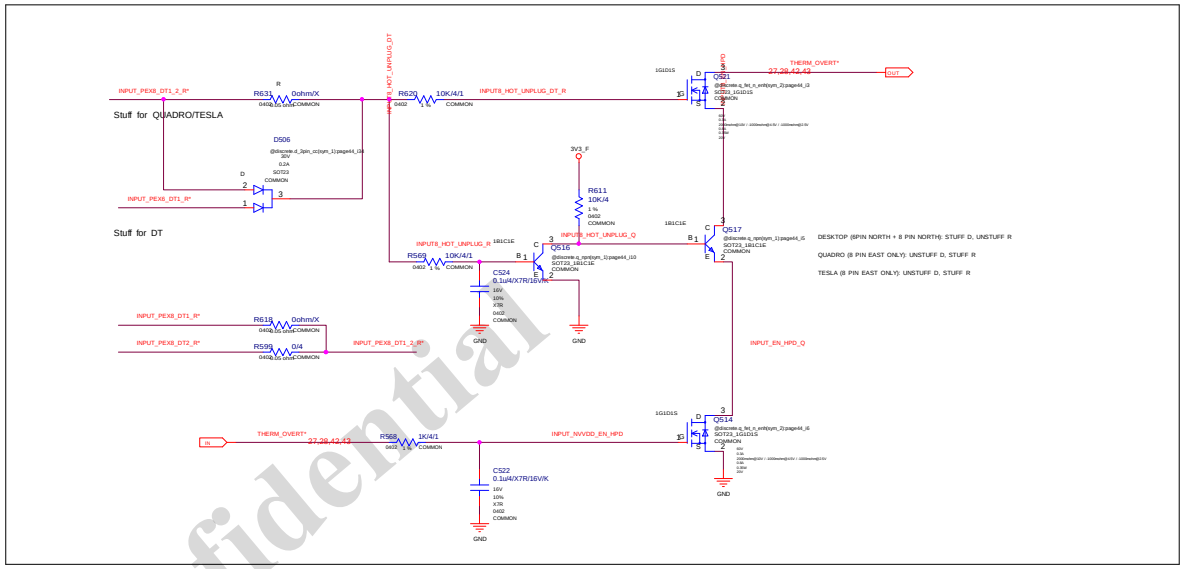
PEX 6 INPUT CONNECTOR IS LOADED
PEX 6 INPUT DETECT MUST BE USED TO CONTROL STEERING

STUFF R1
STUFF R2
STUFF C3

PEX6 IN PEX8 CONNECTOR Present

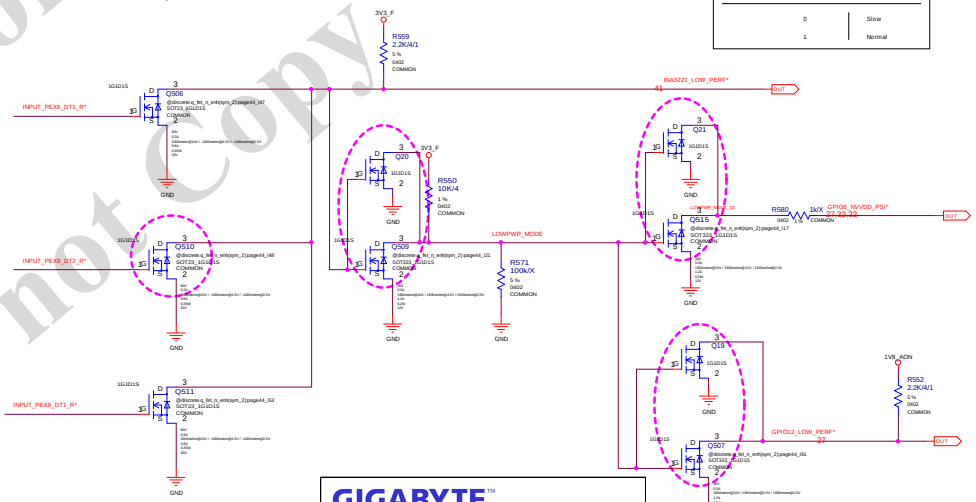
PEX 8 Input Present





PEX Input - Under Power Boot Controls

GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal



A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	PS: Current Steering, Hot Unplug

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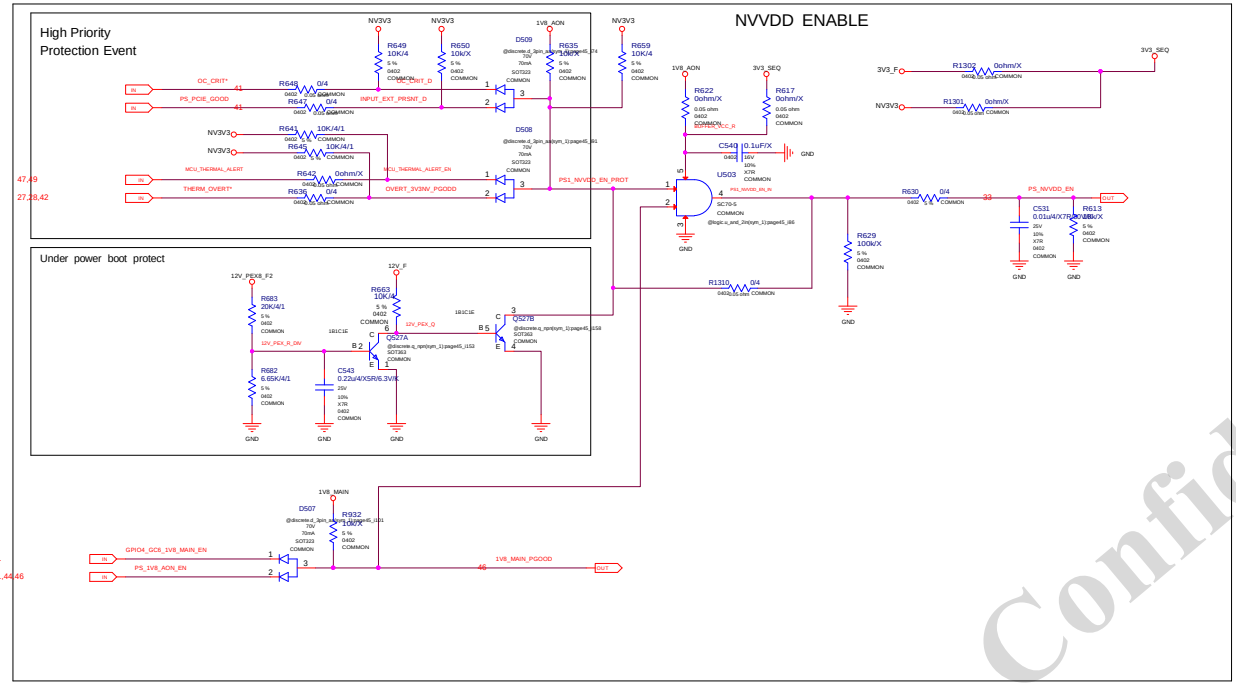
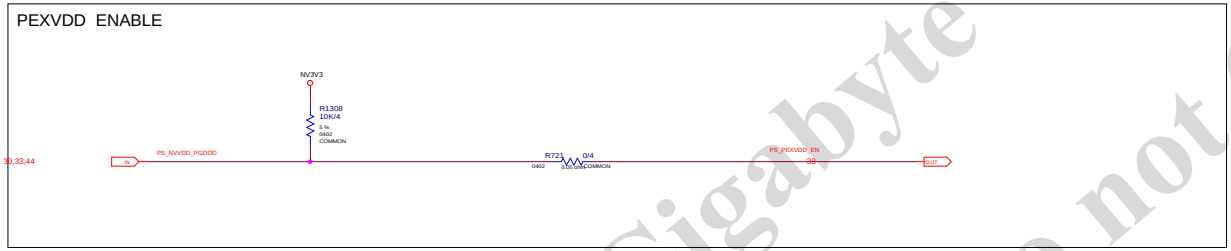
Page43: PS: NVVDD ENABLE





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ASSEMBLY	<ASSEMBLY_DESCRIPTION>		
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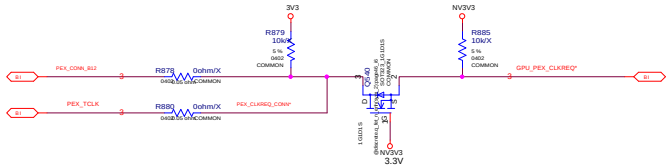
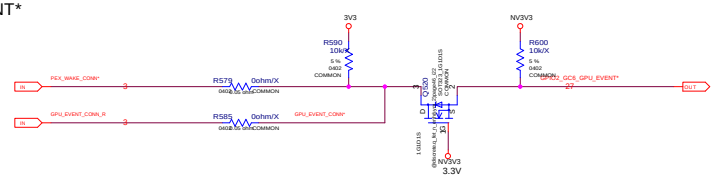
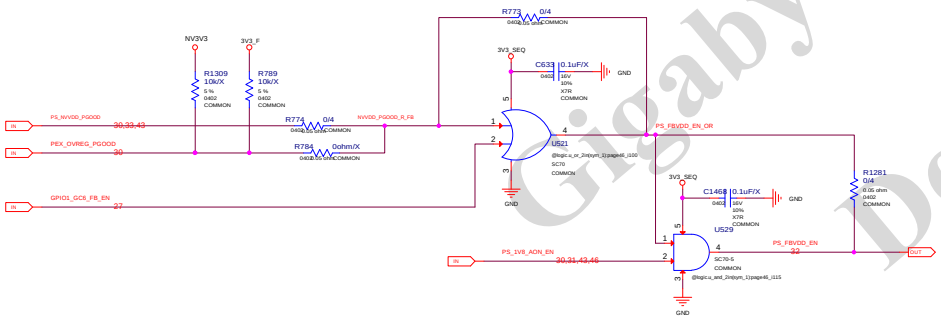
PEX_CLKREQ*



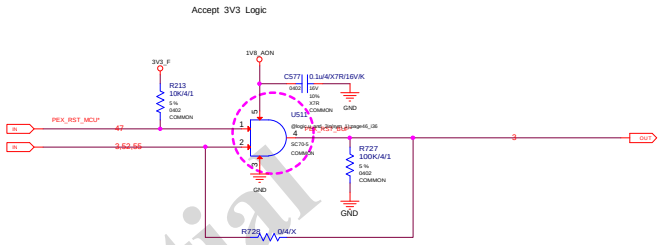
GPU_EVENT*



FBVDD/Q ENABLE



PEX_RST# LOGIC



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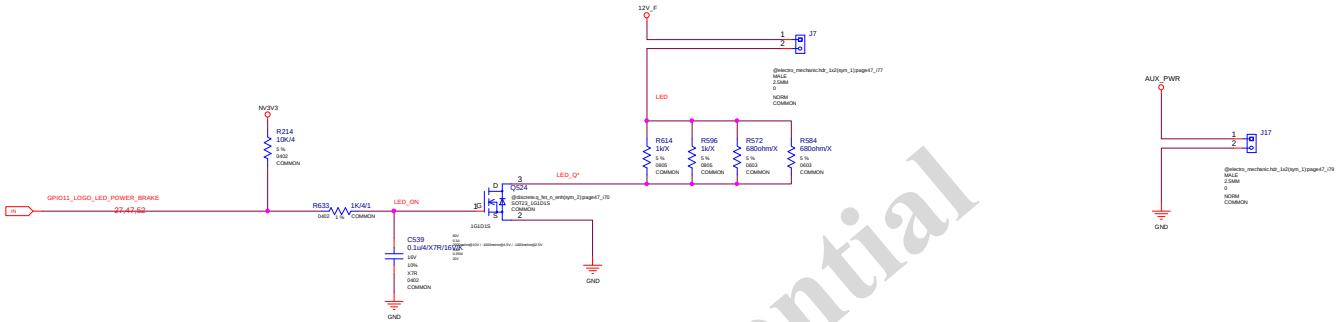
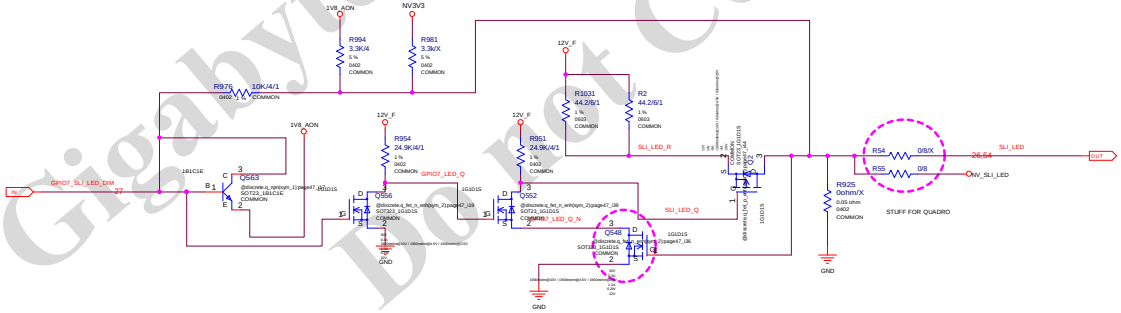
Page45:GEFORCE LED & SLI LED

LED HEADER(GEFORCE ONLY)



SLI LED (GEFORCE ONLY)



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GEFORCE LED AND SLI LED

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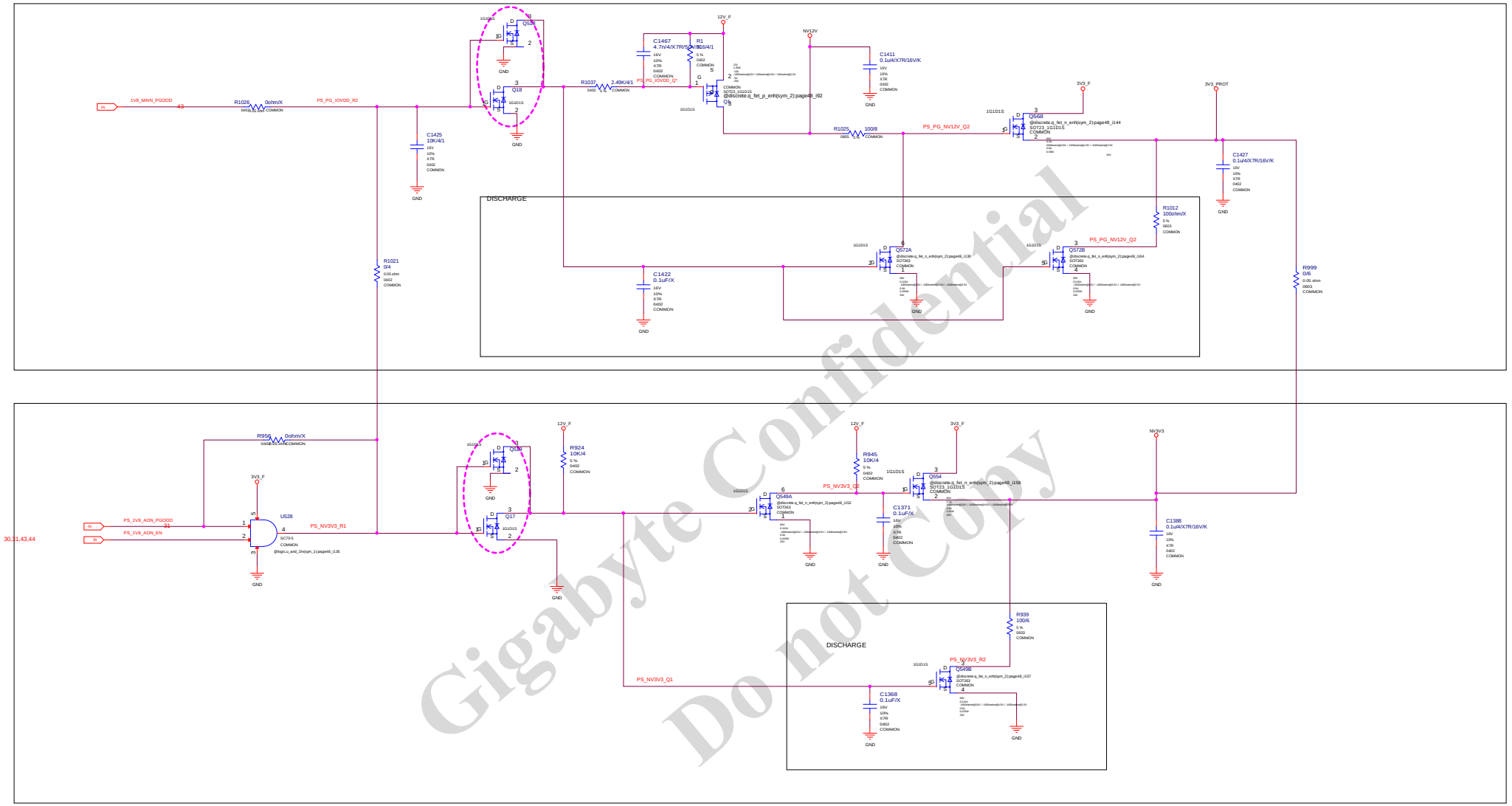

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PAGE DETAIL	PS: NV3V3, NV12V

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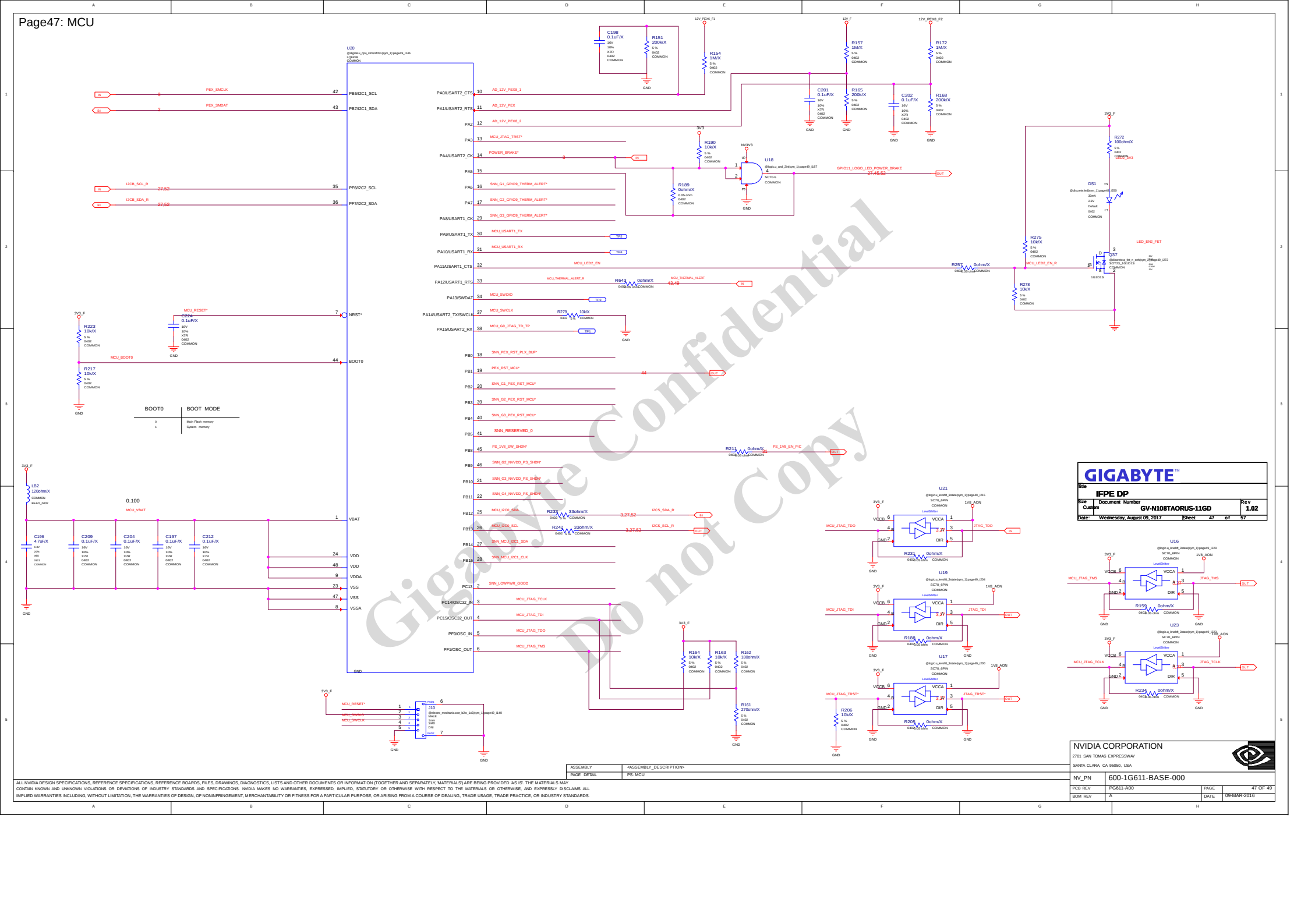
Page47: MCU



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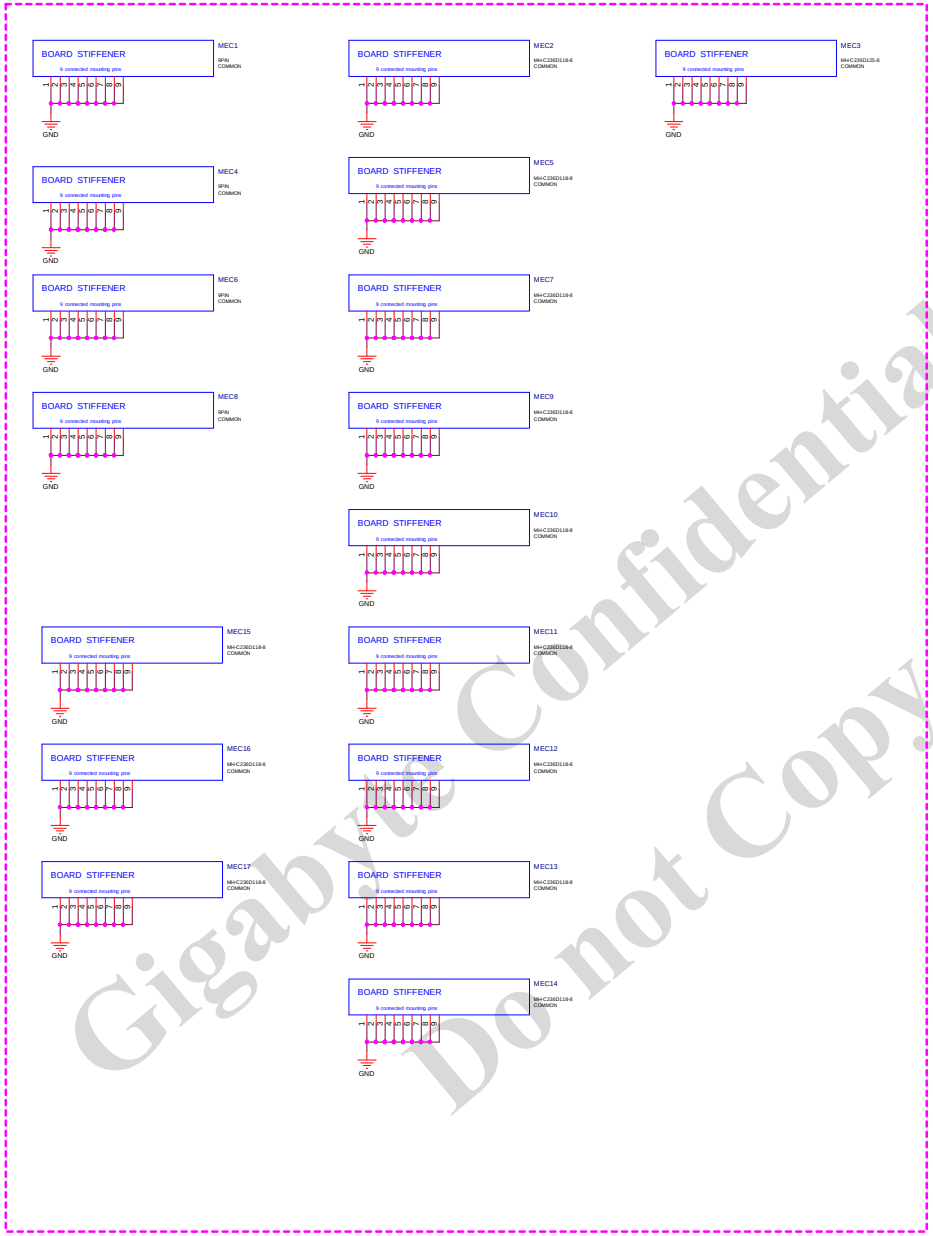

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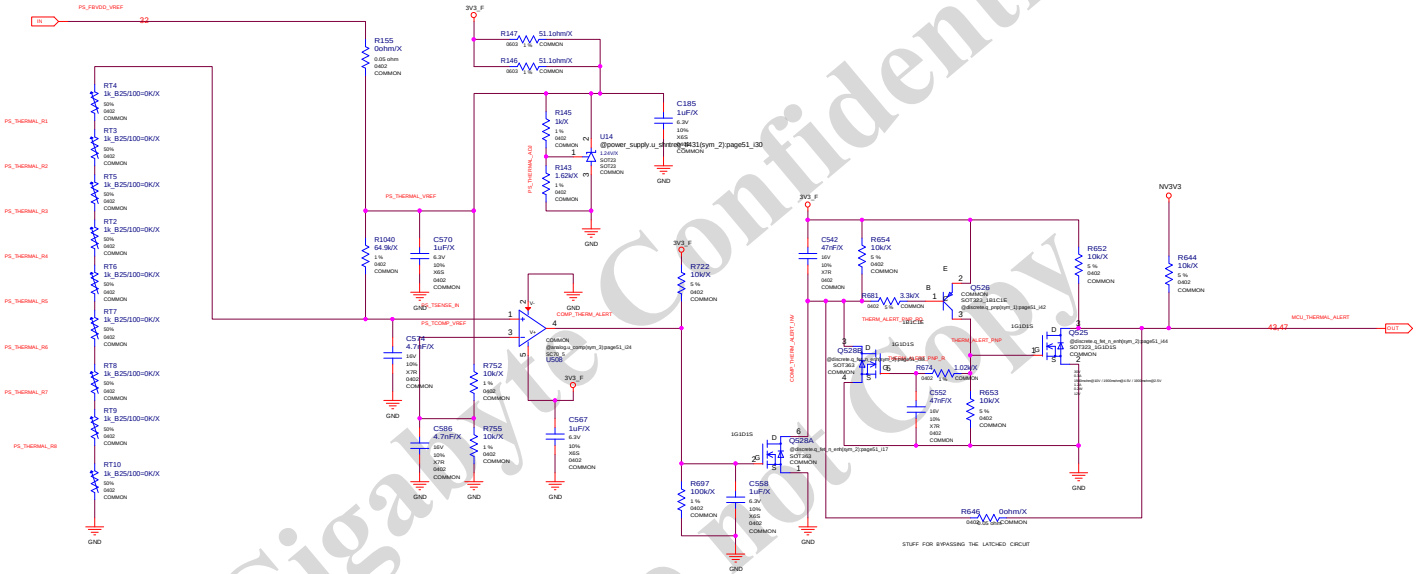

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Title	IFPE DP	
Size: Custom	Document Number: GV-N108TAORUS-11GD	Rev: 1.02
Date: Wednesday, August 09, 2017	Sheet 49 of 57	

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G611-BASE-000		
PCB REV	PG611-A00	PAGE	49 OF 49
BOM REV	A	DATE	09-MAR-2016

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	VR Thermal Protection

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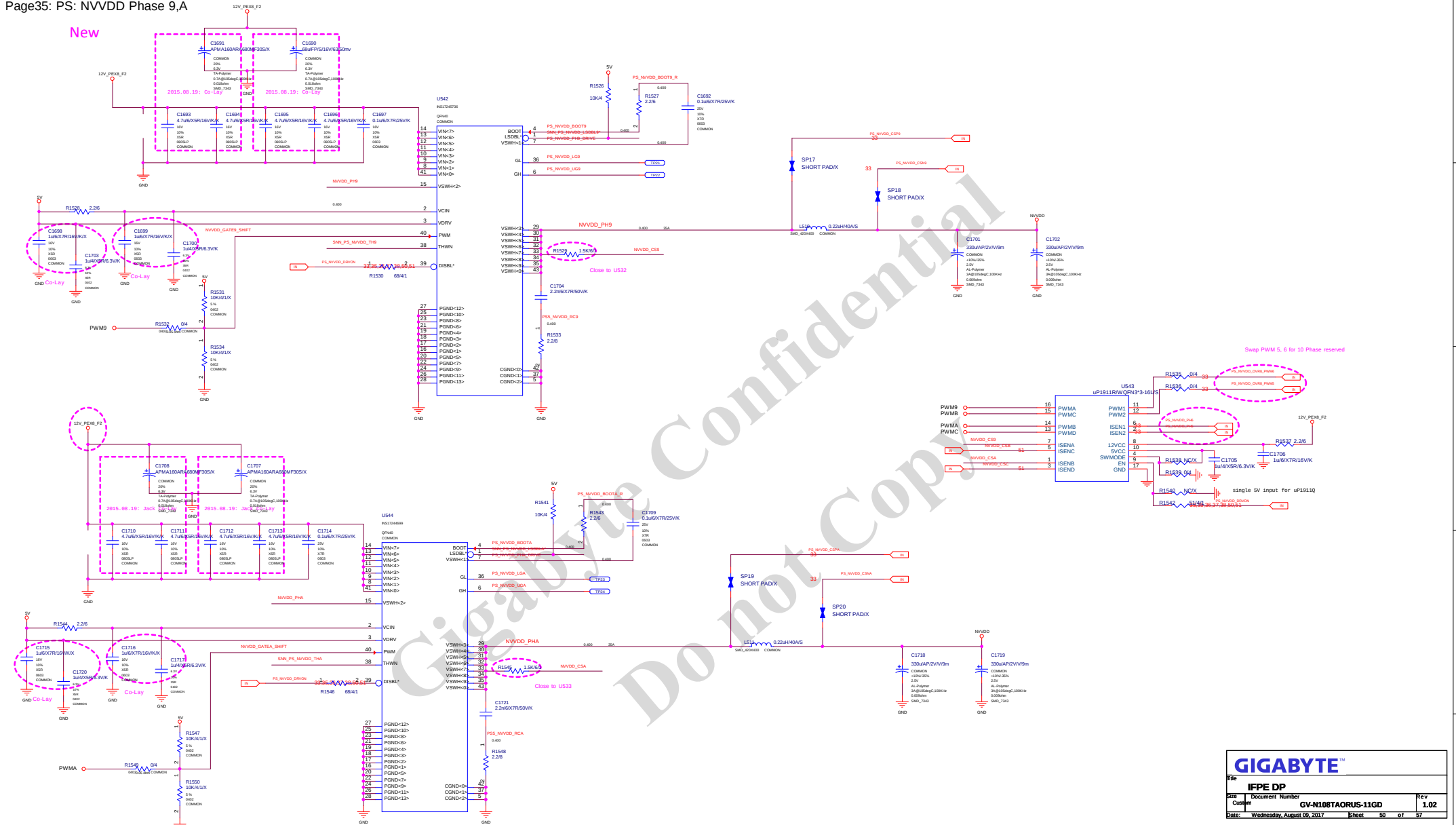
Page35: PS: NVVDD Phase 9,A

New



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CO-LAYOUT: CHOOSE UA OR UB

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVDD Dynamic Switch Phases

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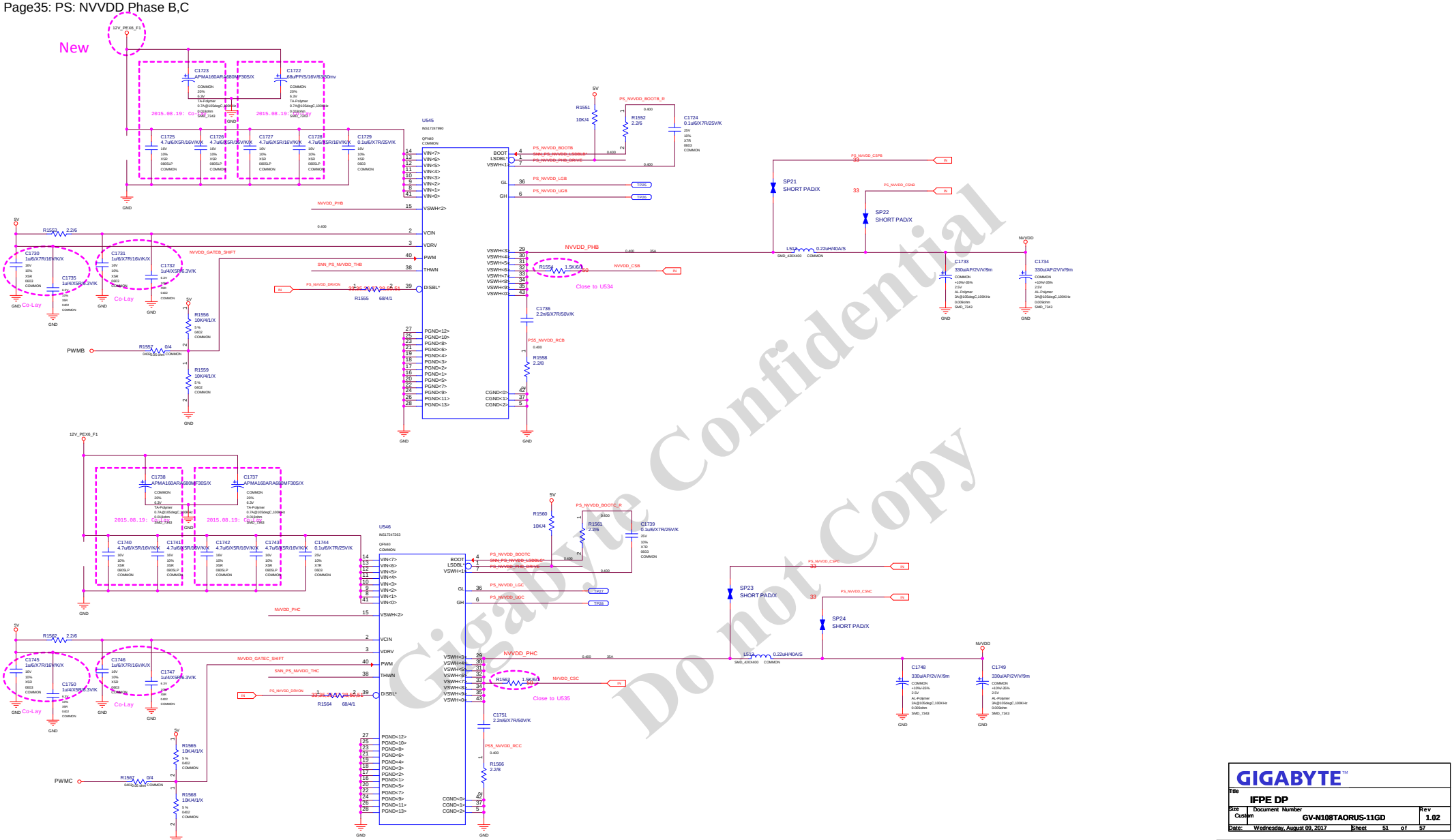
BOM REV	A	DATE	21-APR-2015

Page35: PS: NVVDD Phase B,C



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVDD Dynamic Switch Phases

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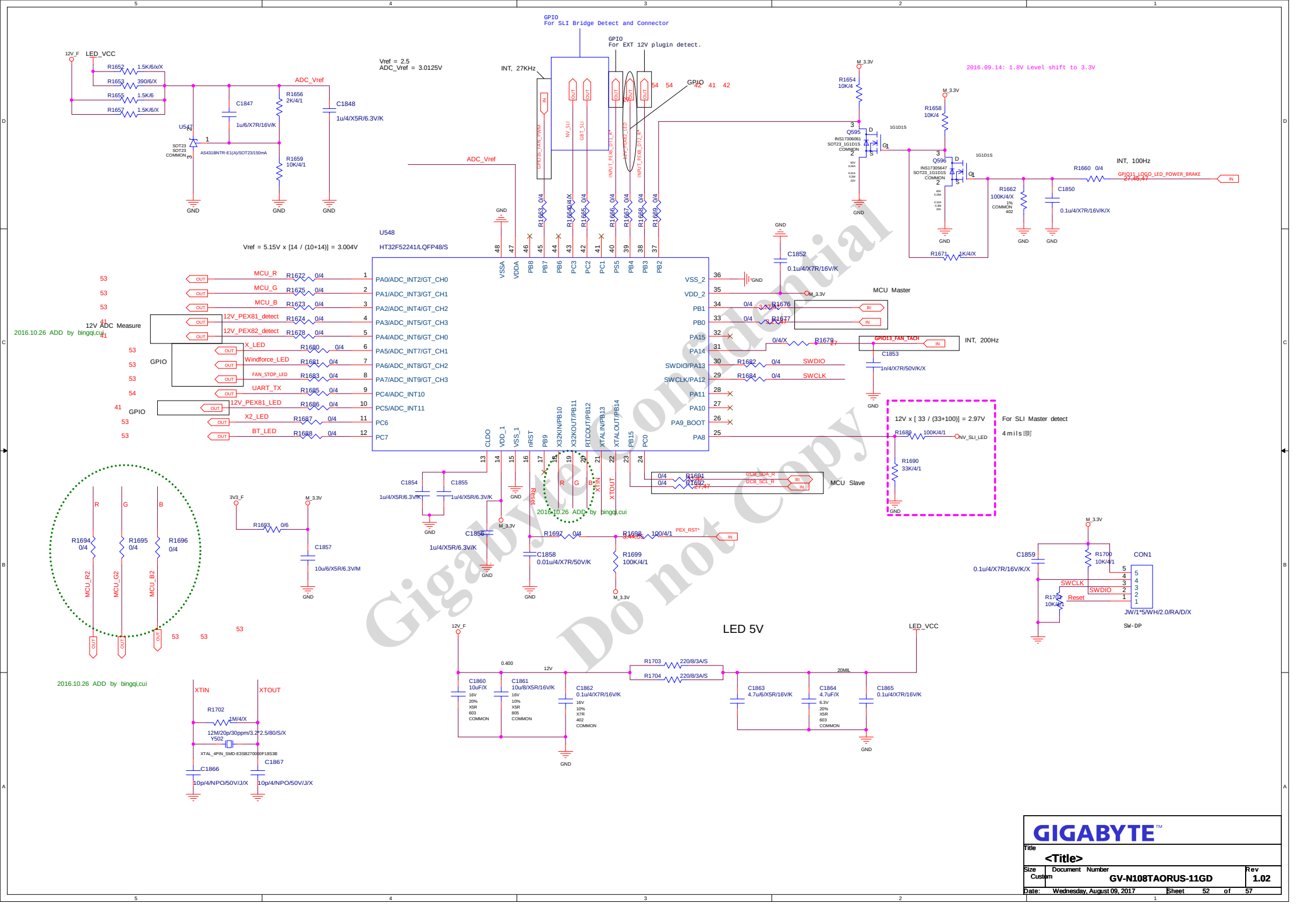
SANTA CLARA, CA 95050, USA

NV_PN	600-1G600-BASE-QS1		
PCB REV	PG600-B02	PAGE	35 OF 45
BOM REV	A	DATE	21-APR-2015


GPIO
For SLI Bridge Detect and Connector
GPIO
For EXT 12V plugin detect.
2016.09.14: 1.8V Level shift to 3.3V
Vref = 2.5
ADC_Vref = 3.0125V
Vref = 5.15V x [14 / (10+14)] = 3.004V
U548
HT32F52241/LQFP48/S
12V ADC Measure
2016.10.26 ADD by bingqi.cui
GPIO
MCU Master
MCU Slave
For SLI Master detect
4 mils 印
LED 5V
Reset
SWCLK
SWDIO
JW/1*5/WH/2.0/RA/D/X
SW-DP
GIGABYTE
Title
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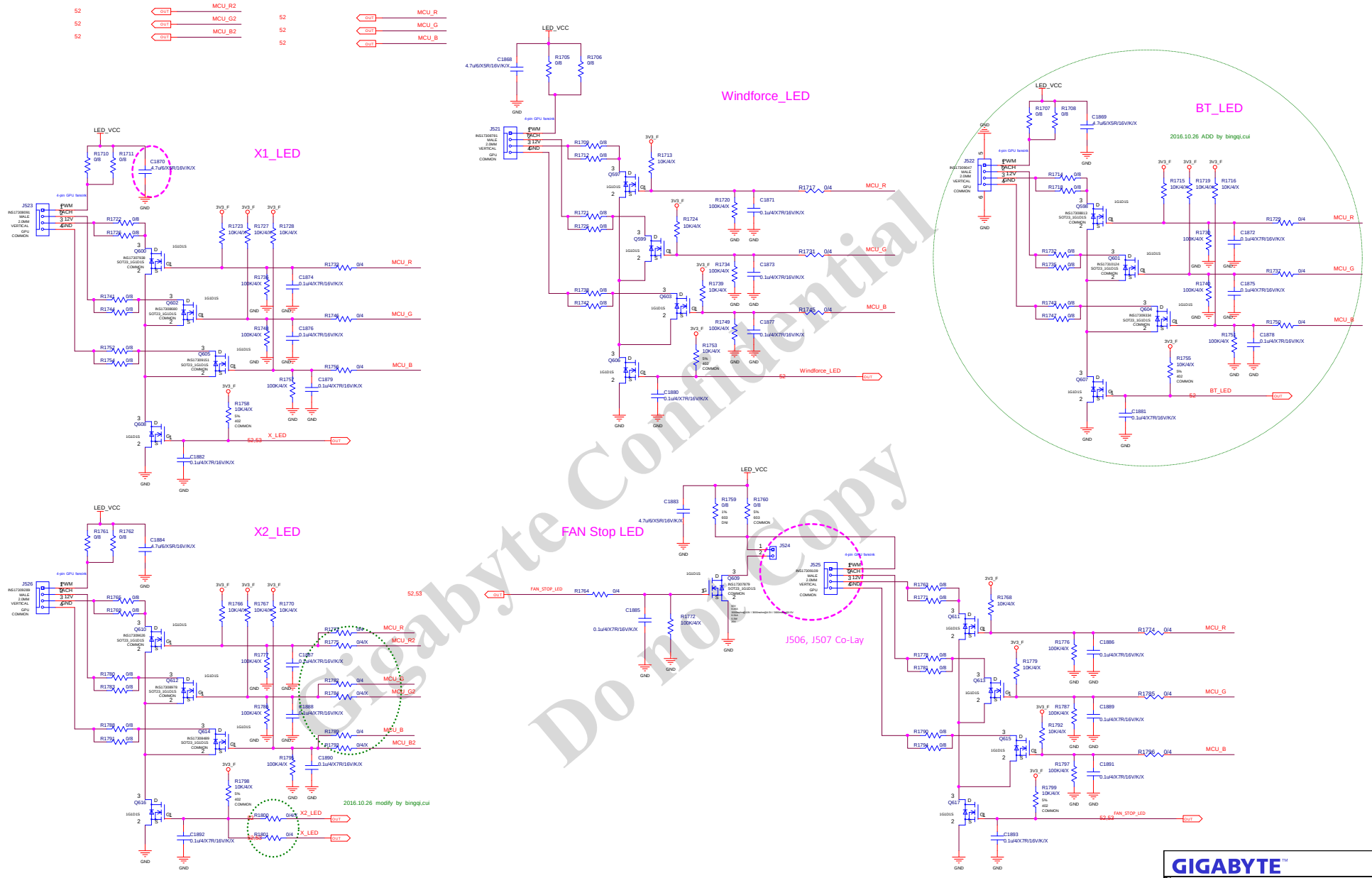

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ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
MECH

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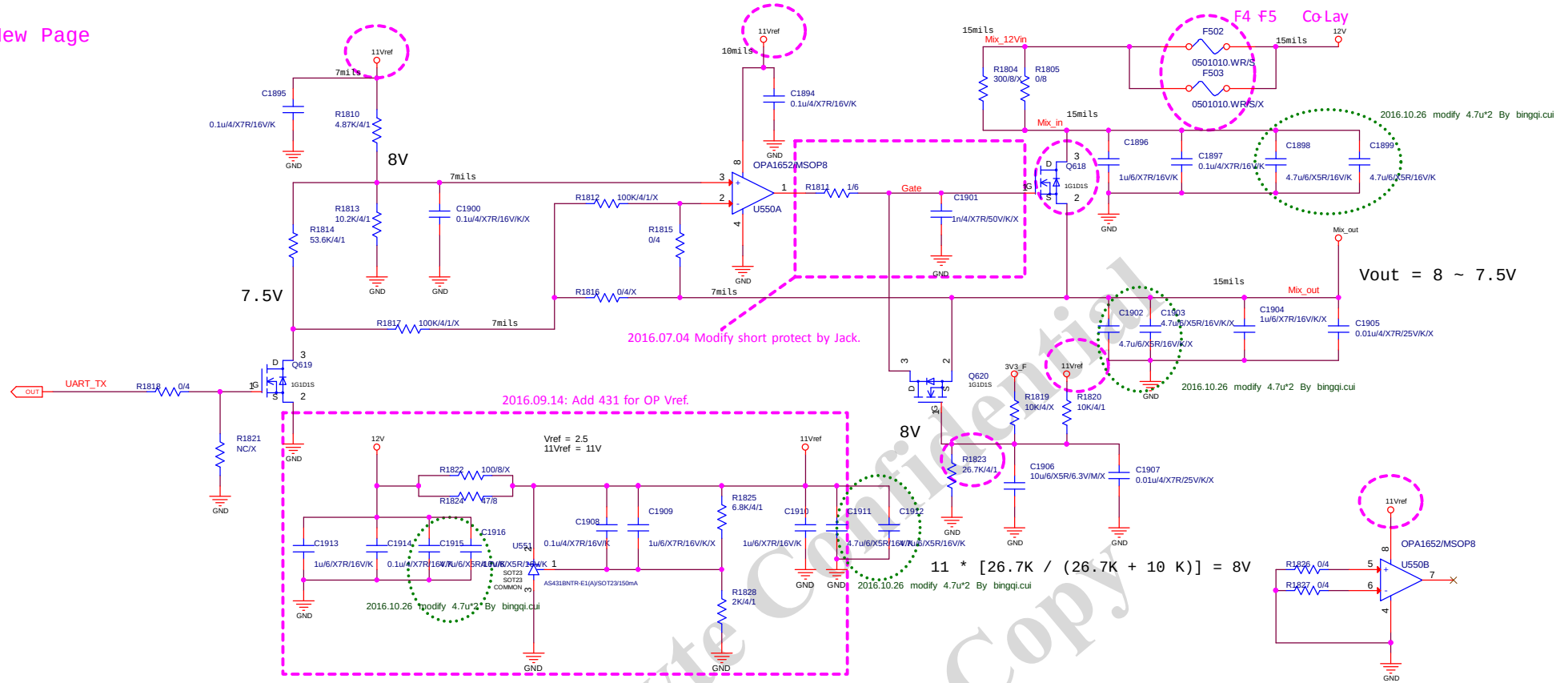
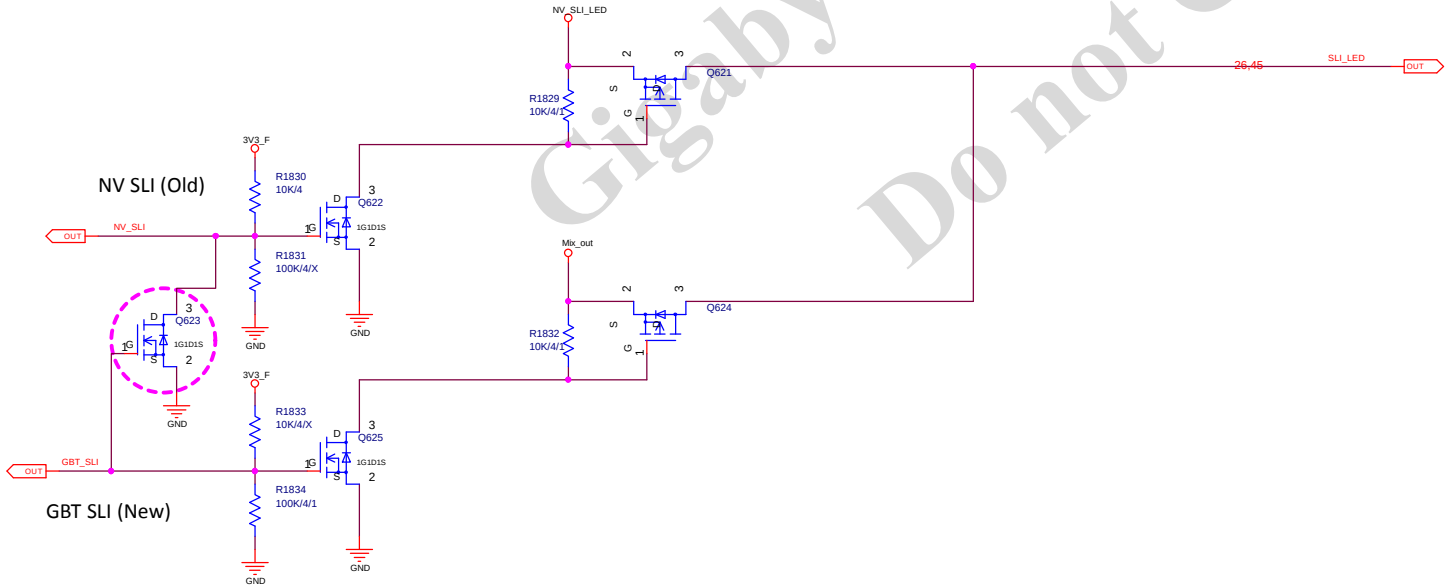
New Page

F4 F5 Co-Lay





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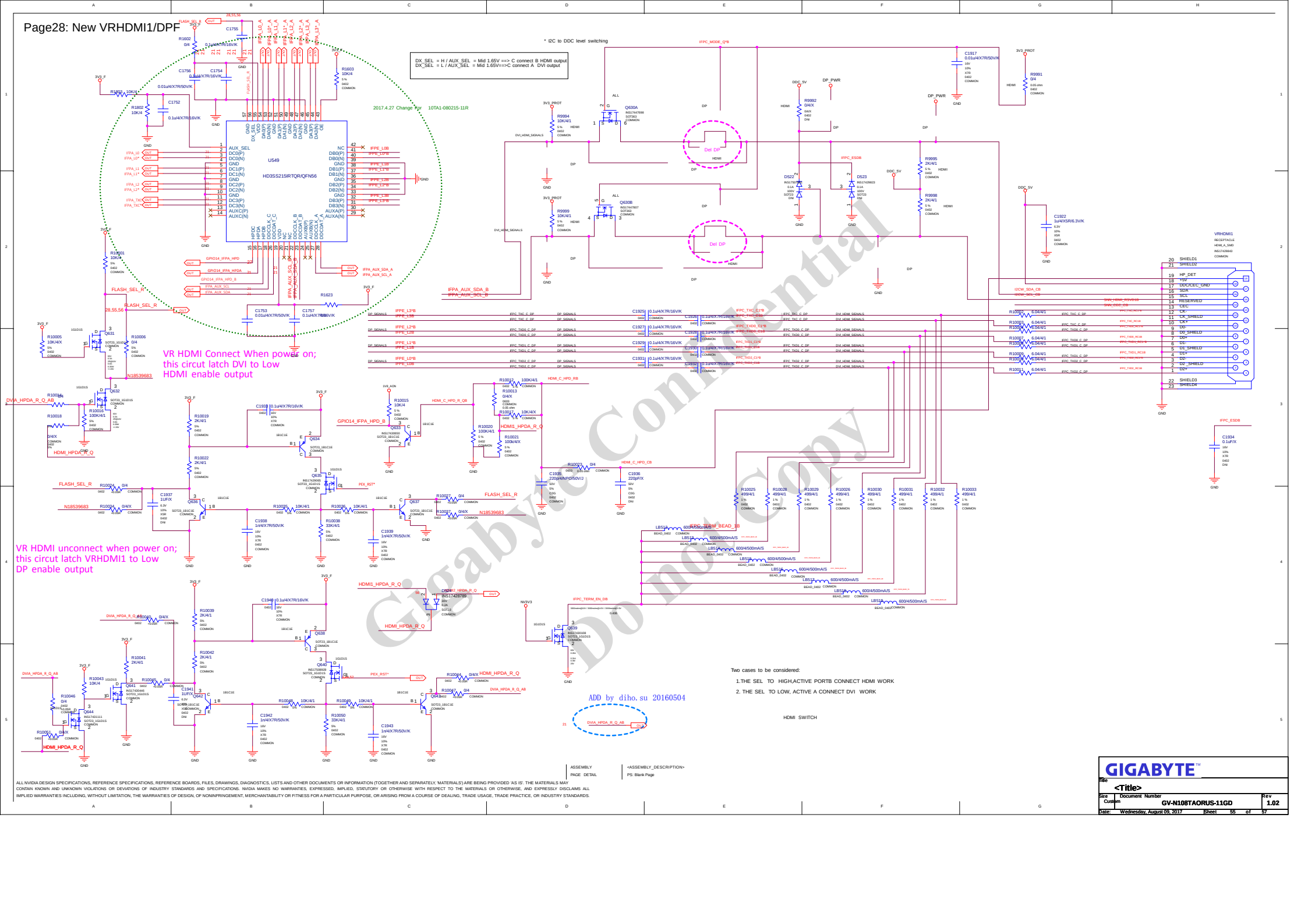
Page28: New VRHDMI1/DPF



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Page31: New VRHDMI2/DPE

DX_SEL/AUX_SEL SET High==>C connect B HDMI output
DX_SEL/AUX_SEL SET Low==>C connect A DP output

2016.04.29 Change for DDC select

2017.4.27 Change for 10TA1-080215-11R

Modify U16&U17 IFPA&IFPB trace by diho.su 20160517

Two cases to be considered:

1.THE SEL TO HIGH,ACTIVE PORTB CONNECT HDMI WORK

2. THE SEL TO LOW, ACTIVE A CONNECT DVI WORK

HDMI SWITCH

* I2C to DDC level switching

FOR ESD DIODES

Place near ESD diodes

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History

Date	Modify
2017.03.01	First version
2017.04.27	Change I/O Switch For 10TA1-080215-11R

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