PG161-A00

TU106 6GB GDDR6, 192b, X16

DVI-D/DP + DP + HDMI

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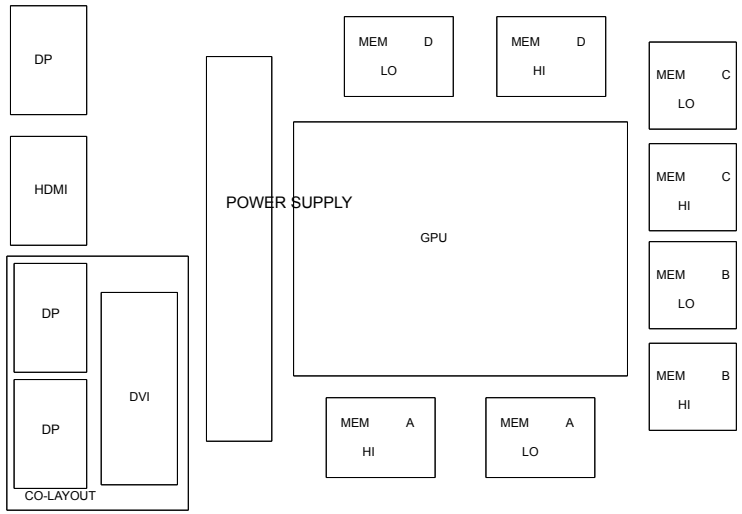
Page2: Block Diagram



Power Supply:

- Power Supply NVVDD-PH6
- Power Supply NVVDD-PH5
- Power Supply NVVDD-PH4
- Power Supply NVVDD-PH3
- Power Supply NVVDD-PH2
- Power Supply NVVDD-PH1
- Power Supply FBVDDQ-PH2
- Power Supply FBVDDQ-PH1
- Power Supply 5V
- PEX_VDD
- 1V8
- Fan
- DP_PWR

EXT_12V 2x4 PWR

PEX_12V Finger

3V3 Finger

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Block Diagram

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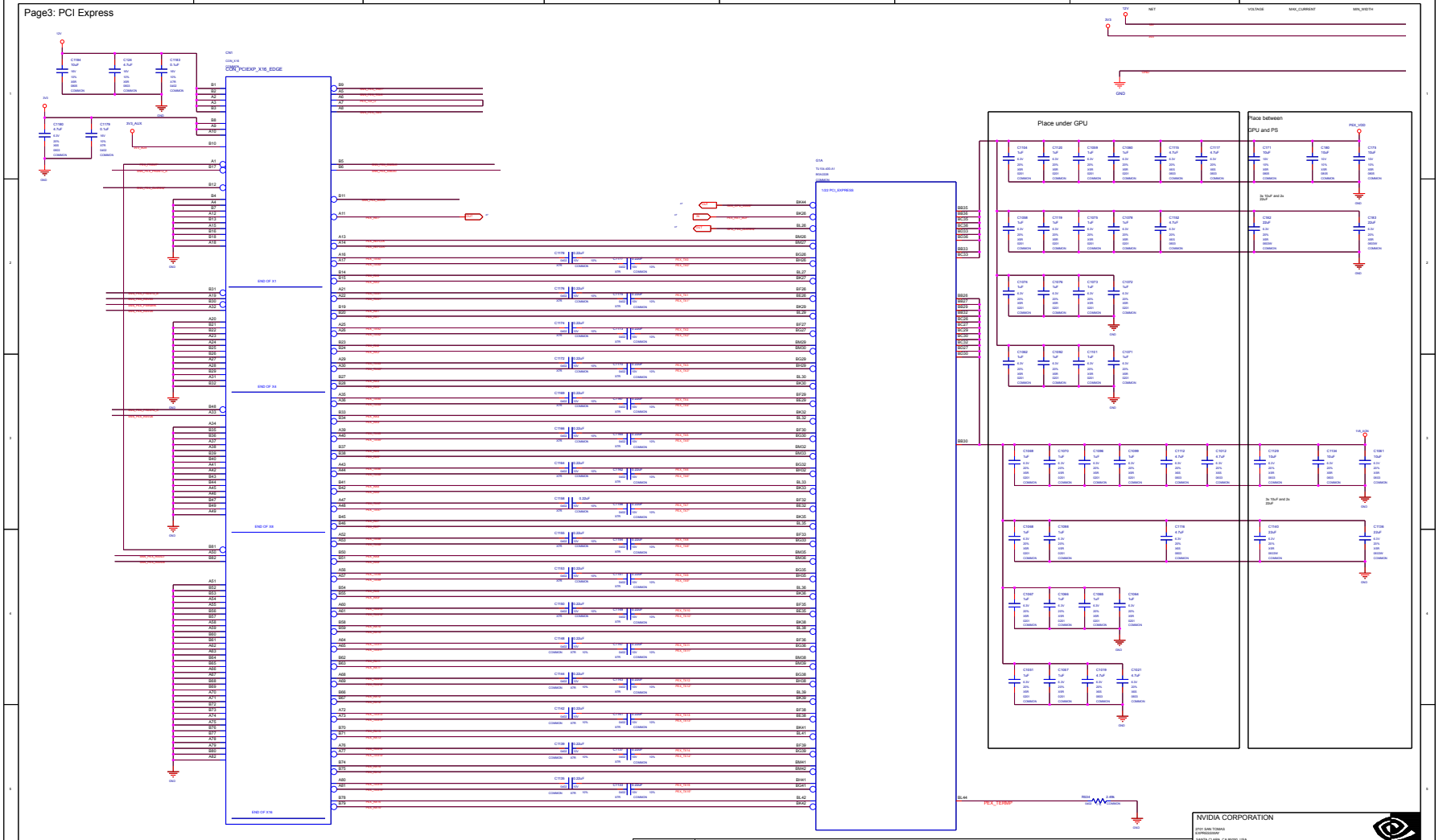
Page3: PCI Express



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
3V3			
GND			

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI Express

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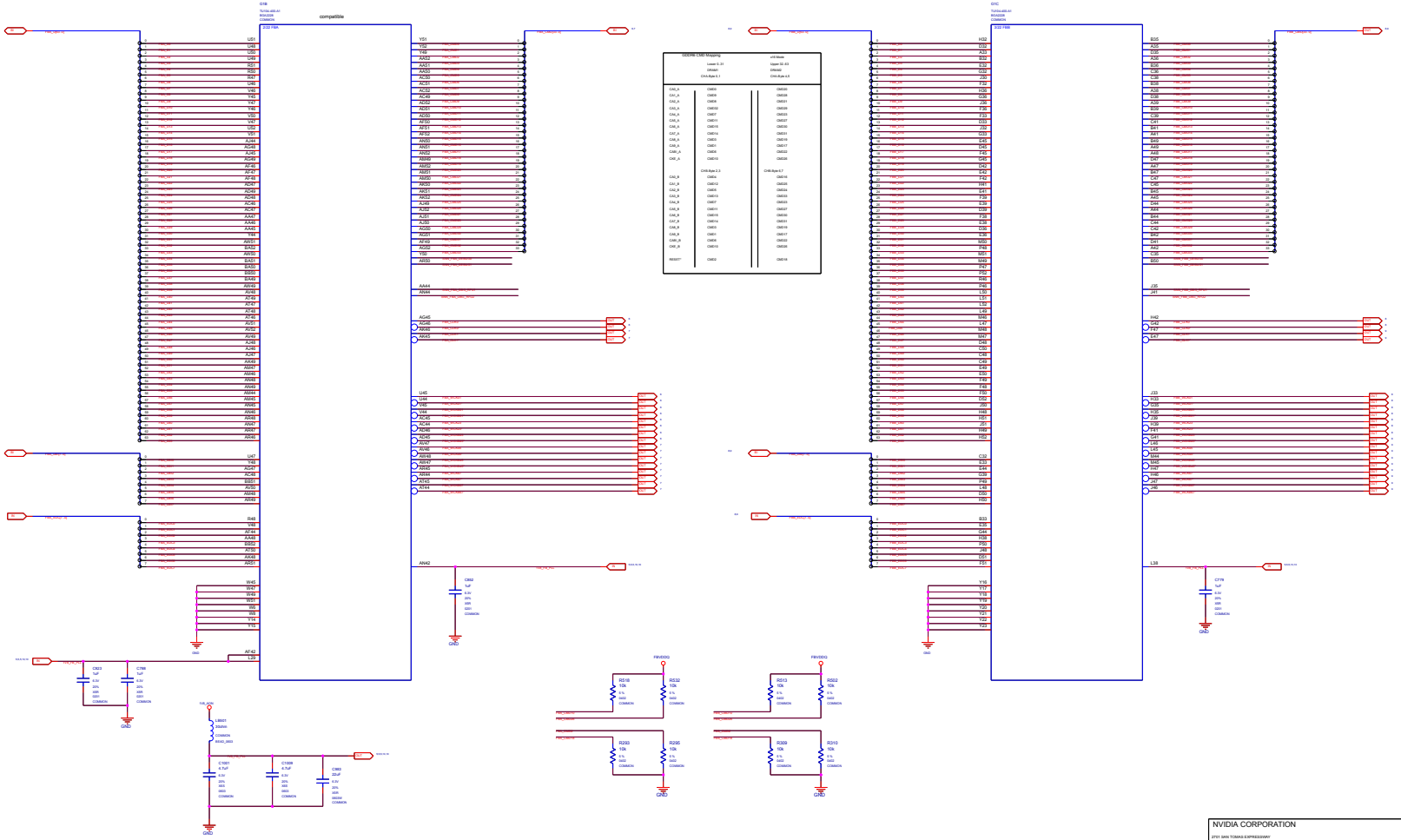
Page5: MEMORY: GPU Partition A/B



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: GPU FB_A/B

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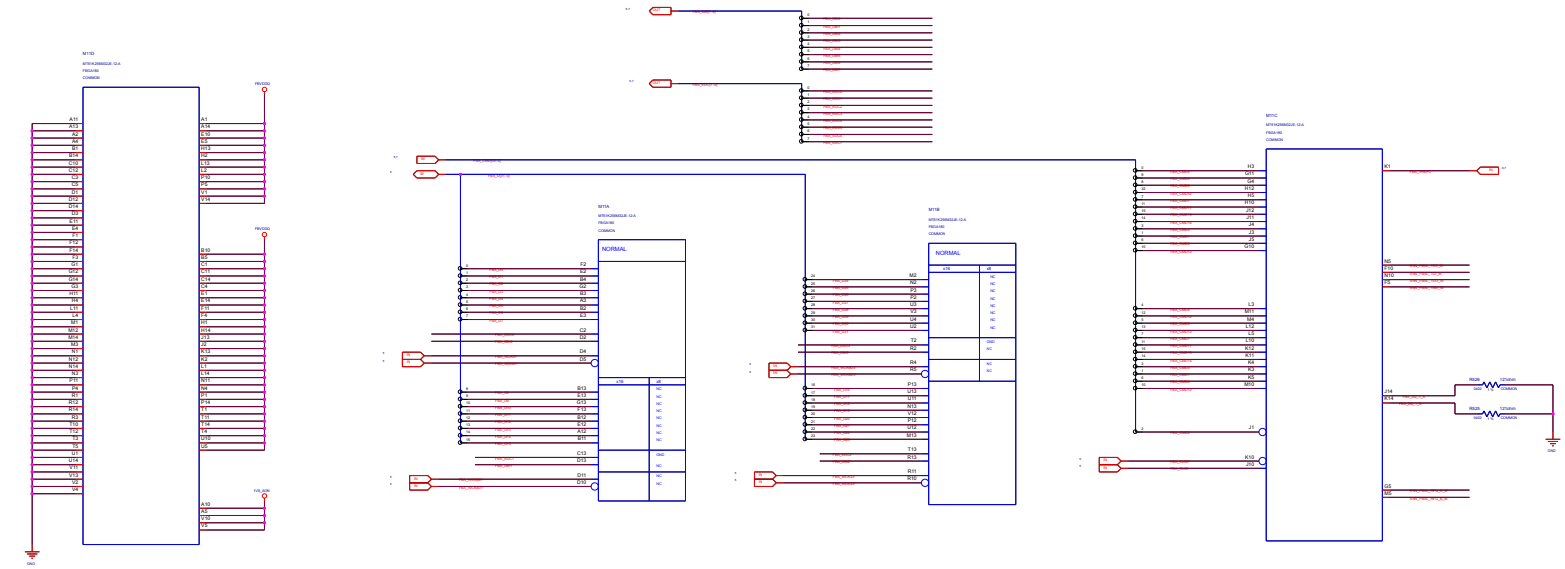
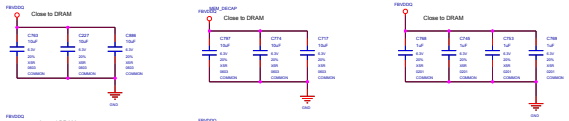
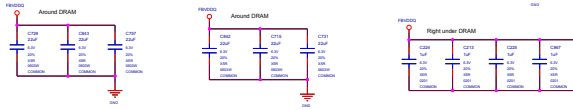
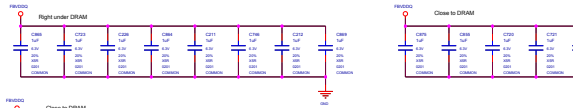
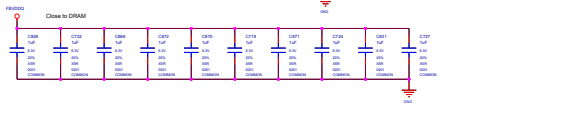
Page6: MEMORY: FBA Partition 31..0



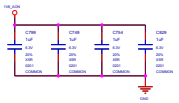








VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R106



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PAGE DETAIL	MEMORY: FBA[31:0]

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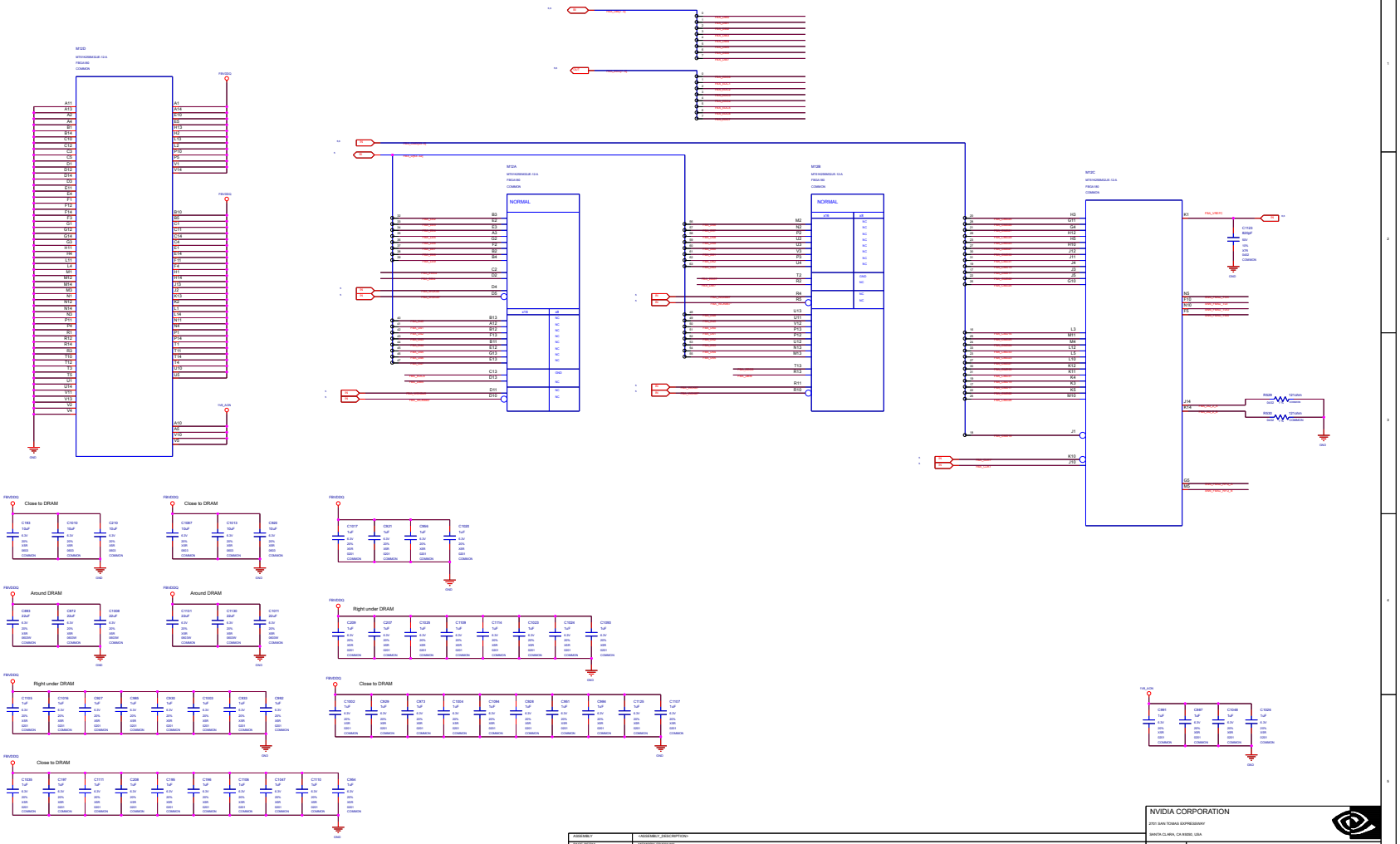
Page7: MEMORY: FBA Partition 63..32



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PAGE DETAIL	MEMORY: FBA[63:32]

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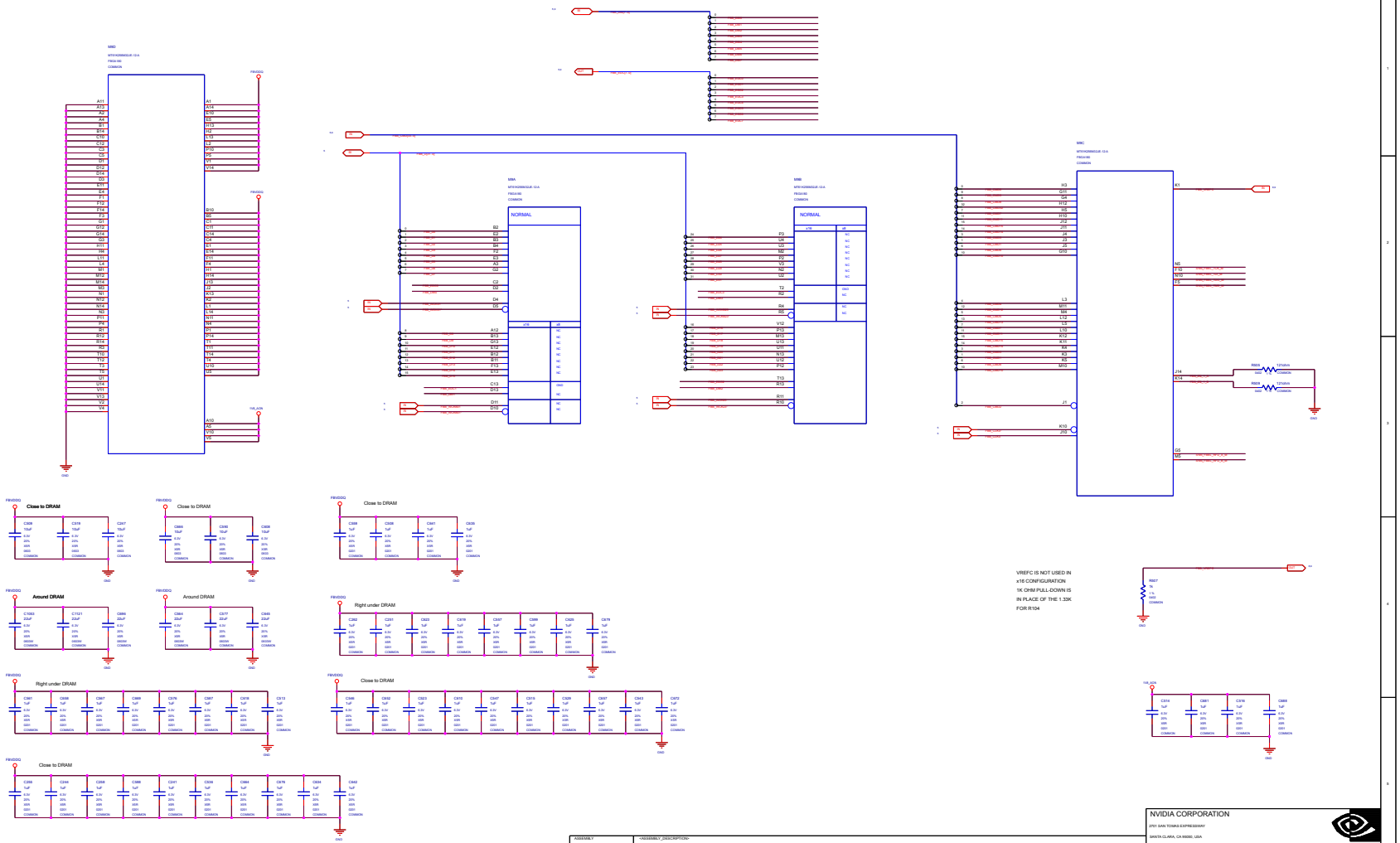
Page8: MEMORY: FBB Partition 31..0



ASSEMBLY	"ASSEMBLY_DESCRIPTION"
PAGE DETAIL	MEMORY: FBB[31:0]

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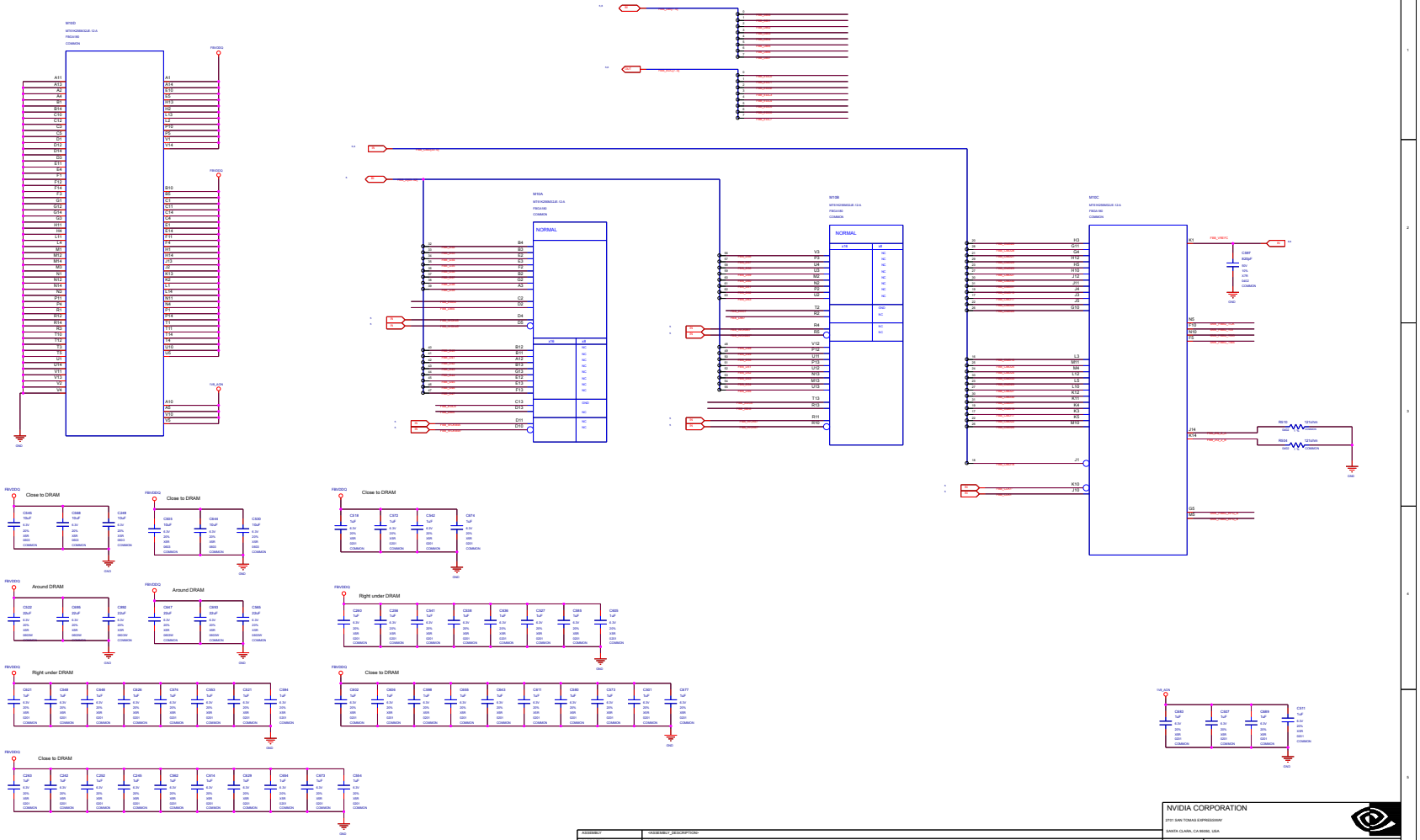
Page9: MEMORY: FBB Partition 63..32



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB[63:32]

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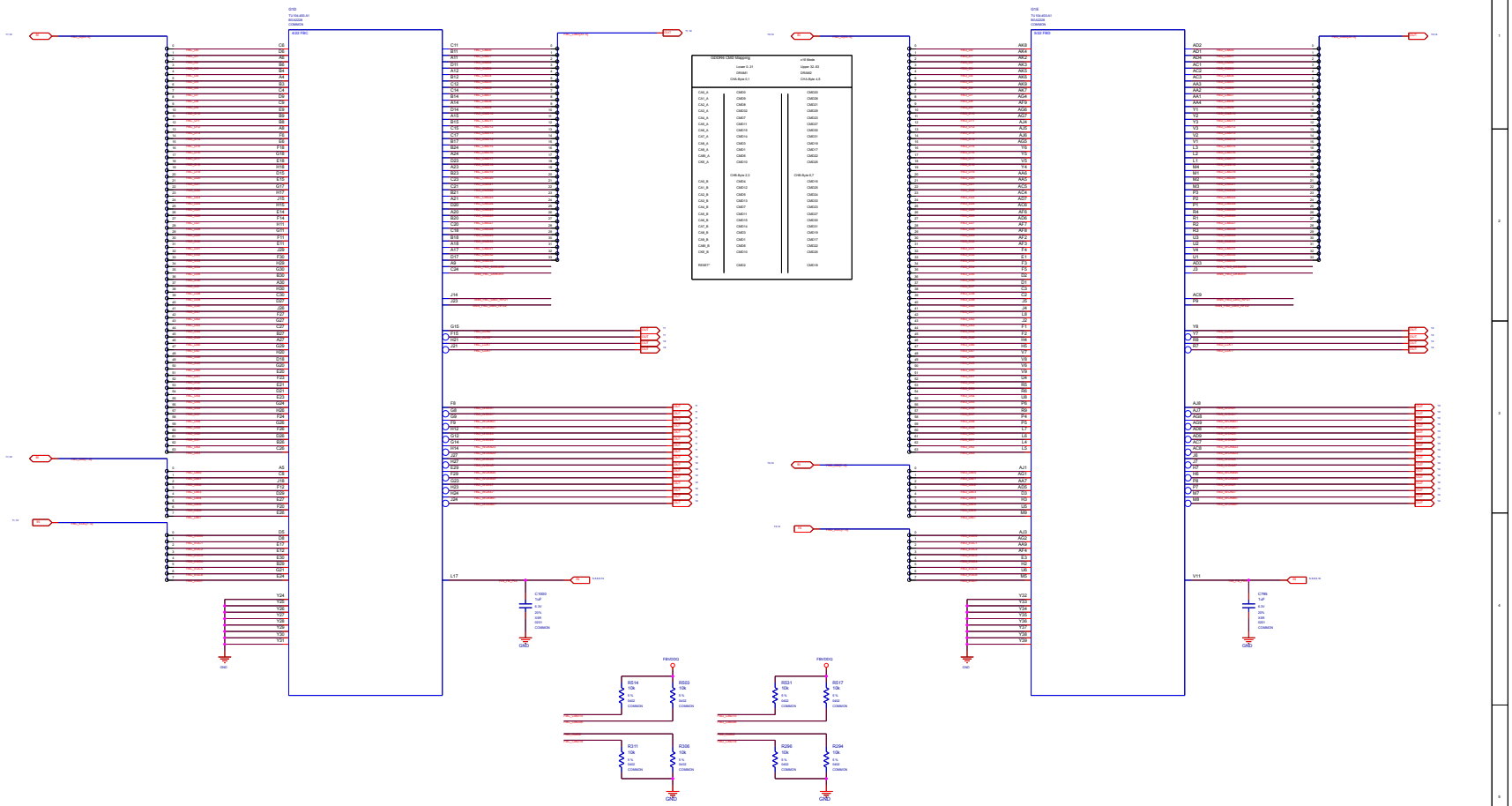
Page10: MEMORY: GPU Partition C/D



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: GPU FB_C/D

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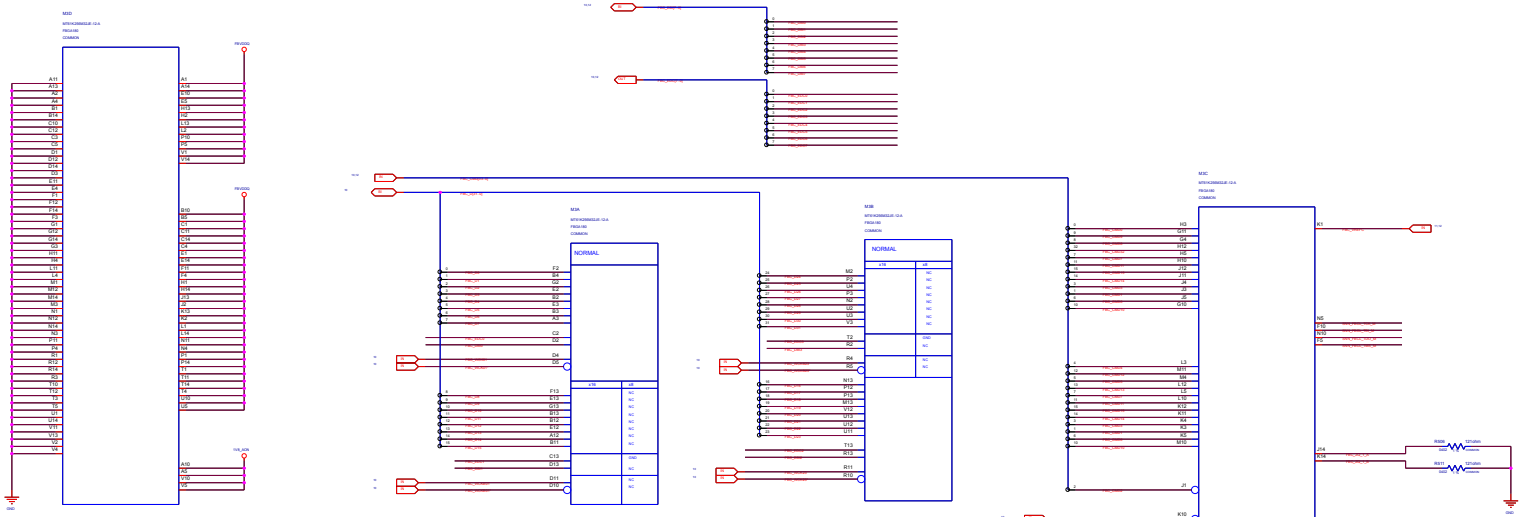
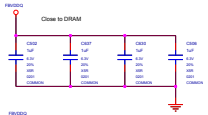
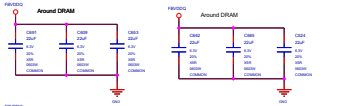
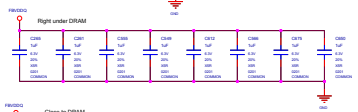
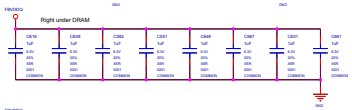
Page11: MEMORY: FBC Partition 31..0

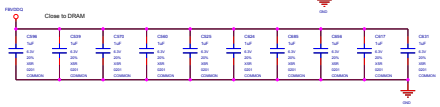


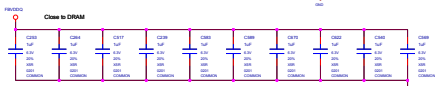




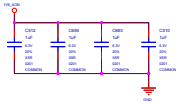








VREFC IS NOT USED IN x16 CONFIGURATION 1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R75



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBC[31:0]

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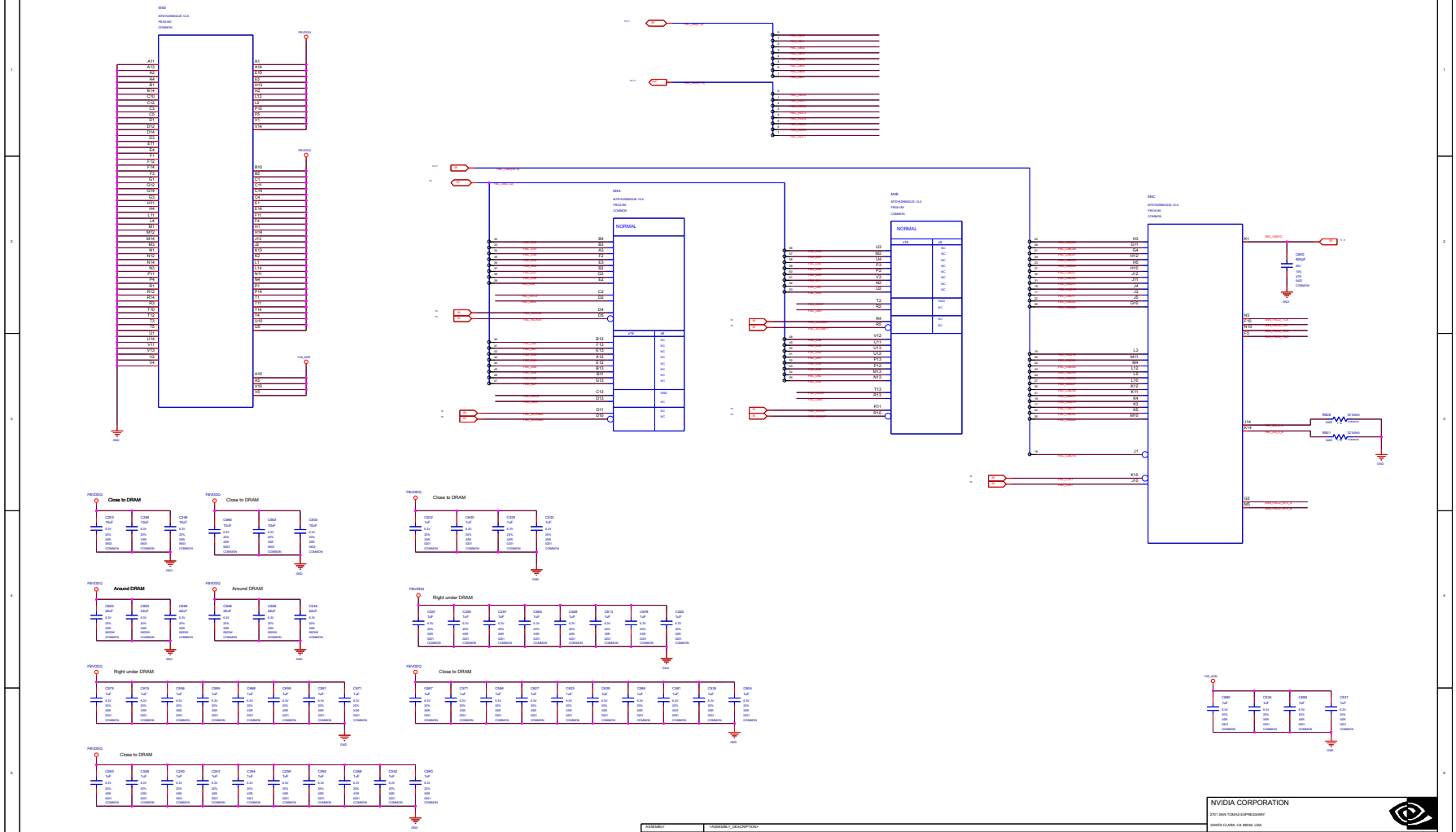
Page12: MEMORY: FBC Partition 63..32



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBC[64:32]

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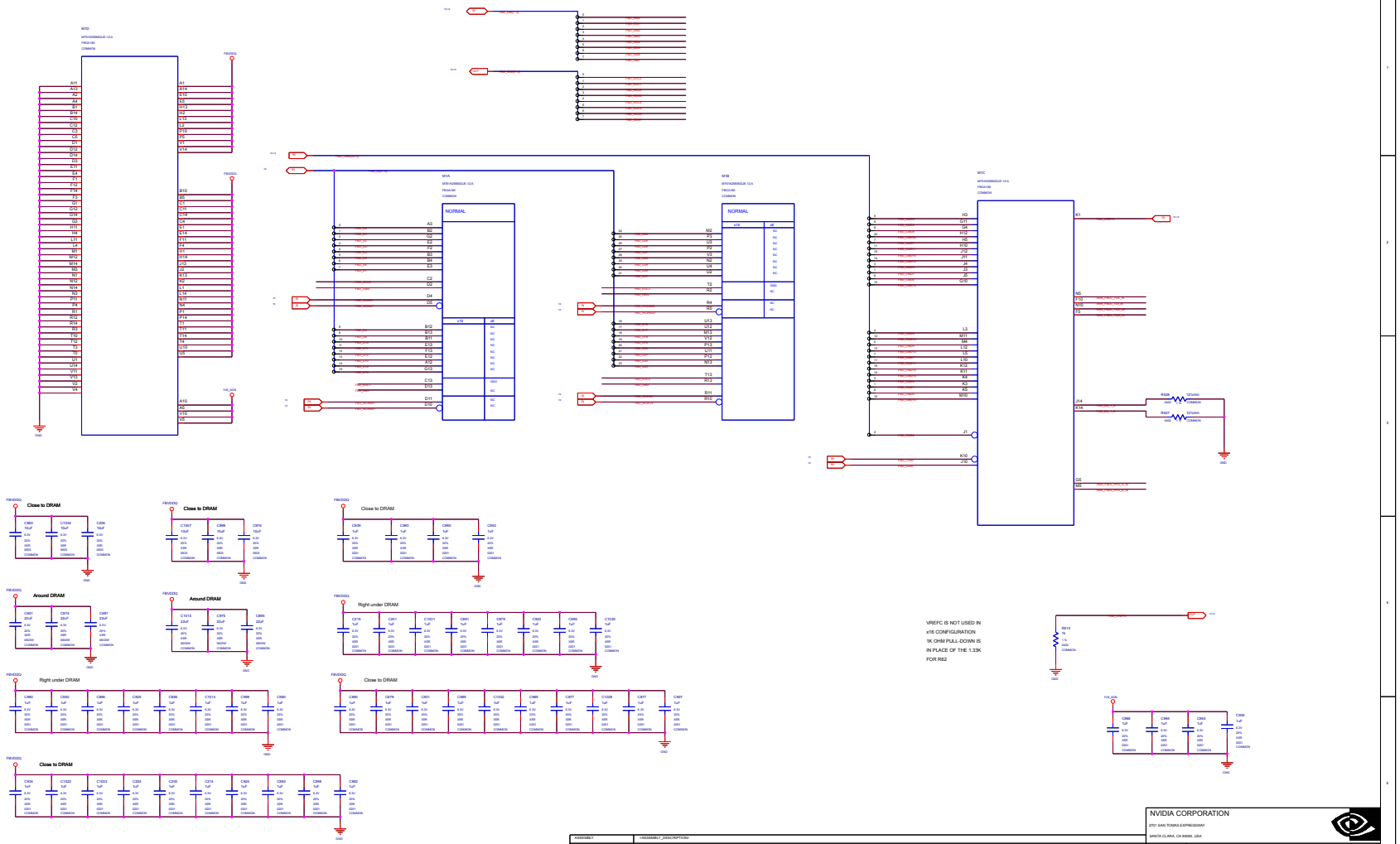
Page13: MEMORY: FBD Partition 31..0



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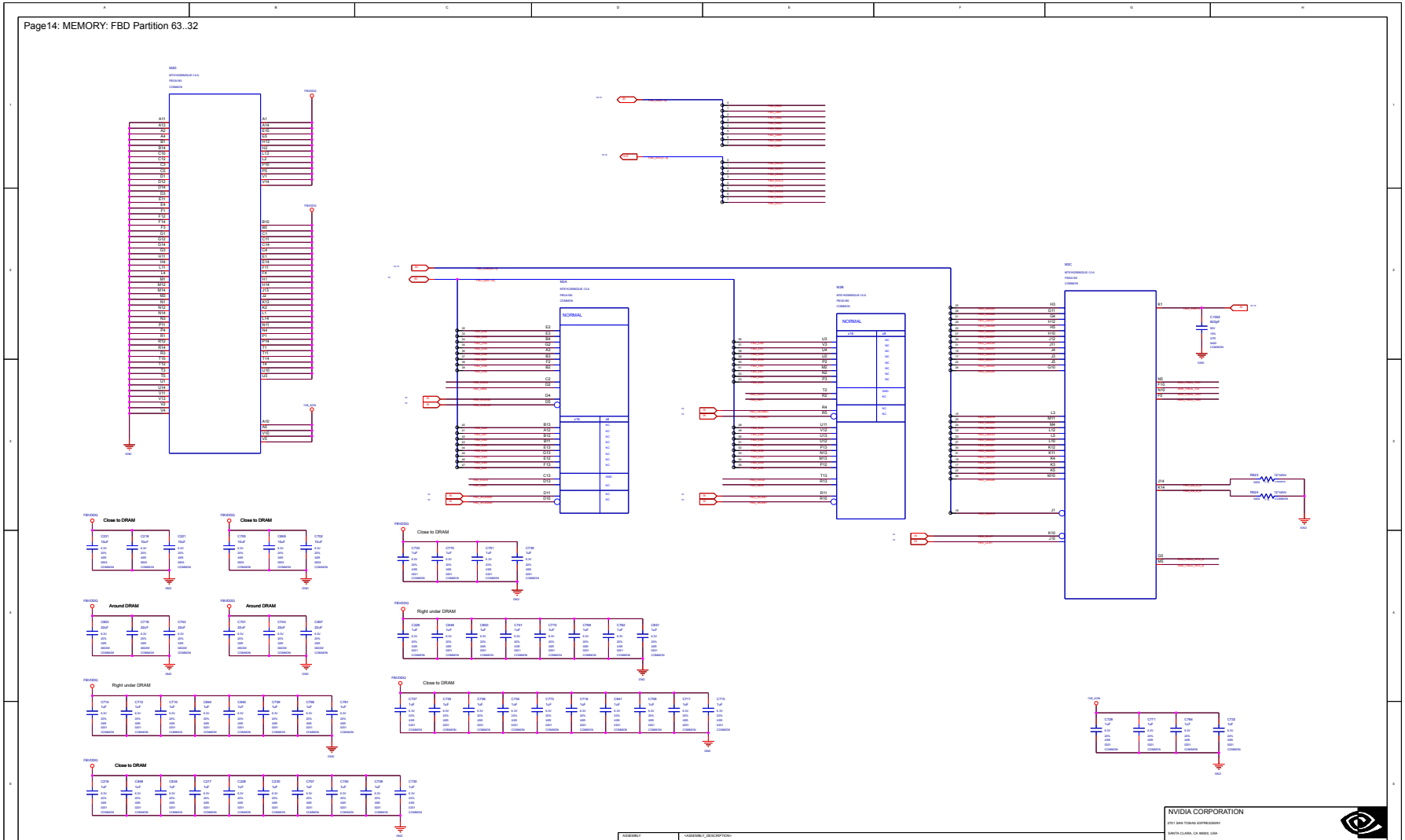
Page14: MEMORY: FBD Partition 63..32



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ASSEMBLY: <ASSEMBLY_DESCRIPTION>
PAGE DETAIL: MEMORY: FBD[63:32]

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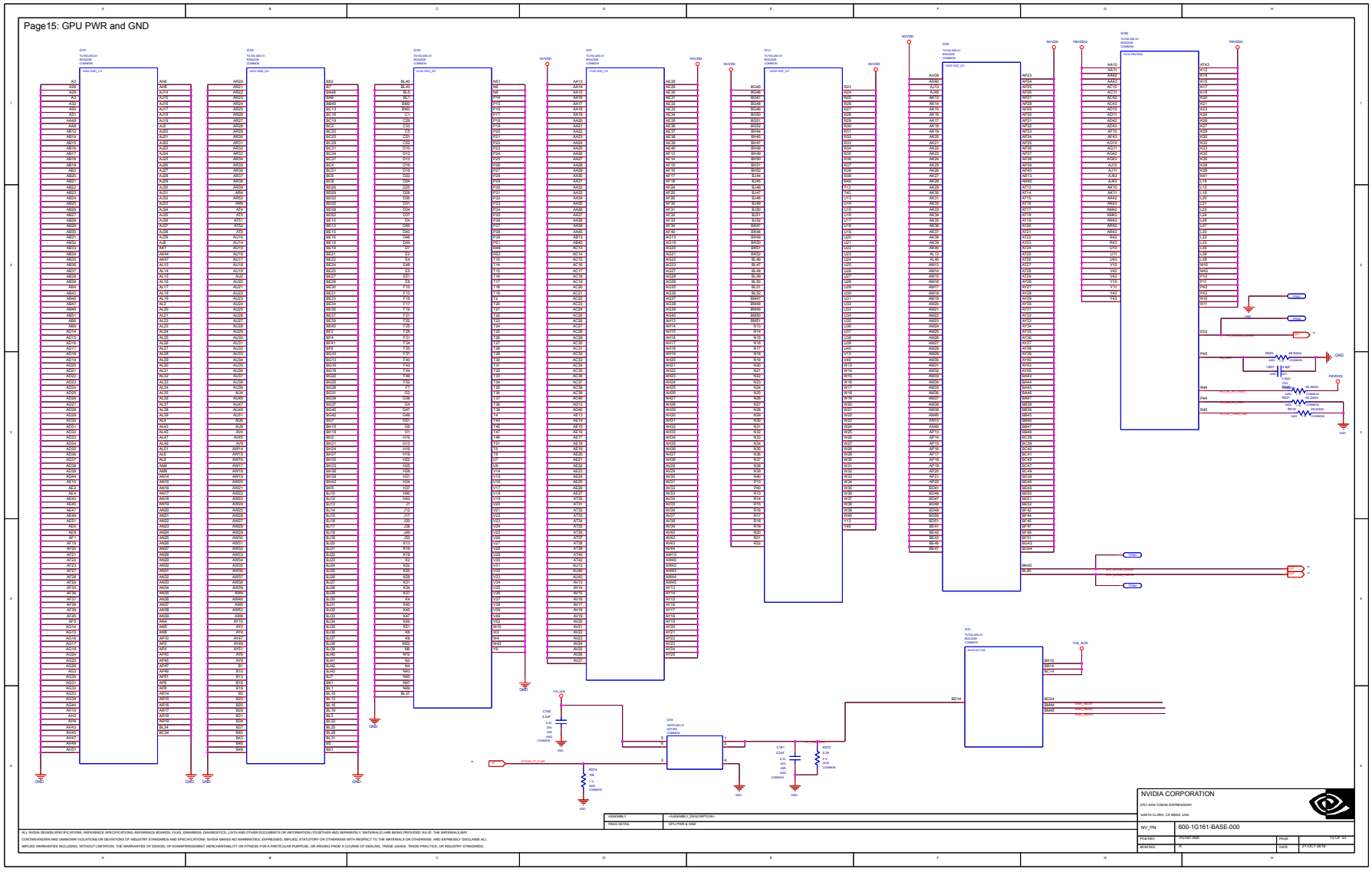
Page15: GPU PWR and GND



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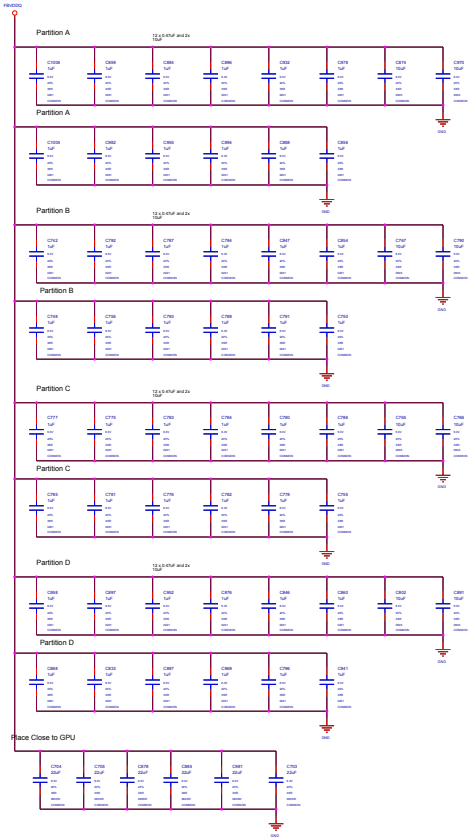
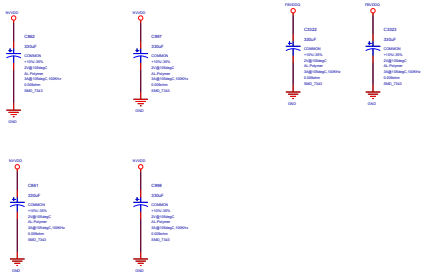
Page16: GPU Decoupling 1

FBVDDQ



NVVDD



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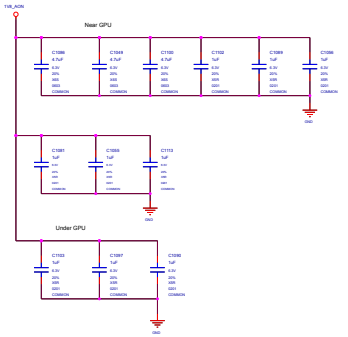

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU Decoupling

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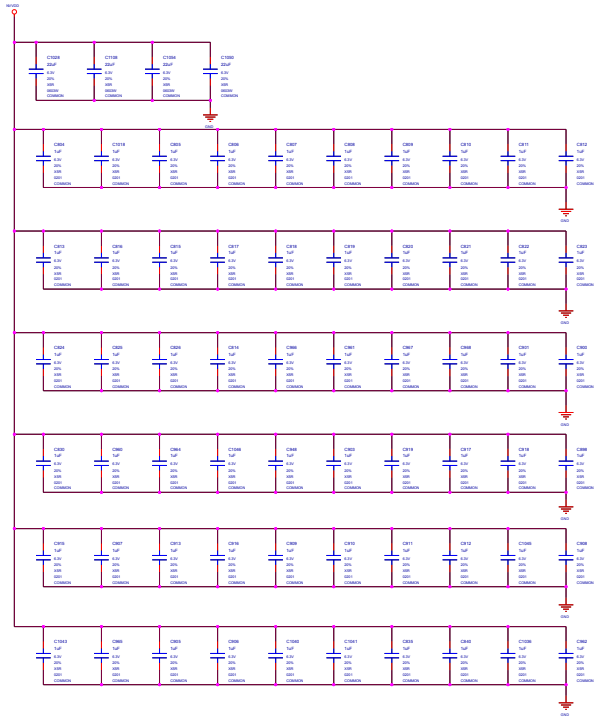
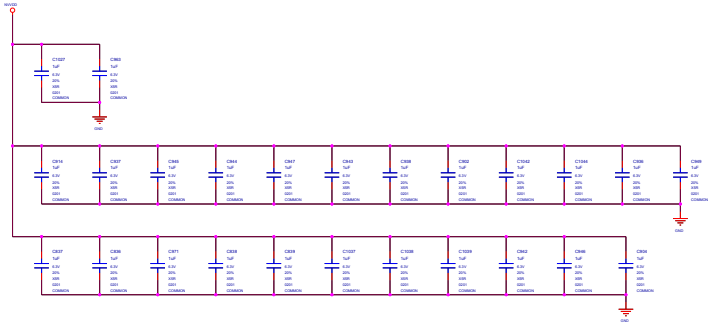
Page17: GPU Decoupling 2

NVVDD





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PAGE DETAIL	GPU Decoupling2

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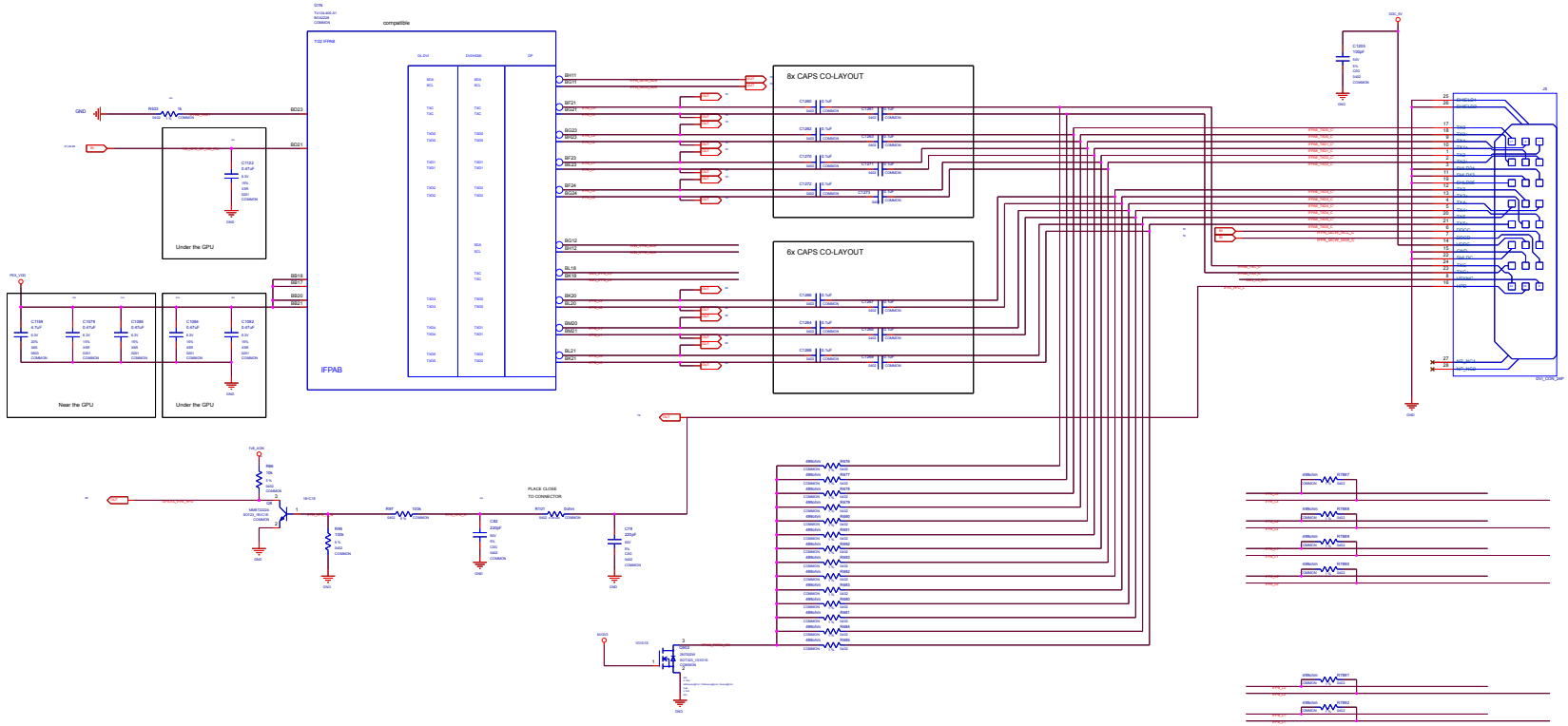
IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



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PAGE DETAIL	02: IFPAB DVI-D-DL

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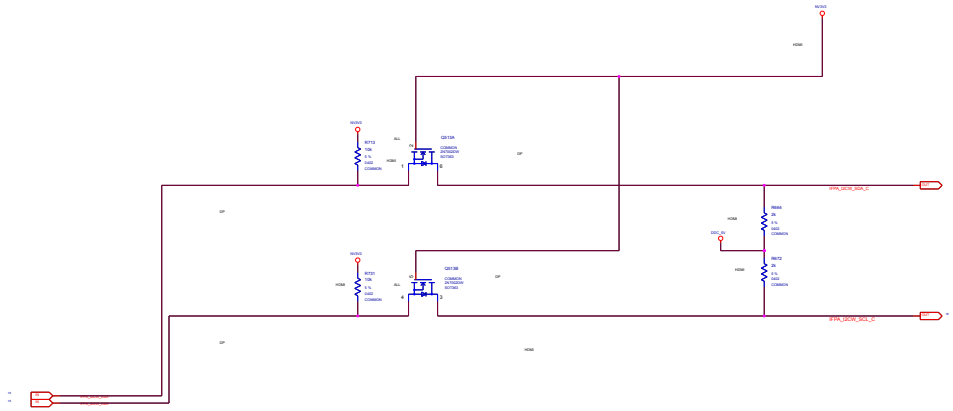
Page19: IFPA DP



IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	ID: IFPA DP

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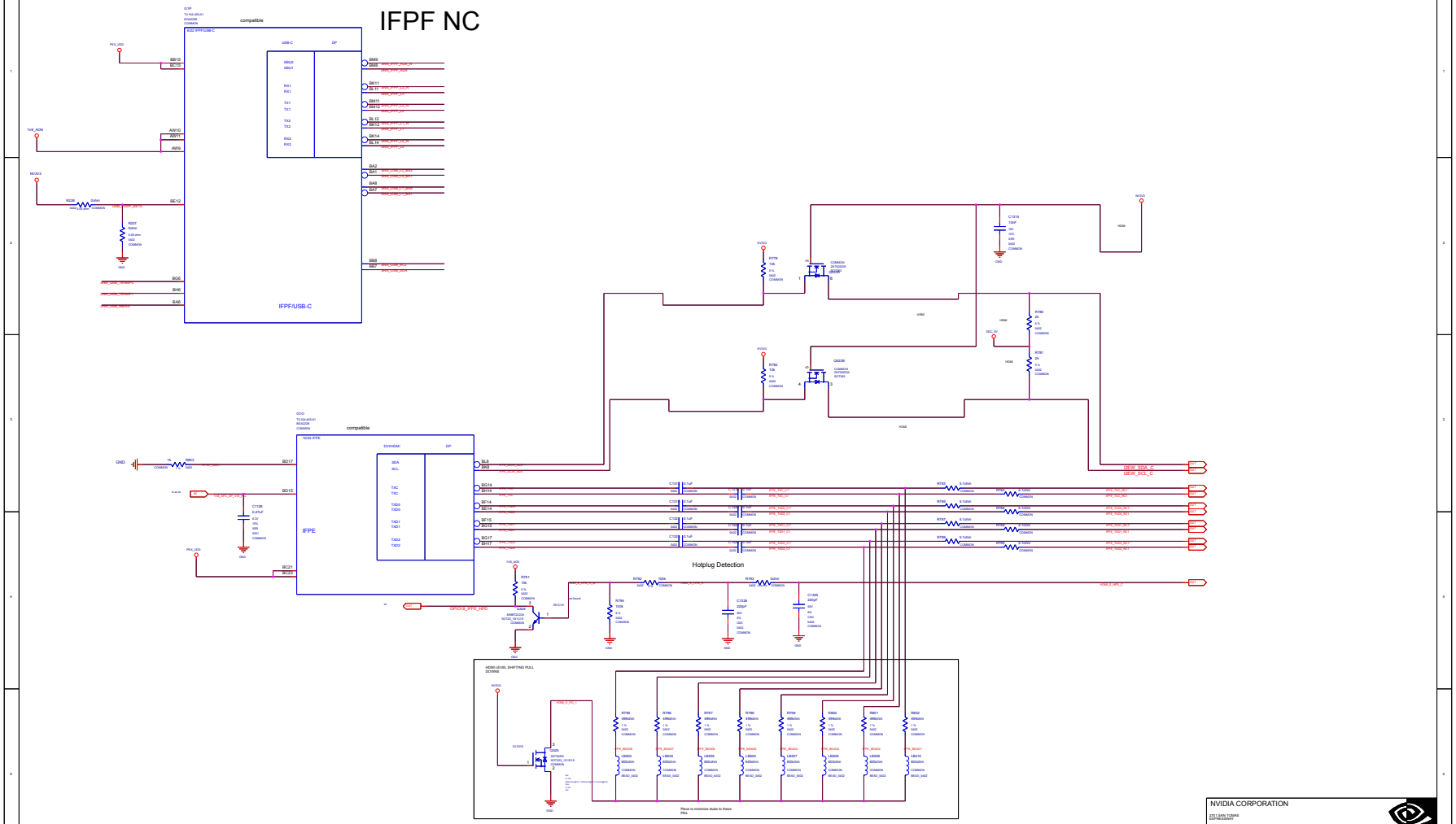
Page20: IFPE & IFPF USB-C NC

IFPF NC



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PNSS DETAIL	

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IO: IFPE & IFPF USBC NC

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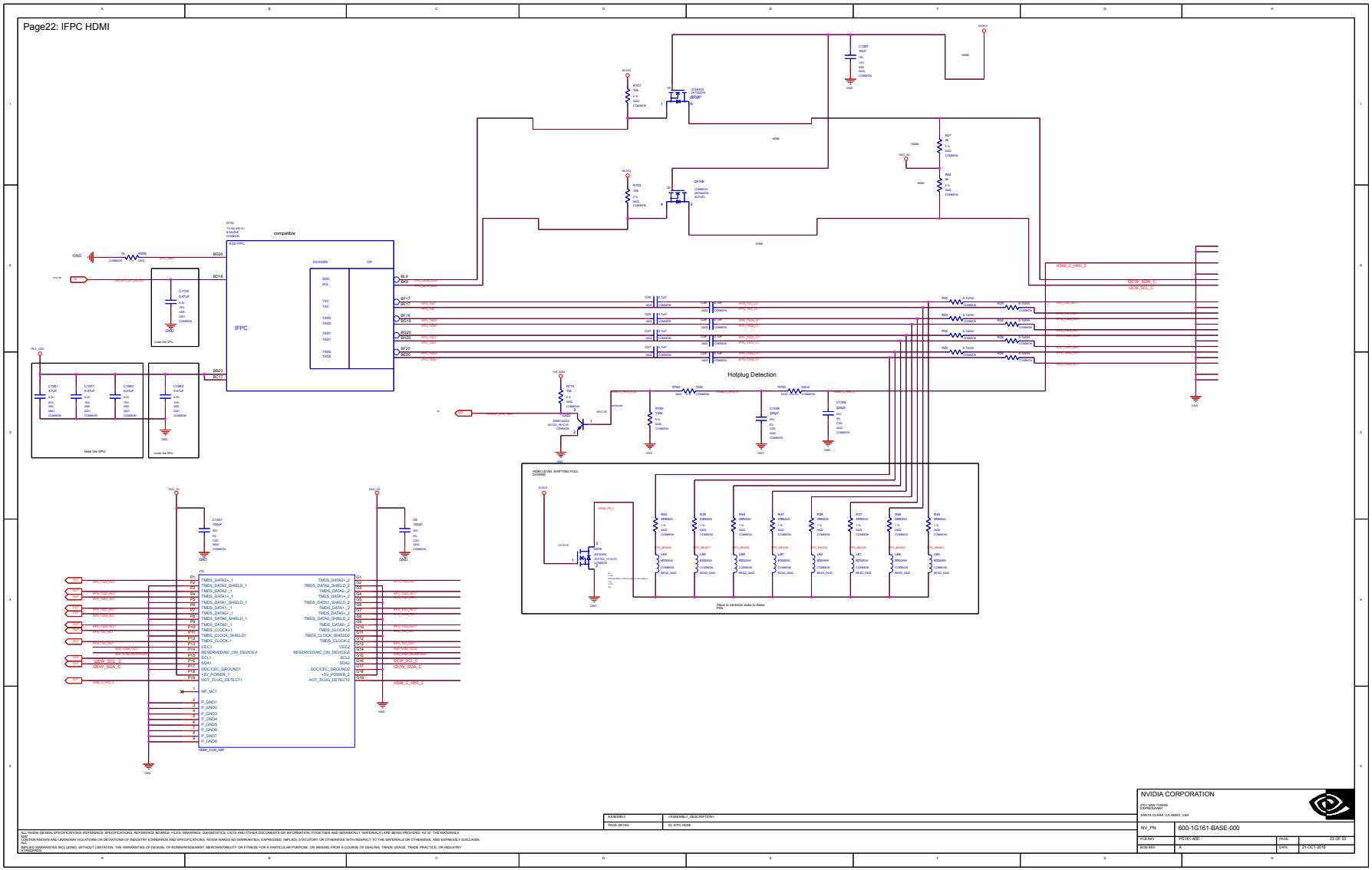
Page22: IFPC HDMI
IFPC
compatible
Hotplug Detection
HDMI LEVEL SHIFTING PULL DOWNS
HDMI_CON_SMP
NVIDIA CORPORATION
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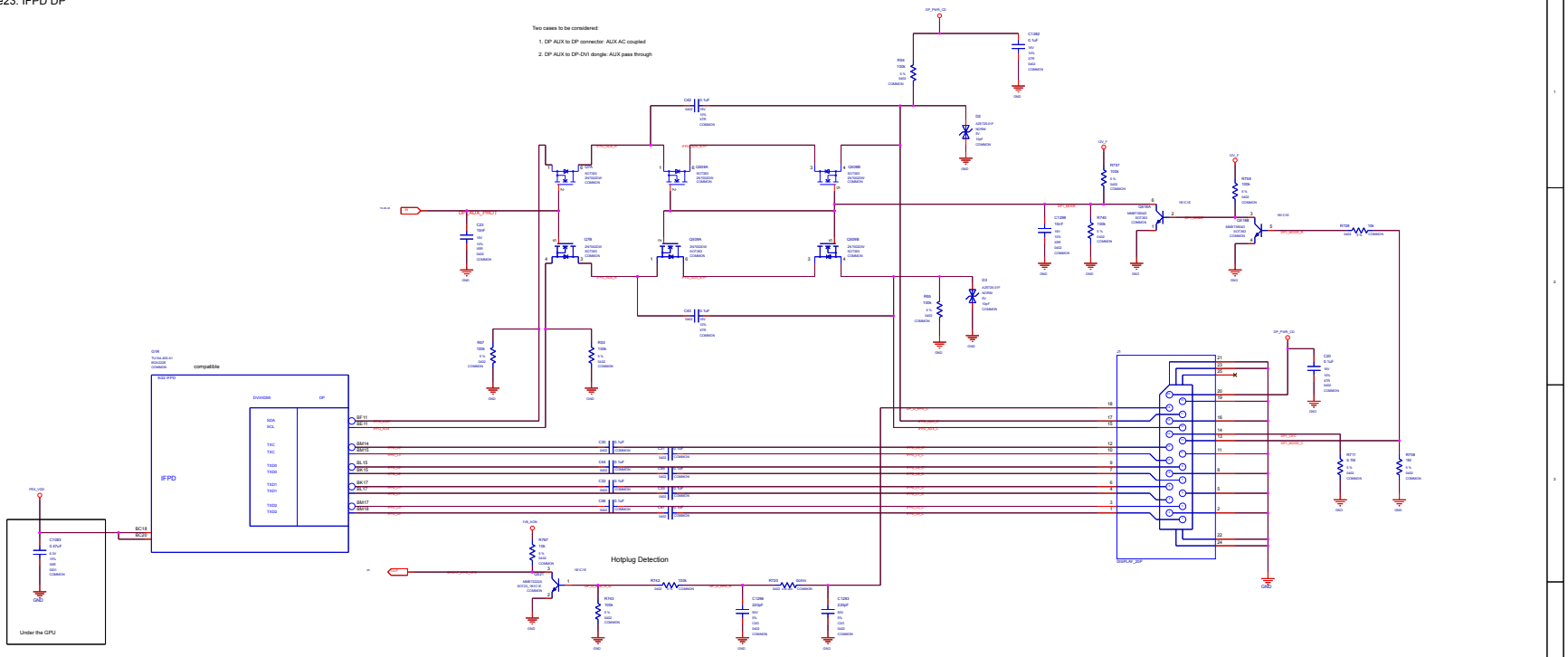
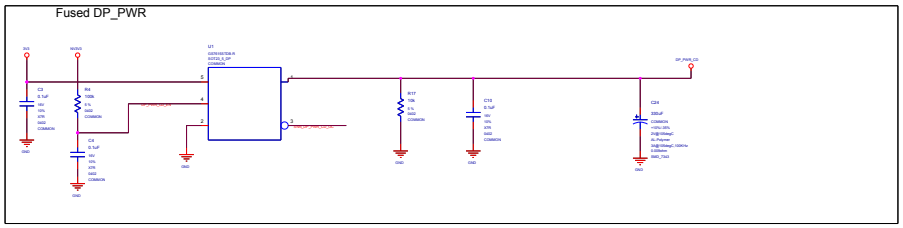
Page23: IFPD DP



Fused DP_PWR



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	12: IFPD DP

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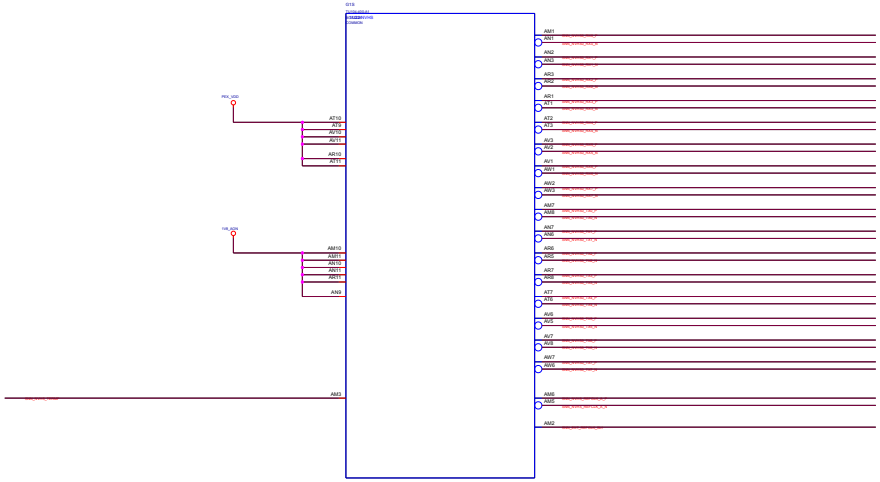
Page24: NVHS Interface and Frame Lock



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO NVHS Interface and Frame Lock

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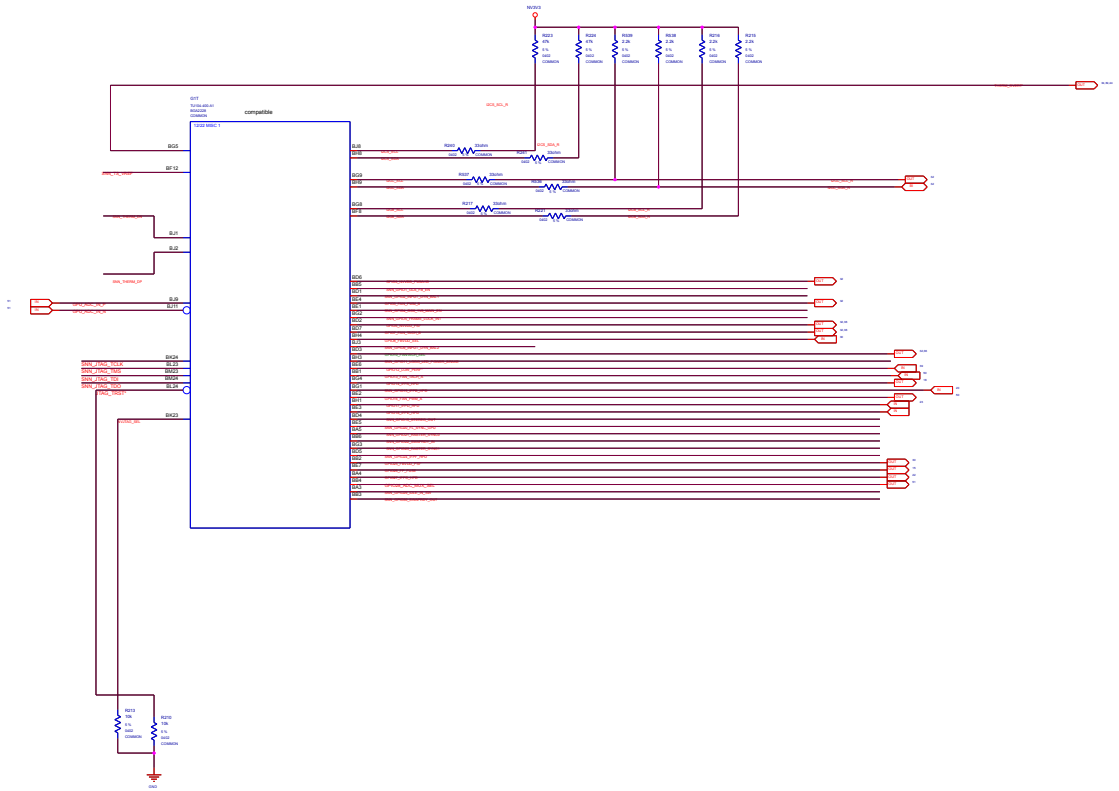
Page25: MISC1: Fan, Thermal, JTAG, GPIO



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: Thermal, JTAG, GPIO,3.0/SMBUS

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Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT		
				1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V

M=Middle:Tied to 0.9V

L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE

0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND

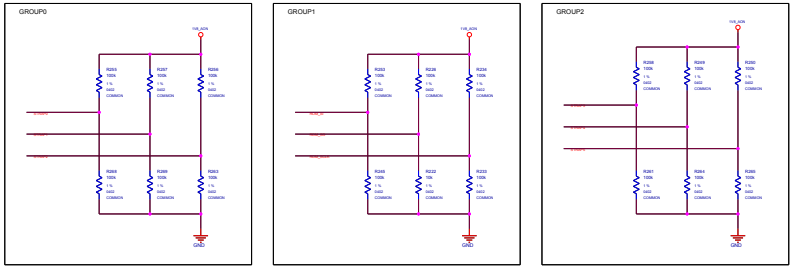
0:DEVID_SEL ORIGNAL

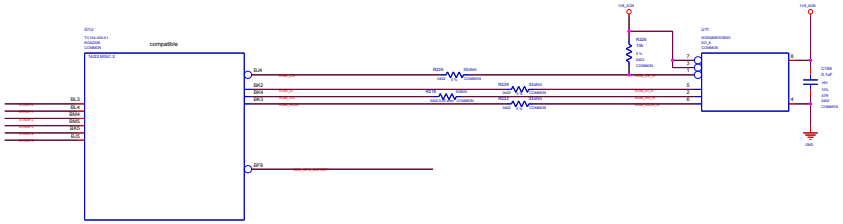
1:PCIE_CFG LOW POWER

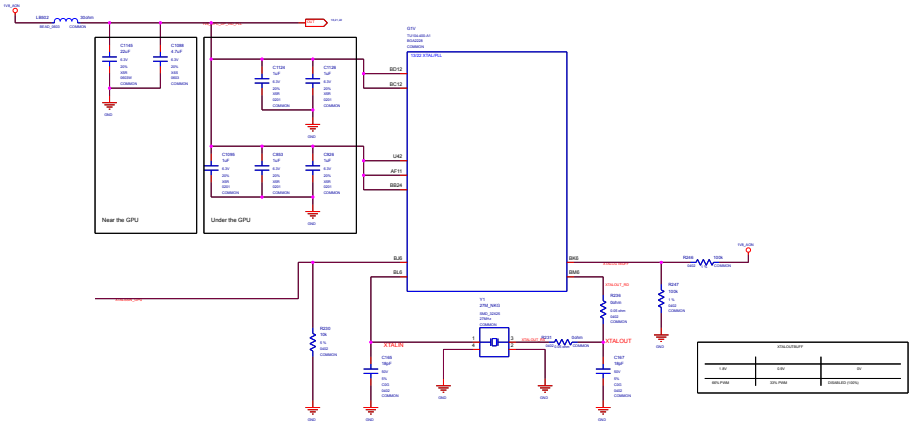
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE

0:VGA_DEVICE DISABLE







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PAGE DETAIL	MISC2 ROM, XTAL,STRAPS

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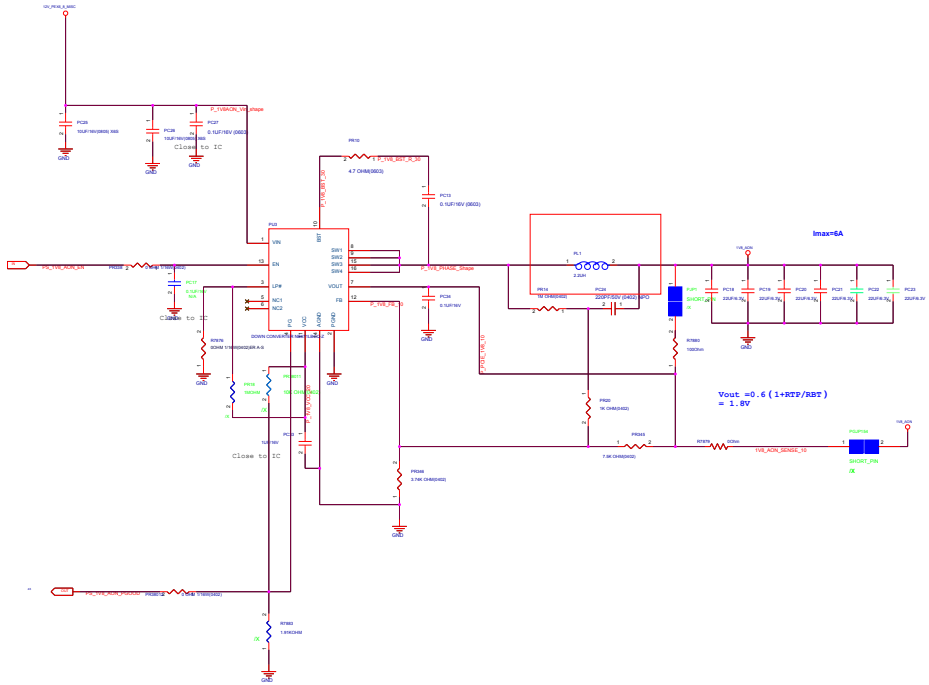
Page27: PS: 1V8_AON



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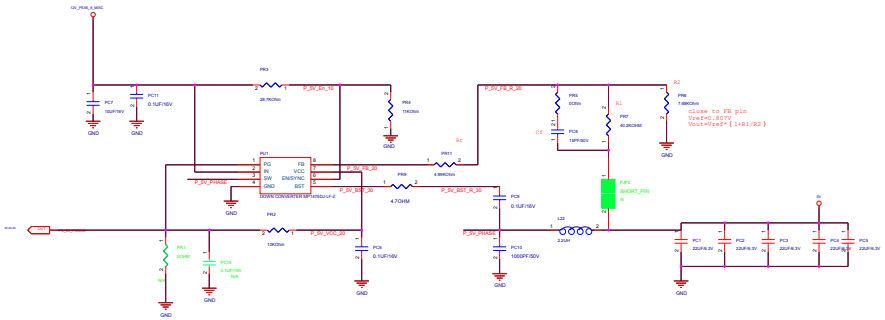
Page28: PS: 5V



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PAGE DETAIL	PS: 5V

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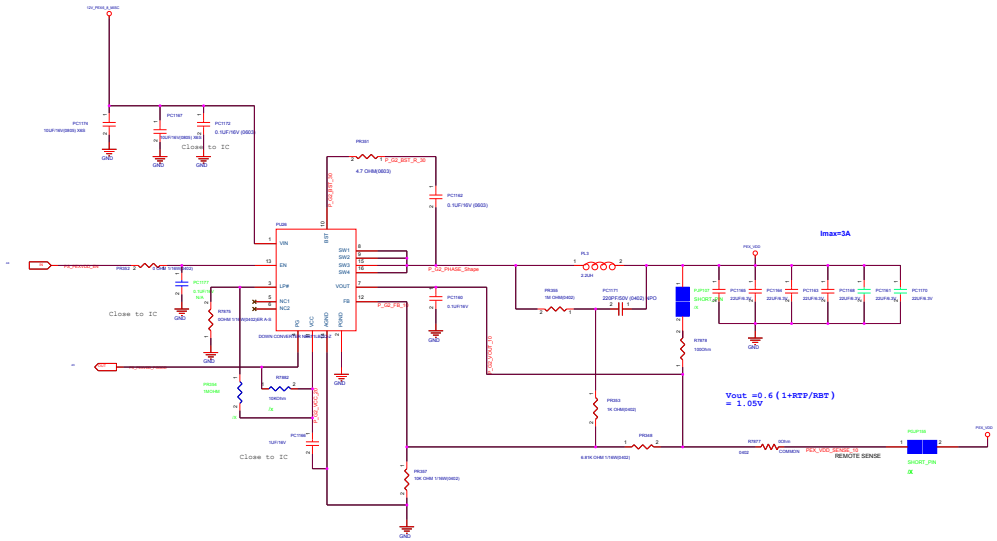
Page29: PS: PEXVDD



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PAGE DETAIL	PS: PEXVDD

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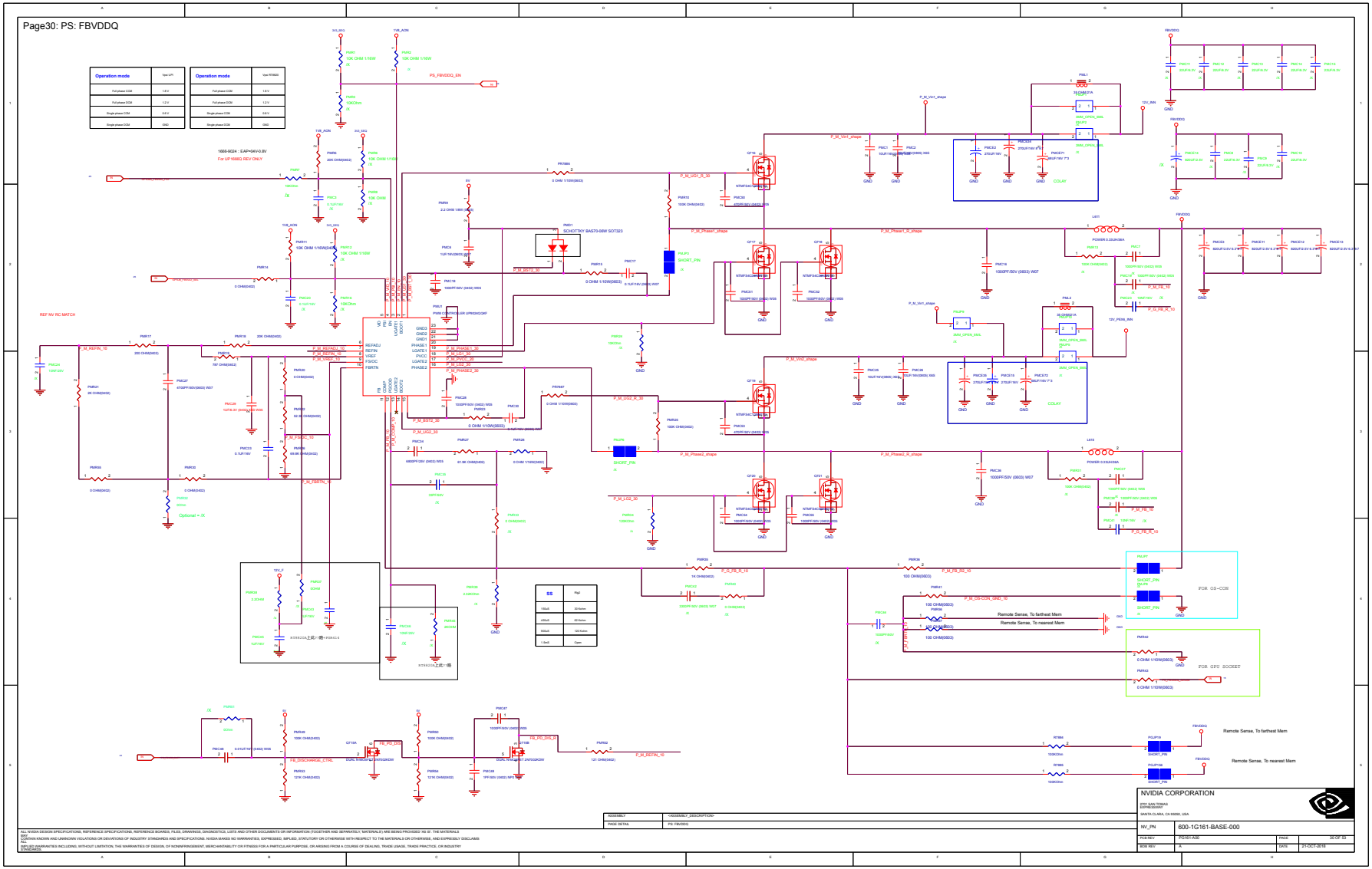
Page30: PS: FBVDDQ
Operation mode
Vpwr UP1
Full phase CCM
1.8 V
Full phase DCM
1.2 V
Single phase CCM
0.6 V
Single phase DCM
GND
Operation mode
Vpwr RTX6O
Full phase CCM
1.8 V
Full phase DCM
1.2 V
Single phase CCM
0.6 V
Single phase DCM
GND
1668-0024 : EAP=04V-0.8V
For UP1668J REV ONLY
REF NV RC MATCH
PS_FBVDDQ_EN
FBVDDQ
12V_INN
12V_PERIL_INN
COLAY
FOR GS-CON
FOR GPU SOCKET
Remote Sense, To farthest Mem
Remote Sense, To nearest Mem
Optional = 0X
SS
50µA
100uA
200uA
300uA
1.0mA
82.5kohm
42.5kohm
125kohm
Open
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PAGE DETAIL
PS: FBVDDQ
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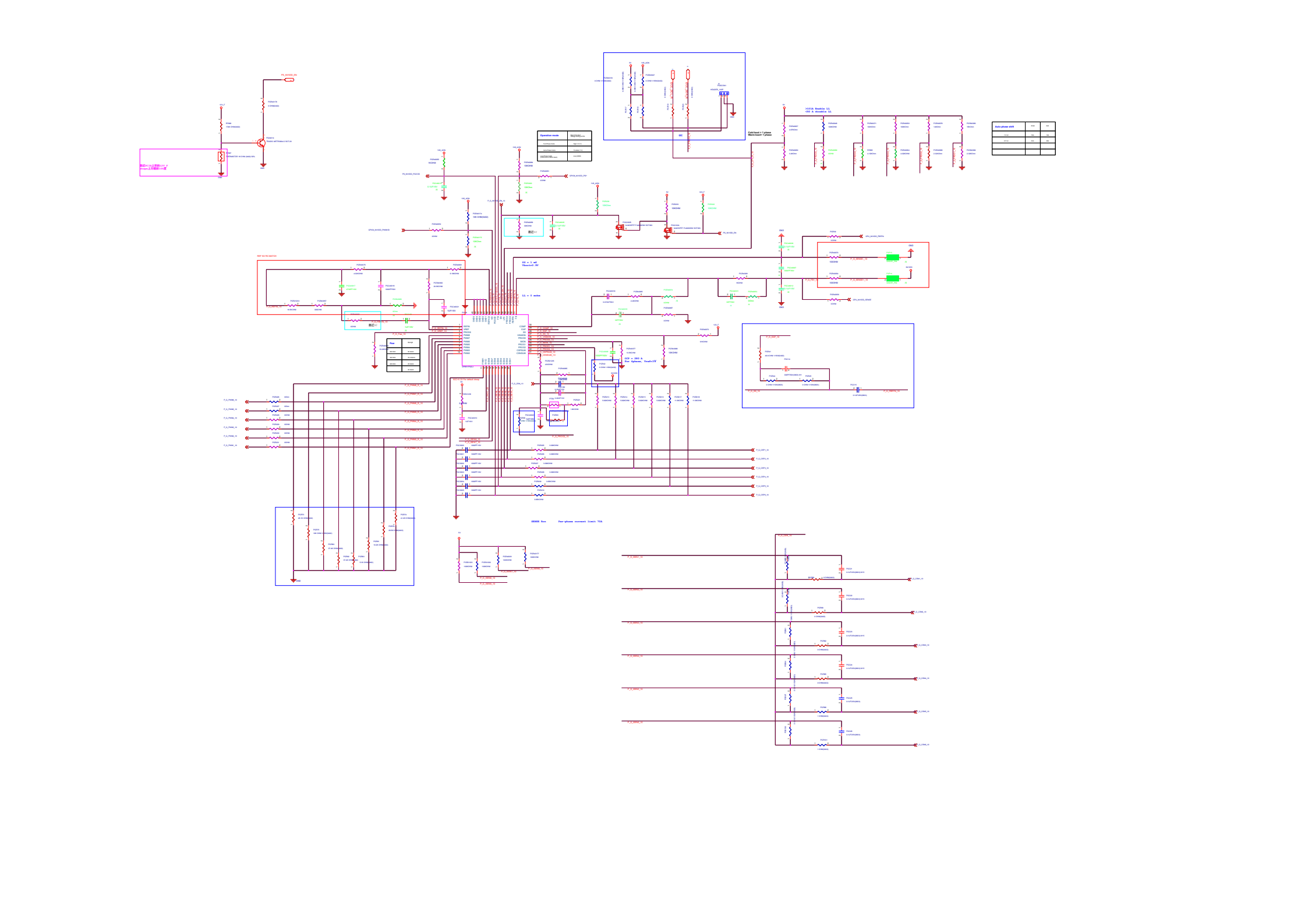
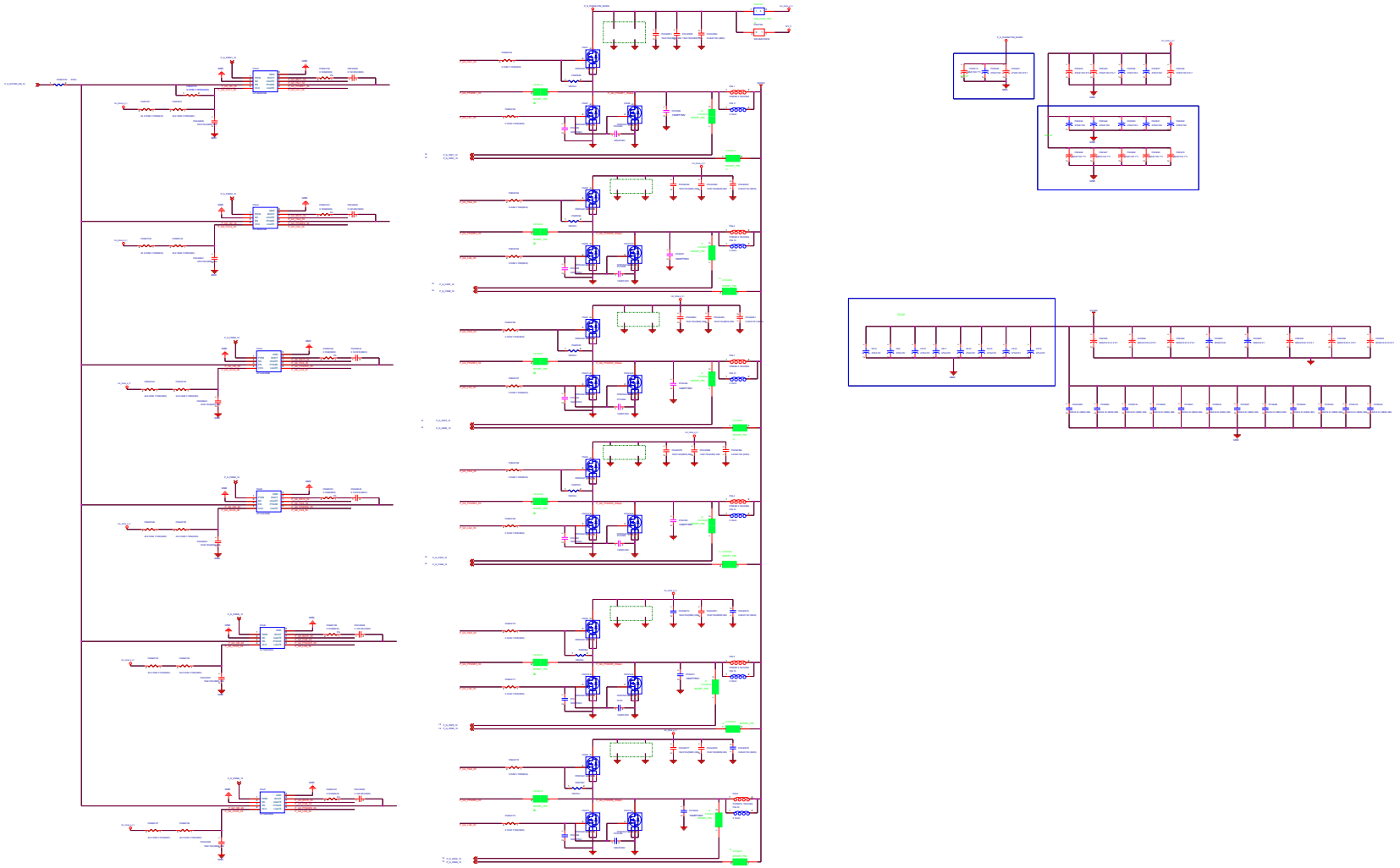
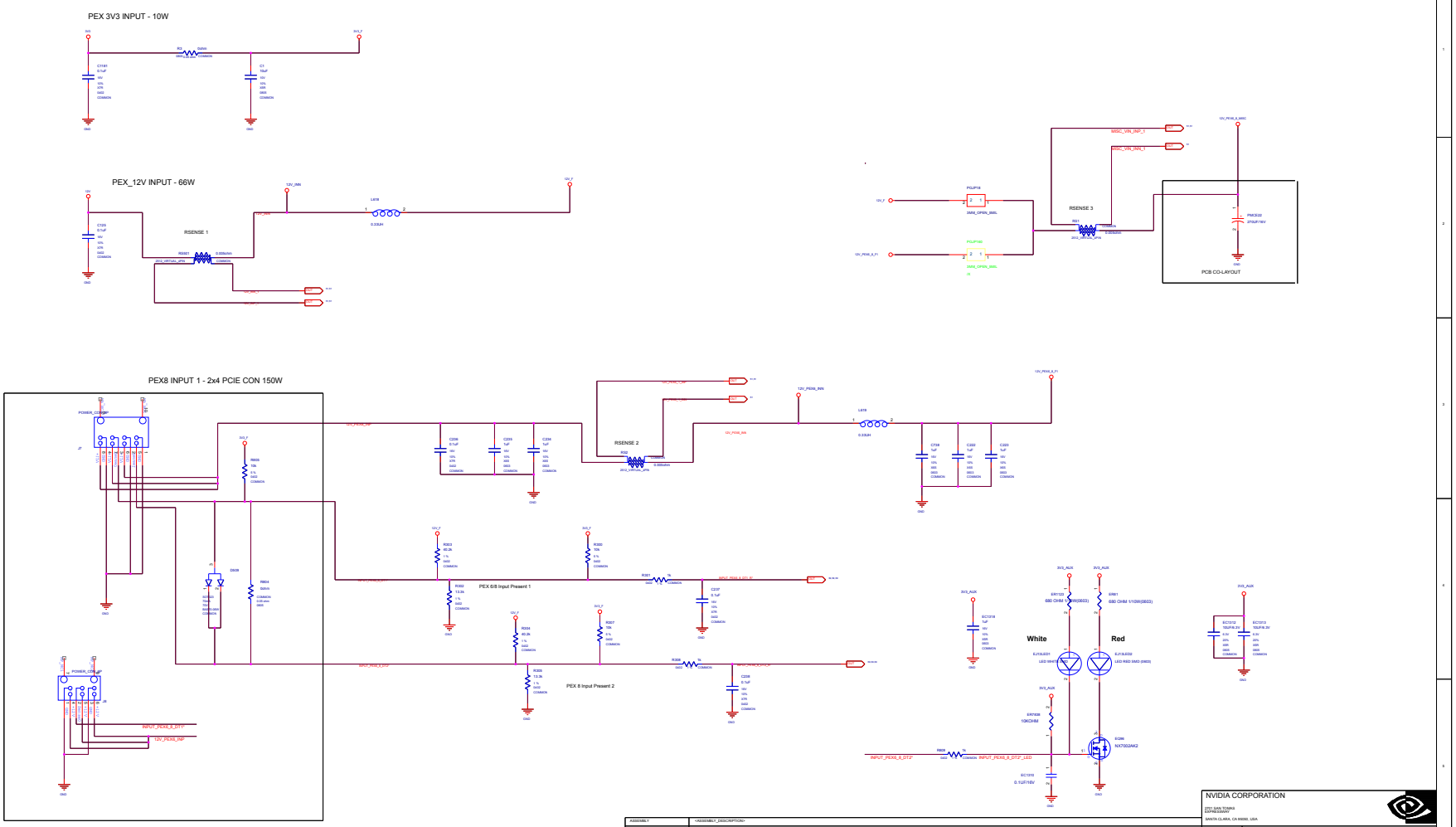




Page38: PS: Inputs, Filtering, and Monitoring



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Input, Filtering, and Monitoring

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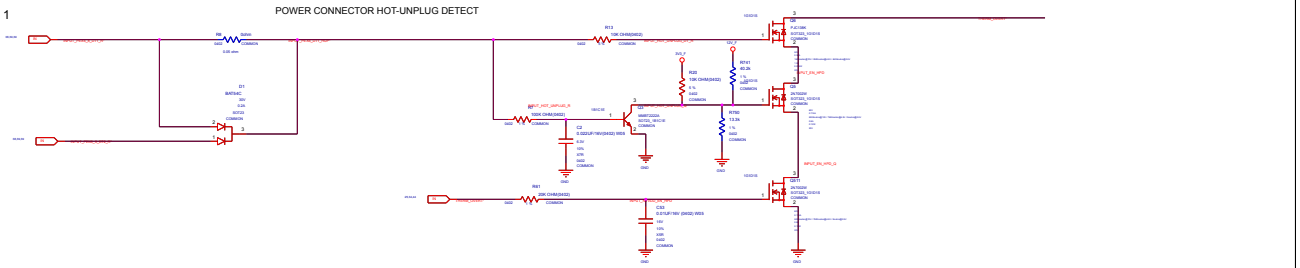
Page39: PS: HOT-UNPLUG, UNDER POWER BOOT, CURRENT STEERING

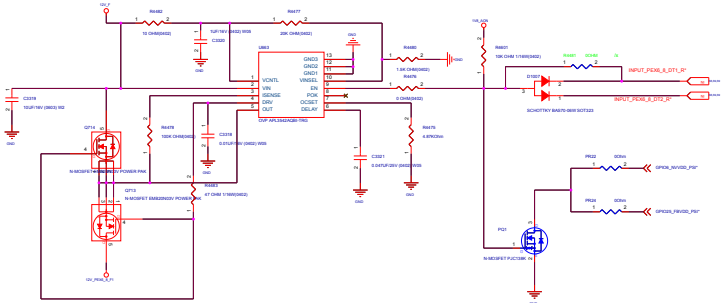
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

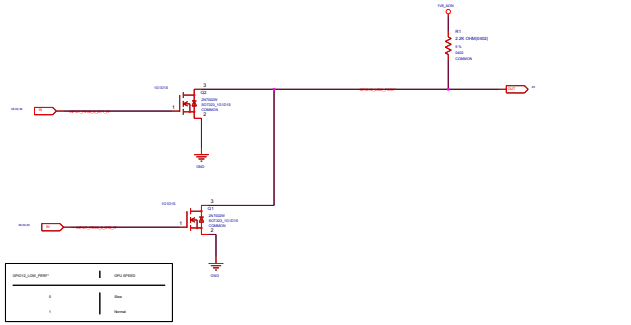


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: STEERING, UPS & HOT-UNPLUG

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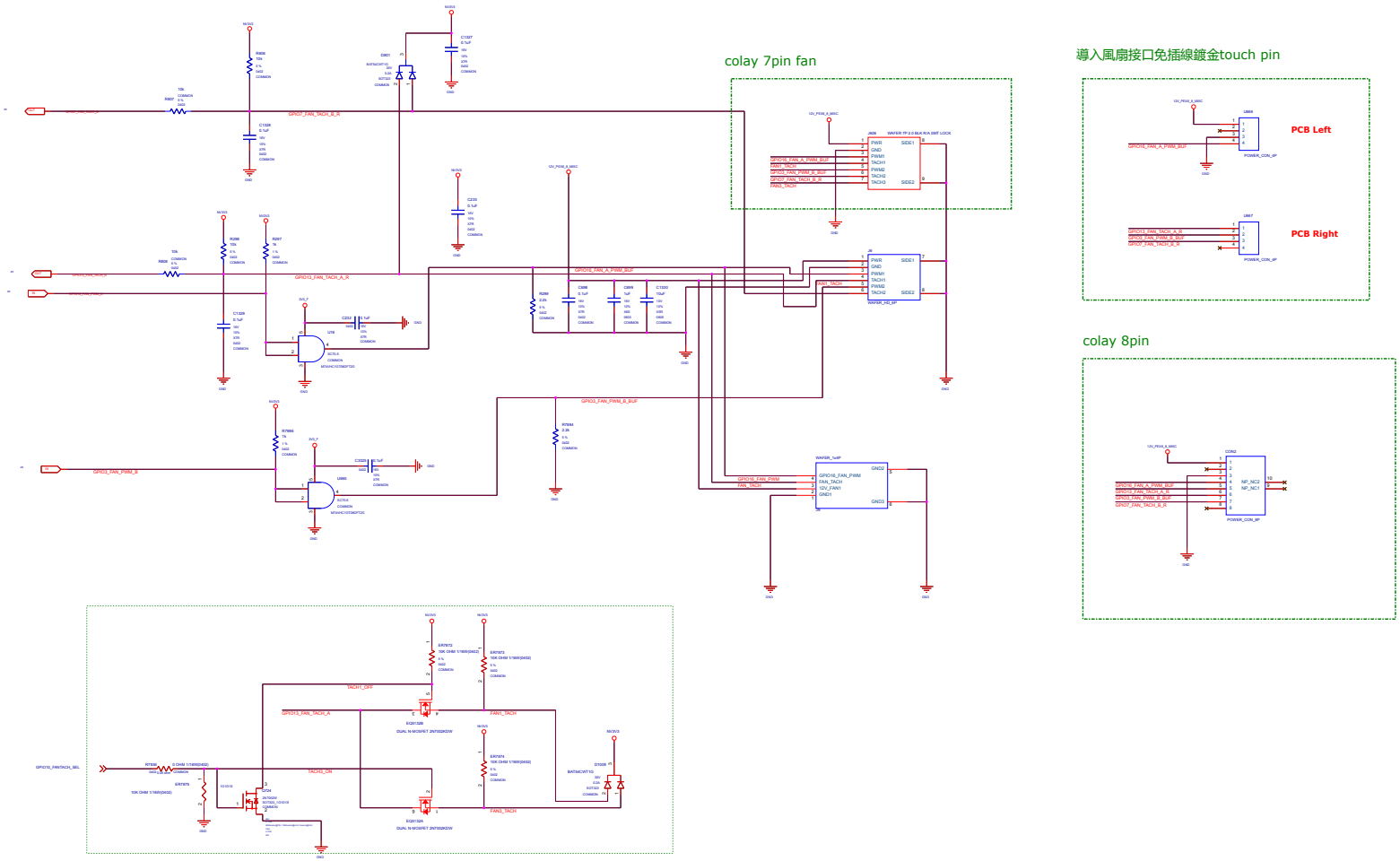
Page50: FAN



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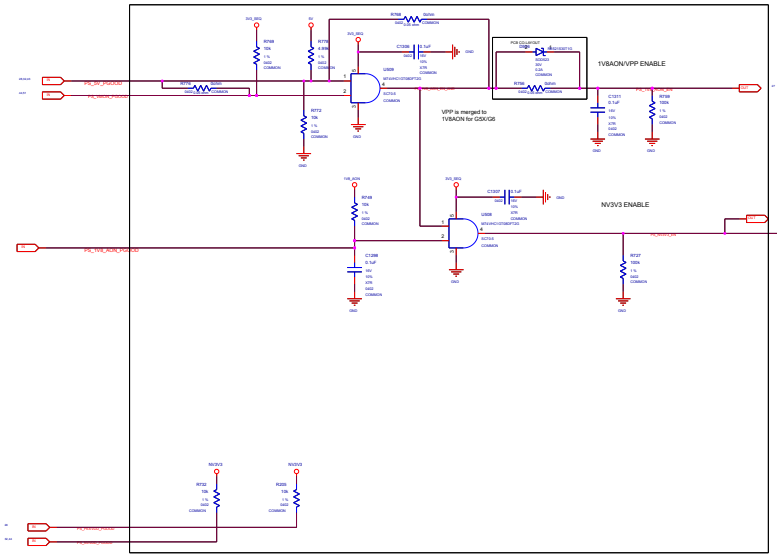
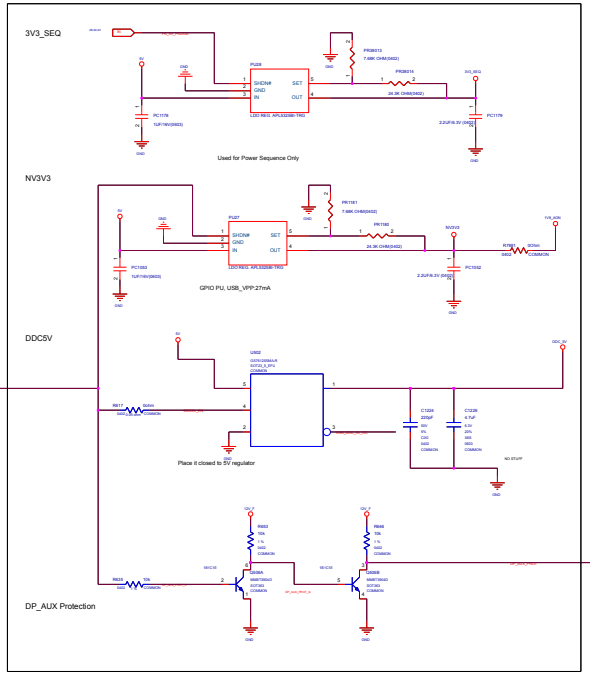
Page43: SEQ:5V,1V8,NV3V3 ENABLE





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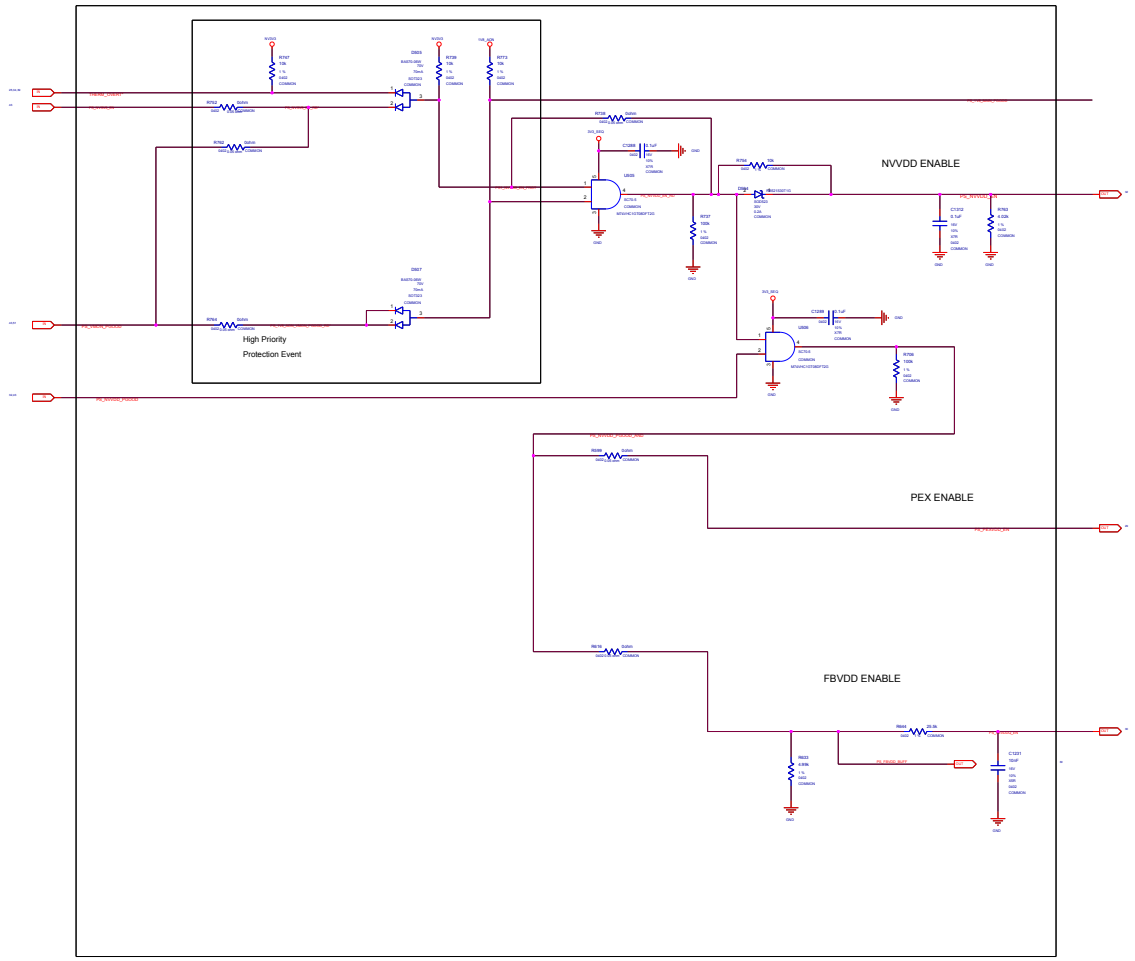
Page44: SEQ:NV,PEX,FB ENABLE



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Page47: SEQUENCE:MISC

PEX_CLKREQ*

PU ON GPU SIDE

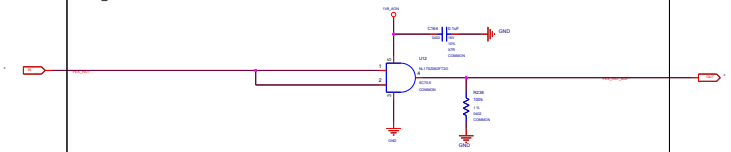
NC ON GOLD FINGER SIDE

GPU_WAKE*

PU ON GPU SIDE

NC ON GOLD FINGER SIDE

PEX_RST# LOGIC



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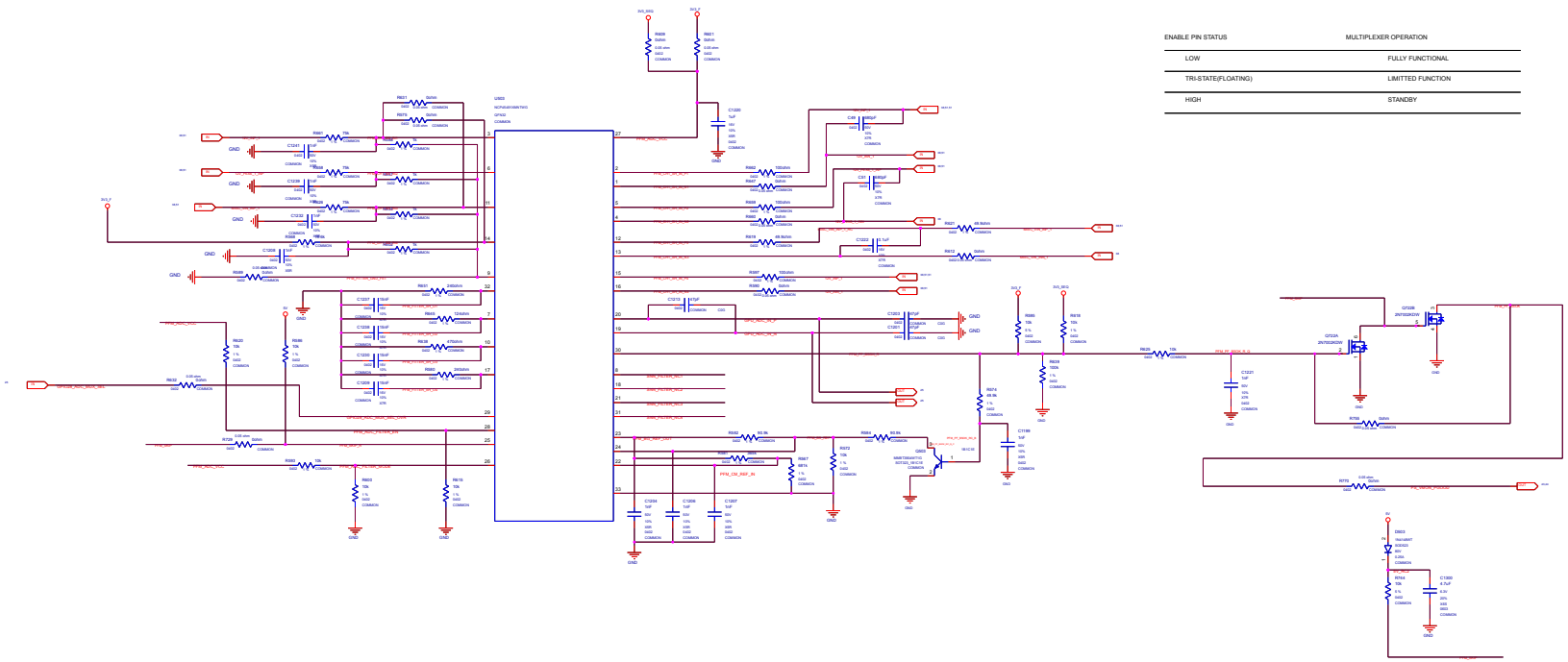
Page51: PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

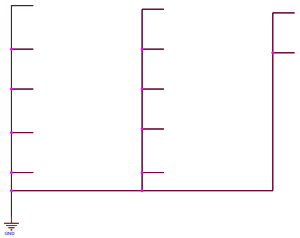
ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



Page52: MECH

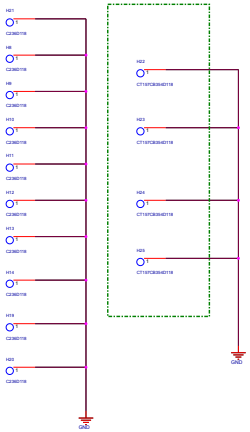
Bracket:

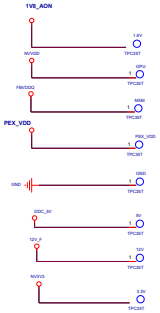
MOUNTING HOLES FOR HS:



BACK STIFFENER:

將GPU螺絲孔位直徑修改成9mm





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PAGE DETAIL	MECH

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