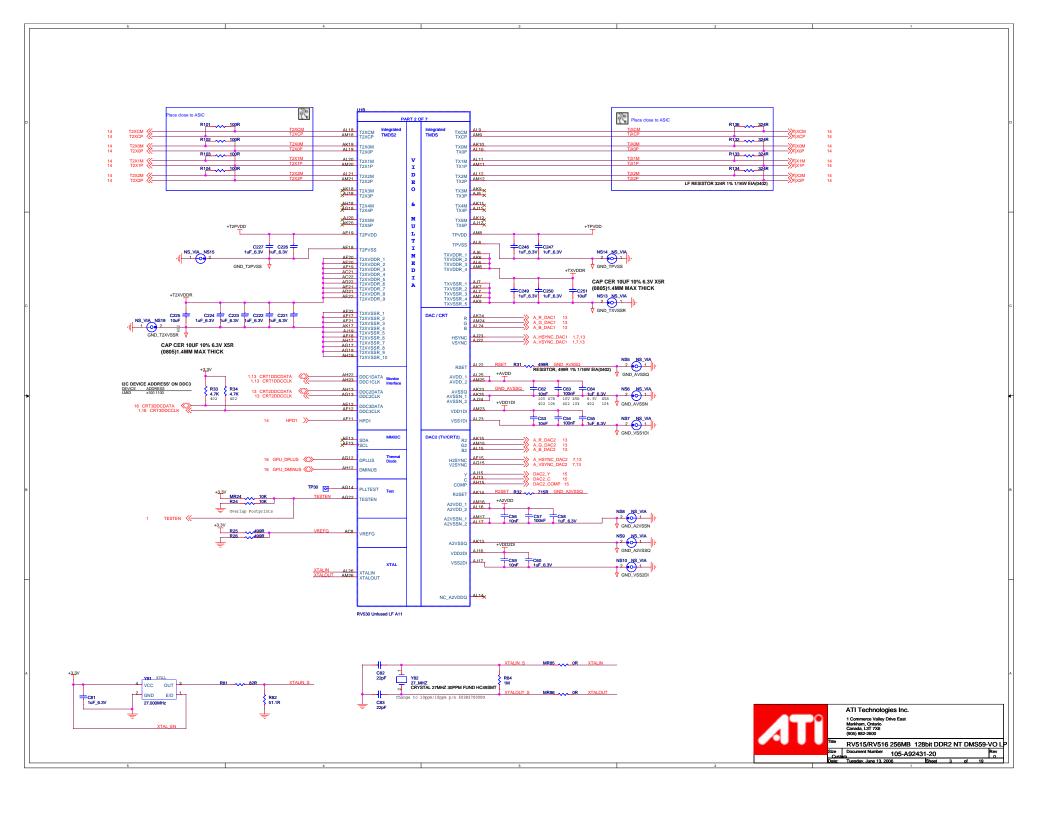


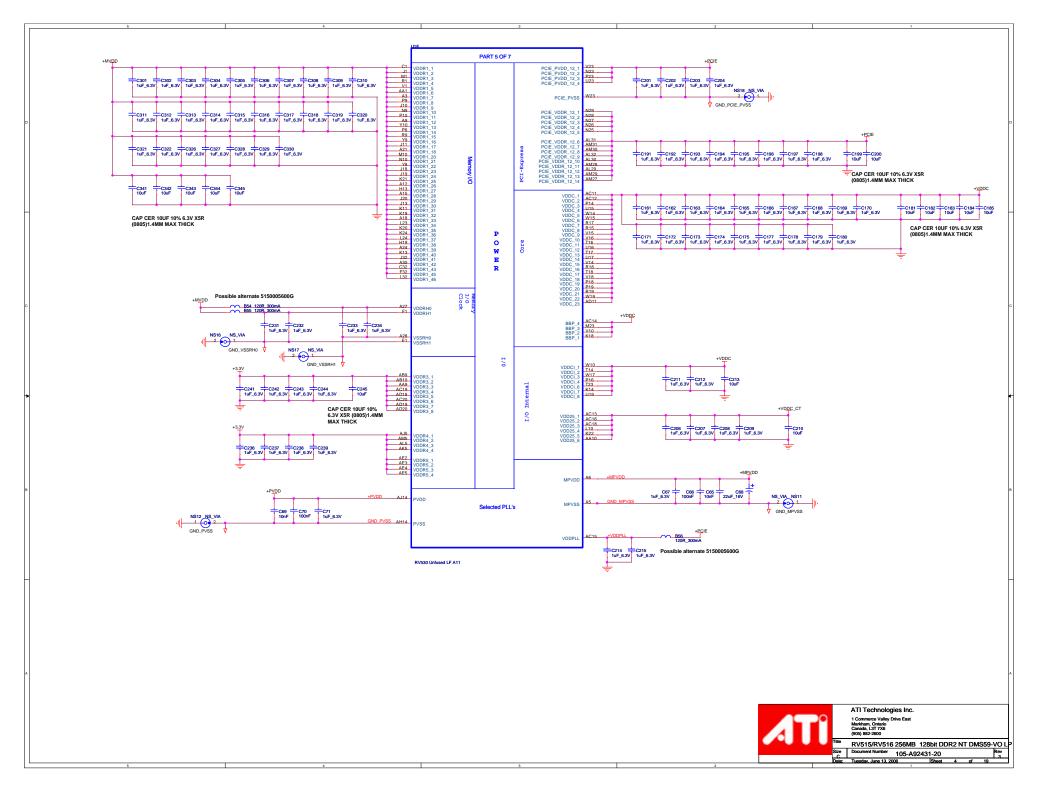


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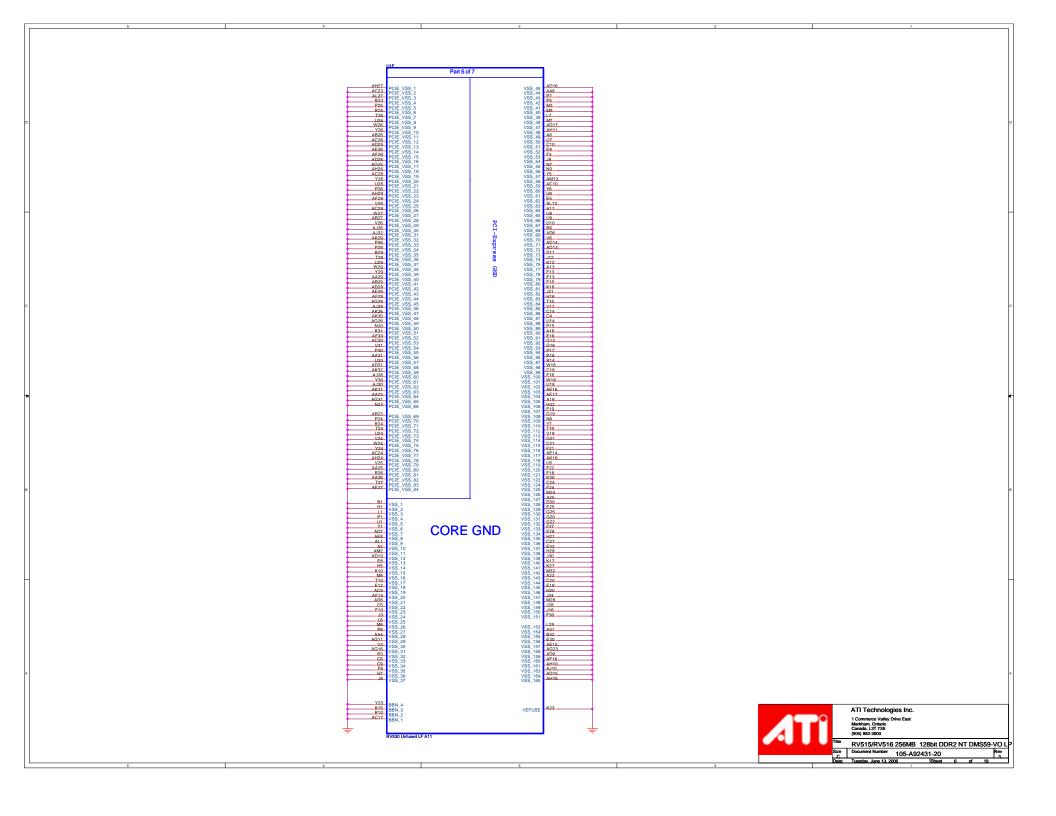
RV515/RV516 256MB 128bit DDR2 NT DMS59-VO L

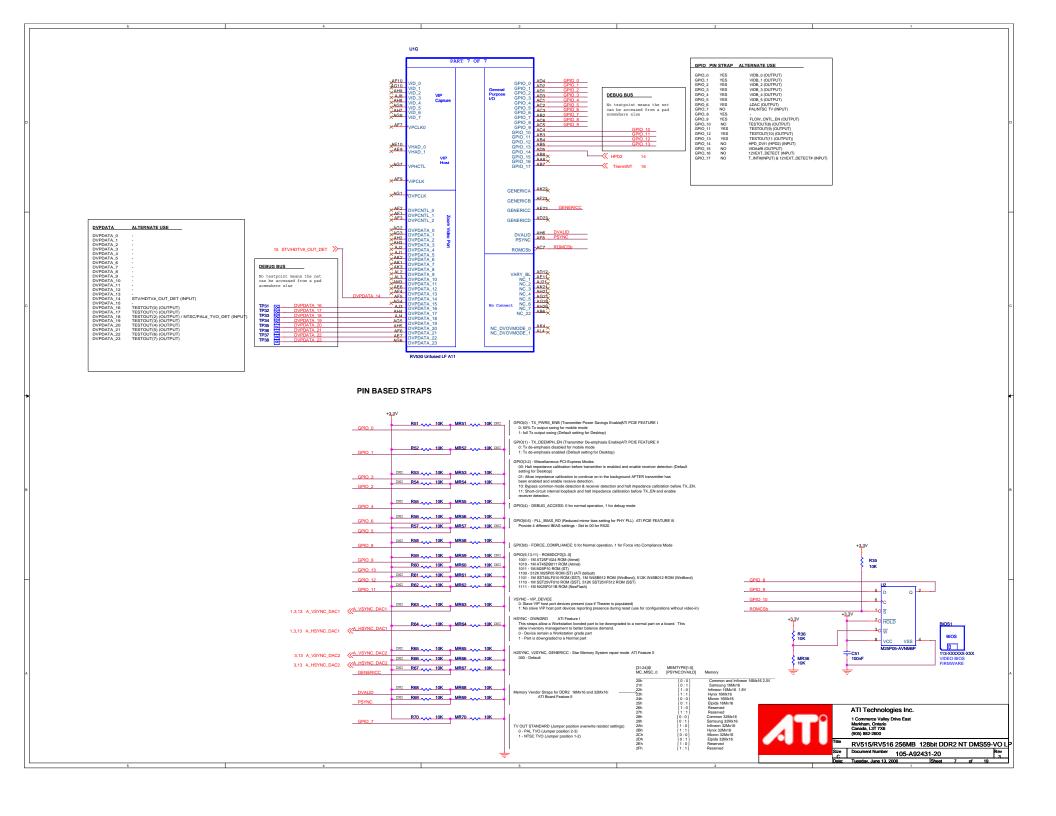
ment Number 105-A92431-20

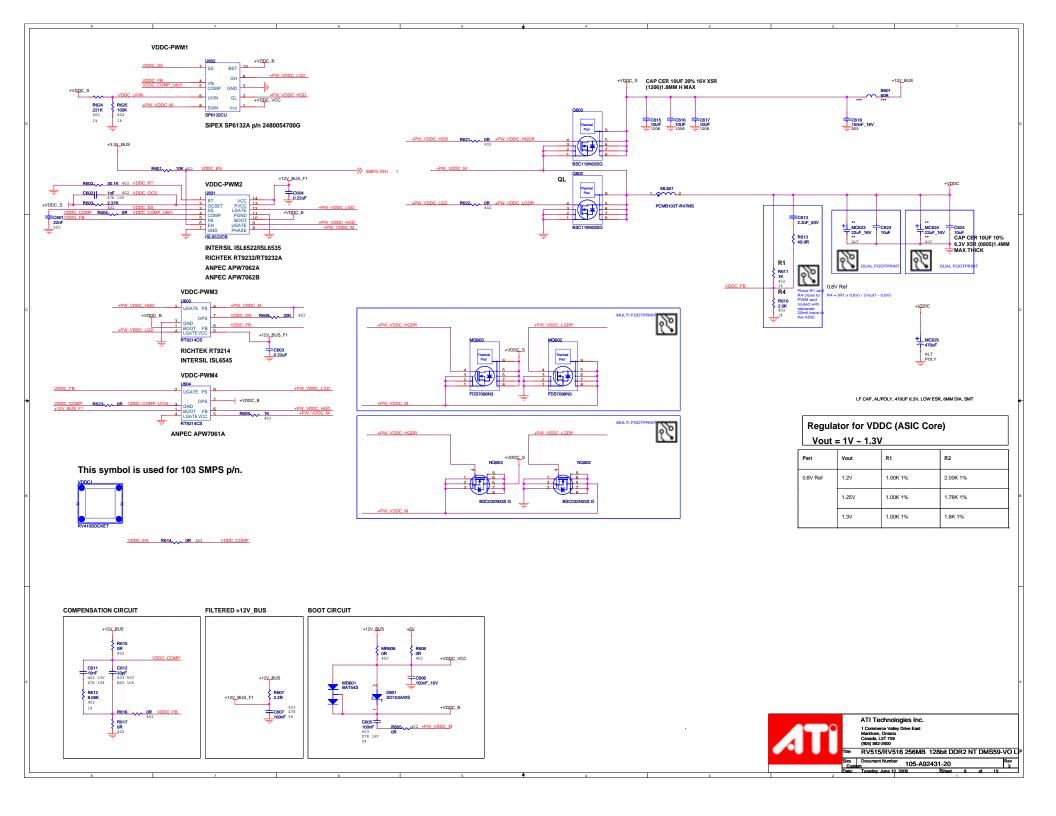


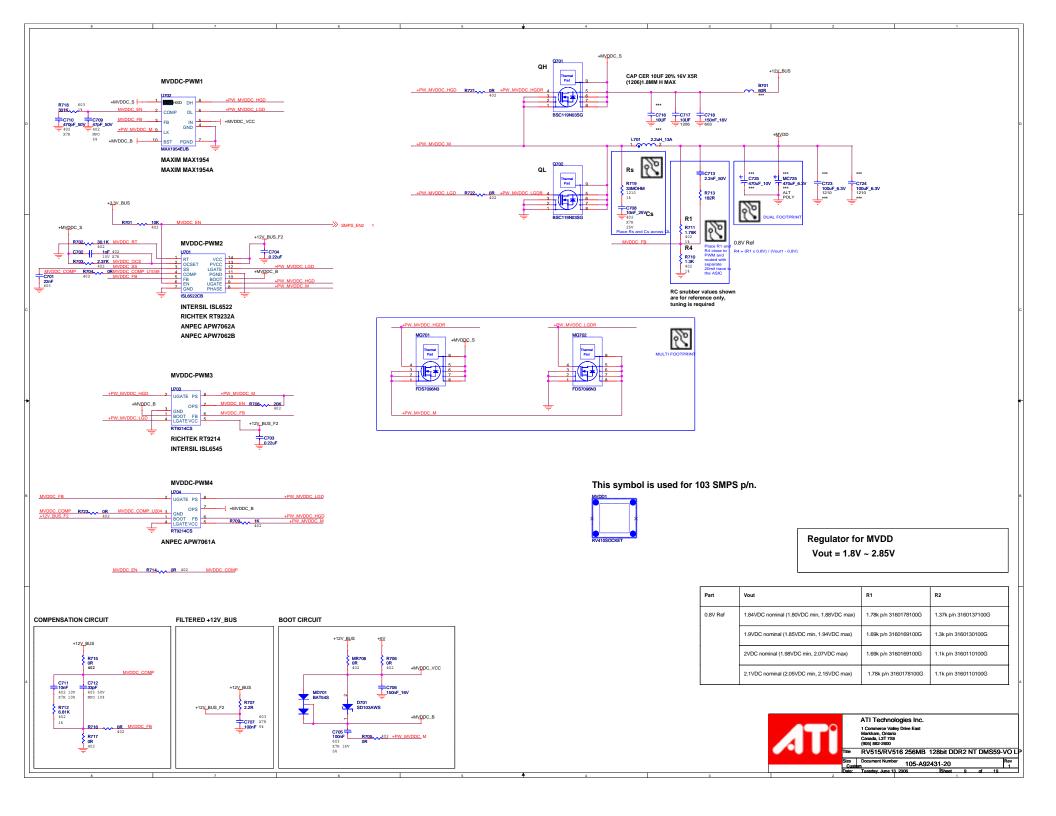


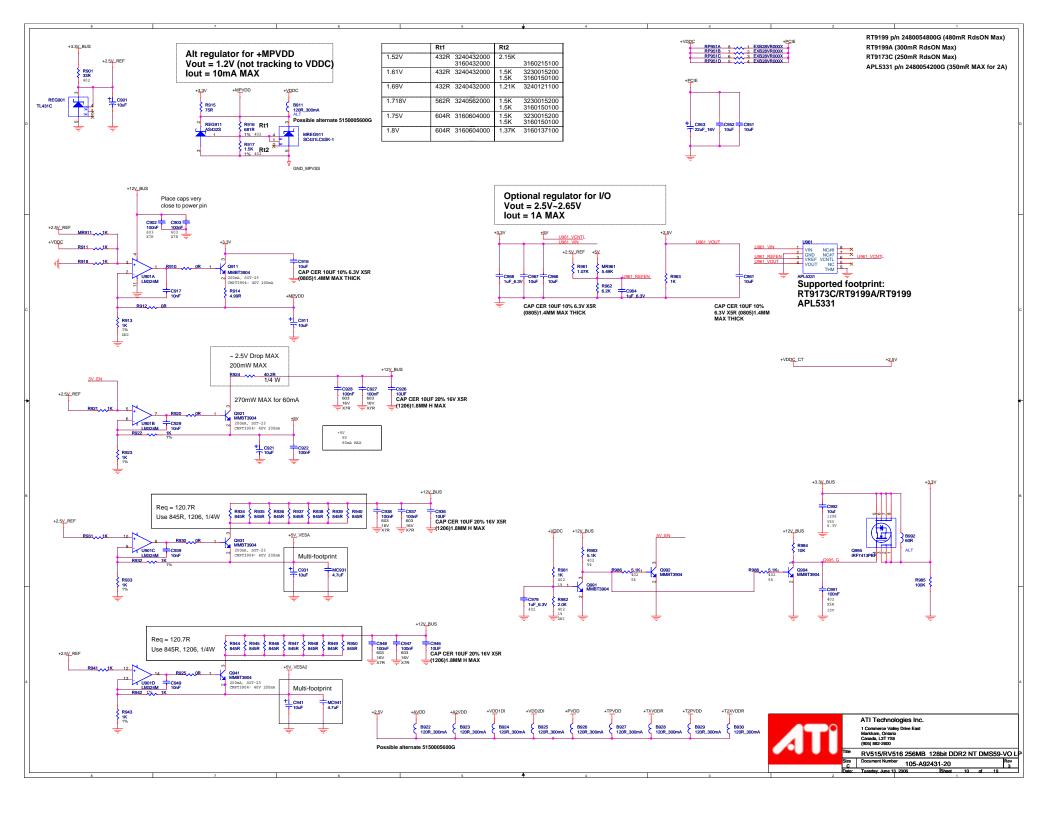
RV530 MEMORY CHANNELS A and B Channel B Channel A 12 M_MDB[63..0] < →>> M_MAB[12..0] 12 Part 4 of 7 11 M_MDA[63..0] <>> →>> M_MAA[12..0] 11 Part 3 of 7 MAB (MAB 2 MAB 3 MAB 4 MAB 4 MAB 5 MAB 1 C12 B11 C11 C8 B7 C7 B6 F12 D12 E11 F11 DA1 M30 DA2 L31 DA2 L31 DA3 L31 DA3 L31 DA3 L31 DA4 H30 DA5 G31 DA6 G30 DA7 L38 DA7 L31 DA8 M27 DA9 M29 DA9 L28 DA9 L2 MEMORY INTERFACE →>> M_MAB[15..14] 12 →>> M DOMB#I7 01 12 →>> M_DQMA#[7..0] 11 G28 H27 H26 F26 G26 H25 H24 H23 H22 J23 ✓ M_QSB[7..0] 12 _____ M_QSA[7..0] 11 QSB_0 QSB_1 QSB_2 QSB_4 QSB_6 QSB_6 QSB_6 QSA_G QSA_G QSA_G QSA_G QSA_G QSA_G QSA_G QSB_0B QSB_1B QSB_2B QSB_3B QSB_4B QSB_5B QSB_6B QSB_6B QSB_7B QSA_0B QSA_1B QSA_2B QSA_3B QSA_4B QSA_5B QSA_6B QSA_6B QSA_7B ODTB0 ODTA0 ODTA0 ODTA0 11 For DDR2 For DDR2 CLKB0 B4 CLKB0 CLKB00 CLKA0 D31 CLKA0 CLKAWO CKEB0 CX CKEB0 12 CKEA0 B30 CKEA0 RASB0b DE2 >>> RASB#0 RASA0b DB28 >>> RASAW0 11 CASBOb D3 CASBNO 12 CASA0b C29 >> CASA#0 11 WEB0b DB2 →>> WEB#0 12 +MVDD WEA0b 0831 -->> WEA#0 11 CSA0b_0 CSA0b_1 CSA0b_ R165 100R 1% CLKB1 DP3 CLKB1 12 CLKB#1 12 CLKA1 B20 CLKA1 11 CLKA1b C19 CLKA#1 11 C351 — C352 100nF 10nF R162 100R 1% CKEB1 13 CKEB1 12 CKEA1 C22 CKEA1 11 C355 100nF +C356 RASB1b DJ2 >>> RASB#1 12 DRAM_RST RASA1b DB24 >>> RASA#1 11 CASB1b DL2 >>> CASB#1 12 TEST_MCLK CASA1b DB22 >>> CASA#1 11 WEB1b 0^{M2}→>> WEB#1 12 TEST_YCLK WEA1b 2821 -->> WEA#1 11 CSB#1_0 12 CSA1b_0 DB23 >>> CSA#1_0 11 MEMTEST ATI Technologies Inc. RV515/RV516 256MB 128bit DDR2 NT DMS59-VO L Size Document Number 10 Date: Tuesday, June 13, 2006 Document Number 105-A92431-20



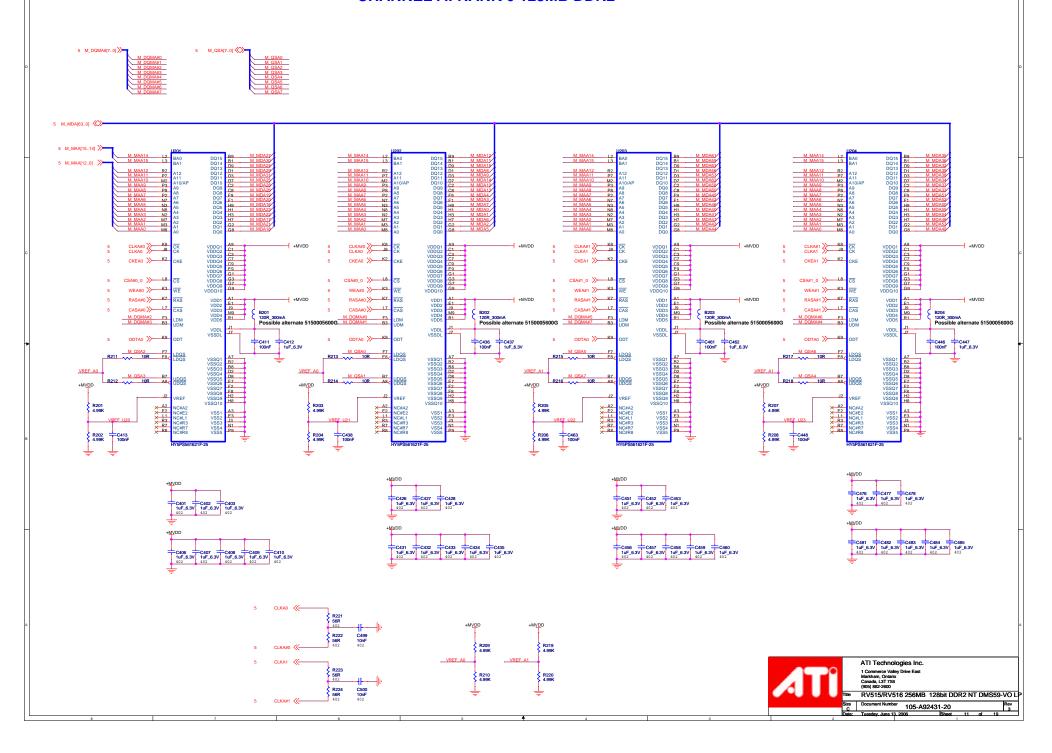




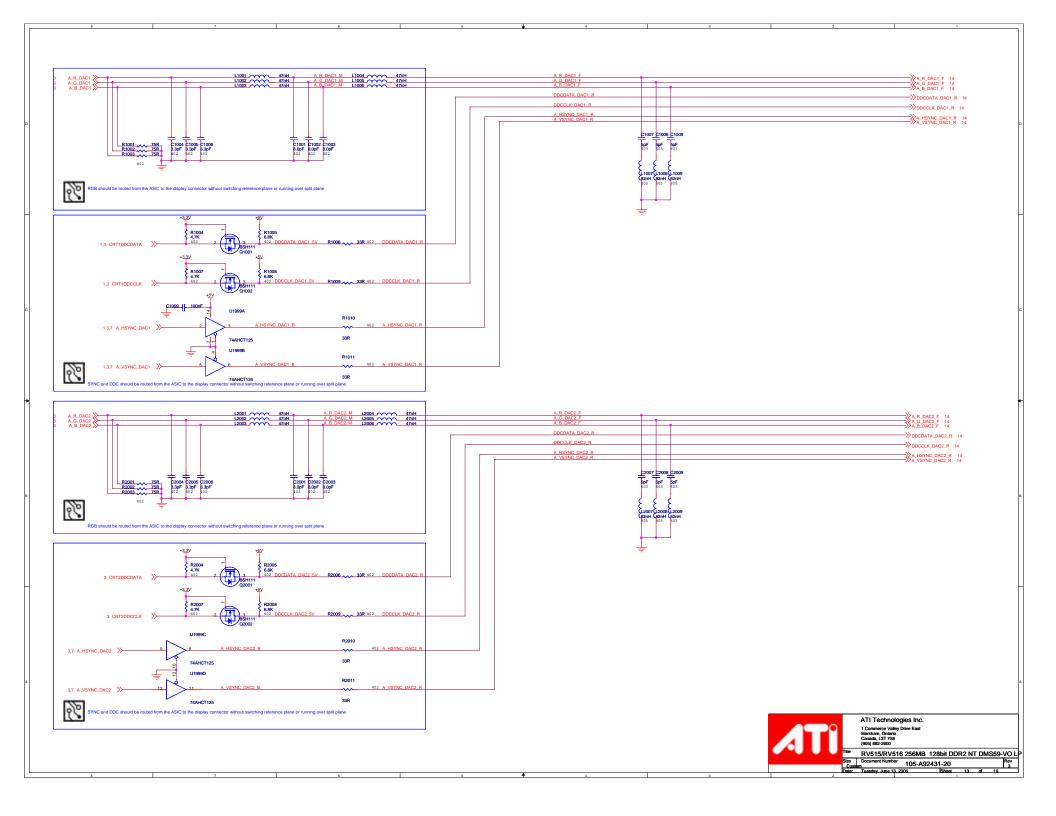




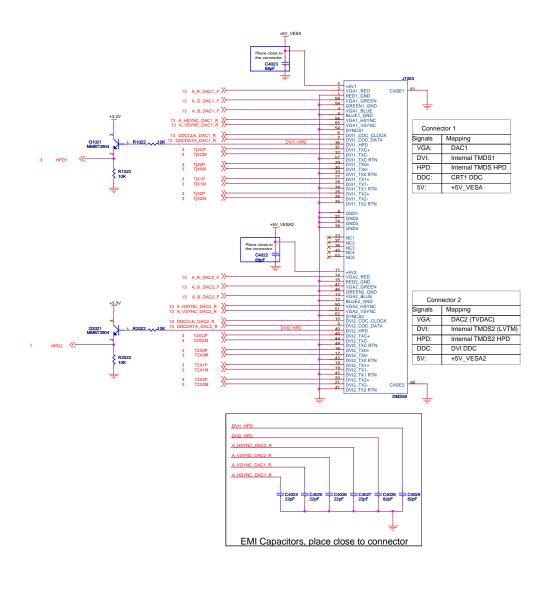
CHANNEL A: RANK 0 128MB DDR2



CHANNEL B: RANK 0 128MB DDR2 5 M_DQMB#[7..0] >>-5 M_QSB[7..0] < 5 M_MAB[15..14] >> VDDQ1 VDDQ2 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 ODTBO >> KS ODTB0 >> C561 C562 100nF 1uF_6.3V C511 +C512 100nF 1uF_6.3V C536 C537 100nF 1uF_6.3V C585 = VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 VSSQ10 VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 +MVDD +MVDD +MVDD R301 4.99K R306 R304 4.99K 4.99K C556 C557 C558 C559 C560 UF_6.3V 1uF_6.3V 1uF_6.3V 1uF_6.3V 1uF_6.3V C580 C581 C582 C583 C584 1uF_6.3V 1uF_6.3V 1uF_6.3V 1uF_6.3V 1uF_6.3V 1uF_6.3V 402 R319 4.99K CLKB1 << VREF B0 ATI Technologies Inc. 1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600 R310 4.99K R324 56R 402 RV515/RV516 256MB 128bit DDR2 NT DMS59-VO L Document Number 105-A92431-20

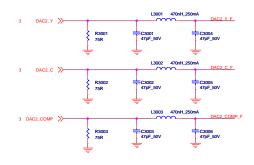


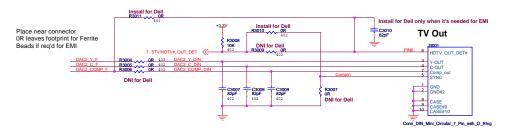
VESA Multi-Display Interface DMS-59 Connector







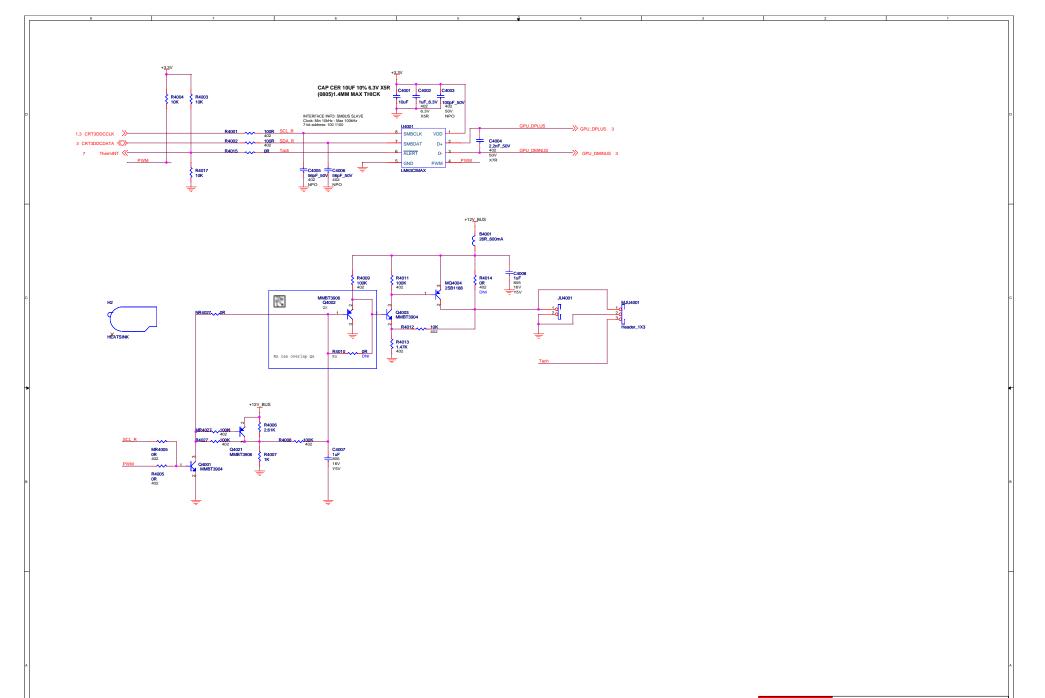




The 7-pin MiniDIN footprint allows one of the two MiniDINs:

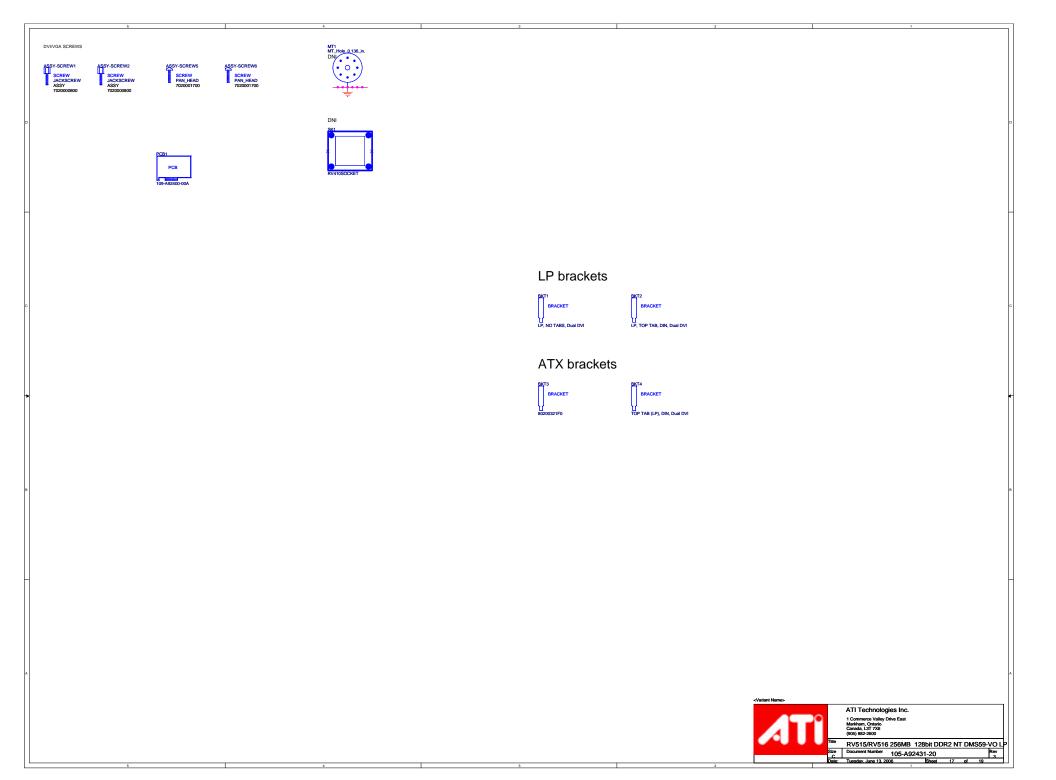
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G







ATI Technologies Inc.



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				Title	Schematic No.	Date:	
ATI				RV515/RV516 256MB 128bit DDR2 NT DMS59-VO LP 105-A92431-20 Tuesday, June 13			006
				REVISION HISTORY			Rev 3
Sch PCB Rev Rev Date		Date	REVISION DESCRIPTION				
	0						
	1						
	2	10	04/27/06	-l0 PCB release, No PCB effecting schematic Changes, Few Layout improvements for EMI (increase spacing of power	er plans from TMDS pairs)		
	3 20A 05/16/06 -20A PCB release, Adding ML601 as dual footprint for NL601 in VDDC SMPS, Moving TV DAC Filter far from VDDC regulator, All TVO Filter caps (C3001-6) changed to 402						
3 20 06/13/06 -20A PCB release, ML601 Removed							
С							(
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L			5	4 3	2	1	

