

P393-A01 Base Design

P393-A01, G92, 8Mx32/16Mx32 GDDR3 (800/1000 MHz),
DVI-I-DL, DVI-I-DL/DisplayPort, HDTVout/Stereo

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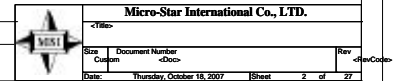
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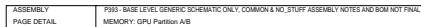
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0	BASE	800-10393-0000-100	P393 -BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU_DT_0000	800-10393-0000-100	P393 Q00-300 512MB GDDR3 18MAJ2 DV1+DV1+HDTV
2	SKU_DT_0002	800-10393-0000-100	P393 Q00-200 512MB GDDR3 18MAJ2 DV1+DV1+HDTV
3	SKU_VS_0000	800-10393-0000-100	P393 Q00-8P5 512MB GDDR3 18MAJ2 DV1+DV1+HDTV
4	SKU_VS_0001	800-10393-0001-100	P393 Q00-8P5 512MB GDDR3 18MAJ2 DV1+DV1+HDTV
5	SKU_DT_0004	800-10393-0004-100	P393 Q00-270 512MB GDDR3 18MAJ2 DV1+DV1+HDTV
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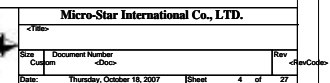
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SUMMARY			
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	Rev		
	<RevCode>		



13MRGA CMD Mapping	
ADON	EMERG
BAG*	CM01
CAG*	CM10
W5*	CM11
C30*	CM16
C40*	CM17
B40	CM12
B41	CM13
Au10	CM14
Au10	CM19
Au10	CM05
Sh10	CM22
Sh10	CM04
Sh10	CM01
Sh10	CM02
Sh10	CM03
Sh10	CM04
Sh10	CM06
Sh10	CM08
Sh10	CM13
Au10	CM01
Au10	CM16
Au10	CM02
Au10	CM03
Au10	CM10
Au10	CM17
Au10	CM01
C40	CM18
RST	CM15



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NET RULES for FrameBuffer A/B

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
3.5 C17 FBA_CLK0	1	80OHM	FBA_CLK0
3.5 C17 FBA_CLK1	1	80OHM	FBA_CLK1
3.5 C17 FBA_CLK17	1	80OHM	FBA_CLK1

3.5 C17 FBA_CMOS0_0	1	80OHM	
3.5 C17 FBA_CMOS0_WF0_0	1	80OHM	
3.5 C17 FBA_CMOS0_WF1_0	1	80OHM	
3.5 C17 FBA_CMOS0_WF2_0	1	80OHM	

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
3.6 C17 FBS_CLK0	1	80OHM	FBS_CLK0
3.6 C17 FBS_CLK1	1	80OHM	FBS_CLK1
3.6 C17 FBS_CLK17	1	80OHM	FBS_CLK1

3.6 C17 FBS_CMOS0_0	1	80OHM	
3.6 C17 FBS_CMOS0_WF0_0	1	80OHM	
3.6 C17 FBS_CMOS0_WF1_0	1	80OHM	
3.6 C17 FBS_CMOS0_WF2_0	1	80OHM	

3 C17 FBA_DEBUG	1	80OHM	
3 C17 FBS_DEBUG	1	80OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
3 C17 FBA_PLLAUX0	1.0V	0.02A	12MIL

5 C17 FBA_VREF0	1.80V	0.02A	12MIL
5 C17 FBA_VREF1	1.80V	0.02A	12MIL
5 C17 FBA_VREF2	1.80V	0.02A	12MIL
5 C17 FBA_VREF3	1.80V	0.02A	12MIL

5 C17 FBA_ZD0	2.0V	0.02A	12MIL
5 C17 FBA_ZD1	2.0V	0.02A	12MIL

6 C17 FBS_VREF0	1.80V	0.02A	12MIL
6 C17 FBS_VREF1	1.80V	0.02A	12MIL
6 C17 FBS_VREF2	1.80V	0.02A	12MIL
6 C17 FBS_VREF3	1.80V	0.02A	12MIL

6 C17 FBS_ZD0	2.0V	0.02A	12MIL
6 C17 FBS_ZD1	2.0V	0.02A	12MIL

3 C17 FB_VREF1	1.80V	0.02A	12MIL
3 C17 FB_VREF2	1.80V	0.02A	12MIL

NET RULES for FrameBuffer C/D

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
4.7 C17 FBC_CLK0	1	80OHM	FBC_CLK0
4.7 C17 FBC_CLK1	1	80OHM	FBC_CLK1
4.7 C17 FBC_CLK17	1	80OHM	FBC_CLK1

4.7 C17 FBC_CMOS0_0	1	80OHM	
4.7 C17 FBC_CMOS0_WF0_0	1	80OHM	
4.7 C17 FBC_CMOS0_WF1_0	1	80OHM	
4.7 C17 FBC_CMOS0_WF2_0	1	80OHM	

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
4.8 C17 FBC_CLK0	1	80OHM	FBC_CLK0
4.8 C17 FBC_CLK1	1	80OHM	FBC_CLK1
4.8 C17 FBC_CLK17	1	80OHM	FBC_CLK1

4.8 C17 FBC_CMOS0_0	1	80OHM	
4.8 C17 FBC_CMOS0_WF0_0	1	80OHM	
4.8 C17 FBC_CMOS0_WF1_0	1	80OHM	
4.8 C17 FBC_CMOS0_WF2_0	1	80OHM	

4 C17 FBC_DEBUG	1	80OHM	
4 C17 FBS_DEBUG	1	80OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
4 C17 FBC_PLLAUX0	1.0V	0.02A	12MIL

7 C17 FBC_VREF0	1.80V	0.02A	12MIL
7 C17 FBC_VREF1	1.80V	0.02A	12MIL
7 C17 FBC_VREF2	1.80V	0.02A	12MIL
7 C17 FBC_VREF3	1.80V	0.02A	12MIL

7 C17 FBC_ZD0	2.0V	0.02A	12MIL
7 C17 FBC_ZD1	2.0V	0.02A	12MIL

8 C17 FBC_VREF0	1.80V	0.02A	12MIL
8 C17 FBC_VREF1	1.80V	0.02A	12MIL
8 C17 FBC_VREF2	1.80V	0.02A	12MIL
8 C17 FBC_VREF3	1.80V	0.02A	12MIL

8 C17 FBC_ZD0	2.0V	0.02A	12MIL
8 C17 FBC_ZD1	2.0V	0.02A	12MIL

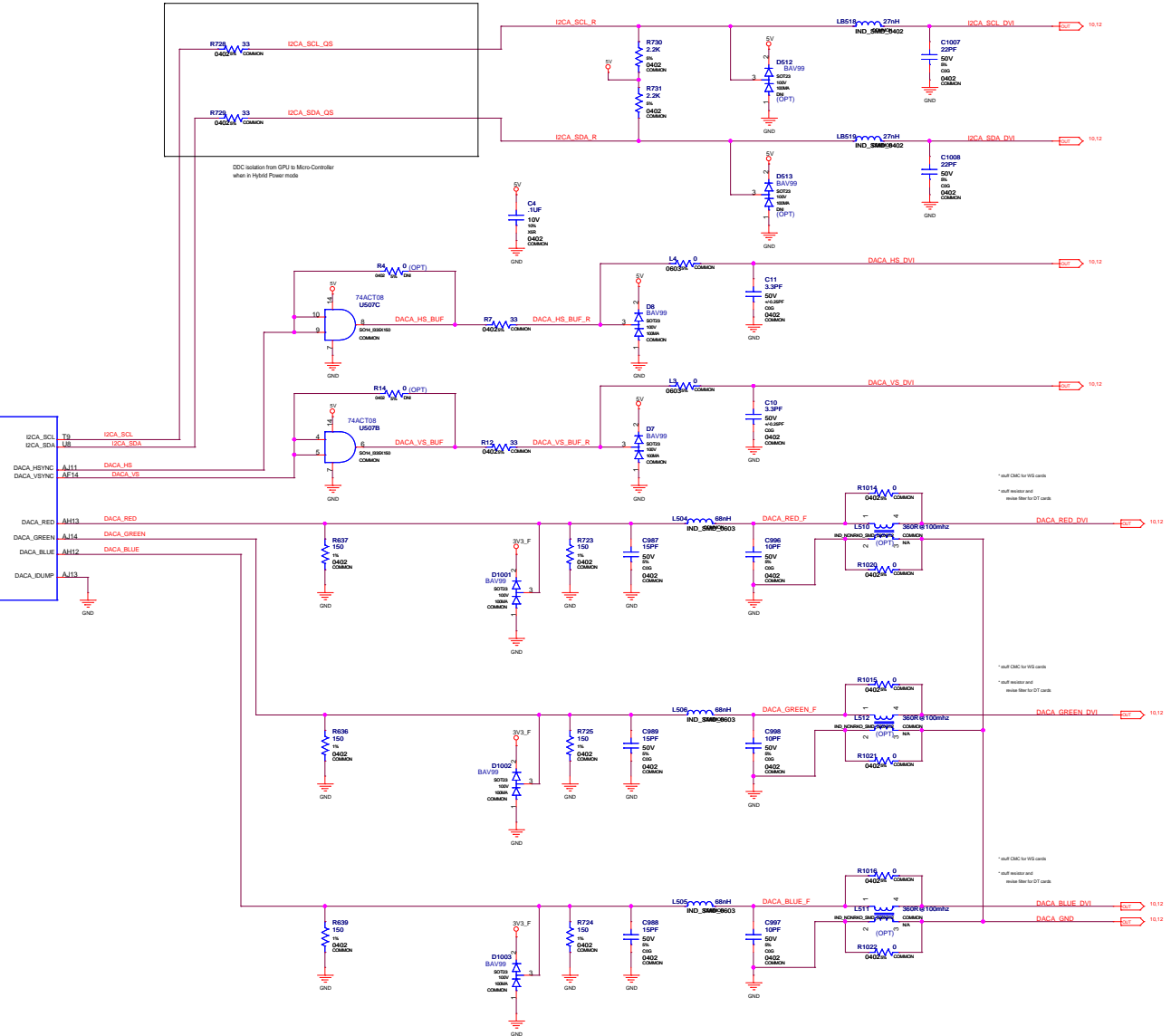
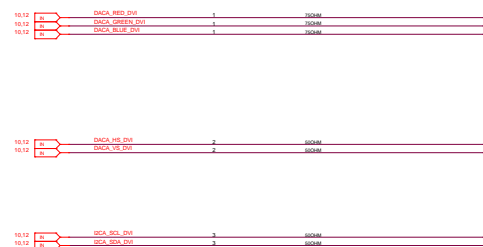
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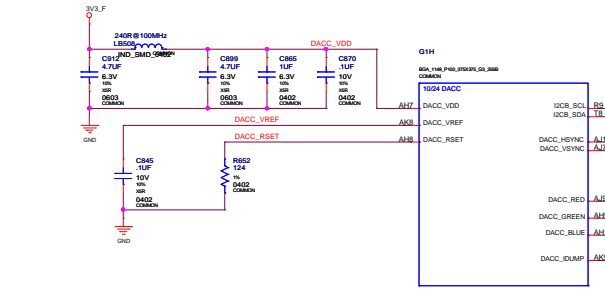
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FrameBuffer Net Rules



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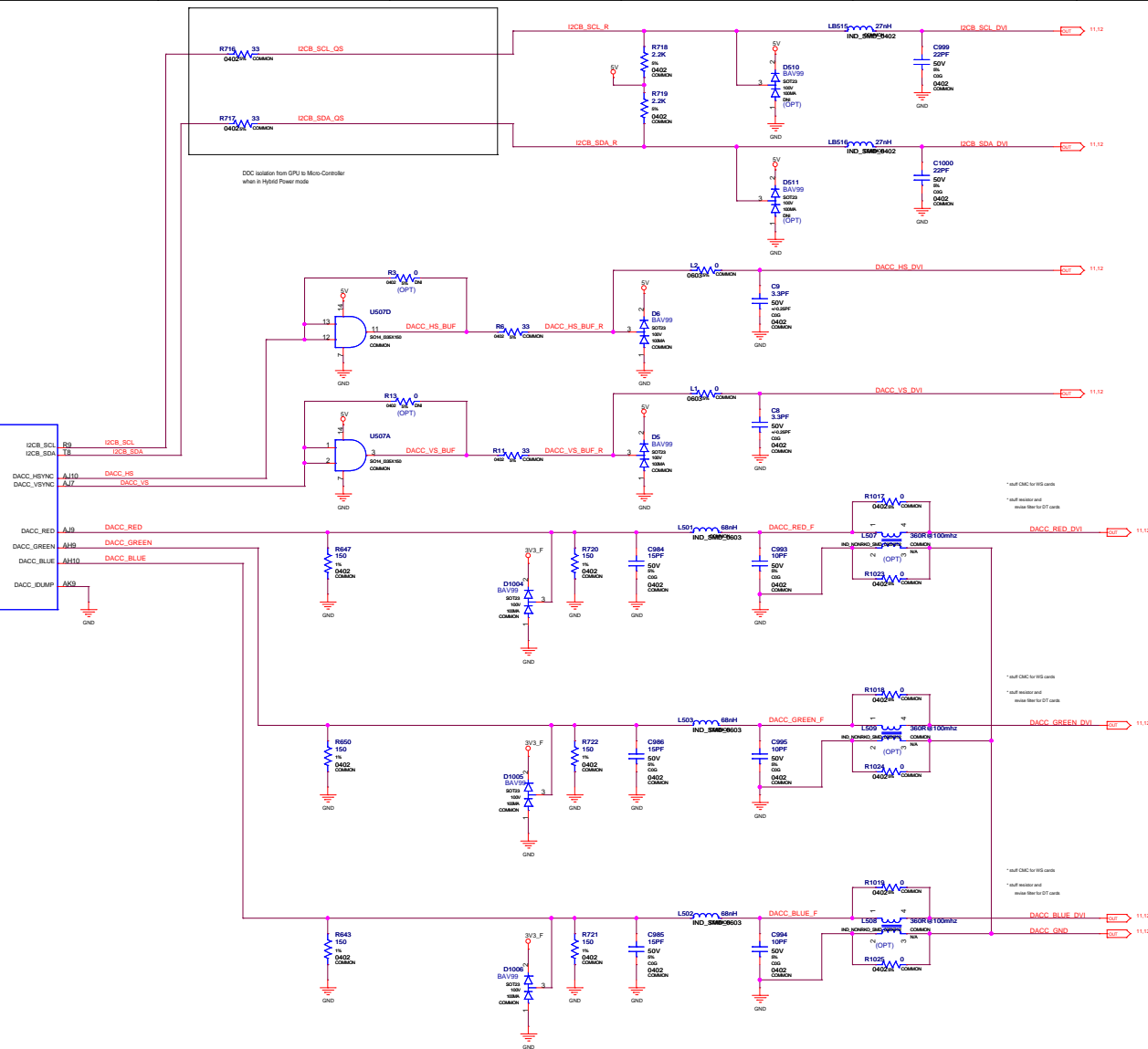
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DACC NET RULES

NET	NY_CRITICAL	NY_IMPEDANCE	DIFF_PAIR
11.02	DAC0_RED_DIN	1	320m
11.02	DAC0_GREEN_DIN	1	320m
11.02	DAC0_BLUE_DIN	1	320m
11.02	DAC0_HB_DIN	2	320m
11.02	DAC0_VB_DIN	2	320m
11.02	DCB_SCL_DIN	3	320m
11.02	DCB_SDA_DIN	3	320m



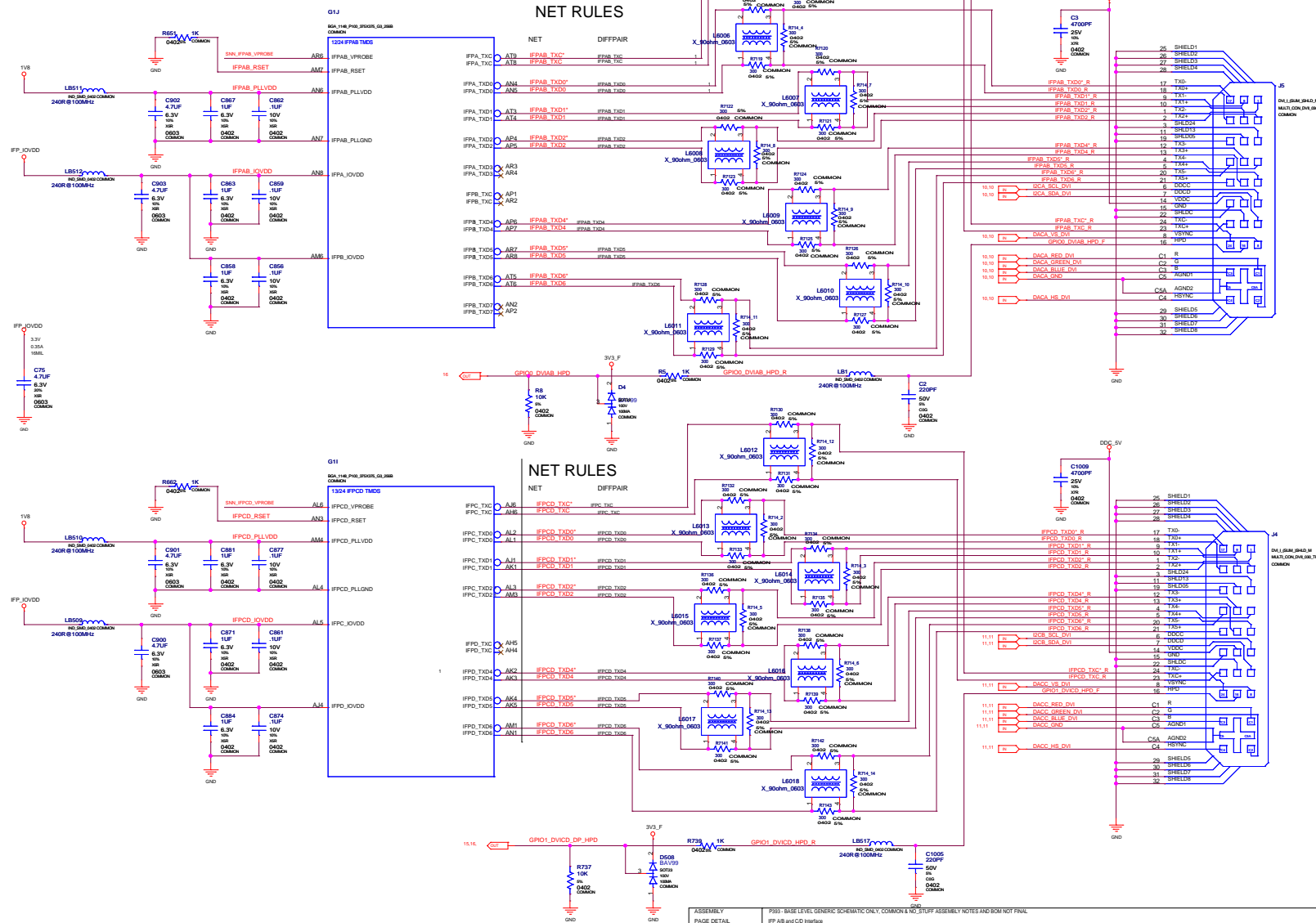
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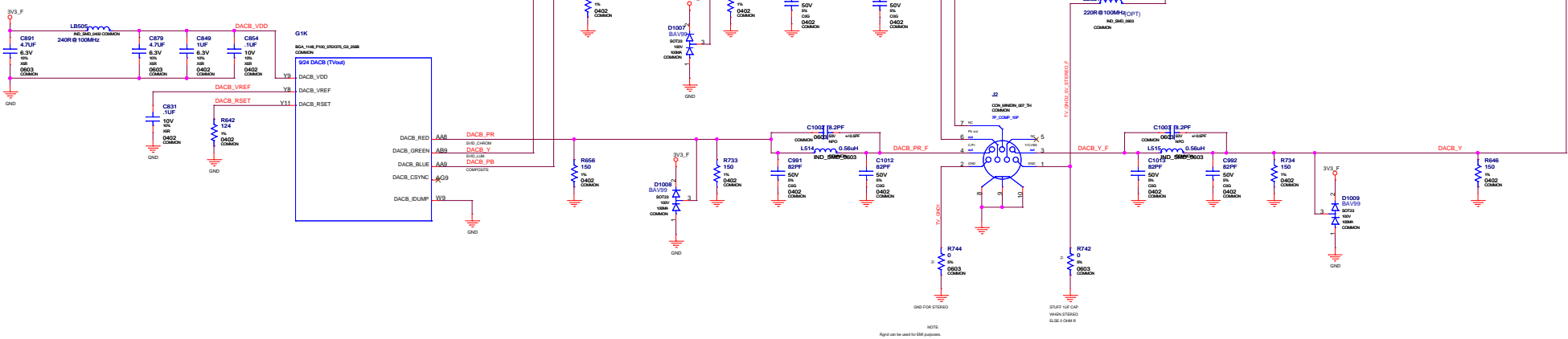
ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC Interface



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PAGE DETAIL	DACB and Stereo Interface

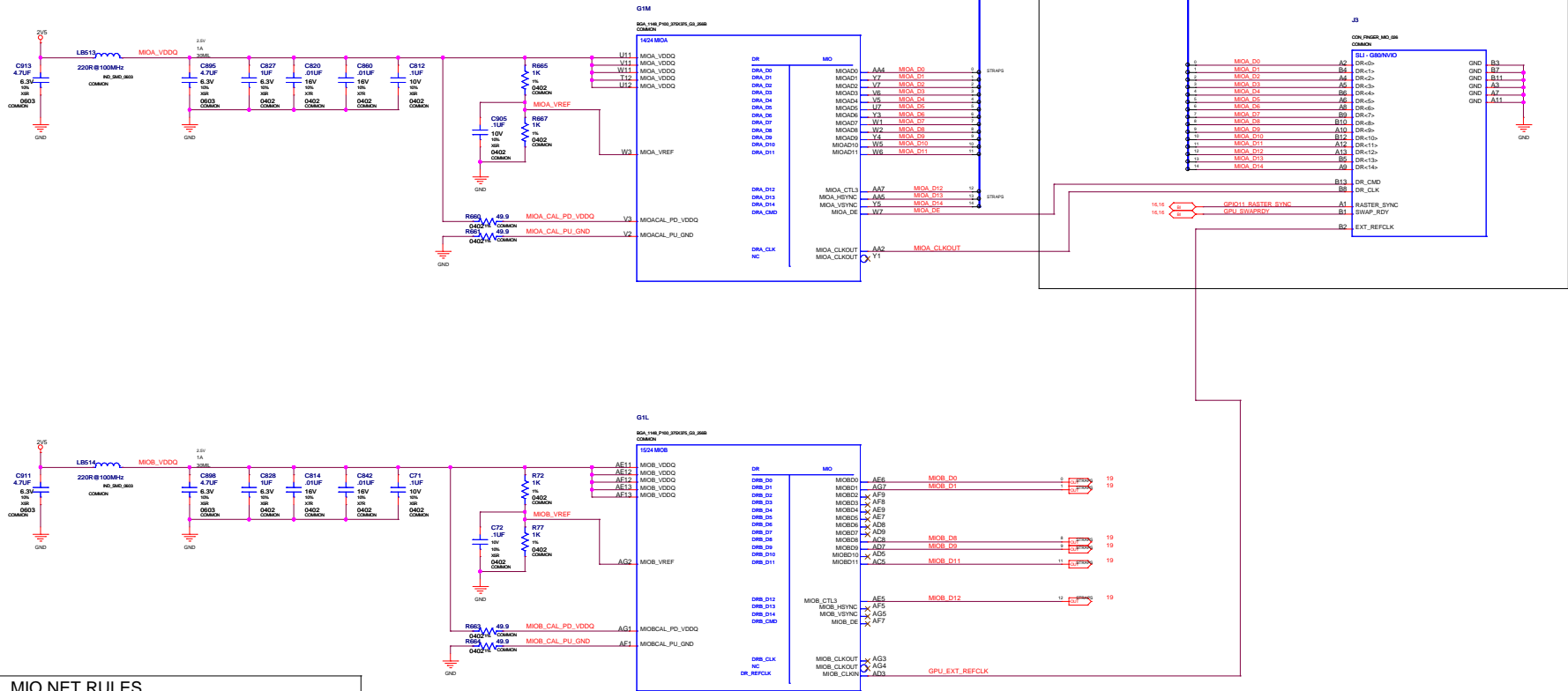
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MIO Feature Connector



MIO NET RULES



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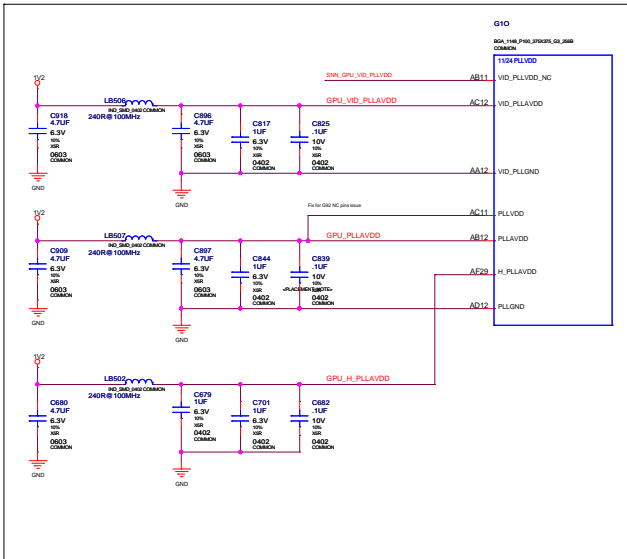
ASSEMBLY PAGE DETAIL P301: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL Multi-use IO(MIO) Interface



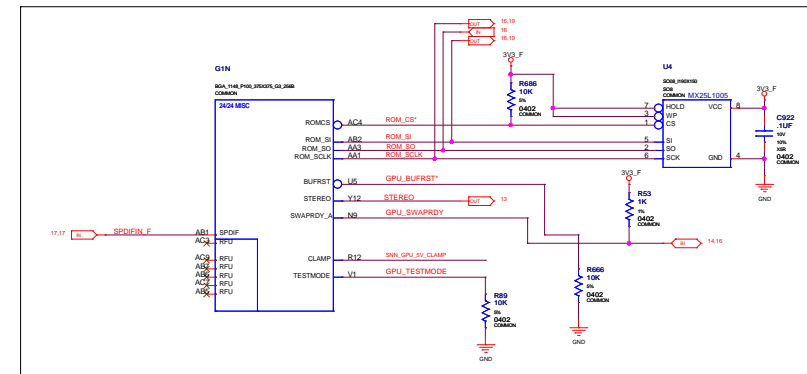
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	A	B	C	D	E	F	G	H	
1	Page15: Display Port (Analogix ANX9802/ANX9805)								
	<div><div><div>* GND jumper should be removed</div><div>* ANX9805 support</div><div>pin 19 - GPVCC to DP mode, from pin 15, grounded on ANX9802 - please GND resistor away from ANX device if needed</div><div>pin 19 - GPVCC, grounded on ANX9802 - please GND resistor away from ANX device if needed</div><div>pin 19 - GND support on FET and padring, grounded on ANX9802 - please GND resistor away from ANX device if needed</div><div>pin 11 - SPVREF - tie to GND, signal stated D1 through internal register</div><div>pin 10 - SPVREF - support for Audio input, grounded on ANX9802 - please GND resistor away from ANX device if needed</div><div>pin 48 - NC - tie to GND</div></div></div>								
2									
3									
4									
5									
ASSEMBLY PAGE DETAIL				P993 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL Display Port					
<div>ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN INACCURACIES OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.</div>									
A	B	C	D	E	F	G	H		
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[illegible][illegible]

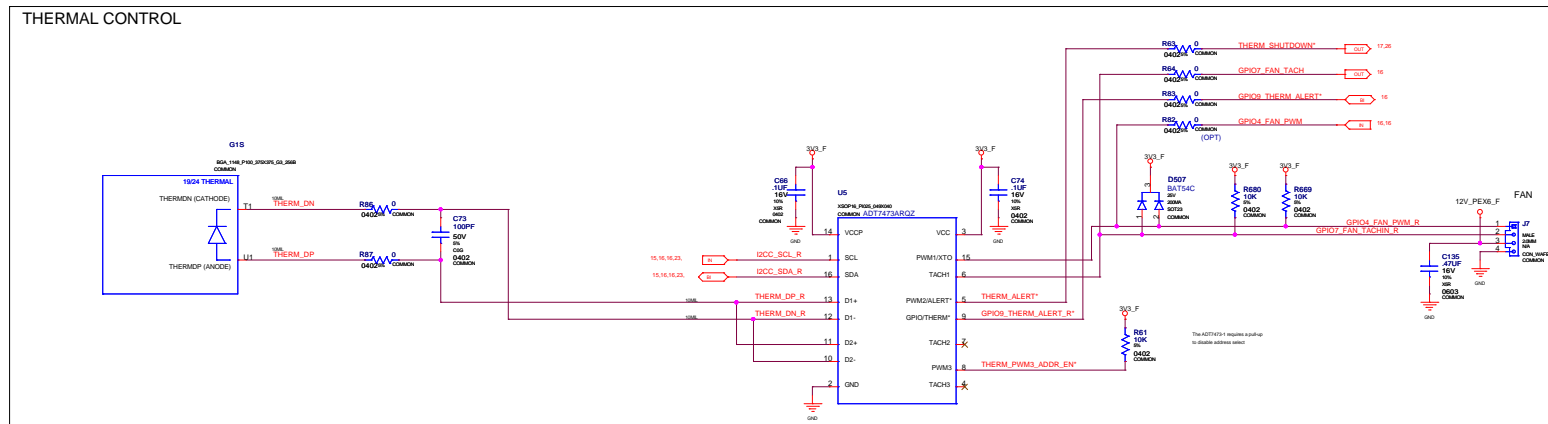
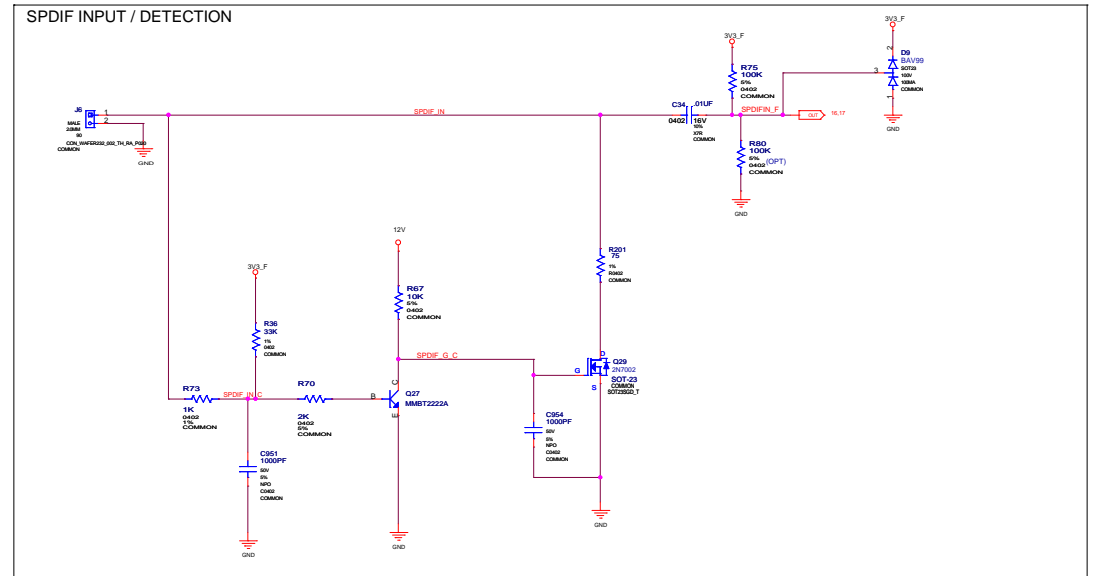
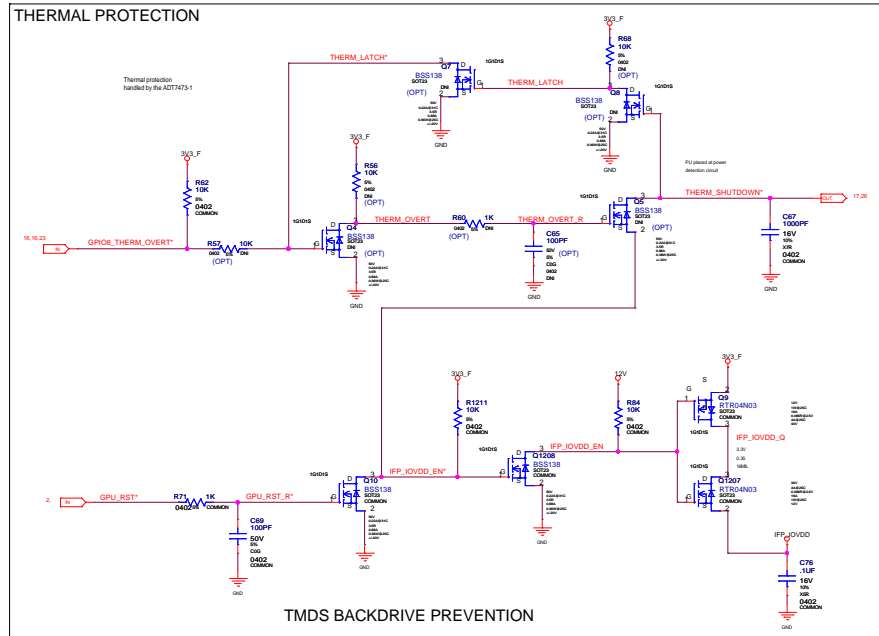
(BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)

[illegible]

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
15,16,17,22	15	UCC_BCL_R	3	NOHM	
15,16,17,22	16	UCC_BCL_R	3	NOHM	
16,19	16	ROM_ID	3	NOHM	
16	16	ROM_CS	3	NOHM	
16,19	16	ROM_BCLK	3	NOHM	
14,16	15	GPU_BKMPDEV	3	NOHM	
16,17	16	GPICH_PAB_PWM	3	NOHM	
16,23	16	GPICH_VREFC	3	NOHM	
16,23	16	GPICH_VREFL	3	NOHM	
16,17	16	GPICH_PAB_TSDM	3	NOHM	
16,17,22	16	GPICH_THERM_OVBEST	3	NOHM	
16,17,22	16	GPICH_THERM_ALERT1	3	NOHM	
		NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH

[illegible]

GPIO	I/O	Function
0	IN	DTI Hopping Detect Switch
1	IN	DTN or DP Hopping Detect Mid
2	IN	Firearmless Interrupt
3	IN	Firearmless GPIOCD Joggle Detect
4	OUT	Fm PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fm Tach Input
8	IN	THERM_ALERT*
9	IN	THERM_ALERT*
10	IN	DisplayPort Interrupt
11	IN	BASTER (GLS) SYNC
12	IN	POWER_ALERT*
13	OUT	DP IC Keypad
14	IN	Firearmless Key

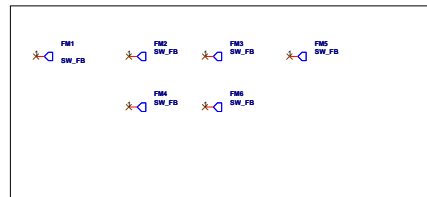
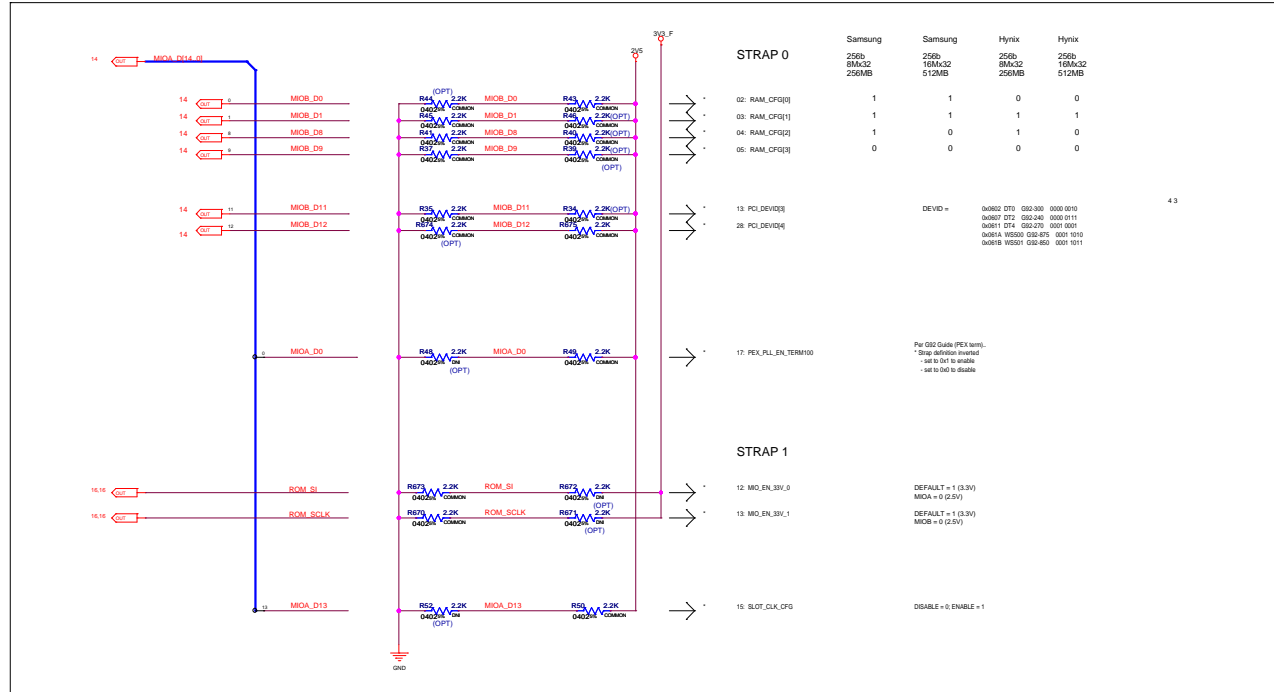


The FAN connector needs to move
as follows for mechanical / ID support:

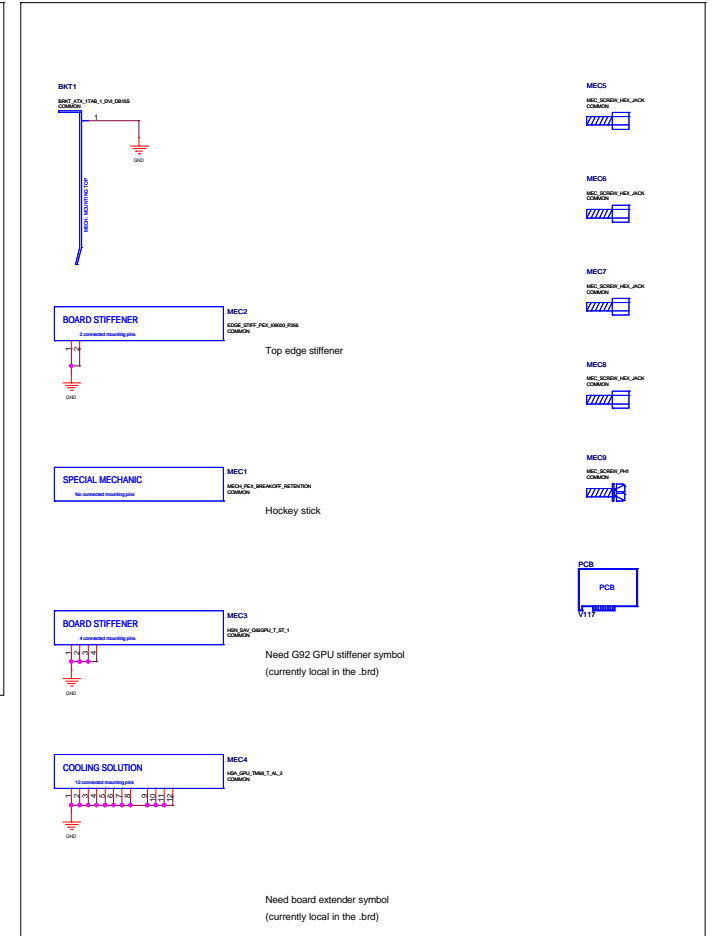
- * move -43mils in Y
- * move +33mils in X

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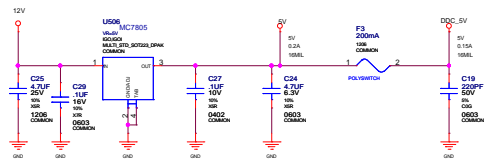
STRAPS



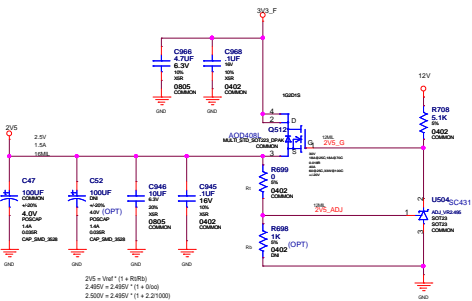
MECHANICAL



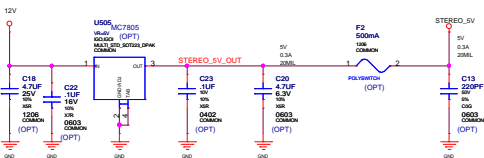
5V and DDC5V Supply



2V5 Supply



5V STEREO Supply



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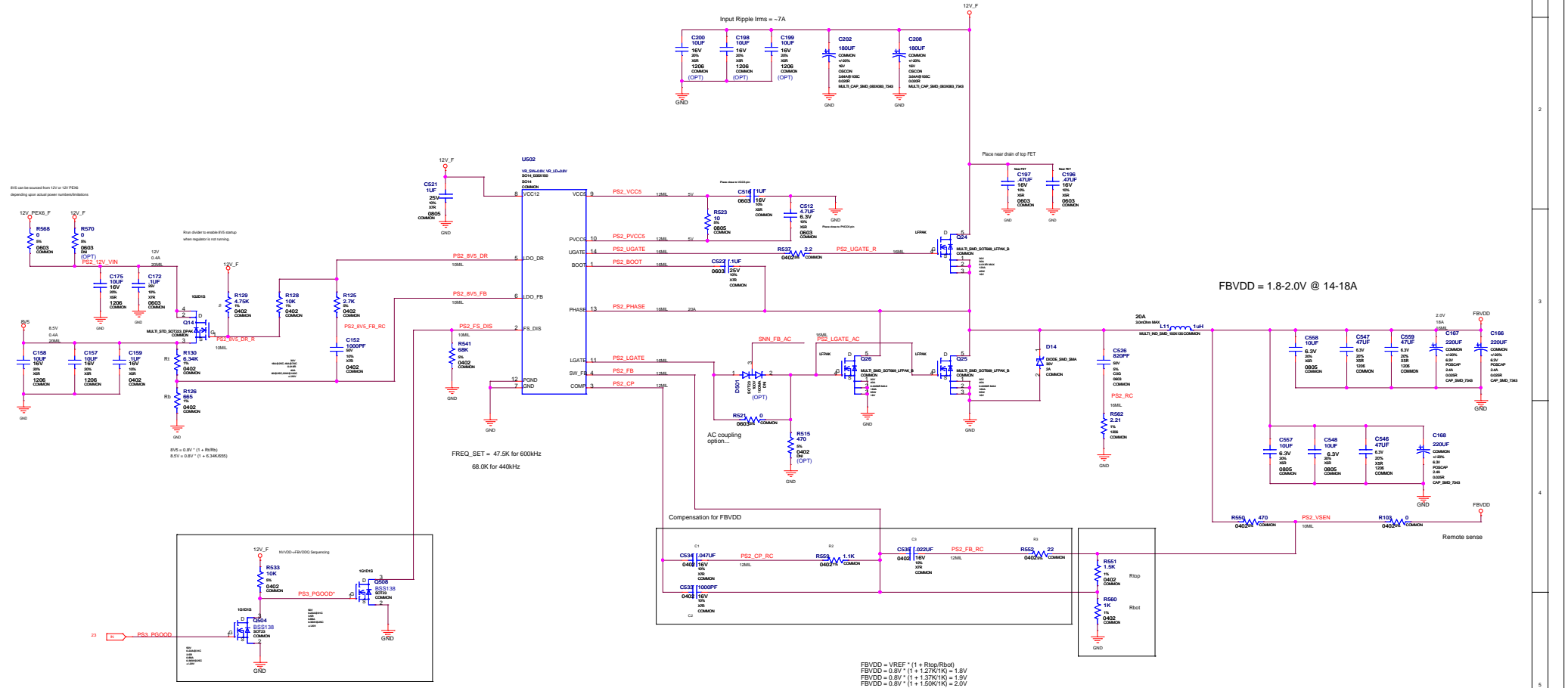
ASSEMBLY PAGE DETAIL P931 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL Power Supply 5V, STEREO_5V, 2V5, DP_PWR



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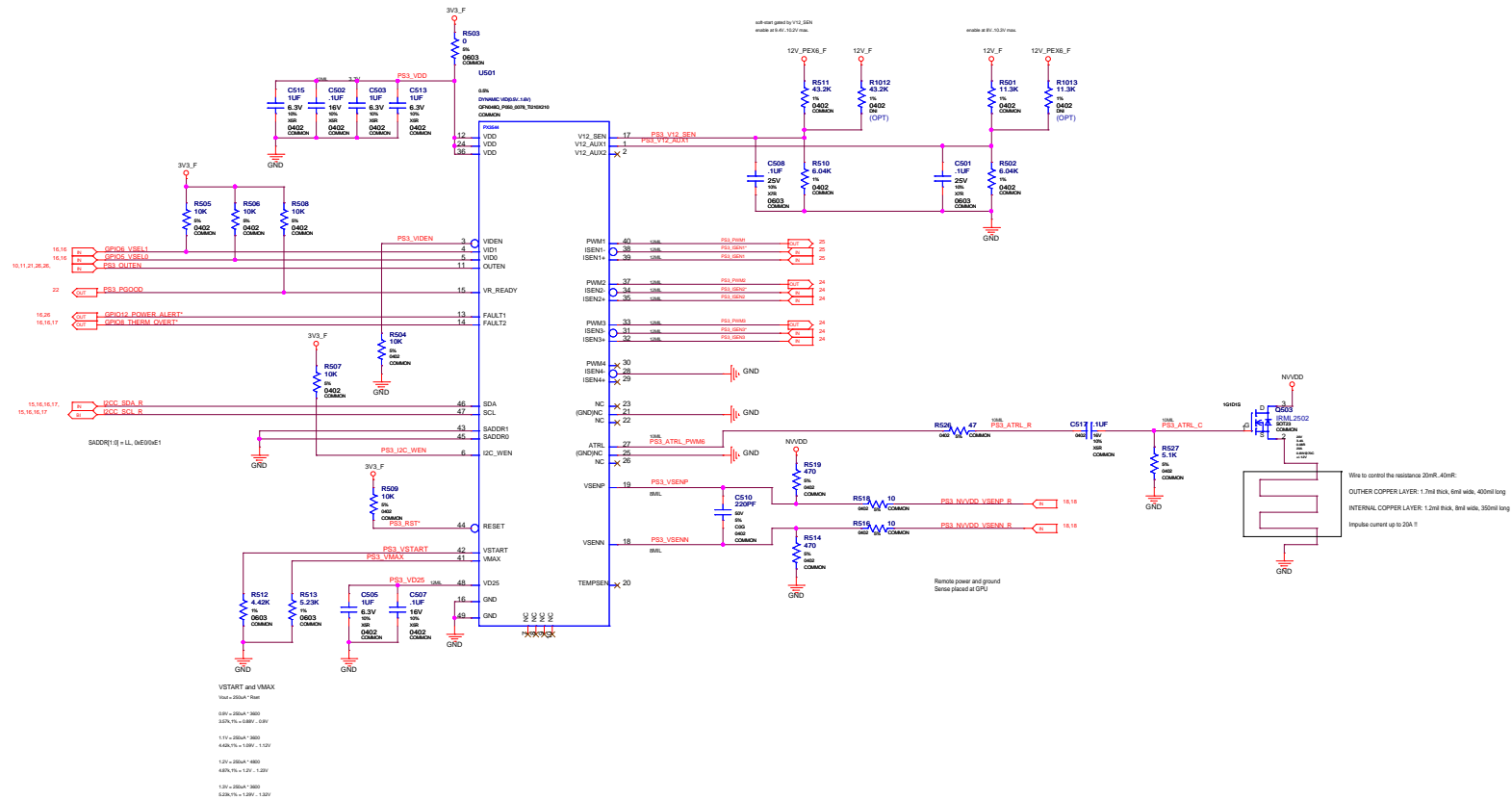


ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: FBVDD/Q, 8V5



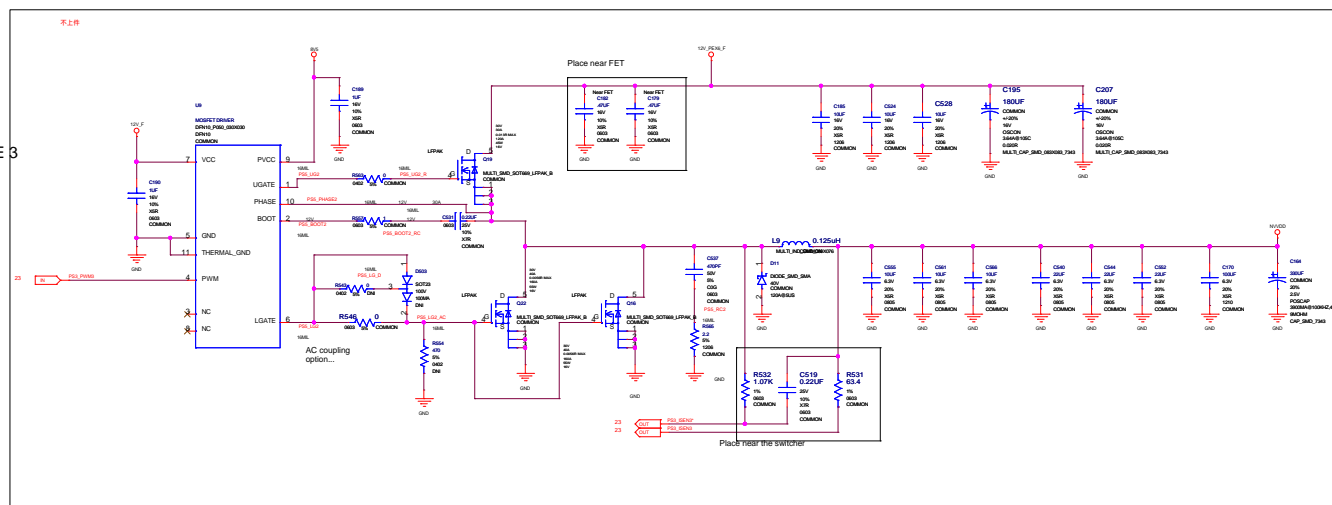
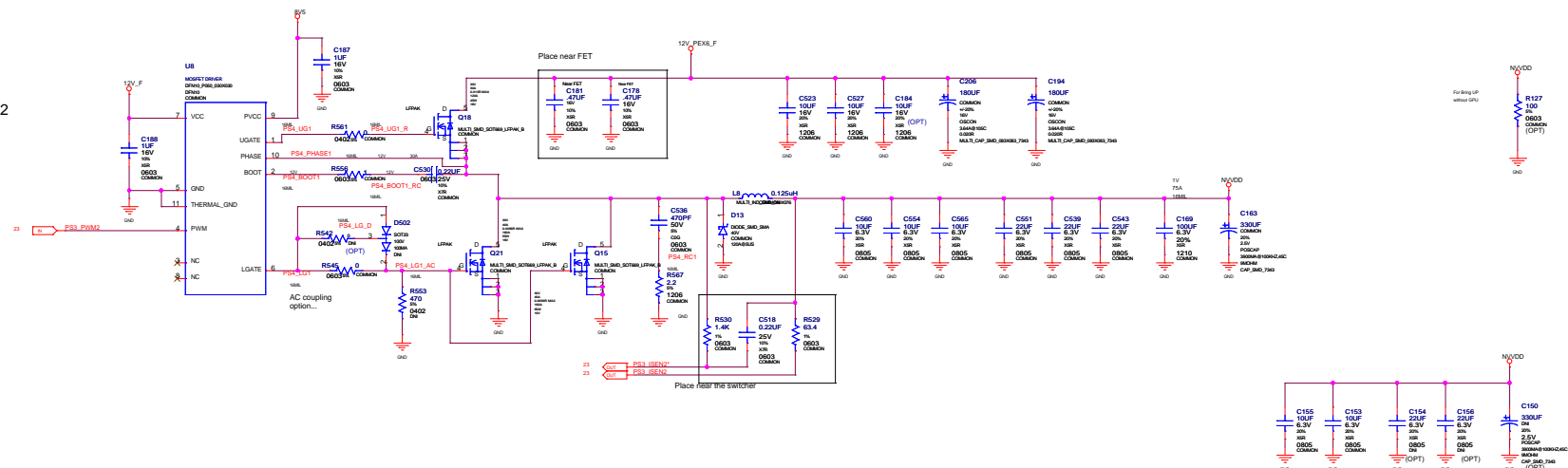
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Wire to control the resistance 20mR, 40mR:
OUTER COPPER LAYER: 1.7mil thick, 6mil wide, 400mil long
INTERNAL COPPER LAYER: 1.2mil thick, 8mil wide, 350mil long
Impulse current up to 20A !!

Remote power and ground
(See also p. 20, 21)

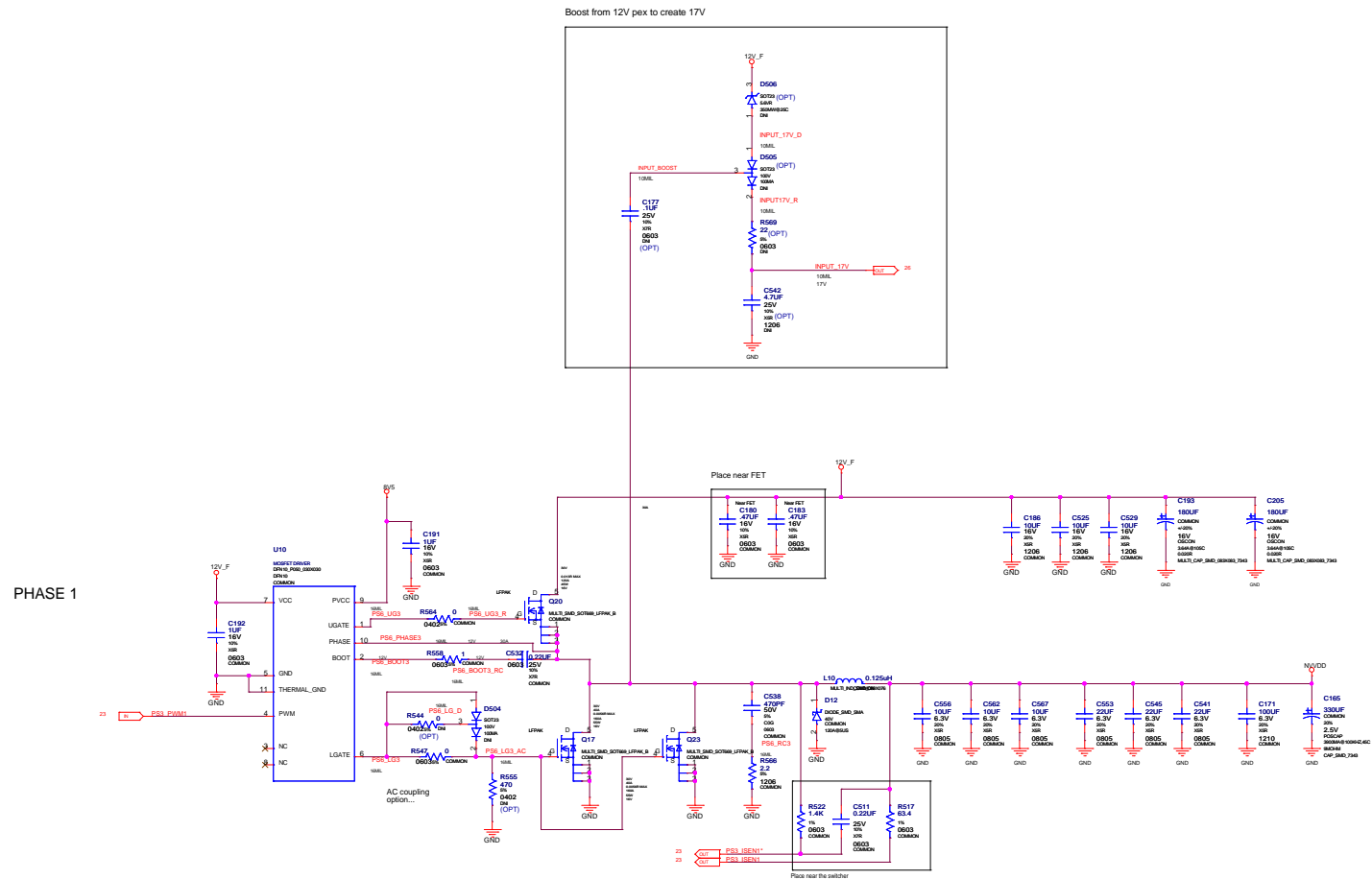


ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVDD Phase 1 & 2



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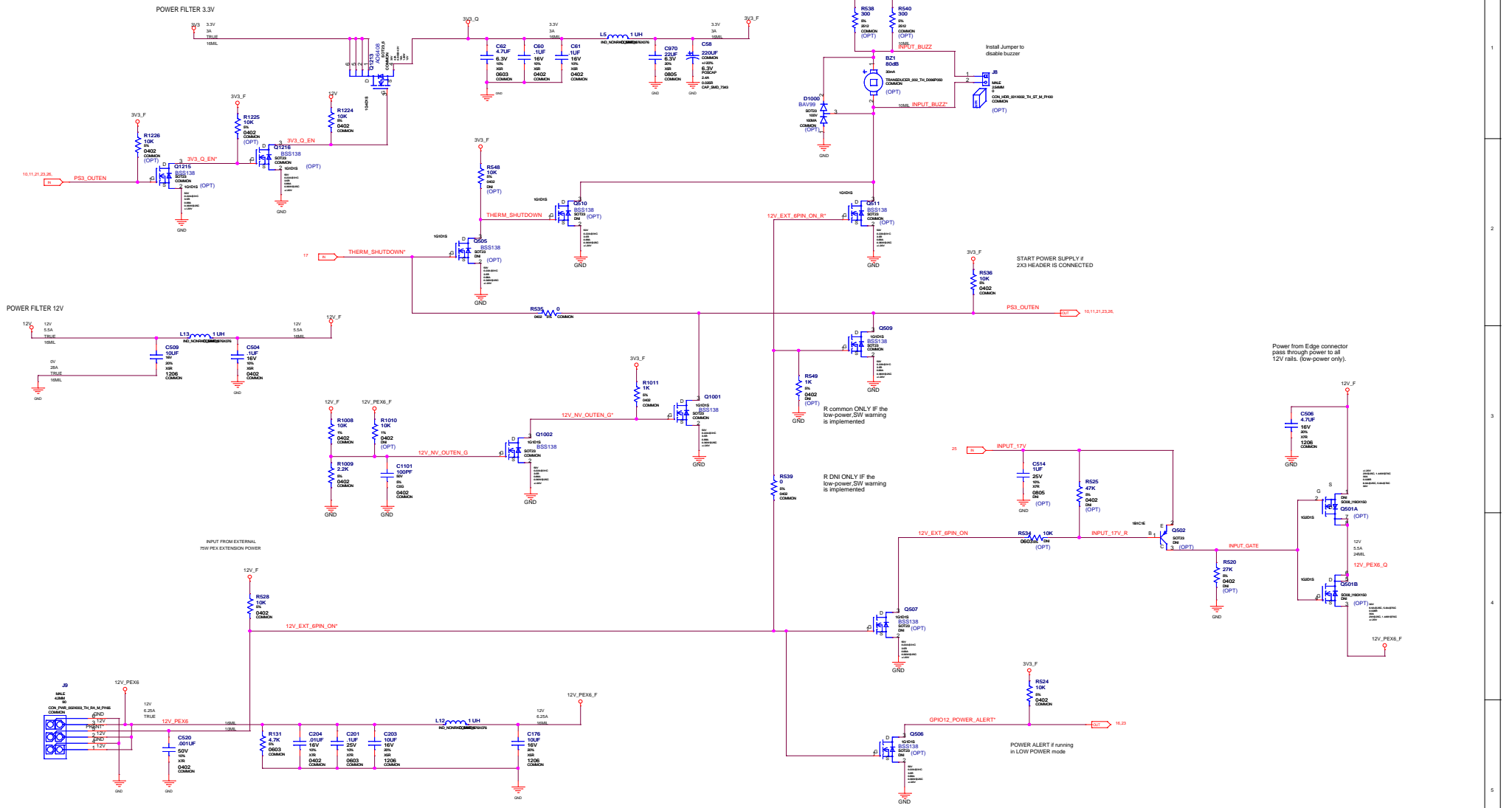
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ASSEMBLY	P933 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVDD Phase 3




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ASSEMBLY PAGE DETAIL P501 BASE LEVEL GENERIC SCHEMATIC ONLY COMMON & NO.3100 ASSEMBLY NOTES AND BOM NOT FINAL Power Supply Filter/Detection of 3V3, 12V, 12V_PEX

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