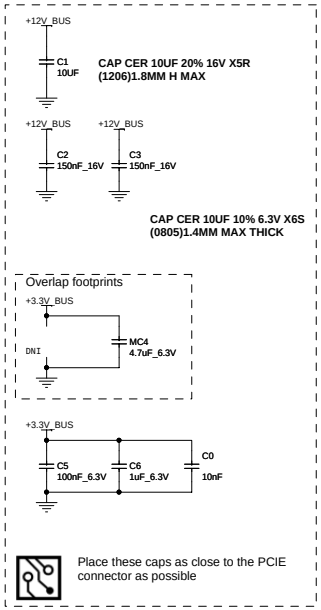
PCI-EXPRESS EDGE CONNECTOR



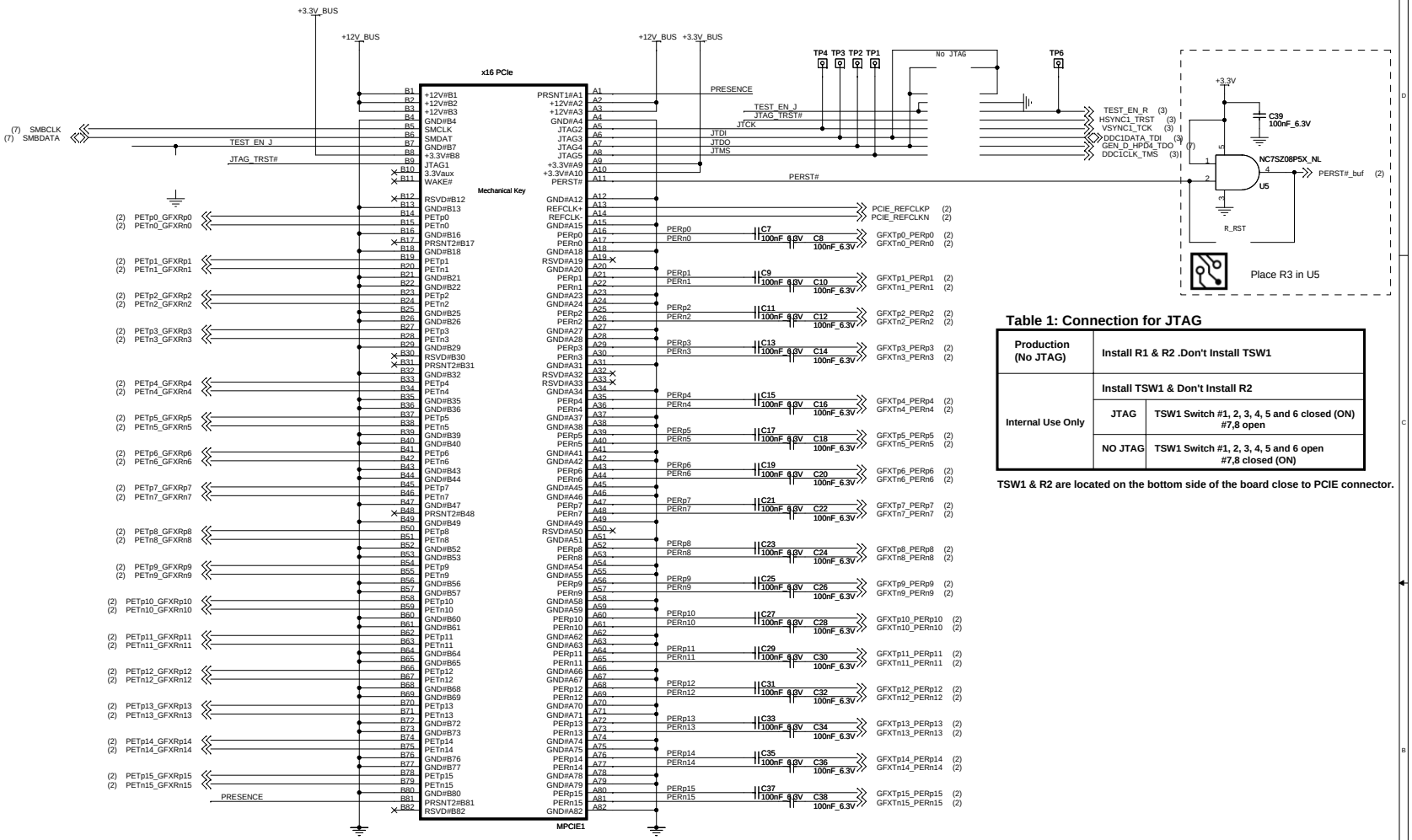


Table 1: Connection for JTAG

Production (No JTAG)	**Install R1 & R2 .Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #7,8 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #7,8 closed (ON)**

TSW1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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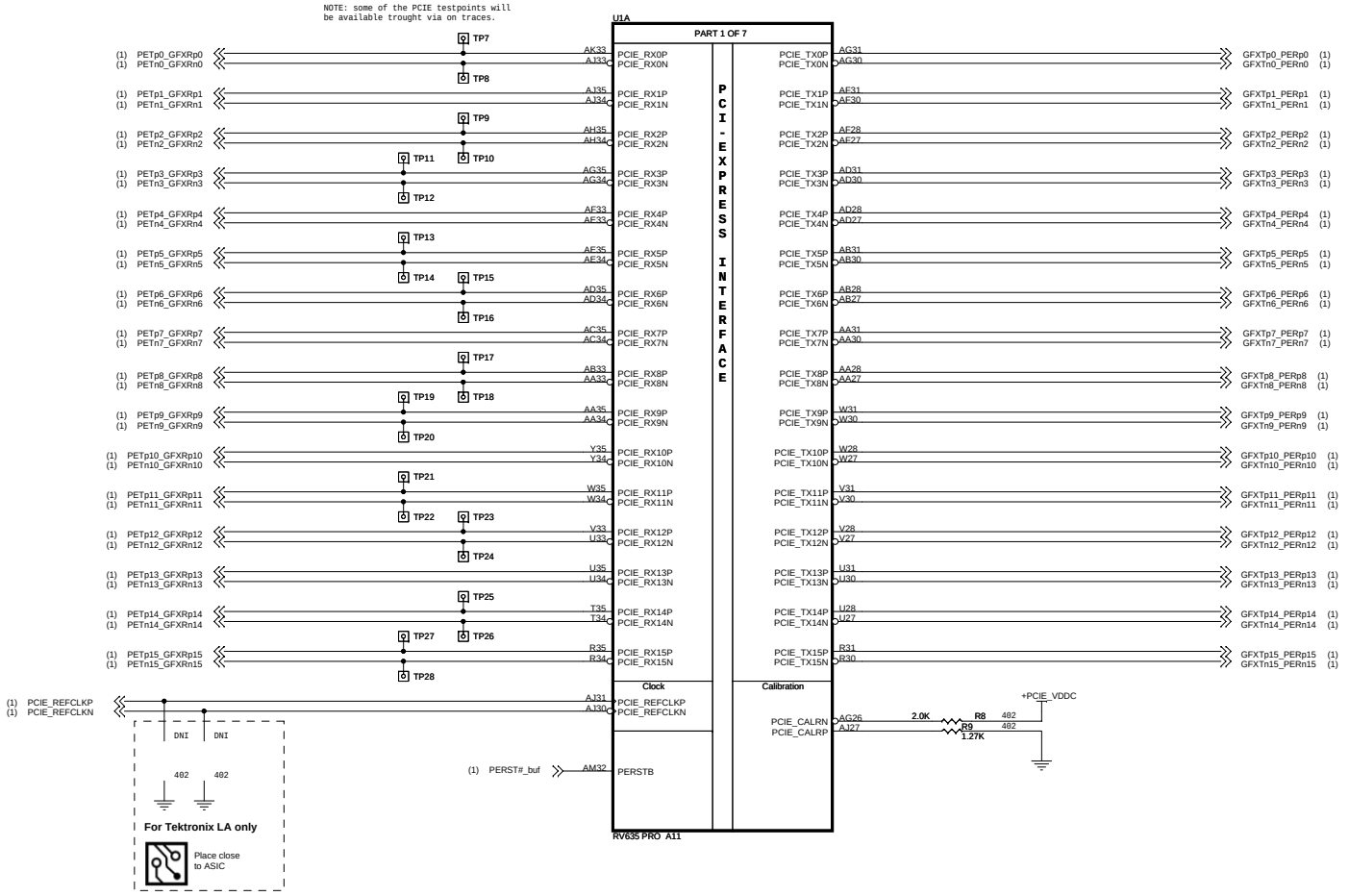
Title	RV635 DDR2 - PCI-E Edge Connector
Doc No.	102-B38101-00



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Title	RV635 DDR2 - ASIC PCIE_Interface
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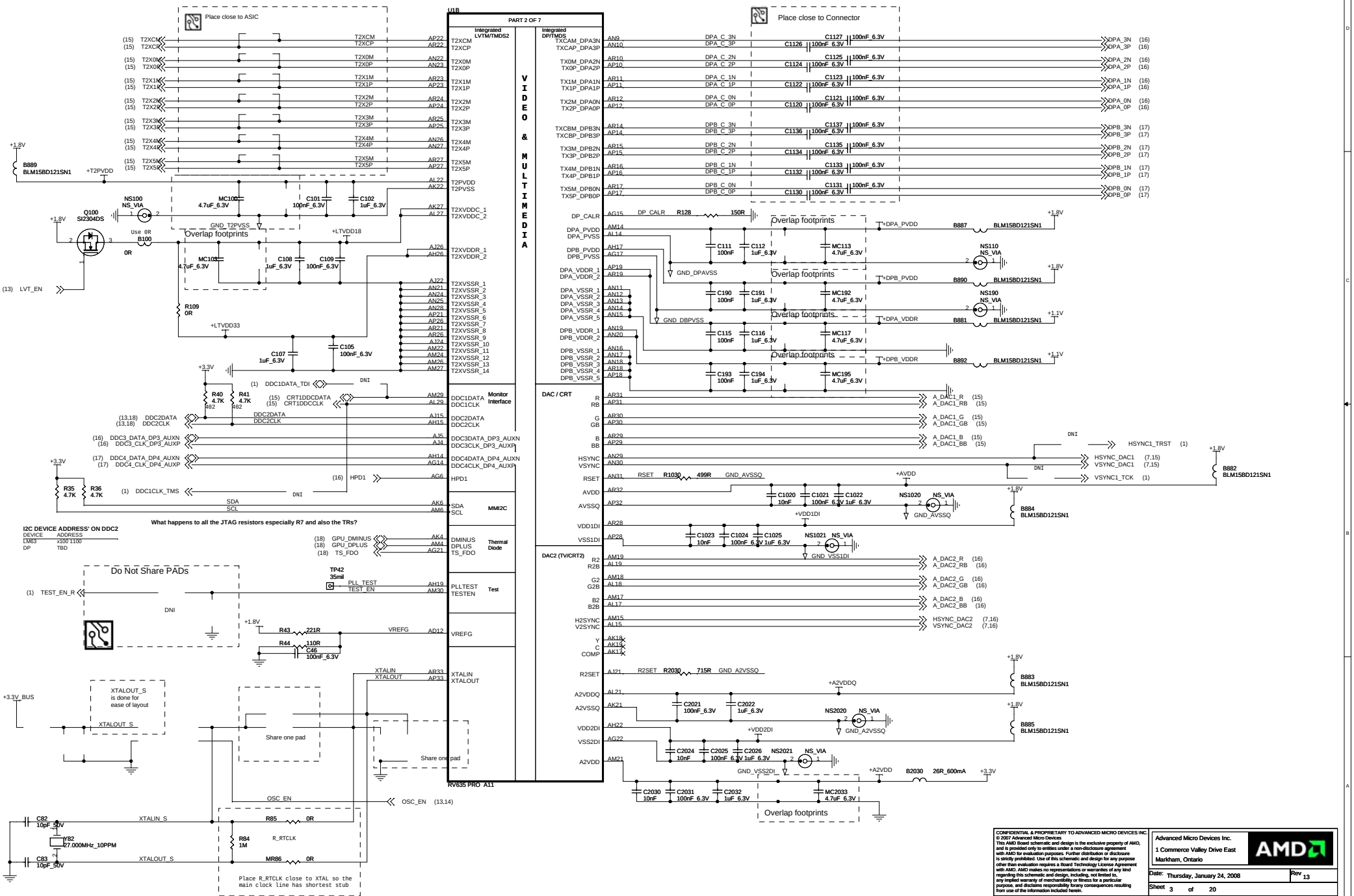
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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Title	RV635 DDR2 - ASIC MAIN
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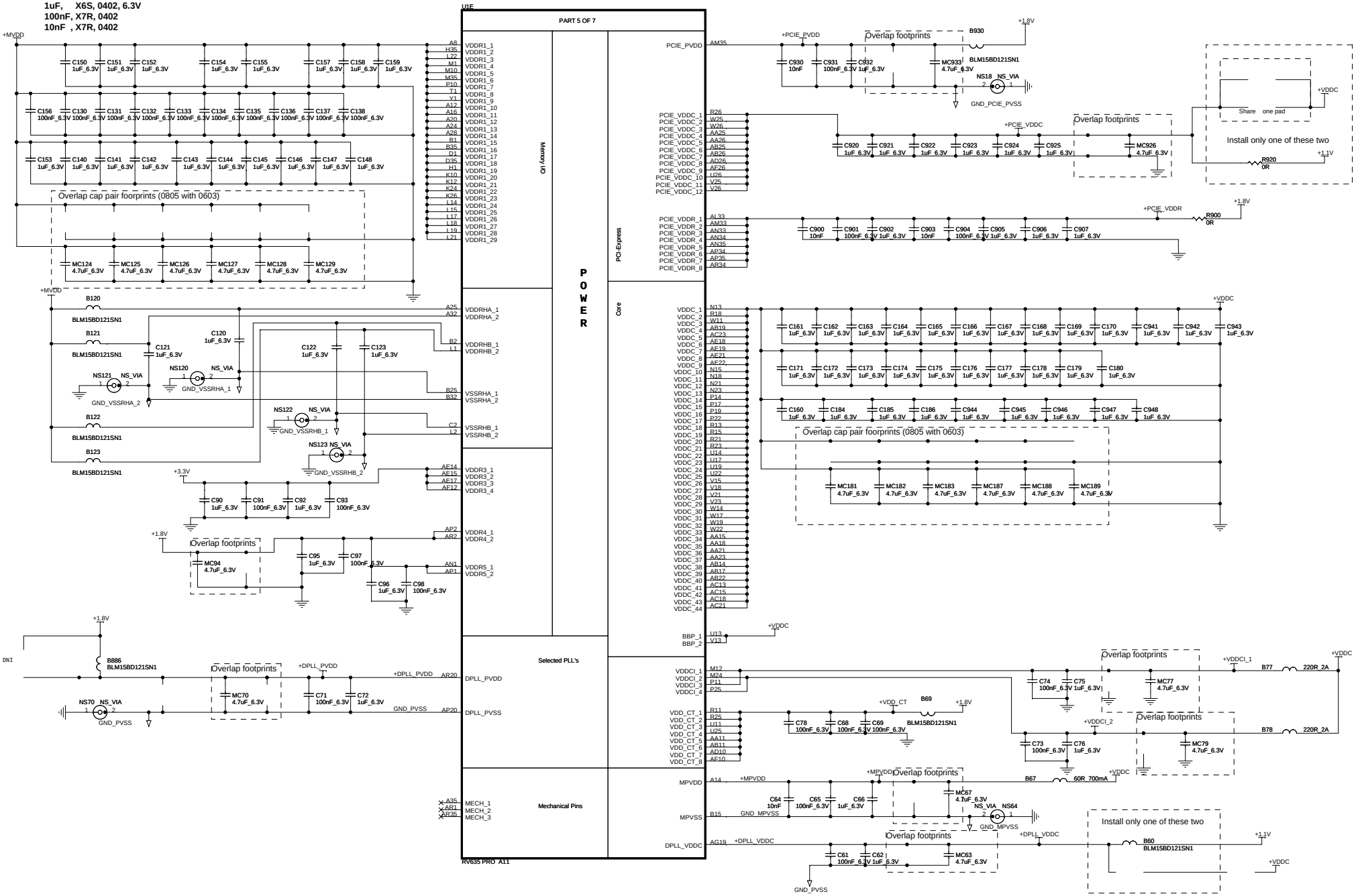
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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Title	RV635 DDR2 - ASIC Power
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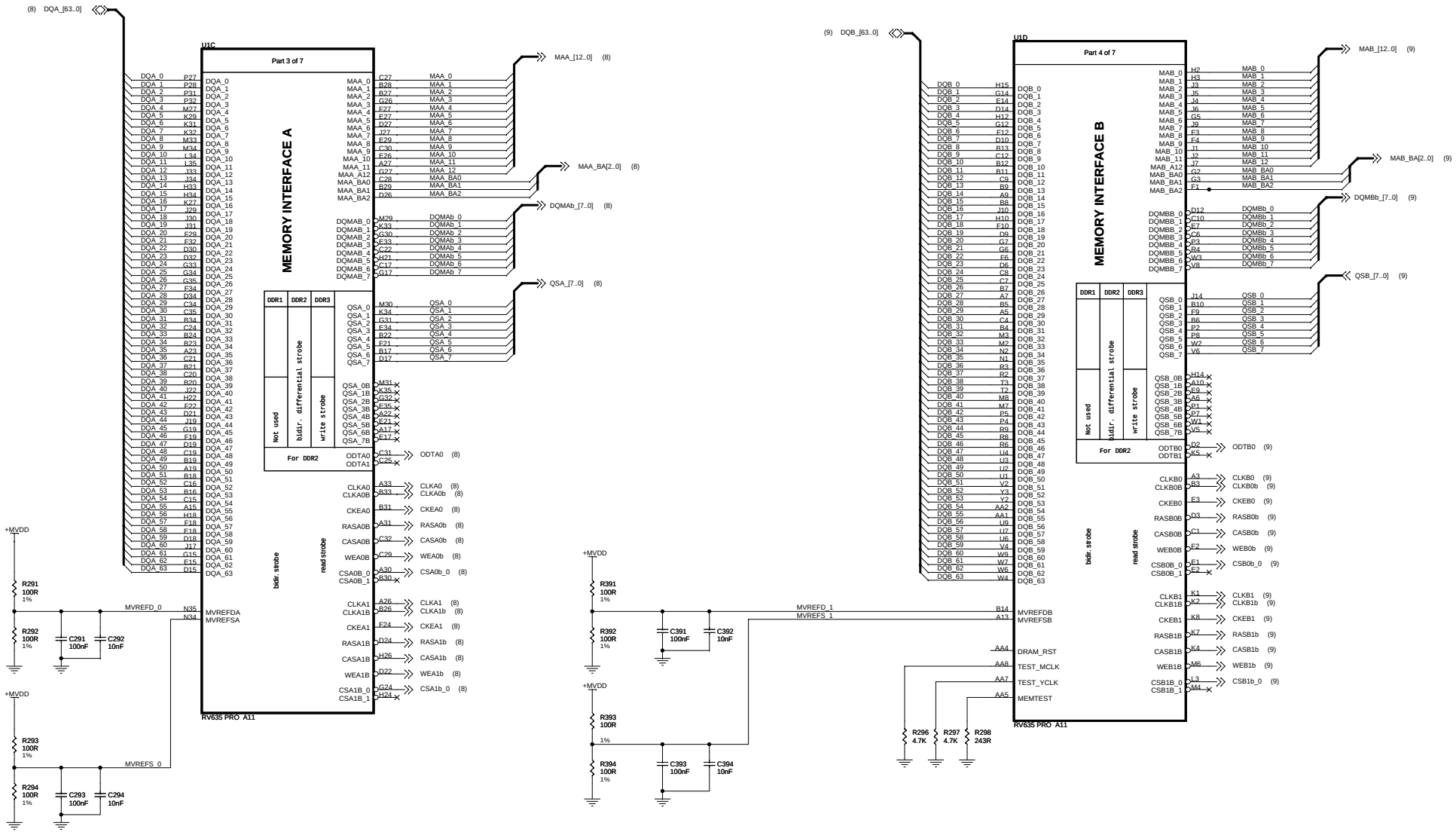

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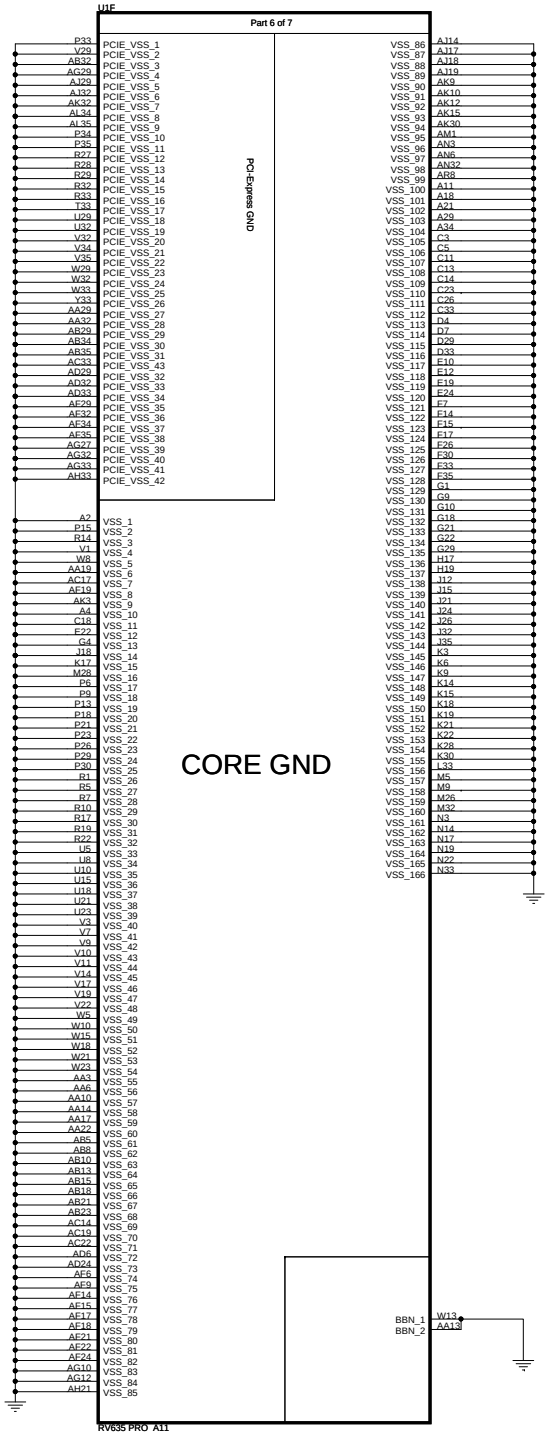
Title RV635 DDR2 - ASIC Memory Interface (Channel A & B)

Doc No. 102-B38101-00



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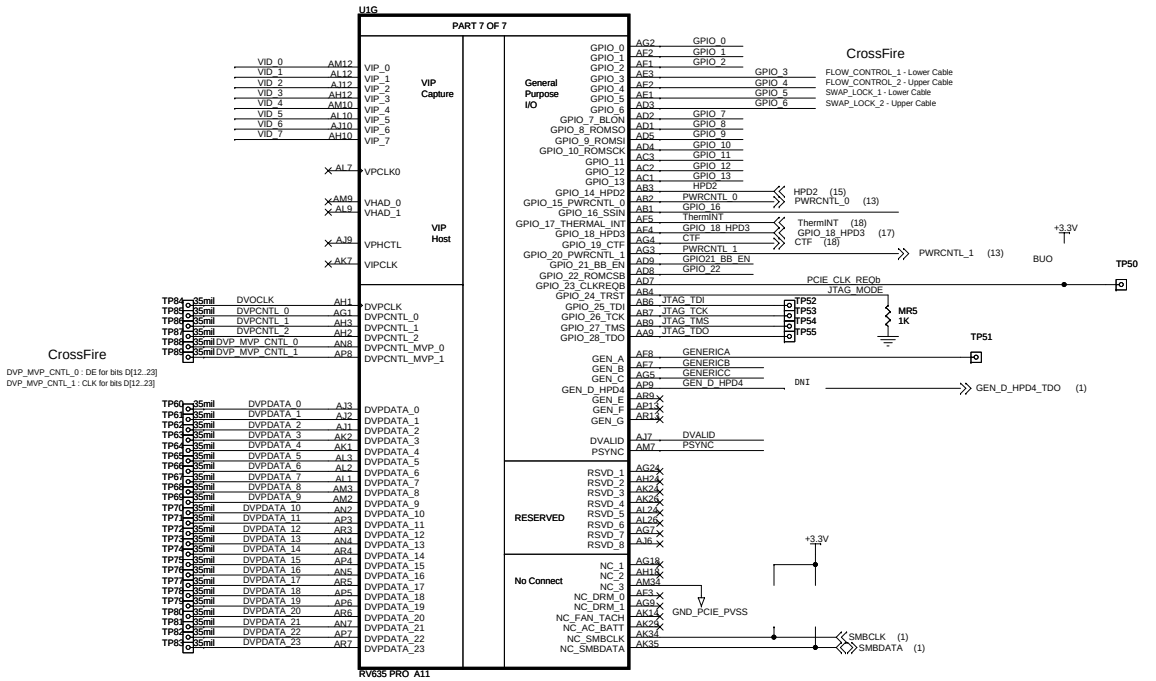
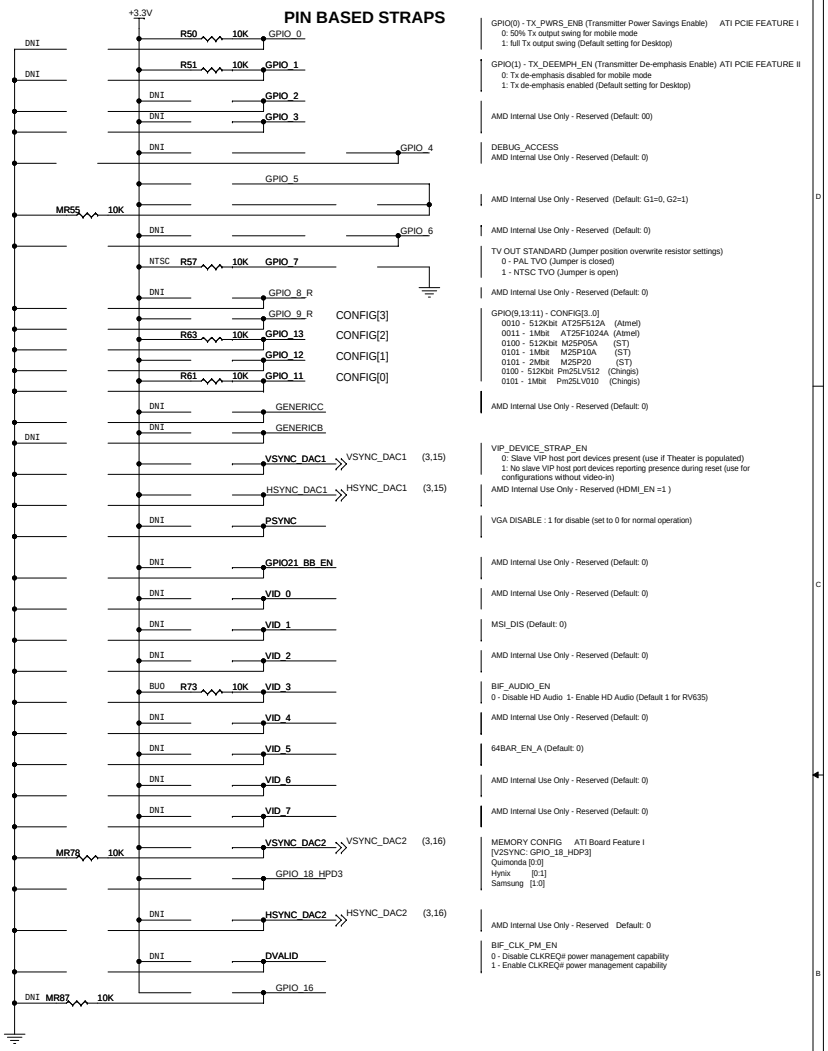
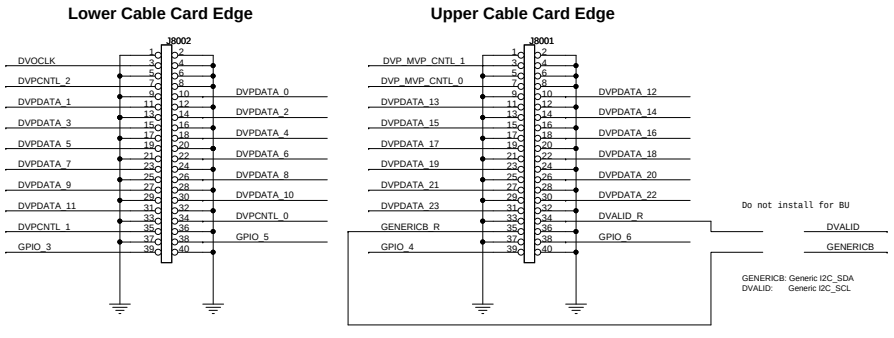
Title RV635 DDR2 - ASIC Grounds

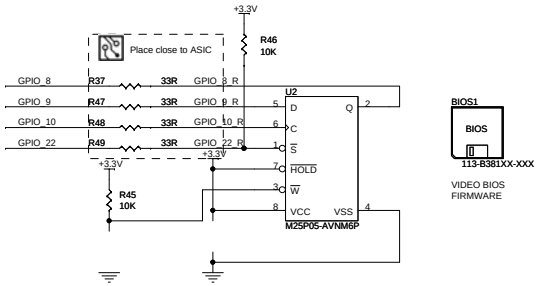
Doc No. 102-B38101-00





CrossFire Card-Edge





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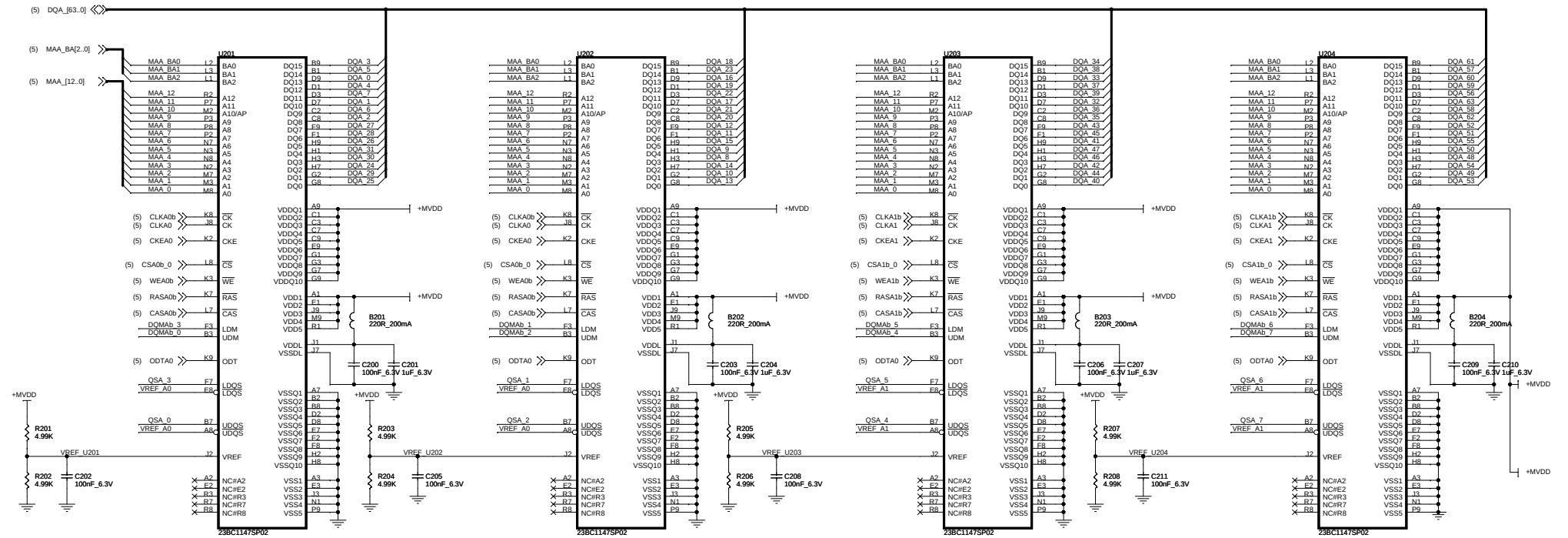
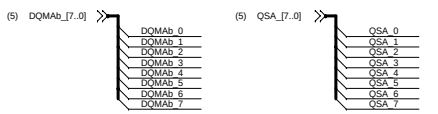
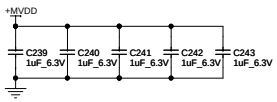
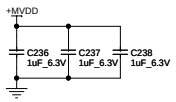
Title RV635 DDR2 - ASIC DVO & GPIOs	Doc No. 102-B38101-00

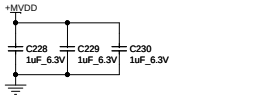
CHANNEL A: 128MB/256MB DDR2

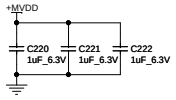


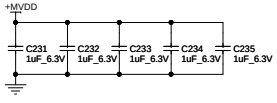


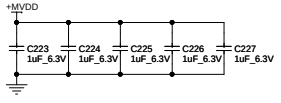


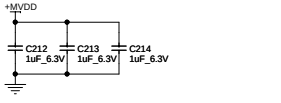


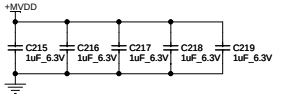


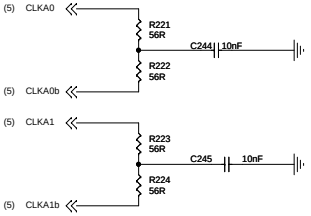


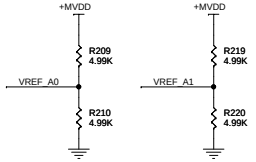












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Title	RV635 DDR2 - MEM CH A
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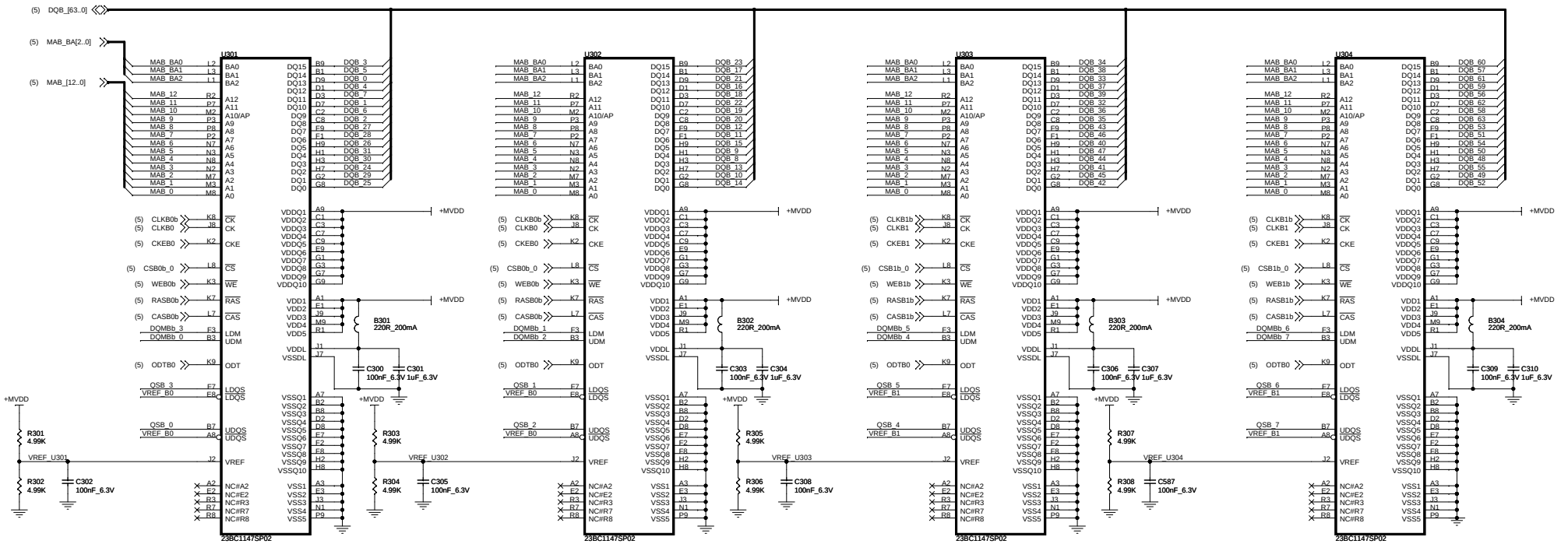
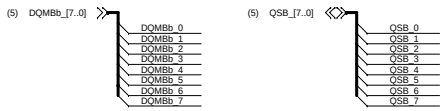
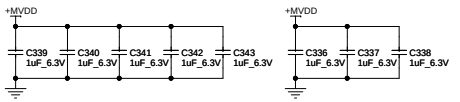
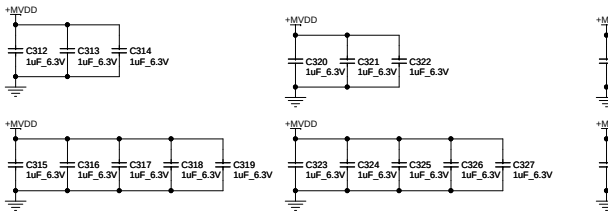
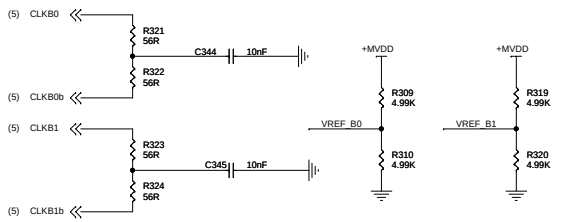
CHANNEL B: 128MB/256MB DDR2











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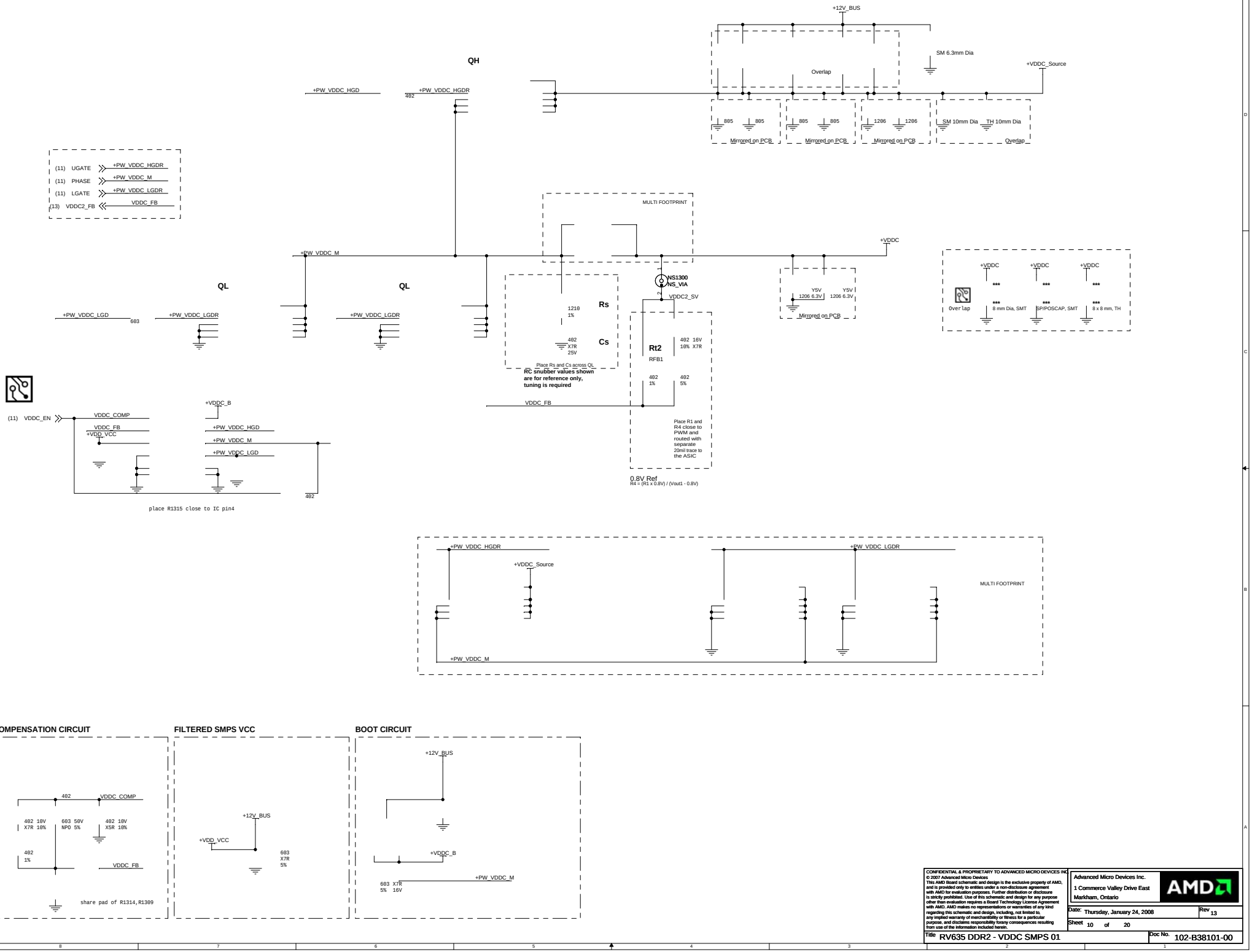

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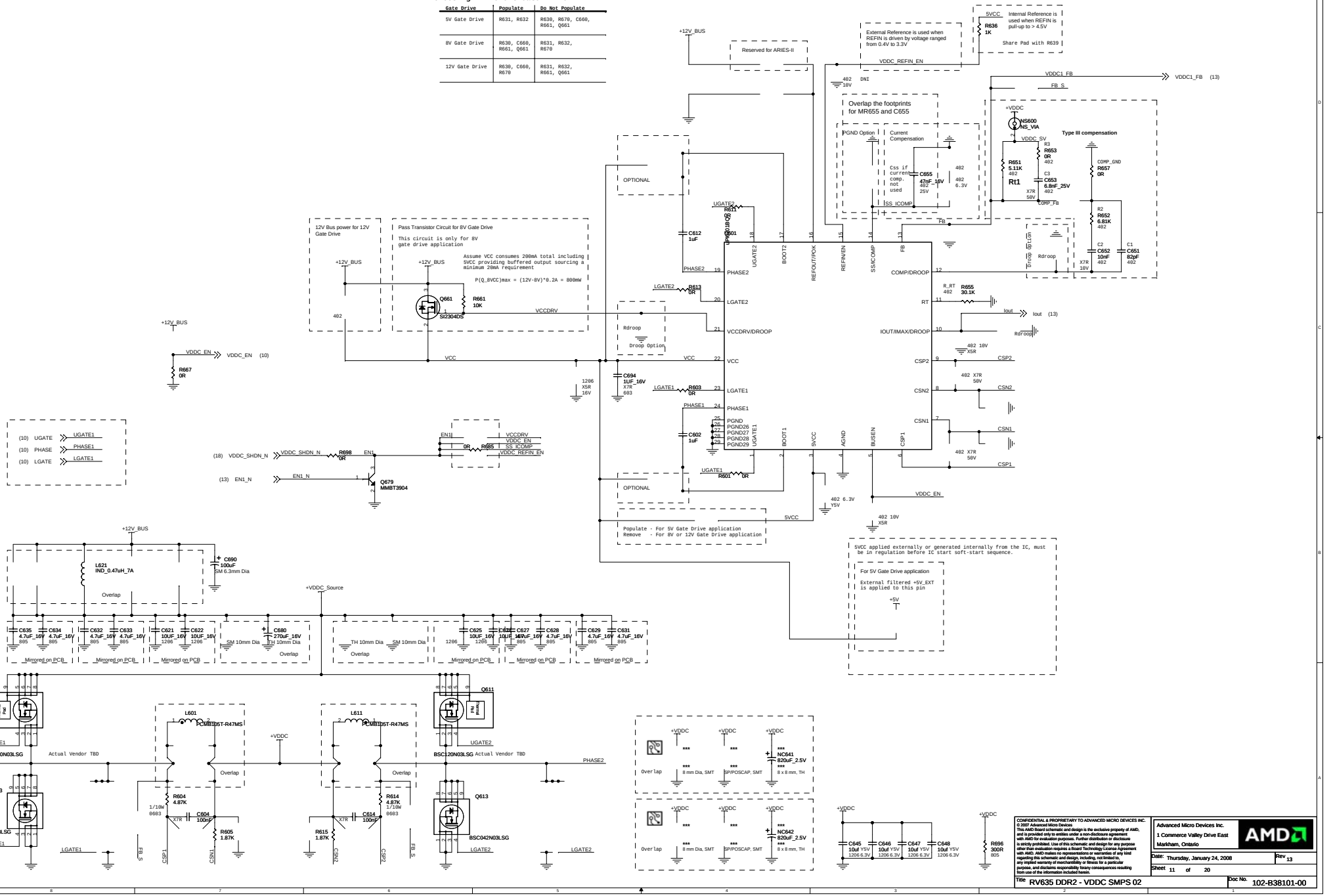
Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661



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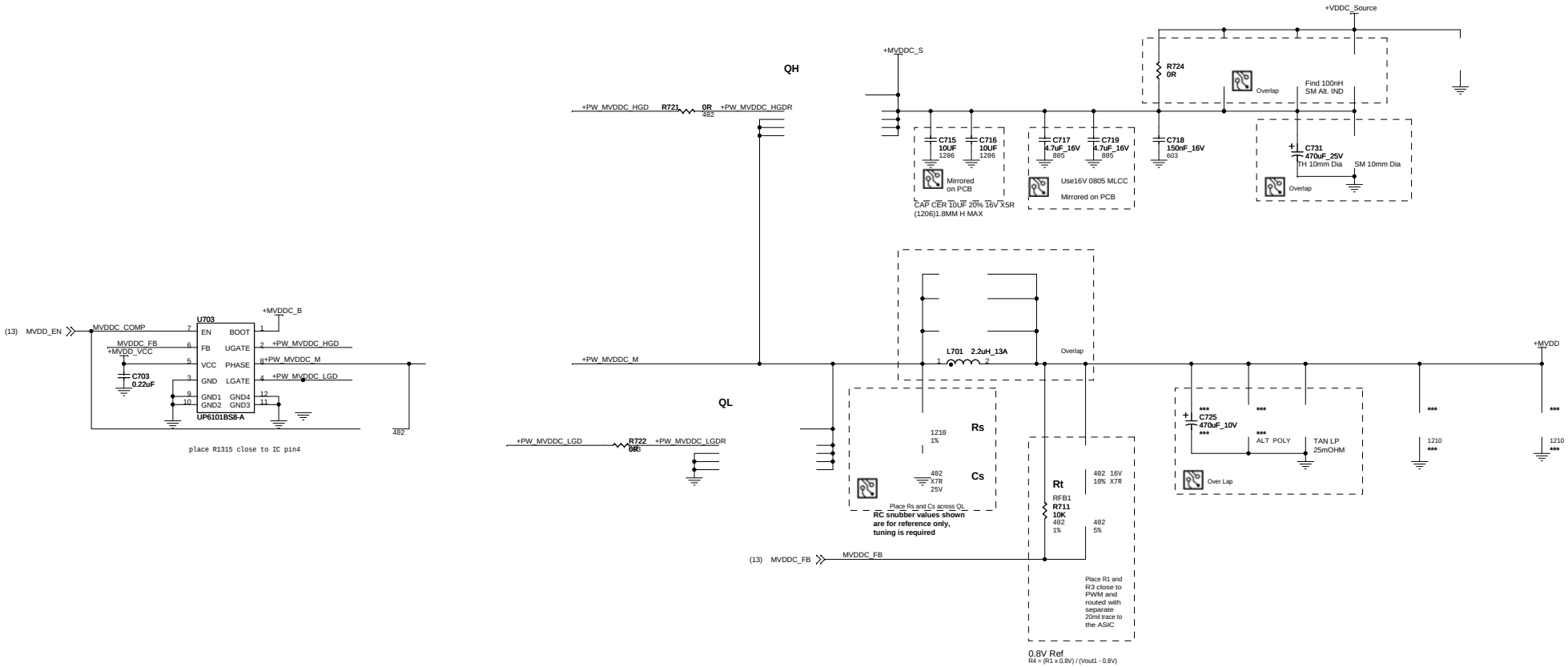
Title	RV635 DDR2 - VDDC SMPS 02
Doc No.	102-B38101-00



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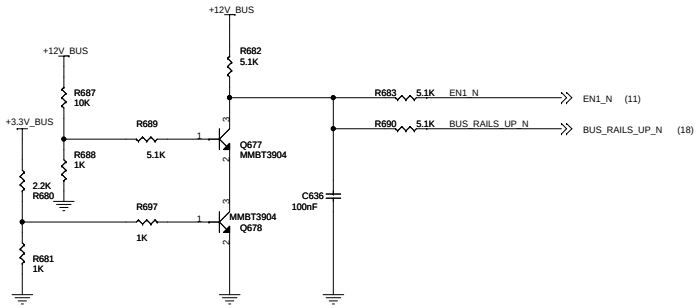
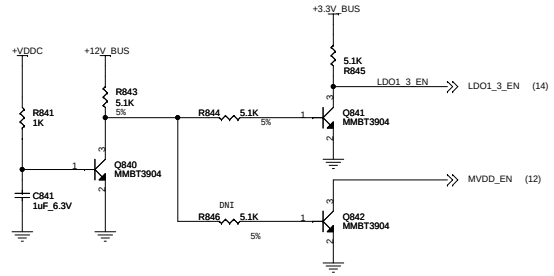
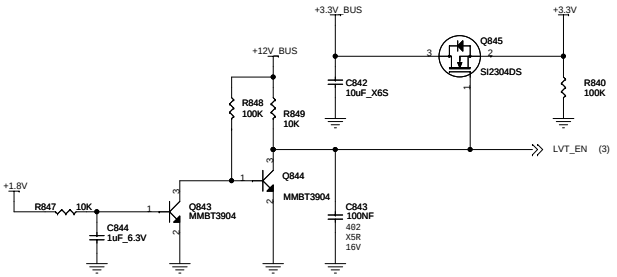
Title	RV635 DDR2 - MVDD SMPS 01
Doc No.	102-B38101-00

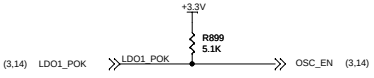
Power up Sequencing



VDDC Enable Circuit





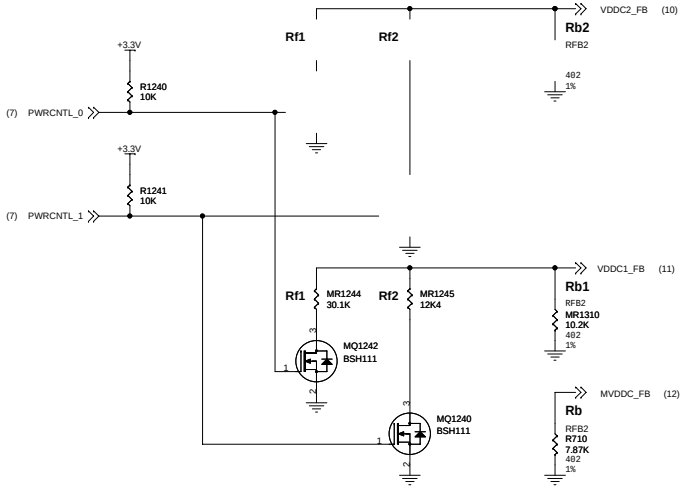


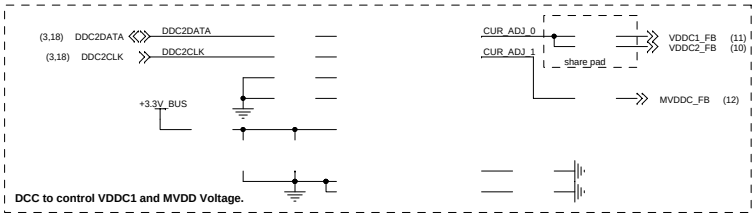
Power Play

VDDC Voltage Settings Using GPIOs (for VDDC1 Dual Phase)

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1=42.2K Rf2=20.5K	Rf1= Rf2=	Rf1= Rf2=	
0	0	0.9V			
0	1	1.00V			
1	0	1.15V			
1	1	1.25V			Power-up Default

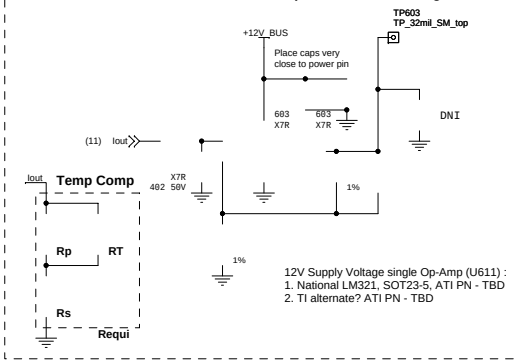
```
Vout = Vref * (1+Rt/Rb)
VDDC1 (Dual Phase):   Vref = 0.6V, Rt = 5.11K
VDDC2 (Single Phase): Vref = 0.8V, Rt = 10K
MVDDC (Single Phase): Vref = 0.8V, Rt = 10K
```





DCC to control VDDC1 and MVDD Voltage.

Buffered VDDC Output Current Monitoring



12V Supply Voltage single Op-Amp (U611) :
1. National LM321, SOT23-5, ATI PN - TBD
2. TI alternate? ATI PN - TBD

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For Testing purposes only

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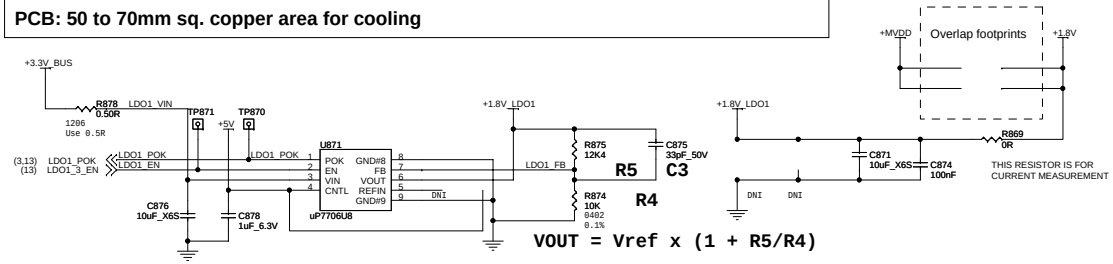
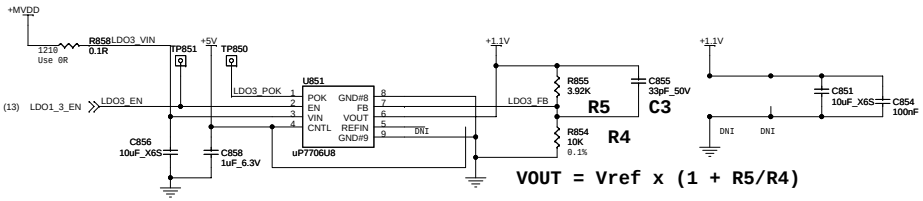
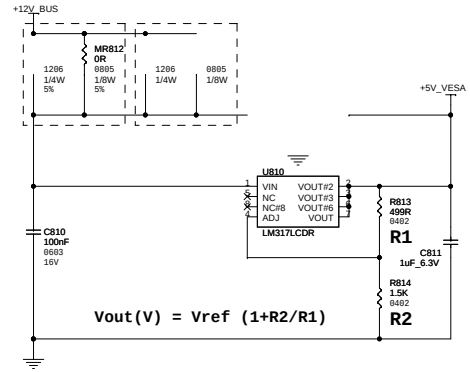
Regulators for +5V, +5V_VESA and +5V_VESA2

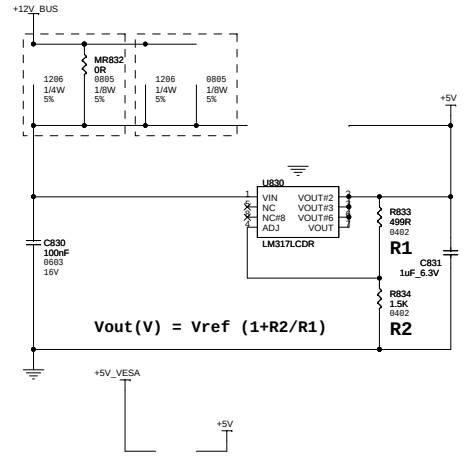
LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #3: Vin = +1.45V to 2.0VMAX Vout = +1.1V +/- 2% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling







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Title RV635 DDR2 - Linear Regulators

Doc No. 102-B38101-00

See BOM for qualified filters

(3) A_DAC1_R — R1001 71.5R — L1001 47nH — A_R_DAC1_M — L1004 0R
(3) A_DAC1_RB — R1027 37.4R
(3) A_DAC1_G — R1002 75R — L1002 47nH — A_G_DAC1_M — L1005 0R
(3) A_DAC1_GB — R1028 37.4R
(3) A_DAC1_B — R1003 75R — L1003 47nH — A_B_DAC1_M — L1006 0R
(3) A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

For ESD Protection

+3.3V
+5V_VESA
R1012 0R
+5V_DAC1_VESA
Overlap pads

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

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(3) CRT1DDCDATA — R1004 10K (+3.3V) — R1005 2.2K (+5V) — Q1001 BSH111 — DDCDATA_DAC1_5V — R1006 33R — DDCDATA_DAC1_R
(3) CRT1DDCCLK — R1007 10K (+3.3V) — R1008 2.2K (+5V) — Q1002 BSH111 — DDCCLK_DAC1_5V — R1009 33R — DDCCLK_DAC1_R

(3,7) HSYNC_DAC1 — C1999 100nF 6.3V (+5V) — U1999A 74VHC125 — HSYNC_DAC1_B — R1010 10R — HSYNC_DAC1_R
(3,7) VSYNC_DAC1 — U1999B 74VHC125 — VSYNC_DAC1_B — R1011 10R — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

(7) HPD2 — Q1021 MMBT3904 — R1022 10K — HPD_DVI2 — R1023 10K (+3.3V)

+5V_DAC1_VESA

J1001 DVI_CONNECTOR

(3) T2X2M	1	TMDS Data2-
(3) T2X2P	2	TMDS Data2+
	3	TMDS Data2/4 Shield
(3) T2X4M	4	TMDS Data4-
(3) T2X4P	5	TMDS Data4+
DDCCLK_DAC1_R	6	DDC Clock
DDCDATA_DAC1_R	7	DDC Data
VSYNC_DAC1_R	8	Analog VSYNC
(3) T2X1M	9	TMDS Data1-
(3) T2X1P	10	TMDS Data1+
	11	TMDS Data1/3 Shield
(3) T2X3M	12	TMDS Data3-
(3) T2X3P	13	TMDS Data3+
	14	+5V Power
	15	GND (for +5V)
HPD_DVI2	16	Hot Plug Detect
(3) T2X0M	17	TMDS Data0-
(3) T2X0P	18	TMDS Data0+
	19	TMDS Data0/5 Shield
(3) T2X5M	20	TMDS Data5-
(3) T2X5P	21	TMDS Data5+
	22	TMDS Clock Shield
(3) T2XCP	23	TMDS Clock+
(3) T2XCM	24	TMDS Clock-
A_R_DAC1_F	C1	Analog Red
A_G_DAC1_F	C2	Analog Green
A_B_DAC1_F	C3	Analog Blue
HSYNC_DAC1_R	C4	Analog HYNC
	C5	Analog GND
	C6	Analog GND#C6
	25	CASE
	26	CASE#26
	27	CASE#27
	28	CASE#28
	29	CASE#29
	30	CASE#30

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See BOM for qualified filters

(3) A_DAC2_R — 402 — 402 — A_R_DAC2_M — 402
(3) A_DAC2_RB — 402 — 402
(3) A_DAC2_G — 402 — 402 — A_G_DAC2_M — 402
(3) A_DAC2_GB — 402 — 402
(3) A_DAC2_B — 402 — 402 — A_B_DAC2_M — 402
(3) A_DAC2_BB — 402 — 402

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R

+3.3V
+5V_VESA
+5V_VESA
+5V_DAC2_VESA
Overlap pads

For ESD Protection

603

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

+5V
(3) DDC3_DATA_DP3_AUXN — 402 DDCDATA_DAC2_5V — 402 DDCDATA_DAC2_R

+5V
(3) DDC3_CLK_DP3_AUXP — 402 DDCCLK_DAC2_5V — 402 DDCCLK_DAC2_R

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C Mechanical Key	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

U1999C
(3,7) HSYNC_DAC2 — 9 — 8 — HSYNC_DAC2_B — 402 HSYNC_DAC2_R
74VHC125
10
U1999D
(3,7) VSYNC_DAC2 — 12 — 11 — VSYNC_DAC2_B — 402 VSYNC_DAC2_R
74VHC125

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

Place close to connector J6001

(3) DPA_0P
(3) DPA_0N
(3) DPA_1P
(3) DPA_1N
(3) DPA_2P
(3) DPA_2N
(3) DPA_3P
(3) DPA_3N

J6001
1 ML_Lane_0p
2 GND_0
3 ML_Lane_0n
4 ML_Lane_1p
5 GND_1
6 ML_Lane_1n
7 ML_Lane_2p
8 GND_2
9 ML_Lane_2n
10 ML_Lane_3p
11 GND_3
12 ML_Lane_3n
13 Pin_13
14 Pin_14
15 AUX_CHp
16 GND_6
17 AUX_CHn
18 Hot_Det
20 DP_PWR
19 PWR_RTN
G4 G3 G2 G1
DISPLAYPORT

+3.3V
DNI
(3) DDC3_CLK_DP3_AUXP
C1128 100nF 6.3V
R121 100K
Q6007 2N7002E
R120 499R
Q6001 Q6003 2N7002E
Q6002 Q6004 2N7002E
+3.3V
C2097 1uF
R141 100K
+12V_BUS
R125 10K
Q6005 2N7002E
+12V_BUS
R126 10K
Q6006 2N7002E
R127 1M
C1129 100nF 6.3V
(3) DDC3_DATA_DP3_AUXN
DPA_AUX_P
DPA_DONGLE_DET
DPA_AUX_N
+3.3V
Q2021 MMBT3904
R2022 10K HPD_DPA
(3) HPD1
R2023 10K
+3.3V_BUS
F120 NANOSMDC150F-2
+3.3V_DP
R129 1M
C2096 10uF
+3.3V
DNI
DNI
DNI
+5V_VESA
DPA_AUX_P
DPA_AUX_N

May be able to use just one Fuse for both connectors.

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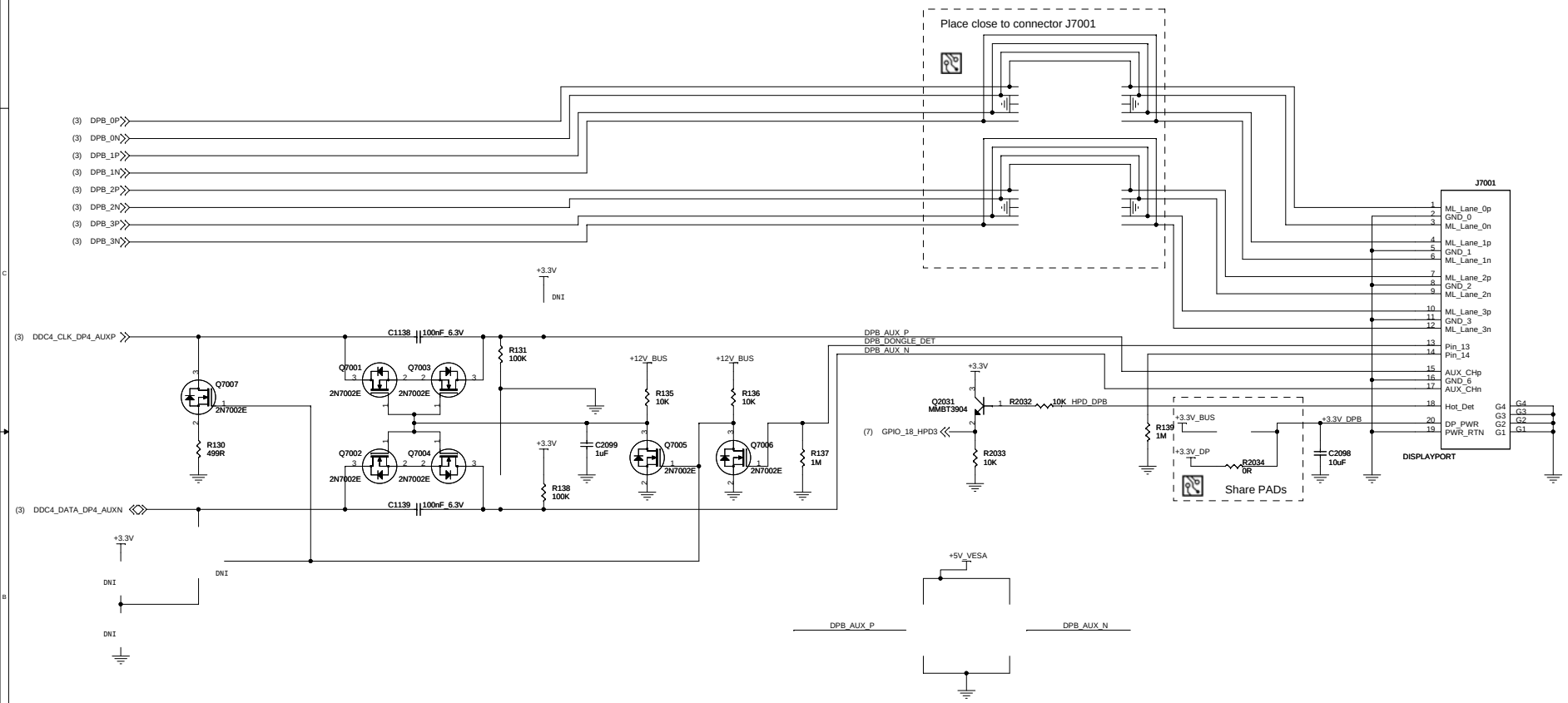

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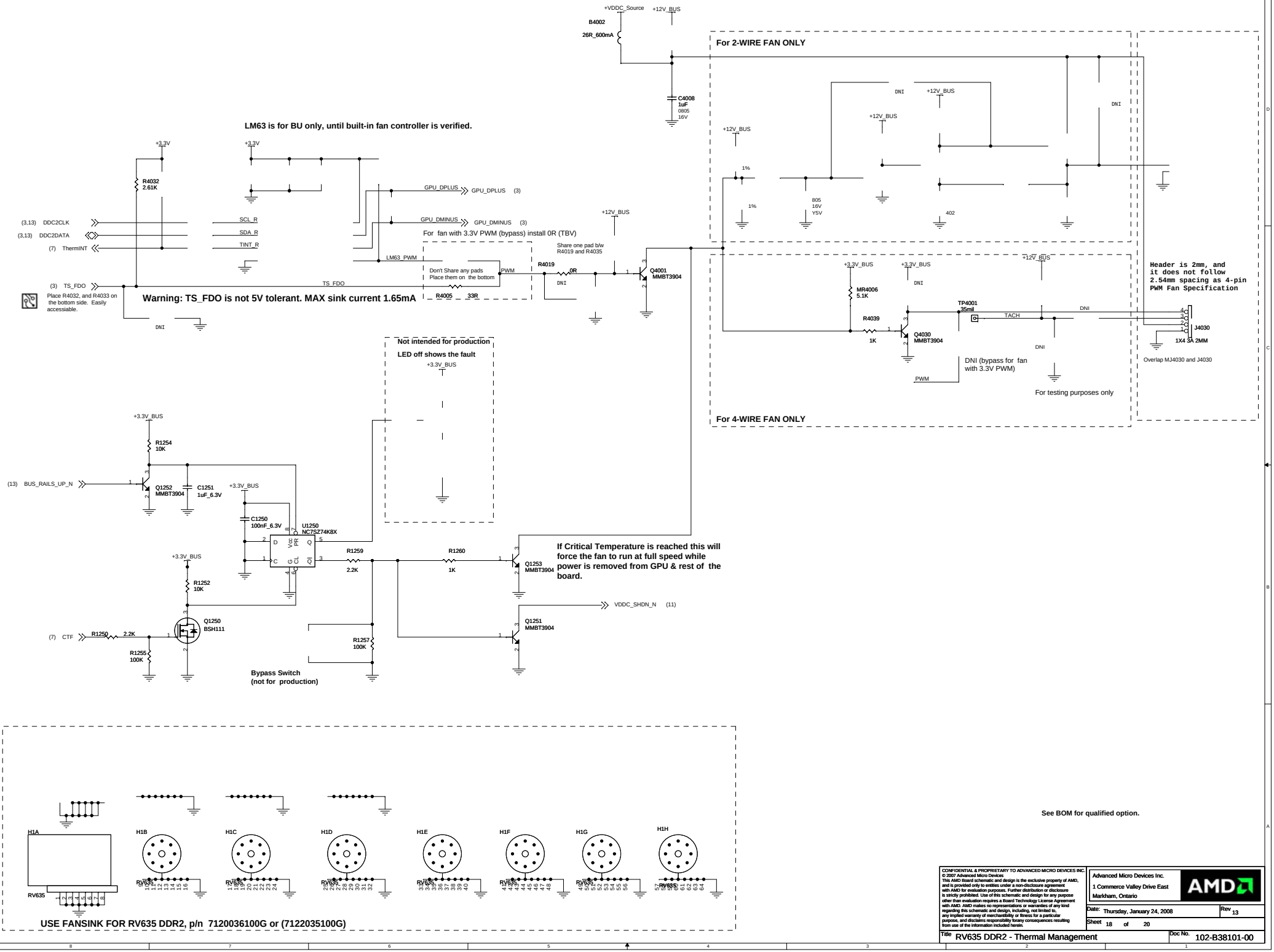

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DVI/DVI SCREWS with top tab

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY1
ANTISTATIC
BAG
6_X_11

BKT1
BRACKET
8020046100G

Need New Bracket

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

MT2
MT_Hole_0.136_in_6VIA

DNI

PCB1
PCB
109-B38131-00B

RV635 Socket

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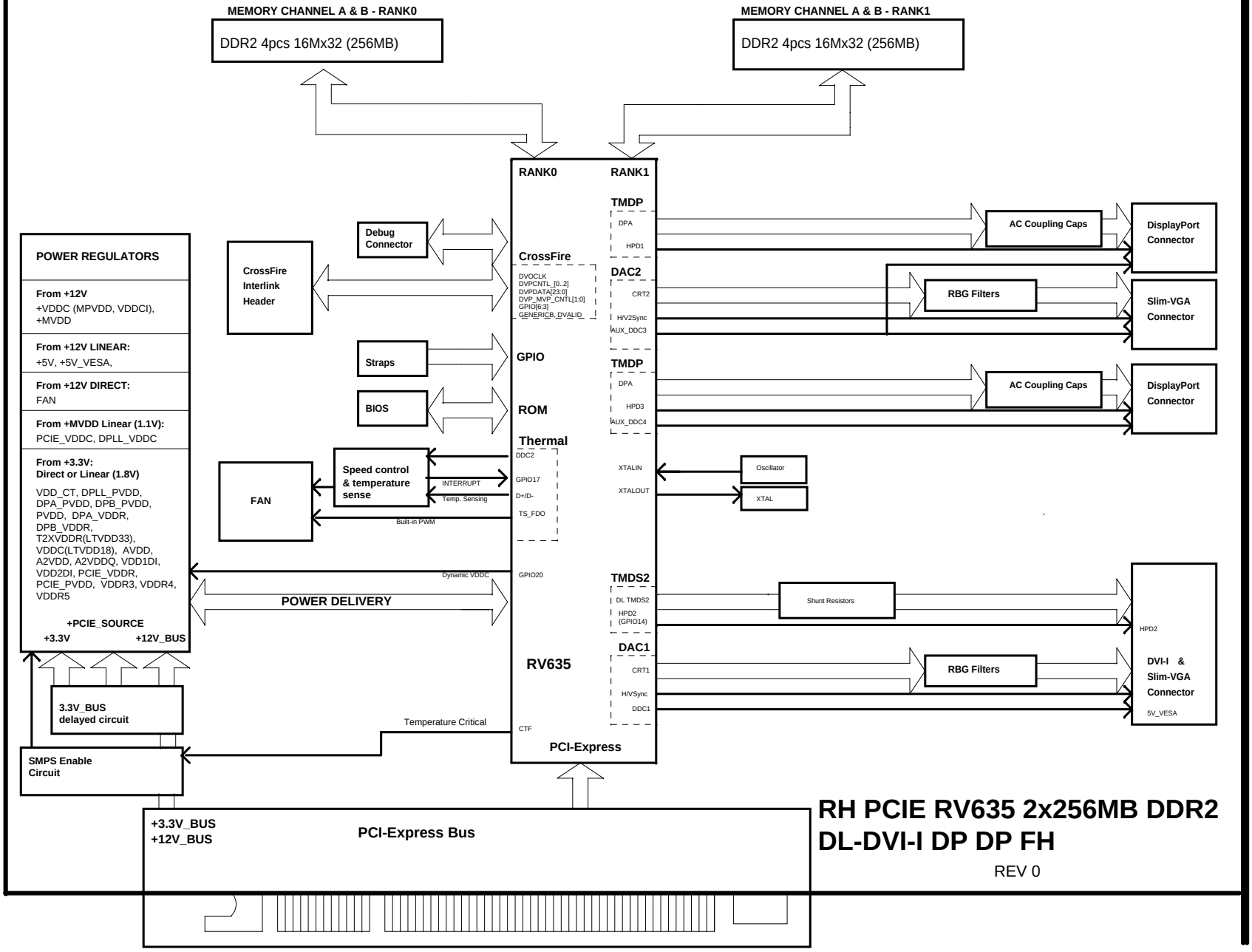

RH PCIE RV635 2x256MB DDR2
DL-DVI-I DP DP FH

REV 0

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Title	Schematic No.	Date:
RH PCIE RV635 2x256MB DDR2 DUAL DL-DVI-I DL-DVI-I VO FH	102-B38101-00	Thursday, January 24, 2008

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 13

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	11/02/07	Initial design for RV635 GDDR3
1	00B	11/15/07	Page 4 - Added B993 and C733 for DPLL_PVDD filtering improvement Page 10 - Changed the VDDC CTLR U1303 from APW7065 to uP6101BU8-A with heatpad Added one low MOSFET Q1303 BSC119N03SG and MQ1303 FDS7096N3 Page 11 - Added R635 10k pull-down DNI on POK of U601 PWR CTLR Added 2 CAP C605 and C615 after inductors Page 12 - Added THT Inductor PL701 Changed the MVDD CTLR U703 from APW7065 to uP6101BU8-A with heatpad Removed MC723 to avoid mecanical conflict with fansink Page 13 - PowerPlay table has changed from 1.03V to 0.9V min and Rf1 and Rf2 were adjusted Page 16 - Added R141 and R142 100k pull-up to 3.3V for DP detection and latest change from Apple. Only one will be installed Changed R125-126 value from 1M to 10K Added ESD Protection RCLAMP0524P REG1132 REG1133 on DPA Page 17 - Added R138 and R140 100k pull-up to 3.3V for DP detection and latest change from Apple. Only one will be installed Changed R135-136 value from 1M to 10K Added ESD Protection RCLAMP0524P REG1130 REG1131 on DPB Page 18 - Added 3 BJT stages for the 2-WIRE FAN CTLR Q4004, Q4002 and Q4003.