P601 REV:1.0 : G96-GS/GE2-128, MXM-II, 512/256MB DDR2 (32/16Mx16)
LVDS, DP-A/B, DVI-A/B/C, TV_OUT, VGA, HD AUDIO, SPDIF
MXM 2.1a SPECIFICATION COMPLIANT

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REVISION HISTORY

Sch Rev	PCB Rev	DATE	REVISION DESCRIPTION
1.0	1.0	2008-04-16	Base NV P616-A03 design. Change GDDR3 to DDR2
1.0	1.0	2008-05-07	Model name change to P601 V1.0

Title: <Title>		
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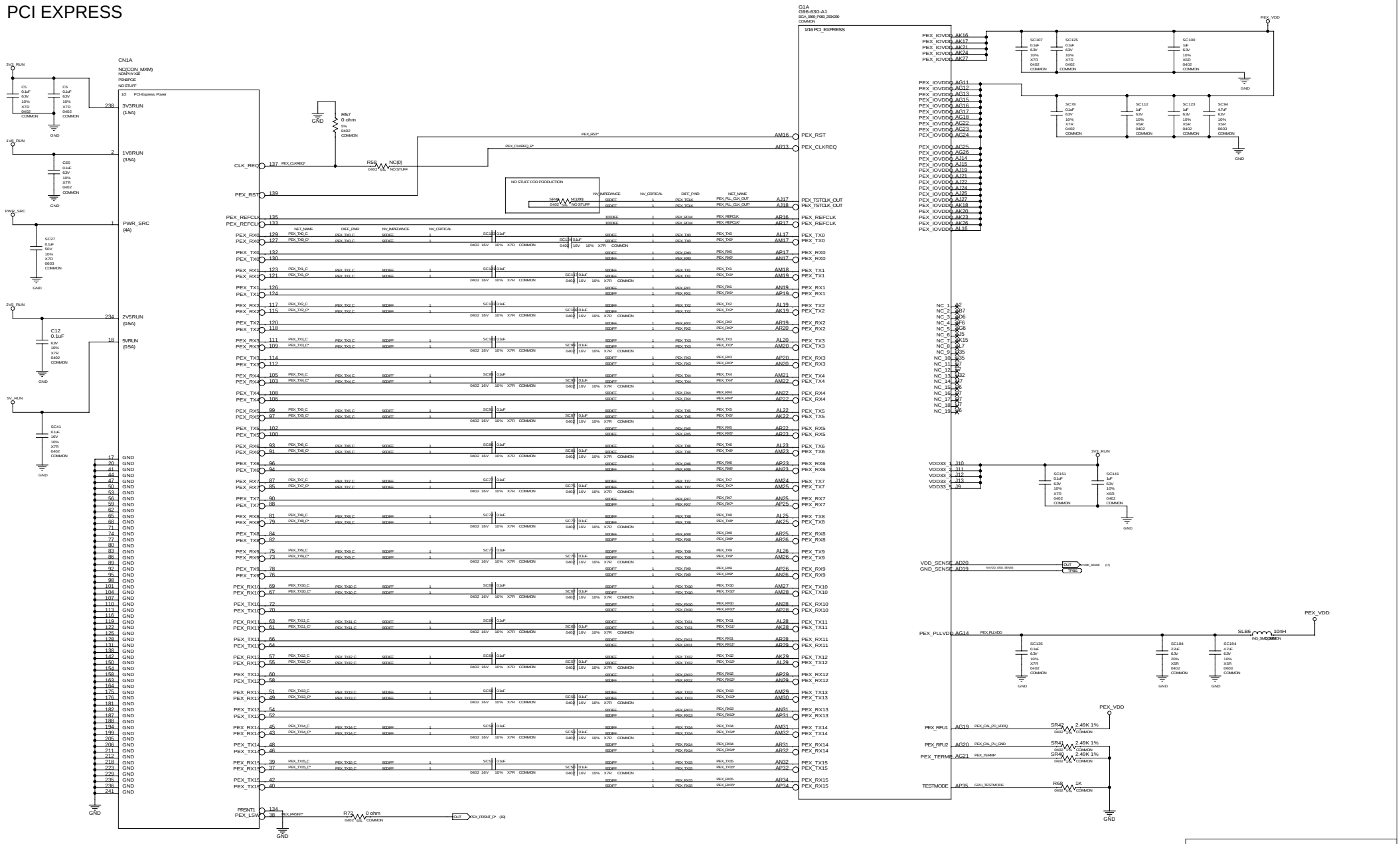
PCI EXPRESS



Title	<Title>
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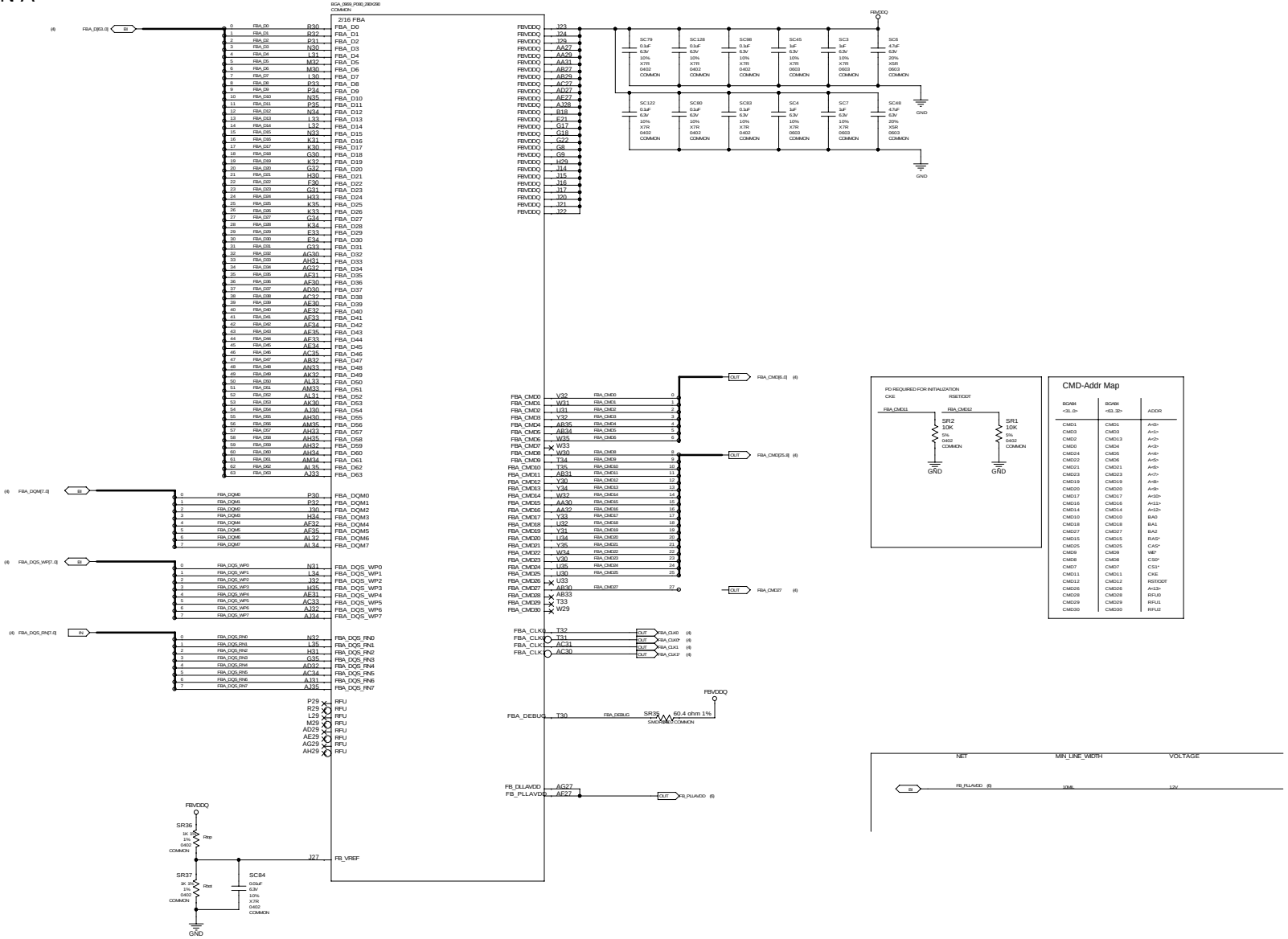
GPU MEMORY INTERFACE: PARTITION A



Title	<Title>		
Size	Document Number		Rev
Custom	<Doc>		A
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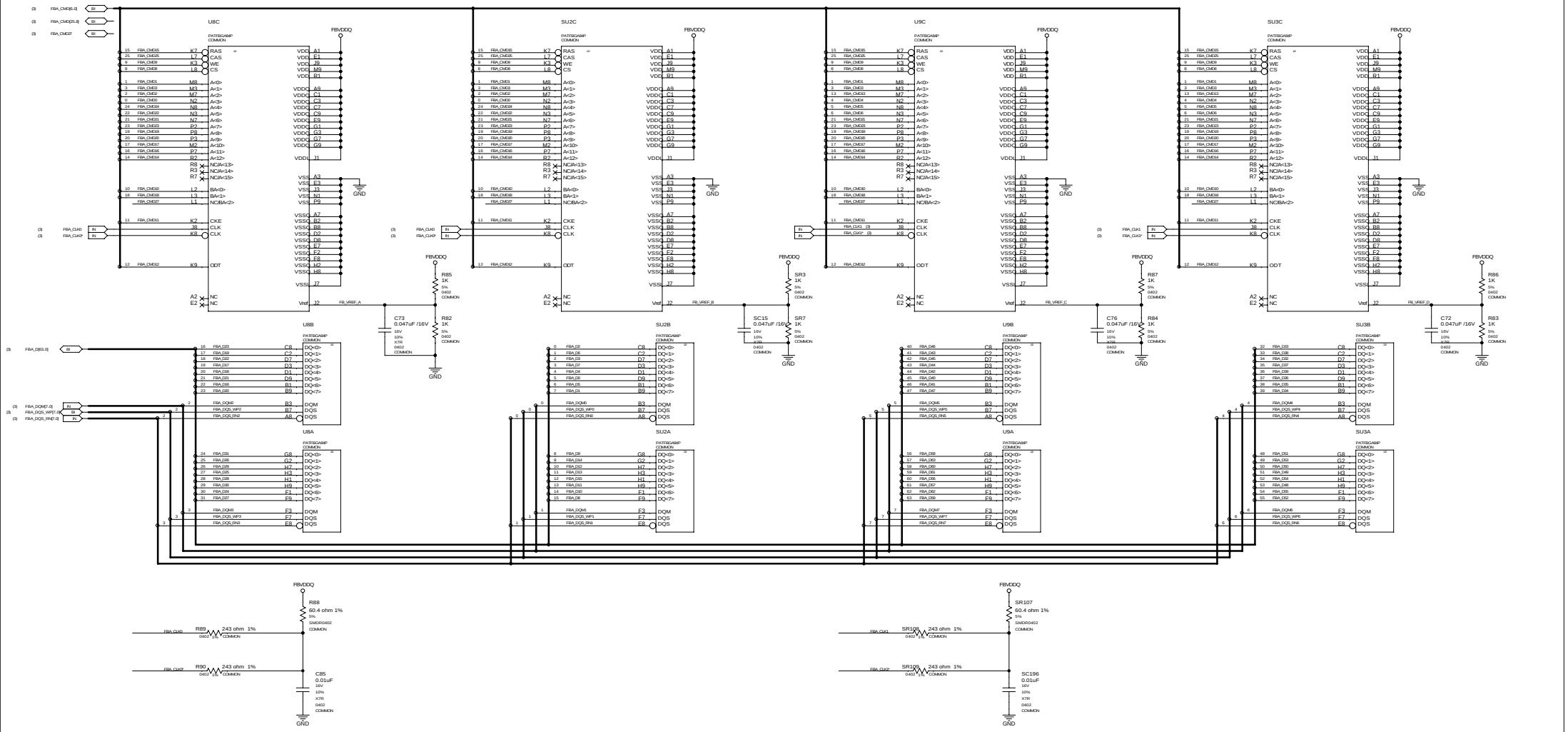
Partition A Memories



Title	<Title>		
Size	Document Number <Doc>		Rev A
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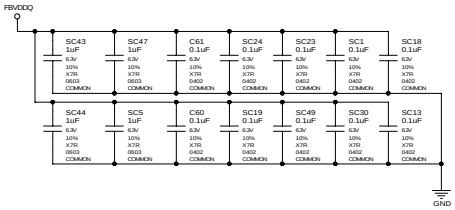
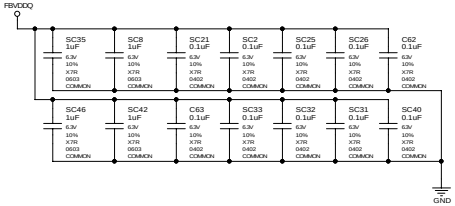
FRAME BUFFER: PARTITION A DECOUPLING

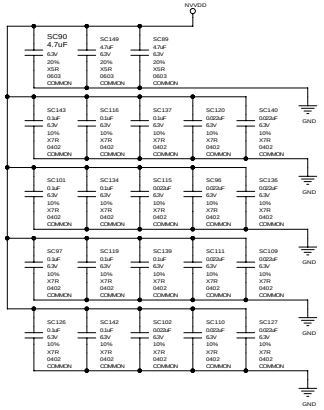


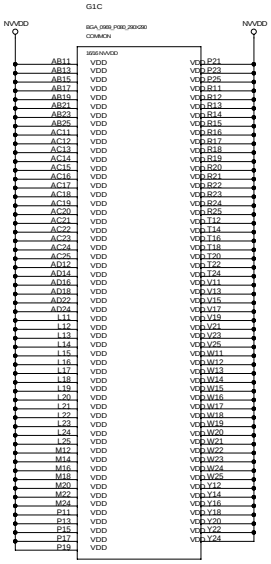
Decoupling for FBA North Side Memory Device.



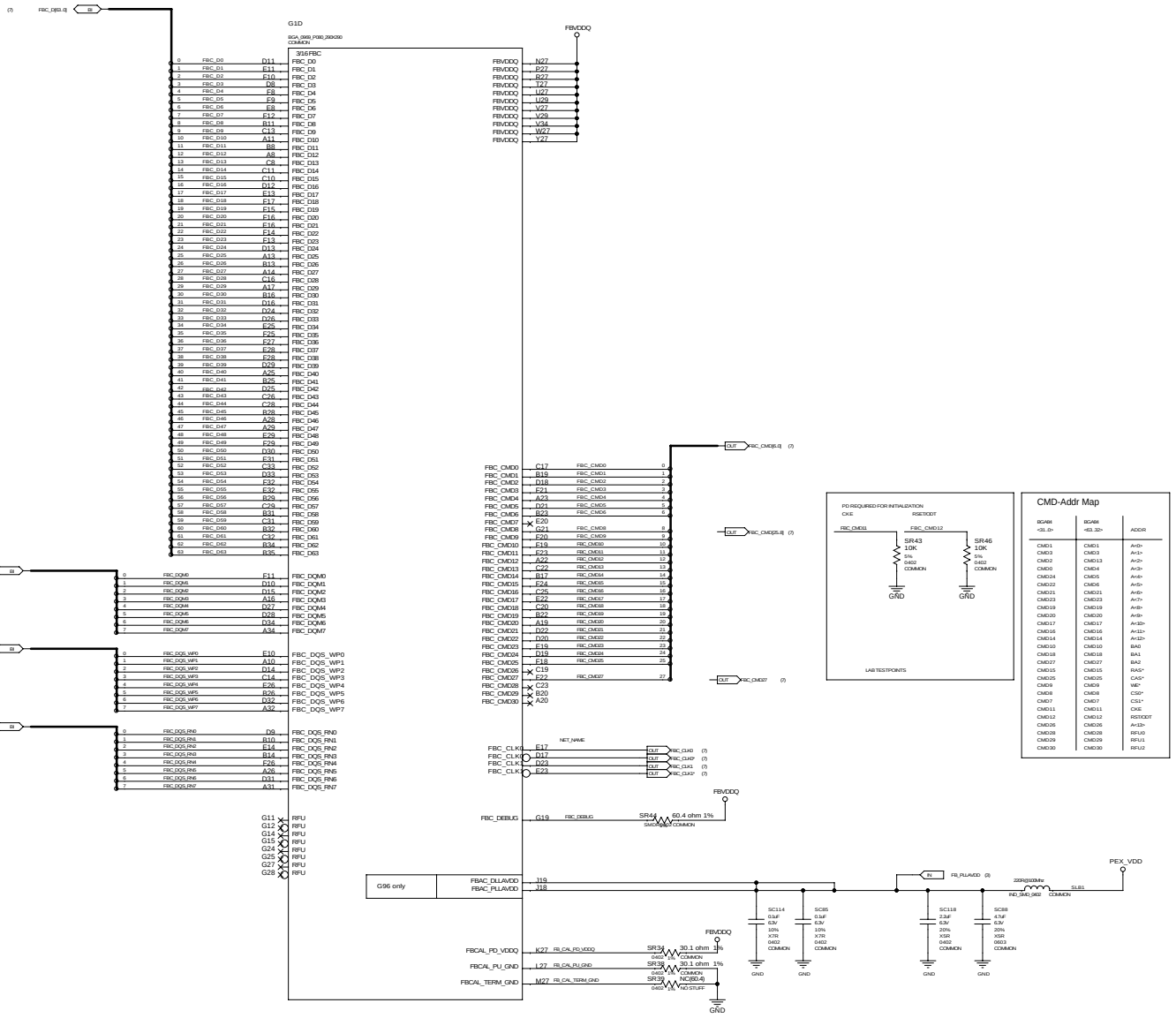
Decoupling for FBA South Side Memory Device.

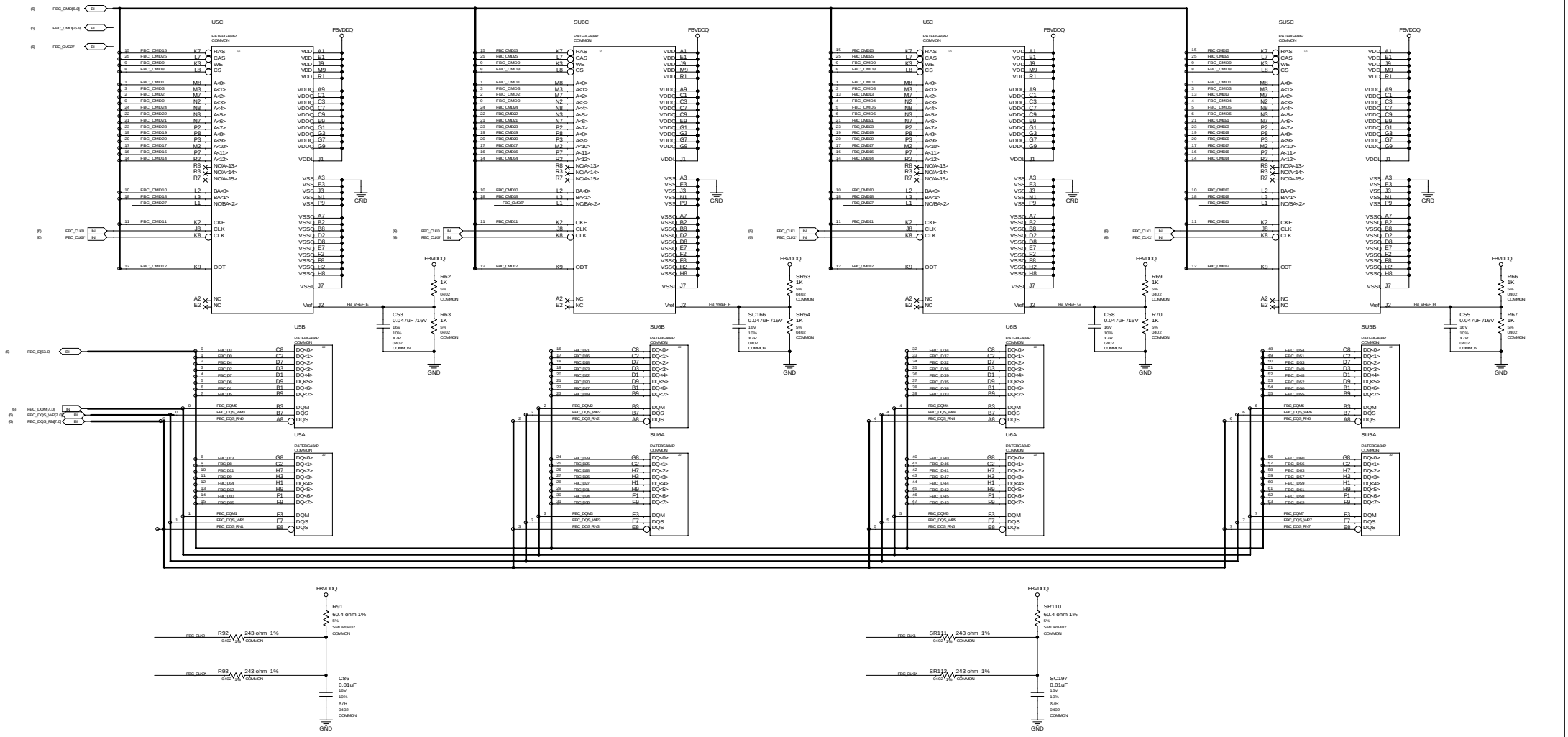
NVVDD POWER AND DECOUPLING




G1C
NVVDD
NVVDD
BGA_0900_P030_28X28
COMMON
1650 NVDD
AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AC11 AC12 AC13 AC14 AC15 AC16 AC17 AC18 AC19 AC20 AC21 AC22 AC23 AC24 AC25 AD12 AD14 AD16 AD18 AD22 AD24 L11 L12 L13 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 M12 M14 M16 M18 M20 M22 M24 P11 P13 P15 P17 P19
VDD
VDD
VDD

GPU MEMORY INTERFACE: PARTITION C





Title	<Title>		
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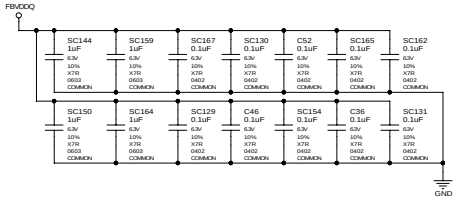
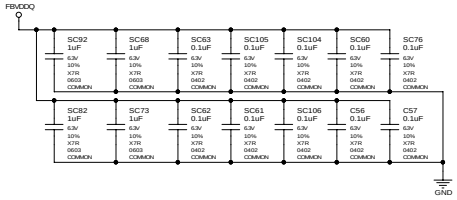
FRAMEBUFFER: PARTITION C DECOUPLING

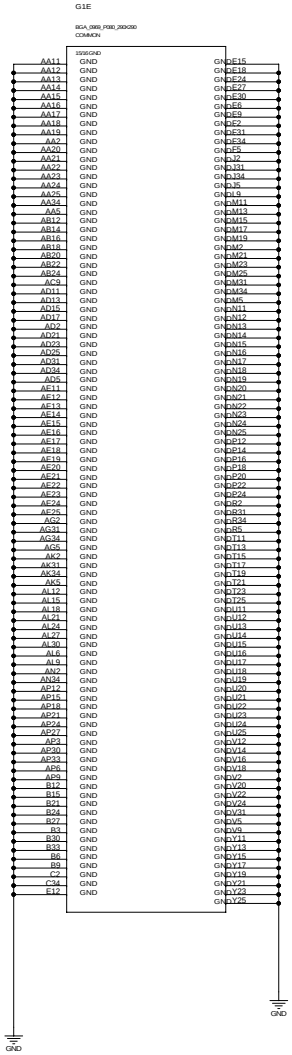


Decoupling for FBC West Side Memory Device.



Decoupling for FBC East Side Memory Device.

NVVDD GROUND



Title	<Title>		
Size	Document Number		Rev
Custom	<Doc>		A
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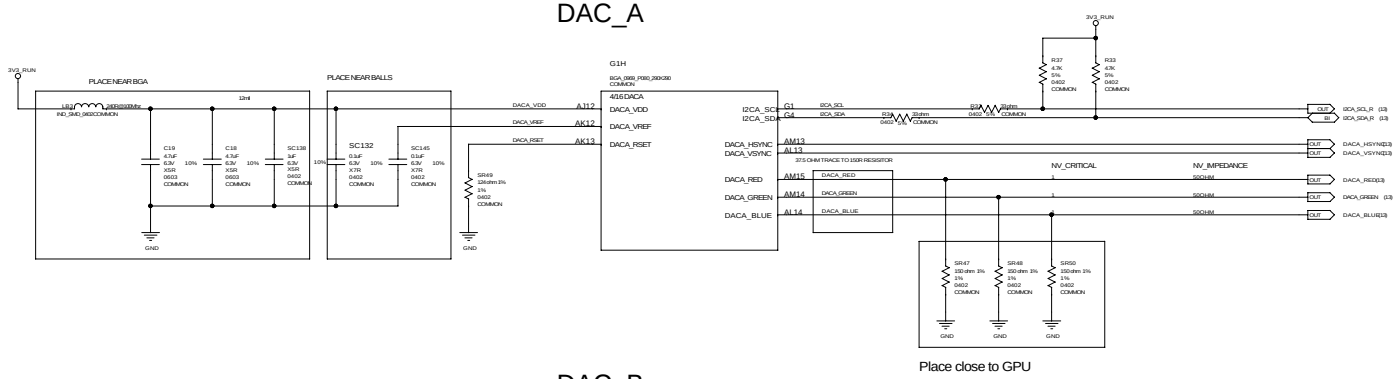
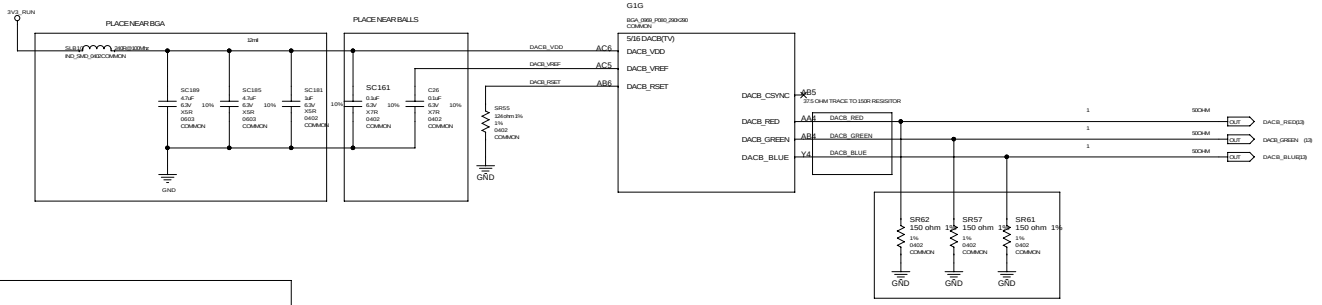
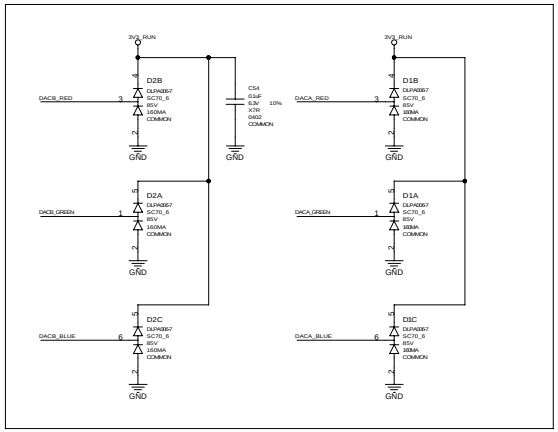
DAC_A



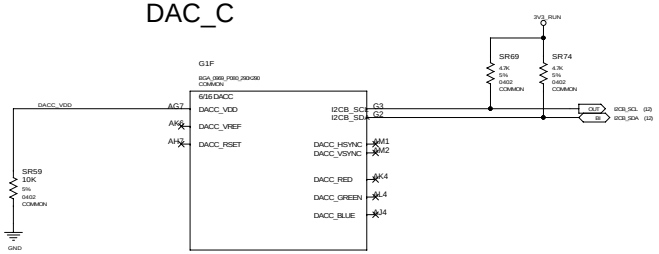
DAC_B





TV DAC ESD PROTECTION

DAC_C



Title	<Title>	
Size	Document Number	Rev
Custom	<Doc>	A
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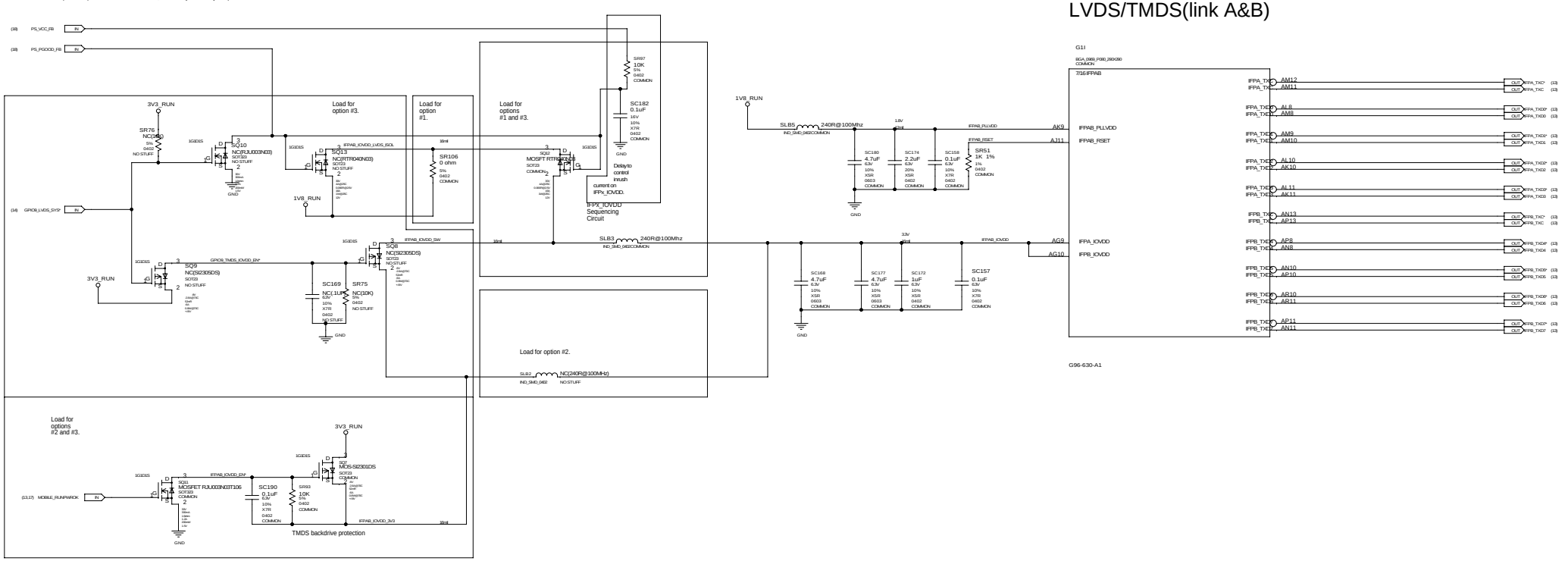
LVDS/TMDS(link A&B)



(LVDS CONSTRAINTS)

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
(13) IFPA_TXD0*	IFPATXD0	1	100DIFF
(13) IFPA_TXD0	IFPATXD0	1	100DIFF
(13) IFPA_TXD1*	IFPATXD1	1	100DIFF
(13) IFPA_TXD1	IFPATXD1	1	100DIFF
(13) IFPA_TXD2*	IFPATXD2	1	100DIFF
(13) IFPA_TXD2	IFPATXD2	1	100DIFF
(13) IFPA_TXD3*	IFPATXD3	1	100DIFF
(13) IFPA_TXD3	IFPATXD3	1	100DIFF
(13) IFPB_TXD4*	IFPBTXD4	1	100DIFF
(13) IFPB_TXD4	IFPBTXD4	1	100DIFF
(13) IFPB_TXD5*	IFPBTXD5	1	100DIFF
(13) IFPB_TXD5	IFPBTXD5	1	100DIFF
(13) IFPB_TXD6*	IFPBTXD6	1	100DIFF
(13) IFPB_TXD6	IFPBTXD6	1	100DIFF
(13) IFPB_TXD7*	IFPBTXD7	1	100DIFF
(13) IFPB_TXD7	IFPBTXD7	1	100DIFF
(13) IFPA_TXC*	IFPATXC	1	100DIFF
(13) IFPA_TXC	IFPATXC	1	100DIFF
(13) IFPB_TXC*	IFPBTXC	1	100DIFF
(13) IFPB_TXC	IFPBTXC	1	100DIFF

Title	<Title>		
Size	Document Number <Doc>		Rev A
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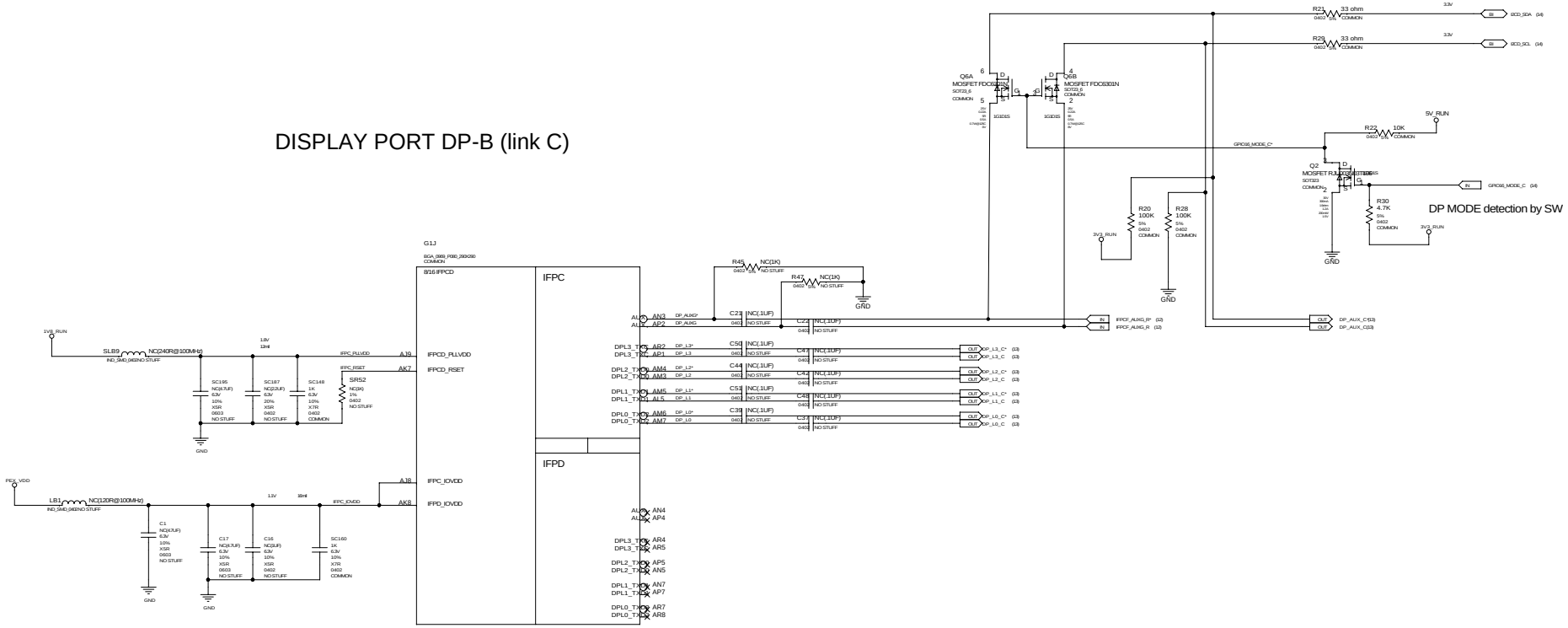
DISPLAY PORT DP-B (link C)



(DP CONSTRAINTS)

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
(13) DP_AUX_C*	DP_AUX3	1	100DIFF
(13) DP_AUX_C	DP_AUX3	1	100DIFF
(13) DP_L3_C*	DPL3C	1	100DIFF
(13) DP_L3_C	DPL3C	1	100DIFF
(13) DP_L2_C*	DPL2C	1	100DIFF
(13) DP_L2_C	DPL2C	1	100DIFF
(13) DP_L1_C*	DPL1C	1	100DIFF
(13) DP_L1_C	DPL1C	1	100DIFF
(13) DP_L0_C*	DPL0C	1	100DIFF
(13) DP_L0_C	DPL0C	1	100DIFF

Title	<Title>	
Size	Document Number <Doc>	Rev A
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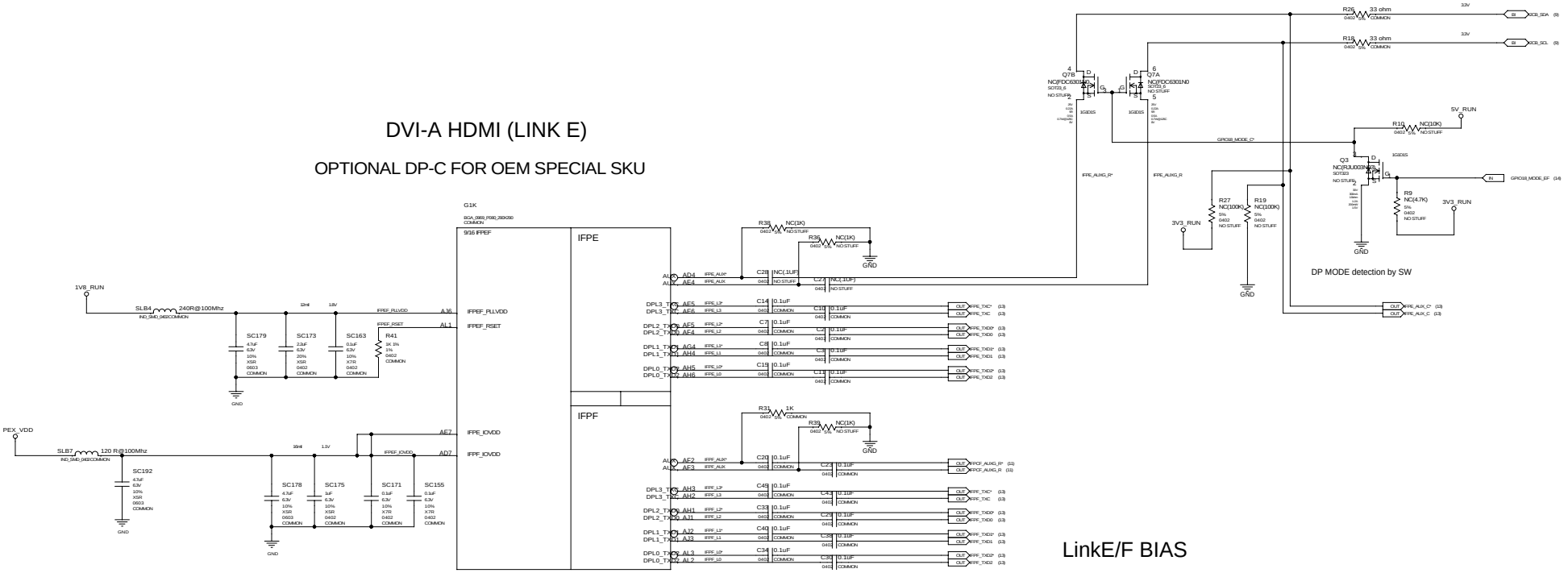
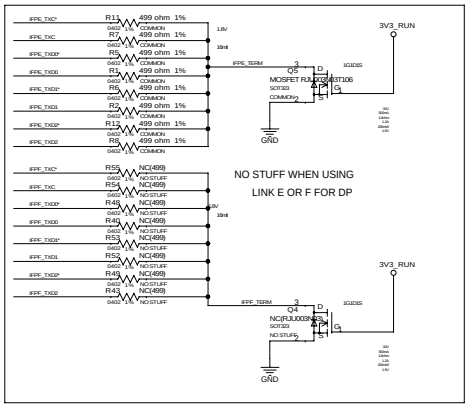
DVI-A HDMI (LINK E)

OPTIONAL DP-C FOR OEM SPECIAL SKU



DISPLAY PORT DP-A (LINK F)

OPTIONAL DVI-B TMDS SL OR DL W/ DVI-A



(TMDS/HDMI/DP OPTION CONSTRAINTS)

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
IFPE_TXC*	IFPETXC	1	100DIFF
IFPE_TXC	IFPETXC	1	100DIFF
IFPE_TXD0*	IFPETXD0	1	100DIFF
IFPE_TXD0	IFPETXD0	1	100DIFF
IFPE_TXD1*	IFPETXD1	1	100DIFF
IFPE_TXD1	IFPETXD1	1	100DIFF
IFPE_TXD2*	IFPETXD2	1	100DIFF
IFPE_TXD2	IFPETXD2	1	100DIFF

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
IFPE_TXC*	IFPETXC	1	100DIFF
IFPE_TXC	IFPETXC	1	100DIFF
IFPE_TXD0*	IFPETXD0	1	100DIFF
IFPE_TXD0	IFPETXD0	1	100DIFF
IFPE_TXD1*	IFPETXD1	1	100DIFF
IFPE_TXD1	IFPETXD1	1	100DIFF
IFPE_TXD2*	IFPETXD2	1	100DIFF
IFPE_TXD2	IFPETXD2	1	100DIFF

Title	<Title>		
Size: Custom	Document Number: <Doc>		Rev: A
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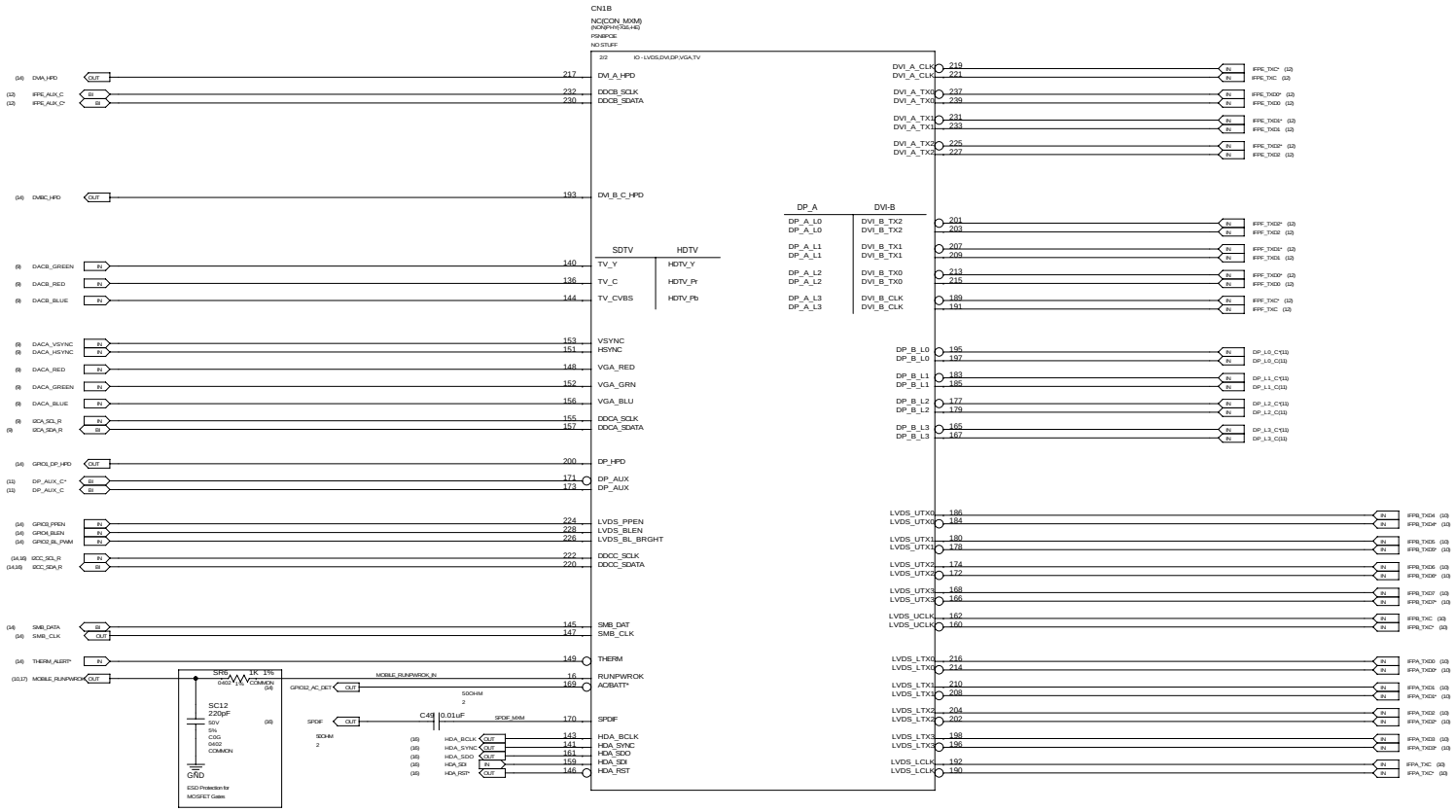
MXM CONNECTOR



Title	<Title>		
Size	Document Number		Rev
Custom	<Doc>		A
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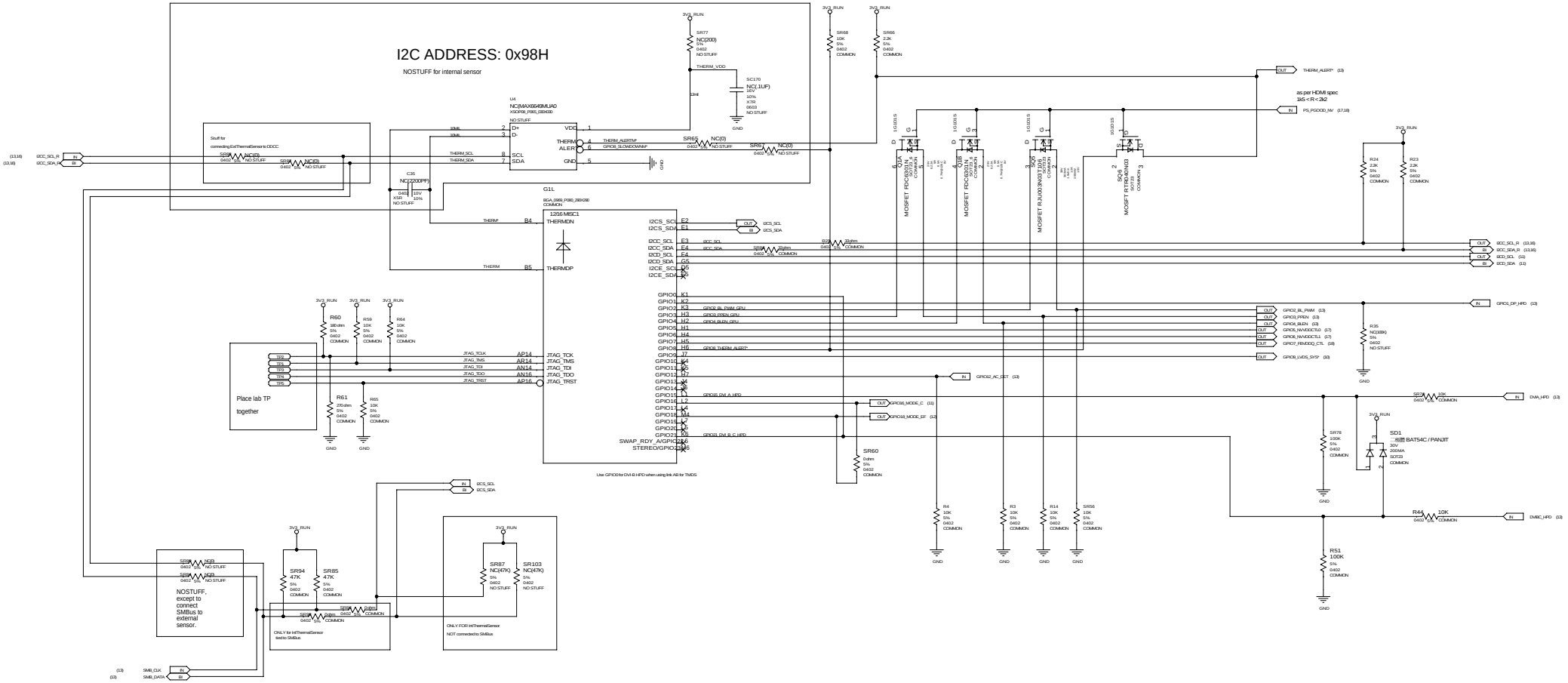
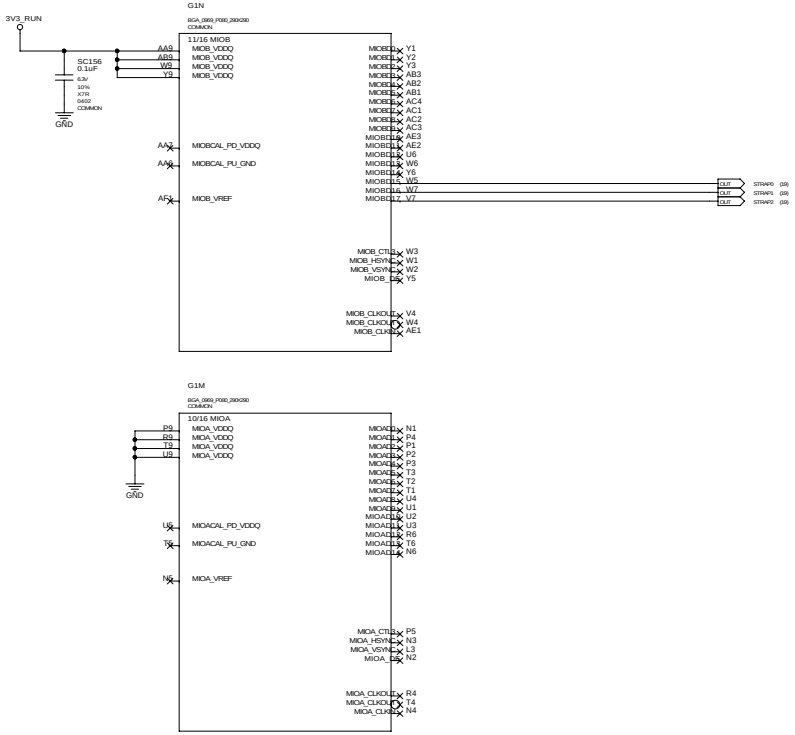
GPIO, TEMP SENSOR, JTAG



MIOA/B



Title	<Title>	
Size	Document Number <Doc>	Rev A
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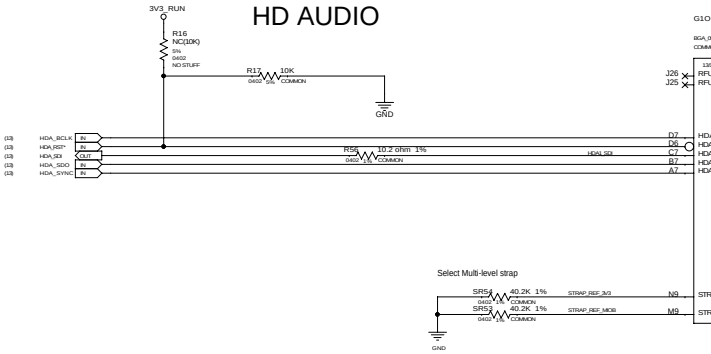
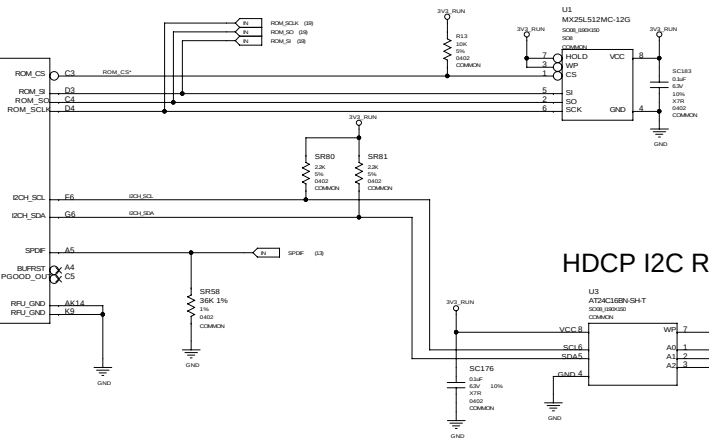
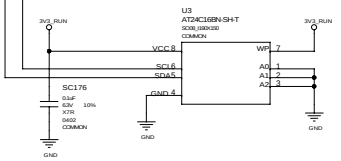
HD AUDIO



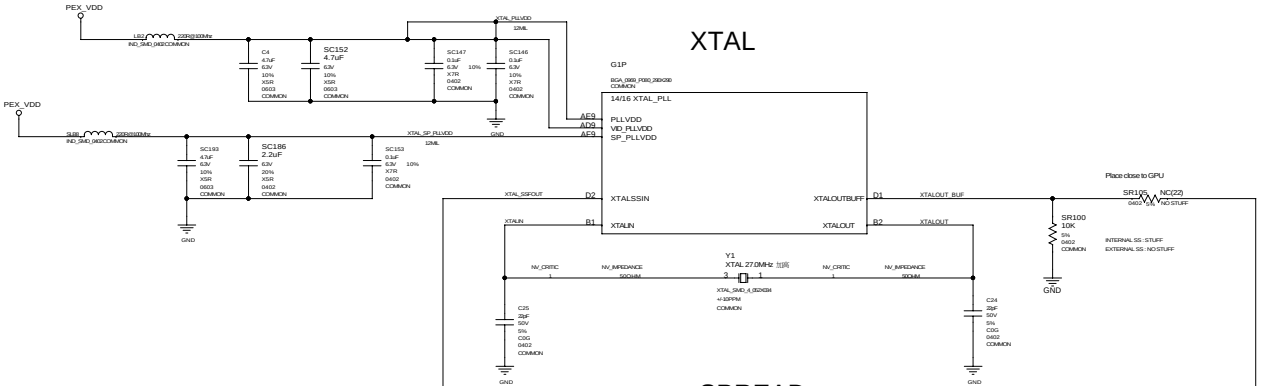
VBIOS ROM



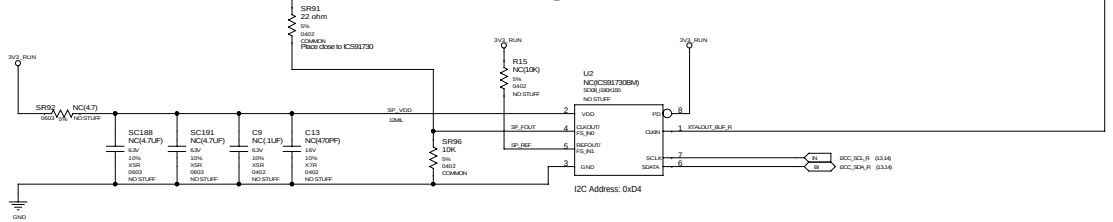
HDCP I2C ROM



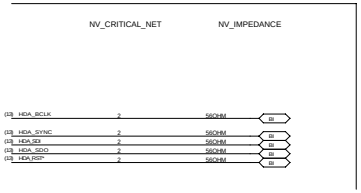
XTAL



SPREAD



(HD AUDIO CONSTRAINTS)



Title	<Title>		
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Custom	<Doc>		A
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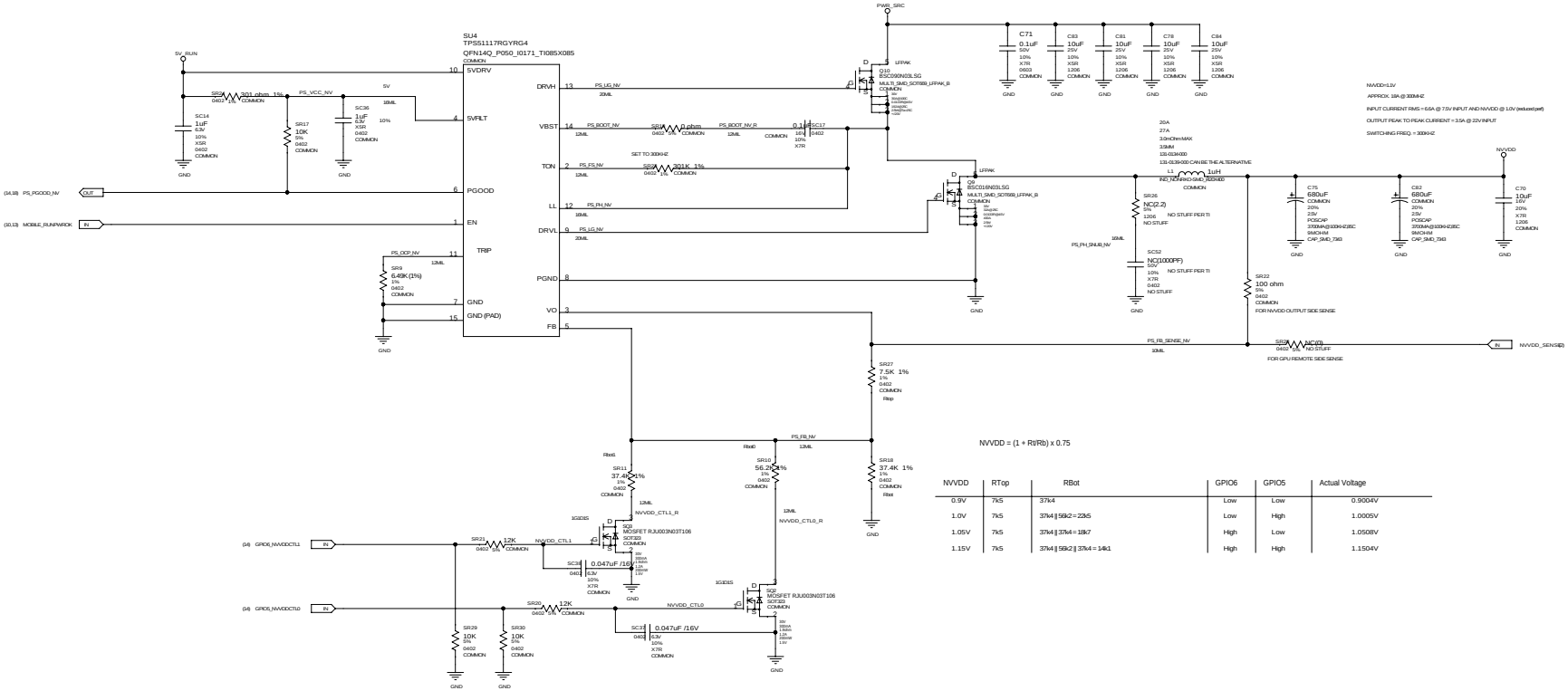
NVVDD POWER SUPPLY

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
NVVDD	1V	12MIL	18A

NVVDD SWITCHER POWER SUPPLY



NVVDD	RTop	RBot	GPIO6	GPIO5	Actual Voltage
0.9V	7k5	37k4	Low	Low	0.9004V
1.0V	7k5	37k4 || 56k2 = 22k5	Low	High	1.0005V
1.05V	7k5	37k4 || 37k4 = 18k7	High	Low	1.0508V
1.15V	7k5	37k4 || 56k2 || 37k4 = 14k1	High	High	1.1504V

Title	<Title>		
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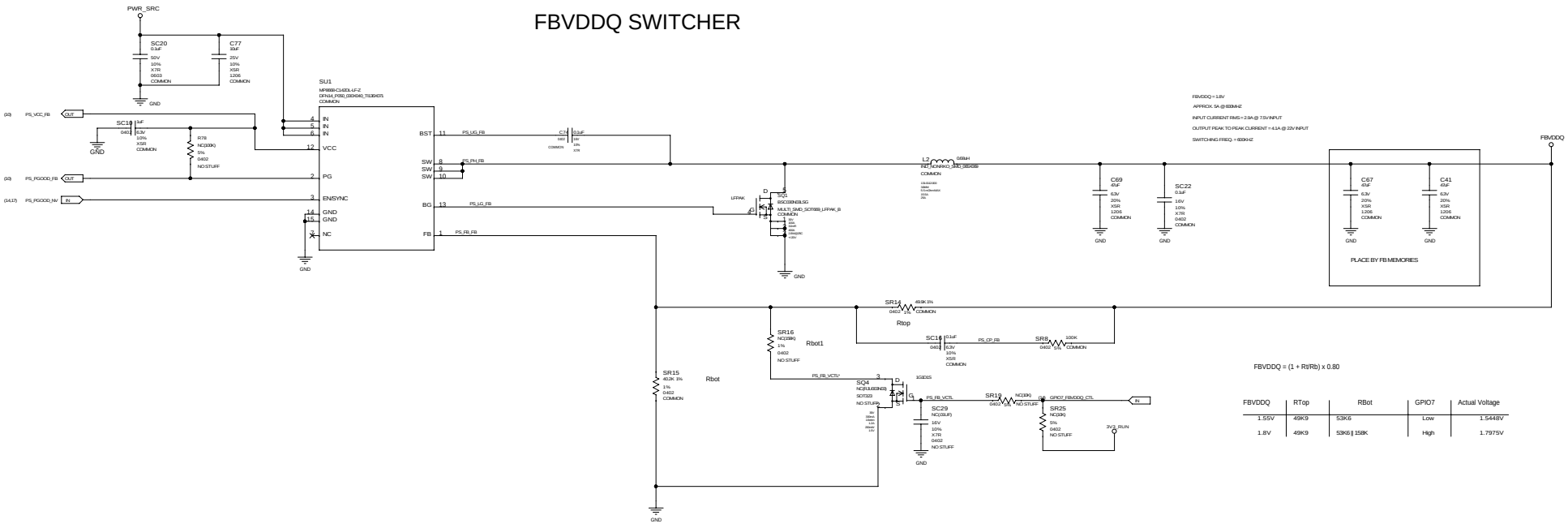
FBVDDQ AND PEX_VDD POWER SUPPLY

NET	VOLTAGE	NV_NET_MAX_CURRENT
PEX_VDD	1.0V	4A
FBVDDQ	1.8V	10A

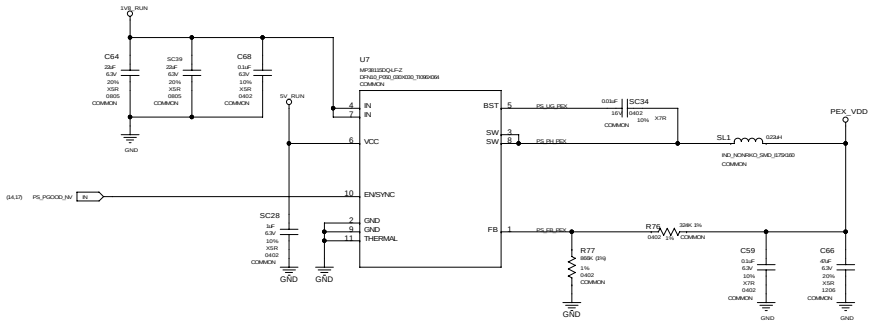
FBVDDQ SWITCHER



FBVDDQ = (1 + Rt/Rb) x 0.80

FBVDDQ	RTop	RBot	GPIO7	Actual Voltage
1.55V	49K9	53K6	Low	1.5448V
1.8V	49K9	53K6 ‖ 158K	High	1.7975V

PEX_VDD SWITCHER



Vout = Vref * (1 + Rtop / Rbot)

1.099V = 0.8V * (1 + 324k / 866k)

Title	<Title>		
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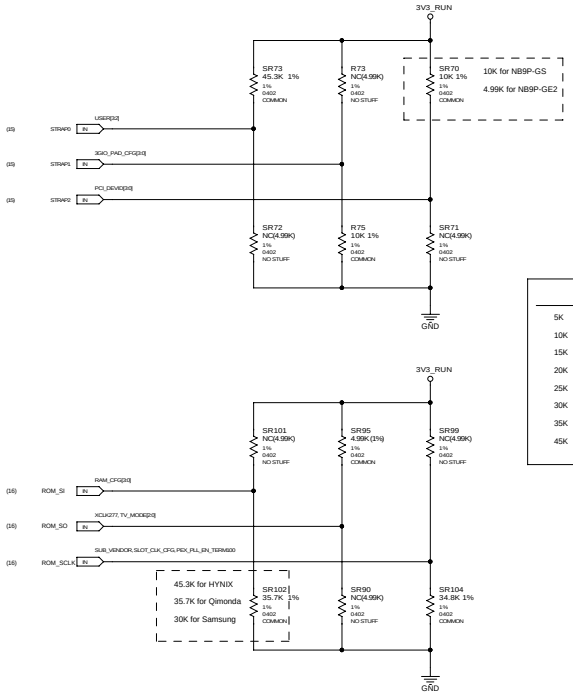
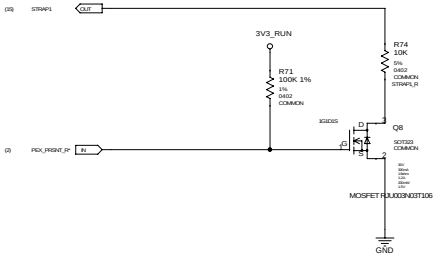
STRAPPING OPTIONS



	3V3	GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

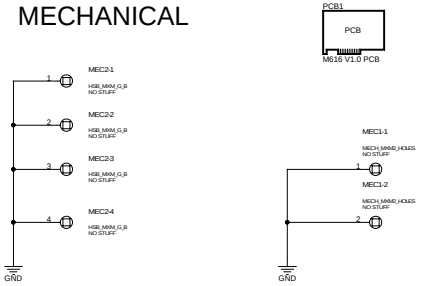
STRAP0	USER_BIT0	0xF: 45K PU (unused)	
	USER_BIT1		
	USER_BIT2		
	USER_BIT3		
STRAP1	3GIO_PADCFG_LUT_ADR0		
	3GIO_PADCFG_LUT_ADR1	0x0: Desktop default (normal swing) - 5k PD	
	3GIO_PADCFG_LUT_ADR2	0x1: Mobile default (low swing) - 10k PD	
	3GIO_PADCFG_LUT_ADR3	acc. to //hw/tesla_g98b/manuals/dev_ext_devices.ref	
STRAP2	PCI_DEVID_0	all 4 bits set by HW strapping	
	PCI_DEVID_1	0x0649: 10K PU (NB9P-GS)	
	PCI_DEVID_2	0x0648: 5K PU (NB9P-GE2)	
	PCI_DEVID_3	0x065C: 25K PU (NB9P-GLM2)	
ROM_SO	TV_MODE_BIT0	0x0: NTSC-M	
	TV_MODE_BIT1		5K PU
	TV_MODE_BIT2		
	XCLK_277	1: PCI-E GEN2	
ROM_SI	RAM_CFG_0	256 MB (4pcs. 16Mx32)	512 MB (4pcs. 32Mx32)
	RAM_CFG_1	RAM_CFG[3:0] Definitions: 0000 Reserved; 0001 Qimonda; 0010 Hynix; 0011 Samsung	RAM_CFG[3:0] Definitions: 0100 25k PD Reserved; 0101 30k PD Qimonda; 0110 35k PD Hynix; 0111 45k PD Samsung
	RAM_CFG_2		
	RAM_CFG_3		
ROM_SCLK	PEX_PLL_EN_TERM100	0:	
	SLOT_CLK_CONFIG	1: GPU/MCH SHARE COM REF CLK	35K PD
	SUB_VENDOR	1: SUB_VENDOR BIOS	
	PCI_DEVID_EXT	0: TERM100 DISABLED	

PEX SWING LEVEL



PEX_PRSNT2_R	R_STRAP1	3_GIO_PADCFG_LUT<3..0>
GND	10k	0x1 MOBILE_DEFAULT
FLOAT	5k (10k ll 10k)	0x0 DESKTOP_DEFAULT

MECHANICAL



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