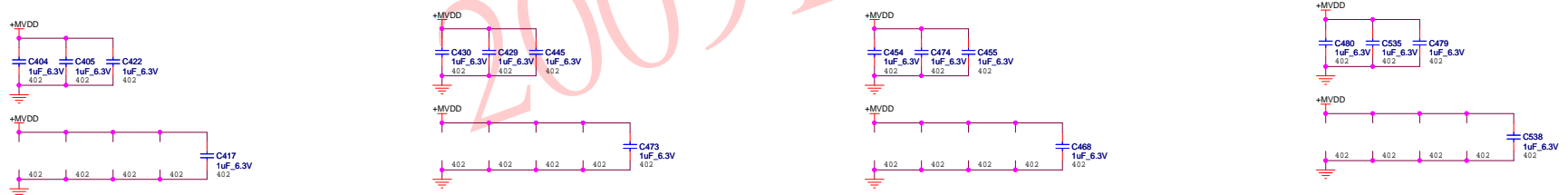
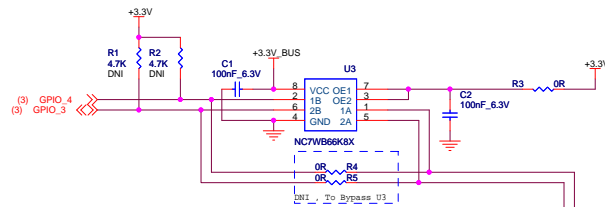


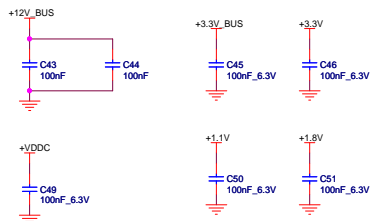
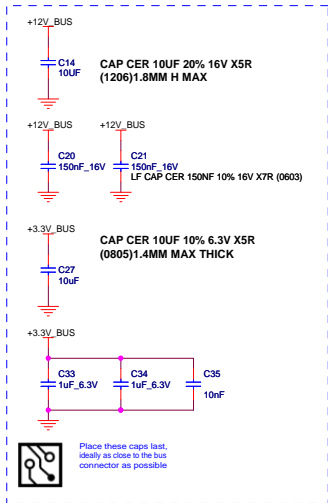
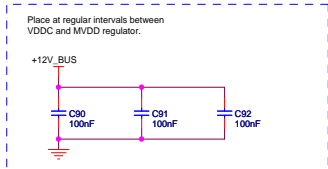
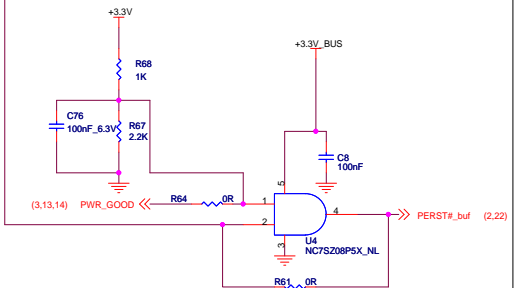
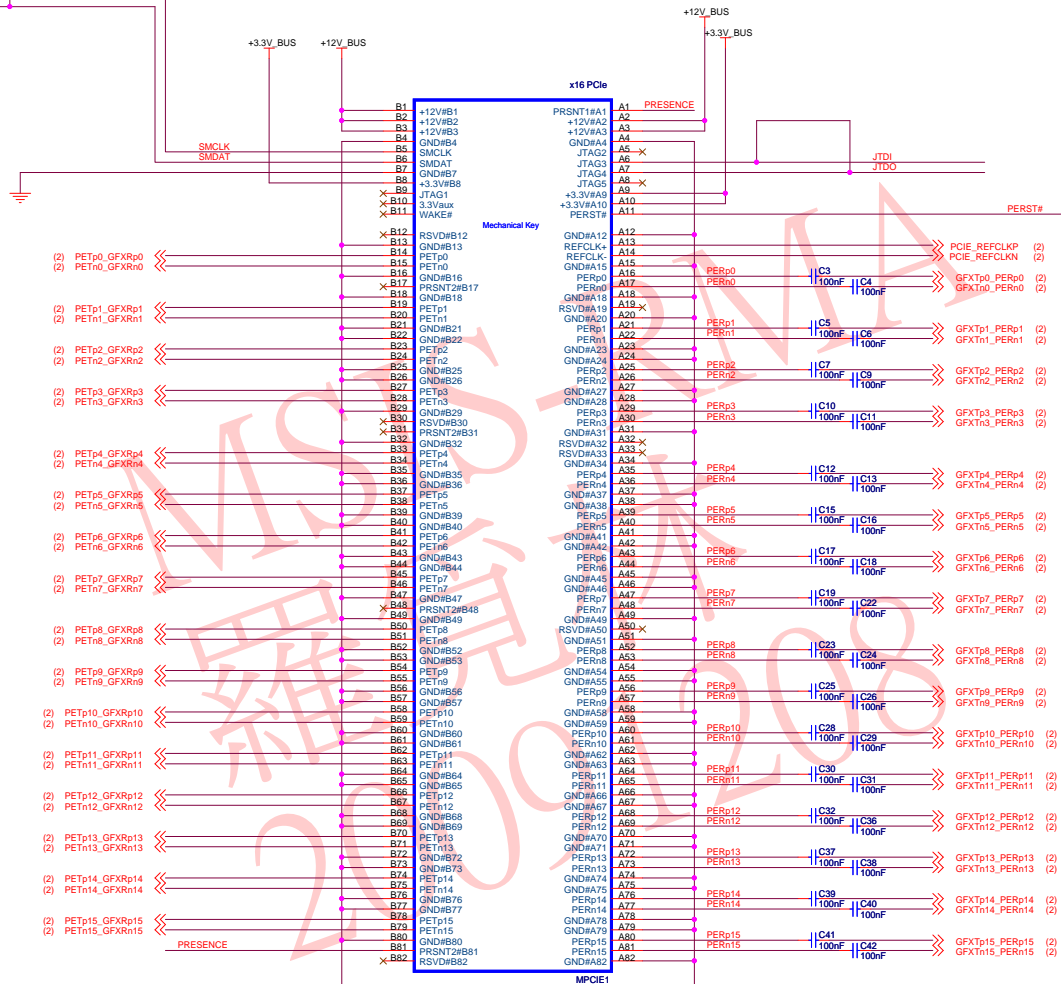
MAX DENSITY: 64Mx16





CLK 與 VREF 線路與RANK1 共用

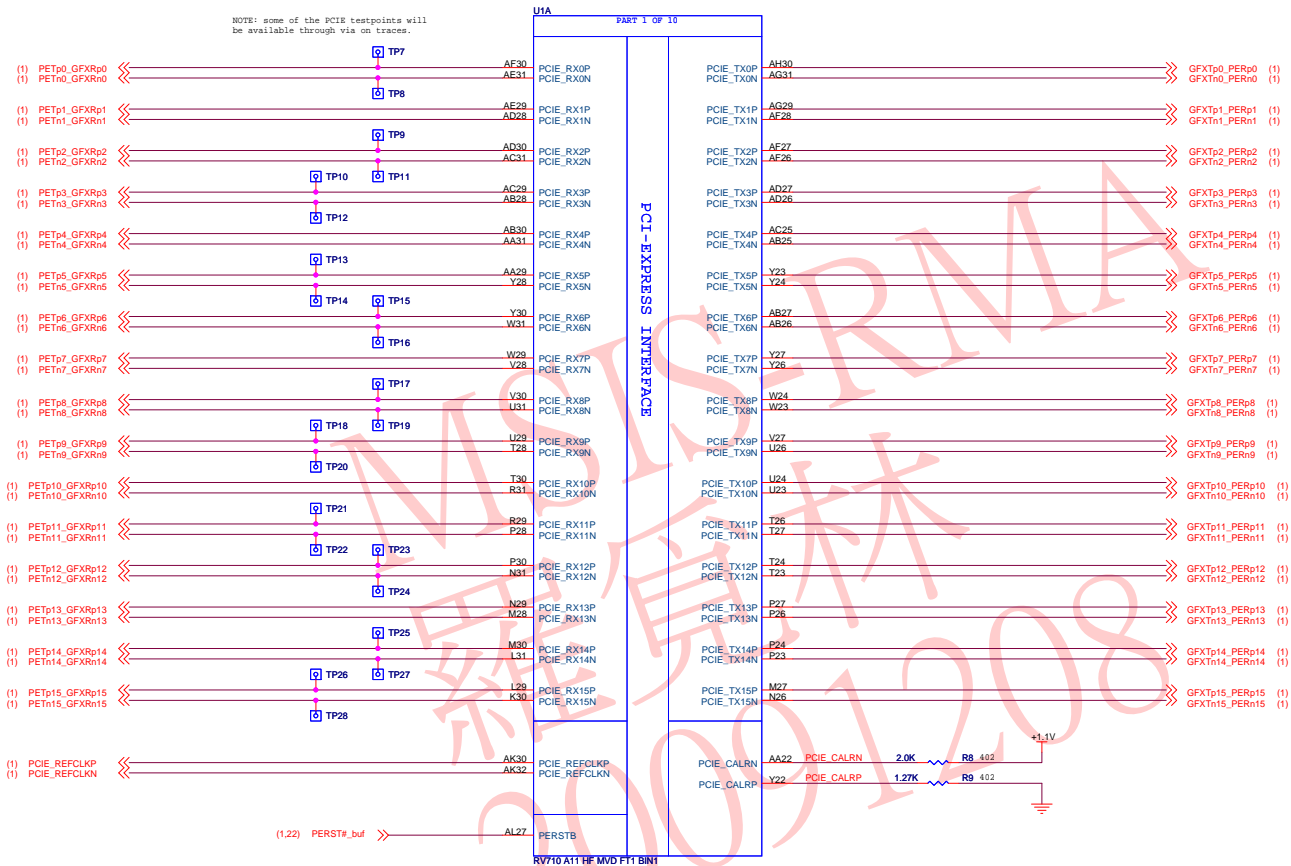


PCI-EXPRESS EDGE CONNECTOR

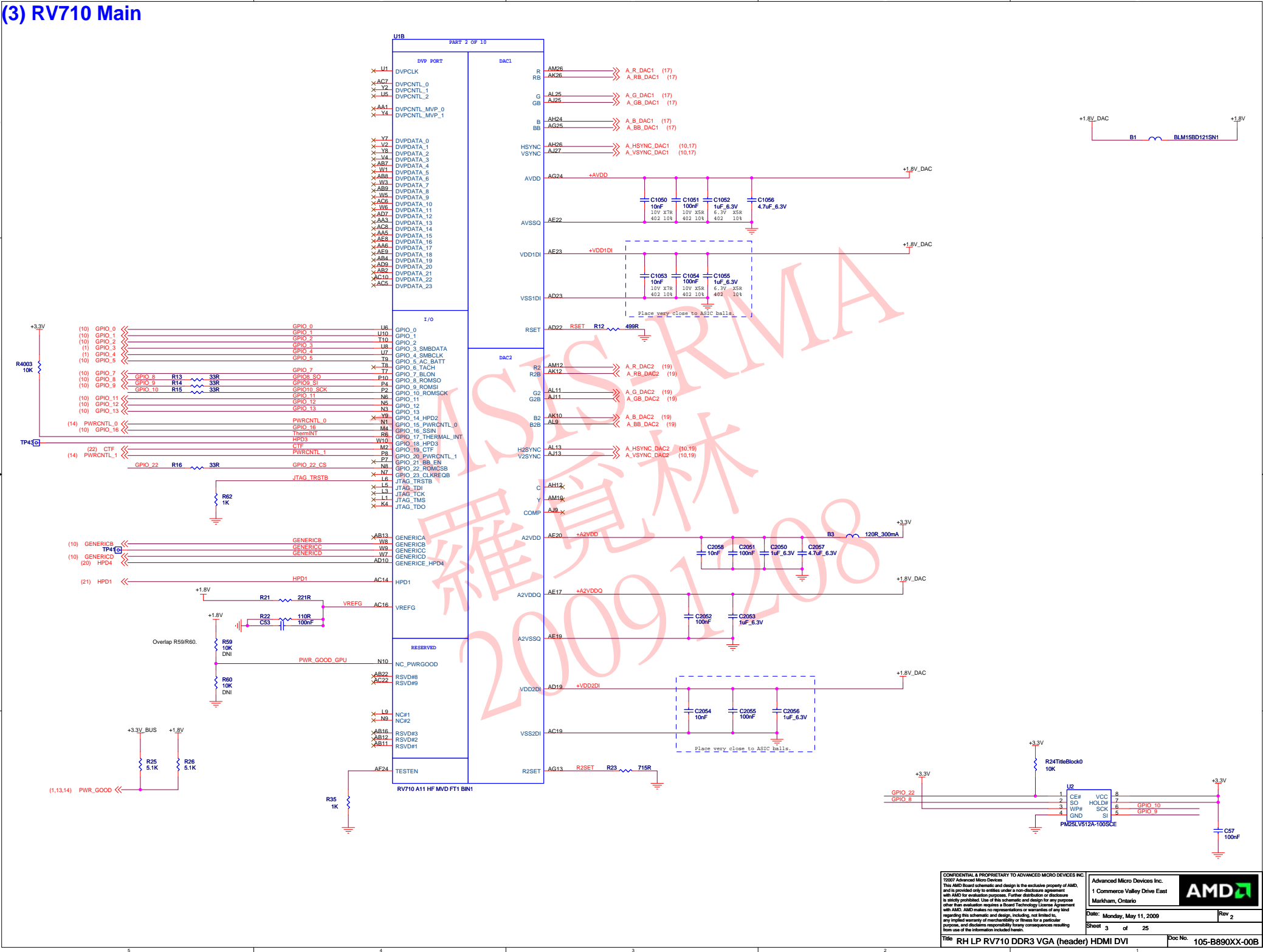


SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

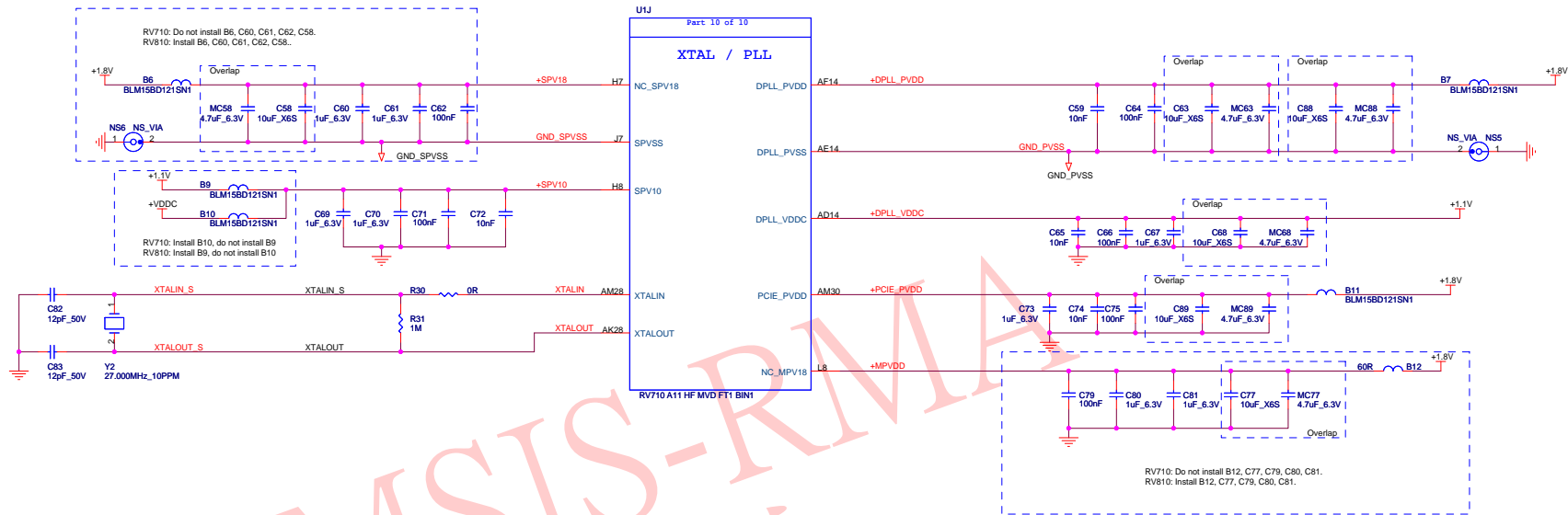
(2) RV710 PCIe Interface



(3) RV710 Main



(04) RV710 GPIOs CF XTAL

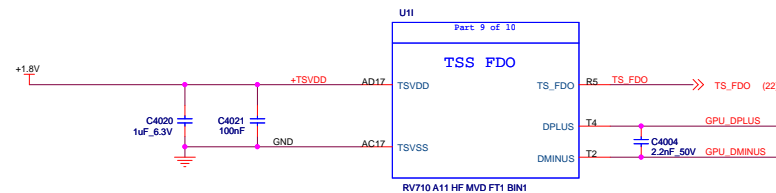
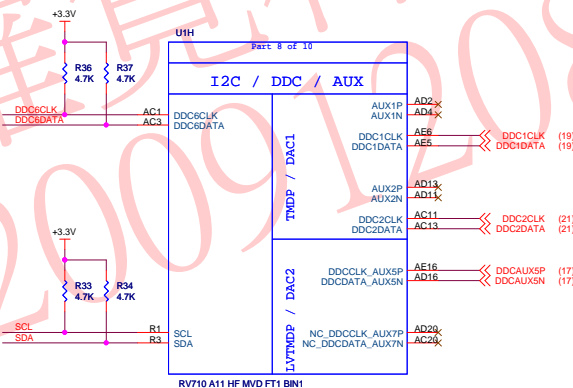


DDC6 BUS:

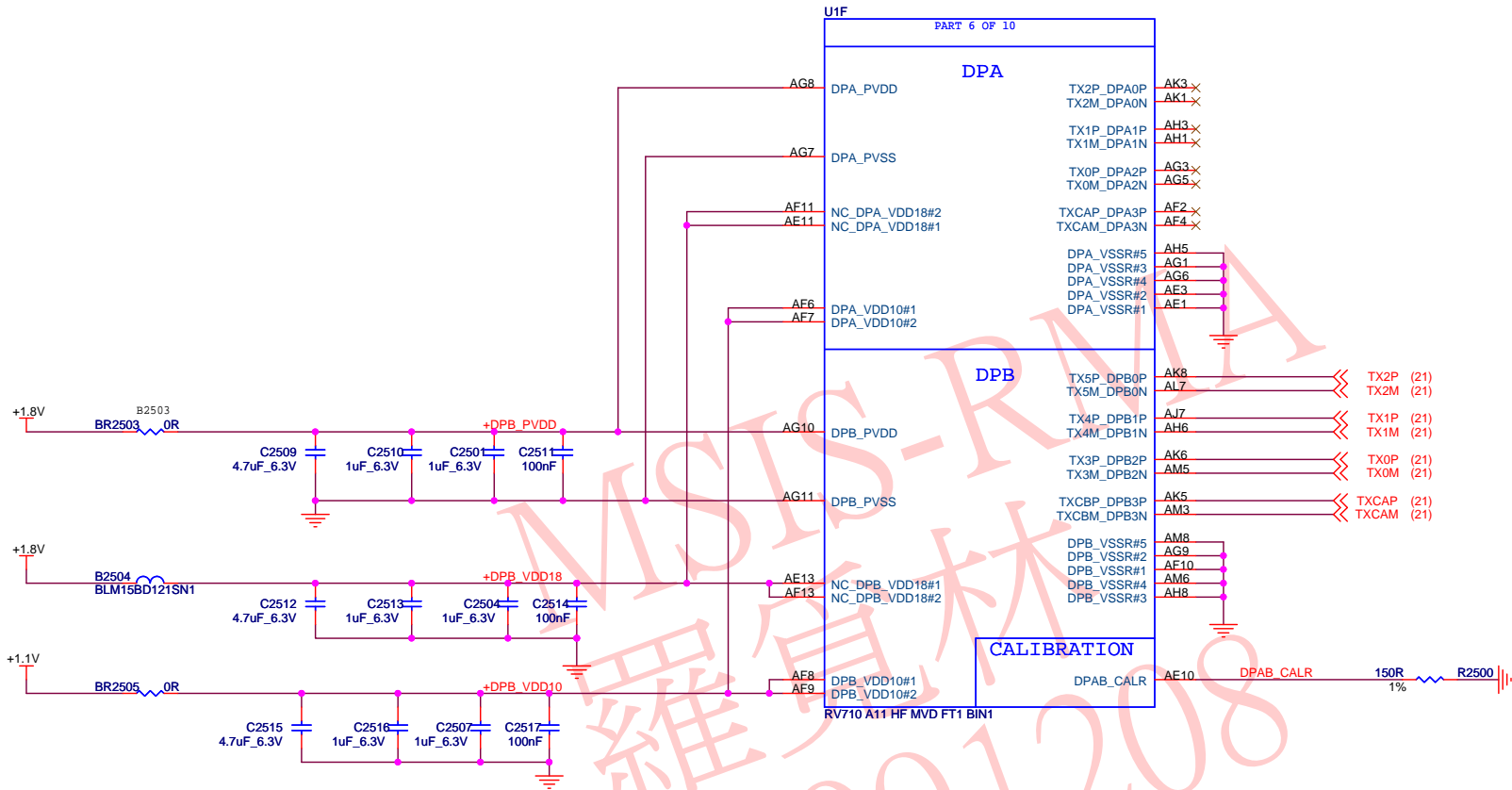
I2C Address	Function	Device
0x90	I2C VDDC Control	DS4402
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:


I2C Address	Function	Device
N/A	N/A	N/A

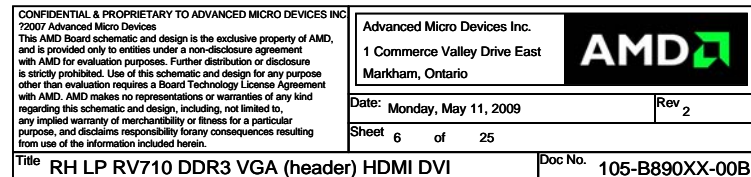


TMDP INTERFACE



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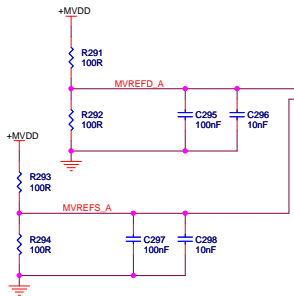
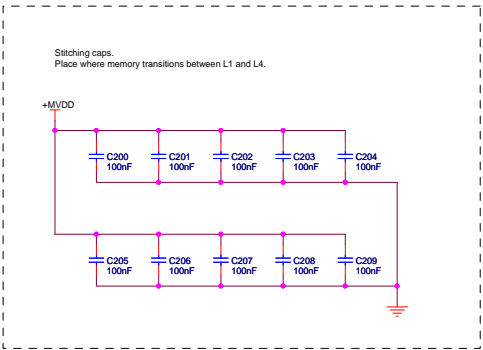
Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario			
Date: Monday, May 11, 2009		Rev 2	
Sheet 5 of 25			
HDMI DVI		Doc No. 105-B890XX-00B	



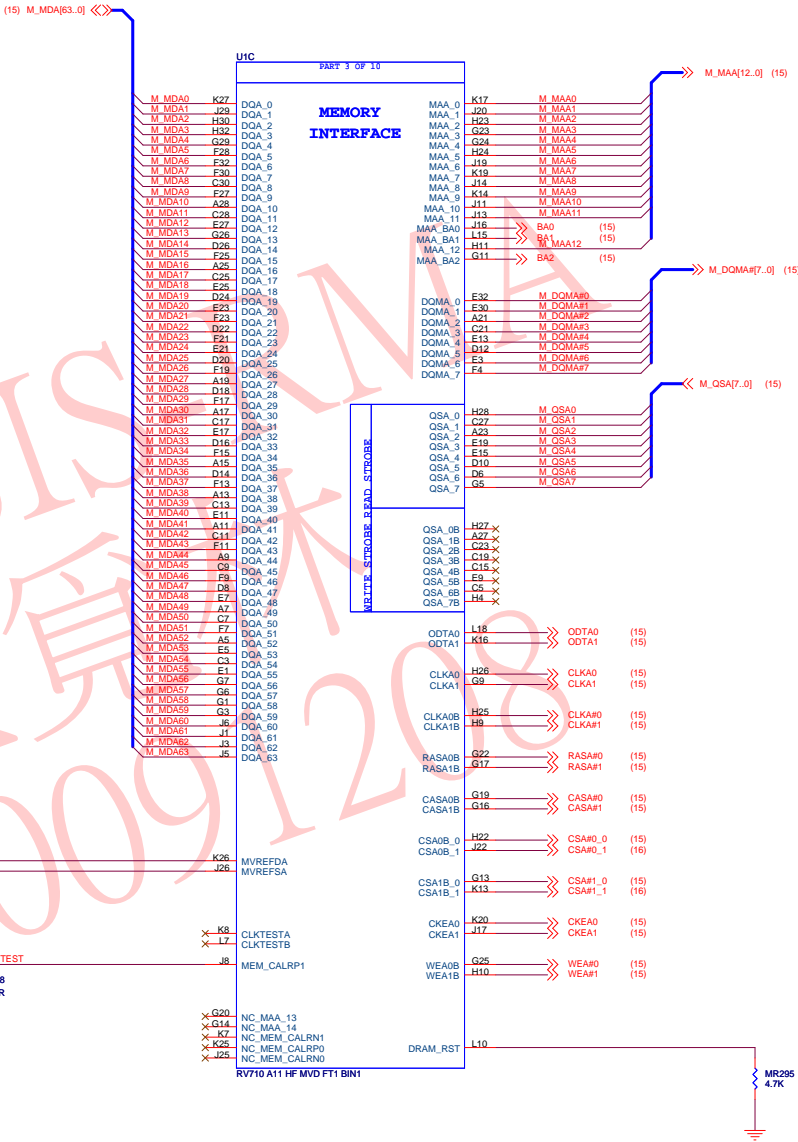
(07) RV710 MEM Interface Ch A

COPY FROM V161 2.1 DDR2 SCH.

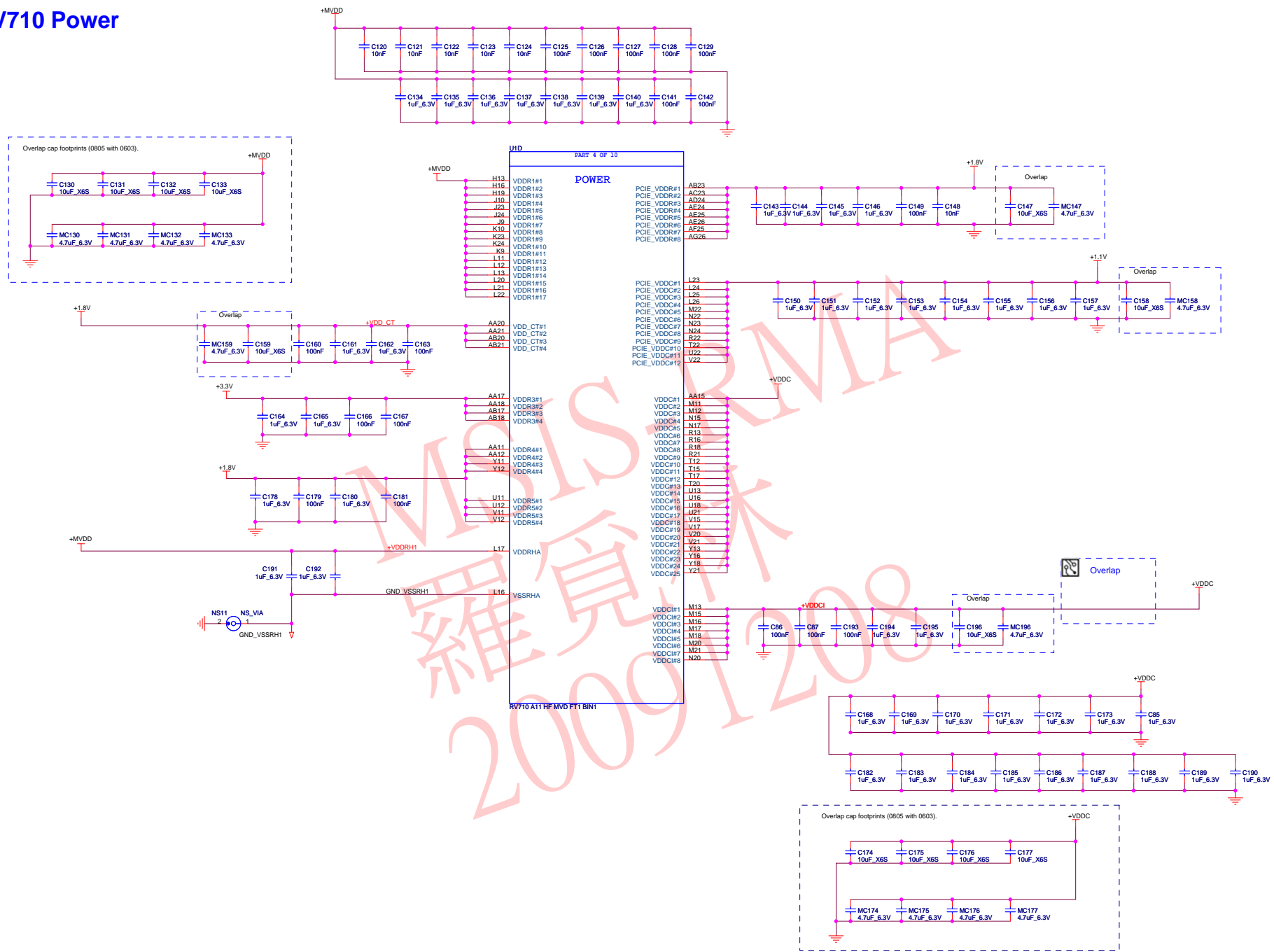
MEMORY INTERFACE



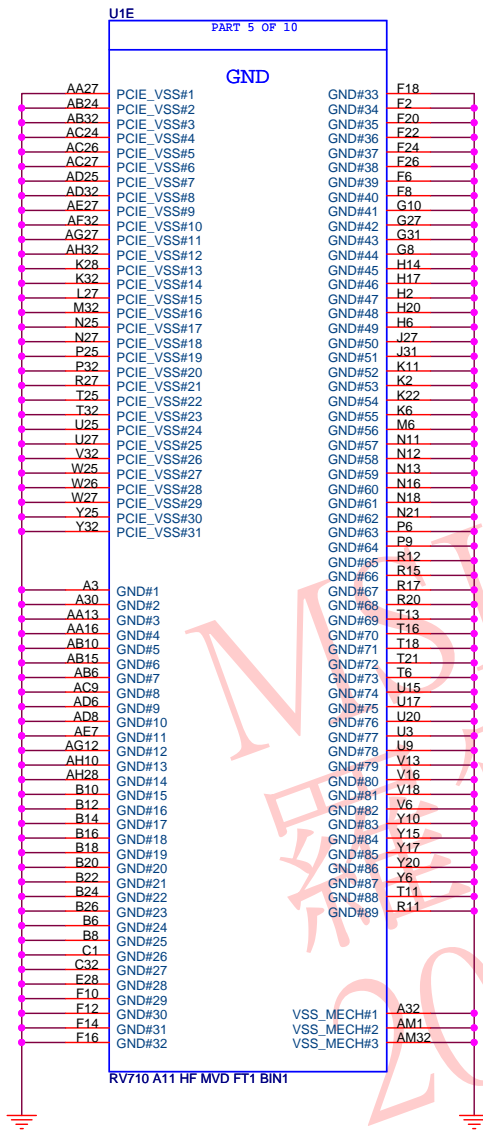
DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R



(08) RV710 Power

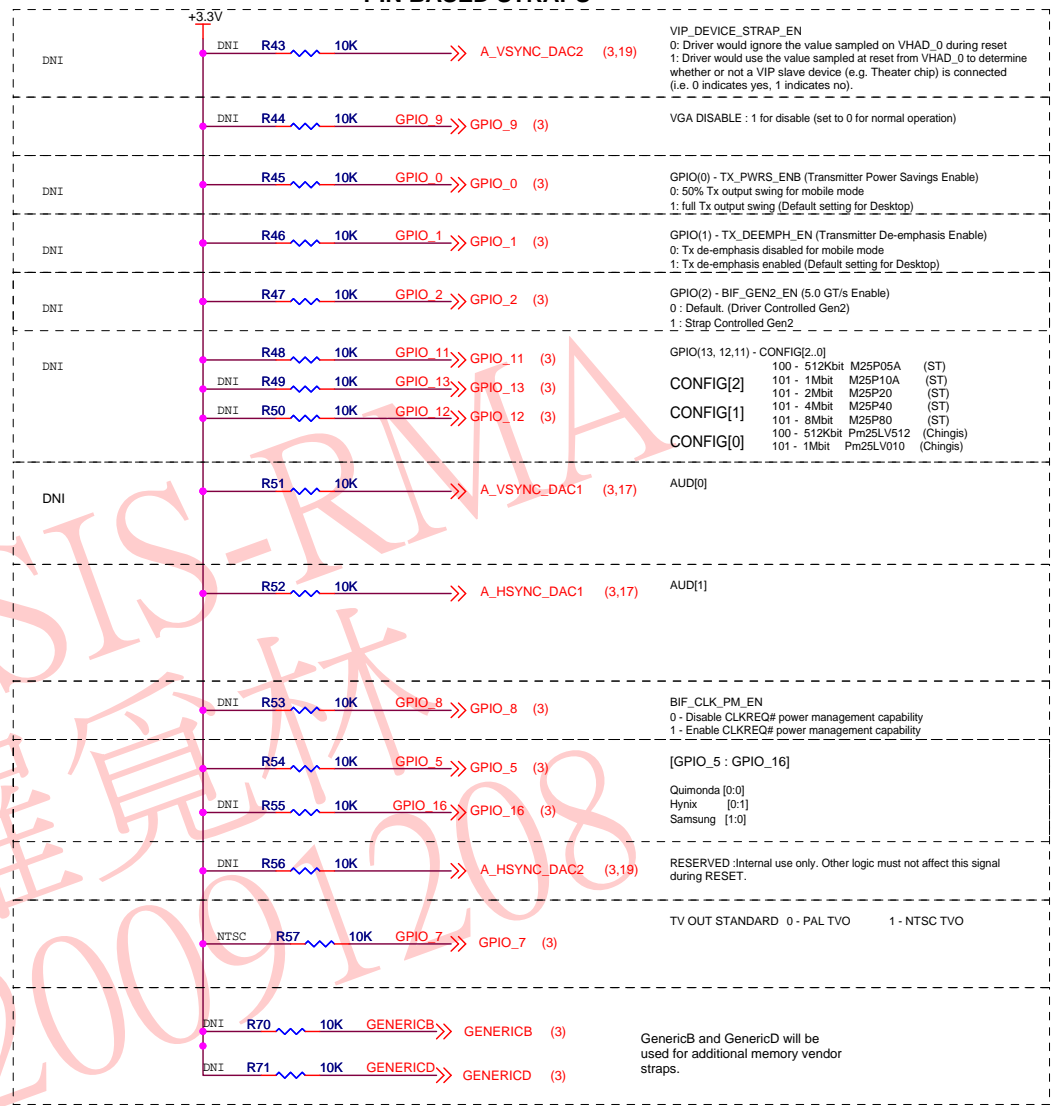


(09) RV710 GND

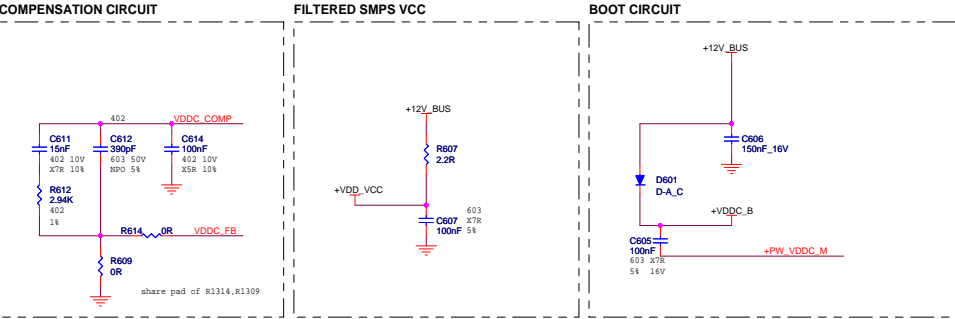
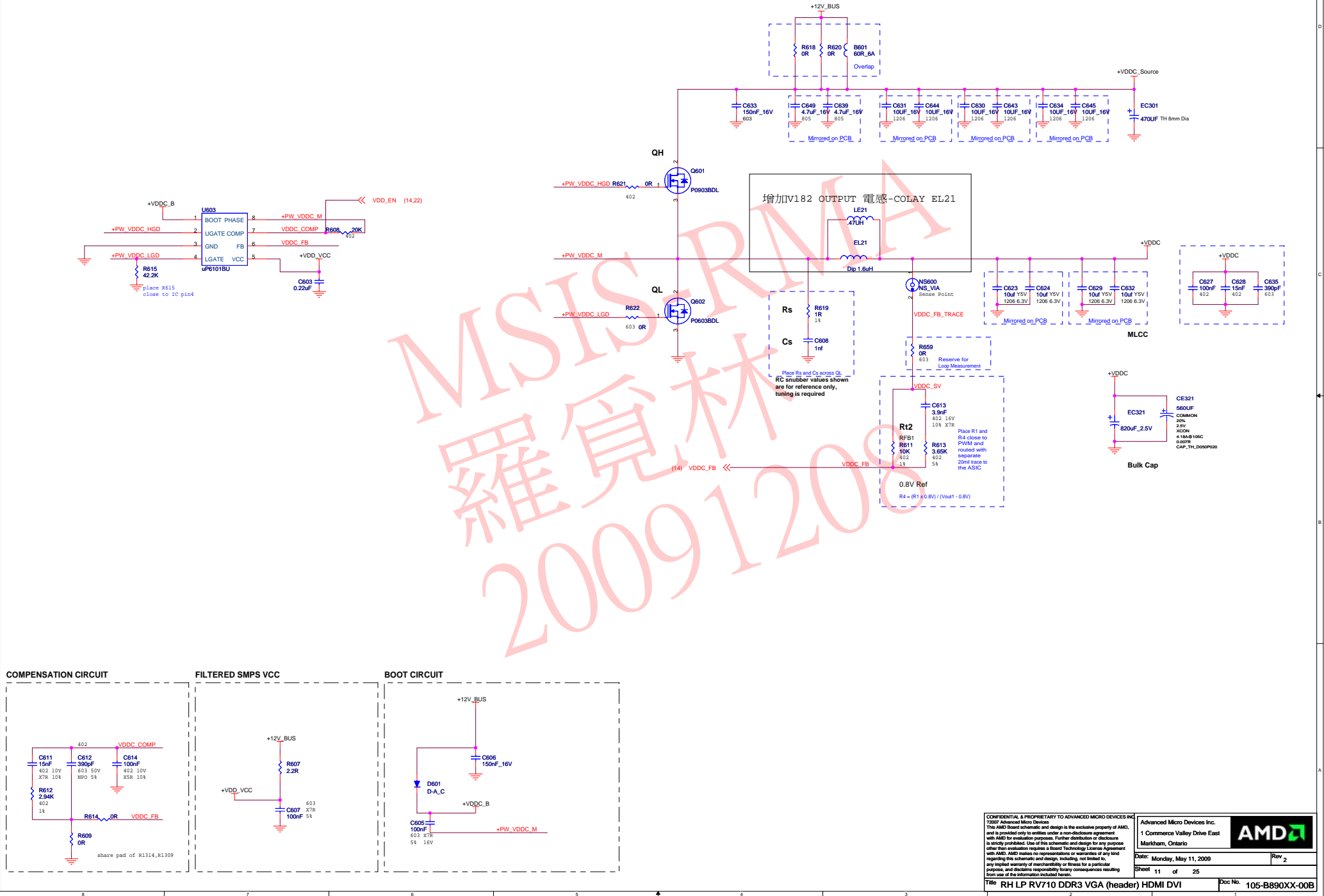


(10) RV710 STRAPS

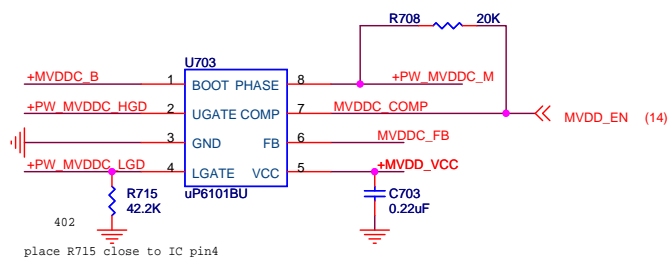
PIN BASED STRAPS



(11) VDDC



(12) MVDD

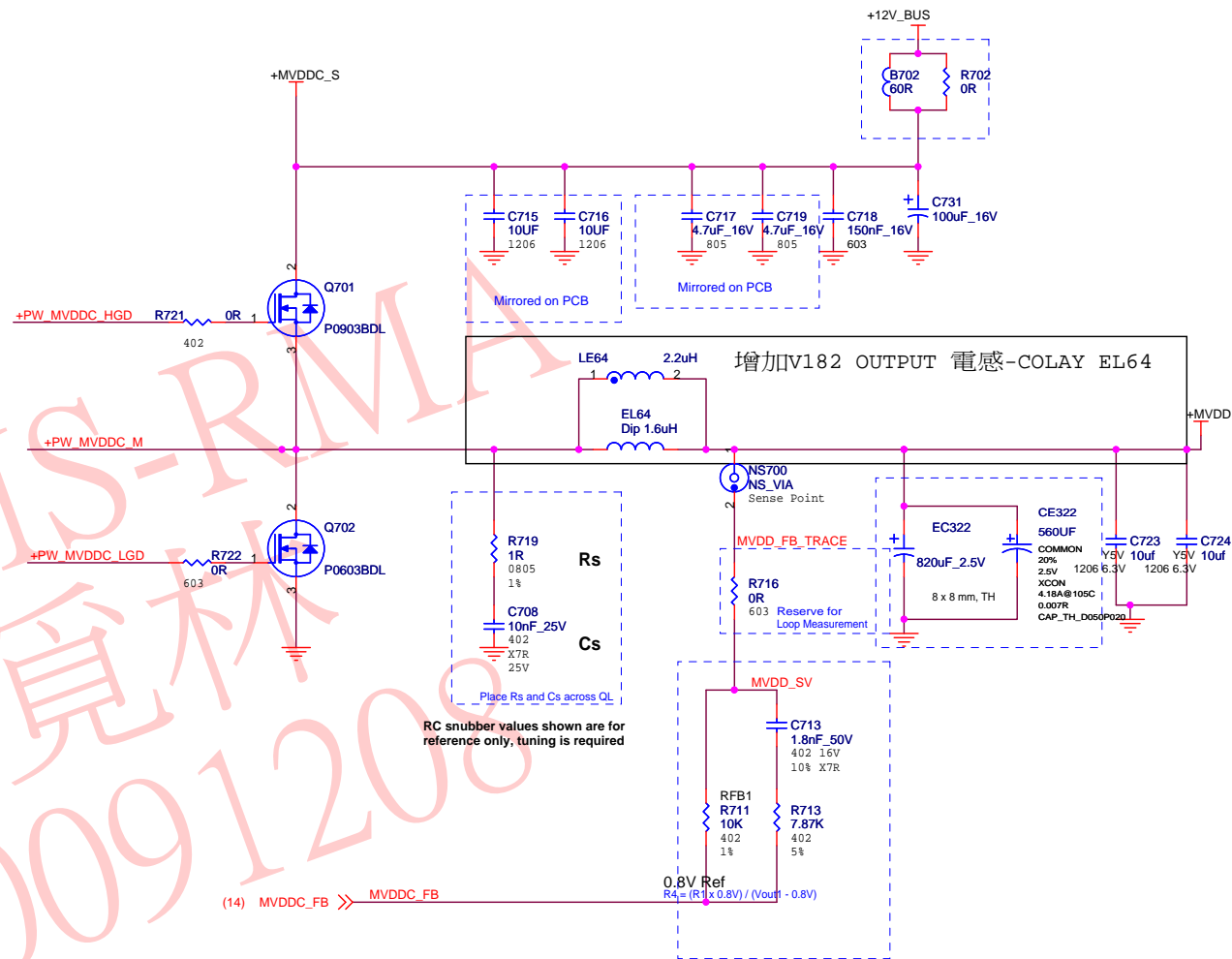
 Layout guideline

1-Position the controller (U703) such that LGate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.

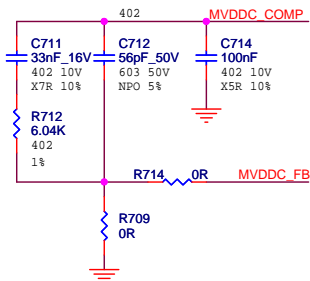
2-Place the bypass capacitors C703 and C705 as close to the Vcc and GND pins of the controller as possible. They are as follows:

Vcc bypass cap is C703, and Boost cap is C705.

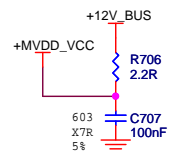
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation components close to the pins and 6. These are R710, R711, R713, C713 and R712, C714 and C715.



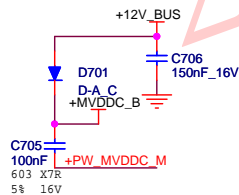
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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Date: Monday, May 11, 2009

Rev 3

Sheet 12 of 25

of 25

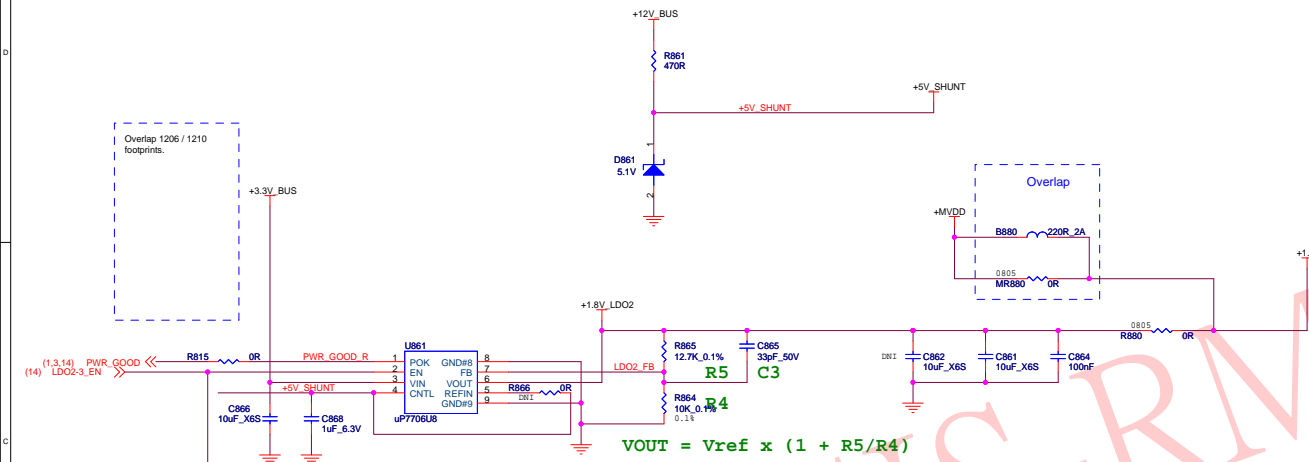
Title	RH LP RV710 DDR3 VGA (header) HDMI DVI
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Doc No.	105-B890XX-00B
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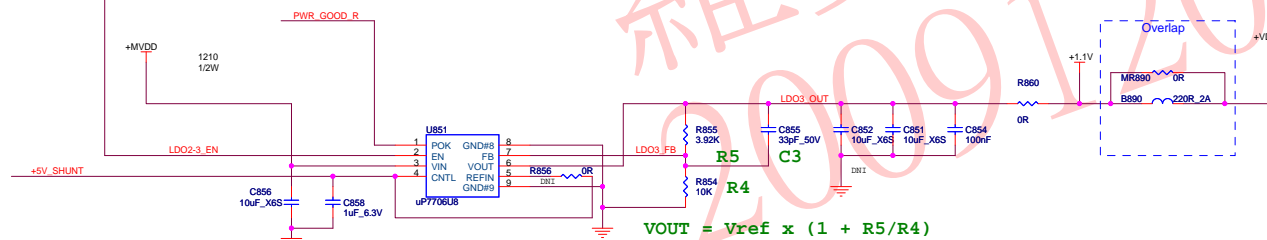
(13) Linear Regulators



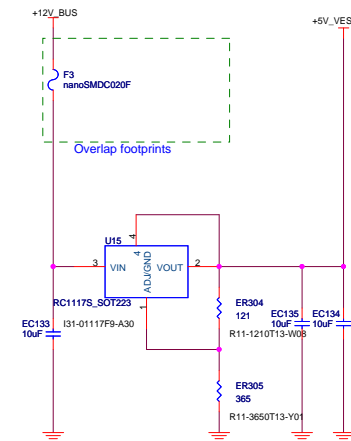
LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #3: Vin = +1.4V to 2.087V MAX Vout = +1.1V +/- 2.5% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

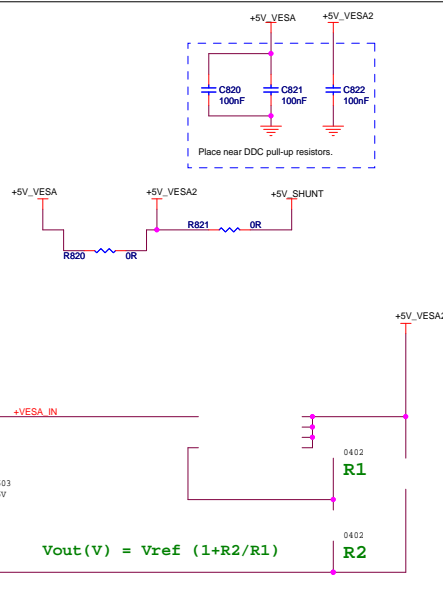


Regulators for +5V_VESA



$$V_{out}=1.25V \cdot [1+(ER305/ER304)]$$

更改+5V_VESA線路,使用1117 (COPY V182)



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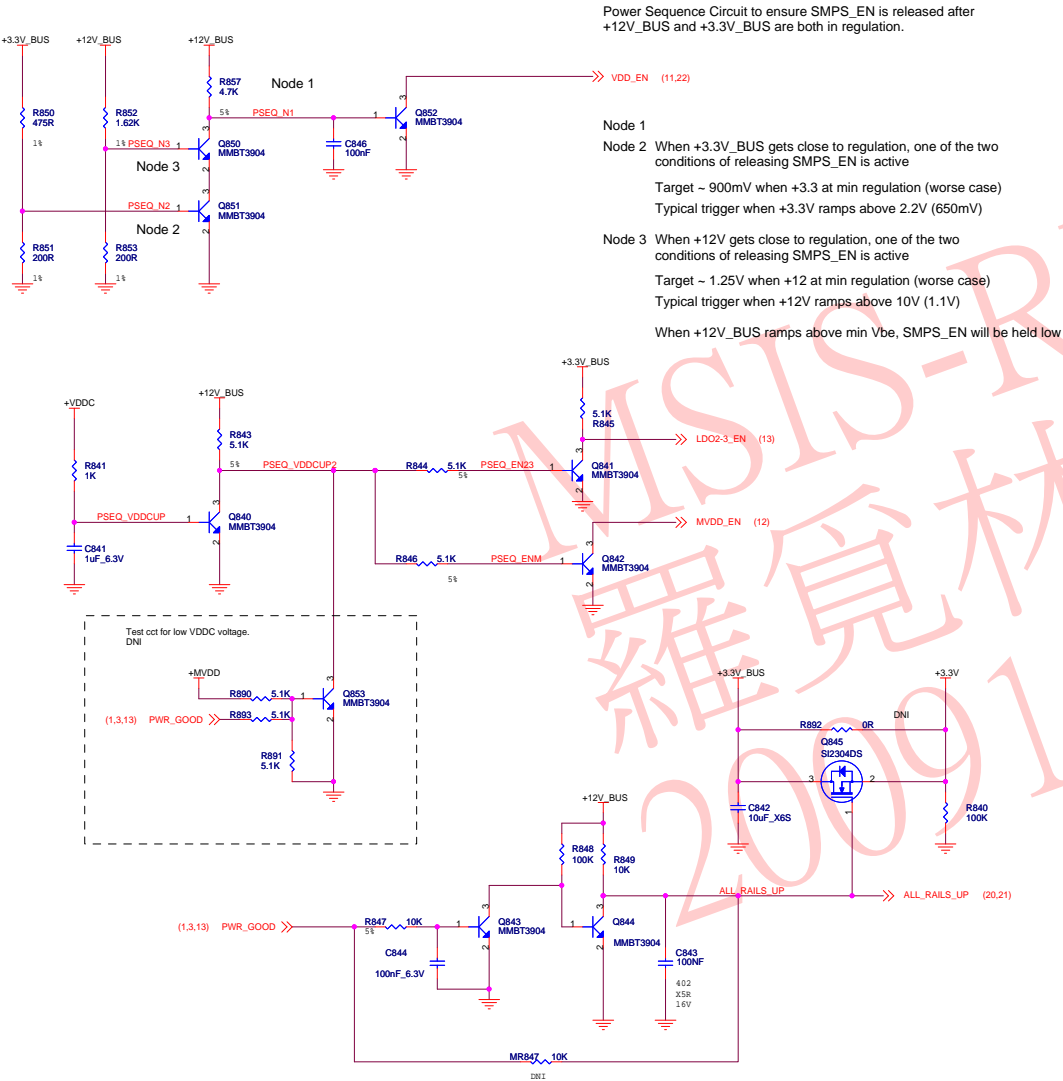
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Markham, Ontario
Date: Monday, May 11, 2009
Sheet 13 of 25
Rev 2



Title RH LP RV710 DDR3 VGA (header) HDMI DVI Doc No. 105-B890XX-00B

(14) Power Management

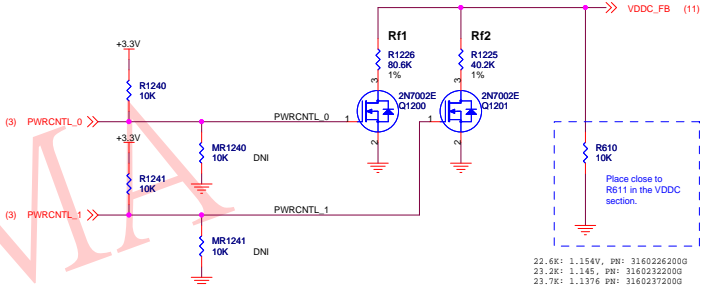
Power up/down Sequencing



Power Play

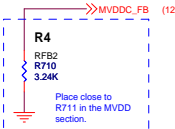
VDDC Voltage Settings Using GPIOs

		Output Voltage (V)			
PWRCTRL_1 GPIO_20	PWRCTRL_0 GPIO_15	RE1= RE2=	RE1= RE2=	RE1= RE2=	
0	0				
0	1				
1	0				
1	1	1	0	1	Power-up Default



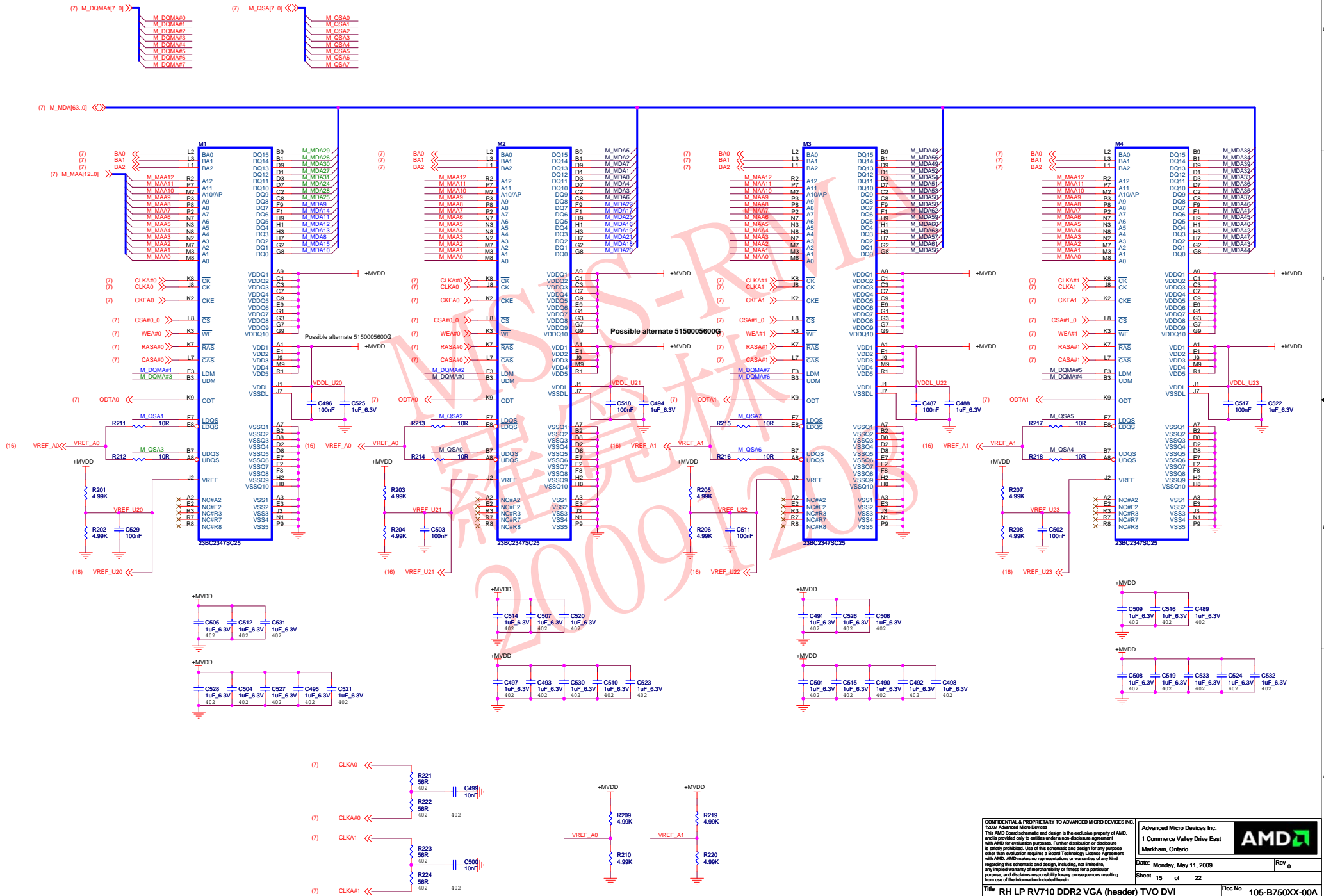
MVDD Voltage Settings Using GPIOs

		Output Voltage (V)			
PWRCTRL_2 GPIO_6		RE1= RE2=	RE1= RE2=	RE1= RE2=	
0					
1		1	0	1	Power-up Default



CHANNEL A: RANK 0 512MB DDR2

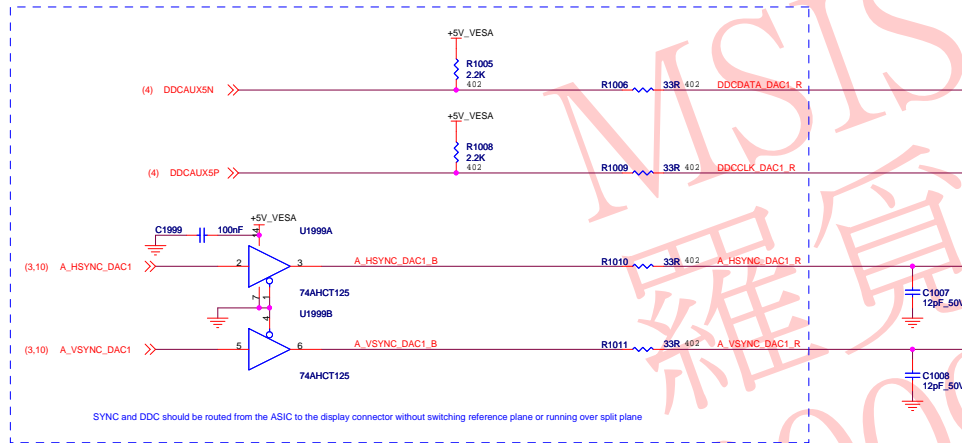
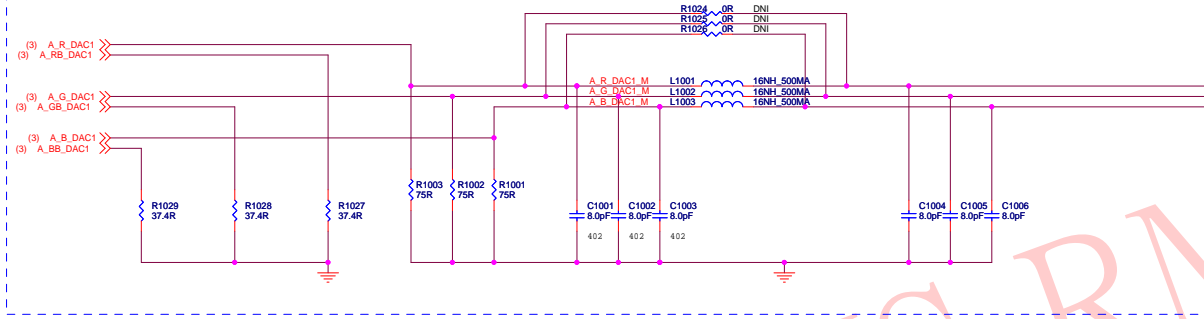
MAX DENSITY: 64Mx16



DAC 1 OUTPUT

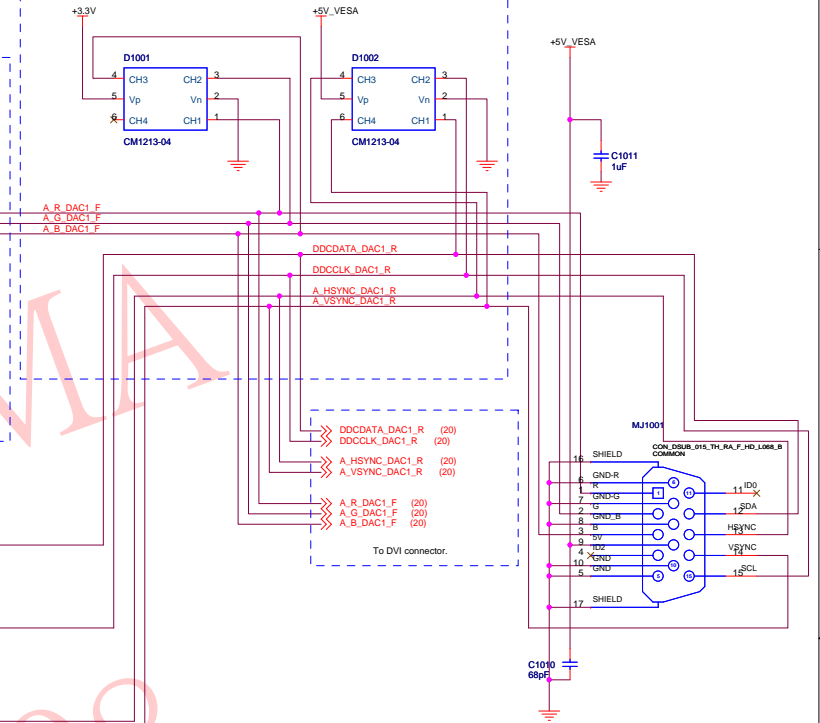


Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)



Optional ESD Protection Diodes

Place close to Connector
ALLOW FOR A LOW INDUCTANCE PATH TO PIN 5



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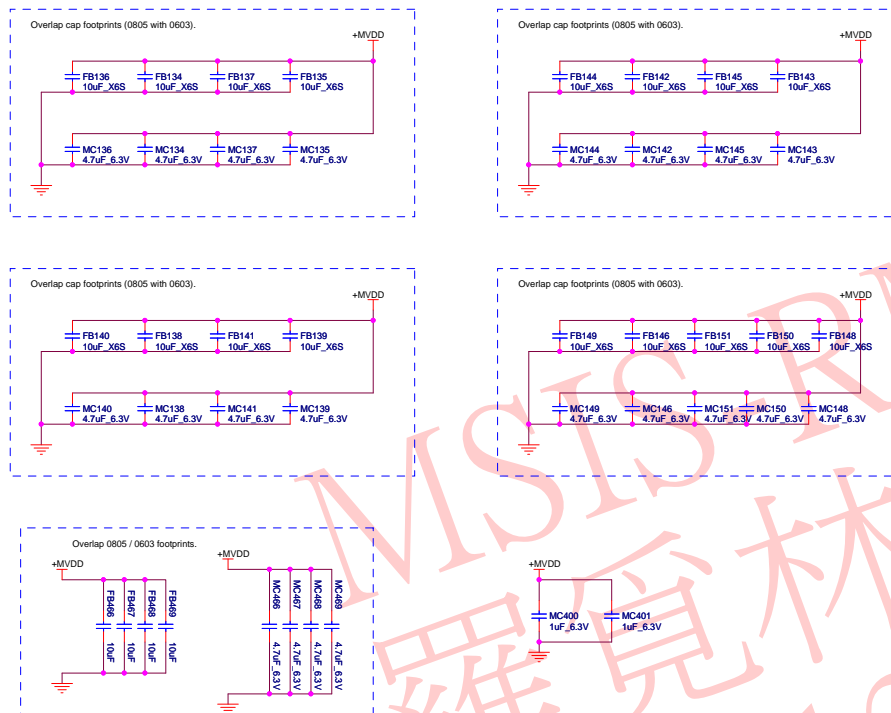
Rev 2

Sheet 17 of 25

Doc No. 105-B890XX-00B

Title RH LP RV710 DDR3 VGA (header) HDMI DVI

(17) DDR3 Termination



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Rev 2

Sheet 18 of 25

Title RH LP RV710 DDR3 VGA (header) HDMI DVI

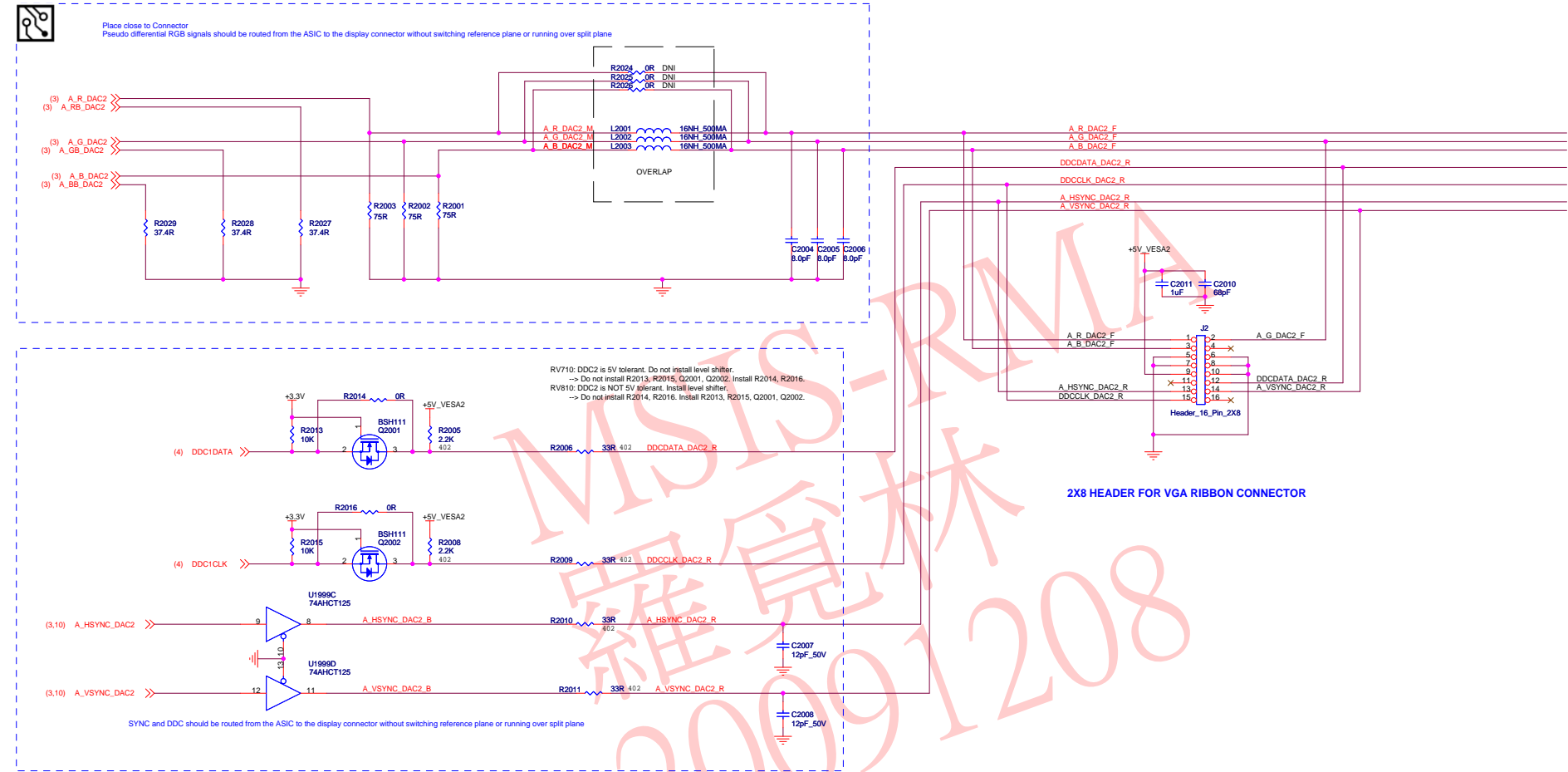
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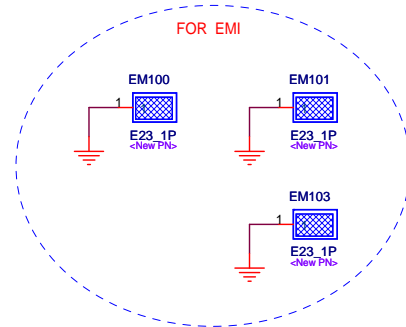
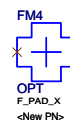
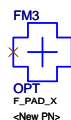
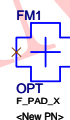
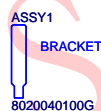
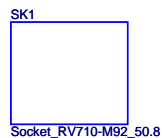
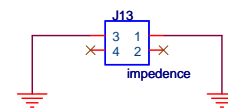
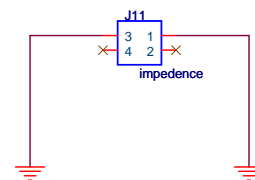
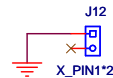
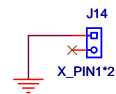
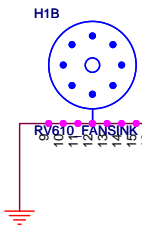
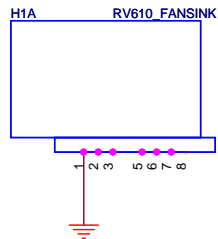
DAC 2 OUTPUT

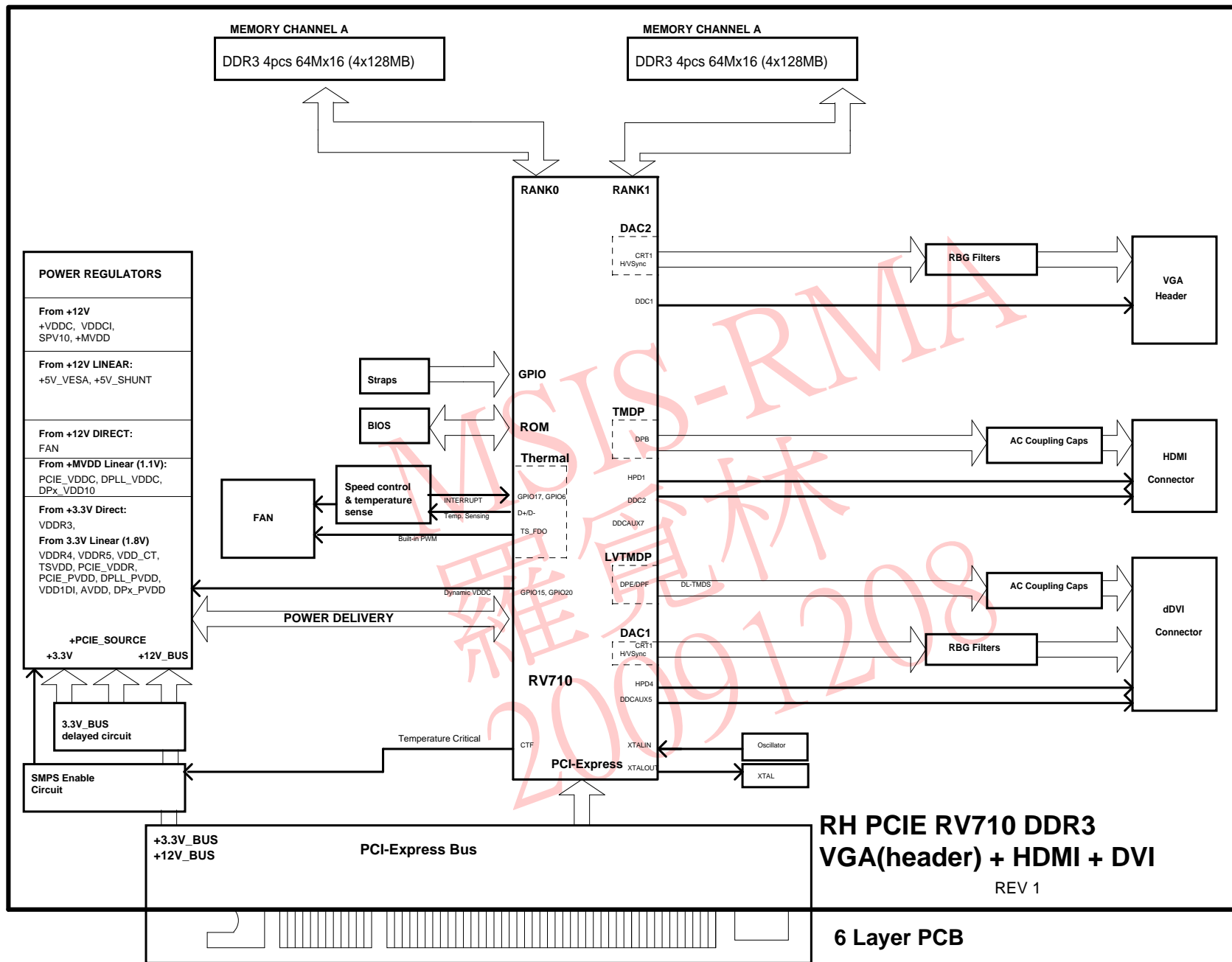
Optional ESD Protection Diodes

Place near D2002, D2003, D2004, D2005

Place close to Connector







<div>AMD</div>			Title		Schematic No.		Date:	
			RH LP RV710 DDR3 VGA (header) HDMI DVI		105-B890XX-00B		Monday, May 11, 2009	
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.					Rev 2
			RV710 ENGINEERING BOARD			REVISION DESCRIPTION		
Sch Rev	PCB Rev	Date						
0	00A	2008.12.30	INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.					
1	00B	2009.01.22	Sch no change. just modify HDMI connnecro location on PCB					
			<div>MSIS-RMA 羅覓林 20091208</div>					