

P727-A01: G96, GB1-128, GDDR3, DL-DVI, DL-DVI/VGA, SD/HDTV

V129-122

PAGE SUMMARY:

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- Page 22: POWER SUPPLY LINEARS: 5V, DDC5V, IFP PLLVDD, IFP IOVDD, MIO VDD, 3V3 FILTER, 12V FILTER
- Page 23: POWER SUPPLY: FBVDDQ +PEX_VDD SINGLE PHASE SWITCHER
- Page 24: POWER SUPPLY: NVVDD DUAL PHASE SWITCHER
- Page 25: POWER SUPPLY: Dynamic NVVDD

REV 1.2 HISTORY

04/01

PAGE 12.Remove J1 Slim-DSUB connector

PAGE 15.Add R761 and R762 to reserve pull down DP AUX
Change F503 and F504 footprint to 1812 size
Remove DP J8 Pin25,Pin26

PAGE 18.Change U514~U517 to EM1~EM6

PAGE 19.Add 2pin Fan control circuit

PAGE 23.Add C120,C149 10uF 1206 footprint to reserve PEX_VDD power

04/08

PAGE 22. Add R92 0805 0ohm Resistor for 3V3 bypass to 2V5 power

REV 1.21 HISTORY

06/04

PAGE 20.Add R774 10K pull down resistor for HDA issue

REV 1.22 HISTORY

07/16

PAGE 22. Reverse Diode at 5V regulator input side to prevent Leakage to 12V

PAGE 22. Reverse CAP SOLID for A2V5

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10727-0000-001	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKJ0000	600-10727-0000-100	G96-A01, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
2	SKJ0001	600-10727-0001-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
3	SKJ0002	600-10727-0002-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI
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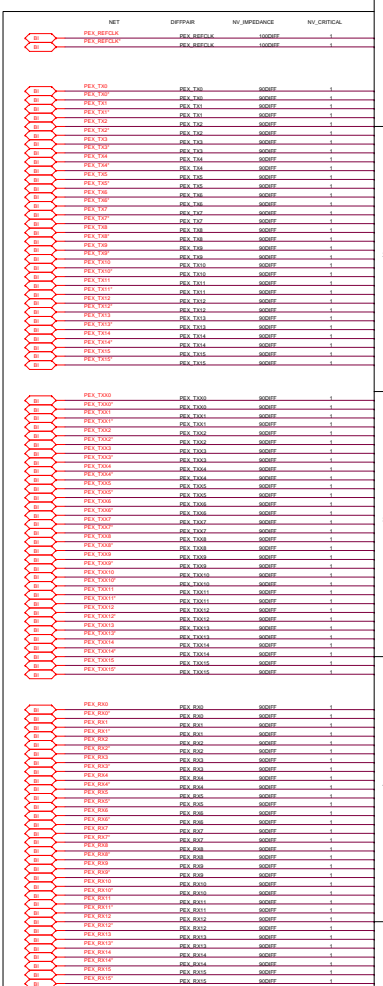
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PAGE DETAIL	TABLE OF CONTENTS

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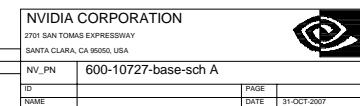
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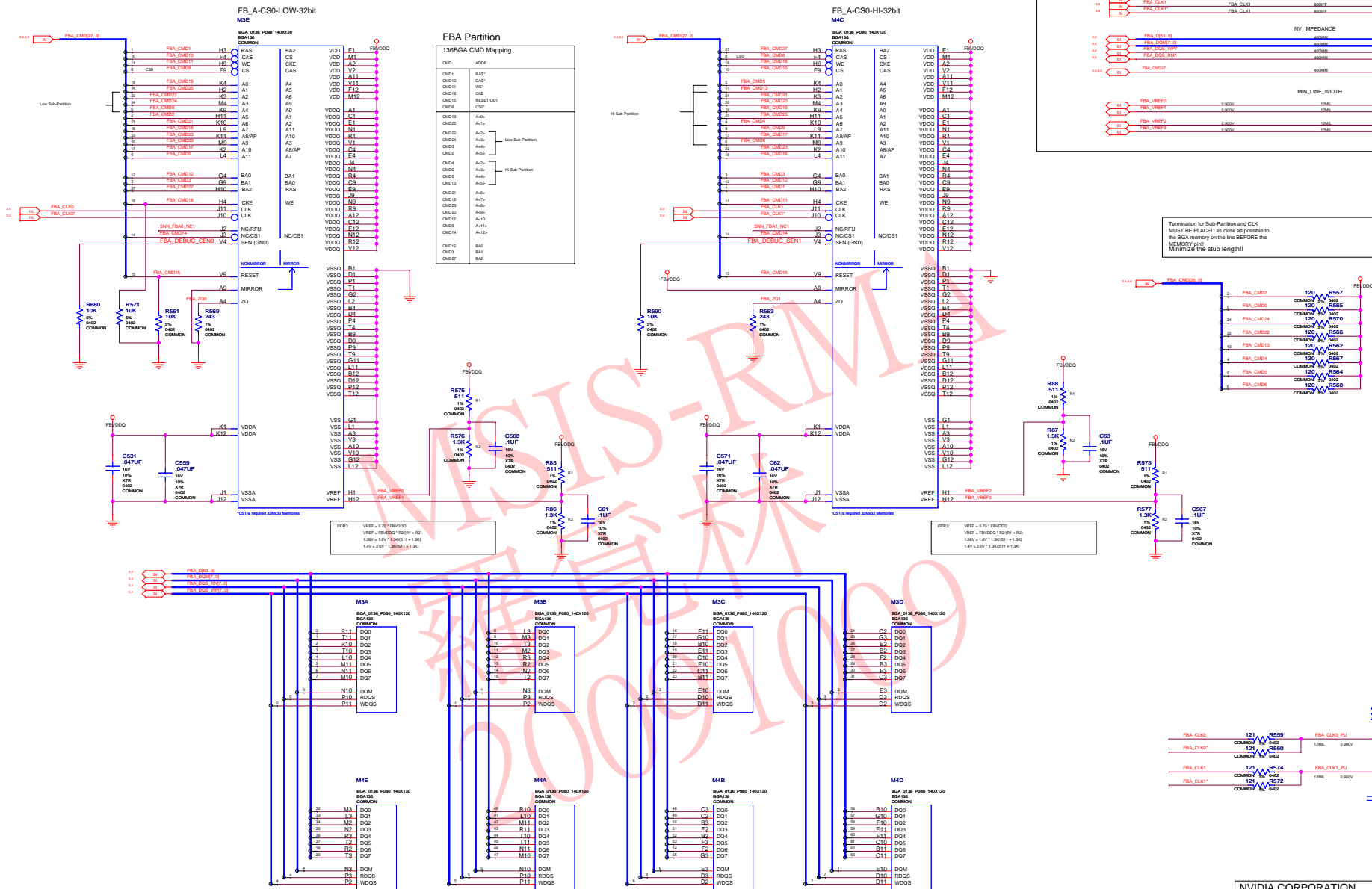
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FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3



1368GA CMD Mapping		
CMD	ADDR	
CM01	RAS*	
CM010	CAS*	
CM011	WE*	
CM018	CHE	
CM015	RESET/ODT	
CM08	CS0*	
CM018	Ar0*	
CM025	Ar1*	
CM022	Ar0*	} Low Sub-Partition
CM024	Ar0*	
CM02	Ar0*	
CM02	Ar0*	
CM05	Ar0*	
CM06	Ar0*	} HS Sub-Partition
CM05	Ar0*	
CM013	Ar0*	
CM021	Ar0*	
CM016	Ar0*	
CM023	Ar0*	
CM030	Ar0*	
CM017	Ar10	
CM09	Ar11*	
CM14	Ar12*	
CM012	BA0	
CM03	BA1	
CM027	BA2	

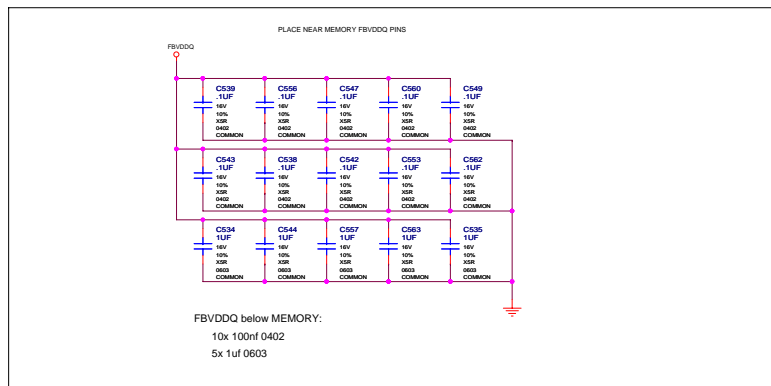
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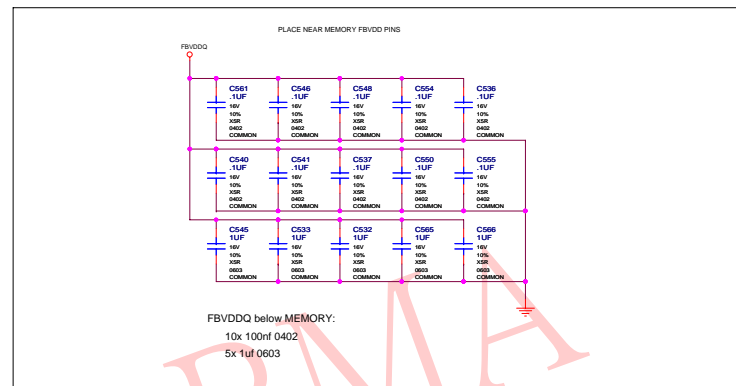
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PAGE DETAIL	FBA 16/32Mx32 GDDR3 MEMORIES, FBA COMMAND BUS PU'S, FBA CLK TERMS

FRAME BUFFER: PARTITION A DECOUPLING

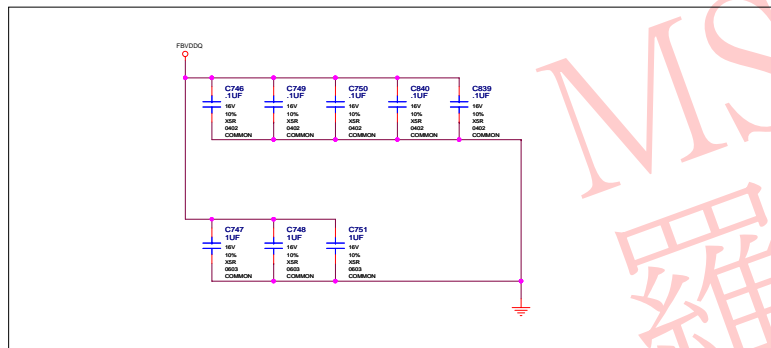
Decoupling for FBA 0..31



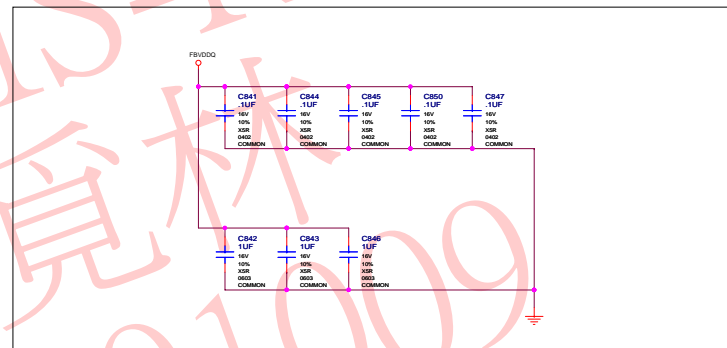
Decoupling for FBA 32..63



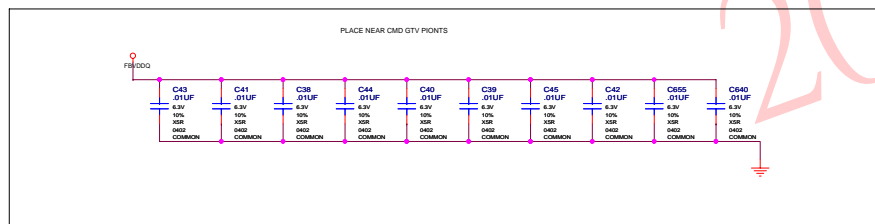
Decoupling for FBA A1 0..31



Decoupling for FBA A1 0..31



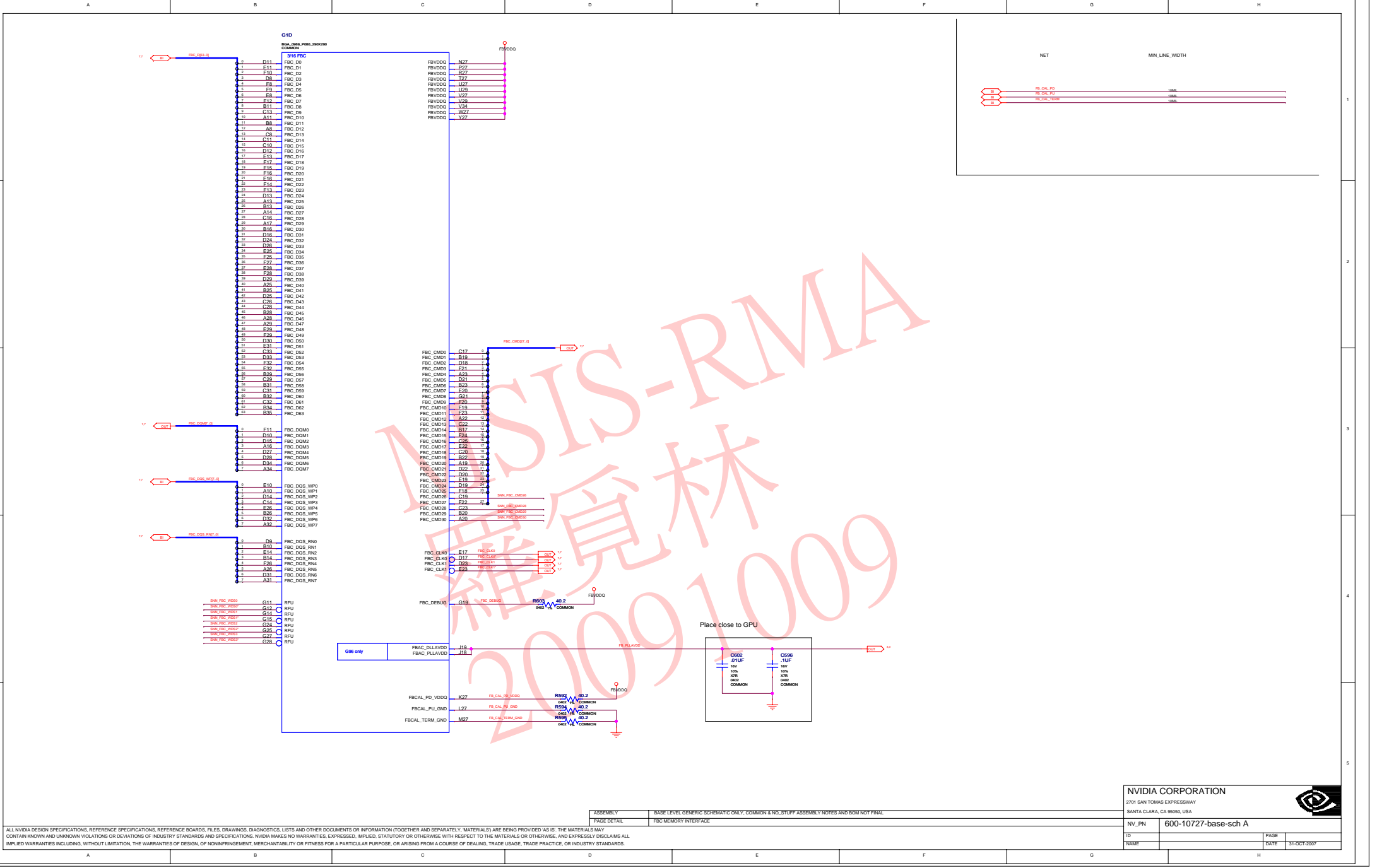
Return path coupling GND/FBVDDQ for FBA



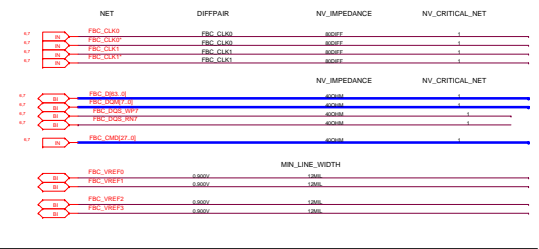
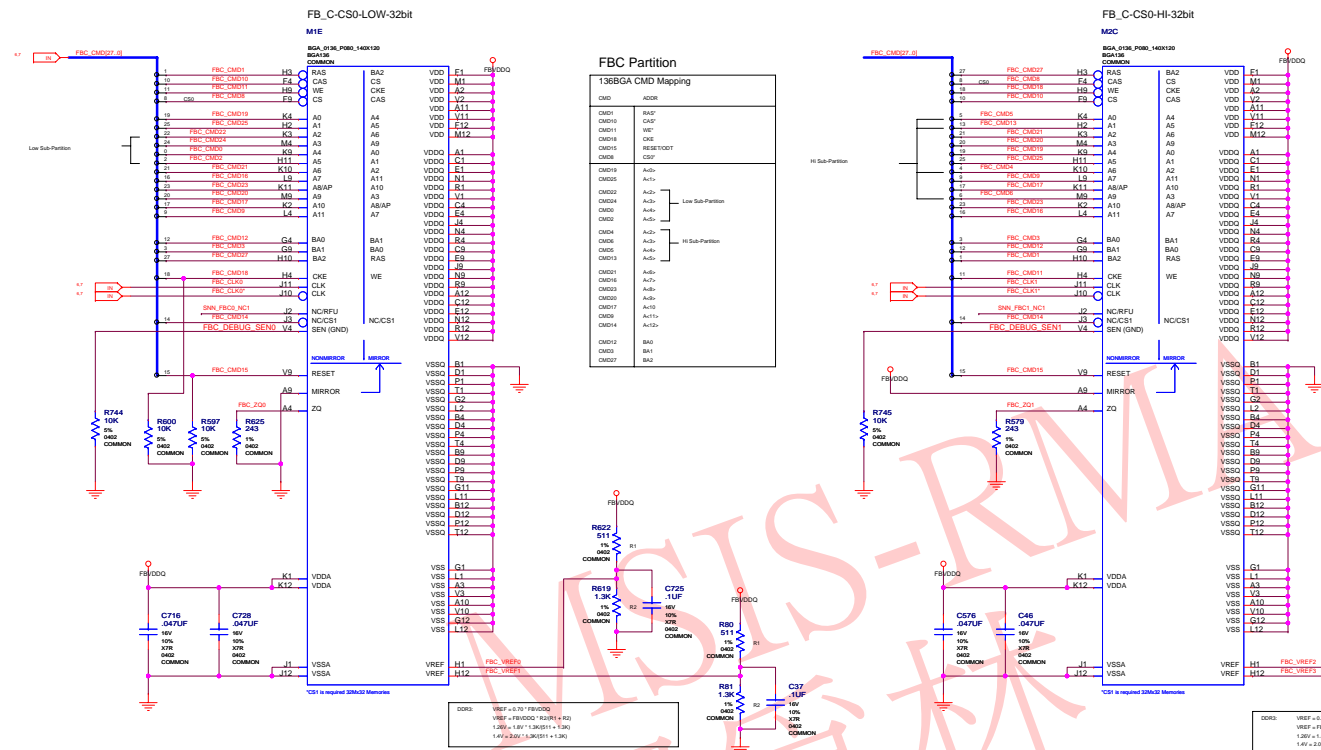
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

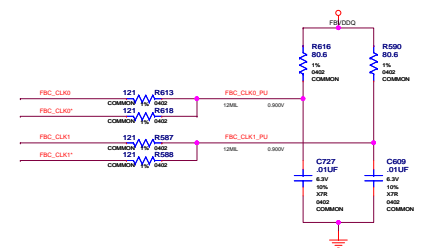
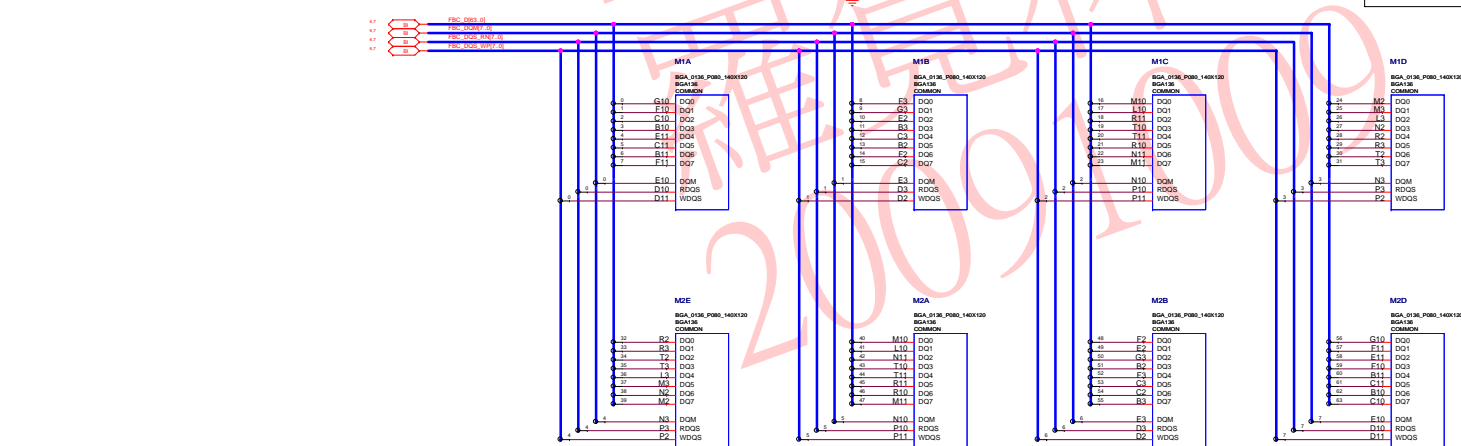
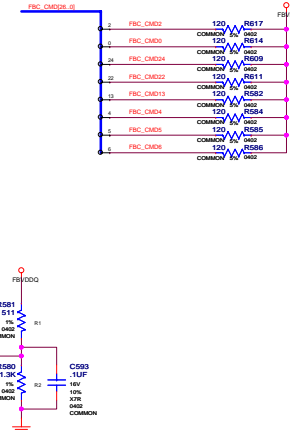
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FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3



Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!



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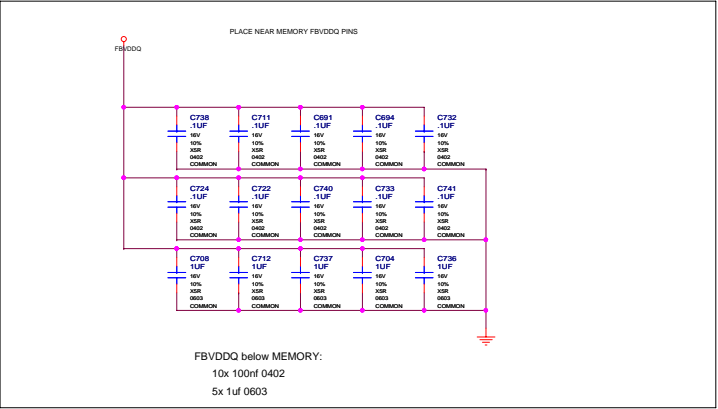
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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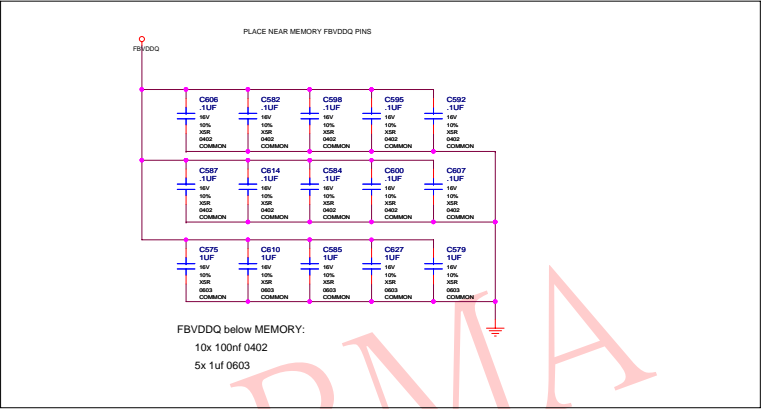
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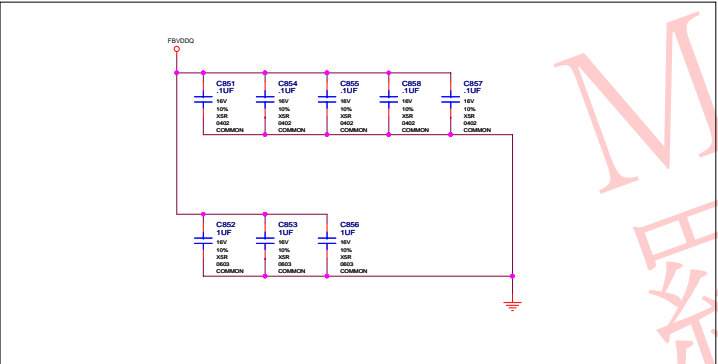
Decoupling for FBC 0..31



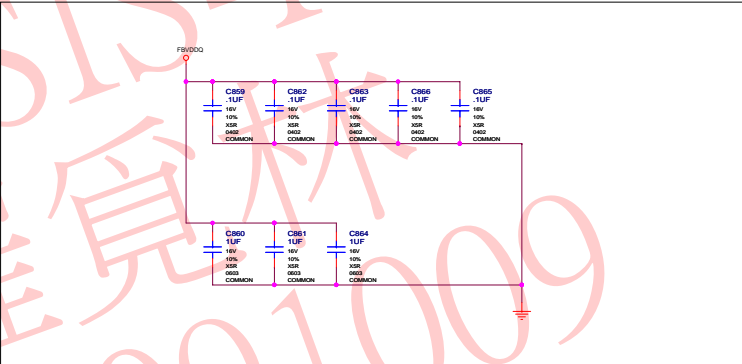
Decoupling for FBC 32..63



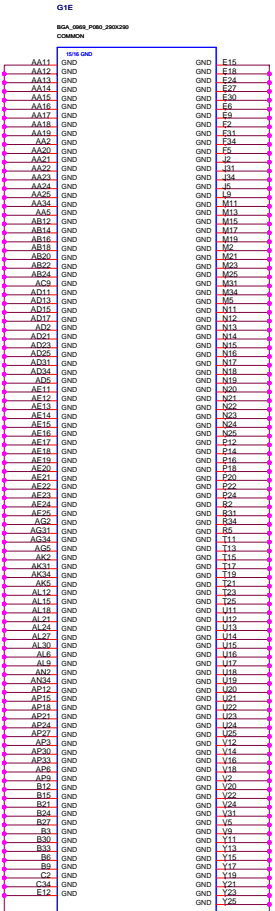
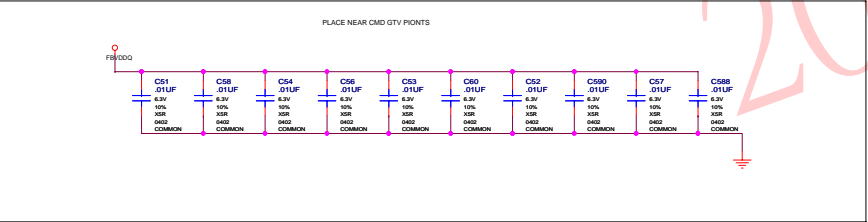
Decoupling for FBC C1 0..31



Decoupling for FBC C1 32..63



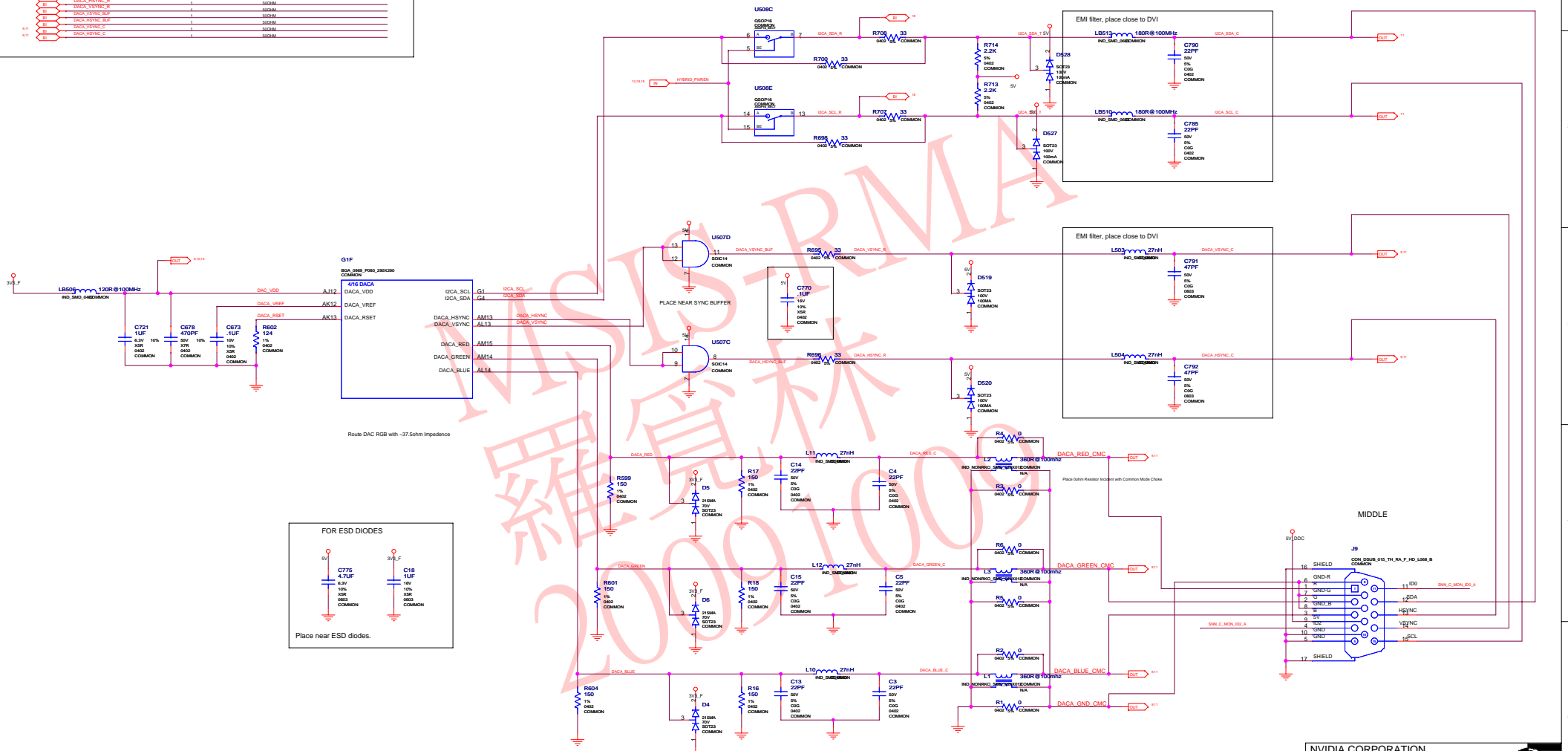
Return path coupling GND/FBVDDQ for FBC



	NET_NAME	WV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
6.3.1.4	IN			3.30 120M
	DATA_VDD			
IN	DATA_VREF			120M
IN	DATA_VBIAS			120M
	DATA_RSD	1	75OHM	
IN	DATA_GREEN	1	75OHM	
IN	DATA_BLUE	1	75OHM	
	DATA_RSD_C	1	75OHM	
IN	DATA_GREEN_C	1	75OHM	
IN	DATA_BLUE_C	1	75OHM	
6.3.1.5	DATA_GND_CMIC			0V 120M
6.3.1	DATA_GREEN_CMIC	1	75OHM	
6.3.1	DATA_BLUE_CMIC	1	75OHM	
6.3.1	DATA_VBIAS_CMIC	1	75OHM	
	DATA_VBIAS	1	50OHM	
	DATA_VREF	1	50OHM	
	DATA_VREF_B	1	50OHM	
	DATA_VREF_R	1	50OHM	
	DATA_VREF_BUF	1	50OHM	
	DATA_VREF_BUF	1	50OHM	
6.3.1	DATA_VREF_C	1	50OHM	
	DATA_VREF_C	1	50OHM	

Primary Display (DACA), DVI-I

DACA RGB-FILTER



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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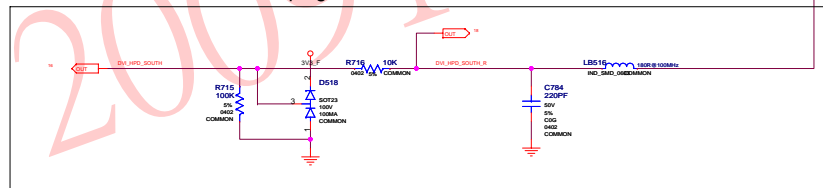
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TMD5 LINK: A & B

PCB layout showing TMD5 LINK: A & B. The layout includes power planes (GND, VDD), decoupling capacitors (C734, C735, C723, C730, C719, C729, C682, C701), and a detailed netlist table. The netlist table lists components like AM12, AM11, AL8, AM8, AM9, AM10, AL10, AK10, AL11, AK11, AN13, AP13, AP8, AN8, AN10, AP10, AR10, AK11, AP11, AN11, and their connections to various nets. The layout also shows a 1200R @ 100MHz termination resistor and a 4700PF capacitor.

NETNAME	OFF PAR NAME	NC_CRITICAL_NET	NC_IMPEDANCE
IFPA_TX0	IFPA_TX0	1	USDET
IFPA_TX0	IFPA_TX0	1	USDET
IFPA_TX00	IFPA_TX00	1	USDET
IFPA_TX00	IFPA_TX00	1	USDET
IFPA_TX01	IFPA_TX01	1	USDET
IFPA_TX01	IFPA_TX01	1	USDET
IFPA_TX02	IFPA_TX02	1	USDET
IFPA_TX02	IFPA_TX02	1	USDET
IFPA_TX03	IFPA_TX03	1	USDET
IFPA_TX03	IFPA_TX03	1	USDET
IFPB_TX0	IFPB_TX0	1	USDET
IFPB_TX0	IFPB_TX0	1	USDET
IFPB_TX04	IFPB_TX04	1	USDET
IFPB_TX04	IFPB_TX04	1	USDET
IFPB_TX05	IFPB_TX05	1	USDET
IFPB_TX05	IFPB_TX05	1	USDET
IFPB_TX06	IFPB_TX06	1	USDET
IFPB_TX06	IFPB_TX06	1	USDET
IFPB_TX07	IFPB_TX07	1	USDET
IFPB_TX07	IFPB_TX07	1	USDET

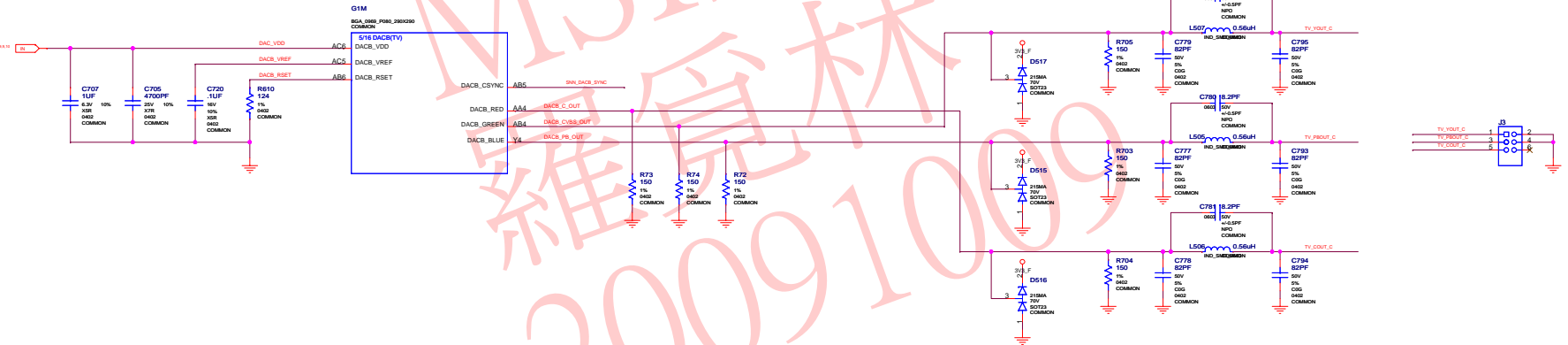
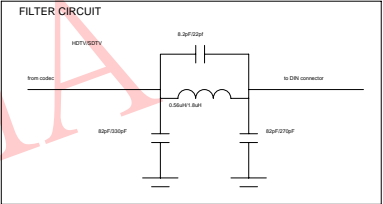
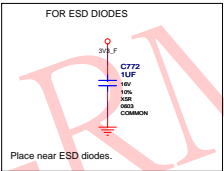


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMD5 LINK A/B, DVI CONNECTOR SOUTH

DACB: SD/HD VIDEO OUT CONNECTOR

NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
DACB_C_OUT	750UM	1	
DACB_VREF	750UM	1	
DACB_RESET	750UM	1	
TV_PROUT_C	750UM	1	
TV_PROUT_E	750UM	1	
TV_PROUT_S	750UM	1	
DACB_VREF	100UM	1	
DACB_RESET	100UM	1	



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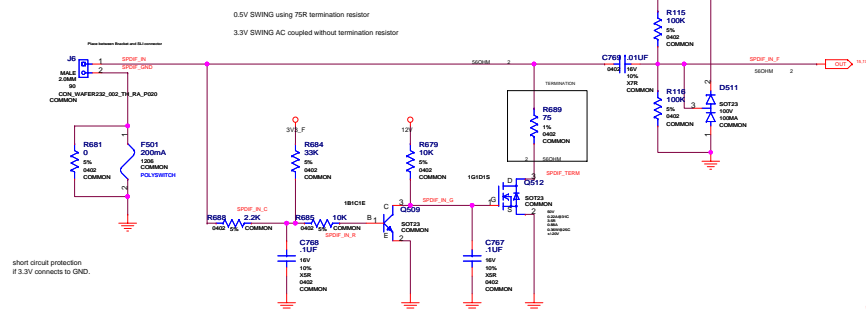
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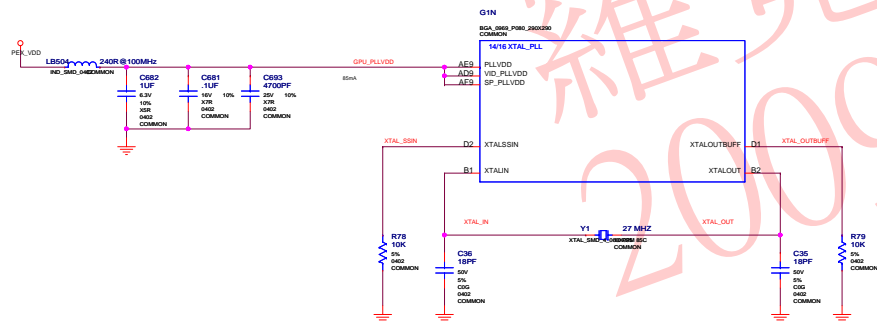
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XTAL/PLLVD/SPDIF IN

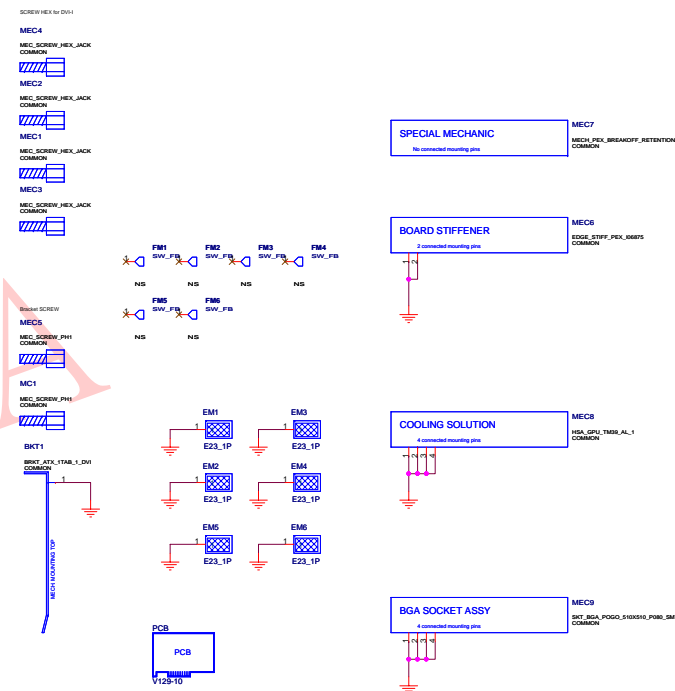
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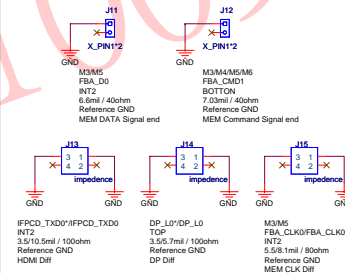
XTAL/GPU_PLLVDD



MECHANICALS & THERMALS



Impedance control line

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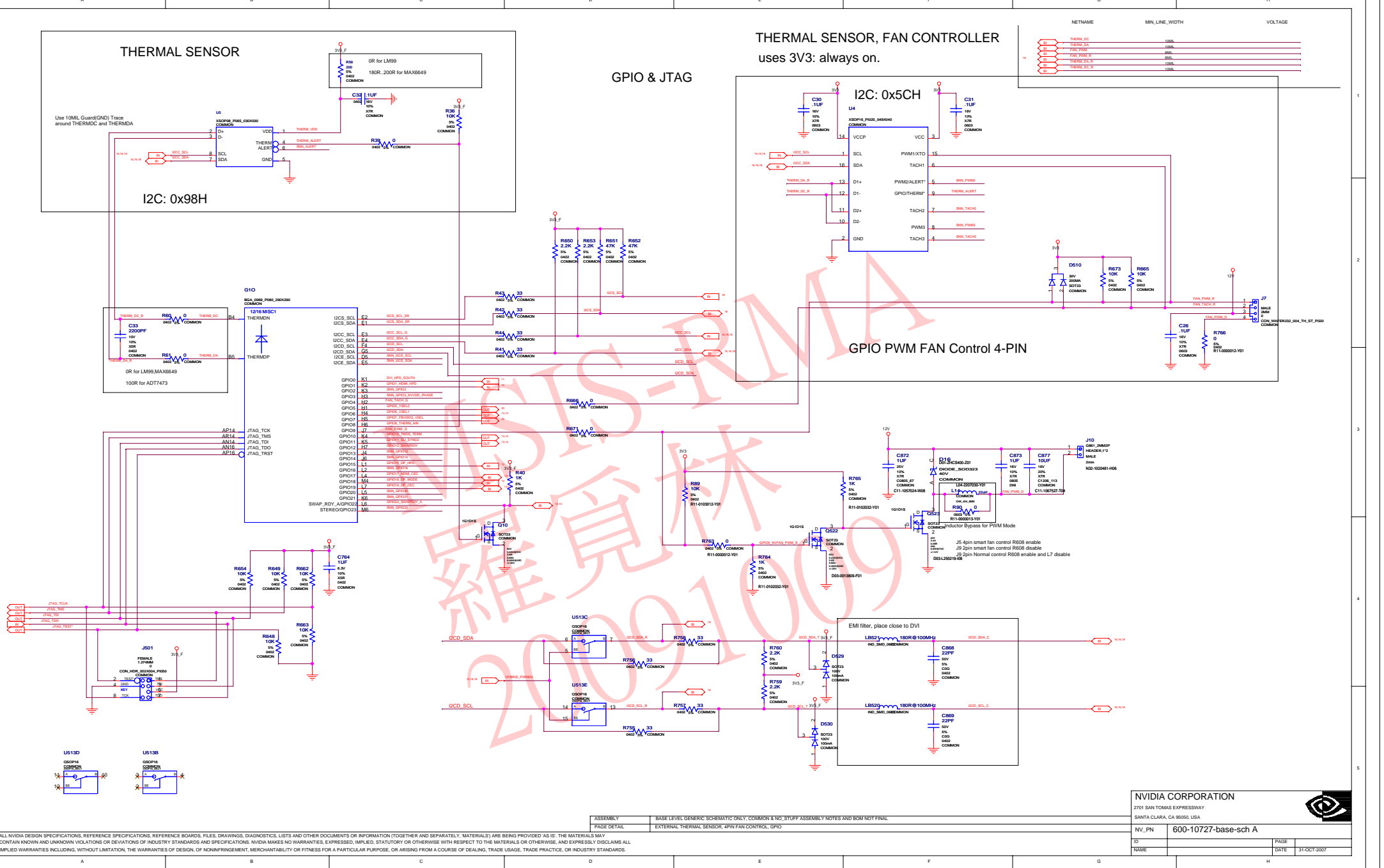
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPOD-IN, XTAL, MECHANICALS, THERMALS



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	EXTERNAL THERMAL SENSOR, 4PIN FAN CONTROL, GPIO

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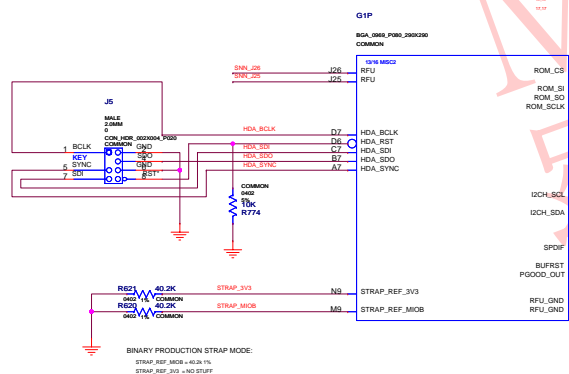
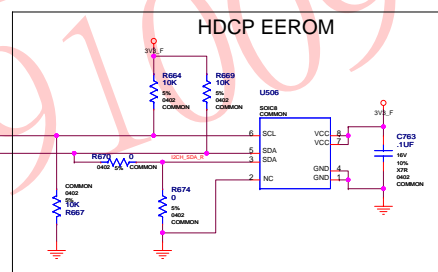
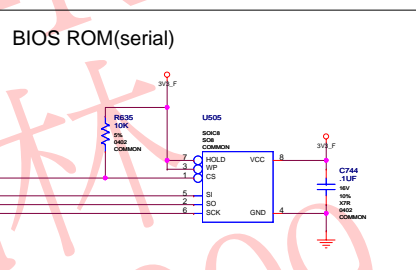
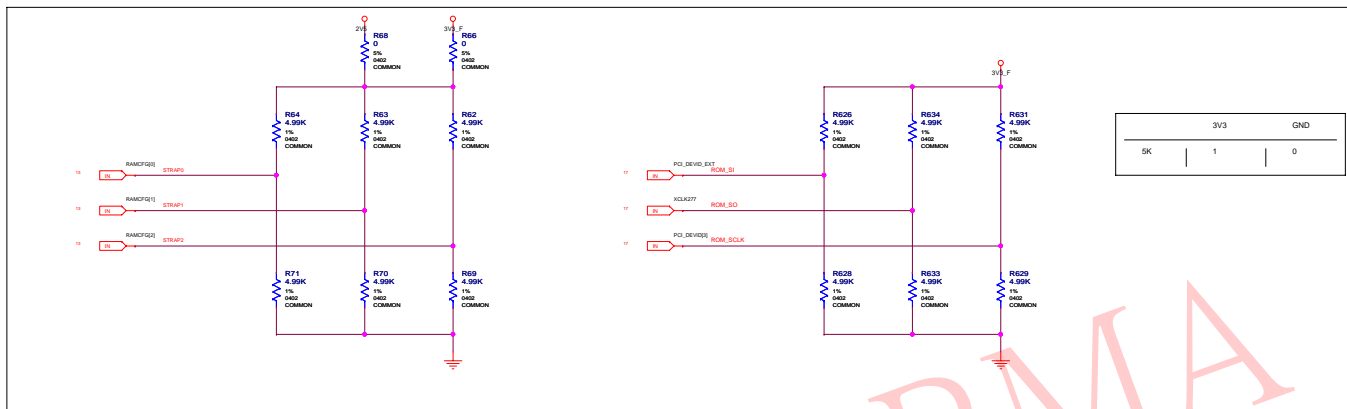


NV_PN	600-10727-base-sch A
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STRAPPING OPTIONS

Assembly: BIOS



	NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
OUT	HDA_BCLK		50Ω(1M)	2
OUT	HDA_FSI1		50Ω(1M)	2
OUT	HDA_SCK		50Ω(1M)	2
OUT	HDA_SDIO		50Ω(1M)	2
OUT	HDA_SSPIC		50Ω(1M)	2

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

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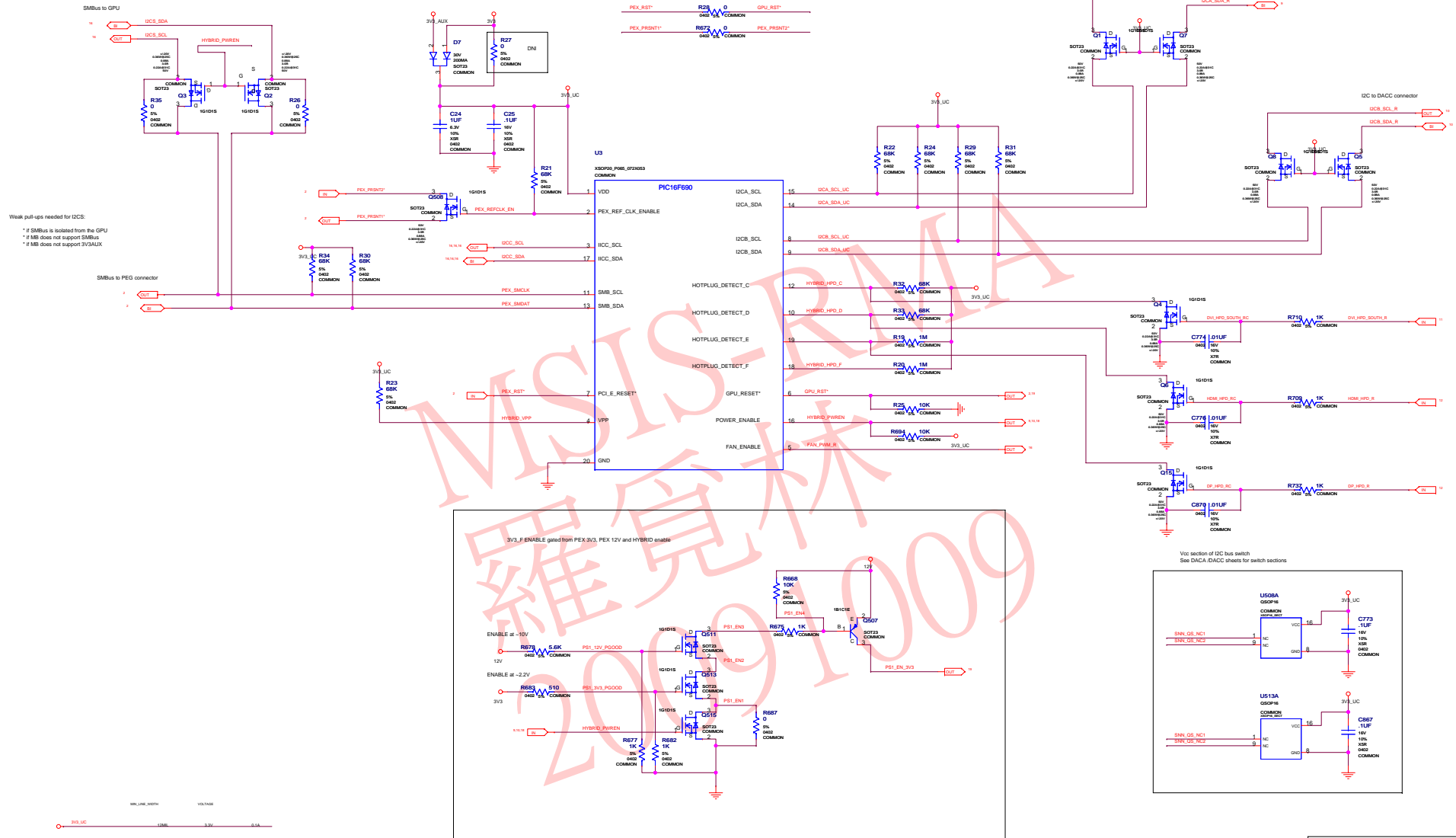
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NAME		DATE	31-OCT-2007

HYBRID POWER

Per Datasheet:

Vf = 400mV at 10mA
* expected current < 2mA

Stuff only to bypass the micro-controller



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	HYBRID POWER CIRCUIT

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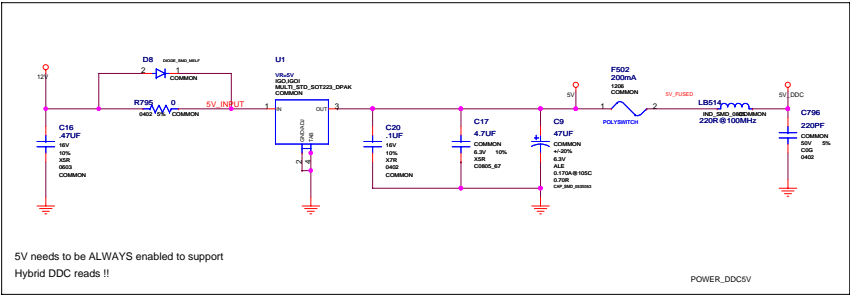
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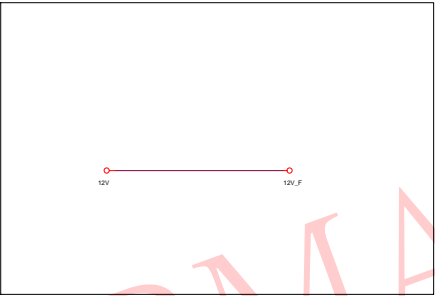
Power Supply: 5V, 5V_DDC, TMDS, MIOA_VDDQ

5V REGULATOR

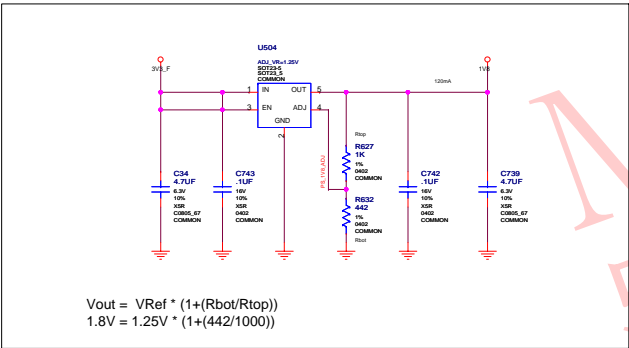


5V DDC

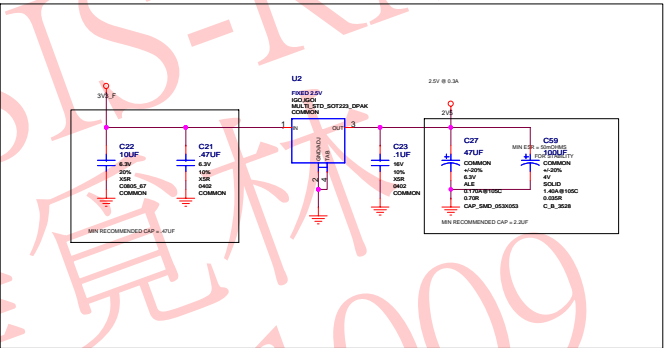
12V filter



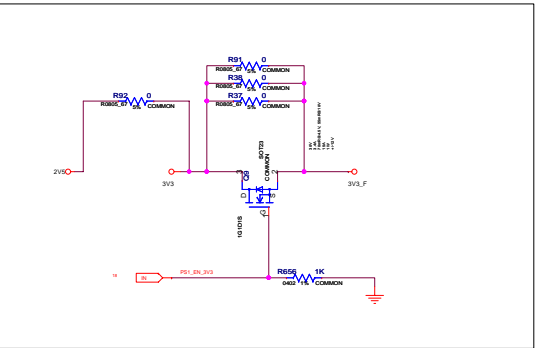
IFP PLL Supply 1.8V



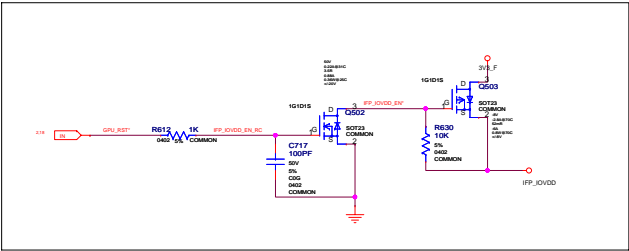
MIO_VDD 2.5V



3V3 switch



IFP_IOVDD BACKDRIVE PREVENTION



NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	0.1A	120M	5V
5V_DDC	0.1A	120M	5V
5V	0.15A	120M	5V
PL1_V16_AD3	0.05A	120M	1.8V
V16	0.15A	120M	1.8V
V15	0.3A	120M	2.5V
DND		100M	3V
V15_F	3.5A	100M	3.5V
V15_F	5A	200M	12V

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 3100FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY LINEARS: 5V, DDC5V, IFPPLLVD, IFP10VDD, MIO VDD, 3V3 FILTER, 12V FILTER

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FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3

1

2

3

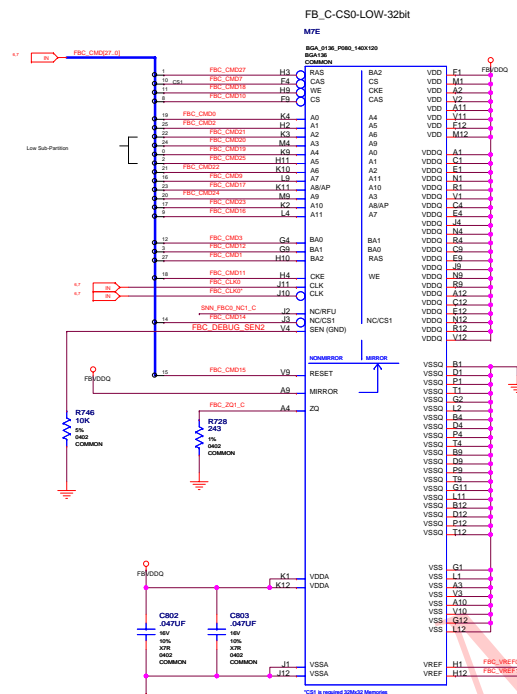
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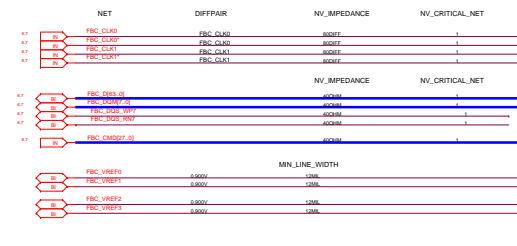
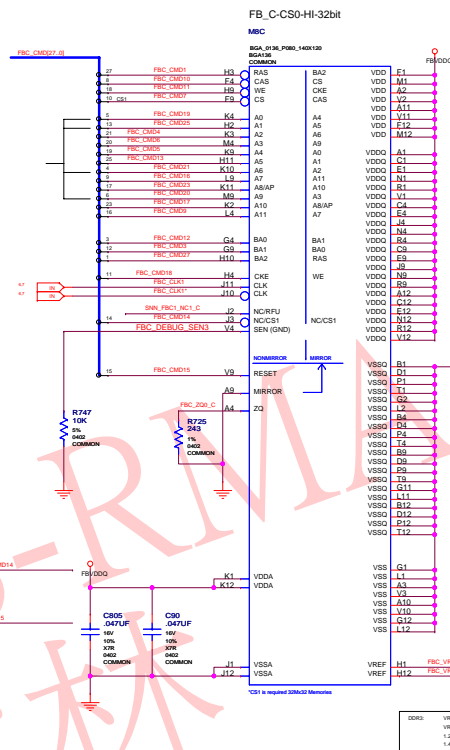
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136BGA CMD Mapping	
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QMC505	BA504*
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QMC507	BA506*
QMC508	BA507*
QMC509	BA508*
QMC510	BA509*
QMC511	BA510*
QMC512	BA511*
QMC513	BA512*
QMC514	BA513*
QMC515	BA514*
QMC516	BA515*
QMC517	BA516*
QMC518	BA517*
QMC519	BA518*
QMC520	BA519*
QMC521	BA520*
QMC522	BA521*
QMC523	BA522*
QMC524	BA523*
QMC525	BA524*
QMC526	BA525*
QMC527	BA526*
QMC528	BA527*
QMC529	BA528*
QMC530	BA529*
QMC531	BA530*
QMC532	BA531*
QMC533	BA532*
QMC534	BA533*
QMC535	BA534*
QMC536	BA535*
QMC537	BA536*
QMC538	BA537*
QMC539	BA538*
QMC540	BA539*
QMC541	BA540*
QMC542	BA541*
QMC543	BA542*
QMC544	BA543*
QMC545	BA544*
QMC546	BA545*

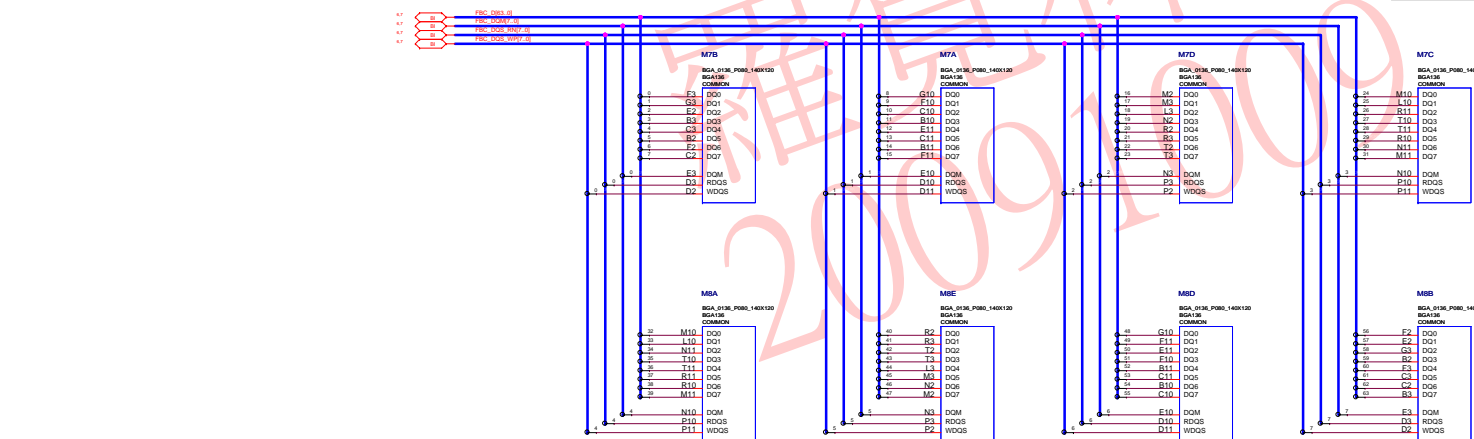
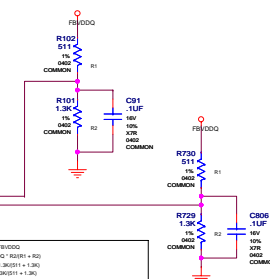
FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3




FBC Partition			CSD
CMD	ADDR		
CMD1	R4D*		
CMD2	CAC*		
CMD11	WE*		
CMD18	CSE		
CMD15	RESET/IO0*		
CMD6	CSD		
CMD19	Ar0a		
CMD25	Ar1a		
CMD3	Ar0a	Line Sub-Partition	
CMD4	Ar0a		
CMD0	Ar0a		
CMD2	Ar0a	HS Sub-Partition	
CMD4	Ar0a		
CMD6	Ar0a		
CMD5	Ar0a		
CMD13	Ar0a		
CMD21	Ar0a		
CMD16	Ar1a*		
CMD3	Ar0a		
CMD0	Ar0a		
CMD17	Ar1S		
CMD5	Ar1a*		
CMD14	Ar12a		
CMD12	BA0		
CMD3	BA1		
CMD27	BA2		



Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!

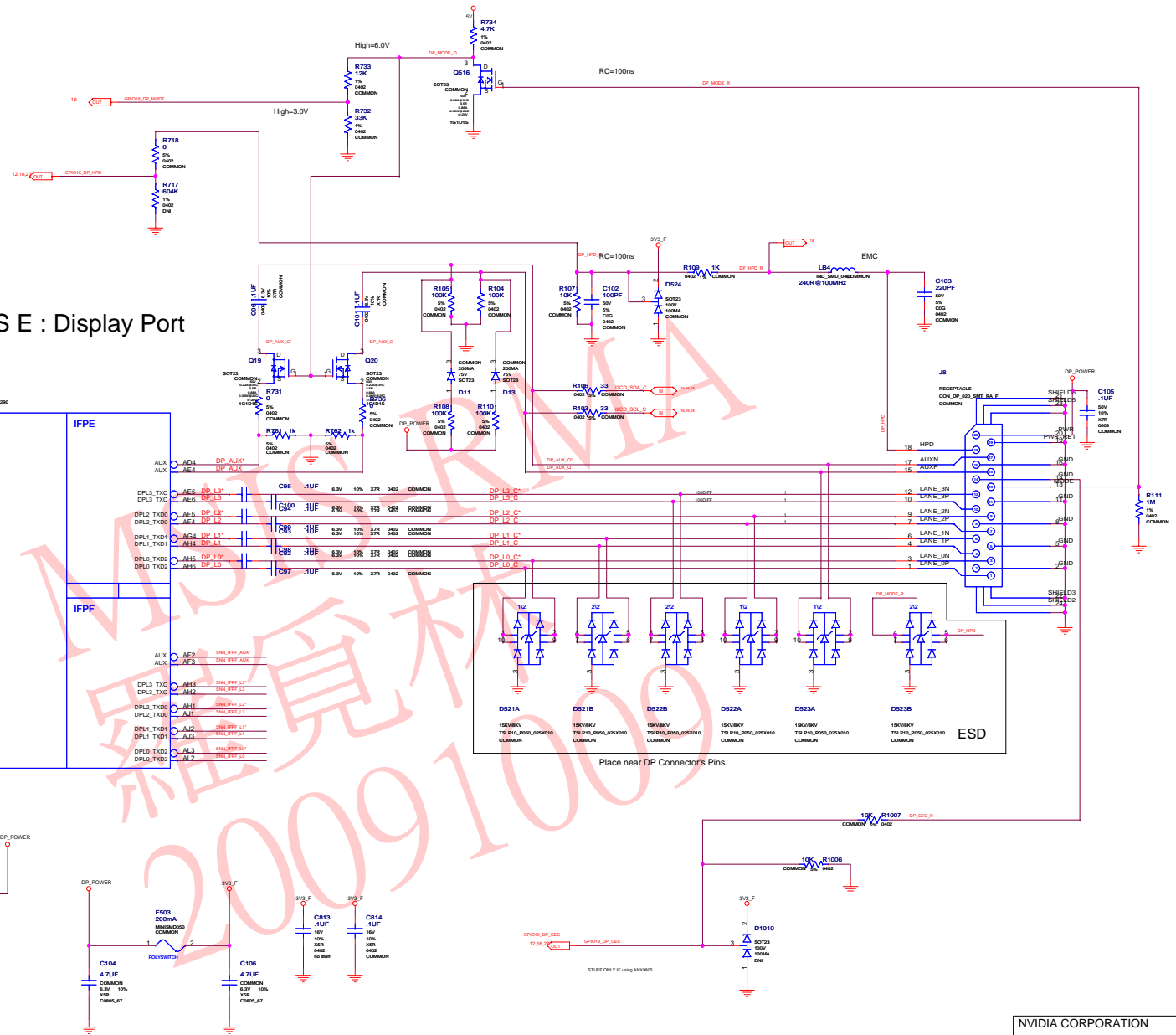


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TMDS LINK: E & F

TMDS E : Display Port



$$V_o = V_{REF} * (1 + (R_{top} / R_{bot})) + I_{adj} * R_{bot}$$

$$3.28V = 1.25V * (1 + (1.58K / 1.00K)) + 55\mu * 1.00K$$

$$3.33V = 1.25V * (1 + (1.62K / 1.00K)) + 55\mu * 1.00K$$

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK C/D, AC COUPLING, PD's, DVI CONNECTOR MID

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