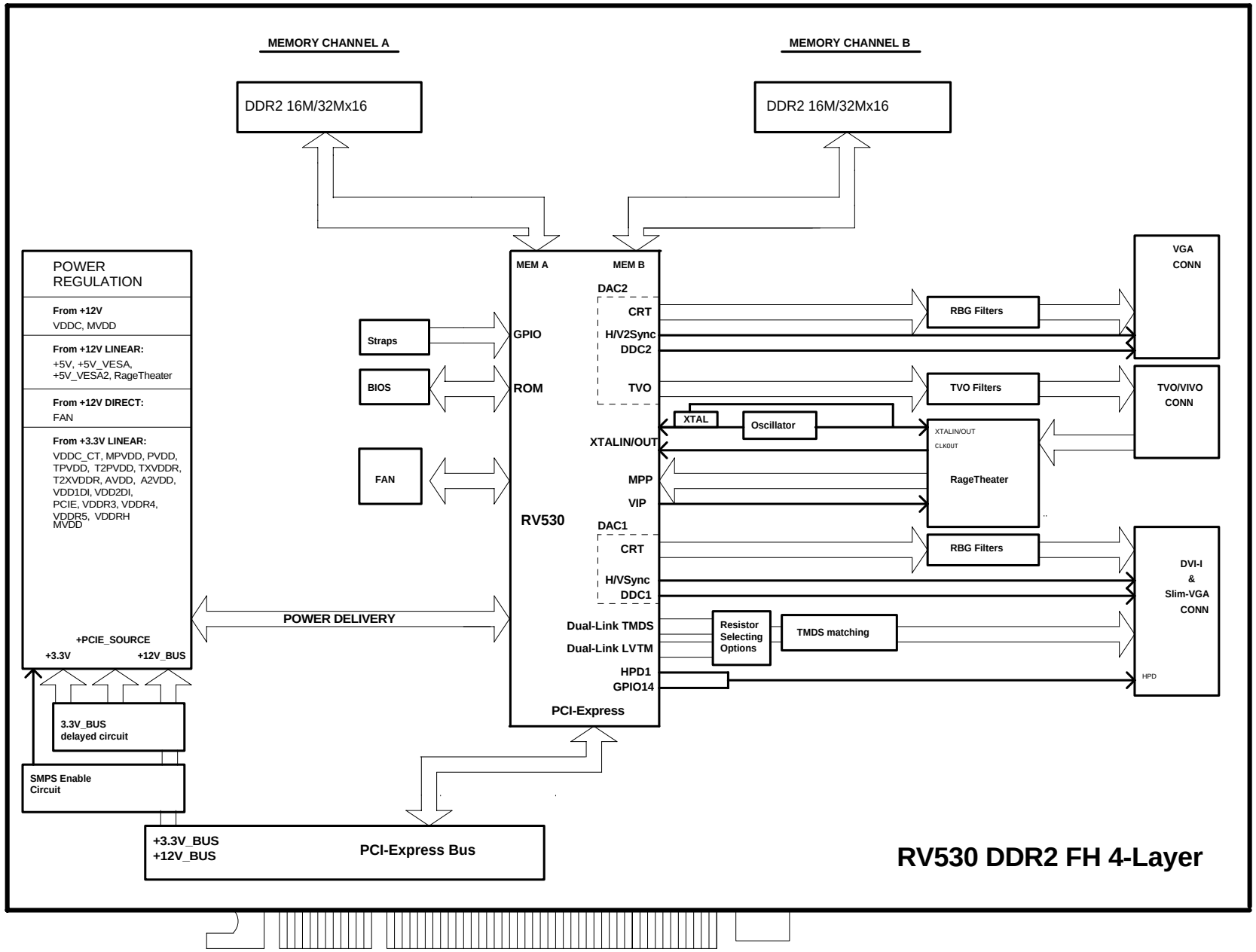

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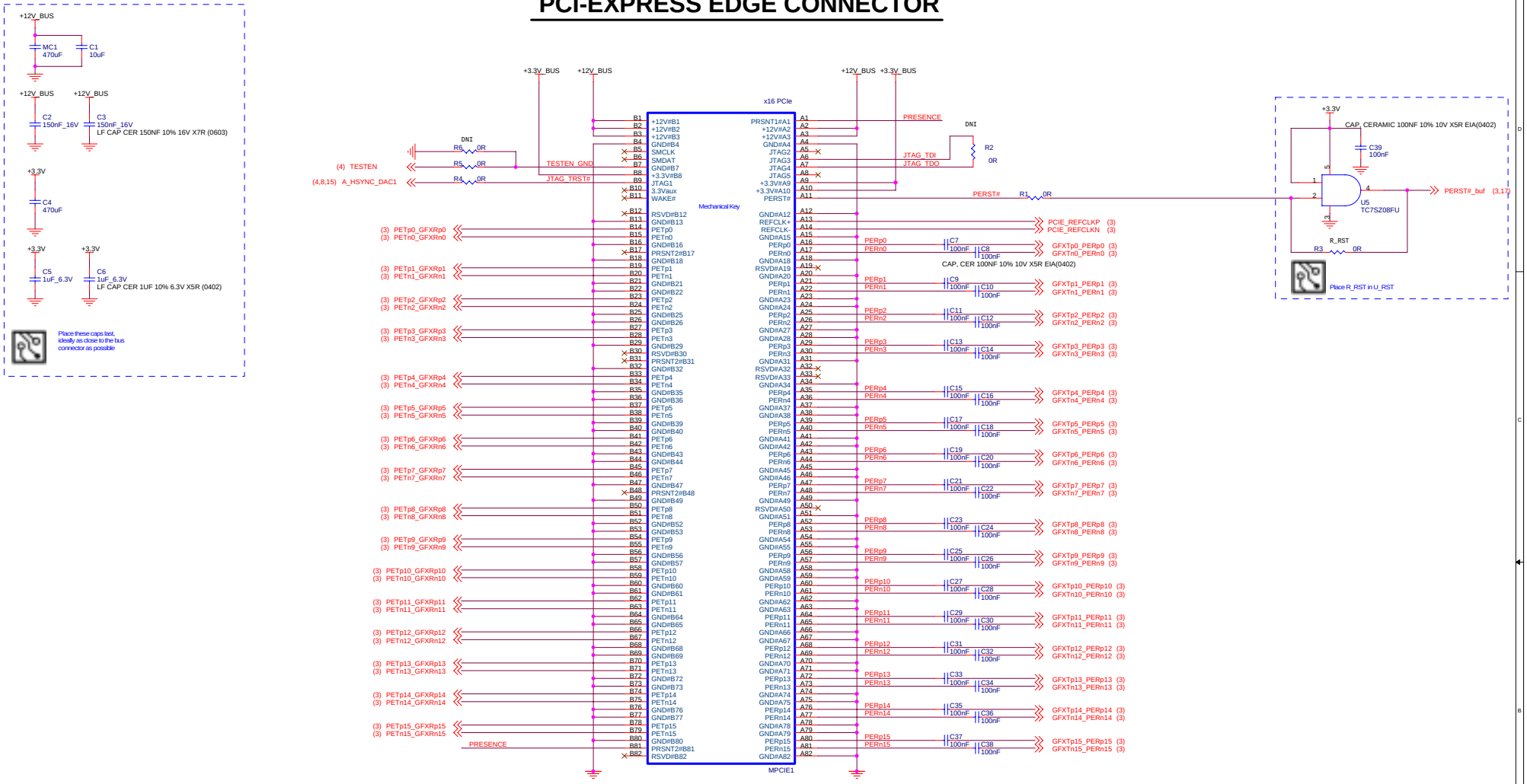
PCI-EXPRESS EDGE CONNECTOR



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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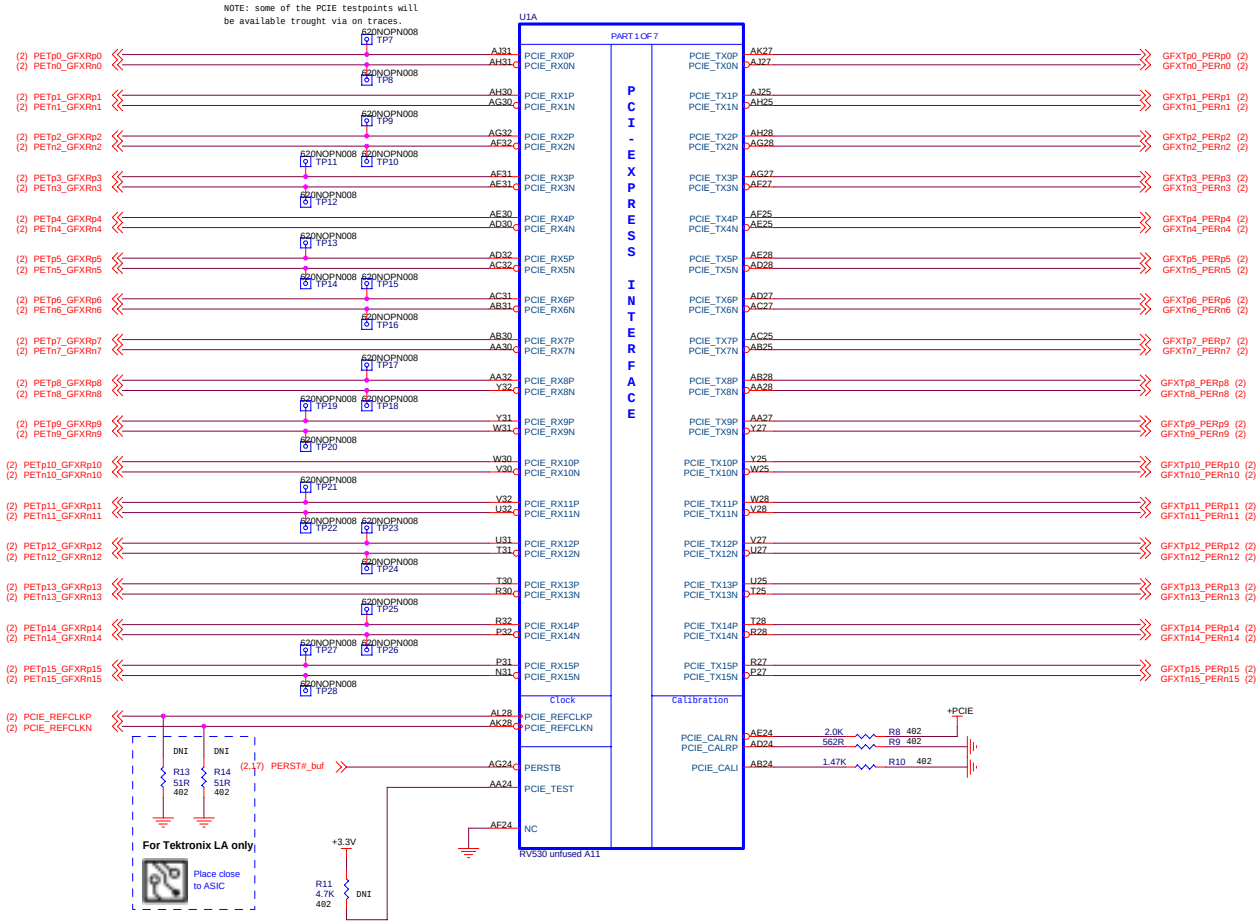

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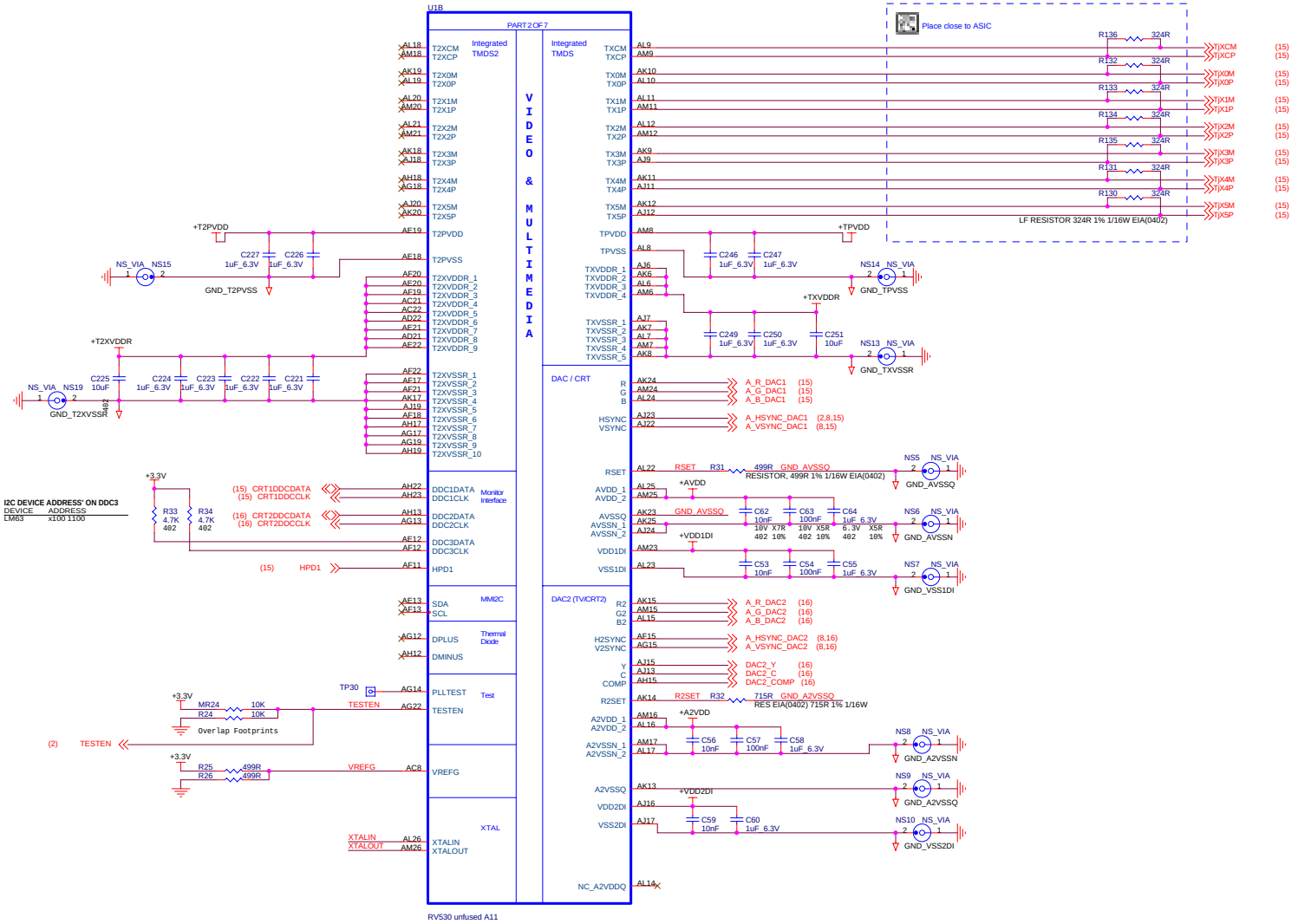

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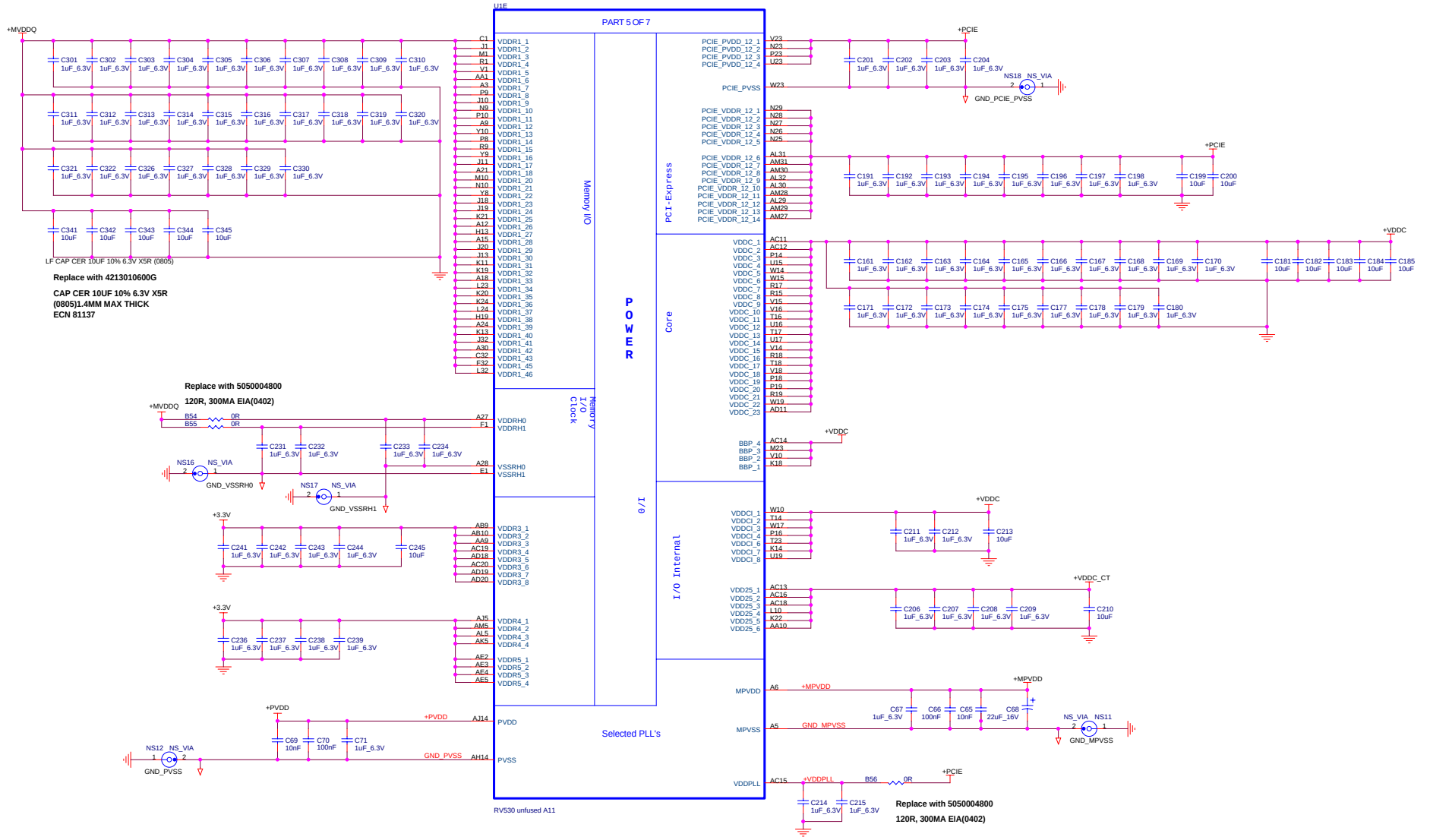

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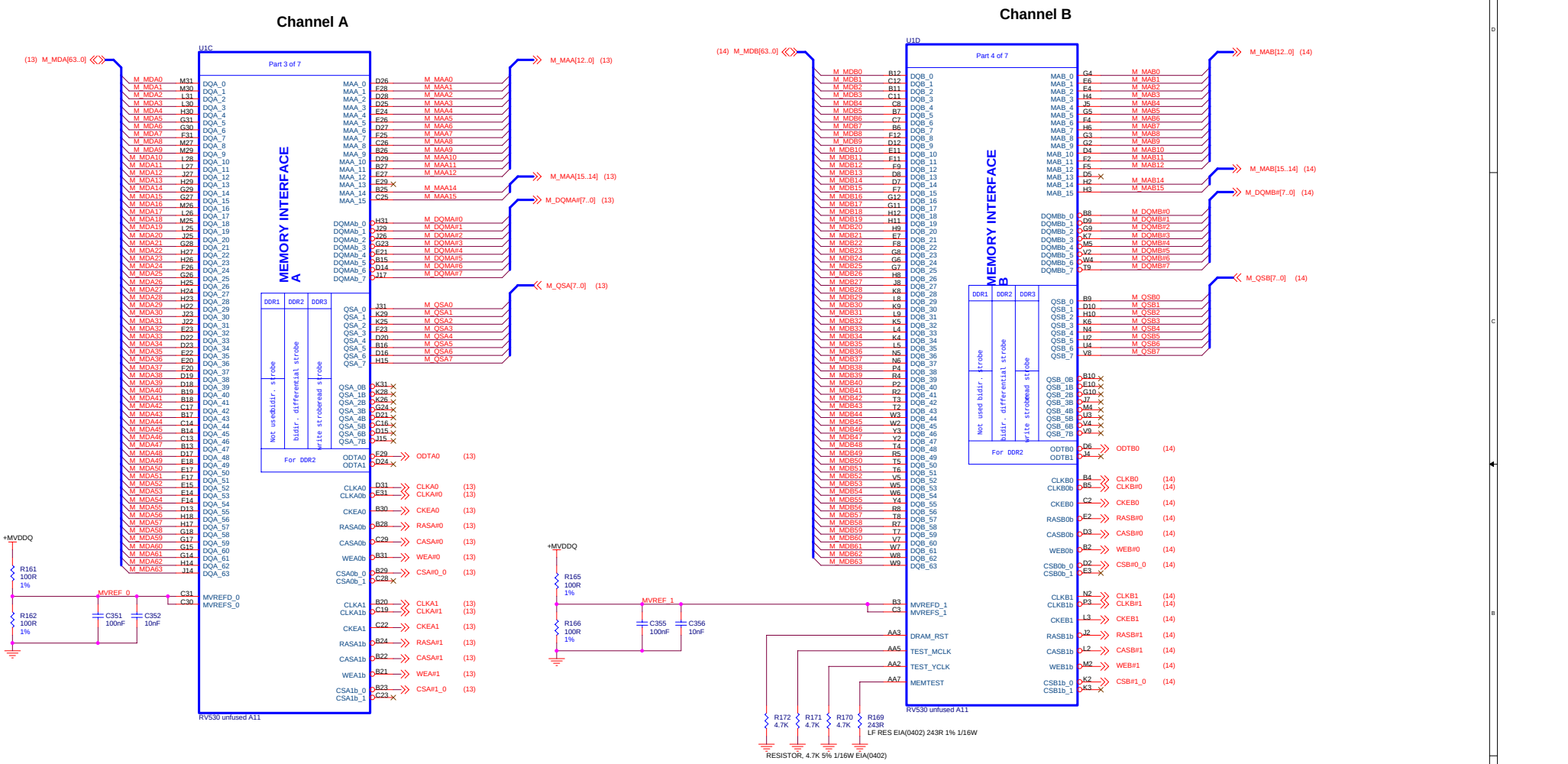
RV530 MEMORY CHANNELS A and B



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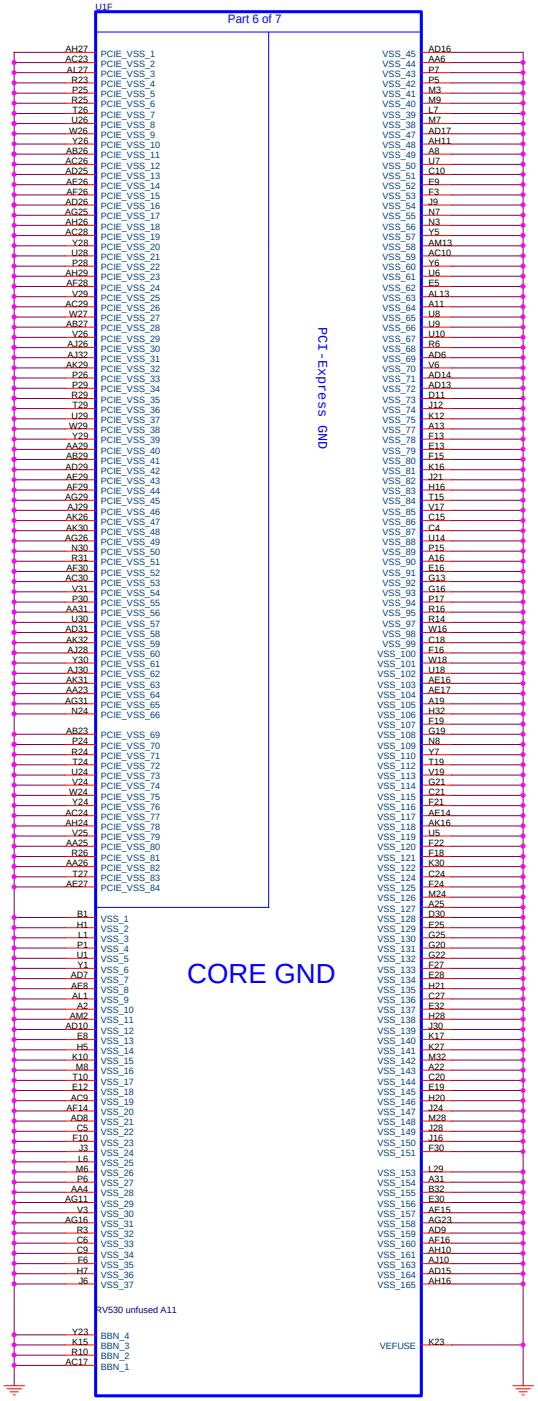

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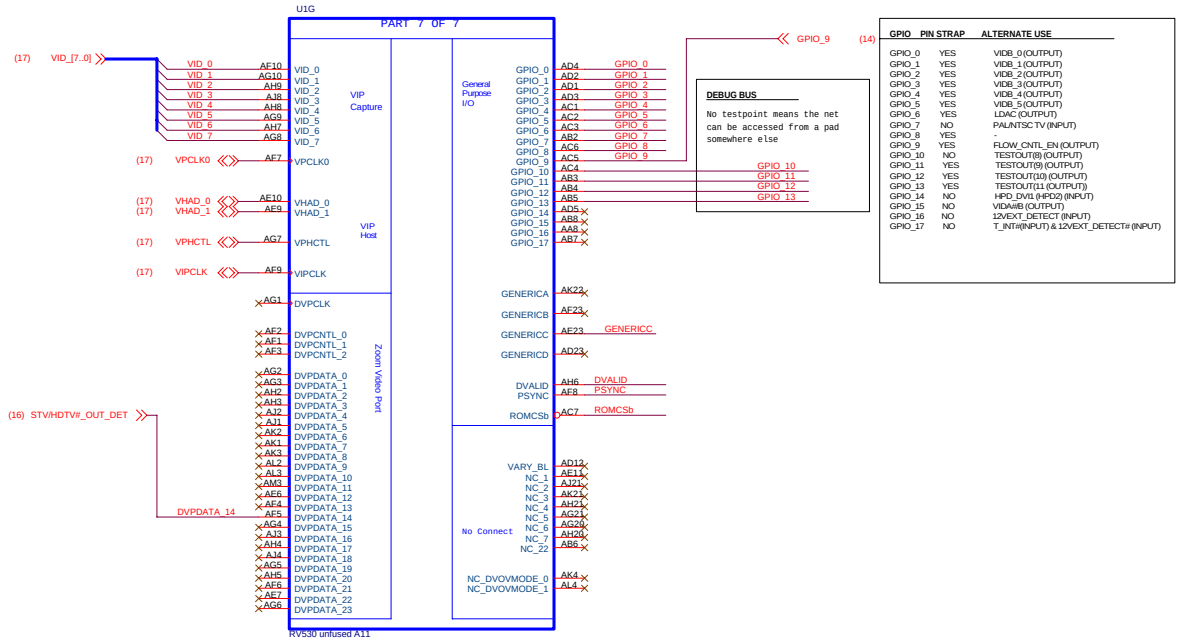
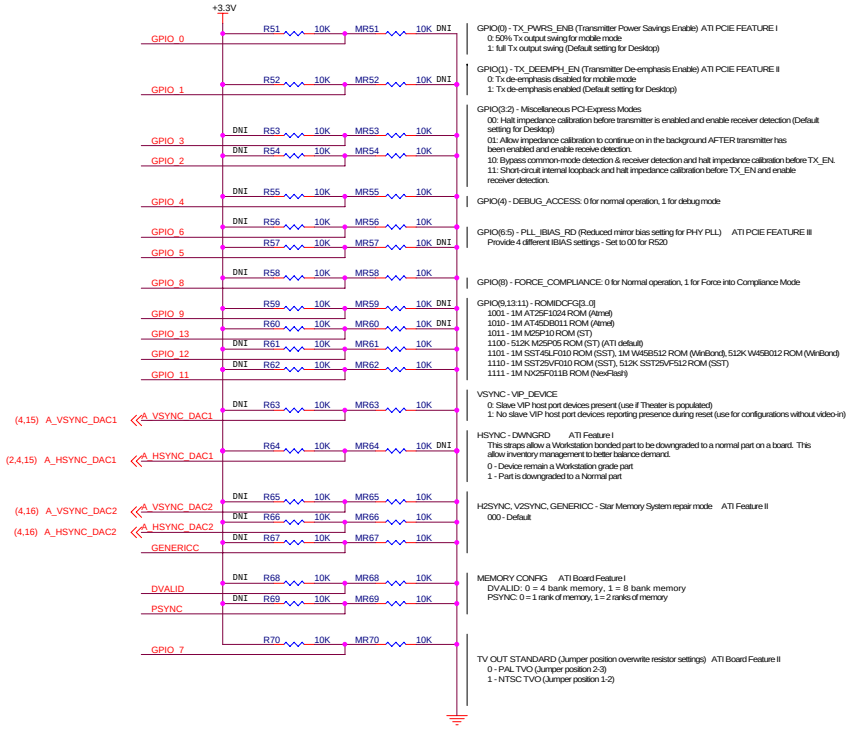
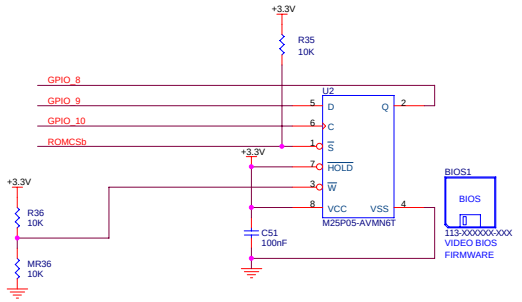


PIN BASED STRAPS





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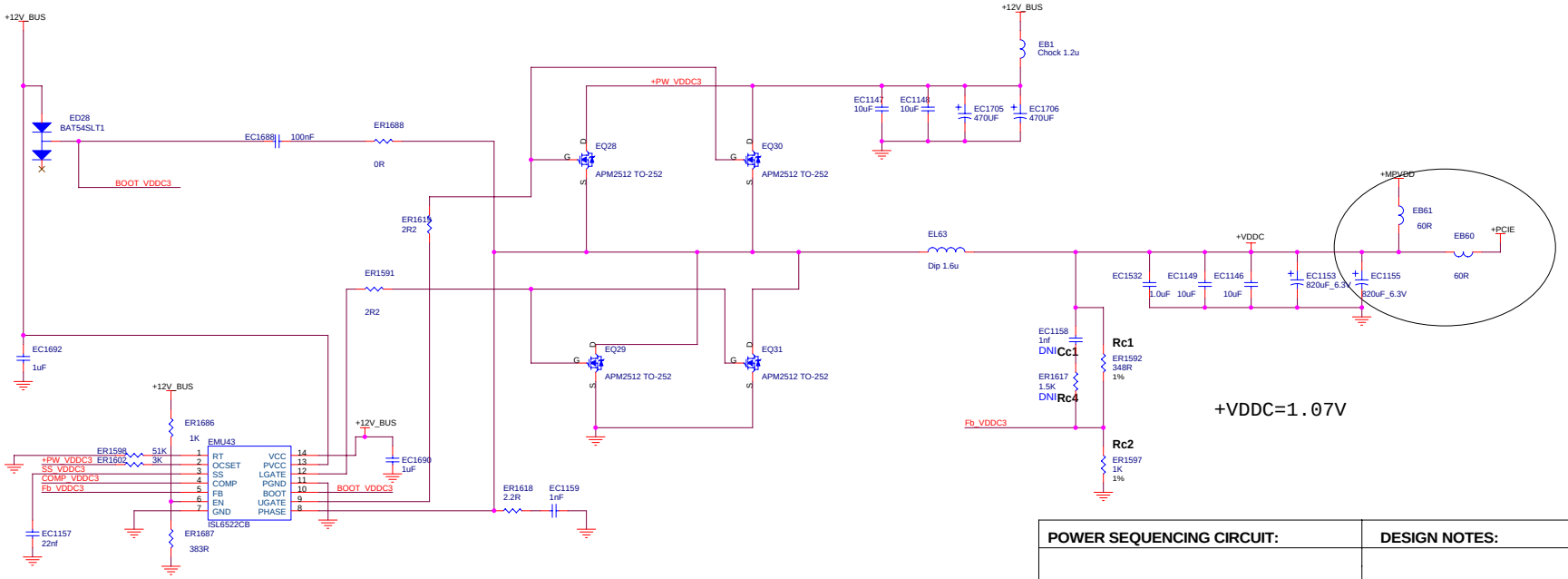
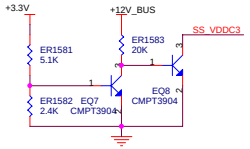
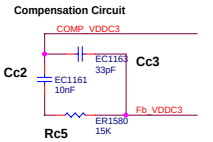
CORE REGULATOR VDDC



Lower MOSFET should be surrounded by a lot of copper for heat dissipation

POWER SEQUENCING CIRCUIT:	DESIGN NOTES:
	
FOR ALTERNATE #1 Remove R374, R375, R371, C168 and U32 Install R370, R112, R954, R305-R308, C166, C159 and MU32	**FOR ALTERNATE #2** Change C157 for 10 uF and C121 for 1 uF Replace C764 by 0 Ohm resistor Replace R314 with a bead Remove R954, R370, R305-R308, C159, R112, C160 and MU32 Install R374, R375, R371, C168 and U32 **Compensation circuit** Rc1 = 10K, Rc2 = 8.06K R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF

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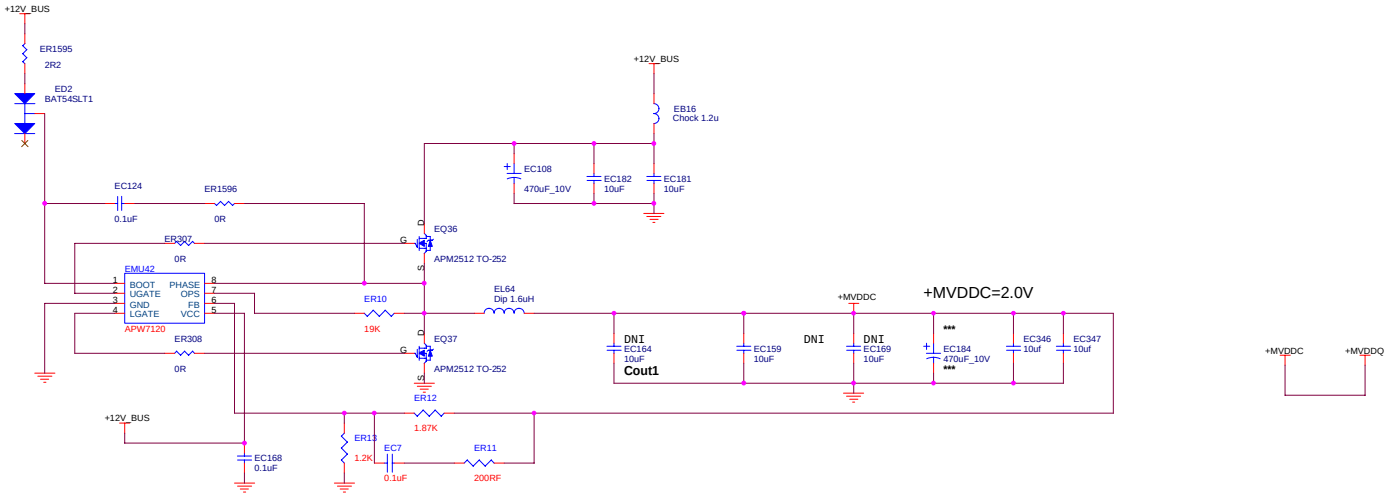

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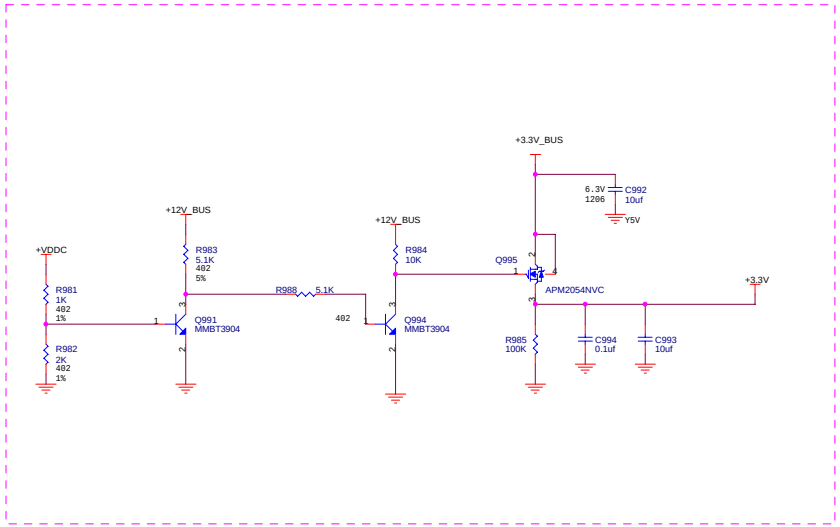

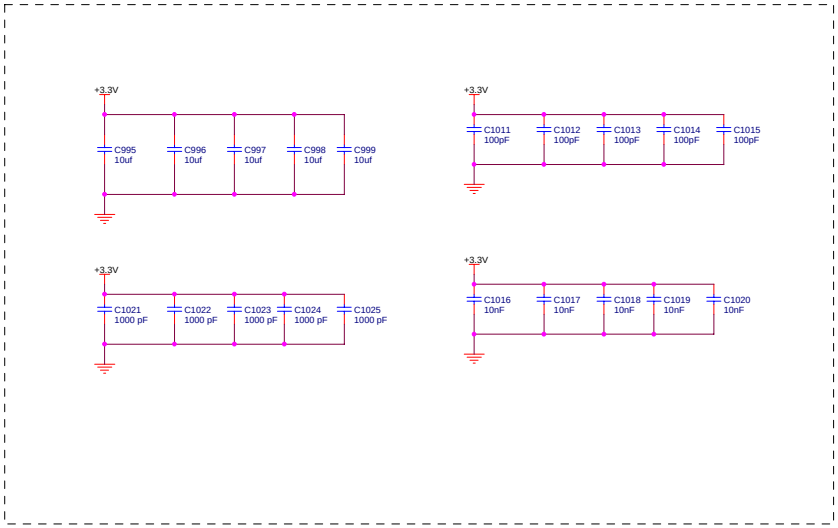

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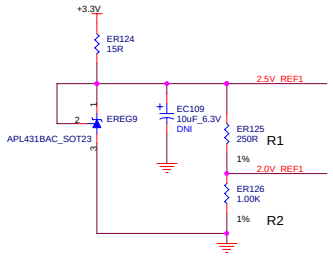

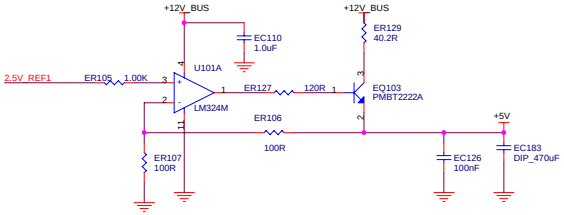

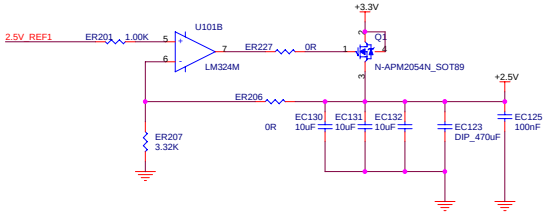

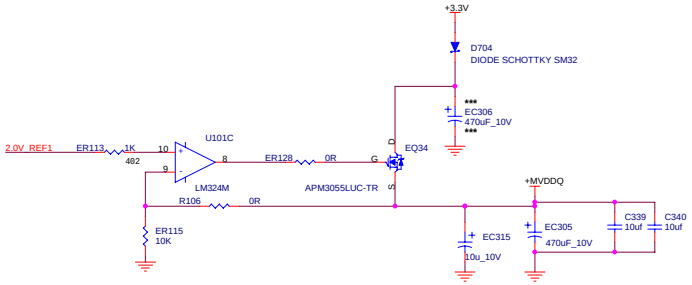

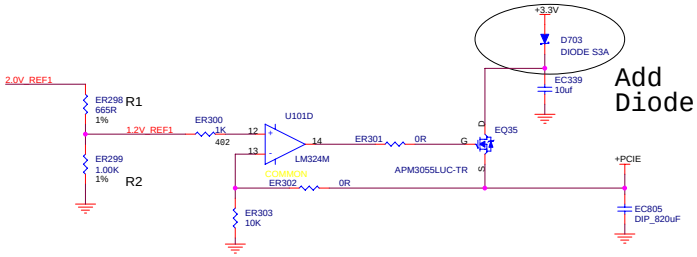

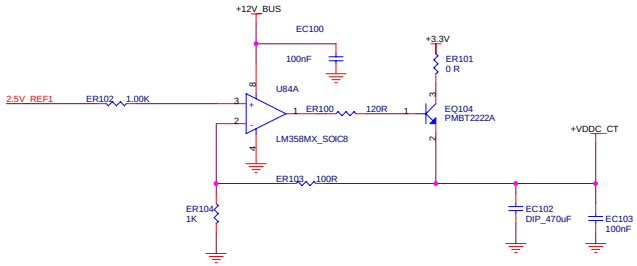

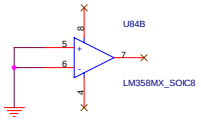

Replace with 5050004800
120R, 300MA EIA(0402)

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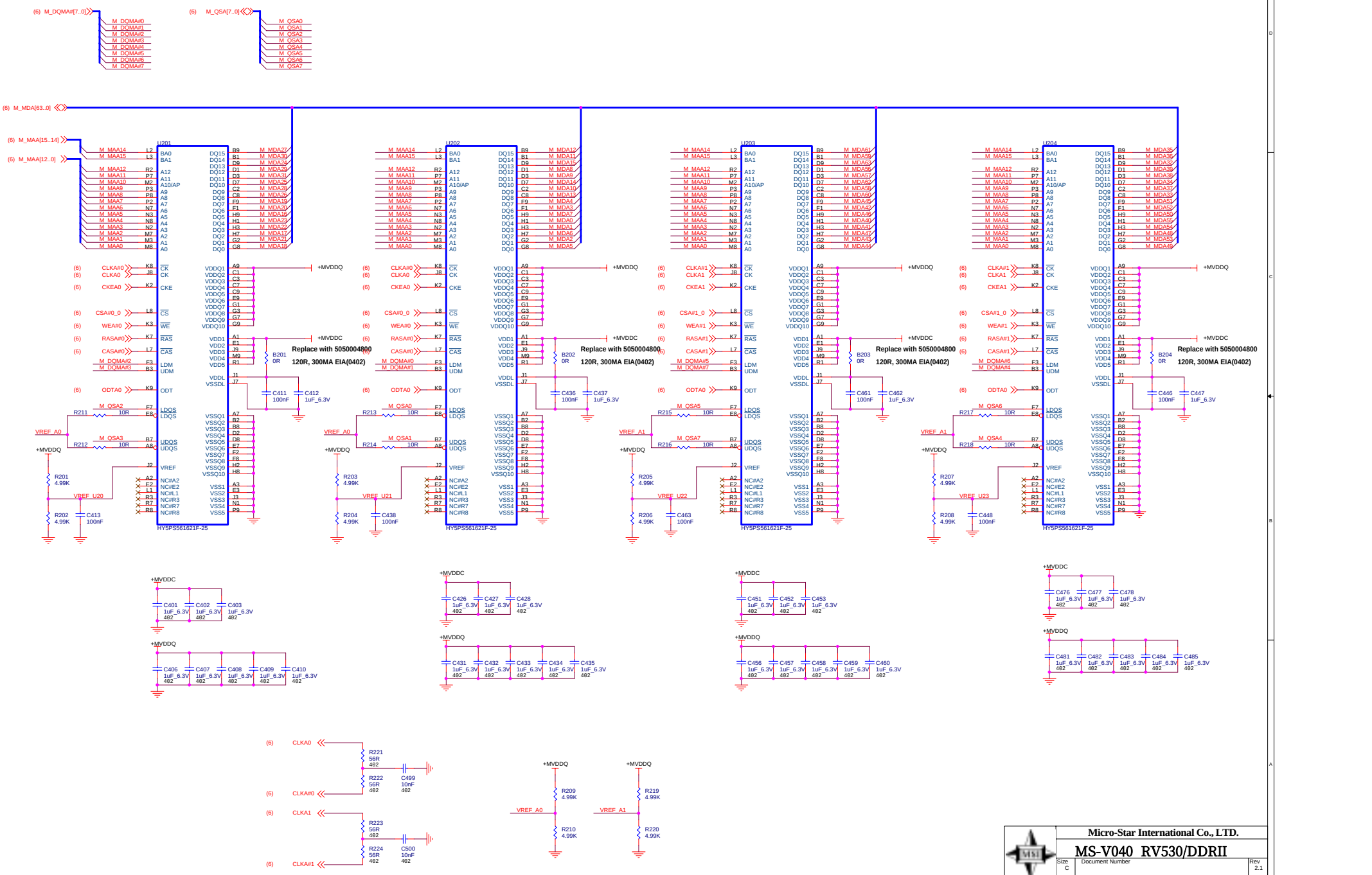
CHANNEL A: RANK 0 128MB DDR2



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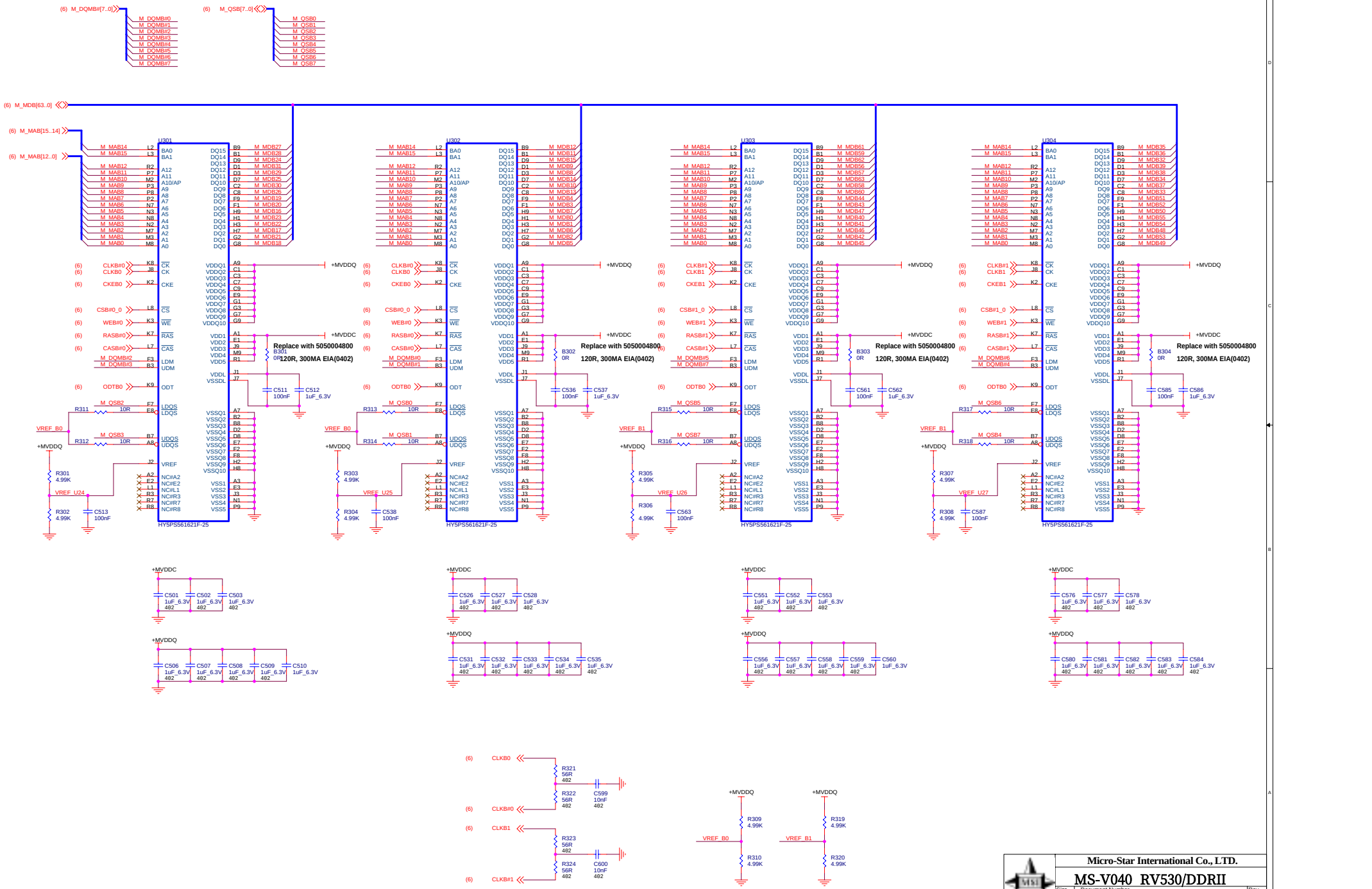
CHANNEL B: RANK 0 128MB DDR2



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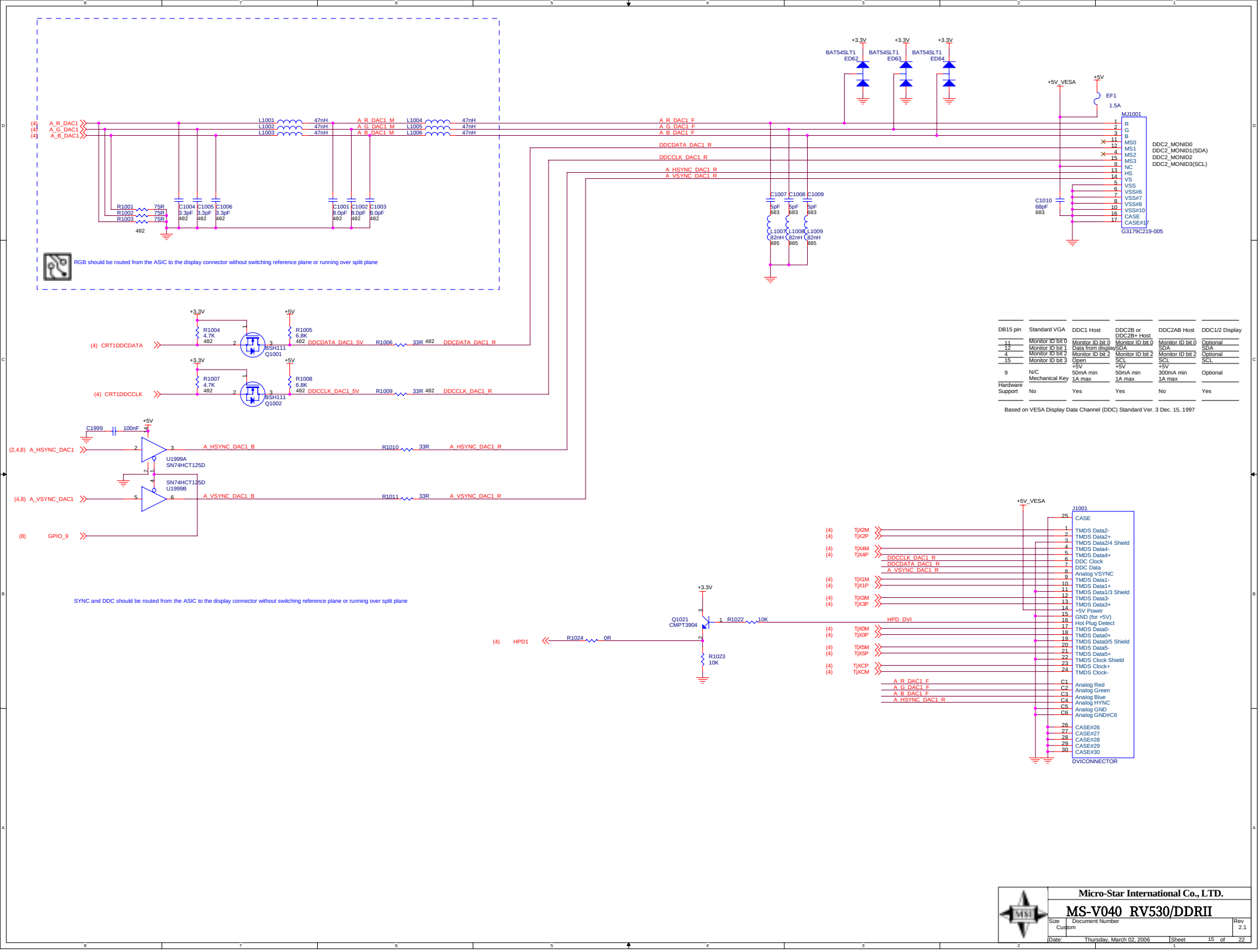

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C Mechanical Key	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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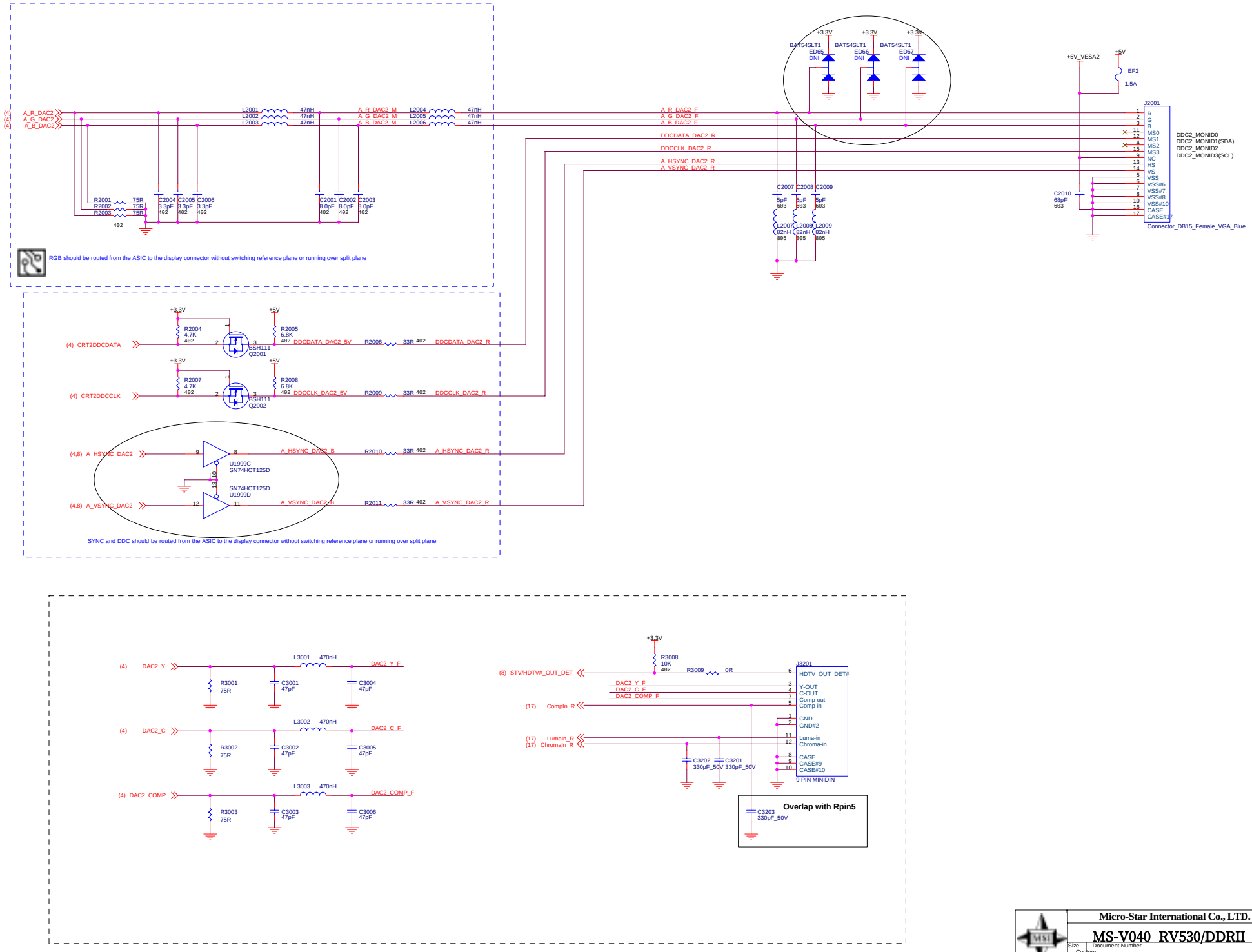

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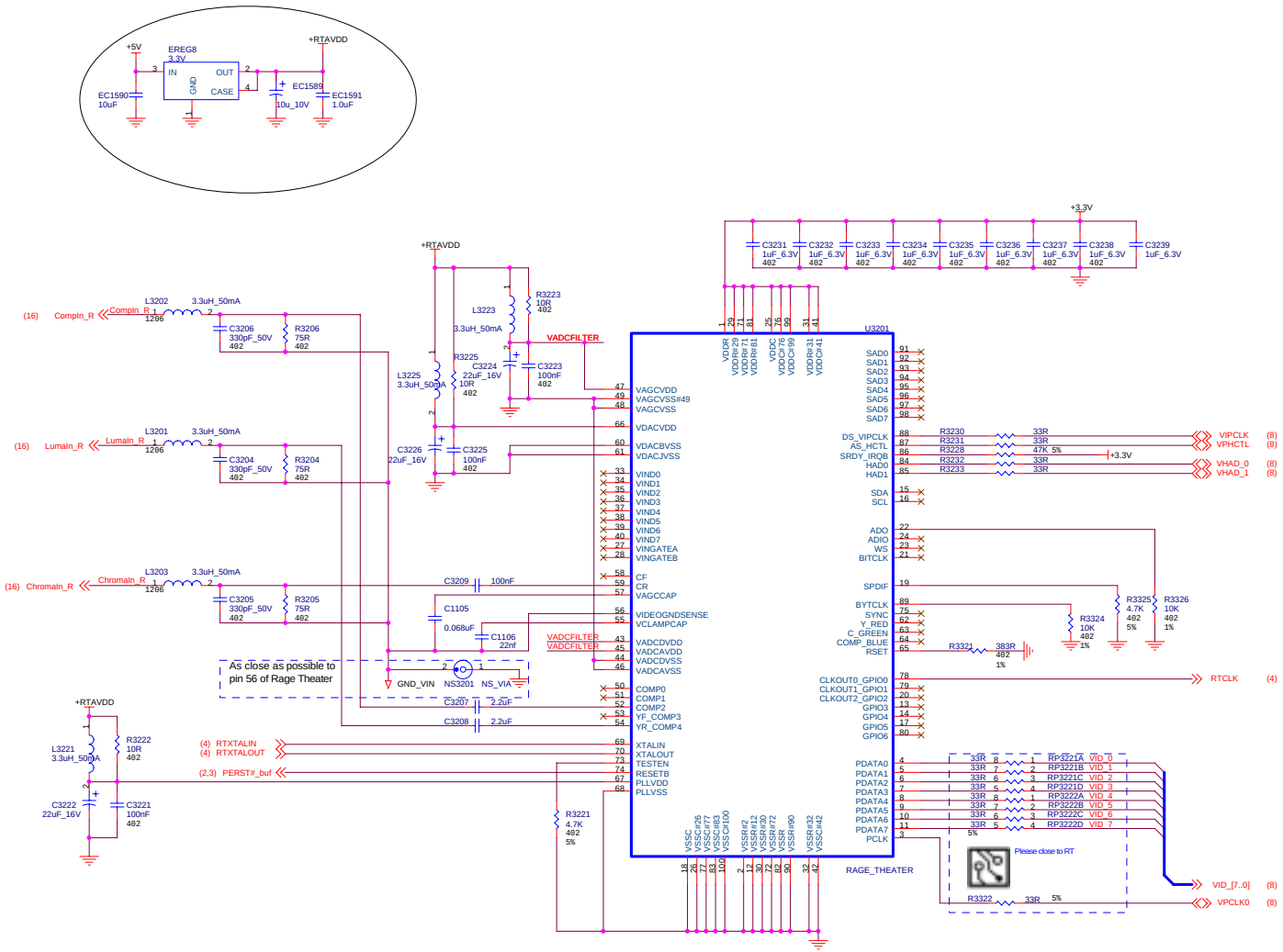

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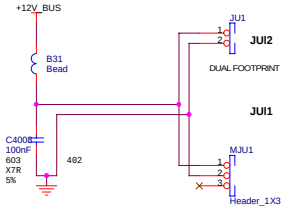

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DVI/VGA SCREWS

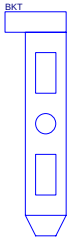
SCREW1
SCREW
JACKSCREW ASSY
7020000800

SCREW2
SCREW
JACKSCREW ASSY
7020000800

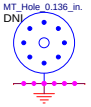
SCREW3
SCREW
JACKSCREW ASSY
7020000800

SCREW4
SCREW
JACKSCREW ASSY
7020000800

BKT



MT1
MT_Hole_0.136_in.
DNI



FM1 SW_FB
FM5 SW_FB
FM2 SW_FB
FM6 SW_FB
FM3 SW_FB
FM4 SW_FB

PCB

H2

LOW PROFILE HS

+MVDDQ
J1
X_PIN1*2
J3
X_PIN1*2
J2
X_PIN1*2
J4
X_PIN1*2

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