

384b GDDR6 x16  
TALL DP + DP + DP + HDMI/DP + USB

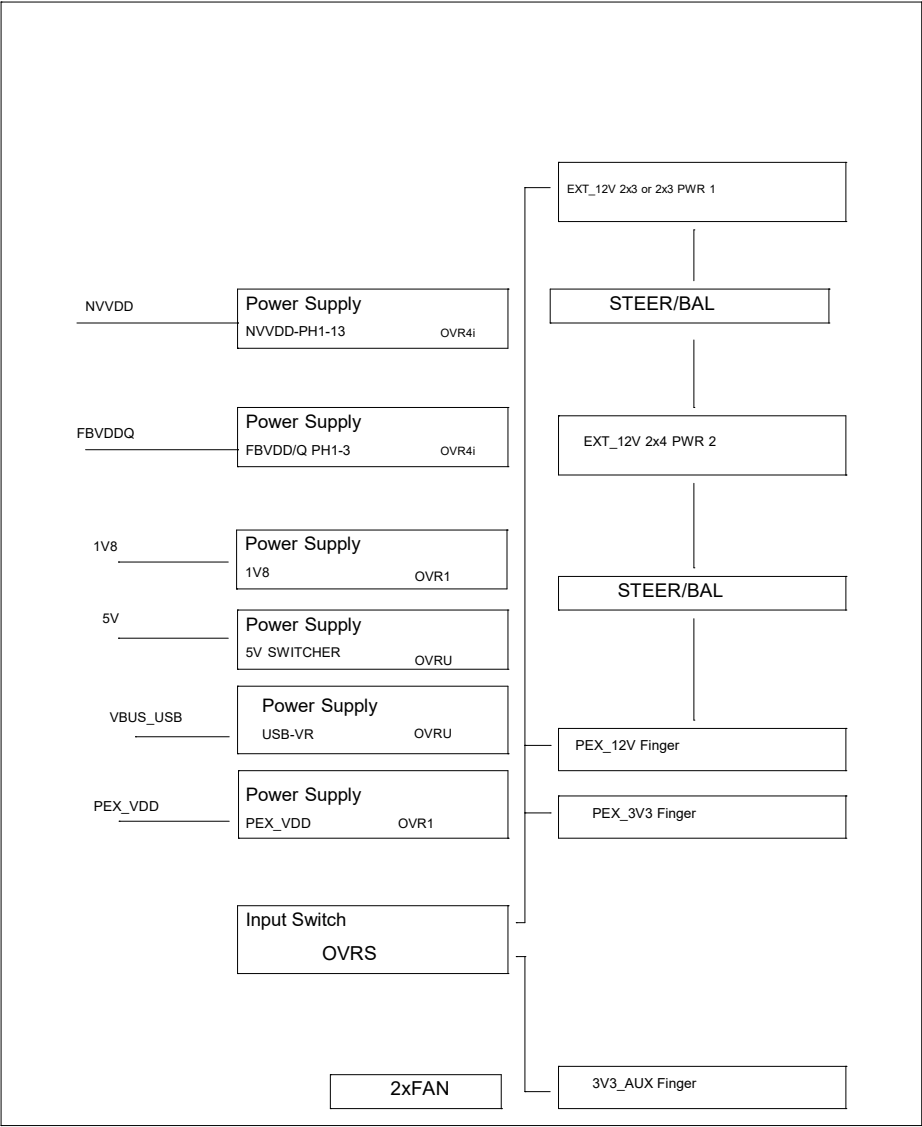
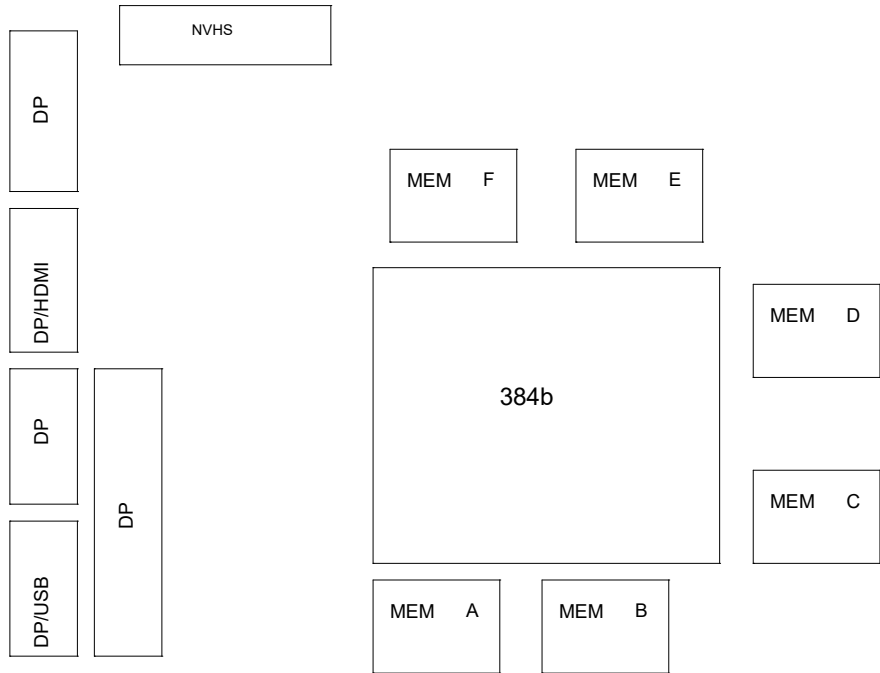
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Block Diagram

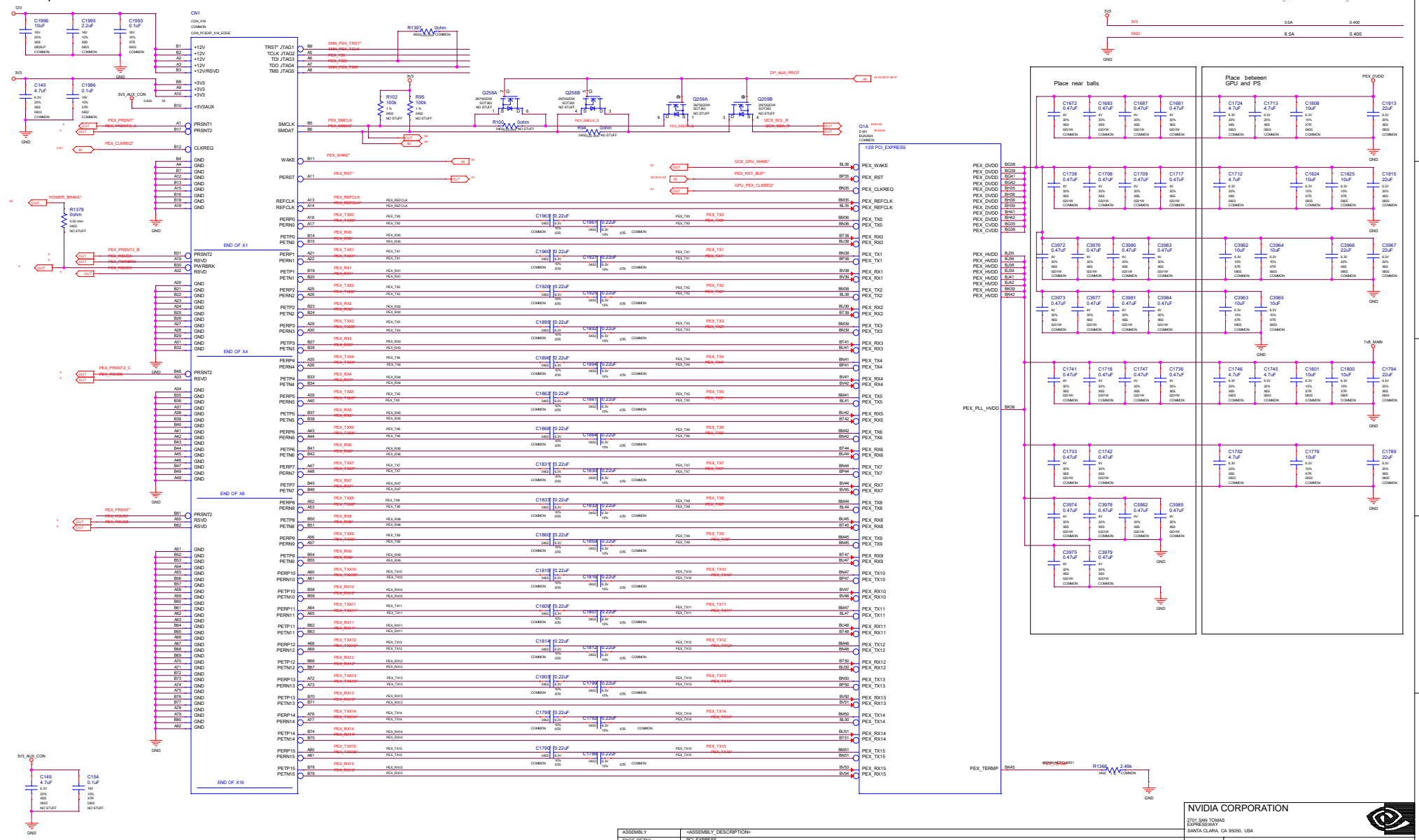


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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	BLOCK DIAGRAM

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-1G150-BASE-403		
POB REV	P0150-C03	PAGE	2 OF 66
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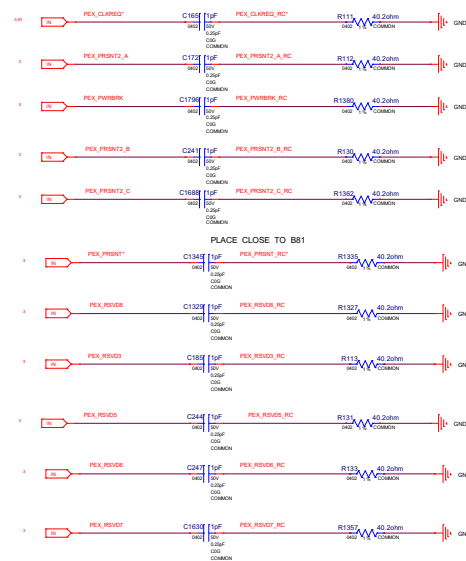
## PCI Express



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ASSEMBLY		<ASSEMBLY_DESCRIPTION>		EXPRESSWAY					
PAGE OF INIL		PG1 EXPRESS		SANTA CLARA, CA 95050, USA					
ISCLAMS				NV_PN		600-1G150-BASE-403			
				PCB REV		PG100-C03		PAGE	3 OF 60
				BOM REV		A		DATE	08-JUL-2018

## PCI TERM

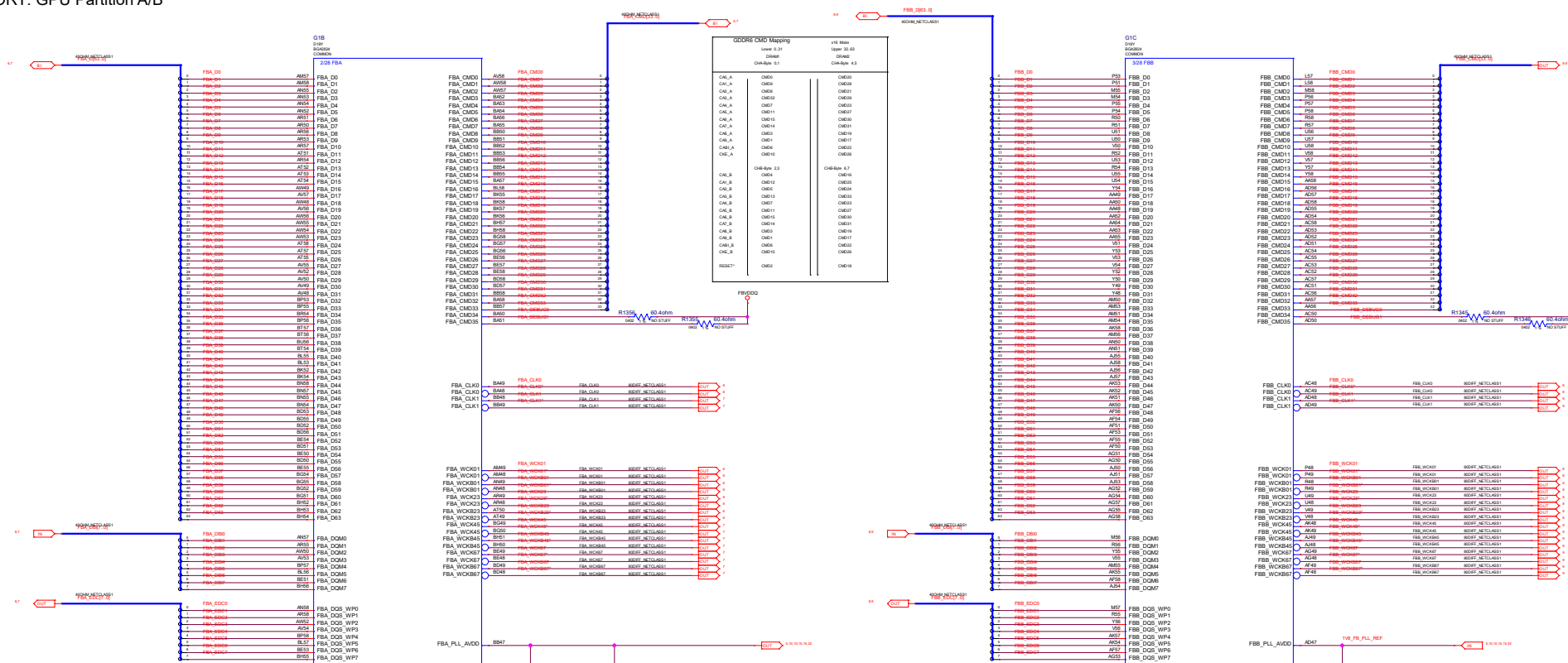


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ASSEMBLY	ASSEMBLY DESCRIPTION	SANTA CLARA, CA 95050, USA
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MAY		INV. PN 600-1G150-BASE-403
DISCIMS ALL		PCB REV PG1502-003 PAGE 4 OF 66
Y STANDARDS		BOOM REV A DATE 09-JUL-2018



# MEMORY: GPU Partition A/B



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ASSEMBLY: GPU PARTITION A/B  
PRICE DETAIL: MEMORY: GPU PARTITION A/B

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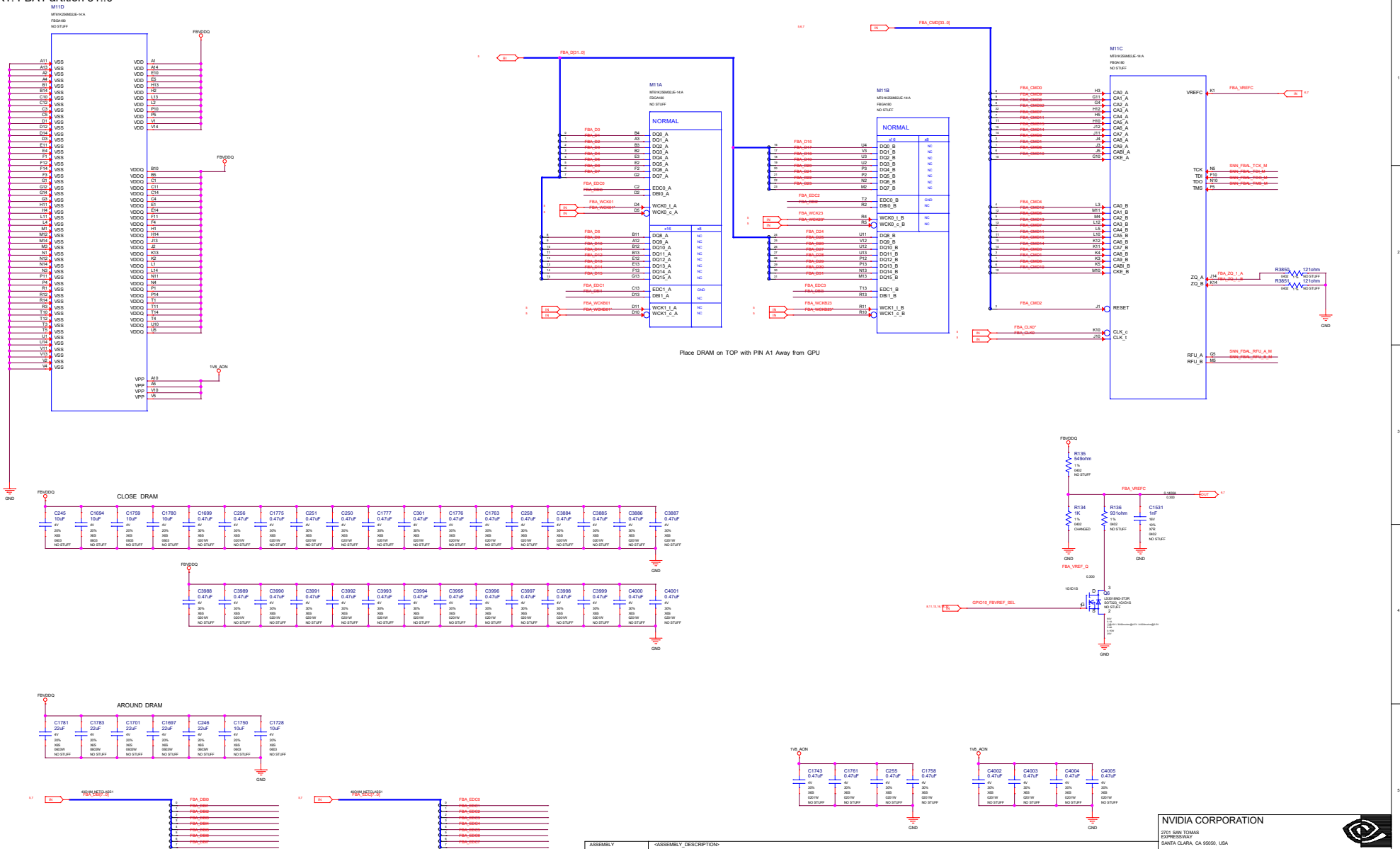
2701 SAN TOMAS  
EXPRESSWAY  
SANTA CLARA, CA 95058, USA



NV\_PN: 600-1G150-BASE-403

PCB REV: P0150-003  
BOM REV: A  
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# MEMORY: FBA Partition 31..0



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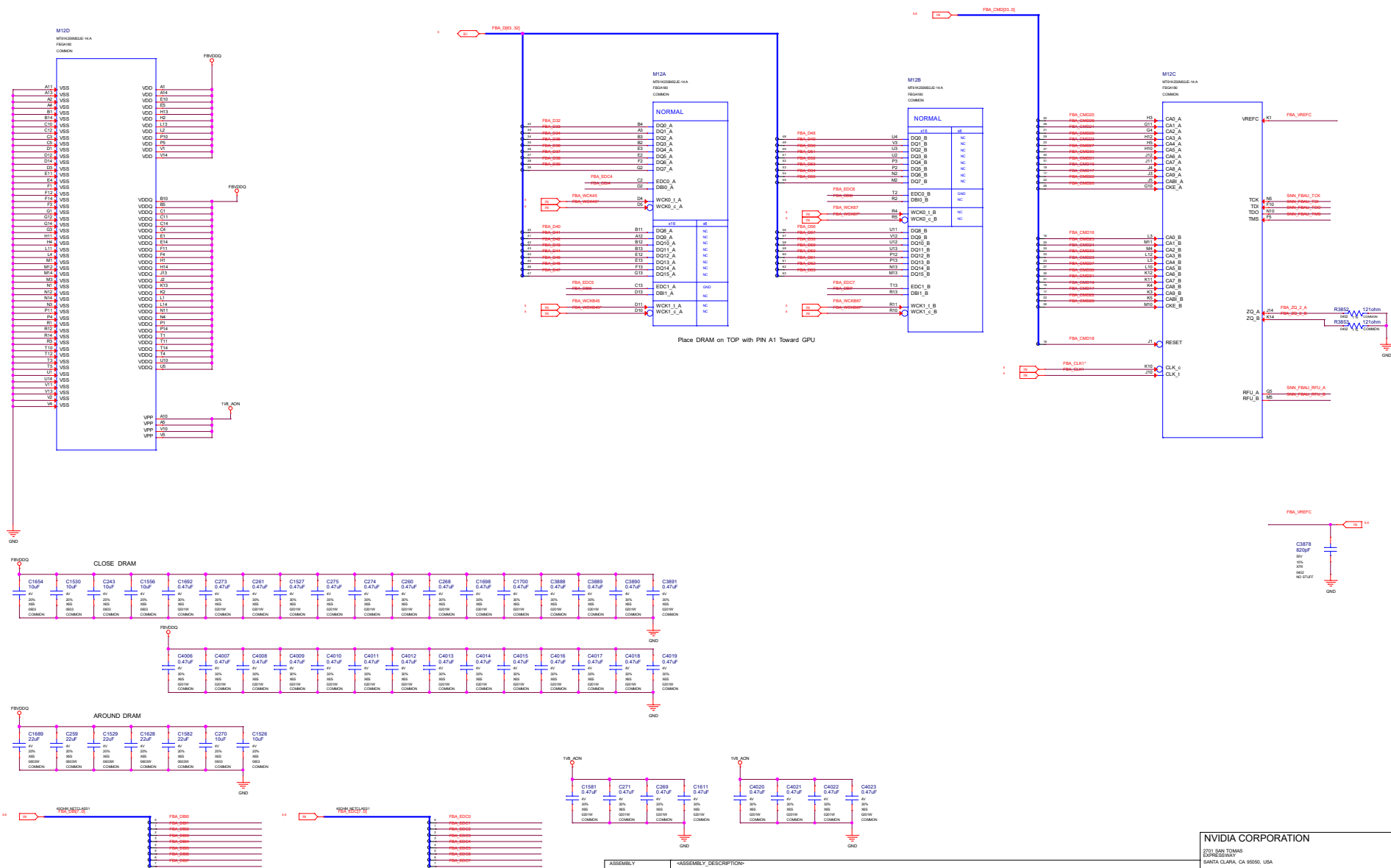
ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	MEMORY: FBA PARTITION 31..0

NV_PN	600-1G150-BASE-403
PCB REV	PG150-003
BOB REV	A

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NV\_PN 600-1G150-BASE-403

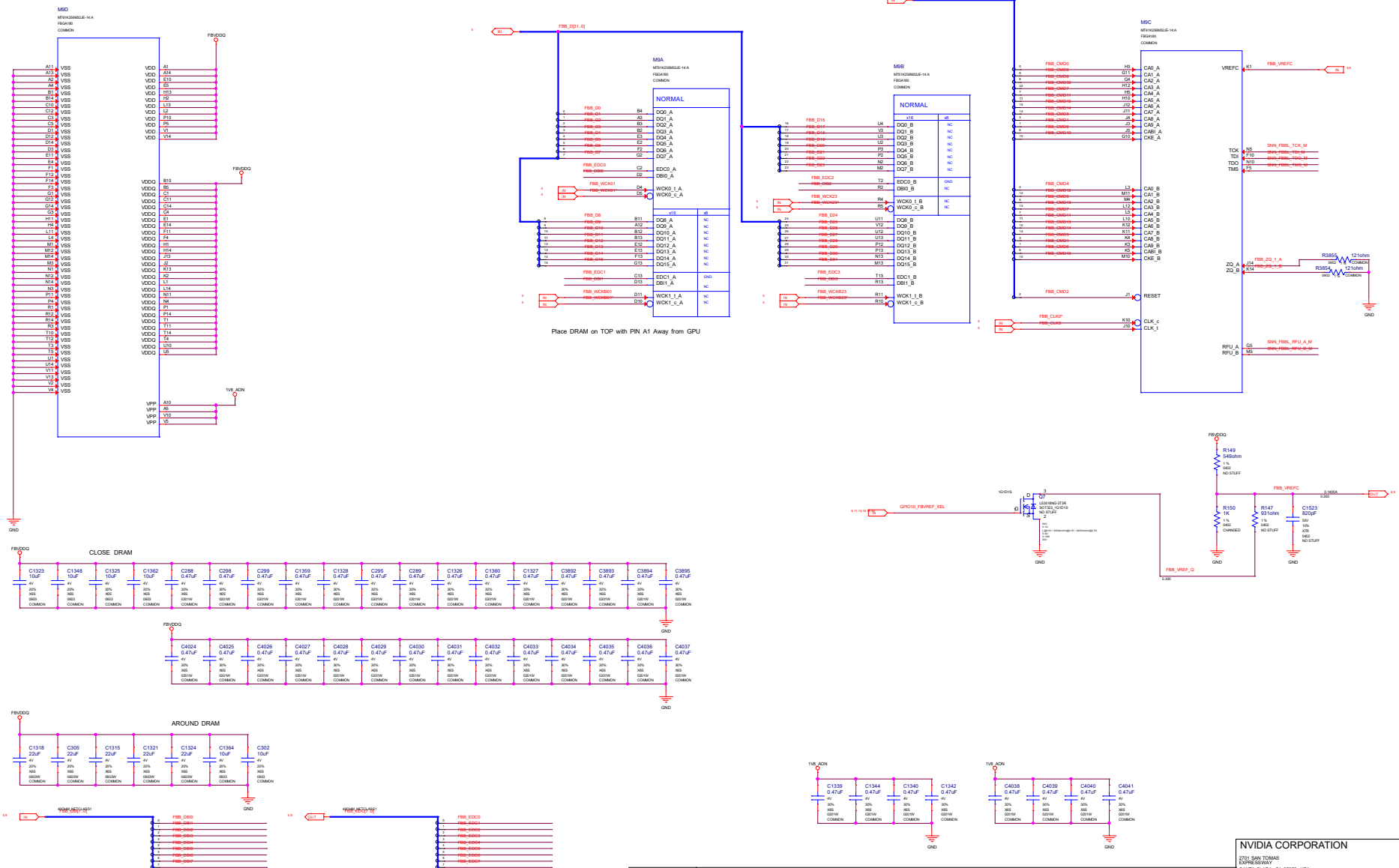
PCB REV PG150-003

BOM REV A


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DATE 09-JUL-2018

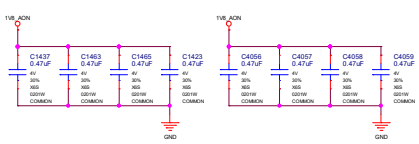
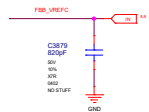
MEMORY: FBB Partition 31..0



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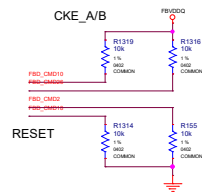
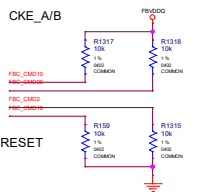
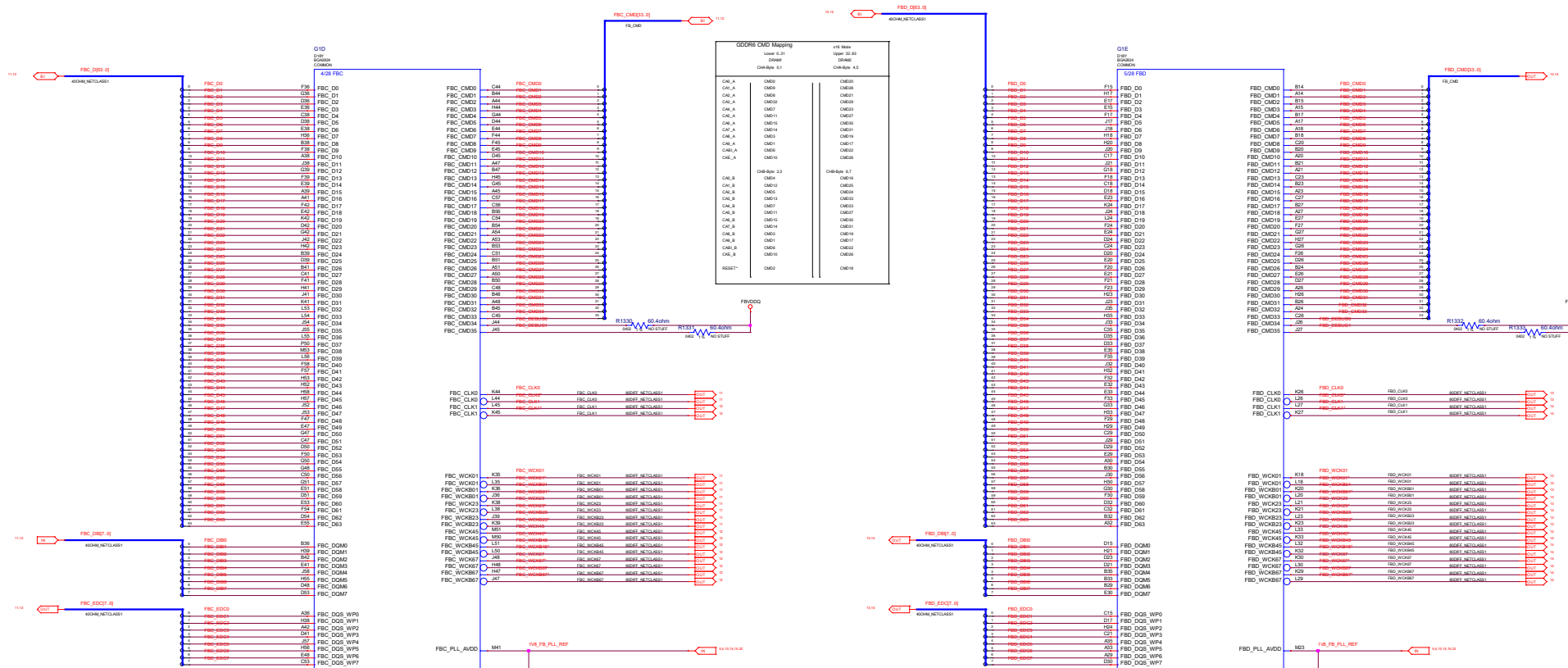
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PAGE OF 60	MEMORY TEST PARTITION(31.0)		
DISCLAIM		600-1G150-BASE-403	
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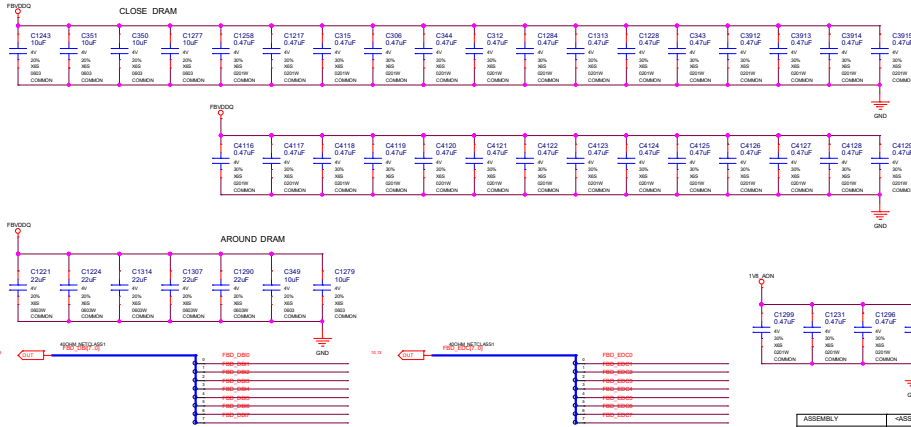
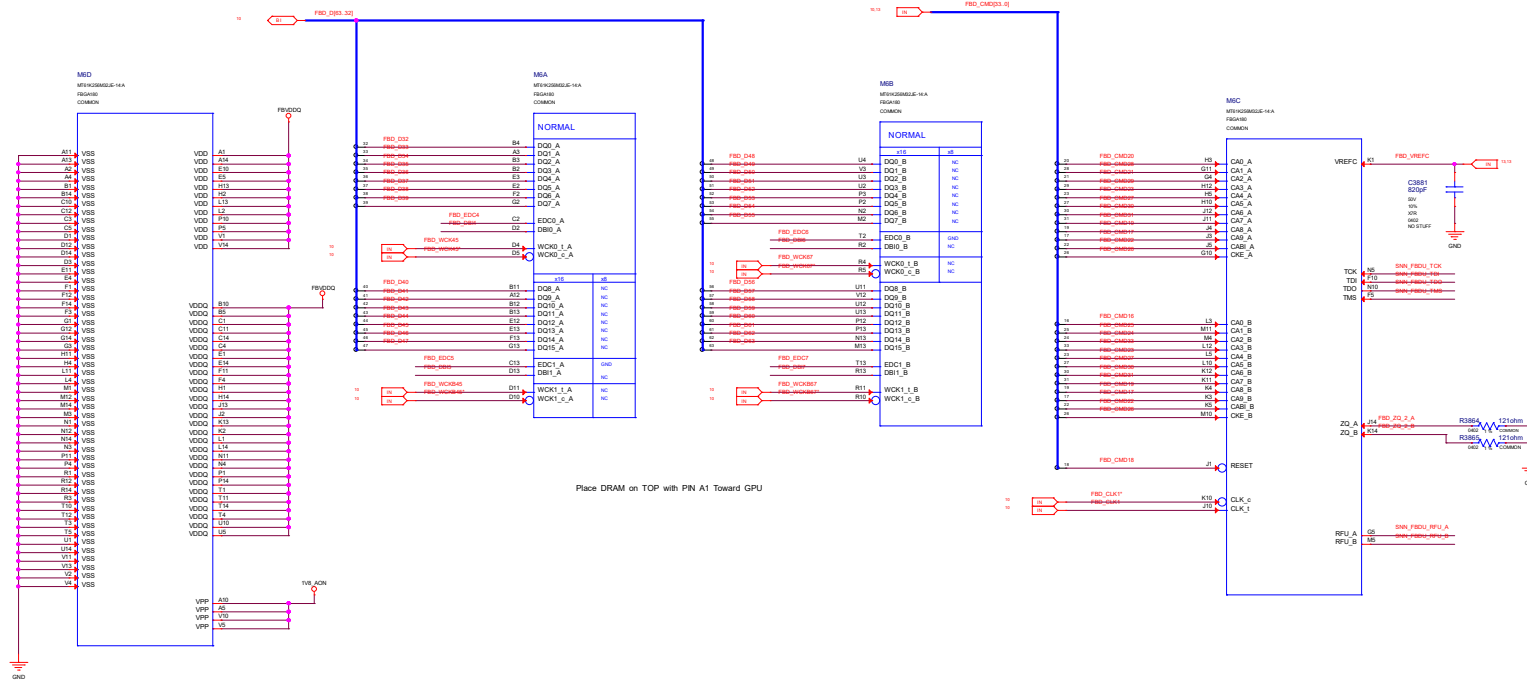
# MEMORY: GPU Partition C/D



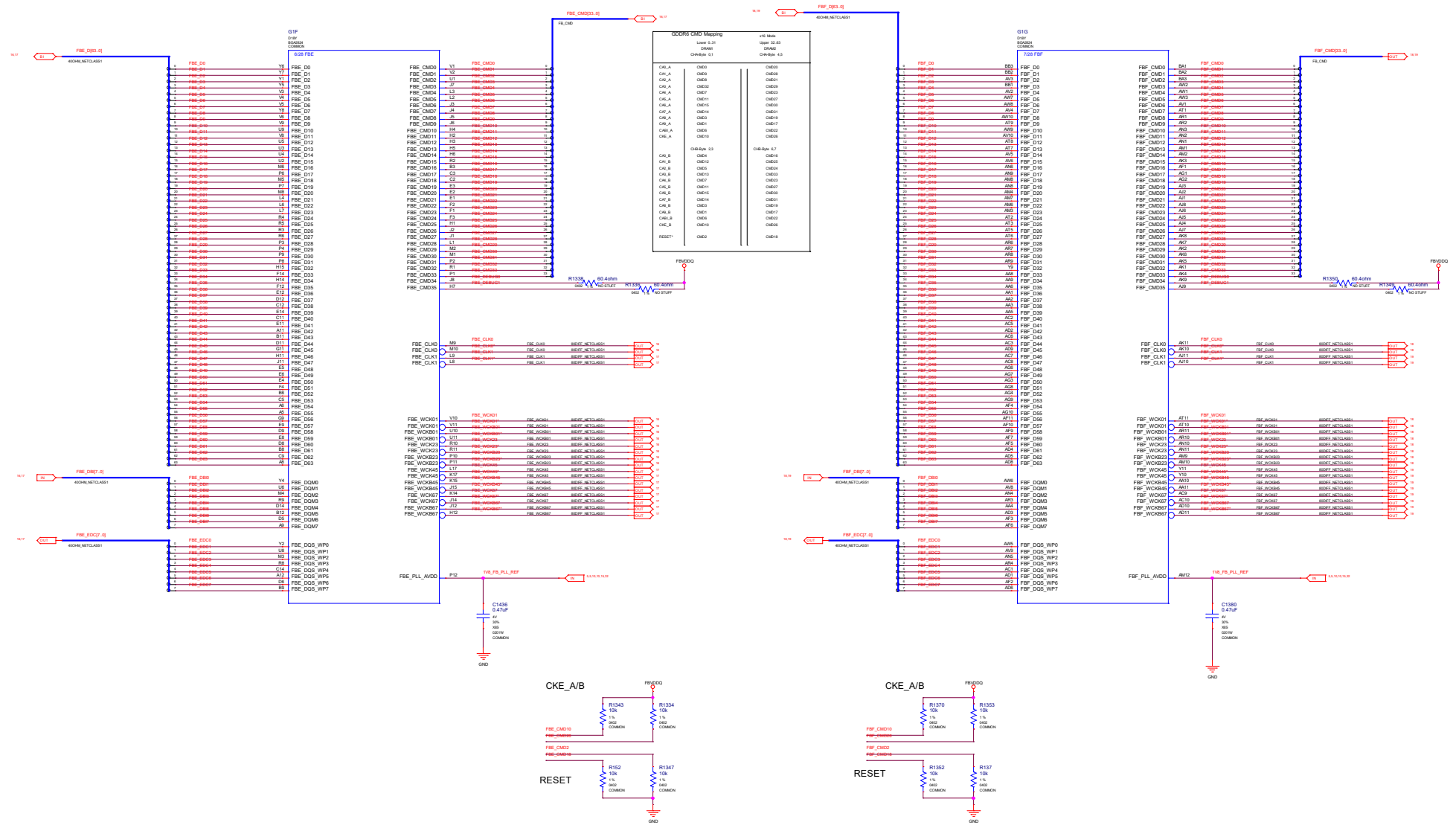




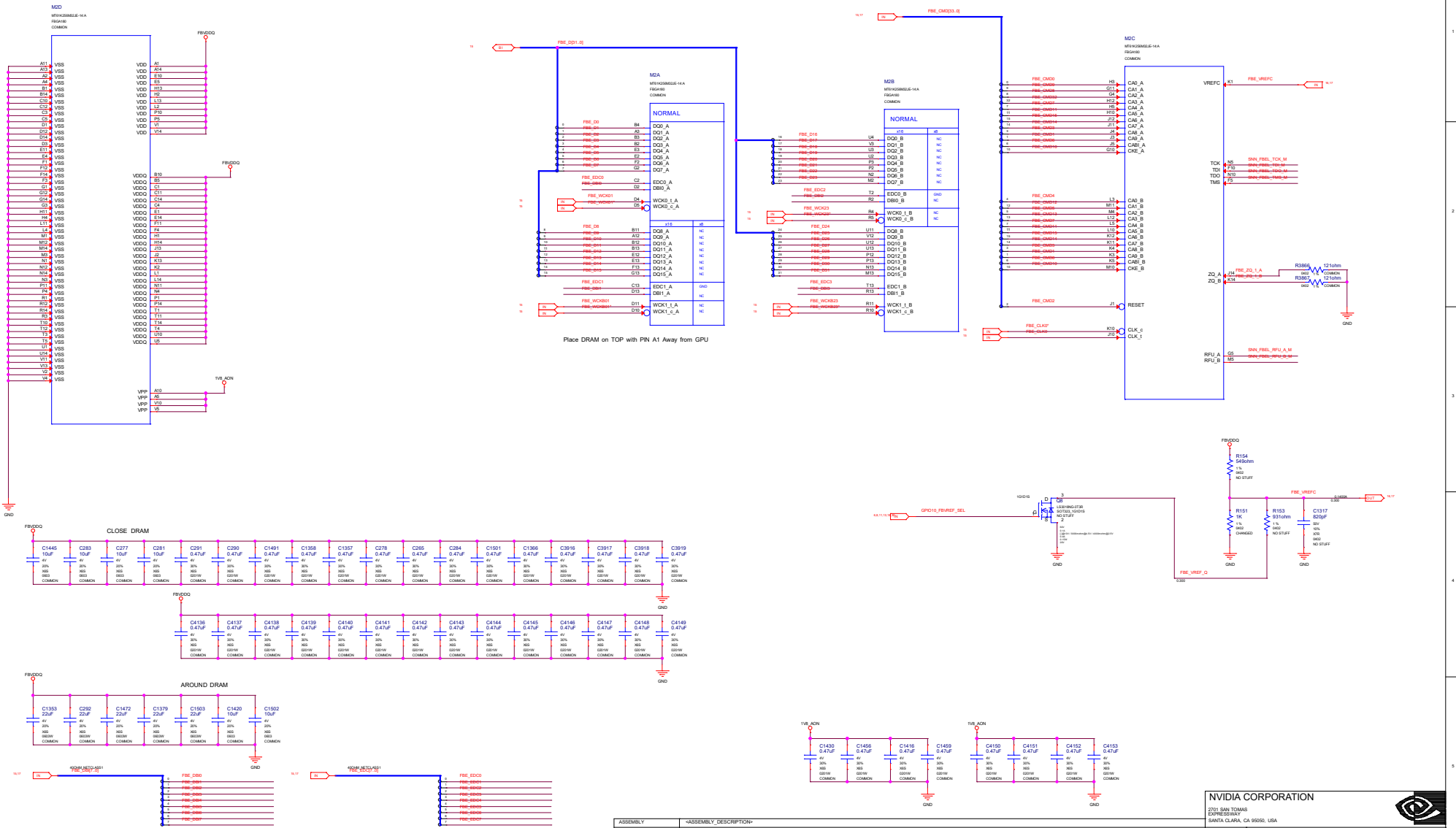




ASSEMBLY	ASSEMBLY DESCRIPTION
PRICE DETAIL	MEMORY: FBD PARTITION(63..32)



# MEMORY: FBE Partition 31.0

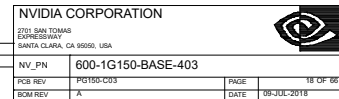


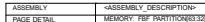
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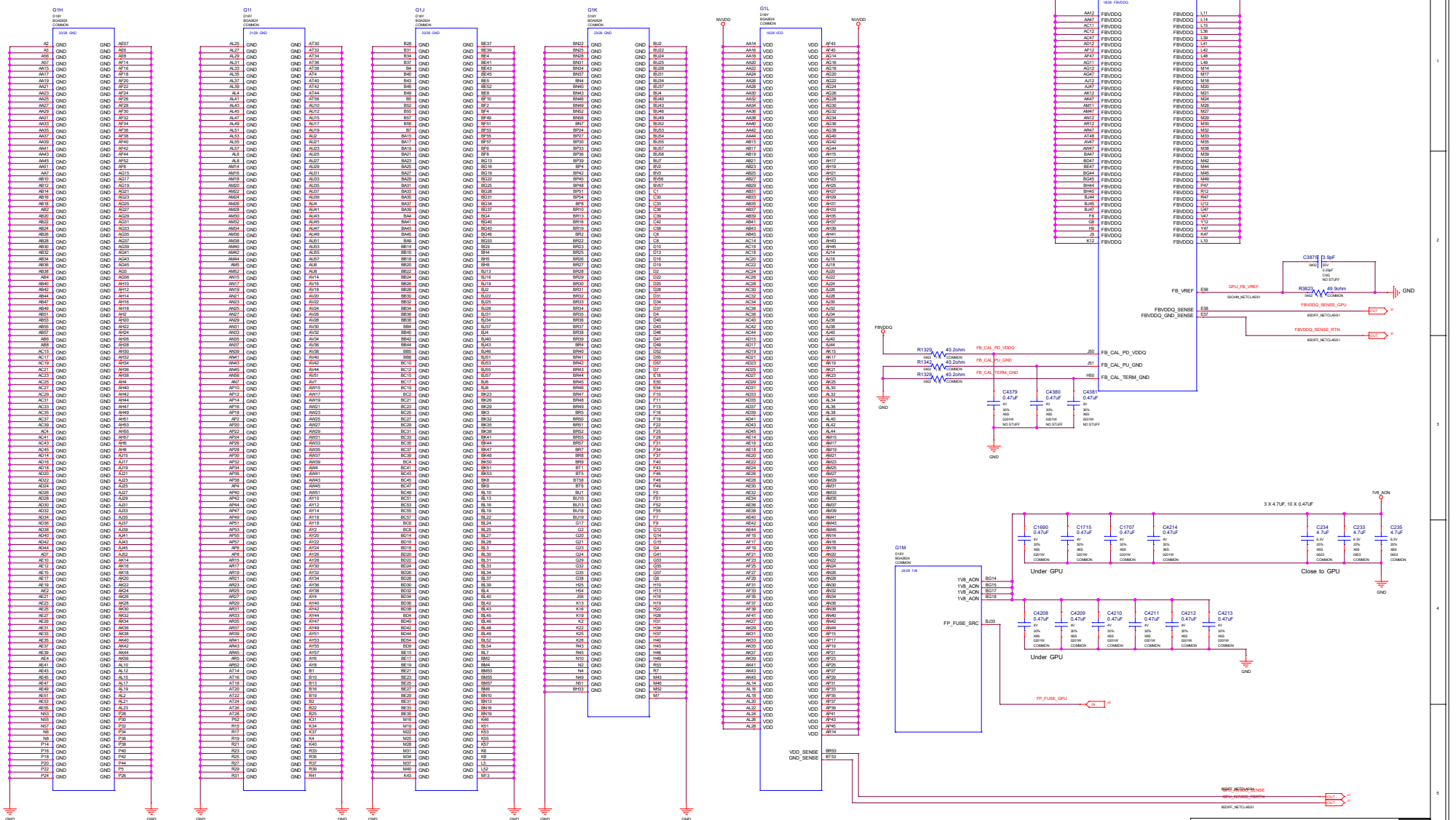


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PAGE DETAIL	MEMORY: FBE PARTITION(03/32)

<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
<b>NV_PN</b>		<b>600-1G150-BASE-403</b>	
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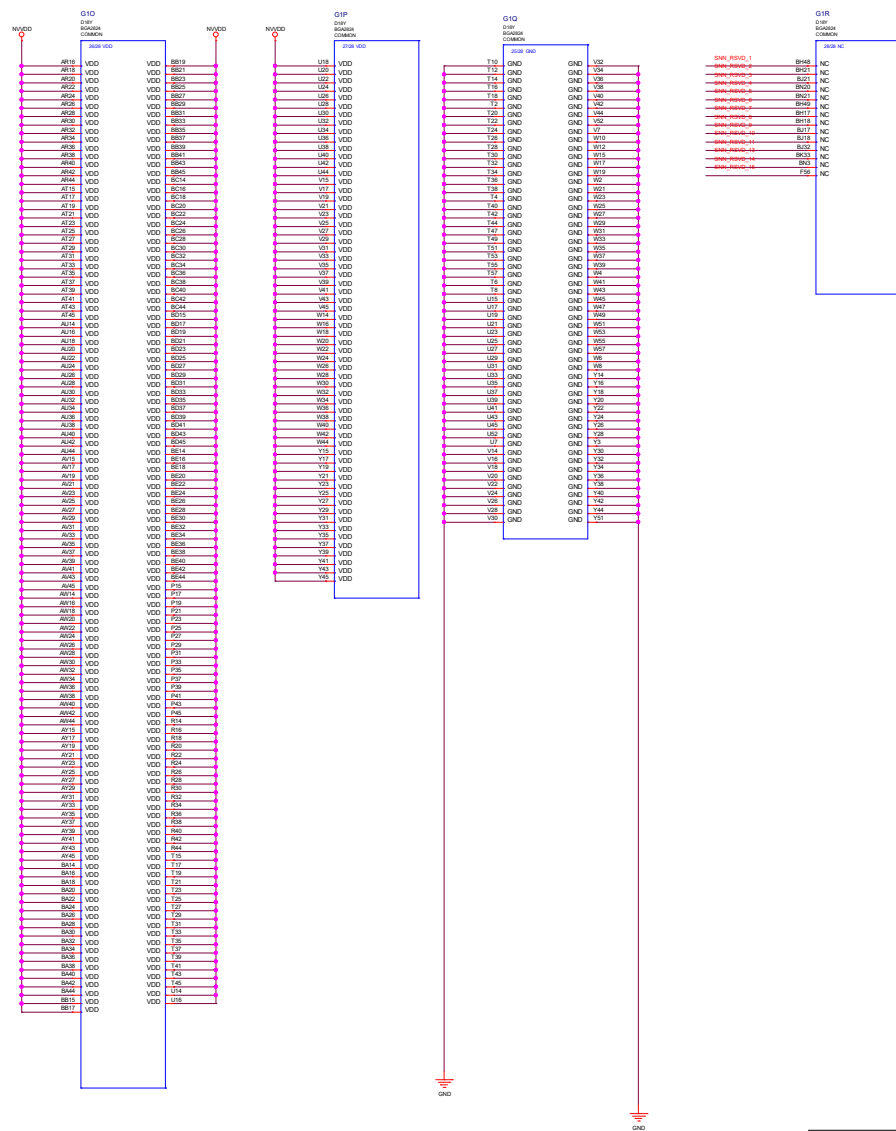
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ASSEMBLY		-ASSEMBLY DESCRIPTION-		SANTA CLARA, CA 95050, USA	
PAGE DETAIL		CPU PWR AND CDR		NV_PN 600-1G150-BASE-403	
ISCLAIM		PCB REV		PG150-C03	PAGE 26 OF 66
		BOM REV		A	DATE 09-JUL-2018

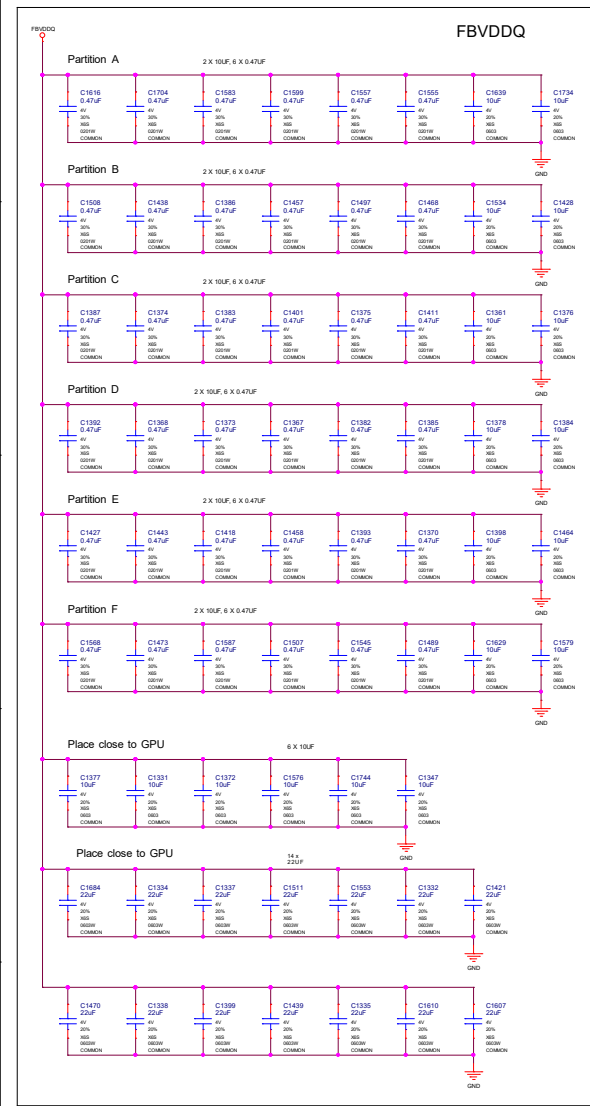
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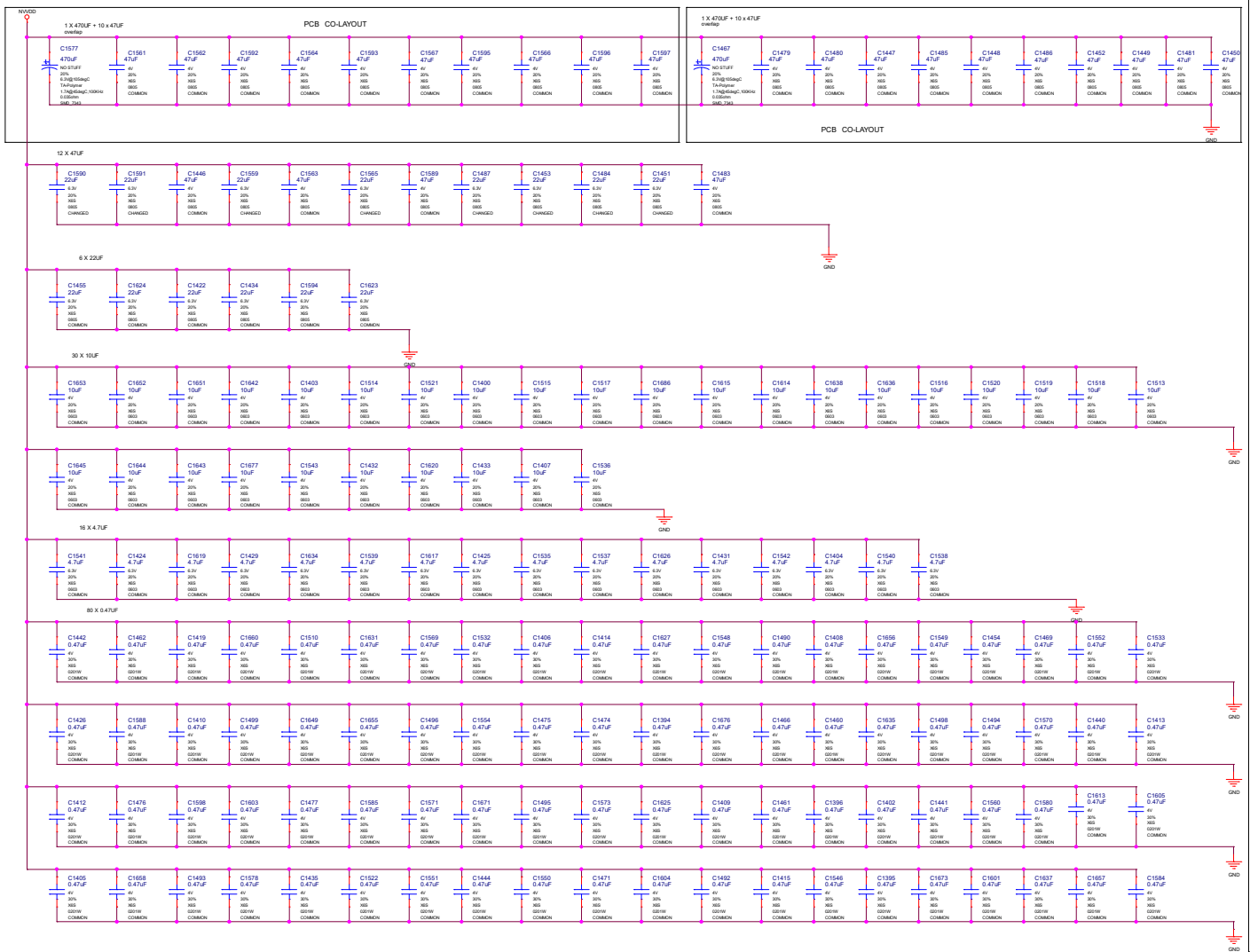
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR, GND and NCs

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## GPU Decoupling



## NVVDD



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EXPRESSWAY  
SANTA CLARA, CA 95050, USA

NV\_PN 600-1G150-BASE-403

PCB REV PG150-DB3

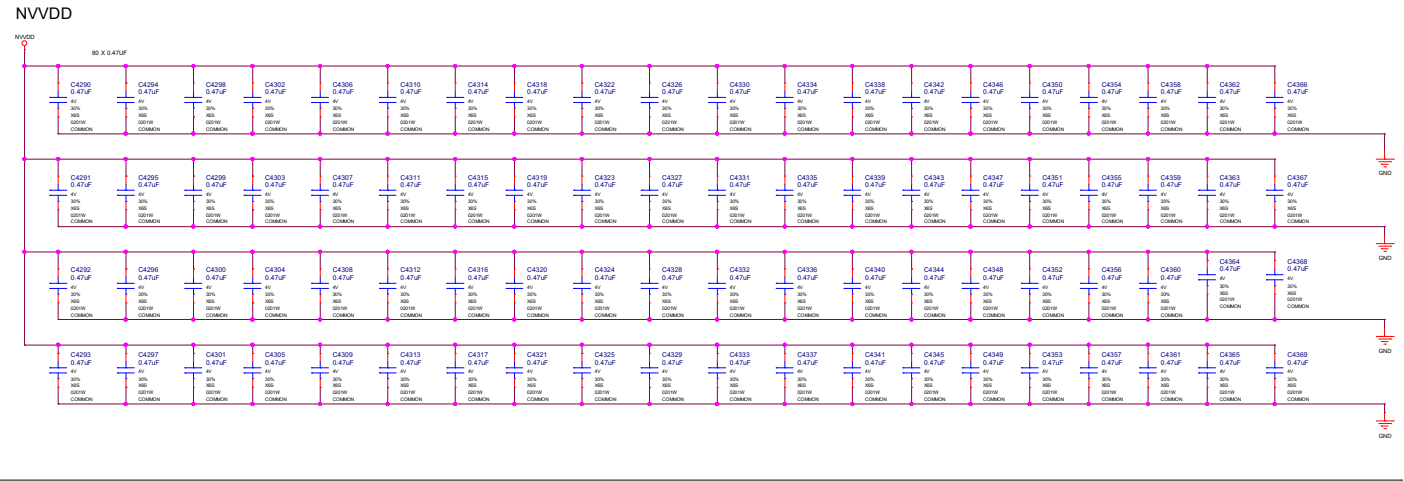
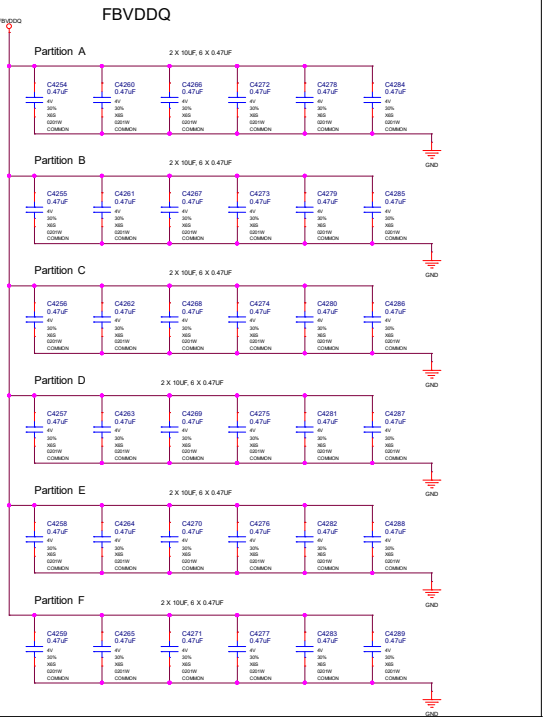
BOM REV A

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GPU Decoupling

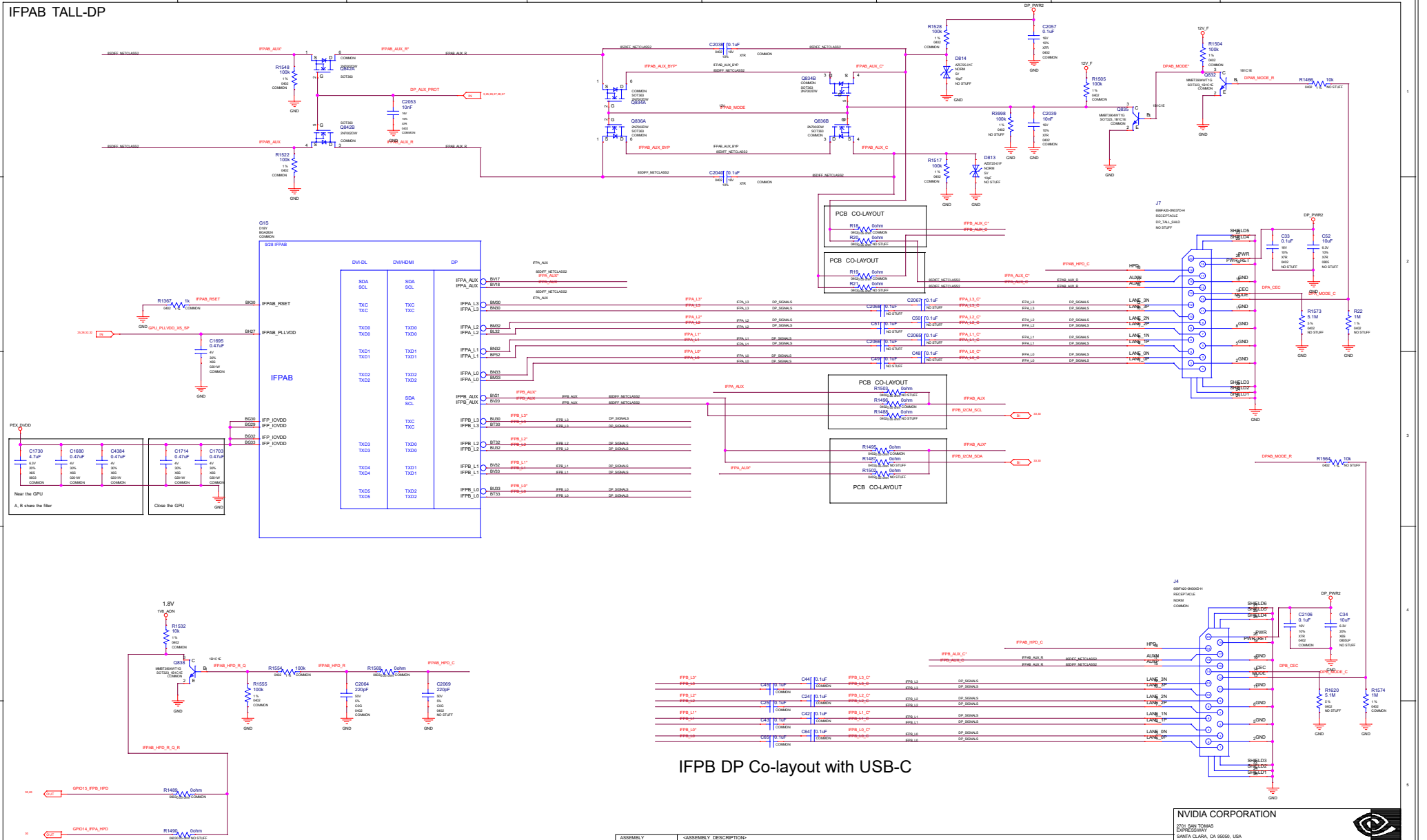


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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	GPU DECOUPLING 2

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95058, USA			
NV_PN	600-1G150-BASE-403		
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## IFPAB TALL-DP

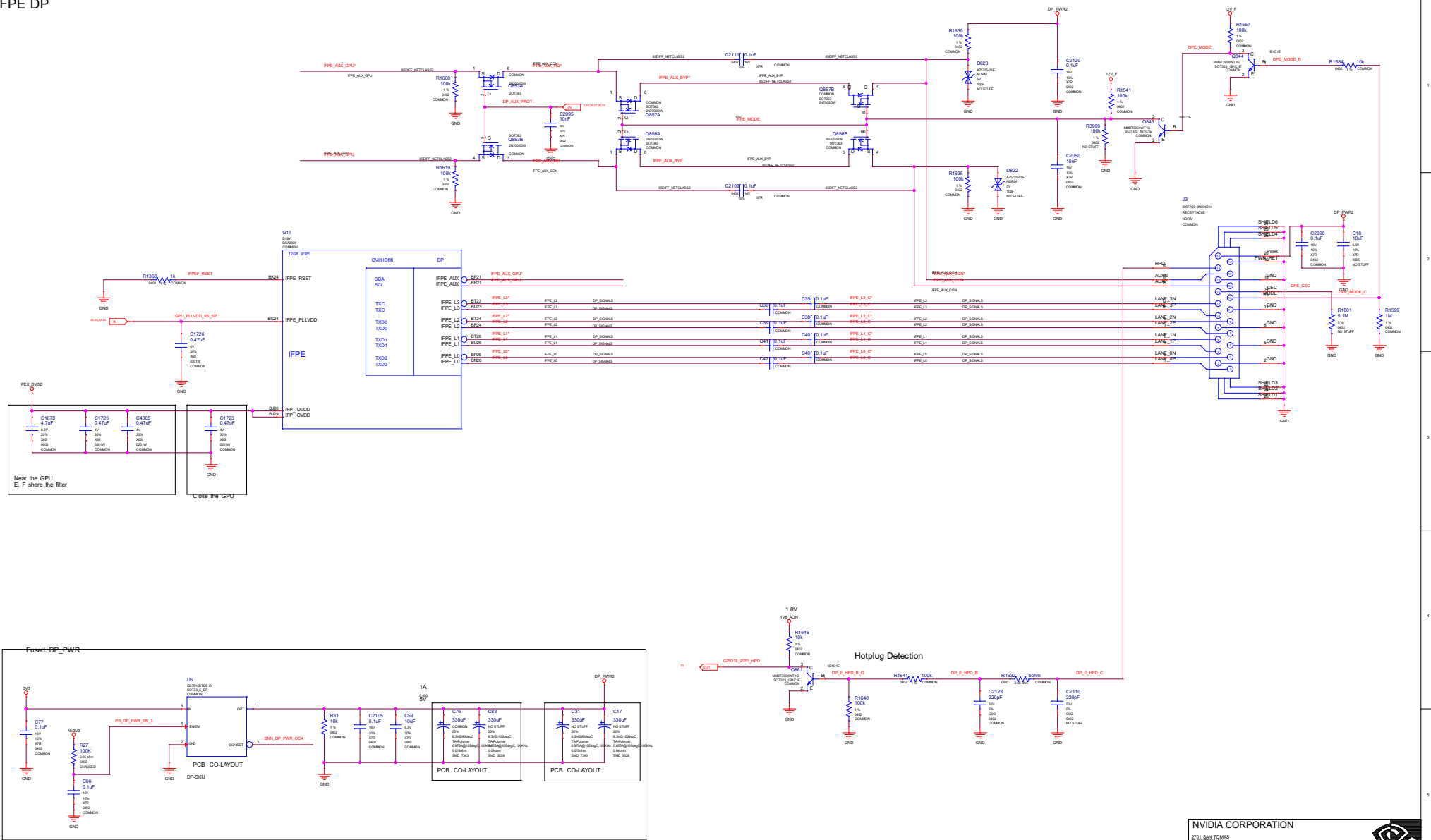


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				NV_PN		600-1G150-BASE-403	
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## IFPE DP

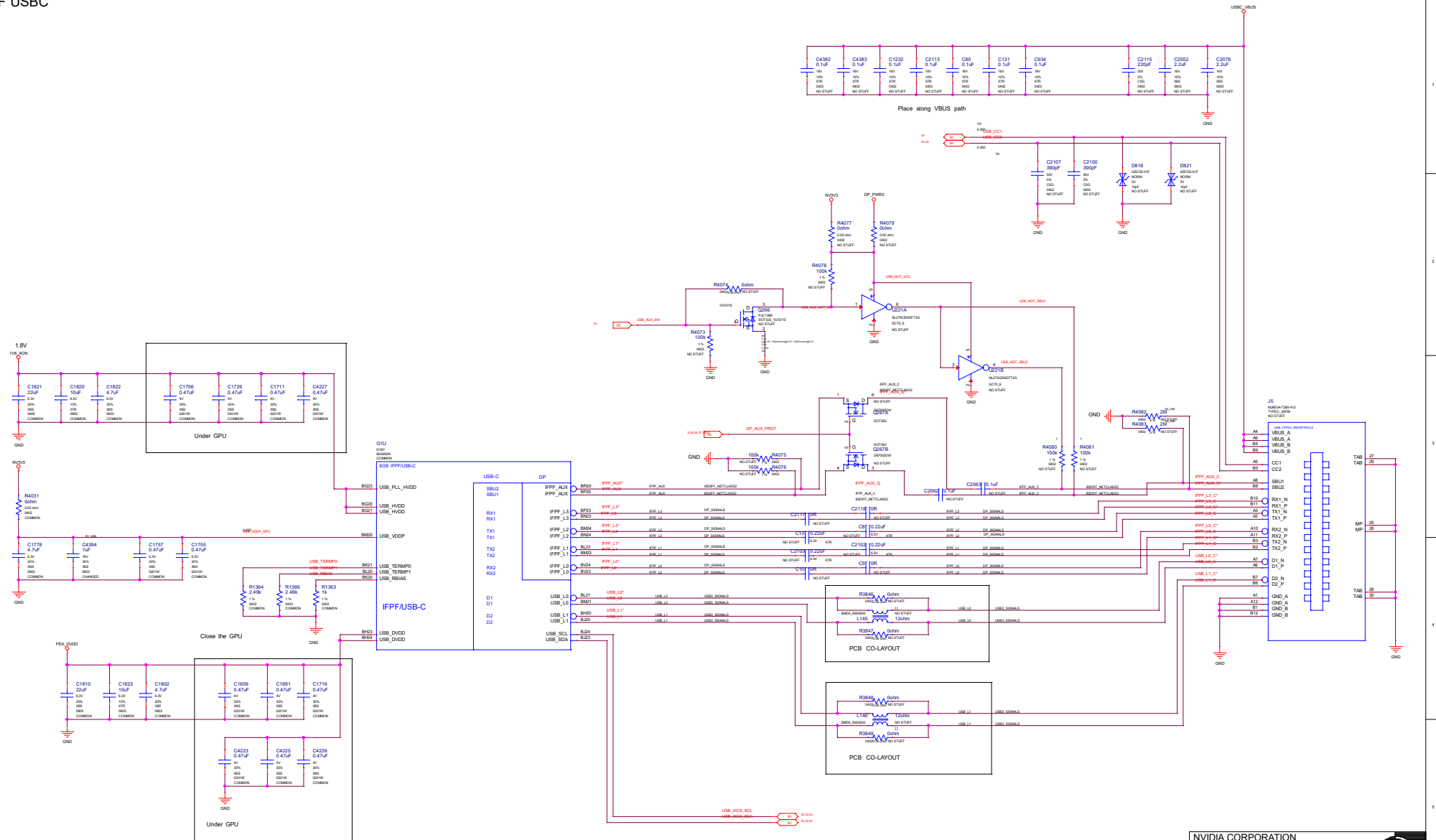



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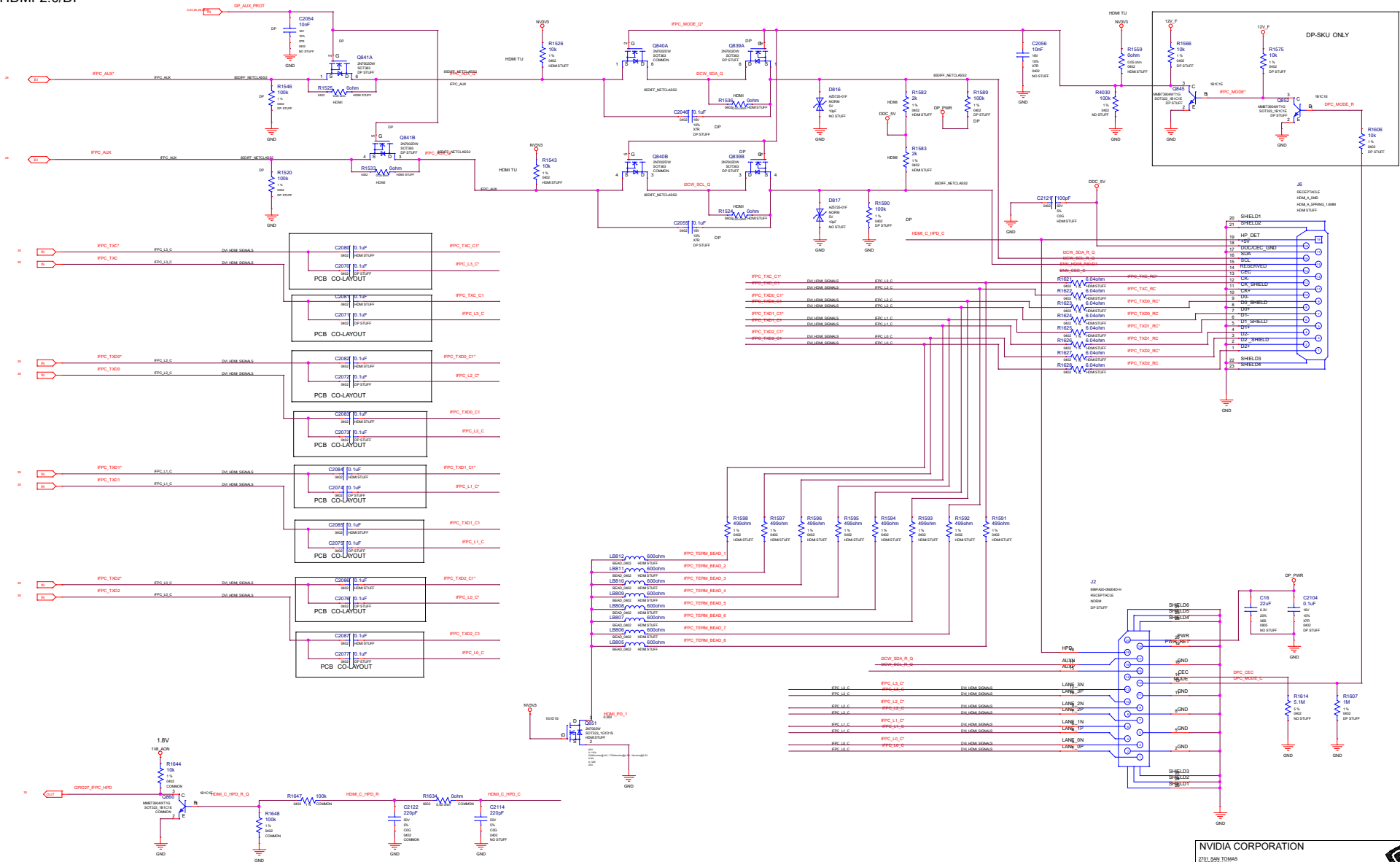


<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
<b>NV_PN</b>		<b>600-1G150-BASE-403</b>		
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## IFPC HDMI 2.0/DP



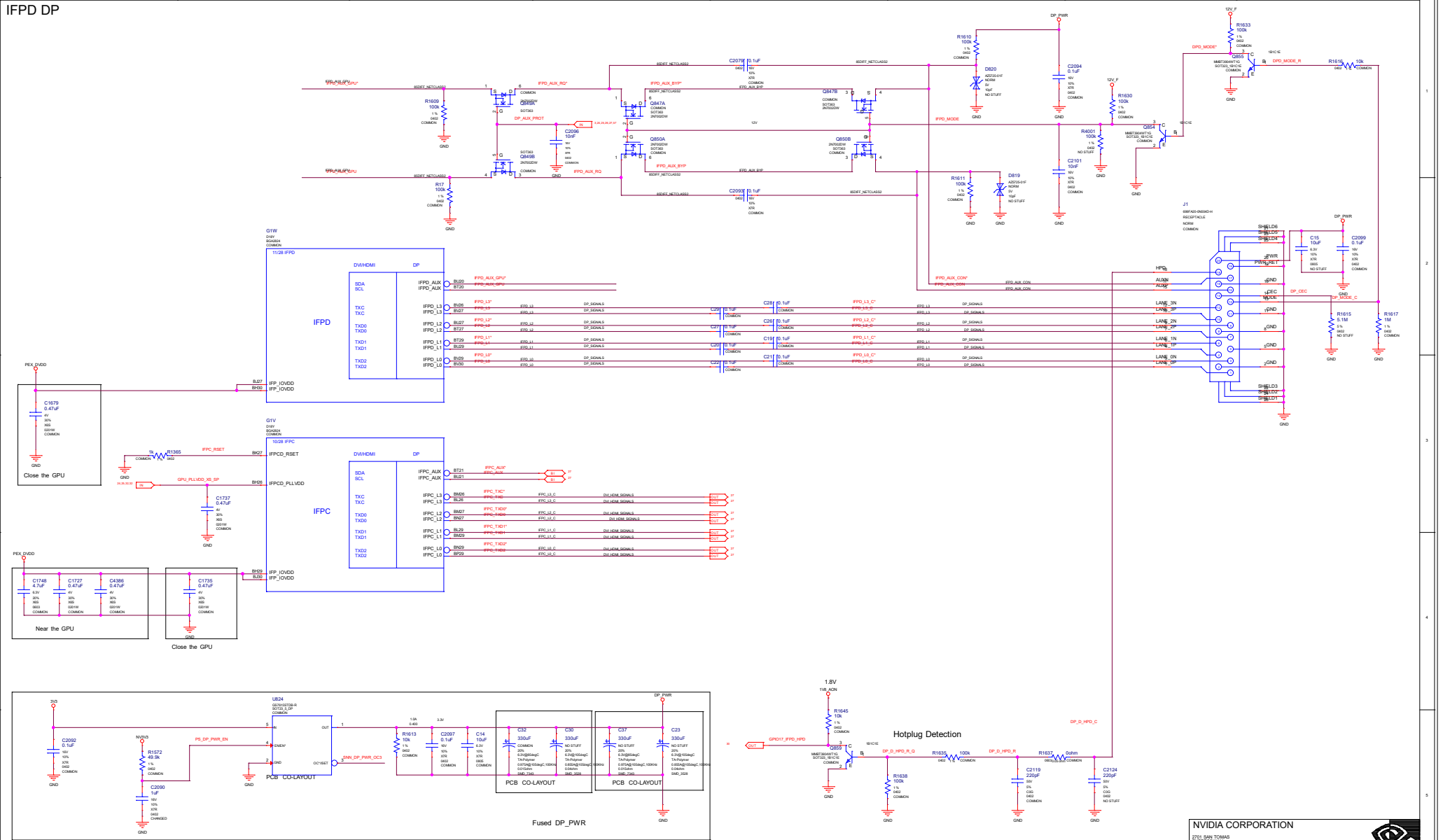
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IIFPC HDMI/OP

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NV PN	600-1G150-BASE-403
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# IFPD DP

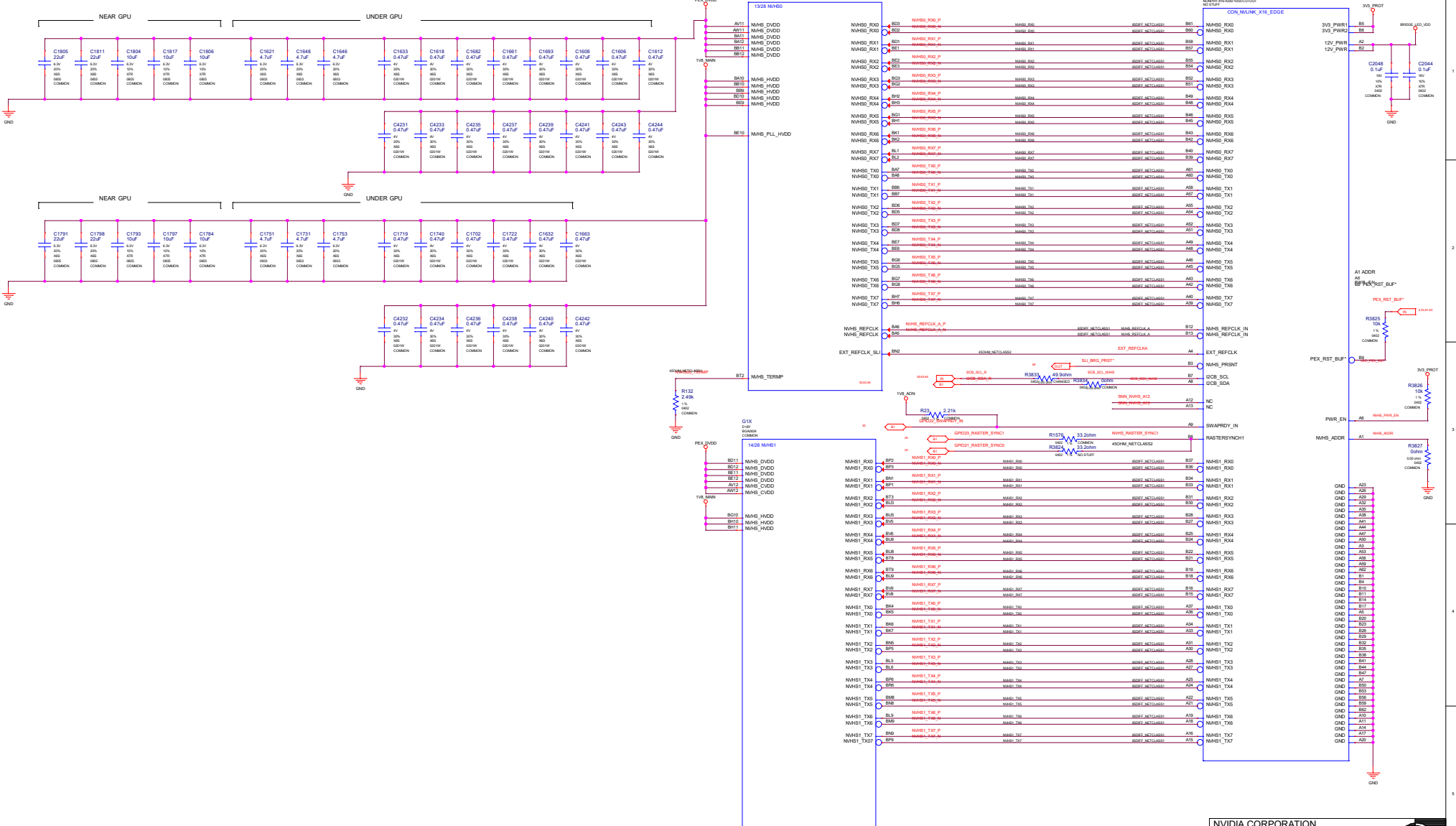


ASSEMBLY		ASSEMBLY DESCRIPTION	
PAGE DETAIL		IFPD DP	
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NV_PN		600-1G150-BASE-403	
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## NVHS Interface and FRAME LOCK



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	NVHS X16

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<b>NV_PN</b>		<b>600-1G150-BASE-403</b>		
<b>PCB REV</b>		<b>PG150-C03</b>		<b>PAGE</b> 25 OF 66
<b>BOM REV</b>		<b>A</b>		<b>DATE</b> 09-JUL-2018

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PCB REV	PG150-C03
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BOM REV	A	DATE	09-JUL-2018
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	H
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MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
H	L	H	00101
H	H	L	00110
H	H	H	00111
L	L	M	01000
L	M	L	01001

DEFAULT

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

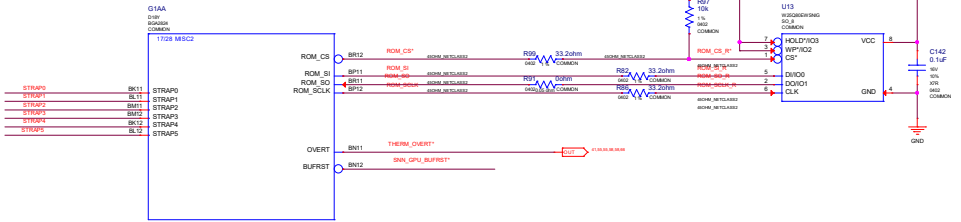
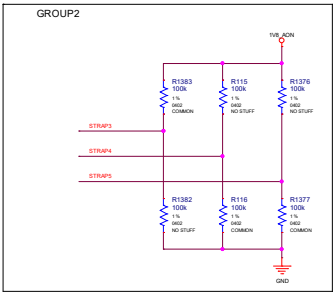
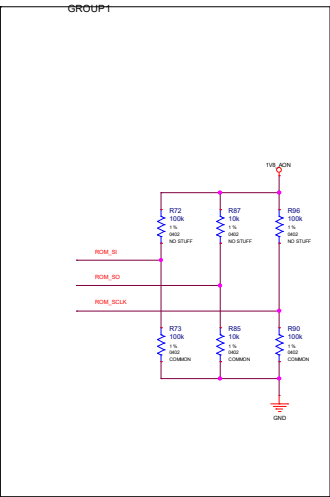
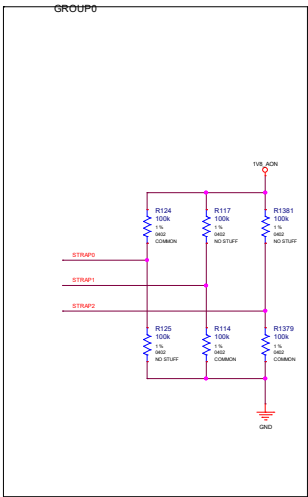
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	H	XXX0	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

SKU 200



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ASSEMBLY	ASSEMBLY DESCRIPTION
PRICE DETAIL	MISC ROM, STRAPS

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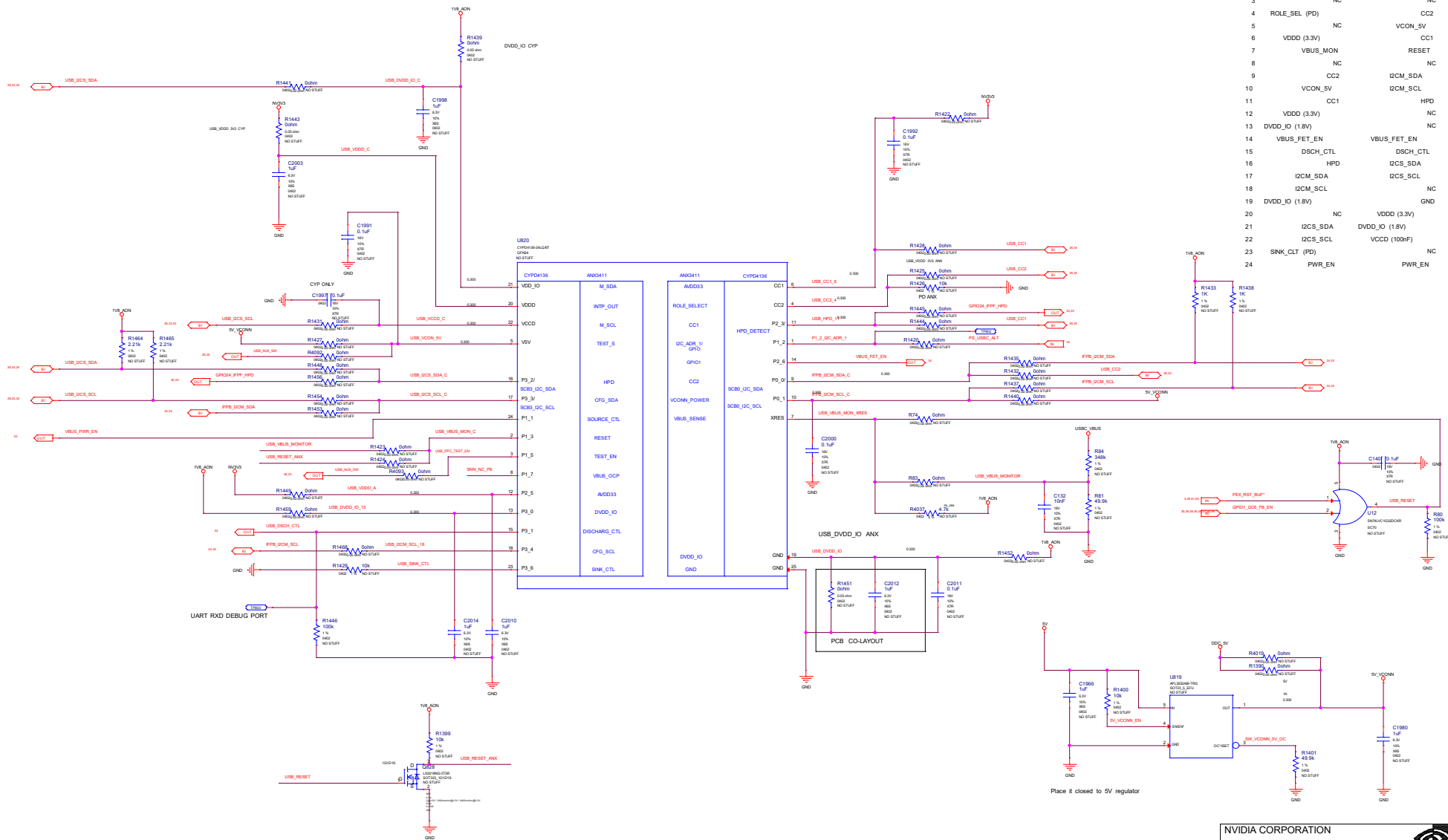
NV\_PN 600-1G150-BASE-403

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MISC: USB PPC



PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDO (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDO (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDO (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100mF)
23	SINK_CTL (PD)	NC
24	PWR_EN	PWR_EN

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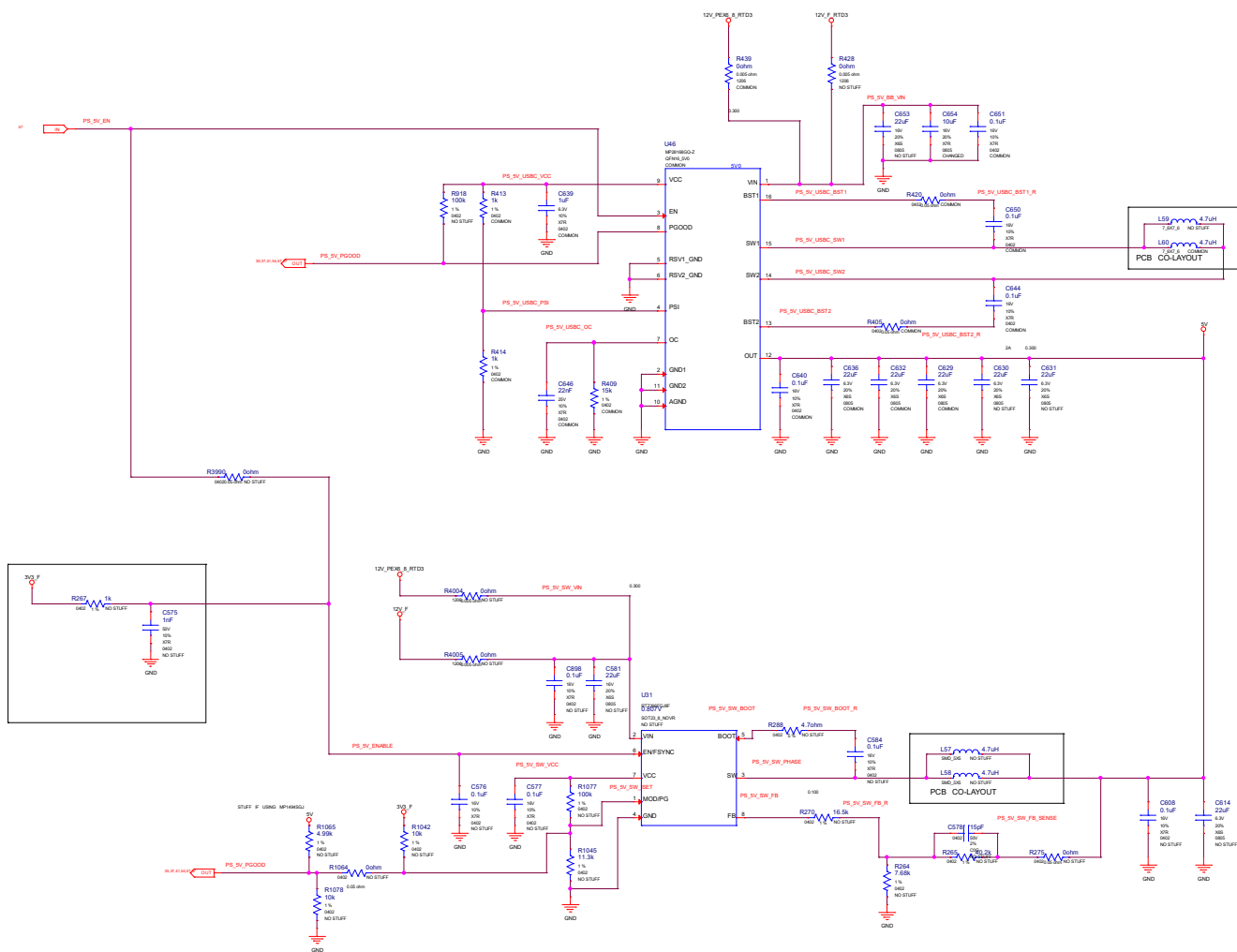
ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	MISC: USB PPC


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PCB REV	PG150-003
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DATE	09-JUL-2018

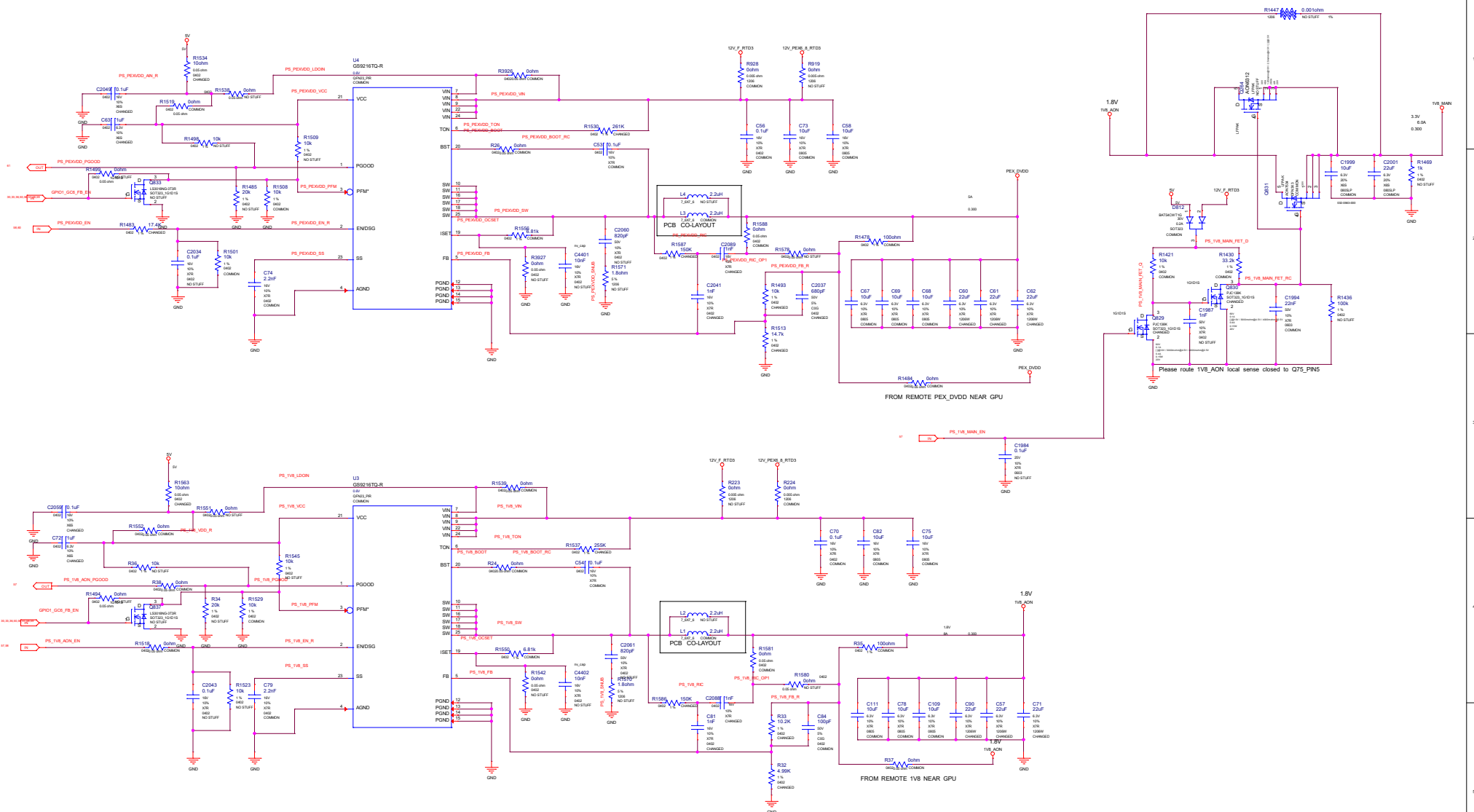




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NV_PN	600-1G150-BASE-403		
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PS: PEXVDD 1V8 Rail



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REV	000-10
PCB REV	PG150-C0

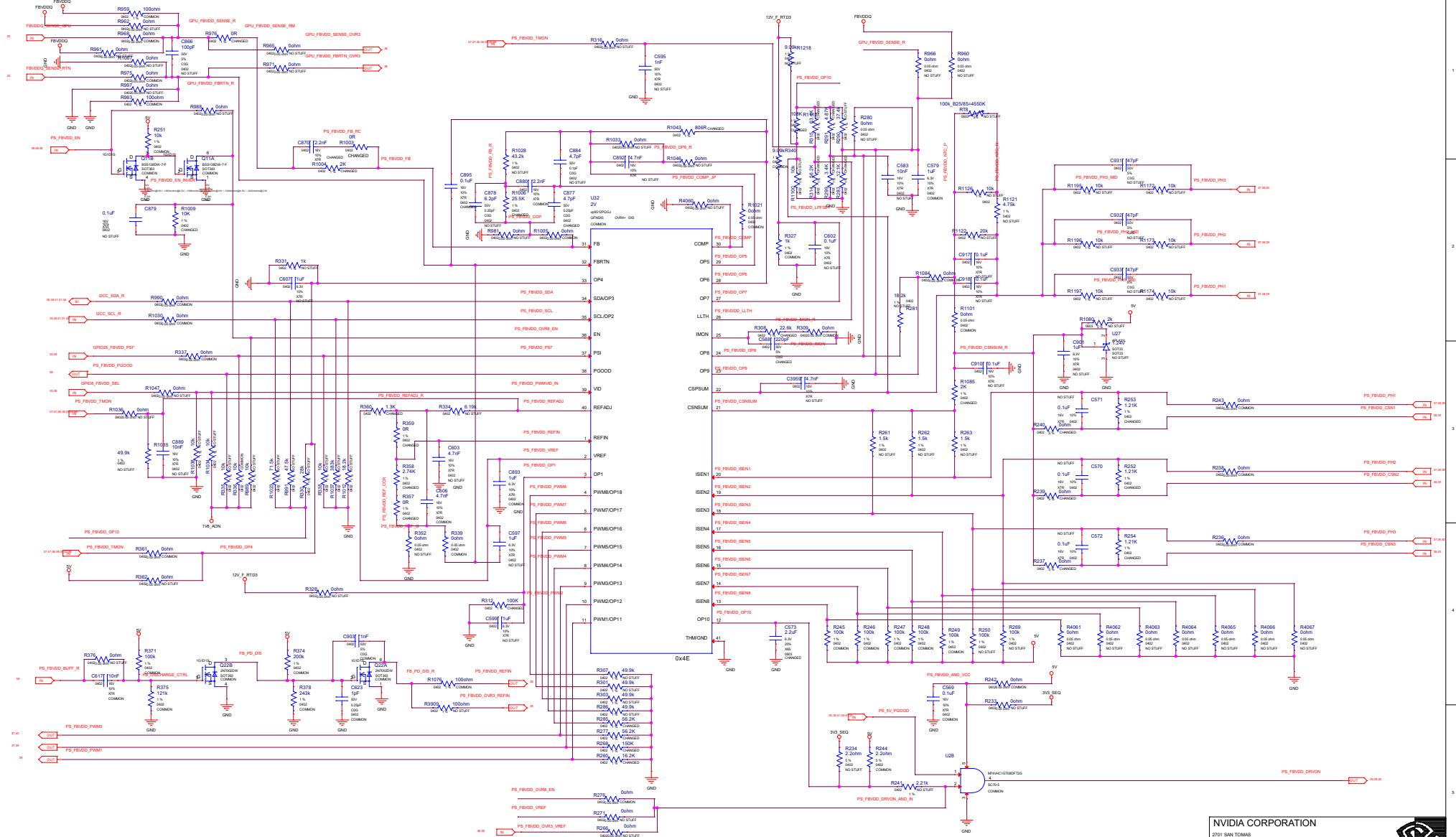
BOB REV	A	DATE	09-JUL-2018
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEXVDD 1V8 Rail

# PS: FBVDD Controller



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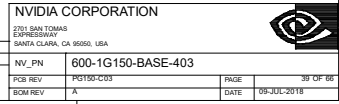
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ASSEMBLY DESCRIPTION

PS: FBVDD Controller

PAGE DETAIL

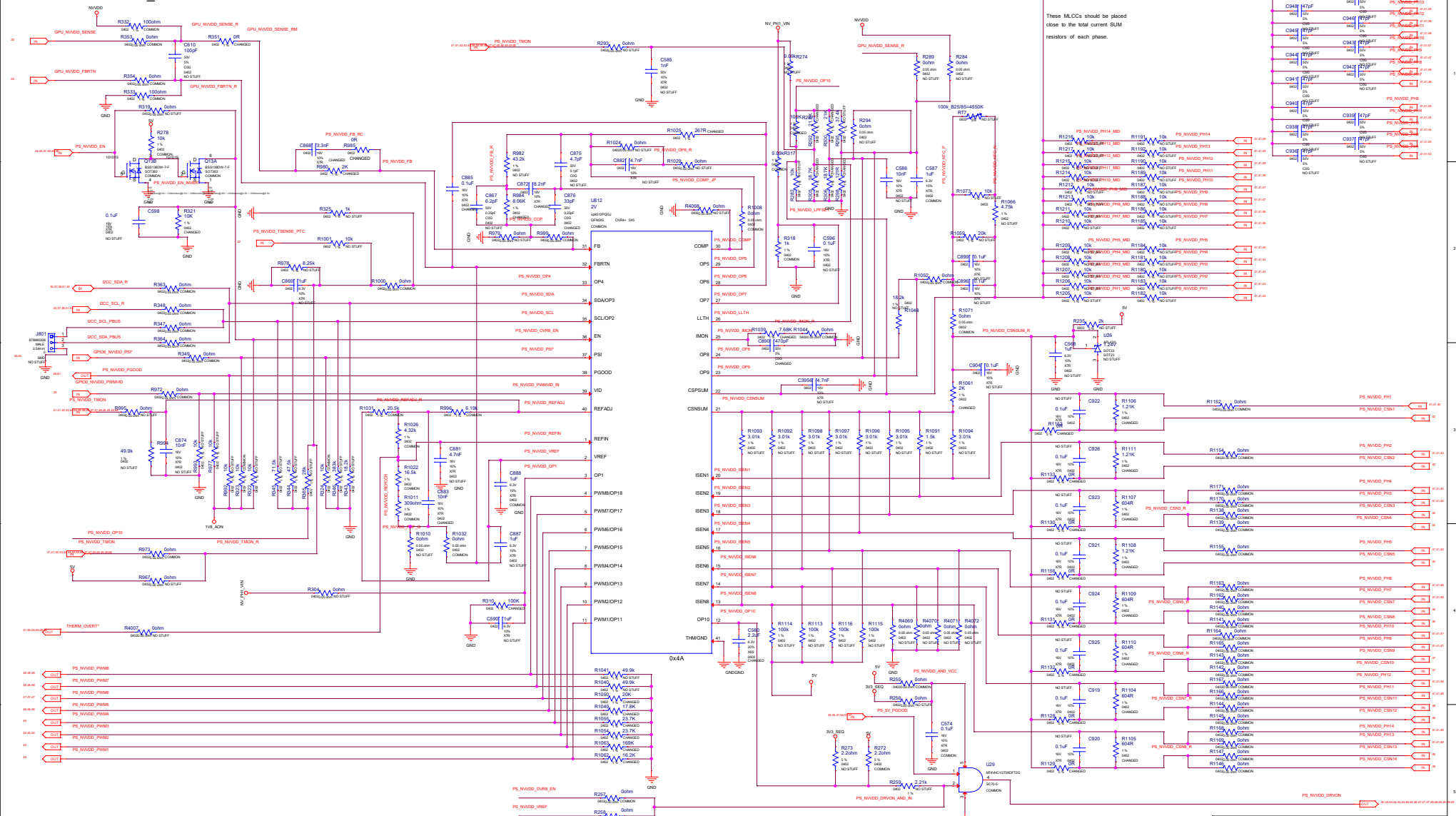









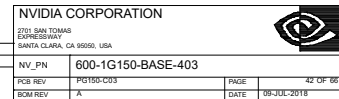
## PS: NVVDD Controller\_OVR8

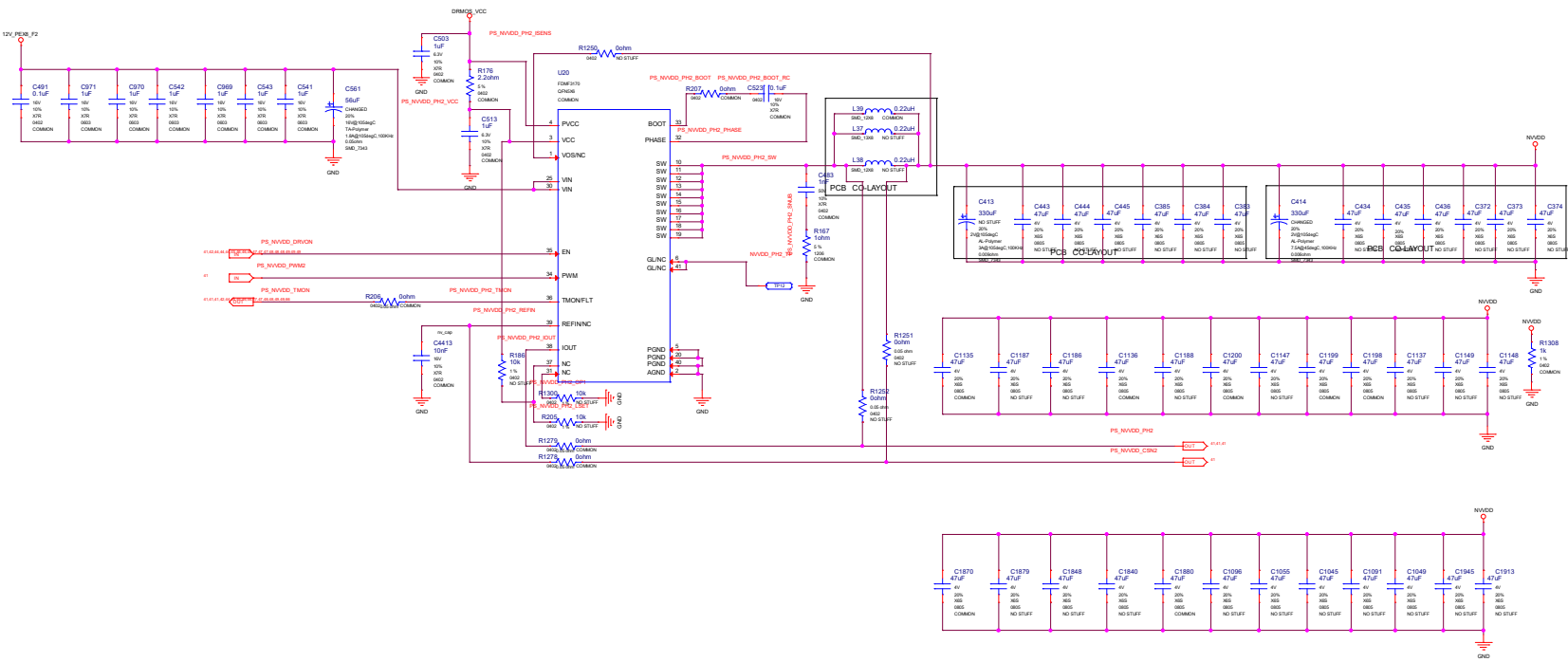


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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVD0 Controller QVR8

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<b>NV_PN</b>		<b>601-1G150-BASE-403</b>		
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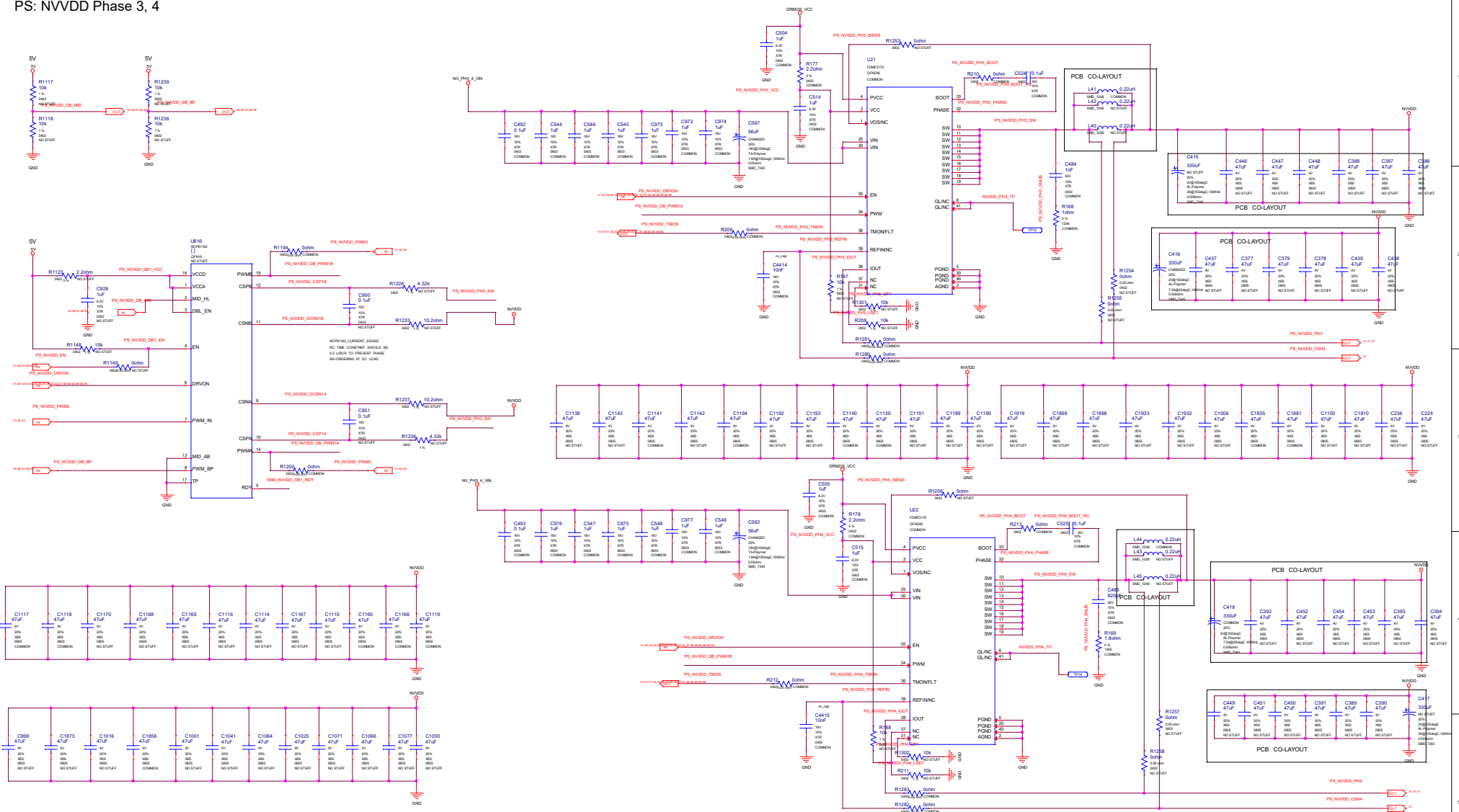


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ASSEMBLY		"ASSEMBLY" DESCRIPTION	
PRICE DETAIL	PS: NVVDD Phase 2		

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NV_PN	600-1G150-BASE-403	PCB REV	PG150-C03
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PS: NVVDD Phase 3, 4



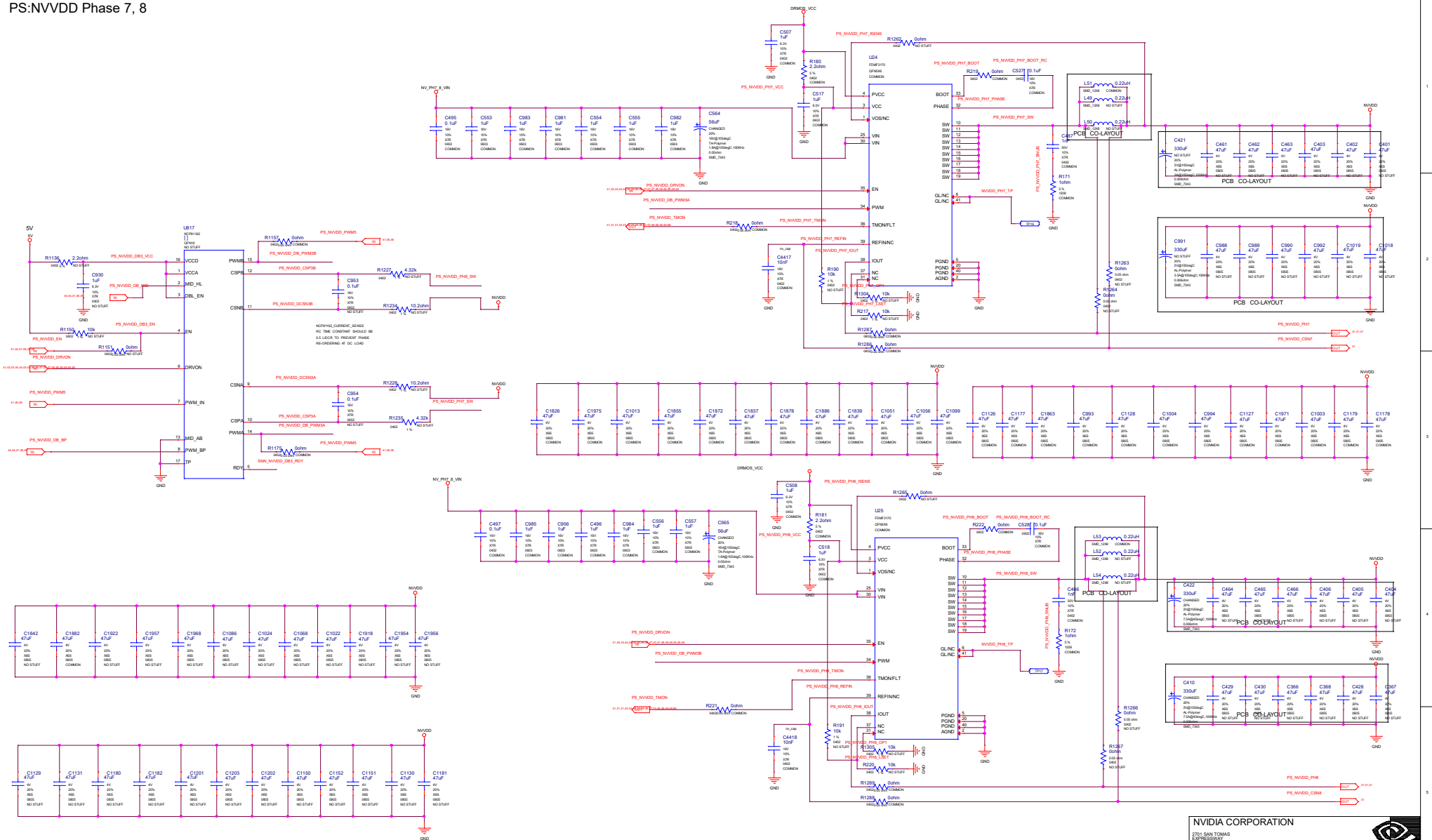
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NV_PN	600-1G150-BASE-403		
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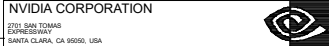


## PS:NVVDD Phase 7, 8



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ASSEMBLY	"ASSEMBLY_DESCRIPTION"	SANTA CLARA, CA 95050, USA
PAGE DETAIL	PS NVGG Phase 7.6	
CLAIMS		
	NV_PN	600-1G150-BASE-403
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	BOM REV	A
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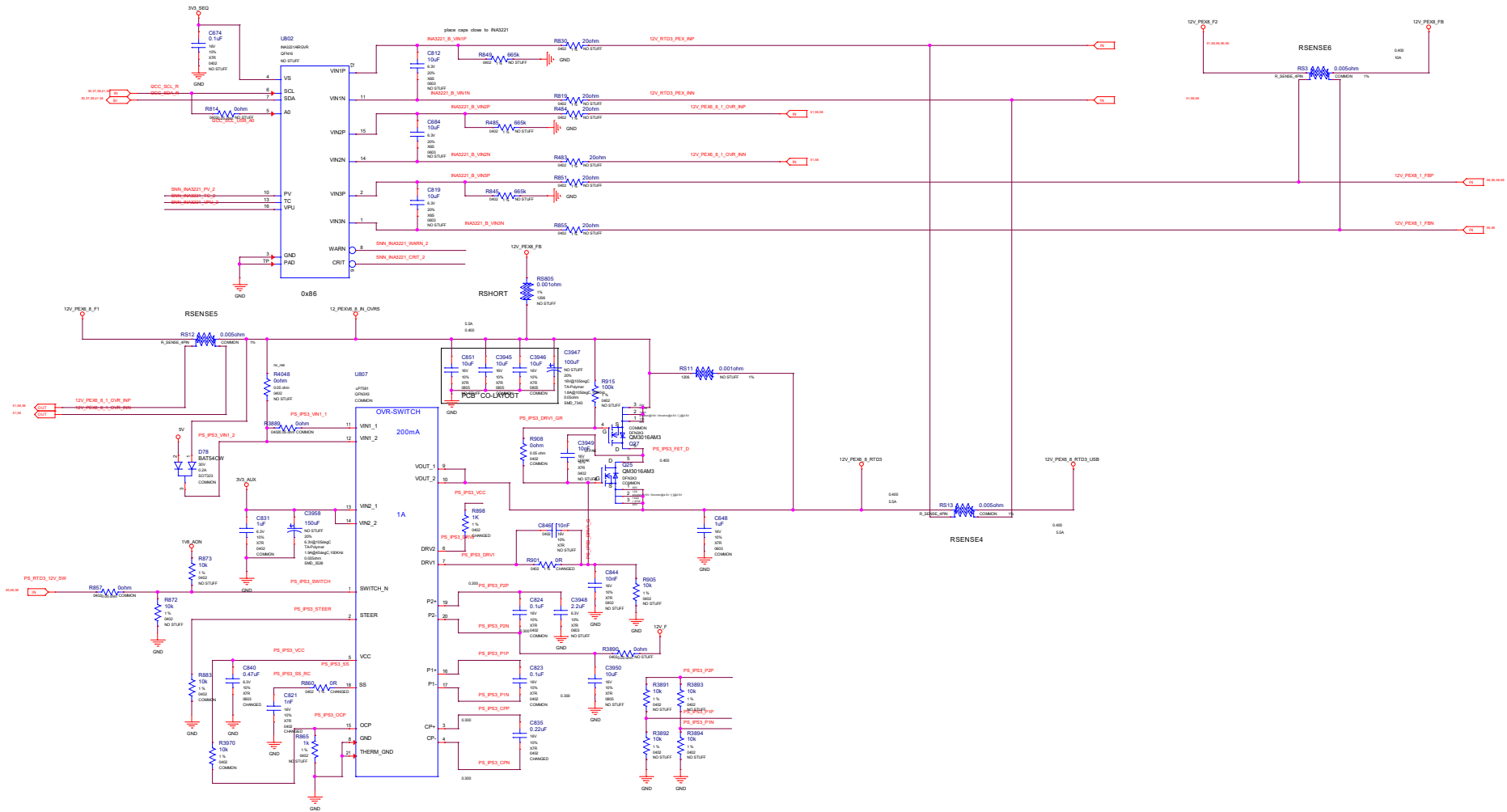
NV_PN	600-1G150-BASE-403		
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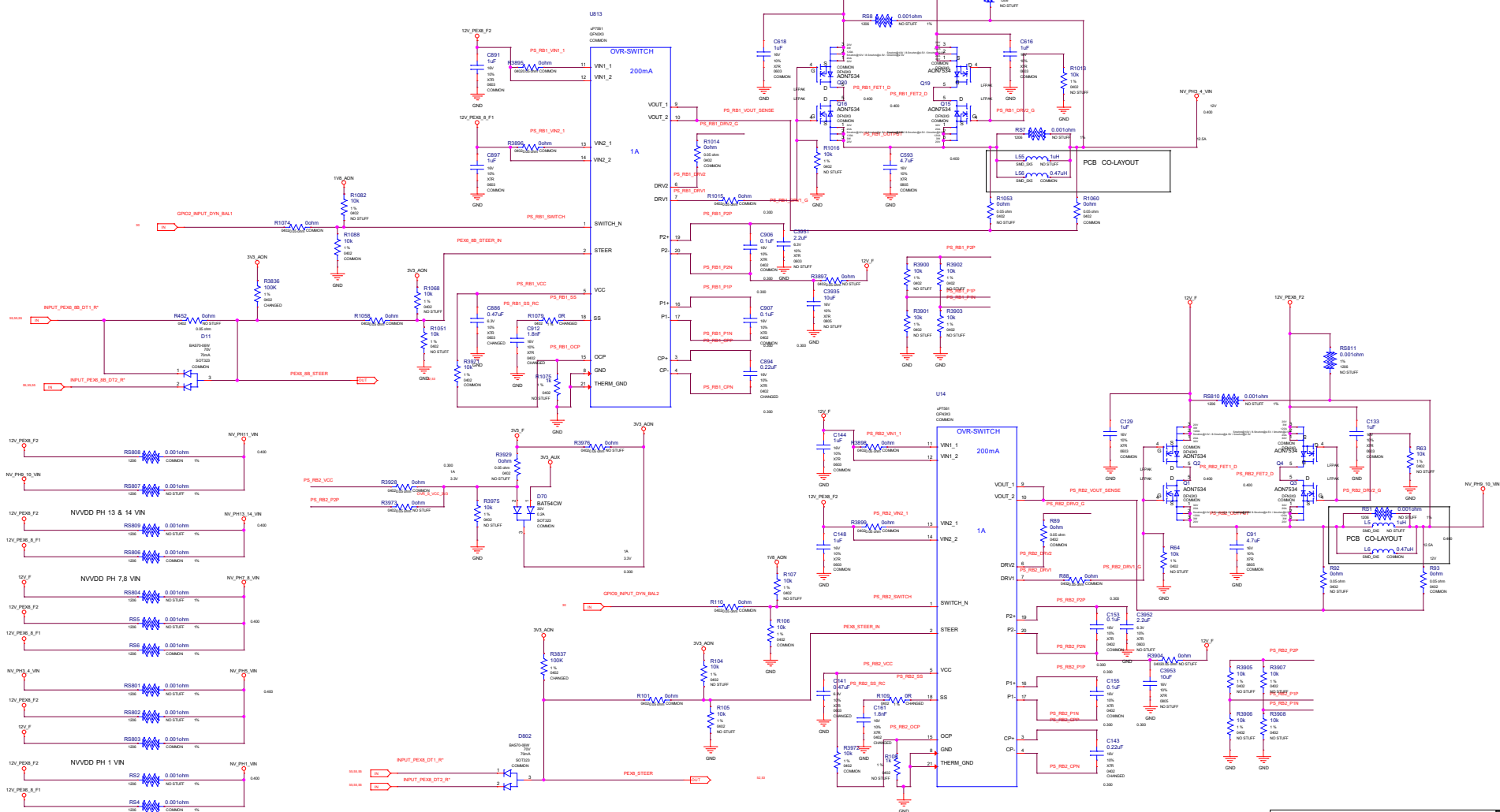



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ASSEMBLY	<ASSEMBLY _ DESCRIPTION>
PAGE DETAIL	PS: INPUT_SWITCH_RT03 USB

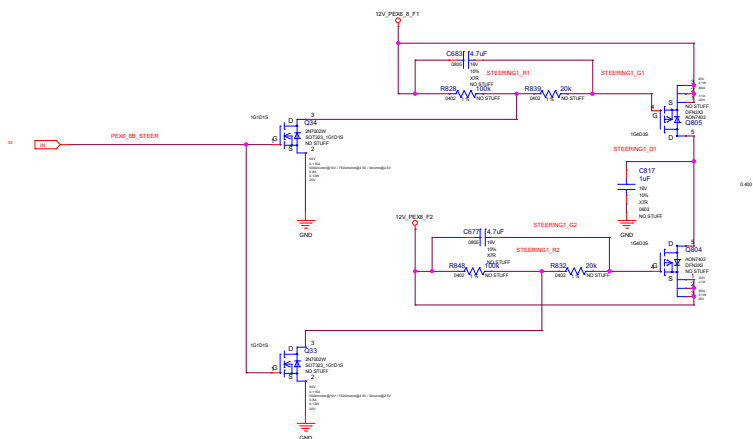
## PS: Input Switch Rail Balance



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<b>NV_PN</b>		<b>600-1G150-BASE-403</b>		
<b>PCB REV</b>	PG150-C03	<b>PAGE</b>	52 OF 66	
<b>BCM REV</b>	A	<b>DATE</b>	09-JUL-2018	

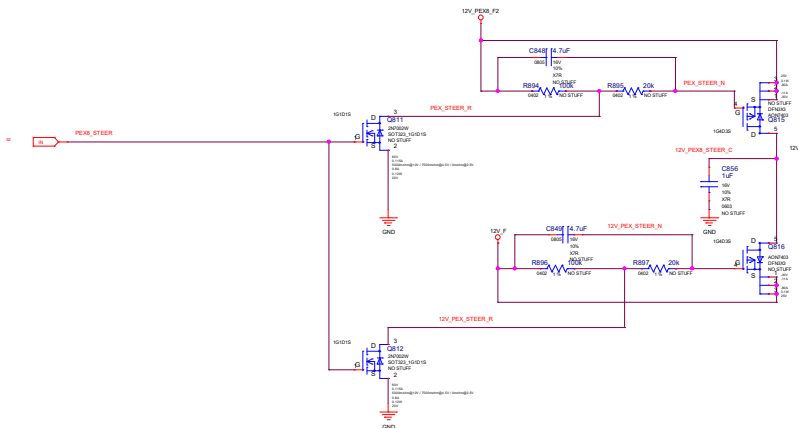
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12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



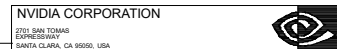
12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For Operating Type4 + Phase Doubler, 2 phase PSI mode

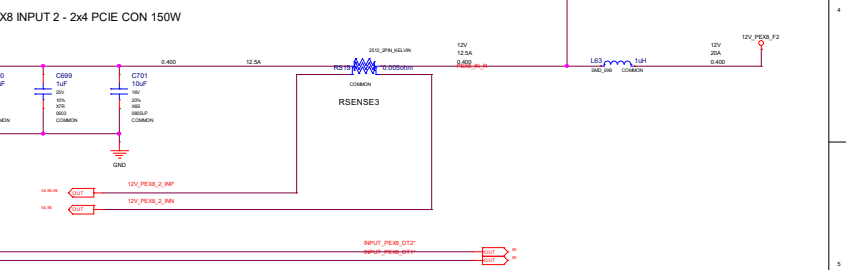
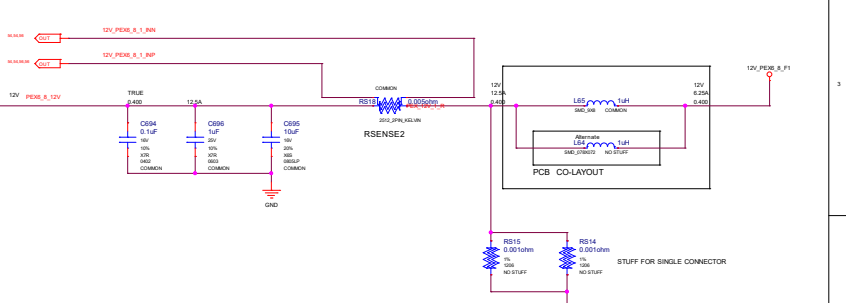
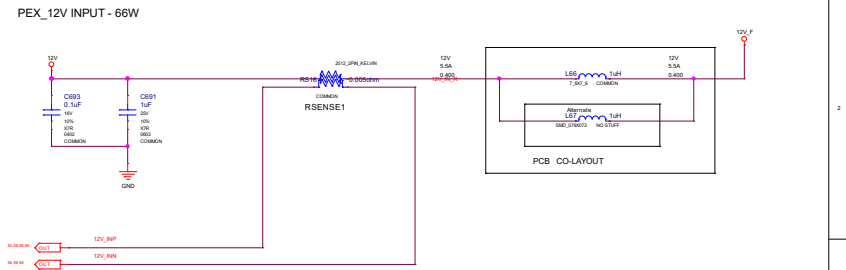
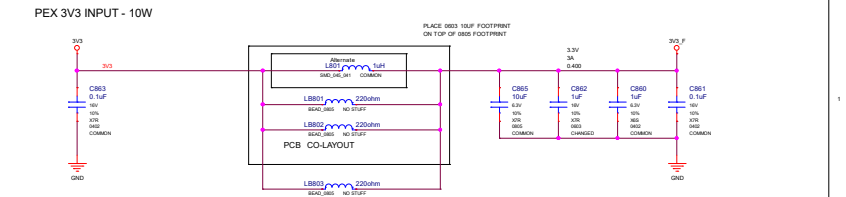
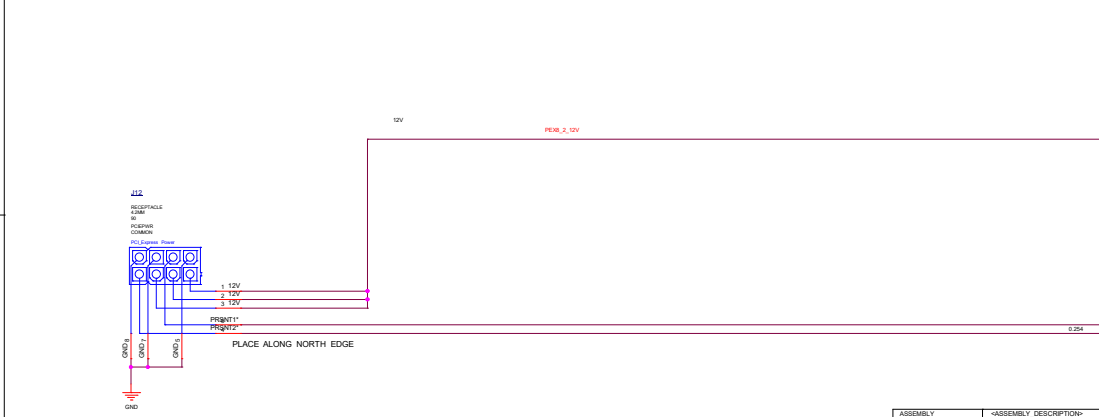
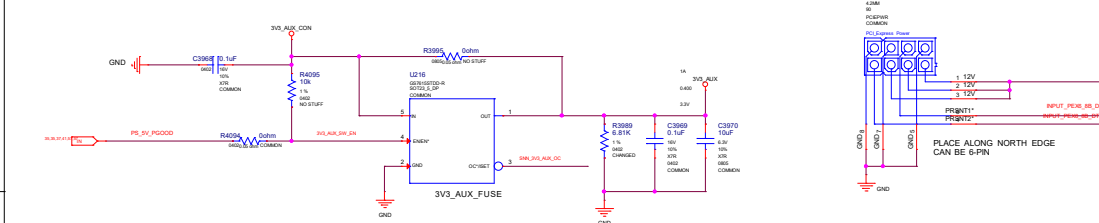
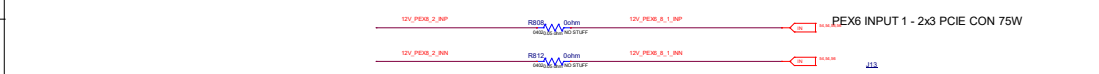
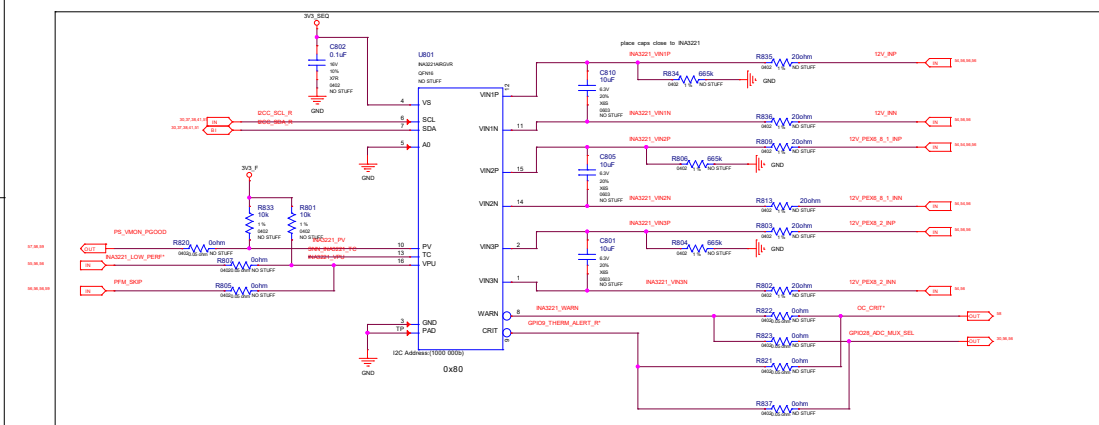



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ASSEMBLY		ASSEMBLY DESCRIPTION	
PCB DETAIL		PSI: DISCRETE STEERING	
NV_PN		600-1G150-BASE-403	
PCB REV		PG150-C03	
BOM REV		A	
PAGE		83 OF 86	
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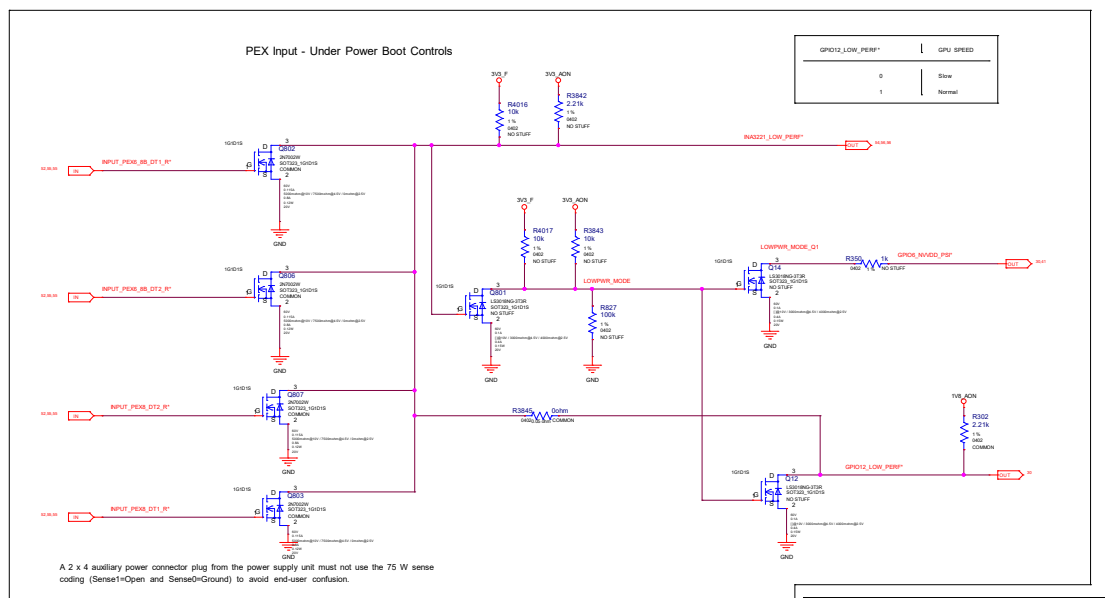
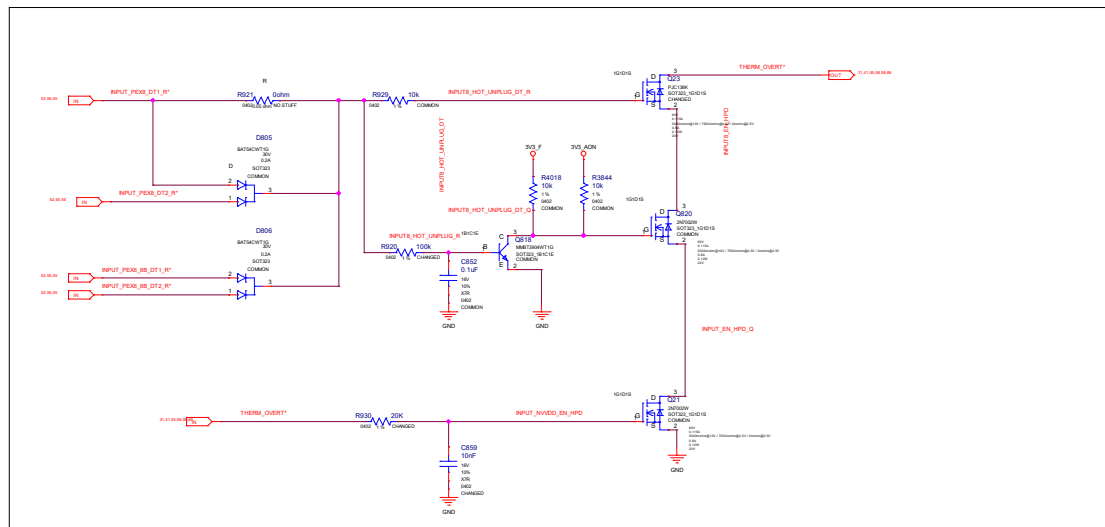
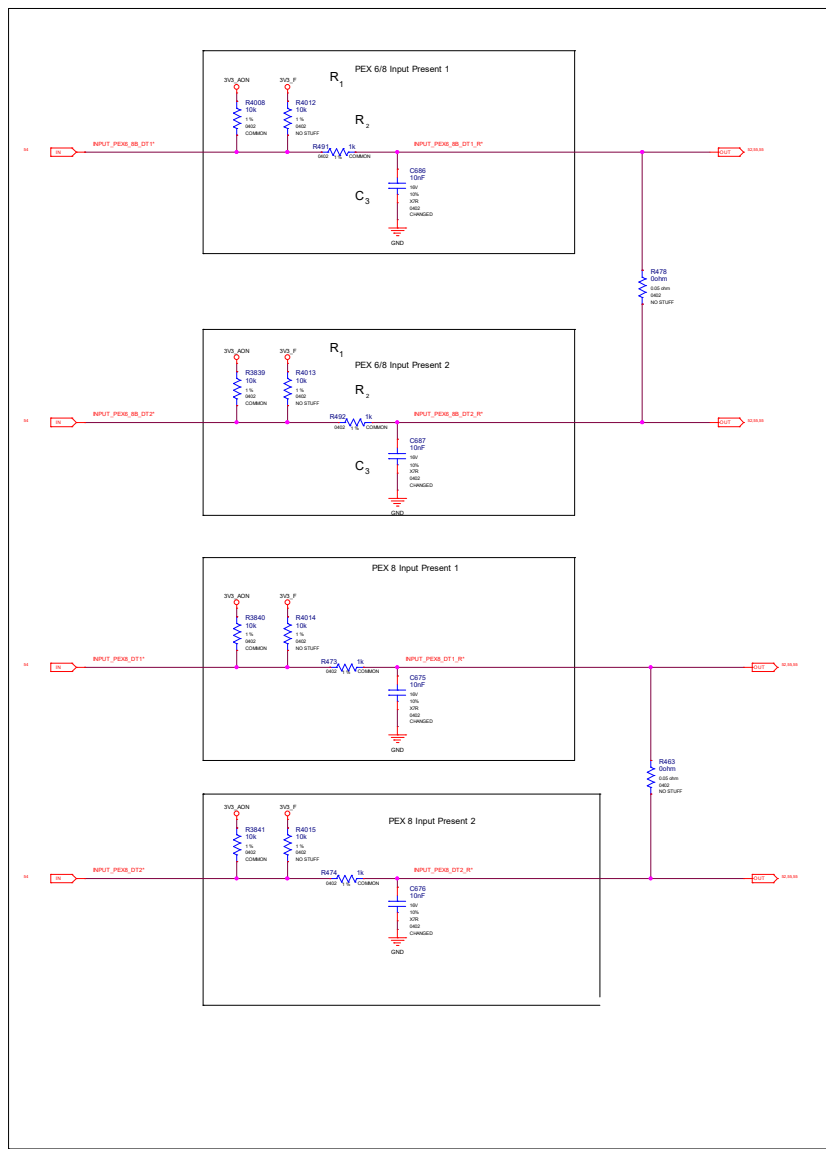
## PS: Inputs, Filtering, and Monitoring



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NV_PN		600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	54 OF 56	
BOM REV	A	DATE	09-JUL-2018	

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## PS: 12V Current Steering &amp; Hot Unplug Detect



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Current Starring, Hot Unplug

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NV_PN	600-1G150-BASE-403
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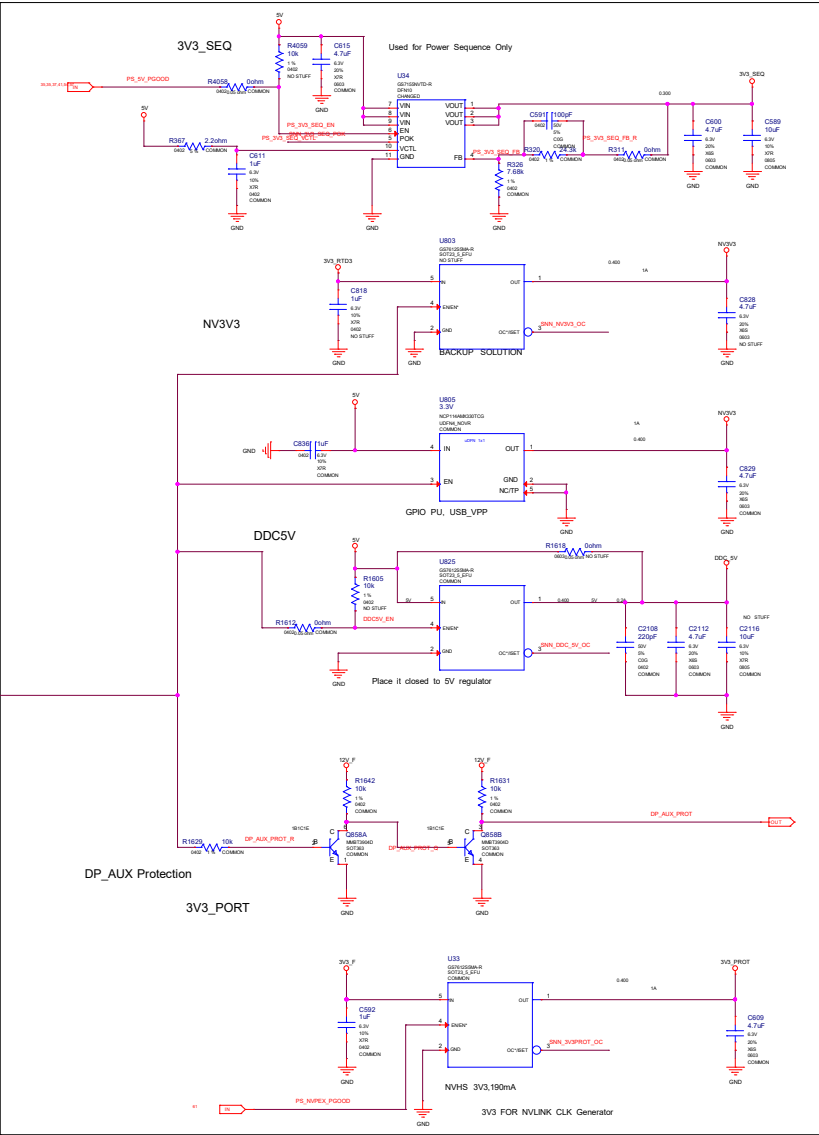
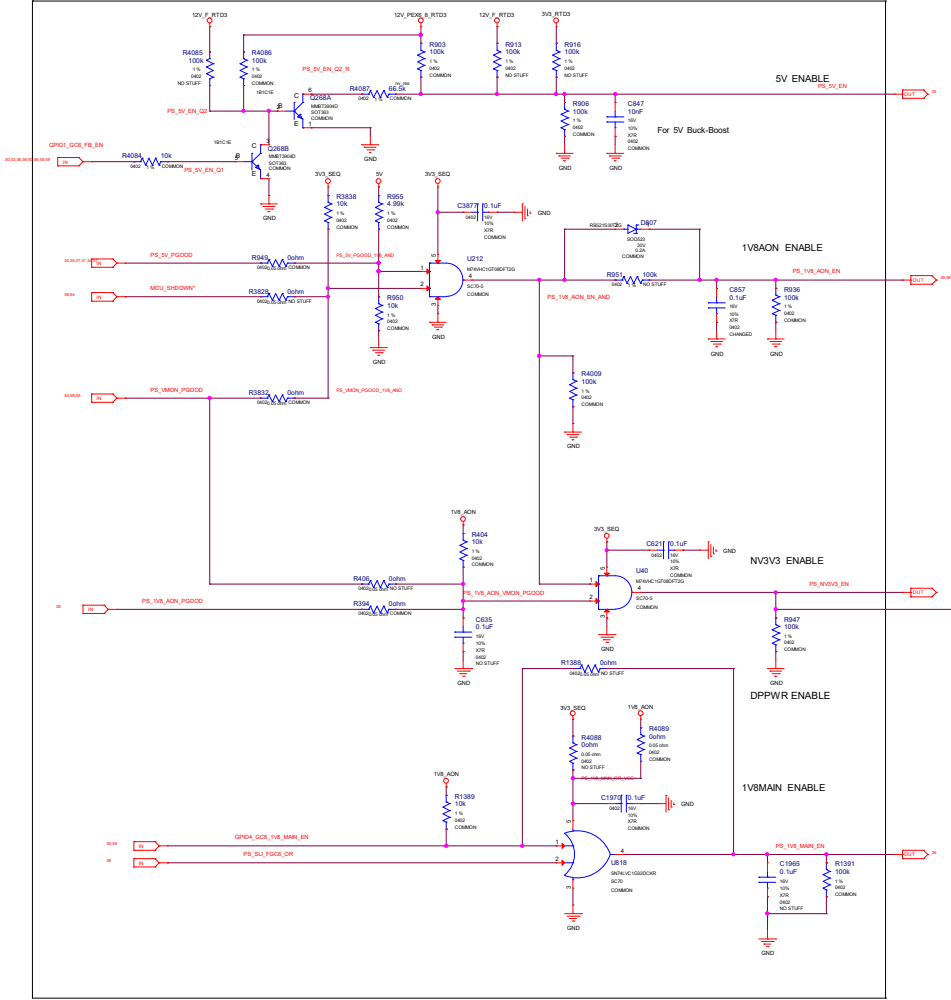
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SEQUENCE:5V,1V8,NV3V3 ENABLE



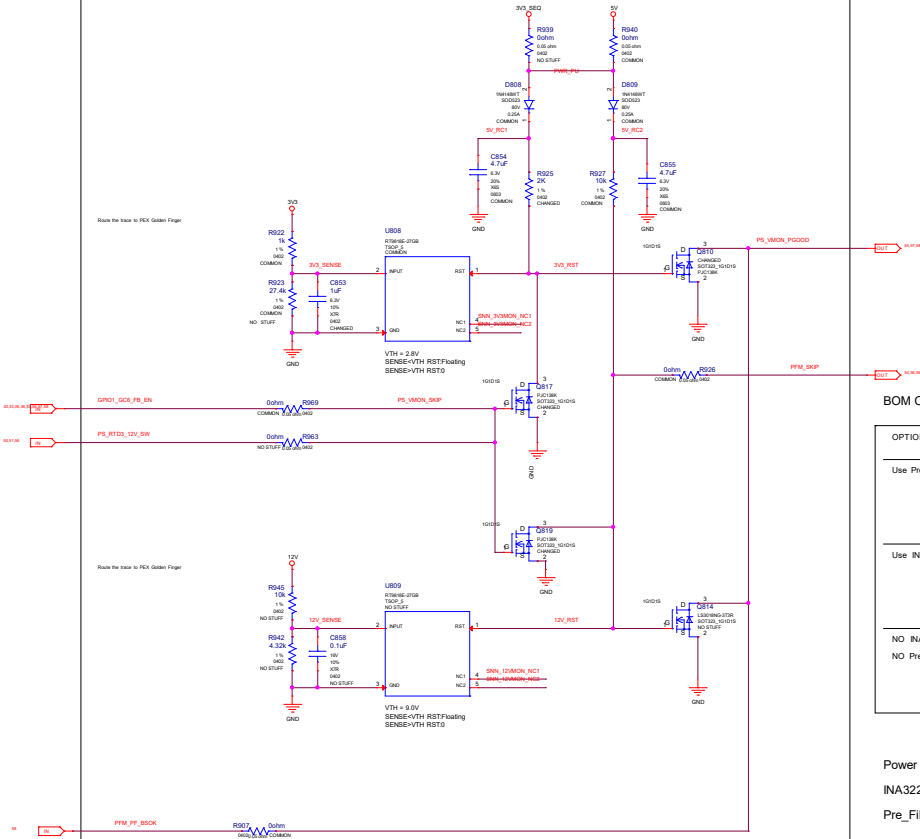
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	Sequence: 5V, 1V8, NV3V3 EN

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NV_PN	600-1G150-BASE-403		
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PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PG00D	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence.Use to Mask the VMON_PG00D
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply  
INA3221:3V3\_SEQ  
Pre\_Filter(ADC\_MUX):3V3(PEX)

Dual Pre-Filter case:  
Only use the Primary Pre-Filter to sense 3V3PEX  
and All Input 12Vs

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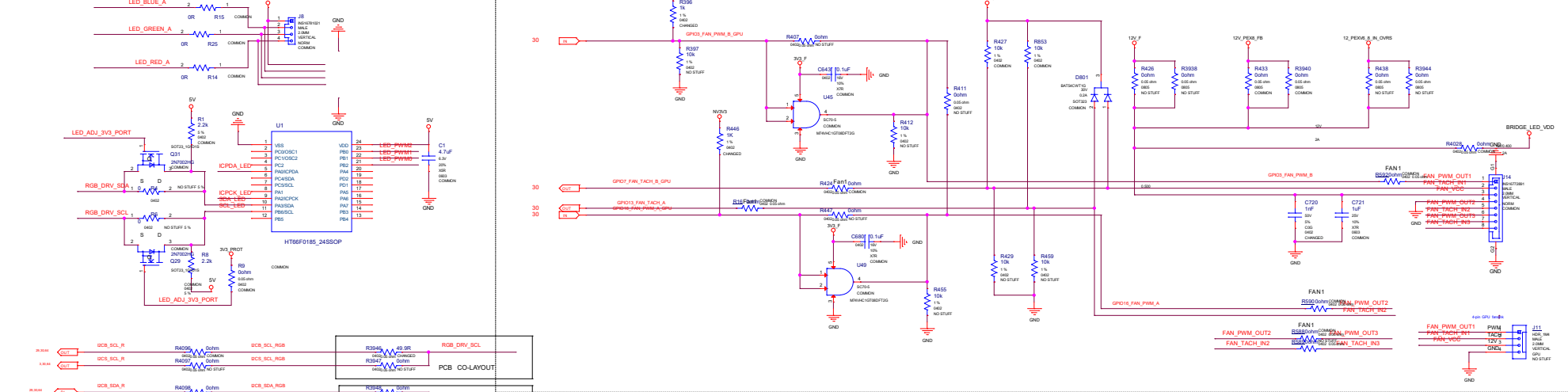


Customer Data			
A	B	C	

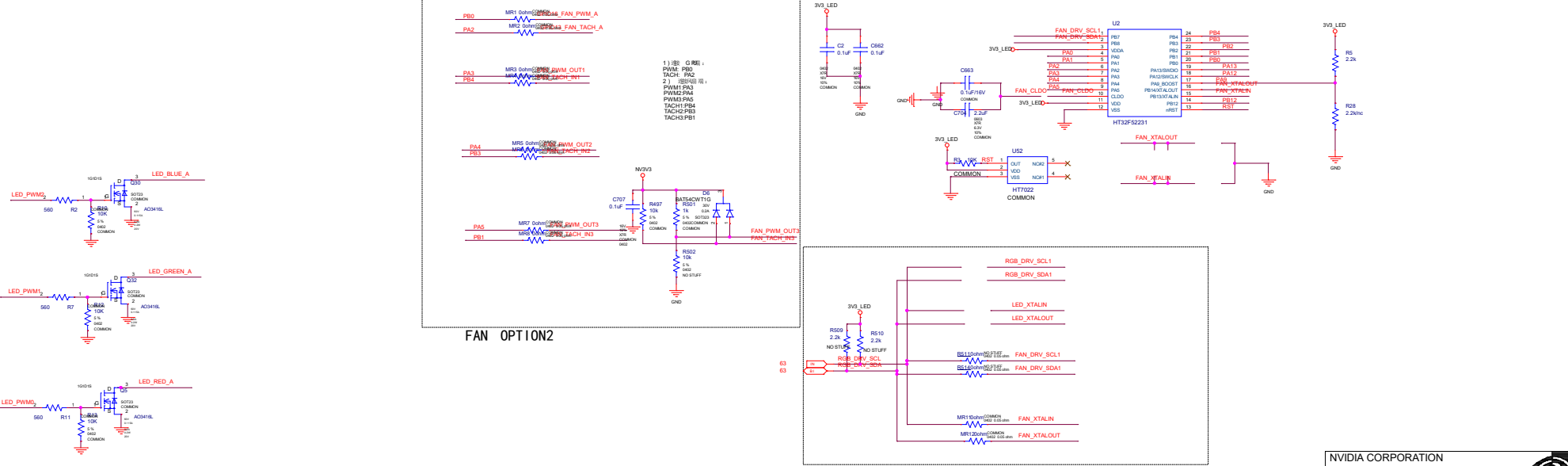


STANDARDS			
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MISC: FAN & LED1



8-bit I2C Address of MCU on Daughter Board: 0x92



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NV_PN	600-1G150-BASE-403		
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MISC: LED2

SCDS\_MAKESLED\_HEADER\_P18\_ASSIGNMENT\_NEW.png00000404

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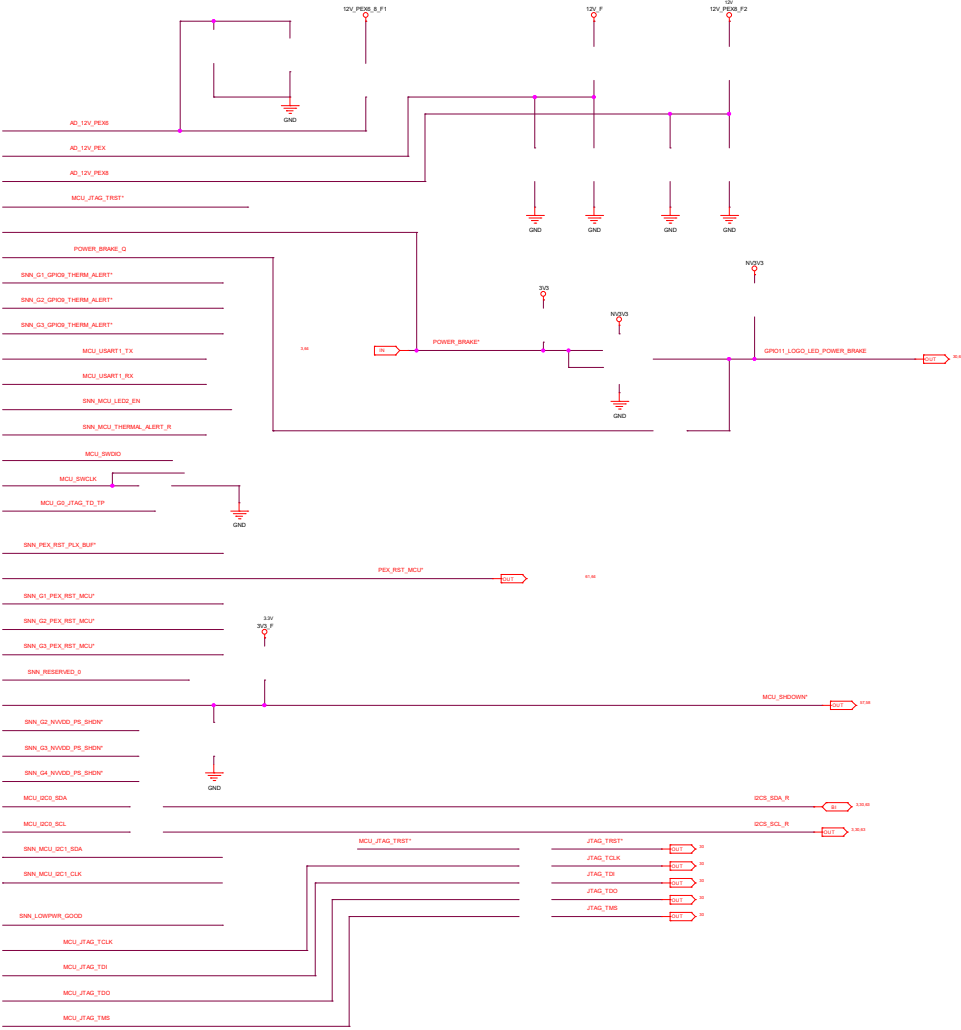
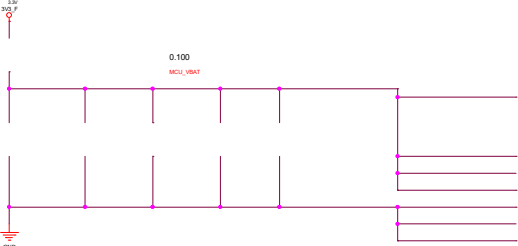
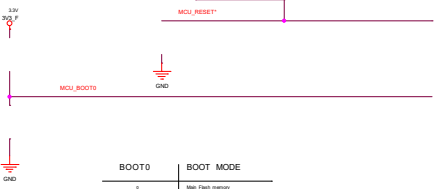
ASSEMBLY	"ASSEMBLY" DESCRIPTION		
PRICE DETAIL	MISC: LED 2		
NV_PN		600-1G150-BASE-403	
PCB REV	PG150-C03		PAGE 83 OF 86
BOM REV	A		DATE 09-JUL-2018

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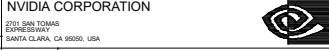


ZERO IDLE POWER MCU



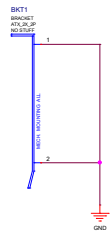
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ASSEMBLY		ASSEMBLY DESCRIPTION	
PCB DETAIL		MCU ZERO POWER	
NV_PN		600-1G150-BASE-403	
PCB REV		PG150-C03	
BOM REV		A	
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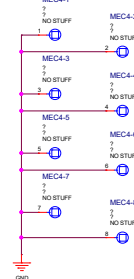
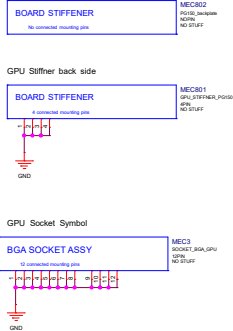





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**MEC1**  
PHI-MD-SHA-XYNMM-SCREW  
STD  
NO STUFF  
  
new LF screw -155-0001-000  
RCHG screw -154-0003-700



ASSEMBLY		-ASSEMBLY DESCRIPTION-	SANTA CLARA, CA 95050, USA				
PAGE DETAIL		MECH					
DISCLAIMS			NV_PN		600-1G150-BASE-403		
y			PCB REV		PG150-C03	PAGE	05 OF 06
			REV		A	DATE	09-JUL-2018

