

GA102 DT SKU P-BOARD

350W, FH Std PCB, 384b, GDDR6X x8

DP + DP + DP + HDMI/DP

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4501 SAN TOME DRIVE

SAN JOSE, CA 95134

NAI_PFE 600-1G132-BASE-400

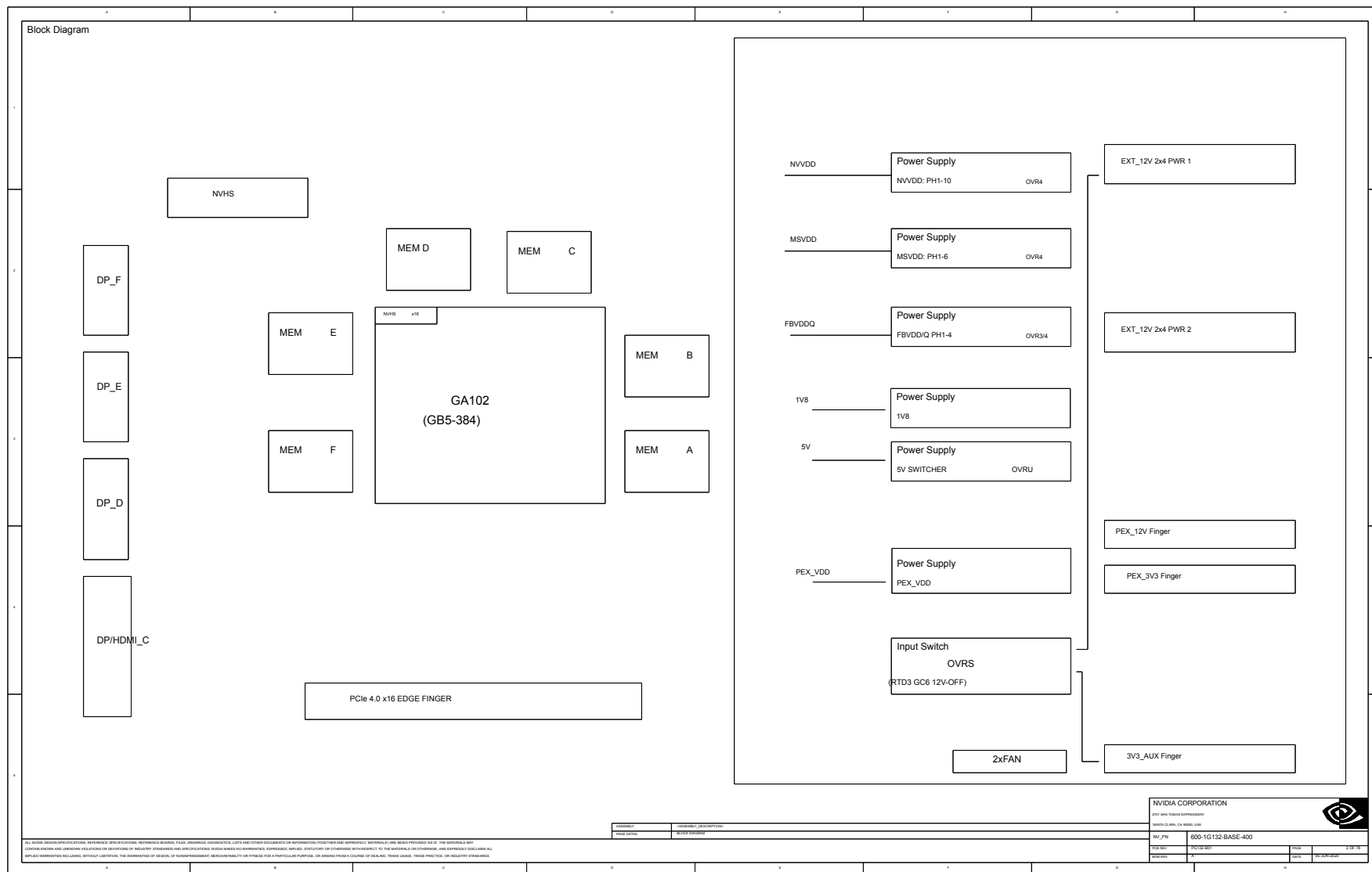
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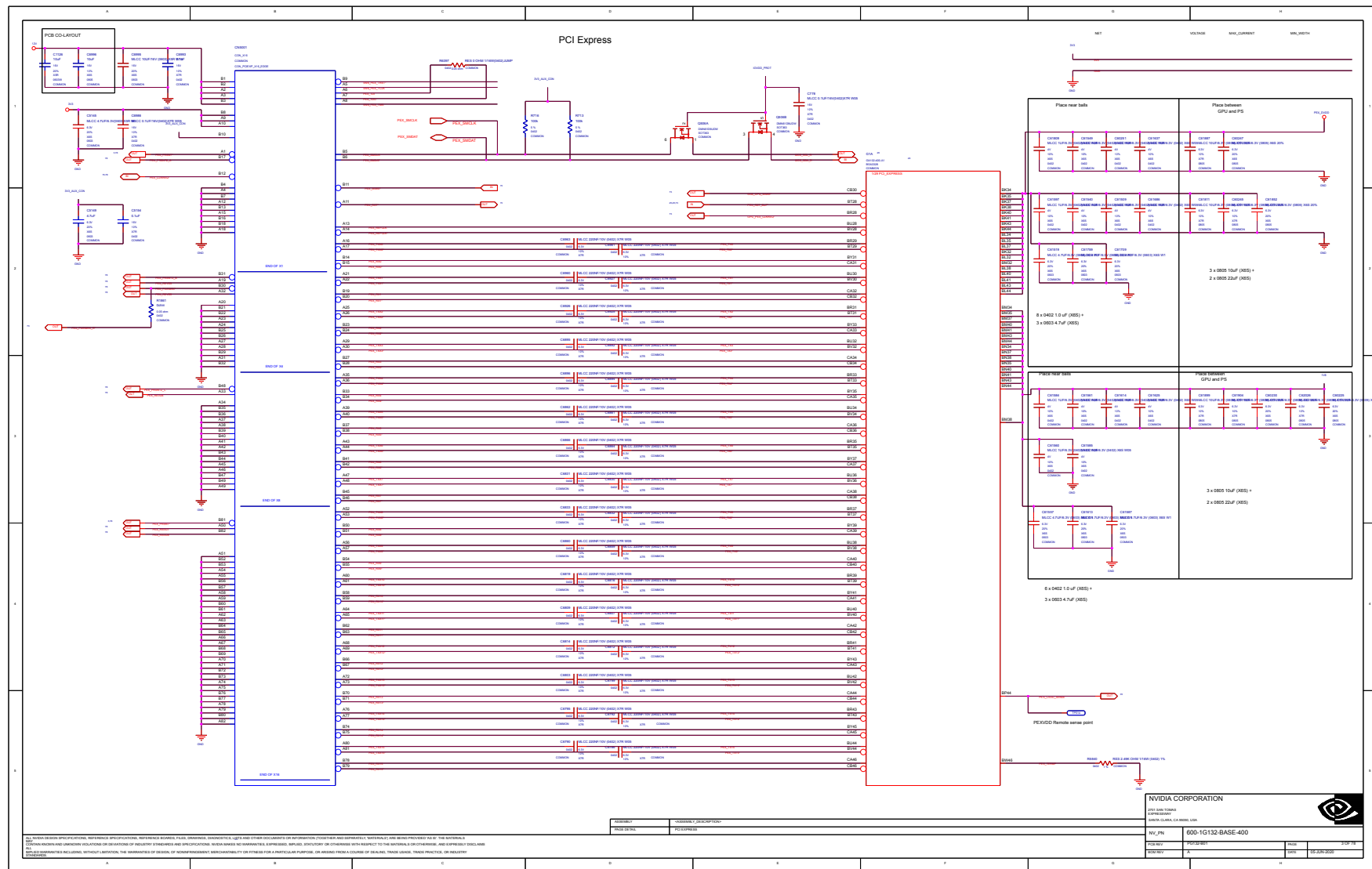
REV 001

DATE 10-20-2020

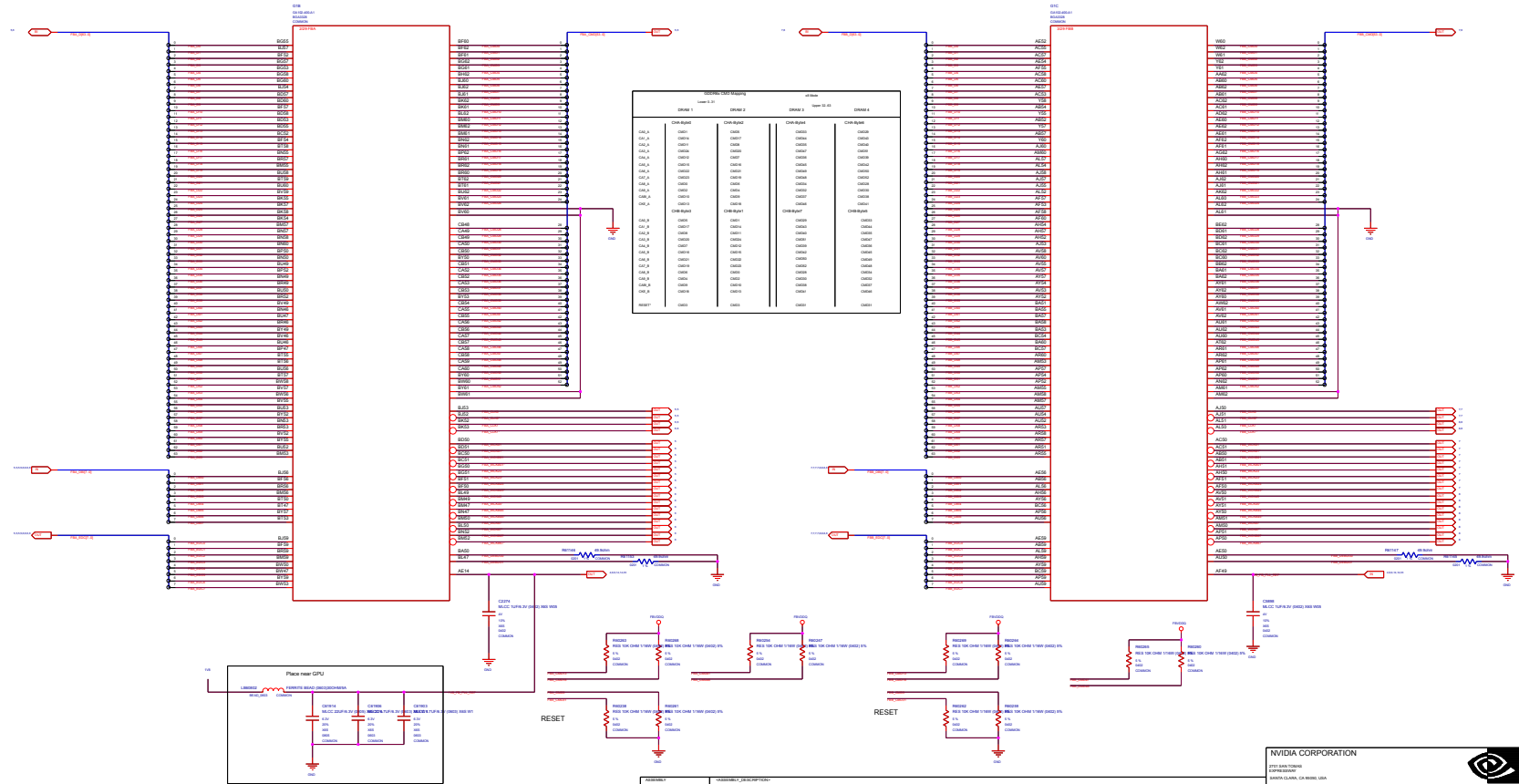


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MEMORY: GPU Partition A/B



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2707 SATOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA	
NV_P/N	600-1G132-BASE-400

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SOM REV	A	DATE	05-JUN-2020

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Figure 1 is a schematic diagram of a 100-MHz PLL circuit. The circuit includes a PLL IC (CDR600) with various pins connected to a 100-MHz reference oscillator (CDR600), a 100-MHz reference oscillator (CDR600), and a 100-MHz reference oscillator (CDR600). The circuit also includes a 100-MHz reference oscillator (CDR600) and a 100-MHz reference oscillator (CDR600). The circuit is powered by a 1.5V supply and a 1.5V supply. The circuit is labeled "100-MHz PLL" and "100-MHz PLL".

The diagram illustrates the timing of various signals for the 10.80MHz channel. It is divided into two main sections: 'NORMAL' and 'SWAPPED', each showing a sequence of signals and their corresponding pin numbers.

10.80MHz Channel Signals:

- Normal Signals:**
 - 10.80MHz (A2)
 - 10.80MHz (A3)
 - 10.80MHz (A4)
 - 10.80MHz (A5)
 - 10.80MHz (A6)
 - 10.80MHz (A7)
 - 10.80MHz (A8)
 - 10.80MHz (A9)
 - 10.80MHz (A10)
 - 10.80MHz (A11)
 - 10.80MHz (A12)
 - 10.80MHz (A13)
 - 10.80MHz (A14)
 - 10.80MHz (A15)
 - 10.80MHz (A16)
 - 10.80MHz (A17)
 - 10.80MHz (A18)
 - 10.80MHz (A19)
 - 10.80MHz (A20)
 - 10.80MHz (A21)
 - 10.80MHz (A22)
 - 10.80MHz (A23)
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 - 10.80MHz (A38)
 - 10.80MHz (A39)
 - 10.80MHz (A40)
 - 10.80MHz (A41)
 - 10.80MHz (A42)
 - 10.80MHz (A43)
 - 10.80MHz (A44)
 - 10.80MHz (A45)
 - 10.80MHz (A46)
 - 10.80MHz (A47)
 - 10.80MHz (A48)
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 - 10.80MHz (A63)
 - 10.80MHz (A64)
 - 10.80MHz (A65)
 - 10.80MHz (A66)
 - 10.80MHz (A67)
 - 10.80MHz (A68)
 - 10.80MHz (A69)
 - 10.80MHz (A70)
 - 10.80MHz (A71)
 - 10.80MHz (A72)
 - 10.80MHz (A73)
 - 10.80MHz (A74)
 - 10.80MHz (A75)
 - 10.80MHz (A76)
 - 10.80MHz (A77)
 - 10.80MHz (A78)
 - 10.80MHz (A79)
 - 10.80MHz (A80)
 - 10.80MHz (A81)
 - 10.80MHz (A82)
 - 10.80MHz (A83)
 - 10.80MHz (A84)
 - 10.80MHz (A85)
 - 10.80MHz (A86)
 - 10.80MHz (A87)
 - 10.80MHz (A88)
 - 10.80MHz (A89)
 - 10.80MHz (A90)
 - 10.80MHz (A91)
 - 10.80MHz (A92)
 - 10.80MHz (A93)
 - 10.80MHz (A94)
 - 10.80MHz (A95)
 - 10.80MHz (A96)
 - 10.80MHz (A97)
 - 10.80MHz (A98)
 - 10.80MHz (A99)
 - 10.80MHz (A100)
- Swapped Signals:**
 - 10.80MHz (A1)
 - 10.80MHz (A2)
 - 10.80MHz (A3)
 - 10.80MHz (A4)
 - 10.80MHz (A5)
 - 10.80MHz (A6)
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 - 10.80MHz (A71)
 - 10.80MHz (A72)
 - 10.80MHz (A73)
 - 10.80MHz (A74)
 - 10.80MHz (A75)
 - 10.80MHz (A76)
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 - 10.80MHz (A89)
 - 10.80MHz (A90)
 - 10.80MHz (A91)
 - 10.80MHz (A92)
 - 10.80MHz (A93)
 - 10.80MHz (A94)
 - 10.80MHz (A95)
 - 10.80MHz (A96)
 - 10.80MHz (A97)
 - 10.80MHz (A98)
 - 10.80MHz (A99)
 - 10.80MHz (A100)

The diagram also includes a 'NORMAL' section for the 10.80MHz channel, which shows the same signals as the 'SWAPPED' section, but with the signals swapped. The 'NORMAL' section is labeled 'NORMAL' and the 'SWAPPED' section is labeled 'SWAPPED'.

The diagram illustrates the timing behavior of a 10.8GHz PLL. It is divided into two main sections: 'NORMAL' and 'UNLOCKED'.

Normal State: The PLL is locked, and the output frequency is 10.8GHz. The output signal (VCO) is shown as a periodic waveform. The output power is 10dBm. The output signal is labeled 'VCO' and '10.8GHz'.

Unlocked State: The PLL is unlocked, and the output frequency is 10.8GHz. The output signal (VCO) is shown as a periodic waveform. The output power is 10dBm. The output signal is labeled 'VCO' and '10.8GHz'.

The diagram shows the relationship between the input signals (VCO, REF, and others) and the output signal (VCO). The input signals are shown as periodic waveforms. The output signal is shown as a periodic waveform. The diagram is labeled 'NORMAL' and 'UNLOCKED'.

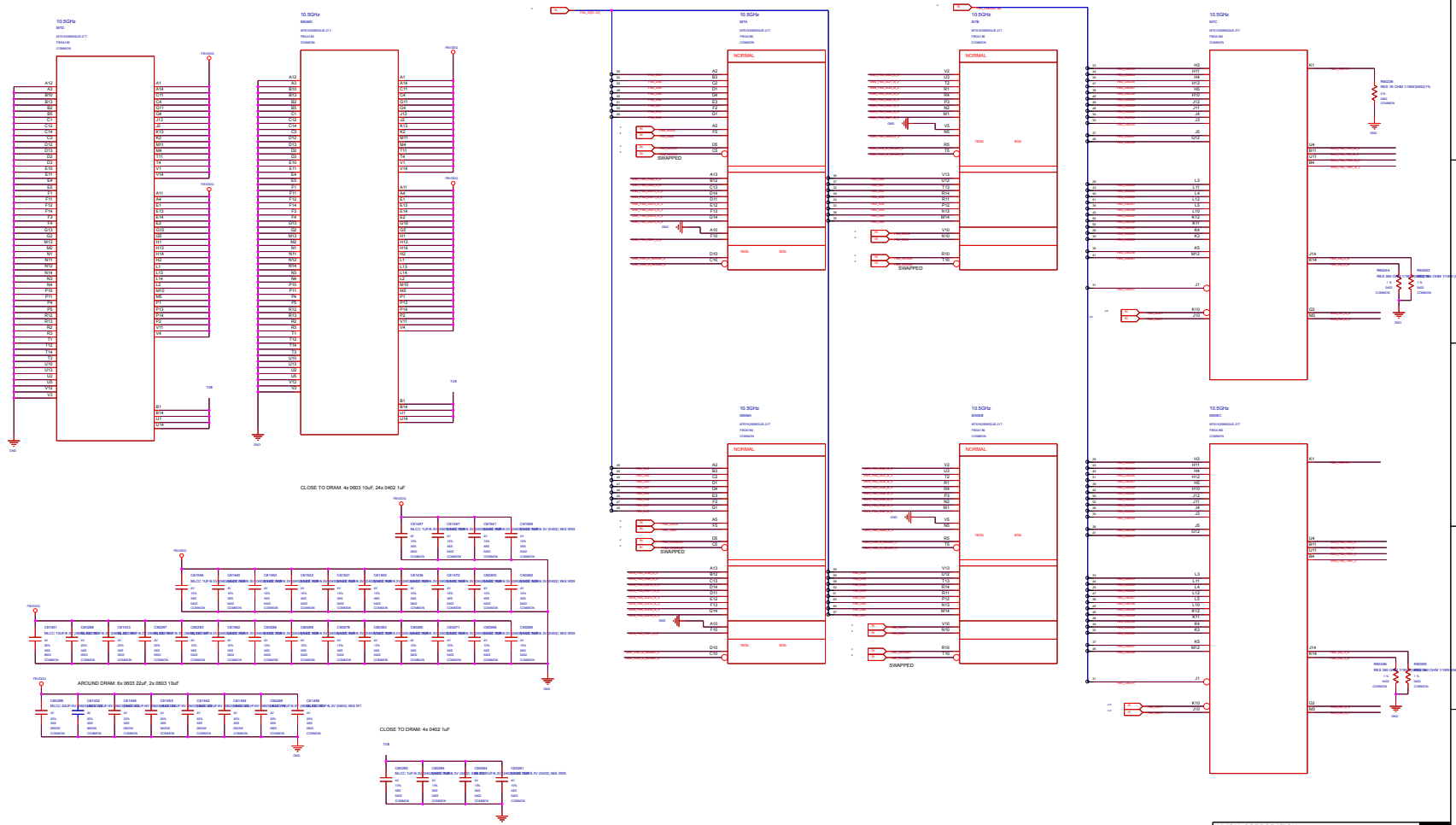
Figure 10 is a schematic diagram of a 10.5GHz receiver. The diagram shows a multi-stage receiver architecture. It starts with an input signal 'in' connected to a series of mixers and amplifiers. The first stage is a 10.5GHz receiver block. The signal then passes through a series of mixers and amplifiers, including a 10.5GHz receiver block. The final output is connected to a 10.5GHz receiver block. The diagram includes various components like mixers, amplifiers, and filters, with their respective gain and noise figures specified.

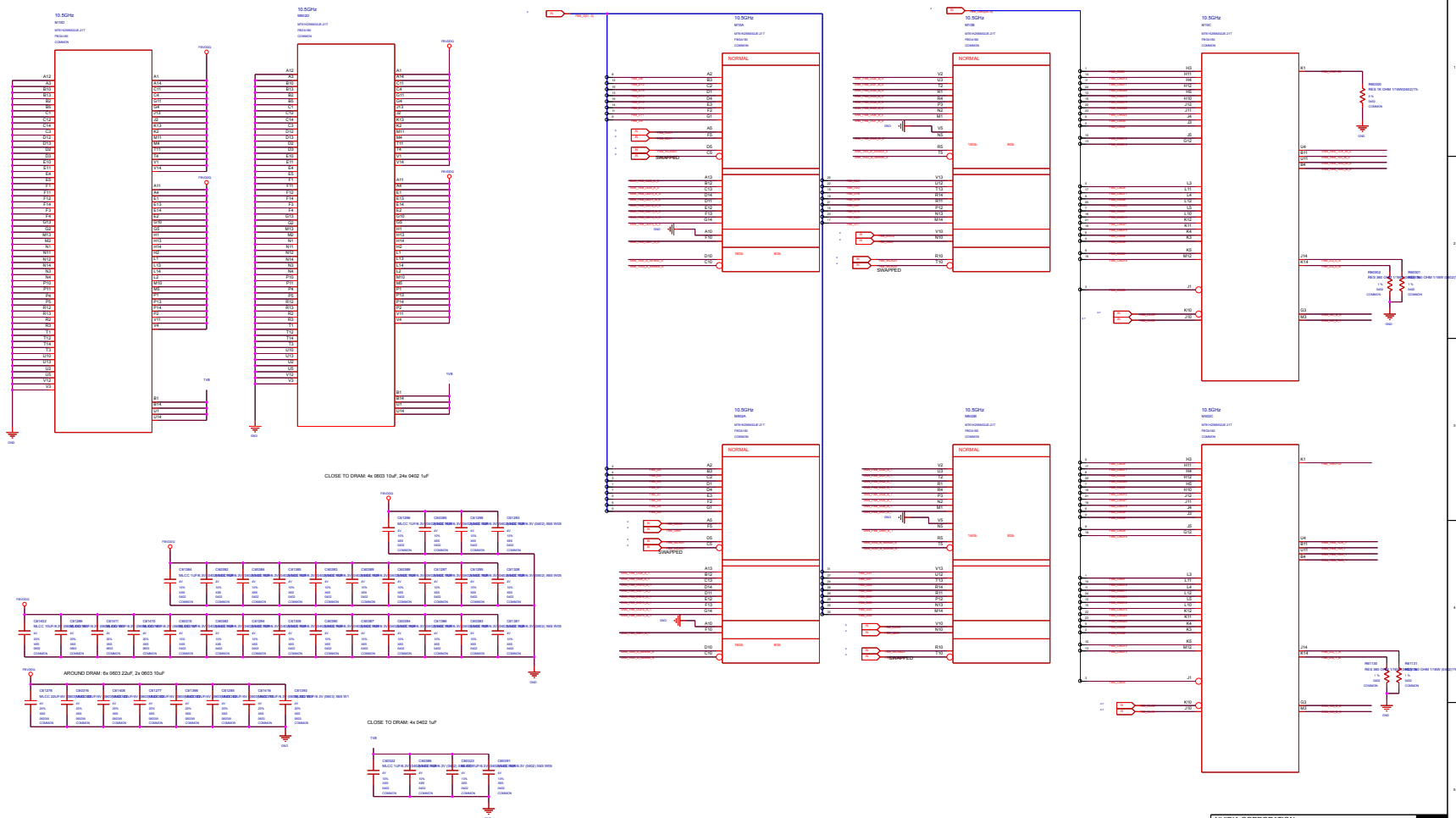
The image contains two identical circuit diagrams, one above the other, both labeled "10-SDH" at the top. Each diagram shows a large rectangular block on the left representing a module. On the right, there are two sets of connections. The top set of connections includes a terminal labeled "E1" connected to a resistor labeled "RESISTOR" with a value of "100 OHMS" and a tolerance of "1%". The bottom set of connections includes a terminal labeled "E1" connected to a resistor labeled "RESISTOR" with a value of "100 OHMS" and a tolerance of "1%". Both diagrams also show a terminal labeled "E1" connected to a resistor labeled "RESISTOR" with a value of "100 OHMS" and a tolerance of "1%". The diagrams are identical and show the same components and connections.

NV_PN	600-1G132-BASE-400
PCB REV	PG132-001
BLD REV	A



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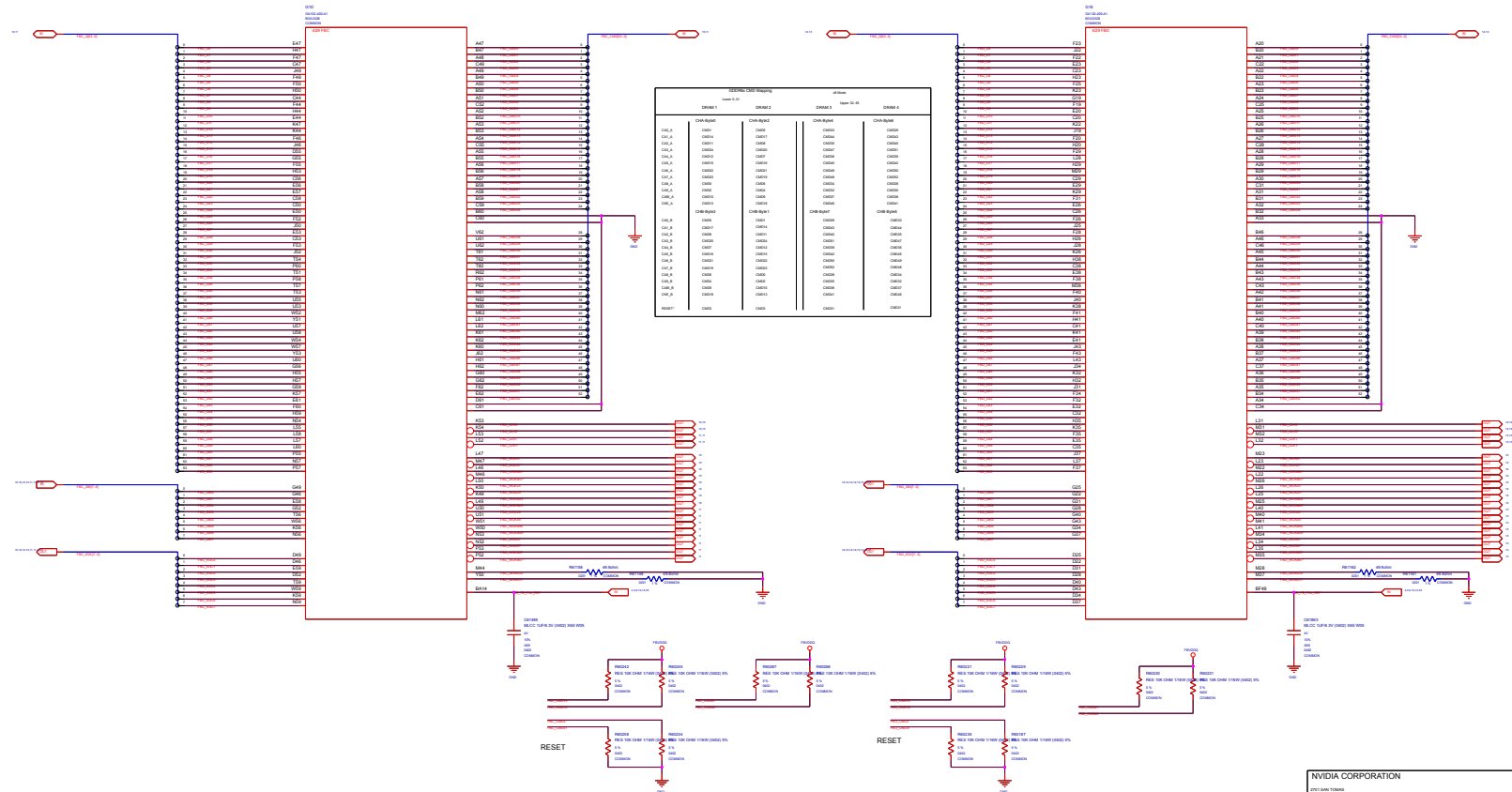
CLOSE TO DRAM

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NV_PN	600-1G132-BASE-400
PLB REV	PLG132-001
BCM REV	A



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MEMORY: GPU Partition C/D

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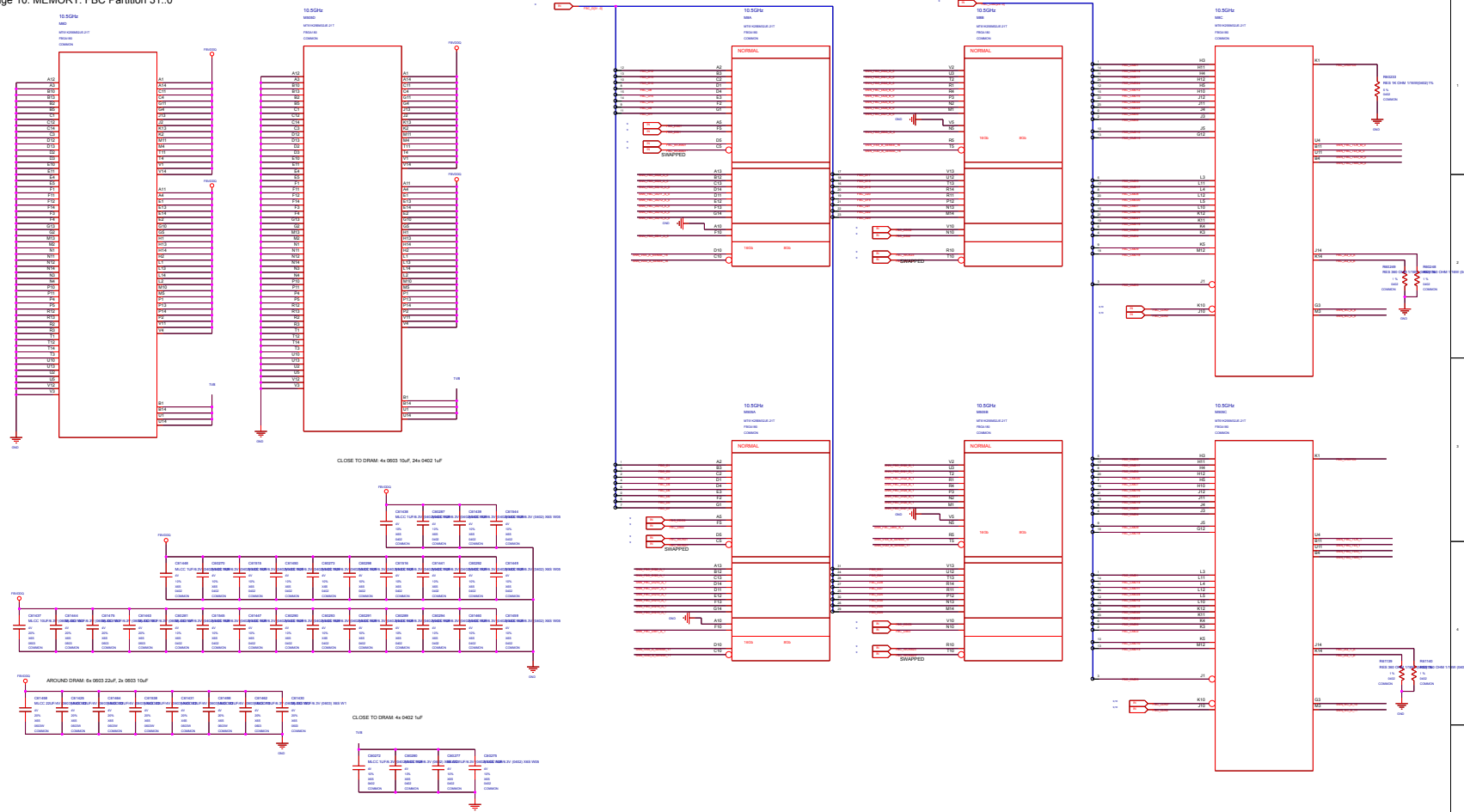
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SANTA CLARA, CA 95050, USA

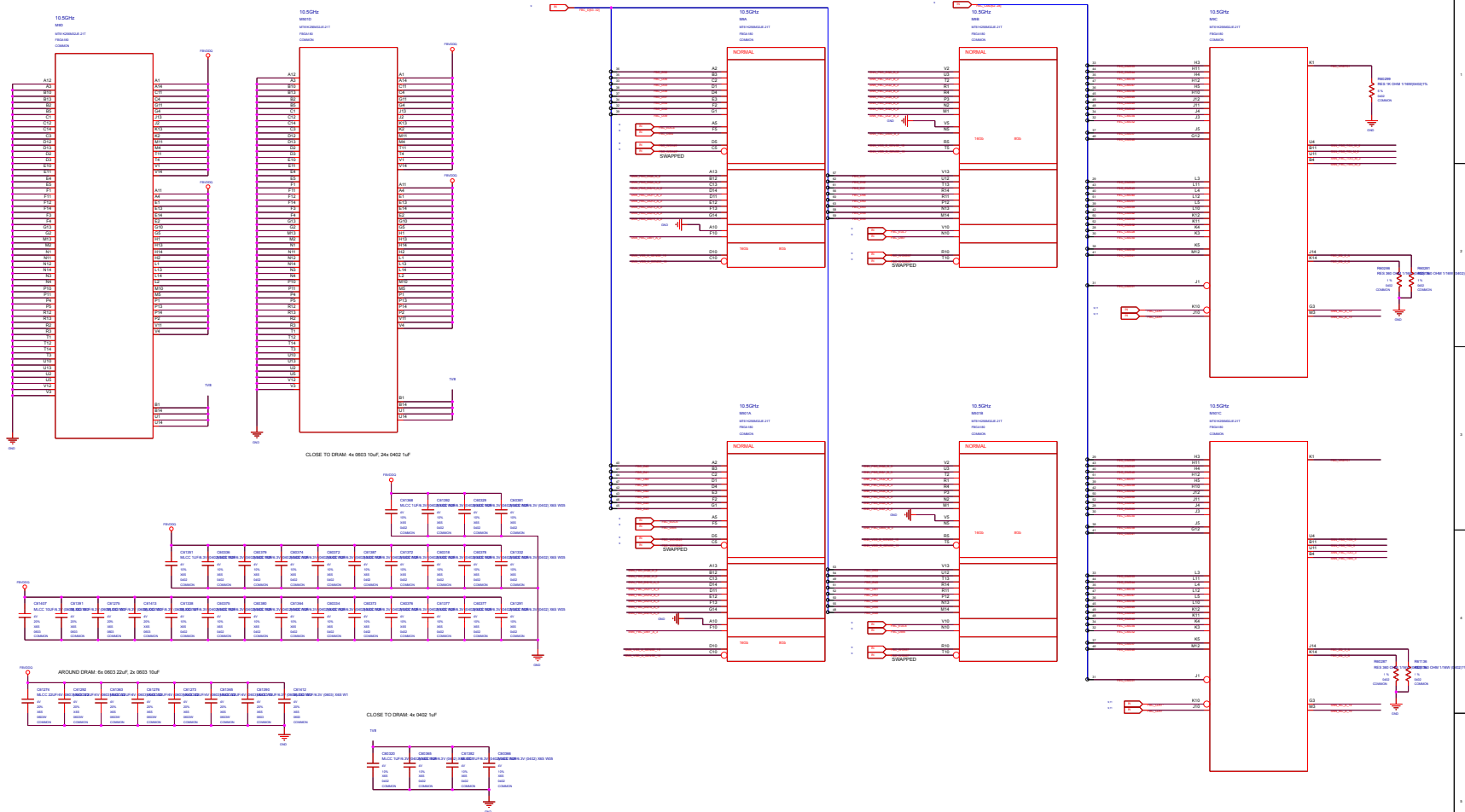


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PCB REF	DATE
PCB REF	DATE

PAGE	30
DATE	DEC 18 1990





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PART NUMBER: MEMORY FBC PARTITION 63..32

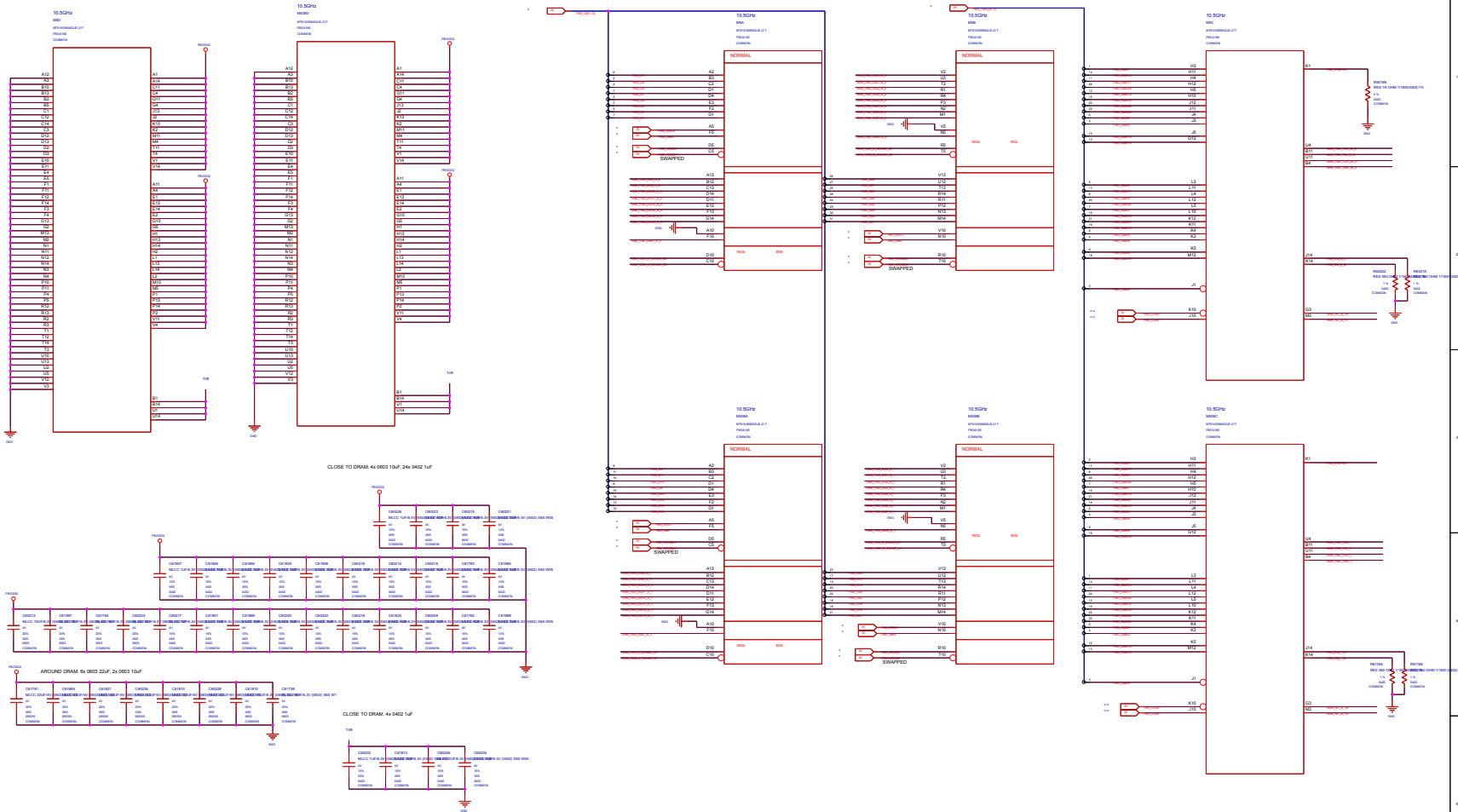
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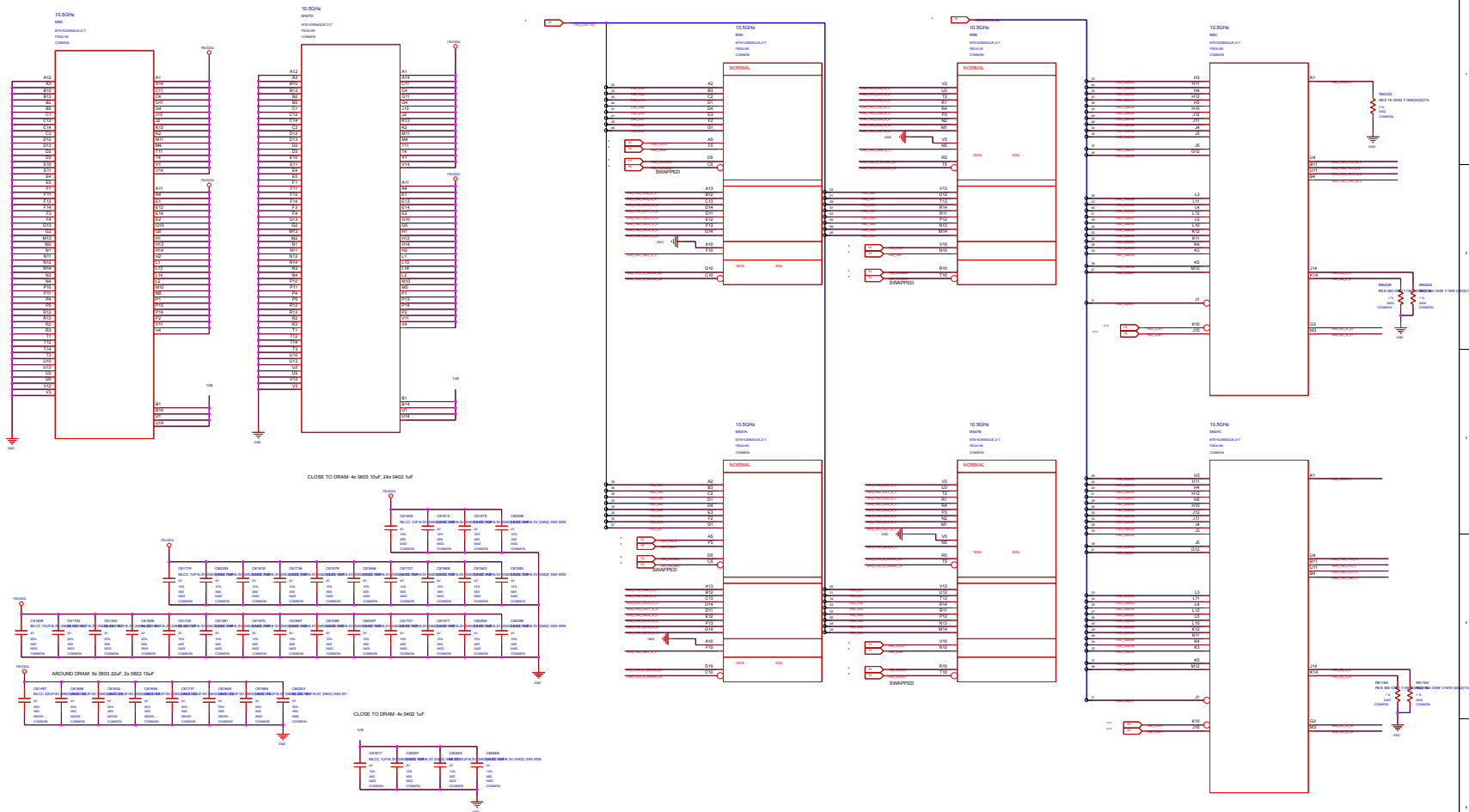
4500 RIVA TOWER
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NVIDIA CORPORATION, 4500 RIVA TOWER



WV_PN: 600-1G132-BASE-400

FIG. 1001	70102 001	DATE	11/08/18
REVISION	1	DATE	11/08/18





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DATE: 01/11/2011

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DATE: 01/11/2011

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SANTA CLARA, CA 95050, USA



600-1G132-BASE-400

REV: 1.0

DATE: 01/11/2011

DESIGN: 1.0

DATE: 01/11/2011

DESIGN: 1.0

DATE: 01/11/2011

DESIGN: 1.0

DATE: 01/11/2011

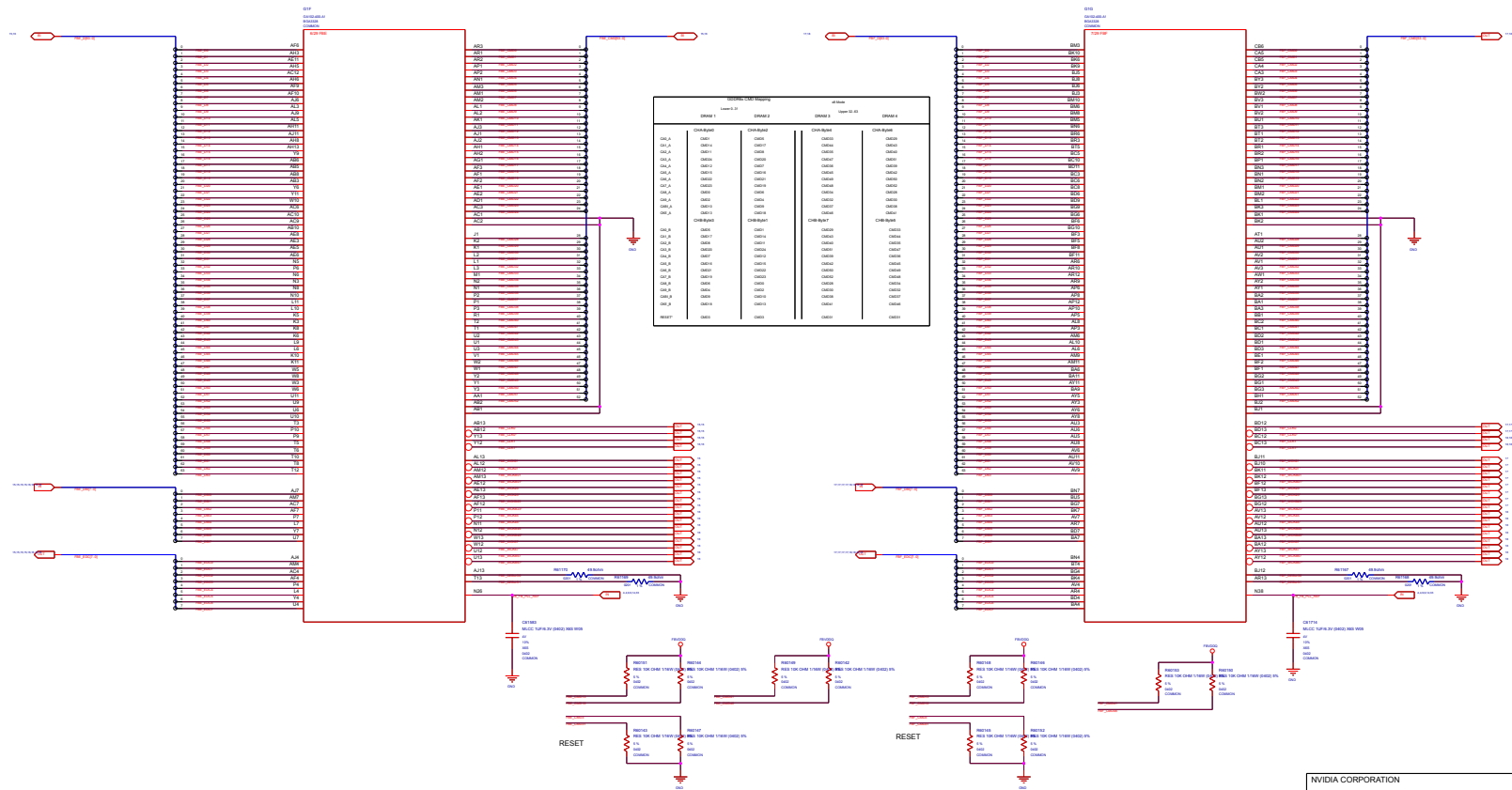
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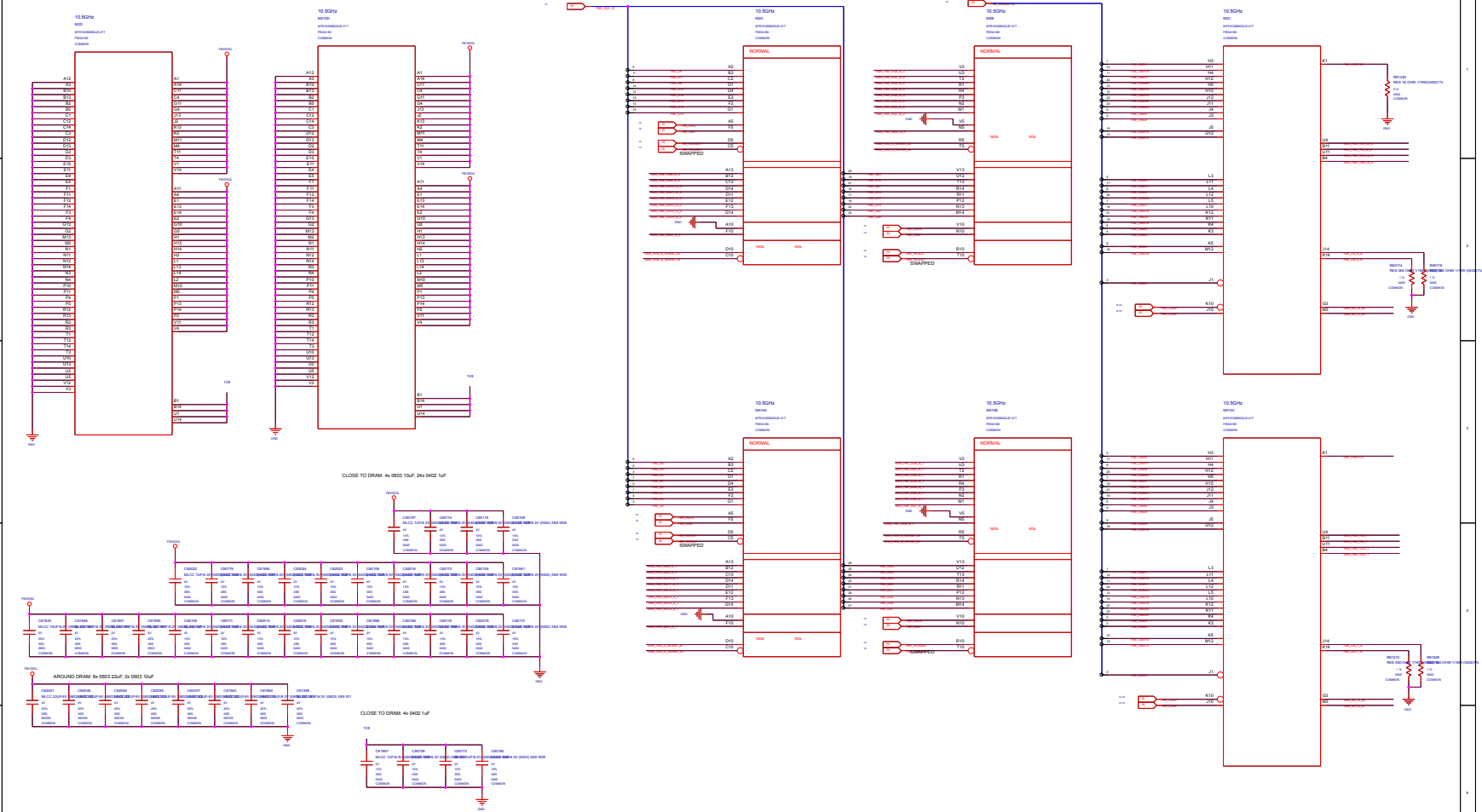
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DESIGN: 1.0

DATE: 01/11/2011

MEMORY: GPU Partition E/F





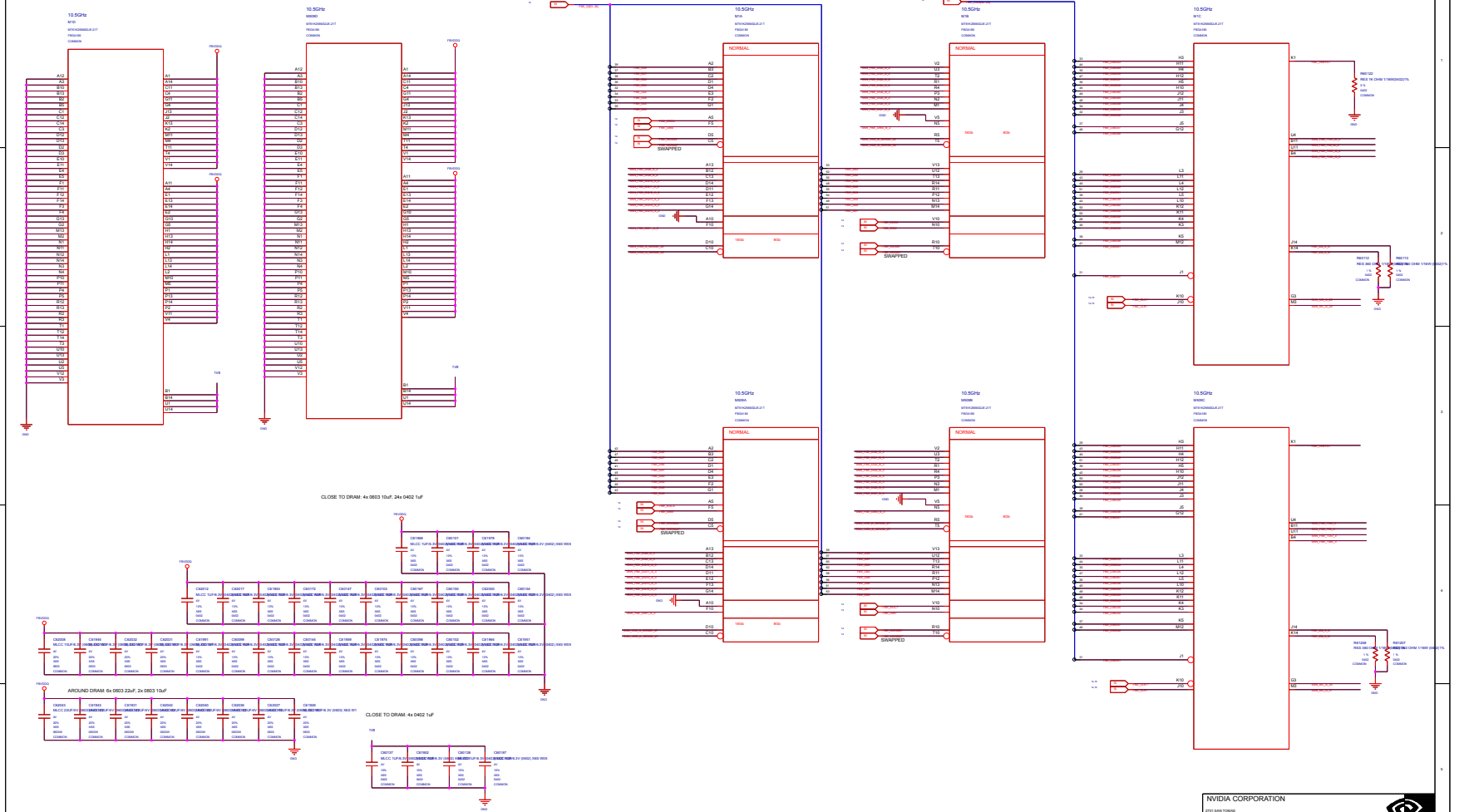
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PROD. DATE	2007-07-01 (REV. 001)

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SANTA CLARA, CA 95058 USA

REV. 001	REV. 001	DATE	10-01-06
REV. 001	REV. 001	DATE	10-01-06

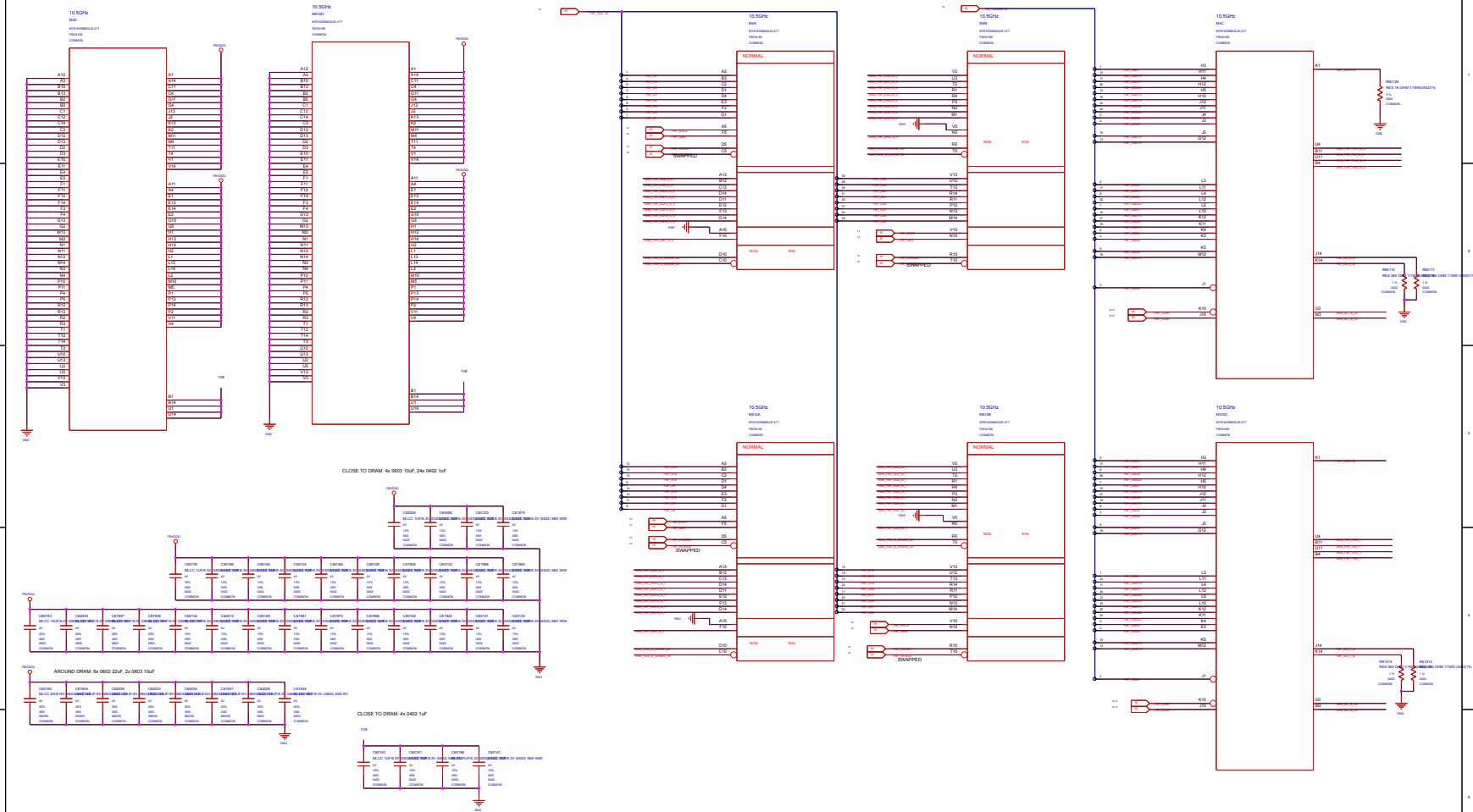
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2701 SAN TOMAS
EXPRESSWAY
SANTA CLARA, CA 95050, USA



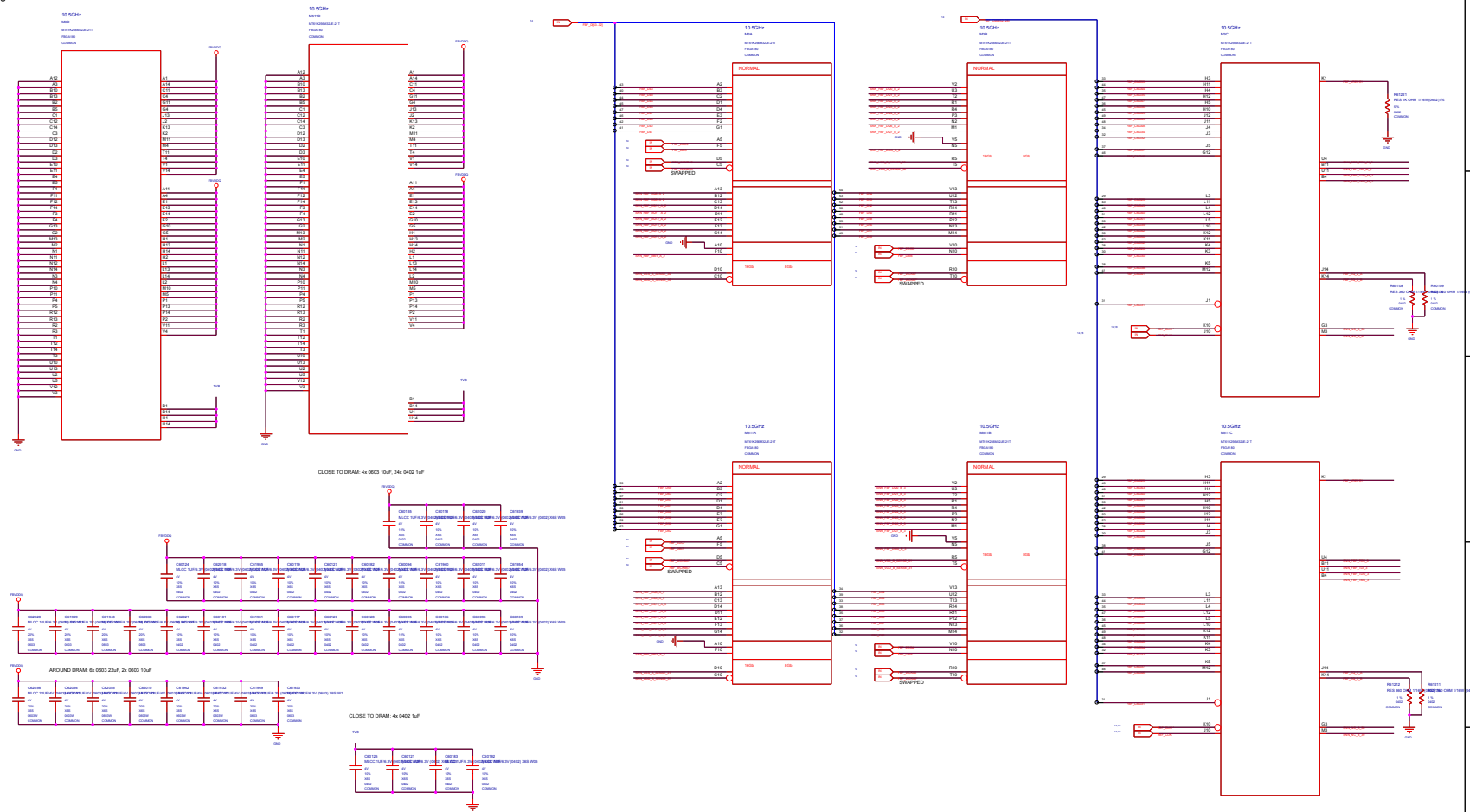
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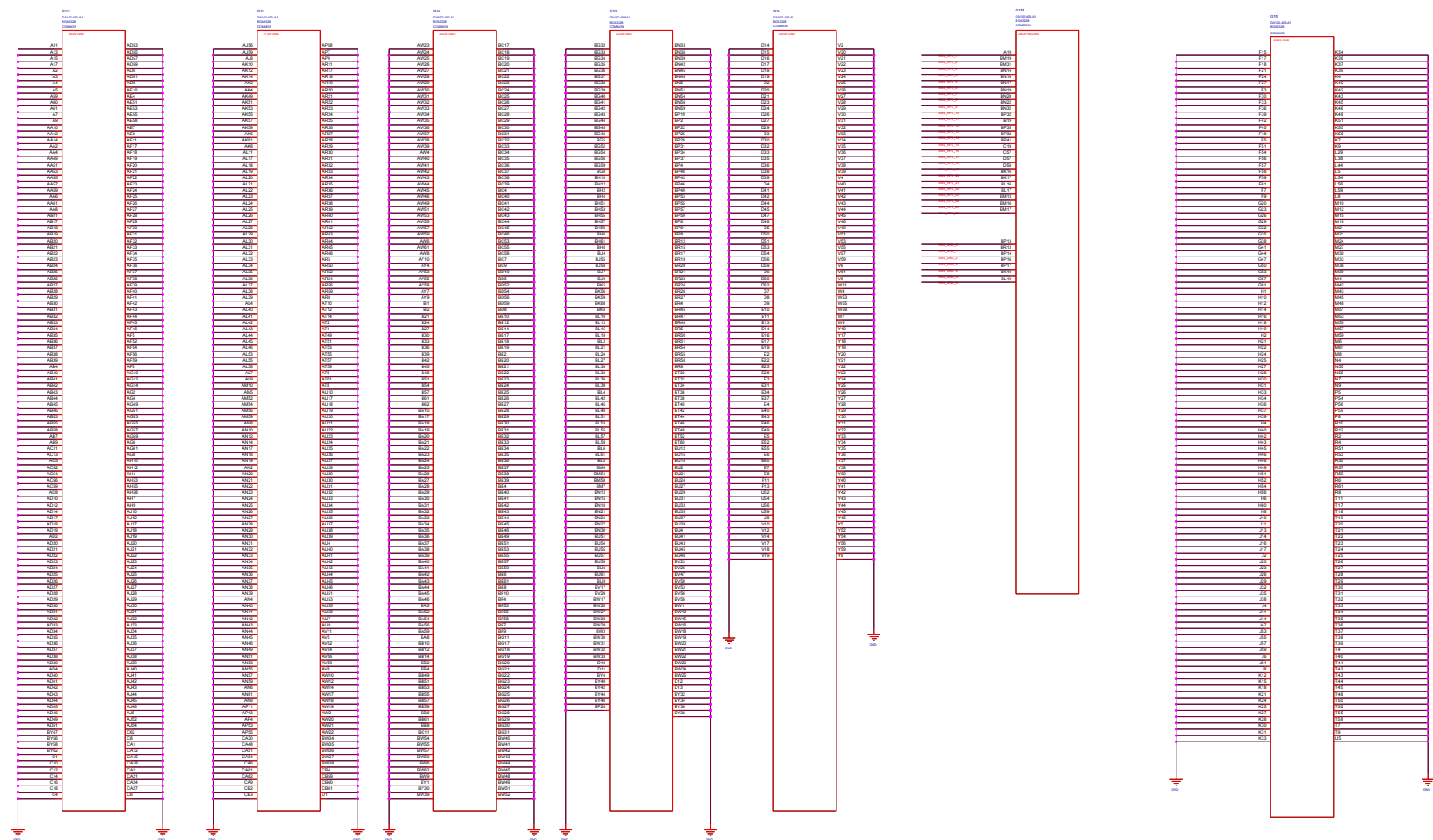
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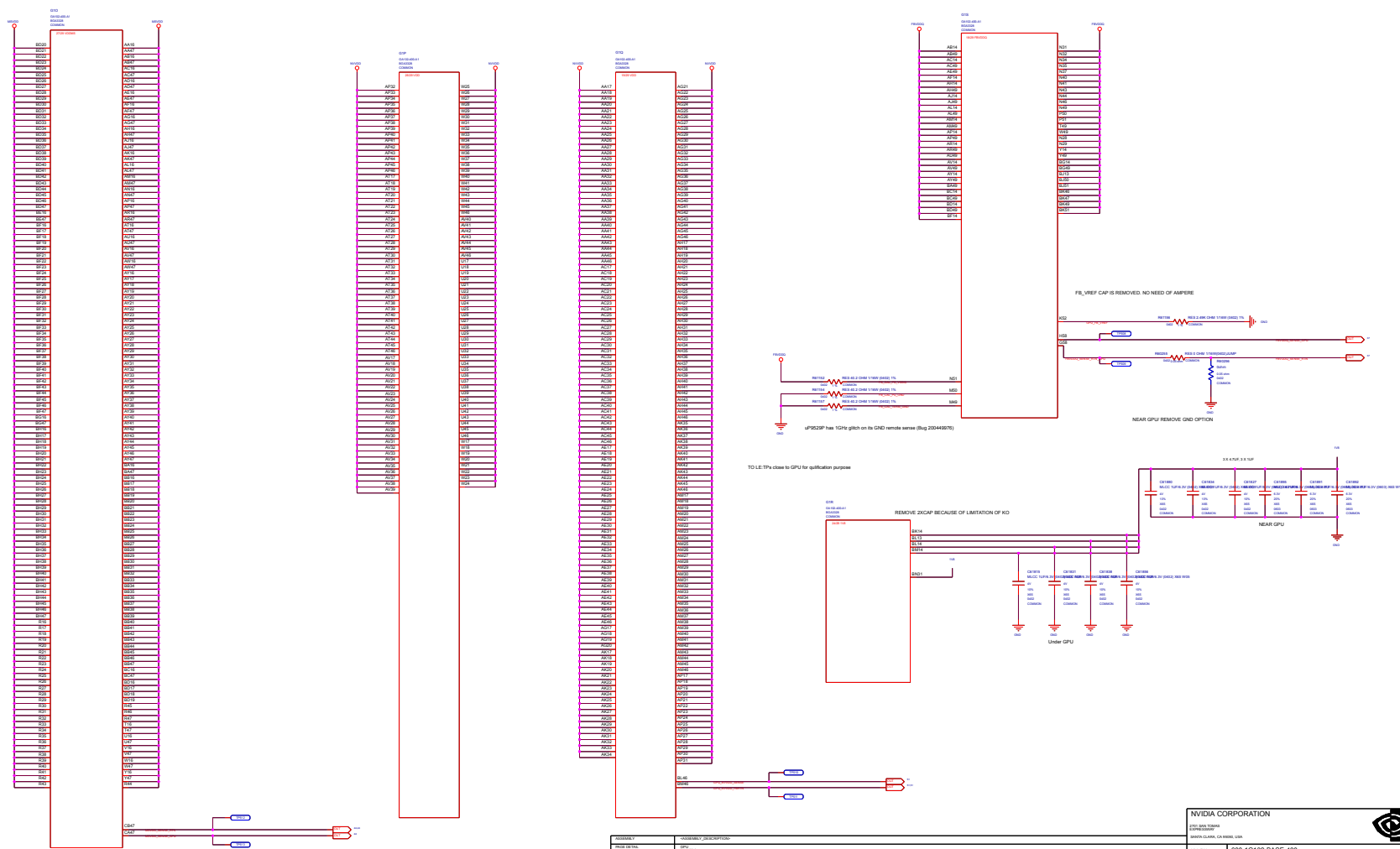




GPU GND, RFUs & RSVD



GPU PWR and GND



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PROJ (ID TAG)	CPU

NVIDIA CORPORATION

2701 SAN TOMAS
SUNBROOK
SANTA CLARA, CA 95050, USA

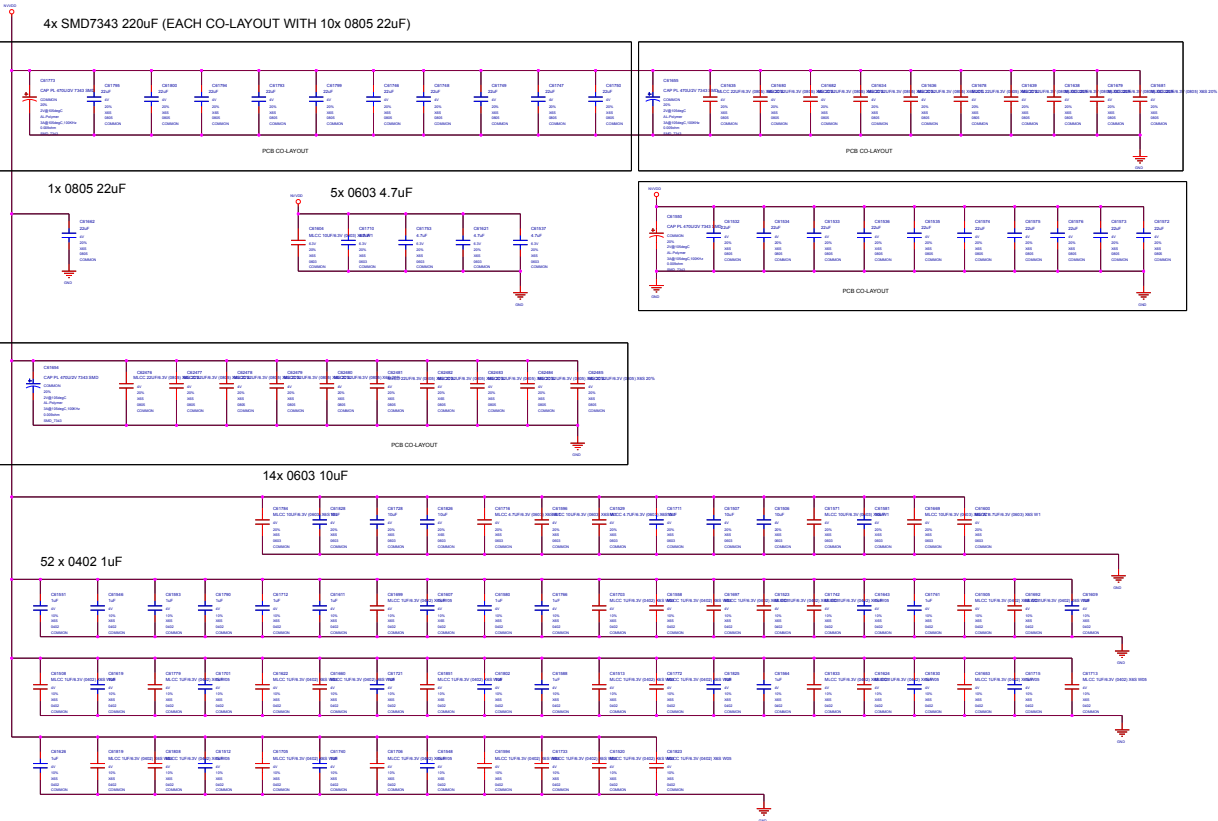


NV_PN	600-1G132-BASE-400
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FOR REV	PG132 021	PAGE	20 OF 2
WORK REV	A	DATE	06-JUN-2020

NVVDD

UNDER GPU



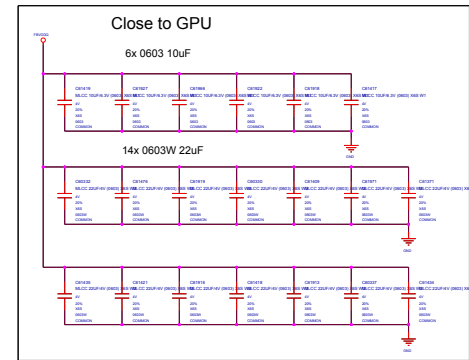
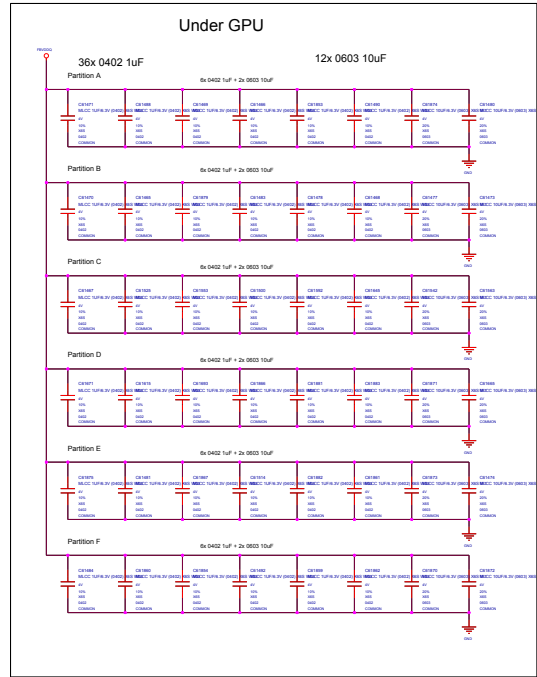
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ASSEMBLY	MANUFACTURE/PRODUCTION
DATE 02/20/2024	DATE 02/20/2024

NVIDIA CORPORATION	
1201 AVENUE OF THE SCIENCES	
SANTA CLARA, CA 95051, USA	
REV./PIN	600-1G132-BASE-400
PCB REV.	70102-B01
DATE	21 OCT 24
DESIGNED BY	100-200-000

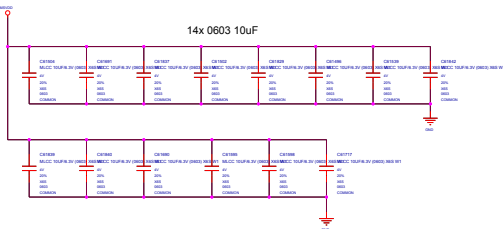


FBVDDQ

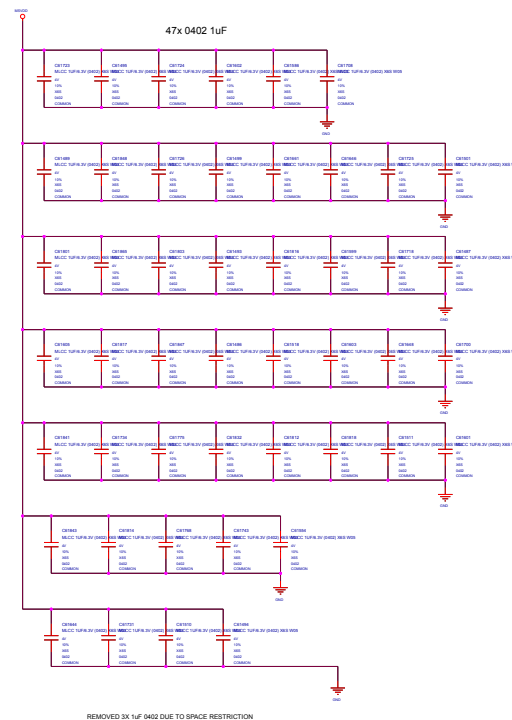
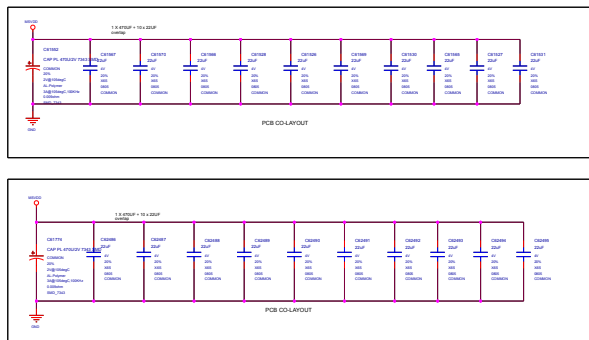


MSVDD

UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



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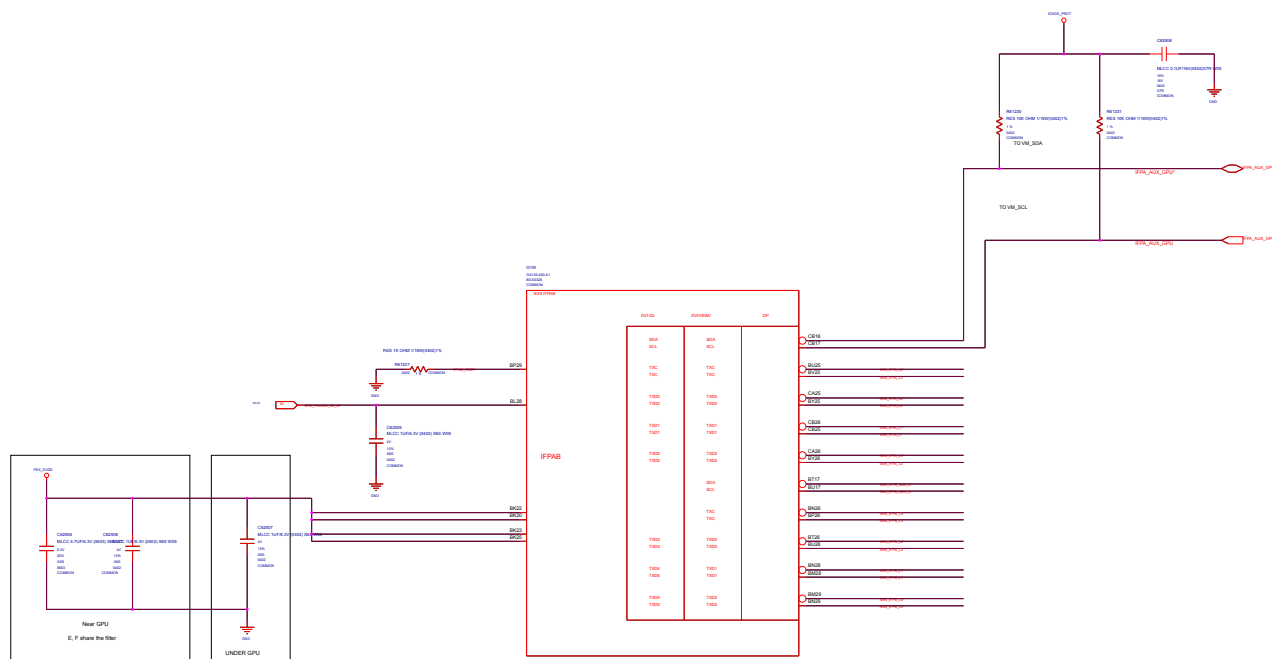
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IFPA UNUSED, IFPB UNUSED



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	OFFER UNLDED, OFFER UNLDED

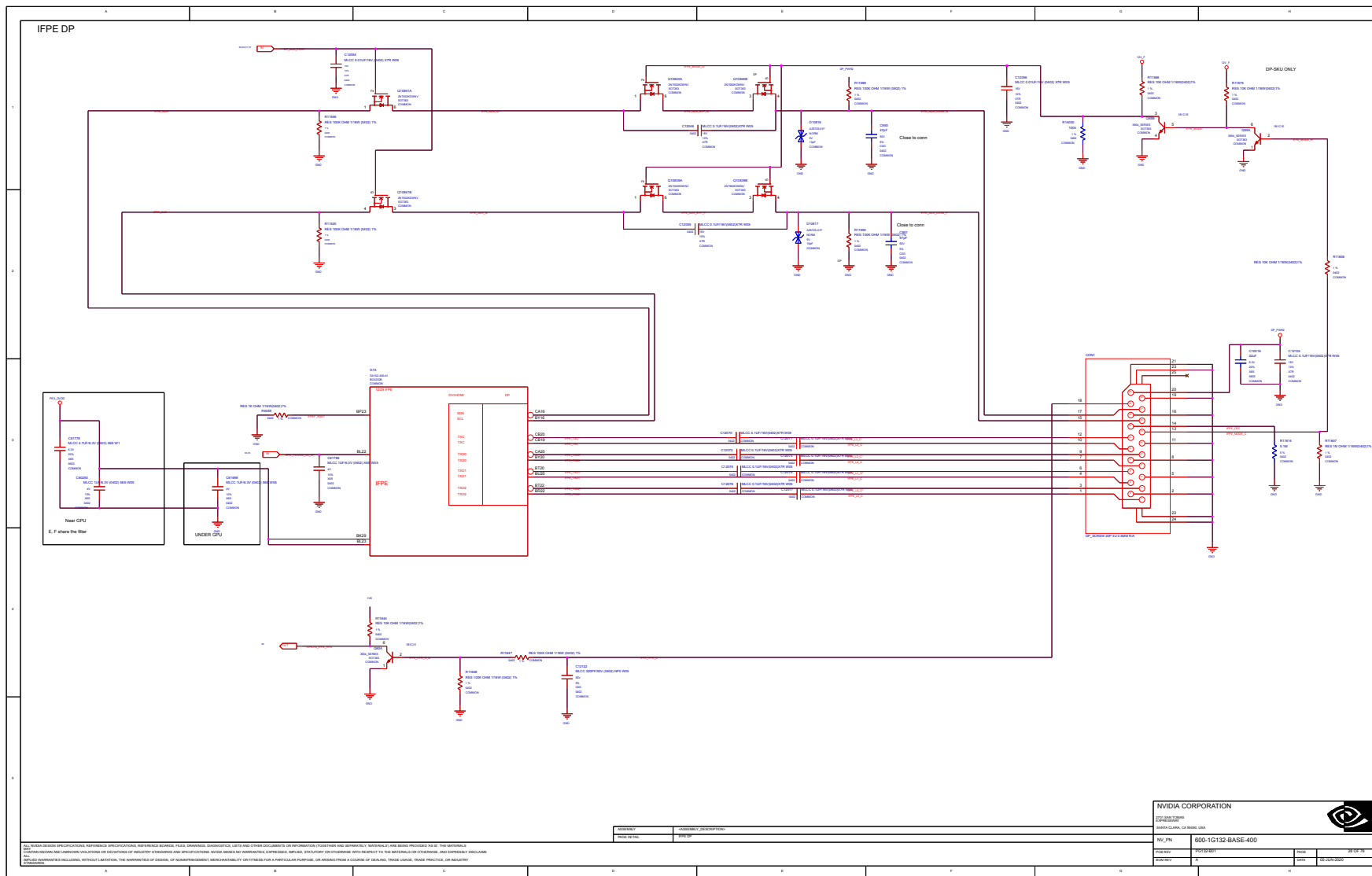
NVIDIA CORPORATION
2700 SAN TOMAS
SUNNYVALE, CA 94088
SANTA CLARA, CA 95050 USA

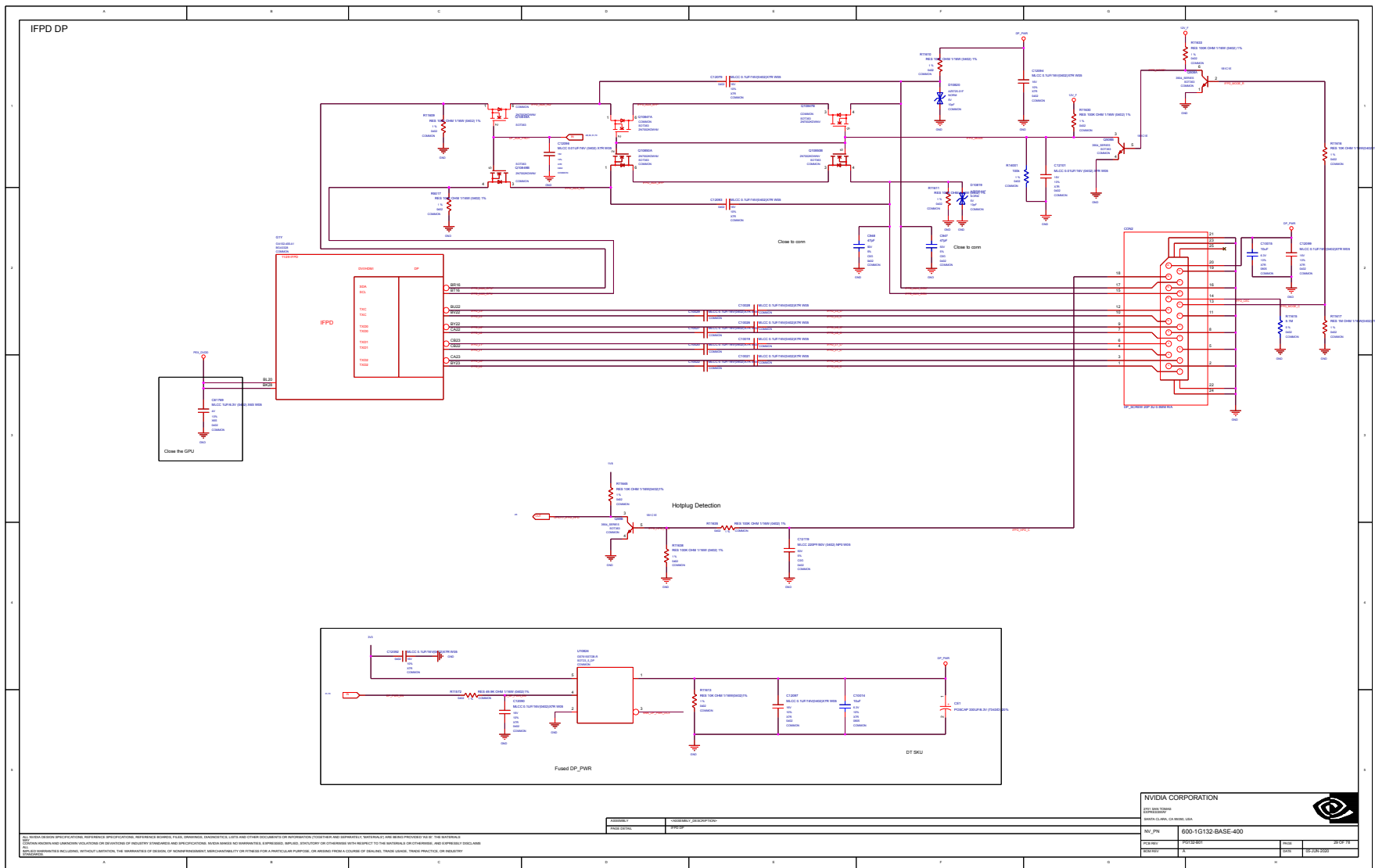


NV_PN	600-1G132-BASE-400
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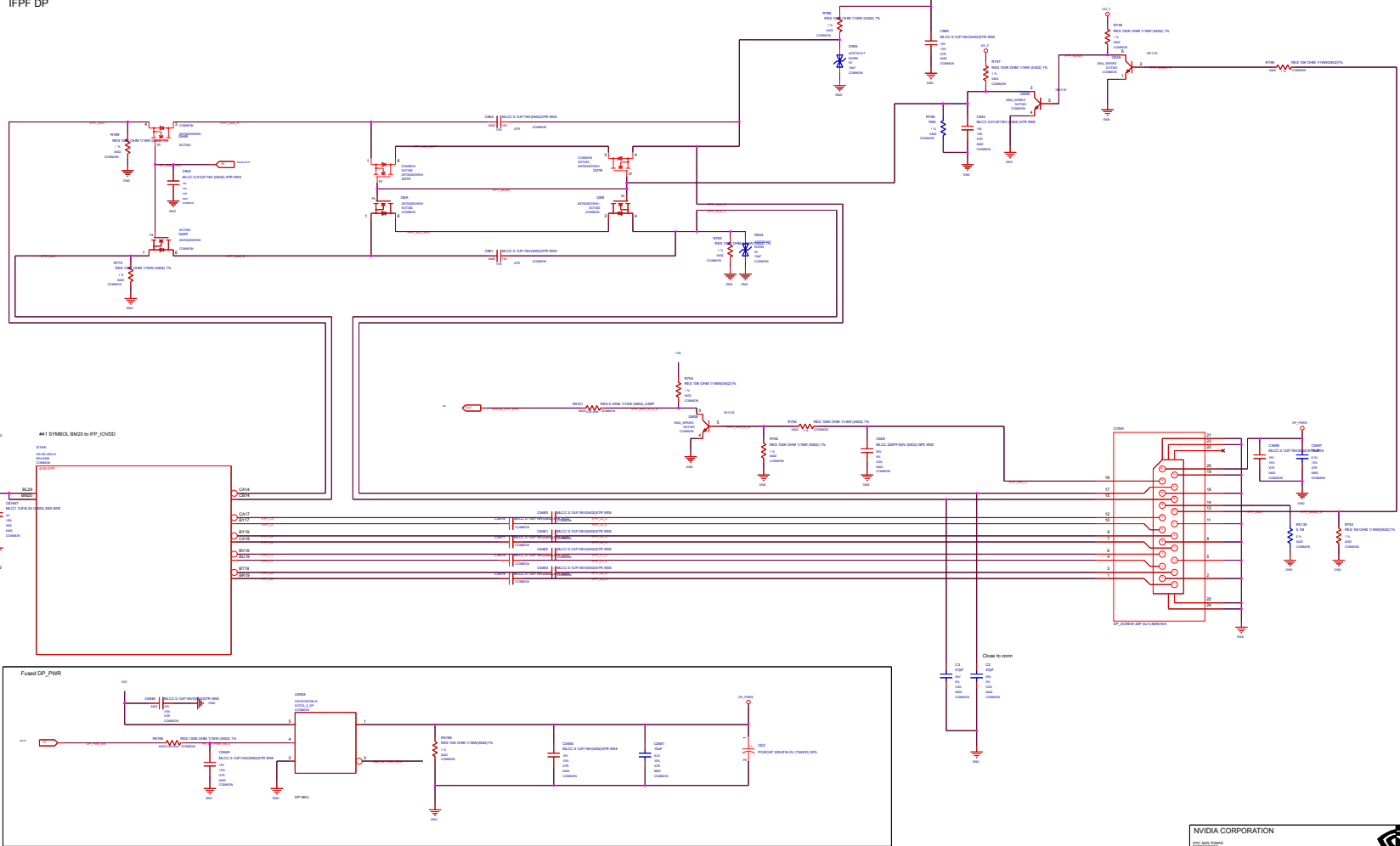
PCB REV	PG132-601	PRJ#	27 OF 1
WCM REV	A	DATE	05-JUN-2020

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IFPF DP



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1000-10132-BASE-400

1000-10132-BASE-400

1000-10132-BASE-400

1000-10132-BASE-400

1000-10132-BASE-400

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1000-10132-BASE-400

1000-10132-BASE-400

1000-10132-BASE-400

MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG	RAMCFG Q4 Q3
L	L	L	00000	RAMCFG MICRON 8Gb 1900ps
L	H	L	00010	RAMCFG T8D
H	L	L	00100	RAMCFG T8D
H	L	H	00101	RAMCFG T8D
H	L	H	00101	RAMCFG MICRON 8Gb 2100ps

H=High, Tied to 1.8V
M=Middle, Tied to 0.9V
L=Low, Tied to 0V

DEFAULT

ROM_BO	ROM_SI	ROM_SCLK	SMARTFANQ3 FS_OVERT	1.ENABLE 0.DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

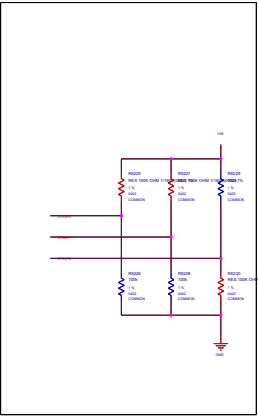
DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCI_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	L	H	1	H	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

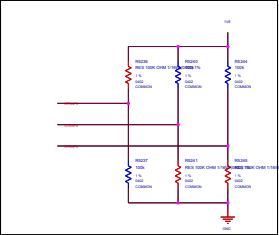
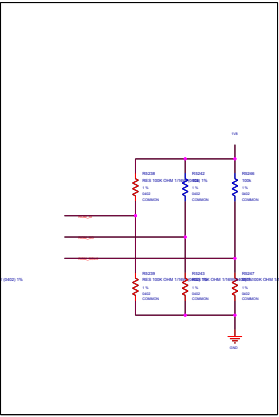
Default

1.SMB_ALT_ADDR ENABLE
0.SMB_ALT_ADDR DISABLE
1.DEVID_SEL REBRAND
0.DEVID_SEL ORIGINAL
1.PCI_CFG LOW POWER
0.PCI_CFG HIGH POWER
1.VGA_DEVICE ENABLE
0.VGA_DEVICE DISABLE

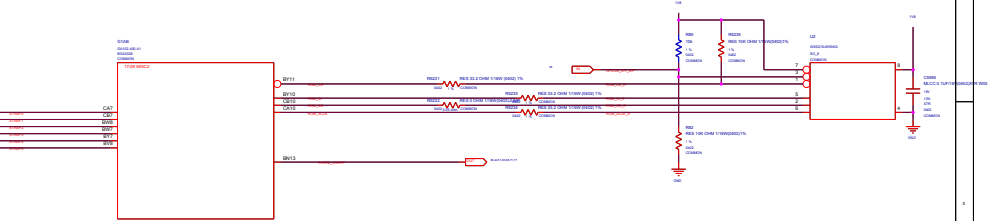
GROUP0



GROUP1



GROUP2



NVIDIA CORPORATION

2011-01-01
NVIDIA CORPORATION
NVIDIA CORPORATION, 2700 SAN JUAN AVENUE, SANTA CLARA, CA 95050, USA

REV: 1.0

800-1G132-BASE-400

REV: 1.0

REV: 1.0

REV: 1.0

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REV: 1.0

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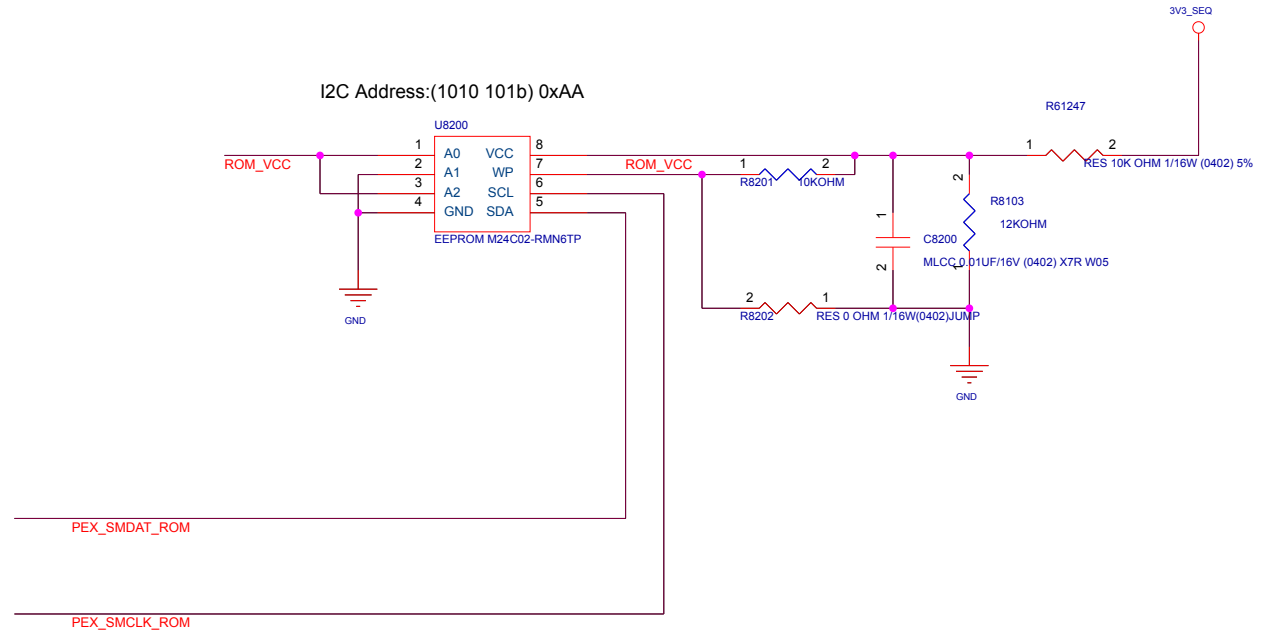
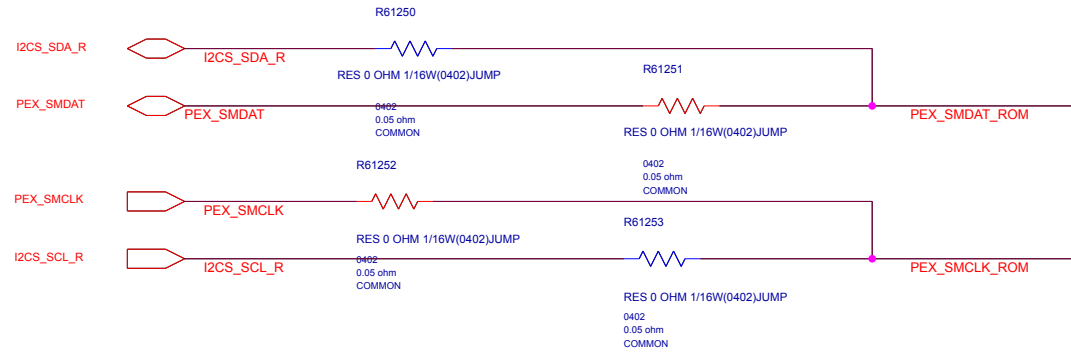
2721 SAN TOMAS
SANTA CLARA, CA 95050

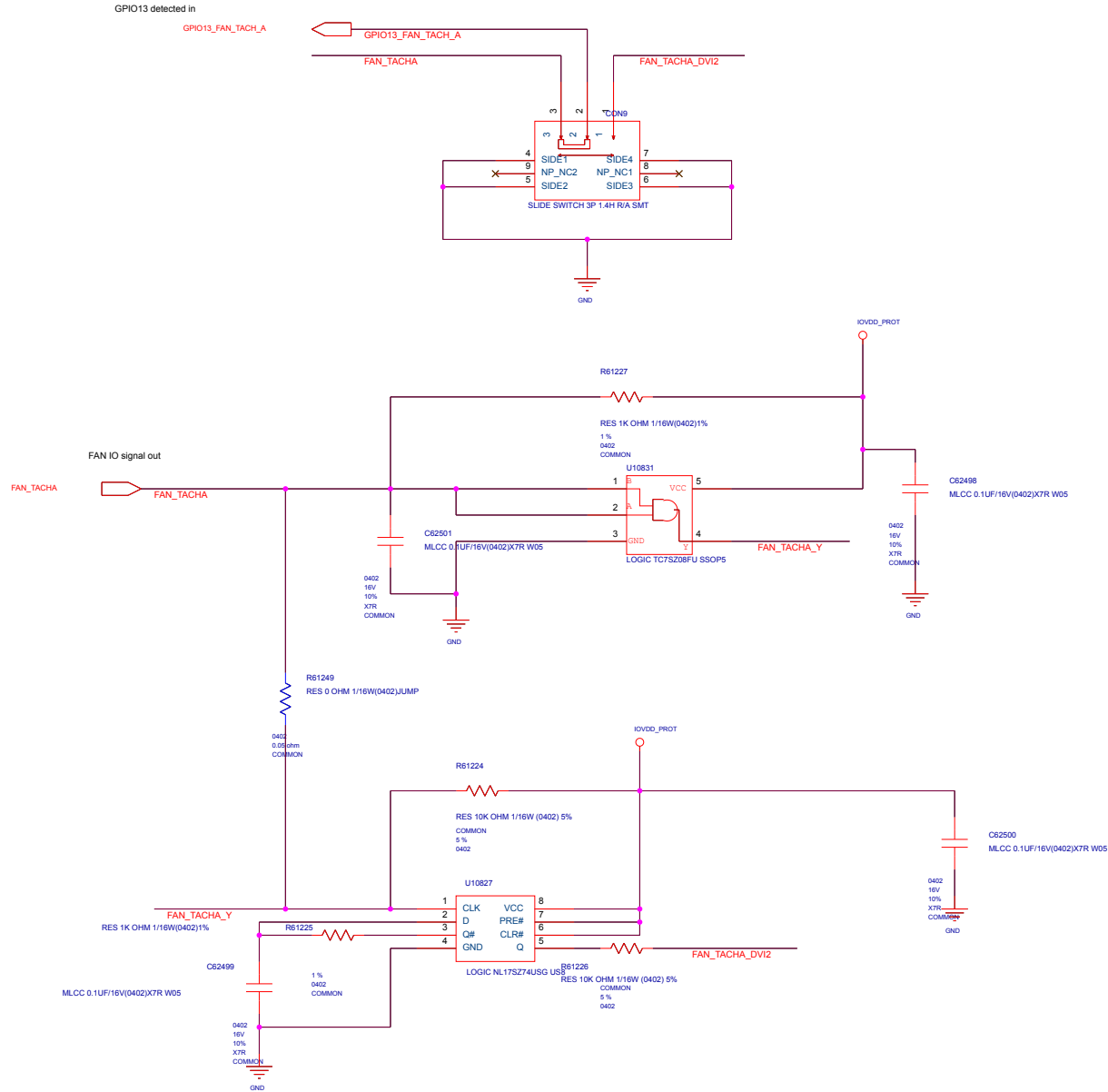


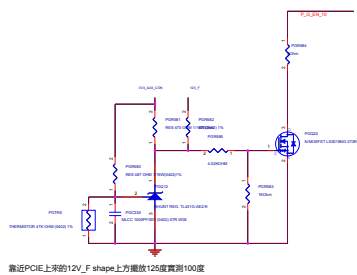
NV_PN	600-1G132-BASE-400
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Pub ref	PL124-881	Pub	33 OF 2
Scd ref	A	Date	05/20/2023

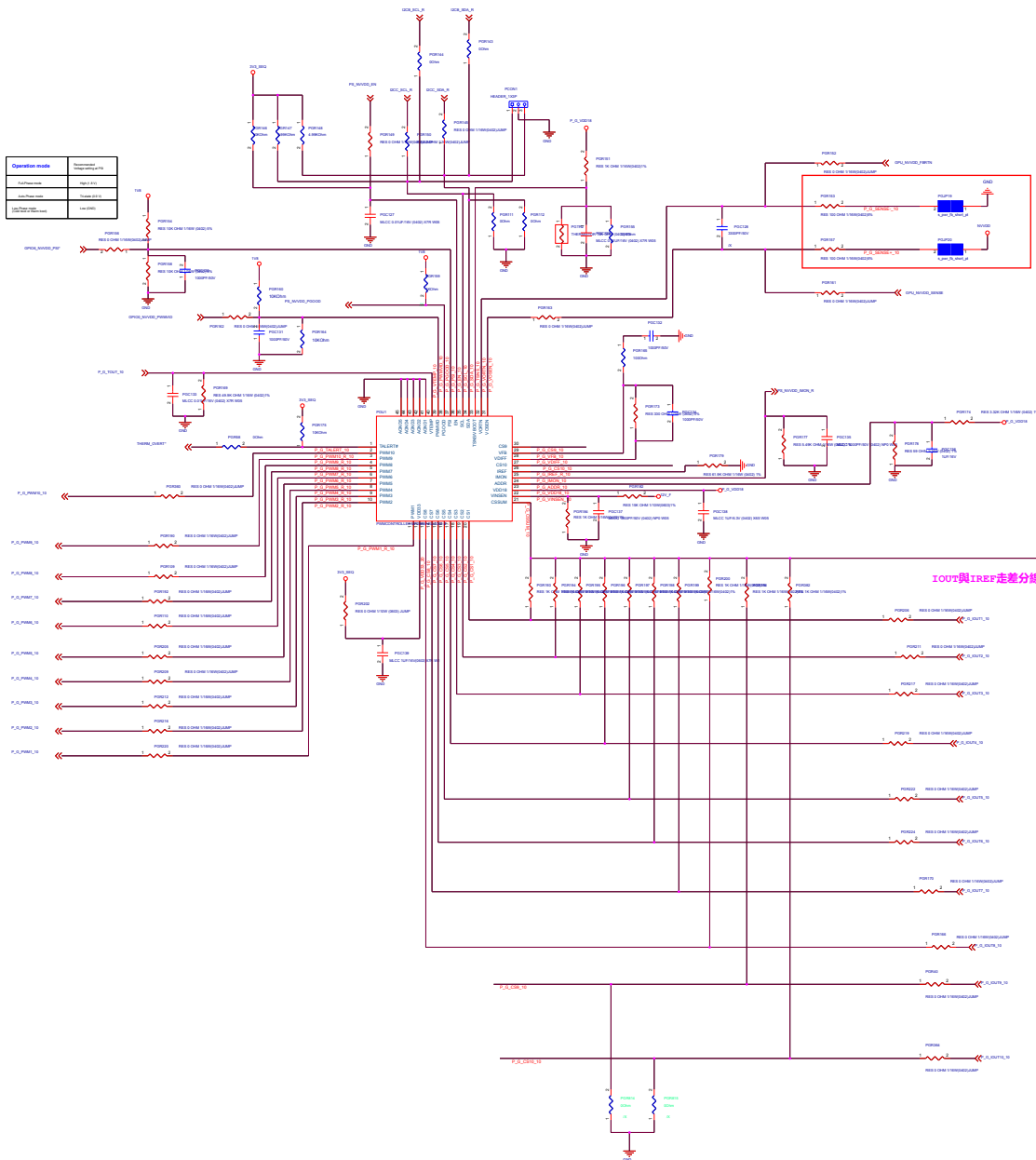
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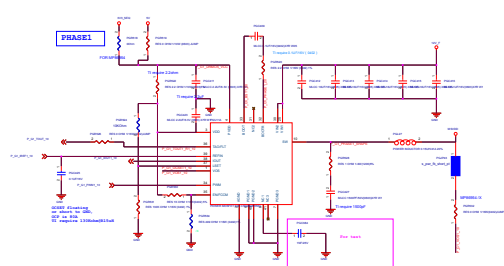




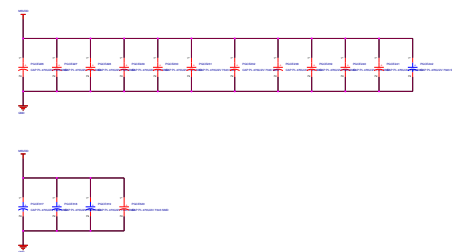
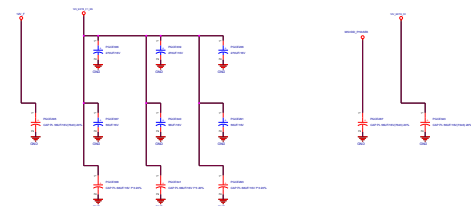
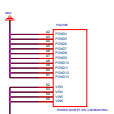
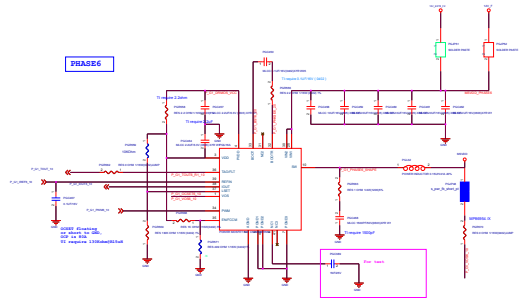
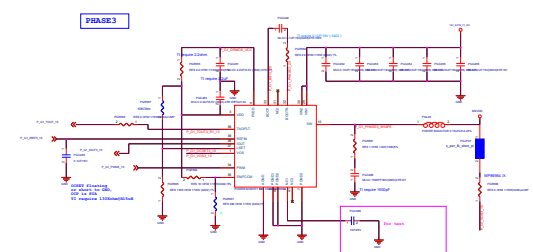
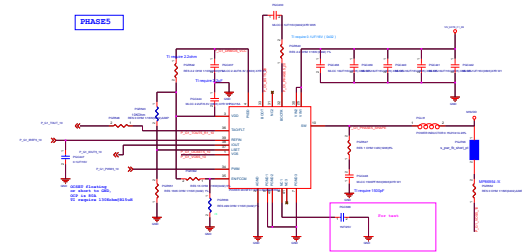
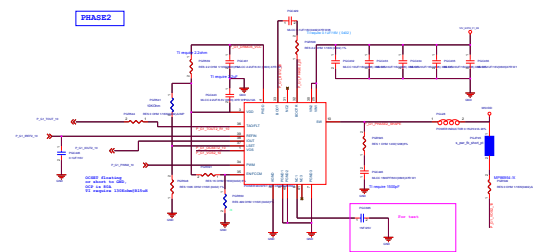
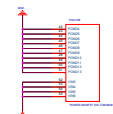
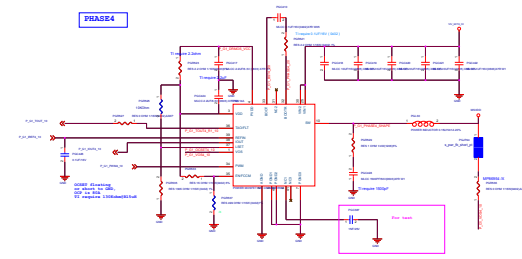
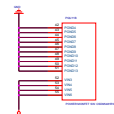


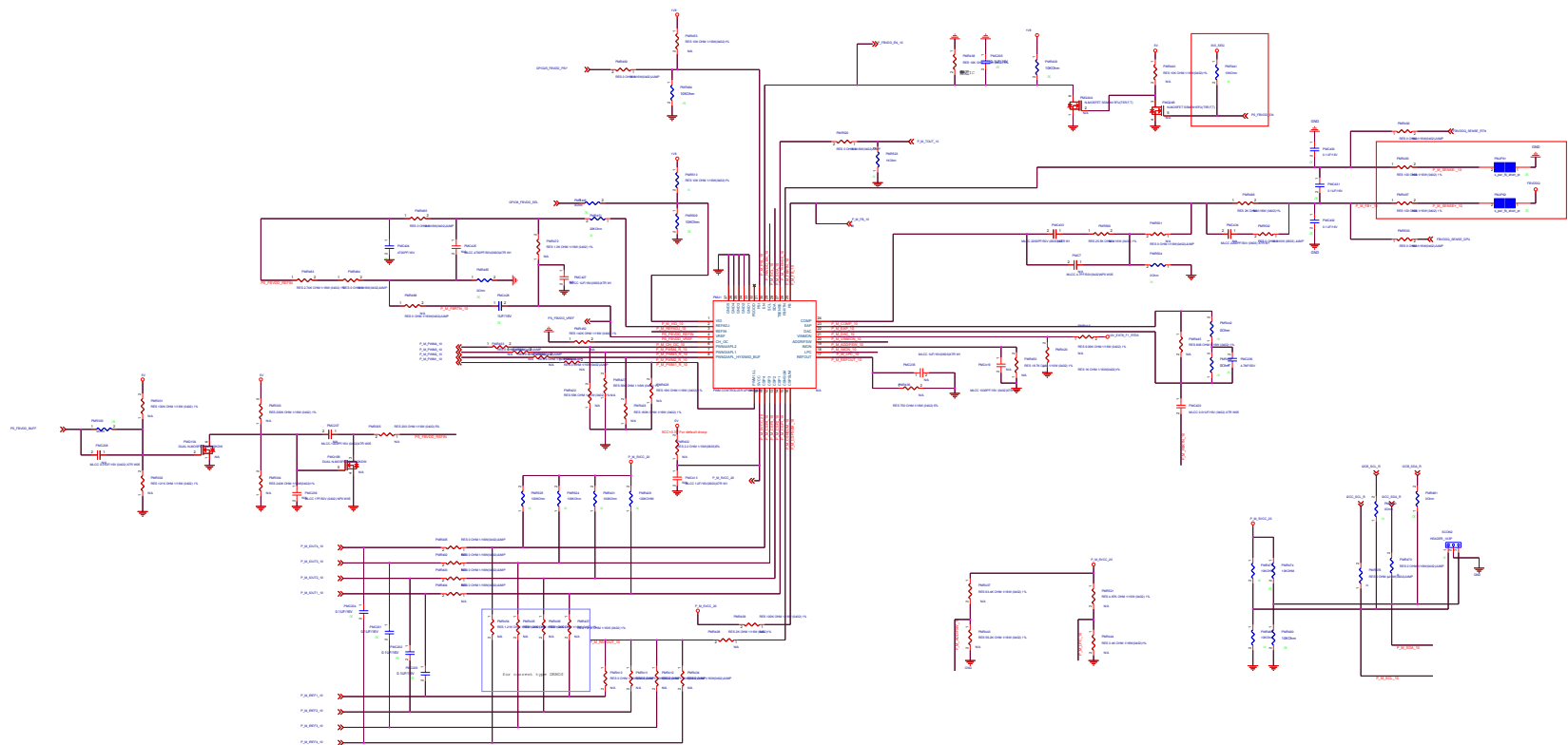
Operation mode	Recommended bitrate setting at PoE
Full-Phase mode	High (2.4K)
Auto-Phase mode	Default (2.0 K)
Lite-Phase mode (Load based or Queue based)	Low (128K)





PHASE	V1	V2	V3	V4
PHASE1	100	100	100	100
PHASE2	10	10	10	10
PHASE3	10	10	10	10
PHASE4	10	10	10	10

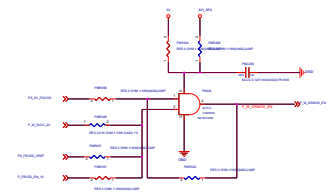
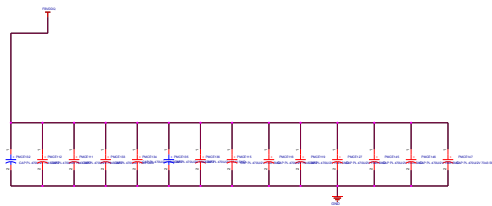
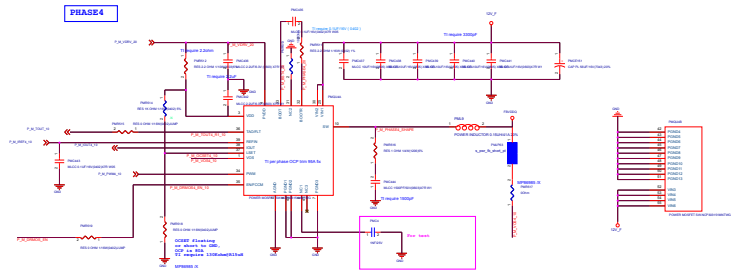
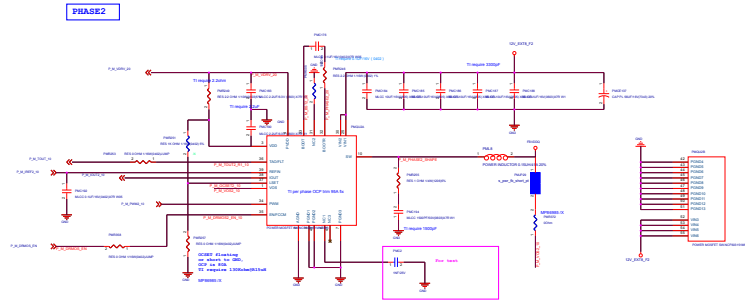
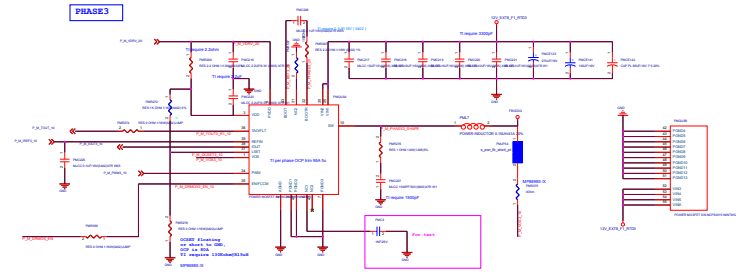
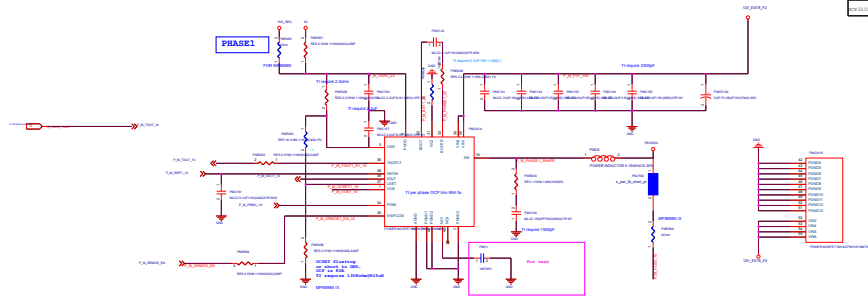


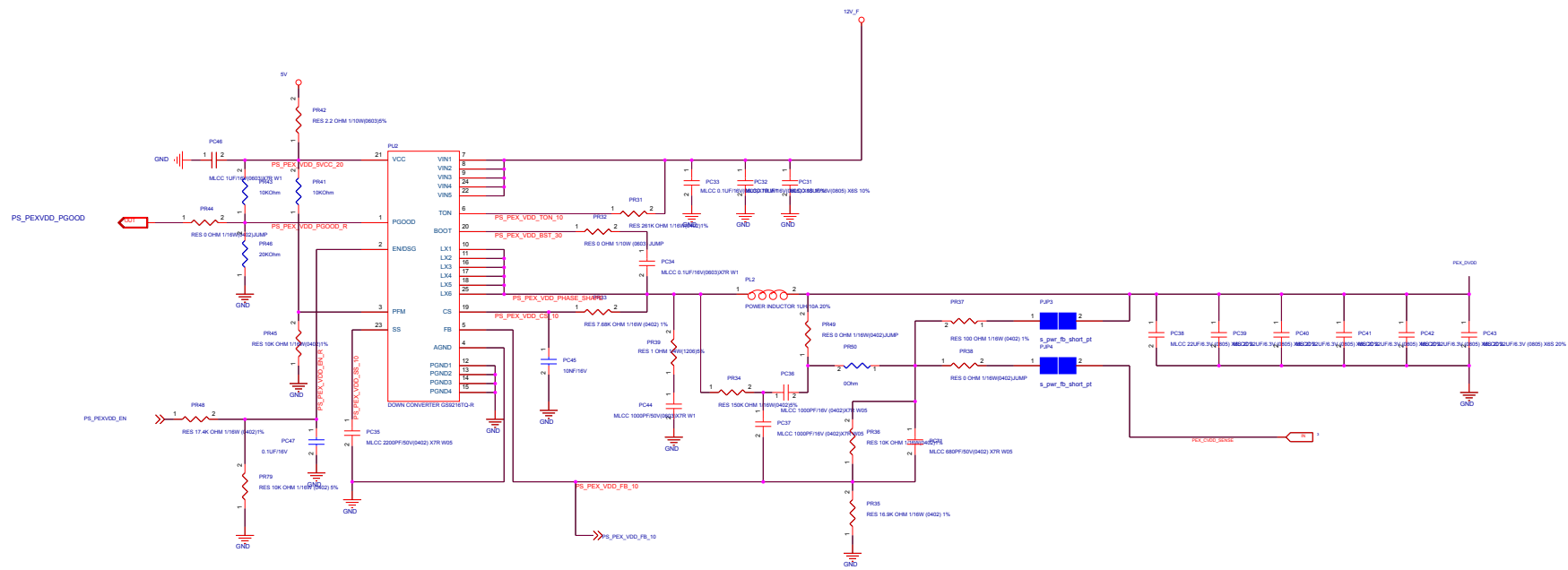


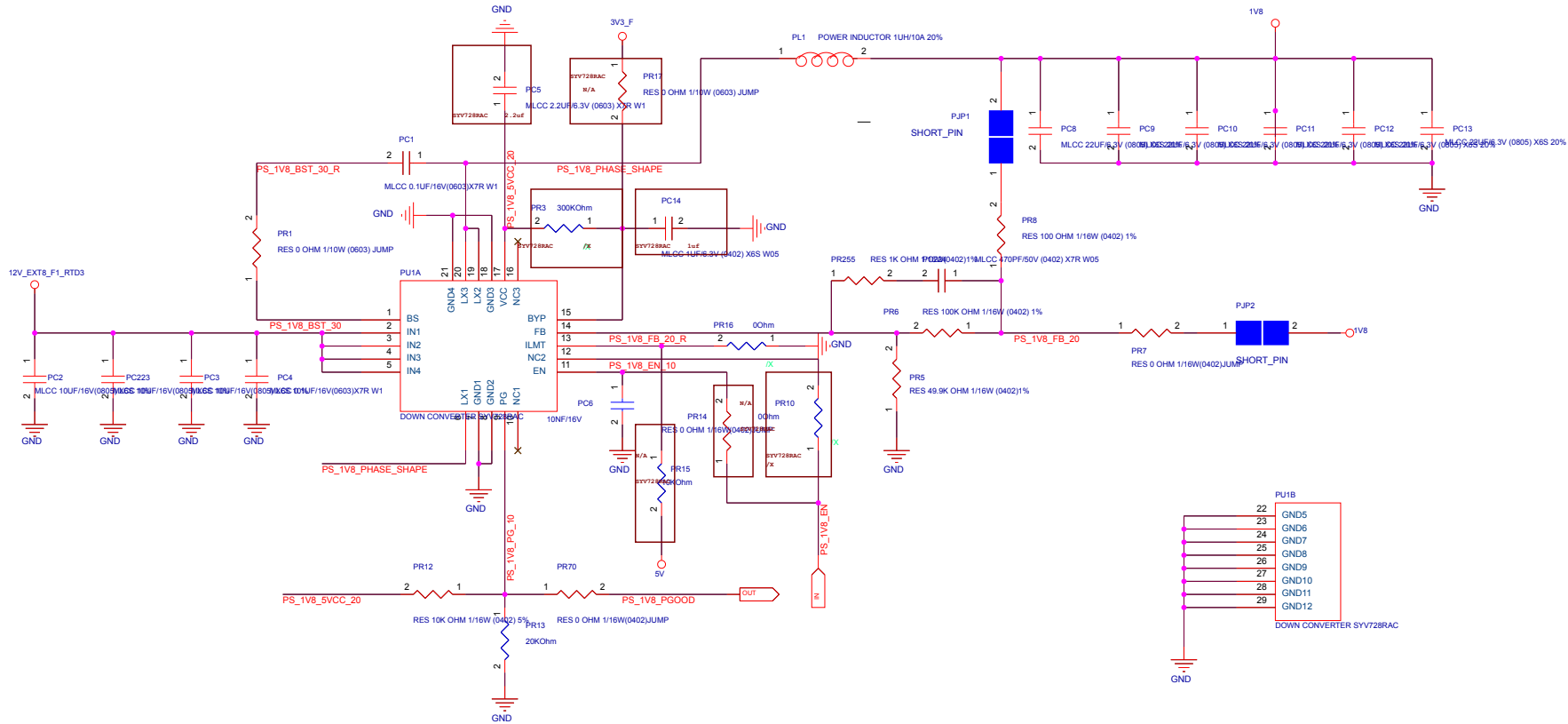
Simulation mode	Simulation type
Transient	Time Domain
AC Sweep	Frequency Domain
DC Sweep	DC Operating Point

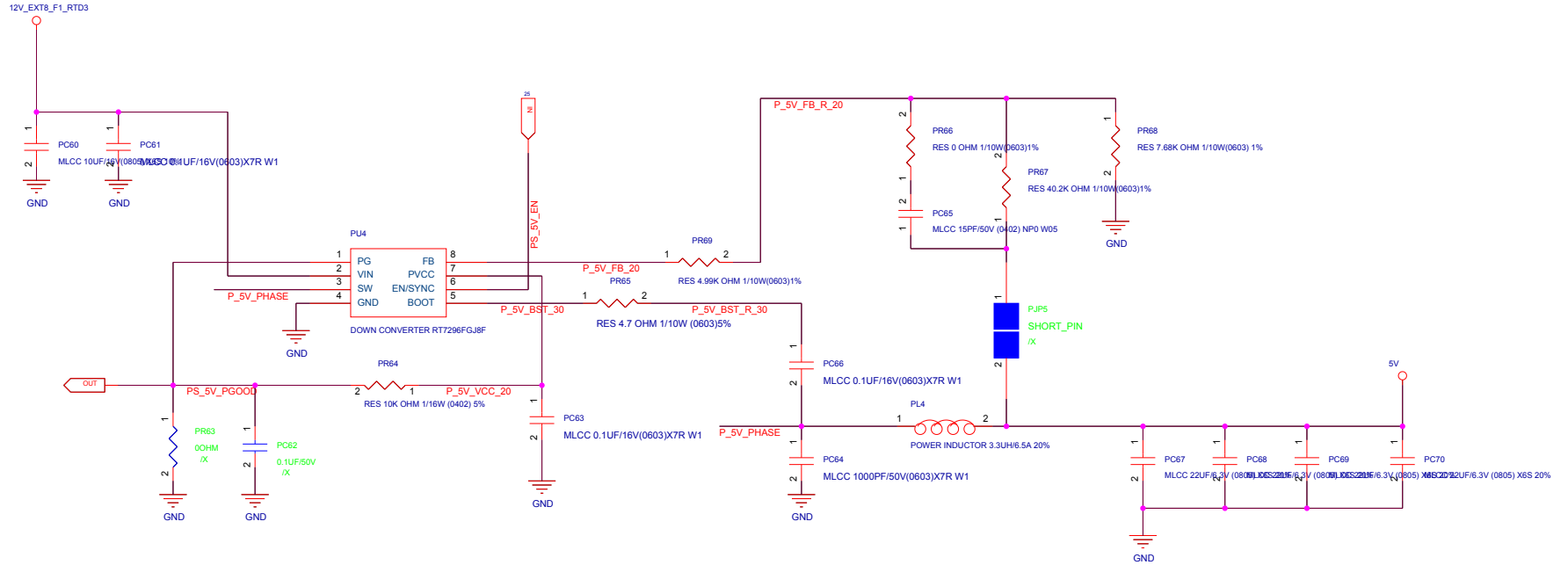
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RC match	Csum	0.1uF	0.1uF
	Rcup	14.7K ohm	30K ohm
Total OCP (40mA)	Rsum	0.9K ohm	0.9K ohm
	Isum	88.7uA	88uA

PHASE1	PHASE2	PHASE3	PHASE4
PHASE1_V1	/2	0.000	/2
PHASE1_V2	/2	/2	0.000
PHASE1_V3	0.000	0.000	/2









PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPI01	GPI03	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



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REVISION: 1.0

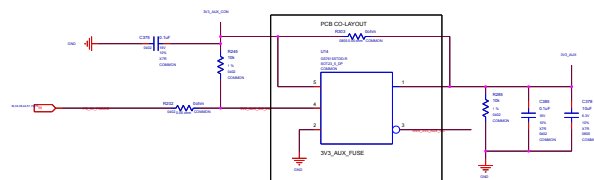
DATE: 10/10/2023

NVIDIA CORPORATION
600-1G132-BASE-400



DATE: 10/10/2023

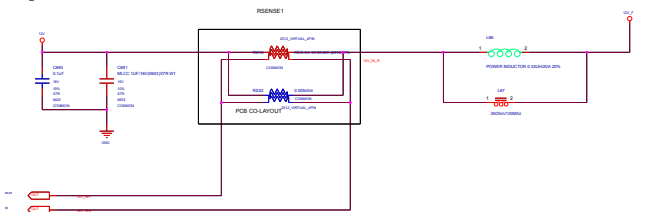
PS: Inputs, Filtering, and Monitoring



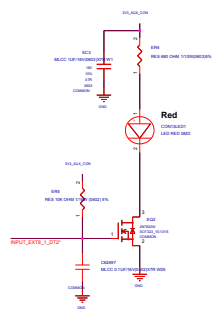
PEX 3V3 INPUT - 10W



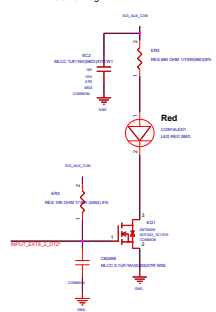
PEX 12V INPUT - 66W



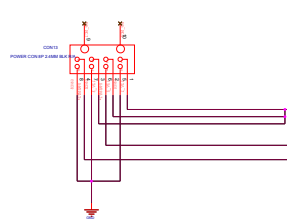
Cable Plug LED



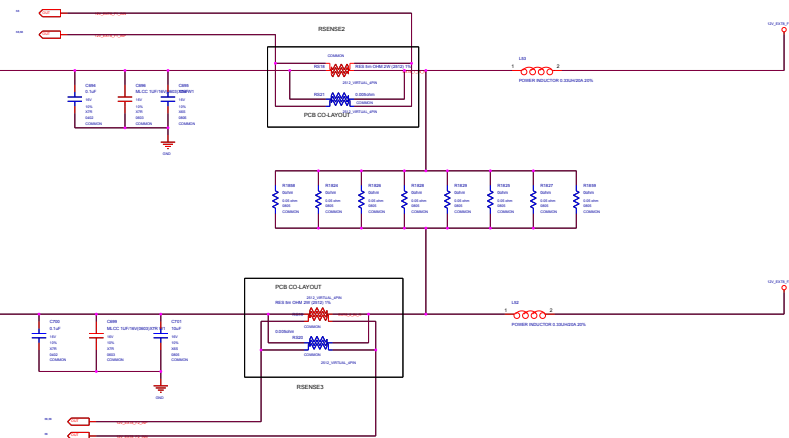
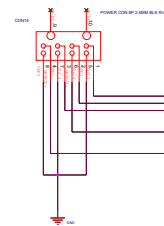
Cable Plug LED



PEX8 INPUT 1 - 2x4 PCIe CON 150W



PEX8 INPUT 2 - 2x4 PCIe CON 150W



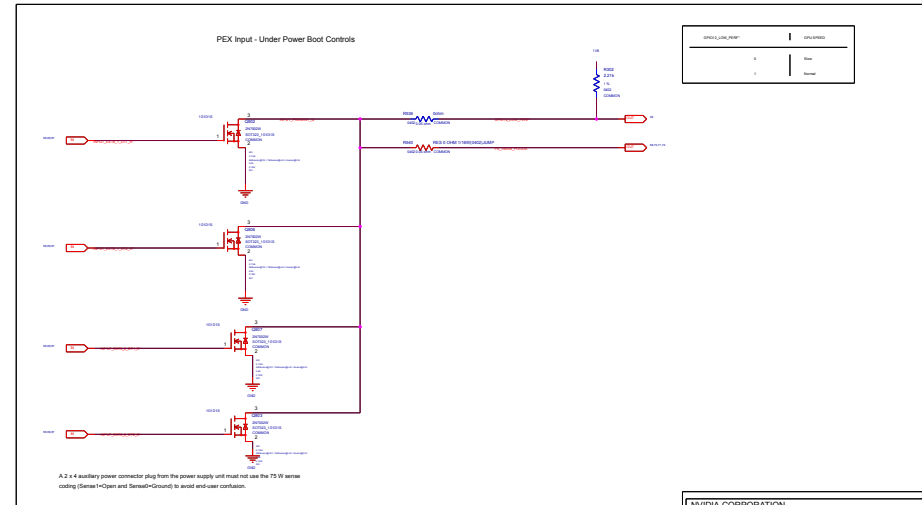
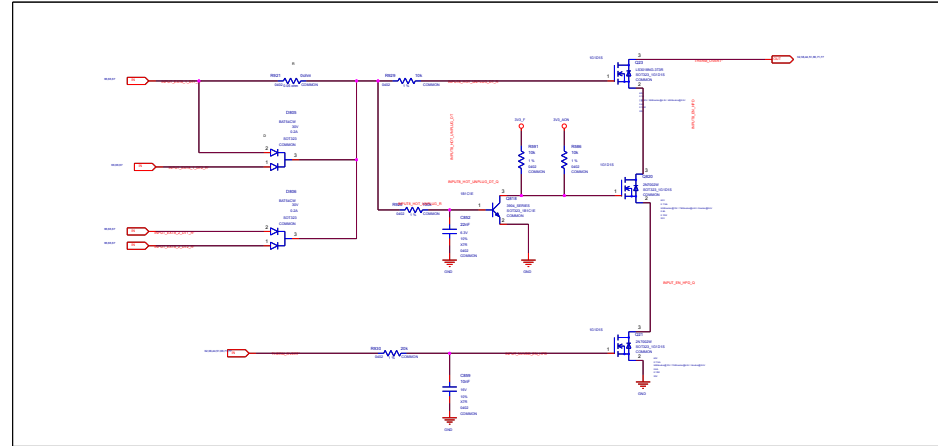
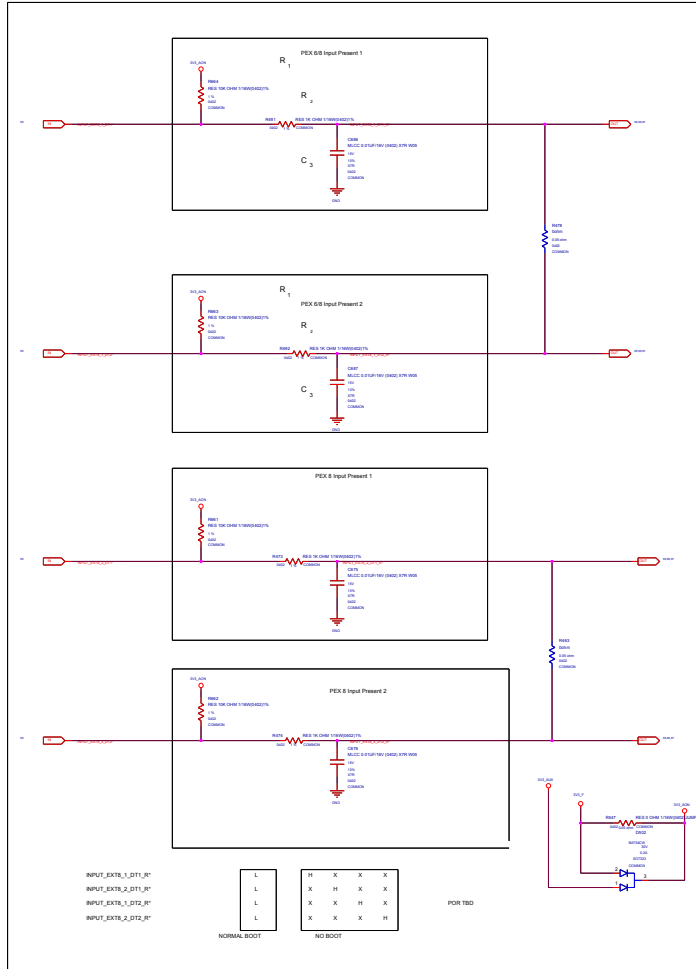
NVIDIA CORPORATION
 2700 LEGACY WAY
 SANTA CLARA, CA 95058, USA

REVISION	DESCRIPTION
1.0	Initial Release

NVIDIA CORPORATION	2700 LEGACY WAY	SANTA CLARA, CA 95058, USA
PEX 3V3 INPUT - 10W	PEX 12V INPUT - 66W	PEX8 INPUT 1 - 2x4 PCIe CON 150W
PEX 3V3 INPUT - 10W	PEX 12V INPUT - 66W	PEX8 INPUT 2 - 2x4 PCIe CON 150W



PS: 12V Current Steering & Hot Unplug Detect

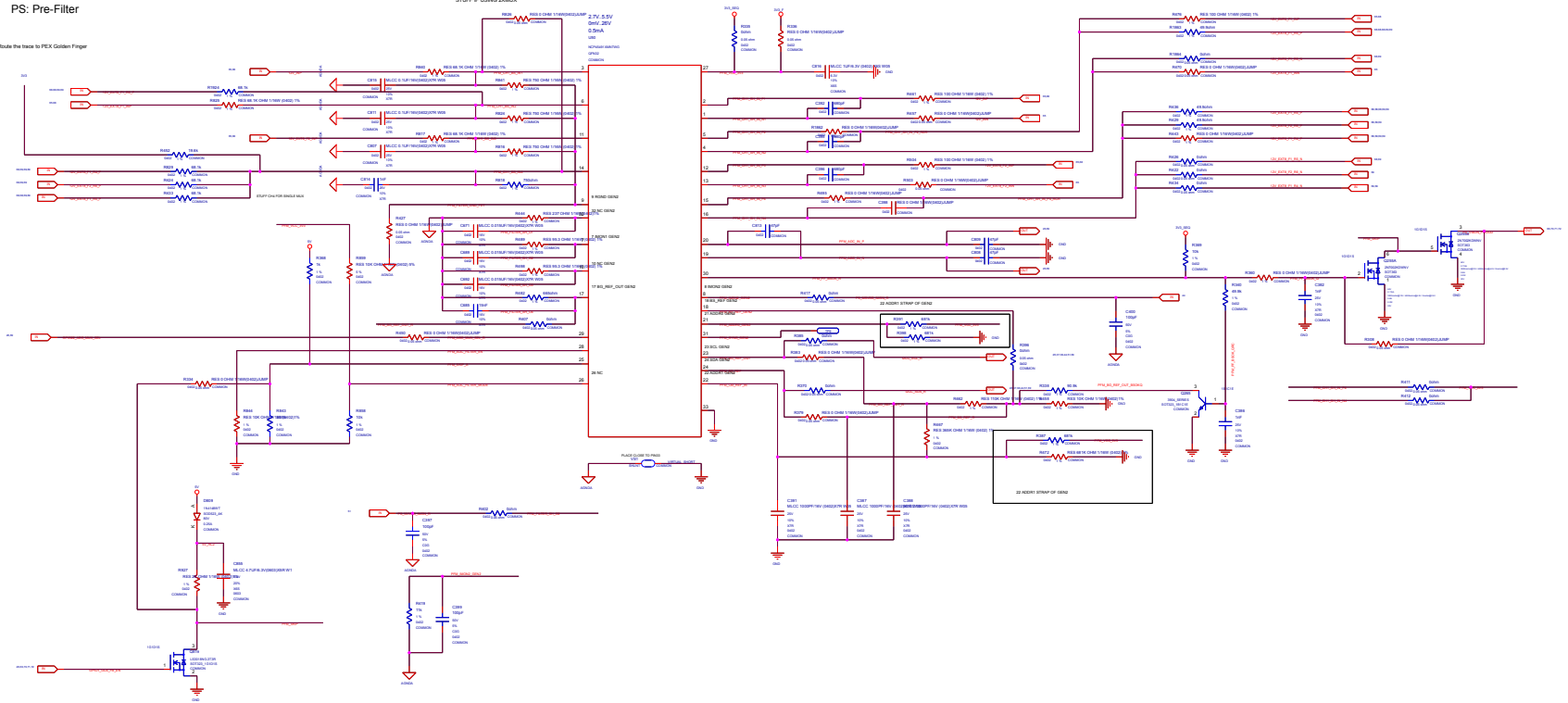


NVIDIA CORPORATION	
2701 SAN TOMAS SANTA CLARA, CA 95050, USA	
NV_PN	600-1G132-BASE-400
PCB REV	PG132-001
SCHEM REV	A

[illegible]

PS: Pre-Filter

Route the trace to PEK Golden Finger



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ASSEMBLY
TO PRELIMINARY

NVIDIA CORPORATION
2001 W. BROADWAY
SANTA ANITA, CA 94068-1000




REV. 1.0 600-10132-BASE-400

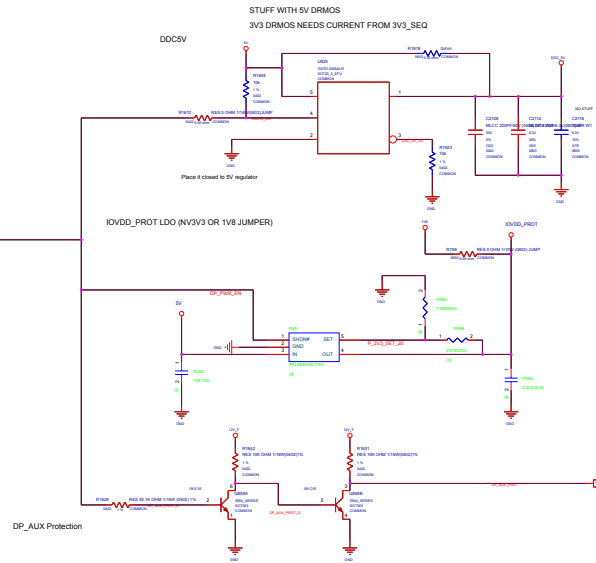
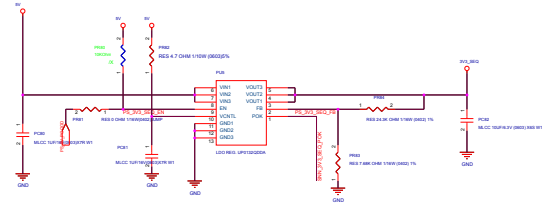
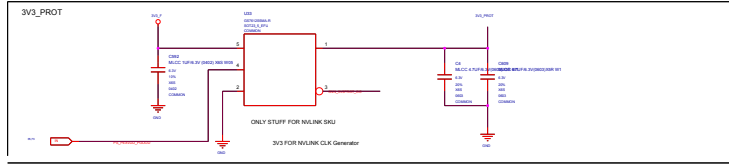
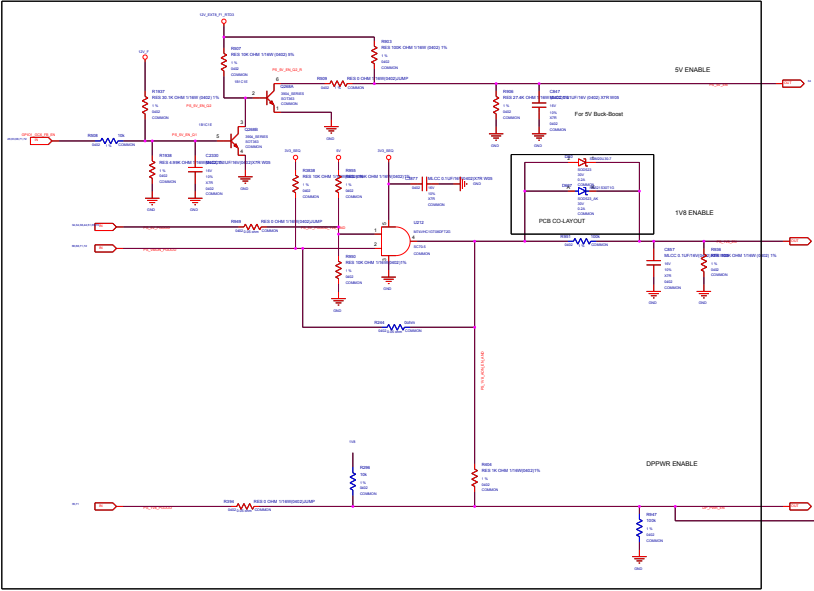
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REV: 1.0
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RV_PN		600-1G132-BASE-400	
PICB REV	PIC132-0001	PRDTS	SE OF TS
MSM REV	A	DATE	10-JUN-2007

SEQUENCE:5V,1V8,3V3_SEQ ENABLE

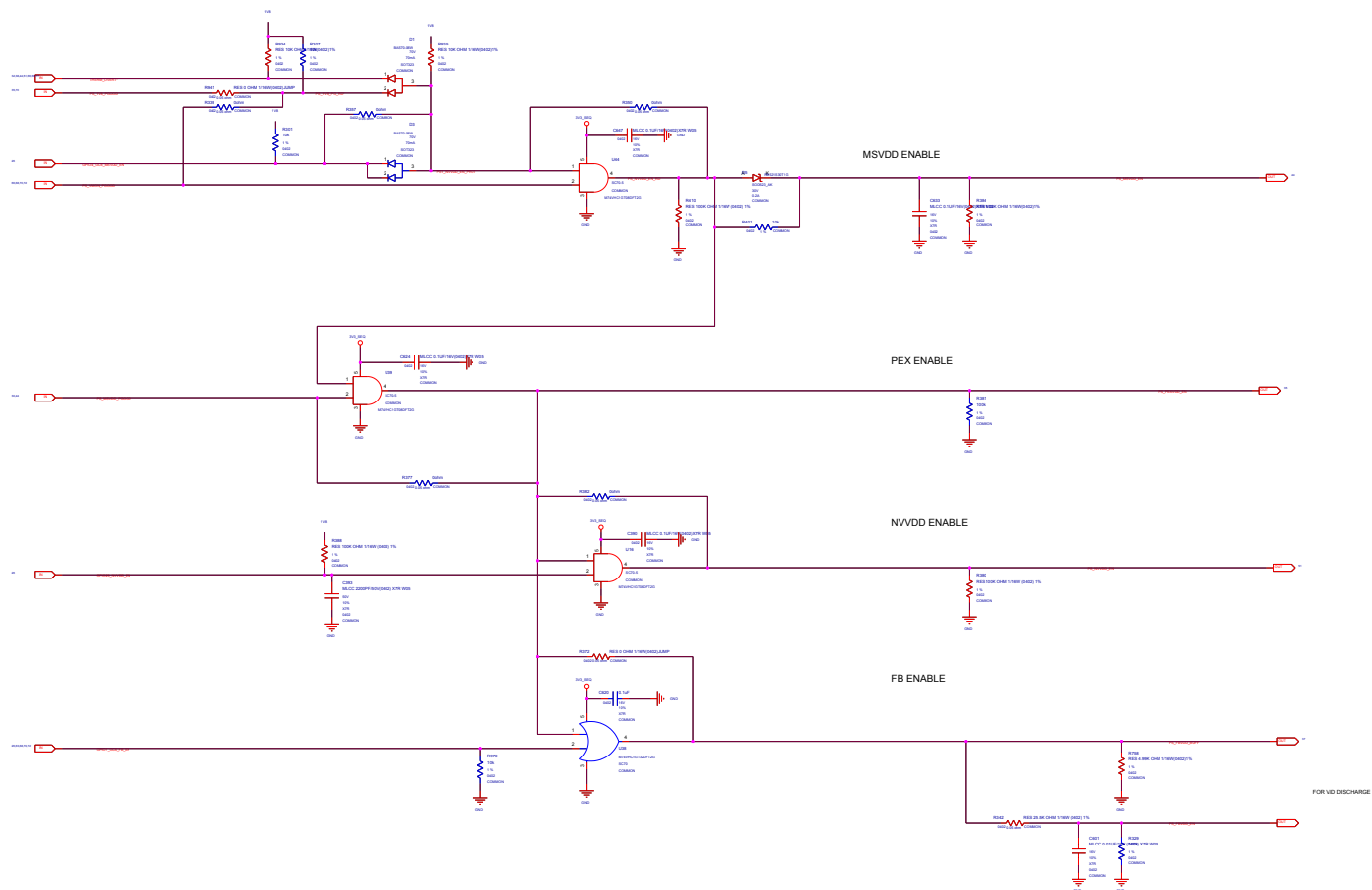


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NVIDIA CORPORATION	
2701 SAN TOME SUNNYVALE, CA 94085, USA	
INV.#N	600-1G132-BASE-400
PUR.REV	PG1.32-M01
SOLD.REV	A



SEQUENCE: NV, PEX, FB ENABLE



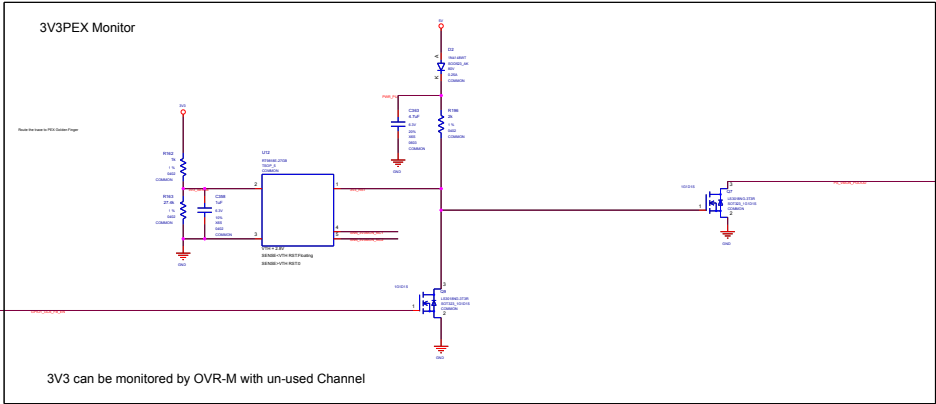
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ASSEMBLY	DESCRIPTION
POWER	SEQUENCE: NV, PEX, FB

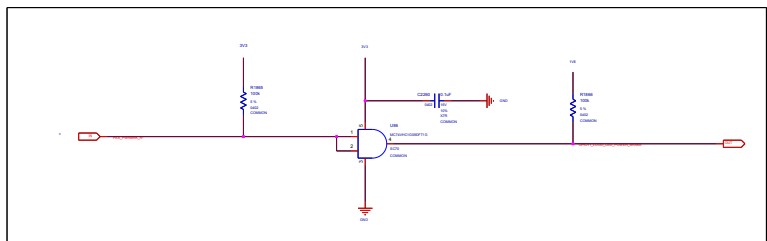
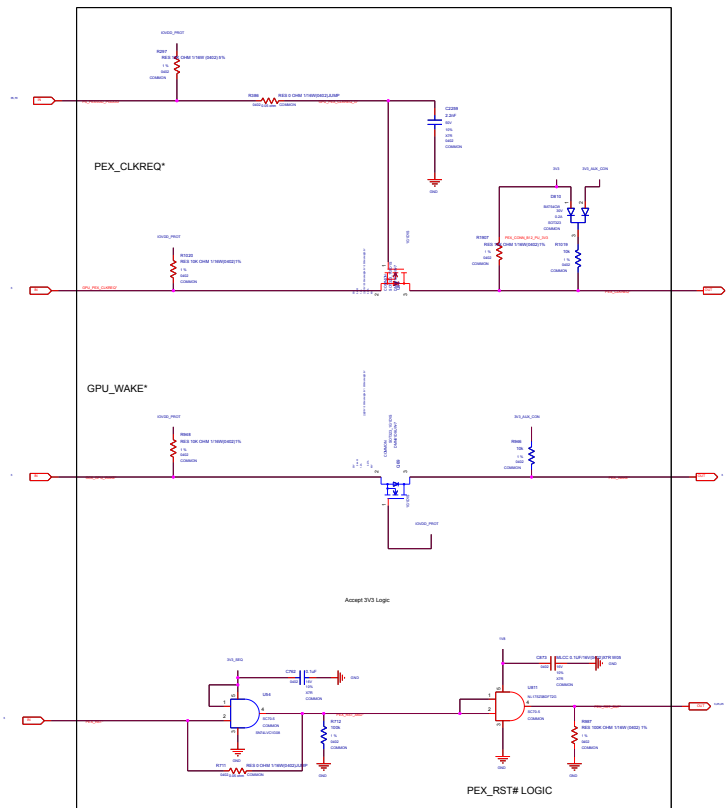
NVIDIA CORPORATION			
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SANTA CLARA, CA 95058, USA			
NV_PN	600-1G132-BASE-400	DATE	11/01/16
REV	1.0	DATE	11/01/16



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SEQUENCE:MISC



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SANTA CLARA, CA 95050, USA



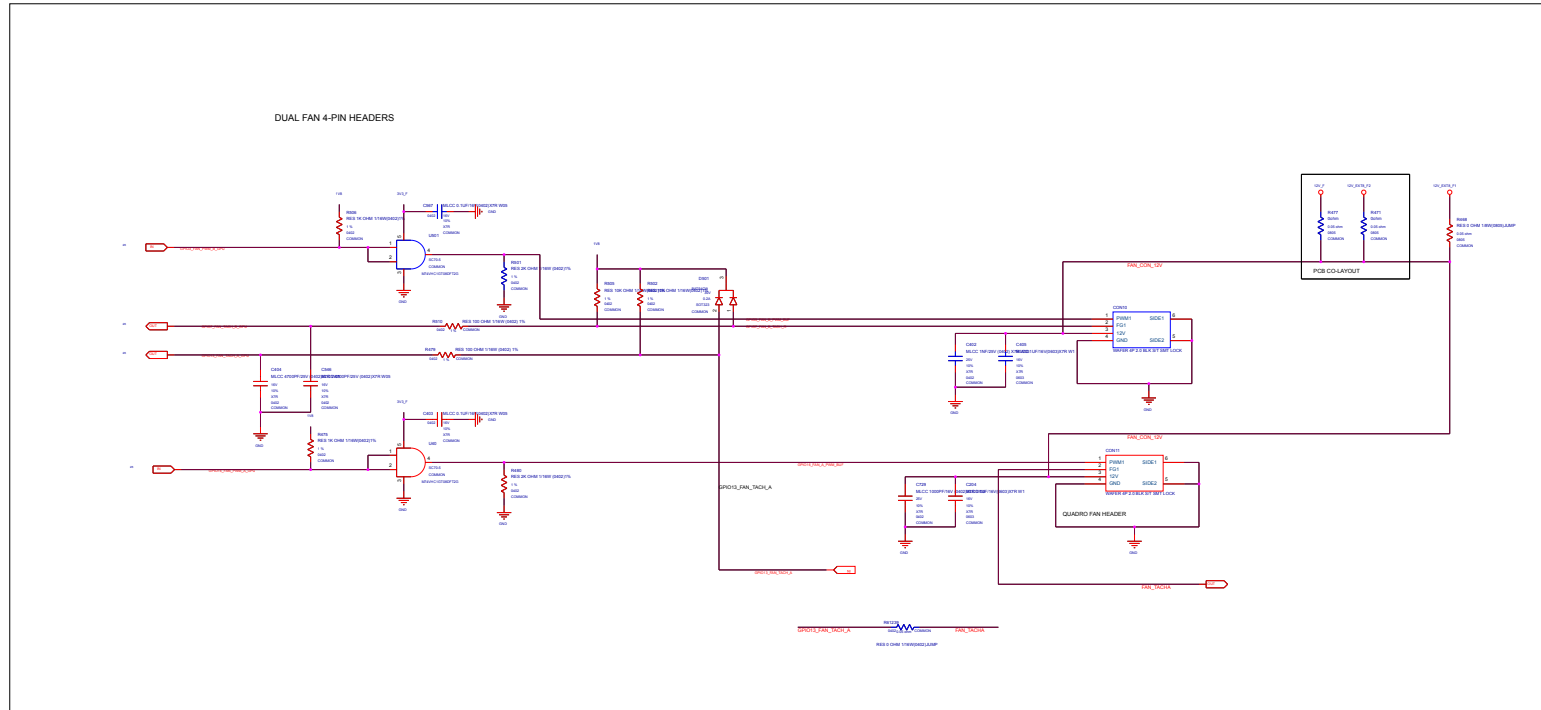
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PLB REV	PG132-0011
BLM REV	A

PRIN	73 OF 75
DATE	05-JUN-2020

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MISC: LED & FAN



ASSEMBLY	ASSEMBLY DESCRIPTION	SANTA CLARA, CA 95050, USA	
PAGE DETAILS	REV: 1.01 & 1.02	600-1G132-BASE-400	
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PCI TERM



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
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NV_FN	600-1G132-BASE-400		
PLN REV	PLN132-001	PAGE	78 OF 78
DATE REV	A	DATE	06-JUN-2020

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