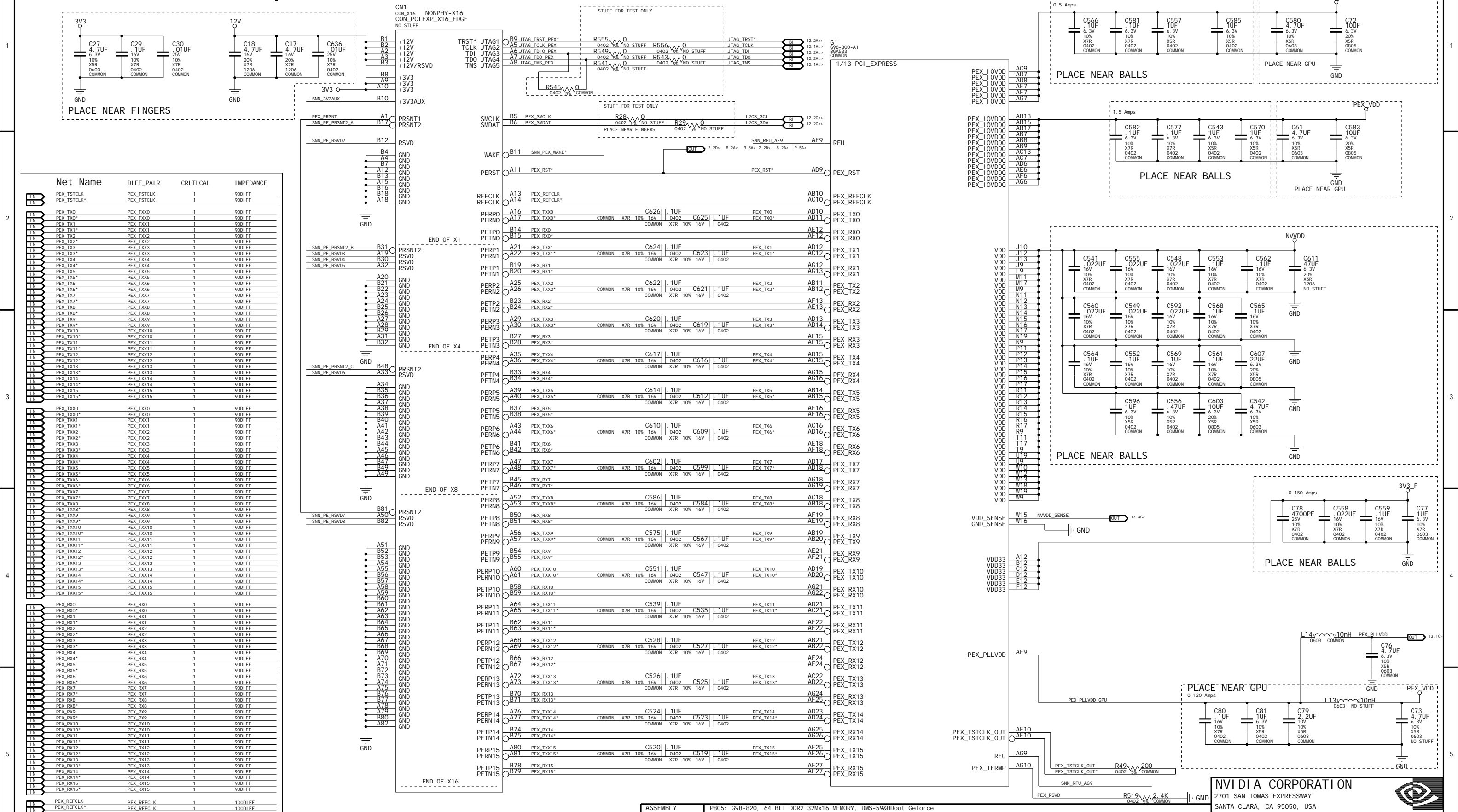


P805: G98, DDR2 MEMORY 32MX16 256MB DMS-59 HDOUT

- Page 1: P805 Overview
- Page 2: PCI EXPRESS INTERFACE
- Page 3: Frame Buffer Interface
- Page 4: Memory 1st Bank 0..31
- Page 5: Memory 1st Bank 32..63
- Page 6: DACA
- Page 7: DACC
- Page 8: VIDEO CONNECTORS: Mini DIN
- Page 9: TMDS Interface
- Page 10: TMDS Interface
- Page 11: Straps, Mechanical Parts
- Page 12: XTAL, GPIO, BIOS, FAN, JTAG, HDCP
- Page 13: Power Supply I: NVVDD, PLLVDD
- Page 14: Power Supply II: F3V3, 5V, DDC5V, FBVDDQ, PEX\_VDD
- Page 15: Basenet Report
- Page 16: Cref Part

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10805-base-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10805-0001-000	P805: G98-820, 64 BIT DDR2 32Mx16 MEMORY, DMS-59&HDout Geforce
2	SKU0502	600-50805-0502-000	P805: G98-820, 64 BIT DDR2 32MX16 MEMORY, MDS-59&HDout Quadro
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

## PAGE2: PCI Express Interface



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ASSEMBLY	P805: G98-820, 64 BIT DDR2 32Mx16 MEMORY, DMS-59&HDout Geforce
PAGE DETAIL	PCI EXPRESS INTERFACE

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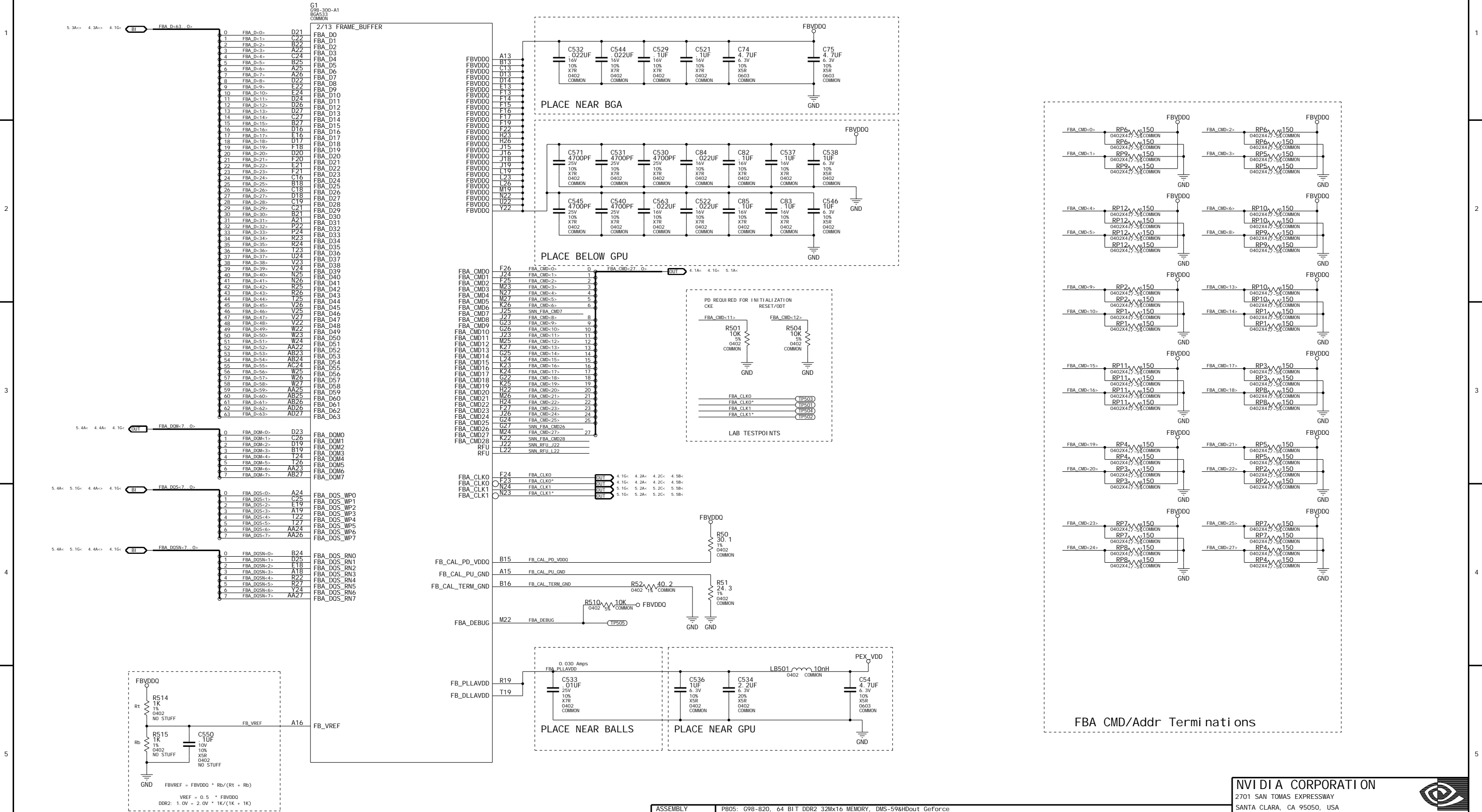
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NV_PN	600-10805-0001-000 C		
ID	p805	PAGE	2 OF 14
NAME	l bao	DATE	23-APR-2008

PAGE3: Frame Buffer Interface

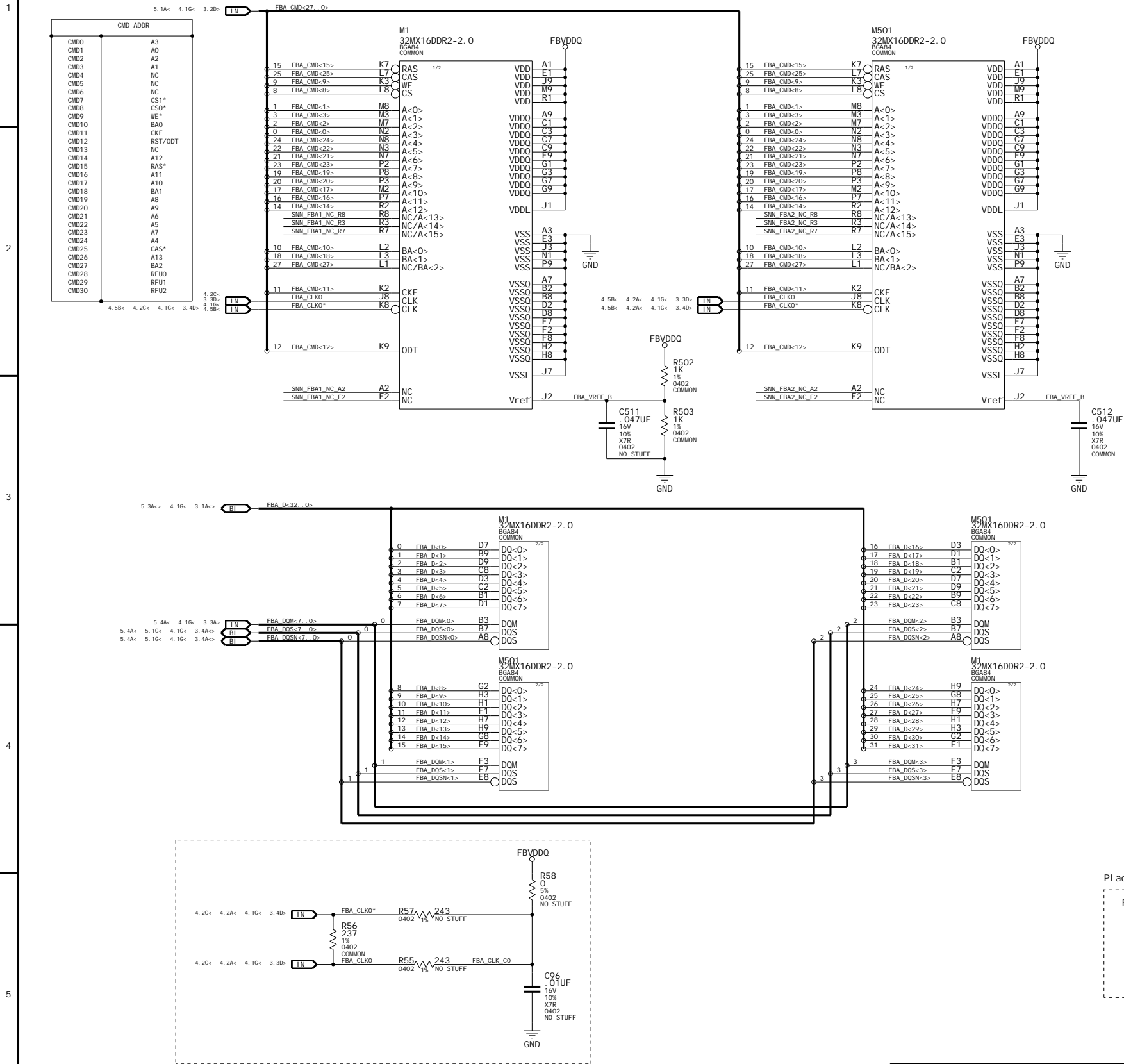
SIGNAL NAME	NV CRITICAL NET	IMPEDENCE
FBA_DEBUG	1	50OHM



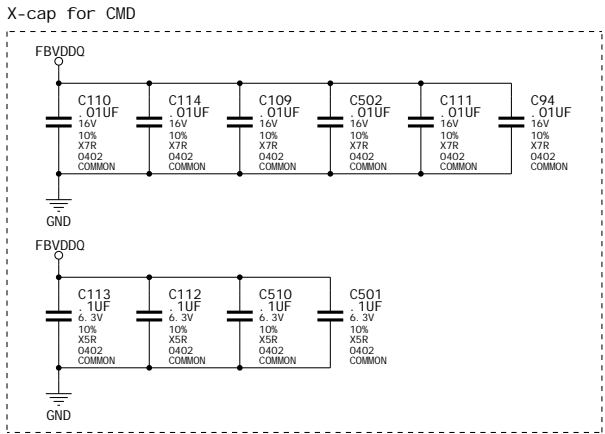
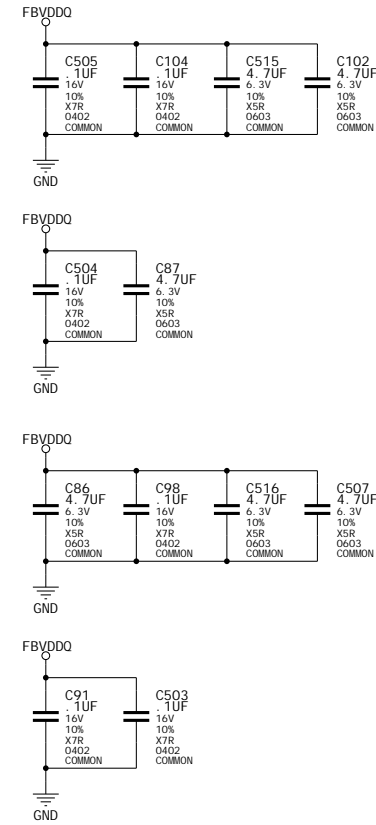
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NV_PN	600-10805-0001-000 C		
ID	p805	PAGE	3 OF 14
NAME	lba0	DATE	23-APR-2008

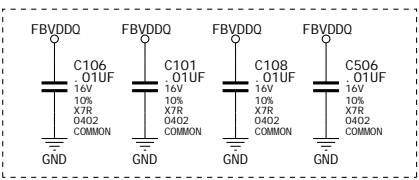
PAGE4: Memory 1st Bank 0..31



Net Name	DI FF_PAIR	CRITICAL	IMPEDANCE
FBA_CLK0	FBA_CLK0	1	100DI FF
FBA_CLK0*	FBA_CLK0	1	100DI FF
FBA_D<63..0>		2	50OHM
FBA_CMD<27..0>		2	50OHM
FBA_DQM<7..0>		2	50OHM
FBA_DQS<7..0>	FBA_DQS<0>	1	100DI FF
FBA_DQS<1>	FBA_DQS<1>	1	100DI FF
FBA_DQS<2>	FBA_DQS<2>	1	100DI FF
FBA_DQS<3>	FBA_DQS<3>	1	100DI FF



Place these caps next to plane transitions



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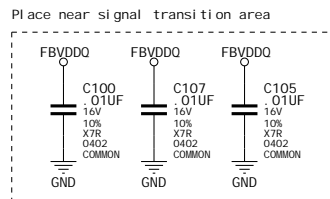
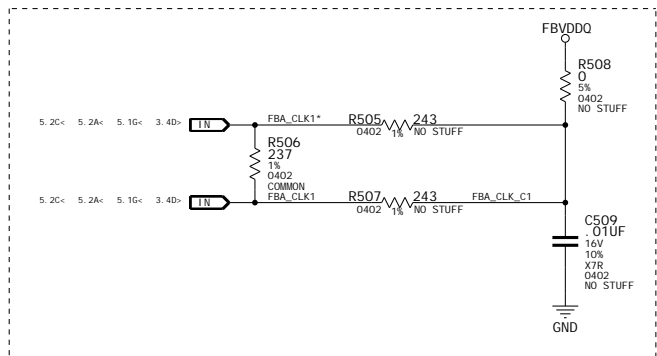
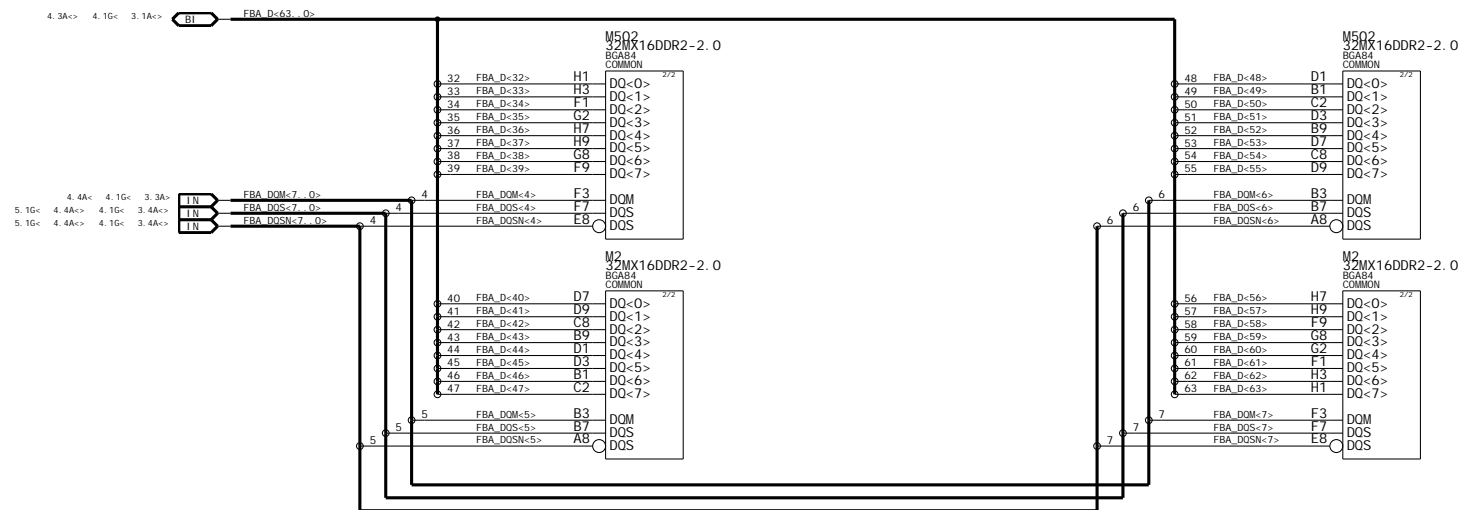
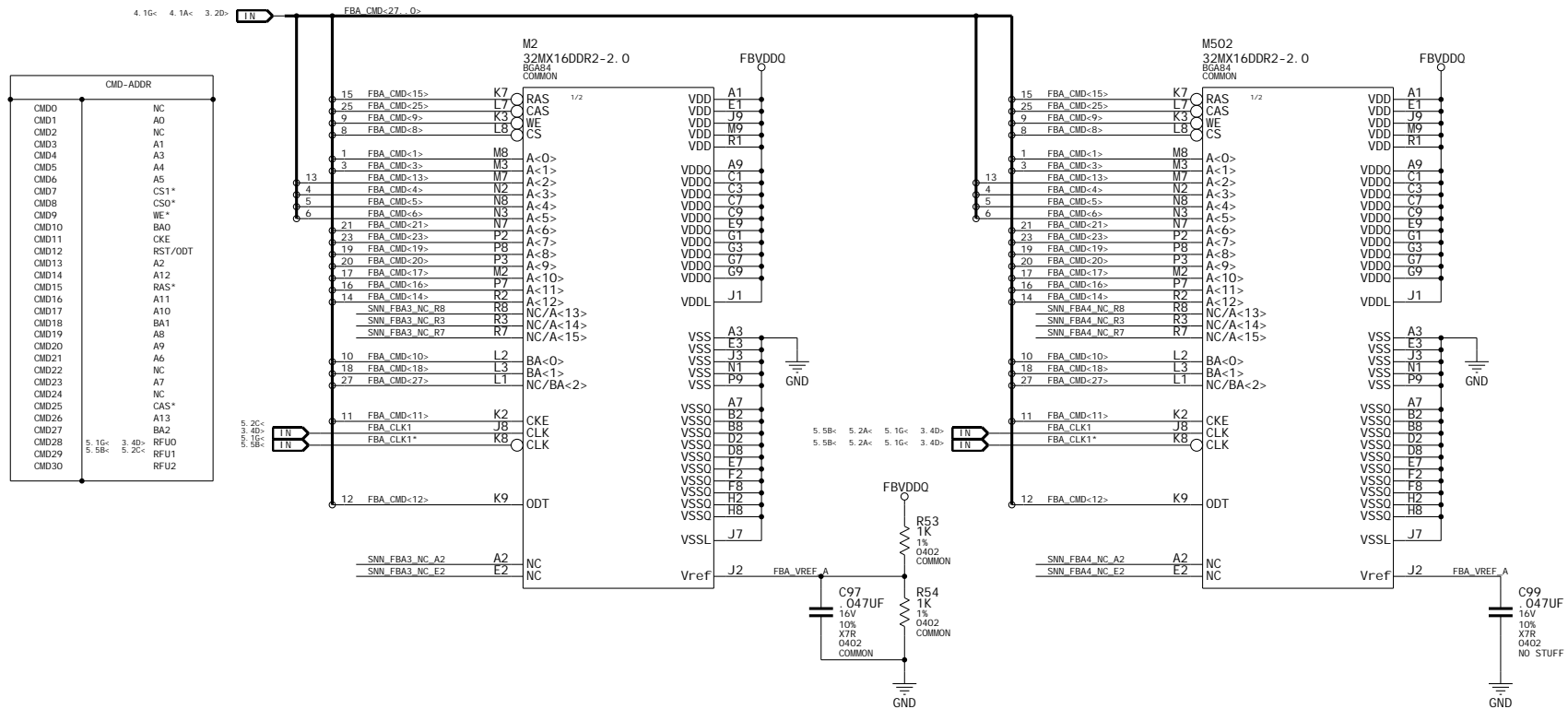
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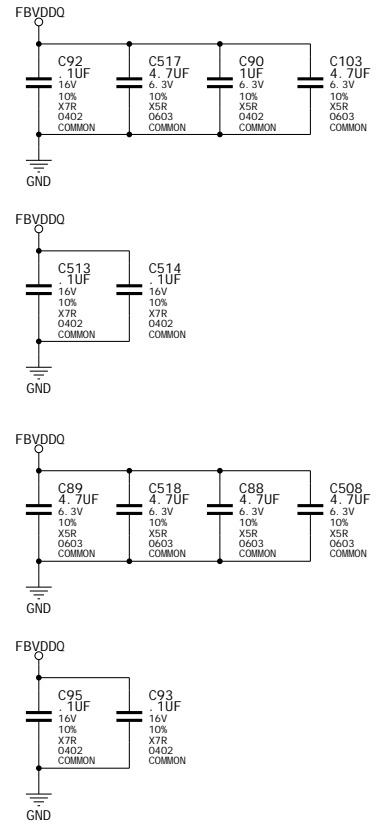


NV_PN	600-10805-0001-000 C		
ID	p805	PAGE	4 OF 14
NAME	tbao	DATE	23-APR-2008

PAGE5: Memory 1st Bank 32..63

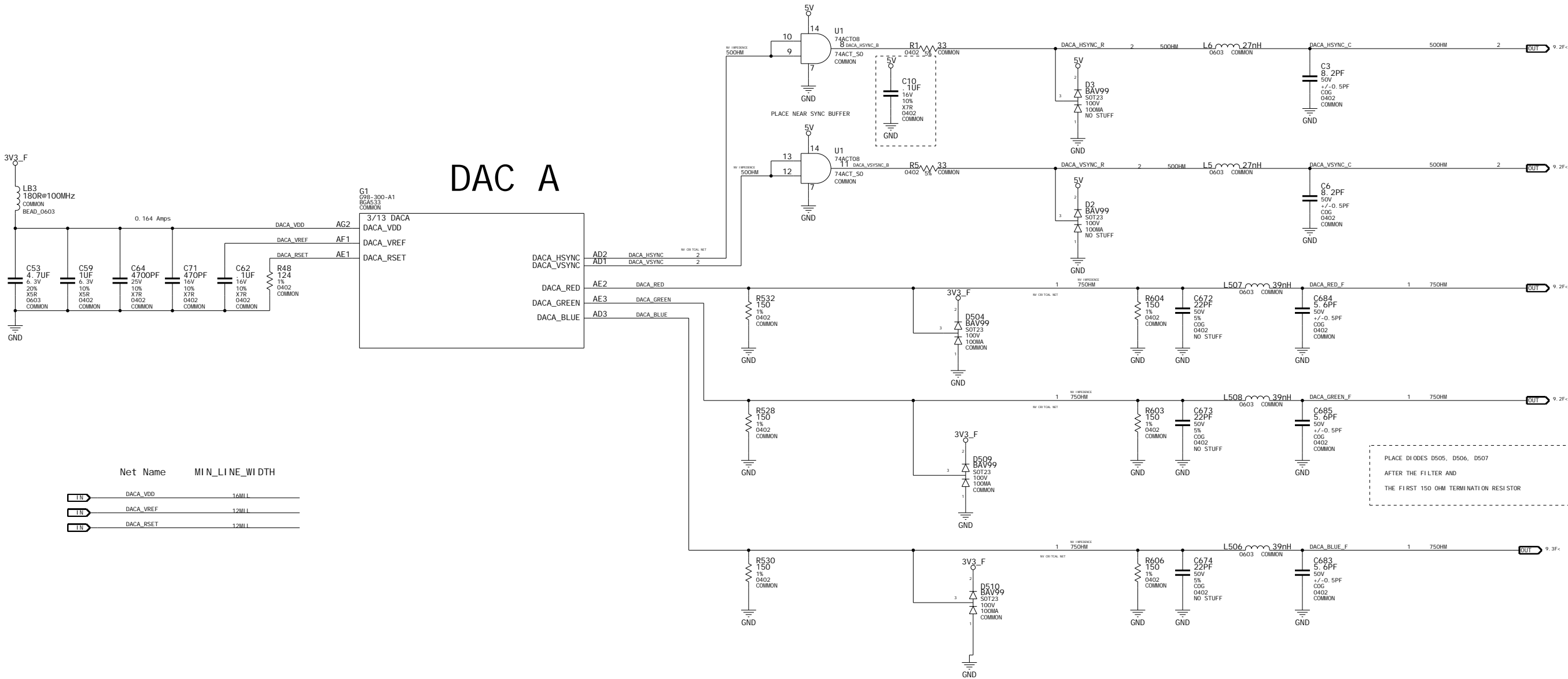


Net Name				DI FF_PAIR	CRITICAL	IMPEDANCE
				FBA_CLK1	1	100DI FF
				FBA_CLK1	1	100DI FF
				FBA_DQS<4>	1	100DI FF
				FBA_DQS<4>	1	100DI FF
				FBA_DQS<5>	1	100DI FF
				FBA_DQS<5>	1	100DI FF
				FBA_DQS<6>	1	100DI FF
				FBA_DQS<7>	1	100DI FF
				FBA_DQS<7>	1	100DI FF



Net Name	MIN LINE WIDTH
DACA_VDD	16MIL
DACA_VREF	12MIL
DACA_RSET	12MIL

DAC A



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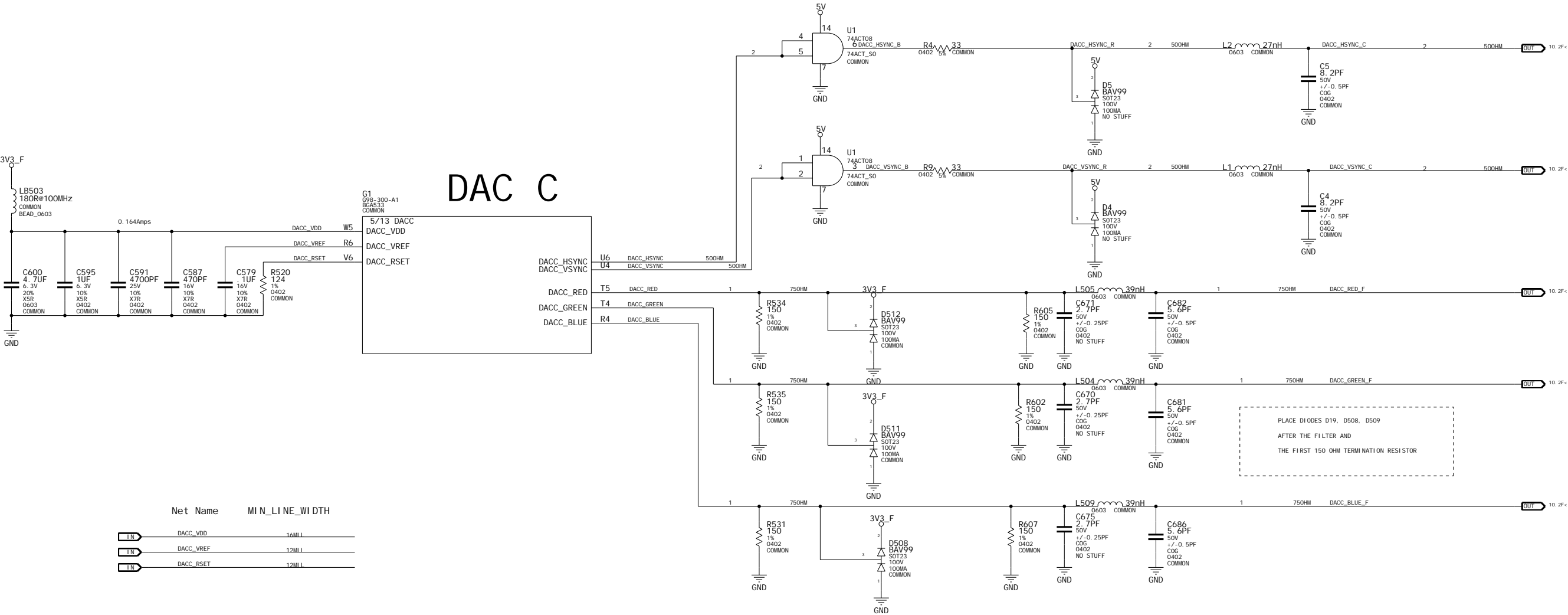
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ASSEMBLY	P805: G98-820, 64 BIT DDR2 32Mx16 MEMORY, DMS-59&Hdout GeForce
PAGE DETAIL	DACA

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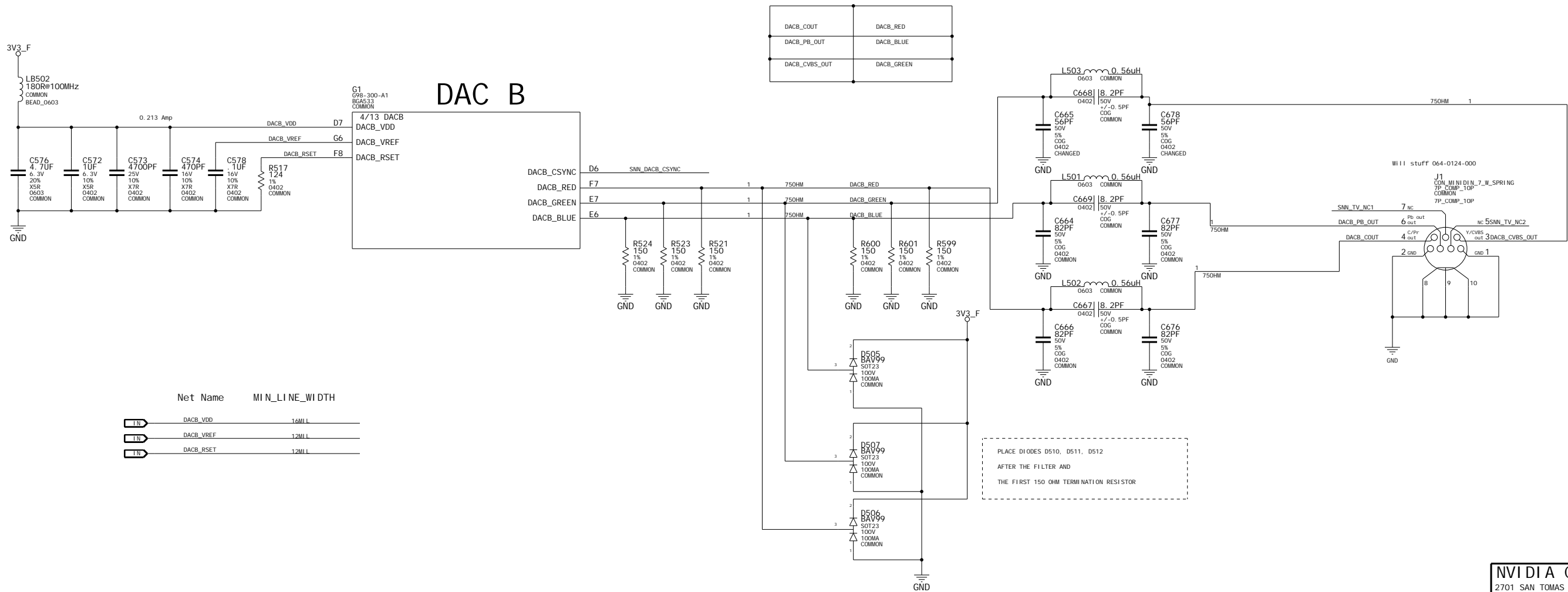
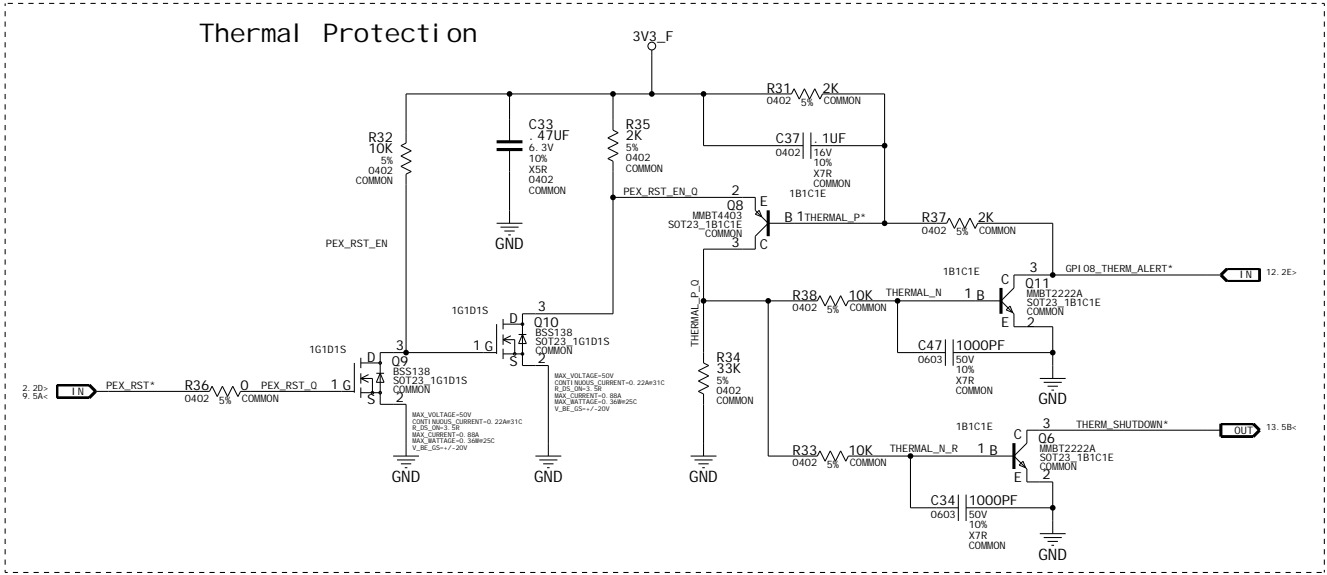
NV_PN	600-10805-0001-000	C
ID	p805	PAGE 6 OF 14
NAME	tbao	DATE 23-APR-2008



Net Name	MIN_LENGTH
DACC_VDD	16MIL
DACC_VREF	12MIL
DACC_RSET	12MIL

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PAGE8: DACB, 7 PIN MINI-DIN, THERMAL Protection



Net Name	MI N_LI N_E_WI DTH
DACB_VDD	14MIL
DACB_VREF	12MIL
DACB_RSET	12MIL

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NAME	tbao	DATE	23-APR-2008



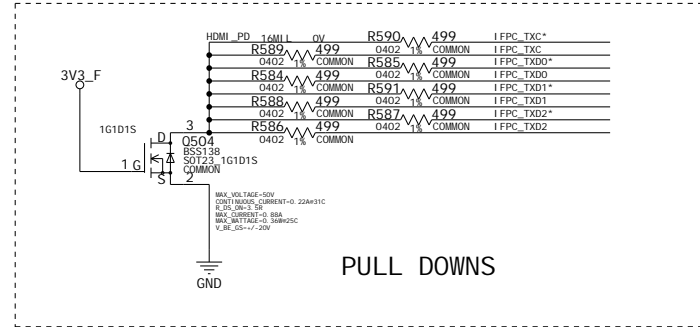
## 1

12

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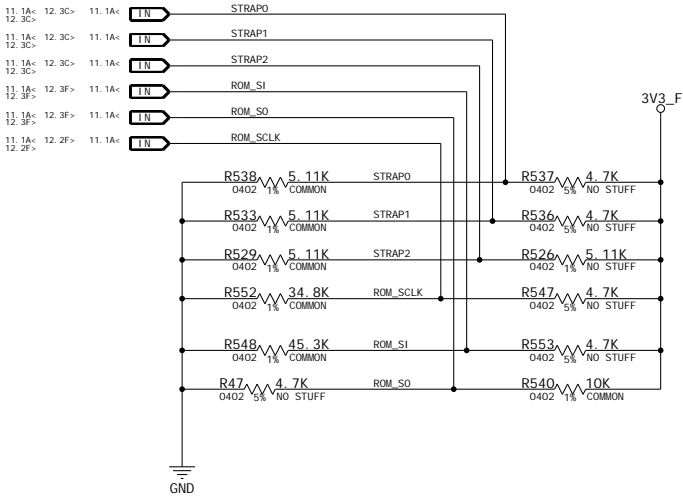
3

PAGE10: TMD5 I NTERFACE



PAGE11: Straps, Mechanical Parts

STRAPS



STRAPS

1. SUB\_VENDOR = 1 ( ROM PRESENT )  
= 0 ( NO ROM PRESENT)
2. DEVICE ID FOR GB1-64 = 0x06EE/0X06F9  
A) PCI\_DEV\_ID = [ 3..0 ] LSB = 0010  
B) PCI\_DEVID\_EXT = [1] 4TH BIT = 0
3. 3GIO\_PADCFG\_LUT\_ADDR[3..0] = 0000
4. TVMODE[2..0] = 001
5. RAMCFG[3..0] = 0000 16Mx16 DDR2 64 BIT ELPIDA  
= 0001 16Mx16 DDR2 64 BIT SAMSUNG, MICRON  
= 0010 16Mx16 DDR2 64 BIT QIMONDA  
= 0011 16Mx16 DDR2 64 BIT HYNIX  
= 0100 32Mx16 DDR2 64 BIT ELPIDA  
= 0101 32Mx16 DDR2 64 BIT SAMSUNG  
= 0110 32Mx16 DDR2 64 BIT QIMONDA  
= 0111 32Mx16 DDR2 64 BIT HYNIX
5. USER[3..0] = 0000

MULTI LEVEL STRAP DECODE ACCORDING TO  
TERMINATION RESISTANCE/VOLTAGE

TERMINATION RESISTANCE	TERMINATION VOLTAGE	
	3V3 [3..0]	GND [3..0]
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

MULTI LEVEL STRAPS

R511 = 40.2K AND R512 = 40.2K

RAM_CFG[3:0]					
256MB					
ROM_SI	0	RAM_CFG_0	0000	32MX16 DDR2 ELPIDA	0100 32MX16 DDR2 NANYA
	1	RAM_CFG_1	0001	RESERVED	0101 32MX16 DDR2 SAMSUNG
	2	RAM_CFG_2	0010	RESERVED	0110 32MX16 DDR2 QIMONDA
	3	RAM_CFG_3	0011	RESERVED	0111 32MX16 DDR2 HYNIX

ROM_SO	0	TVMODE_0	TVMODE[2:0] 000 -----	DEFAULT	ROM_SO NOT REQUIRED TO BE SET UP IN VBIOS
	1	TVMODE_1			
	2	TVMODE_2	XCLK_277 1 -----	DEFAULT	
	3	XCLK_277			

ROM_SCLK	0	PEX_PLL_EN_TERM100	PEX_PLL_EN_TERM100 0 -----	DEFAULT	SUB_VENDOR 1 -----
	1	SLOT_CLK_CFG			DEFAULT
	2	SUB_VENDOR	SLOT_CLK_CFG 1 -----	DEFAULT	PCI_DEVID_EXT 0 -----
	3	PCI_DEVID_EXT			DEFAULT

STRAP0	0	USER_0	USER[3:0] 0000 -----	DEFAULT (DESKTOP)
	1	USER_1		
	2	USER_2		
	3	USER_2		

3GIO_PADCFG_LUT_ADDR[3:0]					
0000 ----- DEFAULT (DESKTOP)					
STRAP1	0	3GIO_PADCFG_LUT_ADDR_0			
	1	3GIO_PADCFG_LUT_ADDR_1			
	2	3GIO_PADCFG_LUT_ADDR_2			
	3	3GIO_PADCFG_LUT_ADDR_3			

PCI_DEVID_0					
STRAP2	0	PCI_DEVID_0	-----	0	PCI_DEVID[2:0] TO BE SET TO ALL 0'S
	1	PCI_DEVID_1	-----	0	AND WILL BE CONTROLLED BY VBIOS
	2	PCI_DEVID_2	-----	0	
	3	PCI_DEVID_3	-----	0	THIS IS THE ONLY BIT DRIVEN BY THE STRAPS

MEC4  
1031-1LP\_4400RPM  
NOT IN  
COMMON

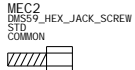
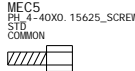
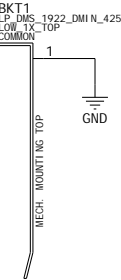
COOLING SOLUTION

No connected mounting pins

COOLING SOLUTION

No connected mounting pins

MEC1  
1M31-7  
NOT IN  
NO STUFF



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NV\_PN 600-10805-0001-000 C

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PAGE12: XTAL, GPIO, BIOS, FAN, JTAG, HDCP

1

2

3

4

5

Net Name		CRITICAL	IMPEDANCE
XTALIN	XTALOUT	1	50OHM
		1	50OHM

Net Name		MIN_LINewidth	VOLTAGE
GPU_PLLVDD			1.1V

12.1A<> 2.1E<> 12.1A<> 2.1E<>  
12.2A<> 2.1E<> 12.2A<> 2.1E<>  
12.2A<> 2.1E<> 12.2A<> 2.1E<>  
12.2A<> 2.1E<> 12.2A<> 2.1E<>

JTAG Header

J501  
HDR\_2F4  
FEMALE  
1.274MM  
KEY6: JTAG\_SMALL  
NO STUFF

JTAG\_TMS 1 TMS  
JTAG\_TDI 3 TDI  
JTAG\_TDO 7 TDO  
JTAG\_TRST\* 2 JTAG\_TRST\*  
KEY 4  
TCK 8 JTAG\_TCLK

3V3\_F

C615  
1UF  
6.3V  
10%  
XSR  
0402  
COMMON

GND

GND

GND

3V3\_F

2.1E<> 2.1E<>

GND

GND

GND

GND

GND

GND

GND

GND

GND

GND

GND

GND

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GND

GND

GND

(TP506) THERMDC

(TP507) THERMDA

JTAG\_TCLK

JTAG\_TMS

JTAG\_TDI

JTAG\_TDO

JTAG\_TRST\*

12CS\_SCL

12CS\_SDA

STRAP0

STRAP1

STRAP2

STRAP\_REF\_3V3

STRAP\_REF\_MIOB

SPDIF

RFU

RFU

RFU

RFU

RFU

RFU

RFU

RFU

RFU

RFU

RFU

RFU

RFU

RFU

RFU

RFU

G1

G98-300-A1

8GA533

COMMON

9/13 12C\_GPIO\_THERM\_JTAG

12CA\_SCL

12CA\_SDA

12CB\_SCL

12CB\_SDA

12CC\_SCL

12CC\_SDA

12CD\_SCL

12CD\_SDA

12CE\_SCL

12CE\_SDA

GPIO0

GPIO1

GPIO2

GPIO3

GPIO4

GPIO5

GPIO6

GPIO7

GPIO8

GPIO9

GPIO10

GPIO11

GPIO12

GPIO13

GPIO14

GPIO15

GPIO16

GPIO17

GPIO18

GPIO19

GPIO20

GPIO21

GPIO22

GPIO23

GPIO24

GPIO25

G1

G98-300-A1

8GA533

COMMON

11/13 MISC

STRAP0

STRAP1

STRAP2

STRAP\_REF\_3V3

STRAP\_REF\_MIOB

SPDIF

RFU

RFU

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RFU

RFU

G1

G98-300-A1

8GA533

COMMON

12/13 XTAL\_PLL

PLLVD

VID\_PLLVD

SP\_PLLVD

XTALSSIN

XTALSSIN

XTALIN

XTALIN

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

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XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

G1

G98-300-A1

8GA533

COMMON

11/13 MISC

STRAP0

STRAP1

STRAP2

STRAP\_REF\_3V3

STRAP\_REF\_MIOB

SPDIF

RFU

RFU

RFU

RFU

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RFU

RFU

G1

G98-300-A1

8GA533

COMMON

12/13 XTAL\_PLL

PLLVD

VID\_PLLVD

SP\_PLLVD

XTALSSIN

XTALSSIN

XTALIN

XTALIN

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

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XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

G1

G98-300-A1

8GA533

COMMON

11/13 MISC

STRAP0

STRAP1

STRAP2

STRAP\_REF\_3V3

STRAP\_REF\_MIOB

SPDIF

RFU

RFU

RFU

RFU

RFU

RFU

RFU

RFU

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RFU

G1

G98-300-A1

8GA533

COMMON

12/13 XTAL\_PLL

PLLVD

VID\_PLLVD

SP\_PLLVD

XTALSSIN

XTALSSIN

XTALIN

XTALIN

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

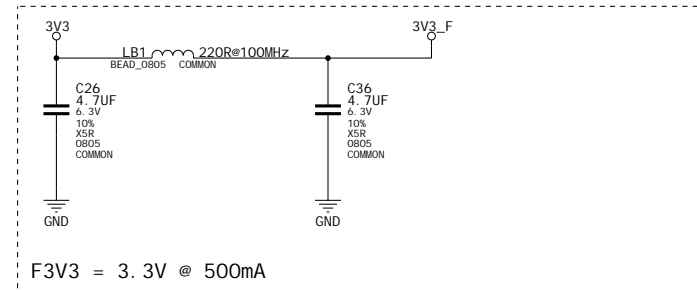
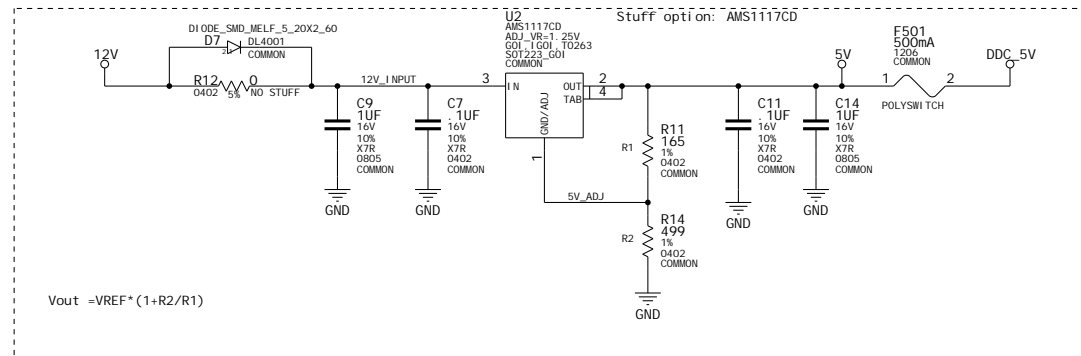
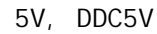
XTALOUT

XTALOUT



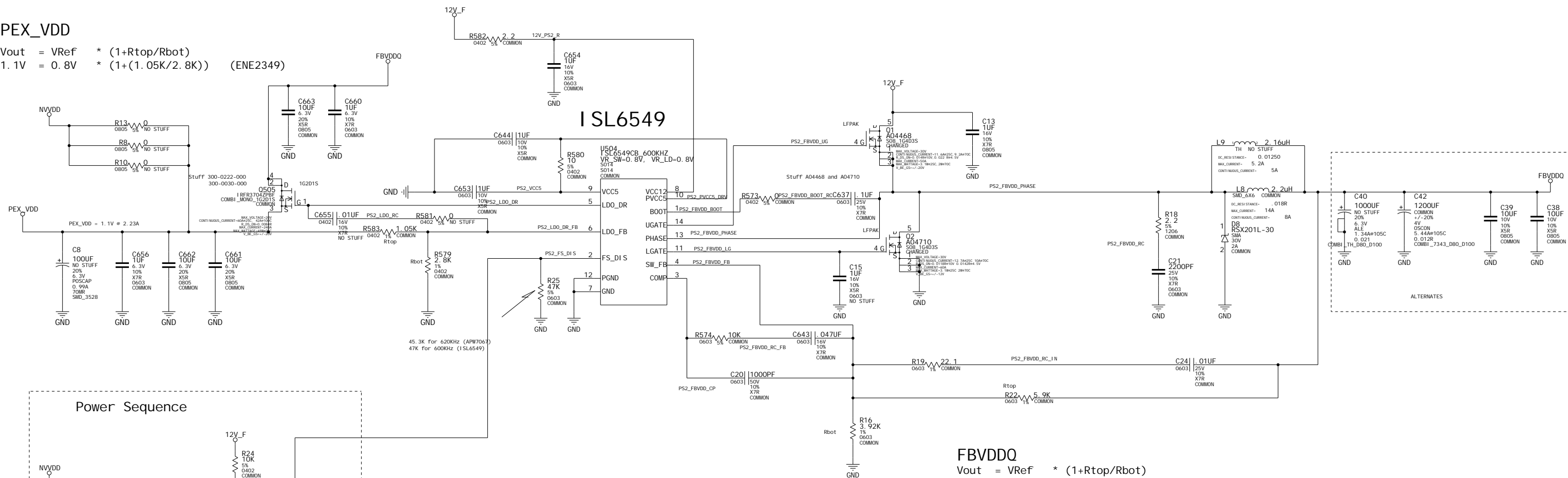
PAGE14: Power Supply II: 5V, DDC5V, F3V3, FBVDDQ, PEX\_VDD

Net	Name	MI_N_LI_NE_WI_DTH	CURRENT	VOLTAGE
5V0	5V	12MIL	0.25A	5V
DDC_5V0	DDC_5V	12MIL	0.2A	5V
3V3_F0	3V3_F	12MIL	3A	3.3V
3V30	3V3	36MIL		3.3V
FBVDD00	FBVDD0	36MIL	3A	2.0V

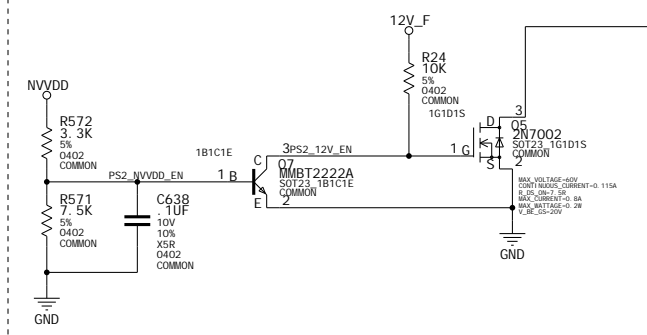


## PEX\_VDD

$$\begin{aligned} V_{out} &= V_{Ref} * (1 + R_{top}/R_{bot}) \\ 1.1V &= 0.8V * (1 + (1.05K/2.8K)) \quad (ENE2349) \end{aligned}$$



## Power Sequence



## FBVDDQ

Vout	=	VRef	*	(1+Rtop/Rbot)	
1.800V	=	0.8V	*	(1+(5.9k/4.75k))	(ISL6549)
2.000V	=	0.8V	*	(1+(5.9k/3.92k))	(ISL6549)
2.156V	=	0.8V	*	(1+(5.9k/3.4k))	(ISL6549)

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