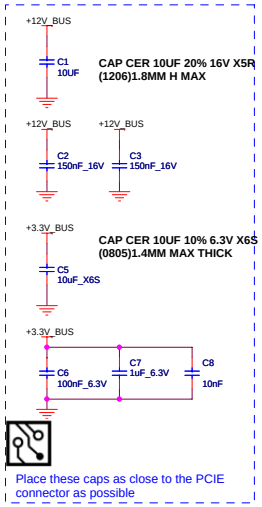
PCI-EXPRESS EDGE CONNECTOR



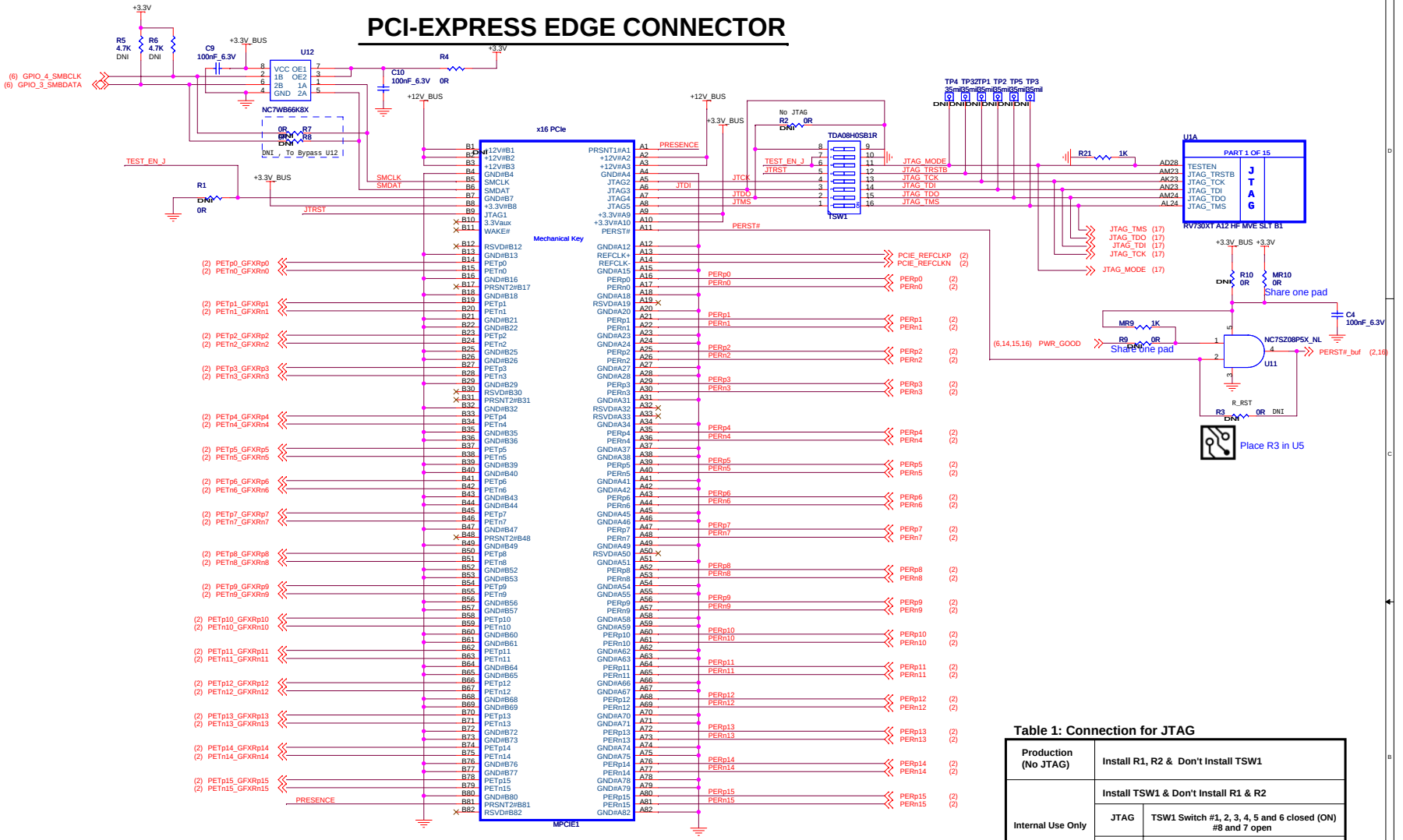


Table 1: Connection for JTAG

Production (No JTAG)	**Install R1, R2 & Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R1 & R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)**

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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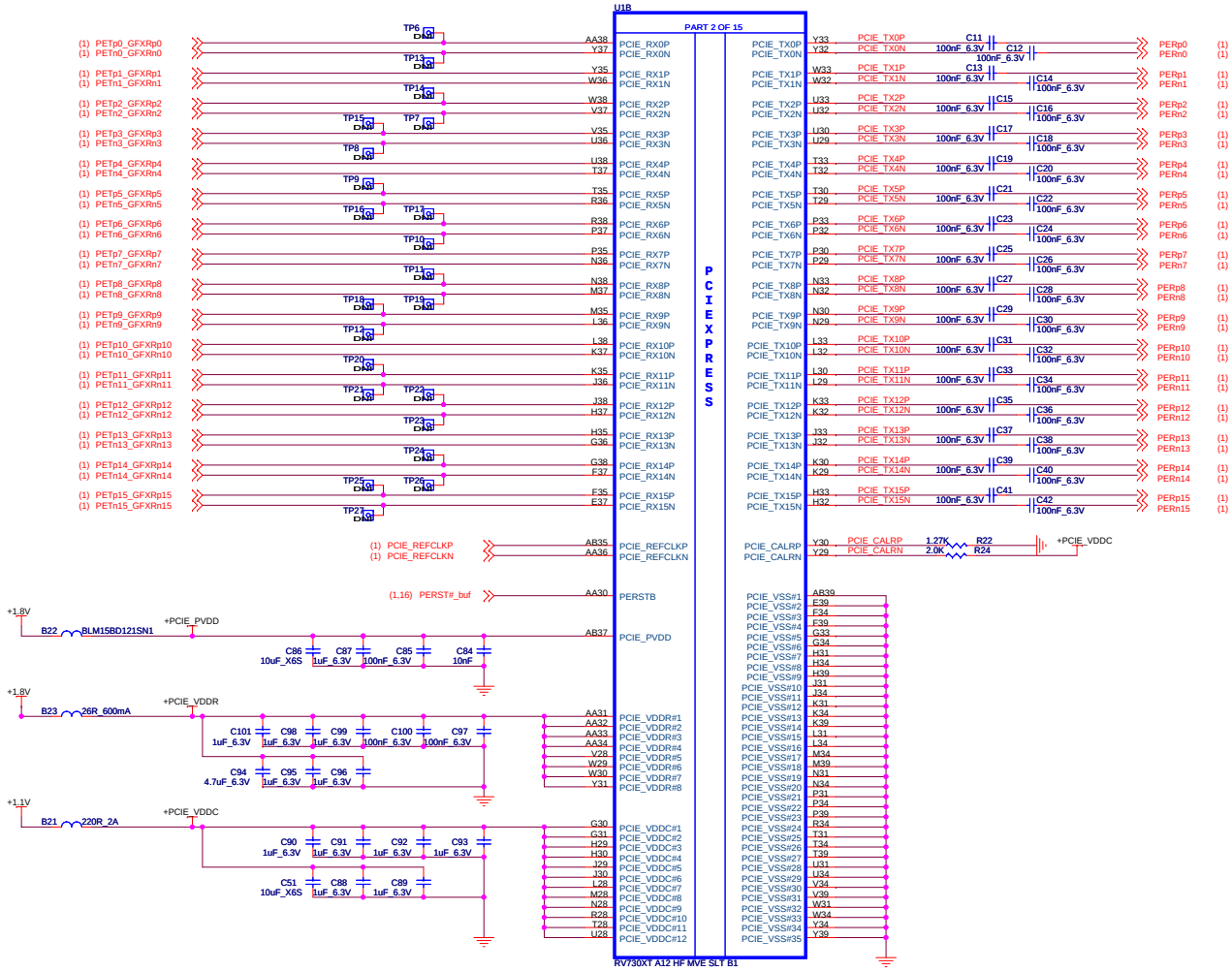
(2) RV730 PCIE Interface

NOTE: some of the PCIE testpoints will
be available trought via on traces.



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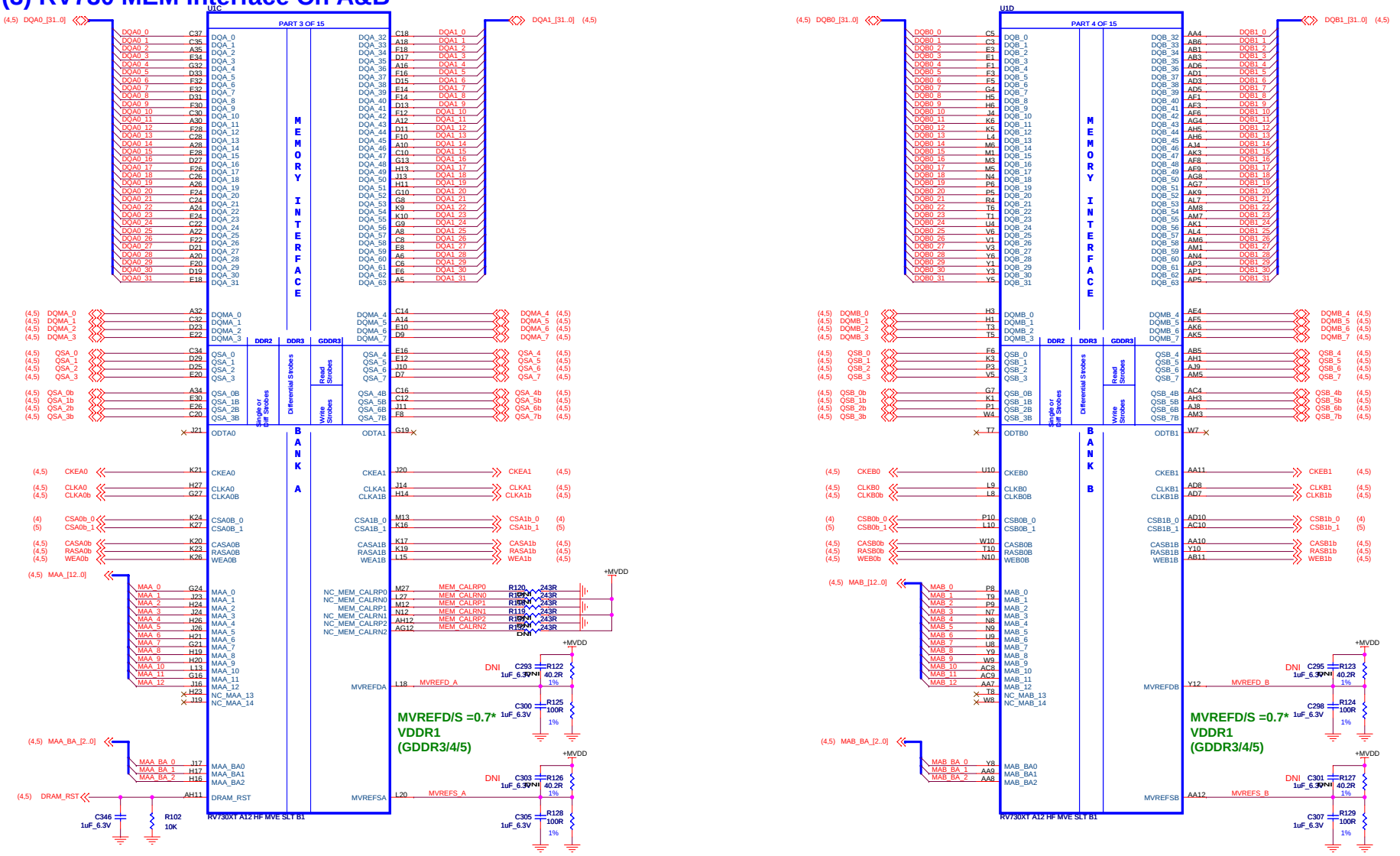
(3) RV730 MEM Interface Ch A&B



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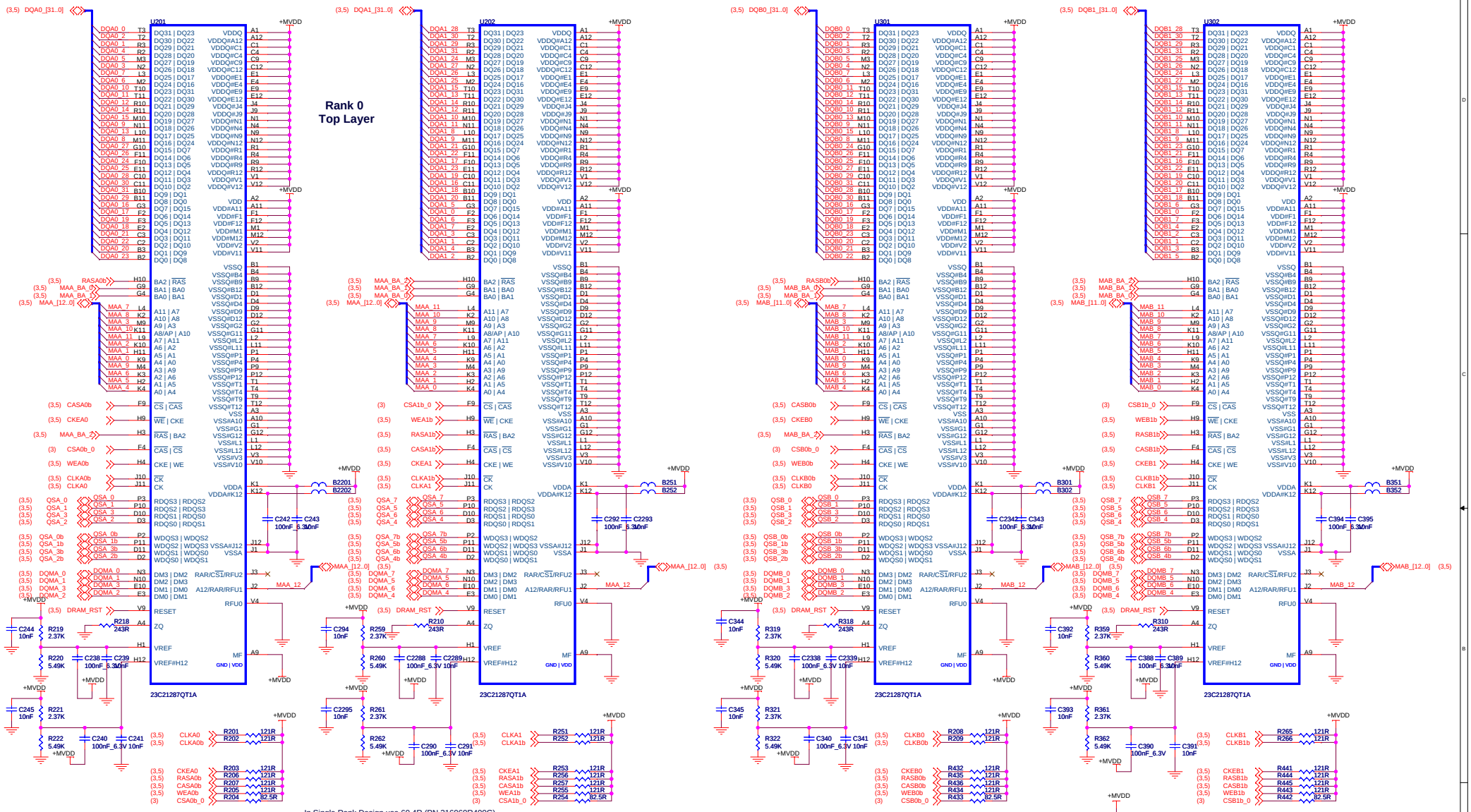
(4) GDDR3 Memory Channel A&B Bank 0



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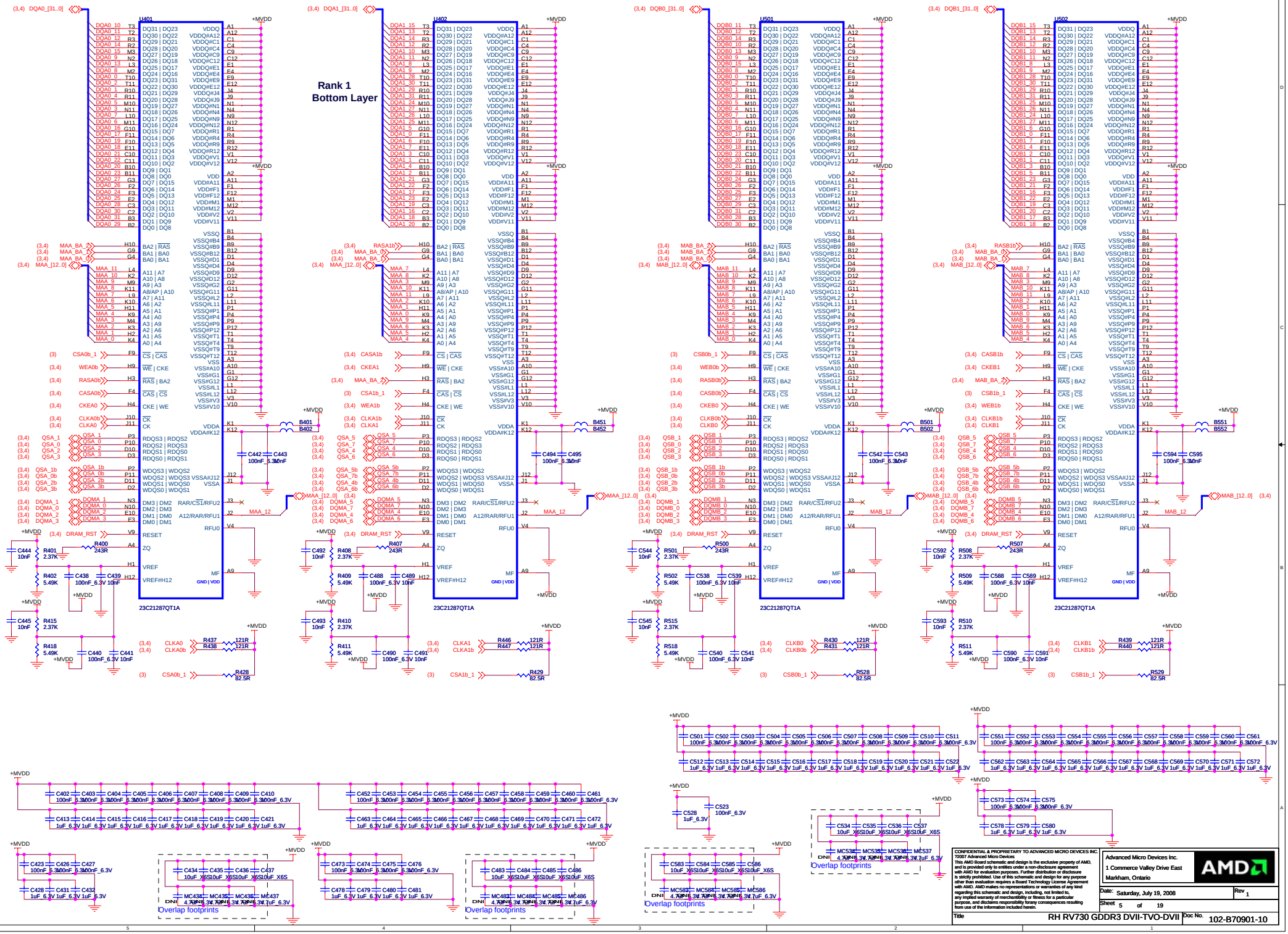
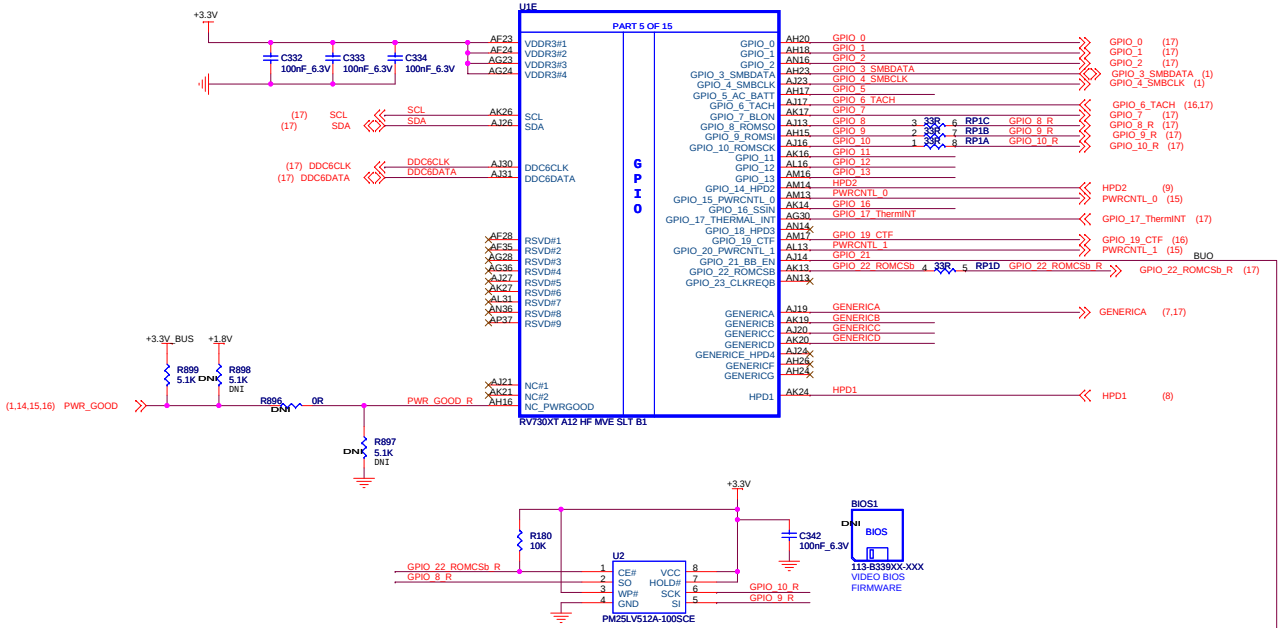
(5) GDDR3 Memory Channel A&B Bank 1

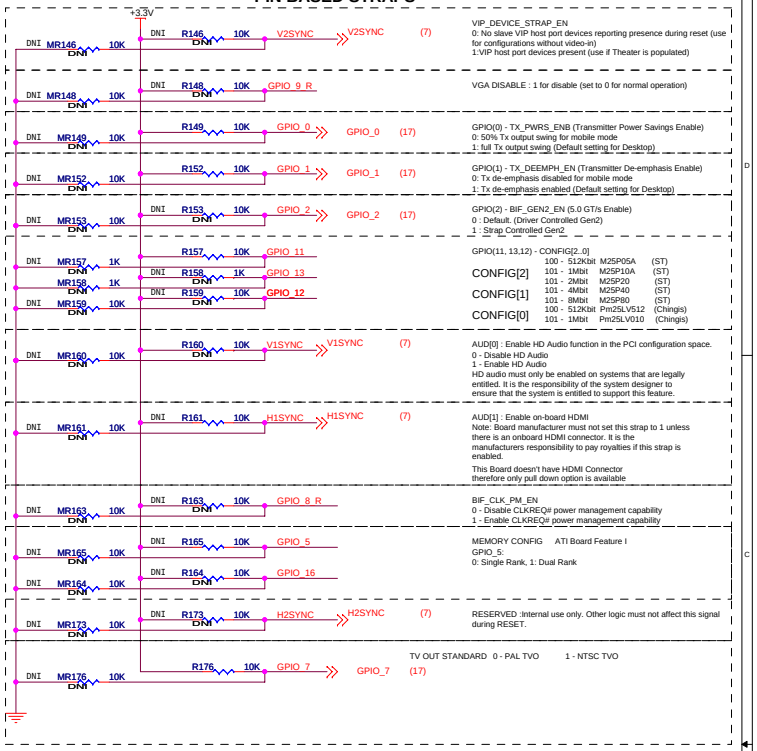


(06) RV730 GPIOs Strap CF XTAL

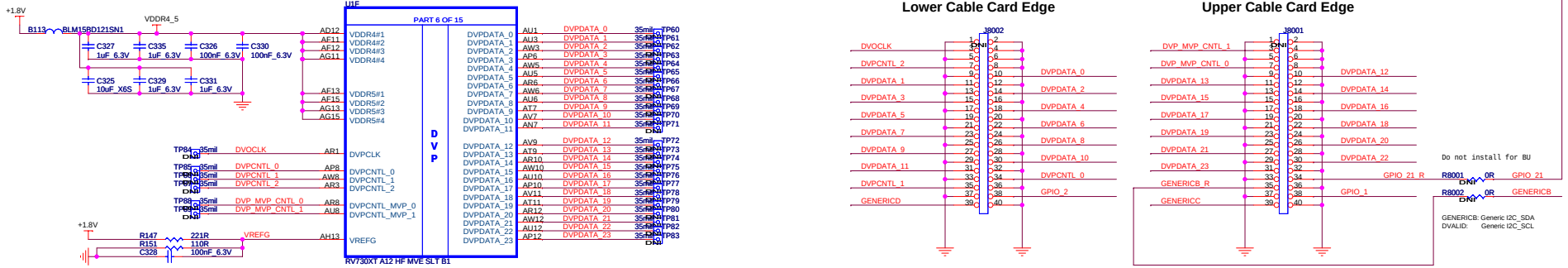


PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

PIN BASED STRAPS



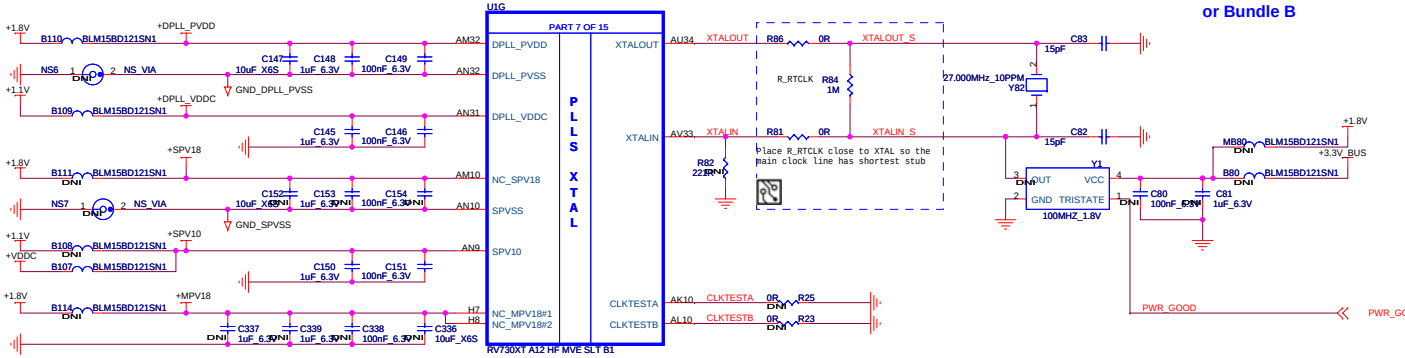
CrossFire Card-Edge



Lower Cable Card Edge

Upper Cable Card Edge

or Bundle B **or Bundle A (closer to the bracket)**



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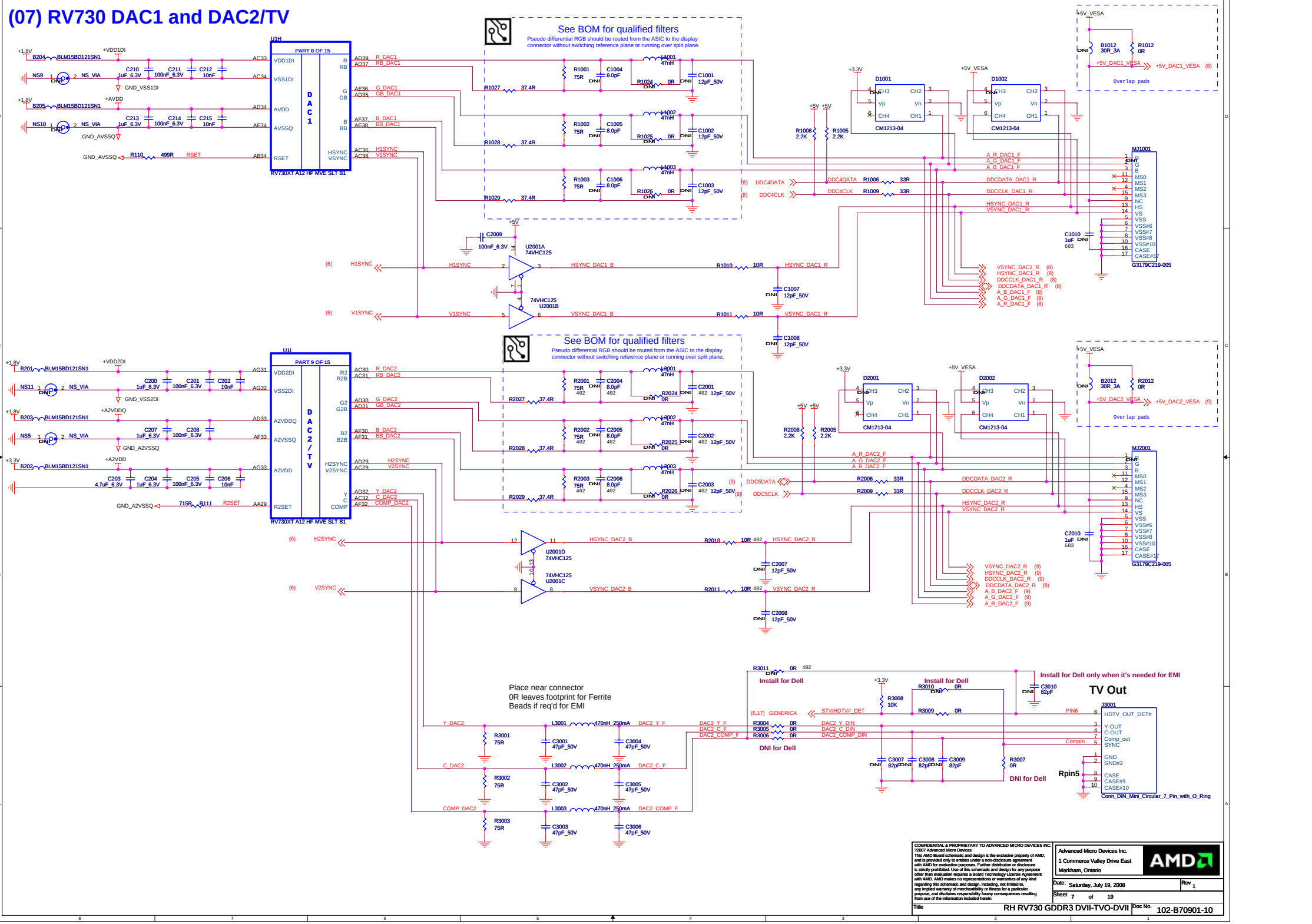
(07) RV730 DAC1 and DAC2/TV



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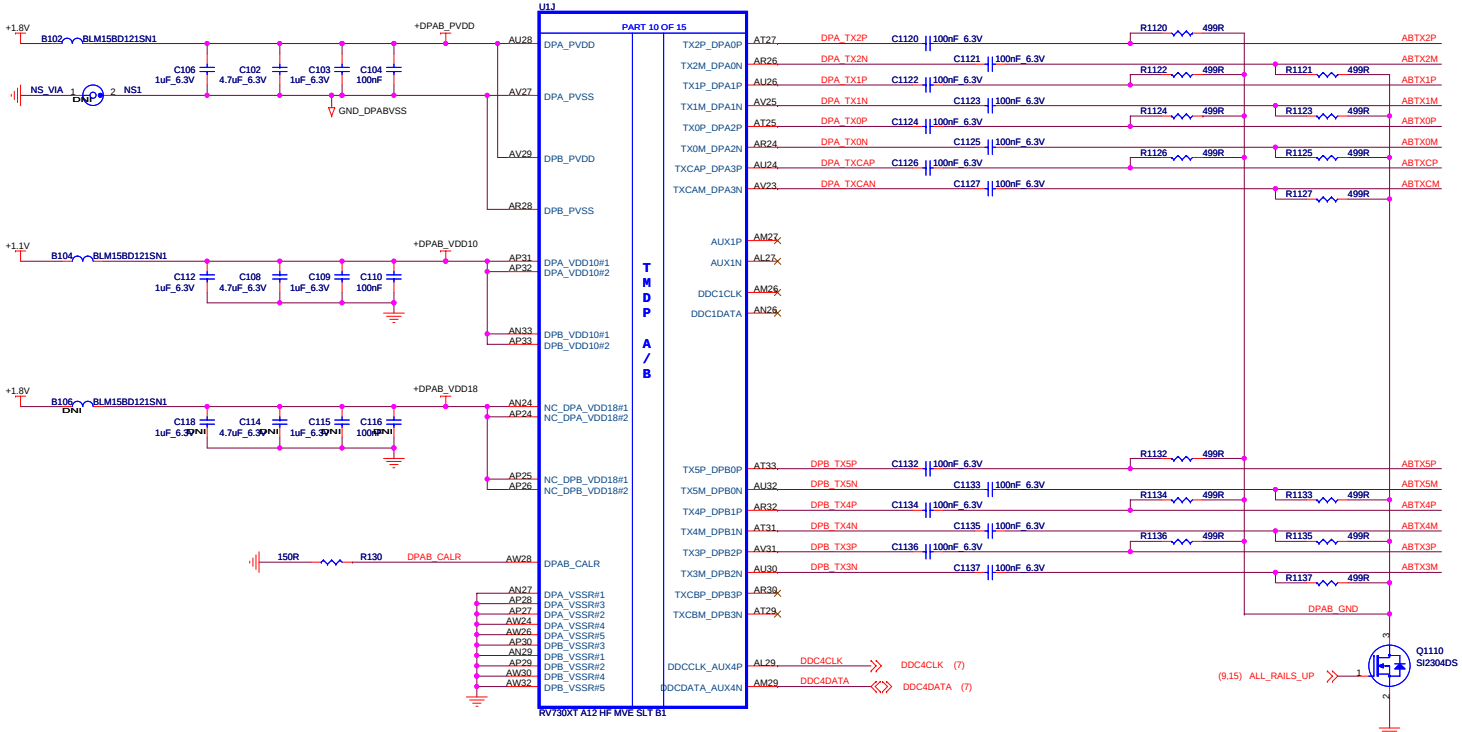
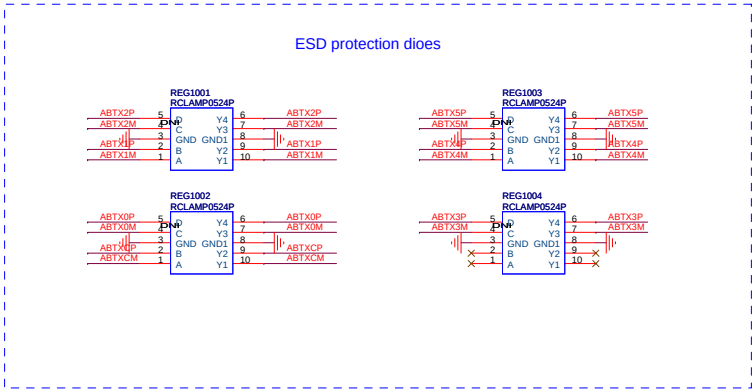
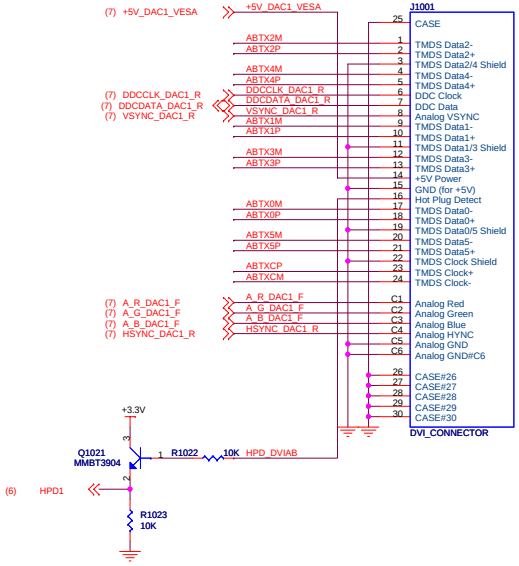
(08) RV730 TMDS A&B







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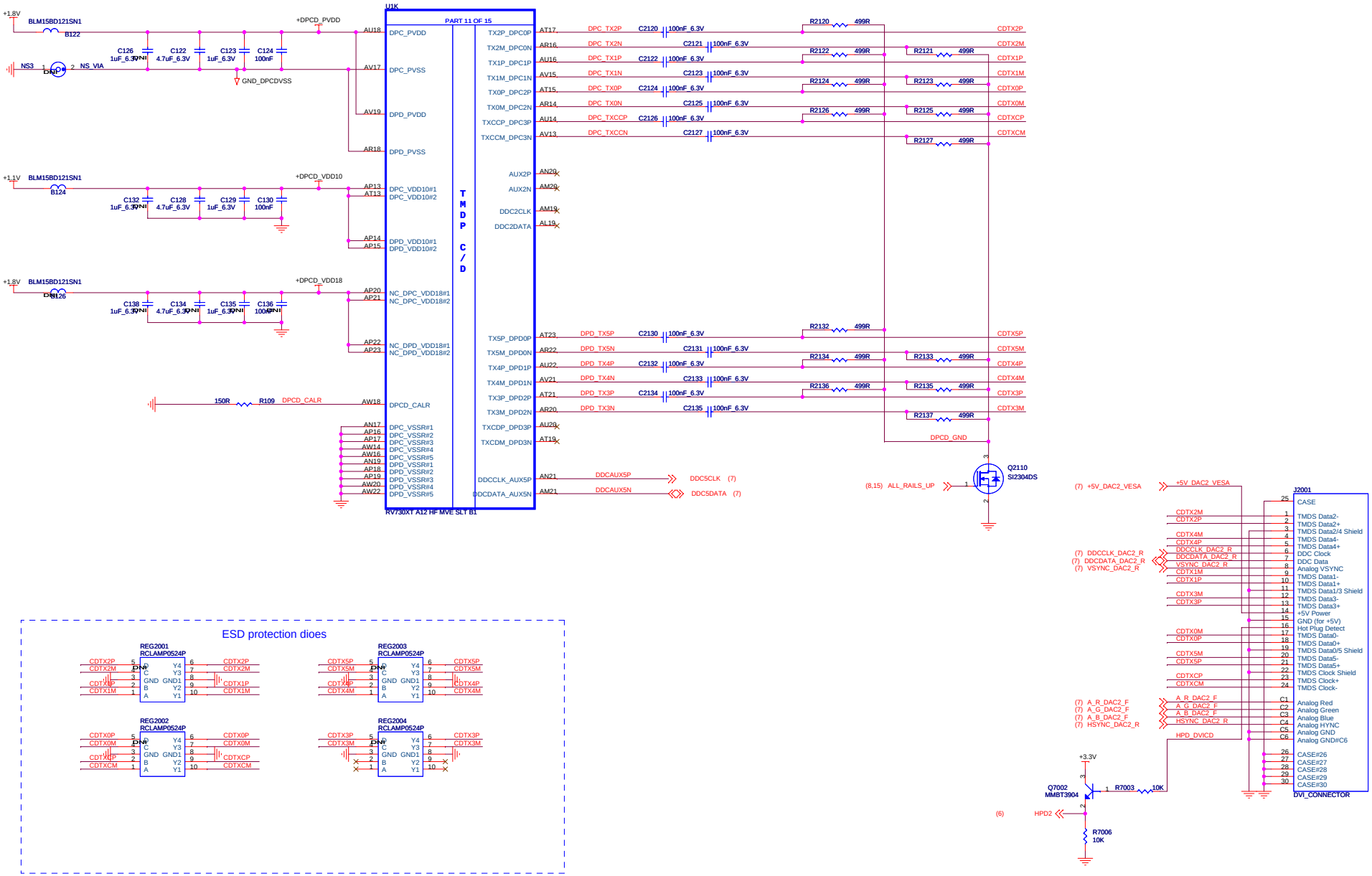
(09) RV730 Display Port C&D



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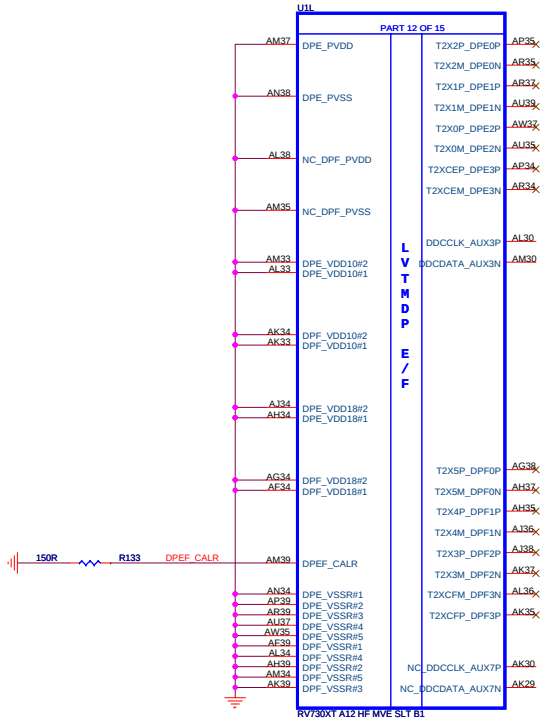
(10) No Connect E&F



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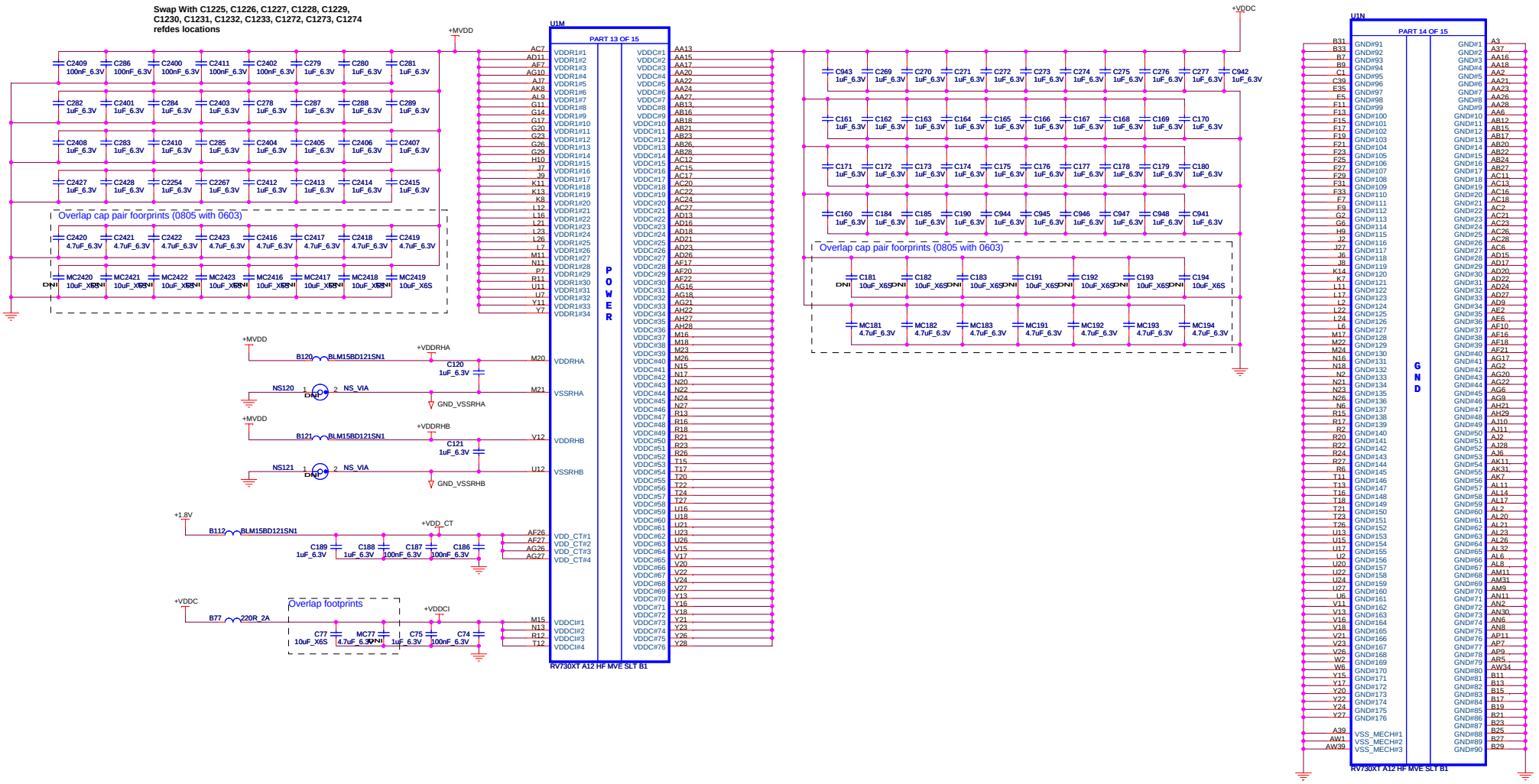
(11) RV730 Power & GND



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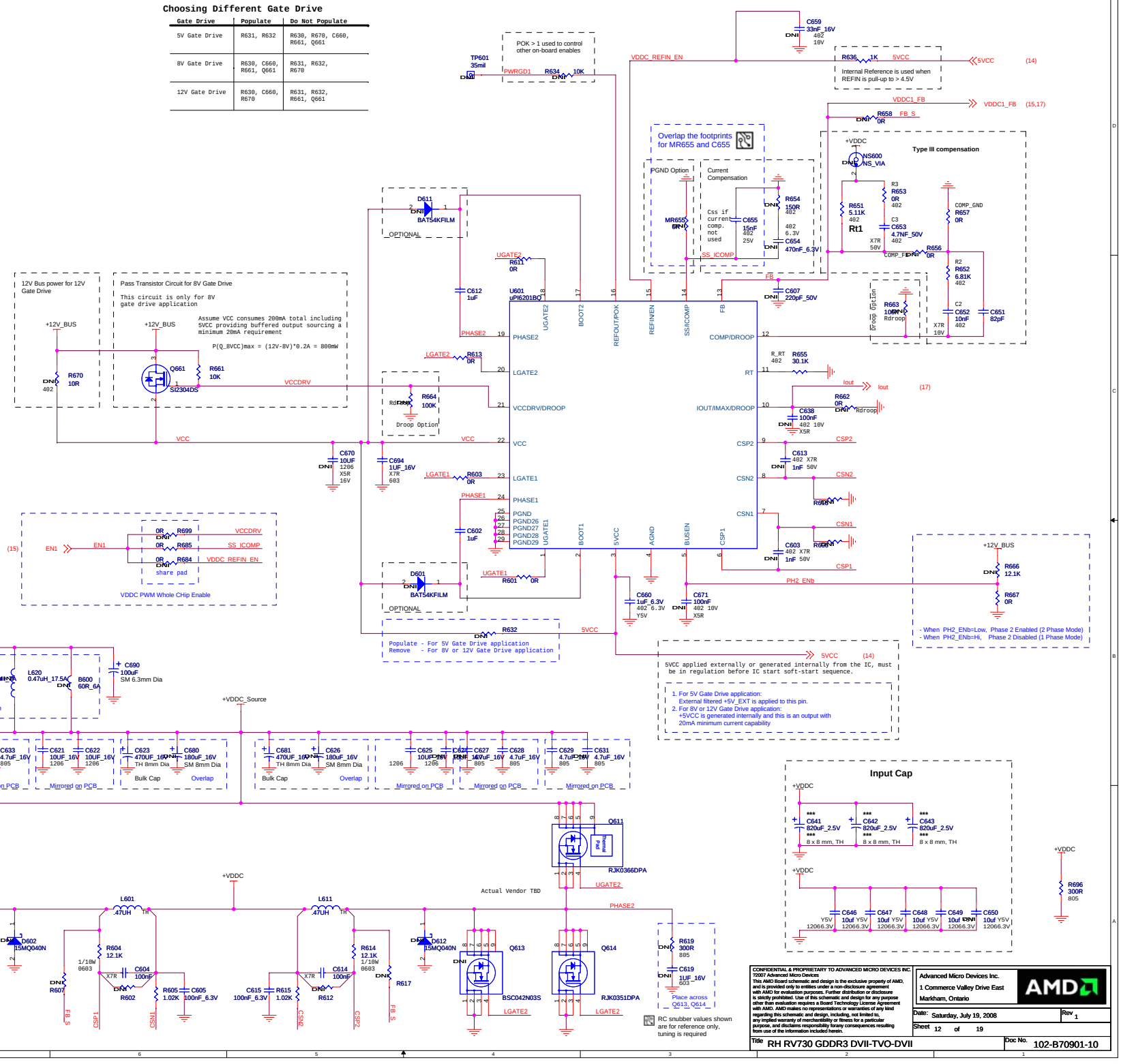
(12) VDDC

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661



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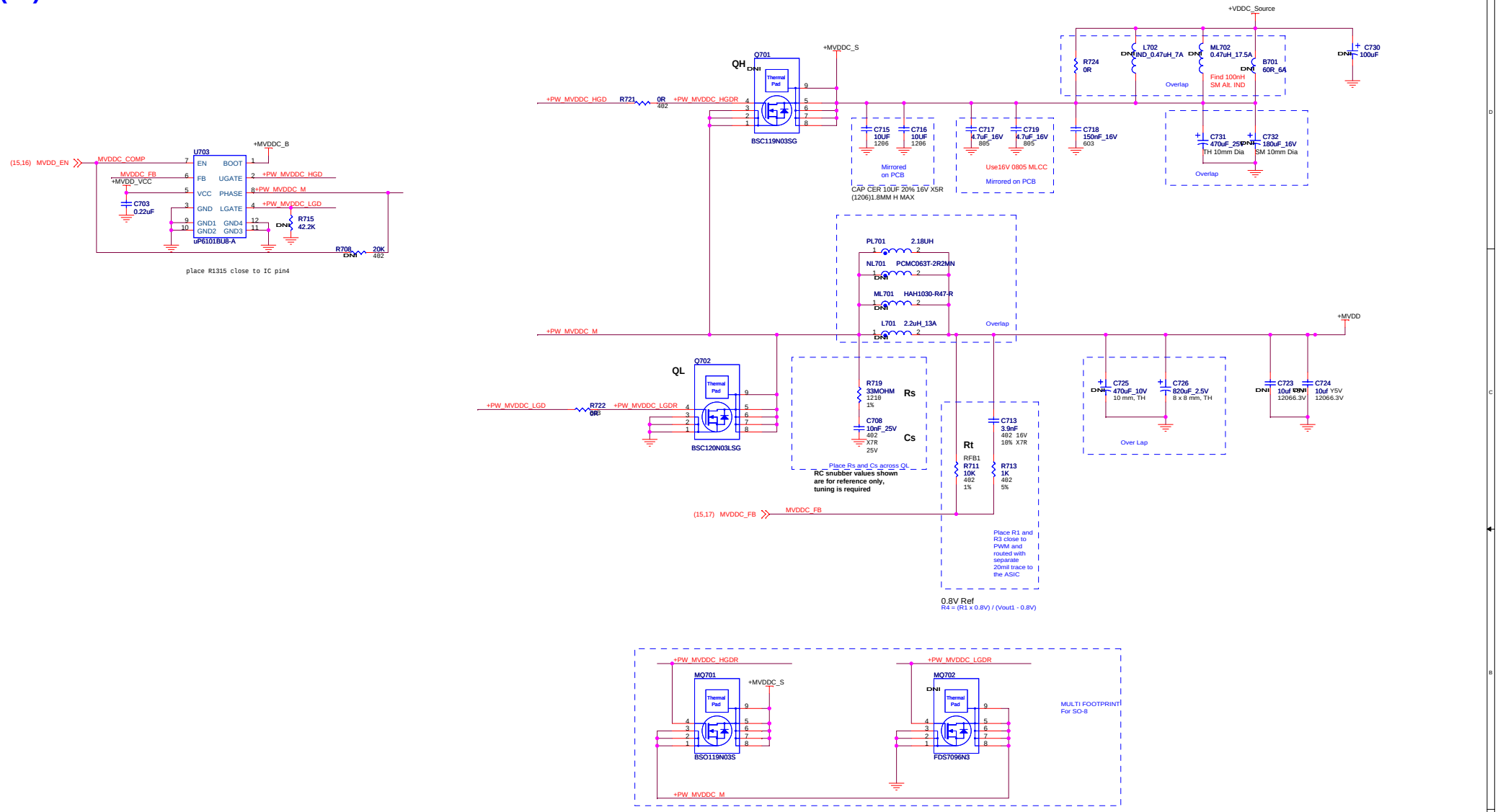
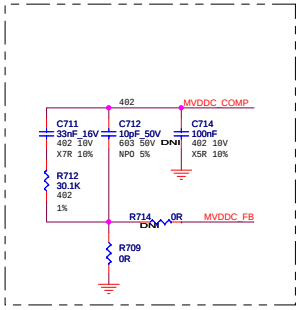
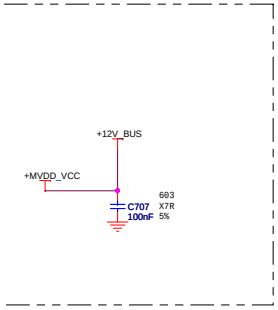
(13) MVDD



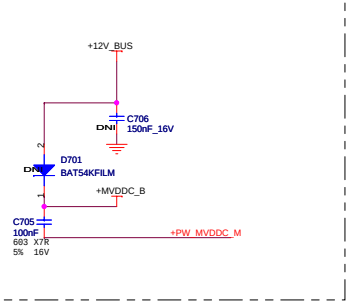
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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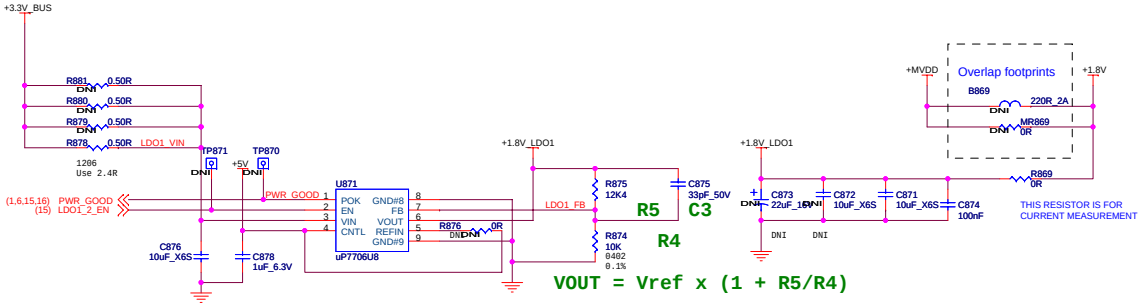
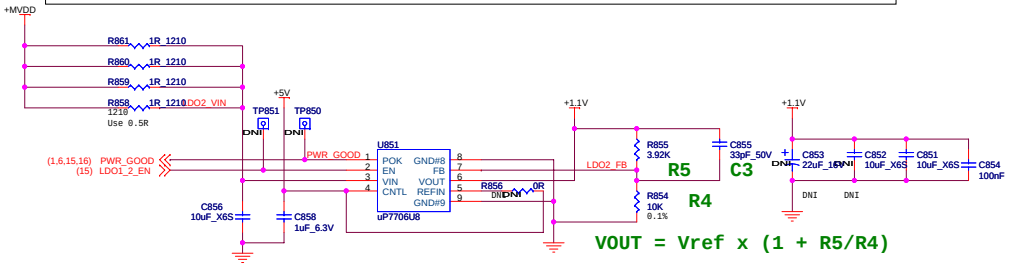
(14) Linear Regulators

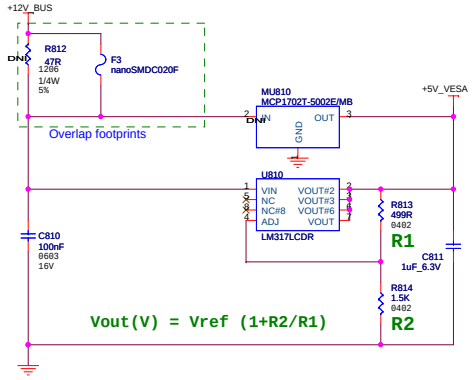
Regulators for +5V, +5V_VESA and +5V_VESA2

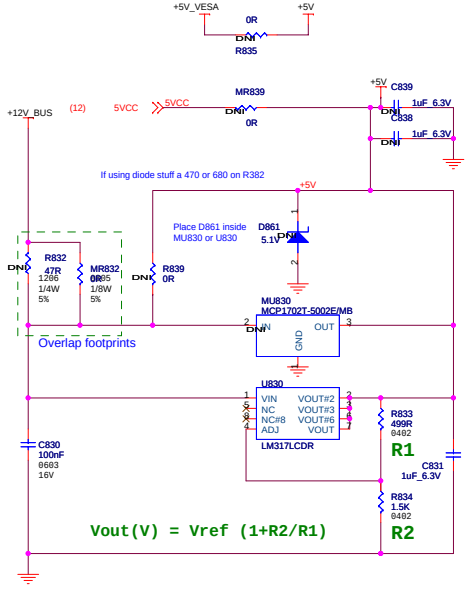
LDO #1: Vin = 3.0V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 1.0A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #2: Vin = +1.5V to 2.0VMAX Vout = +1.1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling







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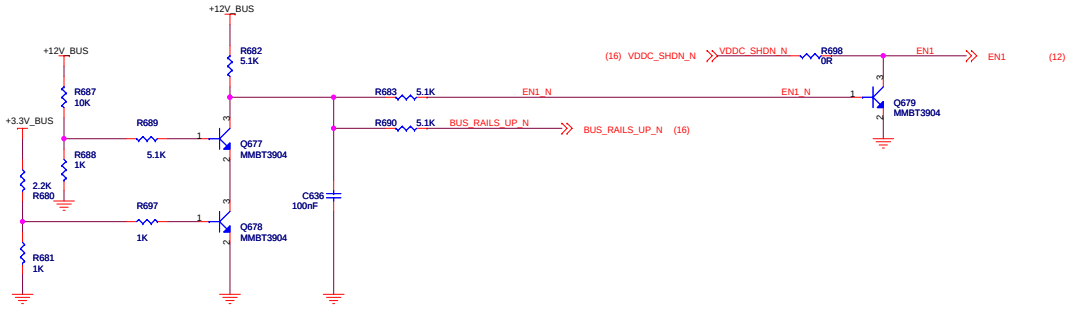
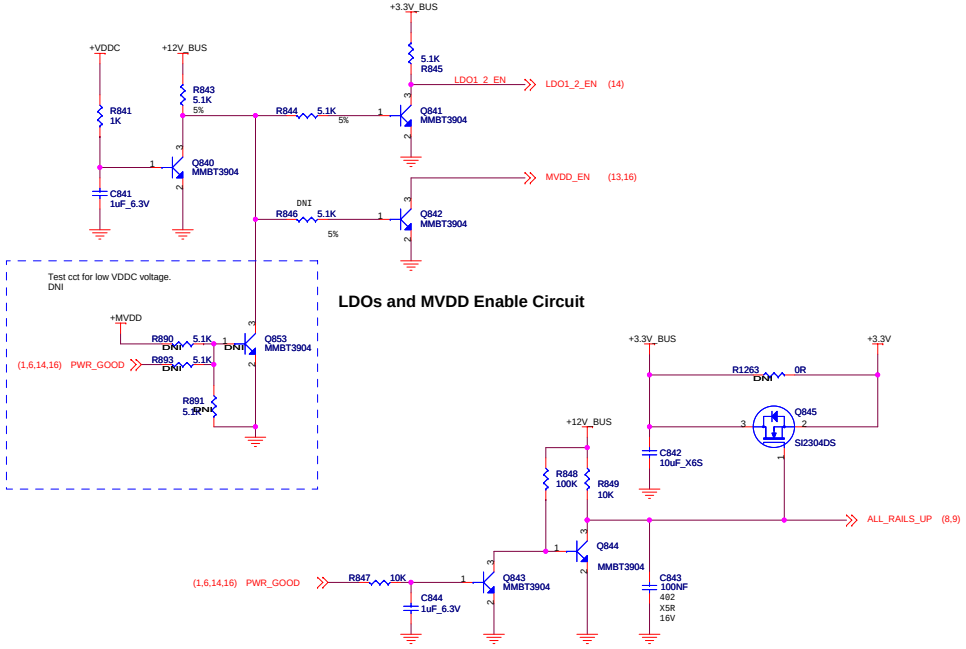
(15) Power Management

Power up Sequencing



VDDC Enable Circuit



LDOs and MVDD Enable Circuit

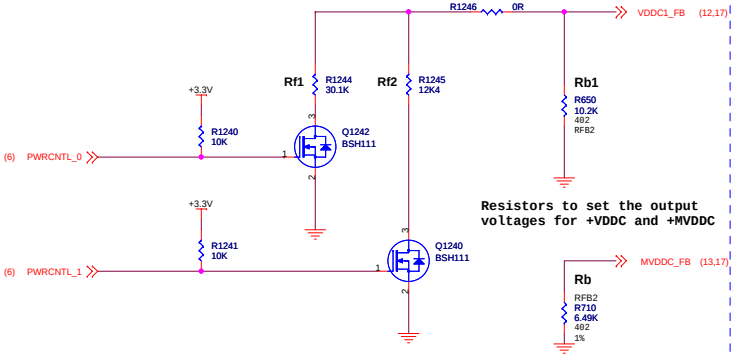
3.3V Enable Circuit

Power Play

VDDC Voltage Settings Using GPIOs (for VDDC1 Dual Phase)

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1=42.2K Rf2=20.5K	Rf1= Rf2=	Rf1= Rf2=	
0	0	0.90V			
0	1	1.00V			
1	0	1.15V			
1	1	1.25V			Power-up Default

```
Vout = Vref * (1+Rt/Rb)
VDDC1 (Dual Phase):    Vref = 0.6V, Rt = 5.11K
VDDC2 (Single Phase):  Vref = 0.8V, Rt = 10K
MVDDC (Single Phase):  Vref = 0.8V, Rt = 10K
```



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(16) Mechanical and Thermal Management

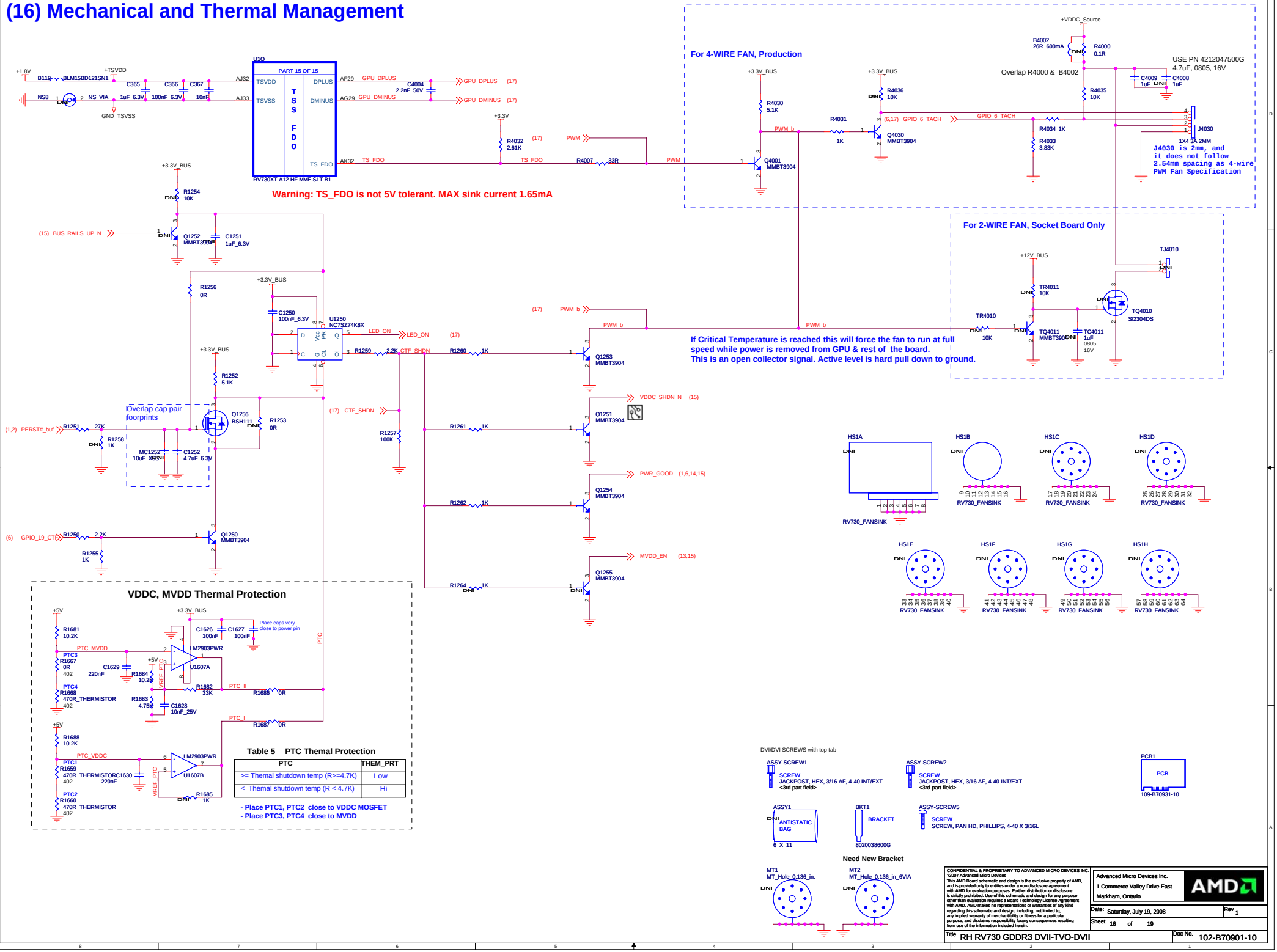

Table 5 PTC Themal Protection

PTC	THEM_PRT
>= Themal shutdown temp (R>=4.7K)	Low
< Themal shutdown temp (R < 4.7K)	Hi

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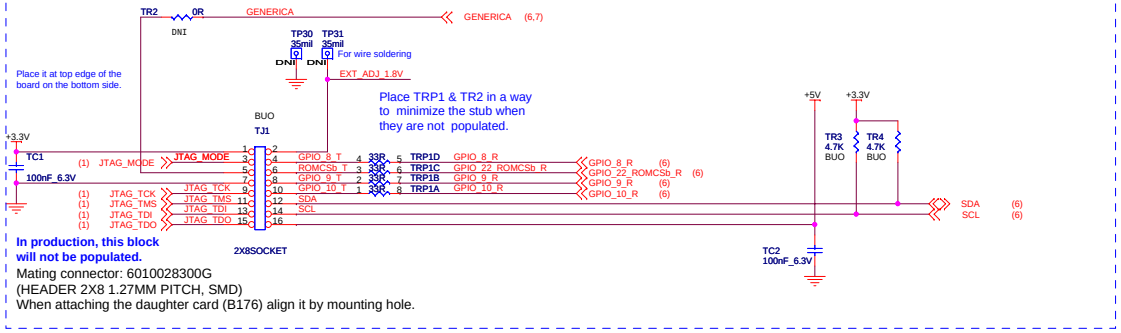
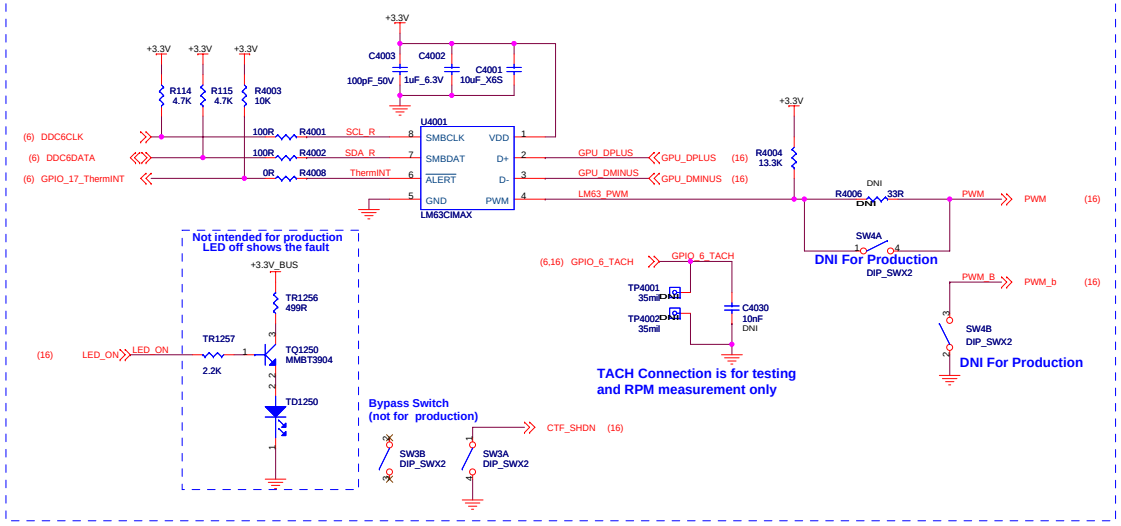
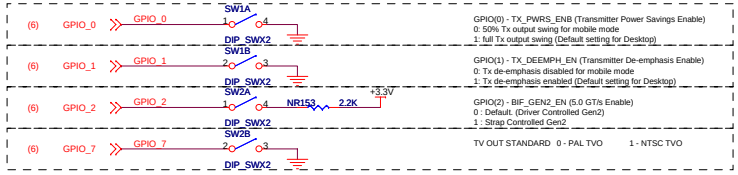
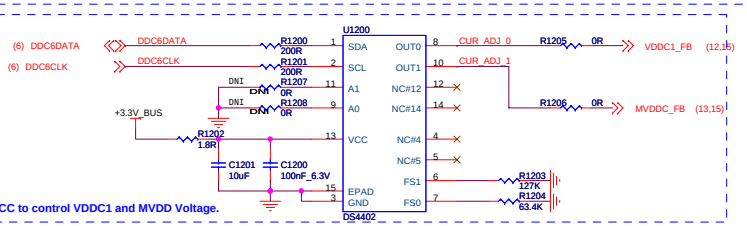
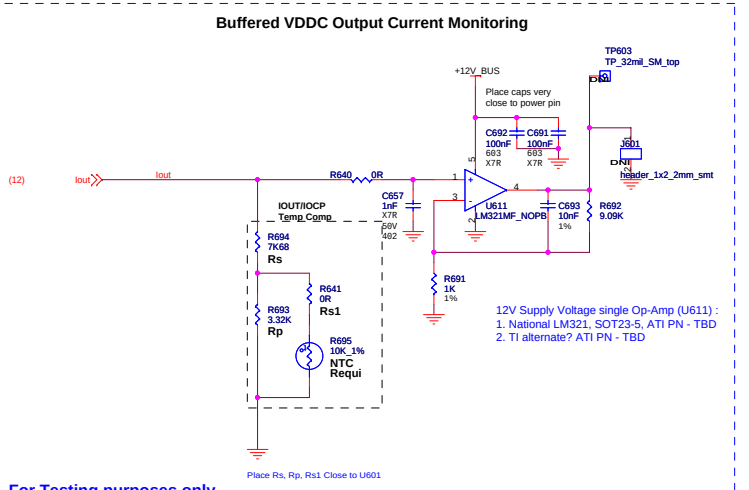
(17) Debug Circuits











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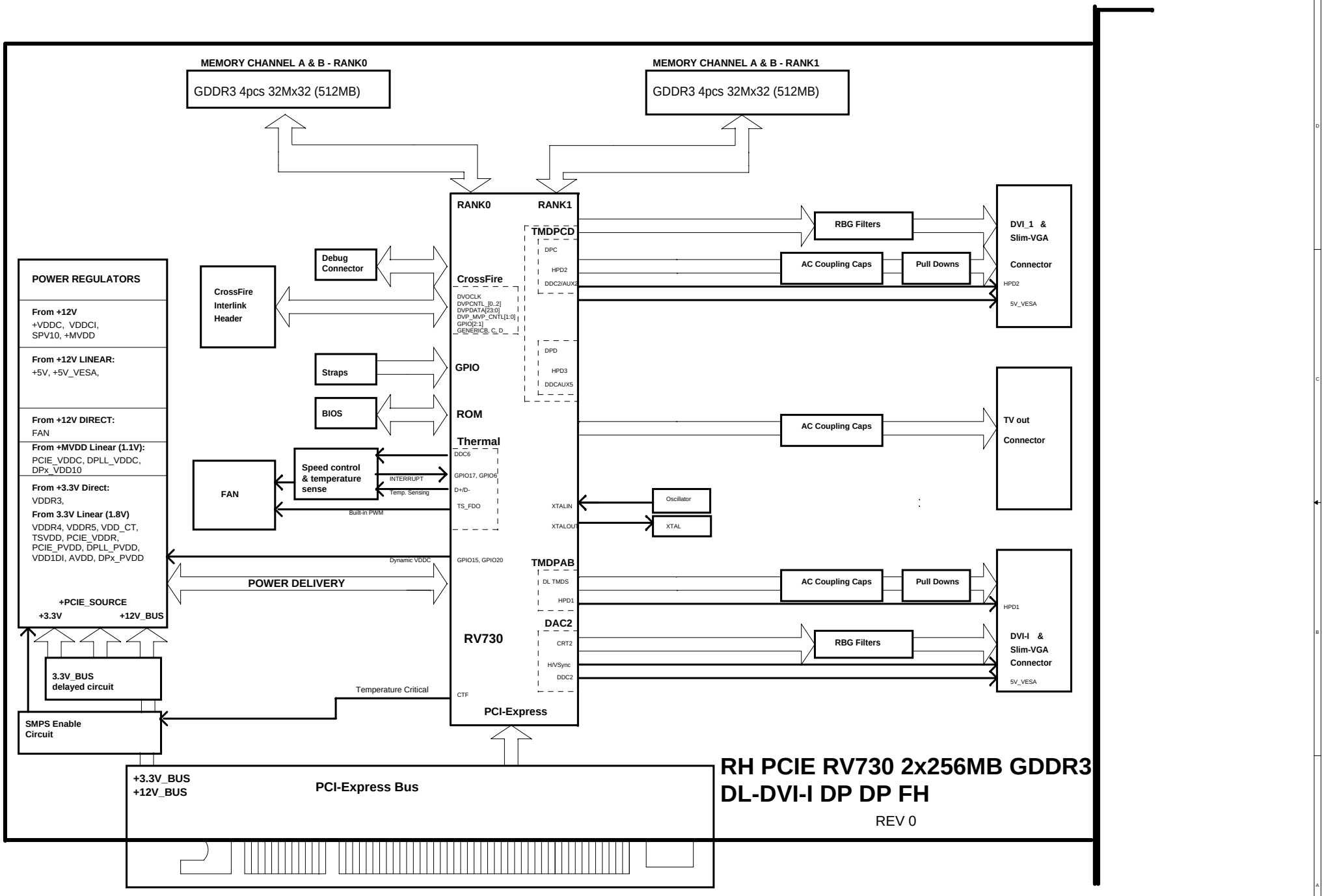

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Title	Schematic No.	Date:
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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	08/06/25	Initial design for RV730 GDDR3 DVII TVO DVII
1	00	08/06/26	Based from B667 and B666
2	10	08/07/11	Removed VID chip and some powergood circuitry. Deleted R900 from HPD3 pin