

Created SCH from P78-X16 for I/O Netlist only

P73-A00-X02
CREATED NX16 MEMORY, DECOUPLING FROM P78

P73-A00-X03
ADDED MEM & CORE FROM P70 PS FOR ISL6529
SAA7114 DECAPS ADDED AND CHANGED TO 0402

P73-A00-X04
PCB Footprint for RAM added

P73-A00-X05
C620, C621 Removed
Extra Mem Decaps removed

P73-A00-X06
PCB Footprint for Inductor, Stacked DB15, ISL6529 added
PCB Footprint for L305, L307, L308, L316-L324
changed to 0603 from 0805.
Added X-Comp R750, R751.

P73-A00-X07
TV-XTAL should be 18pf CL.
Each memory with separate clock

P73-A00-X08
U700-Parallel ROM and C700 decap Removed for space

P73-A00-X09
0603 to 0402 Package Changes for 49 components

P73-A00-X10
Design Review Updates
0603 to 0402 Package Changes for 33 components
0805 to 0603 Package Changes for 17 components
0402 to 0603 Package Changes for 10 components
Removed 25 components

P73-A00-X11
Swaps in Memory termination RN201, RN203, RN205, RN207

P73-A00-X12
C606, C615 TH replacements, Removed for want of space.

P73-A00-X13
Memory bus swaps on 1/11/02-Swap 2

P73-A00-X14
Memory bus swaps on 1/12/02-Swap 3

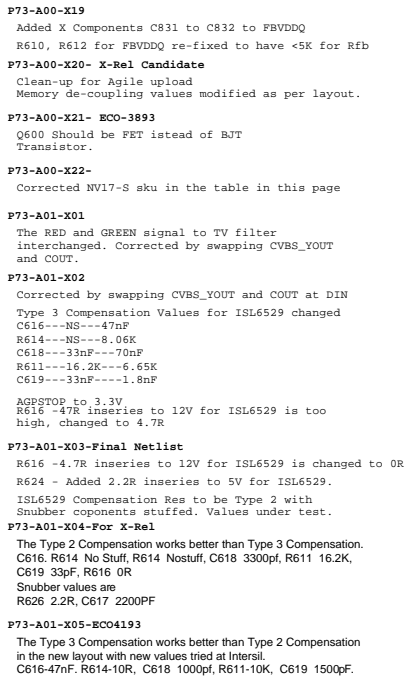
P73-A00-X15
Memory bus byte swaps as per NV17-Ball
arrangement

P73-A00-X16
Memory bus byte and bit swaps as per layout
TV Filter moved to VGA2 page with more routing notes

P73-A00-X17
The C397, C311, C318 changed to 0603 from 0402
for two trace routing near GPU break out.
P300-2 Mounting pins removed from CGND.

P73-A00-X18
Added X Components C824 to C830 to FBVDDQ

PCI DEVICE ID = 0X172 FOR GF4-MX420-XX



Stuff Option	Meaning
COMMON NO STUFF	Common to all assemblies and 1st VGA comps Not present in any assembly
VIDCAP VGA2	Video In or Video Capture 2nd VGA Components and Conenctor
DSUB	Standard single VGA Connector
TV	Second DAC channel goes to Svideo connector as TV Out
TVO	4pin DIN for TV Only
1117	Fixed 1117 linear regulator for A3.3V
1117_ADJ	Adjustable 1117 linear regulator for A3.3V
NO_1117	Connect A3.3V to 3.3V. No 1117 regulator.
CLAMP1	VGA1 Sync/I2C Clamping diodes
RGB_PROT	RGB Protection diodes on primary DAC outputs
CLAMP2	VGA2 Sync/I2C Clamping diodes
RGB2_PROT	RGB Protection diodes on secondary DAC outputs
CLAMP3	VIDCAP I2C/Video In Clamping diodes
TVCLAMP	TV Red/Green Clamping diodes
GPU	GPU ONLY
NV17-S	IDSTRAP OPTION-172H
MEMORY	Memory only
M2-8V	Memory PS output 2.8V
M2-5V	Memory PS output 2.5V

Page 1. Add CE1 and RE1 for EMI solution.
Add compability with M/B.
rename , C22 to C144,R4 to R111,R5 to R112,R6 to R113,U1 to U101
change NET name, U100.AH17 to BUF_PCIRST_ also at the R112 and C144.

Page 4. U300.9,U300.10,U300.1,U300.2 and U300.7 pin connect to GND.

Page 5. remove VGA2 function.

Page 9. Remove SAA7114H function and ADD AV-OUT & S_OUT conector.
remove L500,C500,C505,C506,C538,C539,C507,C508

Page 10. C613,C604,C605,C614,L600 and L601 change to DIP type,ADD C620 , Q1 change to AOS4800

Page 11. R704~R719,R726~R733,R745,R746 PAD size change to 0603 type and Add R747 10k ohm.
Add parallel bios function.
R746,R747 stuff (00)

Page 6 . Add Fan power function.

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Page 2. Add 74XCT74 buffer for PCI_RST function.


Page 5. Add 75ohm and bypass Cap. for TV-OUT function.

Page 9. Swap S-OUT.3 and S-OUT.4 net name.

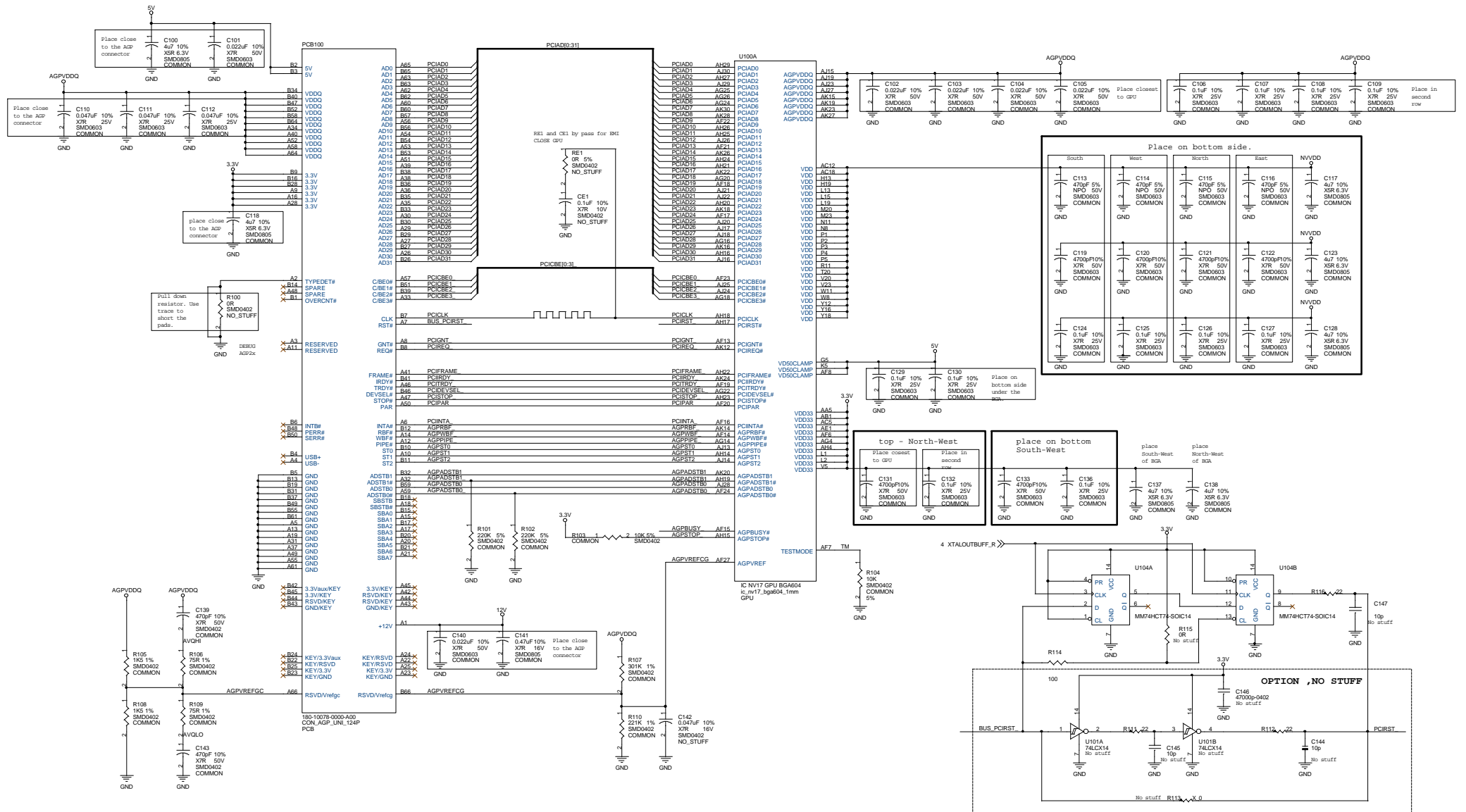
Page 10. Change DIP type CAP. footprint.

Page 11. Change U1000.22 net name.

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Item\tQuantity\tReference\tValue\tAssembly\tMAIN\NVPN\Source Package\AVL1\AVL2\AVL3\AVL4\AVL5
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	Micro-Star International Co., LTD.		
	MS-8878 base on P73 Modify		
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- 1 top (this) page
- 2 1. AGP interface, core decoupling
- 3 2.a NV17 Frame Buffer
- 4 3.a Dual DAC, 1st VGA
- 5 3.b Dual DAC, 2nd VGA
- 6 3.c TMD5 NV17
- 7 4.a Frame Buffer 0..31
- 8 4.b Frame Buffer 32..63
- 9 5. TV-out, video capture, stereo
- 10 6. Power supply
- 11 7. BIOS, Strapping

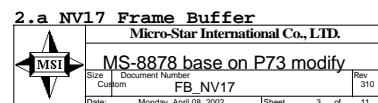


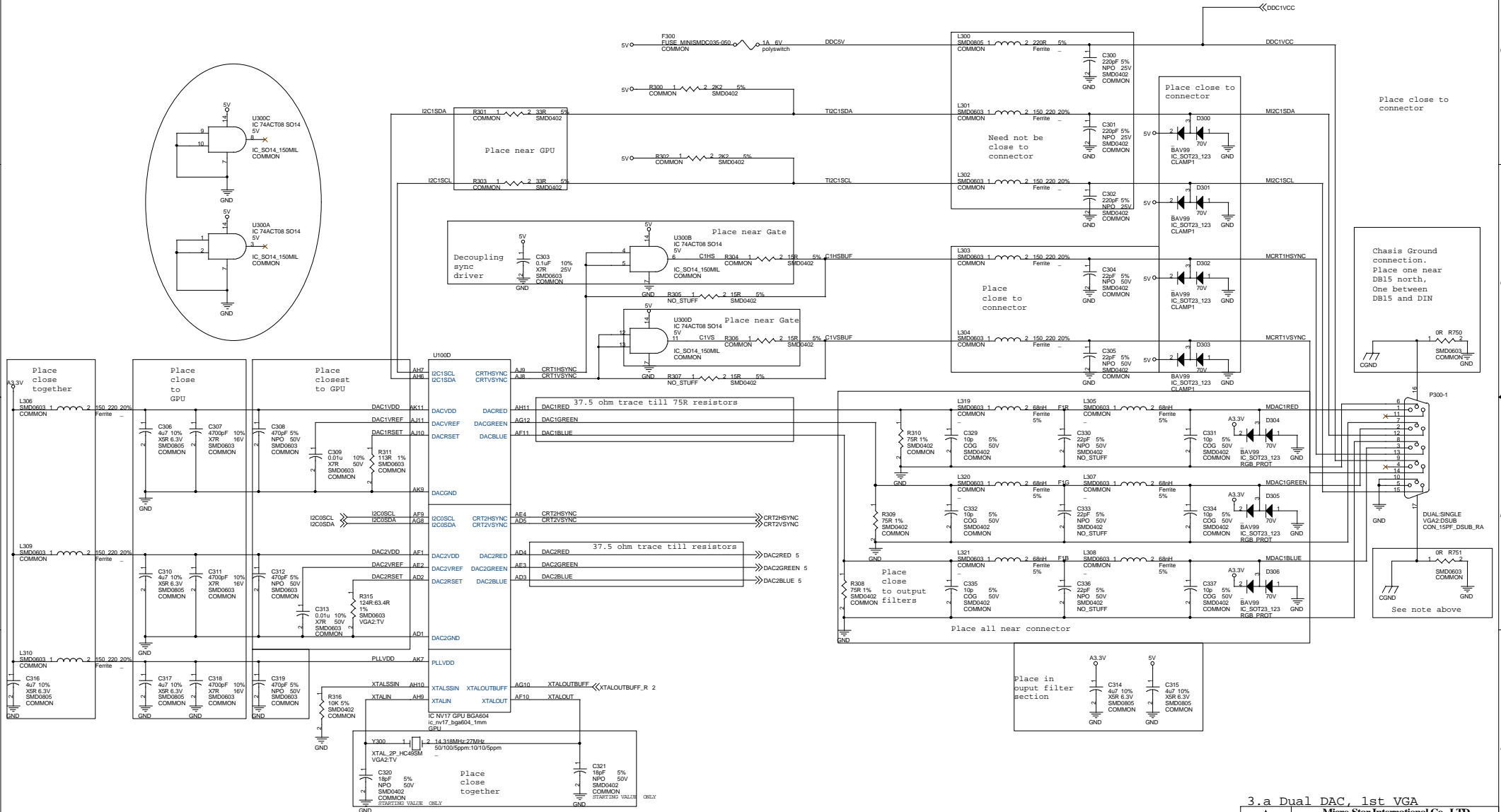
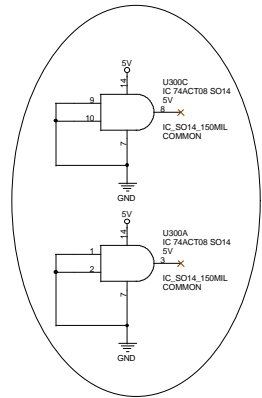
1. AGP interface, core decoupling

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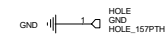
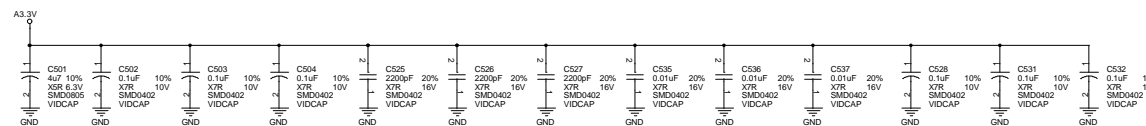
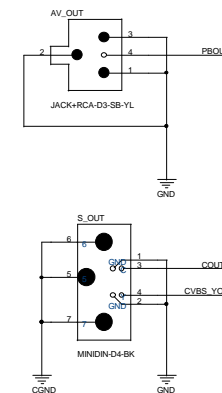
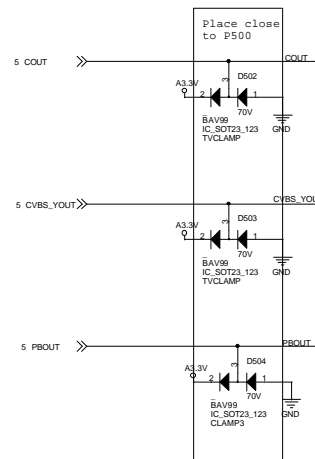


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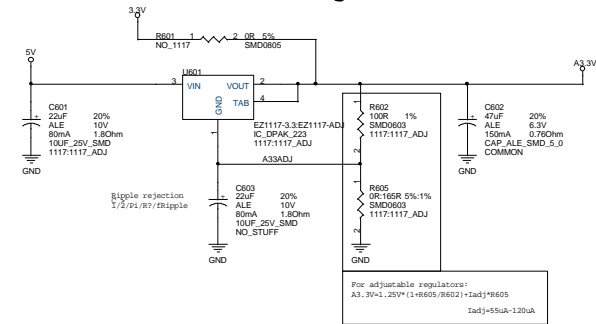


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Analog 3.3V



FOR DESKTOP-NV17
 NVVDD DESIGN TARGET 1.584min/1.616max
 NVVDD QUAL TARGET 1.550min/1.700max

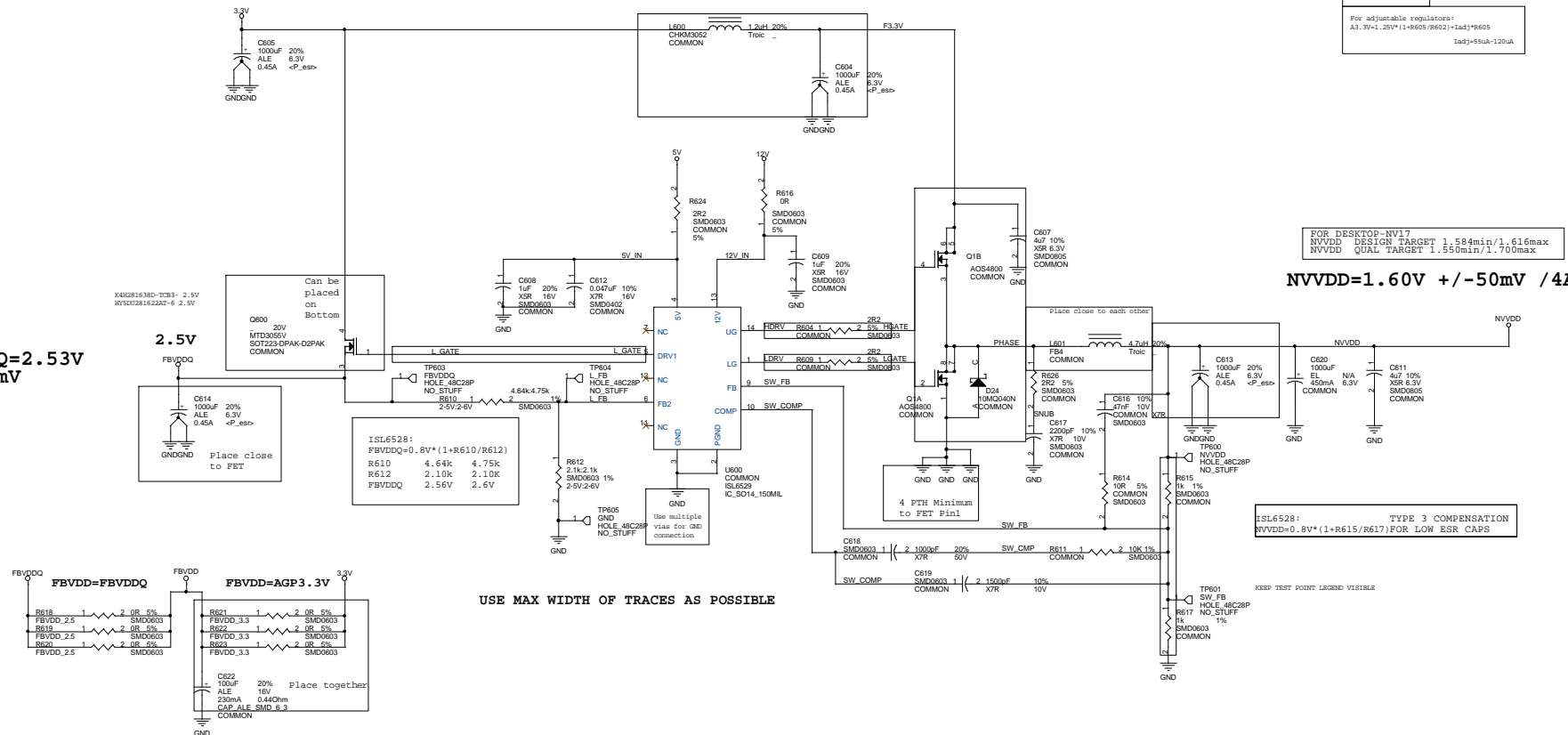
NVVDD=1.60V +/-50mV /4A

ISL6528: TYPE 3 COMPENSATION
 $NVVDD = 0.8V * (1 + R615/R617)$ FOR LOW ESR CAPS

KEEP TEST POINT LABELED VISIBLE

USE MAX WIDTH OF TRACES AS POSSIBLE

**FBVDDQ=2.53V
 +/-30mV**



6. Power supply

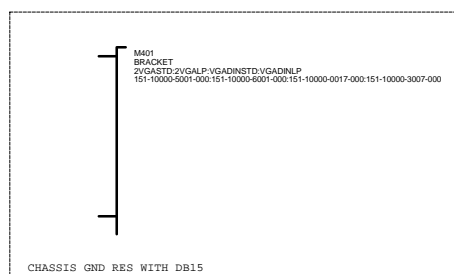
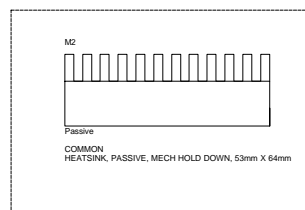
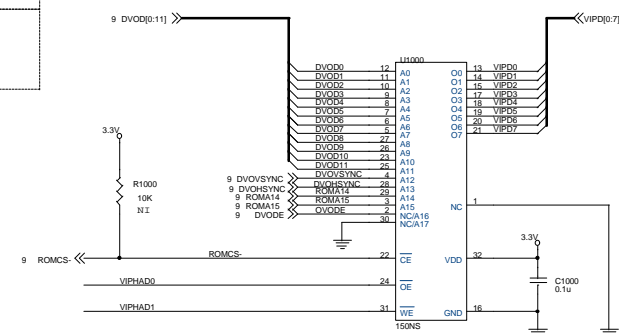
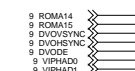
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Power supply

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7. BIOS, Strapping, Mech

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