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P11	删除Partittion A Decoupling
P18	删除SLI
P19	删除INFOROM / JTAG
P24	Add EXT_12V_ocnconnector
P25	Change PEXVDD from SWITCH VR to LINEAR VR Add FBVDD_power_source
P26	NVVDD change to two-pahse 上二下二
P27	Change 2-PIN FAN CONTROL- IC option

REV	VARIANT	NVPN	ASSEMBLY
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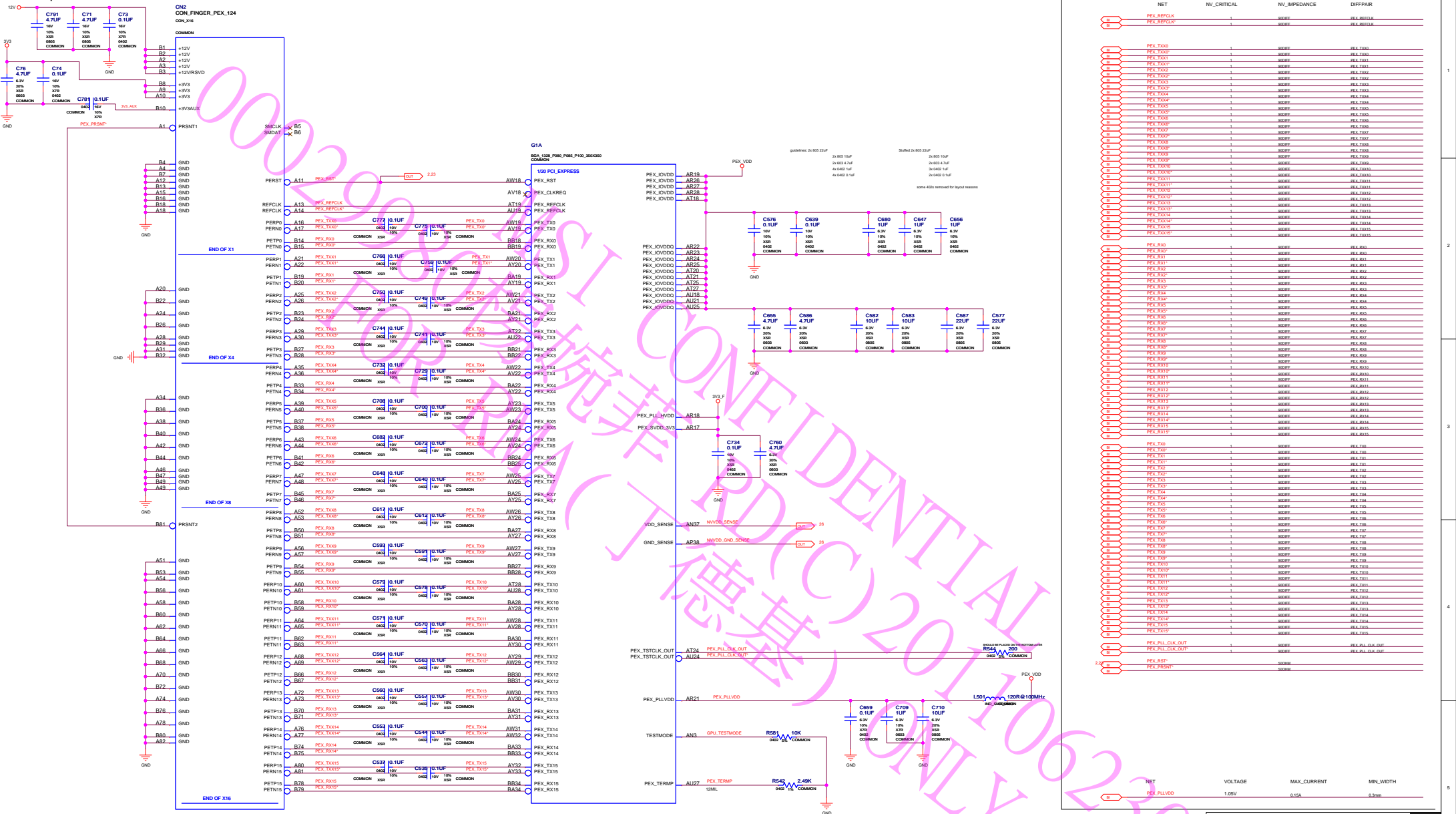
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PCI Express

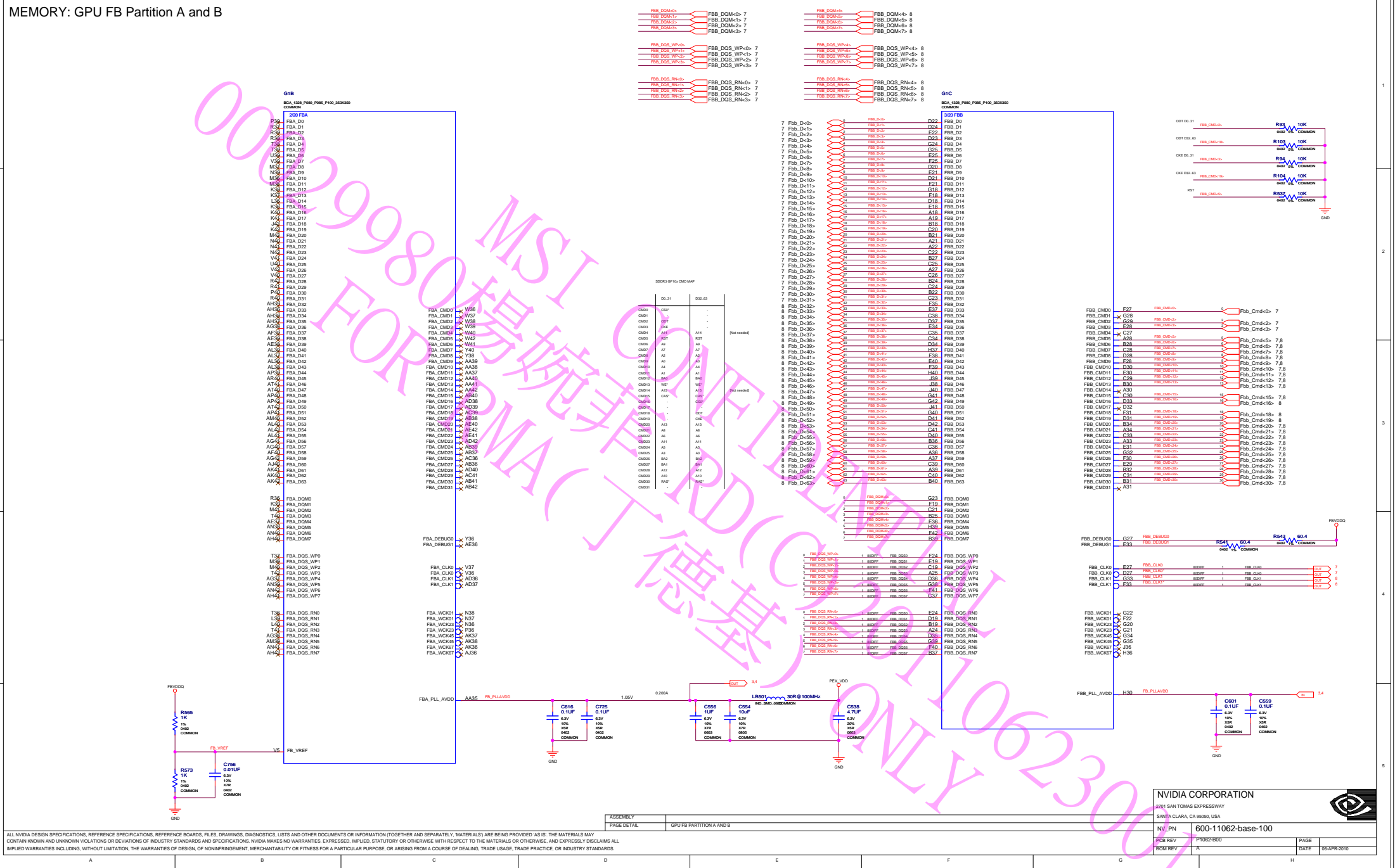


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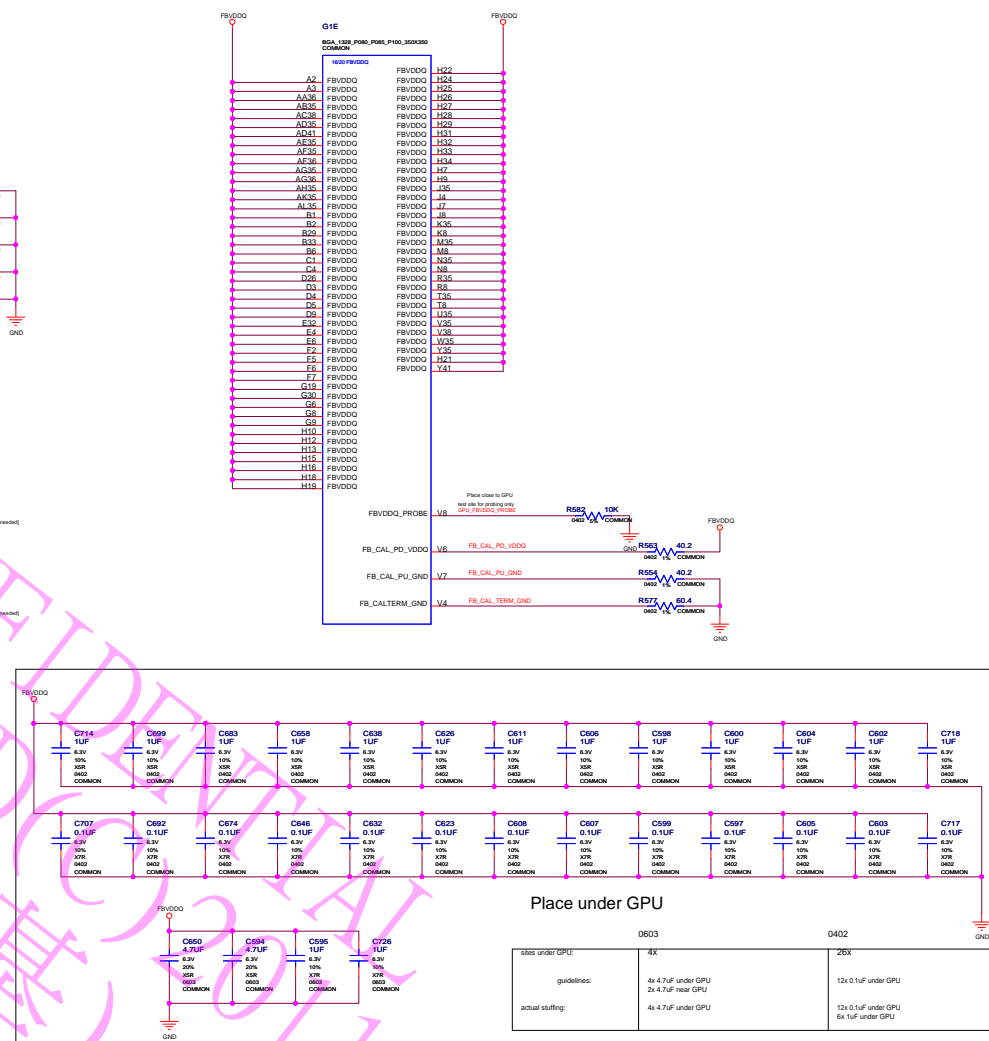
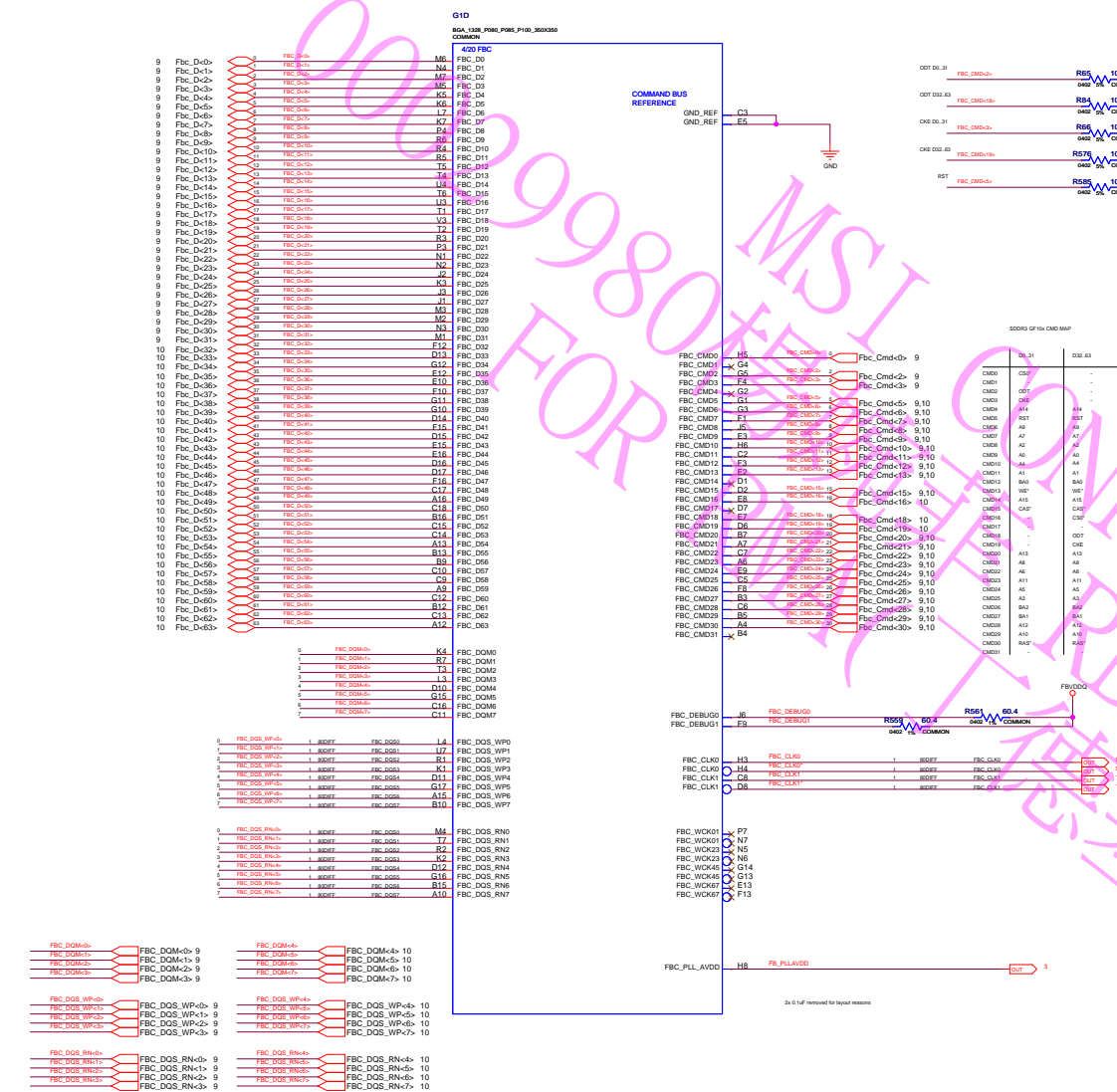
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MEMORY: GPU FB Partition A and B



MEMORY: GPU FB Partition C AND GPU FB Decap



Memory Lower Partition A

DISABLE PARTITON A

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CAS01	0000	0000
CAS02	0000	0000
CAS03	0000	0000
CAS04	0000	0000
CAS05	0000	0000
CAS06	0000	0000
CAS07	0000	0000
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CAS61	0000	0000
CAS62	0000	0000
CAS63	0000	0000

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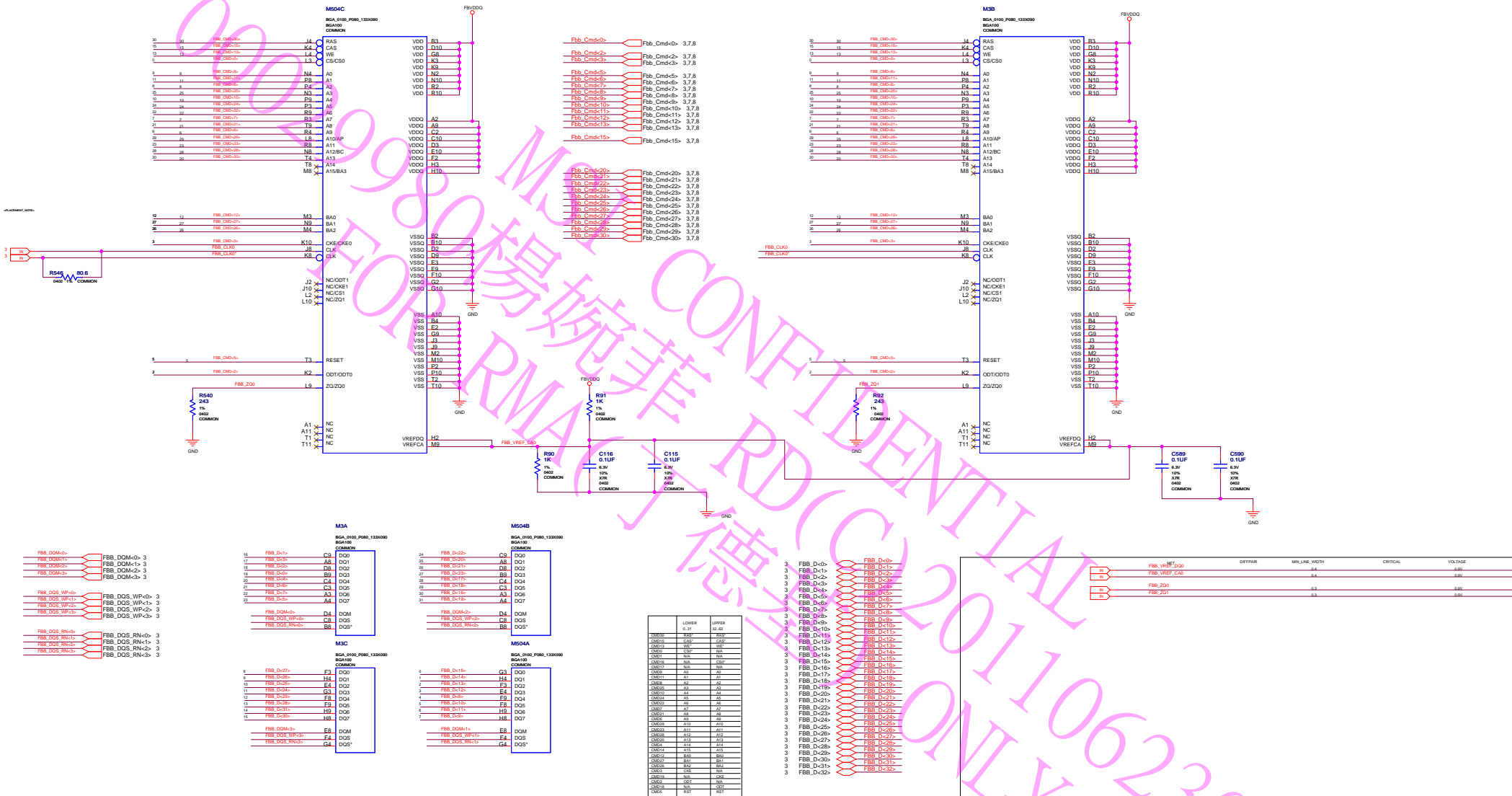
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Memory Lower Partition B



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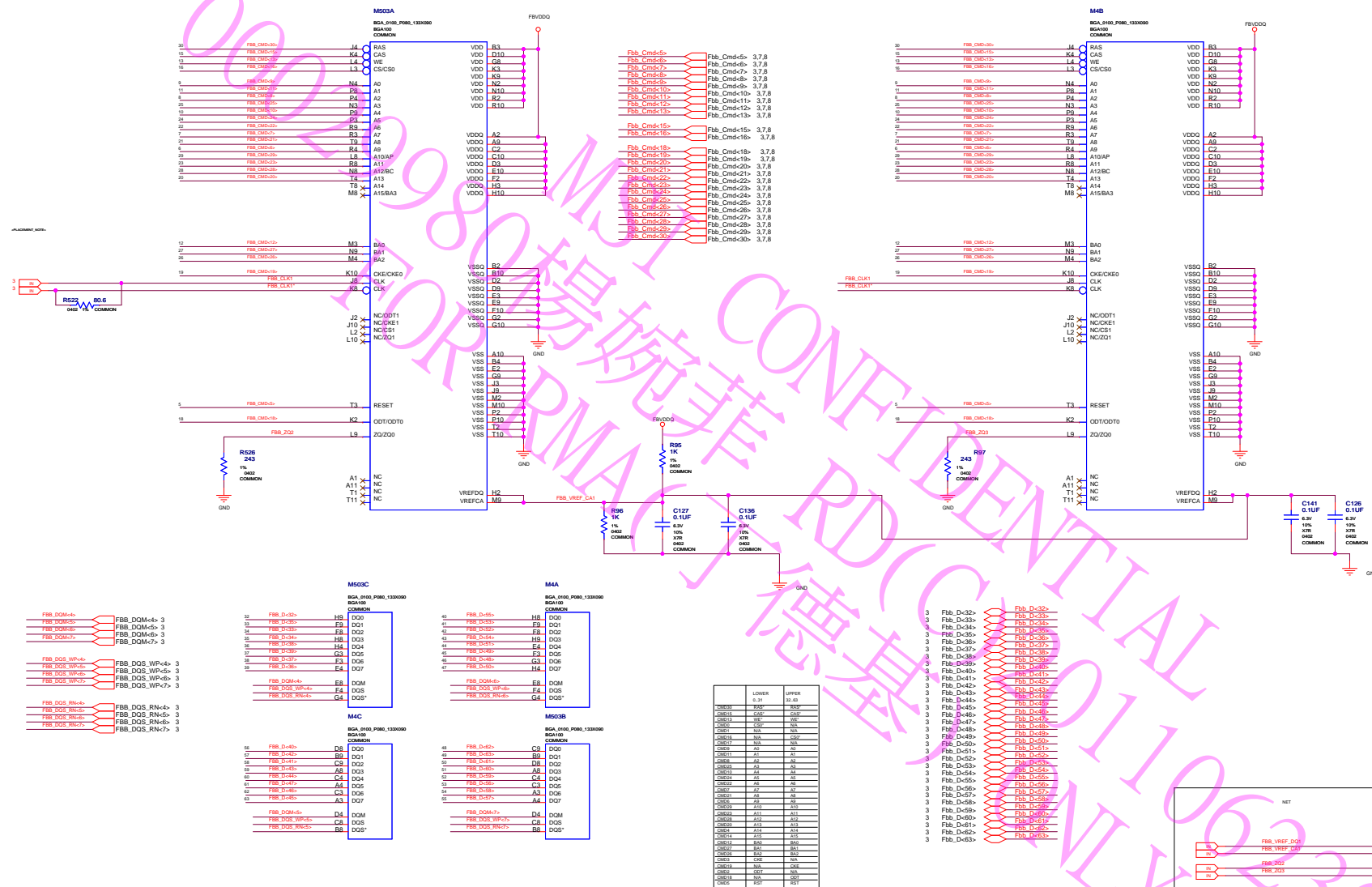
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## Memory Upper Partition B



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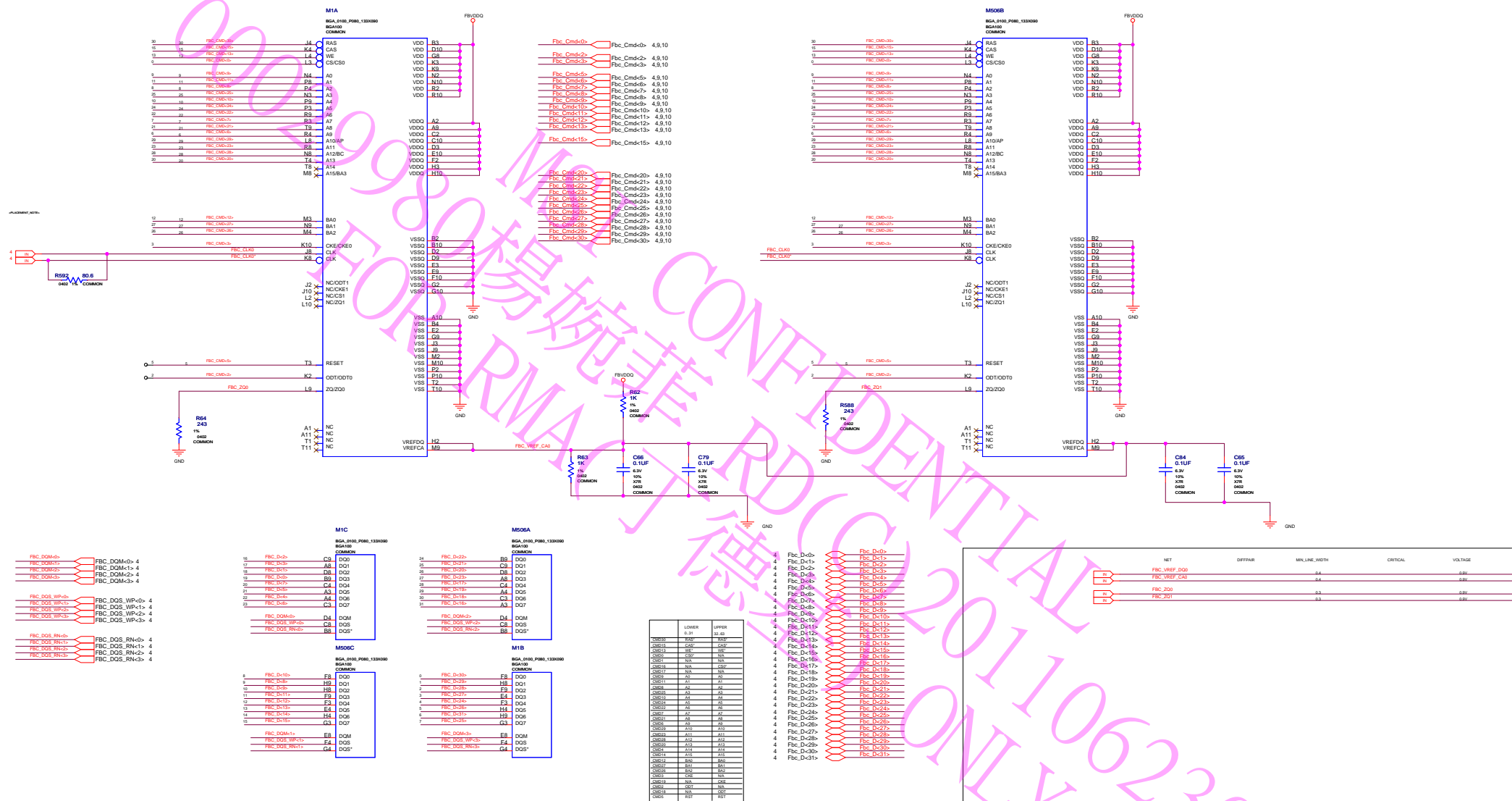
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CM503	AS	

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## Memory Lower Partition C

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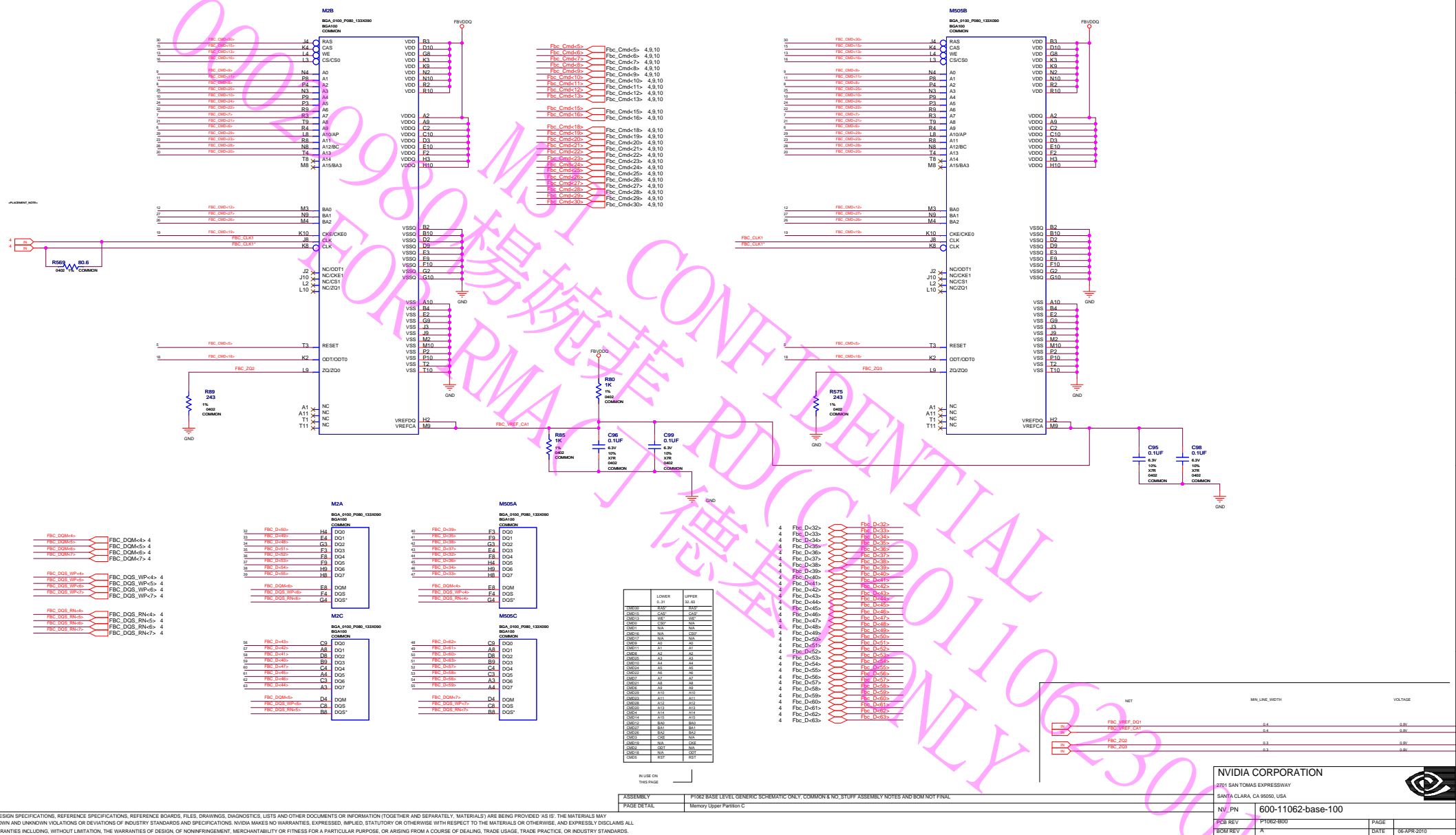
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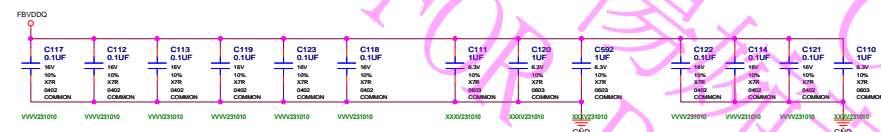
Figure 1. The effect of the number of trials on the number of correct responses.

## Memory Upper Partition C



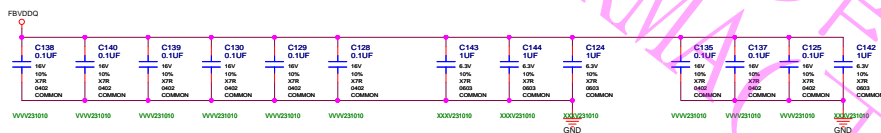
## Memory FBVDD/Q Decoupling

## DECOUPLING FOR M6

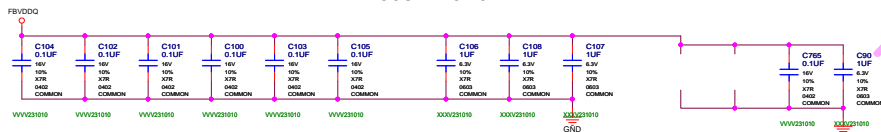


### DECOUPLING FOR M3

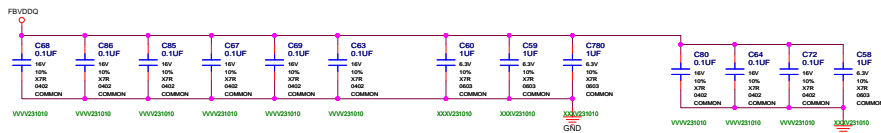
## DECOUPLING FOR M4



## DECOUPLING FOR M2



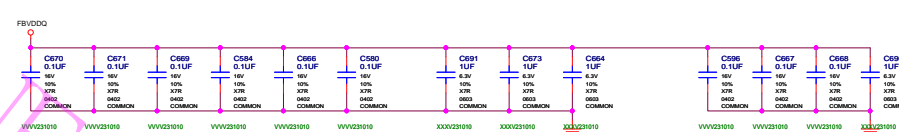
## DECOUPLING FOR M1



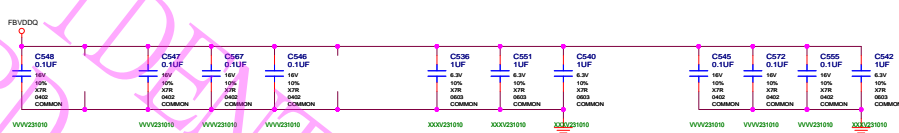
DECOUPLING FOR M502

DECOUPLING FOR M501

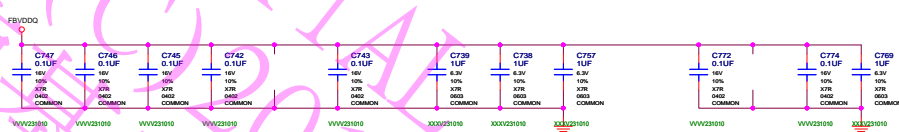
DECOUPLING FOR M504



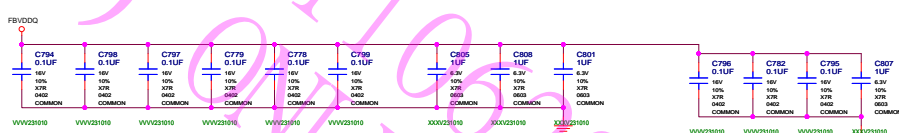
DECOUPLING FOR M503



## DECOUPLING FOR M505



## DECOUPLING FOR M506



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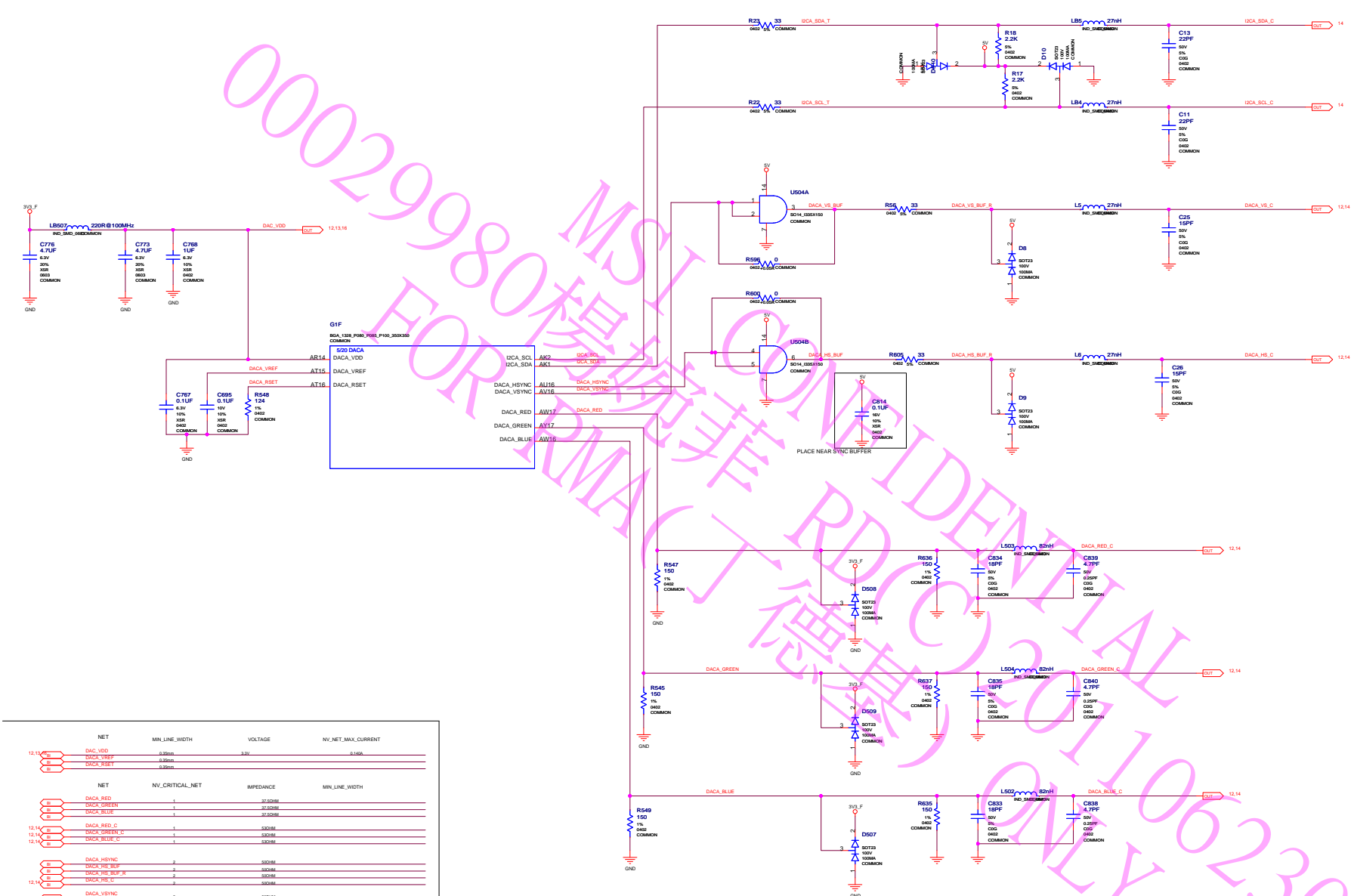
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ASSEMBLY	
PAGE DETAIL	Memory FBVDD/Q Decoupling

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### DACA for South DVI Interface


## DACA RGB-FILTER



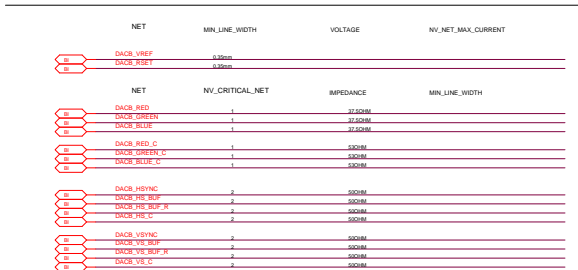
NET		MIN_LENGTH	VOLTAGE	SV_NET_MAX_CURRENT
12, 14	DAC_VDD	0.5mm	3.3V	0.150A
12, 14	DAC_VREF	0.5mm		
12	DAC_RESET	0.5mm		
<hr/>				
NET		SV_CRITICAL_NET	IMPEDANCE	MIN_LENGTH
12	DACA_RED	1	37.500M	
12	DACA_GREEN	1	37.500M	
12	DACA_BLUE	1	37.500M	
12, 14	DACA_RED_C	1	5000M	
12, 14	DACA_GREEN_C	1	5000M	
12, 14	DACA_BLUE_C	1	5000M	
<hr/>				
12	DACA_HYMC	2	5000M	
12	DACA_VIE_BUF	2	5000M	
12	DACA_VIE_BUF_W	2	5000M	
12, 14	DACA_VIE_C	2	5000M	
<hr/>				
12	DACA_VHMC	2	5000M	
12	DACA_VIE_BUF	2	5000M	
12	DACA_VIE_BUF_W	2	5000M	
12, 14	DACA_VIE_C	2	5000M	

ASSEMBLY	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA Interface for DVI

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## DACB RGB-FILTER



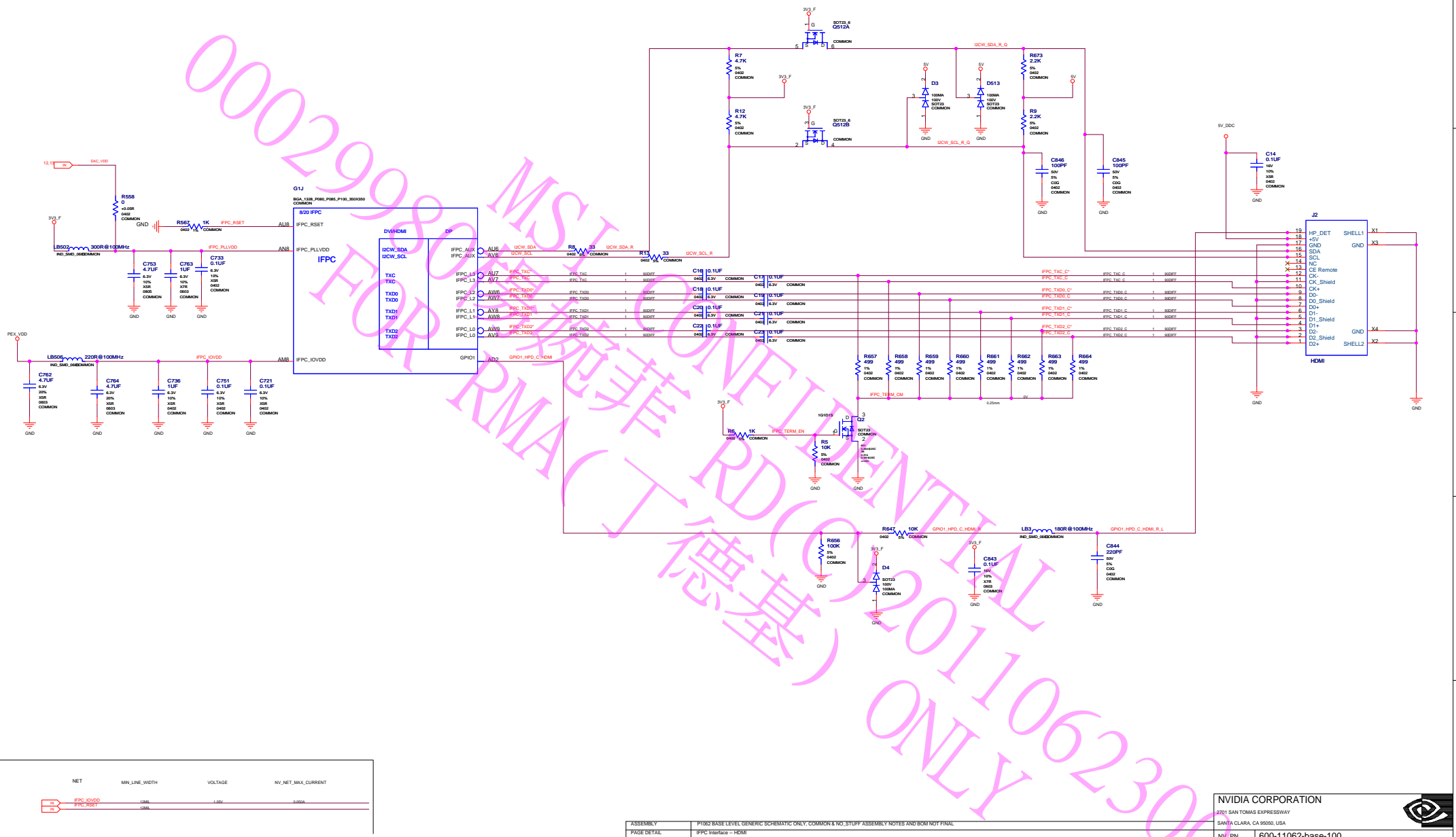
ASSEMBLY	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB Interface for VGA








## IFP C Interface -- HDMI, North



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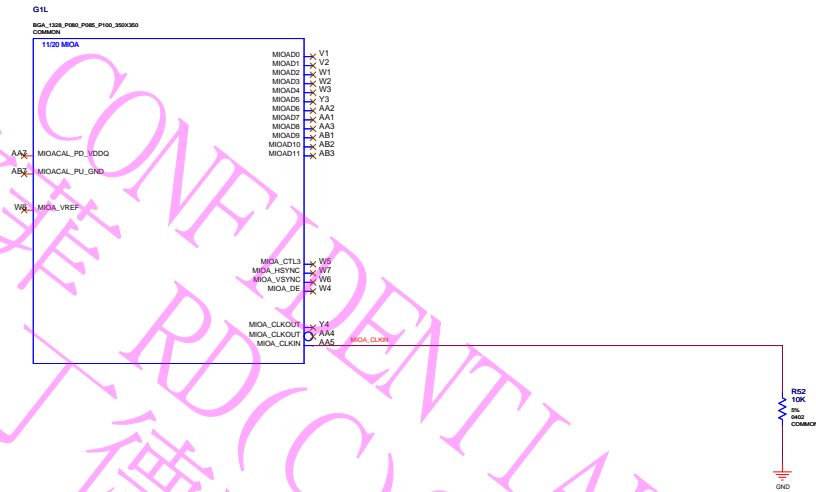
ASSEMBLY	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPC Interface -- HDMI

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BOM REV	A	DATE	06-APR-2010






## MIO A Interface, SLI



NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT

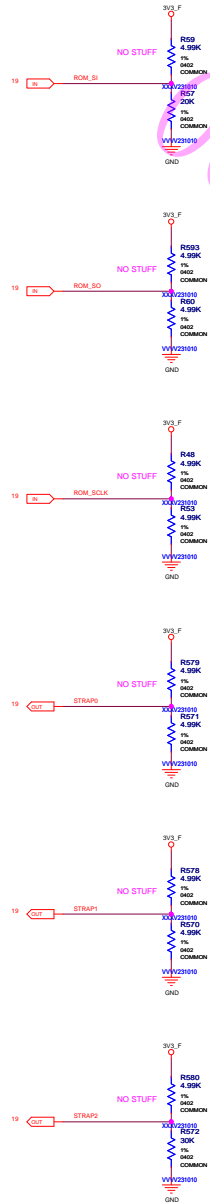
ASSEMBLY	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIO A Interface, SLI

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### Strap Configuration

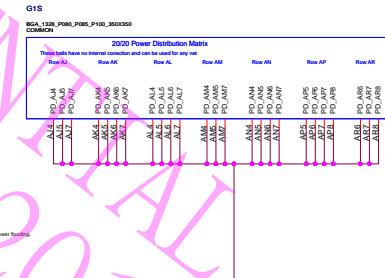
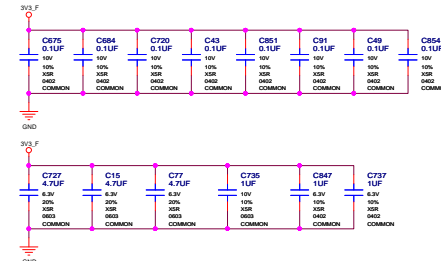
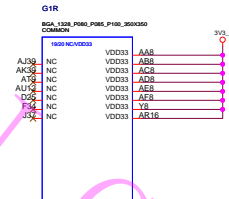
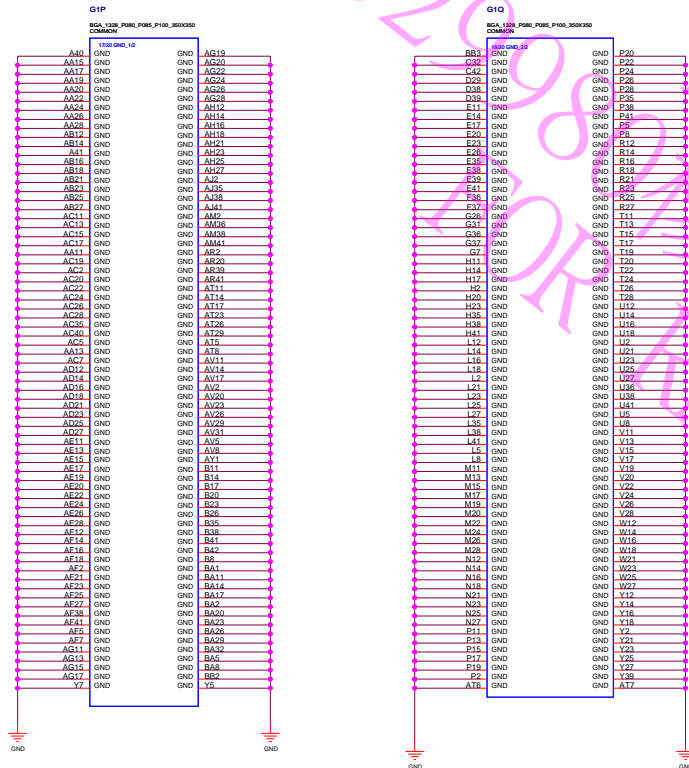


GF106-300: 0x0DC0

[illegible]

Multi-level Strap Restraint Values	
Strap PU/PD Rise (30Ch)	
0	PD 5
1	PD 10
2	PD 15
3	PD 20
4	PD 25
5	PD 30
6	PD 35
7	PD 40
8	PU 5
9	PU 10
10	PU 15
11	PU 20
12	PU 25
13	PU 30
14	PU 35
15	PU 40

## PWR and GND Signals



# NVDD Decoupling

G1T		BGA_1028_P080_P086_P105_300X350	COMMON
AA12	VDD	AA12	VDD
AA14	VDD	AA14	VDD
AA16	VDD	AA16	VDD
AA18	VDD	AA18	VDD
AA21	VDD	AA21	VDD
AA23	VDD	AA23	VDD
AA25	VDD	AA25	VDD
AA27	VDD	AA27	VDD
AB11	VDD	AB11	VDD
AB13	VDD	AB13	VDD
AB15	VDD	AB15	VDD
AB17	VDD	AB17	VDD
AB19	VDD	AB19	VDD
AB21	VDD	AB21	VDD
AB22	VDD	AB22	VDD
AB24	VDD	AB24	VDD
AB26	VDD	AB26	VDD
AB28	VDD	AB28	VDD
AC12	VDD	AC12	VDD
AC14	VDD	AC14	VDD
AC16	VDD	AC16	VDD
AC18	VDD	AC18	VDD
AC21	VDD	AC21	VDD
AC23	VDD	AC23	VDD
AC25	VDD	AC25	VDD
AC27	VDD	AC27	VDD
AD11	VDD	AD11	VDD
AD13	VDD	AD13	VDD
AD15	VDD	AD15	VDD
AD17	VDD	AD17	VDD
AD19	VDD	AD19	VDD
AD21	VDD	AD21	VDD
AD22	VDD	AD22	VDD
AD24	VDD	AD24	VDD
AD26	VDD	AD26	VDD
AD28	VDD	AD28	VDD
AE12	VDD	AE12	VDD
AE14	VDD	AE14	VDD
AE16	VDD	AE16	VDD
AE18	VDD	AE18	VDD
AE21	VDD	AE21	VDD
AE23	VDD	AE23	VDD
AE25	VDD	AE25	VDD
AE27	VDD	AE27	VDD
AF11	VDD	AF11	VDD
AF13	VDD	AF13	VDD
AF15	VDD	AF15	VDD
AF17	VDD	AF17	VDD
AF19	VDD	AF19	VDD
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AF24	VDD	AF24	VDD
AF26	VDD	AF26	VDD
AG12	VDD	AG12	VDD
AG14	VDD	AG14	VDD
AG16	VDD	AG16	VDD
AG18	VDD	AG18	VDD
AG21	VDD	AG21	VDD
AG23	VDD	AG23	VDD
AG25	VDD	AG25	VDD
AG27	VDD	AG27	VDD
AH11	VDD	AH11	VDD
AH13	VDD	AH13	VDD
AH15	VDD	AH15	VDD
AH17	VDD	AH17	VDD
AH19	VDD	AH19	VDD
AH21	VDD	AH21	VDD
AH23	VDD	AH23	VDD
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AH26	VDD	AH26	VDD
AH28	VDD	AH28	VDD
AM12	VDD	AM12	VDD
AM14	VDD	AM14	VDD
AM16	VDD	AM16	VDD
AM18	VDD	AM18	VDD
AM21	VDD	AM21	VDD
AM23	VDD	AM23	VDD
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AM27	VDD	AM27	VDD
AN12	VDD	AN12	VDD
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AW14	VDD	AW14	VDD
AW16	VDD	AW16	VDD
AW18	VDD	AW18	VDD
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0805 0603 0402

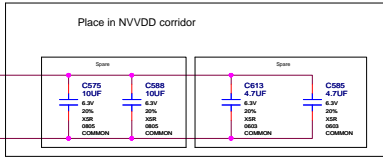
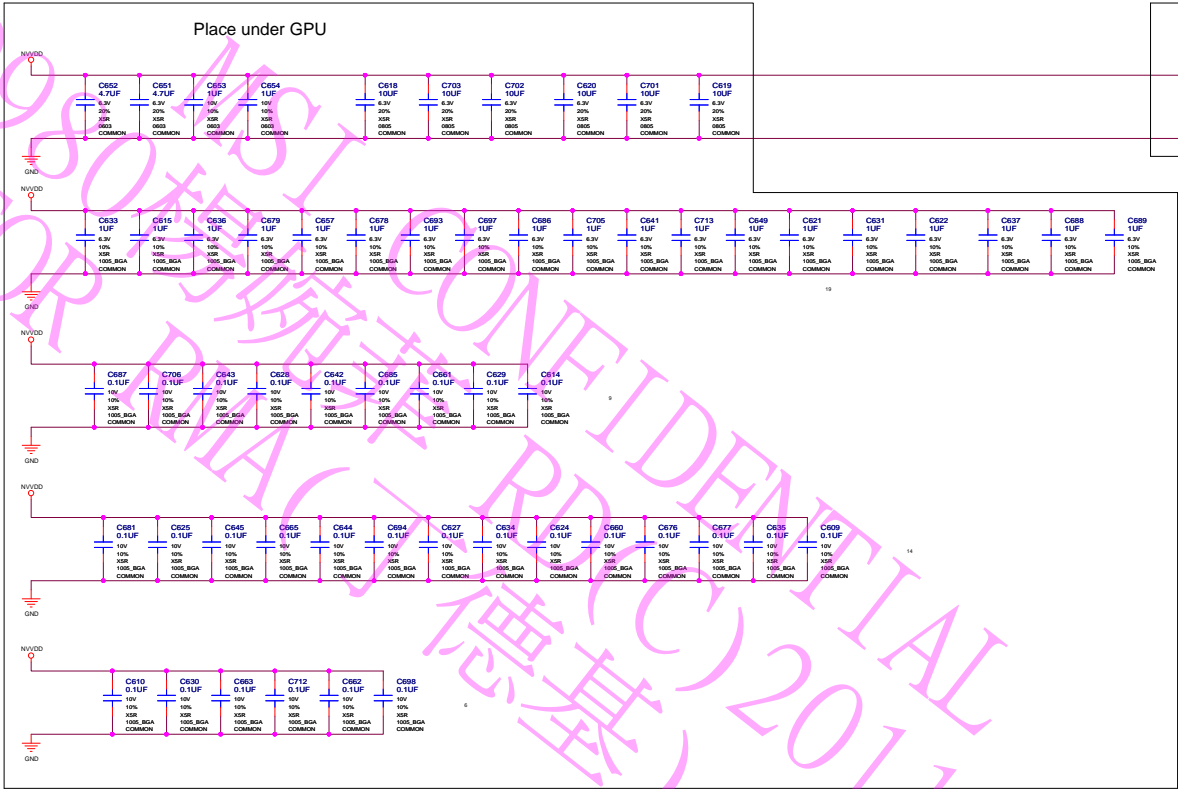
Sites placed under GPU:

Stuf under GPU:

5x 10uF  
1x 22uF

2x 4.7uF  
(2x unused)

10x 10uF  
17x 10uF



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PAGE/DETAIL	NVDD Decoupling

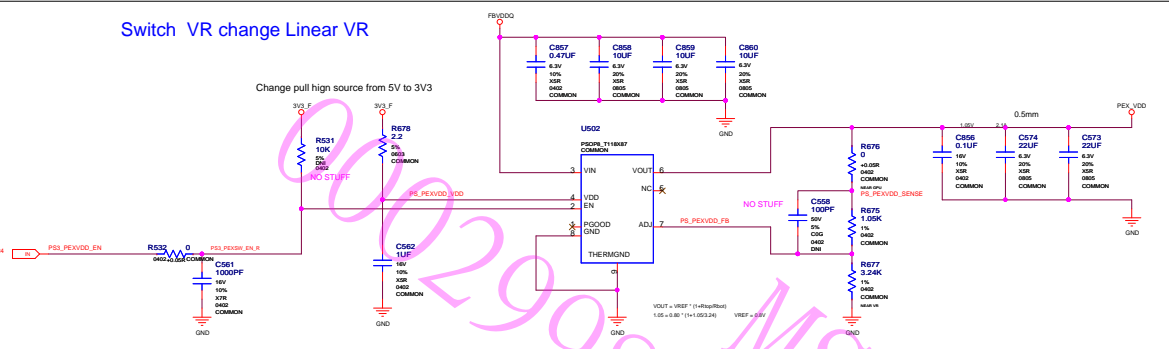
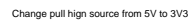
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ICSR REV	P1062-2800	PAGE	
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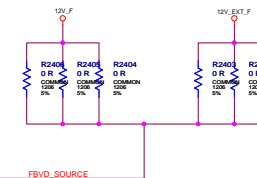




Switch VR change Linear VR



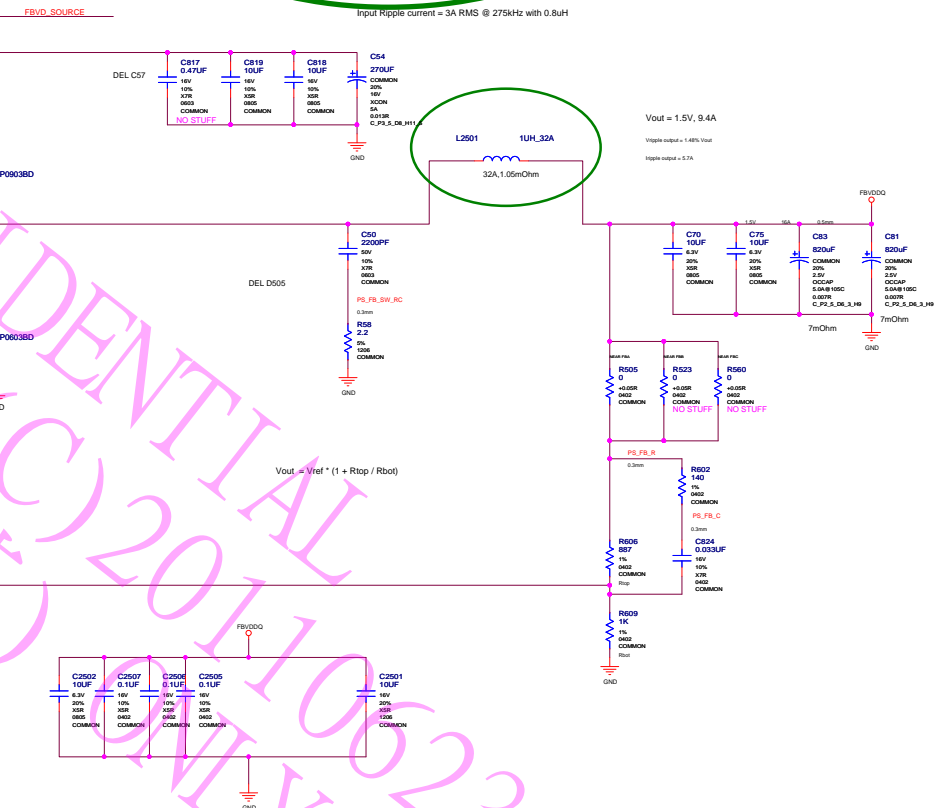
## FBVDDQ SOURCE OPTION



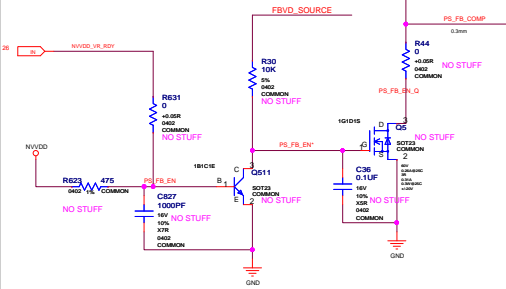
PEXVDD, 2.1A @ 1.05V

CONTROLLER	Fosc	VREF
UP6103A	300kHz	0.6V
APW7120	300kHz	0.8V
APW7165	300kHz	0.8V
RT8105	300kHz	0.8V
NCP1579	275kHz	0.8V
RT8101	300kHz	0.8V
UP6101B	300kHz	0.8V
LG783A	300kHz	0.8V
LG726A	275kHz	0.8V
FP6329	300kHz	0.6V
LG727	300kHz	0.8V

Input Ripple current = 3A RMS @ 275kHz with 0.8uH



## FBVDDQ/PEXVDD GATING


$$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$$


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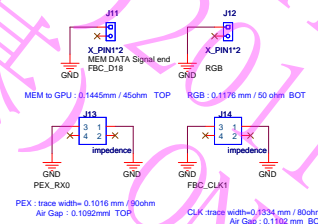
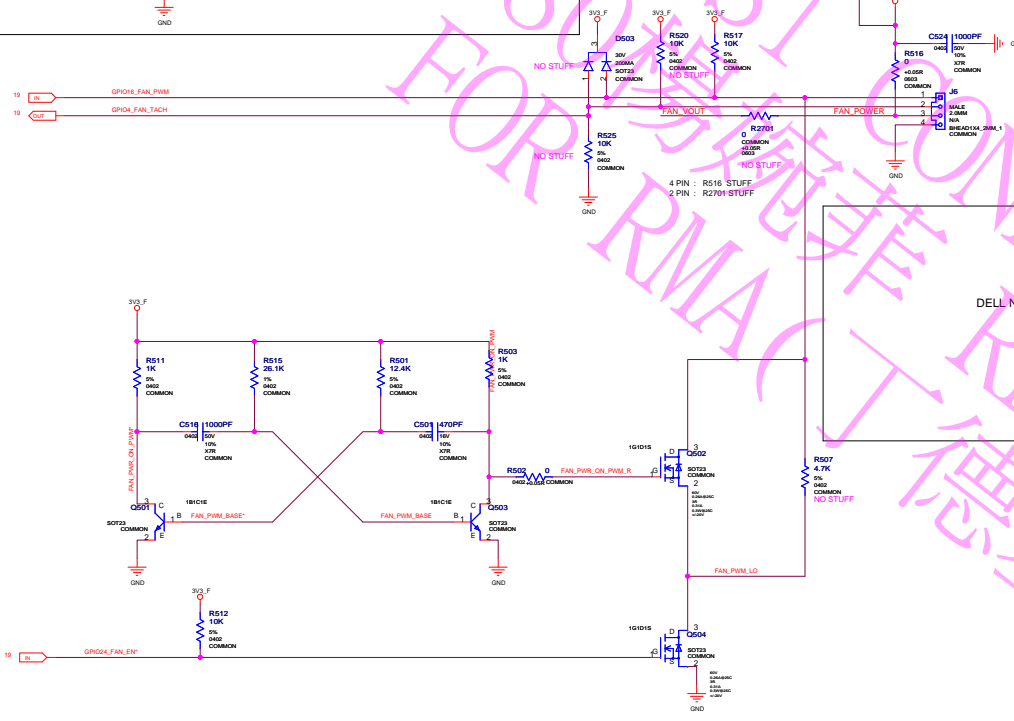
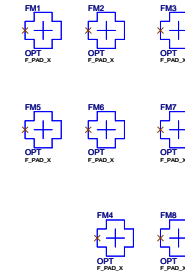
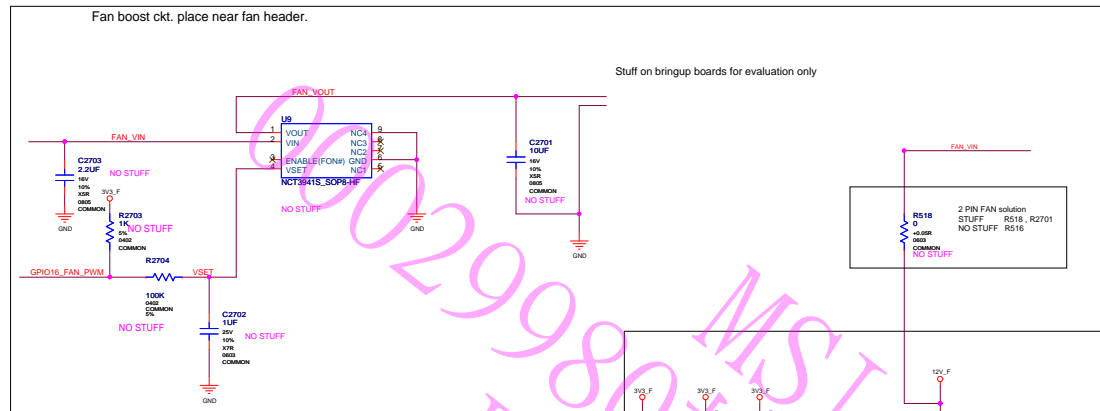
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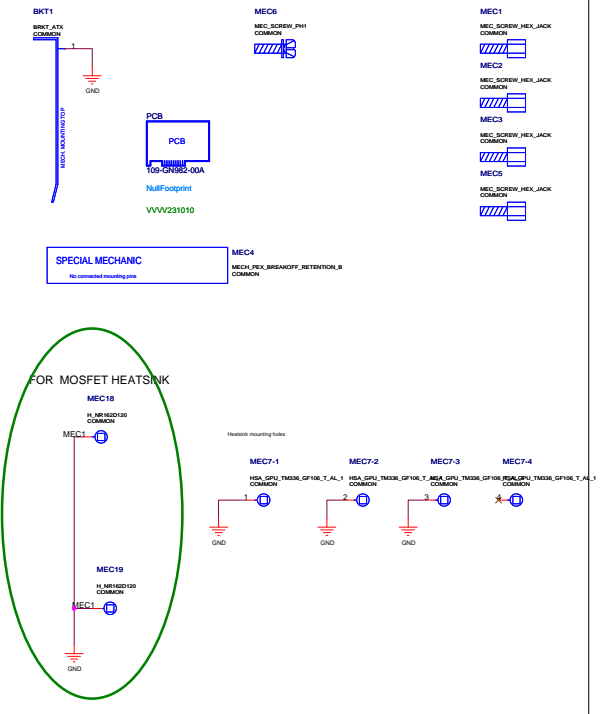
DATE	TIME	LOCATION	REMARKS



# Thermal, Mechanical, and Bracket



## Bracket



Copy from V207's DSN, only for build BOM

COOLING SOLUTION

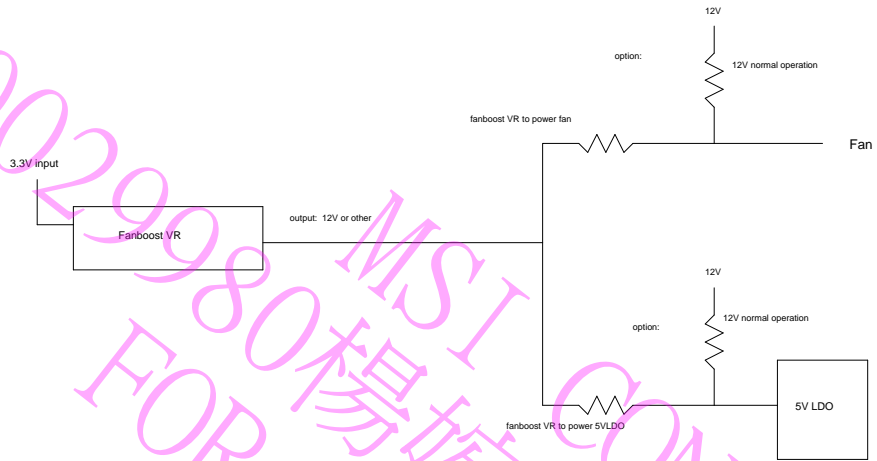
4 connected mounting pins

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PAGE/DETAIL	Fanboost VR, Multibraster, Thermal, and Mechanical

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ASSEMBLY	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. 31 LFP ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Block diagram of 12V options for fan and 5VLDO

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