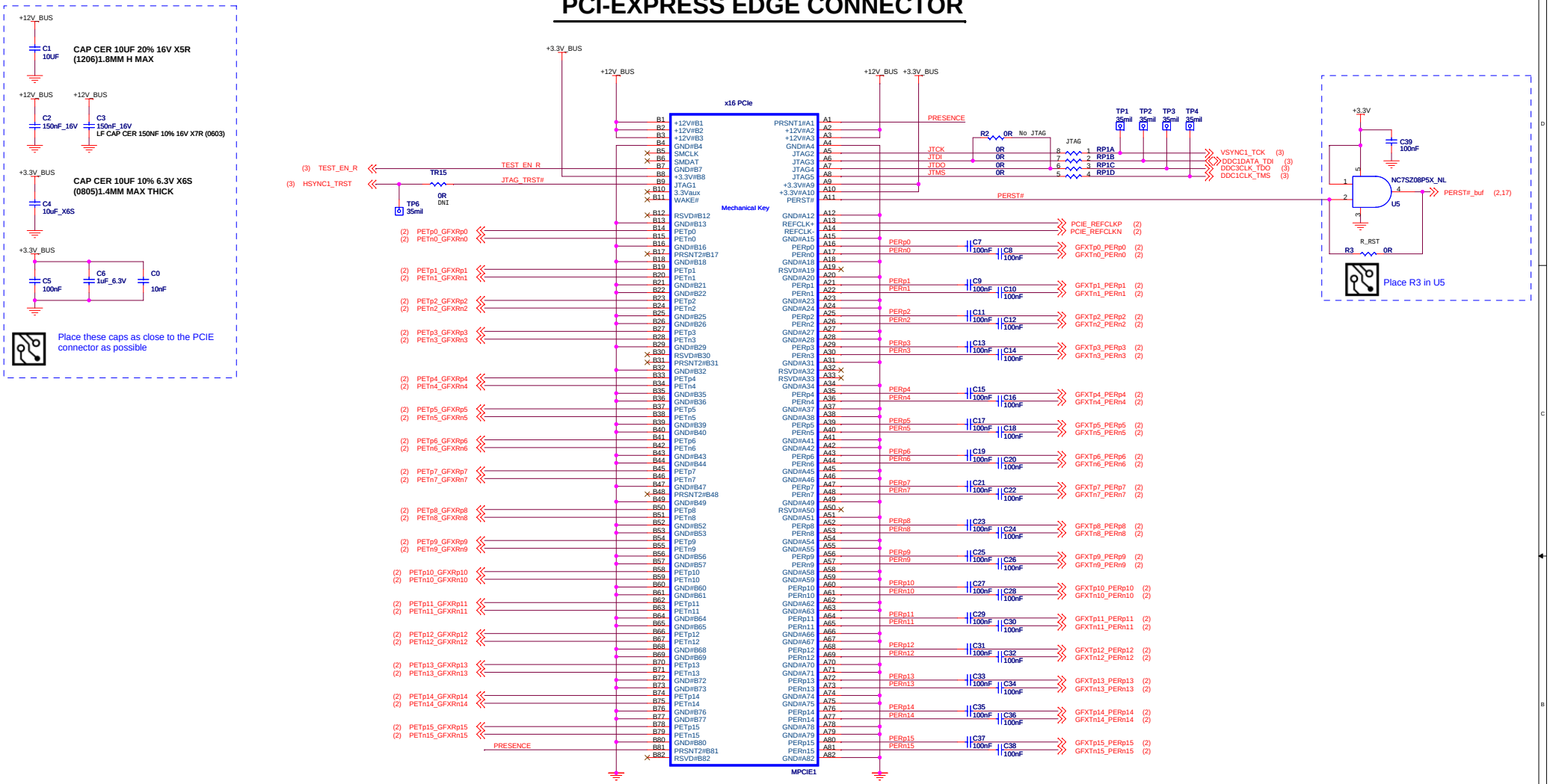
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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Canada, L3T 7X6
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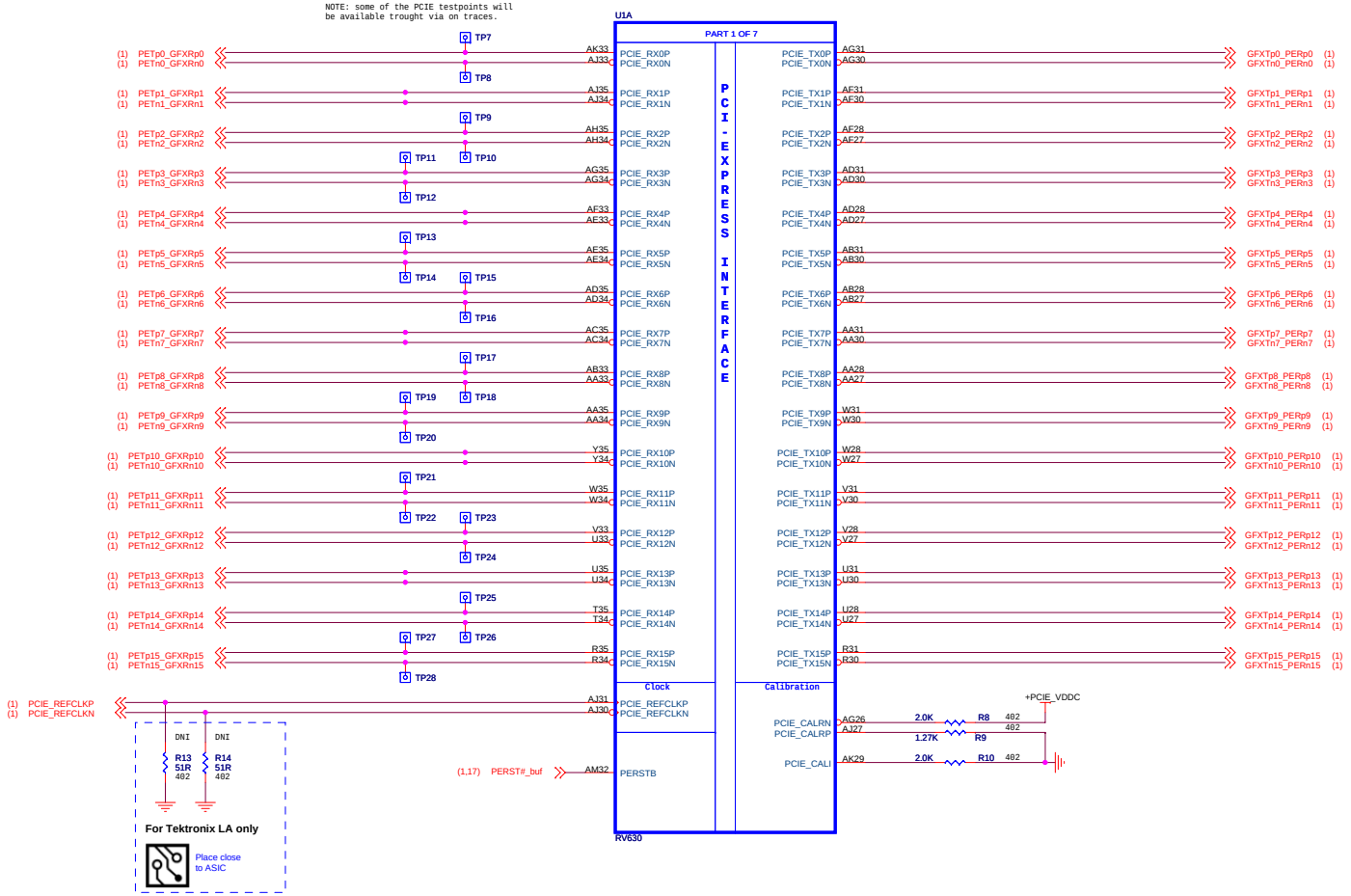
Title	RH RV630 - PCI-E Edge Connector		
Size C	Document Number 105-B101XX-00D		Rev 3
Date: Friday, February 16, 2007		Sheet 1 of 21	



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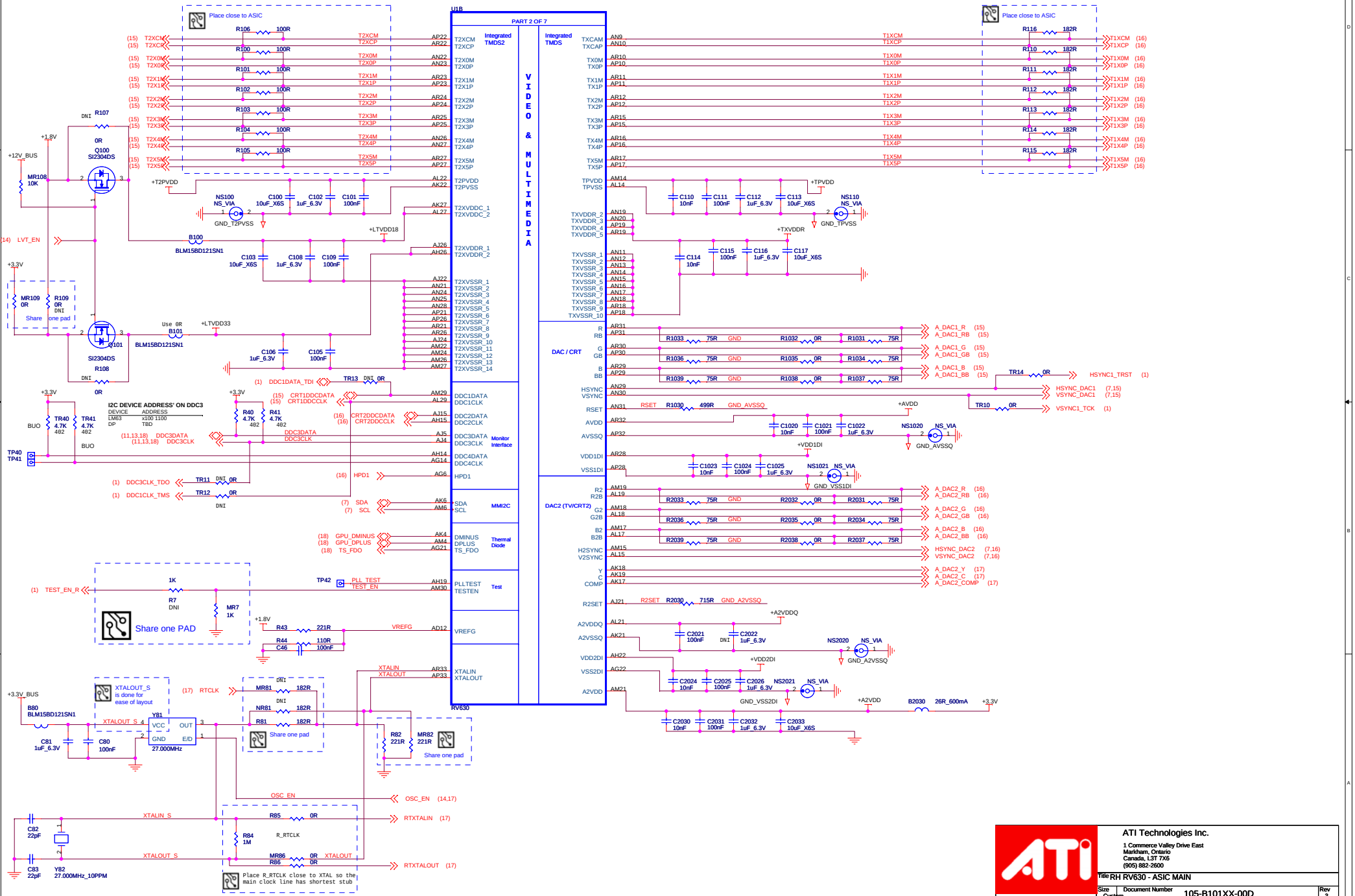
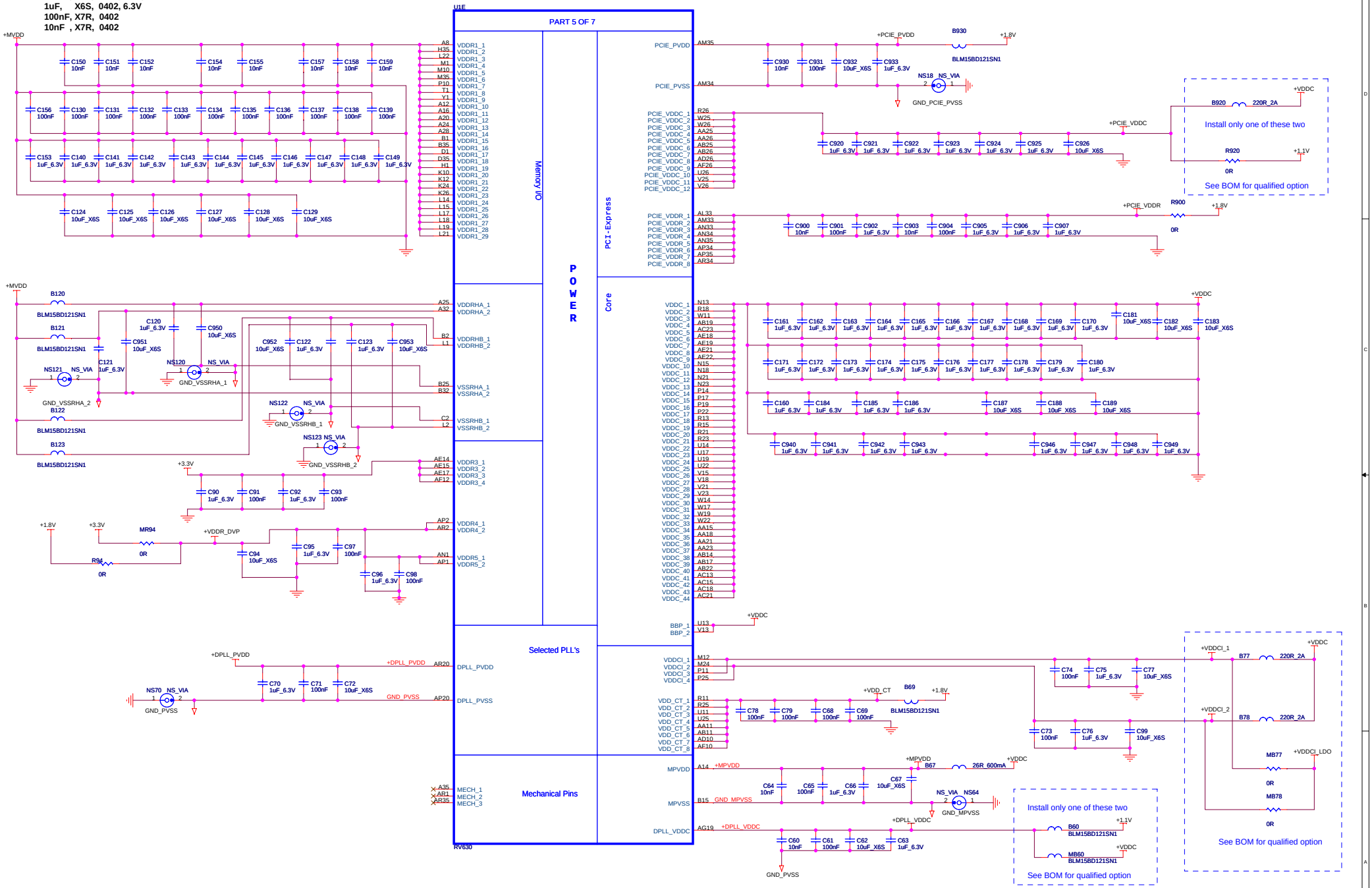
Title	RH RV630 - ASIC PCIE_Interface	
Size C	Document Number 105-B101XX-00D	Rev 3
Date: Friday, February 16, 2007	Sheet 2 of 21	

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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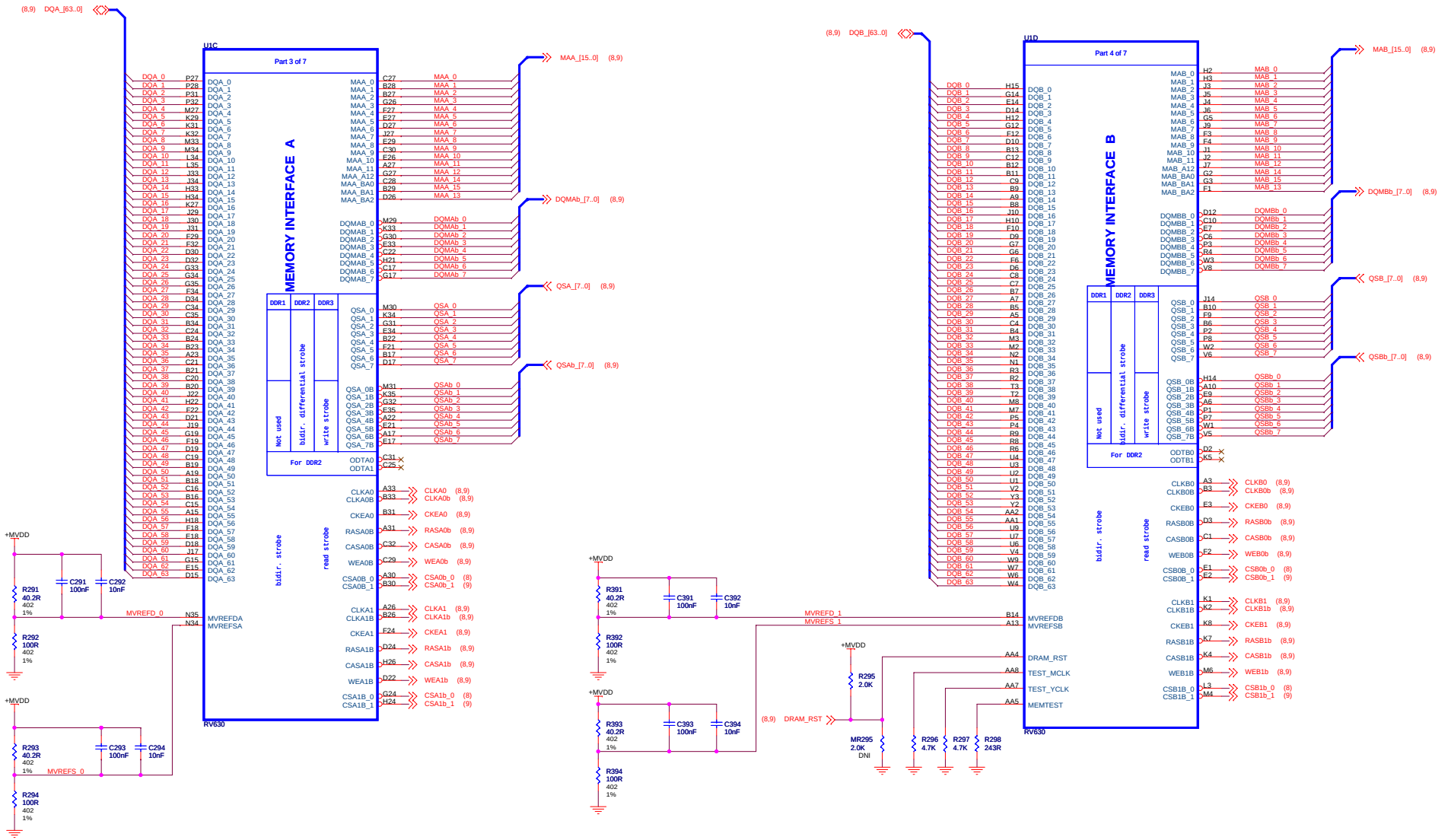
Title	RH RV630 - ASIC Power		
Size C	Document Number 105-B101XX-00D		Rev 3
Date: Thursday, February 15, 2007		Sheet 4 of 21	



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Title	RH RV630 - ASIC Memory Interface (Channel A & B)		
Size C	Document Number 105-B101XX-00D		Rev 3
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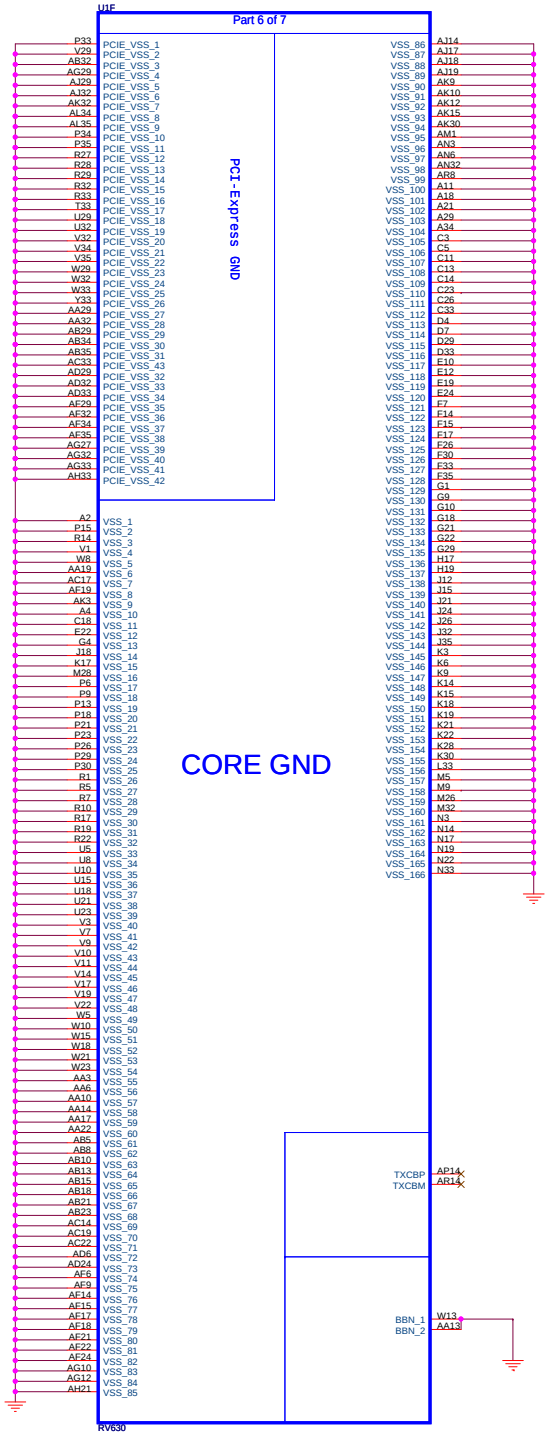

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Title: RH RV630 - ASIC Grounds

Size	Document Number	Rev
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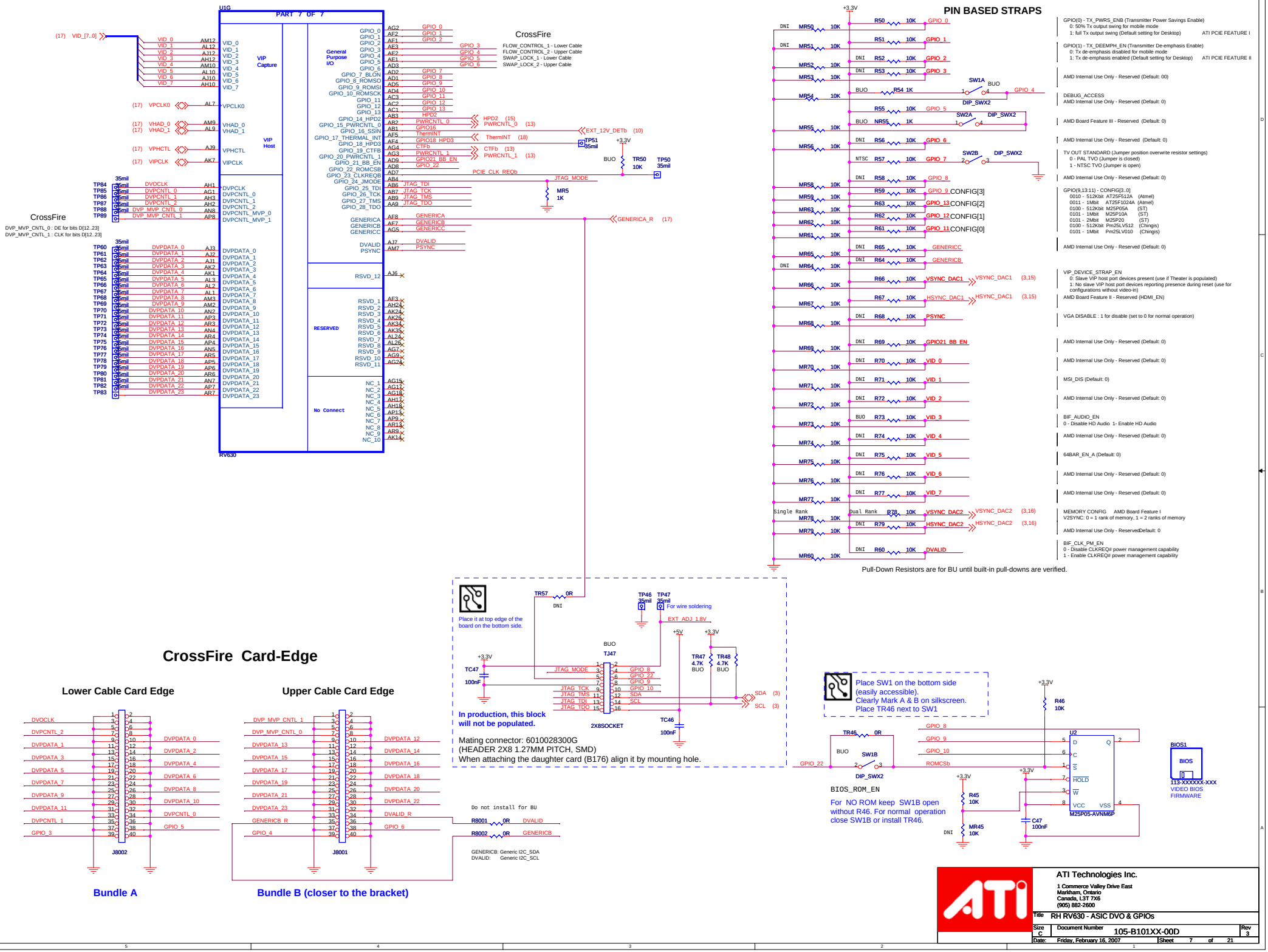
Date: Tuesday, February 06, 2007 Sheet 6 of 21


U1G
PART 7 OF 7
RV630
VIP Capture
VIP Host
CrossFire
General Purpose I/O
RESERVED
No Connect
PIN BASED STRAPS
CrossFire Card-Edge
Lower Cable Card Edge
Upper Cable Card Edge
Bundle A
Bundle B (closer to the bracket)
J8002
J8001
2X8SOCKET
In production, this block will not be populated.
Mating connector: 6010028300G
(HEADER 2X8 1.27MM PITCH, SMD)
When attaching the daughter card (B176) align it by mounting hole.
Place it at top edge of the board on the bottom side.
For wire soldering
Pull-Down Resistors are for BU until built-in pull-downs are verified.
Place SW1 on the bottom side (easily accessible).
Clearly Mark A & B on silkscreen.
Place TR46 next to SW1
BIOS_ROM_EN
For NO ROM keep SW1B open without R46. For normal operation close SW1B or install TR46.
BIOS1
BIOS
113-XXXXXX-XXX
VIDEO BIOS FIRMWARE
M25P05-AVNM6P
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600
Title RH RV630 - ASIC DVO & GPIOs
Size C
Document Number 105-B101XX-00D
Rev 3
Date: Friday, February 16, 2007
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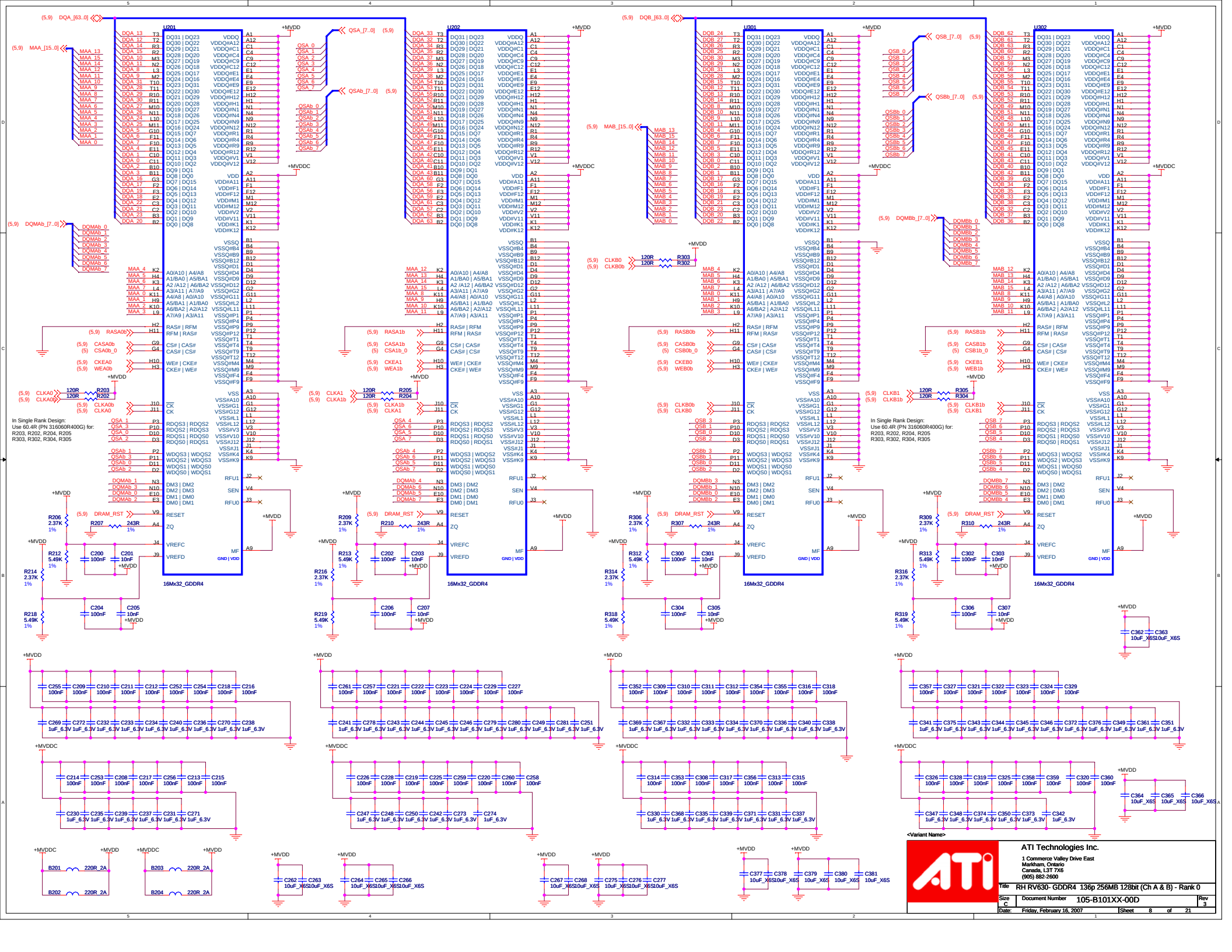
U201
U202
U301
U302
16Mx32_GDDR4
In Single Rank Design:
Use 60.4R (PN 316060R400G) for:
R203, R202, R204, R205
R303, R302, R304, R305
<Variant Name>
ATI Technologies Inc.
1 Commerce Valley Drive East
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(905) 882-2600
Title RH RV630- GDDR4 136p 256MB 128bit (Ch A & B) - Rank 0
Size C
Document Number 105-B101XX-00D
Rev 3
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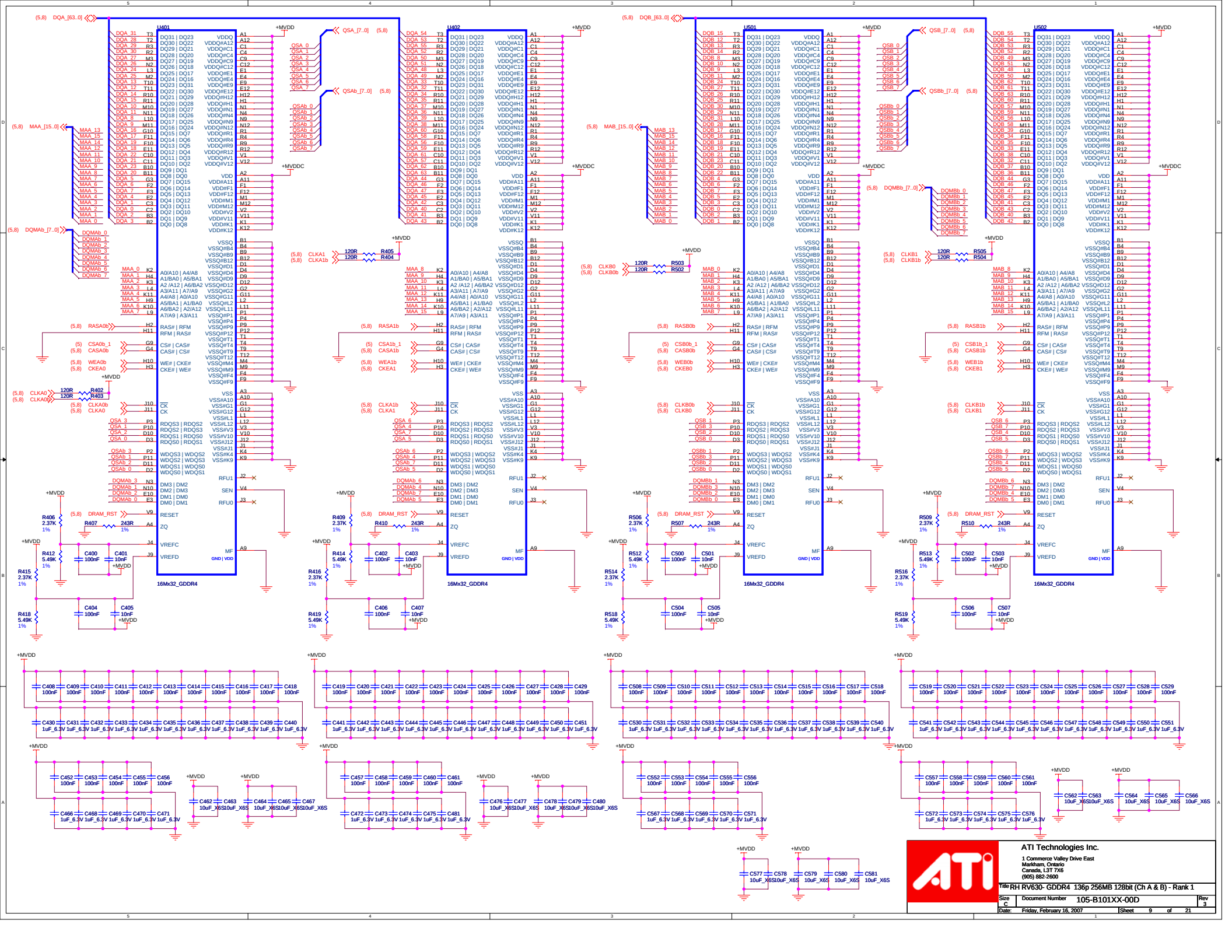
U401
U402
U501
U502
16Mx32_GDDR4
MVDD
MVDDC
DQA_[63..0]
DQB_[63..0]
MAA_[15..0]
MAB_[15..0]
DQMAb_[7..0]
DQMBb_[7..0]
QSA_[7..0]
QSAb_[7..0]
QSB_[7..0]
QSBb_[7..0]
RASA0b
RASA1b
RASB0b
RASB1b
CSA0b_1
CSA0b
CSA1b_1
CSA1b
CSB0b_1
CSB0b
CSB1b_1
CSB1b
CLKA0
CLKA0b
CLKA1
CLKA1b
CLKB0
CLKB0b
CLKB1
CLKB1b
WEA0b
CKEA0
WEA1b
CKEA1
WEB0b
CKEB0
WEB1b
CKEB1
DRAM_RST
120R
R402
R403
R404
R405
R503
R502
R504
R505
R406
R407
R409
R410
R506
R507
R509
R510
243R
2.37K
5.49K
R412
R414
R512
R513
R415
R416
R514
R516
R418
R419
R518
R519
C400
C401
C402
C403
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C507
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10nF
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C547
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C550
C551
1uF_6.3V
C452
C453
C454
C455
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C458
C459
C460
C461
C552
C553
C554
C555
C556
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C480
C562
C563
C564
C565
C566
C567
C568
C569
C570
C571
C572
C573
C574
C575
C576
10uF_X6S
C577
C578
C579
C580
C581
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Markham, Ontario
Canada, L3T 7X6
(905) 882-2600
Title RH RV630- GDDR4 136p 256MB 128bit (Ch A & B) - Rank 1
Size C
Document Number 105-B101XX-00D
Rev 3
Date: Friday, February 16, 2007
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Information on Compatable Controller Parts

	PWM IC #1	PWM IC #2	PWM IC #3	PWM IC #4	
Gate drive voltage	5V, 8V, 12V	5V, 8V, 12V	5V only	12V only	
Vref	0.6V	0.6V	0.6V	0.6V	
Bootstrap diodes	Internal (DNP D601, D611)	Internal (DNP D601, D611)	External (Populate D601, D611)	Internal (DNP D601, D611)	
Phase current adjustable (unbalanced between phases)	Yes	Yes	Yes	TBD	
Option Pin Selection					
Pin 10 (IOUT/IMAX/DROOP)	IOUT/DROOP (R662)	IOUT/IMAX	IOUT	IOUT/IMAX	
Pin 11 (RT)	R_RT ~= 10,000,000/Fsw	TBD	R_RT ~= 18,600,000/Fsw	TBD	
Pin 12 (COMP/DROOP)	COMP	DROOP (R663)	COMP	COMP	
Pin 14 (SS/ICOMP)	SS/EN	GND (SS fixed internally)	ICOMP (SS dependent on Fsw)	SS	
Pin 16 (REFOUT/POK)	POK (Open drain)	IREFOUT/POK POK voltage = 1.2V	INREFOUT/POK PGood voltage = 1.25V	INREFOUT/PGOOD Vrefout = 0.6V	
Pin 21 (VCCDRV/DROOP)	VCCDRV	VCCDRV	DROOP (R664)	DROOP (R664)	

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661

External Detection Circuit and Indication

Cases	Behaviour	Notifications
External cable not plugged in +12V_BUS not in regulation	12V_EXT_DETb = X EN1 -> "0" (by Ri2) ENb1 -> 3.3V ENBUS = "0"	VDDC disabled
External cable not plugged in +12V_BUS in regulation	12V_EXT_DETb = "1" EN1 -> 3V (by Ri1 and Ri2) ENb1 = 0V ENBUS = "1"	VDDC enabled External Power Missing
External cable plugged in +12V_XXX not in regulation	12V_EXT_DETb = "0" EN1 < 3V (due to low 12V) ENb1 = 3.3V ENBUS = "0"	VDDC disabled
External cable plugged in +12V_XXX in regulation	12V_EXT_DETb = "0" EN1 -> 3V ENb1 = 0V ENBUS = "1"	VDDC enabled Normal Operation

SMPS03 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	1.2V ; +2.5%/-2.5%	0.8V ~ 1.5V
Vout ripple (DC)	TBD	
Iout	TBD	55A (target 60A) max
Step load	TBD	
Vout ripple (AC)	TBD	
Switching Freq.	TBD	50kHz ~ 1MHz
Protections		

- Bulk Cap `C SMT, H<10mm (C641, C642, C643)
1. UCC APXE2R5ARA102MH80G, 8x7.7mm, 1000uF, 12mR, 2.5V, 4260mArms, ATI PN - ?
2. UCC APXE2R5ARA152MHA0G, 8x10mm, 1500uF, 10mR, 2.5V, 5220mArms, ATI PN - ?

- Bulk Cap `C TH, H<10mm (NC641, NC642, NC643)
1. Fujitsu FP-2R5RE102M-L8xx, 8x8mm, 1000uF, 6mR, 2.5V, 5600mArms, ATI PN - ?
2. Fujitsu FP-2R5RE152M-L8xx, 8x8mm, 1500uF, 6mR, 2.5V, 5600mArms, ATI PN - ?

- SP/TANT/POS Cap `C SMT (MC641, MC642, MC643)
1. Sanyo 2R5TPD1000M5, POSCAP, 4mmH, 1000uF, 5mR, 2.5V, 6100mArms, 4230010800G
2. NEC/TOKIN TEPSGD0E108M5-12R, SPCAP?, 3mmH, 1000uF, 5mR, 2.5V, 5477mArms, 4230010801G

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Address	1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600
Title	RH RV630 - VDDC SMPS03
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Date:	Friday, February 16, 2007
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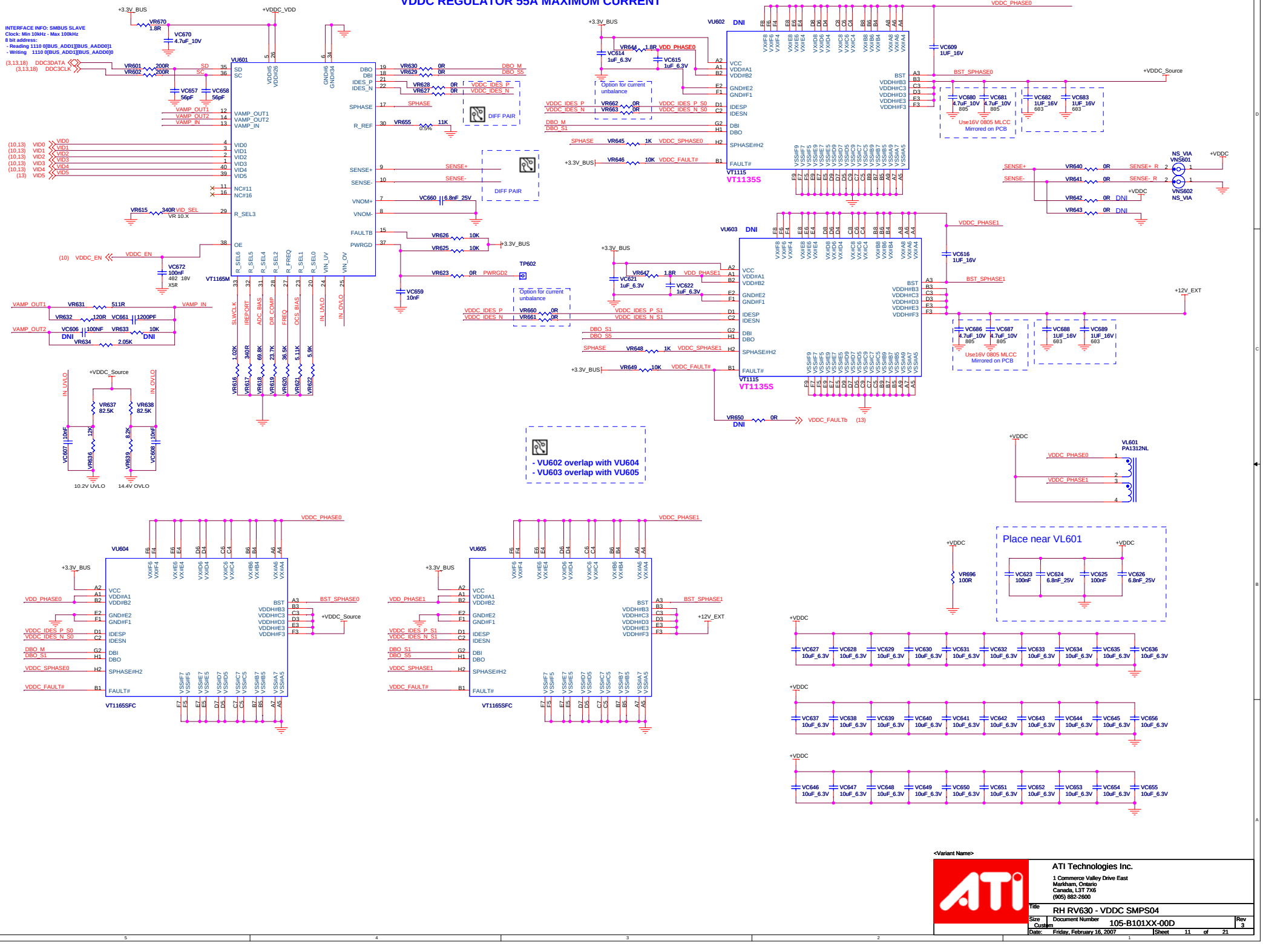
VDDC REGULATOR 55A MAXIMUM CURRENT



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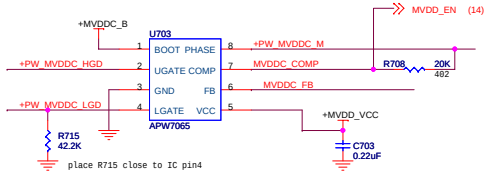
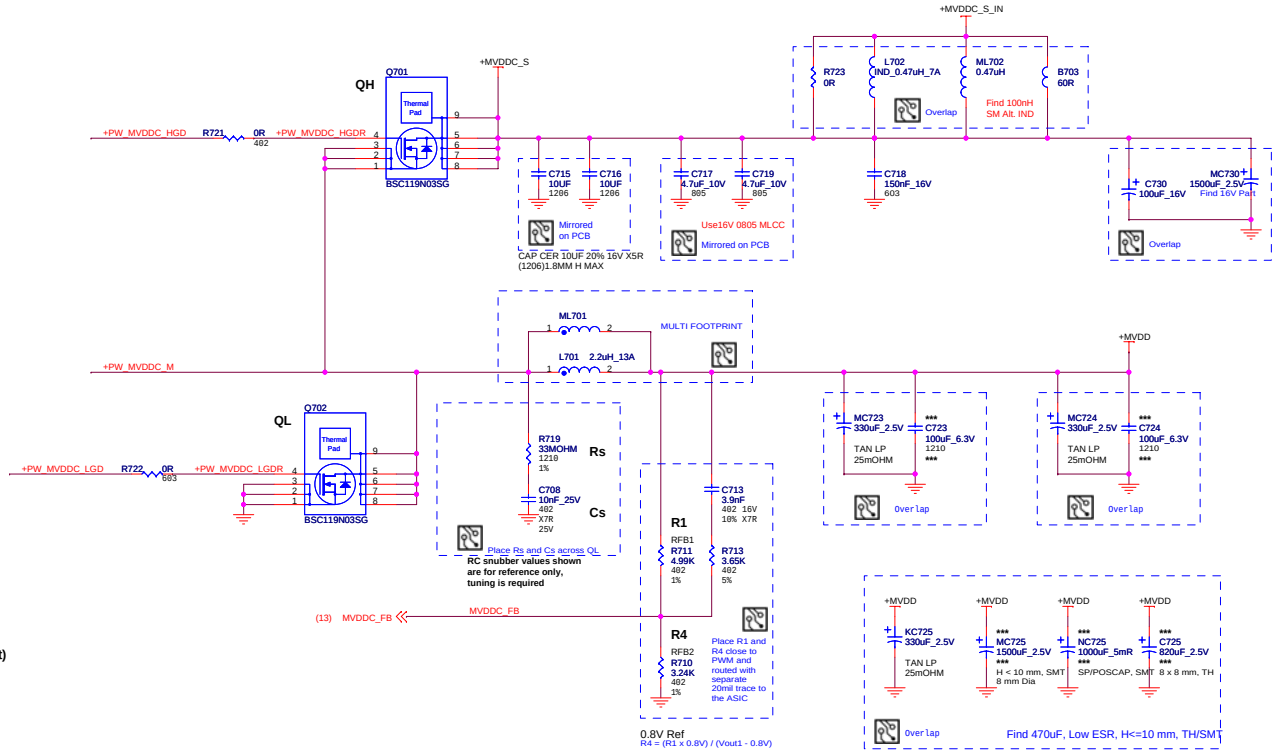
<Variant Name>	Title: RH RV630 - VDDC SMPS04		
	Size: Custom	Document Number: 105-B101XX-00D	Rev: 3
	Date: Friday, February 16, 2007	Sheet 11 of 21	

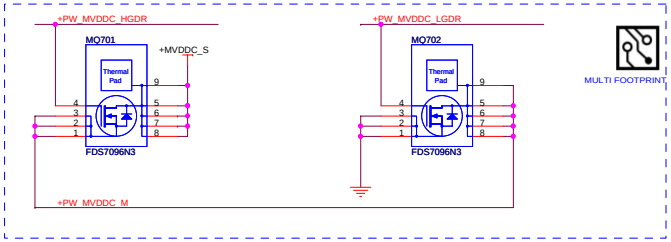


List of supported foodprint

The following ICs are not necessarily evaluated by AMD, please refer to BOM for evaluation status

- **ANPEC APW7120/APW7065 (12V)**
- **CAT CAT7583 (12V)**
- **INTERSIL ISL6545**
- **NEXSEM NX2114/2307**
- **RICHTEK RT9214/RT8101**
- **OnSemi ON1582**
- **uPI UP6101 (No Ext_Vref in)**
- **uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**





SMPS02- Regulator for MVDD

Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G

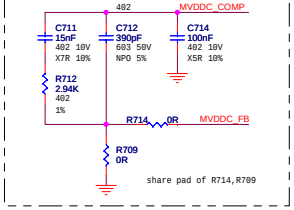
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

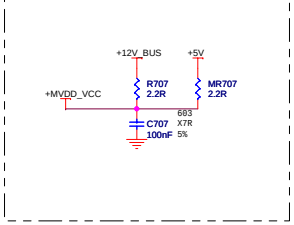
Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

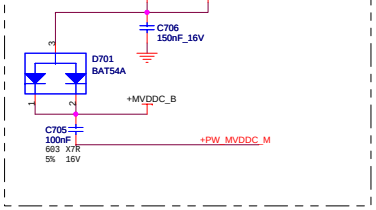
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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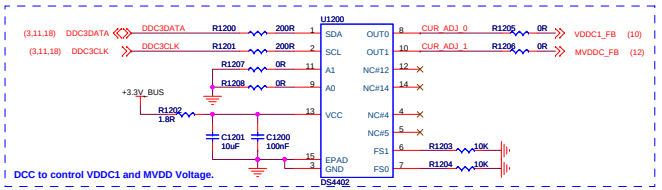
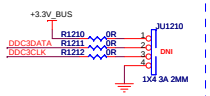
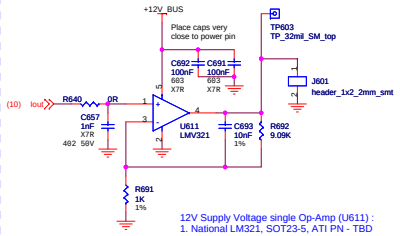
Title: RH RV630 - MVDD SMPS02
Size: Custom | Document Number: 105-B101XX-00D | Rev: 3
Date: Friday, February 16, 2007 | Sheet 12 of 21



DCC to control VDDC1 and MVDD Voltage.

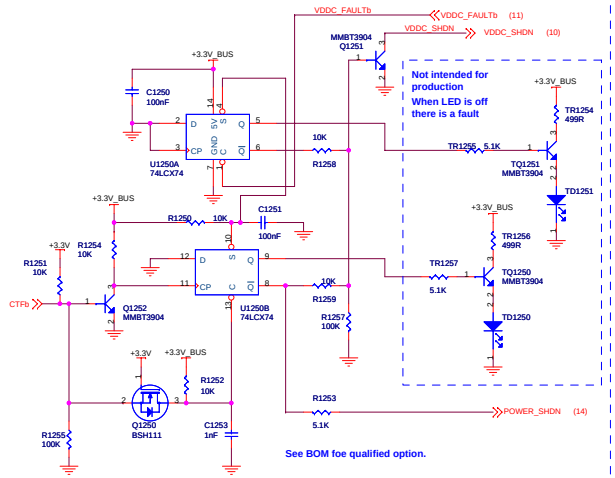


I2C Debugging
Header for testing purpose

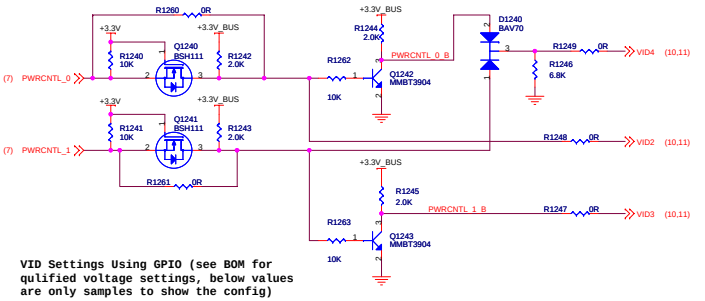


12V Supply Voltage single Op-Amp (U611) :
1. National LM321, SOT23-5, ATI PN - TBD
2. TI alternate? ATI PN - TBD

132-
For Testing purposes only

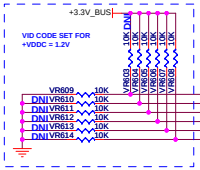


See BOM foe qualified option.

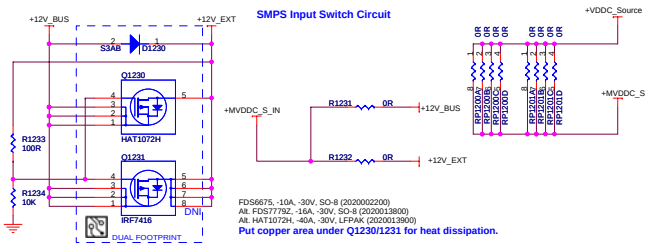


VID Settings Using GPIO (see BOM for qulified voltage settings, below values are only samples to show the config)

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	VID4	VID3	VID2	Output Voltage		
0	0	1	1	0	0.950V		
0	1	0	1	1	1.250V		
1	0	1	0	0	1.150V		
1	1	1	0	1	1.050V		Power-up Default



132-
VID ~ Vout Setting for VDDC



FDS6675, -10A, -30V, SO-8 (2020002200)
Alt. FDS7779Z, -16A, -30V, SO-8 (2020013800)
Alt. HAT1072H, -40A, -30V, LFPAK (2020013900)
Put copper area under Q1230/1231 for heat dissipation.

VDDC, MVDD SMPS Input Options

Option	Cases	VDDC Input	MVDD Input	Status
Option #1 Populate: B701 D702 D703	Normal Operation External cable plugged in	Phase 1 powered from +12V_BUS Phase 2 powered from +12V_EXT	Powered from +12V_EXT	Board works properly
	Power On When External cable not plugged in	Phase 1 powered from +12V_BUS Phase 2 powered from +12V_EXT	Powered from +12V_BUS	Bootup to Dos warning Message Screen
Option #2 Populate: B702	Normal Operation External cable plugged in	Phase 1 powered from +12V_BUS Phase 2 powered from +12V_EXT	Powered from +12V_BUS	Board works properly
	Power On When External cable not plugged in	Phase 1 powered from +12V_BUS Phase 2 powered from +12V_EXT	Powered from +12V_BUS	Bootup to Dos warning Message Screen

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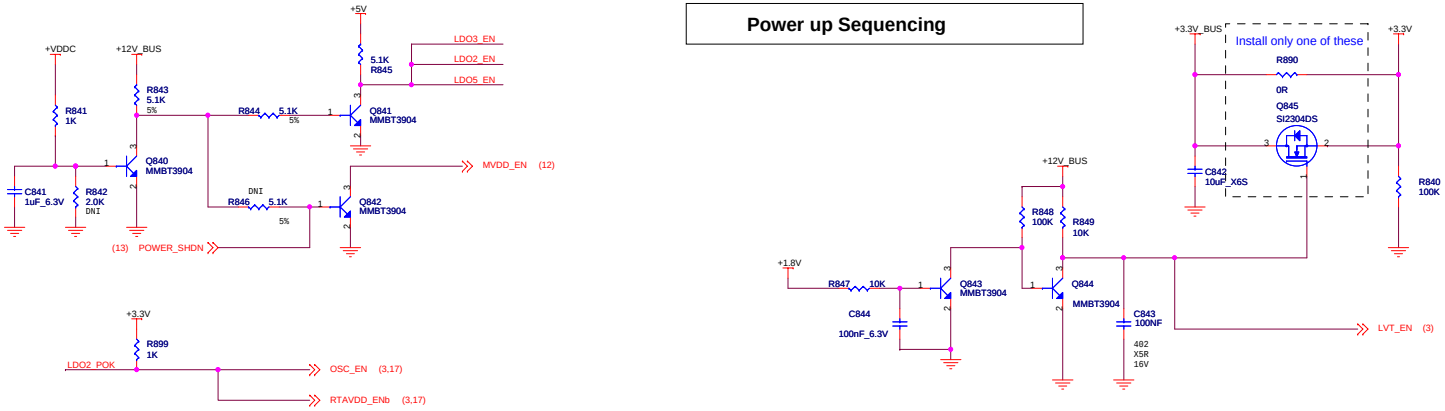
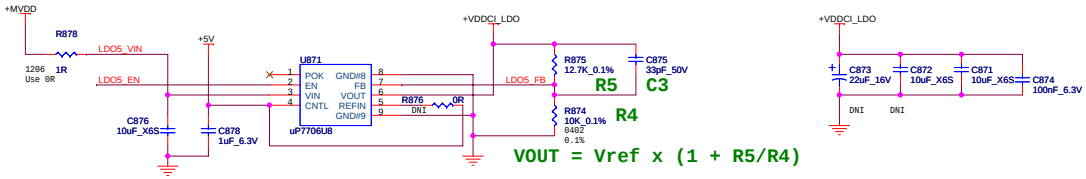
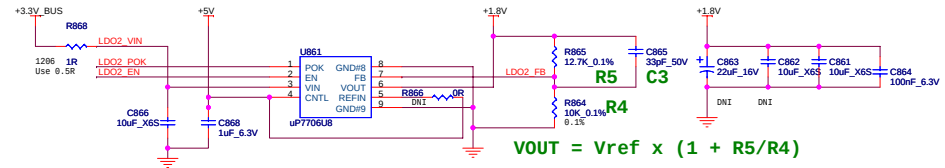
Power up Sequencing



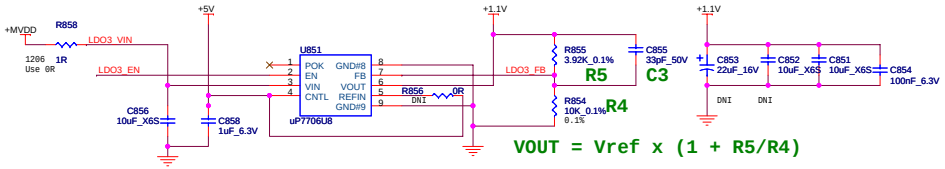
LDO #6: Vin = 1.6V to 2.1V MAX Vout = +1.25V +/- 2% Iout = 1.5A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



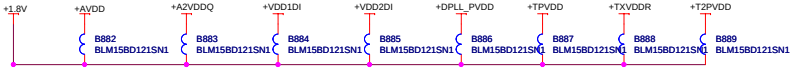
LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



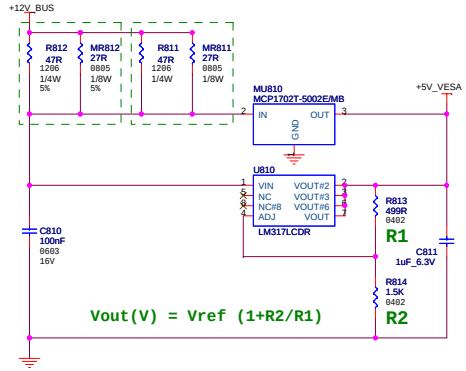
LDO #3: Vin = +1.45V to 2.1VMAX Vout = +1.1V +/- 2% Iout = 1.1A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

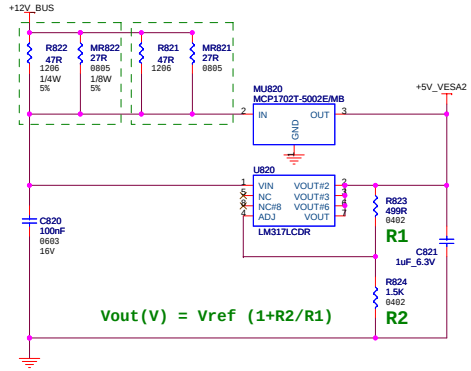


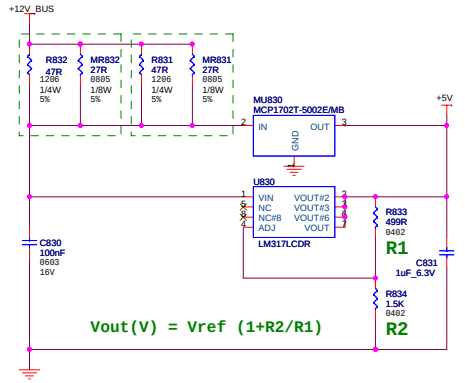
Shared Power Rails



Regulators for +5V, +5V_VESA and +5V_VESA2







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Title	RH RV630 - Linear Regulators	
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See BOM for qualified filters

(3) A_DAC1_R → R1001 75R 402 → C1004 8.0pF 402 → L1001 68nH_300mA → R1024 0R → C1001 12pF_50V 402 → A_R_DAC1_M → L1004 36NH

(3) A_DAC1_RB → R1027 37.4R

(3) A_DAC1_G → R1002 75R 402 → C1005 8.0pF 402 → L1002 68nH_300mA → R1025 0R → C1002 12pF_50V 402 → A_G_DAC1_M → L1005 36NH

(3) A_DAC1_GB → R1028 37.4R

(3) A_DAC1_B → R1003 75R 402 → C1006 8.0pF 402 → L1003 68nH_300mA → R1026 0R → C1003 12pF_50V 402 → A_B_DAC1_M → L1006 36NH

(3) A_DAC1_BB → R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

For ESD Protection

D1001 CM1213-04 (+3.3V; CH3, CH2, Vp, Vn, CH4, CH1)

D1002 CM1213-04 (+5V_VESA; CH3, CH2, Vp, Vn, CH4, CH1)

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

+5V_VESA

C1010 68pF 603

MJ1001 G3179C219-005

MJ1001 pin	Signal
1	R
2	G
3	B
11	MS0
12	MS1
4	MS2
15	MS3
9	NC
13	HS
14	VS
5	VSS
6	VSS#6
7	VSS#7
8	VSS#8
10	VSS#10
16	CASE
17	CASE#17

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

(3) CRT1DDCDATA → R1004 10K (+3.3V) → Q1001 BSH111 → R1005 2.2K (+5V) → DDCDATA_DAC1_5V → R1006 33R 402 → DDCDATA_DAC1_R

(3) CRT1DDCCLK → R1007 10K (+3.3V) → Q1002 BSH111 → R1008 2.2K (+5V) → DDCCLK_DAC1_5V → R1009 33R 402 → DDCCLK_DAC1_R

(3,7) HSYNC_DAC1 → C1999 100nF → U1999A 74AHCT125 → HSYNC_DAC1_B → R1010 10R 402 → HSYNC_DAC1_R

(3,7) VSYNC_DAC1 → U1999B 74AHCT125 → VSYNC_DAC1_B → R1011 10R 402 → VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

Q1021 MMBT3904 (+3.3V) → R1022 10K → HPD_DVI2

(7) HPD2 → R1023 10K

+5V_VESA

J1001 DVI_CONNECTOR

J1001 pin	Signal
25	CASE
1	TMDS Data2-
2	TMDS Data2+
3	TMDS Data2/4 Shield
4	TMDS Data4-
5	TMDS Data4+
6	DDC Clock
7	DDC Data
8	Analog VSYNC
9	TMDS Data1-
10	TMDS Data1+
11	TMDS Data1/3 Shield
12	TMDS Data3-
13	TMDS Data3+
14	+5V Power
15	GND (for +5V)
16	Hot Plug Detect
17	TMDS Data0-
18	TMDS Data0+
19	TMDS Data0/5 Shield
20	TMDS Data5-
21	TMDS Data5+
22	TMDS Clock Shield
23	TMDS Clock+
24	TMDS Clock-
C1	Analog Red
C2	Analog Green
C3	Analog Blue
C4	Analog HYNC
C5	Analog GND
C6	Analog GND#C6
26	CASE#26
27	CASE#27
28	CASE#28
29	CASE#29
30	CASE#30

(3) T2X2M / (3) T2X2P
(3) T2X4M / (3) T2X4P
DDCCLK_DAC1_R
DDCDATA_DAC1_R
VSYNC_DAC1_R
(3) T2X1M / (3) T2X1P
(3) T2X3M / (3) T2X3P
HPD_DVI2
(3) T2X0M / (3) T2X0P
(3) T2X5M / (3) T2X5P
(3) T2XCP / (3) T2XCM
A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
HSYNC_DAC1_R

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Title	RH RV630 - DAC1/TMDS2	
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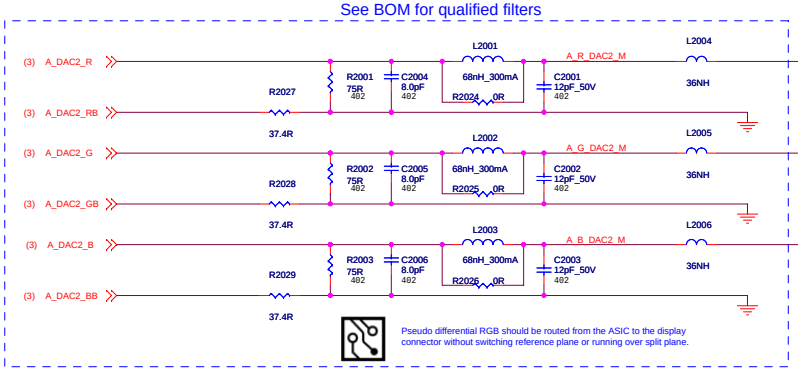
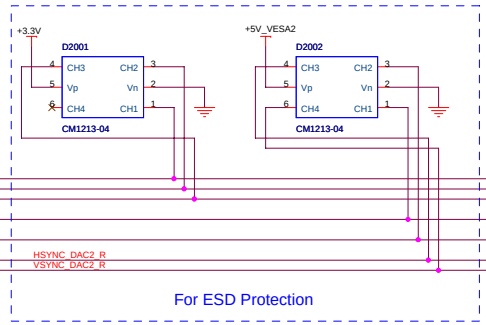
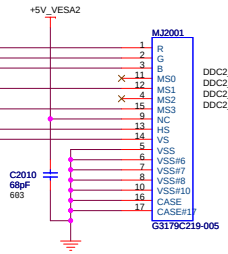
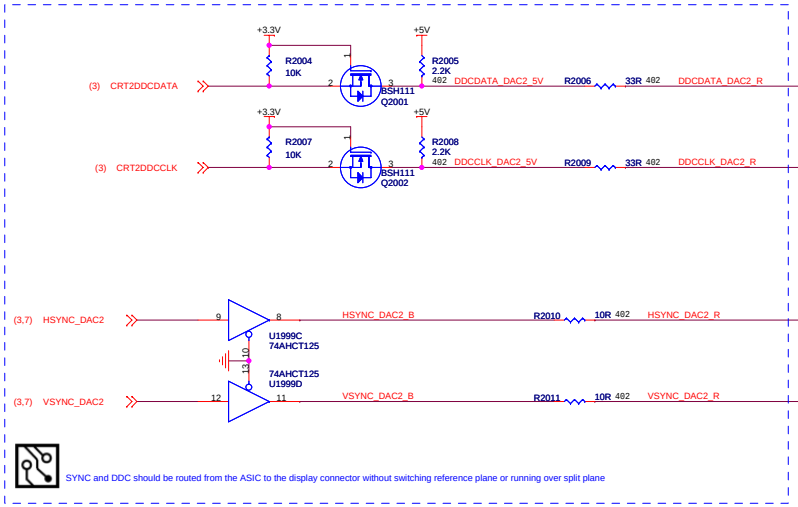
See BOM for qualified filters





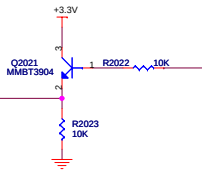
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R

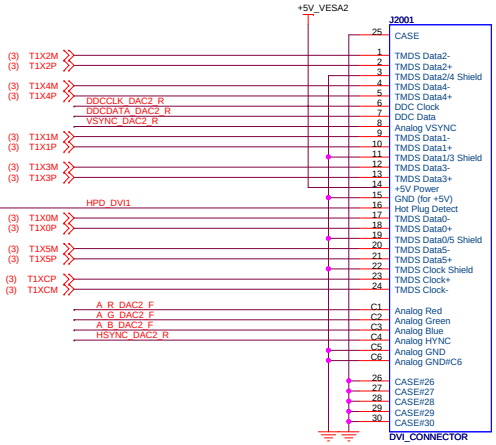




DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





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Title	RH RV630 - DAC2/TMDS1	
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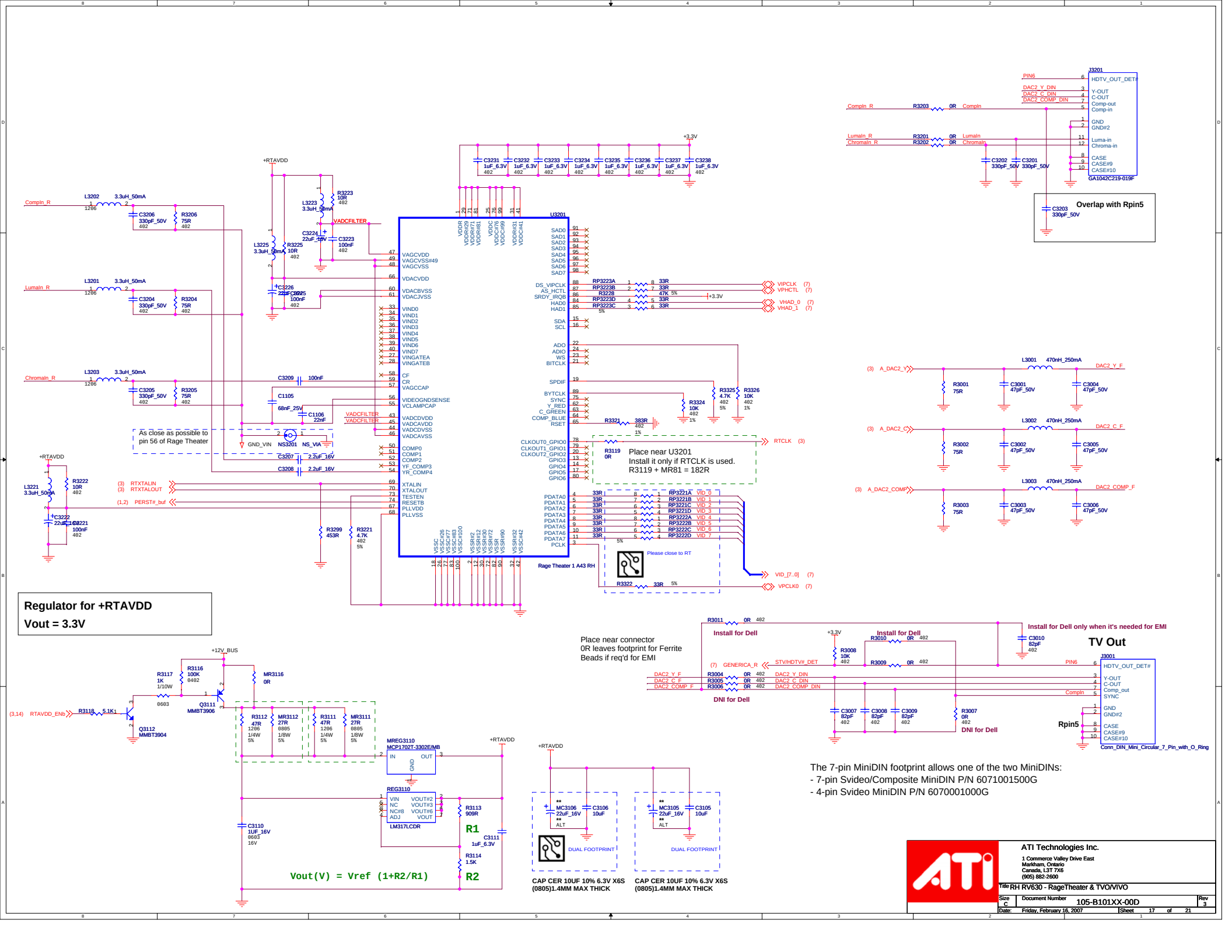
Regulator for +RTAVDD
Vout = 3.3V
Vout(V) = Vref (1+R2/R1)
R1
R2
Rage Theater 1 A43 RH
Place near U3201
Install it only if RTCLK is used.
R3119 + MR81 = 182R
Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI
Overlap with Rpin5
TV Out
Rpin5
Conn_DIN_Mini_Circular_7_Pin_with_O_Ring
The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G
CAP CER 10UF 10% 6.3V X6S
(0805)1.4MM MAX THICK
CAP CER 10UF 10% 6.3V X6S
(0805)1.4MM MAX THICK
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RH RV630 - RageTheater & TVO/VIVO
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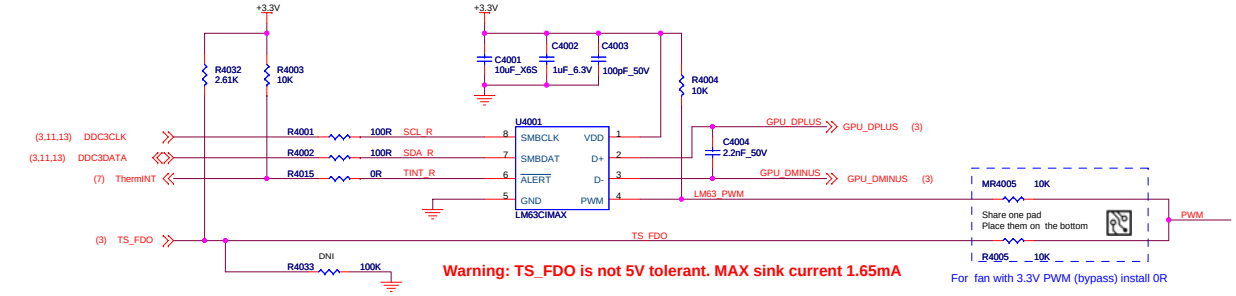
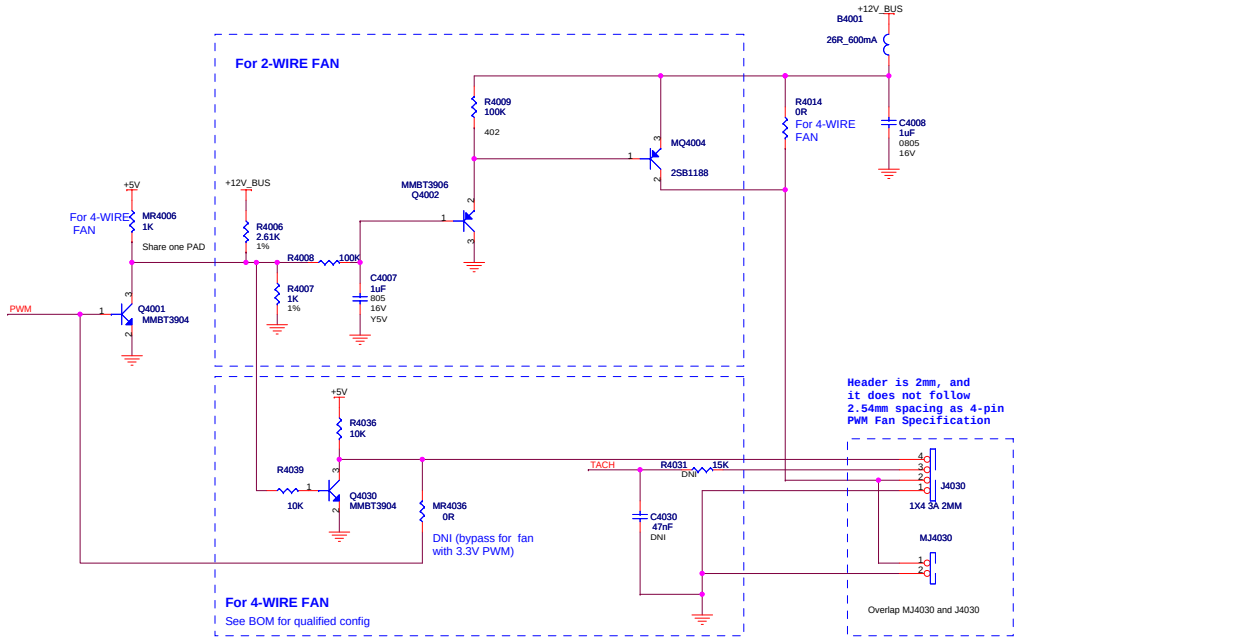
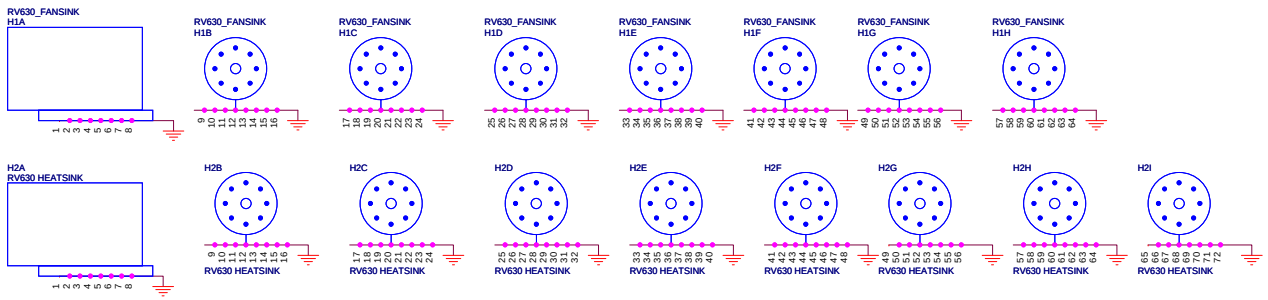
External thermal sensor is for testing, and will not be populated in production.







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DVI/DVI SCREWS with top tab

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY1
ANTISTATIC BAG
6_X_11

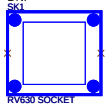
BKT1
BRACKET
8020044300G

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

MT1
MT_Hole_0.136 TM 5.5 BM 7.0

MT2
MT_Hole_0.136_in_6VIA

DNI
SK1



RV630 SOCKET

PCB1

109-B101xx-00D

<Variant Name>

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<variant Name>

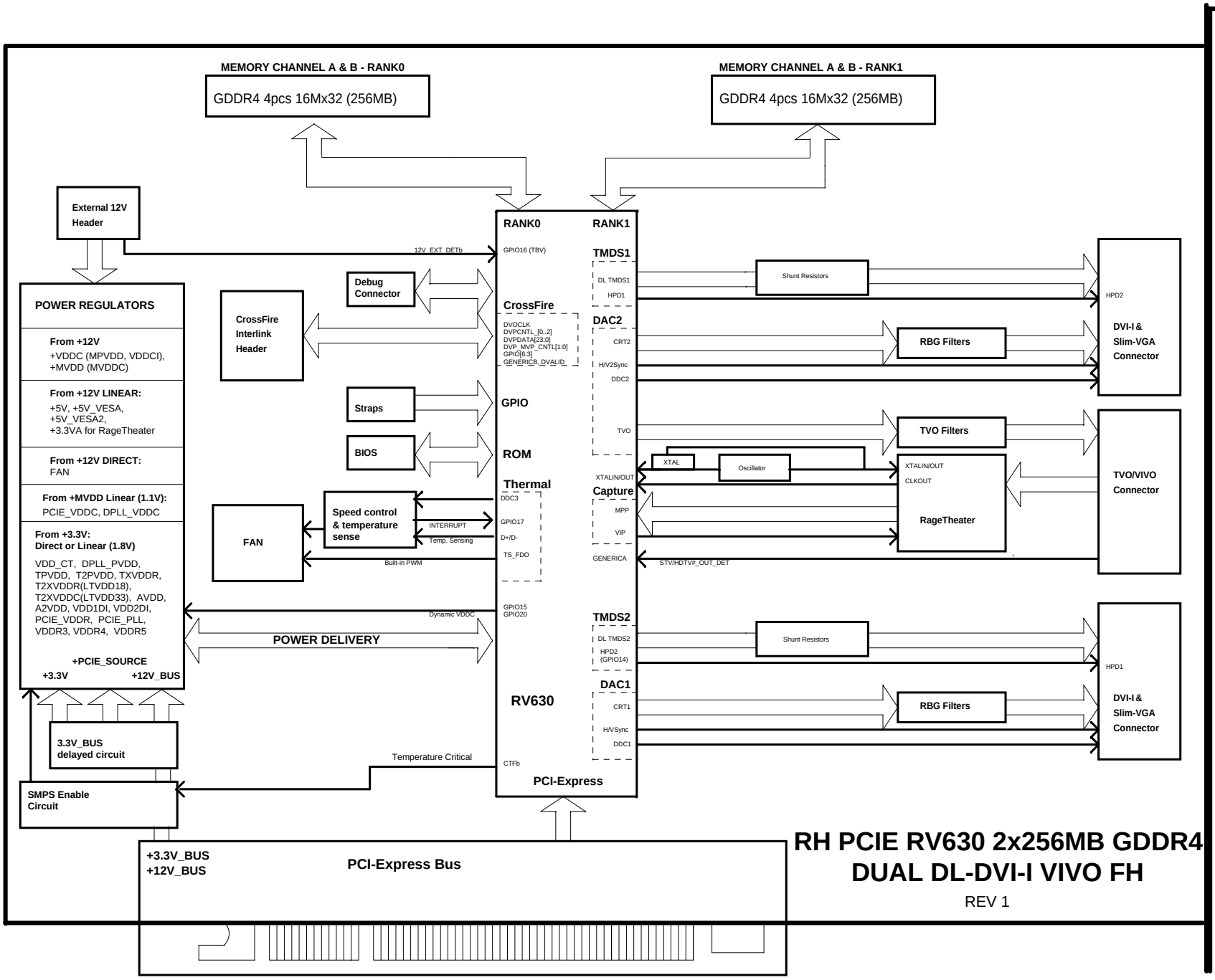
Title	Schematic No.	Date:
RH PCIE RV630 2x256MB GDDR4 DUAL DL-DVI-I VIVO FH	105-B101XX-00D	Saturday, February 17, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact ATI representative to obtain latest BOM closest to the application desired.**

Rev 3

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/11/08	Initial design for RV630 pipe cleaner
1	00B	06/11/18	Regrouping of parts (Cosmetic) Power-up sequecning updated VID control and EXT detection are updated VDDC SMPS updated
2	00C	06/12/08	(pg 05) Re-assignment of MAA_13, MAA_14, MAA_15, MAB_13, MAB_14, and MAB_15 (pg 10) SMPS updated (pg 11) SMPS updated (pg 12) SMPS updated - Adding +5V option (pg 14) Adding R891 (pg 18) Adding Heatsink symbols H1 and H2 (pg 49) Adding MT1 (Layout) Heatsink mounting holes modified and one added.
3	00D	07/02/06	Removing some of test featuers (pg 14) Renaming LDO1 to LDO5 and for connecting to VDDCI if needed (pg 18) Merging 2-wire and 4-wire fan buffer circuitry (pg 3, 4) Adding 10uF caps to VDDRH, VDDCI, T2XVDDR, T2PVDD, and PLL rails (pg 10) Adding buffer for EXT_DETECT line, R1229 and C630 (pg 13) Adding option to control shut down circuitry for critical temperature (pg 14) Removing R891 (pg 7) Adding DIP switch to GPIO7 and GPIO5 (pg 1, 3) Adding TR10 to TR15 to support legacy JTAG for internal testing.



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Title	RH PCIE-2 RV630 2x256MB GDDR4 DUAL DL-DVI-I VIVO FH	
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