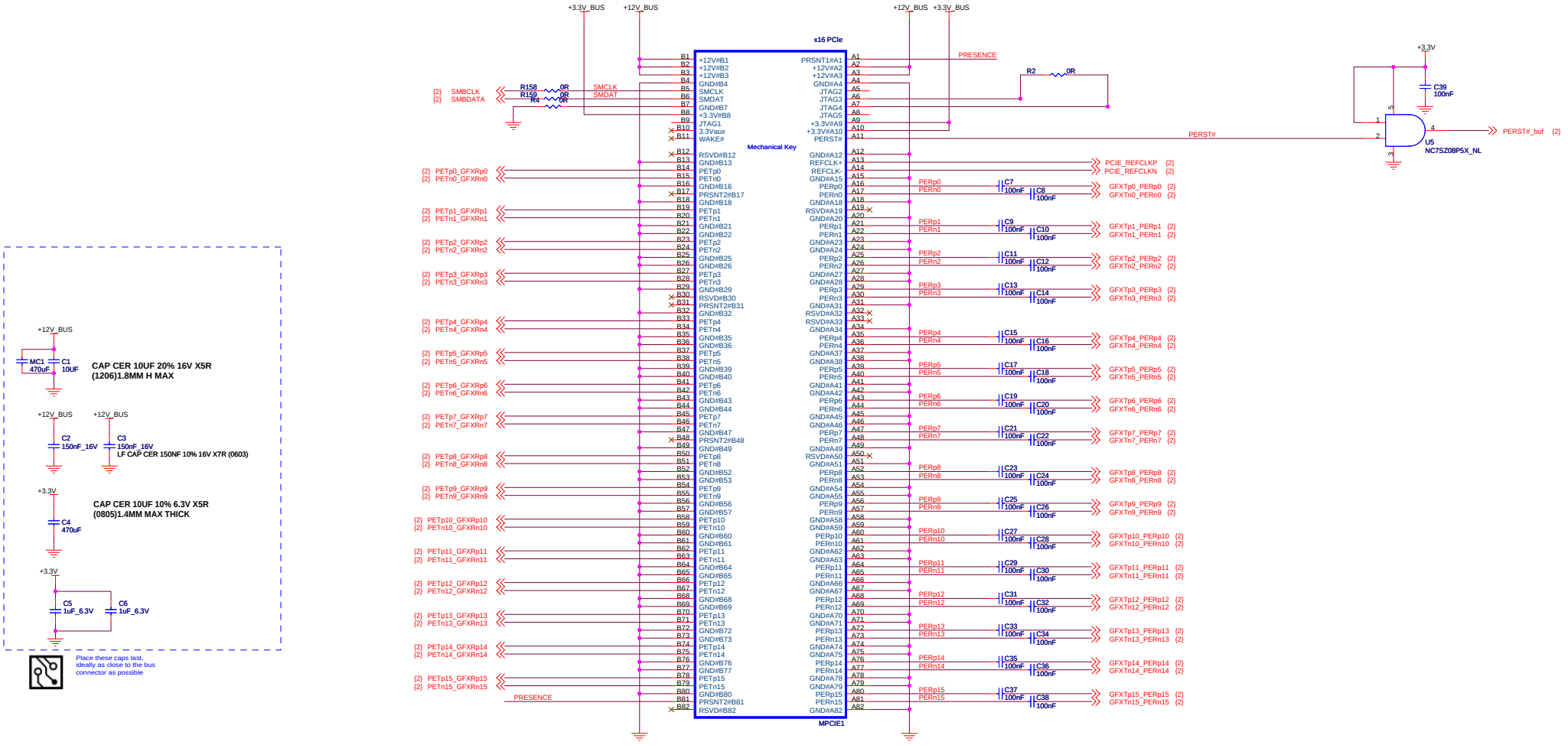
PCI-EXPRESS EDGE CONNECTOR

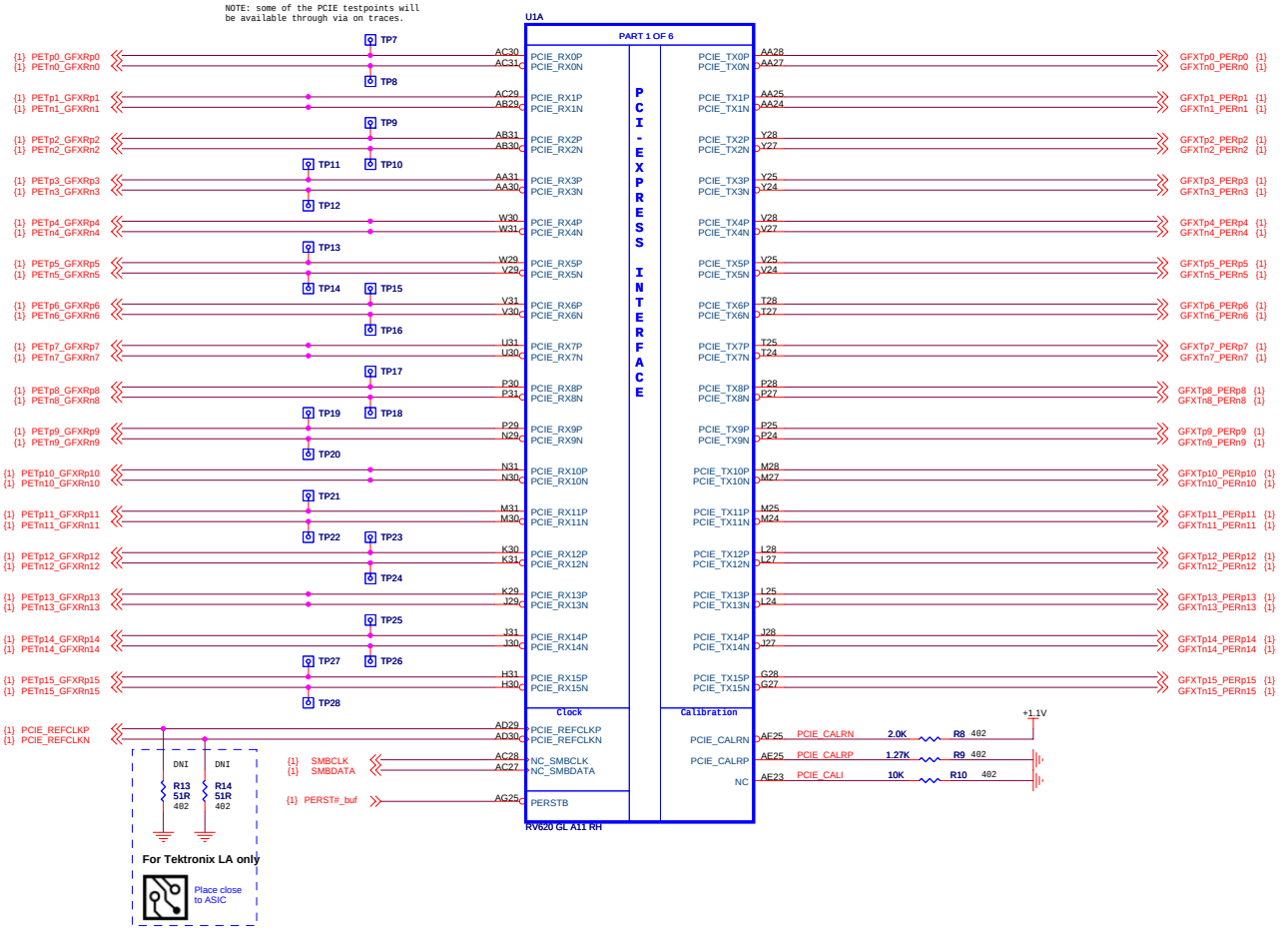


SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Thursday, October 25, 2007
Rev	1
Sheet	1 of 20
Title	RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No.	105-B350xx-00B



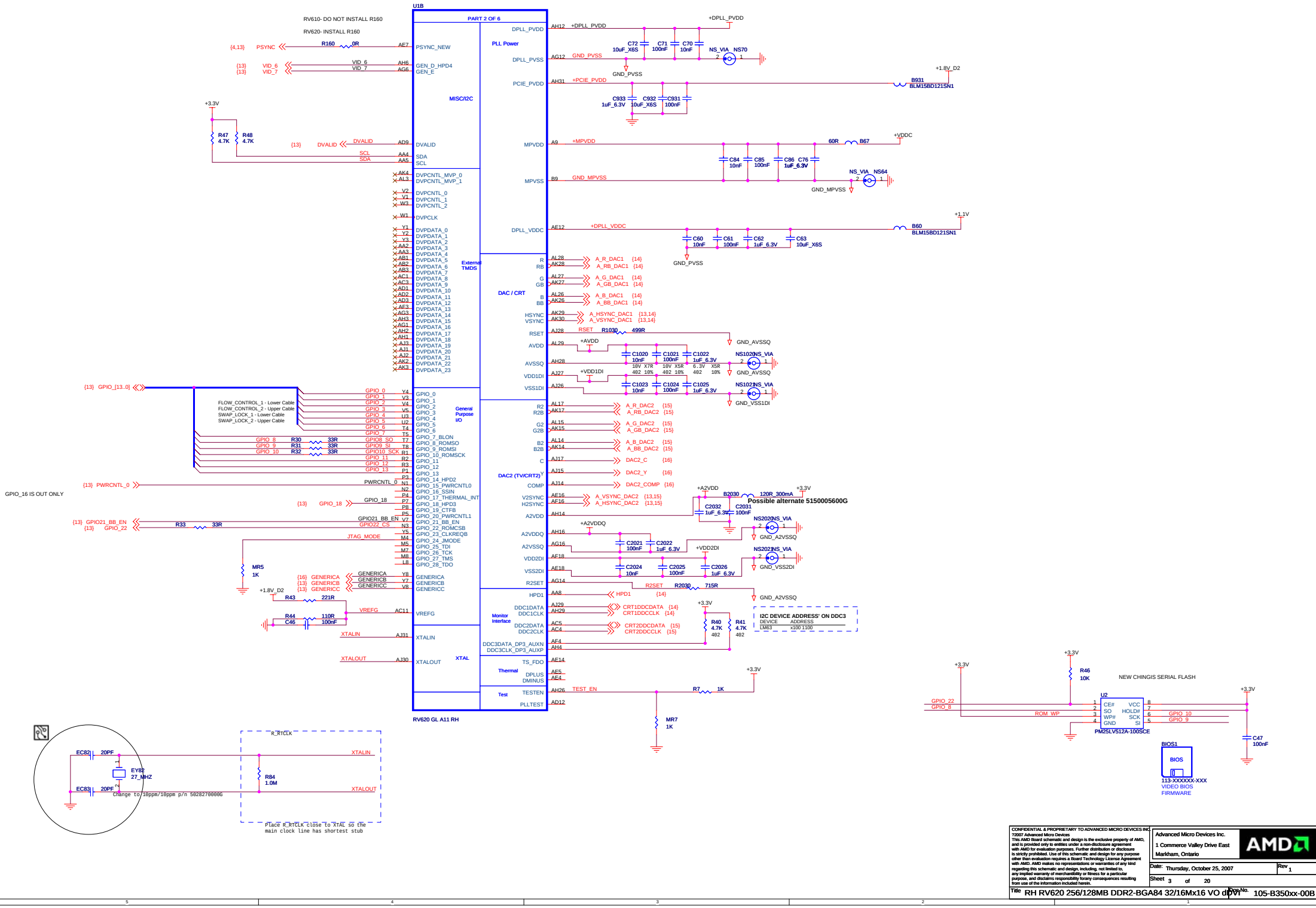
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

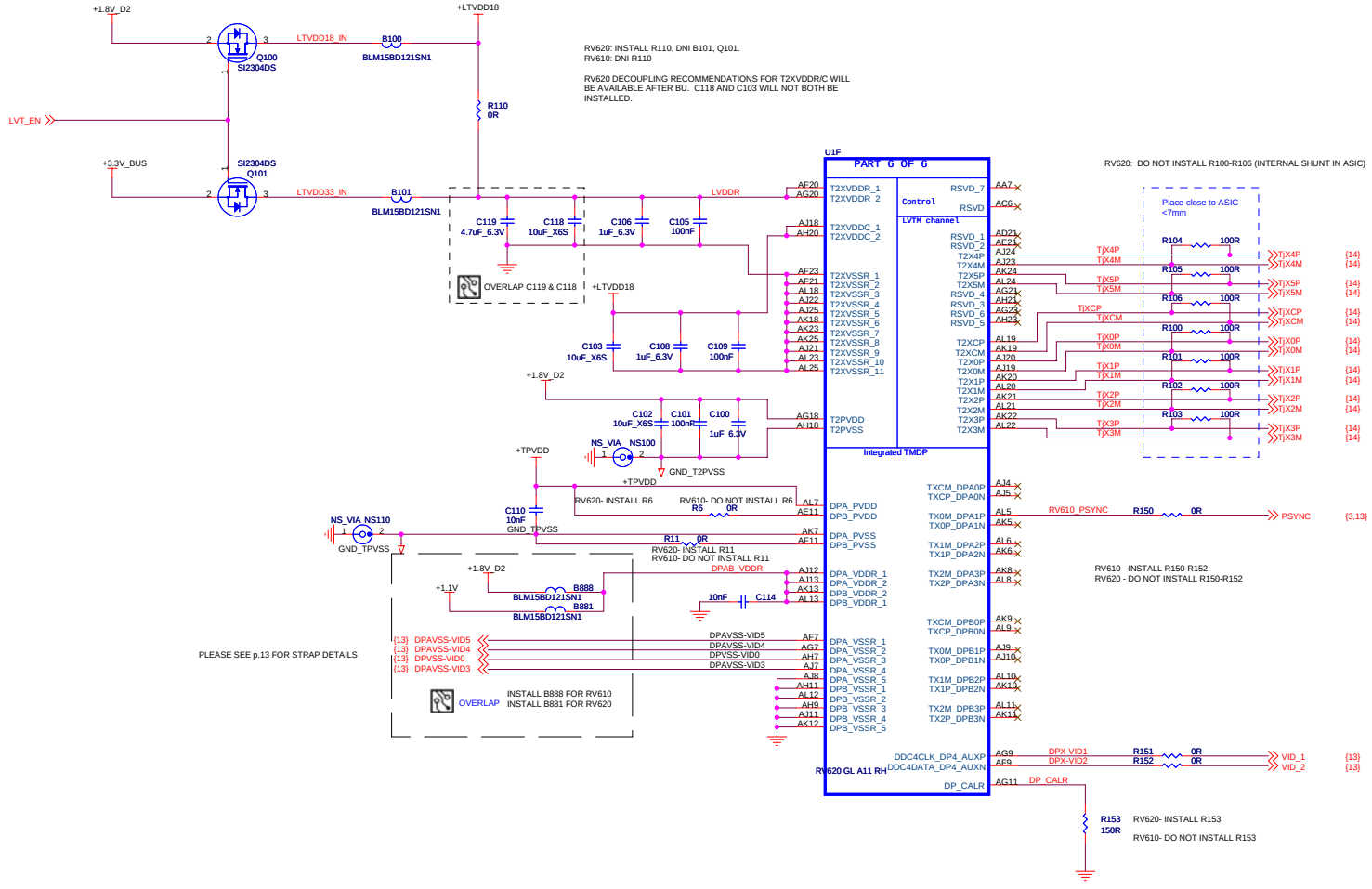
Date: Thursday, October 25, 2007 Rev 1

Sheet 2 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

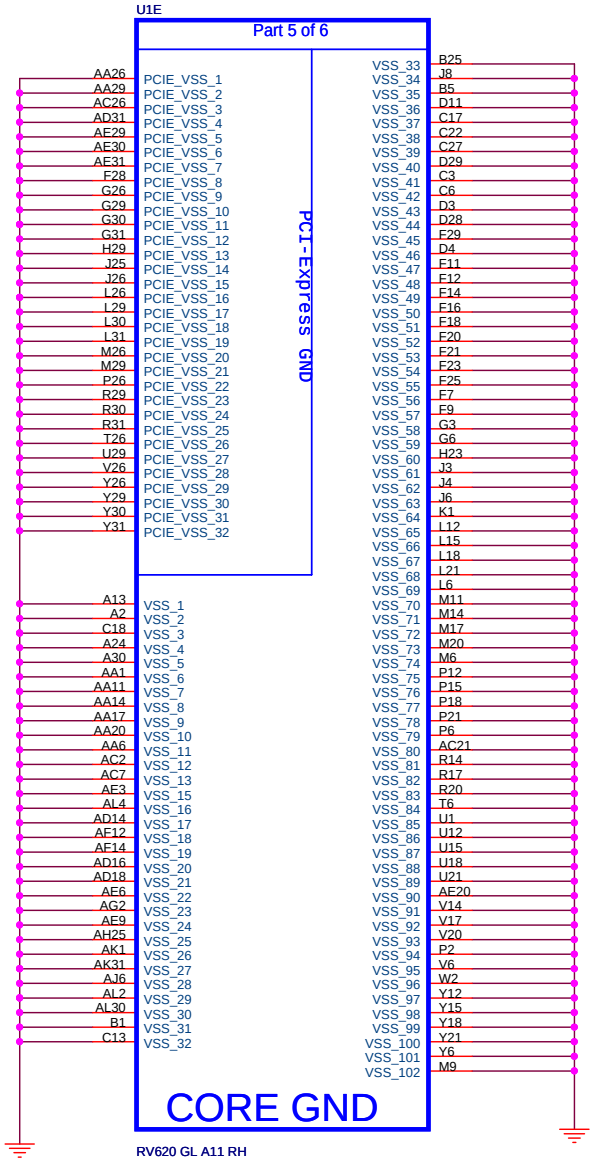
Doc No. 105-B350xx-00B


U1B
PART 2 OF 6
RV610- DO NOT INSTALL R160
RV620- INSTALL R160
PLL Power
MISC/I2C
External TMDS
DAC / CRT
General Purpose I/O
DAC2 (TV/CRT2)
Monitor Interface
Thermal
Test
XTAL
RV620 GL A11 RH
I2C DEVICE ADDRESS' ON DDC3
Possible alternate 5150005600G
NEW CHINGIS SERIAL FLASH
PM25LV512A-100SCE
BIOS1
113-XXXXXX-XXX
VIDEO BIOS FIRMWARE
Change to 10ppm/10ppm p/n 50282700006
Place R_RTCLK close to XTAL so the main clock line has shortest stub
CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario
Date: Thursday, October 25, 2007
Rev 1
Sheet 3 of 20
Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dpvi
Doc No. 105-B350xx-00B



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Thursday, October 25, 2007
Rev	1
Sheet	4 of 20
Title	RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No.	105-B350xx-00B

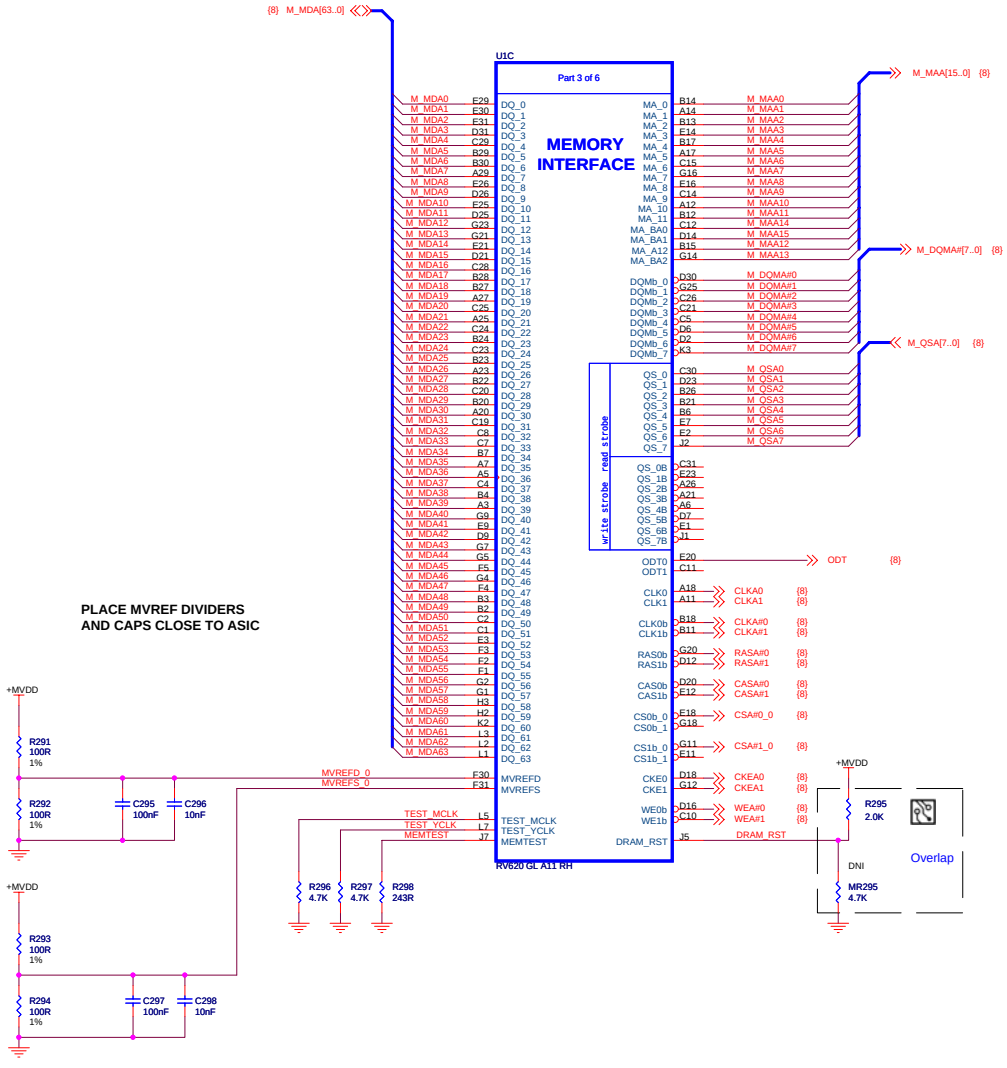


Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, October 25, 2007 Rev 1

Sheet 5 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI Doc No. 105-B350xx-00B



DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

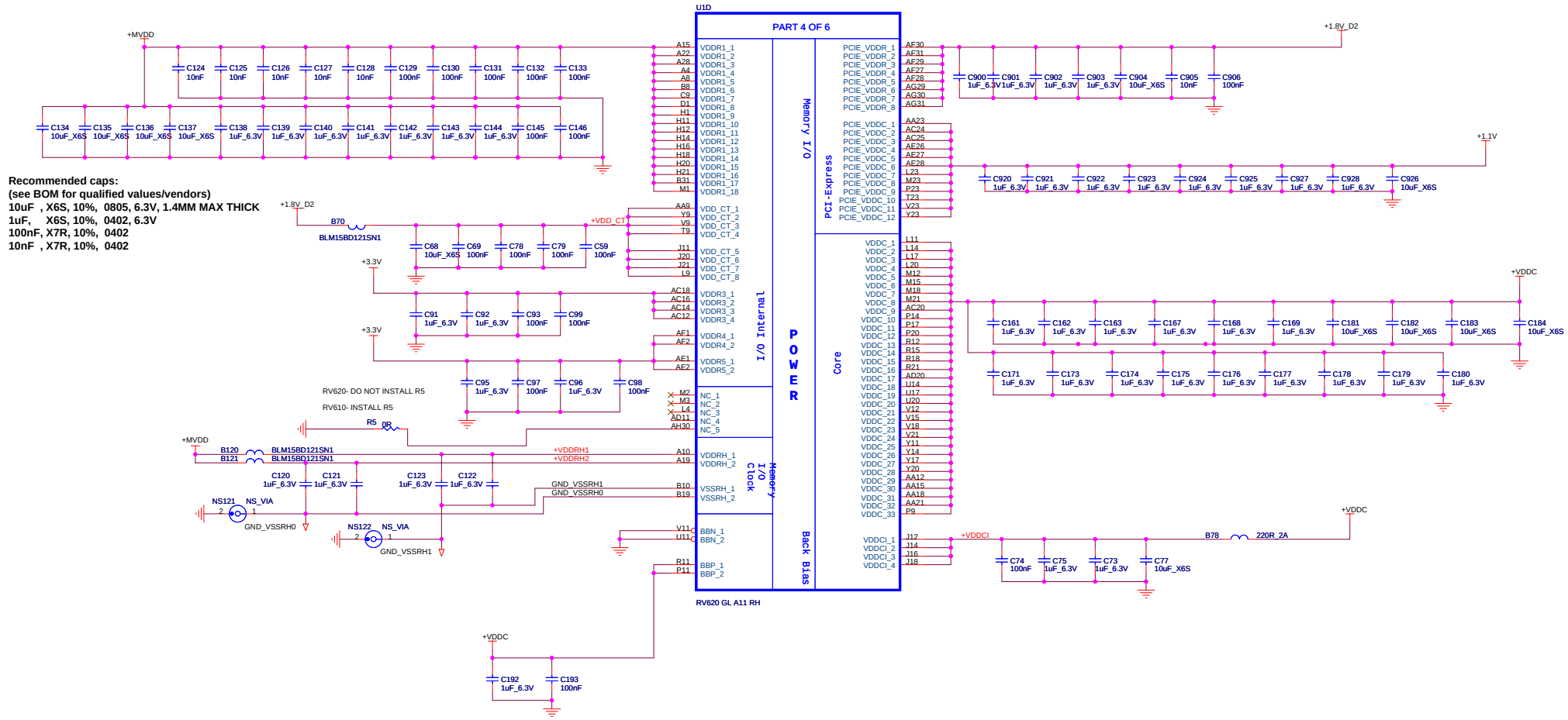
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, October 25, 2007 Rev 1

Sheet 6 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVT

Doc No. 105-B350xx-00B



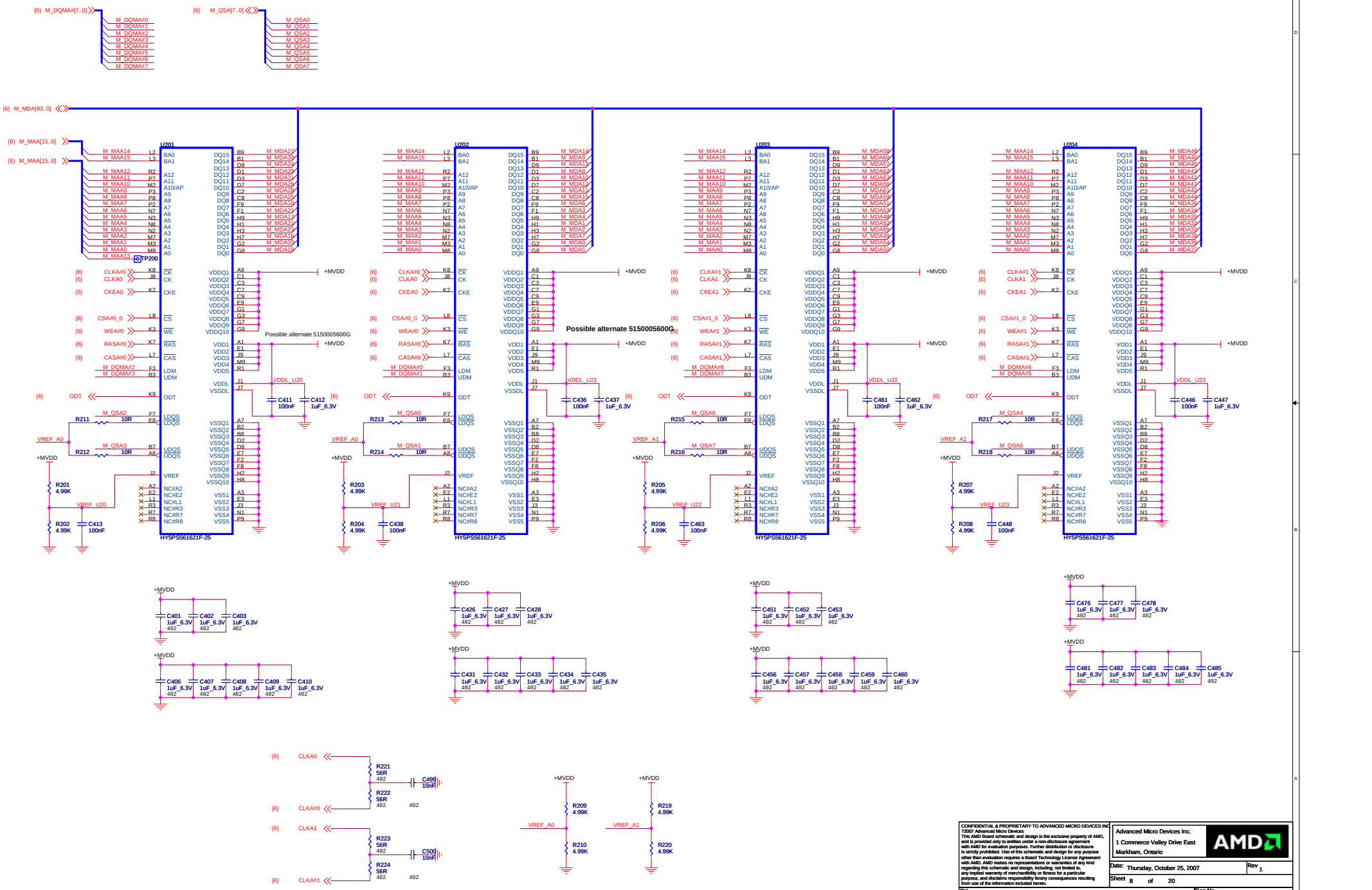
CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.
©2007 Advanced Micro Devices
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology Licence Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantibility or fitness for a particular purpose, and disclaims responsibility forany consequences resulting from use of the information included herein.

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, October 25, 2007
Rev 1
Sheet 7 of 20

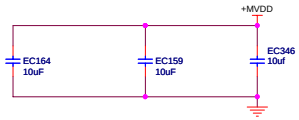
Title: RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No. 105-B350xx-00B

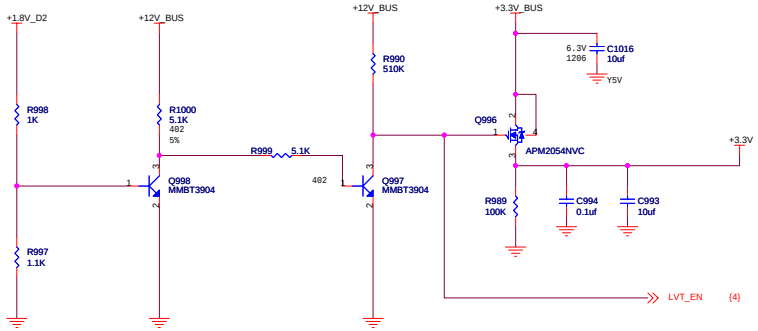
CHANNEL A: RANK 0 128MB DDR2

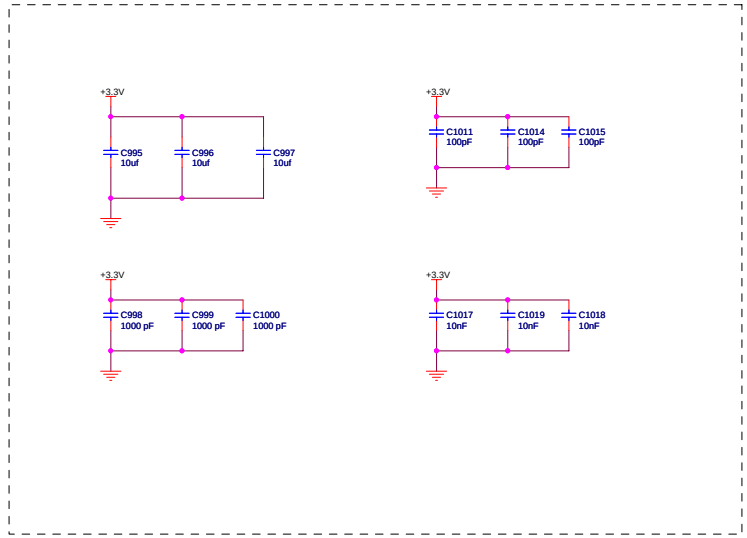


Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Thursday, October 25, 2007
Rev	1
Sheet	8 of 20
Title	RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No.	105-B350xx-00B







Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

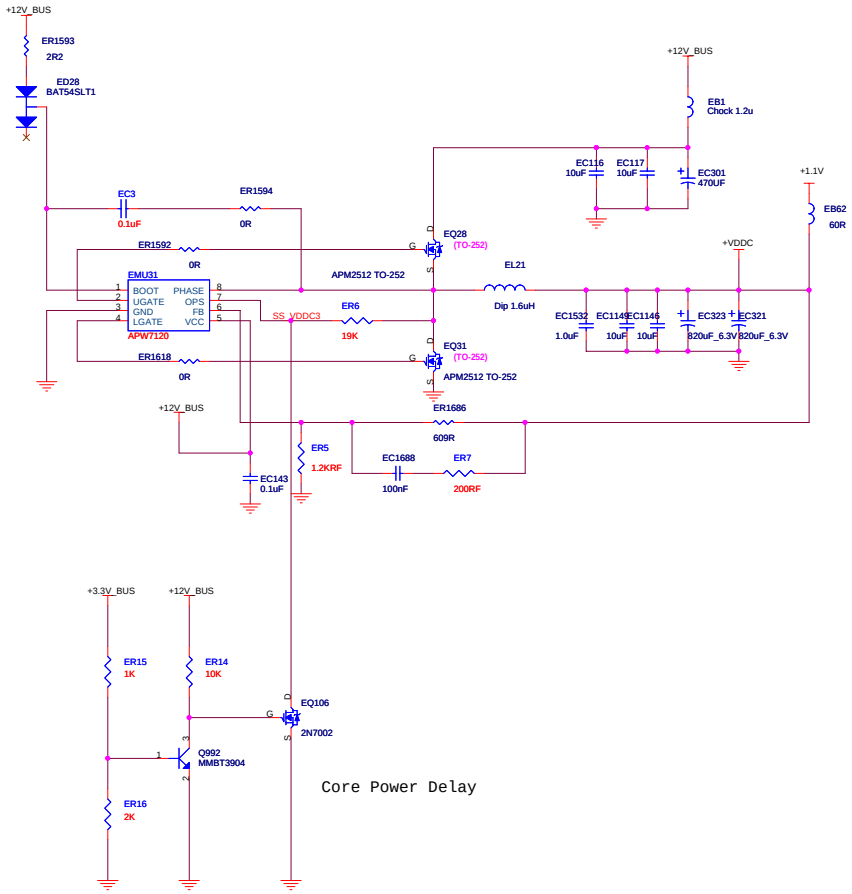
Date: Thursday, October 25, 2007 | Rev 1

Sheet 9 of 20

Title: RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

Doc No. 105-B350xx-00B

CORE REGULATOR +VDDC



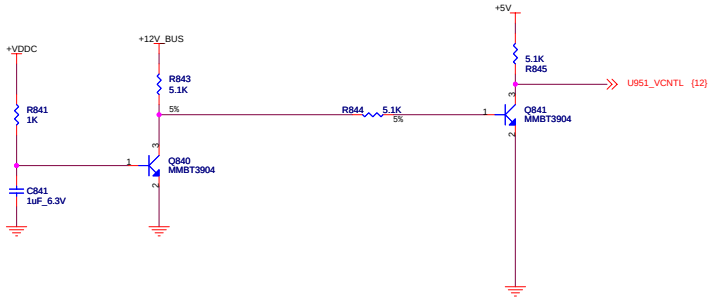
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, October 25, 2007 Rev 1

Sheet 10 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

Doc No. 105-B350xx-00B



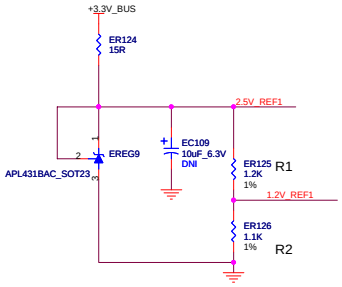
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

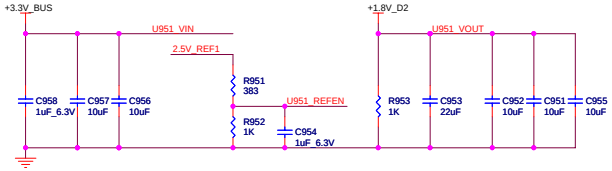
Date: Thursday, October 25, 2007 Rev 1

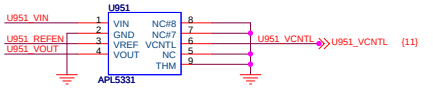
Sheet 11 of 20

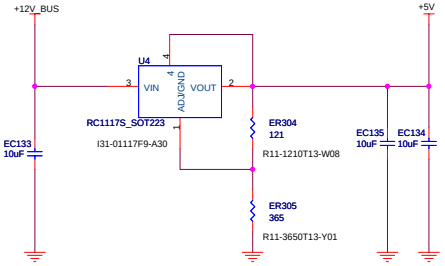
Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

Doc No. 105-B350xx-00B

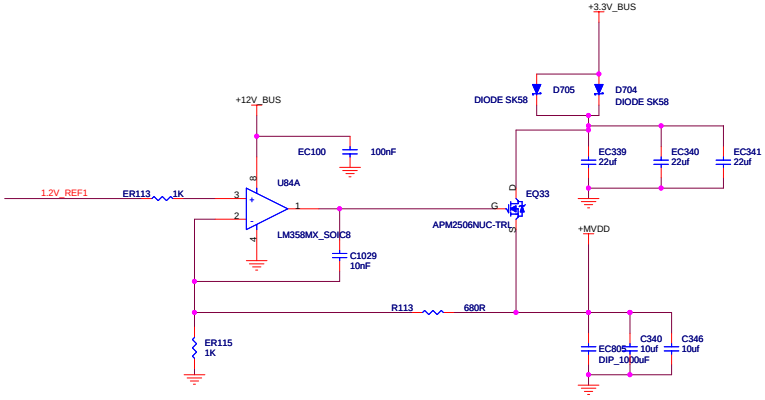




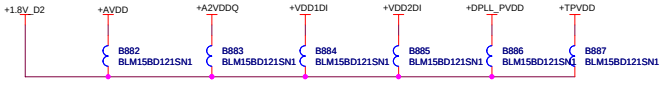


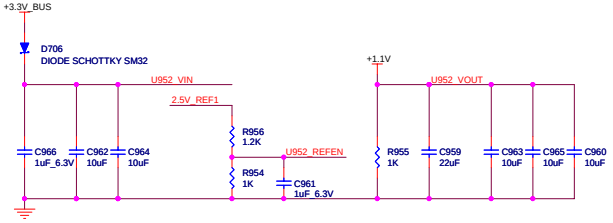


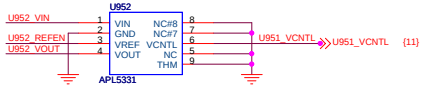
Vout=1.25V* [1+(ER305/ER304)]



Shared Power Rails







Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Thursday, October 25, 2007
Rev	1
Sheet	12 of 20
Title	RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No.	105-B350xx-00B

PIN BASED STRAPS

+3.3V

DNI	MR50	10K	R50	10K	GPIO_0	
DNI	MR51	10K	R51	10K	GPIO_1	
MR52	10K	DNI	R52	10K	GPIO_2	
MR53	10K	DNI	R53	10K	GPIO_3	
MR54	10K	DNI	R54	10K	GPIO_4	
MR55	10K	DNI	R55	10K	GPIO_5	
MR56	10K	DNI	R56	10K	GPIO_6	
MR57	10K	NTSC	R57	10K	GPIO_7	
MR58	10K		R58	10K	GPIO_8	
MR59	10K		R59	10K	GPIO_9	
MR63	10K		R63	10K	GPIO_13	
MR62	10K		R62	10K	GPIO_12	
MR61	10K		R61	10K	GPIO_11	
MR65	10K	DNI	R65	10K	GENERICC	GENERICC {3}
DNI	MR64	10K	DNI	R64	10K	GENERICB	GENERICB {3}
MR66	10K		R66	10K	A_VSYNC_DAC1	A_VSYNC_DAC1 {3,14}
MR67	10K		R67	10K	A_HSYNC_DAC1	A_HSYNC_DAC1 {3,14}
MR68	10K	DNI	R68	10K	PSYNC	
MR69	10K	DNI	R69	10K	GPIO21_BB_EN	GPIO21_BB_EN {3}
MR70	10K	DNI	R70	10K		DPVSS-VID0 {4}
MR71	10K	DNI	R71	10K		VID_1 {4}
MR72	10K	DNI	R72	10K		VID_2 {4}
DNI	MR73	10K		R73	10K		DPAVSS-VID3 {4}
MR74	10K	DNI	R74	10K		DPAVSS-VID4 {4}
MR75	10K	DNI	R75	10K		DPAVSS-VID5 {4}
MR76	10K	DNI	R76	10K		VID_6 {3}
MR77	10K	DNI	R77	10K		VID_7 {3}
DNI	MR80	10K		R80	10K	A_VSYNC_DAC2	A_VSYNC_DAC2 {3,15}
MR79	10K	DNI	R79	10K	A_HSYNC_DAC2	A_HSYNC_DAC2 {3,15}
MR60	10K	DNI	R60	10K	DVALID	
DNI	MR87	10K	DNI	R87	10K		PWRCNTL_0 {3}
DNI	MR46	10K				GPIO_22	GPIO_22 {3}
DNI	MR88	10K		R88	10K		GPIO_18 {3}

RV610: INSTALL MR58
RV620: INSTALL R58

PSYNC {3,4}
DVALID {3}

RV610: (DEFAULT) MR70, R73, MR74, MR75 INSTALLED

RV620: MR70, MR73, MR74, MR75 MUST BE INSTALLED

{3} GPIO_[13..0]

GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - ATI Internal Use Only - Reserved (Default: 00)

GPIO(4) - DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(7) - TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

GPIO(8) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0] IF BIOS_ROM_EN=1 [default] (GPIO_22)
tmel - AT25F512A (512 kbit)0010
AT25F1024A (1 Mbit)0011
ST Microelectronics- M25P05A (512 kbit) 0100
M25P10A (1 Mbit) 0101
M25P20 (2 Mbit) 0101
Chingis (formerly PMC) -
Pm25LV512 (512 kbit) 0100
Pm25LV010 (1 Mbit) 0101

If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. (Config 3 = don care).
x000 128MB
x001 256MB
x010 64MB
x011 32MB
x100 512MB
x101 1GB
x110 2GB
x111 4GB

GENERICC, GENERICB - ATI Internal Use Only - Reserved (Default: 0)

VSYNC - VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - ATI Internal Use Only - Reserved (Default 0)

PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO_21 - ATI Internal Use Only - Reserved (Default: 0)

VID_0 - ATI Internal Use Only - Reserved (Default: 0)

VID_1 - MSI_DIS (Default: 0)

VID_2 - ATI Internal Use Only - Reserved (Default: 0)

VID_3 - ATI Internal Use Only - Reserved (Default: 0)

VID_4 - ATI Internal Use Only - Reserved (Default: 0)

VID_5 - 64BAR_EN_A (Default: 0)
Enable 64-bit BARS

VID_6:7 - ATI Internal Use Only - Reserved (Default: 00)

VSYNC - DDR2 VENDOR SELECT ATI Board Feature I
(see GPIO_18)

HSYNC2 - ATI Internal Use Only - Reserved (Default: 0)

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

GPIO_15 - FOR FUTURE EXPANSION

GPIO_22_ROMCSb - Enable external BIOS ROM device (Default 1)

GPIO_18 - DDR2 MEM VENDOR [V2SYNC:GPIO_18] ATI Board Feature I
QUIMONDA [0:0]
HYNIX [0:1]
SAMSUNG [1:0]

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground High logic voltage

Signal

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, October 25, 2007 Rev 1

Sheet 13 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

Doc No. 105-B350xx-00B

Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)

{3} A_R_DAC1
{3} A_RB_DAC1
{3} A_G_DAC1
{3} A_GB_DAC1
{3} A_B_DAC1
{3} A_BB_DAC1

R1029 37.4R
R1028 37.4R
R1027 37.4R
R1003 75R
R1002 75R
R1001 75R

A_R_DAC1_M
A_G_DAC1_M
L1004 47nH
L1005 47nH
L1006 47nH

C1001 8.0pF 402
C1002 8.0pF 402
C1003 8.0pF 402
C1005 8.0pF 402
C1006 8.0pF 402
C1004 8.0pF 402

DDCDATA_DAC1_R
DDCCLK_DAC1_R
A_HSYNC_DAC1_R
A_VSYNC_DAC1_R

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F

+5V
+5V_VESA
EF1 0.2A

MJ1001
1 R
2 G
3 B
11 MS0
12 MS1
4 MS2
15 MS3
9 NC
13 HS
14 VS
5 VSS
6 VSS#6
7 VSS#7
8 VSS#8
10 VSS#10
16 CASE
17 CASE#17
G3179C219-005
SLIM VGA

C1010 100nF

Place close to Connector
SHOULD BE A LOW INDUCTANCE PATH TO PIN 5

+3.3V
+5V
{3} CRT1DDCDATA
R1004 10K 402
R1005 1.9K 402
BSH111 Q1001
DDCDATA_DAC1_5V
R1006 33R
DDCDATA_DAC1_R

+3.3V
+5V
{3} CRT1DDCCLK
R1007 10K 402
R1008 1.9K 402
BSH111 Q1002
DDCCLK_DAC1_5V
R1009 33R
DDCCLK_DAC1_R

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

C1999 100nF
+5V
{3,13} A_HSYNC_DAC1
U1999A SN74HCT125D
A_HSYNC_DAC1_B
R1010 33R 402
A_HSYNC_DAC1_R

SN74HCT125D U1999B
{3,13} A_VSYNC_DAC1
A_VSYNC_DAC1_B
R1011 33R 402
A_VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

+3.3V
Q1021 MMBT3904
R1022 10K
HPD_DVI1
{3} HPD1
R1023 10K

+5V_VESA
J1001
25 CASE
1 TMDS Data2-
2 TMDS Data2+
3 TMDS Data2/4 Shield
4 TMDS Data4-
5 TMDS Data4+
6 DDC Clock
7 DDC Data
8 Analog VSYNC
9 TMDS Data1-
10 TMDS Data1+
11 TMDS Data1/3 Shield
12 TMDS Data3-
13 TMDS Data3+
14 +5V Power
15 GND (for +5V)
16 Hot Plug Detect
17 TMDS Data0-
18 TMDS Data0+
19 TMDS Data0/5 Shield
20 TMDS Data5-
21 TMDS Data5+
22 TMDS Clock Shield
23 TMDS Clock+
24 TMDS Clock-
C1 Analog Red
C2 Analog Green
C3 Analog Blue
C4 Analog HYNC
C5 Analog GND
C6 Analog GND#C6
26 CASE#26
27 CASE#27
28 CASE#28
29 CASE#29
30 CASE#30
DVI_CONNECTOR

{4} TjX2M
{4} TjX2P
{4} TjX4M
{4} TjX4P
DDCCLK_DAC1_R
DDCDATA_DAC1_R
A_VSYNC_DAC1_R
{4} TjX1M
{4} TjX1P
{4} TjX3M
{4} TjX3P
{4} TjX0M
{4} TjX0P
{4} TjX5M
{4} TjX5P
{4} TjXCP
{4} TjXCM
A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
A_HSYNC_DAC1_R

TMDS_2(Daul_Link) + DAC_1-CRT

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, October 25, 2007
Rev 1
Sheet 14 of 20
Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No. 105-B350xx-00B

2X7 HEADER FOR VGA RIBBON CONNECTOR

Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane

{3} A_R_DAC2
{3} A_RB_DAC2
{3} A_G_DAC2
{3} A_GB_DAC2
{3} A_B_DAC2
{3} A_BB_DAC2

R2029 37.4R
R2028 37.4R
R2027 37.4R
R2003 75R
R2002 75R
R2001 75R
402

A_R_DAC2_M
A_G_DAC2_M
A_B_DAC2_M
L2004 47nH
L2005 47nH
L2006 47nH

OVERLAP

C2001 8.0pF 402
C2002 8.0pF 402
C2003 8.0pF 402
C2004 8.0pF 402
C2005 8.0pF 402
C2006 8.0pF 402

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R

Place close to Connector

+3.3V
+5V
R2004 10K 402
R2005 2.2K 402
{3} CRT2DDCDATA
Q2001 BSH111
DDCDATA_DAC2_5V
R2006 33R 402
DDCDATA_DAC2_R

R2007 10K 402
R2008 2.2K 402
{3} CRT2DDCCLK
Q2002 BSH111
DDCCLK_DAC2_5V
R2009 33R 402
DDCCLK_DAC2_R

+5V_VESA

J1
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R
DDCDATA_DAC2_R
DDCCLK_DAC2_R

{3,13} A_HSYNC_DAC2
A_HSYNC_DAC2_B
R2010 33R 402
A_HSYNC_DAC2_R

U1999C SN74HCT125D
U1999D SN74HCT125D

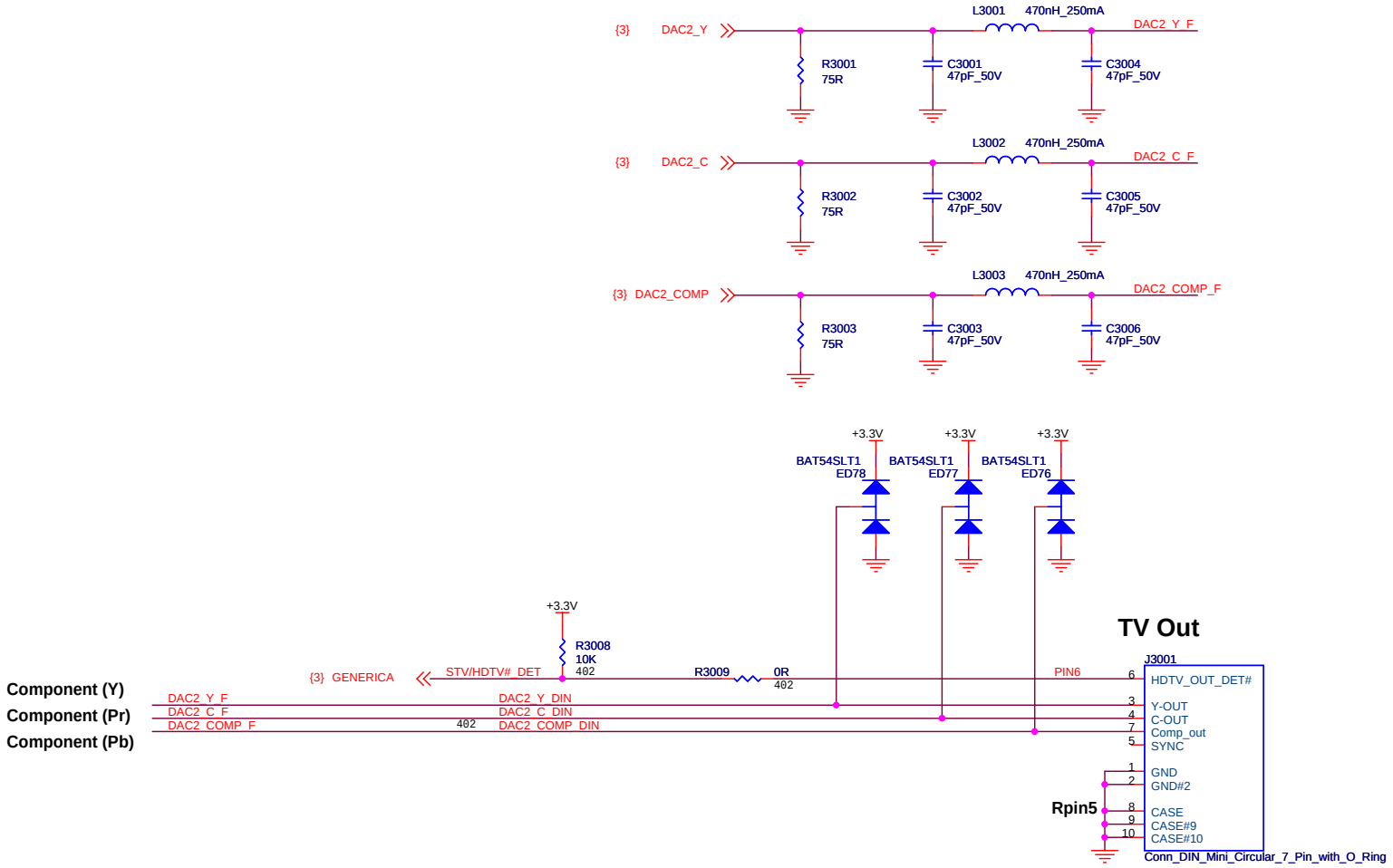
{3,13} A_VSYNC_DAC2
A_VSYNC_DAC2_B
R2011 33R 402
A_VSYNC_DAC2_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

TMDS_1(Single_Link) + DAC_2-CRT

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, October 25, 2007
Rev 1
Sheet 15 of 20
Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No. 105-B350xx-00B



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

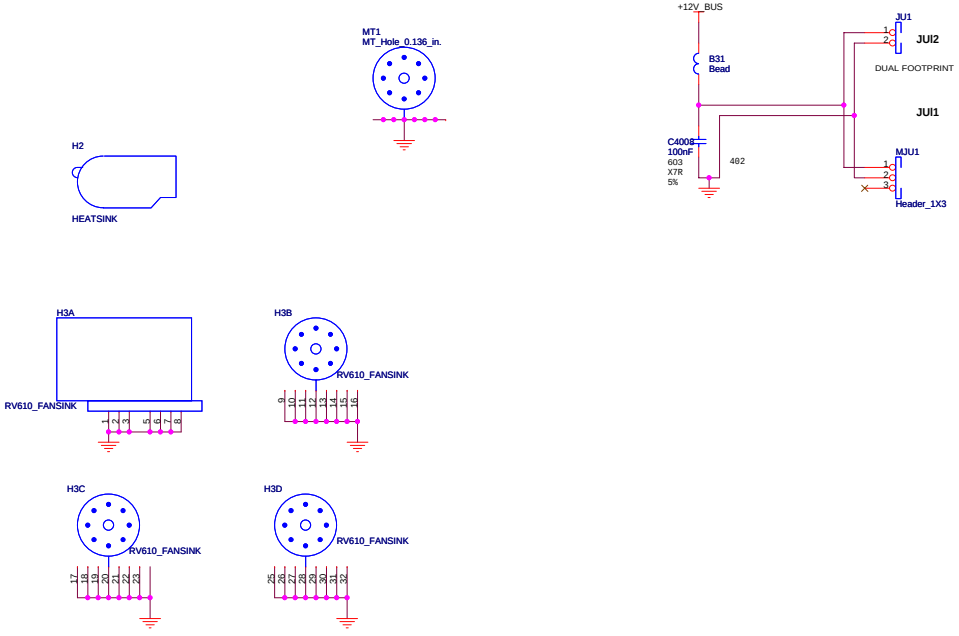
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, October 25, 2007 Rev 1

Sheet 16 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

Doc No. 105-B350xx-00B



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, October 25, 2007	Rev 1
Sheet 17 of 20	
Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI	Doc No. 105-B350xx-00B

ASSY1

BRACKET

8020040100G

ASSY2

BRACKET
LP

8020040400G

SK1

BGA_Socket_RV620

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, October 25, 2007

Rev 1

Sheet 18 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

Doc No. 105-B350xx-00B

<variant Name>

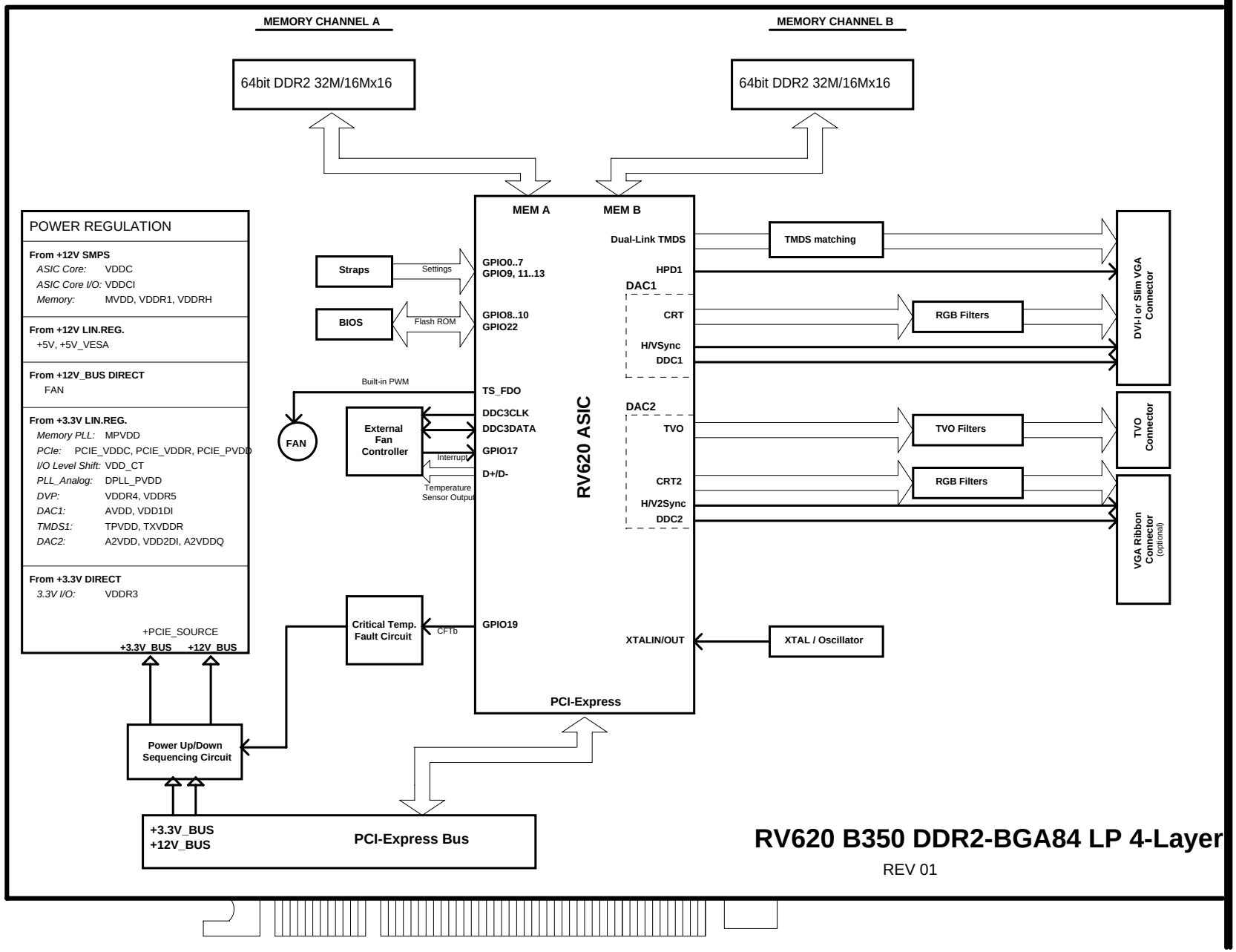
Title	Schematic No.	Date:
RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI	105-B350xx-00B	**Thursday, October 25, 2007**

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
01	00A	2007.05.07	START NEW SCHEMATIC. DERIVED FROM B170 (RV610) SCHEMATIC.
02	00A	2007.05.17	p. 4 MR155/R155 FIX SHORT
03	00A	2007.05.17	RM R7, NR7, R5, MB60, MR45, R45, R890, R1248, R1247, R1242, R1243, C853, C863; ADD R2, B890, MR890, C846; CHANGE R1022, R1023;
04	00A	2007.05.22	REMOVE GND_TXVSSR, GND_PVSS; AG23 NOW NC - WAS SCHEM MISTAKE; ADD R858 FOR BUO; R858 CHANGE TO 1210;
05	00A	2007.05.24	CTF: ADD Q1252, R1254, R1255, R1256, R1258, Q1253, Q1254, CHANGE U1250 TO SINGLE FF; UPDATE BLOCK DIAGRAM.
06	00A	2007.05.25	LVTM: ADD R110, RM R109, MR109, R108, R107;
07	00A	2007.05.28	LVTM: ADD C118, RM C104; REMOVE MR85, MR86 FOR SIMPLIFICATION;
08	00A	2007.05.28	XTALIN/OUT: LAYOUT EASEMENT; REMOVE MR108 (R849 ALREADY THERE); LVTM: ADD C119 (LOWER COST OPTION); POWER SUPPLY: REMOVE R706, MR707, R606 & MR607;
09	00A	2007.05.29	REMOVAL OF +5V: ADD R861, MR861, R862, REG861, R869, R863, R867; REMOVE MU830, U830, C830. R833, R834, C831, R832, MR832, R831, MR831; CONNECT DDC TO 5V_VESA;
010	00A	2007.05.30	CHNG C858 TO 3.3VBUS; CONNECTION TO R845 CHNG; ADD R870, MR870, C867;
011	00A	2007.05.30	REMOVE R4033; REMOVE B201-204; ADD R30-33 [PLACE NEAR ASIC]; REMOVE R3004, R3005;
012	00A	2007.05.31	REMOVE C164-C166, C170, C172 PER SIMULATION RESULTS - THESE CAPS DO NOT IMPROVE DECOUPLING. RM TP860 (LAYOUT CONSTRAINTS. ALREADY ICT TP ON THAT NET);
013	00A	2007.05.31	RM R154-R157, MR154-157 -> FUNCTIONALITY TAKEN BY EXISTING STRAPS. LAYOUT USE PLACE OF M/R154-7; ADD R7; RM MR706, MR606, B889, R863; ADD D861;
014	00A	2007.05.32	ADD SOCKET SK1
015	00A	2007.06.1	SK? CORRECTED TO SK1.
016	00B	2007.06.25	NO NETLIST CHANGES; - MOUNTING HOLES CHANGED TO 3.175mm;



RV620 B350 DDR2-BGA84 LP 4-Layer

REV 01

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Thursday, October 25, 2007
Rev	1
Sheet	20 of 20
Title	RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No.	105-B350xx-00B