PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI

Tall DVI-I + DP + DP + DP/HDMI + DP

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Block Diagram

DP

HDMI/
DP

DP

DP

DVI-I

SLI/

QD:FRAME LOCK

MEM C
LO

MEM C
HI

MEM B
LO

MEM B
HI

MEM A
LO

MEM A
HI

QD:STEREO

QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

Power Supply
NVVDD-PH4

Power Supply
NVVDD-PH3

Power Supply
NVVDD-PH2

Power Supply
NVVDD-PH1

EXT_12V 2x3 PWR 1
(NORTH)

Power Supply
5V Linear

Power Supply
FBVDD/FBVDDQ

PEX_12V Finger

PEX_VDD
LDO

VID_PLL
LDO

PEX_3V3 Finger

Fan

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Block Diagram

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PCI Express

ADD FUSE by diho.su 20150702

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GIGABYTE

Title: PCIE EXPRESS

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MEMORY: GPU Partition A/B

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1B
@digital:u_gpu_gb2b_192(sym_2):page4_i1905
BGA1428
COMMON

2/18 FBA

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1C
@digital:u_gpu_gb2b_192(sym_3):page4_i1906
BGA1428
COMMON

3/18 FBB

GDDR5_BGA170_MIRROR

	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD32		
CMD34	DBG0	DBG0
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*
CMD33		
CMD35	DBG1	DBG1

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MEMORY: GPU Partition A/B

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Title: DDR

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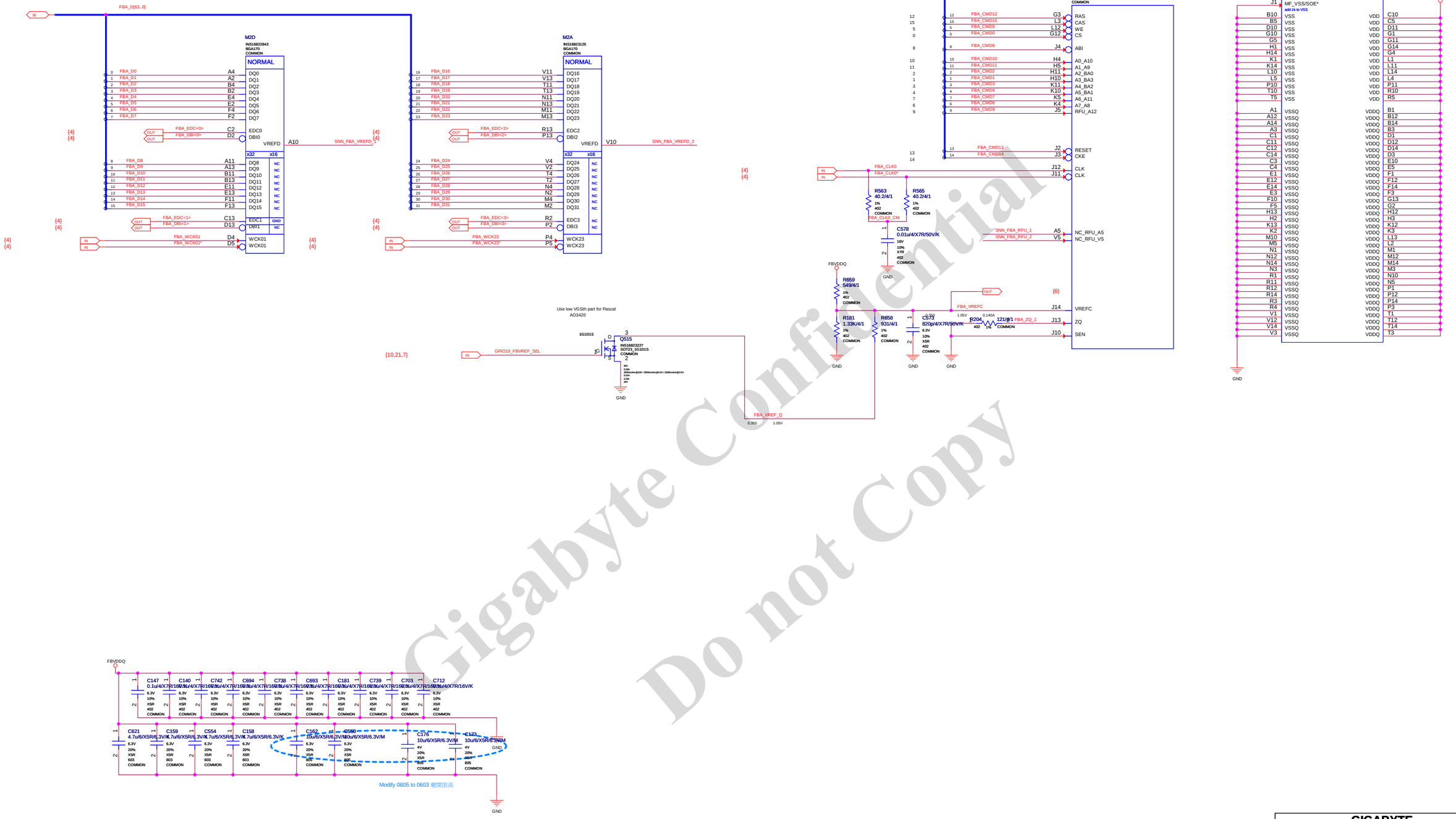
MEMORY: FBA Partition 31..0



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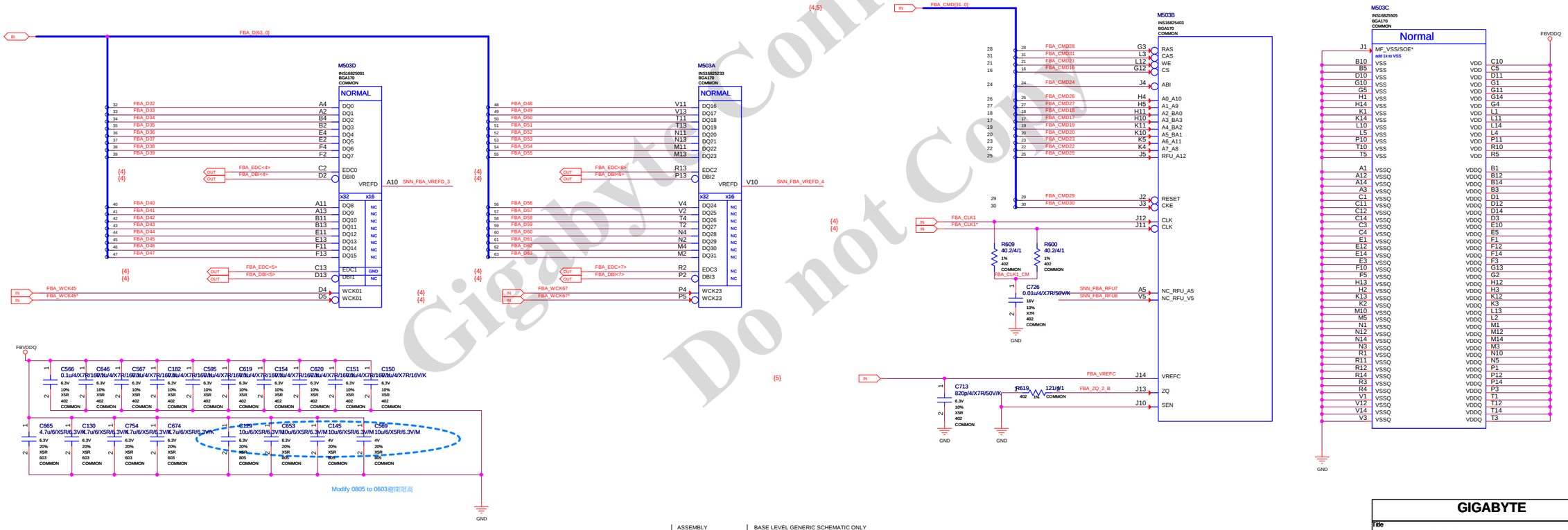
MEMORY: FBA Partition 63..32



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Title: DDR

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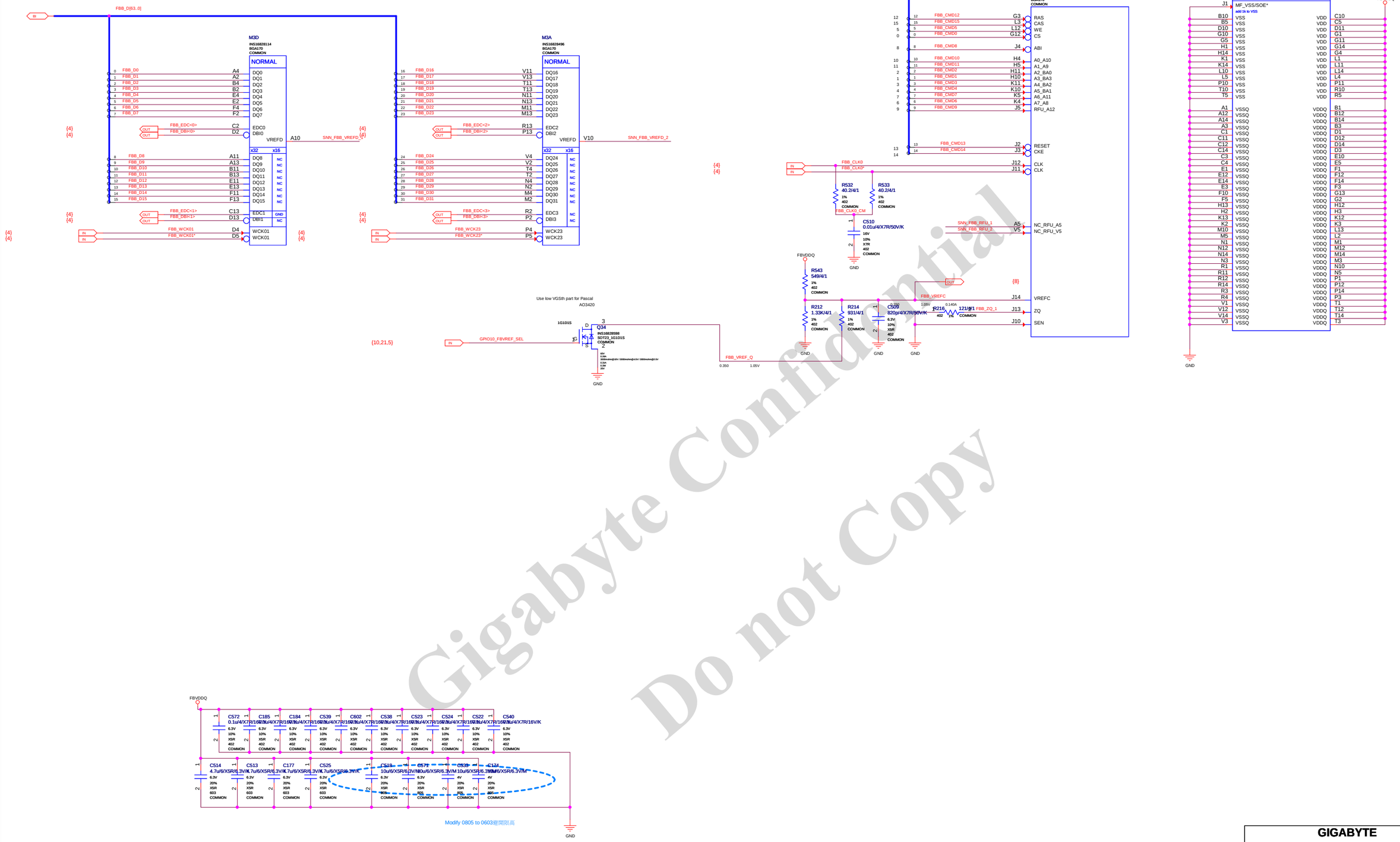
MEMORY: FBB Partition 31..0



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Title: DDR

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MEMORY: GPU Partition C/D

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
C1D
INS16832012
BGA1428
COMMON

4/18 FBC

FB_DATA
FBC_D[63..0]

FB_CMD
FBC_CMD[31..0]

FBC NOT AVAILABLE WITH GM206

0	FBC_D0	AB5	FBC_D0	FBC_CMD0	N6
1	FBC_D1	AB6	FBC_D1	FBC_CMD1	N5
2	FBC_D2	AC7	FBC_D2	FBC_CMD2	N4
3	FBC_D3	AB4	FBC_D3	FBC_CMD3	N7
4	FBC_D4	AA5	FBC_D4	FBC_CMD4	N8
5	FBC_D5	AA4	FBC_D5	FBC_CMD5	M4
6	FBC_D6	W4	FBC_D6	FBC_CMD6	M5
7	FBC_D7	W5	FBC_D7	FBC_CMD7	M6
8	FBC_D8	W1	FBC_D8	FBC_CMD8	L5
9	FBC_D9	Y3	FBC_D9	FBC_CMD9	L7
10	FBC_D10	W2	FBC_D10	FBC_CMD10	M8
11	FBC_D11	W3	FBC_D11	FBC_CMD11	G3
12	FBC_D12	AB1	FBC_D12	FBC_CMD12	F3
13	FBC_D13	AB2	FBC_D13	FBC_CMD13	F1
14	FBC_D14	AC3	FBC_D14	FBC_CMD14	F2
15	FBC_D15	AB3	FBC_D15	FBC_CMD15	G2
16	FBC_D16	V5	FBC_D16	FBC_CMD16	D4
17	FBC_D17	V6	FBC_D17	FBC_CMD17	E4
18	FBC_D18	V4	FBC_D18	FBC_CMD18	F4
19	FBC_D19	T4	FBC_D19	FBC_CMD19	G4
20	FBC_D20	P7	FBC_D20	FBC_CMD20	H4
21	FBC_D21	R5	FBC_D21	FBC_CMD21	D3
22	FBC_D22	R6	FBC_D22	FBC_CMD22	D1
23	FBC_D23	R4	FBC_D23	FBC_CMD23	B3
24	FBC_D24	P3	FBC_D24	FBC_CMD24	C2
25	FBC_D25	R1	FBC_D25	FBC_CMD25	L3
26	FBC_D26	R2	FBC_D26	FBC_CMD26	N3
27	FBC_D27	R3	FBC_D27	FBC_CMD27	M3
28	FBC_D28	U3	FBC_D28	FBC_CMD28	M1
29	FBC_D29	V2	FBC_D29	FBC_CMD29	E3
30	FBC_D30	V3	FBC_D30	FBC_CMD30	D2
31	FBC_D31	V1	FBC_D31	FBC_CMD31	M2
32	FBC_D32	D13	FBC_D32	SNN_FBC_CMD<32>	K8
33	FBC_D33	G14	FBC_D33	SNN_FBC_CMD<33>	K9
34	FBC_D34	E13	FBC_D34	FBC_DEBUG0	K7
35	FBC_D35	F13	FBC_D35	FBC_DEBUG1	L8
36	FBC_D36	D12	FBC_D36		
37	FBC_D37	E12	FBC_D37		
38	FBC_D38	E10	FBC_D38		
39	FBC_D39	D10	FBC_D39		
40	FBC_D40	B10	FBC_D40		
41	FBC_D41	C10	FBC_D41		
42	FBC_D42	A10	FBC_D42		
43	FBC_D43	C11	FBC_D43		
44	FBC_D44	C13	FBC_D44		
45	FBC_D45	A13	FBC_D45		
46	FBC_D46	D14	FBC_D46		
47	FBC_D47	B13	FBC_D47		
48	FBC_D48	D9	FBC_D48		
49	FBC_D49	D7	FBC_D49		
50	FBC_D50	G8	FBC_D50		
51	FBC_D51	E7	FBC_D51		
52	FBC_D52	G5	FBC_D52		
53	FBC_D53	F6	FBC_D53		
54	FBC_D54	E6	FBC_D54		
55	FBC_D55	D6	FBC_D55		
56	FBC_D56	C5	FBC_D56		
57	FBC_D57	B6	FBC_D57		
58	FBC_D58	C6	FBC_D58		
59	FBC_D59	A6	FBC_D59		
60	FBC_D60	C8	FBC_D60		
61	FBC_D61	C9	FBC_D61		
62	FBC_D62	A9	FBC_D62		
63	FBC_D63	B9	FBC_D63		

FBC_DBI<0>	AA6	FBC_DQM0	
FBC_DBI<1>	AA1	FBC_DQM1	
FBC_DBI<2>	U7	FBC_DQM2	
FBC_DBI<3>	T1	FBC_DQM3	
FBC_DBI<4>	F12	FBC_DQM4	
FBC_DBI<5>	A12	FBC_DQM5	
FBC_DBI<6>	H6	FBC_DQM6	
FBC_DBI<7>	A7	FBC_DQM7	
FBC_EDC<0>	AB8	FBC_DQS_WP0	
FBC_EDC<1>	AA2	FBC_DQS_WP1	
FBC_EDC<2>	T5	FBC_DQS_WP2	
FBC_EDC<3>	T2	FBC_DQS_WP3	
FBC_EDC<4>	H13	FBC_DQS_WP4	
FBC_EDC<5>	B12	FBC_DQS_WP5	
FBC_EDC<6>	G7	FBC_DQS_WP6	
FBC_EDC<7>	B7	FBC_DQS_WP7	
SNN_FBC_DQS_RN<0>	AA7	FBC_DQS_RN0	
SNN_FBC_DQS_RN<1>	AA3	FBC_DQS_RN1	
SNN_FBC_DQS_RN<2>	T6	FBC_DQS_RN2	
SNN_FBC_DQS_RN<3>	T3	FBC_DQS_RN3	
SNN_FBC_DQS_RN<4>	G12	FBC_DQS_RN4	
SNN_FBC_DQS_RN<5>	C12	FBC_DQS_RN5	
SNN_FBC_DQS_RN<6>	F7	FBC_DQS_RN6	
SNN_FBC_DQS_RN<7>	C7	FBC_DQS_RN7	

FBC_CLK0	N2	FBC_CLK0	
FBC_CLK0	N1	FBC_CLK0*	
FBC_CLK1	A4	FBC_CLK1	
FBC_CLK1	B4	FBC_CLK1*	
FBC_WCK01	V7	FBC_WCK01	
FBC_WCK01	U8	FBC_WCK01*	
FBC_WCKB01	Y8	SNN_FBC_WCKB01	
FBC_WCKB01	W7	SNN_FBC_WCKB01*	
FBC_WCK23	Y7	FBC_WCK23	
FBC_WCK23	W6	FBC_WCK23*	
FBC_WCKB23	R8	SNN_FBC_WCKB23	
FBC_WCKB23	T7	SNN_FBC_WCKB23*	
FBC_WCK45	E9	FBC_WCK45	
FBC_WCK45	F9	FBC_WCK45*	
FBC_WCKB45	H8	SNN_FBC_WCKB45	
FBC_WCKB45	H9	SNN_FBC_WCKB45*	
FBC_WCK67	G11	FBC_WCK67	
FBC_WCK67	F10	FBC_WCK67*	
FBC_WCKB67	H11	SNN_FBC_WCKB67	
FBC_WCKB67	G10	SNN_FBC_WCKB67*	

FBC_PLL_AVDD P8 — FB_PLLVDD — {15,4}

C612 0.1uF/X 16V 10% X7R 402 COMMON

R568 60.4ohm/X 402 1% DNI
R570 60.4ohm/X 402 1% DNI

R546 10k/X 5% 402 COMMON
R573 10k/X 5% 402 COMMON
R569 10k/X 5% 402 COMMON
R547 10k/X 5% 402 COMMON

CKE* — FBC_CMD30 / FBC_CMD14
RST* — FBC_CMD29 / FBC_CMD13

GDDR5_BGA170_MIRROR

	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD32		
CMD34	DBG0	DBG0
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*
CMD33		
CMD35	DBG1	DBG1

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MEMORY: GPU Partition C

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GIGABYTE			
Title: DDR			
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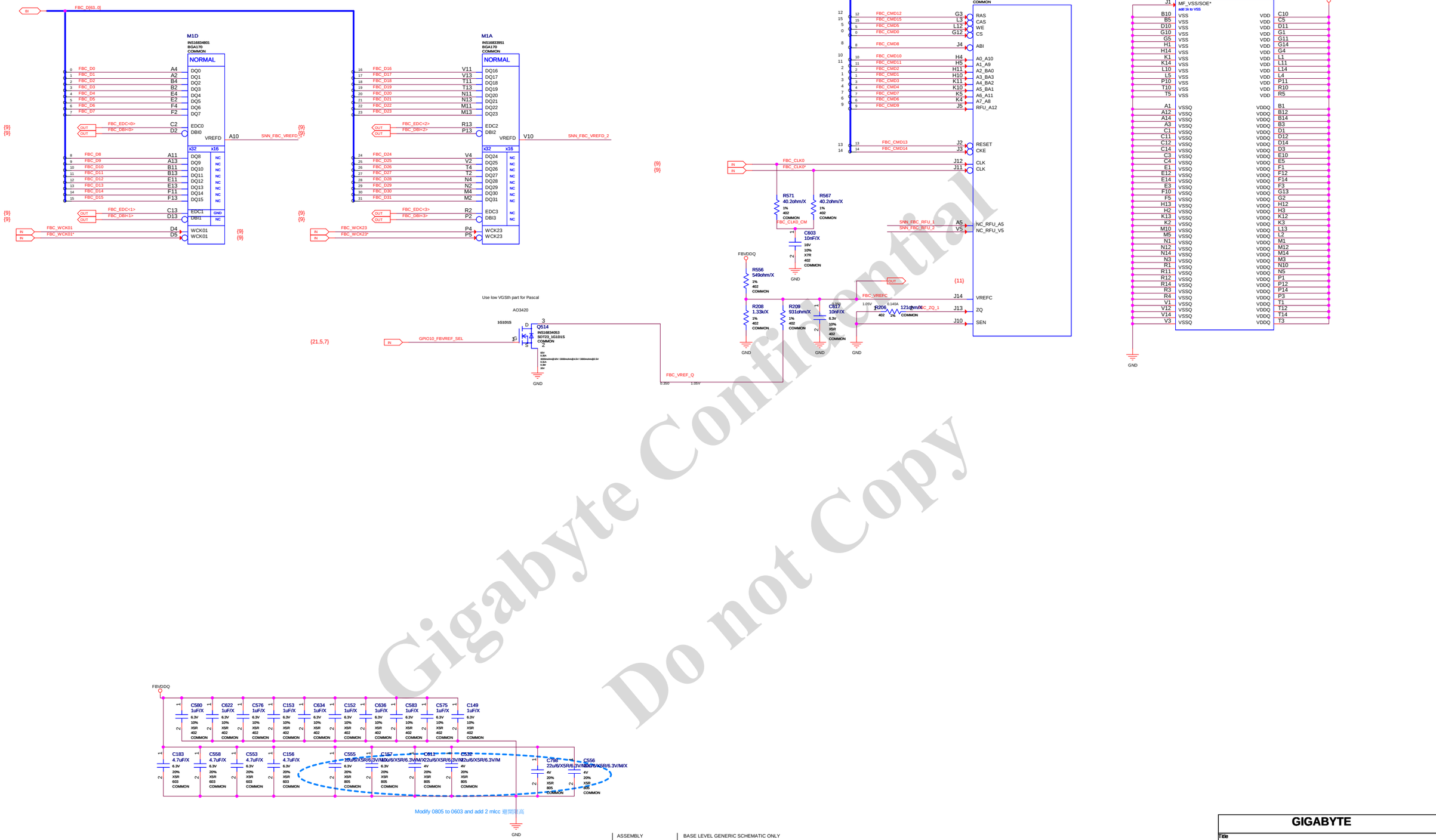
MEMORY: FBC Partition 31..0



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BASE LEVEL GENERIC SCHEMATIC ONLY
MEMORY: FBC[31:0]

GIGABYTE

Title: DDR

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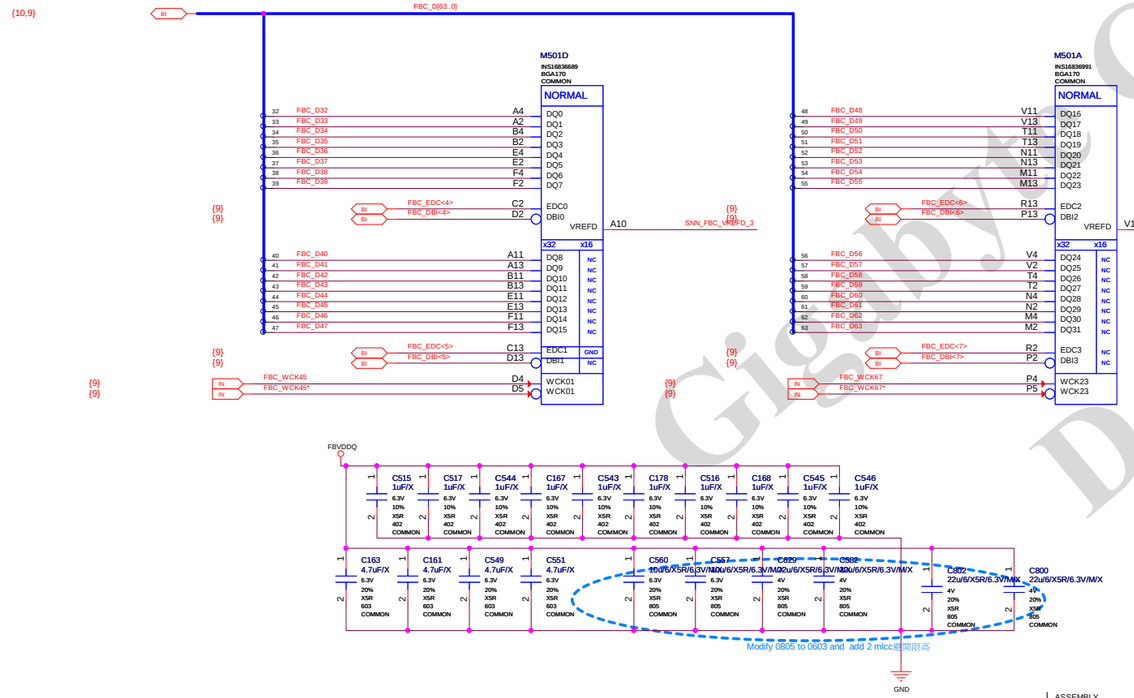
MEMORY: FBC Partition 63..32



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PAGE DETAIL	MEMORY: FBC[63:32]

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GIGABYTE

Title	DDR	
Size: Custom	Document Number: GV-N950XTREME-2GD	Rev: 1.0
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GPU PWR and GND

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1E
@digital:u_gpu_gb2b_192(sym_14):page12_i76
BGA1428
COMMON
14/18 GND

BA1	GND	GND	M17
BA11	GND	GND	M19
BA14	GND	GND	M21
BA17	GND	GND	M23
BA2	GND	GND	M25
BA20	GND	GND	M27
BA23	GND	GND	M35
BA26	GND	GND	N12
BA29	GND	GND	N14
BA32	GND	GND	N16
BA35	GND	GND	N18
BA5	GND	GND	N20
BA8	GND	GND	N22
BB2	GND	GND	N24
BB3	GND	GND	N26
C42	GND	GND	N28
D11	GND	GND	P11
D17	GND	GND	P13
D20	GND	GND	P15
D33	GND	GND	P17
D35	GND	GND	P19
D5	GND	GND	P2
D8	GND	GND	U26
E11	GND	GND	U28
E14	GND	GND	U38
E17	GND	GND	U4
E20	GND	GND	U41
E23	GND	GND	U5
E35	GND	GND	V11
E38	GND	GND	V13
E41	GND	GND	V15
E5	GND	GND	V17
E8	GND	GND	V19
F36	GND	GND	V21
F39	GND	GND	V23
G13	GND	GND	V25
G22	GND	GND	V27
G33	GND	GND	V8
G38	GND	GND	W12
G6	GND	GND	W14
G9	GND	GND	W16
H12	GND	GND	W18
H16	GND	GND	W20
H18	GND	GND	W22
H21	GND	GND	W24
H32	GND	GND	W26
H34	GND	GND	W28
H39	GND	GND	W8
H41	GND	GND	Y11
H7	GND	GND	Y13
K35	GND	GND	Y15
K37	GND	GND	Y17
L12	GND	GND	Y19
L14	GND	GND	Y2
L16	GND	GND	Y21
L18	GND	GND	Y23
L20	GND	GND	Y25
L22	GND	GND	Y27
L24	GND	GND	Y4
L26	GND	GND	Y5
L28	GND	GND	P25
L38	GND	GND	P27
L39	GND	GND	AL9
L41	GND	GND	AK9
M11	GND		
M13	GND		
M15	GND		

GND GND

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1F
@digital:u_gpu_gb2b_192(sym_15):page12_i77
BGA1428
COMMON
15/18 GND

A41	GND	GND	AW24
AA12	GND	GND	AW25
AA14	GND	GND	AW27
AA16	GND	GND	AW28
AA18	GND	GND	AW30
AA20	GND	GND	AW31
AA22	GND	GND	AW33
AA24	GND	GND	AW34
AA26	GND	GND	AY1
AA28	GND	GND	AY20
AA8	GND	GND	AY23
AB11	GND	GND	AY26
AB13	GND	GND	AY29
AB15	GND	GND	AY32
AB17	GND	GND	AY35
AB19	GND	GND	B11
AB21	GND	GND	B14
AB23	GND	GND	B17
AB25	GND	GND	B20
AB27	GND	GND	B23
AB7	GND	GND	B32
AC12	GND	GND	B35
AC14	GND	GND	B38
AC16	GND	GND	B41
AC18	GND	GND	B42
AC2	GND	GND	B5
AC20	GND	GND	B8
AC22	GND	GND	A40
AC24	GND	GND	AM41
AC26	GND	GND	AM5
AC28	GND	GND	AM7
AC4	GND	GND	AR2
AC5	GND	GND	AR39
AD11	GND	GND	AR41
AD13	GND	GND	AR5
AD15	GND	GND	AR7
AD17	GND	GND	AT11
AD19	GND	GND	AT14
AD21	GND	GND	AT17
AD23	GND	GND	AT20
AD25	GND	GND	AT23
AD27	GND	GND	AT26
AE12	GND	GND	AT29
AE14	GND	GND	AT32
AE16	GND	GND	AV11
AE18	GND	GND	AV14
AE20	GND	GND	AV17
AE22	GND	GND	AV2
AE24	GND	GND	AV35
AE26	GND	GND	AV5
AE28	GND	GND	AV8
AF11	GND	GND	AW19
AF13	GND	GND	AW21
AF15	GND	GND	AW22
AF17	GND	GND	P38
AF19	GND	GND	P39
AF2	GND	GND	P41
AF21	GND	GND	P5
AF23	GND	GND	R12
AF25	GND	GND	R14
AF27	GND	GND	R16
AF35	GND	GND	R18
AF41	GND	GND	R20
AF5	GND	GND	R22
AF7	GND	GND	R24
AG12	GND	GND	R26
AG14	GND	GND	R28
AG16	GND	GND	R35
AG18	GND	GND	R7
AG20	GND	GND	T11
AG22	GND	GND	T13
AG24	GND	GND	T15
AG26	GND	GND	T17
AG36	GND	GND	T19
AH11	GND	GND	T21
AH13	GND	GND	T23
AH15	GND	GND	T25
AH17	GND	GND	T27
AH19	GND	GND	T36
AH21	GND	GND	T8
AH23	GND	GND	U12
AH25	GND	GND	U14
AH35	GND	GND	U16
AJ2	GND	GND	U18
AJ38	GND	GND	U2
AJ39	GND	GND	U20
AJ41	GND	GND	U22
AJ5	GND	GND	U24
AJ7	GND	GND	P21
AK35	GND	GND	P23
AL35	GND		
AM2	GND		
AM38	GND		
AM39	GND		

GND GND

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1G
@digital:u_gpu_gb2b_192(sym_16):page12_i78
BGA1428
COMMON
16/18 VDD

NVVDD NVVDD NVVDD NVVDD

AA11	VDD	VDD	AN34
AA13	VDD	VDD	AN35
AA15	VDD	VDD	AP31
AA17	VDD	VDD	AP32
AA19	VDD	VDD	AP33
AA21	VDD	VDD	AP34
AA23	VDD	VDD	AP35
AA25	VDD	VDD	AP36
AA27	VDD	VDD	AR32
AB12	VDD	VDD	AR33
AB14	VDD	VDD	AR34
AB16	VDD	VDD	AR35
AB18	VDD	VDD	AR36
AB20	VDD	VDD	AR37
AB22	VDD	VDD	AT33
AB24	VDD	VDD	AT34
AB26	VDD	VDD	AT35
AB28	VDD	VDD	AT36
AC11	VDD	VDD	AT37
AC13	VDD	VDD	AT38
AC15	VDD	VDD	AT39
AC17	VDD	VDD	AU35
AC19	VDD	VDD	AU36
AC21	VDD	VDD	AU37
AC23	VDD	VDD	AU38
AC25	VDD	VDD	AU39
AC27	VDD	VDD	AU40
AD12	VDD	VDD	AU41
AD14	VDD	VDD	AU42
AD16	VDD	VDD	AV36
AD18	VDD	VDD	AV37
AD20	VDD	VDD	AV38
AD22	VDD	VDD	AV39
AD24	VDD	VDD	AV40
AD26	VDD	VDD	AV41
AD28	VDD	VDD	AW36
AE11	VDD	VDD	AW37
AE13	VDD	VDD	AW38
AE15	VDD	VDD	AW39
AE17	VDD	VDD	AW40
AE19	VDD	VDD	AW41
AE21	VDD	VDD	AW42
AE23	VDD	VDD	AY36
AE25	VDD	VDD	AY37
AE27	VDD	VDD	AY38
AF12	VDD	VDD	AY39
AF14	VDD	VDD	AY40
AF16	VDD	VDD	AY41
AF18	VDD	VDD	AY42
AF20	VDD	VDD	BA37
AF22	VDD	VDD	BA38
AF24	VDD	VDD	BA39
AF26	VDD	VDD	BA40
AF28	VDD	VDD	BA41
AG11	VDD	VDD	BA42
AG13	VDD	VDD	BB37
AG15	VDD	VDD	BB39
AG17	VDD	VDD	BB40
AG19	VDD	VDD	BB41
AG21	VDD	VDD	L11
AG23	VDD	VDD	L13
AG25	VDD	VDD	L15
AG27	VDD	VDD	L17
AG28	VDD	VDD	L19
AH12	VDD	VDD	L21
AH14	VDD	VDD	L23
AH16	VDD	VDD	L25
AH18	VDD	VDD	L27
AH20	VDD	VDD	M12
AH22	VDD	VDD	R19
AH24	VDD	VDD	R21
AH26	VDD	VDD	R23
AH27	VDD	VDD	R25
AH28	VDD	VDD	R27
AM34	VDD	VDD	T12
M14	VDD	VDD	T14
M16	VDD	VDD	T16
M18	VDD	VDD	T18
M20	VDD	VDD	T20
M22	VDD	VDD	T22
M24	VDD	VDD	T24
M26	VDD	VDD	T26
M28	VDD	VDD	T28
N11	VDD	VDD	U11
N13	VDD	VDD	U13
N15	VDD	VDD	U15
N17	VDD	VDD	U17
N19	VDD	VDD	U19
N21	VDD	VDD	U21
N23	VDD	VDD	U23
N25	VDD	VDD	U25
N27	VDD	VDD	U27
P12	VDD	VDD	V12
P14	VDD	VDD	V14
P16	VDD	VDD	V16
P18	VDD	VDD	V18
P20	VDD	VDD	V20
P22	VDD	VDD	V22
P24	VDD	VDD	V24
P26	VDD	VDD	V26
P28	VDD	VDD	V28
R11	VDD	VDD	W11
R13	VDD	VDD	W13
R15	VDD	VDD	W15
R17	VDD	VDD	W17
Y20	VDD	VDD	W19
Y22	VDD	VDD	W21
Y24	VDD	VDD	W23
Y26	VDD	VDD	W25
Y28	VDD	VDD	W27
		VDD	Y12
		VDD	Y14
		VDD	Y16
		VDD	Y18

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1H
@digital:u_gpu_gb2b_192(sym_17):page12_i79
BGA1428
COMMON
17/18 FBVDDQ

FBVDDQ FBVDDQ FBVDDQ

A2	FBVDDQ	FBVDDQ	B27
A27	FBVDDQ	FBVDDQ	B28
A28	FBVDDQ	FBVDDQ	C1
A3	FBVDDQ	FBVDDQ	C27
AA34	FBVDDQ	FBVDDQ	C28
AA35	FBVDDQ	FBVDDQ	C4
AA36	FBVDDQ	FBVDDQ	D23
AA37	FBVDDQ	FBVDDQ	D27
AA38	FBVDDQ	FBVDDQ	D28
AA39	FBVDDQ	FBVDDQ	E27
AA40	FBVDDQ	FBVDDQ	E28
AA41	FBVDDQ	FBVDDQ	E32
AA42	FBVDDQ	FBVDDQ	F27
AA9	FBVDDQ	FBVDDQ	F28
AB34	FBVDDQ	FBVDDQ	G1
AB35	FBVDDQ	FBVDDQ	G27
AB36	FBVDDQ	FBVDDQ	G28
AB37	FBVDDQ	FBVDDQ	H2
AB38	FBVDDQ	FBVDDQ	H27
AB39	FBVDDQ	FBVDDQ	H28
AB40	FBVDDQ	FBVDDQ	H5
AB41	FBVDDQ	FBVDDQ	J1
AB42	FBVDDQ	FBVDDQ	J10
AB9	FBVDDQ	FBVDDQ	J11
AC34	FBVDDQ	FBVDDQ	J12
AC8	FBVDDQ	FBVDDQ	J13
AC9	FBVDDQ	FBVDDQ	J14
AD34	FBVDDQ	FBVDDQ	J15
AE39	FBVDDQ	FBVDDQ	J16
B1	FBVDDQ	FBVDDQ	J17
B2	FBVDDQ	FBVDDQ	J18
P34	FBVDDQ	FBVDDQ	J19
P4	FBVDDQ	FBVDDQ	J2
P9	FBVDDQ	FBVDDQ	J20
R34	FBVDDQ	FBVDDQ	J21
R9	FBVDDQ	FBVDDQ	J22
T34	FBVDDQ	FBVDDQ	J23
T9	FBVDDQ	FBVDDQ	J24
U34	FBVDDQ	FBVDDQ	J25
U39	FBVDDQ	FBVDDQ	J26
U9	FBVDDQ	FBVDDQ	J27
V34	FBVDDQ	FBVDDQ	J28
V9	FBVDDQ	FBVDDQ	J29
W34	FBVDDQ	FBVDDQ	J3
W9	FBVDDQ	FBVDDQ	J30
Y34	FBVDDQ	FBVDDQ	J31
Y9	FBVDDQ	FBVDDQ	J32
		FBVDDQ	J33
		FBVDDQ	J34
		FBVDDQ	J4
		FBVDDQ	J5
		FBVDDQ	J6
		FBVDDQ	J7
		FBVDDQ	J8
		FBVDDQ	J9
		FBVDDQ	K1
		FBVDDQ	K2
		FBVDDQ	K3
		FBVDDQ	K34
		FBVDDQ	K4
		FBVDDQ	K5
		FBVDDQ	K6
		FBVDDQ	L34
		FBVDDQ	L9
		FBVDDQ	M34
		FBVDDQ	M9
		FBVDDQ	N34
		FBVDDQ	N9

AC39	GND_OPT		
AC41	GND_OPT		
AD36	GND_OPT		
B26	GND_OPT		
B29	GND_OPT		
C3	GND_OPT		
D26	GND_OPT		
D29	GND_OPT		
E2	GND_OPT		
G25	GND_OPT		
G30	GND_OPT		
H3	GND_OPT		
L2	GND_OPT		
L4	GND_OPT		
M7	GND_OPT		
W36	GND_OPT		
Y39	GND_OPT		
Y41	GND_OPT		

GND

FBVDDQ_SENSE AR31 16MIL FBVDDQ_SENSE_GPU OUT {24}
FB_GND_PROBE AR30
FB_CLAMP AJ34
FB_VREF H33 SNN_FB_VREF_PROBE
FB_CAL_PD_VDDQ U35 FB_CAL_PD_VDDQ R576 402 40.2Ω/1 1% COMMON
FB_CAL_PU_GND N35 FB_CAL_PU_GND R574 402 40.2Ω/1 1% COMMON
FB_CALTERM_GND Y35 FB_CAL_TERM_GND R578 402 60.4Ω/1 1% COMMON
FBVDDQ
GND

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1I
@digital:u_gpu_gb2b_192(sym_18):page12_i89
BGA1428
COMMON
18/18 NC/3V3

IOVDD

SNN_NC_1	AK34	NC		
SNN_NC_2	AM9	NC		
SNN_NC_3	AN9	NC		
SNN_NC_4	AT31	NC		
SNN_NC_5	AW15	NC	VDD33	AD6
SNN_NC_6	F5	NC	VDD33	AD7
SNN_NC_7	AT30	NC	VDD33	AD8
SNN_NC_8	F8	NC	VDD33	AE6
SNN_NC_9	AP14	NC	VDD33	AE7
SNN_NC_10	AP15	NC	VDD33	AE8
SNN_NC_11	AP16	NC	VDD33	AF8
SNN_NC_12	AT24	NC	VDD33	AF9
SNN_NC_13	AT27	NC	VDD33	AG8
SNN_NC_14	G39	NC	VDD33	AG9
SNN_NC_15	G40	NC	VDD33	AH9
SNN_NC_16	H10	NC		
SNN_NC_17	H14	NC		
		3V3AUX_NC	AH8	SNN_3V3AUX_NC
		3V3_AON	AJ8	IOVDD
		3V3_AON	AJ9	

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GPU PWR and GND

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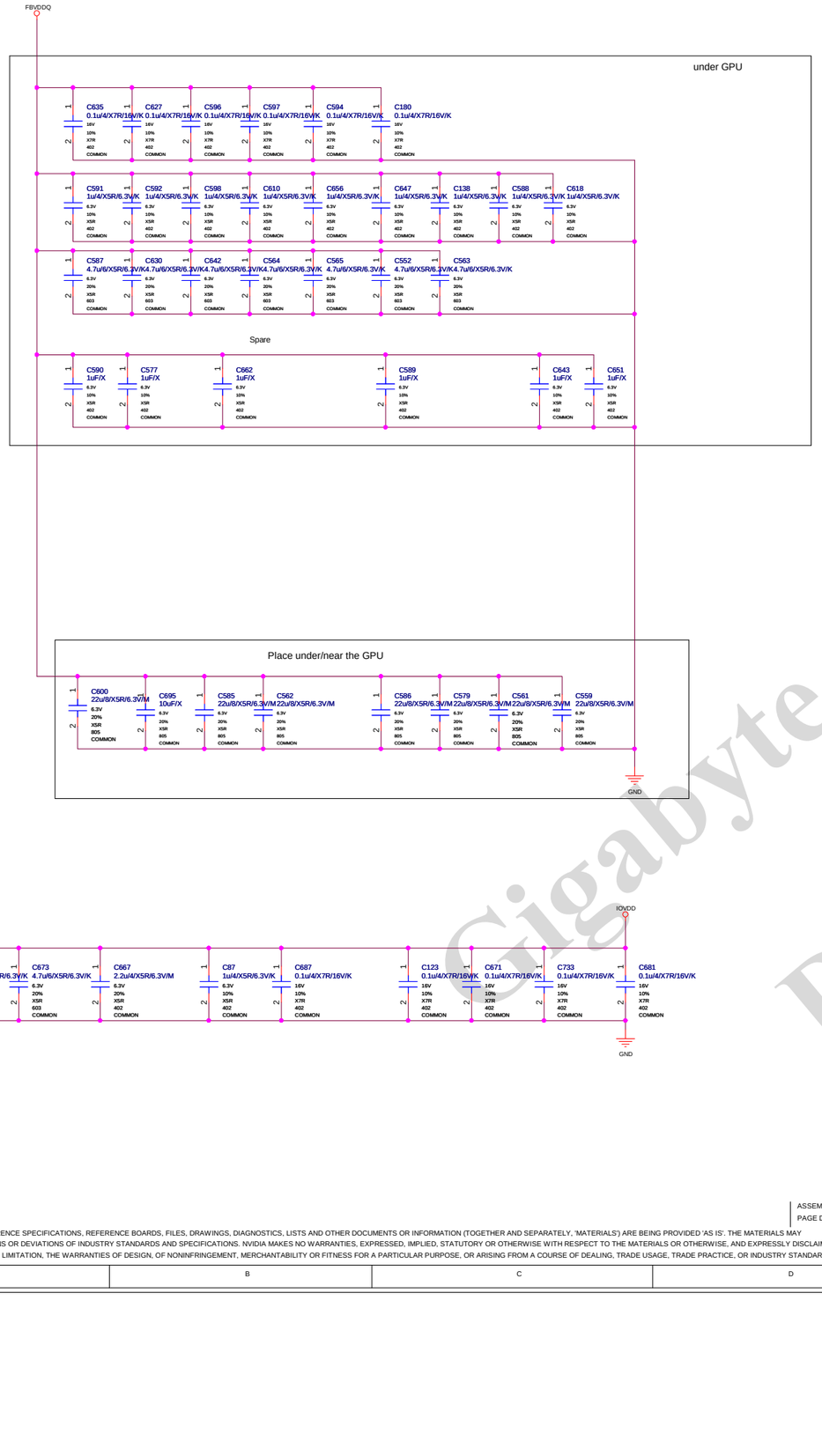
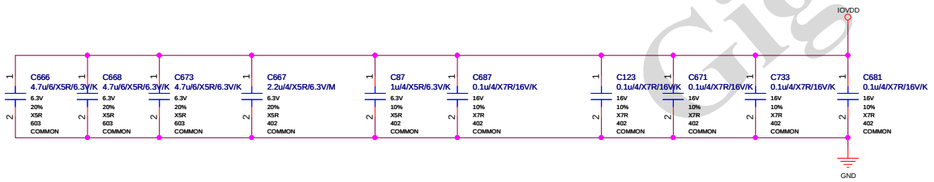
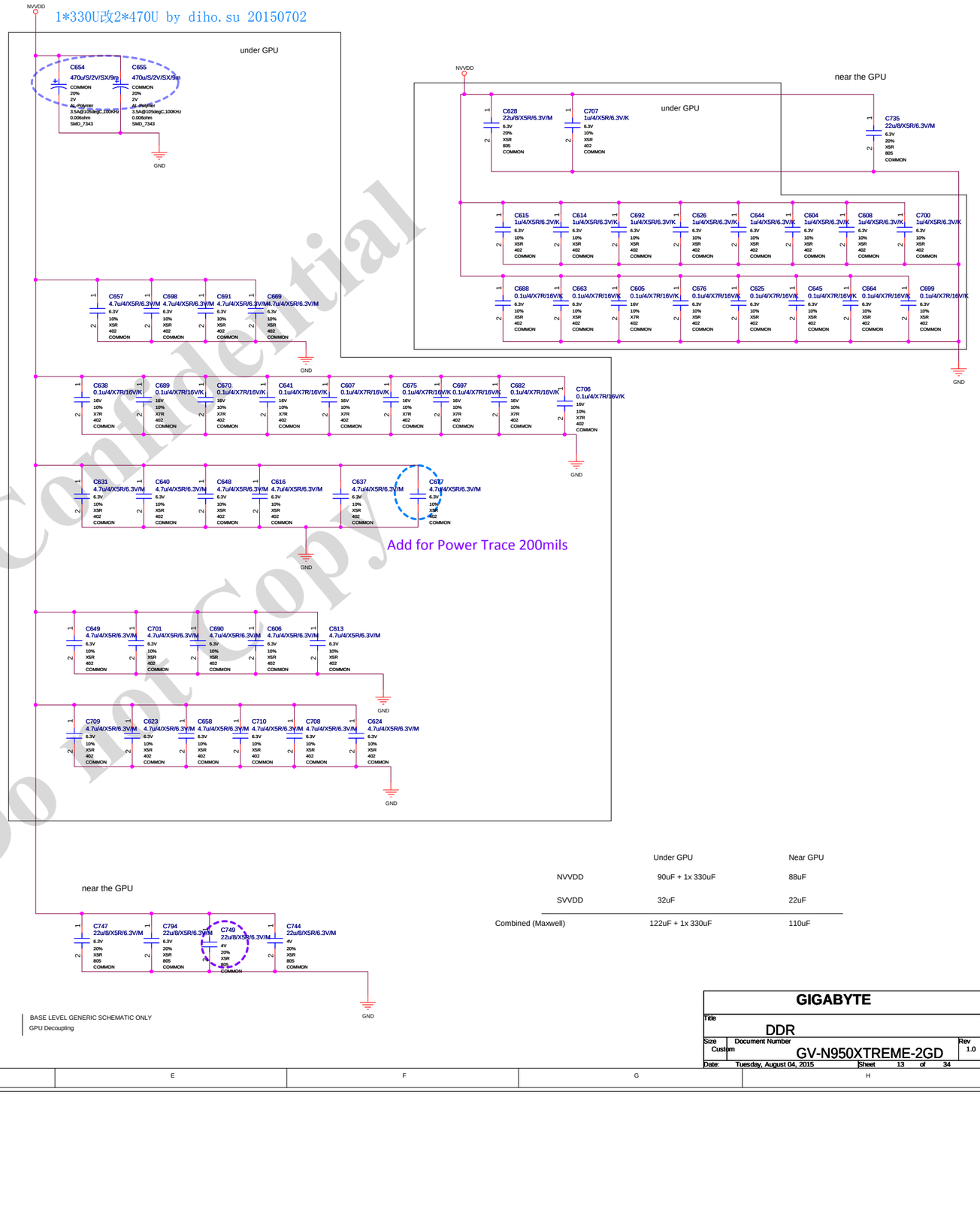
GPU Decoupling

FBVDDQ





NVVDD



	Under GPU	Near GPU
NVVDD	90uF + 1x 330uF	88uF
SVVDD	32uF	22uF
Combined (Maxwell)	122uF + 1x 330uF	110uF

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PAGE DETAIL | GPU Decoupling

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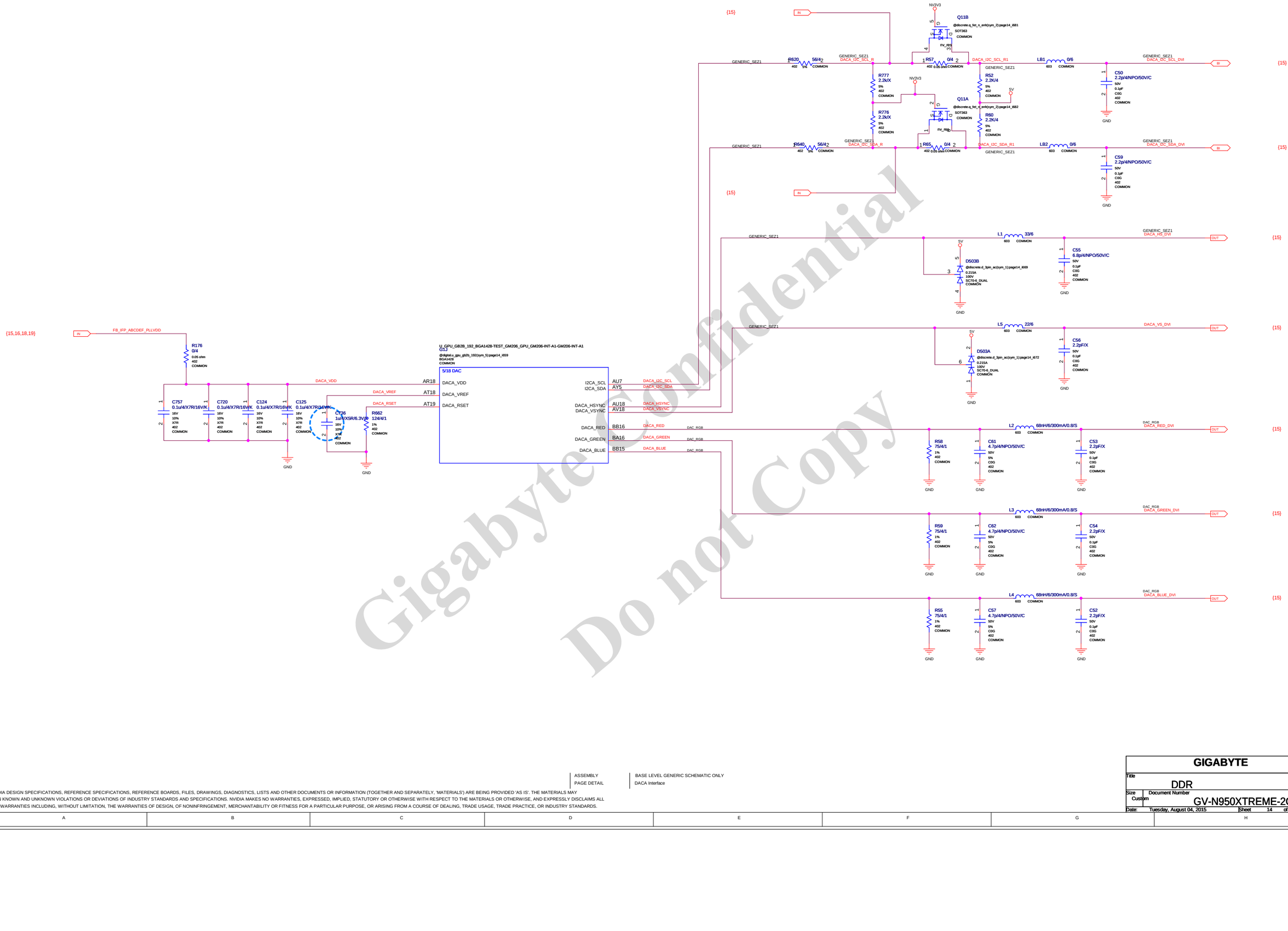
Title: DDR

Size: Custom | Document Number: GV-N950XTREME-2GD | Rev: 1.0

Date: Tuesday, August 04, 2015 | Sheet 13 of 34

DACA Interface



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DACA Interface

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Title: DDR

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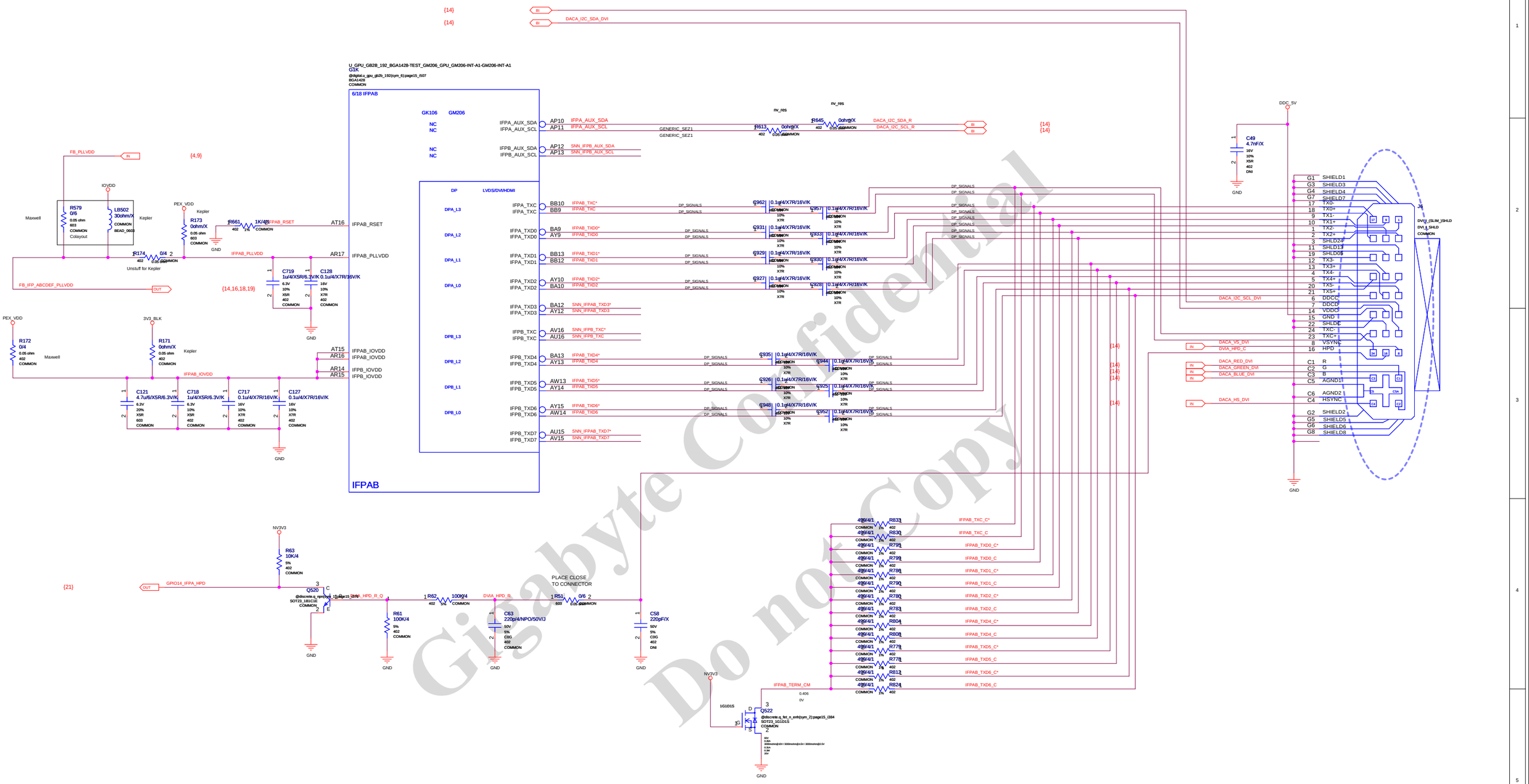
IFPAB DVI-I-DL



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IFPAB DVI-I-DL

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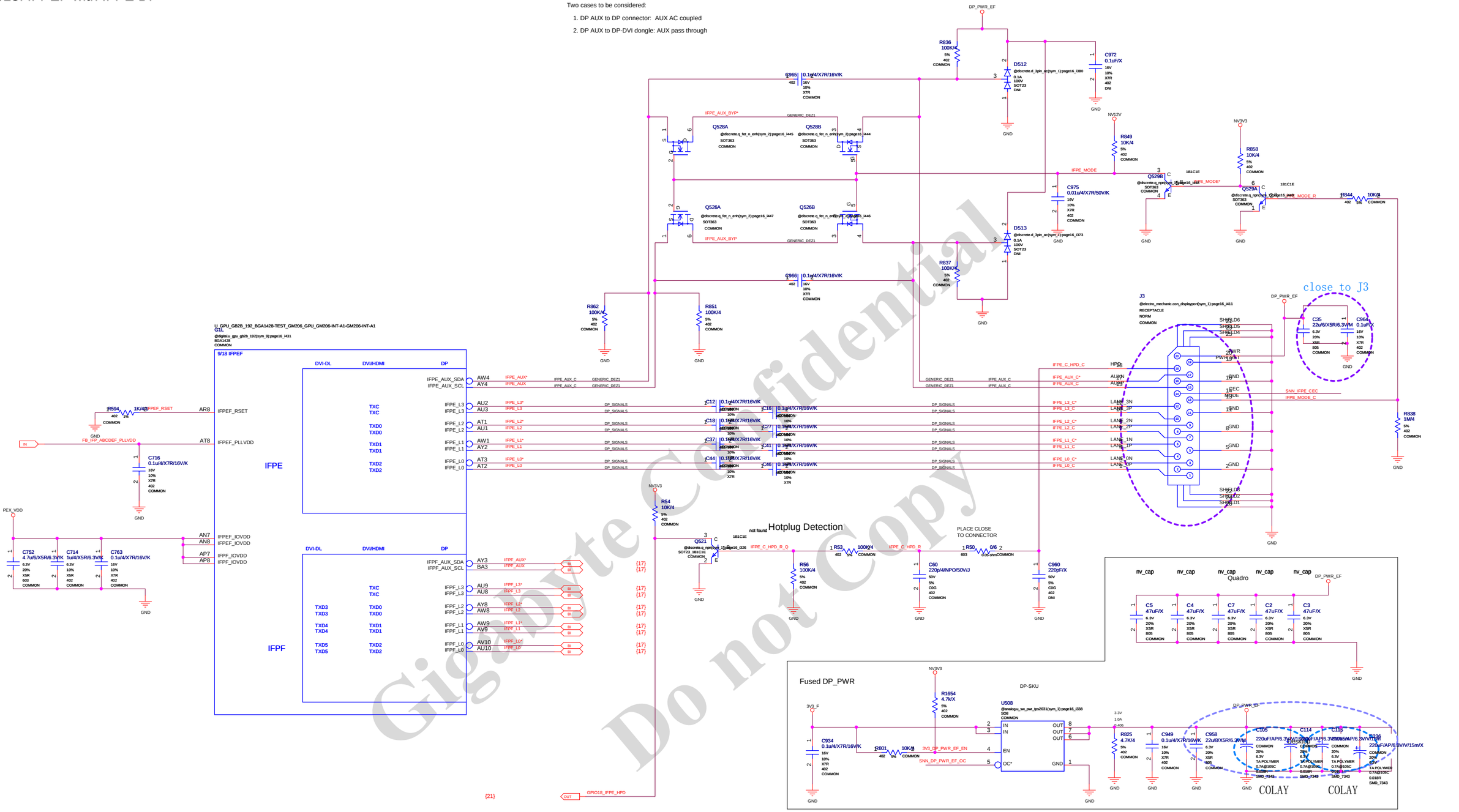
Page18: IFPEF with IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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IFPEF with IFPE DP

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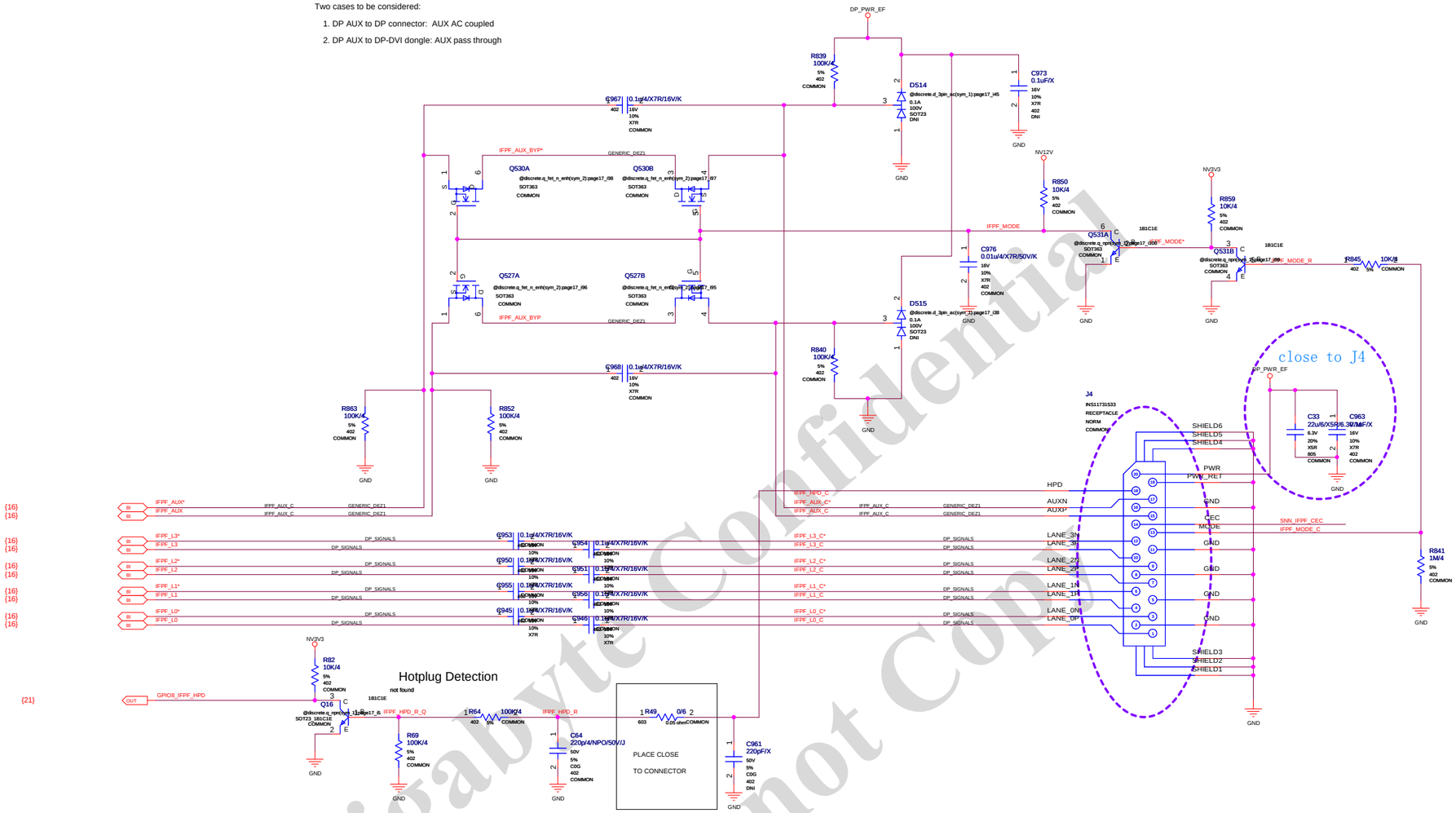
GIGABYTE			
Title	DDR		
Size: Custom	Document Number: GV-N950XTREME-2GD		Rev: 1.0
Date: Tuesday, August 04, 2015	Sheet 16 of 34		

IFPF DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPF DP

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Page20: IFPC HDMI/DP

* I2C to DDC level switching

FOR ESD DIODES

IFPC_ESD

C947 0.1uF/X 16V 10% X7R 402 DNI

Place near ESD diodes

DP-SKU ONLY

DP FOR QUADRO

del DP colay by diho.su 20150702

Fused DP_PWR

DP-SKU

COLAY

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PAGE DETAIL	IFPC HDMI/DP

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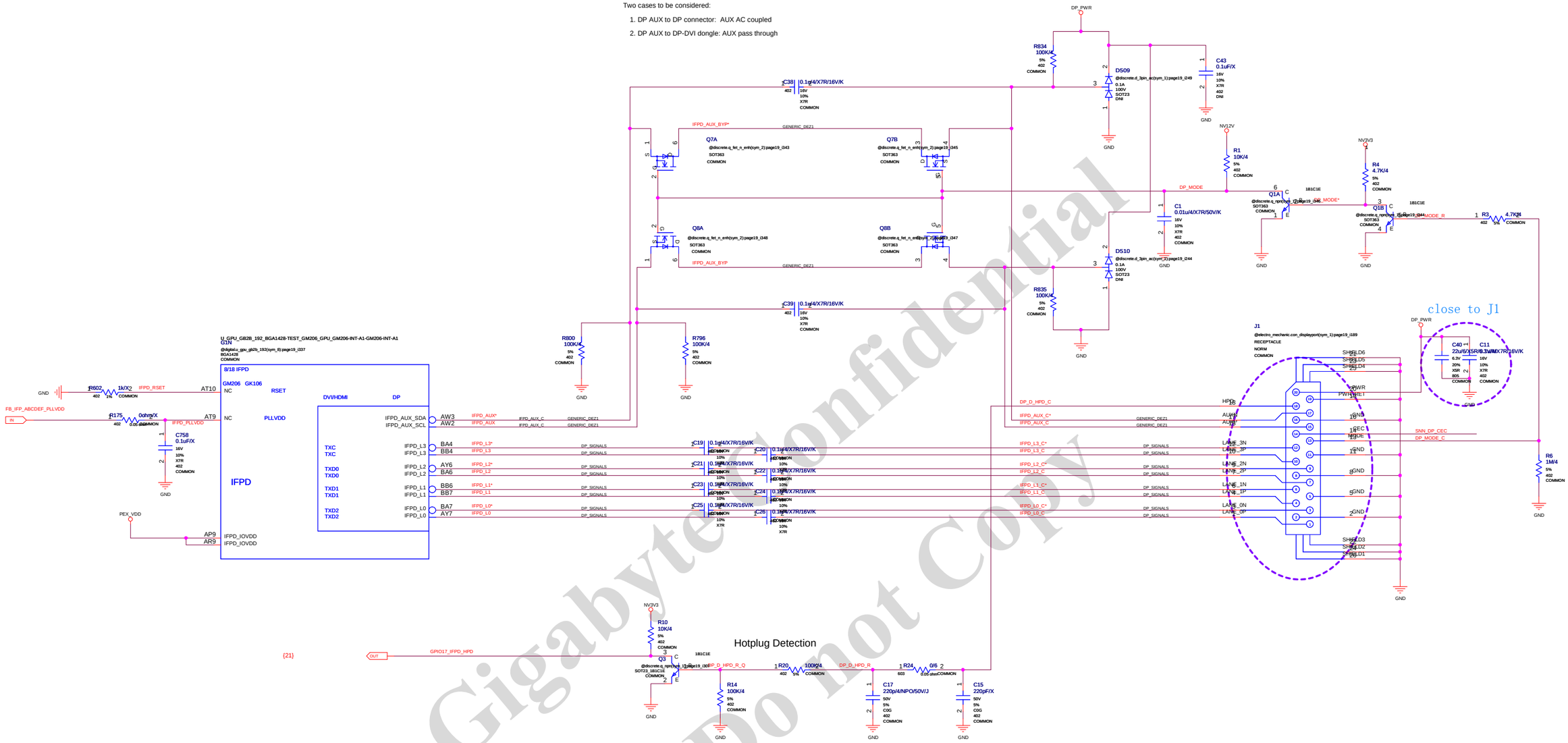
IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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PAGE DETAIL | IFPD DP

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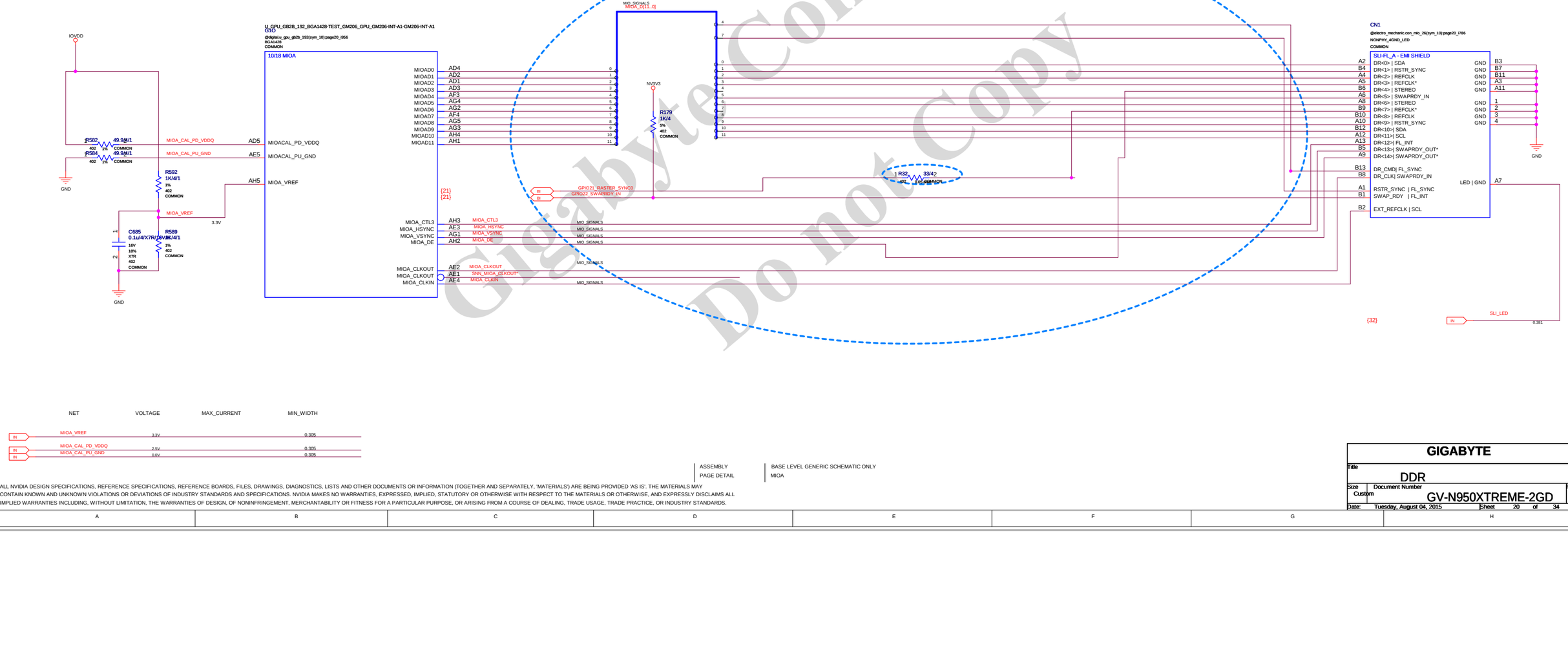
MIOA/SLI Interface

DEL MIO RESERVER CIRCUIT



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	3.3V		0.305
MIOA_CAL_PD_VDDQ	2.5V		0.305
MIOA_CAL_PU_GND	0.0V		0.305

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MIOA

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MISC1: Fan, Thermal, JTAG, GPIO

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1P
@digital:u_gpu_gb2b_192(sym_11):page21_ii416
BGA1428
COMMON

11/18 MISC_1

GM206 GK106

GK106 GM206

pads for deadbugging

C702 0.2pF/X 50V 0.1pF C0G 402 COMMON

C250 {21} {15} {16} {35} 0.1u/4/X7R/16V/K/X COMM0402 0402 X7R 10% 16V

C250 place close to GPU by diho.su 20150702

C536 1n/4/X7R/50V/K 16V 10% X7R 402 COMMON

C542 1u/6/X7R/16V/K 16V 10% X5R 603 COMMON

* JTAG

Use Low Vth device for 16nm

Q31 @discrete:q_fet_n_enh(sym_2):page21_i394 SOT23_1G1D1S DNI

Q30A Q30B Q32A Q32B Q504A Q504B Q516A Q516B @discrete:q_fet_n_enh(sym_2):page21_i503 SOT363 COMMON

D501 @discrete:d_3pin_schottky(sym_1):page21_i301 30V 0.2A SOT23 COMMON

J9 @electro_mechanic:hdr_1x4(sym_1):page21_i307 MALE 2.0MM N/A NORM COMMON

R184 10K/4 5% 402 COMMON

R183 10k/X 5% 402 COMMON

R185 0/4 402 0.05 ohm COMMON

R178 10K/4 5% 402 COMMON

R601 10k/X 5% 402 COMMON

R644 33/4/2 402 5% COMMON

R643 33/4/2 402 5% COMMON

R642 33/4/2 402 5% COMMON

R641 33/4/2 402 5% COMMON

R595 0ohm/X 402 0.05 ohm COMMON

R198 0/4 402 0.05 ohm COMMON

R593 10K/4 5% 402 COMMON

R545 10K/4 5% 402 COMMON

R537 10K/4 5% 402 COMMON

R555 0/8 805 COMMON

R210 0ohm/X 0.05 ohm 805 COMMON

R541 10k/X 5% 402 DNI

R586 10k/X 5% 402 COMMON

R182 10k/X 5% 402 DNI

R202 10k/X 5% 402 COMMON

R616 10k/X 5% 402 DNI

R599 10k/X 5% 402 DNI

R590 10k/X 5% 402 DNI

R607 10K/4 5% 402 COMMON

R522 10k/X 5% 402 COMMON

R502 10K/4 402 0.05 ohm COMMON

R501 10k/X 5% 402 COMMON

R521 0/4 402 0.05 ohm COMMON

R131 10k/X 5% 402 DNI

R121 10k/X 5% 402 DNI

R112 180ohm/X 5% 402 DNI

R687 10K/4 5% 402 COMMON

R736 270ohm/X 5% 402 DNI

R668 2.2K/4 5% 402 COMMON

R649 2.2k/4 5% 402 COMMON

R650 2.2k/4 5% 402 COMMON

R164 0/4 402 0.05 ohm COMMON

R652 0/4 402 0.05 ohm COMMON

R651 0/4 402 0.05 ohm COMMON

R1656 2.2k/X 5% 402 COMMON

R1657 2.2k/X 5% 402 COMMON

R1658 2.2k/X 5% 402 COMMON

R1659 2.2k/X 5% 402 COMMON

R188 10k/X 5% 402 COMMON

R189 0/4 402 0.05 ohm COMMON

R671 2.2K/4 5% 402 COMMON

R161 0/4 402 0.05 ohm COMMON

R190 10K/4 5% 402 COMMON

AN3	OVERT	GPIO8	
AM8	THERMDN		
AL8	THERMDP		
AV6	I2CS_SCL		
AU6	I2CS_SDA		
AW7	I2CC_SCL		
AV7	I2CC_SDA		
AW5	I2CB_SCL		
AW6	I2CB_SDA		
AT6	GPIO0_NVAPI_1_PWM_VID		
AT7	SNN_GPIO1_SVDD_PWM_VID		
AL1	SNN_GPIO2		
AL2	GPIO3_OC_WARN*		
AP3	GPIO4_GPU_IFPF_HPD_GK106		
AP4	GPIO5_FRAME_LOCK_INT		
AK1	GPIO6_GPU_PSI*		
AK2	GPIO7_FBVDD_SEL		
AG7	GPIO8_GPU_IFPF_HPD		
AR6	GPIO9_GPU_THERM_ALERT*		
AM3	GPIO10_FBVREF_SEL		
AM4	GPIO11_LOGO_LED		
AR3	GPIO12_GPU_LOW_PERF*		
AJ3			
AL3	GPIO14_IFPA_HPD		
AL4	GPIO15_IFPC_HPD		
AR4	GPIO16_FAN_PWM		
AP5	GPIO17_IFPD_HPD		
AN5	GPIO18_IFPE_HPD		
AK3			
AK4	GPIO20_SLI_LED_DIM		
AL5	GPIO21_RASTER_SYNC0		
AK5	GPIO22_SWAPRDY_IN		
AJ4	GPIO23_RASTER_SYNC1		
AN4	GPIO24_SWAPRDY_OUT		
AK8	SNN_GPIO25		
AH6	SNN_GPIO26		
AG6	GPIO27		
BA18	JTAG_TCK	GPIO8_NC	
AW16	JTAG_TMS		
AW18	JTAG_TDI		
AY18	JTAG_TDO		
AY16	JTAG_TRST		

GPIO25_NC
GPIO26_NC
GPIO27_NC

JTAG_TCLK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST*

THERM_OVERT_GPU*
THERM_OVERT*
I2CC_SCL_GPU
I2CC_SDA_GPU
GPIO9_GPU_THERM_ALERT*
GPIO13_FAN_TACH
FAN_PWR
GPIO6_GPU_PSI*
GPIO12_GPU_LOW_PERF*
I2CC_SDA_GPU
I2CB_SCL_GPU
I2CB_SDA_GPU
I2CC_SDA_R
I2CB_SCL_R
I2CB_SDA_R
I2CC_SCL_GPU
GPIO9_GPU_THERM_ALERT*
I2CC_SCL_R

IOVDD
NV3V3
12V_F
12V_PEX6_F1
3V3_F
GND

ASSEMBLY
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MISC1: Fan, Thermal, JTAG, GPIO

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MISC2: ROM, XTAL, Straps

	KEPLER	MAXWELL
STRAP0	USER_BIT [3:0]*	
STRAP1	3GIO_PADCFG_LUT_ADR*	
STRAP2	PCI_DEVID [3:0]*	
STRAP3	SOR_EXPOSED [3:0]*	
STRAP4	DP_PLL_VDD_33V*	
	PEX_MAX_SPEED*	
	PEX_SPD_CHANGE_GEN3*	
	*	
ROM_SI	RAMCFG[0]*	RAMCFG[0]*
	RAMCFG[1]*	RAMCFG[1]*
	RAMCFG[2]*	RAMCFG[2]*
	RAMCFG[3]*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	VGA_DEVICE*
	SMB_ALT_ADDR*	SMB_ALT_ADDR*
	FB[0]_APERTURE_SIZE*	PCIE_CFG*
	FB[1]_APERTURE_SIZE*	DEVID_SEL*
ROM_SCLK	PEX_PLL_EN_TERM100*	SOR0_EXPOSED*
	PCI_DEVID_EXT[5]*	SOR1_EXPOSED*
	SUB_VENDOR*	SOR2_EXPOSED*
	PCI_DEVID_EXT[4]*	SOR3_EXPOSED*

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

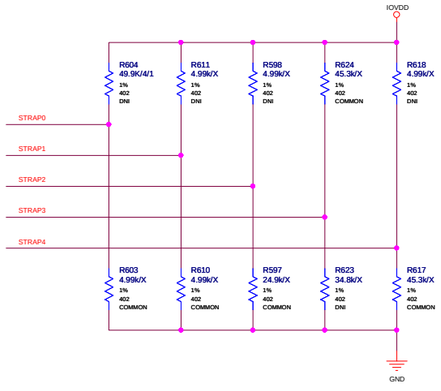
MULTI_STRAP_REF0_GND

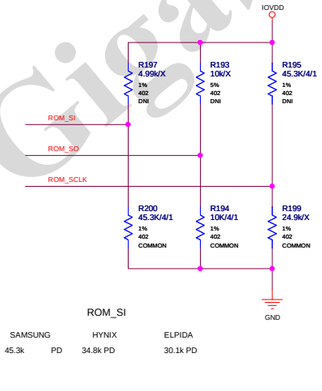
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND

MAXWELL

STRAP0

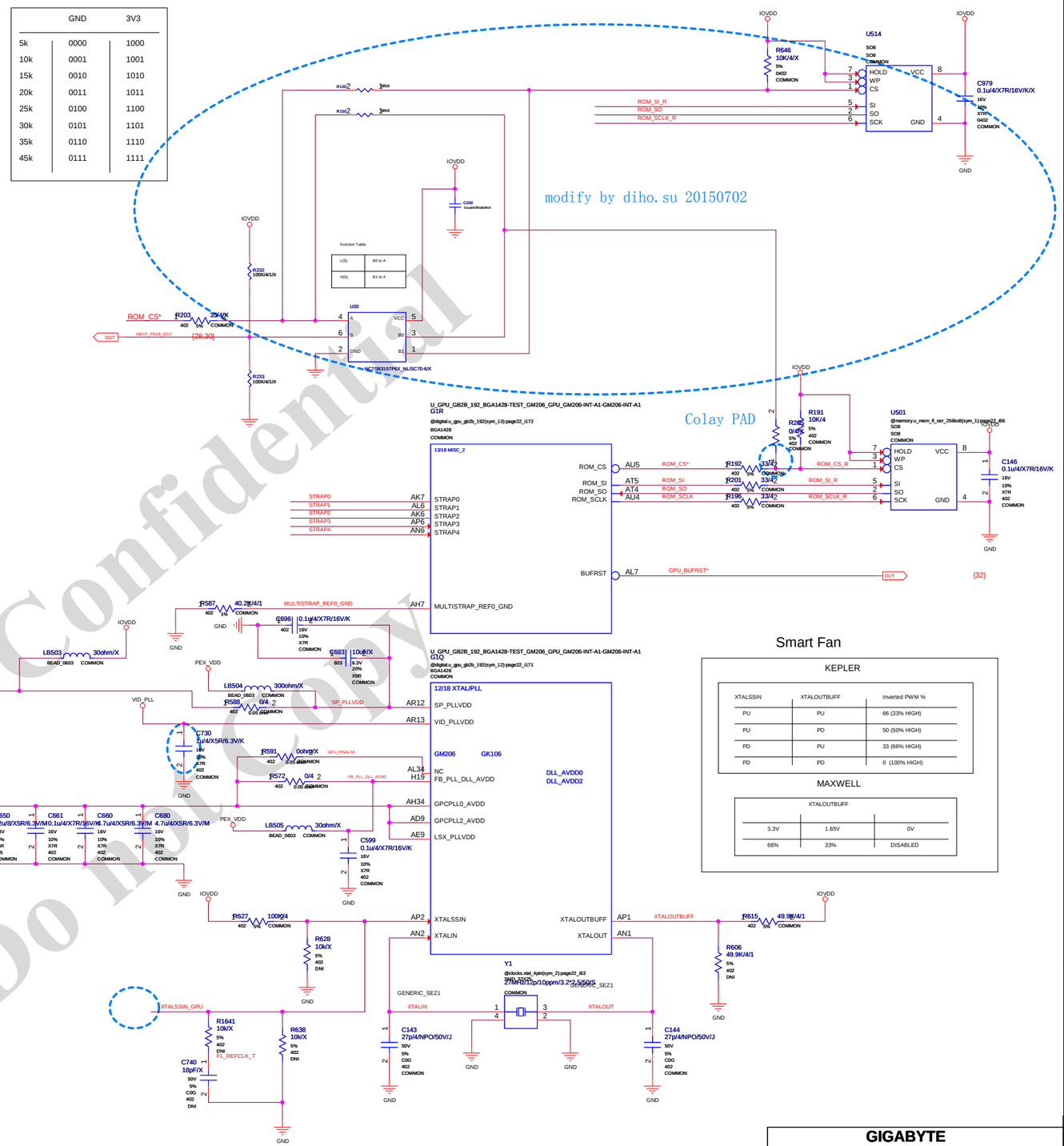
3.3V	1.65V	0V
GC6+ ISLAND ENABLED	GC6+ DEBUG MODE	GC6+ ISLAND DISABLED





ROM_SI

SAMSUNG	HYNIX	ELPIDA
45.3k PD	34.8k PD	30.1k PD



Smart Fan

KEPLER

XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

MAXWELL

XTALOUTBUFF		
3.3V	1.65V	0V
66%	33%	DISABLED

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MISC2: ROM, XTAL, Straps

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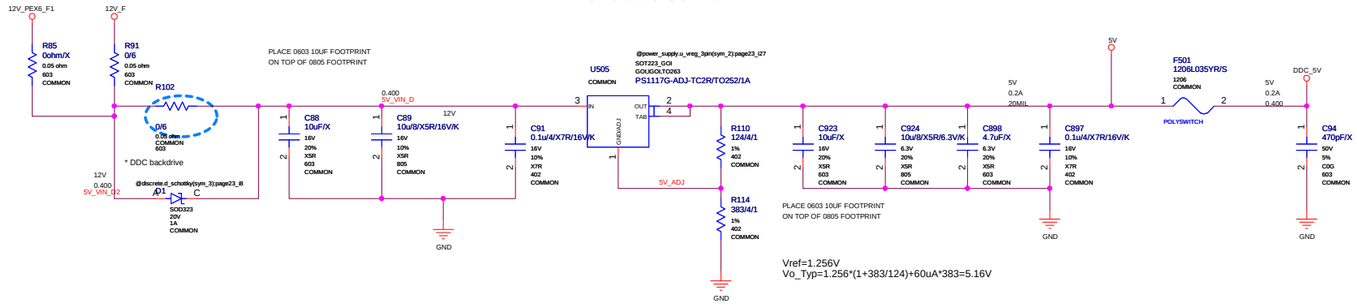
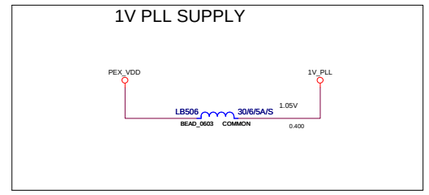
PS: 5V, PEX_VDD

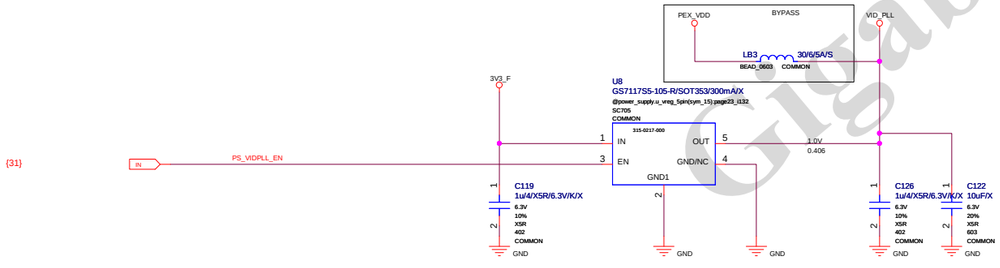
5V / DDC SUPPLY



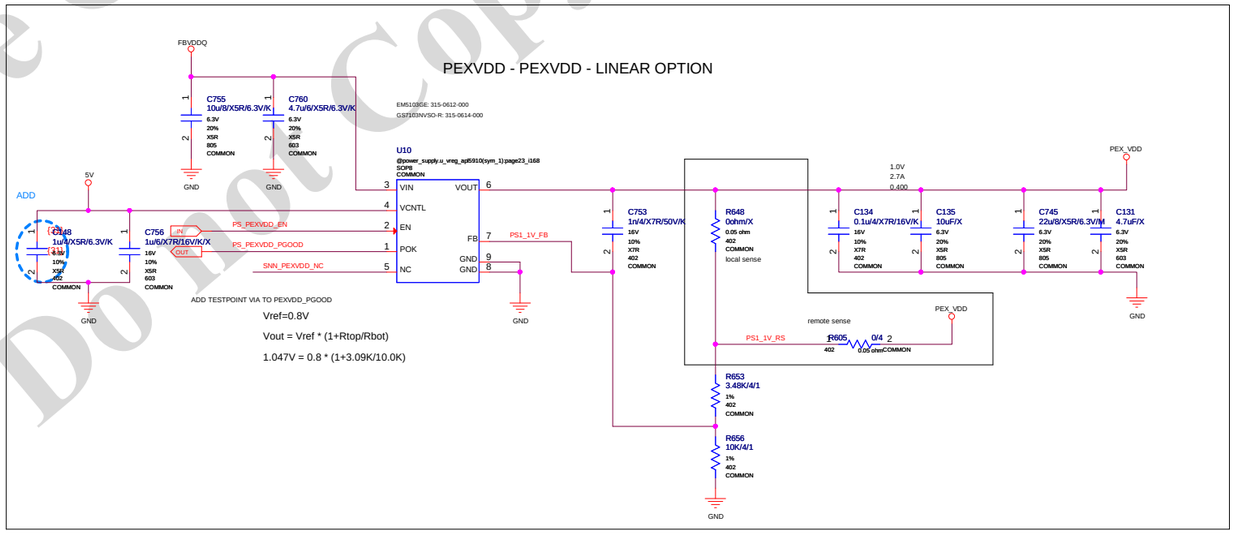
1V PLL SUPPLY



VID PLL SUPPLY



PEXVDD - PEXVDD - LINEAR OPTION



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BASE LEVEL GENERIC SCHEMATIC ONLY
PS: 5V, PEX_VDD, VID_PLL

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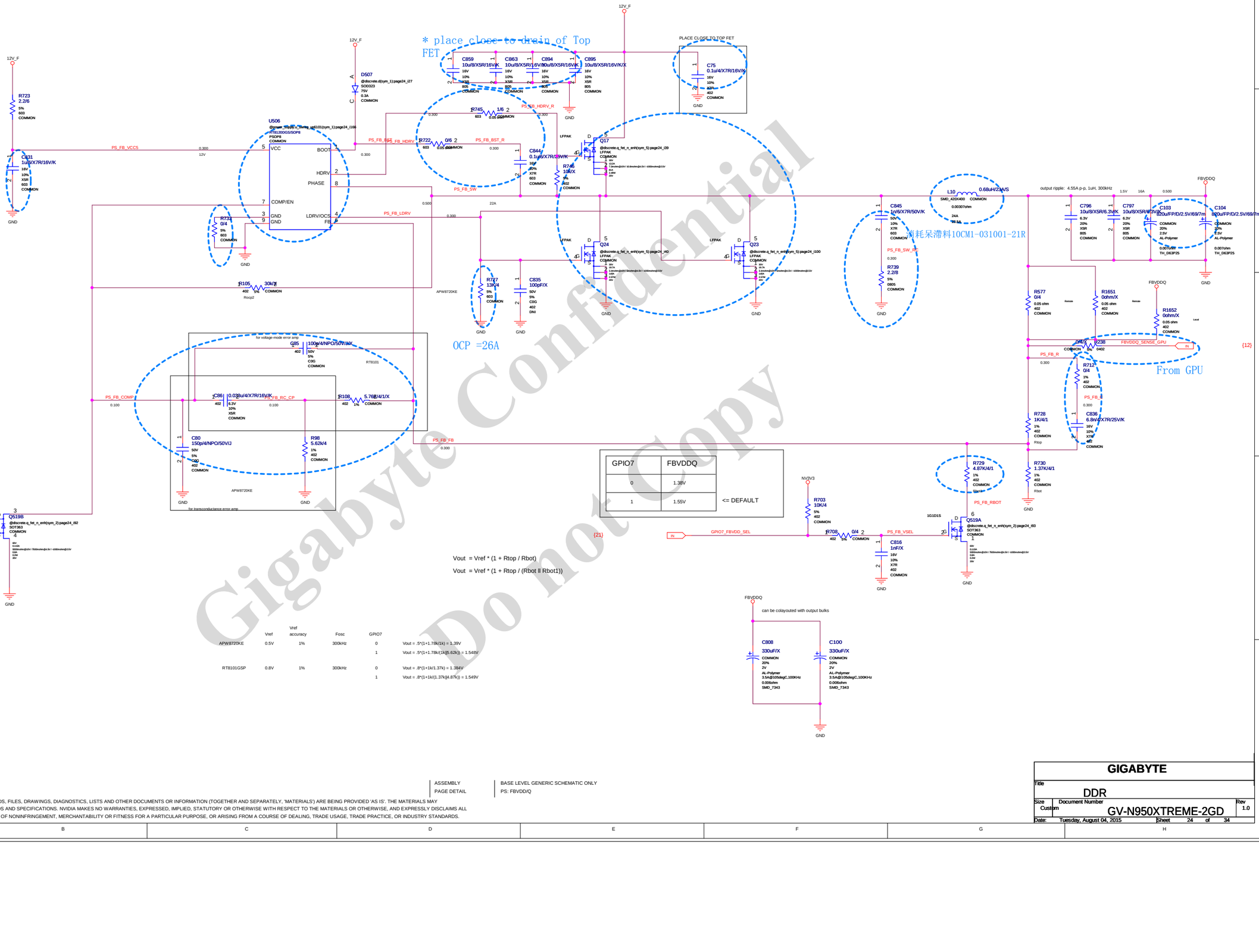
PS: FBVDDQ



	Vref	Vref accuracy	Fosc	GPIO7	
APW8720KE	0.5V	1%	300kHz	0	Vout = .5*(1+1.78k/1k) = 1.39V
				1	Vout = .5*(1+1.78k/(1k‖5.62k)) = 1.548V
RTB101GSP	0.8V	1%	300kHz	0	Vout = .8*(1+1k/1.37k) = 1.384V
				1	Vout = .8*(1+1k/(1.37k‖4.87k)) = 1.549V

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PS: FBVDD/Q

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PS: NVVDD Controller

Overshoot Recovery Enhancement

R_VREF1	R_VREF2	R_REFADJ	Vboot	Vmax	Vmin
6.98k	6.04k	6.04k	0.95V	1.302V	0.604V

RDRP1	RDRP2	CDRP		
open circuit	dont care	dont care	0 ohm	DC Loadline
dont care	1.91k	4.7nF	1.3mOhm AC Loadline, 9us recovery	

RLIM1	RLIM2	OCP
12.1k	3.3k	240A

ROSC	Fsw
24.3K	400kHz

RESERVE FOR NTC

PLACE NTC_N RESISTOR CLOSE TO PHASE 1 INDUCTOR AND ON THE SAME OF THE BOARD AS THE INDUCTOR

ASSEMBLY
PAGE DETAIL

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PS: NVVDD Controller OVR4 option

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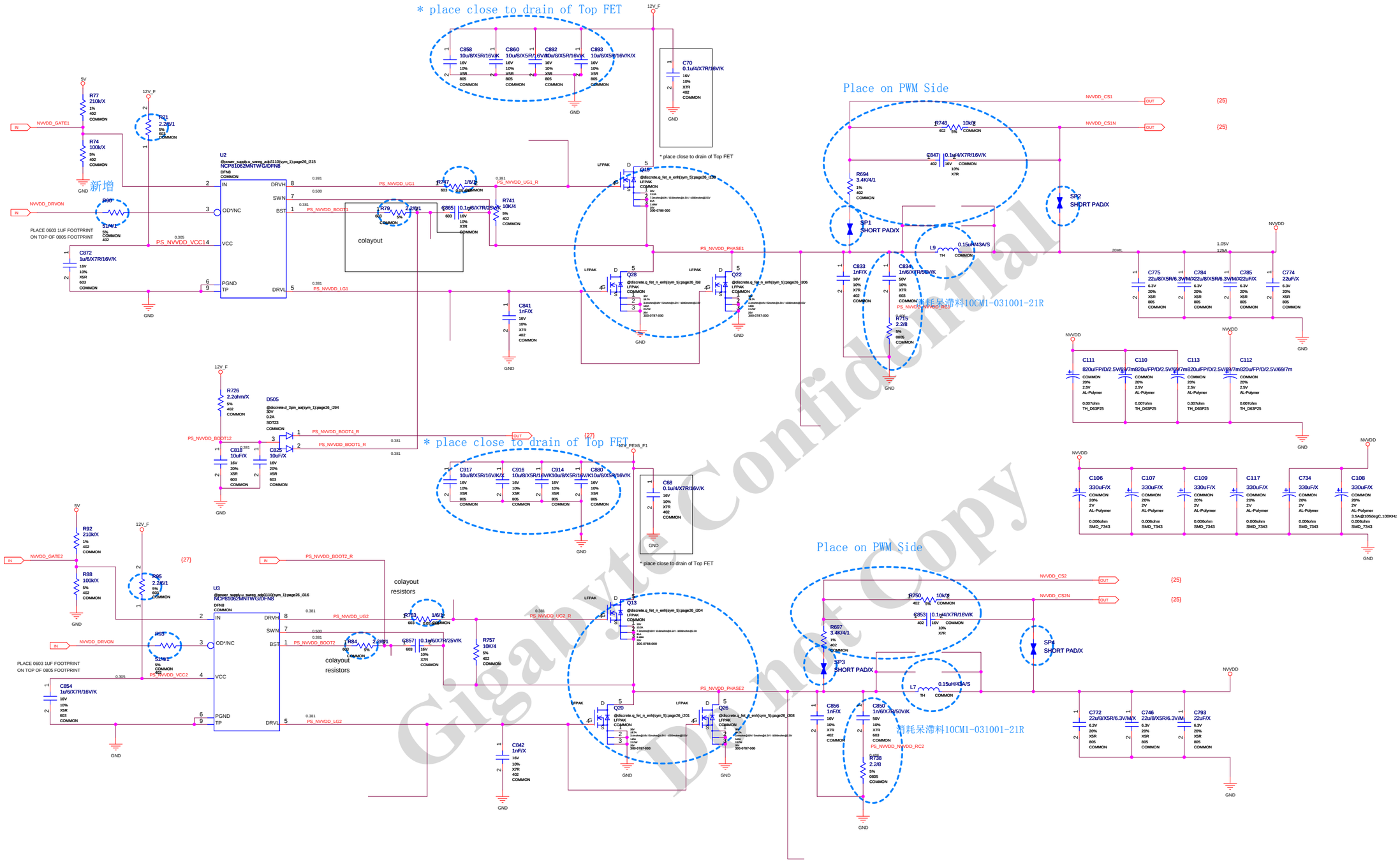
PS: NVVDD Phase 1,2



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PAGE DETAIL	PS: NVVDD Phase 1,2

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PS: NVVDD Phase 3,4

* place close to drain of Top FET

Place on PWM Side

* place close to drain of Top FET

Place on PWM Side

stuff 0ohm for 3phase

上件phase4 by diho.su 20150702

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ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
PS: NVVDD Phase 3,4

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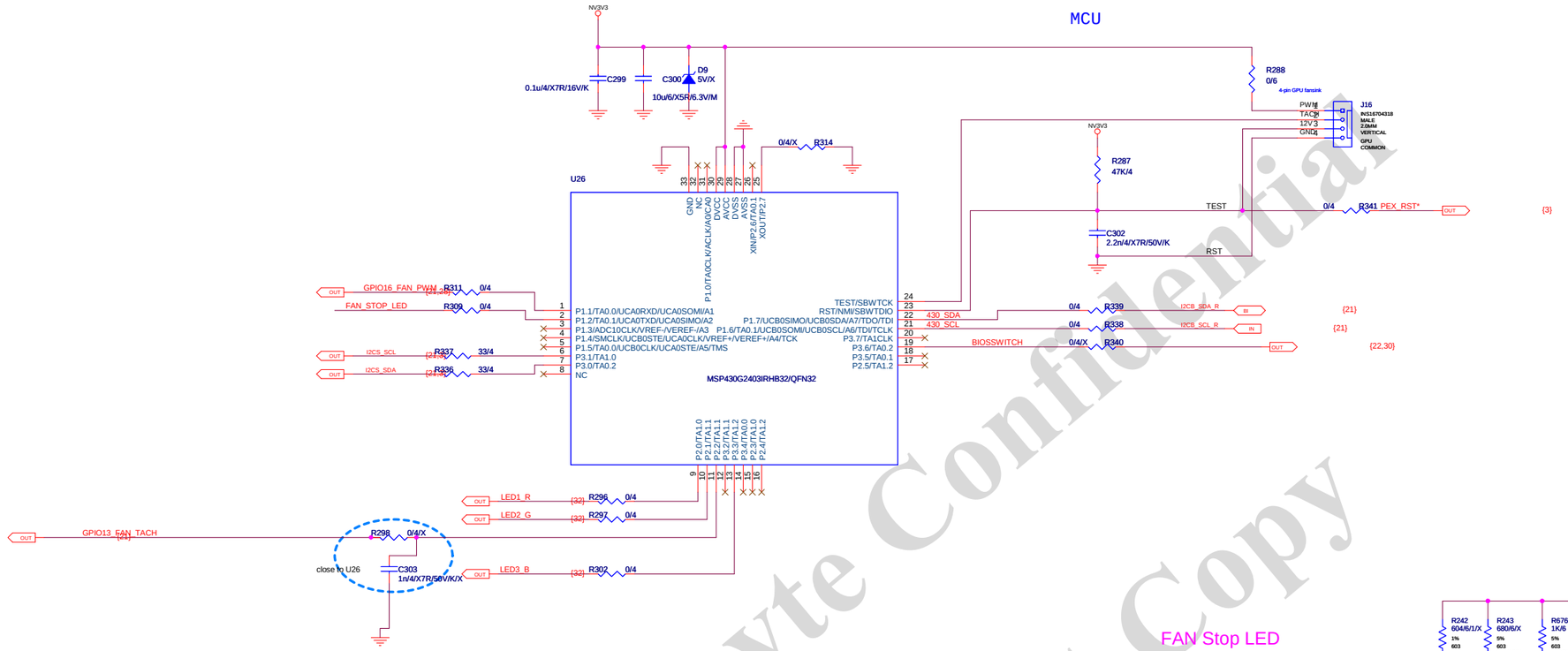
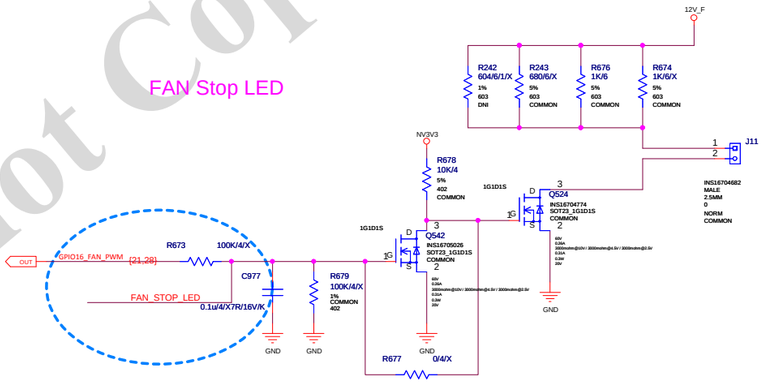
Multi Colors LED Winforce Control by diho.su 20150702

MCU



FAN Stop LED



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PAGE DETAIL | [RESERVED]

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PS: NVVDD OVR2+1 POWER

DEL NVVDD COLAY PWM

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PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
PS: NVVDD OVR2+1 option

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GIGABYTE		
Title: DDR		
Size: Custom	Document Number: GV-N950XTREME-2GD	Rev: 1.0
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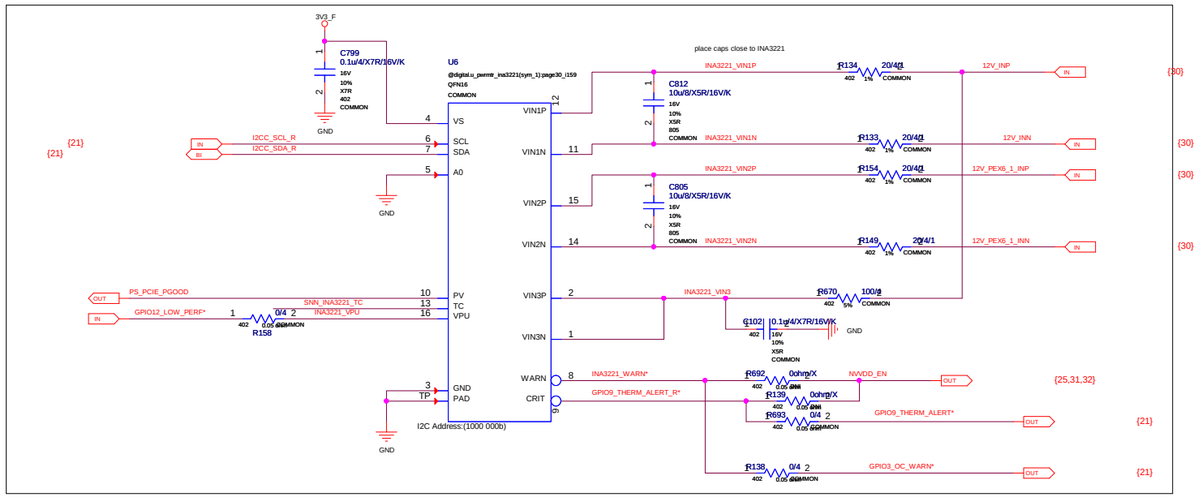
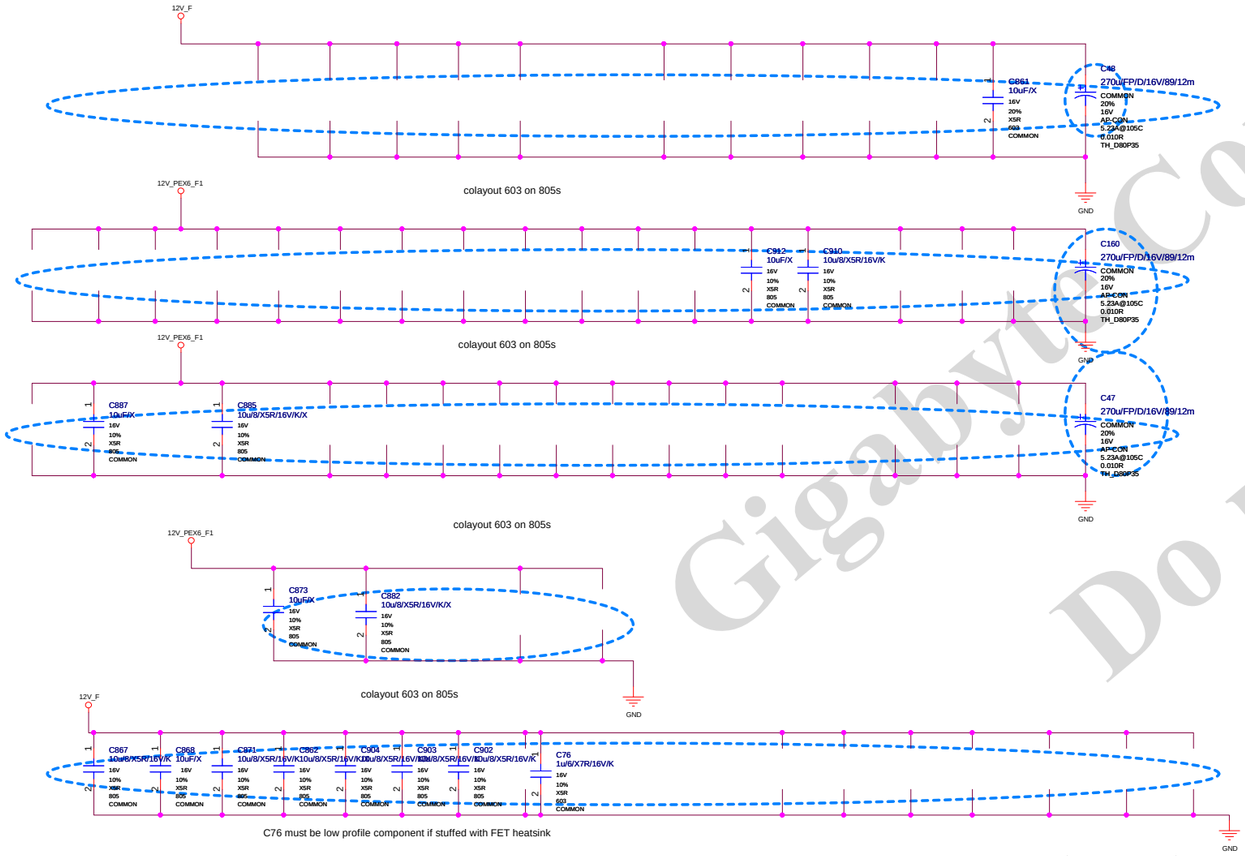
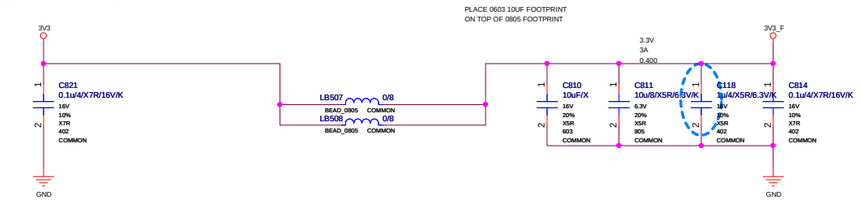
PS: Inputs, Filtering, and Monitoring

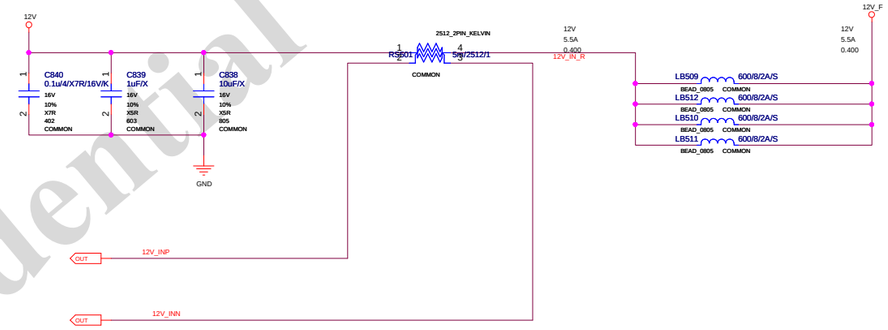




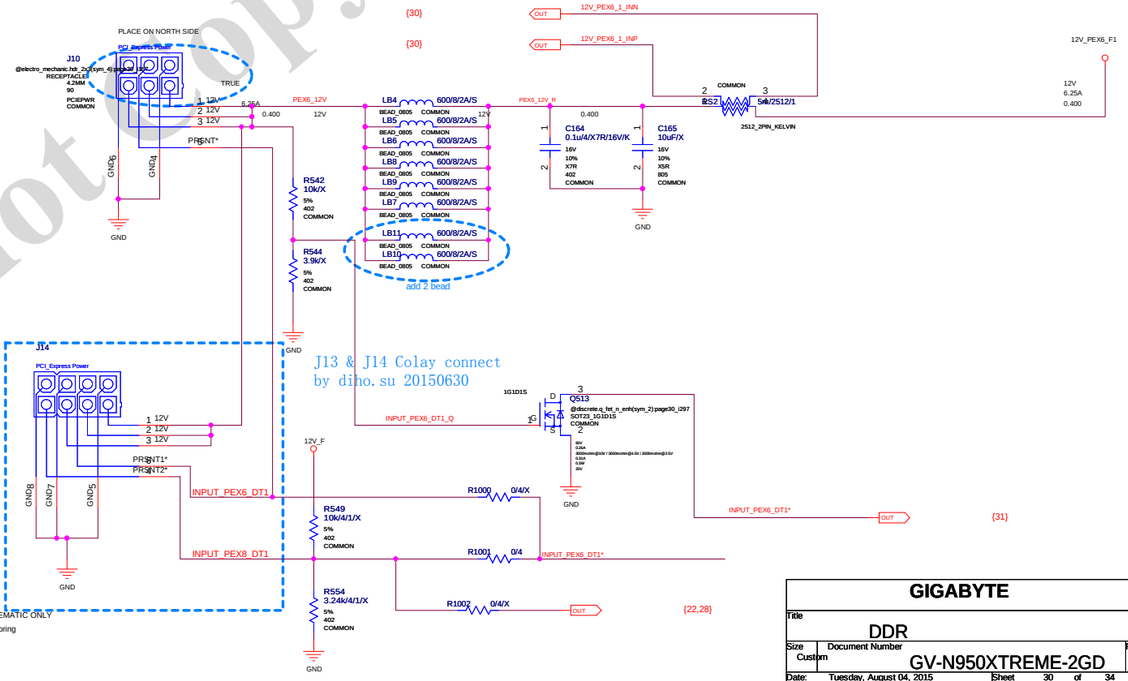
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX6 INPUT - 2x3 PCIE CON 75W



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

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	DDR		
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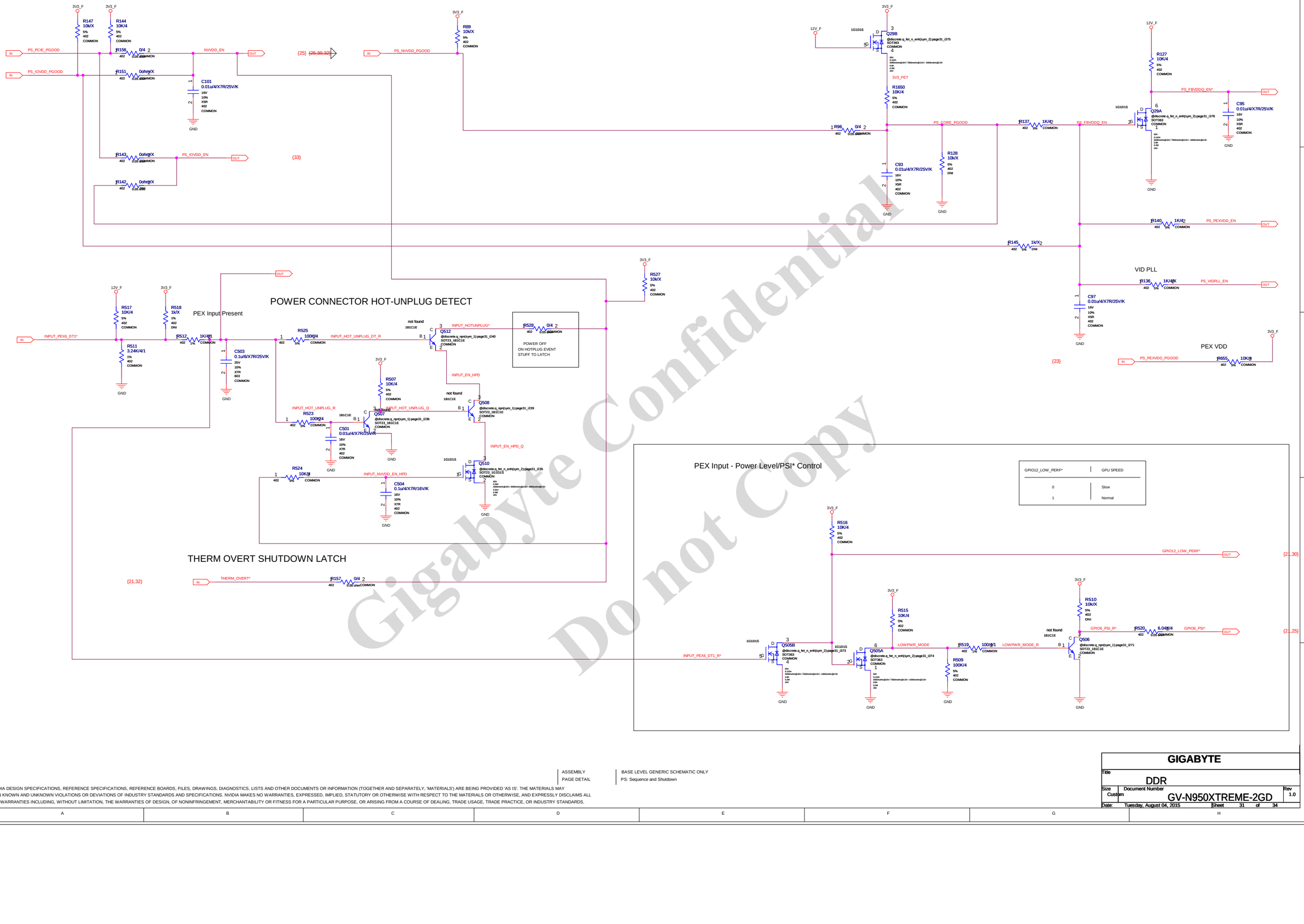
PS: Sequence and Shutdown



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ASSEMBLY
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BASE LEVEL GENERIC SCHEMATIC ONLY
PS: Sequence and Shutdown

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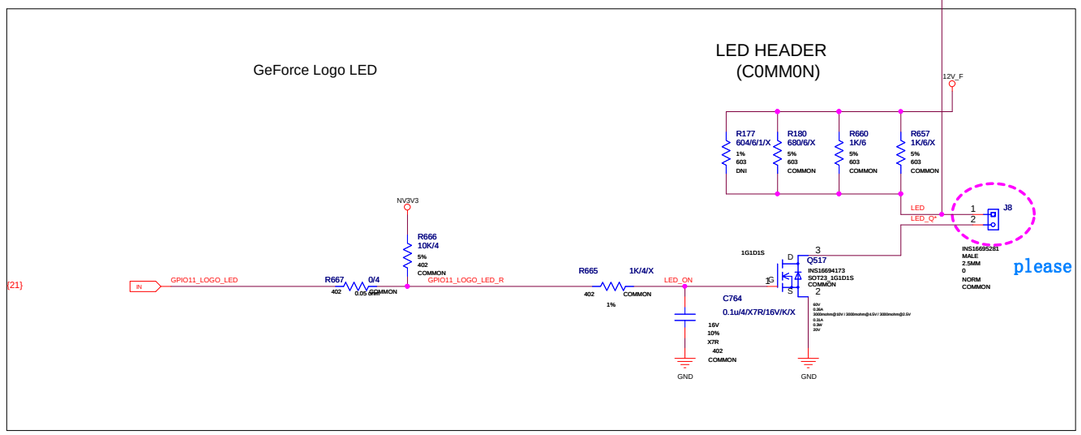
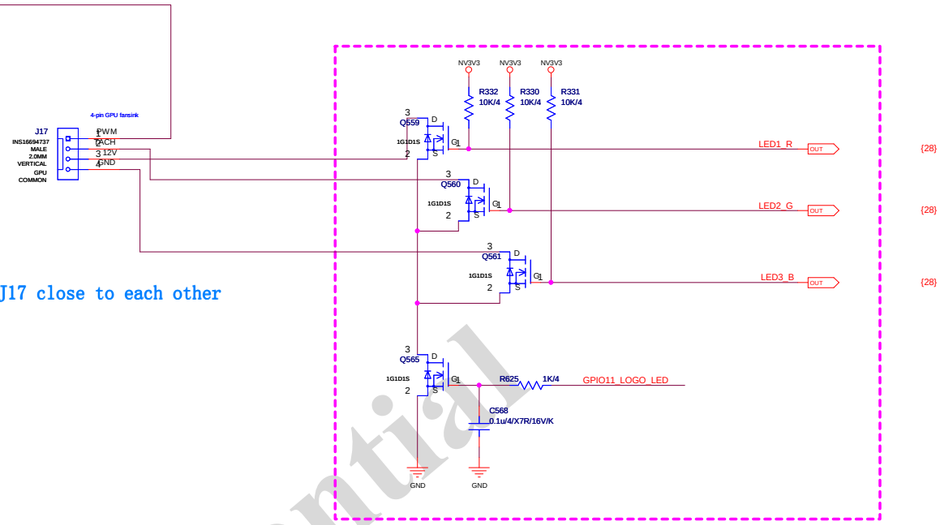
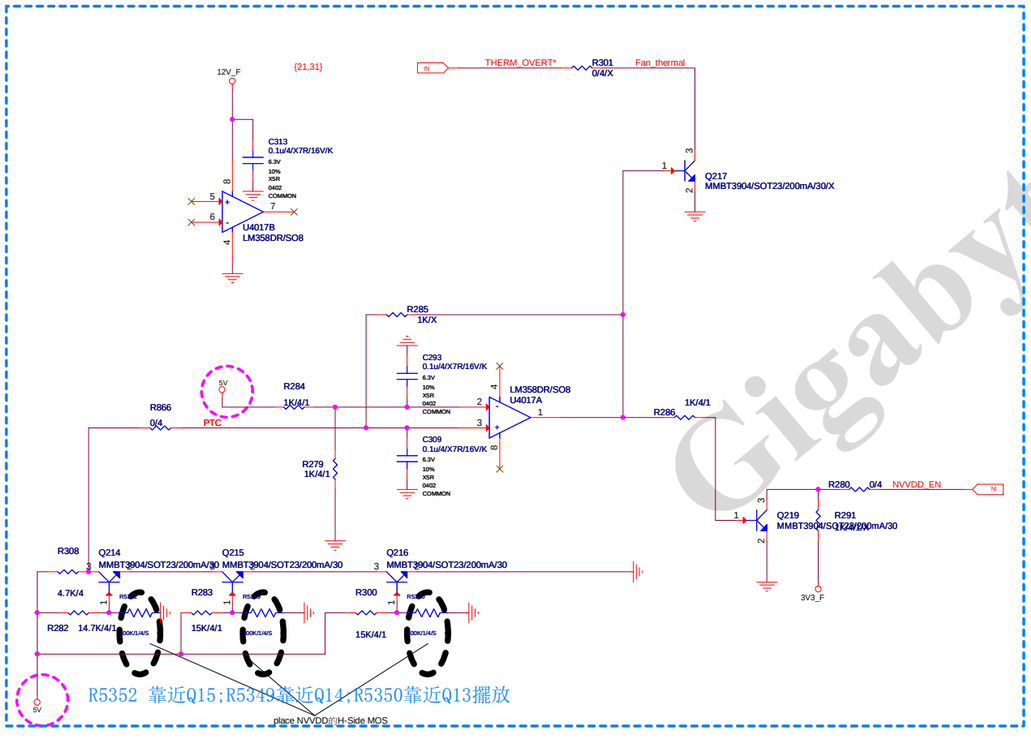
GIGABYTE

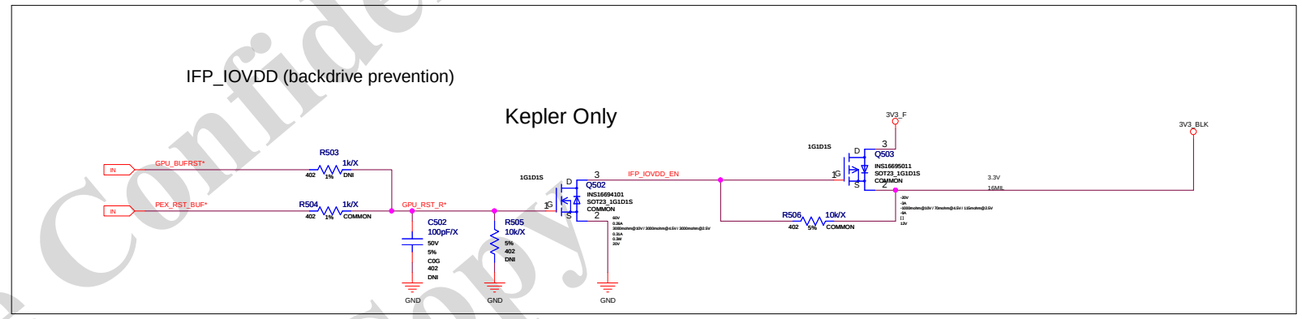
LEDs & 3 Pin FAN

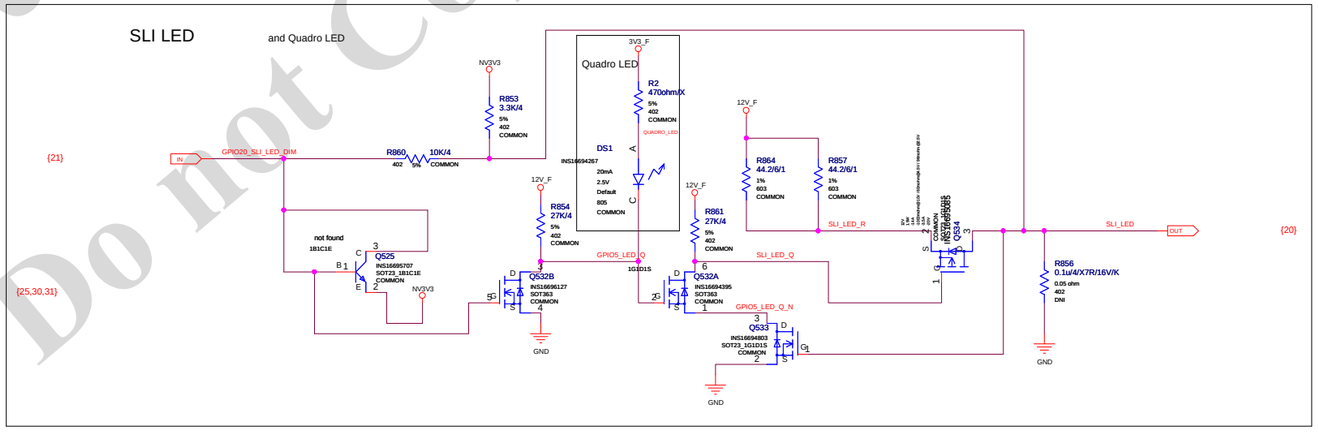


please place J8&J17 close to each other









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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	LEDs

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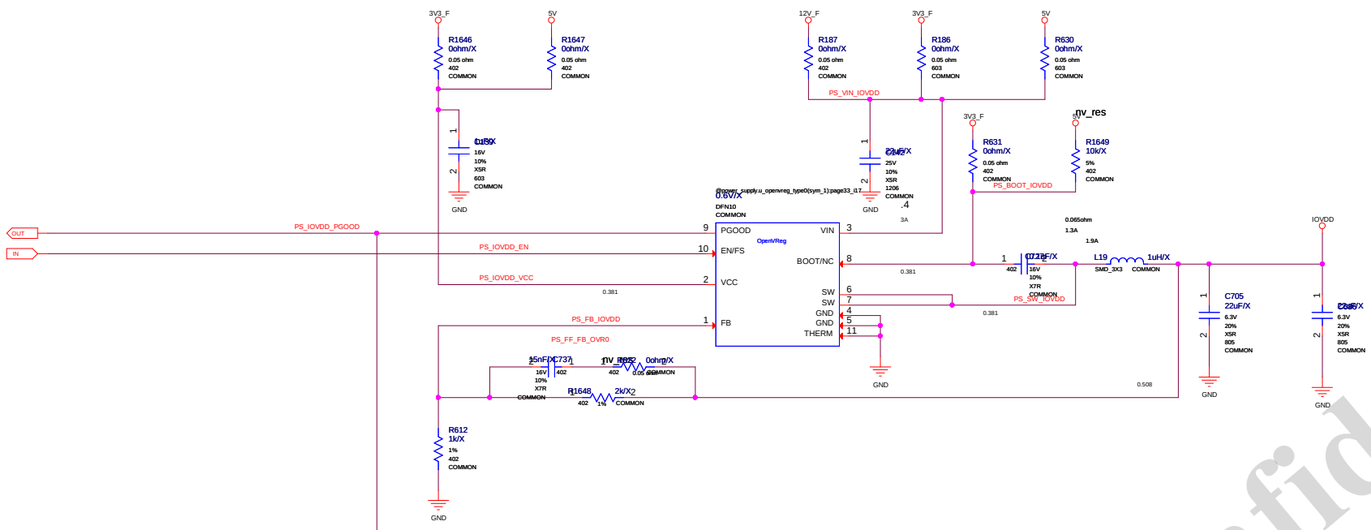
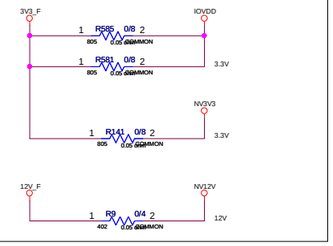
PS: IOVDD, NV3V3, NV12V

OVR0 1.8V REGULATOR. STUFF FOR 16nm



Special Note:
1. Place [C_OUT] close to [L_OUT]
2. Use local FB sense (refer to design guide for detals)
3. Place PLL/IO filter ferrite bead to the same position as FB local sense point

BYPASS. STUFF FOR 28nm



Gated rails required for 16nm

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PS: IOVDD Regulator

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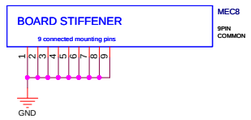
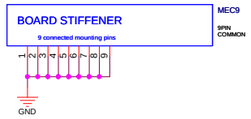
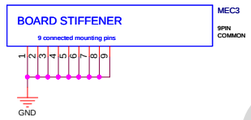
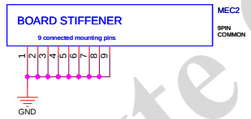
Mechanical: Bracket/Thermal Solution

GPU 螺絲孔

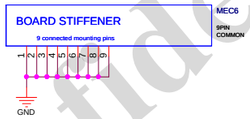


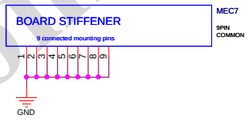


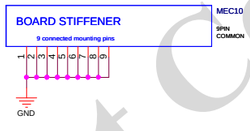


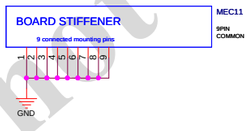


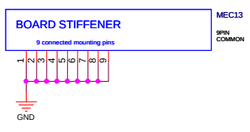
MOS 螺絲孔



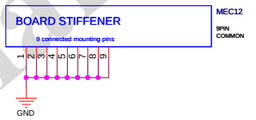








BK 螺絲孔



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MECH: Bracket/Thermal

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