

PG150-C03

384b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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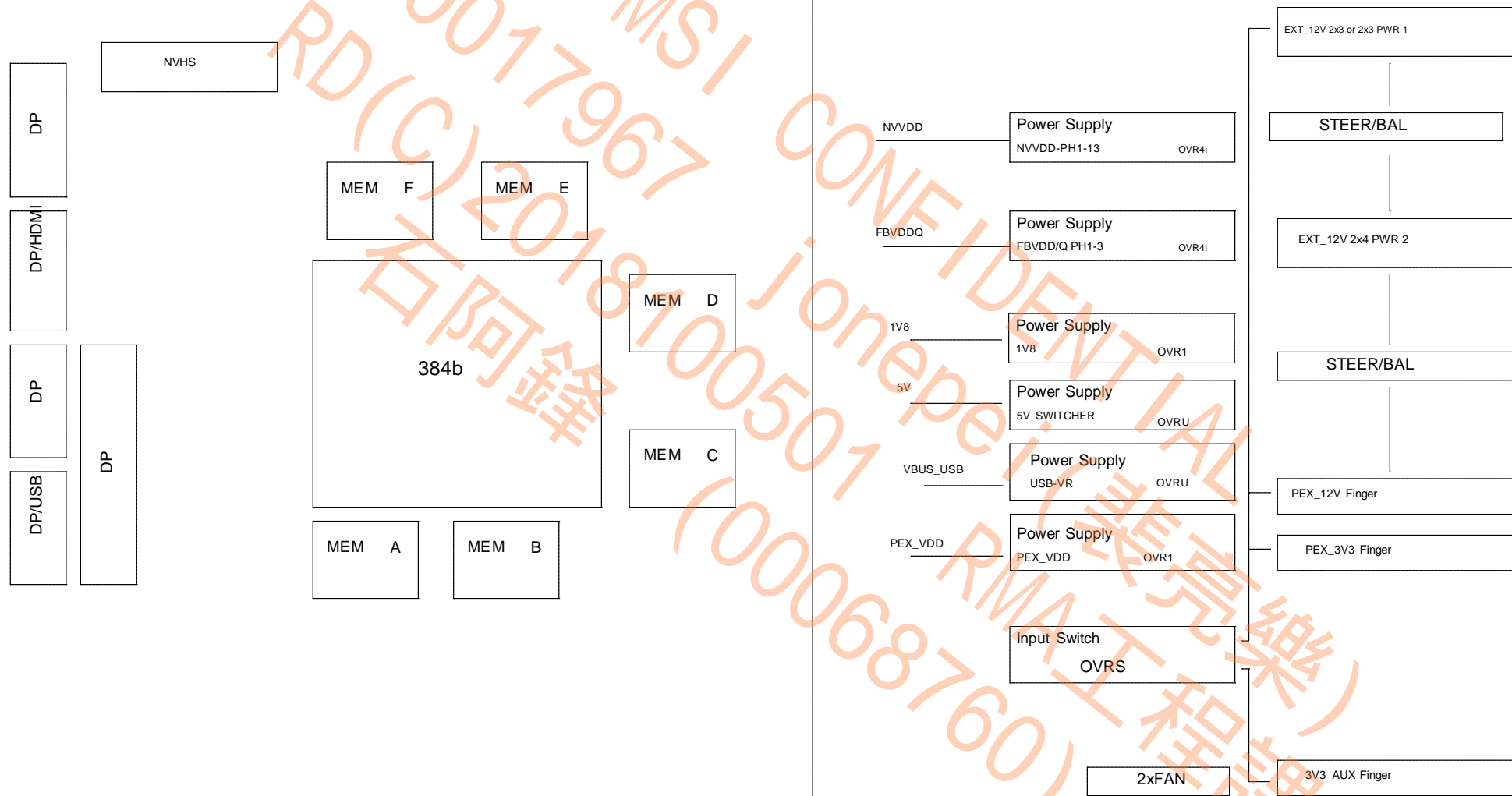
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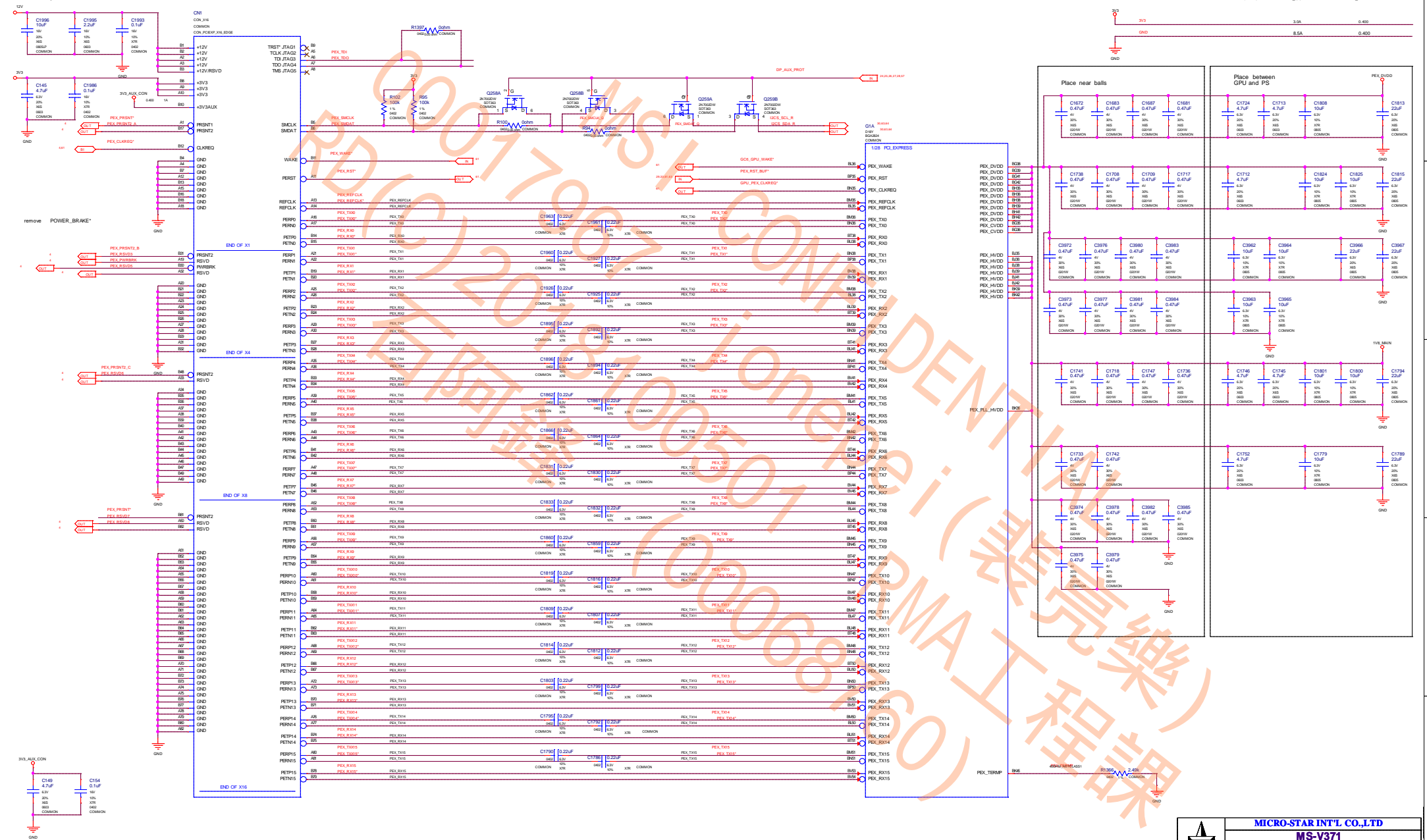
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Block Diagram



PCI Express

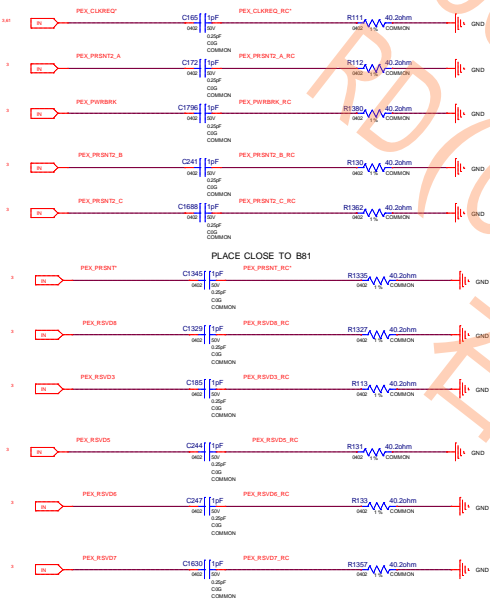


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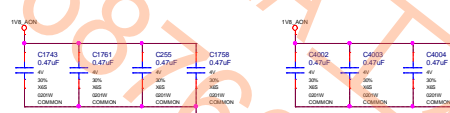
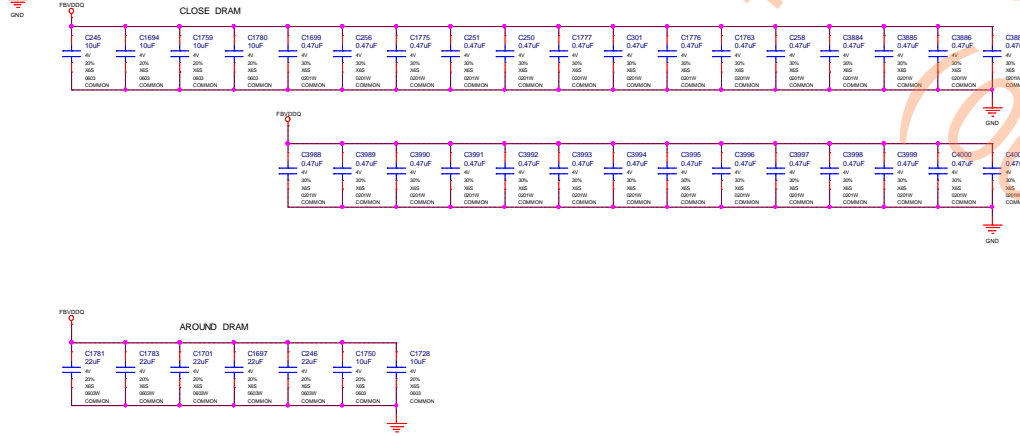
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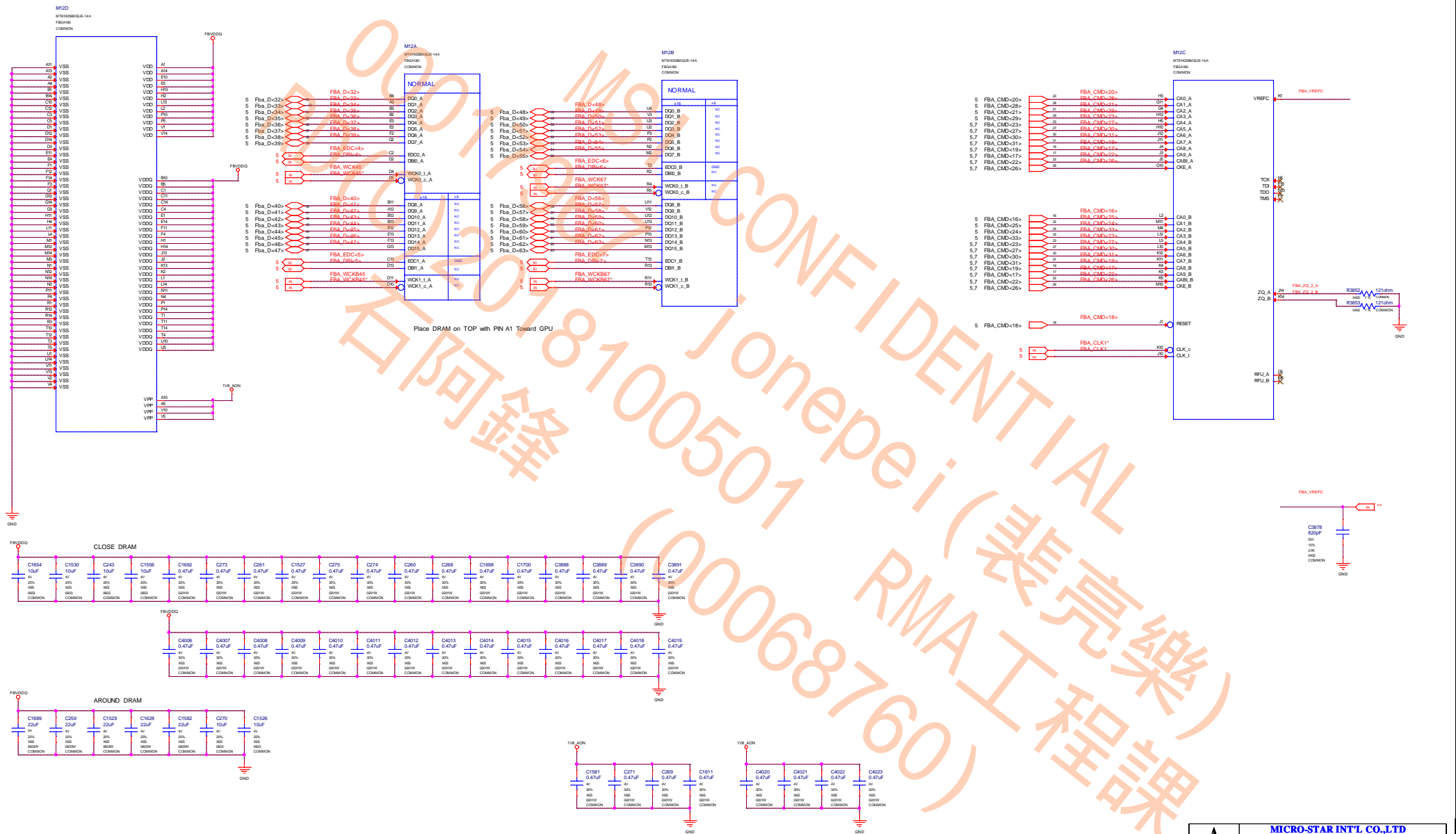
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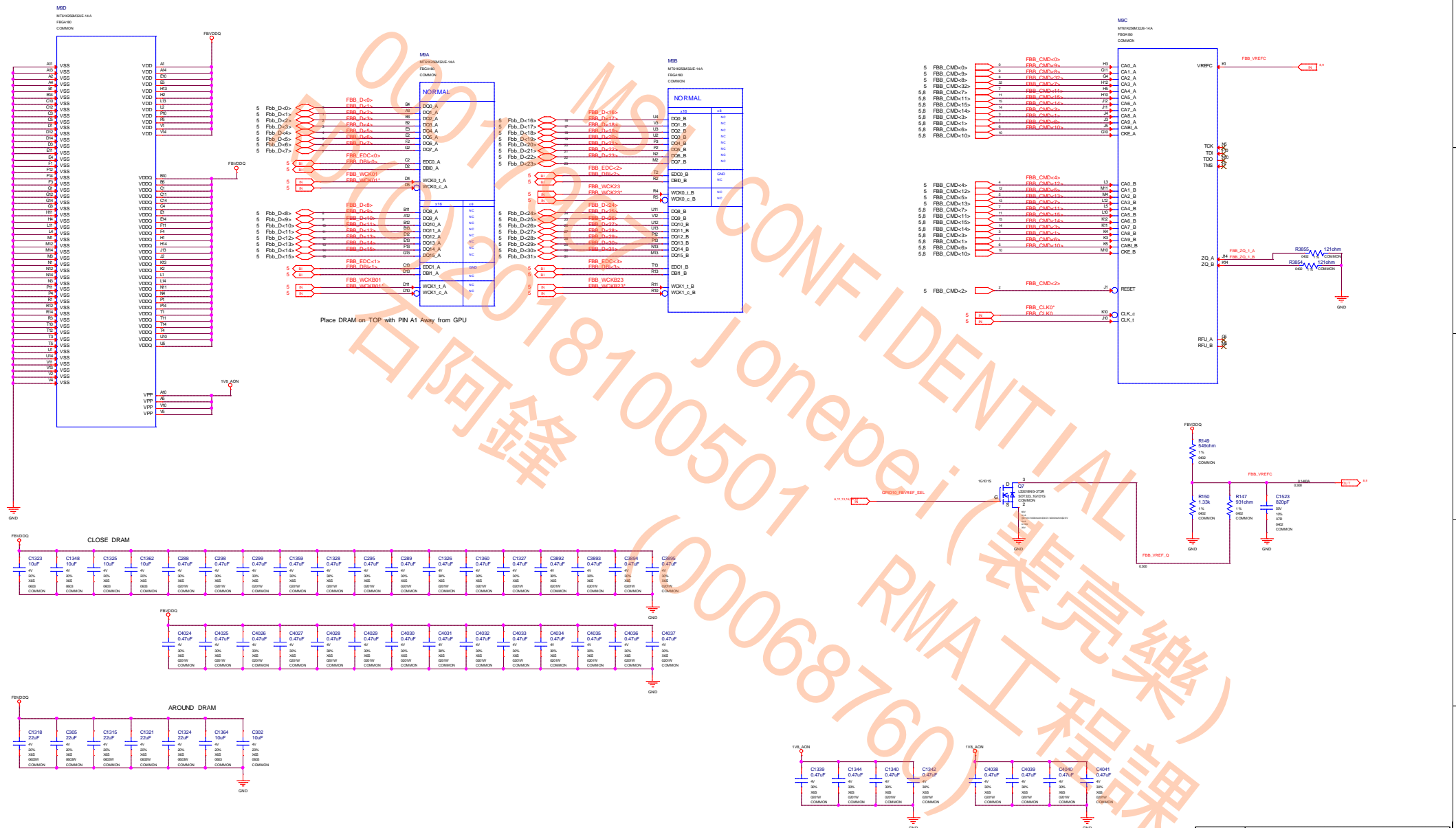


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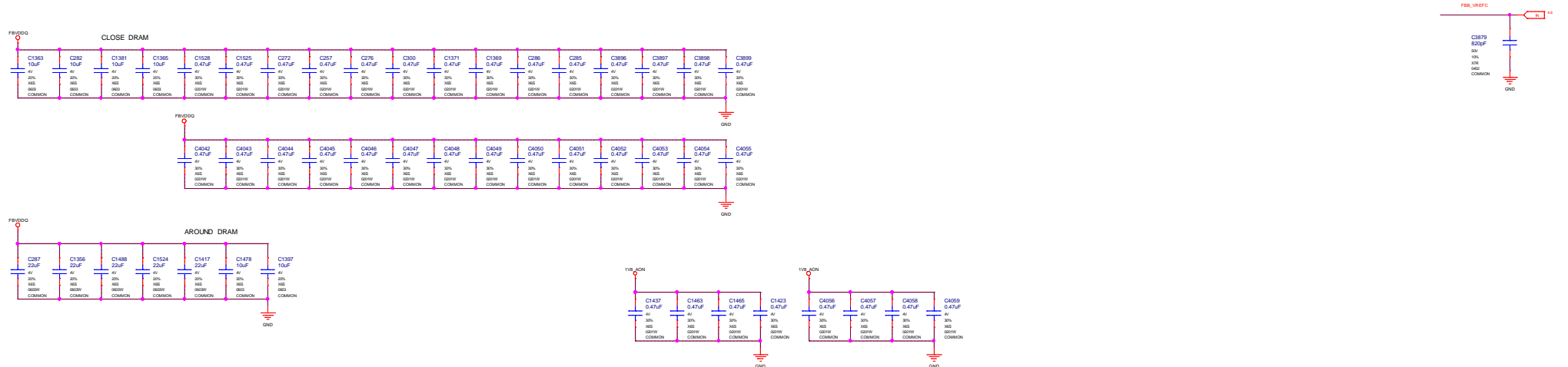
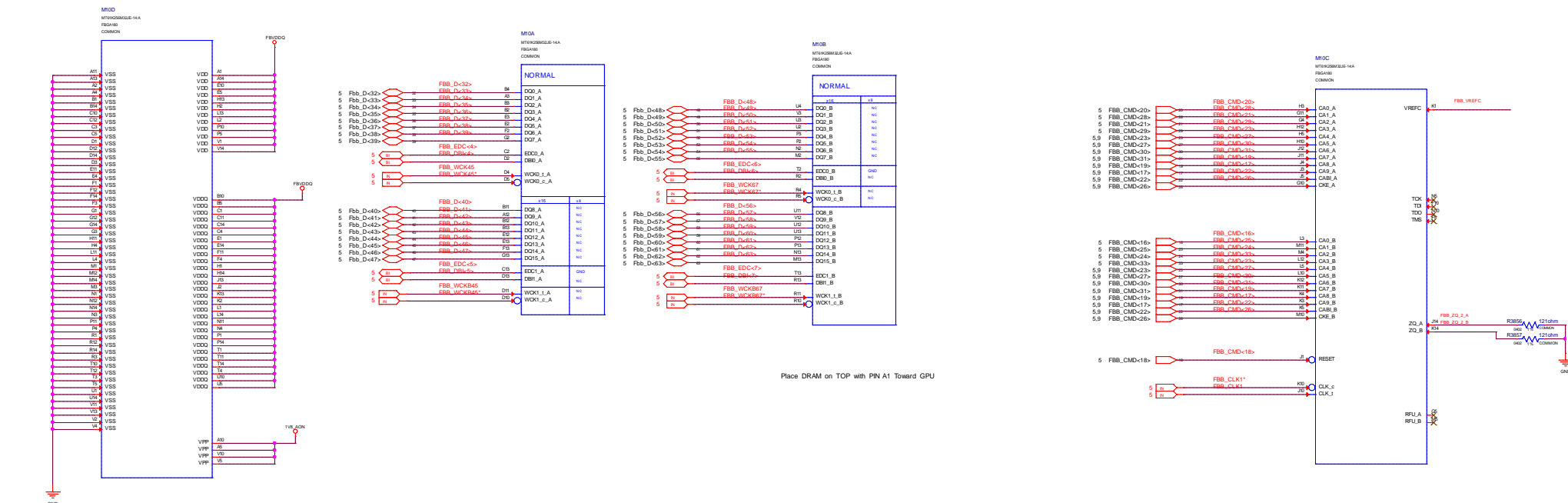
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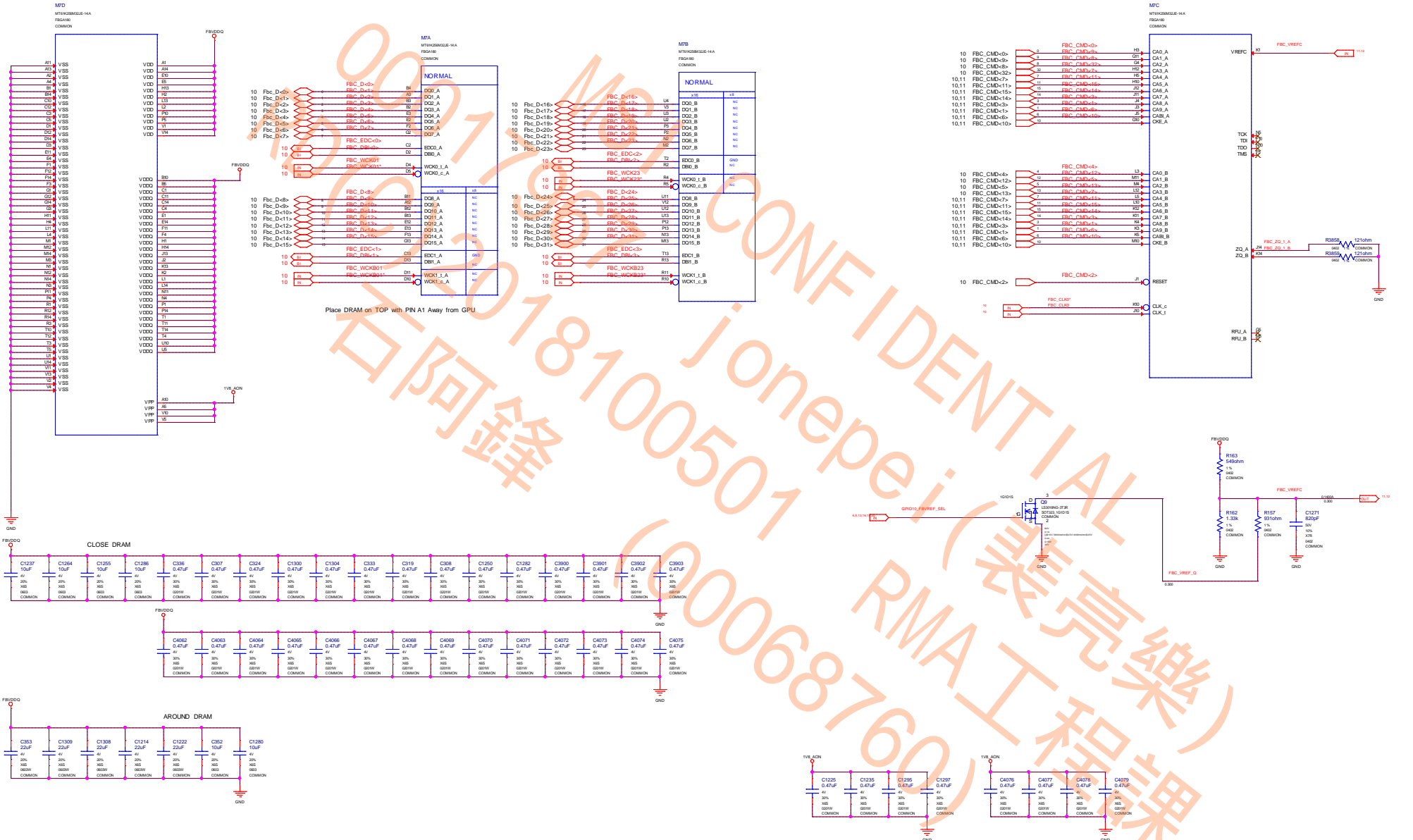


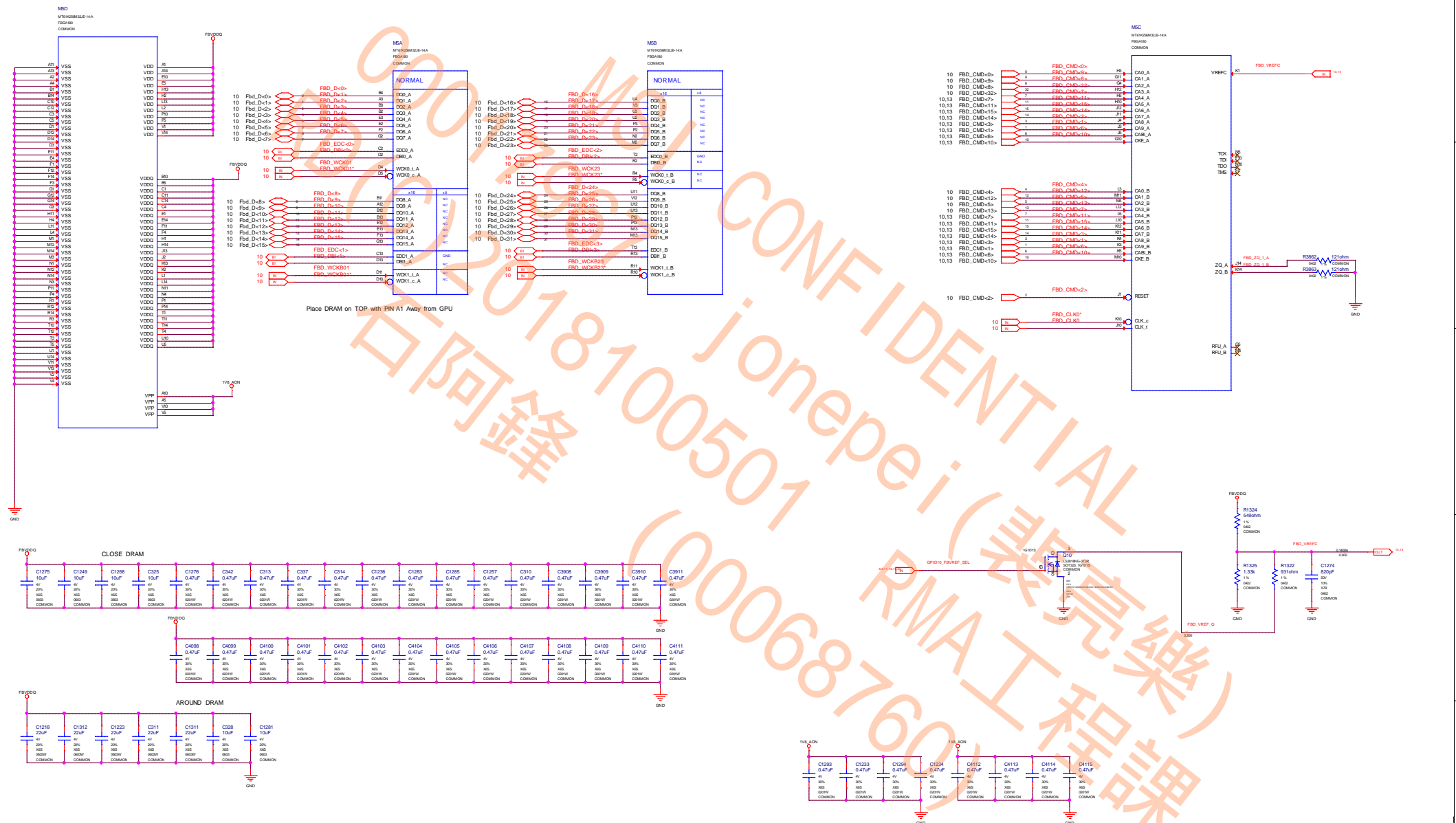
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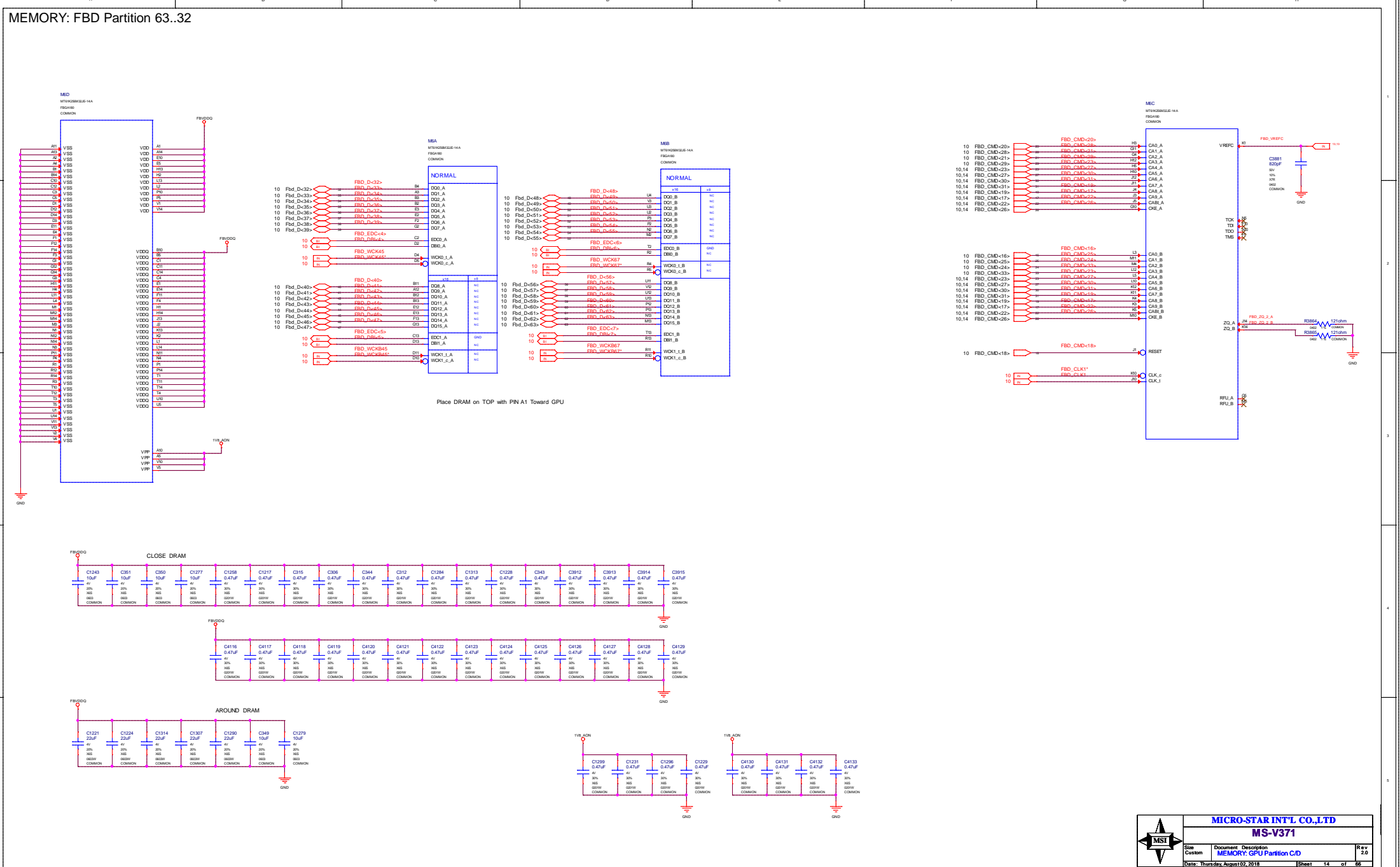




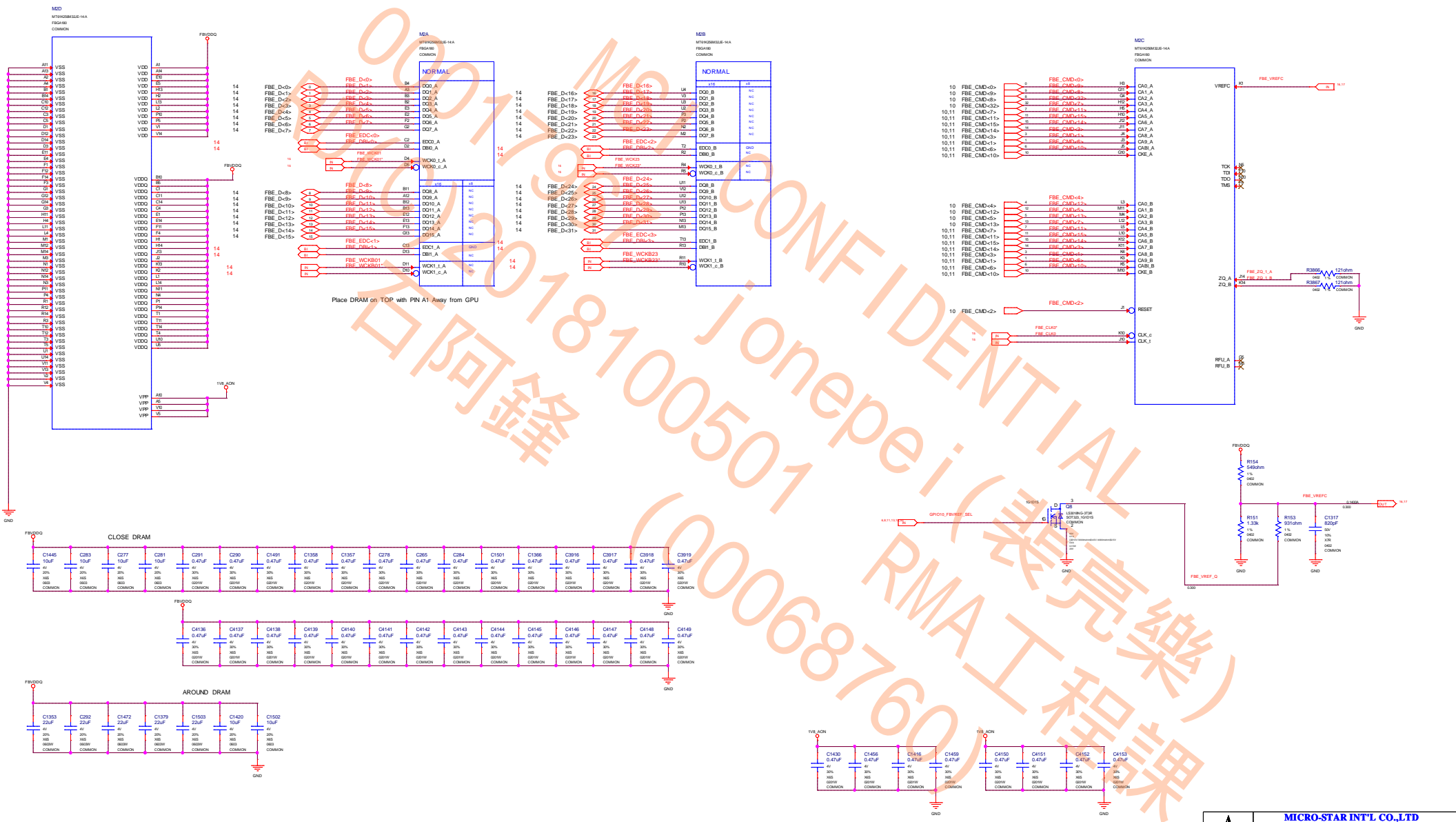
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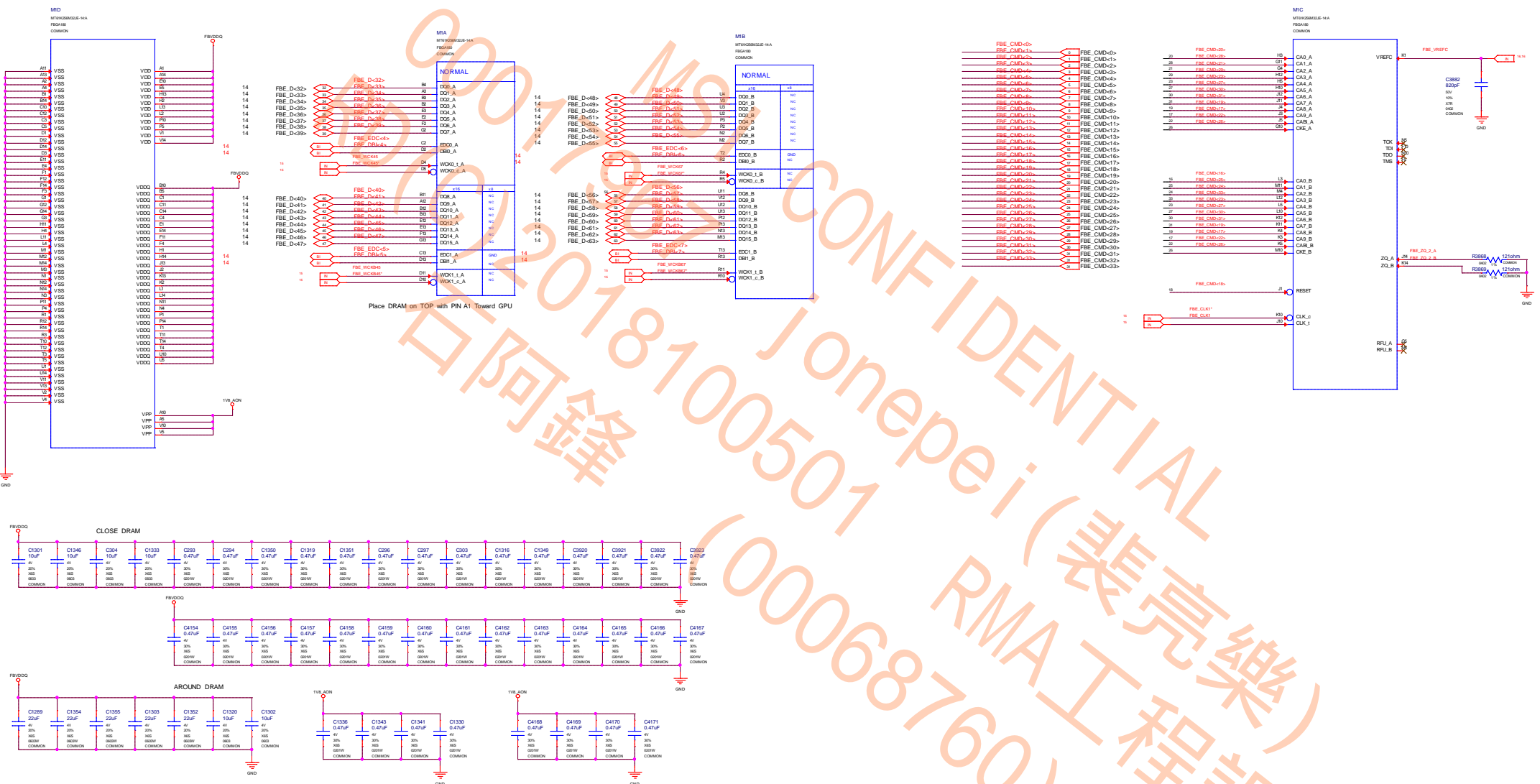


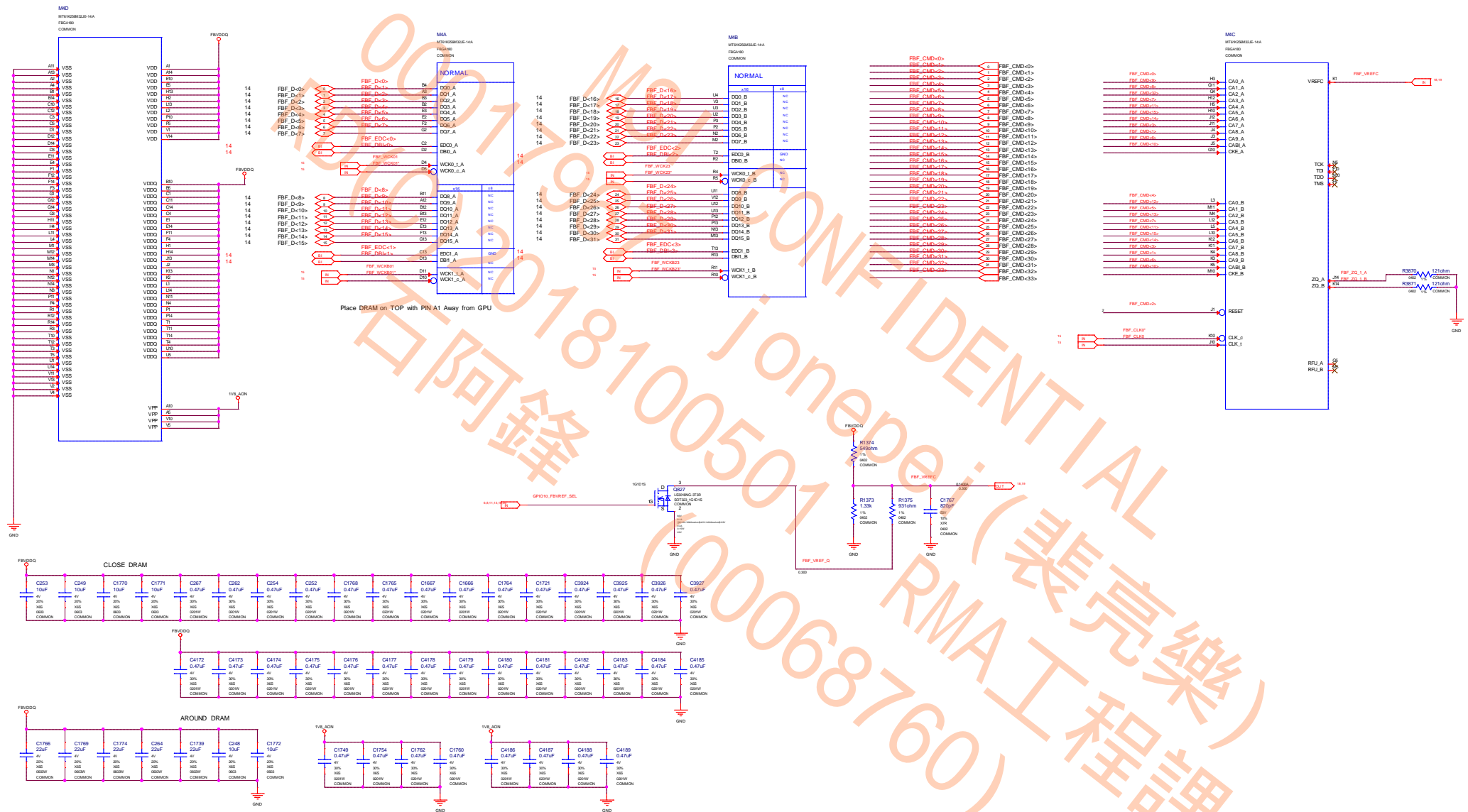


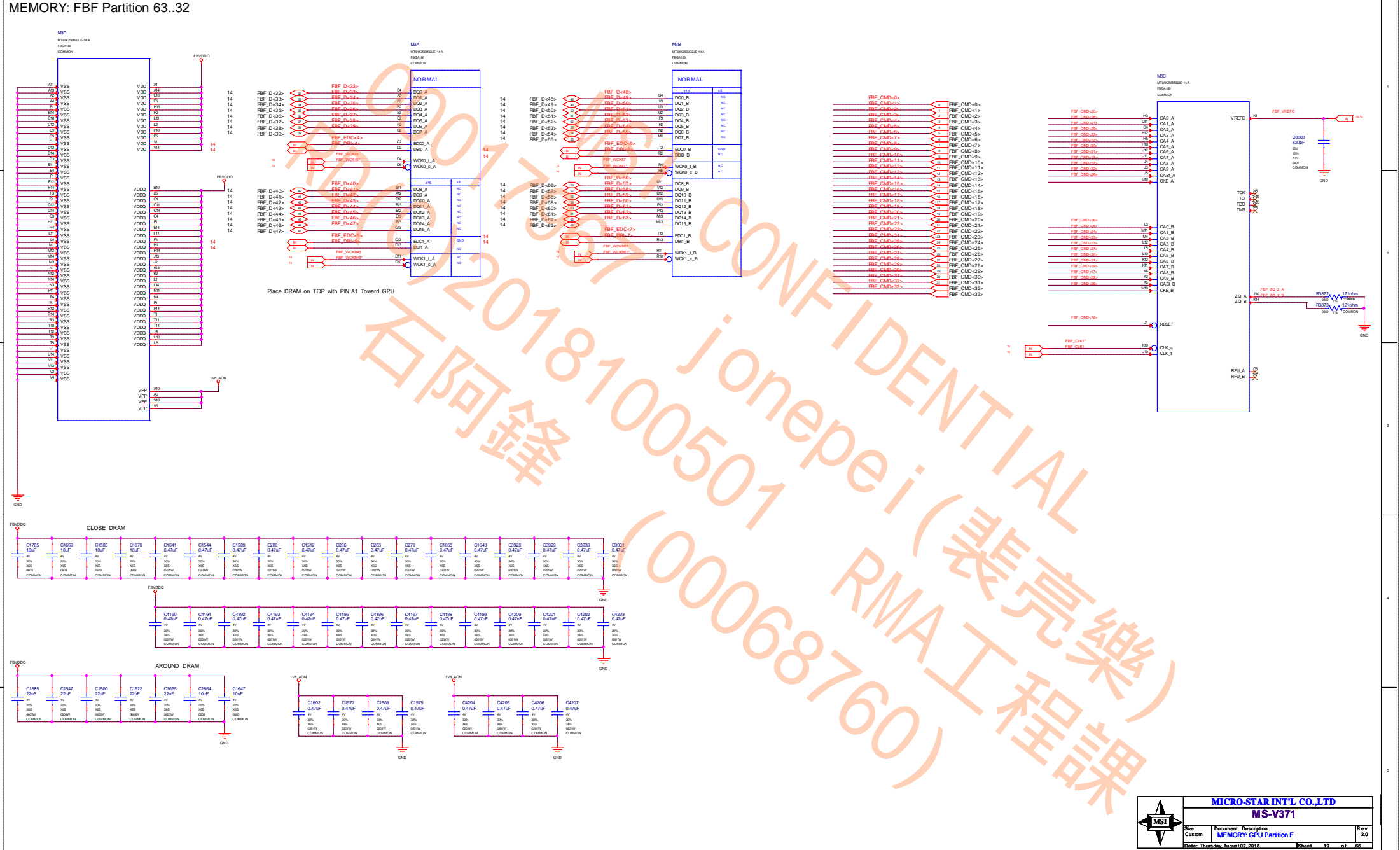




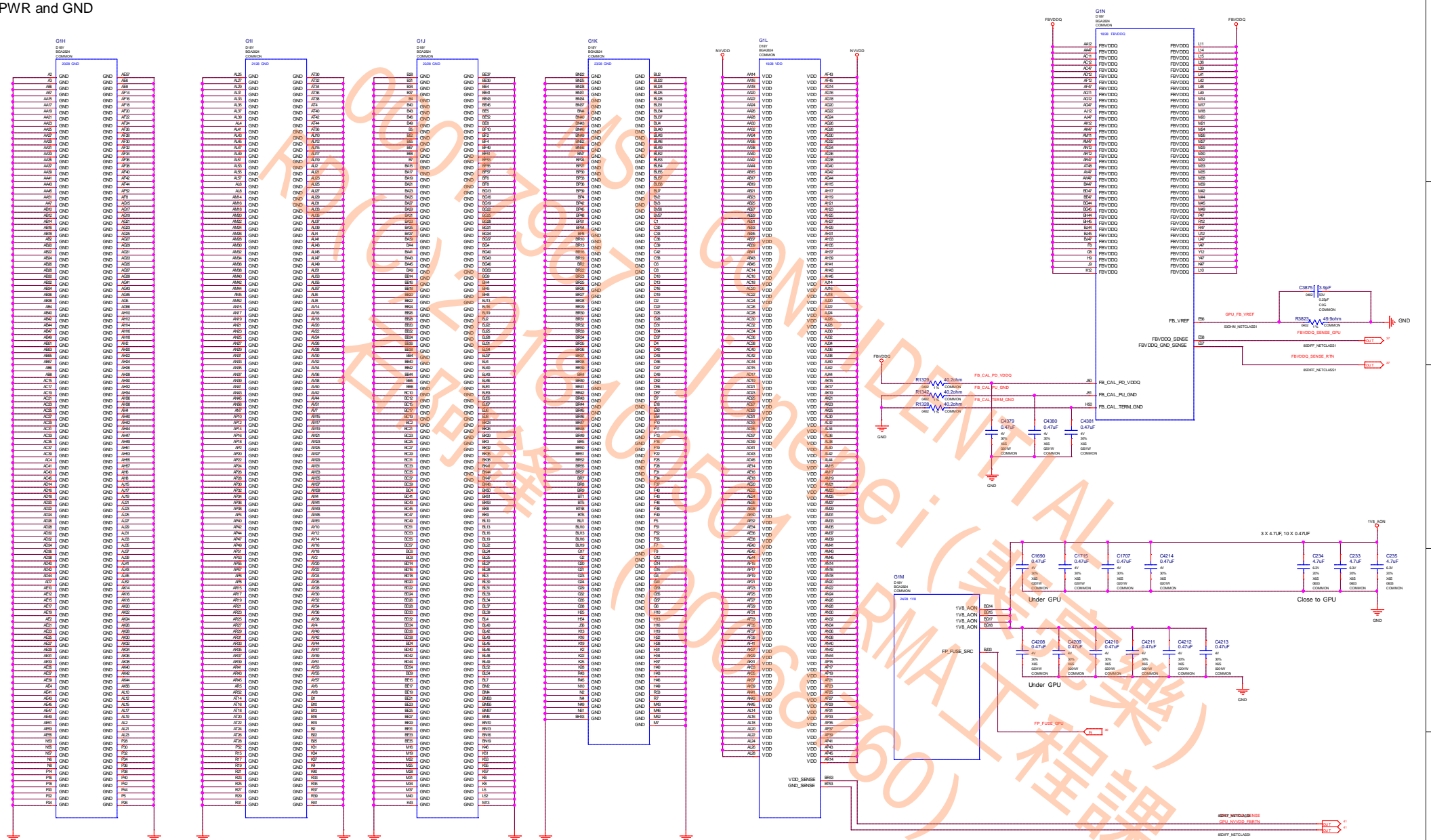




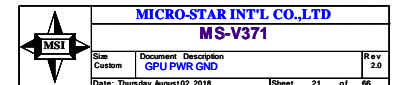
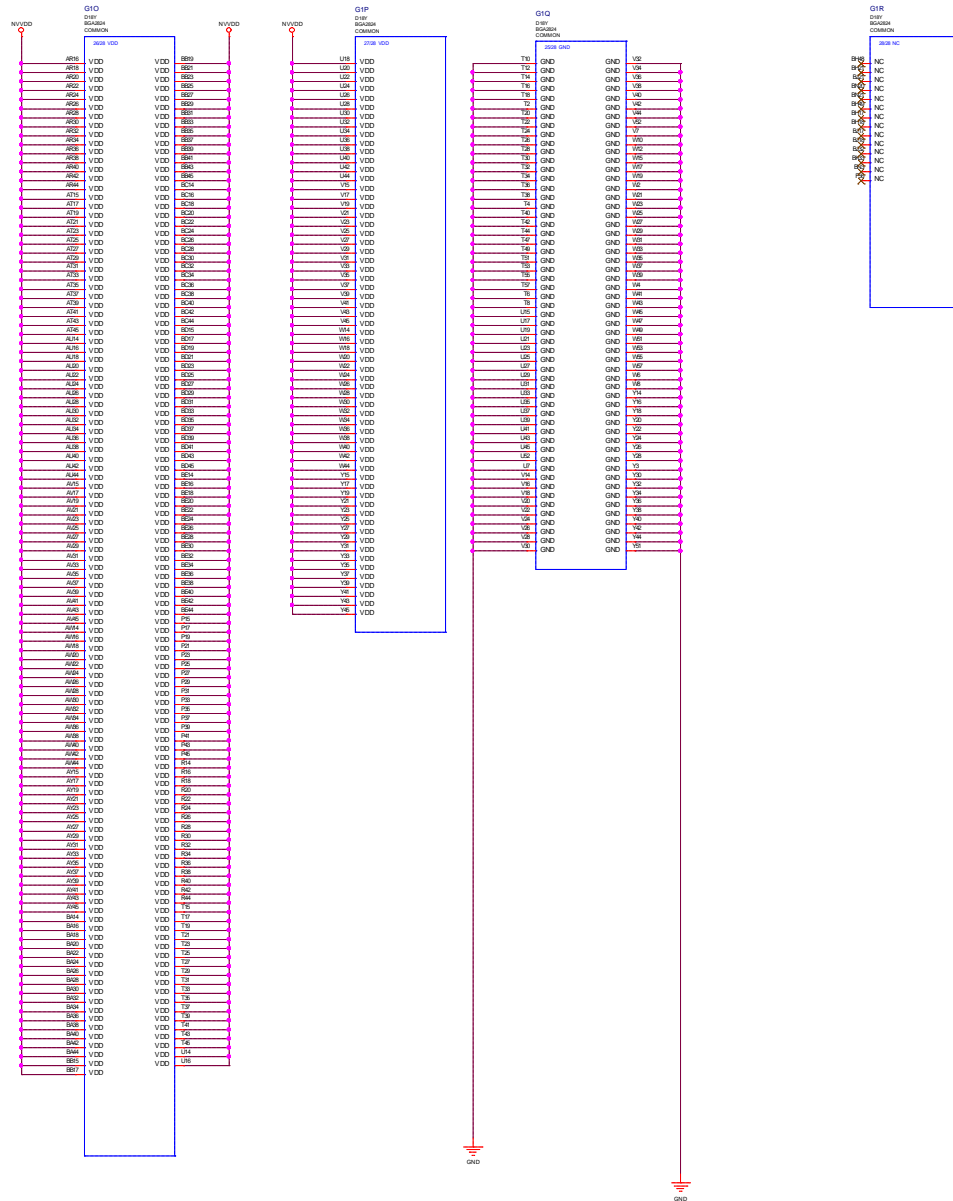




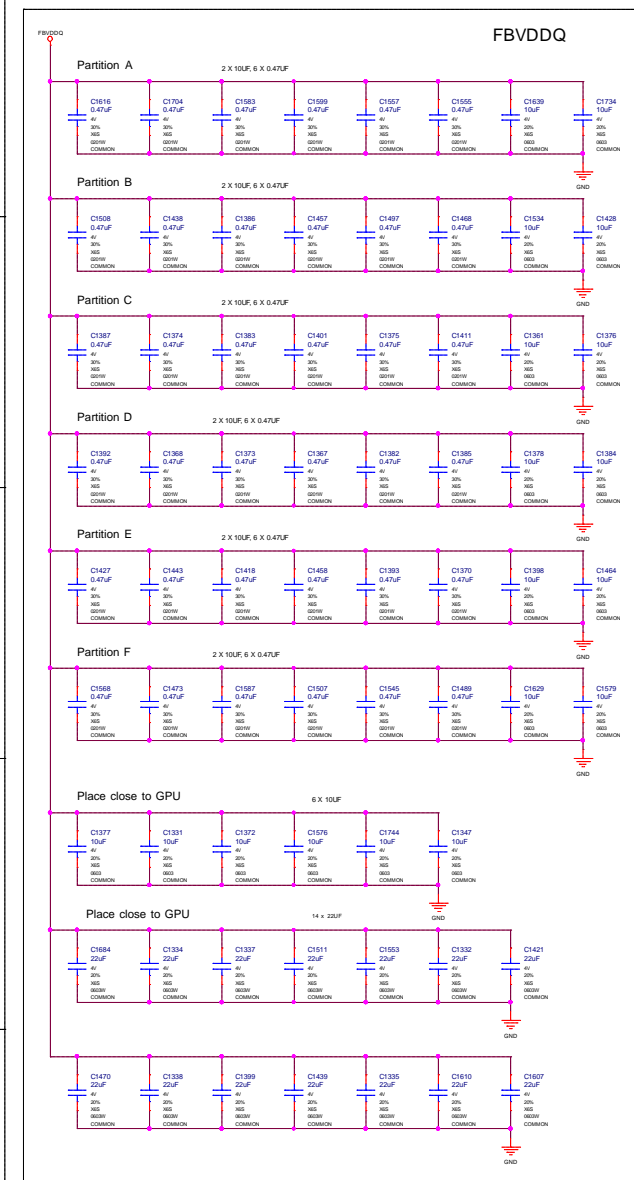
GPU PWR and GND



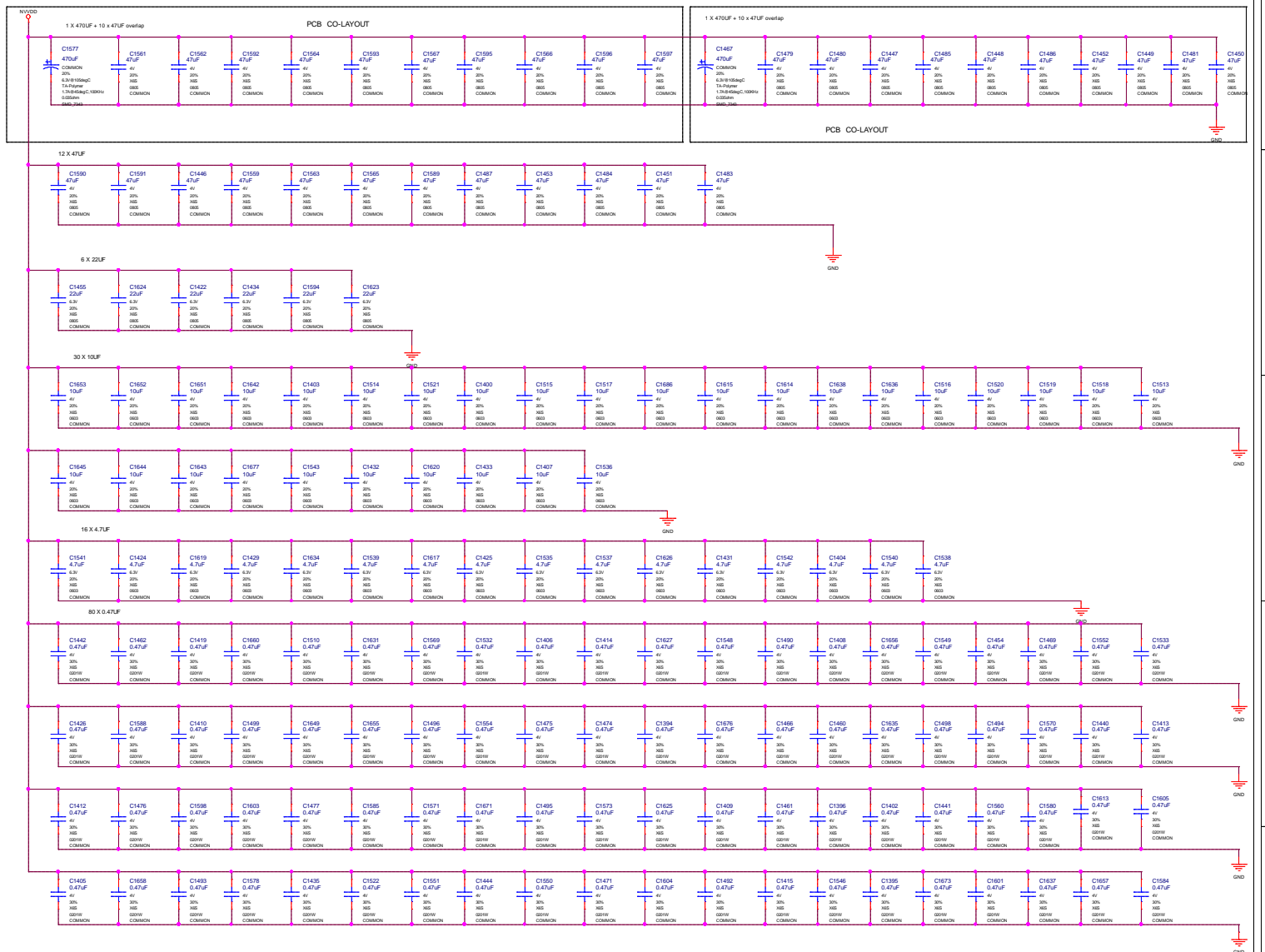
GPU PWR GND NCs



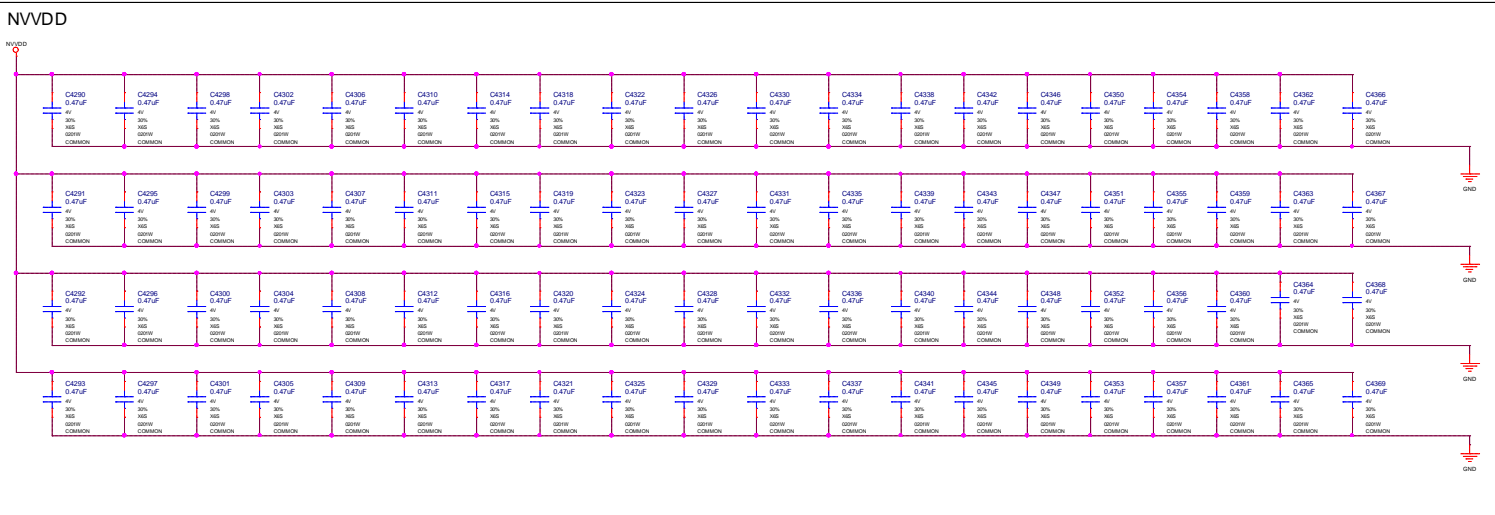
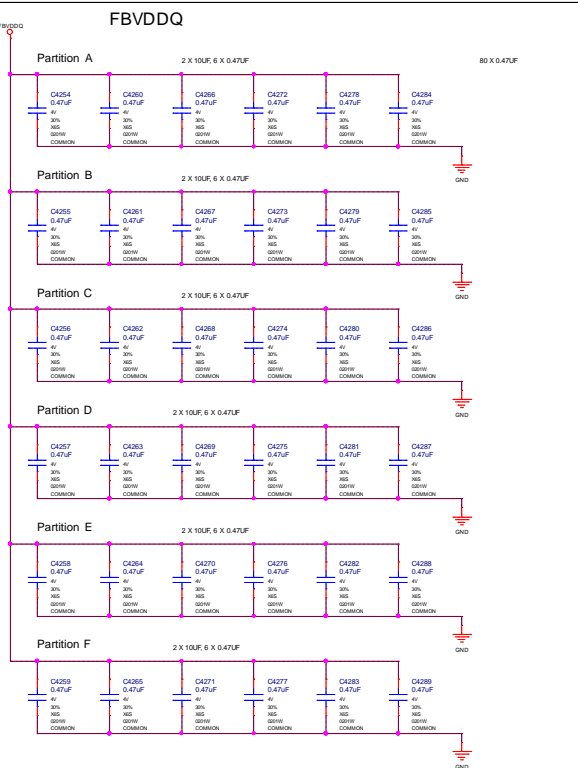
GPU Decoupling




NVVDD



GPU Decoupling





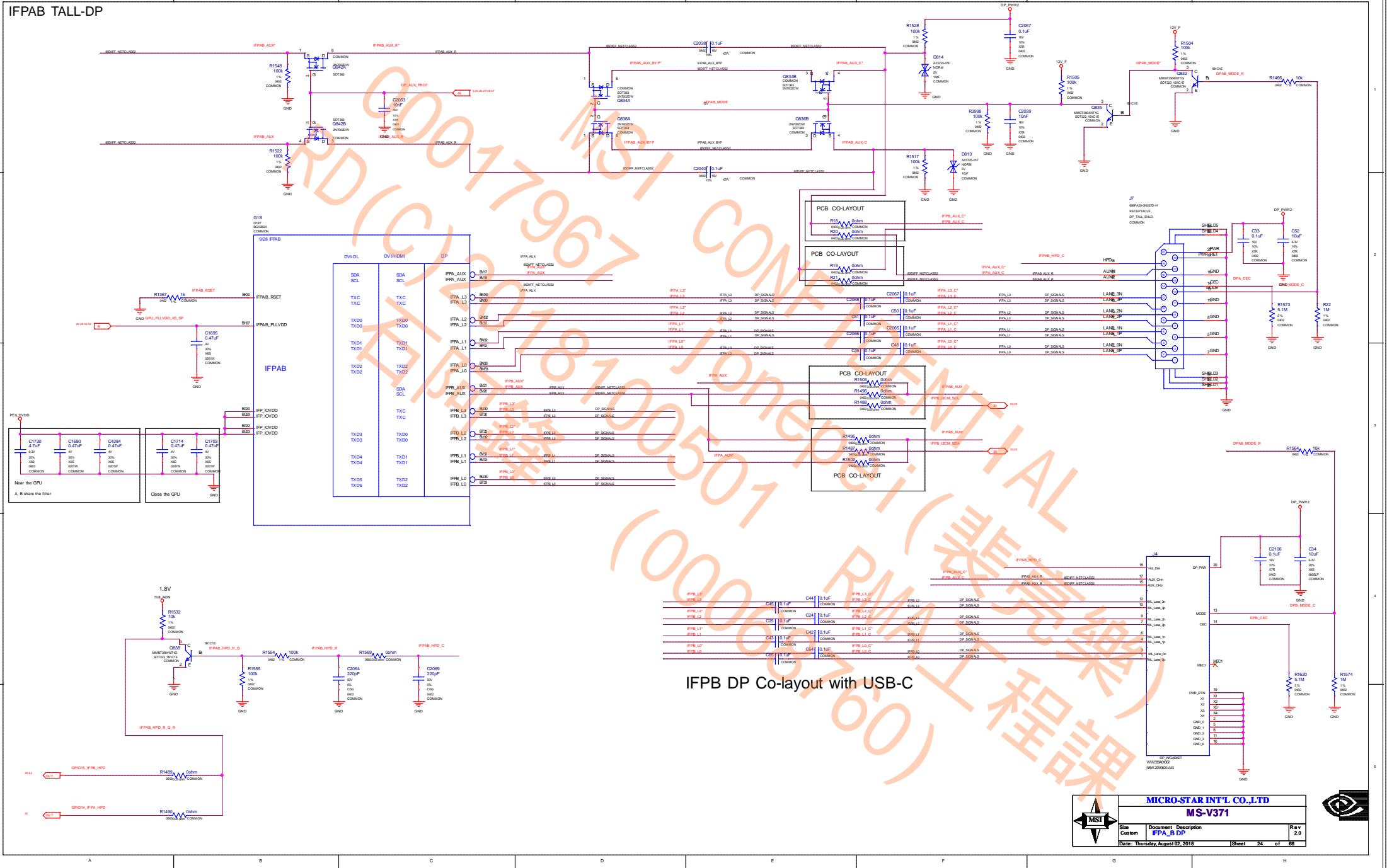
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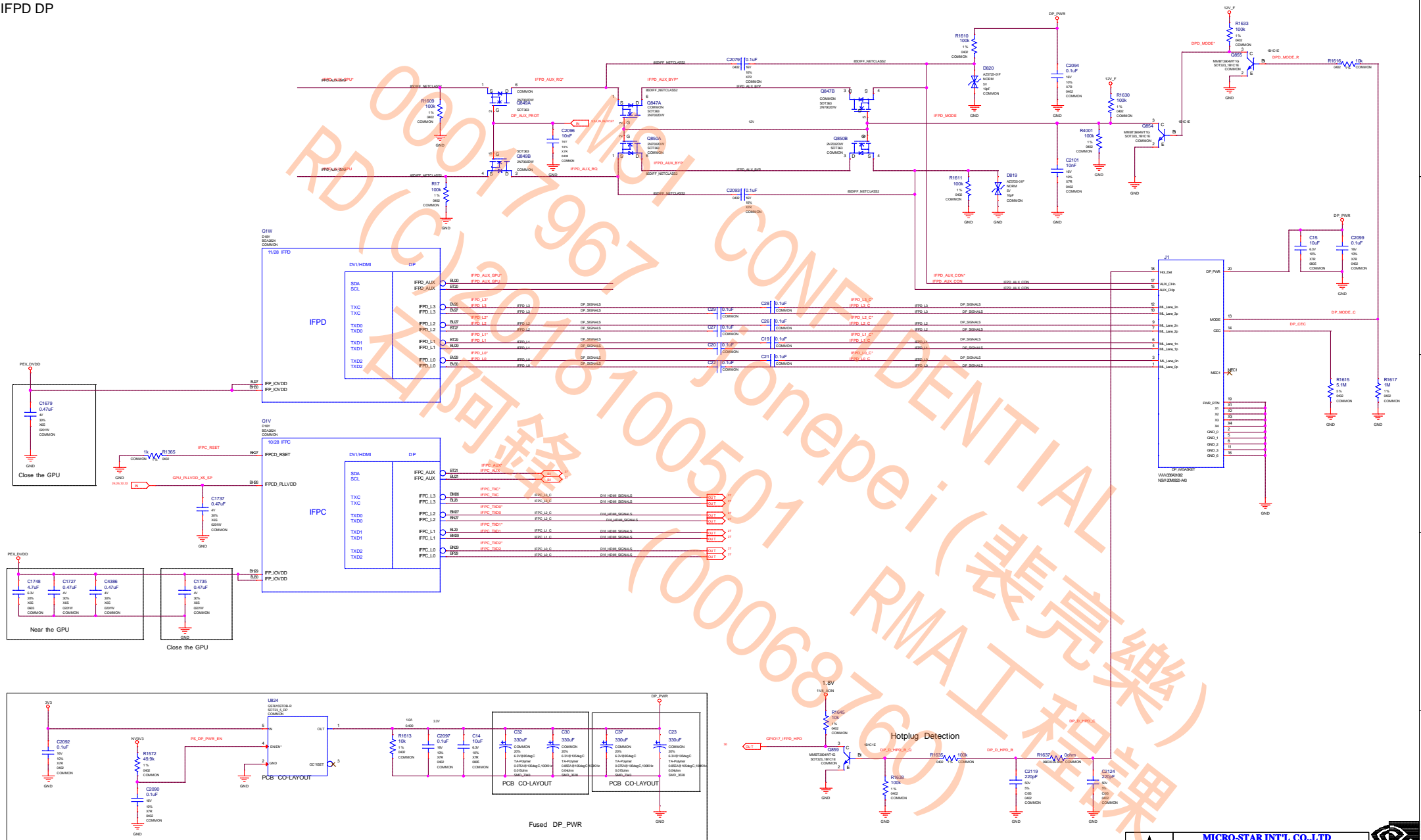
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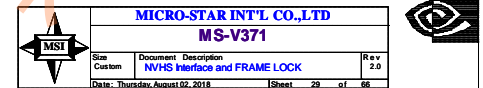


IFPAB TALL-DP

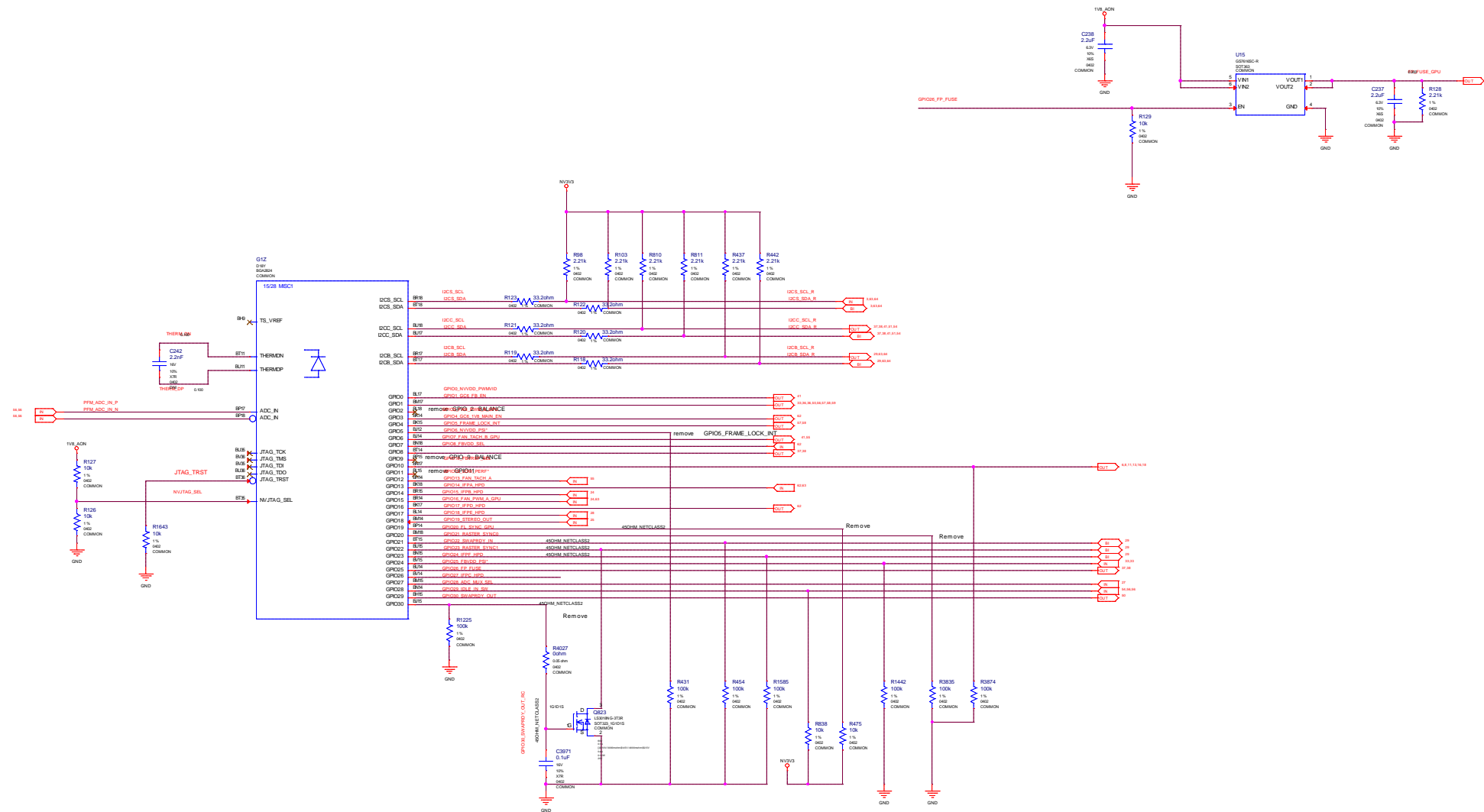




NVHS Interface and FRAME LOCK



MISC1: Fan, Thermal, JTAG, GPIO, STEREO



MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
H	L	H	00101
H	H	L	00110
H	H	H	00111
L	L	M	01000
L	M	L	01001

DEFAULT

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

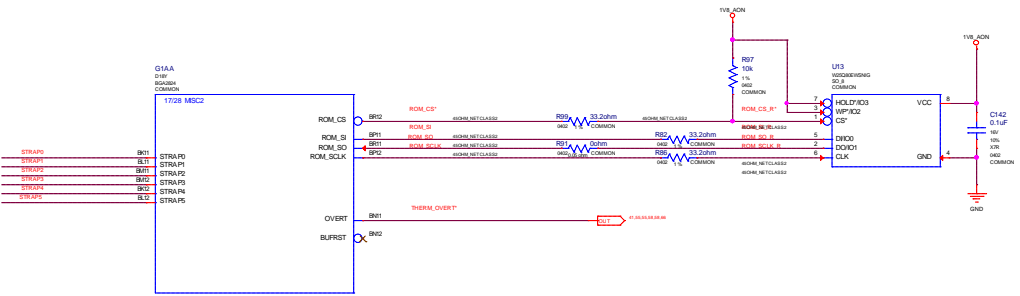
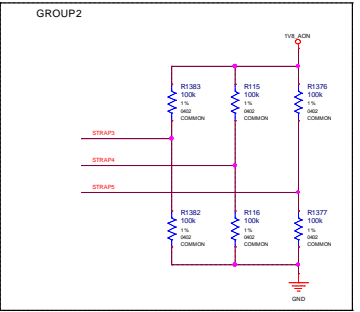
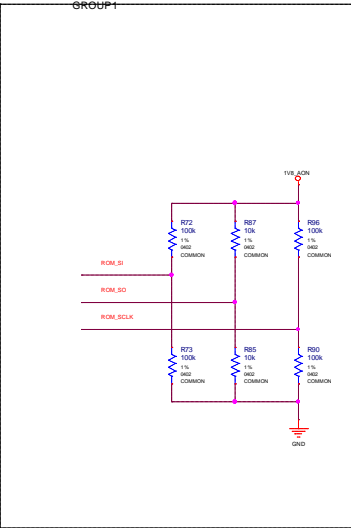
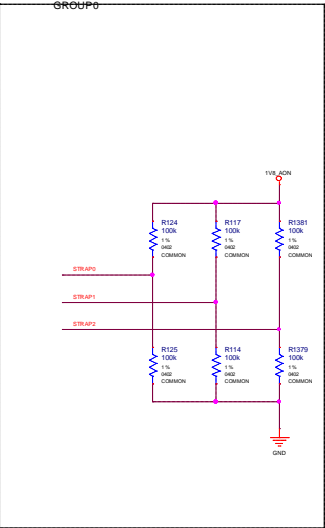
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	H	XXX0	FS_OVERT DISABLE


DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

SKU 200






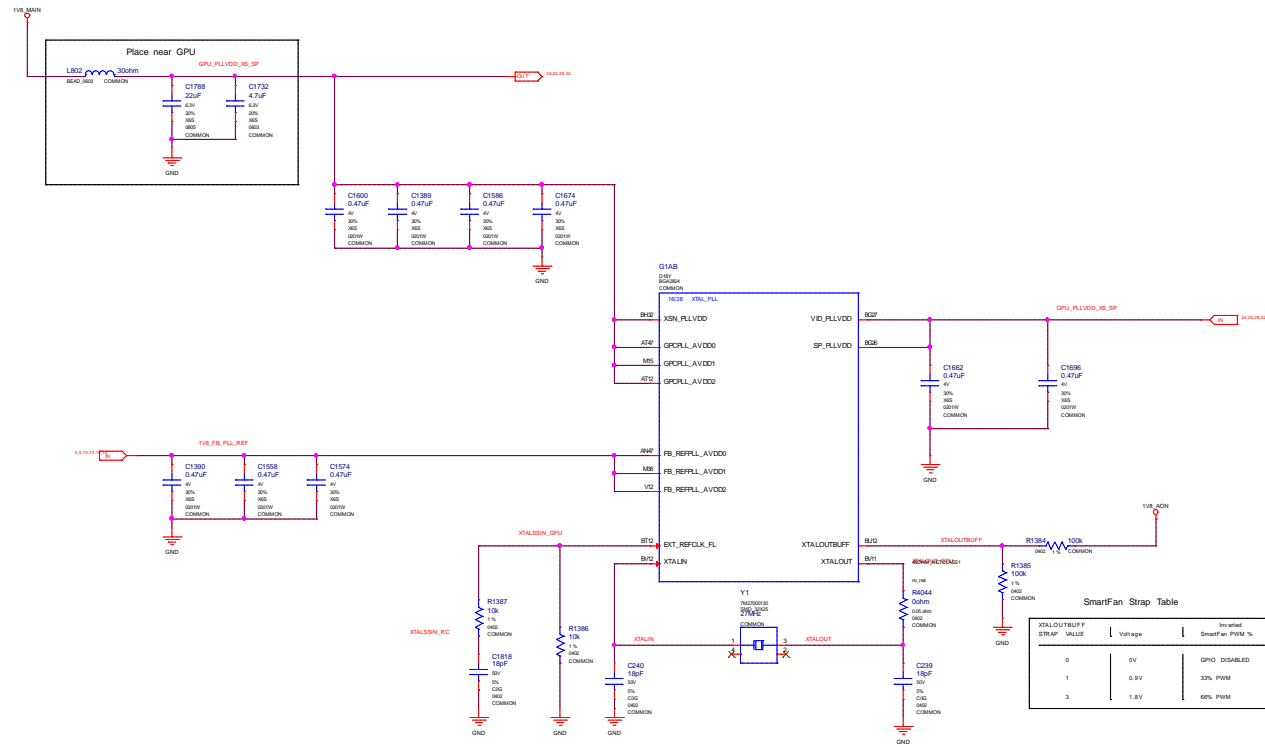
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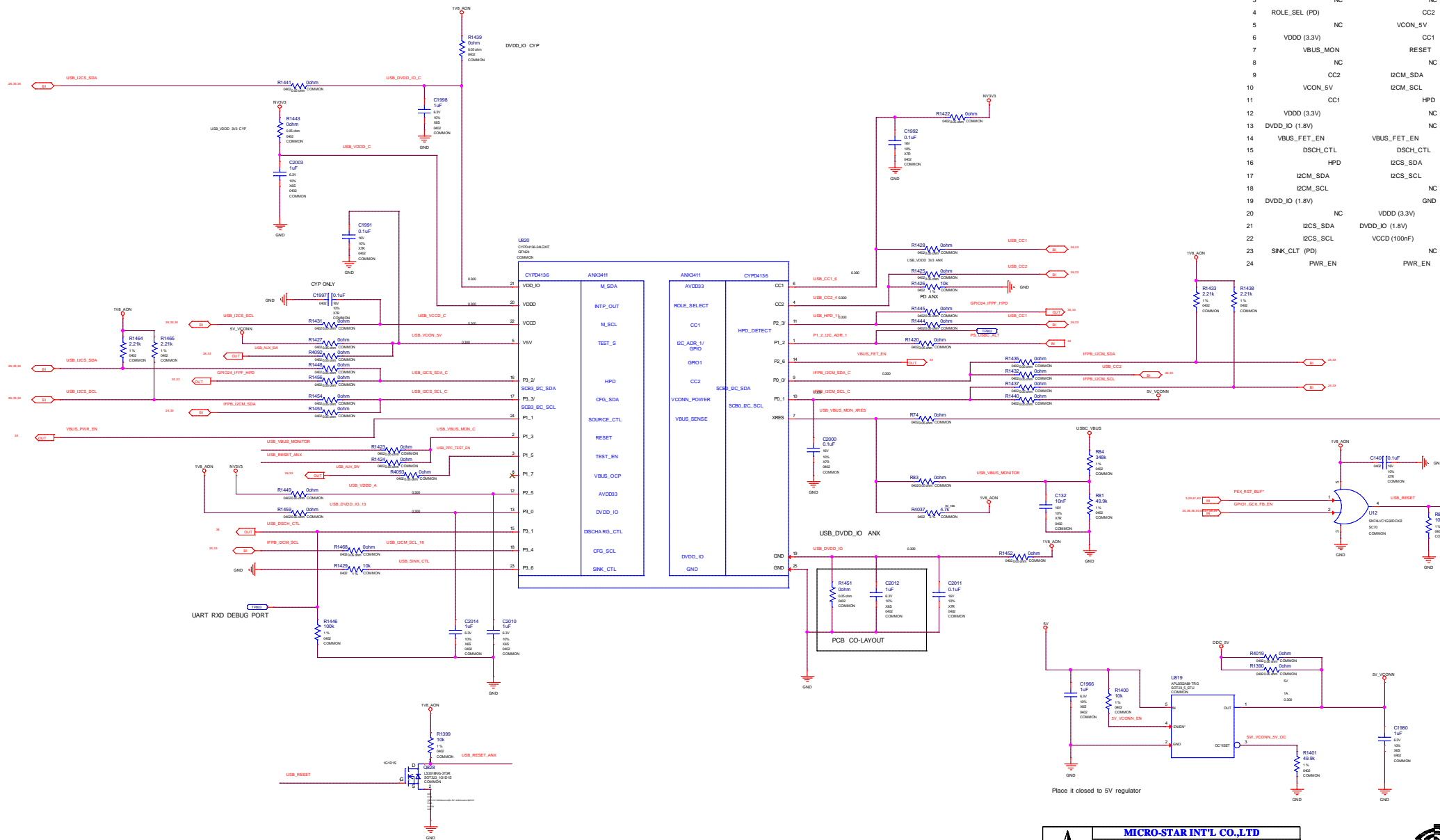
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MISC: USB PPC



PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	
4	ROLE_SEL (PD)	NC
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CS_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100mF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN

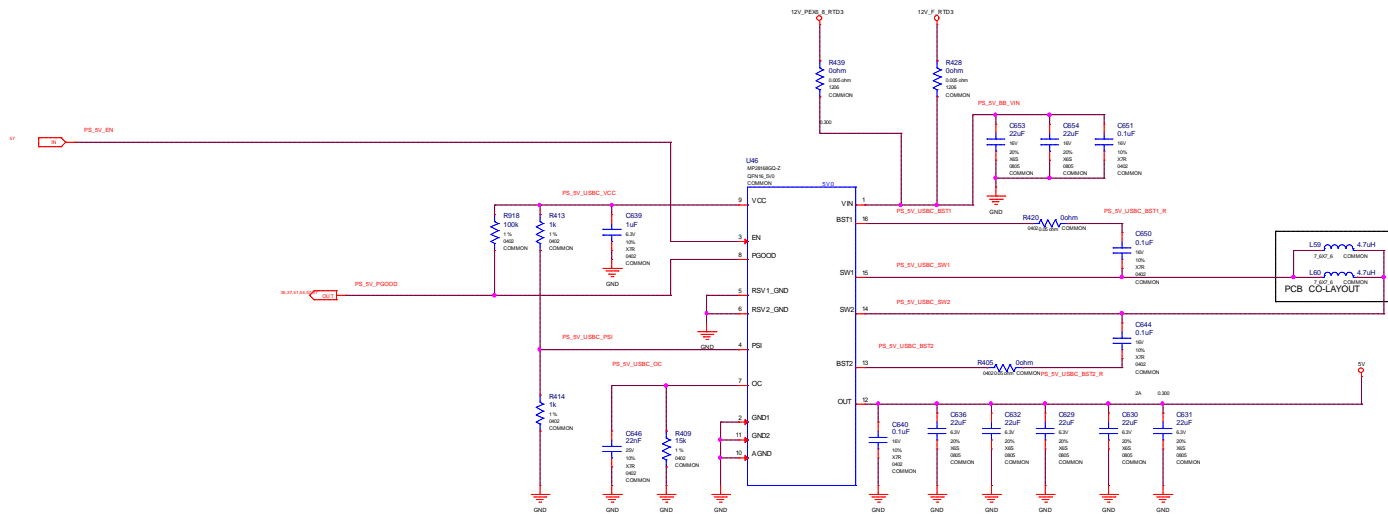


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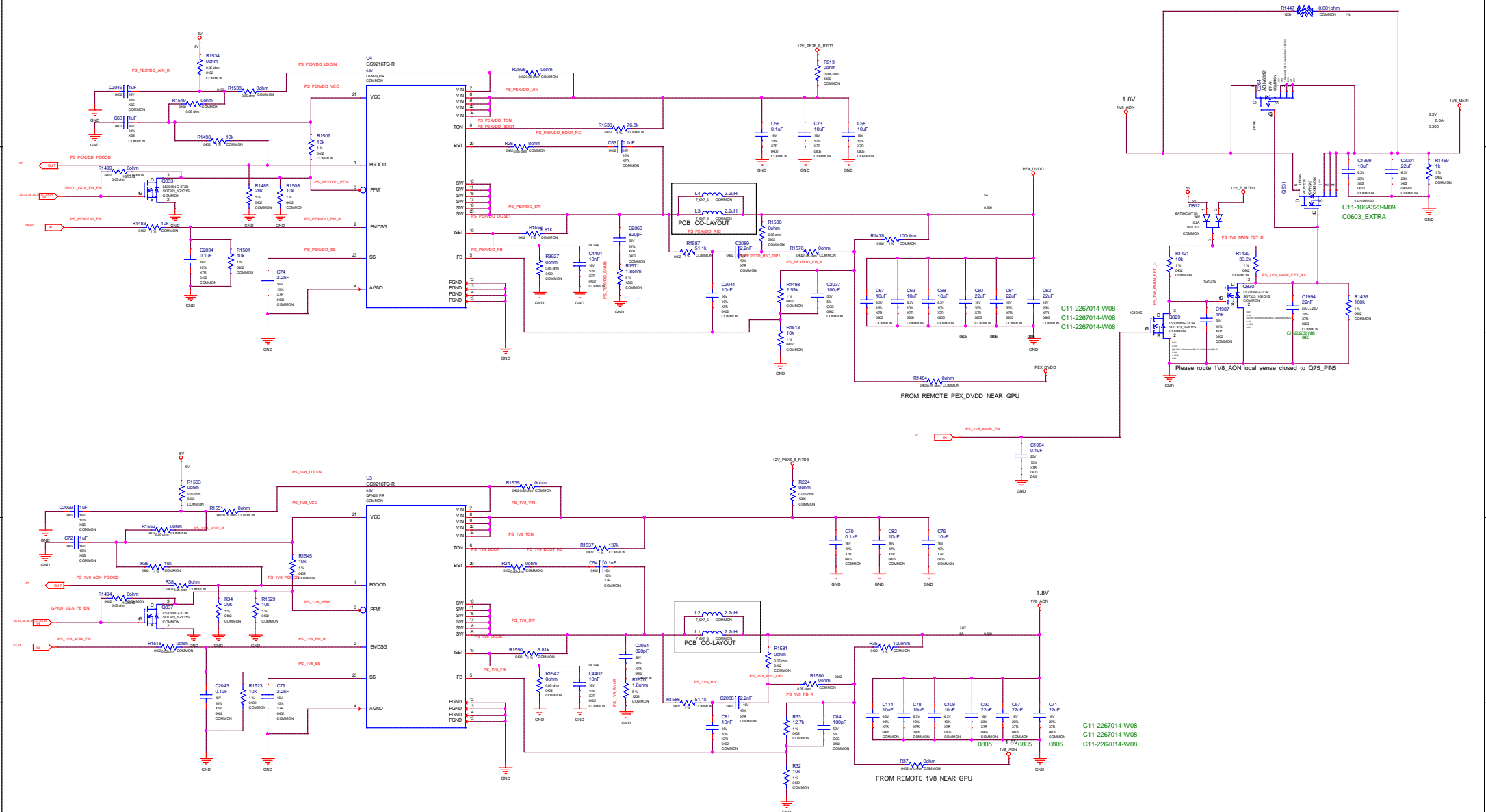
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PS: 5V, 5V_BACKUP



PS: PEXVDD 1V8 Rail



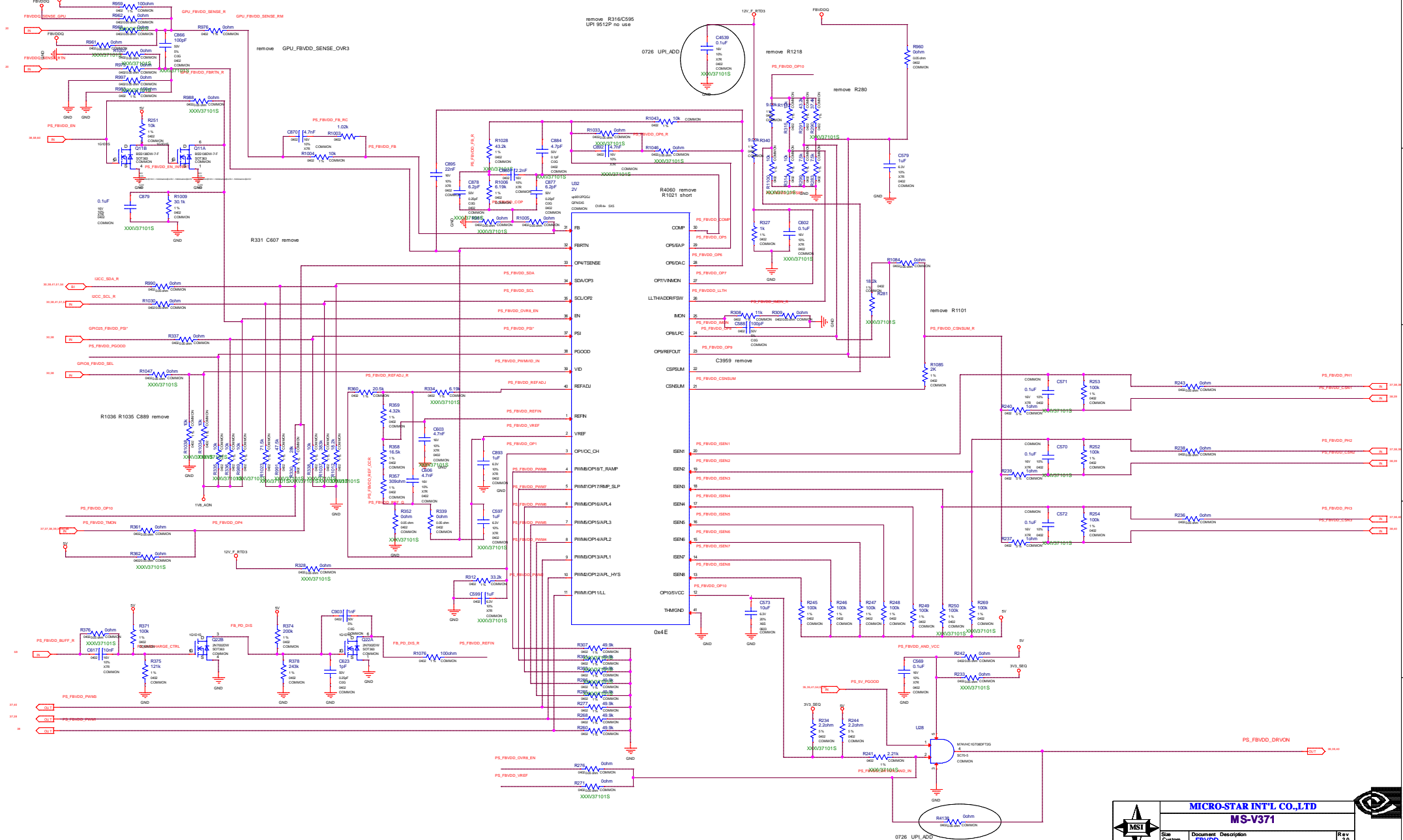
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PS: FBVDD Controller





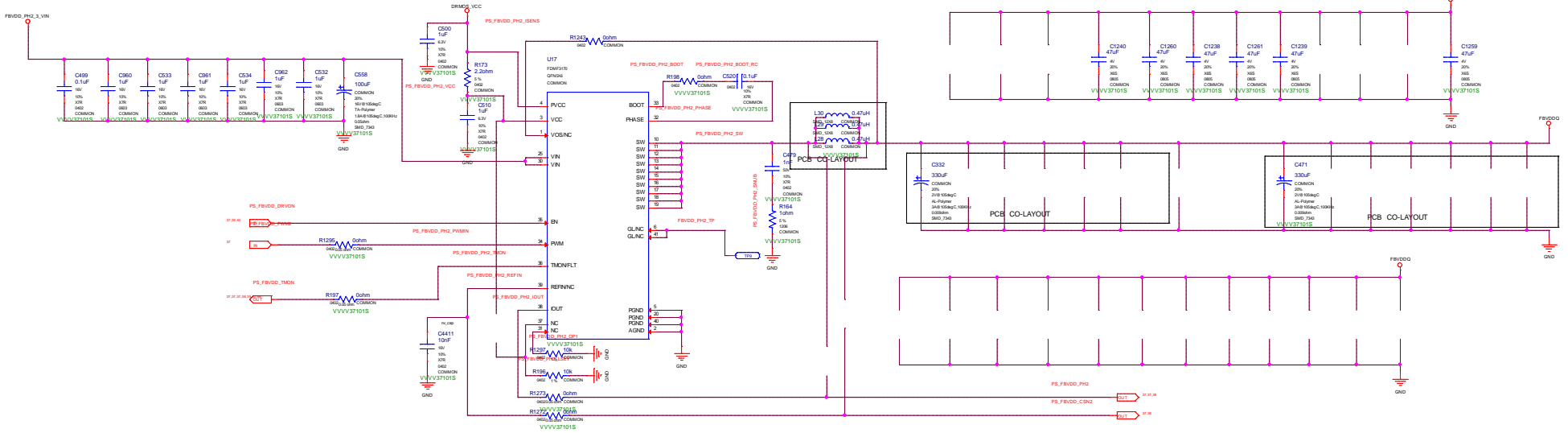
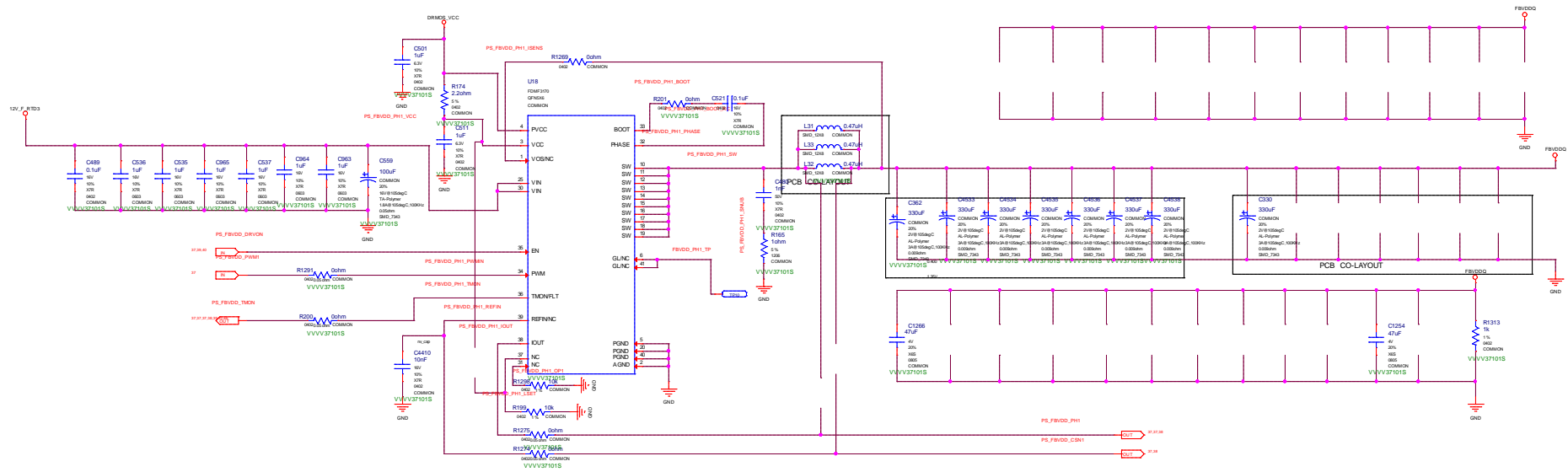
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PS: FBVDD Controller OVR3

remove FBVDDQ

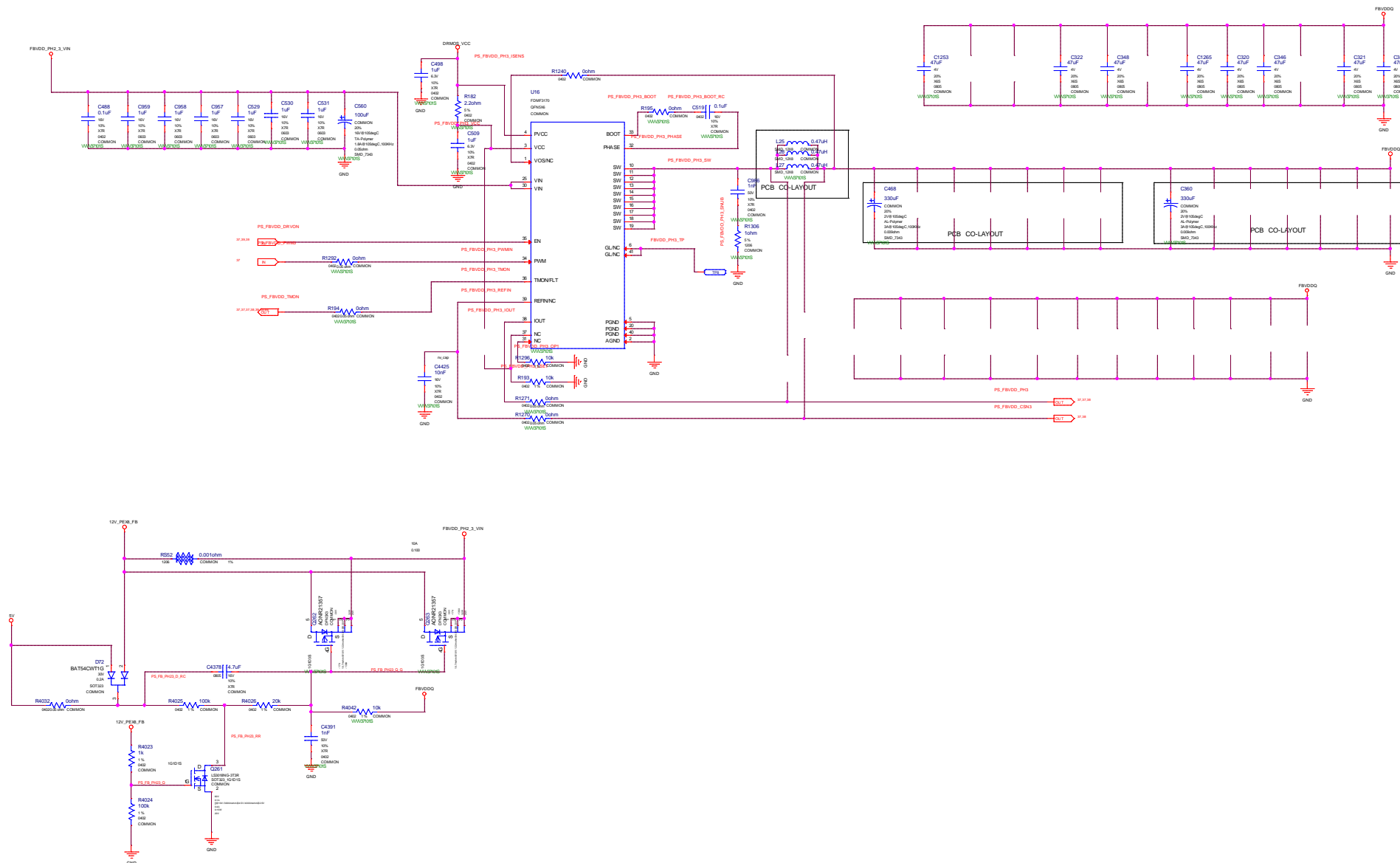
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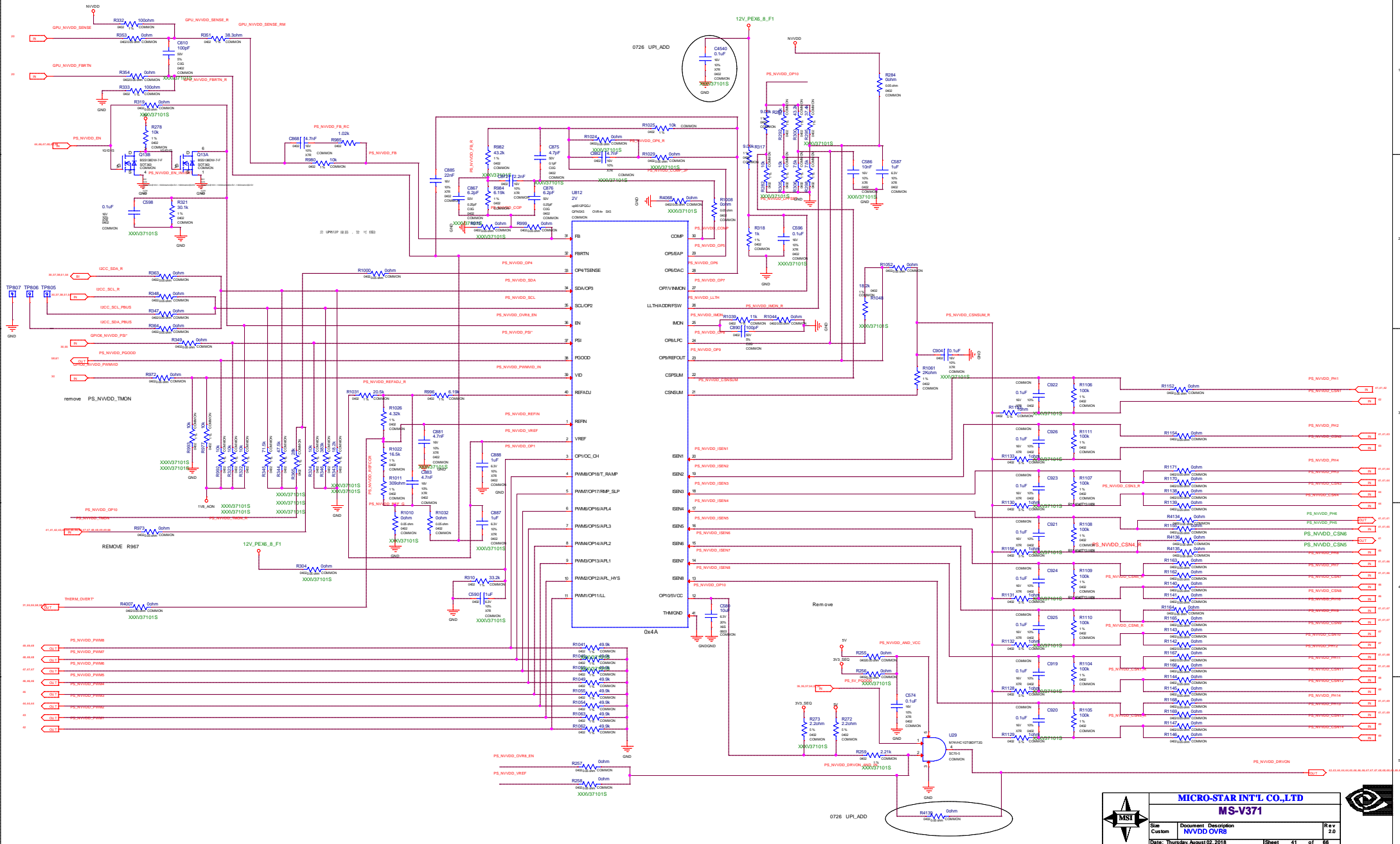
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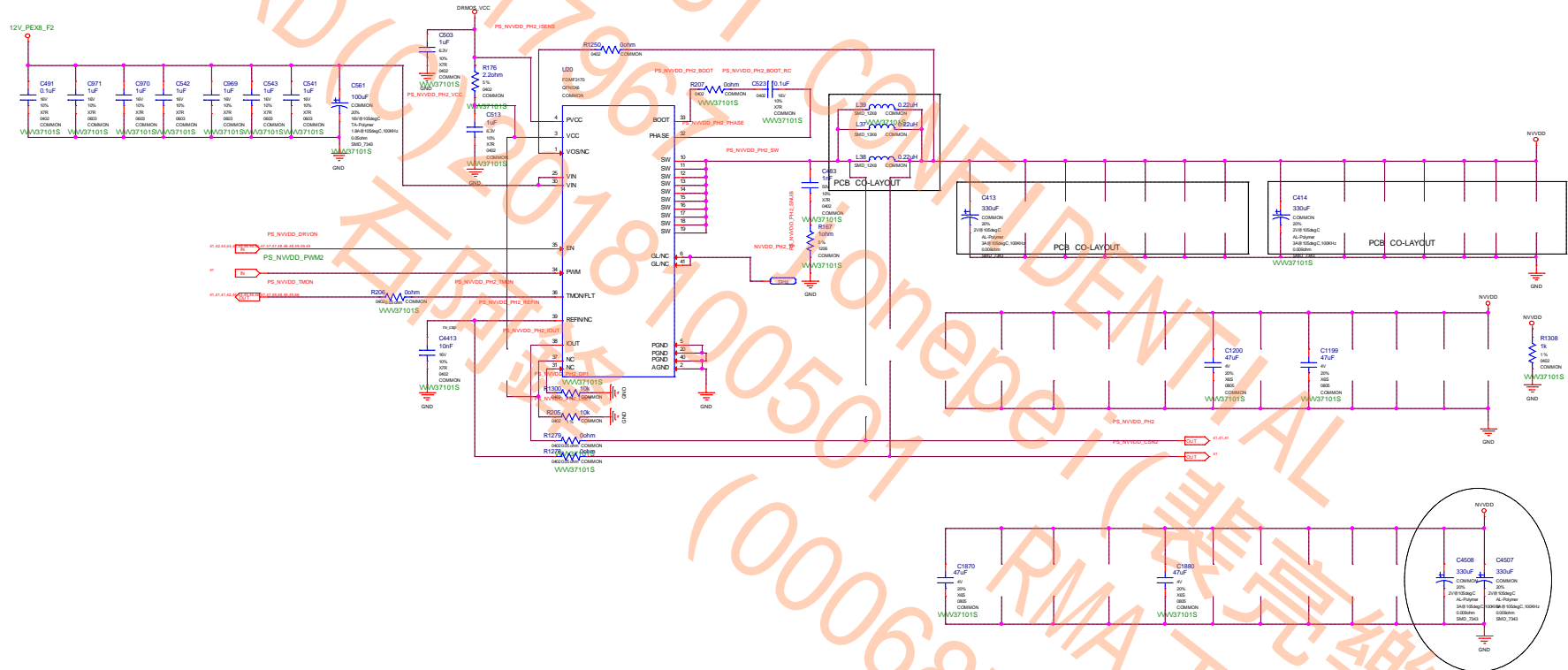
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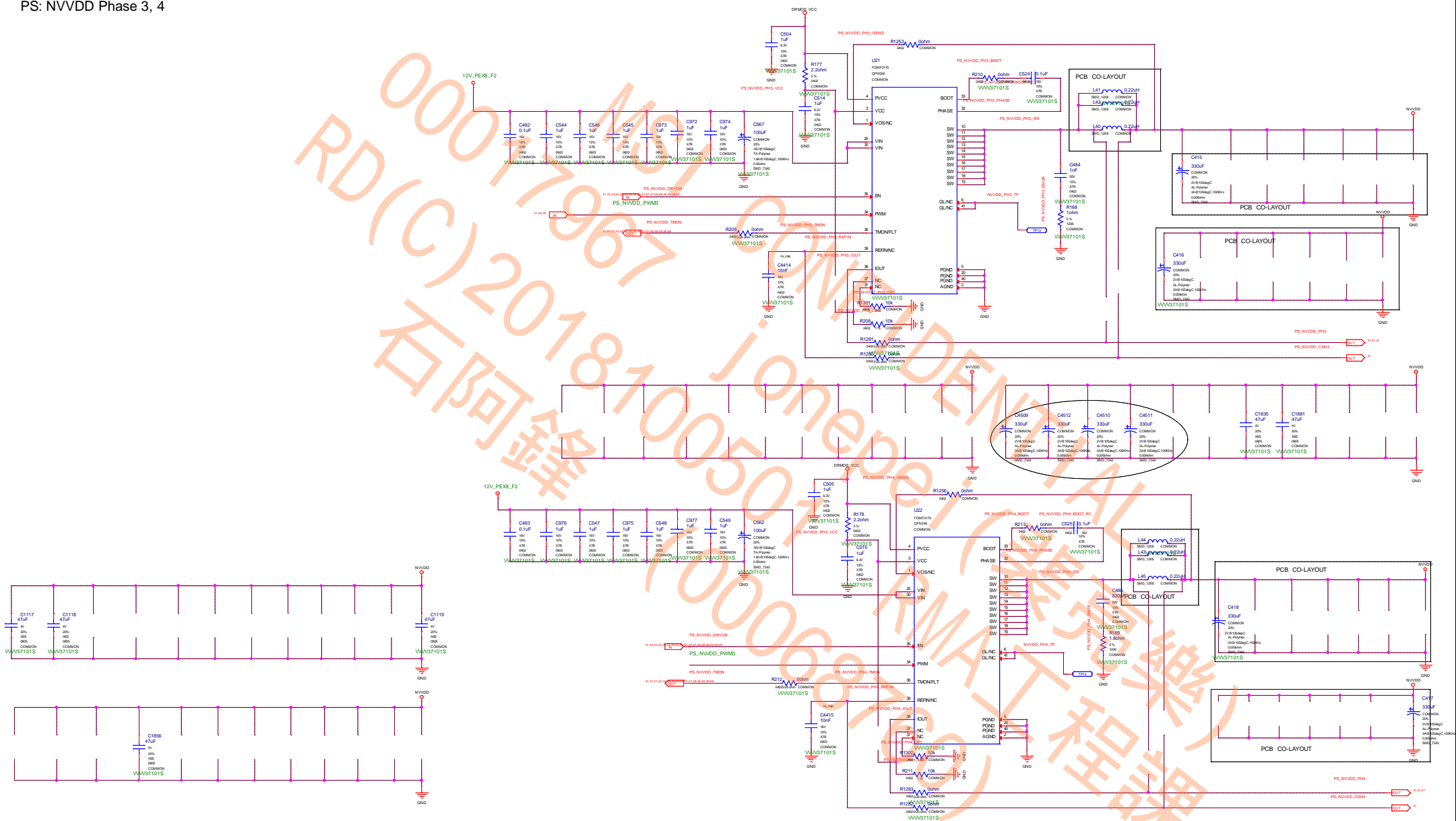


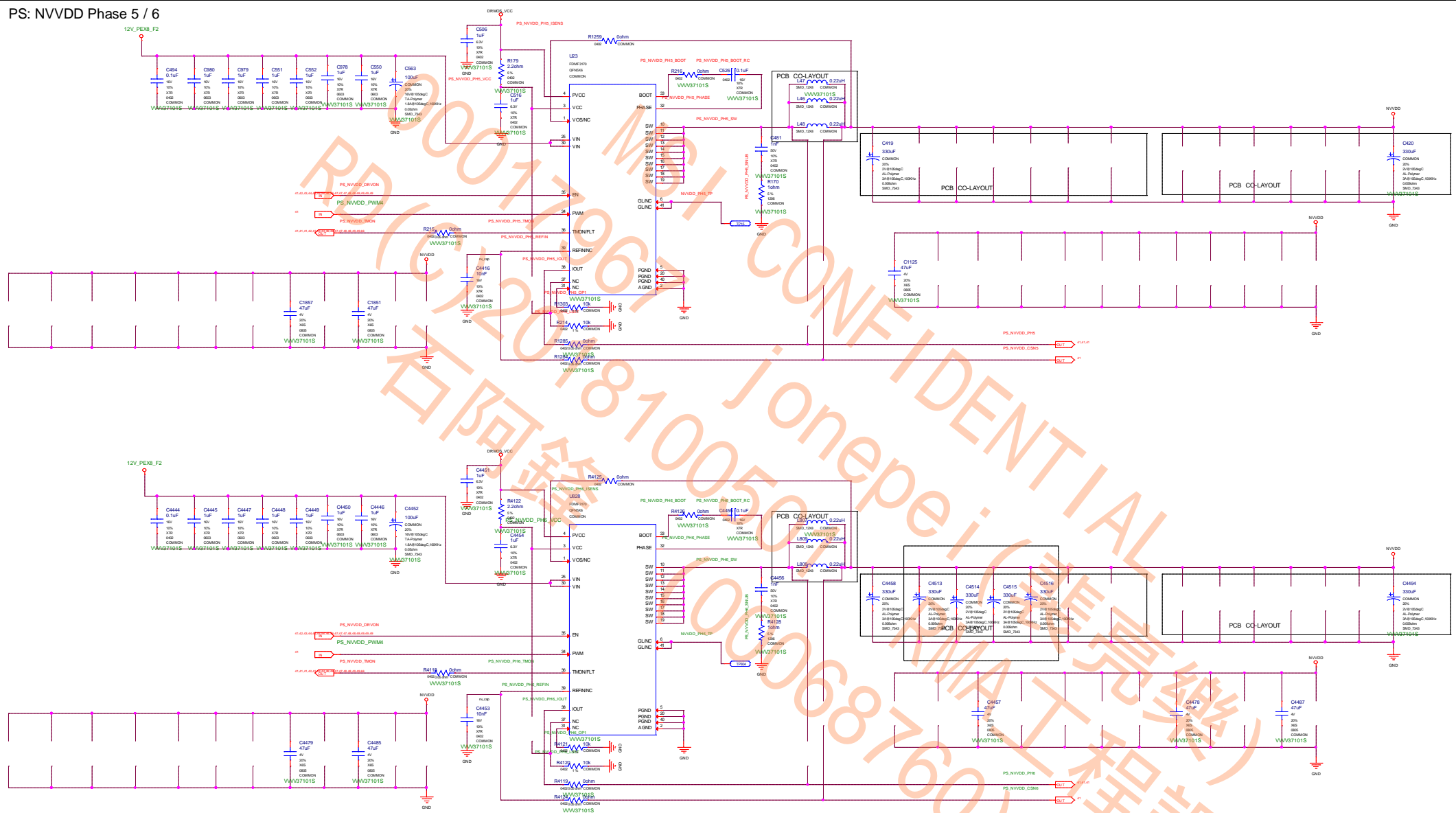
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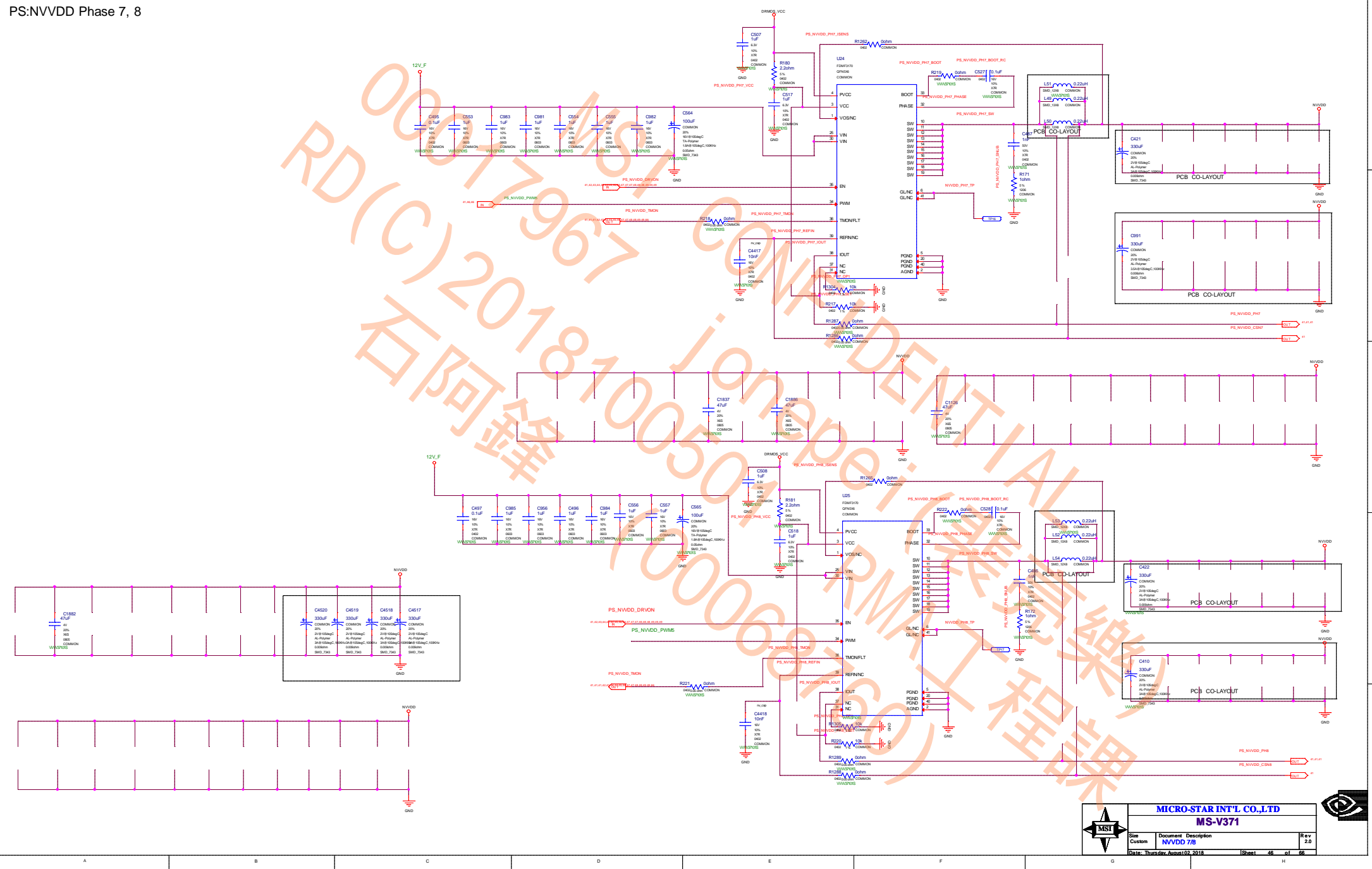


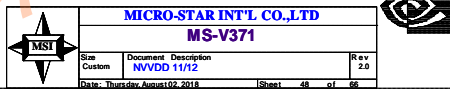


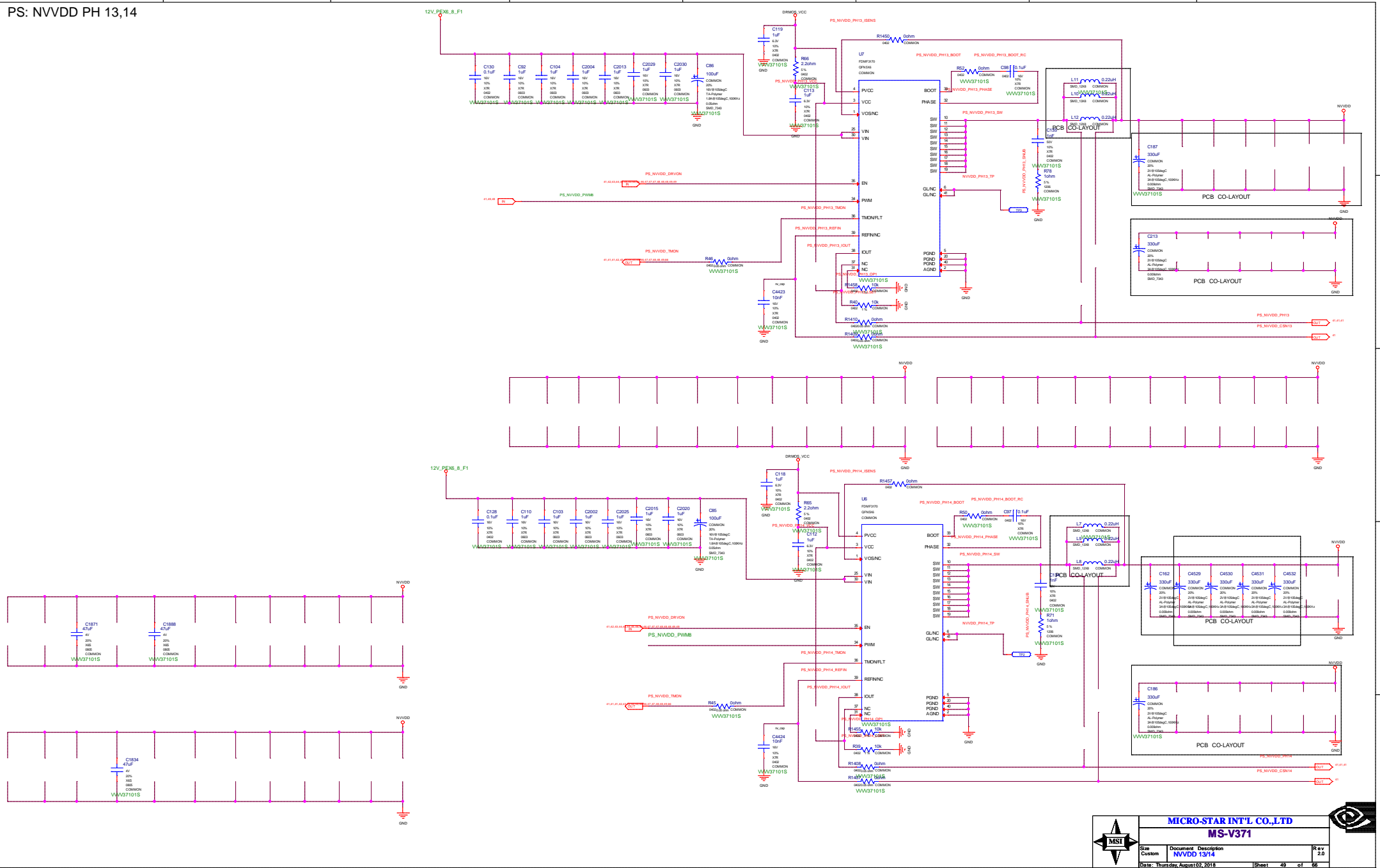
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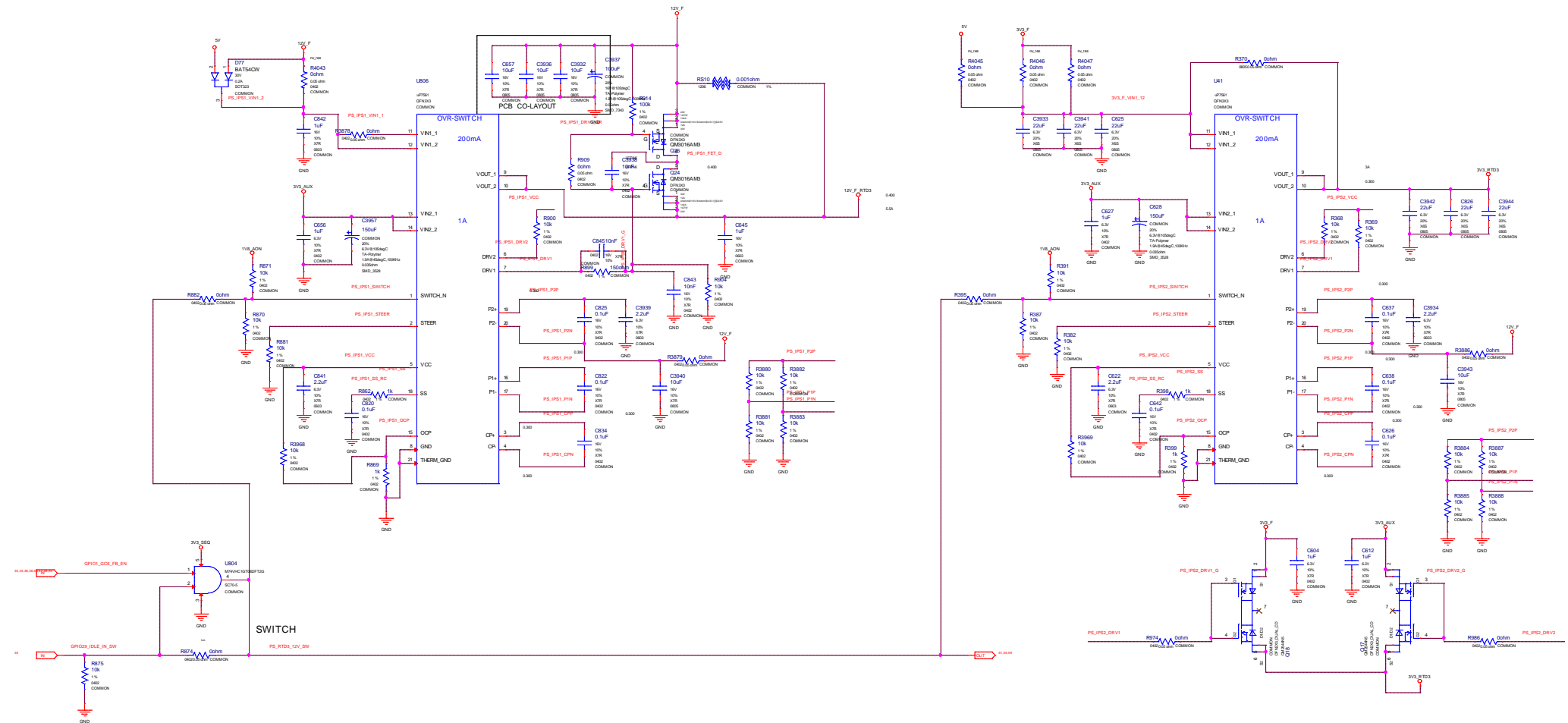
PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

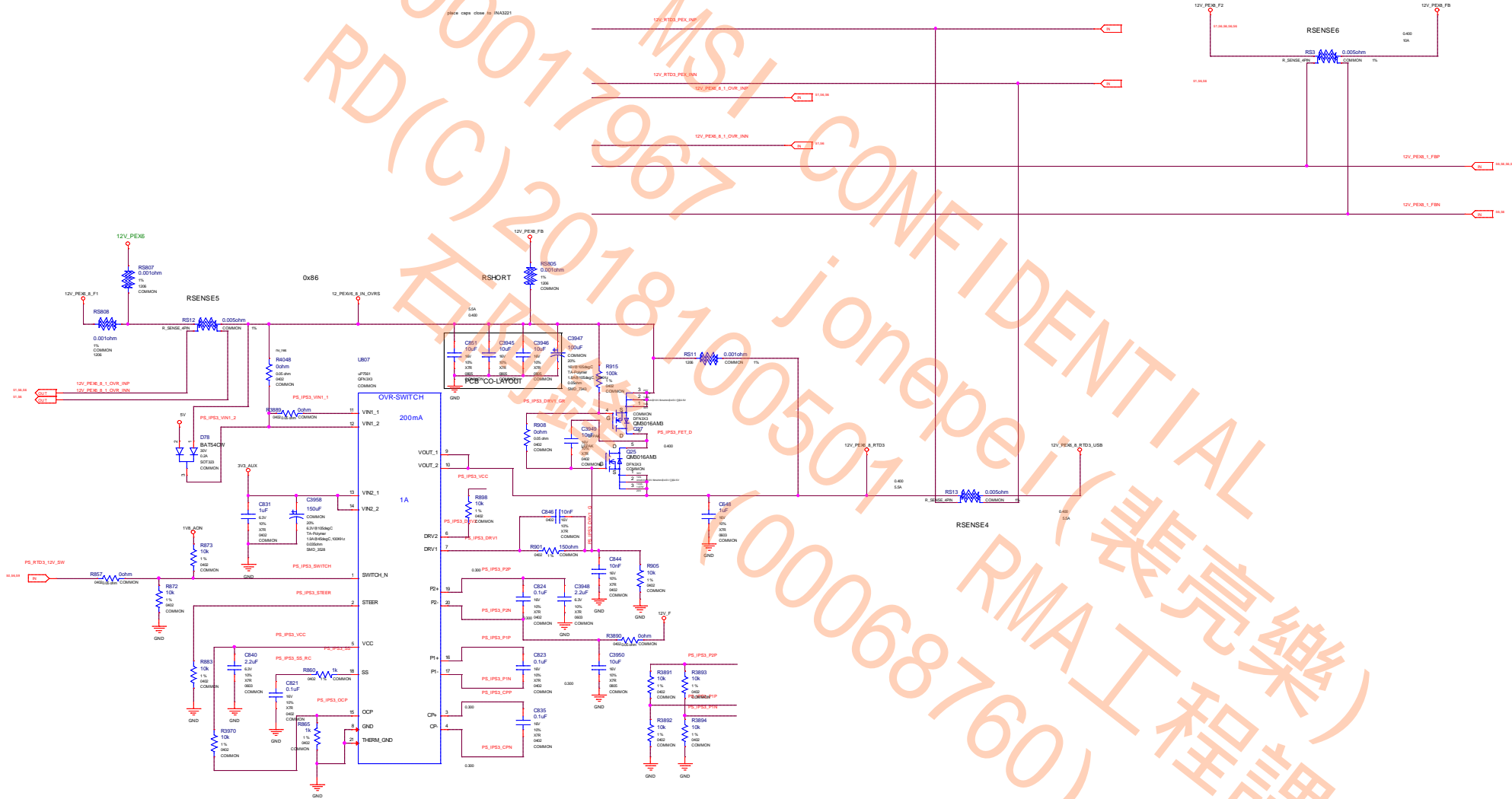




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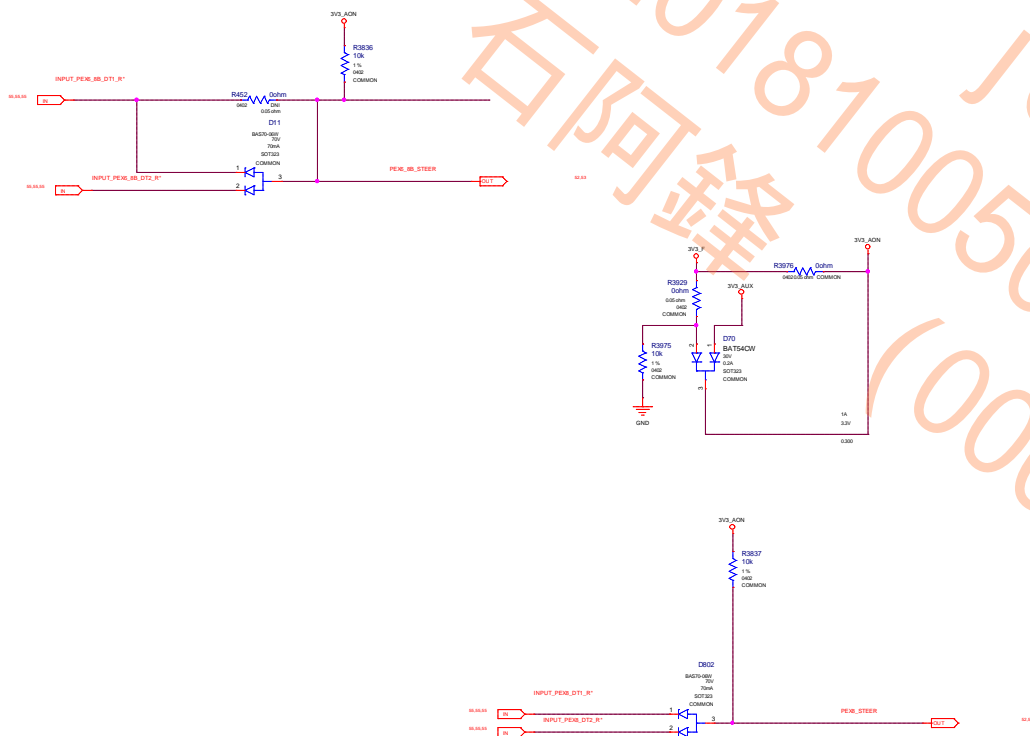


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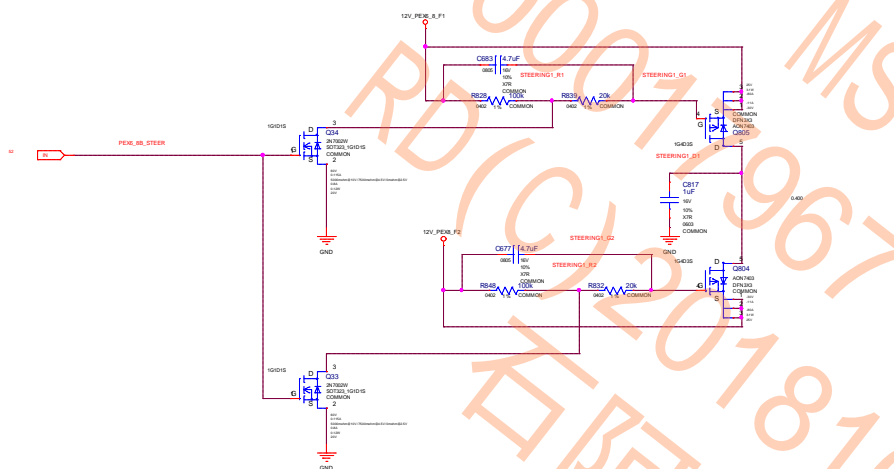
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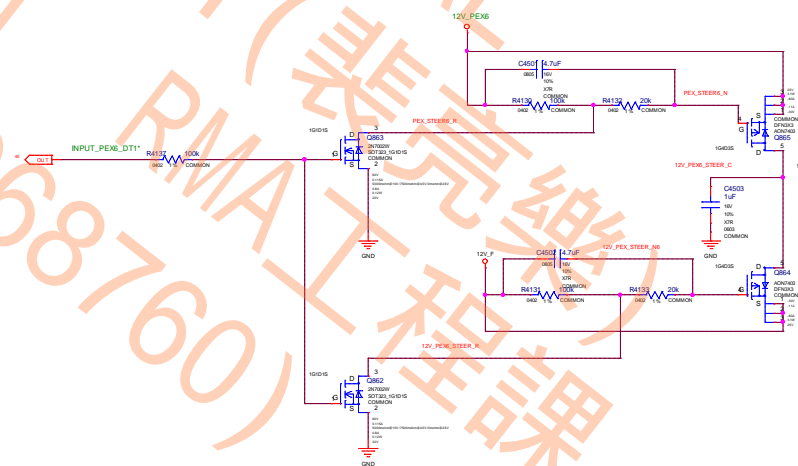
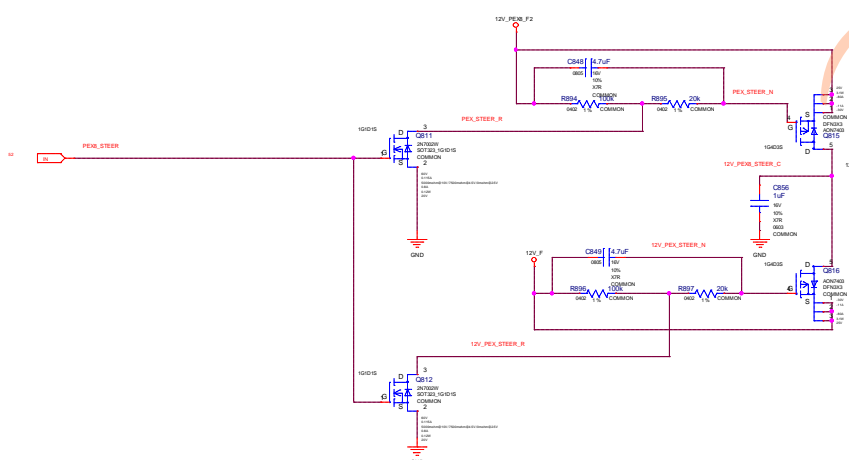


GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSl mode

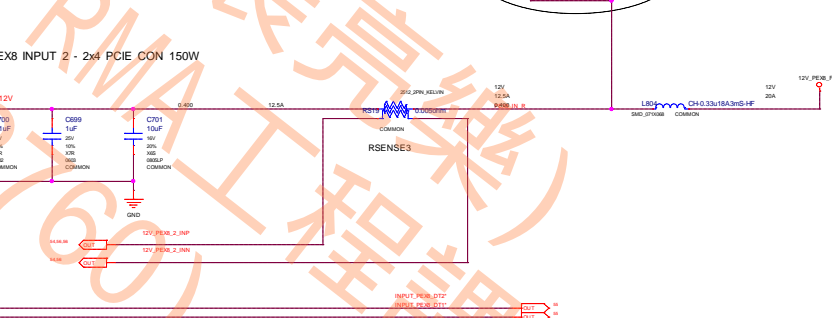
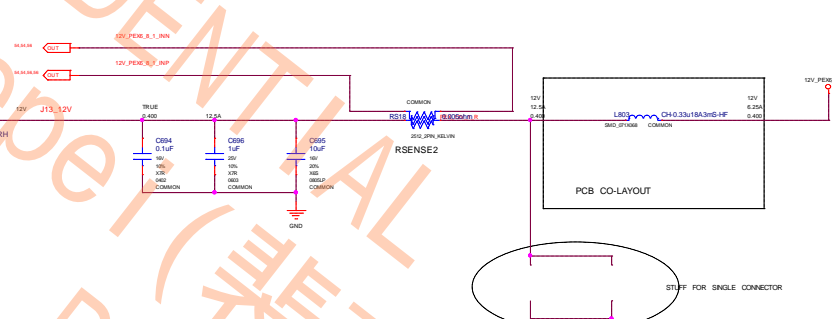
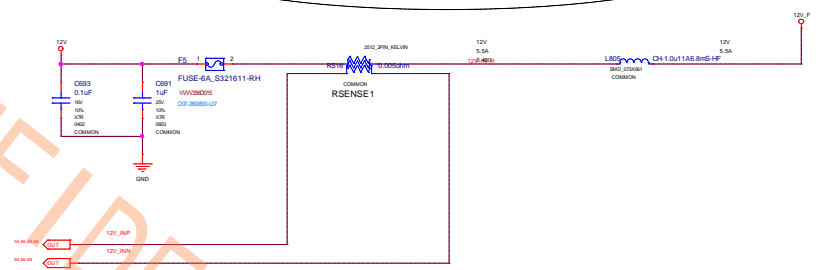
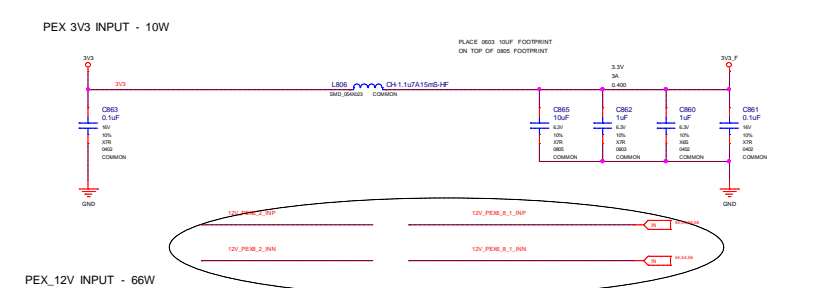
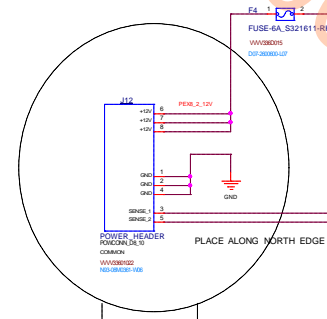
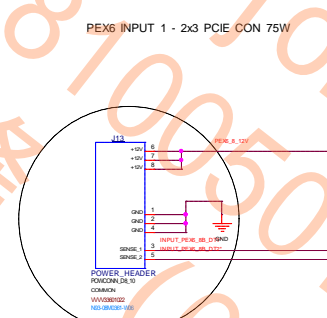
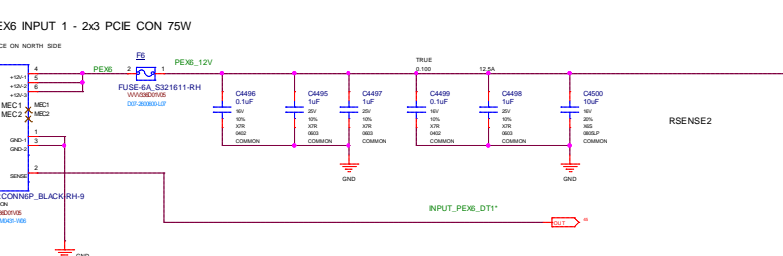
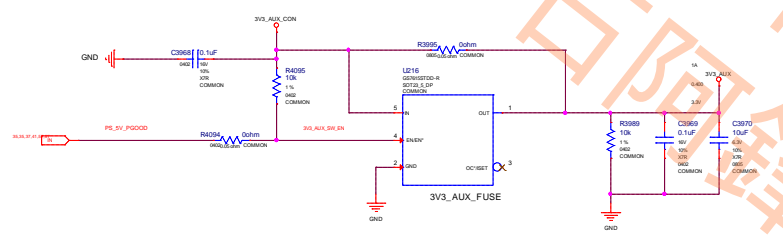
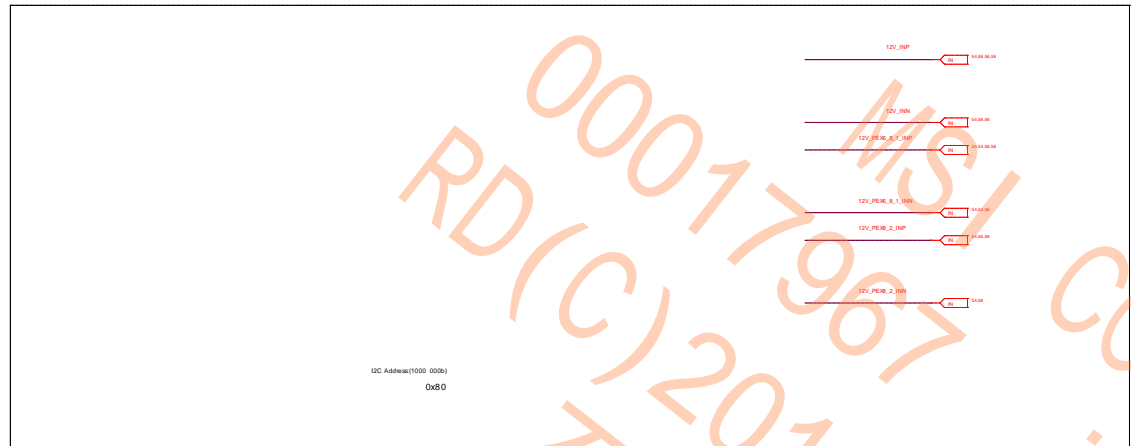


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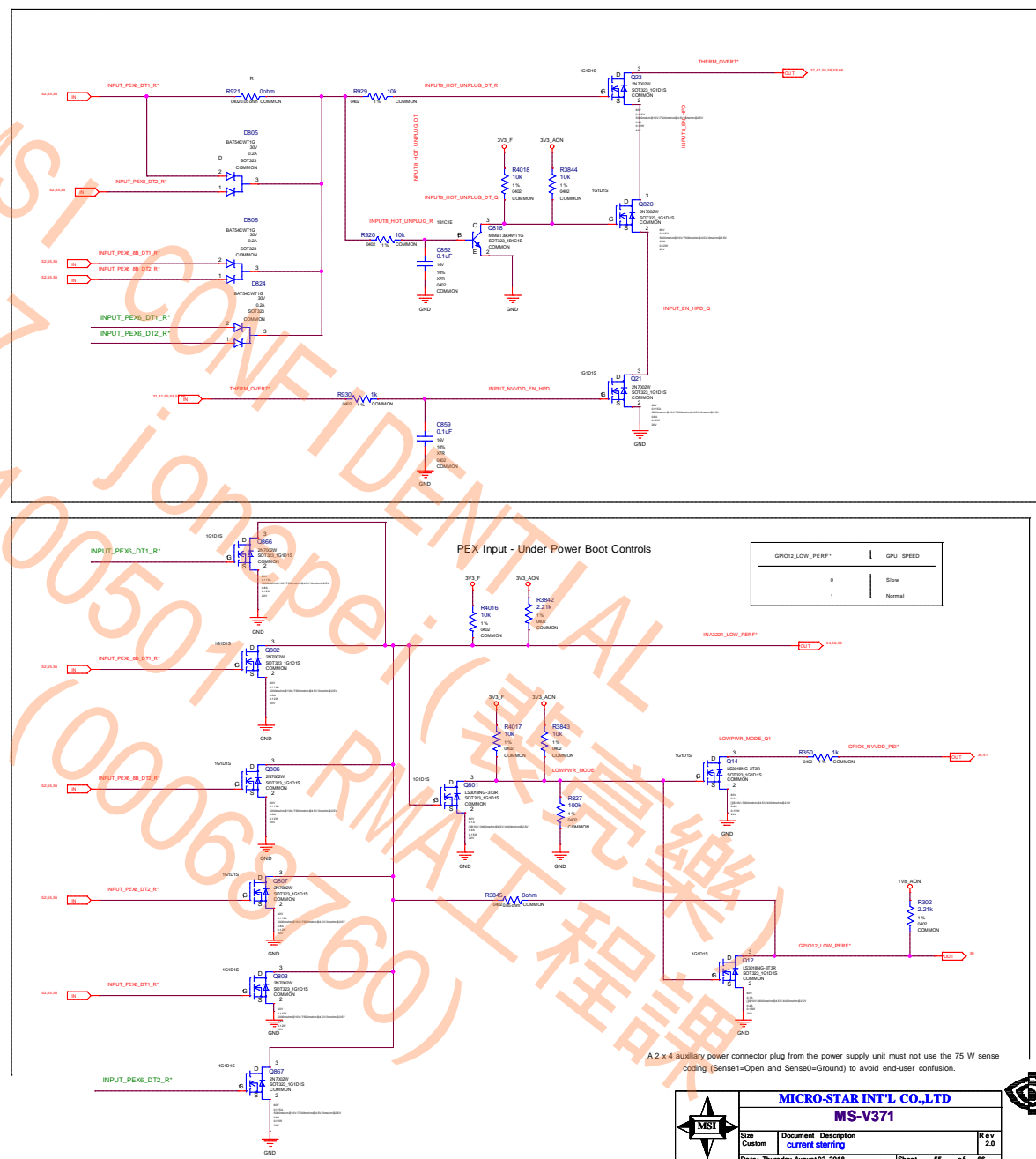
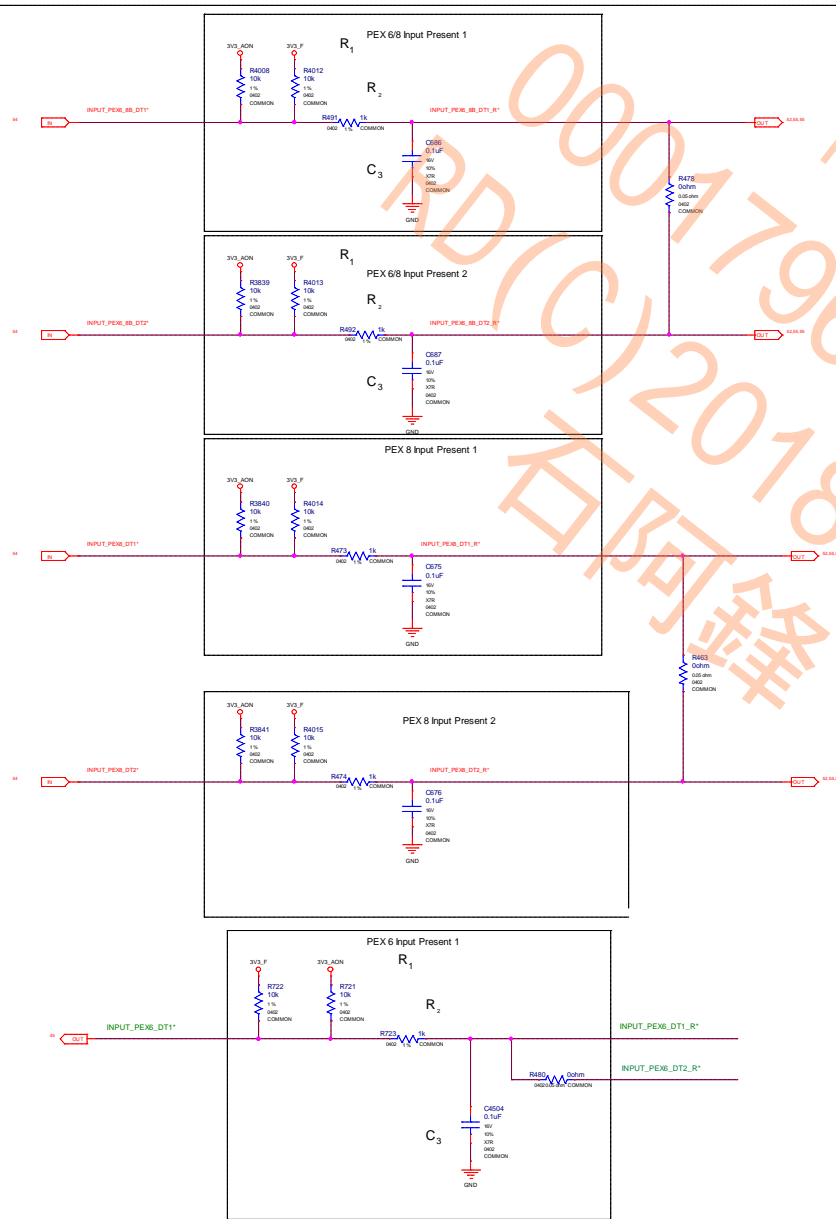
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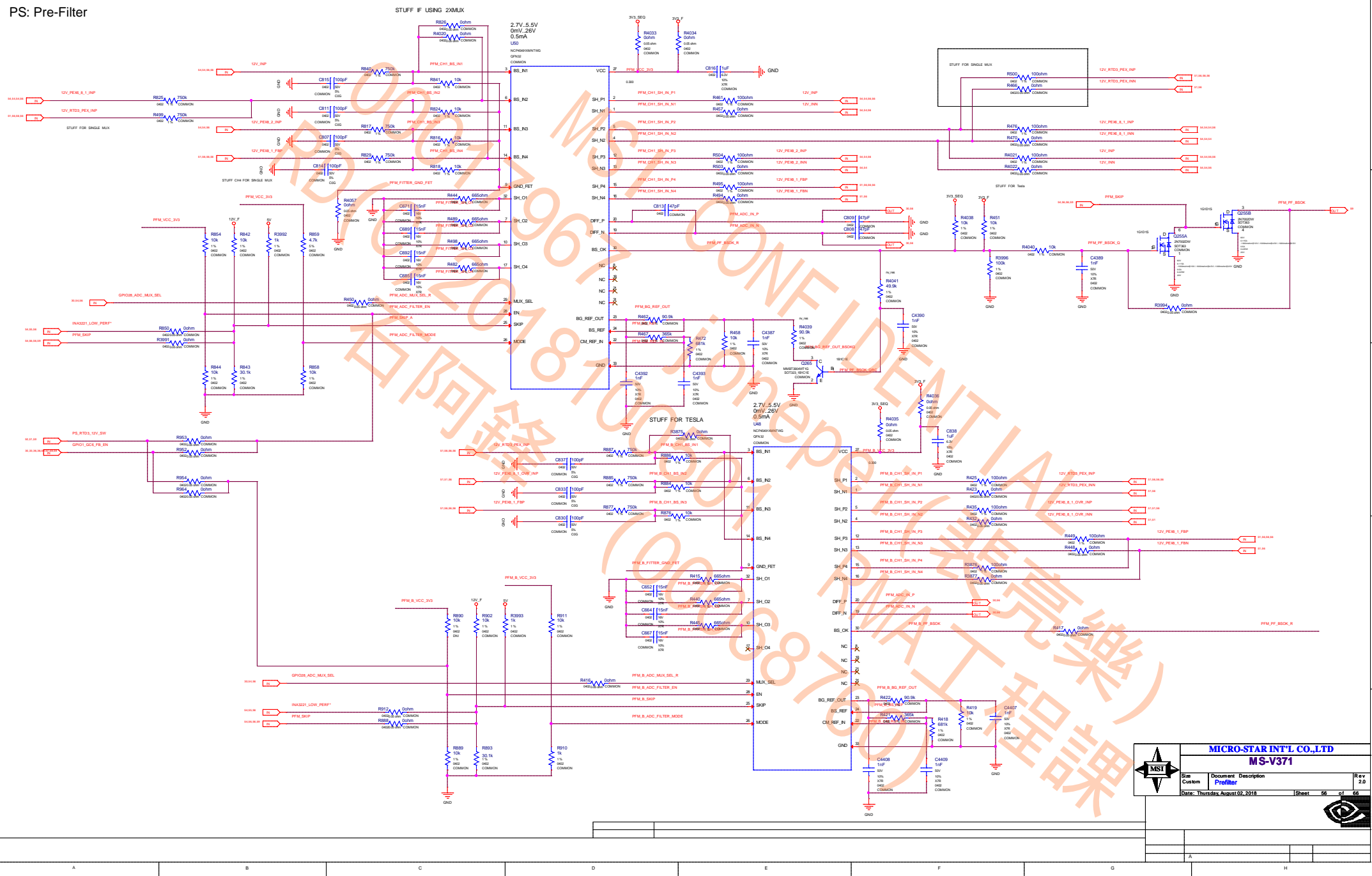
PS: Inputs, Filtering, and Monitoring



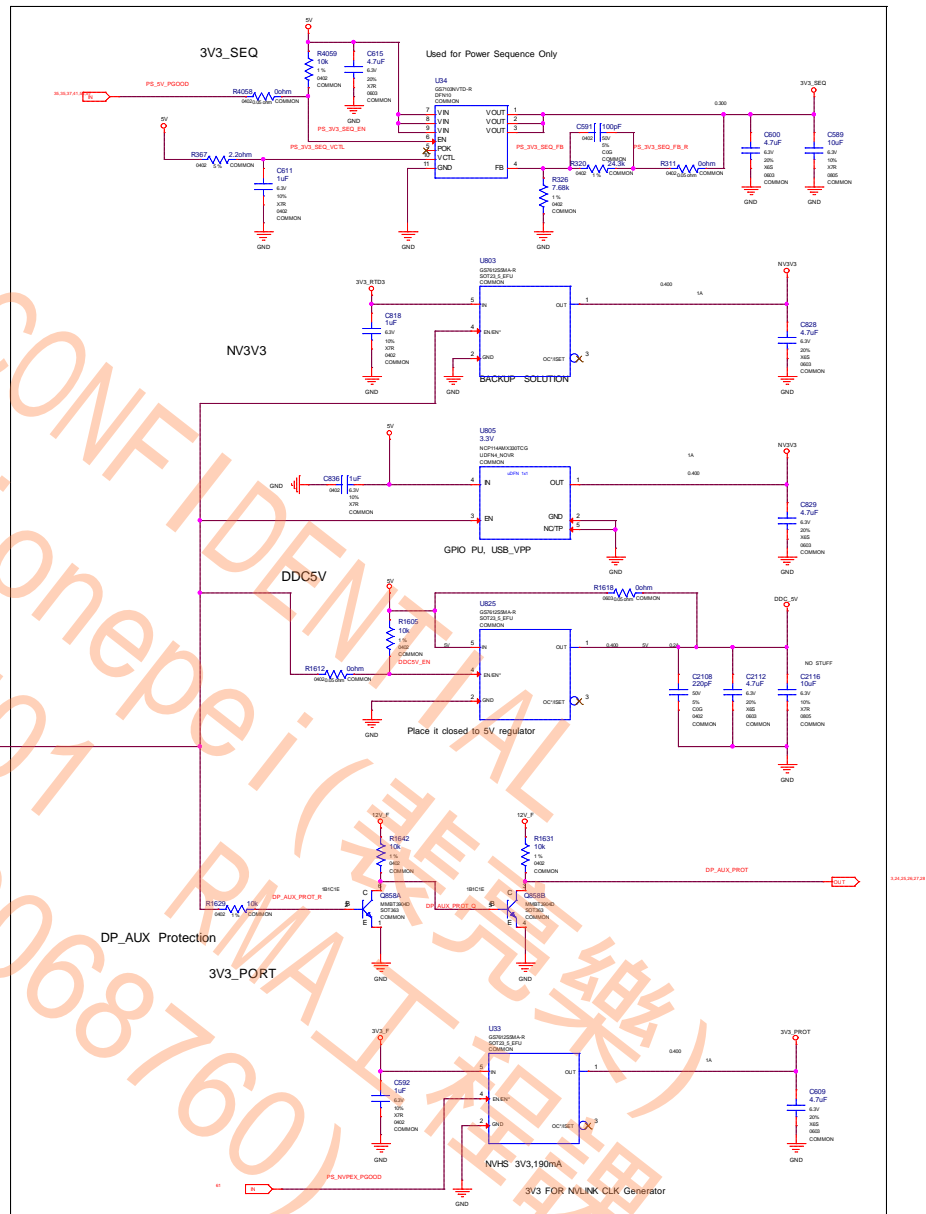
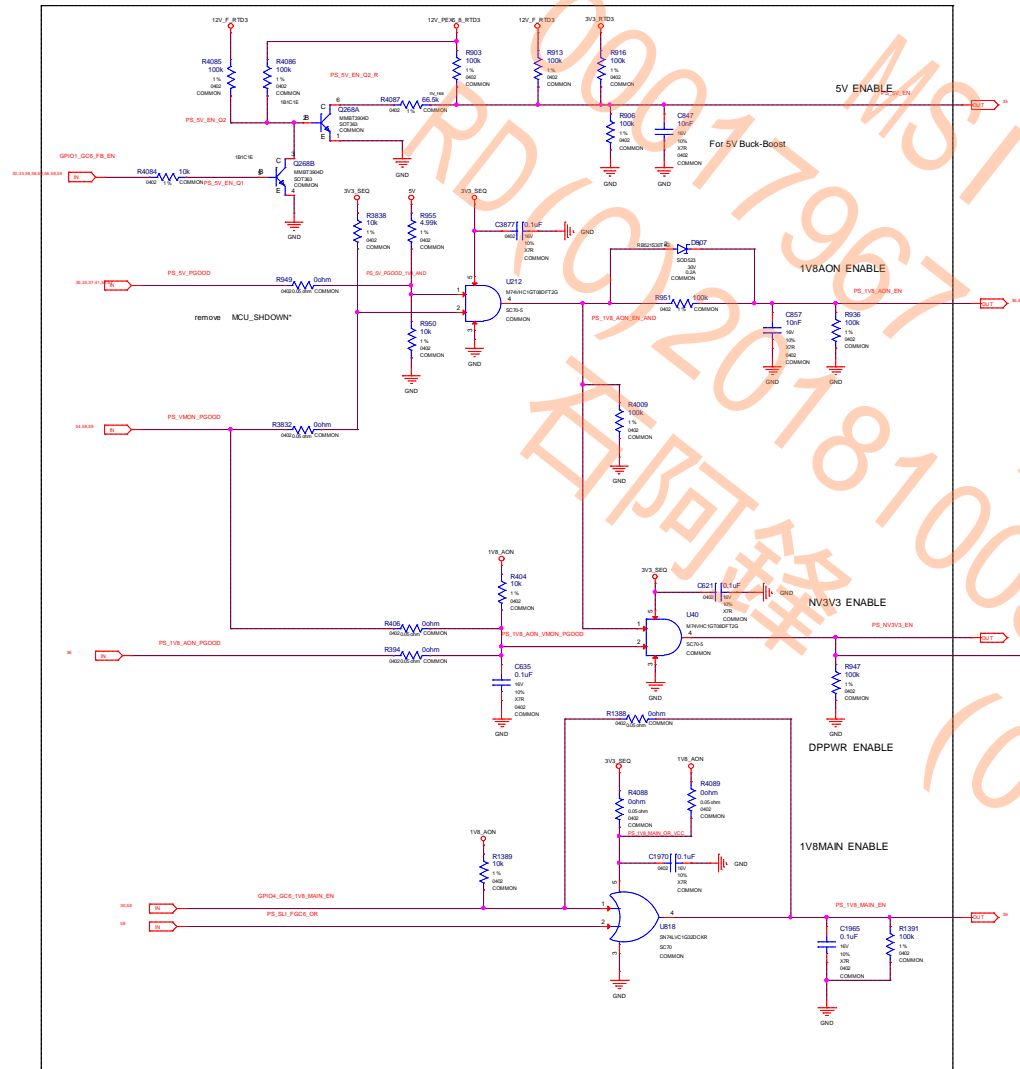
PS: 12V Current Steering & Hot Unplug Detect



PS: Pre-Filter



SEQUENCE:5V,1V8,NV3V3 ENABLE



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ASSEMBLY
PAGE DETAIL

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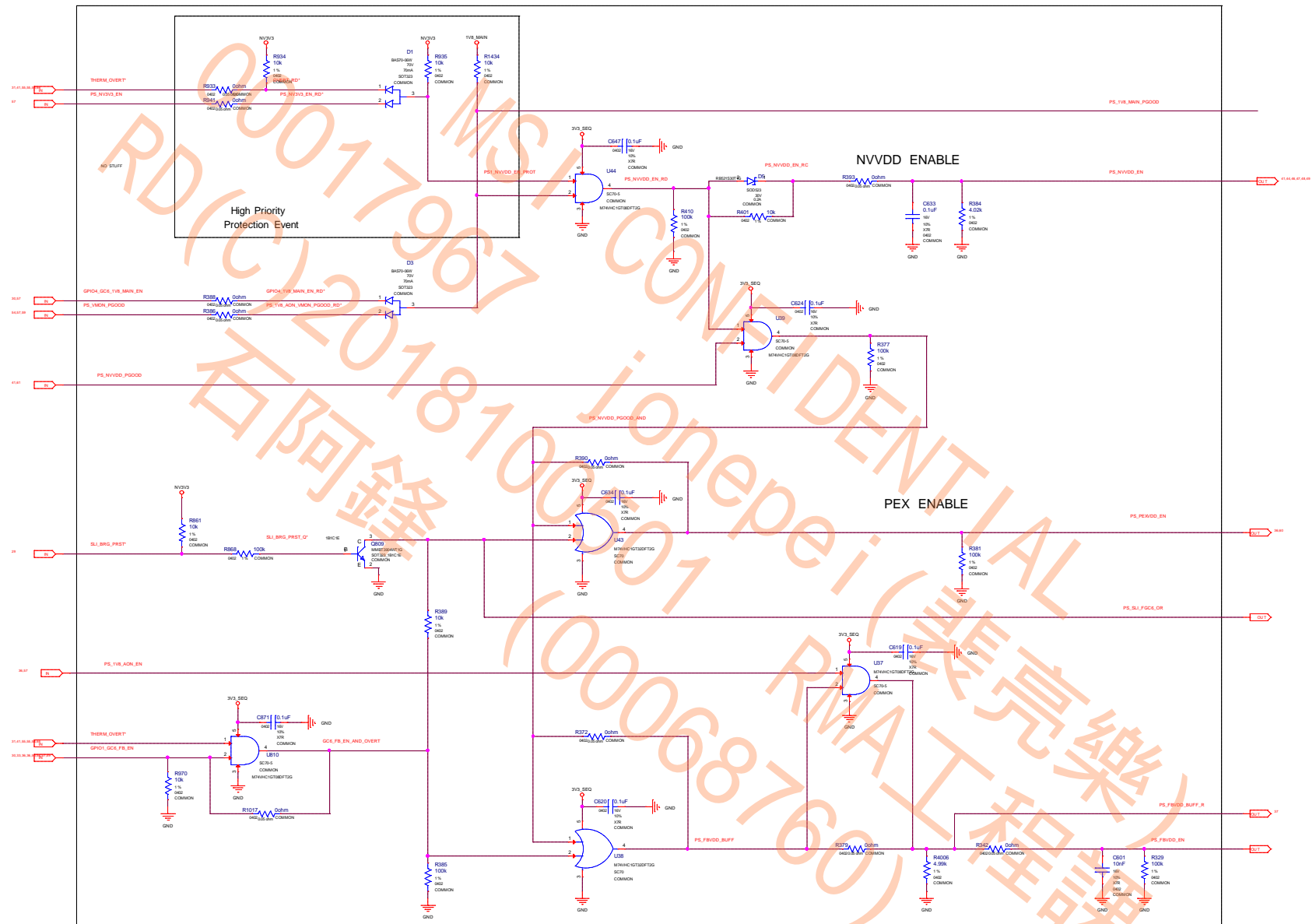


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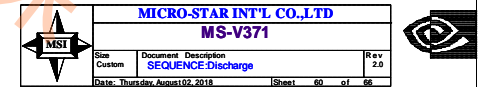
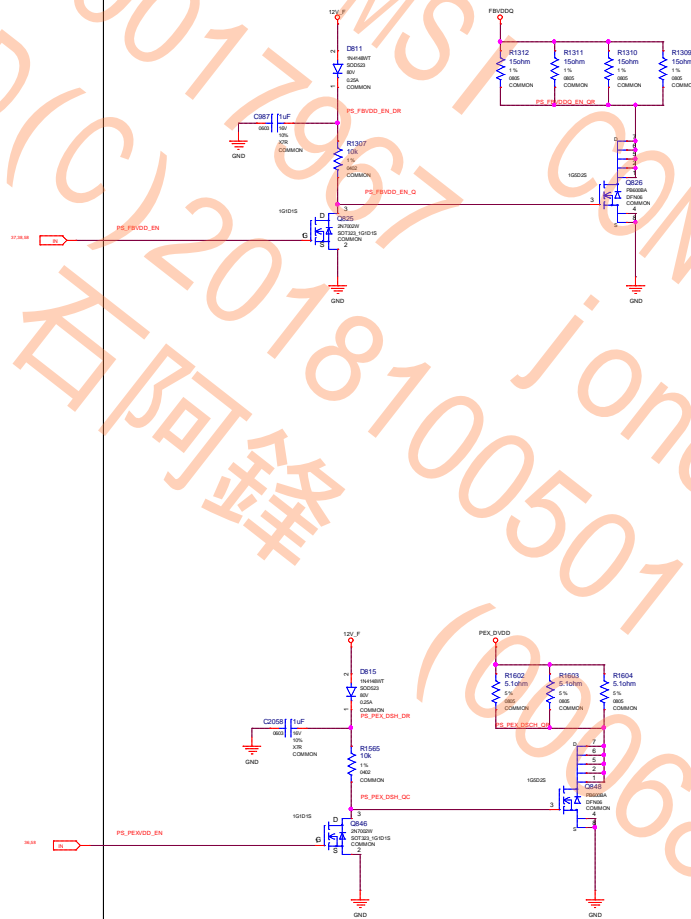
SEQUENCE:NV,PEX,FB ENABLE

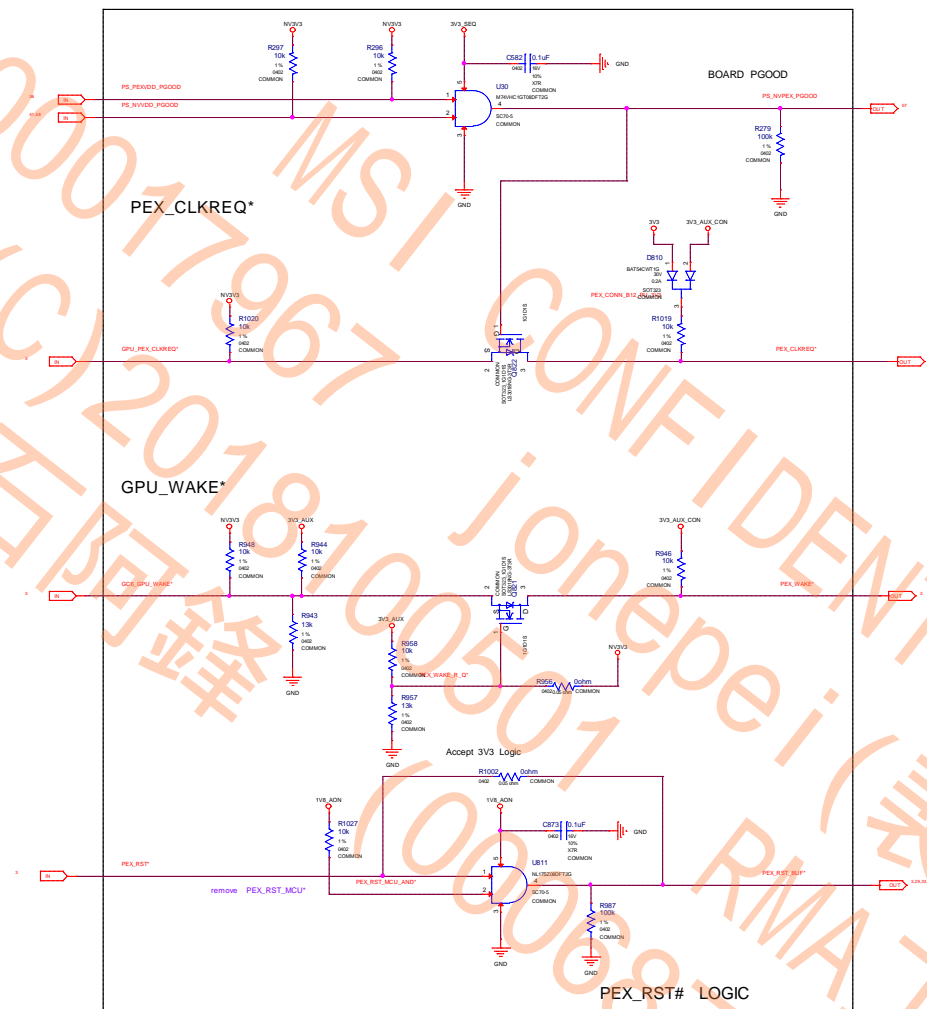


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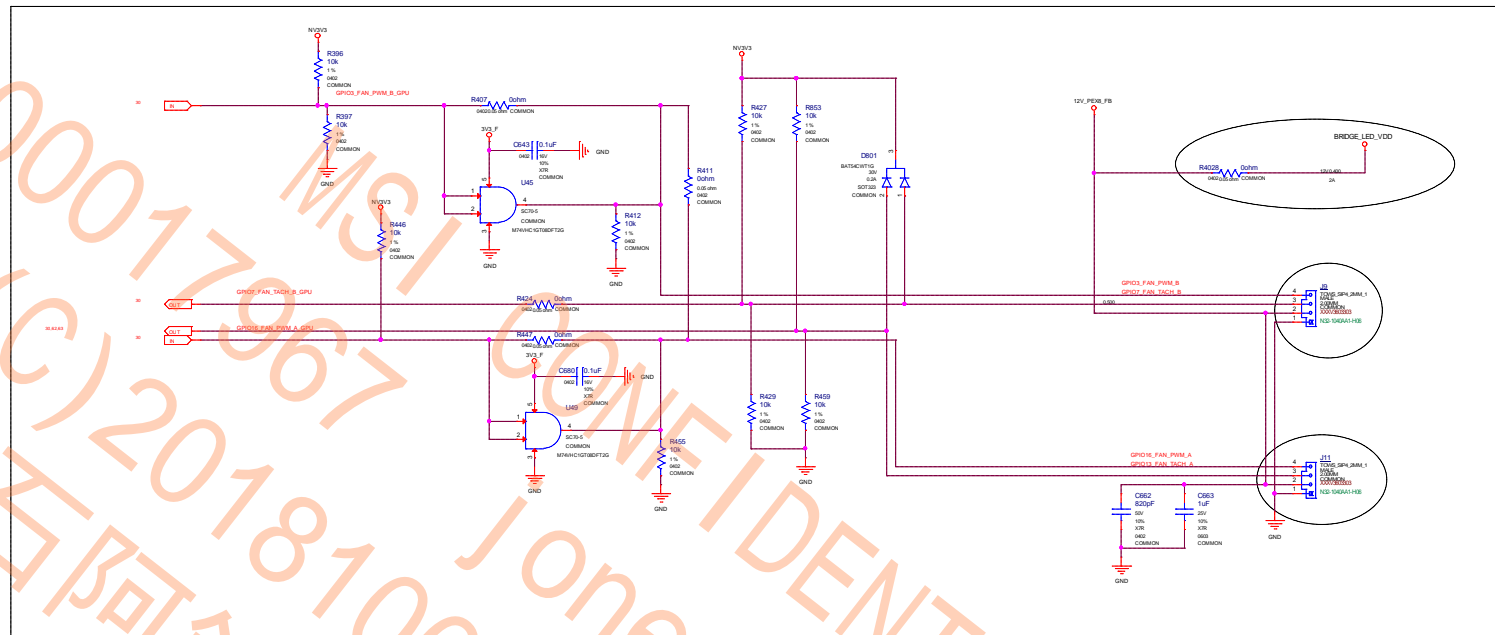
Size Custom	Document Description SEQUENCE-IV,PEX,FB ENABLE	Rev 2.0
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MISC: FAN & LED1



Firmware Programming

Debug

5V_LED

J803

1

2

3

4

5

GND

SM0DAT3

SM0CLR3

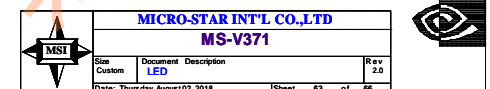
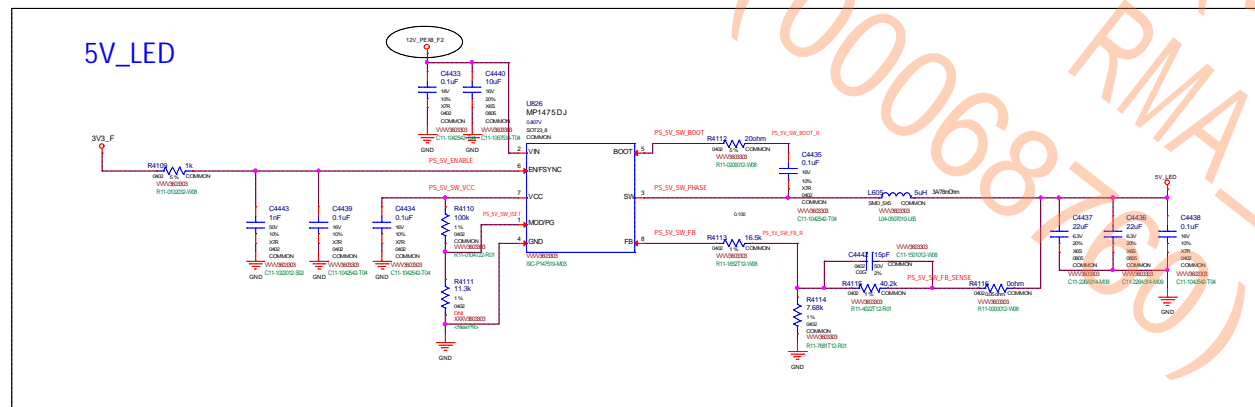
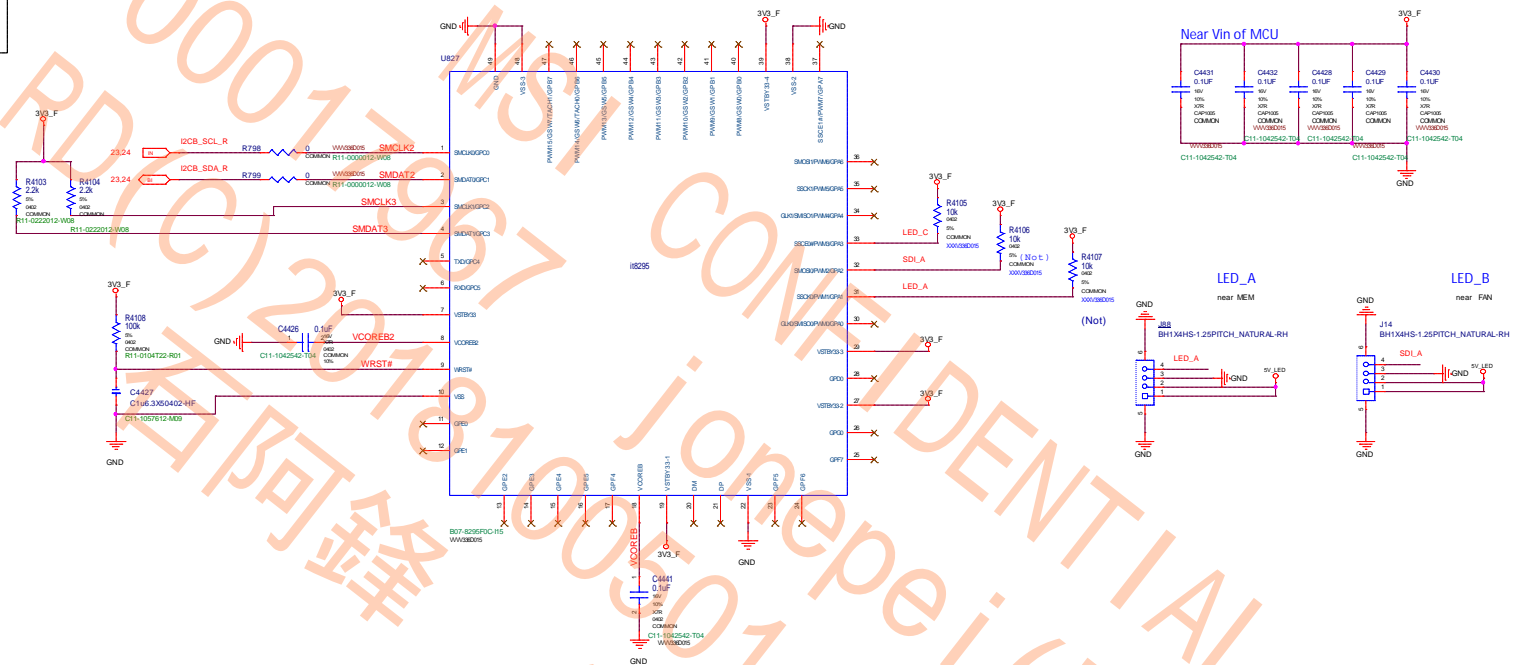
3V3_F

H1XS

0x4

0x000000015

NXP-1302061-H06



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