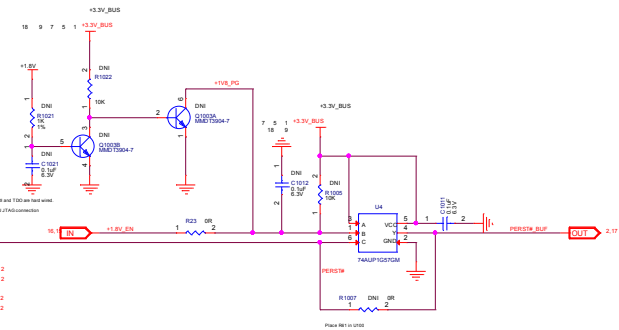
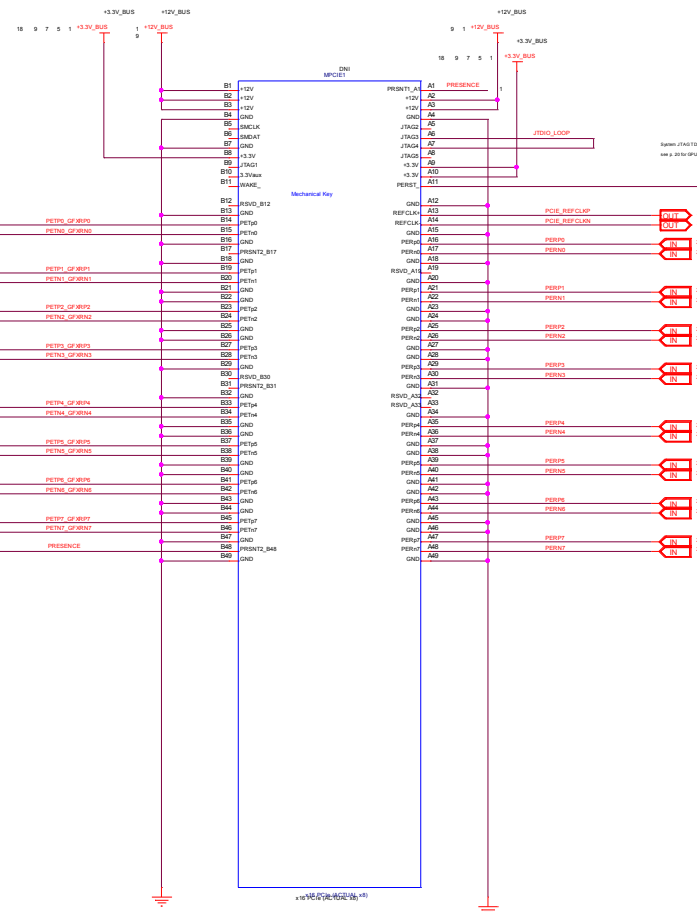
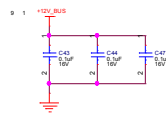
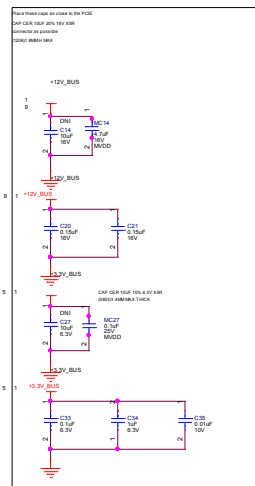
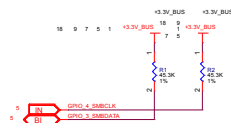




## PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DN1	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BJO	BRING UP ONLY

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#46, No.1387, ZHANGDONG ROAD  
SHANGHAI, CHINA 201203

**SHEET:** PCIe Edge Connector

DATE: Wed Aug 29 03:27:33 2018

REV: P00

SHEET NUMBER: 1 OF 2

DOCUMENT NUMBER: 105\_d12900\_00

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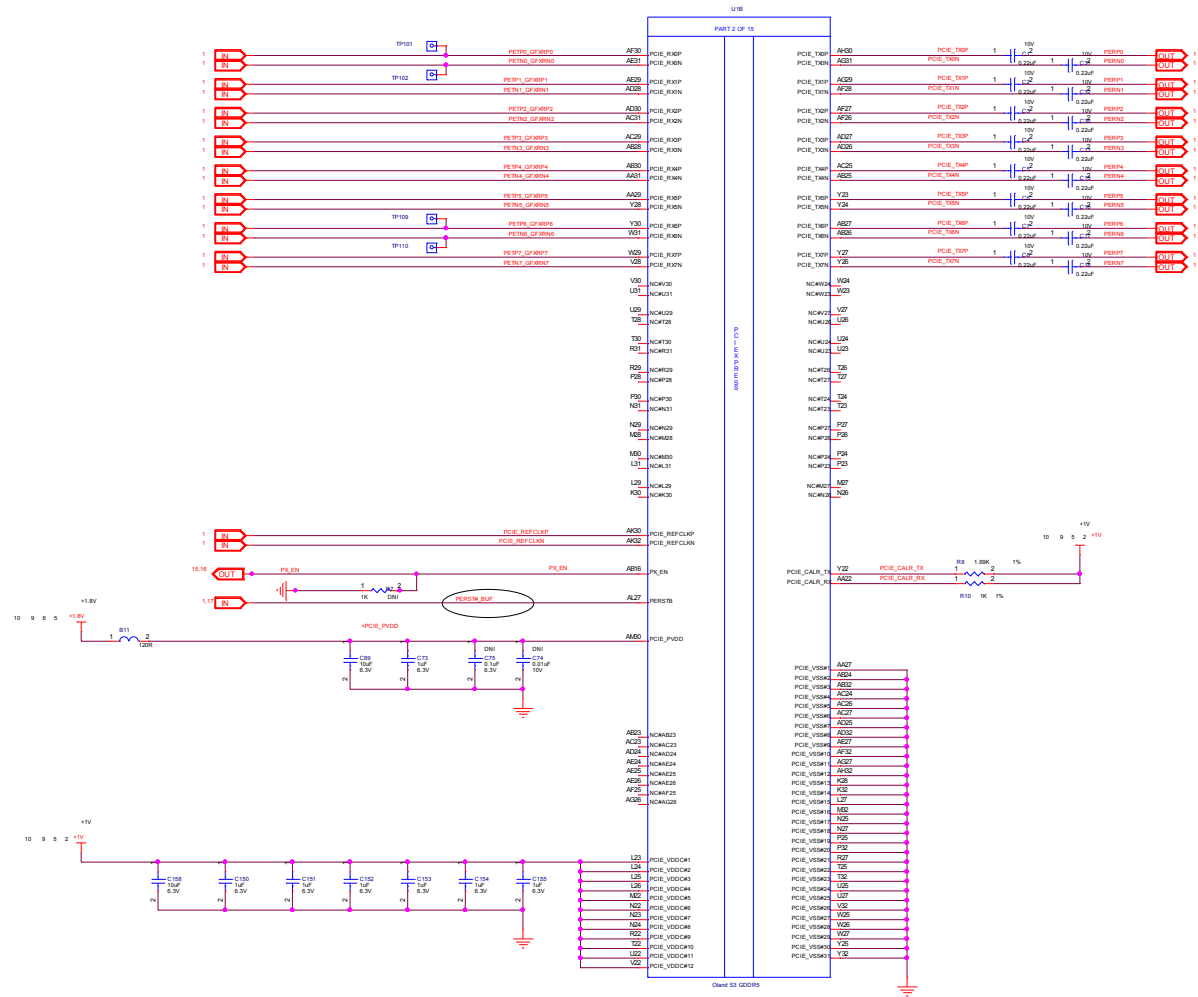
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TITLE: \_\_\_\_\_

XXX

OLAND PCIe Interface

NOTE: Some of the PCIe waypoints will  
be available through vias on traces.



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SHEET: Oland PCIe#8 Interface

DATE: Thu Jan 05 05:41:57 2017

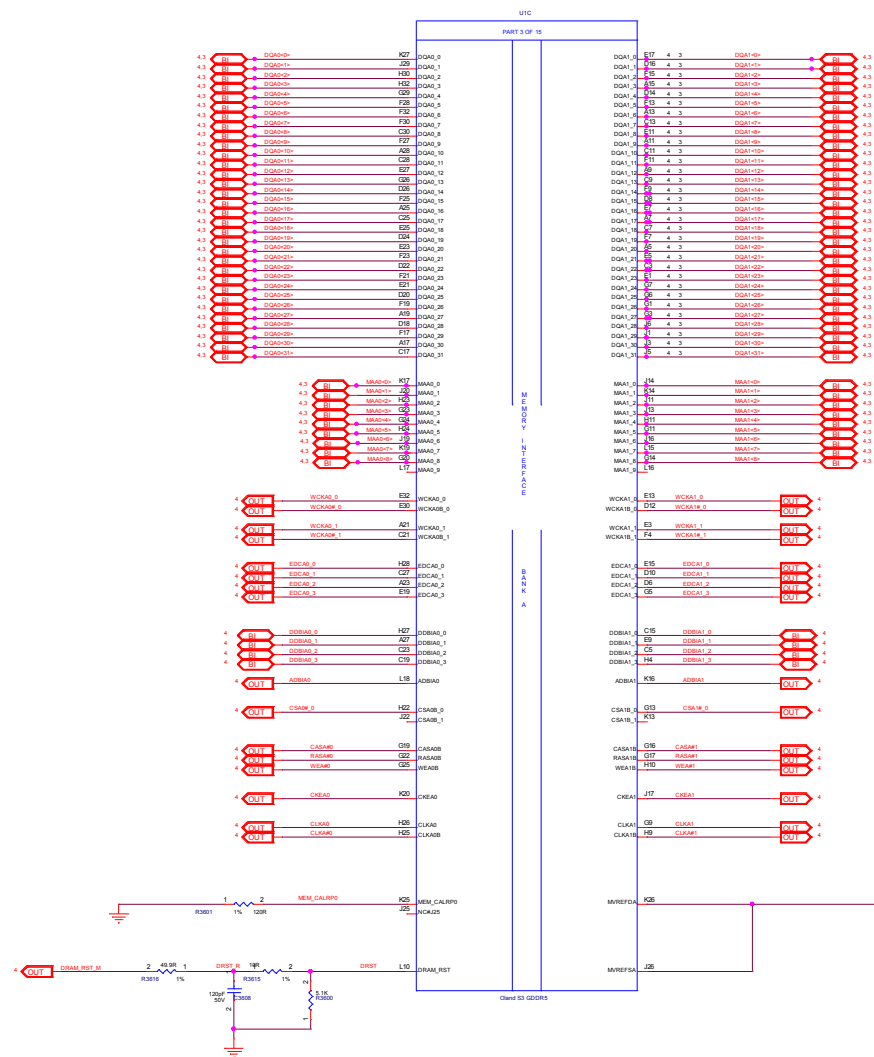
SHEET NUMBER: 2 OF 20


DOCUMENT NUMBER: 105\_412800\_00A

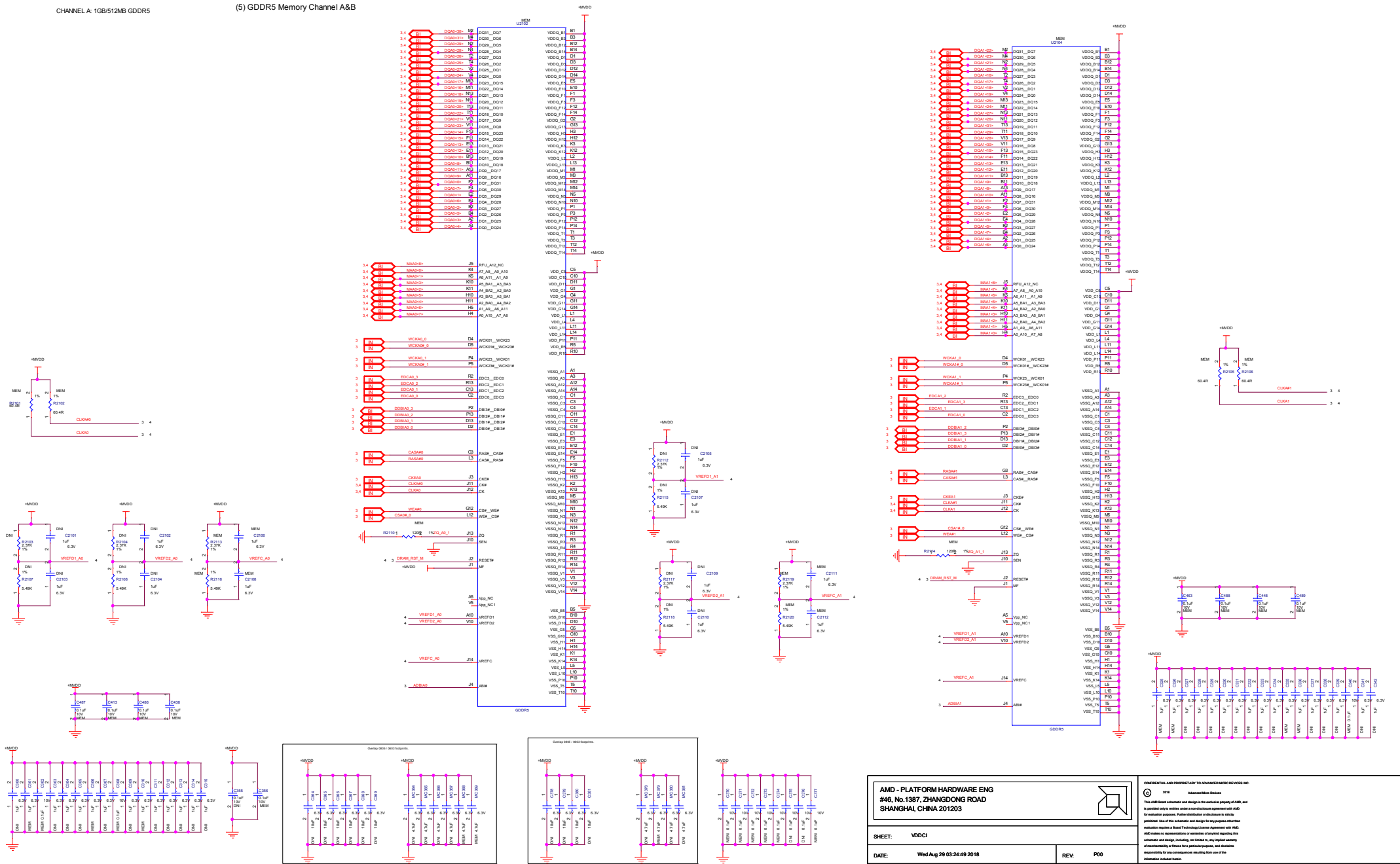
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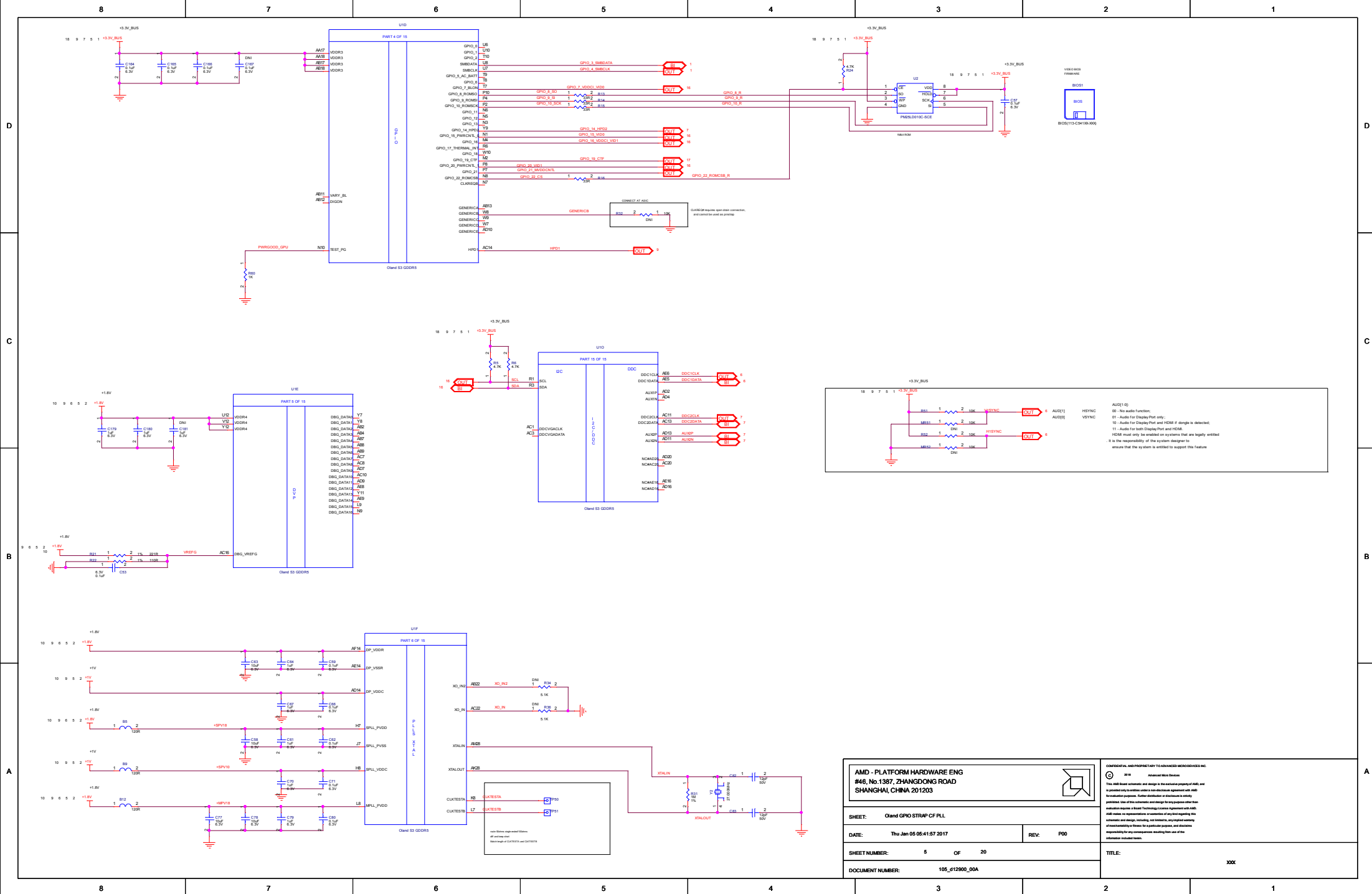
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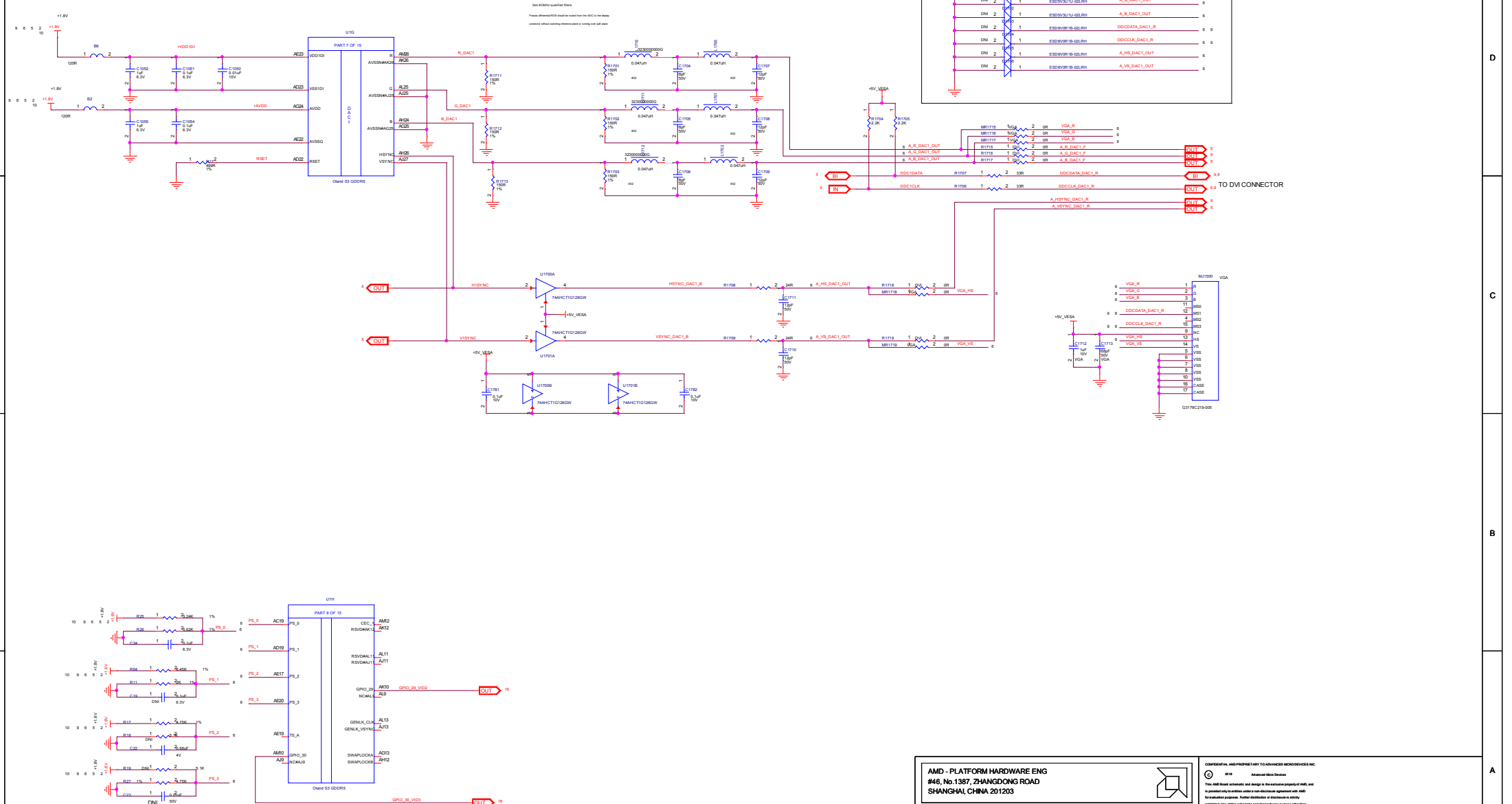



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SHEET: VDDCI		REV: P00		TITLE:	
DATE: Wed Aug 29 03:24:49 2018				XXX	
SHEET NUMBER: 3 OF 20					
DOCUMENT NUMBER: 105_012900_00A					
NOTES: NOTE					



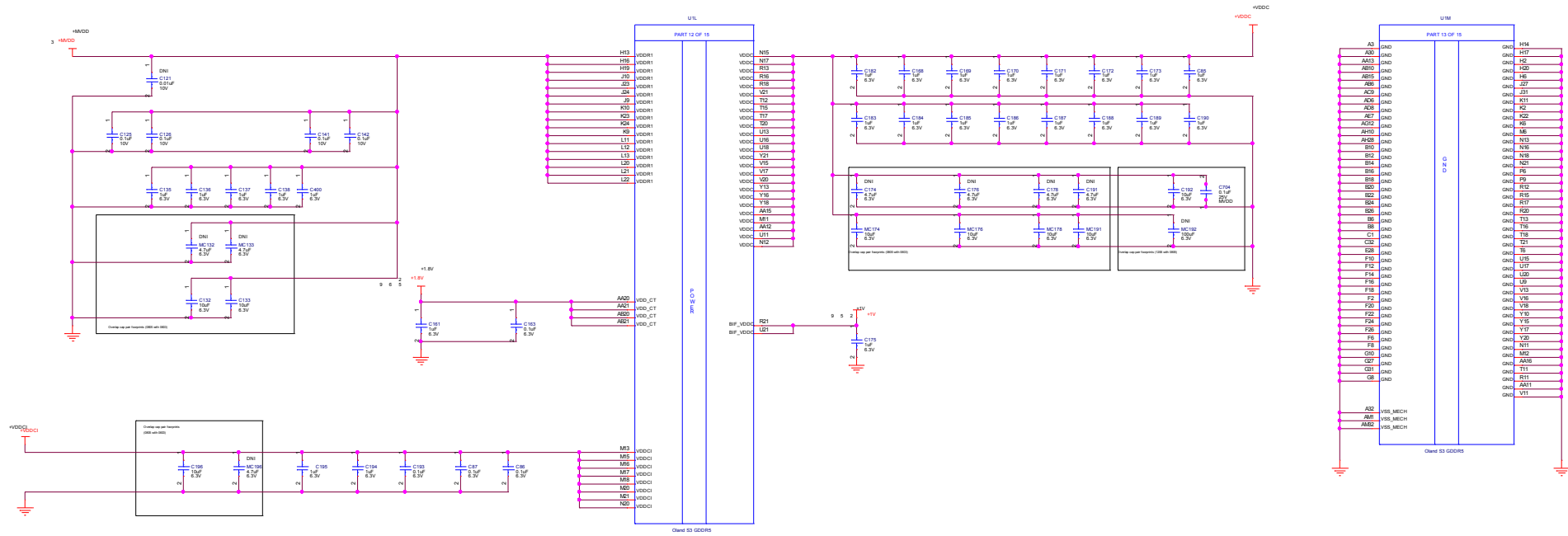



# Oland DAC1

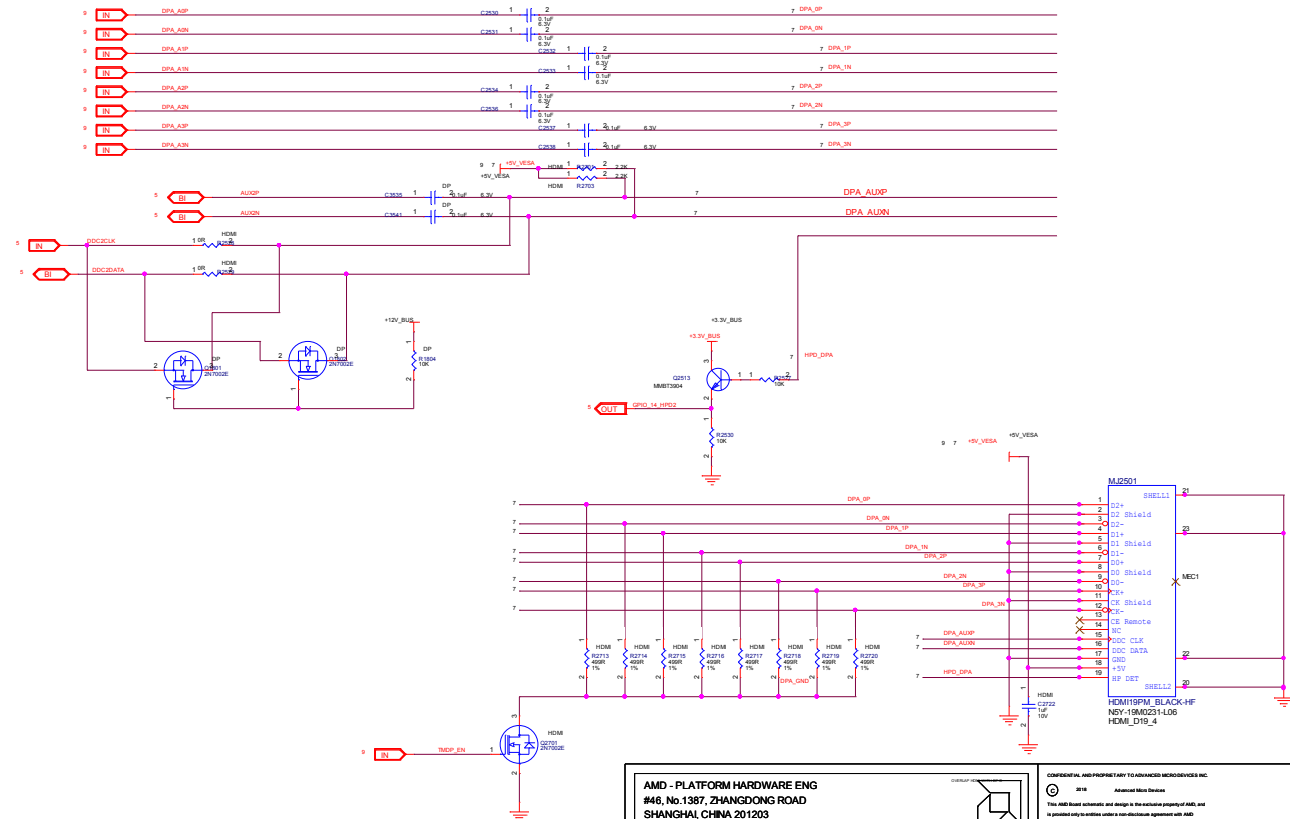
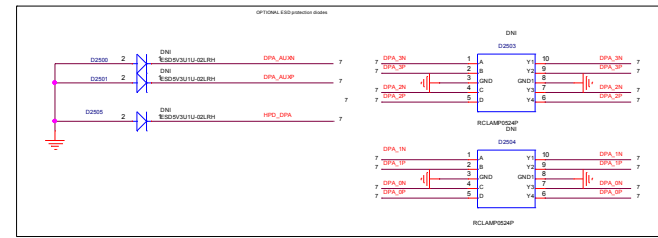


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SHEET: Oland DAC		REV: P00		TITLE: XXX	
DATE: Thu Jan 05 05:41:56 2017					
SHEET NUMBER: 6 OF 20					
DOCUMENT NUMBER: 105_d12900_00A					

## OLAND S3 Power & GND

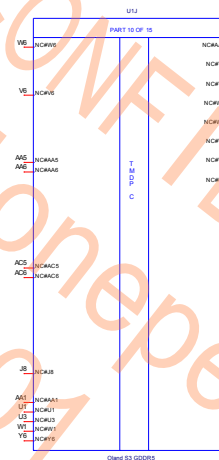
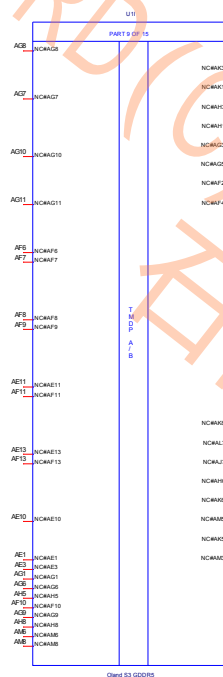



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<b>SHEET: VODCI</b>		<b>DATE: Wed Aug 29 03:24:49 2018</b>	
<b>SHEET NUMBER: 10 OF 20</b>		<b>REV: P00</b>	
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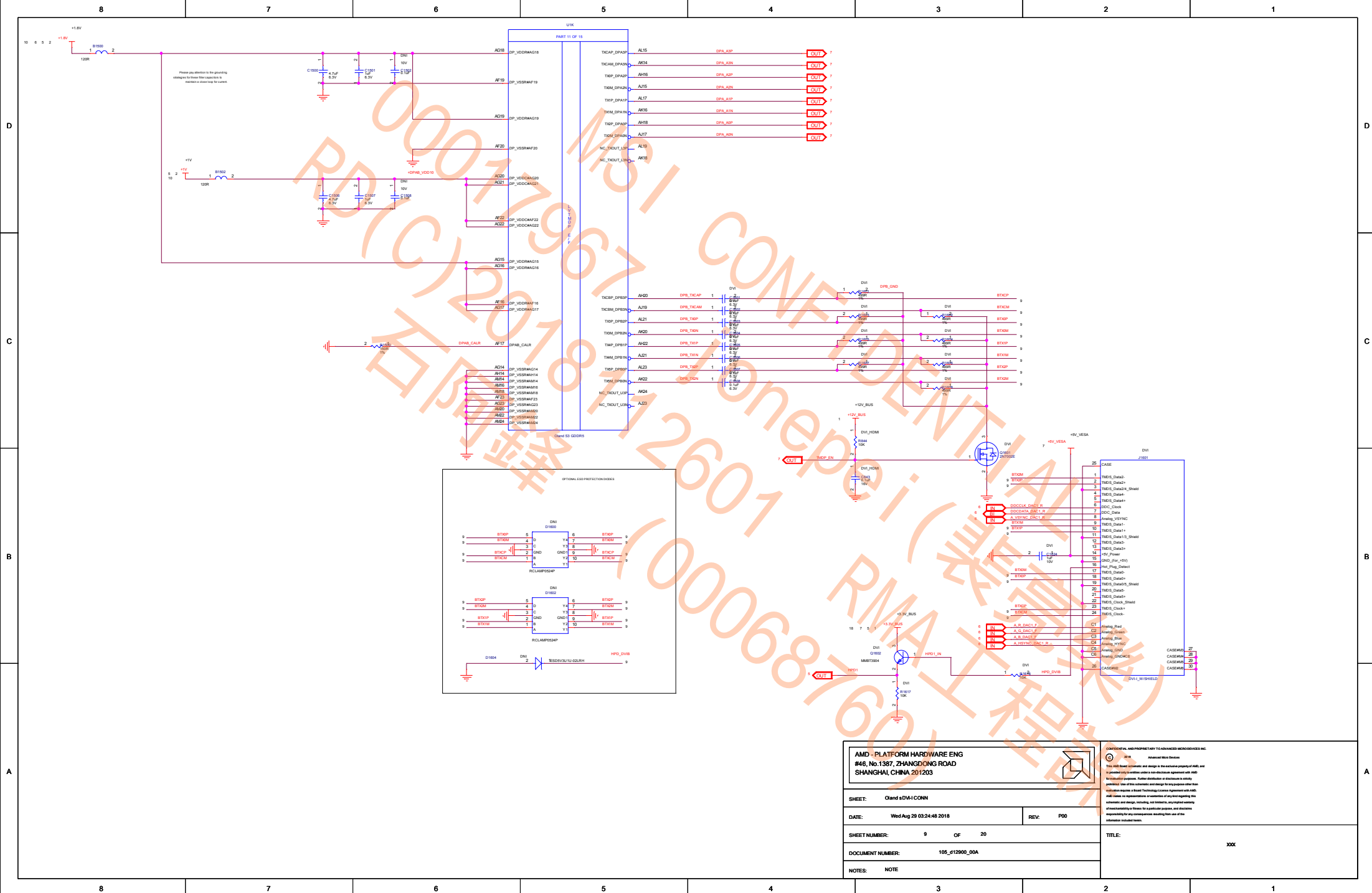


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<p>SHEET: Grand HDMOP</p>			<p>TITLE:</p>	
<p>DATE: Thu Jan 05 05:41:56 2017</p>			<p>XXX</p>	
<p>SHEET NUMBER: 7 OF 20</p>				
<p>DOCUMENT NUMBER: 106_d12900_00A</p>				





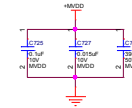
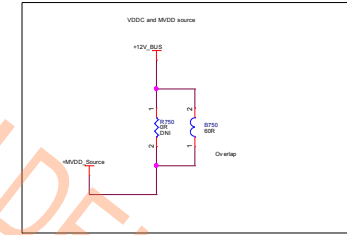
<p><b>AMD - PLATFORM HARDWARE ENG</b></p> <p><b>#46: NO.1387, ZHANGDONG ROAD</b></p> <p><b>SHANGHAI, CHINA 201203</b></p>	<div style="text-align: center;">  </div> <p><b>CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRODEVICES INC.</b></p> <p><b>TOP SECRET</b></p> <p>1. This document contains and depicts the exclusive property of AMD, and is prepared only for internal use in a non-disclosure agreement with AMD.</p> <p>2. This document contains information that is confidential to AMD, and is not to be disclosed to any third party without the prior written consent of AMD. Further disclosure or disclosure in violation of this policy may result in disciplinary action, including termination of employment.</p> <p>3. This document contains information that is confidential to AMD, and is not to be disclosed to any third party without the prior written consent of AMD. Further disclosure or disclosure in violation of this policy may result in disciplinary action, including termination of employment.</p> <p>4. This document contains information that is confidential to AMD, and is not to be disclosed to any third party without the prior written consent of AMD. Further disclosure or disclosure in violation of this policy may result in disciplinary action, including termination of employment.</p>
<p><b>SHEET:</b>      <b>Grand Unused Modules</b></p>	<p><b>DATE:</b>      <b>Wed Aug 29 03:24:48 2018</b></p>
<p><b>SHEET NUMBER:</b>      <b>8</b>      <b>OF</b>      <b>20</b></p>	<p><b>REV:</b>      <b>P00</b></p>
<p><b>DOCUMENT NUMBER:</b>      <b>105_012900_00A</b></p>	<p><b>FILE:</b>      <b>xxx</b></p>
<p><b>NOTES:</b>      <b>NOTE</b></p>	<p><b>REVISIONS:</b></p>





Regulator for MVD0

Use +VDDC\_Source to share L601 to eliminate PCB's 12V current slew rate over spec (max) 1A/us  
+MVD0\_Source



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SHEET: MVD0

DATE: Wed Aug 29 03:24:48 2018

REV: P00

SHEET NUMBER: 12 OF 20

DOCUMENT NUMBER: 105\_d12900\_00A


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TITLE: XXX

Regulator for M100

Use rVDDC\_Sense to share L801 to eliminate PCIe 12V current slew rate over spec issue(0.1A/us)  
rVDDC\_Sense

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SHEET: VDDCI	
DATE: Wed Aug 29 03:24:49 2018	REV: P00
SHEET NUMBER: 13 OF 20	
DOCUMENT NUMBER: 105_012900_00A	
NOTES: NOTE	

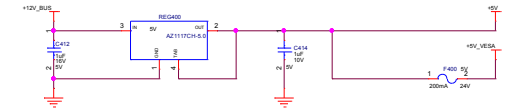
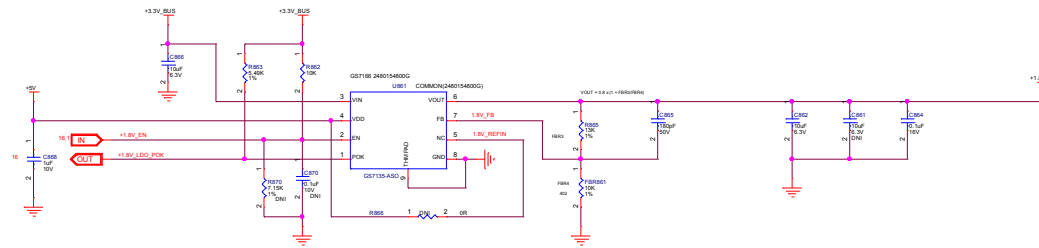
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TITLE: XXX



## Linear Regulators

LDO #2: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2% Iout = 1.6A (TbV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling



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SHEET: Linear Regulators

DATE: Thu Jan 05 05:41:58 2017

REV: P00

SHEET NUMBER: 15 OF 20

DOCUMENT NUMBER: 105\_d12900\_00A

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TITLE: \_\_\_\_\_

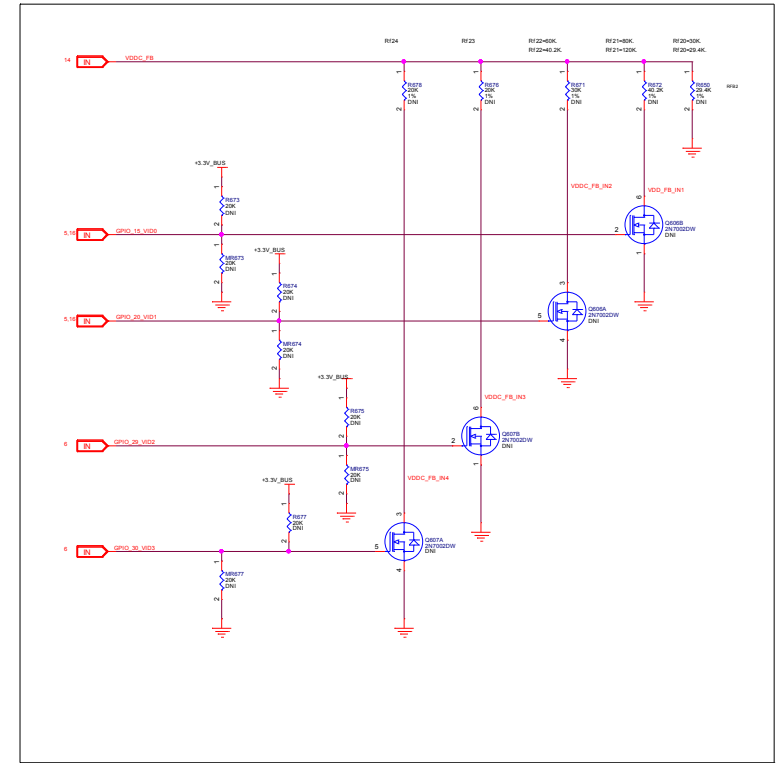
XXX

POWER SEQUENCE  
+1.8V-2.8ms->AVDD-3.4ms->0.95V-4.3ms->VDDC  
0.95V must ramp up before VDDC

[illegible]

Symbols should use uP(B010) if bigger one

1st Source: 2A00171000\_GDSB01  
2nd Source: 2A00171000\_uP(B01)



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SHEET: VDDCI	
DATE: Wed Aug 29 03:24:49 2018	REV: P00
SHEET NUMBER: 16 OF 20	
DOCUMENT NUMBER: 105_d12900_00A	
NOTES: NOTE	

TITLE:

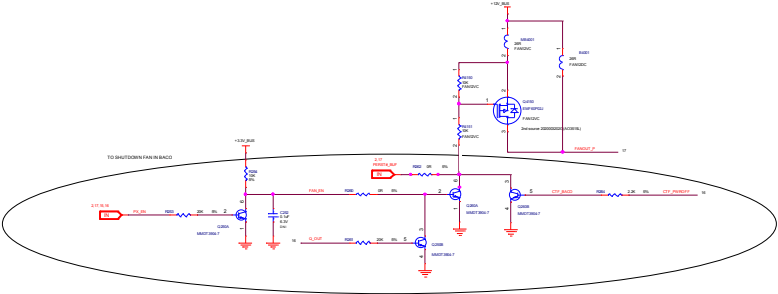
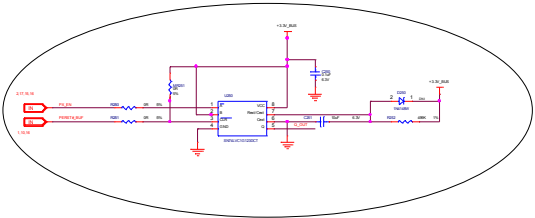
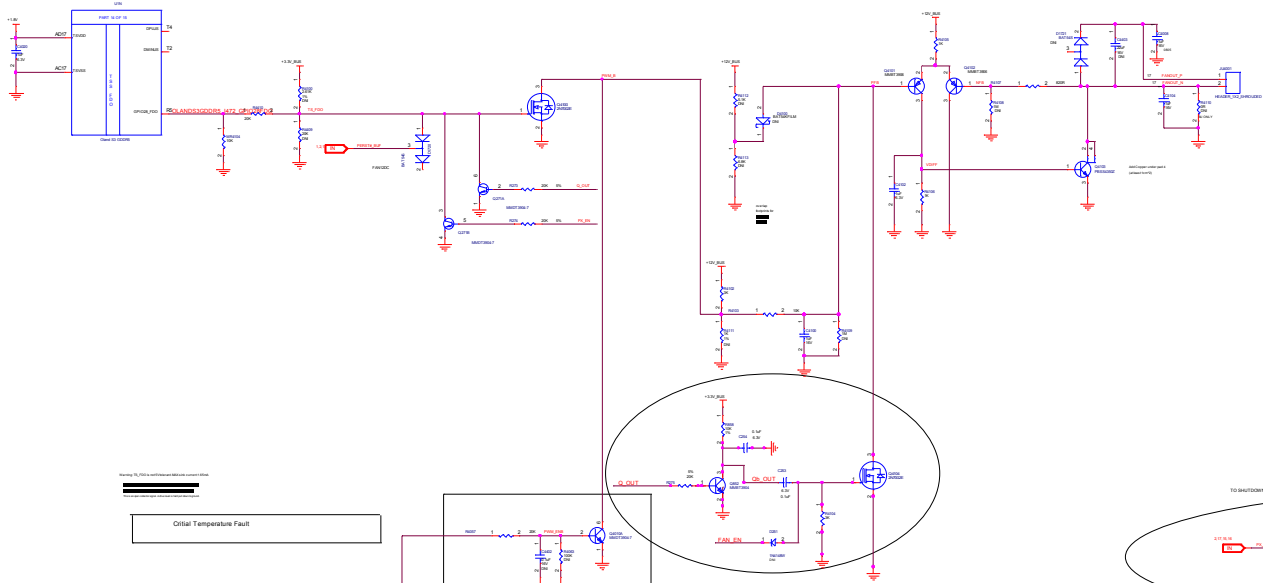
XXX



Initial PBD	CPH000-0-0 Rev.000 CPH000-0-0 Rev.000
Initial PBD (Initial PBD)	CPH000-0-0 Rev.000 CPH000-0-0 Rev.000

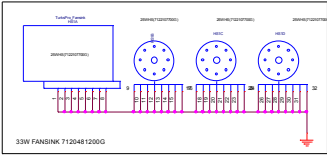
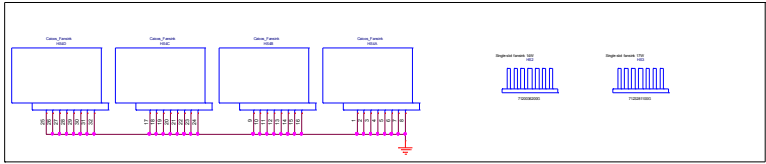
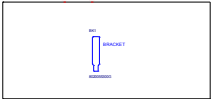
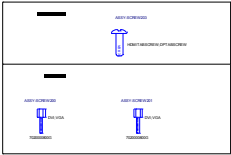


Mechanical and Thermal Management



Critical Temperature Fault

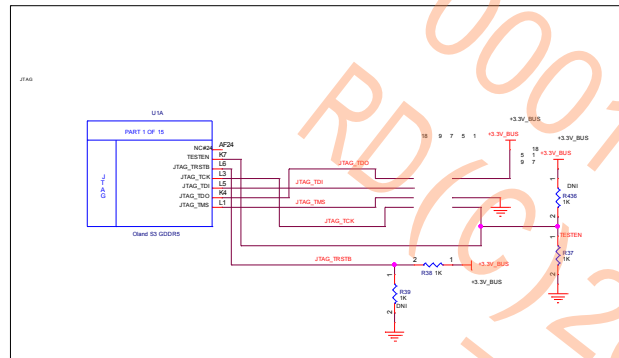
Critical Temperature Fault



Shanghai VCA Model D14	800000000
Shanghai VCA D14 Model D14	800000000
Shanghai VCA D14 Model D14	800000000
Shanghai VCA D14 Model D14	800000000

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DATE: 19th Aug 2015 14:00:00		REV: P0	
SHEET NUMBER: 17		OF 20	
DOCUMENT NUMBER: VCS0000000		TITLE: XXX	
NOTE: NOTE			

FM1 SW\_FB  
FM2 SW\_FB  
FM3 SW\_FB  
FM4 SW\_FB  
FM5 SW\_FB  
FM6 SW\_FB




TOP  
Single end  
Memory data  
45 ohm +/- 5 ohm  
5.12 mils

Bottom  
Single end  
Address trunk  
45 ohm +/- 5 ohm  
5.12 mils

TOP  
Different  
TMS  
85 ohm +/- 10 %  
4.33 mils / 5.51 mils

Bottom  
Different  
PEX PCIE  
85 ohm +/- 10 %  
4.33 mils / 5.51 mils

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<p>SHEET: Debog</p>		<p>REV: P00</p>	
<p>DATE: Thu Jan 05 06:41:58 2017</p>		<p>TITLE:</p>	
<p>SHEET NUMBER: 18 OF 20</p>		<p>XXX</p>	
<p>DOCUMENT NUMBER: 105_of12900_00A</p>			



