

V034-1A NV44 128 MB DDR2, VGA, DVI-I, SD/HDTV

HISTORY

0A base on v001 1.1 modify
removed TSOP-66 DDR change to BGA-84 DDR2.
add 2nd RT9218 for FBVDD/Q.
add APL5331 for FBVTT.
10 removed RT9218 and VTT.
add op+mos circuit.
and cost down 0402 parts change to 0603.
11 pin header change to box header for samsung request.

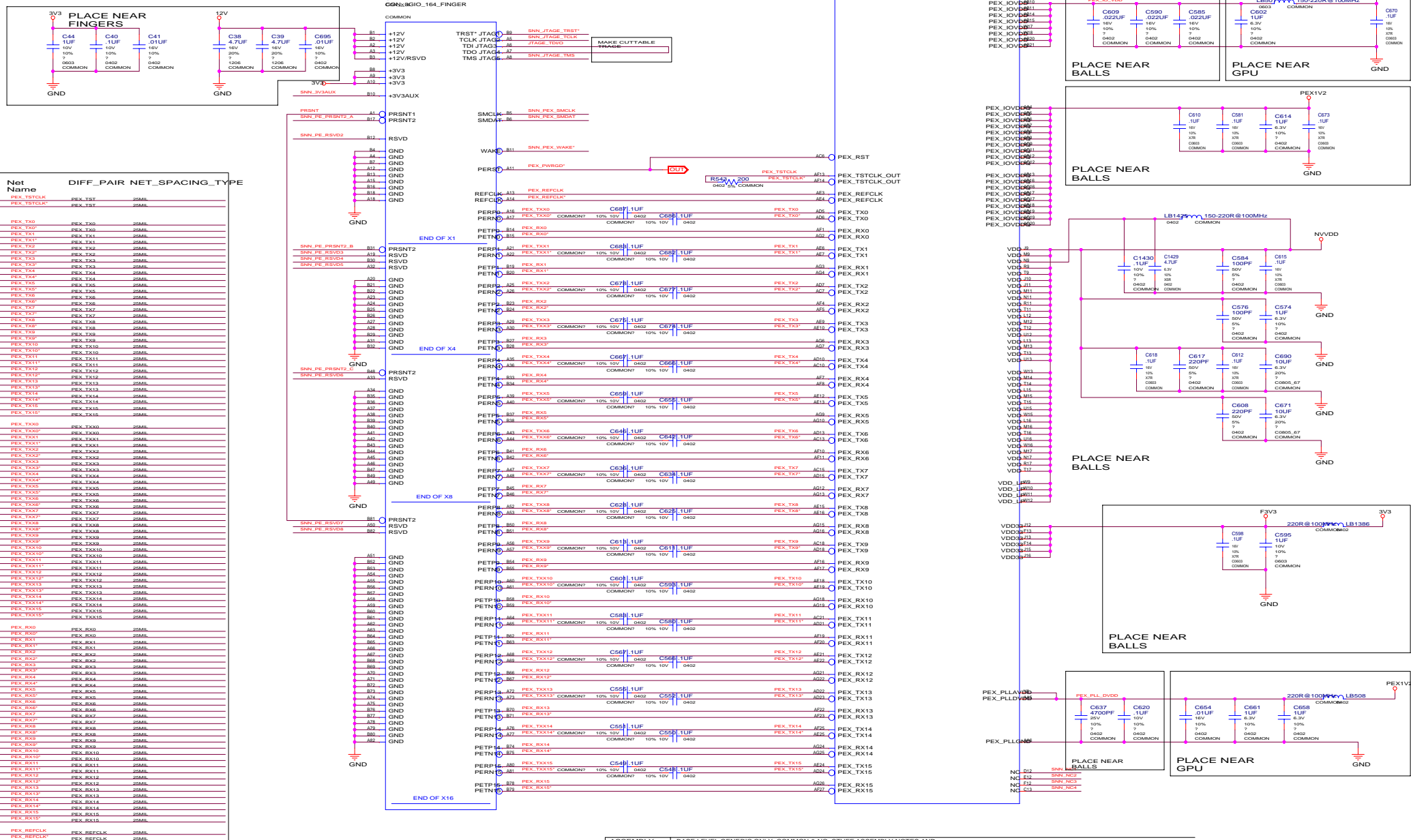
- 01. Cover page
- 02. PEX interface
- 03. GPU FB-interface
- 04. MEMORY Bit 0..31
- 05. MEMORY Bit 32..64
- 06. DAC-A, DB15 Con.
- 07. DAC-B, MUX, DB15
- 08. Internal TMDS
- 09. MIOA, MIOB
- 10. Straps
- 11. BIOS, GPIO, FAN Con.
- 12. Mini DIN
- 13. Power :NVVDD/FBVDD
- 14. Power others

A01

- 9/22/2004:
 - Changed TMDS_PLLVDD to PLLVDD
 - Added Bead option to PLLVDD rail of NV44
 - Changed RSET values for DACA and DACB
 - Changed DACB RSET FET to a dual package with GPIO11 control-Macrovision
 - Added F3V3 bypass to PLLVDD linear regulator
 - Changed location of R62

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10262-0000-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
1	0000	600-10262-0000-000	NOT FINAL
2	0001	600-10262-0001-000	<UNDEFINED>
3	0002	600-10262-0002-000	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

PEX-Interface

[illegible]

GPU: FB-Interface

UBB

BGA533_P0B_23X23MM_G3-64

COMMON

2112 FRAME_BUFFER

FB_DQ00

FB_DQ01

FB_DQ02

FB_DQ03

FB_DQ04

FB_DQ05

FB_DQ06

FB_DQ07

FB_DQ08

FB_DQ09

FB_DQ10

FB_DQ11

FB_DQ12

FB_DQ13

FB_DQ14

FB_DQ15

FB_DQ16

FB_DQ17

FB_DQ18

FB_DQ19

FB_DQ20

FB_DQ21

FB_DQ22

FB_DQ23

FB_DQ24

FB_DQ25

FB_DQ26

FB_DQ27

FB_DQ28

FB_DQ29

FB_DQ30

FB_DQ31

FB_DQ32

FB_DQ33

FB_DQ34

FB_DQ35

FB_DQ36

FB_DQ37

FB_DQ38

FB_DQ39

FB_DQ40

FB_DQ41

FB_DQ42

FB_DQ43

FB_DQ44

FB_DQ45

FB_DQ46

FB_DQ47

FB_DQ48

FB_DQ49

FB_DQ50

FB_DQ51

FB_DQ52

FB_DQ53

FB_DQ54

FB_DQ55

FB_DQ56

FB_DQ57

FB_DQ58

FB_DQ59

FB_DQ60

FB_DQ61

FB_DQ62

FB_DQ63

FB_DQ64

FB_DQ65

FB_DQ66

FB_DQ67

FB_DQ68

FB_DQ69

FB_DQ70

FB_DQ71

FB_DQ72

FB_DQ73

FB_DQ74

FB_DQ75

FB_DQ76

FB_DQ77

FB_DQ78

FB_DQ79

FB_DQ80

FB_DQ81

FB_DQ82

FB_DQ83

FB_DQ84

FB_DQ85

FB_DQ86

FB_DQ87

FB_DQ88

FB_DQ89

FB_DQ90

FB_DQ91

FB_DQ92

FB_DQ93

FB_DQ94

FB_DQ95

FB_DQ96

FB_DQ97

FB_DQ98

FB_DQ99

FB_DQ100

FB_DQ101

FB_DQ102

FB_DQ103

FB_DQ104

FB_DQ105

FB_DQ106

FB_DQ107

FB_DQ108

FB_DQ109

FB_DQ110

FB_DQ111

FB_DQ112

FB_DQ113

FB_DQ114

FB_DQ115

FB_DQ116

FB_DQ117

FB_DQ118

FB_DQ119

FB_DQ120

FB_DQ121

FB_DQ122

FB_DQ123

FB_DQ124

FB_DQ125

FB_DQ126

FB_DQ127

FB_DQ128

FB_DQ129

FB_DQ130

FB_DQ131

FB_DQ132

FB_DQ133

FB_DQ134

FB_DQ135

FB_DQ136

FB_DQ137

FB_DQ138

FB_DQ139

FB_DQ140

FB_DQ141

FB_DQ142

FB_DQ143

FB_DQ144

FB_DQ145

FB_DQ146

FB_DQ147

FB_DQ148

FB_DQ149

FB_DQ150

FB_DQ151

FB_DQ152

FB_DQ153

FB_DQ154

FB_DQ155

FB_DQ156

FB_DQ157

FB_DQ158

FB_DQ159

FB_DQ160

FB_DQ161

FB_DQ162

FB_DQ163

FB_DQ164

FB_DQ165

FB_DQ166

FB_DQ167

FB_DQ168

FB_DQ169

FB_DQ170

FB_DQ171

FB_DQ172

FB_DQ173

FB_DQ174

FB_DQ175

FB_DQ176

FB_DQ177

FB_DQ178

FB_DQ179

FB_DQ180

FB_DQ181

FB_DQ182

FB_DQ183

FB_DQ184

FB_DQ185

FB_DQ186

FB_DQ187

FB_DQ188

FB_DQ189

FB_DQ190

FB_DQ191

FB_DQ192

FB_DQ193

FB_DQ194

FB_DQ195

FB_DQ196

FB_DQ197

FB_DQ198

FB_DQ199

FB_DQ200

FB_DQ201

FB_DQ202

FB_DQ203

FB_DQ204

FB_DQ205

FB_DQ206

FB_DQ207

FB_DQ208

FB_DQ209

FB_DQ210

FB_DQ211

FB_DQ212

FB_DQ213

FB_DQ214

FB_DQ215

FB_DQ216

FB_DQ217

FB_DQ218

FB_DQ219

FB_DQ220

FB_DQ221

FB_DQ222

FB_DQ223

FB_DQ224

FB_DQ225

FB_DQ226

FB_DQ227

FB_DQ228

FB_DQ229

FB_DQ230

FB_DQ231

FB_DQ232

FB_DQ233

FB_DQ234

FB_DQ235

FB_DQ236

FB_DQ237

FB_DQ238

FB_DQ239

FB_DQ240

FB_DQ241

FB_DQ242

FB_DQ243

FB_DQ244

FB_DQ245

FB_DQ246

FB_DQ247

FB_DQ248

FB_DQ249

FB_DQ250

FB_DQ251

FB_DQ252

FB_DQ253

FB_DQ254

FB_DQ255

FB_DQ256

FB_DQ257

FB_DQ258

FB_DQ259

FB_DQ260

FB_DQ261

FB_DQ262

FB_DQ263

FB_DQ264

FB_DQ265

FB_DQ266

FB_DQ267

FB_DQ268

FB_DQ269

FB_DQ270

FB_DQ271

FB_DQ272

FB_DQ273

FB_DQ274

FB_DQ275

FB_DQ276

FB_DQ277

FB_DQ278

FB_DQ279

FB_DQ280

FB_DQ281

FB_DQ282

FB_DQ283

FB_DQ284

FB_DQ285

FB_DQ286

FB_DQ287

FB_DQ288

FB_DQ289

FB_DQ290

FB_DQ291

FB_DQ292

FB_DQ293

FB_DQ294

FB_DQ295

FB_DQ296

FB_DQ297

FB_DQ298

FB_DQ299

FB_DQ300

FB_DQ301

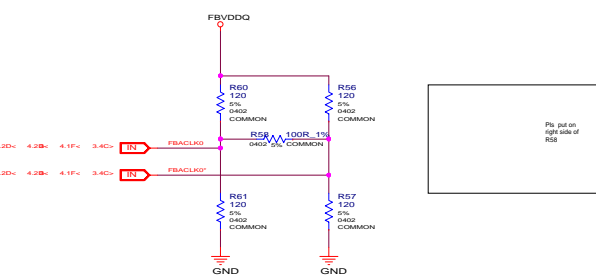
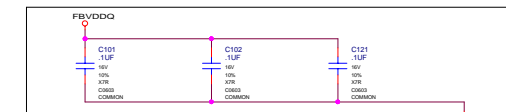
FB_DQ302

FB_DQ303

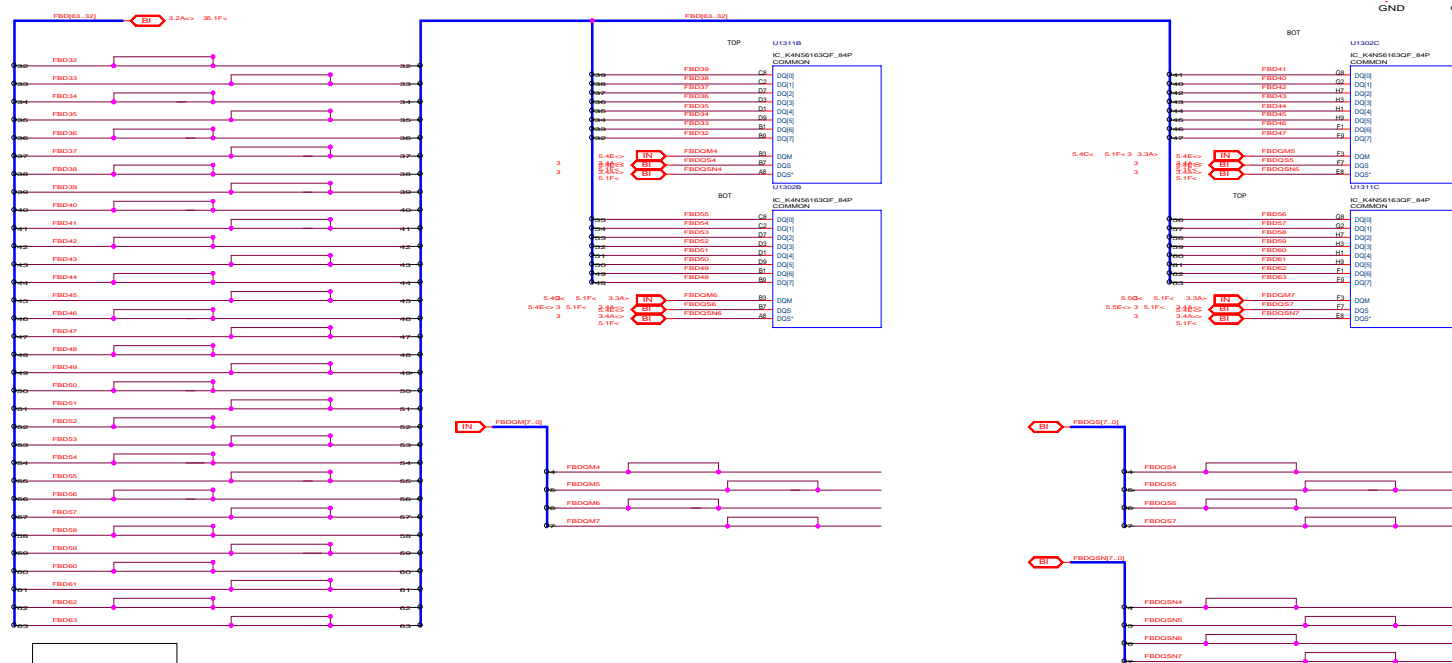
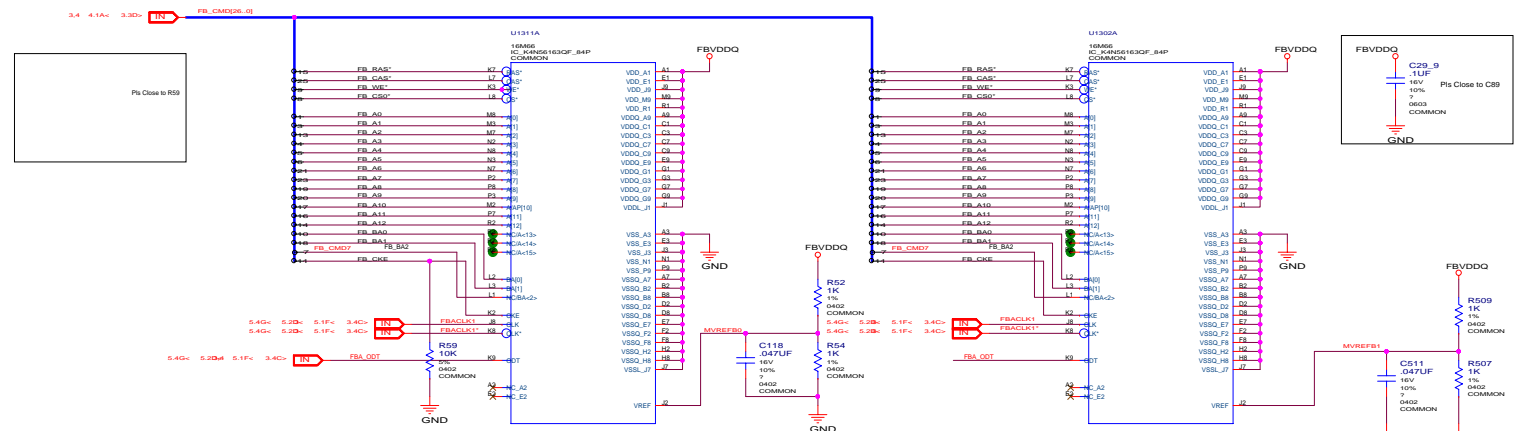
Between trace of
FB_CMD16 and
FB_CMD14



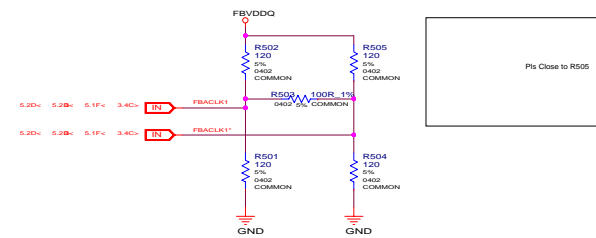
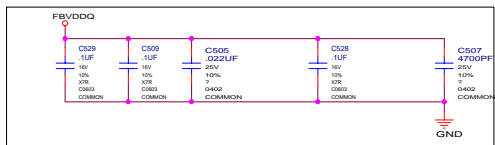
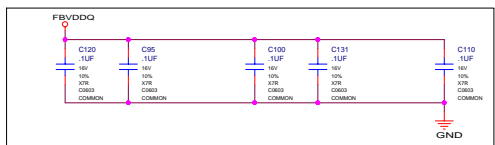
Diagram of a 5V regulator circuit. The input is PBVD00 (pin 9) connected to a 100V capacitor C535. The output is pin 1 connected to a 100V capacitor C520. The circuit includes a 100V capacitor C534, a 220V capacitor C506, and a 100V capacitor C515. All capacitors are connected to a common ground.



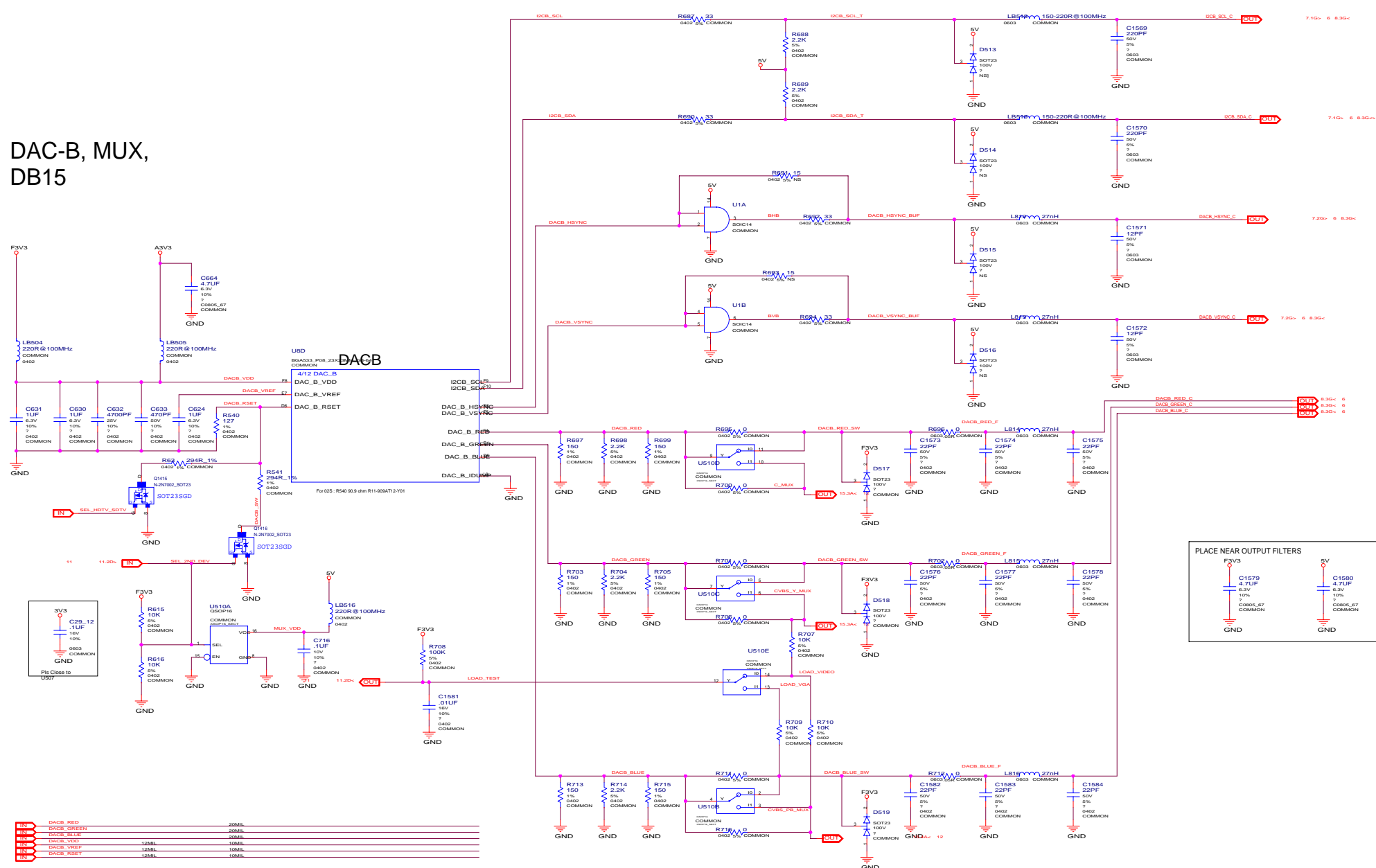
Memory Bit 32..63



Net	Diffpair	NET_SPACING_RULE
IN FBACLK1	FBACLK1	200MIL
IN FBACLK1	FBACLK1	200MIL
IN FRC003_321		100MIL
IN FRC0047_4		100MIL
IN FRC0057_4		100MIL
IN FRC00647_4		100MIL



DAC-B, MUX,
DB15

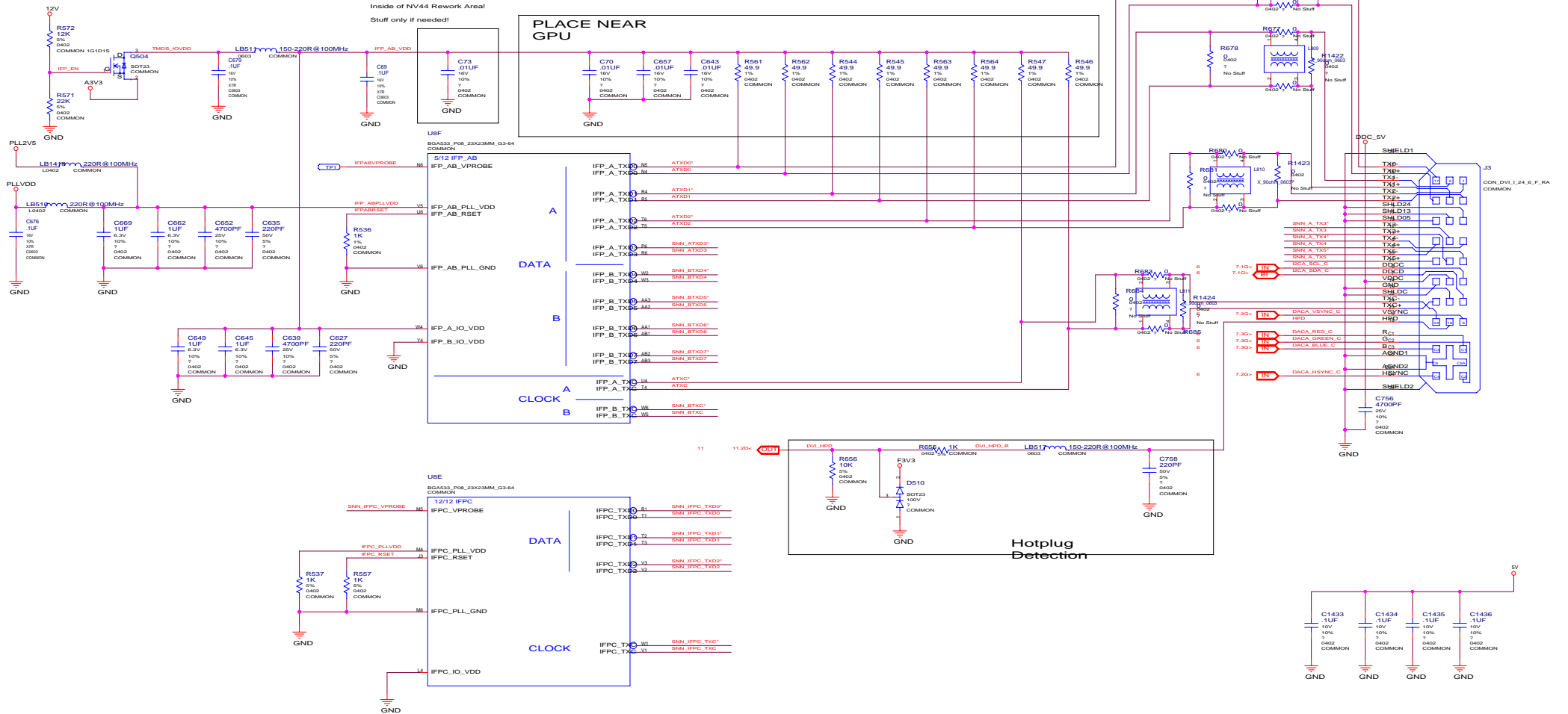
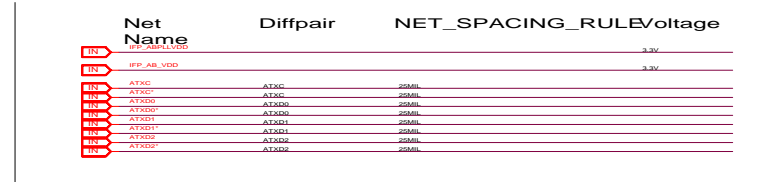


PLACE NEAR OUTPUT FILTERS

Two circuit diagrams illustrating the placement of output filters near the output. The left diagram shows a 3V3 input connected to a C1579 4.7UF 6.3V 10% capacitor, which is connected to COB05_67 COMMON and GND. The right diagram shows a 5V input connected to a C1580 4.7UF 6.3V 10% capacitor, which is connected to COB05_67 COMMON and GND.

IN	DACS_RED	208M
IN	DACS_GREEN	208M
IN	DACS_BLUE	208M
IN	DACS_VDD	128M
IN	DACS_VREF	108M
IN	DACS_RSET	108M

Internal TMDS, DVI-Connector



ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND
PAGE	BOM NOT FINAL
	TMD5

V034

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE PROVIDED UNDER A DESIGN MATERIALS LICENSE. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. NOTWITHSTANDING ANYTHING TO THE CONTRARY CONTAINED HEREIN, NVIDIA'S TOTAL LIABILITY UNDER ALL APPLICABLE LAWS, INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE OR COURSE OF PERFORMANCE, SHALL BE LIMITED TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW.

A

B

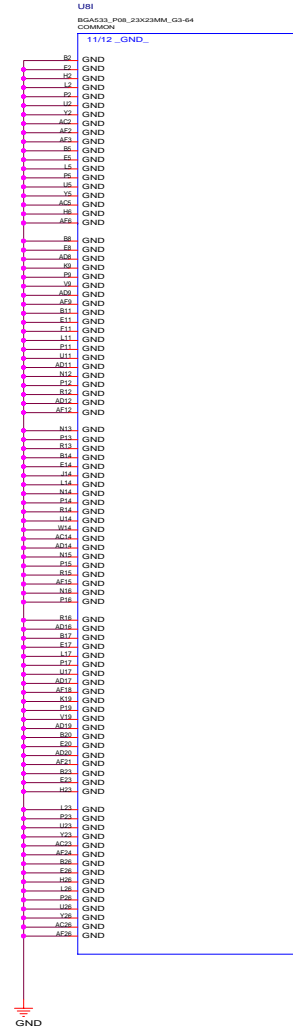
C

D

E

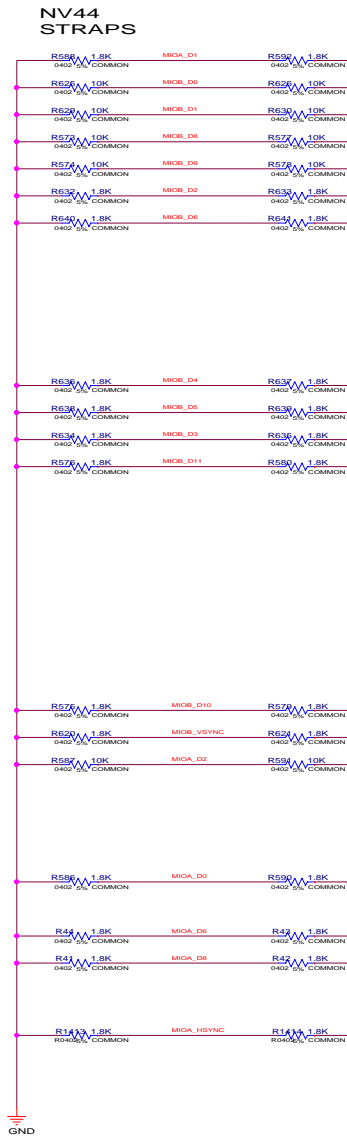
F

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE PROVIDED UNDER AN "AS IS" BASIS AND WITHOUT WARRANTY, OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. NVIDIA MAKES NO REPRESENTATION OR WARRANTY OF ANY KIND CONCERNING THE RESULTS OF THE USE OF THE MATERIALS. NVIDIA DISCLAIMS ALL WARRANTIES, INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, OR CUSTOM.

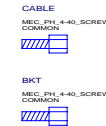
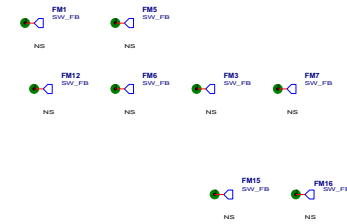


ASSEMBLY	LPC_ROM
PAGE	MIOA, MIOB Interface,

STRAPS, Mechanical Parts



Bit Signal	Values
00: PCI_AD_SWAP	0 REVERSED 1 NORMAL
01: SUB_VENDOR	0 VENDOR FROM 1 SUBVENDOR
02: RAM_CFG_0	0000 W00 0001 8Mx16DDR W01 0010 W02 0011 W03 0100 W04 0101 W05 0110 W06 0111 W07 1000 W08 1001 W09 1010 W10 1011 W11 1100 W12 1101 W13 1110 W14 1111 W15
03: RAM_CFG_1	
04: RAM_CFG_2	
05: RAM_CFG_3	
06: CRYSTAL_0	00 13.500 Mhz 01 14.31818 Mhz 10 19.200 Mhz 11 UNKNOWN
22: CRYSTAL_1	11 UNKNOWN
07: TV_MODE_0	00 2FCAM 01 4FCAM 10 WTC 11 VCL CRT
08: TV_MODE_1	
09: AGP_30_Bx	0 AGP8x 1 AGP6x 2 AGP4x 3 AGP3x 4 AGP2x 5 AGP1x 6 AGP0x 7 RESERVED 8 DISABLED
10: AGP_SBA	0 SBA 1 SBAE 2 SBAE 3 SBAE 4 SBAE 5 SBAE 6 SBAE 7 SBAE 8 SBAE 9 SBAE 10 SBAE 11 SBAE 12 SBAE 13 SBAE 14 SBAE 15 SBAE 16 SBAE 17 SBAE 18 SBAE 19 SBAE 20 SBAE 21 SBAE 22 SBAE 23 SBAE 24 SBAE 25 SBAE 26 SBAE 27 SBAE 28 SBAE 29 SBAE 30 SBAE 31 SBAE 32 SBAE 33 SBAE 34 SBAE 35 SBAE 36 SBAE 37 SBAE 38 SBAE 39 SBAE 40 SBAE 41 SBAE 42 SBAE 43 SBAE 44 SBAE 45 SBAE 46 SBAE 47 SBAE 48 SBAE 49 SBAE 50 SBAE 51 SBAE 52 SBAE 53 SBAE 54 SBAE 55 SBAE 56 SBAE 57 SBAE 58 SBAE 59 SBAE 60 SBAE 61 SBAE 62 SBAE 63 SBAE 64 SBAE 65 SBAE 66 SBAE 67 SBAE 68 SBAE 69 SBAE 70 SBAE 71 SBAE 72 SBAE 73 SBAE 74 SBAE 75 SBAE 76 SBAE 77 SBAE 78 SBAE 79 SBAE 80 SBAE 81 SBAE 82 SBAE 83 SBAE 84 SBAE 85 SBAE 86 SBAE 87 SBAE 88 SBAE 89 SBAE 90 SBAE 91 SBAE 92 SBAE 93 SBAE 94 SBAE 95 SBAE 96 SBAE 97 SBAE 98 SBAE 99 SBAE 100 SBAE 101 SBAE 102 SBAE 103 SBAE 104 SBAE 105 SBAE 106 SBAE 107 SBAE 108 SBAE 109 SBAE 110 SBAE 111 SBAE 112 SBAE 113 SBAE 114 SBAE 115 SBAE 116 SBAE 117 SBAE 118 SBAE 119 SBAE 120 SBAE 121 SBAE 122 SBAE 123 SBAE 124 SBAE 125 SBAE 126 SBAE 127 SBAE 128 SBAE 129 SBAE 130 SBAE 131 SBAE 132 SBAE 133 SBAE 134 SBAE 135 SBAE 136 SBAE 137 SBAE 138 SBAE 139 SBAE 140 SBAE 141 SBAE 142 SBAE 143 SBAE 144 SBAE 145 SBAE 146 SBAE 147 SBAE 148 SBAE 149 SBAE 150 SBAE 151 SBAE 152 SBAE 153 SBAE 154 SBAE 155 SBAE 156 SBAE 157 SBAE 158 SBAE 159 SBAE 160 SBAE 161 SBAE 162 SBAE 163 SBAE 164 SBAE 165 SBAE 166 SBAE 167 SBAE 168 SBAE 169 SBAE 170 SBAE 171 SBAE 172 SBAE 173 SBAE 174 SBAE 175 SBAE 176 SBAE 177 SBAE 178 SBAE 179 SBAE 180 SBAE 181 SBAE 182 SBAE 183 SBAE 184 SBAE 185 SBAE 186 SBAE 187 SBAE 188 SBAE 189 SBAE 190 SBAE 191 SBAE 192 SBAE 193 SBAE 194 SBAE 195 SBAE 196 SBAE 197 SBAE 198 SBAE 199 SBAE 200 SBAE 201 SBAE 202 SBAE 203 SBAE 204 SBAE 205 SBAE 206 SBAE 207 SBAE 208 SBAE 209 SBAE 210 SBAE 211 SBAE 212 SBAE 213 SBAE 214 SBAE 215 SBAE 216 SBAE 217 SBAE 218 SBAE 219 SBAE 220 SBAE 221 SBAE 222 SBAE 223 SBAE 224 SBAE 225 SBAE 226 SBAE 227 SBAE 228 SBAE 229 SBAE 230 SBAE 231 SBAE 232 SBAE 233 SBAE 234 SBAE 235 SBAE 236 SBAE 237 SBAE 238 SBAE 239 SBAE 240 SBAE 241 SBAE 242 SBAE 243 SBAE 244 SBAE 245 SBAE 246 SBAE 247 SBAE 248 SBAE 249 SBAE 250 SBAE 251 SBAE 252 SBAE 253 SBAE 254 SBAE 255 SBAE 256 SBAE 257 SBAE 258 SBAE 259 SBAE 260 SBAE 261 SBAE 262 SBAE 263 SBAE 264 SBAE 265 SBAE 266 SBAE 267 SBAE 268 SBAE 269 SBAE 270 SBAE 271 SBAE 272 SBAE 273 SBAE 274 SBAE 275 SBAE 276 SBAE 277 SBAE 278 SBAE 279 SBAE 280 SBAE 281 SBAE 282 SBAE 283 SBAE 284 SBAE 285 SBAE 286 SBAE 287 SBAE 288 SBAE 289 SBAE 290 SBAE 291 SBAE 292 SBAE 293 SBAE 294 SBAE 295 SBAE 296 SBAE 297 SBAE 298 SBAE 299 SBAE 300 SBAE 301 SBAE 302 SBAE 303 SBAE 304 SBAE 305 SBAE 306 SBAE 307 SBAE 308 SBAE 309 SBAE 310 SBAE 311 SBAE 312 SBAE 313 SBAE 314 SBAE 315 SBAE 316 SBAE 317 SBAE 318 SBAE 319 SBAE 320 SBAE 321 SBAE 322 SBAE 323 SBAE 324 SBAE 325 SBAE 326 SBAE 327 SBAE 328 SBAE 329 SBAE 330 SBAE 331 SBAE 332 SBAE 333 SBAE 334 SBAE 335 SBAE 336 SBAE 337 SBAE 338 SBAE 339 SBAE 340 SBAE 341 SBAE 342 SBAE 343 SBAE 344 SBAE 345 SBAE 346 SBAE 347 SBAE 348 SBAE 349 SBAE 350 SBAE 351 SBAE 352 SBAE 353 SBAE 354 SBAE 355 SBAE 356 SBAE 357 SBAE 358 SBAE 359 SBAE 360 SBAE 361 SBAE 362 SBAE 363 SBAE 364 SBAE 365 SBAE 366 SBAE 367 SBAE 368 SBAE 369 SBAE 370 SBAE 371 SBAE 372 SBAE 373 SBAE 374 SBAE 375 SBAE 376 SBAE 377 SBAE 378 SBAE 379 SBAE 380 SBAE 381 SBAE 382 SBAE 383 SBAE 384 SBAE 385 SBAE 386 SBAE 387 SBAE 388 SBAE 389 SBAE 390 SBAE 391 SBAE 392 SBAE 393 SBAE 394 SBAE 395 SBAE 396 SBAE 397 SBAE 398 SBAE 399 SBAE 400 SBAE 401 SBAE 402 SBAE 403 SBAE 404 SBAE 405 SBAE 406 SBAE 407 SBAE 408 SBAE 409 SBAE 410 SBAE 411 SBAE 412 SBAE 413 SBAE 414 SBAE 415 SBAE 416 SBAE 417 SBAE 418 SBAE 419 SBAE 420 SBAE 421 SBAE 422 SBAE 423 SBAE 424 SBAE 425 SBAE 426 SBAE 427 SBAE 428 SBAE 429 SBAE 430 SBAE 431 SBAE 432 SBAE 433 SBAE 434 SBAE 435 SBAE 436 SBAE 437 SBAE 438 SBAE 439 SBAE 440 SBAE 441 SBAE 442 SBAE 443 SBAE 444 SBAE 445 SBAE 446 SBAE 447 SBAE 448 SBAE 449 SBAE 450 SBA

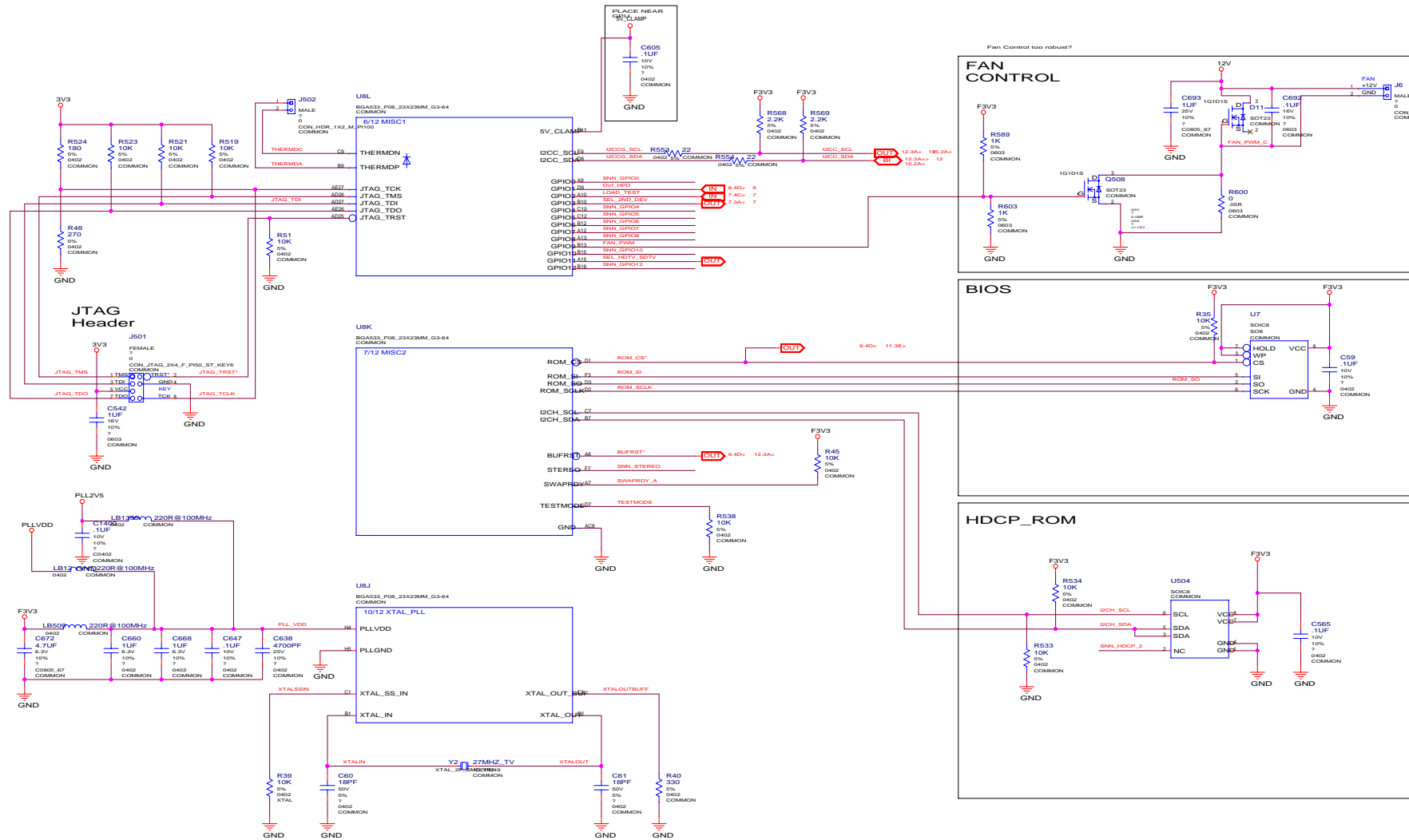


ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND
PAGE	BCM NOT FINAL STRAPS, Mechanical

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE
 BEING PROVIDED AS IS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS. NVIDIA ASSUMES NO LIABILITY FOR DAMAGES, INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, OR COURSE OF PERFORMANCE.

XTAL, GPIO, BIOS, Fan Control, JTAG Headers

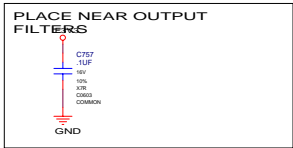
Net Name	NET_PHYSICAL_TYPE	NET_SPACING_RULE
PLVDD	5MIL_TRACE	20MIL
PLVDD	5MIL_TRACE	20MIL
PLVDD	12MIL_TRACE	10MIL
DMB_PLVDD	12MIL_TRACE	10MIL



ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND
PAGE	PCB NOT FINAL XTAL, GPIO, BIOS, Fan Control, JTAG Headers

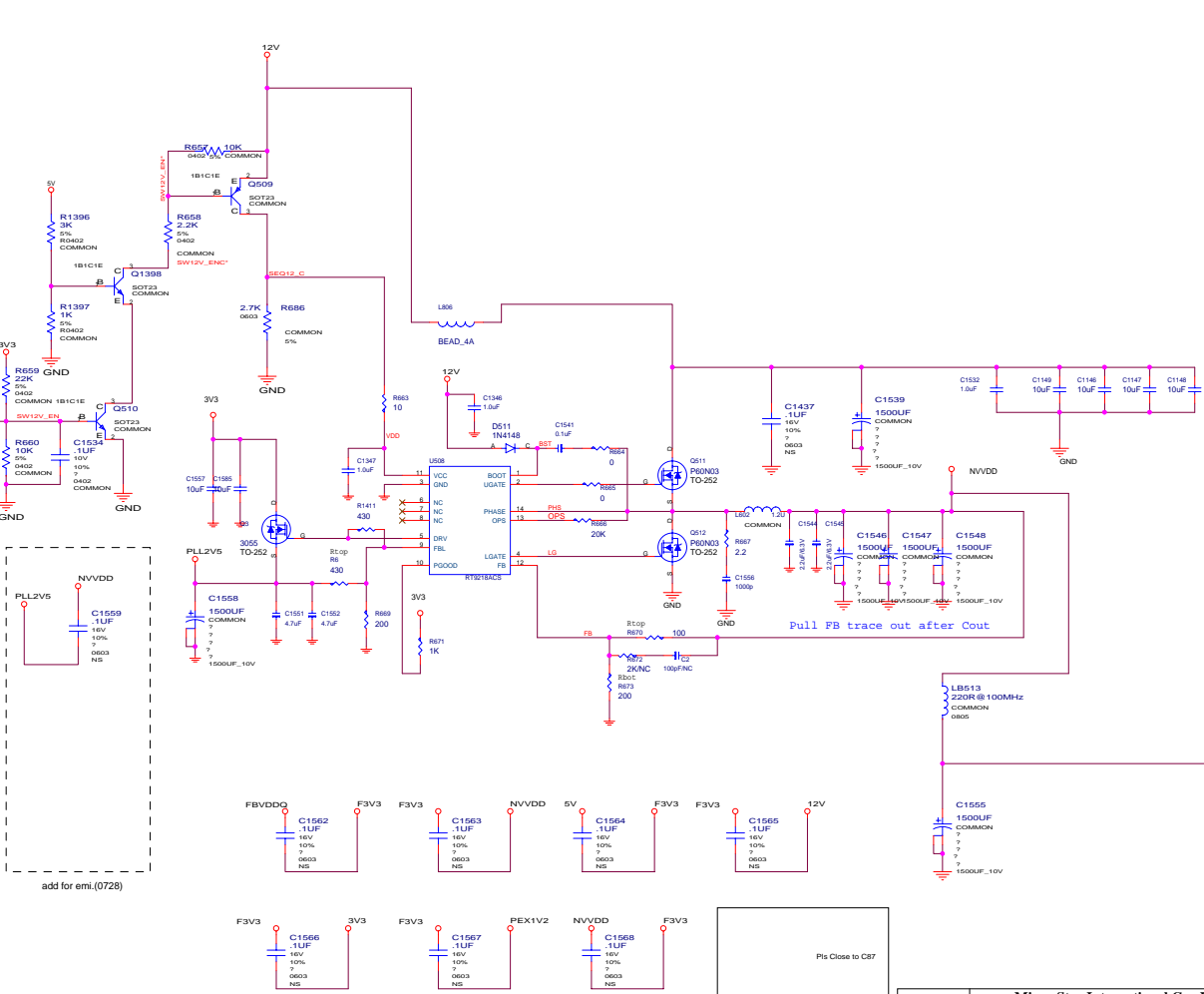
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE
UNWARRANTED AND AS AVAILABLE WITH NO WARRANTIES, EXPRESSED OR IMPLIED, STATUTORY OR OTHERWISE, WITH RESPECT TO THE MATERIALS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE, WITH RESPECT TO THE MATERIALS.
 IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE

~~TRADE PRACTICE, OR INDUSTRY STANDARDS~~



CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR THE WORKMANSHIP AND EXPRESSLY DISCLAIMS ALL WARRANTIES, INCLUDING BUT NOT LIMITED TO, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

PowerSupplyII: 5V, DDC5V, A3V3, F3V3, TMD5_PLLVDD



FBVDDQ

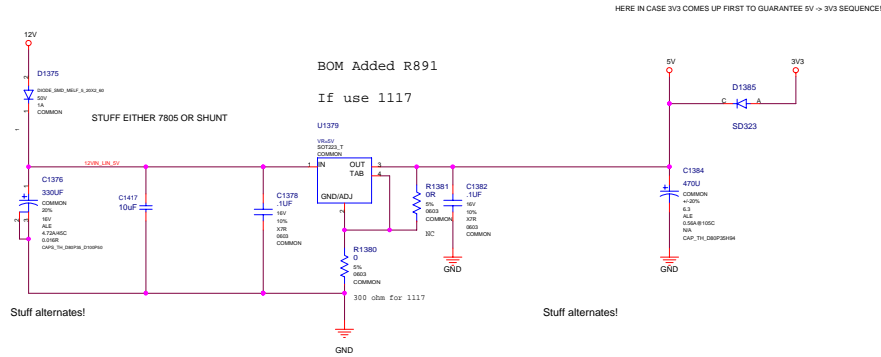
$$V_{out} = V_{Ref} \cdot (1 + R_{top}/R_{bot})$$

$1.8V = 0.8V \cdot (1 + (200/160)) \quad (RT9218)$

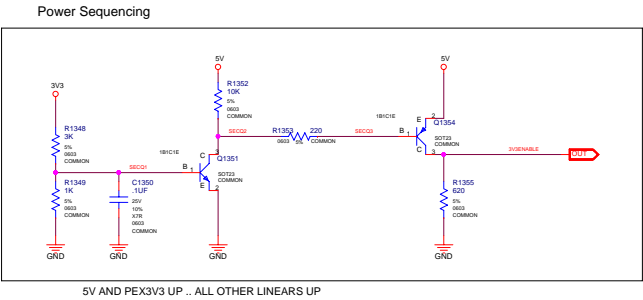
$2.0V = 0.8V \cdot (1 + (240/160)) \quad (RT9218)$

14 Others Power Supply (Linears)

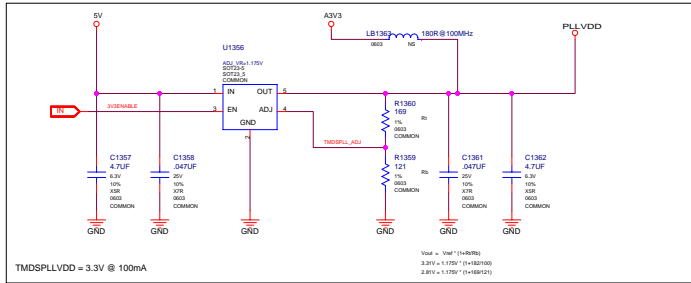
5V,FBVDDQ,A3V3,3V3,TMDS_PLLVDD,TMDS_IOVDD,FBVTT



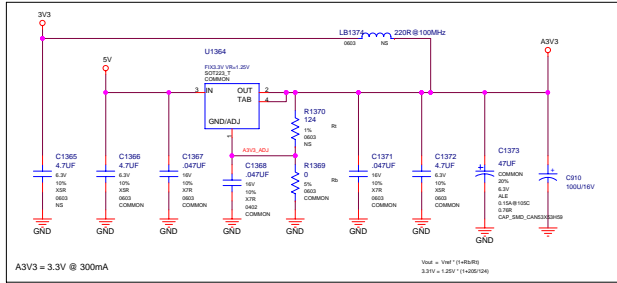
5V LOW COST REGULATOR



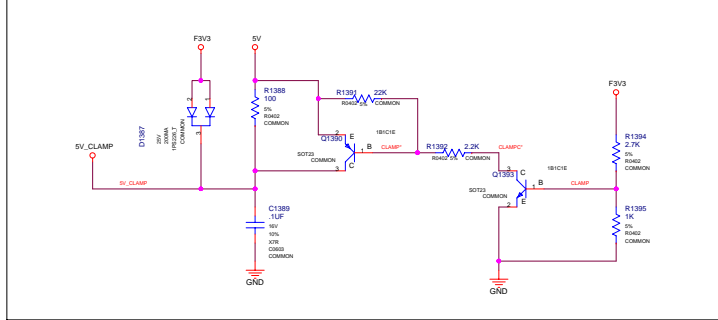
TMDS PLL Supply



A3V3 Power Supply



5V_CLAMP



Micro-Star International Co., LTD.

V034

Size Document Number
Custom

Date Wednesday, December 06, 2006 Sheet 14 of 14