

MS-V046 VER 10

Base on P295-A00 DESIGN NV43 300/267MHZ 128MB/256MB/512MB DDR2 84-FBGA to modify V046

PAGE SUMMARY:

Page1: P295 Overview
Page2: PCI EXPRESS, NVVDD, VDD33
Page3: FB BANK A, FBVTT TERMINATIONS, FBVDDQ DECOUPLING
Page4: FB BANK C, FBVTT TERMINATIONS
Page5: MEMORY PARTITION A 0..31
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Page9: GPU GND
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Page11: DACB - TVOUT, VIDEO IN
Page12: DACC - VGA
Page13: STRAPS, FANSINK, MECHANICALS
Page14: GPIO, HDCP ROM, VBIOS ROM, FAN CONTROL
Page15: INTERNAL TMDS LINK A/B
Page16: INTERNAL TMDS LINK C/D
Page17: MIOA, MIOB, NVPLL
Page18: Power Supply (Linears)
Page19: FBVDD with MS11 HW monitor
Page20: NVVDD with MS11 GPIO CTRLer

Page Changed:


Chage FBVDD & NVVDD Power solution for MS11 20050829
Adding DACA_C RSET SETTING 20050829
Adding Bridge & termination resister for DVI 20050829
Pull 3v3 for GPIO30-33 of GPIO controller 20050831

- 20051031**
- 1.Page 10&15 : Modify DACA RGB Net J4,J502 RGB Net need connect,
 - 2.Page 12&16 : Modify I2CB_SDA and I2CB_SCL Net
 - 3.Page 19 : Memory sence circuit CSP & CSN swap
 - 4.Page 19 : Modify Capacitor 1,2 to C1111,C2222
 - 5.For G73 reserve circuit
 - a.2.5V
 - a.2.5V

Suggestion : remove MS11 FBVDD VID control

-20051125

- Reserve G73 circuit**
- Reserve FBVTT circuit**
- Reserve HDCP circuit**

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MS-V046			
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16X PCIe Interface

NET RULES

NET	DIFFER	IMPEDANCE	NO. CRITICAL NET
PEX_100	DIFFER	100OHM	1
PEX_101	DIFFER	100OHM	1
PEX_102	DIFFER	100OHM	1
PEX_103	DIFFER	100OHM	1
PEX_104	DIFFER	100OHM	1
PEX_105	DIFFER	100OHM	1
PEX_106	DIFFER	100OHM	1
PEX_107	DIFFER	100OHM	1
PEX_108	DIFFER	100OHM	1
PEX_109	DIFFER	100OHM	1
PEX_110	DIFFER	100OHM	1
PEX_111	DIFFER	100OHM	1
PEX_112	DIFFER	100OHM	1
PEX_113	DIFFER	100OHM	1
PEX_114	DIFFER	100OHM	1
PEX_115	DIFFER	100OHM	1
PEX_116	DIFFER	100OHM	1
PEX_117	DIFFER	100OHM	1
PEX_118	DIFFER	100OHM	1
PEX_119	DIFFER	100OHM	1
PEX_120	DIFFER	100OHM	1
PEX_121	DIFFER	100OHM	1
PEX_122	DIFFER	100OHM	1
PEX_123	DIFFER	100OHM	1
PEX_124	DIFFER	100OHM	1
PEX_125	DIFFER	100OHM	1
PEX_126	DIFFER	100OHM	1
PEX_127	DIFFER	100OHM	1
PEX_128	DIFFER	100OHM	1
PEX_129	DIFFER	100OHM	1
PEX_130	DIFFER	100OHM	1
PEX_131	DIFFER	100OHM	1
PEX_132	DIFFER	100OHM	1
PEX_133	DIFFER	100OHM	1
PEX_134	DIFFER	100OHM	1
PEX_135	DIFFER	100OHM	1
PEX_136	DIFFER	100OHM	1
PEX_137	DIFFER	100OHM	1
PEX_138	DIFFER	100OHM	1
PEX_139	DIFFER	100OHM	1
PEX_140	DIFFER	100OHM	1
PEX_141	DIFFER	100OHM	1
PEX_142	DIFFER	100OHM	1
PEX_143	DIFFER	100OHM	1
PEX_144	DIFFER	100OHM	1
PEX_145	DIFFER	100OHM	1
PEX_146	DIFFER	100OHM	1
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PEX_194	DIFFER	100OHM	1
PEX_195	DIFFER	100OHM	1
PEX_196	DIFFER	100OHM	1
PEX_197	DIFFER	100OHM	1
PEX_198			

[illegible]

FB PARTITION A

LIB1

BOARD: P41 3000000

COMMON

274 FBA

1 FBA00

2 FBA01

3 FBA02

4 FBA03

5 FBA04

6 FBA05

7 FBA06

8 FBA07

9 FBA08

10 FBA09

11 FBA10

12 FBA11

13 FBA12

14 FBA13

15 FBA14

16 FBA15

17 FBA16

18 FBA17

19 FBA18

20 FBA19

21 FBA20

22 FBA21

23 FBA22

24 FBA23

25 FBA24

26 FBA25

27 FBA26

28 FBA27

29 FBA28

30 FBA29

31 FBA30

32 FBA31

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284 FBA283

285 FBA284

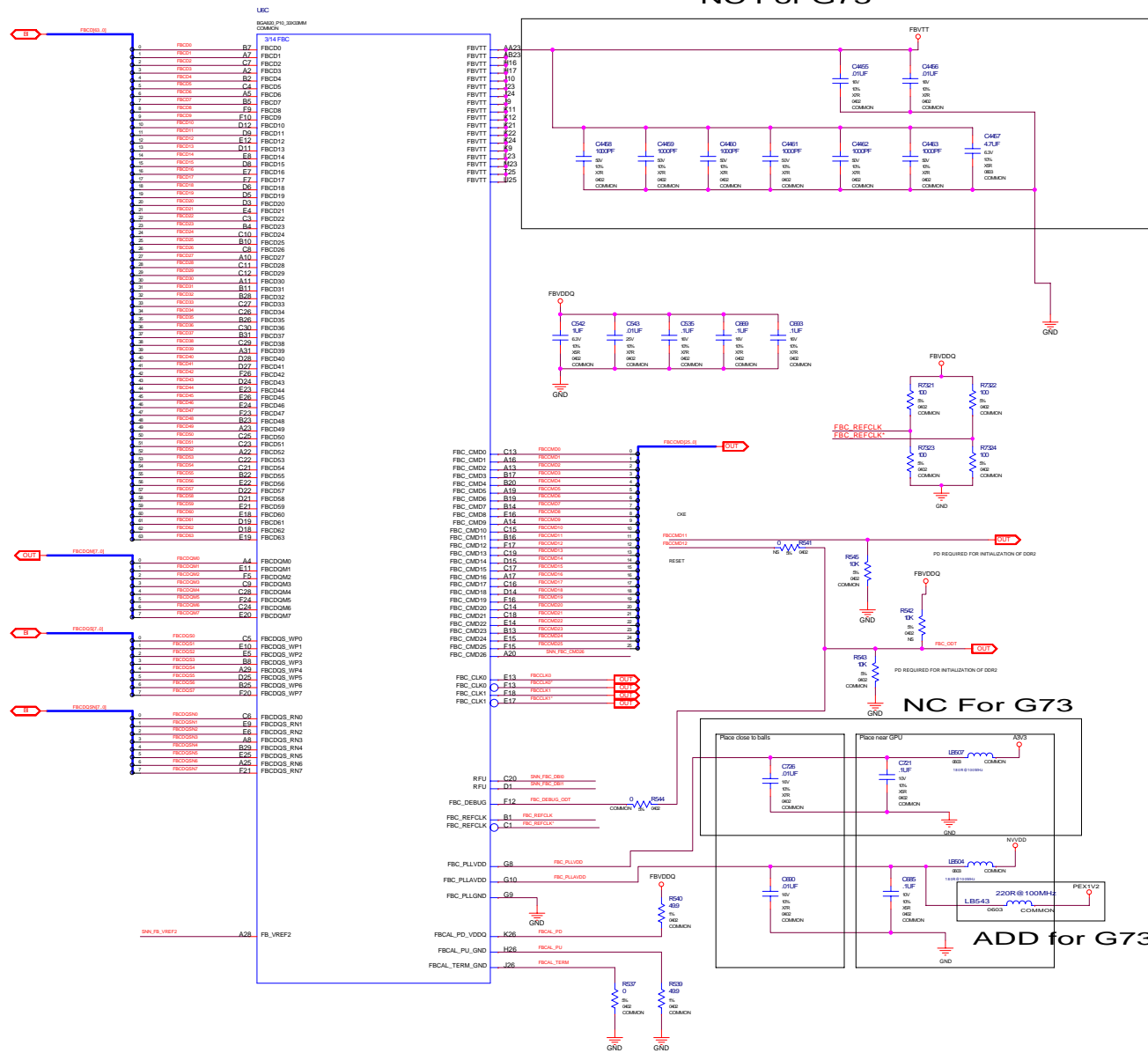
286 FBA285

287 FBA286

288 FBA287

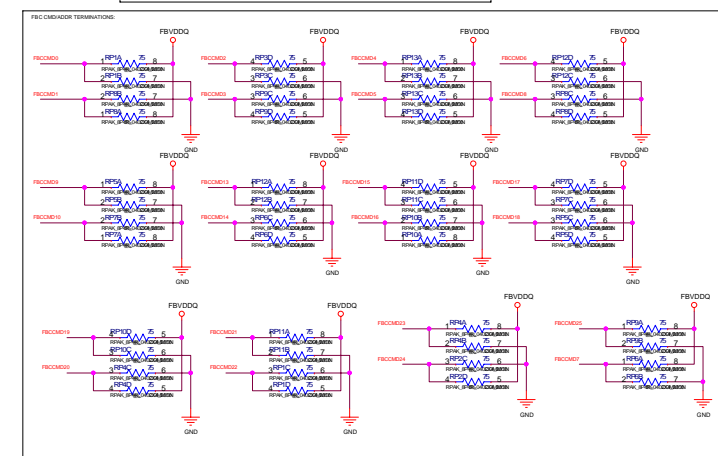
FB PARTITION C

NC For G73

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DOR2 OPERATION

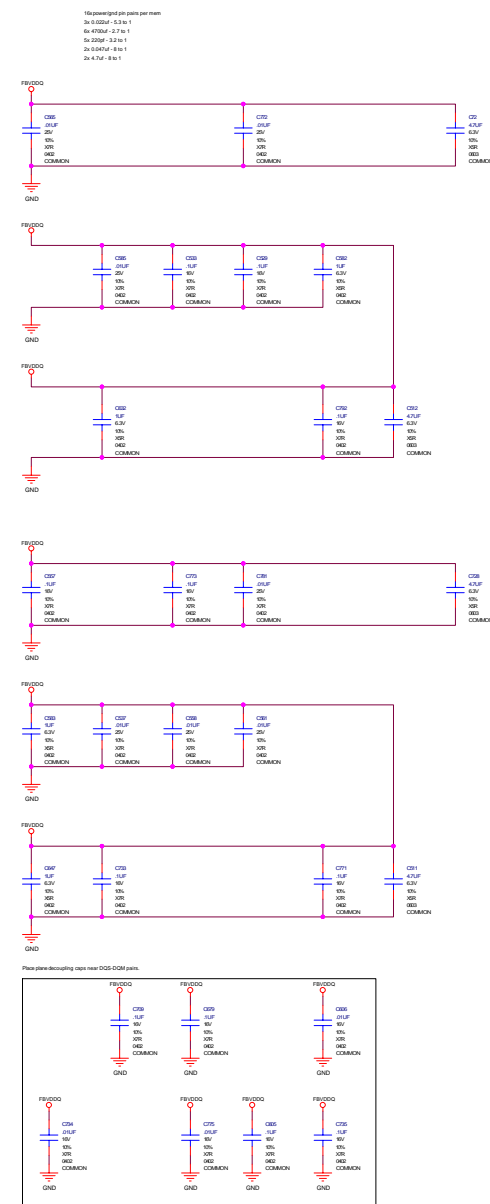
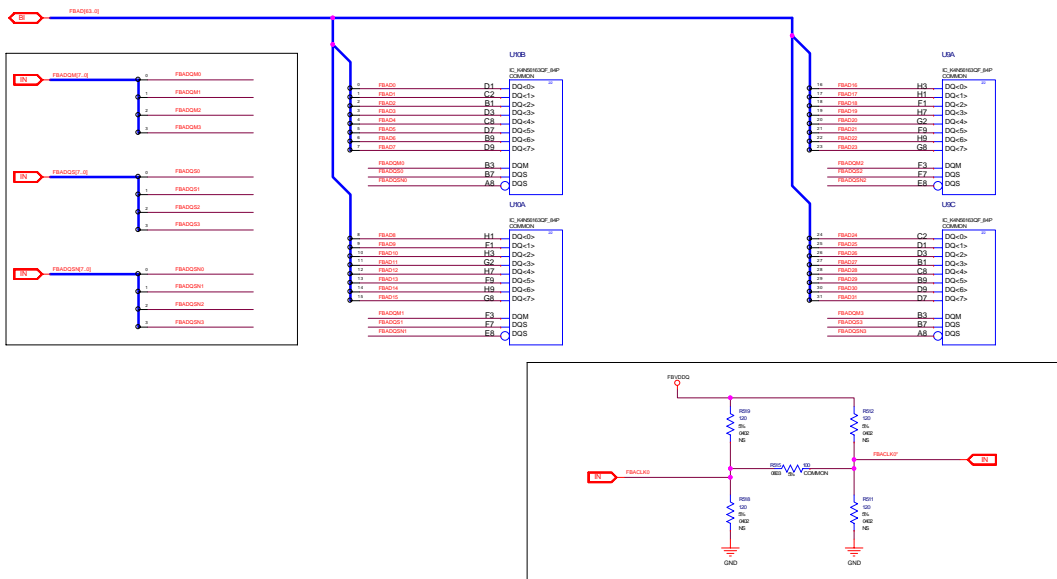
- 1) During initialization CKE and ODT low
- 2) Runtime - CKE high and ODT operated by debug state machine
- 3) No termination spike for CKE or DEBUG pins



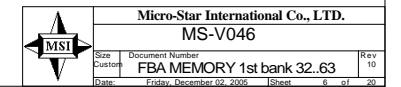
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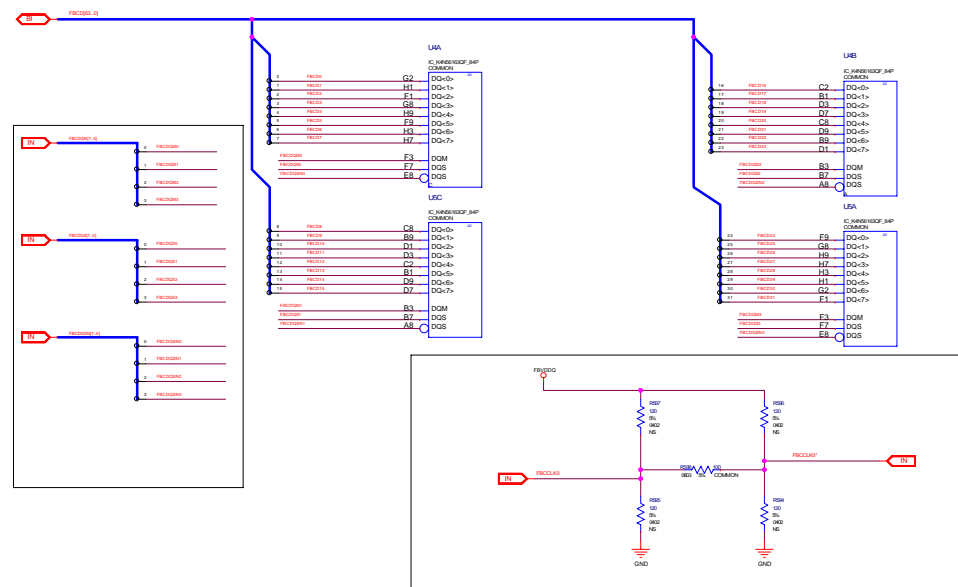
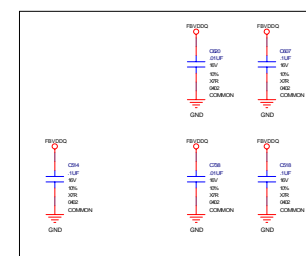
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

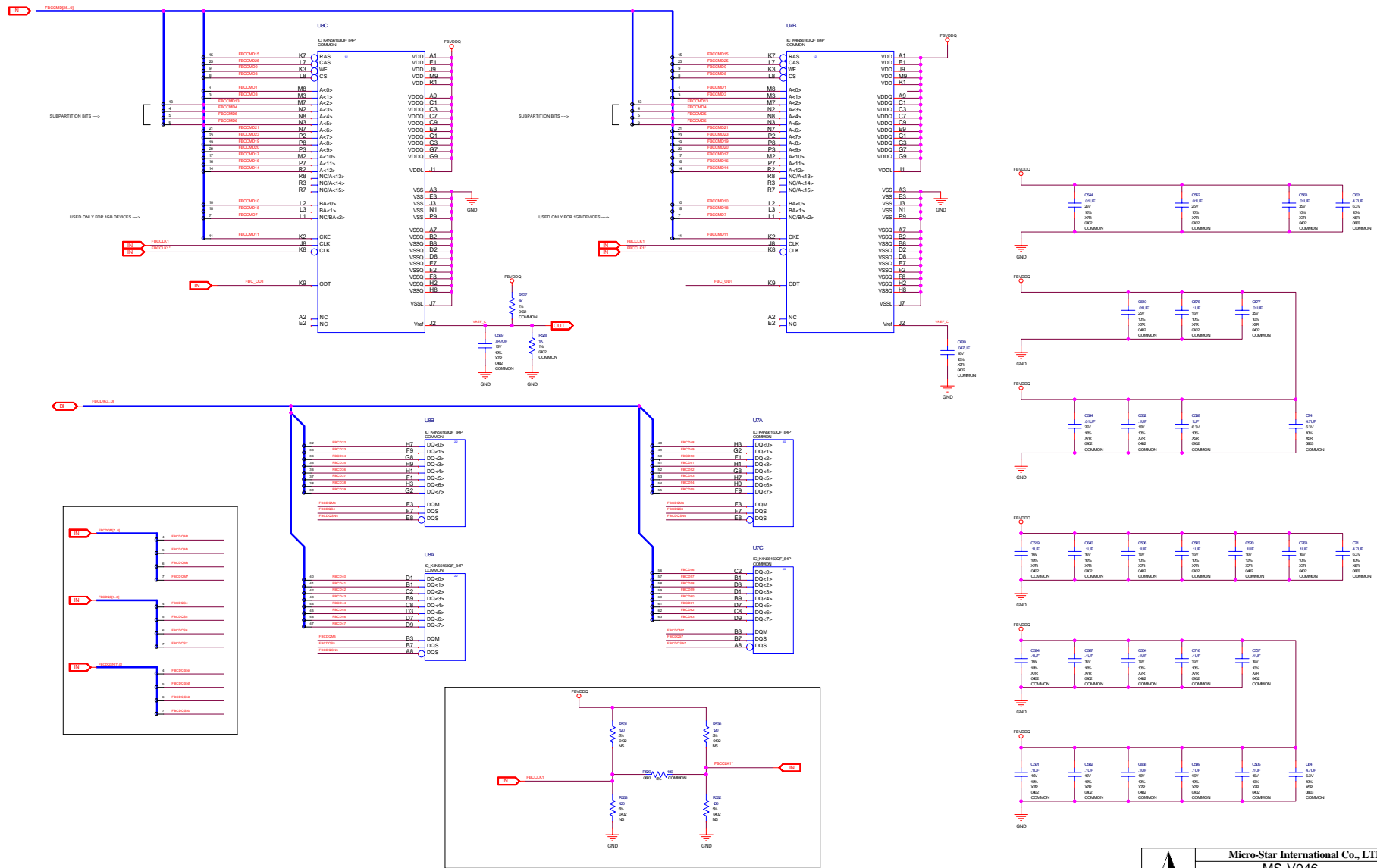


PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

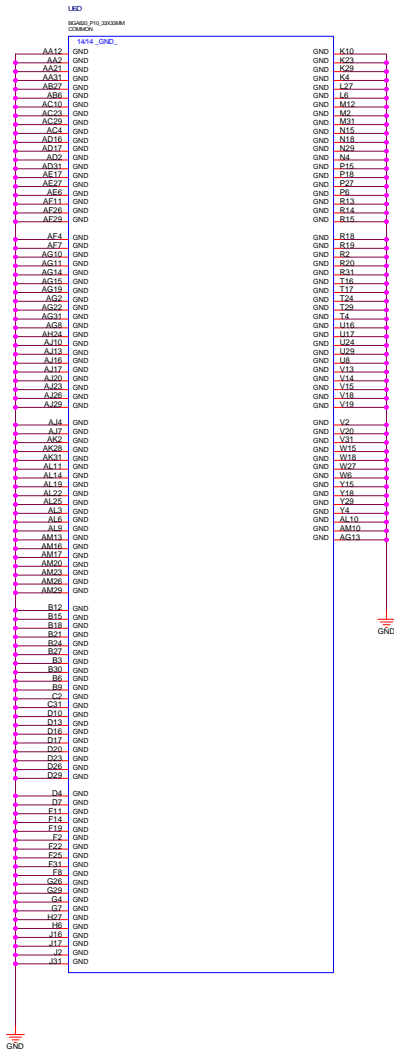


FBC MEMORY 2nd bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



GND



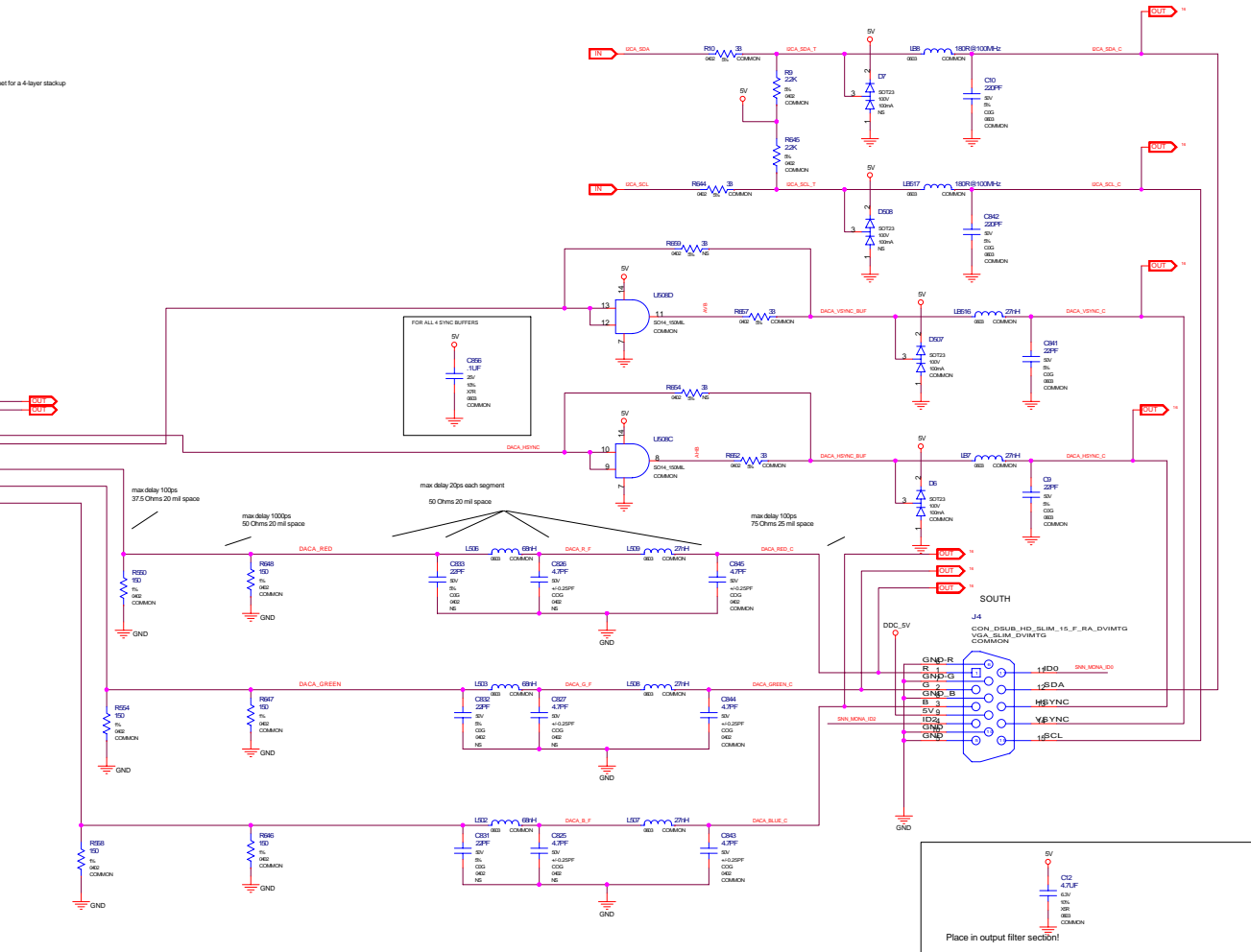
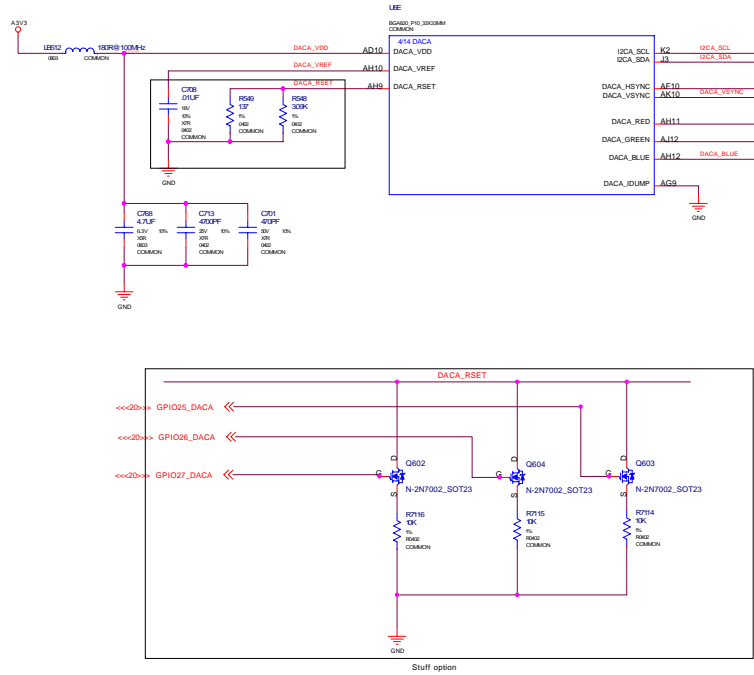
DACA VGA

NET_NAME	MIN_LINE_WIDTH	NY_CRITICAL_NET	NY_IMPEDANCE
DACA_SCL			
DACA_SDA			
DACA_HSYNC		2	50OHM
DACA_VSYNC		2	50OHM
DACA_VSYNC_BUF		2	50OHM
DACA_VSYNC_BUF		2	50OHM
DACA_VSYNC_C		2	50OHM
DACA_VSYNC_C		2	50OHM
AVS		2	50OHM
AVS		2	50OHM
DACA_RED		1	50OHM
DACA_GREEN		1	50OHM
DACA_BLUE		1	50OHM
DACA_R_F		1	50OHM
DACA_G_F		1	50OHM
DACA_B_F		1	50OHM
DACA_RED_C		1	50OHM
DACA_GREEN_C		1	50OHM
DACA_BLUE_C		1	50OHM
DACA_VDD			
DACA_VREF			
DACA_RESET			

Note that this impedance is the highest one on the v-net for a 4-layer stackup

Change for G73

C708 0.1u
R549 124ohm
R548 1.78Kohm

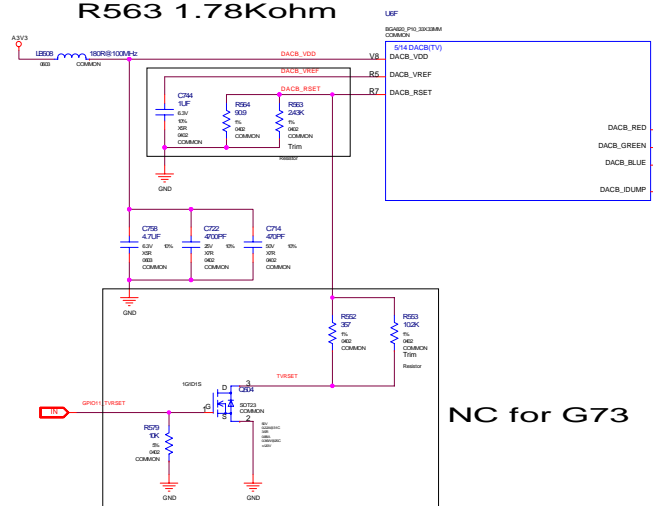


NET_NAME	MIN_LINE_WIDTH	NV_CRITICAL_NET	NV_IMPEDANCE
DACB_C_OUT		1	50OHM
DACB_CIN_VDD1		1	50OHM
DACB_PB_OUT		1	50OHM
DDOUT_C		1	50OHM
DDOUT_C		1	50OHM
PDOUT_C		1	50OHM
DACB_VDD	0.2		
DACB_VREF	0.4		
DACB_RST	0.4		
TURST	0.4		
DD_C	0.2		
DD_Y	0.2		

Note that this is the highest impedance on the knot

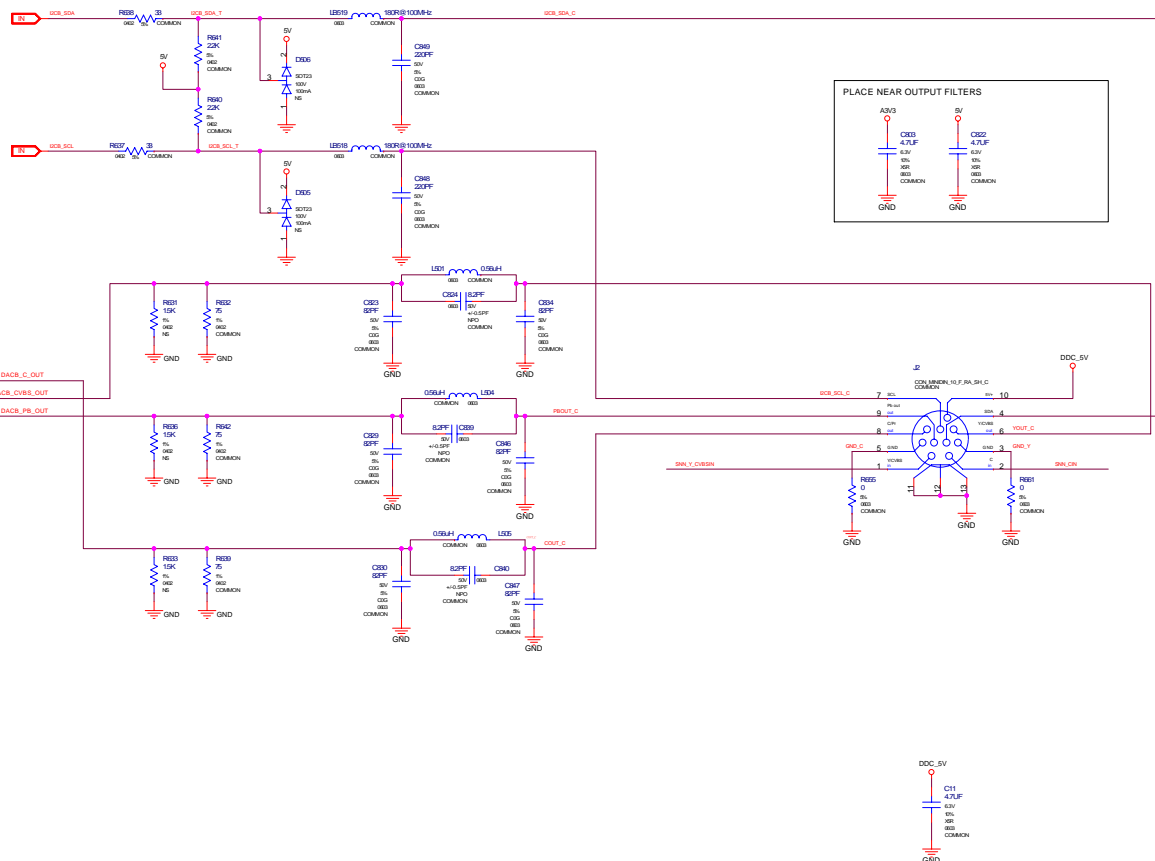
Change for G73

C744 0.1u
R564 124ohm
R563 1.78Kohm



NC for G73

DACB TVOUT



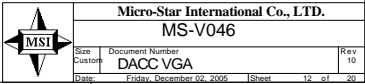
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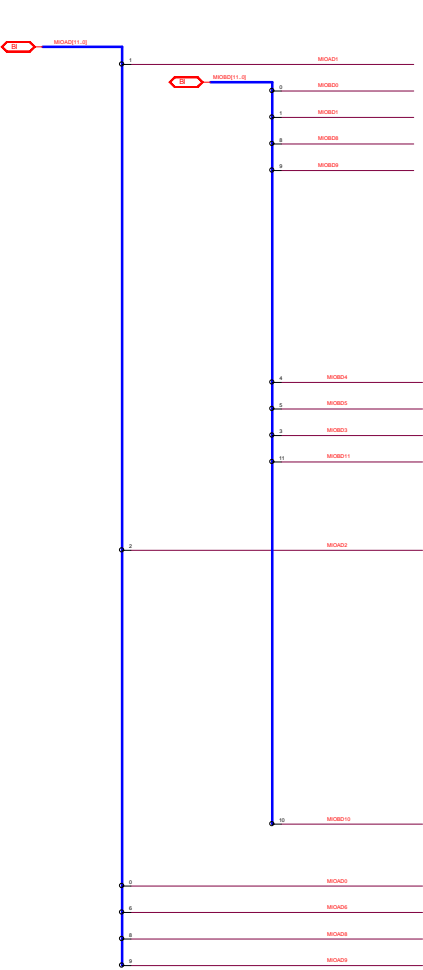
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Custom	DACB TVOUT	
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







DACC VGA

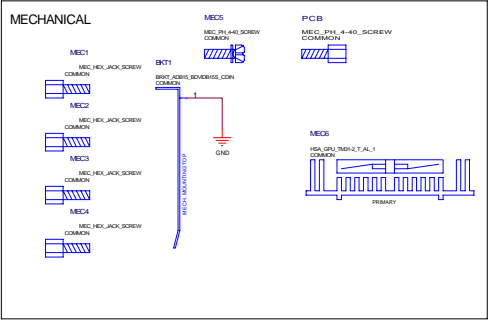
C747 0.1u
R566 124ohm
R568 1.78Kohm



STRAPS



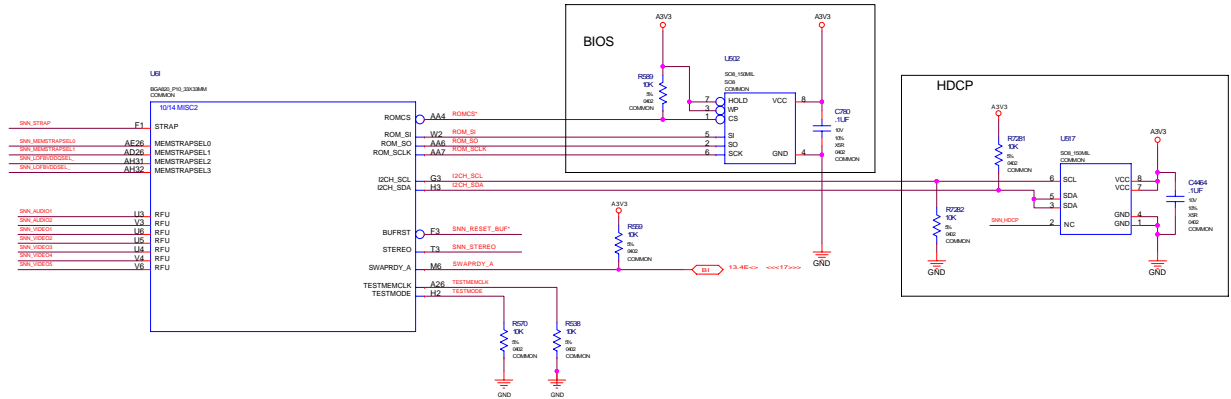
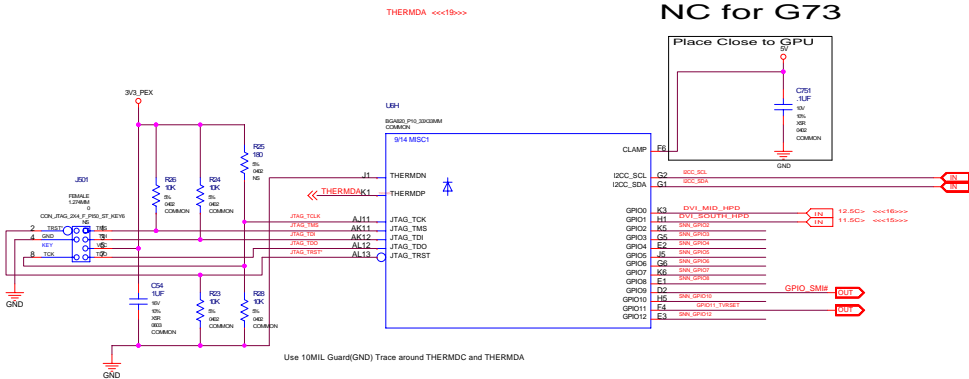
STRAPS		Bit Signal	Values
 10K	MIC0A011	00: PCI_AD_SWAP	0 REVERSED 1 NORMAL
 10K	MIC0A010	01: SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS (DEFAULT)
 10K	MIC0B010	02: RAM_CFG_0	RAM_CFG_0
 10K	MIC0B009	03: RAM_CFG_1	0000 0000 0000 1000T 0001 0000 0000 1000T 0010 0000 0000 1000T 0011 0000 0000 1000T 0100 0000 0000 1000T 0101 0000 0000 1000T 0110 0000 0000 1000T 0111 0000 0000 1000T
 10K	MIC0B008	04: RAM_CFG_2	0000 0000 0000 1000T 0001 0000 0000 1000T 0010 0000 0000 1000T 0011 0000 0000 1000T 0100 0000 0000 1000T 0101 0000 0000 1000T 0110 0000 0000 1000T 0111 0000 0000 1000T
 10K	MIC0B007	05: RAM_CFG_3	0000 0000 0000 1000T 0001 0000 0000 1000T 0010 0000 0000 1000T 0011 0000 0000 1000T 0100 0000 0000 1000T 0101 0000 0000 1000T 0110 0000 0000 1000T 0111 0000 0000 1000T
 10K	MIC0B006	06: CRYSTAL_0	00 13.000 MHz 01 14.285714 MHz 10 27.000 MHz 11 UNKNOWN
 10K	MIC0B005	07: TV_MODE_0	00 SECAM 01 NTSC 10 PAL 11 CRT
 10K	MIC0B004	08: TV_MODE_1	00 SECAM 01 NTSC 10 PAL 11 CRT
 10K	MIC0B003	09: AGP_3D_0	0 AGP0 ENABLED 1 AGP0 DISABLED
 10K	MIC0B002	10: AGP_3D_1	0 AGP1 ENABLED 1 AGP1 DISABLED
 10K	MIC0B001	11: AGP_FASTWR	0 FV0 ENABLED 1 FV0 DISABLED
 10K	MIC0B000	12: PCI_DEV_0	0001 0000 (DEFAULT) 1 1000 0000
 10K	MIC0B000	13: PCI_DEV_1	0001 0000 (DEFAULT) 1 1000 0000
 10K	MIC0B000	20: PCI_DEV_2	0001 0000 (DEFAULT) 1 1000 0000
 10K	MIC0B000	21: PCI_DEV_3	0001 0000 (DEFAULT) 1 1000 0000
 10K	MIC0B000	14: BUS_TYPE	0 PCI 1 AGP
 10K	MIC0B000	15: FP_FACE	0 240S 1 120S (DEFAULT)
 10K	MIC0B000	16: USER_0	0000 (DEFAULT)
 10K	MIC0B000	17: USER_1	0000 (DEFAULT)
 10K	MIC0B000	18: USER_2	0000 (DEFAULT)
 10K	MIC0B000	19: USER_3	0000 (DEFAULT)
 10K	MIC0B000	22: FB_0	00 64M 01 128M 10 256M (DEFAULT) 11 512M
 10K	MIC0B000	24: FB_1	00 64M 01 128M 10 256M (DEFAULT) 11 512M
 10K	MIC0B000	25: BR	0 BRIDGE DISABLED 1 BRIDGE ENABLED
 10K	MIC0B000	26: BR_128M	BR BITS IGNORED IF BRIDGE IS DISABLED
 10K	MIC0B000	27: BR_AGP	0 BR AGP 1 BR AGP
 10K	MIC0B000	28: BR_ID	00 PARALLEL 01 SERIAL_AT32F
 10K	MIC0B000	29: ROM_TYPE_0	00 PARALLEL 01 SERIAL_AT32F
 10K	MIC0B000	30: ROM_TYPE_1	00 PARALLEL 01 SERIAL_AT32F
 10K	MIC0B000	NU_STRAP_1 11: PEK_PL1_EN_TERR100	0 ENABLED (DEFAULT) 1 DISABLED
 10K	MIC0B000	NU_STRAP_1 12: SGIO_PACCFG_LUT_ADR_0	00 DEFAULT 01 DESKTOP LOW THIR 10 DESKTOP HIGH THIR 11 DESKTOP HIGH THIR
 10K	MIC0B000	NU_STRAP_1 13: SGIO_PACCFG_LUT_ADR_1	00 DEFAULT 01 DESKTOP LOW THIR 10 DESKTOP HIGH THIR 11 DESKTOP HIGH THIR
 10K	MIC0B000	NU_STRAP_1 14: SGIO_PACCFG_LUT_ADR_2	00 DEFAULT 01 DESKTOP LOW THIR 10 DESKTOP HIGH THIR 11 DESKTOP HIGH THIR



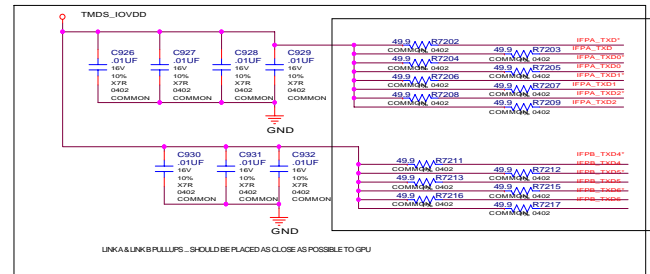
JTAG, GPIO, BIOS ROM

GPIO Assignment Table		
GPIO	I/O	FUNCTION
0	IN	DIM MIO HOTPLUG DET
1	IN	RESERVED
2	IN	RESERVED
3	IN	RESERVED
4	IN	RESERVED
5	IN	RESERVED
6	IN	RESERVED
7	IN	RESERVED
8	IN	THERM ALERTSLOW
9	OUT	FAN CONTROL
10	IN	RESERVED
11	OUT	HOTPLUG SELECT
12	IN	RESERVED

NET	MIN_LINE_WIDTH
FAN_THERM_BYPASS	0.1
FAN_FAN	0.1
FAN_FAN_B	0.1
FAN_FAN_C	0.1
THERMDC	0.1
THERMDA	0.1



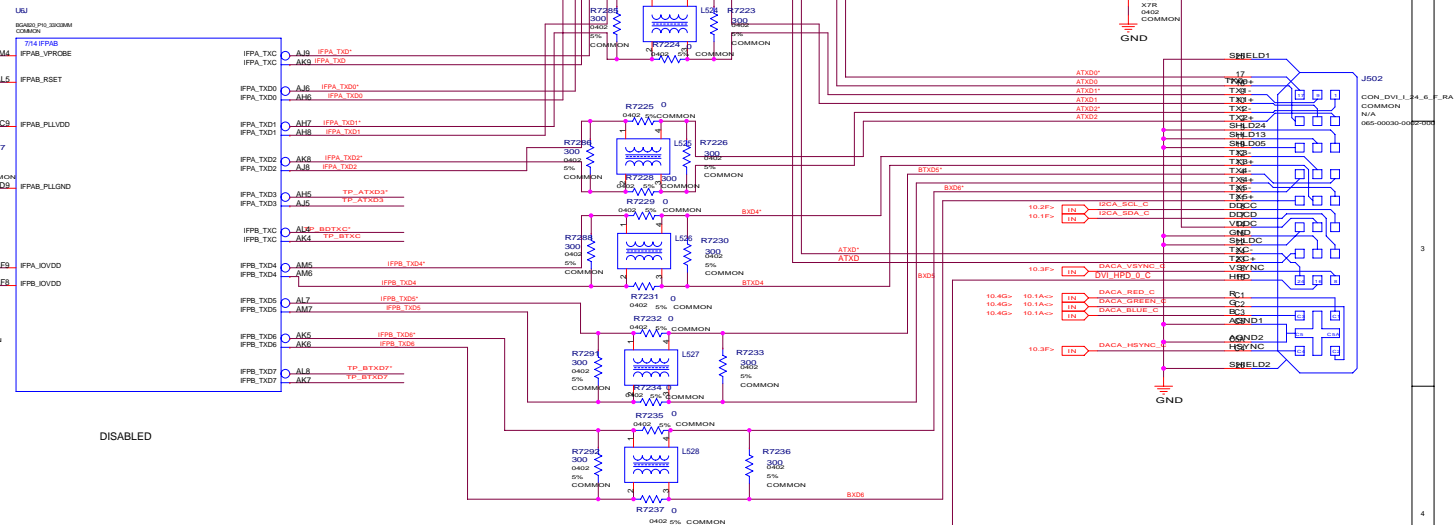
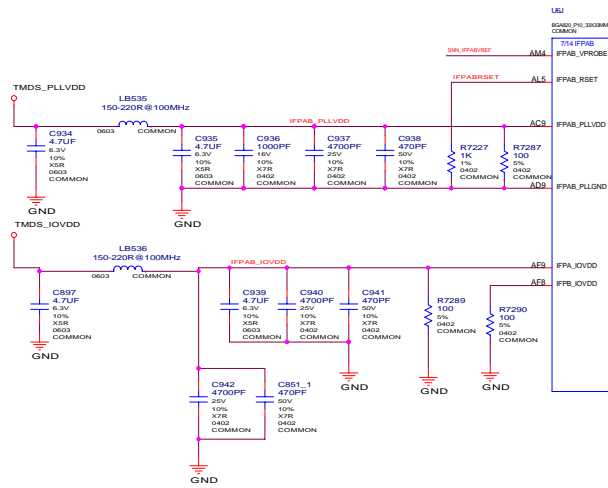
INTERNAL TMDS LINK A/B



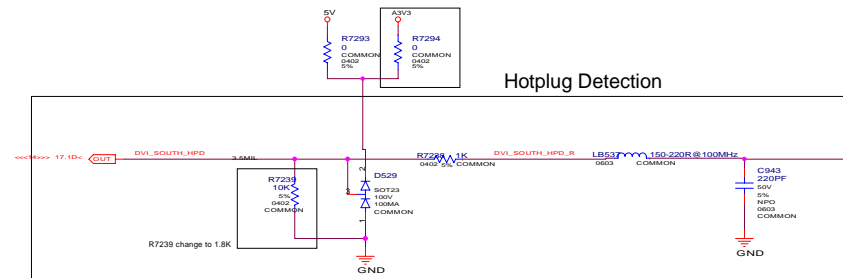
NC for G73

NET	MIN_LINE_WIDTH
FPABSET	12
FPABFLD0	12
FPABJ0D0	12
FPB0J0D0	12

INTERNAL TMDS ..LINK A/B



ADD A3V3 for G73



R7239 change to 1.8K for G73

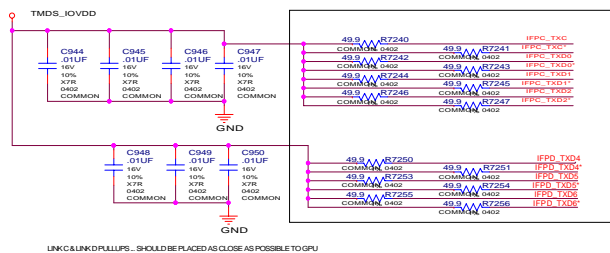


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Size	Document Number	Rev
Custom	INTERNAL TMD5 LINK A/B	10
Date:	Friday, December 02, 2005	Sheet 15 of 20

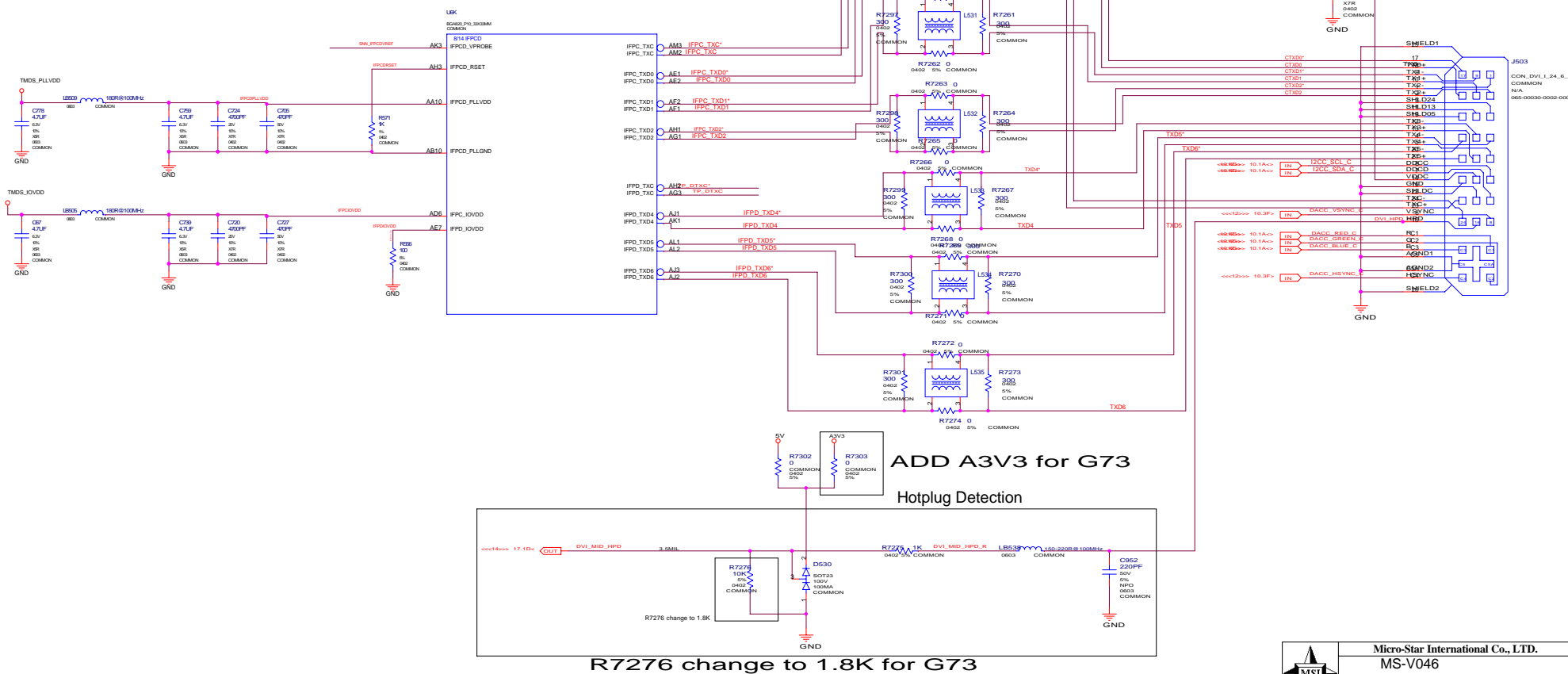
INTERNAL TMDS LINK C/D

INTERNAL TMDS .. LINK C & D



NC for G73

NET	MN_LINE_WIDTH	VOLTAGE
#PCDVRREF	12	3.3V
#PCDPLLVD	12	3.3V
#PCDIOVDD	12	3.3V
#PCDIOVDD	12	3.3V
#PCDRESET	12	3.3V



ADD A3V3 for G73

Hotplug Detection

R7276 change to 1.8K for G73

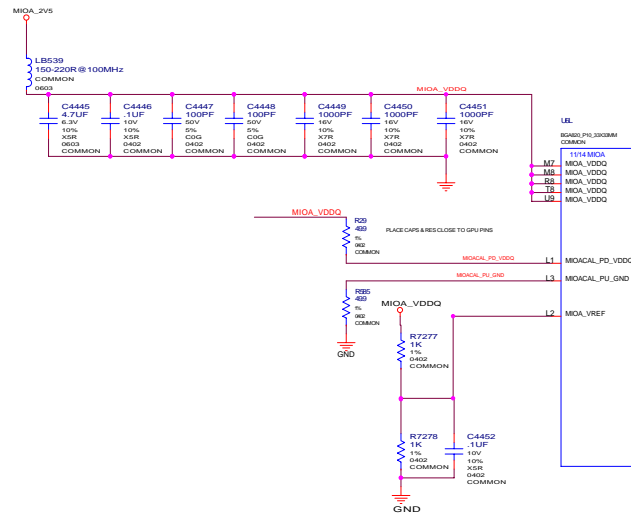


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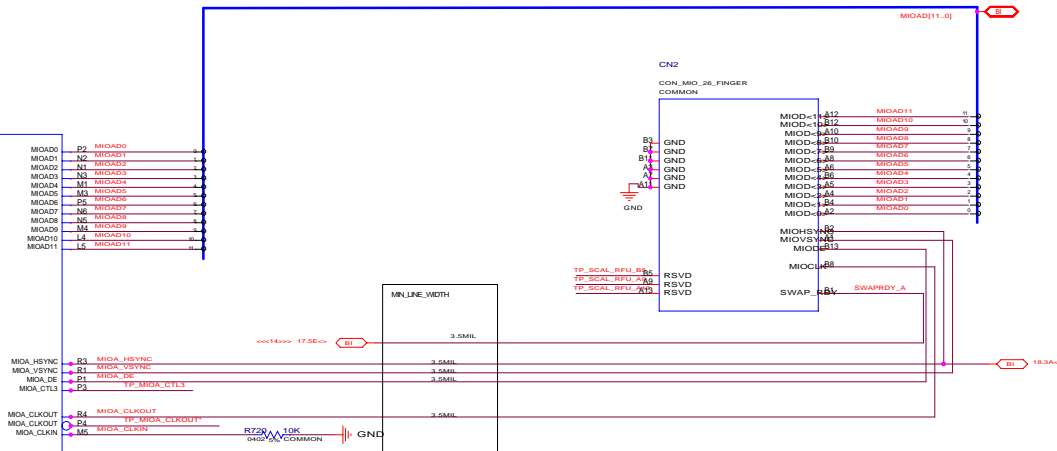
Document Number	Rev
INTERNAL TMD5 LINK C/D	10
Friday, December 02, 2005	Sheet 16 of 20

MIOA/B XTALPLL VDD

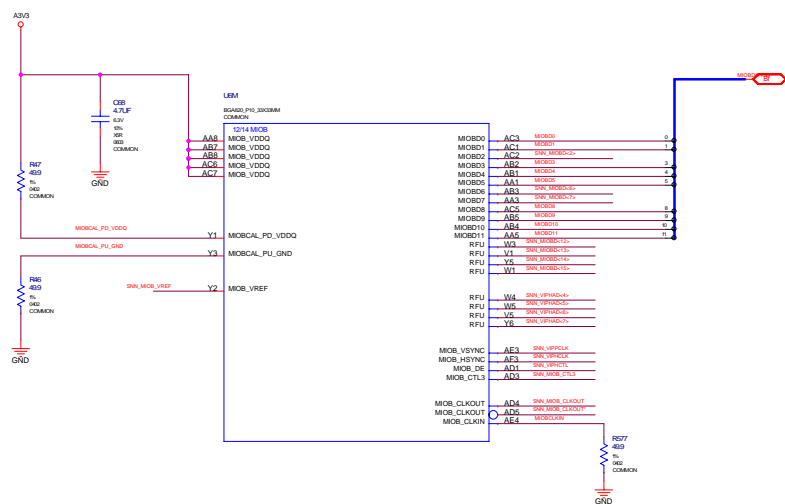
MIOA



Feature Connector

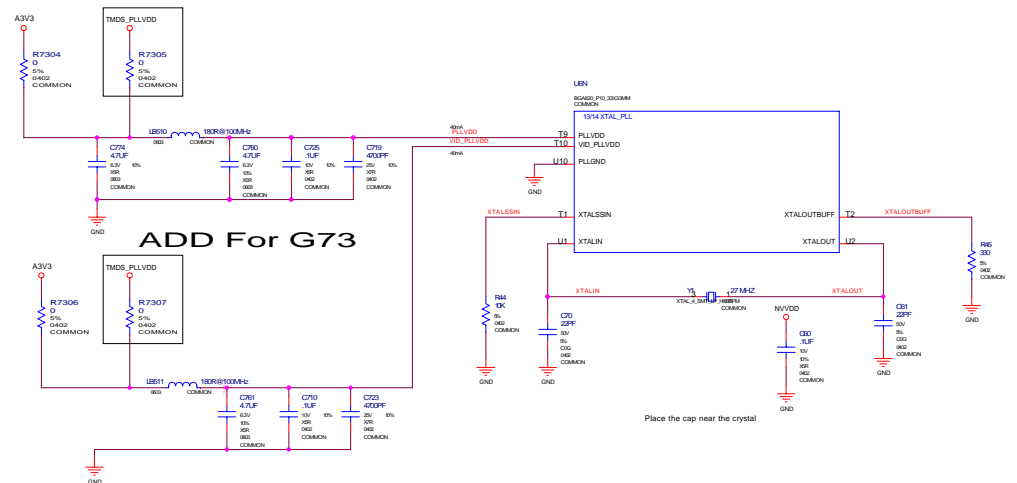


MIOB



XTAL/PLLVD

ADD For G73

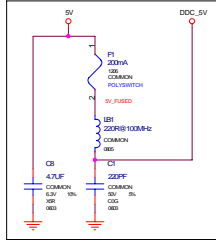


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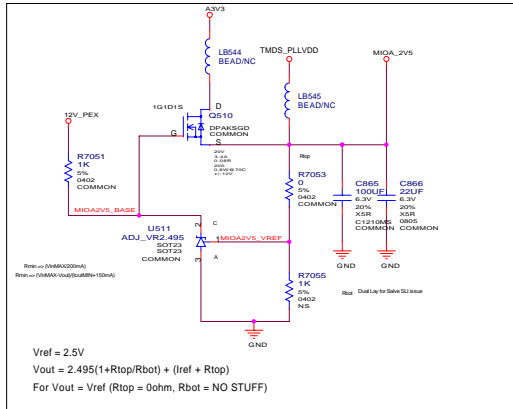
Size	Document Number	Rev
Custom	MIOAB XTALPLLVD	10
Date:	Friday, December 02, 2005	Sheet 17 of 20

5V/PEX1V2/PLLVDV/OVDD

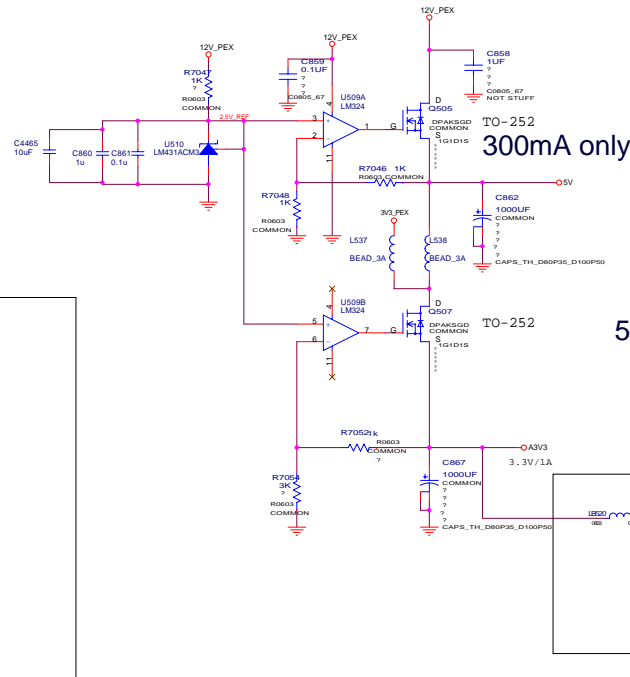
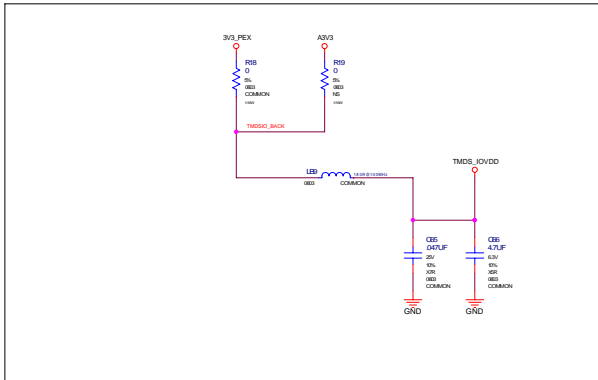
DDC 5V



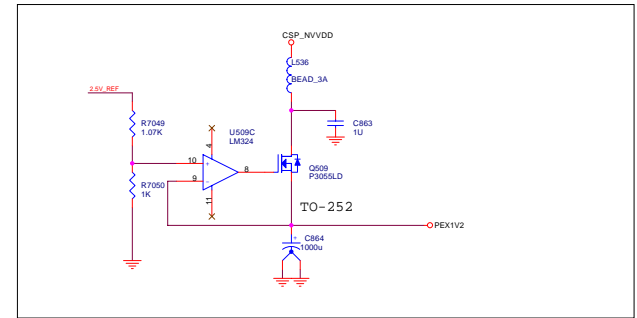
MIOA_VDDQ



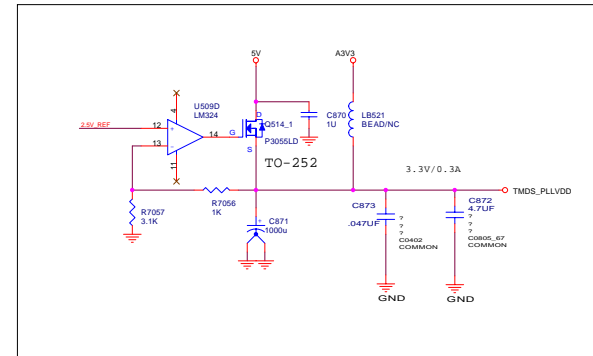
TMSD IO SUPPLY WITH BACKDRIVE PROTECTION



PEX1V2

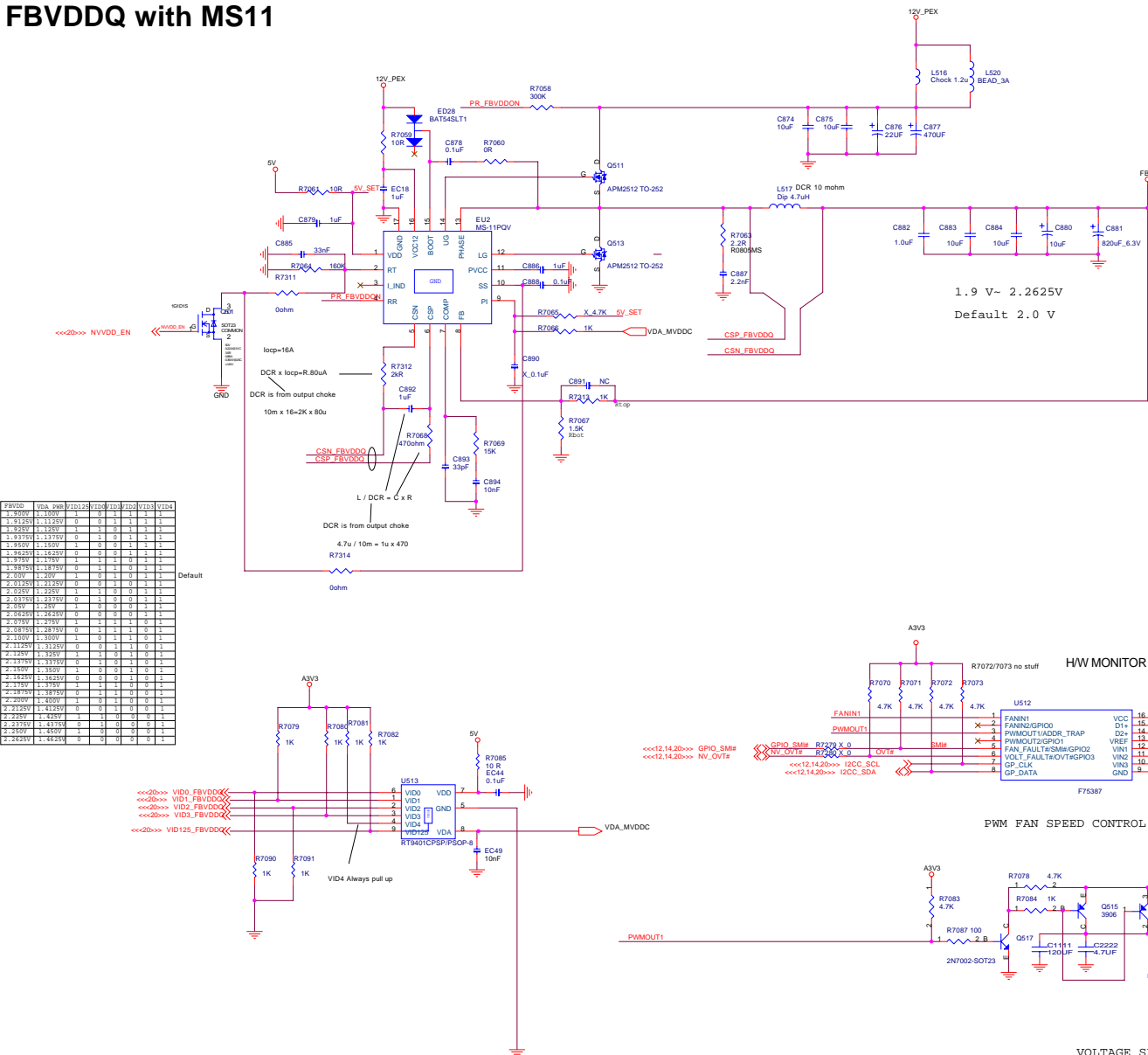


TMSD AB/CD PLL Supply

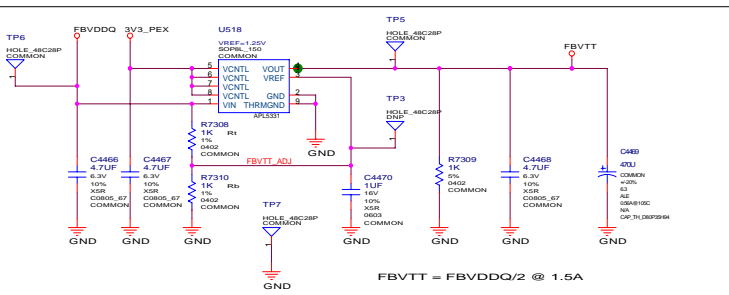


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MS-V046		
Size	Document Number	Rev
2-inches	5V/PEX1V2/PLLVDV/OVDD	10
Date	Friday, December 02, 2005	18:41

FBVDDQ with MS11

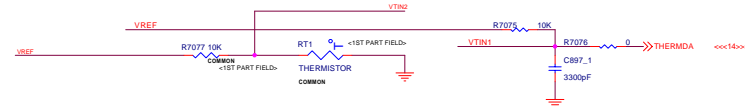


FBVTT TERMINATION

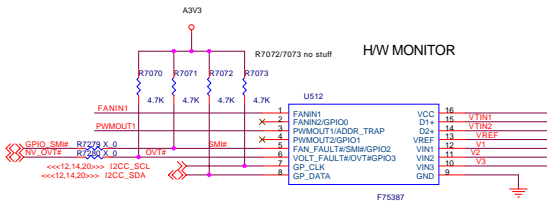


FBVTT TERMINATION $FBVTT = FBVDDQ/2$ @

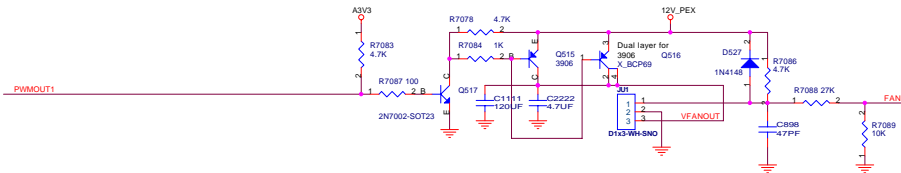
TEMPERATURE MONITORING



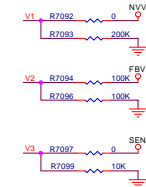
H/W MONITORING



PWM FAN SPEED CONTR



VOLTAGE SENSING CIRCUIT



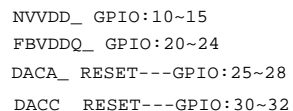
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MS-V046

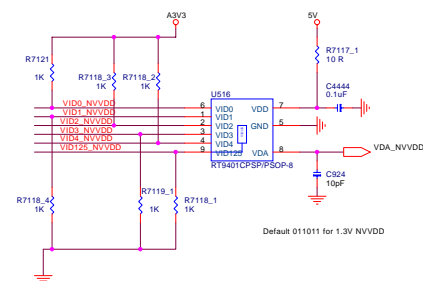
```
Rcsn= DCR*Icop/80uA =
1mohm*40Amp/80uA=499 ohm

I_ind= (Icop*DCR/Rcsn )*4
= (40A*1mohm/499ohm)*4=80uA

R_ind=V_ind/I_ind= 1V/80uA=
3.3K
```



70A_V000	70D125	70D100	70D100	70D100	70D100
1.1875V	0	1	1	0	1
1.200V	1	0	1	0	1
1.2125V	0	0	1	0	1
1.225V	1	1	0	0	1
1.2375V	0	1	0	0	1
1.250V	1	0	0	0	1
1.2625V	0	0	0	0	1
1.275V	1	1	1	1	0
1.287V	0	1	1	1	0
1.300V	1	0	1	1	0
1.3125V	0	1	0	1	0
1.325V	1	1	0	1	0
1.3375V	0	1	0	1	0
1.350V	1	0	0	1	0
1.3625V	0	0	0	1	0
1.375V	1	1	1	0	0
1.3875V	0	1	1	0	0
1.400V	1	0	1	0	0
1.4125V	0	0	1	0	0



NVVDD 1.33V default 010101