

V207-10

P672: GT215-128bit, 32Mx32 GDDR5

DL-DVI, VGA, HDMI

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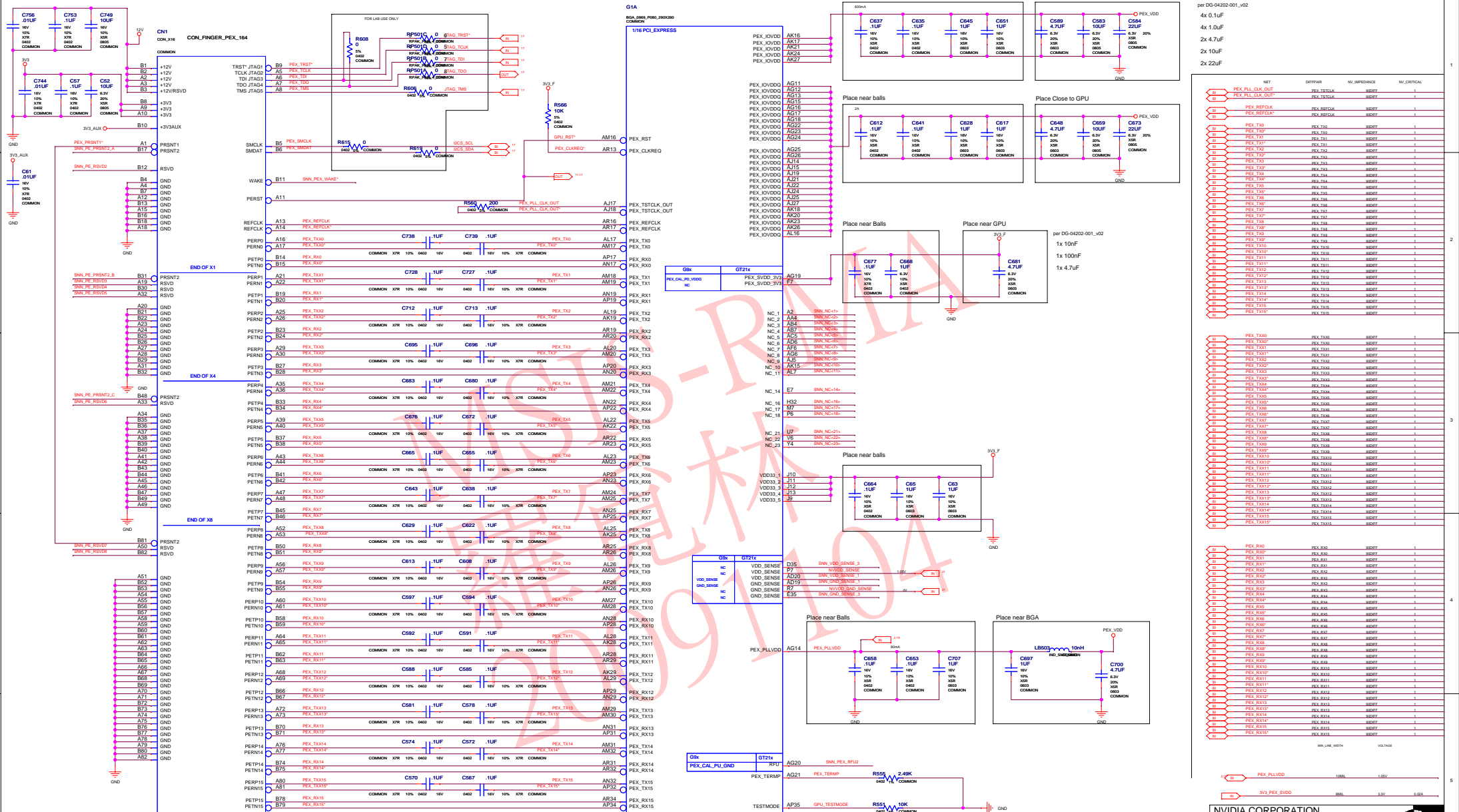
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V207 20 pcb change list

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REV	VARIANT	NVPN	ASSEMBLY
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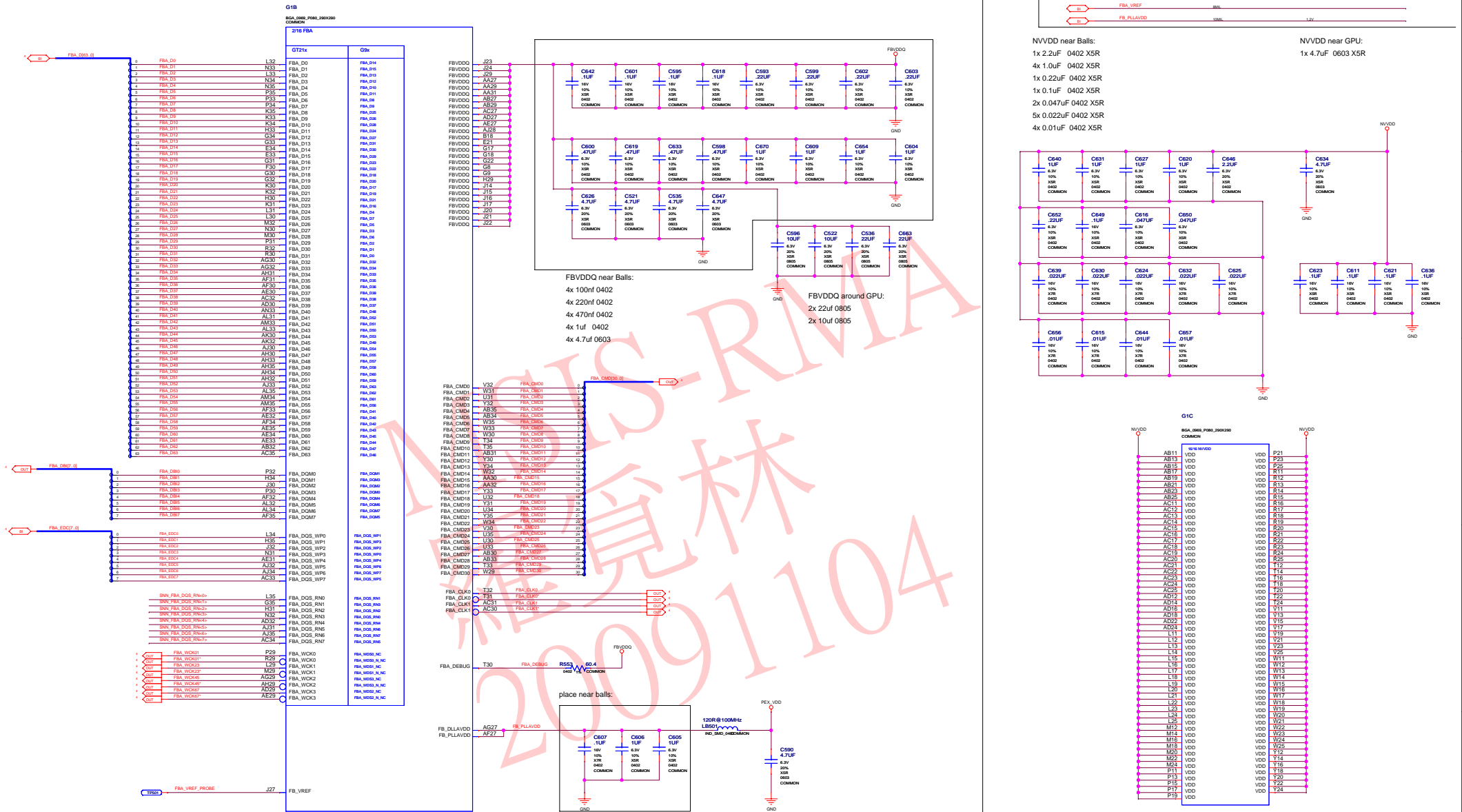
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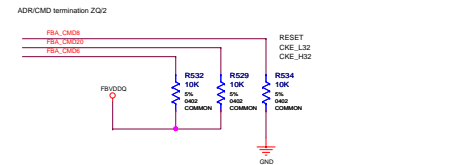
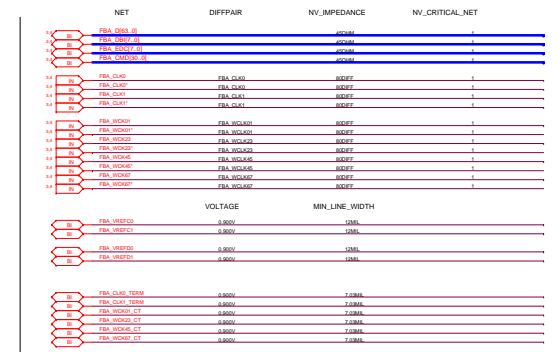
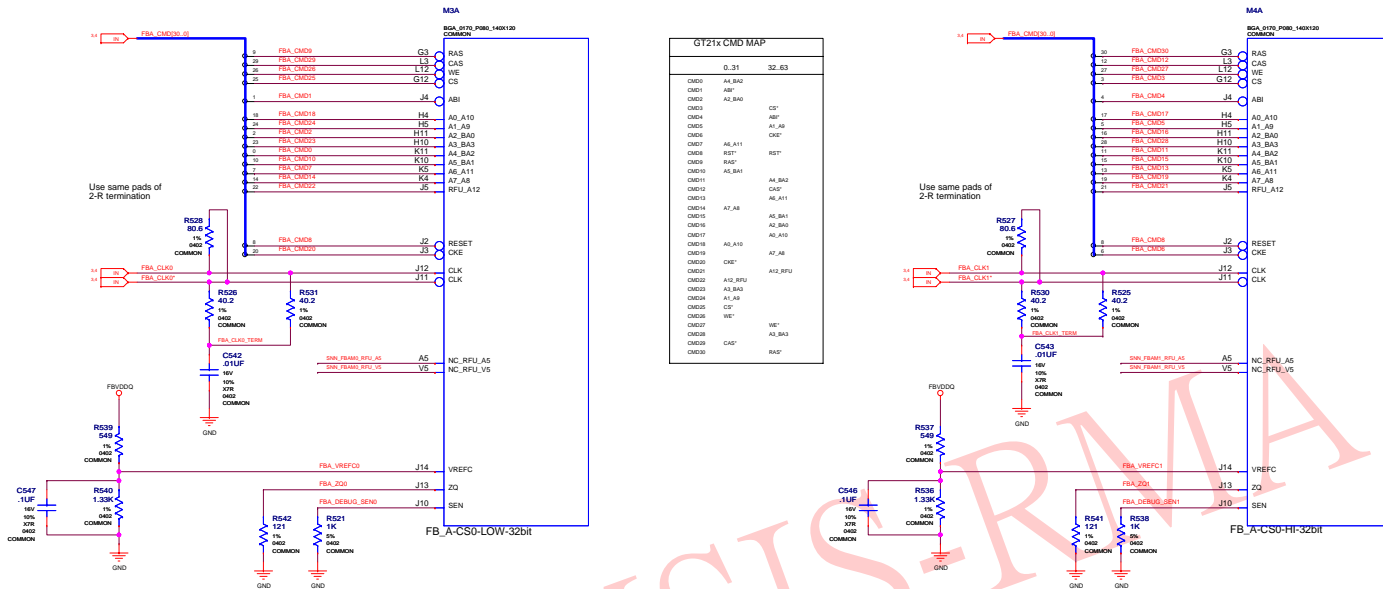
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
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NAME		DATE	01-JUL-2009

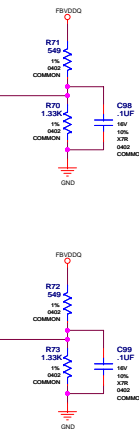
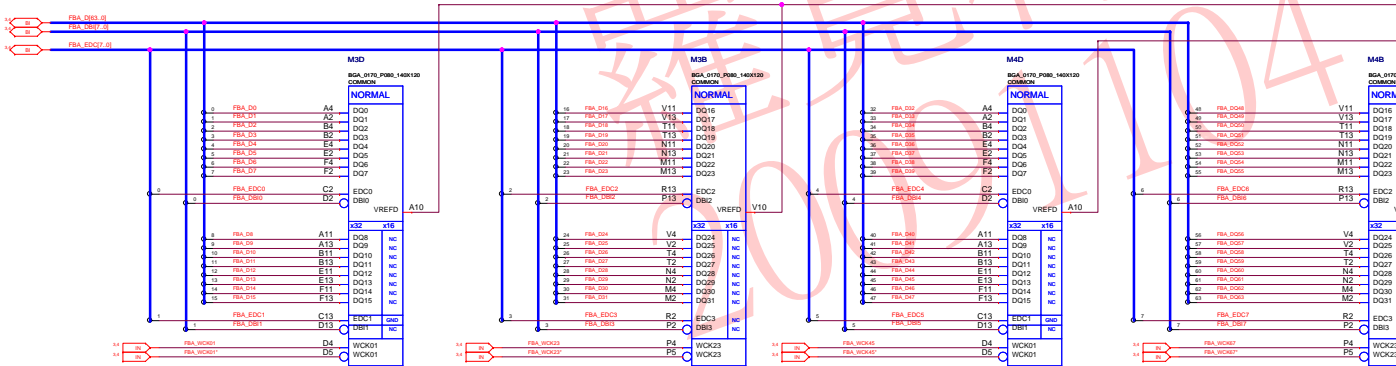
MEMORY Partition A - GPU, FBVDD/Q & NVVDD DECOUPLING



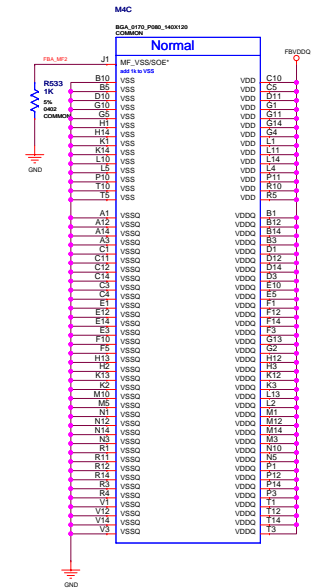
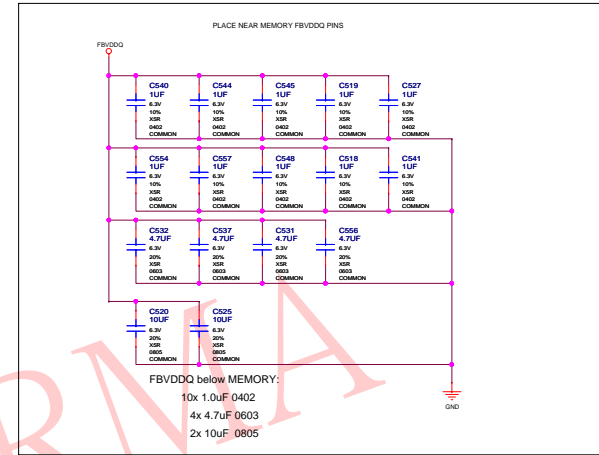
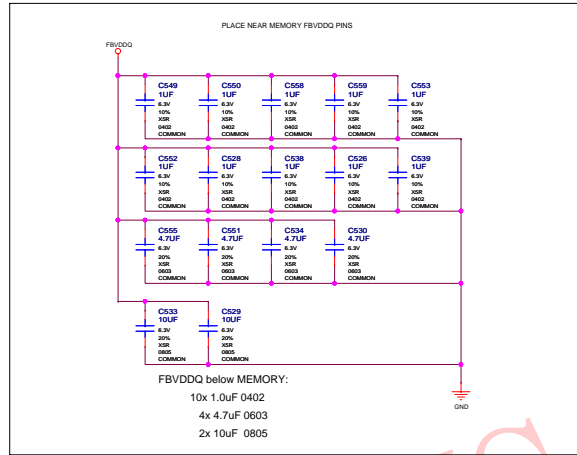
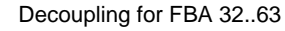
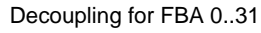
MEMORY Partition A



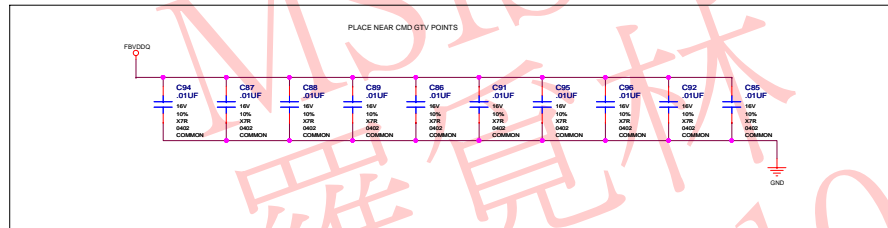
!!! Place all WCK termination inline instead at the memory near end (<50ps ~300MIL from DRAM pin) !!!



MEMORY Partition A - Decoupling



Return path coupling GND/FBVDDQ for FBA



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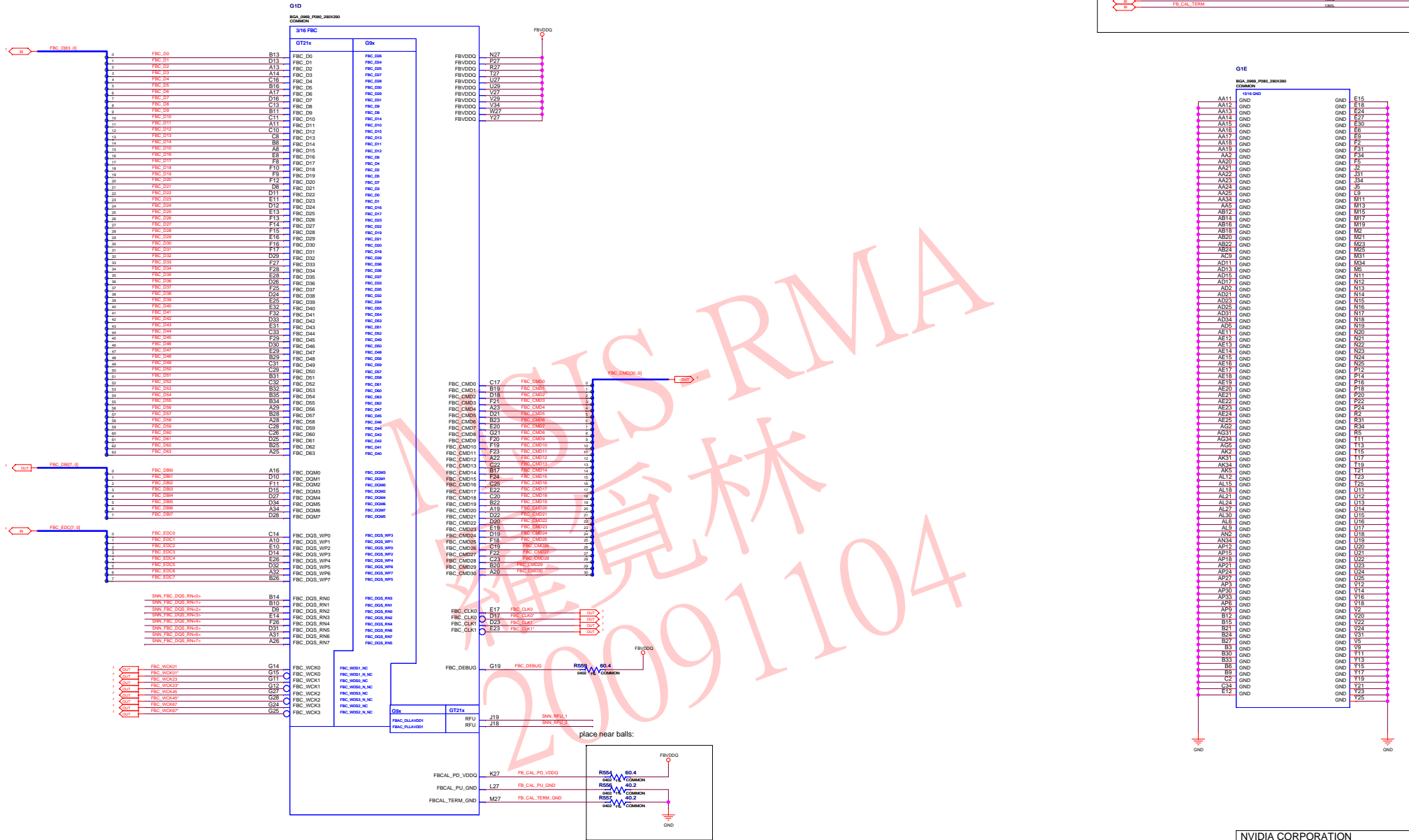


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MEMORY Partition C - GPU



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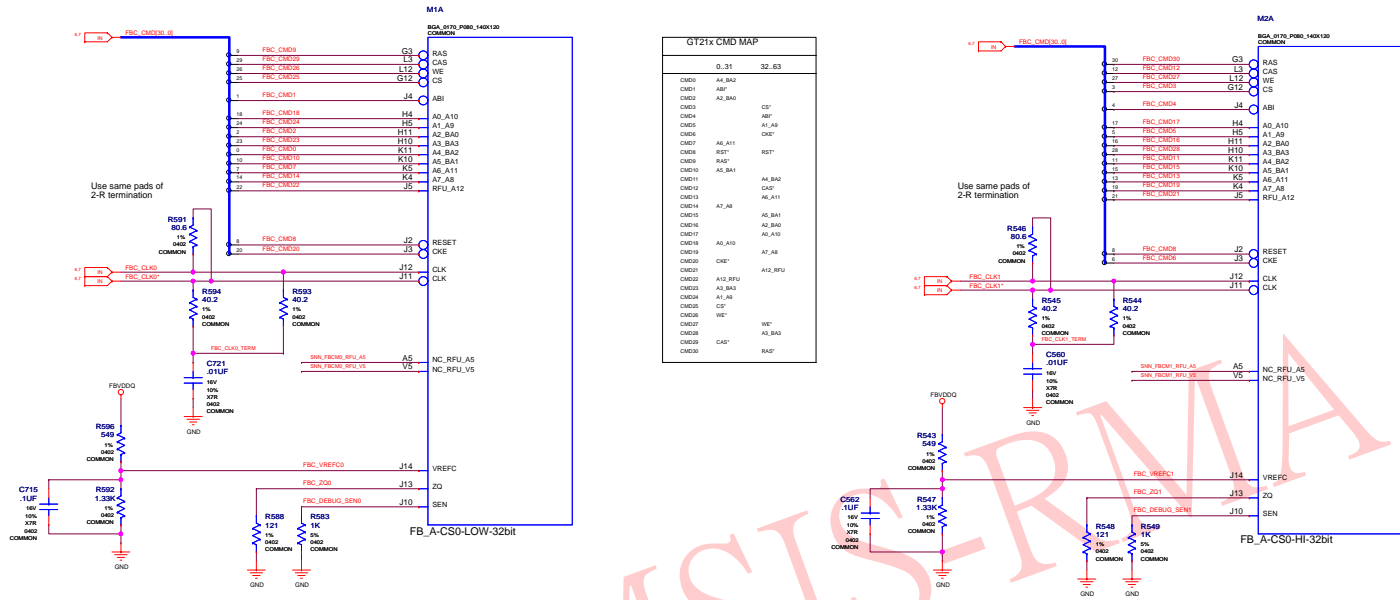


NV_PN	600-10672-base-100 A
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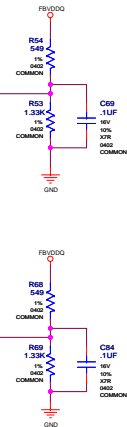
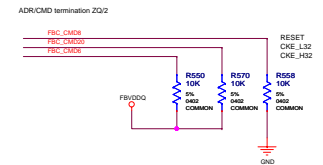
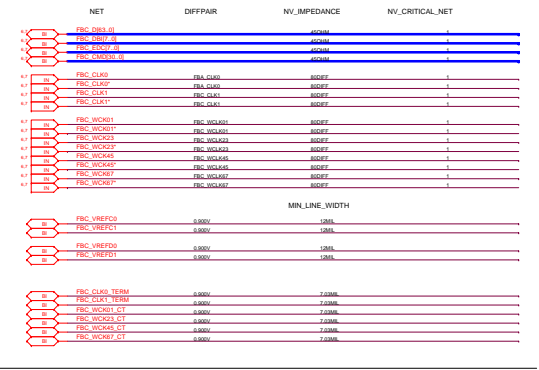
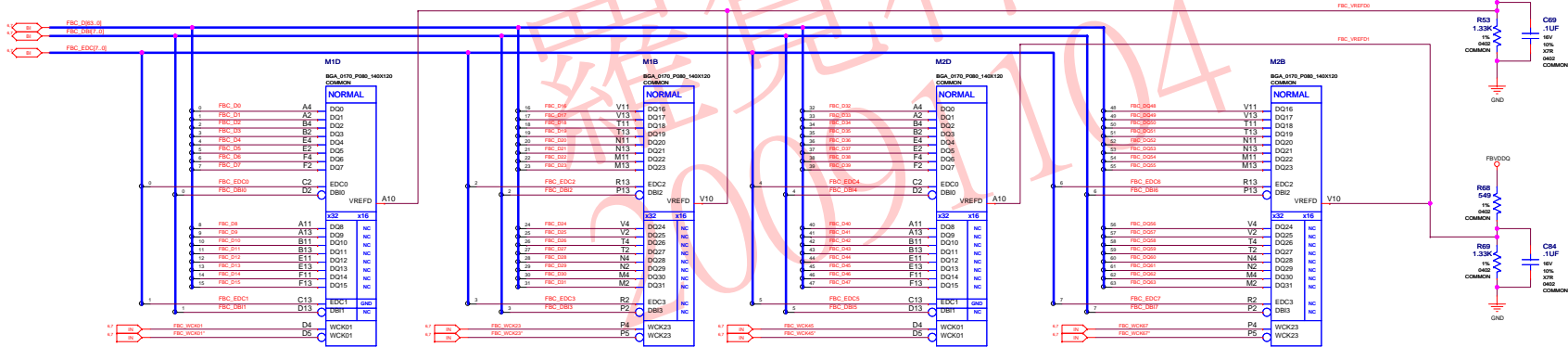
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NAME		DATE	01-JUL-2009

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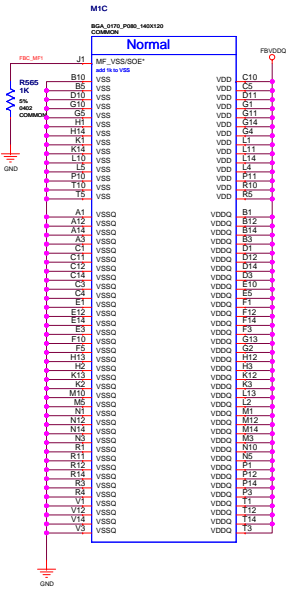
MEMORY Partition C



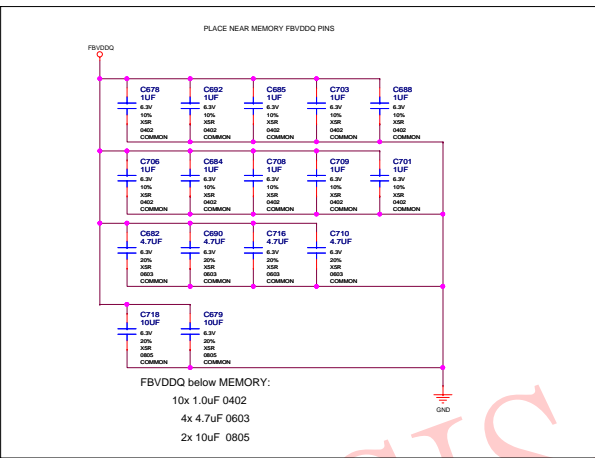
!!! Place all WCK termination inline instead at the memory near end (<50ps ~300MIL from DRAM pin)!!!



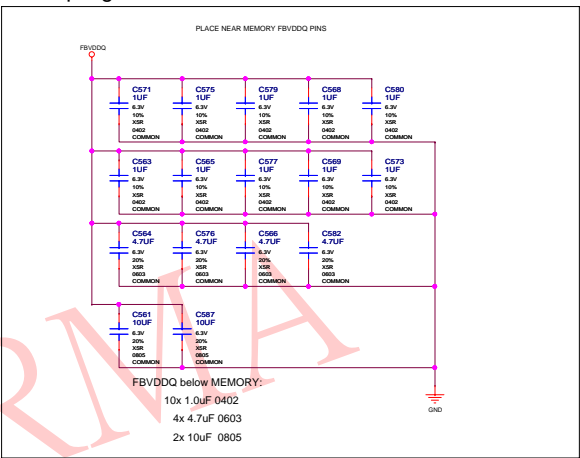
MEMORY PARTITION C DECOUPLING



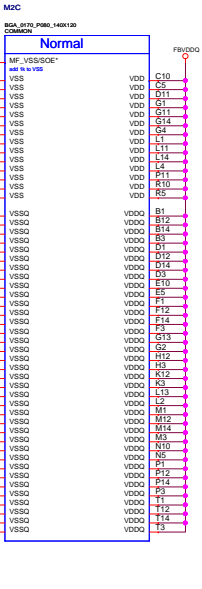
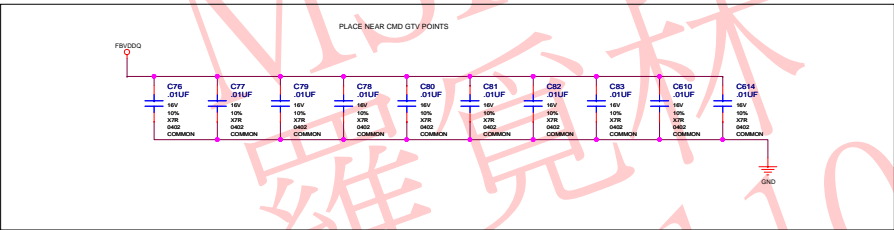
Decoupling for FBC 0..31



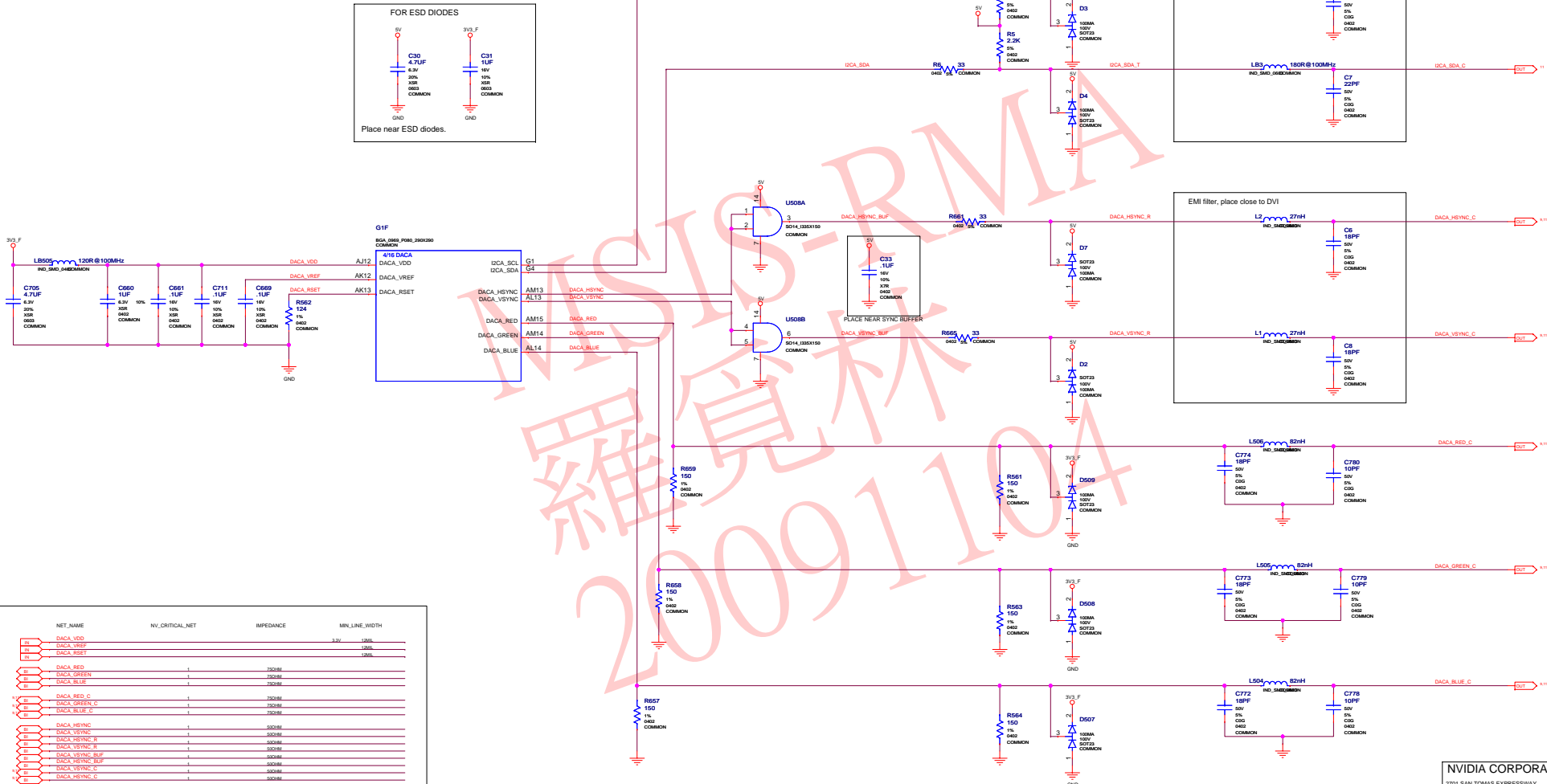
Decoupling for FBC 32..63



Return path coupling GND/FBVDDQ for FBC



Primary Display (DACA), DVI-I (South)



	NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
15	DACIA_VDD			3.2V 120u
16	DACIA_VREF			100u
17	DACIA_VREF			120u
18	DACIA_RED	1	7500u	
19	DACIA_GREEN	1	7500u	
20	DACIA_BLUE	1	7500u	
21	DACIA_RED_C	1	7500u	
22	DACIA_GREEN_C	1	7500u	
23	DACIA_BLUE_C	1	7500u	
24	DACIA_V5VNC	1	5000u	
25	DACIA_V5VNC_B	1	5000u	
26	DACIA_V5VNC_C	1	5000u	
27	DACIA_V5VNC_BUF	1	5000u	
28	DACIA_V5VNC_BUF	1	5000u	
29	DACIA_V5VNC_C	1	5000u	
30	DACIA_V5VNC_C	1	5000u	

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA (PRIMARY DVI-I)

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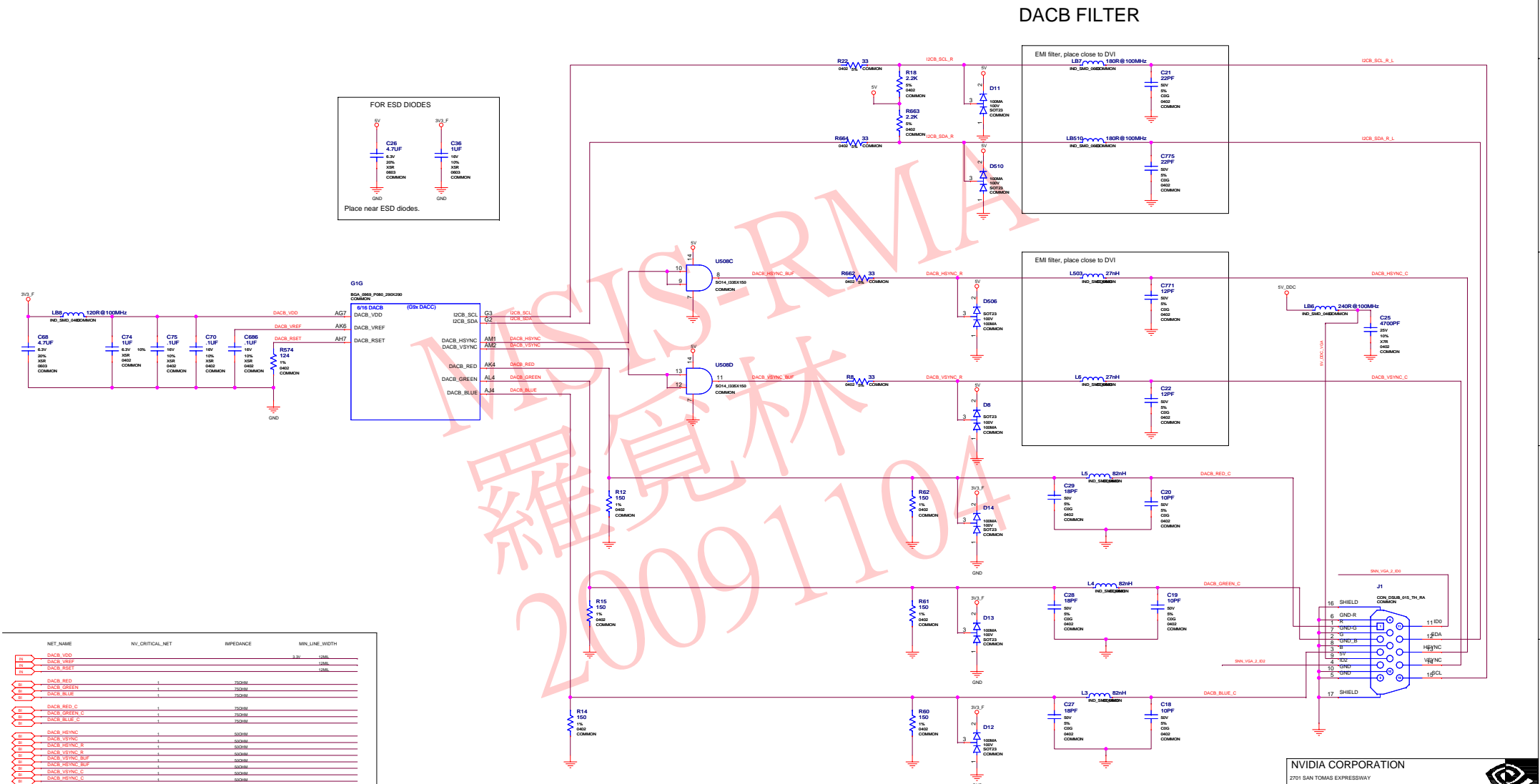
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Secondary Display (DACB), VGA (Mid)



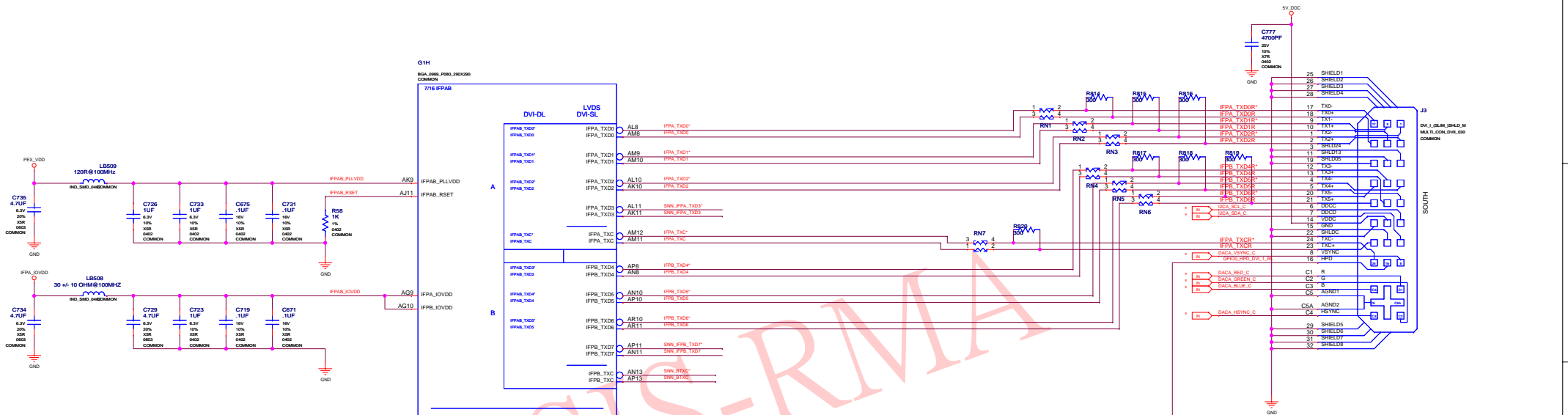
	NET_NAME	IV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
1	DACB_VDD			32v 100M
2	DACB_VREF			100M
3	DACB_PSET			100M
4	DACB_RED	+	7500M	
5	DACB_GREEN	+	7500M	
6	DACB_BLUE	+	7500M	
7	DACB_RED_C	+	7500M	
8	DACB_GREEN_C	+	7500M	
9	DACB_BLUE_C	+	7500M	
10	DACB_HYSTING	+	5000M	
11	DACB_VSTING	+	5000M	
12	DACB_HYSTING_R	+	5000M	
13	DACB_VSTING_R	+	5000M	
14	DACB_HYSTING_BUF	+	5000M	
15	DACB_VSTING_BUF	+	5000M	
16	DACB_VSTING_C	+	5000M	
17	DACB_HYSTING_C	+	5000M	

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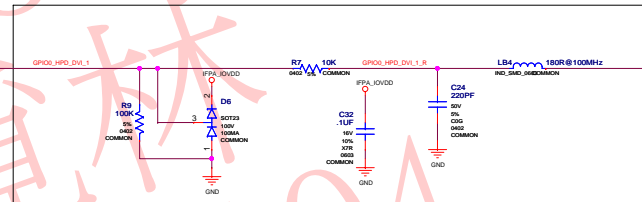
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB (SECONDARY VGA)

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NAME		DATE	01-JUL-2009

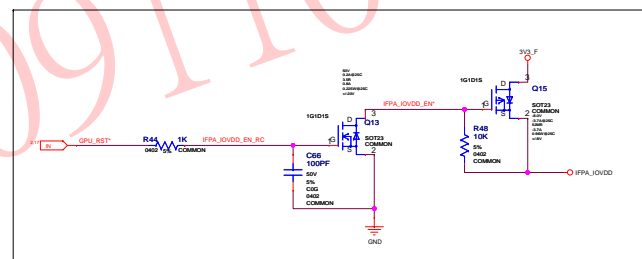
LINK A/B: TMDS, Primary DVI-I DL (South)



HOTPLUG DETECTION



IFP_IOVDD BACKDRIVE PREVENTION



	NETNAME	DIFF PAIR NAME	IV, CRITICAL	IV, REFERENCE
10	IFPA_T0C1	FPA_T0C1	1	5000T
10	IFPA_T0C2	FPA_T0C2	1	5000T
10	IFPA_T0D0	FPA_T0D0	1	5000T
10	IFPA_T0D1	FPA_T0D1	1	5000T
10	IFPA_T0D11	FPA_T0D1	1	5000T
10	IFPA_T0D2	FPA_T0D2	1	5000T
10	IFPA_T0D21	FPA_T0D21	1	5000T
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10	IFPA_T0D24	FPA_T0D24	1	5000T
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10	IFPA_T0D26	FPA_T0D26	1	5000T
10	IFPA_T0D27	FPA_T0D27	1	5000T
10	IFPA_T0D28	FPA_T0D28	1	5000T
10	IFPA_T0D29	FPA_T0D29	1	5000T
10	IFPA_T0D30	FPA_T0D30	1	5000T
10	IFPA_T0D31	FPA_T0D31	1	5000T
10	IFPA_T0D32	FPA_T0D32	1	5000T
10	IFPA_T0D33	FPA_T0D33	1	5000T
10	IFPA_T0D34	FPA_T0D34	1	5000T
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10	IFPA_T0D36	FPA_T0D36	1	5000T
10	IFPA_T0D37	FPA_T0D37	1	5000T
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10	IFPA_T0D41	FPA_T0D41	1	5000T
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10	IFPA_T0D91	FPA_T0D91	1	5000T
10	IFPA_T0D92	FPA_T0D92	1	5000T
10	IFPA			

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PAGE DETAIL	TMD5 LINK A/B: DVI-I (SOUTH)

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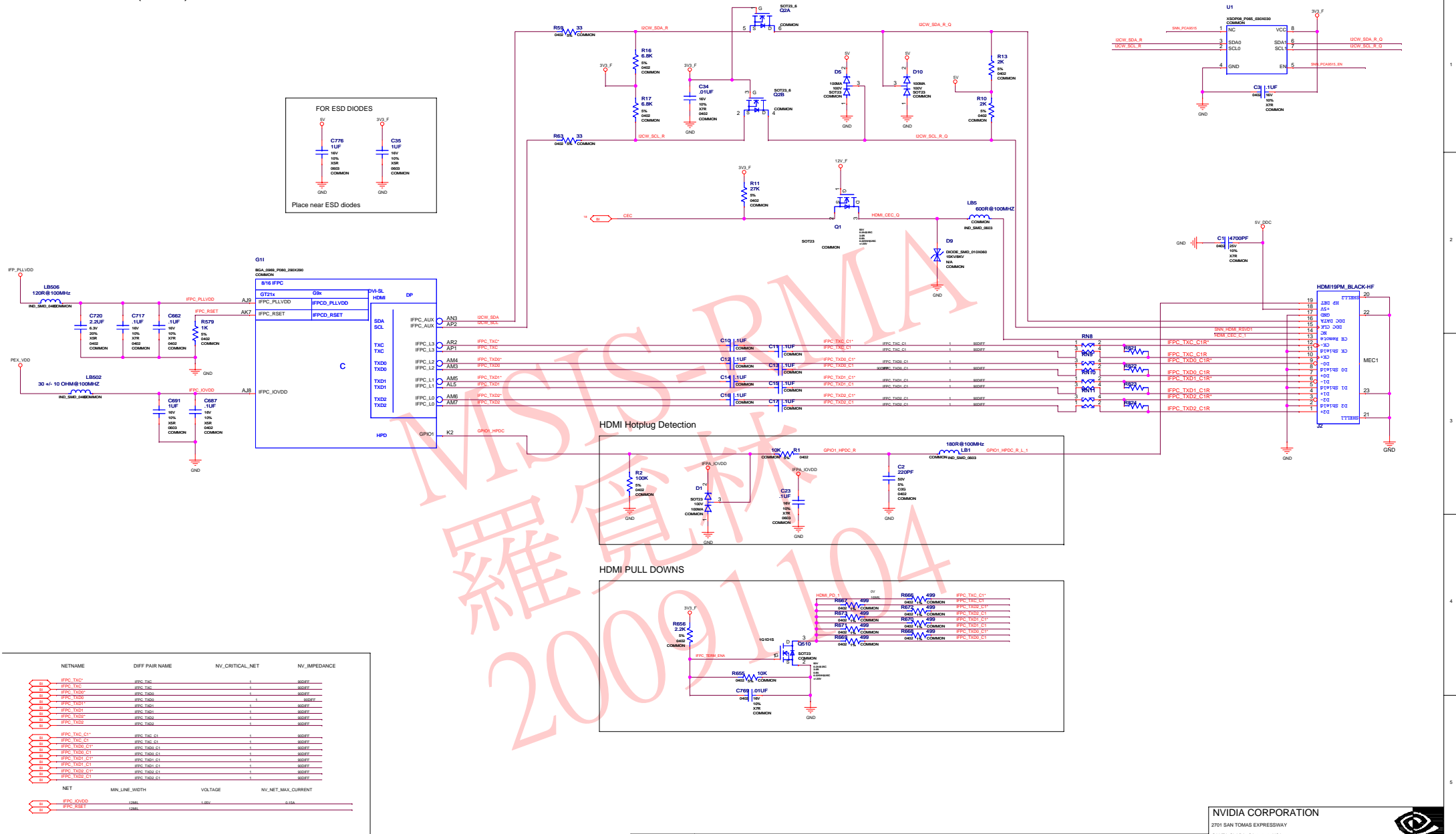
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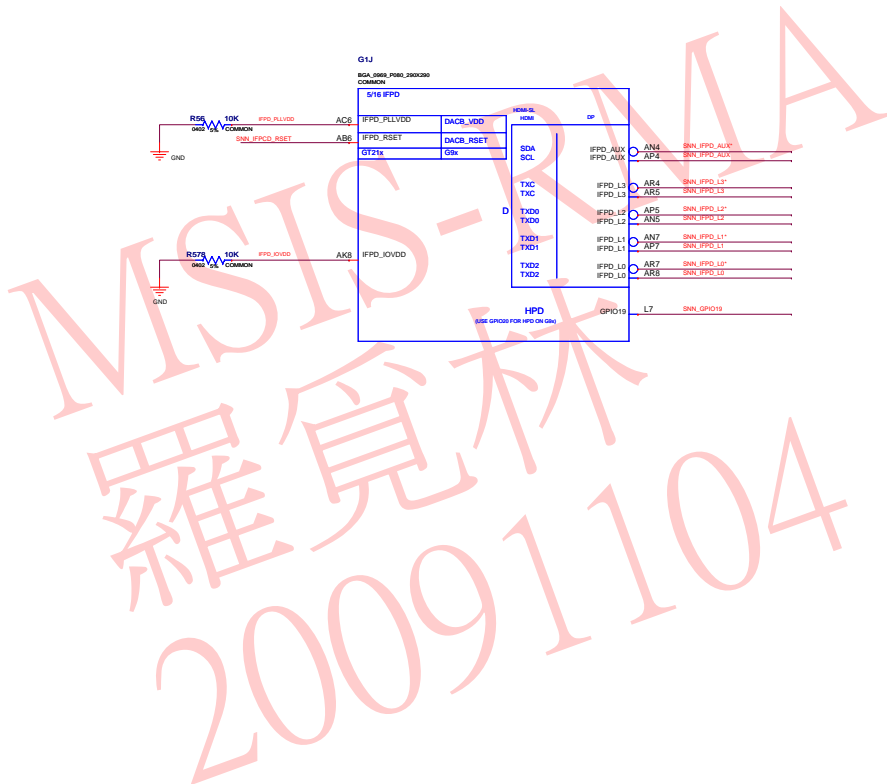
LINK C: HDMI (North)



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PAGE DETAIL	LINK C: HDMI (NORTH)

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A



A

3

C

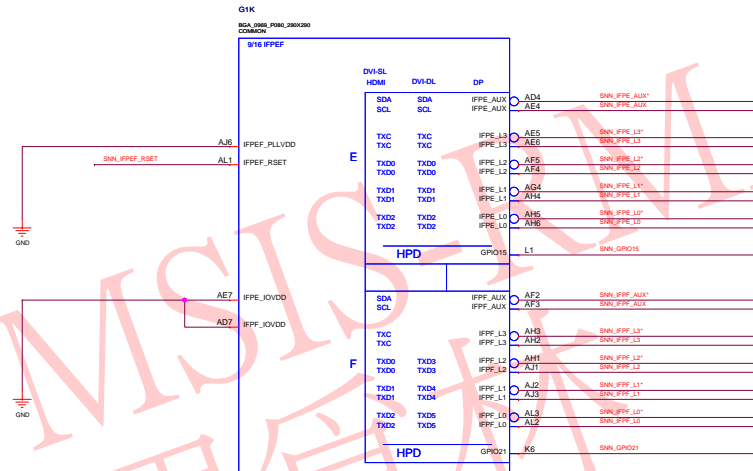
P

3

F

Q

LINK E/F: (UNUSED)



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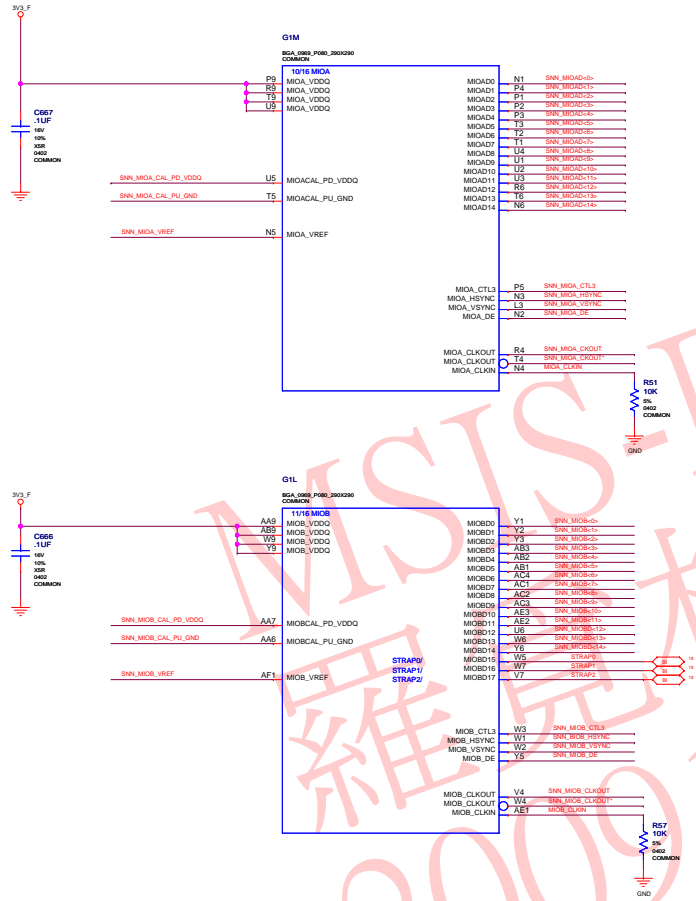
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A	B	C	D	E	F	G	H
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MIOA/B UNUSED



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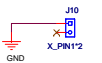
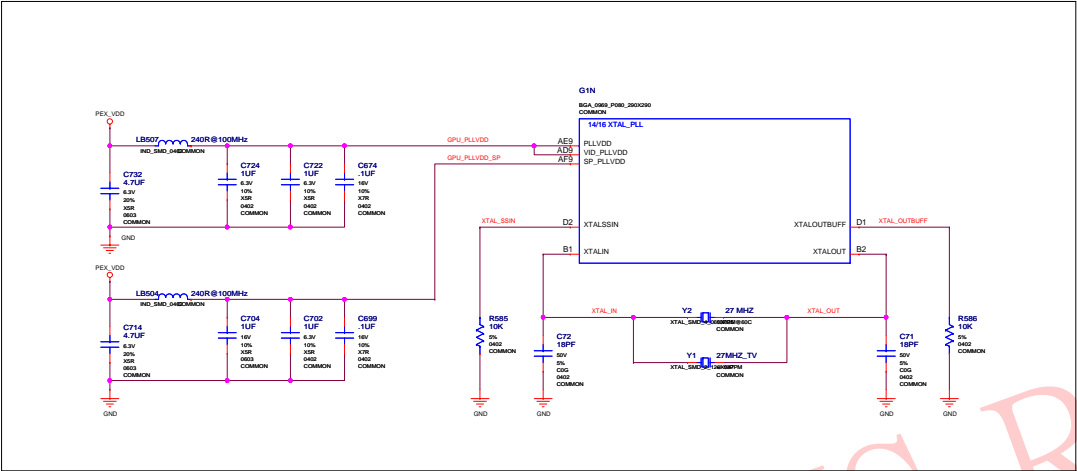


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB (UNUSED)

XTAL, MECHANICALS

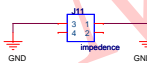
XTAL/GPU_PLLVDD



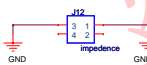
MEM Data
FBA_Data
TOP
5.69mils / 45ohm +/- 10%
Reference INT1 GND



MEM CMD
FBA_CMD<0>
BOTTOM
5.69mils / 45ohm +/- 10%
Reference INT2 GND

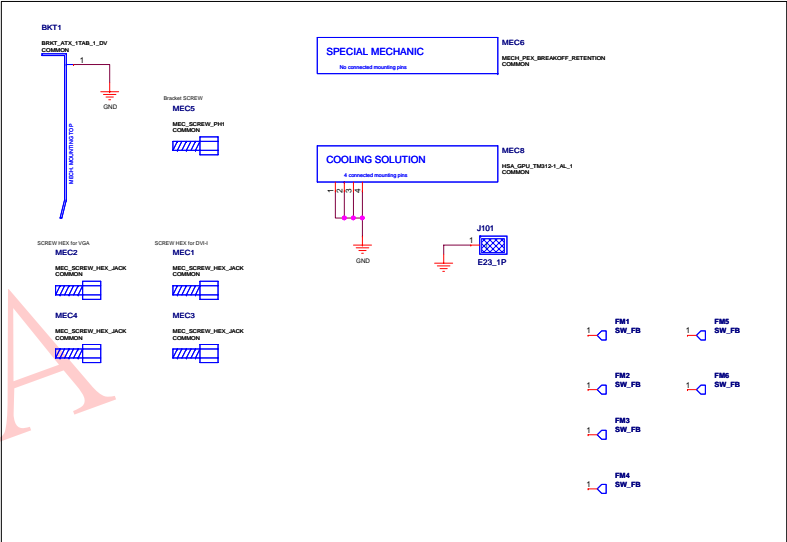


MEM CLK
FBA_CLK0
BOTTOM
5.25mils / 80ohm +/- 10%
Reference INT2 GND



HDMI
IPC_TXC*
BOTTOM
4.00mils / 80ohm +/- 10%
Reference INT2 GND

MECHANICALS & THERMALS



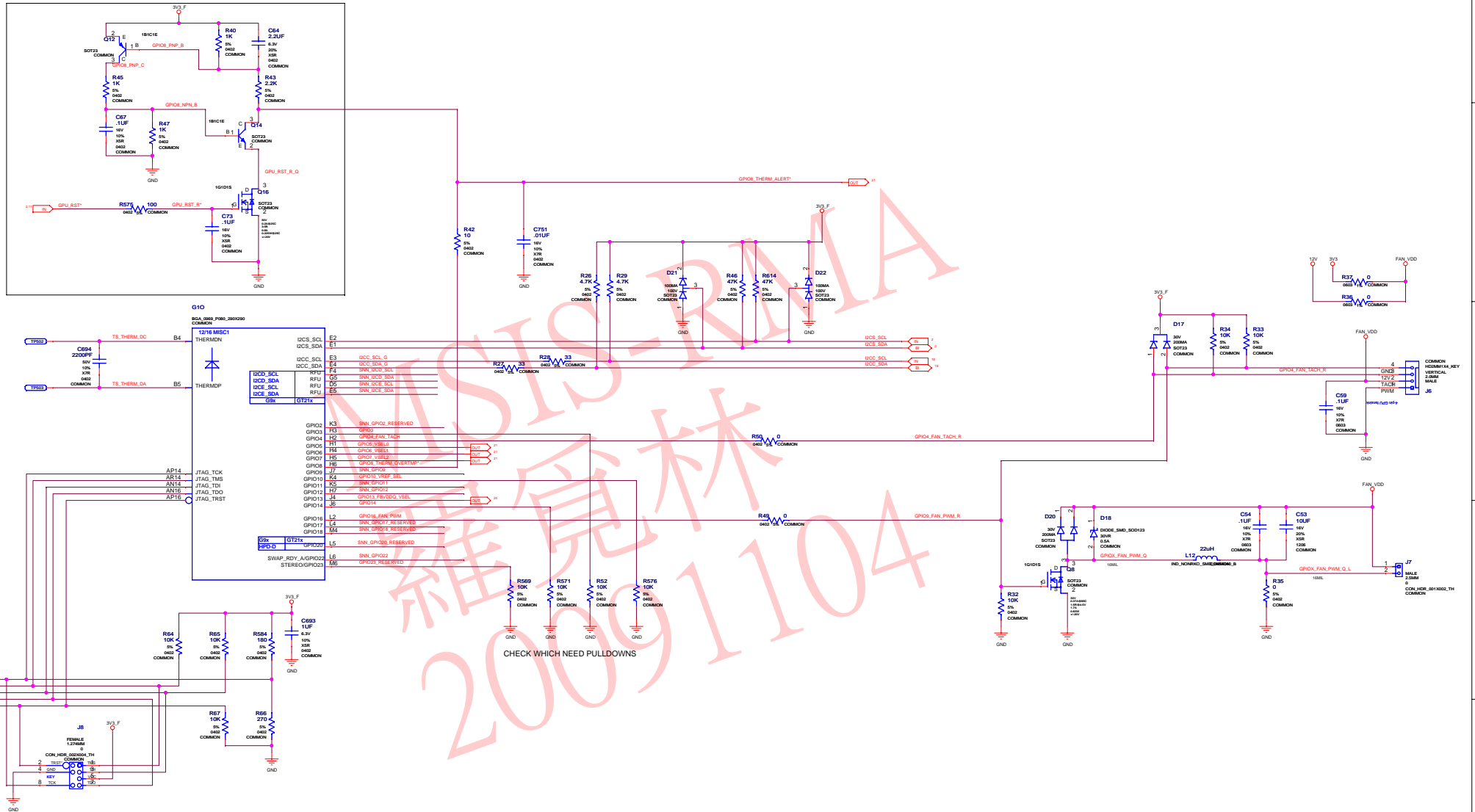
NETNAME	MIN_LINE_WIDTH
GPU_PLLVDD	12M
GPU_PLLVDD_SP	12M
XTAL_IN	12M
XTAL_OUT	12M

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THERM ALERT, FAN CONTROL, GPIO & JTAG

THERM ALERT LATCH



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PAGE DETAIL	FAN CONTROL, THERMAL ALERT, GPIO, JTAG

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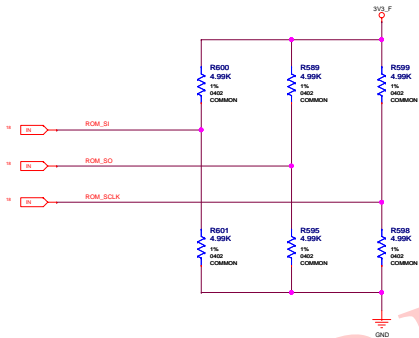
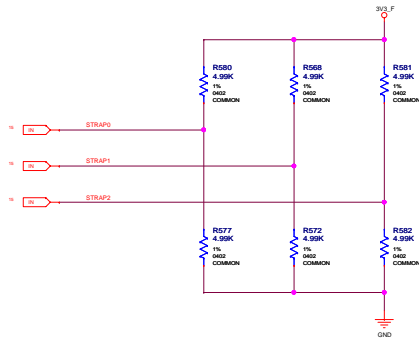
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STRAPPING, VBIOS, INFOROM

STRAPPING OPTIONS



STRAP1[3..0] = 0x8 (3GIO_PADCFG DSKTOP default plus 0x8)

STRAP2[3..0] = 0xB (PCI_DEVID = 0xCAB)

ROM_SO[0] = 1 (VGA Device Enable)

ROM_SO[1] = 0 (SMB_ALT_ADDR, default (1GPU))

ROM_SO[2] = 0 (FB aper. size 256MB, default)

ROM_SO[3] = 0 (XCLK_417, default)

ROM_SCLK[0] = 0 (PEX_PLL_EN_TERM100 disabled, default)

ROM_SCLK[1] = 1 (SLT_CLK_CFG, default)

ROM_SCLK[2] = 1 (VBIOS RM present, default)

ROM_SCLK[3] = 0 (PCI_DEVID[4] = 0)

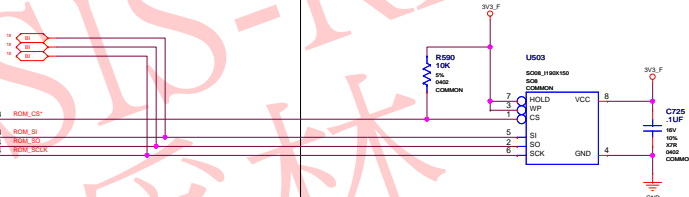
ROM_SI[3..0] = RAMCFG[3..0]

0x0001	Qimonda	128-bit, GDDR5
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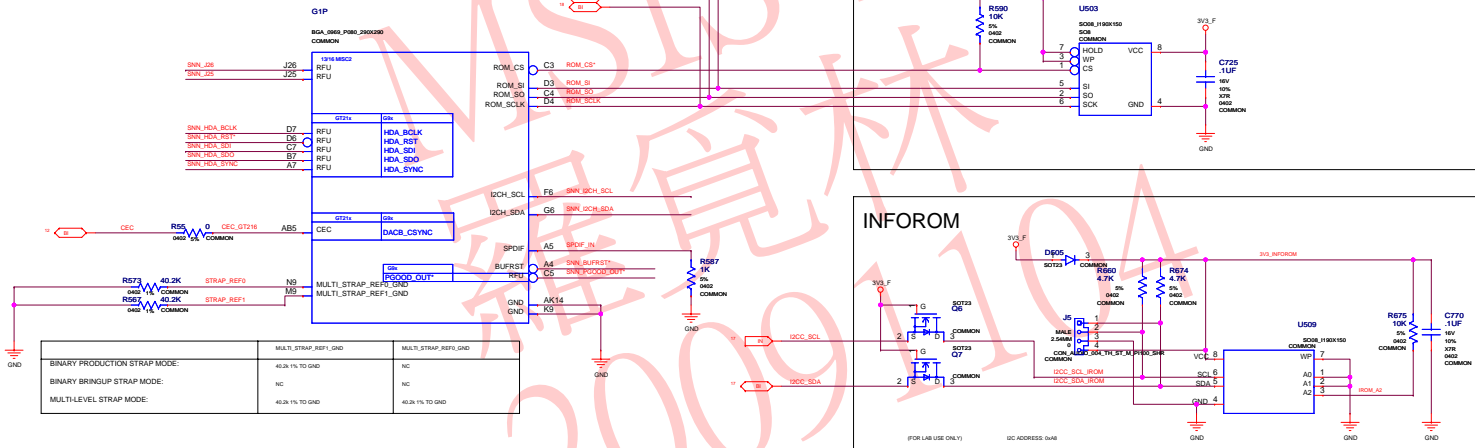
0x0010	Hynix	128-bit, GDDR5
0x0011	Samsung	128-bit, GDDR5

DATA

BIOS ROM(serial)



INFORM



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FBVDDQ Power Supply 1.35-1.50V@15A

[illegible]

	GPIO13
FBVDDQ = 1.35V	0
FBVDDQ = 1.55V	1

$$\begin{aligned} \text{FBVDDQ} &= \text{VREF} * (1 + (\text{Rtop} / \text{Rbot})) \\ 1.358\text{V} &= 0.8\text{V} * (1 + (698 / 1\text{K})) \end{aligned}$$

$$\begin{aligned} \text{FBVDDQ} &= \text{VREF} * (1 + (\text{Rtop} / \text{Rbot} \parallel \text{Rbot1})) \\ 1.548\text{V} &= 0.8\text{V} * (1 + (698 / (1\text{K} \parallel 2.94\text{K}))) \end{aligned}$$

NET		MIN_LEN_WIDTH	VOLTAGE	IN_NET_MAX_CURRENT
RVDD0	RVDD0	120kΩ	1.8V	60A
RVDD0	RVDD0	200kΩ	1.8V	30A
PEX_VDD0	PEX_VDD0	200kΩ	1.05V	30A
PS_FB_BOOT	PS_FB_BOOT	120kΩ		
PS_FB_BOOT_A	PS_FB_BOOT_A	120kΩ		
PS_FB_USATE	PS_FB_USATE	120kΩ		
PS_FB_USATE_B	PS_FB_USATE_B	120kΩ		
PS_FB_PHASE	PS_FB_PHASE	200kΩ		50A
PS_FB_USATE	PS_FB_USATE	120kΩ		
PS_FB_VCC12	PS_FB_VCC12	120kΩ	12V	
PS_FB_VCC5	PS_FB_VCC5	120kΩ	5V	
PS_FB_VVCC5	PS_FB_VVCC5	120kΩ	5V	
PS_V12_DR	PS_V12_DR	120kΩ		
PS_V12_FB	PS_V12_FB	120kΩ		
PS_V12_BC	PS_V12_BC	120kΩ		
PS_FB	PS_FB	120kΩ		
PS_FB_FB	PS_FB_FB	120kΩ		
PS_FB_SVFLY	PS_FB_SVFLY	120kΩ		
PS_FB	PS_FB	120kΩ		
PS_FB_VO	PS_FB_VO	120kΩ		
PS_FB_SNB	PS_FB_SNB	120kΩ		
PS_FB_COMP	PS_FB_COMP	120kΩ		
PS_FB_SC_CP	PS_FB_SC_CP	120kΩ		
PS_FB_E	PS_FB_E	120kΩ		
PS_FB_C	PS_FB_C	120kΩ		

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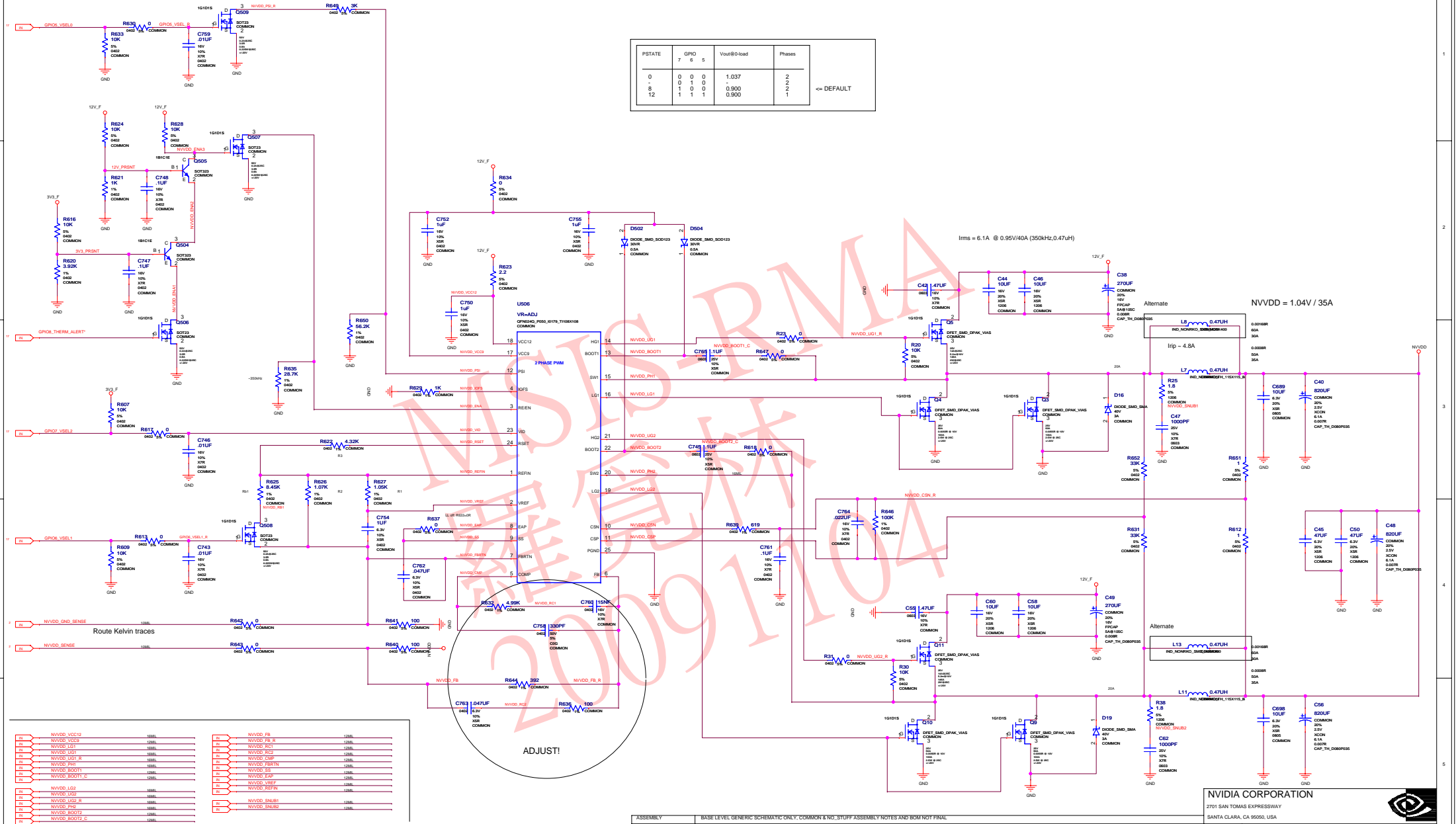
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBVDDQ SINGLE PHASE SWITCHER, PEX_VDD LINEAR

POWER SUPPLY: NVVDD DUAL-PHASE SWITCHER

NVVDD Power Supply 35A@1.04V



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