

P1041-B01 GF104

GF104-300, 768MB/1536MB, GDDR5 192b 32M/64Mx32  
DVI-I-DL, DVI-I-DL/DP, mHDMI

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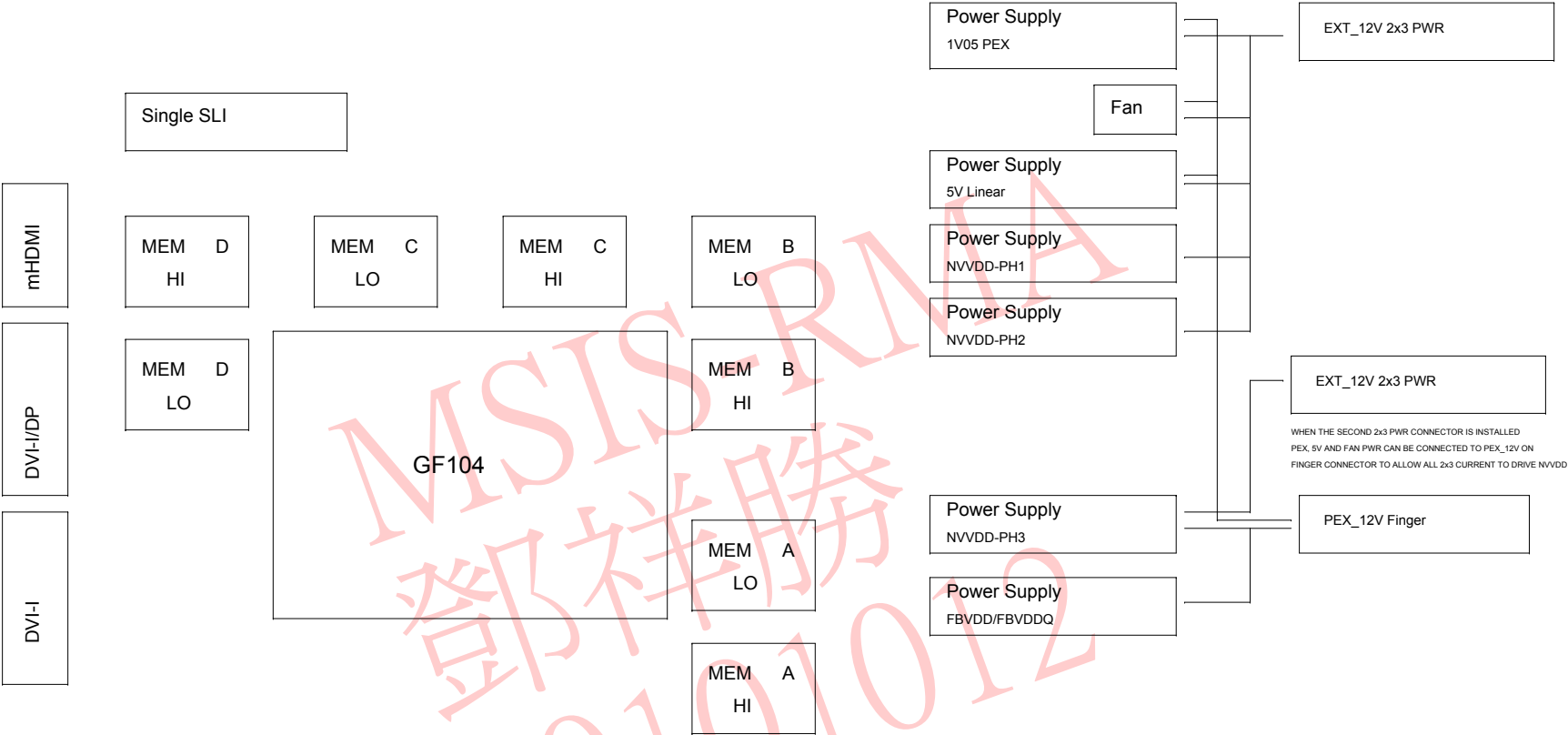
P4~P14 add 铬 &~<>~才腹(copy V238 11)  
P14, 埃T呼蹈結  
P16, 埃C878 C876马 470UF糖 篆臂  
P19,add D-SUB钡 copy V804-11 D-SUBノI2CB舱  
P21, 埃J3 DVI Mid 钡 結隔  
P22, 埃DP场だ 結隔  
P23, mHDMI钡 ㄟ肚参 HDMI钡 copy V804-11  
P27, 锣5Vcm钡DP powerそノ12V DP 奔 T 砧场だ  
埃12Vく倒DP 铬 結场だ U4 footprintㄟT  
P30,31 埃core output篆臂 colay and change all dip篆臂to  
msi footprint Tフ海  
P32,PEX6 & PEX\_12V input 篆稍ㄟ R50, 埃藪L12 colay 4  
LB 篆稍  
P33, 6 厩撻, 撒 k兵

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11041-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-11041-0000-300	P1041 GF104-300 768MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
2	SKU0010	600-11041-0010-300	P1041 GF104-300 1536MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
3	Q51	600-11041-0000-Q51	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
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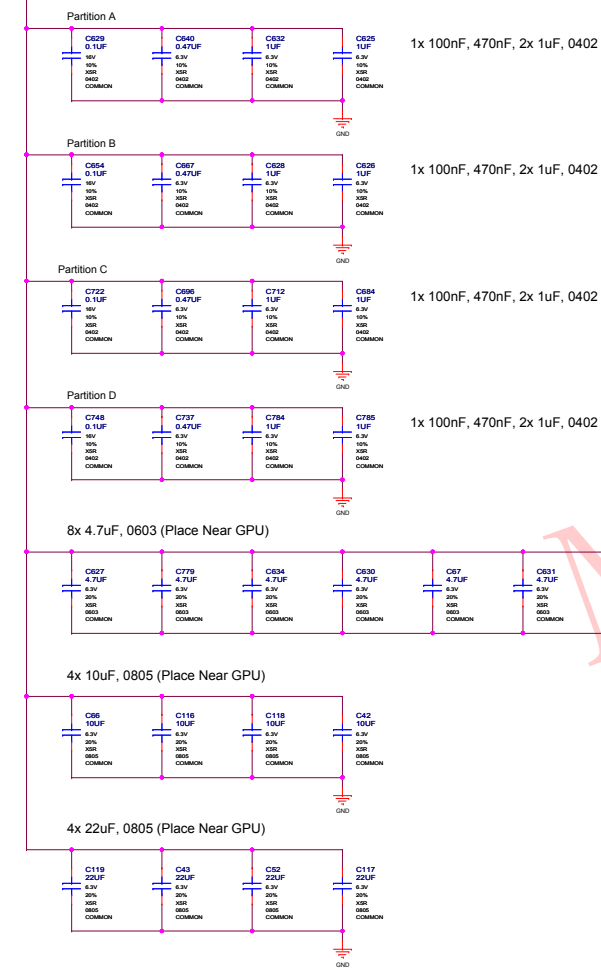
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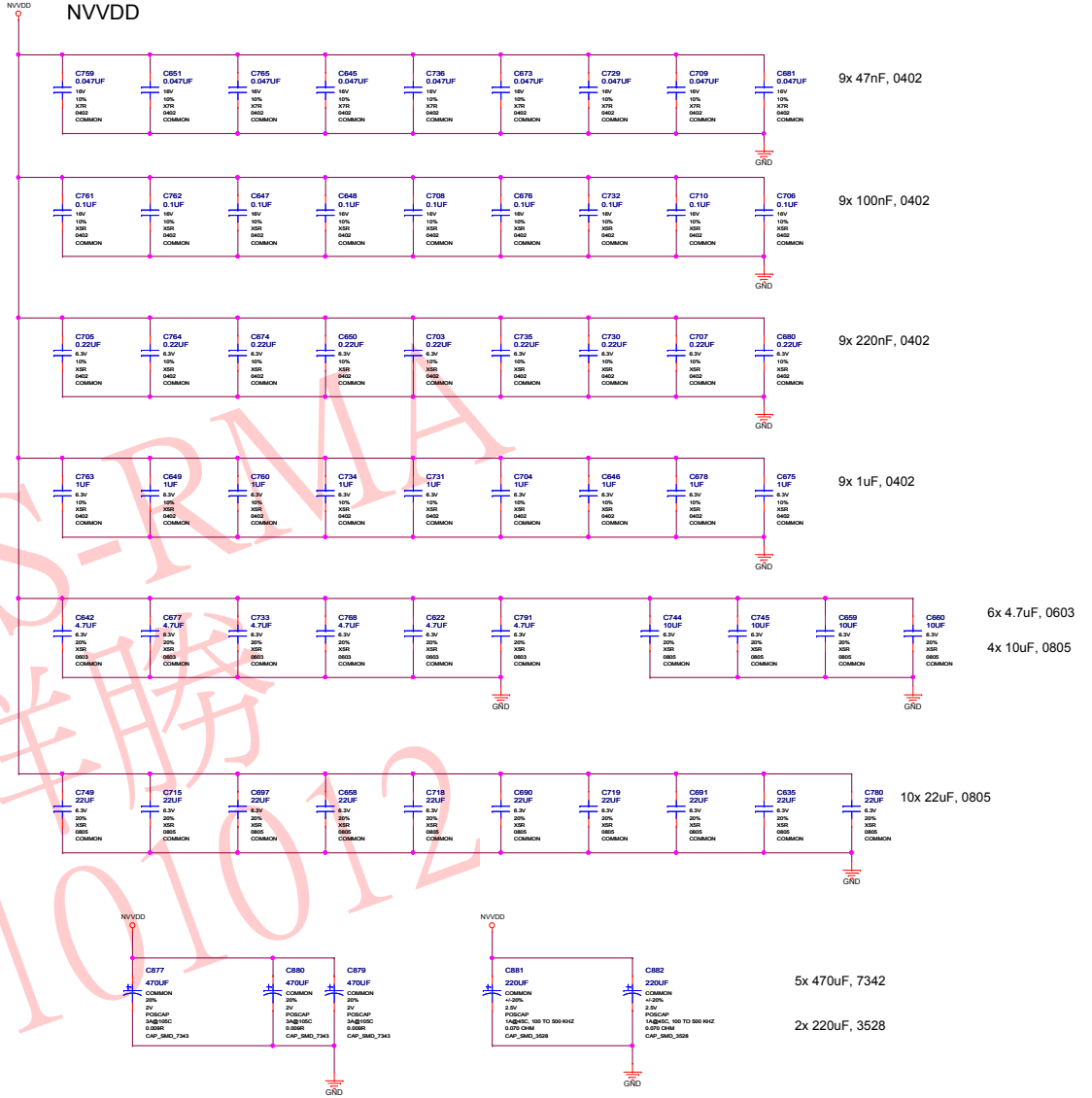




FBVDDQ



NVDD



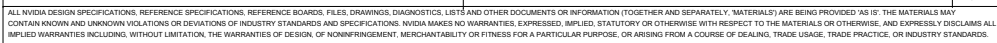
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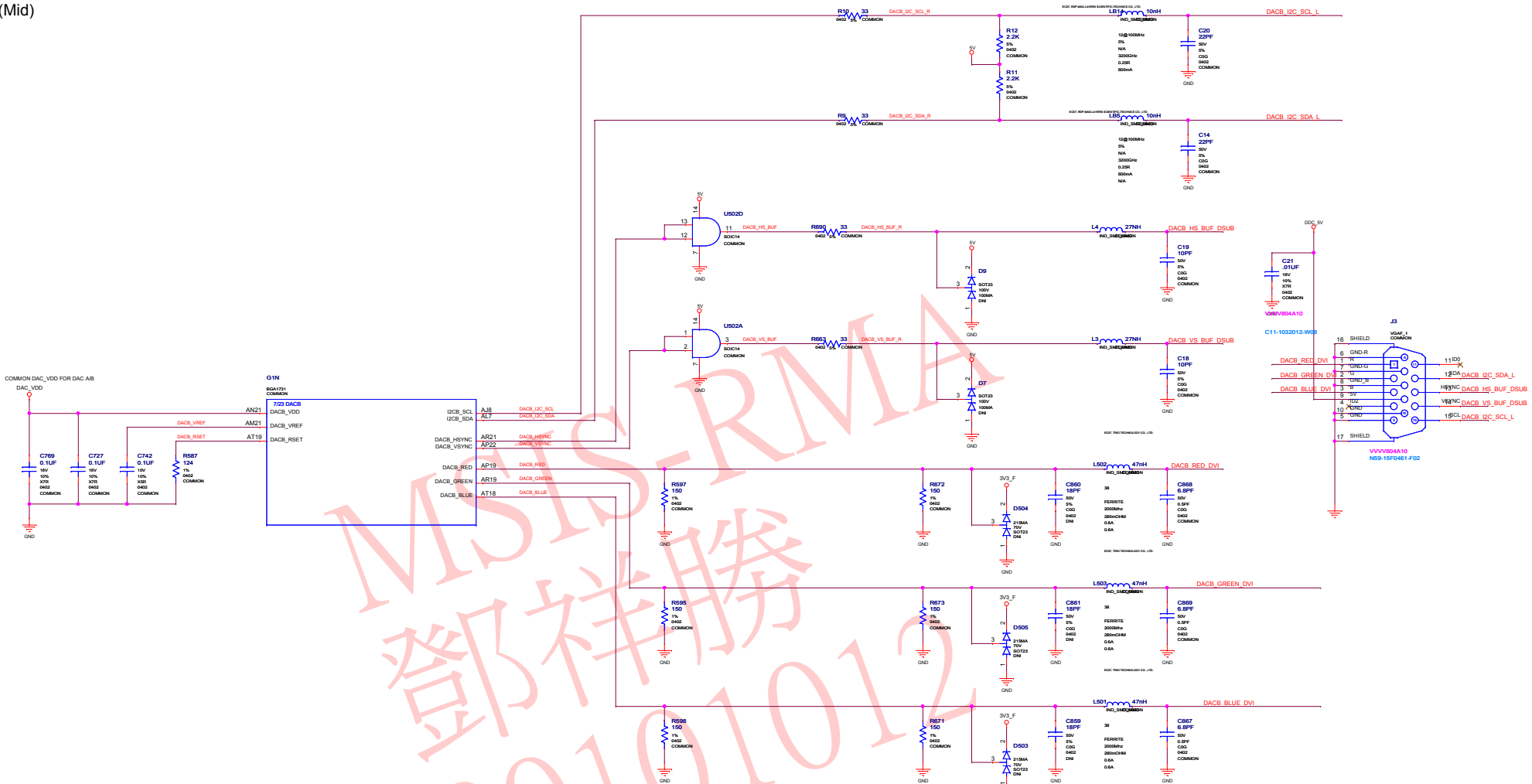
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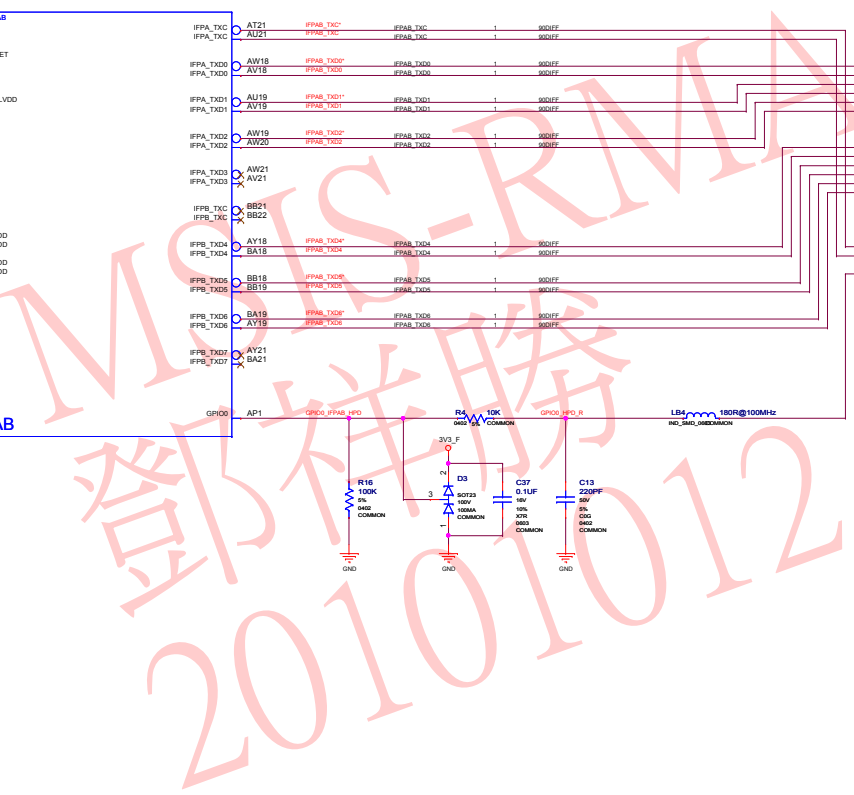
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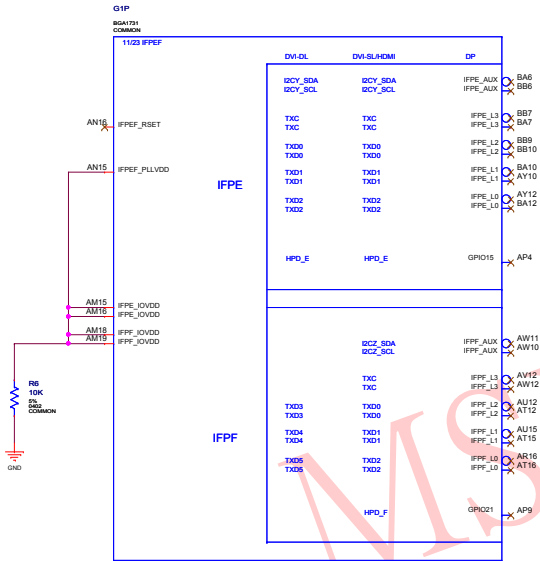


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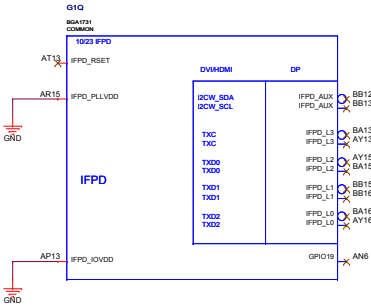
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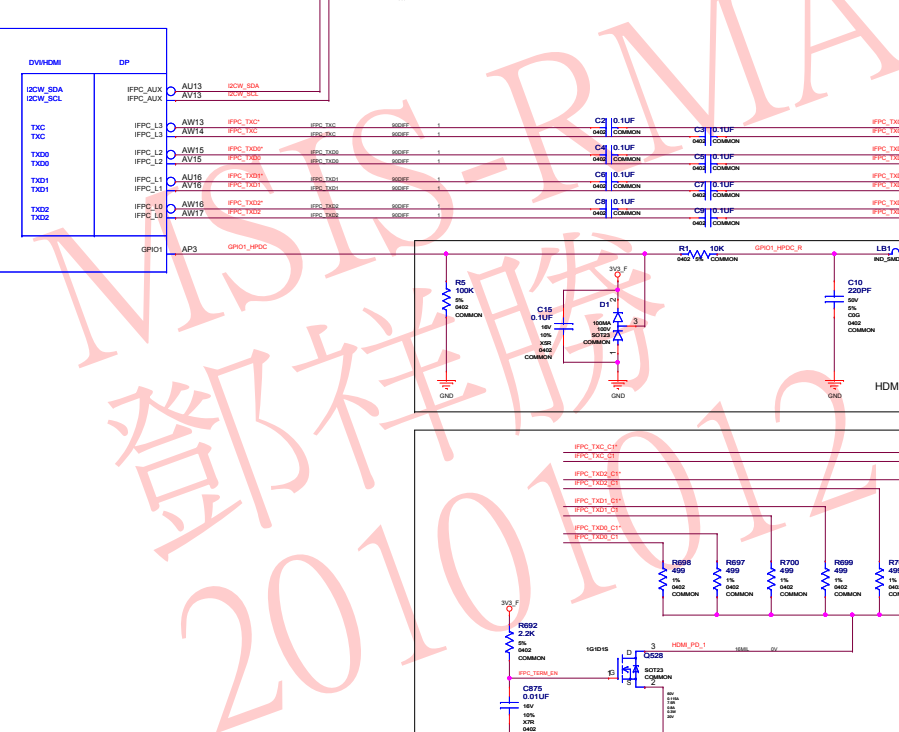


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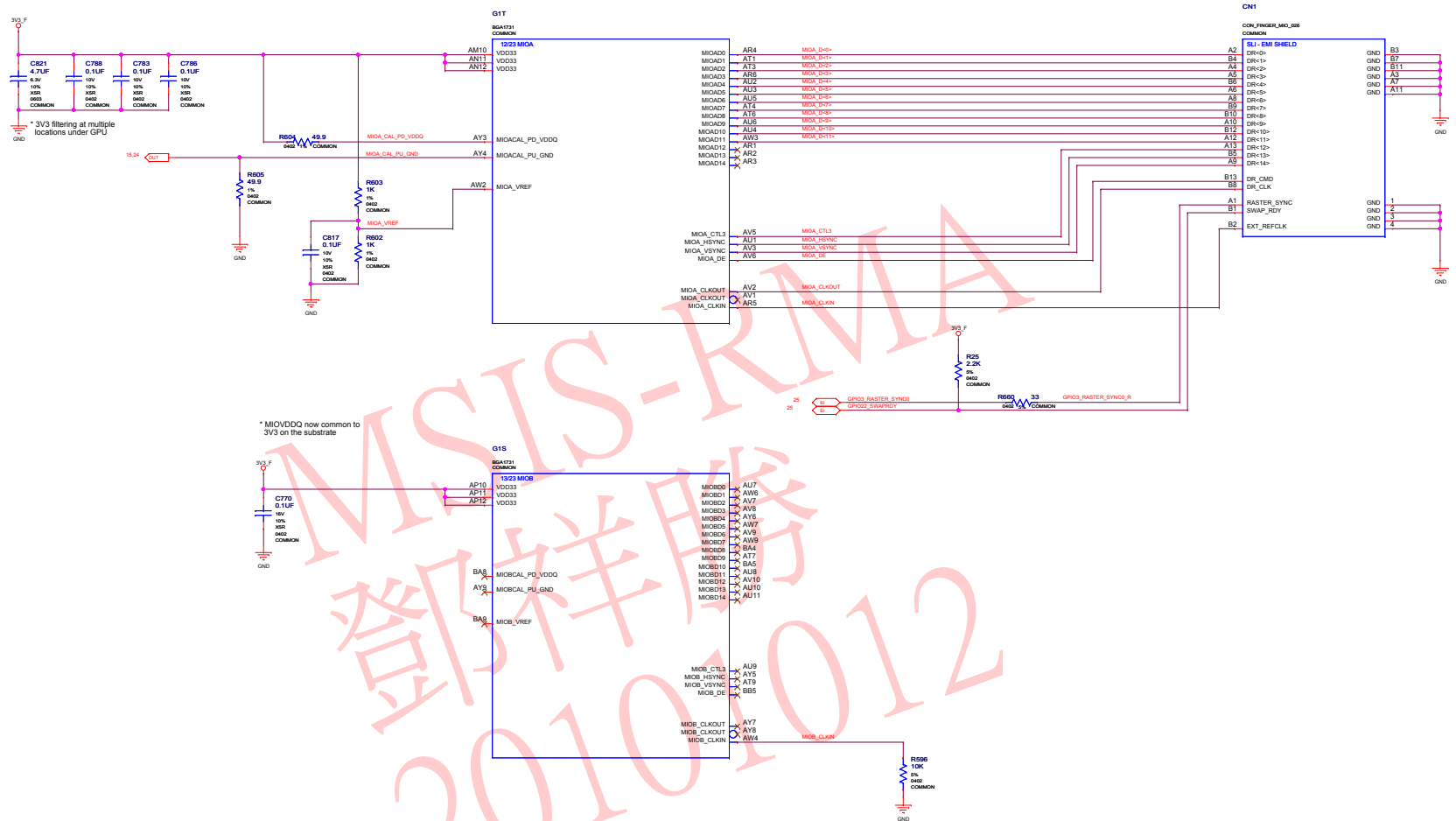
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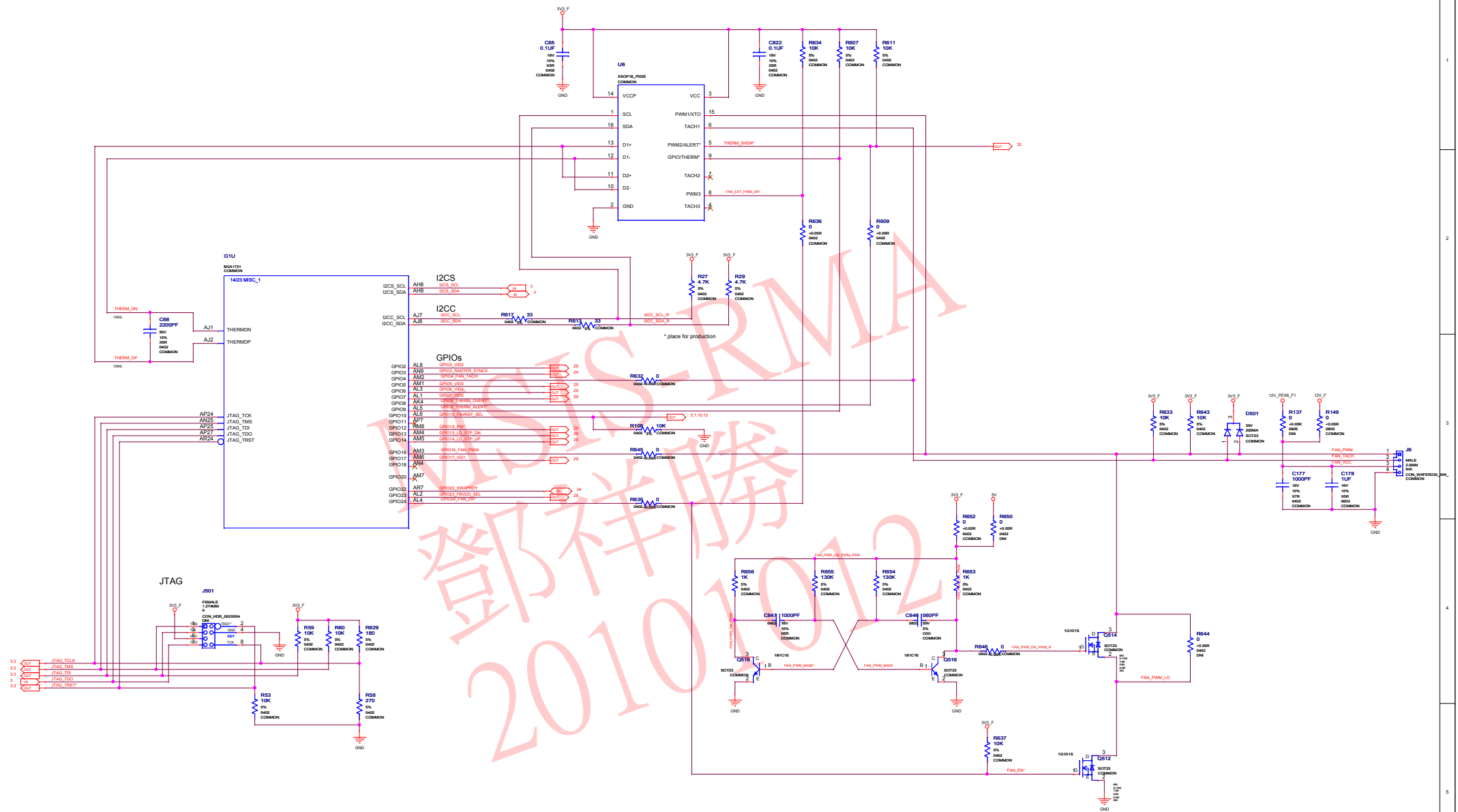
\* MIOVDDQ now common to 3V3 on the substrate

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WORK REV	A
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_3V3UFF ASSEMBLY NOTES AND BOM NOT FINAL
PAZEE DETAIL	Misc Fan Thermal JTAG GPIO

Page26: Misc: ROM, HDCP, XTAL, Straps

STRAP0	USER_BIT [3..0]	0000 => 5K PD
STRAP1	3GIO_PADCFG_LUT_ADR	0000 =>5K PD 0000 Desktop
STRAP2	PCI_DEVID [3..0]	0010 For 0x0E22 => 15K PD 0100 For 0x0E24 => 25K PD
ROM_SI	RAMCFG[0]	32Mx32 256-bit Samsung for SNU 10-bit memory 0111: 1Kb 25K 32Mx32 256-bit Hynix for SNU 10 2nd memory 0110: PD 15K
	RAMCFG[1]	
	RAMCFG[2]	32Mx32 192-bit Samsung for SNU 0-bit memory 1011: 1Kb 25K 32Mx32 192-bit Hynix for SNU 0 2nd memory 1010: PU 15K
	RAMCFG[3]	
ROM_SO	VGA_DEVICE	1
	SMB_ALT_ADDR	0 10k PD
	FB[0]_BAR_SIZE	0
ROM_SCLK	XCLK_417	0
	PEX_PLL_EN_TERM100	1 ENABLED
	SLOT_CLK_CFG	1 ENABLE
	SUB_VENDOR	1 Dedicated BIOS
	PCI_DEVID_EXT	0 0xC

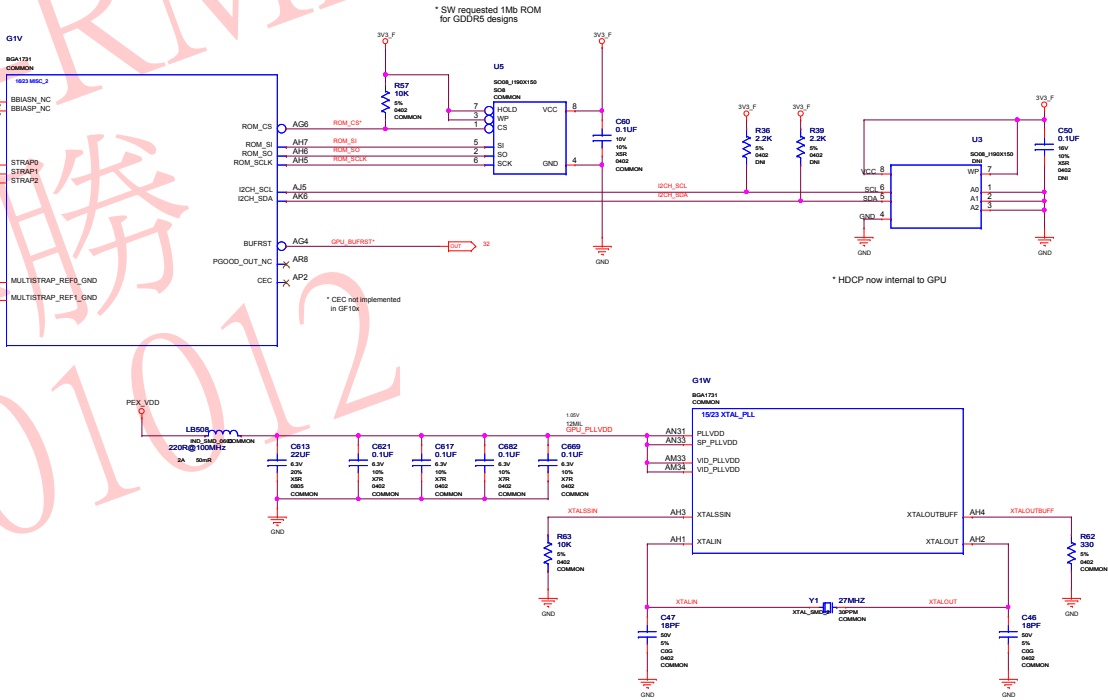
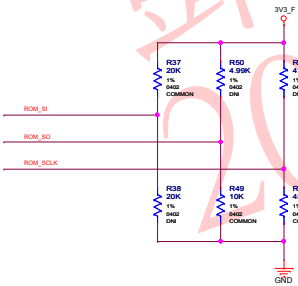
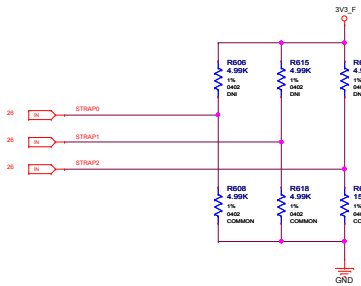
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3..0] Config Width	Vendor
0000	Reserved
0001	32Mx32 256-bit Qimonda
0010	32Mx32 256-bit Hynix
0011	32Mx32 256-bit Samsung
0100	Reserved
0101	64Mx32 256-bit Qimonda
0110	64Mx32 256-bit Hynix
0111	64Mx32 256-bit Samsung
1000	Reserved
1001	32Mx32 192-bit Qimonda
1010	32Mx32 192-bit Hynix
1011	32Mx32 192-bit Samsung
1100	Reserved
1101	64Mx32 192-bit Qimonda
1110	64Mx32 192-bit Hynix
1111	64Mx32 192-bit Samsung

MISC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE
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	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	45.2k 1% TO GND	NC
BINARY BRINGUP	NC	NC
MULTI-LEVEL	45.2k 1% TO GND	45.2k 1% TO GND



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PAGE DETAIL	Misc ROM, TRCP, XTAL, Straps

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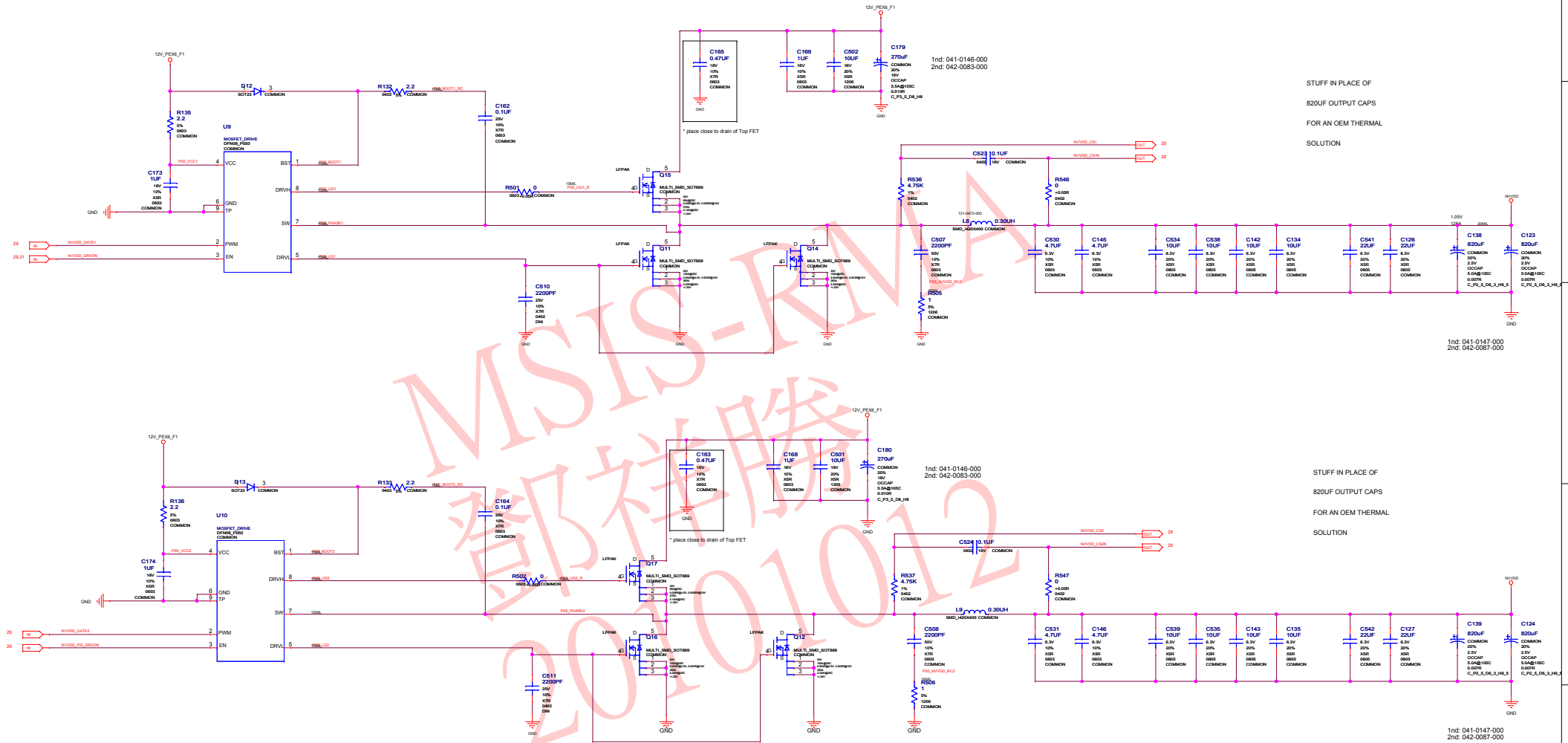


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PAGE DETAIL	PS: FBVDDXQ

PAGE	
DATE	12-MAY-2010



Input ripple (Irms)/phase = 10.175A @ 90A  
Irms shared across phase 1-2 input caps



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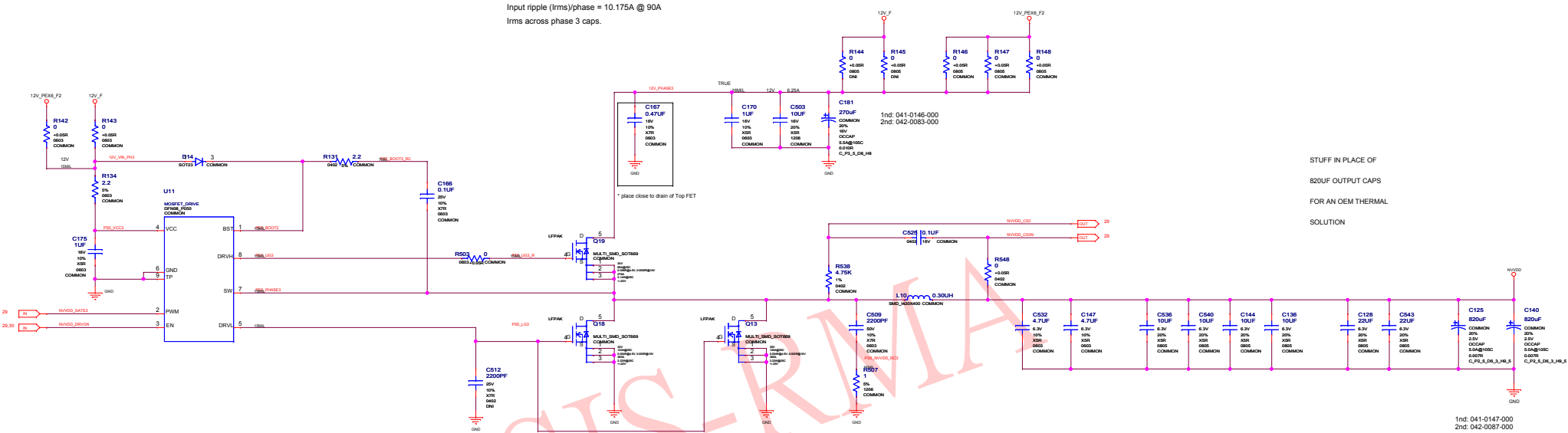
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BOARD REV APAGE 1  
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Input ripple (Irms)/phase = 10.175A @ 90A  
Irms across phase 3 caps.

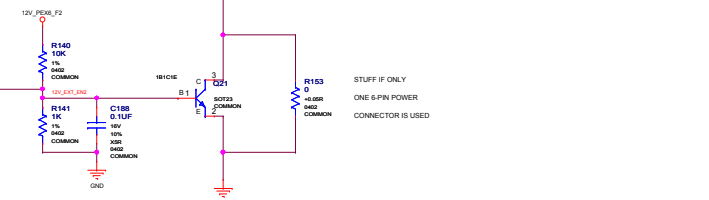
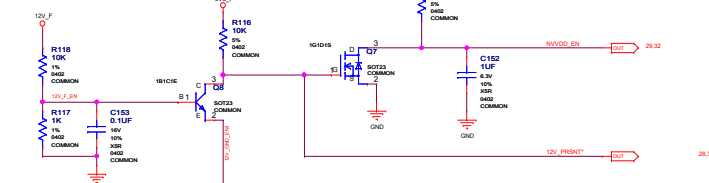
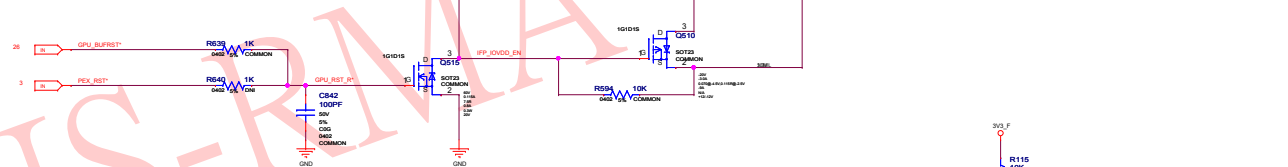
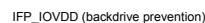
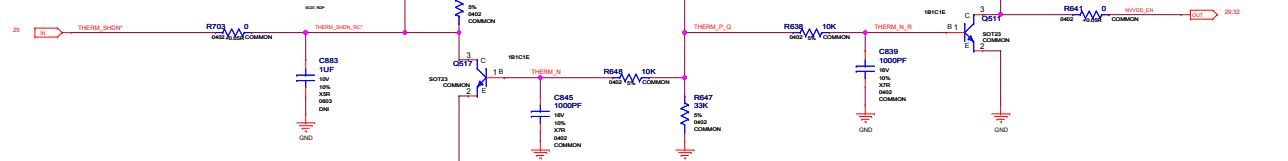
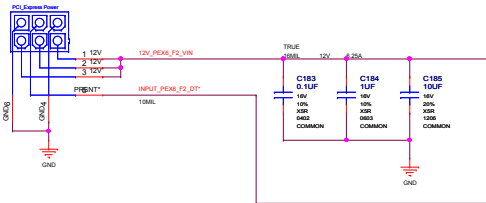
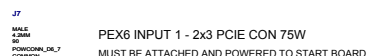
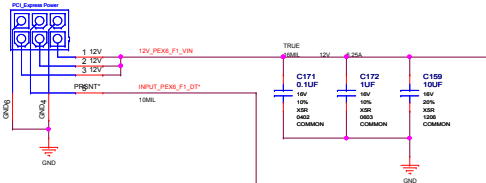
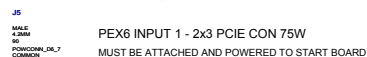
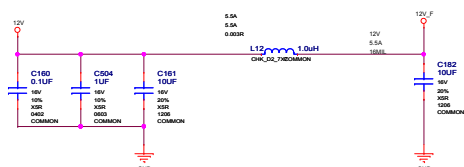
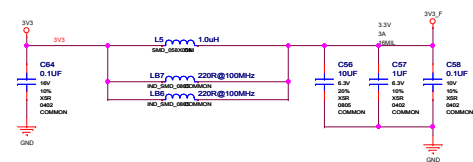


STUFF IN PLACE OF  
820UF OUTPUT CAPS  
FOR AN OEM THERMAL  
SOLUTION

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PAGE: DETAIL	P3: NVVDD Phase 3

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PAGE DETAIL	PS: Inputs, Shutdown

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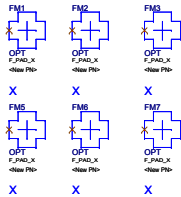
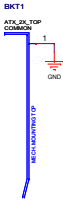
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Brackets:

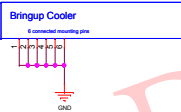
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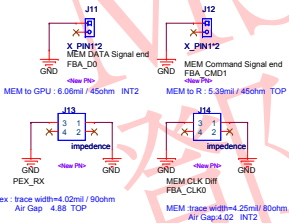
Bracket Screw



Cooler/GPU Stiffener



P1041 MOUNTING HOLE LOCATIONS



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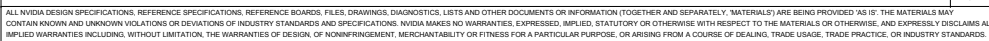
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PAGE DETAIL	11/24

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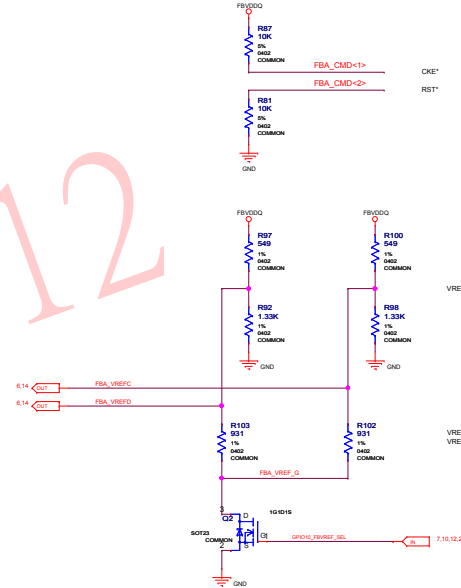
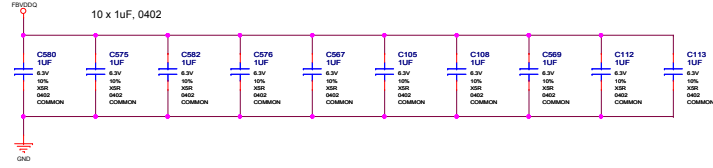
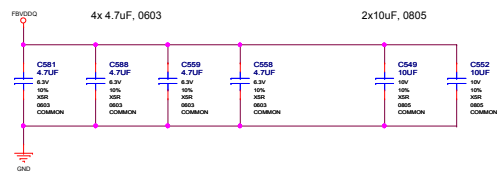
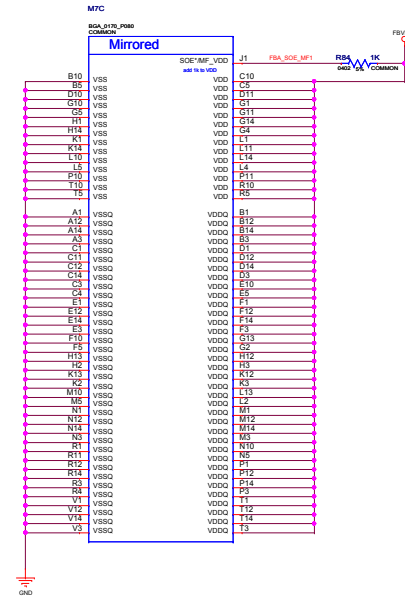
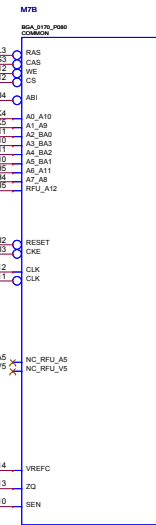
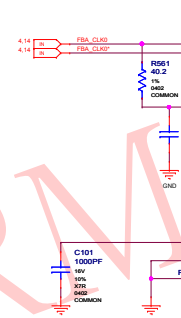
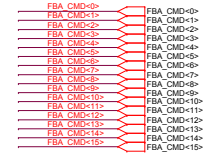
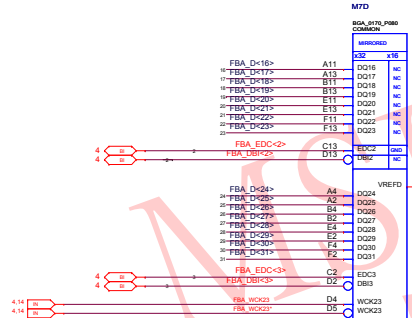
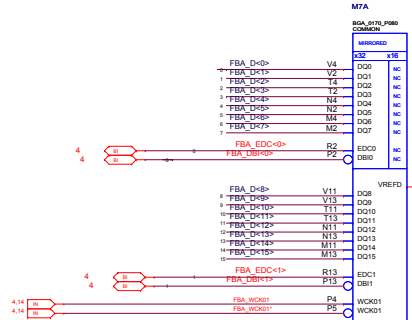






FtsA-D1  
FtsA-D2  
FtsA-D3  
FtsA-D4  
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FtsA-D31


$$V_{REF} = 1.5 * [1.33K / (549 + 1.33K)] = 1.05V$$
$$V_{REF} = 1.5 * ((542/542+549)) = 0.75V$$
$$V_{REF} = 1.35 \cdot ((542/542+549)) = 0.67V$$

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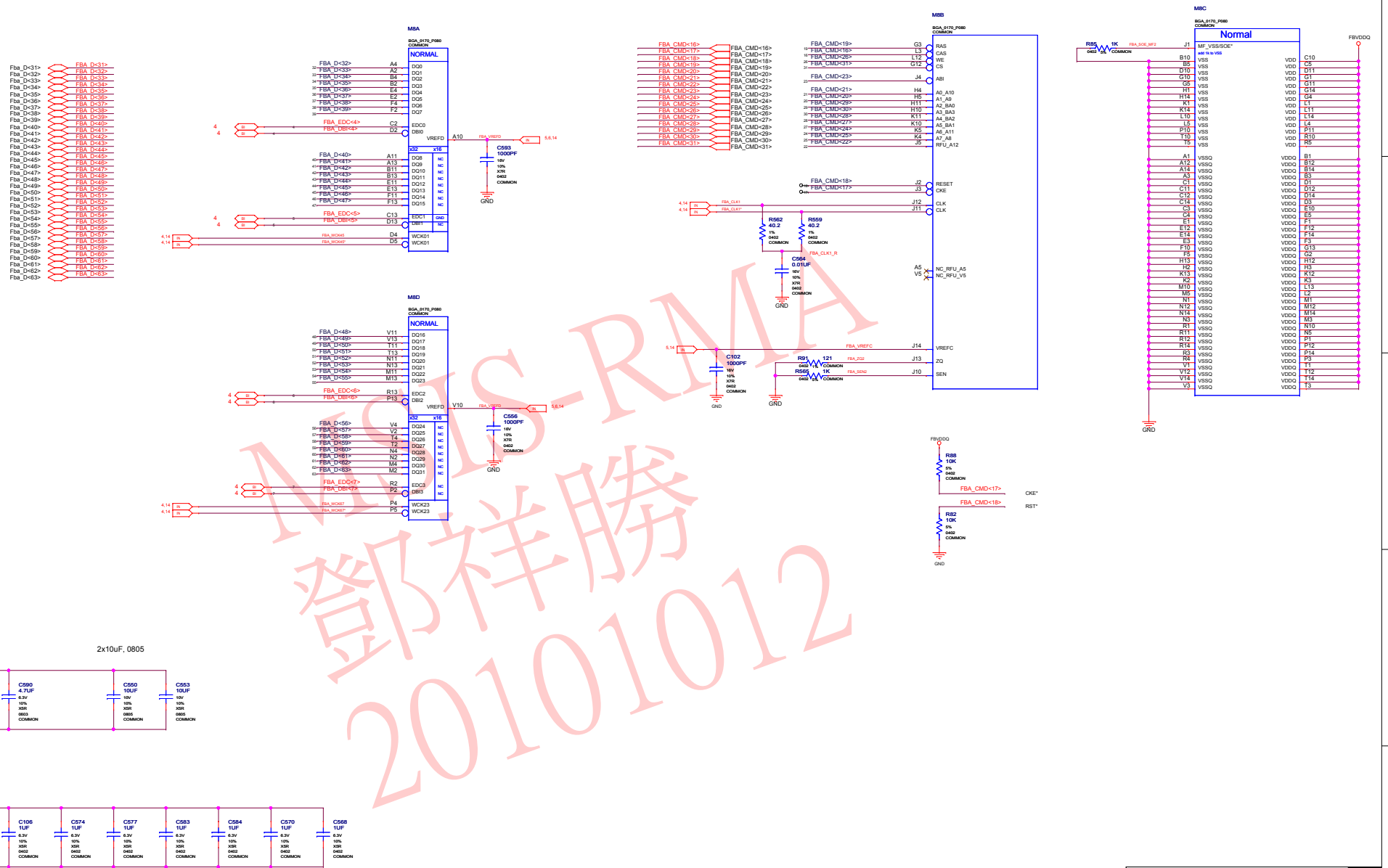
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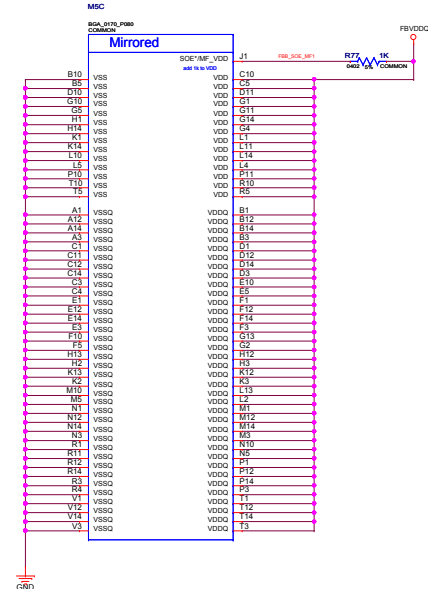
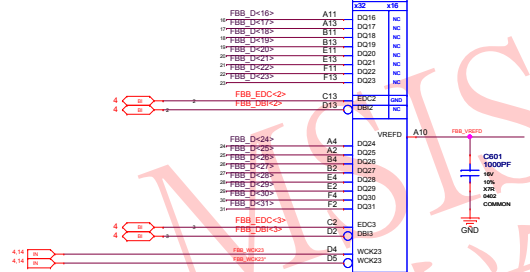
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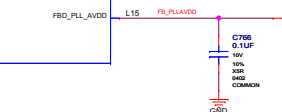
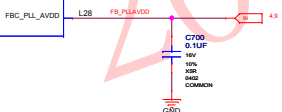
PAGE	
DATE	12-MAY-2010

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- \*\* Vref switching options:
- internal Vref should be POR for VrefID
- potential for update

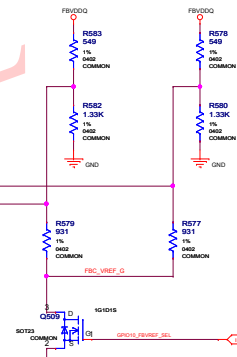
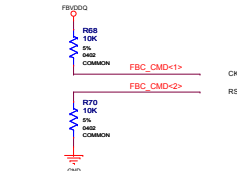
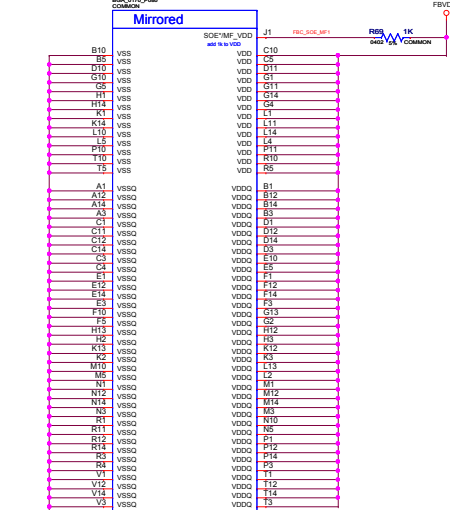
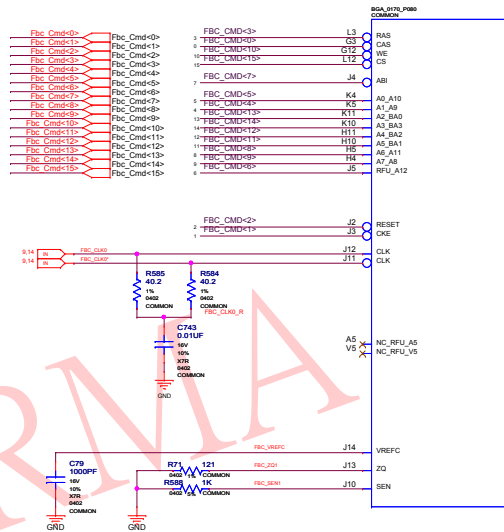
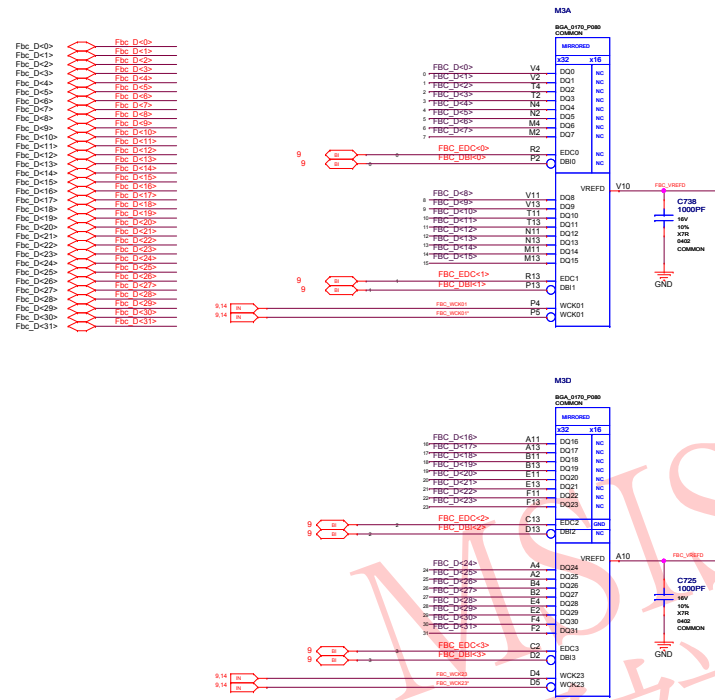


GDDR5 CMD Mapping		
CMD	0..31	32..63
CM00	CAS0	
CM01	CAS1	
CM02	RS0	
CM03	RS1	
CM04	AL_A0	
CM05	AL_A1	
CM06	AL_A2	
CM07	AL_A3	
CM08	AL_A4	
CM09	AL_A5	
CM10	AL_A6	
CM11	AL_A7	
CM12	AL_A8	
CM13	AL_A9	
CM14	AL_A10	
CM15	AL_A11	
CM16	AL_A12	
CM17	AL_A13	
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CM36	AL_A32	
CM37	AL_A33	
CM38	AL_A34	
CM39	AL_A35	
CM40	AL_A36	
CM41	AL_A37	
CM42	AL_A38	
CM43	AL_A39	
CM44	AL_A40	
CM45	AL_A41	
CM46	AL_A42	
CM47	AL_A43	
CM48	AL_A44	
CM49	AL_A45	
CM50	AL_A46	
CM51	AL_A47	
CM52	AL_A48	
CM53	AL_A49	
CM54	AL_A50	
CM55	AL_A51	
CM56	AL_A52	
CM57	AL_A53	
CM58	AL_A54	
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CM423	AL_A419	
CM424	AL_A420	
CM425	AL_A421	
CM426	AL_A422	
CM427	AL_A423	
CM428	AL_A424	
CM429	AL_A4	



The top diagram shows a circuit for the FIBVDDQ pin. It features a 4x 4.7uF, 0603 capacitor array. The array consists of six capacitors connected in parallel. Each capacitor is labeled with its value (4.7uF) and part number (C754, C748, C753, C741, C777, C740). The capacitors are connected to the FIBVDDQ pin and GND. The array is labeled 4x 4.7uF, 0603. The capacitors are connected to the FIBVDDQ pin and GND. The array is labeled 4x 4.7uF, 0603.

The bottom diagram shows a circuit for the FIBVDDQ pin. It features a 10 x 1uF, 0402 capacitor array. The array consists of six capacitors connected in parallel. Each capacitor is labeled with its value (1uF) and part number (C739, C755, C776, C775, C721, C720, C75). The capacitors are connected to the FIBVDDQ pin and GND. The array is labeled 10 x 1uF, 0402. The capacitors are connected to the FIBVDDQ pin and GND. The array is labeled 10 x 1uF, 0402.



$$V_{REF} = 1.5 * [1.33K(549+1.33K)] = 1.06V$$


$$V_{REF} = 1.5 * ((542/542+549)) = 0.75V$$

$$V_{REF} = 1.35 * ((542/542+549)) = 0.67V$$

$$V_{REF} = 1.35 \cdot \left( \frac{542}{542+549} \right) = 0.67V$$

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC Partition 31..0

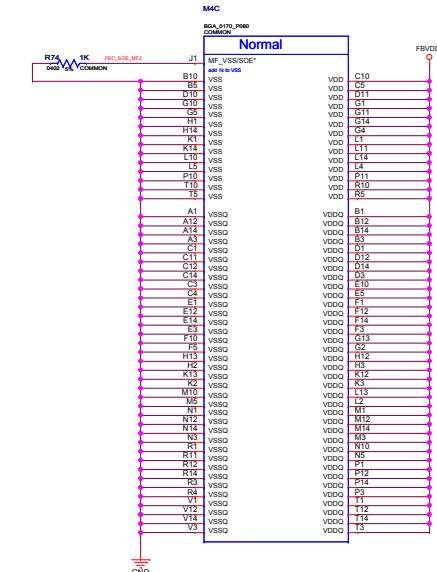
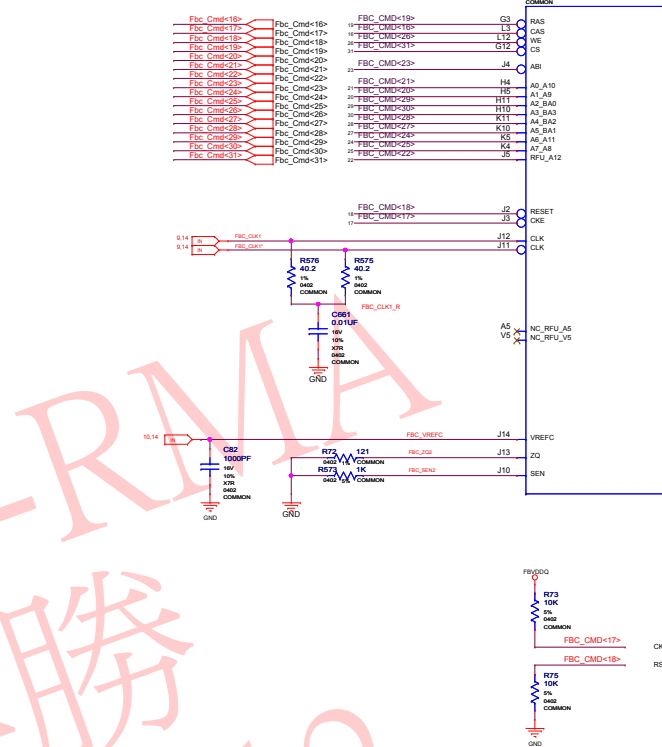
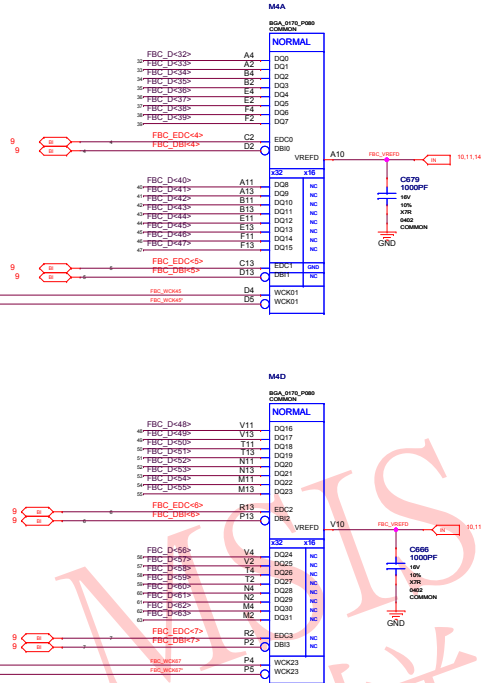
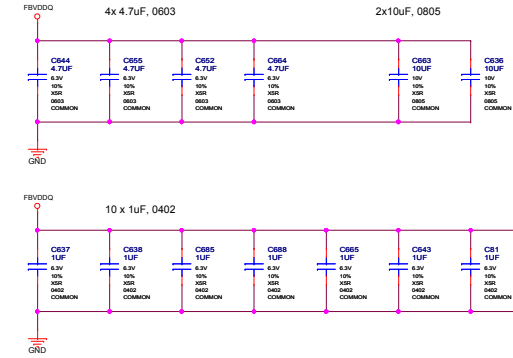
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BOM REV	A		DATE	12-MAY-2010



GDORS CMD Mapping		
CMD	0..31	32..63
0x00	CMD0	
0x01	CMD1	
0x02	RS1*	
0x03	RS0*	
0x04	AL_A0	
0x05	AL_A10	
0x06	AL_A19	
0x07	AL_A1	
0x08	AL_A8	
0x09	AL_A10	
0x0A	AL_A10	
0x0B	AL_A10	
0x0C	AL_A10	
0x0D	AL_A10	
0x0E	AL_A10	
0x0F	AL_A10	
0x10	AL_A10	
0x11	AL_A10	
0x12	AL_A10	
0x13	AL_A10	
0x14	AL_A10	
0x15	AL_A10	
0x16	AL_A10	
0x17	AL_A10	
0x18	AL_A10	
0x19	AL_A10	
0x1A	AL_A10	
0x1B	AL_A10	
0x1C	AL_A10	
0x1D	AL_A10	
0x1E	AL_A10	
0x1F	AL_A10	
0x20	AL_A10	
0x21	AL_A10	
0x22	AL_A10	
0x23	AL_A10	
0x24	AL_A10	
0x25	AL_A10	
0x26	AL_A10	
0x27	AL_A10	
0x28	AL_A10	
0x29	AL_A10	
0x2A	AL_A10	
0x2B	AL_A10	
0x2C	AL_A10	
0x2D	AL_A10	
0x2E	AL_A10	
0x2F	AL_A10	
0x30	AL_A10	
0x31	AL_A10	

\*\* Vref switching options:  
- Internal Vref should be PWR for VrefD  
- potential for update



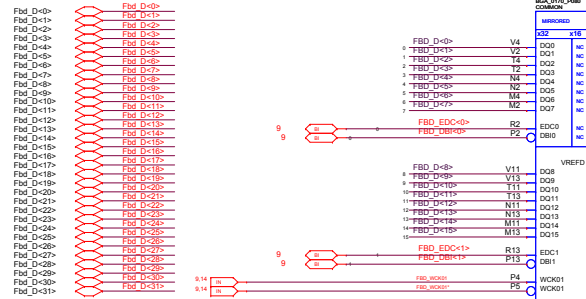
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PAGE: DETAIL	FBC PART63 63..32

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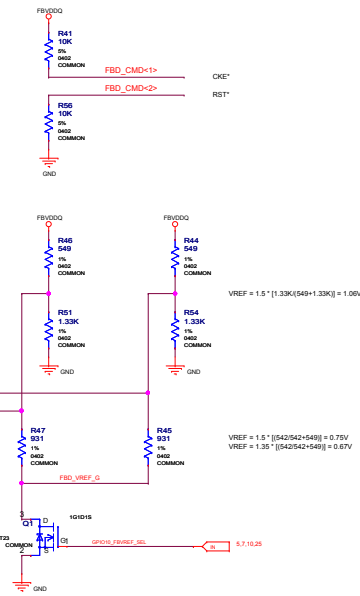
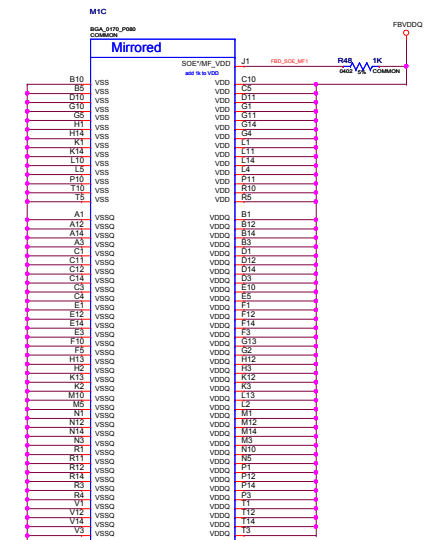
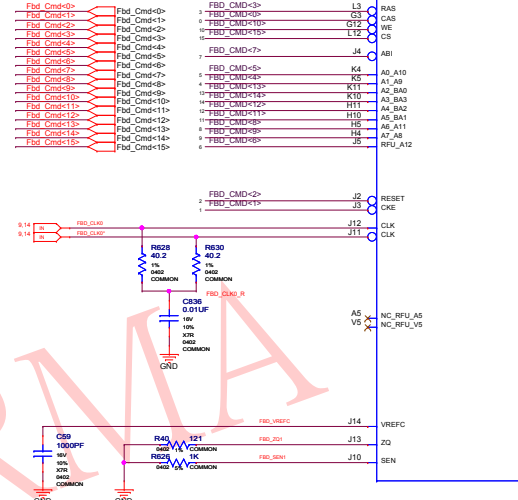
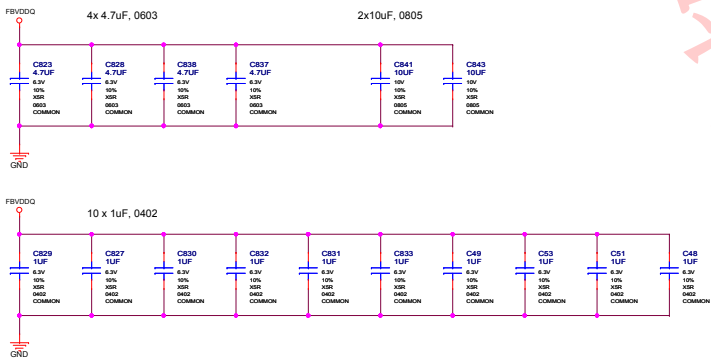
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INV_PN	600-11041-BASE-000	PAGE	12
PCB REV	P1041-B01	DATE	12-MAY-2010
WORK REV	A		



GDORS CMD Mapping		
CMD		32.83
CM00	CMP	
CM01	CMP	
CM02	REF	
CM03	RA0	
CM04	AL_A0	
CM05	AL_A0	
CM06	AL_A0	
CM07	AMP	
CM08	AL_A11	
CM09	AL_A0	
CM10	AL_A0	
CM11	AL_A0	
CM12	AL_A0	
CM13	AL_A0	
CM14	AL_A0	
CM15	AMP	
CM16	CMP	
CM17	CMP	
CM18	CMP	
CM19	RA0	
CM20	AL_A0	
CM21	AL_A0	
CM22	AL_A0	
CM23	AL_A0	
CM24	AL_A0	
CM25	AL_A0	
CM26	AL_A0	
CM27	AL_A0	
CM28	AL_A0	
CM29	AL_A0	
CM30	AL_A0	
CM31	CMP	



\*\* Vref switching options:  
- internal Vref should be POR for VrefD  
- potential for update



ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO\_01UFF ASSEMBLY NOTES AND BOM NOT FINAL FBD P060311.0

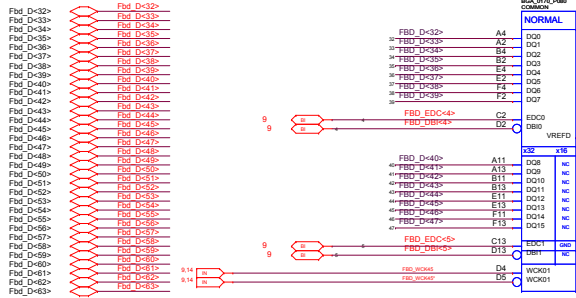
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WORK REV	A	DATE	12-MAY-2010

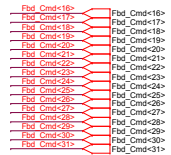
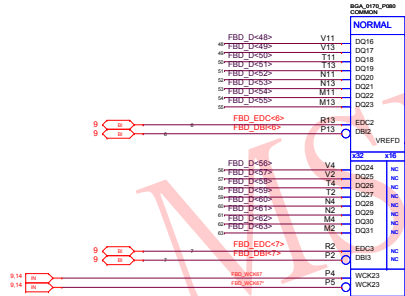
GDORS CMD Mapping

Cmd	0..31	32..63
Cmd0	Cmd0	
Cmd1	Cmd1	
Cmd2	Cmd2	
Cmd3	Cmd3	
Cmd4	AL_A0	
Cmd5	AL_A10	
Cmd6	AL_A11	
Cmd7	Cmd7	
Cmd8	AL_A1	
Cmd9	AL_A2	
Cmd10	WE	
Cmd11	AL_BA1	
Cmd12	AL_BA2	
Cmd13	AL_BA3	
Cmd14	AL_BA3	
Cmd15	Cmd15	
Cmd16	Cmd16	
Cmd17	Cmd17	
Cmd18	Cmd18	
Cmd19	Cmd19	
Cmd20	AL_A0	
Cmd21	AL_A10	
Cmd22	AL_A11	
Cmd23	Cmd23	
Cmd24	AL_A1	
Cmd25	AL_A2	
Cmd26	WE	
Cmd27	AL_BA1	
Cmd28	AL_BA2	
Cmd29	AL_BA3	
Cmd30	AL_BA3	
Cmd31	Cmd31	

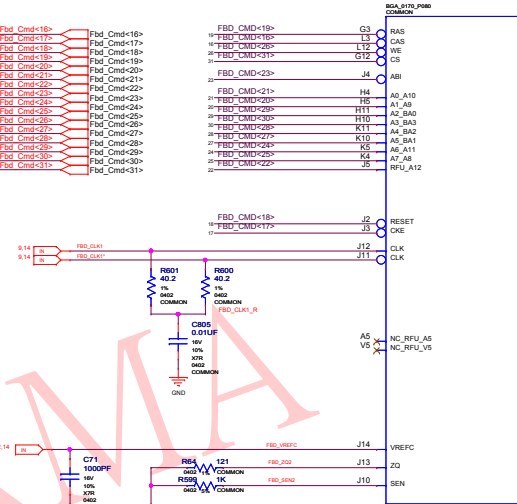
\*\* Vref switching options:  
Internal Vref should be POR for VrefD  
potential for update



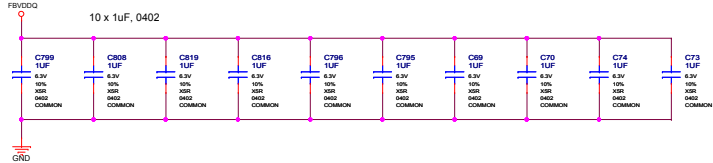
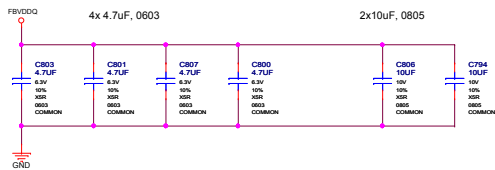
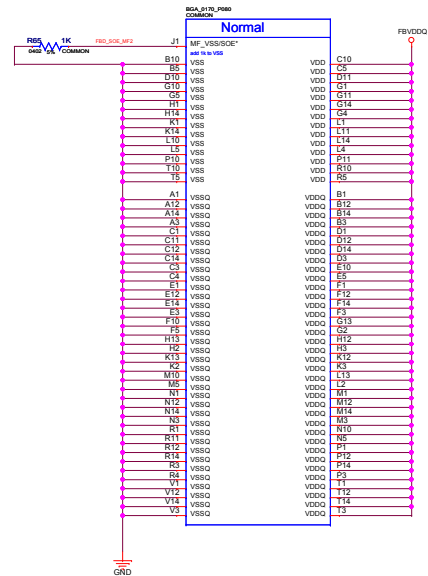
M2D



M2B



M2C



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