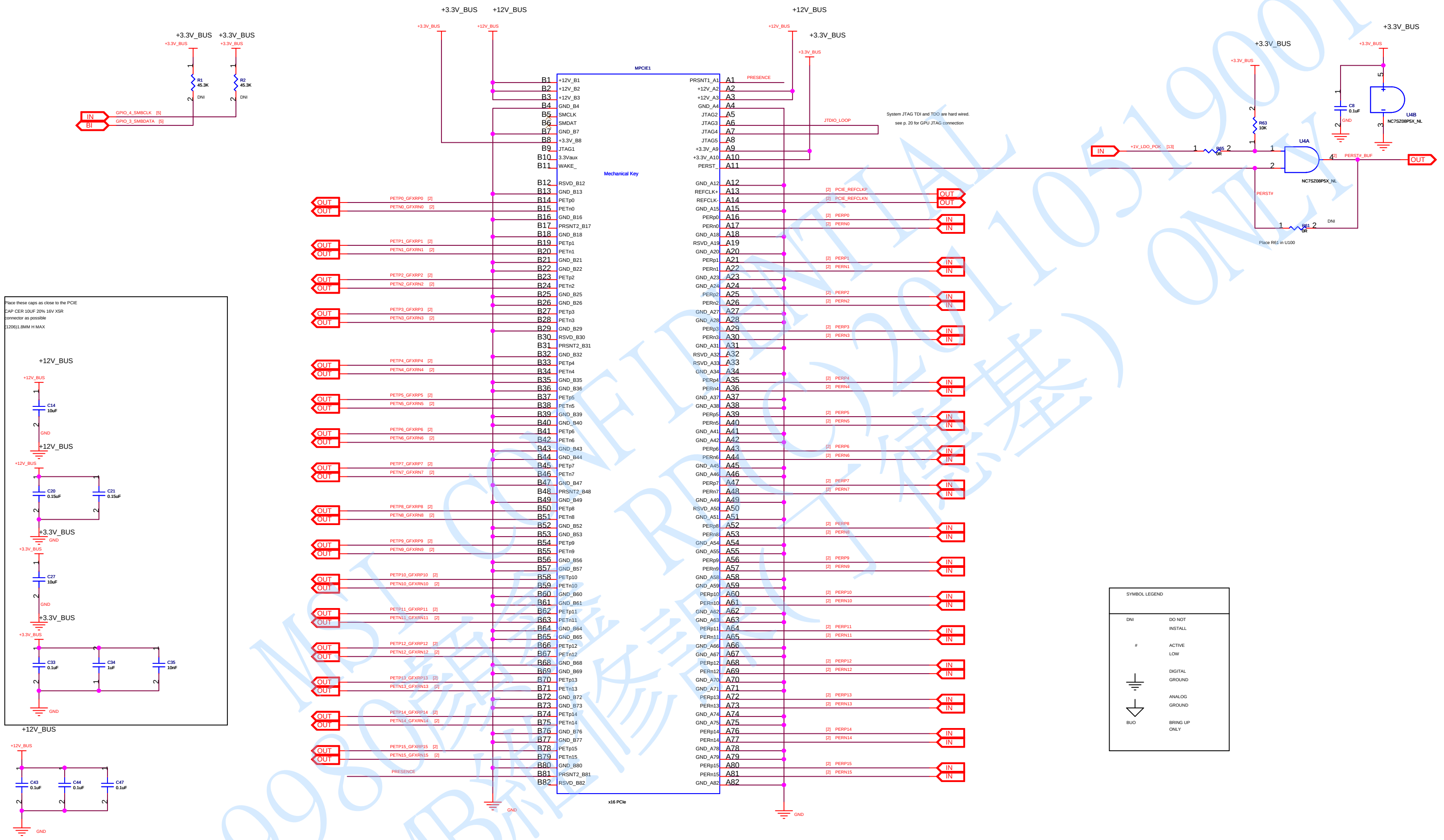
PCI-EXPRESS EDGE CONNECTOR



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SHANGHAI CHINA 201203

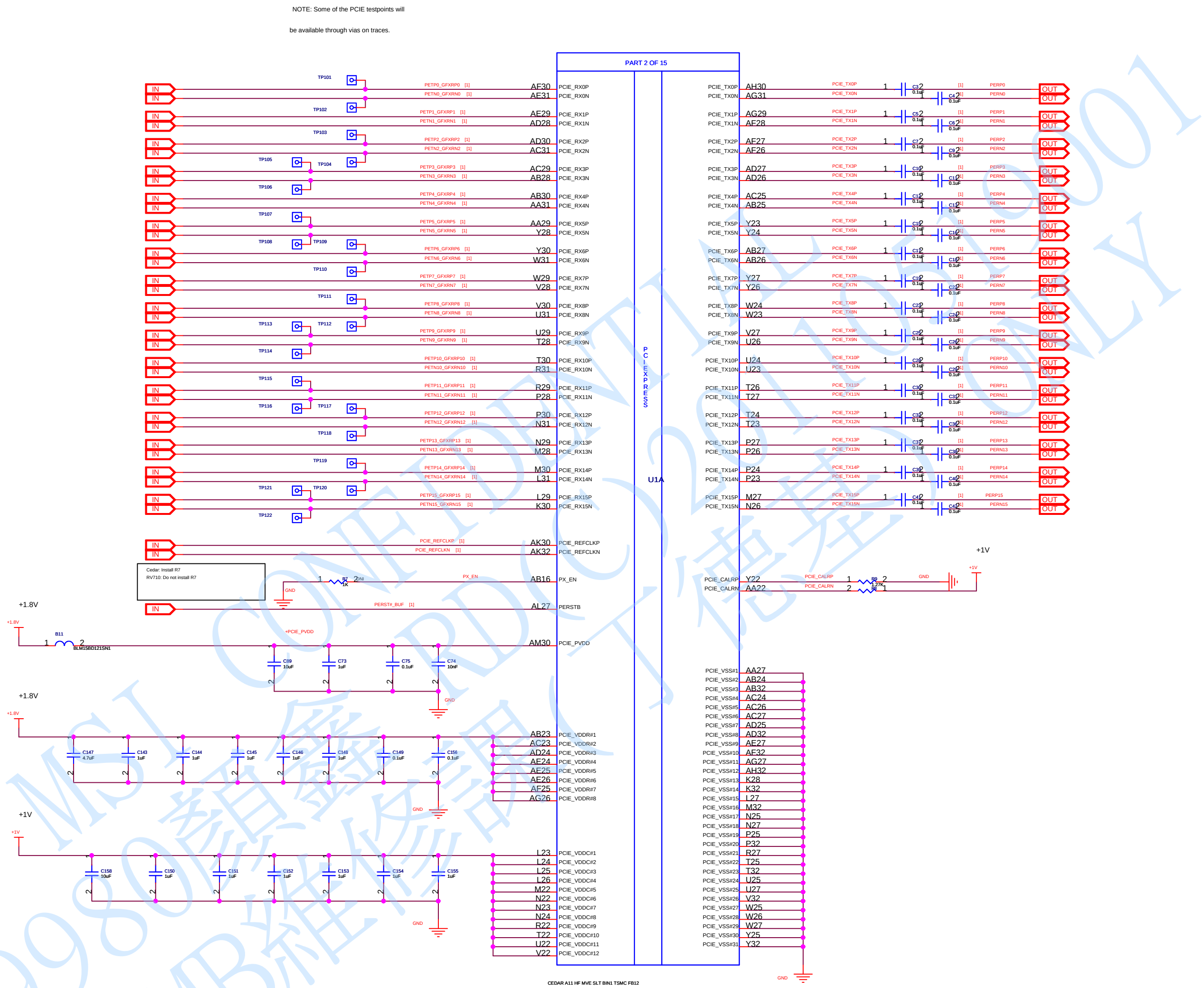
Date: Thursday, October 28, 2010 | Rev P00

Sheet 1 of 18

Title: HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA
PCI-E Edge Connector

Doc No. 105-C264XX-00A

CAICOS/CEDAR PCIe Interface



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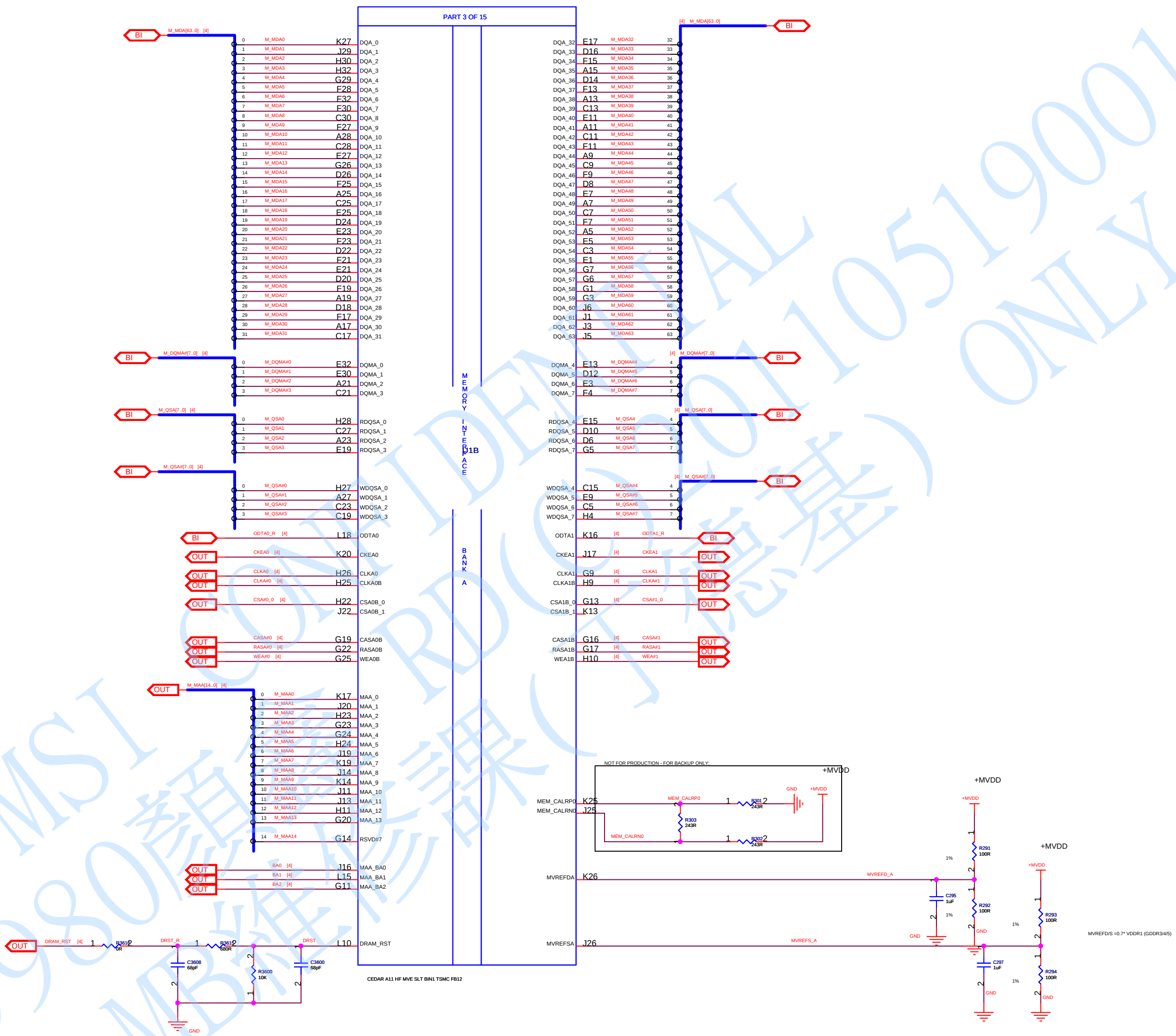
AMD

Date: Thursday, October 28, 2010	Rev P00
Sheet 2 of 18	
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/VGA CAICOS PCIE Interface	Doc No. 105-C264XX-00A



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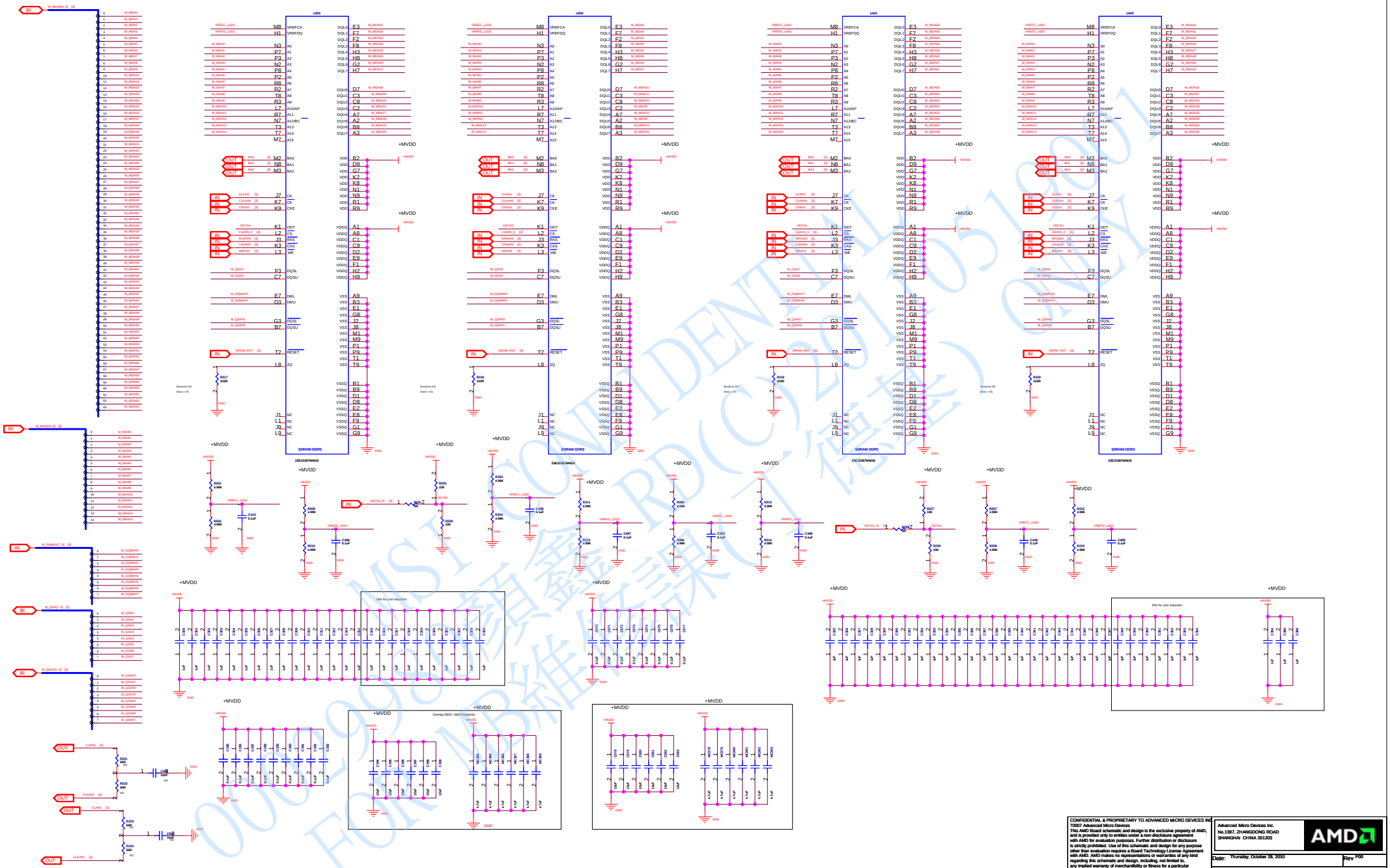
Date: Thursday, October 28, 2010

Rev P00

Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA
CAICOS MEM I/F CHA

Doc No. 105-C264XX-00A

CHANNEL A: 256MB/512MB DDR3



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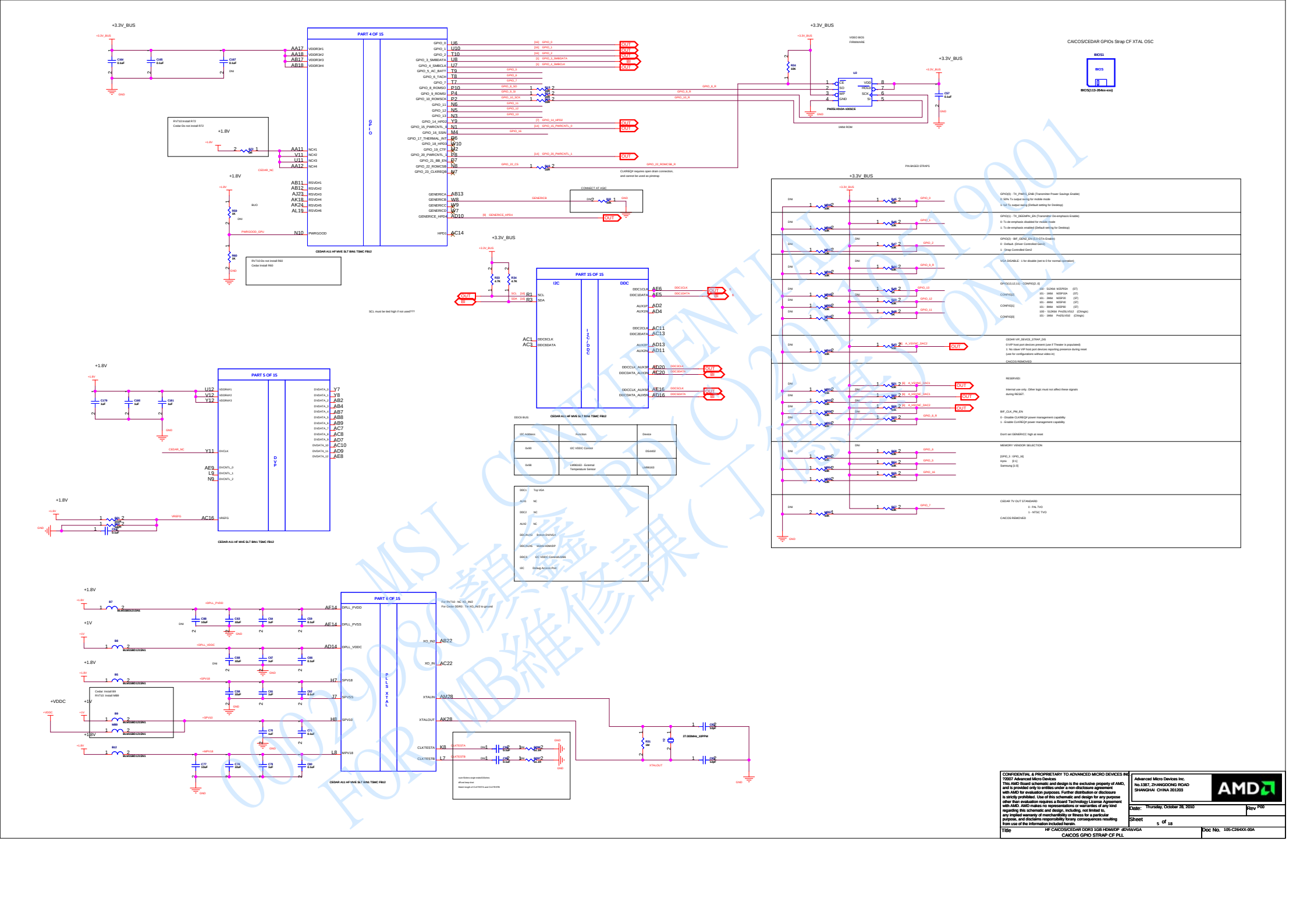
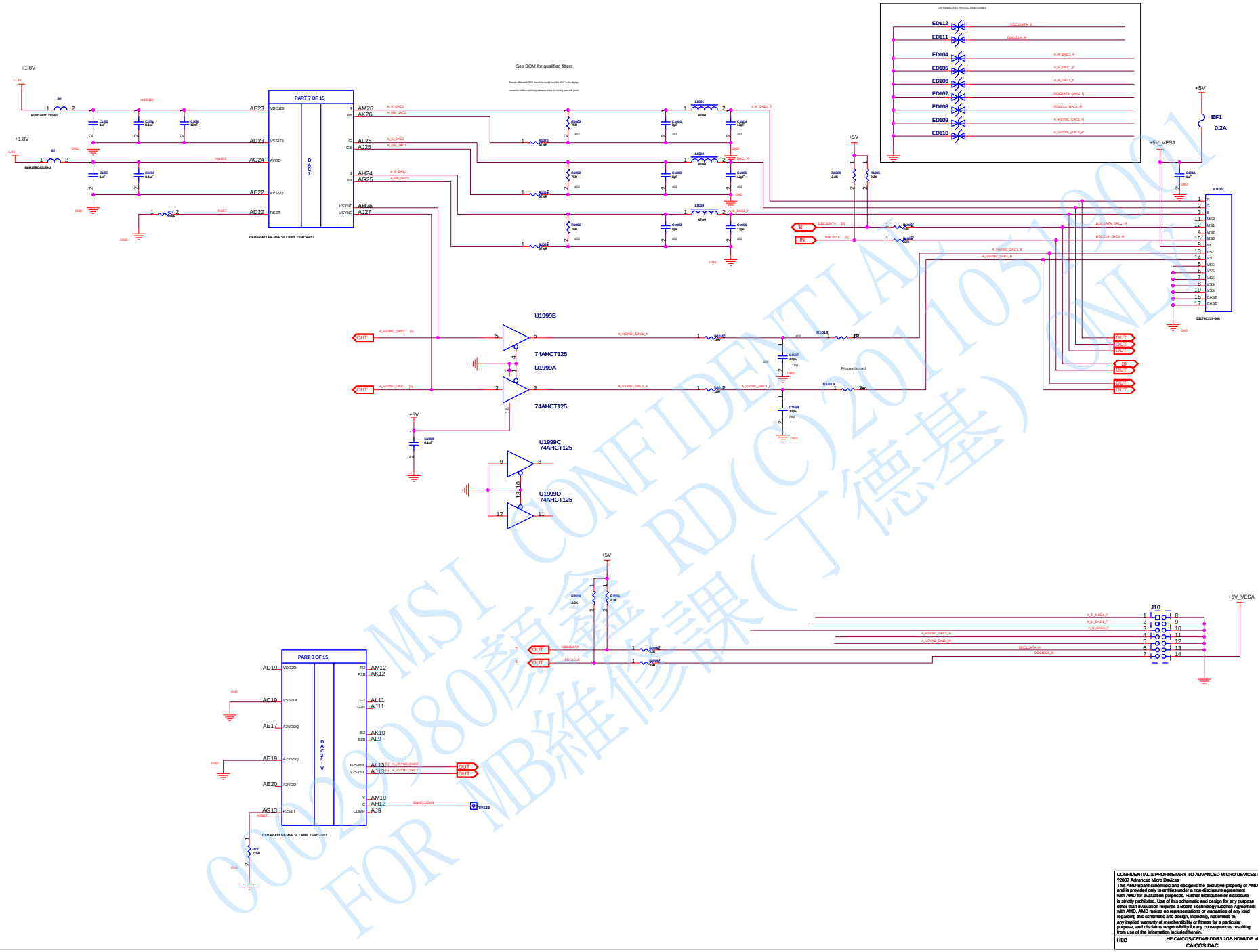
SHANGHAI CHINA 201203

Date:	Thursday, October 28, 2010
Rev	P00
Sheet	4 of 18
Title	HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/VGA DDR3 CHA
Doc No.	105-C26400-00A


PART 4 OF 15
PART 15 OF 15
PART 5 OF 15
PART 6 OF 15
CAICOS/CEDAR GPIOs Strap CF XTAL OSC
CAICOS GPIO STRAP CF PLL
Advanced Micro Devices Inc.
No.1387, ZHANGDONG ROAD
SHANGHAI CHINA 201203
Date: Thursday, October 28, 2010
Rev P00
Sheet 5 of 18
Doc No. 105-C26400-00A



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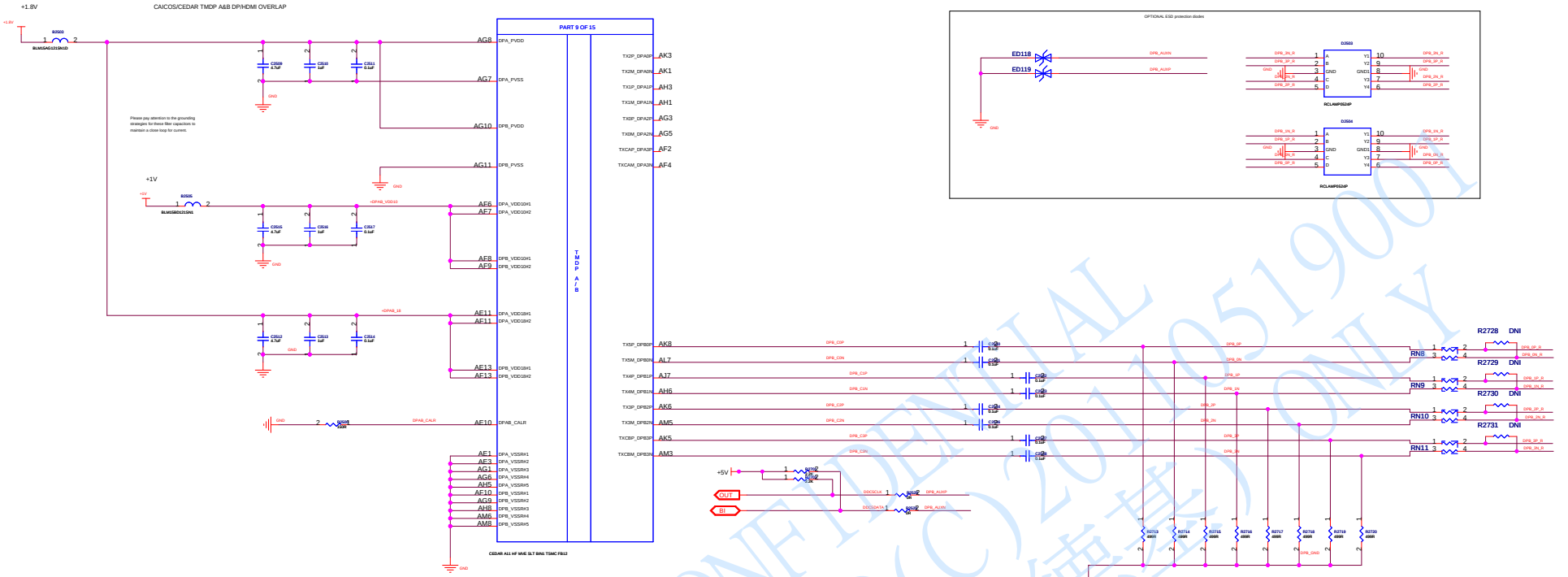
SHANGHAI CHINA 201203

Date:	Thursday, October 28, 2010
Rev	P00
Sheet	6 of 18
Title	HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA CAICOS DAC
Doc No.	105-C26400-00A



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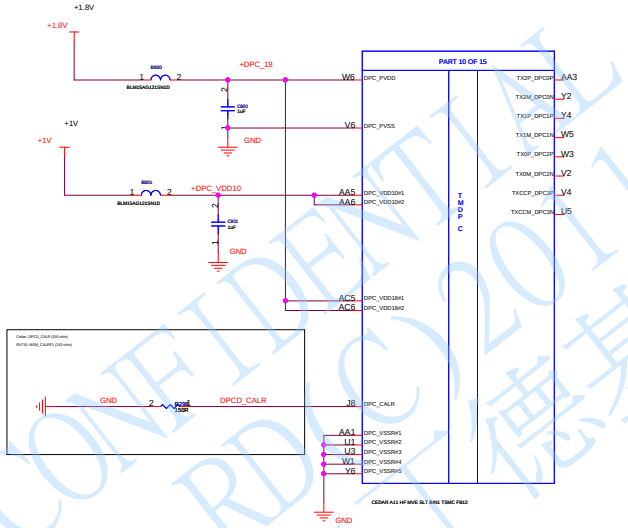
SHANGHAI CHINA 201203

Date:	Thursday, October 28, 2010
Rev	P00
Sheet	7 of 18
Title	HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA CAICOS TMDP A&B HDMI/DP
Doc No.	105-C26400-00A

CAICOS/CEDAR Display Port C (Unused)



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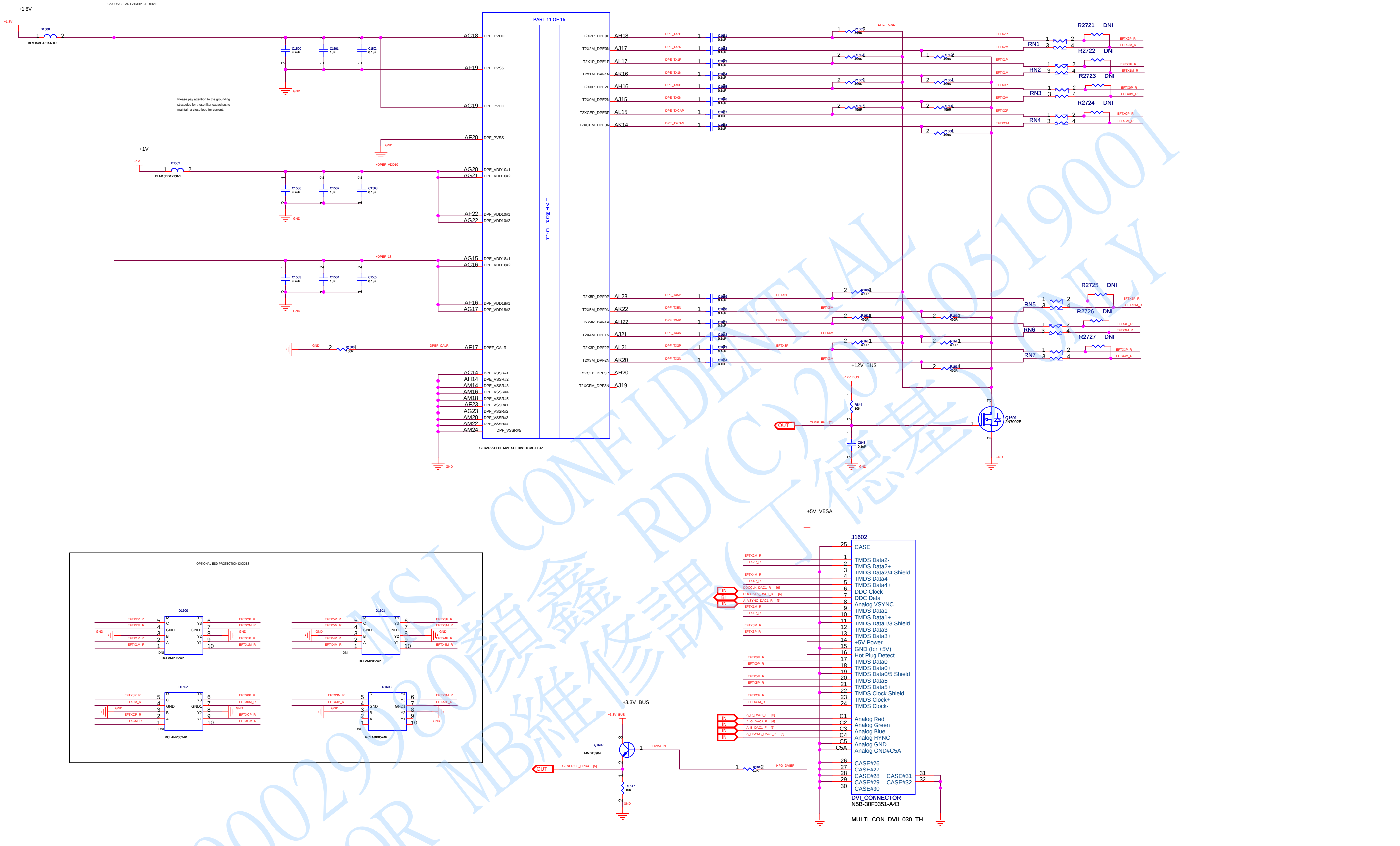
SHANGHAI CHINA 201203

Date: Thursday, October 28, 2010	Rev P00
Sheet 8 of 18	
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA CAICOS TMDP C (UNUSED)	Doc No. 105-C26400-00A



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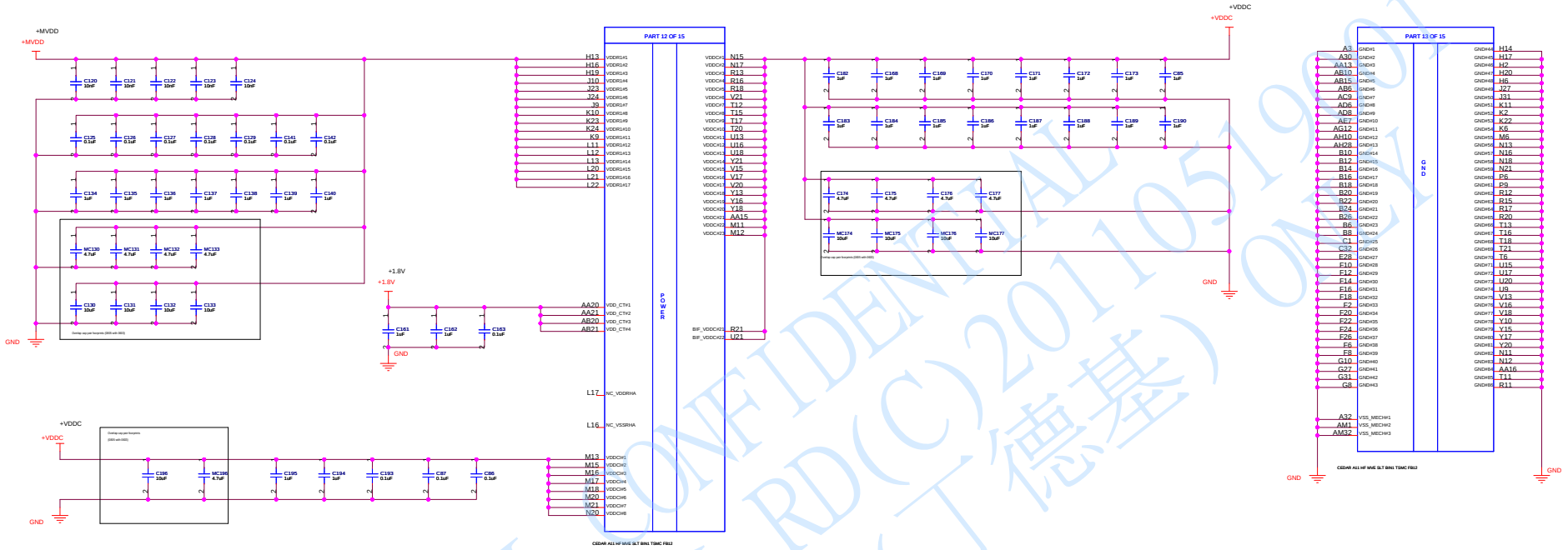
SHANGHAI CHINA 201203

AMD

Date: Thursday, October 28, 2010	Rev P00
Sheet 9 of 18	
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/bVGA CAICOS LVTMDP E&F dDVI-I	Doc No. 105-C264XX-00A

CAICOS/CEDAR Power & GND



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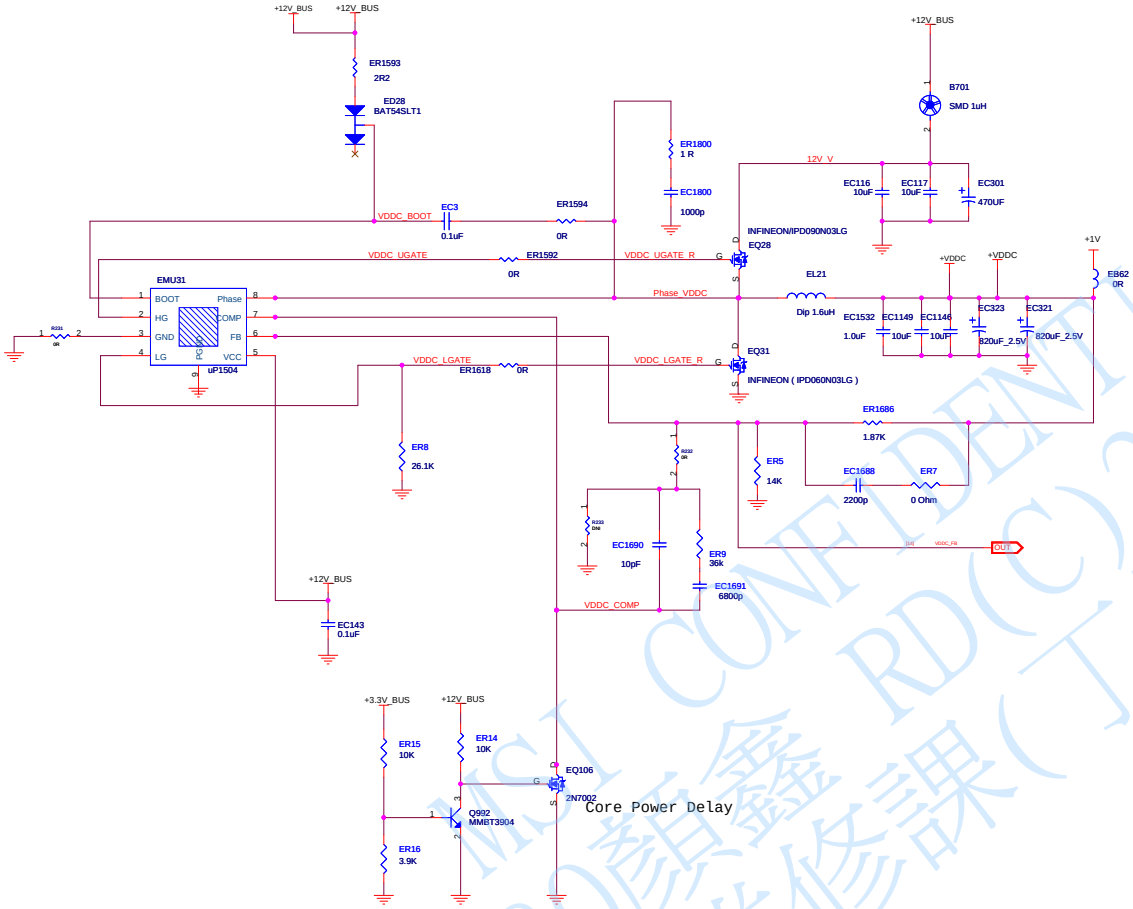
SHANGHAI CHINA 201203

Date: Thursday, October 28, 2010	Rev P00
Sheet 10 of 18	
Title: HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA CAICOS POWER&GND	Doc No. 105-C26400-00A



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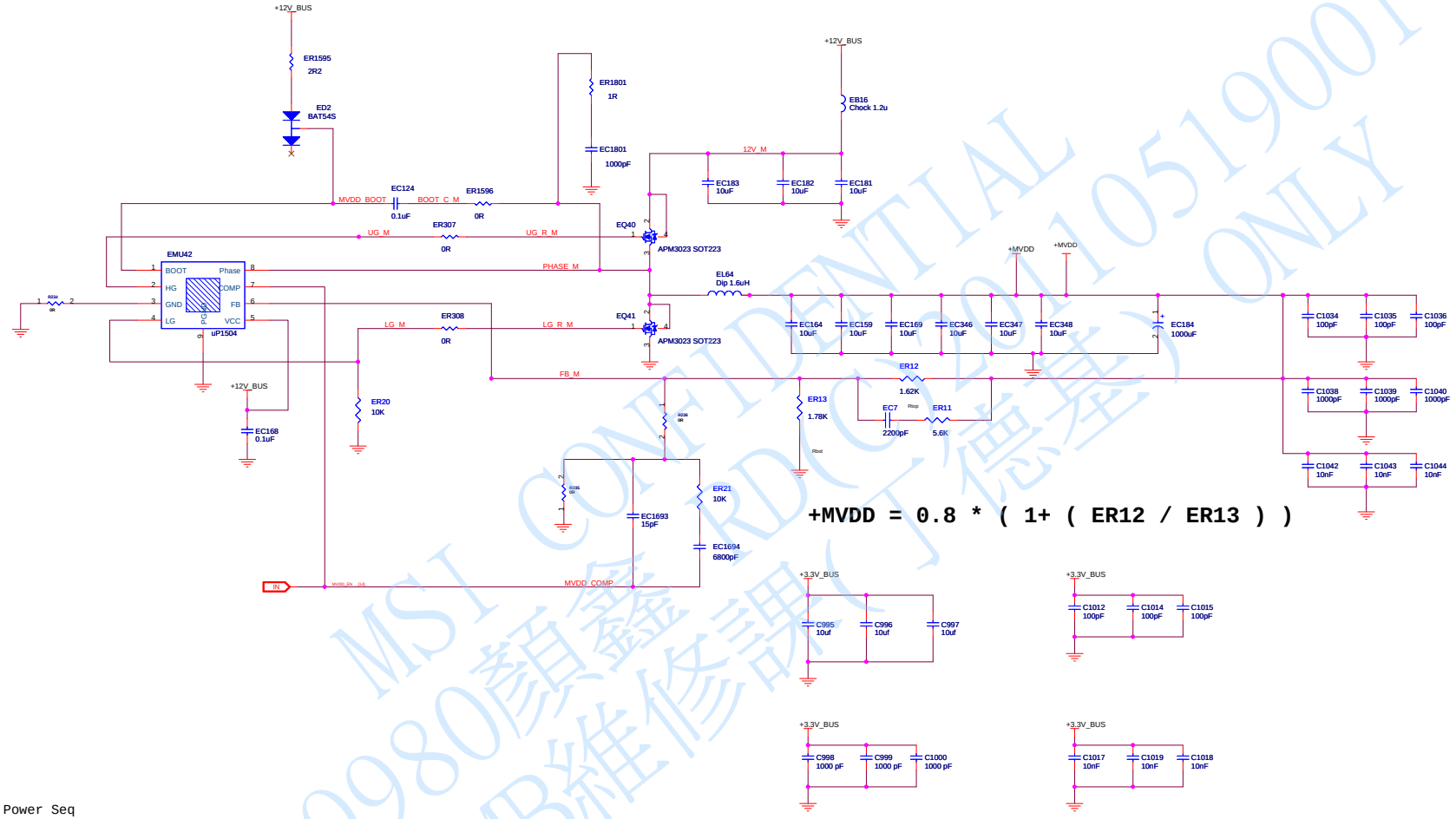
No.1387, ZHANGDONG ROAD
SHANGHAI CHINA 201203

Date: Thursday, October 28, 2010	Rev P00
Sheet 11 of 18	
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA VDDC	Doc No. 105-C26400-00A



Memory Power Seq

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SHANGHAI CHINA 201203

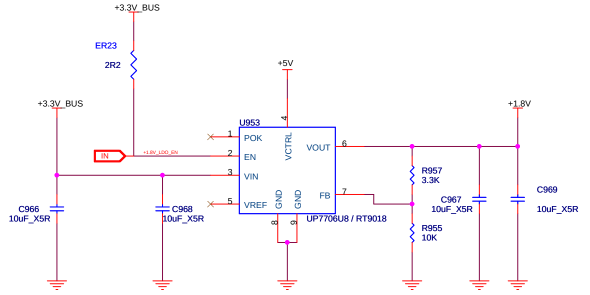
AMD

Date: Thursday, October 28, 2010
Rev P00
Sheet 12 of 18
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA MVDD
Doc No. 105-C26400-00A

Linear Regulators

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX

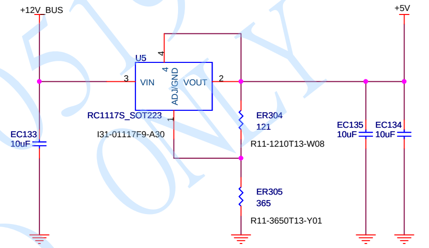
PCB: 50 to 70mm sq. copper area for cooling



Vout=0.8V * (1+ R957 / R955)

1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

Regulators for +5V, +5V_VESA and +5V_VESA2

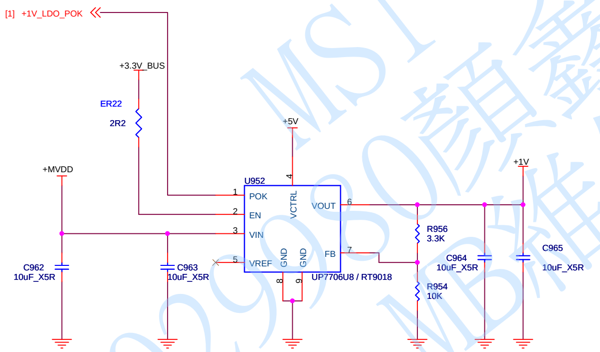


Vout=1.25V* [1+(ER305/ER304)]

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA



Vout=0.8V * (1+ R956 / R954)

Advanced Micro Devices Inc.
No.1387, ZHANGDONG ROAD
SHANGHAI CHINA 201203

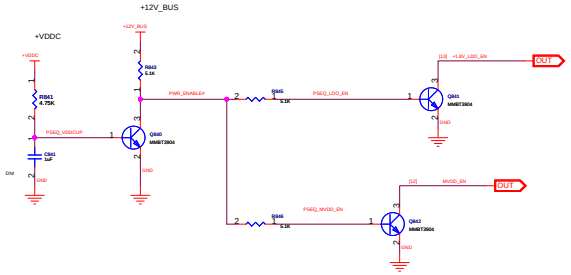
Date: Thursday, October 28, 2010 Rev P00

Sheet 13 of 18

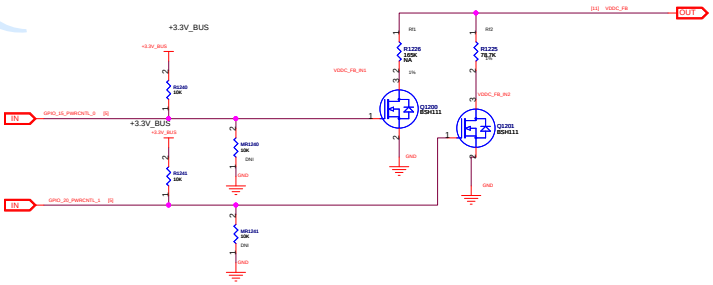
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA
LINEAR REGULATORS

Doc No. 105-C264XX-00A

POWER SEQUENCING CIRCUIT



VDDC Low Side Divider



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No.1387, ZHANGDONG ROAD
SHANGHAI CHINA 201203

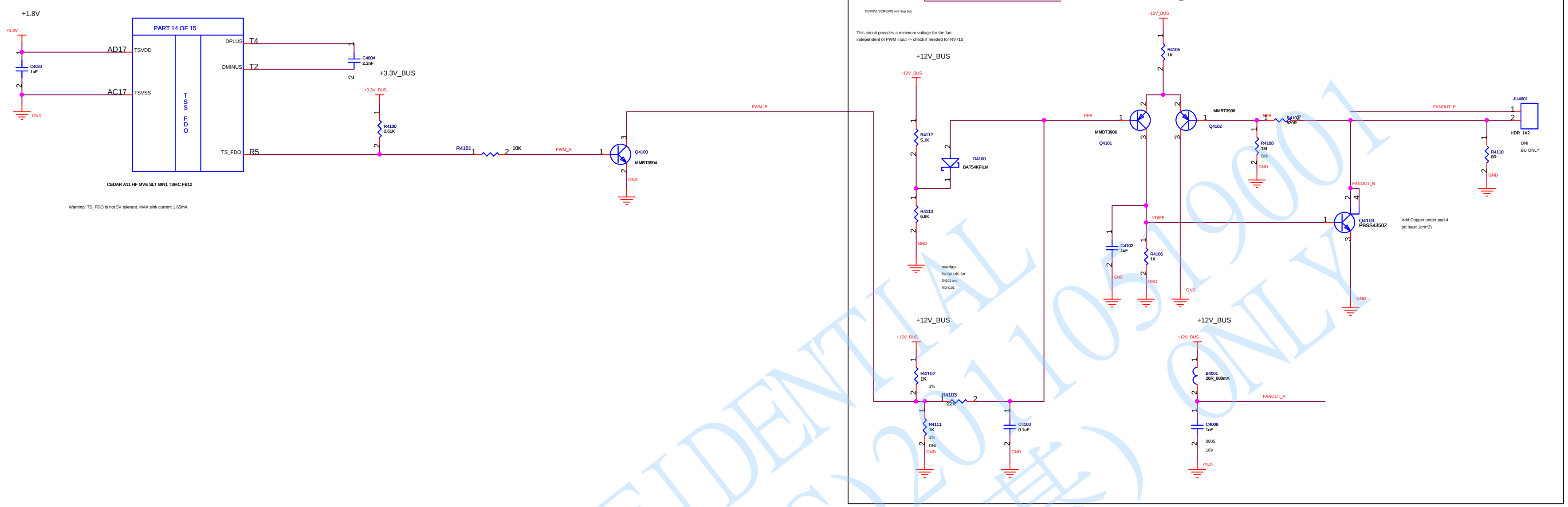
Date: Thursday, October 28, 2010 Rev P00

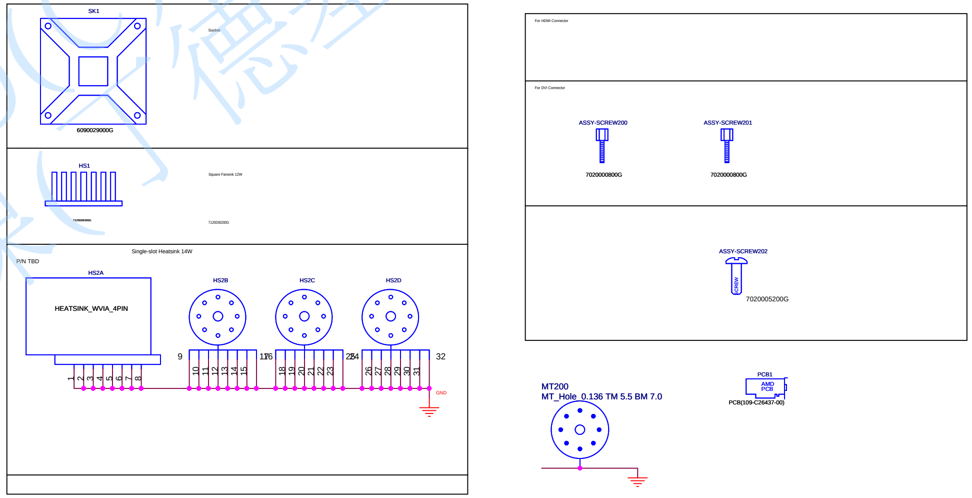
Sheet 14 of 18

Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA PWR& MGMT &SEQ

Doc No. 105-C26400-00A

Mechanical and Thermal Management





TOP
Single end
Address branch
50 ohm +/- 5 ohm
3.82 mils

Bottom
Single end
Memory data
45 ohm +/- 5 ohm
4.724 mils

TOP
Different
TMDS
85 ohm +/- 10 %
4.33 mils / 5.511 mils

Bottom
Different
PEX_PCIE
85 ohm +/- 10 %
4.921 mils / 6.889 mils

SKU	P/N	CONFIGURATION	Form Factor
JUNBONATOR	80200528A0G	dDVI-I + HDMI	FH / SS
JUNBONATOR-COMMERCIAL	8020052800G	dDVI-I + DP	FH / SS
JUNBONATOR-COMMERCIAL	8020051600G	DVI + DP	LP / SS
JUNBONATOR	80200516A0G	DVI +HDMI	LP / SS
	8020051700G	DVI + DP + VGA	FH / DS
	80200517A0G	DVI +HDMI+ VGA	FH / DS

Rectangular Heatsink 8W

FM1 SW_FB
FM5 SW_FB
FM2 SW_FB
FM6 SW_FB
FM3 SW_FB
FM4 SW_FB

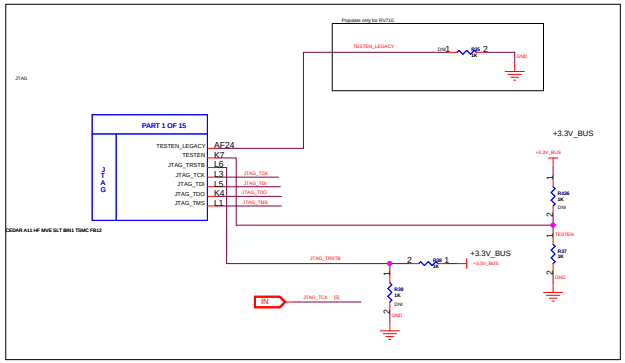
Advanced Micro Devices Inc.
No.1387, ZHANGDONG ROAD
SHANGHAI CHINA 201203

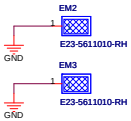
Date: Thursday, October 28, 2010
Rev P00

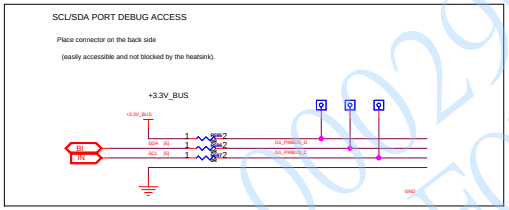
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA
MECH/THERMAL MANAGEMENT

Doc No. 105-C264XX-00A

(19) Debug Circuits







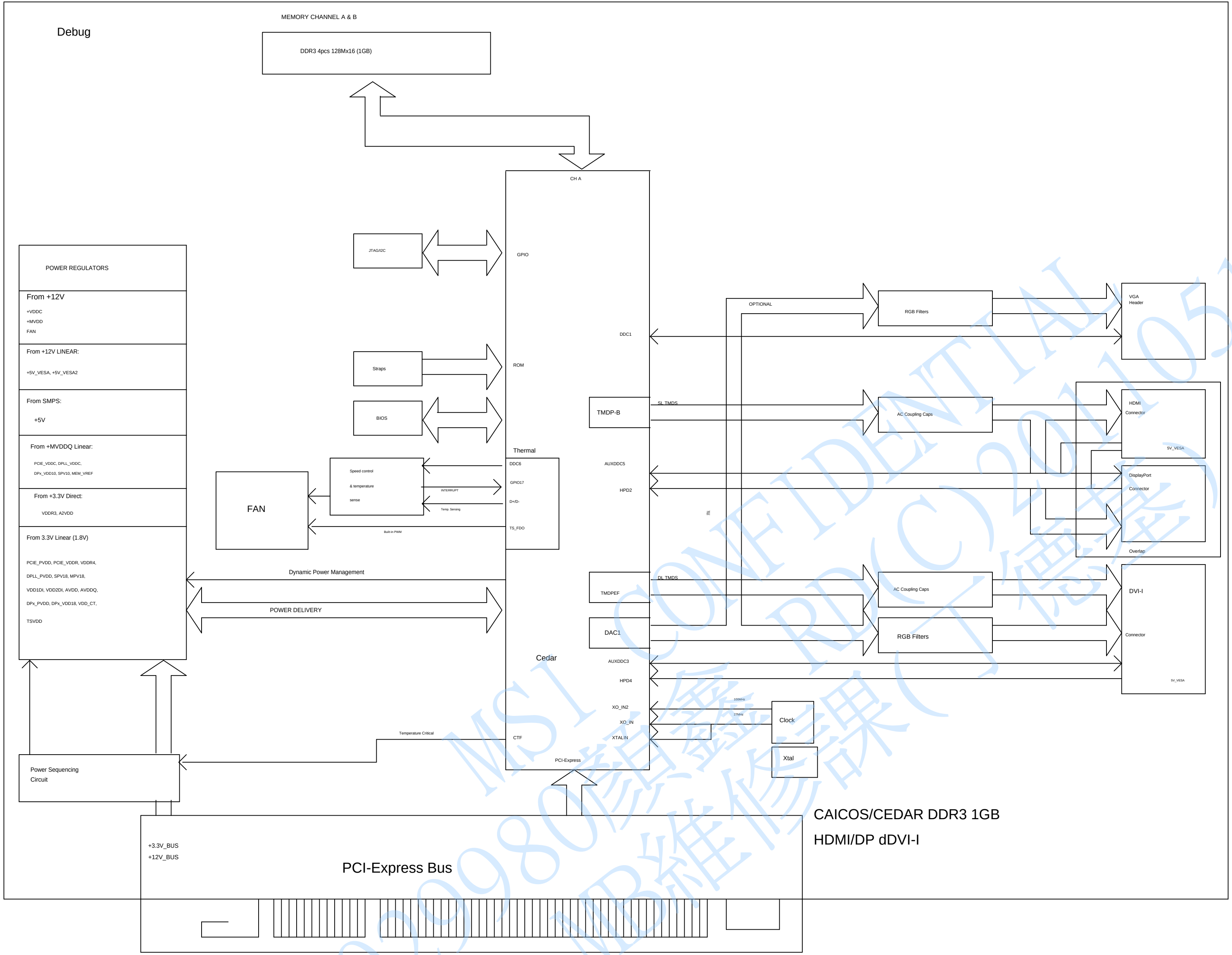
Advanced Micro Devices Inc.
No.1387, ZHANGDONG ROAD
SHANGHAI CHINA 201203

Date: Thursday, October 28, 2010 | Rev P00

Sheet 16 of 18

Title: HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA DEBUG CIRCUIT

Doc No. 105-C26400-00A


Debug
MEMORY CHANNEL A & B
DDR3 4pcs 128Mx16 (1GB)
CH A
POWER REGULATORS
From +12V
+VDDC
+MVDD
FAN
From +12V LINEAR:
+5V_VESA, +5V_VESA2
From SMPS:
+5V
From +MVDDQ Linear:
PCIE_VDDC, DPLL_VDDC,
DPx_VDD10, SPV10, MEM_VREF
From +3.3V Direct:
VDDR3, A2VDD
From 3.3V Linear (1.8V)
PCIE_PVDD, PCIE_VDDR, VDDR4,
DPLL_PVDD, SPV18, MPV18,
VDD1DI, VDD2DI, AVDD, AVDDQ,
DPx_PVDD, DPx_VDD18, VDD_CT,
TSVDD
JTAG/I2C
GPIO
Straps
ROM
BIOS
Thermal
Speed control
& temperature
sense
DDC6
GPIO17
D+/D-
TS_FDO
INTERRUPT
Temp. Sensing
Built-in PWM
FAN
Dynamic Power Management
POWER DELIVERY
OPTIONAL
RGB Filters
VGA
Header
DDC1
TMDP-B
SL TMDS
AC Coupling Caps
HDMI
Connector
5V_VESA
DisplayPort
Connector
Overlap
AUXDDC5
HPD2
TMDPEF
DL TMDS
AC Coupling Caps
DVI-I
DAC1
RGB Filters
Connector
Cedar
AUXDDC3
HPD4
5V_VESA
XO_IN2
XO_IN
XTALIN
Clock
Xtal
CTF
Temperature Critical
PCI-Express
Power Sequencing
Circuit
+3.3V_BUS
+12V_BUS
PCI-Express Bus

CAICOS/CEDAR DDR3 1GB

HDMI/DP dDVI-I

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SHANGHAI CHINA 201203

Date: Thursday, October 28, 2010 | Rev P00

Sheet 17 of 18

Title: HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA BLOCK DIAGRAM

Doc No. 105-C264XX-00A

AMD	Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA	Schematic No. 105-C264XX-00A	Date: Thursday, October 28, 2010

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev P00

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2010/03/31	Initial Caicos Schematic, based on C026XX-10
			.....