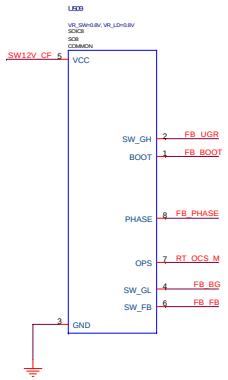
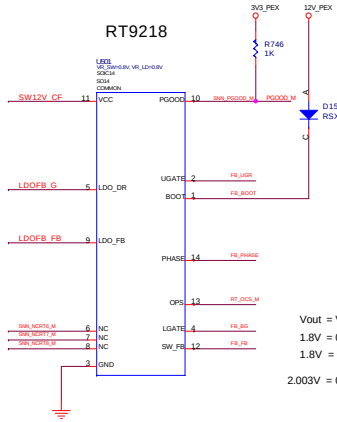
PowerSupplyIII: FBVDDQ, PEX1V2

FBVDDQ & PEX1V2

APW7120 / RT9214



RT9218



FBVDDQ:-RT9218

Vout = VRef * (1+Rtop/Rbot)

1.8V = 0.8V * (1+(5k/4k)) (RT9218)

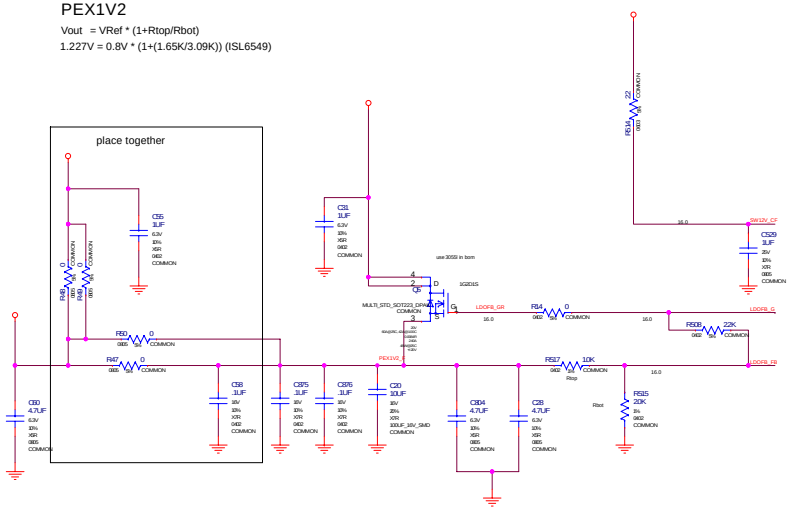
1.8V = 0.8V * (1+(200/160)) (RT9218) Samsung MEM

2.003V = 0.8V * (1+(200/133)) (RT9218) Infineon MEM default

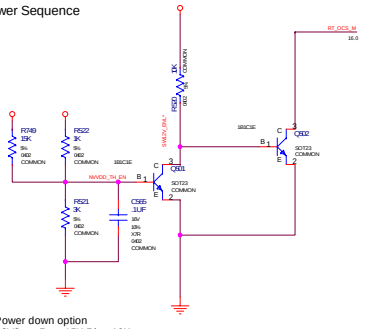
PEX1V2

Vout = VRef * (1+Rtop/Rbot)

1.227V = 0.8V * (1+(1.65K/3.09K)) (ISL6549)



Power Sequence



Power down option

A3V3 Rtop 15K Rbot 10K

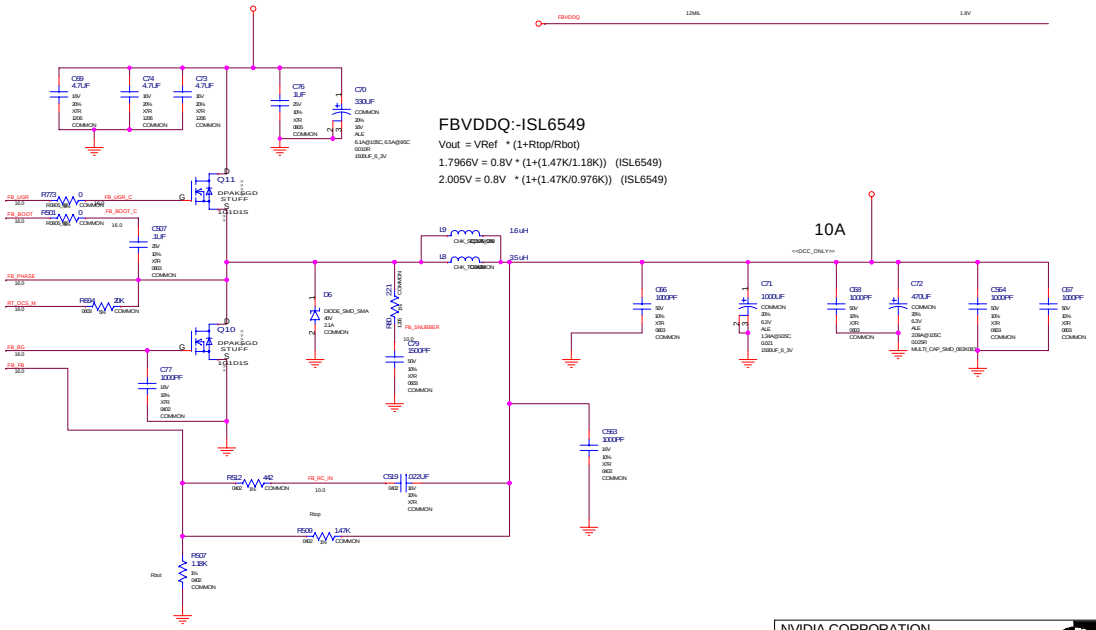
NVVDD Rtop 1K Rbot 3K

FBVDDQ:-ISL6549

Vout = VRef * (1+Rtop/Rbot)

1.7966V = 0.8V * (1+(1.47K/1.18K)) (ISL6549)

2.005V = 0.8V * (1+(1.47K/0.976K)) (ISL6549)



Net Name	LINE_WIDTH	CURRENT	Voltage
FBVDDQ	12MIL		1.8V

ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: PowerSupplyIII: FBVDDQ, PLLVDD

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2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

PowerSupplyII: NVVDD

Net Name	LINE_WIDTH	Current	Voltage
NVVDD	30MIL	15A	1.2V
PEXTV2	24MIL	1.5A	1.2/3.3V
NVVDD_SENSE	16MIL	0.5A	1.2V
NVVDD_SENSE_M	16MIL	0.5A	1.2V

APW7065

25A

Power Sequence

NVVDD

Vout = VRef * (1+Rtop/Rbot)

1.1V = 0.8V * (1+(1.54k/4.02k)) (ISL6549)

1.2V = 0.8V * (1+(1.54k/3.09k)) (ISL6549)

1.2V = 0.8V * (1+(10k/20k)) (APW7065)

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PowerSupply: NVVDD

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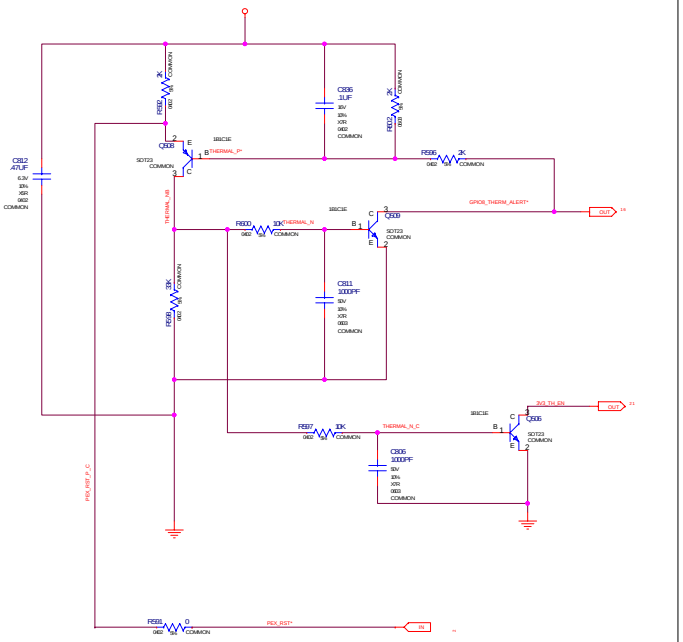
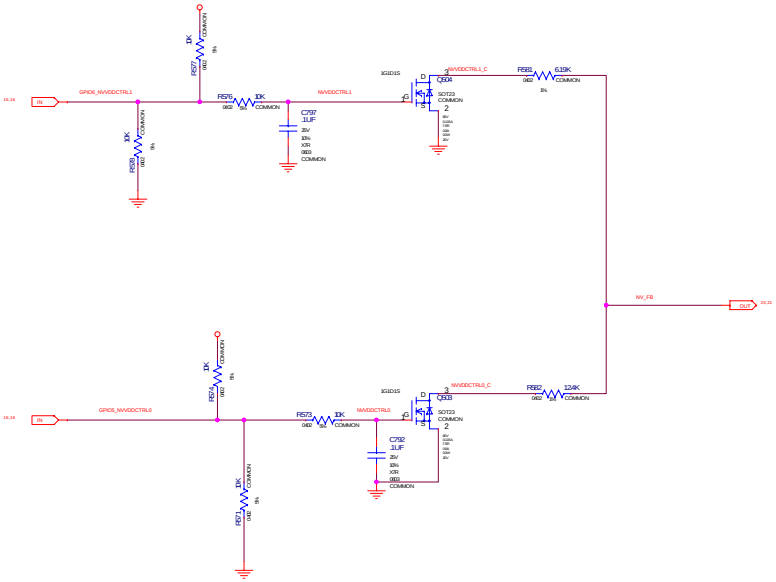
NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

thermal protection and dynamic NVVDD



Thermal protection



dynamic NVVDD

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	thermal protection and dynamic NVVDD

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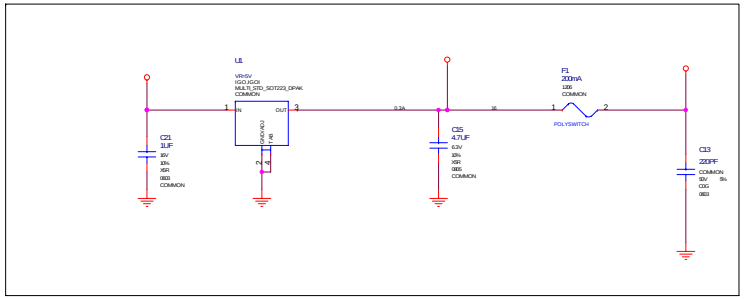
NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

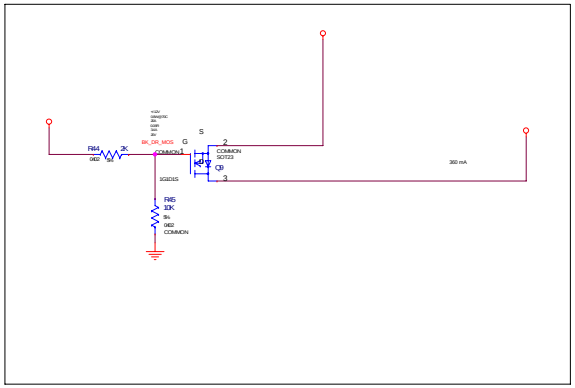
Power SupplyI:TMDS_IOVDD A3V3 DDC_5V IFP_PLLVDD

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	0.1A	12.0	5.00000V
A3V3	1.5A	30.0	3.30000V
IFPAB_IOVDD	0.3A	16	3.30000V
GND		35.0	0.00000V
IFP_PLLVDD	0.3A	16	1.80000V
MIOA_2VS	1A	12MIL	2.0V

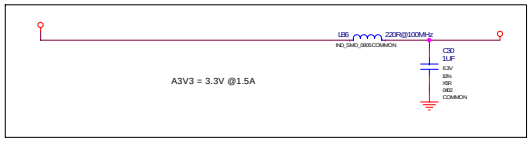
DDC 5V



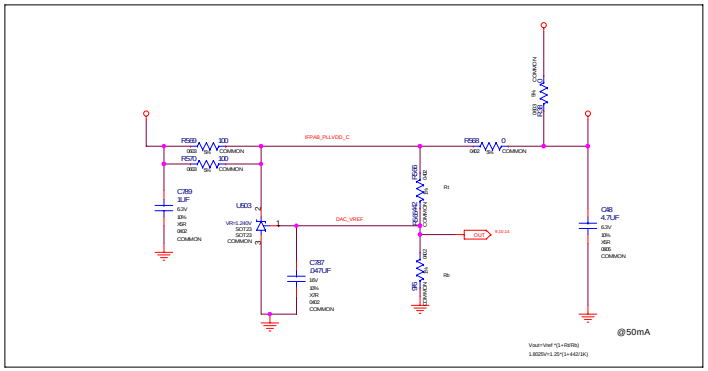
TMDS IO SUPPLY WITH BACKDRIVE PROTECTION



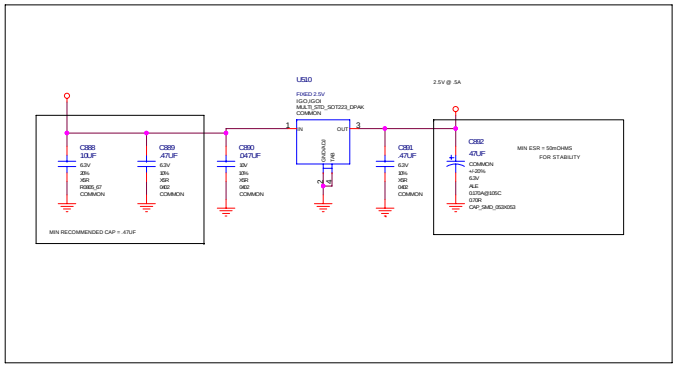
A3V3 Power Supply



IFP_PLL SUPPLY



MIOA_VDDQ



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: TMDS IOVDD,5V,A3V3

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
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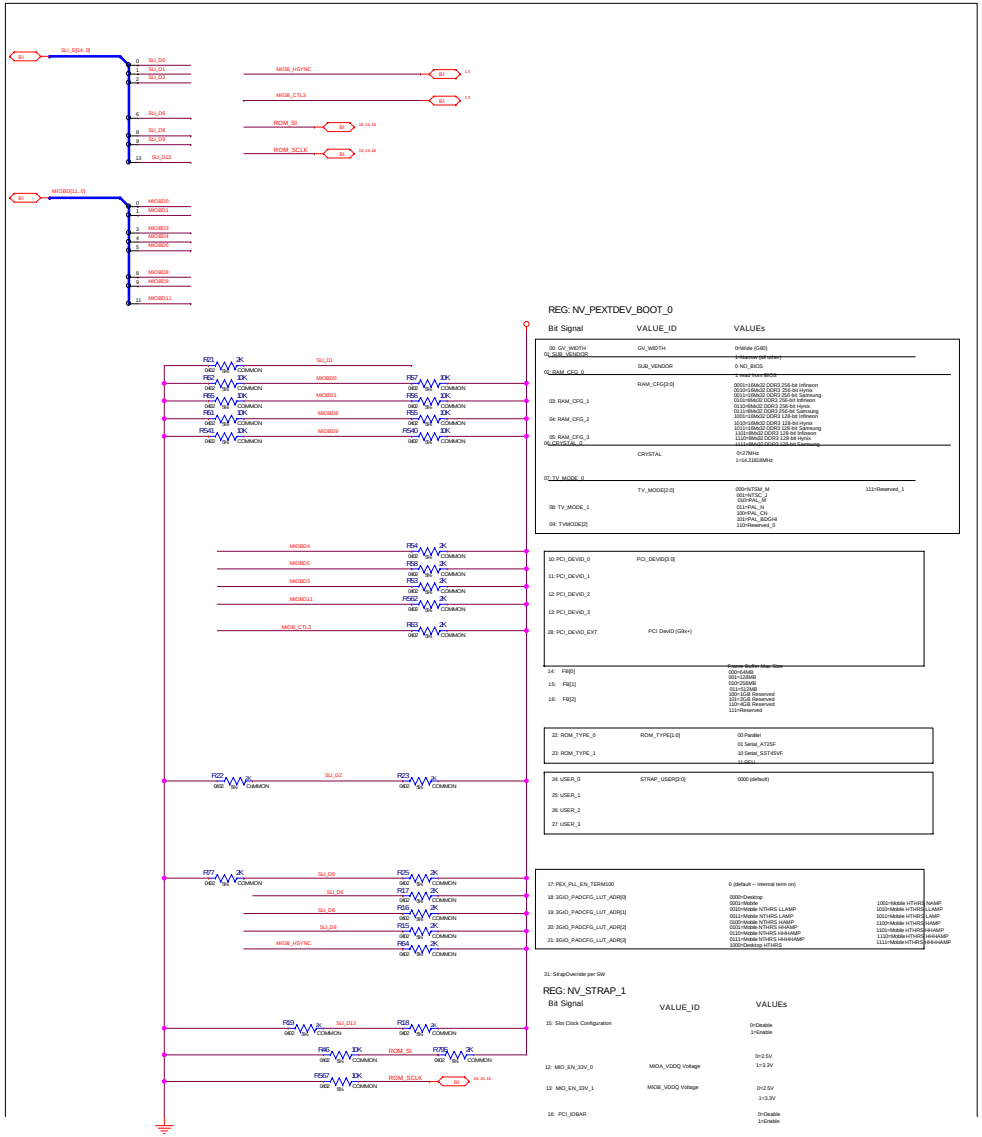
NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

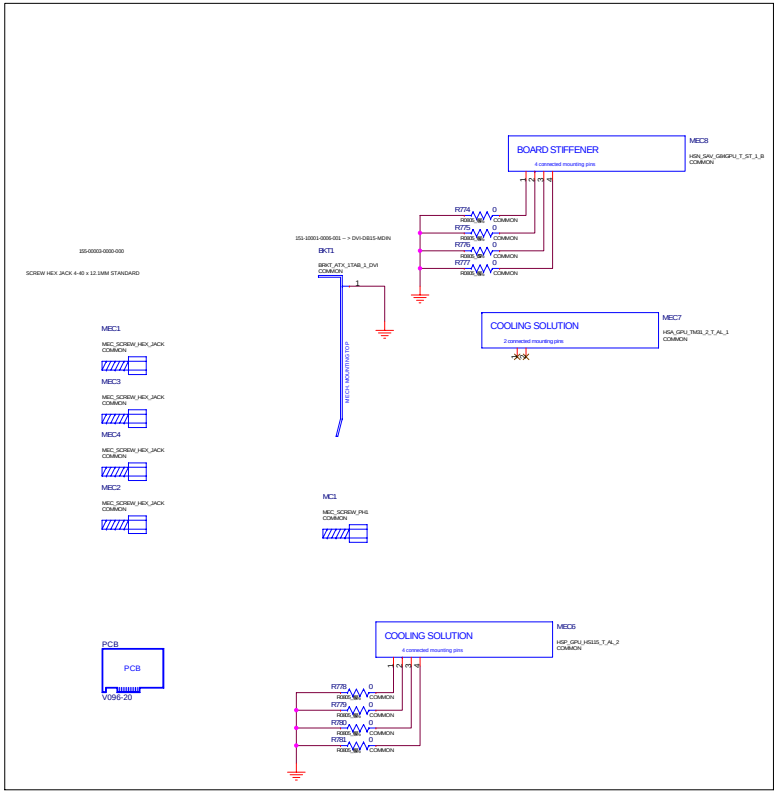
BIOS, Straps, Misc

Straps

Assembly: BIOS



Mechanical parts



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS STRAPS & MECHANICALS

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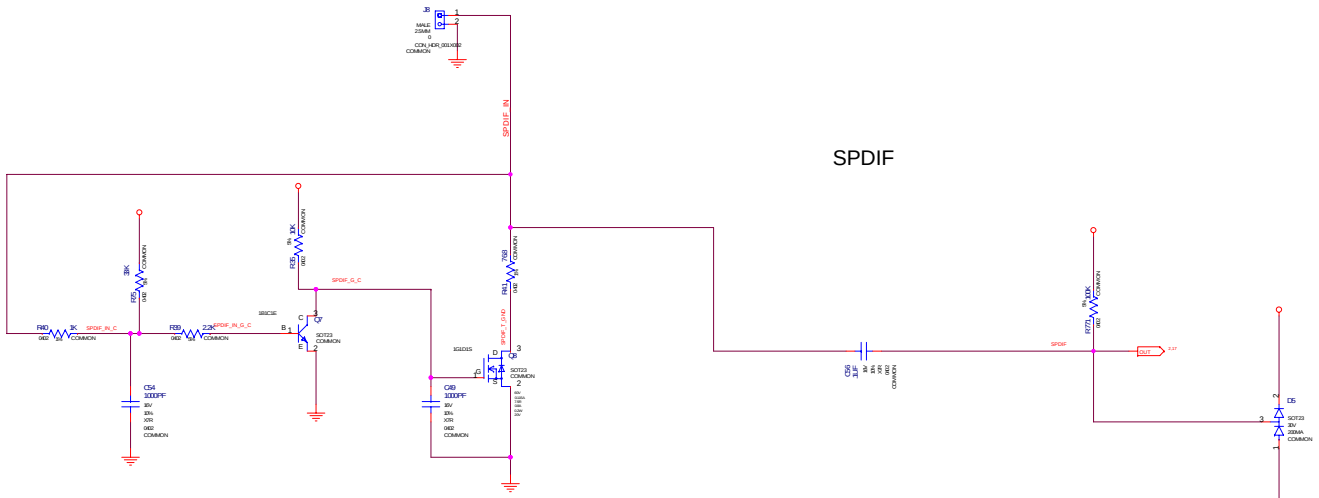
NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

SPDIF



SPDIF

place close to GPU

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF

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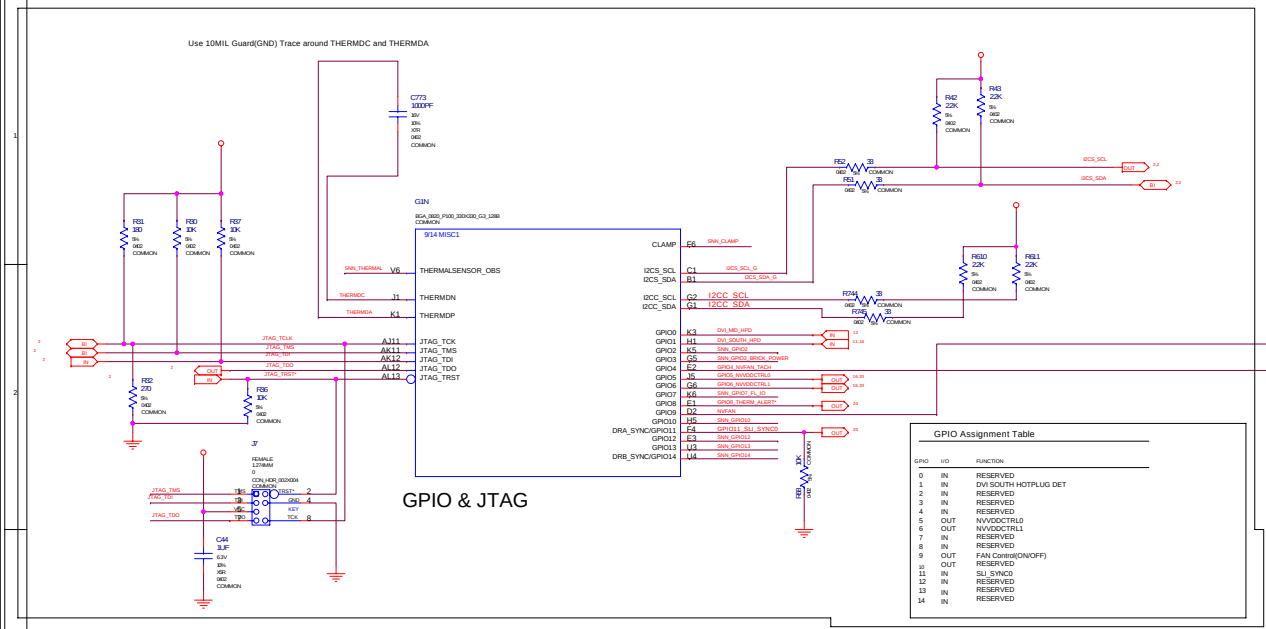
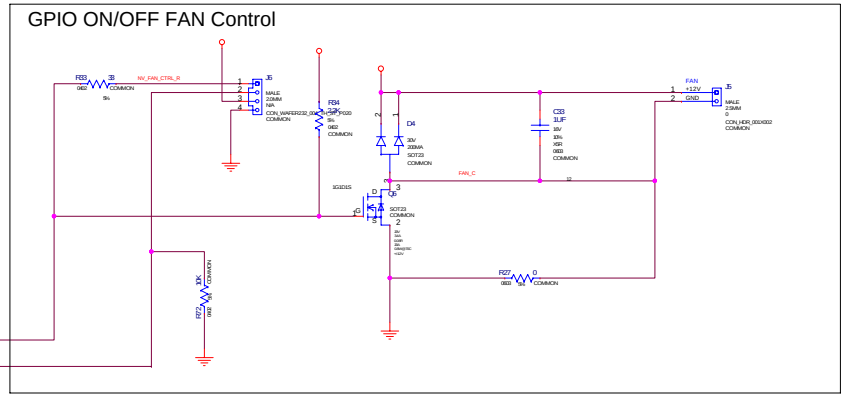
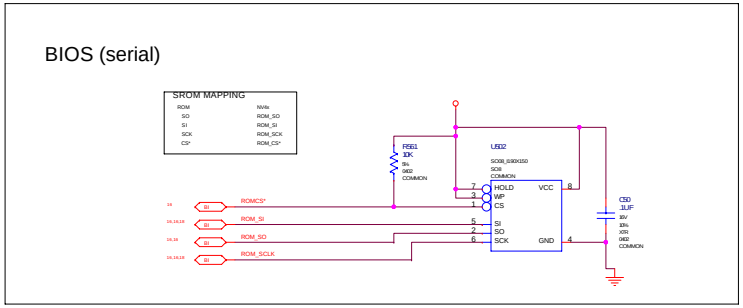
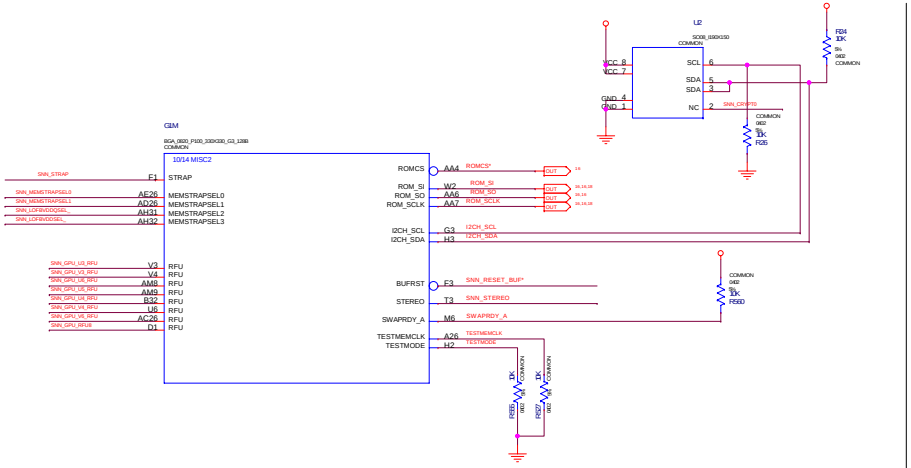
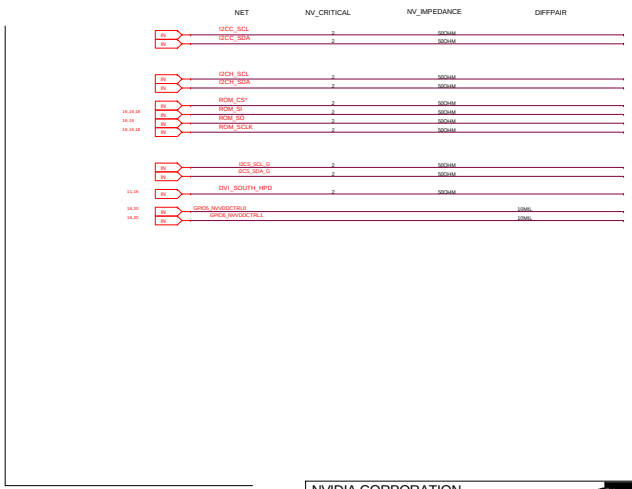
NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007











ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	JTAG, BIOS ROM, HDCP ROM, FAN CONTROL, GPIO

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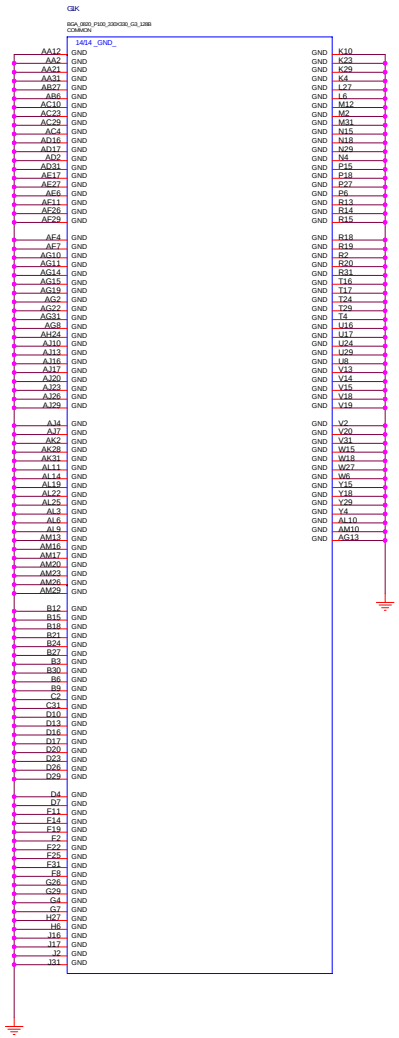
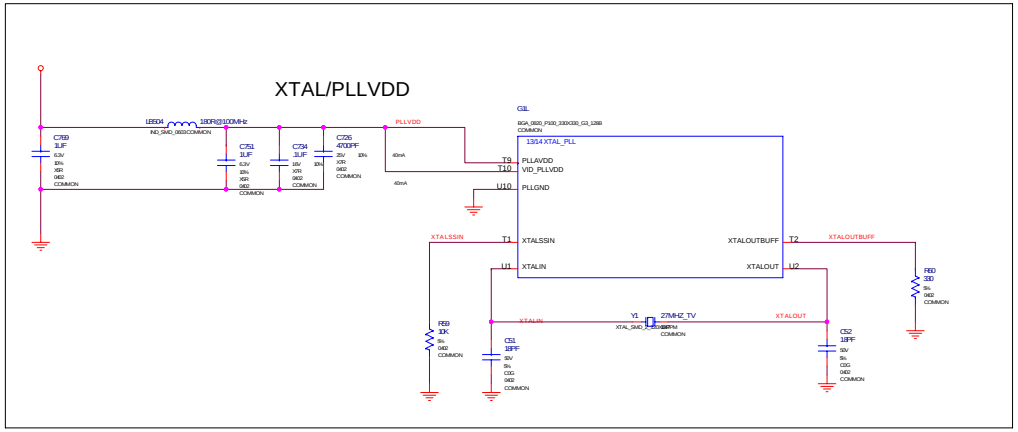
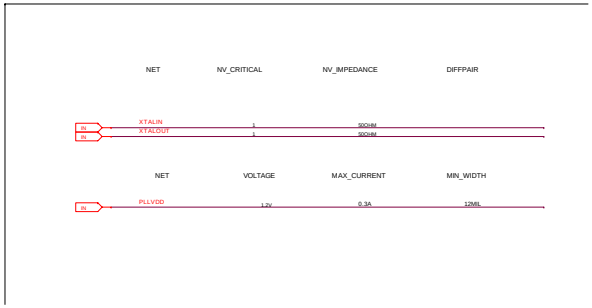
NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

GPU GND CONNECTION, XTAL





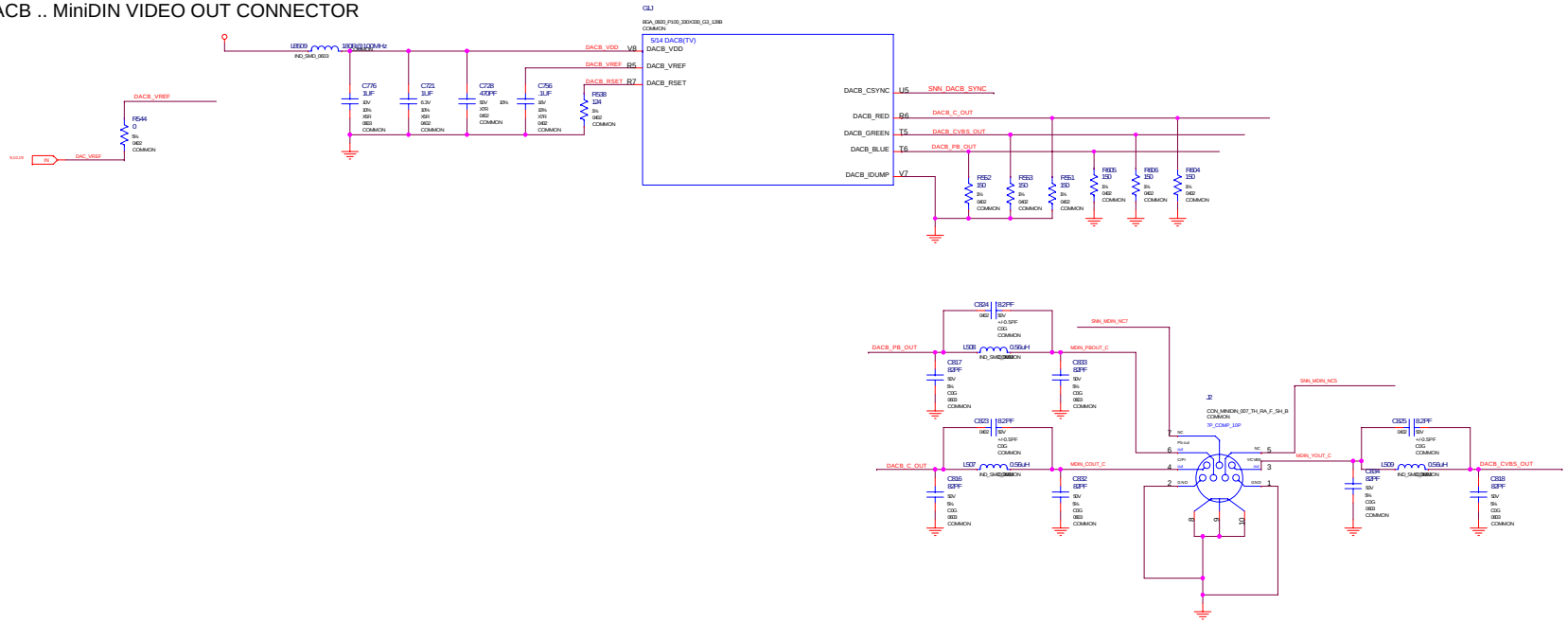


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	GPU GND CONNECTION, XTAL

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

DACB .. MiniDIN VIDEO OUT CONNECTOR



DACB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
TV_CHRO_F	1	90OHM	
MDIN_COUT_C	1	90OHM	
TV_LUMA_F	1	90OHM	
MDIN_YOUT_C	1	90OHM	
TV_CVBS_F	1	90OHM	
MDIN_PBOUT_C	1	90OHM	
MDIN_SCL_C	2	90OHM	
MDIN_SDA_C	2	90OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACB_VDD	3.30000V	0.07A	16.0
DACB_VREF			16.0
DACB_RSET			16.0

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, SYNC STRIPPER, MINIDIN CONNECTOR NORTH,HDTV HEADER

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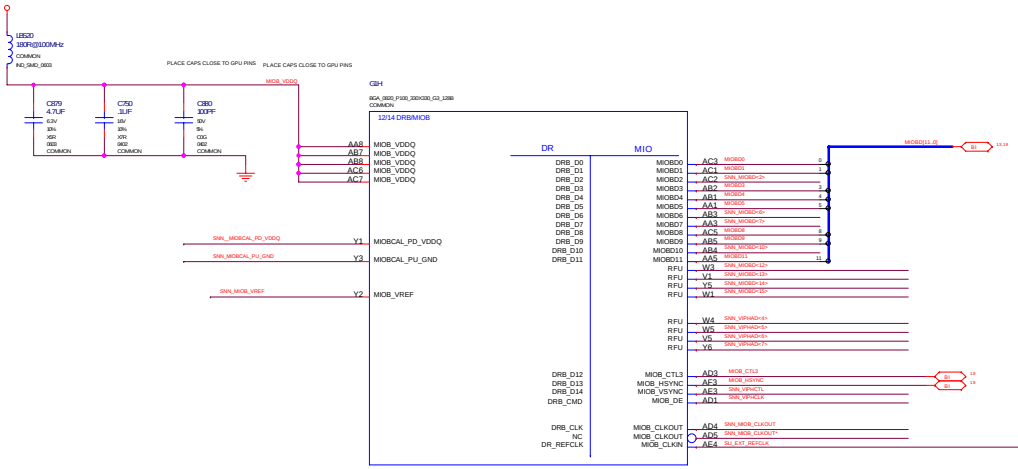
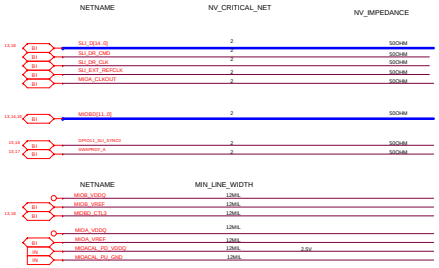
NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

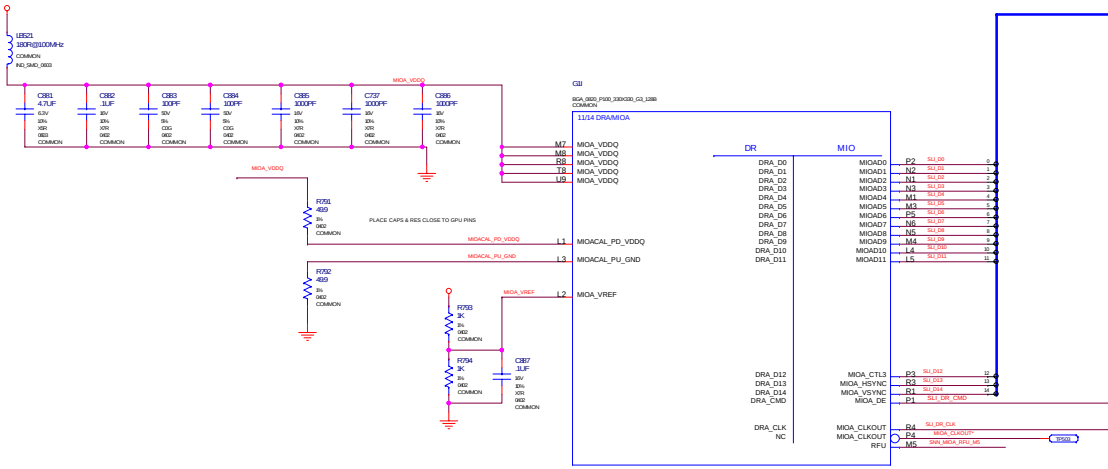
G3 VIP/MIOB



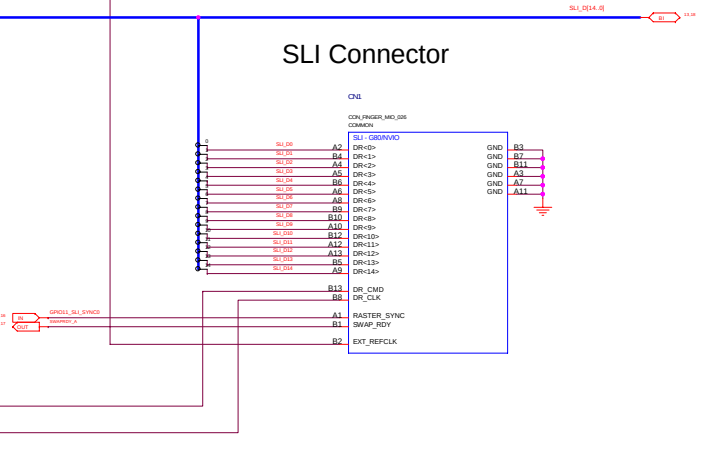
MIO NET RULES



G3 MIOA



SLI Connector



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB

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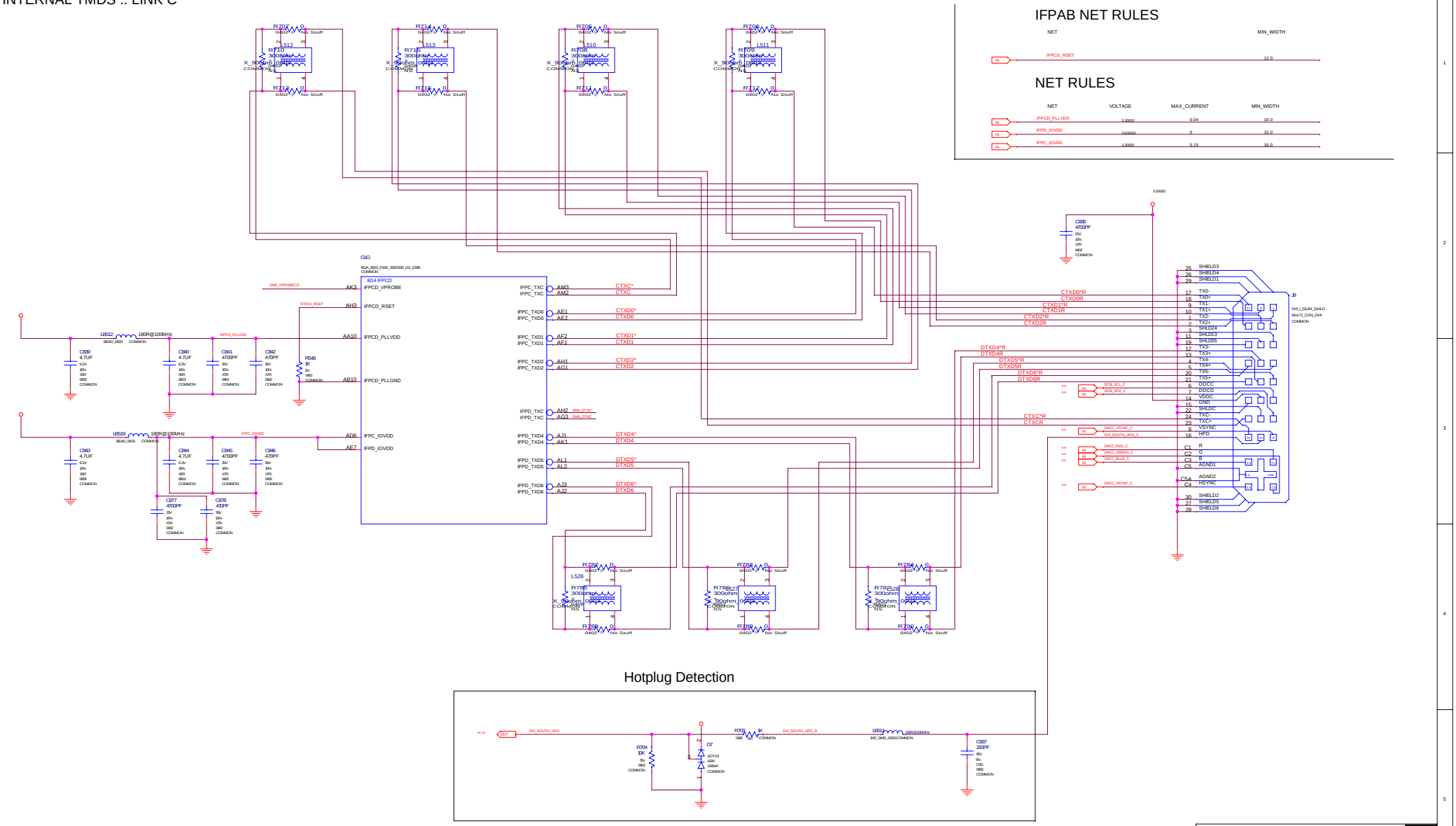
NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

INTERNAL TMDS .. LINK C



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK C

NVIDIA CORPORATION
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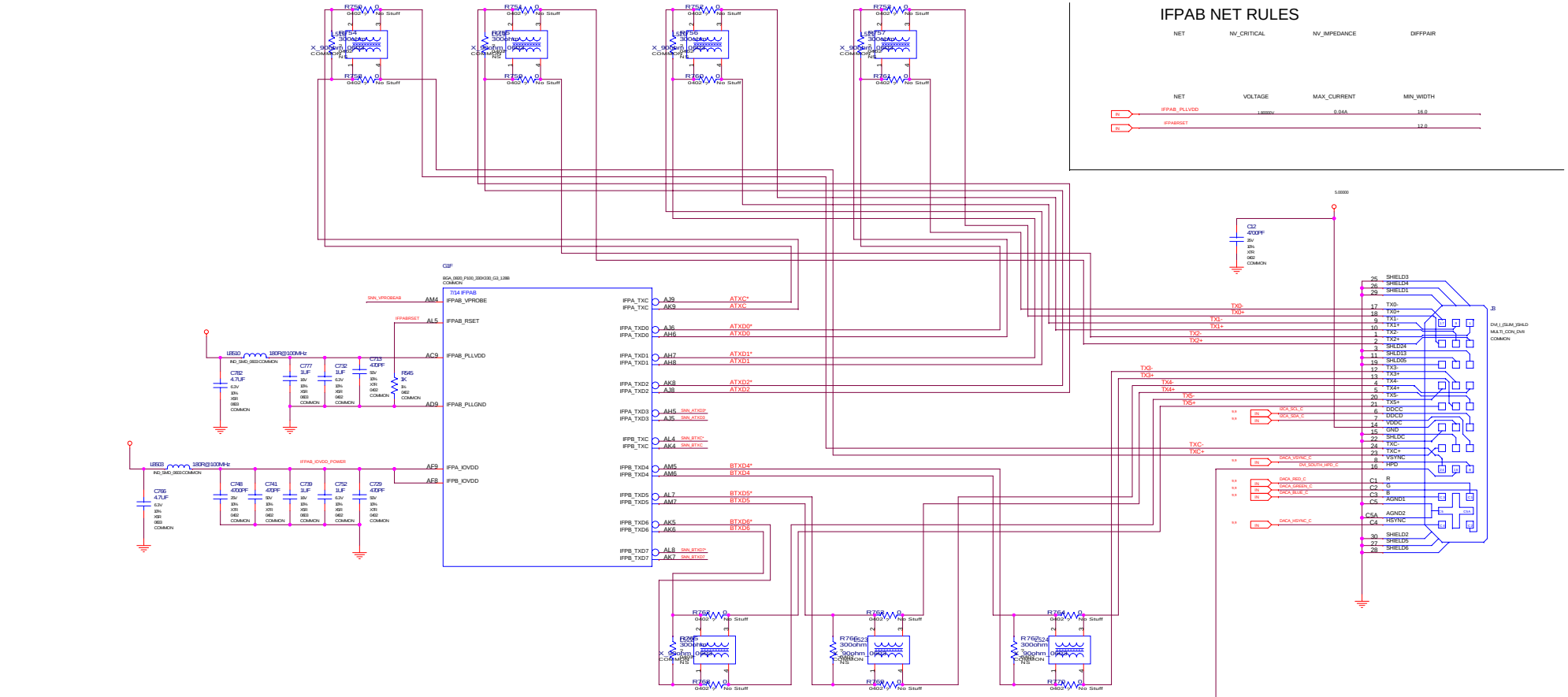
SANTA CLARA, CA 95050, USA

NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

INTERNAL TMDS .. LINK A & B



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK A & PU's, DVI CONNECTOR SOUTH

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2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

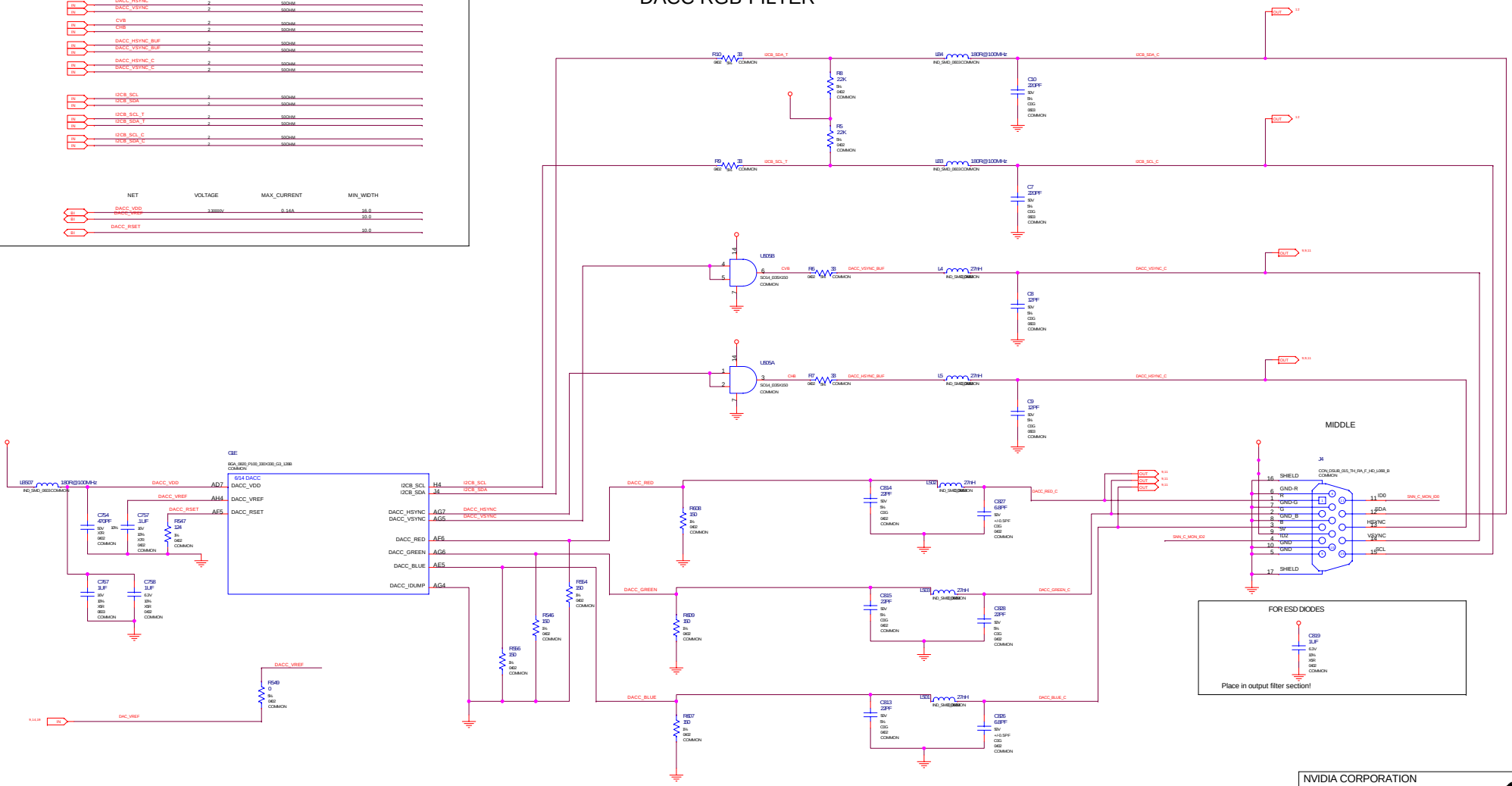
Secondary Display (DACC), DB15

DACC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACC_RED	1	50OHM	
DACC_GREEN	1	50OHM	
DACC_BLUE	1	50OHM	
DACC_RED_C	1	50OHM	
DACC_GREEN_C	1	50OHM	
DACC_BLUE_C	1	50OHM	
DACC_HSYNC	2	50OHM	
DACC_VSYNC	2	50OHM	
CVB	2	50OHM	
CHB	2	50OHM	
DACC_HSYNC_BUF	2	50OHM	
DACC_VSYNC_BUF	2	50OHM	
DACC_HSYNC_C	2	50OHM	
DACC_VSYNC_C	2	50OHM	
I2CB_SCL	2	50OHM	
I2CB_SDA	2	50OHM	
I2CB_SCL_T	2	50OHM	
I2CB_SDA_T	2	50OHM	
I2CB_SCL_C	2	50OHM	
I2CB_SDA_C	2	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACC_VDD	3.30000V	0.14A	10.0
DACC_VREF			10.0
DACC_RSET			10.0

DACC RGB-FILTER



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

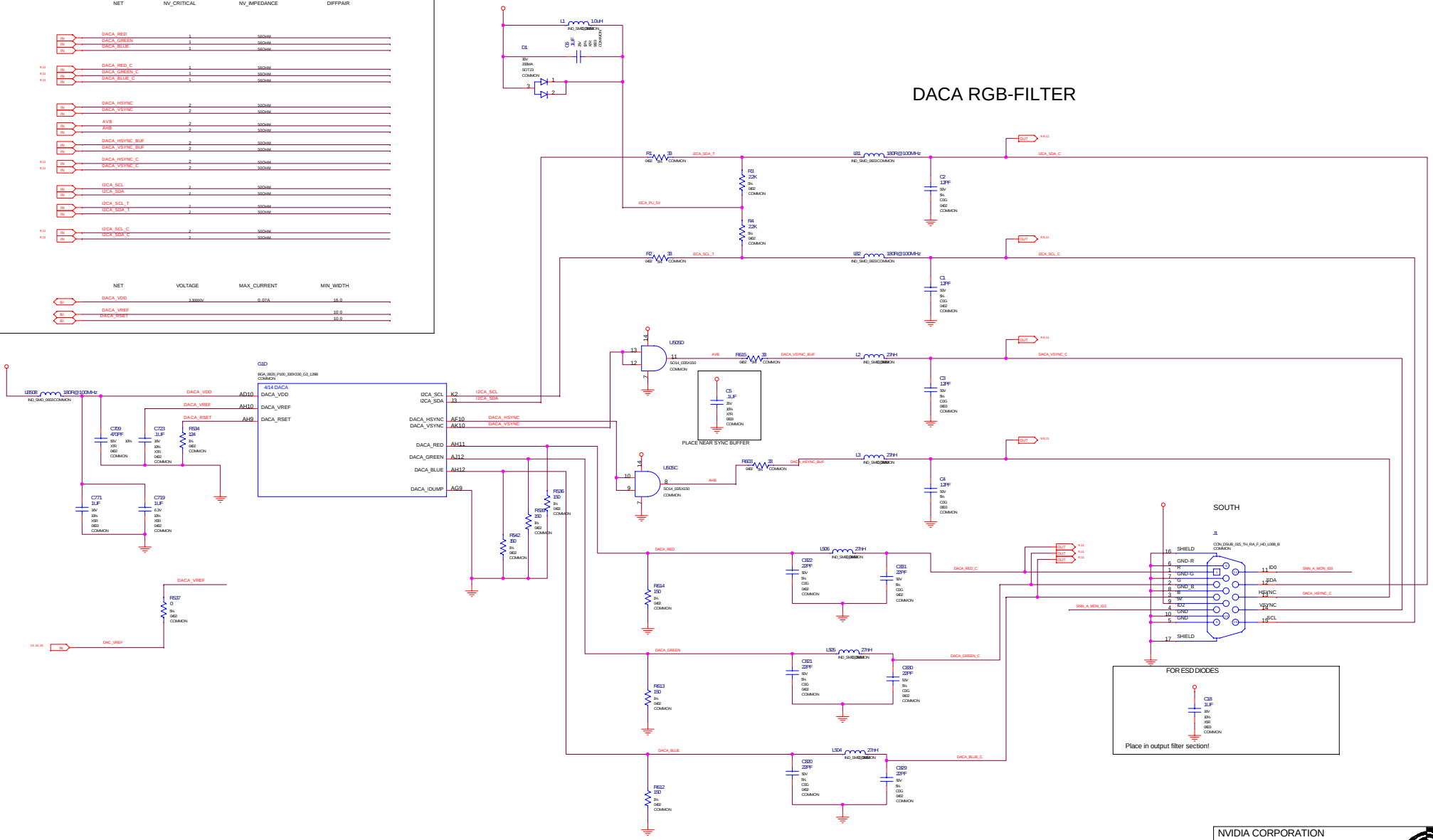
Primary Display (DACA), Slim DB15

DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACA_RED	1	50OHM	
DACA_GREEN	1	50OHM	
DACA_BLUE	1	50OHM	
DACA_RED_C	1	50OHM	
DACA_GREEN_C	1	50OHM	
DACA_BLUE_C	1	50OHM	
DACA_HSYNC	2	50OHM	
DACA_VSYNC	2	50OHM	
AVB	2	50OHM	
AYB	2	50OHM	
DACA_HSYNC_BUF	2	50OHM	
DACA_VSYNC_BUF	2	50OHM	
DACA_HSYNC_C	2	50OHM	
DACA_VSYNC_C	2	50OHM	
I2CA_SCL	2	50OHM	
I2CA_SDA	2	50OHM	
I2CA_SCL_T	2	50OHM	
I2CA_SDA_T	2	50OHM	
I2CA_SCL_C	2	50OHM	
I2CA_SDA_C	2	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACA_VDD	3.30000V	0.07A	16.0
DACA_VREF			10.0
DACA_RSET			10.0

DACA RGB-FILTER



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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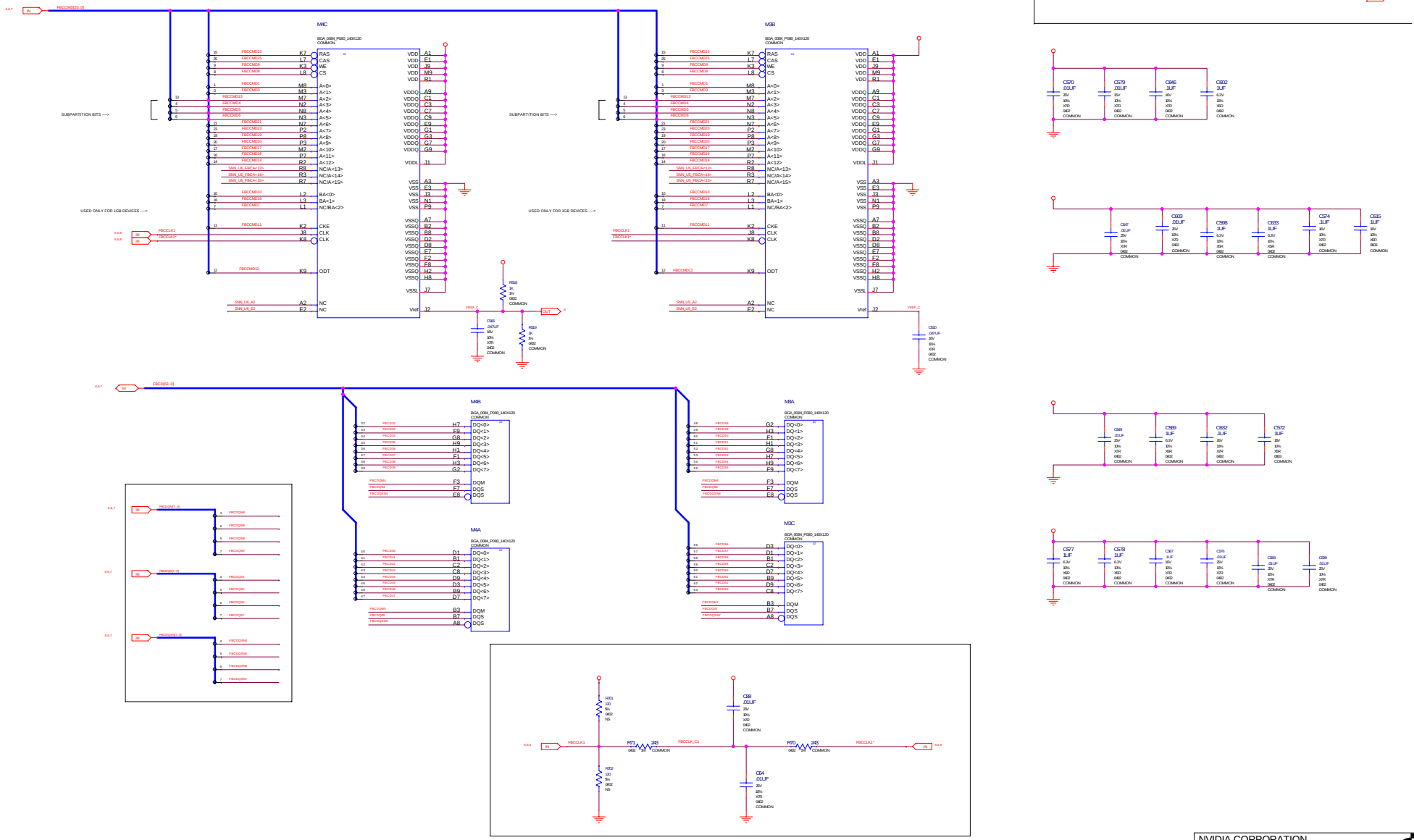
SANTA CLARA, CA 95050, USA

NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

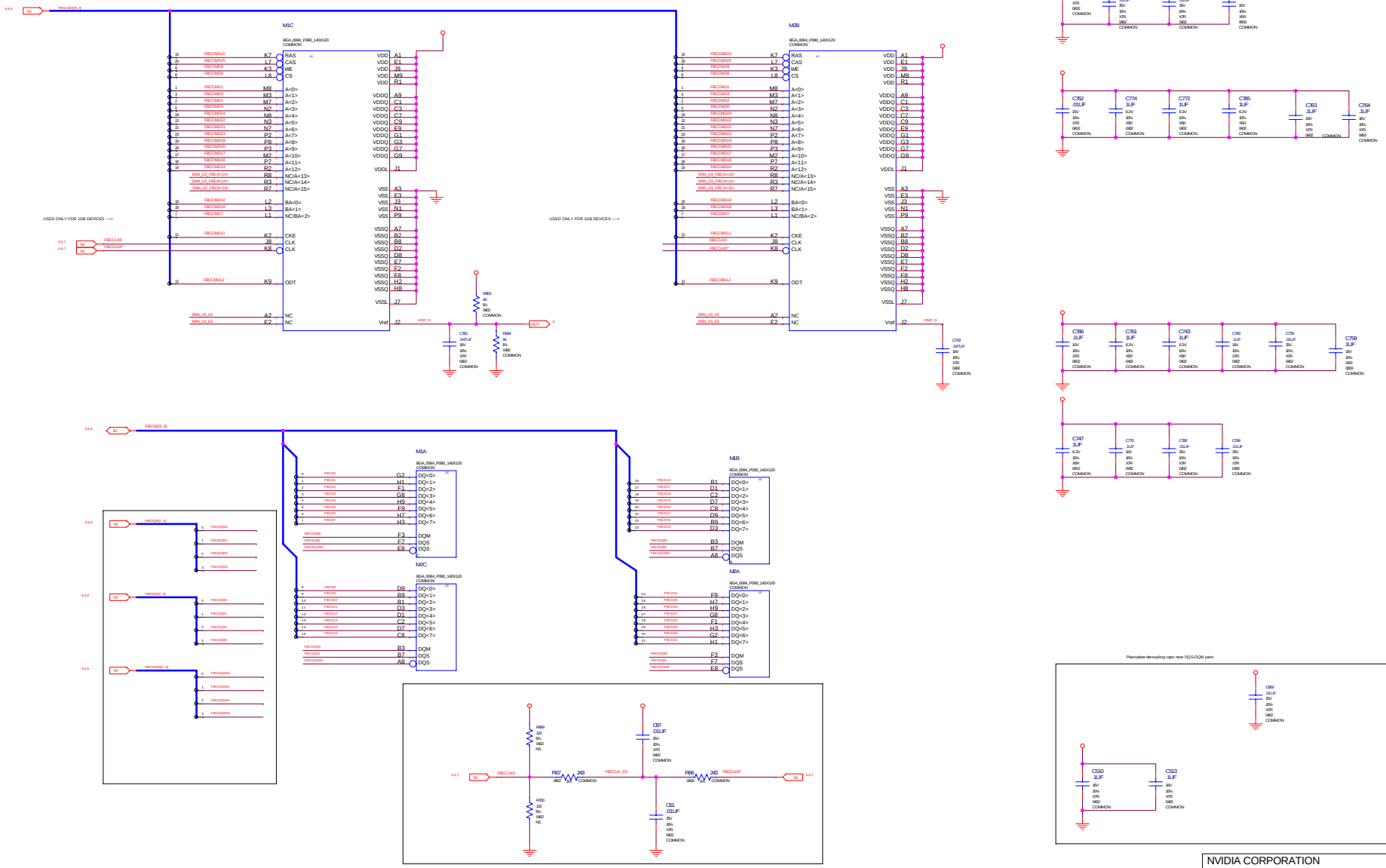
FBC MEMORY 2nd bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



FBC MEMORY 2nd bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16MX16 DDR2 MEMORIES, 2ND BANK 0..31

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NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

GIC
3/14 FBC
PLACE CLOSE TO
TERMINATION RISISTORS
DDR2 OPERATION:
1) During initialization CKE and ODT low
2) Runtime - CKE high and ODT operated by debug state machine
3) No termination rpak for CKE or DEBUG pins
FBC CMD/ADDR TERMINATIONS:
PD REQUIRED FOR INITIALIZATION OF DDR2
Place close to balls
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ASSEMBLY BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL FBC MEMORY INTERFACE, GPU FBVTT, FBVDDQ
DATE 12-JAN-2007
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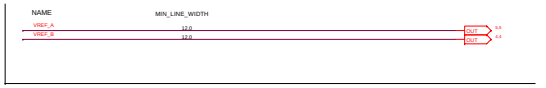
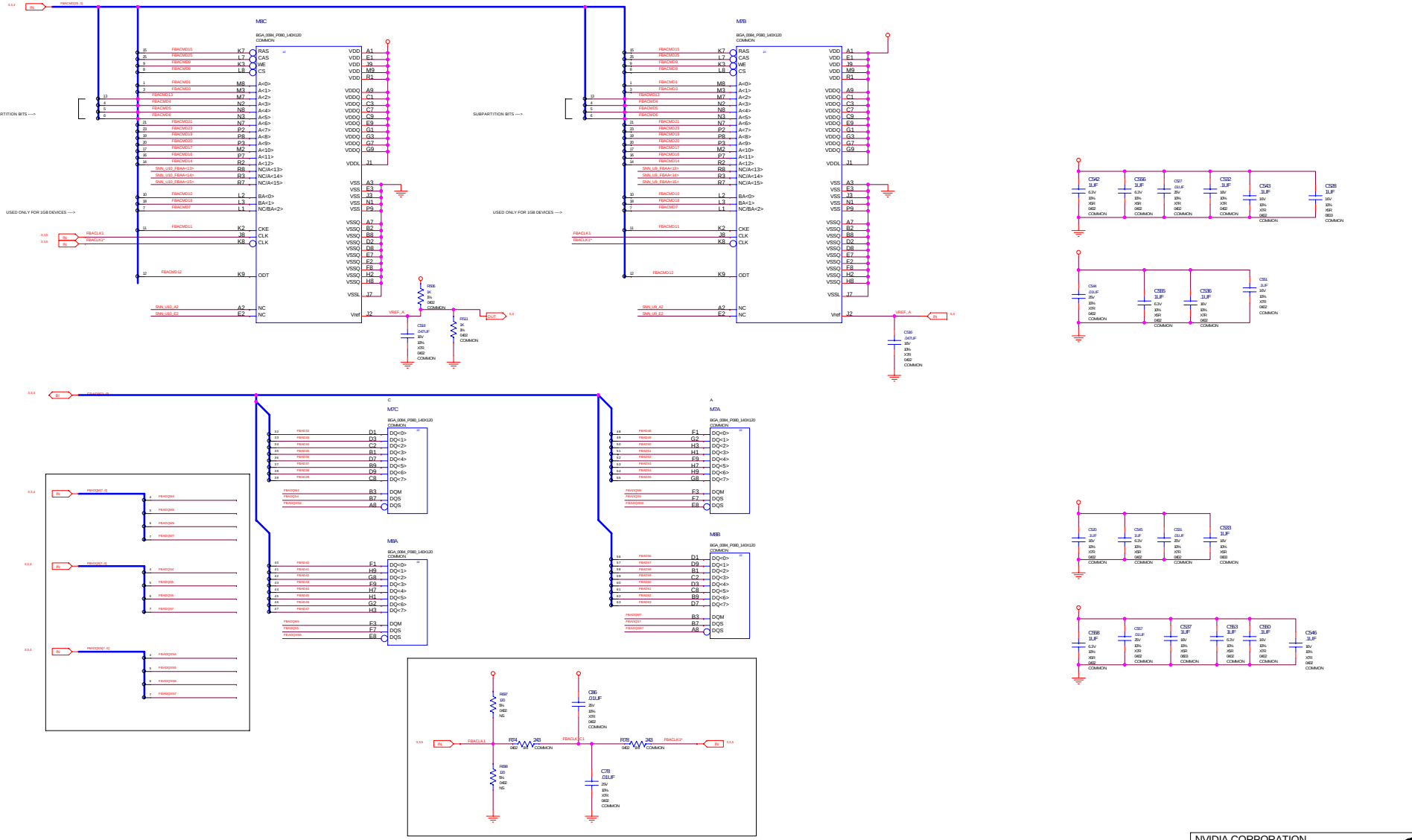
FBA MEMORY 1st bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16Mx16 DDR2 MEMORIES, 1ST BANK 32..63

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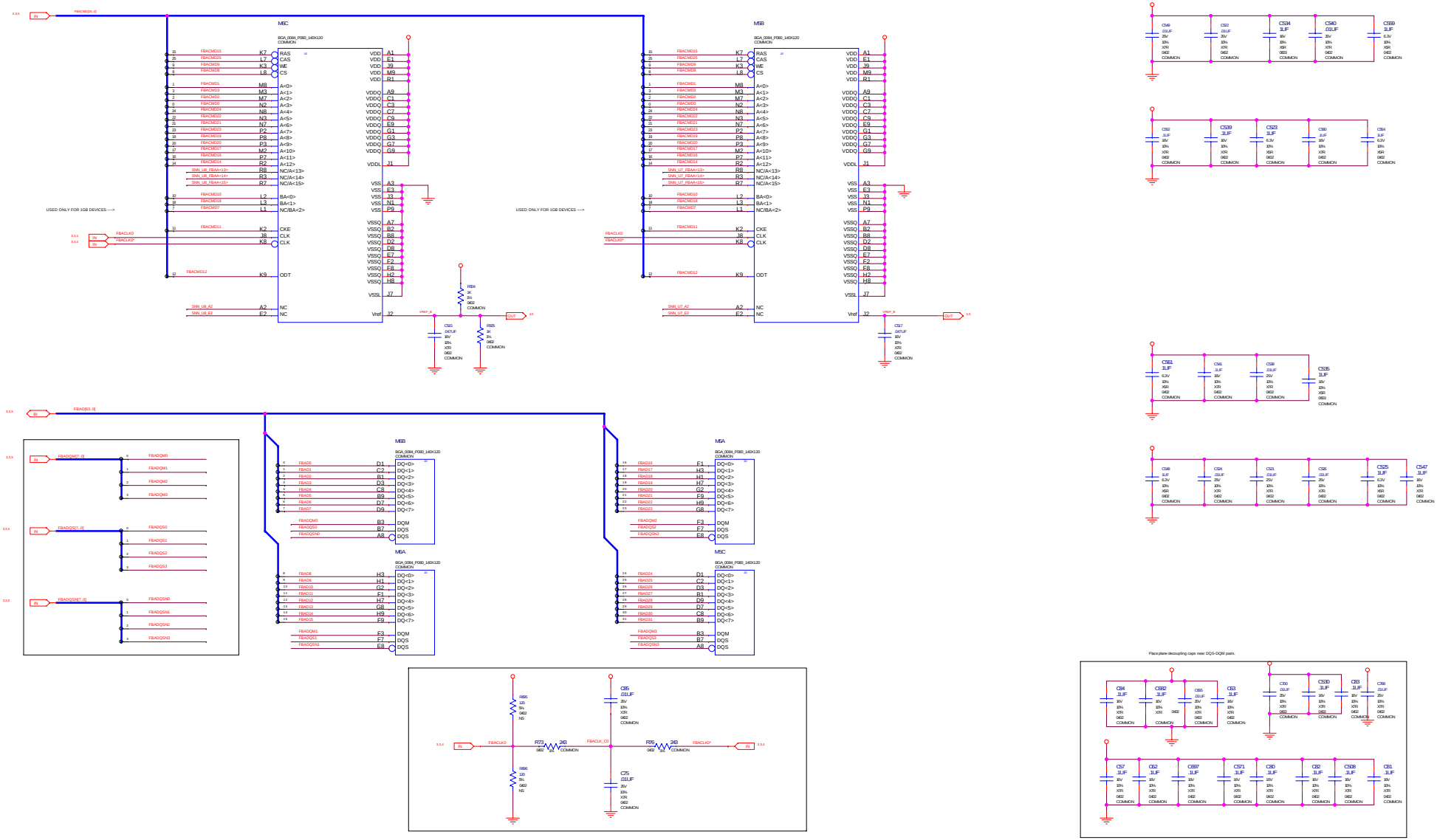
NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

FBA MEMORY 1st bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16Mx16 DDR2 MEMORIES, BANK 0..31

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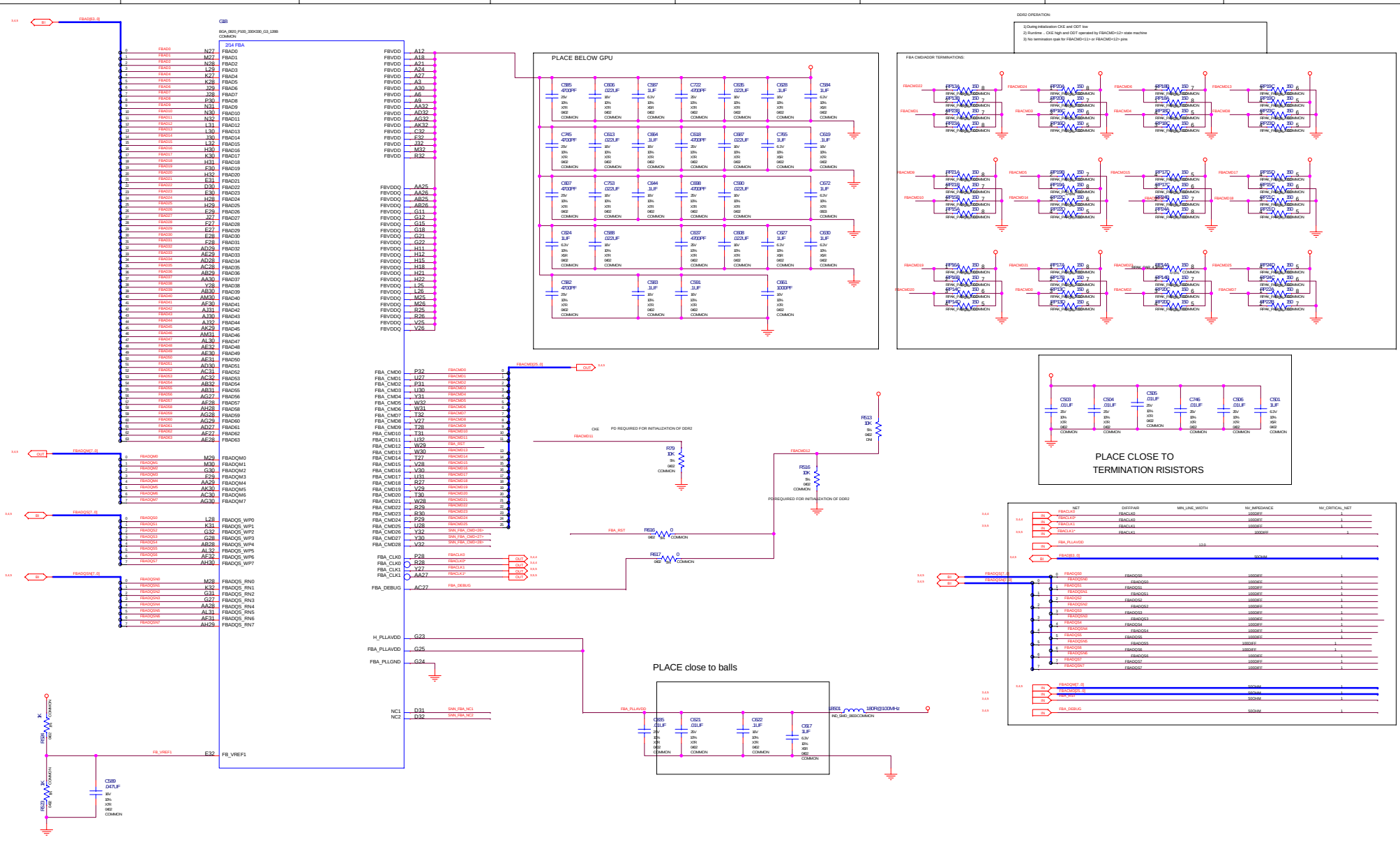
NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY INTERFACE, GPU FBVDDQ DECOUPLING CAPS, FBVTT TERMINATION

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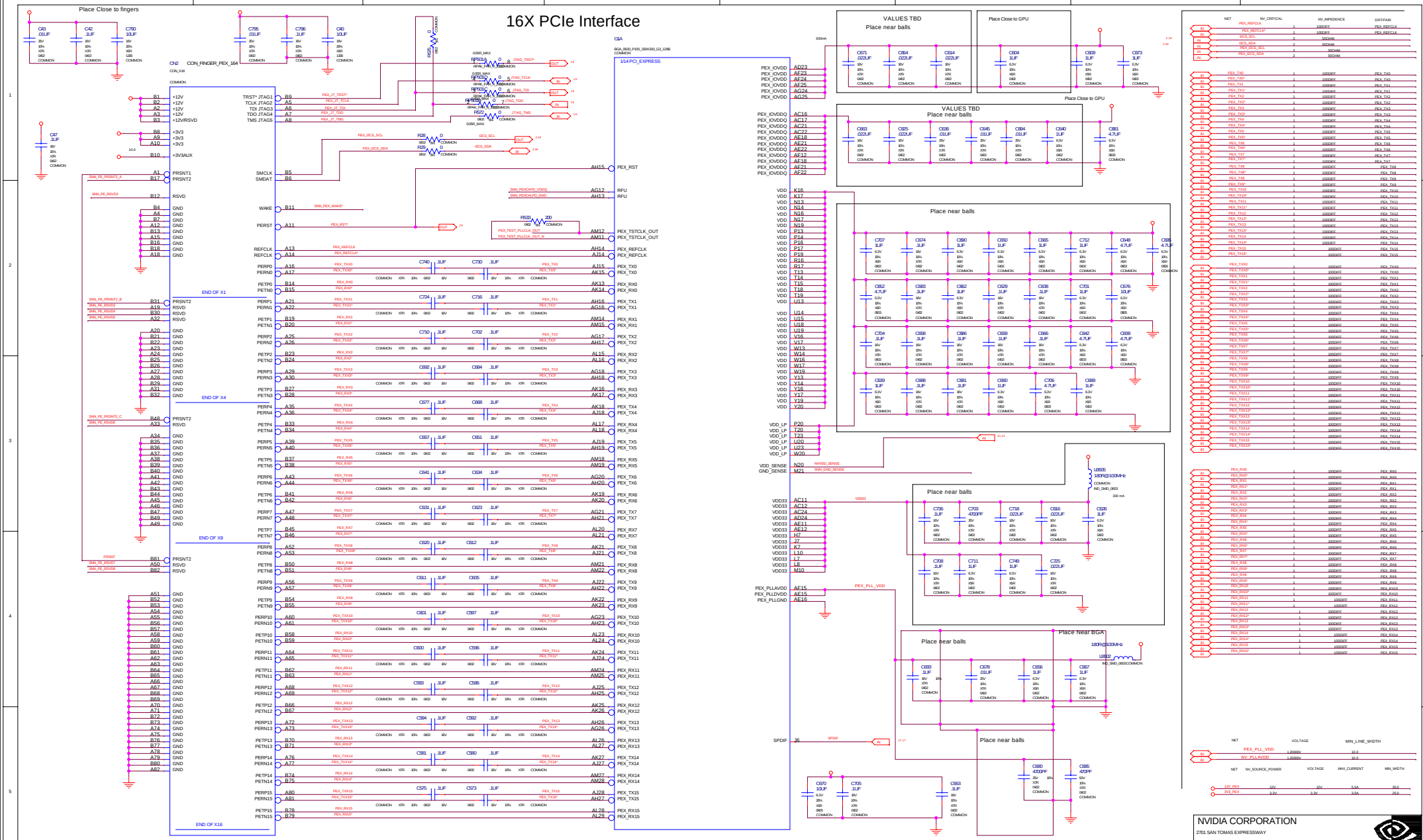
NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

16X PCIe Interface



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS 16X, NVVDD DECOUPLING CAPS,PEX_IOVDDQ DECOUPLING CAPS

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NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007

P403-B00 DESIGN -- G84-200, 256 MB DDR2,DVI-I, VGA, HDTV

PAGE SUMMARY:

sku	VARIANT	NVPN	ASSEMBLY
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2	SKU0021	600-10403-0021-200	P403-B00 G84-200 459/400MHz 256MB 16Mx16 BGA84 GDDR2 DVI-I-DL+VGA+HDTV-Out
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TABLE OF CONTENTS & REVISION HISTORY

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NV_PN	600-10403-0000-200 A		
ID		PAGE	
NAME		DATE	12-JAN-2007