DVI-D_DL (DP + DP) + HDMI (DP) + DP TABLE OF CONTENTS Page Description Page Description 26 PS V: NVVDD Phase 3 Table of Contents 27 MECH: Bracket/Thermal Block Diagram PCI Express MEMORY: GPU Partition A/B MEMORY: FBA[31:0] MEMORY: FBA[63:32] MEMORY: FBB[31:0] MEMORY: FBB[63:32] GPU FBVDDQ & 1V8 Decoupling GPU NVVDD & NVVDDS DECOUPLING 10 11 IFPAB DVI-DL 12 IFPD DP 13 IFPC HDMI 14 IFPEF UNUSED MISC1: Fan, Thermal, JTAG, GPIO MISC2: ROM, XTAL, Straps 17 Power Inputs and Filtering Power Sequence 19 PS: NV3V3 & NV12V 20 PSI: 1V8 21 PSII: 5V & 12V_FAN 22 PS III: PEXVDD 23 PS IV: FBVDDQ PS V: NVVDD OVR2+1 24 PS V: NVVDD Phase 1,2 NVIDIA CORPORATION SANTA CLARA, CA 95050, USA PAGE DETAIL Table of Content NV_PN 600-1G210-BASE-SCH ALL MIDIA DESIGN SPECIFICATIONS, REFERENCE SPECFICATIONS, REFERENCE BOARDS, FLES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVATIONS OF HOUSTRY STANDARDS AND SPECIFICATIONS. WIDIA MAKES NO WARRANTIES, EXPRESSED, MPLED, STATUTIORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSELY DISCLAMAS ALL MPLED WARRANTIES INCLIDING, WITHOUT LIMITATION, THE WARRANTES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS. PCB REV BOM REV DATE dd-mon-year

PG210 B00

GP107 128b GDDR5, 75W, PCB 5.7"



















































