PCI-EXPRESS EDGE CONNECTOR

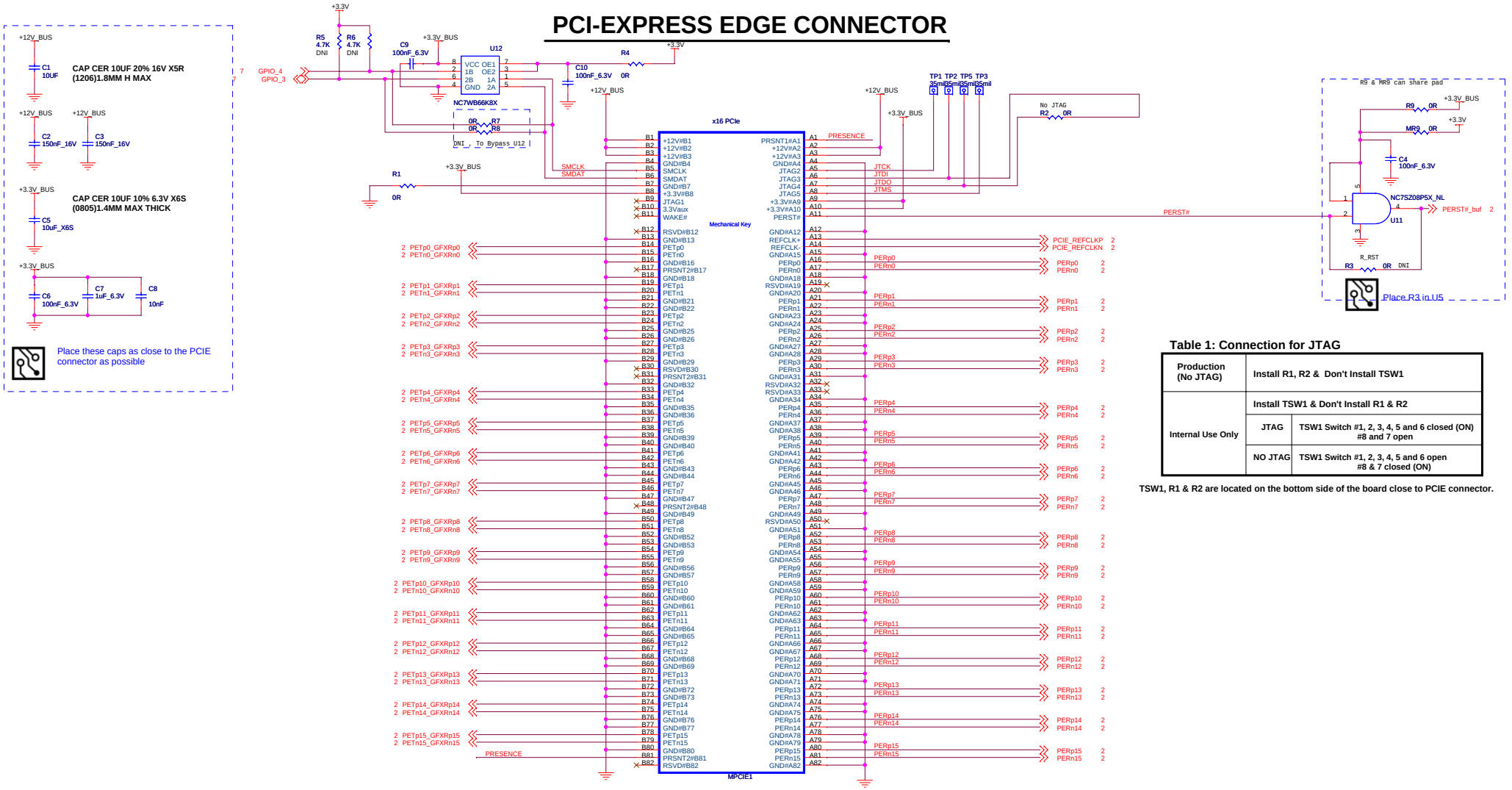

Table 1: Connection for JTAG

Production (No JTAG)	Install R1, R2 & Don't Install TSW1	
Internal Use Only	Install TSW1 & Don't Install R1 & R2	
	JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open
	NO JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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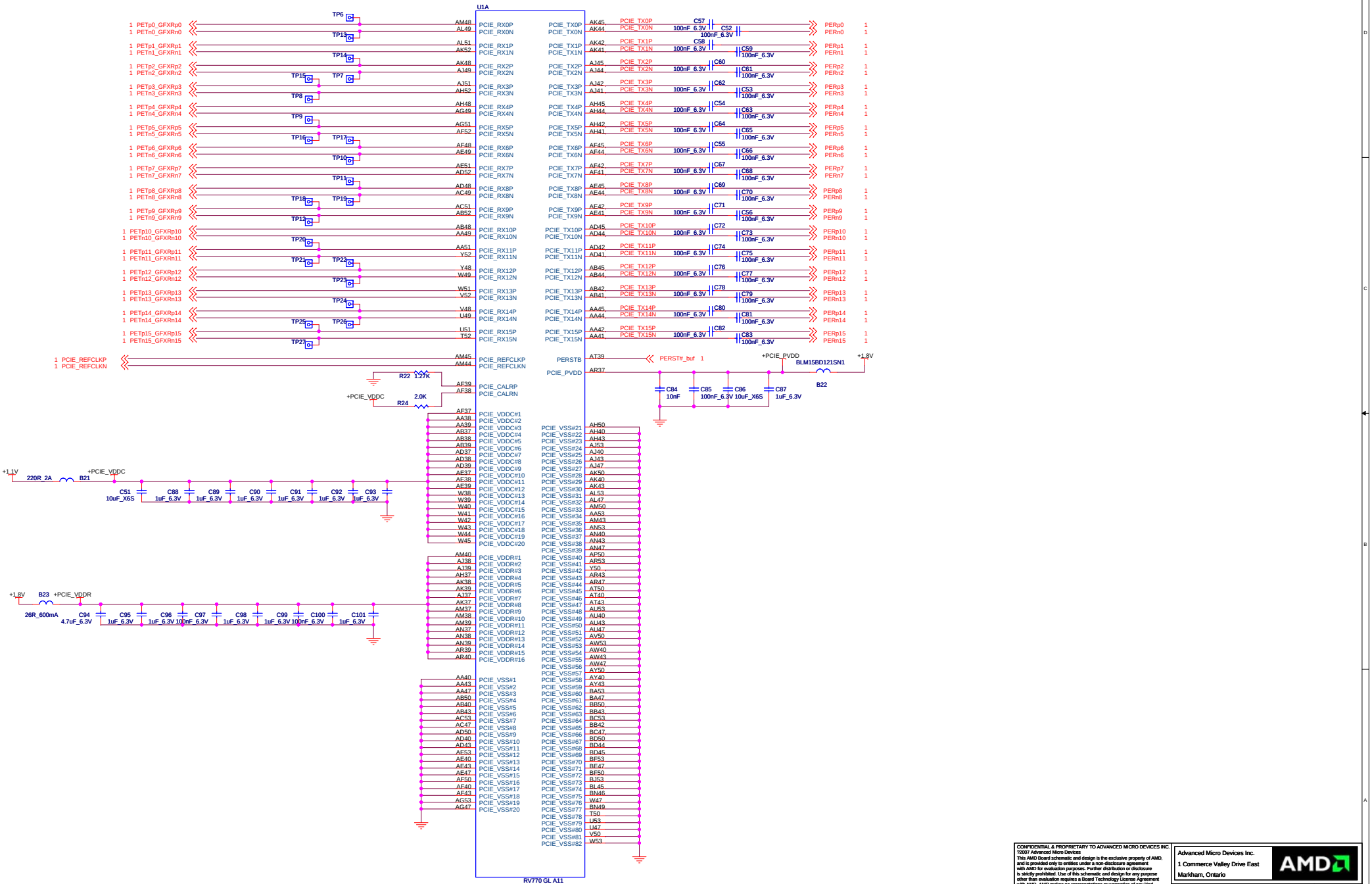
Title: RH RV770 GDDR5 DVI-I VO DVI-I PH

Opt No. 105-B507xx-11

NOTE: some of the PCIE testpoints will
be available trought via on traces.



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Title RH RV770 GDDR5 DVI-I VO DVI-I FH

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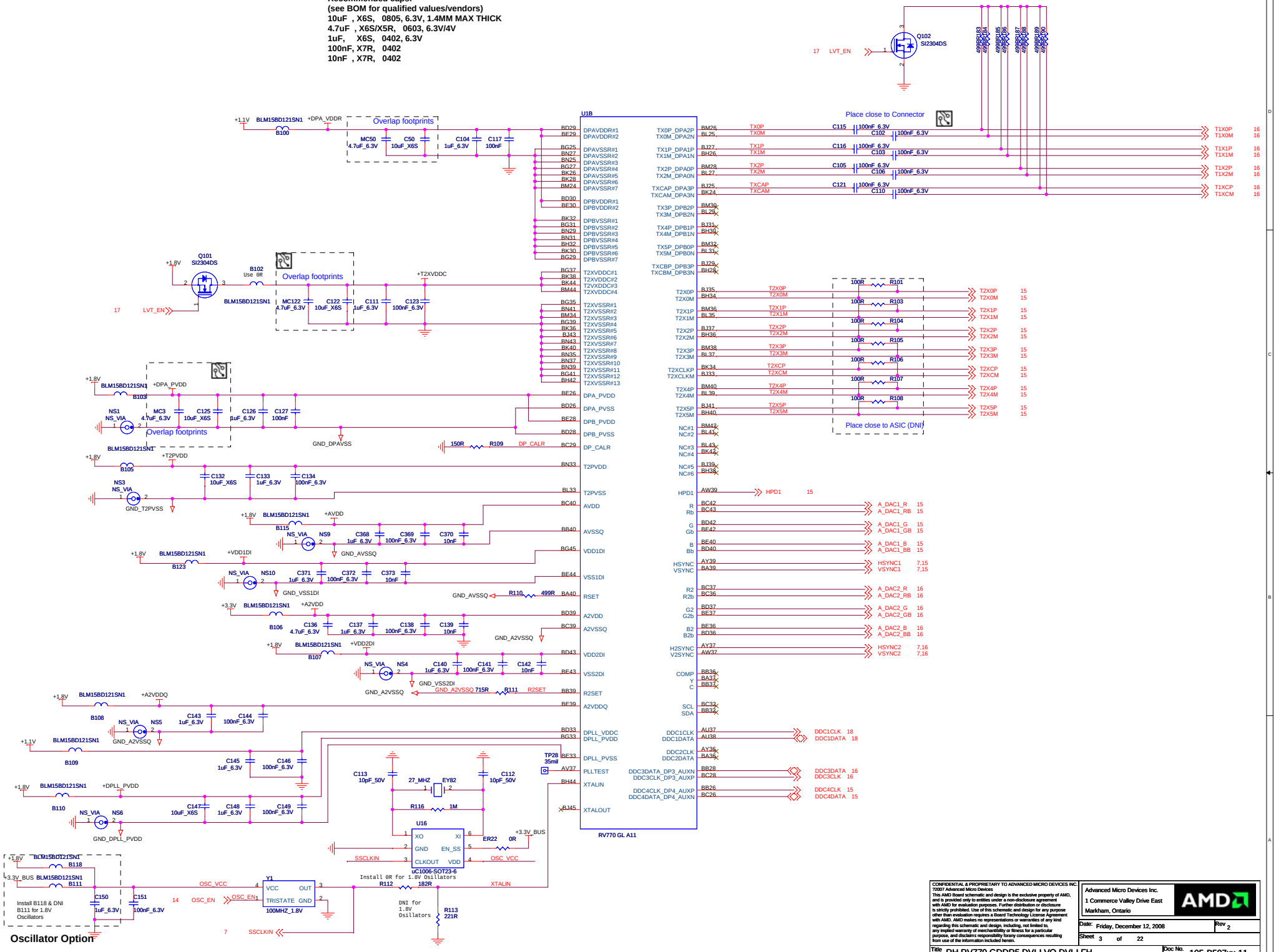
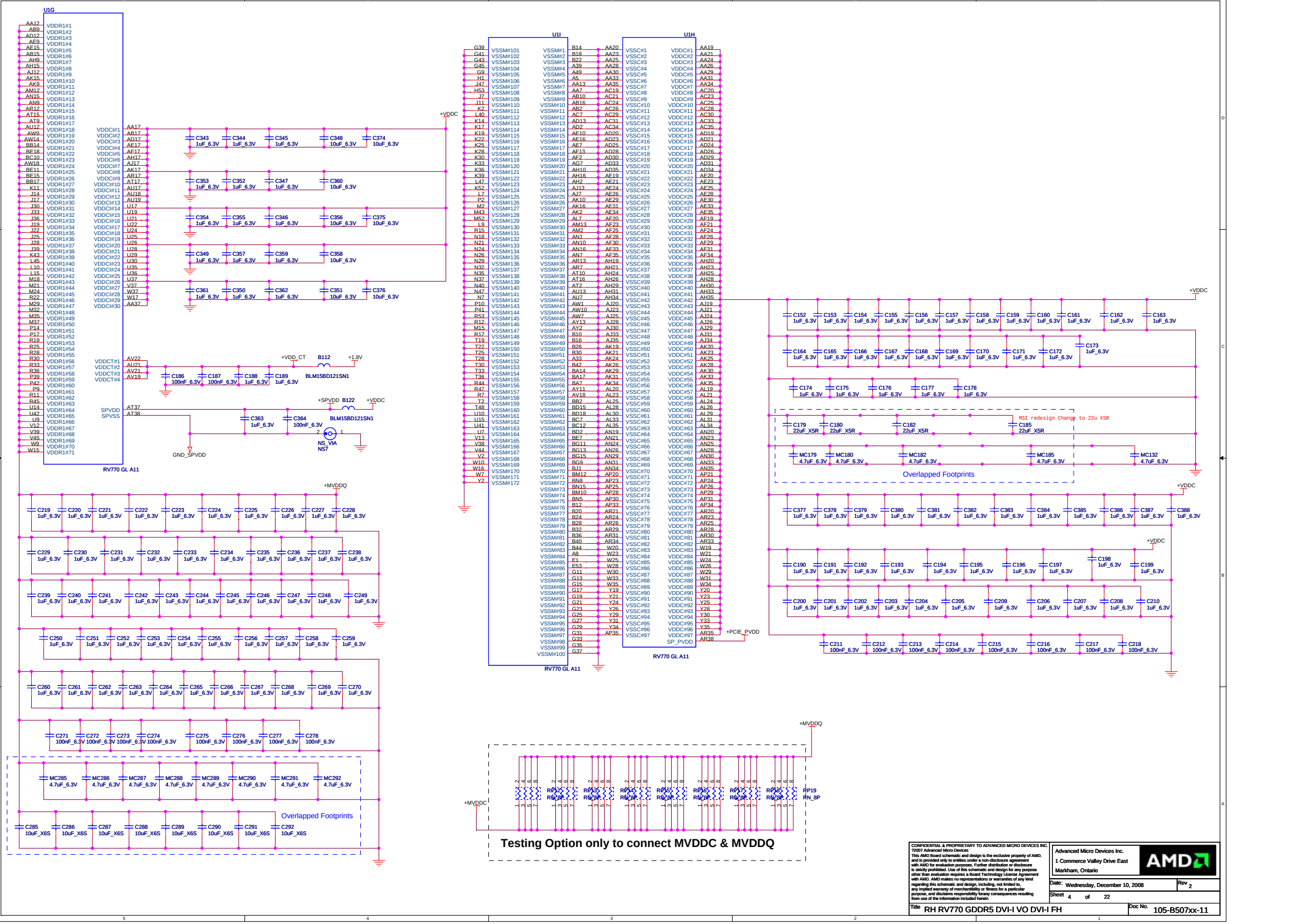
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402





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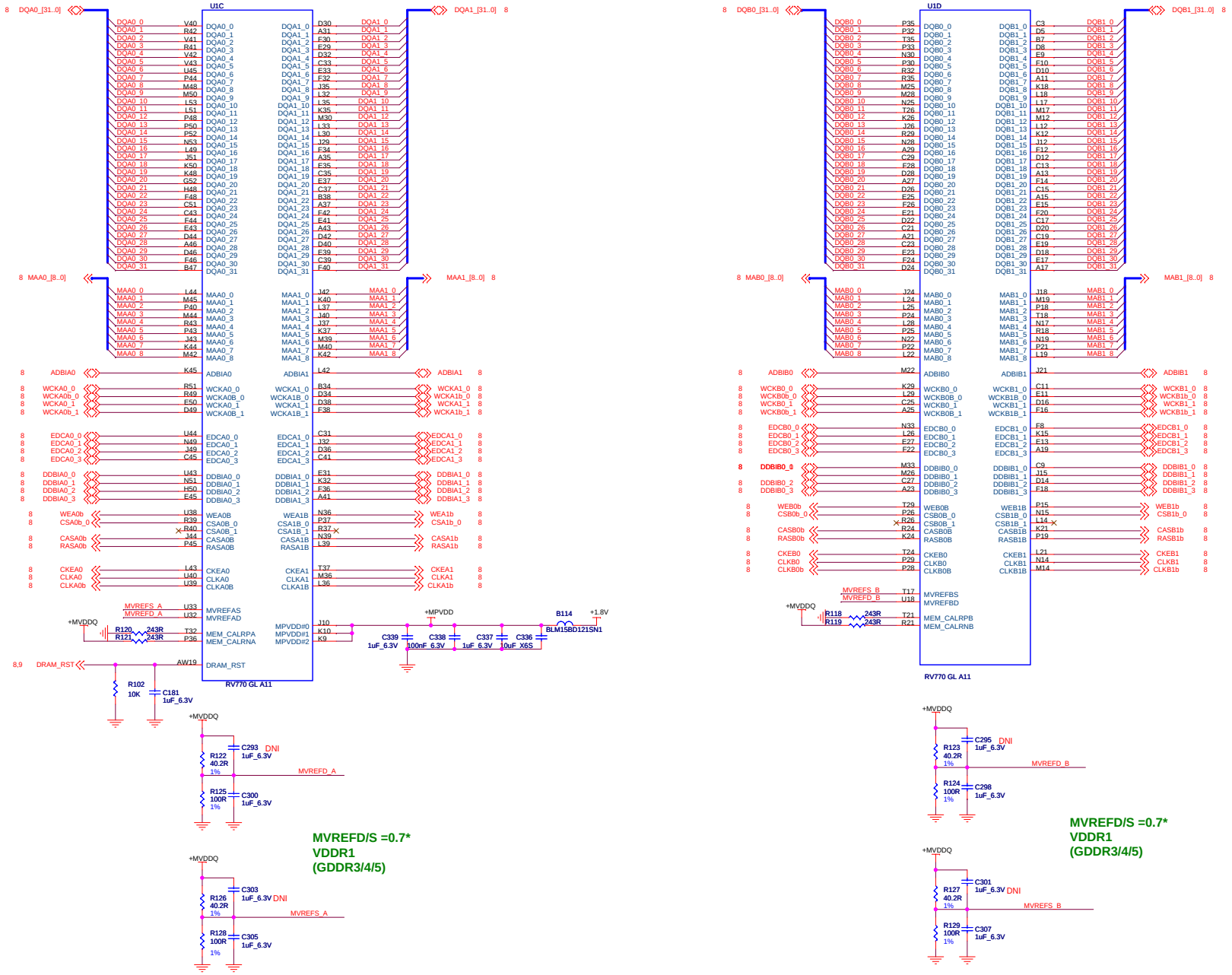

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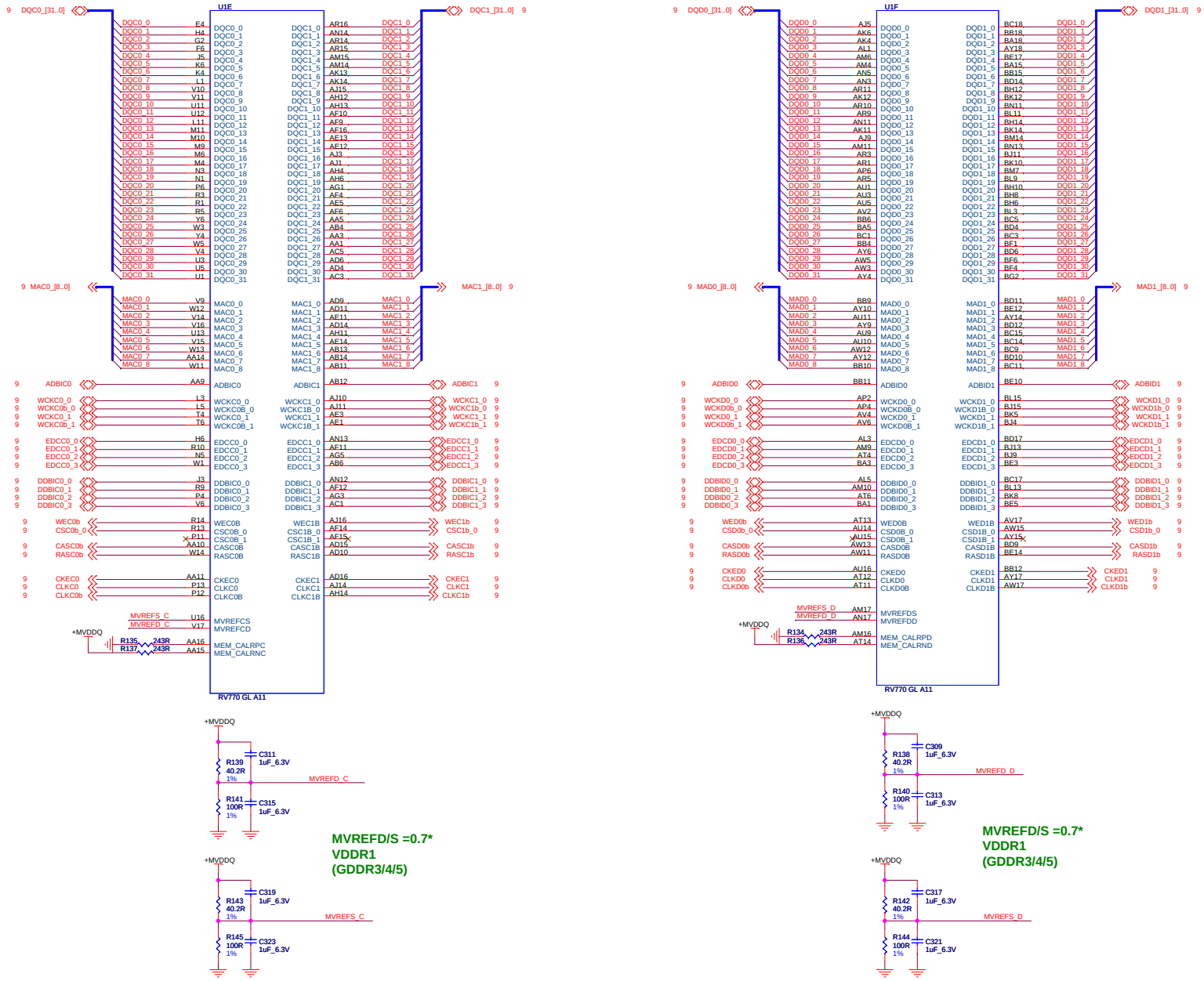
PH Part No.	105-B507xx-11



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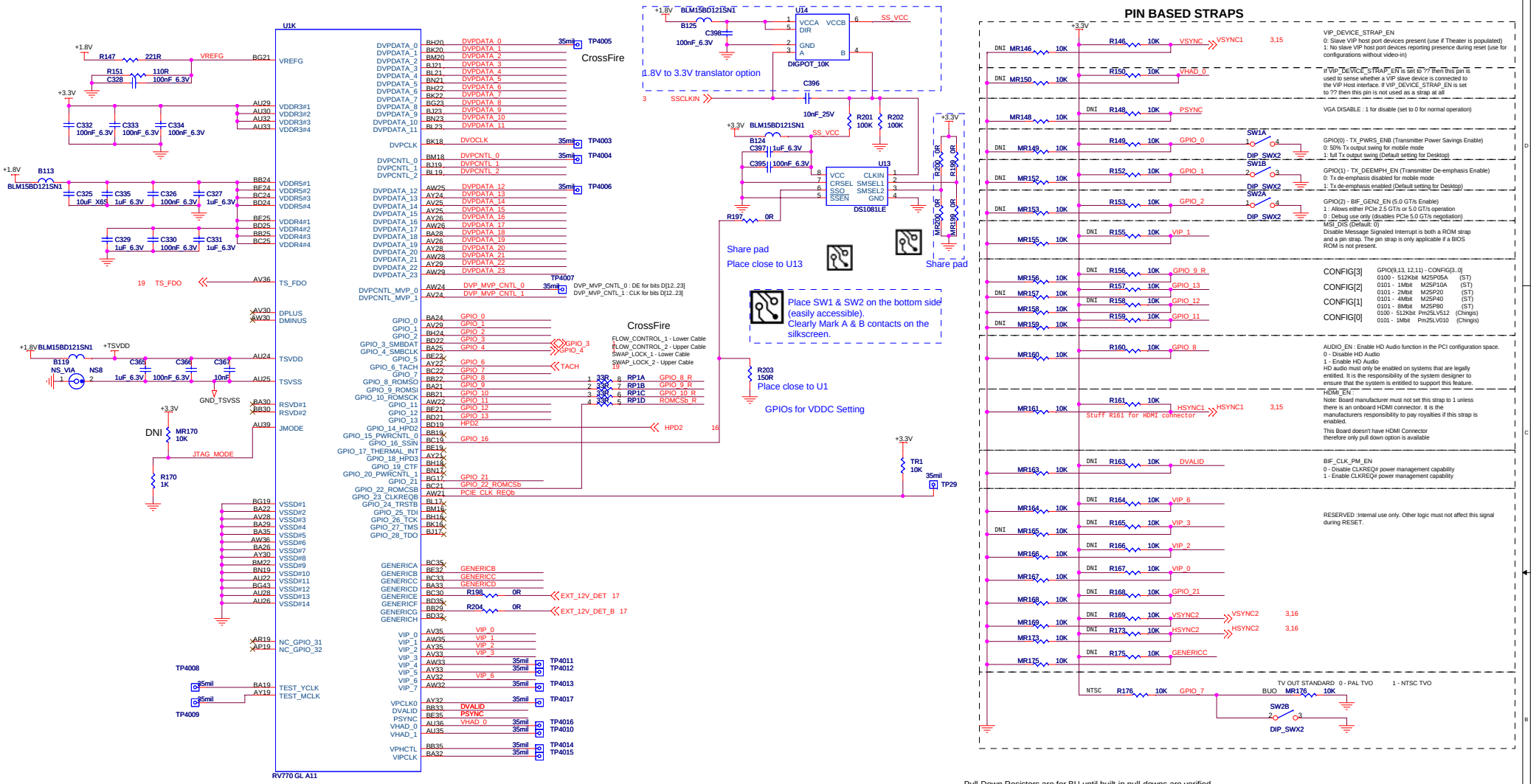
U1K
RV770 GL A11
CrossFire Card-Edge
CrossFire
1.8V to 3.3V translator option
DIGPOT_10K
DS1081LE
Share pad
Place close to U13
Share pad
Place SW1 & SW2 on the bottom side (easily accessible).
Clearly Mark A & B contacts on the silkscreen.
Place close to U1
GPIOs for VDDC Setting
PIN BASED STRAPS
VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)
If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all
VGA DISABLE : 1 for disable (set to 0 for normal operation)
GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)
GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)
GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
1 : Allows either PCIe 2.5 GT/s or 5.0 GT/s operation
0 : Debug use only (disables PCIe 5.0 GT/s negotiation)
MSI_DIS (Default: 0)
Disable Message Signaled Interrupt is both a ROM strap and a pin strap. The pin strap is only applicable if a BIOS ROM is not present.
CONFIG[3] GPIO(9,13, 12,11) - CONFIG[3..0]
CONFIG[2] 0100 - 512Kbit M25P05A (ST)
CONFIG[1] 0101 - 1Mbit M25P10A (ST)
CONFIG[0] 0101 - 2Mbit M25P20 (ST)
0101 - 4Mbit M25P40 (ST)
0101 - 8Mbit M25P80 (ST)
0100 - 512Kbit Pm25LV512 (Chingis)
0101 - 1Mbit Pm25LV010 (Chingis)
AUDIO_EN : Enable HD Audio function in the PCI configuration space.
0 - Disable HD Audio
1 - Enable HD Audio
HD audio must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.
HDMI_EN :
Note: Board manufacturer must not set this strap to 1 unless there is an onboard HDMI connector. It is the manufacturers responsibility to pay royalties if this strap is enabled.
This Board doesn't have HDMI Connector therefore only pull down option is available
BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability
RESERVED :Internal use only. Other logic must not affect this signal during RESET.
TV OUT STANDARD 0 - PAL TVO 1 - NTSC TVO
Pull-Down Resistors are for BU until built-in pull-downs are verified.
Lower Cable Card Edge
Upper Cable Card Edge
Bundle B
Bundle A (closer to the bracket)
GENERICB: Generic I2C_SDA
DVALID: Generic I2C_SCL
PM25LV010-25SCE
PN 2280007900G for 1Mbit (PM25LV010A-100SCE)
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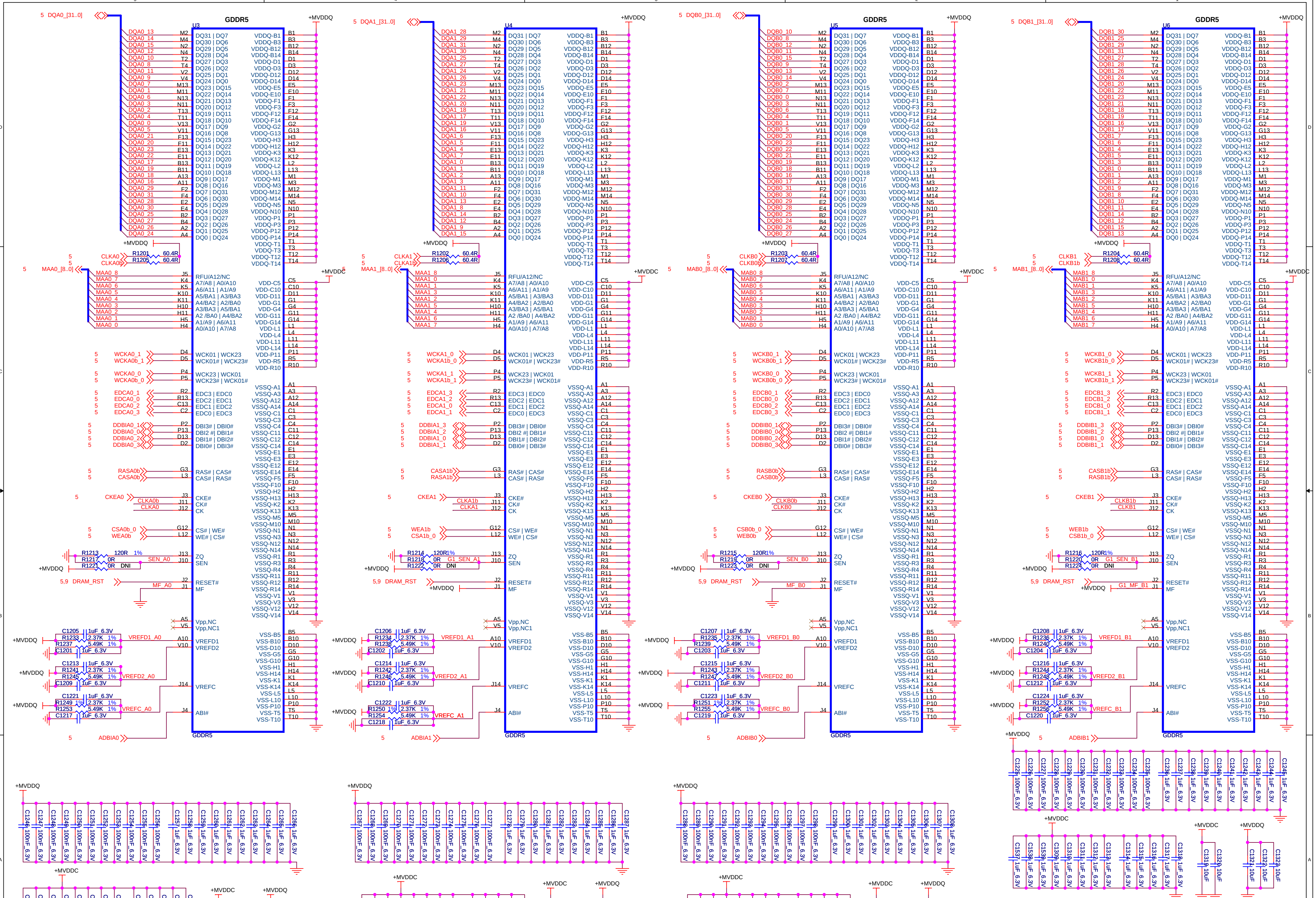

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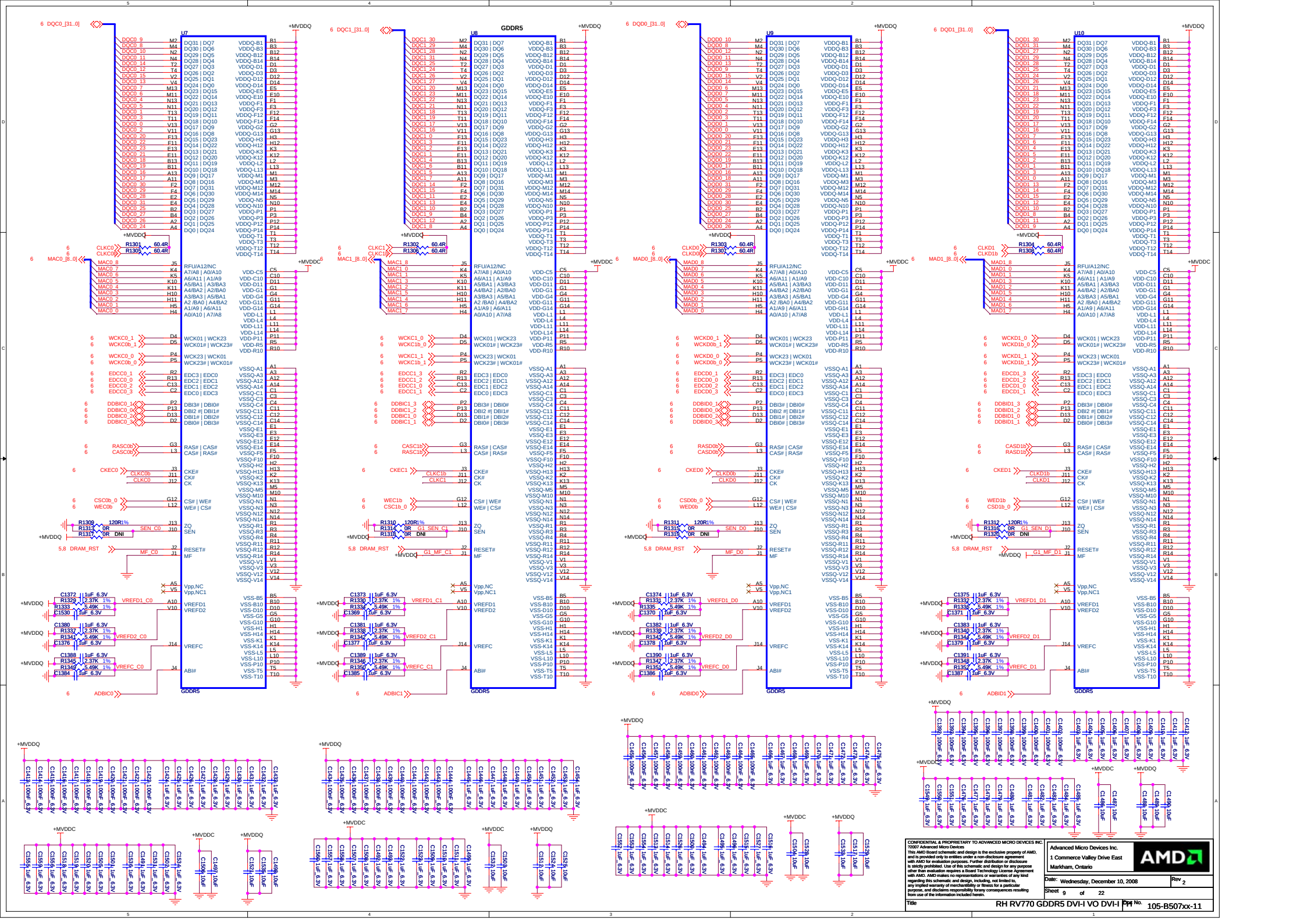

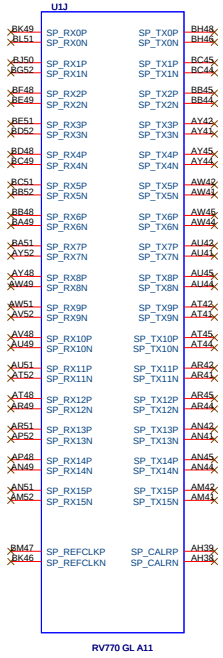

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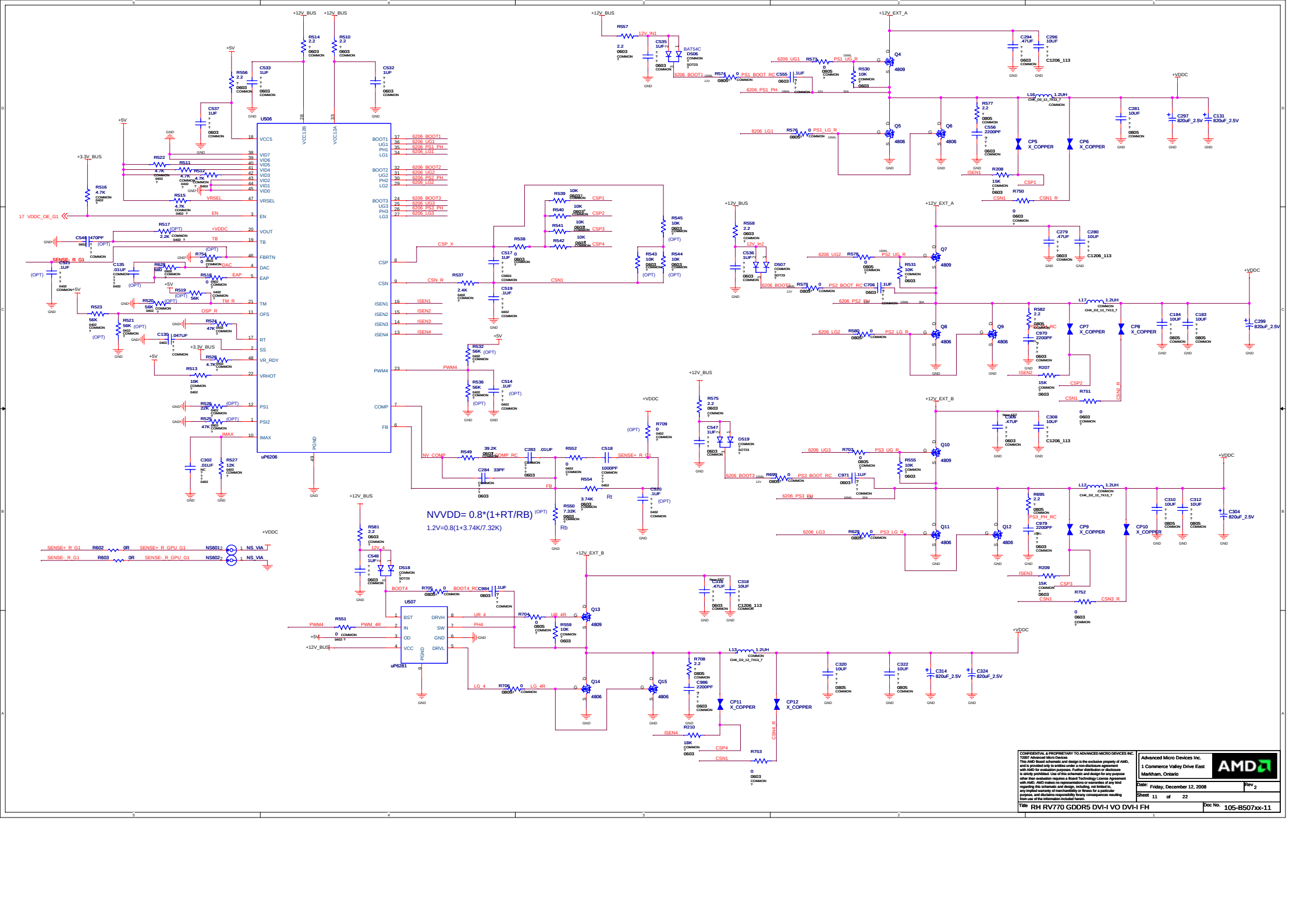
U506
uP6206
U507
uP6281
NVVDD= 0.8*(1+RT/RB) (OPT)
1.2V=0.8(1+3.74K/7.32K)
Rt
Rb
SENSE- R G1
SENSE+ R G1
NS_VIA
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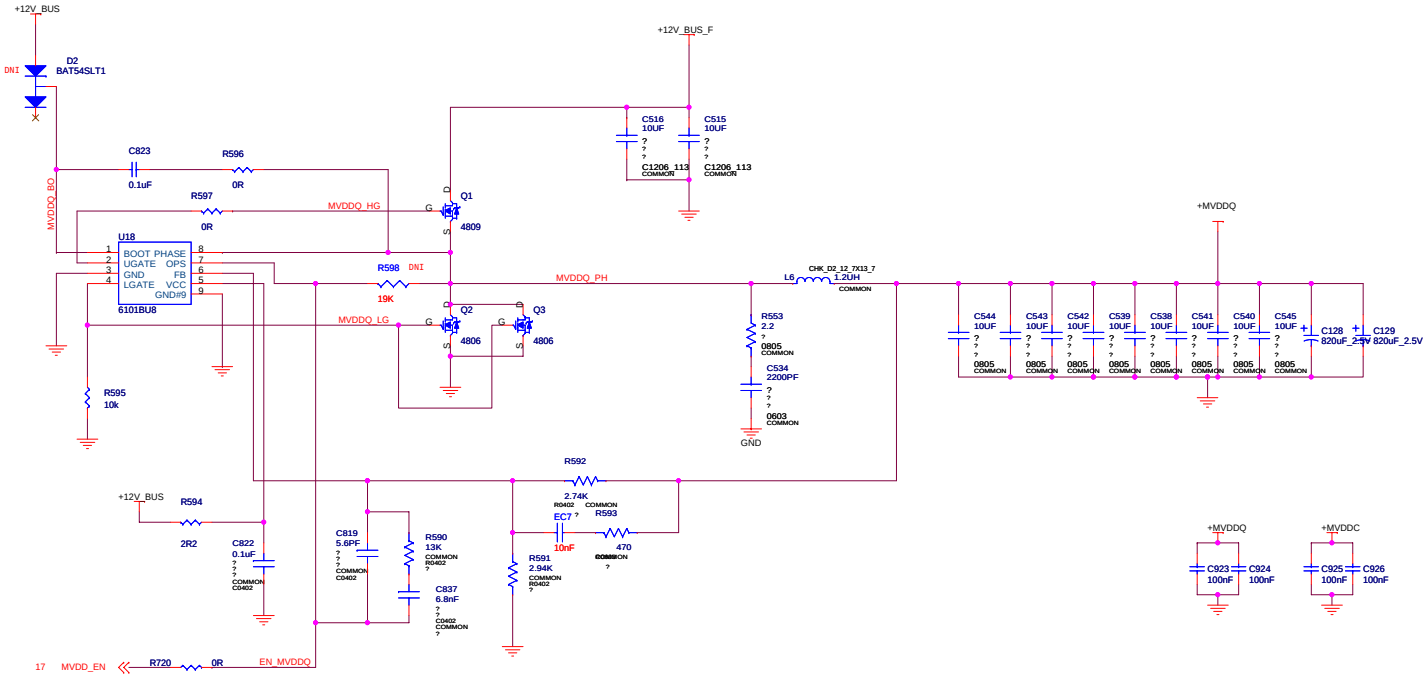

+MVDDQ=0.8*(1+(R592 / R591)

+MVDDQ=0.8*(1+(2.74 / 3.09)=1.509V
+MVDDQ=0.8*(1+(2.74 / 2.94)=1.545V

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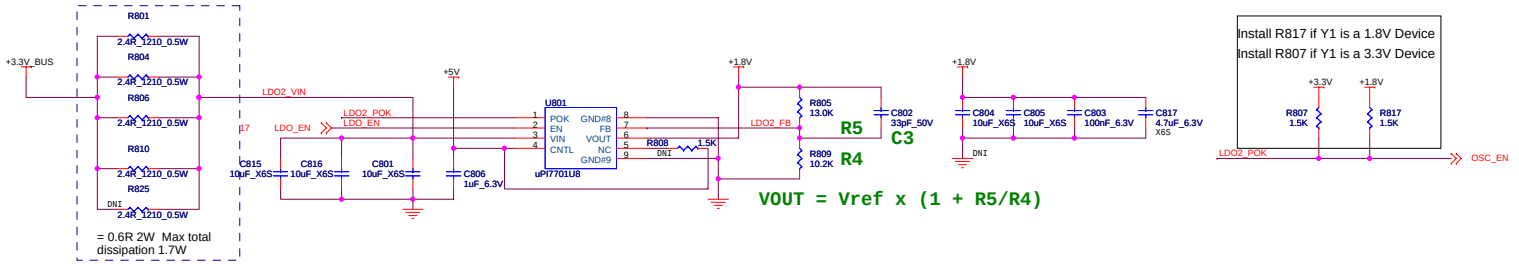
LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 1.7A (TBV) RMS MAX

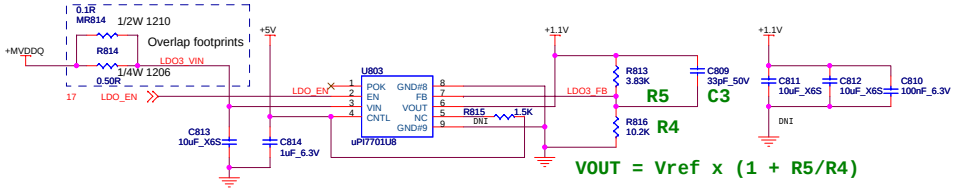
PCB: Min 70mm sq. copper area for cooling



VOUT = Vref x (1 + R5/R4)

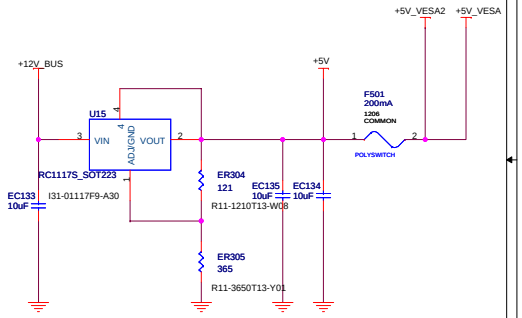
LDO #3: Vin = +1.50V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX

PCB: Min 70mm sq. copper area for cooling



VOUT = Vref x (1 + R5/R4)

Regulators for +5V, +5V_VESA and +5V_VESA2



Vout=1.25V* [1+(ER305/ER304)]

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See BOM for qualified filters

3 A_DAC1_R — R1001 75R 402 — C1004 8.0pF 402 — L1001 47nH ML1001 36NH — C1001 12pF_50V 402

3 A_DAC1_RB — R1027 37.4R

3 A_DAC1_G — R1002 75R 402 — C1005 8.0pF 402 — L1002 47nH ML1002 36NH — C1002 12pF_50V 402

3 A_DAC1_GB — R1028 37.4R

3 A_DAC1_B — R1003 75R 402 — C1006 8.0pF 402 — L1003 47nH ML1003 36NH — C1003 12pF_50V 402

3 A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

L100x and ML100x footprints are overlapped

For ESD Protection

+3.3V — D1001 CM1213-04 (CH3, CH2, Vp, Vn, CH4, CH1)

+5V_VESA — D1002 CM1213-04 (CH3, CH2, Vp, Vn, CH4, CH1)

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

+5V_VESA — C1010 68pF 603

MJ1001 G3179C219-005

MJ1001		
1	R	
2	G	
3	B	
11	MS0	DDC2_MONID0
12	MS1	DDC2_MONID1(SDA)
4	MS2	DDC2_MONID2
15	MS3	DDC2_MONID3(SCL)
9	NC	
13	HS	
14	VS	
5	VSS	
6	VSS#6	
7	VSS#7	
8	VSS#8	
10	VSS#10	
16	CASE	
17	CASE#17	

3 DDC4DATA — +5V — R1005 2.2K — DDCDATA_DAC1_5V — R1006 33R 402 — DDCDATA_DAC1_R

3 DDC4CLK — +5V — R1008 2.2K — DDCCLK_DAC1_5V — R1009 33R 402 — DDCCLK_DAC1_R

3,7 HSYNC1 — U1999C 74VHC125 — HSYNC_DAC1_B — R1010 10R 402 — HSYNC_DAC1_R

3,7 VSYNC1 — U1999D 74VHC125 — VSYNC_DAC1_B — R1011 10R 402 — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

+3.3V — Q1021 MMBT3904 — R1022 10K — HPD_DVI2 — R1023 10K — 3 HPD1

+5V_VESA — J1001 DVI_CONNECTOR

J1001		
25	CASE	
1	T2X2M	TMDS Data2-
2	T2X2P	TMDS Data2+
3		TMDS Data2/4 Shield
4	T2X4M	TMDS Data4-
5	T2X4P	TMDS Data4+
6	DDCCLK_DAC1_R	DDC Clock
7	DDCDATA_DAC1_R	DDC Data
8	VSYNC_DAC1_R	Analog VSYNC
9	T2X1M	TMDS Data1-
10	T2X1P	TMDS Data1+
11		TMDS Data1/3 Shield
12	T2X3M	TMDS Data3-
13	T2X3P	TMDS Data3+
14		+5V Power
15		GND (for +5V)
16	HPD_DVI2	Hot Plug Detect
17	T2X0M	TMDS Data0-
18	T2X0P	TMDS Data0+
19		TMDS Data0/5 Shield
20	T2X5M	TMDS Data5-
21	T2X5P	TMDS Data5+
22		TMDS Clock Shield
23	T2XCP	TMDS Clock+
24	T2XCM	TMDS Clock-
C1	A_R_DAC1_F	Analog Red
C2	A_G_DAC1_F	Analog Green
C3	A_B_DAC1_F	Analog Blue
C4	HSYNC_DAC1_R	Analog HYNC
C5		Analog GND
C6		Analog GND#C6
26		CASE#26
27		CASE#27
28		CASE#28
29		CASE#29
30		CASE#30

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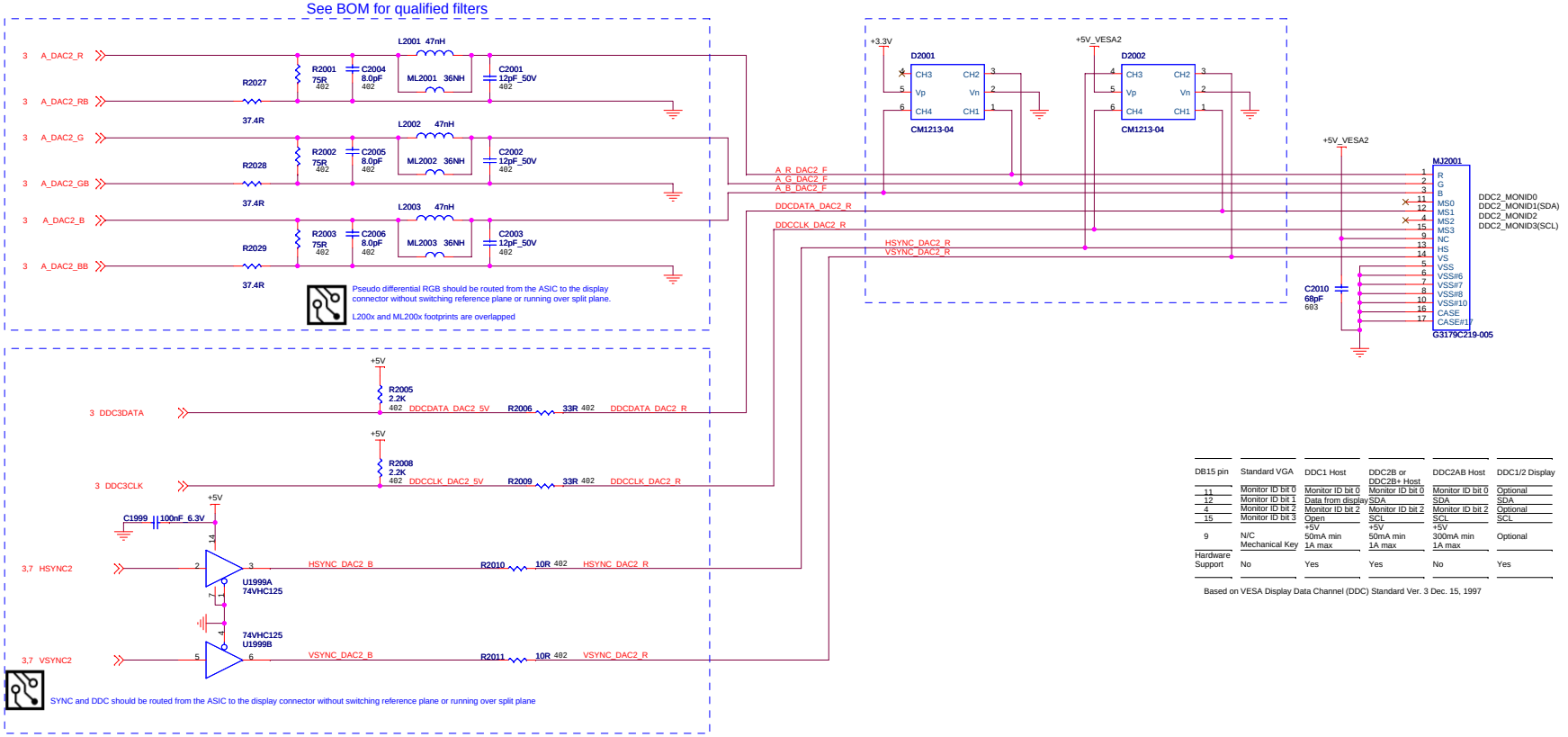
See BOM for qualified filters



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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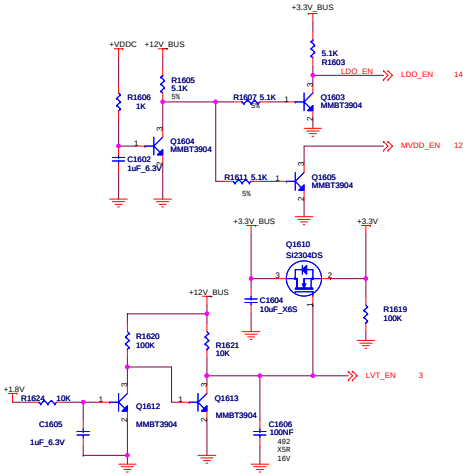
See BOM for qualified config.

See BOM for qualified config.

Power up Sequencing



Phase Control Support

Phase Control Support

AUX plug Enforcment option (BUO not for production)

AUX plug Enforcment option (BUO not for production)

12V AUX Power up Fault Support

12V AUX Power up Fault Support

Single GPIO detection method only

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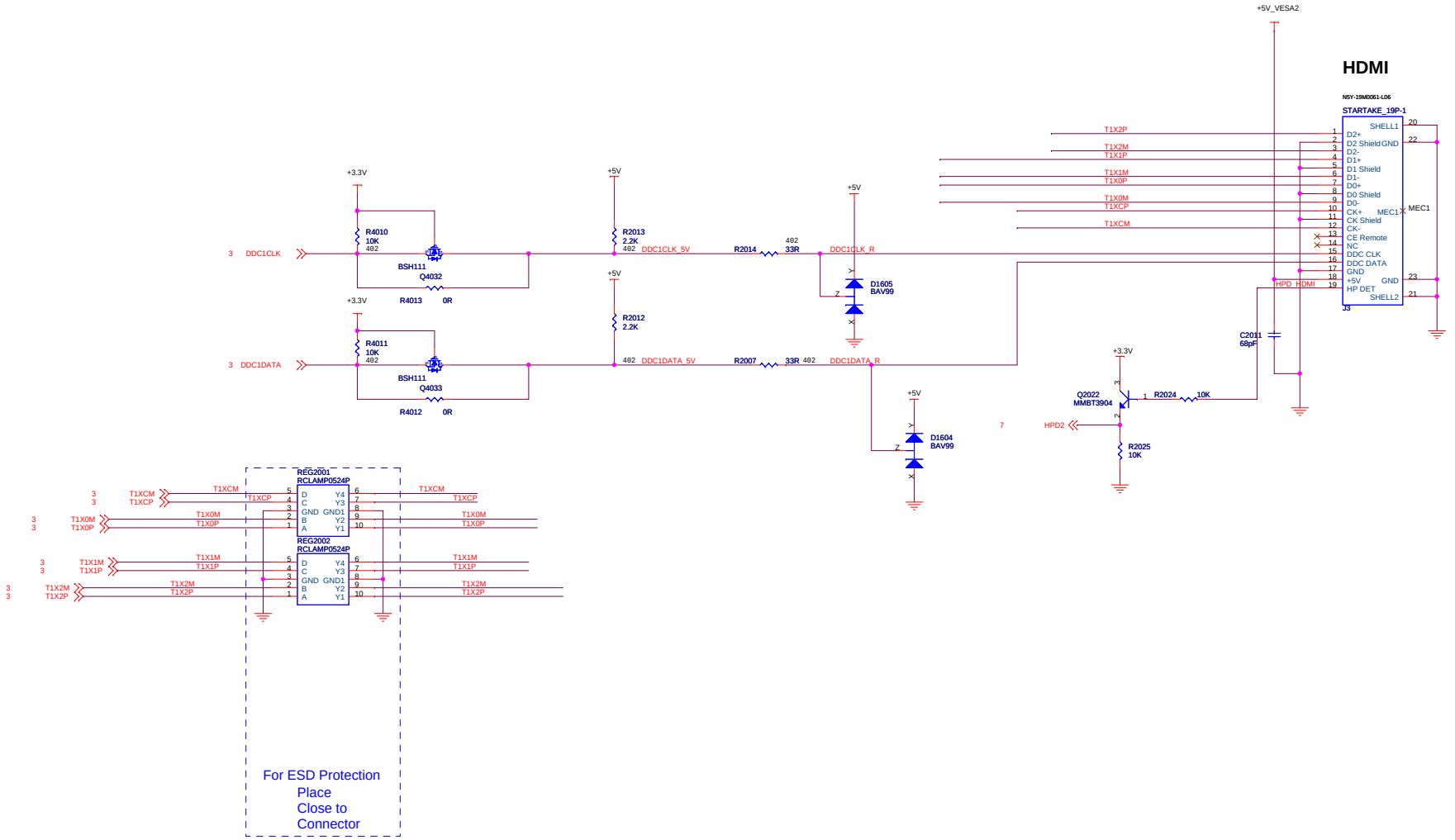

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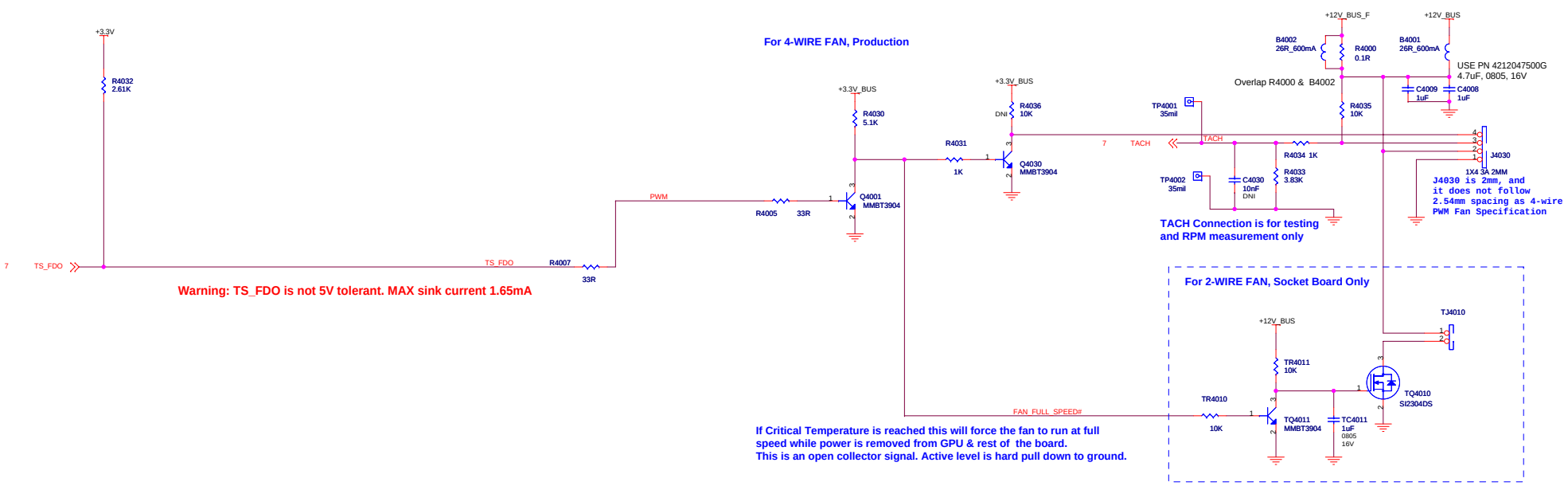

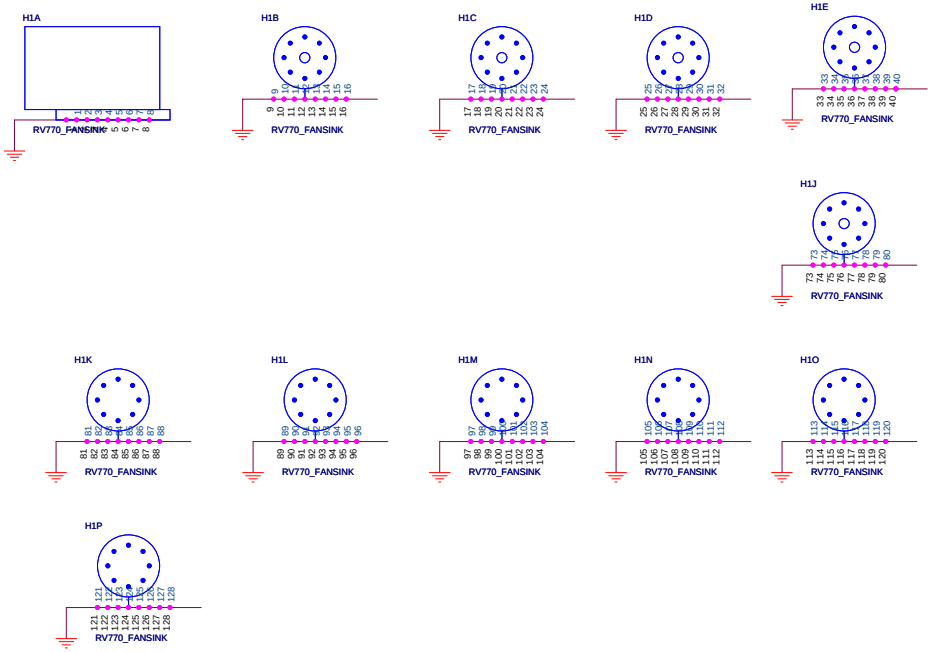

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SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET DUAL
80200388B0G

SCREW5
SCREW
SCREW

BKT1: DS, DVI - DIN - DVI

FAN
Socket_RV770

PCB
PCB
V174-0A

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM5 SW_FB
FM4 SW_FB
FM6 SW_FB

J11 X_PIN1*2 GND
J12 X_PIN1*2 GND
J13 X_PIN1*2 GND
J14 3 1 4 2 impedence GND GND

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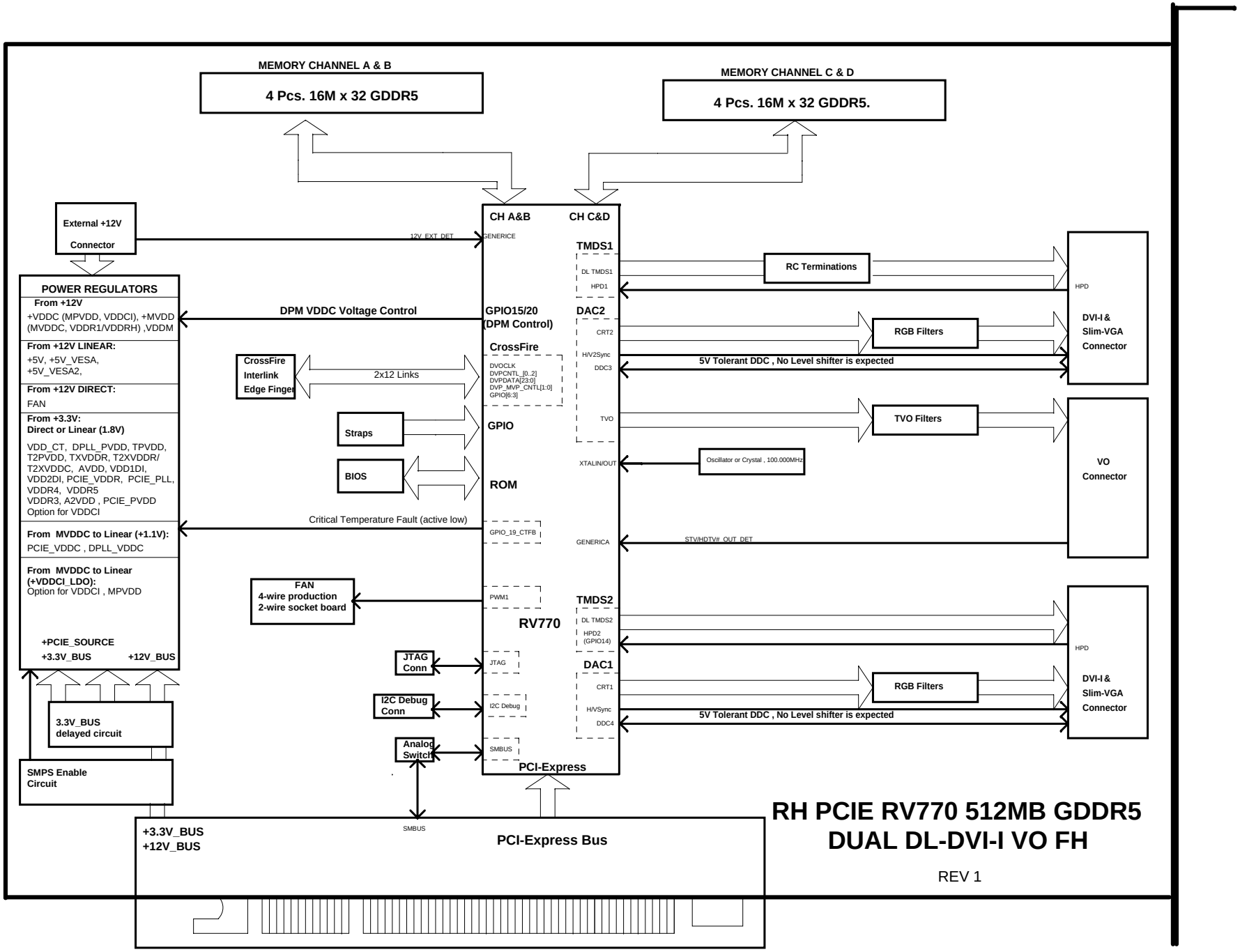
Title	Schematic No.	Date:
RH RV770 GDDR5 DVI-I VO DVI-I FH	105-B507xx-11	Wednesday, December 10, 2008

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	08/01/04	Initial design for B507 based on B500 board with display chanaged to DVI VO- DVI
1	10	08/05/05	Based on B507-00 PCB with the following changes: 1. Spread Spectrum changed to MAXIM- pg.7 2. Add second 12V AUX power supply - pg.17 3. Add temperature monitor for VDDC regulator - pg.17 4. Add 12V_BUS & 12V_EXT input switch circuit - pg.17
2	11	08/07/21	08/07/21
V174-0A	0A	08/11/04	**1.Page1 Remove TSW1** **2.Page3 Remove TX3,TX4,TX5 ,Enable DDC1 and Add CLK GEN** **3.Page7 Close GPIO5,15,18,19,20,24~28, GENERICA** **4.Page11 Change VDDC POWER solution to UP6206** **5.Page12 Change +MVDDQ POWER solution to UP6101** **6.Page13 Combine +MVDDC with +MVDDQ in same circuit** **7.Page14 Change +5V circuit** **8.Page16 Del DVI Connector** **9.Page17 Del AUX Hot Plug/ Unplug Fault supprt, 12V_BUS & 12V_EXT Input Switch Circuit** **10.Page18 Add HDMI Connector** **11.Page19 Del U4001**
	10	08/12/10	**1.Page11 Change VDDC output chock footprint** **2.Page11 Change U507 VCC conenct to 12V** **3.Page12 Change MVDD output chock footprint.**



RH PCIE RV770 512MB GDDR5
DUAL DL-DVI-I VO FH

REV 1

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Date: Wednesday, December 10, 2008	Rev 2
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