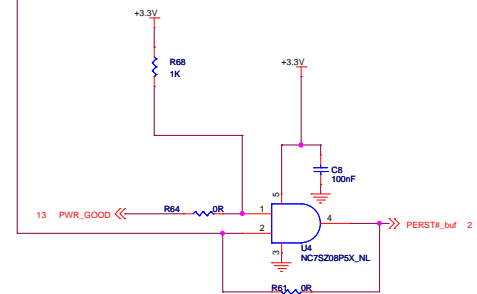
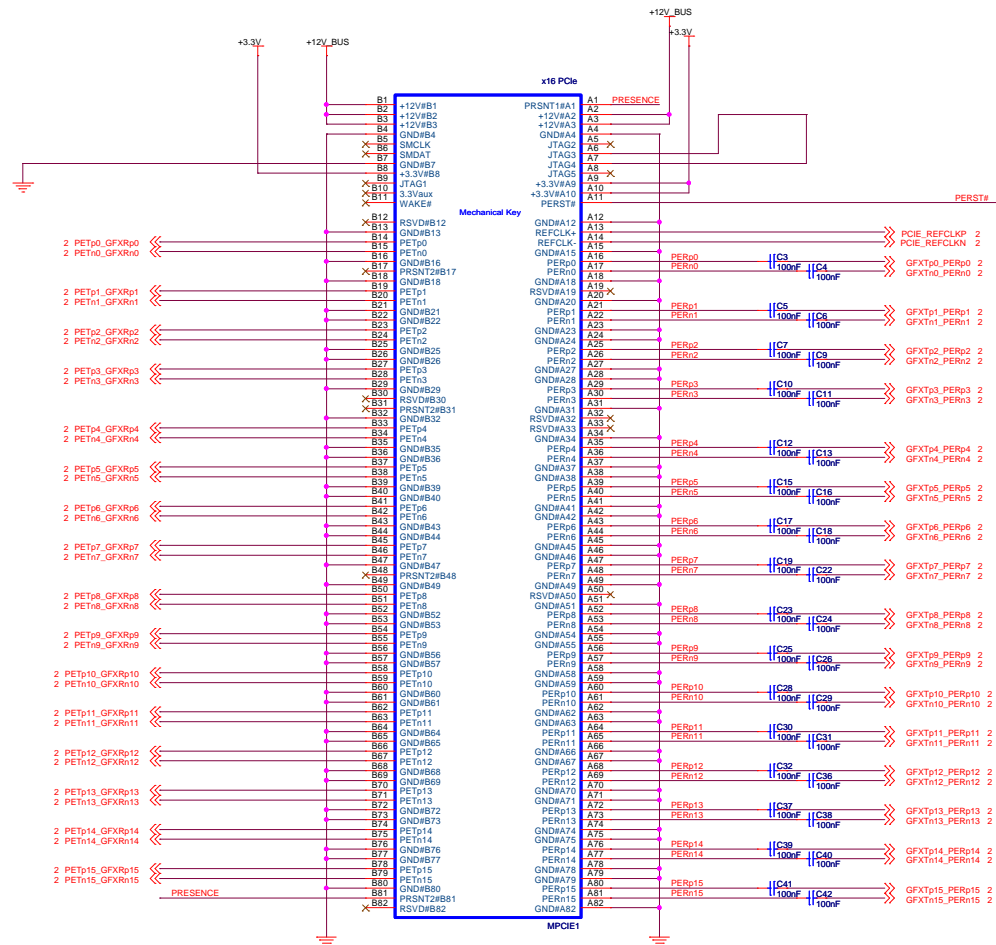
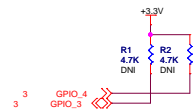


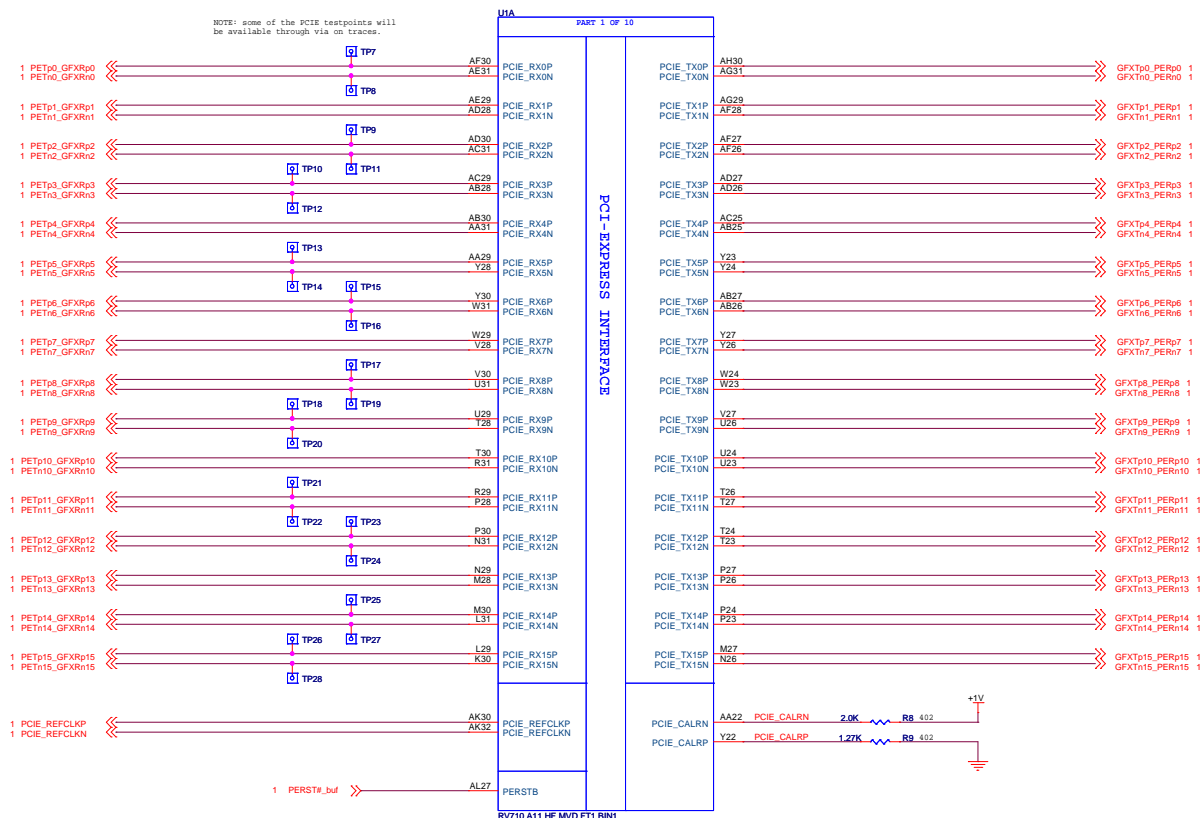


## PCI-EXPRESS EDGE CONNECTOR

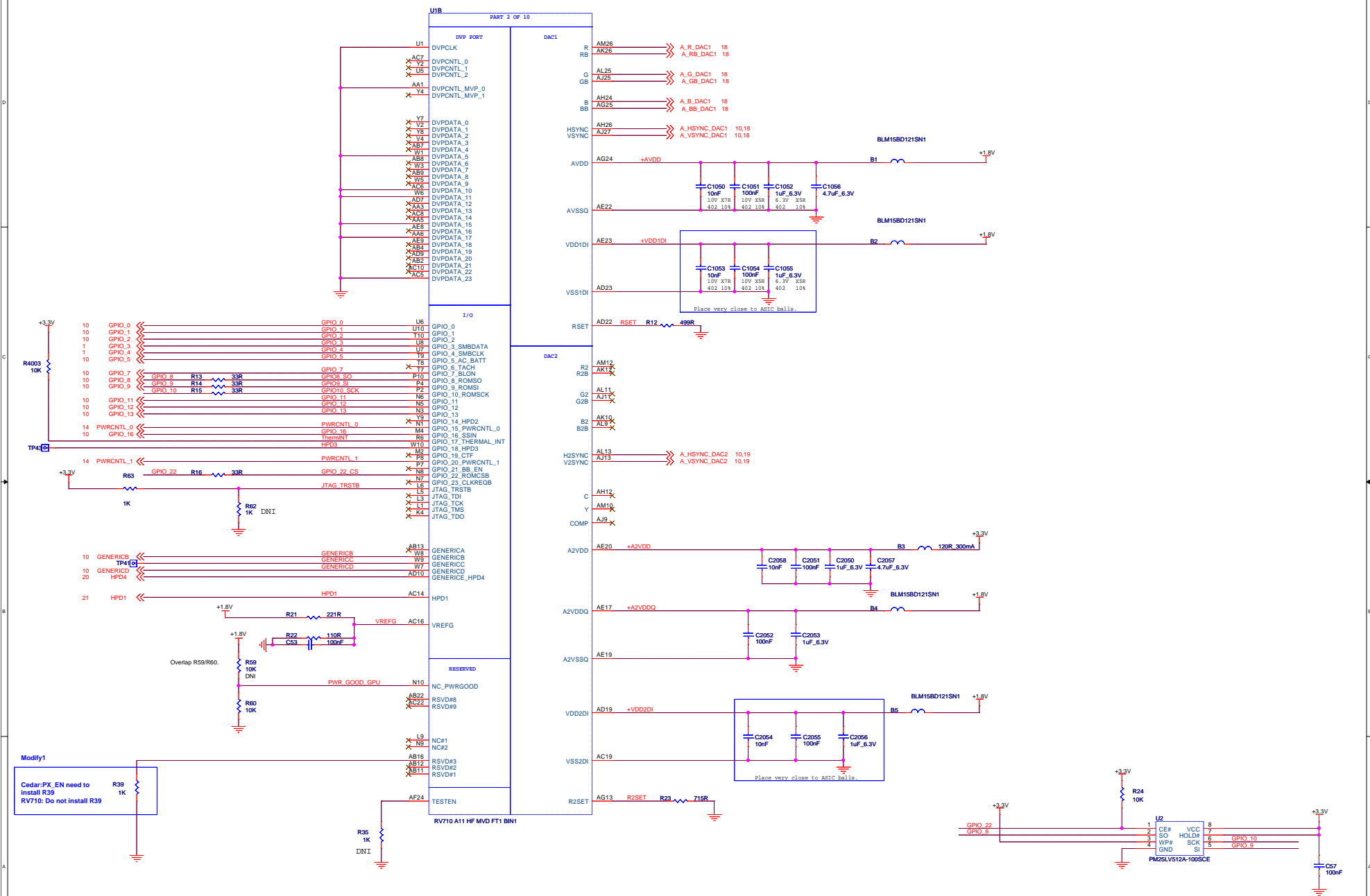



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

(2) RV710 PCIe Interface

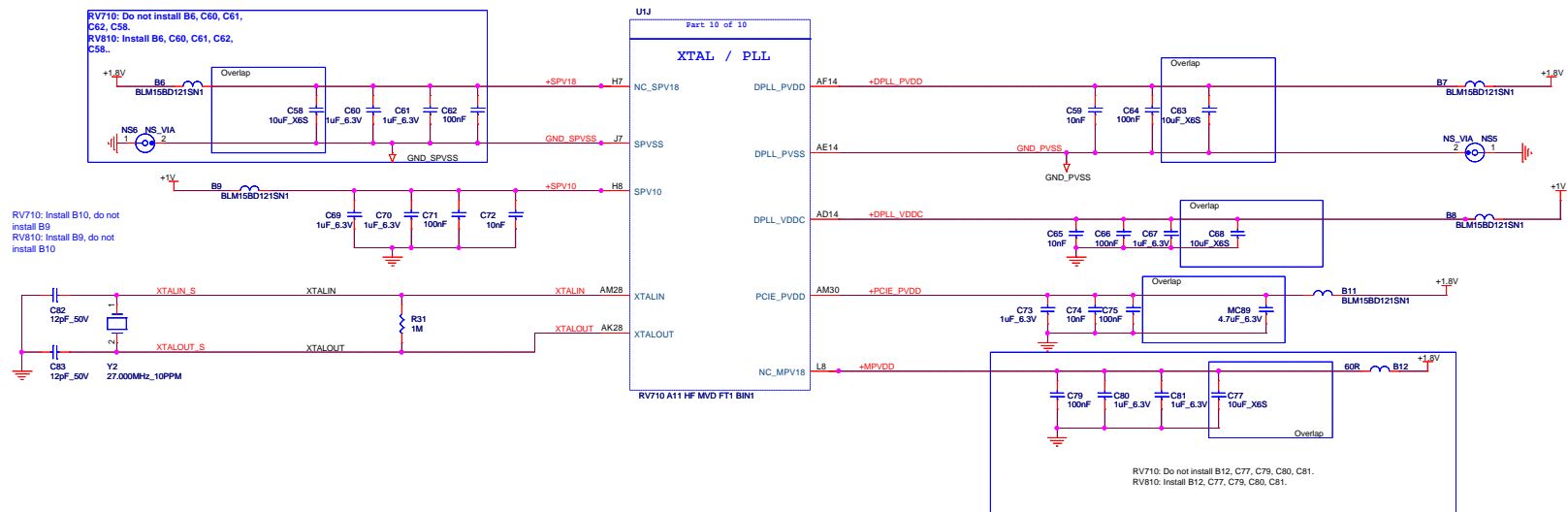


**(3) RV710 Main**



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	Sheet 3 of 25		
	Title RH LP RV710 DDR3 VGA (header) HDMI DVI		Doc No. 105-B890X-00B

# (04) RV710 GPIOs CF XTAL

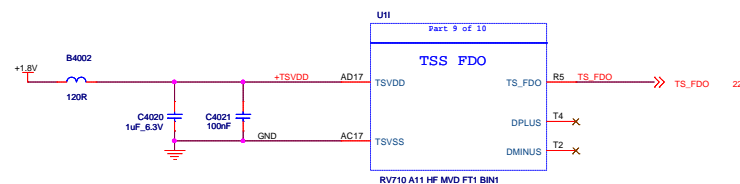
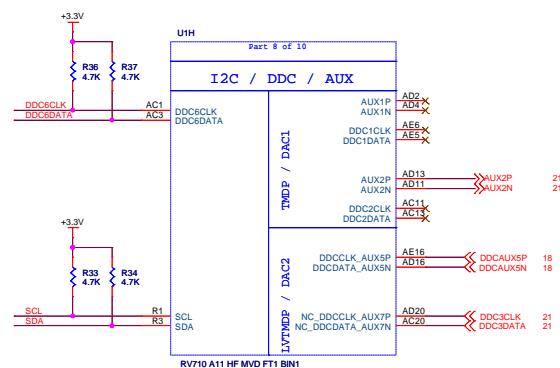


DDC6 BUS:

I2C Address	Function	Device
0x90	I2C VDDC Control	DS4402
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A

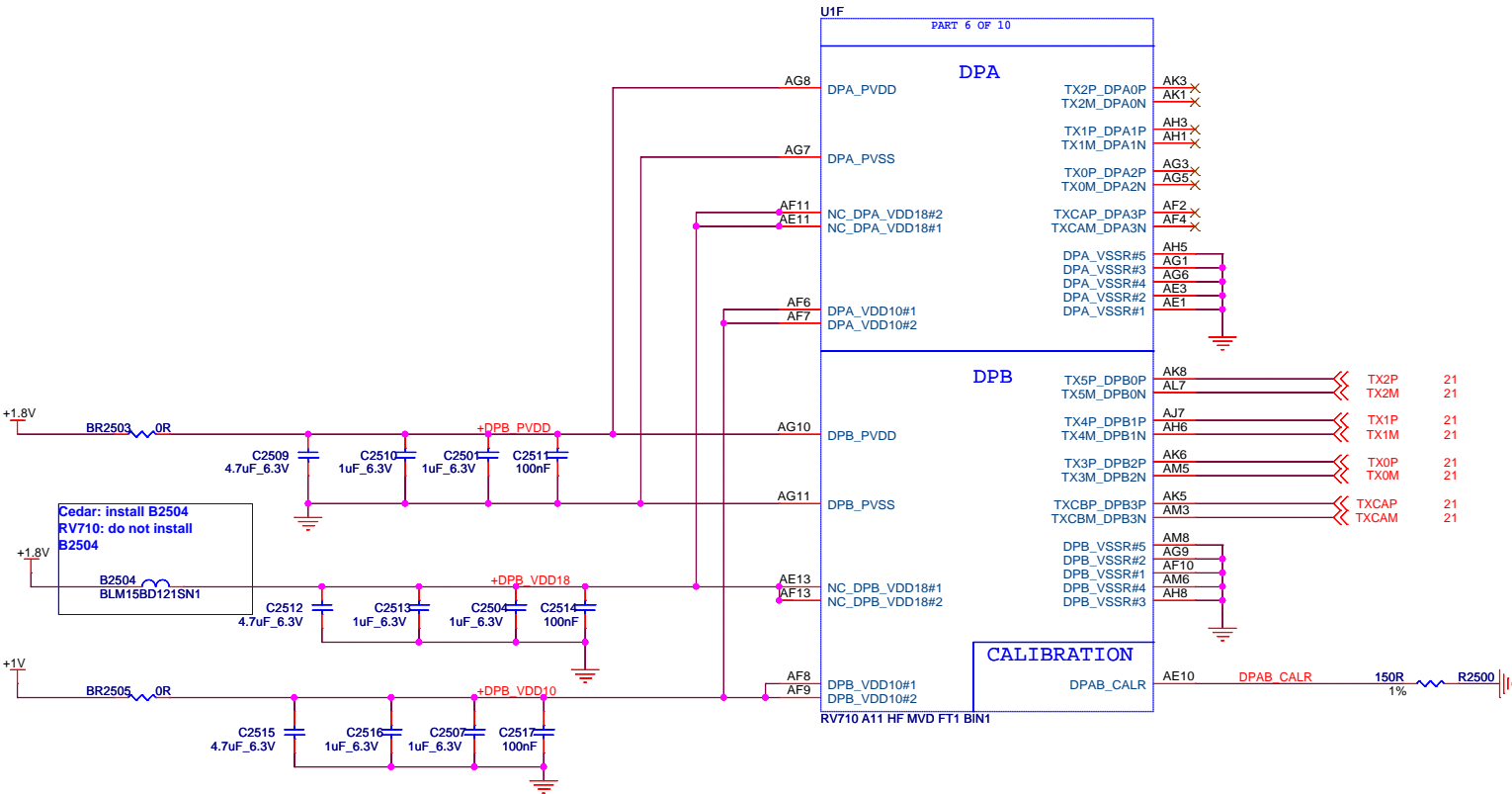


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Doc No: 105-B890XX-008

(05) RV710 TMDP A&B

TMDP INTERFACE



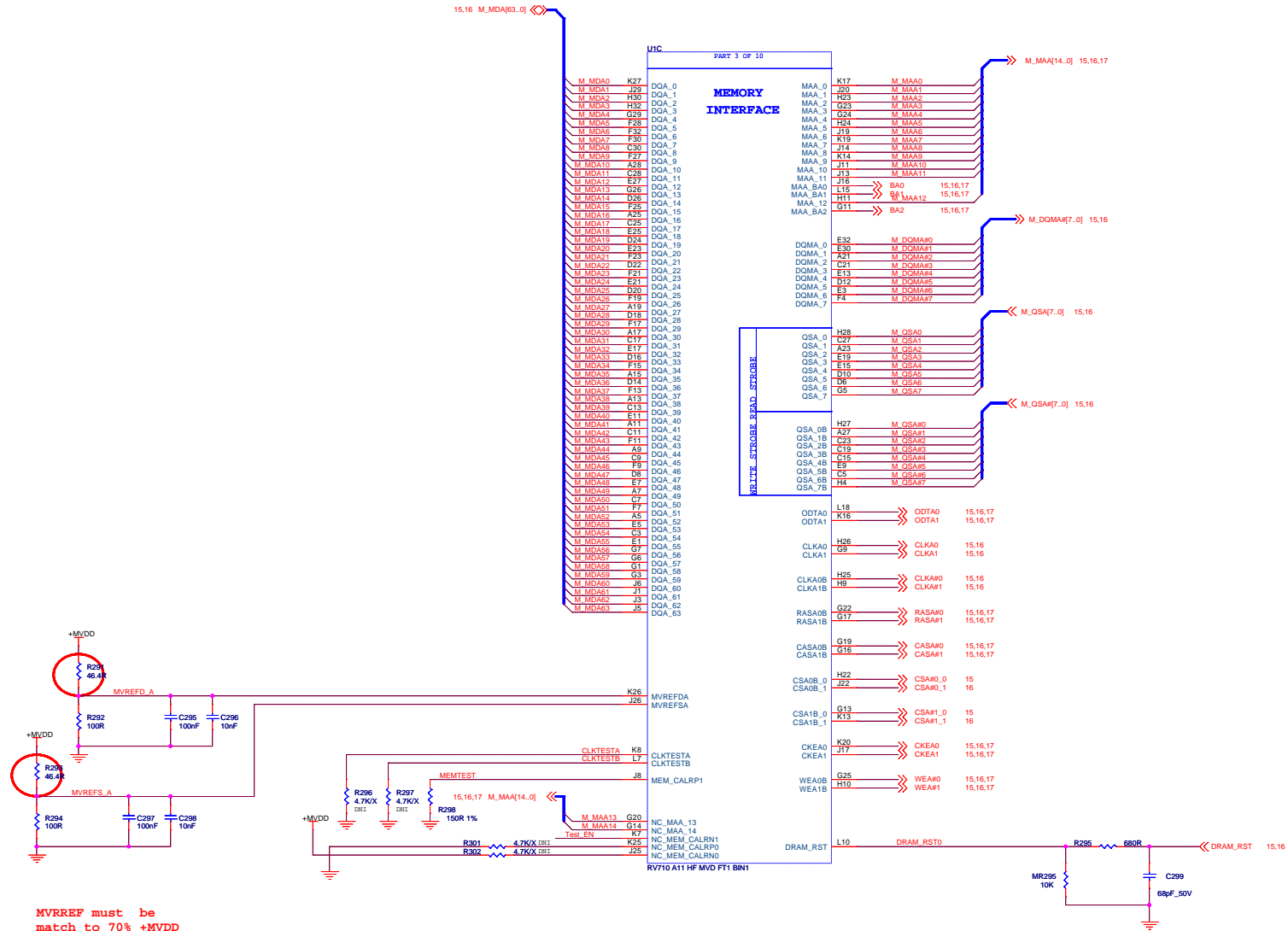
## LVTMDP INTERFACE



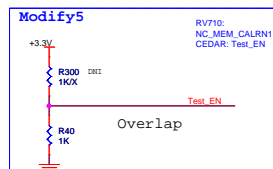
Title		Doc No.
RH LP RV710 DDR3 VGA (header) HDMI DVI		105-B890XX-00E

### (07) RV710 MEM Interface Ch A

## MEMORY INTERFACE

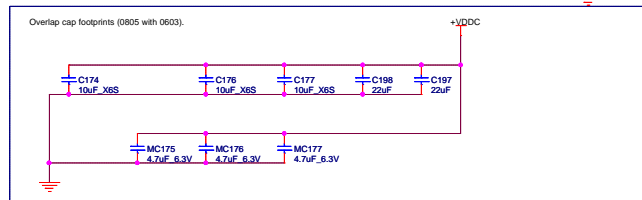
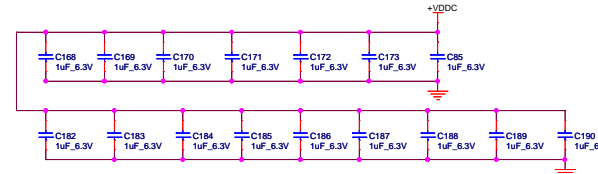
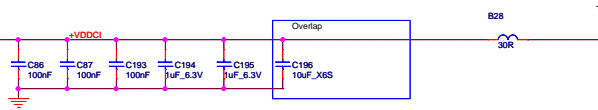
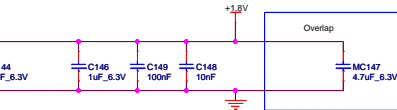
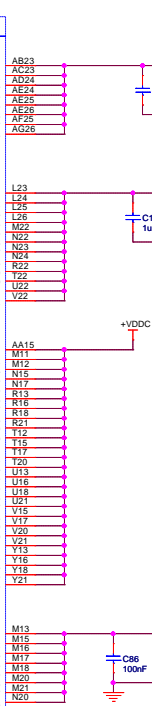
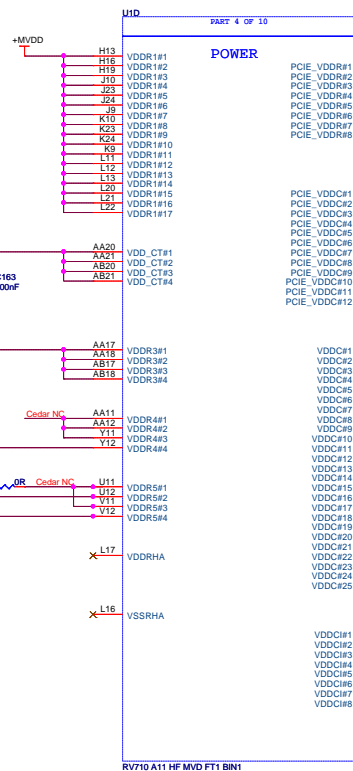
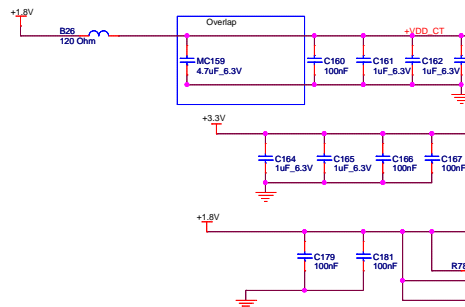
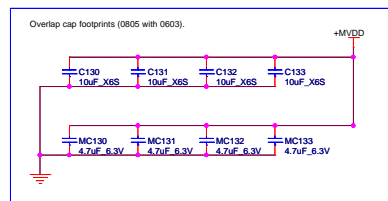


DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R



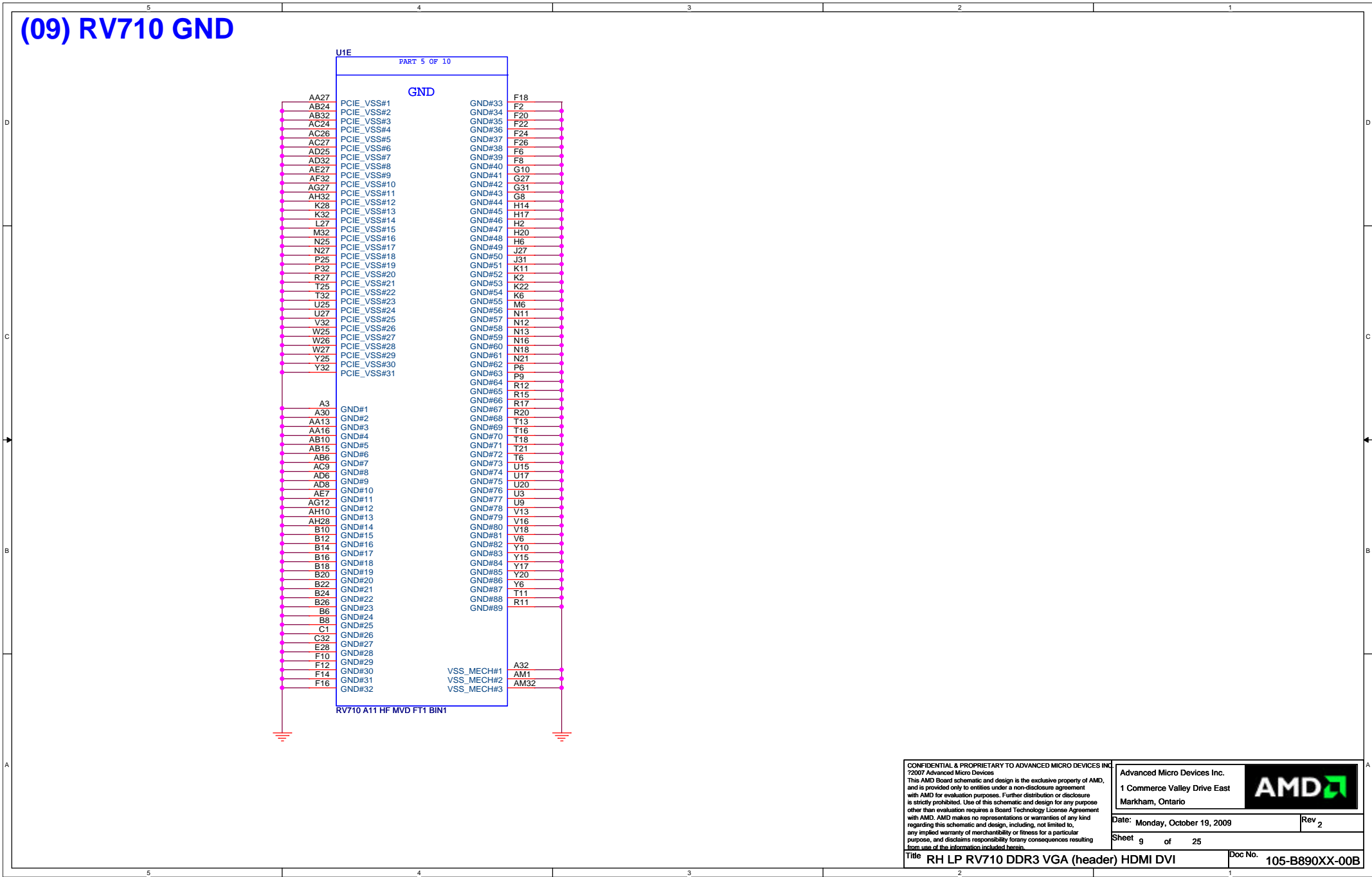
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## (08) RV710 Power





(09) RV710 GND



(10) RV710 STRAPS

PIN BASED STRAPS

DNI	+3.3V	DNI	R43	10K	A_VSYNC_DAC2	3,19	VIP_DEVICE_STRAP_EN 0: Driver would ignore the value sampled on VHAD_0 during reset 1: Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no).
		DNI	R44	10K	GPIO_9	3	VGA DISABLE : 1 for disable (set to 0 for normal operation)
DNI			R45	10K	GPIO_0	3	GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) 0 : 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
DNI			R46	10K	GPIO_1	3	GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)
DNI			R47	10K	GPIO_2	3	GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable) 0 : Default. (Driver Controlled Gen2) 1 : Strap Controlled Gen2
DNI			R48	10K	GPIO_11	3	GPIO(13, 12, 11) - CONFIG[2..0] 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)
DNI		DNI	R49	10K	GPIO_13	3	
DNI		DNI	R50	10K	GPIO_12	3	
DNI			R51	10K	A_VSYNC_DAC1	3,18	AUD[0]
			R52	10K	A_HSYNC_DAC1	3,18	AUD[1]
		DNI	R53	10K	GPIO_8	3	BIF_CLK_PM_EN 0 - Disable CLKREQ# power management capability 1 - Enable CLKREQ# power management capability
			R54	10K	GPIO_5	3	[GPIO_5 : GPIO_16]
		DNI	R55	10K	GPIO_16	3	Quimonda [0:0] Hynix [0:1] Samsung [1:0]
		DNI	R56	10K	A_HSYNC_DAC2	3,19	RESERVED :Internal use only. Other logic must not affect this signal during RESET.
	NTSC		R57	10K	GPIO_7	3	TV OUT STANDARD 0 - PAL TVO 1 - NTSC TVO
DNI			R70	10K	GENERICB	3	GenericB and GenericD will be used for additional memory vendor straps.
DNI			R71	10K	GENERICD	3	

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(11) VDDC

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Title: RH LP RV710 DDR3 VGA (header) HDMI DVI Doc No: 105-B890XX-00B

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Date: Wednesday, October 21, 2009		Rev 2	
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(r) HDMI DVI		Doc No. 105-B890XX-00B	

[illegible]

**(12) MVDD**

+12V\_BUS

Vin Ims = 5.8A @ 1.8V/15A

Vout ripple = 5.3A @ 300kHz

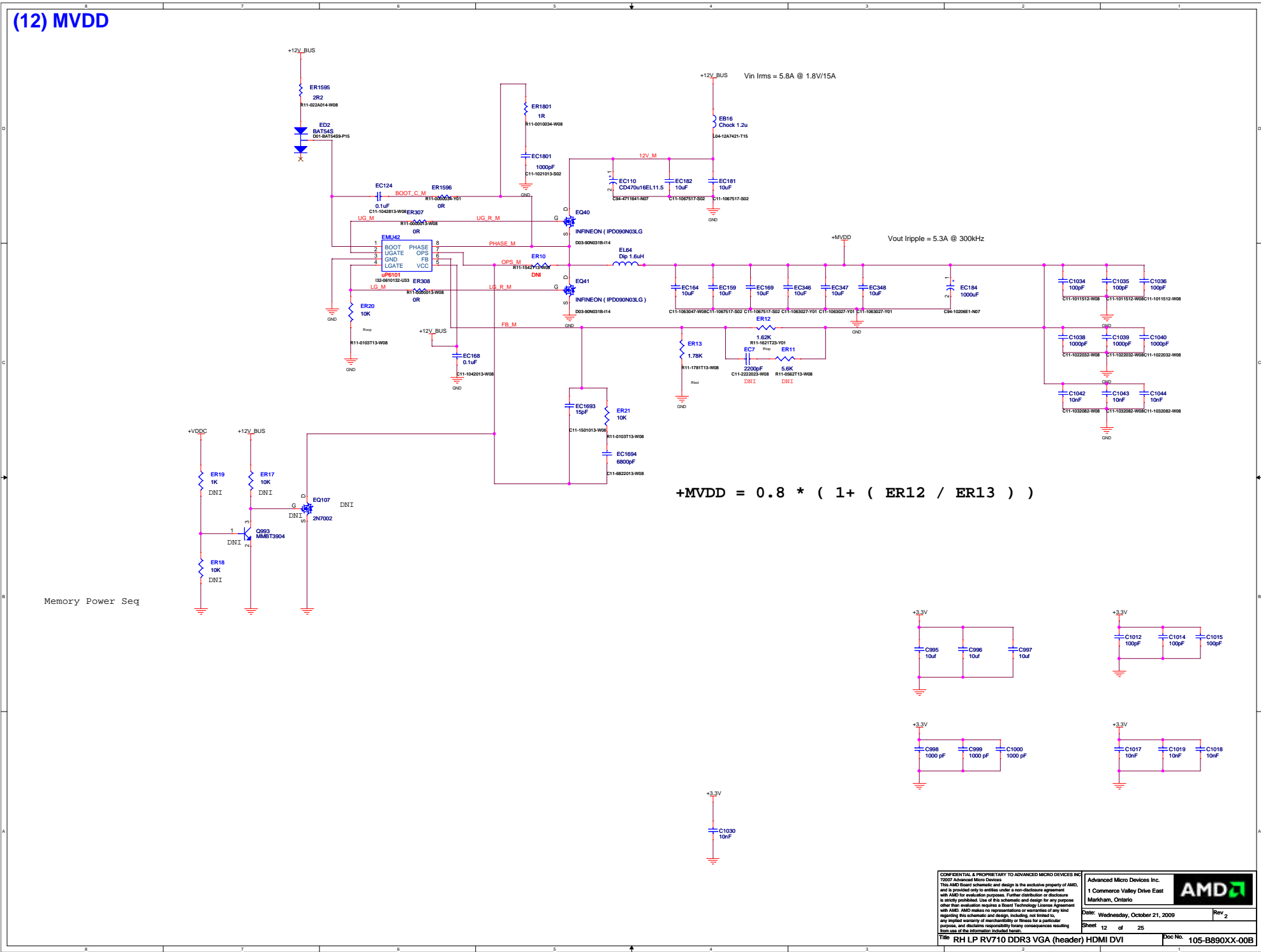
$$+MVDD = 0.8 * \left( 1 + \left( \frac{ER12}{ER13} \right) \right)$$

Memory Power Seq

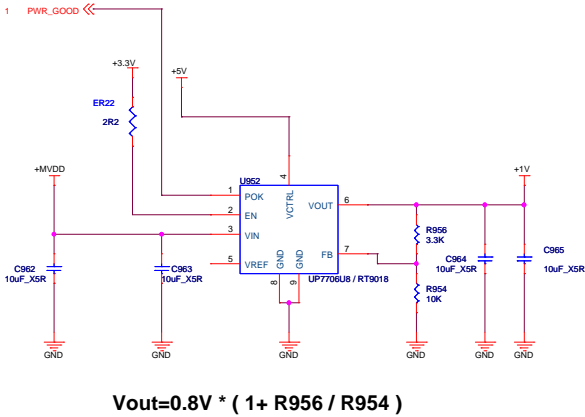
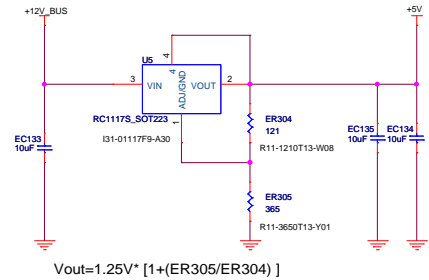
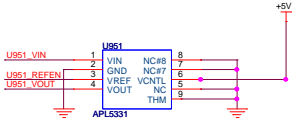
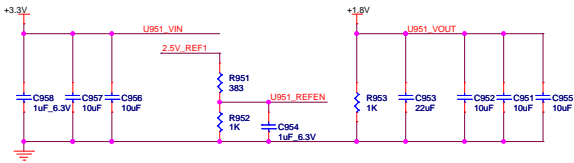
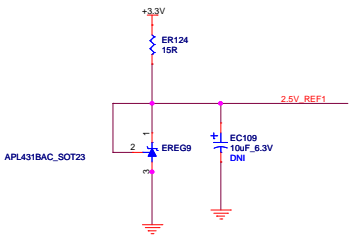
AMD logo

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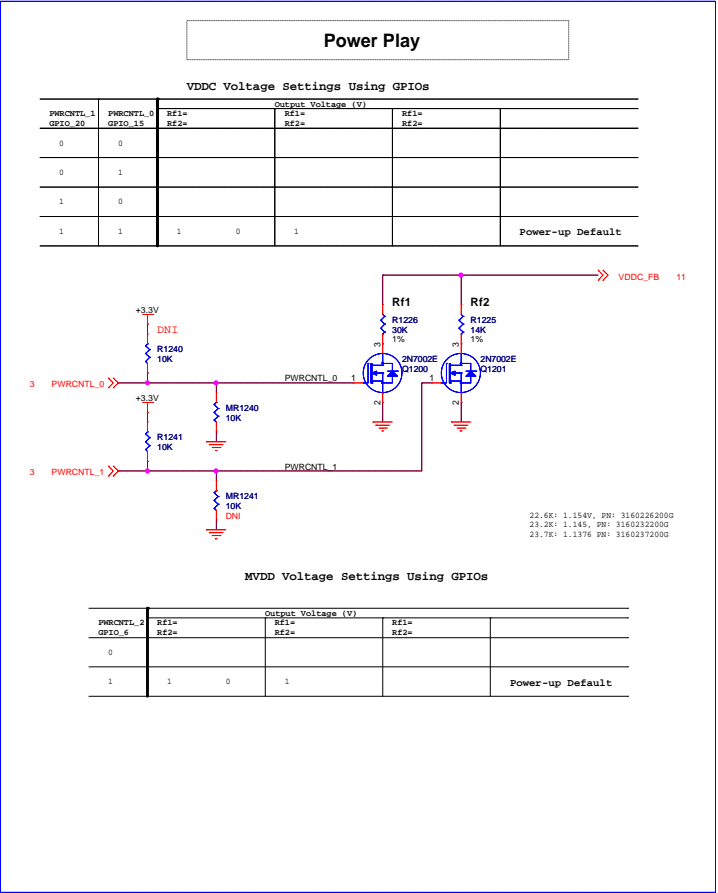
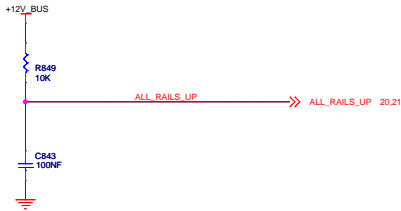
Title RH LP RV710 DDR3 VGA (header) HDMI DVI Doc No. 105-B890XX-00B



(13) Linear Regulators

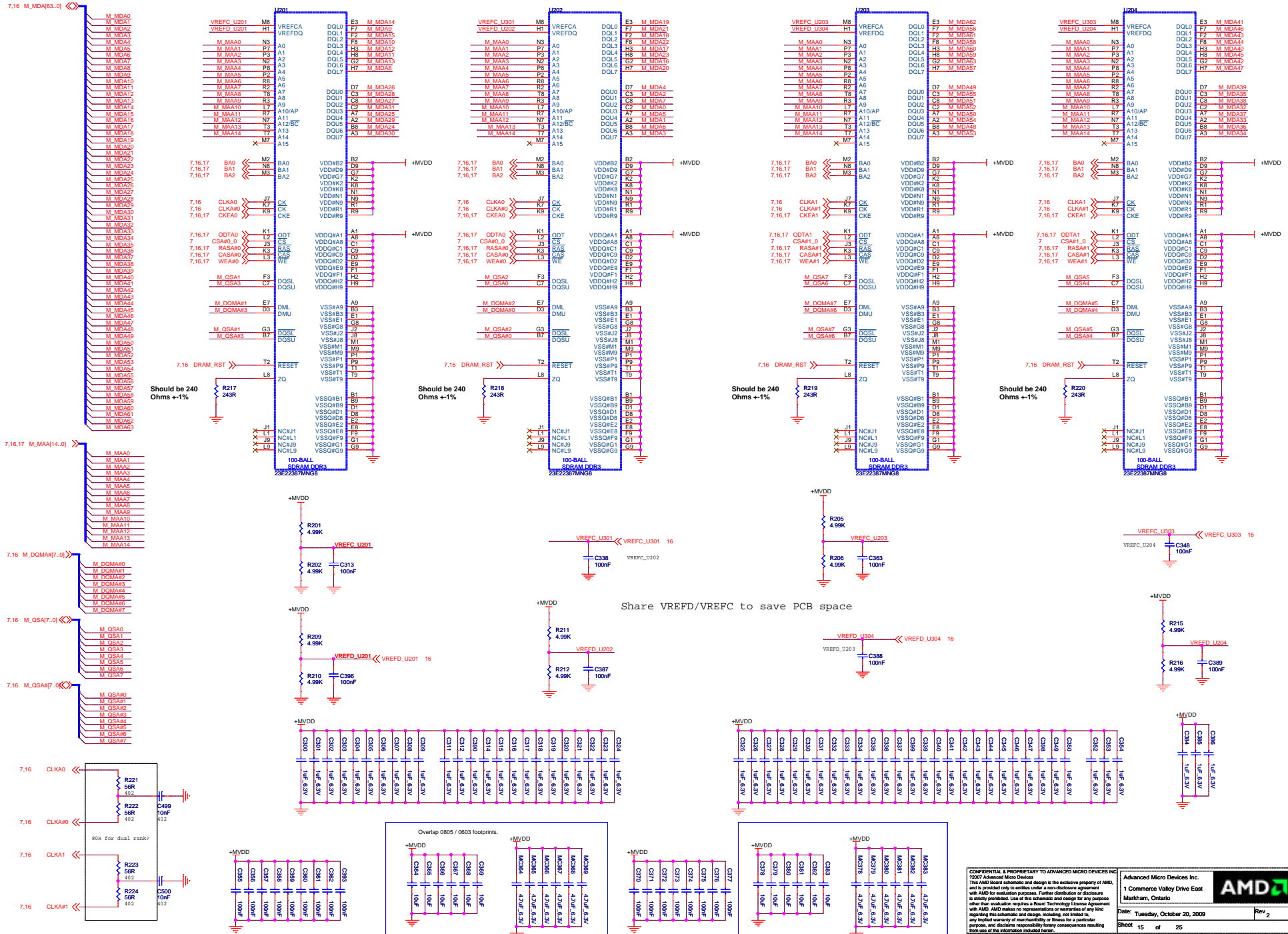


(14) Power Management

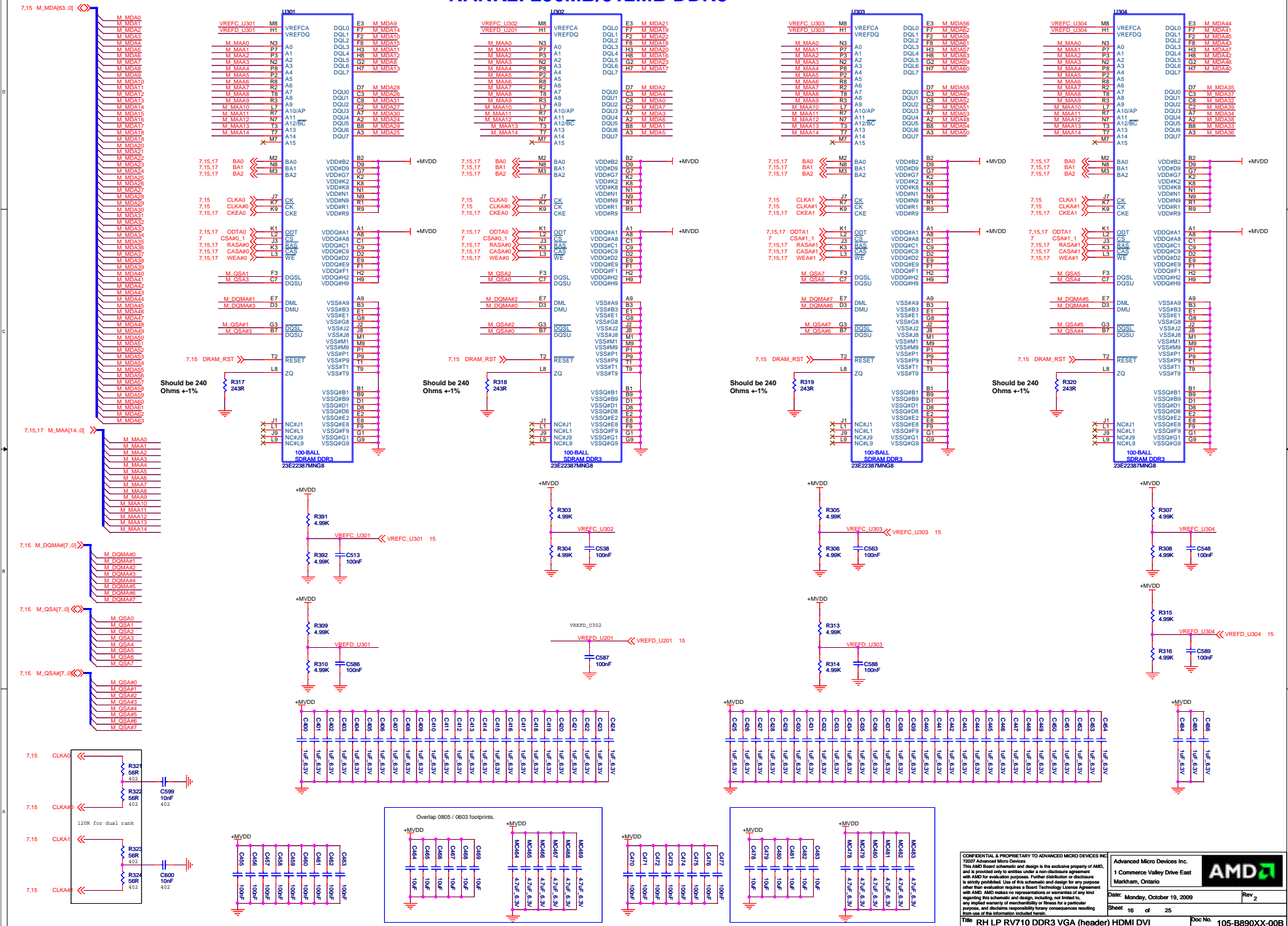


# (15) DDR3 RANK1

## RANK1: 256MB/512MB DDR3

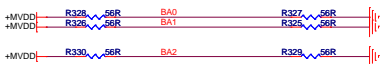
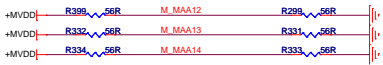
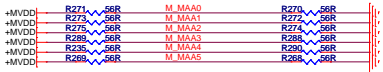
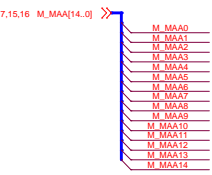
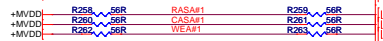
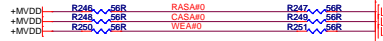
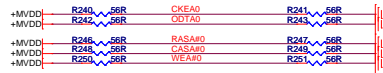


**RANK2: 256MB/512MB DDR3**





(17) DDR3 Termination

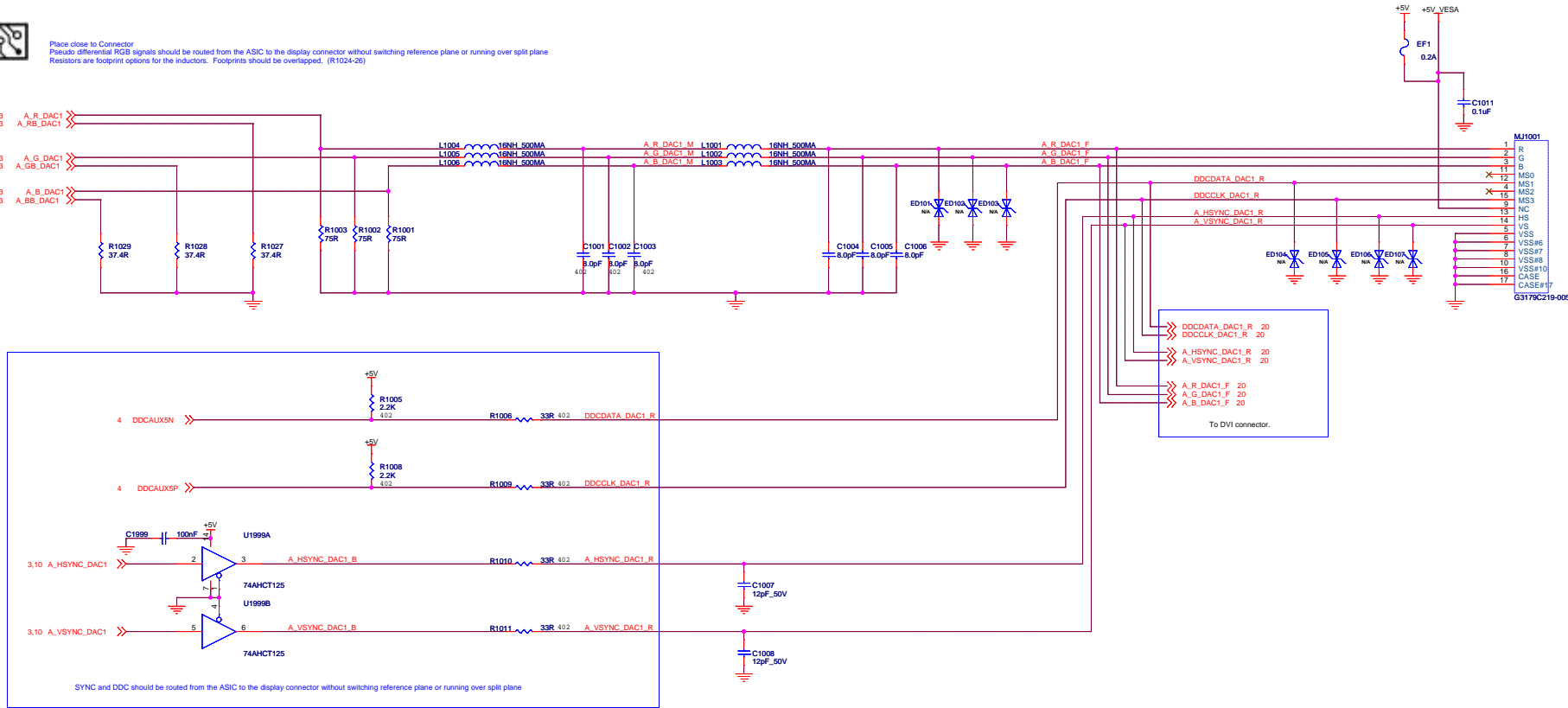


(18) DAC1 OUTPUT

DAC 1 OUTPUT



Place close to Connector  
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane  
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)



(19) DAC2 OUTPUT

DAC 2 OUTPUT

Optional ESD Protection Diodes

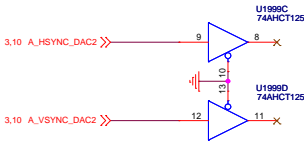
Place near D2002, D2003, D2004, D2005



Place close to Connector  
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane

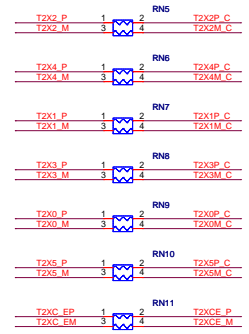
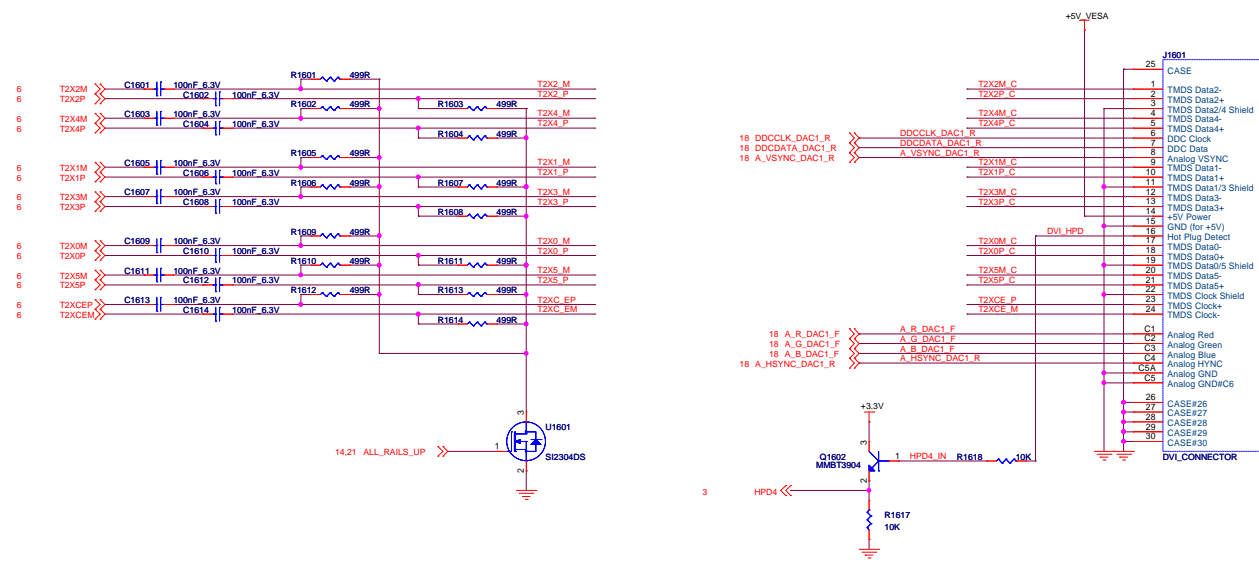
RV710: DDC2 is 5V tolerant. Do not install level shifter.  
--> Do not install R2013, R2015, Q2001, Q2002. Install R2014, R2016.  
RV810: DDC2 is NOT 5V tolerant. Install level shifter.  
--> Do not install R2014, R2016. Install R2015, R2015, Q2001, Q2002.

Remove VGA RIBBON CONNECTOR  
2009/09/23



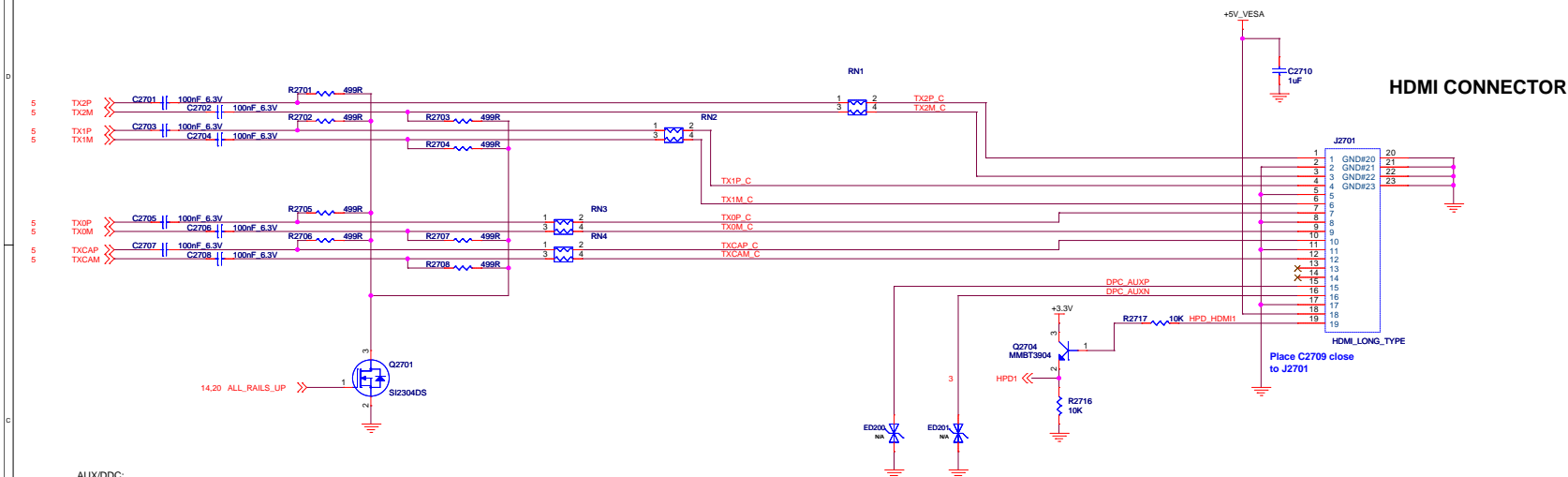
(20) DVI OUTPUT

DPE / DPF OUTPUT

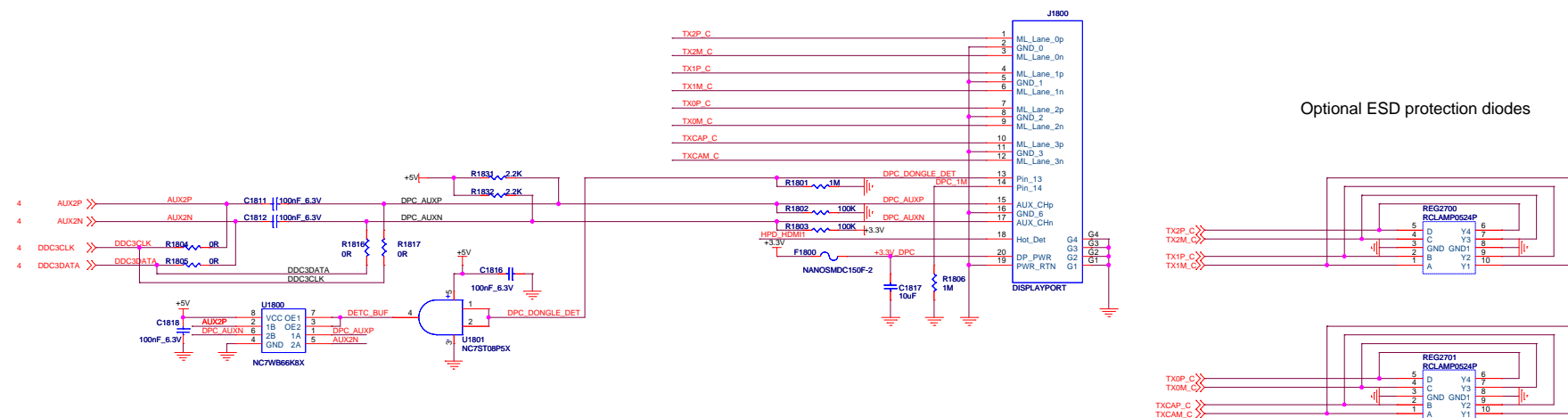


**(21) HDMI OUTPUT**

## TMDP-B OUTPUT

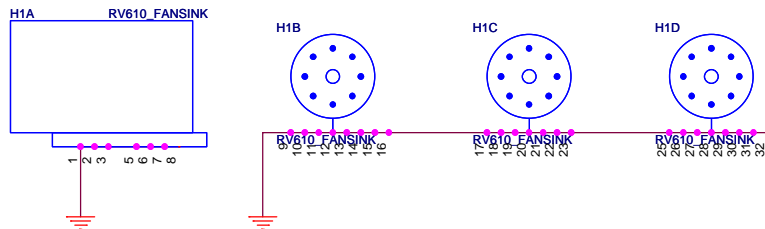


AUX/DDC:  
FOR 740/730, INSTALL OR ON ASIC-SIDE OF AC COUPLING CAPS  
ONLY;  
FOR JUNIPER, INSTALL OR ON CONNECTOR SIDE OF AC COUPLING  
CAPS ONLY;

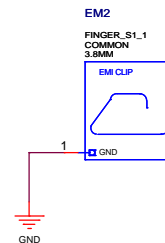
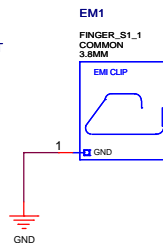
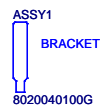
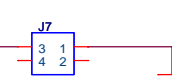
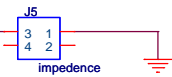
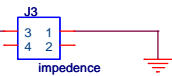
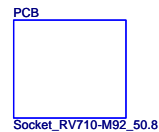
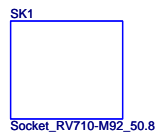


Optional ESD protection diodes





7120036200G



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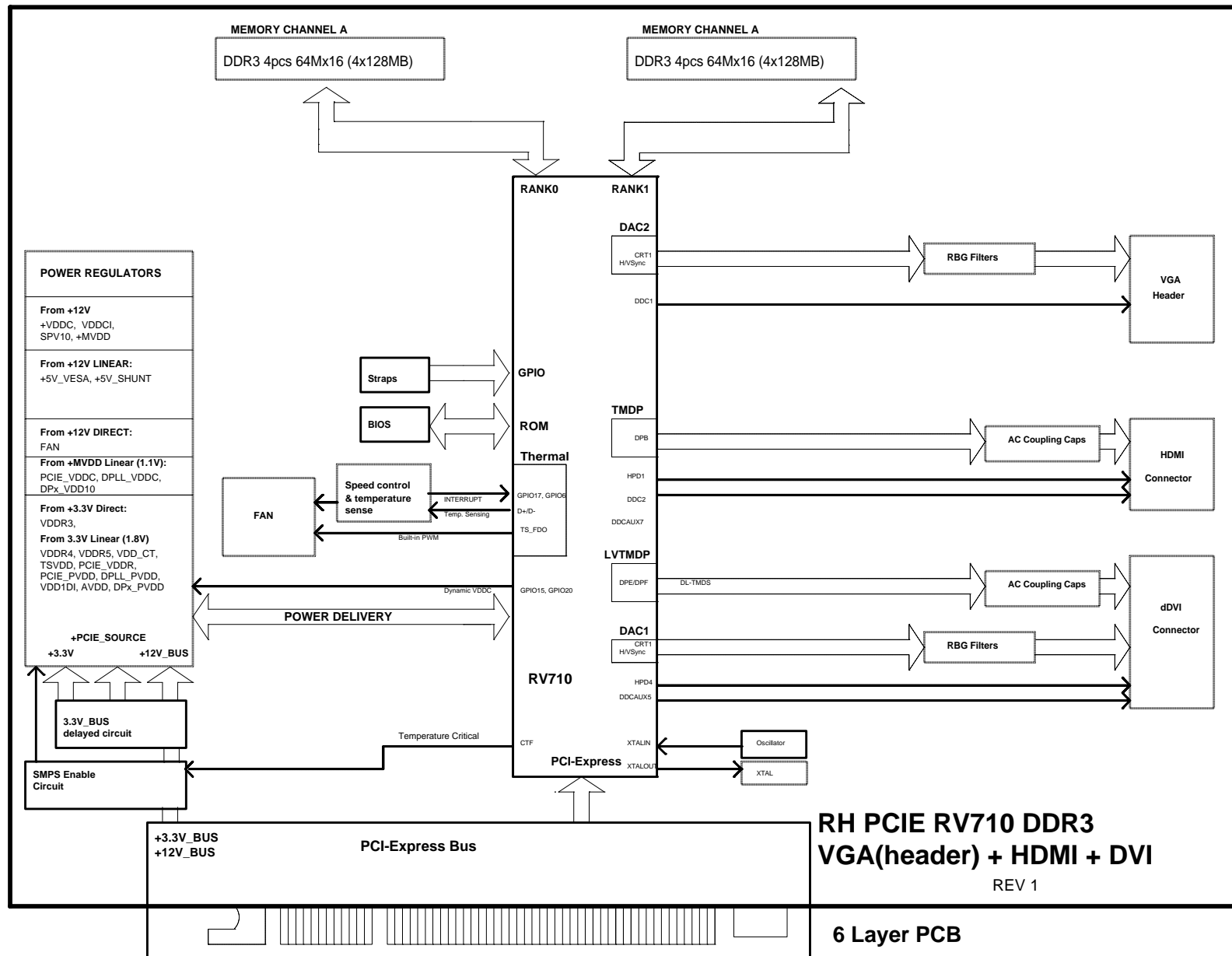
Date: Tuesday, October 20, 2009

Rev 2


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Title RH LP RV710 DDR3 VGA (header) HDMI DVI

Doc No. 105-B890XX-00B





5					4					3					2					1				
					Title RH LP RV710 DDR3 VGA (header) HDMI DVI										Schematic No. 105-B890XX-00B					Date: Monday, October 19, 2009				
					REVISION HISTORY										NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI  ş? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.									
Sch Rev		PCB Rev		Date		RV710 ENGINEERING BOARD REVISION DESCRIPTION																		
0		00A		2008.12.30		INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.																		
1		00B		2009.01.22		Sch no change. just modify HDMI connnecro location on PCB																		
5					4					3					2					1				