

31P141, NV31, 4(8,16)Mx16, 64(128,256)MB, VIDEO IN/OUT, DVI-I, VGA

Page Overview

1 31P141 OVERVIEW

2 NV31 AGP Section and AGP connector

3 NV31 FRAMEBUFFER Interface

4 MEMORY Partition A Bits 0..31

5 MEMORY Partition A Bits 31..63

6 MEMORY Partition B Bits 0..31

7 MEMORY Partition B Bits 31..63

8 NV31 DACA, DACB output, SYNC amplifier

PLL Section

9 PRIMARY DISPLAY (DACA) Filter and DB15 Connector

10 SECONDARY DISPLAY (DACB)

DACB Multiplexer Filter long DB15 Connector

11 NV31 INTERNAL TMDS Transmitter

TMDS Backdrive circuit

Hotplug detection and DVI-I Connector

12 VIDEO CAPTURE Philips 7114 I/O

13 VIDEO IN/OUT, Filter and Connector

VIDEO INTERNAL Input

14 VIP, DVO, GPIO Section

15 BIOS, STRAPPS

16 POWER SUPPLY: NVVDD, FBVDDQ, A3V3, TMDS

17 POWER SUPPLY: FBVDD, DDC5V

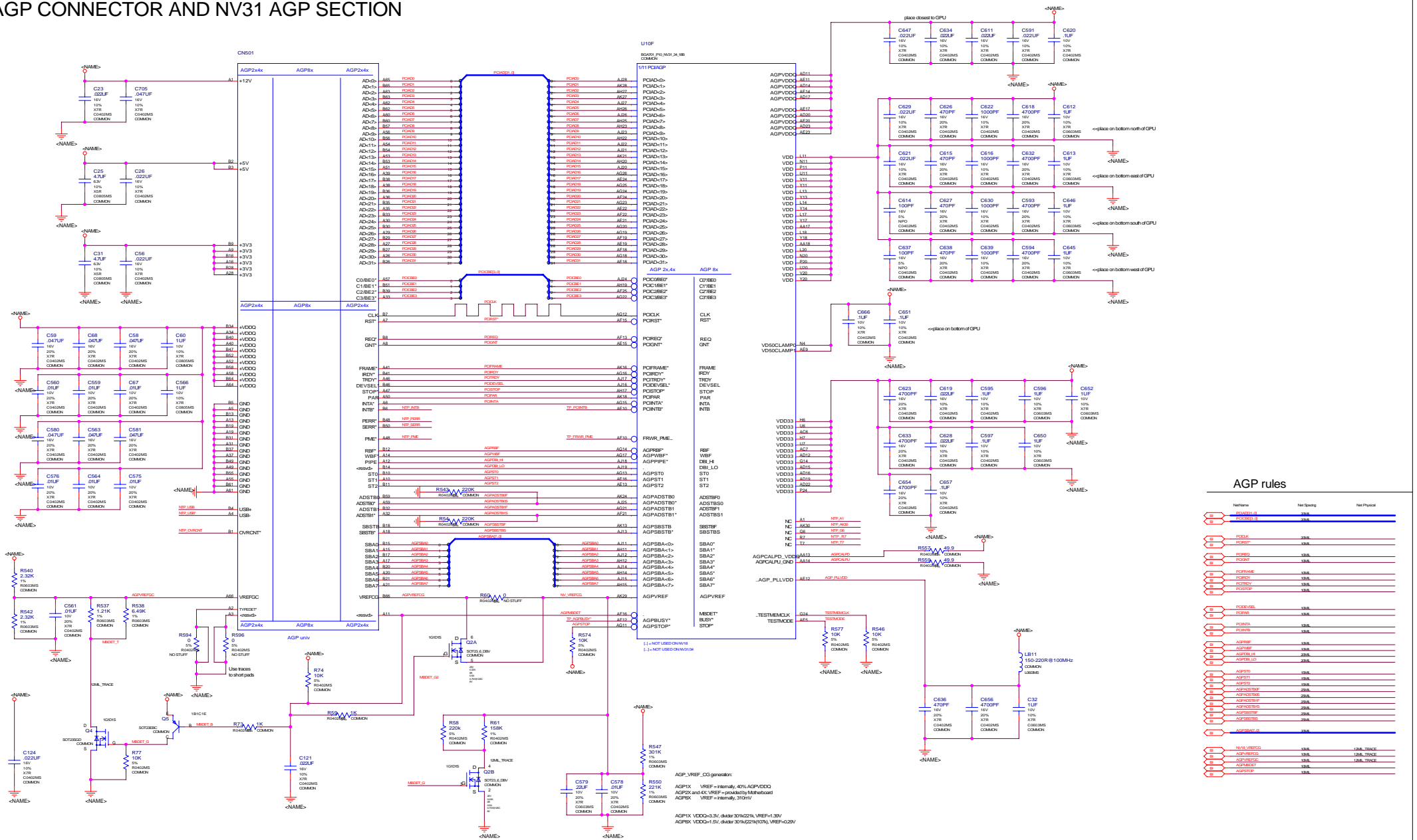
A00

HISTORY:

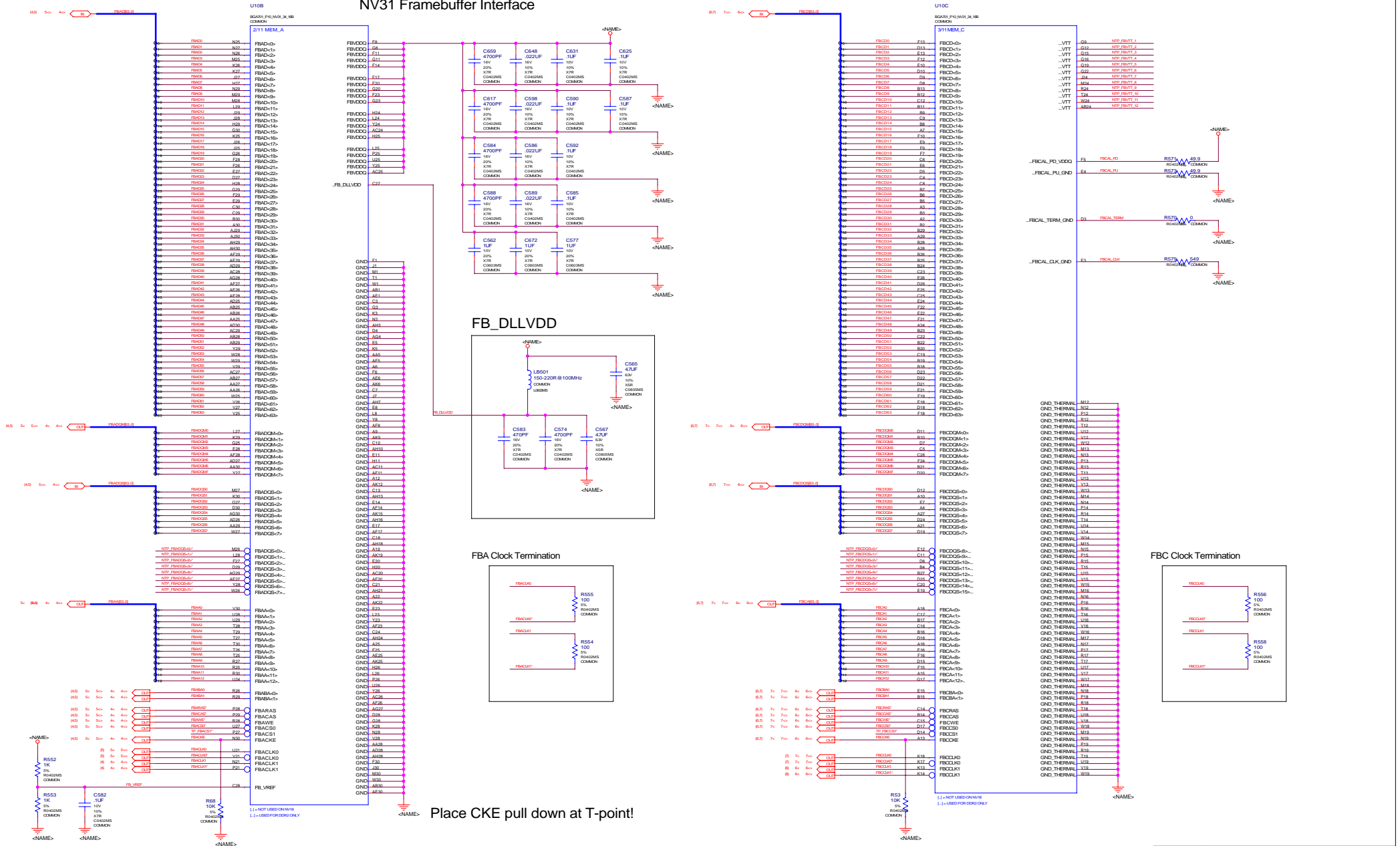
X00:	INITIAL VERSION
X01:	First Review
	Replaced series resistors in sync lines with 33ohms
	Moved clamping diodes next to GPU
	Added parallel caps to EMI filter DACB
	Removed not needed strap on SAA7114
	Connected RESET and WP of SST ROM to ROMVCC
	Added parallel ROM and Strapps
	Added FBVDD regulator
	Added STEREO glasses circuit
	Removed Decoupling CAPs on VIP VDD, covered by Caps on page 2
	Added ROM_VCC for cleaner planes
	Changed used TMDS lines of IFPA and IFPB to TP from NTP
	Changed Resistor for AGP Vref circuit to 158k
X02:	Final Review
	Added clock termination resistors
	Added net name for FBCALxxx
	Added cap on filter input for FB_DLLVDD, DACA_VDD & DACB_VDD
	Changed netnames for SAA7114 NTPs to NTP_xxx
	Added 1uF cap parallel to fan connector
	Changed all xxCALxx resistors to 50 Ohms
	Changed all FBxDQS*-<x> to NTP_FBxDQS*-<x> with NO_TEST property

602-10141-0000-000 Base Schematic

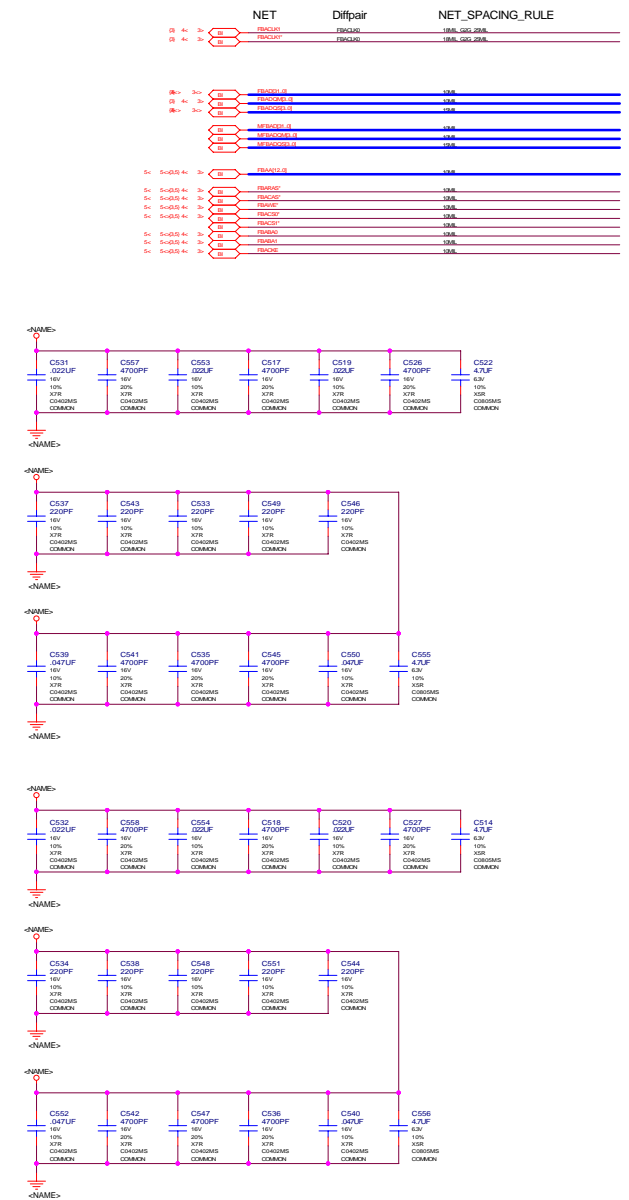
## AGP CONNECTOR AND NV31 AGP SECTION



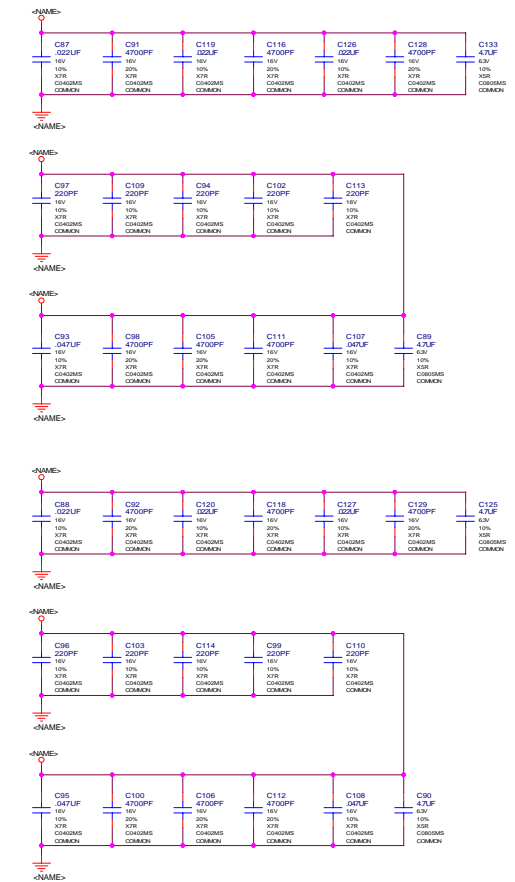
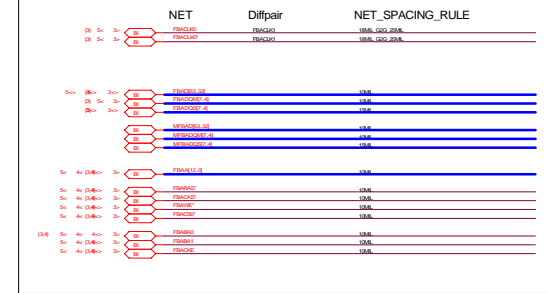
# NV31 Framebuffer Interface



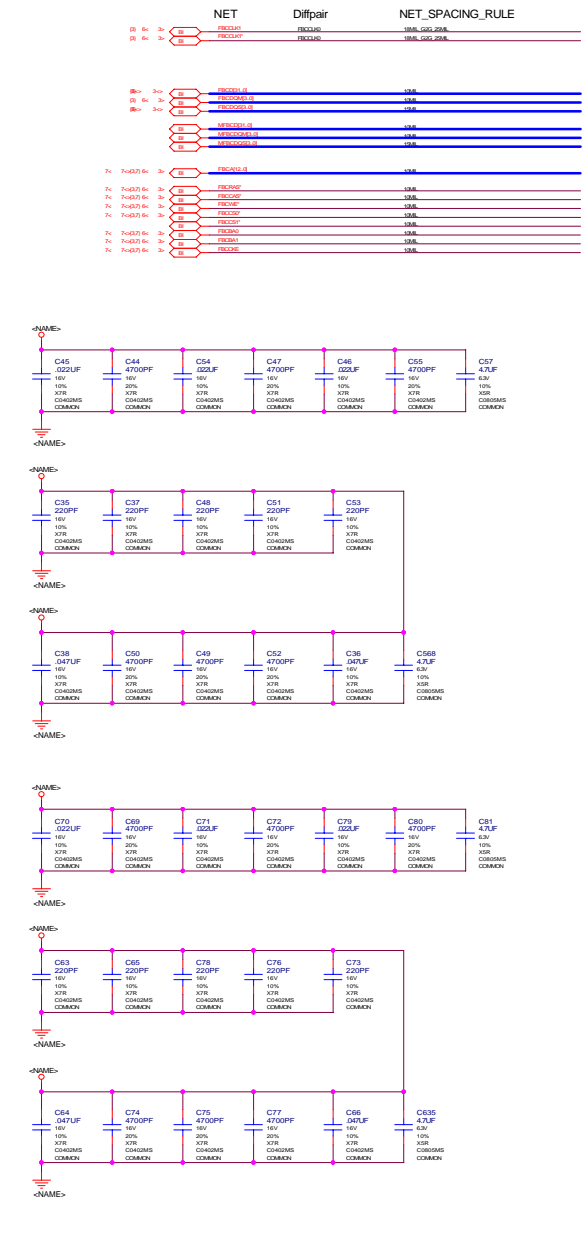
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



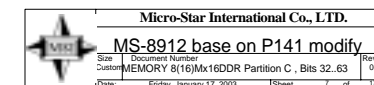
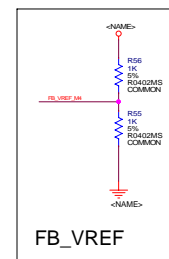
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

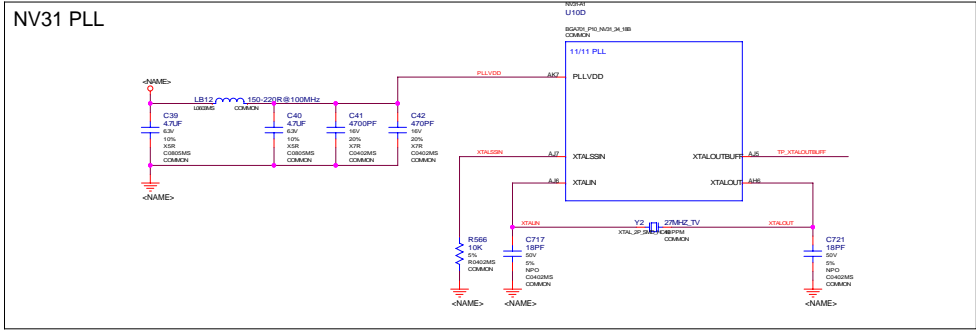
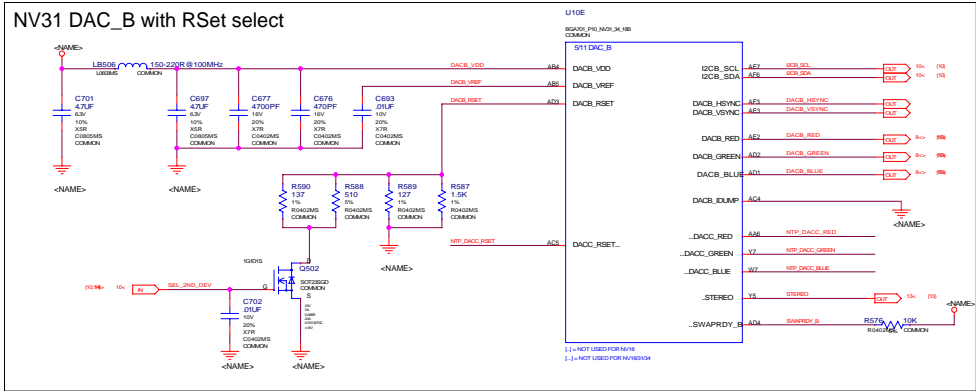
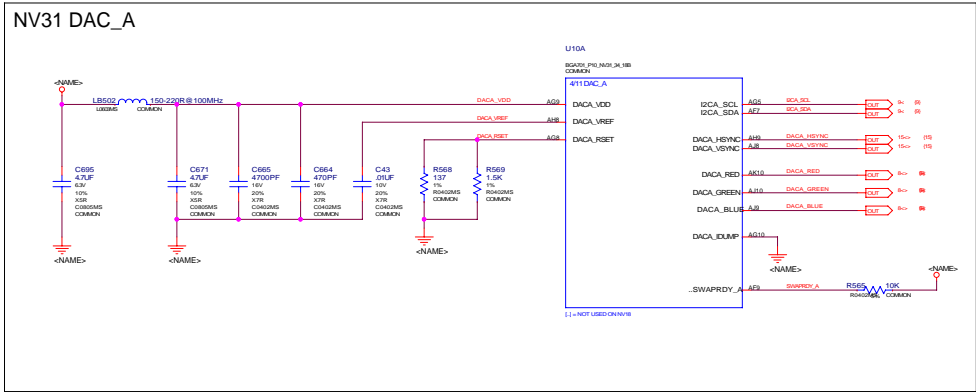


PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

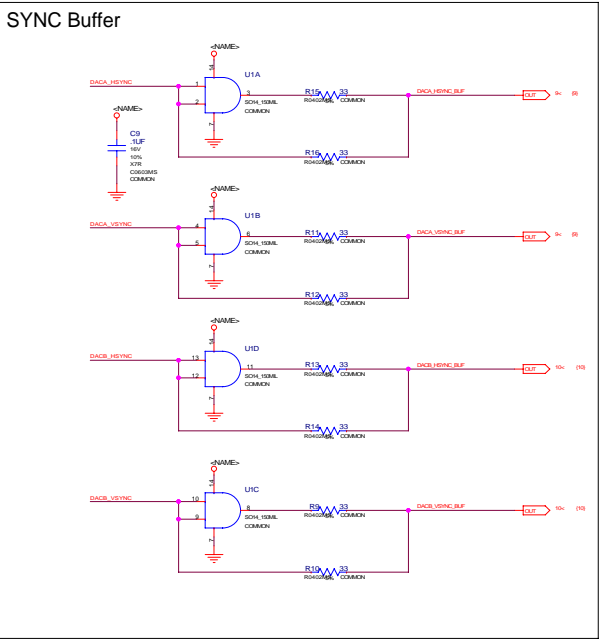


PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!





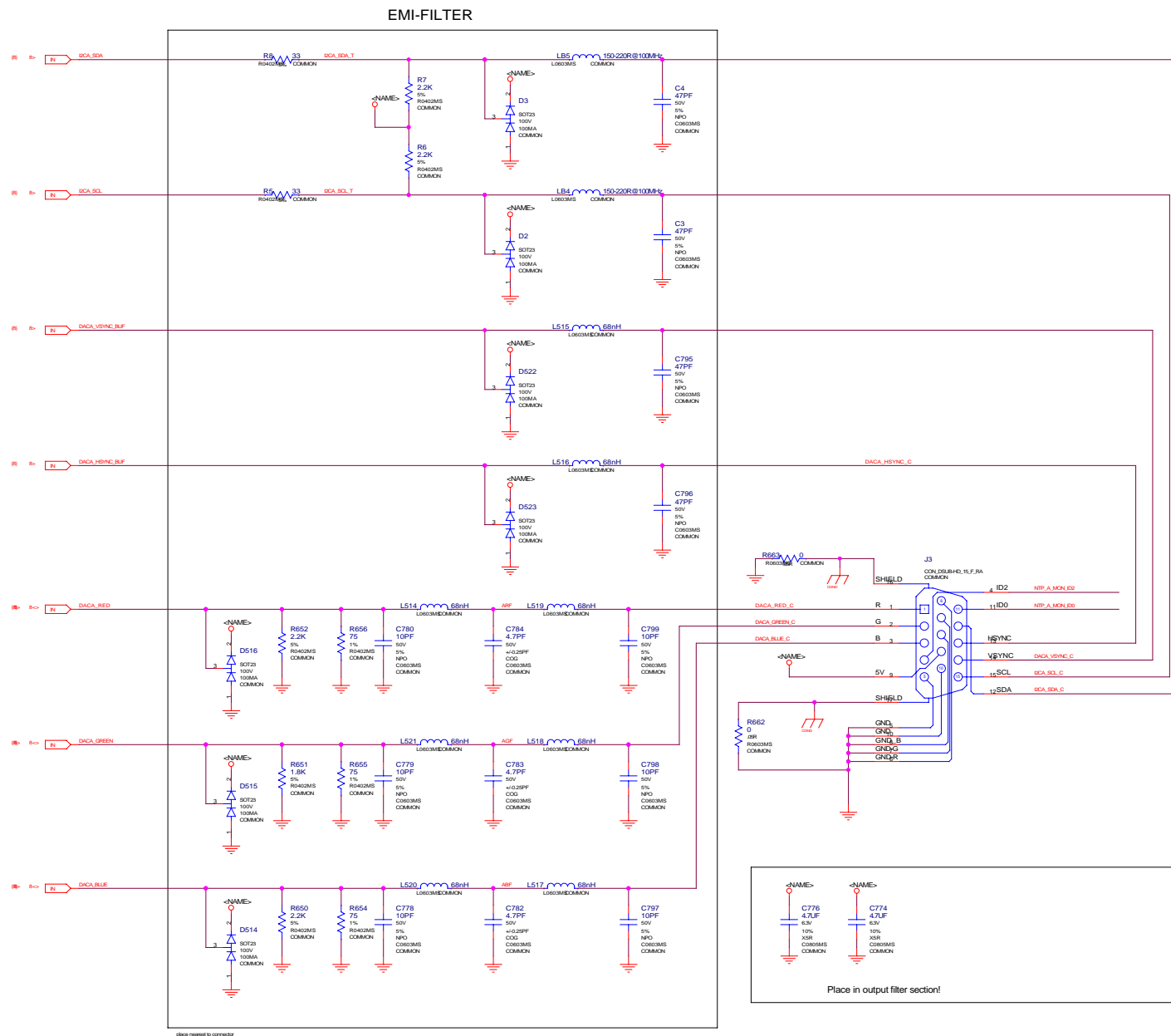
NET	NET_PHYSICAL_TYPE	VOLTAGE
DACA_VDD	100M_TRACK	3.3V
DACA_VREF	100M_TRACK	3.3V
DACA_RSET	100M_TRACK	3.3V
DACA_VDD	100M_TRACK	3.3V
DACA_VREF	100M_TRACK	3.3V
DACA_RSET	100M_TRACK	3.3V
PLL_VDD	100M_TRACK	3.3V
PLL_VREF	100M_TRACK	3.3V
PLL_RSET	100M_TRACK	3.3V
NET	NET_PHYSICAL_TYPE	NET_SPACING_RULE
DACA_RED	100M_TRACK	100M_TRACK
DACA_GREEN	100M_TRACK	100M_TRACK
DACA_BLUE	100M_TRACK	100M_TRACK
DACA_RED	100M_TRACK	100M_TRACK
DACA_GREEN	100M_TRACK	100M_TRACK
DACA_BLUE	100M_TRACK	100M_TRACK





Primary Display (DACA), DB15 only!

NET		NET_SPACING_RULE	
BI	ASF	2XMR, GIG, XMR	
BI	AGP	2XMR, GIG, XMR	
BI	ASF	2XMR, GIG, XMR	
BI	DACA, RED, C	2XMR, GIG, XMR	
BI	DACA, GREEN, C	2XMR, GIG, XMR	
BI	DACA, BLUE, C	2XMR, GIG, XMR	



Place all filter components  
on the side nearest to the  
reference GND plane!

Route all signals only on  
layers referenced to GND!

Don't split the reference  
GND plane beneath  
a RGB signal!

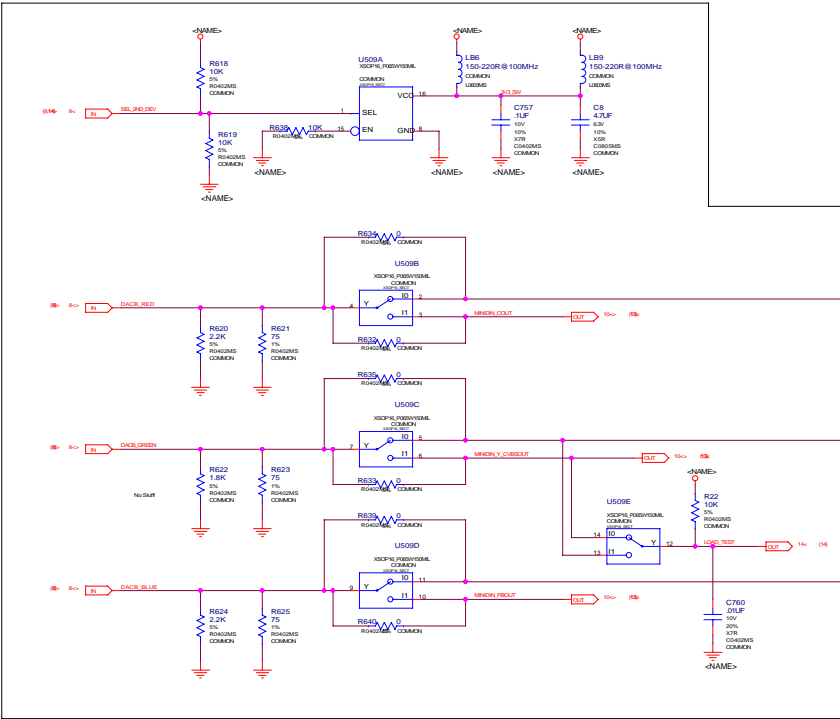
Secondary Display (DACB), long DB15 optional DVI-I

Place all filter components  
on the side nearest to the  
reference GND plane!

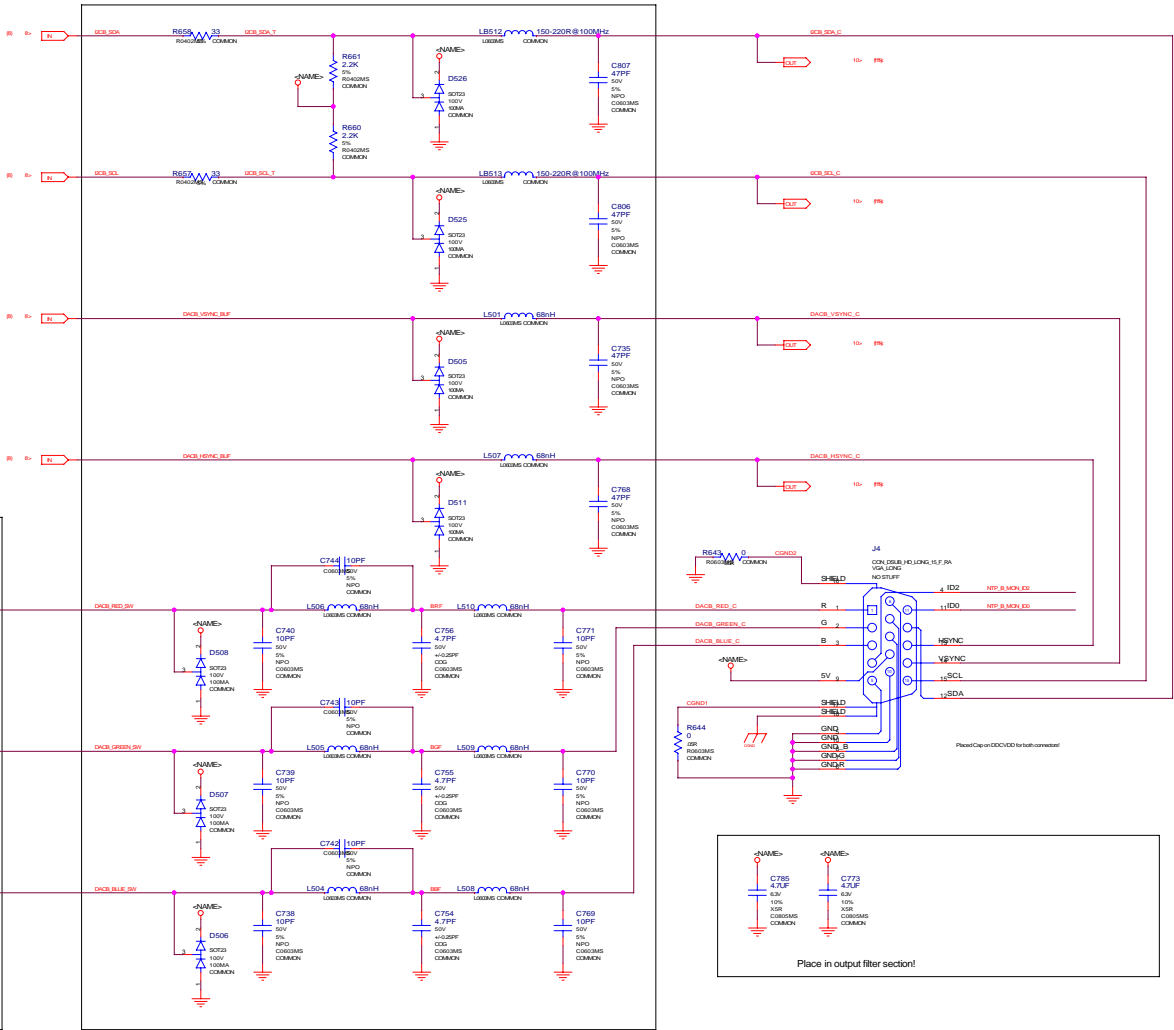
Route all signals only on  
layers referenced to GND!

Don't split the reference  
GND plane beneath  
a RGB signal!

DACB Multiplexer

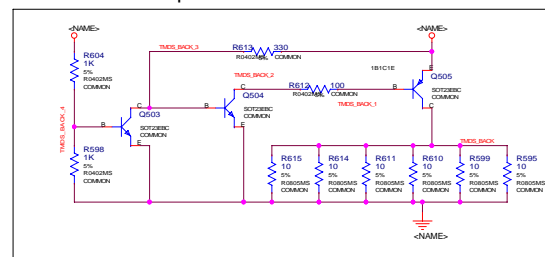


EMI-FILTER

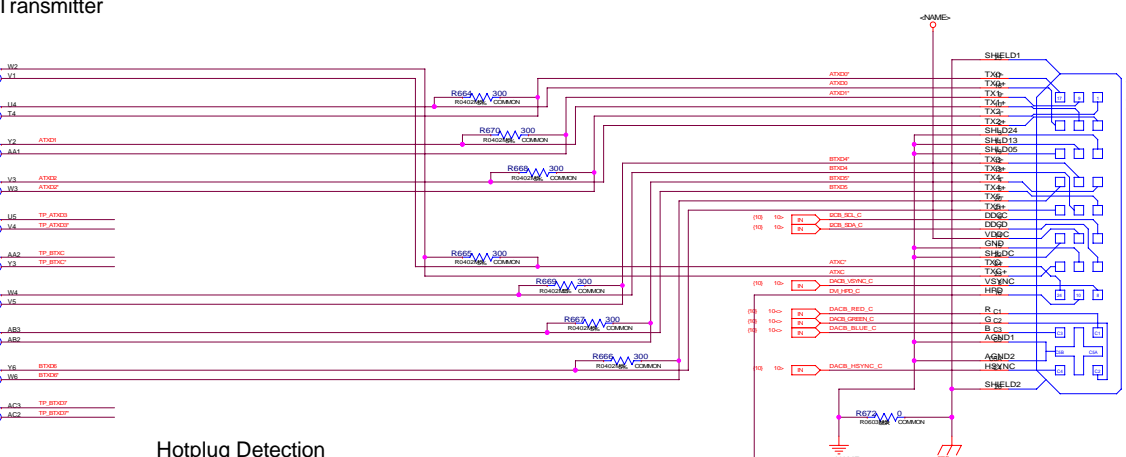
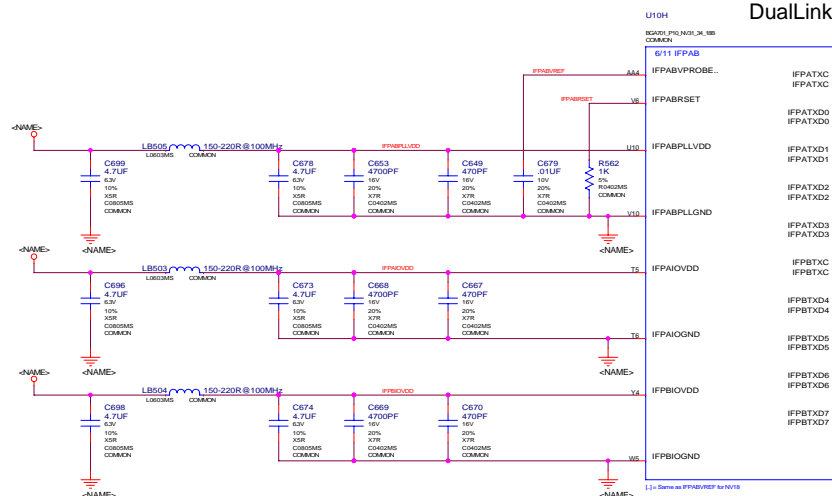


NET		NET_SPACING_RULE	
1	REF	2000	2000
2	REF	2000	2000
3	REF	2000	2000
4	DACB_RED_C	2000	2000
5	DACB_GREEN_C	2000	2000
6	DACB_BLUE_C	2000	2000
7	DACB_RED_BV	2000	2000
8	DACB_GREEN_BV	2000	2000
9	DACB_BLUE_BV	2000	2000
10	MINI_V_COSMET	2000	2000
11	MINI_V_COSMET	2000	2000
12	MINI_V_COSMET	2000	2000

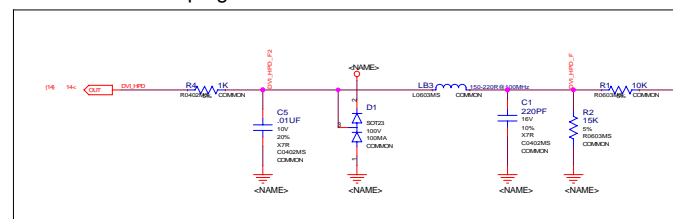
### Unused Transmitter

[illegible]

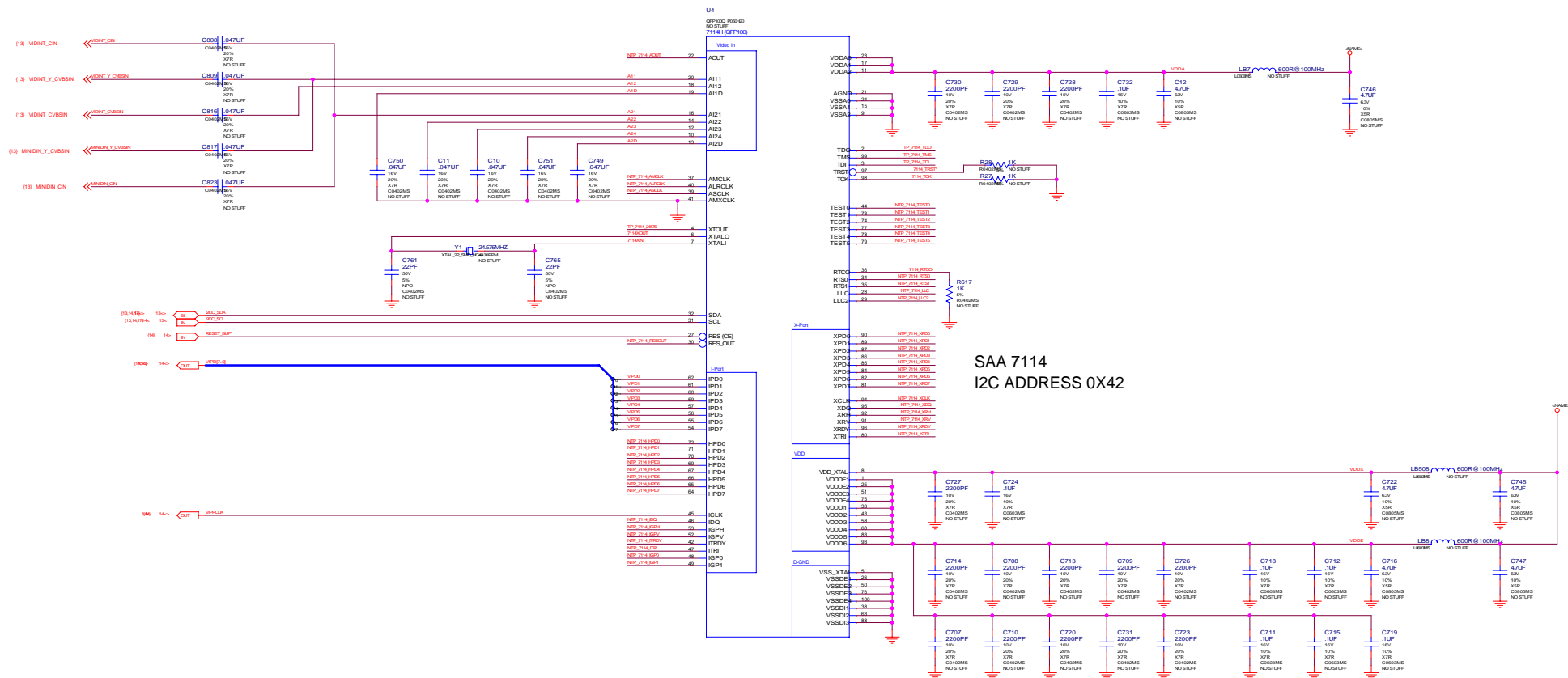
## DualLink Transmitter



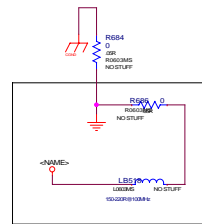
## Hotplug Detection



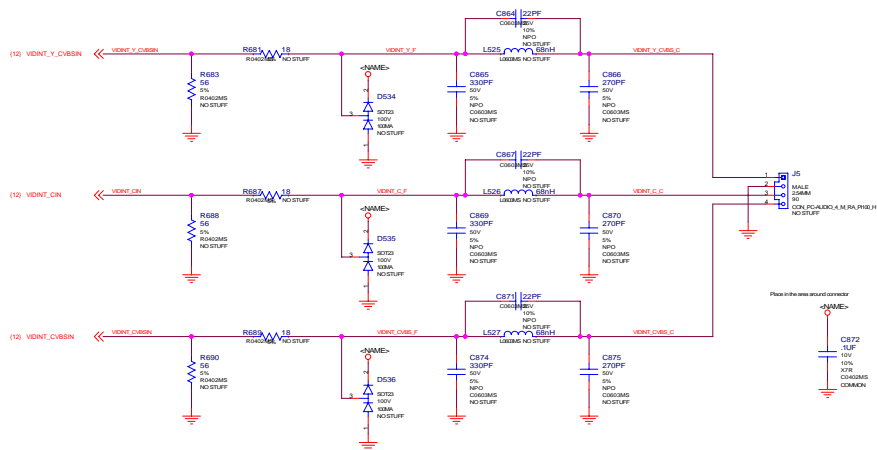
## VIDEO CAPTURE



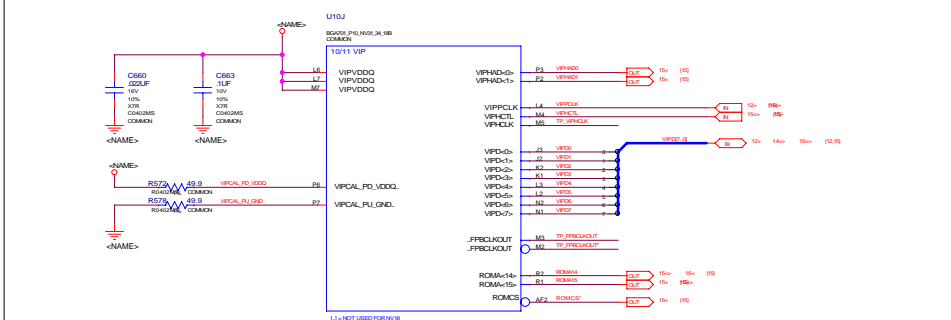
## INTERNAL VIDEO IN CONNECTOR



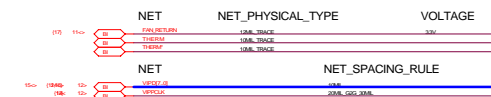
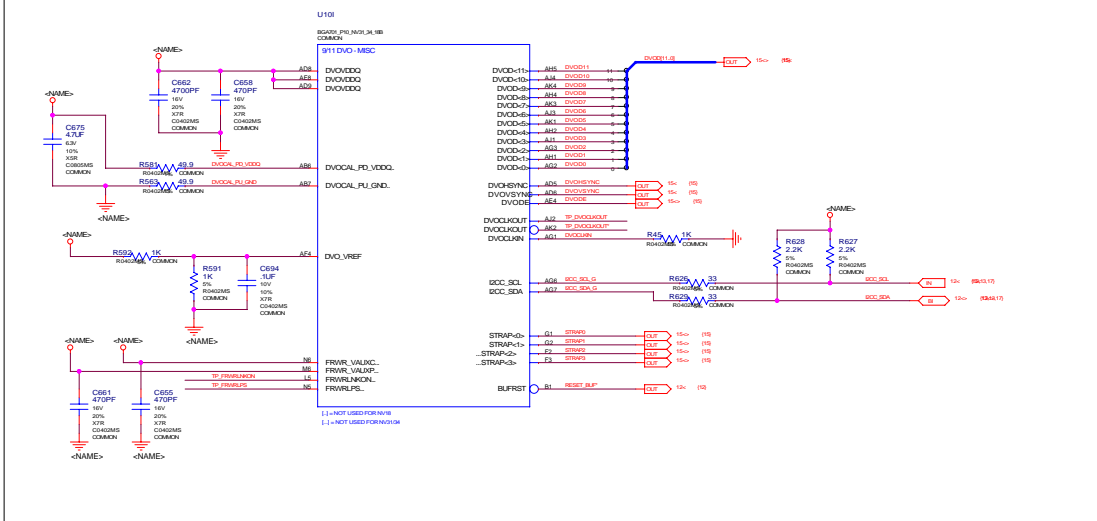
STEREO GLASSES BUFFER

[illegible]

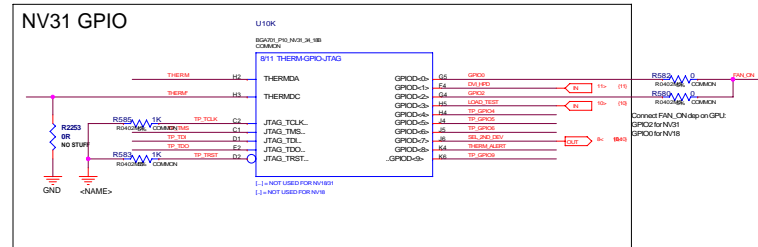
## NV31 VIP



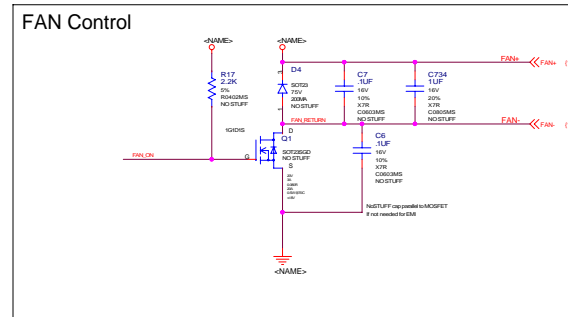
\_\_\_\_\_



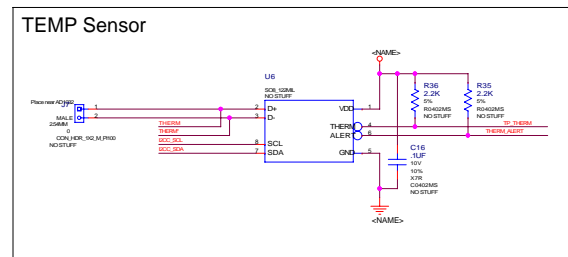
\_\_\_\_\_



© 2005 Blackwell Publishing Ltd

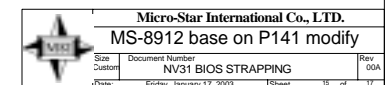
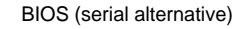


\_\_\_\_\_



OR MASK  
1  $\Rightarrow$  DESIRED=1 AND MASK=0

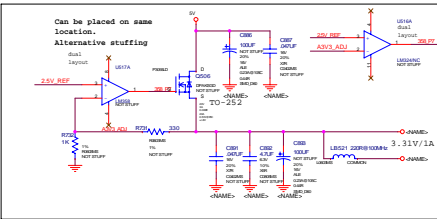
## BIOS (serial)



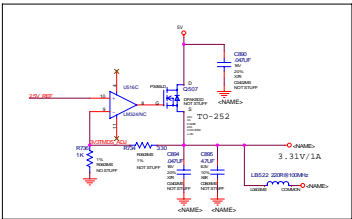
POWER SUPPLY

POWER SUPPLY

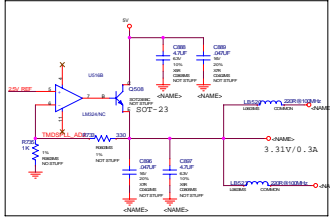
ANALOG 3V3



TMDS 3V3 Supply

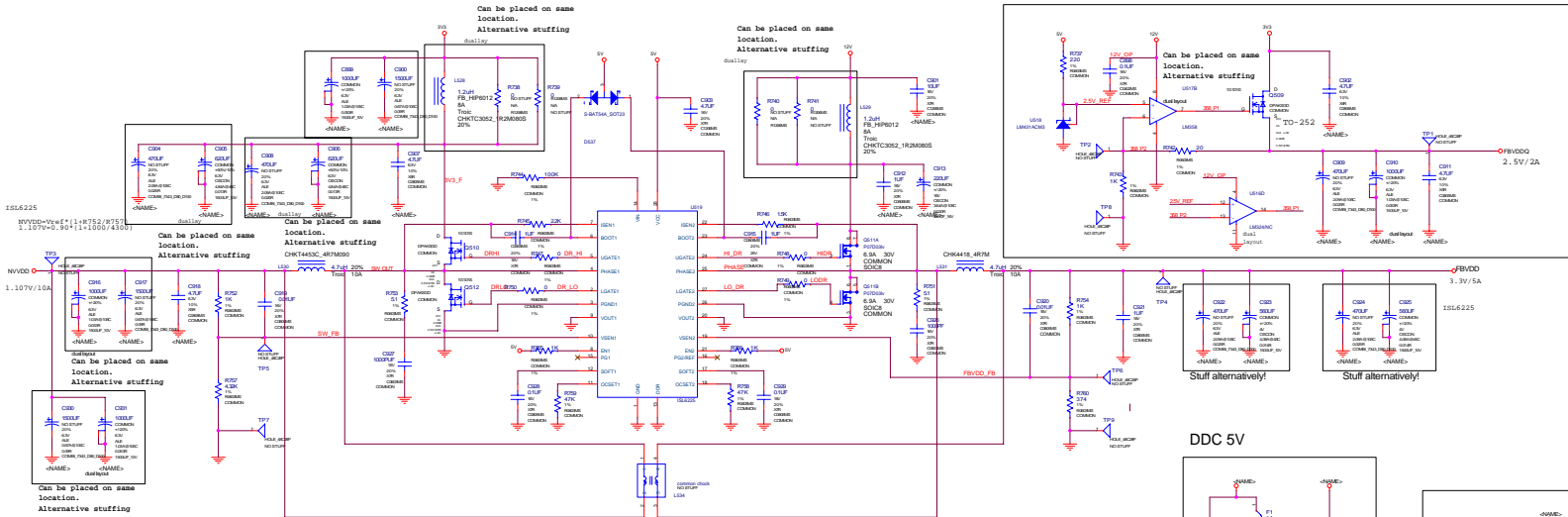


TMDS PLL Supply

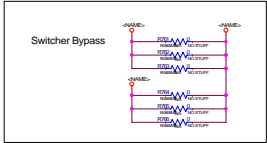
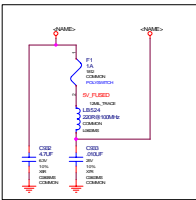


NVDD-SWITCHER / FBVDDQ-LDO CONTROLLER

Replaced ISL6225 with ISL6225.  
Replaced POT03LV with APMT7312.

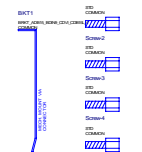


DDC 5V



MECHANICAL COMPONENTS

BRACKET



HEATSINK

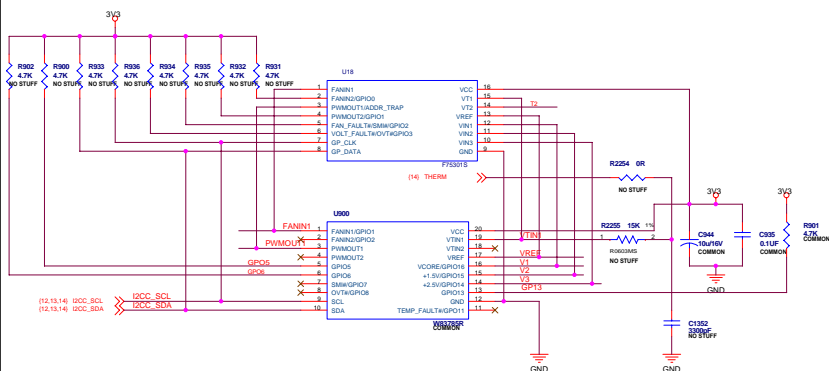
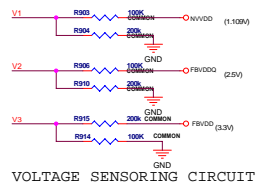
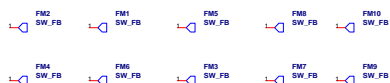


FBVDDQ= VRef \* (1+Rtop/ Rbot)  
ISL6225 2.5V = 0.800V \* (1+2.37K/1.13K)  
SC2610 2.5V = 1.250V \* (1+1.02K/1.02K)

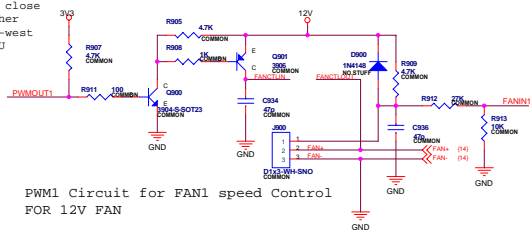
Va=[0.9V\*( Rtop +Rbot )] / Rbot

ISL6225 FBVDD = [0.9V \* (1K+375)] / 375 =3.3V  
NV31 NVVDD = [0.9V \* (1K+4.3K)] / 4.3K =1.109V  
NV18B Stand Volt need 1.656 V.





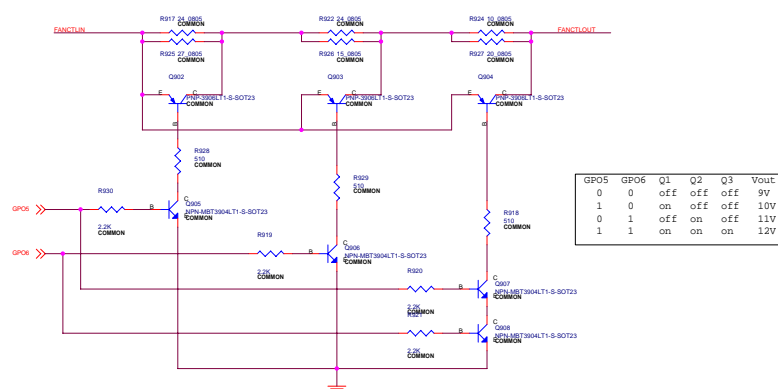
Place close  
together  
south-west  
of GPU



PWM1 Circuit for FAN1 speed Control  
FOR 12V FAN



TEMPERATURE SENSING CIRCUIT



GPO5	GPO6	Q1	Q2	Q3	Vout
0	0	off	off	off	9V
1	0	on	off	off	10V
0	1	off	on	off	11V
1	1	on	on	on	12V