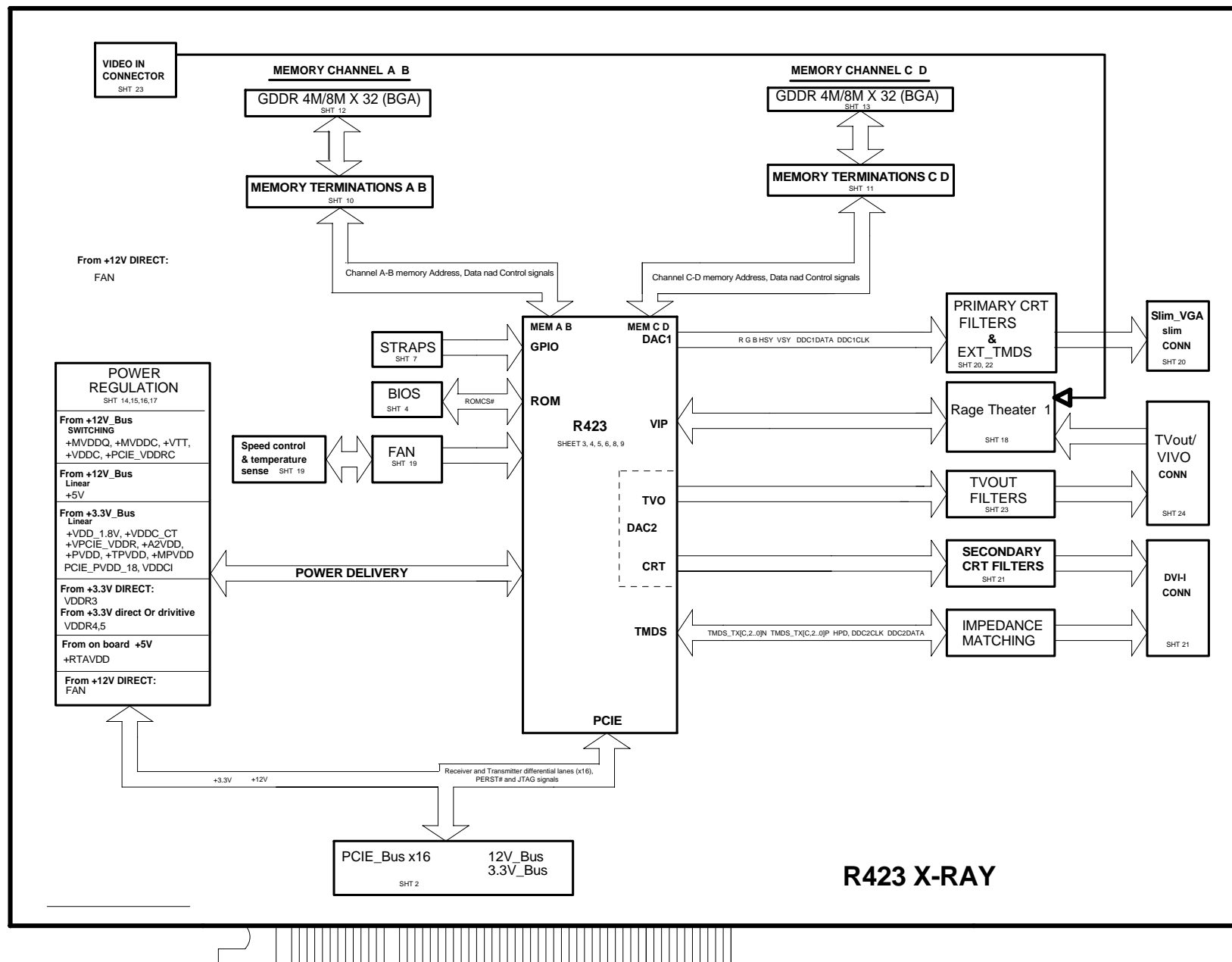


MS8997 100 (A321)

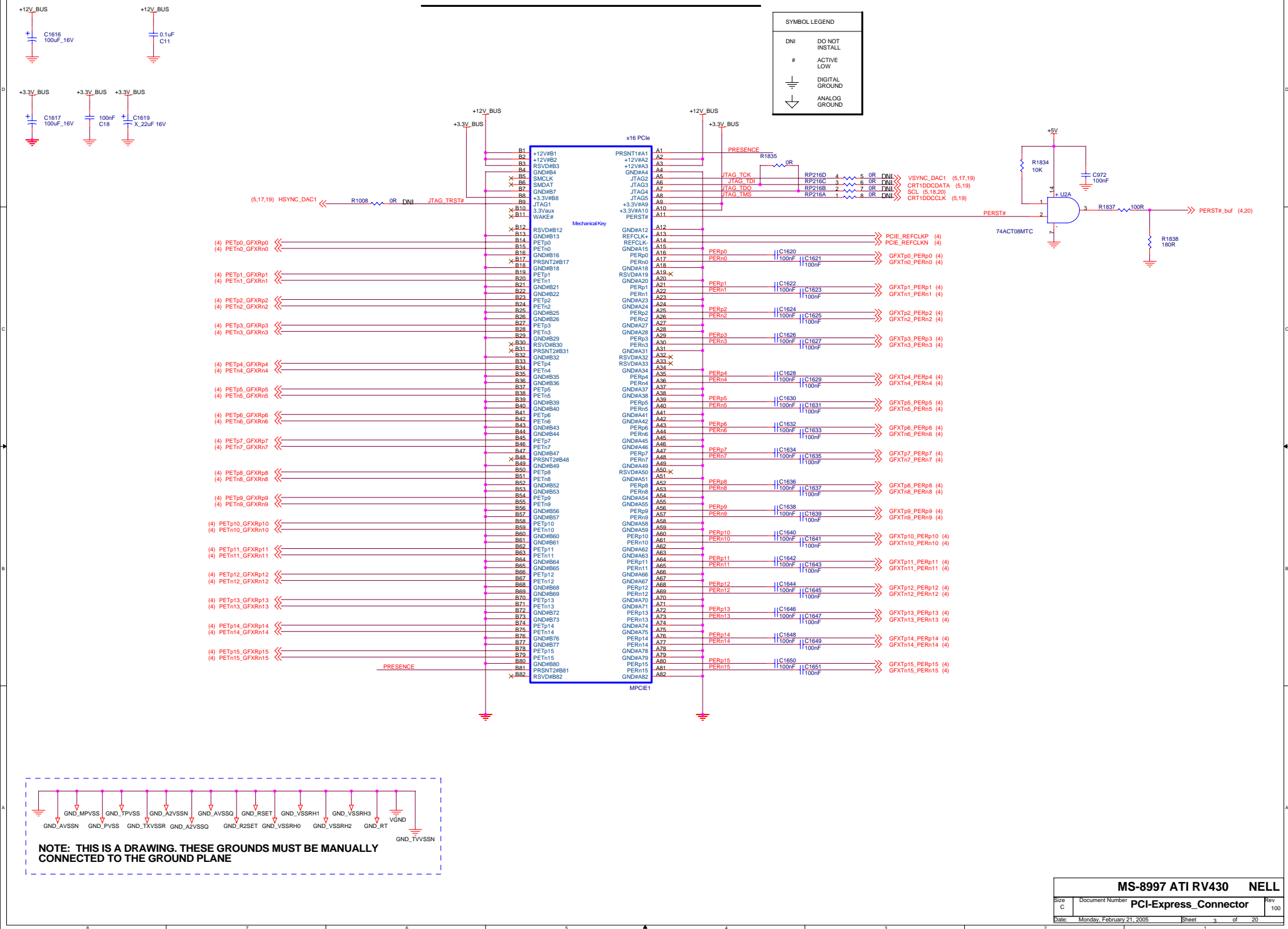
ATI-PCIEXPRESS RV430 BGA 8MX32 DDR-I, VGA, DVI-I, TV-OUT, SCART (VIA1623)

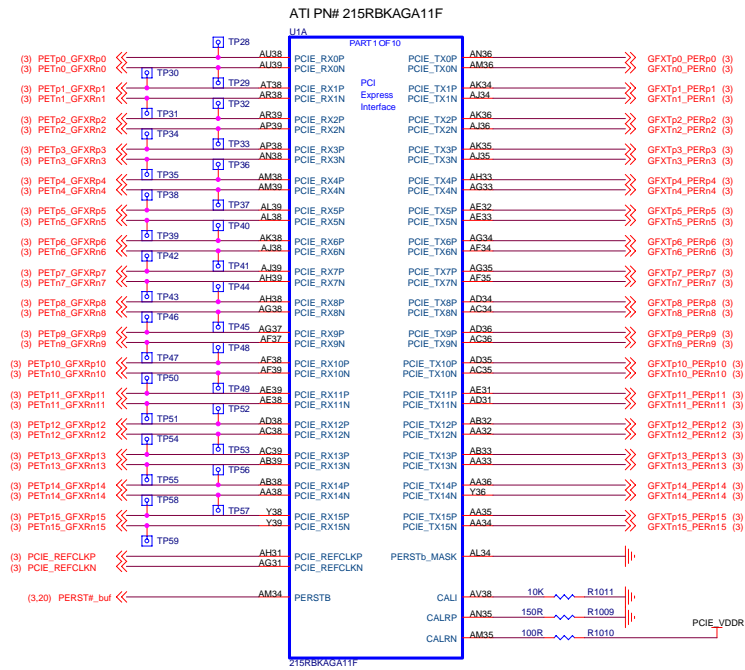
TITLE	PAGE
COVER	1
BLOCK	2
PCI-EXPRESS CONNECTOR	3
RV430 PCIE_INTERFACE	4
RV430_MAIN	5
RV430_POWER	6
RV430 GND	7
REGULATOR FOR GPU, MEMORY AND OTHERS	8, 9, 10
RV430 MEMORY A-B / C-D	11, 12
VTT TERMINATION FOR MEMORY A-B / C-D	13, 14
BGA 4MX32 / 8MX32 DDR A-B / C-D	15, 16
STRAPPING	17
THERMAL MANAGEMENT	18
CRT, DVI-I CONNECTOR	19
VIA 1623M (SCART OUT)	20

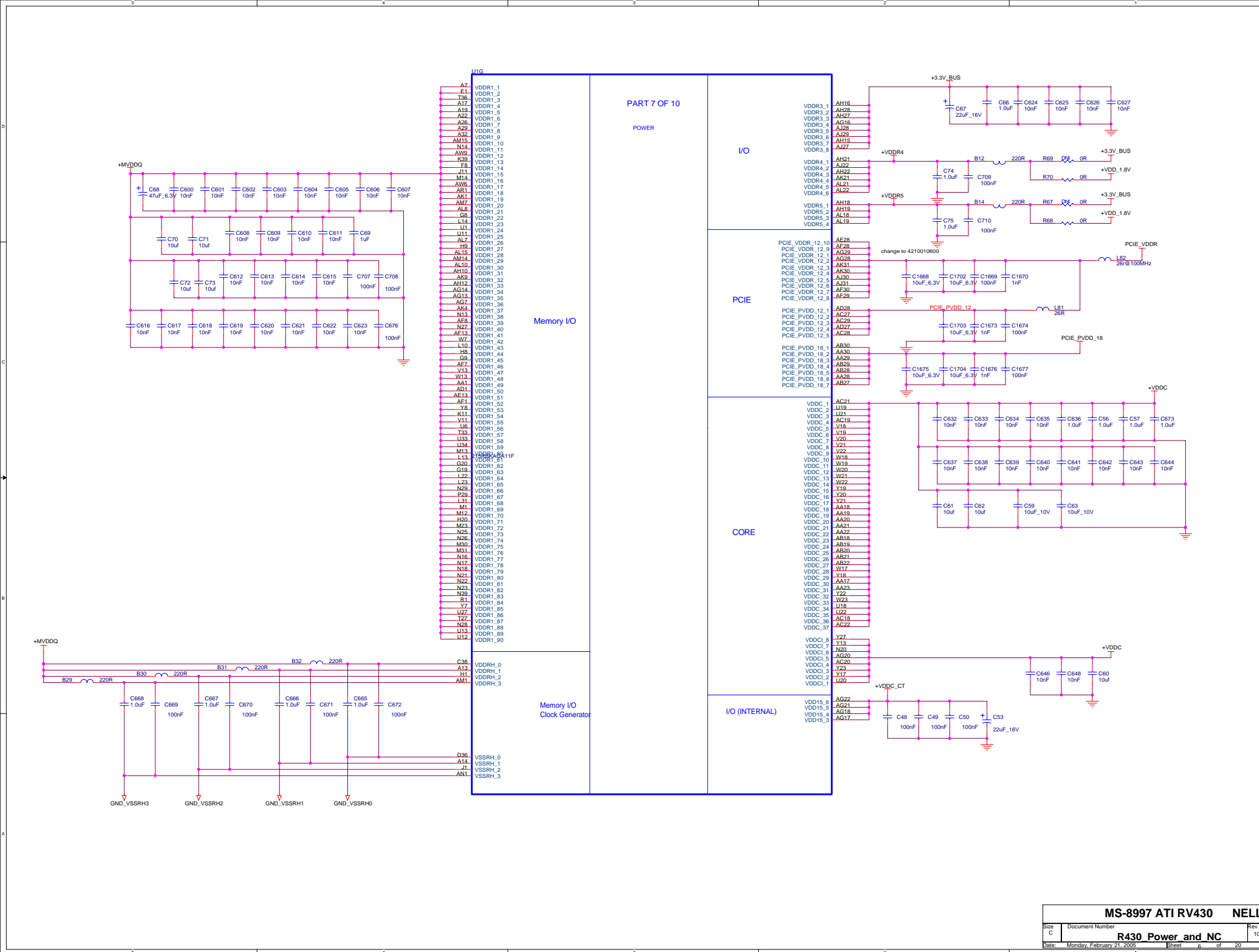
FREQUENCY	MHZ
CORE	400
MEMORY	350

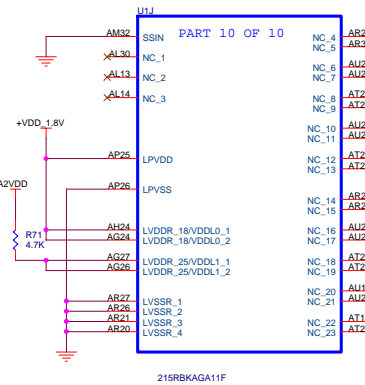
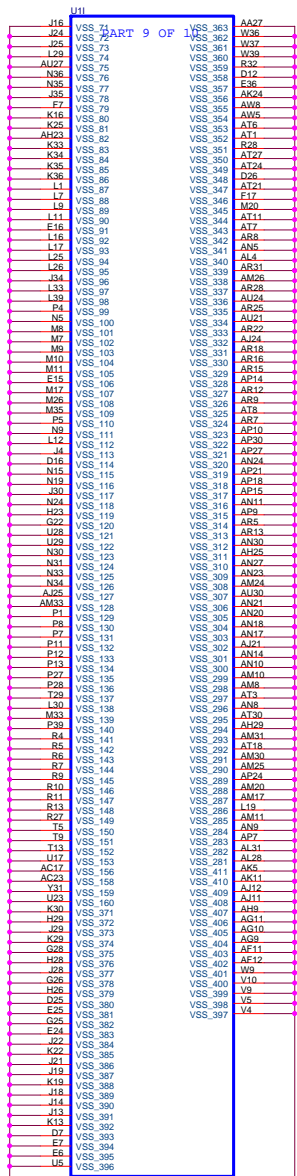
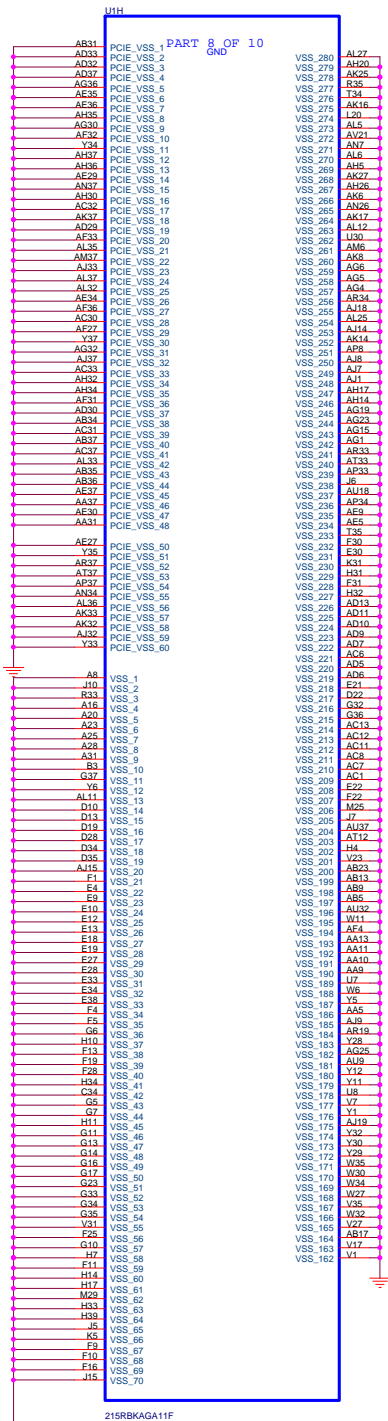


PCI-EXPRESS EDGE CONNECTOR

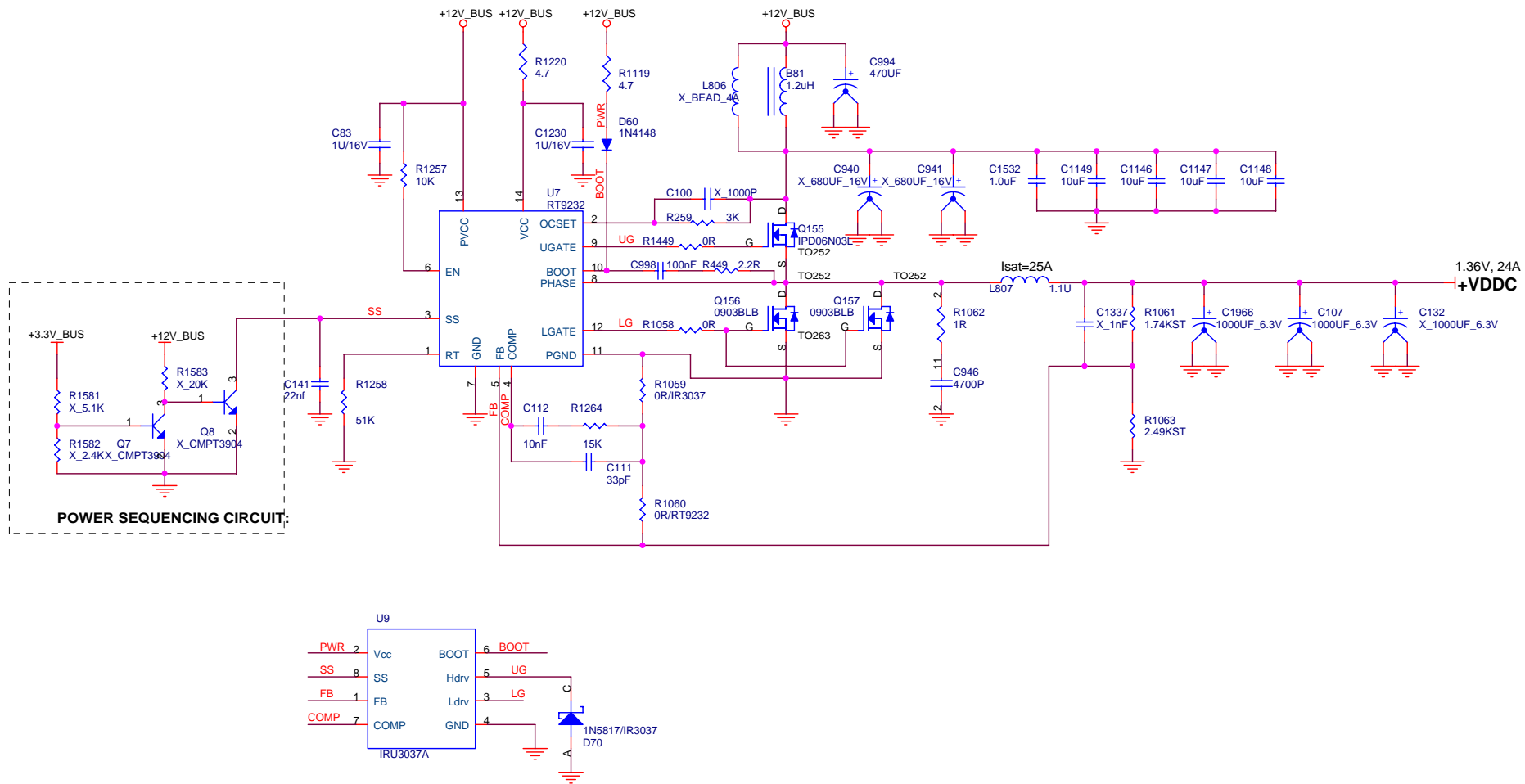








VDDC



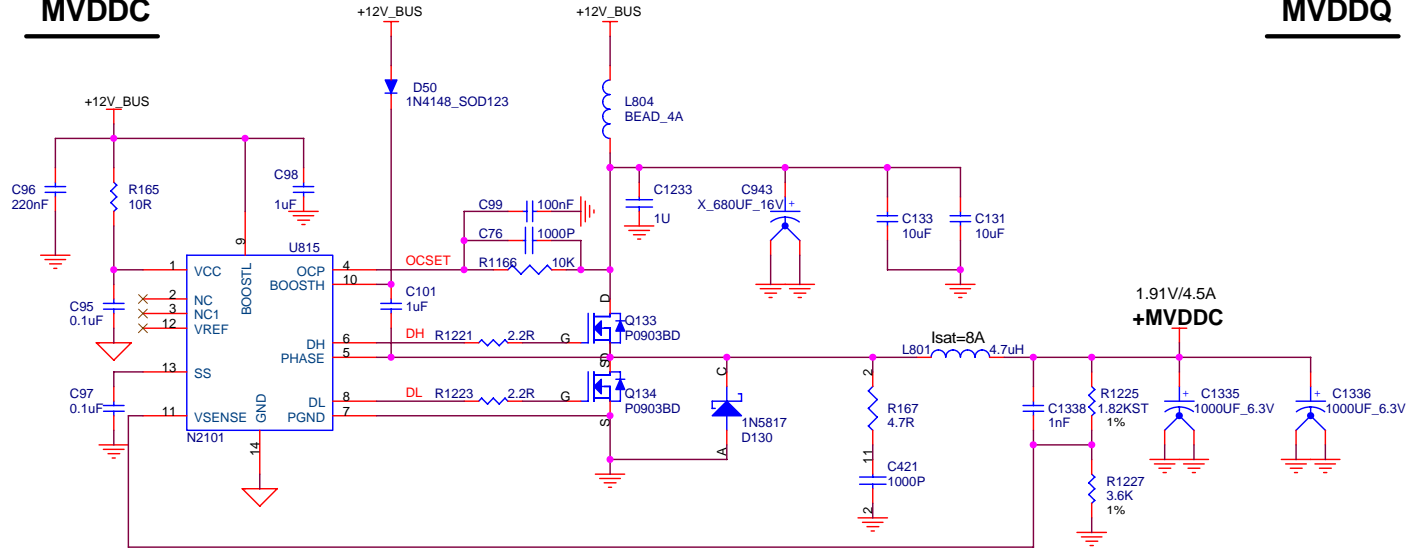
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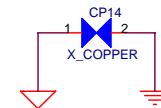
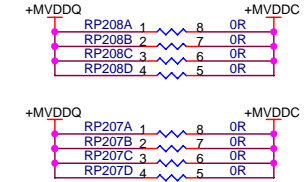
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Regulator of GPU

MVDDC

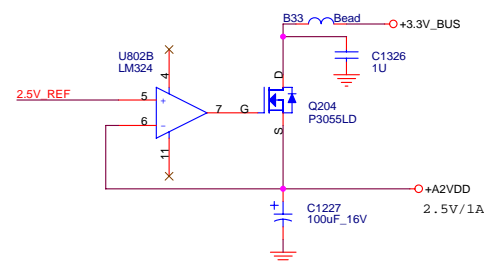
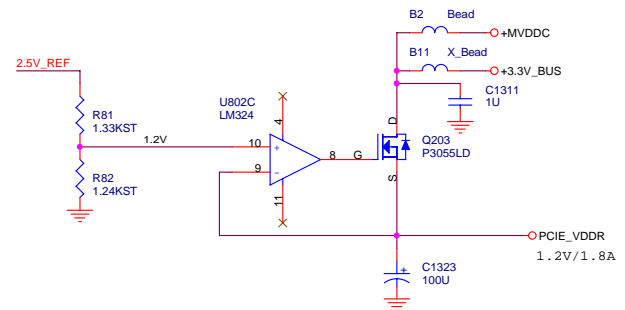
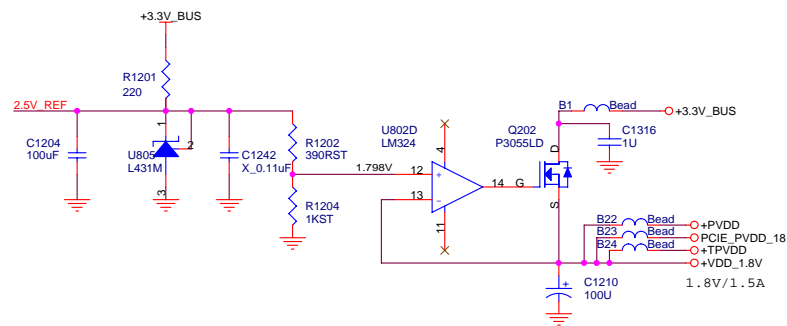
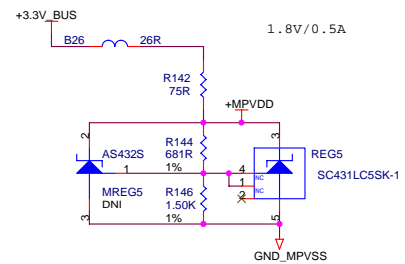
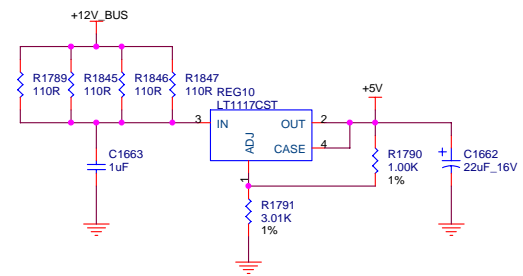
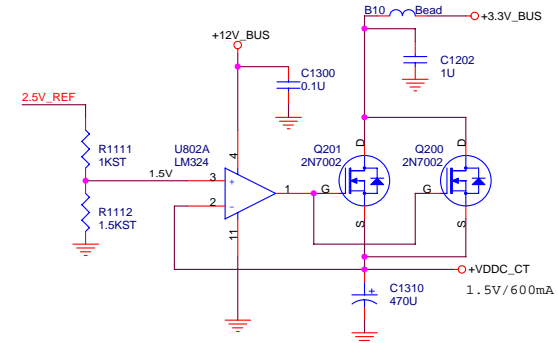
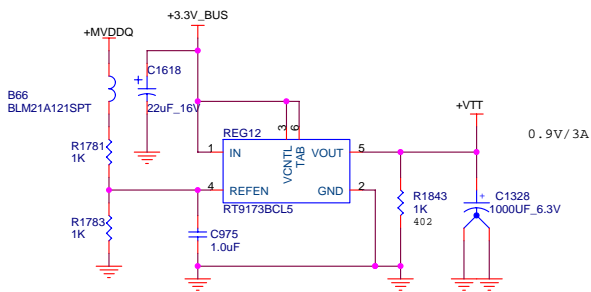


MVDDQ



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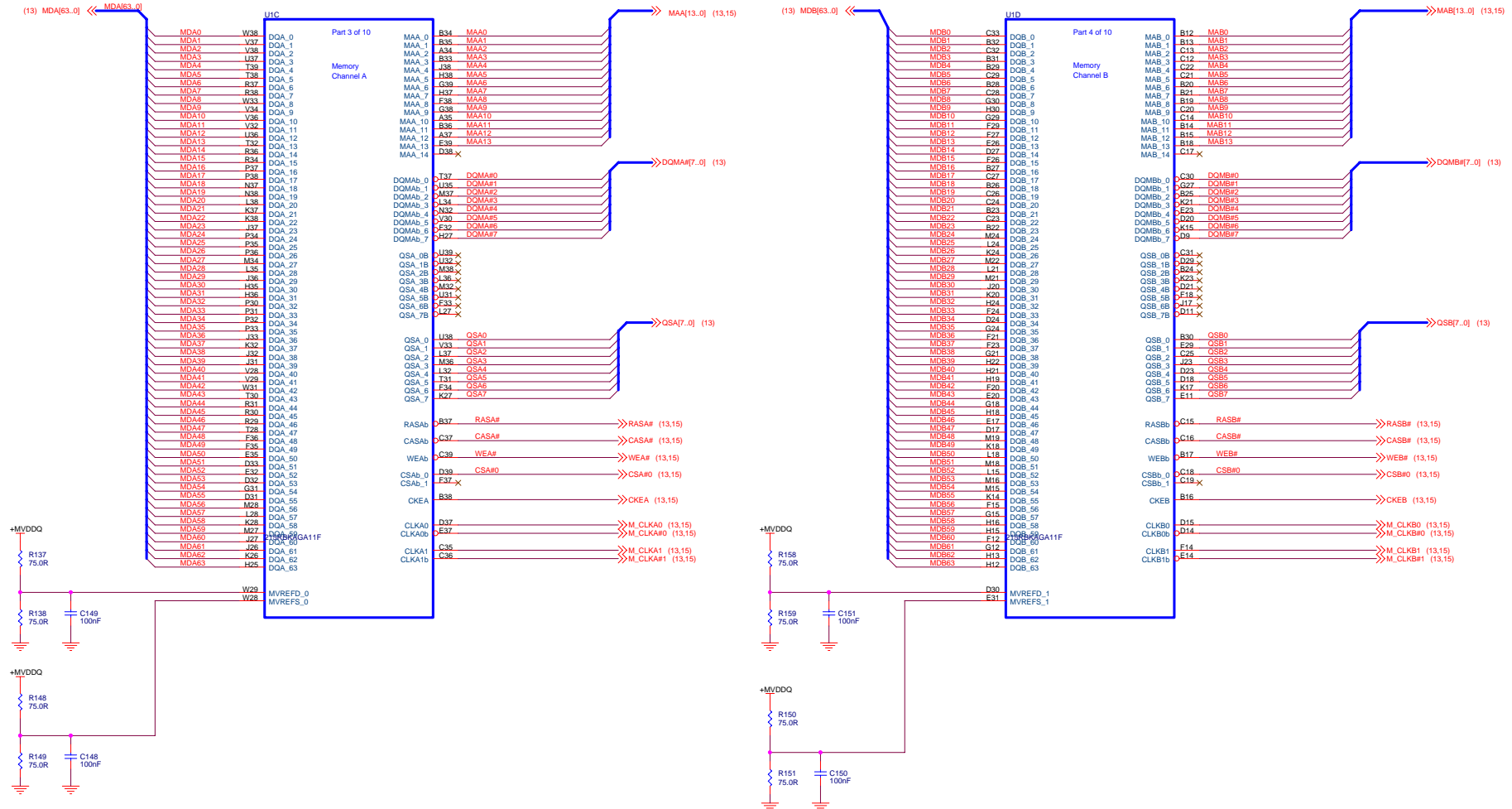
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Regulator of Memory
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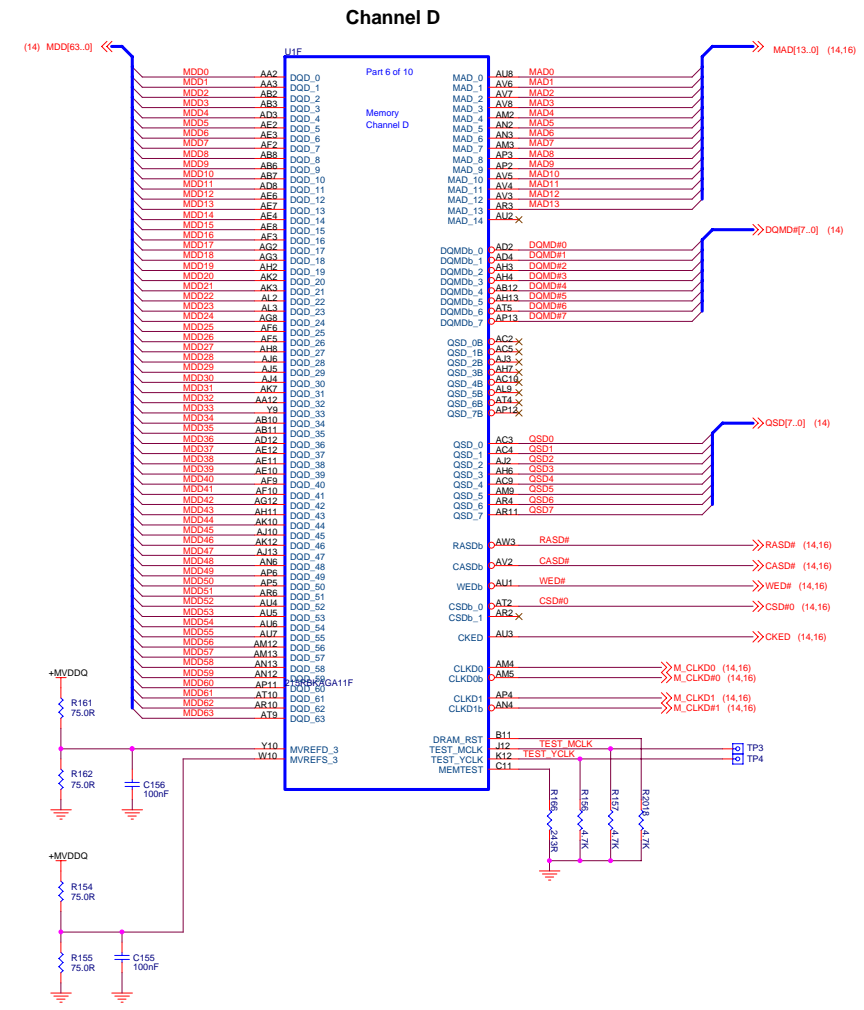
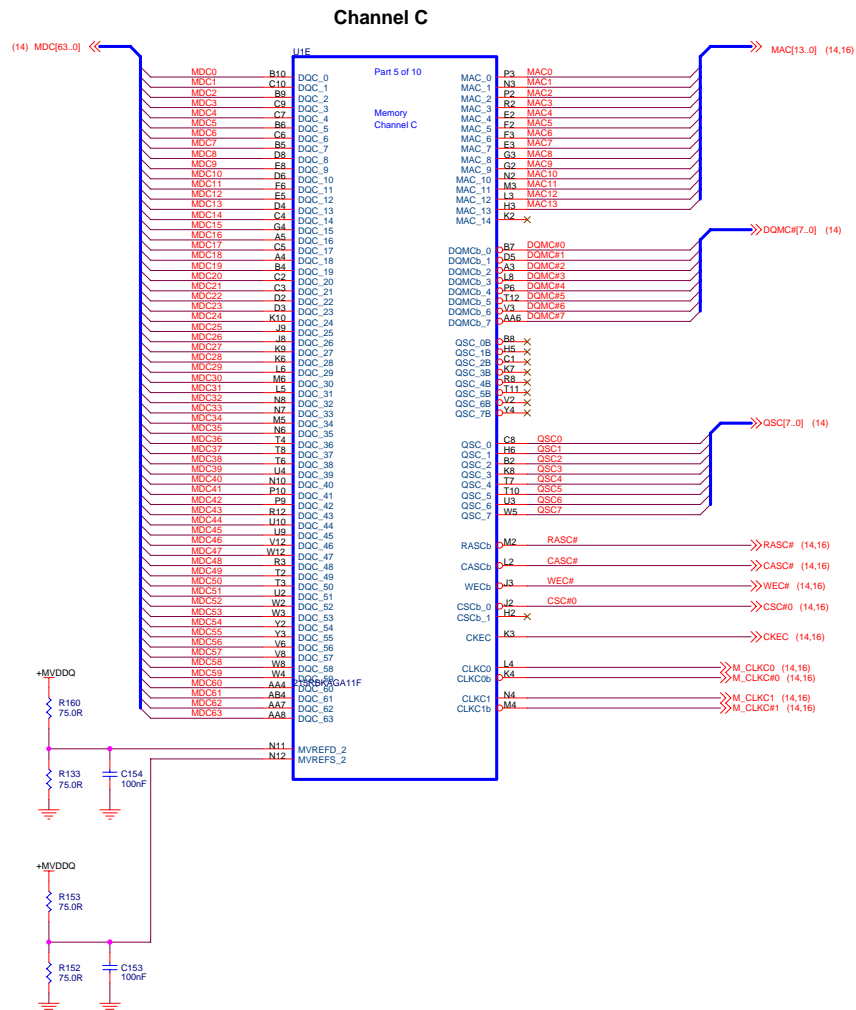
R-420 MEMORY CHANNELS A and B

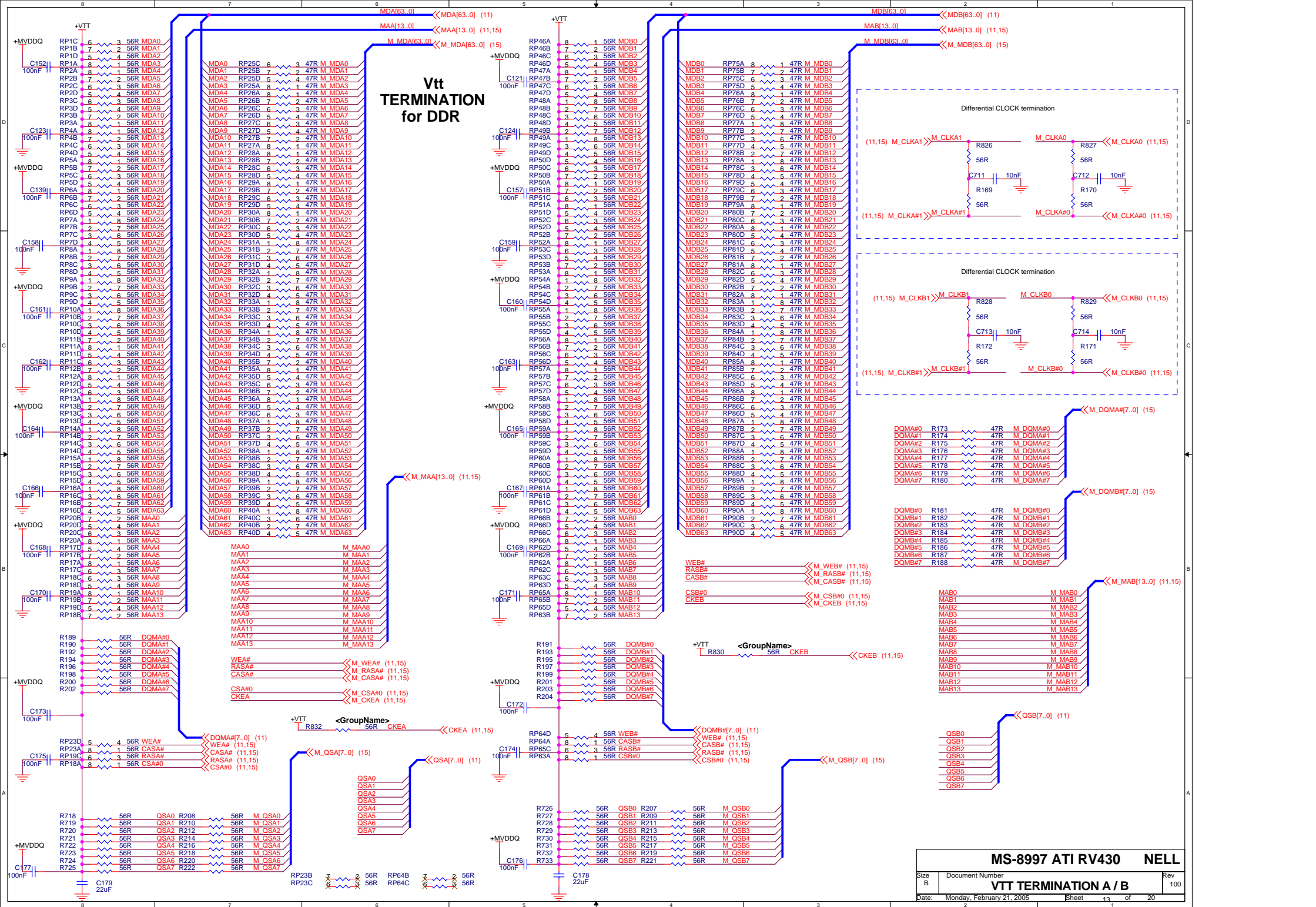
Channel A

Channel B

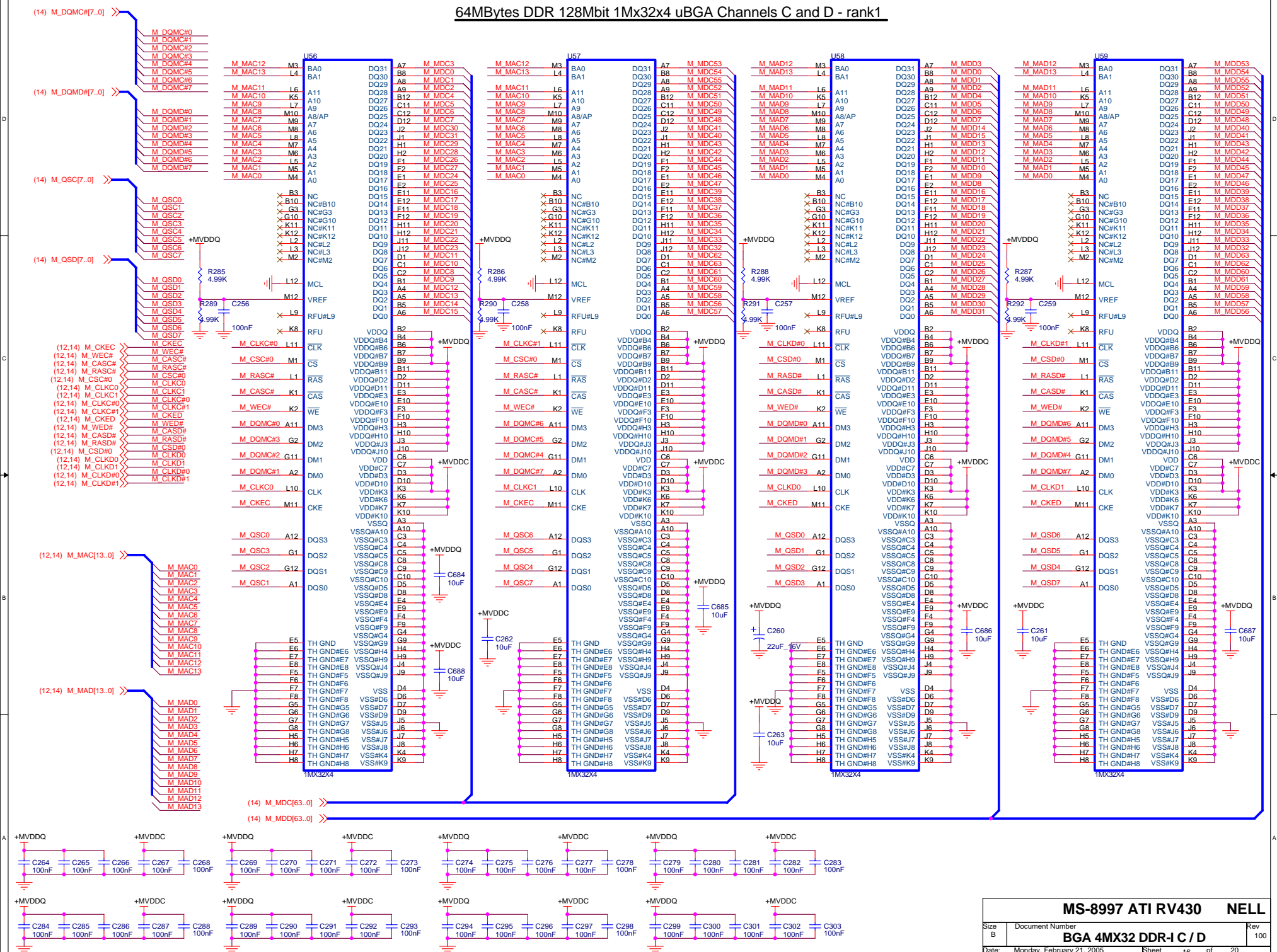


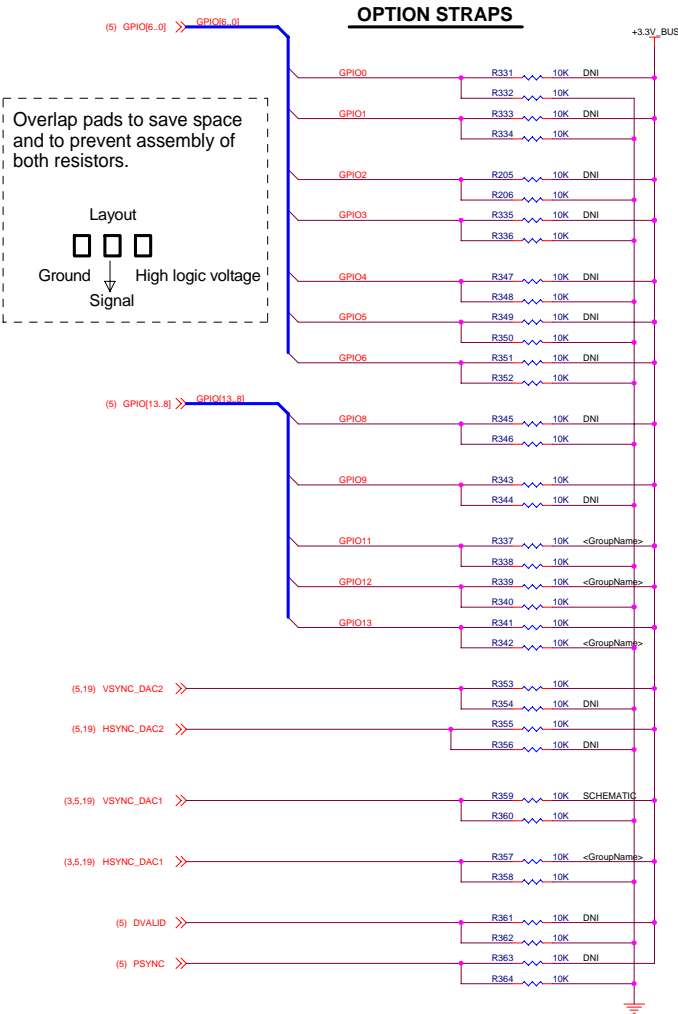
R-420 MEMORY CHANNELS C and D





64MBytes DDR 128Mbit 1Mx32x4 uBGA Channels C and D - rank1

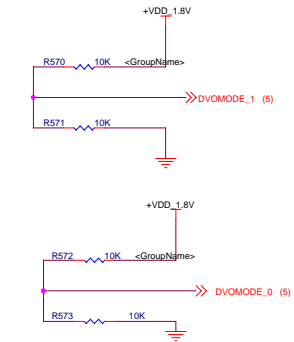
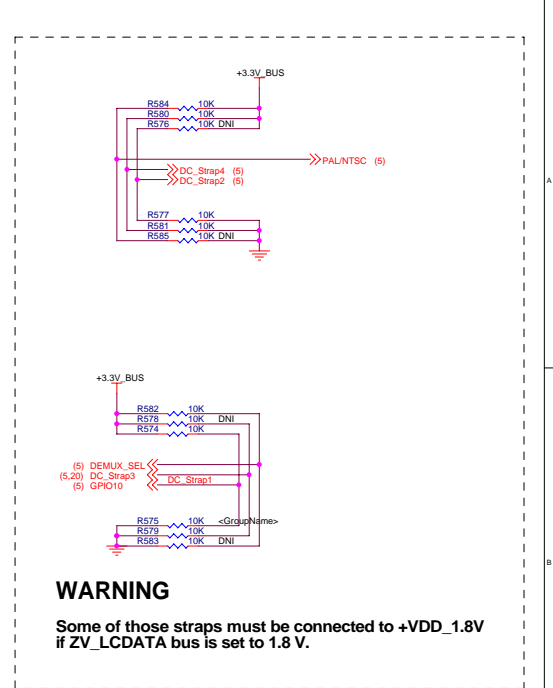




R423 Shared Straps			REV. 0.0
STRAPS	PIN	DESCRIPTION	DEFAULT
MOBILE_FEATURE0	GPIO(0)	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Desktop must have an external pullup)	0
MOBILE_FEATURE1	GPIO(1)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Desktop must have an external pullup)	0
PCI_E_MODE (ATI Internal)	GPIO(3/2)	PCI_E mode: 00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: Short-circuit internal loopback and PCI Express 1.0A mode	00
TX_IEXT	GPIO(4)	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
FORCE_COMPLIANCE	GPIO(5)	Force chip to get to compliance state quickly for Tester purposes 0: Normal operation 1: Force to compliance state	0
PLL_BW (ATI Internal)	GPIO(6)	0: Full PLL Bandwidth 1: Reduced PLL bandwidth	0
DEBUG_ACCESS	GPIO(8)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible 0: Disable debug access 1: Enable debug access	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDs. If rom attached identifies ROM type. GPIO(9,13,12,11) 000x - No ROM,CHG_ID=00 001x - No ROM, CHG_ID=01 010x - No ROM, CHG_ID=10 011x - No ROM, CHG_ID=11 1001 - 1M Serial AT25F1024 ROM (Atmel) 1010 - 1M Serial AT45DB011 ROM (Atmel) 1011 - 1M Serial M25P10 ROM (ST) 1100 - 512K Serial M25P05 ROM (ST) 1101 - 1M Serial SST45LF010 ROM (SST) 1110 - 1M Serial W45B512 ROM (Winbond) 1111 - 1M Serial SST25VF012 ROM (SST) 1111 - 1M NX25P011B ROM (NexFlash) Chip IDs: Chip ID is based on substrate fuses and CHG_ID strap (which comes from ROM if used, or pin straps if no ROM is connected): CHG_ID = ROMIDCFG[2:1] = GPIO[13:12]	1100
MULTIFUNC(1:0)	H2SYNC, V2SYNC	Multi-function device select 00 - single function device. 01 - two function device. 10 - two function device. 11 - two function device.	10
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present such as "Theater" 1 - No slave VIP host port devices reporting presence during reset	0
RFU	HSYNC	RFU 0 - Normal 1 - Not used	0

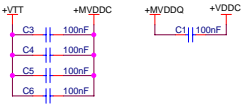
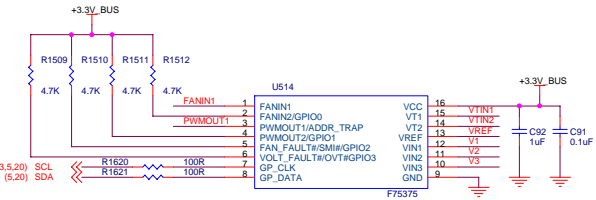
R423 Dedicated Straps			REV. 0.0
ZV_VOLTAGE_SEL0	DVOMODE_0	DVOMODE_0 is for ZV_LCDCTRL and ZV_LCDDATA(11:0). 0 - 3.3 V signaling 1 - 1.8 V signaling	0
ZV_VOLTAGE_SEL1	DVOMODE_1	DVOMODE_1 is for ZV_LCDDATA(23:12) 0 - 3.3 V signaling 1 - 1.8 V signaling	0

Board Straps			REV. 0.0
STRAPS	PIN	DESCRIPTION	DEFAULT
MEMTYPE(1:0)	DVALID, PSYNC	Memory connected to R423 identification for BIOS 00 - Hynix GDDR-1 memory 144 Ball BGA package 01 - TBD 10 - TBD 11 - TBD	00
DC_Strap1	GPIO(10)	Internal TMDs Enabled 0 - Disabled 1 - Enabled	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled 0 - Disabled 1 - Enabled	0
DC_Strap3	LCDDATA(14)	Not defined	0
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PALNTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)	1
EXT_PWR	GPIO15	External power cable detect 0 - Cable is properly connected 1 - Cable is not properly connected. Software should prevent the board from booting, should display a warning at screen and should decrease engine and memory clock speed.	NA

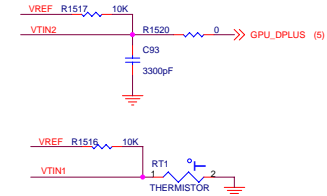


DVOMODE	ZV_LCD Level
0V	3.3V Mode
1.8V	1.8V Mode

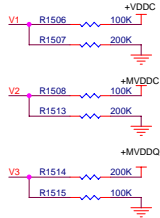
TEMPERATURE SENSE AND SPEED CONTROLLED FAN



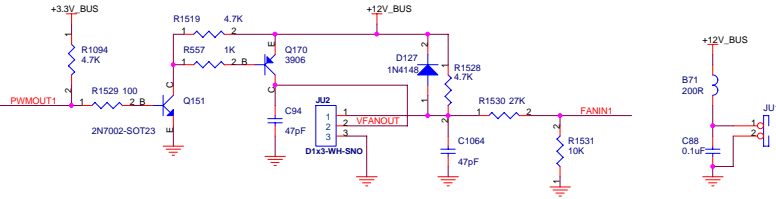
TEMPERATURE SENSING CIRCUIT



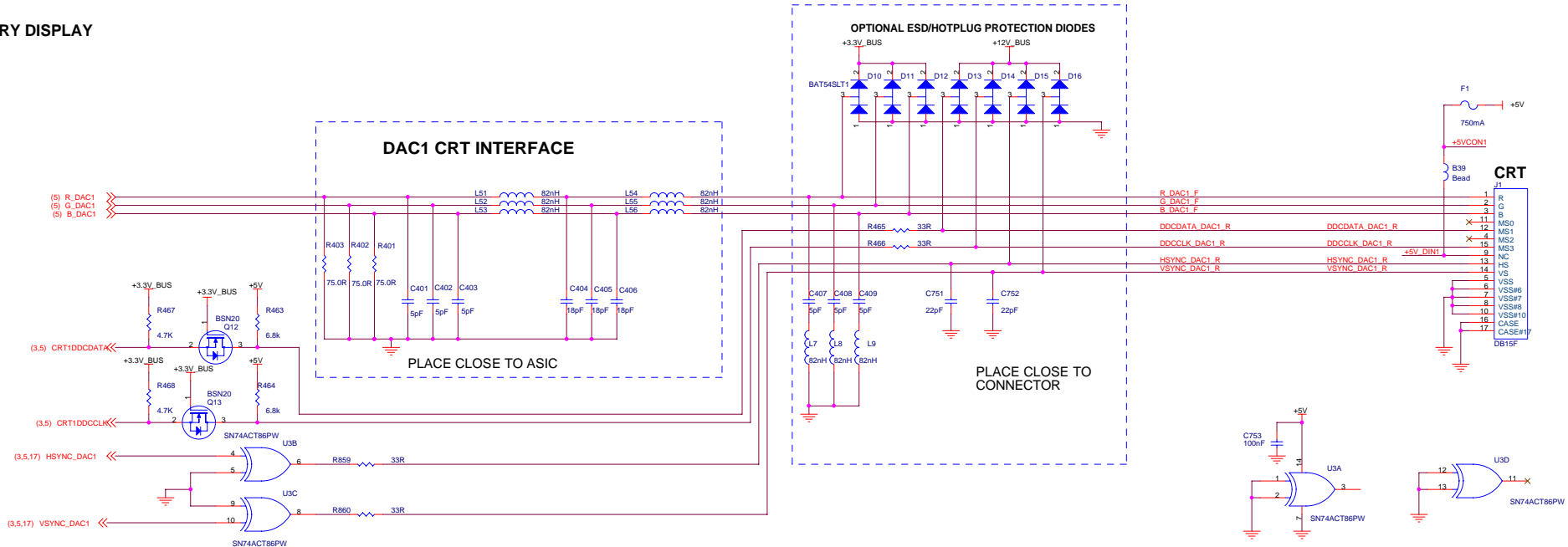
VOLTAGE SENSING CIRCUIT



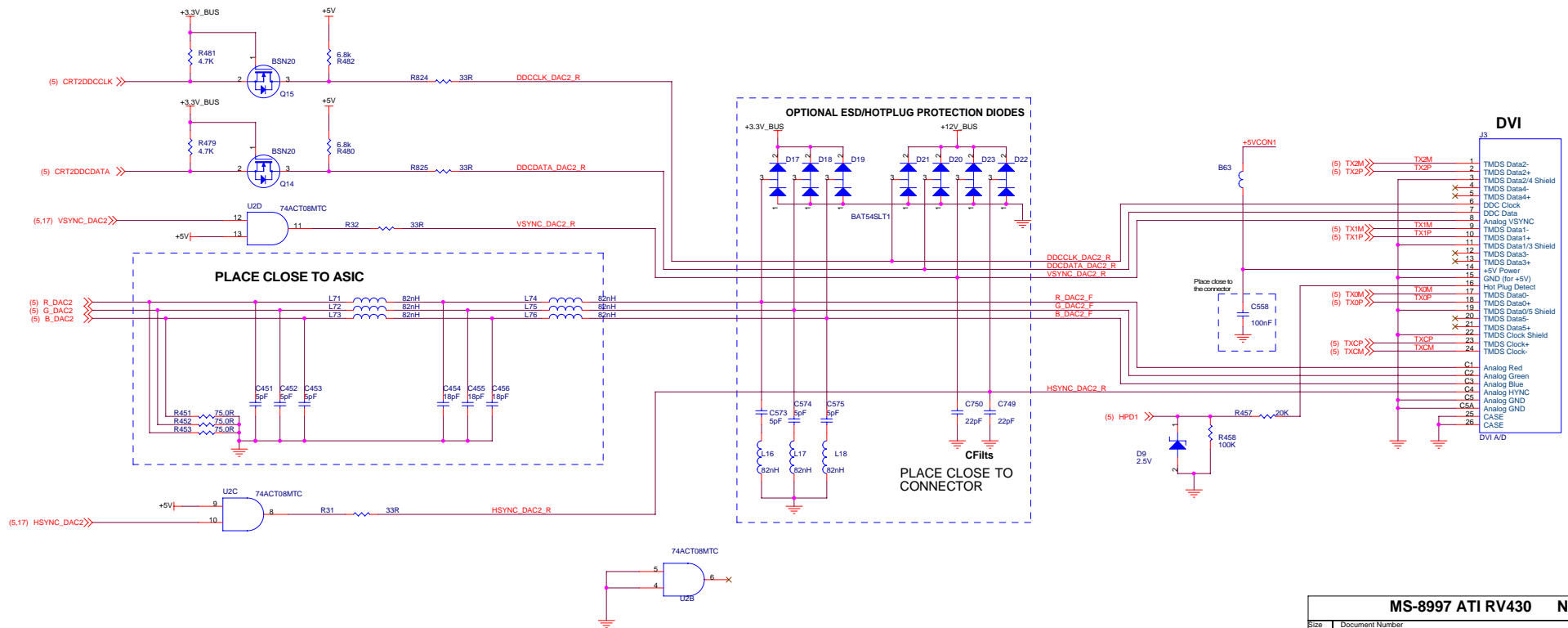
SMART FAN



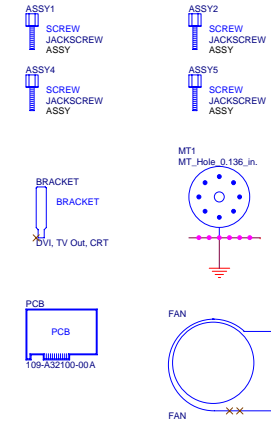
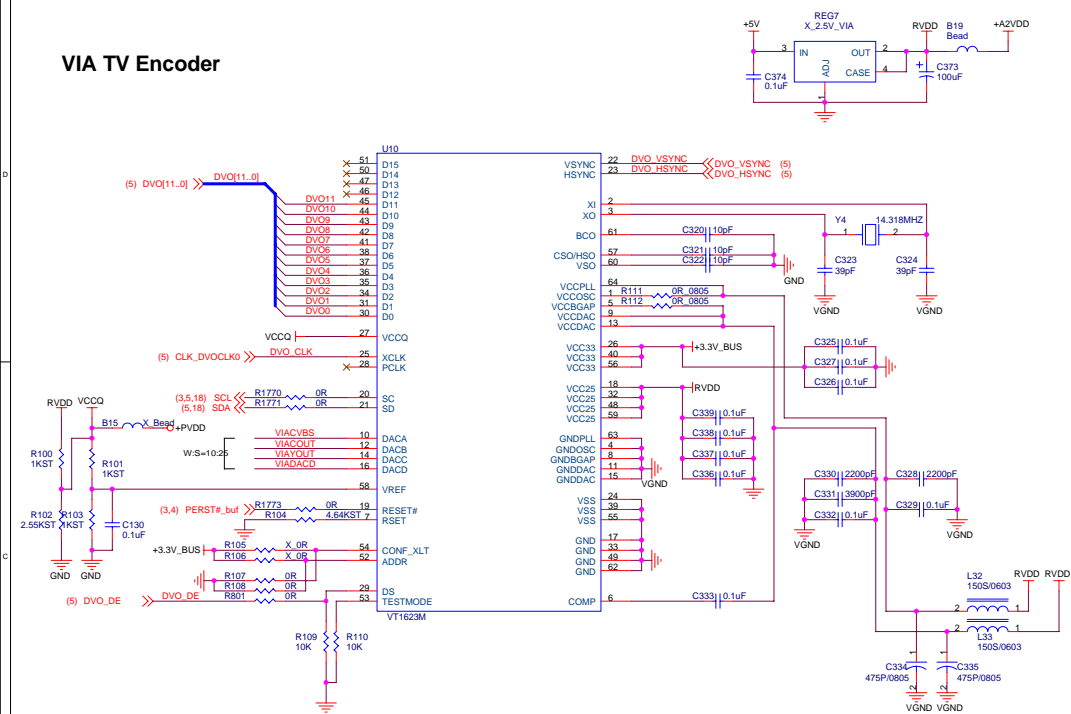
PRIMARY DISPLAY



SECONDARY DISPLAY

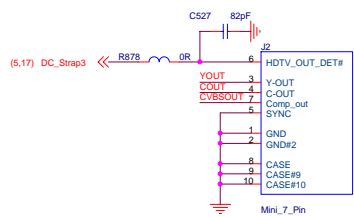
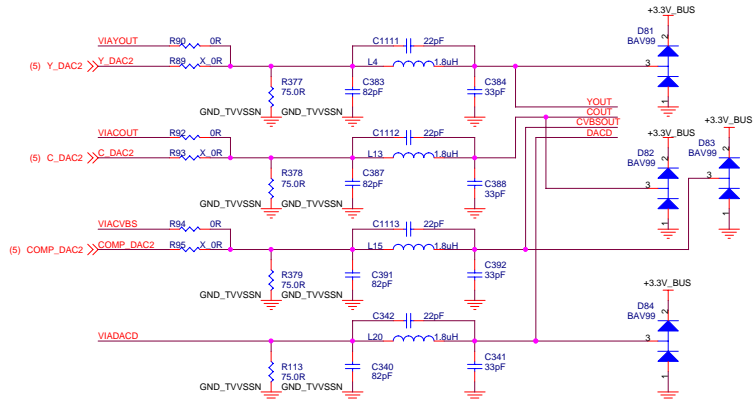


VIA TV Encoder

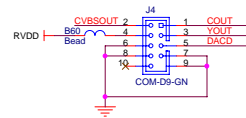


TV-OUT FILTER

TV-OUT from VIA 1623M : install R90, R92, R94 : remove R89, R93, R95
TV-OUT from ATI R400 : remove R90, R92, R94 : install R89, R93, R95



SCART



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C	VIA 1623 (SCART)	100
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