PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI

Tall DVI-I + DP + DP + DP/HDMI + DP

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V320-2.0 change item:

Page15:DVI add esd

Page18:remove DP colay

Page20:HDMI add esd

Page21:4pin housing colay 6pin housing

Page25:NVVDD enable phase4

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Page29:remove colay NVVDD power solution

Page30: 12V input bead change to choke
6pin power con colay 8pin con
remove 0603 MLCC colay

Page32:stuff logo LED

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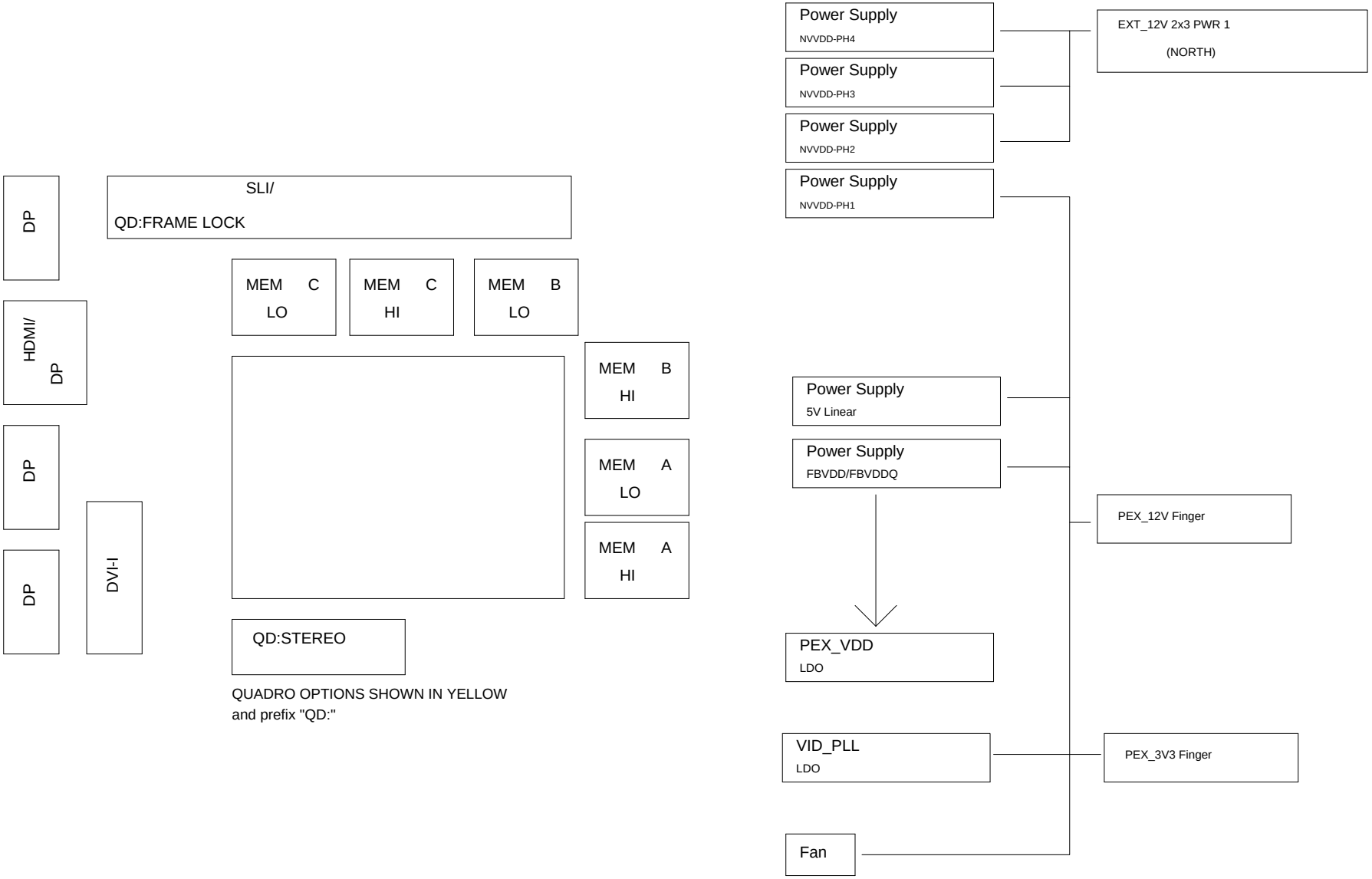
Block Diagram



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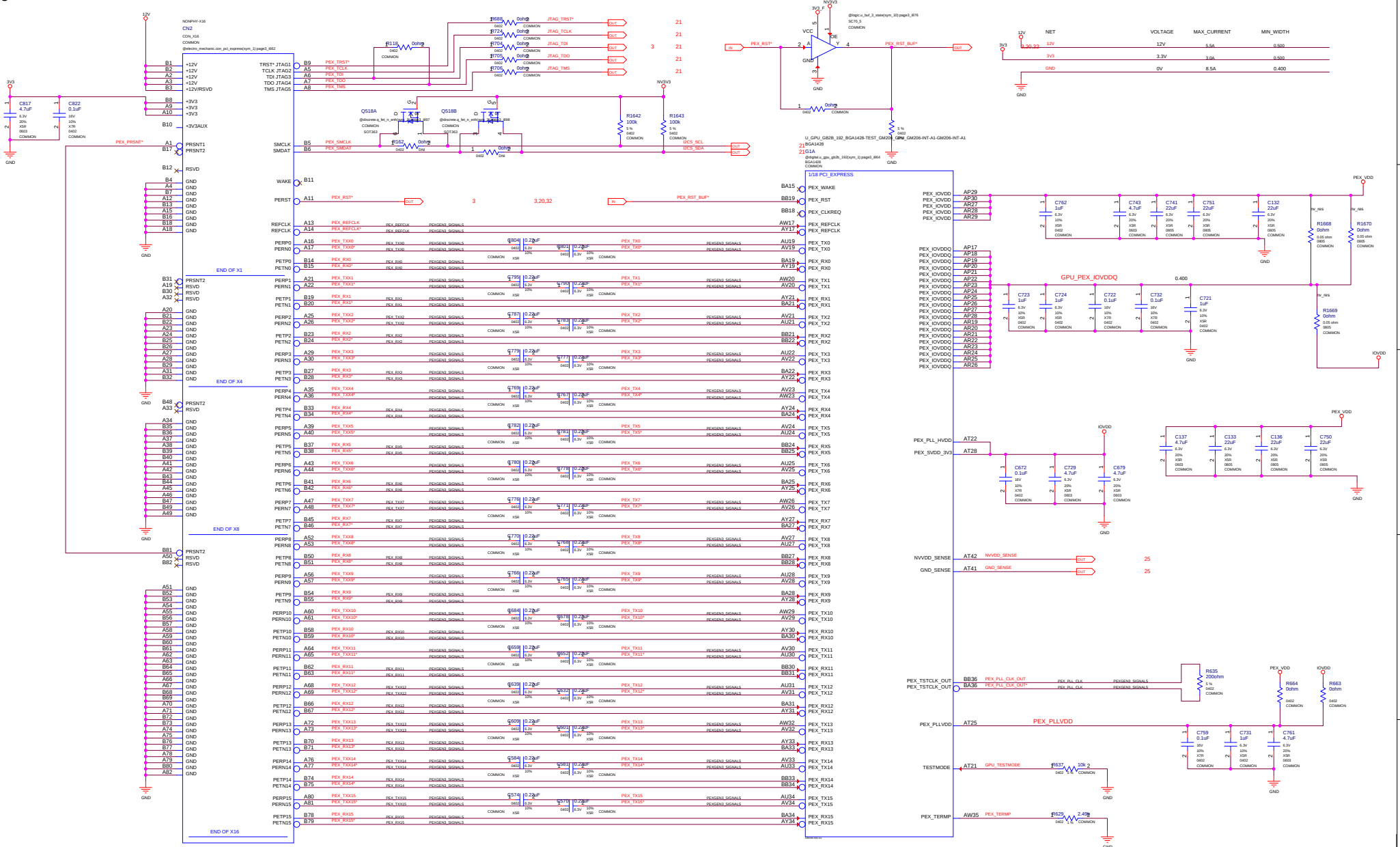
PCI Express



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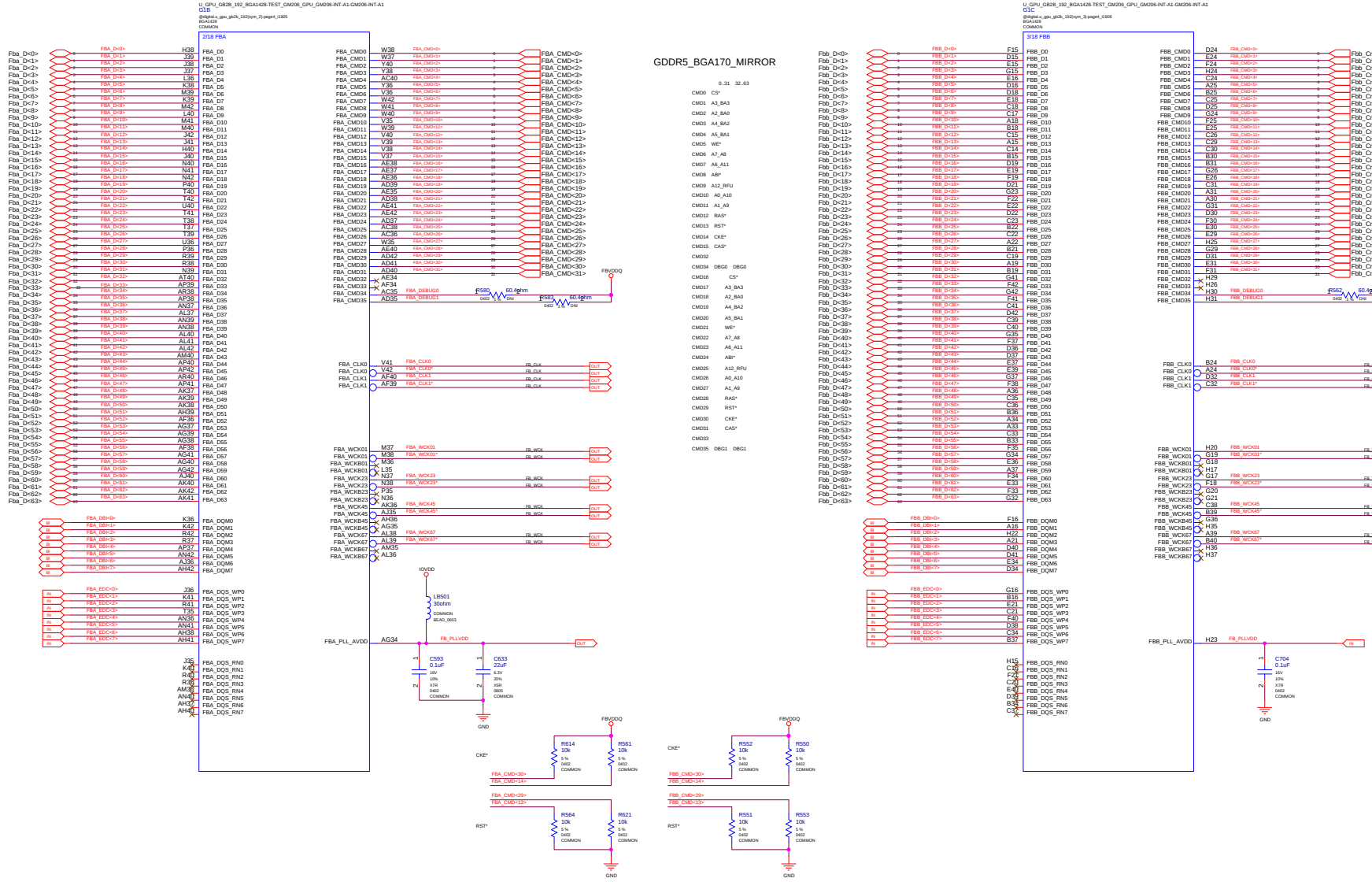
MEMORY: GPU Partition A/B



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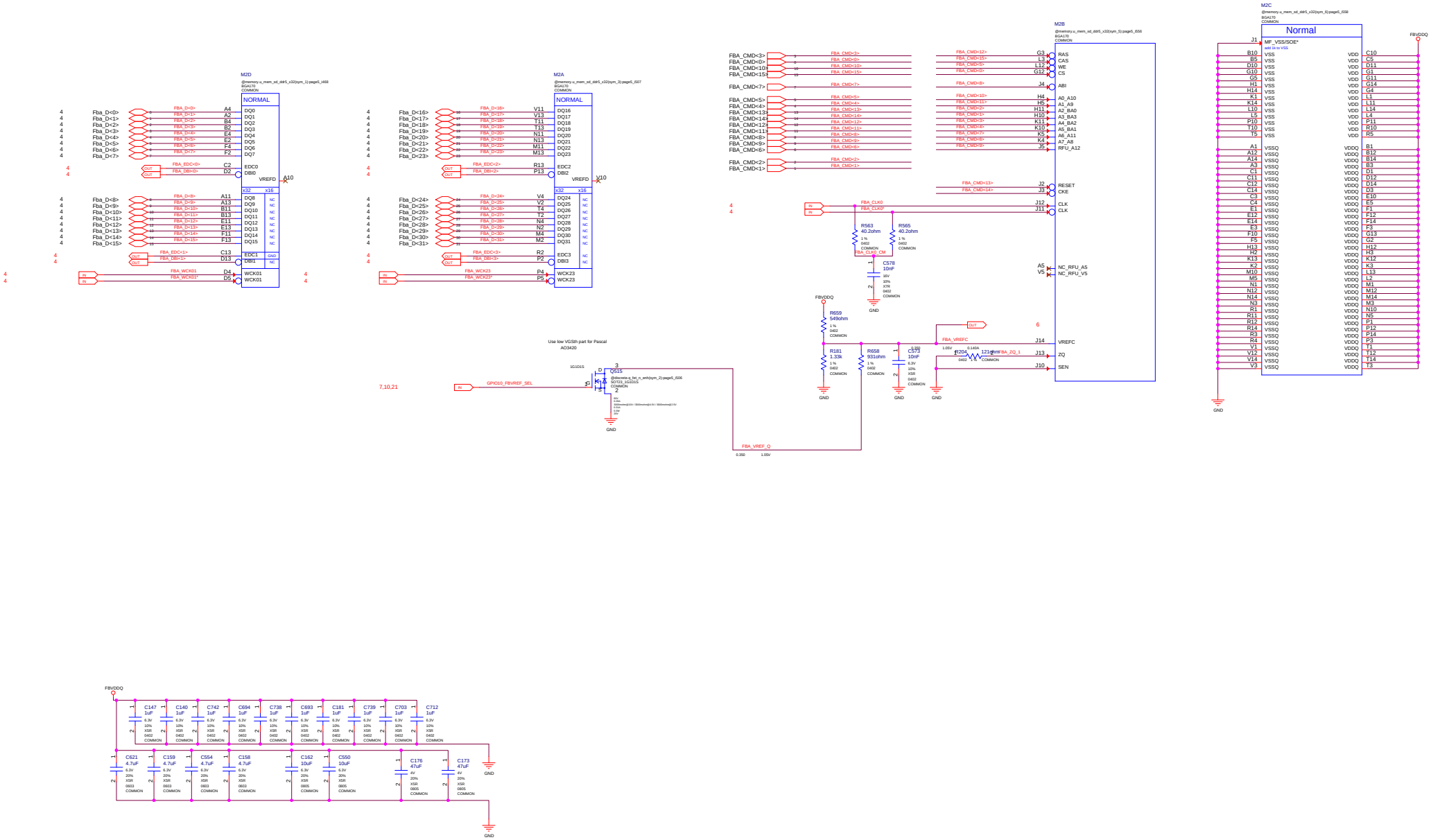
MEMORY: FBA Partition 31..0



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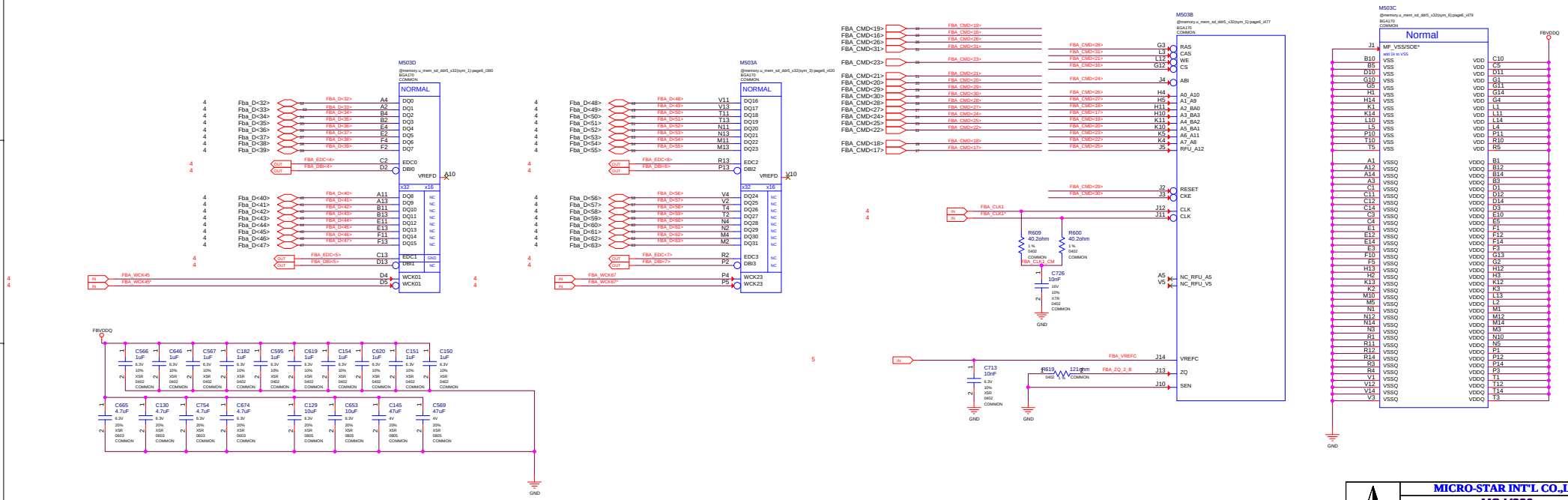
MEMORY: FBA Partition 63..32



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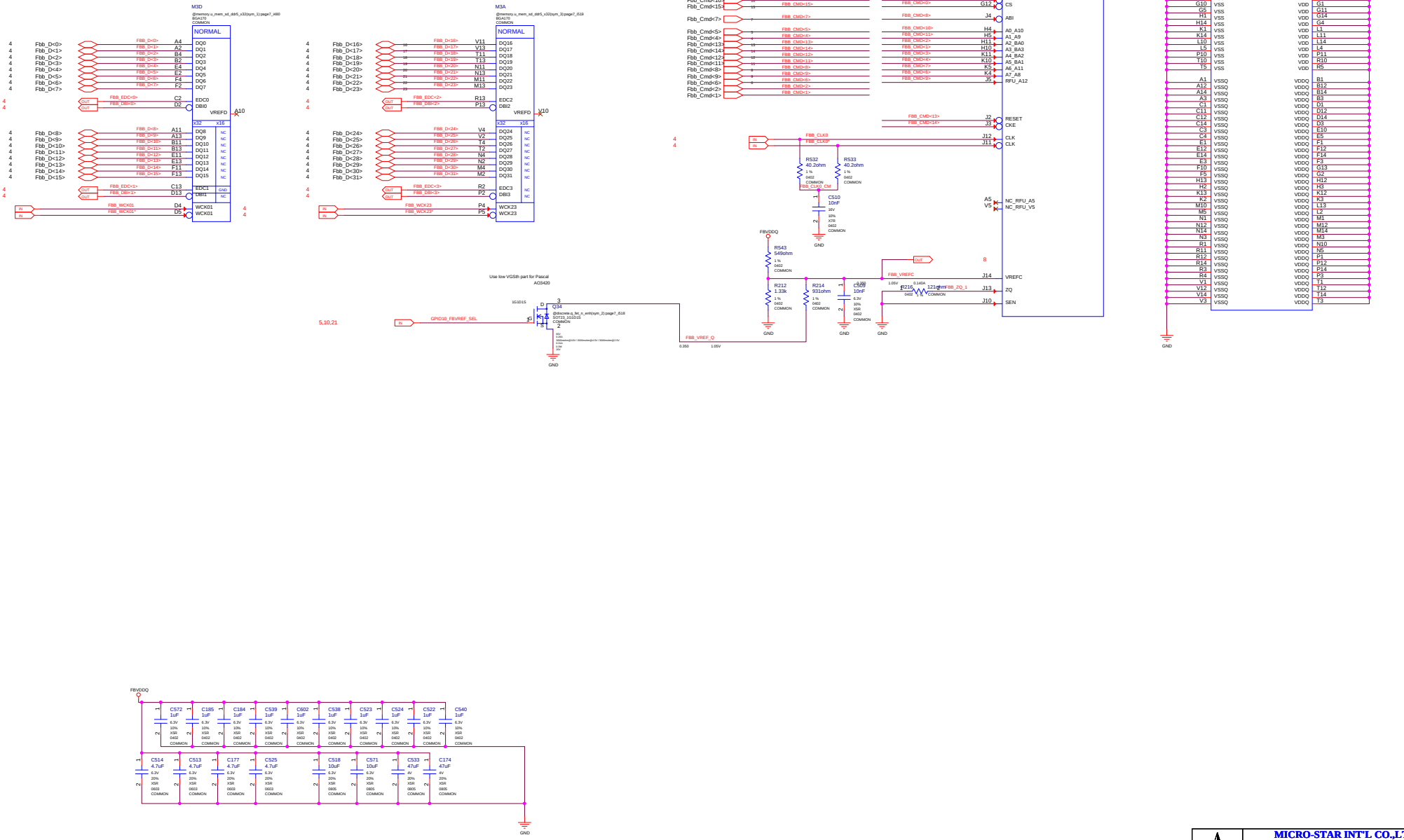

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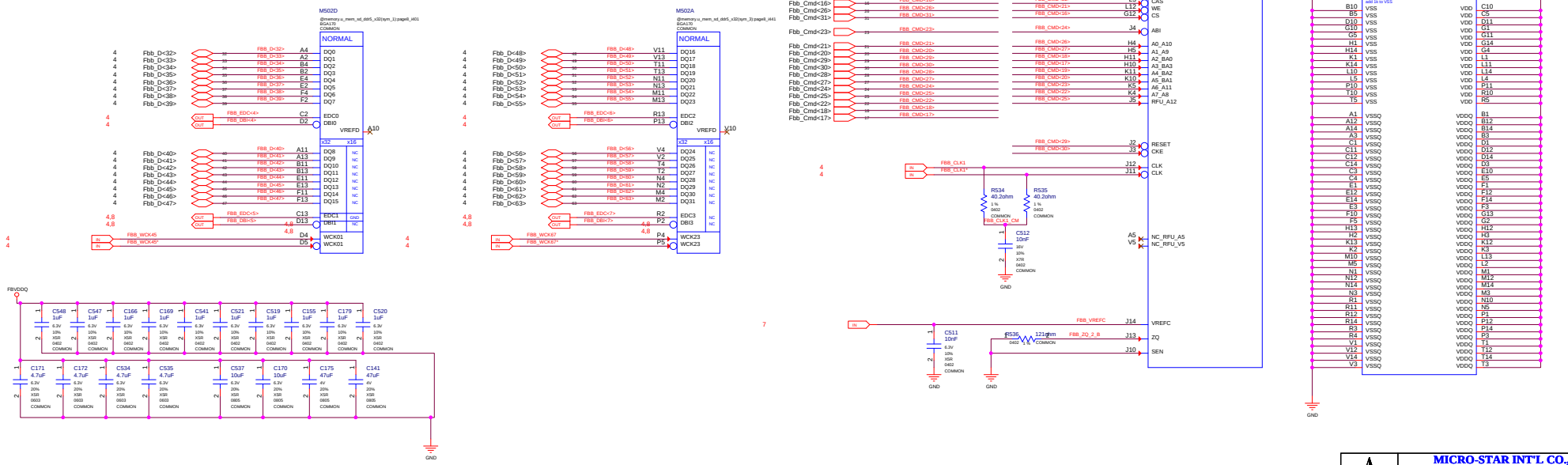
MEMORY: FBB Partition 63..32



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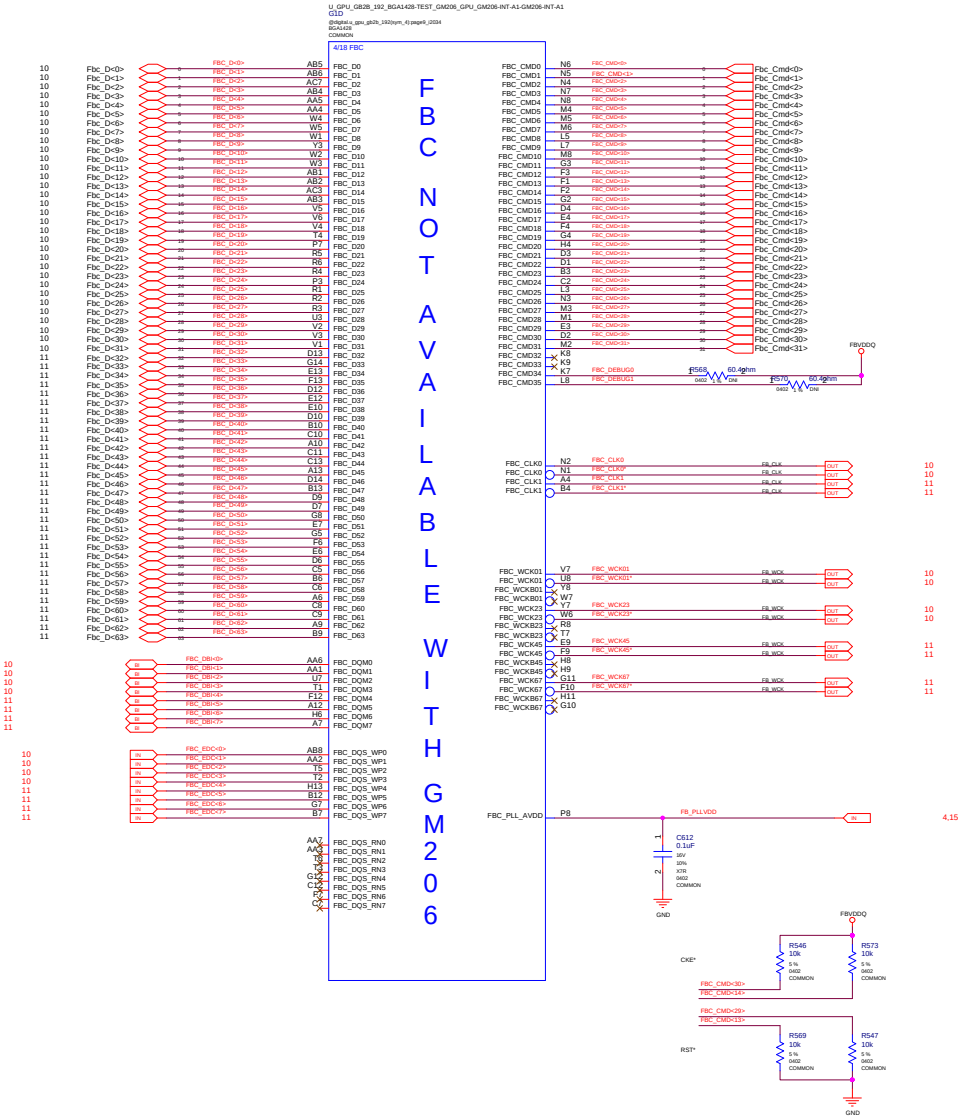
MEMORY: GPU Partition C/D



GDDR5_BGA170_MIRROR

	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD32		
CMD34	DBG0	DBG0
CMD16	CS*	
CMD17	A3_BA3	
CMD18	A2_BA0	
CMD19	A4_BA2	
CMD20	A5_BA1	
CMD21	WE*	
CMD22	A7_A8	
CMD23	A6_A11	
CMD24	ABI*	
CMD25	A12_RFU	
CMD26	A0_A10	
CMD27	A1_A9	
CMD28	RAS*	
CMD29	RST*	
CMD30	CKE*	
CMD31	CAS*	
CMD33		
CMD35	DBG1	DBG1

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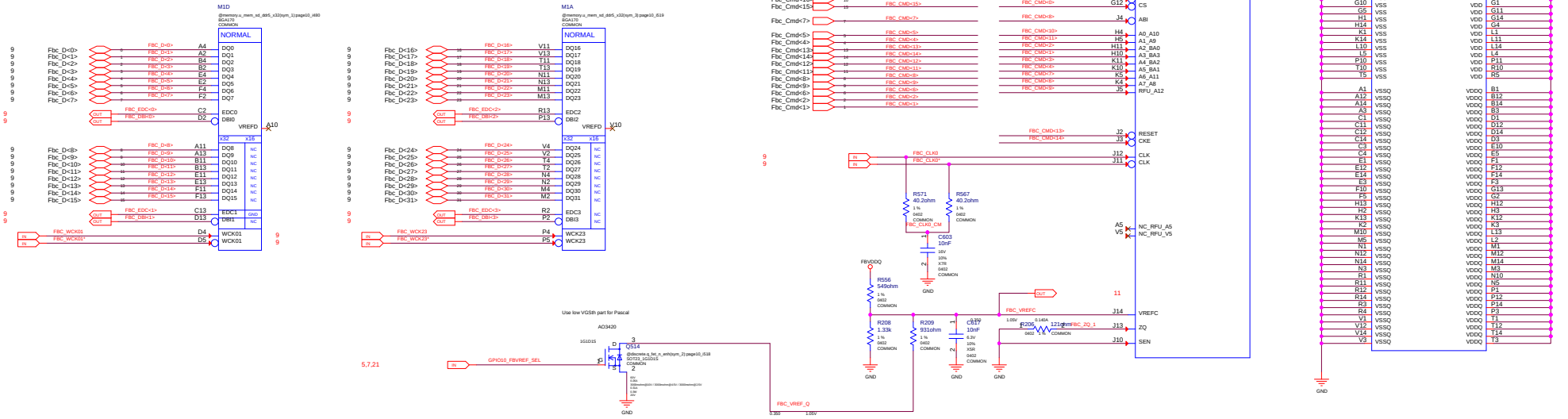
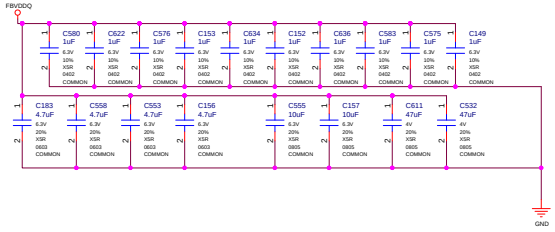
MEMORY: FBC Partition 31..0





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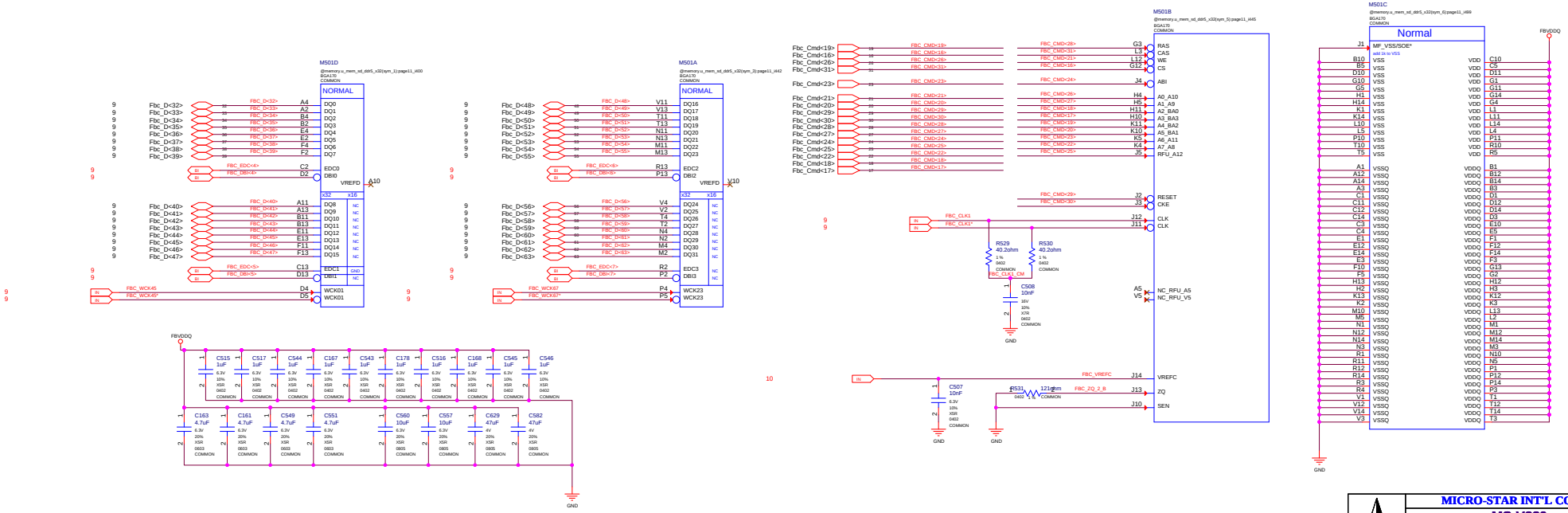

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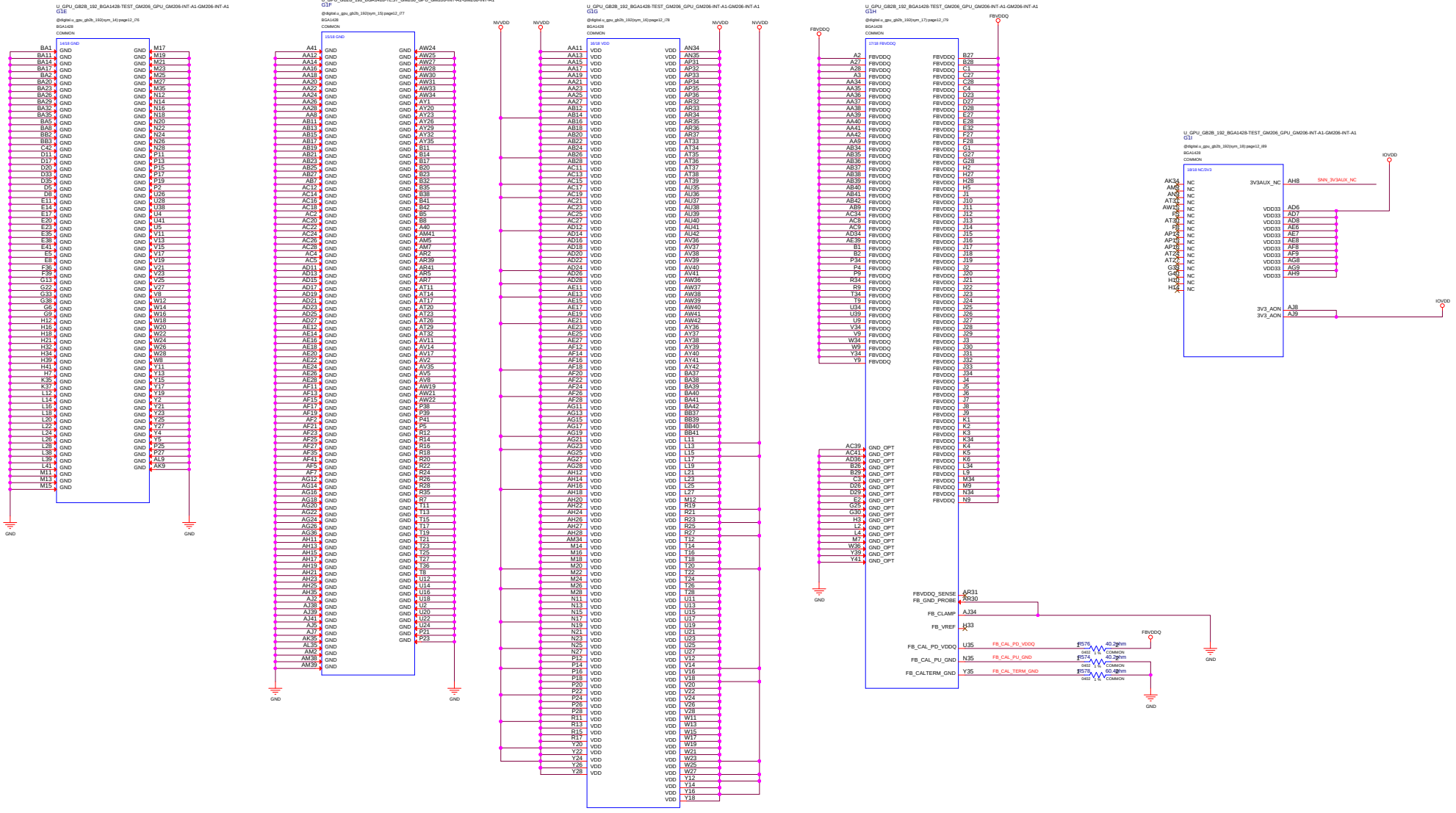
GPU PWR and GND



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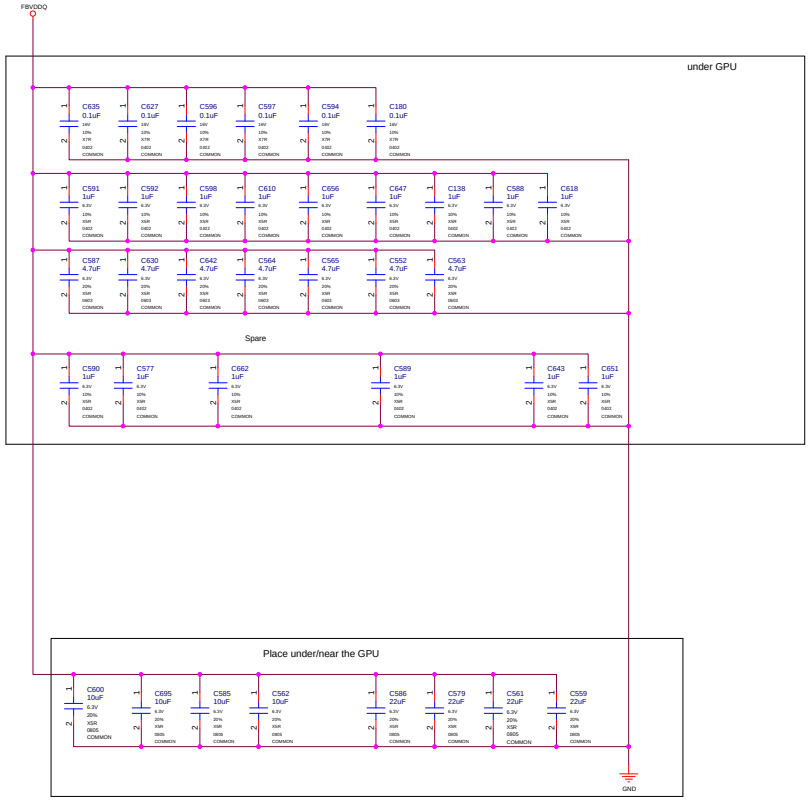
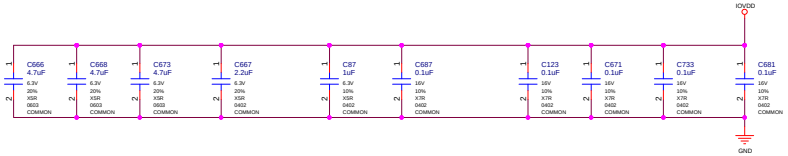
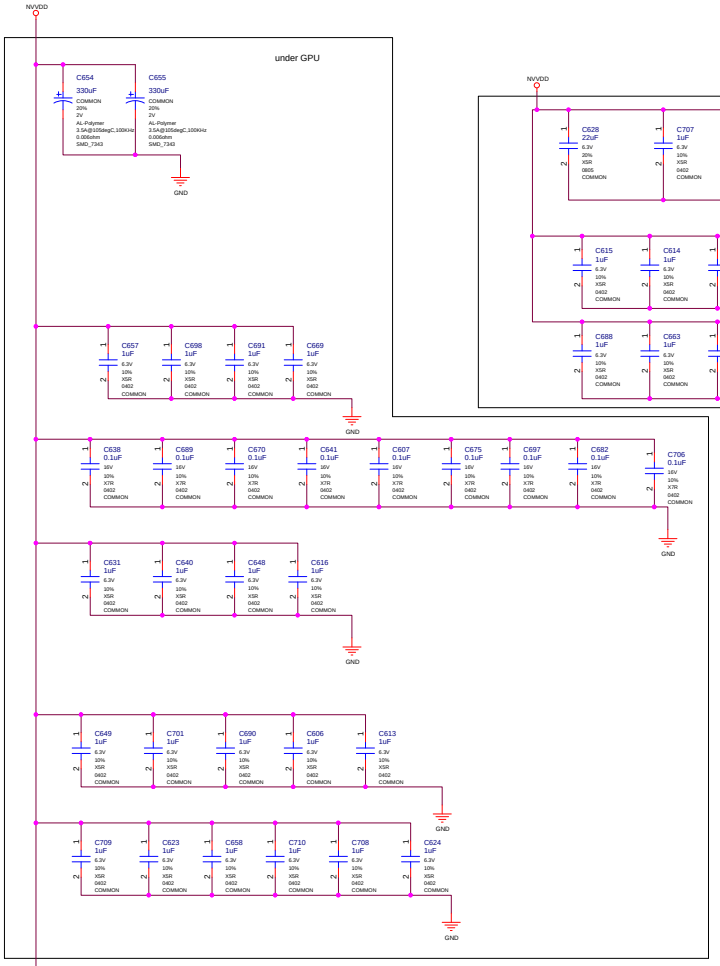
GPU Decoupling

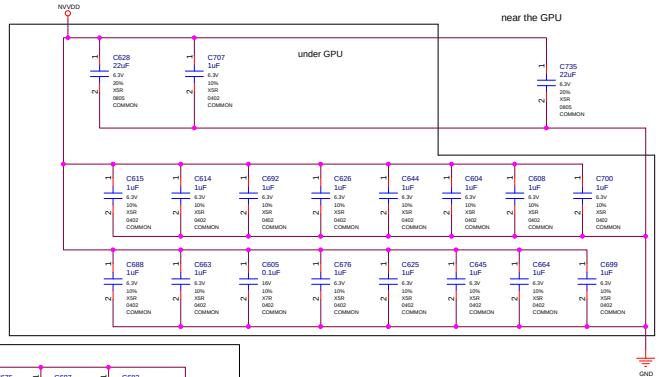
FBVDDQ

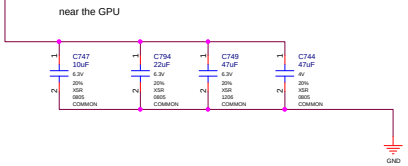




NVVDD







	Under GPU	Near GPU
NVVDD	90uF + 1x 330uF	88uF
SVVDD	32uF	22uF
Combined (Maxwell)	122uF + 1x 330uF	110uF

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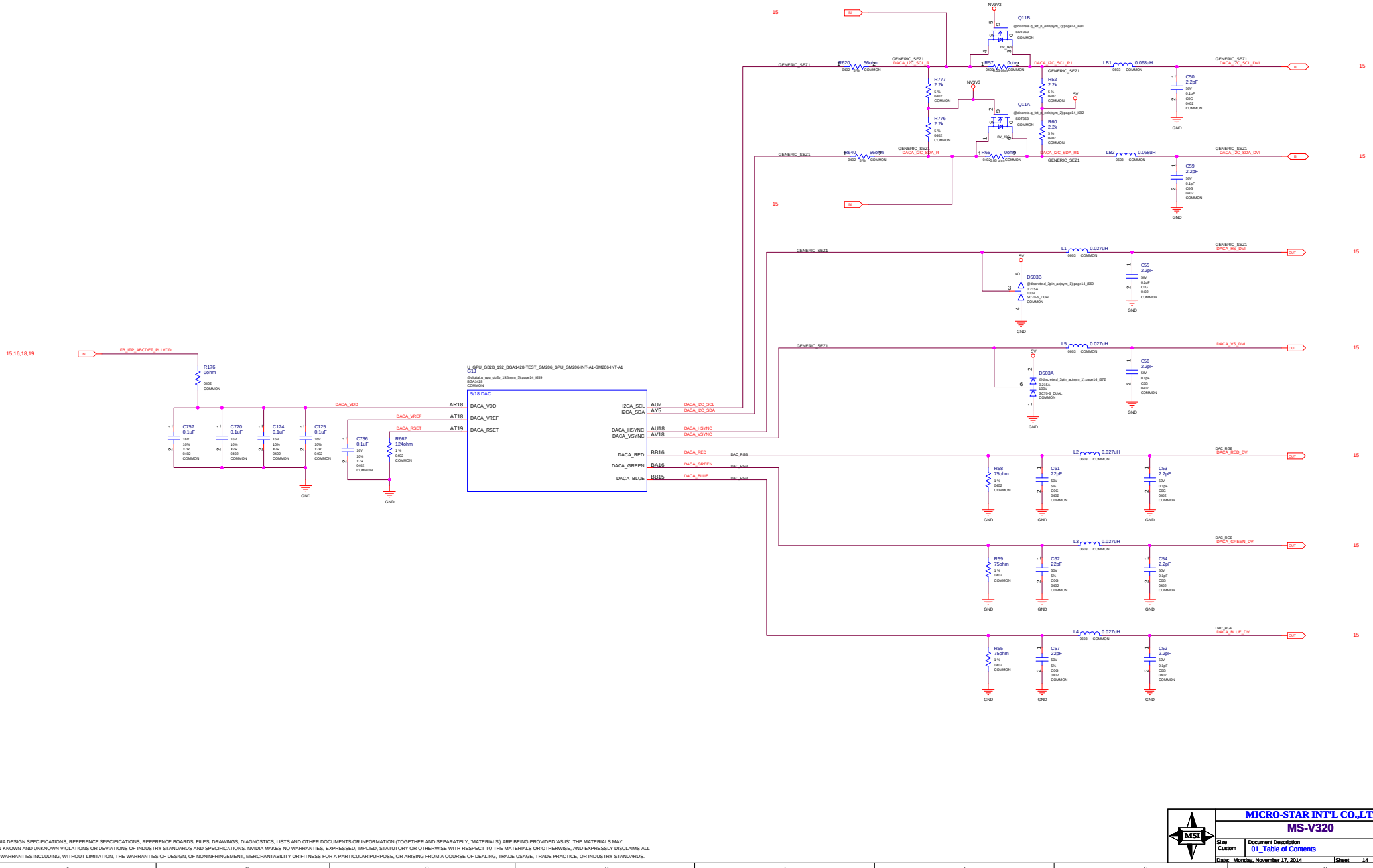
DACA Interface



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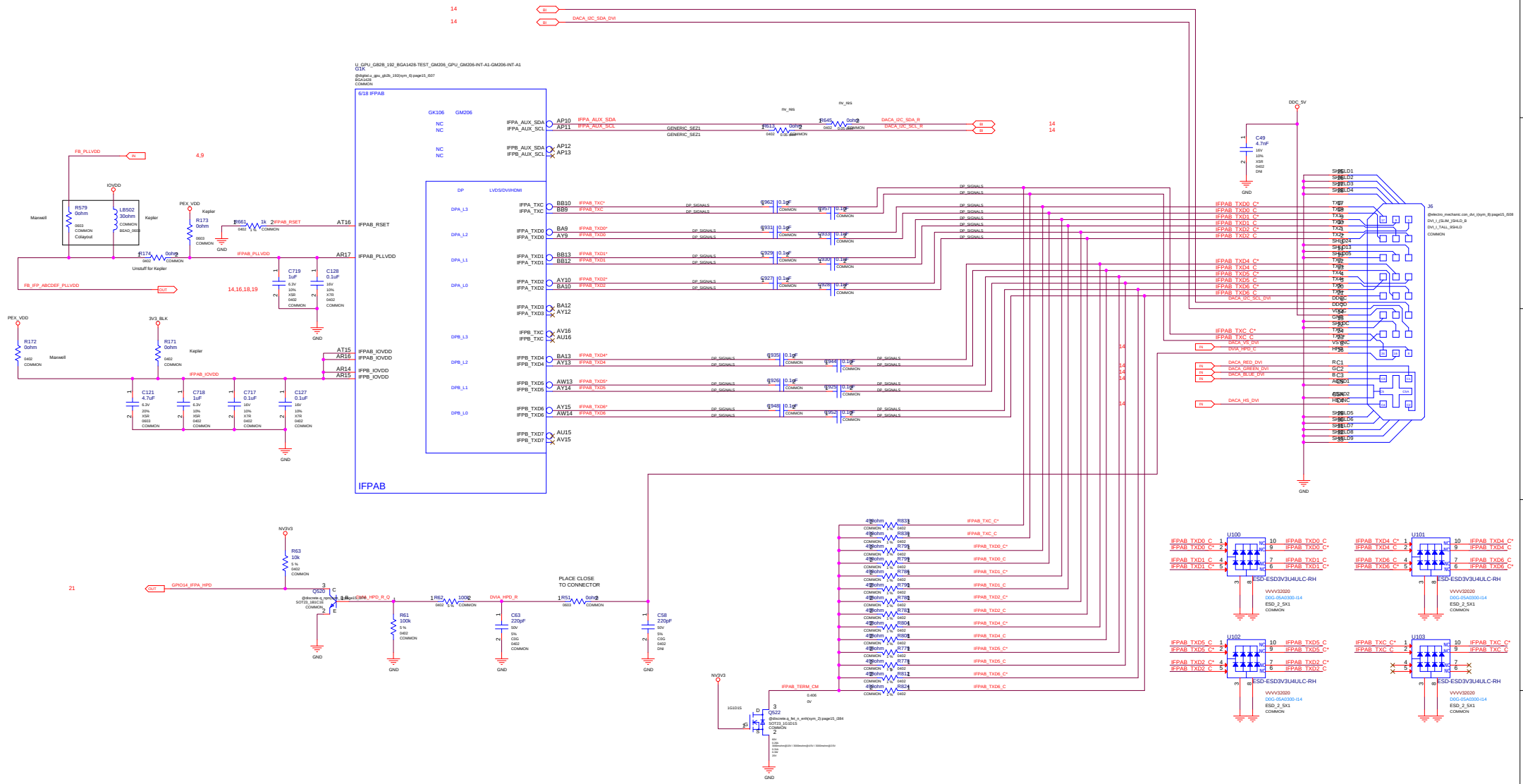
IFPAB DVI-I-DL



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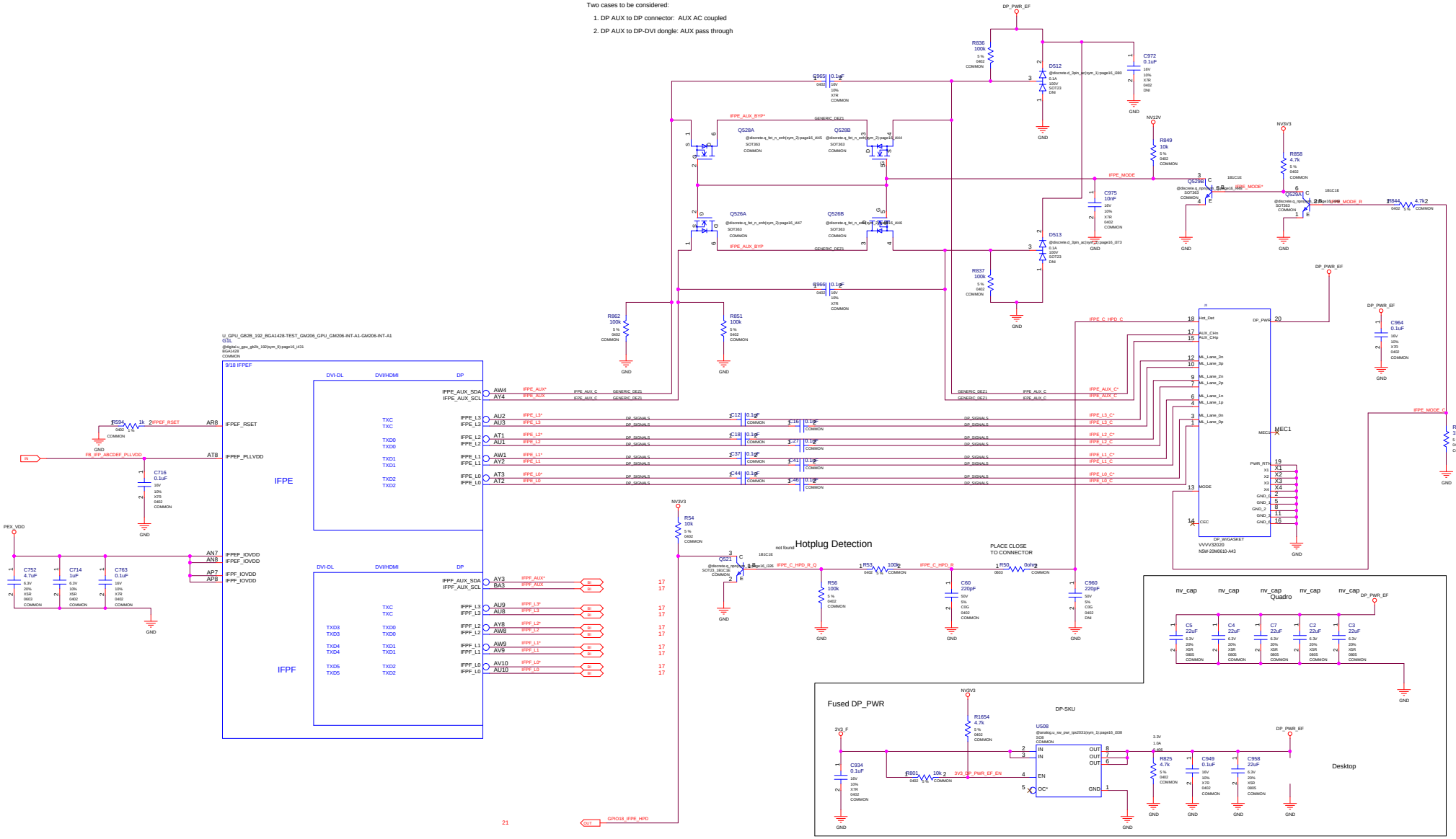
Page18: IFPEF with IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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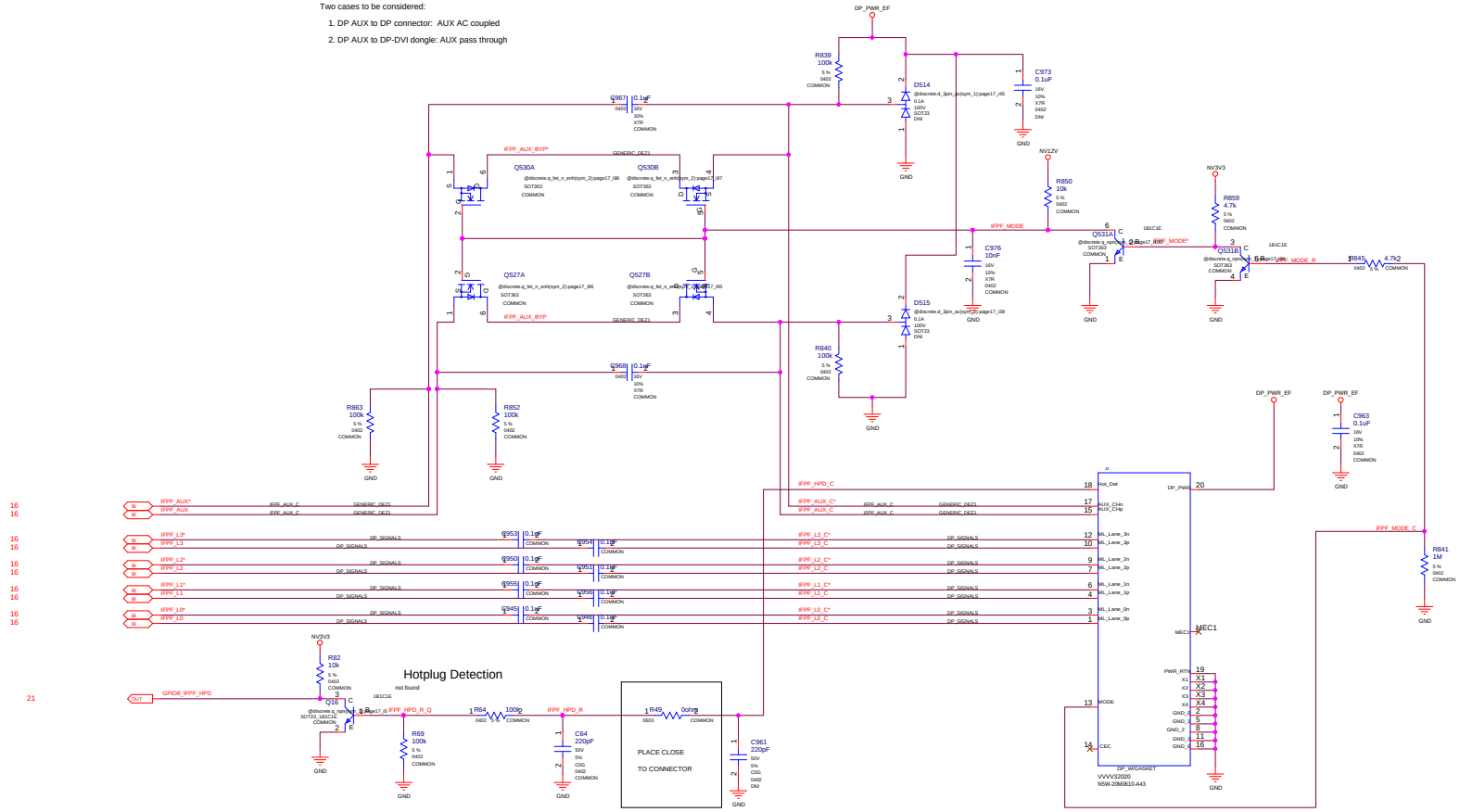
IFPF DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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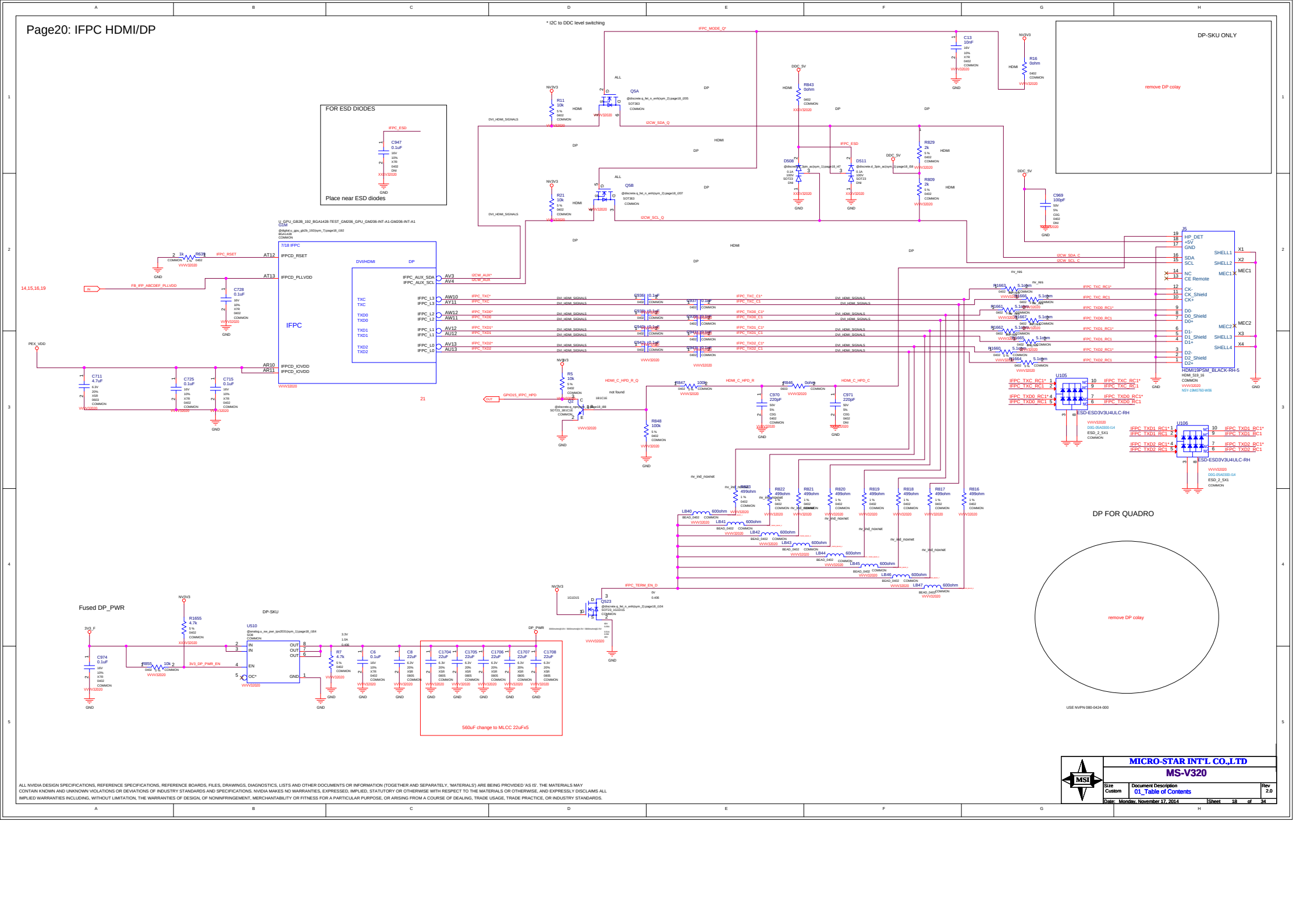
Page20: IFPC HDMI/DP



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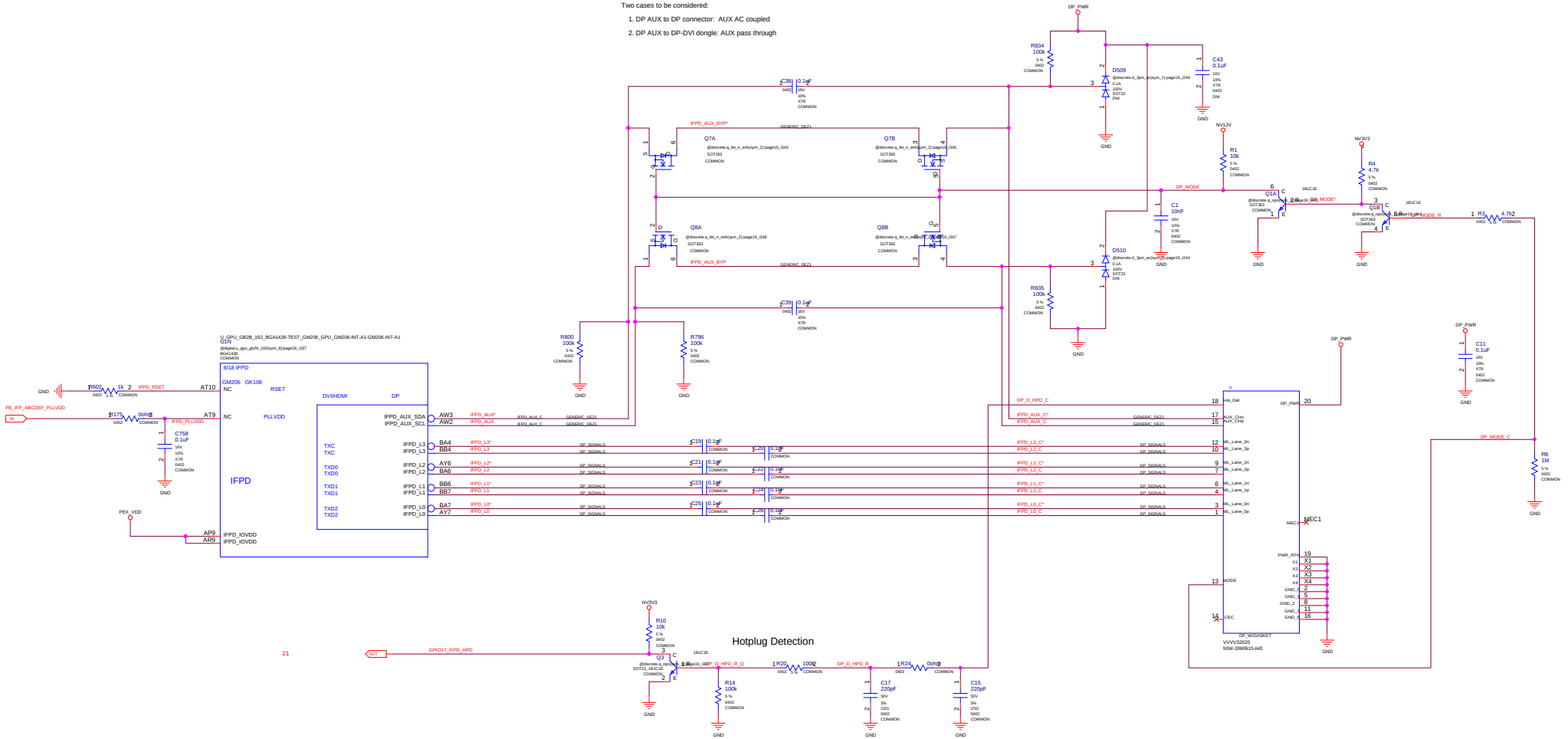
IFPD DP



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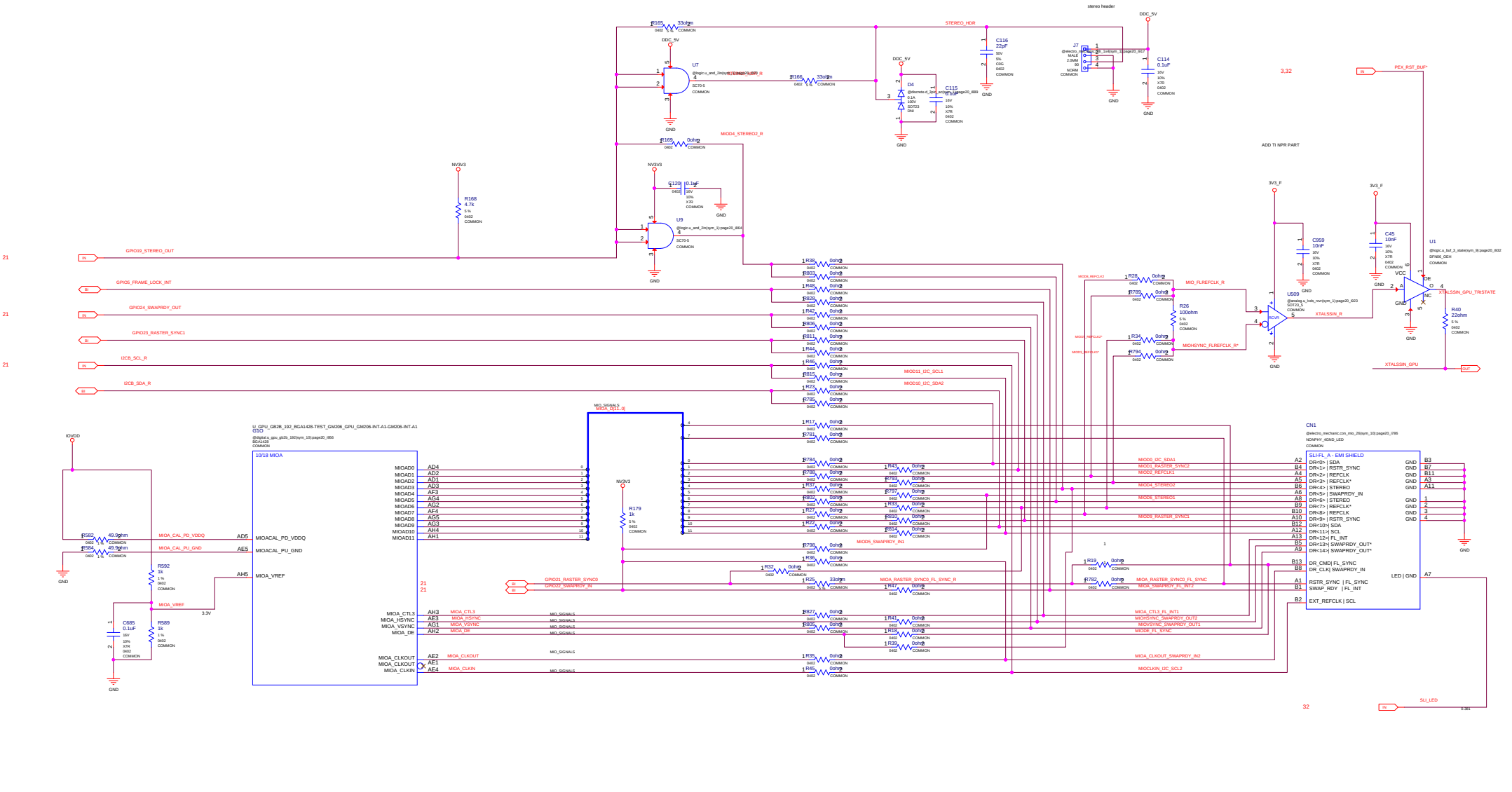
MIOA/SLI Interface



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	3.3V		0.305
MIOA_CAL_PD_VDDQ	2.5V		0.305
MIOA_CAL_PU_GND	0.0V		0.305

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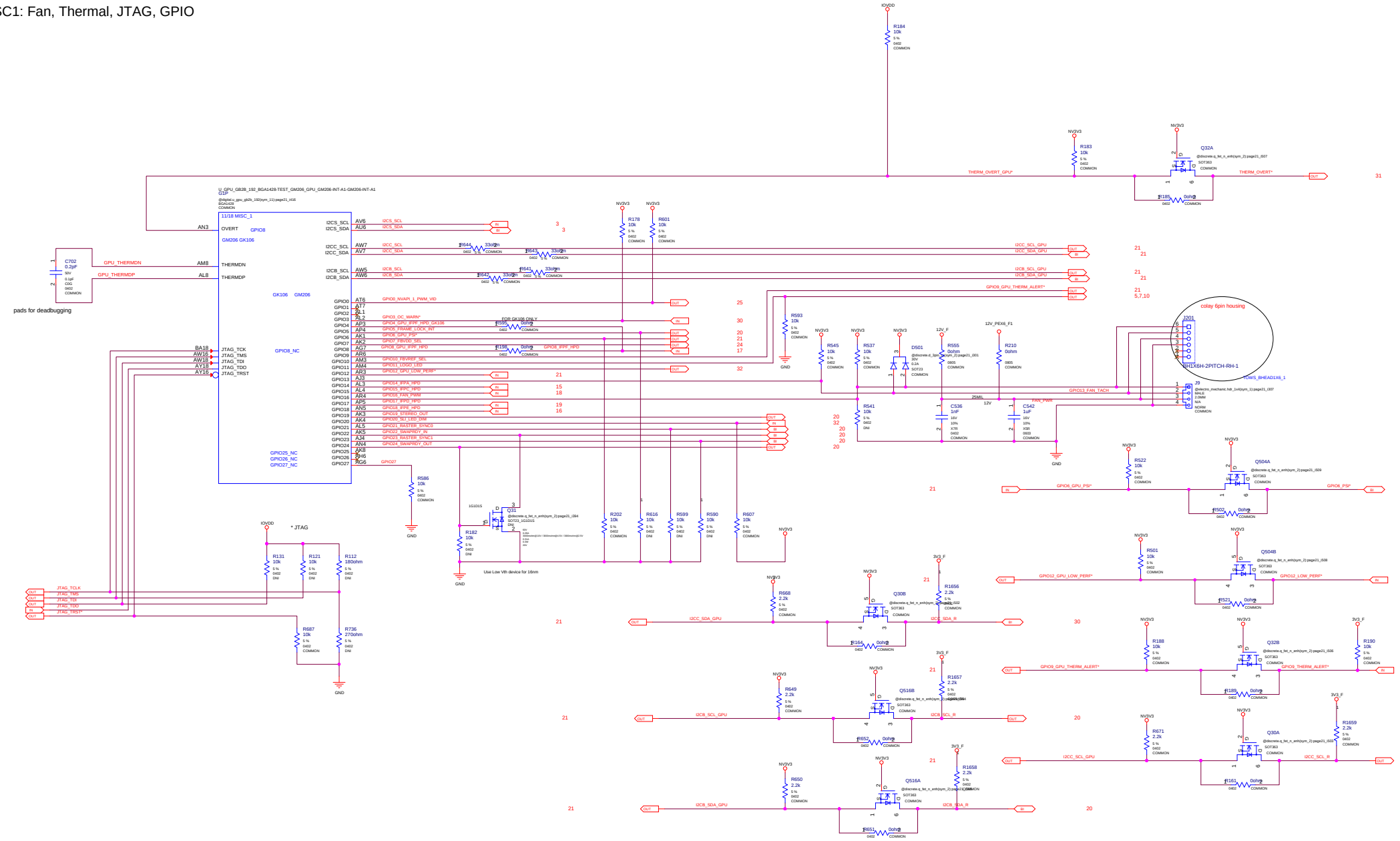
MISC1: Fan, Thermal, JTAG, GPIO



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MISC2: ROM, XTAL, Straps

	KEPLER	MAXWELL
STRAP0	USER_BIT [3:0]*	
STRAP1	3GIO_PADCFG_LUT_ADR*	
STRAP2	PCI_DEVID [3:0]*	
STRAP3	SOR_EXPOSED [3:0]*	
STRAP4	DP_PLL_VDD_33V*	
	PEX_MAX_SPEED*	
	PEX_SPD_CHANGE_GEN3*	
	*	
ROM_SI	RAMCFG[0]*	RAMCFG[0]*
	RAMCFG[1]*	RAMCFG[1]*
	RAMCFG[2]*	RAMCFG[2]*
	RAMCFG[3]*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	VGA_DEVICE*
	SMB_ALT_ADDR*	SMB_ALT_ADDR*
	FB[0]_APERTURE_SIZE*	PCIE_CFG*
	FB[1]_APERTURE_SIZE*	DEVID_SEL*
ROM_SCLK	PEX_PLL_EN_TERM100*	SOR0_EXPOSED*
	PCI_DEVID_EXT[5]*	SOR1_EXPOSED*
	SUB_VENDOR*	SOR2_EXPOSED*
	PCI_DEVID_EXT[4]*	SOR3_EXPOSED*

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

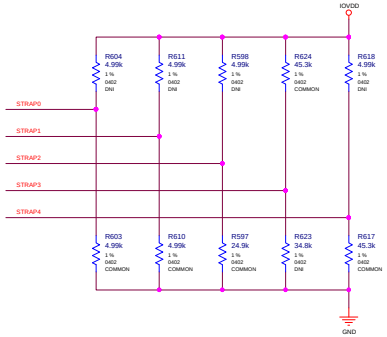
MULTI_STRAP_REF0_GND

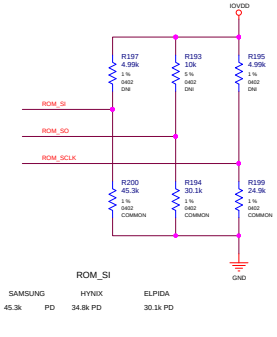
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND

MAXWELL

STRAP0

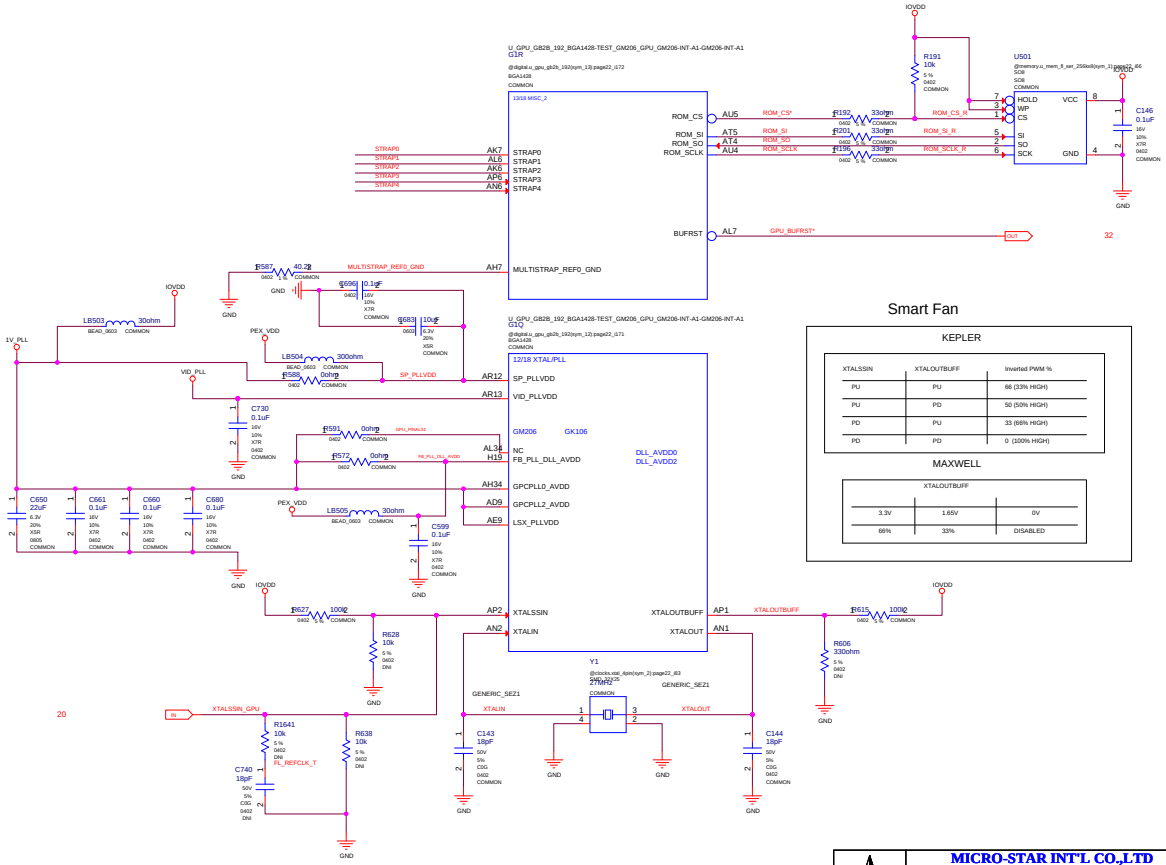
3.3V	1.65V	0V
GC6+ ISLAND ENABLED	GC6+ DEBUG MODE	GC6+ ISLAND DISABLED





ROM_SI

SAMSUNG	HYNIX	ELPIDA
45.3k	PD 34.8k PD	30.1k PD



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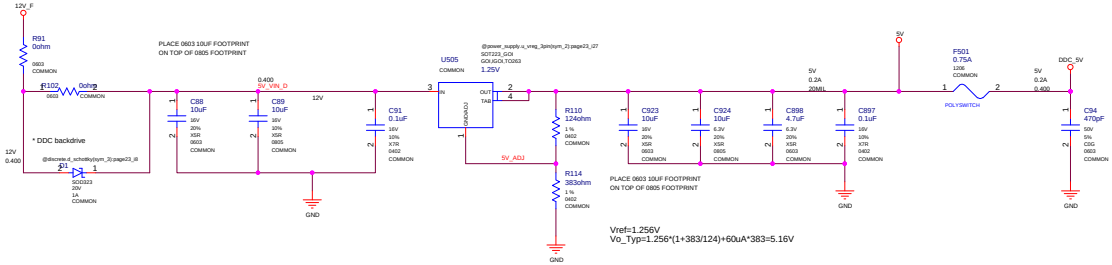
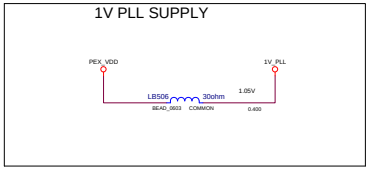
PS: 5V, PEX_VDD

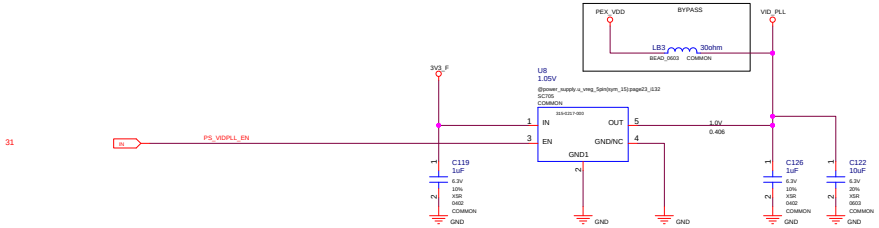
5V / DDC SUPPLY



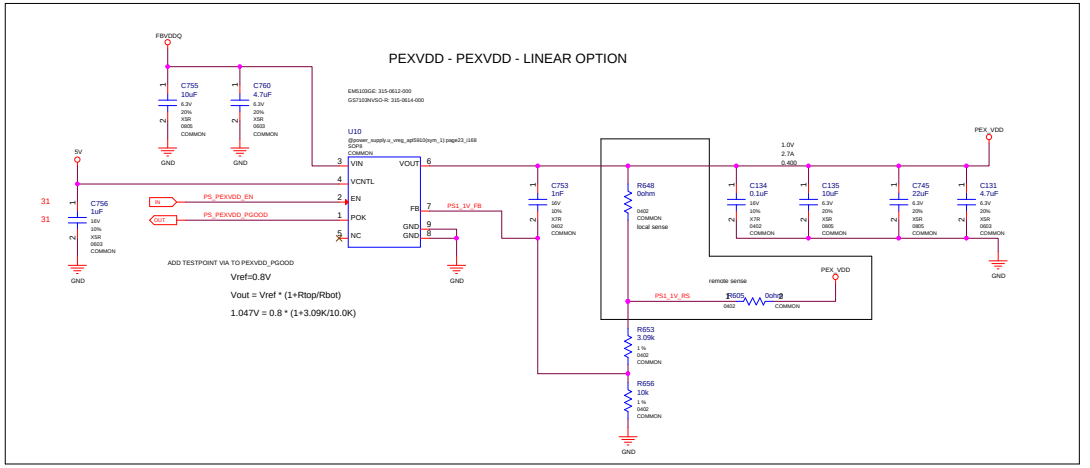
1V PLL SUPPLY



VID PLL SUPPLY



PEXVDD - PEXVDD - LINEAR OPTION



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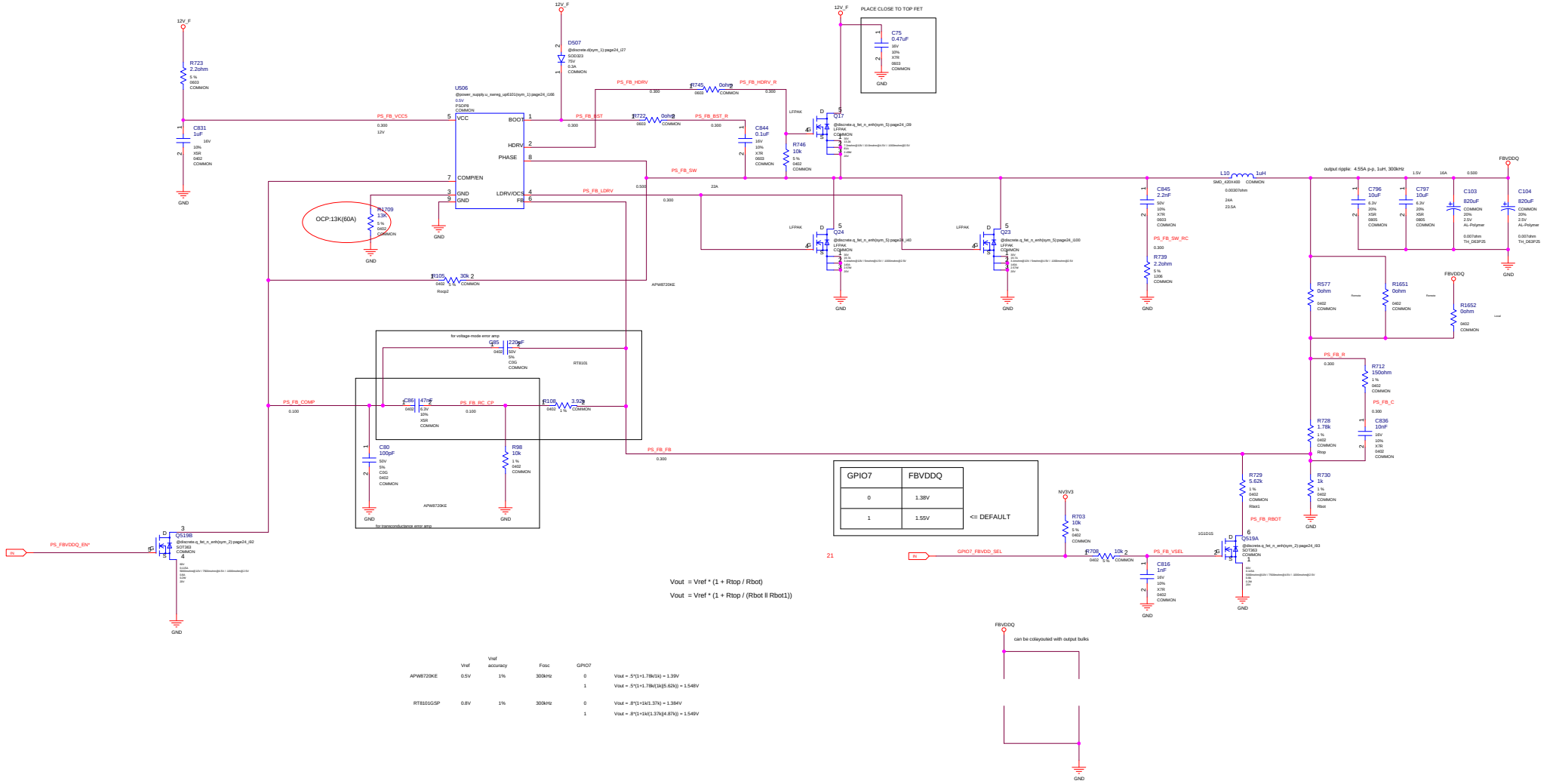
PS: FBVDDQ



GPIO7	FBVDDQ	
0	1.38V	
1	1.55V	<= DEFAULT

Vout = Vref * (1 + Rtop / Rbot)

Vout = Vref * (1 + Rtop / (Rbot ll Rbot1))

	Vref	Vref accuracy	Fosc	GPIO7	
APW8720KE	0.5V	1%	300kHz	0	Vout = .5*(1+1.78k/1k) = 1.39V
				1	Vout = .5*(1+1.78k/(1k||5.62k)) = 1.548V
RT8101GSP	0.8V	1%	300kHz	0	Vout = .8*(1+1k/1.37k) = 1.384V
				1	Vout = .8*(1+1k/(1.37k||4.87k)) = 1.549V

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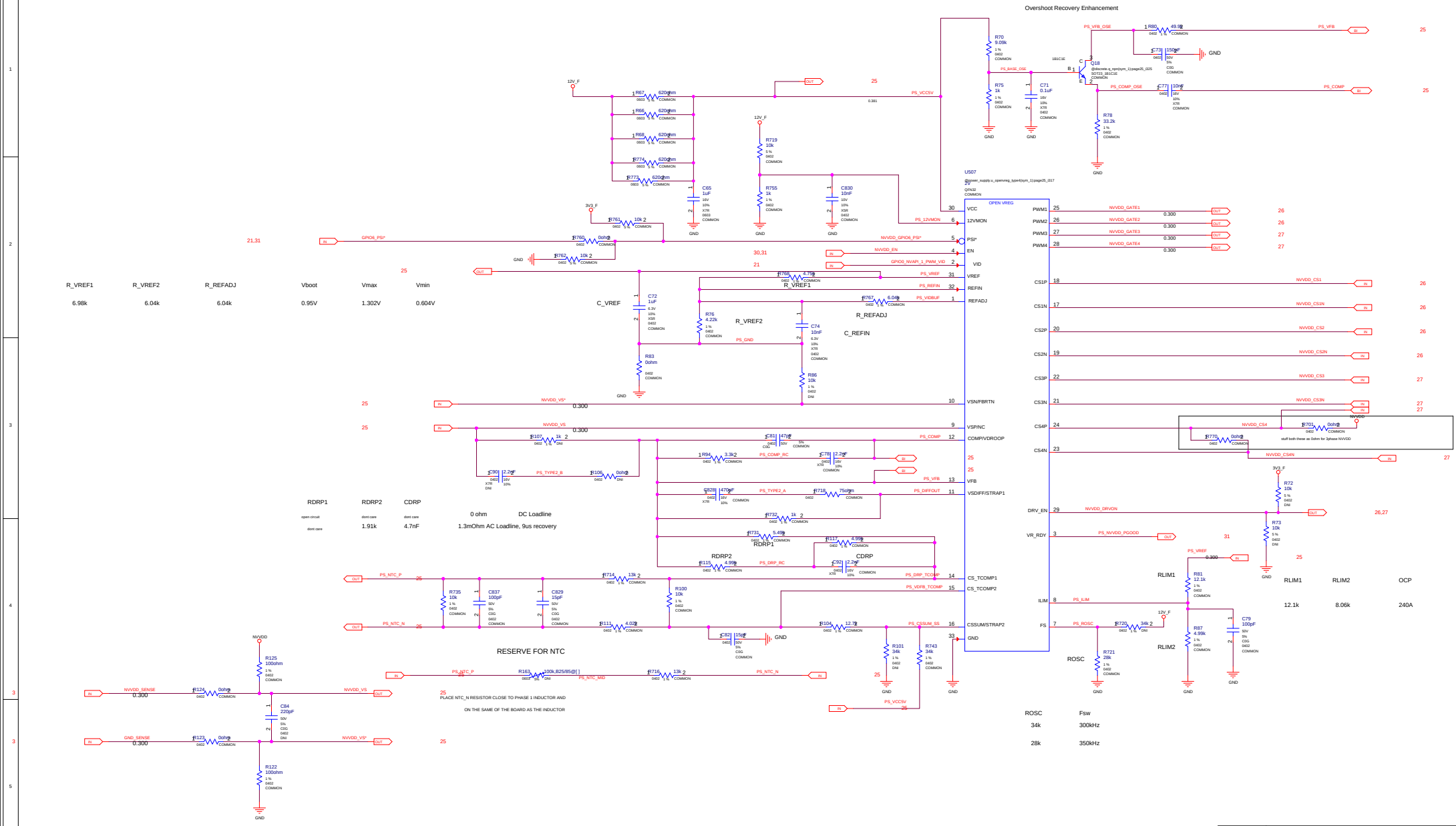
PS: NVVDD Controller



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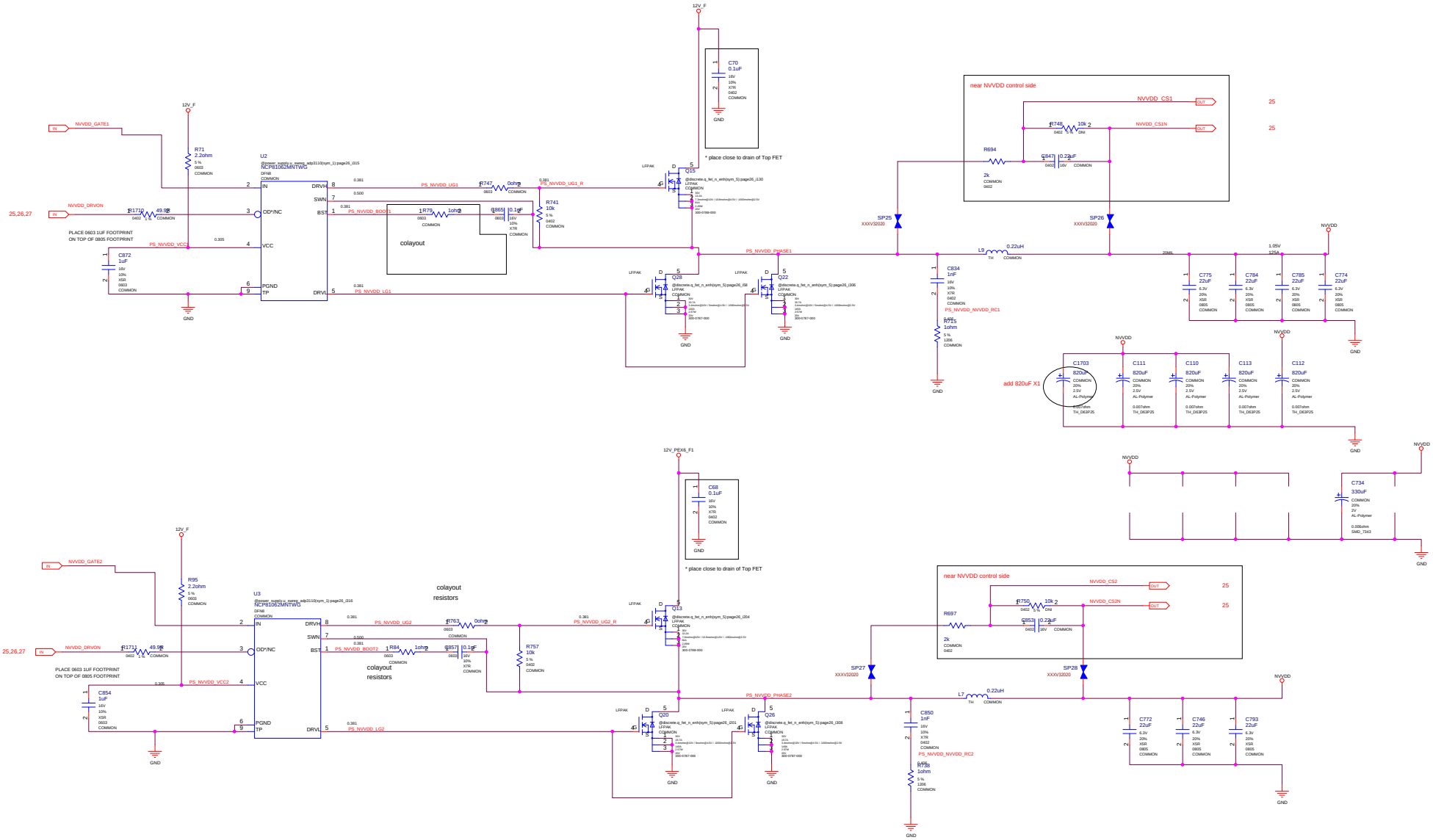
PS: NVVDD Phase 1,2



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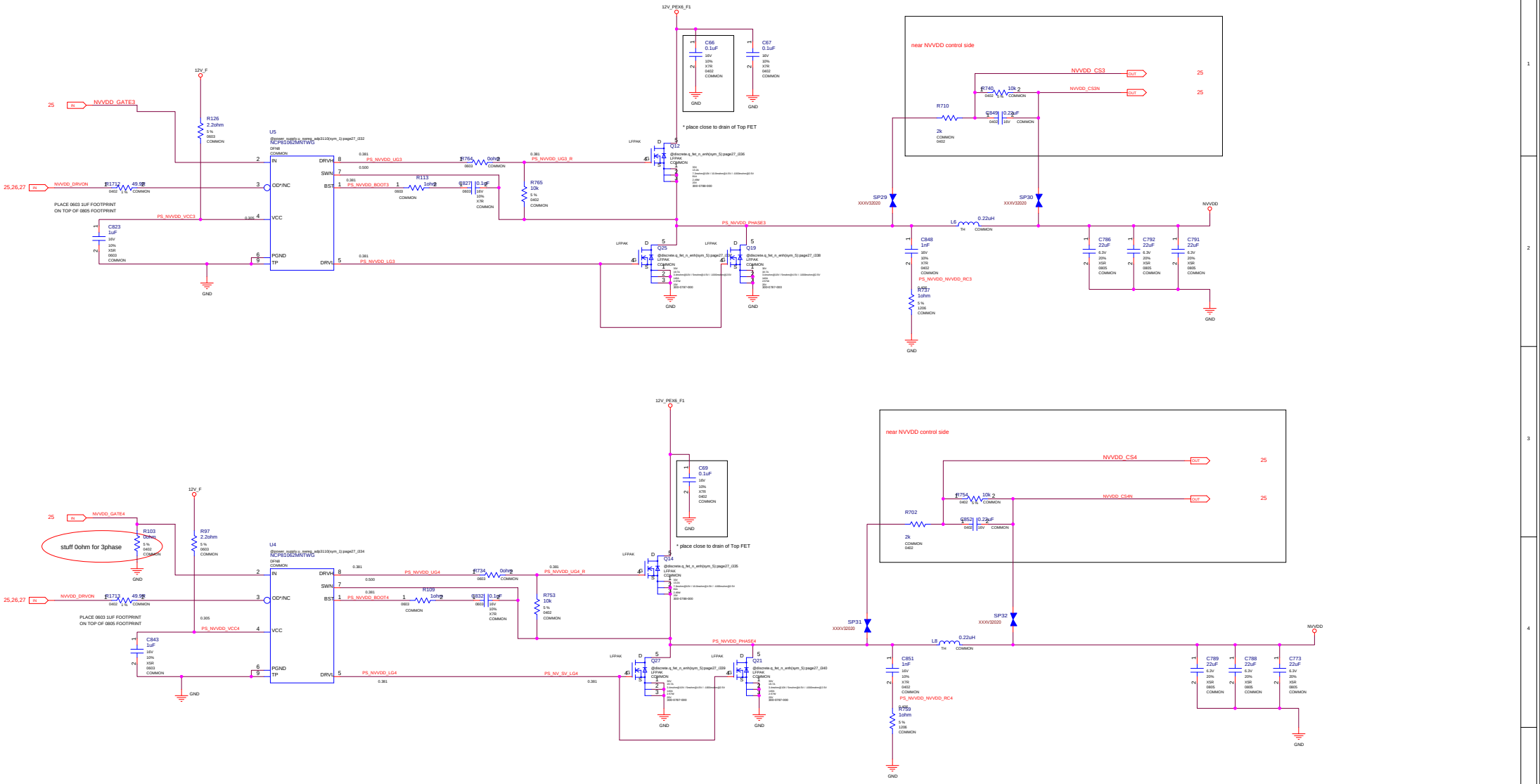
PS: NVVDD Phase 3,4



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PS: NVVDD OVR2+1 POWER

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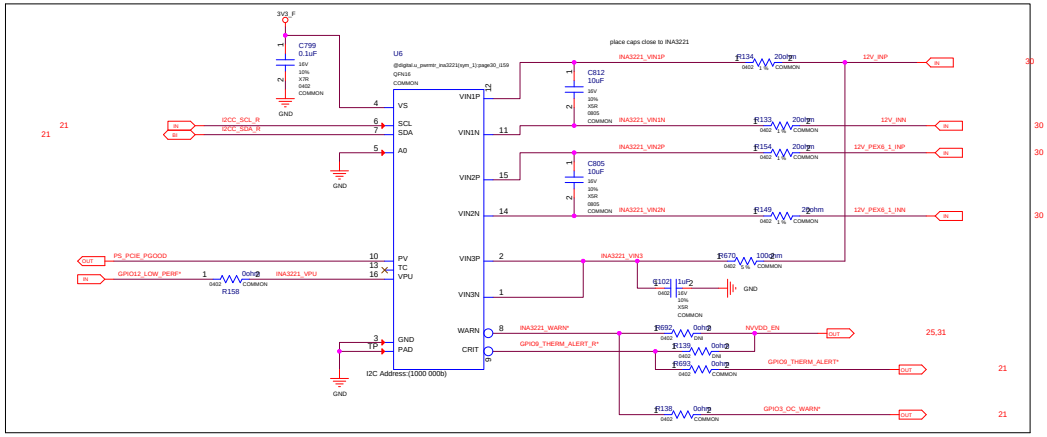
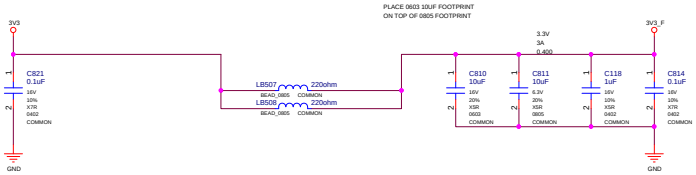
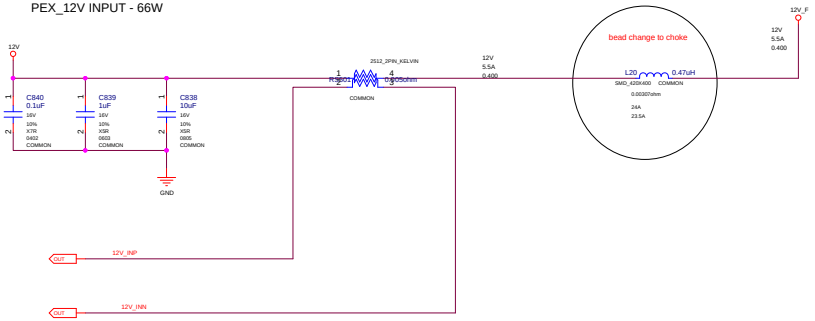
PS: Inputs, Filtering, and Monitoring

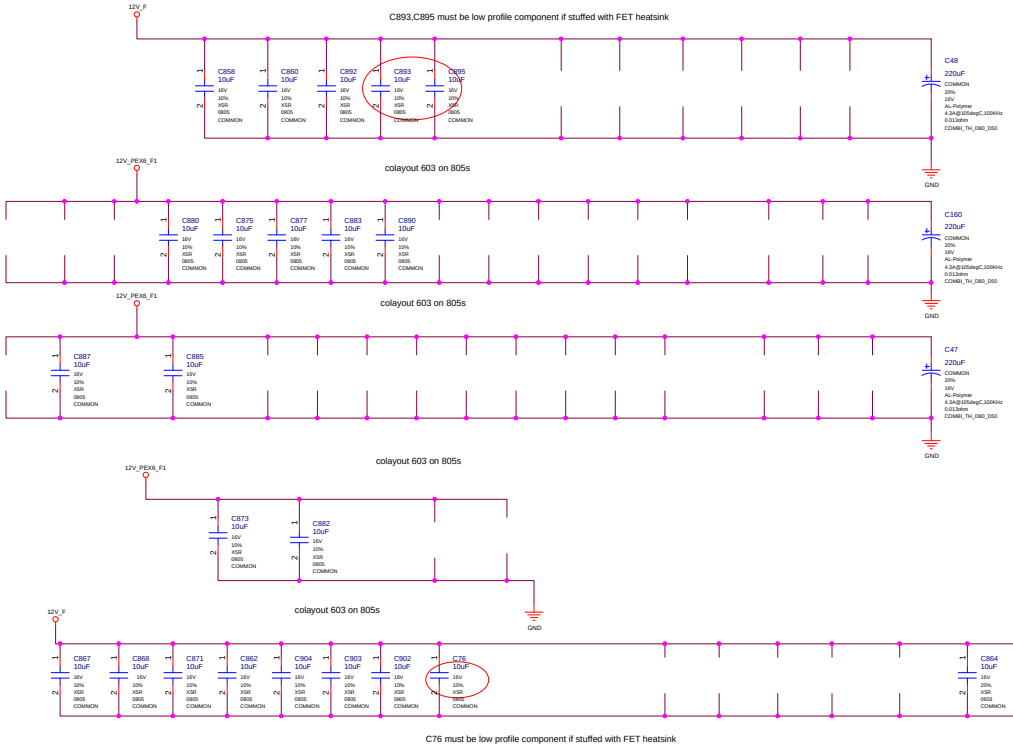


PEX 3V3 INPUT - 10W

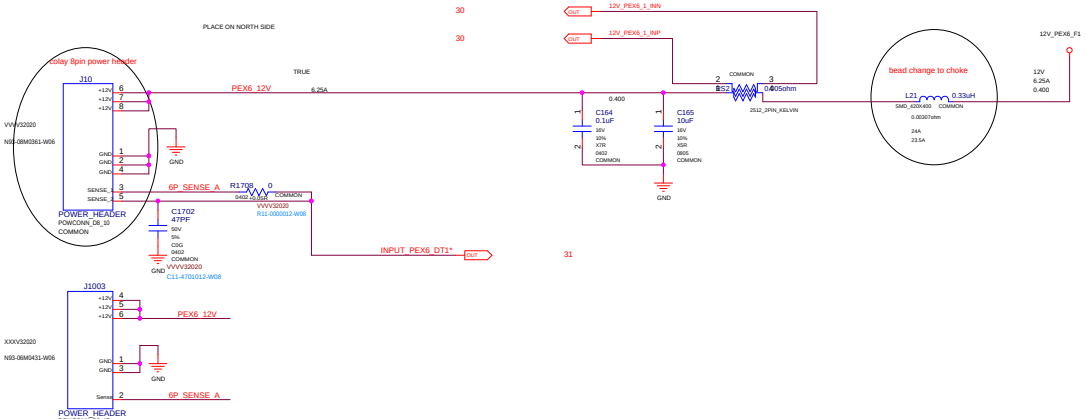


PEX_12V INPUT - 66W





PEX6 INPUT - 2x3 PCIE CON 75W



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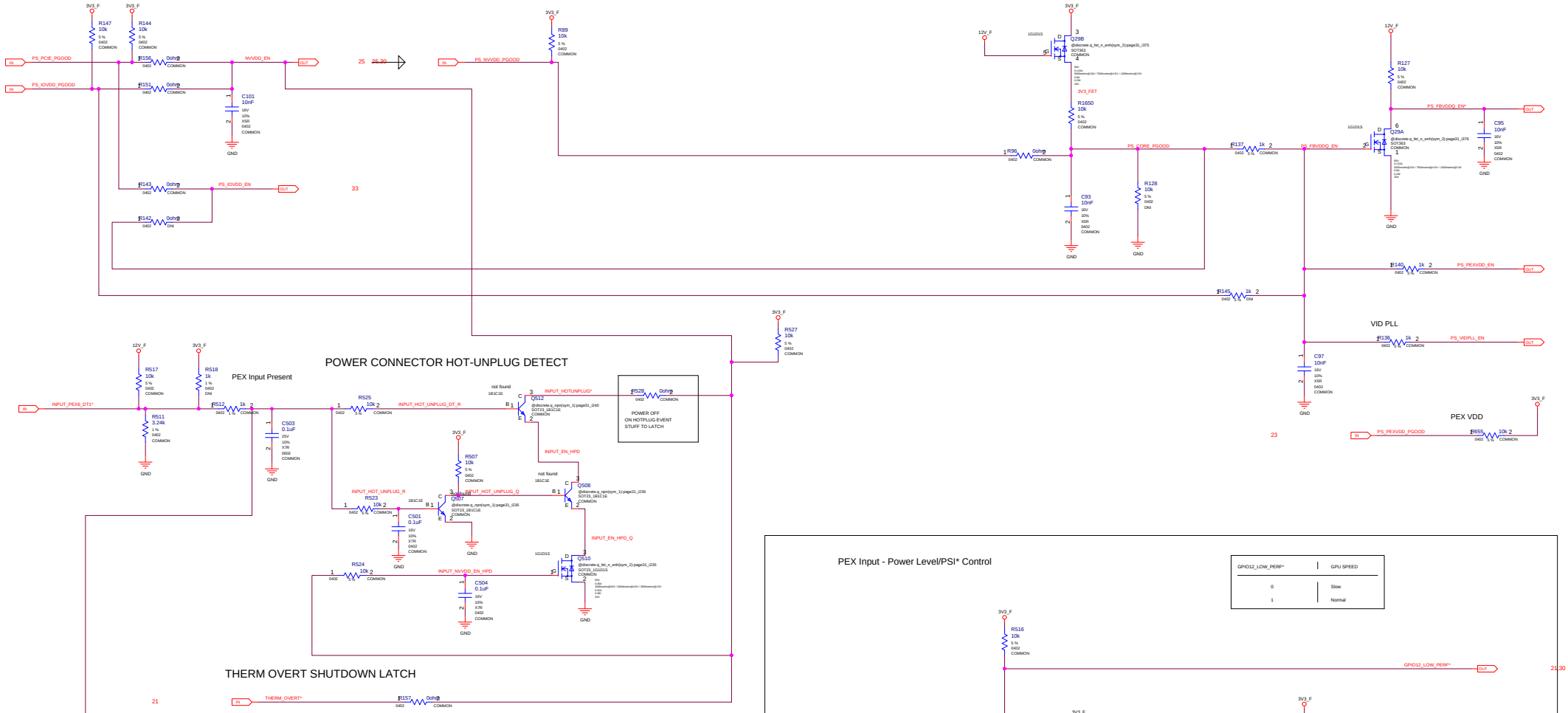
PS: Sequence and Shutdown



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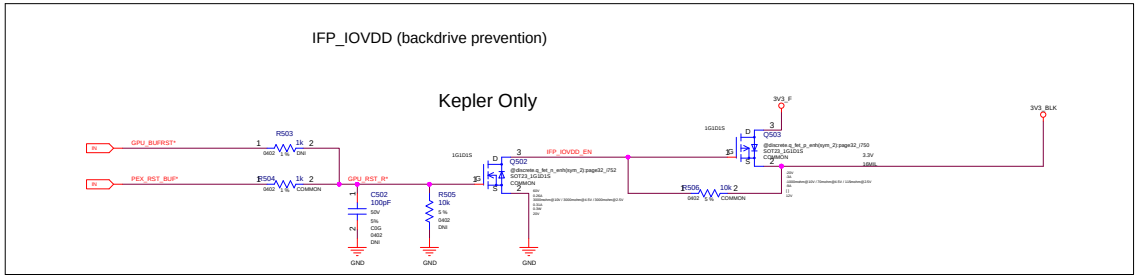
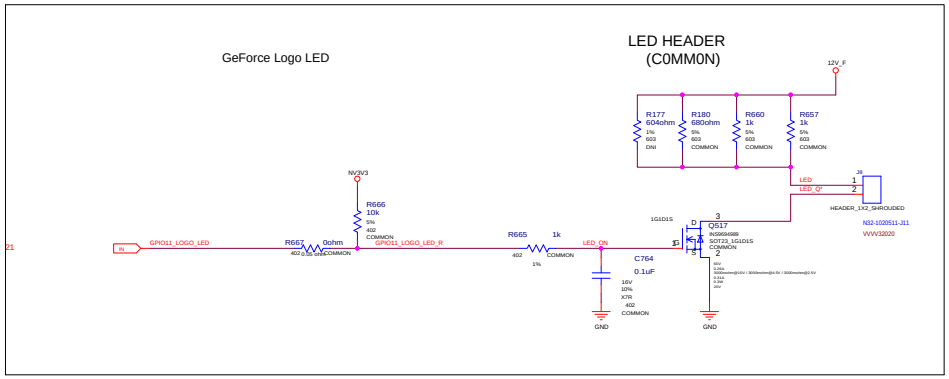
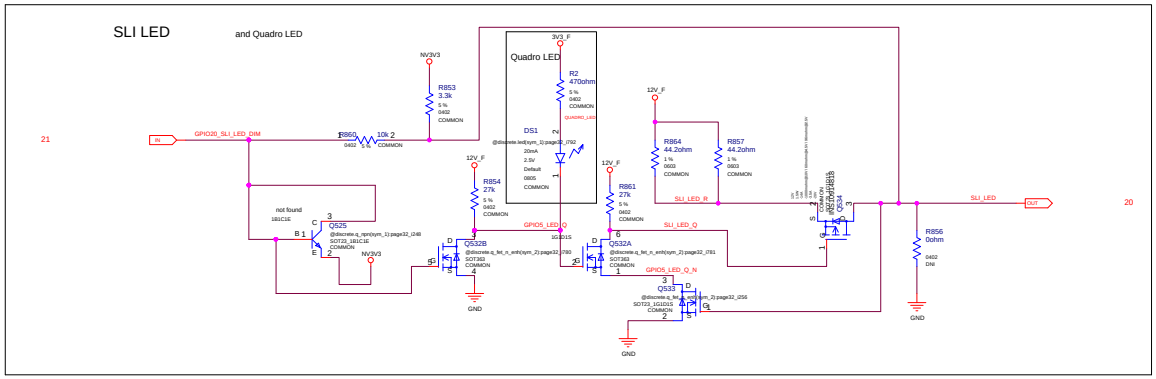
LEDs







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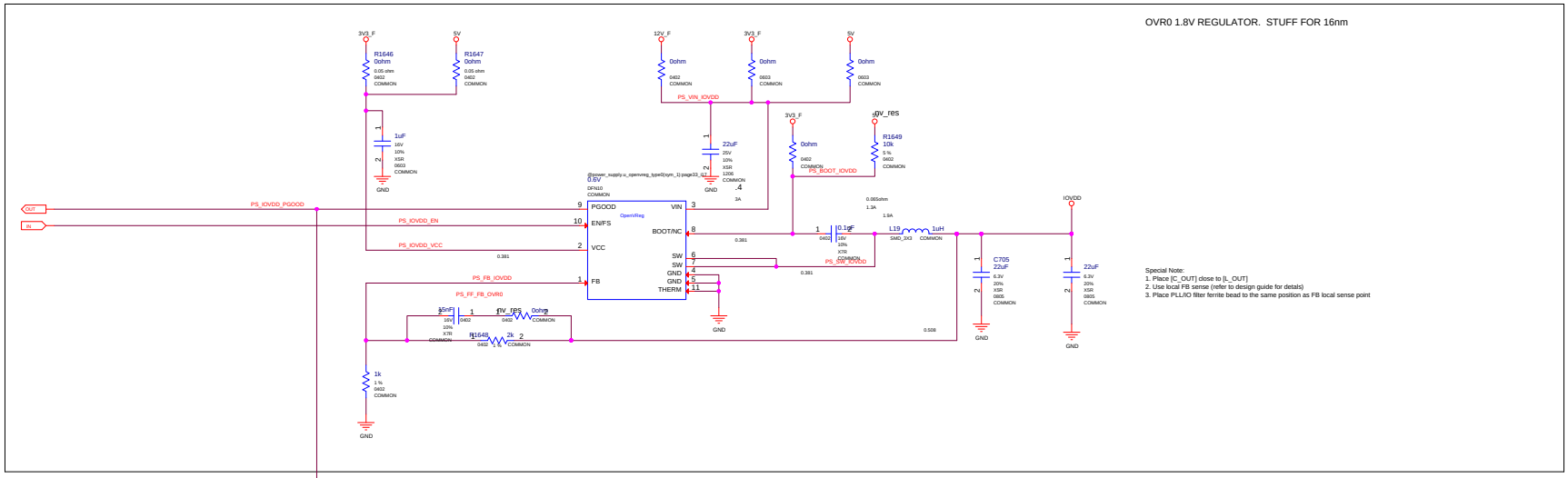

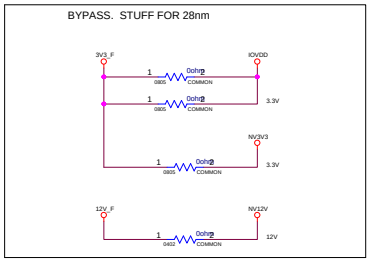

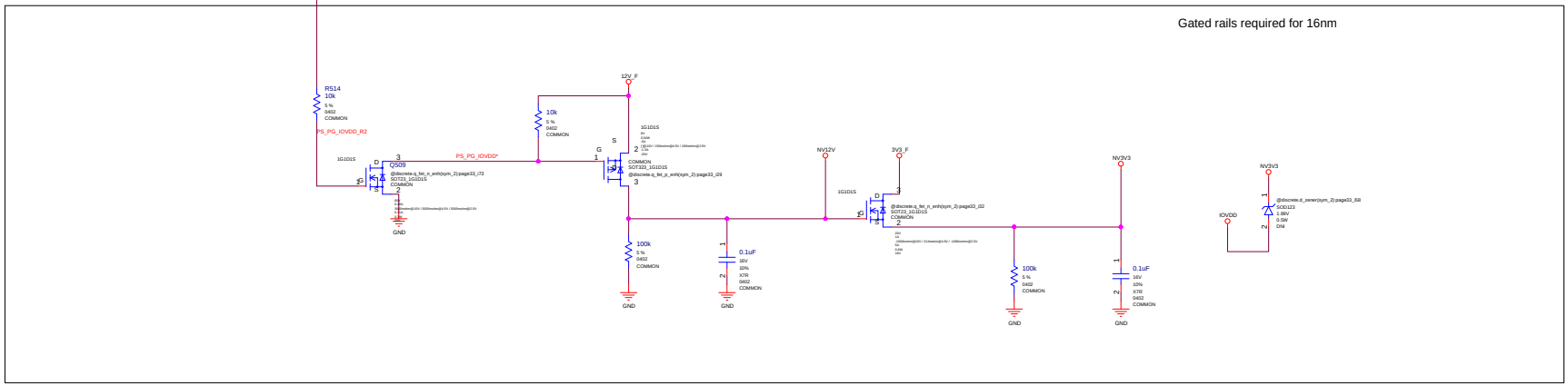

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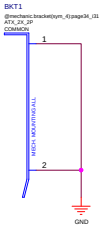
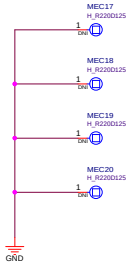
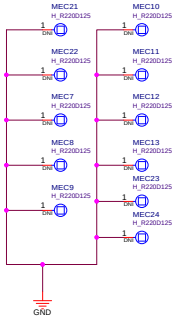
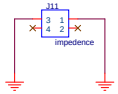
Mechanical: Bracket/Thermal Solution

Brackets:



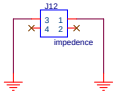






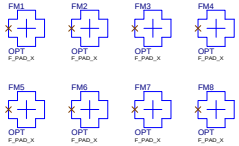
TOP:PEX_RX6

0.101 / 0.123mm 90ohm +/-10%



BOT:IFPC_TXC

0.102 / 0.178mm 95ohm +/-10%



TOP:FBC_D<56>

47ohm / 0.126mm

L3:FBC_DBI<6>

47ohm / 0.127mm

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