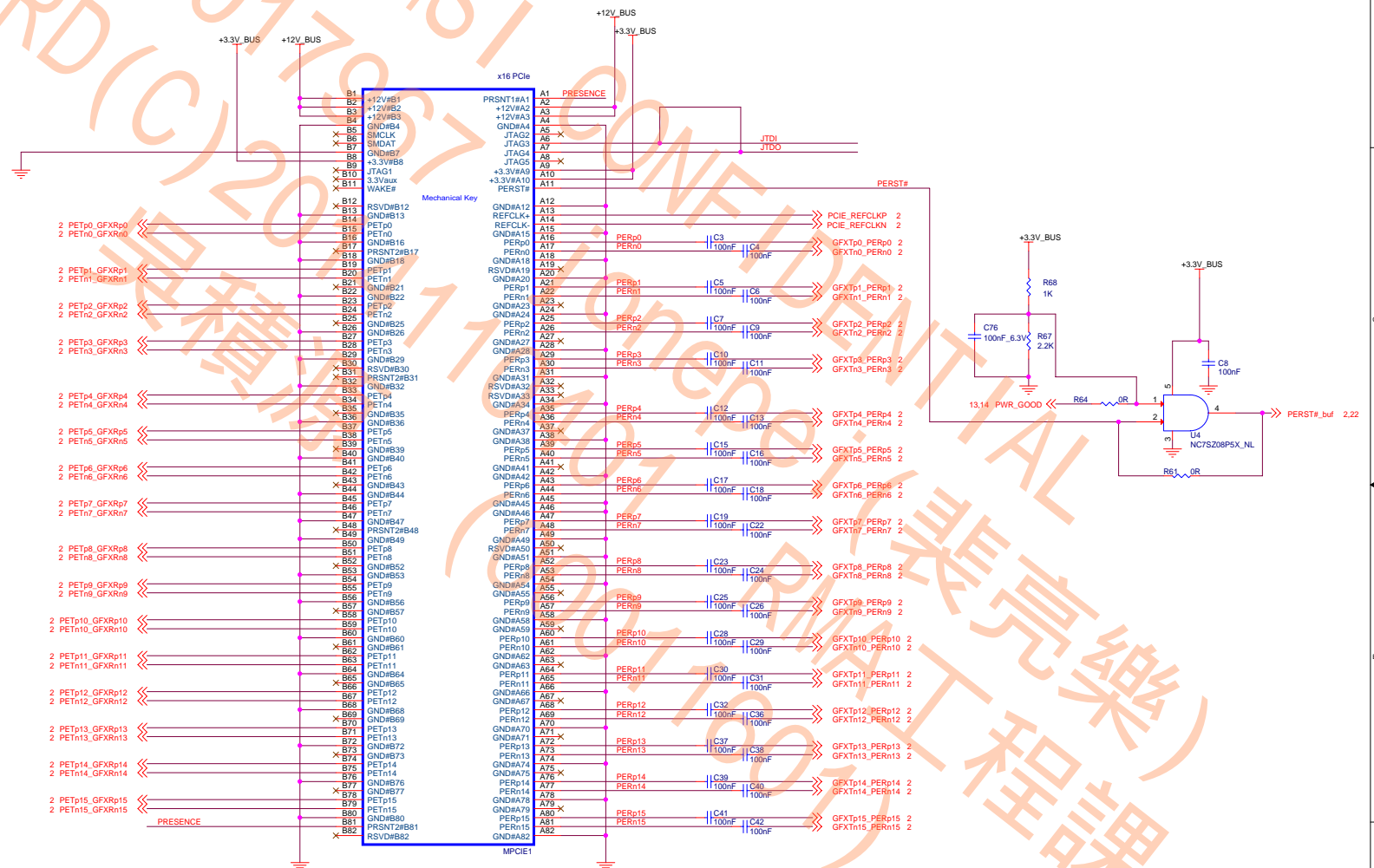
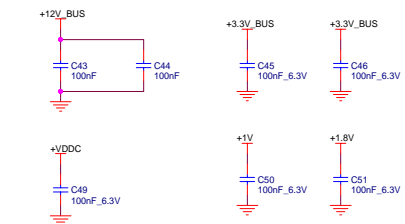
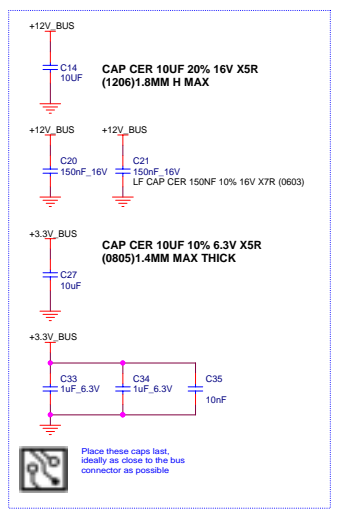
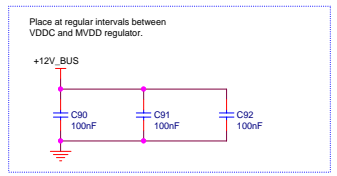
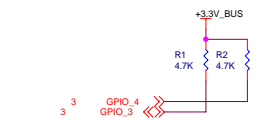


PCI-EXPRESS EDGE CONNECTOR



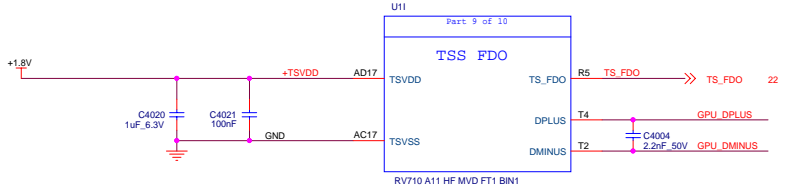
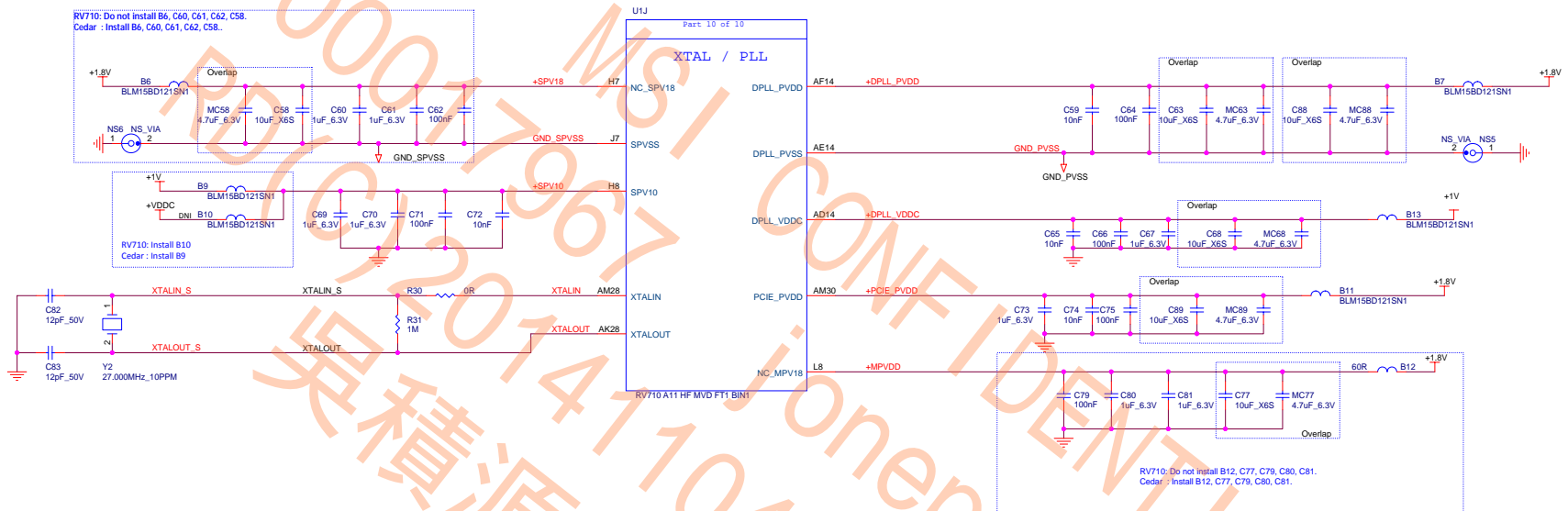
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

(2) Cedar PCIE Interface

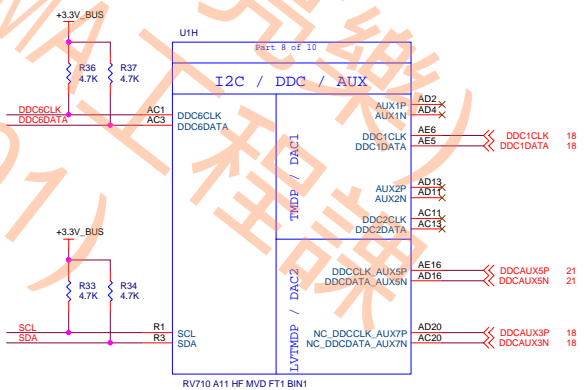
NOTE: some of the PCIE testpoints will be available through via on traces.



(04) Cedar GPIOs CF XTAL

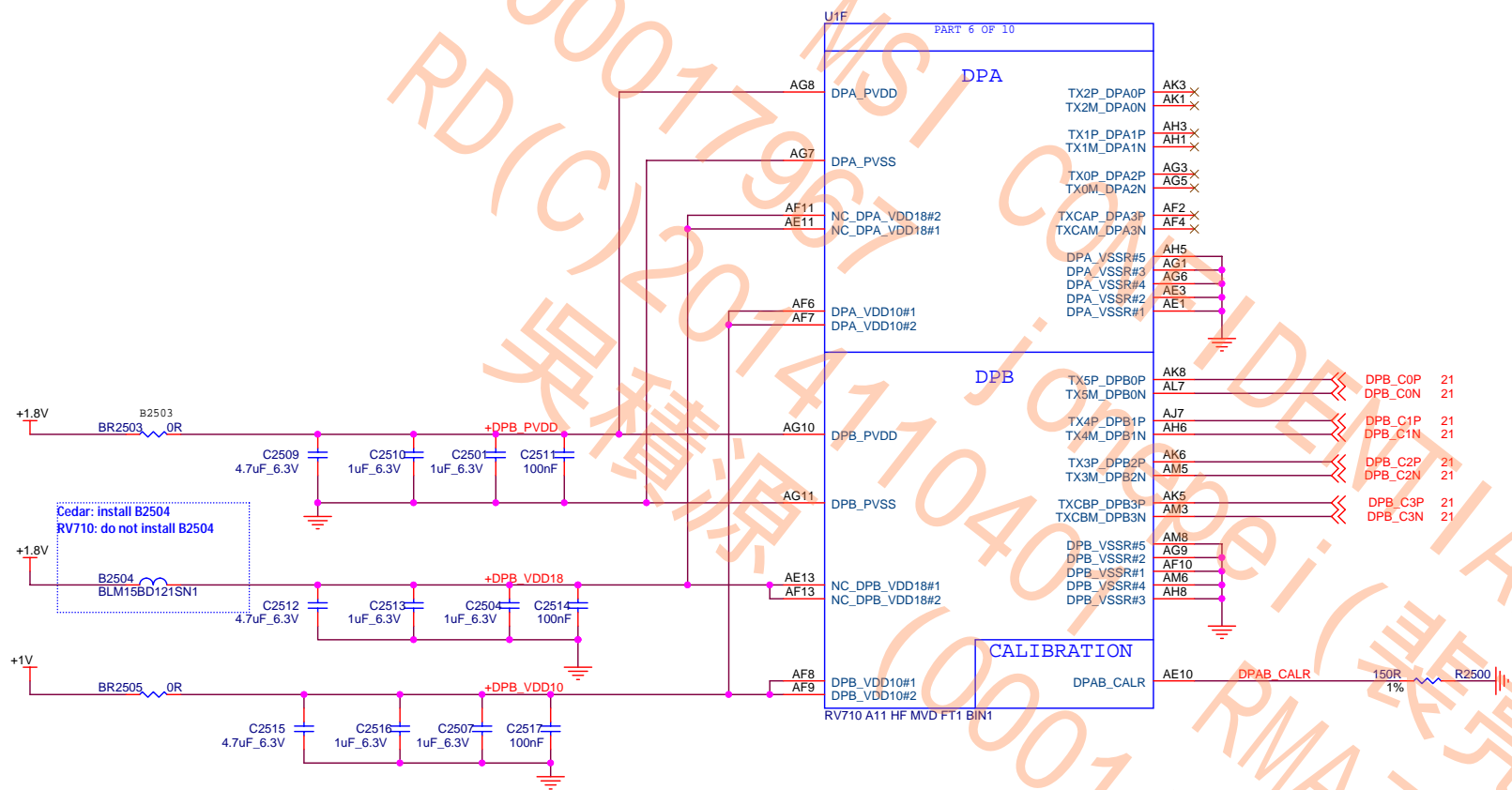


DDC1	Top VGA
AUX1	NC
DDC2	NC
AUX2	NC
DDC/AUX3	Middle HDMI/DP
DDC/AUX5	Bottom DVI/VGA
DDC6	NA
I2C	Debug Access Port

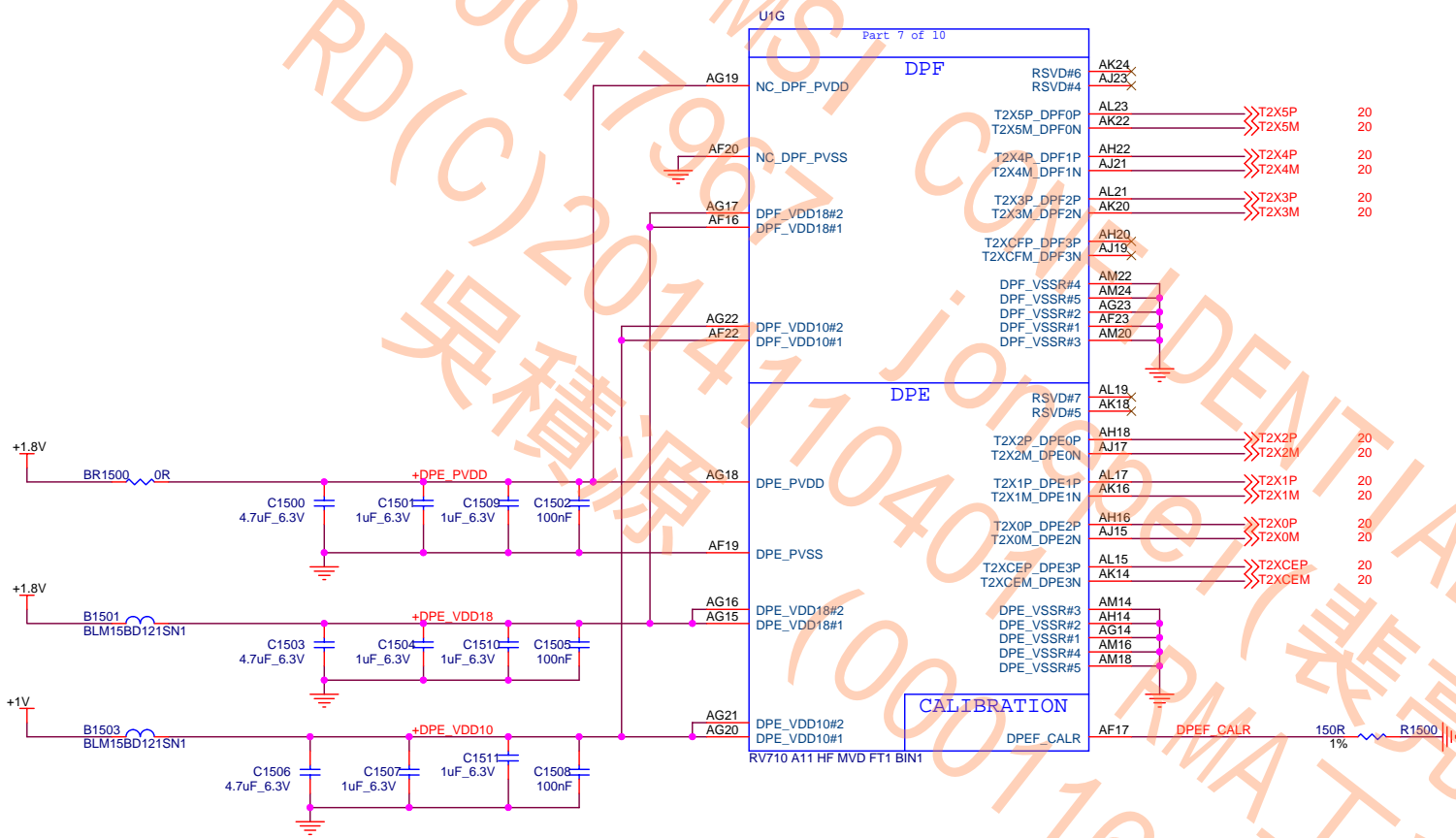


(05) Cedar TMDP A&B

TMDP INTERFACE



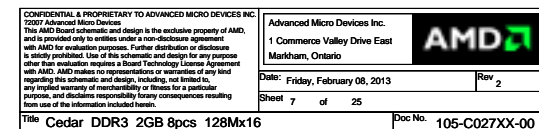
LVTMDP INTERFACE



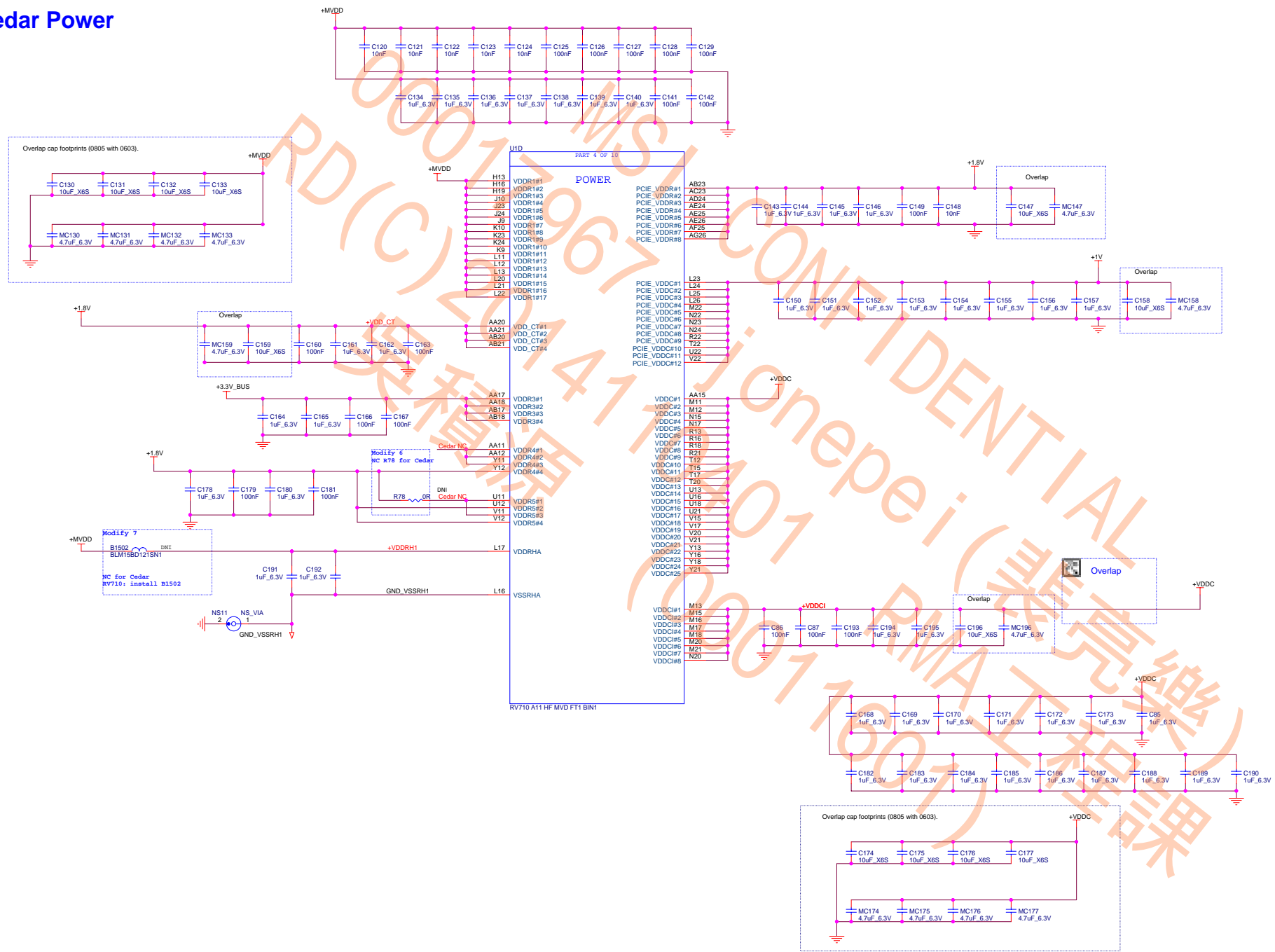
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Date: Friday, February 01, 2013	Rev 2	
Sheet 6 of 25		Doc No. 105-C027XX-00

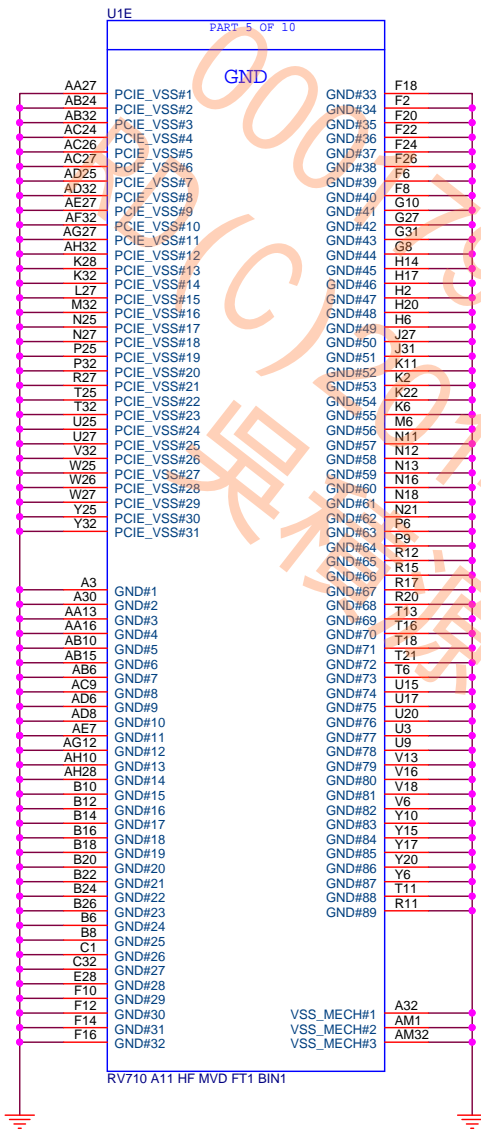
MEMORY INTERFACE




(08) Cedar Power



(09) Cedar GND

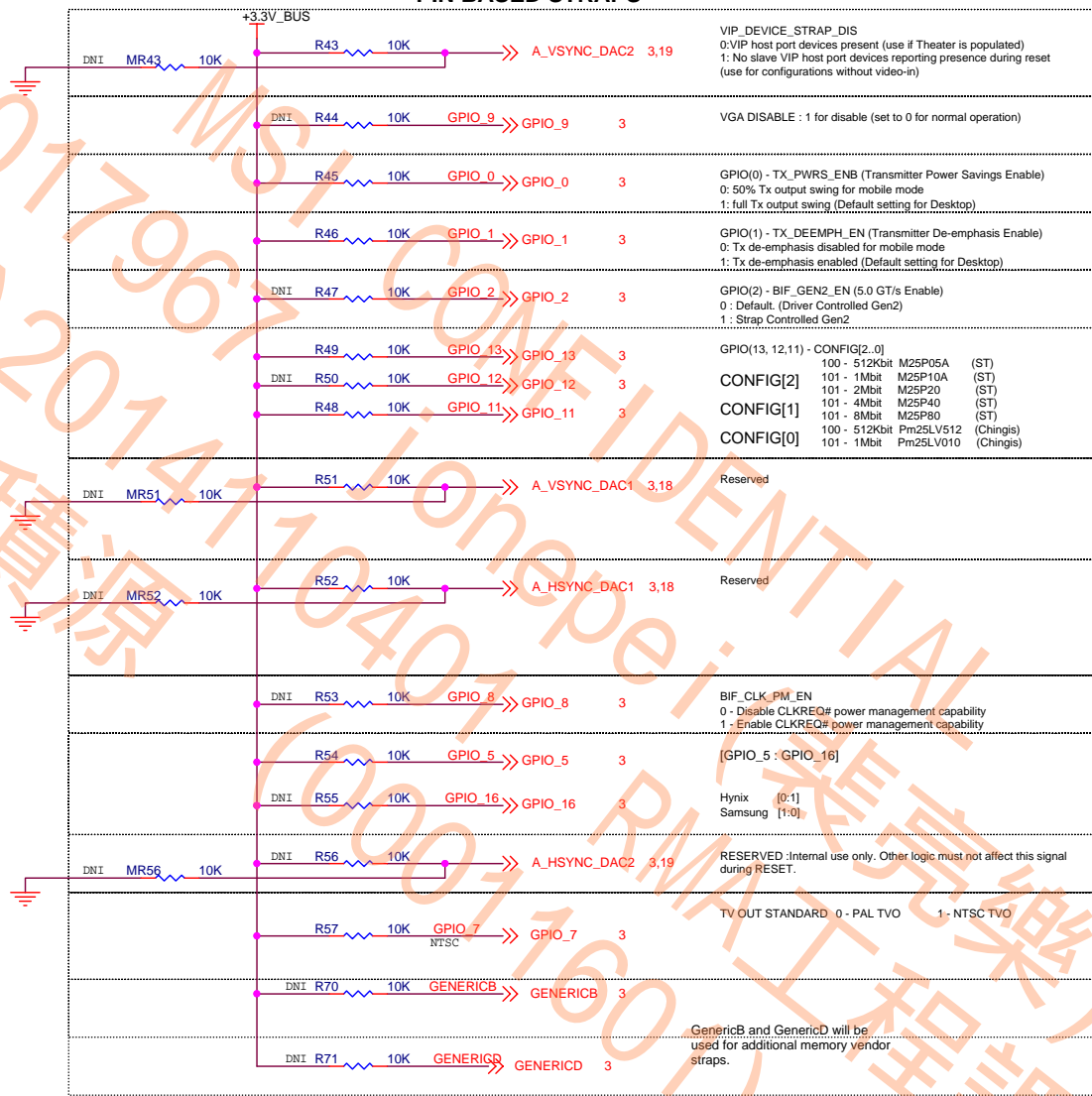


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Title Cedar DDR3 2GB 8pcs 128Mx16		Doc No. 105-C027XX-00

(10) Cedar STRAPS

PIN BASED STRAPS



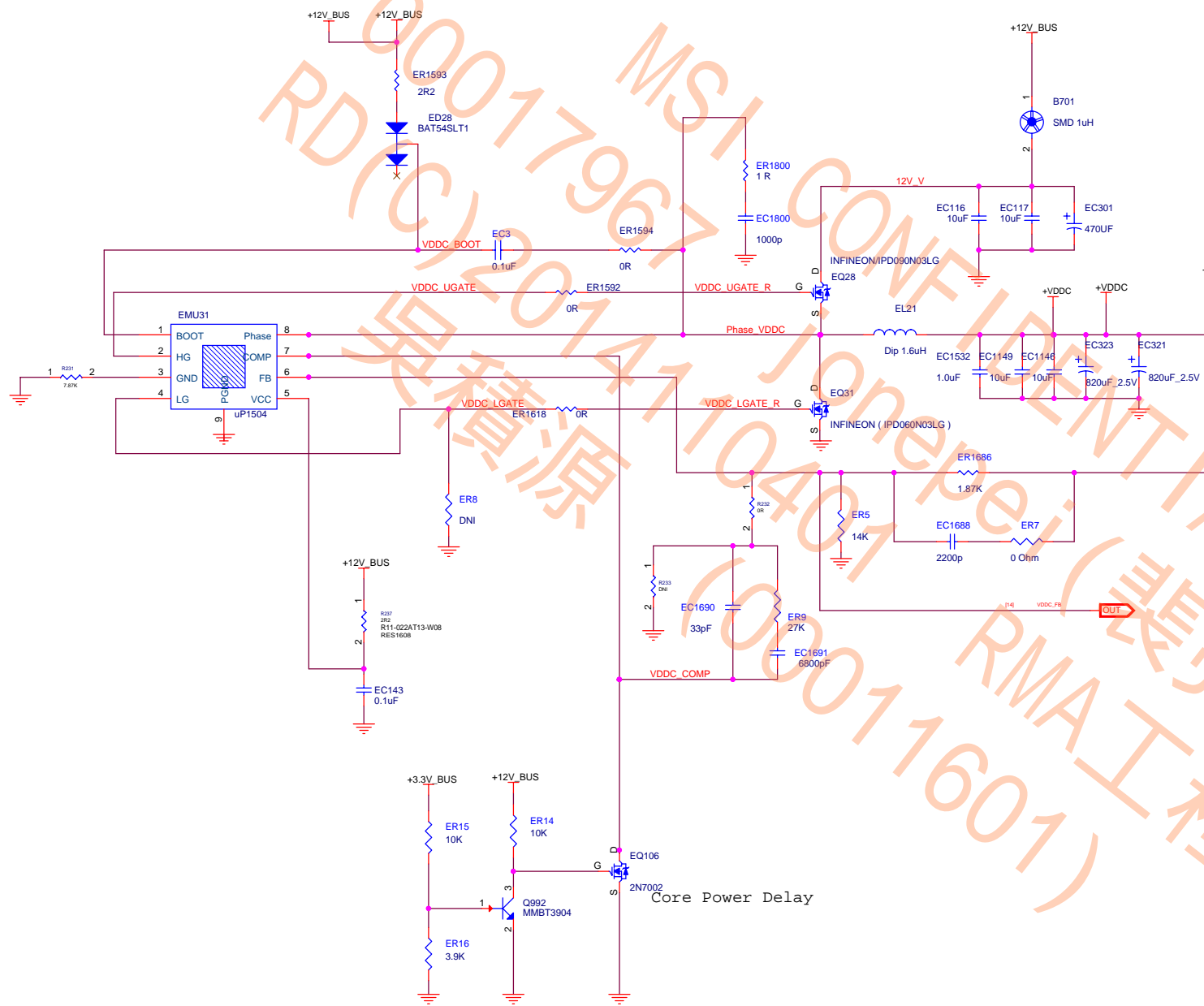
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Rev 2
Doc No. 105-C027XX-00

Title Cedar DDR3 2GB 8pcs 128Mx16



(13) Linear Regulators

Linear Regulators

LDO #1:

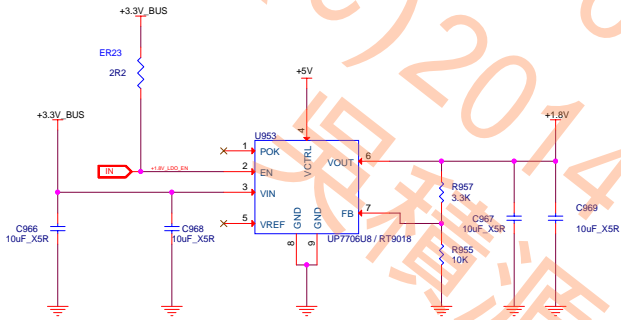
Vin = 3.00V to 3.60V (3.3V +/- 9%)

Vout = +1.8V +/- 2%

Iout = 1.6A (TbV) RMS MAX

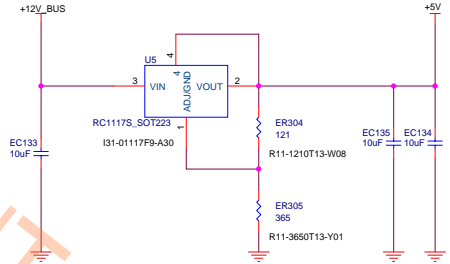
PCB: 50 to 70mm sq. copper area for cooling

Regulators for +5V_VESA and +5V_VESA2



$V_{out}=0.8V * (1+ R957 / R955)$

1.8V WORST-CASE REQUIREMENT	
Display Config	Exit Current
On+HDMI-CP	150mA



$V_{out}=1.25V* [1+(ER305/ER304)]$

LDO #2:

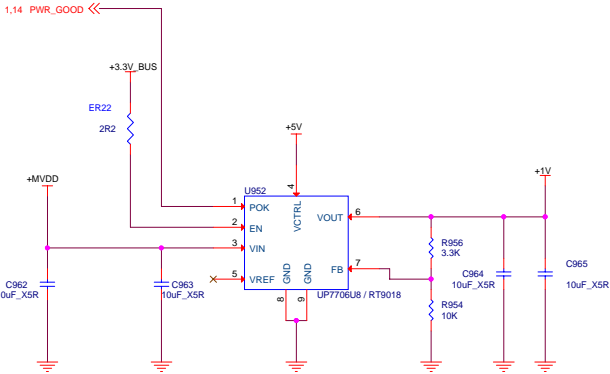
Vin = +1.32V to 1.84V MAX

Vout = +1.01V +/- 2%

Iout = 1.7A (TbV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

1.0V WORST-CASE REQUIREMENT	
Display Config	Exit Current
On+HDMI-CP	150mA



$V_{out}=0.8V * (1+ R956 / R954)$

Power Play

Power up/down Sequencing

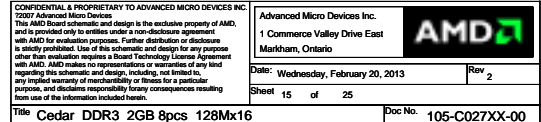


Rev

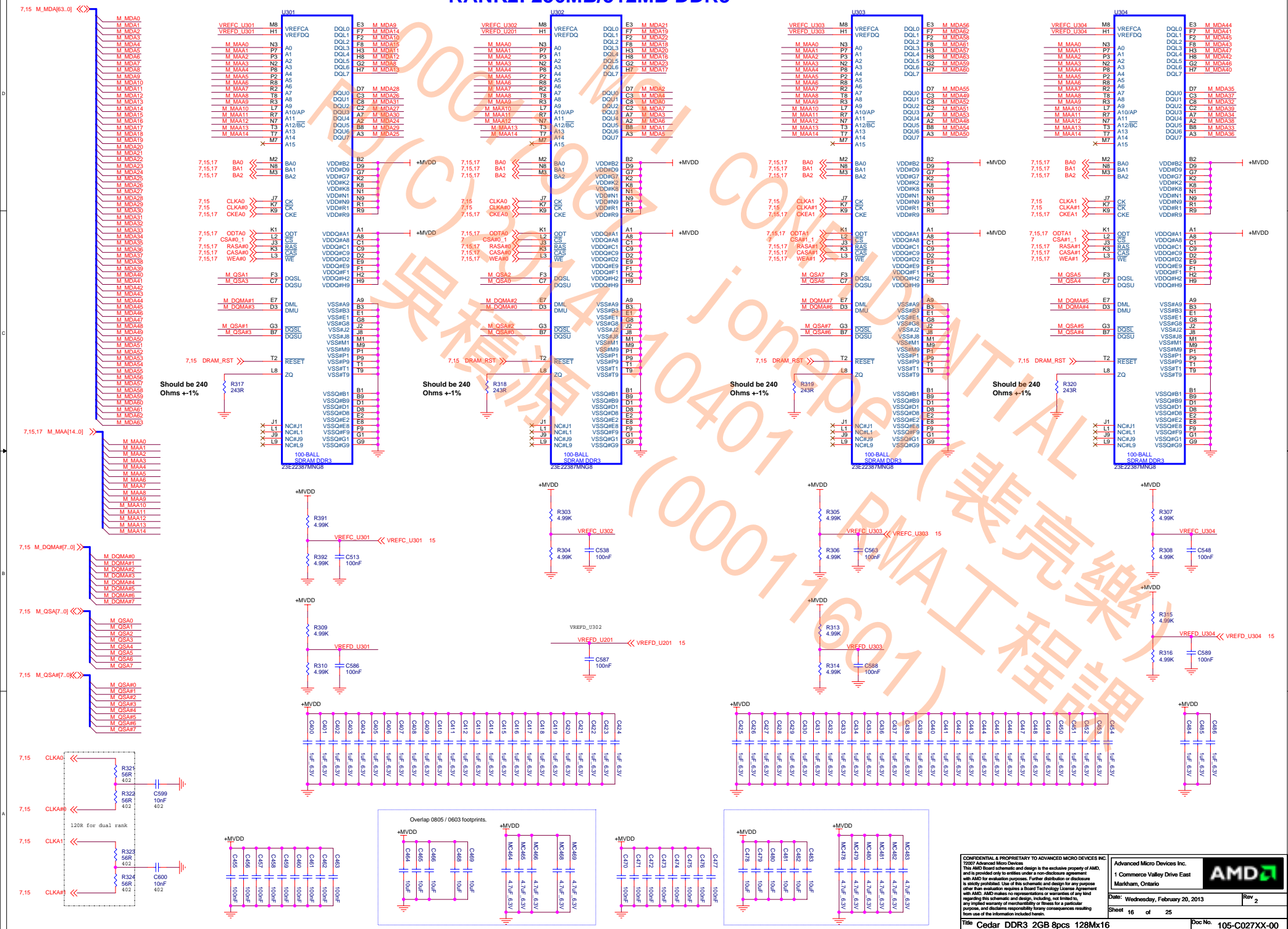
25

Doc No.	105-C027XX-00
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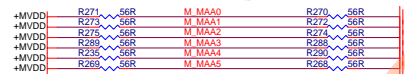
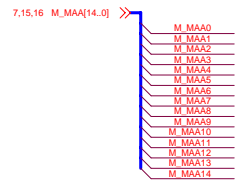
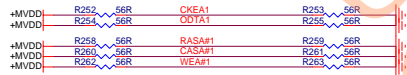
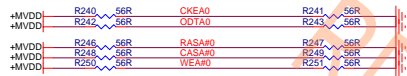
RANK1: 256MB/512MB DDR3



RANK2: 256MB/512MB DDR3



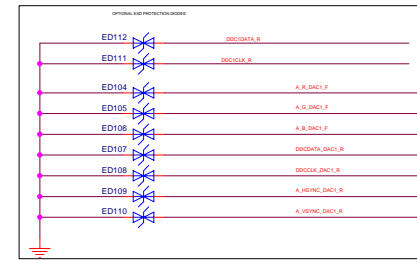
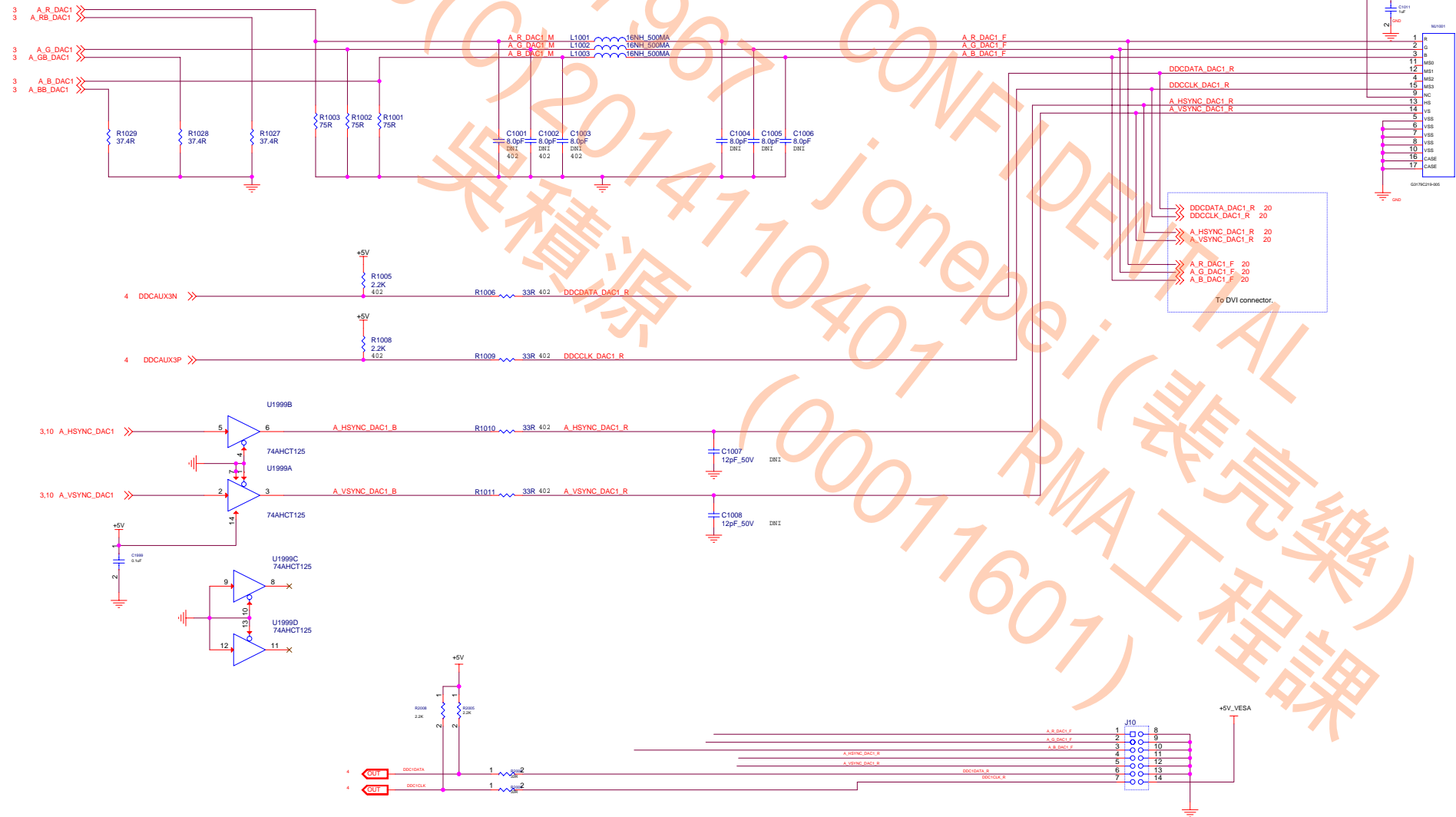
(17) DDR3 Termination



DAC 1 OUTPUT



Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane.
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1029-26)



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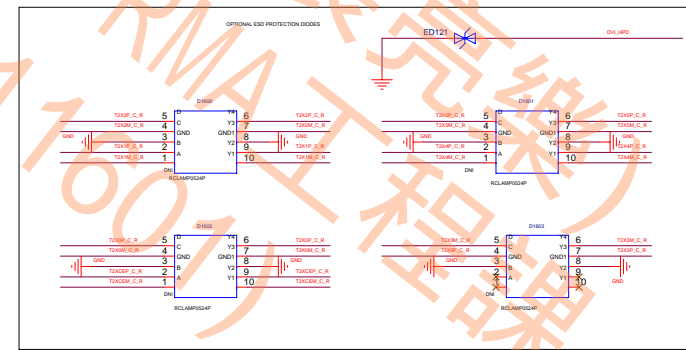
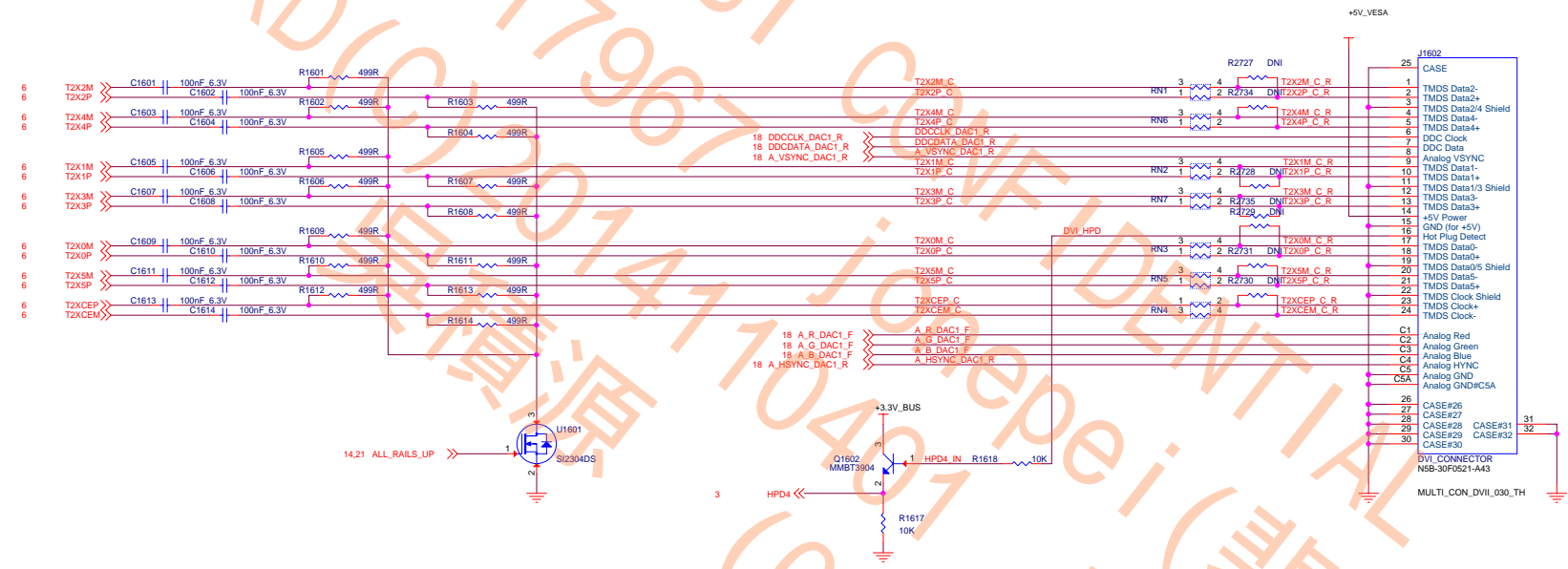
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Rev 2

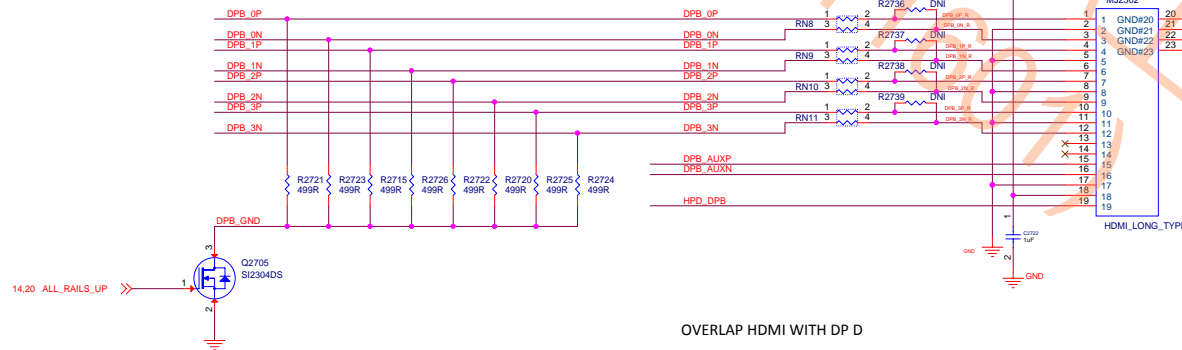
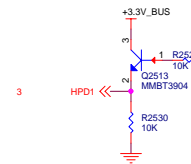
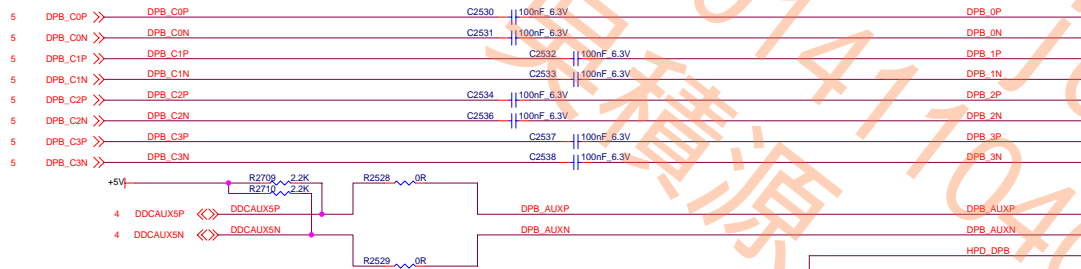
Title Cedar DDR3 2GB 8pcs 128Mx16
Doc No. 105-C027XX-00

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00017967
RD(C)2014110401
吳積源
jonepei (裴亮樂)
RMA工程師
(00011601)

DPE / DPF OUTPUT



OPTIONAL ESD protection diodes



OVERLAP HDMI WITH DP D

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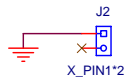
Date: Monday, January 28, 2013

Rev 2

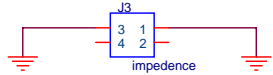
Sheet 21 of 25

Title Cedar DDR3 2GB 8pcs 128Mx16

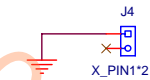
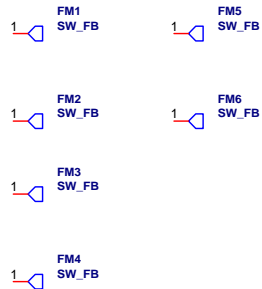
Doc No. 105-C027XX-00B



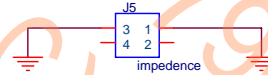
M_MDA31
INT3
0.148 mm / 45ohm +/- 10%
Reference INT2 GND



HDMI TMDS signals
DPB_C1N / DPB_C1P
TOP
0.0864 mm / 0.323 mm / 100ohm +/- 10%
Reference INT2 GND



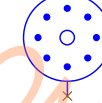
M_MDA37
TOP
0.1242MM / 45ohm +/- 10%
Reference INT2 GND



PEX_PCIE
GFXT4_PERP4 / GFXT4_PERN4
Bottom
0.101 mm / 0.15 mm / 85 ohm +/- 10 %
Reference INT5 GND

Bracket Components

MT1
MT_Hole 0.136 TM 5.5 BM 7.0



ASSY-SCREW202
SCREW
SCREW

7020005200G

For DVI Connector

ASSY-SCREW200

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW201

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

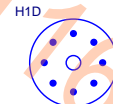
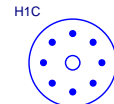
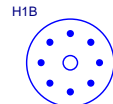
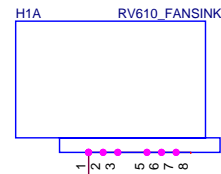
Square Fansink 12W

7120036200G BLACK

7120336200G RED

Rectangular Fansink 22W

7120035100G

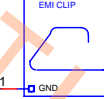


Dual-slot Heatsink 14W

7120181000G

MEC7

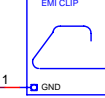
FINGER_S1_1
COMMON
2.3mm



GND

MEC8

FINGER_S1_1
COMMON
2.3mm



GND

ASSY1
BRACKET
8020040100G

ASSY2
BRACKET
LP
8020040400G

SKU	P/N	CONFIGURATION	Form Factor
WALLEYE	8020051300G	DVI + DP + VGA	FH / SS
	8020051400G	DVI +HDMI+ VGA	FH / SS
	8020051700G	DVI + DP + VGA	FH / DS
	80200517A0G	DVI +HDMI+ VGA	FH / DS

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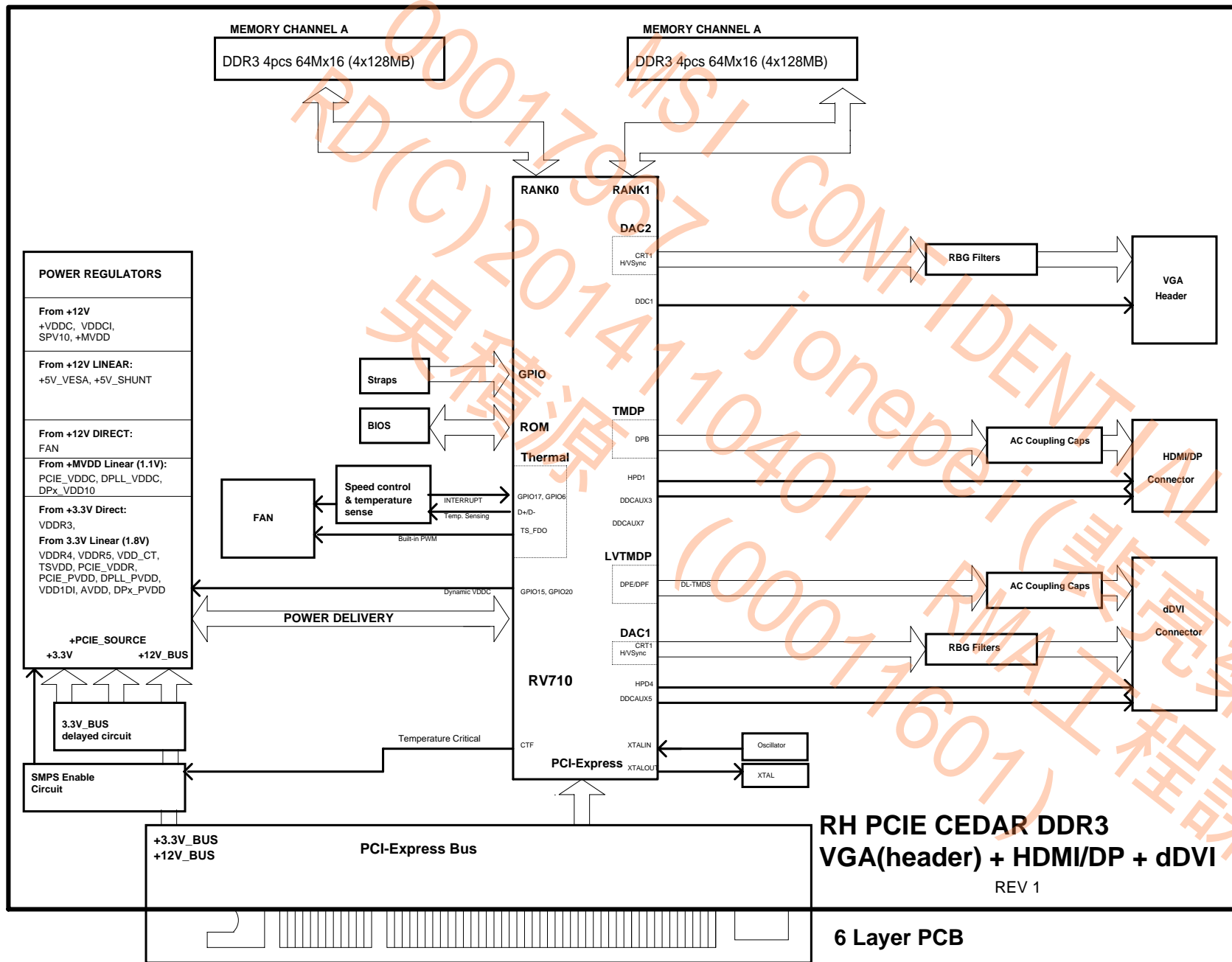
Date: Wednesday, February 20, 2013

Rev 1

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Title Cedar DDR3 2GB 8pcs 128Mx16

Doc No. 105-C027XX-00B



**RH PCIE CEDAR DDR3
VGA(header) + HDMI/DP + dDVI**
REV 1

6 Layer PCB

<div>AMD</div>			Title		Schematic No.		Date:				
			Cedar DDR3 2GB 8pcs 128Mx16		105-C027XX-00		Friday, January 25, 2013				
			REVISION HISTORY						NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.		Rev 2
Sch Rev	PCB Rev	Date	Cedar 1GB DDR3 Walleye		REVISION DESCRIPTION						
0	00A	2008.12.30	Sch no change. just modify HDMI connector location on PCB								
1	00B	2009.08.24	Page 1:remove C1,C2,R3,U3,Add Q1,Q2 Page 7:Add C97,C98 Page 10:Add MR43,MR51,MR52,MR56 Page 18:Add L1004,L1005,L1006 Page 19:Remove R2013,R2014,R2015,R2016,Q2001,Q2002								
2	00	2009.09.23	Change HDMI/DP DDC line to DDCAUX3								