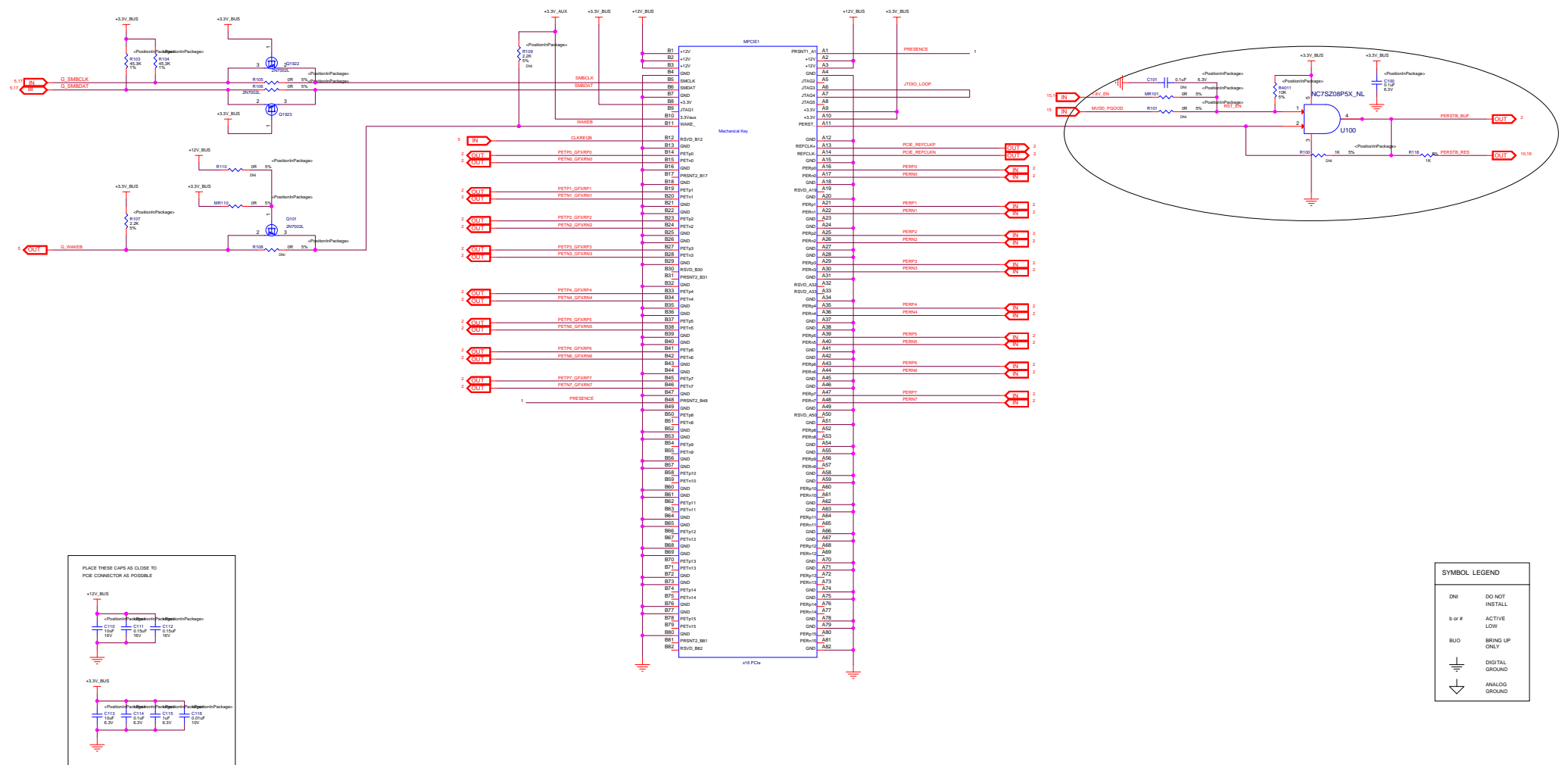


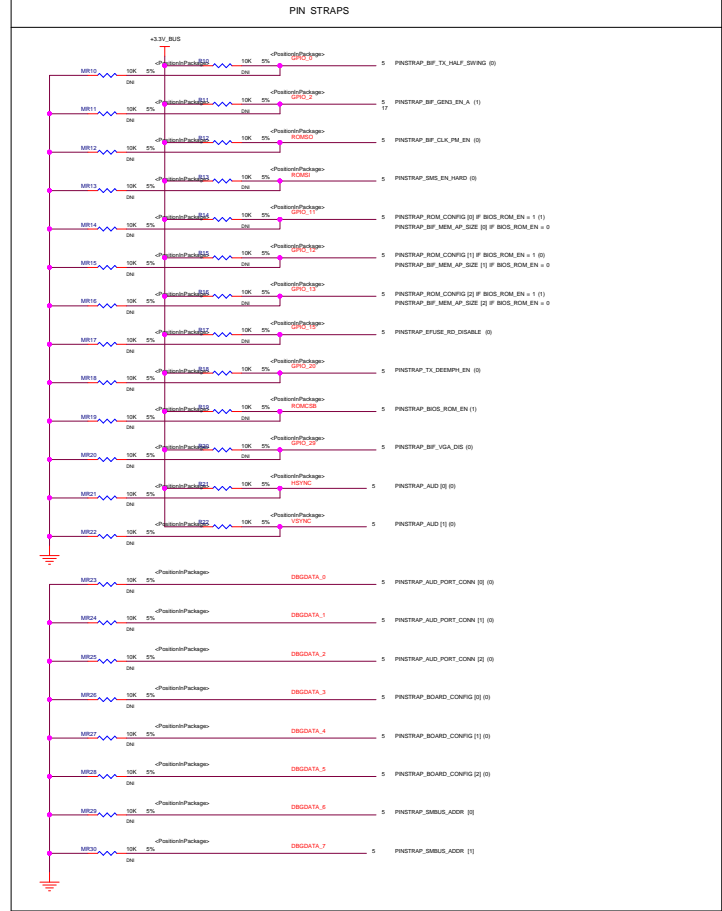
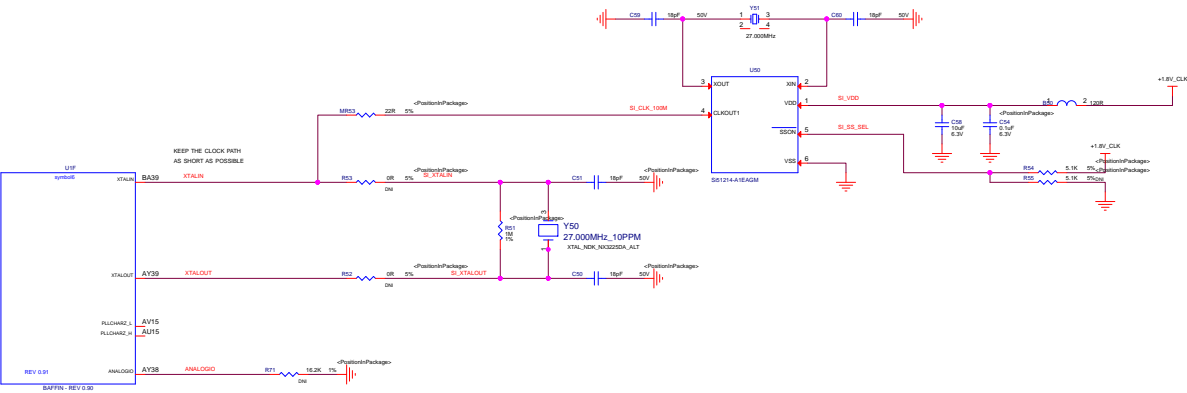
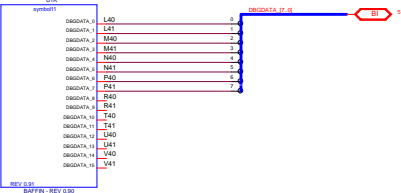
(1) PCIE EDGE CONNECTOR



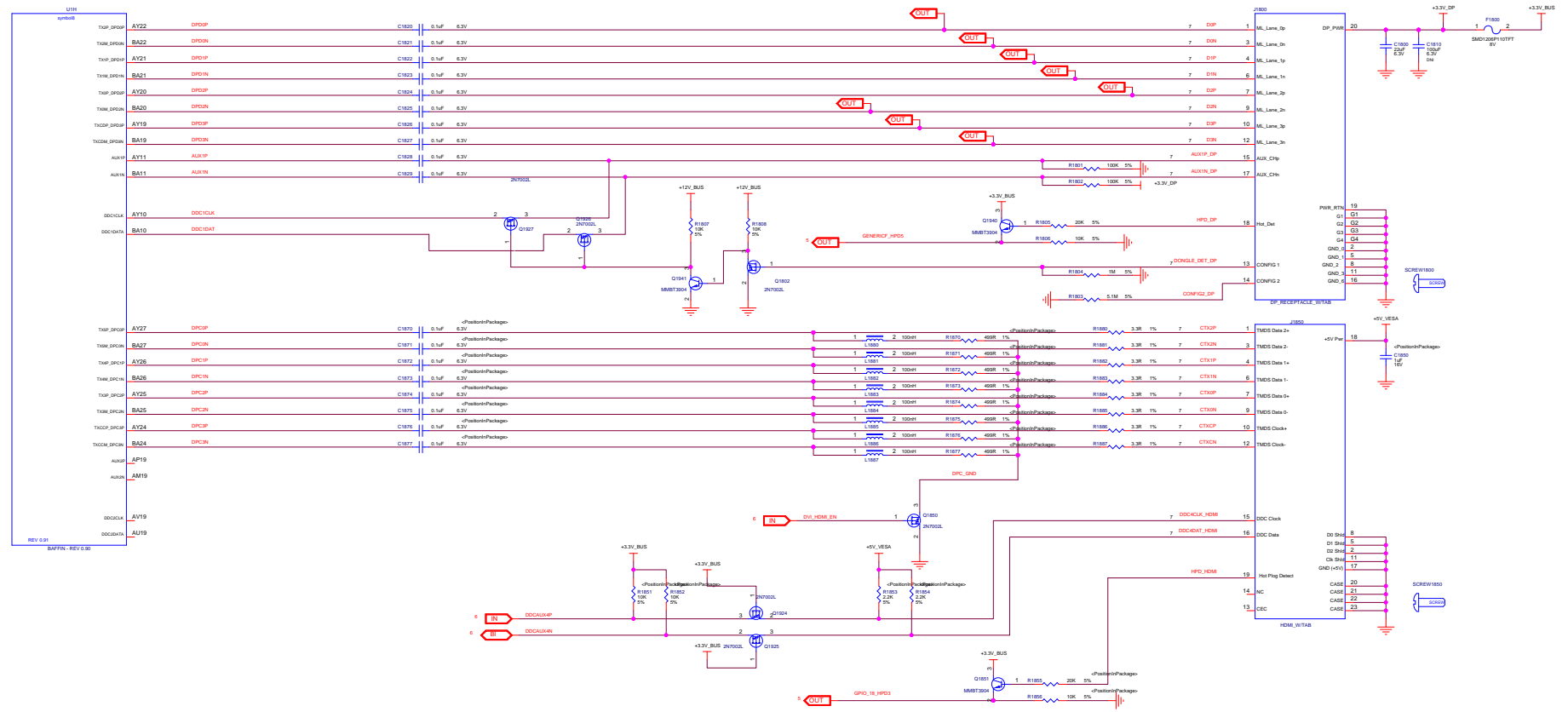
(5) BAFFIN GPIO STRAPS CLK

DEVICE	ADDRESS
ADS274	0x5C
RT9403	0x62
VTHM II	

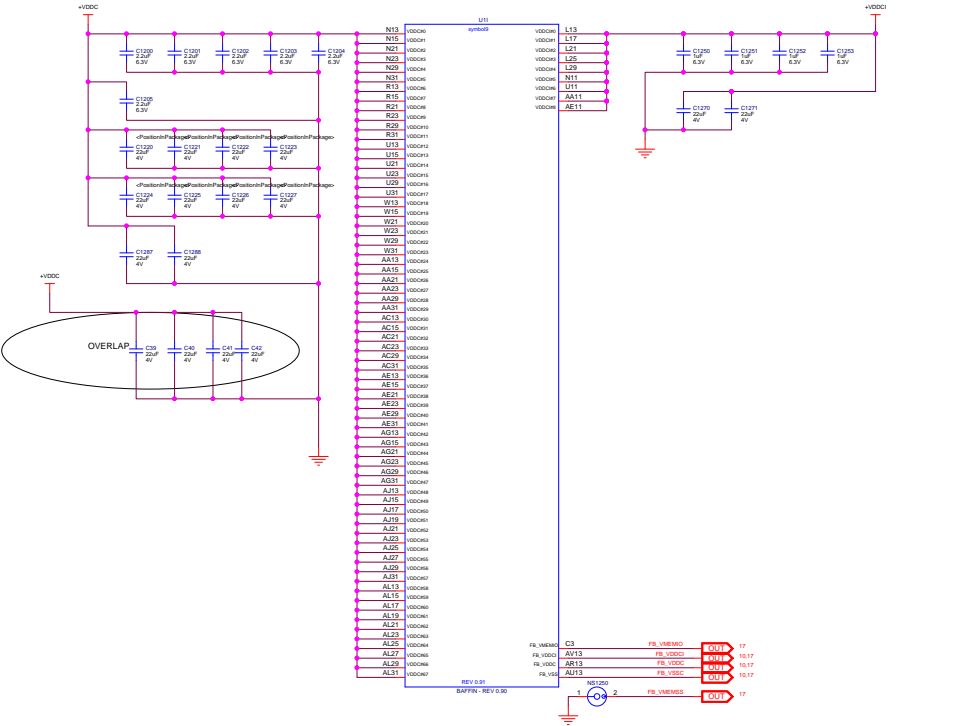
DEVICE	ADDRESS
LM90G03	0x98

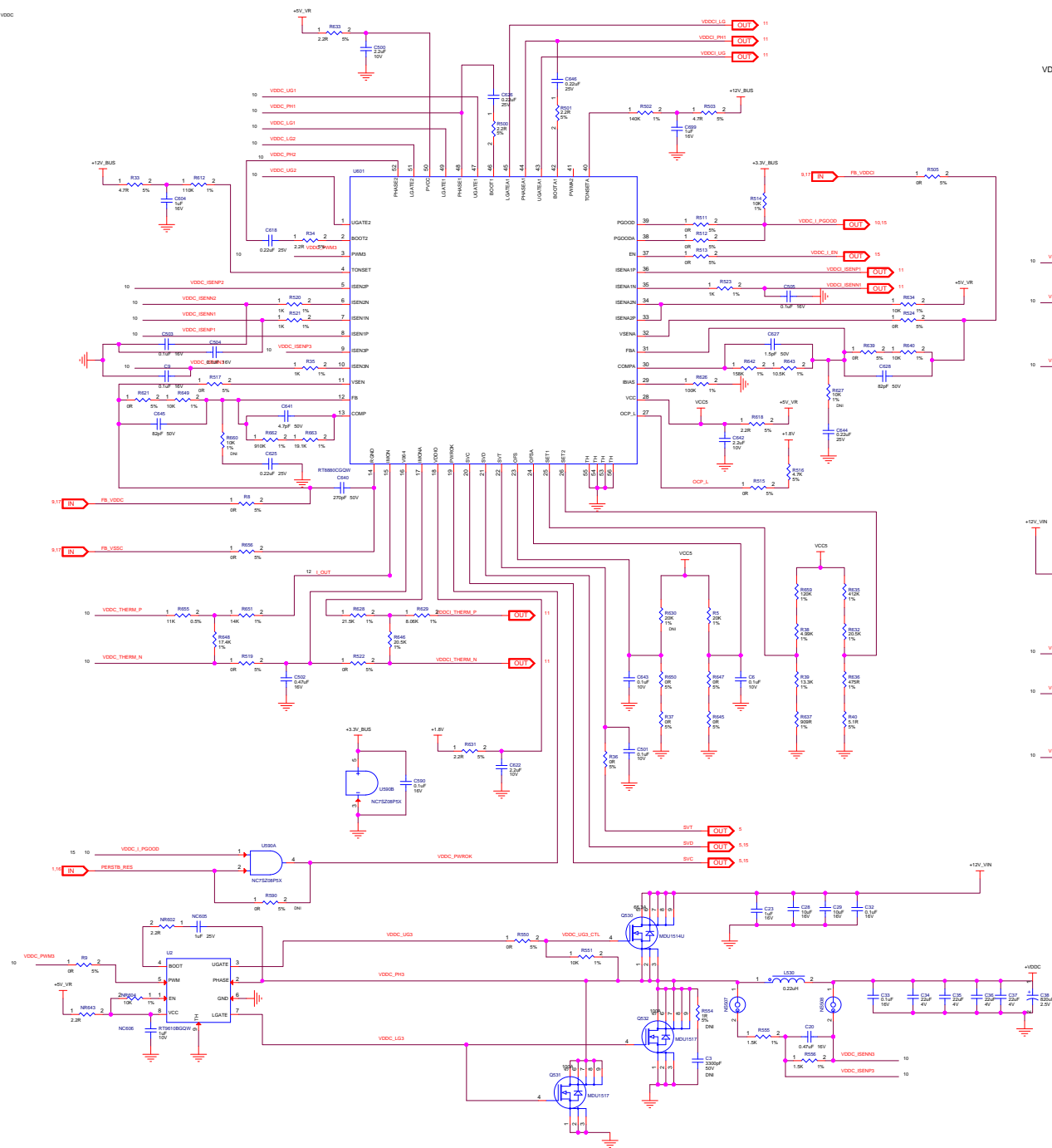


(7) BAFFIN TMDPCD - HDMI DP

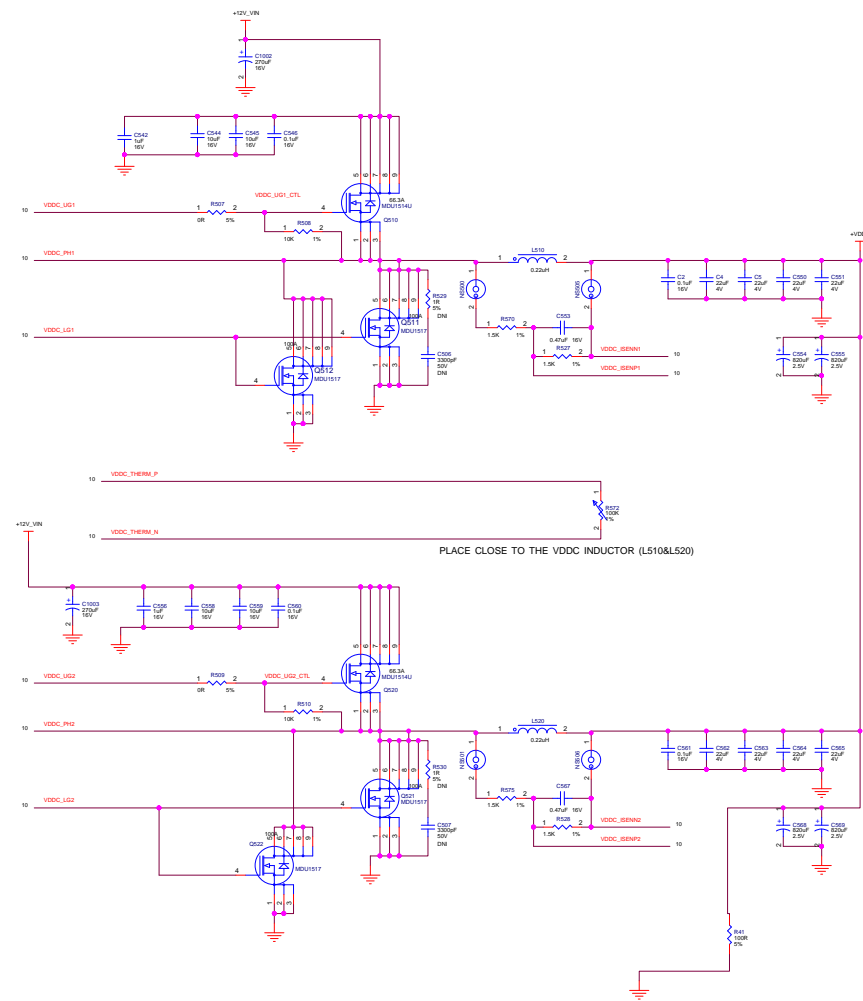


(9) BAFFIN POWER GND

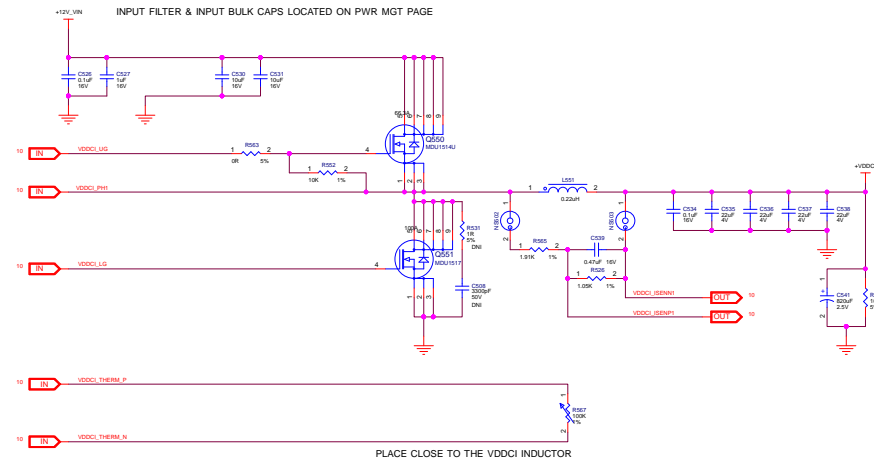




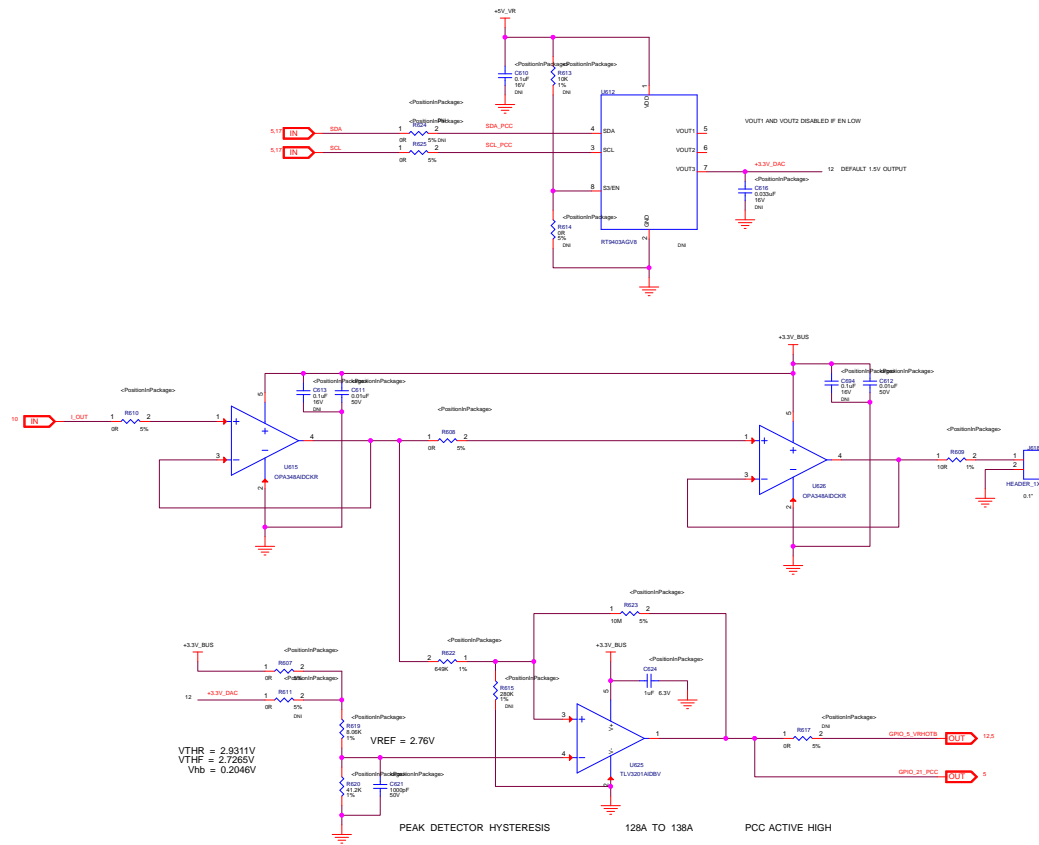
VDDC INPUT



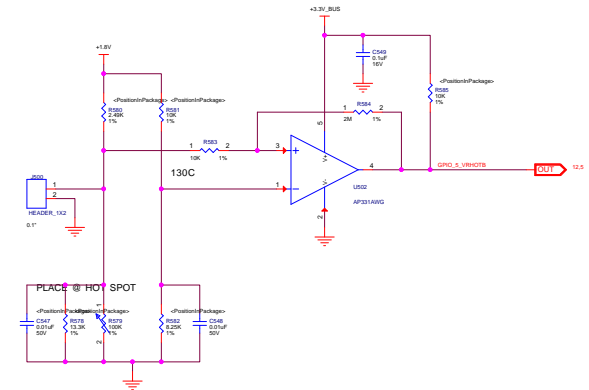
(11) VDDCI

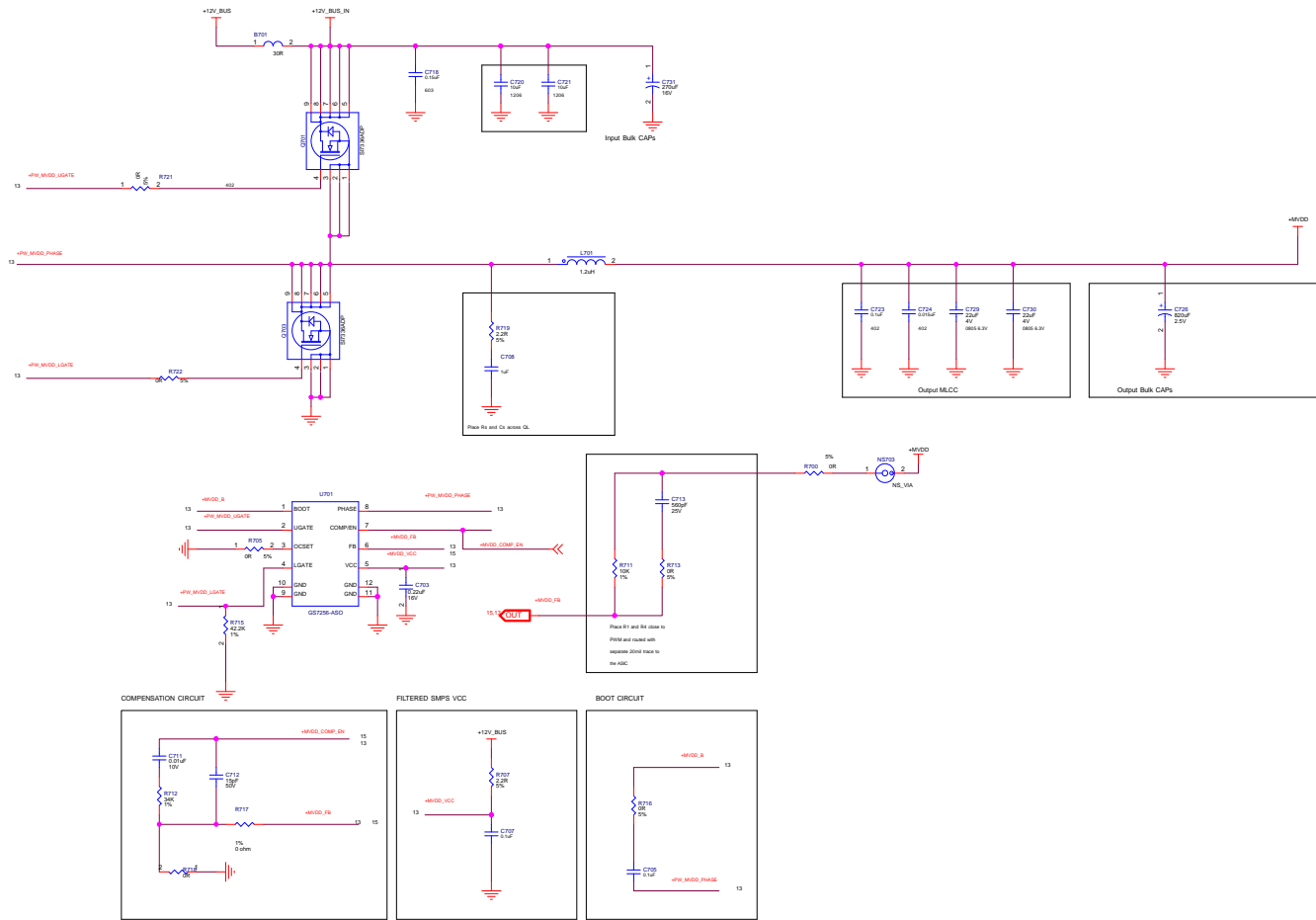


PEAK CURRENT CONTROL

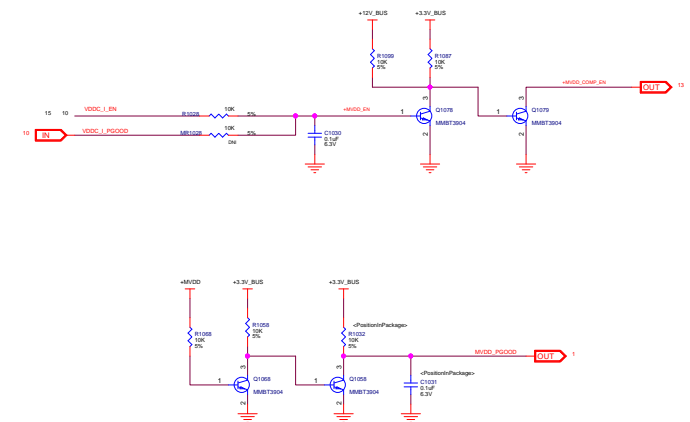
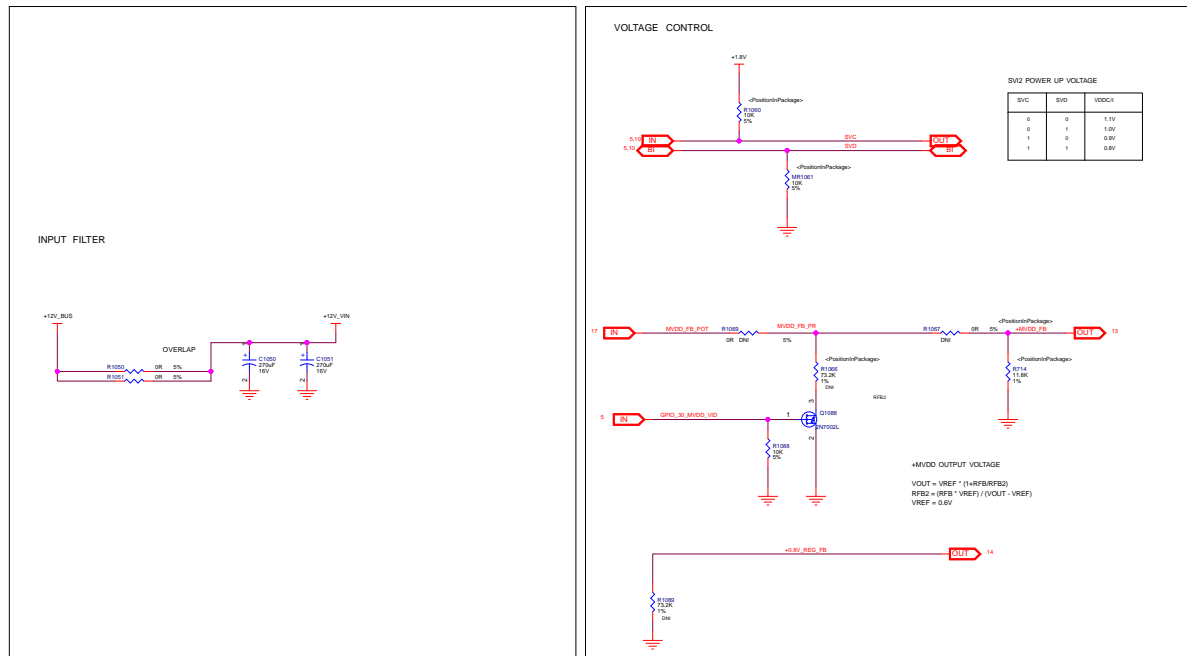
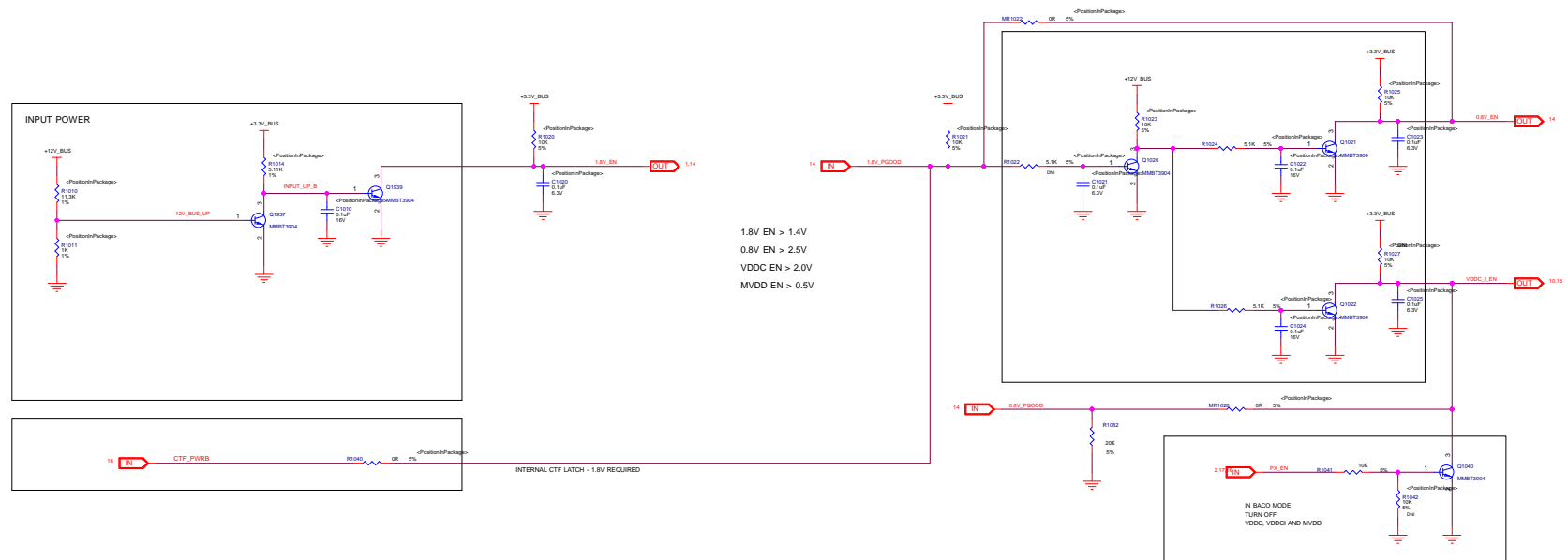


VR TEMPERATURE PROTECTION

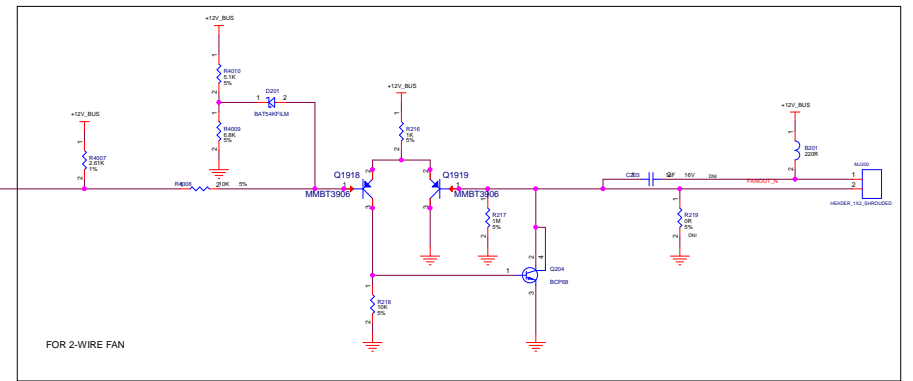
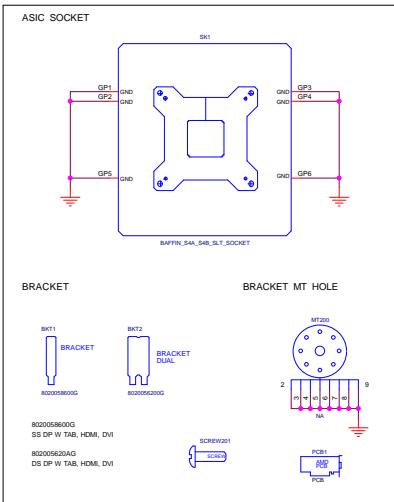
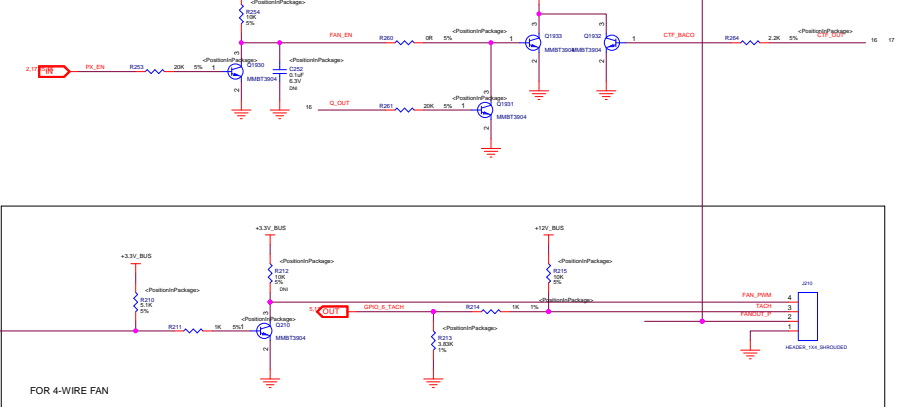
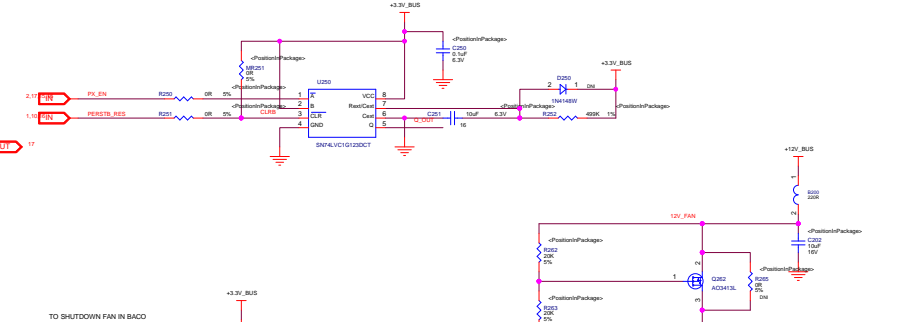




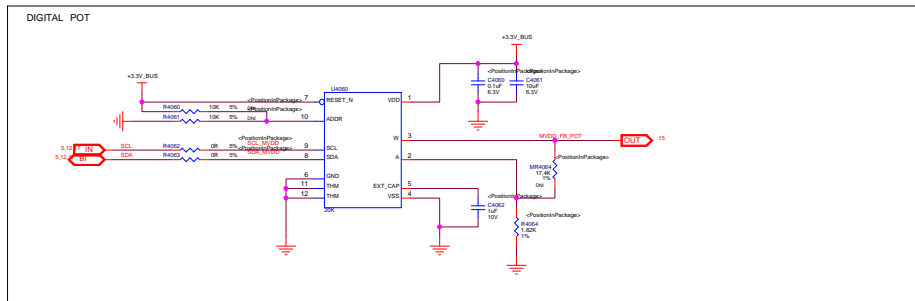
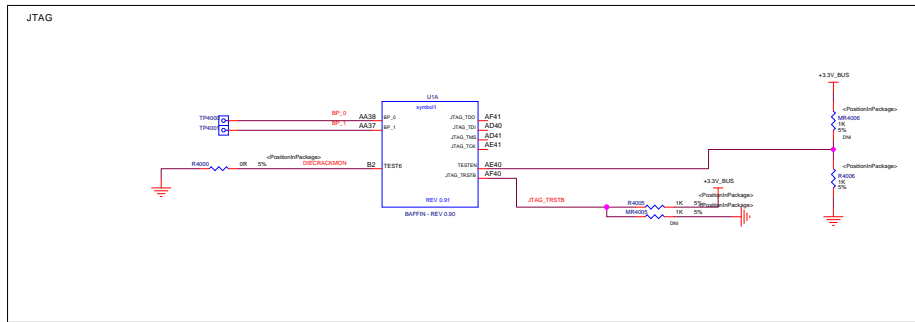
(16) POWER MANAGEMENT



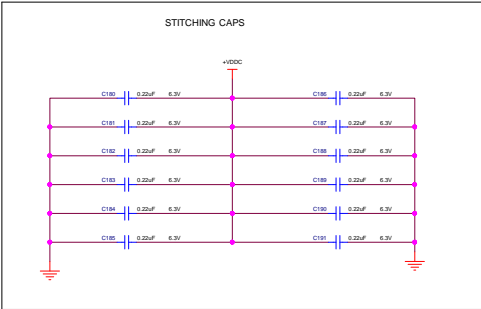
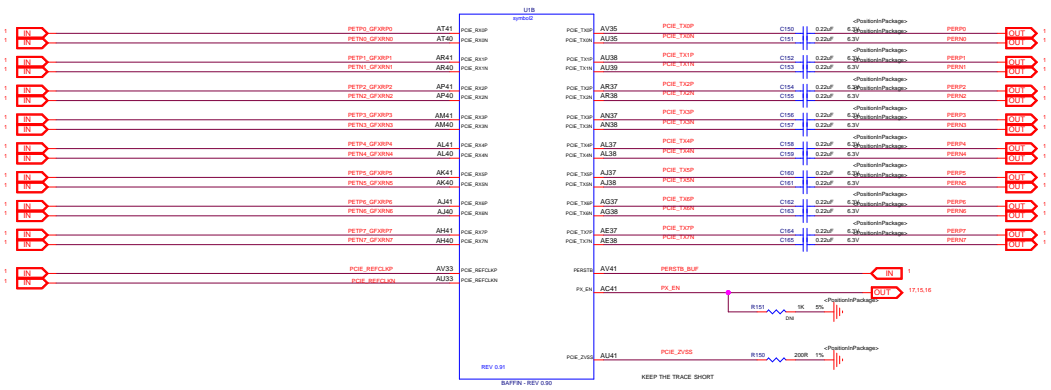
(17) THERMAL MANAGEMENT



(18) DEBUG CIRCUITS



(2) BAFFIN PCIE

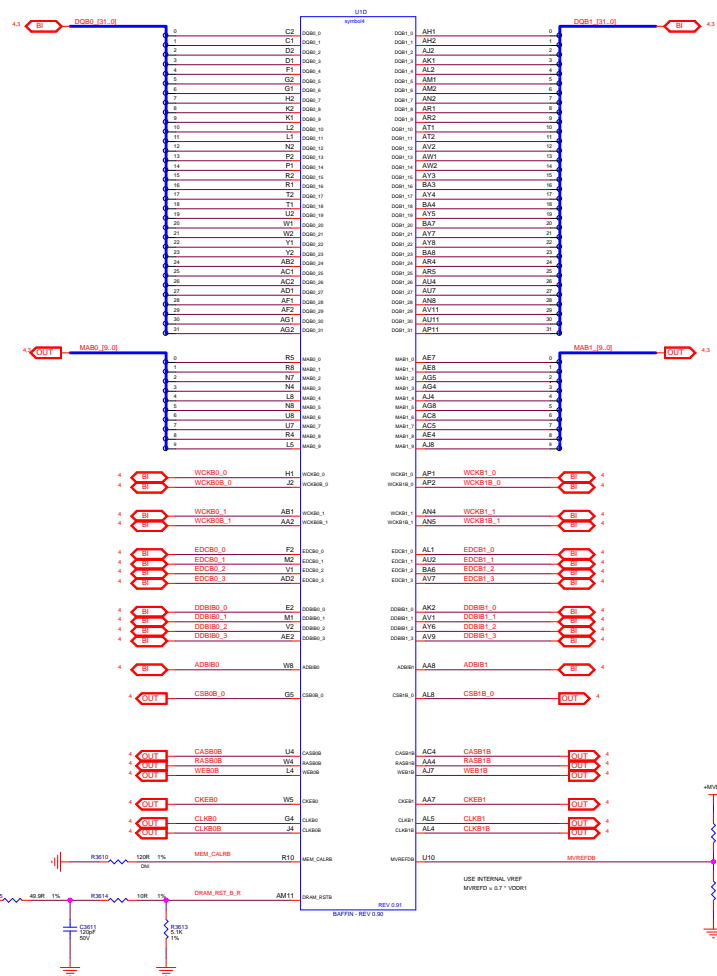
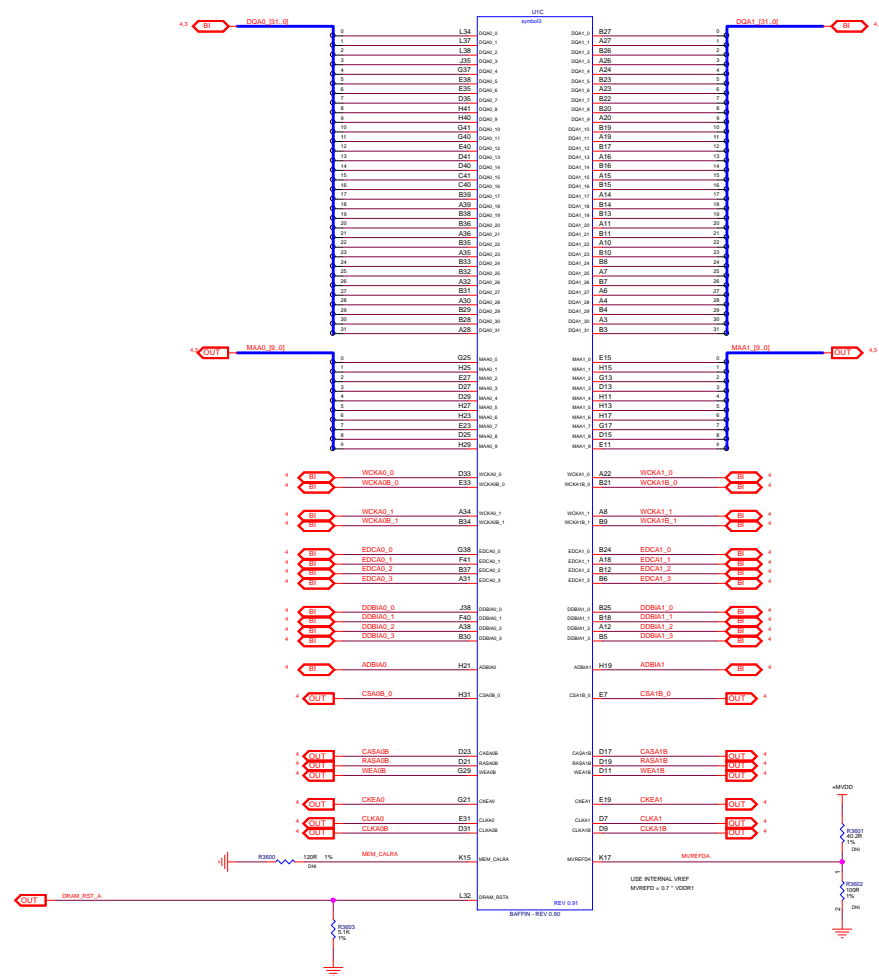


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SHANGHAI, CHINA 201203

SHEET: BAFFIN PCIE	
DATE: Mon Apr 11 07:16:00 2016	REV: 1.0
SHEET NUMBER: 2 OF 20	TITLE:
DOCUMENT NUMBER: 106_CXXX00_00A	TITLE

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(3) RACERX MEMORY INTERFACE



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SHEET: BAFFIN MEMORY

DATE: Mon Apr 11 07:15:00 2016

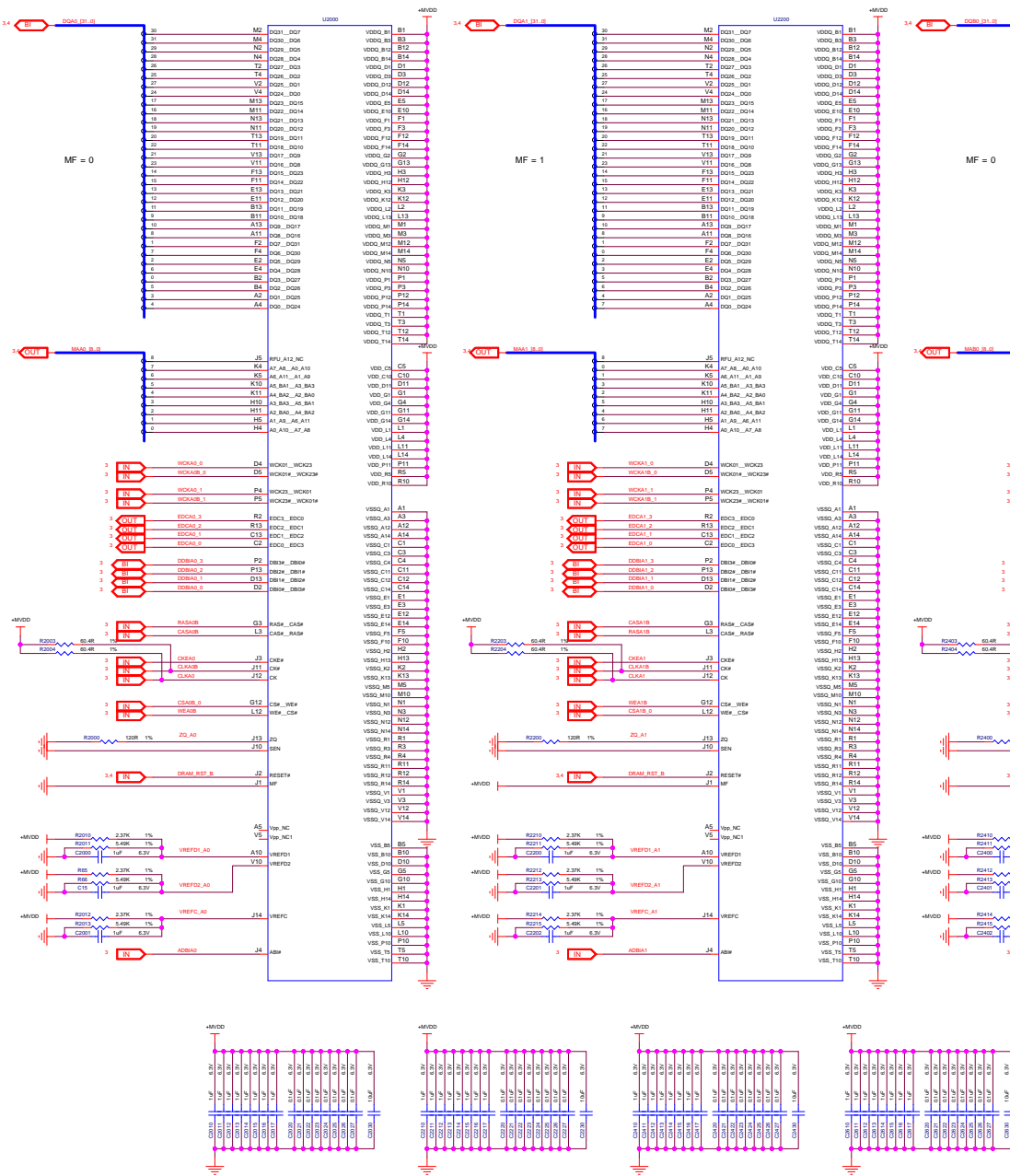
REV: 1.0

SHEET NUMBER: 3 OF 2

TITLE:	TITLE
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DOCUMENT NUMBER: 105_CXXX00_00

(4) GDDR5 CHAB x32



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SHEET: GDDR5 x32 CHAB

DATE: Mon Apr 11 07:16:01 2016

REV: 1.0

SHEET NUMBER: 4 OF 20

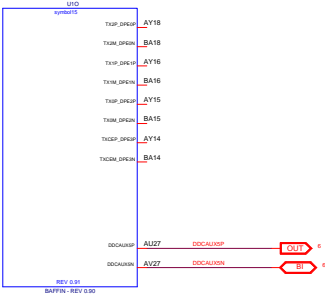
DOCUMENT NUMBER: 106_CXX000_00A

TITLE:


TITLE

(6) BAFFIN TMDPAB - dDVI

(8) BAFFIN TMDPE



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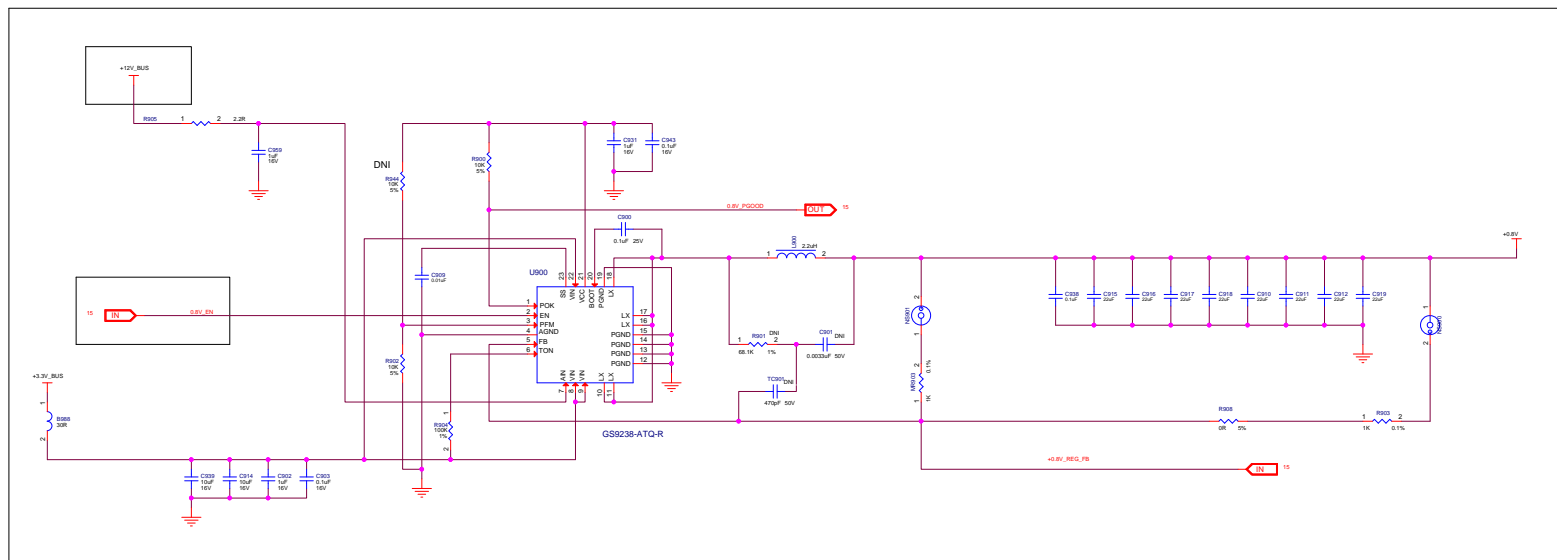


SHEET: BAFFIN TMDPE - NC	
DATE: Mon Apr 11 07:16:01 2016	REV: 1.0
SHEET NUMBER: 8 OF 20	
DOCUMENT NUMBER: 105_CXXX00_00A	

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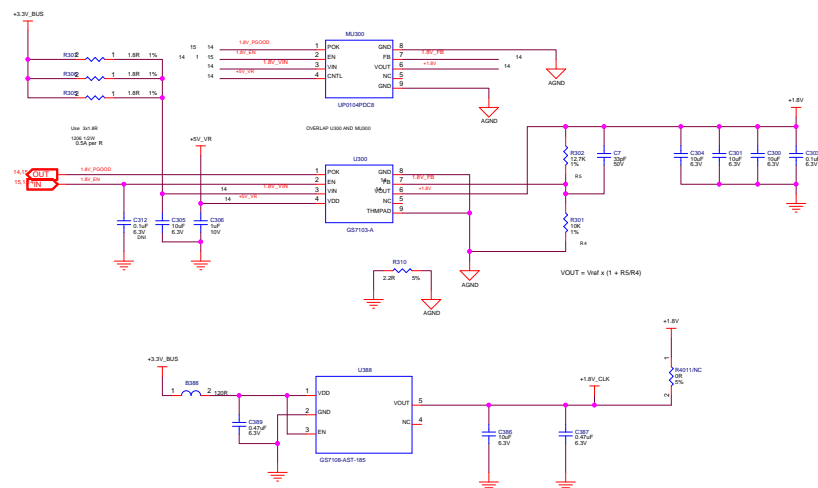
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(19) 0.8V

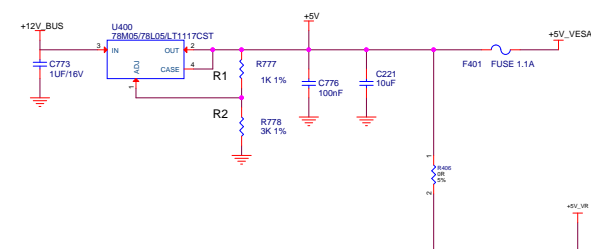



REGULATOR FOR +5V RAILS
IOUT MAX = 150mA

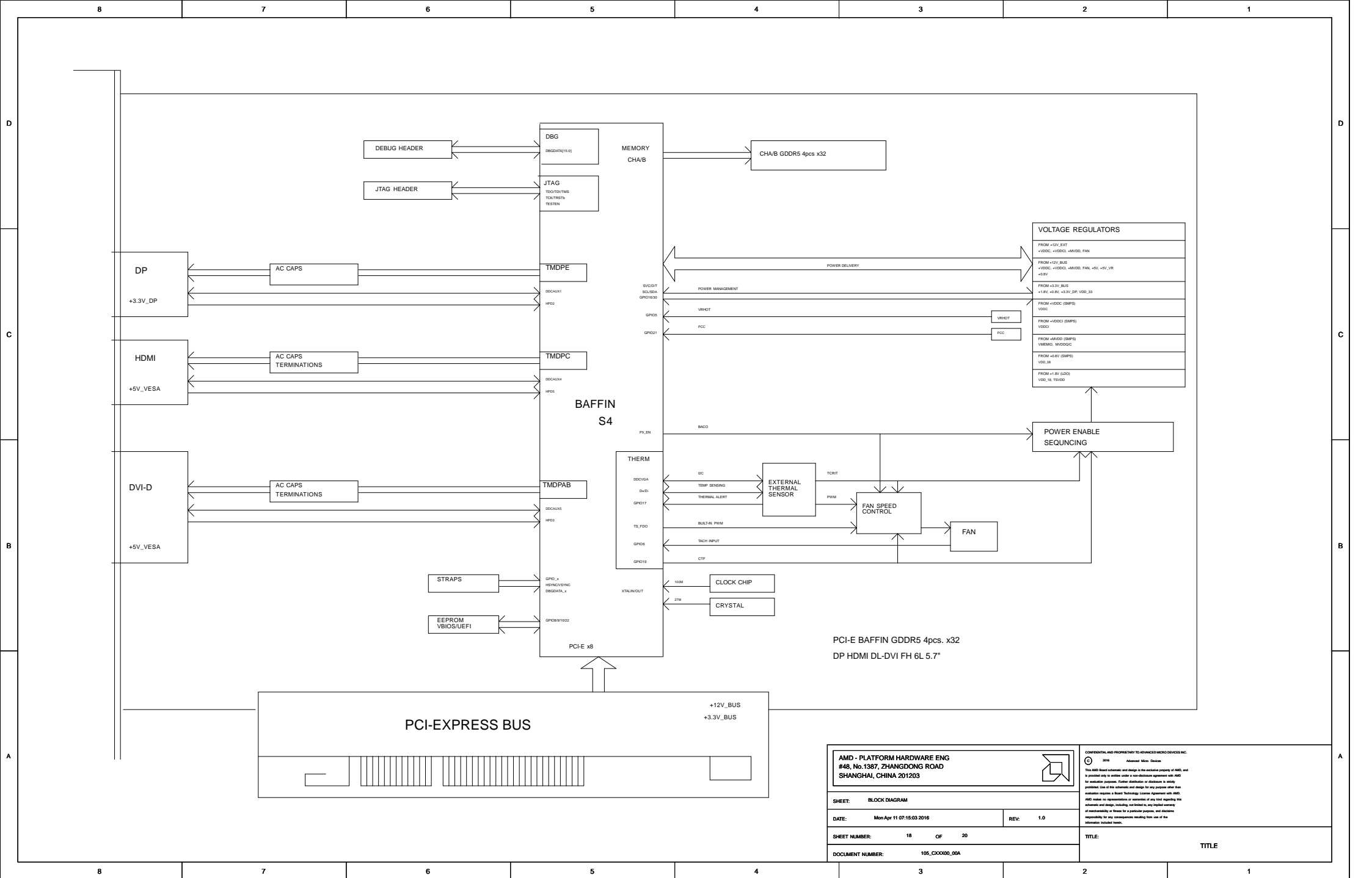
LDO #1: VIN = 3.0V TO 3.6V MAX VOUT = +1.8V +/- 2% IOUT = 1.3A RMS MAX
PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING



$$V_{out} = 1.25V \times (1 + R2/R1)$$



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<p>SHEET: 0.8V REG</p>	<p>REV: 1.0</p>
<p>DATE: Mon Apr 11 07:15:02 2016</p>	
<p>SHEET NUMBER: 14 OF 20</p>	
<p>DOCUMENT NUMBER: 105_CXX000_00A</p>	<p>TITLE:</p> <p style="text-align: center; font-weight: bold; font-size: 1.2em;">TITLE</p>
<p>NOTES: NOTE</p>	



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REVISION HISTORY				ENGINEER: XXX		NOTES: NOTE		<div>CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. This AMD Board schematic and design is the exclusive property of AMD, and is provided only to fulfill under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding this schematic and design, including, not limited to, any explicit warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.</div> <div>C 2016 Advanced Micro Devices</div> <div>AMD - PLATFORM HARDWARE ENG #48, No.1367, ZHANGDONG ROAD SHANGHAI, CHINA 201203</div>			
SCH Rev	PCB Rev	Date	REVISION DESCRIPTION								
0	00A	18/10/2015	INITIAL DESIGN								
1	00B	18/09/2015	AMD 1.0V1.020704 CLK 0200, AMD 100MHz CLOCK speed Change 0.001 power good pin up								

D

C

B

A


D

C

B

A

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D									D
C									C
B									B
A									A
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SHEET: SHEET TITLE		
DATE: Mon Apr 11 07:15:03 2016	REV: 1.0	
SHEET NUMBER: 20 OF 20		
DOCUMENT NUMBER: 105_CXX00_00A		
NOTES: NOTE		

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