MS-V094-0A-- G86GS, 128/256 Mb DDR3-136pin, VGA, DVI-I, SD/HDTV

SUMMARY:

1. Base on P456-A02 to Modify
2. BGA-136 DDRIII

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Page 3: FBA INTERFACE
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Page 13: TMDS LINK A & B
Page 14: TMDS LINK C & D
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Page 16: GPIO/ROM/HDCP ROM
Page 17: Straps/Mechanical
Page 18: Linear Power
Page 19: NVVDD,5V,A3V3
Page 20: FBVDDQ

Rev History

1.Remove VIDEO IN
2. Modify Page 9, Modify SLI circuit for G86

3.Modify Page 14, Remove TMDS LINK C&D circuit

4. Modify Page 15, Remove SPDIF circuit

5.Modify Page 20 FBVDDQ,PWM IC change to use 7210, Add LINEAR POWER & APW 7080

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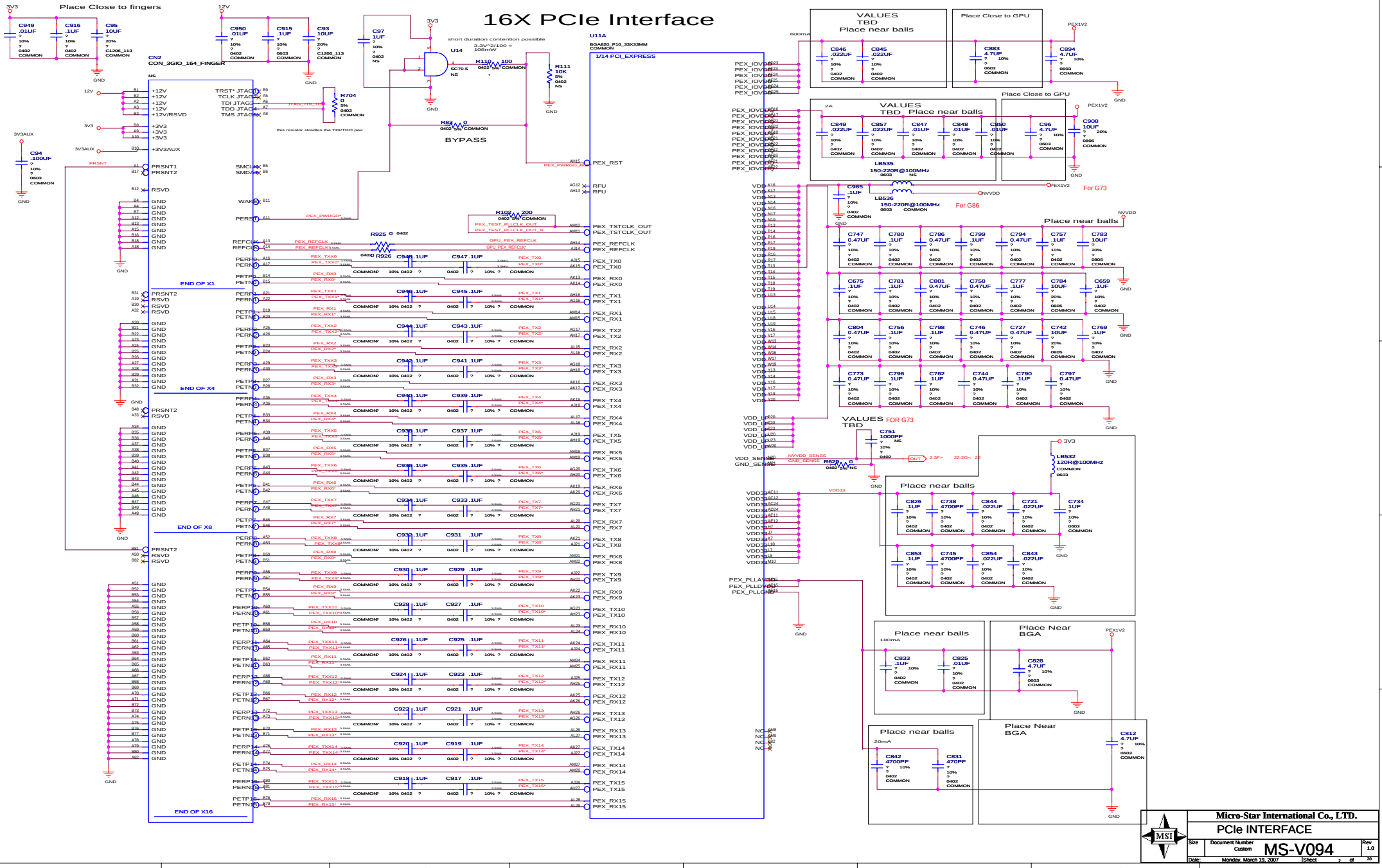
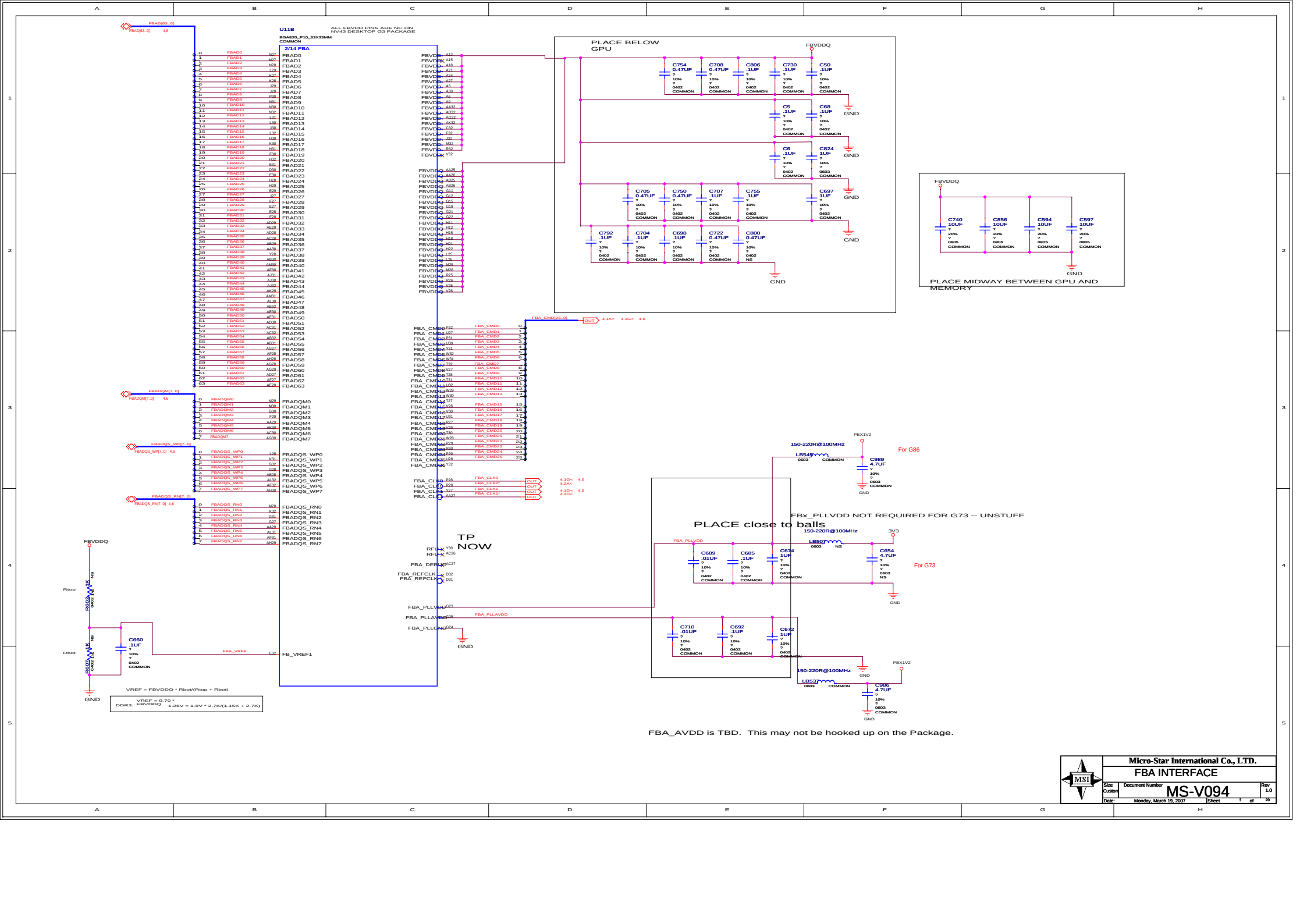
16X PCIe Interface




U11B
BGA820_P10_33X33MM
COMMON
2/14 FBA
ALL FBVDD PINS ARE NC ON NV43 DESKTOP G3 PACKAGE
PLACE BELOW GPU
FBVDDQ
PLACE MIDWAY BETWEEN GPU AND MEMORY
PLACE close to balls
FBx_PLLVDD NOT REQUIRED FOR G73 -- UNSTUFF
For G86
For G73
TP NOW
FBA_AVDD is TBD. This may not be hooked up on the Package.
VREF = FBVDDQ * Rbot/(Rtop + Rbot)
VREF = 0.70 * FBVDDQ 1.26V = 1.8V * 2.7K/(1.15K + 2.7K)
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FBA INTERFACE
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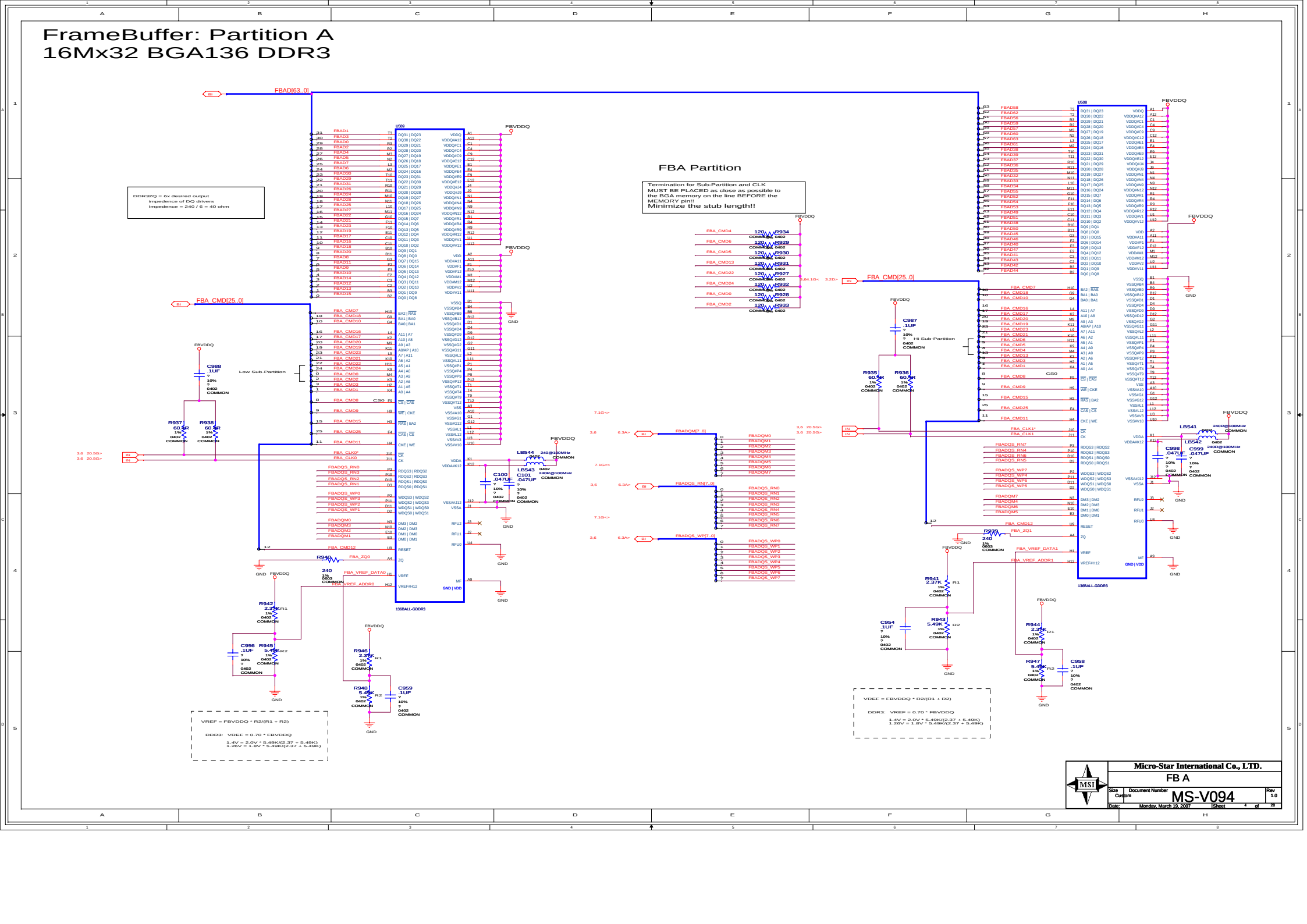
FrameBuffer: Partition A
16Mx32 BGA136 DDR3



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FB A	
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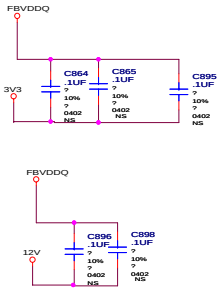
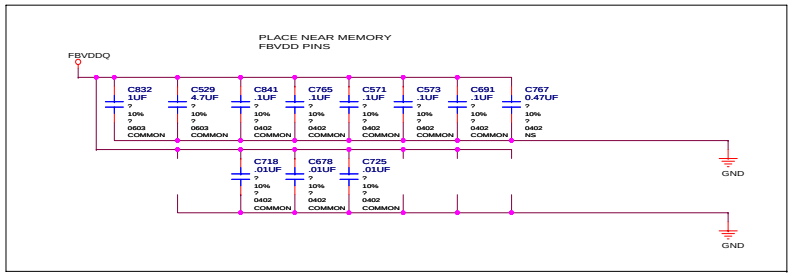
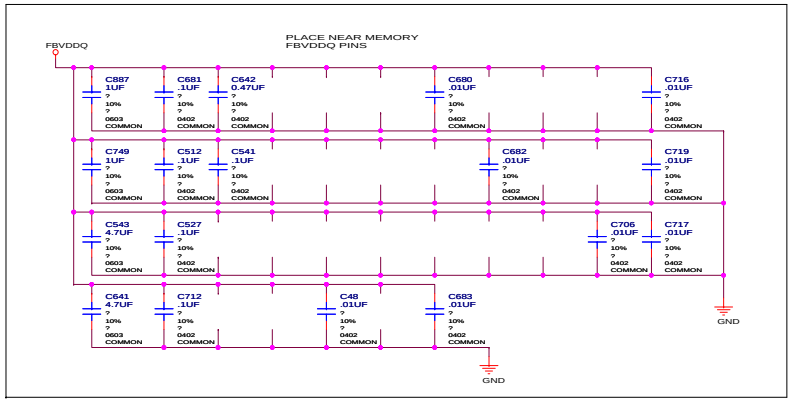
FRAME BUFFER: PARTITION A DECOUPLING

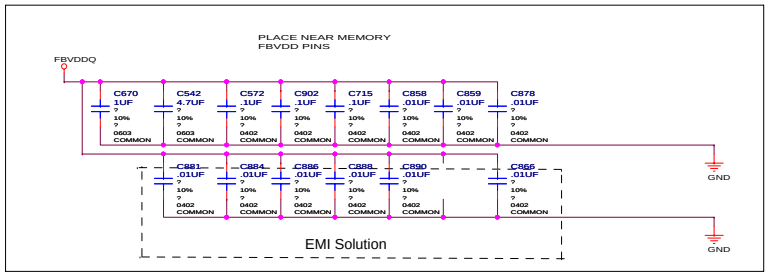
Decoupling for FBA 0..31

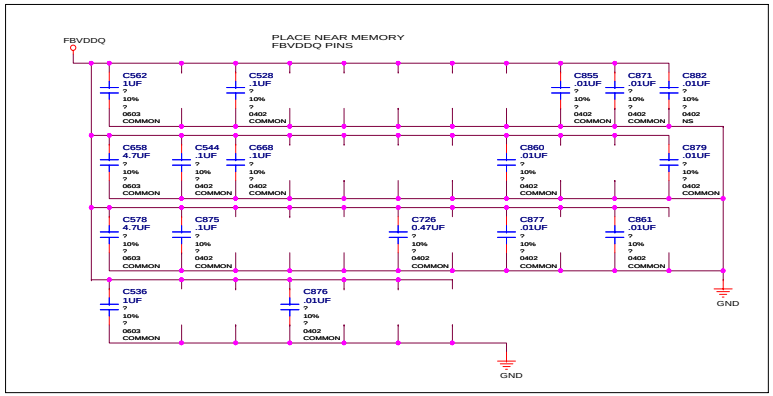






Decoupling for FBA 32..63





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FBA DECOUPLING		
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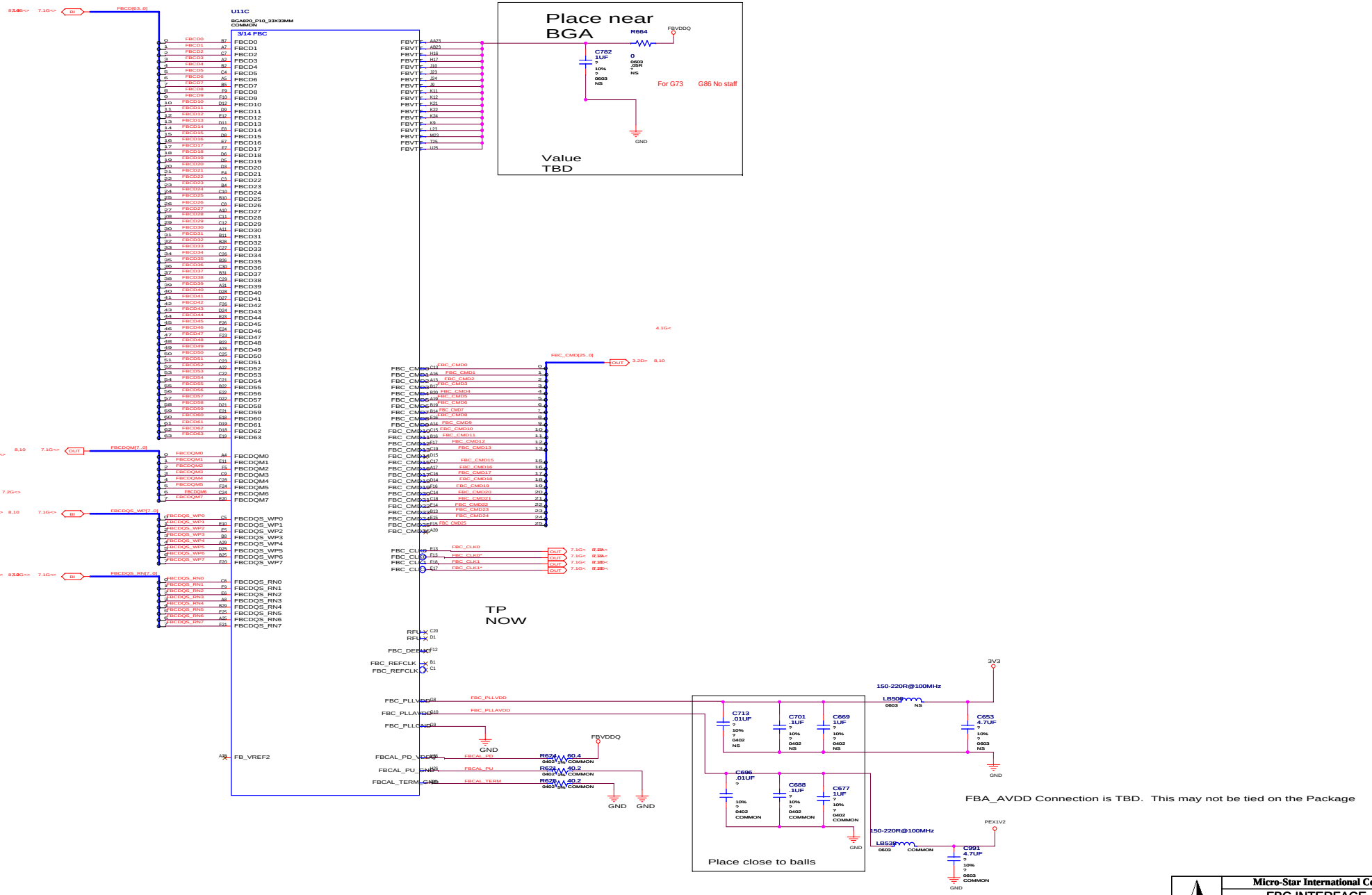
U11C
BGA820_P10_33X33MM
COMMON
3/14 FBC
Place near BGA
R664
FBVDDQ
C782 1UF
0 0603
For G73
G86 No staff
GND
Value TBD
FBC_CMD[25..0]
FBCDQM[7..0]
FBCDQS_WP[7..0]
FBCDQS_RN[7..0]
FBC[63..0]
TP NOW
FB_VREF2
FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_TERM_GND
R624 60.4
R623 40.2
R625 40.2
FBA_AVDD Connection is TBD. This may not be tied on the Package
Place close to balls
3V3
150-220R@100MHz
LB509
LB538
C713 .01UF
C701 .1UF
C669 1UF
C653 4.7UF
C686 .01UF
C688 .1UF
C677 1UF
C991 4.7UF
PEX1V2
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FBC INTERFACE
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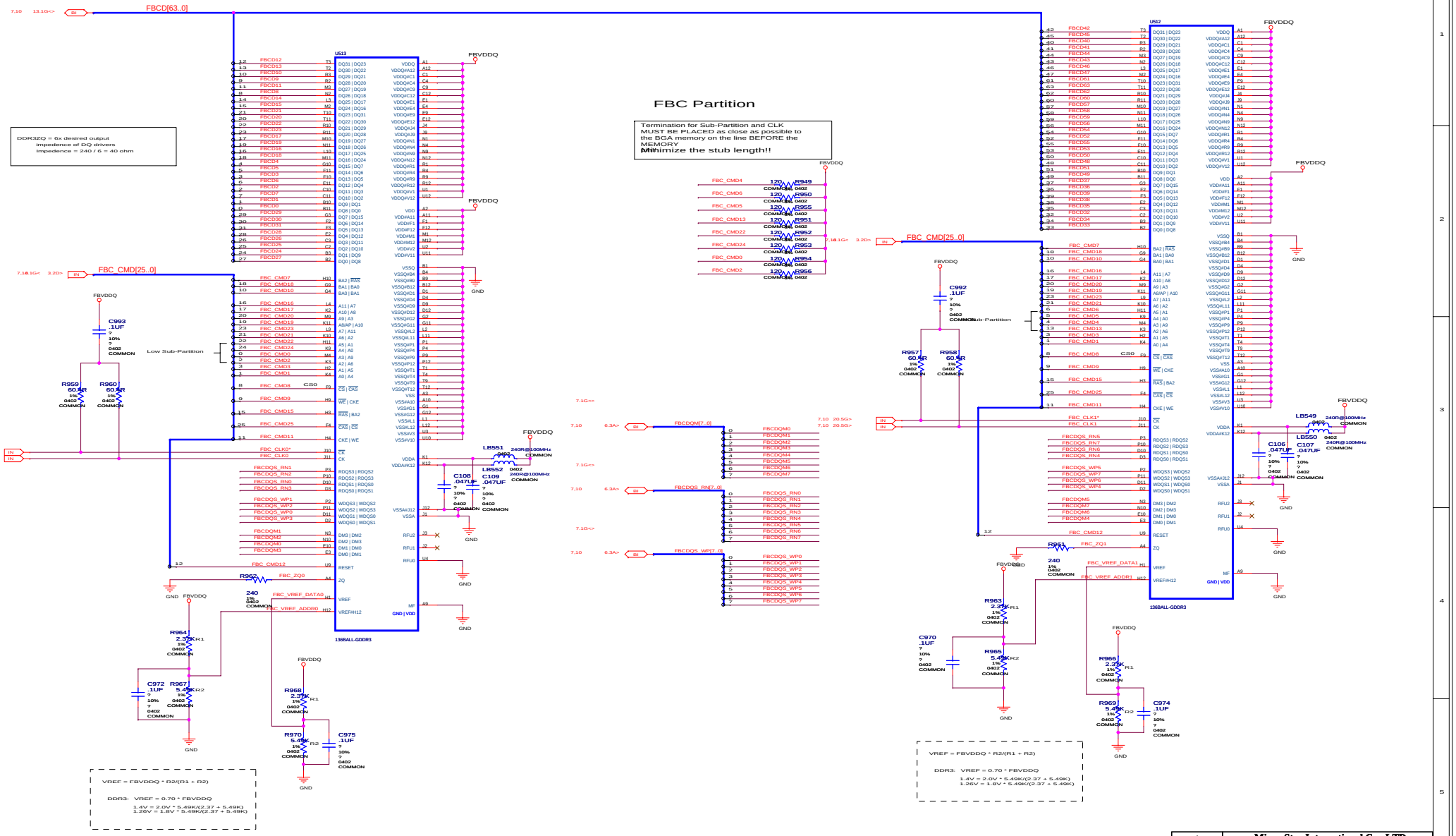
FRAMEBUFFER: PARTITION
C 16Mx32 BGA136 DDR3



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FB C	
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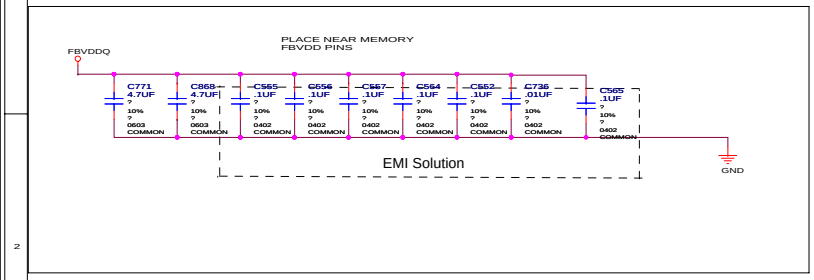
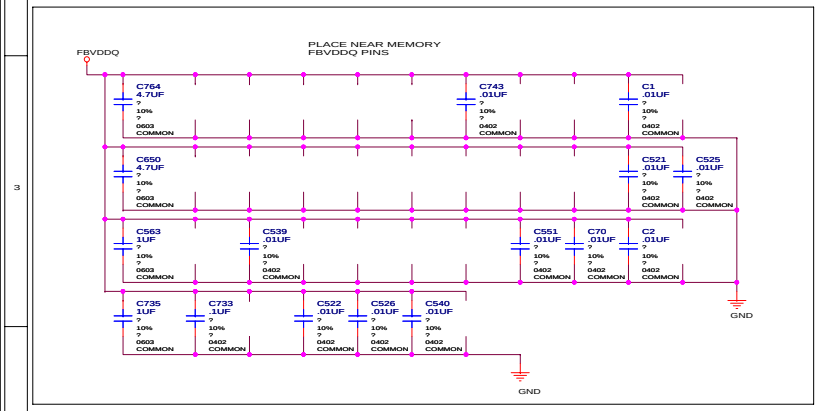
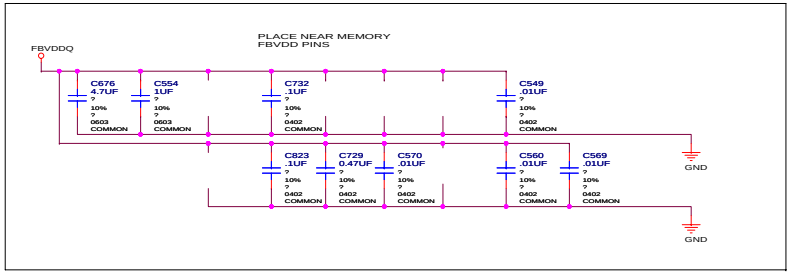
FRAMEBUFFER: PARTITION C DECOUPLING

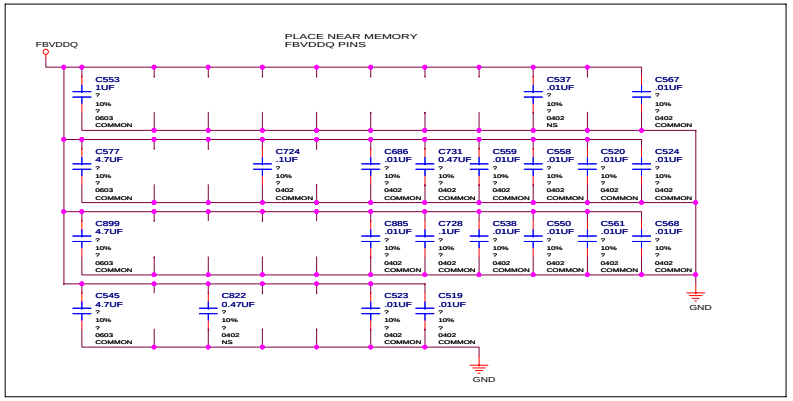
Decoupling for FBC 0..31

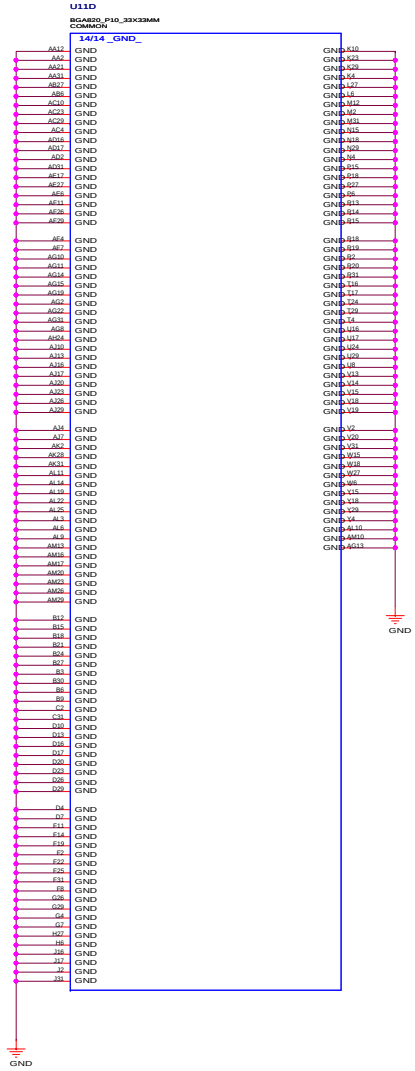




Decoupling for FBC 32..63







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FBC DECOUPLING		
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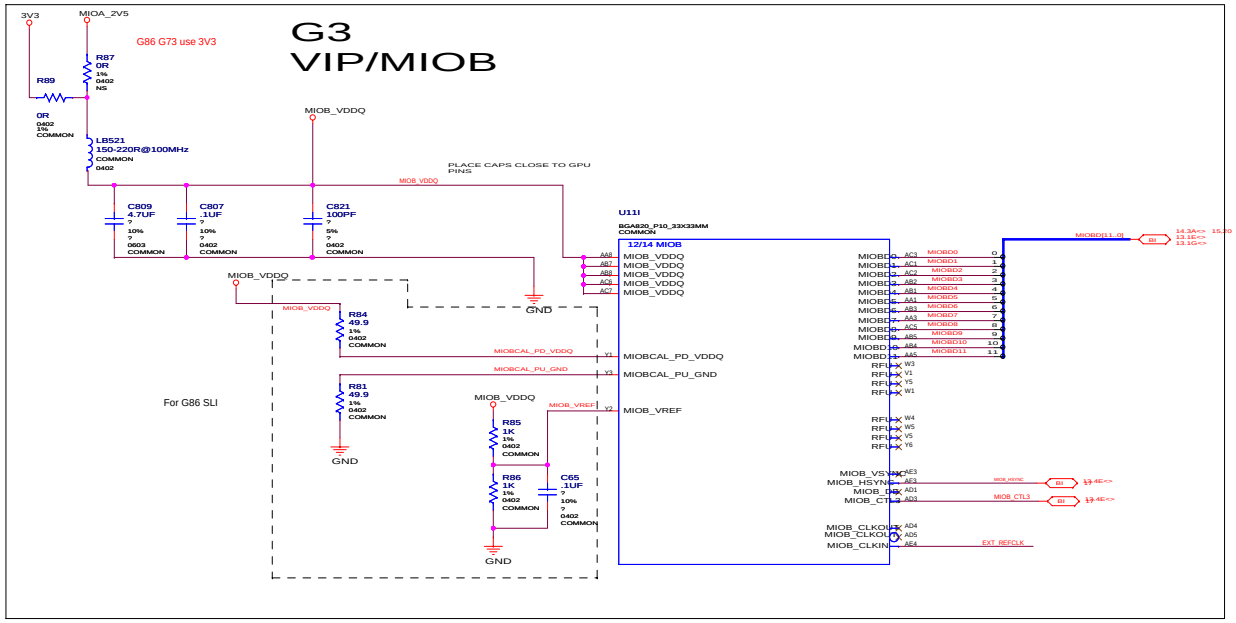

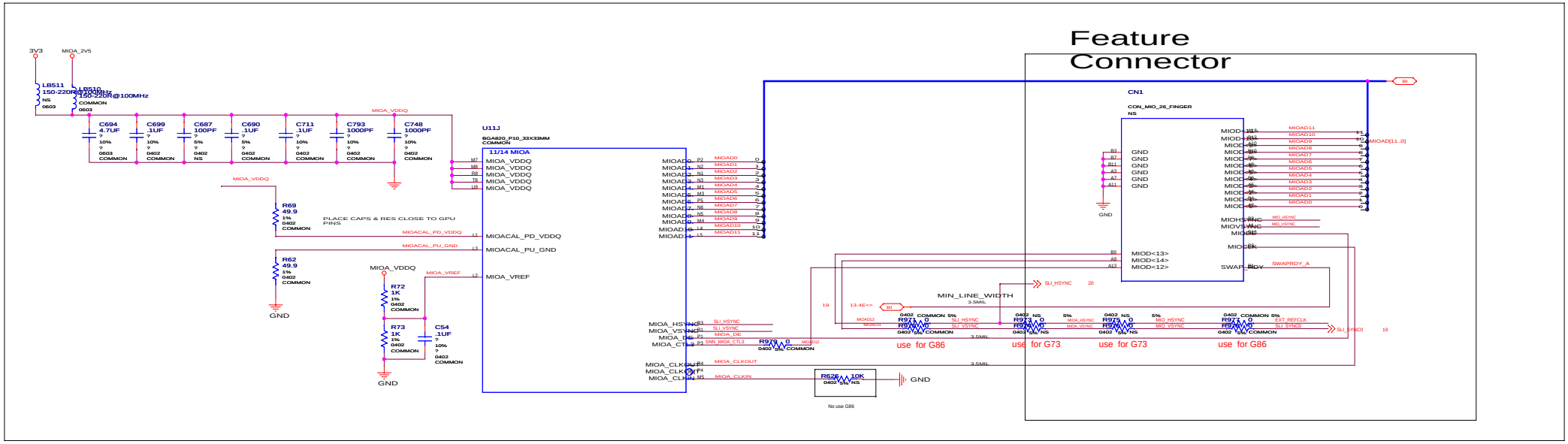

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MIOA/MIOB	
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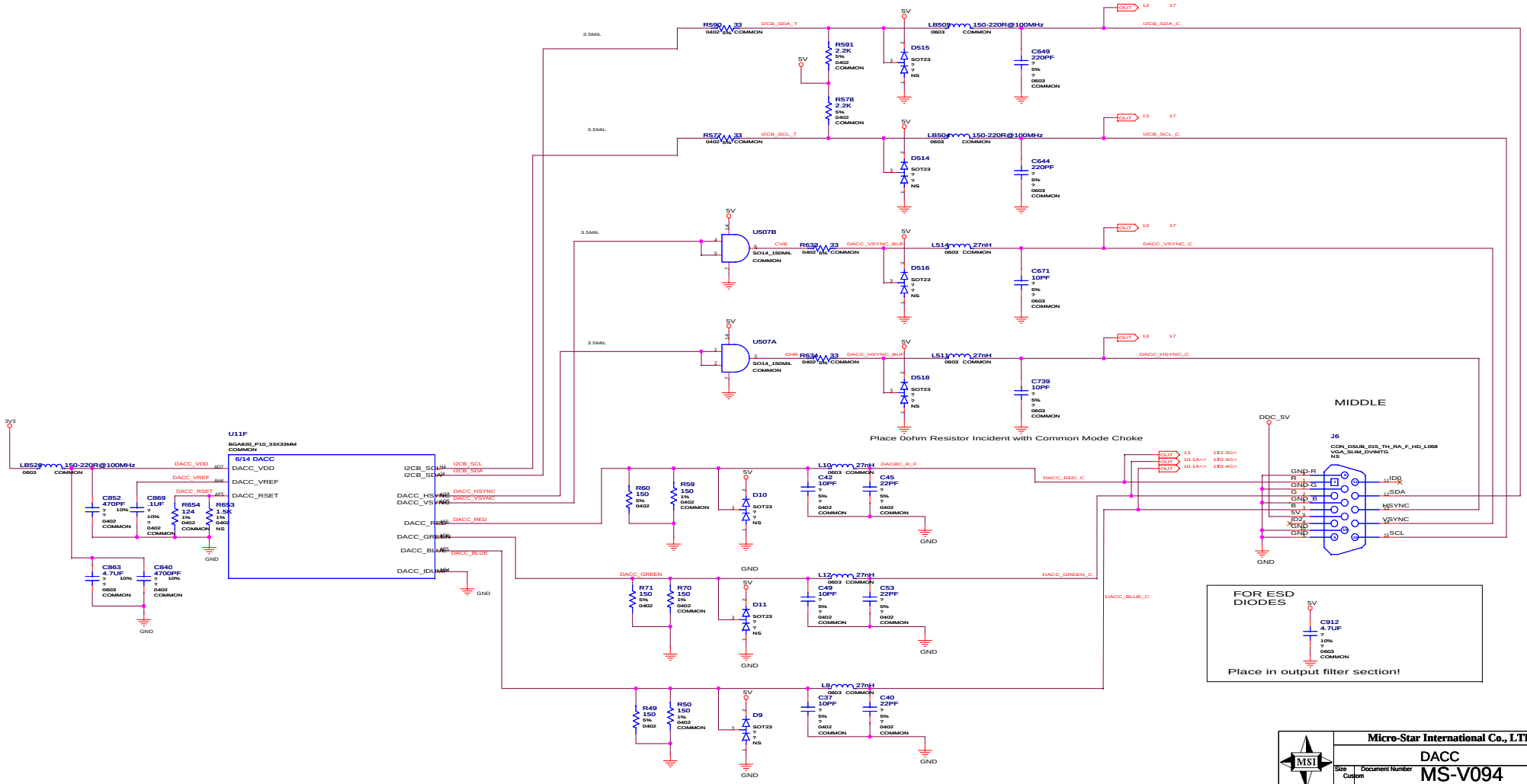
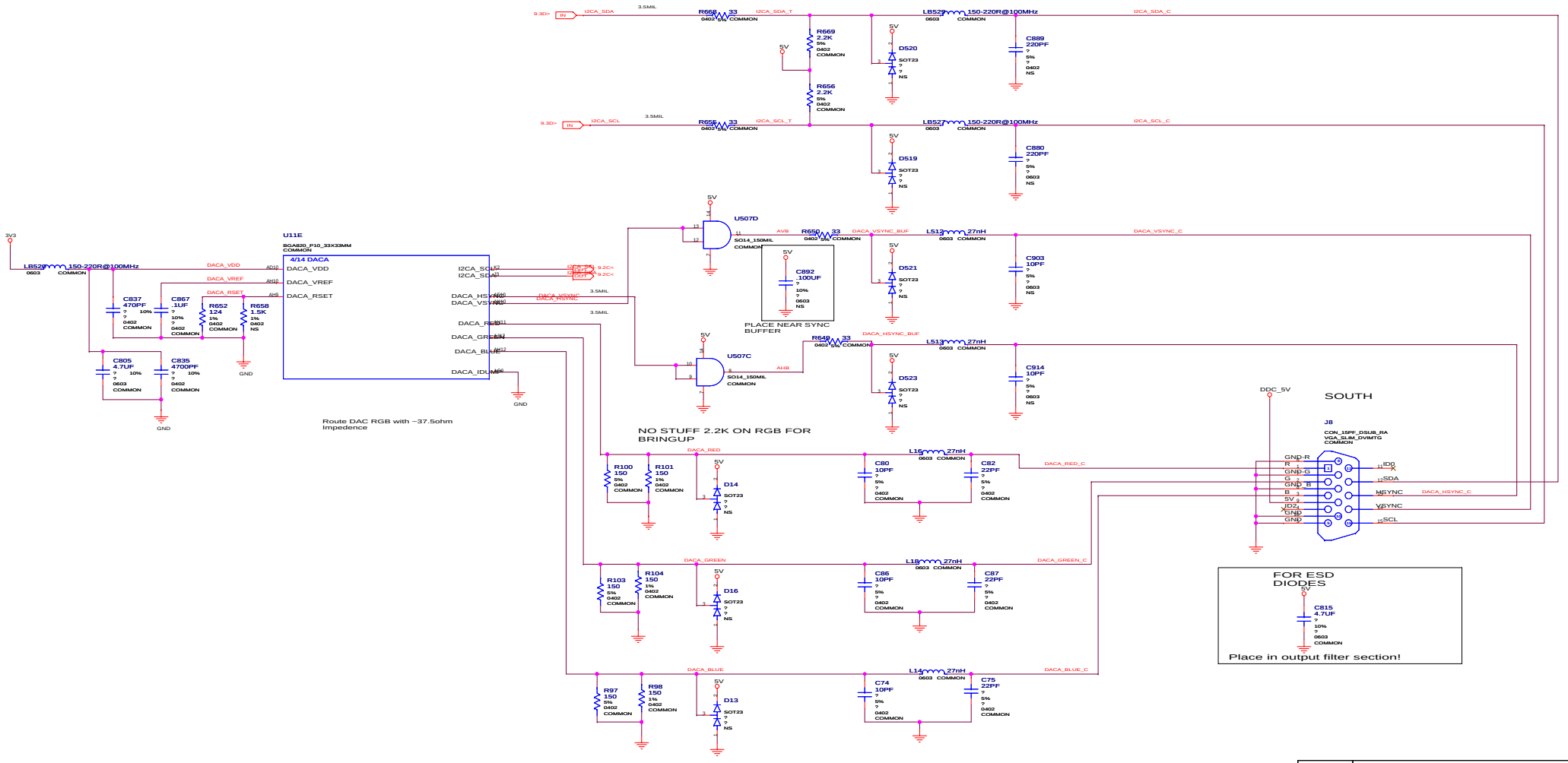
Secondary Display (DACC), Slim DB15

DACC RGB-FILTER



Primary Display (DACA), Slim DB15

DACA
RGB-FILTER



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DACA			
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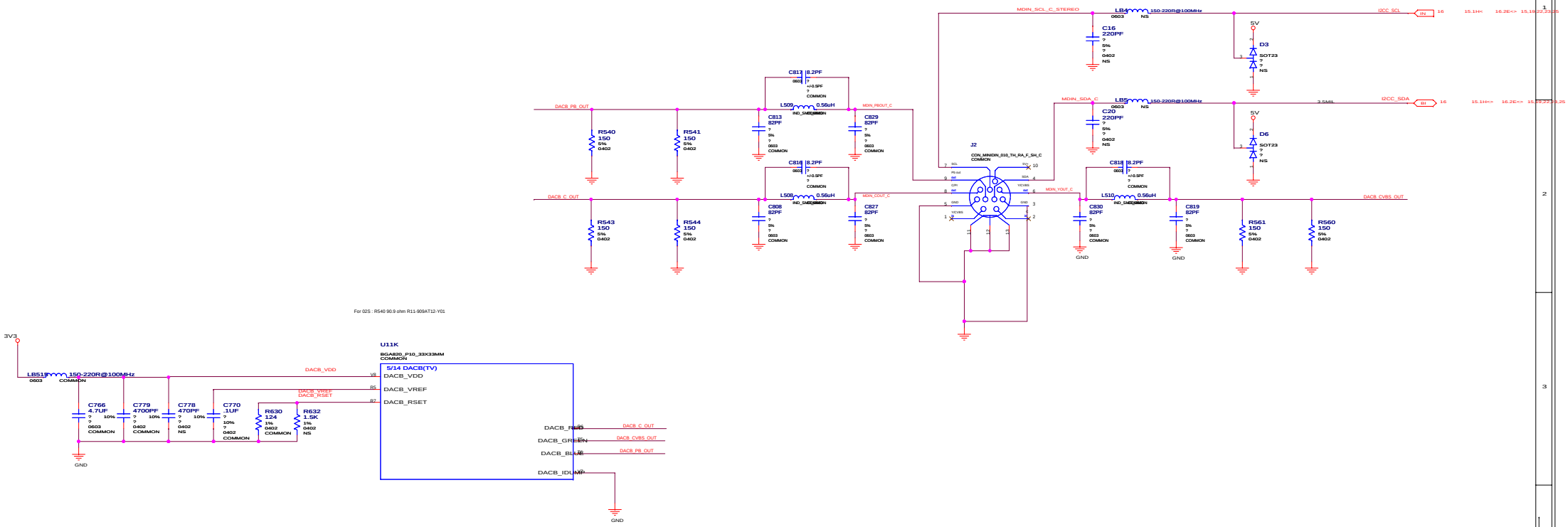
DACB .. MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES



For 02S : R540 90.9 ohm R11-909AT12-Y01

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DACB	
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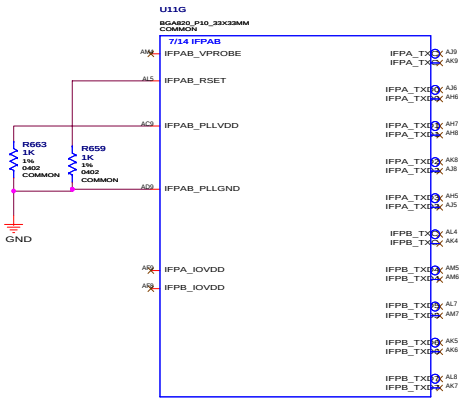
INTERNAL
TMDS .. LINK A
& B



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TMDS LINK A & B		
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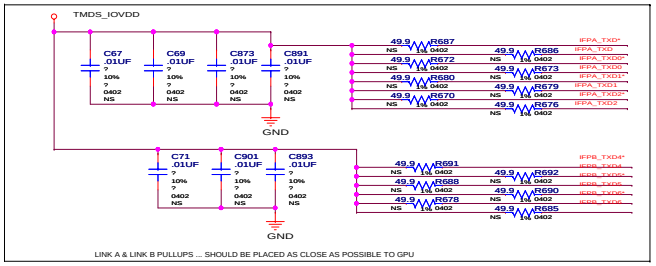
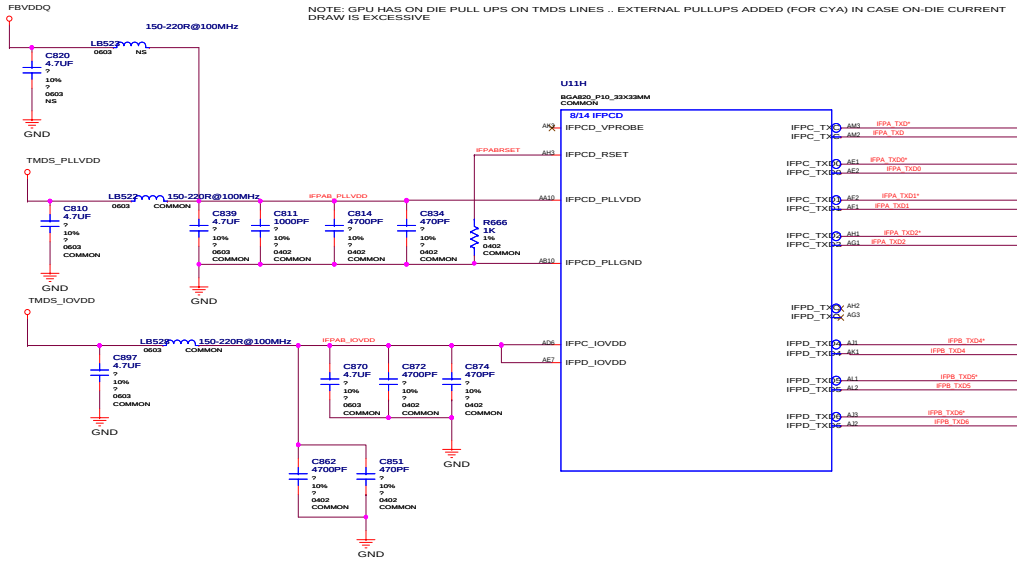
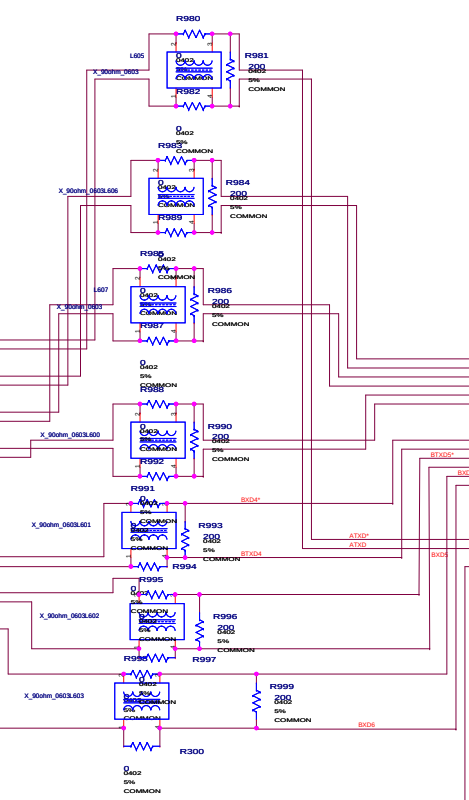
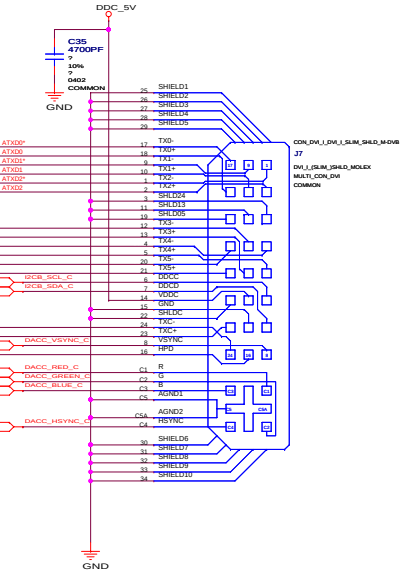
INTERNAL TMDS .. LINK C & D



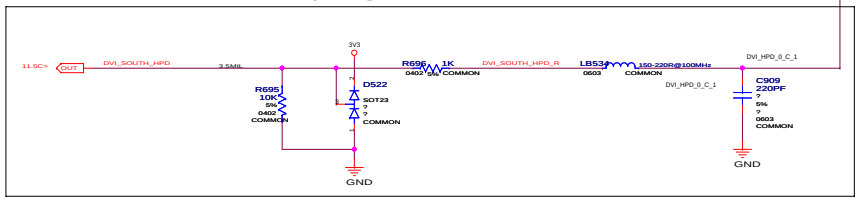
NOTE: GPU HAS ON DIE PULL UPS ON TMDS LINES .. EXTERNAL PULLUPS ADDED (FOR CYA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE







Hotplug Detection



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TMDS LINK C & D	
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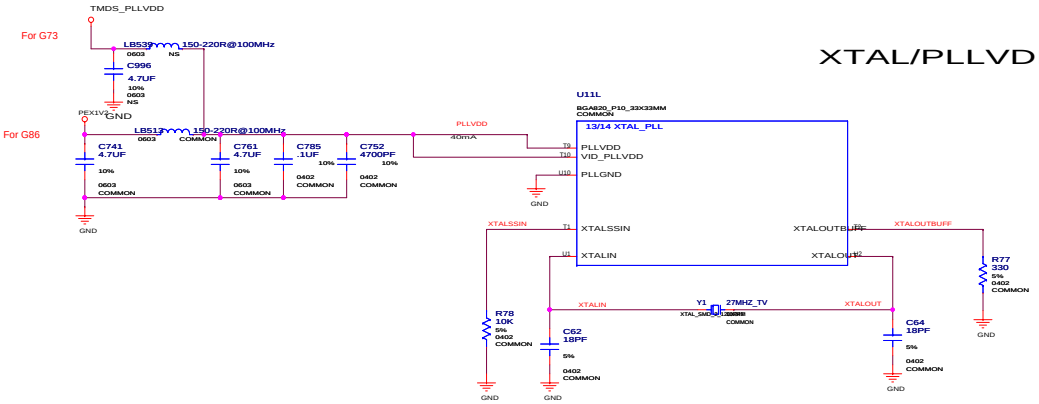
XTAL/PLLVDD



XTAL/PLLVDD

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XTAL/PLLVDD/SPDIF IN			
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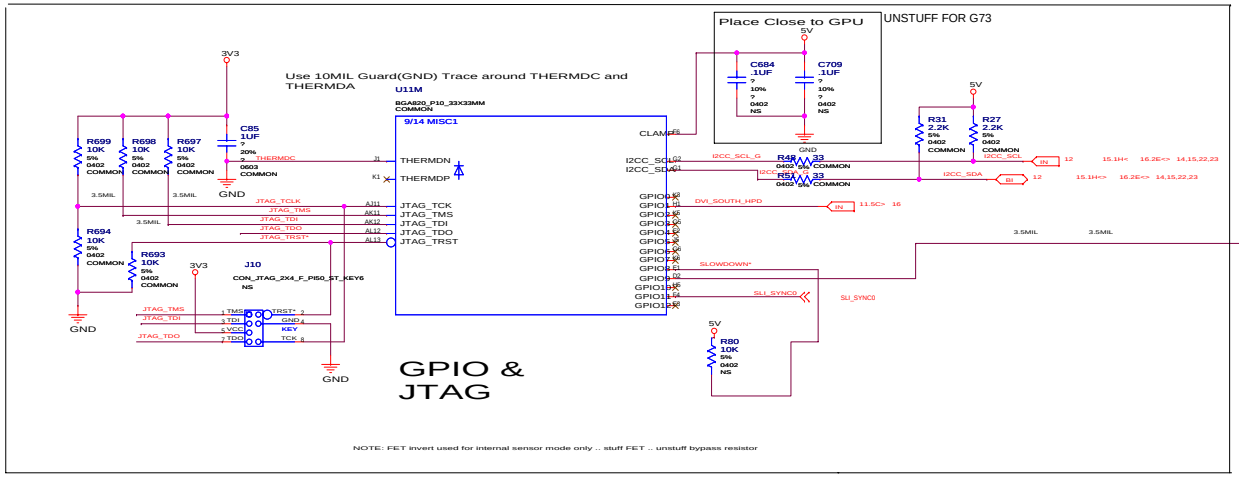
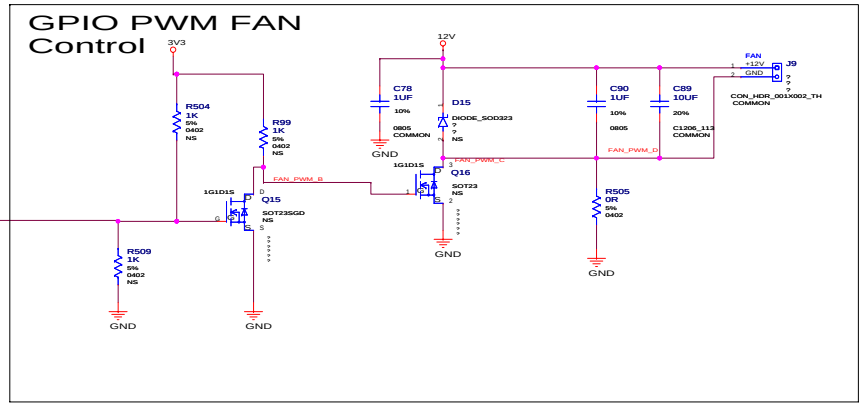
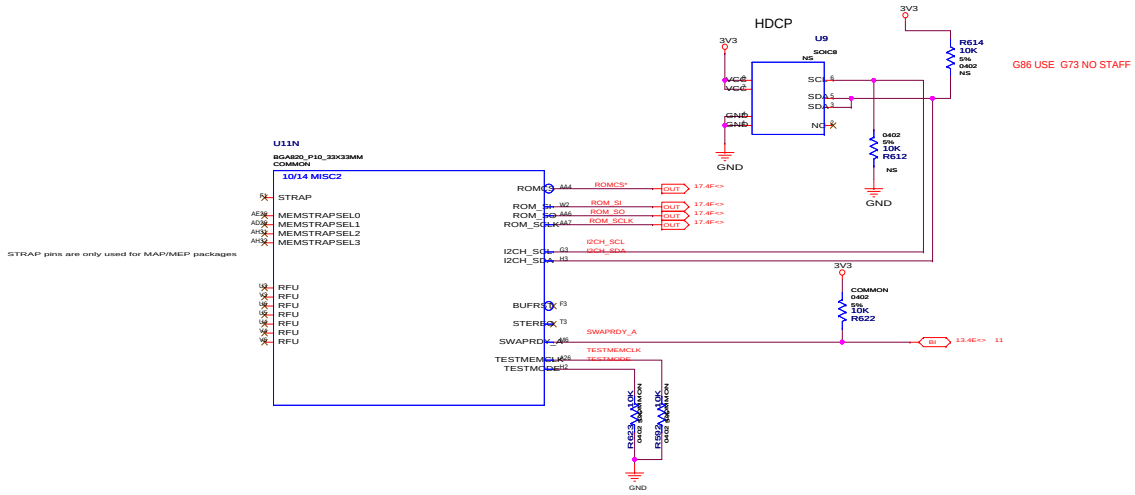
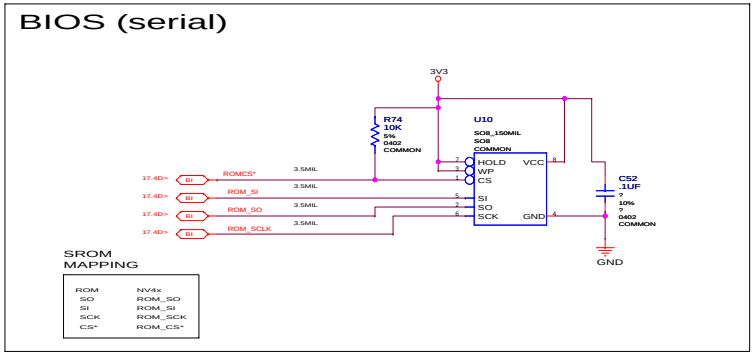




GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	DVI SOUTH HOTPLUG DET
2	IN	RESERVED
3	IN	RESERVED
4	IN	TUNER IRQ
5	OUT	NVVDD VOLTAGE SELECT 0
6	OUT	NVVDD VOLTAGE SELECT 1
7	IN	RESERVED
8	IN	RESERVED
9	OUT	PWM FAN
10	IN	RESERVED
11	IN	TVRSET
12	IN	RESERVED





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GPIO/ROM/HDCP ROM	
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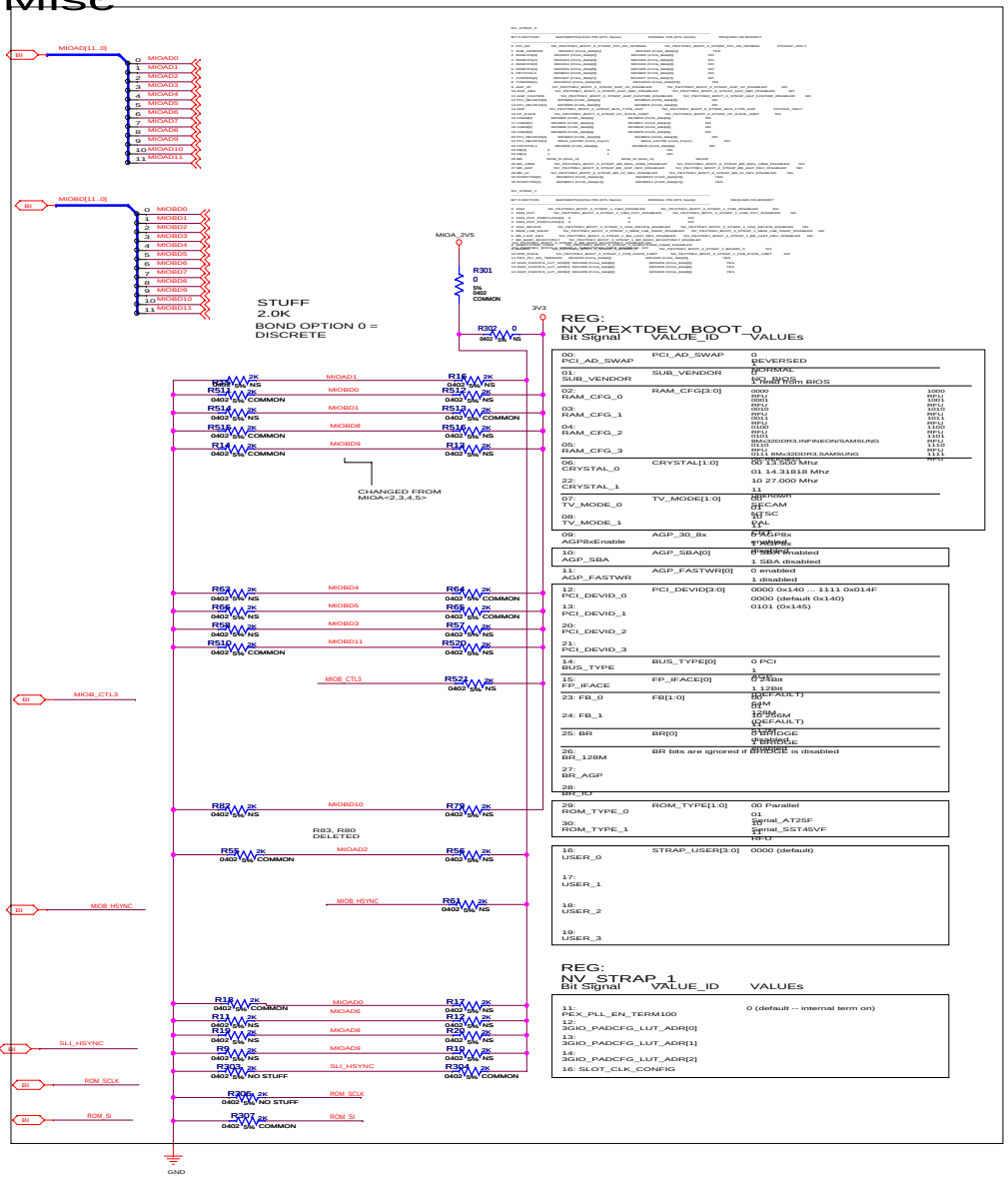
BIOS, Straps, Misc

Straps

Assembly: BIOS



REG: NV_PEXTDEV_BOOT_0

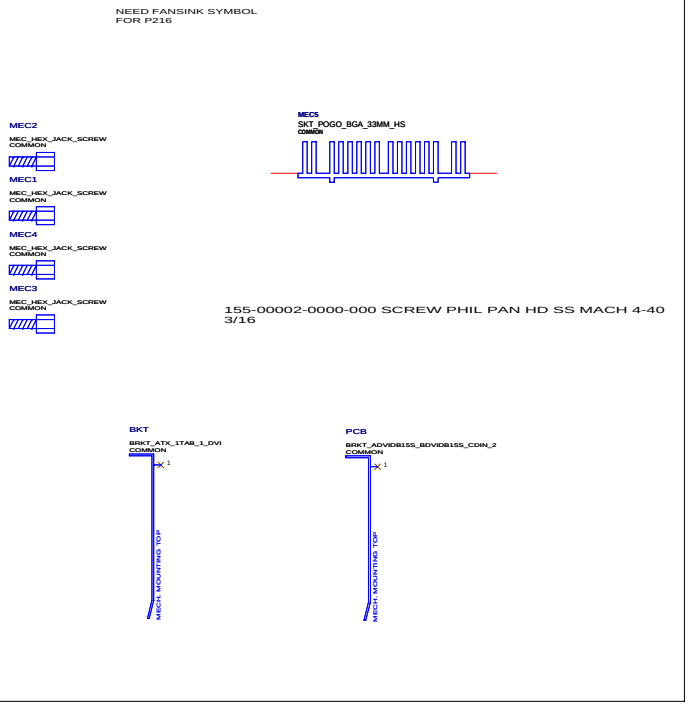
Bit	Signal	VALUE_ID	VALUEs
00:	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED 1 NORMAL
01:	SUB_VENDOR	SUB_VENDOR	0 NO BIOS 1 Read from BIOS
02:	RAM_CFG_0	RAM_CFG[3:0]	0000 RFU 0001 RFU 0010 RFU 0011 RFU 0100 RFU 0101 RFU 0110 RFU 0111 8MG32DDR3,SAMSUNG 1000 RFU 1001 RFU 1010 RFU 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 RFU
03:	RAM_CFG_1		
04:	RAM_CFG_2		
05:	RAM_CFG_3		
06:	CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz 01 14.31818 Mhz 10 27.000 Mhz 11
22:	CRYSTAL_1		
07:	TV_MODE_0	TV_MODE[1:0]	00 NTSC 01 SECAM 10 PAL 11 RFU
08:	TV_MODE_1		
09:	AGP8xEnable	AGP_30_8x	0 AGP8x enabled 1 AGP8x disabled
10:	AGP_SBA	AGP_SBA[0]	0 SBA enabled 1 SBA disabled
11:	AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled
12:	PCI_DEVID_0	PCI_DEVID[3:0]	0000 0x140 .. 1111 0x014F 0000 (default 0x140) 0101 (0x145)
13:	PCI_DEVID_1		
20:	PCI_DEVID_2		
21:	PCI_DEVID_3		
14:	BUS_TYPE	BUS_TYPE[0]	0 PCI 1 AGP
15:	FP_IFACE	FP_IFACE[0]	0 24bit 1 12Bit
23:	FB_0	FB[1:0]	00 (DEFAULT) 64M 128M 256M (DEFAULT) 11
24:	FB_1		
25:	BR	BR[0]	0 BRIDGE disabled 1 BRIDGE enabled
26:	BR_128M	BR bits are ignored if BRIDGE is disabled	
27:	BR_AGP		
28:	BR_IO		
29:	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F 10 Serial_SST45VF RFU
30:	ROM_TYPE_1		
16:	USER_0	STRAP_USER[3:0]	0000 (default)
17:	USER_1		
18:	USER_2		
19:	USER_3		

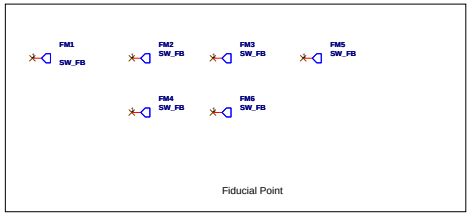
REG: NV_STRAP_1

Bit	Signal	VALUE_ID	VALUEs
11:	PEX_PLL_EN_TERM100		0 (default -- internal term on)
12:	3GIO_PADCFG_LUT_ADR[0]		
13:	3GIO_PADCFG_LUT_ADR[1]		
14:	3GIO_PADCFG_LUT_ADR[2]		
16:	SLOT_CLK_CONFIG		

Mechanical parts

NEED FANSINK SYMBOL FOR P216





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Straps/Mechanical	
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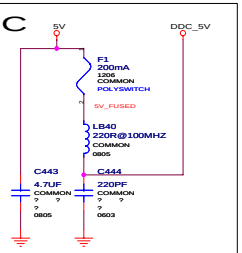
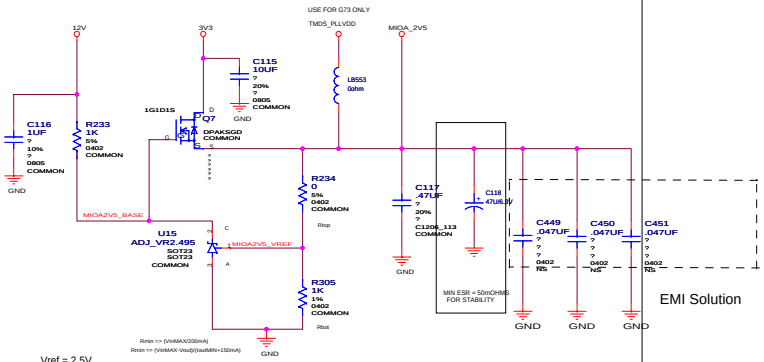
Power Supply TMDS/MIOA/DDC

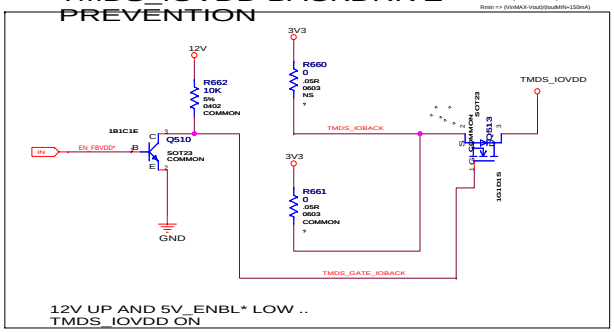
DDC 5V



MIOA_VDDQ



TMDS_IOVDD BACKDRIVE PREVENTION



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Linear Power	
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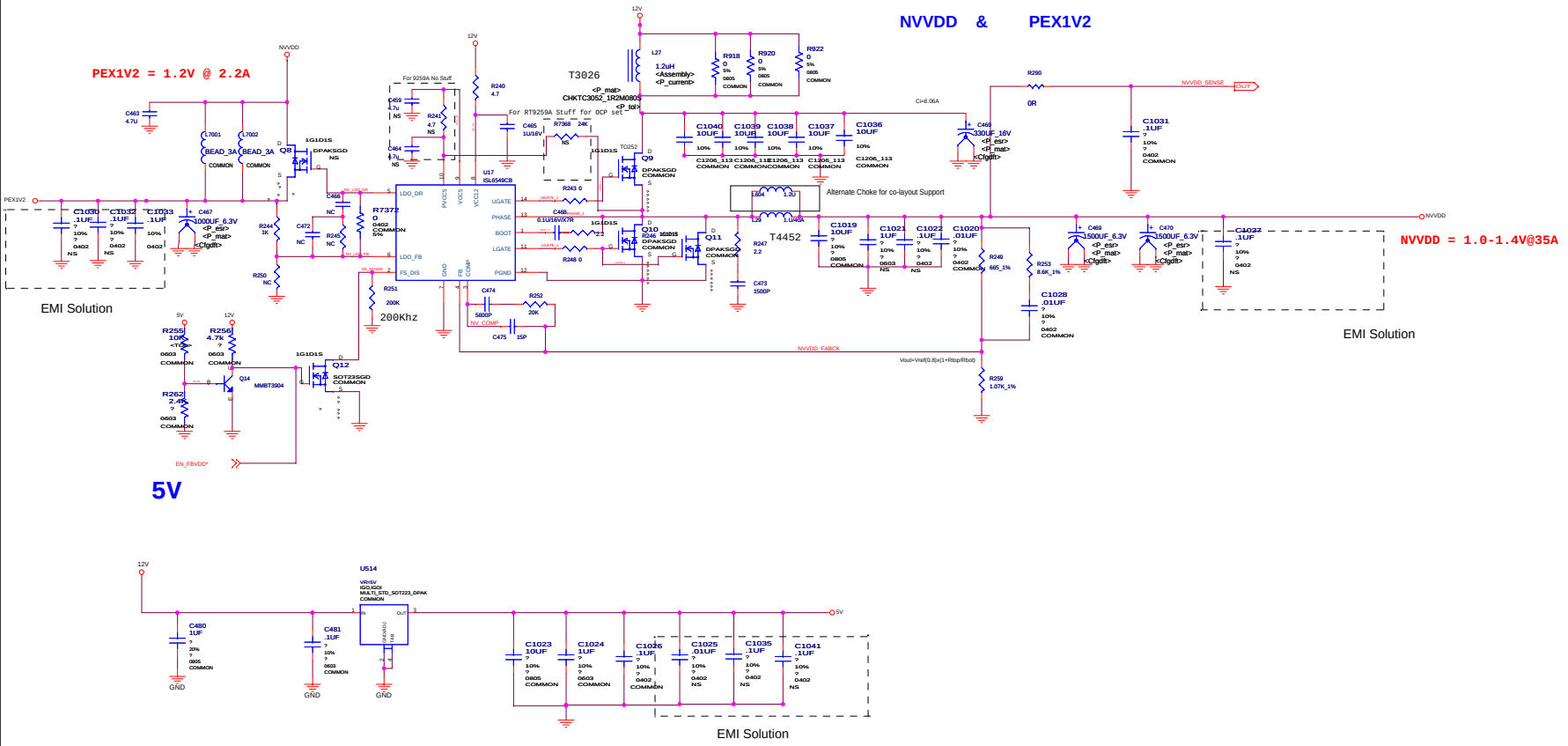
NVVDD ,FBVDD, 5V,A3V3 POWER SUPPLY

NVVDD ,FBVDD, 5V,A3V3 POWER SUPPLY



5V

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NVVDD,FBVDD/Q,5V,A3V3	
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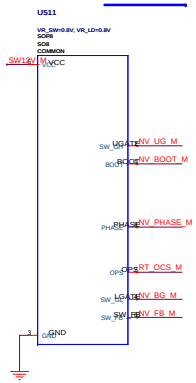
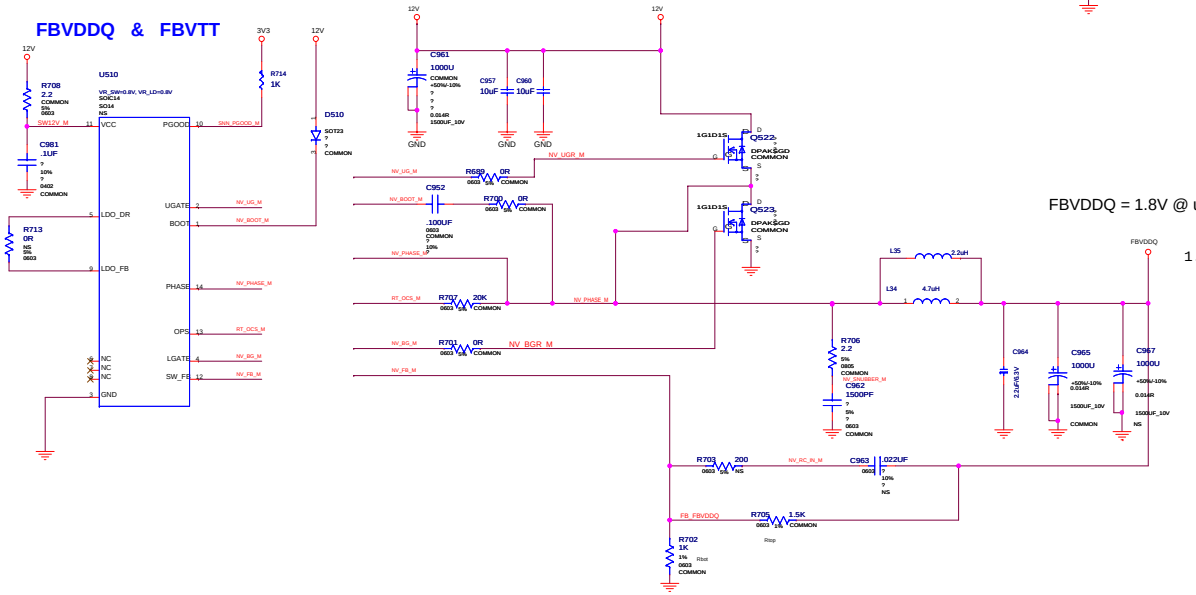
FBVDD



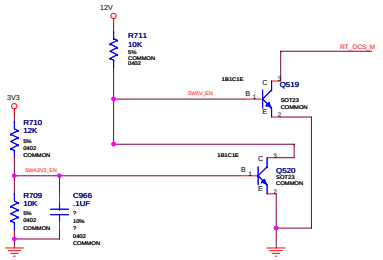
FBVDDQ & FBVTT



Power sequence

FBVDDQ = 1.8V @ upto 5A

1.8V/5.0A



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	FBVDDQ	
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