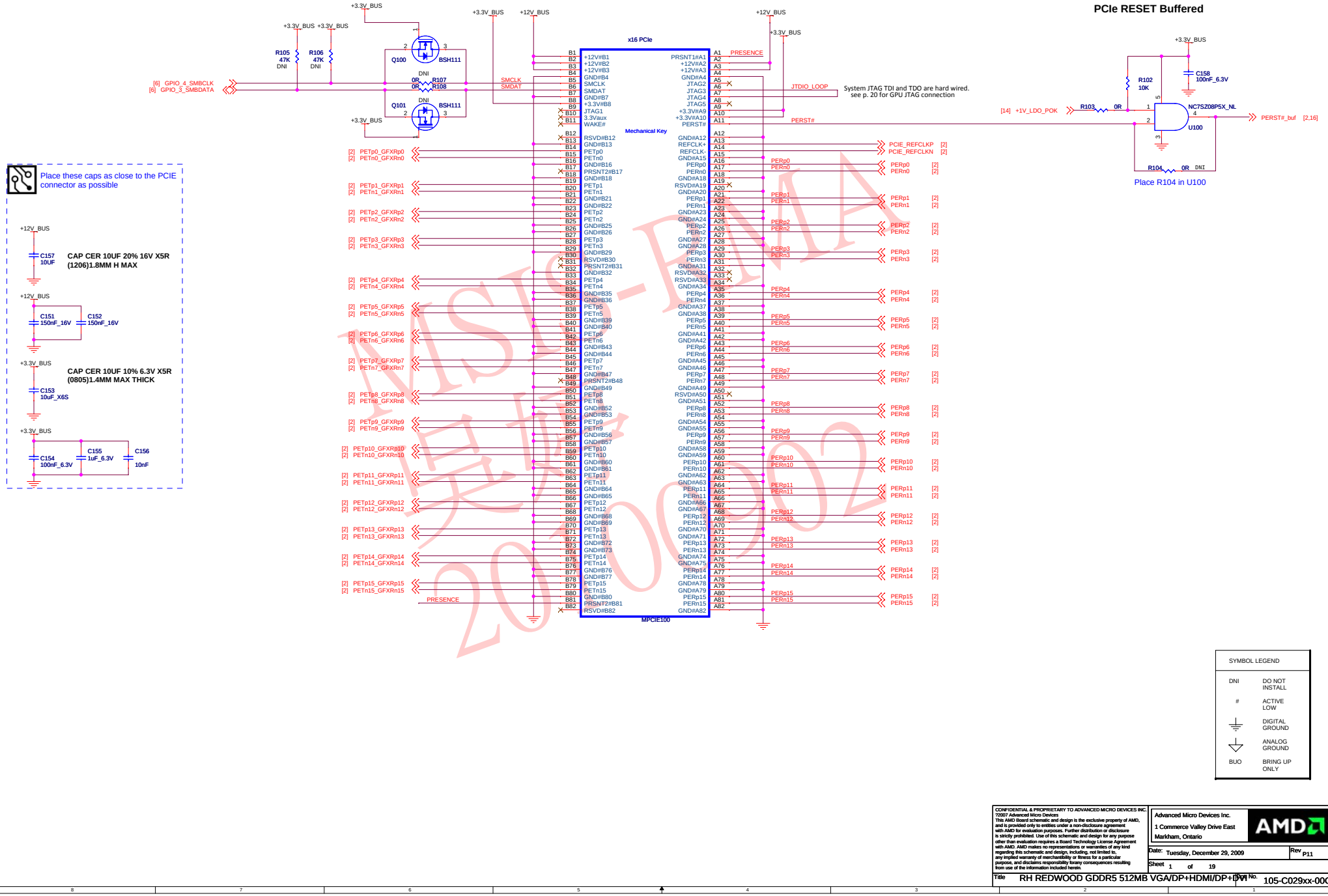
PCI-EXPRESS EDGE CONNECTOR

REDWOOD WOLVERINE



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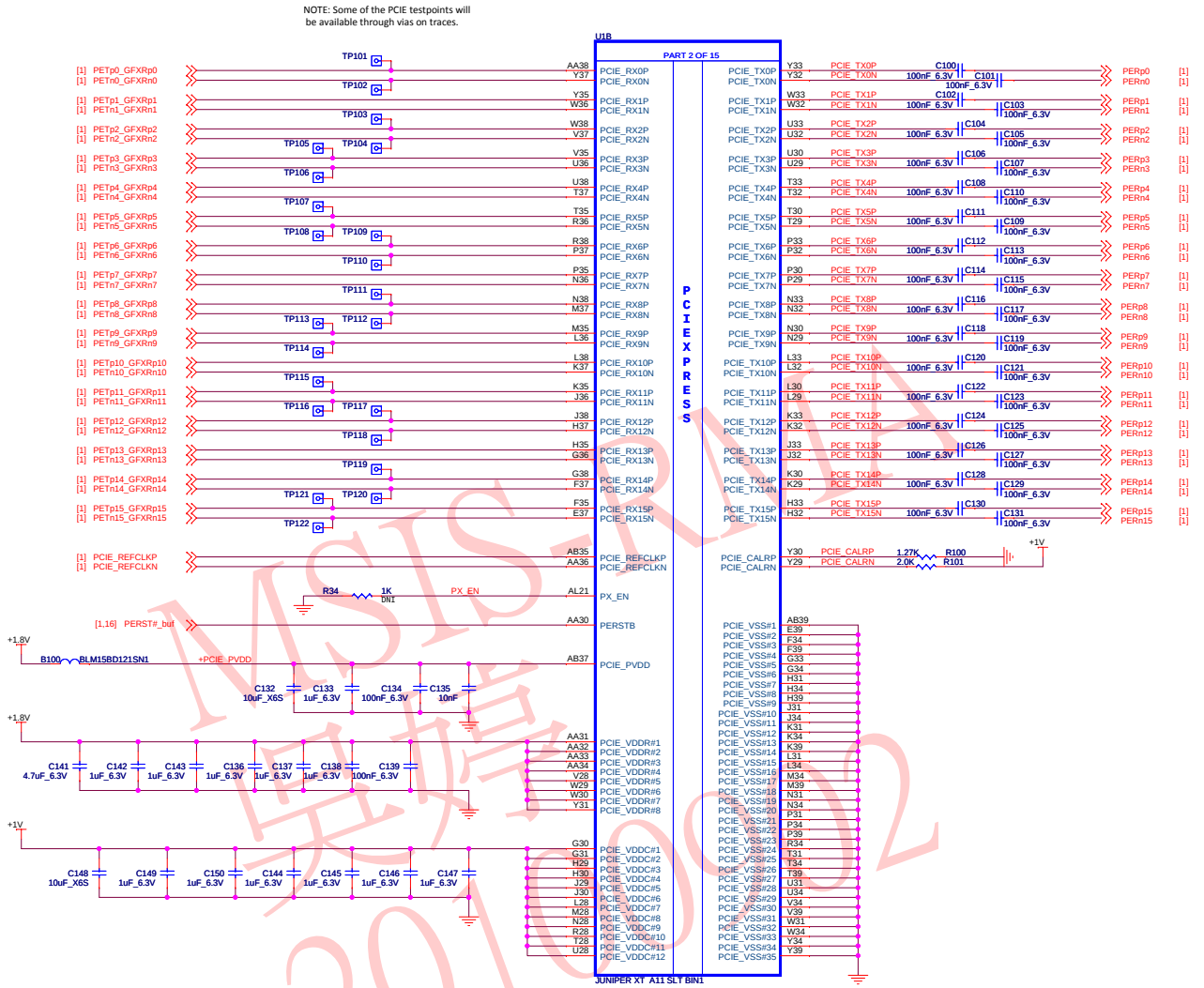
(2) REDWOOD PCIe Interface



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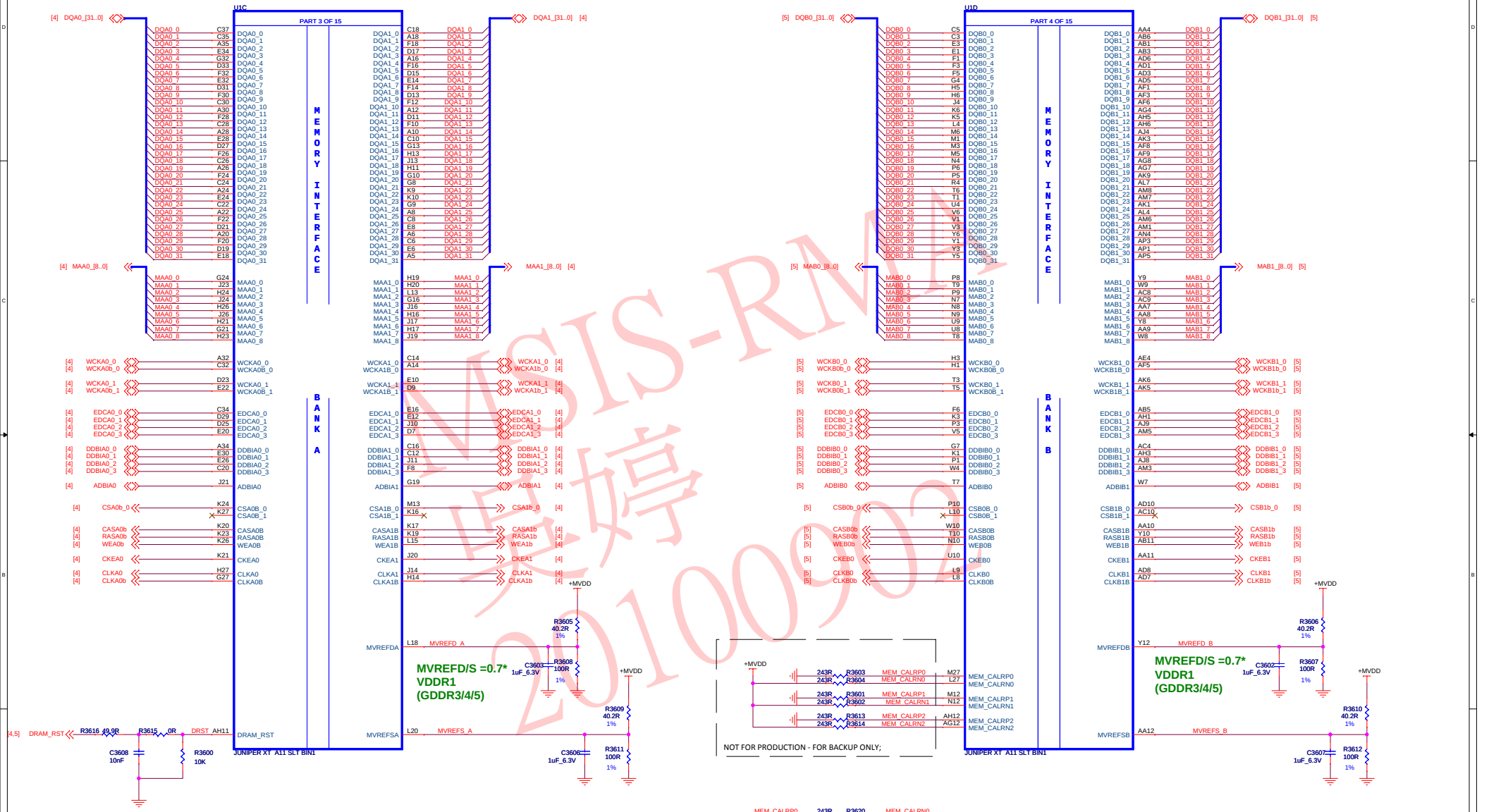
(3) REDWOOD MEM Interface Ch A&B



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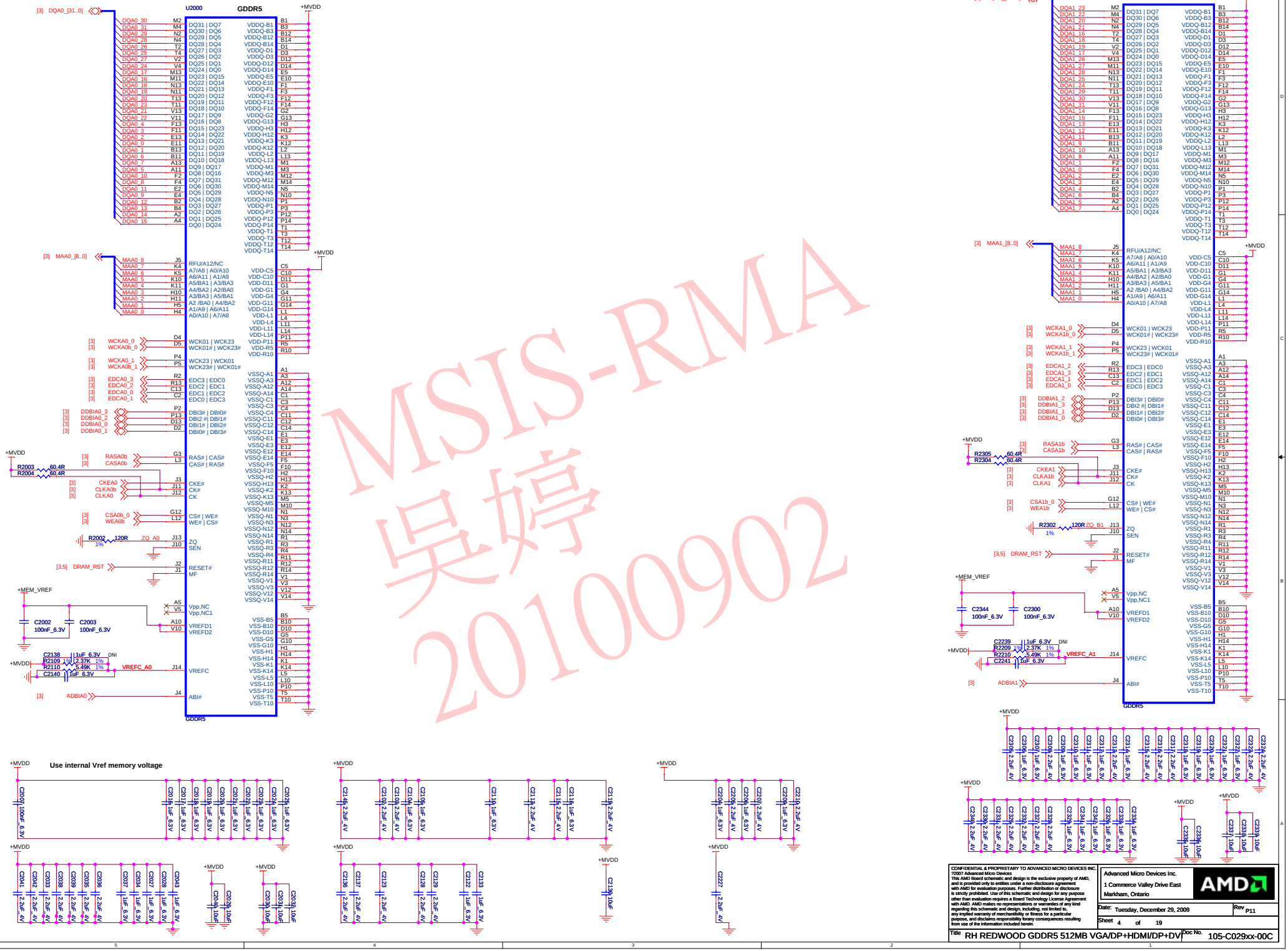
(4) GDDR5 x16 MEM Channel A

CH_A0 =U2000

CH_A1 = U2300



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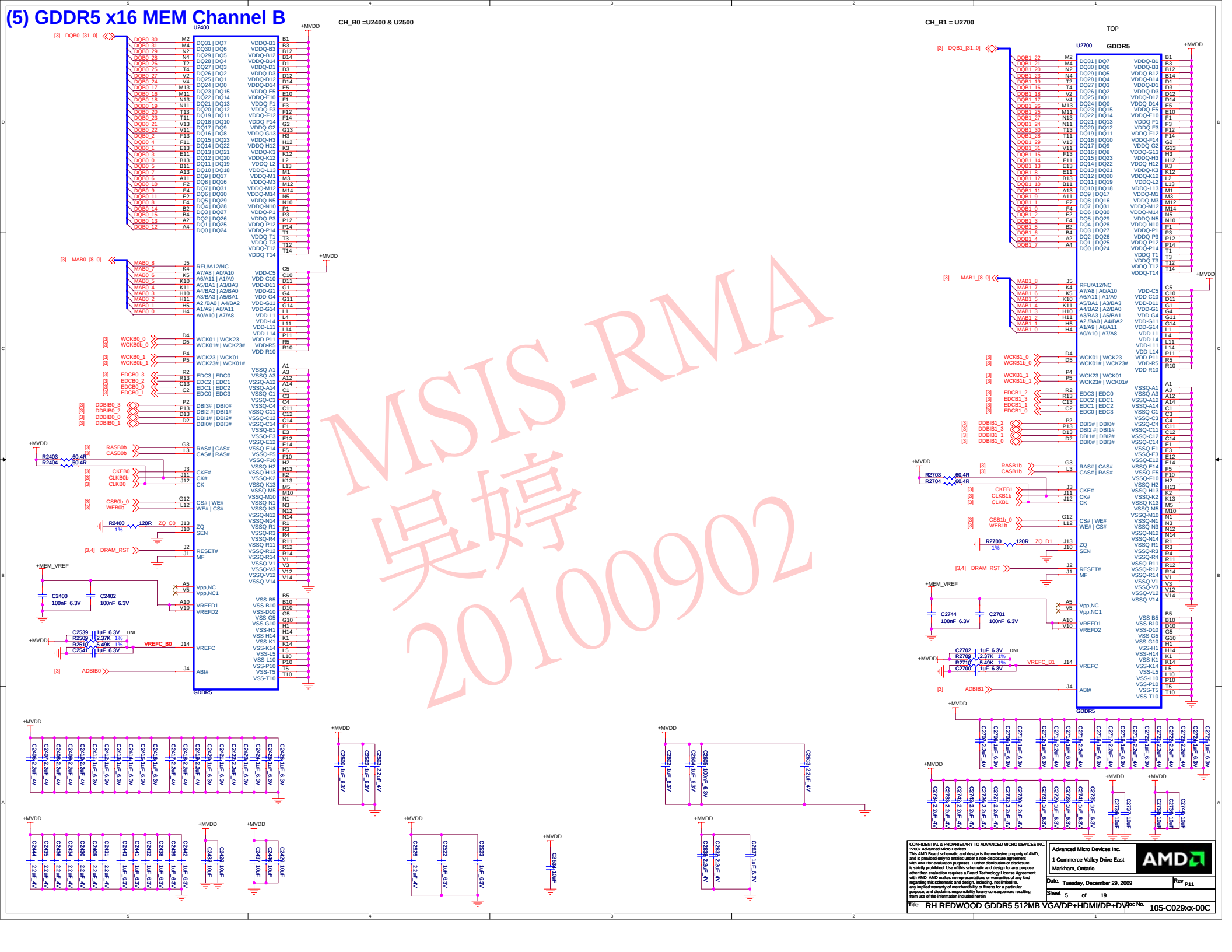
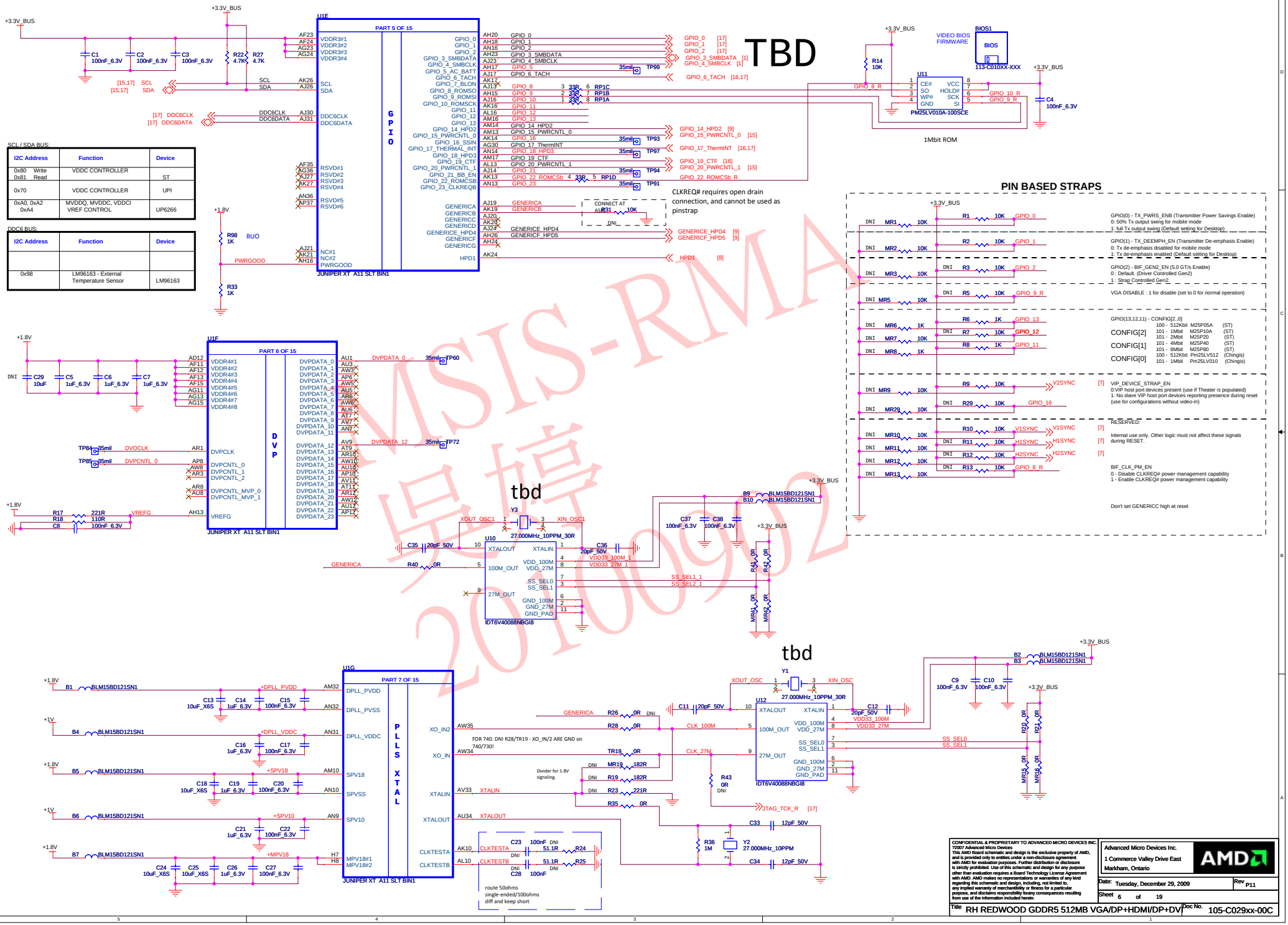
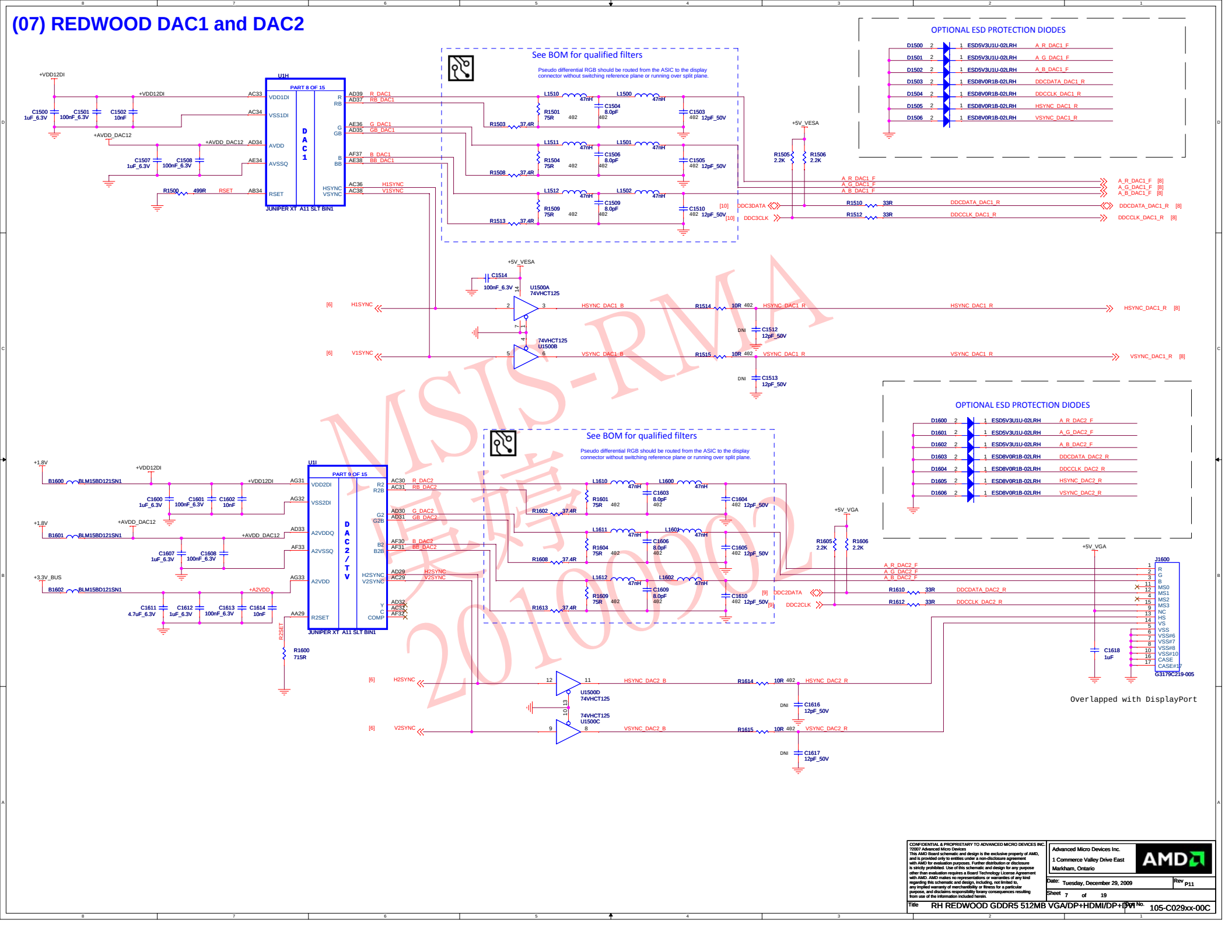
(5) GDDR5 x16 MEM Channel B



(06) REDWOOD GPIOs Strap CF XTAL OSC



(07) REDWOOD DAC1 and DAC2



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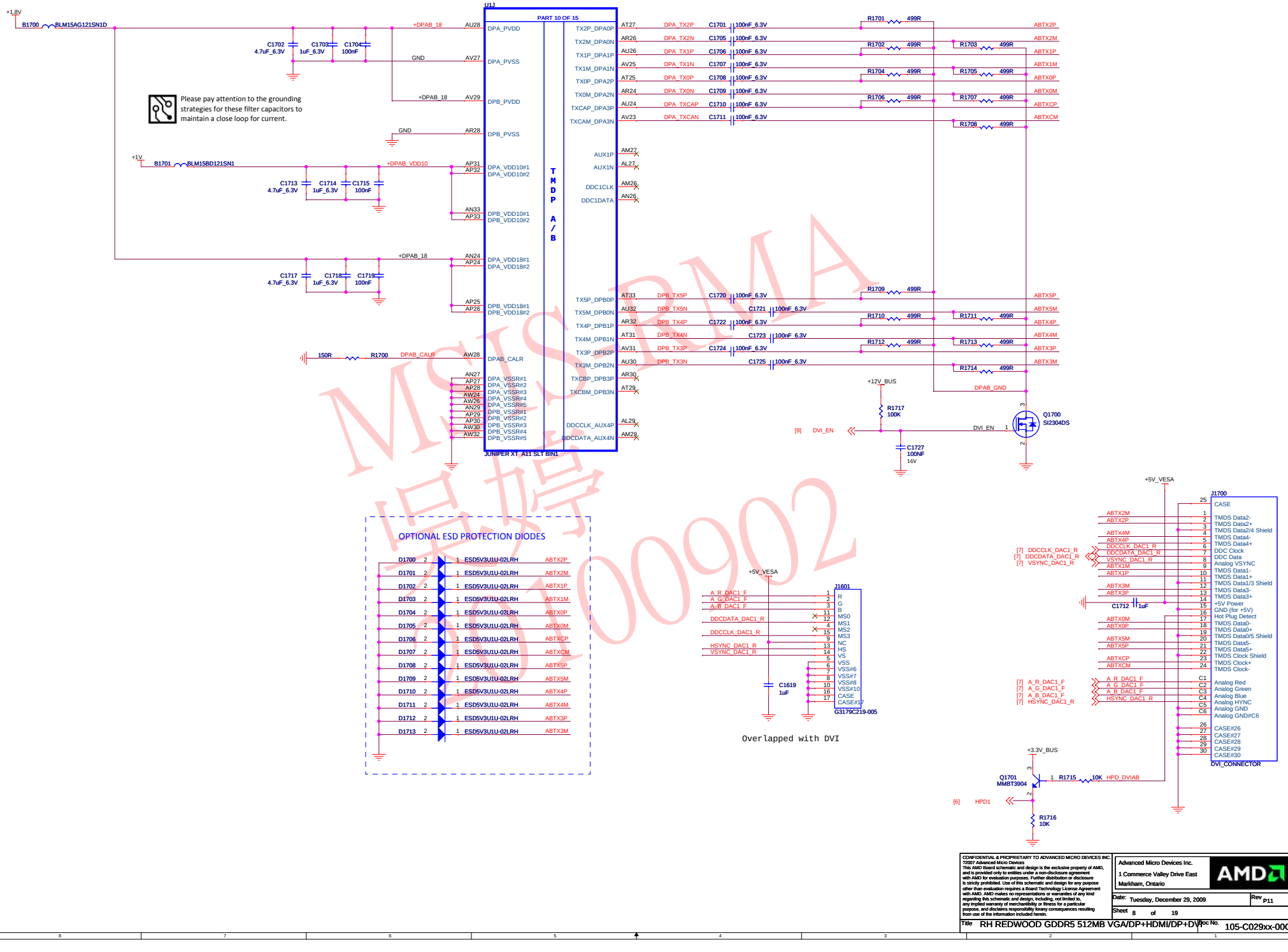
(08) REDWOOD TMDP A&B dDVI-I TOP



(09) REDWOOD Display Port C & Display Port/HDMI D

To DP/HDMI connector.

To VGA connector.

DDC2CLK DDC2CLK [7]

DDC2DATA DDC2DATA [7]

AUX/DDC:
FOR 740/730, INSTALL 0R ON ASIC-SIDE OF AC COUPLING CAPS ONLY;
FOR JUNIPER, INSTALL 0R ON CONNECTOR SIDE OF AC COUPLING CAPS ONLY;

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

U1K
PART 11 OF 15
TMDP C/D
JUNIPER XT A11 SLT BIN1

OPTIONAL ESD protection diodes

Share PADs

OVERLAP HDMI WITH DP D

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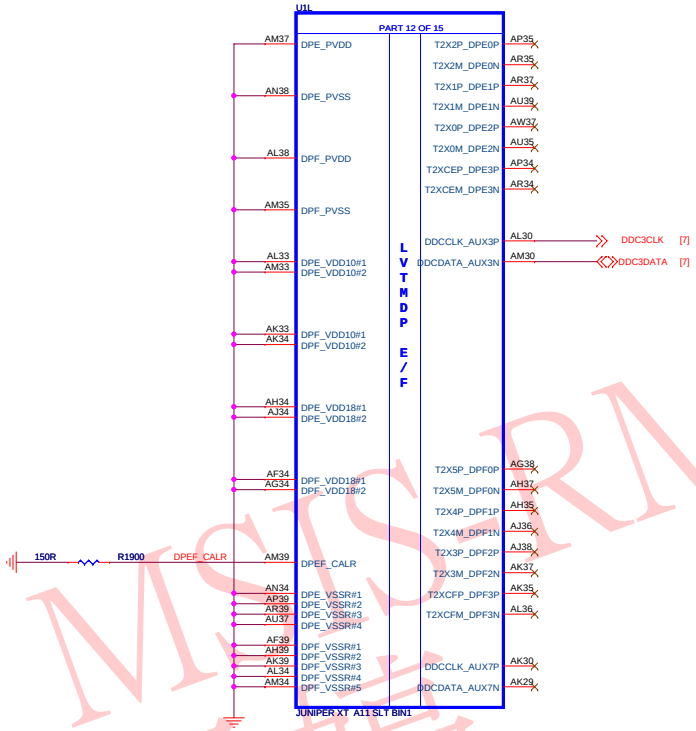
(10) REDWOOD LVTMDP E&F



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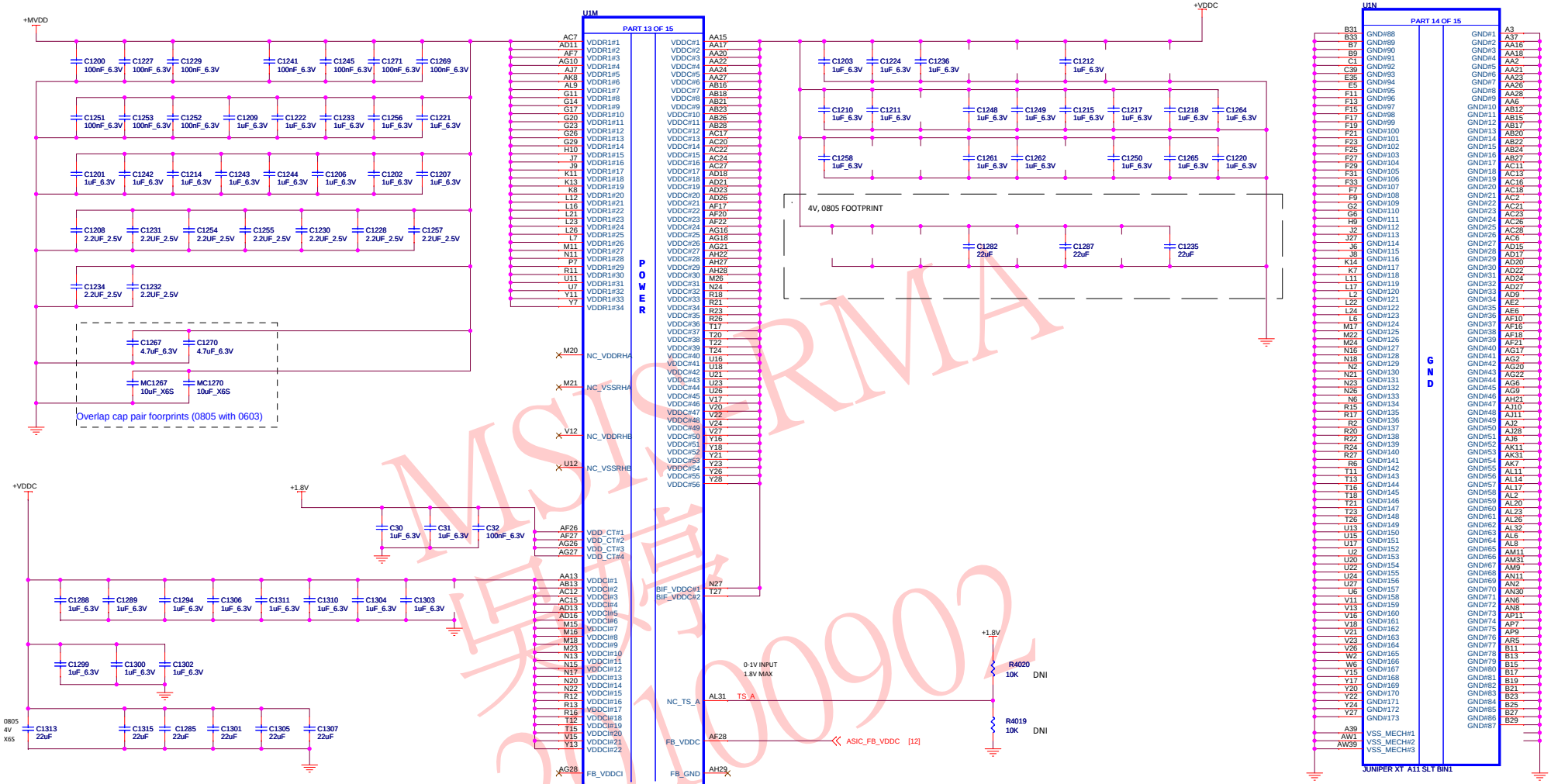
(11) REDWOOD Power & GND



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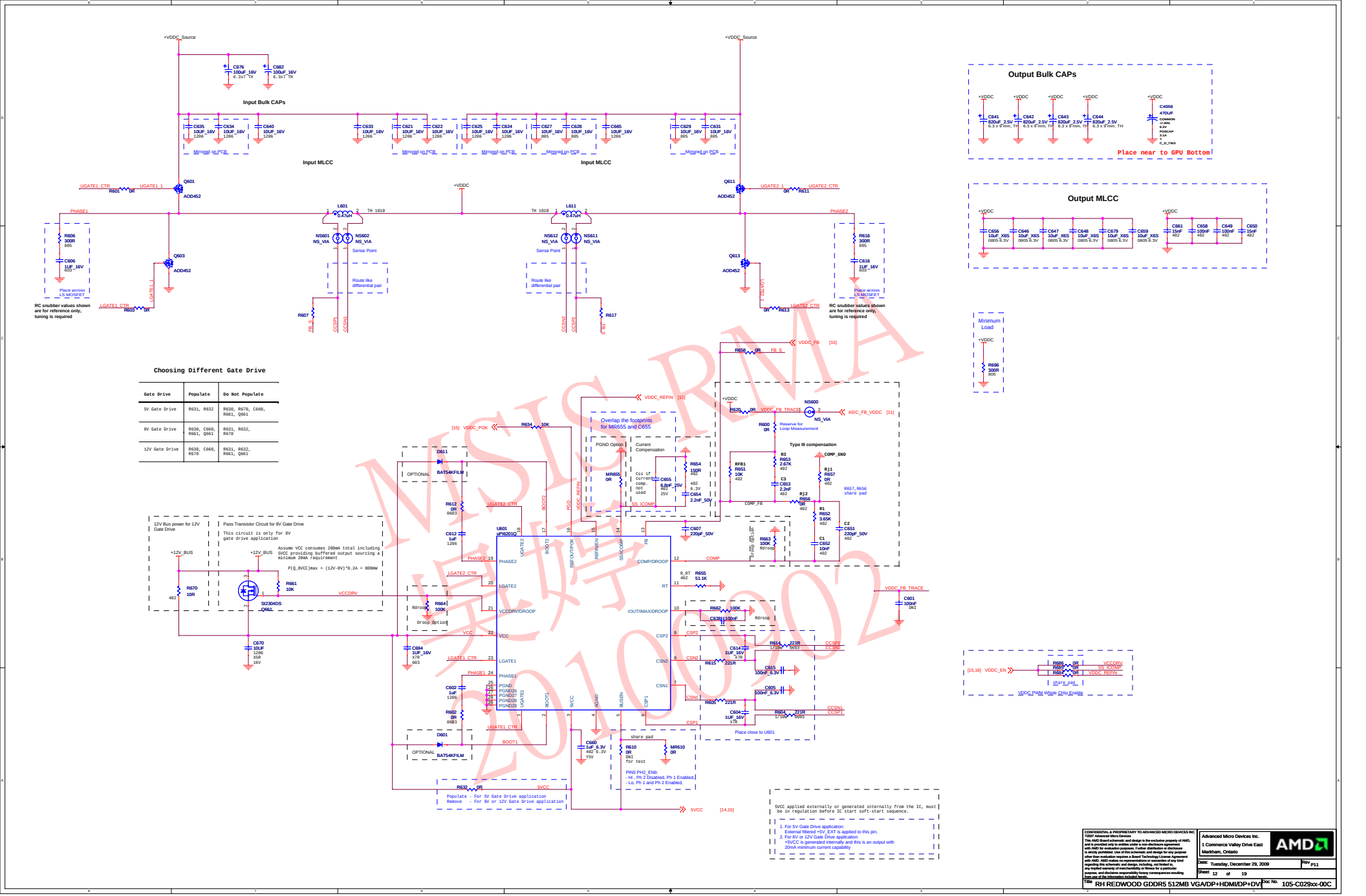

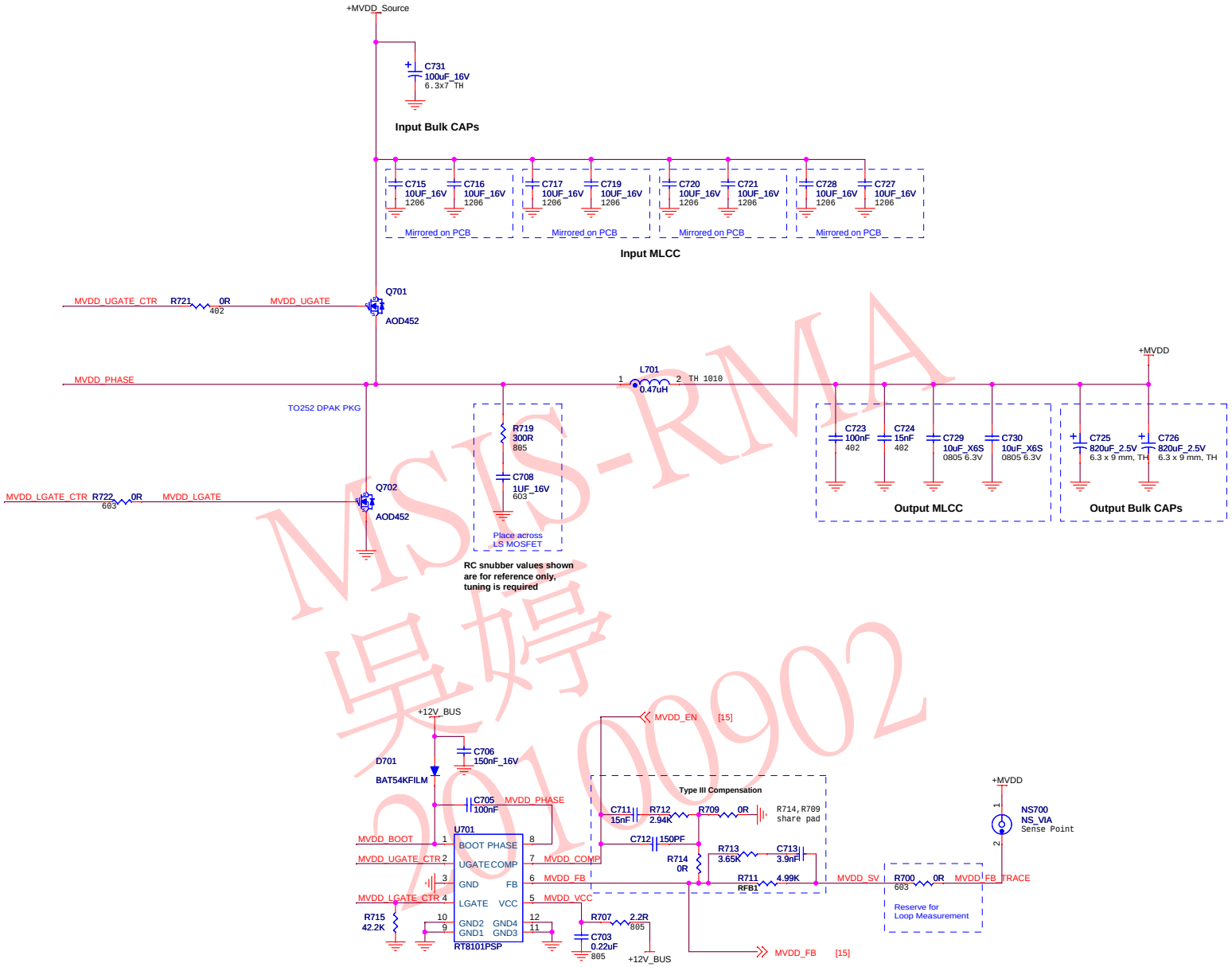

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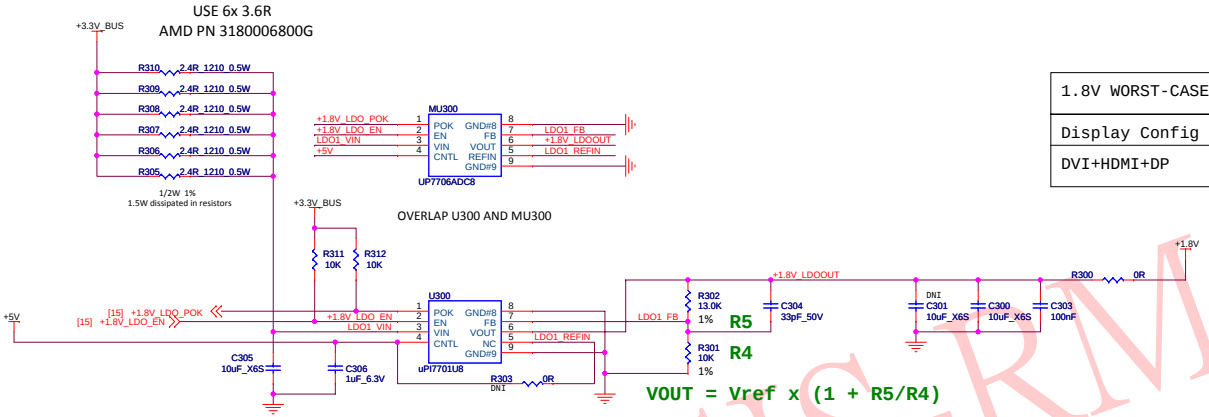
(15) Linear Regulators

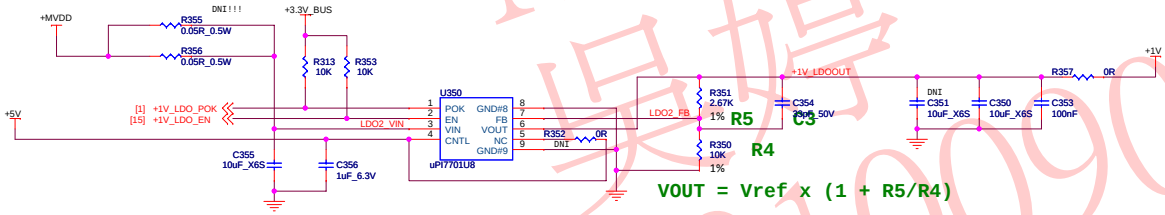
Regulators for +5V, +5V_VESA and +5V_HDMI

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



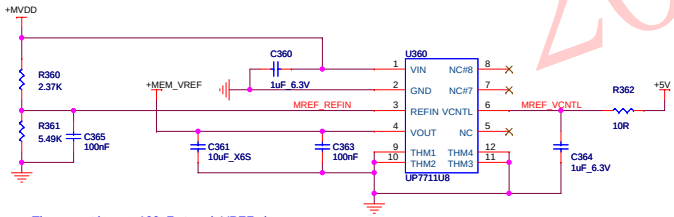
1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

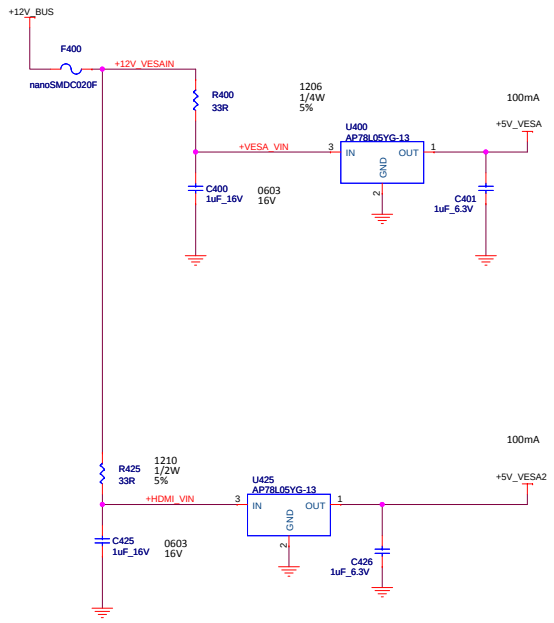


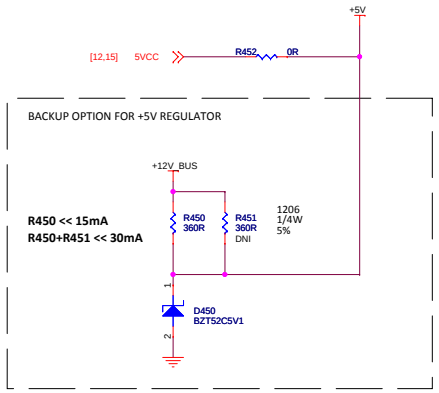
1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA

Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ



There must be one 100nF at each VREF pin
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices





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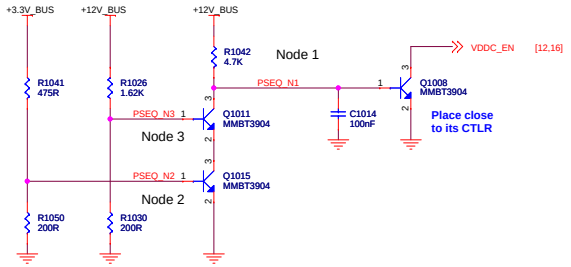
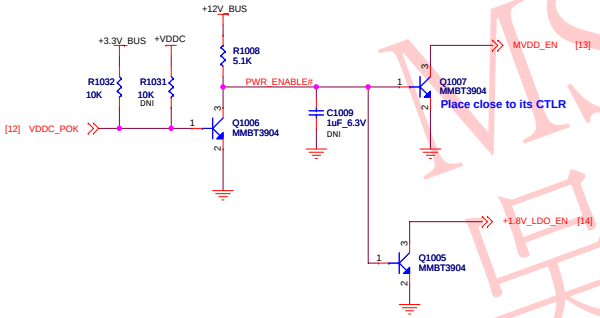
(16) Power Management - Power Gating and Dynamic Voltage Control

12V_BUS & 3V3_BUS POWER SEQUENCING

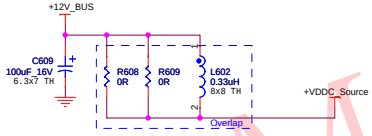


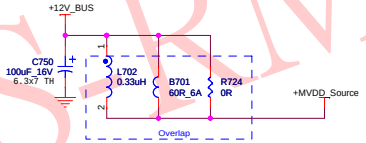
POWER SEQUENCING CIRCUIT



Install R1010 to gate 1V LDO with 1.8V LDO.

[14] +1.8V_LDO_POK — R1010 0R — +1V_LDO_EN [14]

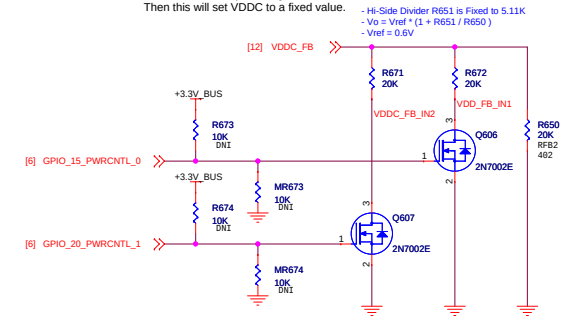




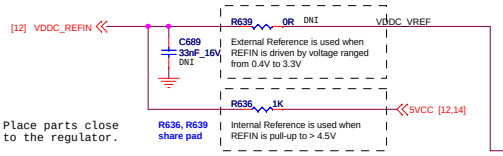
MVDD Low Side Divider

VDDC Low Side Divider

R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.



VDDC Reference Voltage Selection

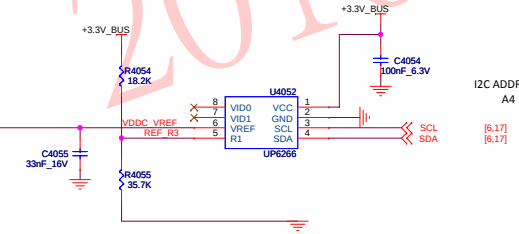


Place parts close to the regulator.

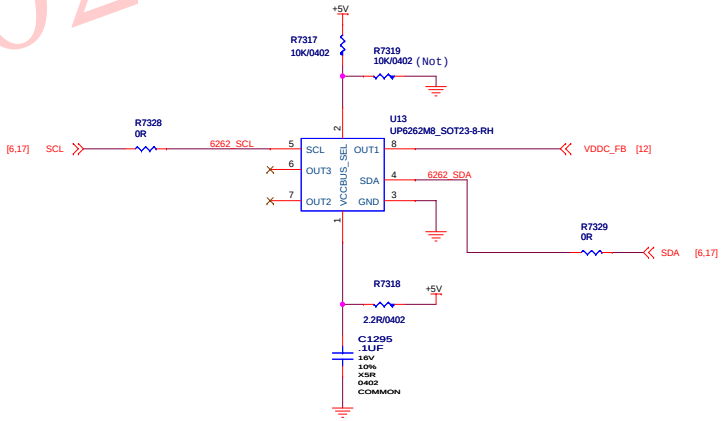
VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

I2C VOLTAGE REFERENCE FOR VDDC (not for production)



I2C ADDRESS: A4



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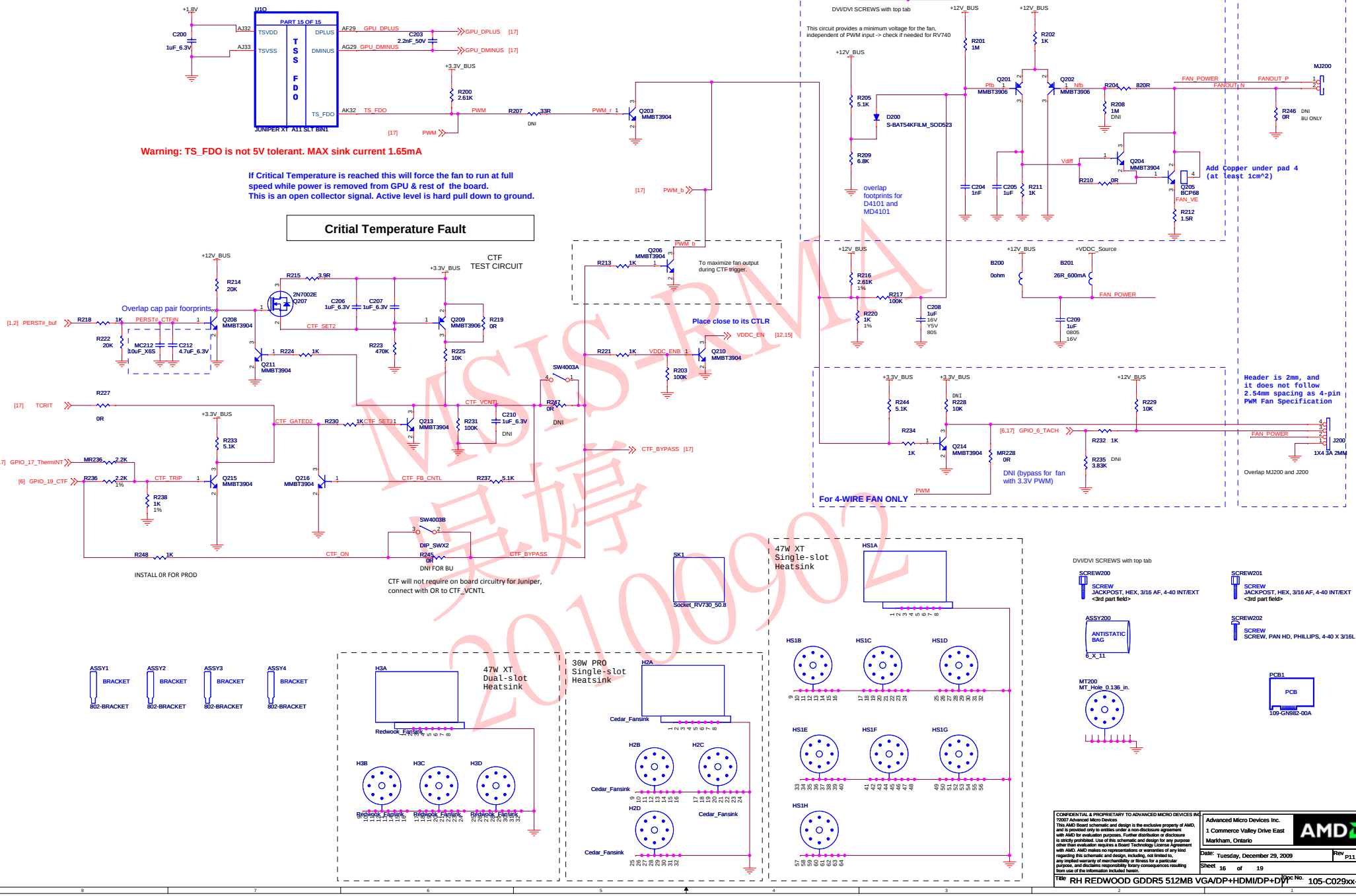
(19) Mechanical and Thermal Management



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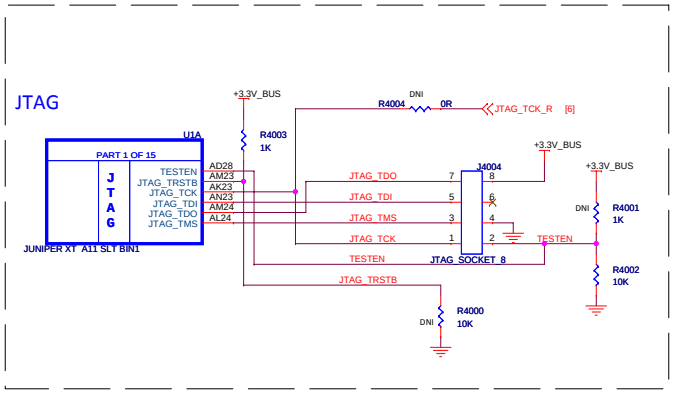
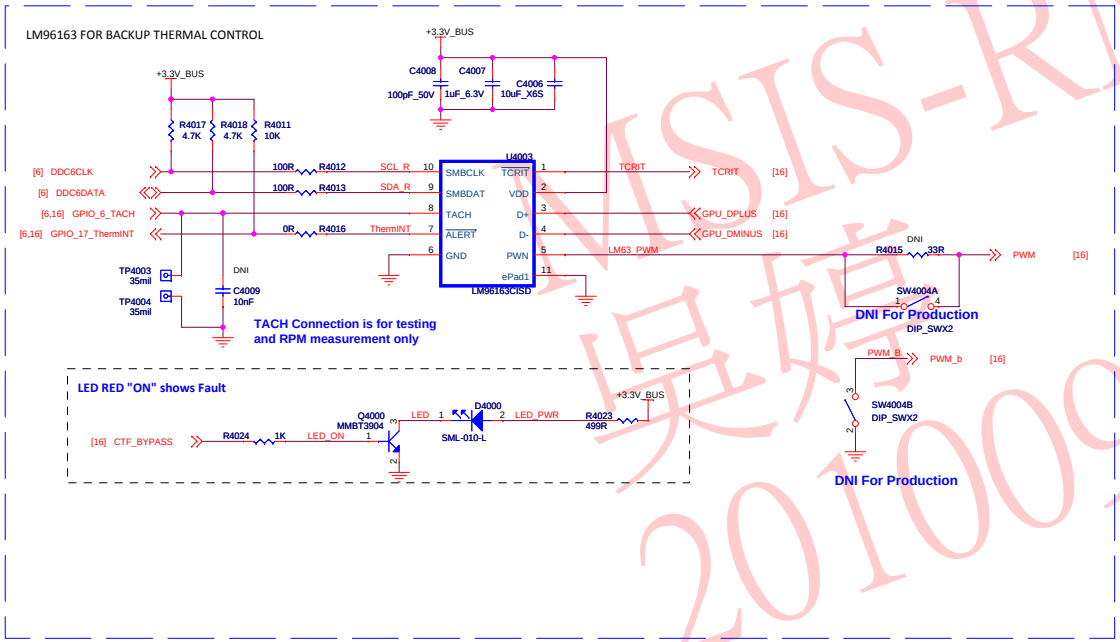
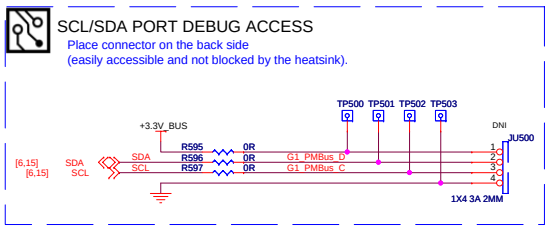
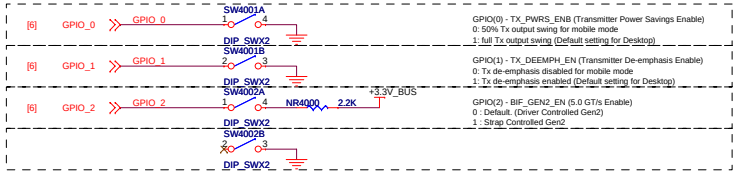
(19) Debug Circuits

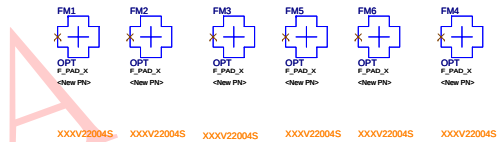


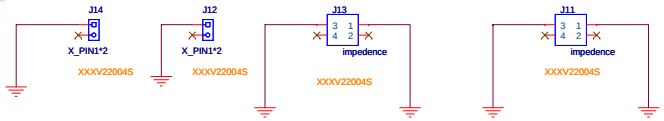




SWITCH CONNECTIONS TO PINSTRAPS







J11 6 層 80OHM (0.14mm/0.17mm =>5.5 mils/6.7 mils) MEM_CLK
J13 3 層 80OHM (0.175mm/0.28mm=>6.889 mils/11.0236 mils) MEM_CLK
J12 1.6層 45OHM (0.13mm => 5.1181 mils) MEM
J14 3 層 45OHM (0.175mm =>6.9mils) MEM

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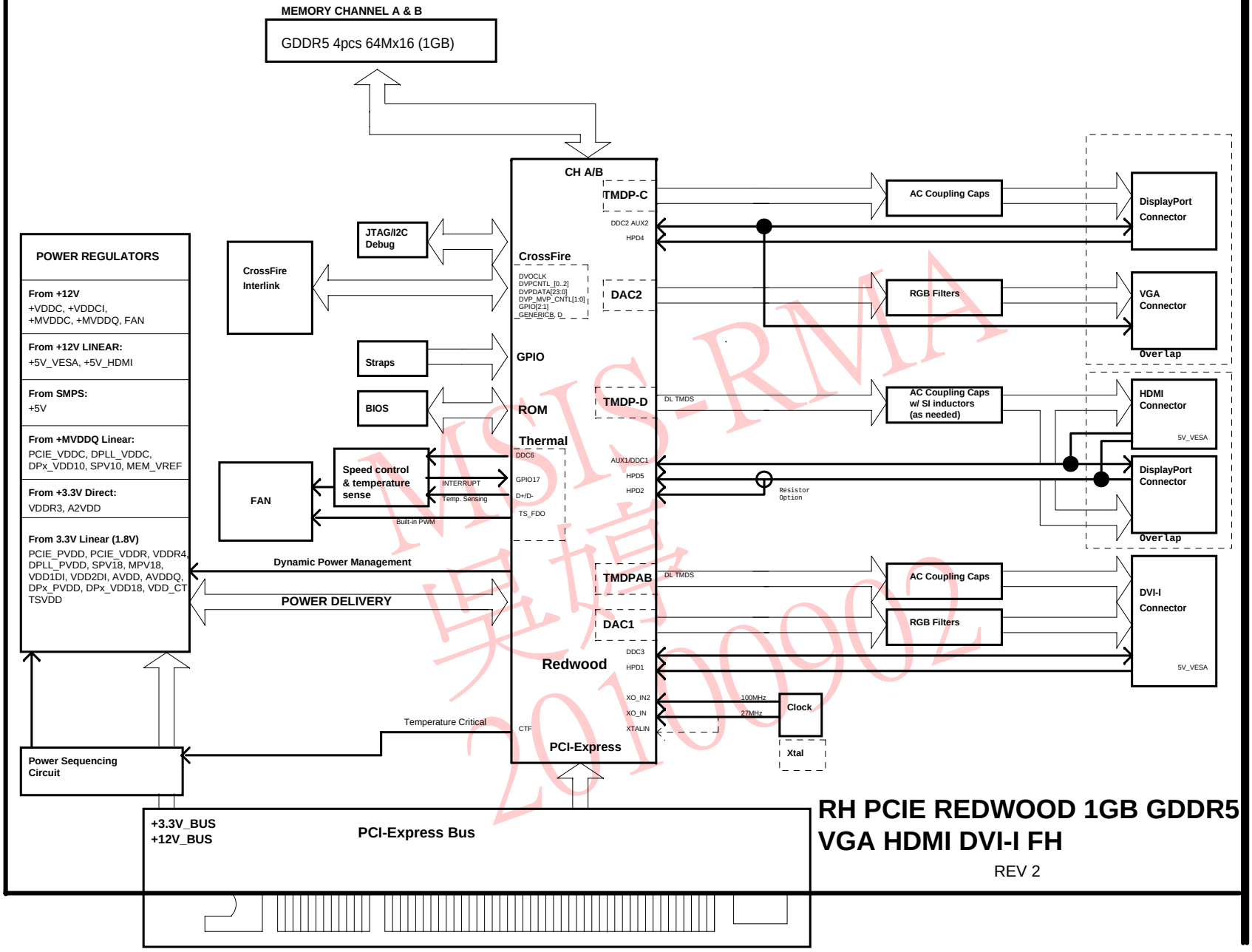

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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

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Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/05/08	REDWOOD XT GDDR5 512MB - BASED ON C020 ;
	00B	2009/10/12	1) SWAP DDC LINE TO FIX HDMI CERTIFICATE ISSUE 2) ADD ONE MORE SERIES RESISTOR ON DRAM_RST NET BASED ON SI TEAM SIMULATION RESULT 3) ADD 27MHz CLOCK TO JTAG CLK
	00C	2009/12/02	1) ADD 1.8V I/O SHUT DOWN CIRCUIT
	V220-4.0	2009/12/25	1)Modify Choke to SSC 2)Add POSCAP 1)Add uPI / uP6262