電子類元件 零件承認書文件 CHECK LIST

零件廠商：**UPI**　　品名規格：SMD WQFN3X3-8L

技嘉料號：10TA1-601909-20R

項次	文件項目
Data Sheet 檢核項目	
1	DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2**
8	零件樣品 20PCS(Chipset 等高單價，至少 1PCS)
9	**電子零件承認基本調查表。註 3**
10	以上資料電子檔為 PDF 檔，且是同 1 個 File
GSCM 綠色產品管理系統-物料管制文件檢核清單	
物料管制文件 1	GSCM 綠色產品管理系統：零件照片
物料管制文件 2	GSCM 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4**
物料管制文件 3	GSCM 綠色產品管理系統：Data Sheet
GSCM 綠色產品管理系統-MCD 表格	
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
其他文件 (僅適用電阻、電容類之系列元件)	
附件 1	危害物質測試報告 Test Report of Hazardous Substances。**註 5**
附件 2	元件調查表 Component Composition Table

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等

※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)

2.1. 基本需符合 JEDEC 規範

2.2. Ambient Temp. (Reflow Temp endurace): >225℃, 70 sec. 零件塑膠材質需 PA9T(含)等級以上

2.3. PASTE IN HOLE 零件塑膠材質需 PA9T(含)等級以上

※ **3. 電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G*,11T***

非 IC 類：10C*,11C*,10L*,11L*,10X*,11X*,10R*,11B*

※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”

※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

電子零件承認基本調查表

一、原物料規格/來源

項次	部位名稱/規格	材質	原物料來源產地
1	CHIP	金屬	MAXCHIP
2	DIE ATTACH	EPOXY	SUMITOMO
3	LEAD FRAME	金屬	SHINKO
4	BONDING WIRE	金屬	MK
5	MOLDING COMPOUND	EPOXY	SUMITOMO
6	PLATING	鍍錫	JAU JANQ

二、晶圓廠(非 IC 類免填)

項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	(MAX)鉅晶電子	TW	8	100	N/A
2					
3					

三、封裝廠(IC 類)；成品之生產製造工廠(非 IC 類)

項次	工廠名稱	生產產地	投產比率(%)	自有/外包
1	GTK(超豐電子)	TW	50	NA
2	JCET(長電)	TW	40	NA
3	嘉盛(蘇州)	CN	10	NA

四、產能

總產能(月/PCS)	可供技嘉產能(月/PCS)
NA	NA

※ 1. IC 類之晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 2. 非 IC 類零件之成品生產製造工廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 3. 以上資訊欄位若有不足，可自行增加行數

5V MOSFET Driver for High Voltage Synchronous Rectified Buck Converter

General Description

The uP1909R is a high efficiency 5V MOSFET driver specifically designed to drive N-channel power MOSFET pair in a synchronous rectified buck converter for mobile computing application. This part has integrated bootstrap FET to eliminate external bootstrap diode. The resistor commonly placed between MOSFET gate and source for discharge is also integrated, making external component minimal. The uP1909R supports enable/disable function that reduces the power consumption to prolong battery life. This device also supports three PWM input states that along with PWM controller to provide a complete power solution. The uP1909R implements shoot-through protection that monitors converter switching node voltage to prevent high side and low side MOSFETs from cross-conduction. This part is available in WDFN3x3 - 8L package.

Features

- **Dual MOSFET Drivers for Synchronous Buck Converter**
- **Single 5V Driving Voltage Output**
- **Integrated Bootstrap FET**
- **Integrated Gate-to-Source Discharge Resistor**
- **Enable/Disable Control**
- **Low Consumption Current in Disable Mode**
- **Three PWM Input States: High, Low and Tri-State**
- **MOSFET Shoot-Through Protection**
- **Supply Voltage Power on Reset Function**
- **RoHS Compliant and Halogen Free**

Ordering Information

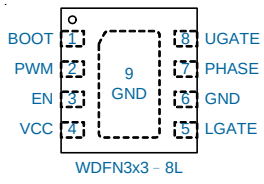
Order Number	Package	Remark
uP1909RDD8	WDFN3x3 - 8L	

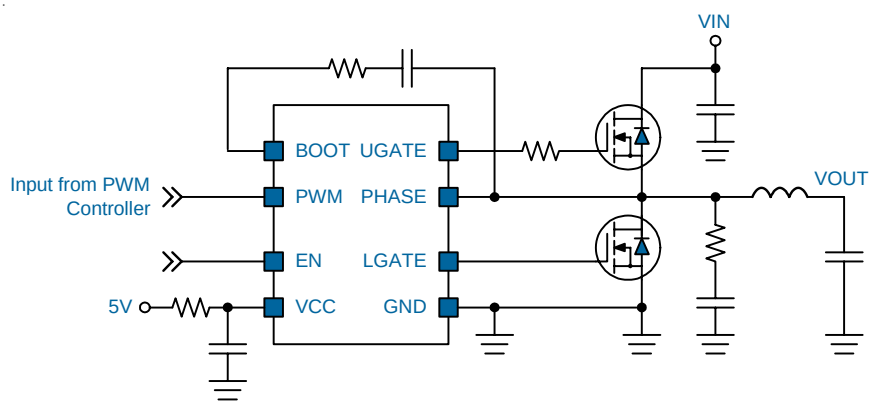
Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Applications

- **Laptop Computer CPU Voltage Regulator**
- **High Frequency Low Profile DC/DC Buck Converters**
- **High Input Voltage DC/DC Buck Converters**

Pin Configuration & Typical Application Circuit

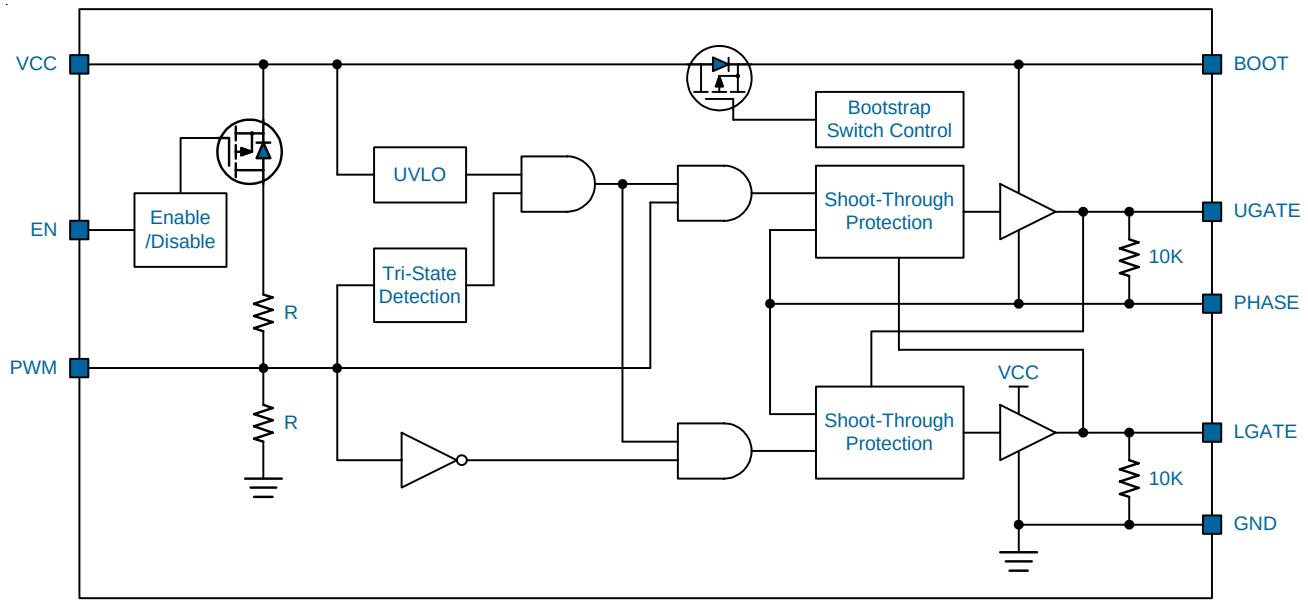




Functional Pin Description

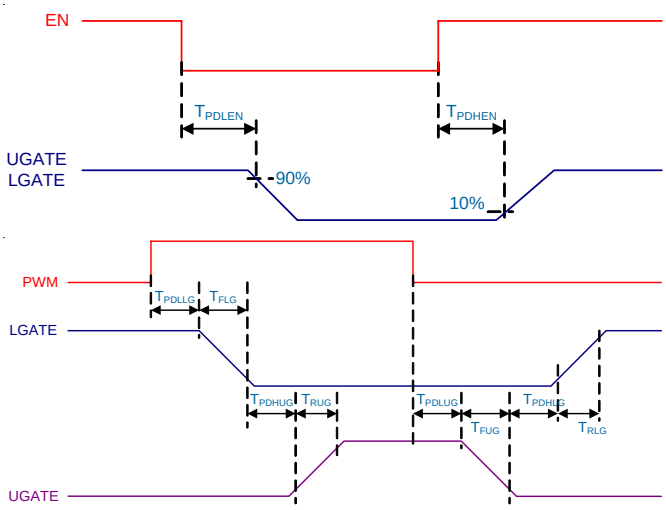
Pin Name	Pin Function
BOOT	**Bootstrap Supply.** Connect the bootstrap capacitor C_{BOOT} between BOOT pin and PHASE pin for floating drive. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Use MLCC as C_{BOOT}, and make sure C_{BOOT} is placed near the IC.
PHASE	**Switching Node.** Connect this pin to the joint of upper MOSFET source, inductor and lower MOSFET drain. This pin is used as the return ground for upper MOSFET floating drive. Voltage on this pin is monitored by the shoot-through protection circuitry to determine when to turn on/off the upper MOSFET.
UGATE	**Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on/off upper MOSFET. There is a typical 10kΩ resistor internally connected between UGATE and PHASE for discharge.
LGATE	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on/off the lower MOSFET. There is a typical 10kΩ resistor internally connected between LGATE and GND for discharge.
PWM	**PWM Input.** This pin receives logic level input and controls the driver outputs.
EN	**Enable/Disable Control.** Input logic high to this pin enables the chip. Pull low this pin to disable the whole chip. If this pin is left open, it is internally pulled low.
VCC	**Supply Voltage Input.** This pin is the voltage supply for the IC. Connect this pin to 5V voltage source with at least 1uF MLCC bypass capacitor.
GND	**Ground.** This pin is the ground for lower MOSFET gate driver and for the whole chip. All voltages levels are measured with respect to this pin.
Exposed Pad	**Ground.** The ground for lower MOSFET gate driver and for whole chip. The exposed pad dominates heat conduction path and should be well soldered to PCB for optimal thermal performance.

Functional Block Diagram



Functional Description

Switching Timing Diagram



Supply Voltage

The uP1909R works with a single 5V supply input voltage. VCC is the power for MOSFET driving circuit and logic circuit. Having a good power quality for VCC is important. Connect VCC to a 5V voltage source, and bypass this pin to GND with at least 1uF MLCC.

Enable/Disable Control

The uP1909R provides enable/disable function. The EN pin controls the working state of the whole chip. Logic high input to the EN pin enables this IC, and it drives MOSFET on or off according to PWM input signal. When the input to EN pin is logic low, the uP1909R shuts down with minimal consumption current. The EN pin is internally pulled low to GND to ensure the IC stays in shutdown state when the EN pin is left floating. In most applications, the EN pin is typically connected to the VCC pin such that the driver works immediately as VCC is powered on.

PWM Input States

The PWM pin has three input states, and the uP1909R drives MOSFET according to these input states. Table 1 shows the PWM input states and the MOSFET working states. Logic high input to this pin turns on upper MOSFET and turns off lower MOSFET. In reverse, upper MOSFET is turned off and lower MOSFET is turned on when the PWM pin input is of logic low. In both cases, the upper and lower MOSFET switches in a complementary way. The PWM input has third state, which is tri-state or high impedance (high-Z). This means the PWM input from voltage regulator (VR) controller is neither high nor low, but in open circuit condition. When PWM input is in tri-state, both upper and lower MOSFETs are turned off. Since the PWM input from VR controller is in open circuit condition, the PWM pin voltage is determined by the uP1909R. In this tri-state, the PWM pin voltage will be half of VCC voltage. The PWM tri-state input is for converter shutdown and phase shedding function of multi-phase VR controller.

Table 1. PWM Input State

PWM Input	UGATE	LGATE
High	ON	OFF
Tri-State	OFF	OFF
Low	OFF	ON

Shoot-Through Protection

A rising edge of low to high logic input to the PWM pin initiates turn-off of lower MOSFET and then turn-on of upper MOSFET. The lower gate begins to fall after a short propagation delay T_{PDLLG}. The uP1909R has shoot-through protection circuit that monitors LGATE and PHASE voltage. When LGATE has fallen below 1V and then after a specific delay (dead time), UGATE is allowed to turn on. This prevents both lower and upper MOSFETs from conducting simultaneously, also known as shoot-through. There is a dead time between the turn-off of LGATE and the turn-on of UGATE. A falling edge of high to low logic input to the PWM pin initiates turn-off of upper MOSFET and then turn-on of lower MOSFET. The upper gate begins to fall after a short propagation delay T_{PDLUG}. The shoot-through protection circuit monitors UGATE and PHASE voltage. When UGATE - PHASE voltage difference has fallen below 1V and PHASE has dropped below 1V, LGATE is allowed to turn on. This prevents both lower and upper MOSFETs from shoot-through. There is a dead time between the turn-off of UGATE and the turn-on of LGATE.

Upper MOSFET Gate Driver

The upper gate driver is designed to drive a floating N-Channel MOSFET. VCC is the supply voltage of the upper driver, and it is internally connected to the BOOT pin via a bootstrap FET. An external bootstrap capacitor C_{BOOT} connected between BOOT and PHASE pins provides the charge for the upper MOSFET gate driver. The C_{BOOT} is charged to near VCC when PHASE pin is grounded by turning on the lower MOSFET. The PHASE voltage rises to VIN when the upper MOSFET is turned on, forcing the BOOT pin voltage near to VIN + VCC that provides voltage to keep the upper MOSFET on. The upper gate driver output is in phase with the PWM input when it is enabled. The upper gate driver is held low if the PWM pin input is in tri-state.

Lower MOSFET Gate Driver

The lower MOSFET gate driver is designed to drive a ground-referenced N-Channel MOSFET. VCC directly supplies power to the lower MOSFET gate driver. The uP1909R is optimized for converters with large step-down ratio where the lower MOSFET conducts for a relatively longer time than that of the upper MOSFET in a switching cycle. Power MOSFET with low on-resistance usually has large gate capacitance. To provide sufficient driving capability, the lower gate driver is therefore sized much larger to meet this application requirement. Parasitic components of a power MOSFET may cause gate voltage of lower MOSFET rising above its threshold level when upper MOSFET is turning on. This is likely to turn on upper and lower MOSFET simultaneously. The lower gate driver has low on-resistance that holds the LGATE tightly to ground and eliminate the risk of shoot-through.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC ---------- -0.3V to +6V
BOOT to PHASE ---------- -0.3V to +6V
PHASE to GND
- DC ---------- -0.7V to 30V
- <100ns ---------- -8V to 36V

BOOT to GND
- DC ---------- -0.3V to 36V
- <100ns ---------- -0.3V to 42V

UGATE to PHASE
- DC ---------- -0.3V to (BOOT-PHASE+0.3V)
- <100ns ---------- -5V to (BOOT-PHASE+0.3V)

LGATE to GND
- DC ---------- -0.3V to (VCC+0.3V)
- <100ns ---------- -5V to (VCC+0.3V)

Other Pin ---------- 0.3V to (VCC+0.3V)
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- WDFN3x3 - 8L θ_{JA} ---------- 68°C/W
- WDFN3x3 - 8L θ_{JC} ---------- 6°C/W

Power Dissipation, P_D @ T_A = 25°C
- WDFN3x3 - 8L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- +4.5V to 5.5V
Power Stage Input Voltage, V_{IN} ---------- +4.5V to 28V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(VCC = 5V, V_{IN} = 12V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Voltage						
Supply Current	I_{VCC}	PWM input = floating	--	80	120	uA
VCC POR Rising Threshold	V_{CCRTH}	V_{CC} rising	--	3.4	3.9	V
VCC POR Hysteresis	V_{CCHYS}		--	0.5	--	V
PWM Input						
Input High Threshold	PWM_{RTH}		3.5	3.8	4.1	V
Input Low Threshold	PWM_{FTH}		0.7	1	1.3	V
PWM Floating Voltage	PWM_{FLT}		--	2.5	--	V
PWM Input Current	I_{PWM}	PWM = 0V	--	-250	--	uA
		PWM = 5V	--	250	--	uA
Tri-State Shutdown Hold-Off Time			100	175	250	ns
Enable/ Disable Control						
Input High	EN_H		2	--	--	V
Input Low	EH_L		--	--	0.5	V
EN Pin Pull-Low Current	I_{EN_SINK}		--	1	--	uA
Propagation Delay Time	T_{PDHEN}		--	40	--	us
	T_{PDLEN}		--	120	--	ns
Bootstrap Switch						
On Resistance	$R_{DS(ON)}$	Forward bias current = 3.5mA	--	80	--	Ω
Upper Gate Driver						
Output Resistance, Sourcing	R_{H_SRC}	V_{BOOT} - V_{PHASE} = 5V, I_{UGATE} = 500mA	--	1	2.5	Ω
Output Resistance, Sinking	R_{H_SNK}	V_{BOOT} - V_{PHASE} = 5V, I_{UGATE} = 500mA	--	1	2.5	Ω
Output Rising Time	T_{RUGATE}	V_{BOOT} - V_{PHASE} = 5V, C_{LOAD} = 3nF	--	8	--	ns
Output Falling Time	T_{FUGATE}	V_{BOOT} - V_{PHASE} = 5V, C_{LOAD} = 3nF	--	8	--	ns
Propagation Delay Time	T_{PDHUG}	V_{BOOT} - V_{PHASE} = 5V, output no load	--	30	--	ns
	T_{PDLUG}	V_{BOOT} - V_{PHASE} = 5V, output no load	--	18	--	ns
Lower Gate Driver						
Output Resistance, Sourcing	R_{L_SRC}	V_{CC} = 5V, I_{UGATE} = 500mA	--	1	2.5	Ω
Output Resistance, Sinking	R_{L_SNK}	V_{CC} = 5V, I_{UGATE} = 500mA	--	0.5	1	Ω
Output Rising Time	T_{RLGATE}	V_{CC} = 5V, C_{LOAD} = 3nF	--	8	--	ns
Output Falling Time	T_{FLGATE}	V_{CC} = 5V, C_{LOAD} = 3nF	--	8	--	ns
Propagation Delay Time	T_{PDHLG}	V_{CC} = 5V, output no load	--	30	--	ns
	T_{PDLLG}	V_{CC} = 5V, output no load	--	15	--	ns

Application Information

Bootstrap Capacitor Selection

The uP1909R has an internal bootstrap FET rather than bootstrap diode. This minimizes the voltage difference between VCC supply voltage and the actual driving voltage for the upper MOSFET. Connect an external capacitor C_{BOOT} between BOOT and PHASE to form the bootstrap circuit. This capacitor is used to hold electrical charge to turn on the upper MOSFET. C_{BOOT} is charged every time when lower MOSFET is on, and is only discharged when upper MOSFET is on. To select the capacitance value of C_{BOOT}, there are two parameters need to be taken into consideration. One is the total gate charge of MOSFET being driven ($Q_{G,total}$), and the other is maximum allowable driving voltage drop (ΔV_{BOOT}). The capacitance can be determined as follows.

$$C_{BOOT} = \frac{Q_{G,total}}{\Delta V_{BOOT}}$$

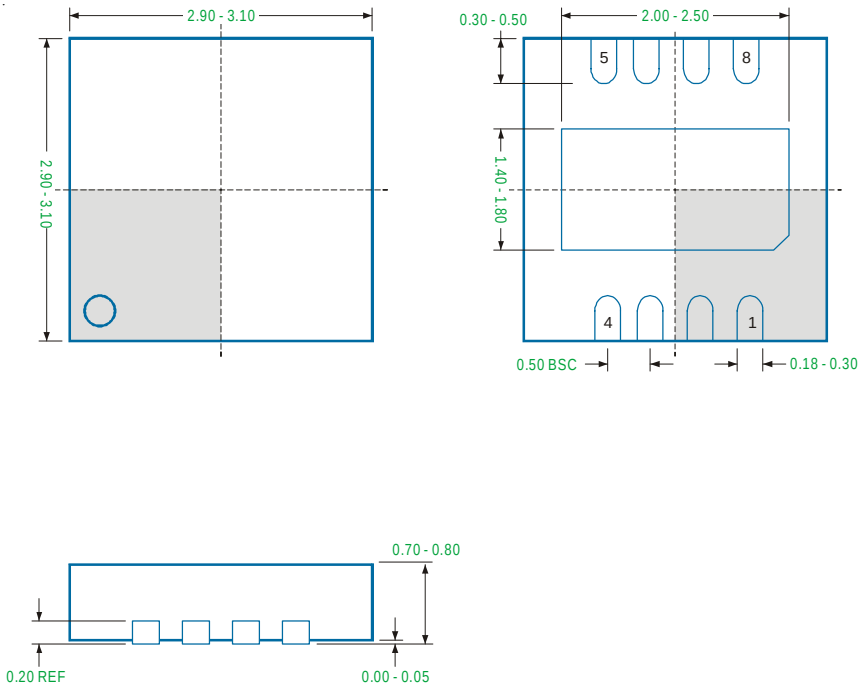
For example, two MOSFET in parallel have total gate charge of 25nC at 5V, and the maximum allowable driving voltage drop is 0.25V, the resulting C_{BOOT} is 0.1uF. Higher C_{BOOT} results in lower driving voltage drop. In most applications, C_{BOOT} value is usually between 0.1uF to 1uF. Make sure ceramic capacitor is used as the C_{BOOT}, since this capacitor is in high frequency operation.

PCB Layout Guide

- The MOSFET driver itself should be placed close to the power MOSFETs to be driven.
- All the trace between power MOSFET and gate driver output (UGATE, PHASE, LGATE) should be as short as possible, and the trace width should be wide. Short trace length has lower trace inductance, and wide trace width has lower resistance. These helps reduce the ringing spike in high frequency switching.
- Bootstrap capacitor C_{BOOT} must be placed close to the MOSFET driver. The trace length between BOOT and PHASE must be short. Use wide trace in this routing.
- Use at least 1uF ceramic capacitor and connect it between VCC and GND. Place this capacitor physically close to the VCC pin. The routing trace width should be wide, and the ground via should be placed near the capacitor pad.
- The exposed pad should be soldered on the ground plane with minimum impedance. Place sufficient ground via on the exposed pad layout area since it is the driving current return path.
- Avoid using via in the trace routing between power MOSFET and gate driver output (UGATE, PHASE, LGATE). If via must be used, make sure the number of via is sufficient to sustain at least 2A driving current.

Package Information

WDFN3x3 - 8L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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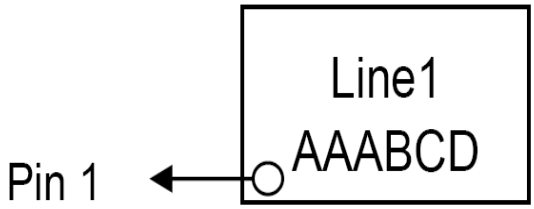
Top Marking Rule



Line 1 : Product Code

Part No.	Product Code
uP1909RDD8	**uP1909R**

Line 2 :
AAA - uPI internal trace code
BCD - Date Code, rules as below:

B：Last one of western calendar year (0~9), ex. 2007=7, 2008=8

C：Month

Month	Code	Month	Code	Month	Code	Month	Code
Jan	**1**	Apr	**4**	Jul	**7**	Oct	**A**
Feb	**2**	May	**5**	Aug	**8**	Nov	**B**
Mar	**3**	Jun	**6**	Sep	**9**	Dec	**C**

D：Date

Date	Code	Date	Code	Date	Code	Date	Code
1	**1**	9	**9**	17	**H**	25	**S**
2	**2**	10	**A**	18	**J**	26	**T**
3	**3**	11	**B**	19	**K**	27	**U**
4	**4**	12	**C**	20	**L**	28	**V**
5	**5**	13	**D**	21	**M**	29	**W**
6	**6**	14	**E**	22	**N**	30	**X**
7	**7**	15	**F**	23	**P**	31	**Y**
8	**8**	16	**G**	24	**R**		

WDFN3x3 Package

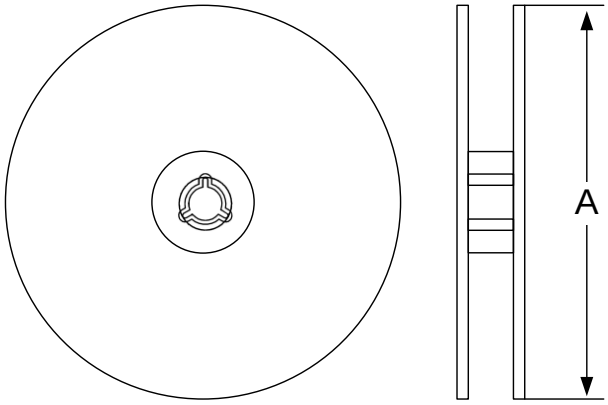
Definition:

DFN = Dual Flat No Lead

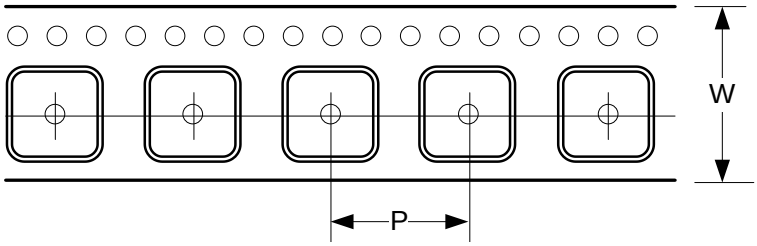
W Type= Very Very Thin Package(Thickness = 0.75 ± 0.05mm)

Tape & Reel Drawing

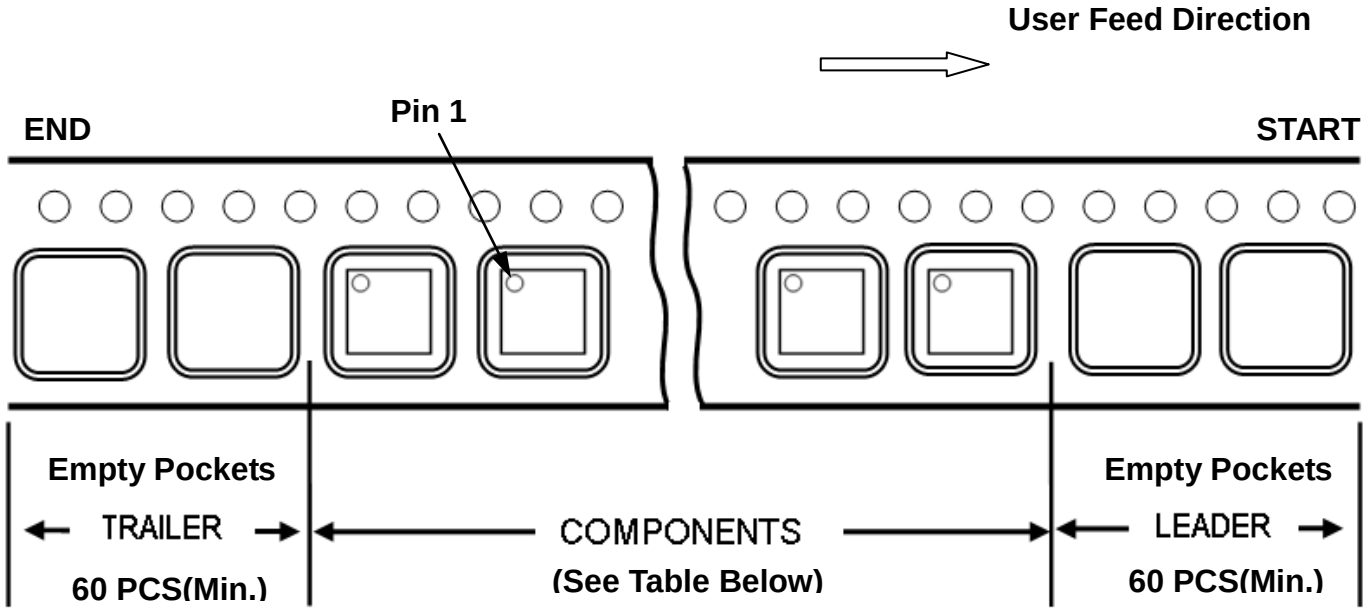
Lock Reel



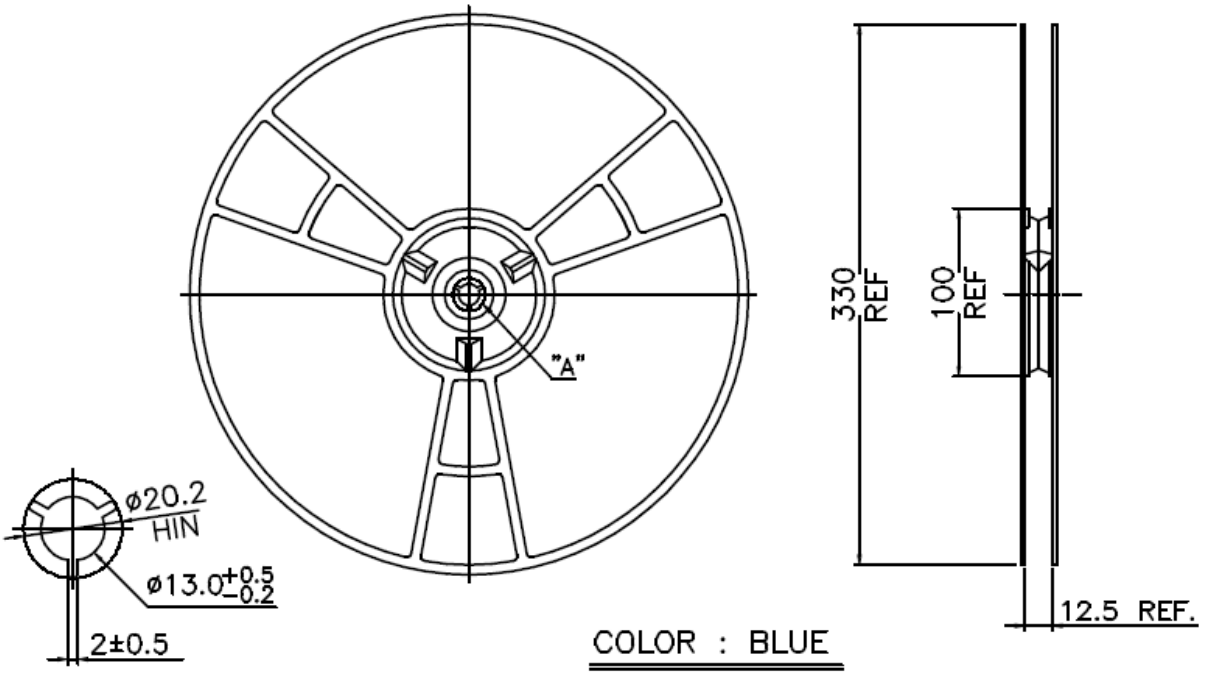
Carrier Tape

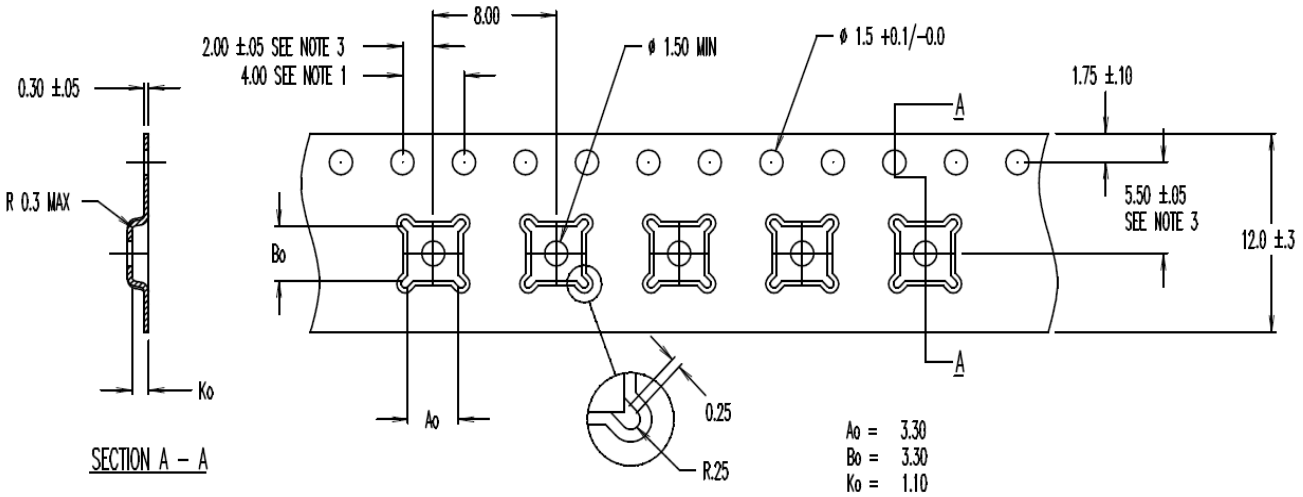


Packing Illustration



Carrier Tape Drawing





Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Cover Tape width 9.3±0.1mm.

Packing Quantity List

PKG Type Body Size	Reel Diameter(A) (inch/mm)	Carrier Width(W) (mm)	Carrier Pitch(P) (mm)	Reel Quantity (pcs)	Remark
WDFN 3x3	13 / 330	12	8	2500	

Packaging Drawing

Barcode Label – Apply for Reel/Al Bag/Inner Box and Outer Carton

P/N：uPI Part Number

LOT：Wafer Lot Number

QTY：Packing Quantity

D/C：Manufacturing Date Code

DATE：Packing Date

Note：For Internal Use Only

Inner Box

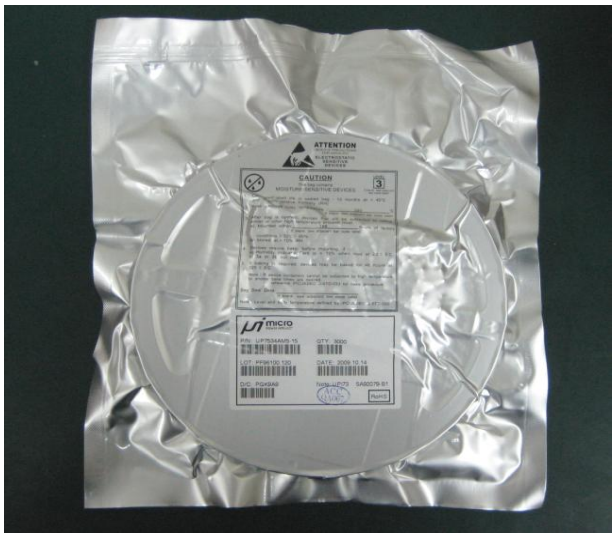
Box (13” Reel 355 x338 x 50 mm)

Outer Carton

Carton A (382 x 283 x390 mm)

Package Storage Condition:

- Vacuum Sealed into Moisture Barrier Bag and Meet MSL Level 3 requests.
- Comply with J-STD-033 standard.



- Storage Condition

  Vacuum Sealed : 12 months at <40℃ and 90%RH

  Bag Opened : Within 168 hrs at < 30℃ / 60%RH

- Baking Condition

  Re-Backing @ 125℃ +/- 5 ℃, 9hrs for IC only;

  Floor life begins counting at time =0 after Re-Backing.

  The times of Re-Backing: 2 times, Max.