

PG142-B00

DP + DP + DP + HDMI/DP


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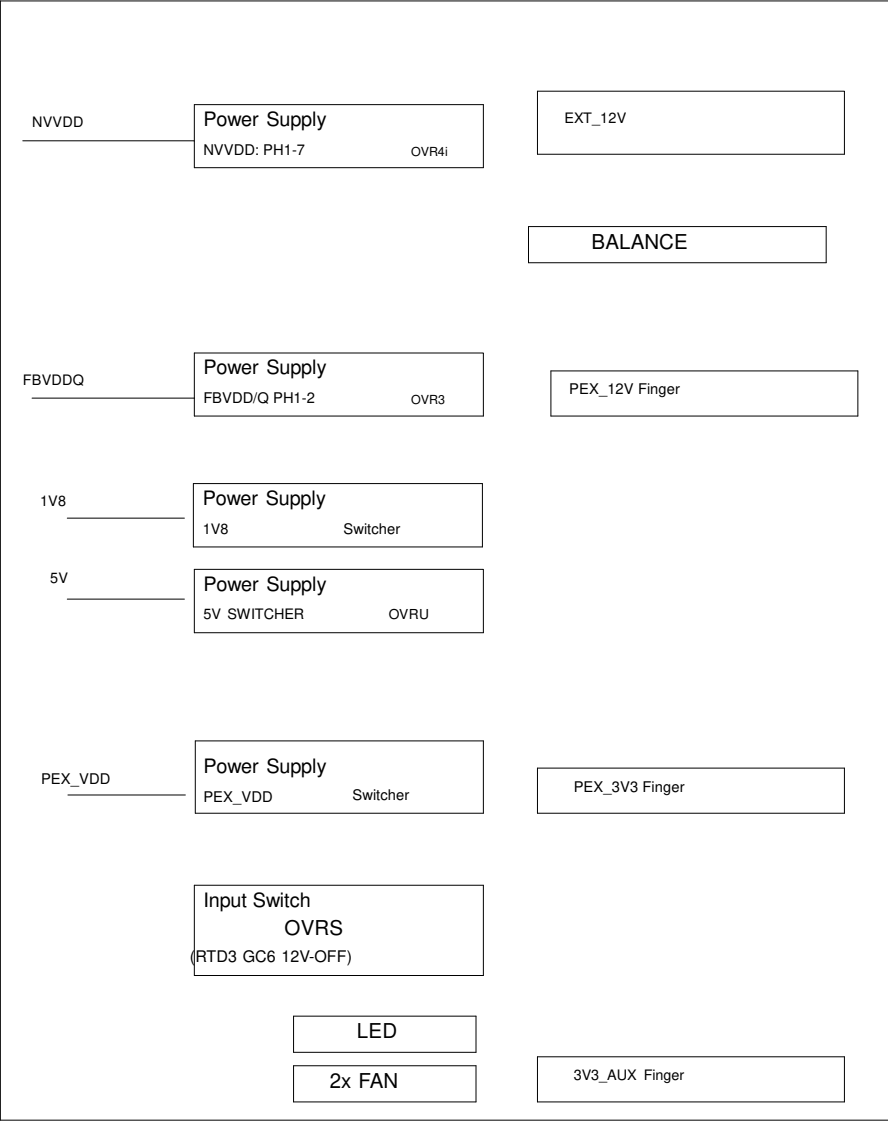
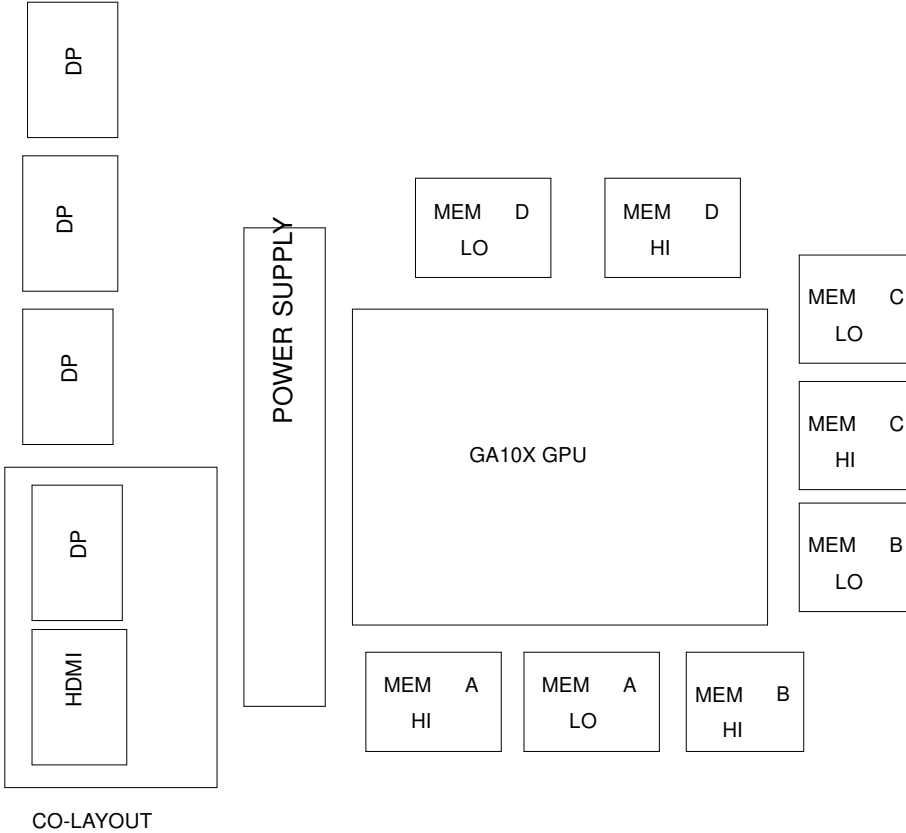
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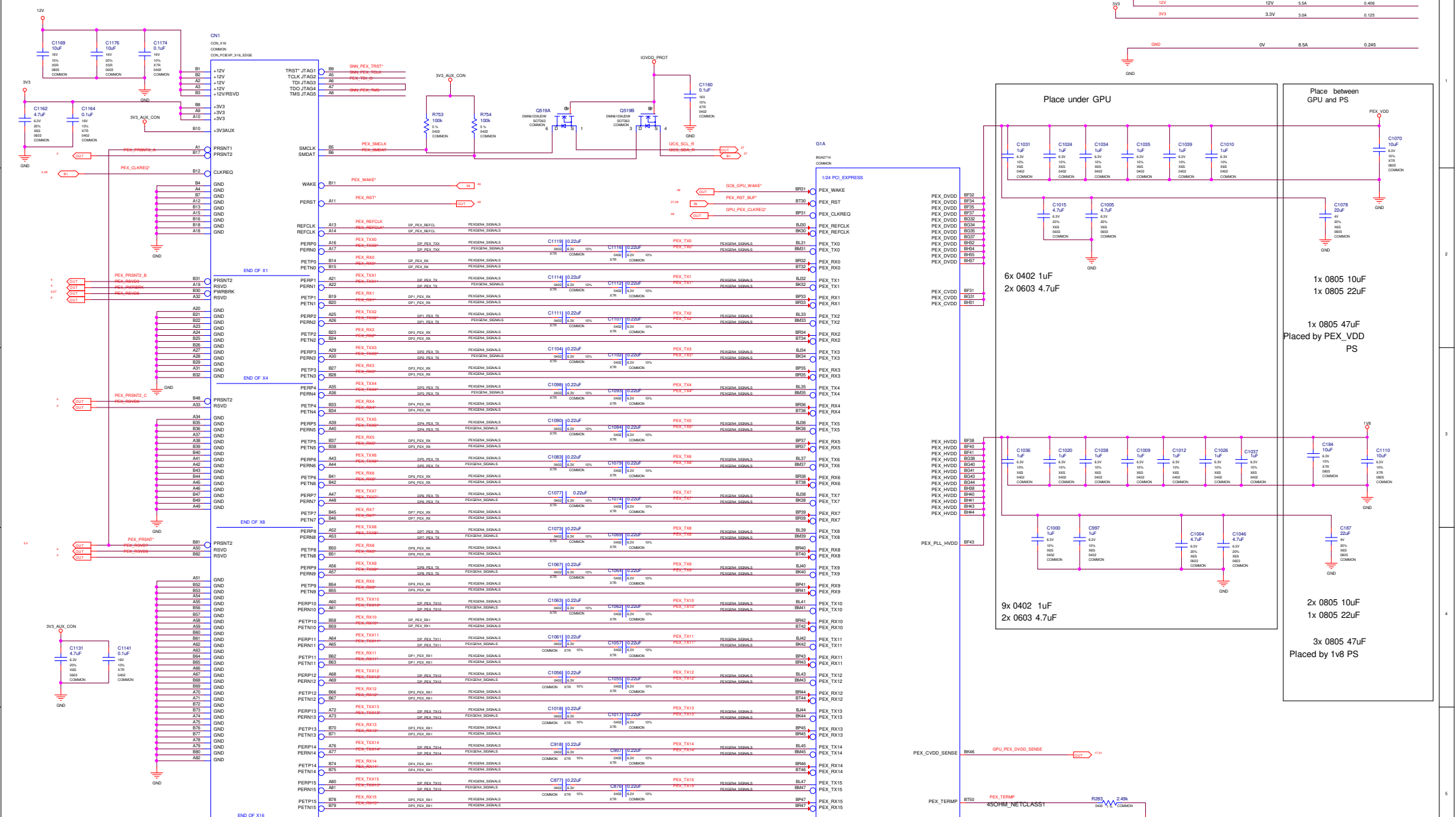


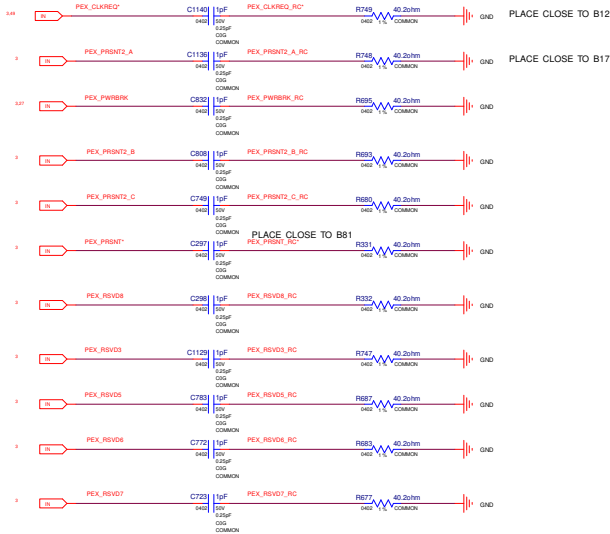
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ASSEMBLY	-ASSEMBLY DESCRIPTION-
PAGE: DETAIL	Block Diagram

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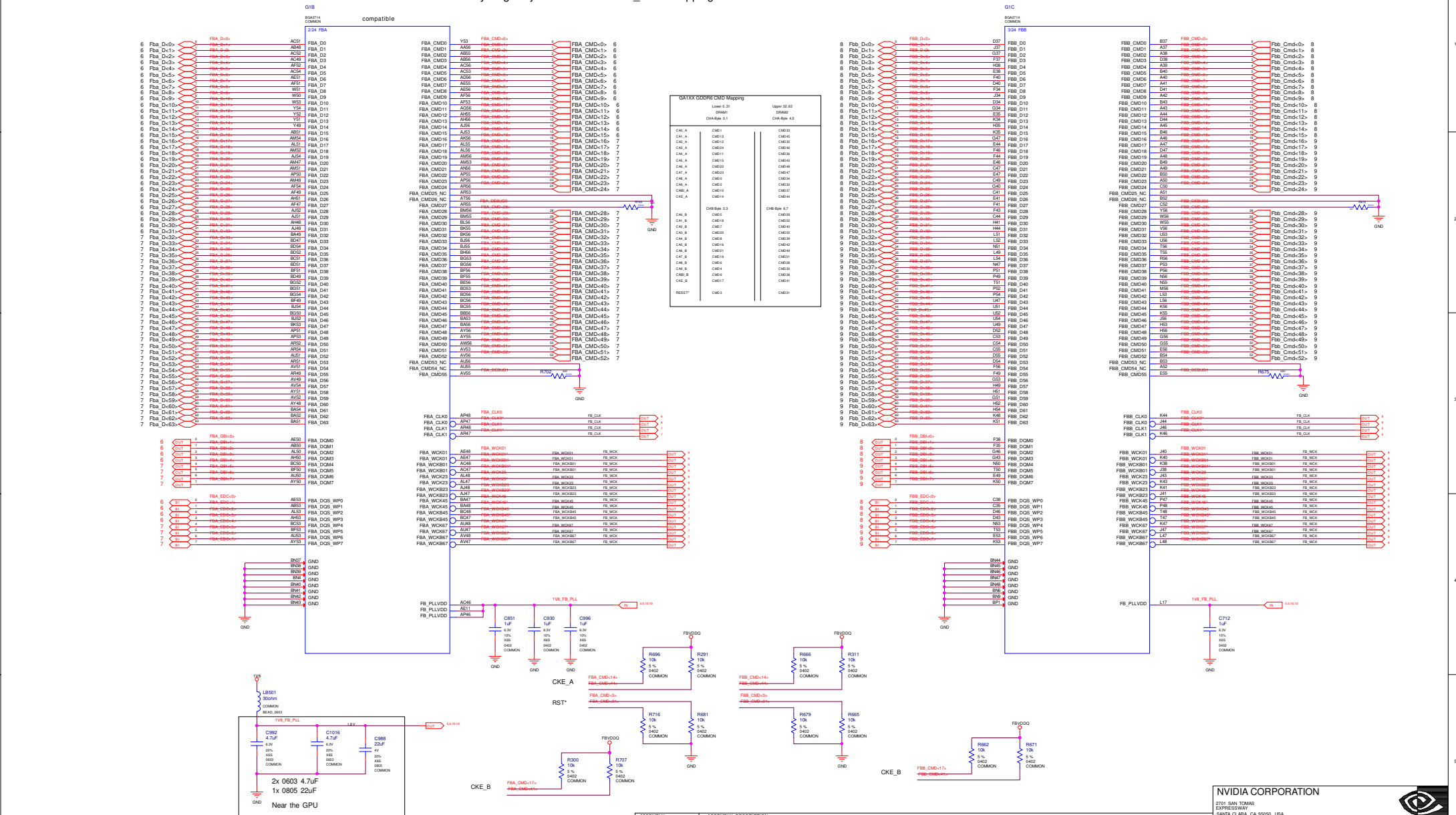
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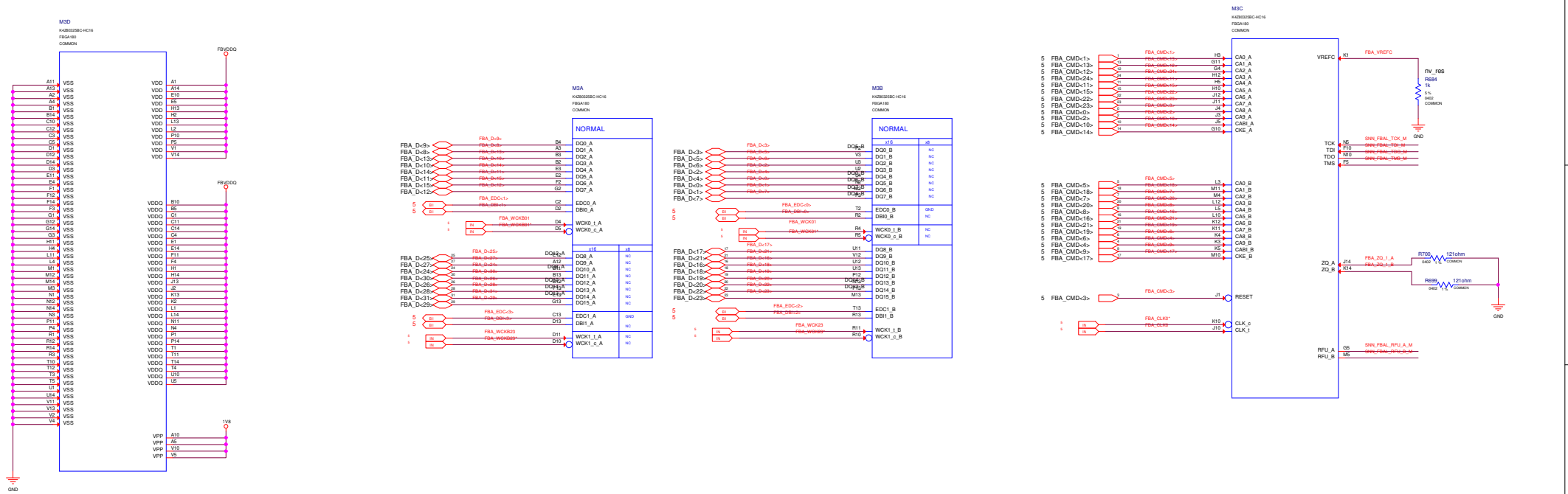
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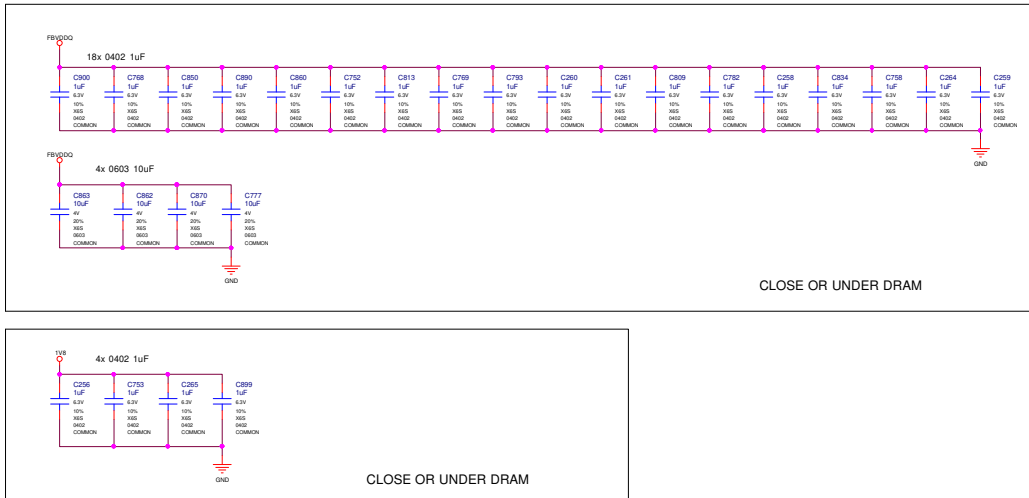


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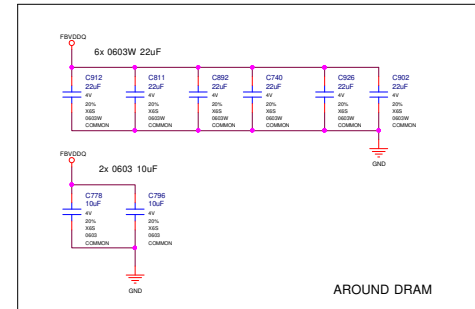
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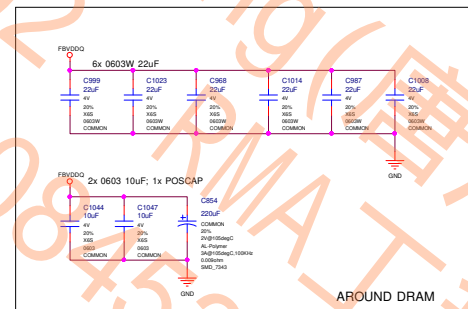
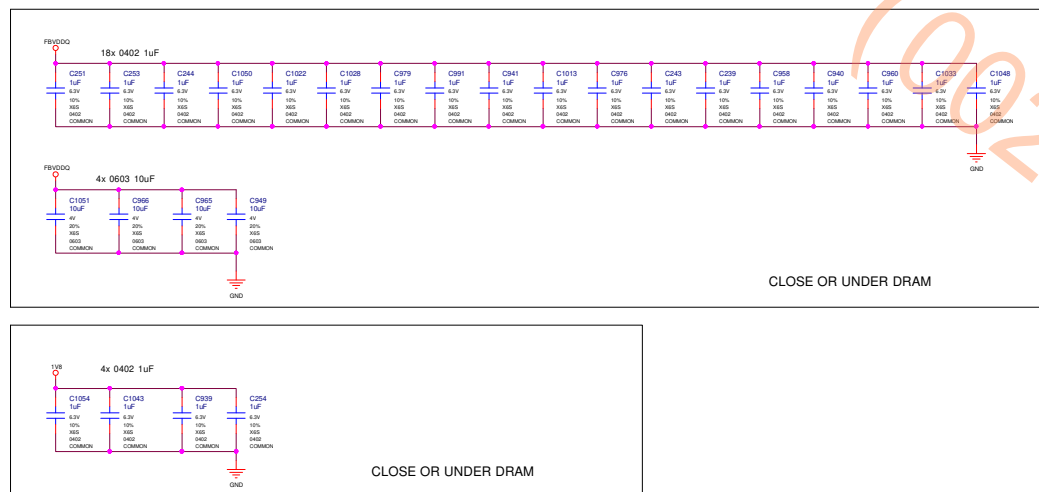
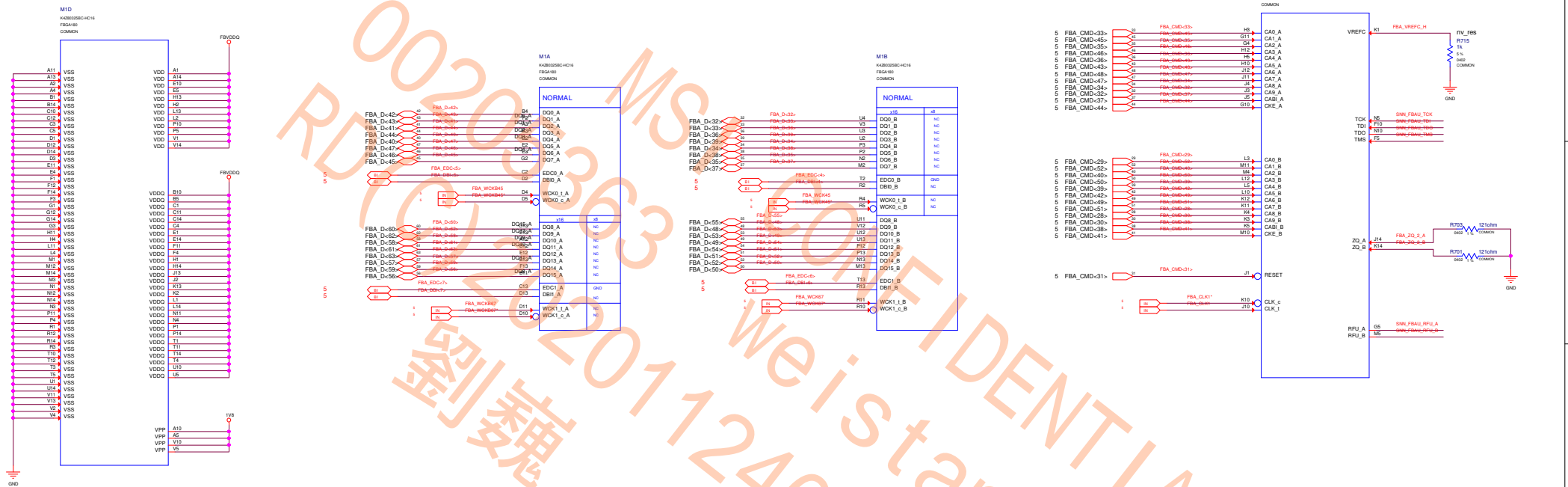
decap via : at least 2 grnd vias and 2 power vias for each cap



CLOSE OR UNDER DRAM




AROUND DRAM



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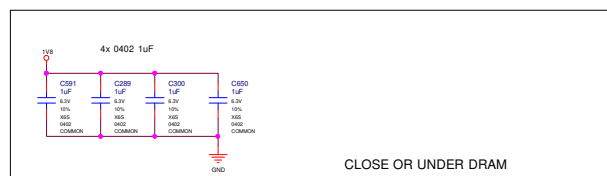
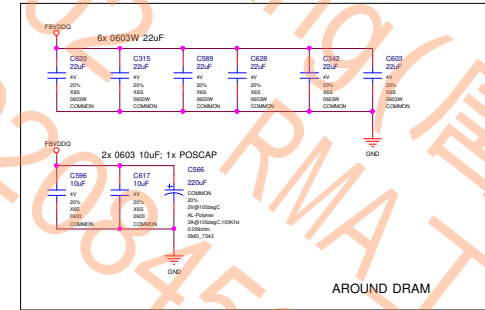
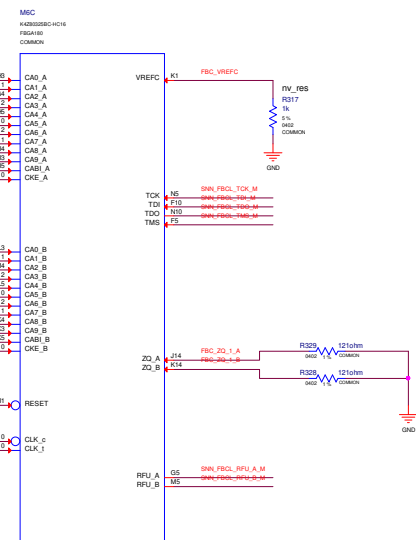
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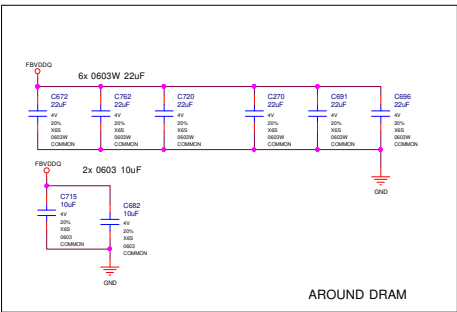
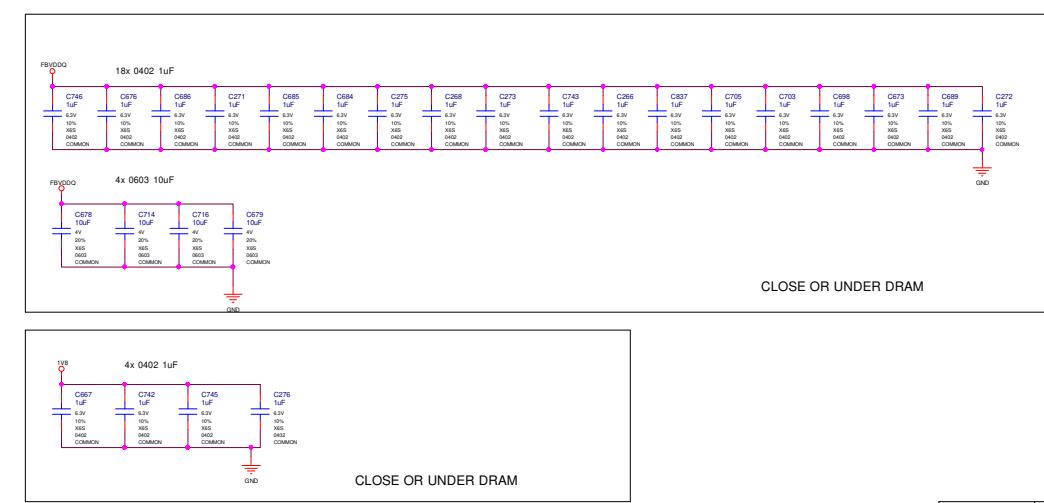


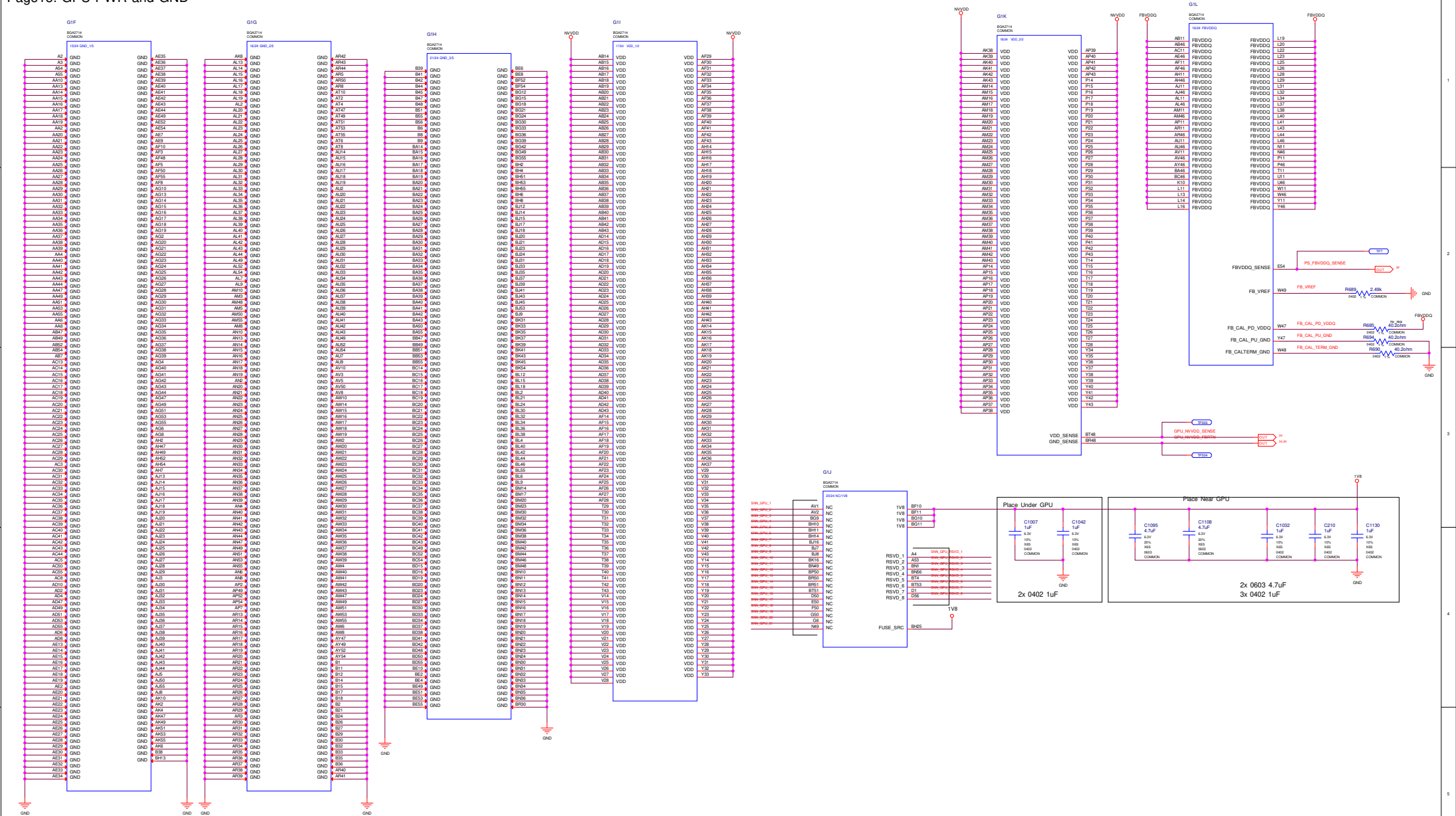


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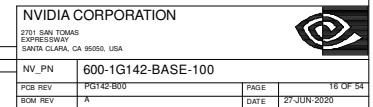
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 PAGE DETAIL GPU PWR & GND

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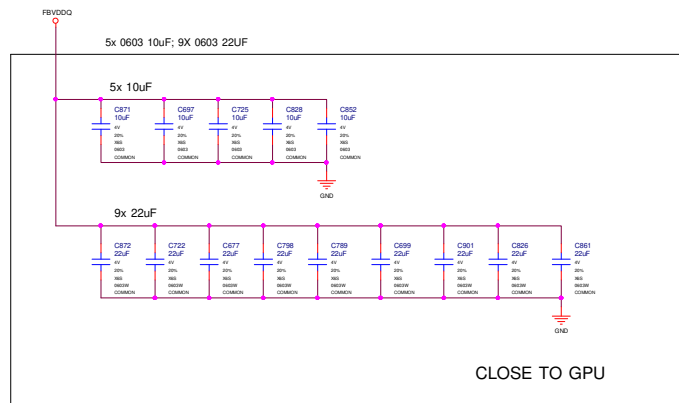
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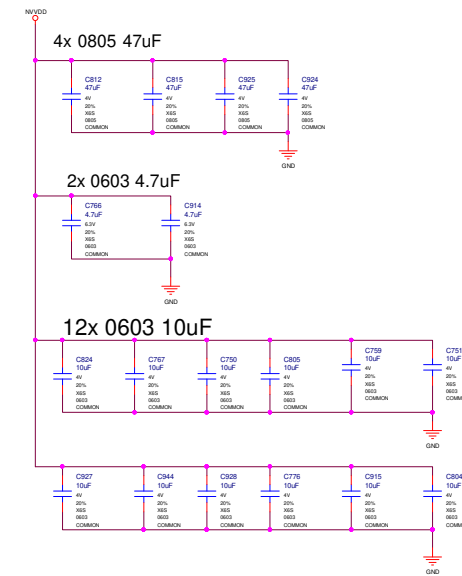
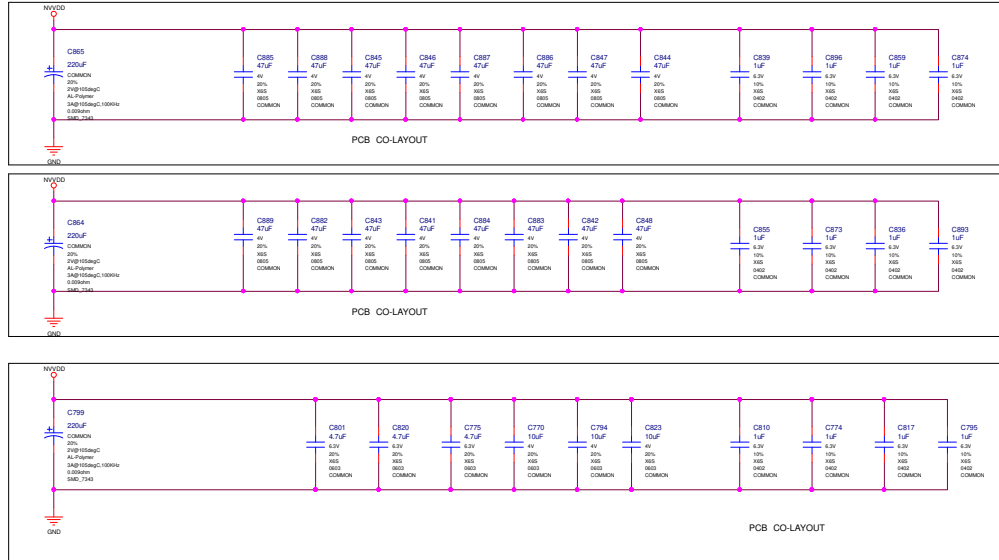




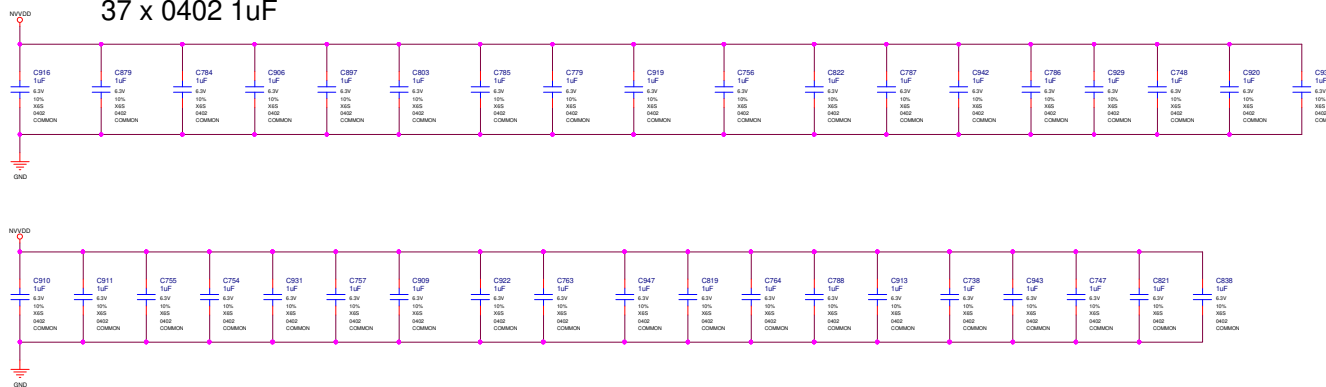
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UNDER GPU






37 x 0402 1uF

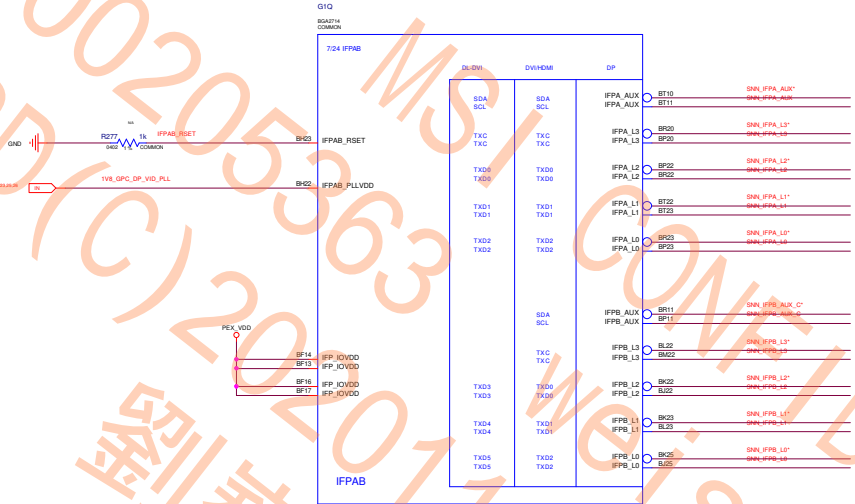


UNDER GPU

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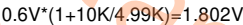


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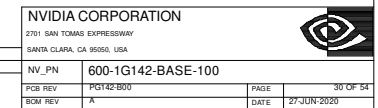


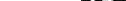


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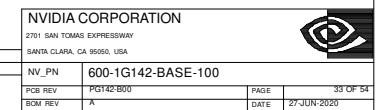


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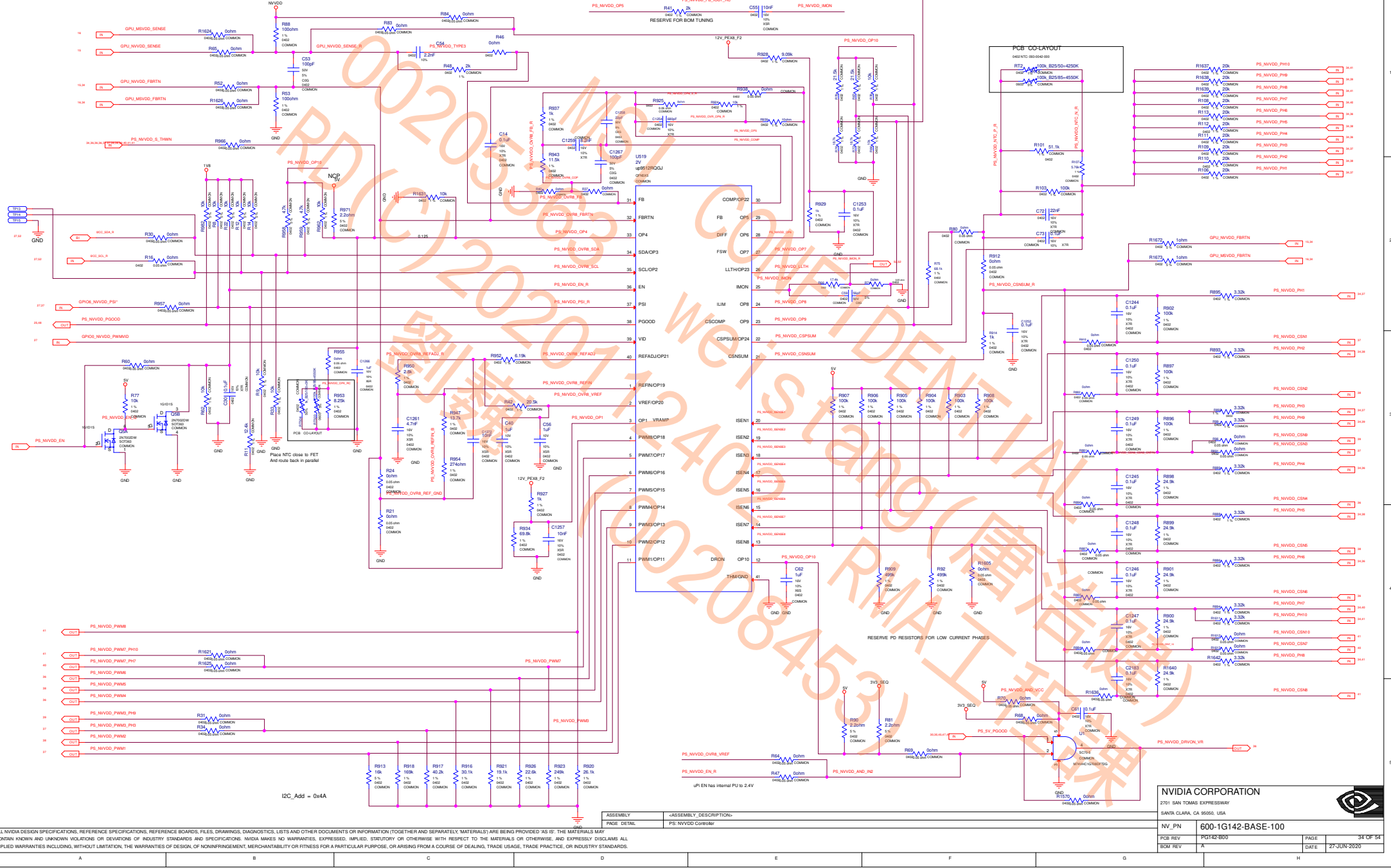


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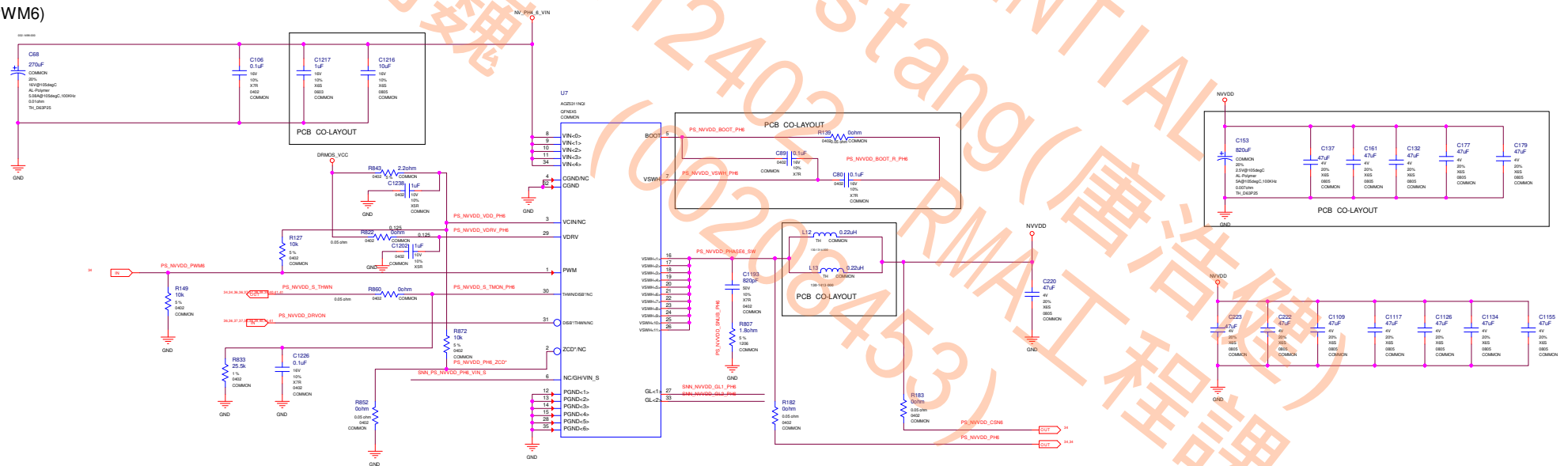
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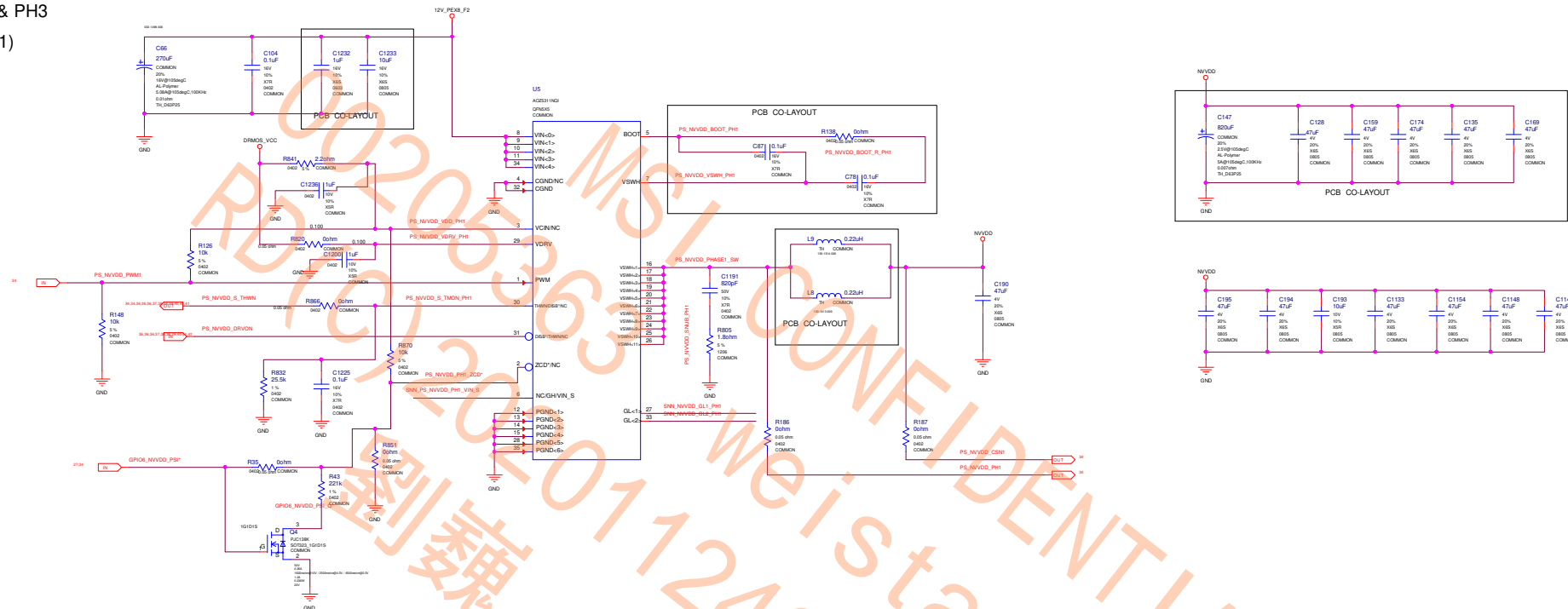
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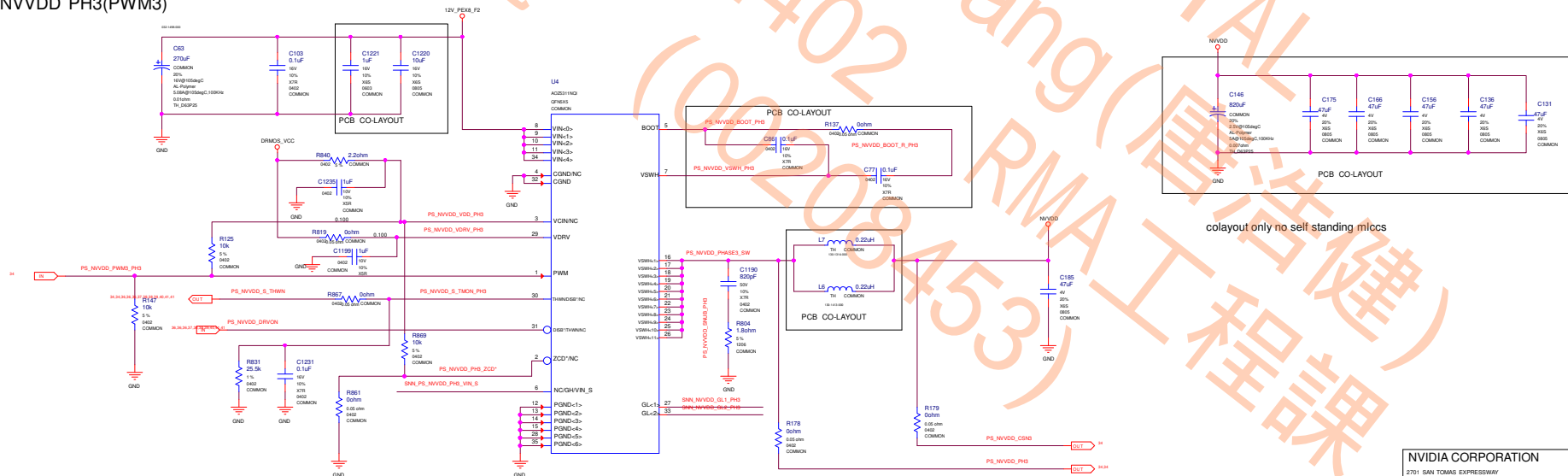




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NVVDD PH3(PWM3)



colayout only no self standing mlccs

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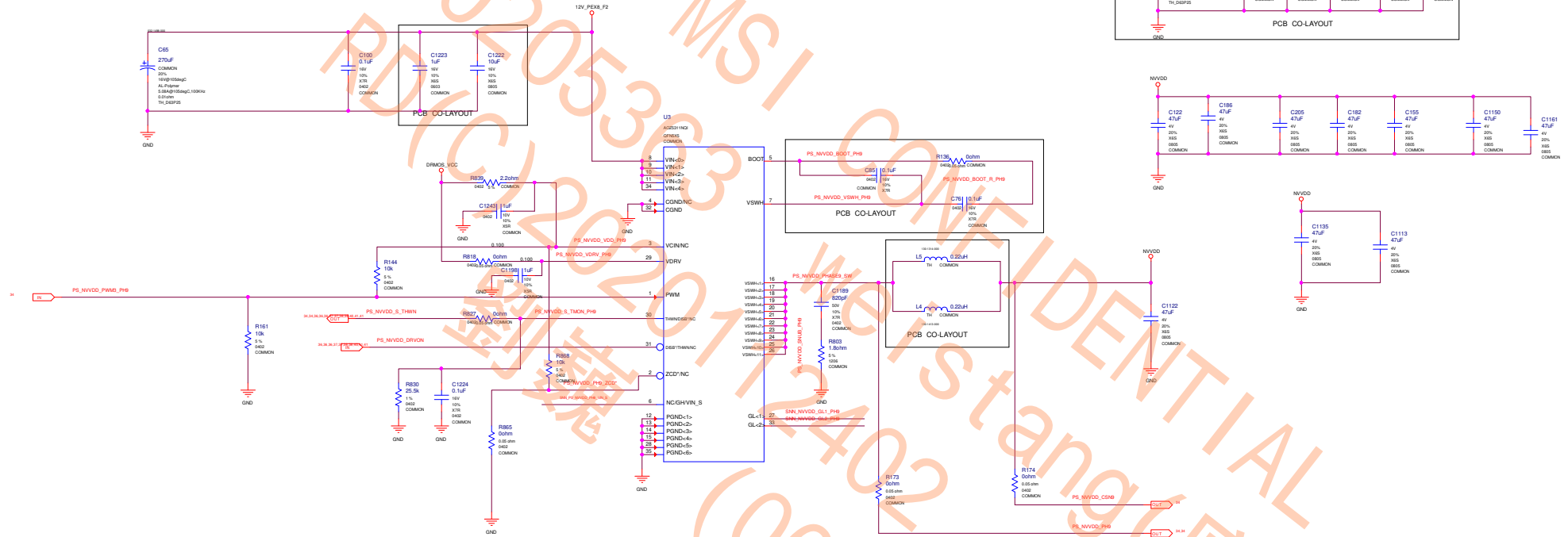
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NVVDD PH9(PWM3)



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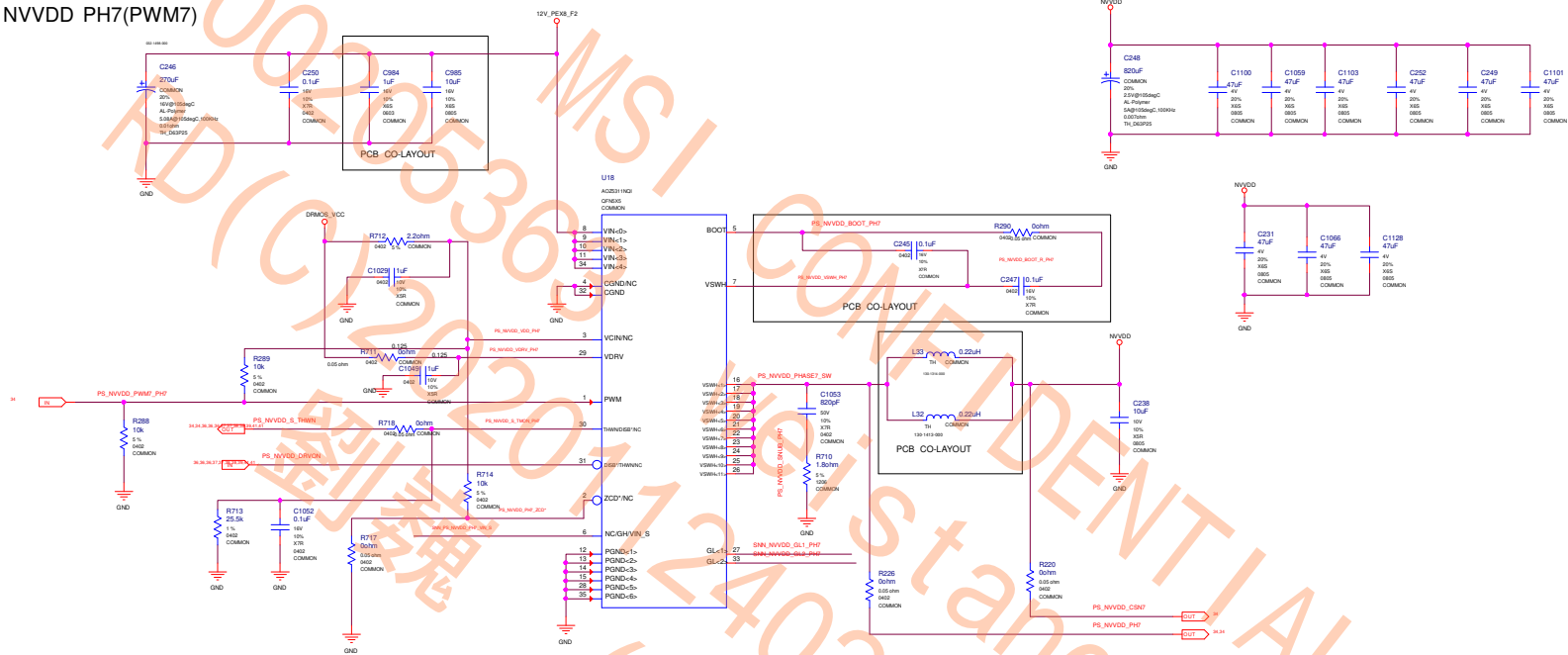
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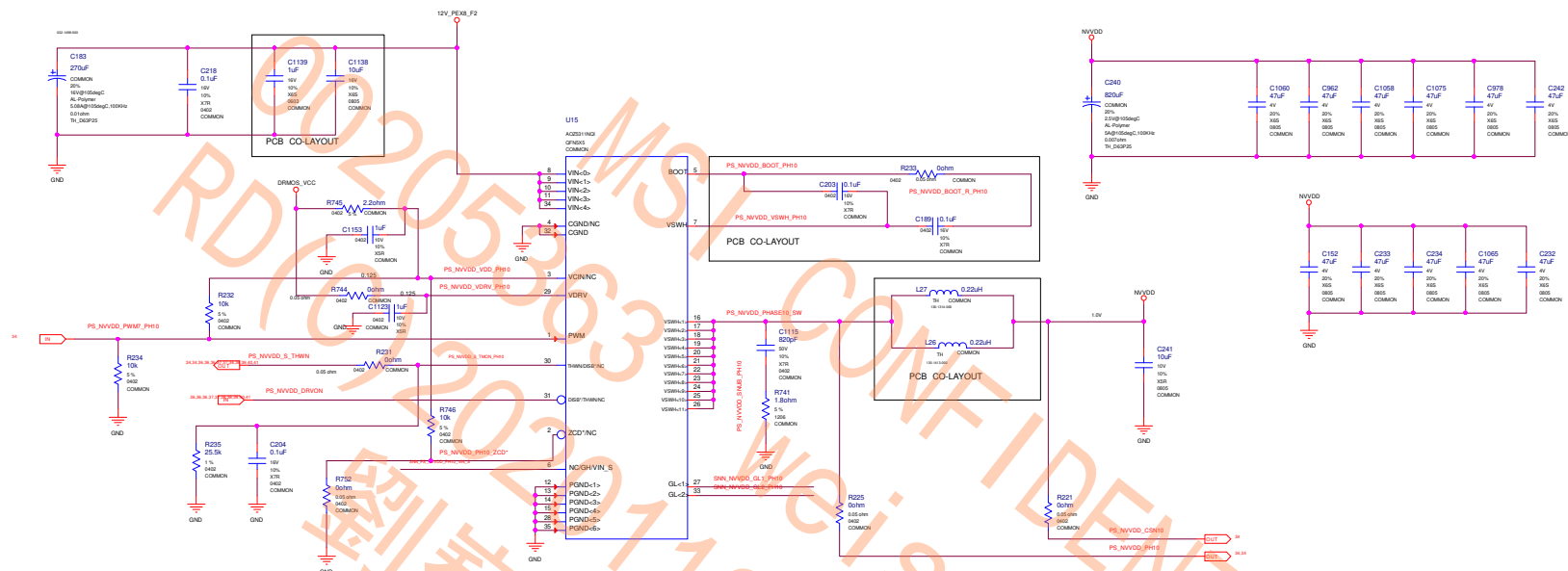
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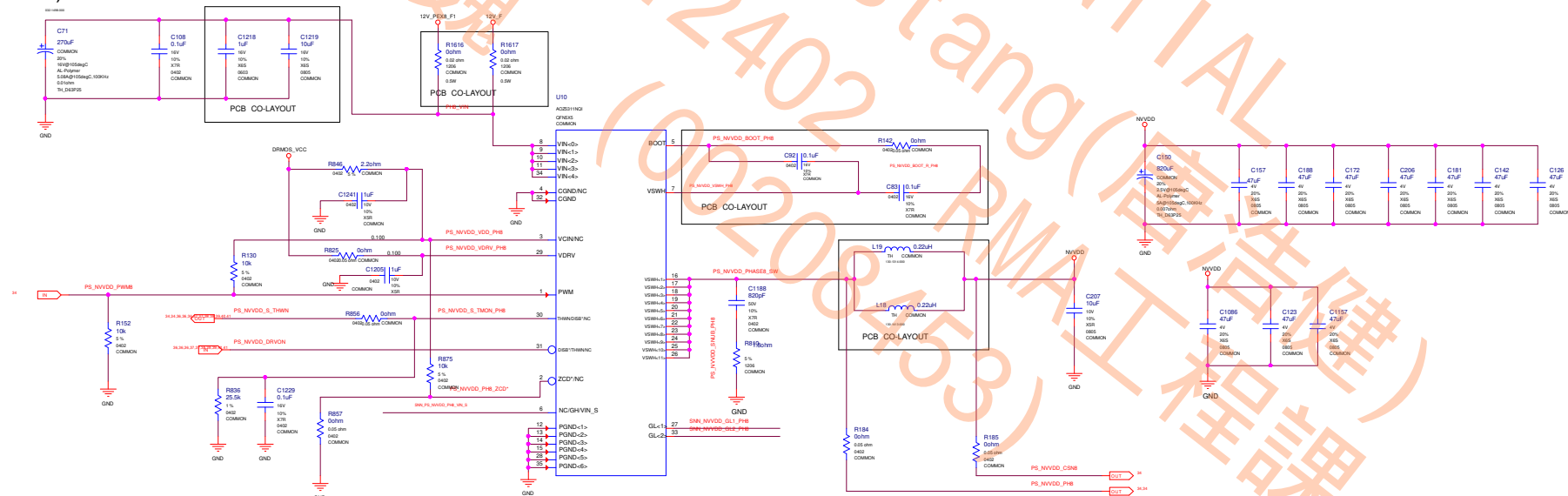
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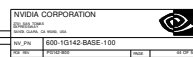


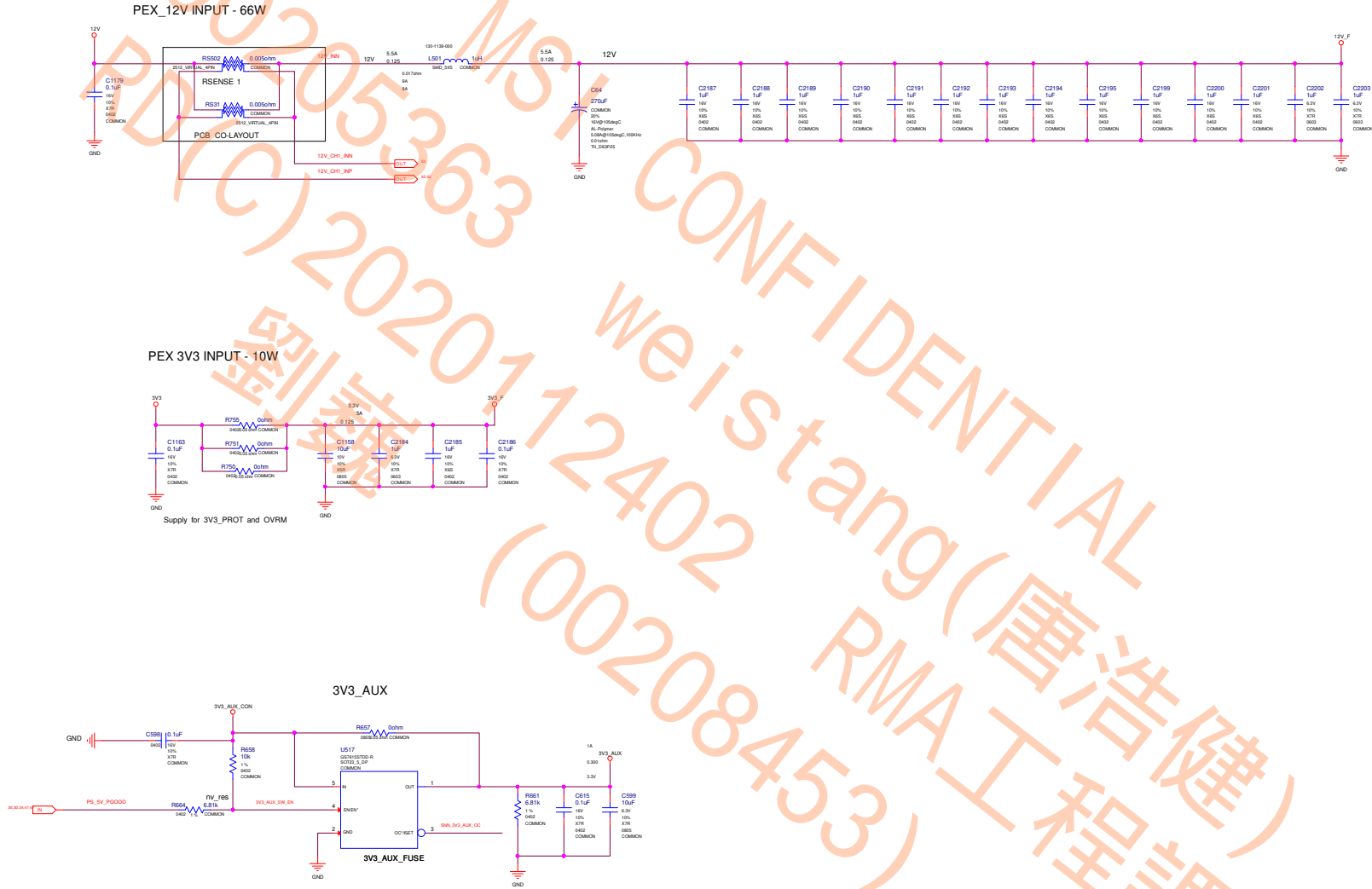
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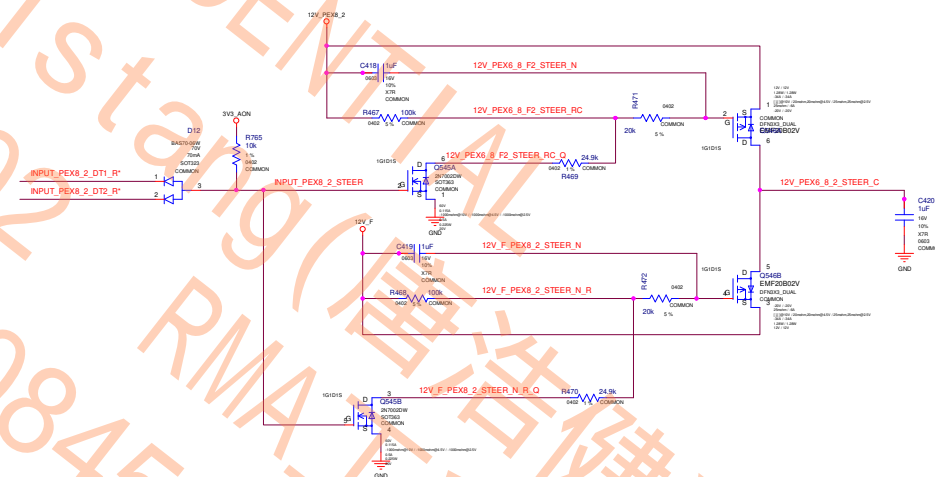
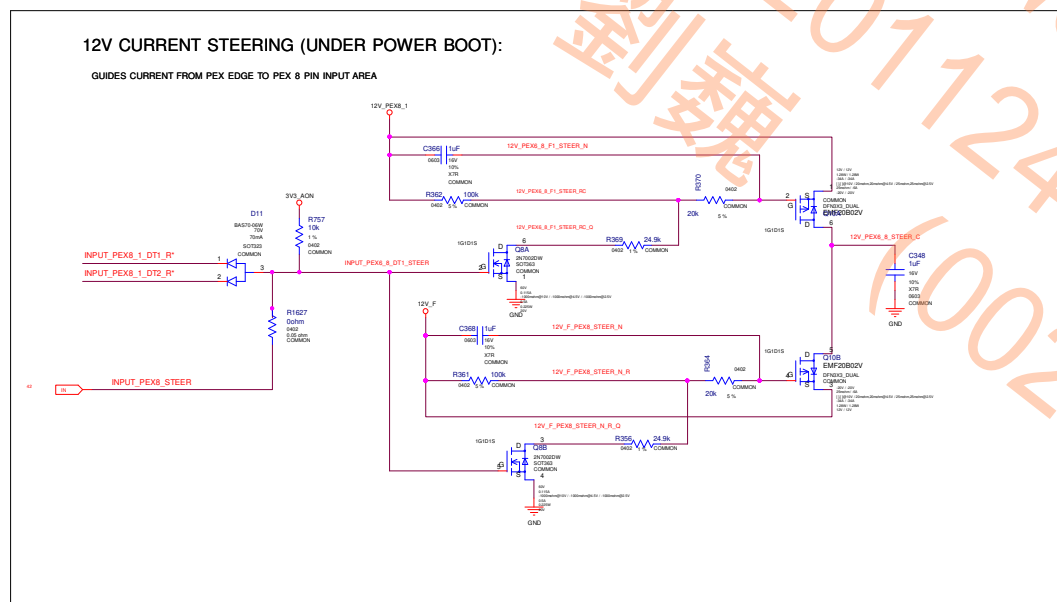
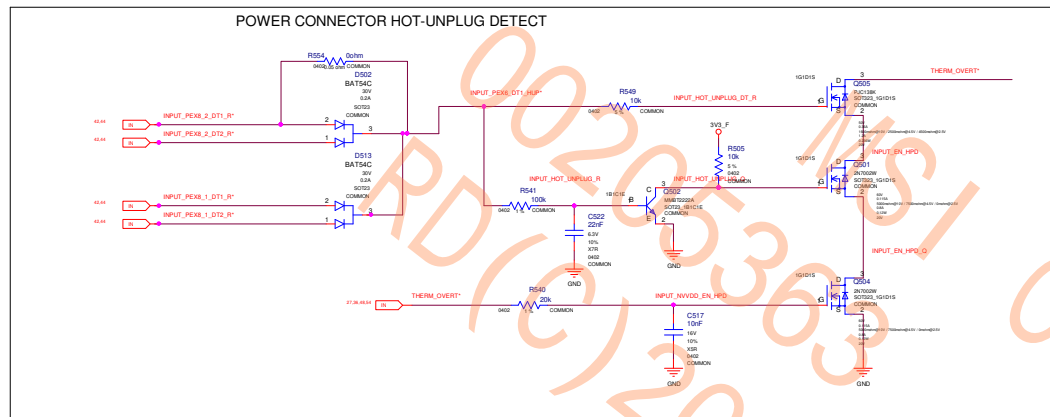
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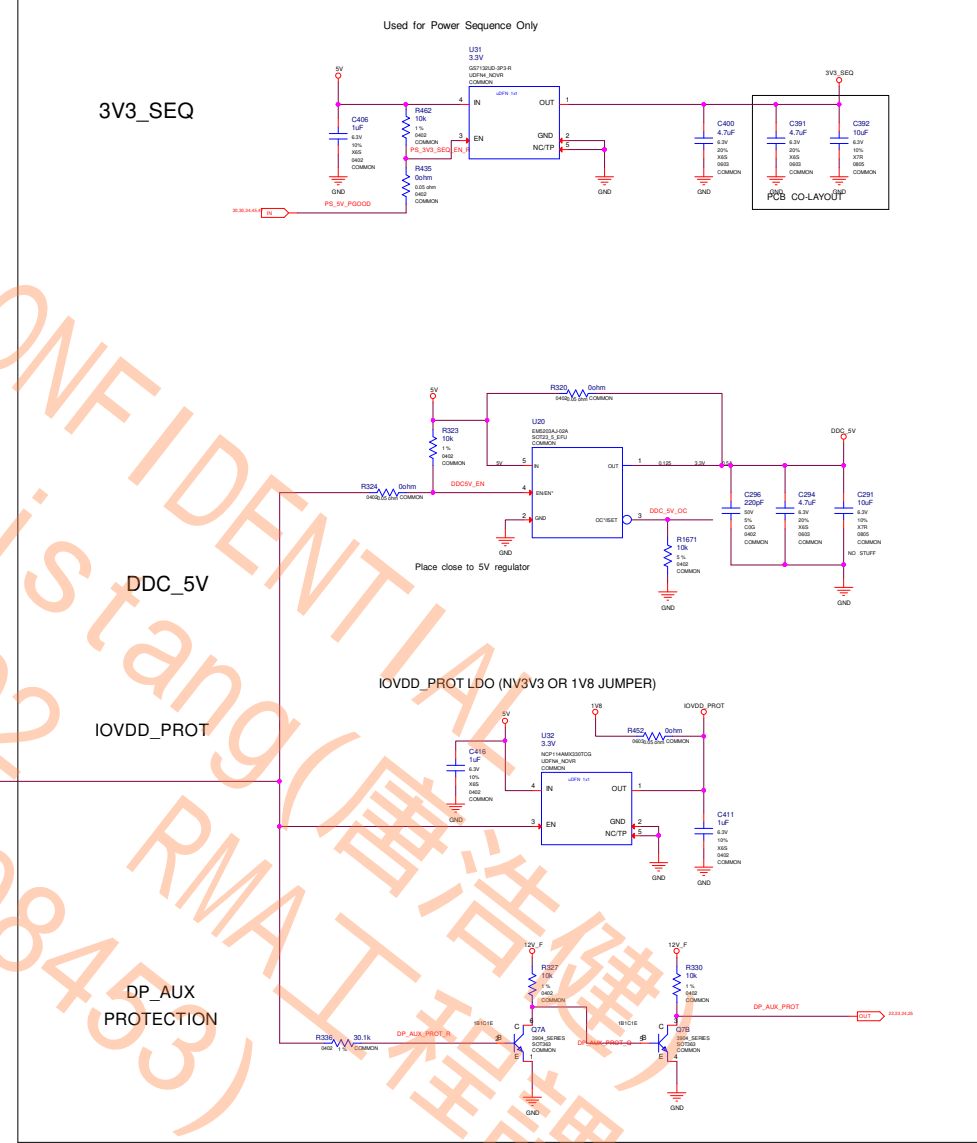
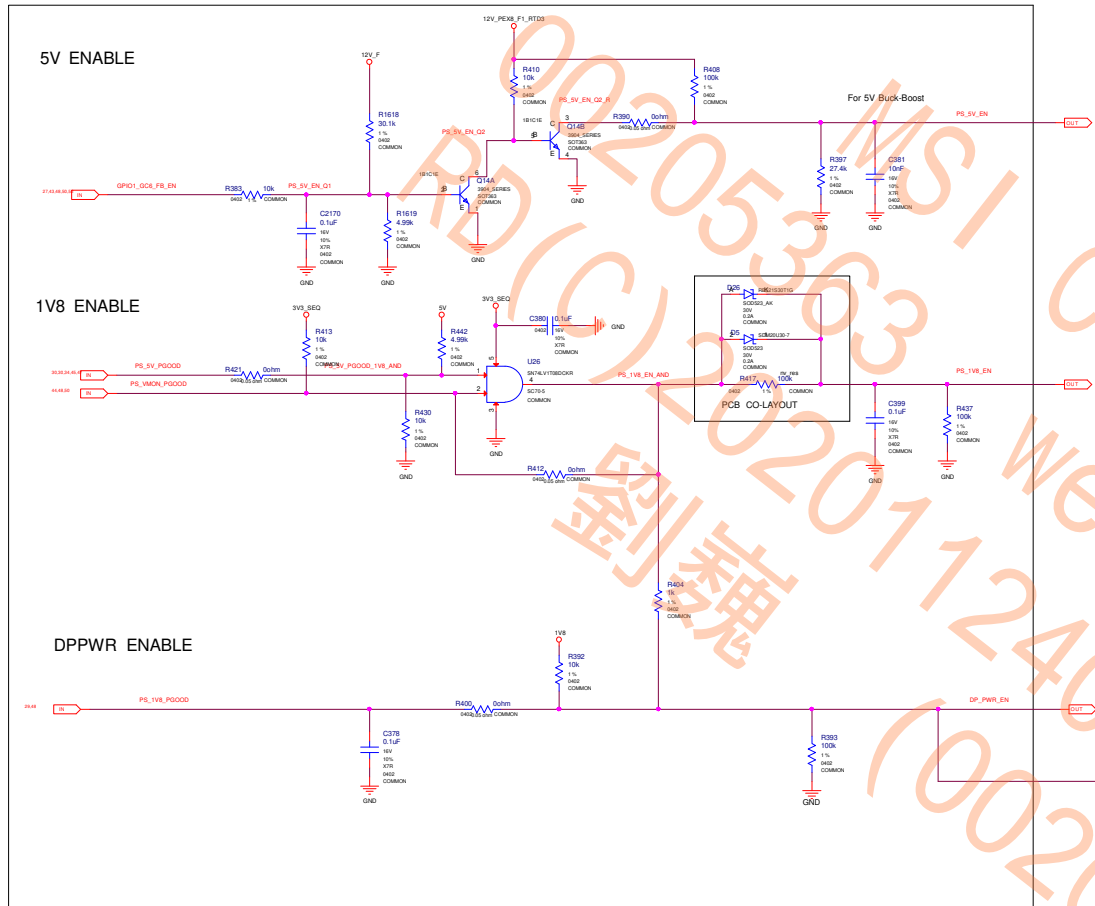
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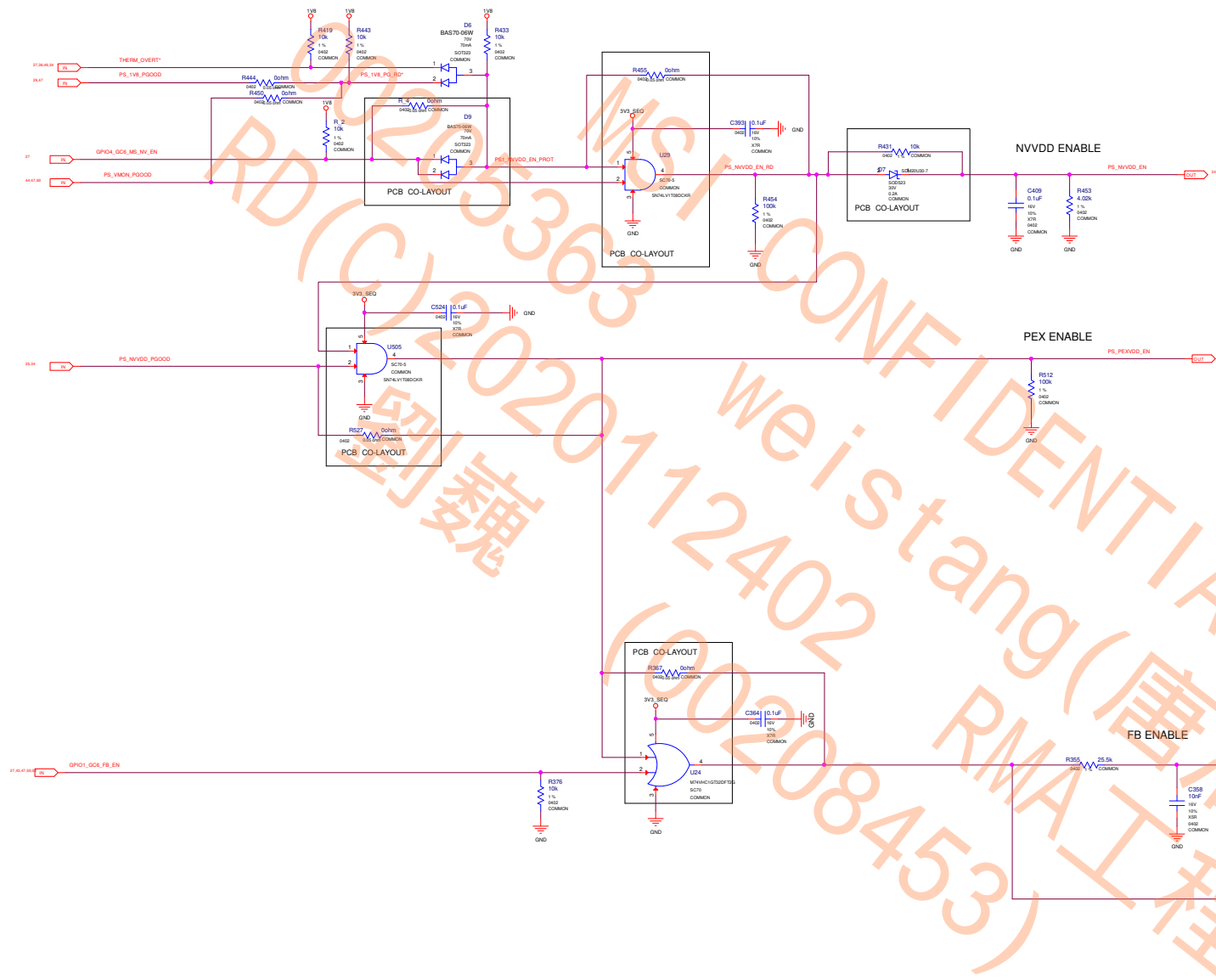
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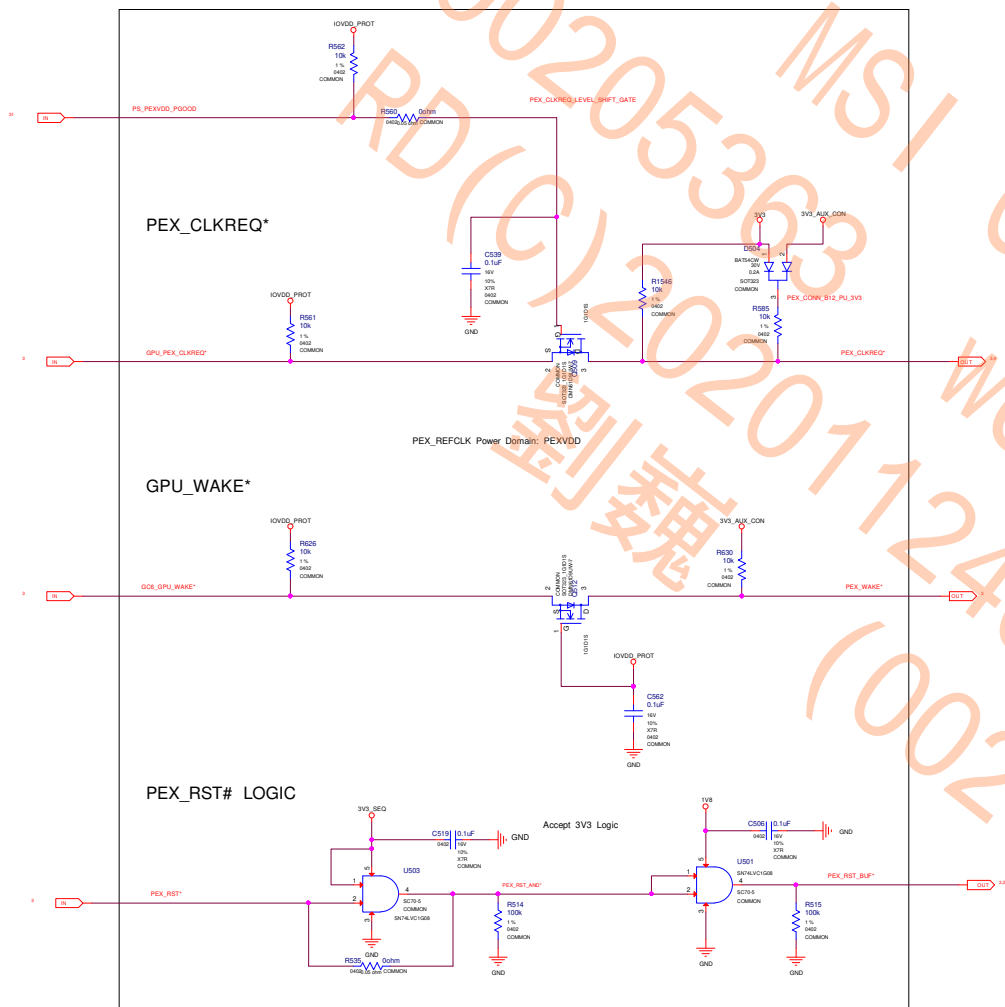
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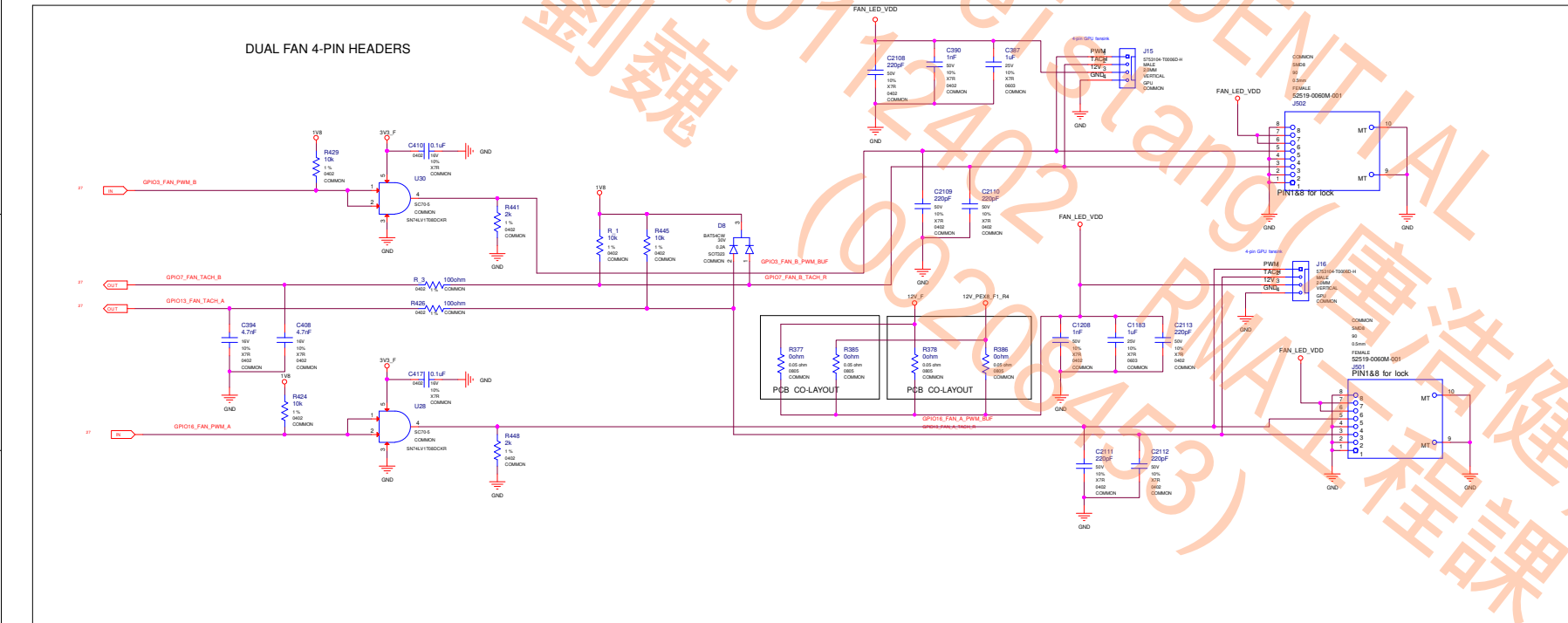
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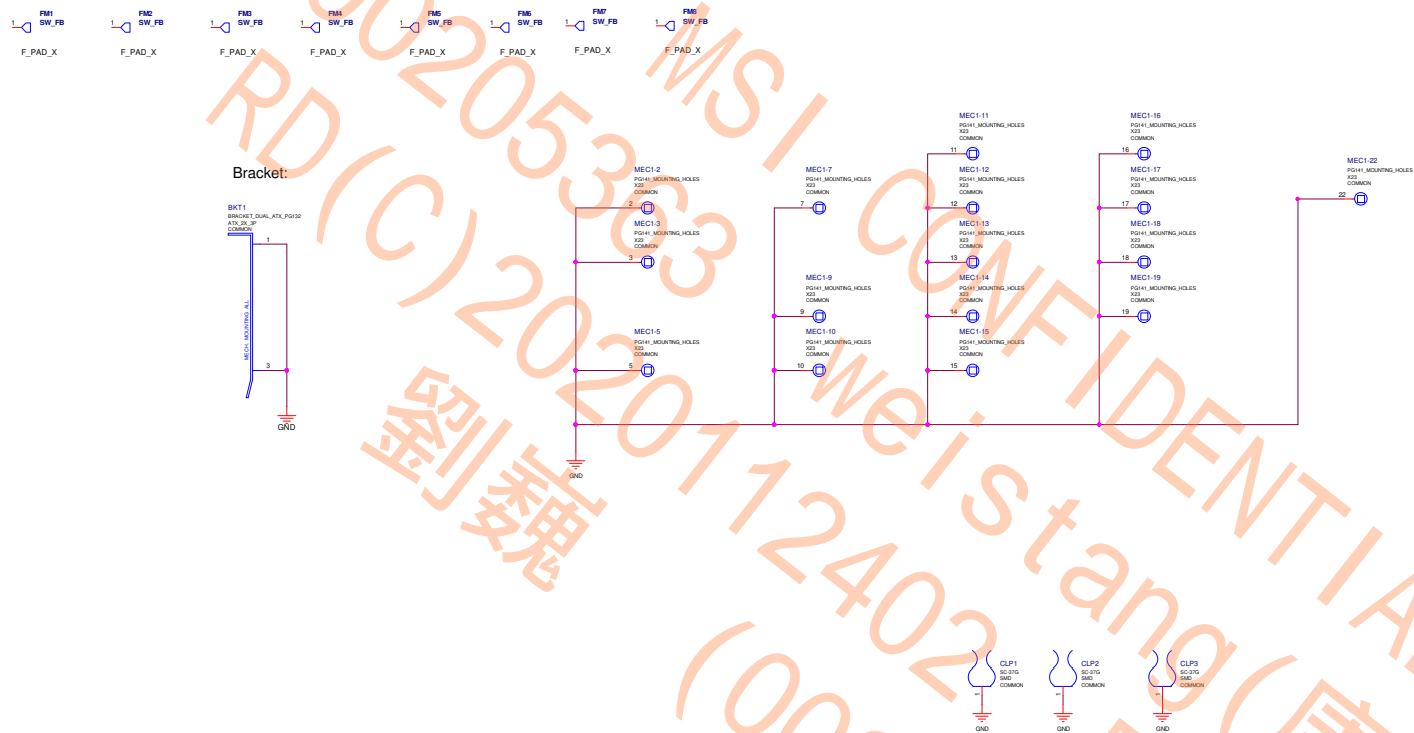
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