<Variant Name>

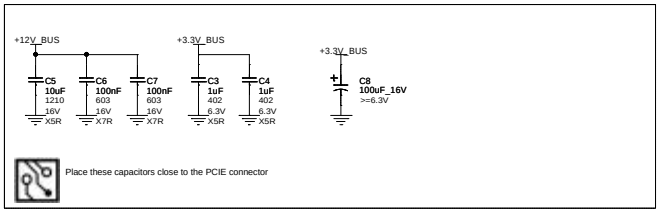
Title	Schematic No.	Date:
RV370 128bit 256MB DDR2 NT DMS59-VO LP	105-A62931-00	Tuesday, June 07, 2005

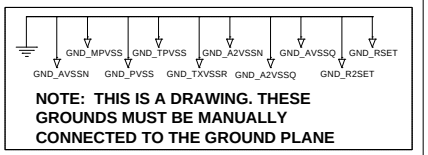
REVISION HISTORY

Rev 1

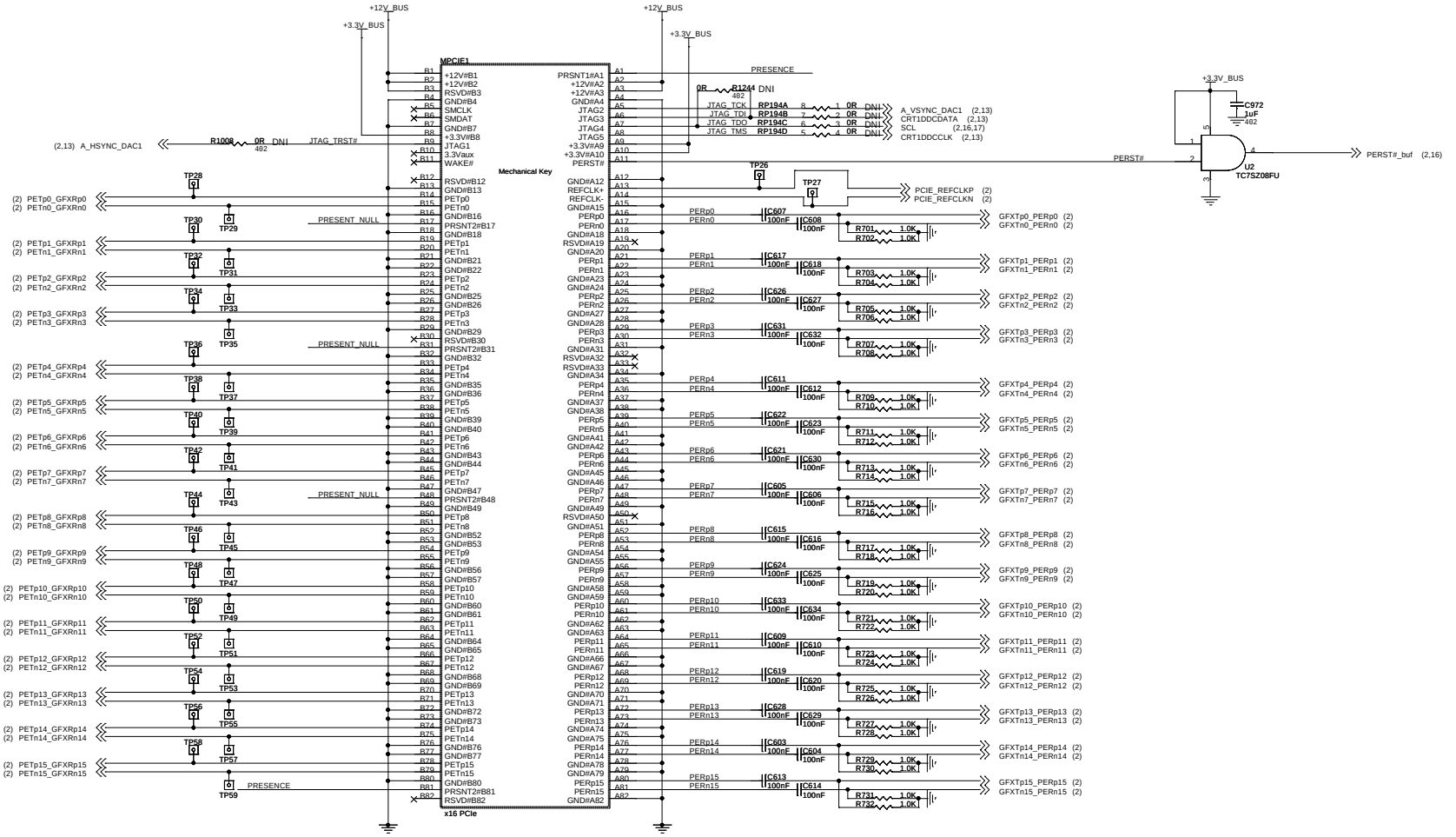
Sch Rev		Date	REVISION DESCRIPTION
0	00A	2005-01-11	PRELIMINARY BASED ON 105-A532XX-00A - Memory portion based on A51600-00B
1	00	2005-03-30	- Change R15 and R142 footprint to1210 for power dissipation - Correct U37 pin 11 to tide to +VREF_TMDS accroding to SiliconImage datasheet requirement - Add R104 for surge current protection

PCI-EXPRESS EDGE CONNECTOR





NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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Size C	Document Number 105-A62931-00	Rev 1
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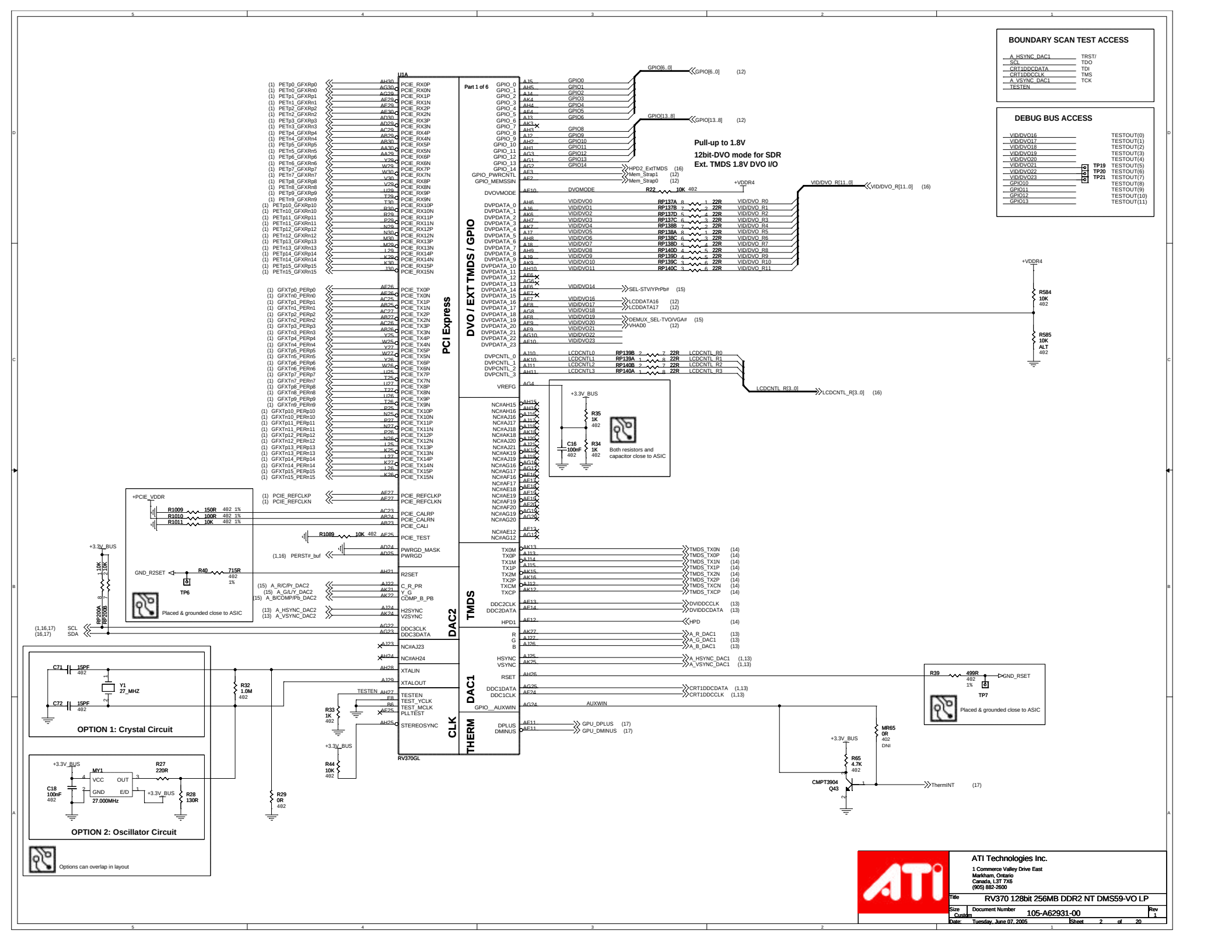
BOUNDARY SCAN TEST ACCESS
A_HSYNC_DAC1
SCL
CRT1DDCDATA
CRT1DDCCLK
A_VSYNC_DAC1
TESTEN
TRST/
TDO
TDI
TMS
TCK
DEBUG BUS ACCESS
VID/DVO16
VID/DVO17
VID/DVO18
VID/DVO19
VID/DVO20
VID/DVO21
VID/DVO22
VID/DVO23
GPIO10
GPIO11
GPIO12
GPIO13
TP19
TP20
TP21
TESTOUT(0)
TESTOUT(1)
TESTOUT(2)
TESTOUT(3)
TESTOUT(4)
TESTOUT(5)
TESTOUT(6)
TESTOUT(7)
TESTOUT(8)
TESTOUT(9)
TESTOUT(10)
TESTOUT(11)
U1A
Part 1 of 6
PCI Express
DVO / EXT TMDS / GPIO
DAC2
TMDS
DAC1
CLK
THERM
RV370GL
Pull-up to 1.8V
12bit-DVO mode for SDR
Ext. TMDS 1.8V DVO I/O
OPTION 1: Crystal Circuit
OPTION 2: Oscillator Circuit
Options can overlap in layout
Placed & grounded close to ASIC
Both resistors and capacitor close to ASIC
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Title
RV370 128bit 256MB DDR2 NT DMS59-VO LP
Size
Custom
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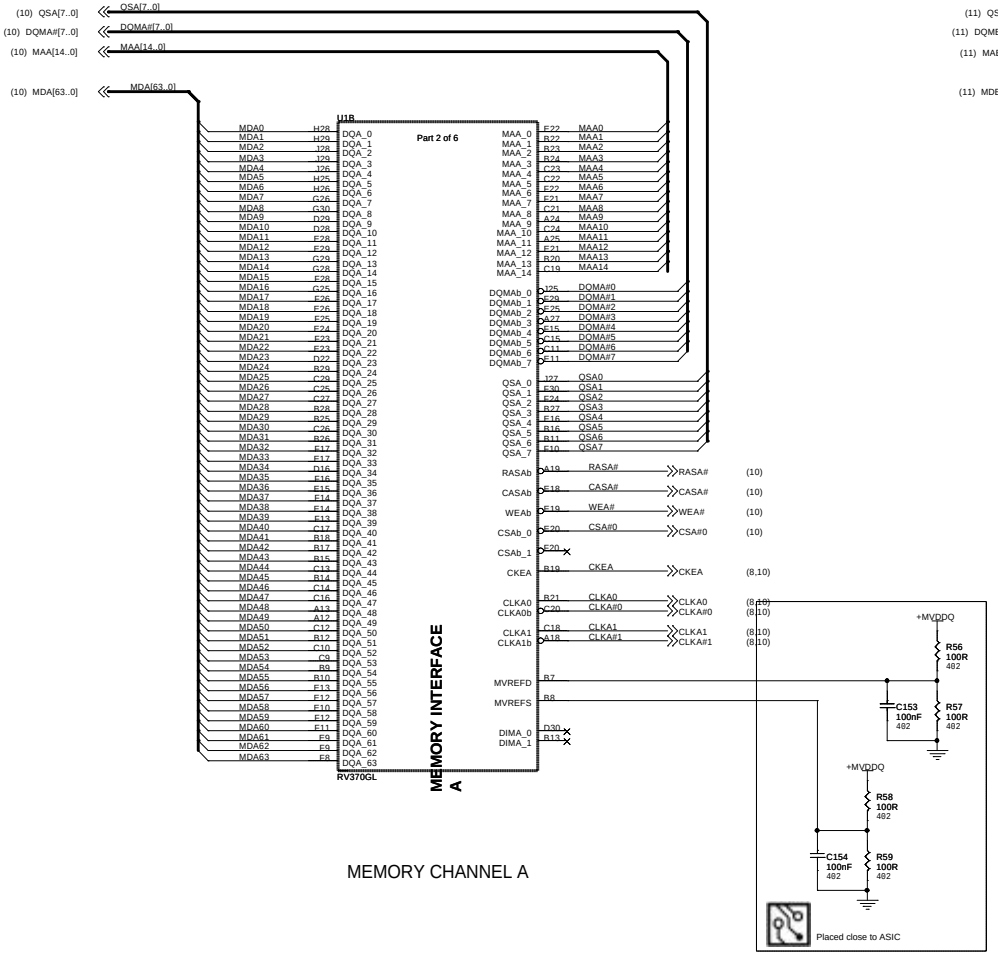
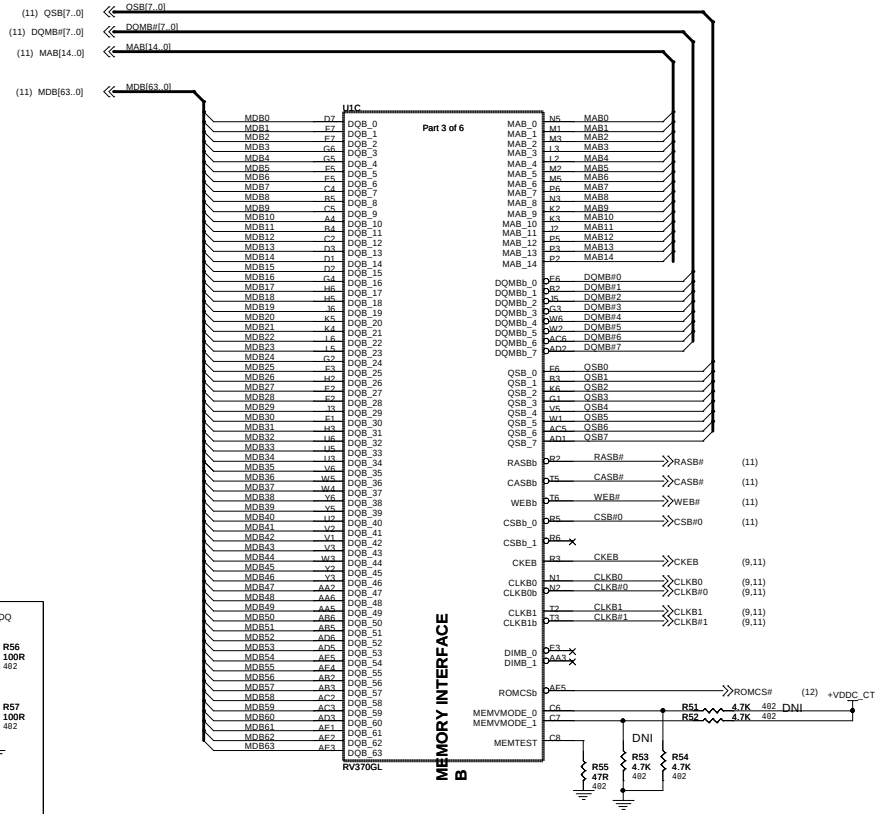
20



MEMORY CHANNEL A



MEMORY CHANNEL B

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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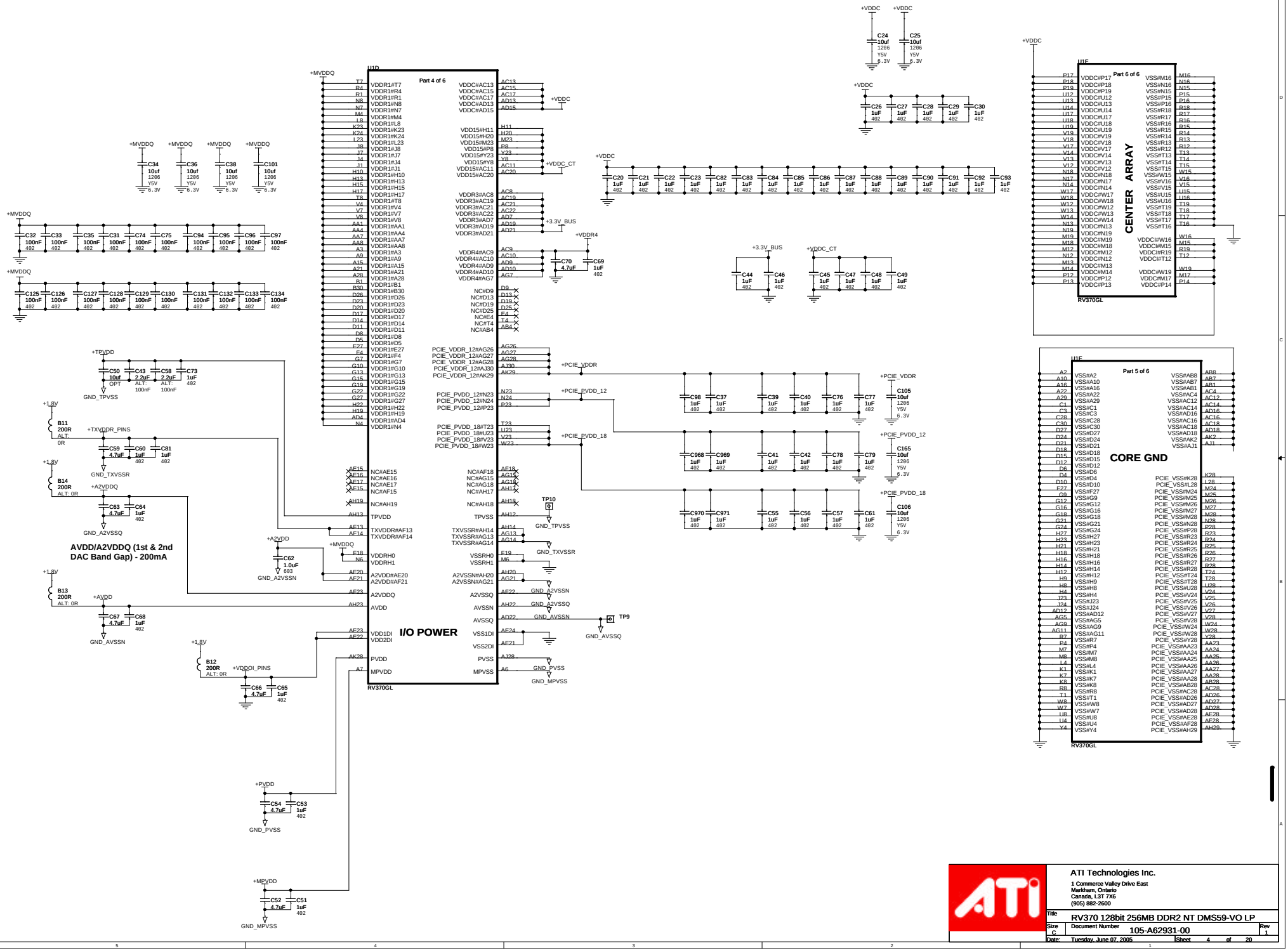
U1D
Part 4 of 6
RV370GL
I/O POWER
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
U1E
Part 5 of 6
CORE GND
RV370GL
U1E
Part 6 of 6
CENTER ARRAY
RV370GL
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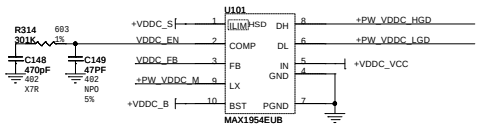
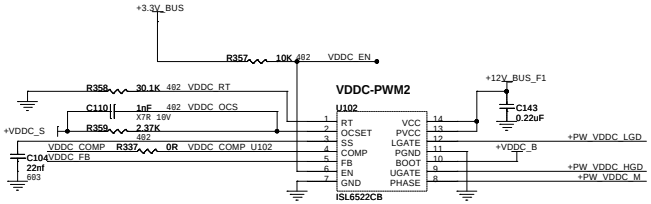
VDDC-PWM1



MAXIM MAX1954

VDDC-PWM2



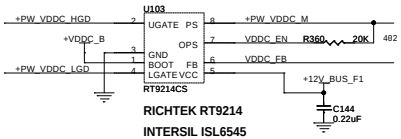
INTERSIL ISL6522

RICHTEK RT9232A

ANPEC APW7062A

ANPEC APW7062B

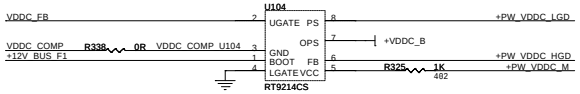
VDDC-PWM3



RICHTEK RT9214

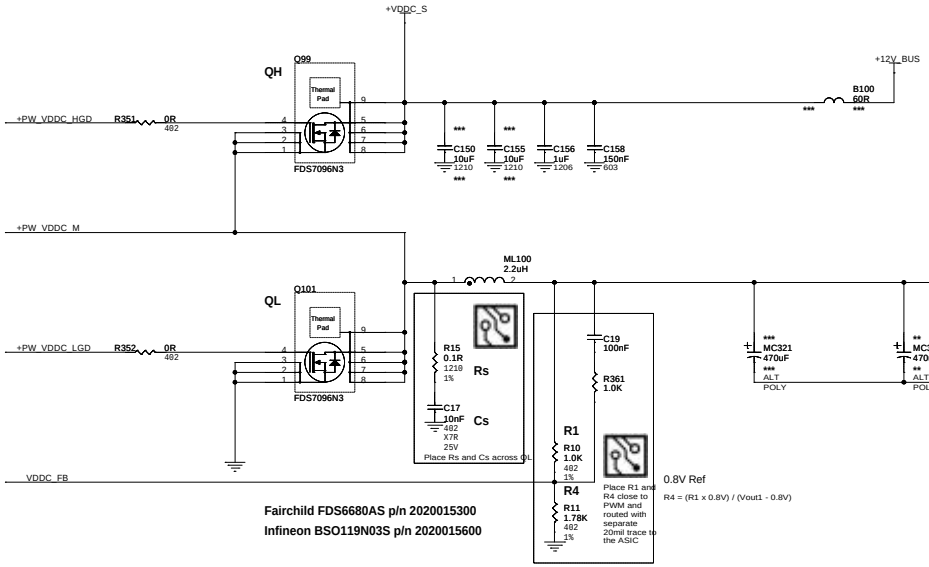
INTERSIL ISL6545

VDDC-PWM4



ANPEC APW7061A

VDDC_EN R324 0R 402 VDDC_COMP

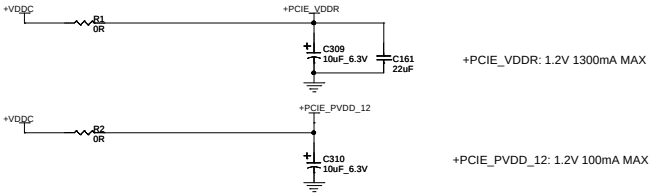


0.8V Ref

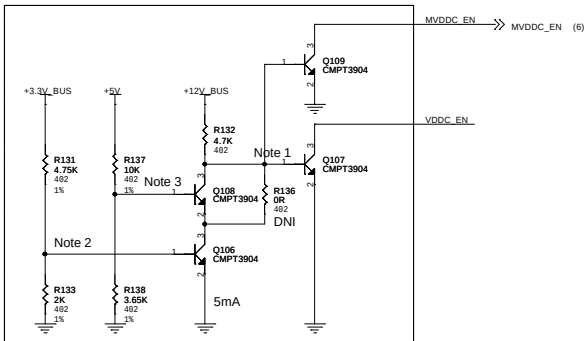
R4 = (R1 x 0.8V) / (Vout1 - 0.8V)

Fairchild FDS6680AS p/n 2020015300

Infineon BSO119N03S p/n 2020015600



POWER SEQUENCING



Power Sequence Circuit to ensure SMPS_EN is released after +12V and +3.3V are both in regulation.

Note 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Note 2 When +3.3V gets closed to regulation, one of the two conditions of releasing SMPS_EN is active

Target for 920mV when +3.3 at min regulation (worse case)

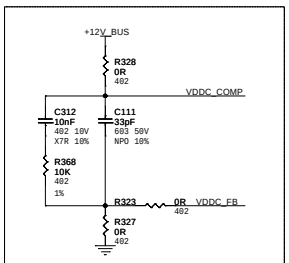
Typical trigger when +3.3V ramps above 2.2V (650mV)

Note 3 When +5V (derived from +12V) gets closed to regulation, one of the two conditions of releasing SMPS_EN is active

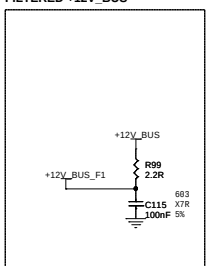
Target for 1.2V when +5 at min regulation (worse case)

Typical trigger when +5V ramps above 3.2V (850mV)

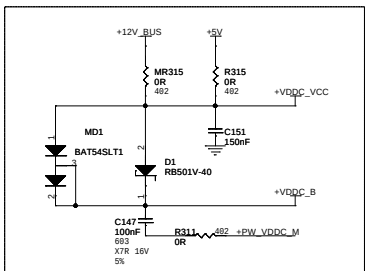
COMPENSATION CIRCUIT



FILTERED +12V_BUS



BOOT CIRCUIT



Regulator for VDDC (ASIC Core)

Vout = 1.2V ~ 1.3V

Part	Vout	R1	R2
0.8V Ref	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
	1.25V	1.00K 1% ATI P/N 3240100100	1.78K 1% ATI P/N 3240178100
	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100

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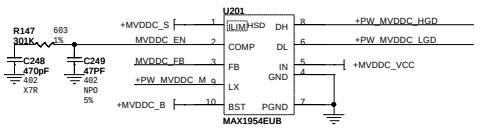
Regulator for MVDDC (Memory Core)

Vout = 2.5V ~ 2.85V

Part	Vout	R1	R2
0.8V Ref	1.9V	1K 3160100100G	715R 3160715000G
	2.0V	1K 3160100100G	649R
	2.1V	1.1K 3160110100	681R 3240681000G 603 681R 31606810000G 402
	2.55V	1K 3160100100G	453R 3160453000
	2.855V		

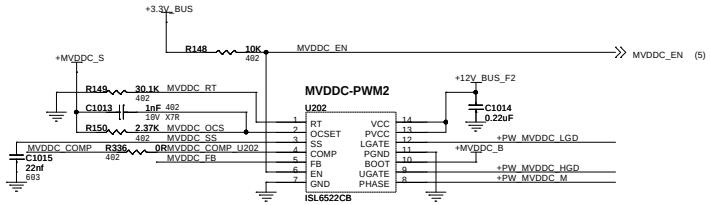
MVDDC-PWM1



MAXIM MAX1954

MAXIM MAX1954A

MVDDC-PWM2



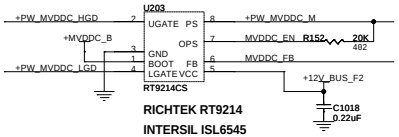
INTERSIL ISL6522

RICHTEK RT9232A

ANPEC APW7062A

ANPEC APW7062B

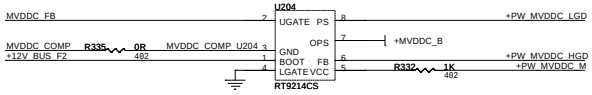
MVDDC-PWM3



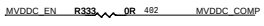
RICHTEK RT9214

INTERSIL ISL6545

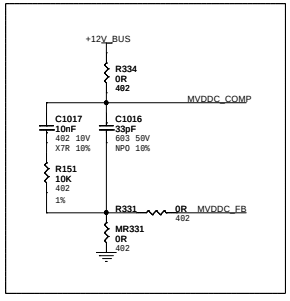
MVDDC-PWM4



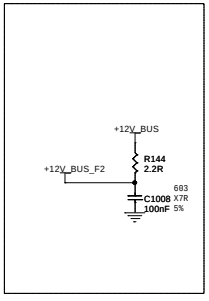
ANPEC APW7061A



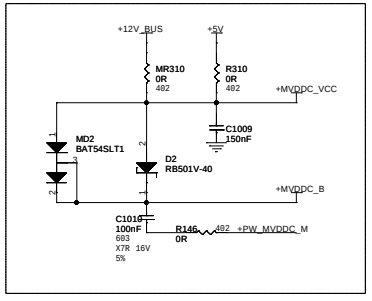
COMPENSATION CIRCUIT



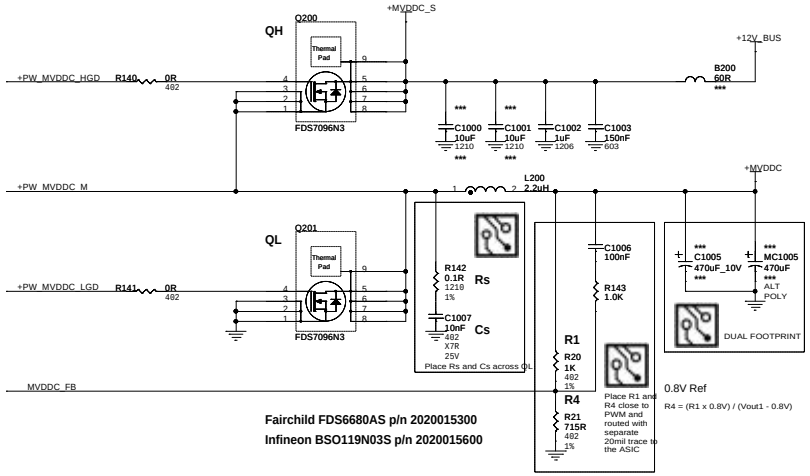
FILTERED +12V_BUS



BOOT CIRCUIT



QH / QL

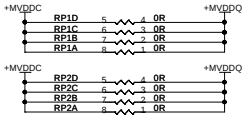


Fairchild FDS6680AS p/n 2020015300

Infineon BSO119N03S p/n 2020015600

0.8V Ref

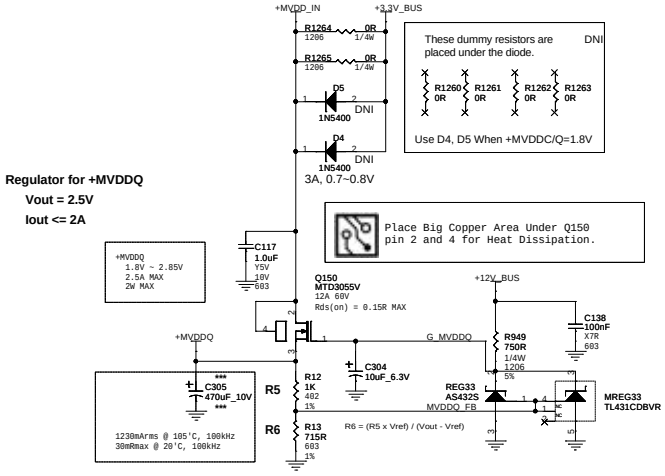
R4 = (R1 x 0.8V) / (Vout1 - 0.8V)



Regulator for +MVDDQ

Vout = 2.5V

Iout <= 2A



Regulator for +MVDDQ

Vout = 1.8V ~ 2.85V

Iout = ??A MAX

Voltage Req.	R5	R6	
3.34V	4.32K	2.55K	CHK
3.45V	4.32K	2.43K	CHK
2.85V			
2.55V	2.5V Ref.	22.1R 316022R100G	1.1K 3240110100G
2.5V	2.5V Ref.	0R 3150000000	DNI
2.1V	1.25V Ref.	681R 3160681000G	953R 3240953000
2.0V	1.25V Ref.	681R 3160681000G	1.1K 3240110100G
1.9V	1.25V Ref.	1K 3160100100G	715R 3160715000G
1.8V	1.25V Ref.	681R 3160681000G	1.5K 3230015200 CHK

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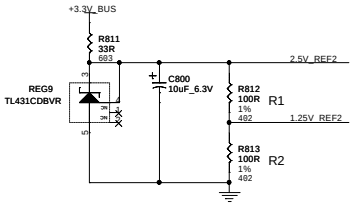
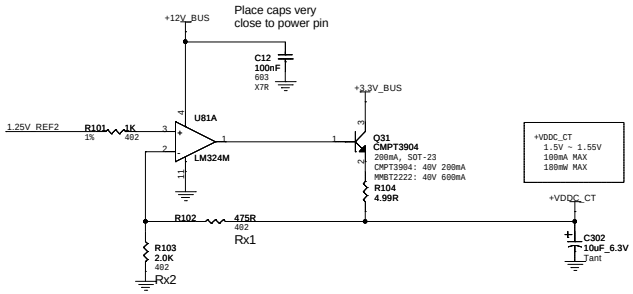
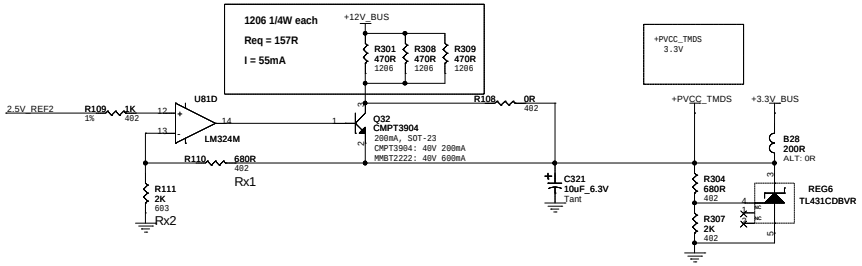


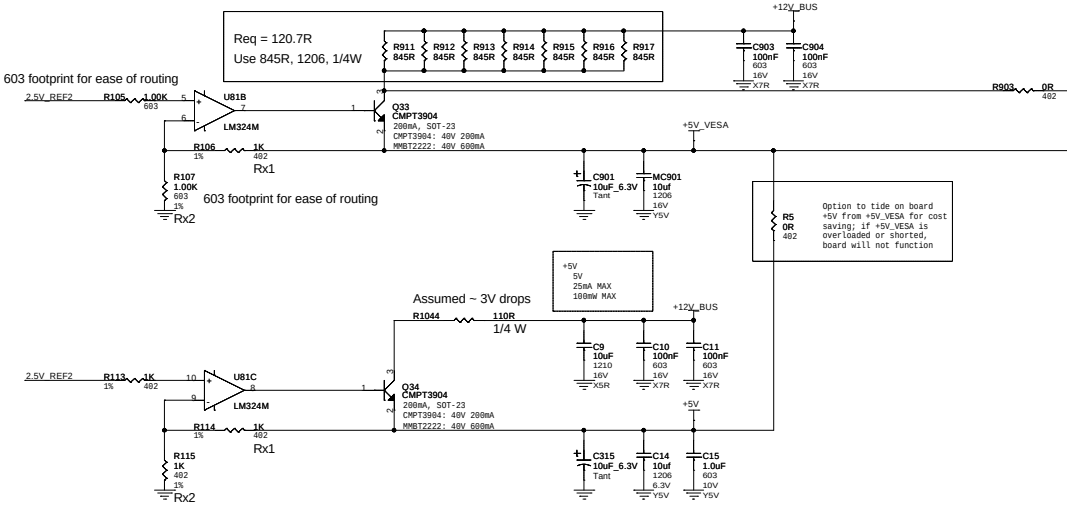
Voltage Req.	R1	R2
0.8V	150R P/N 3160150000 402	71.5R P/N 324075R500
1.25V	100R P/N 3160100000 402	100R P/N 3160100000 402
1.5V	100R P/N 3160100000 402	150R P/N 3160150000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

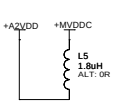
Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.55	475R (402, 1%) P/N 3160475000	2K (1%) P/N 31602001000 (402) P/N 3240200100 (603)
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240150100

Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100 603 P/N 3160107100 402	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.61V	221R (402, 1%) P/N 3160221000	4.99K (402, 1%) P/N 3160499100
2.5V	0R P/N 3230000000 603 P/N 3150000000 402	DNI

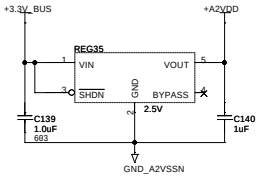




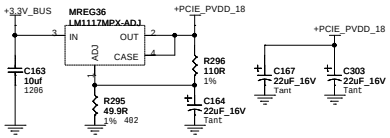




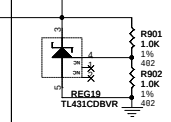
Alt. regulator for +A2VDD
Vout = 2.5V
Iout = 120mA MAX



Alt. Regulator for PCIE_PVDD_18
Vout = 1.82V
Iout = 500mA MAX



Alt regulator for +5V_VESA

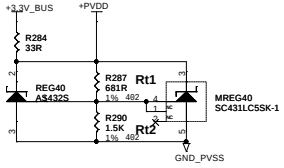


Normal +5V regulated operation
This circuit provide upto 55mA

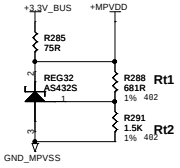
If Iload > 55mA, +5V will drop

If Vout is shorted
Current across each Rx is 12V/845R = 14.2mA
Power dissipated by each Rx is 14.2mA x 12V = 171mW
Each Rx are rated 250mW (1/4W)
Derating 250mW by 70% is 175mW (1/4W)

Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX

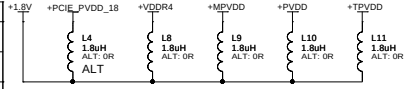


Alt regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX



	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100

+VDDR4: 100mA MAX
+MPVDD: 10mA MAX
+PVDD: 25mA MAX
+TPVDD: 50mA MAX



Rails derived from +1.8V
+AVDD: 10mA MAX
+A2VDDQ: 20mA MAX
+VDDOI_PINS: 20mA MAX
+TXVDDR_PINS: 20mA MAX

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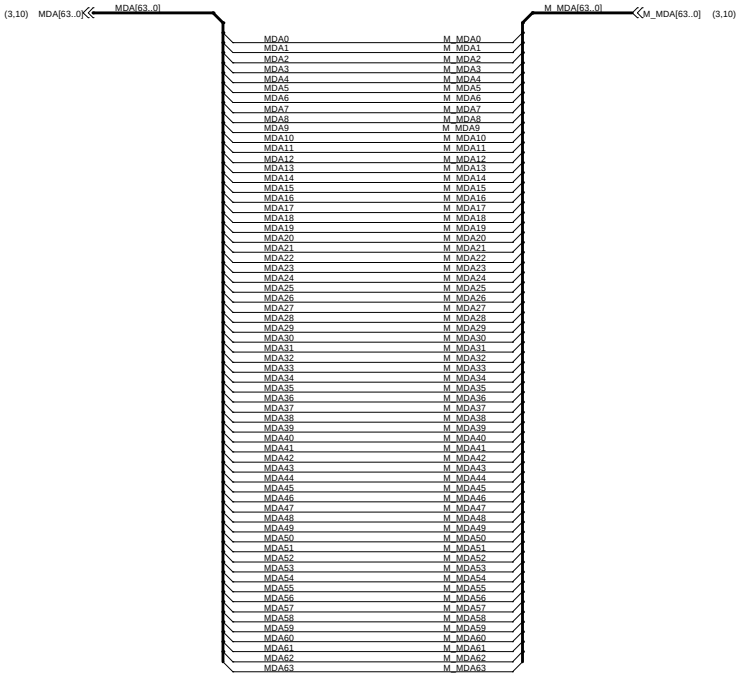

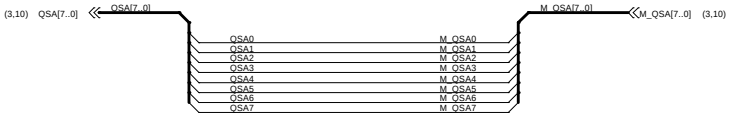

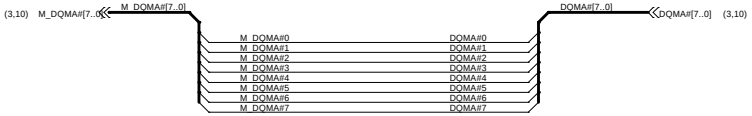

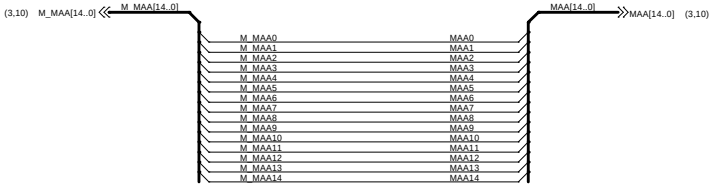

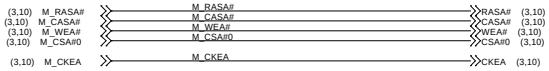

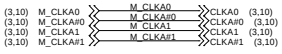

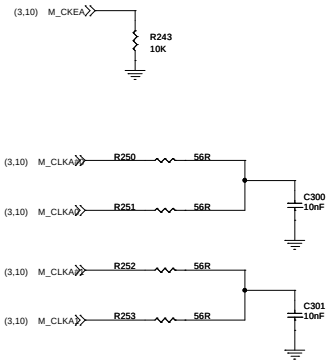

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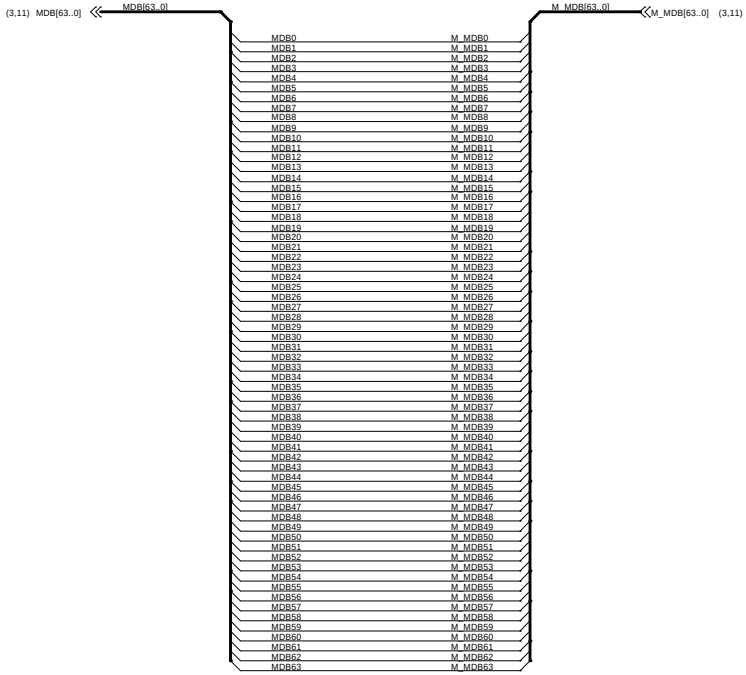

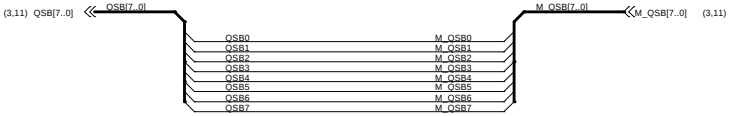

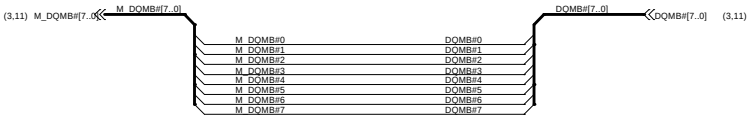

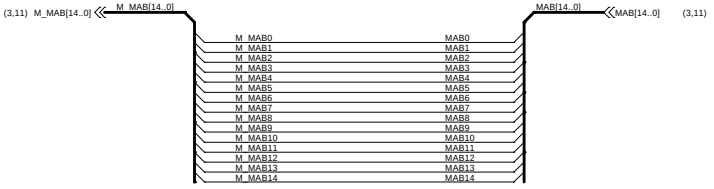

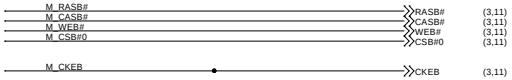

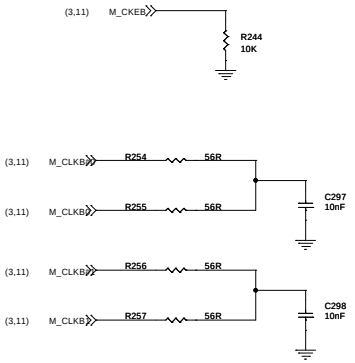

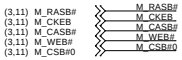

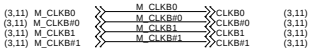

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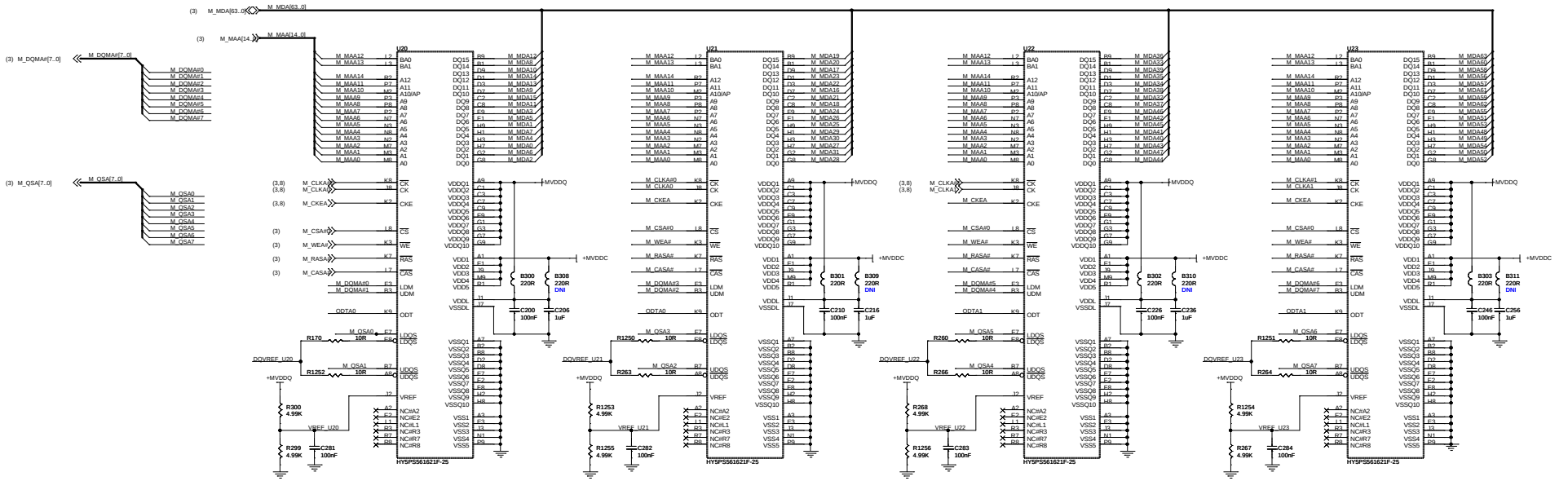

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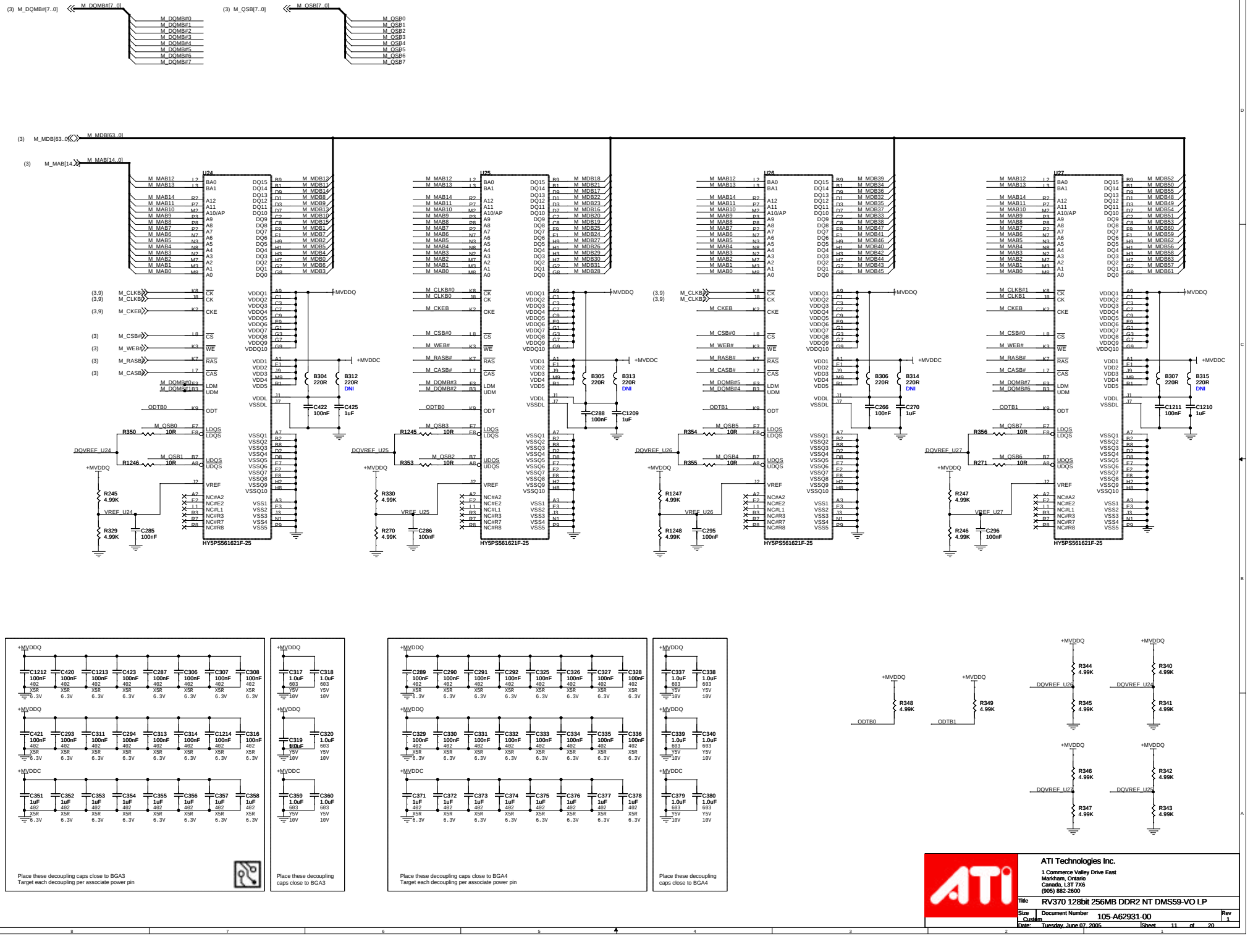
(3) M_DQMB#[7..0]
M_DQMB#[7..0]
M_DQMB#0
M_DQMB#1
M_DQMB#2
M_DQMB#3
M_DQMB#4
M_DQMB#5
M_DQMB#6
M_DQMB#7
(3) M_QSB[7..0]
M_QSB[7..0]
M_QSB0
M_QSB1
M_QSB2
M_QSB3
M_QSB4
M_QSB5
M_QSB6
M_QSB7
(3) M_MDB[63..0]
M_MDB[63..0]
(3) M_MAB[14..0]
M_MAB[14..0]
U24
U25
U26
U27
HY5PS561621F-25
+MVDDQ
+MVDDC
DQVREF_U24
DQVREF_U25
DQVREF_U26
DQVREF_U27
VREF_U24
VREF_U25
VREF_U26
VREF_U27
ODTB0
ODTB1
B304 220R
B312 220R DNI
B305 220R
B313 220R DNI
B306 220R
B314 220R DNI
B307 220R
B315 220R DNI
C422 100nF
C425 1uF
C288 100nF
C1209 1uF
C266 100nF
C270 1uF
C1211 100nF
C1210 1uF
R350 10R
R1246 10R
R1245 10R
R353 10R
R354 10R
R355 10R
R356 10R
R271 10R
R245 4.99K
R329 4.99K
R285 100nF
R330 4.99K
R270 4.99K
R286 100nF
R1247 4.99K
R1248 4.99K
R295 100nF
R247 4.99K
R246 4.99K
R296 100nF
R348 4.99K
R349 4.99K
R344 4.99K
R345 4.99K
R340 4.99K
R341 4.99K
R346 4.99K
R347 4.99K
R342 4.99K
R343 4.99K
Place these decoupling caps close to BGA3
Target each decoupling per associate power pin
Place these decoupling caps close to BGA3
Place these decoupling caps close to BGA4
Target each decoupling per associate power pin
Place these decoupling caps close to BGA4
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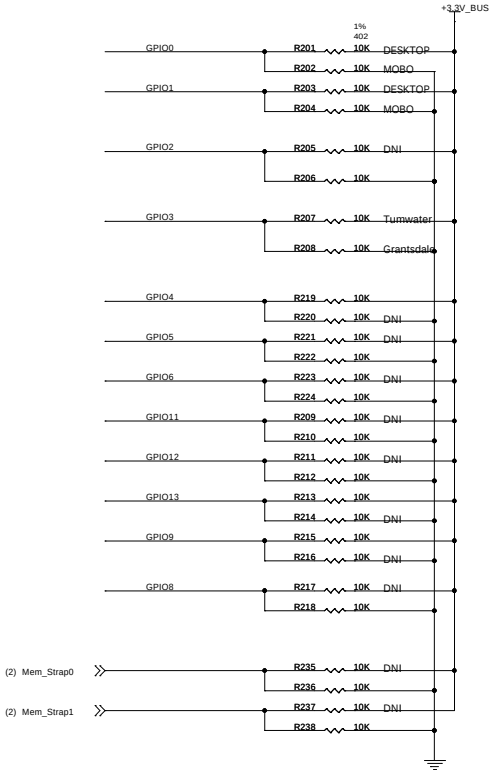
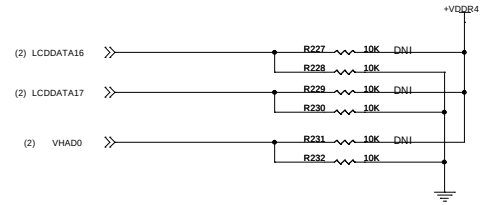
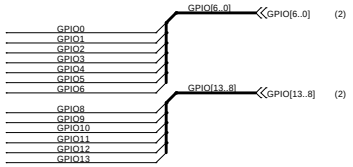
OPTION STRAPS





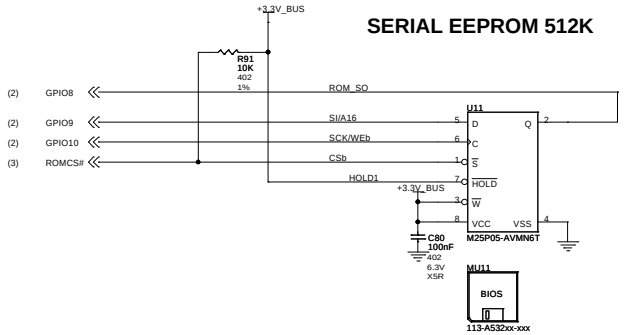


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K



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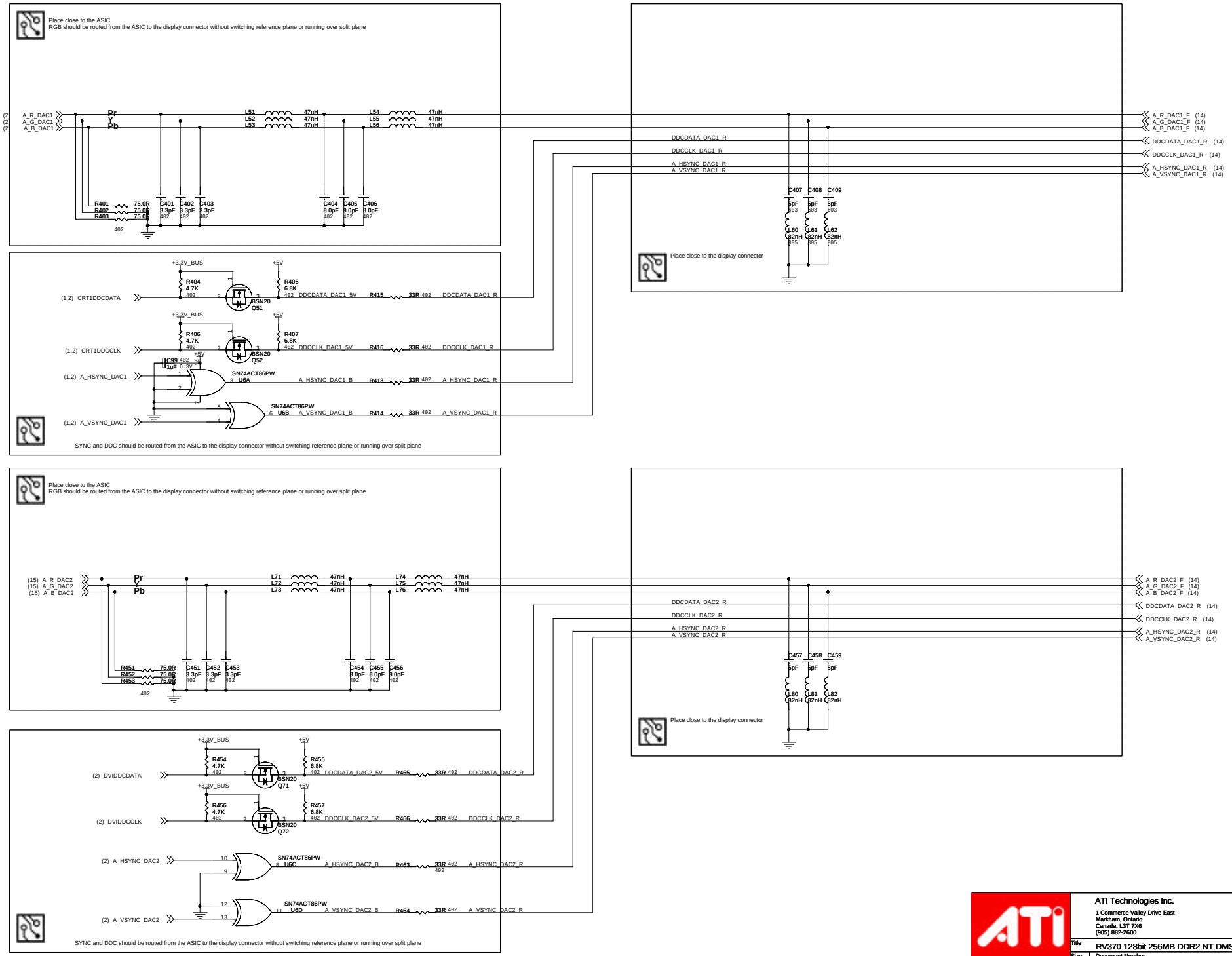
Place close to the ASIC
RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane
(2) A_R_DAC1
(2) A_G_DAC1
(2) A_B_DAC1
Pr
Y
Pb
L51 47nH
L52 47nH
L53 47nH
L54 47nH
L55 47nH
L56 47nH
R401 75.0R
R402 75.0R
R403 75.0R
C401 3.3pF
C402 3.3pF
C403 3.3pF
C404 8.0pF
C405 8.0pF
C406 8.0pF
A_R_DAC1_F (14)
A_G_DAC1_F (14)
A_B_DAC1_F (14)
DDCDATA_DAC1_R
DDCCLK_DAC1_R
A_HSYNC_DAC1_R
A_VSYNC_DAC1_R
DDCDATA_DAC1_R (14)
DDCCLK_DAC1_R (14)
A_HSYNC_DAC1_R (14)
A_VSYNC_DAC1_R (14)
C407 5pF
C408 5pF
C409 5pF
L60 82nH
L61 82nH
L62 82nH
Place close to the display connector
+3.3V_BUS
+5V
R404 4.7K
R405 6.8K
(1,2) CRT1DDCDATA
BSN20 Q51
DDCDATA_DAC1_5V
R415 33R
R406 4.7K
R407 6.8K
(1,2) CRT1DDCCLK
BSN20 Q52
DDCCLK_DAC1_5V
R416 33R
C99 1uF 6.3V
(1,2) A_HSYNC_DAC1
SN74ACT86PW U6A
A_HSYNC_DAC1_B
R413 33R
(1,2) A_VSYNC_DAC1
SN74ACT86PW U6B
A_VSYNC_DAC1_B
R414 33R
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane
Place close to the ASIC
RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane
(15) A_R_DAC2
(15) A_G_DAC2
(15) A_B_DAC2
Pr
Y
Pb
L71 47nH
L72 47nH
L73 47nH
L74 47nH
L75 47nH
L76 47nH
R451 75.0R
R452 75.0R
R453 75.0R
C451 3.3pF
C452 3.3pF
C453 3.3pF
C454 8.0pF
C455 8.0pF
C456 8.0pF
A_R_DAC2_F (14)
A_G_DAC2_F (14)
A_B_DAC2_F (14)
DDCDATA_DAC2_R
DDCCLK_DAC2_R
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R
DDCDATA_DAC2_R (14)
DDCCLK_DAC2_R (14)
A_HSYNC_DAC2_R (14)
A_VSYNC_DAC2_R (14)
C457 5pF
C458 5pF
C459 5pF
L80 82nH
L81 82nH
L82 82nH
Place close to the display connector
+3.3V_BUS
+5V
R454 4.7K
R455 6.8K
(2) DVIDDCDATA
BSN20 Q71
DDCDATA_DAC2_5V
R465 33R
R456 4.7K
R457 6.8K
(2) DVIDDCCLK
BSN20 Q72
DDCCLK_DAC2_5V
R466 33R
(2) A_HSYNC_DAC2
SN74ACT86PW U6C
A_HSYNC_DAC2_B
R463 33R
(2) A_VSYNC_DAC2
SN74ACT86PW U6D
A_VSYNC_DAC2_B
R464 33R
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane
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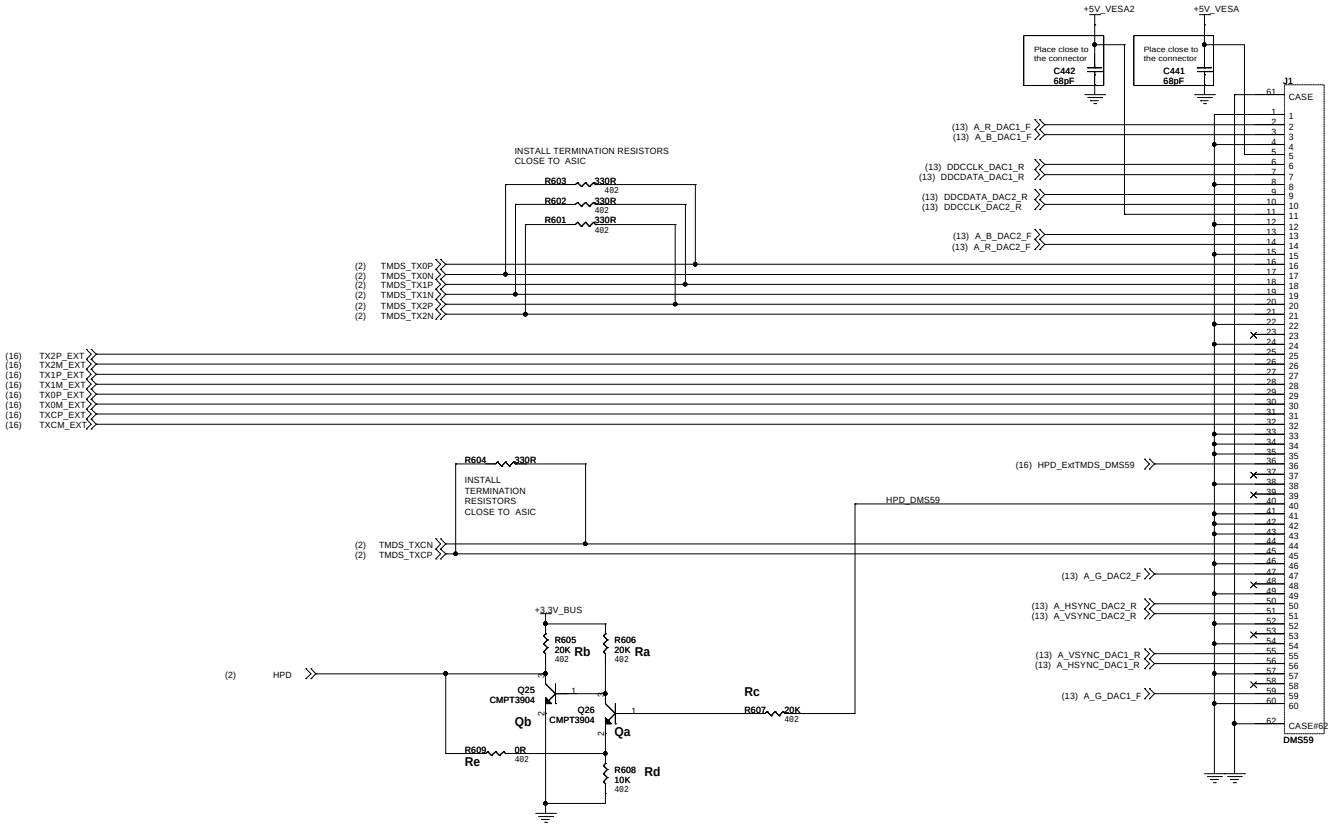
VESA Multi-Display Interface DMS-59 Connector



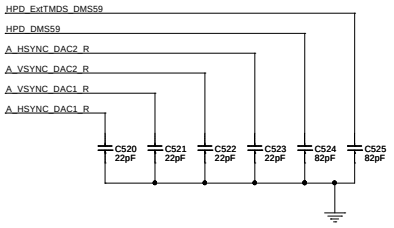
Connector 1	
Signals	Mapping
VGA:	DAC1
DVI:	External TMDS
HPD:	External TMDS HPD
DDC:	CRT1 DDC
5V:	+5V_VESA

Connector 2	
Signals	Mapping
VGA:	DAC2 (TVDAC)
DVI:	Internal/Integrated TMDS
HPD:	Internal/Integrated TMDS HPD
DDC:	DVI DDC
5V:	+5V_VESA2

STUFFING OPTIONS

Hot-Plug Detect Circuit	MUST INSTALL	MUST NOT INSTALL
Type A	Ra, Rb, Rc, Rd=0R, Qa, Qb	Re
Type B	Ra=0R, Rc, Rd=10K, Re, Qa	Rb, Qb

	HPD_ExtTMDS_DVI	HPD_ExtTMDS Type A	HPD_ExtTMDS Type B
NC	High Z	0 (0V)	0 (0V)
Connected	5V	1 (3.3V)	1 (3.3V)



EMI Capacitors, place close to connector

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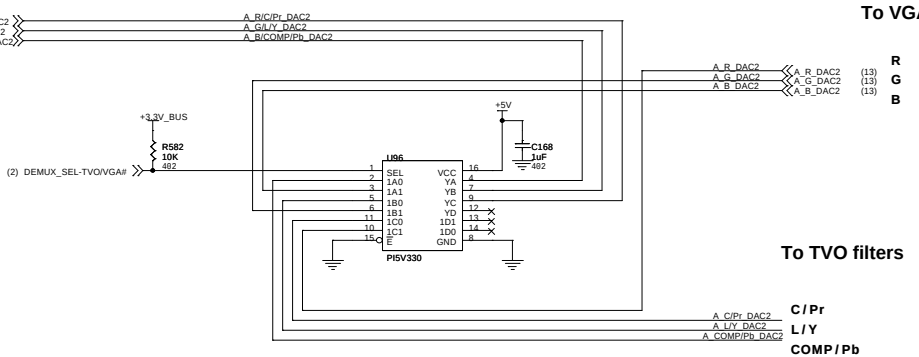
From DAC2

R / C / Pr
G / L / Y
B / COMP / Pb

DAC2 DeMux



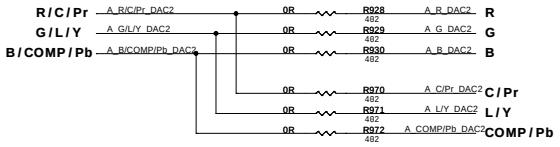
To VGA Filters

A_R_DAC2 (13) R
A_G_DAC2 (13) G
A_B_DAC2 (13) B

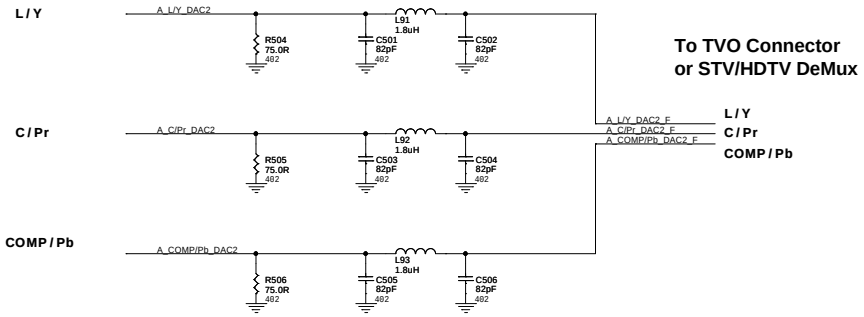
To TVO filters

A_C/Pr_DAC2 C / Pr
A_L/Y_DAC2 L / Y
A_COMP/Pb_DAC2 COMP / Pb

DAC2 DeMux BYPASS



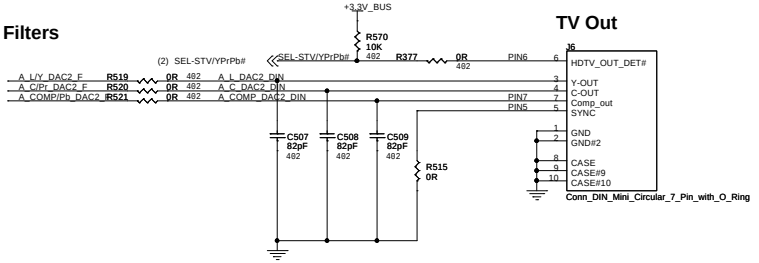
From VGA DeMux



To TVO Connector or STV/HDTV DeMux

From TVO Filters

L / Y
C / Pr
COMP / Pb



TV Out

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500
- 4-pin Svideo MiniDIN P/N 6070001000

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Please this resistor pack closed to the TMDS chip to avoid stub when it's not populated

LCDCNTL_R[3..0]

LCDCNTL_R0	RP600A	1	8	10K
LCDCNTL_R1	RP600B	2	7	10K
LCDCNTL_R2	RP600C	3	6	10K
LCDCNTL_R3	RP600D	4	5	10K

+3.3V_BUS

MUST BE INSTALLED IF NO TMDS IS INSTALLED

12bit, Dual Edge DVO

Sil170B

U37

(2) VID/DVO_R[11..0] — VID/DVO_R[11..0]

VID/DVO_R0 18 D0
VID/DVO_R1 17 D1
VID/DVO_R2 16 D2
VID/DVO_R3 15 D3
VID/DVO_R4 14 D4
VID/DVO_R5 13 D5
VID/DVO_R6 10 D6
VID/DVO_R7 9 D7
VID/DVO_R8 8 D8
VID/DVO_R9 7 D9
VID/DVO_R10 6 D10
VID/DVO_R11 5 D11

TX0- 35 TX0M_EXT
TX0+ 36 TX0P_EXT
TX1- 38 TX1M_EXT
TX1+ 39 TX1P_EXT
TX2- 41 TX2M_EXT
TX2+ 42 TX2P_EXT
TXC- 32 TXCM_EXT
TXC+ 33 TXCP_EXT

TXCP_EXT (14)
TXCM_EXT (14)
TX2P_EXT (14)
TX2M_EXT (14)
TX1P_EXT (14)
TX1M_EXT (14)
TX0P_EXT (14)
TX0M_EXT (14)

R1240 301R C481 100nF
R1241 301R C482 100nF
R1242 301R C483 100nF
R1243 301R C484 100nF

Use 130R p/n 3160130000G

+AVCC_TMDS

AVCC 34 AVCC#40 40
AGND 37 AGND#43 43

C460 1nF 402
C461 1uF 402 6.3V X5R
C462 1uF 402 6.3V X5R
C463 1nF 402
C464 1uF 402 6.3V X5R
C465 1uF 402 6.3V X5R
C466 10uf 1206 Y5V 6.3V

+3.3V_BUS — R24 200R ALT: 0R

(2) LCDCNTL_R[3..0] — LCDCNTL_R[3..0]

LCDCNTL_R1 20 HSYNC
LCDCNTL_R0 21 VSYNC
LCDCNTL_R2 19 DE
LCDCNTL_R3 12 IDICK+
11 IDICK-
48 MSEN
44 EDGE/HTPLG
25 ISEL/RST#
26 SDA
27 SCL
24 CTL3/A2

+3.3V_BUS
+VREF_TMDS
R306 5.1K 402 MSEN_TMDS
R322 0R 402
MR322 0R 402 HPD_ExtTMDS
(2) HPD2_ExtTMDS
(1,2) PERST#_buf — I2C_RST
(2,17) SDA — SDA
(1,2,17) SCL — SCL

DDC3 from GPU

VREF 2 — +VREF_TMDS
EXT_SWING 30 — EXT_SWING

R_Ext-Swing
R305 390R

PVCC1 28 — +PVCC1_TMDS
PVCC2 46 — +PVCC2_TMDS
PGND 29
PGND#45 45
VCC#22 22
VCC 3

+3.3V_BUS

C472 1nF 402
C473 1uF 402 6.3V X5R
C474 1nF 402
C475 1uF 402 6.3V X5R
C476 10uf 1206 Y5V 6.3V
C477 10uf 1206 Y5V 6.3V

GND 4
GND#23 23
TH_GND 49
GND#1 1
AGND#31 31
PD# 47

Sil1162

+PVCC_TMDS

+PVCC1_TMDS
C469 1nF 402
C470 1uF 402 6.3V X5R
C485 10uf 1206 Y5V 6.3V

B22 200R ALT: 0R

+PVCC2_TMDS
B23 200R ALT: 0R
C479 1nF 402
C480 1uF 402 6.3V X5R
C486 10uf 1206 Y5V 6.3V

+PVCC2_TMDS Filters

+3.3V_BUS

R317 20K Rb 402
R318 20K Ra 402

HPD_ExtTMDS

Q29 CMPT3904
Q30 CMPT3904
Qb
Qa
Rc
R316 20K 402 — HPD_ExtTMDS_DMS59 (14)
R326 0R 402 Re
R321 10K 402 Rd

Req = 120.8R
Use 845R, 1206, 1/4W

+12V_BUS

R921 845R
R922 845R
R923 845R
R924 845R
R925 845R
R953 845R
R954 845R

Option to tide on board +5V_VESA2 from +5V_VESA for cost saving; if +5V_VESA is overloaded or shorted, +5V_VESA2 will followed

+5V_VESA — R6 0R 402 — +5V_VESA2

REG20 TL431CDBVR
R918 1.0K 1% 402
R919 1.0K 1% 402

Multi-footprint
C912 10uF_6.3V
MC912 4.7uF

Normal +5V regulated operation
This circuit provide upto 55mA

If Iload > 55mA, +5V will drop

If Vout is shorted
Current across each Rx is 12V/845R = 14.2mA
Power dissipated by each Rx is 14.2mA x 12V = 171mW
Each Rx are rated 250mW (1/4W)
Derating 250mW by 70% is 175mW (1/4W)

+VDDR4

C467 100nF 402 6.3V X5R
R302 1.0K 402 1%
+VREF_TMDS
C468 100nF 402 6.3V X5R
R303 1.0K 402 1%

STUFFING OPTIONS

EXT TMDS TX TO BE USED	MUST INSTALL	MUST NOT INSTALL	CAN BE REMOVED
Sil1162	R_Ext-Swing = 523R		

STUFFING OPTIONS

Hot-Plug Detect Circuit	MUST INSTALL	MUST NOT INSTALL
Type A	Ra, Rb, Rc, Rd=0R, Qa, Qb	Re
Type B	Ra=0R, Rc, Rd=10K, Re, Qa	Rb, Qb

	HPD_ExtTMDS_DVI	HPD_ExtTMDS Type A	HPD_ExtTMDS Type B
NC	High Z	0 (0V)	0 (0V)
Connected	5V	1 (3.3V)	1 (3.3V)

NOTE:
1 - Other components are to be installed.
2 - Components marked as DNI should not be installed. They should only be installed if default board settings are to be changed in which case other components may have to be adjusted accordingly.

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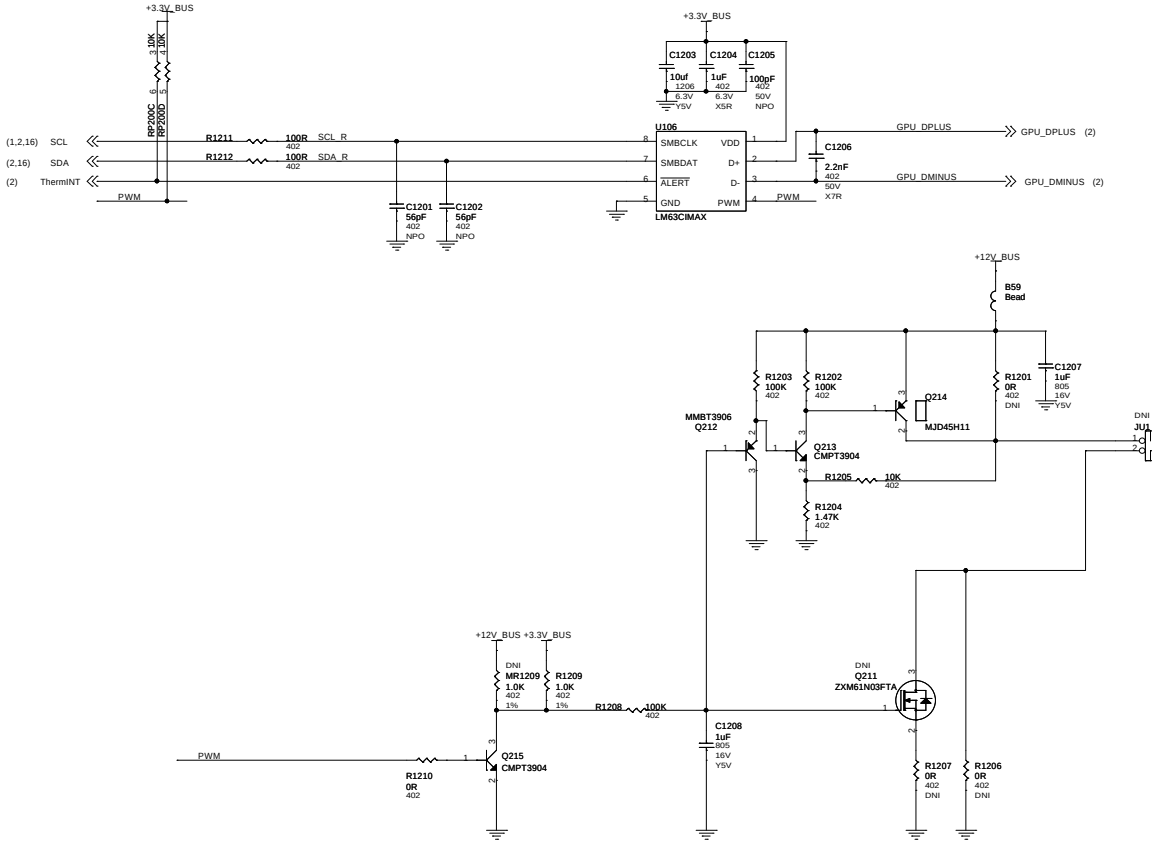

H101 heatsink 7120005800
H100 HEATSINK 7120005100
Spring push-pin
MH101 HEATSINK 7120002700
MH100 HEATSINK 7120008000
ITW push-pin

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DVI/VGA SCREWS

ASSY1
SCREW
SCREW

ASSY2
SCREW
SCREW

Bracket Screws

ASSY10
SCREW
PAN_HEAD

MISC. BOARD PARTS

ASSY3
BLANK LABEL
1.5W_X_0.50H

ASSY4
LABEL
2"_X_0.25"

ASSY5
LABEL
0.75"_X_0.25"

ASSY6
LABEL
STATIC_AWARNESS_LABEL

ASSY7
ANTISTATIC BAG
6_X_11

ASSY_PCB1
ATI LOGO LABEL
ATI_LOGO_LABEL
9110054500

MT1
MT_Hole_0.136_in.

LP brackets

BKT1
BRACKET
BRACKET, LP, NO TABS, DUAL DVI
80200326B0

BKT2
BRACKET
BRACKET, LP, TOP TAB, DIN, DUAL DVI
80200327F0

ATX brackets

BKT3
BRACKET
DUAL, NO TABS, Slim VGA, DIN, DVI
80200321F0

BKT4
BRACKET
TOP TAB (LP), DIN, Dual DVI
80200330A0

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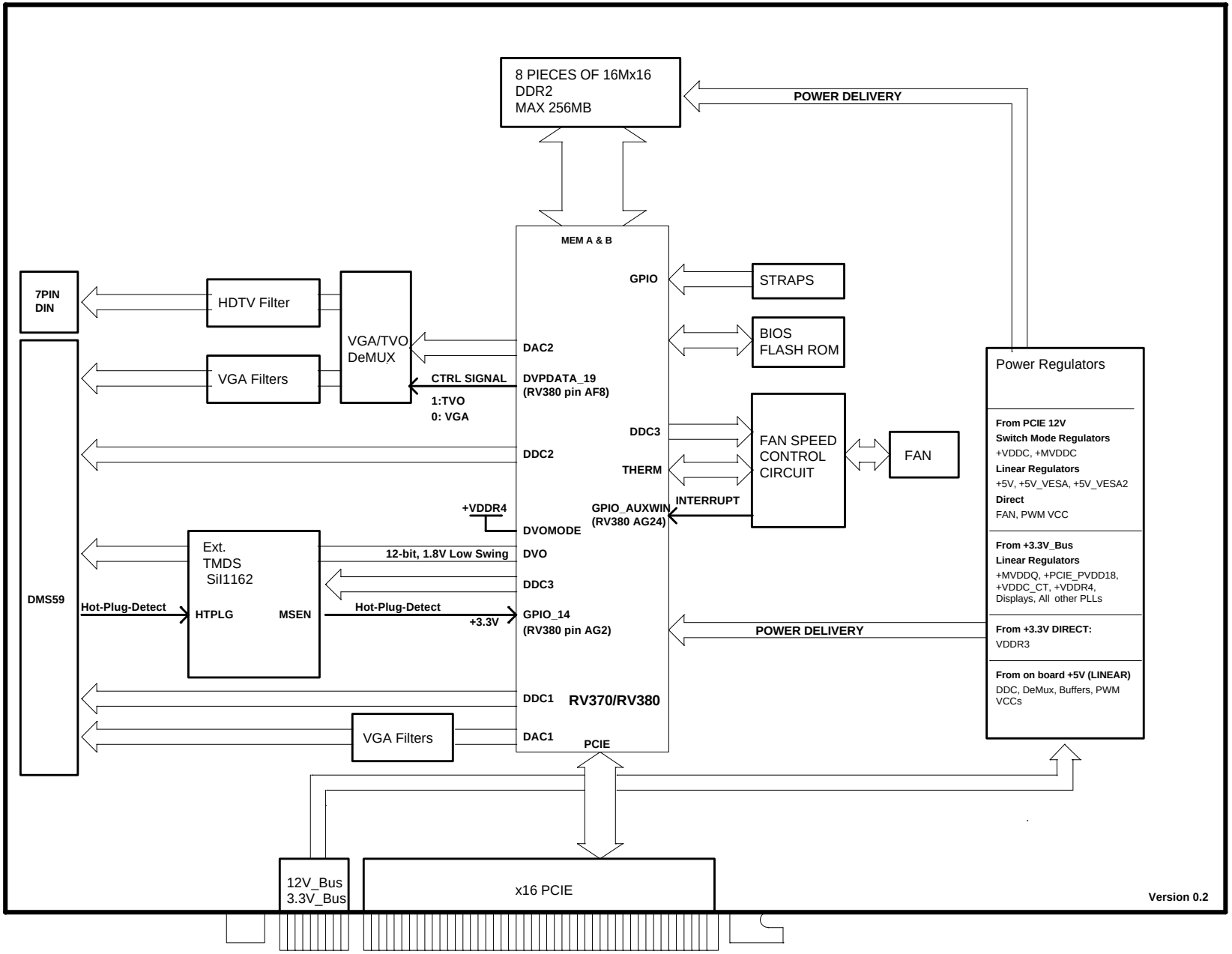

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