

A

B

C

D

E

F

A

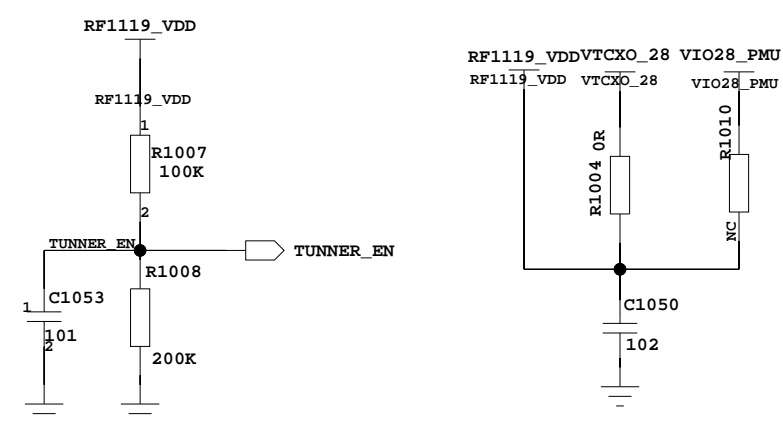
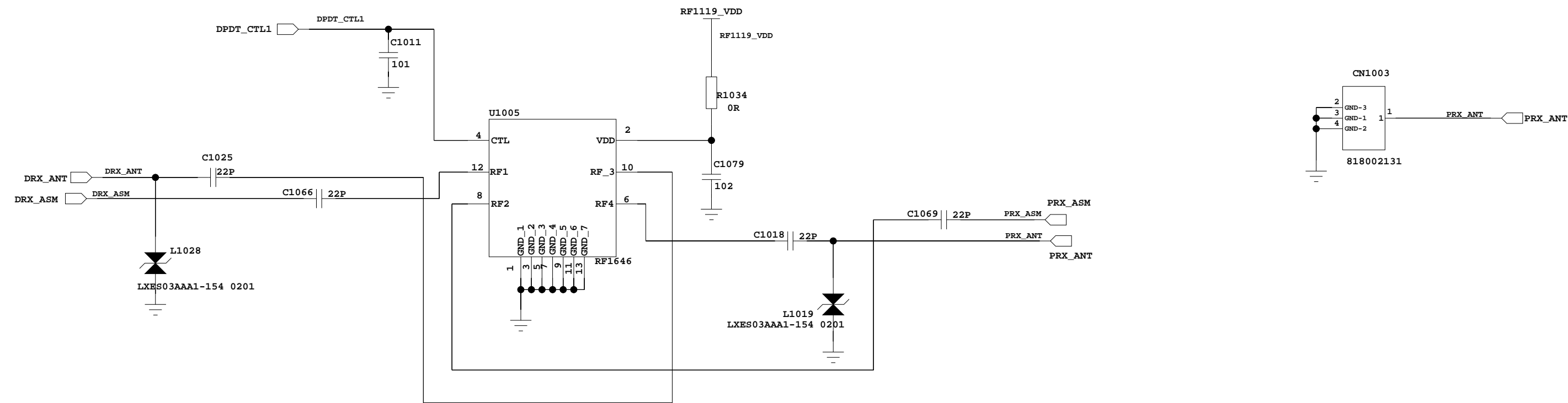
B

C

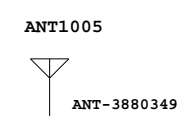
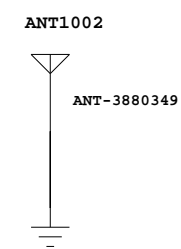
D

E

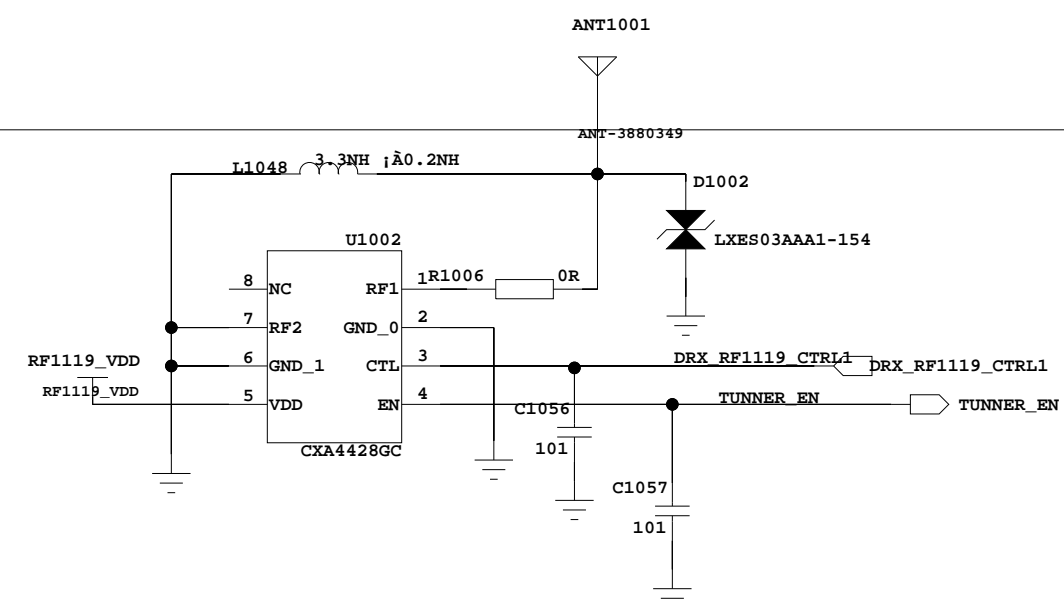
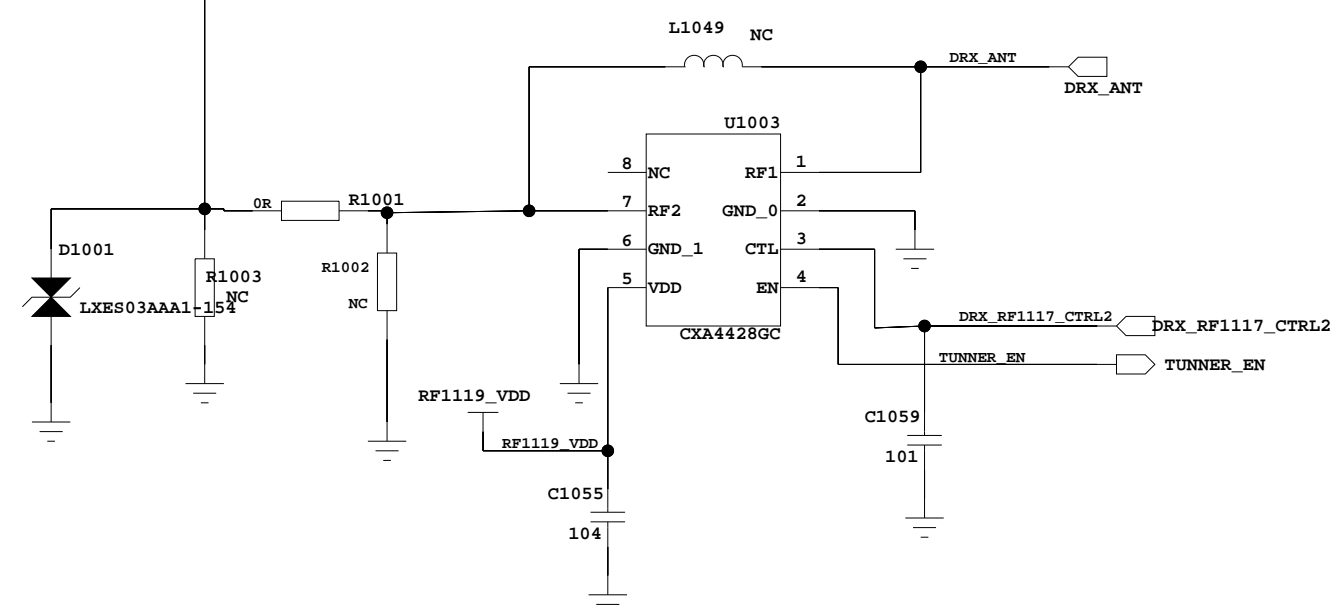
F

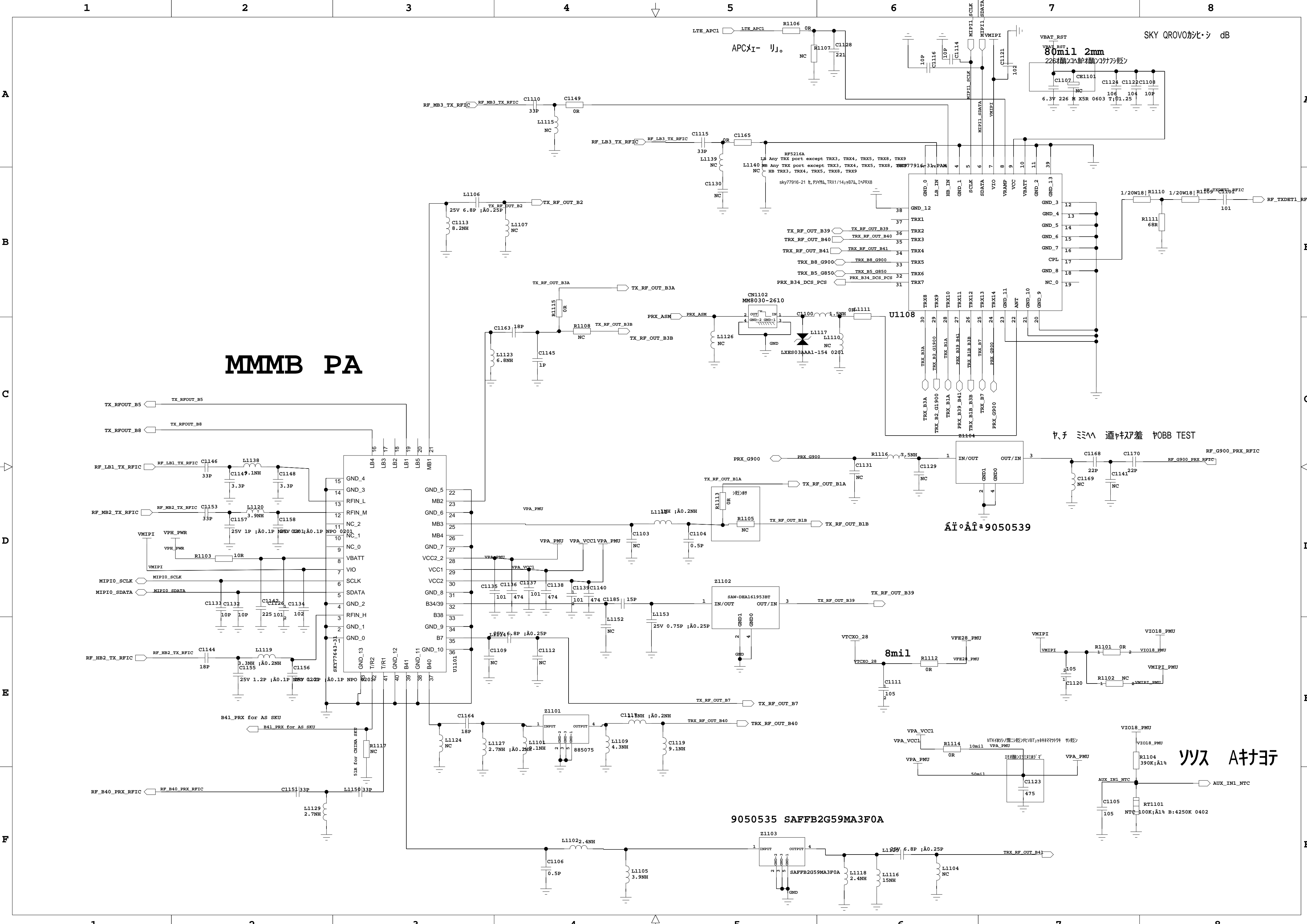


ANT_DRX



ANT-3880349





MMMB PA

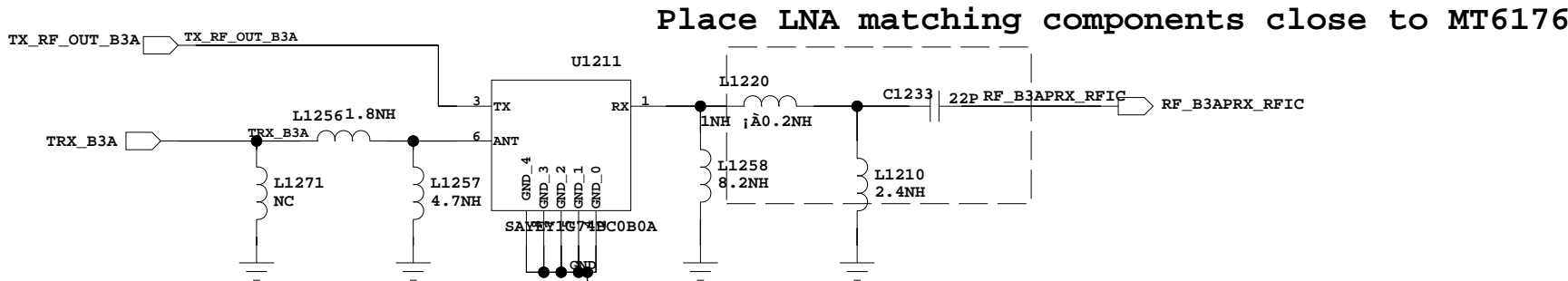
9050539

9050535 SAFFB2G59MA3F0A

ソス Aキナヲ

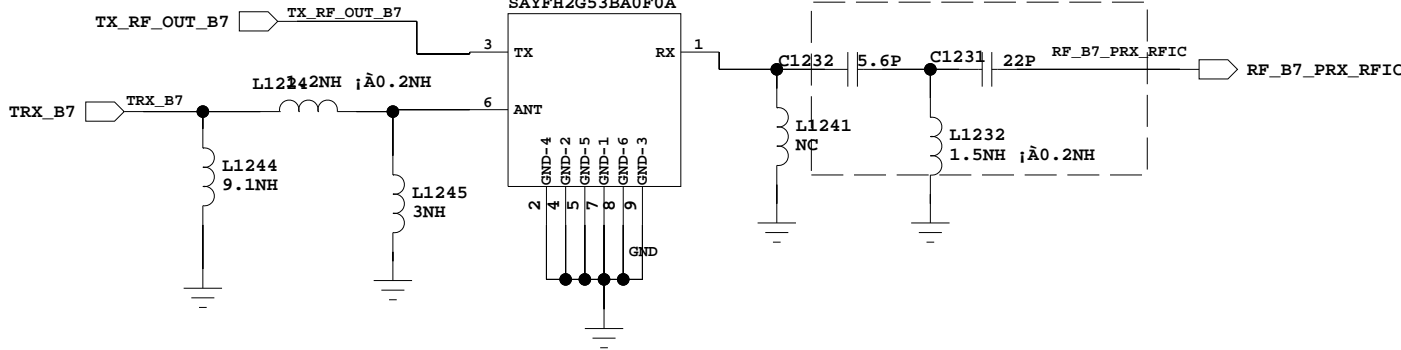
A

B3A TRX



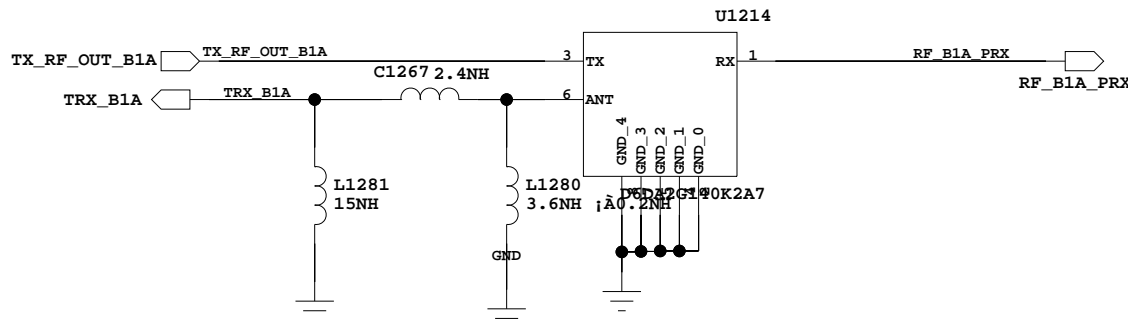
Place LNA matching components close to MT6177

B7 TRX



B

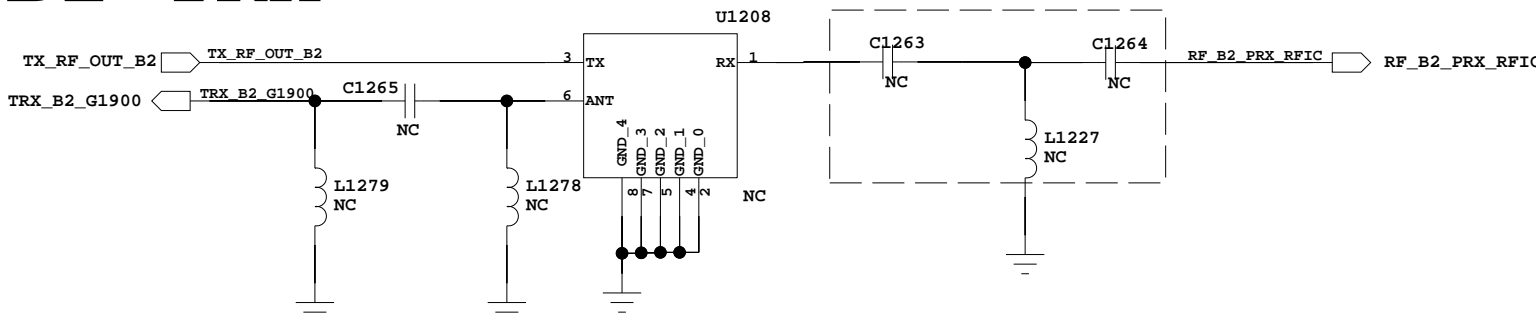
B1A TRX



C

B2 TRX

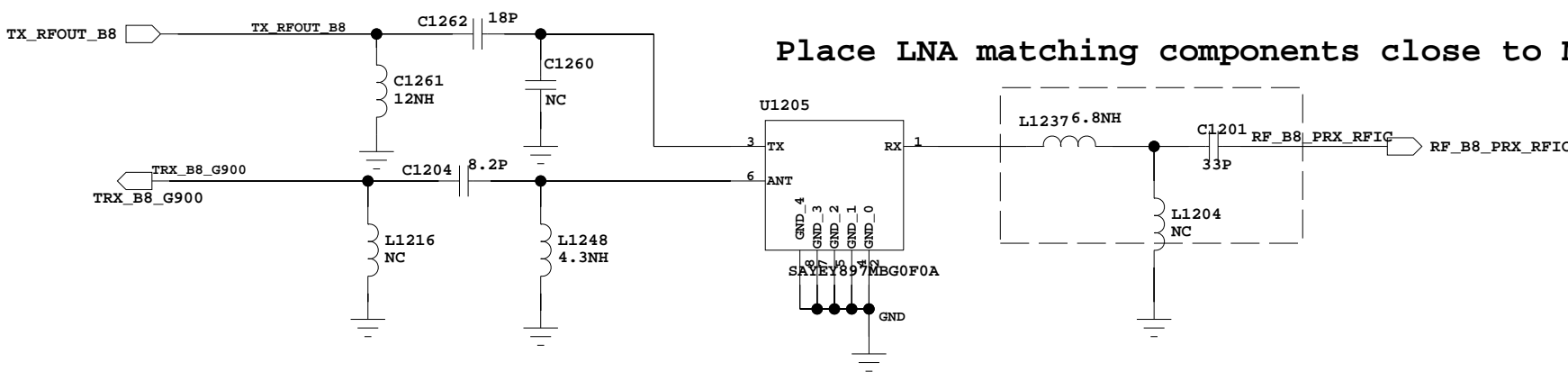
Place LNA matching components close to MT6177



D

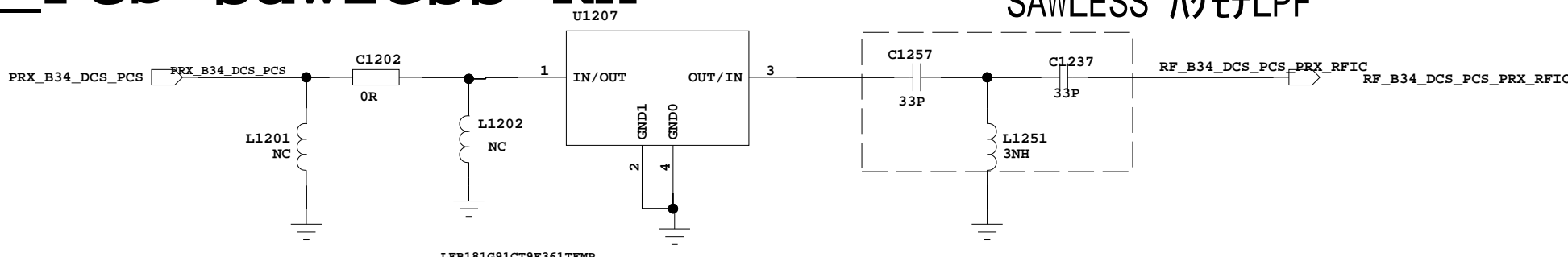
B8 TRX

Place LNA matching components close to MT6177



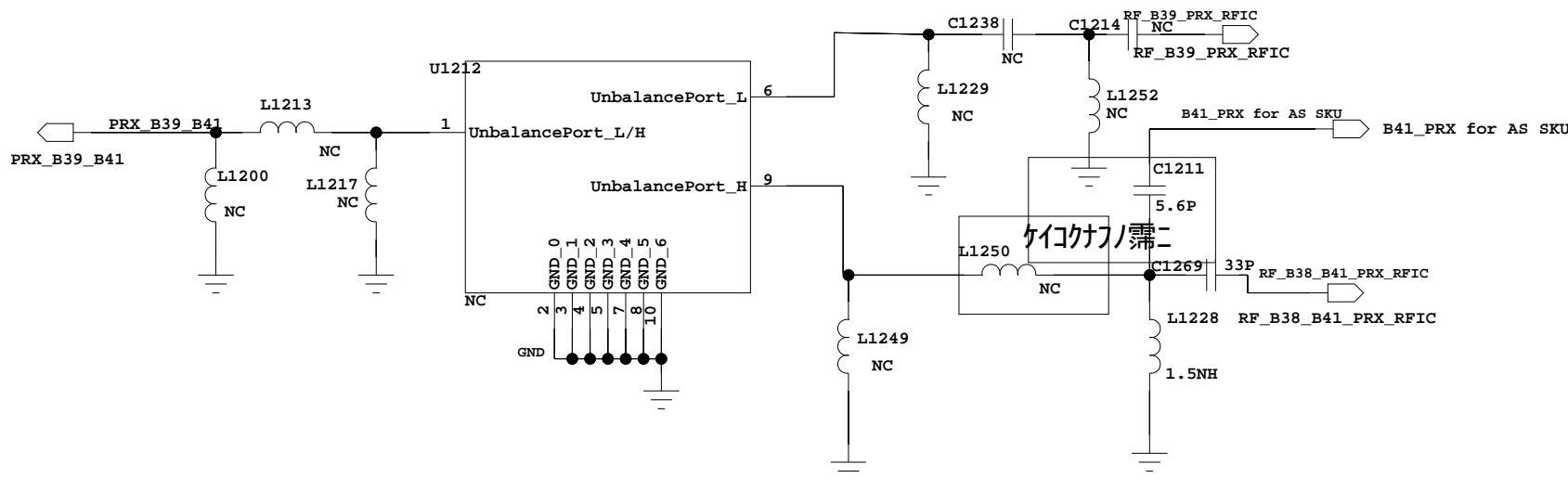
E

B34_DCS_PCS sawless RX



F

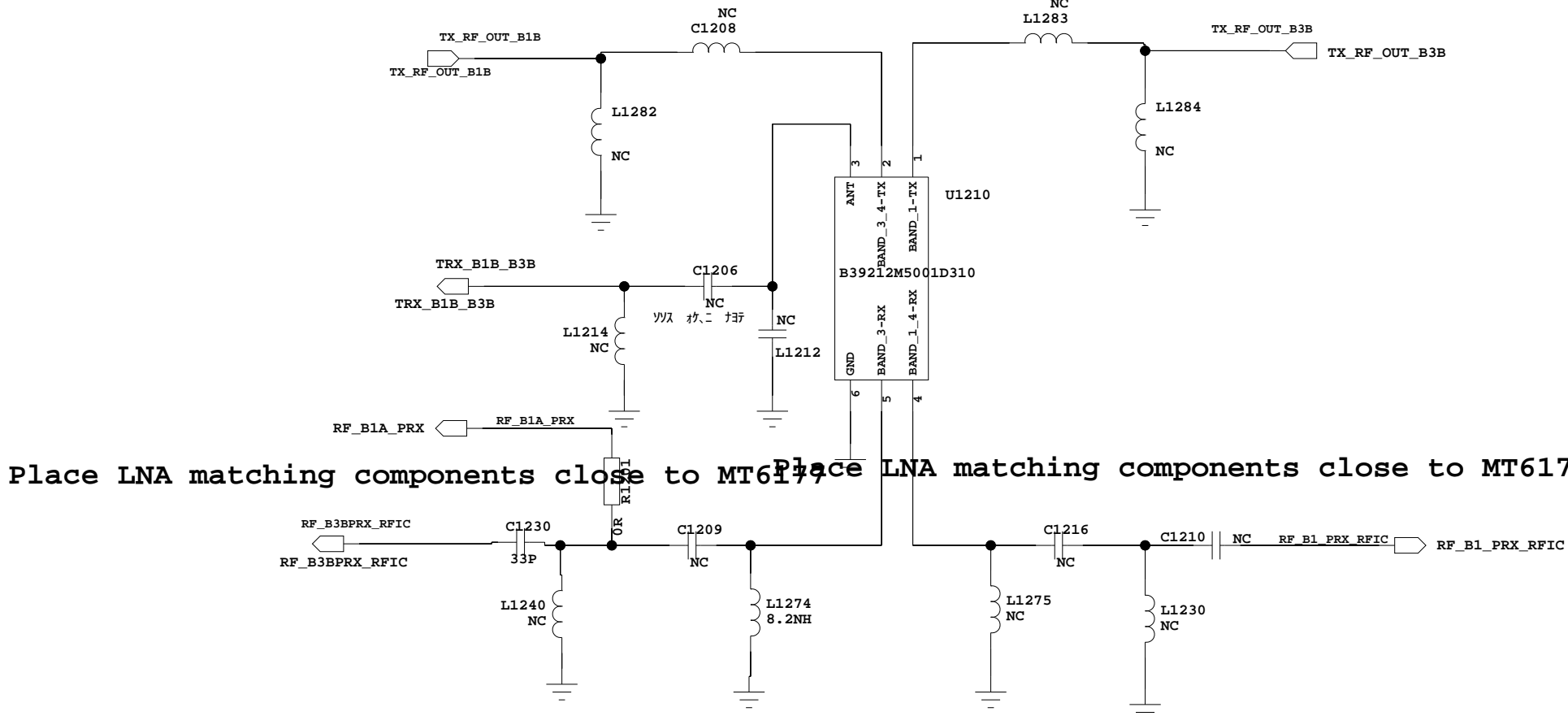
B39B41 CA



A

B

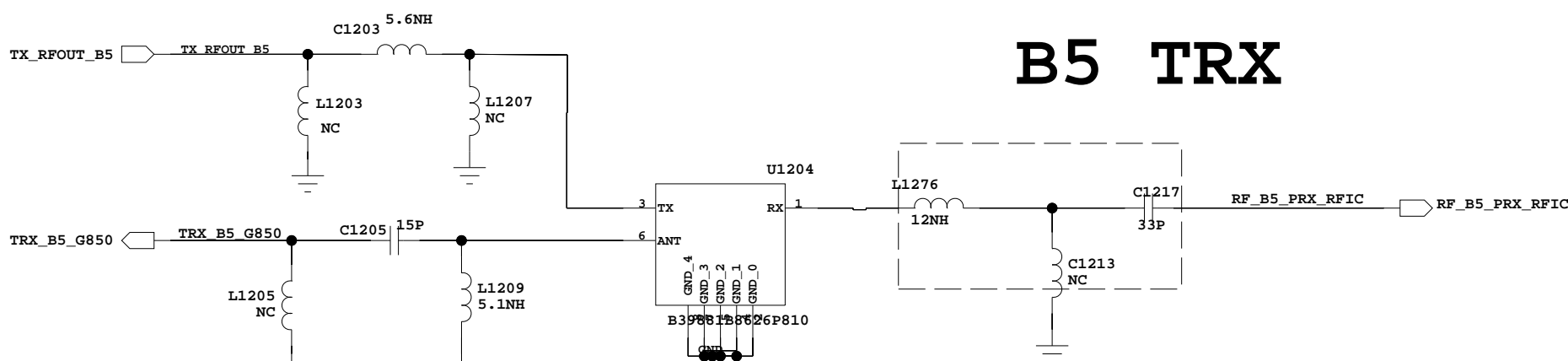
B1B/B3B CA TRX



C

D

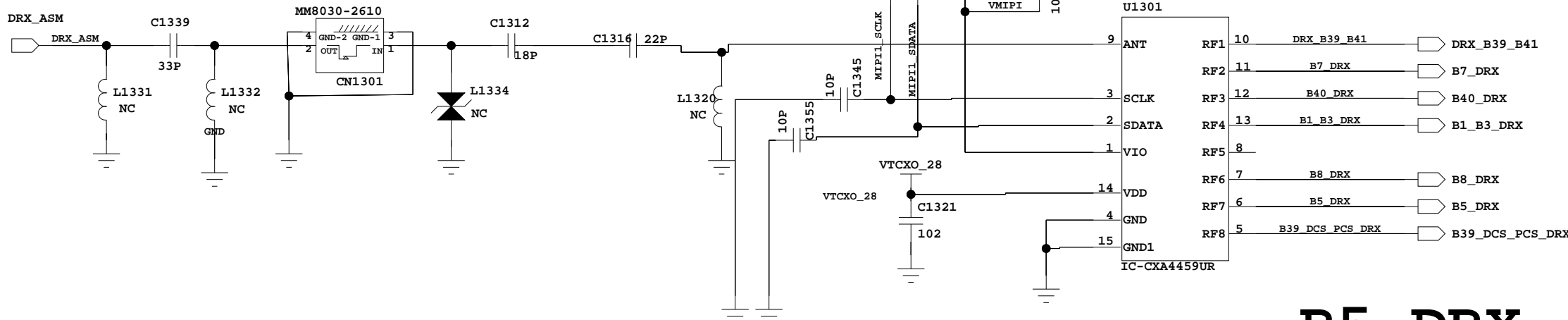
B5 TRX



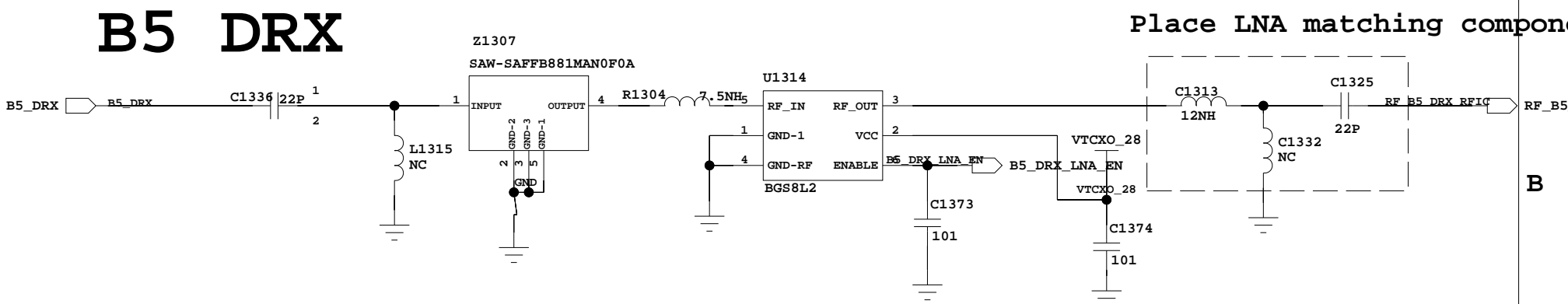
E

Place LNA matching components close to MT6177

LTE DRX

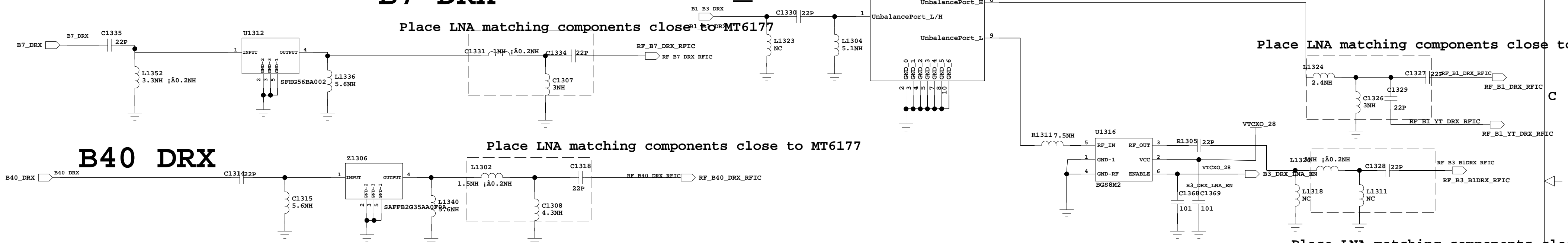


B5 DRX

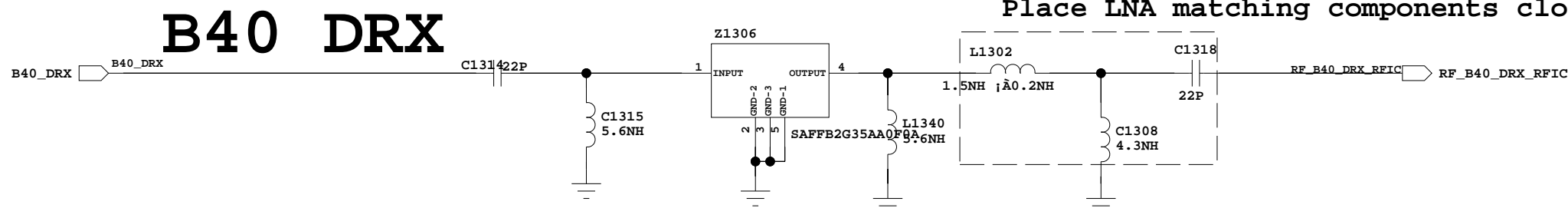


B7 DRX

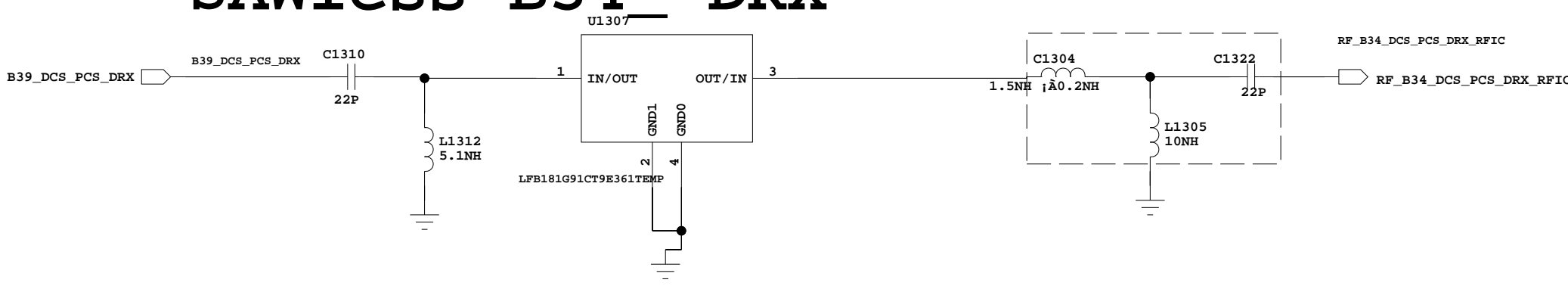
B1_B3 DRX



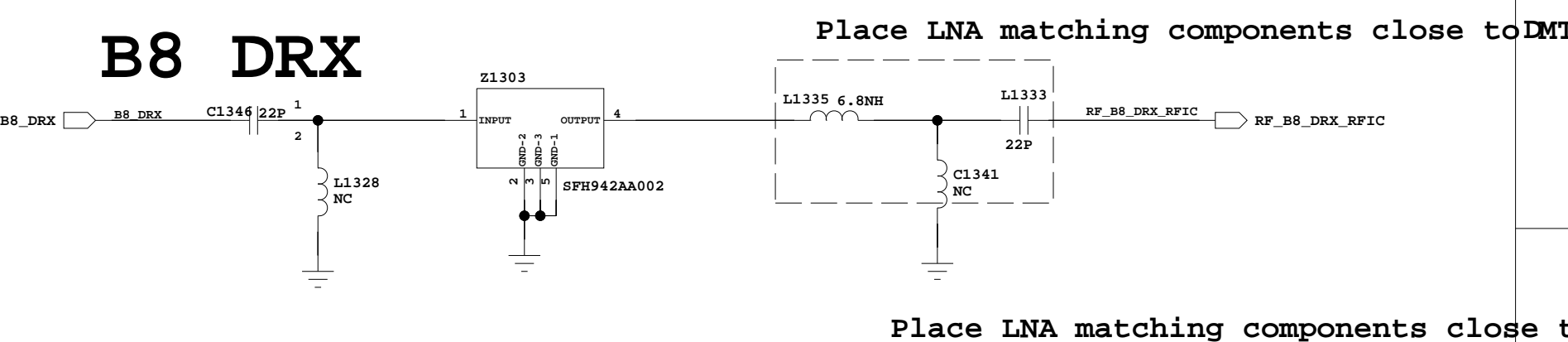
B40 DRX



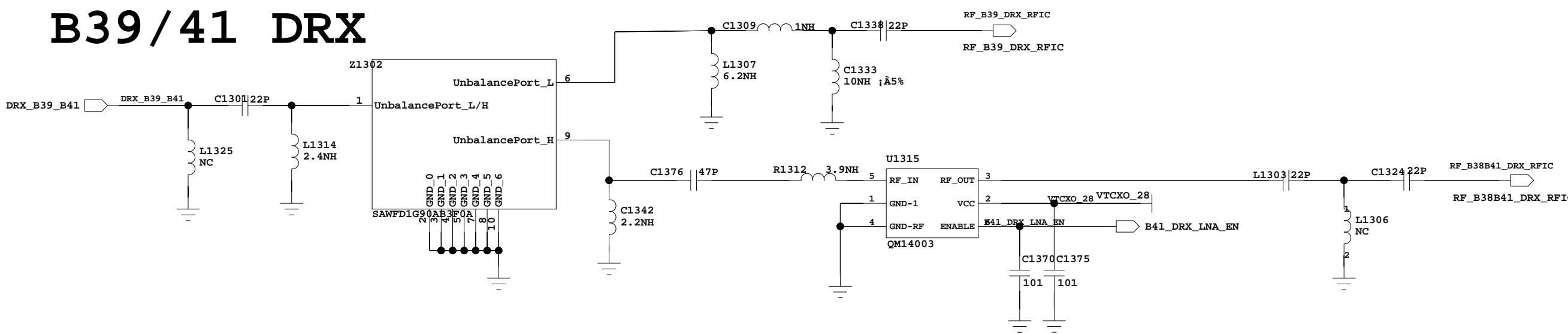
SAWless B34_DRX

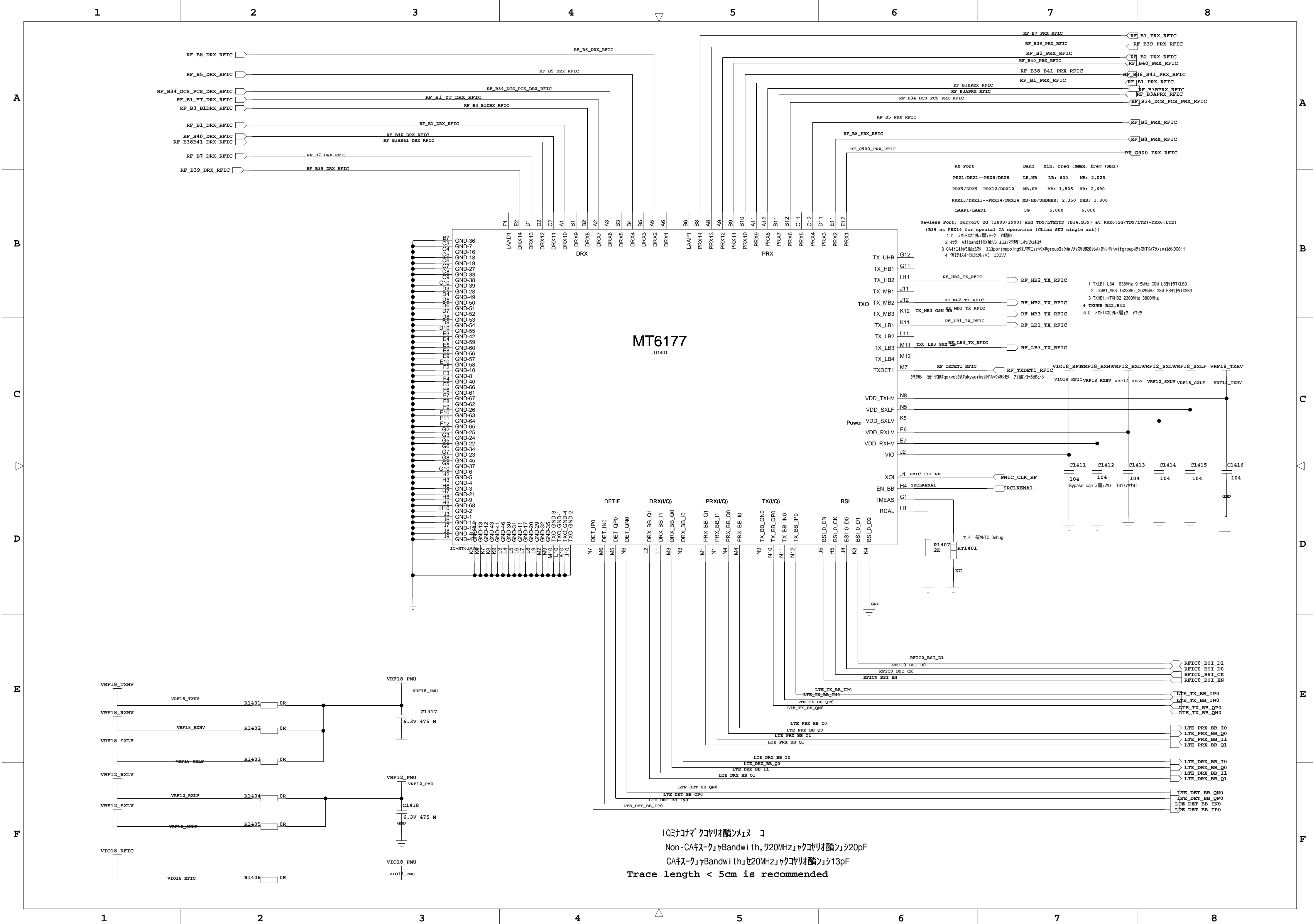


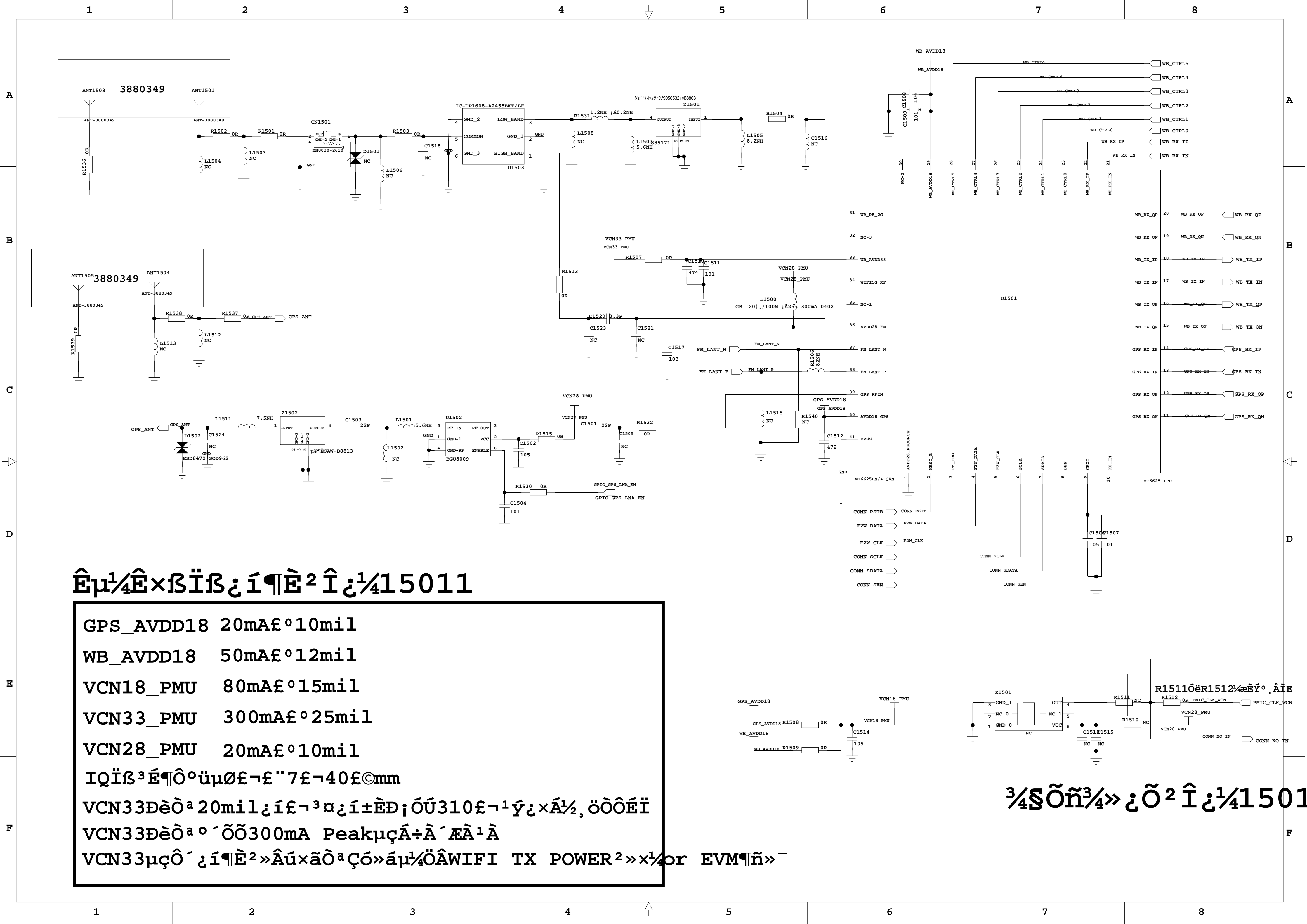
B8 DRX

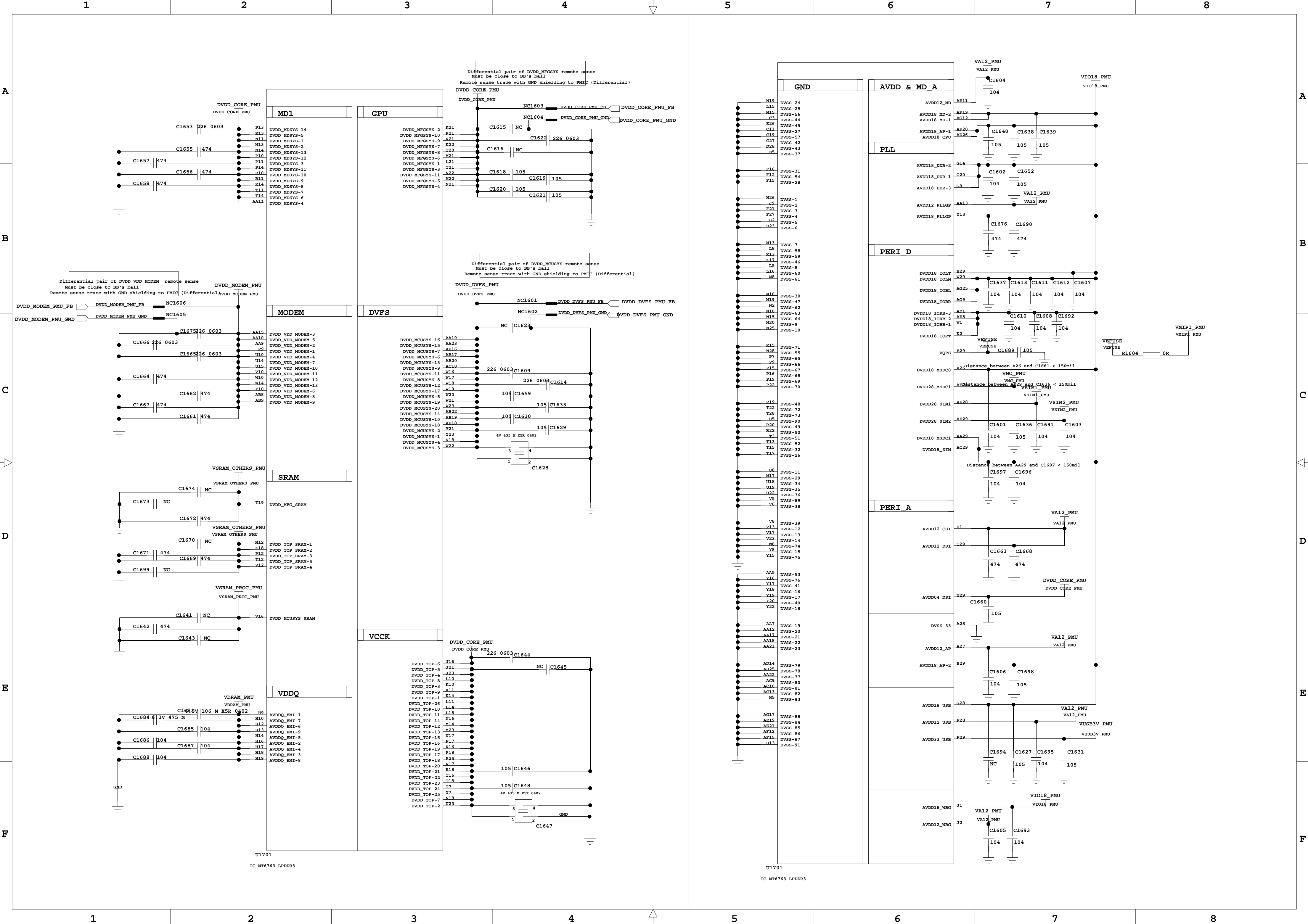


B39/41 DRX









A

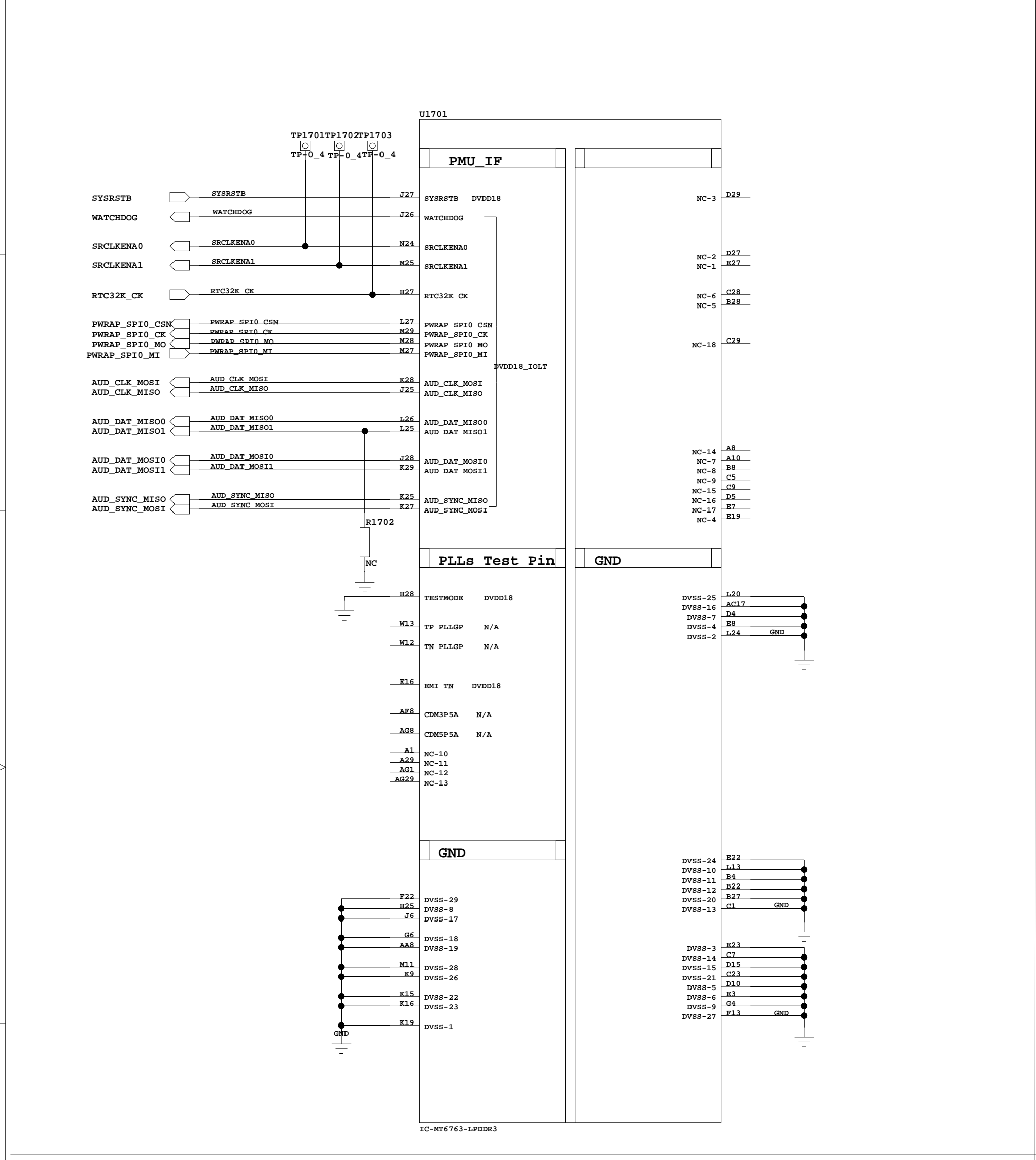
B

C

D

E

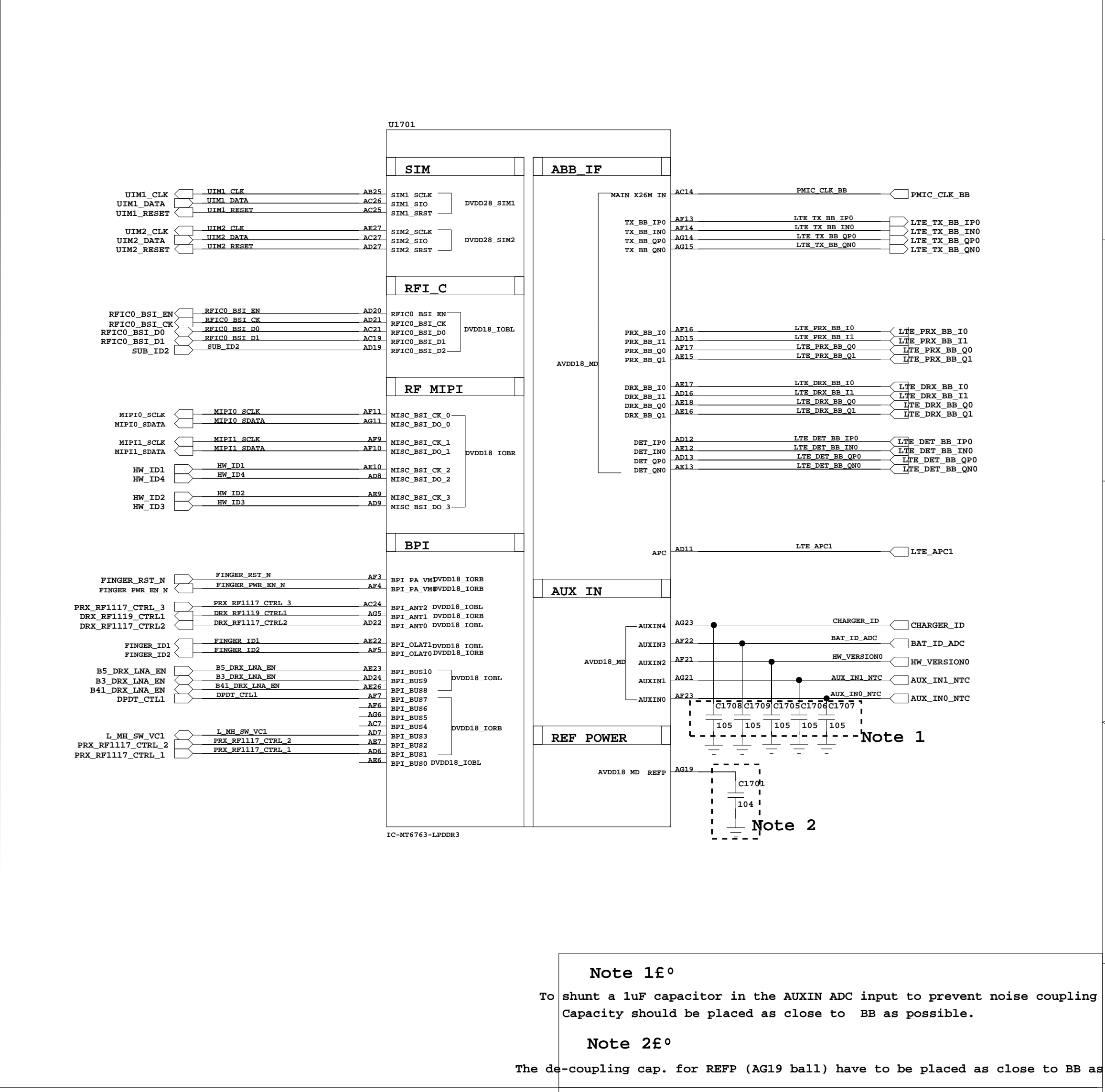
F



Note:

PWRAP_SPI0_CSN and AUD_DAT_MOSI are JTAG feature in bootstrap.

set to N/A by trapping pin, Do not set GPIO[85:88, 8] as JTAG mode (Aux Func. 7) in DCT tool (dws file)

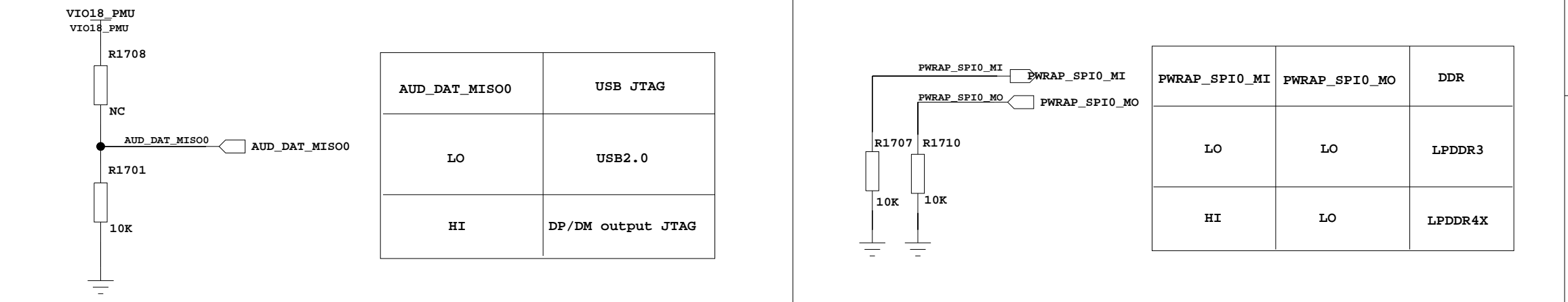
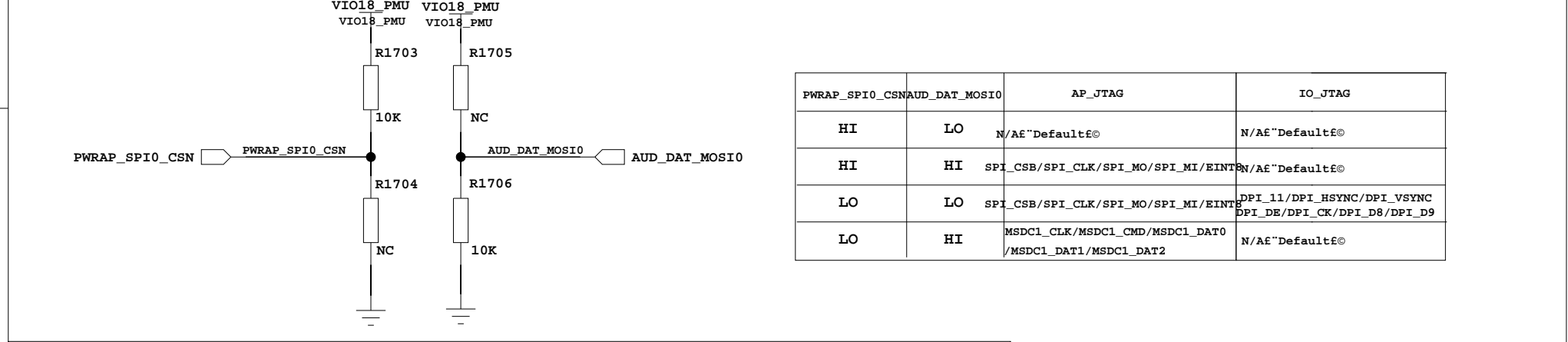


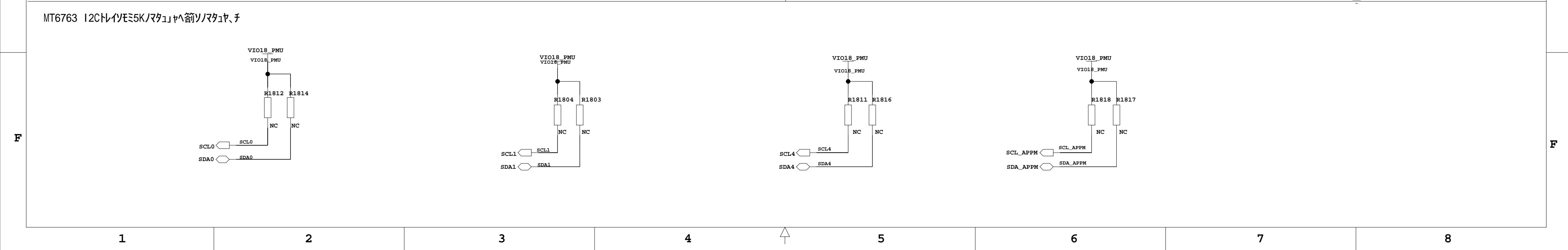
Note 1

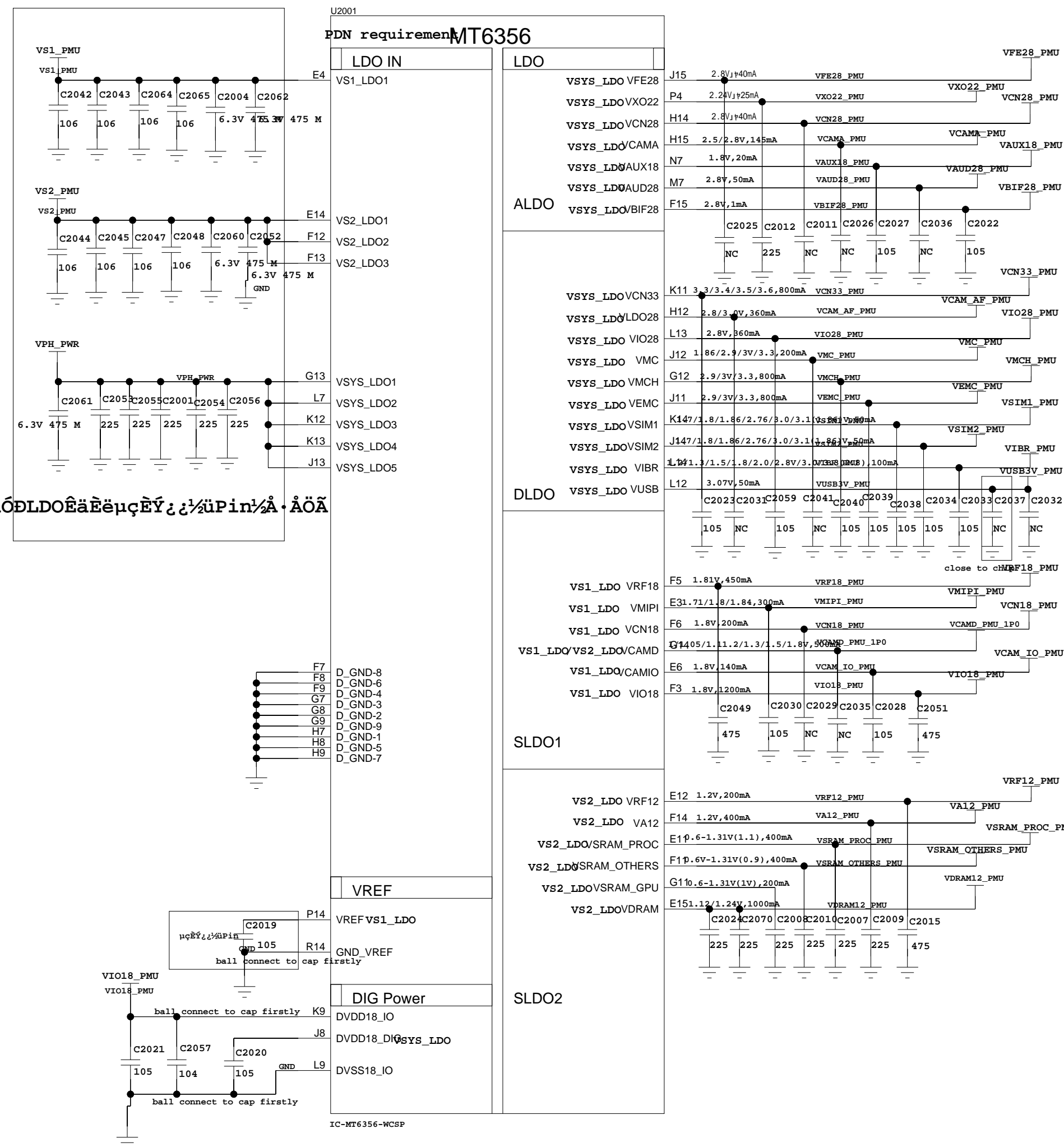
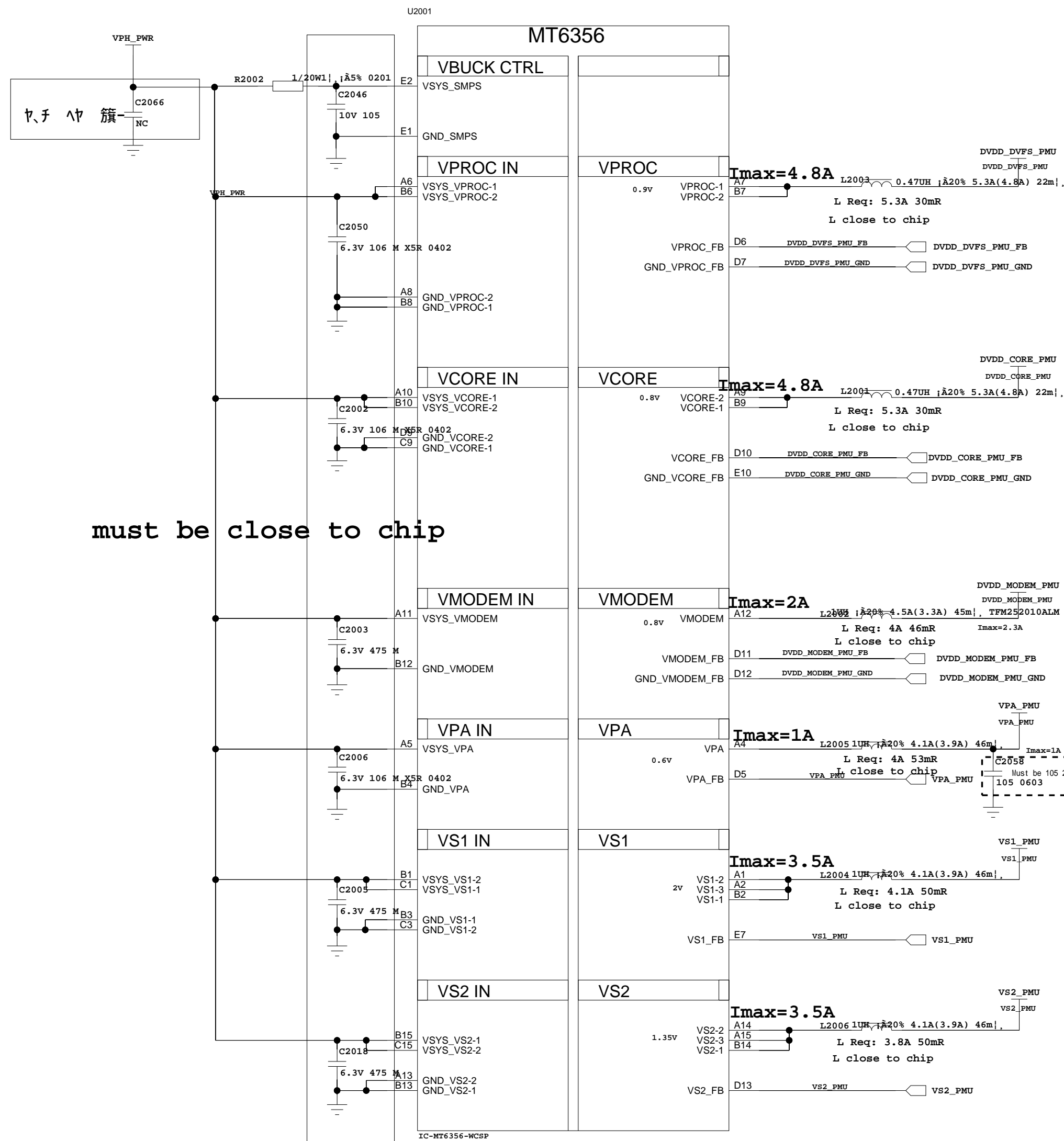
To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling Capacity should be placed as close to BB as possible.

Note 2

The de-coupling cap. for REFP (AG19 ball) have to be placed as close to BB as possible

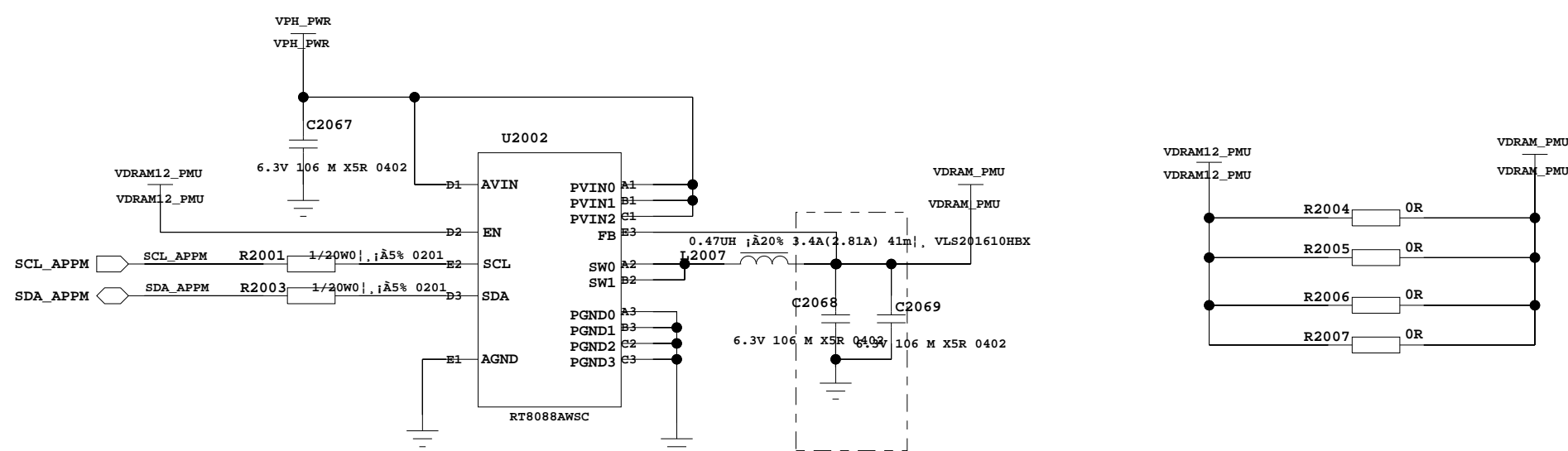




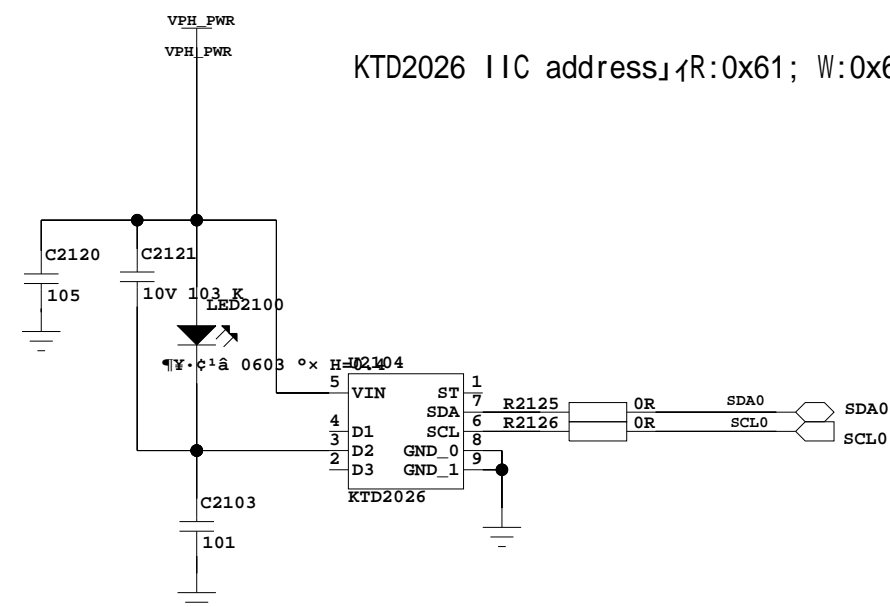
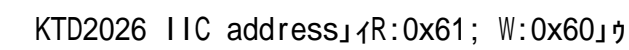


Note 1f°
output cap SHOULD be placed even if the LDO is not used. Such as VSRAM_GPU, VDRAM.

Note 2f°
VDRAM from MT6356 is used for LPDDR3 power. Ext. buck is for LPDDR4X.



A



Route AVDD18_AUXADC/AUXADC_VIN as differential trace (3 mil each) with well GND shielding and route AVSS18_AUXADC with 15mil trace width under AVDD18_AUXADC/AUXADC_VIN trace to provide return current path.

7

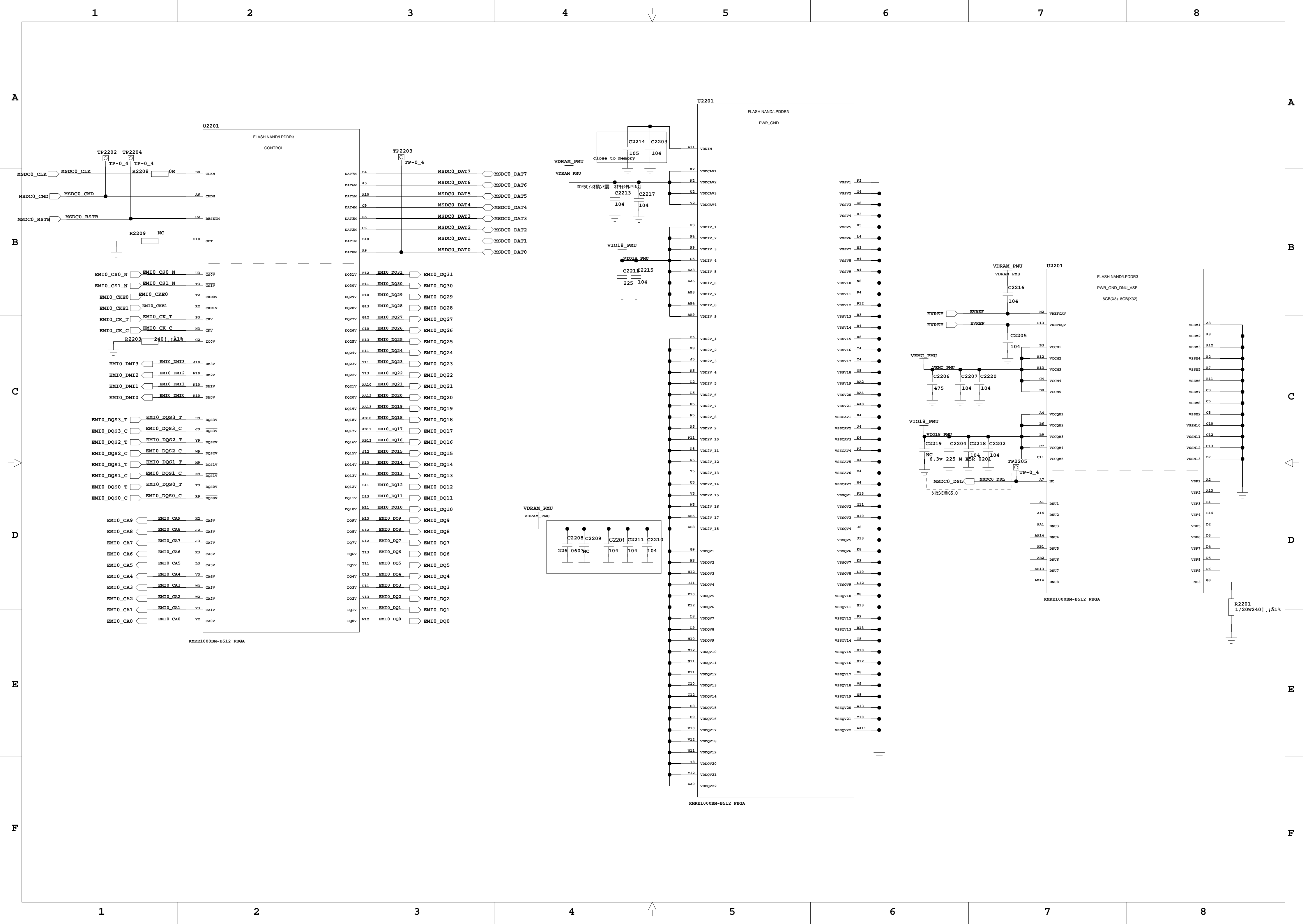
1

•

1

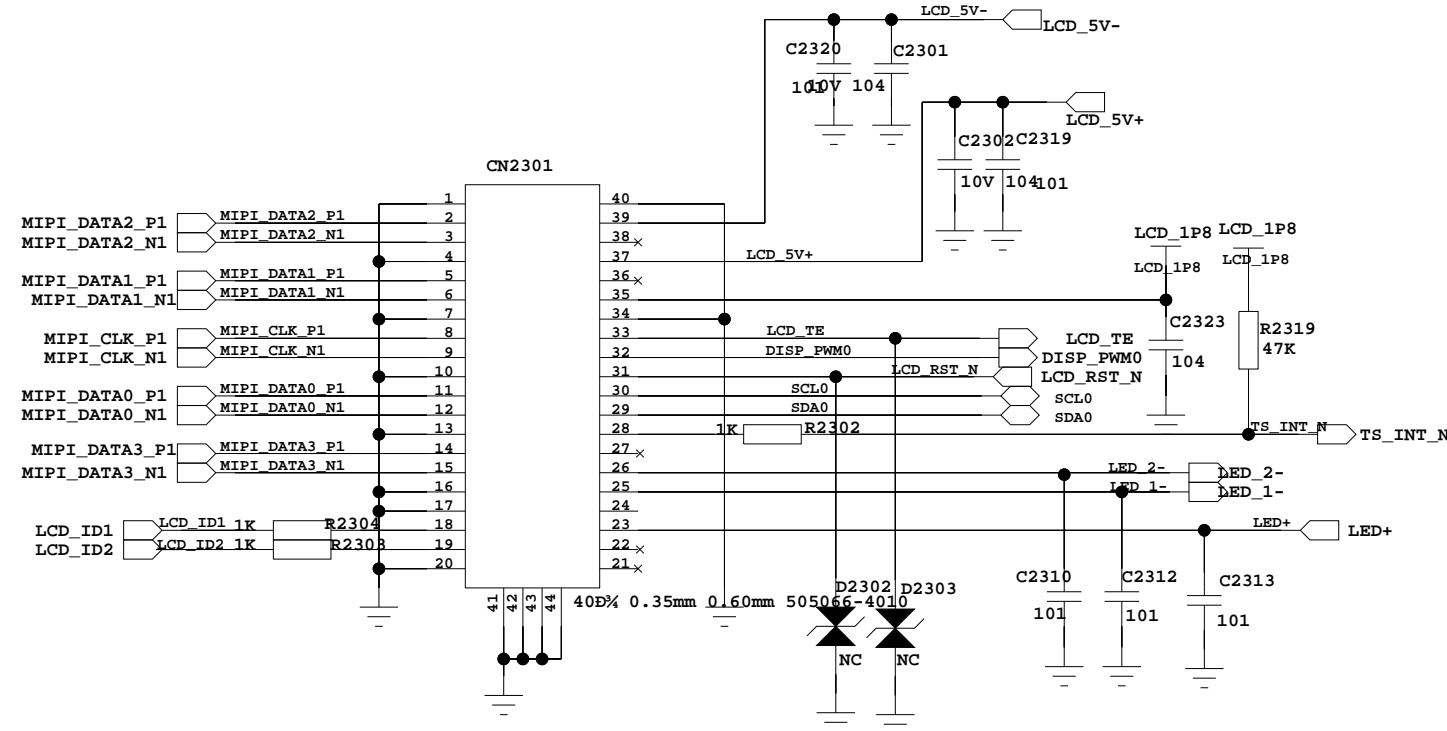
1

1

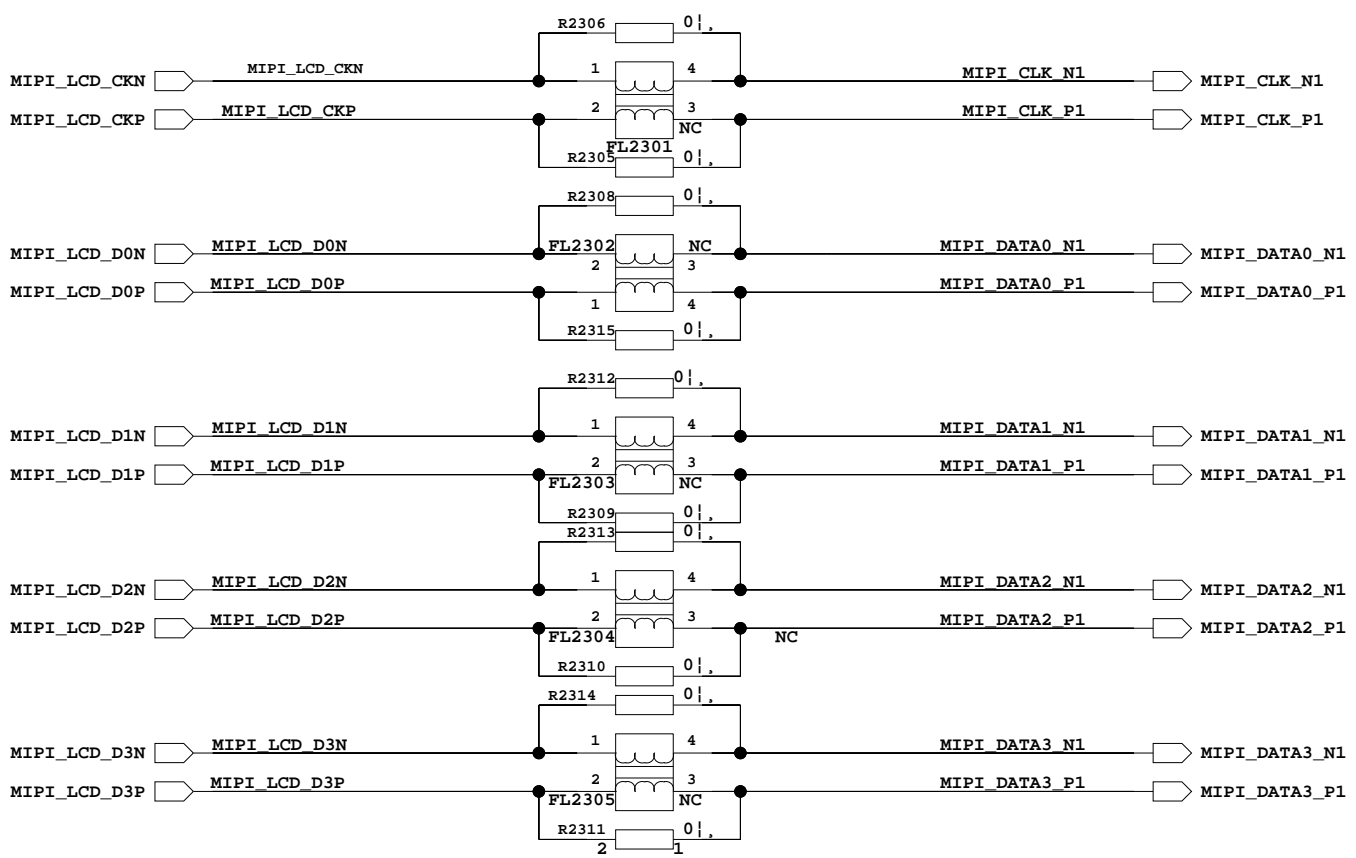


LCM Connector

TD4310 IIC address「R:0x21; W:0x20」



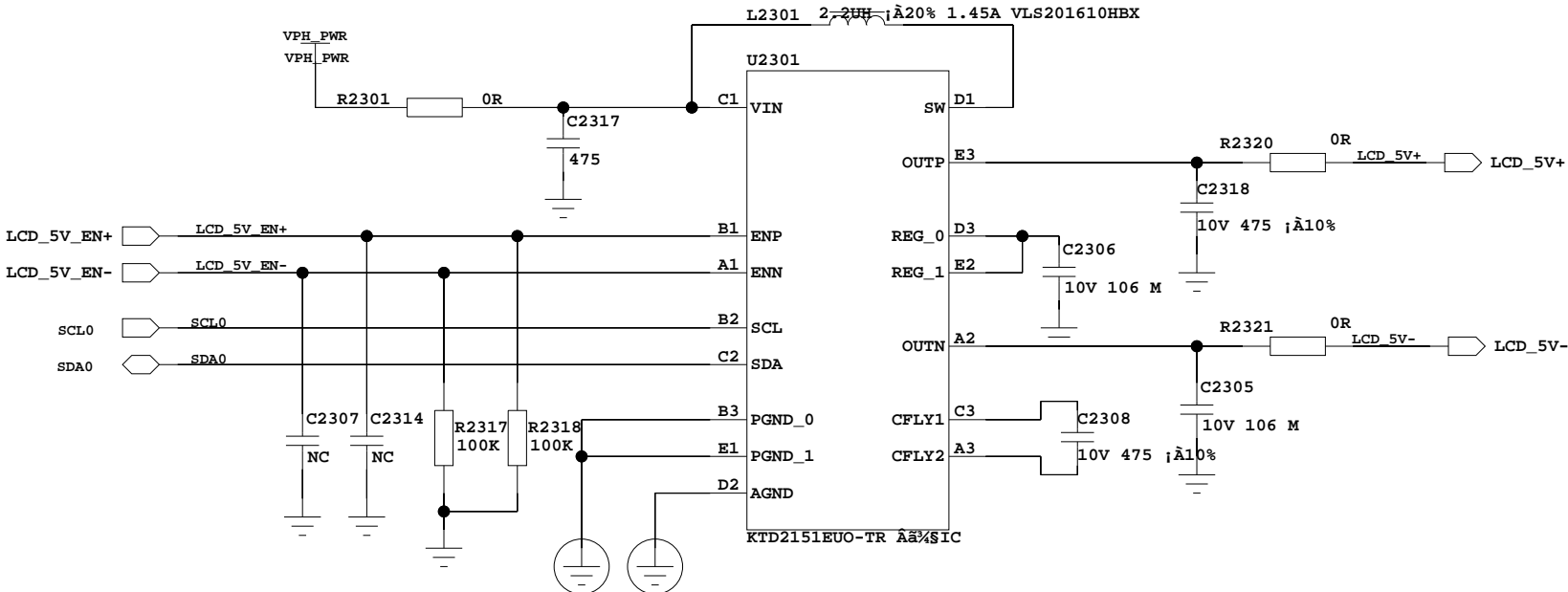
DSI CMF



LCD 5V Driver

KTD2151 I2C address「R:0x7D; W:0x7C」

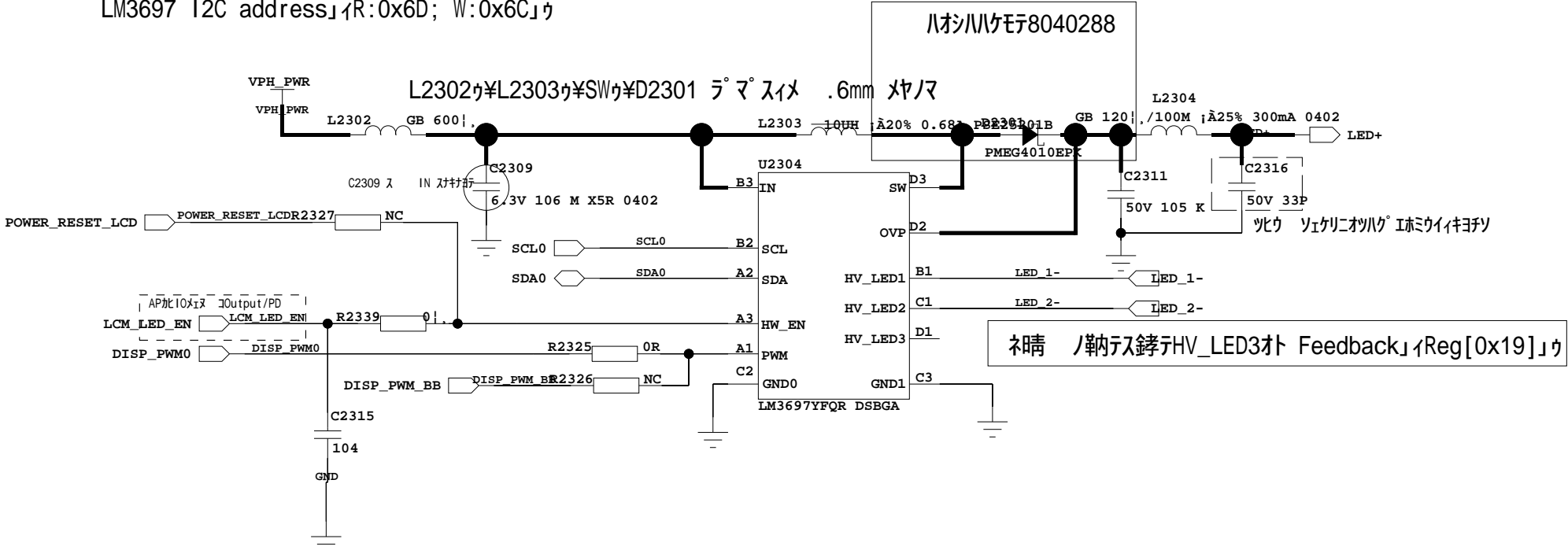
ツ贏アIC」ヤラ「メ筈シヨホサヨモヲチ



ノ釐イリ」ト筈ヲキヨエマツヨ リ

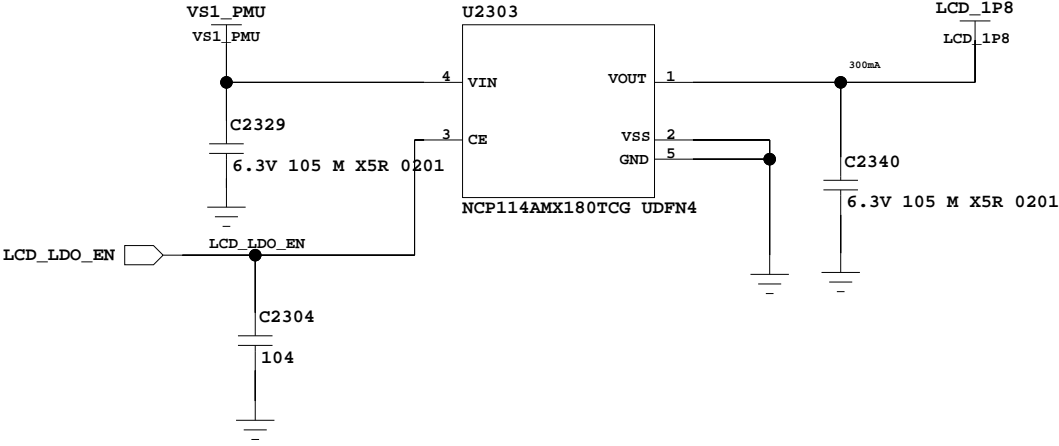
LCD BL

LM3697 I2C address「R:0x6D; W:0x6C」



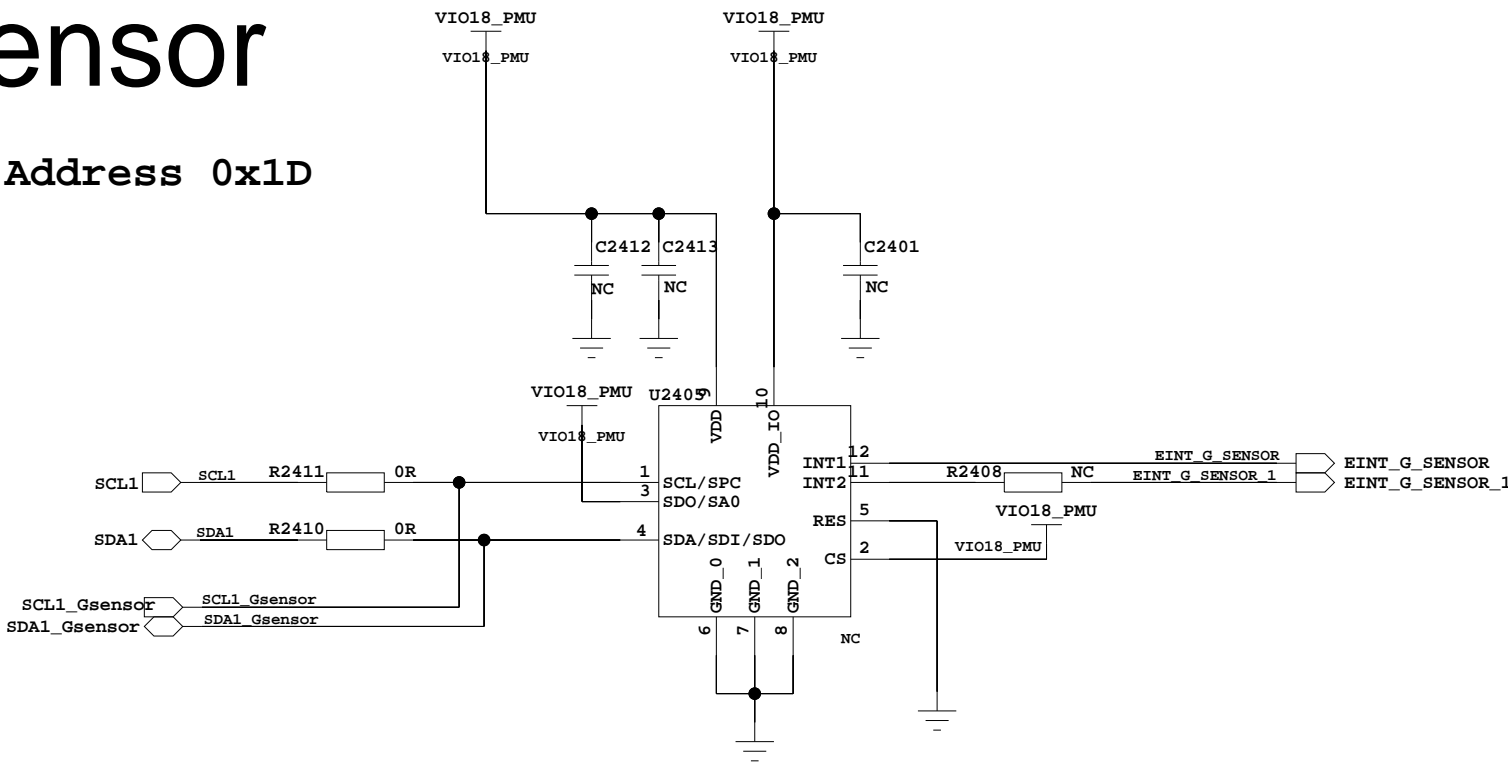
ネ晴 ノ靴ナス録テHV_LED3オト Feedback」Reg[0x19]」

LCD IO LDO



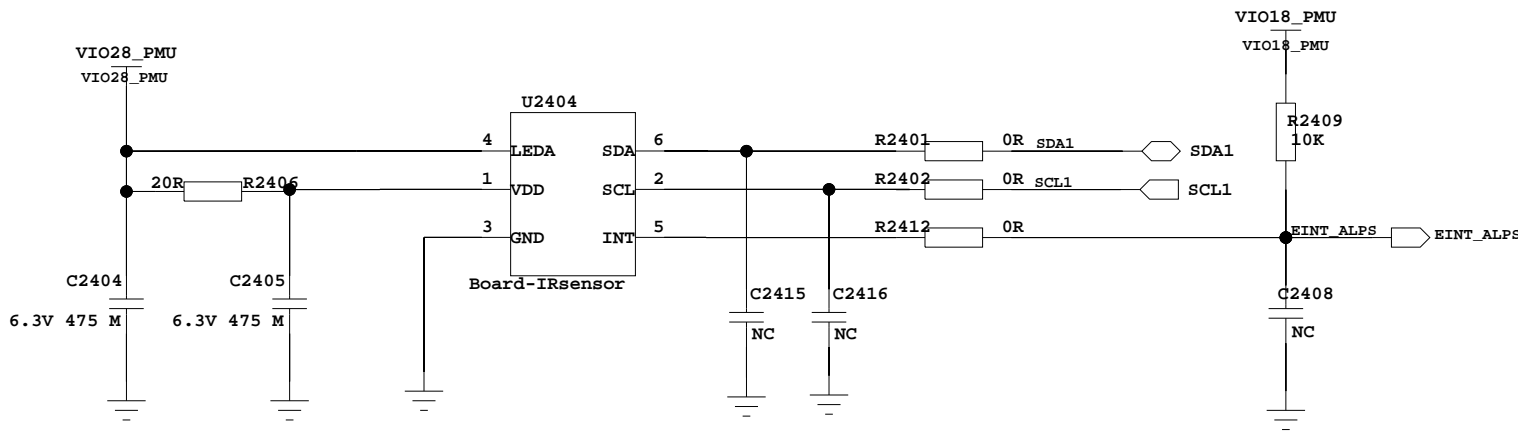
G-Sensor

LIS2DS I2C Address 0x1D

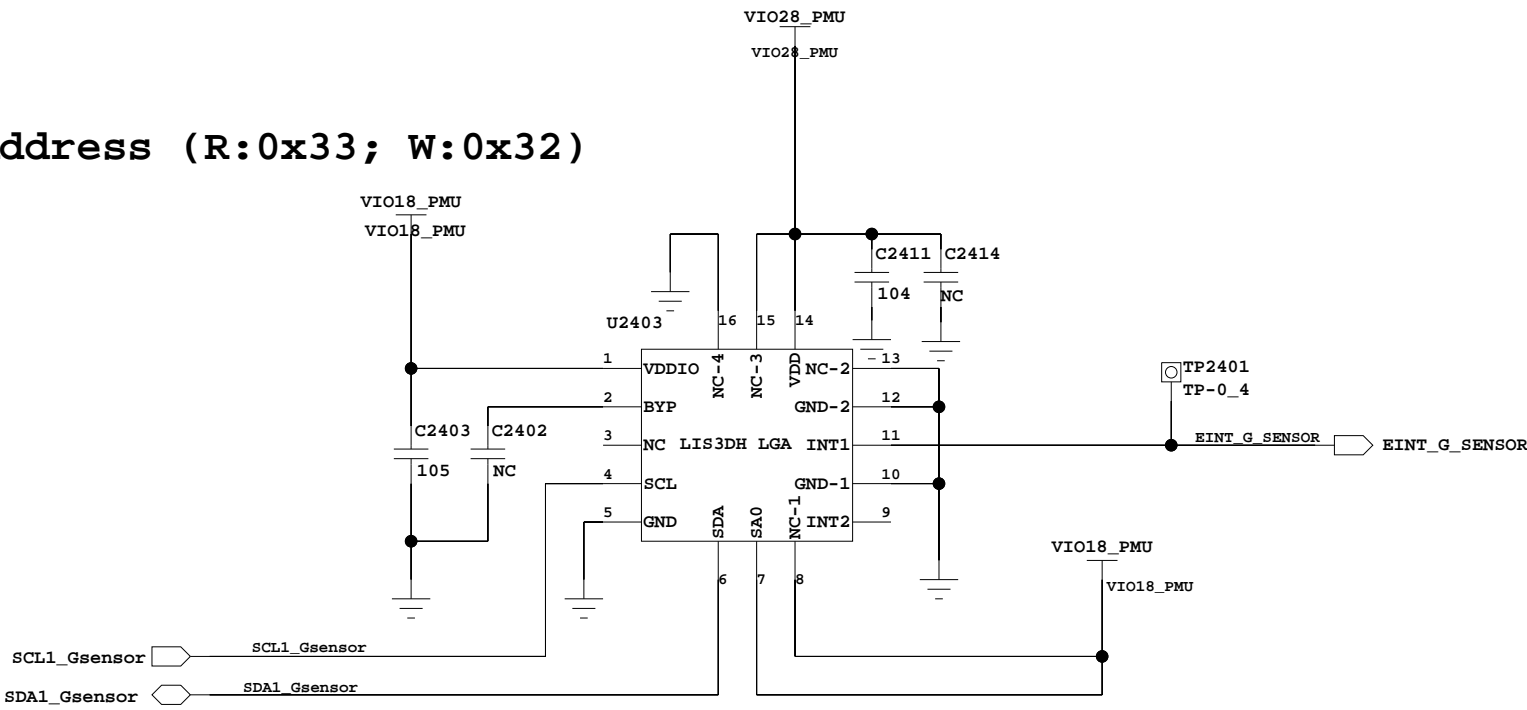


A.L.S.+P.S sensor

APDS9922 I2C Address (R:0xA7; W:0xA6)

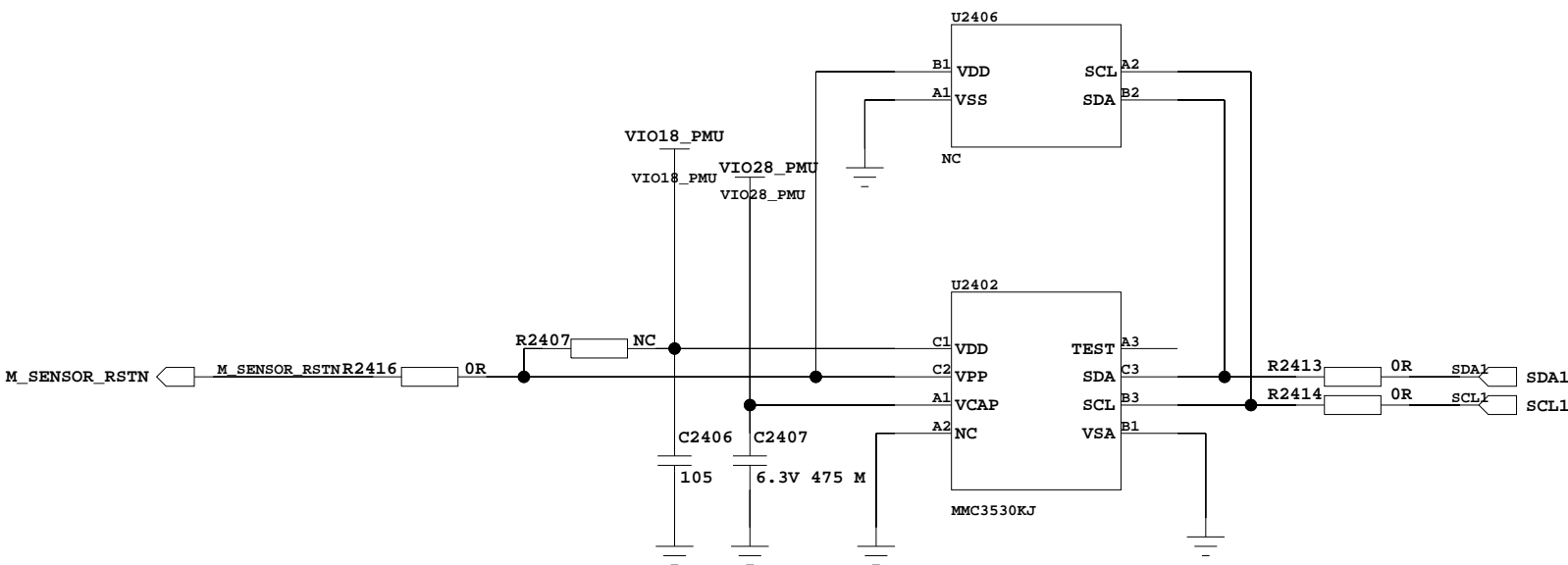


LIS3DH I2C Address (R:0x33; W:0x32)

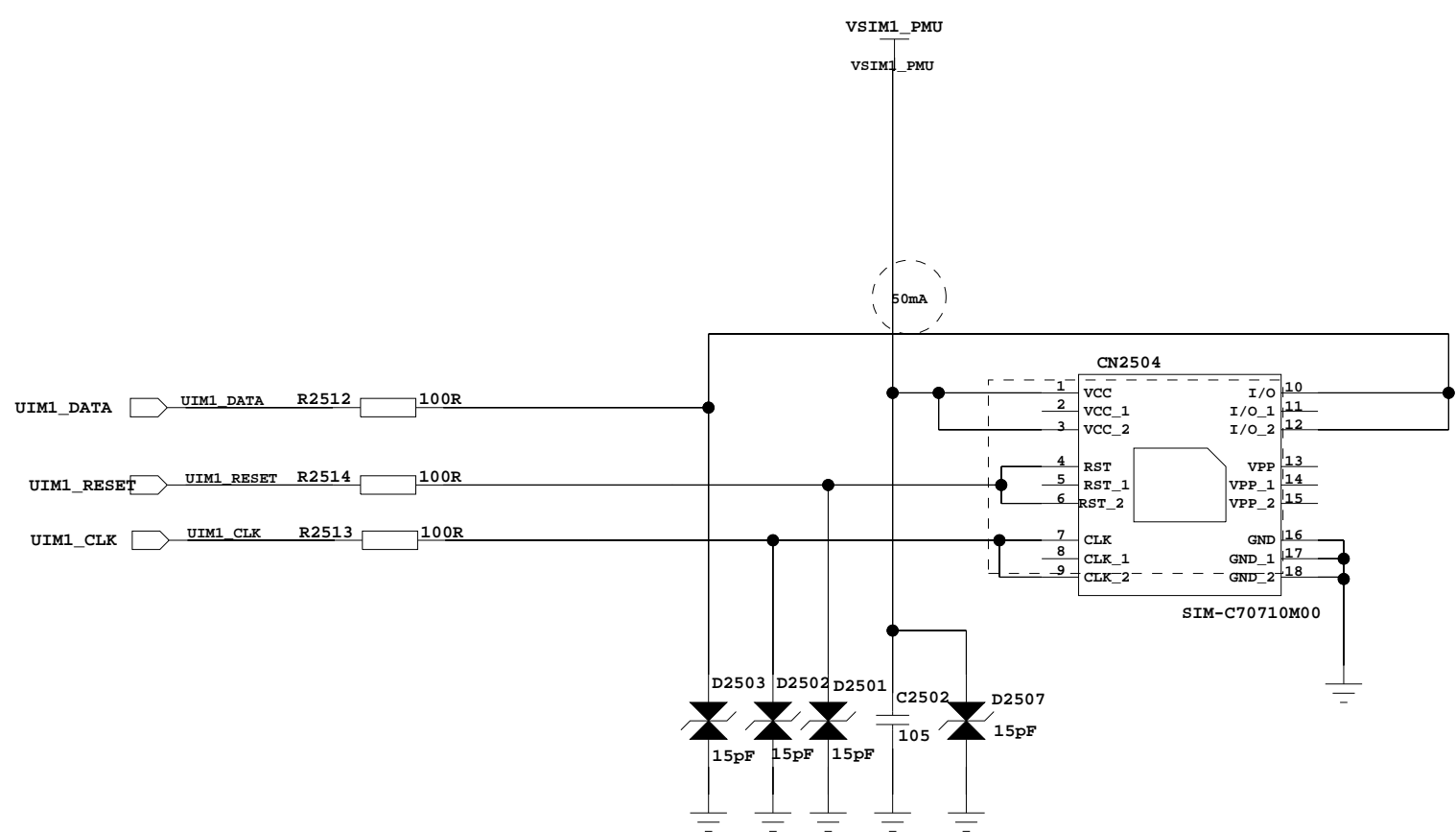


M Sensor

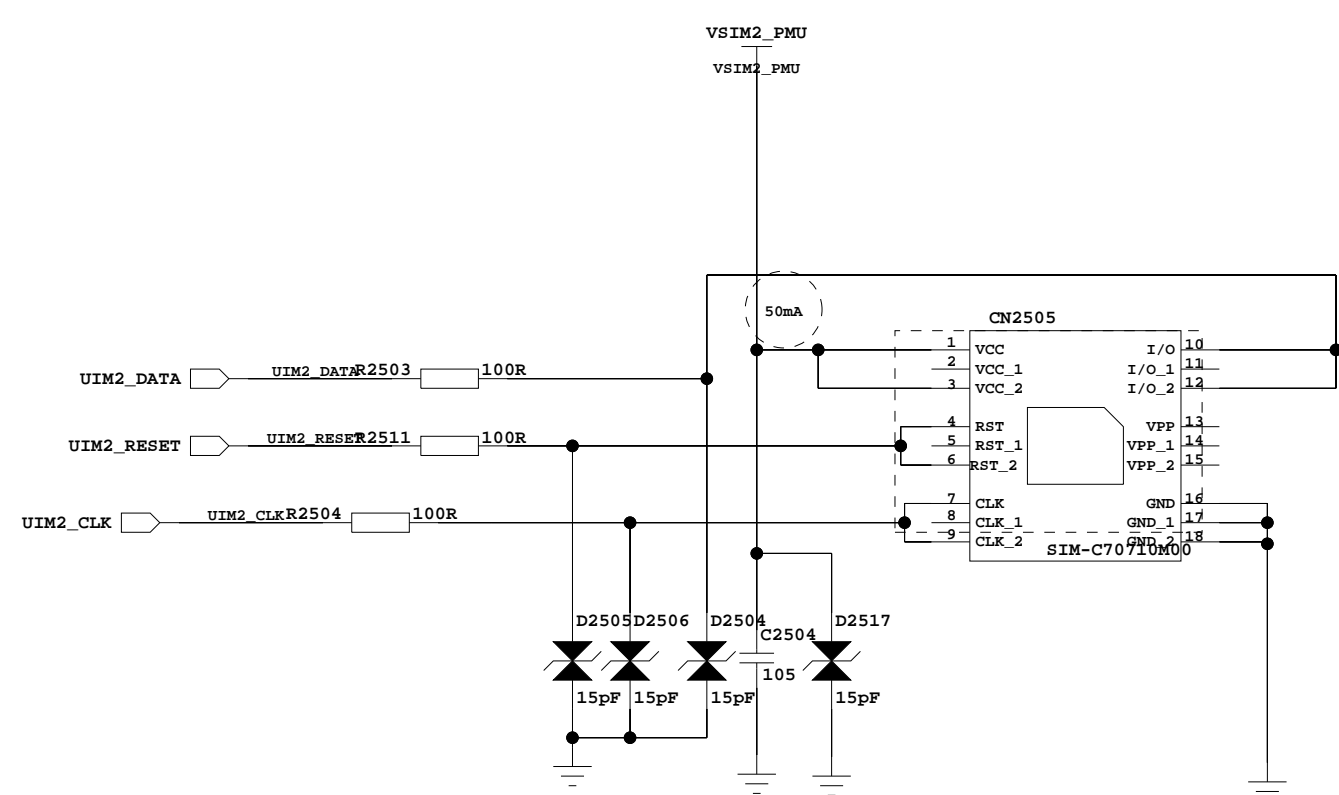
AK09911 I2C Address (R:0x19; W:0x18)



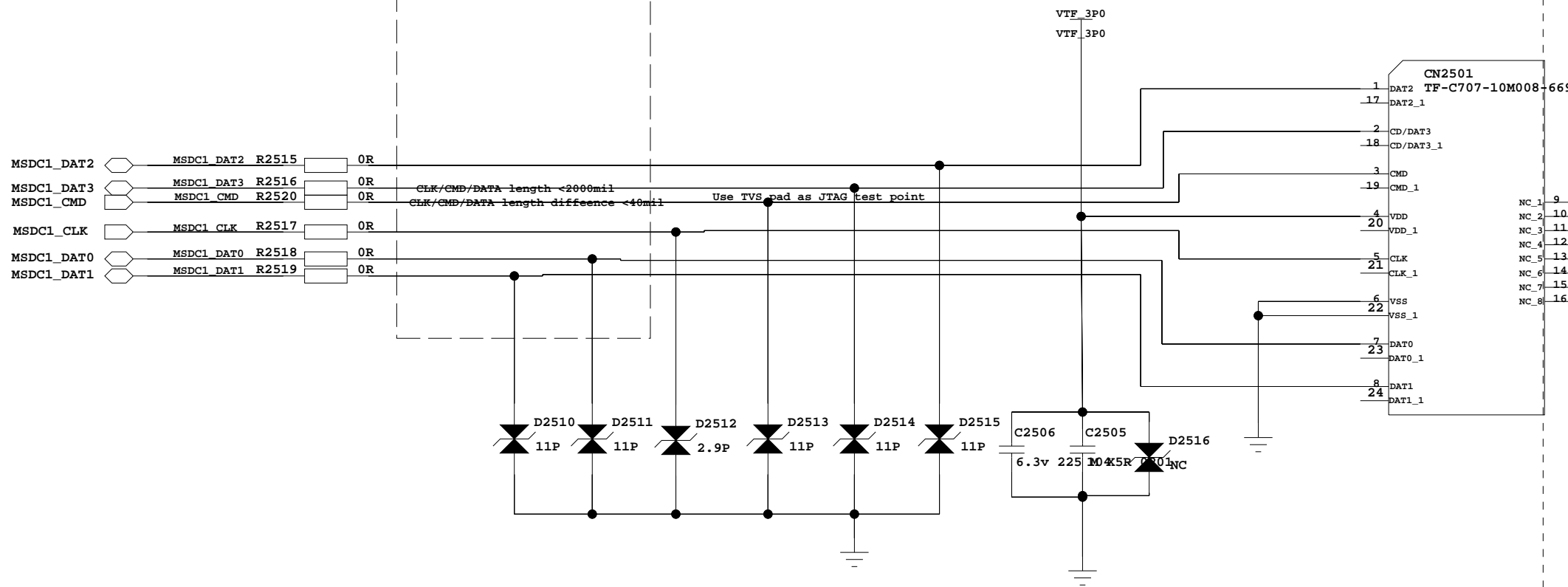
SIM1 Card



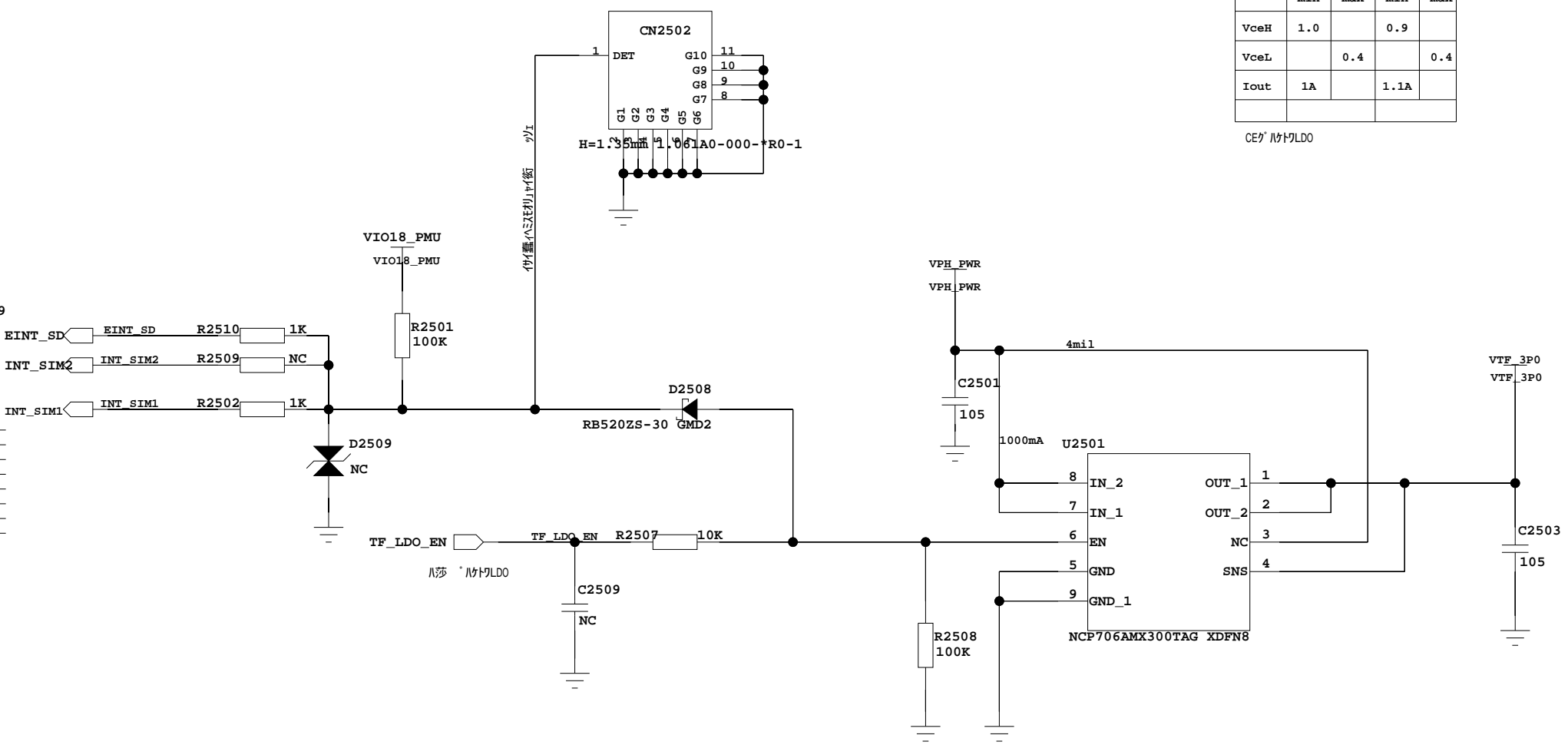
SIM2 Card



TF_CARD



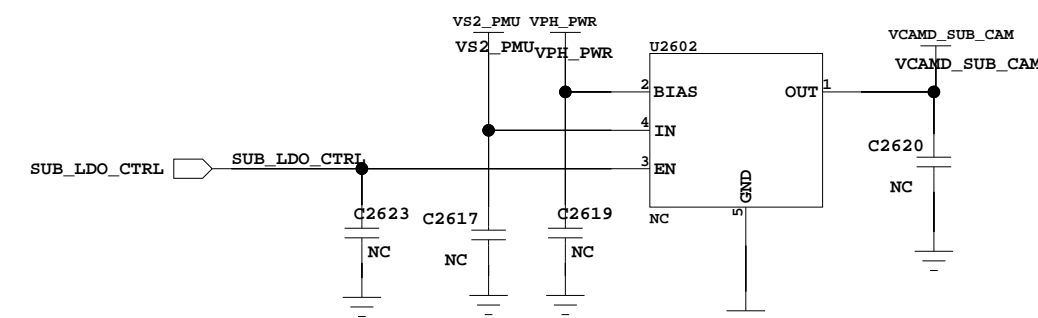
Hot plug: Ext 2.95v supply



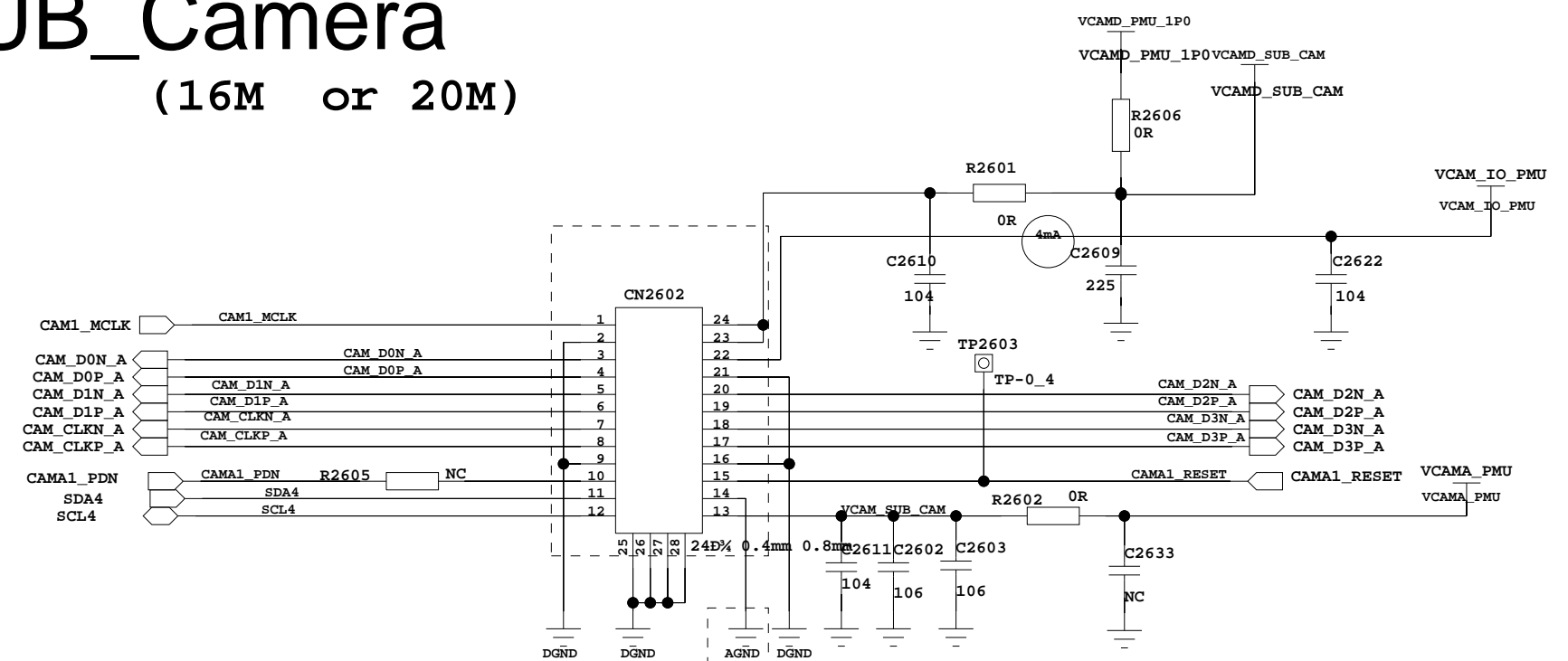
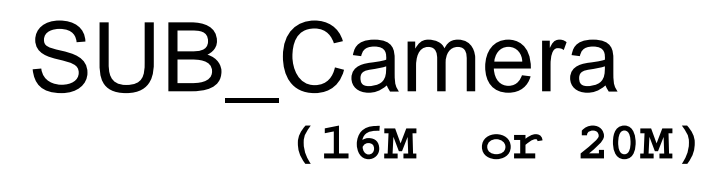
	RP115L301D 9170125		NCP706A 9170224	
	min	max	min	max
VceH	1.0		0.9	
VceL		0.4		0.4
Iout	1A		1.1A	

CEP / 1019LDO


```
3P8SX I2C address_1R:0x5B; W:0x5A;
AF_Driver I2C address_1R:0x19; W:0x18;
EEPROM I2C address_1R:0xA1; W:0xA0;
```

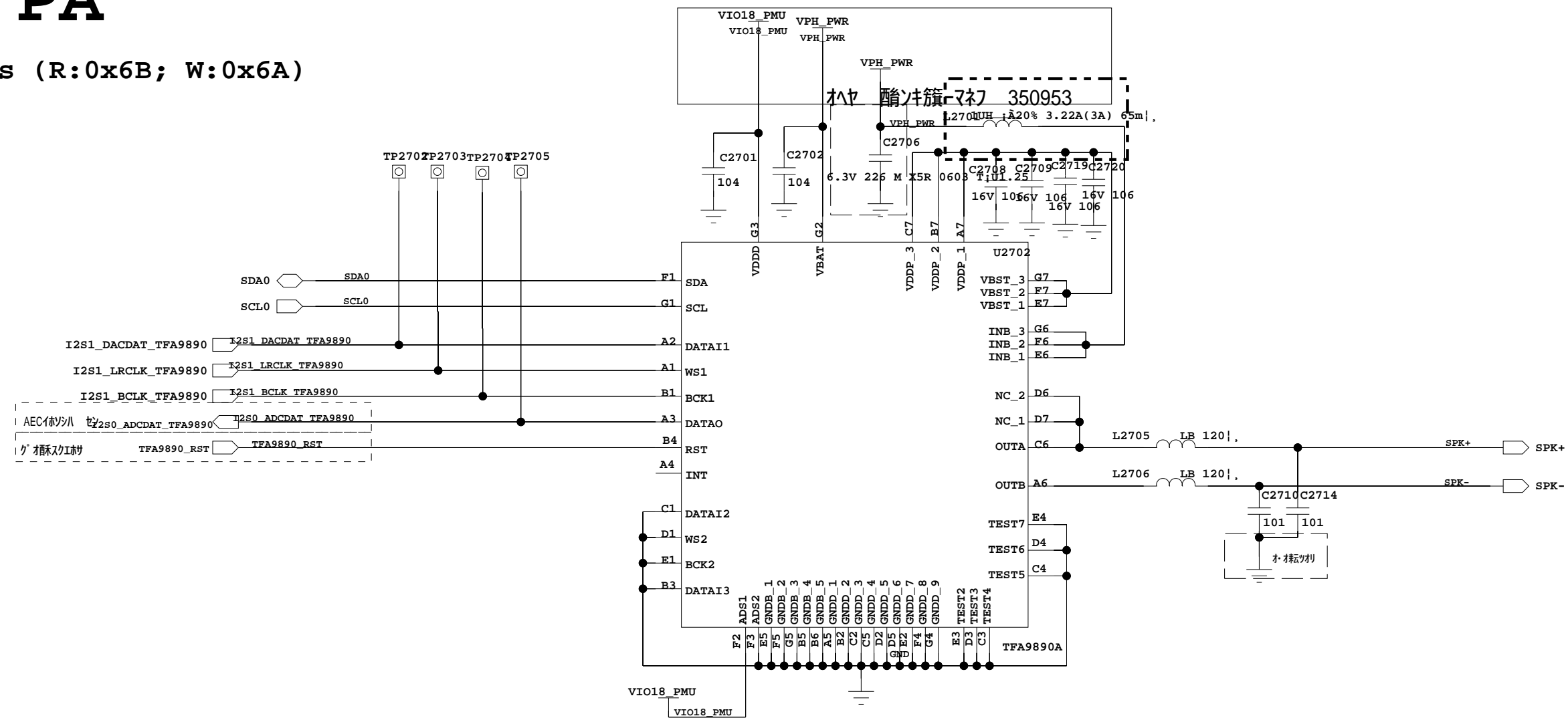


MP3331 slave Address is 0x0X67

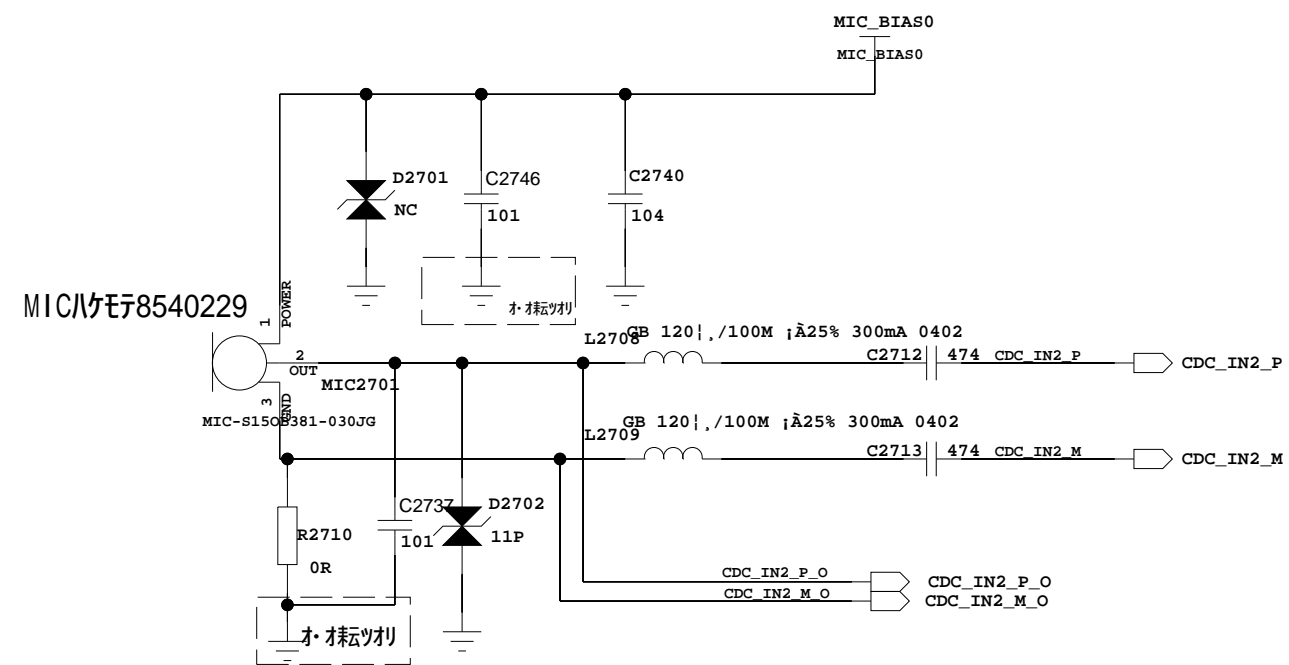


SMART PA

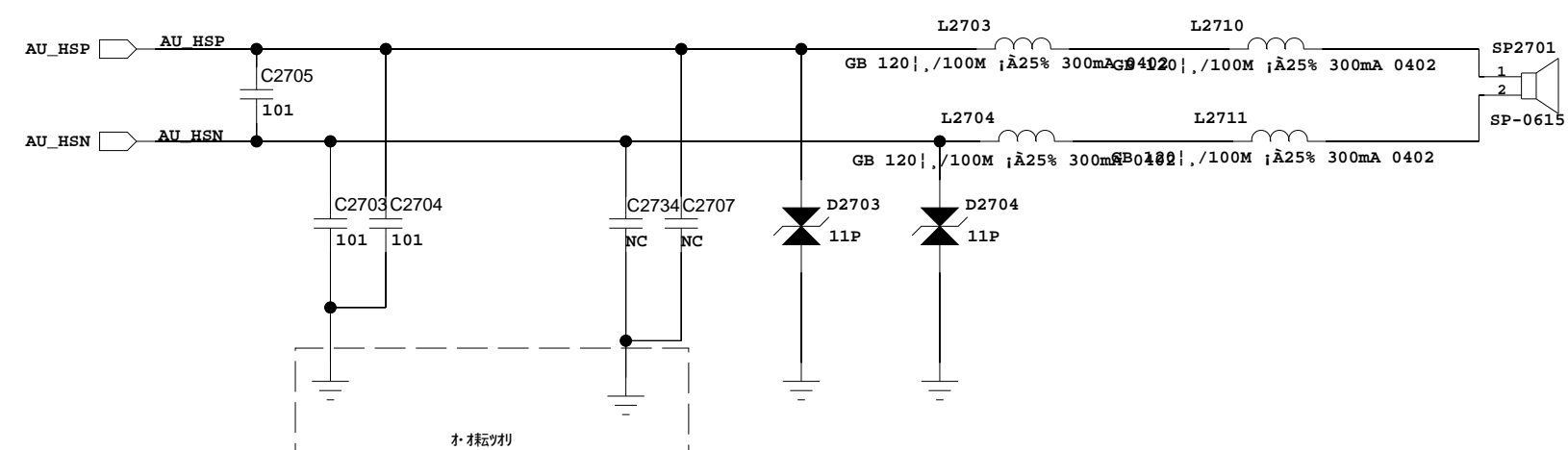
TFA9890A I2C Address (R:0x6B; W:0x6A)



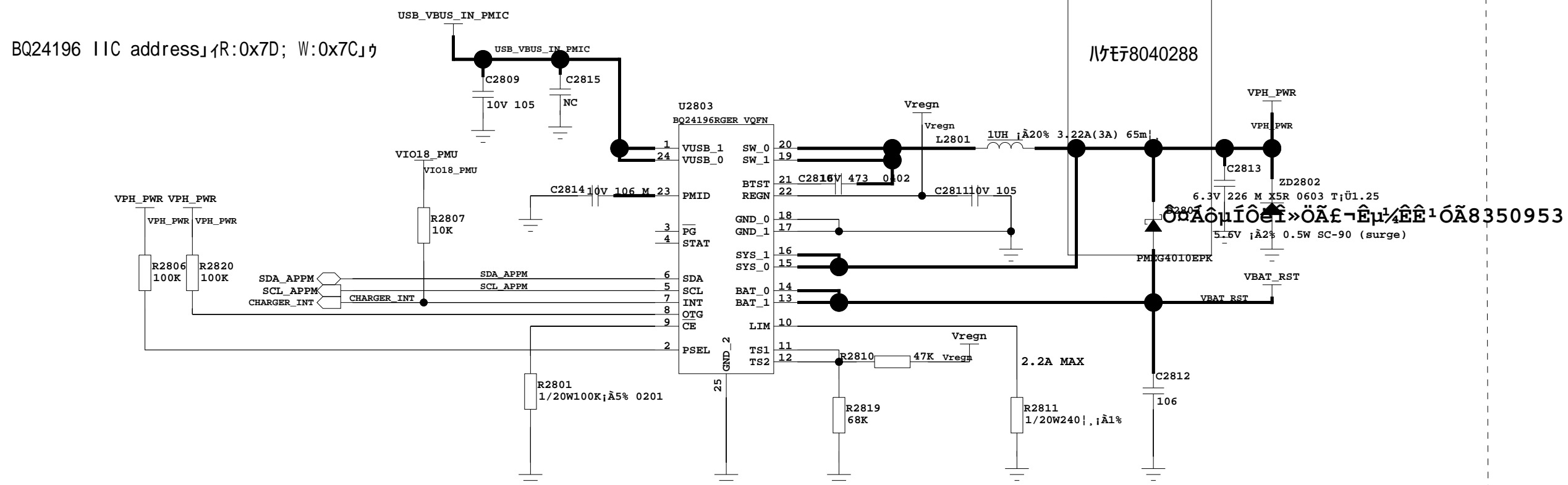
Ant-Noise MIC



Receiver

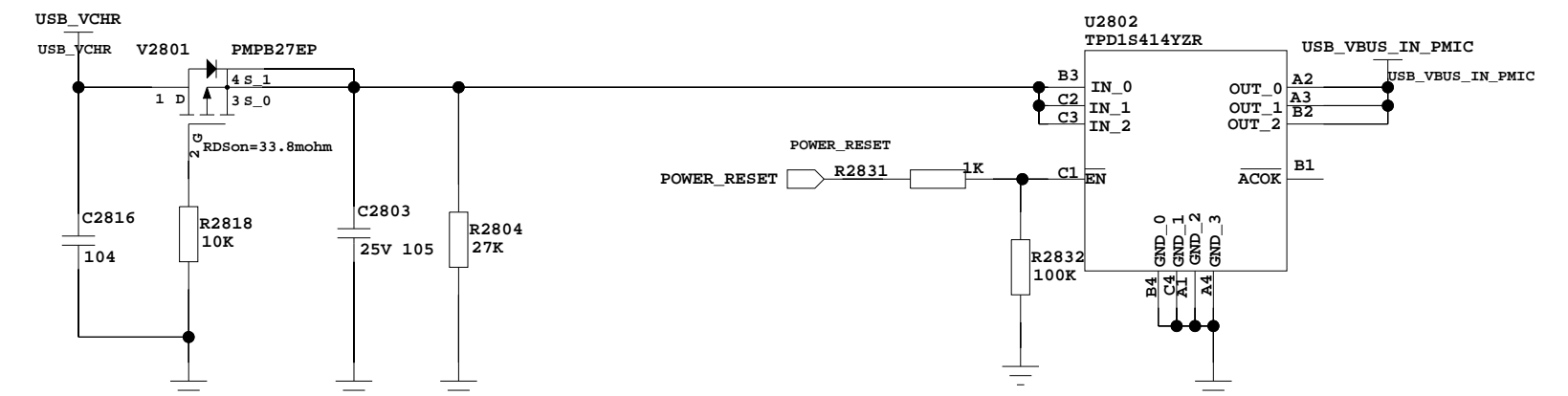


Internal Switching Charge

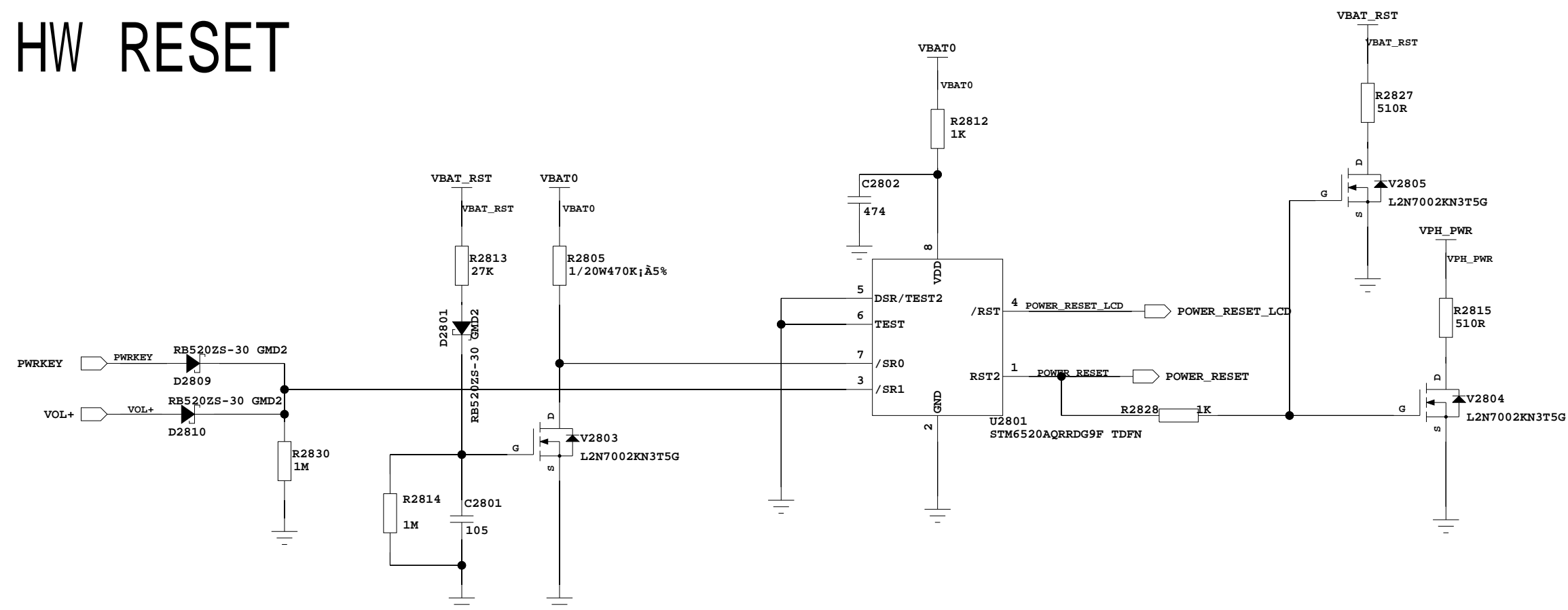


BQ24196 slave Address is 0x6B

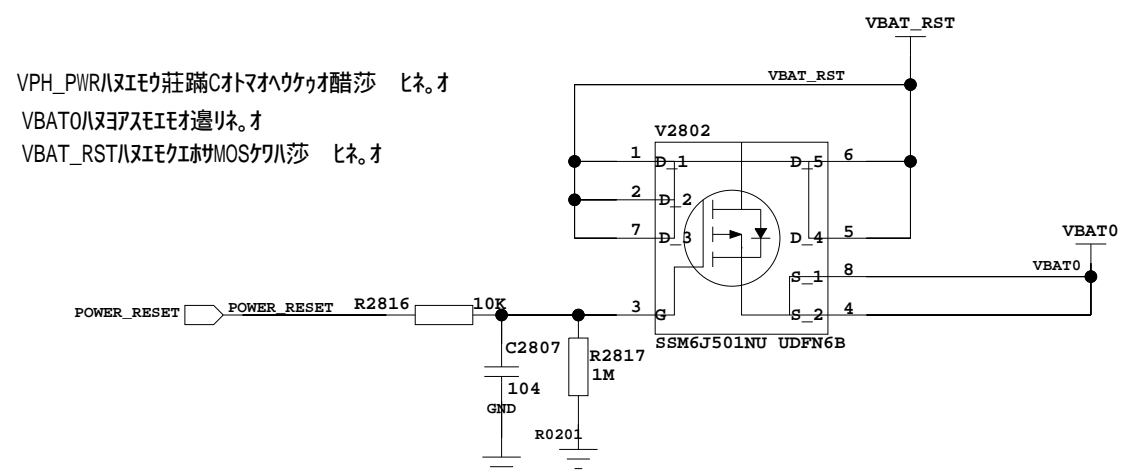
NVP&OVP



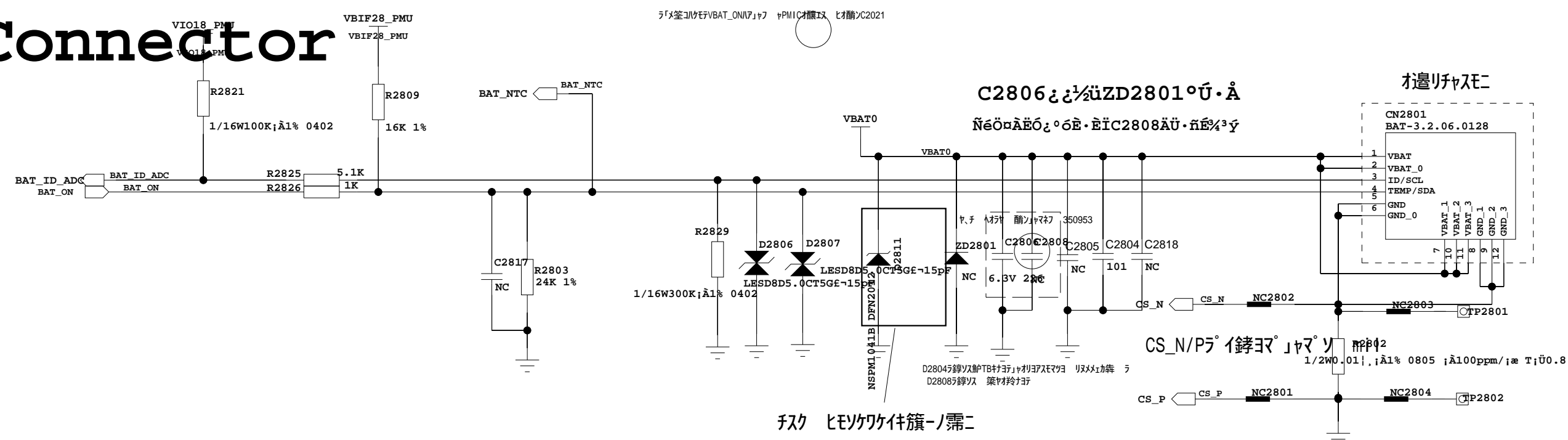
HW RESET

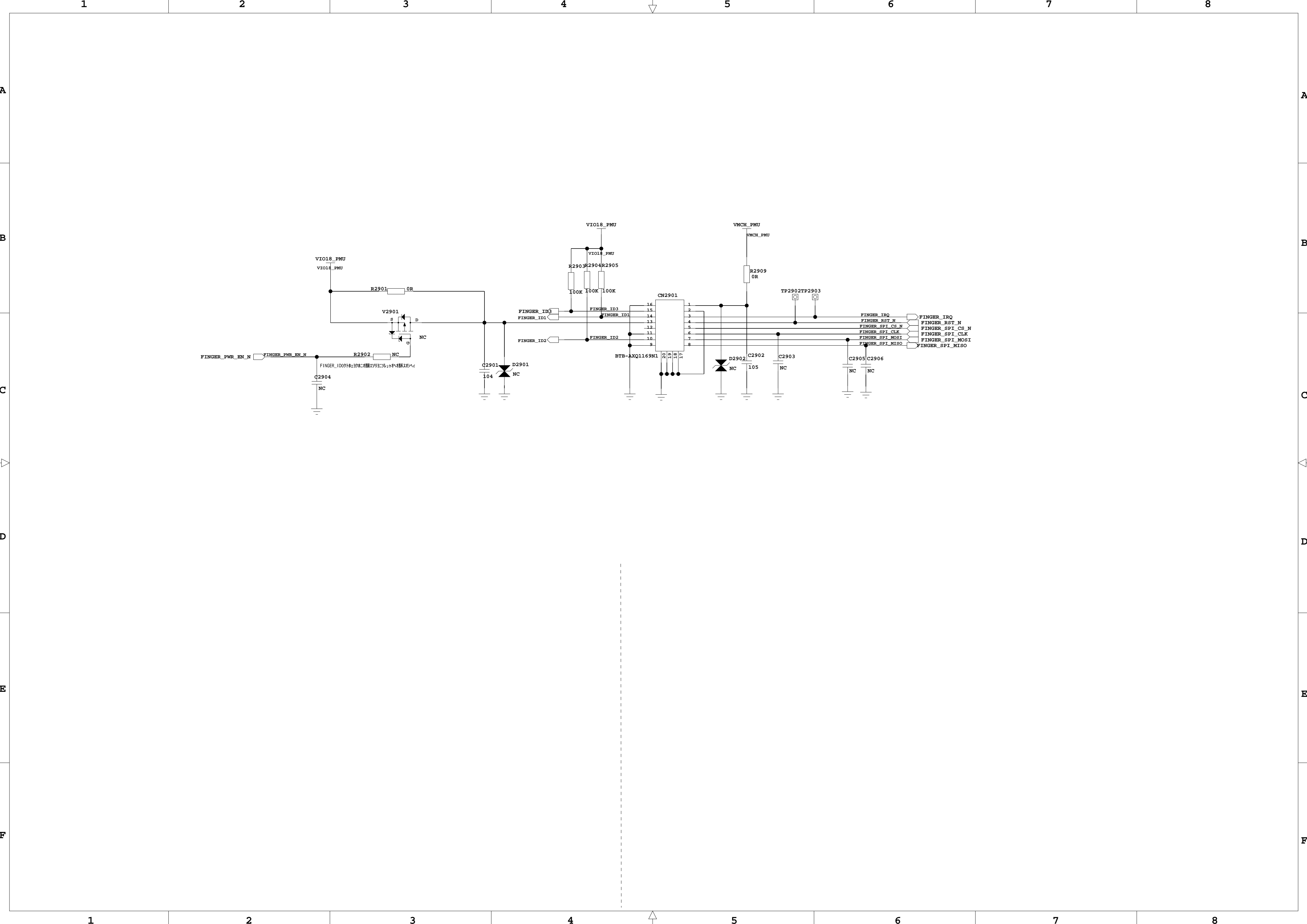


BAT_MOSFET



Battery Connector





A



A

B

C

C

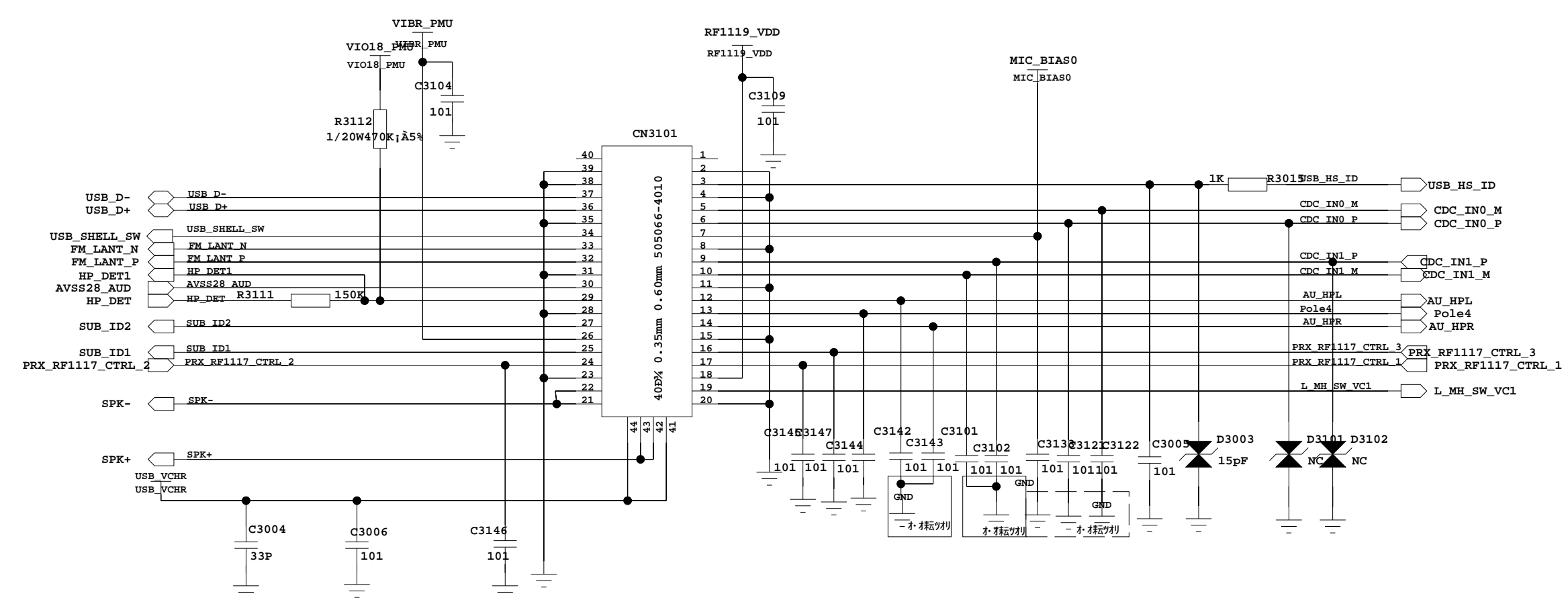


D

**F**

The diagram shows four test points labeled TP3016, TP3018, TP3019, and TP3020. Each test point is represented by a square symbol with a circle inside. TP3016, TP3018, and TP3019 are connected to a common ground line (indicated by a dashed line). TP3020 is connected to a separate ground point (indicated by a solid line).

FPC CONNECT BTB



RE

