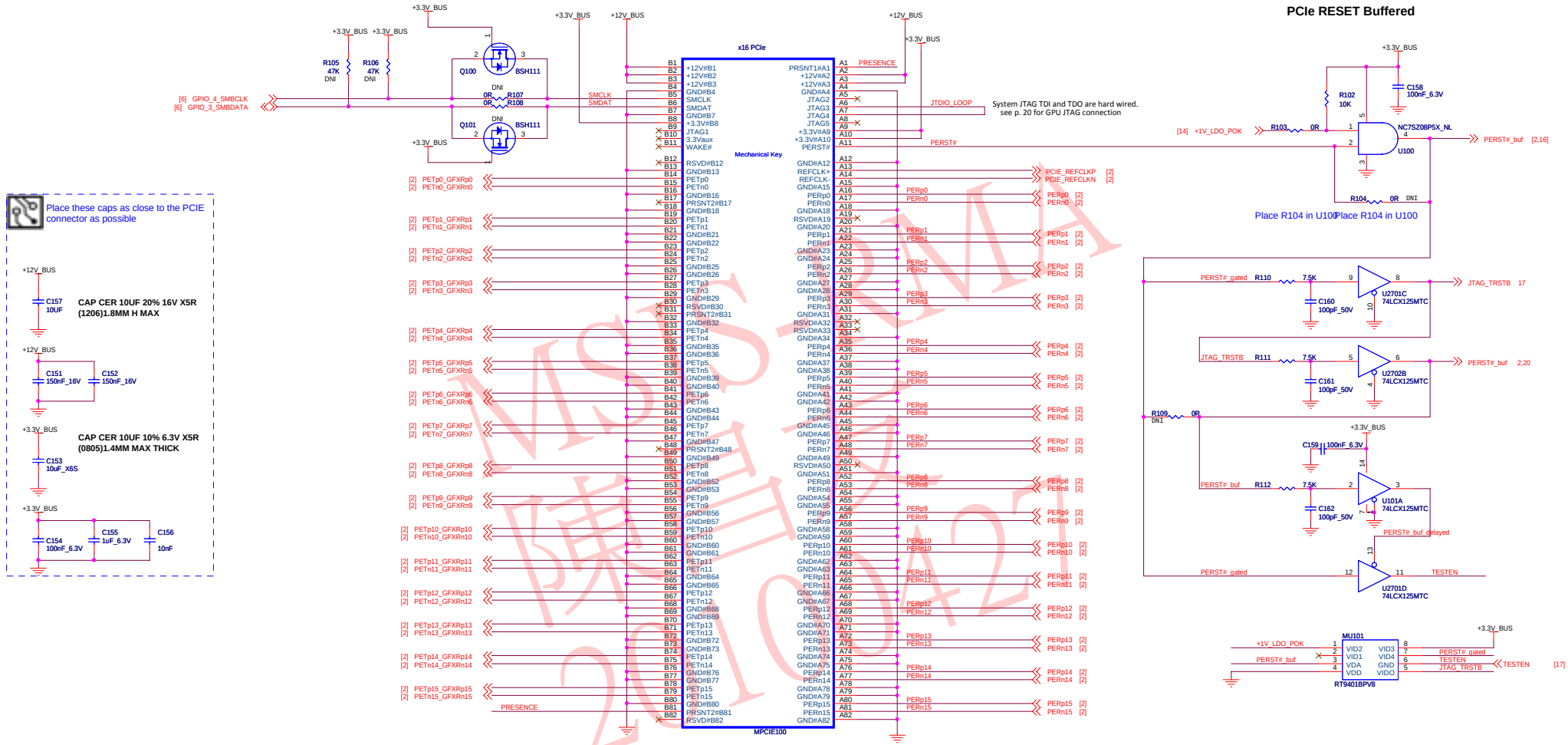
PCI-EXPRESS EDGE CONNECTOR

REDWOOD WOLVERINE



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(2) REDWOOD PCIe Interface

NOTE: Some of the PCIE testpoints will be available through vias on traces.

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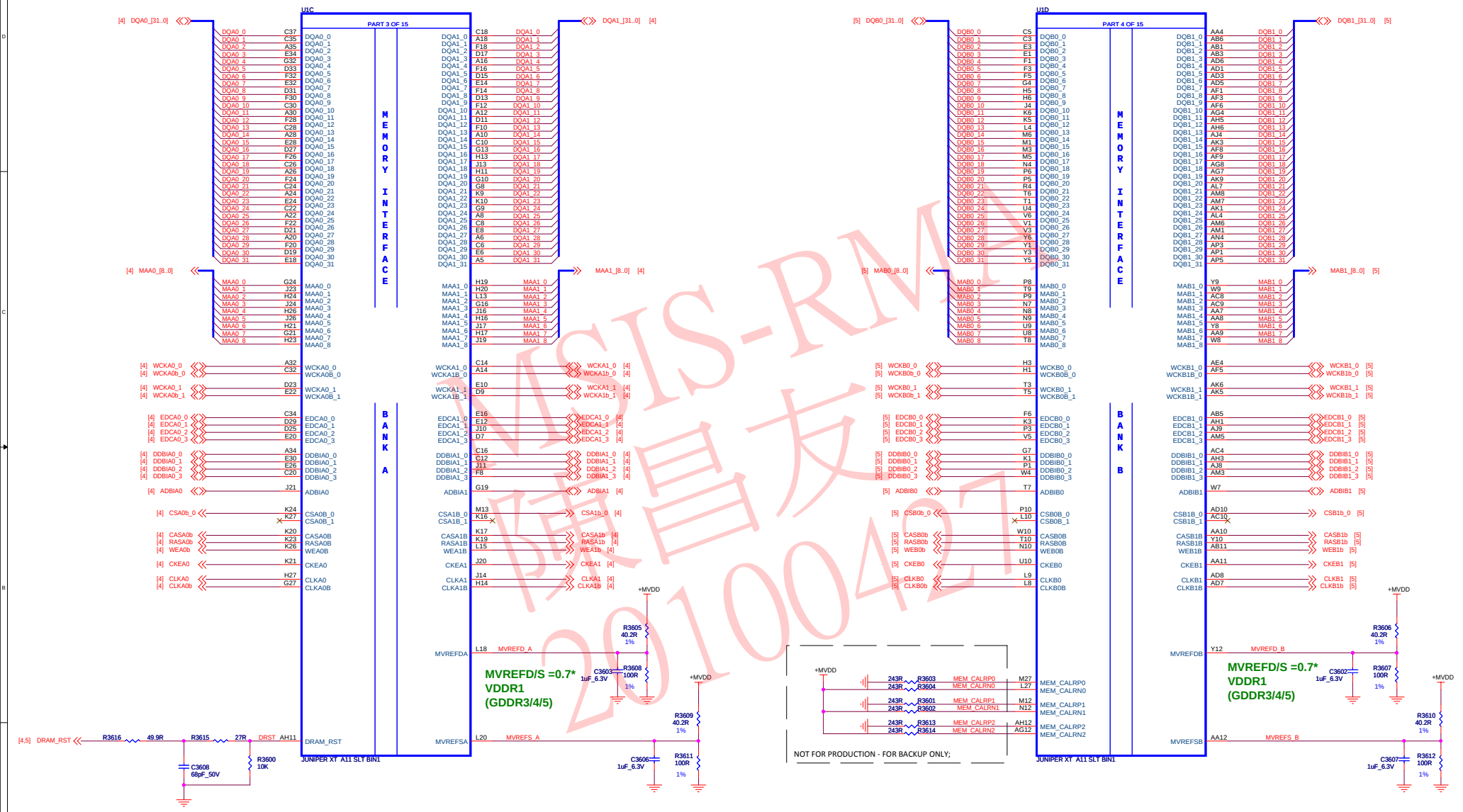
(3) REDWOOD MEM Interface Ch A&B



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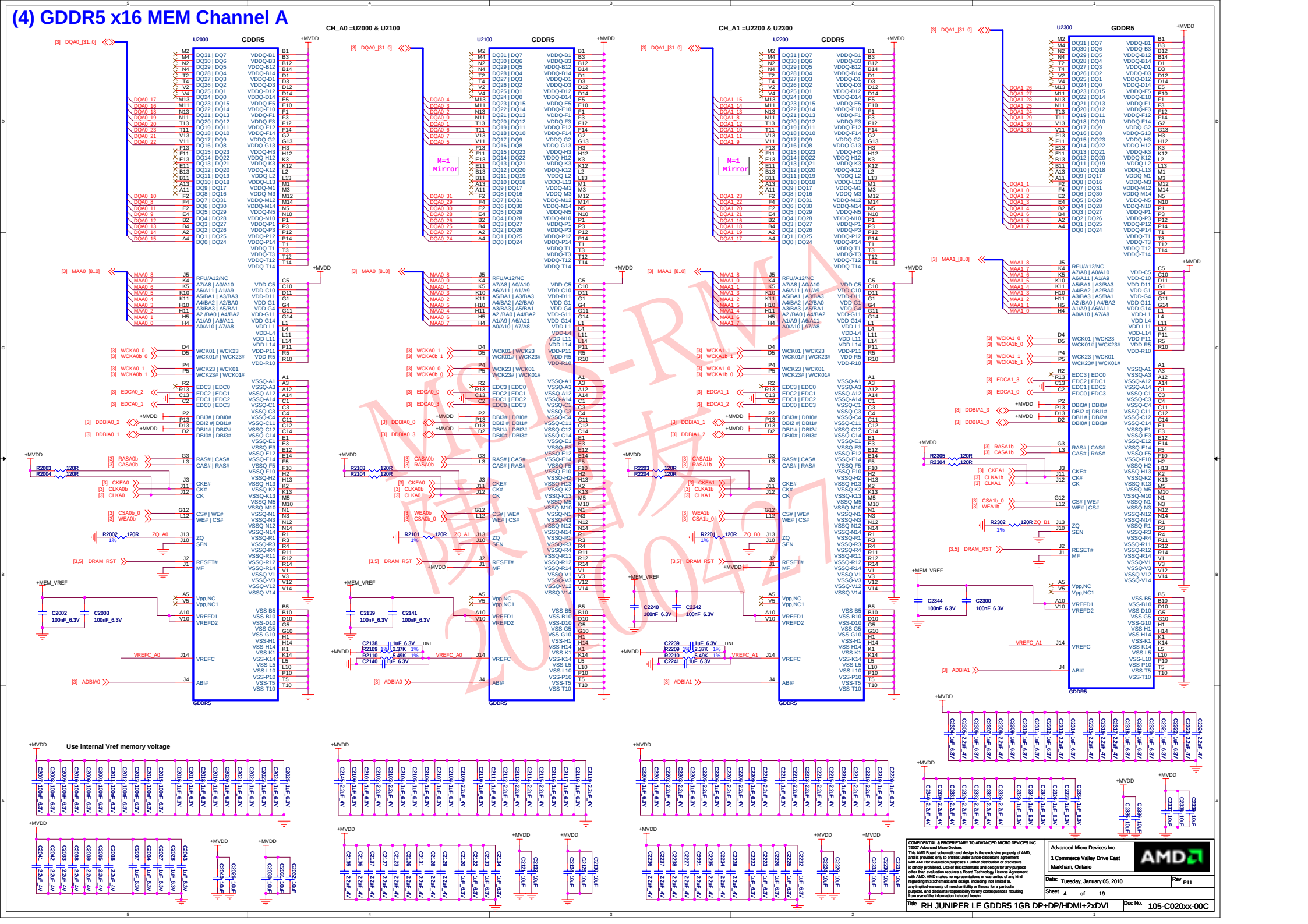
(4) GDDR5 x16 MEM Channel A



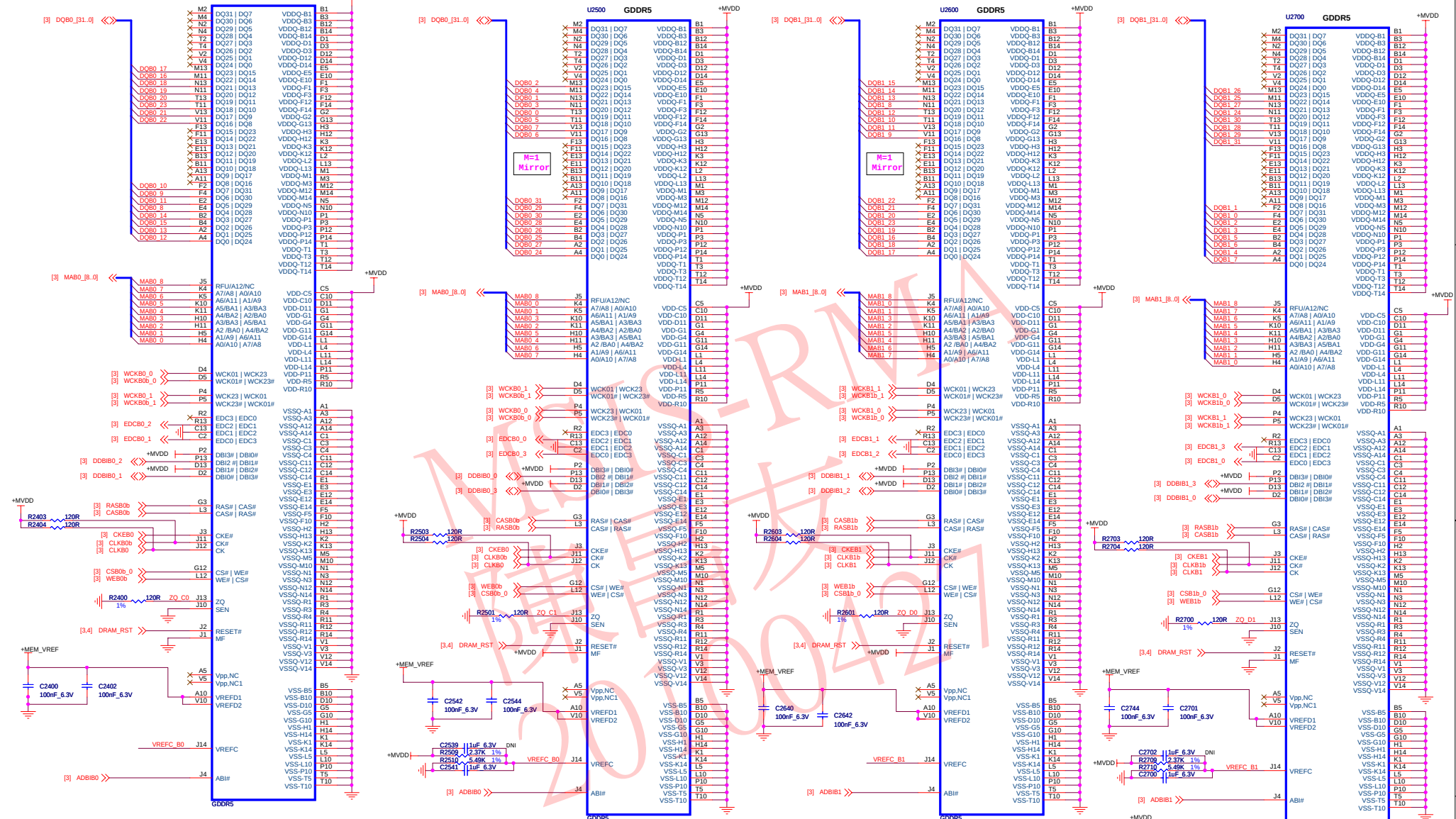
(5) GDDR5 x16 MEM Channel B

CH_B0 =U2400 & U2500

CH_B1 =U2600 & U2700

BOTTOM

TOP



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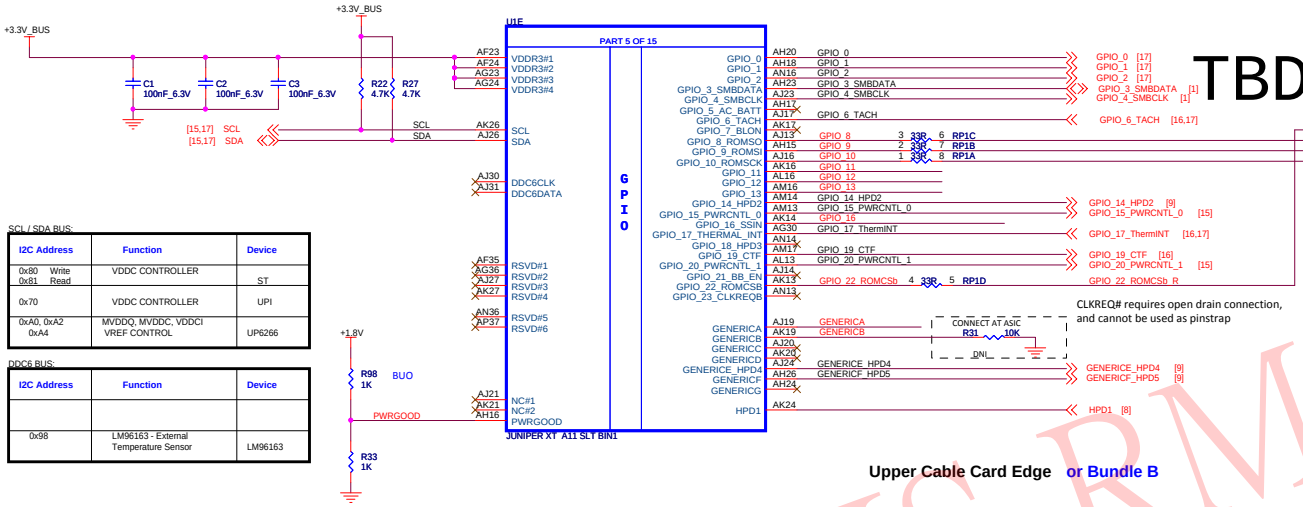
(06) REDWOOD GPIOs Strap CF XTAL OSC



SCL / SDA BUS:

I2C Address	Function	Device
0x80 Write 0x81 Read	VDDC CONTROLLER	ST
0x70	VDDC CONTROLLER	UPI
0xA0, 0xA2 0xA4	MVDDQ, MVDDC, VDDCI VREF CONTROL	UP6266

DDC6 BUS:

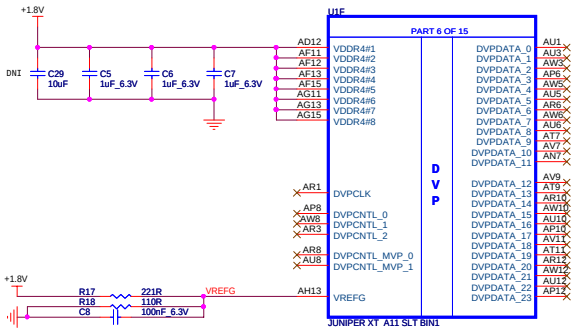
I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

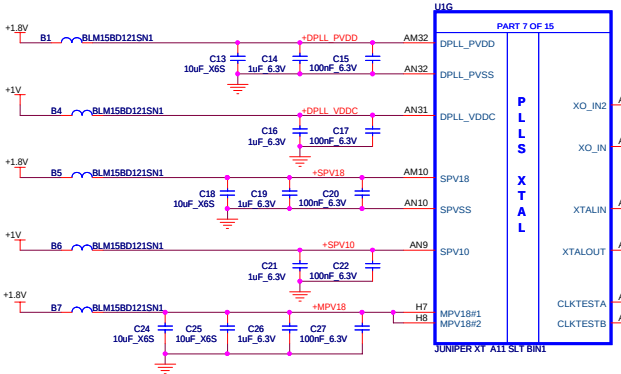
TBD

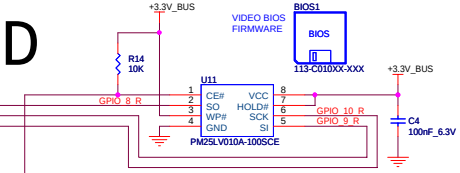
CLKREQ# requires open drain connection, and cannot be used as pinstrap

Upper Cable Card Edge or Bundle B

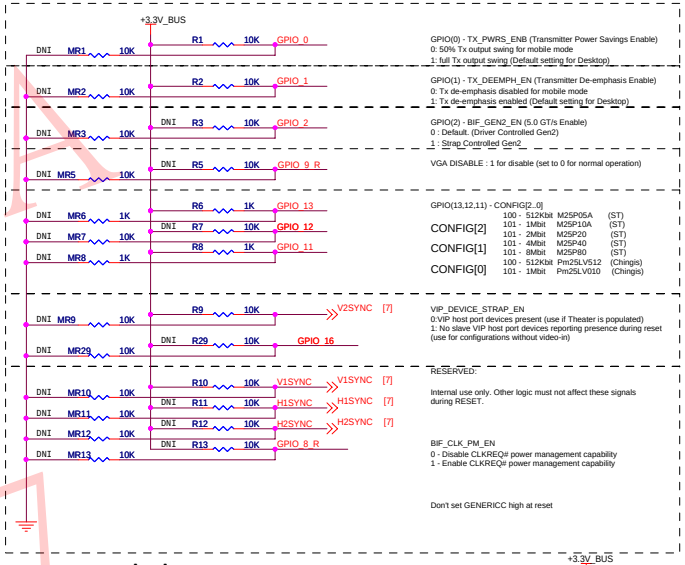
CrossFire Card-Edge

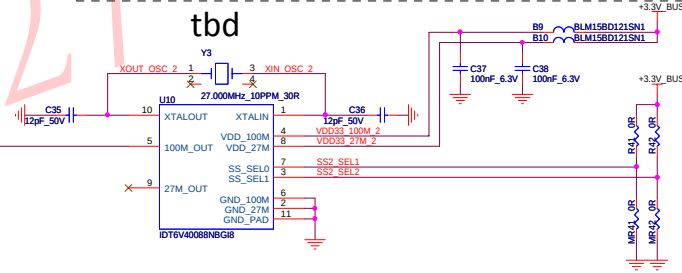


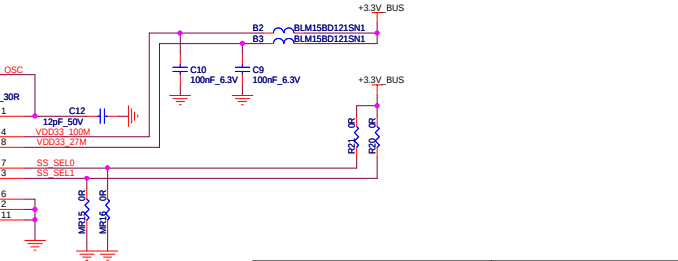




PIN BASED STRAPS







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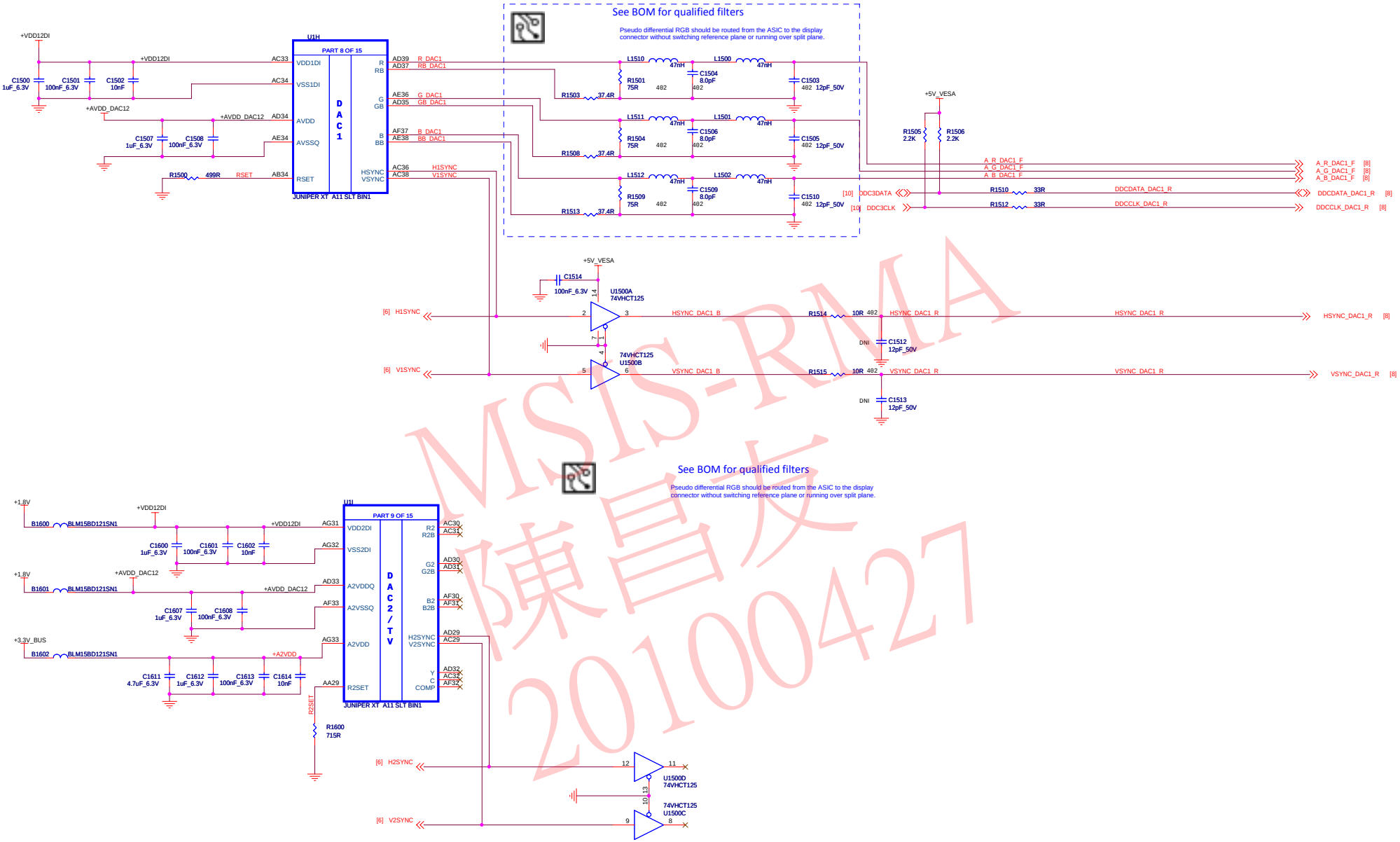
(07) REDWOOD DAC1 and DAC2



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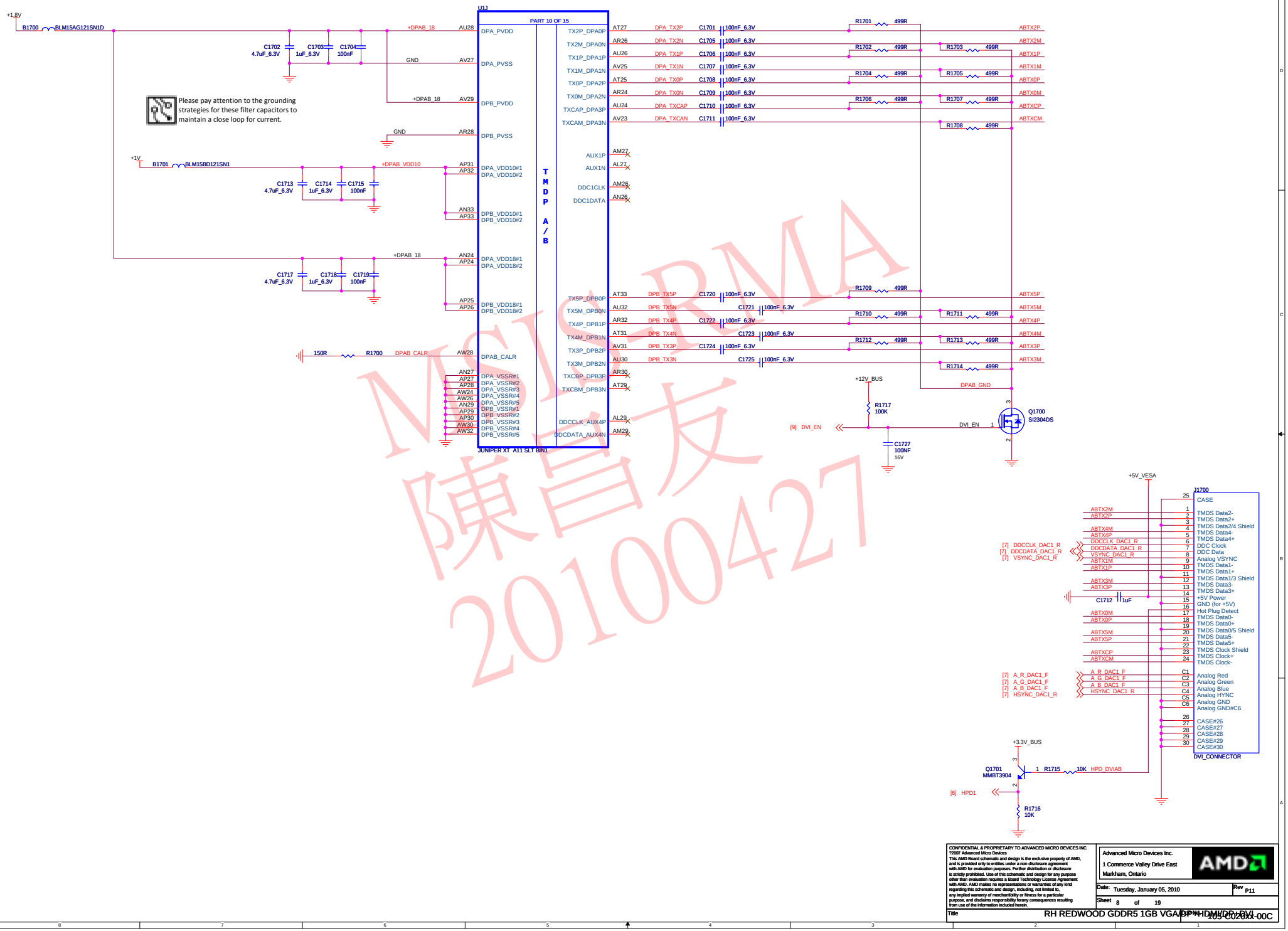
(08) REDWOOD TMDP A&B dDVI-I TOP



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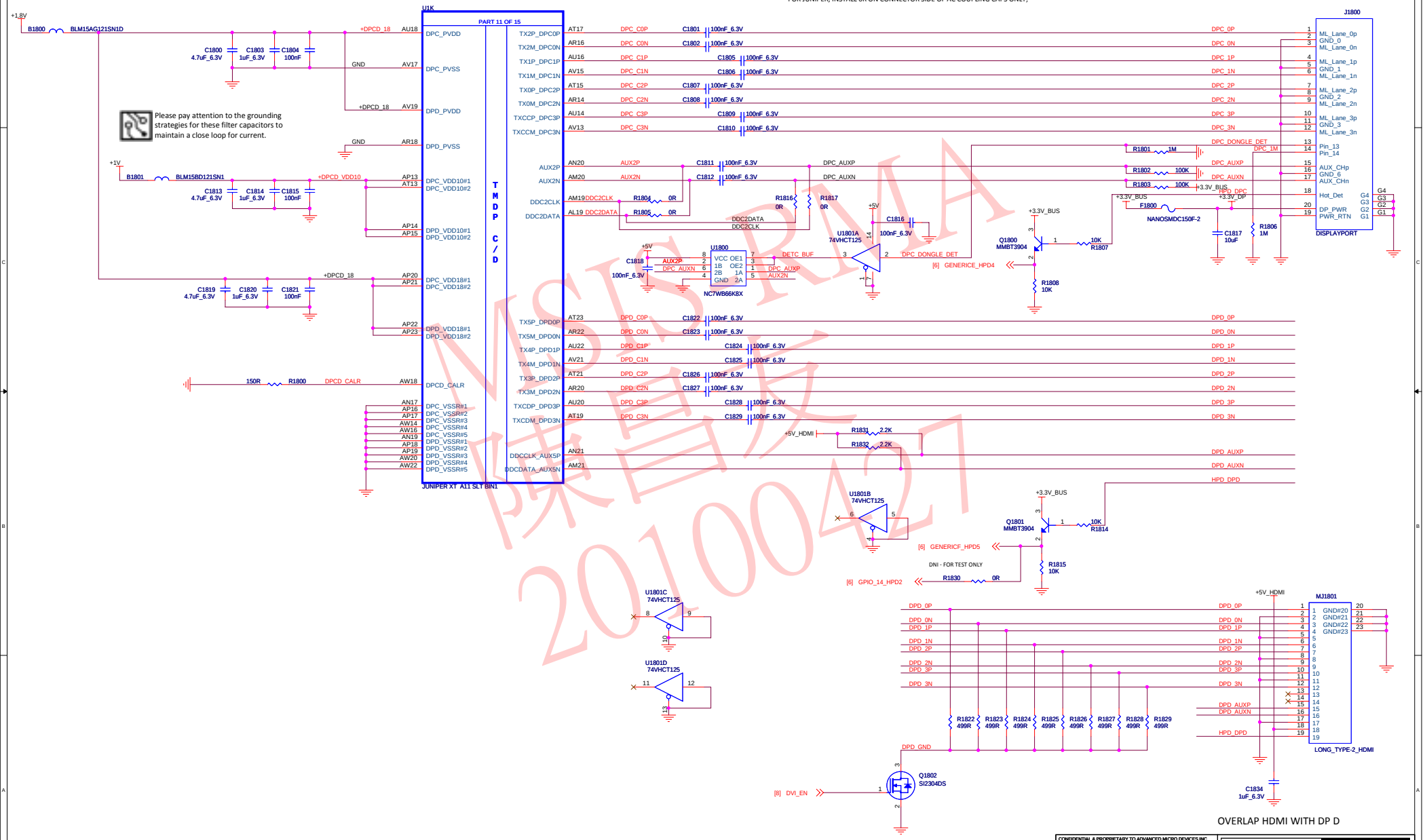
(09) REDWOOD Display Port C & Display Port/HDMI D



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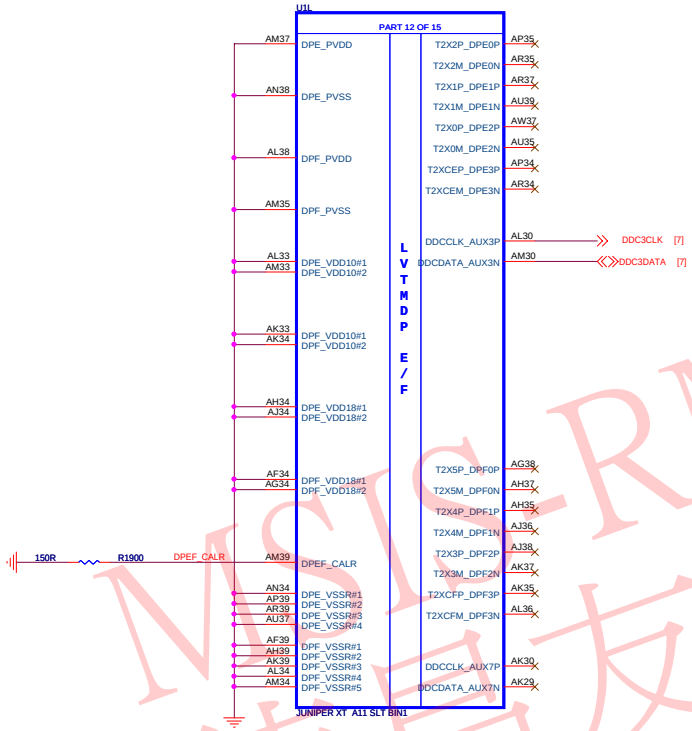
(10) REDWOOD LVTMDP E&F



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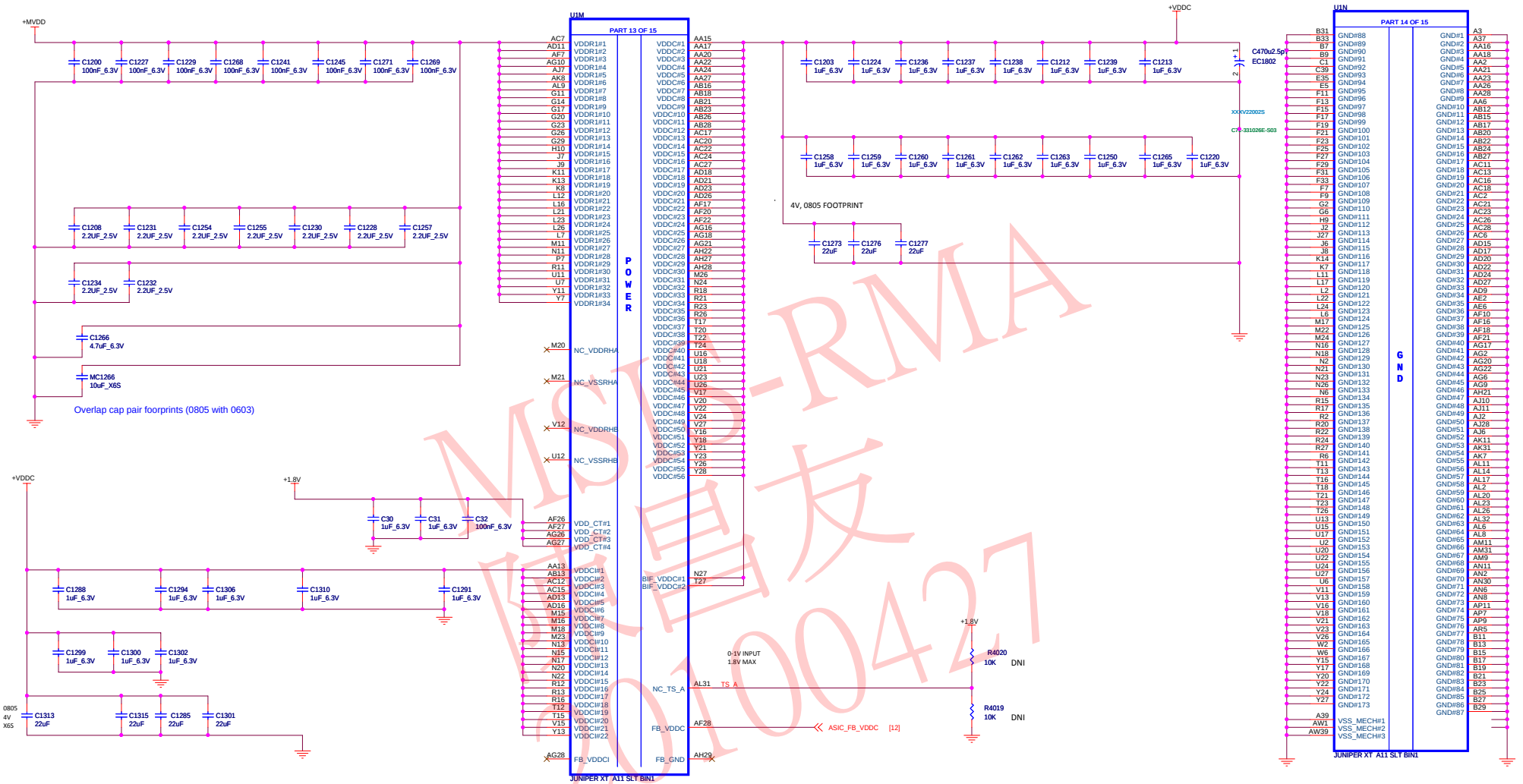
(11) REDWOOD Power & GND



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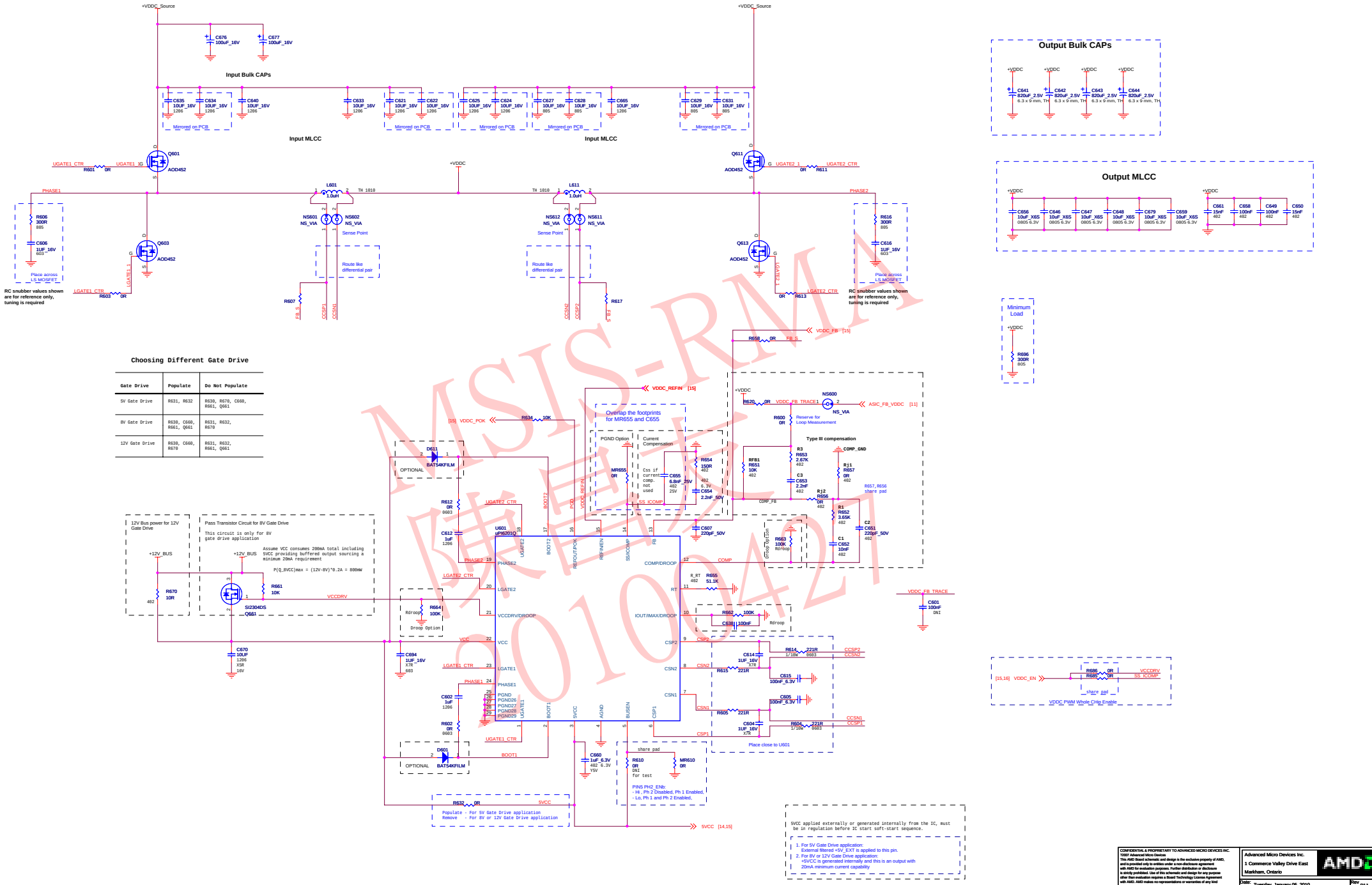
+VDDC_Source
Input Bulk CAPs
C676 100uF_16V
C677 100uF_16V
C635 10UF_16V 1206
C634 10UF_16V 1206
C640 10UF_16V 1206
C633 10UF_16V 1206
C621 10UF_16V 1206
C622 10UF_16V 1206
C625 10UF_16V 1206
C624 10UF_16V 1206
C627 10UF_16V 805
C629 10UF_16V 805
C655 10UF_16V 1206
C629 10UF_16V 805
C631 10UF_16V 805
Mirrored on PCB
Input MLCC
Q601 AOD452
Q611 AOD452
UGATE1_CTR
UGATE2_CTR
R601 0R
R611 0R
PHASE1
PHASE2
L601 1.0uH
L611 1.0uH
TH 1010
+VDDC
NS601 NS_VIA
NS602 NS_VIA
NS612 NS_VIA
NS611 NS_VIA
Sense Point
Route like differential pair
R606 300R 805
C606 1UF_16V 603
Place across LS MOSFET
Q603 AOD452
Q613 AOD452
LGATE1_CTR
LGATE2_CTR
R603 0R
R613 0R
R616 300R 805
C616 1UF_16V 603
RC snubber values shown are for reference only, tuning is required
R607
R617
FB_S
CCSP1
CCSN1
CCSN2
CCSP2
Output Bulk CAPs
C641 820uF_2.5V 6.3 x 9 mm, TH
C642 820uF_2.5V 6.3 x 9 mm, TH
C643 820uF_2.5V 6.3 x 9 mm, TH
C644 820uF_2.5V 6.3 x 9 mm, TH
Output MLCC
C656 10uF_X6S 0805 6.3V
C646 10uF_X6S 0805 6.3V
C647 10uF_X6S 0805 6.3V
C648 10uF_X6S 0805 6.3V
C679 10uF_X6S 0805 6.3V
C659 10uF_X6S 0805 6.3V
C661 15nF 402
C658 100nF 402
C649 100nF 402
C650 15nF 402
Minimum Load
R696 300R 805
Choosing Different Gate Drive
Gate Drive | Populate | Do Not Populate
5V Gate Drive | R631, R632 | R630, R670, C660, R661, Q661
8V Gate Drive | R630, C660, R661, Q661 | R631, R632, R670
12V Gate Drive | R630, C660, R670 | R631, R632, R661, Q661
12V Bus power for 12V Gate Drive
+12V_BUS
R670 10R
Pass Transistor Circuit for 8V Gate Drive
This circuit is only for 8V gate drive application
Assume VCC consumes 200mA total including SVCC providing buffered output sourcing a minimum 20mA requirement
P(Q_8VCC)max = (12V-8V)*0.2A = 800mW
R661 10K
SI2304DS Q661
VCCDRV
C670 10UF 1206 X5R 16V
C694 1UF_16V X7R 603
C612 1uF 1206
R612 0R 0603
D611 BAT54KFILM
OPTIONAL
D601 BAT54KFILM
C602 1uF 1206
R602 0R 0603
R664 100K
Rdroop
Droop Option
U601 isl96201Q
UGATE2
BOOT2
PVCC
REFOUT/POK
REFIN/EN
SS/COMP
FB
COMP/DROOP
VCCDRV/DROOP
VCC
LGATE2
PHASE2
LGATE1
PHASE1
PGND
PGND26
PGND27
PGND28
PGND29
UGATE1
BOOT1
SVCC
AGND
BUSEN
CSP1
RT
IOUT/IMAX/DROOP
CSP2
CSN2
CSN1
R_RT R655 51.1K
R662 100K
C638 100nF
R614 221R 1/10W 0603
C614 1UF_16V X7R
R615 221R
C615 100nF_6.3V
C605 100nF_6.3V
R605 221R
R604 221R 1/10W 0603
C604 1UF_16V X7R
Place close to U601
C660 1uF_6.3V 402 6.3V Y5V
R610 0R DNI for test
MR610 0R
share pad
PINS PH2_ENb:
- Hi , Ph 2 Disabled, Ph 1 Enabled.
- Lo, Ph 1 and Ph 2 Enabled.
R632 0R
SVCC
Populate - For 5V Gate Drive application
Remove - For 8V or 12V Gate Drive application
SVCC applied externally or generated internally from the IC, must be in regulation before IC start soft-start sequence.
1. For 5V Gate Drive application:
External filtered +5V_EXT is applied to this pin.
2. For 8V or 12V Gate Drive application:
+5VCC is generated internally and this is an output with 20mA minimum current capability
VDDC_REFIN [15]
VDDC_POK [15]
R634 10K
Overlap the footprints for MR655 and C655
PGND Option
Current Compensation
Css if current comp. not used
C655 6.8nF_25V
C654 2.2nF_50V
MR655 0R
R654 150R
SS_ICOMP
C607 220pF_50V
R620 0R
VDDC_FB_TRACE1
NS600 NS_VIA
ASIC_FB_VDDC [11]
R600 0R
Reserve for Loop Measurement
Type III compensation
RF81 R651 10K
R3 R653 2.67K
C3 C653 2.2nF
Rj1 R657 0R
Rj2 R656 0R
C2 C651 220pF_50V
R1 R652 3.65K
C1 C652 10nF
COMP_GND
COMP_FB
R657, R656 share pad
R663 100K Rdroop
Droop Option
VDDC_FB [15]
R658 0R FB_S
VDDC_FB_TRACE
C601 100nF DNI
[15,16] VDDC_EN
R686 0R
R685 0R
VCCDRV
SS_ICOMP
share pad
VDDC_PWM Whole Chip Enable
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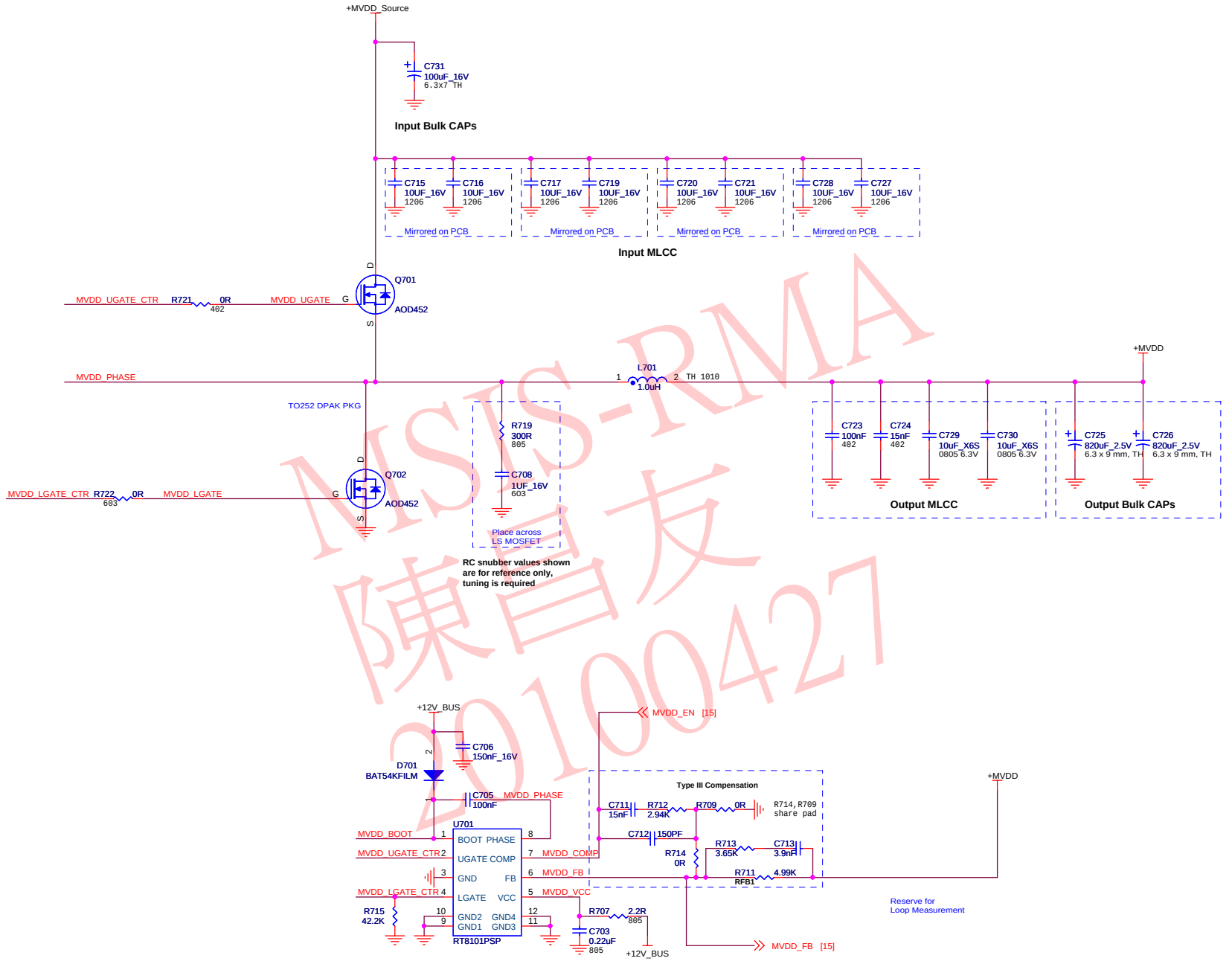

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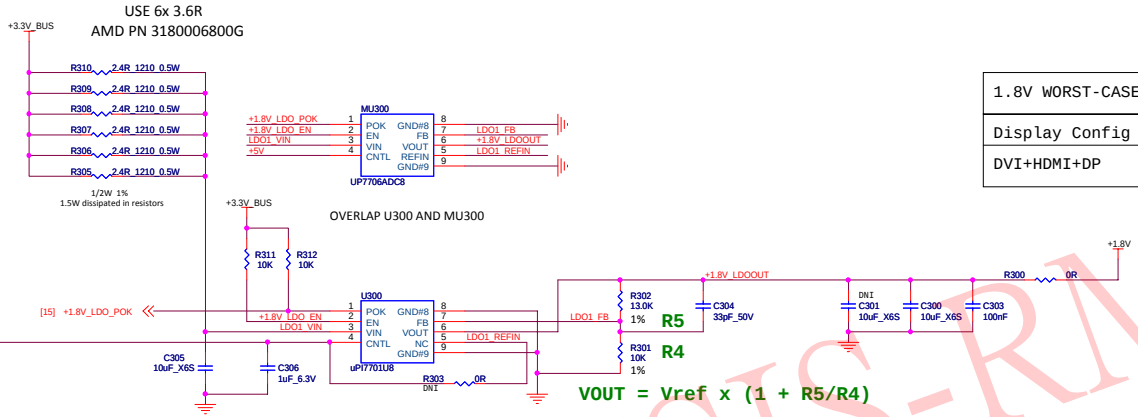
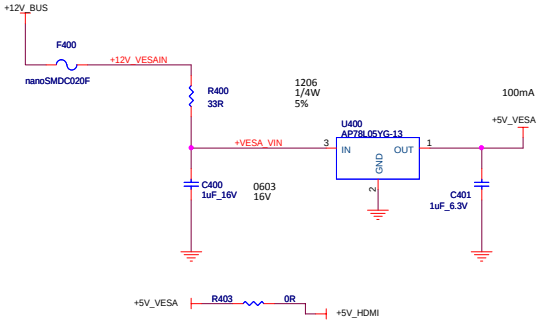
(15) Linear Regulators

Regulators for +5V, +5V_VESA and +5V_HDMI

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

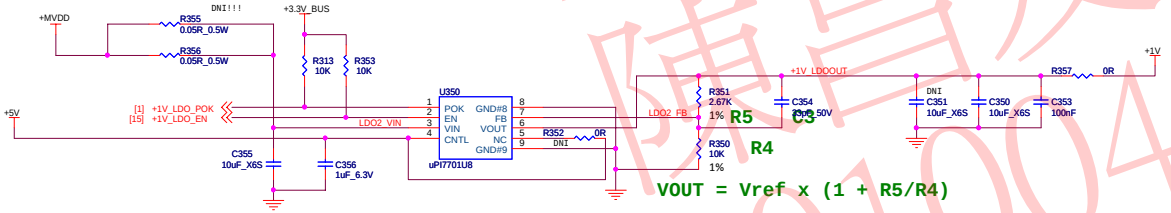


1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

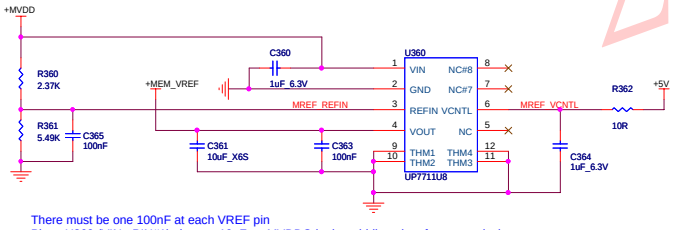


LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

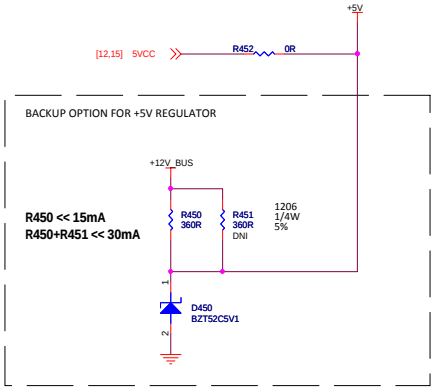
1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA



Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ



There must be one 100nF at each VREF pin
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices



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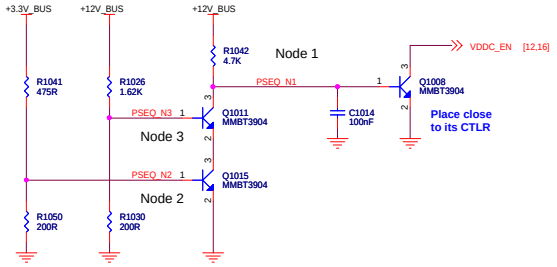
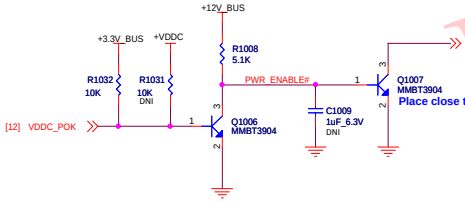
(16) Power Management - Power Gating and Dynamic Voltage Control

12V_BUS & 3V3_BUS POWER SEQUENCING



POWER SEQUENCING CIRCUIT

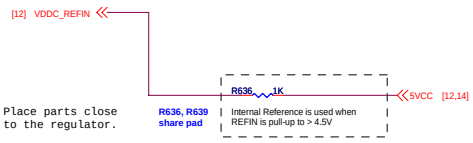


VDDC Reference Voltage Selection

VDDC Vref Mode Selection

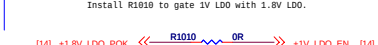
Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

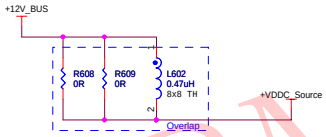
I2C VOLTAGE REFERENCE FOR VDDC (not for production)

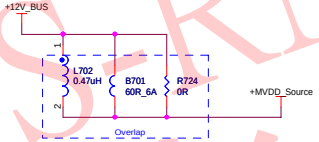


I2C ADDRESS: A4

Install R1010 to gate 1V LDO with 1.8V LDO.





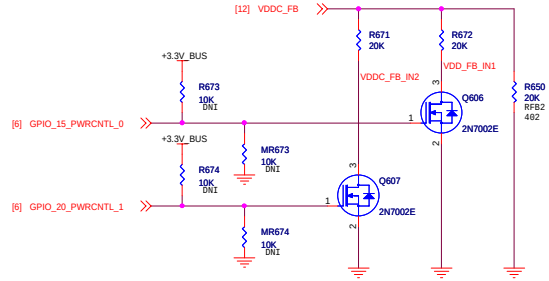


MVDD Low Side Divider

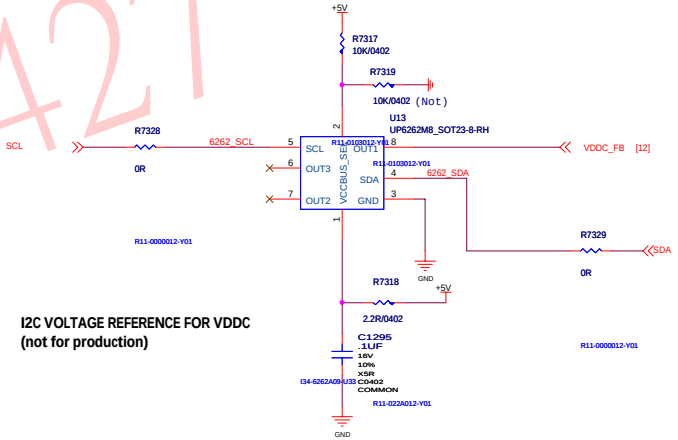
VDDC Low Side Divider

R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.

- Hi-Side Divider R651 is Fixed to 5.11K
- Vo = Vref * (1 + R651 / R650)
- Vref = 0.6V



I2C VOLTAGE REFERENCE FOR VDDC (not for production)



I2C ADDRESS: A4

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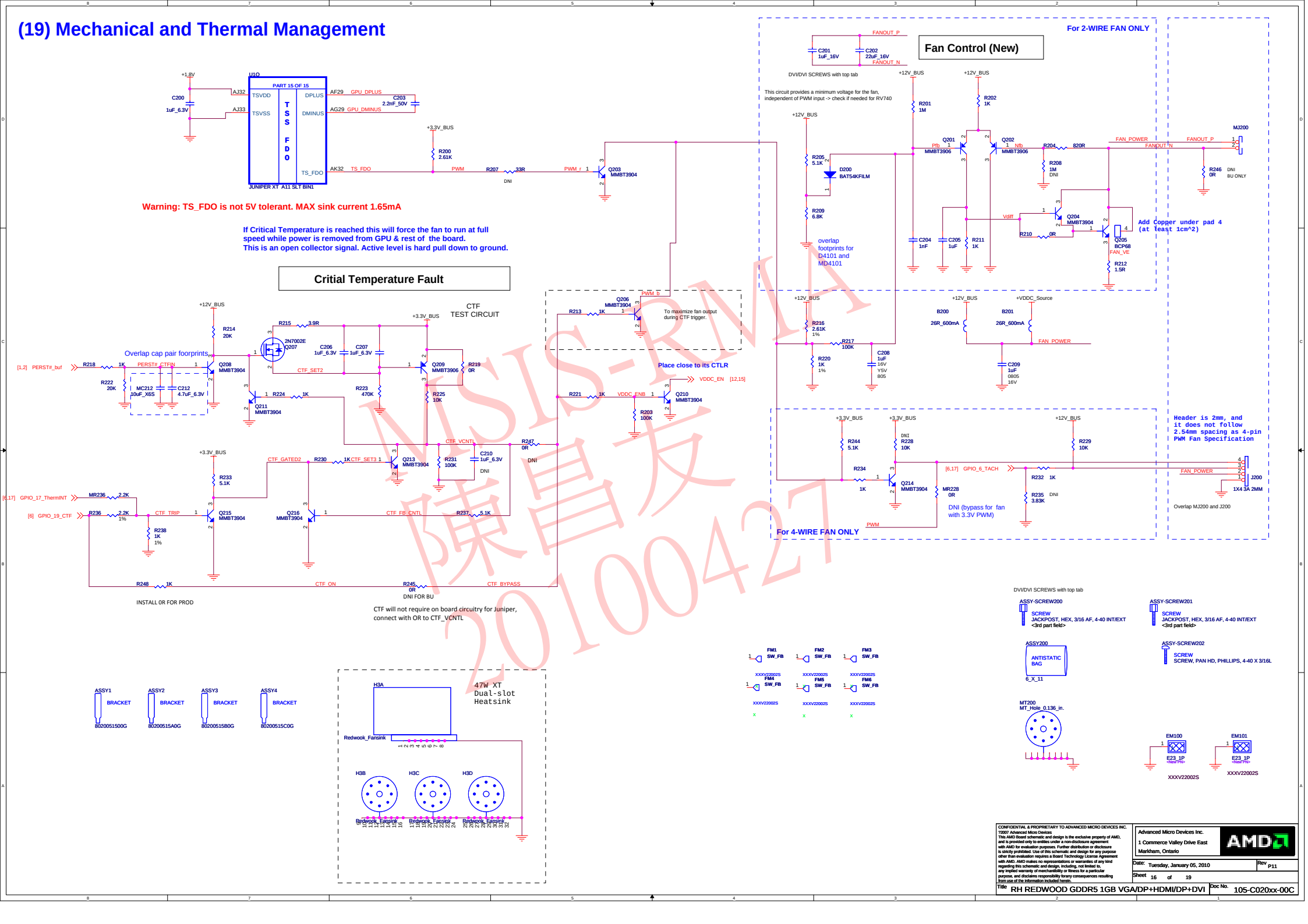
(19) Mechanical and Thermal Management



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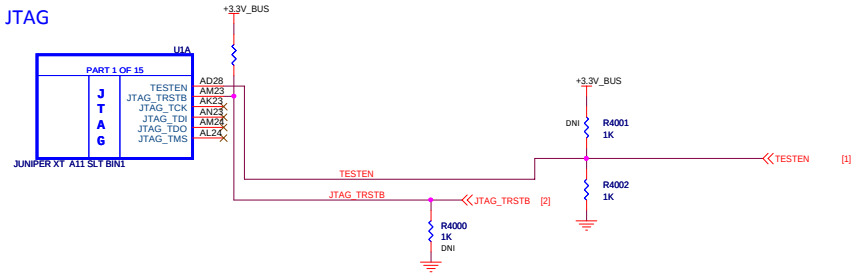
(19) Debug Circuits



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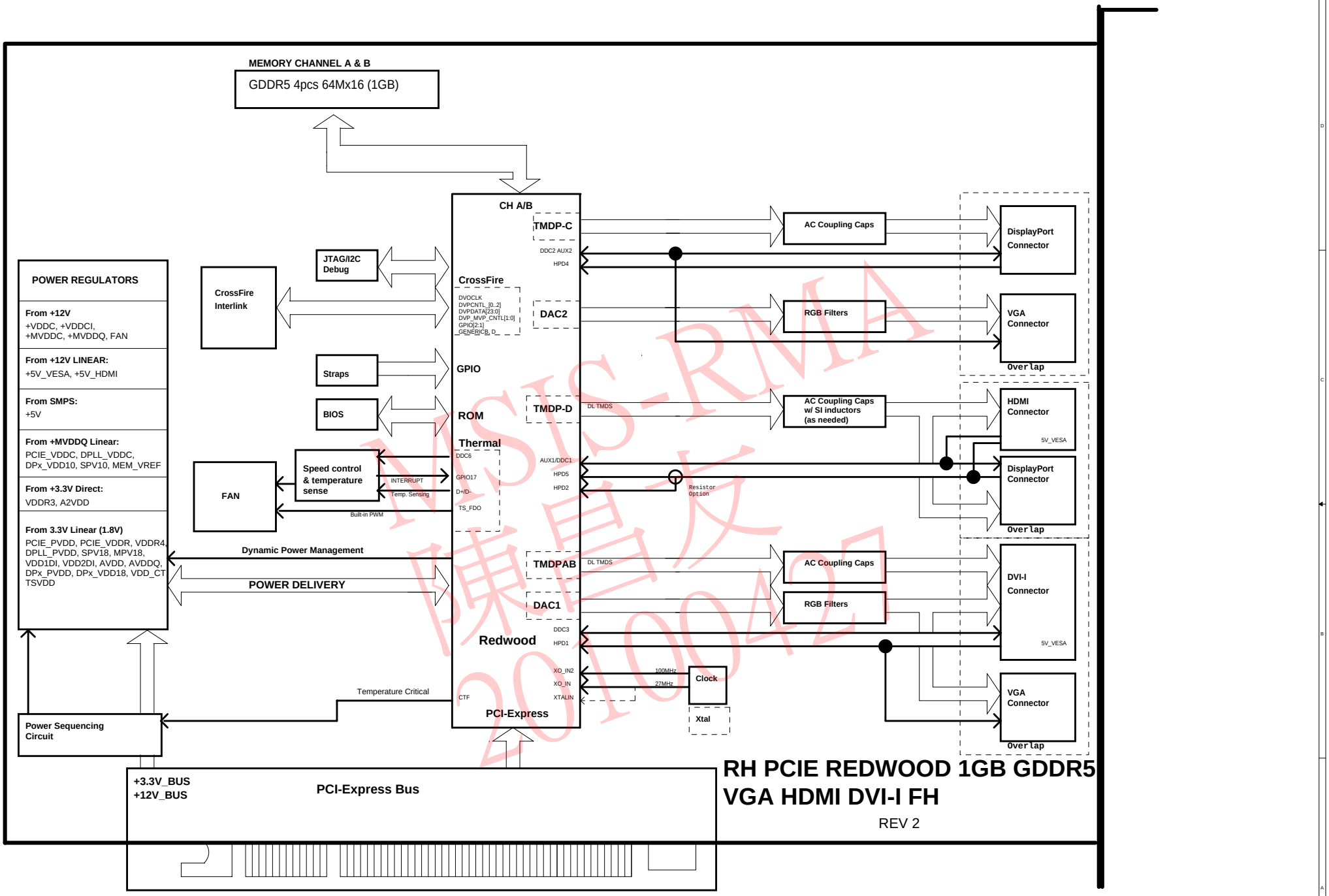

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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev P11

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/05/08	
01	00B	2009/08/20	
02	00C	2009/09/28	REDWOOD XT GDDR5 1GB - Initial Release