



PCB layout diagram for the NVIDIA 600-10684-base-100 C board, showing the placement of components and the connection of signals.

The diagram includes the following components and connections:

- Power and Ground:** 1.2V, 1.8V, 3.3V, 5.0V, and GND planes. Power planes are labeled PE1, PE2, PE3, PE4, PE5, PE6, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PE16, PE17, PE18, PE19, PE20, PE21, PE22, PE23, PE24, PE25, PE26, PE27, PE28, PE29, PE30, PE31, PE32, PE33, PE34, PE35, PE36, PE37, PE38, PE39, PE40, PE41, PE42, PE43, PE44, PE45, PE46, PE47, PE48, PE49, PE50, PE51, PE52, PE53, PE54, PE55, PE56, PE57, PE58, PE59, PE60, PE61, PE62, PE63, PE64, PE65, PE66, PE67, PE68, PE69, PE70, PE71, PE72, PE73, PE74, PE75, PE76, PE77, PE78, PE79, PE80, PE81, PE82, PE83, PE84, PE85, PE86, PE87, PE88, PE89, PE90, PE91, PE92, PE93, PE94, PE95, PE96, PE97, PE98, PE99, PE100, PE101, PE102, PE103, PE104, PE105, PE106, PE107, PE108, PE109, PE110, PE111, PE112, PE113, PE114, PE115, PE116, PE117, PE118, PE119, PE120, PE121, PE122, PE123, PE124, PE125, PE126, PE127, PE128, PE129, PE130, PE131, PE132, PE133, PE134, PE135, PE136, PE137, PE138, PE139, PE140, PE141, PE142, PE143, PE144, PE145, PE146, PE147, PE148, PE149, PE150, PE151, PE152, PE153, PE154, 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ASSEMBLY	
PAGE DETAIL	PCI-EXPRESS INTERFACE

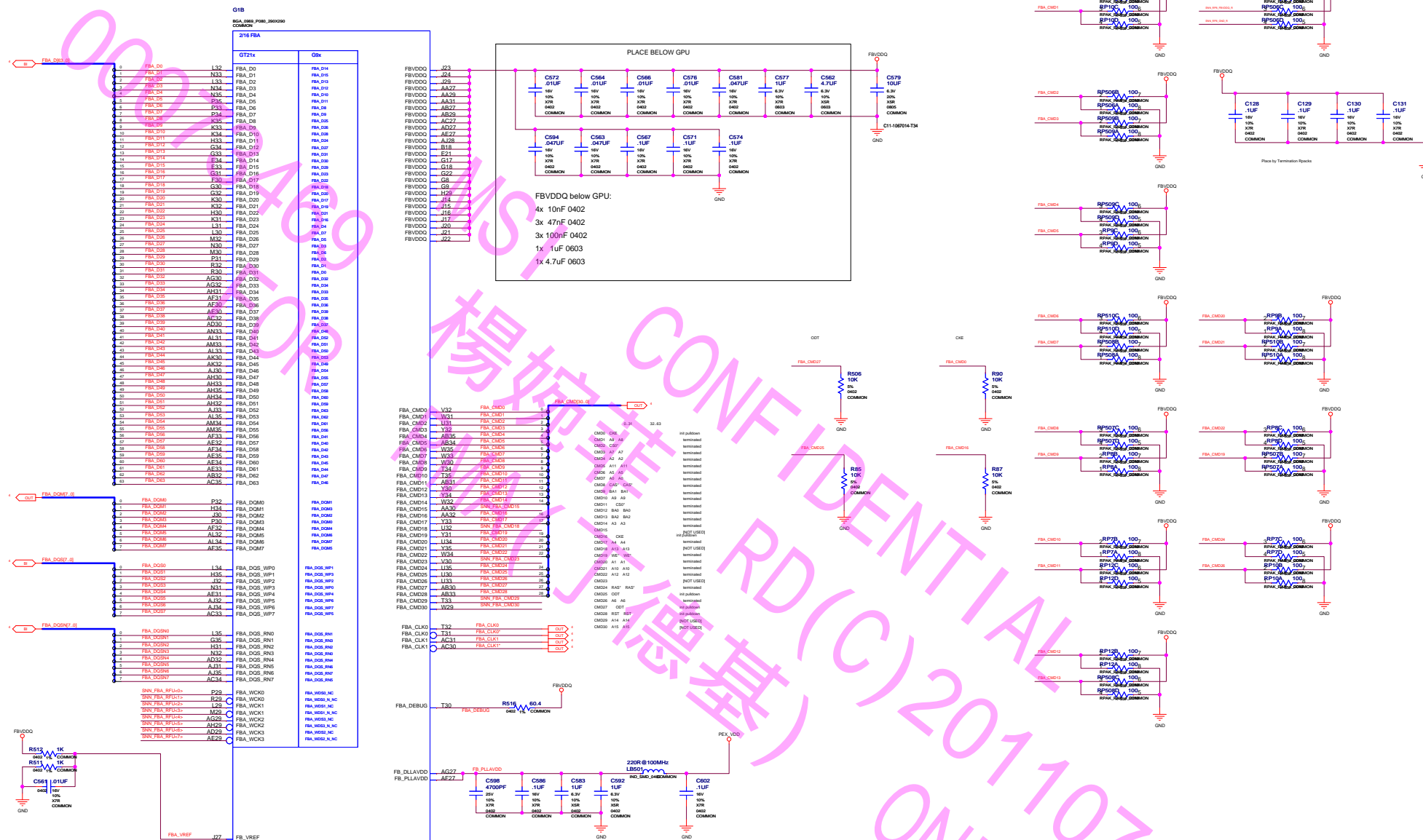
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PAGE DETAIL	PCI-EXPRESS INTERFACE

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NAME		DATE	13-FEB-2009

## PARTITION A FRAME BUFFER INTERFACE



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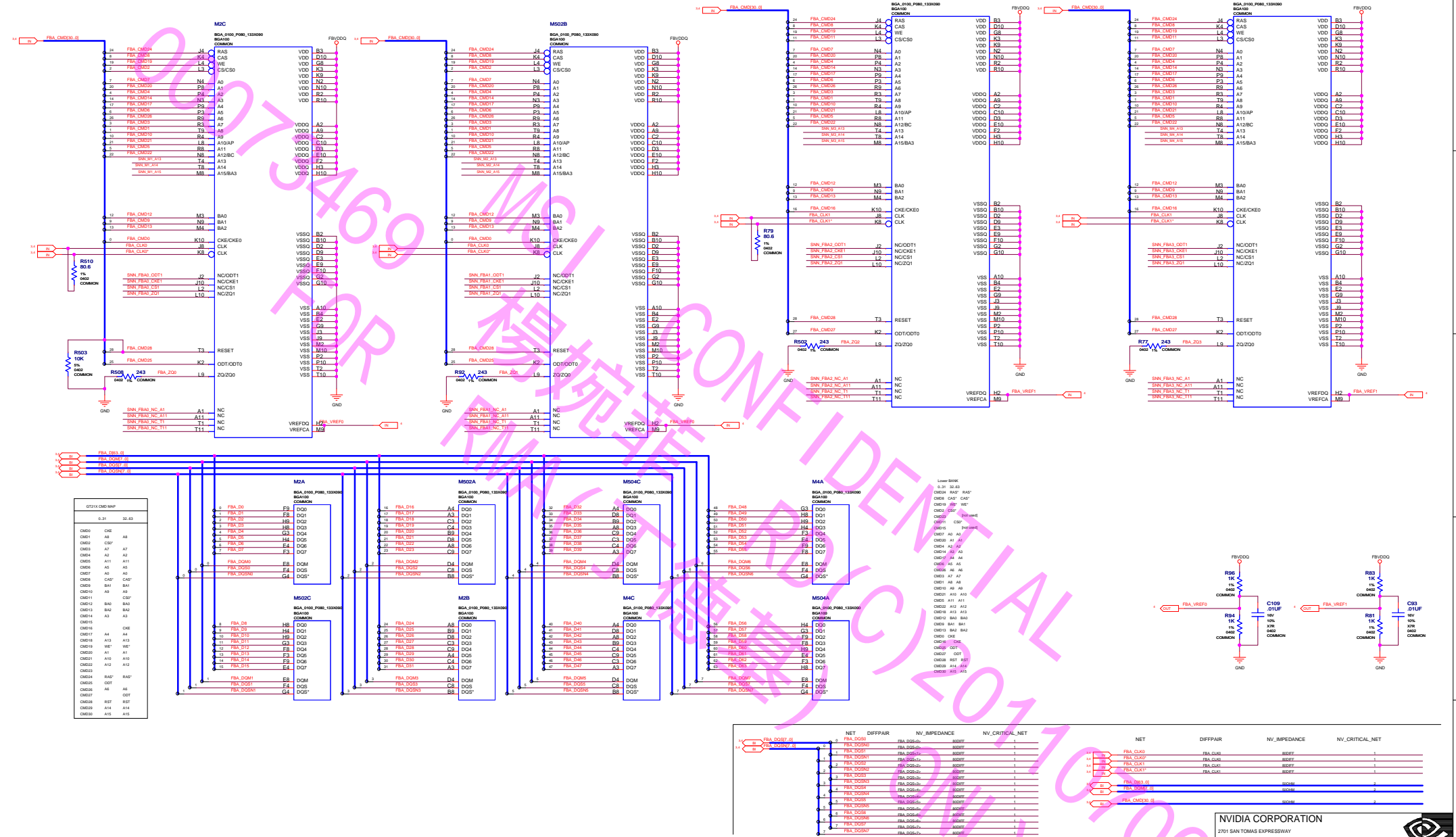


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## PARTITION A MEMORY



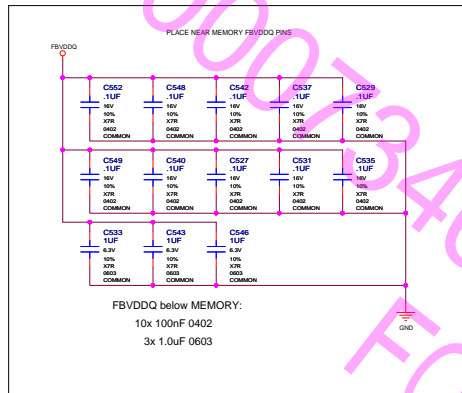
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PAGE DETAIL	PARTITION A MEMORIES

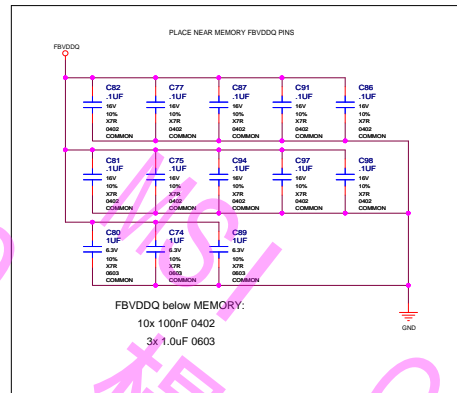
<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
<b>NV_PN</b>		<b>600-10684-base-100 C</b>	
<b>ID</b>		<b>PAGE</b>	
<b>NAME</b>		<b>DATE</b>	13-FEB-2009

## FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS

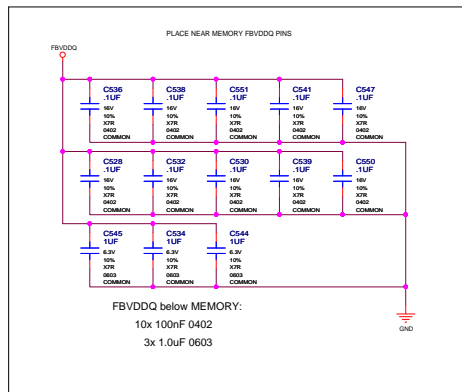
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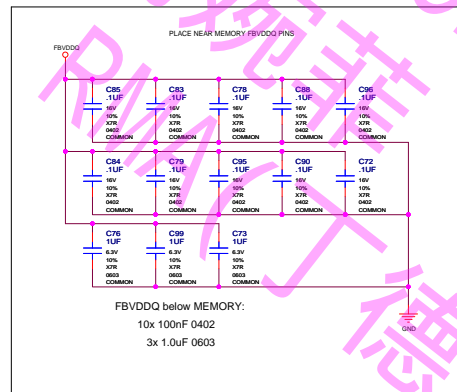
Decoupling for FBA 16..31



Decoupling for FBA 32..47



## Decoupling for FBA 48..63



NVVDD under GPU:

4x 0.01uF 0402 X7R

2x 0.047uF 0402 X7R

1x 0.1uF 0402 X7R

4x 1.0uF 0402 X5R

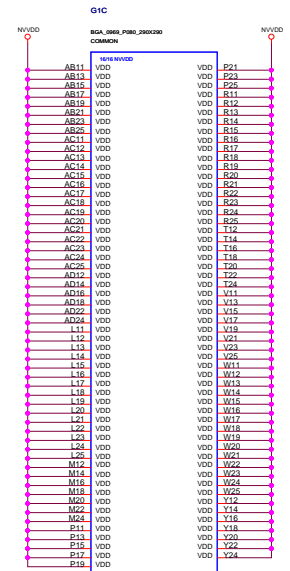
1x 2.2uF 0402 X5R  
2x 10uF 0805 X5R

2X 100F 0805 X5R

100

100

# A.



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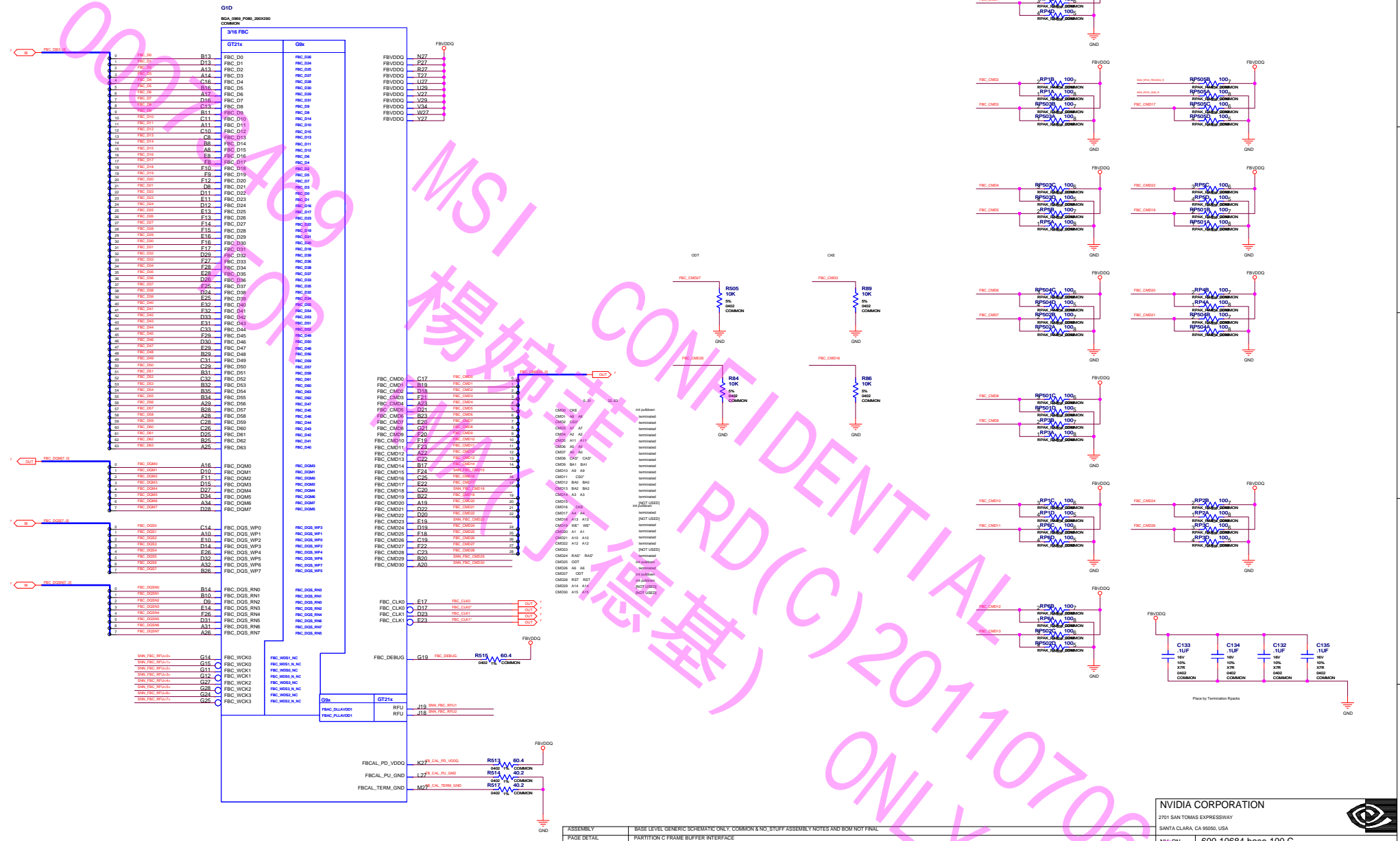
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100%

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA DECOUPLING CAPS & NVDD DECOUPLING CAPS

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## PARTITION C FRAME BUFFER INTERFACE



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## PARTITION C MEMORY



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PLACE NEAR MEMORY FBVDDQNS

FBVDDQ

C124 1uF 16V X7E 0402 COMMON

C116 1uF 16V X7E 0402 COMMON

C100 1uF 16V X7E 0402 COMMON

C103 1uF 16V X7E 0402 COMMON

C122 1uF 16V X7E 0402 COMMON

C114 1uF 16V X7E 0402 COMMON

C104 1uF 16V X7E 0402 COMMON

C110 1uF 16V X7E 0402 COMMON

C106 1uF 16V X7E 0402 COMMON

C118 1uF 16V X7E 0402 COMMON

C127 1uF 3.3V X7E 0803 COMMON

C112 1uF 3.3V X7E 0803 COMMON

C123 1uF 3.3V X7E 0803 COMMON

FBVDDQ below MEMORY:

10x 100nF 0402

3x 1.0uF 0603

GND

FBVDDQ

PLACE NEAR MEMORY FBVDDQ PINS

C502 1uF 10% 0805 COMMON

C507 1uF 10% 0805 COMMON

C517 1uF 10% 0805 COMMON

C518 1uF 10% 0805 COMMON

C522 1uF 10% 0805 COMMON

C503 1uF 10% 0805 COMMON

C506 1uF 10% 0805 COMMON

C508 1uF 10% 0805 COMMON

C513 1uF 10% 0805 COMMON

C515 1uF 10% 0805 COMMON

C510 1uF 10% 0805 COMMON

C512 1uF 10% 0805 COMMON

C524 1uF 10% 0805 COMMON

FBVDDQ below MEMORY:

10x 100nF 0402

3x 1.0uF 0603

GND

PLANE NEAR MEMORY FBVDDQ PINS

Capacitor	Value	Voltage	Tolerance	Package	Common
C115	1.0μF	18V	±10%	X7R	COMMON
C121	1.0μF	18V	±10%	X7R	COMMON
C107	1.0μF	18V	±10%	X7R	COMMON
C102	1.0μF	18V	±10%	X7R	COMMON
C119	1.0μF	18V	±10%	X7R	COMMON
C105	1.0μF	18V	±10%	X7R	COMMON
C117	1.0μF	18V	±10%	X7R	COMMON
C111	1.0μF	18V	±10%	X7R	COMMON
C130	1.0μF	18V	±10%	X7R	COMMON
C101	1.0μF	18V	±10%	X7R	COMMON
C113	1.0μF	6.3V	±10%	X7R	COMMON
C125	1.0μF	6.3V	±10%	X7R	COMMON
C126	1.0μF	6.3V	±10%	X7R	COMMON

FBVDDQ below MEMORY:  
 10x 100nF 0402  
 3x 1.0uF 0603

GND

[illegible]BGA\_0069\_P060\_200X200  
COMMON

1916 GND		
AA11	GND	GND E15
AA12	GND	GND E16
AA13	GND	GND E24
AA14	GND	GND E27
AA15	GND	GND E30
AA16	GND	GND E31
AA17	GND	GND E32
AA18	GND	GND E33
AA19	GND	GND E34
AA20	GND	GND E35
AA21	GND	GND E36
AA22	GND	GND E37
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AA190	GND	GND E205
AA191	GND	GND E206
AA192	GND	GND E207
AA193	GND	GND E208
AA194	GND	GND E209
AA195	GND	GND E210
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AA441	GND	GND E456
AA442	GND	GND E457

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC DECOUPLING CAPS

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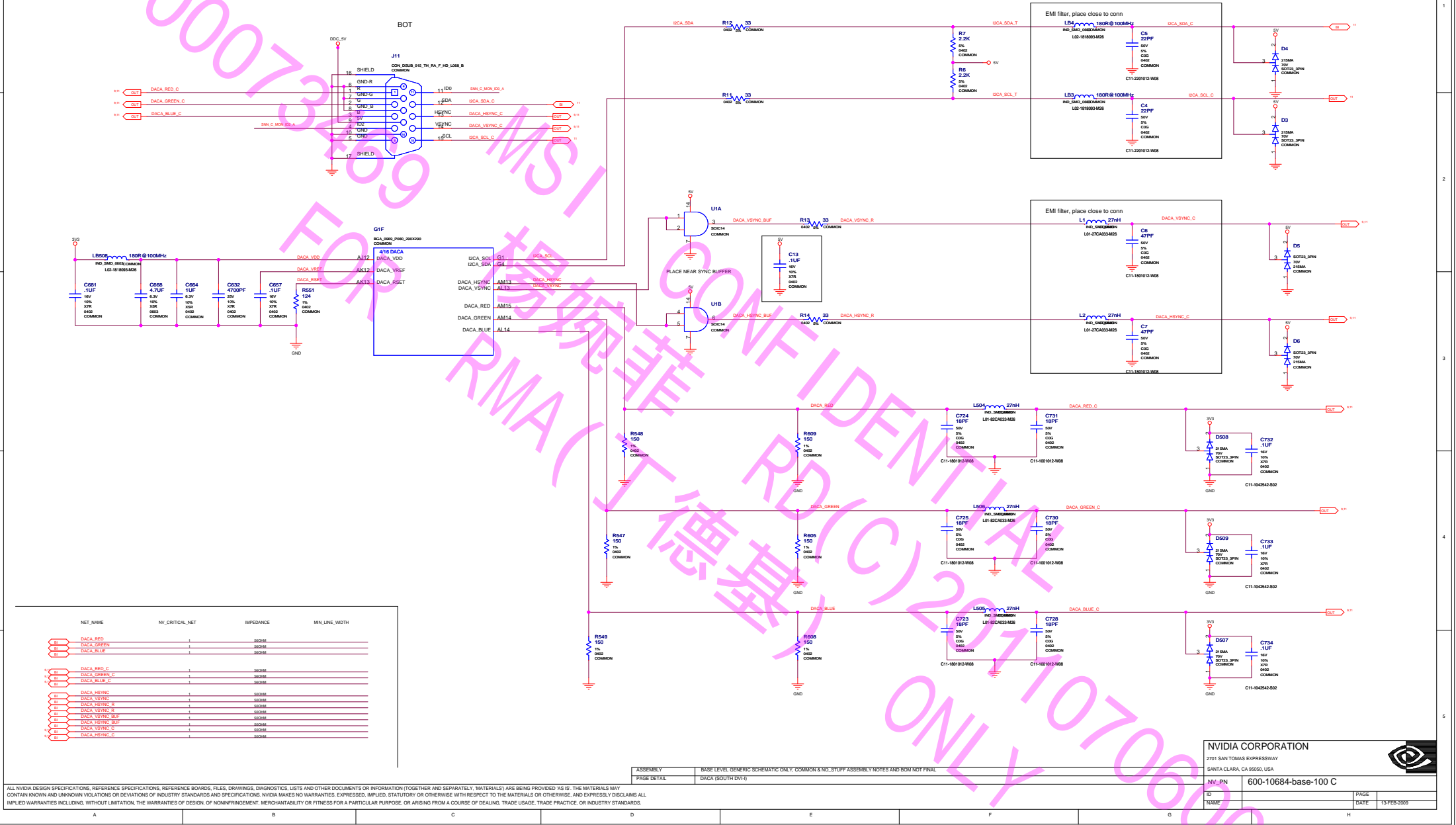


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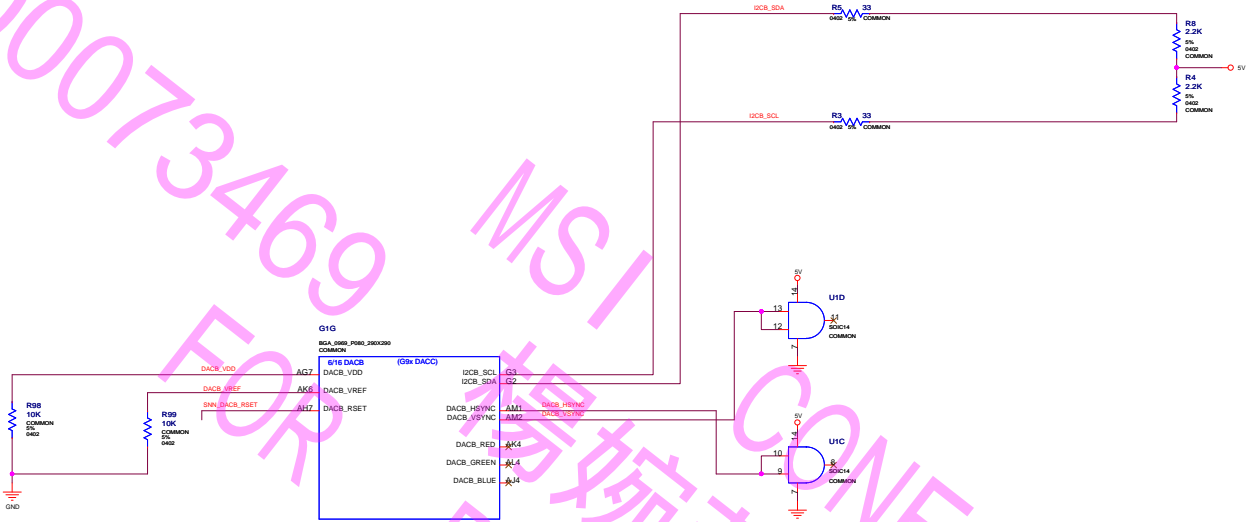
NAME		DATE	13-FEB-2009
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DACA (SOUTH DVI-I)



DACB (cable-up VGA)



DACB_RED	1	500K14
DACB_GREEN	1	500K14
DACB_BLUE	1	500K14
DACB_RED_C	1	500K14
DACB_GREEN_C	1	500K14
DACB_BLUE_C	1	500K14
DACB_HSYNC	1	500K14
DACB_HSYNC_A	1	500K14
DACB_HSYNC_B	1	500K14
DACB_HSYNC_C	1	500K14
DACB_HSYNC_D	1	500K14
DACB_HSYNC_E	1	500K14
DACB_HSYNC_F	1	500K14
DACB_HSYNC_G	1	500K14
DACB_HSYNC_H	1	500K14
DACB_HSYNC_I	1	500K14
DACB_HSYNC_J	1	500K14

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PAGE DETAIL	DACB (MIO DV11)

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NAME

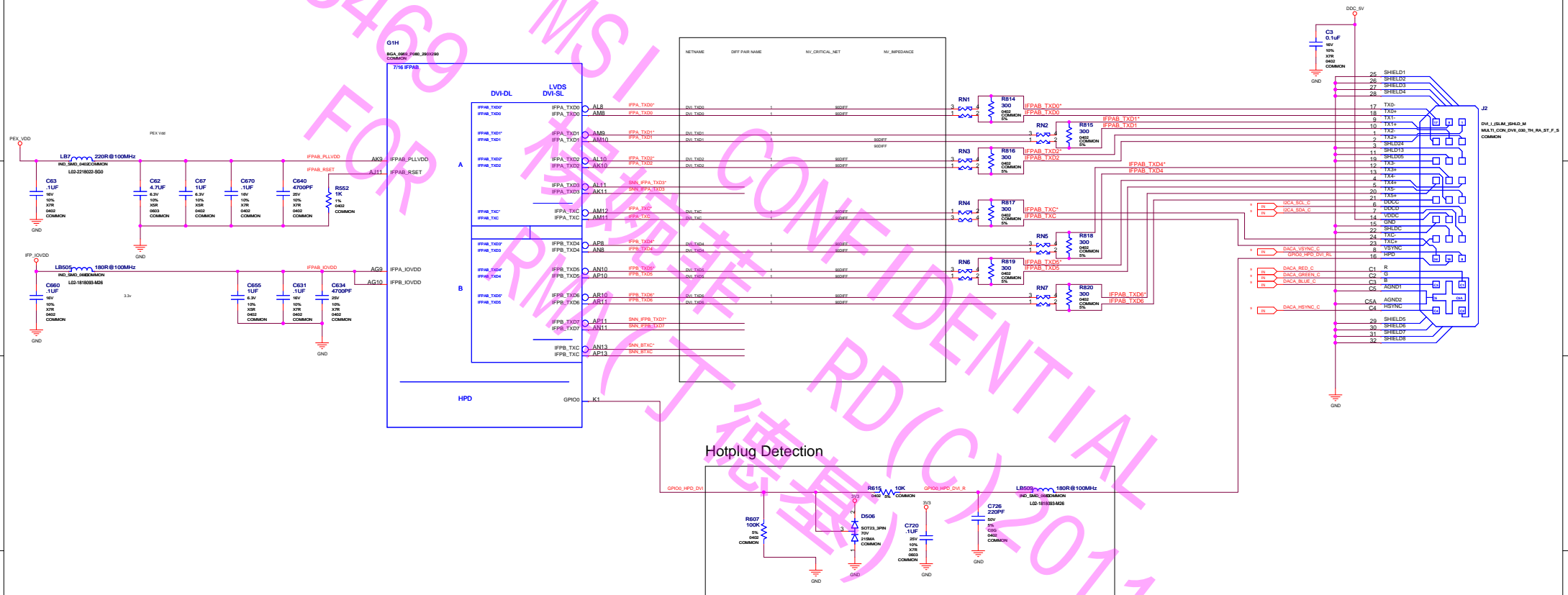
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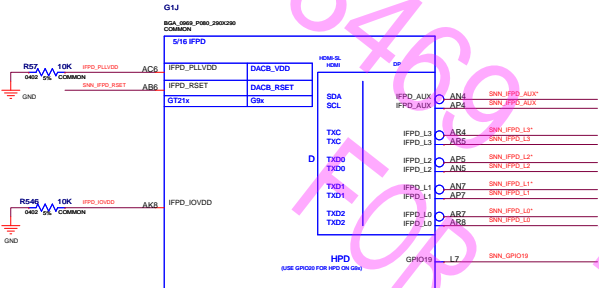


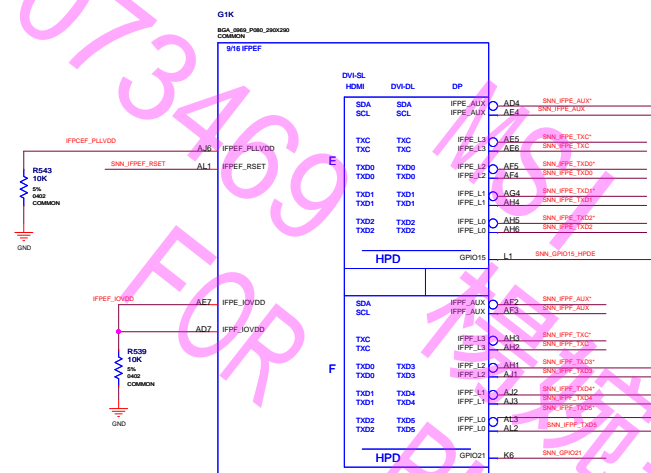
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IFP D (UNUSED)



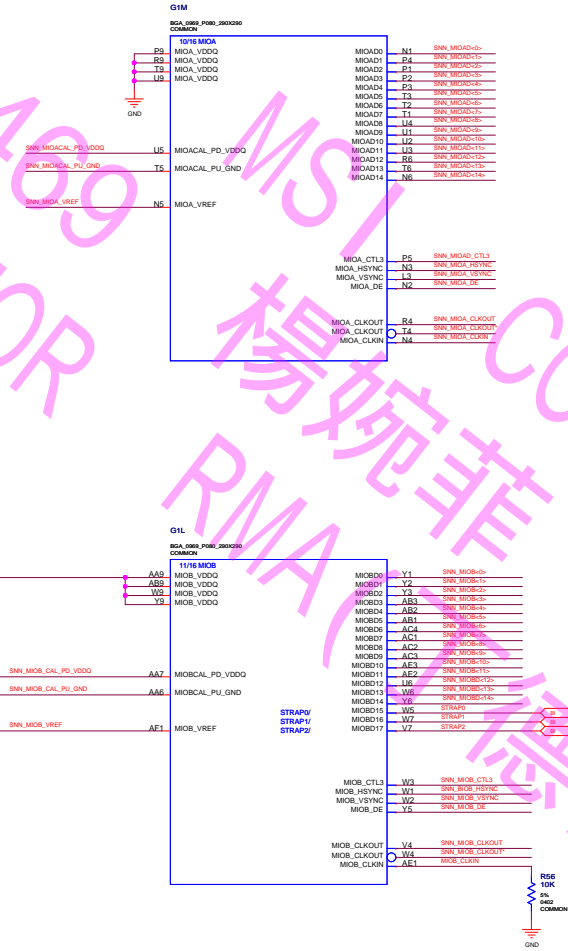
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PAGE DETAIL	IFP EF (MID DVI-I)

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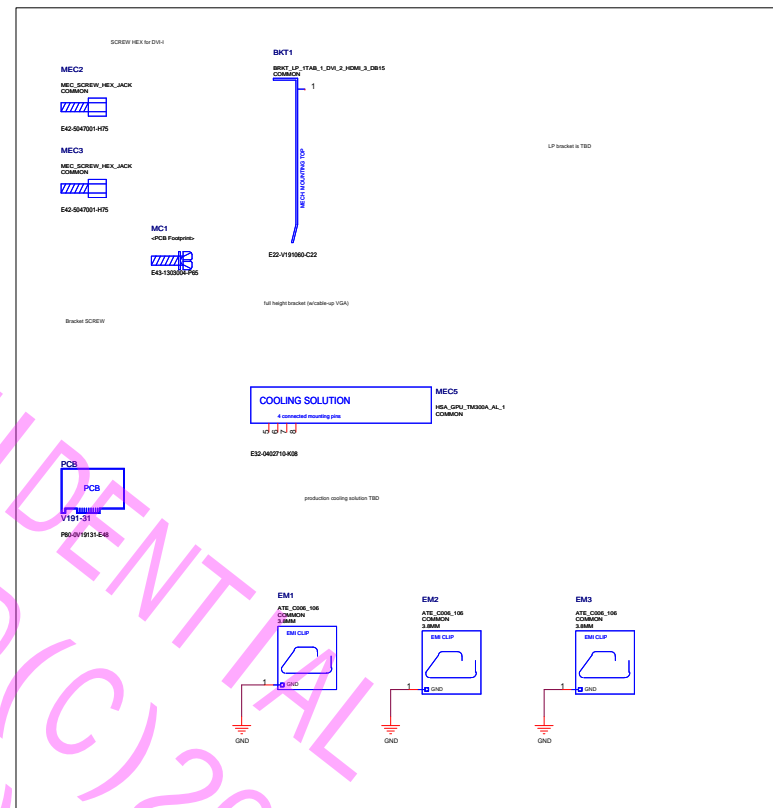
MIOA & MIOB




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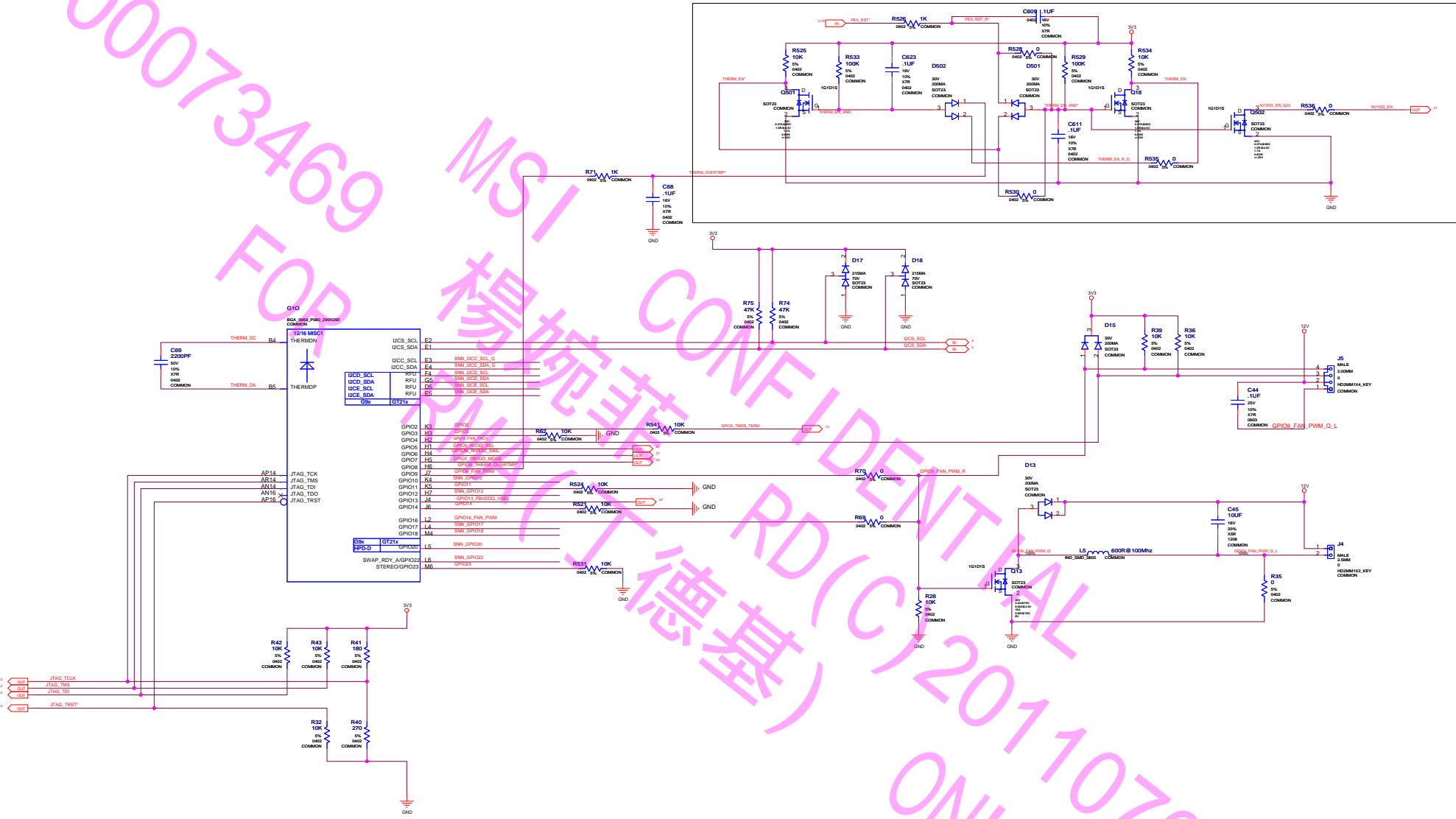
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ID		PAGE	
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NV_PN	600-10684-base-100 C		
ID		PAGE	
NAME		DATE	13-FEB-2009

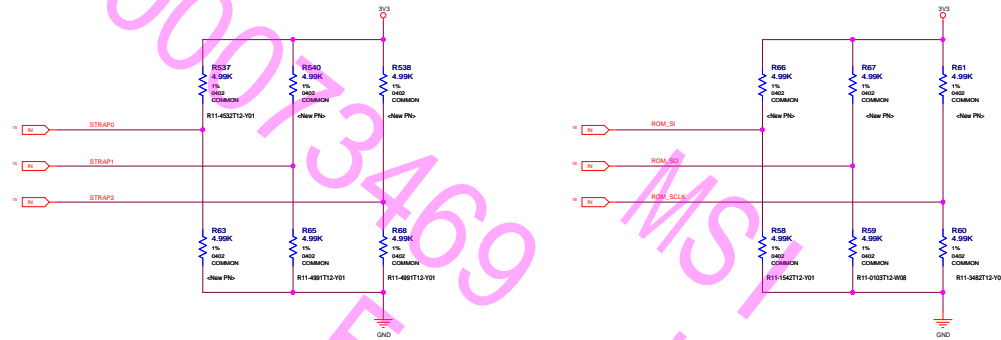
FAN CONTROL, GPIO, JTAG

OVERTEMP LATCH

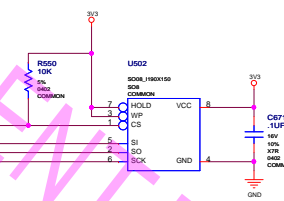


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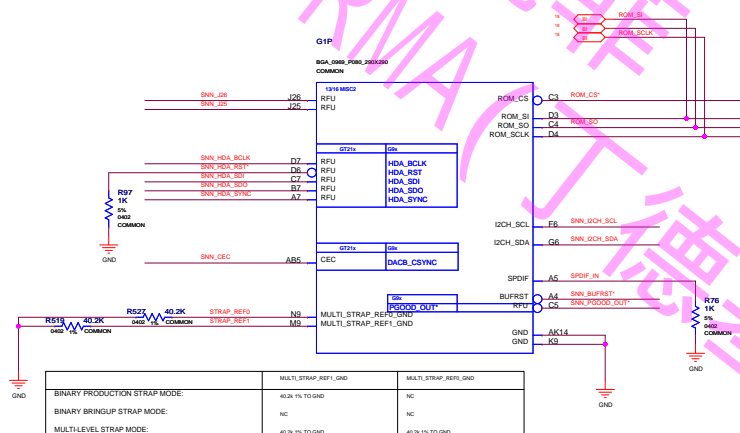
## STRAPPING OPTIONS



Stream	USERREG[3]	EXD0_1111	45x pulsed	0 to 100	0 to 5k Pul
Stream1	XGCPADCFG[3]	Desktop_0000	5x publication	1 to 100	0 to 5k Pul
Stream2	PCI_DEVCFG[3]	GT216-500-0A20	5x publication	3 to 20	1 to 20k Pul
ROM_ID	RAMCFG[3]	64MB16 D032 HY6H-0011 64MB16 D032 Samsung 0011	15x publication 20x publication	4 to 20 7 to 40	1 to 20k Pul 15 to 40k Pul
ROM_ID0	3: SCLK_#17 2: FREE 1: SDRAM_ALT_ADDR 0: VISA_DEVICE	0010		15x Pul	
ROM_SCLK	3: PCI_DEV_EXT 2: SUB_VENDOR 1: SIOST_CLK_CFG 0: PEX_PUL_EN_TERM100	0110		35x Pul	



For Lab Use Only



	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION STRAP MODE:	40.2% 1% TO GND	NC
BINARY BRINGUP STRAP MODE:	NC	NC
MULTI-LEVEL STRAP MODE:	40.2% 4% TO GND	40.2% 4% TO GND

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00073469

ONLY

FOR RMA (丁德基)

CONFIDENTIAL

# 5V & DDC\_5V REGULATOR

$V_{out} = 1.25V \cdot [1 + (ER305/ER304)]$

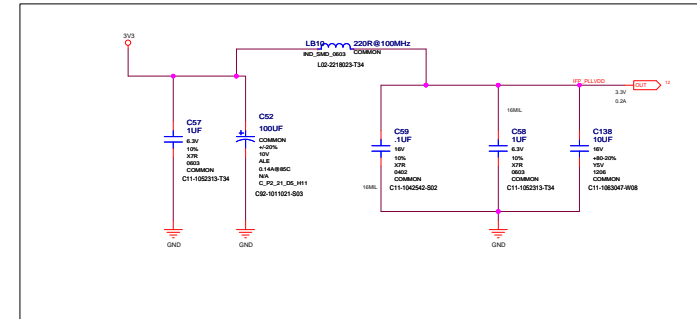
$5.0206 = 1.25V \cdot [1 + (ER305/ER304)]$

# IFP\_PLLVDD SUPPLY

# IFP\_IOVDD BACKDRIVE PREVENTION


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL
TRADE DETAIL	LINEAR POWER SUPPLIES

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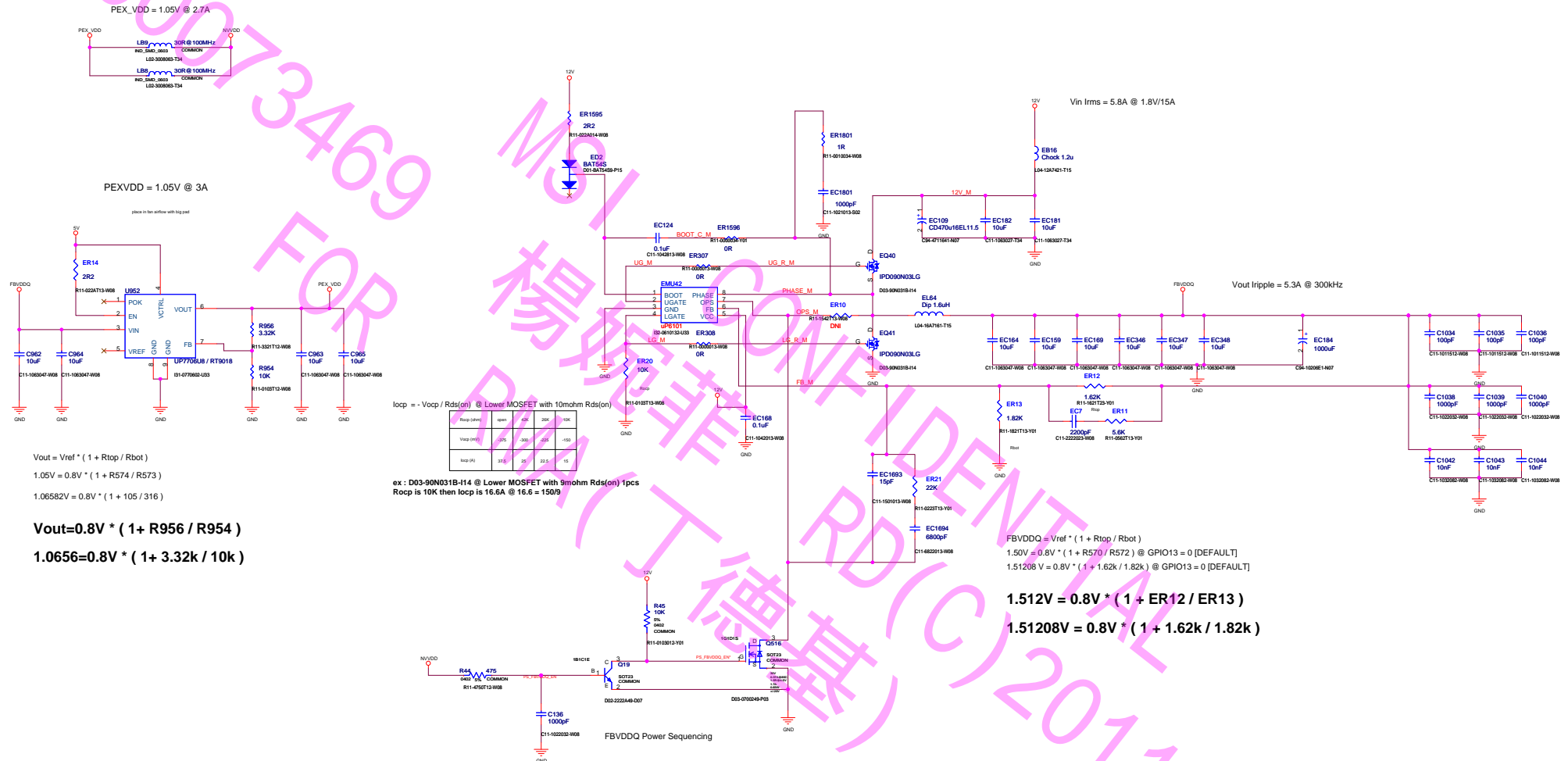


The diagram shows a precision current source circuit. It features an RC1117S3 3.3V LDO (U5) with its VIN connected to a 1.25V source through a 10µF capacitor (EC133). The LDO's GND is connected to ground. The LDO's VOUT is connected to a load resistor (R11-121013-008) and a feedback resistor (ER304) in series with a 3.3V source. The feedback resistor (ER304) is connected to the LDO's ADJ pin. The load resistor (R11-121013-008) is connected to ground. The output voltage is Vout = 1.25V \* [1 + (ER305/ER304)].

$$5.0206 = 1.25V^* [1 + (ER_{305}/ER_{304})]$$

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<b>NAME</b>		<b>DATE</b>	13-FEB-2009

## FBVDDQ/PEXVDD POWER SUPPLY



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PAGE DETAIL	FBVDDQ/PEXVDD POWER SUPPLY





[illegible]

V <sub>out</sub> = V <sub>in</sub> * (1+R <sub>1</sub> /R <sub>2</sub> )						
V <sub>IN</sub> (VDC)	GP05	GP06	R <sub>1</sub>	R <sub>2</sub>	Actual	
0.5V	L	L	1.02k	9.09k (9.09%)	0.501V	calculated per spec
0.55V	L	H	1.02k	9.42k (9.42%)	0.550V	
1.0V	H	L	1.02k	9.09k (9.09%)	1.002V	
1.05V	H	H	1.02k	9.42k (9.42%)	1.051V	

The figure contains six schematic diagrams arranged in a 3x2 grid. Each diagram shows a reference impedance connected to a signal line and ground. The top row shows the 100 Ohm reference impedance (blue box) for MEM Data, MEM CLK, and HDMI/DVI. The middle row shows the 200 Ohm reference impedance (red box) for MEM Data, MEM CLK, and HDMI/DVI. The bottom row shows the 100 Ohm reference impedance (blue box) for MEM CMD, MEM DQS, and PCIe. Each diagram includes a signal line, a reference impedance, and a ground connection. The signal lines are labeled with their respective signals and reference impedances.

Signal	Reference Impedance
MEM Data	100 Ohm
MEM Data	200 Ohm
MEM CLK	100 Ohm
MEM CLK	200 Ohm
HDMI/DVI	100 Ohm
HDMI/DVI	200 Ohm
MEM CMD	100 Ohm
MEM DQS	100 Ohm
PCIe	100 Ohm

