

P616-A00: G96-GB1-128, MXM-II, 512/256MB GDDR3 (32/16Mx32),
LVDS, HDMI, DP, TV_OUT, VGA, HD AUDIO,
MXM 2.1a SPECIFICATION COMPLIANT

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SKU	VARIANT	NVPN	ASSEMBLY
B	Base	600-10616-0000-000	BASE LEVEL GENERAL SCHEMATIC ONLY
1	SKU0001	600-10616-0001-000	NB9P-GS G96M 400MHz, 512MB(128bit) GDDR3 32Mx32 84FBGA, LVDS + DP + HDMI + SD/HD(TV_OUT) + VGA
2	SKU0002	600-10616-0002-000	Cancelled 128MB version
3	SKU0003	600-10616-0003-000	NB9P-GE2 G96M 400MHz, 512MB(128bit) GDDR3 32Mx32 84FBGA, LVDS + DP + HDMI + SD/HD(TV_OUT) + VGA
4	SKU9998	600-10616-9998-000	All components
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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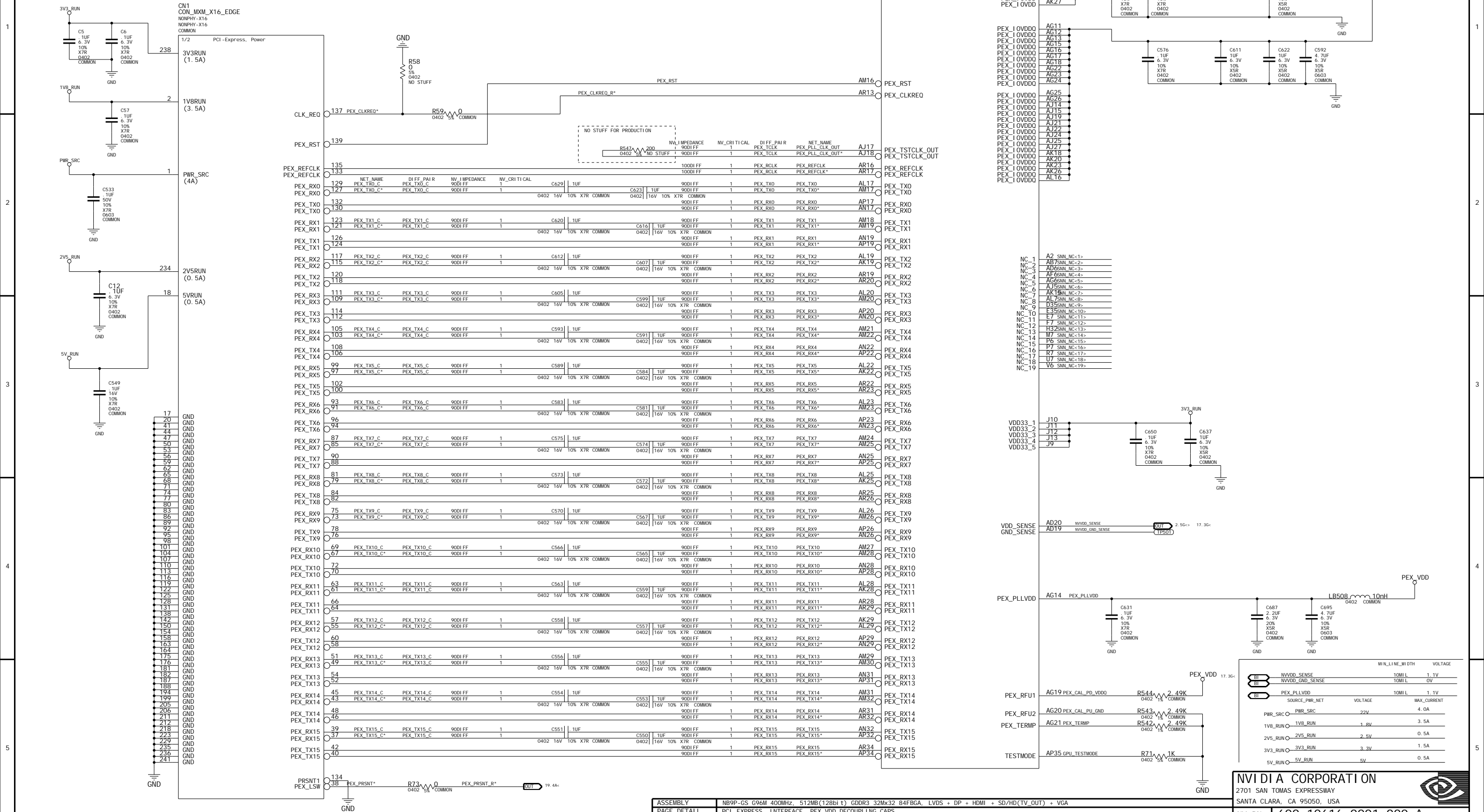
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NAME	wbrenckle	DATE	07-NOV-2007

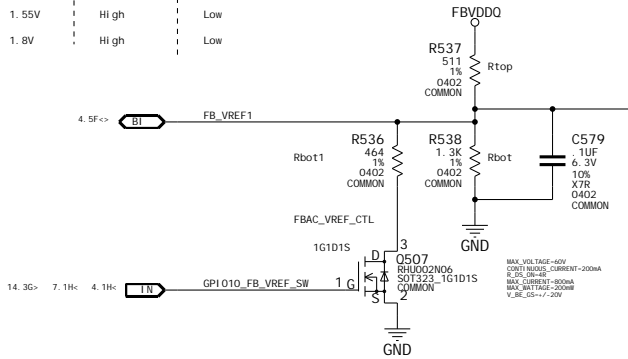
PCI EXPRESS



GPU MEMORY INTERFACE: PARTITION A

VREF	RTop	RBot	FBVDDQ	PERF MODE	GPI010
0.62V	511	1k3	1.55V	Low	Hi gh
0.72V	511	1k3	1.8V	Low	Hi gh
1.09V	511	1k3 464	1.55V	Hi gh	Low
1.26V	511	1k3 464	1.8V	Hi gh	Low

LOW PERF: VREF = 0.40 * FBVDDQ
HIGH PERF: VREF = 0.70 * FBVDDQ
VREF = FBVDDQ * Rbot/(Rtop + Rbot)



G1
STD
COMMON

- 2/16 FBA
- FBA D0> R30
- FBA D1> R32
- FBA D2> P31
- FBA D3> N30
- FBA D4> L31
- FBA D5> M32
- FBA D6> M30
- FBA D7> L30
- FBA D8> P33
- FBA D9> P35
- FBA D10> N35
- FBA D11> P35
- FBA D12> N34
- FBA D13> L33
- FBA D14> L32
- FBA D15> N33
- FBA D16> K31
- FBA D17> K30
- FBA D18> G30
- FBA D19> K32
- FBA D20> G32
- FBA D21> H30
- FBA D22> F30
- FBA D23> G31
- FBA D24> H33
- FBA D25> K35
- FBA D26> K33
- FBA D27> G34
- FBA D28> K34
- FBA D29> E33
- FBA D30> E34
- FBA D31> G33
- FBA D32> AG30
- FBA D33> AH31
- FBA D34> AG32
- FBA D35> AF31
- FBA D36> AF30
- FBA D37> AD30
- FBA D38> AC32
- FBA D39> AF30
- FBA D40> AF32
- FBA D41> AF33
- FBA D42> AF34
- FBA D43> AE33
- FBA D44> AE33
- FBA D45> AE34
- FBA D46> AC35
- FBA D47> AB32
- FBA D48> AH35
- FBA D49> AK32
- FBA D50> AL33
- FBA D51> AM33
- FBA D52> AL31
- FBA D53> AK30
- FBA D54> AJ30
- FBA D55> AH30
- FBA D56> AH35
- FBA D57> AH33
- FBA D58> AH35
- FBA D59> AH32
- FBA D60> AH34
- FBA D61> AM34
- FBA D62> AL35
- FBA D63> AJ33

- FBA DOM0
- FBA DOM1
- FBA DOM2
- FBA DOM3
- FBA DOM4
- FBA DOM5
- FBA DOM6
- FBA DOM7
- FBA DOS_WP0
- FBA DOS_WP1
- FBA DOS_WP2
- FBA DOS_WP3
- FBA DOS_WP4
- FBA DOS_WP5
- FBA DOS_WP6
- FBA DOS_WP7
- FBA DOS_RN0
- FBA DOS_RN1
- FBA DOS_RN2
- FBA DOS_RN3
- FBA DOS_RN4
- FBA DOS_RN5
- FBA DOS_RN6
- FBA DOS_RN7

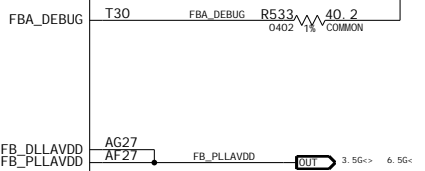
- SNN_FBA_WDS0
- SNN_FBA_WDS1
- SNN_FBA_WDS1*
- SNN_FBA_WDS2
- SNN_FBA_WDS2*
- SNN_FBA_WDS3
- SNN_FBA_WDS3*

- RFU
- RFU
- RFU
- RFU
- RFU
- RFU
- RFU

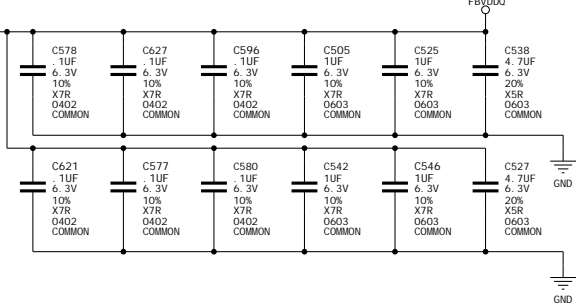
- FBA_CMD0 V32
- FBA_CMD1 W31
- FBA_CMD2 U31
- FBA_CMD3 Y32
- FBA_CMD4 AB35
- FBA_CMD5 AB34
- FBA_CMD6 W35
- FBA_CMD7 W33
- FBA_CMD8 W30
- FBA_CMD9 T34
- FBA_CMD10 T35
- FBA_CMD11 AB31
- FBA_CMD12 Y30
- FBA_CMD13 W32
- FBA_CMD14 AA30
- FBA_CMD15 AA32
- FBA_CMD16 Y33
- FBA_CMD17 U32
- FBA_CMD18 Y31
- FBA_CMD19 U34
- FBA_CMD20 U34
- FBA_CMD21 Y35
- FBA_CMD22 W34
- FBA_CMD23 Y30
- FBA_CMD24 U35
- FBA_CMD25 U30
- FBA_CMD26 U33
- FBA_CMD27 AB30
- FBA_CMD28 AB33
- FBA_CMD29 T33
- FBA_CMD30 W29
- FBA_CMD0> 0
- FBA_CMD1> 1
- FBA_CMD2> 2
- FBA_CMD3> 3
- FBA_CMD4> 4
- FBA_CMD5> 5
- FBA_CMD6> 6
- FBA_CMD7> 7
- FBA_CMD8> 8
- FBA_CMD9> 9
- FBA_CMD10> 10
- FBA_CMD11> 11
- FBA_CMD12> 12
- FBA_CMD13> 13
- FBA_CMD14> 14
- FBA_CMD15> 15
- FBA_CMD16> 16
- FBA_CMD17> 17
- FBA_CMD18> 18
- FBA_CMD19> 19
- FBA_CMD20> 20
- FBA_CMD21> 21
- FBA_CMD22> 22
- FBA_CMD23> 23
- FBA_CMD24> 24
- FBA_CMD25> 25
- SNN_FBA_CMD26
- SNN_FBA_CMD27
- SNN_FBA_CMD28
- SNN_FBA_CMD29
- SNN_FBA_CMD30

- FBA_CLK0 T32
- FBA_CLK1 AC31
- FBA_CLK1* AC30

- FBA_CLK0 OUT 4.2A< 4.4F<
- FBA_CLK1 OUT 4.2A< 4.4F<
- FBA_CLK1* OUT 4.20< 4.4F<



- FBVDDQ J23
- FBVDDQ J24
- FBVDDQ J29
- FBVDDQ AA27
- FBVDDQ AA29
- FBVDDQ AB27
- FBVDDQ AB29
- FBVDDQ AC27
- FBVDDQ AD27
- FBVDDQ AE27
- FBVDDQ AJ28
- FBVDDQ B18
- FBVDDQ E21
- FBVDDQ G17
- FBVDDQ G18
- FBVDDQ G22
- FBVDDQ G8
- FBVDDQ G9
- FBVDDQ H29
- FBVDDQ J14
- FBVDDQ J15
- FBVDDQ J16
- FBVDDQ J17
- FBVDDQ J20
- FBVDDQ J21
- FBVDDQ J22



NET MI N_LI NE_WI DTH VOLTAGE

3.4F< 6.5G< FBVDDQ 10M L 1.2V

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ASSEMBLY N89P-GS G96M 400MHz, 512MB(128bi t) GDDR3 32Mx32 84FBGA, LVDS + DP + HDMI + SD/HD(TV_OUT) + VGA

PAGE DETAIL FBA MEMORY INTERFACE & FBVDDQ DECOUPLING CAPS

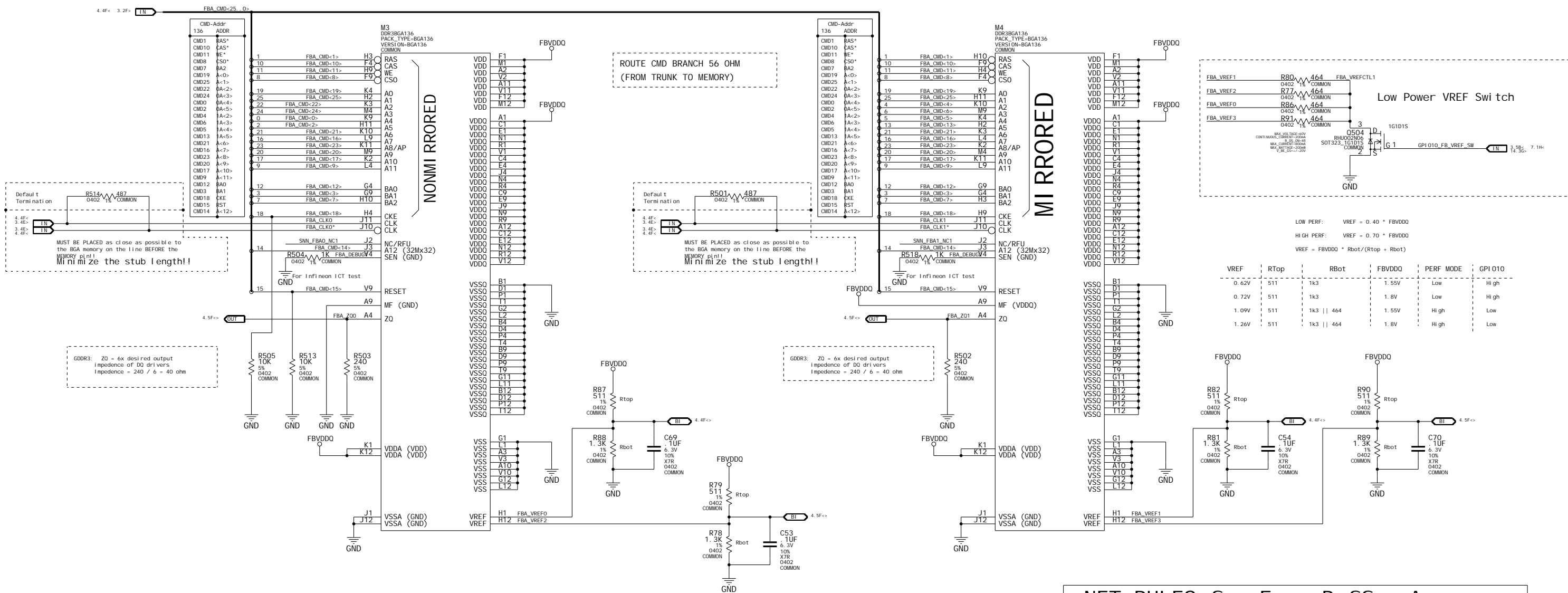
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FRAME BUFFER PARTITION A

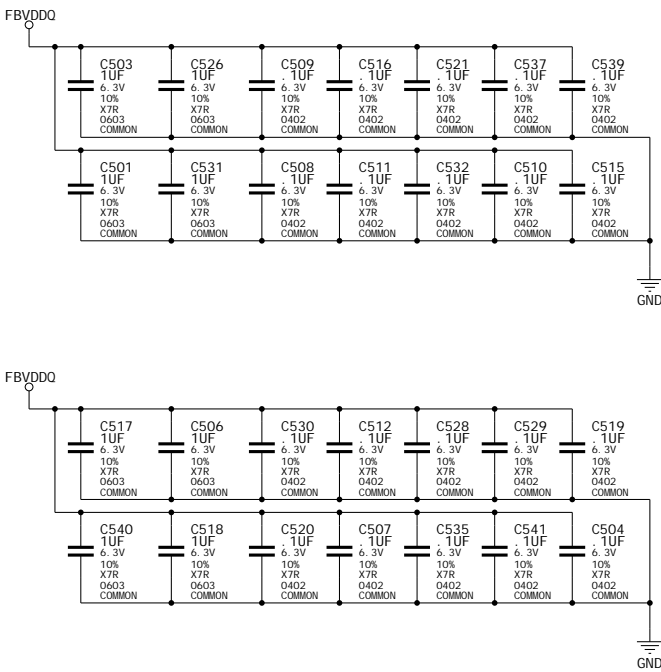


NET RULES for FrameBuffer A

NET		NV_CRI T1 CAL		NV_I IMPEDANCE		MI_NI DTH	
4. 2A<	3. 4E>	FBA_CLK0	1	800I FF	FBA_CLK0		
4. 2A<	3. 4E>	FBA_CLK0*	1	800I FF	FBA_CLK0		
4. 2D<	3. 4E>	FBA_CLK1	1	800I FF	FBA_CLK1		
4. 2D<	3. 4E>	FBA_CLK1*	1	800I FF	FBA_CLK1		
4. 5A<	3. 3C>	FBA_DQS_WP<7, 0>	1	500HM			
4. 4A<	3. 4C>	FBA_DQS_RN<7, 0>	1	500HM			
4. 4A<	3. 3C>	FBA_DQS<7, 0>	1	500HM			
4. 4B<	3. 1C>	FBA_D<63, 0>	1	500HM			
4. 1A<	3. 2F>	FBA_CMD<25, 0>	1	500HM			
NET		VOLTAGE		MAX_CURRENT		MI_NI DTH	
4. 3D>	BI	FBA_VREF0	1. 47V	0. 02A	12MI L		
4. 3E>	BI	FBA_VREF1	1. 47V	0. 02A	12MI L		
4. 3E>	BI	FBA_VREF2	1. 47V	0. 02A	12MI L		
4. 3H>	BI	FBA_VREF3	1. 47V	0. 02A	12MI L		
4. 2B>	BI	FBA_Z00	1. 47V	0. 02A	12MI L		
4. 2E>	BI	FBA_Z01	1. 47V	0. 02A	12MI L		
5. 6B<	BI	FB_VREF1	1. 47V	0. 02A	12MI L		



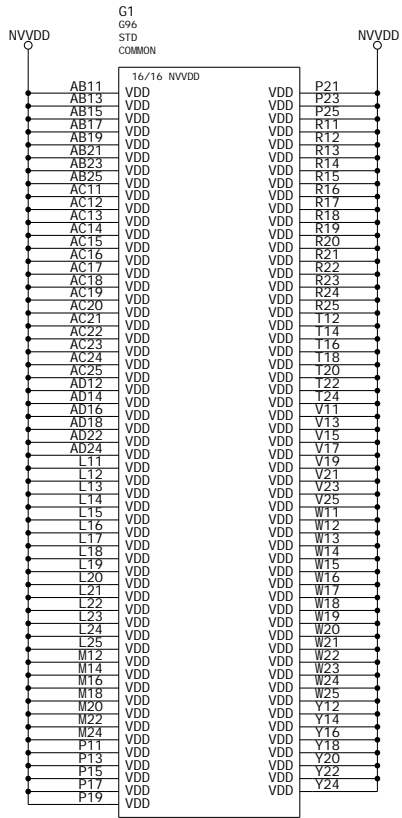
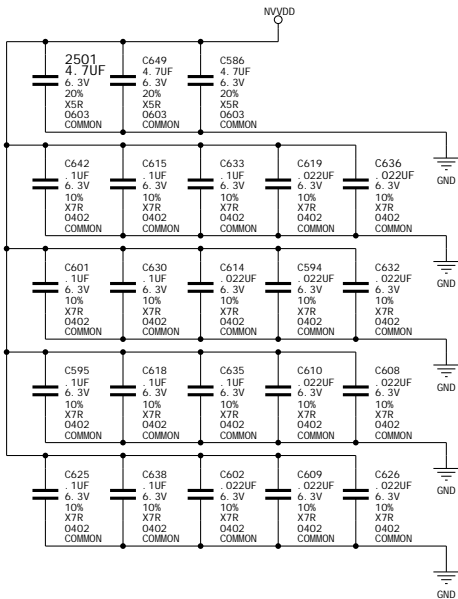
FRAME BUFFER: PARTITION A DECOUPLING



Decoupling for
FBA North Side
Memory Device.

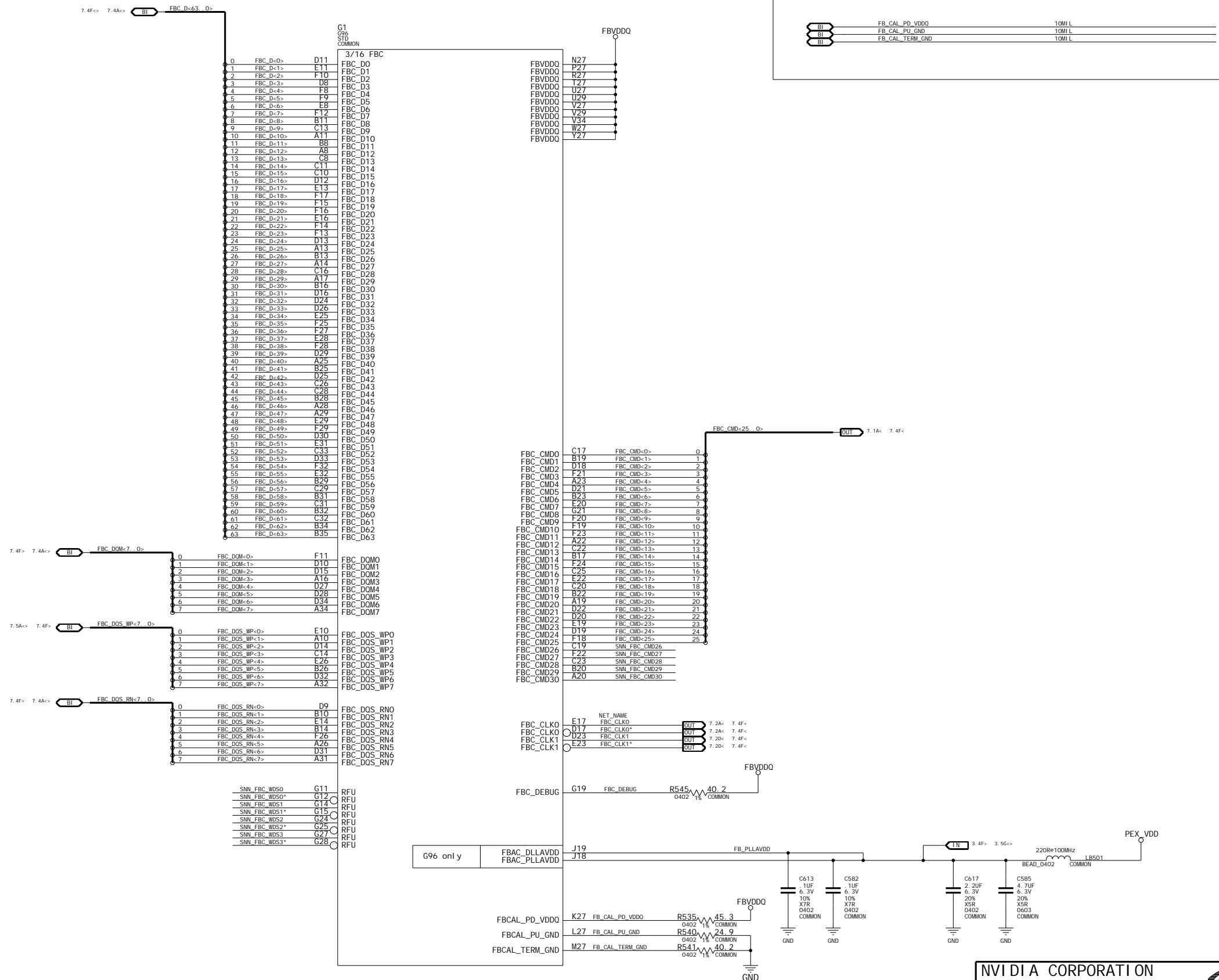
Decoupling for
FBA South Side
Memory Device.

NVVDD POWER AND DECOUPLING



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GPU MEMORY INTERFACE: PARTITION C

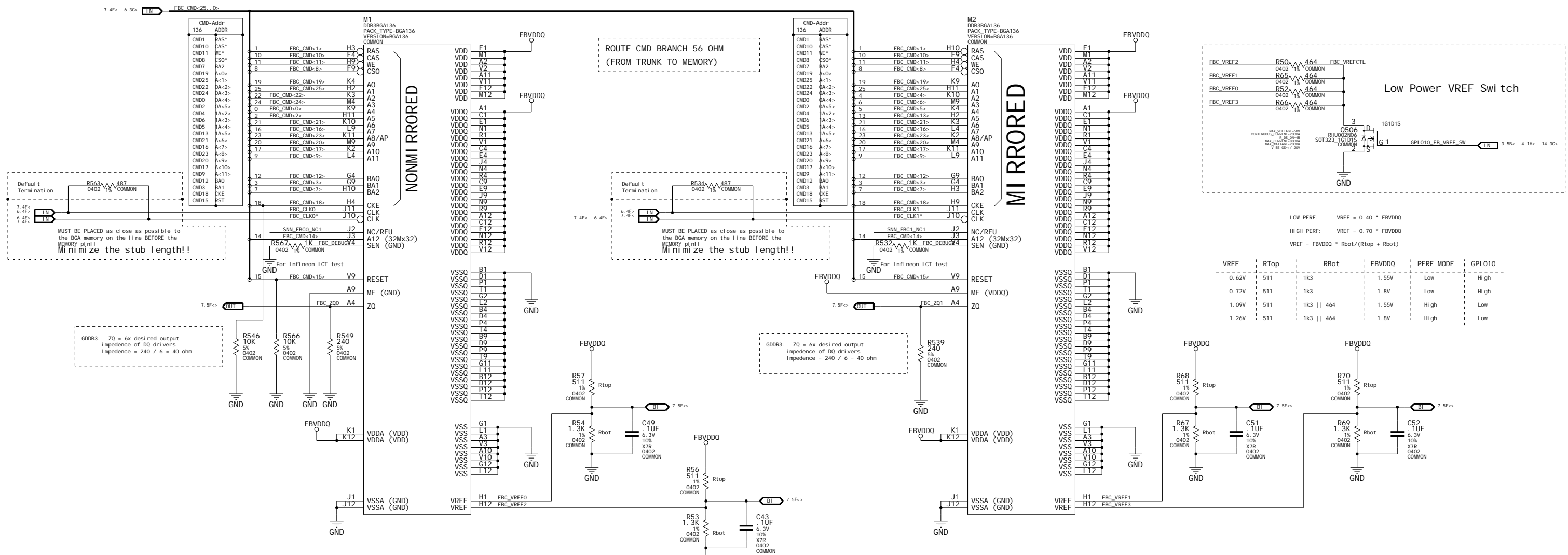


ASSEMBLY	NB9P-GS G96M 400MHz, 512MB(128bit) GDDR3 32Mx32 84FBGA, LVDS + DP + HDMI + SD/HD(TV_OUT) + VGA
PAGE DETAIL	FBC MEMORY INTERFACE


















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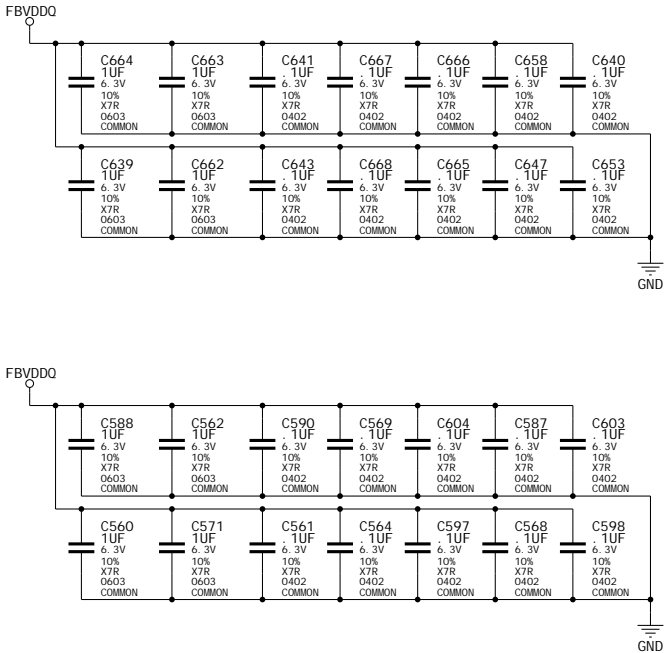
FRAME BUFFER PARTITION C



NET RULES for FrameBuffer C

	NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
7. 2A< 6. 4F>	 FBC_CLK0	1	80DI FF	FBC_CLK0
7. 2A< 6. 4F>	 FBC_CLK0*	1	80DI FF	FBC_CLK0
7. 2D< 6. 4F>	 FBC_CLK1	1	80DI FF	FBC_CLK1
7. 2D< 6. 4F>	 FBC_CLK1*	1	80DI FF	FBC_CLK1
<hr/>				
7. 5A<> 6. 4C<>	 FBC_DQS_WP<7...0>	1	50OHM	
7. 4A<> 6. 4C<>	 FBC_DQS_RN<7...0>	1	50OHM	
7. 4A<> 6. 3C<>	 FBC_DQ<7...0>	1	50OHM	
7. 4A<> 6. 3C<>	 FBC_D<6,3...0>	1	50OHM	
7. 4A<> 6. 3C<>	 FBC_CMD<25...0>	1	50OHM	
7. 3C<> 6. 3C<>	 FBC_CMD<25...0>	1	50OHM	
7. 3C<> 6. 3C<>	 FBC_CMD<25...0>	1	50OHM	
<hr/>				
	NET	VOLTAGE	MAX_CURRENT	MI N_WI DTH
7. 3D<> 7. 3G<>	 FBC_VREF0	1. 47V	0. 02A	12MI L
7. 3D<> 7. 3G<>	 FBC_VREF1	1. 47V	0. 02A	12MI L
7. 3E<> 7. 3H<>	 FBC_VREF2	1. 47V	0. 02A	12MI L
7. 3E<> 7. 3H<>	 FBC_VREF3	1. 47V	0. 02A	12MI L
7. 2B<> 7. 2E<>	 FBC_Z00	1. 47V	0. 02A	12MI L
7. 2B<> 7. 2E<>	 FBC_Z01	1. 47V	0. 02A	12MI L

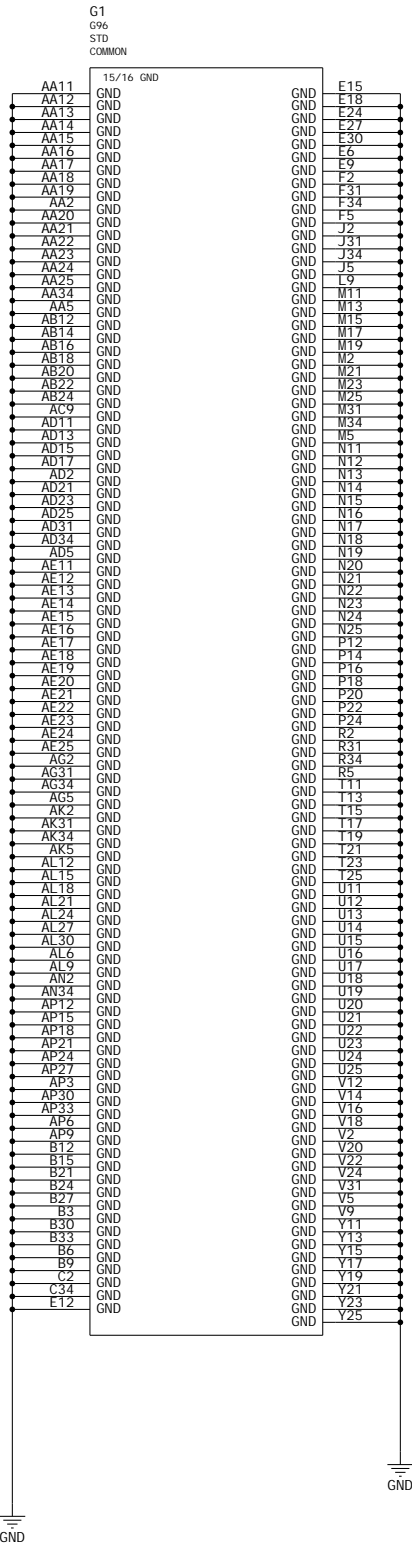
FRAMEBUFFER: PARTITION C DECOUPLING



Decoupling for FBC West Side Memory Device.

Decoupling for FBC East Side Memory Device.

NVVDD GROUND



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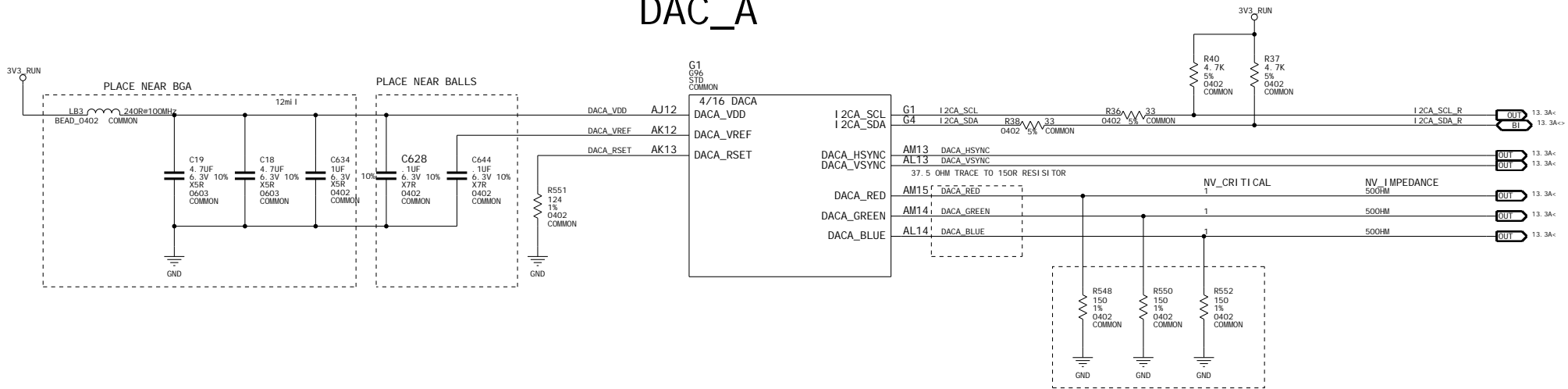
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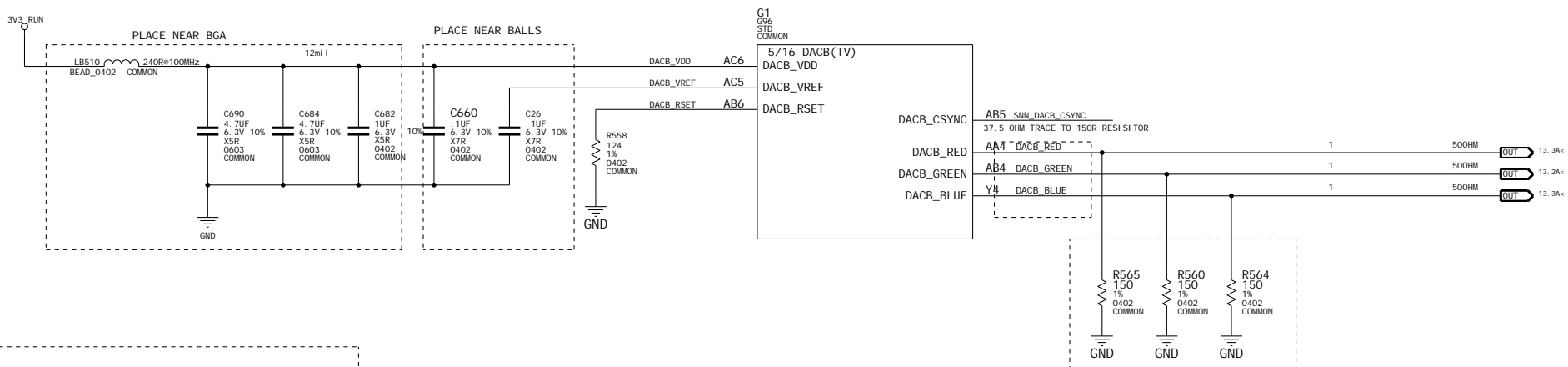
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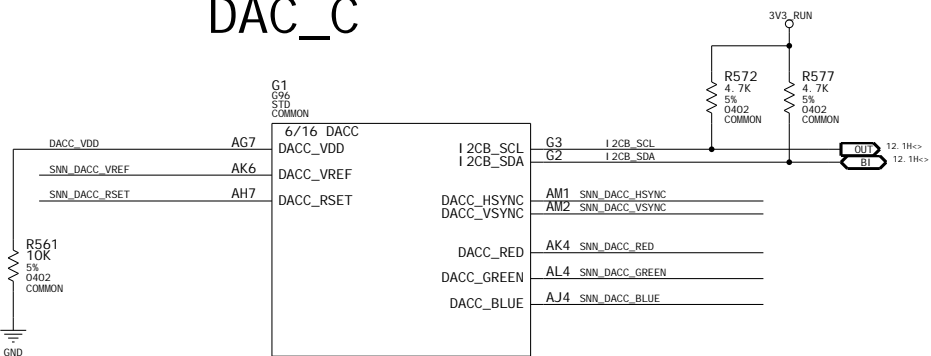
DAC_A



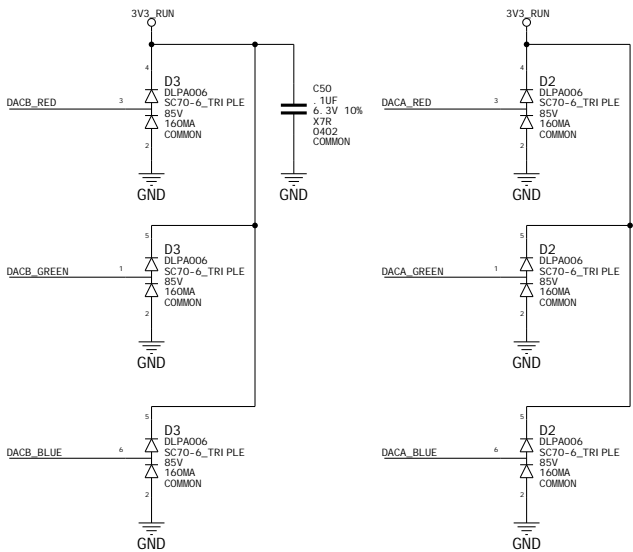
DAC_B



DAC_C



TV DAC ESD PROTECTION



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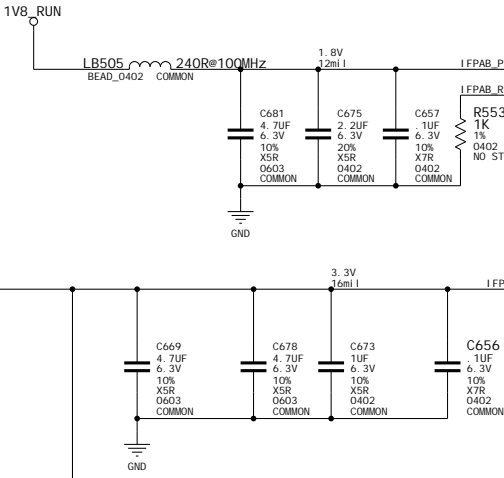
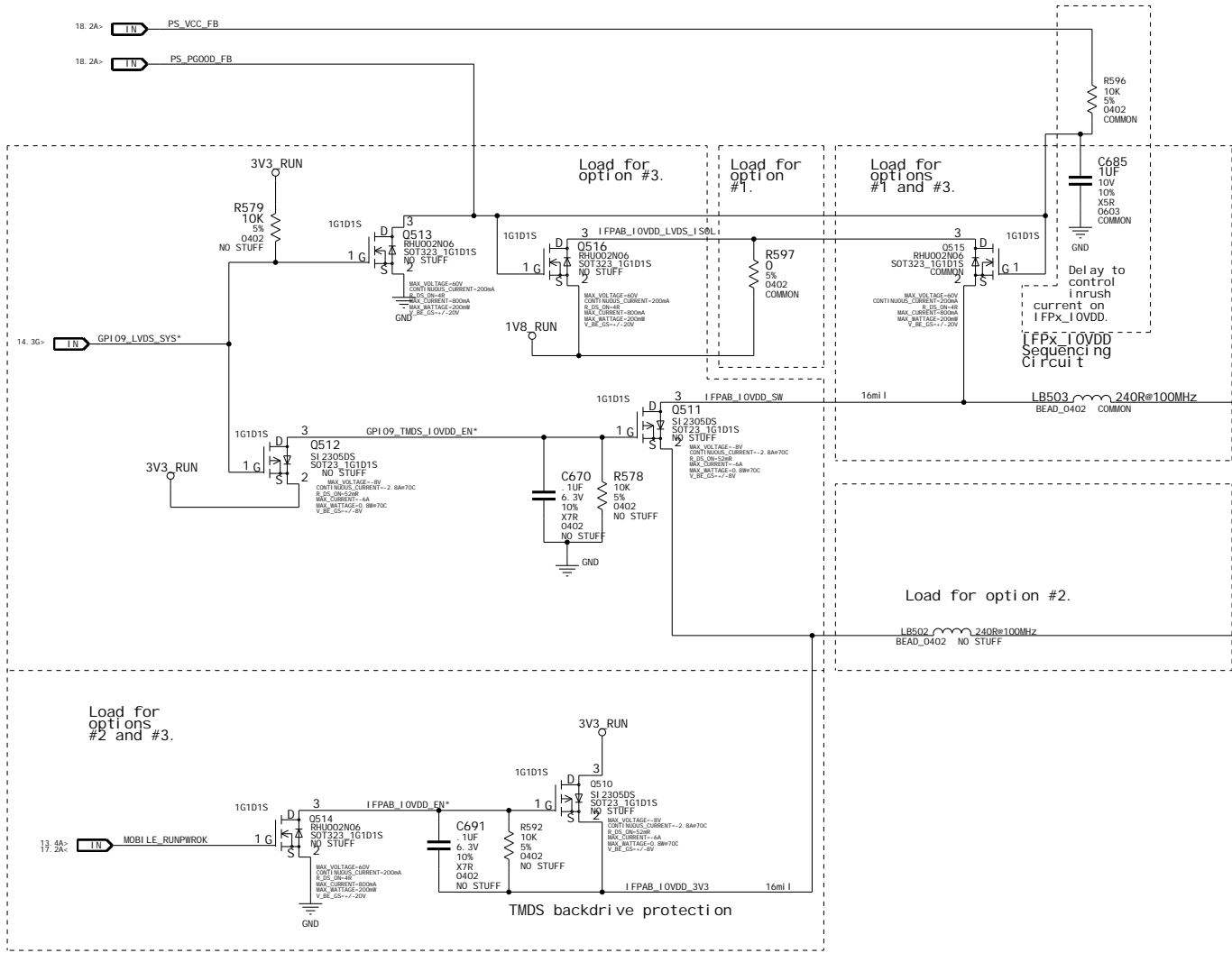
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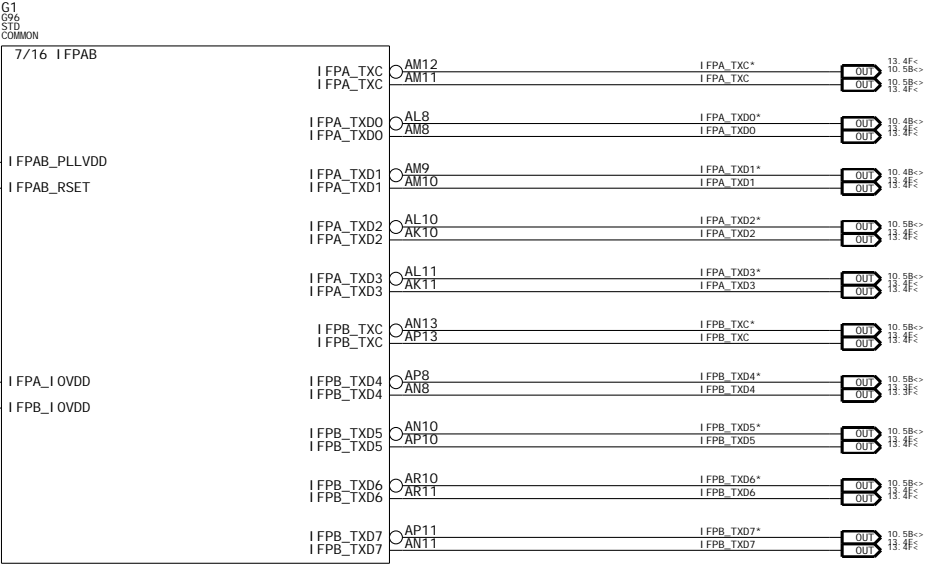
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Loading options for IFPAB outputs

- Option #1) IFPAB outputs to LVDS only.
Option #2) IFPAB outputs to DVI-C only.
Option #3) Controlled with GPIO9, IFPAB dynamically outputs to LVDS or DVI -C.



LVDS/TMDS(Link A&B)



(LVDS CONSTRAINTS)

NET	NAME	DIFFPAIR	NV_CRTICAL_NET	NV_IMPEDANCE
IFPA_TXD0*	IFPATXD0	1	100DIFF	13.4f<
IFPA_TXD0	IFPATXD0	1	100DIFF	10.1h<
IFPA_TXD1*	IFPATXD1	1	100DIFF	13.4f<
IFPA_TXD1	IFPATXD1	1	100DIFF	10.2h<
IFPA_TXD2*	IFPATXD2	1	100DIFF	13.4f<
IFPA_TXD2	IFPATXD2	1	100DIFF	10.2h<
IFPA_TXD3*	IFPATXD3	1	100DIFF	13.4f<
IFPA_TXD3	IFPATXD3	1	100DIFF	10.2h<
IFPB_TXD4*	IFPBTXD4	1	100DIFF	13.4f<
IFPB_TXD4	IFPBTXD4	1	100DIFF	10.2h<
IFPB_TXD5*	IFPBTXD5	1	100DIFF	13.4f<
IFPB_TXD5	IFPBTXD5	1	100DIFF	10.2h<
IFPB_TXD6*	IFPBTXD6	1	100DIFF	13.4f<
IFPB_TXD6	IFPBTXD6	1	100DIFF	10.2h<
IFPB_TXD7*	IFPBTXD7	1	100DIFF	13.4f<
IFPB_TXD7	IFPBTXD7	1	100DIFF	10.2h<
IFPA_TXC*	IFPATXC	1	100DIFF	10.1h<
IFPA_TXC	IFPATXC	1	100DIFF	13.4f<
IFPB_TXC*	IFPBTXC	1	100DIFF	10.2h<
IFPB_TXC	IFPBTXC	1	100DIFF	13.4f<

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ASSEMBLY	NB9P-GS G96M 400MHz, 512MB(128bit) GDDR3 32Mx32 84FBGA, LVDS + DP + HDMI + SD/HD(TV_OUT) + VGA
PAGE DETAIL	LVDS/TMDS OPTION (LINK A/B)

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PAGE

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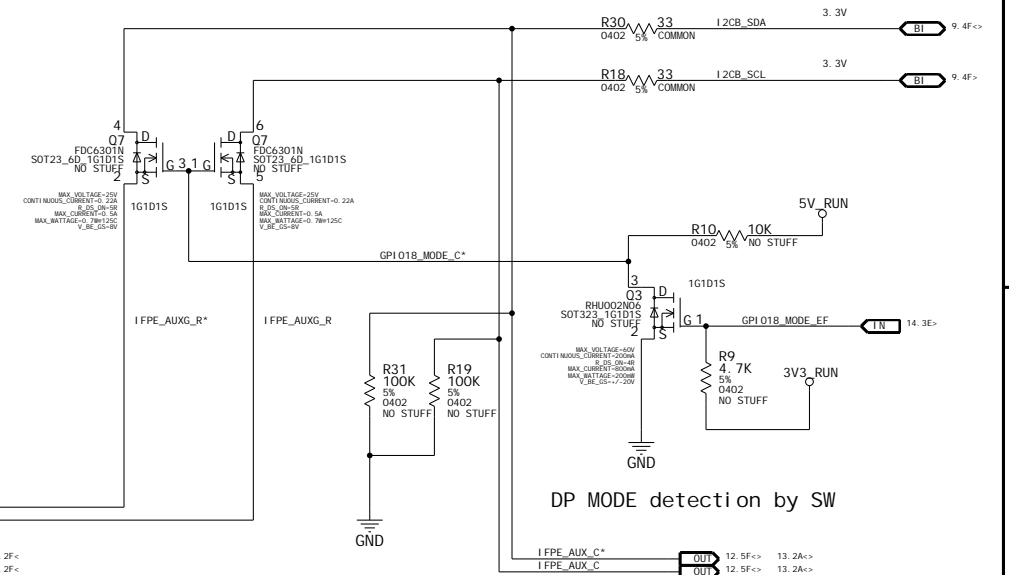
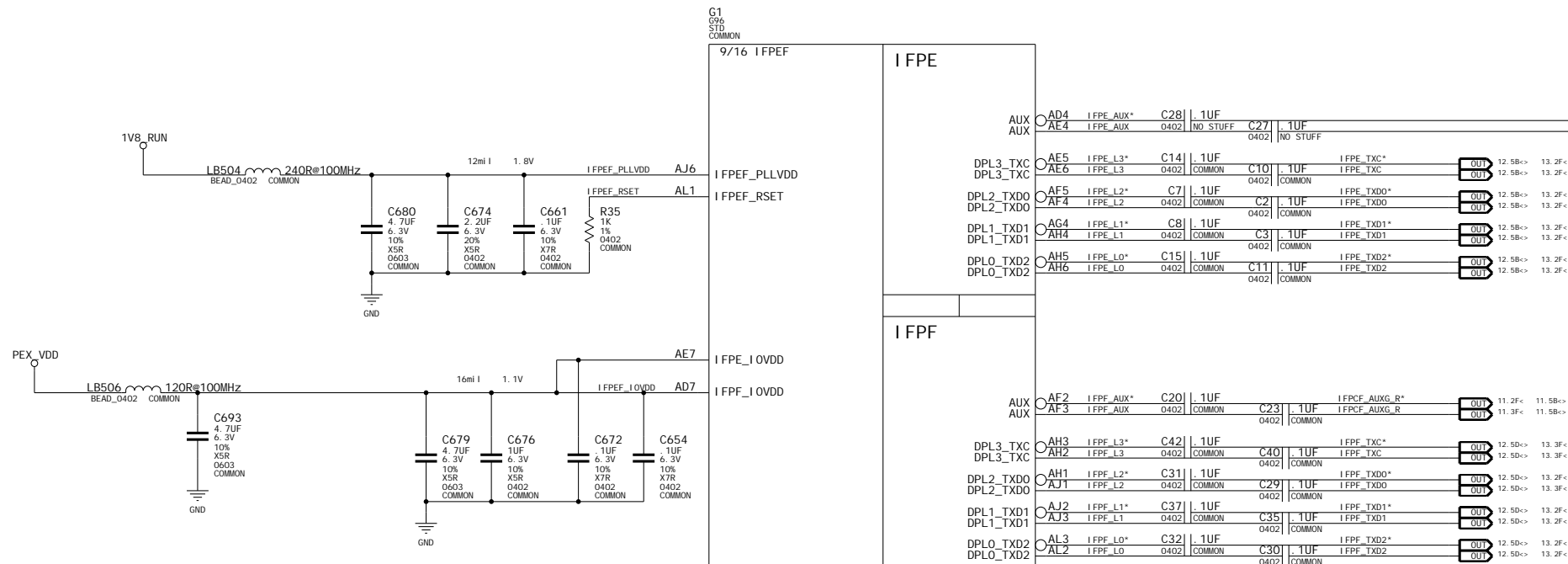
NAME

wbrenckle

DATE

07-NOV-2007

HDMI /DP OPTI ON (LINK E)



TMDS (LINK F)

(TMDS/HDMI /DP OPTI ON CONSTRAI NTS)

NET NAME	DI FFP AI R	NV_CRI TI CAL_NET	NV_I MPEDANCE	NET NAME	DI FFP AI R	NV_CRI TI CAL_NET	NV_I MPEDANCE	NET NAME	DI FFP AI R	NV_CRI TI CAL_NET	NV_I MPEDANCE
I FPE_L3*	I FPE_L3	1	100DI FF	I FPF_L3*	I FPF_L3	1	100DI FF	I FPE_AUX*	I FPE_AUX	1	100DI FF
I FPE_L3	I FPE_L3	1	100DI FF	I FPF_L3	I FPF_L3	1	100DI FF	I FPE_AUX	I FPE_AUX	1	100DI FF
I FPE_L2*	I FPE_L2	1	100DI FF	I FPF_L2*	I FPF_L2	1	100DI FF	I FPE_AUXG_R*	I FPE_AUXG_R	1	100DI FF
I FPE_L2	I FPE_L2	1	100DI FF	I FPF_L2	I FPF_L2	1	100DI FF	I FPE_AUXG_R	I FPE_AUXG_R	1	100DI FF
I FPE_L1*	I FPE_L1	1	100DI FF	I FPF_L1*	I FPF_L1	1	100DI FF				
I FPE_L1	I FPE_L1	1	100DI FF	I FPF_L1	I FPF_L1	1	100DI FF				
I FPE_LO*	I FPE_LO	1	100DI FF	I FPF_LO*	I FPF_LO	1	100DI FF	I FPE_AUX_C*	I FPE_AUX_C	1	100DI FF
I FPE_LO	I FPE_LO	1	100DI FF	I FPF_LO	I FPF_LO	1	100DI FF	I FPE_AUX_C	I FPE_AUX_C	1	100DI FF
I FPE_TXC*	I FPE_TXC	1	100DI FF	I FPF_TXC*	I FPF_TXC	1	100DI FF				
I FPE_TXC	I FPE_TXC	1	100DI FF	I FPF_TXC	I FPF_TXC	1	100DI FF				
I FPE_TXD0*	I FPE_TXD0	1	100DI FF	I FPF_TXD0*	I FPF_TXD0	1	100DI FF	I FPF_AUX*	I FPF_AUX	1	100DI FF
I FPE_TXD0	I FPE_TXD0	1	100DI FF	I FPF_TXD0	I FPF_TXD0	1	100DI FF	I FPF_AUX	I FPF_AUX	1	100DI FF
I FPE_TXD1*	I FPE_TXD1	1	100DI FF	I FPF_TXD1*	I FPF_TXD1	1	100DI FF				
I FPE_TXD1	I FPE_TXD1	1	100DI FF	I FPF_TXD1	I FPF_TXD1	1	100DI FF				
I FPE_TXD2*	I FPE_TXD2	1	100DI FF	I FPF_TXD2*	I FPF_TXD2	1	100DI FF				
I FPE_TXD2	I FPE_TXD2	1	100DI FF	I FPF_TXD2	I FPF_TXD2	1	100DI FF				

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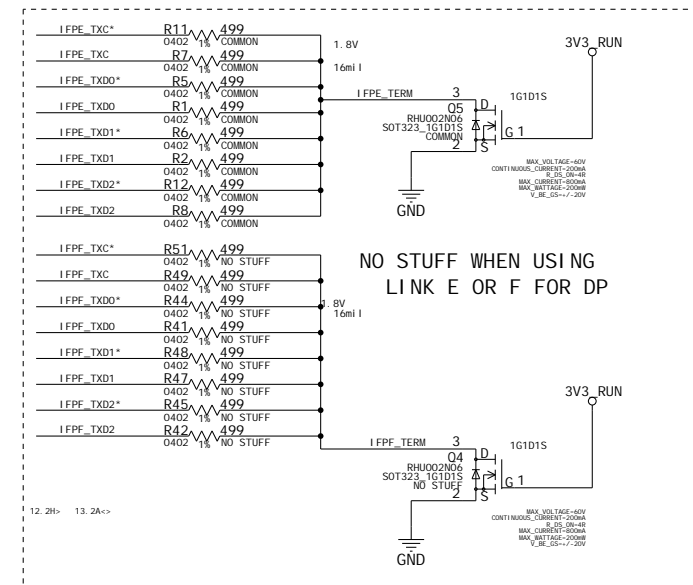
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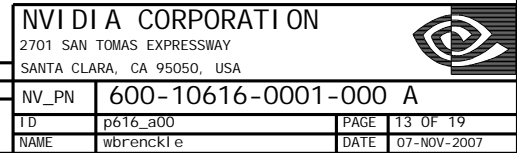
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CN1
CON_MXM_X16_EDGE
(NON)PHY(-X16, -HE)
NONPHY-X16
COMMON

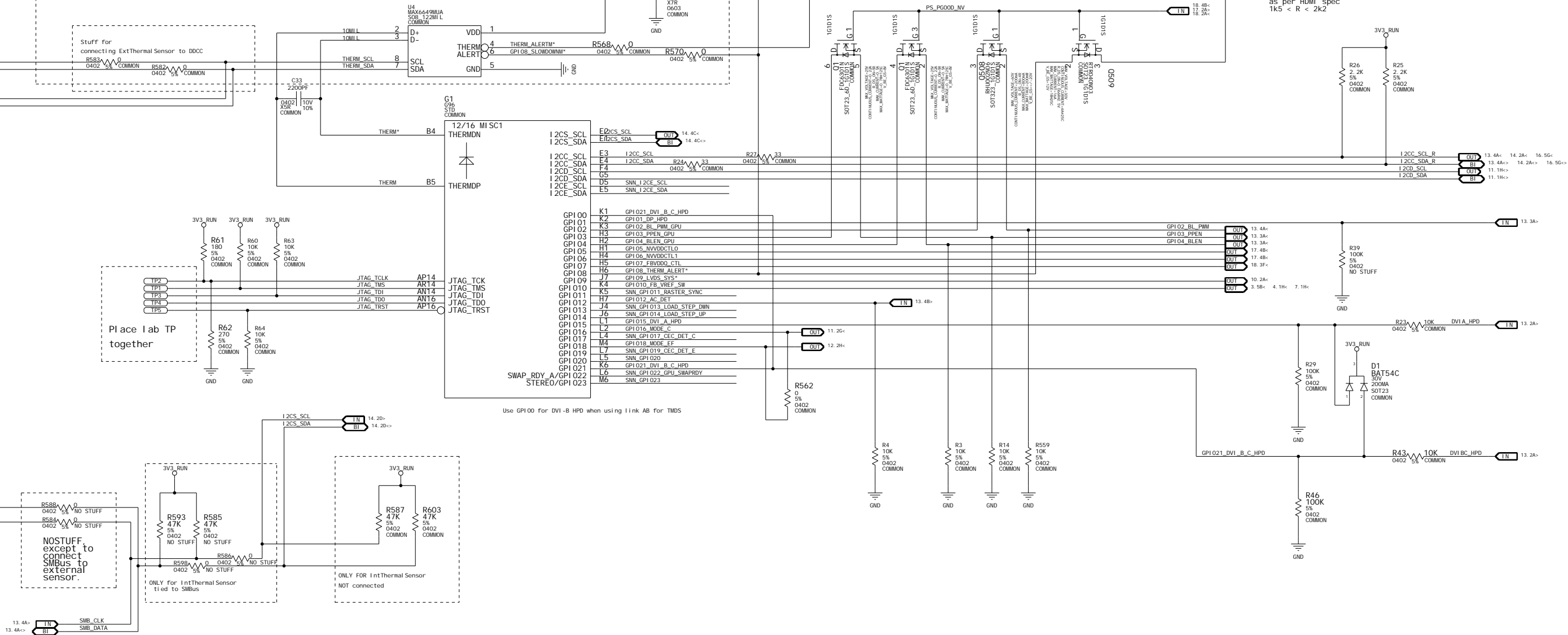


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GPI0, TEMP SENSOR, JTAG

I2C ADDRESS: 0x98H

NOSTUFF for internal sensor



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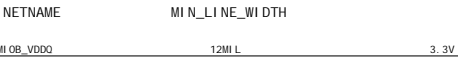


ASSEMBLY	NB9P-GS G96M 400MHz, 512MB(128bit) GDDR3 32Mx32 84FBGA, LVDS + DP + HDMI + SD/HD(TV_OUT) + VGA
PAGE DETAIL	GPI0, JTAG, TEMP SENSOR

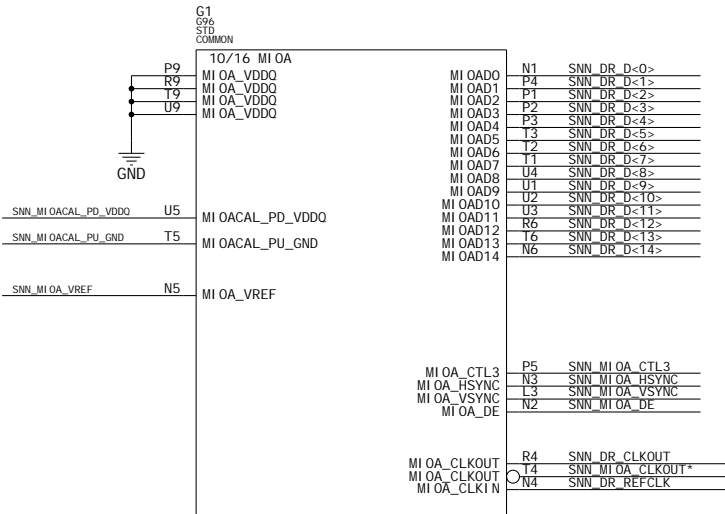
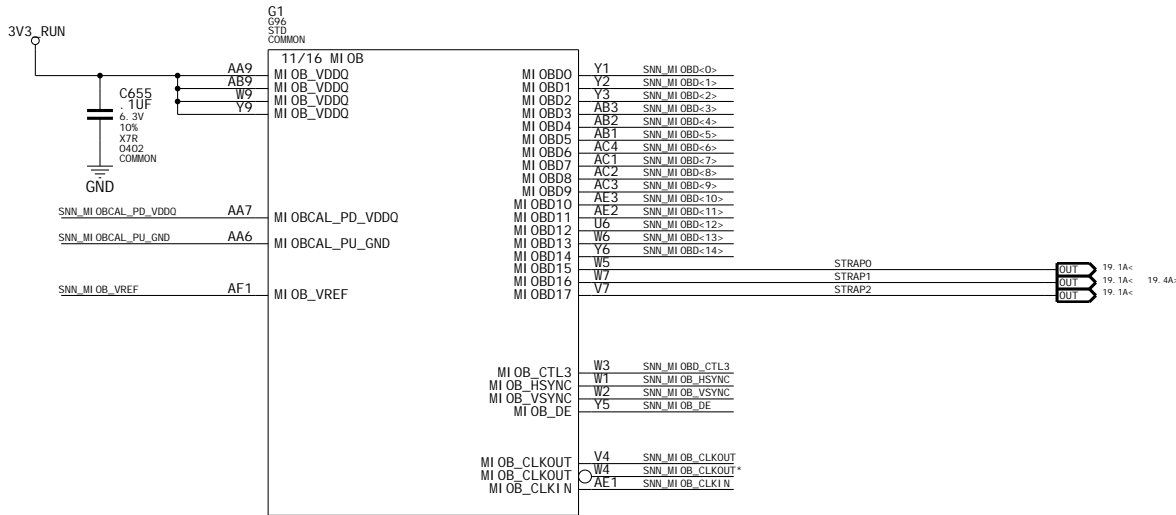
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ID	p616_a00	PAGE 14 OF 19
NAME	wbrenckle	DATE 07-NOV-2007

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MI 0A/B



(MI OB CONSTRAI NTS)



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ASSEMBLY N89P-GS G96M 400MHz, 512MB(128bit) GDDR3 32Mx32 84FBGA, LVDS + DP + HDMI + SD/HD(TV_OUT) + VGA

PAGE DETAIL MI 0 A/B

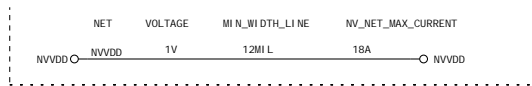
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ID p616_a00 PAGE 15 OF 19

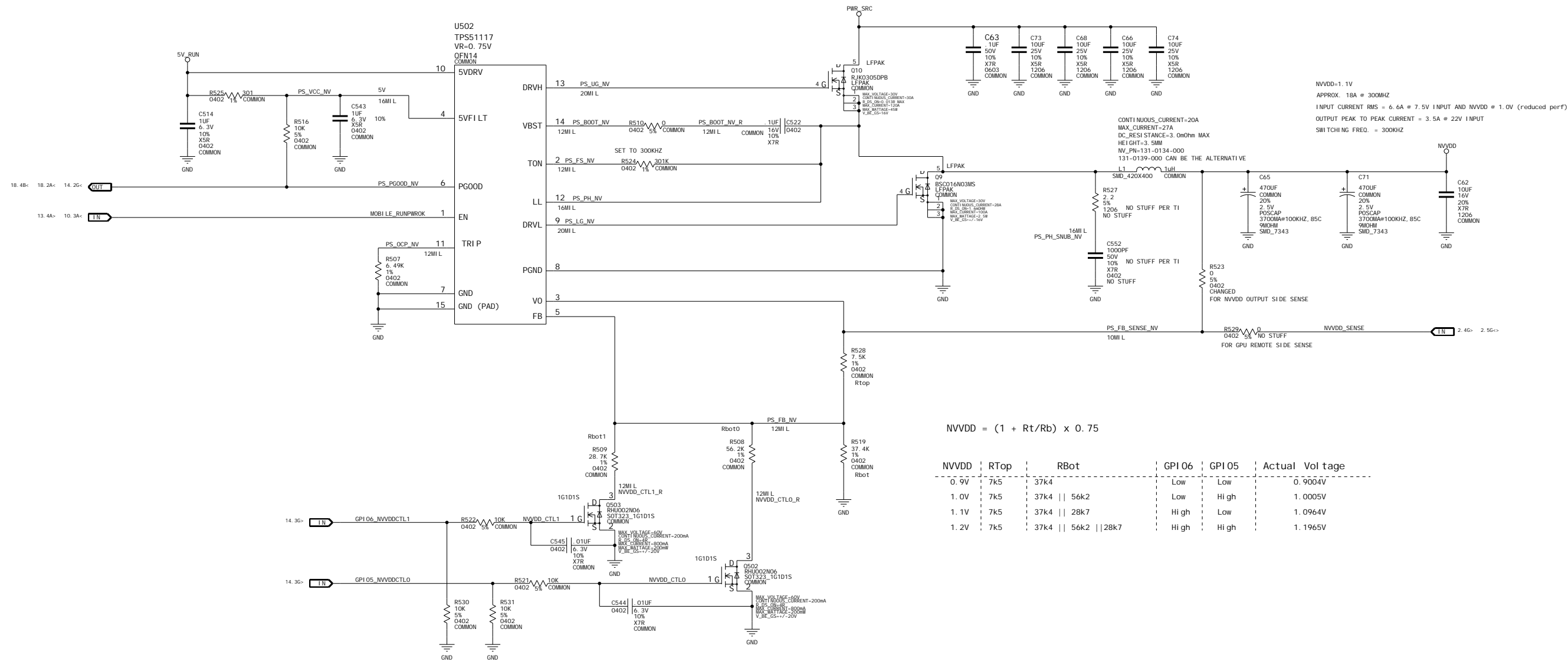
NAME wbrenckle DATE 07-NOV-2007

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NVVDD POWER SUPPLY



NVVDD SWITCHER POWER SUPPLY



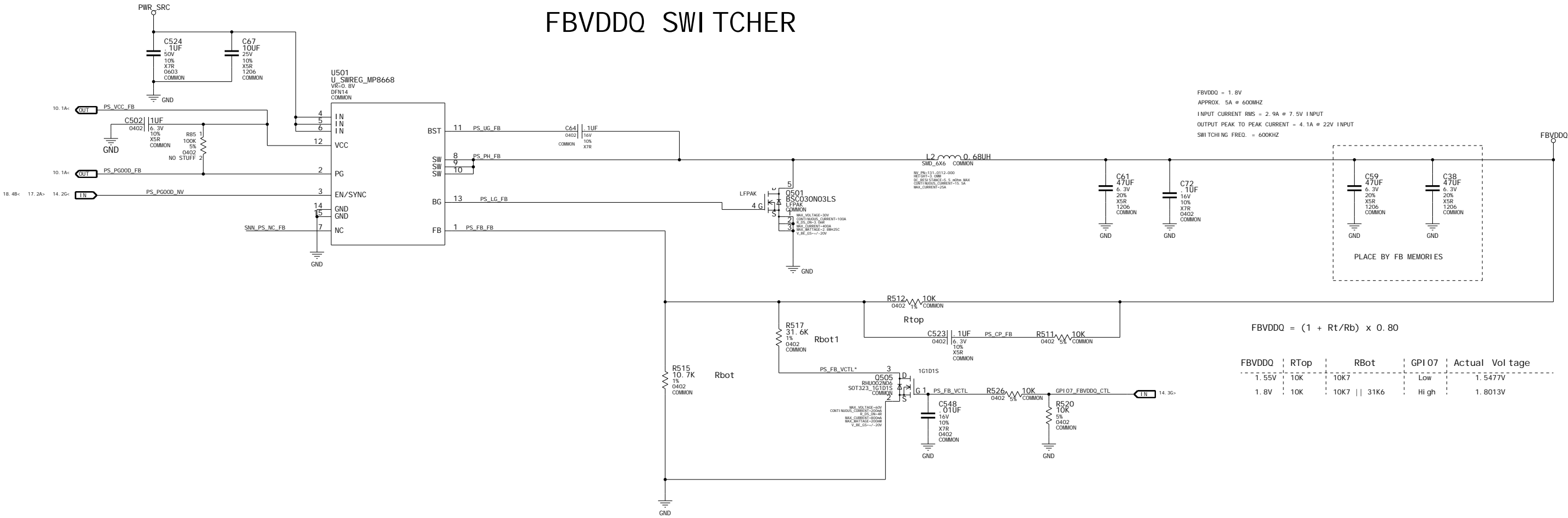
$$NVVDD = (1 + R_t/R_b) \times 0.75$$

NVVD	RTop	RBot	GPI 06	GPI 05	Actual	Vol tage
0.9V	7k5	37k4	Low	Low	0.9004V	
1.0V	7k5	37k4 56k2	Low	Hi gh	1.0005V	
1.1V	7k5	37k4 28k7	Hi gh	Low	1.0964V	
1.2V	7k5	37k4 56k2 28k7	Hi gh	Hi gh	1.1965V	

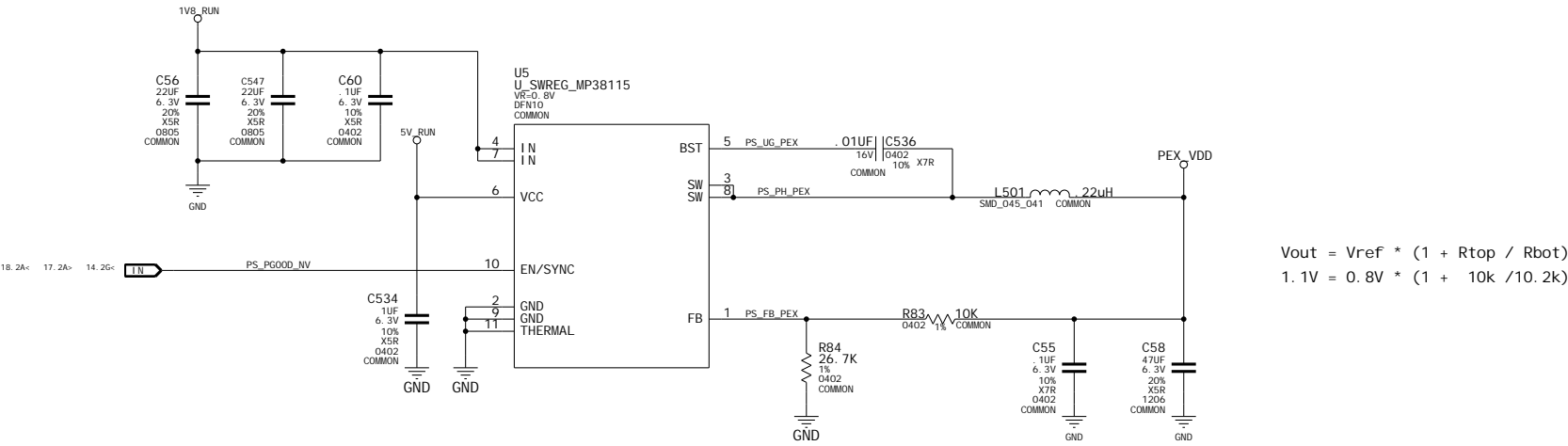
FBVDDQ AND PEX_VDD POWER SUPPLY

NET	VOLTAGE	NV_NET_MAX_CURRENT
PEX_VDD	1.1V	4A
FBVDDQ	1.8V	5A

FBVDDQ SWITCHER



PEX_VDD SWITCHER



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ASSEMBLY

PAGE DETAIL

NB9P-GS G96M 400MHz, 512MB(128bit) GDDR3 32Mx32 84FBGA, LVDS + DP + HDMI + SD/HD(TV_OUT) + VGA

FBVDDQ AND PEX_VDD POWER SUPPLY

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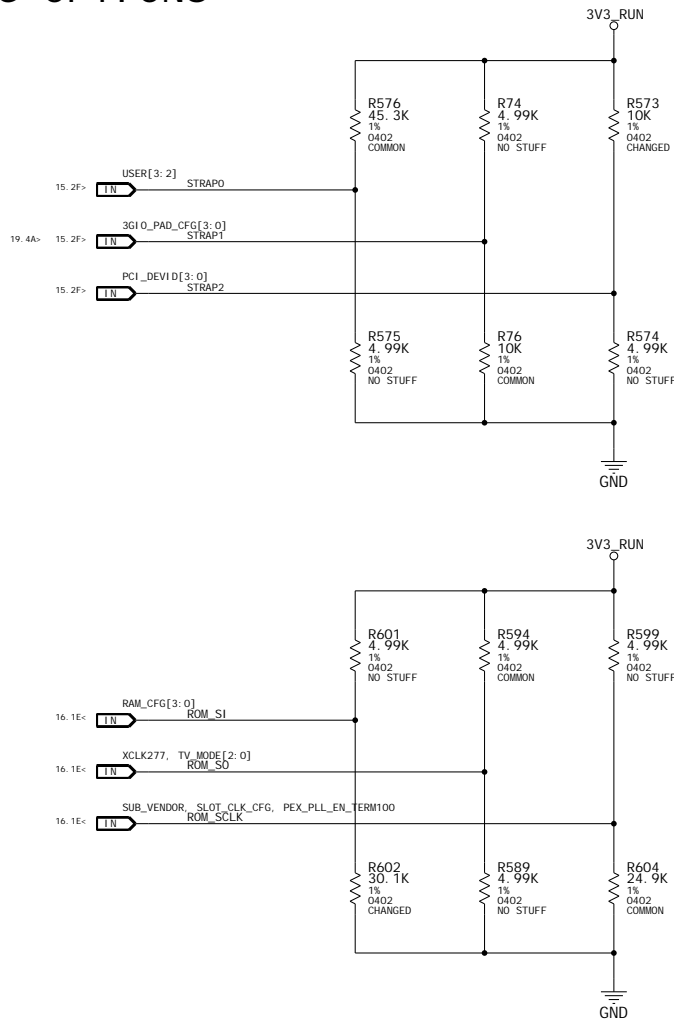
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STRAPPING OPTIONS



	3V3	GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

STRAP0

USER_BIT0 0xF: 45K PU (unused)

USER_BIT1

USER_BIT2

USER_BIT3

STRAP1

3GIO_PADCFG_LUT_ADR0

3GIO_PADCFG_LUT_ADR1

0x0: Desktop default (normal swing) - 5k PD

3GIO_PADCFG_LUT_ADR2

0x1: Mobile default (low swing) - 10k PD

3GIO_PADCFG_LUT_ADR3

acc. to //hw/tesla_g98b/manuals/dev_ext_devices.ref

STRAP2

PCI_DEVID_0

all 4 bits set by HW strapping

PCI_DEVID_1

0x0649: 10K PU (NB9P-GS)

PCI_DEVID_2

0x0648: 5K PU (NB9P-GE2)

PCI_DEVID_3

ROM_SI

TV_MODE_BIT0

0x0: NTSC-M

TV_MODE_BIT1

5K PU

TV_MODE_BIT2

XCLK_277

1: PCI-E GEN2

ROM_SI

RAM_CFG_0 256 MB (4pcs. 16Mx32)

512 MB (4pcs. 32Mx32)

RAM_CFG_1 RAM_CFG[3:0] Definitions

RAM_CFG[3:0] Definitions

RAM_CFG_2 0000 Reserved

0100 25k PD Reserved

RAM_CFG_3 0001 Dimonda

0101 30k PD Dimonda

PCI_DEVID_EXT

0:

SUB_VENDOR

1: SUB_VENDOR BIOS

25K PD

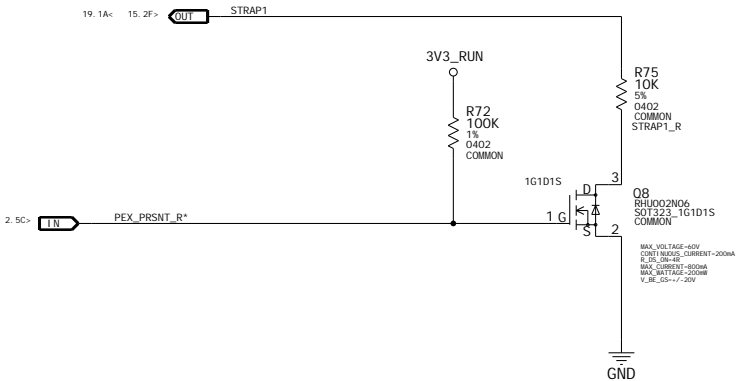
SLOT_CLK_CONFIG

0:

PEX_PLL_EN_TERM100

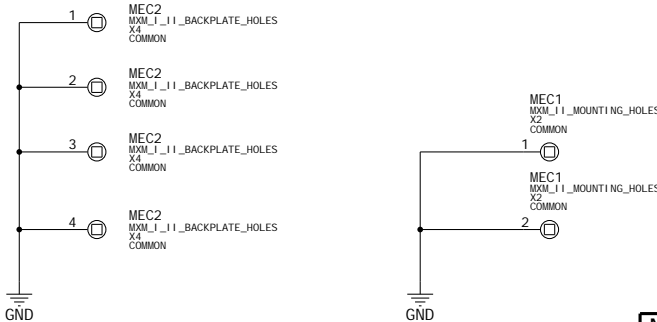
0: TERM100 DISABLED

PEX SWING LEVEL



PEX_PRST2_R	R_STRAP1	3GIO_PADCFG_LUT<3..0>
GND	10k	0x1 MOBILE_DEFAULT
FLOAT	5k (10k 10k)	0x0 DESKTOP_DEFAULT

MECHANICAL



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