

PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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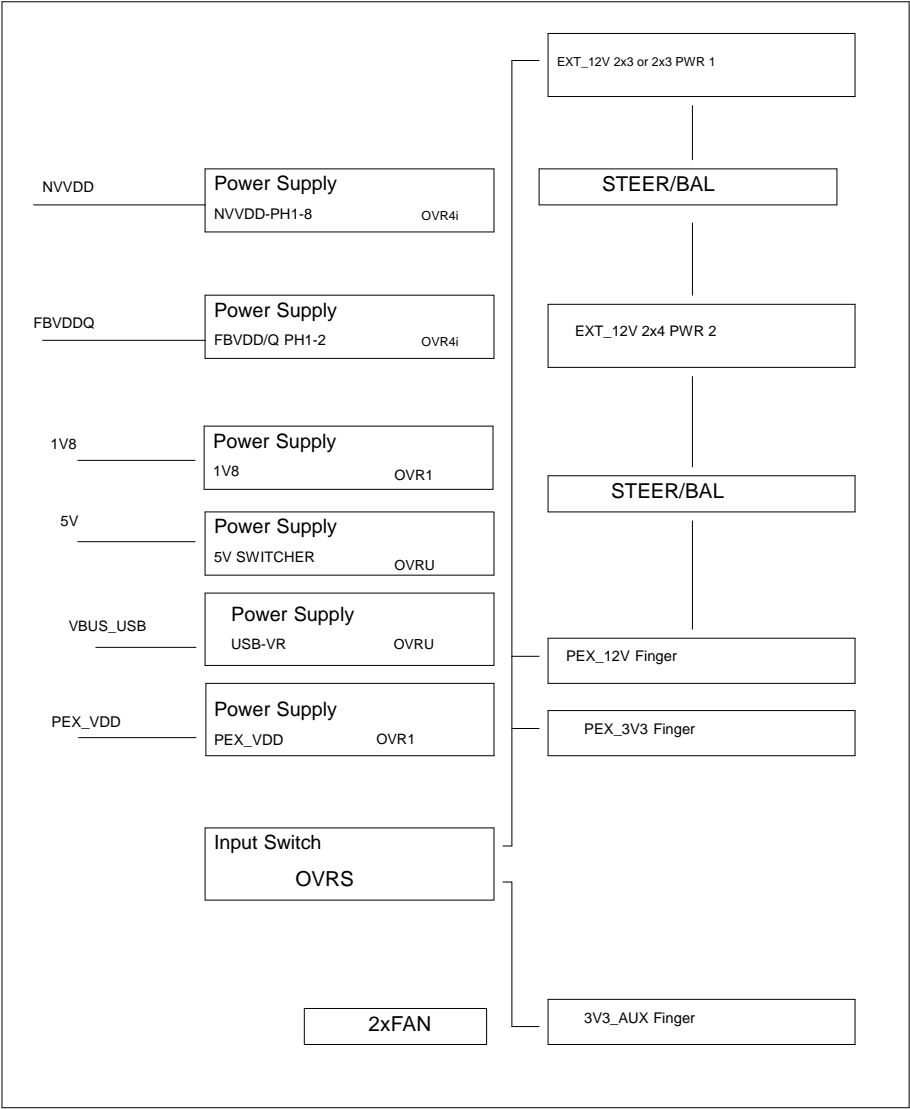
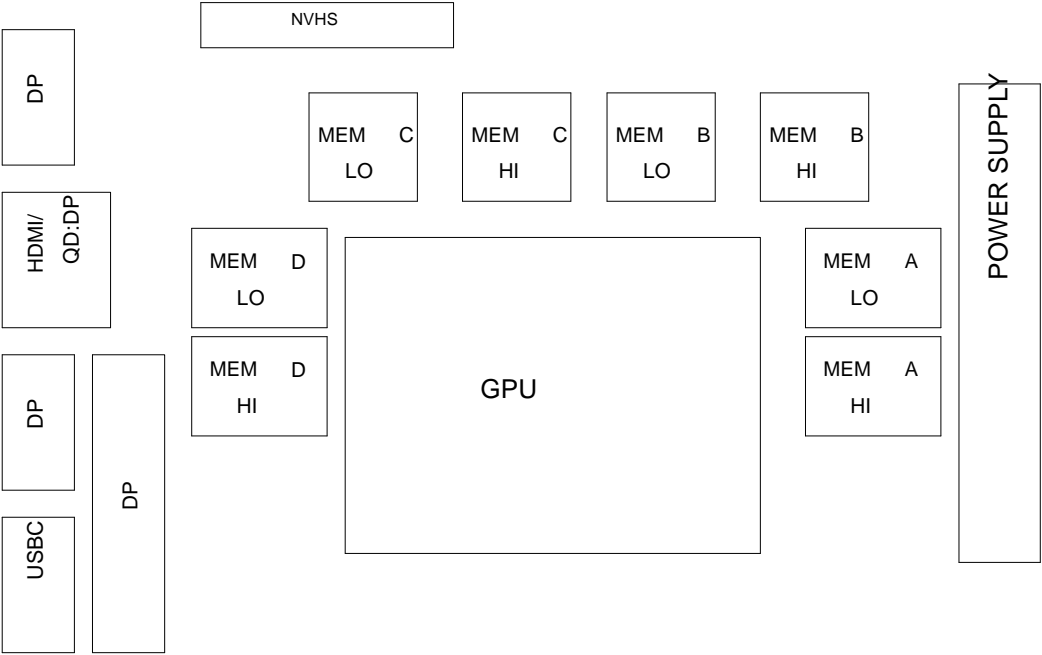
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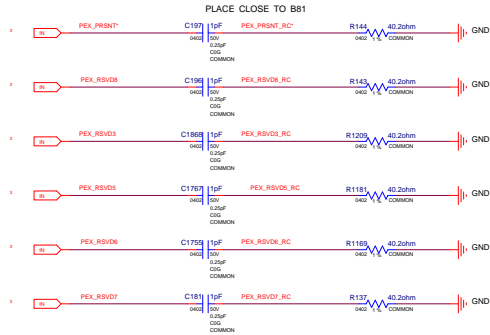
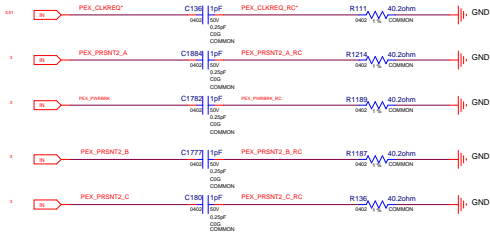
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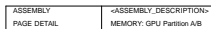
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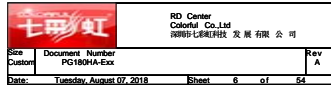


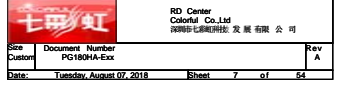
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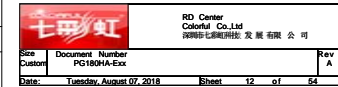
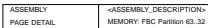


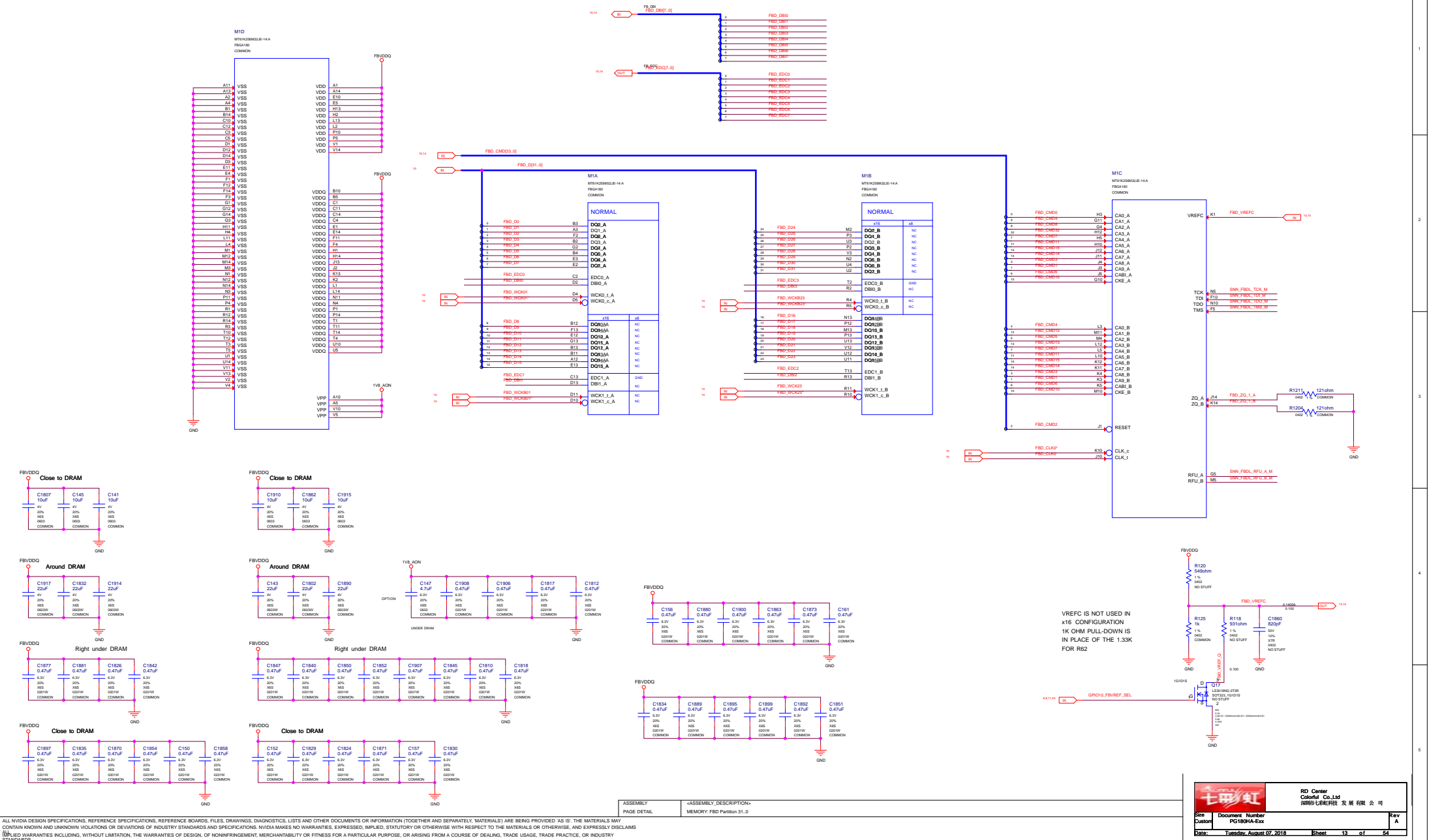




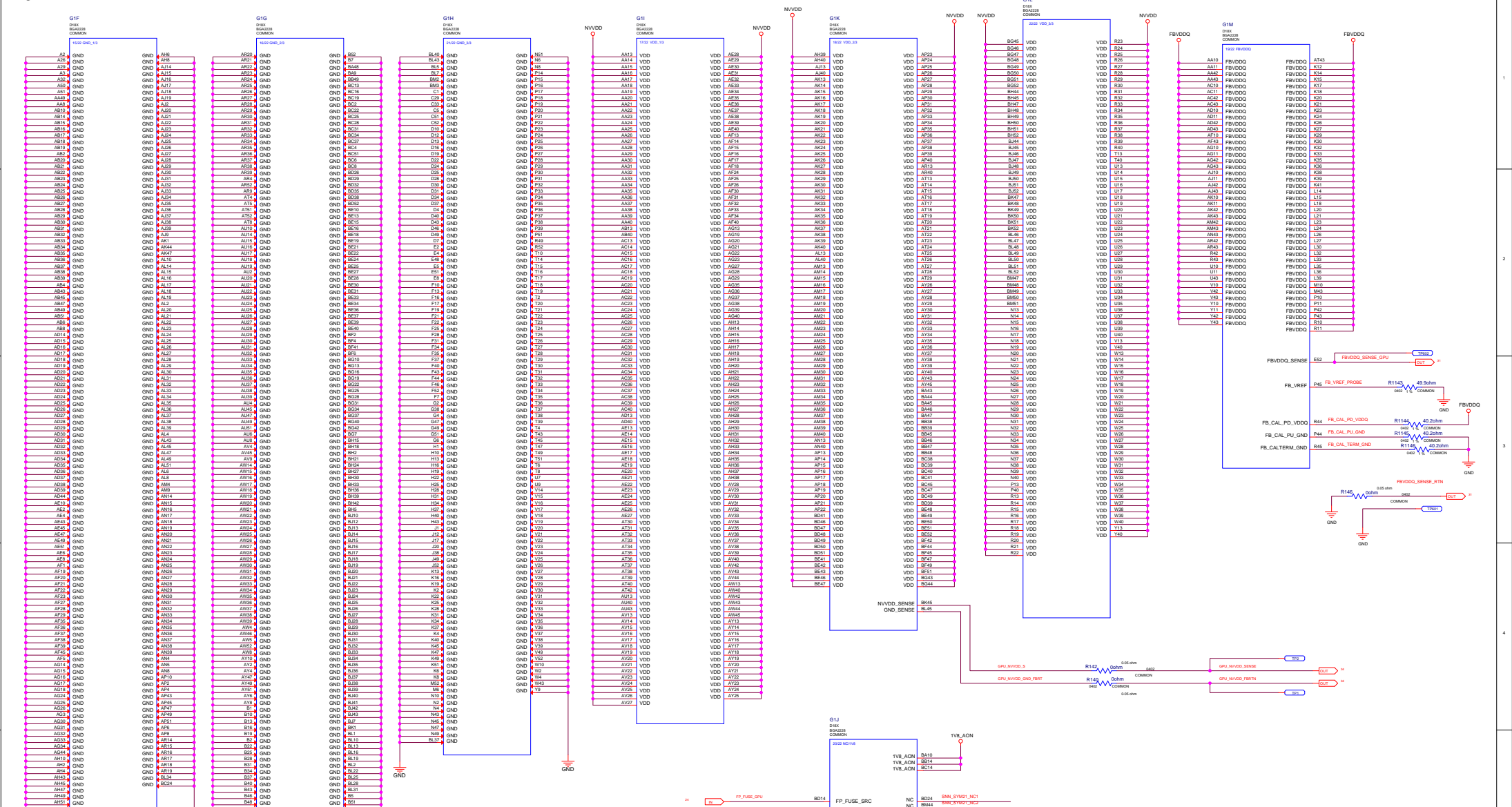






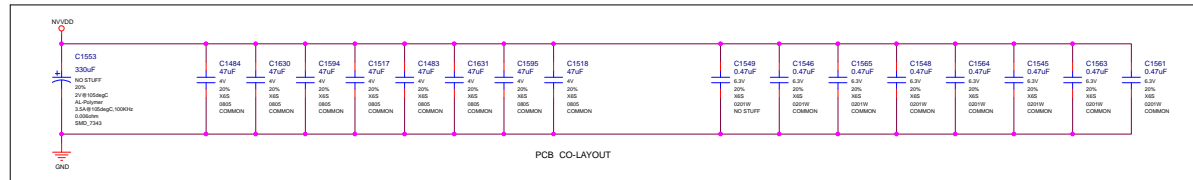
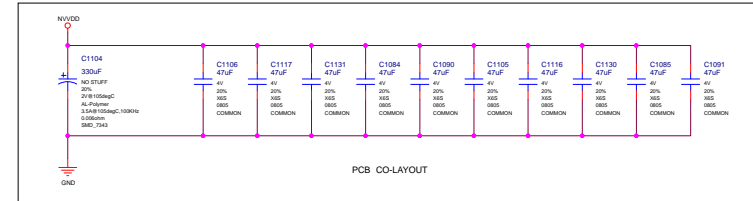
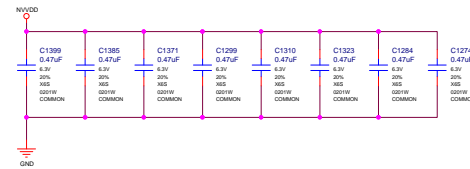
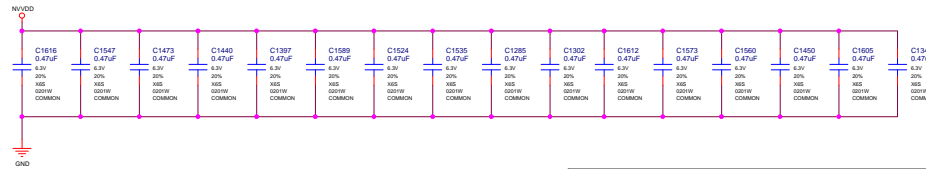
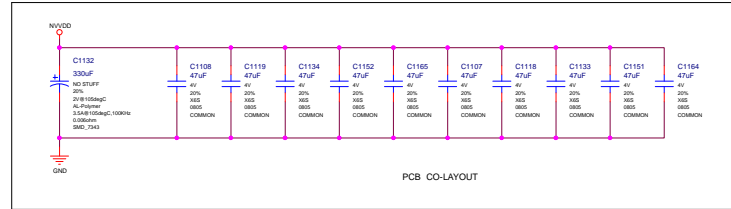
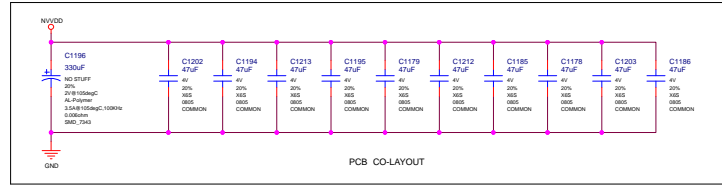
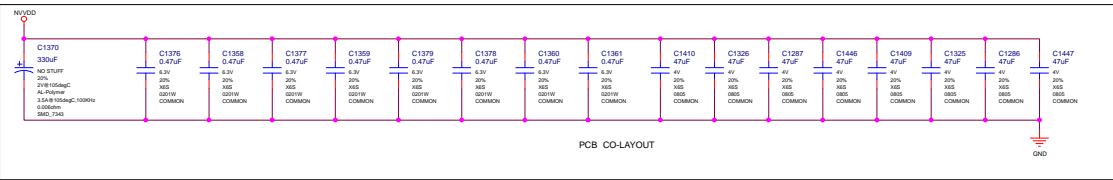







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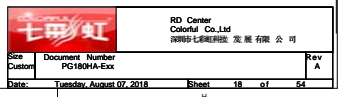
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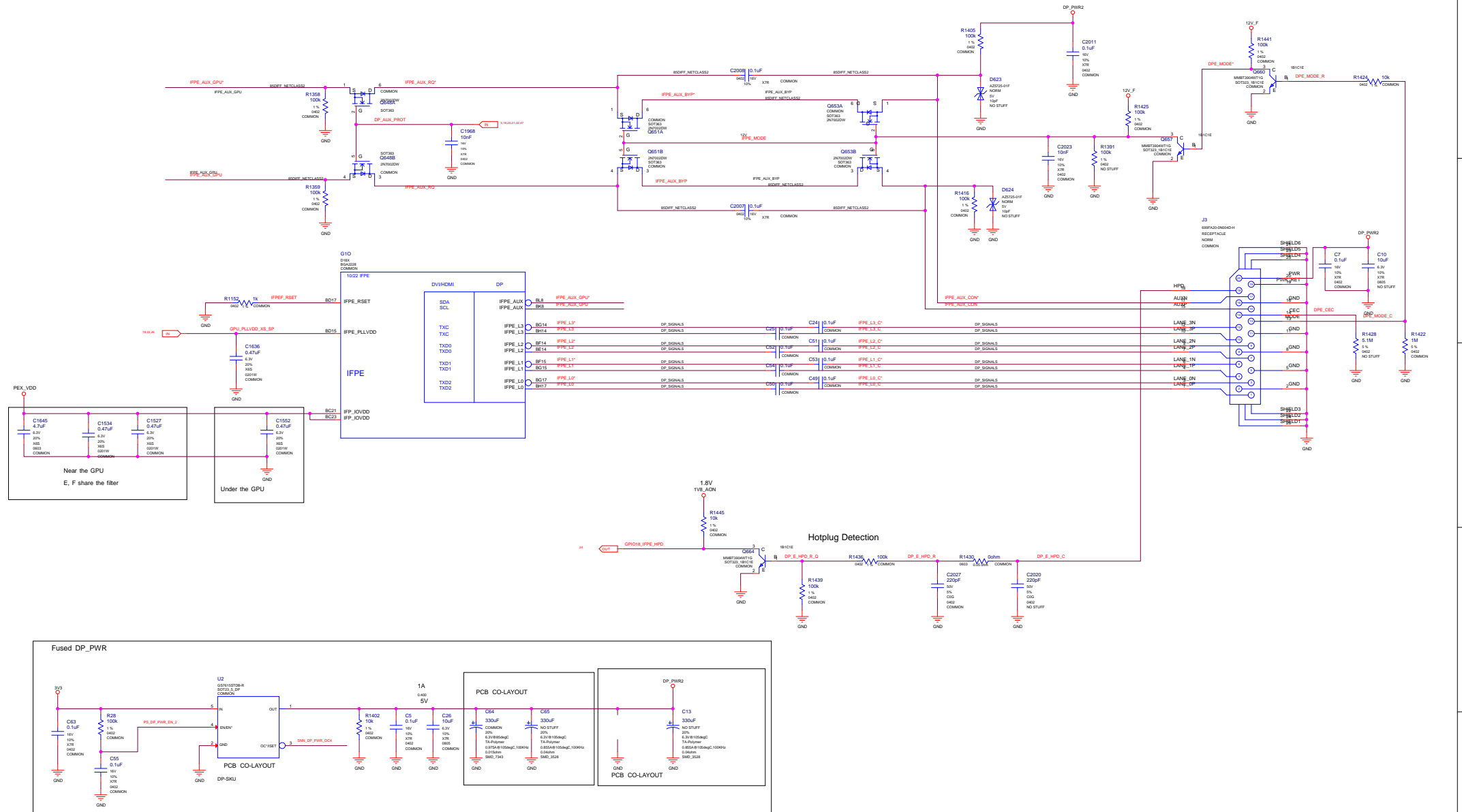


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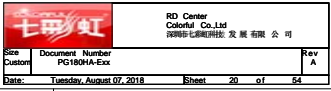
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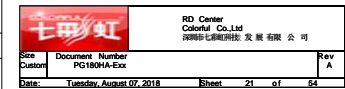




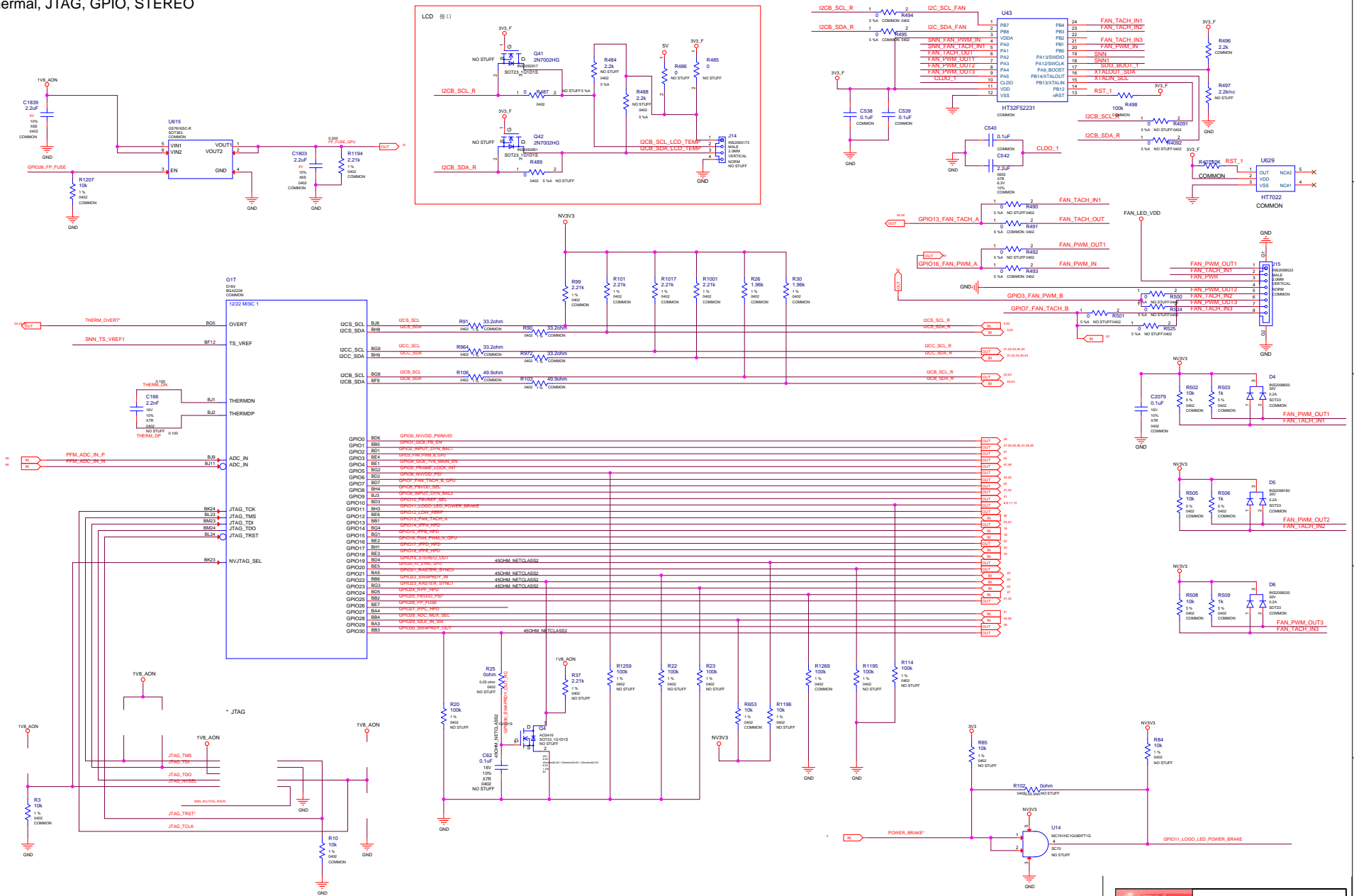
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IFPE DP










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PAGE DETAIL	MISC: FAN,THERMAL,JTAG,GPIO,STEREO

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H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

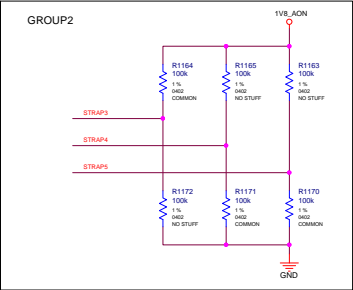
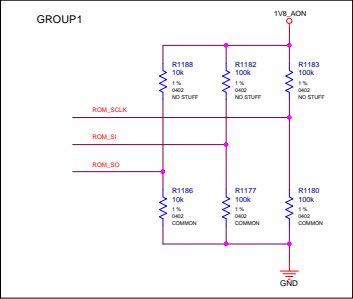
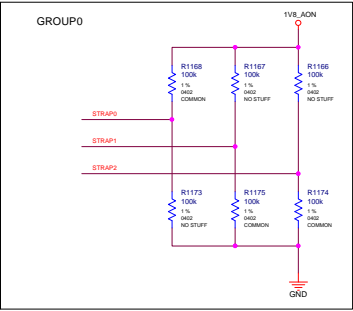
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

DEFAULT

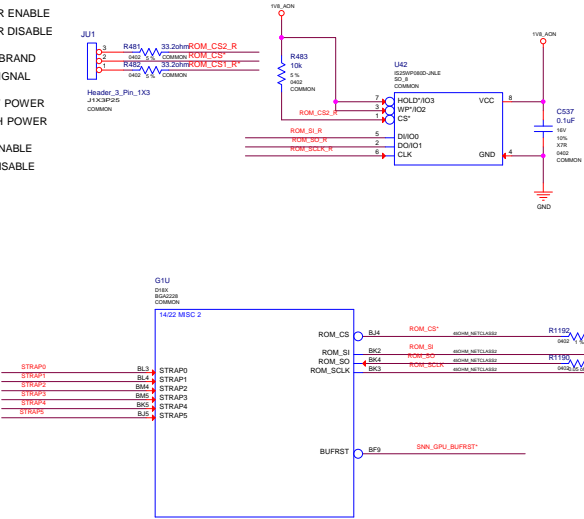
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

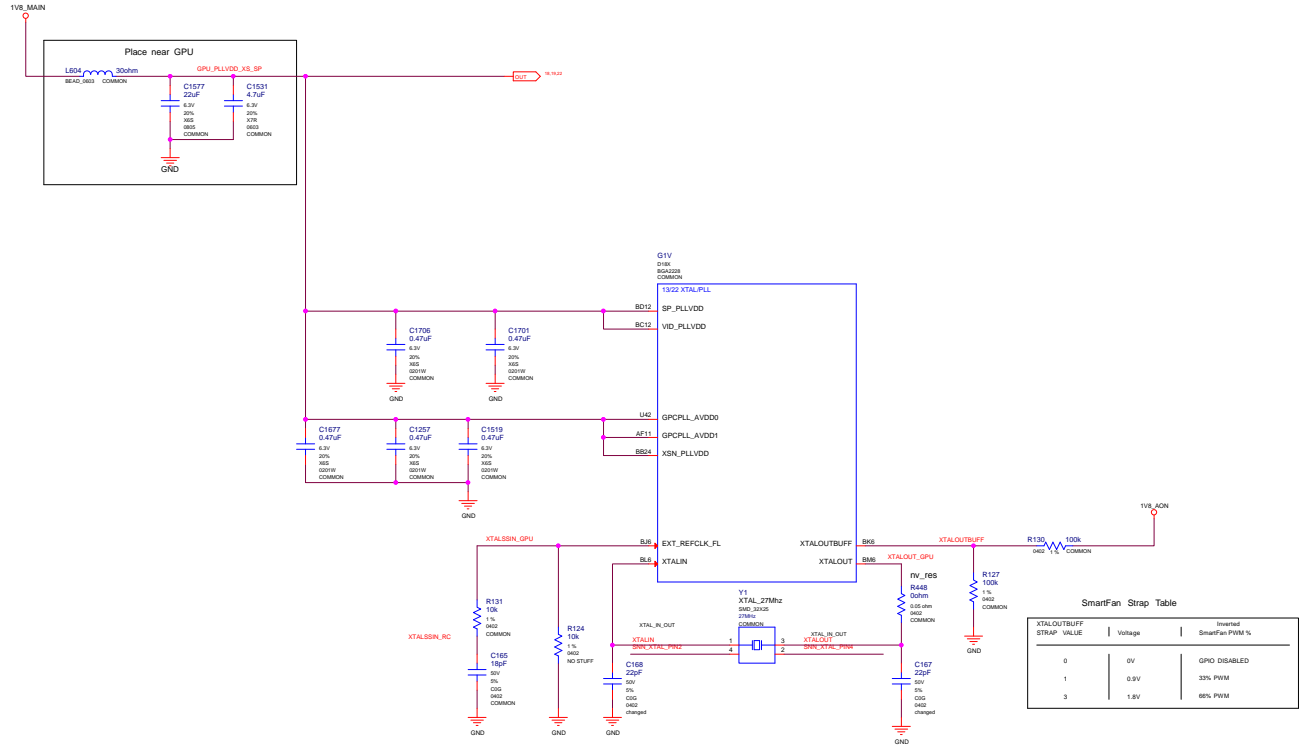
RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung



- 1:SMB_ALT_ADDR ENABLE
- 0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
- 0:DEVID_SEL ORIGINAL
- 1:PCIE_CFG LOW POWER
- 0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
- 0:VGA_DEVICE DISABLE



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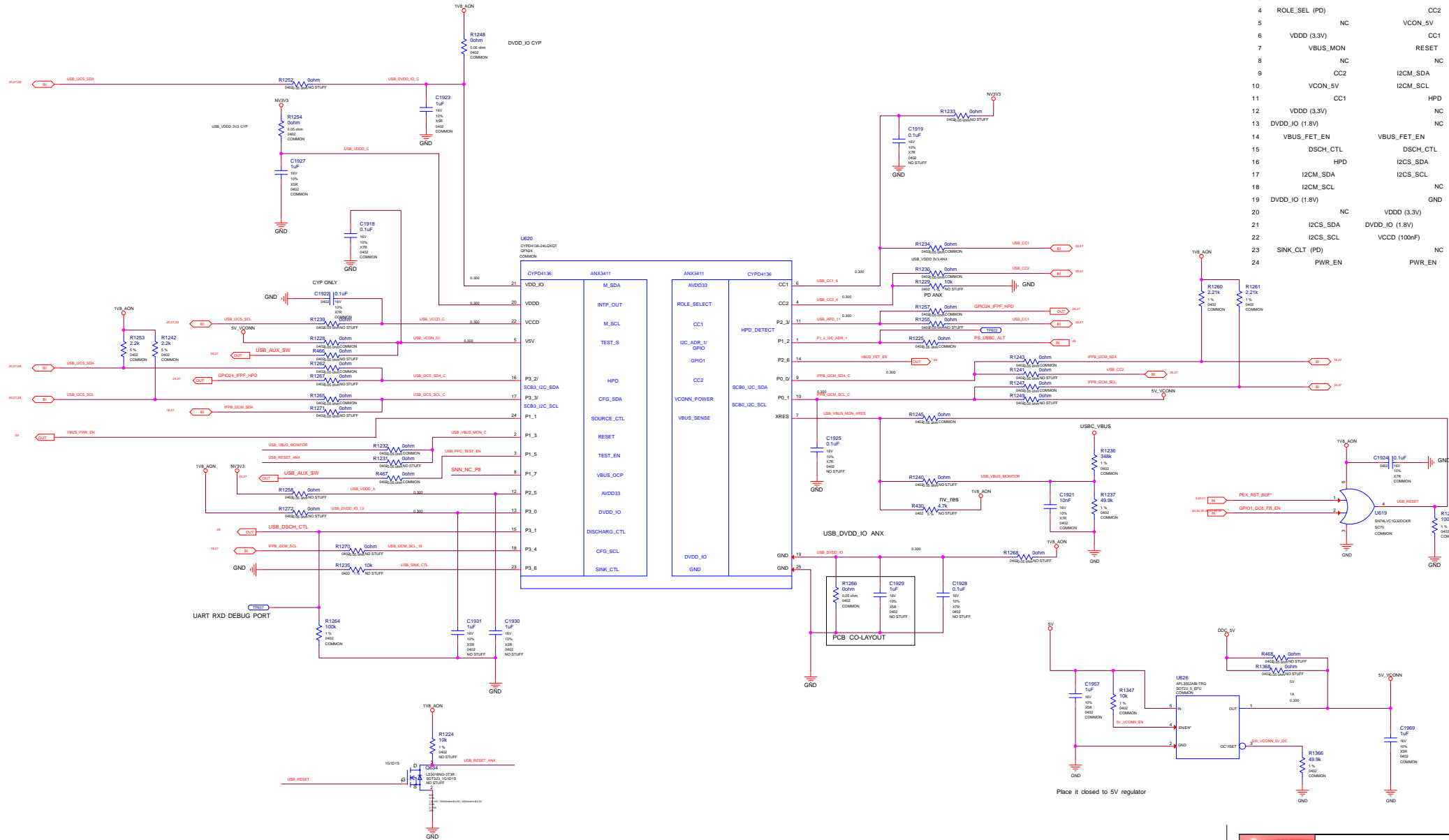


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PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100mF)
23	SINK_CTL (PD)	NC
24	PWR_EN	PWR_EN

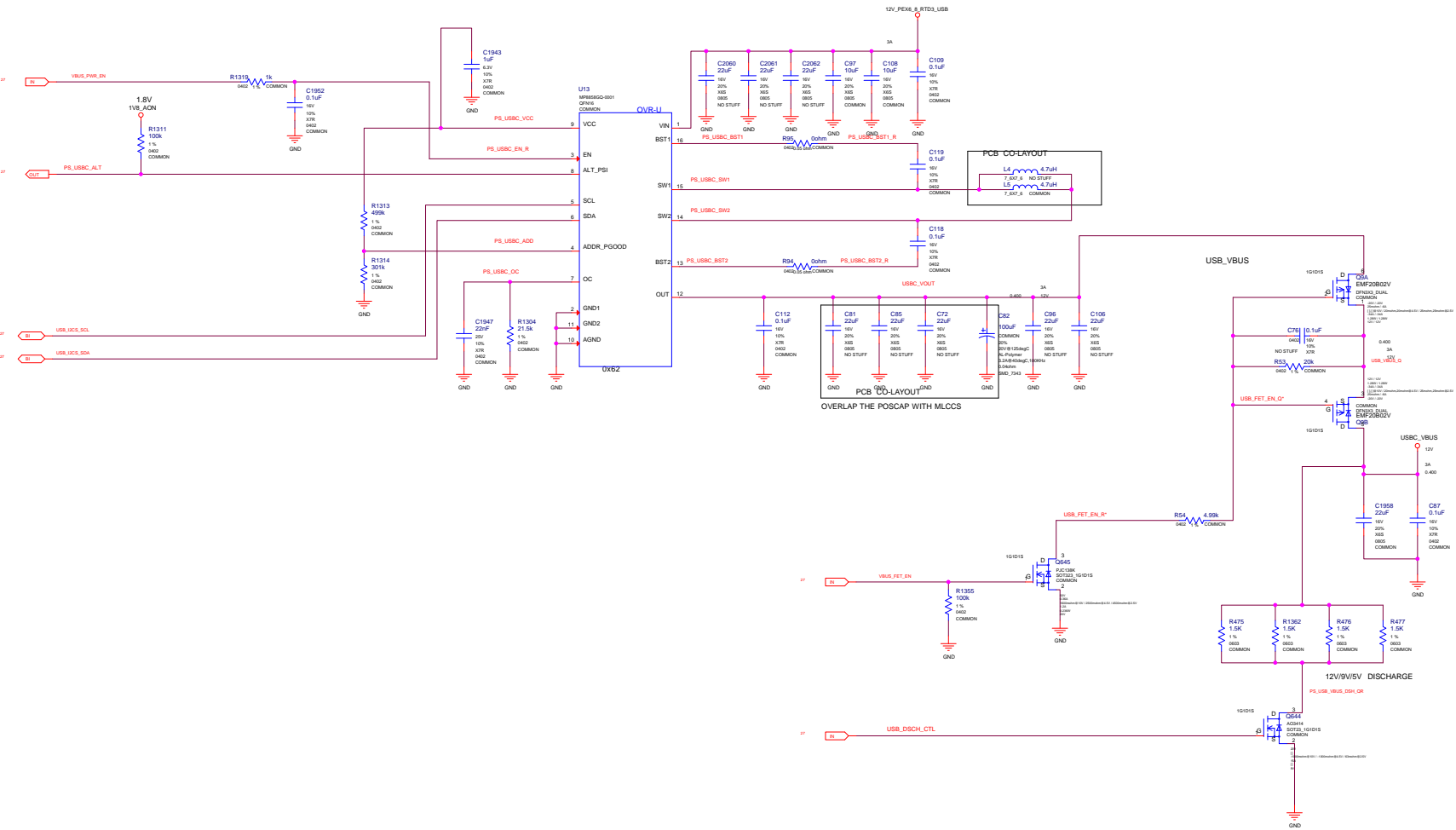
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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	MISC: USB PPC



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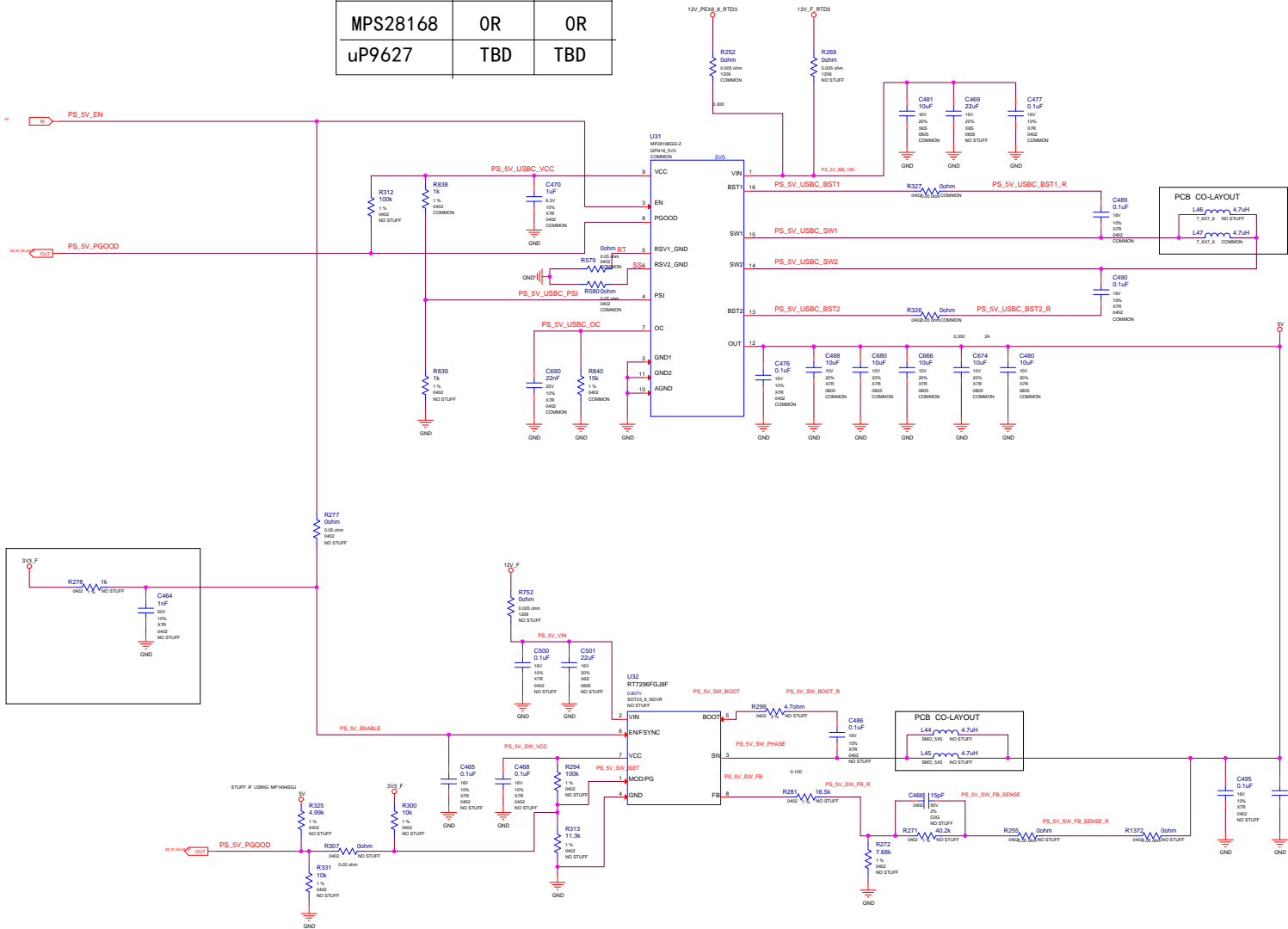


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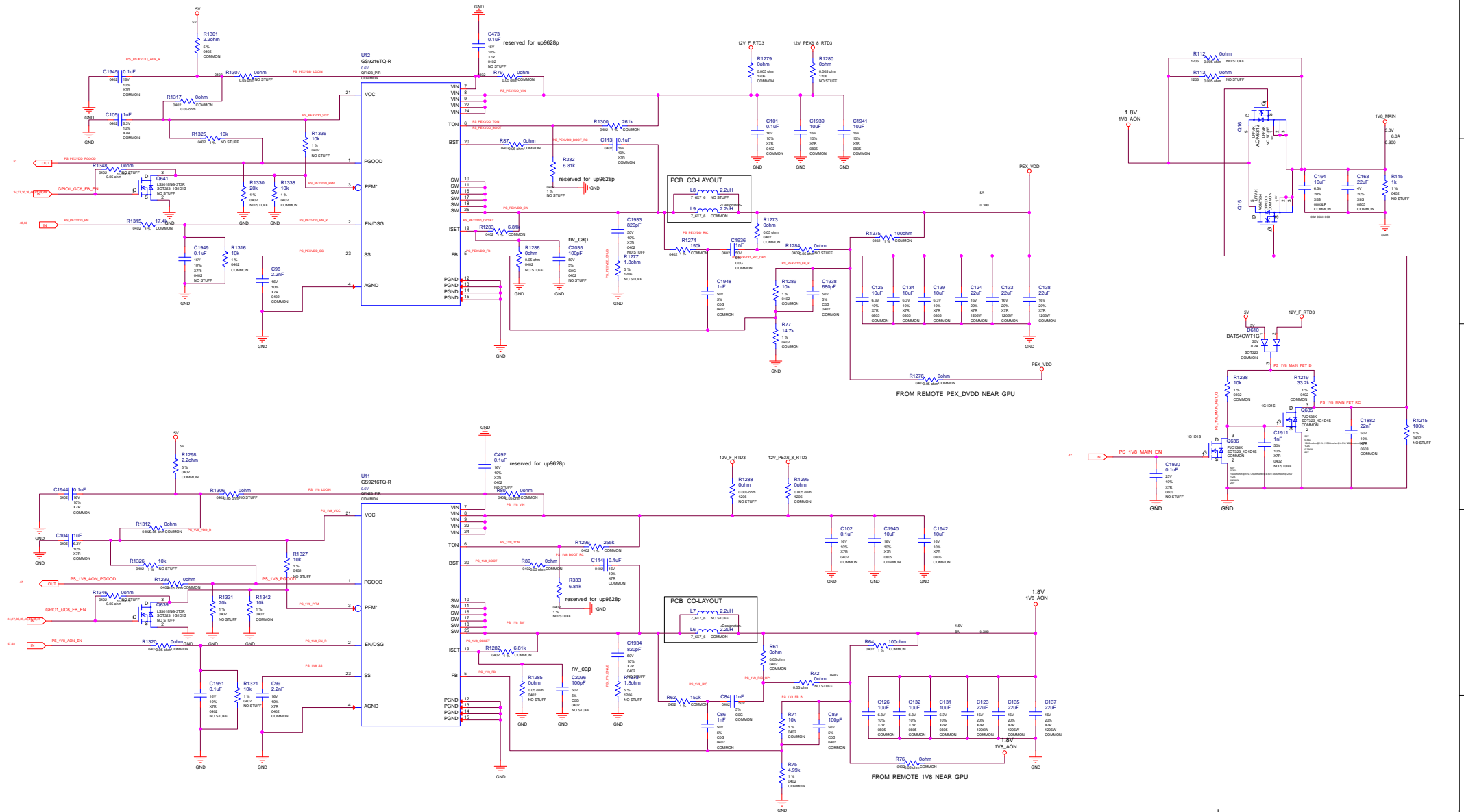
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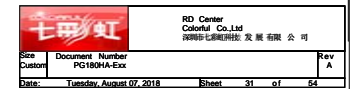
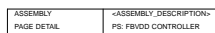
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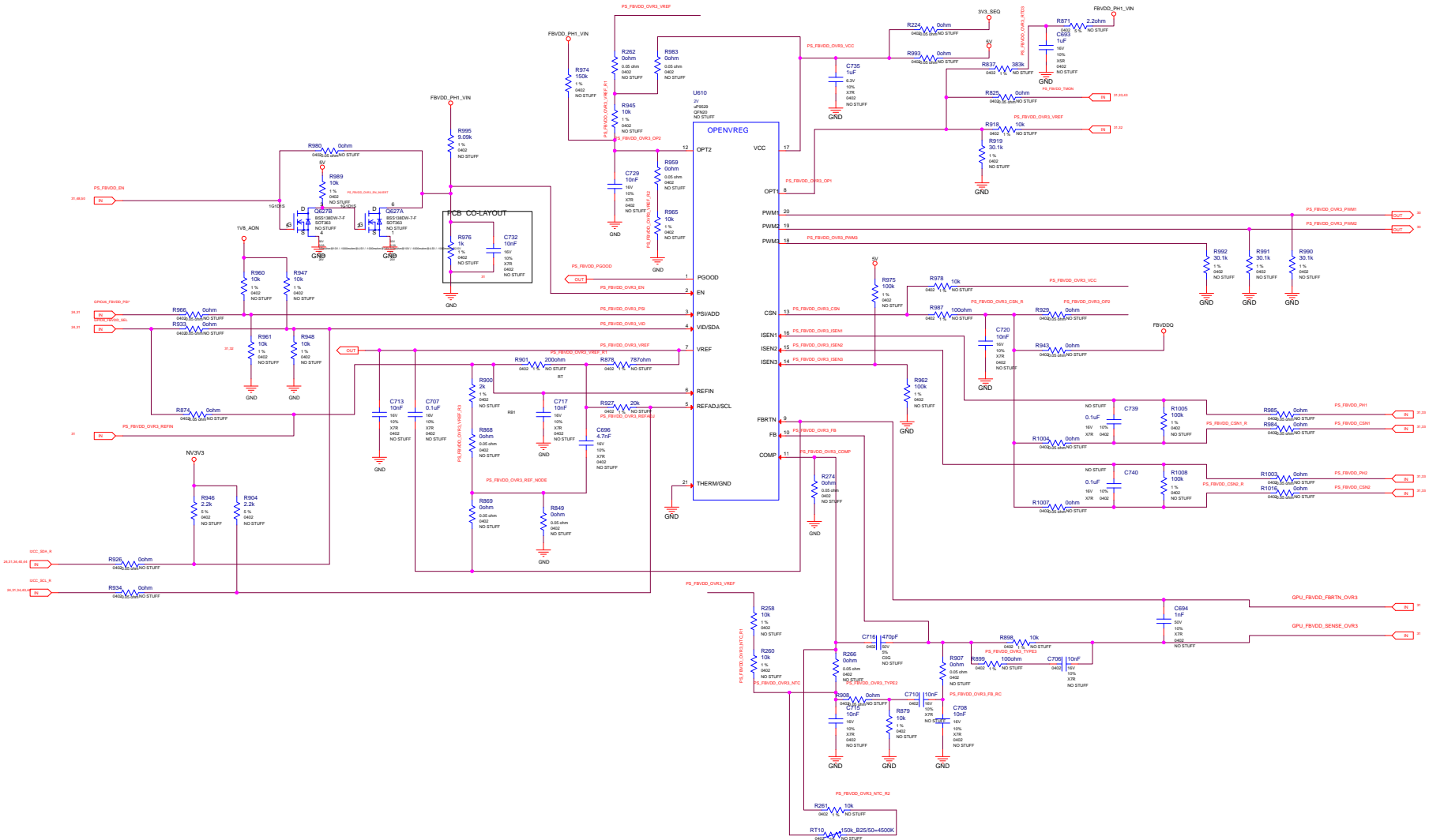




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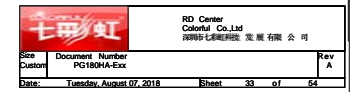
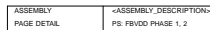


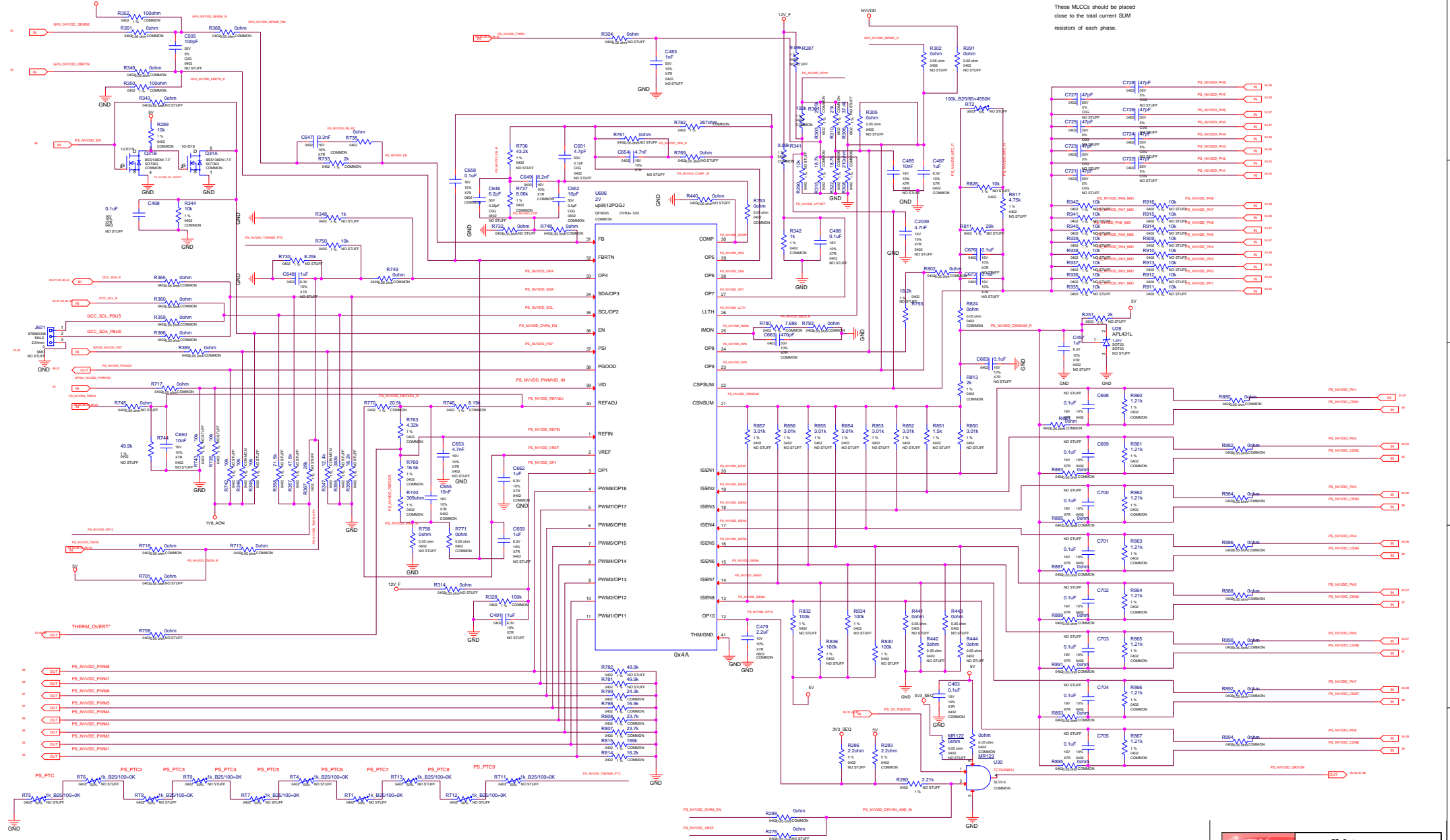


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ASSEMBLY PAGE DETAIL	ASSEMBLY DESCRIPTION PS: FBVDD CONTROLLER OVR3
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Size Custom	Document Number PS180A-Exc	Rev A	
Date: Tuesday, August 07, 2018		Sheet 32	of 64

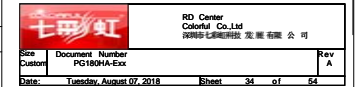


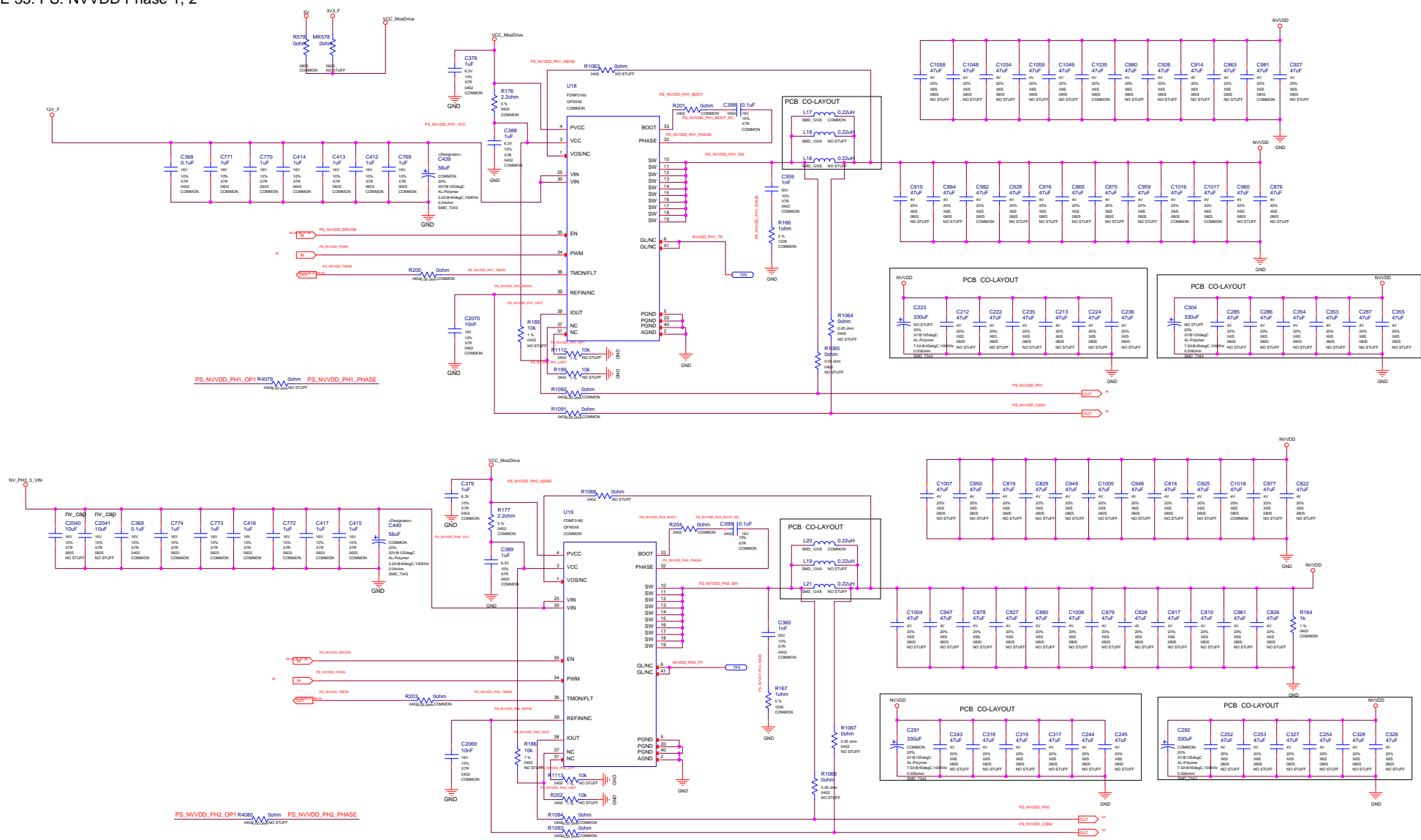


These MLCCs should be placed close to the total current SUM resistors of each phase.


ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	PS: NVVDD CONTROLLER OVR

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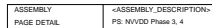


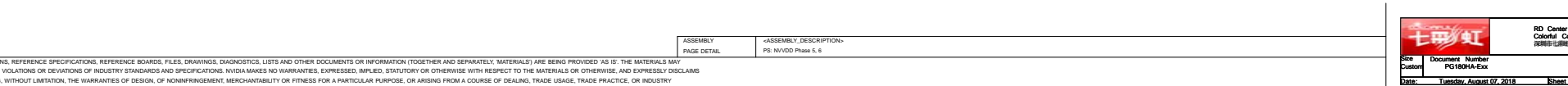


ASSEMBLY	ASSEMBLY DESCRIPTION
PS: NVVDD Phase 1, 2	

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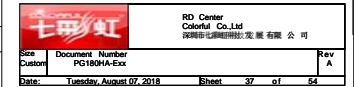
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A	B	C	D
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A horizontal timeline labeled "DAY" with a single tick mark.



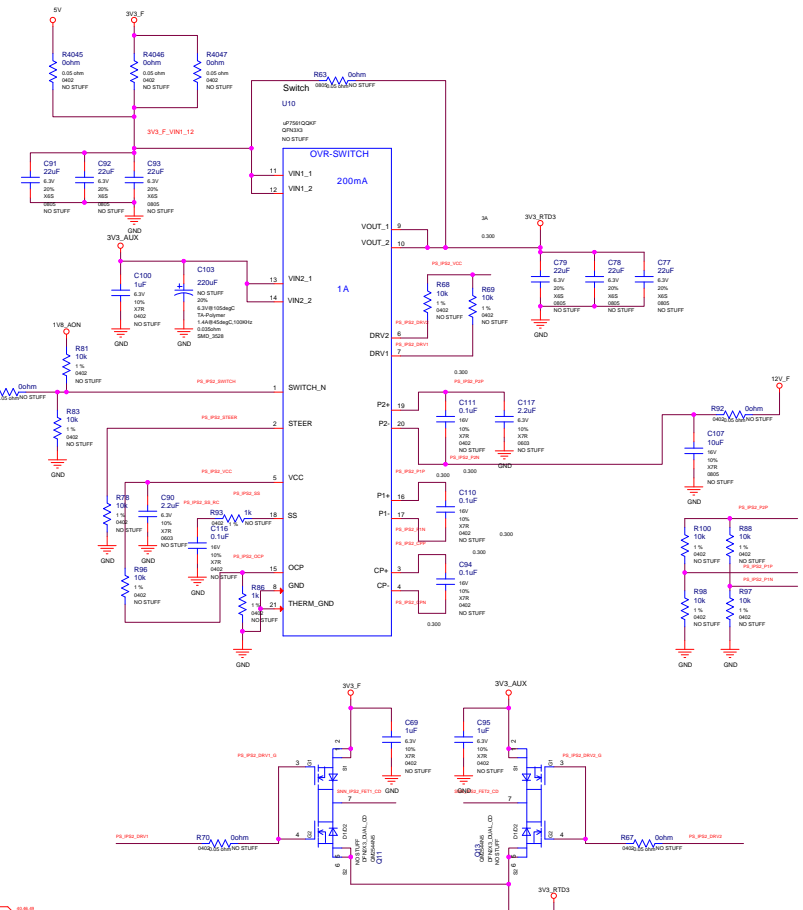
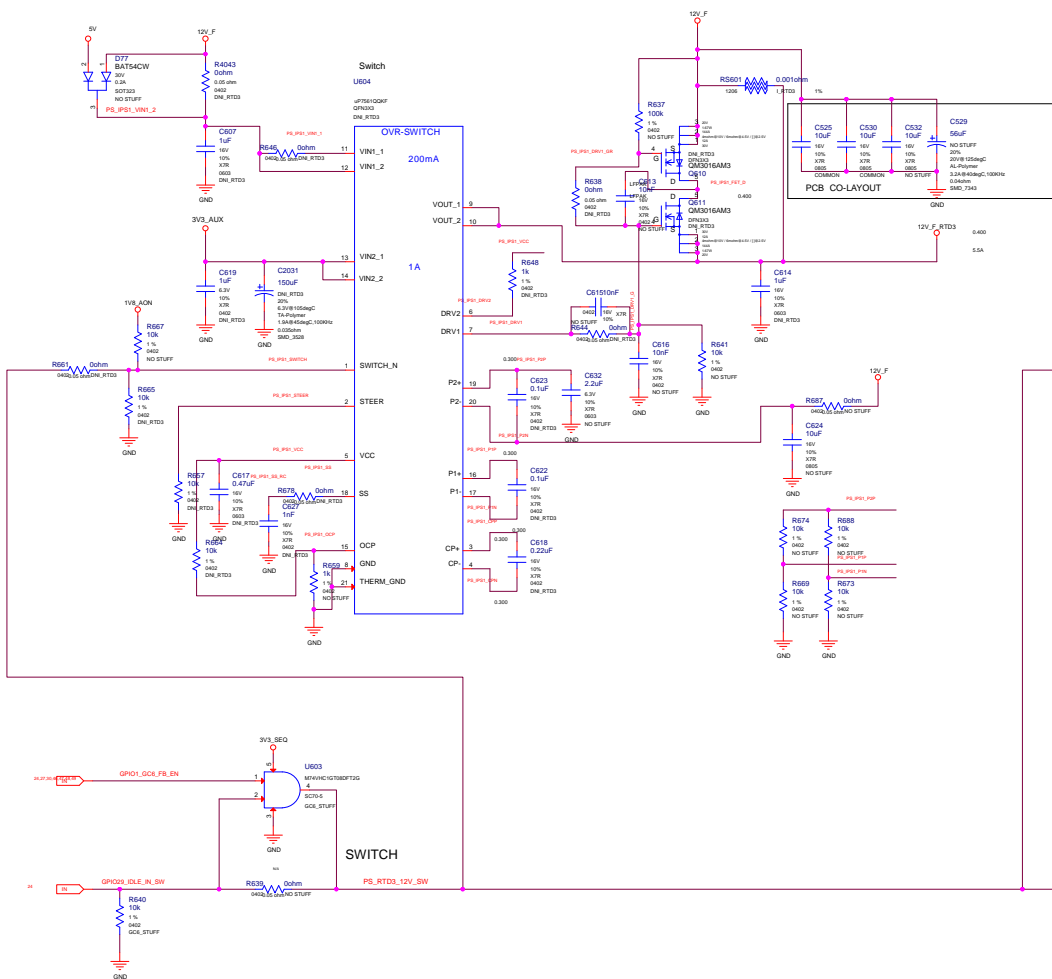


ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	PS: NVVDD Phase 7, 8

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

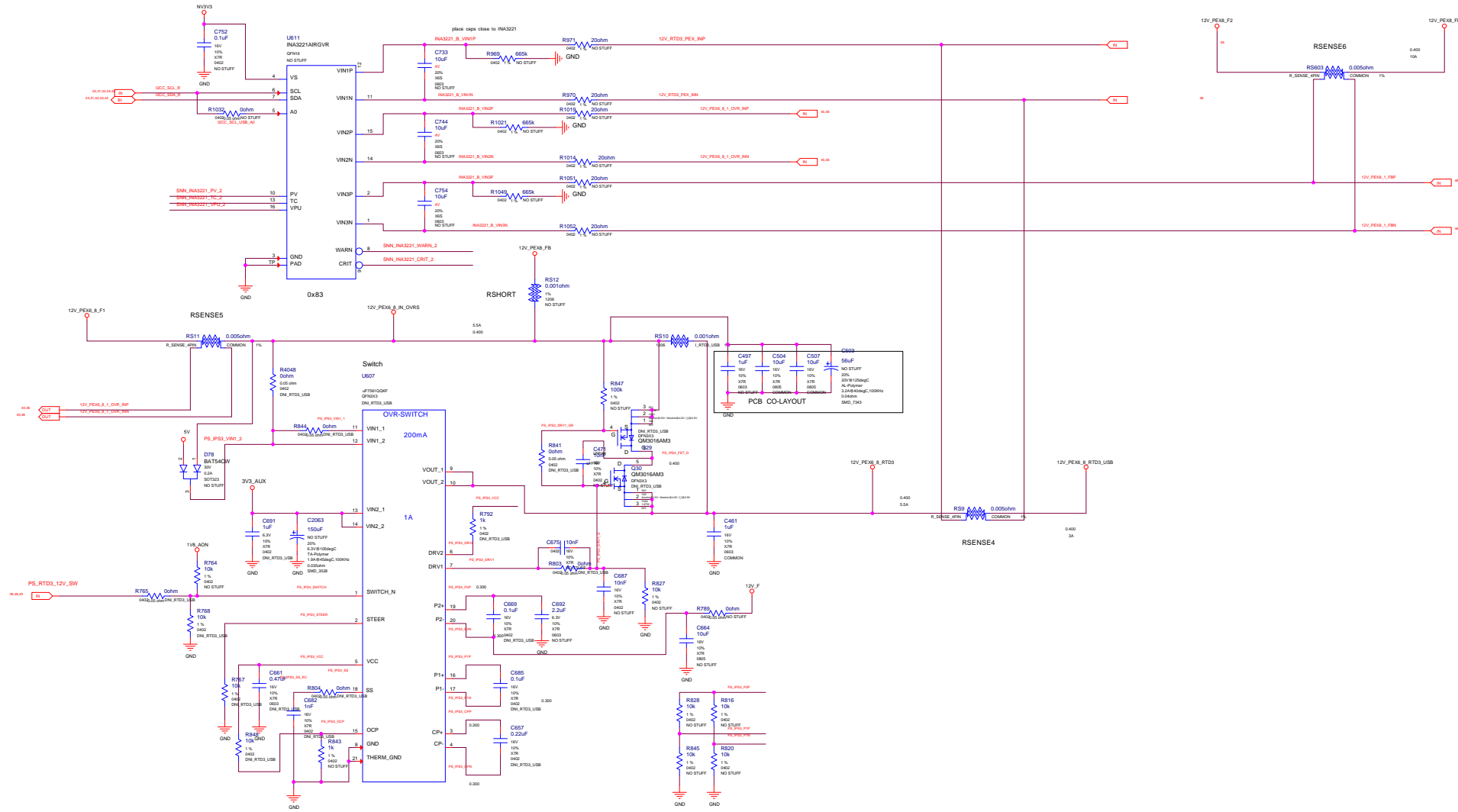
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	PS: INPUT SWITCH RTD3


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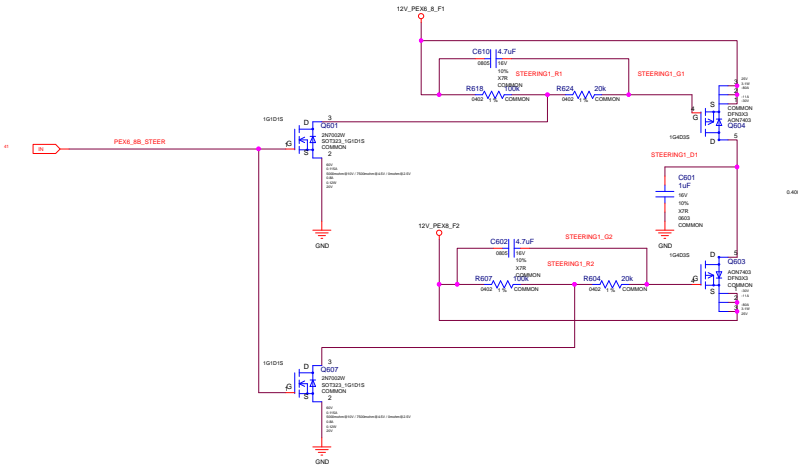
ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: INPUT SWITCH RTD3 USB



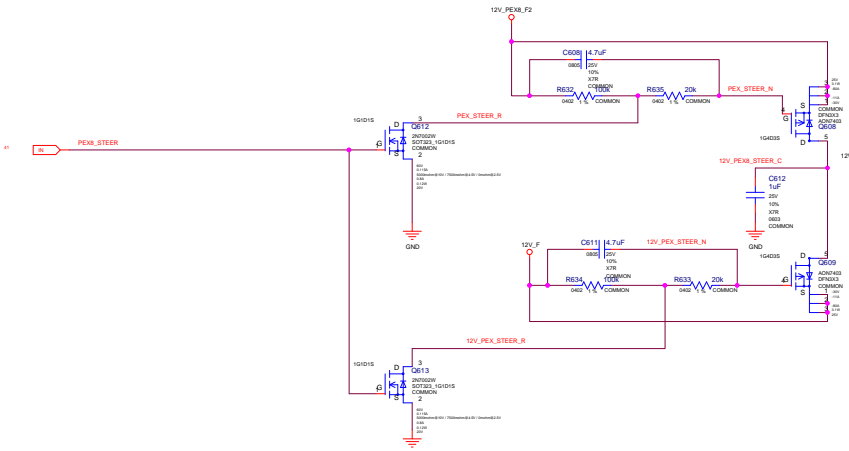
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12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA




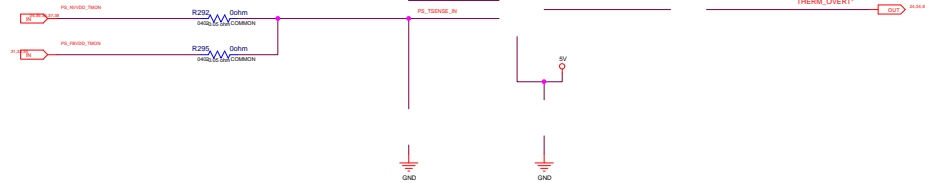
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



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PAGE DETAIL	PS: 12V CURRENT STEERING

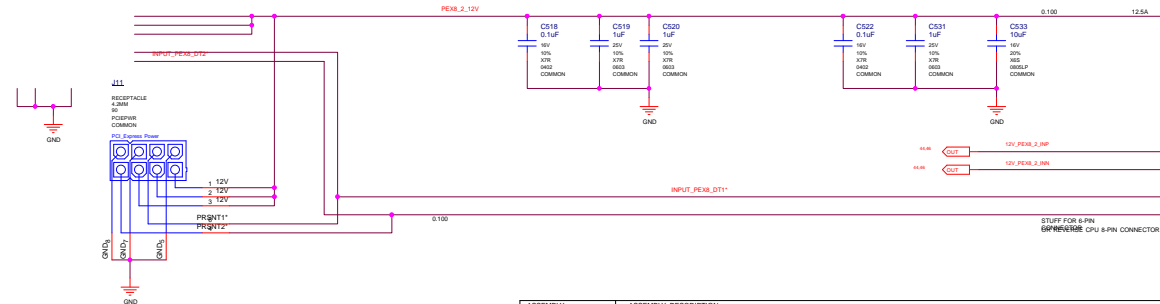
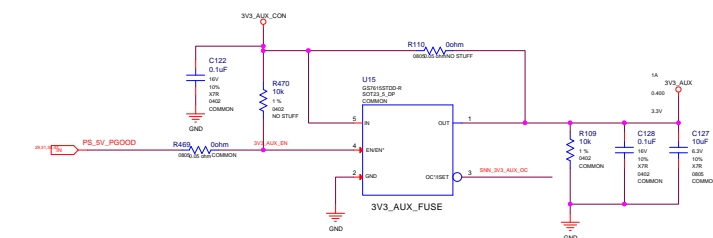
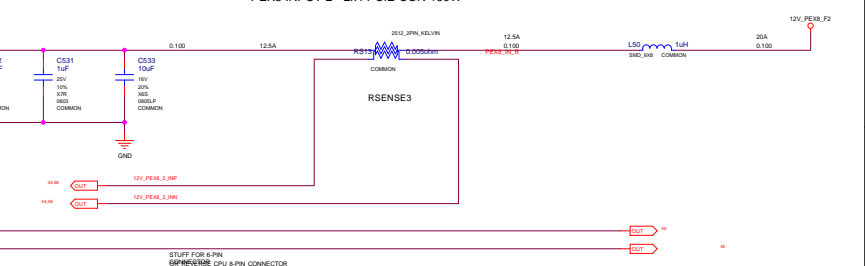
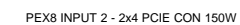
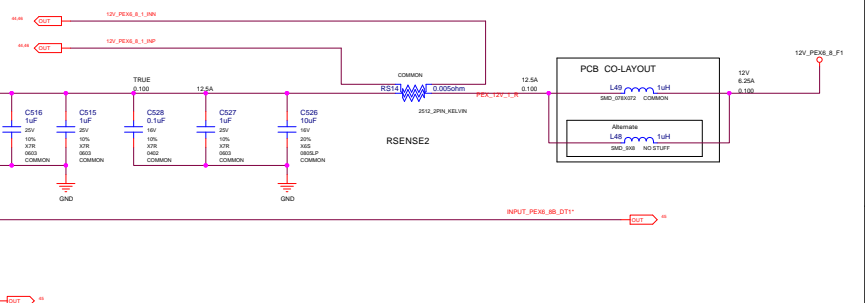
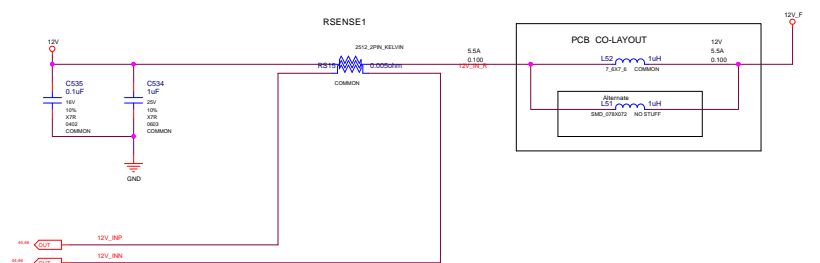
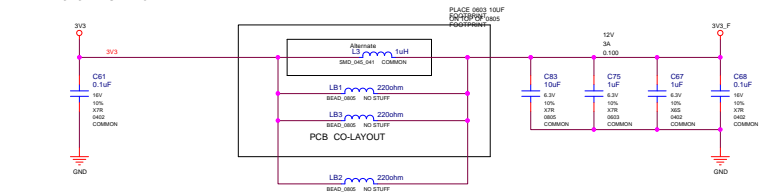
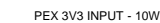
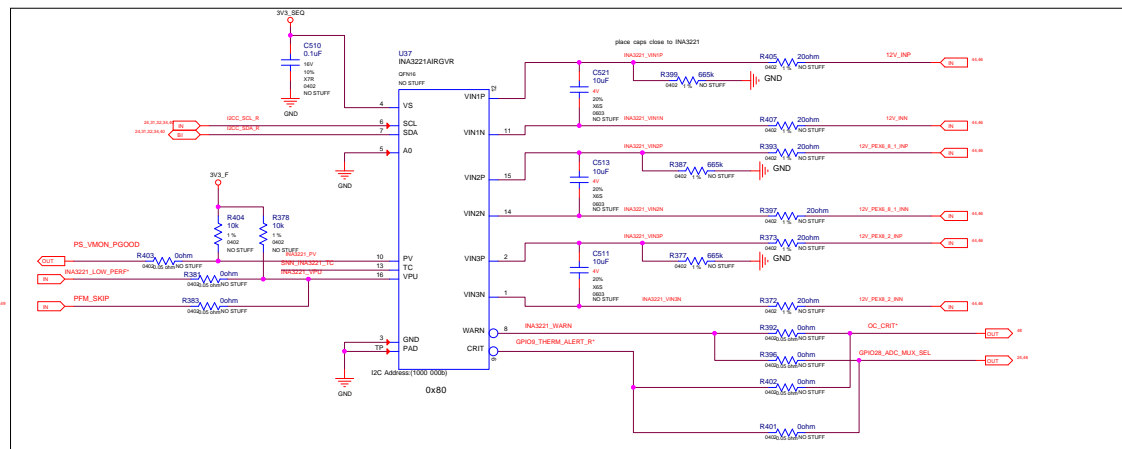
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ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	PS: VR THERMAL PROTECTION

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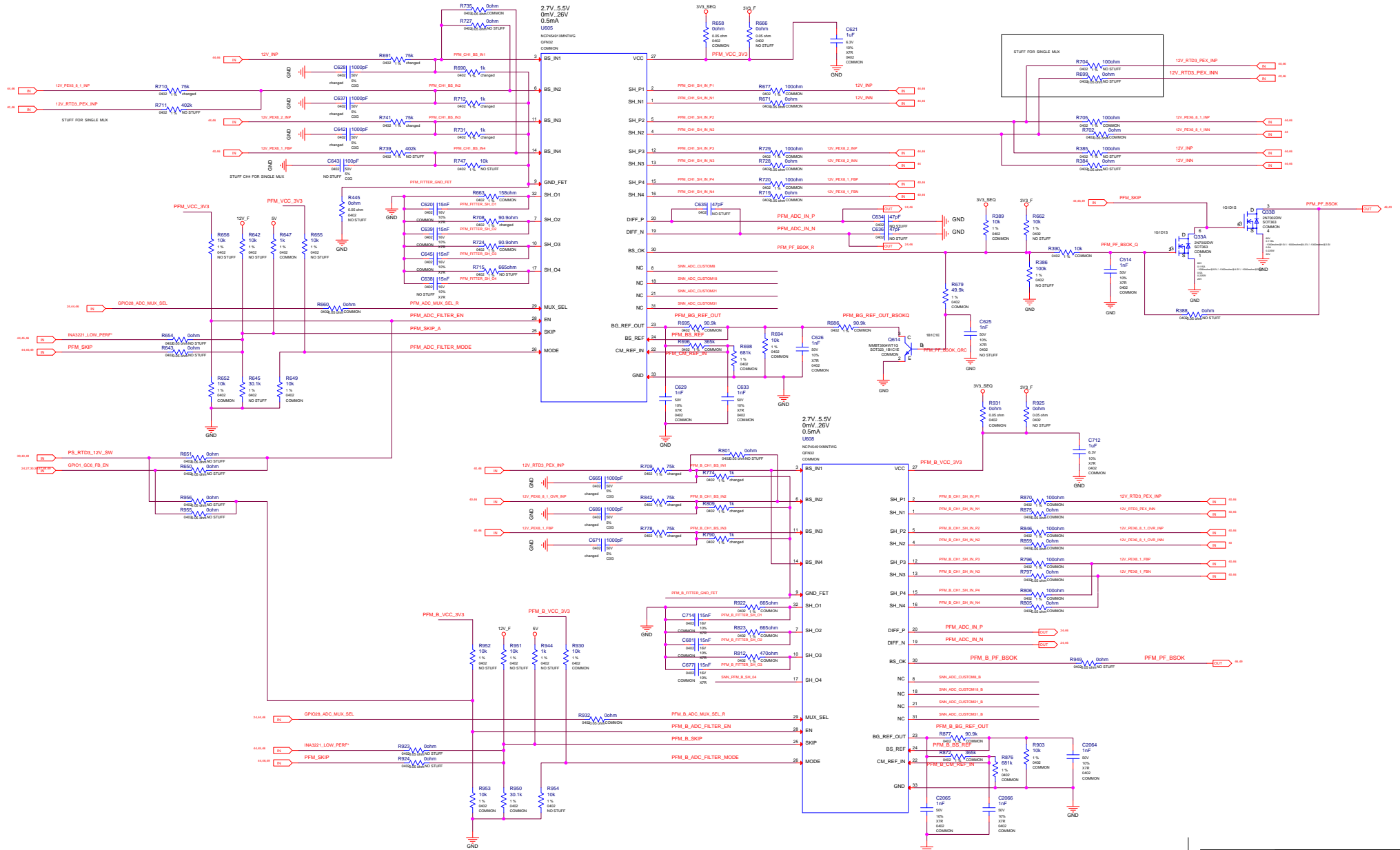
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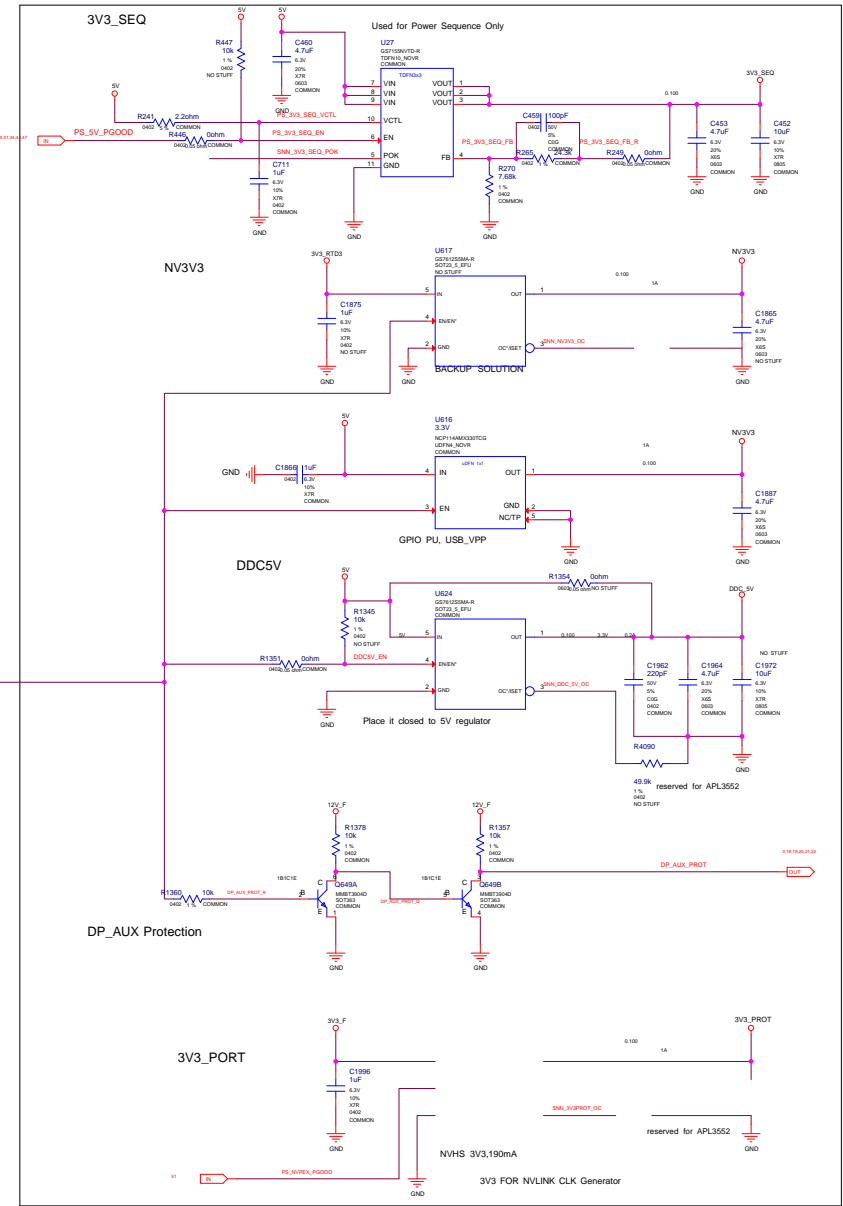
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PAGE DETAIL	PS: INPUTS, FILTERING AND MONITORING


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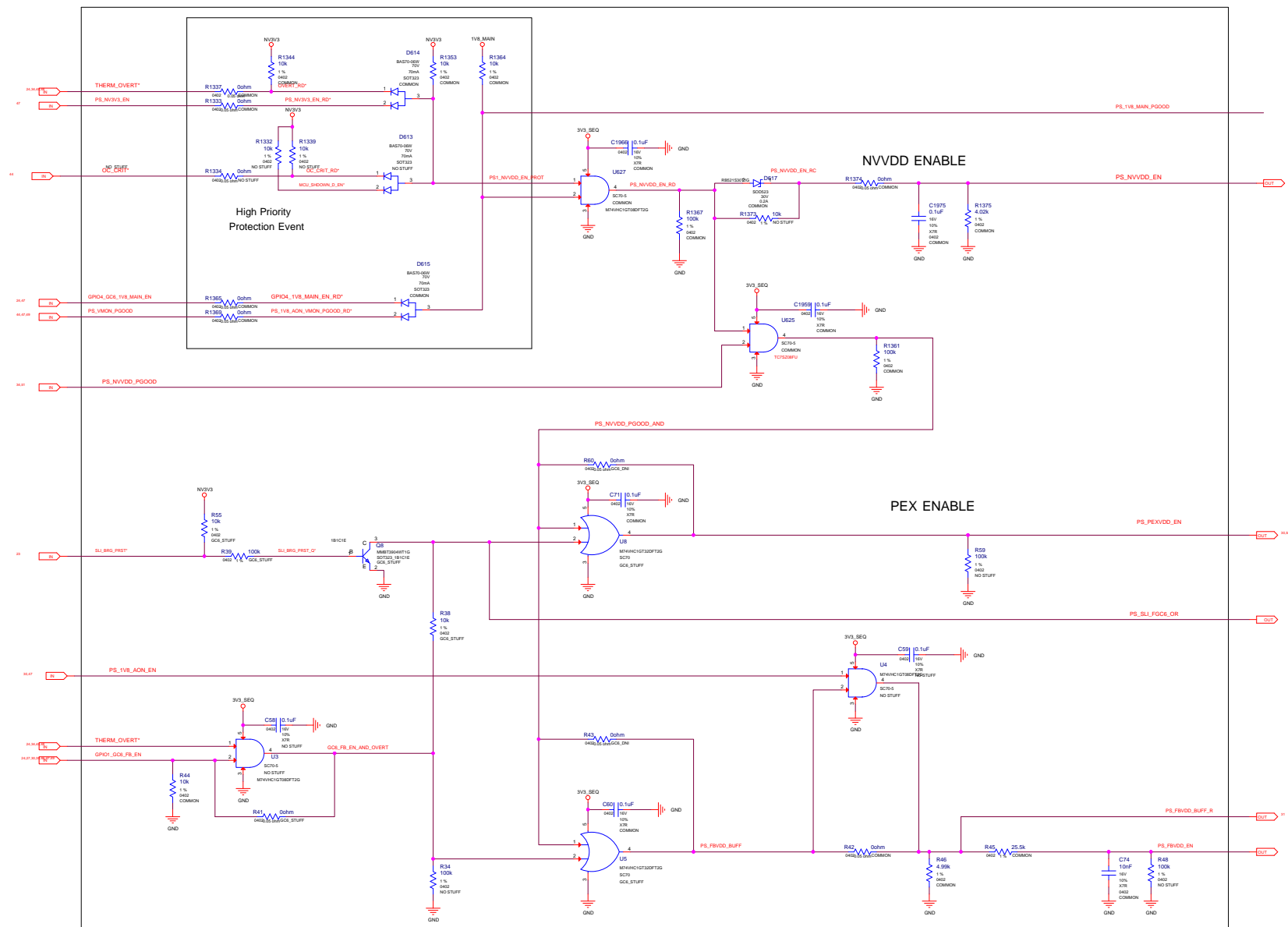
STUFF IF USING 2XMUX



ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: PRE-FILTER



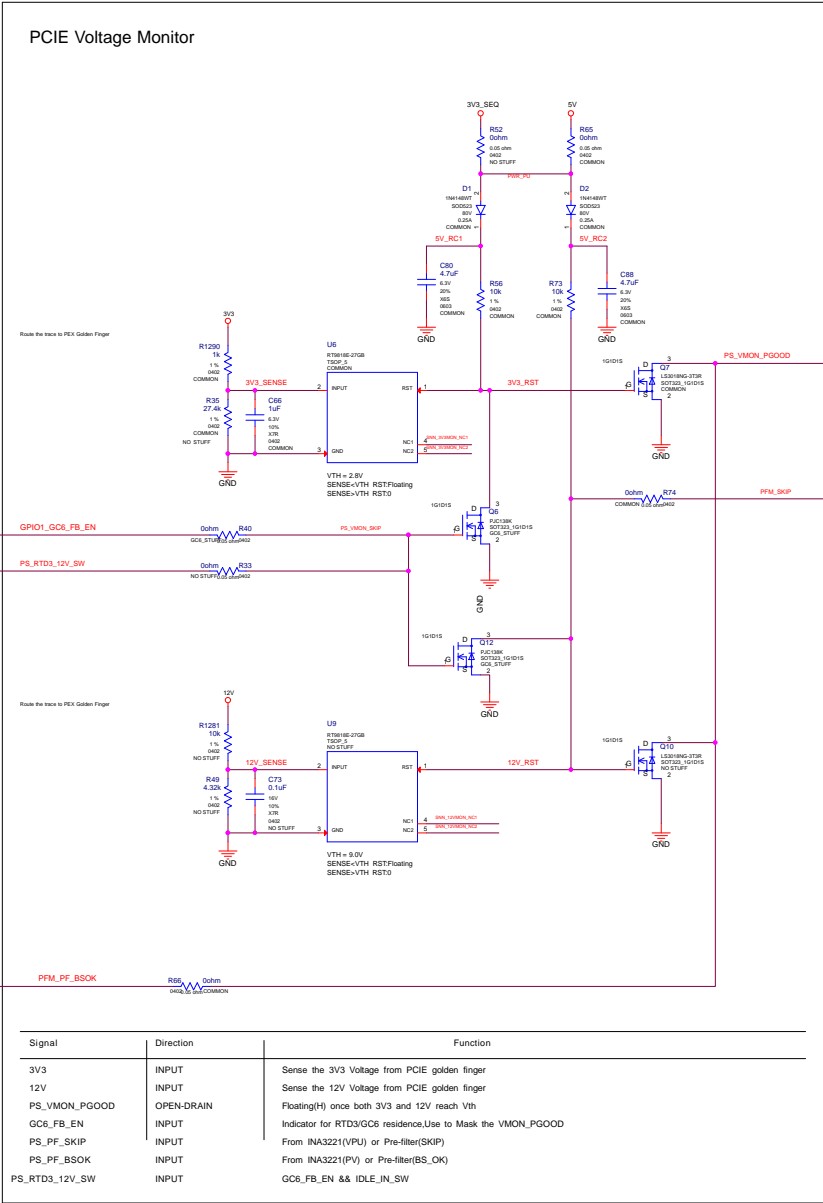
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ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	SEQUENCE: NV, PEX, FB ENABLE

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BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

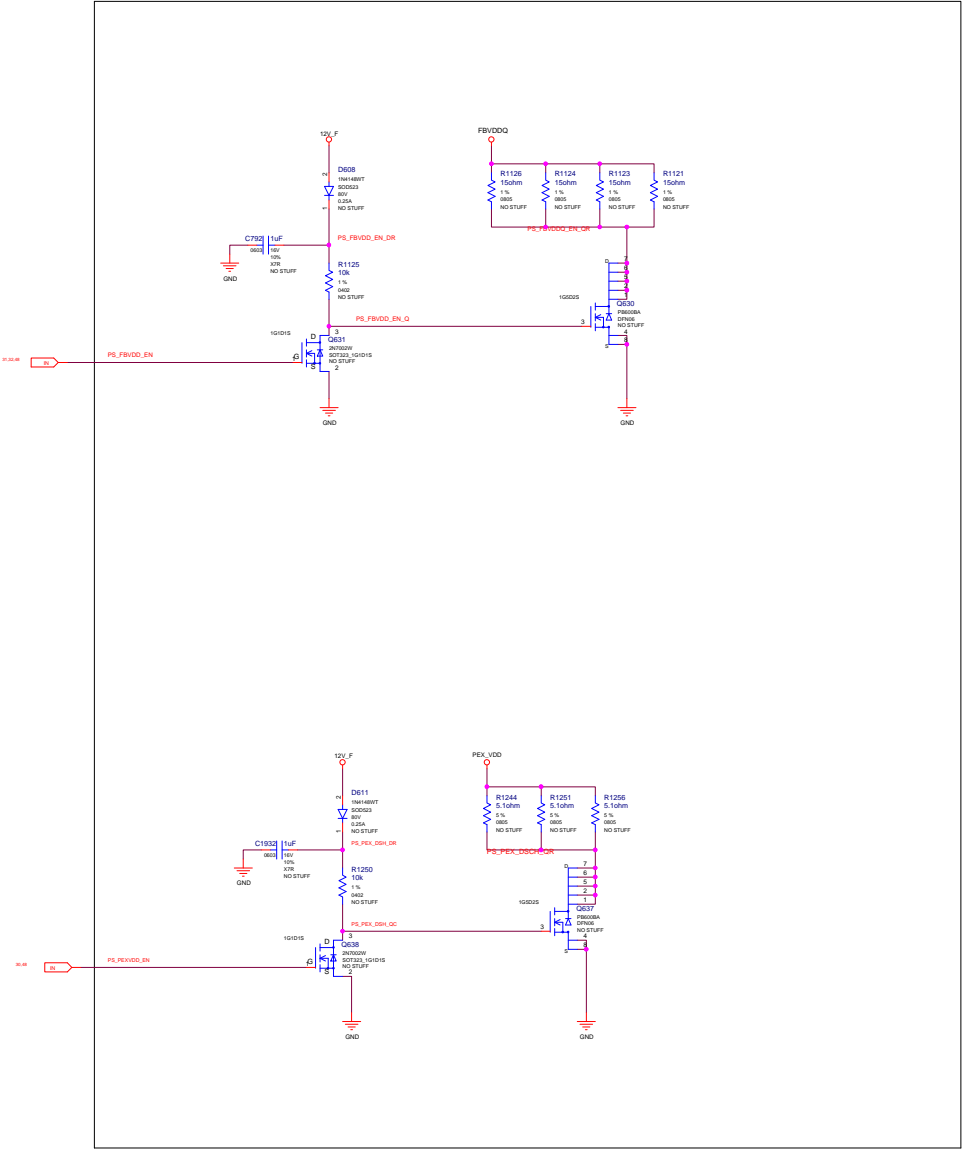
and All Input 12Vs

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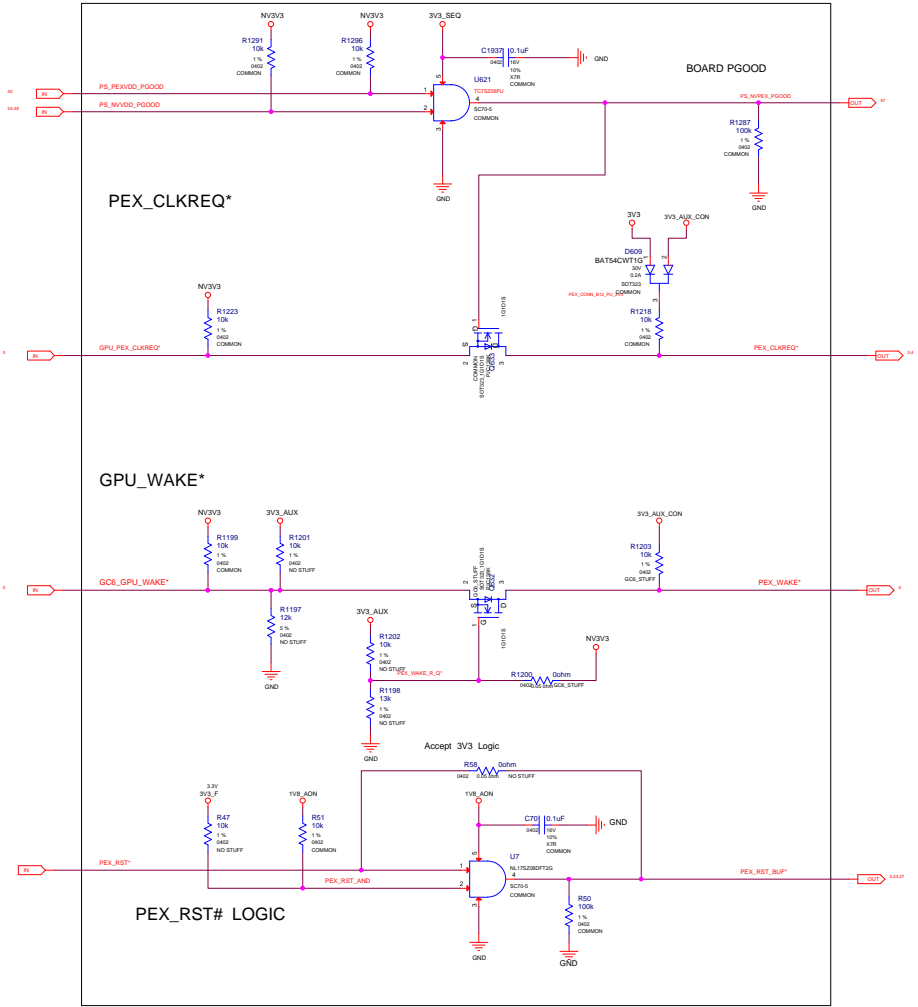


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ASSEMBLY PAGE DETAIL

SEQUENCE: DISCHARGE

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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	SEQUENCE: MISC

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$$\begin{aligned} V_{out} &= (1 + R_{top}/R_{bot}) * V_{ref} \\ &= (1 + 287K/10K) * 0.6V \\ &= 17.82V \end{aligned}$$

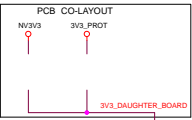
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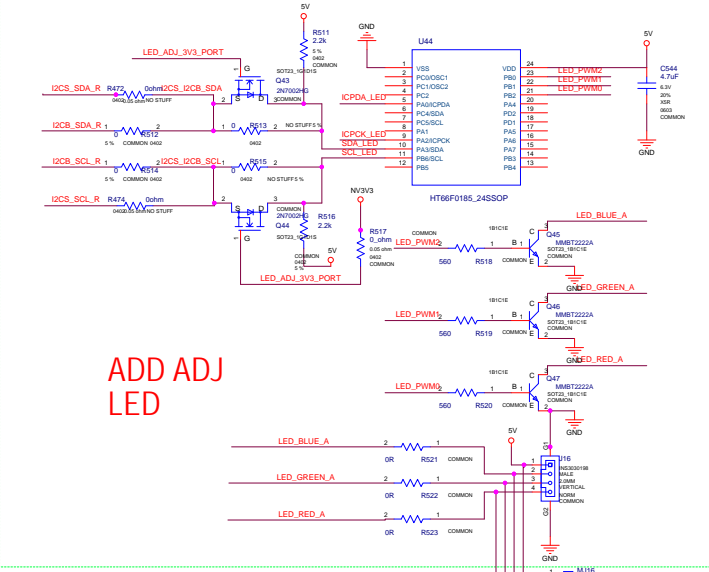
12V FROM FAN PAGE

FAN_LED_VDD

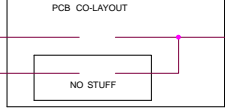
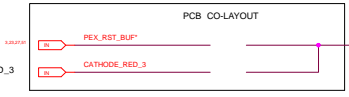
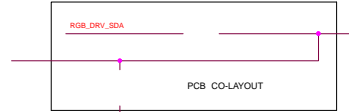
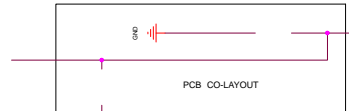
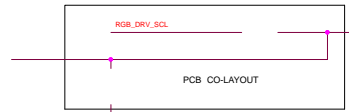
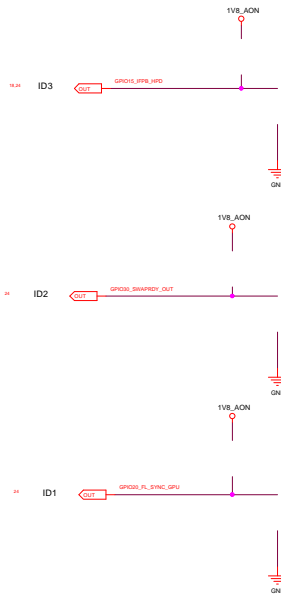
PLACE CAPS CLOSE TO CONNECTOR



8-bit I2C Address of MCU on Daughter Board: TBD

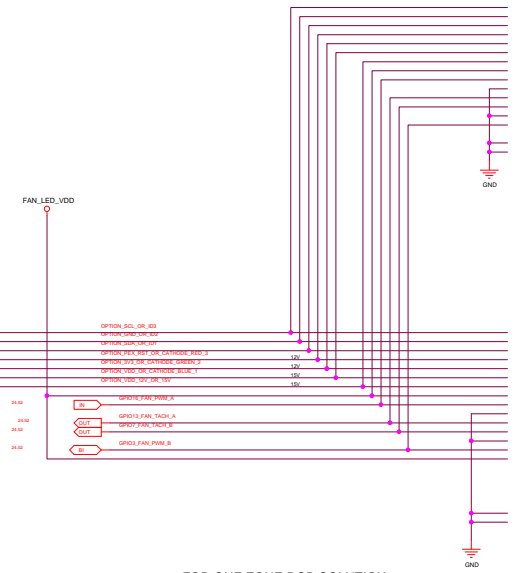


ADD ADJ LED



14-PIN STRAIGHT PRIMARY SOURCE -> 080-1586-000 ACES \$0.115
14-PIN STRAIGHT SECOND SOURCE -> 080-1600-000 WIESON \$0.2

FOR MCU SOLUTION



FOR ONE ZONE RGB SOLUTION

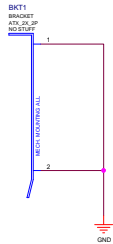
15-PIN STRAIGHT PRIMARY SOURCE -> 080-1617-000 ACES \$0.1165
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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	LED 2

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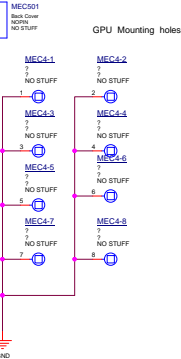
Brackets:



Bracket Screw



BOARD STIFFENER



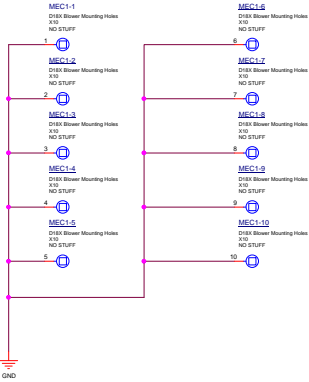
GPU Mounting holes

STIFFENER

GPU Socket Symbol




Mechanical Holes Symbol



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	Mechanical: Bracket/Thermal Solution

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