P684-A01 GT216 DESKTOP Low Profile
PCI-EXPRESSx16 DL-DVI HDMI VGA DDR3

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5.0

Page 21: PWM Change to UP6205 ; Add UP6262 Circuit

Page 20: Removed GPIO7_FBVDD_MODE Circuit
Removed GPIO13

Page 19: Removed 3V3 change to 1.8V IFP_PLLVDD SUPPLY

Page 18: Removed INFO ROM, HDCP ROM

Page 17: Removed 2Pin FAN CONTROL
Removed JTAG

5.1

Page 20: Changed L10 Footprint,removed Q5,Q15 co-layout Powerpak MOS
Page 12: Changed J1 Footprint

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REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10684-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P684-A01 OVERVIEW

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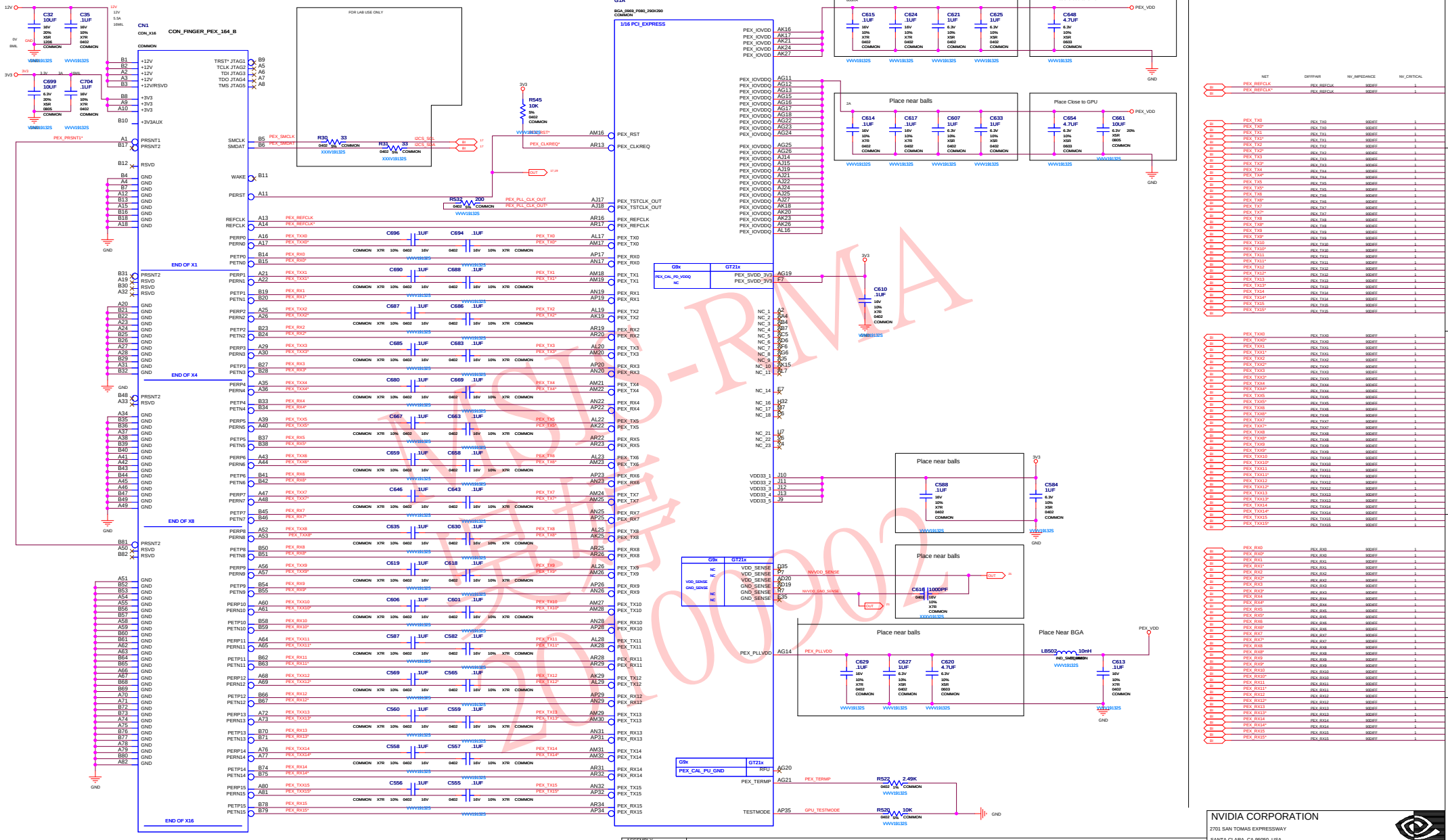
PCI-EXPRESS INTERFACE



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ASSEMBLY	
PAGE DETAIL	PCI-EXPRESS INTERFACE

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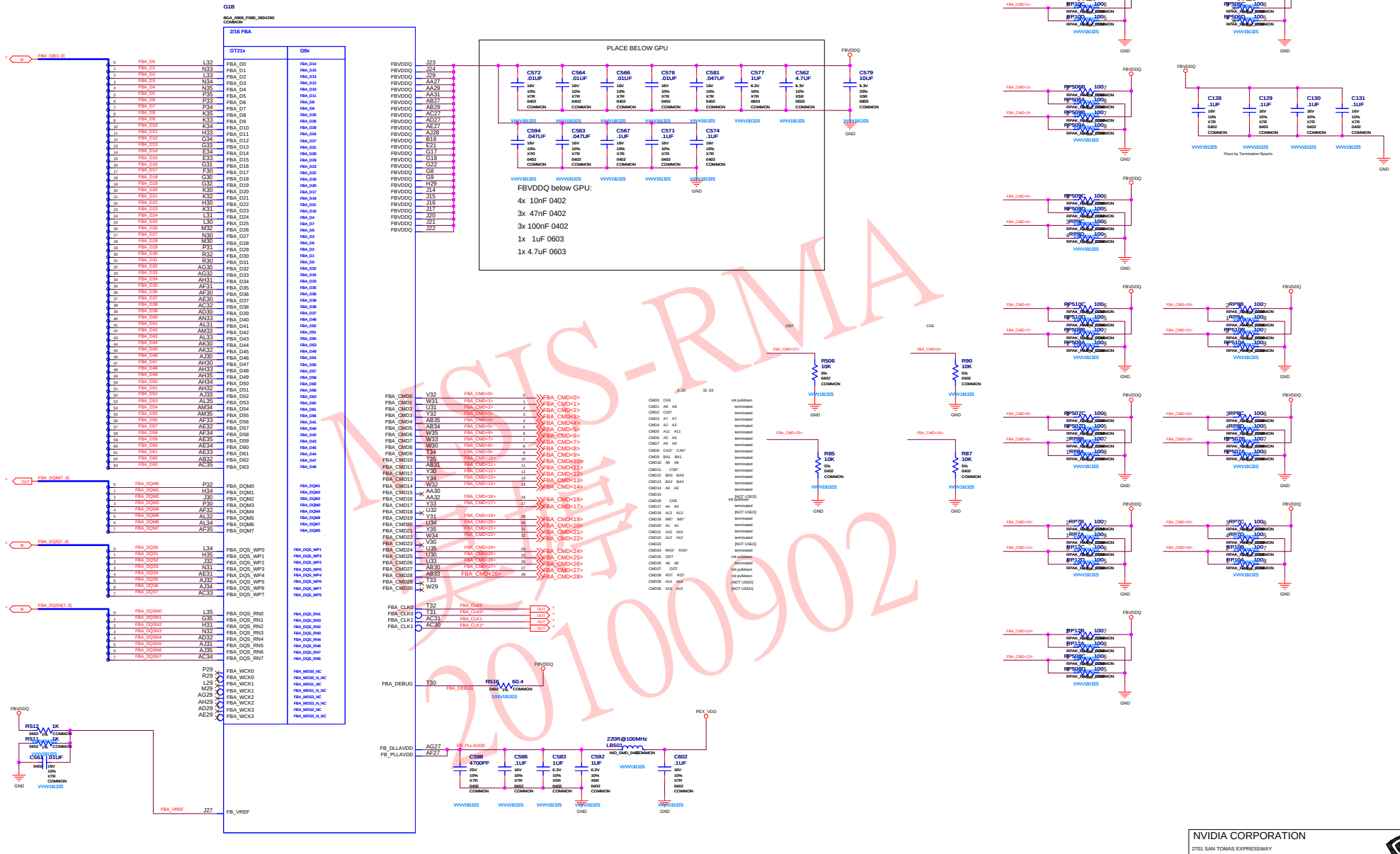
PARTITION A FRAME BUFFER INTERFACE



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ASSEMBLY	
PAGE DETAIL	PARTITION A FRAME BUFFER INTERFACE

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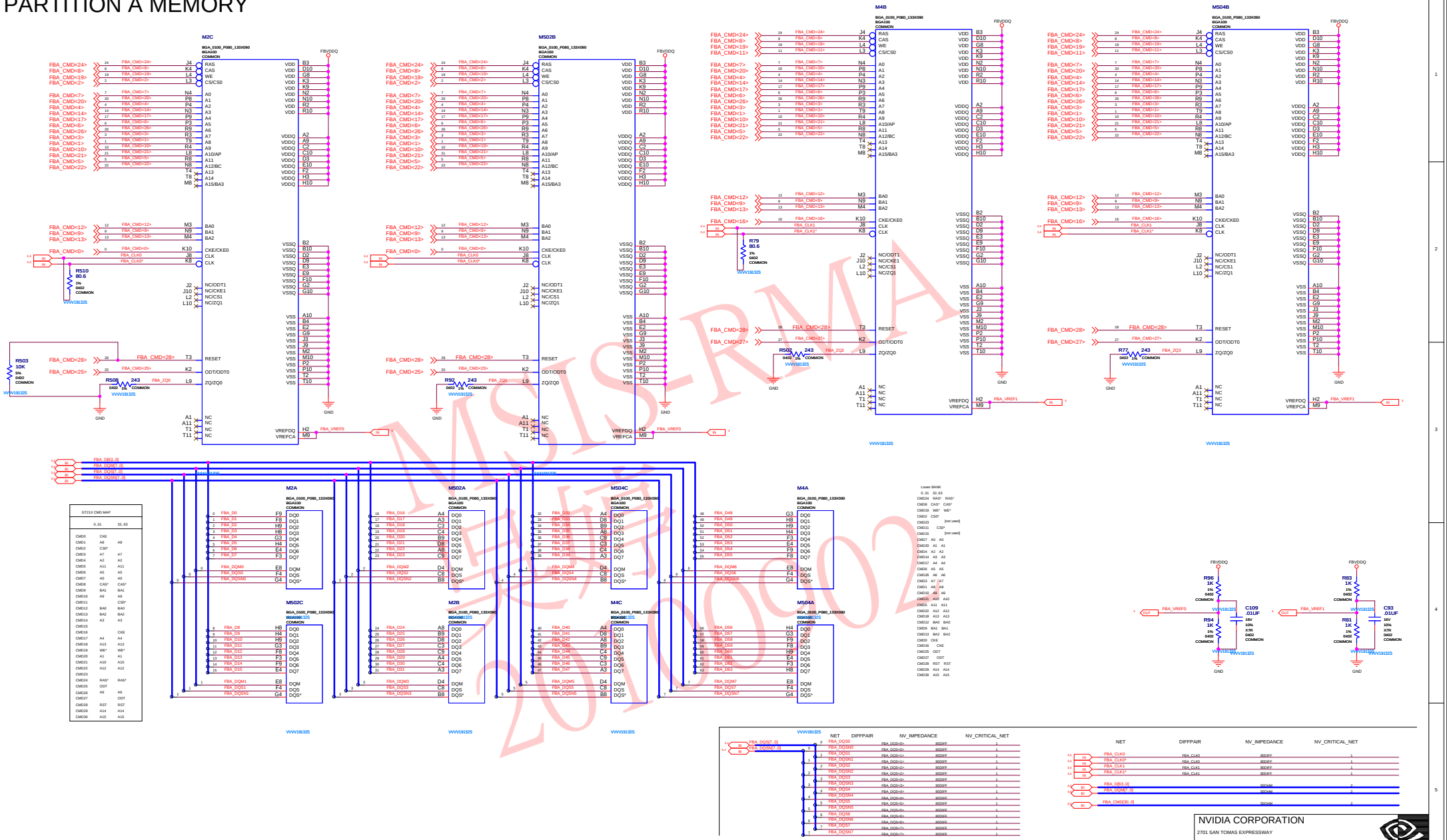
PARTITION A MEMORY



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PAGE DETAIL	PARTITION A MEMORIES

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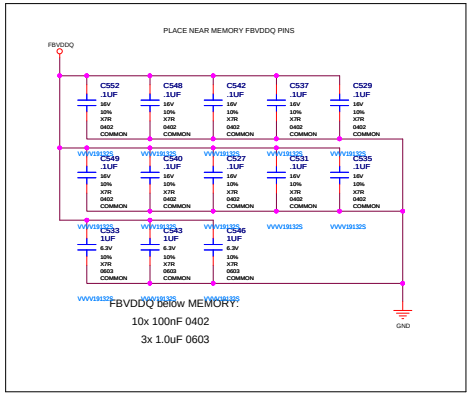
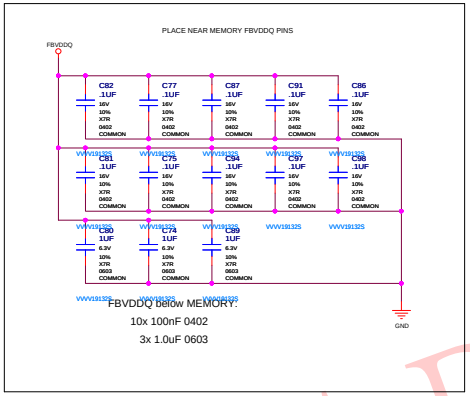
NAME		DATE	13-FEB-2009

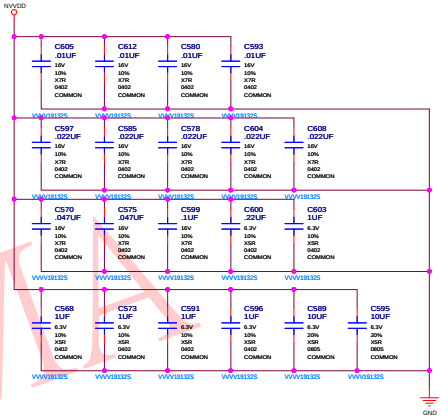
FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS

Decoupling for FBA 0..15



Decoupling for FBA 16..31





NVVDD under GPU:

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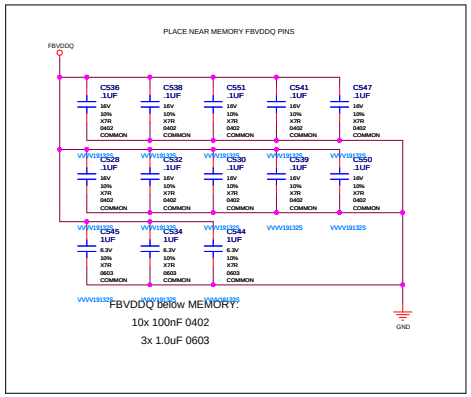
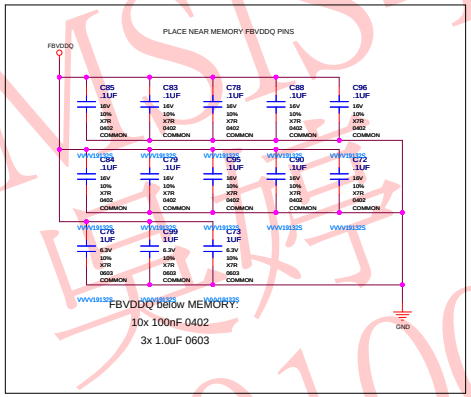
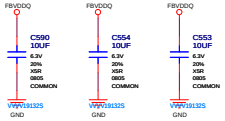
5x 0.022uF 0402 X7R
2x 0.047uF 0402 X7R
1x 0.1uF 0402 X7R
1x 0.22uF 0402 X7R
4x 1.0uF 0402 X5R
2x 2.2uF 0402 X5R
2x 10uF 0805 X5R

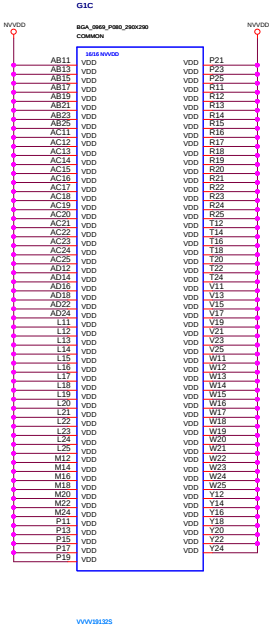
Decoupling for FBA 32..47



Decoupling for FBA 48..63







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PAGE DETAIL	FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS

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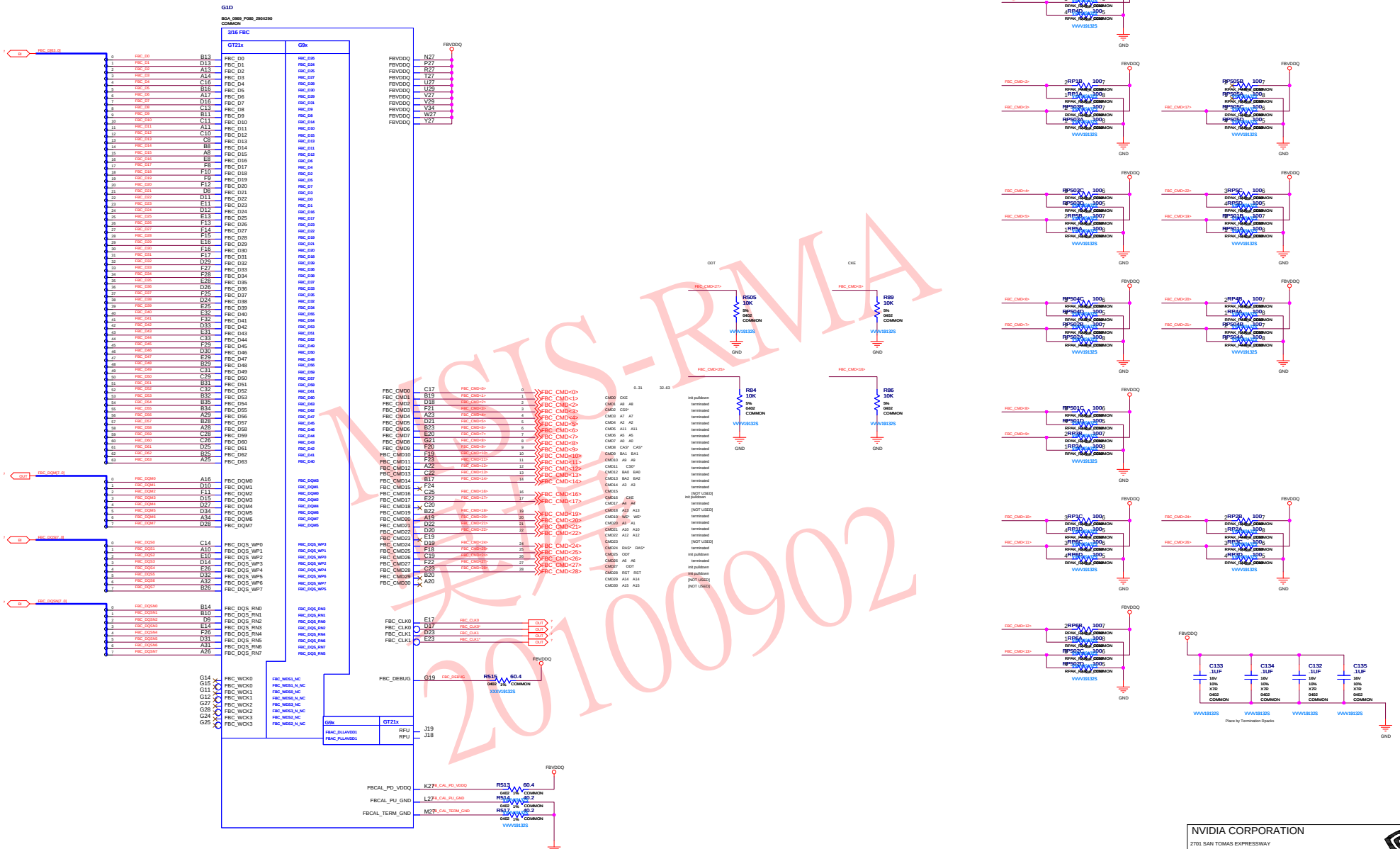
PARTITION C FRAME BUFFER INTERFACE



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PARTITION C FRAME BUFFER INTERFACE

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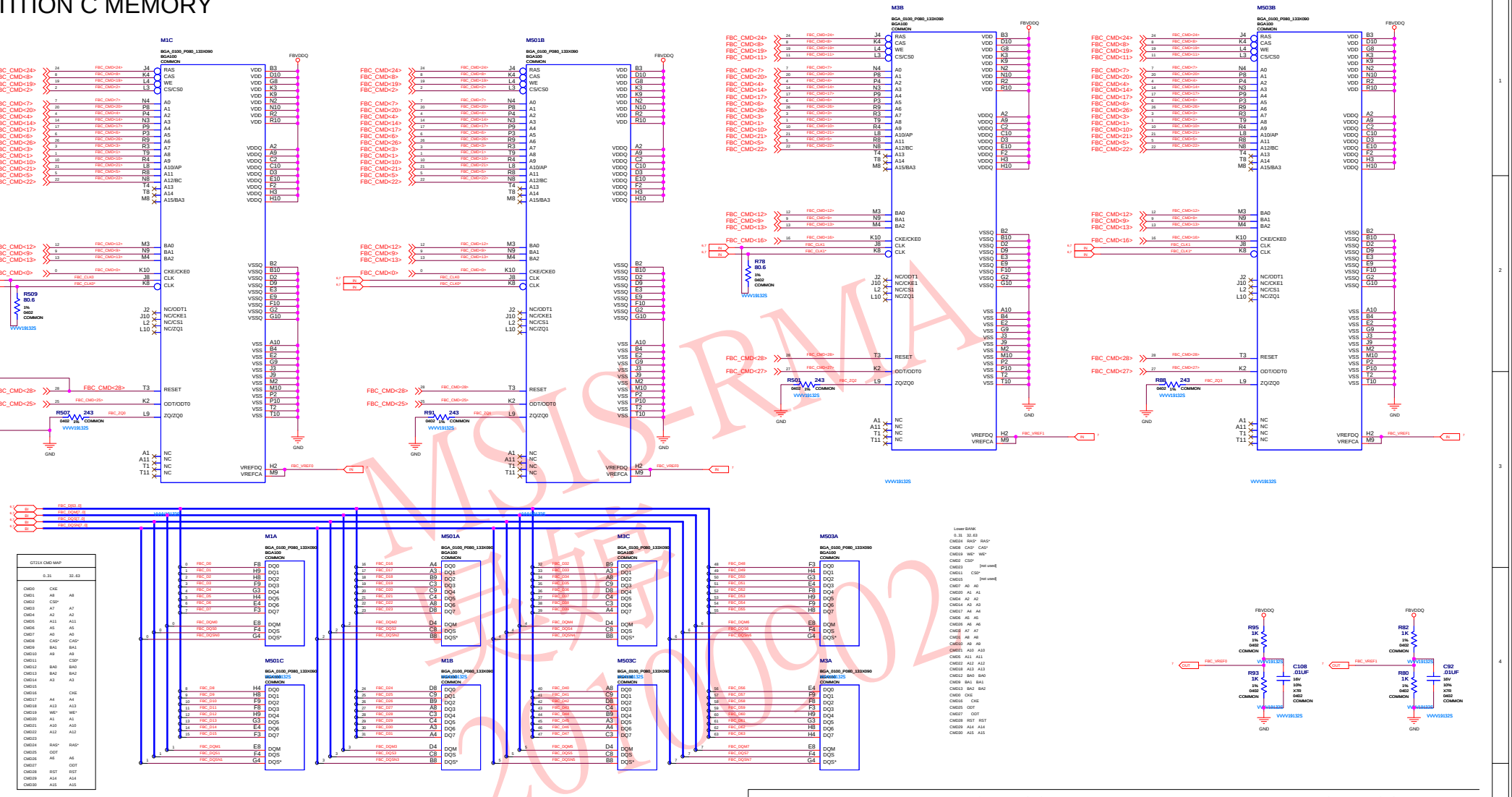
PARTITION C MEMORY



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FBC_DBI0_0		SIGNAL	2
FBC_DQM0_0		SIGNAL	2
FBC_CMD30_0		SIGNAL	2

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PARTITION C MEMORIES

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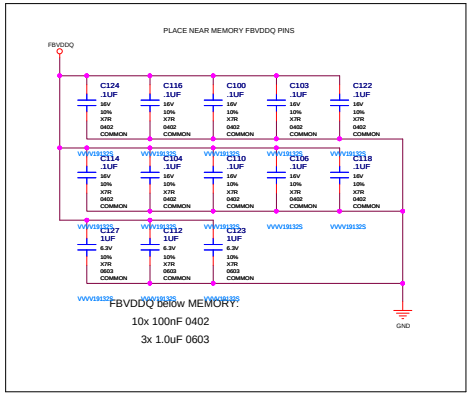
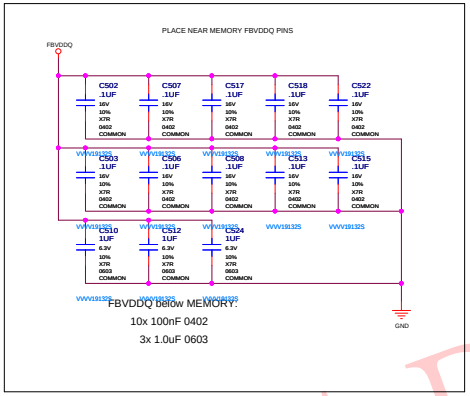
FBC DECOUPLING CAPS & NVVDD DECOUPLING CAPS

Decoupling for FBC 0..15



Decoupling for FBC 16..31



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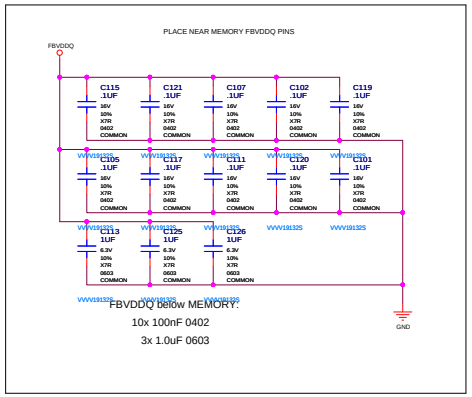
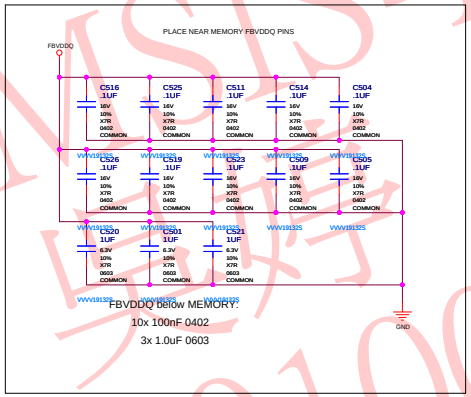
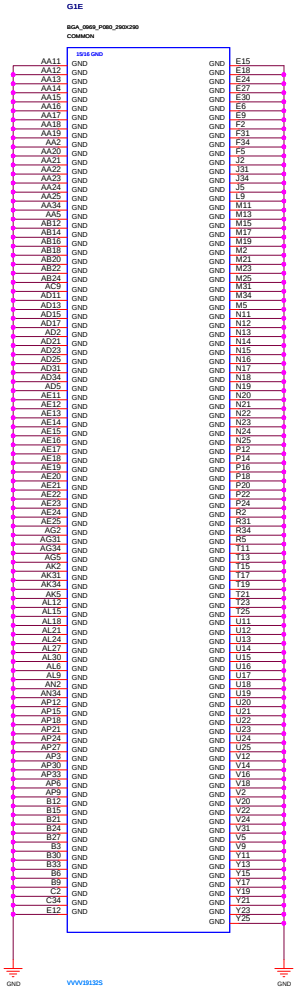


Decoupling for FBC 48..63





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PAGE DETAIL	FBC DECOUPLING CAPS

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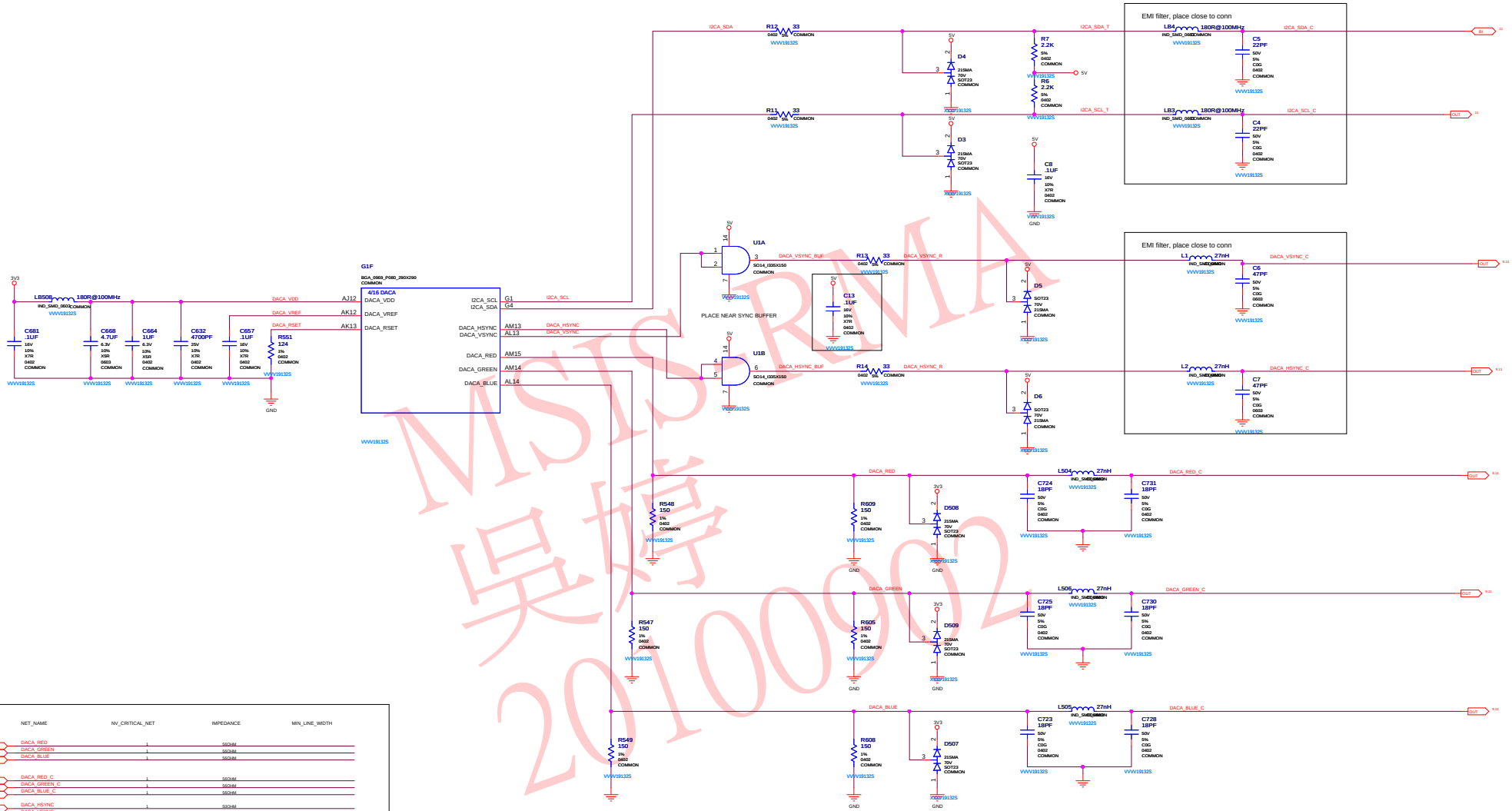
DACA (SOUTH DVI-I)



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DACA_BLUE	1	50OHM	
DACA_RED_C	1	50OHM	
DACA_GREEN_C	1	50OHM	
DACA_BLUE_C	1	50OHM	
DACA_HSYNC	1	50OHM	
DACA_VSYNC	1	50OHM	
DACA_HSYNC_R	1	50OHM	
DACA_VSYNC_R	1	50OHM	
DACA_VSYNC_BUF	1	50OHM	
DACA_HSYNC_BUF	1	50OHM	
DACA_VSYNC_C	1	50OHM	
DACA_HSYNC_C	1	50OHM	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA (SOUTH DVI-I)

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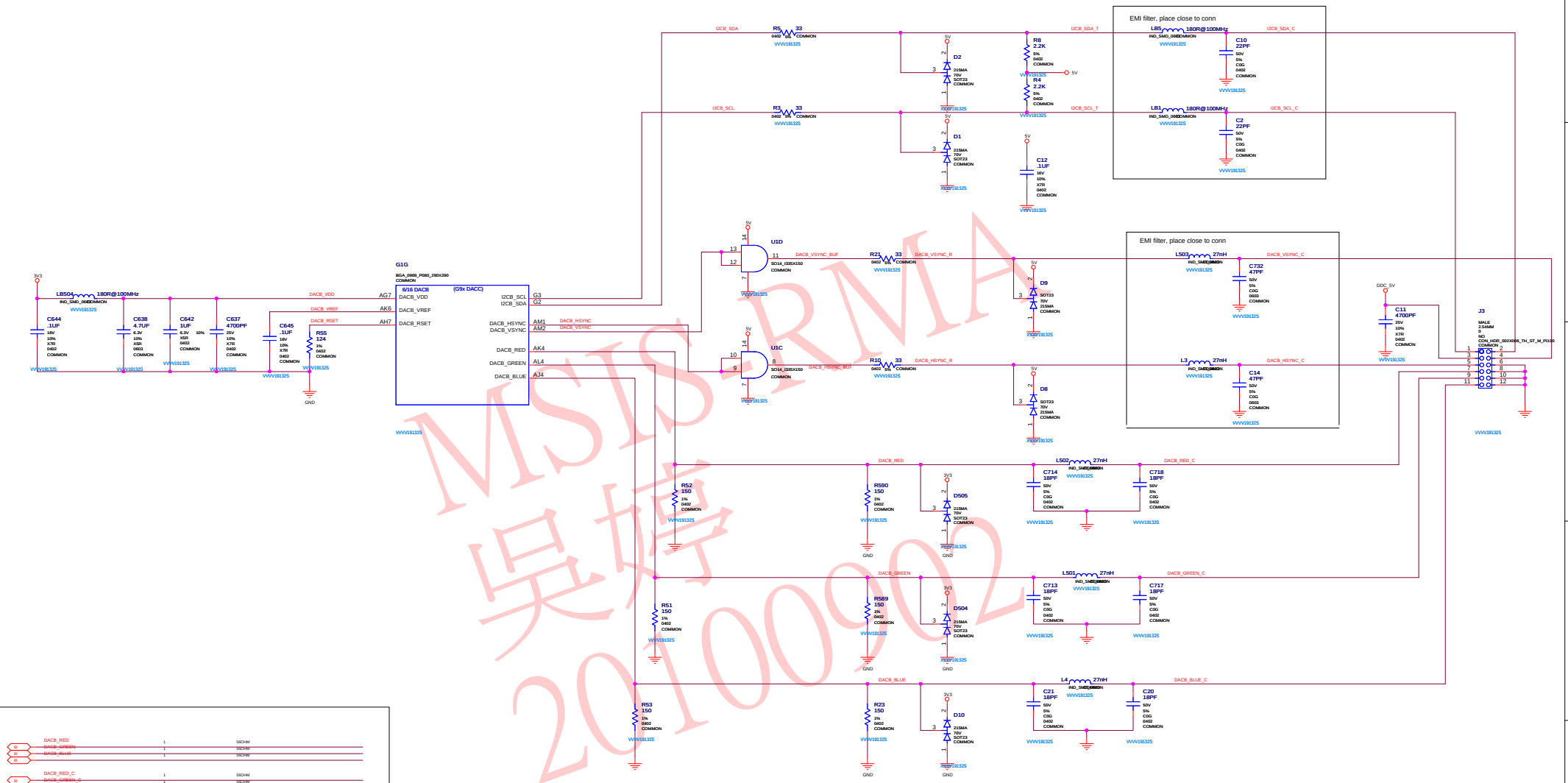
DACB (cable-up VGA)



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PAGE DETAIL	DACB (MID DVI-I)

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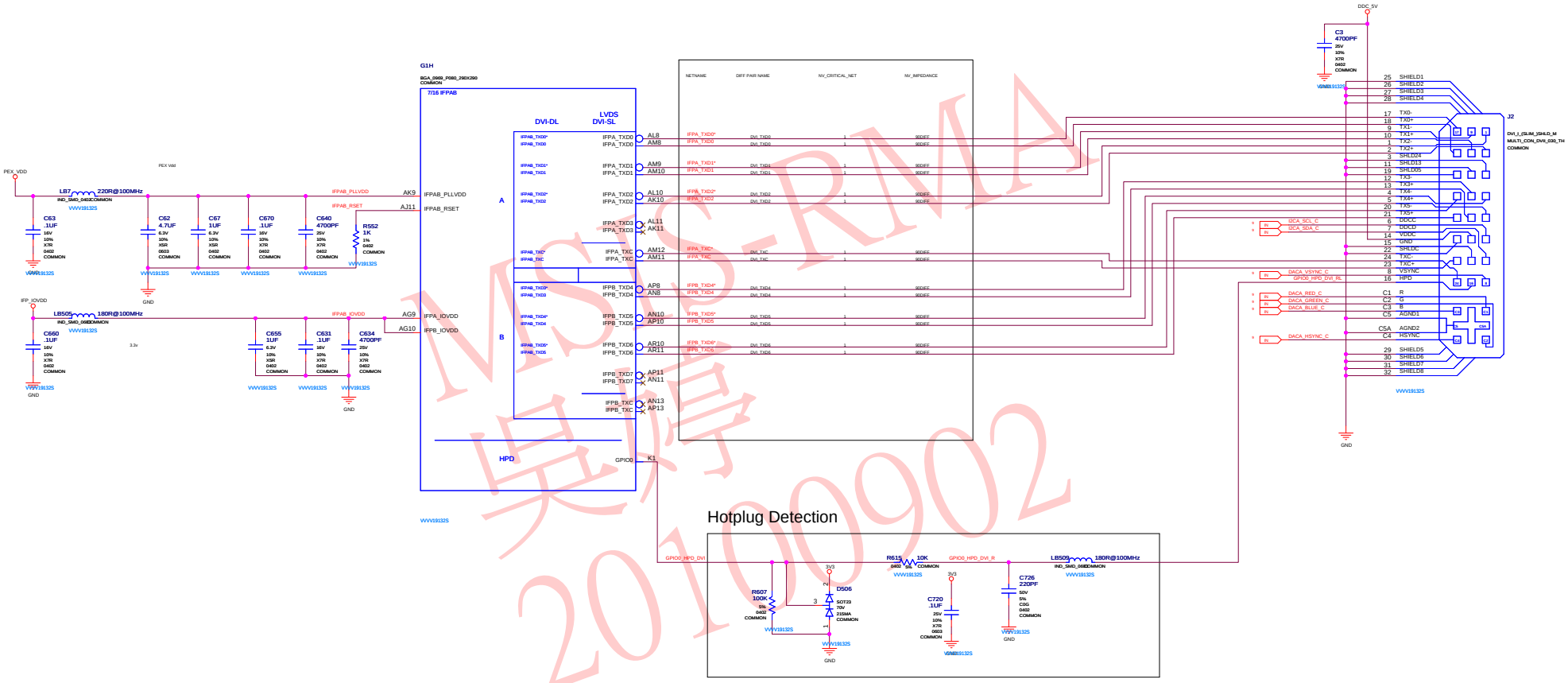

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PAGE DETAIL	IFP AB (SOUTH DVI-I)

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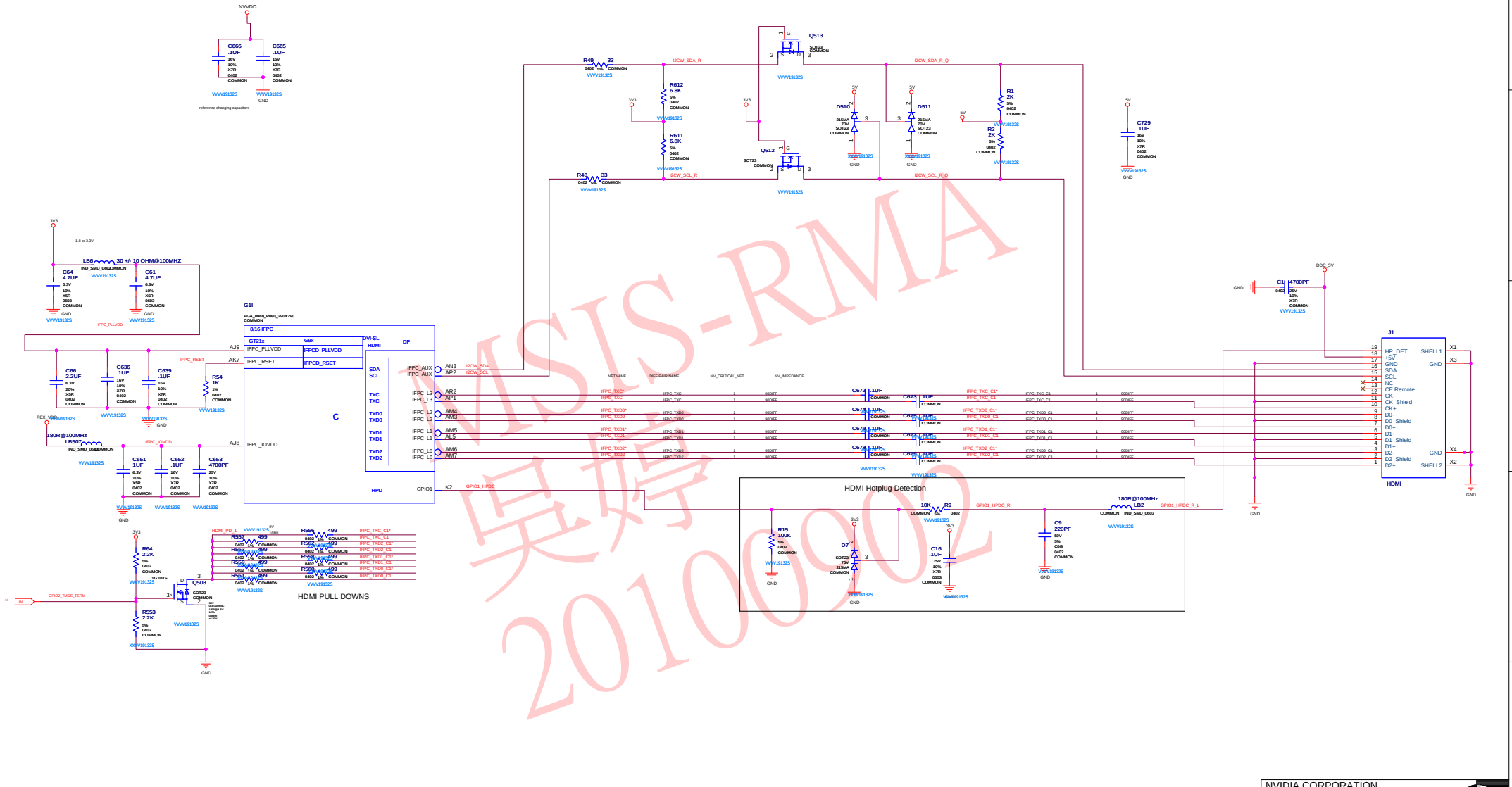
IFP C (NORTH HDMI)



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PAGE DETAIL | IFP C (NORTH nHDMI)

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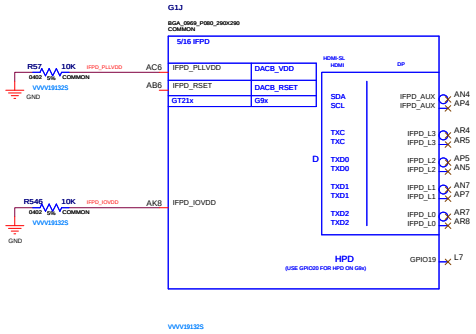
IFP D (UNUSED)



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NET	PAIR	NV_CRITICAL	IMPEDANCE
IFPE_AUX_BYP	IFPE_AUX_BYP	1	90DIFF
IFPE_AUX_BYP*	IFPE_AUX_BYP	1	90DIFF

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PAGE DETAIL	IFP D (UNUSED) & MID DISPLAYPORT

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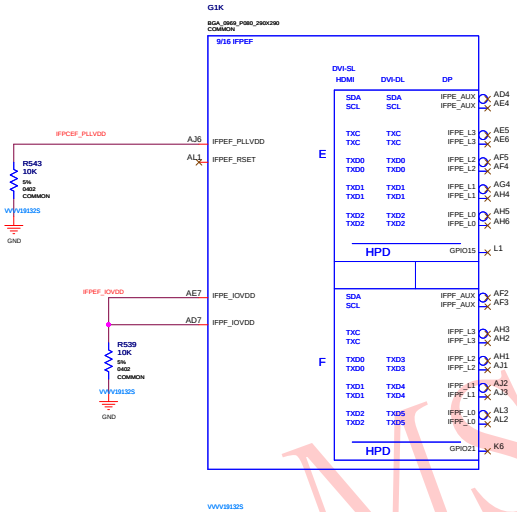
IFP EF (unused)



NET	PAIR	NV_CRITICAL	IMPEDANCE
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IFPE_TXC* / IFPE_TXC	IFPE_TXC	1	90DIFF
IFPE_TXD0* / IFPE_TXD0	IFPE_TXD0	1	90DIFF
IFPE_TXD1* / IFPE_TXD1	IFPE_TXD1	1	90DIFF
IFPE_TXD2* / IFPE_TXD2	IFPE_TXD2	1	90DIFF
IFPF_TXD3* / IFPF_TXD3	IFPF_TXD3	1	90DIFF
IFPF_TXD4* / IFPF_TXD4	IFPF_TXD4	1	90DIFF
IFPF_TXD5* / IFPF_TXD5	IFPF_TXD5	1	90DIFF
IFPEF_TXD3* / IFPEF_TXD3	IFPEF_TXD3	1	90DIFF
IFPEF_TXD4* / IFPEF_TXD4	IFPEF_TXD4	1	90DIFF
IFPEF_TXD5* / IFPEF_TXD5	IFPEF_TXD5	1	90DIFF
IFPEF_TXD0* / IFPEF_TXD0	IFPEF_TXD0	1	90DIFF
IFPEF_TXD1* / IFPEF_TXD1	IFPEF_TXD1	1	90DIFF
IFPEF_TXD2* / IFPEF_TXD2	IFPEF_TXD2	1	90DIFF
IFPE_AUX* / IFPE_AUX	IFPE_AUX	1	90DIFF

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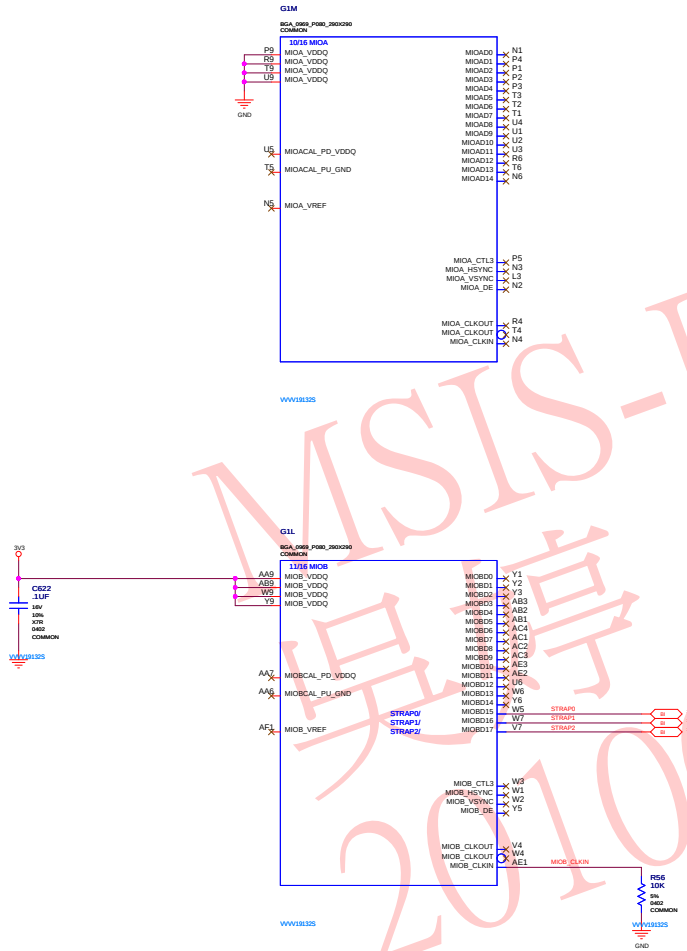
MIOA & MIOB



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PAGE DETAIL	MIOA & MIOB

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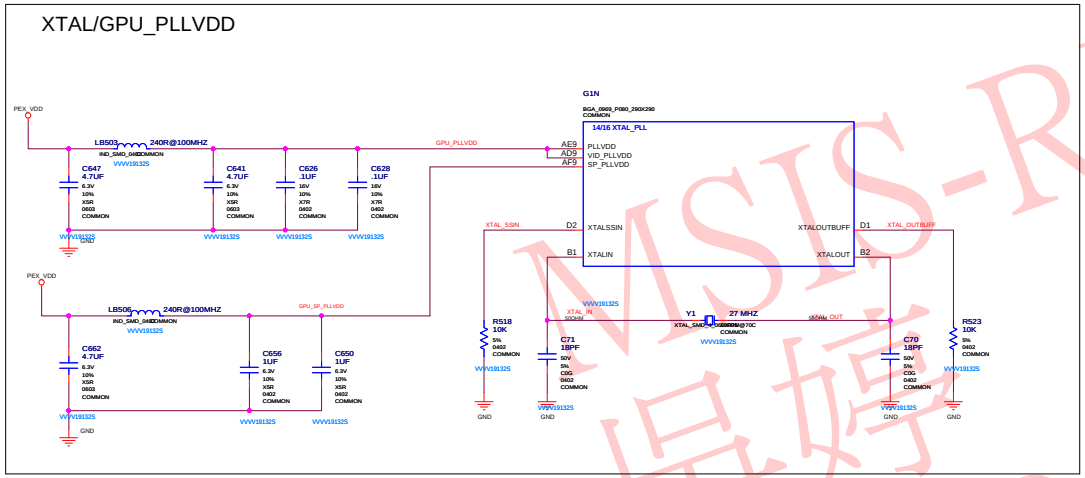
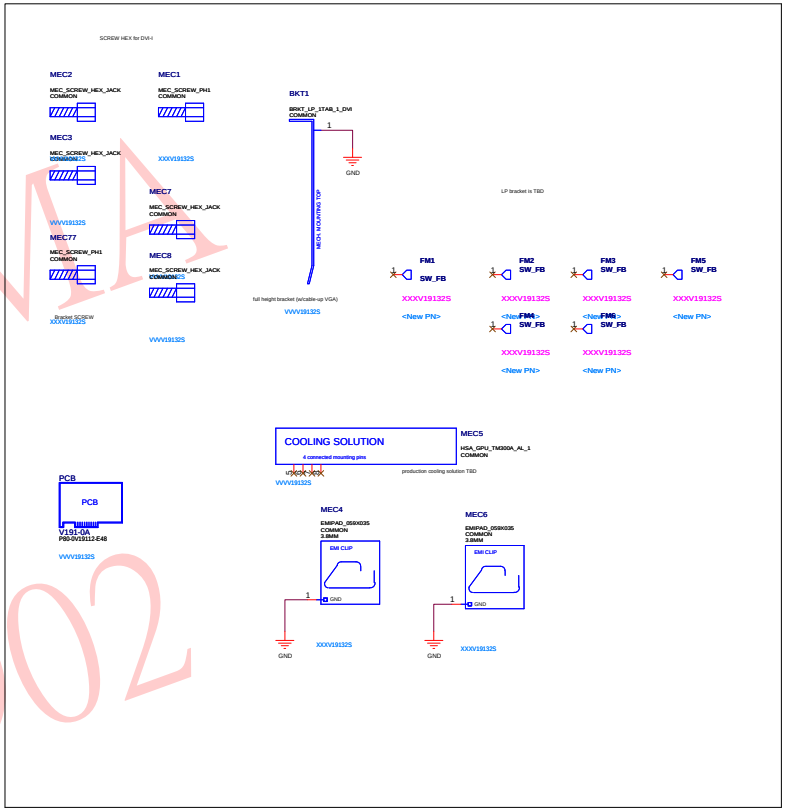
XTAL, MECHANICALS, THERMALS





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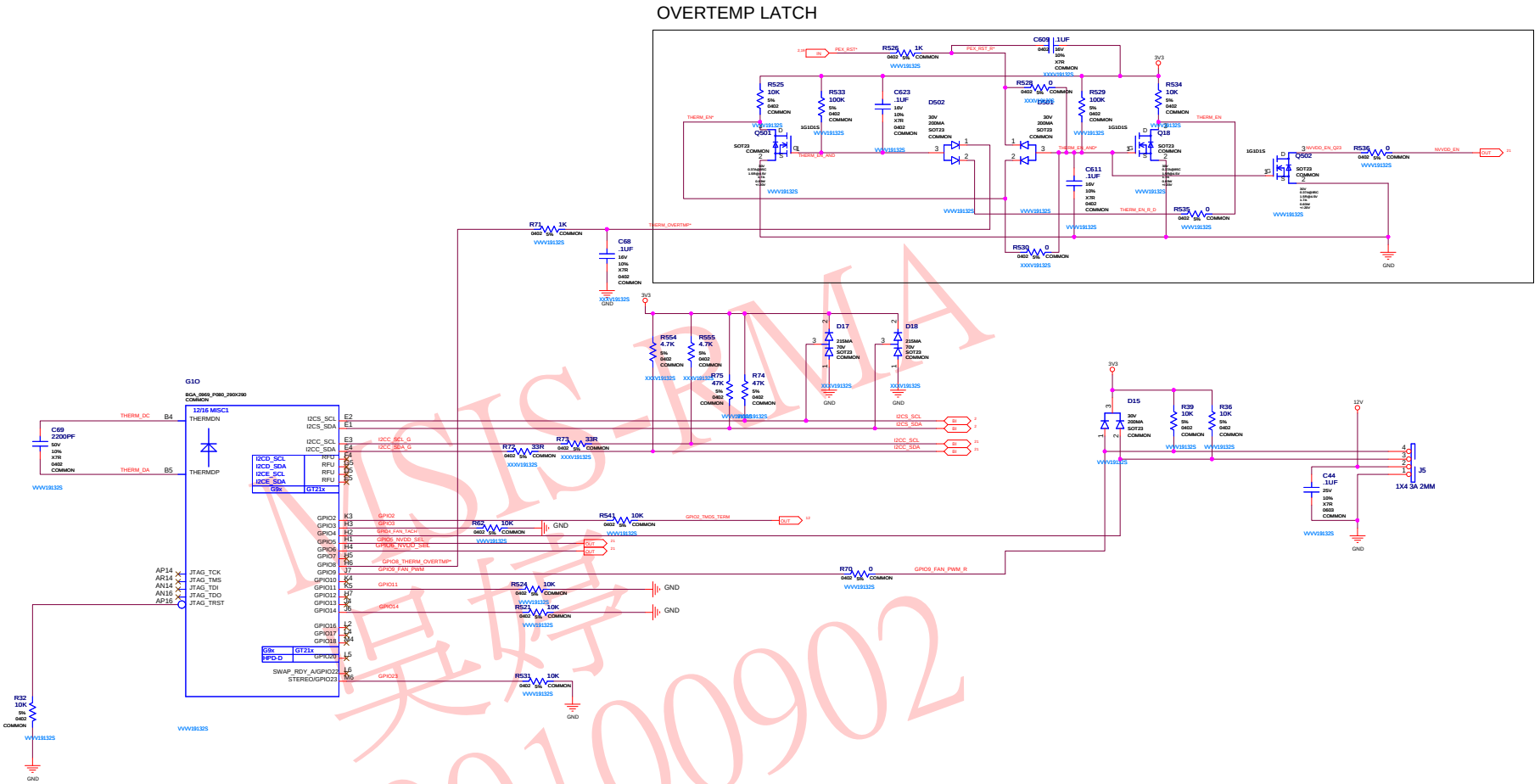
FAN CONTROL, GPIO, JTAG



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PAGE DETAIL	FAN CONTROL, GPIO, JTAG

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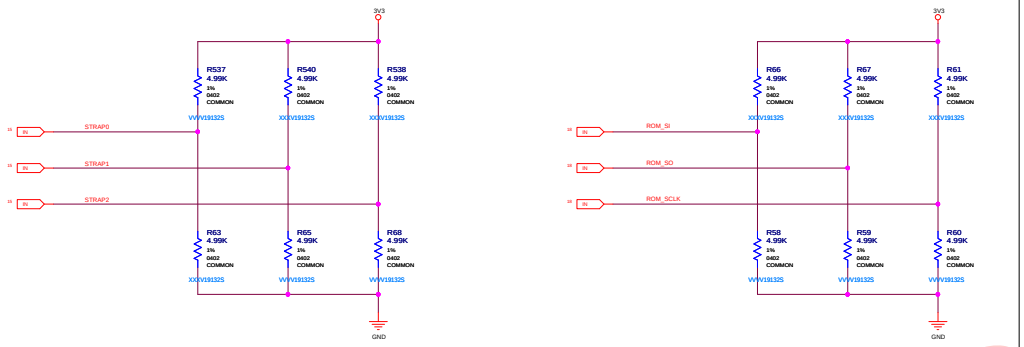
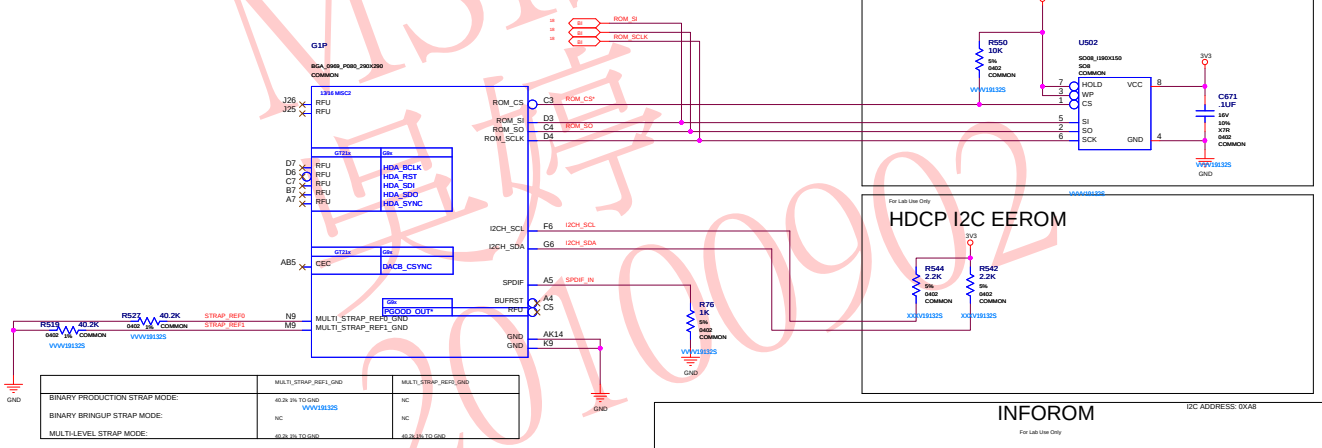
BIOS ROM, HDCP ROM, STRAPPING OPTIONS

STRAPPING OPTIONS



Strap0	USER[3:0]	EDID: 1111	45k pullup
Strap1	3GIOPADCFG[3:0]	Desktop: 0000	5k pulldown
Strap2	PCI_DEVID[3:0]	GT216-350: 0A20	5k pulldown
ROM_SI	RAMCFG[3:0]	64Mx16 DDR3 Hynix: 0010 64Mx16 DDR3 Samsung: 0011	15k pulldown 20k pulldown
ROM_SO	3: XCLK_417 2: FB[] 1: SMB_ALT_ADDR 0: VGA_DEVICE	0010	10k PD
ROM_SCLK	3: PCI_DEV_EXT 2: SUB_VENDOR 1: SLOT_CLK_CFG 0: PEX_PLL_EN_TERM100	0110	35k PD

0: 5k PD	8: 5k PU		
1: 10k PD	9: 10k PU		
2: 15k PD	10: 15k PU		
3: 20k PD	11: 20k PU		
4: 25k PD	12: 25k PU		
5: 30k PD	13: 30k PU		
6: 35k PD	14: 30k PU		
7: 45k PD	15: 45k PU		



	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION STRAP MODE:	40.2k 1% TO GND	NC
BINARY BRINGUP STRAP MODE:	NC	NC
MULTI-LEVEL STRAP MODE:	40.2k 1% TO GND	40.2k 1% TO GND

BIOS ROM(serial)

HDCP I2C EEROM

INFOROM

I2C ADDRESS: 0XA8

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PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

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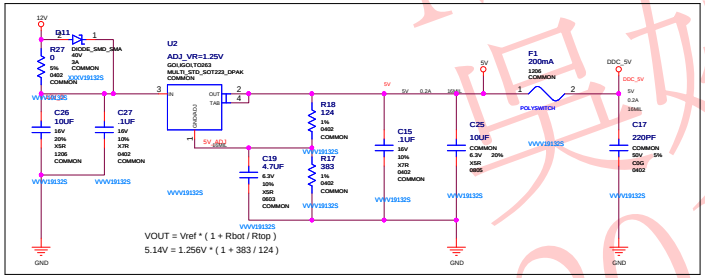
LINEAR POWER SUPPLIES

3v3 cap to minimize coupled noise from NVVDDF8VDD power supplies

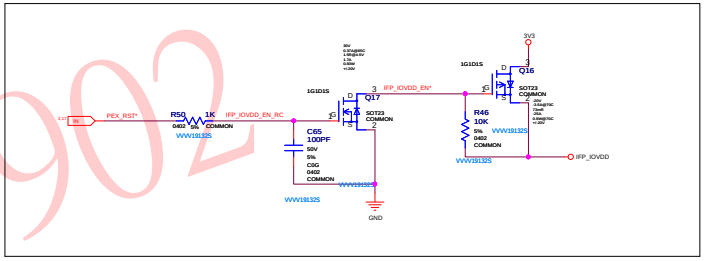
IFP_PLLVDD SUPPLY

VOUT = Vref * (1 + Rbot / Rtop)
1.793V = 0.8V * (1 + 1k / 0.806k)

5V & DDC_5V REGULATOR



IFP_IOVDD BACKDRIVE PREVENTION



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PAGE DETAIL	LINEAR POWER SUPPLIES

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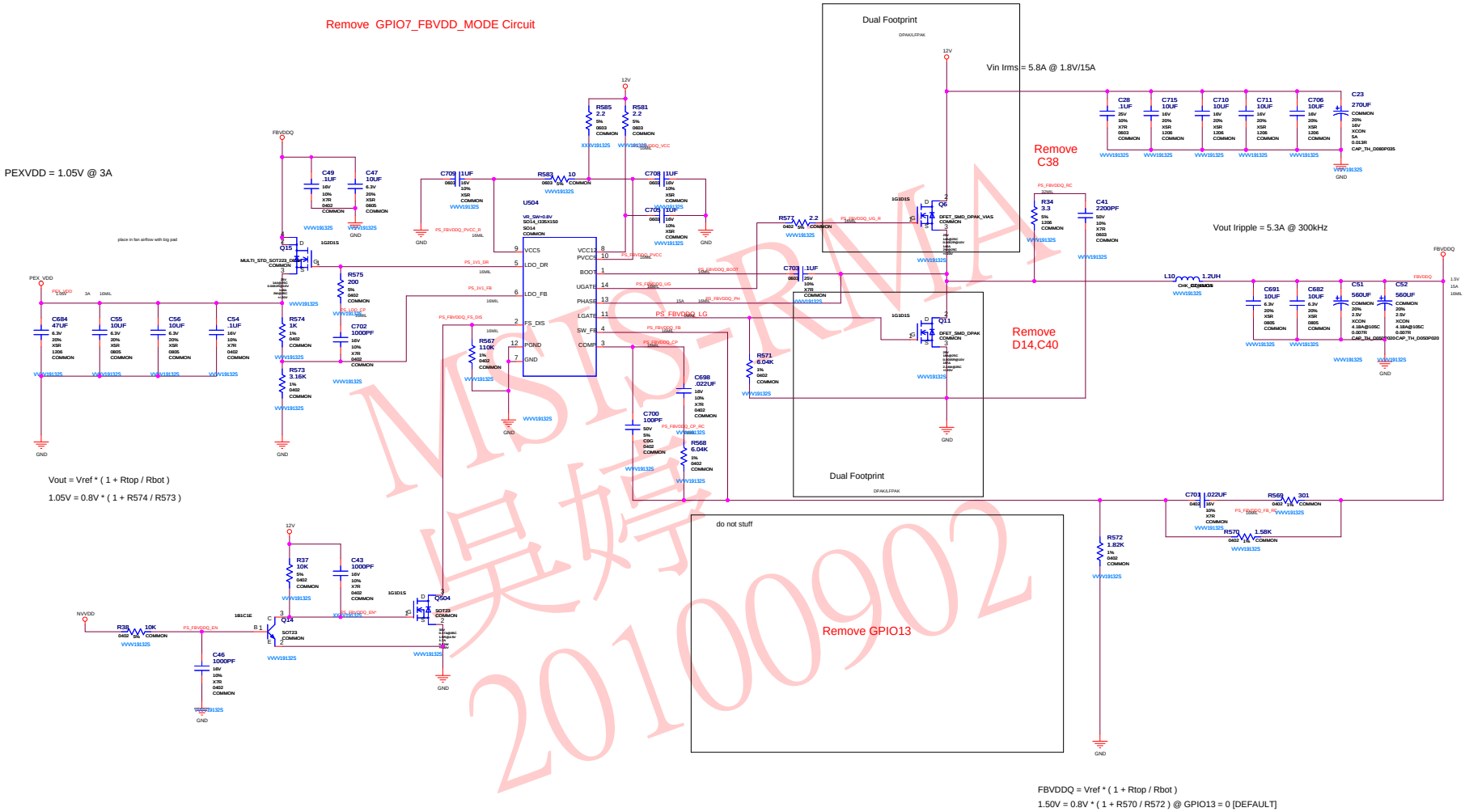
FBVDDQ/PEXVDD POWER SUPPLY



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PAGE DETAIL	FBVDDQ/PEXVDD POWER SUPPLY

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NVVDD POWER SUPPLY

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
NVVDD	38A	20MIL	1.05V

Irms = 7.2A @ 1V/38A/Two phase

NVVDD Power Supply

NVVDD = 1V @ 35-40A

I_ripple=6.49A

V_ripple=22mv

300KHz per phase

NVVDD ENABLE

NVVDD = 0.6 * (1 + Rtop/Rbot)

GPIO6	GPIO5	NVVDD
0	0	0.95V (Low perfmode)
1	0	1.0V
1	1	1.05V

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