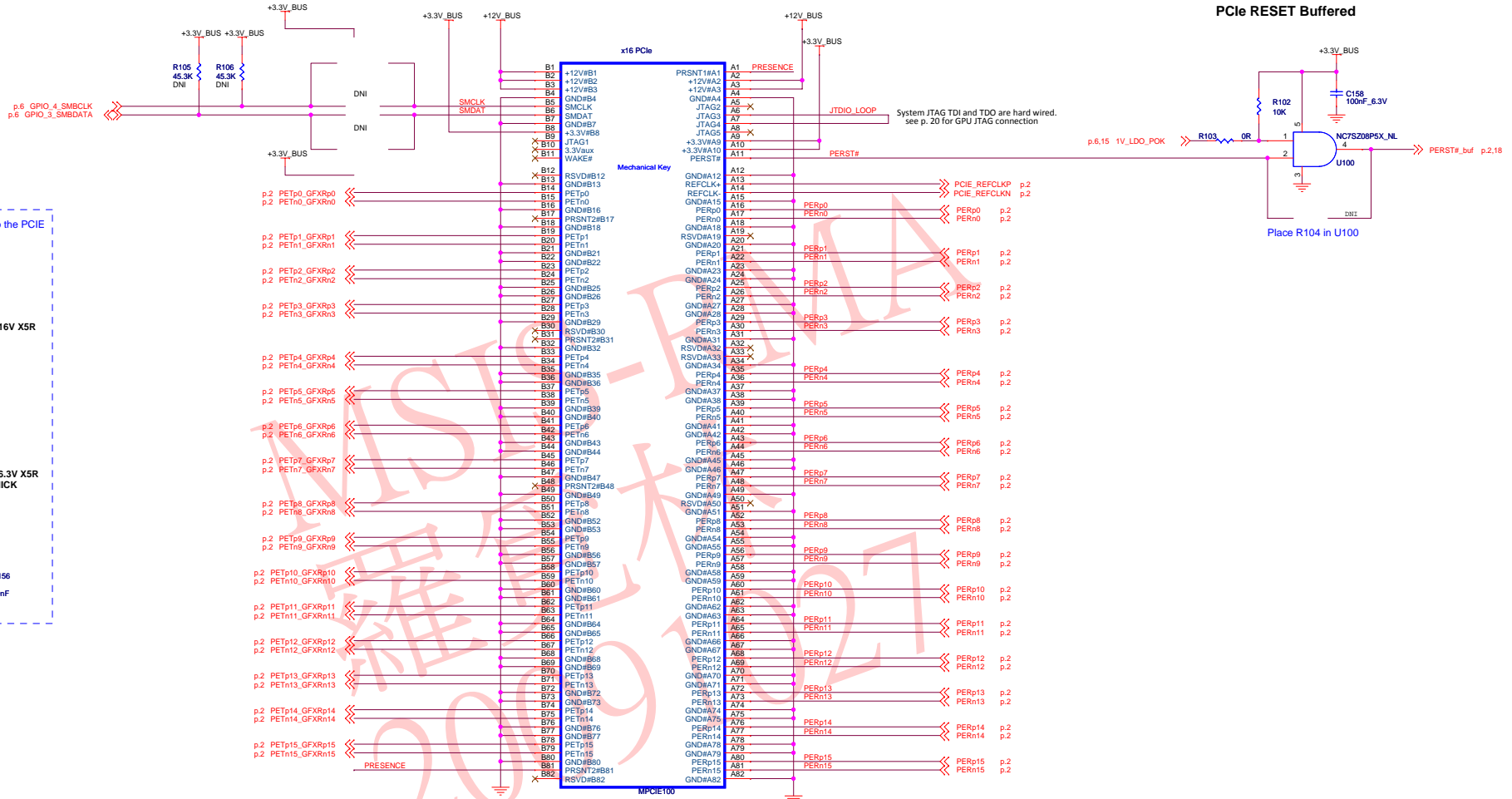


PCI-EXPRESS EDGE CONNECTOR

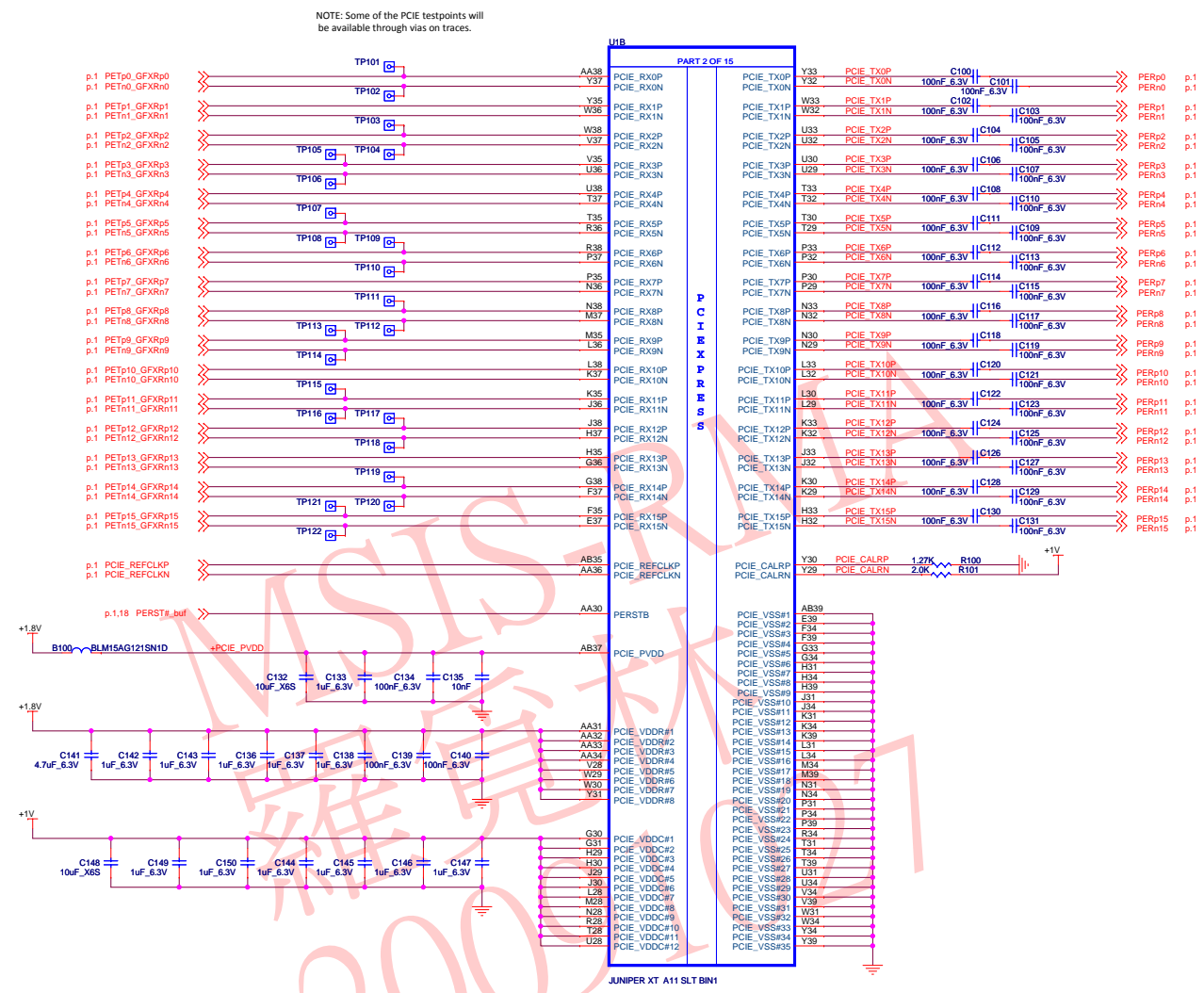


Place these caps as close to the PCIe connector as possible

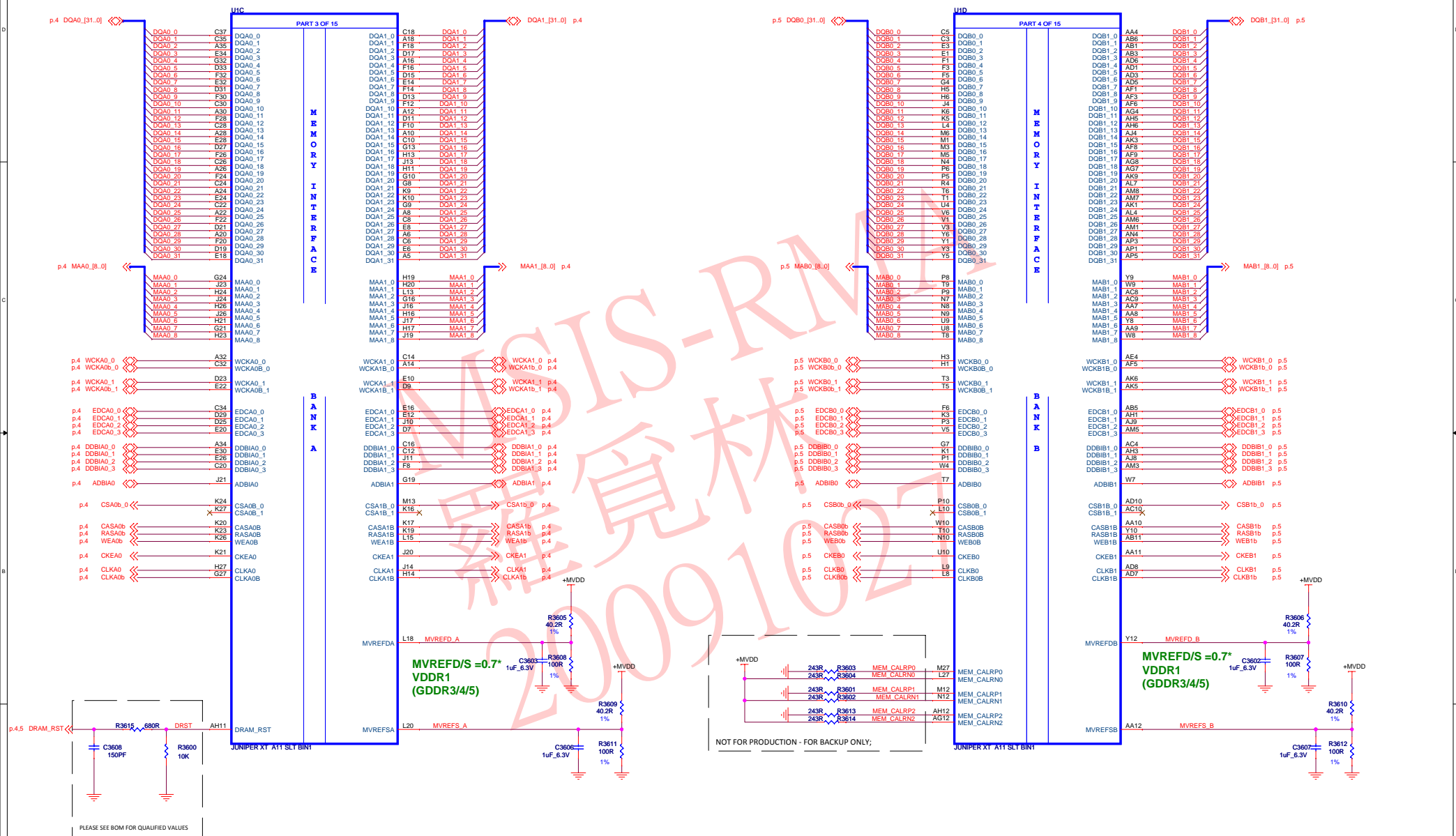
Place R104 in U100

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

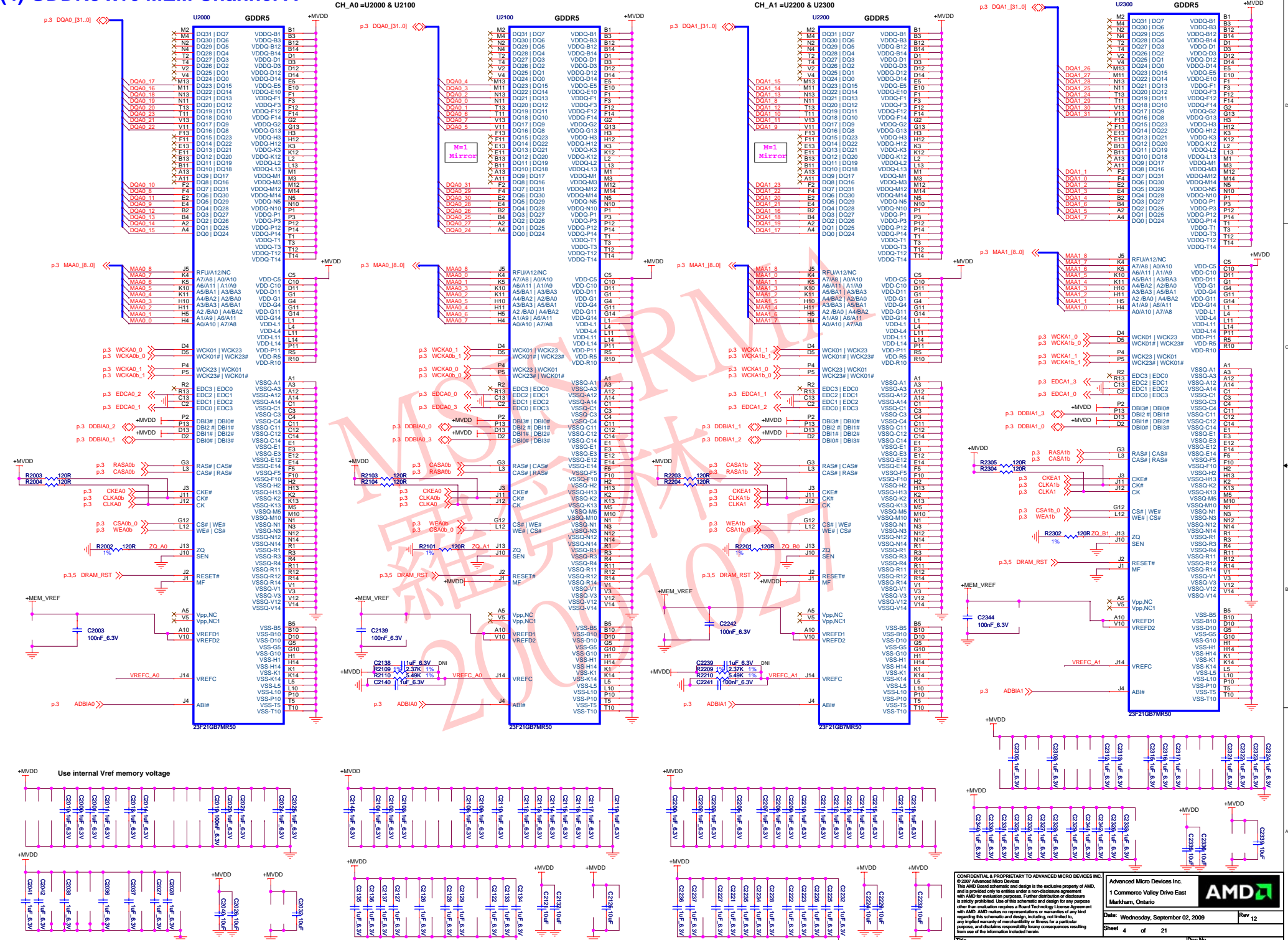
(2) JUNIPER PCIe Interface

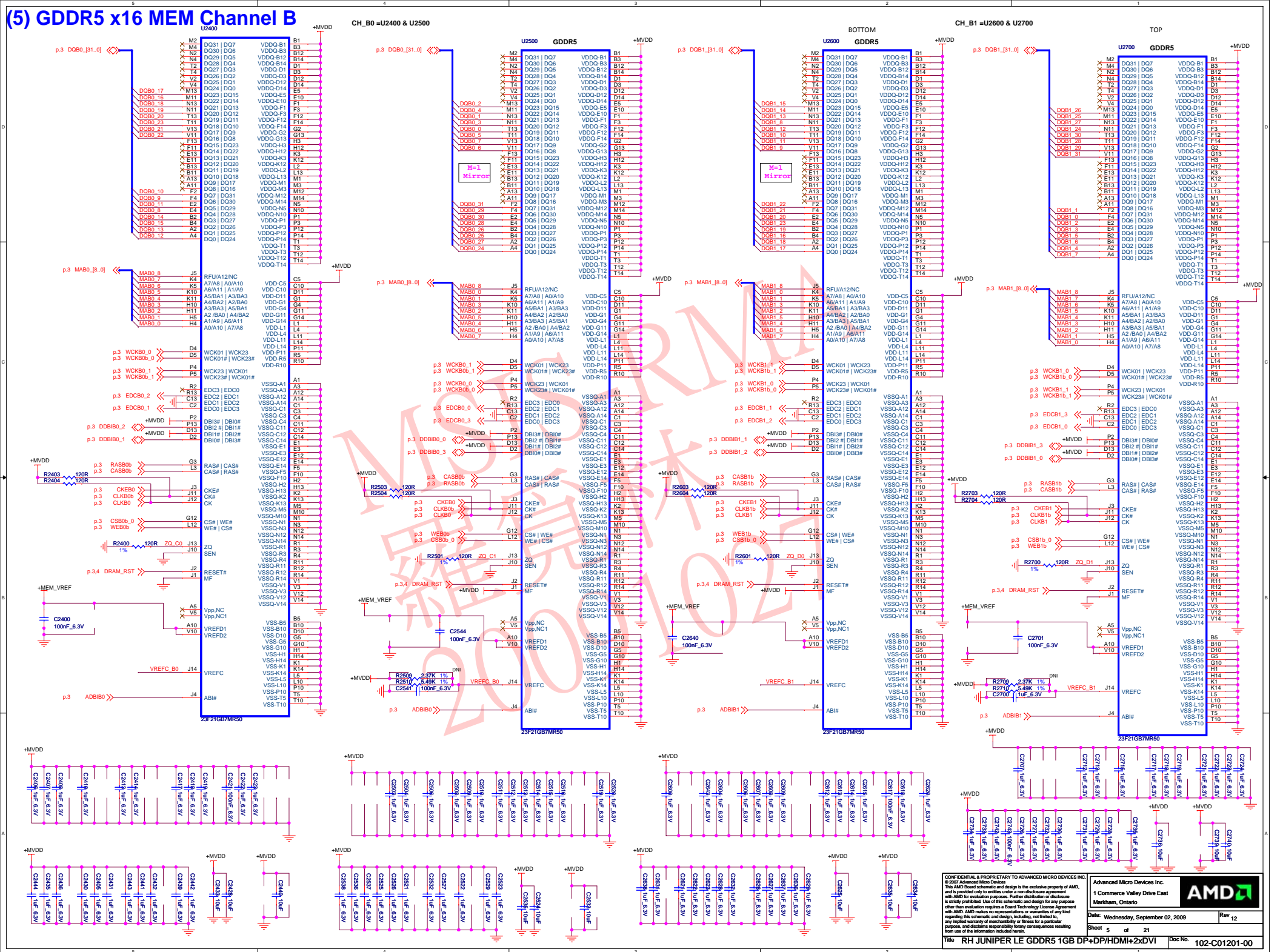


(3) JUNIPER MEM Interface Ch A&B

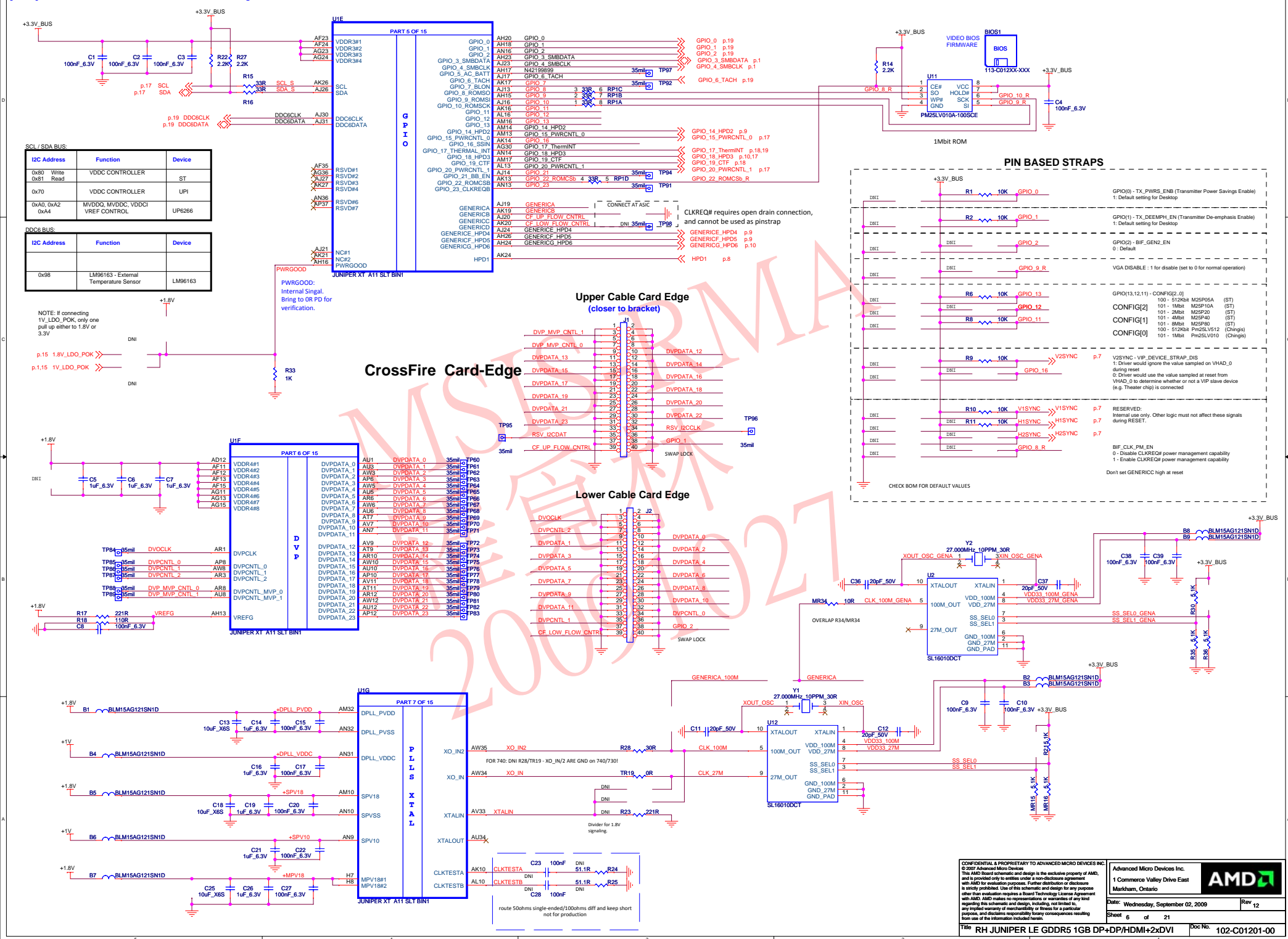


(4) GDDR5 x16 MEM Channel A

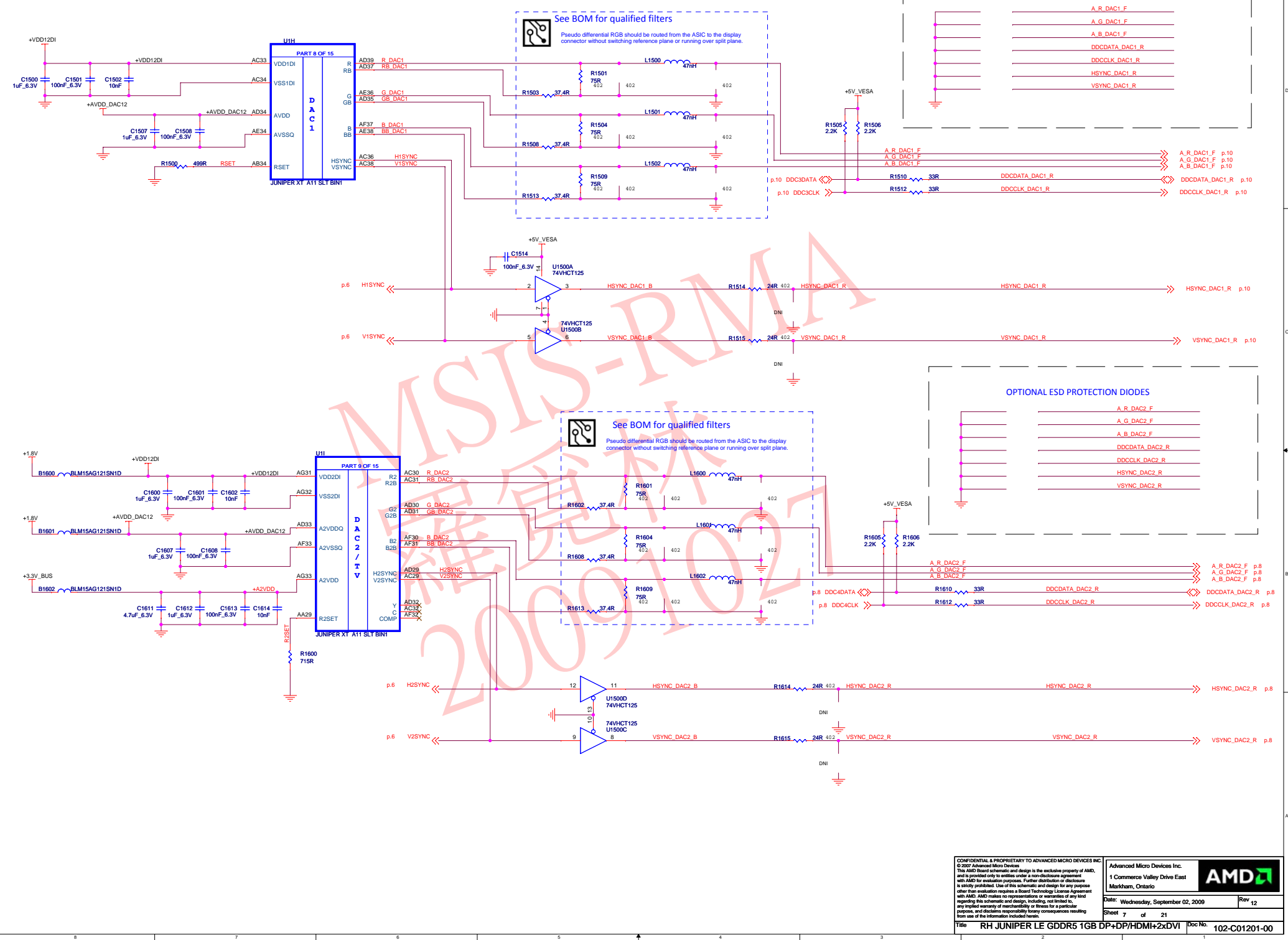




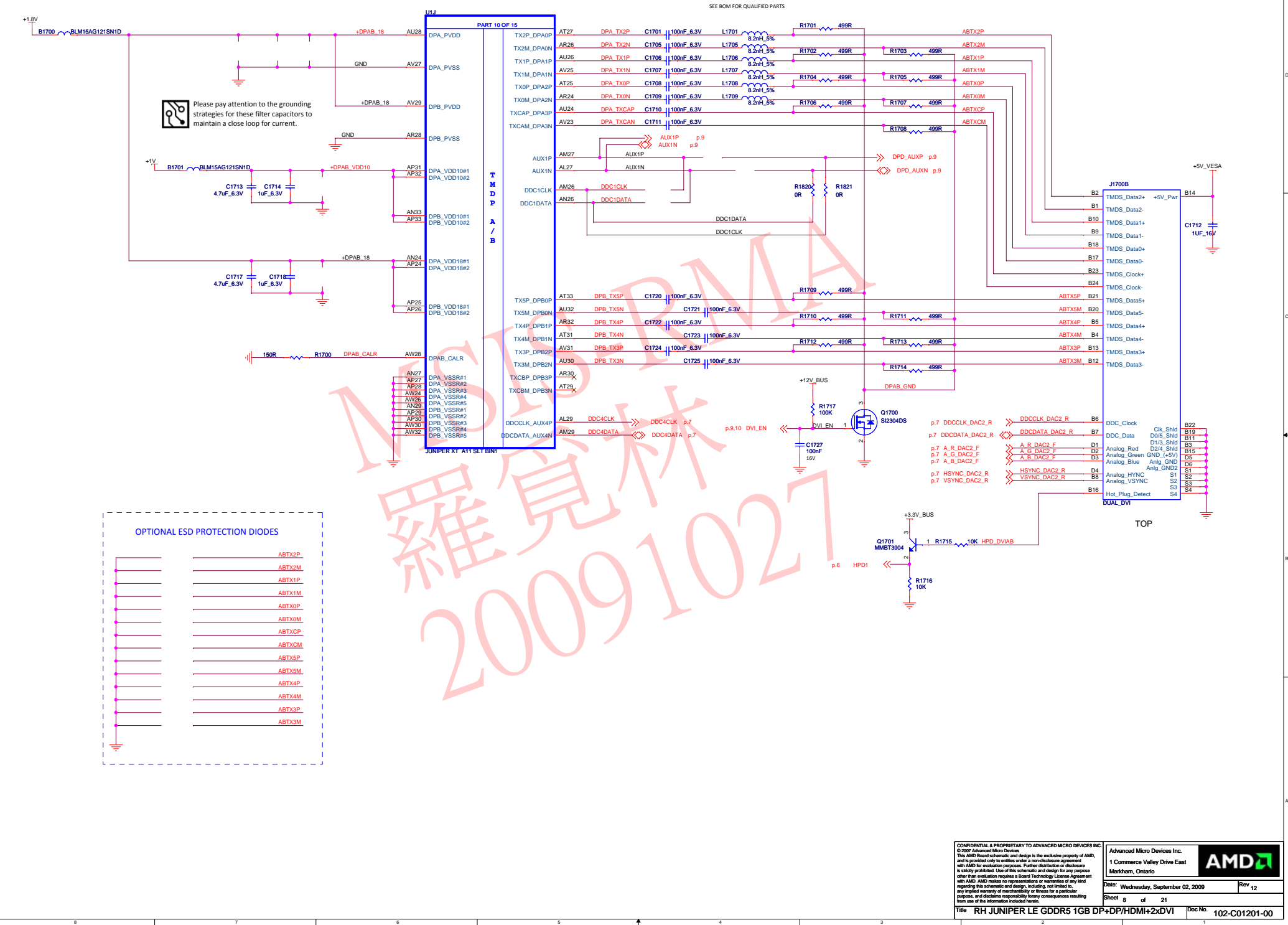
(06) JUNIPER GPIOs Strap CF XTAL OSC



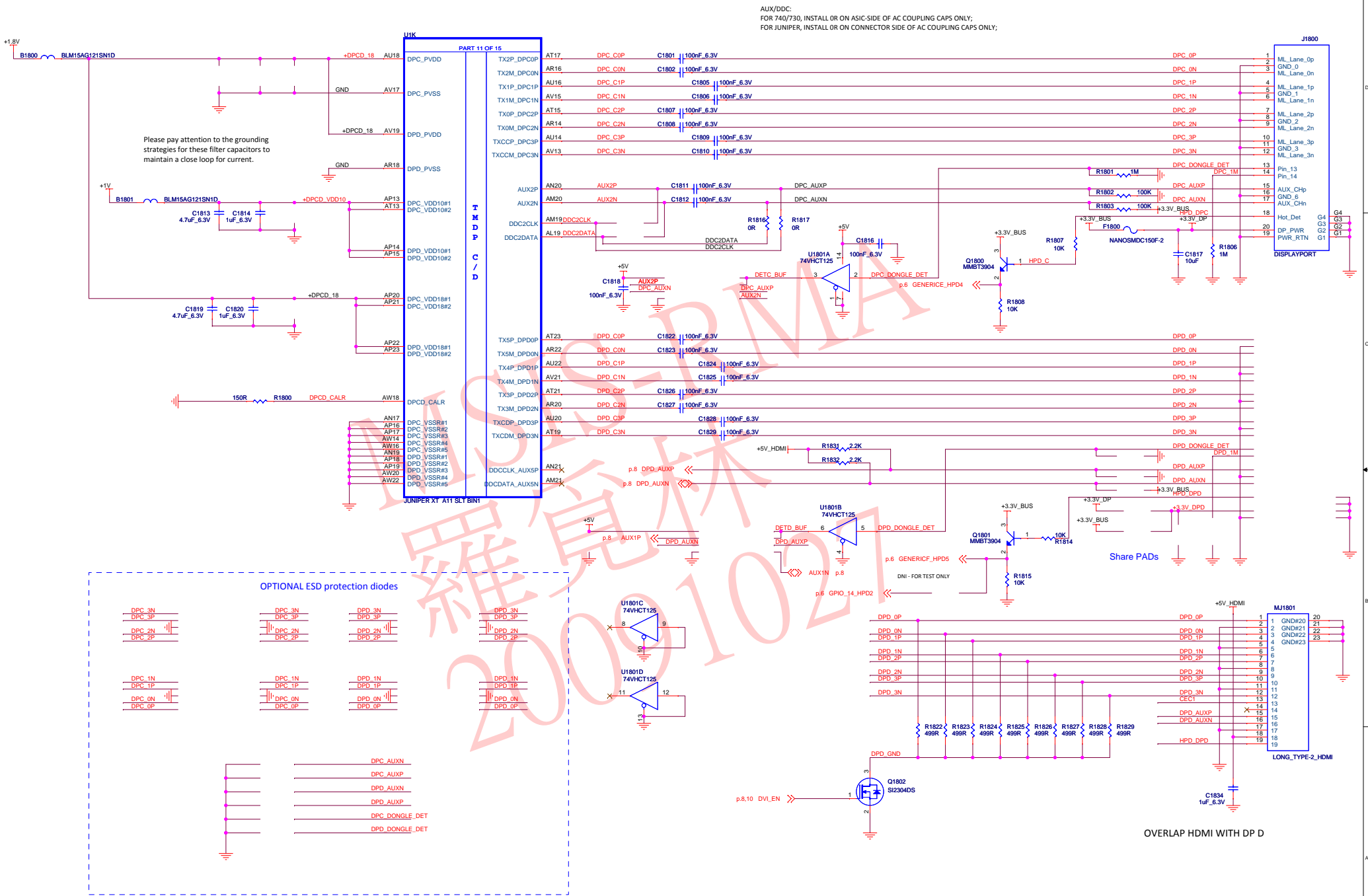
(07) JUNIPER DAC1 and DAC2




(08) JUNIPER TMDP A&B dDVI-I TOP

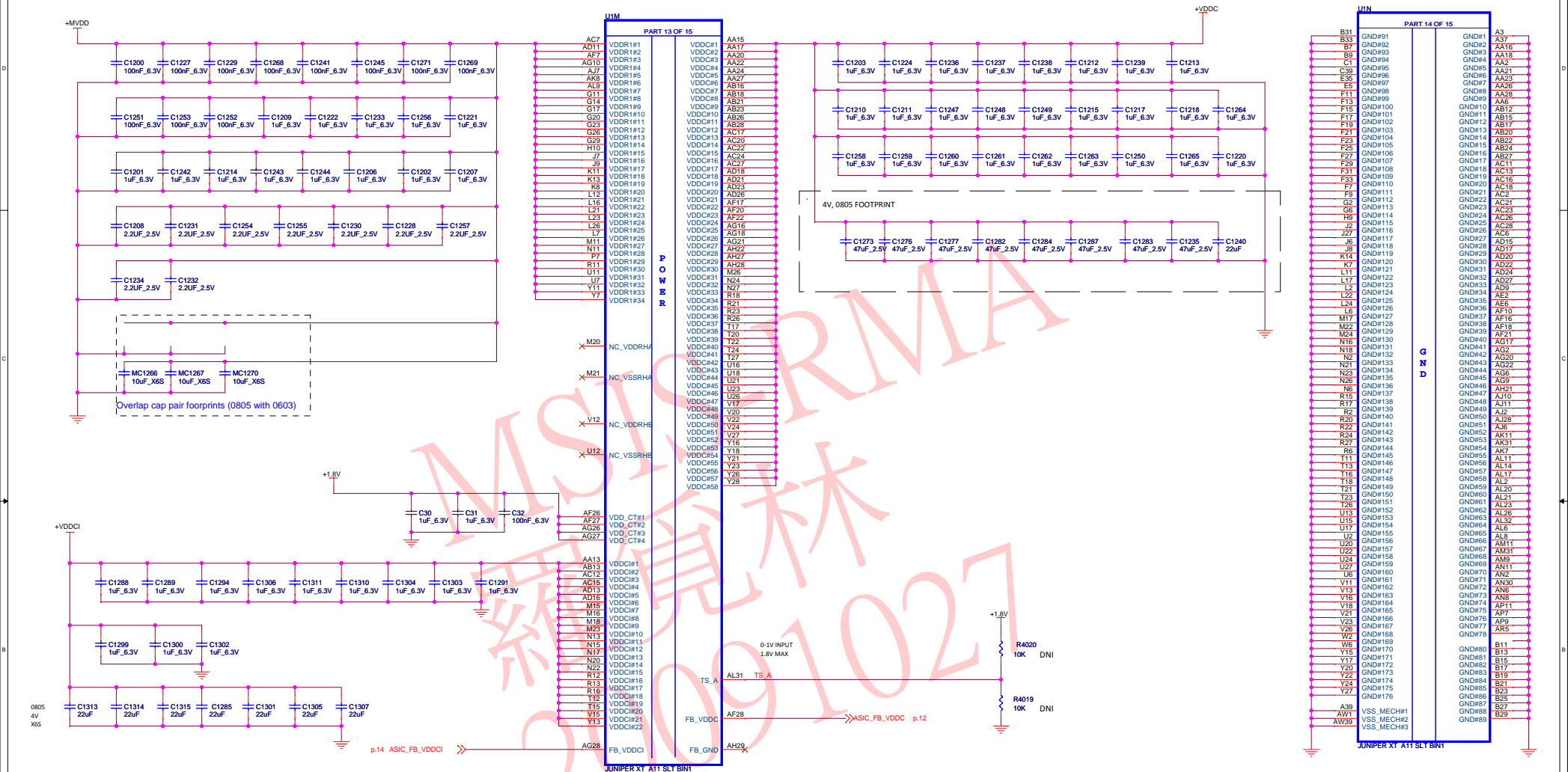


(09) JUNIPER Display Port C & Display Port/HDMI D




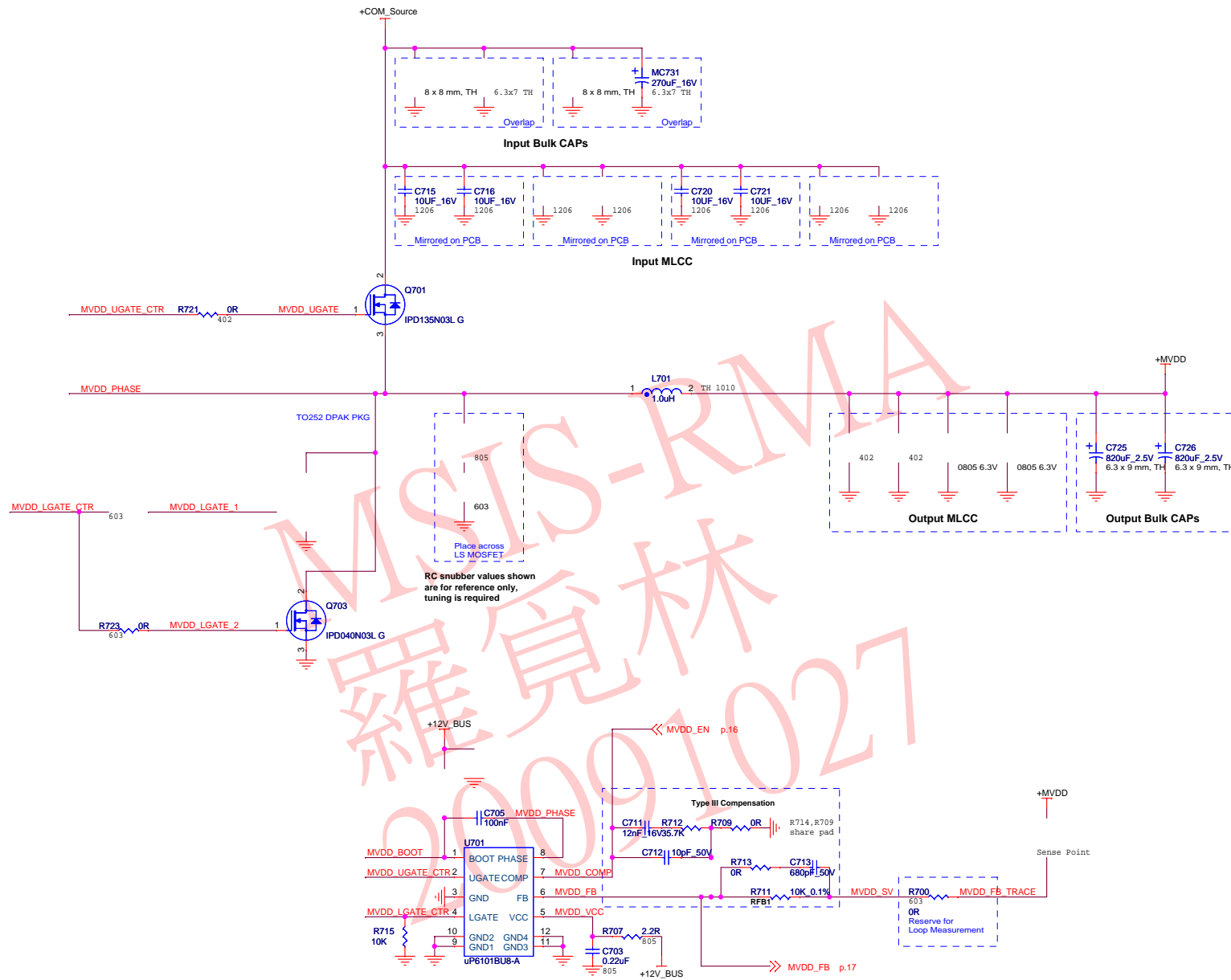
Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario			
Date: Wednesday, September 02, 2009		Rev 12	
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P+DP/HDMI+2xDVI		Doc No. 102-C01201-00	

(11) JUNIPER Power & GND





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Date: <u>Wednesday, September 02, 2009</u>		Rev: <u>12</u>	
Sheet: <u>21</u>		of <u>21</u>	
RH_JUNIPER LE_GDDR5 1GB_DP/HDMI+2xDMI		Doc No: <u>102-C01201-00</u>	



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Date: Wednesday, September 02, 2009

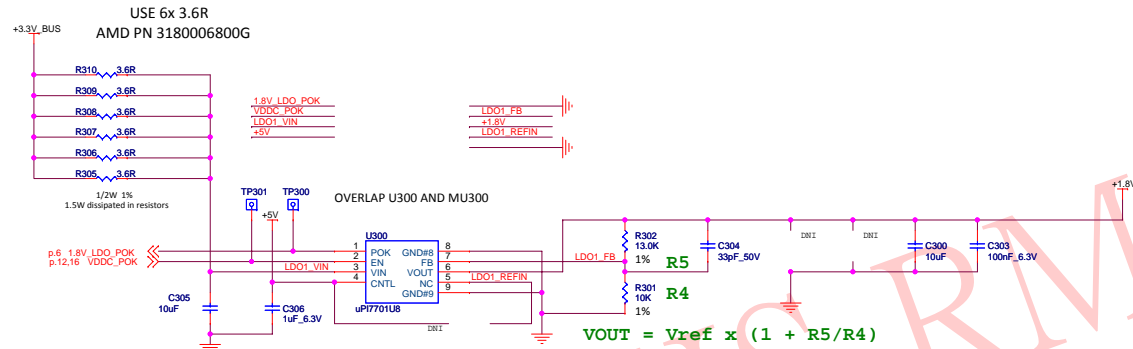
Rev 12

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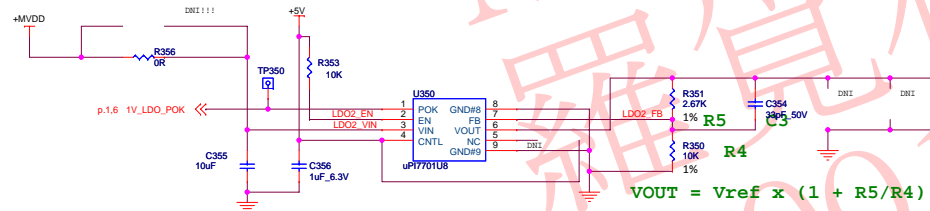
Title RH JUNIPER LE GDDR5 1GB DP+DP/HDMI+2xDVI Doc No. 102-C01201-00

(15) Linear Regulators

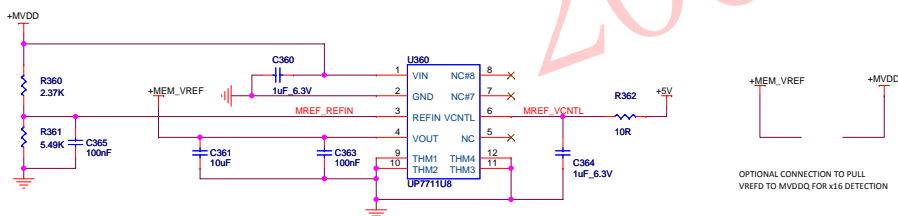
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

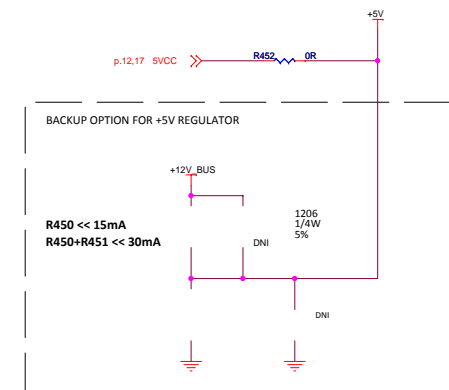
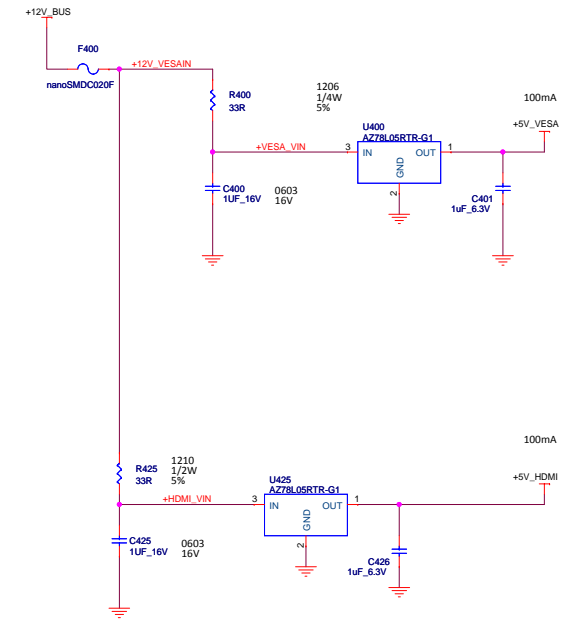


Memory VREF: $V_{in} = MVDDQ$ $V_{out} = 0.7 \times MVDDQ$

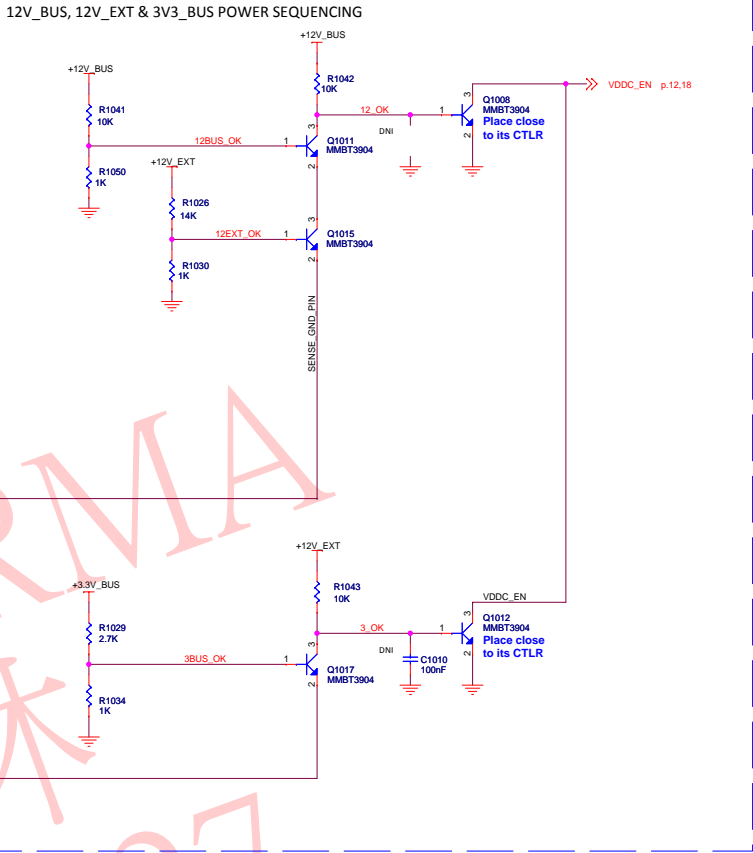
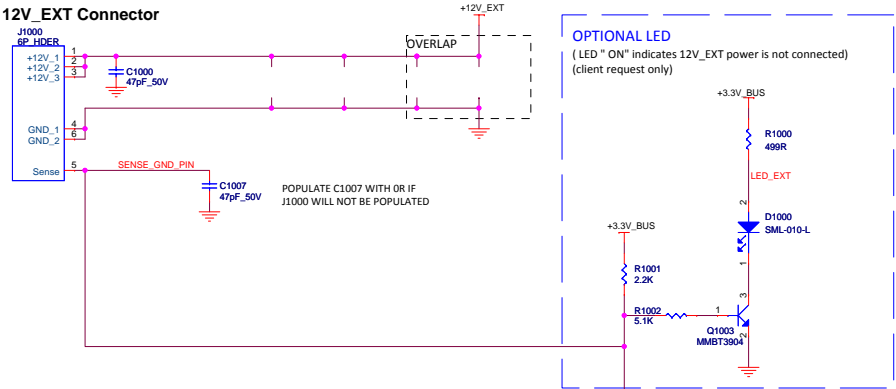


There must be one 100nF at each VREF pin
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices

Regulators for +5V, +5V_VESA and +5V_HDMI

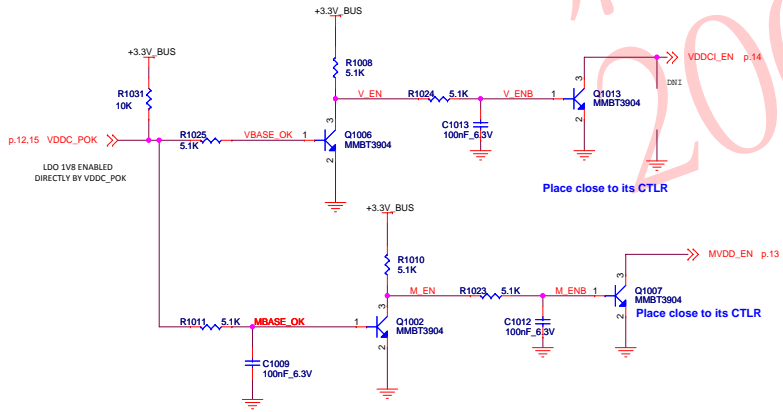


(16) Power Management - Power Gating and External Power Detect

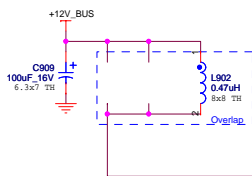
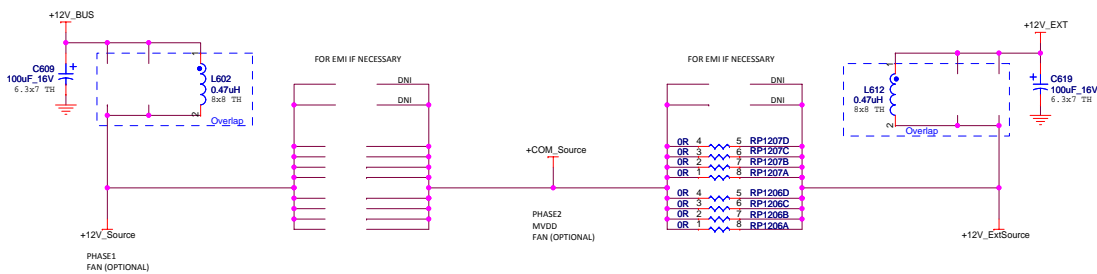


POWER SEQUENCING CIRCUIT

FOR MVDD & VDDCI
(ENABLES CANNOT BE SHARED SINCE IT IS ALSO THE COMPENSATION PIN OF THE SMPS REGULATOR)



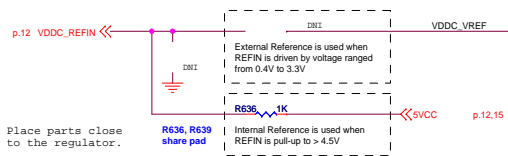
(18) Power Management 2



I2C VOLTAGE REFERENCE FOR VDDC (not for production)



VDDC Reference Voltage Selection



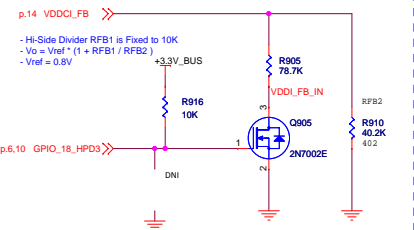
VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

MVDD Low Side Divider

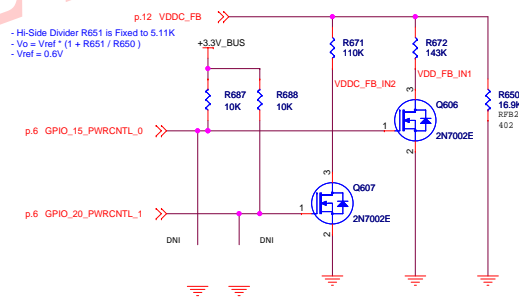


VDDCI Low Side Divider

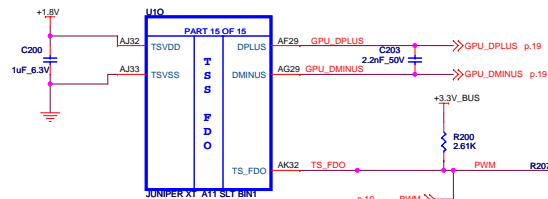


VDDC Low Side Divider

R650 must be populated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.



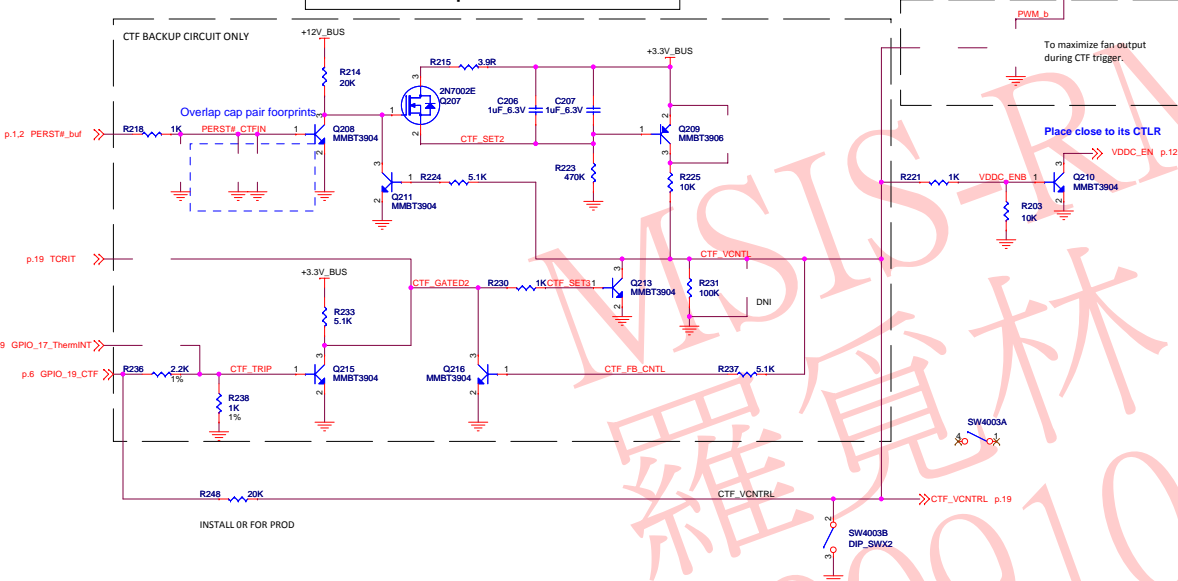
(19) Mechanical and Thermal Management



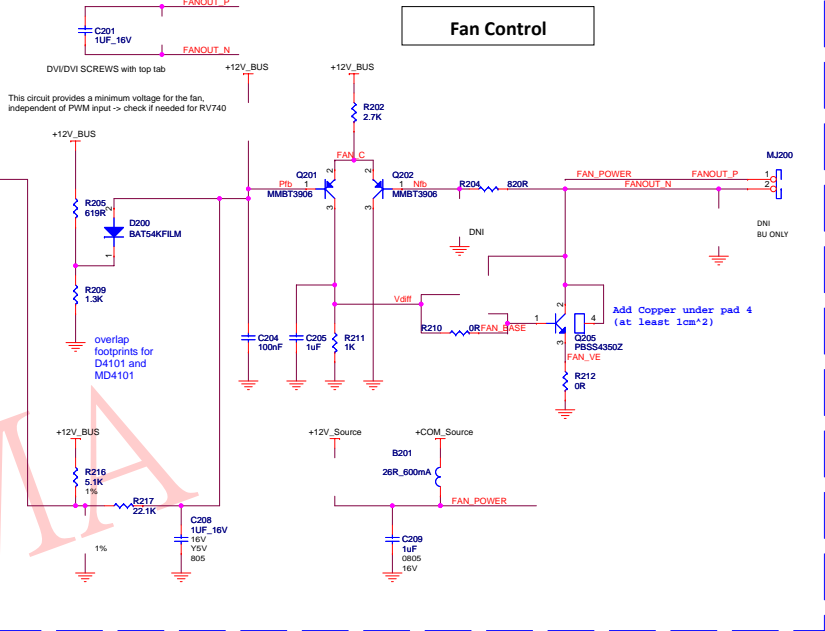
Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board.
This is an open collector signal. Active level is hard pull down to ground.

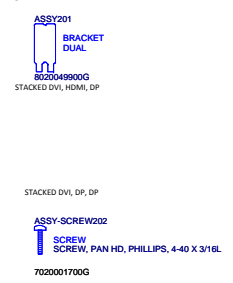
Critical Temperature Fault



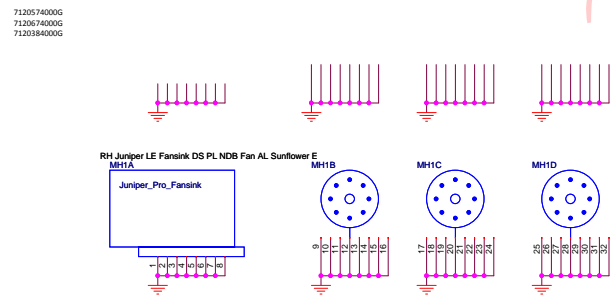
For 2-WIRE FAN



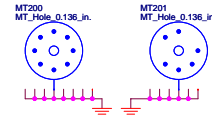
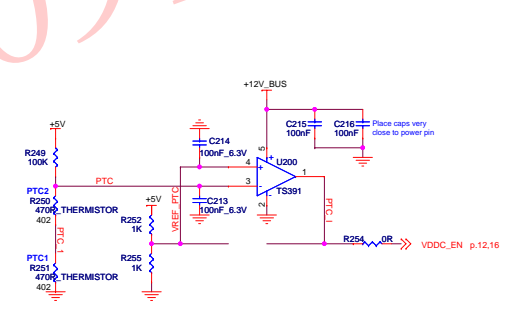
BRACKET



HEATSINK

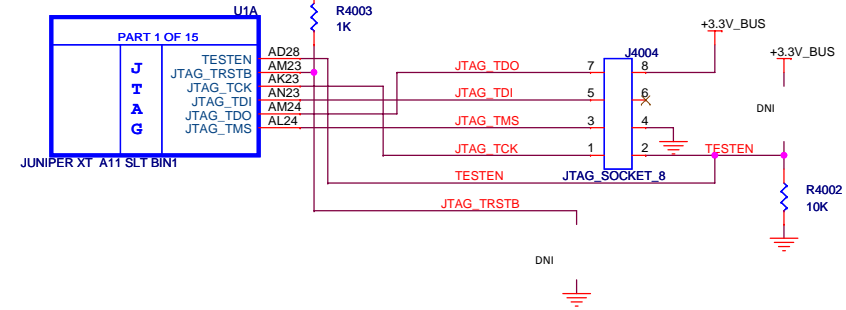


VDDC Thermal Protection

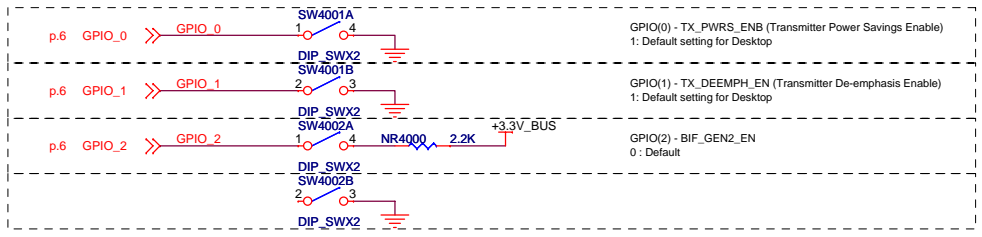


(19) Debug Circuits

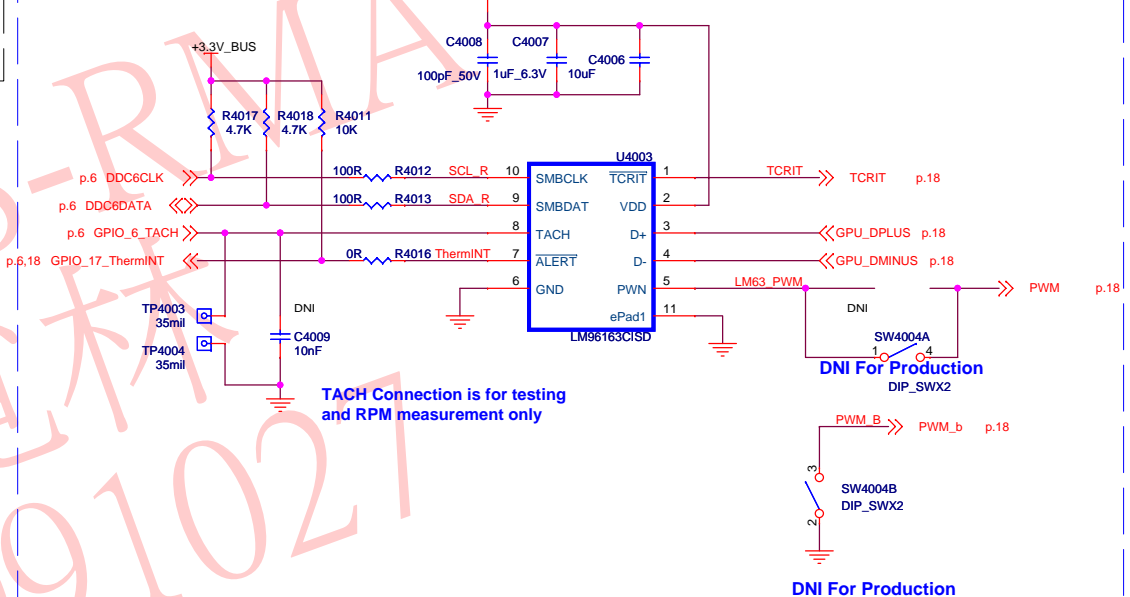
JTAG



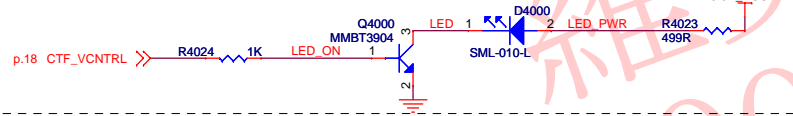
SWITCH CONNECTIONS TO PINSTRAPS



LM96163 FOR BACKUP THERMAL CONTROL



LED RED "ON" shows Fault



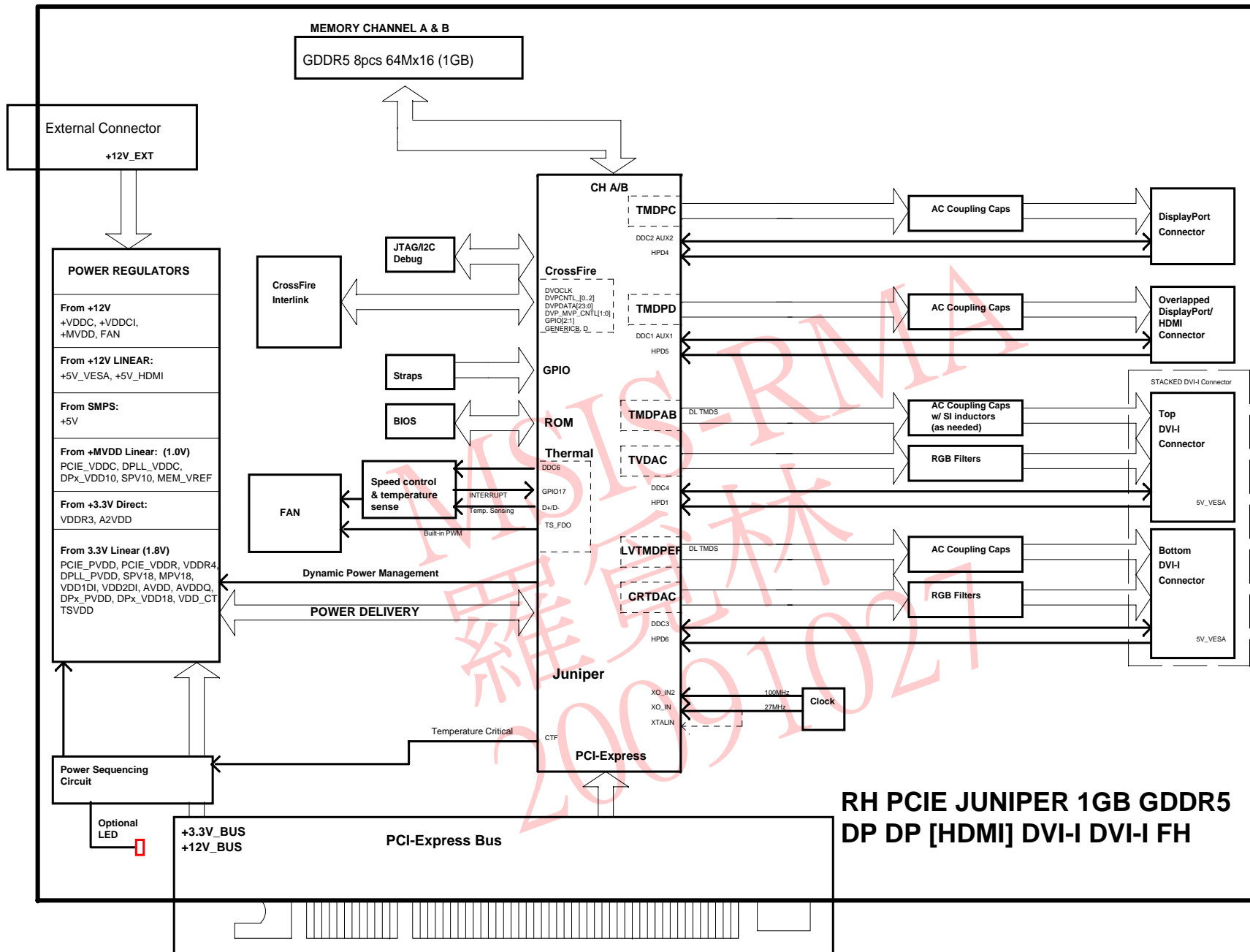
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Rev 12

Title RH JUNIPER LE GDDR5 1GB DP+DP/HDMI+2xDVI Doc No. 102-C01201-00



**RH PCIE JUNIPER 1GB GDDR5
DP DP [HDMI] DVI-I DVI-I FH**

<div>AMD</div>			Title RH JUNIPER LE GDDR5 1GB DP+DP/HDMI+2xDVI		Schematic No. 102-C01201-00	Date: Wednesday, September 02, 2009	
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.				Rev 12
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION				
00	00A	2009/03/23	INITIAL -00A RELEASE				
01	00B	2009/07/13	INITIAL -00B RELEASE				

MSIS-RMA
羅覓林
20091027