NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X

PCI DEVICE ID 0X0=0X200 FOR NV20.

NVVDD SET TO: 1.52V
FBVDD SET TO: 3.47V
FBVDDQ SET TO: 2.59V

HISTORY REVISION:

X00: Based on P50-A06
- See change list in 149- file.
- Set FBVDDQ=2.59V

P50-A07-X01:

- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

P50-A08:

X04: - Delay PLL_VDD to come up after NVVDD.
X05: - Added 1UF accross R257.
X06: - Removed X04-5 above, added a switcher generated PLL delay option.
- SSENA cap for 2nd SW changed to 1UF.
- A05 Si, NVVDD=1.52V

P50-A09:

X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.
X03: - Added option to pull up power good to 12V

ECO1235: - Changed R841 PU to 10K (from 4.7K)

ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction. Replaced C303,306,309 with 75ohm and no stuffed R208-210.

{Item}\t{Quantity}\t{Reference}\t{Source Package} {USR DFINE} {Value}\t{Assembly} {Assembly}{Source Package} {Value}{PN}{AVL1}{AVL2}{AVL3}{AVL4}{AVL5}

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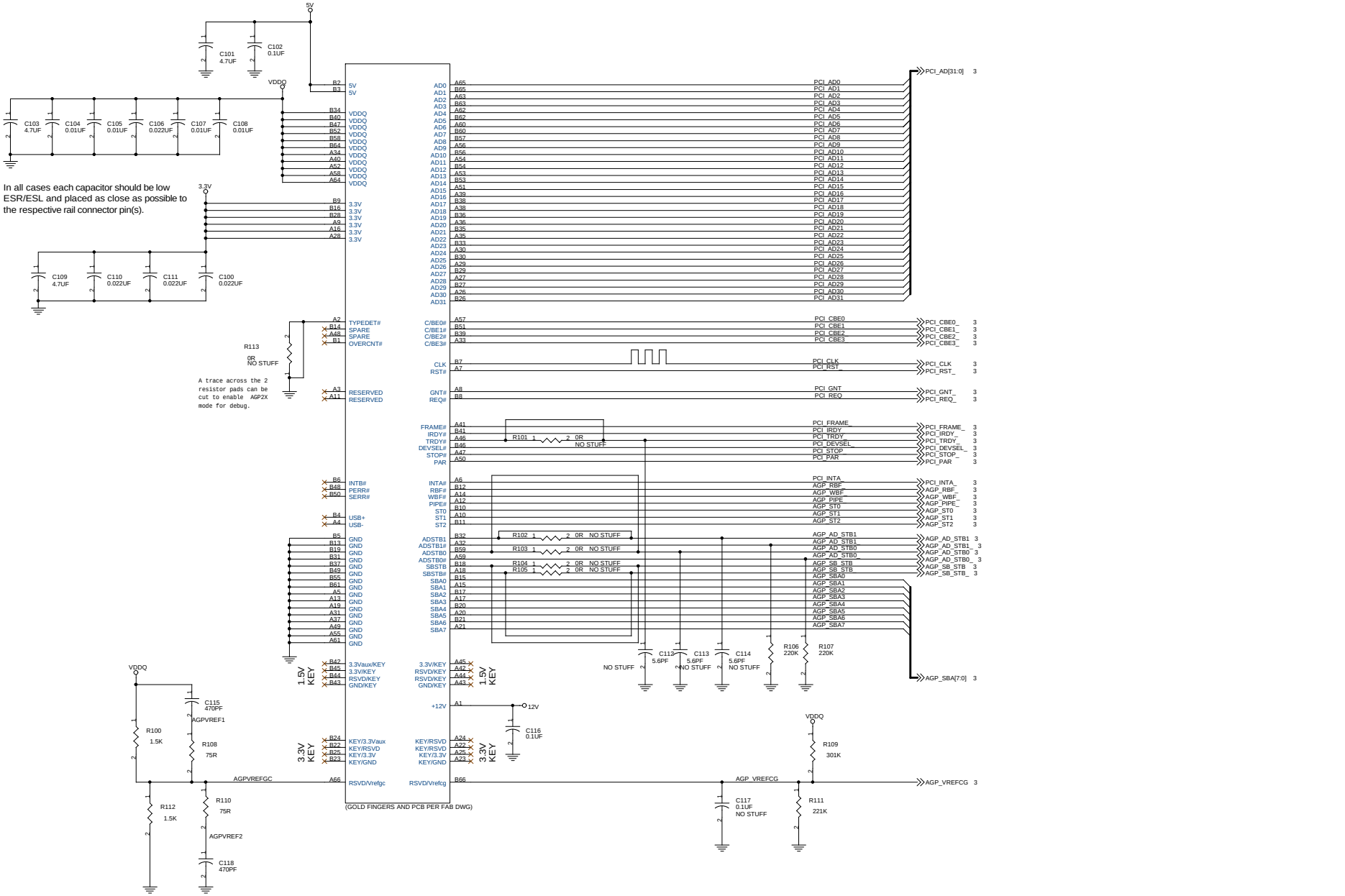

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Size: C	Document Number: BUS I/O	Rev: 0A
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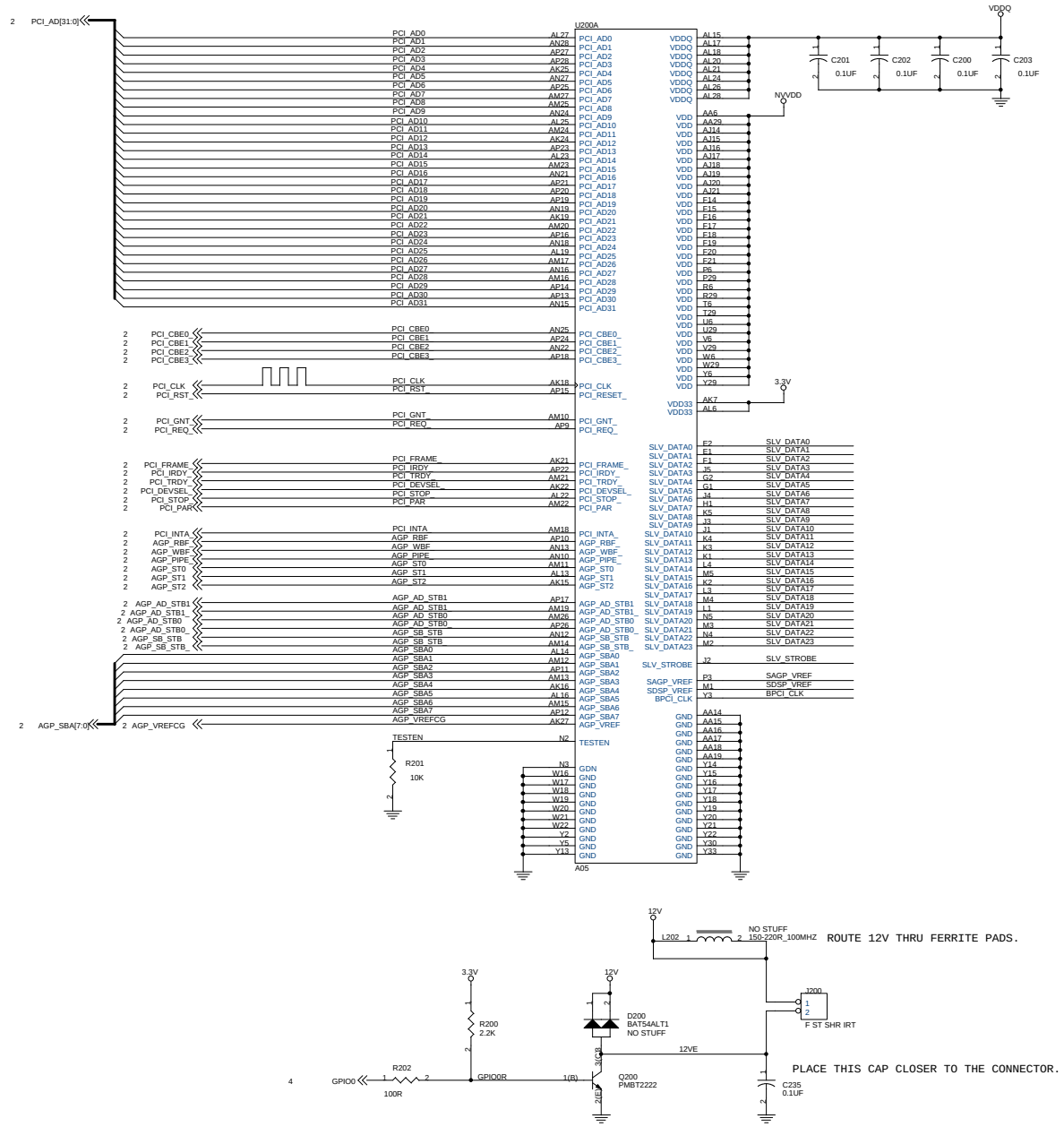

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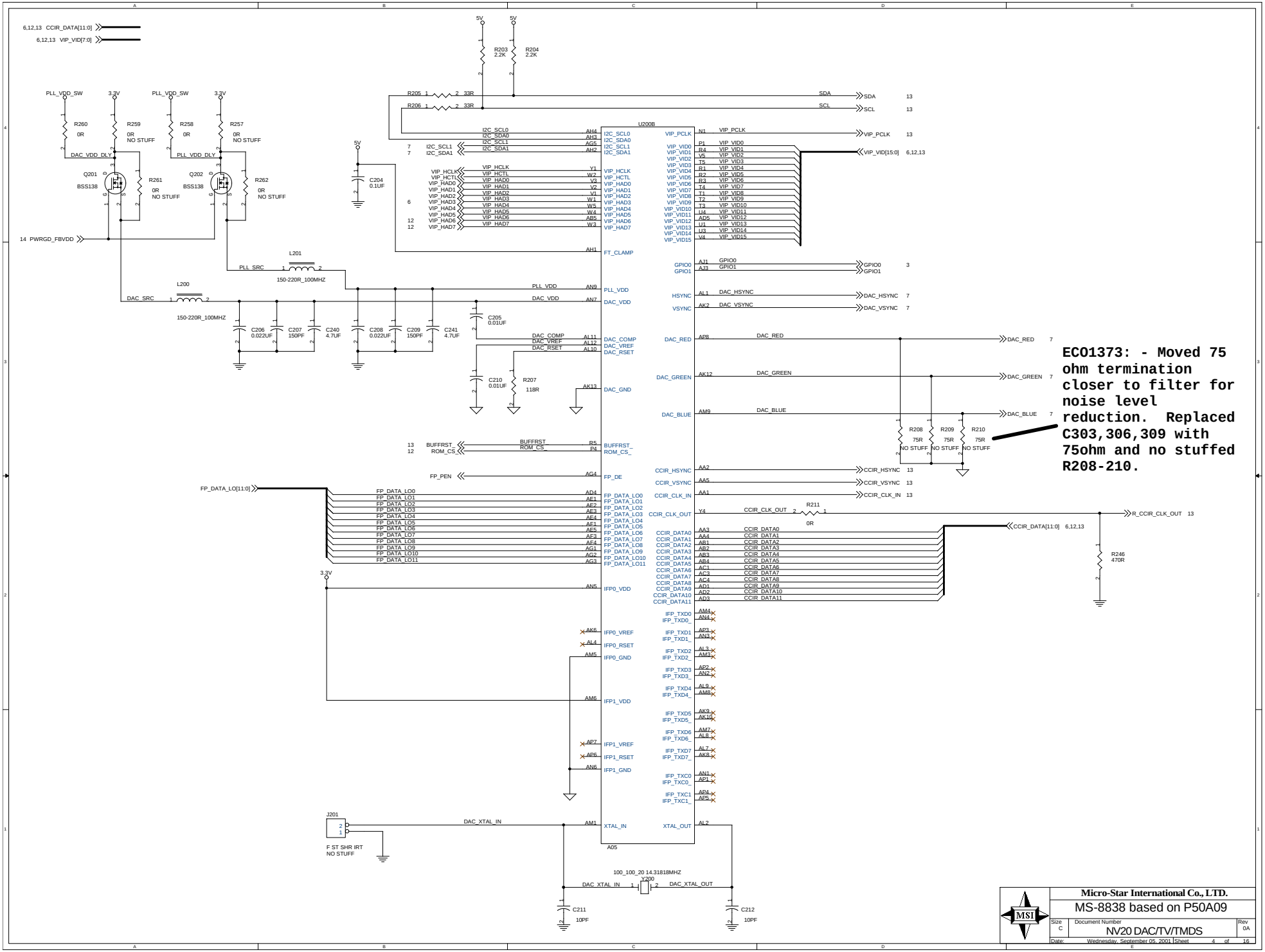
6,12,13 CCIR_DATA[11:0]
6,12,13 VIP_VID[7:0]
U200B
R203 2.2K
R204 2.2K
R205 33R
R206 33R
SDA
SCL
I2C_SCL0
I2C_SDA0
I2C_SCL1
I2C_SDA1
VIP_PCLK
VIP_VID[15:0]
PLL_VDD_SW
3.3V
R260 0R
R259 0R NO STUFF
R258 0R
R257 0R NO STUFF
DAC_VDD_DLY
PLL_VDD_DLY
Q201 BSS138
Q202 BSS138
R261 0R NO STUFF
R262 0R NO STUFF
14 PWRGD_FBVDD
C204 0.1UF
VIP_HCLK
VIP_HCTL
VIP_HAD0
VIP_HAD1
VIP_HAD2
VIP_HAD3
VIP_HAD4
VIP_HAD5
VIP_HAD6
VIP_HAD7
FT_CLAMP
L201
PLL_SRC
150-220R_100MHZ
L200
DAC_SRC
150-220R_100MHZ
C205 0.01UF
C206 0.022UF
C207 150PF
C240 4.7UF
C208 0.022UF
C209 150PF
C241 4.7UF
PLL_VDD
DAC_VDD
DAC_COMP
DAC_VREF
DAC_RSET
C210 0.01UF
R207 118R
DAC_GND
GPIO0
GPIO1
HSYNC
VSYNC
DAC_HSYNC
DAC_VSYNC
DAC_RED
DAC_GREEN
DAC_BLUE
R208 75R NO STUFF
R209 75R NO STUFF
R210 75R NO STUFF
BUFFRST_
ROM_CS_
FP_PEN
FP_DE
FP_DATA_LO[11:0]
FP_DATA_LO0
FP_DATA_LO1
FP_DATA_LO2
FP_DATA_LO3
FP_DATA_LO4
FP_DATA_LO5
FP_DATA_LO6
FP_DATA_LO7
FP_DATA_LO8
FP_DATA_LO9
FP_DATA_LO10
FP_DATA_LO11
CCIR_HSYNC
CCIR_VSYNC
CCIR_CLK_IN
CCIR_CLK_OUT
R211 0R
R_CCIR_CLK_OUT
CCIR_DATA[11:0]
CCIR_DATA0
CCIR_DATA1
CCIR_DATA2
CCIR_DATA3
CCIR_DATA4
CCIR_DATA5
CCIR_DATA6
CCIR_DATA7
CCIR_DATA8
CCIR_DATA9
CCIR_DATA10
CCIR_DATA11
R246 470R
IFP_TXD0_
IFP_TXD1_
IFP_TXD2_
IFP_TXD3_
IFP_TXD4_
IFP_TXD5_
IFP_TXD6_
IFP_TXD7_
IFP_TXC0_
IFP_TXC1_
IFP0_VDD
IFP0_VREF
IFP0_RSET
IFP0_GND
IFP1_VDD
IFP1_VREF
IFP1_RSET
IFP1_GND
J201
F ST SHR IRT NO STUFF
DAC_XTAL_IN
XTAL_IN
XTAL_OUT
A05
100_100_20 14.31818MHZ
Y200
DAC_XTAL_OUT
C211 10PF
C212 10PF
ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction. Replaced C303,306,309 with 75ohm and no stuffed R208-210.
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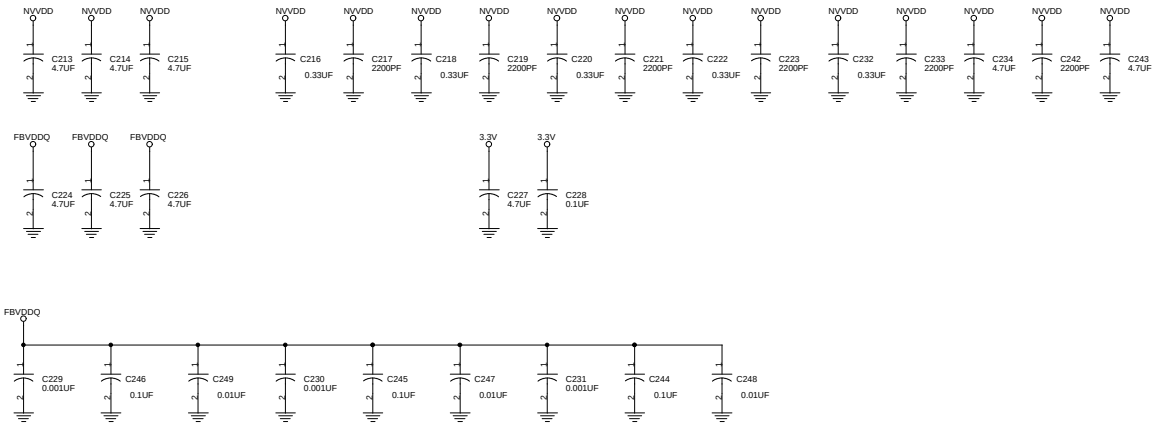
Use thick (non-impedance controlled) traces on XTALIN/OUT



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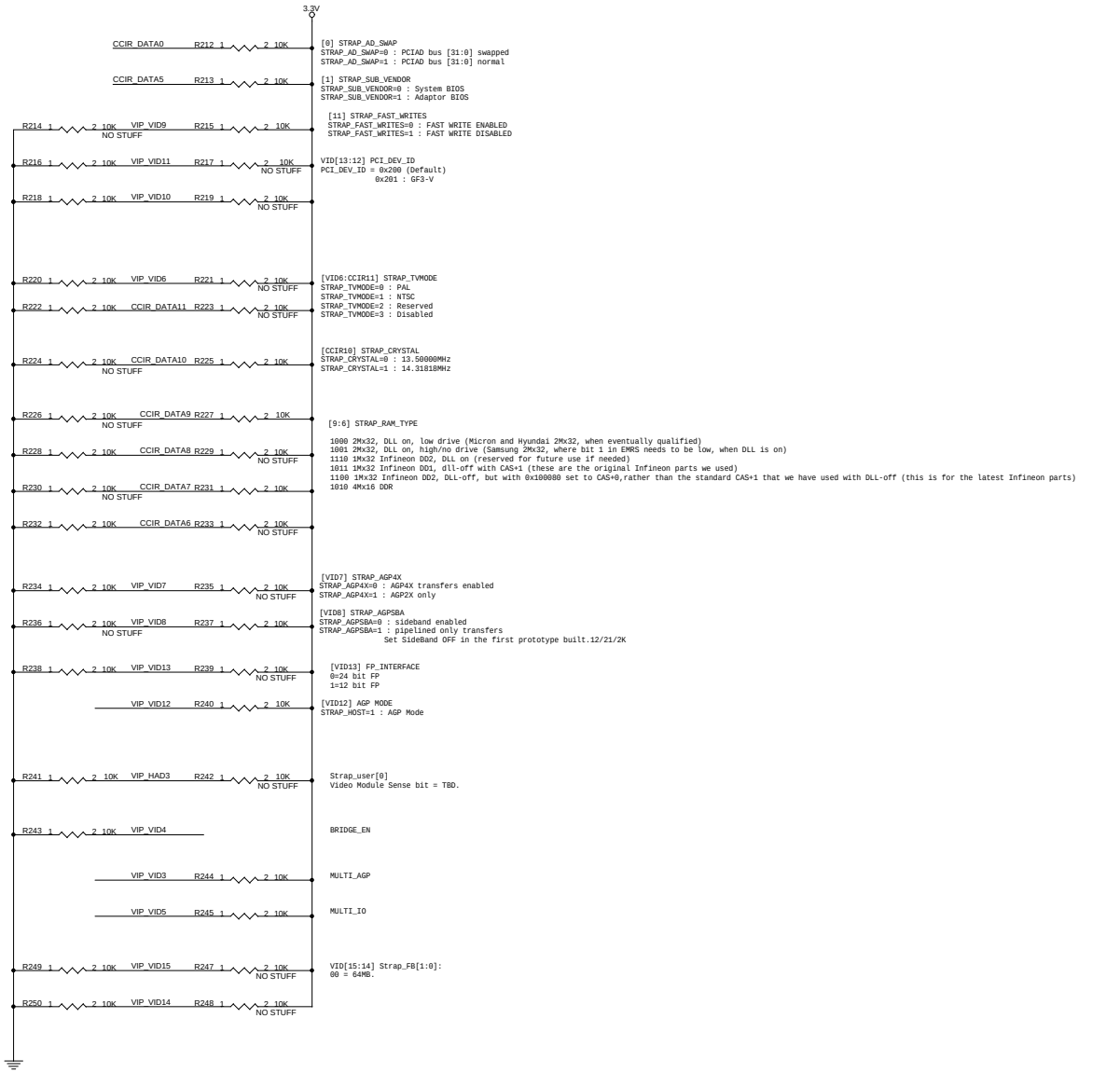
4,12,13 CCIR_DATA[11:0]
4,12,13 VIP_VID[15:0]
4 FP_DATA_LO[11:0]

4 VIP_HAD0
4 VIP_HAD1
4 VIP_HAD2
4 VIP_HAD3
4 VIP_HAD4
4 VIP_HAD5
4,12 VIP_HAD6
4,12 VIP_HAD7



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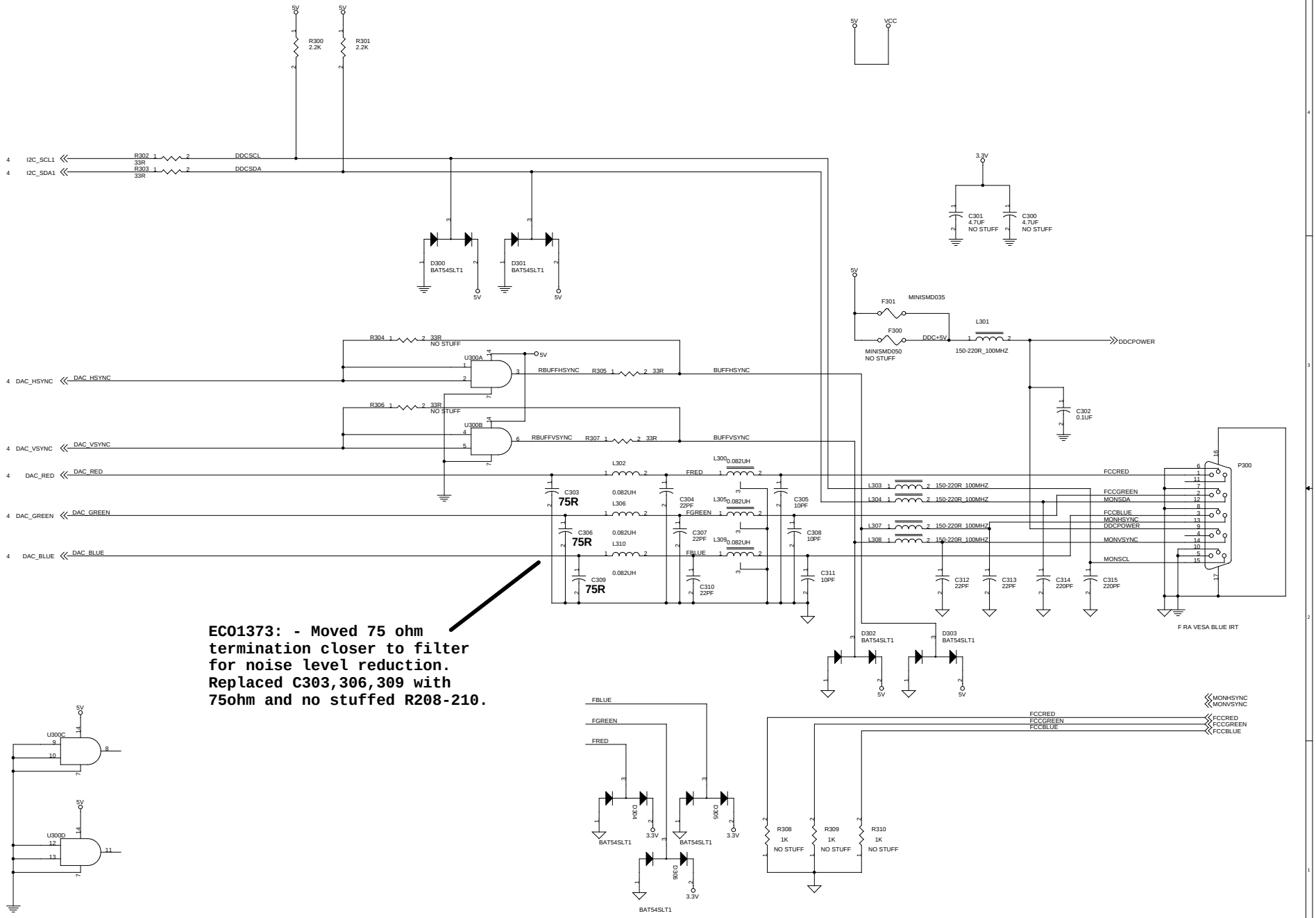

ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction. Replaced C303,306,309 with 75ohm and no stuffed R208-210.

Micro-Star International Co., LTD.		
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Size: C	Document Number: DAC I/O	Rev: 0A
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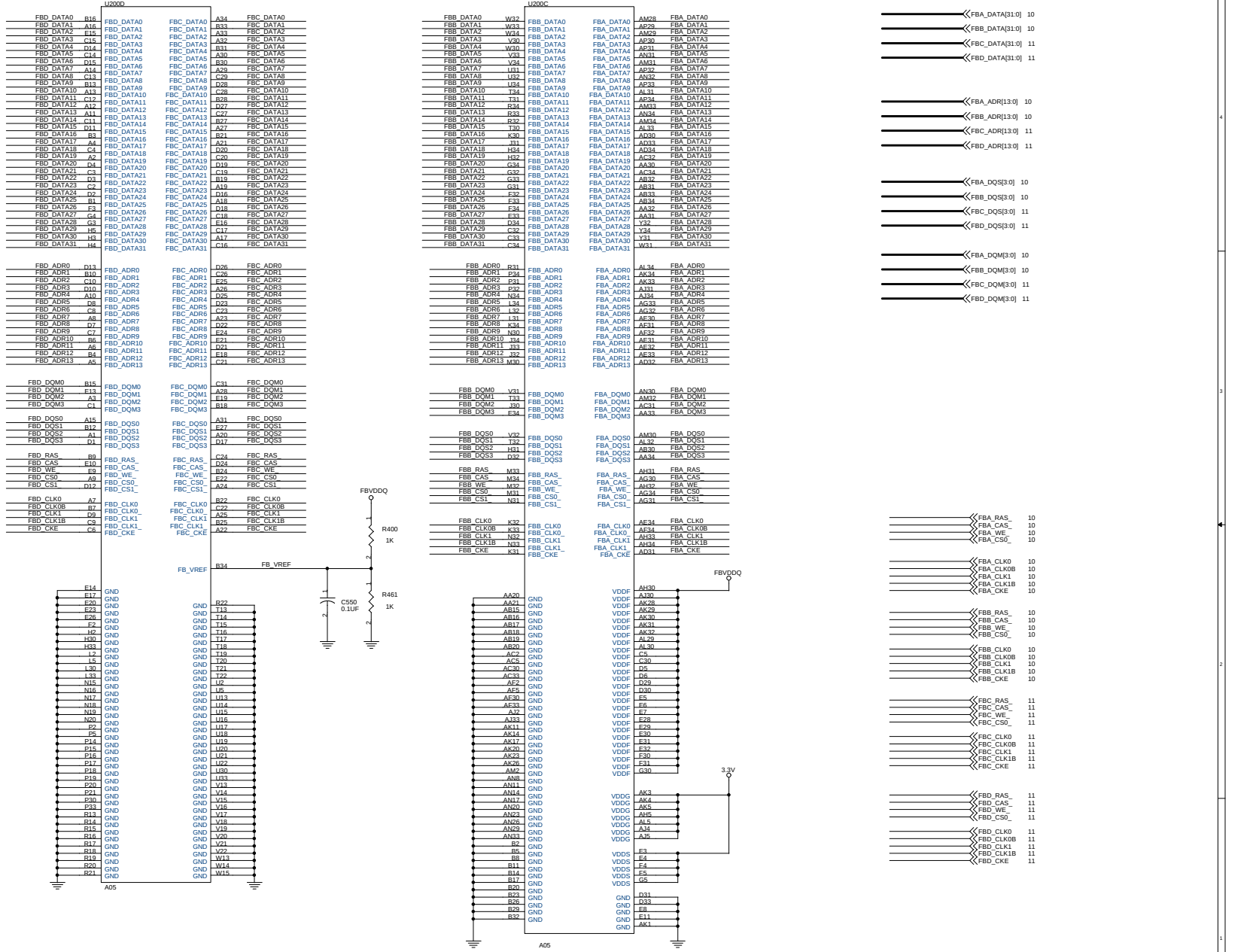

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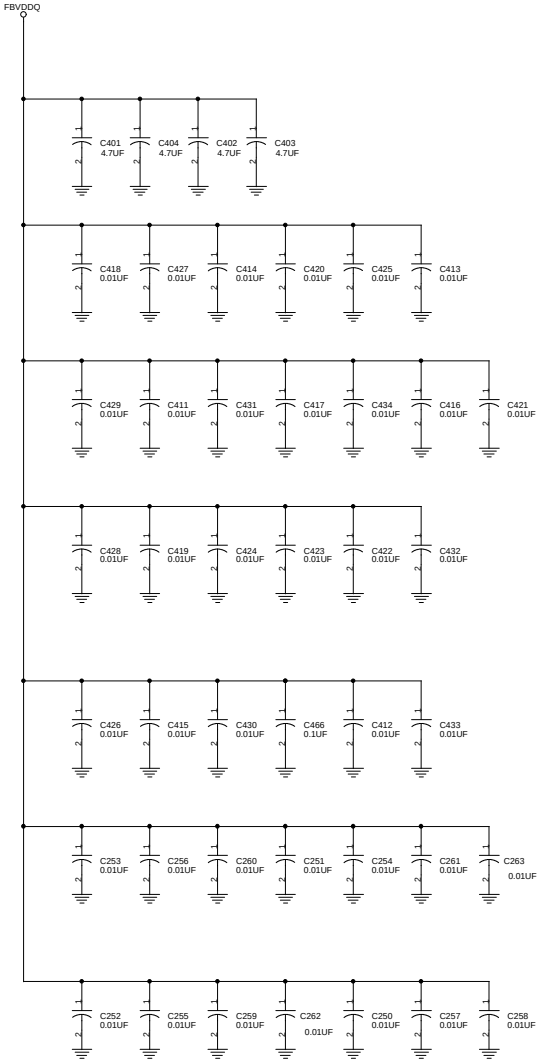

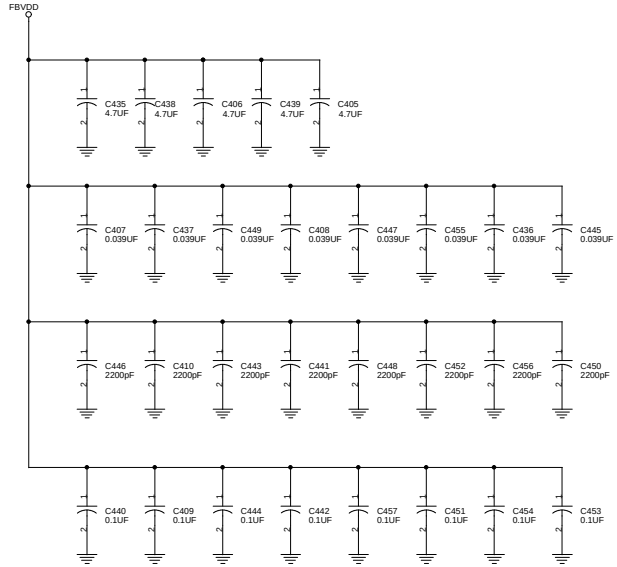

MSI	Micro-Star International Co., LTD.	
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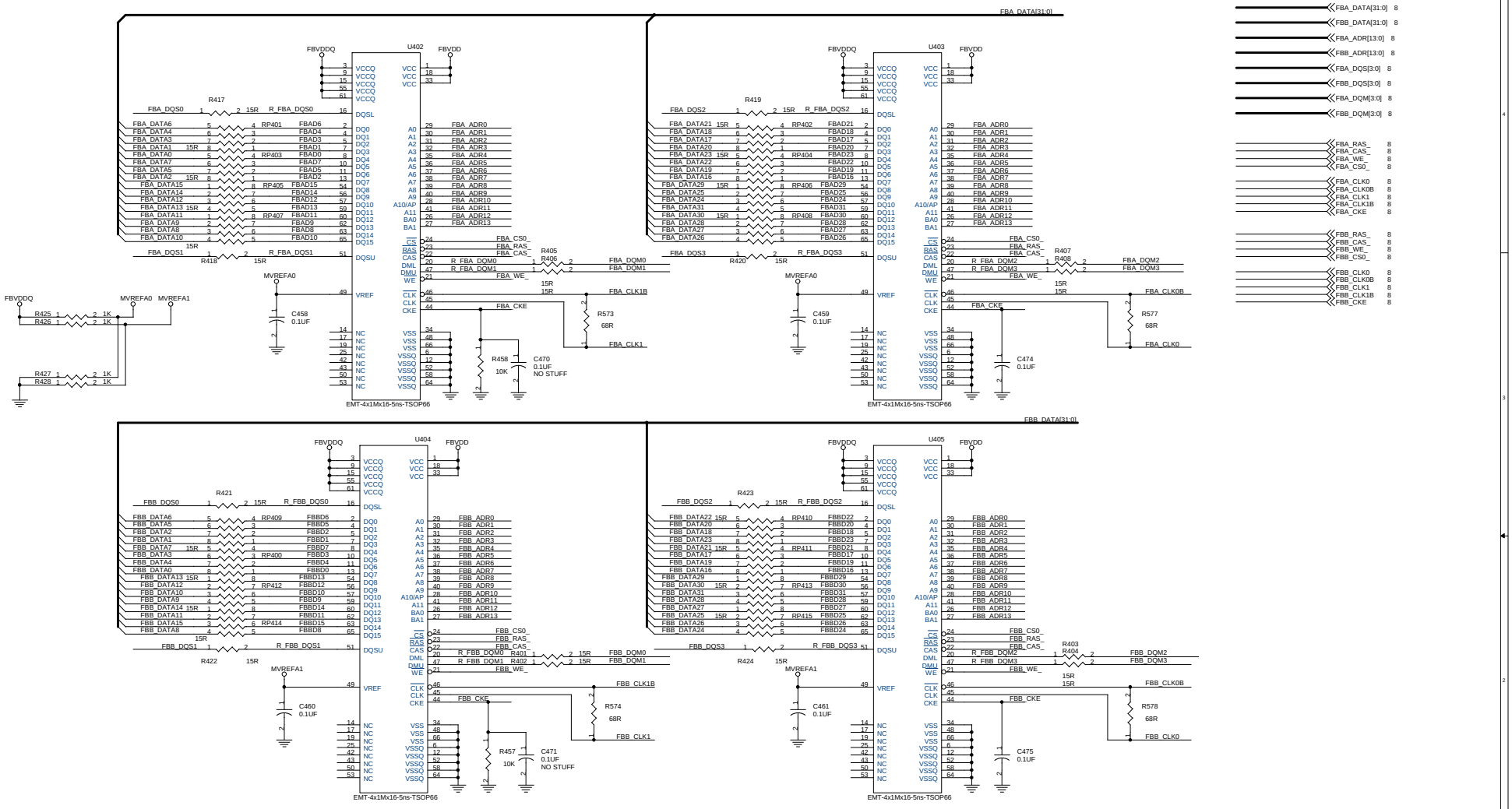

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Size: C	Document Number: FBA/B DDR 4MX16 SDRAM	Rev: 0A
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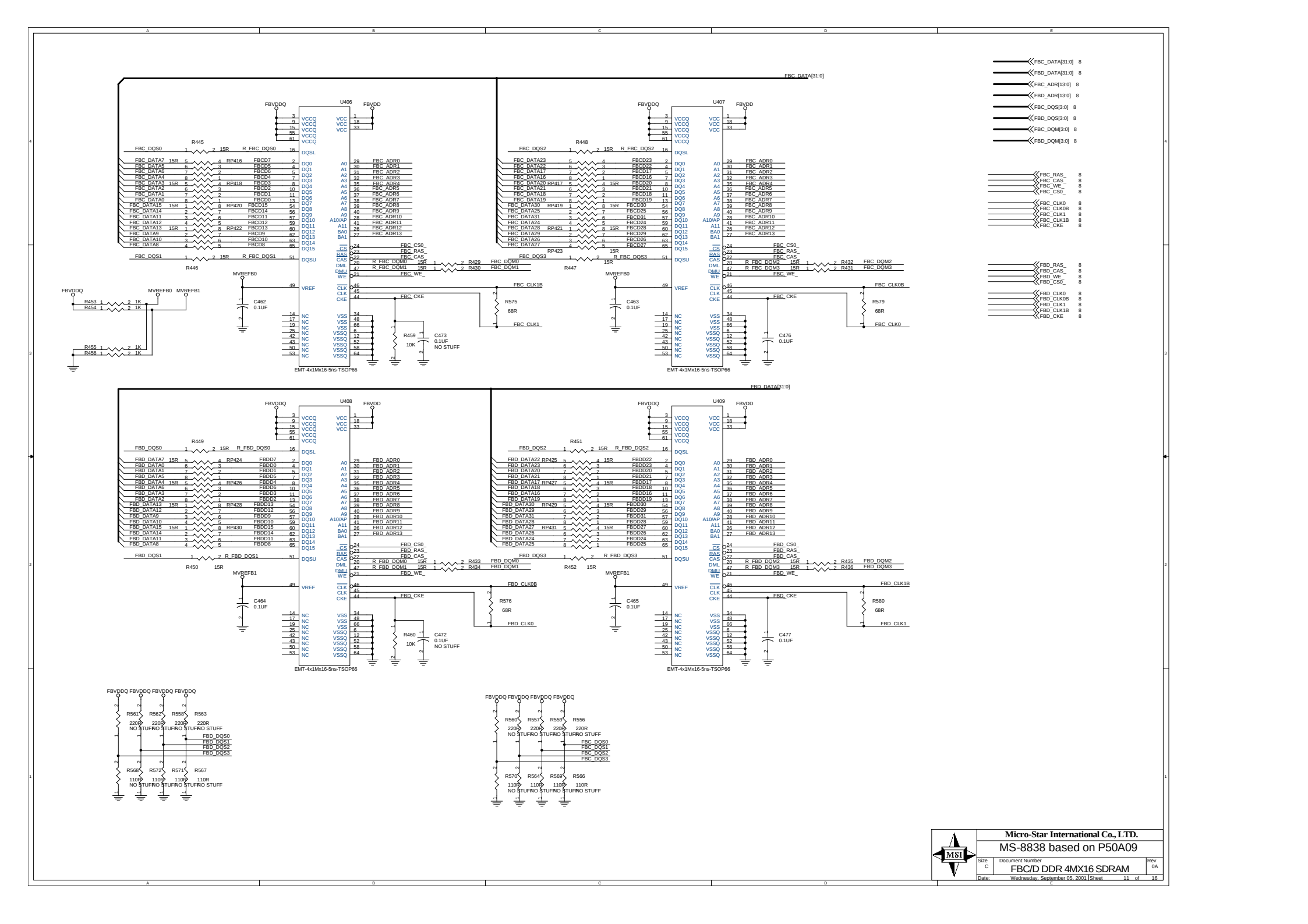

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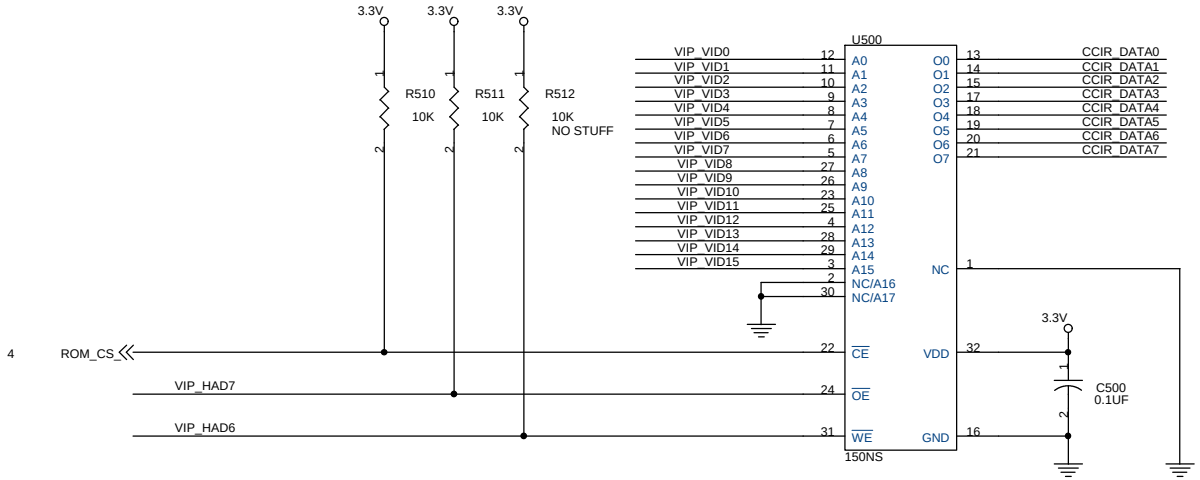
4,6,13 VIP_VID[15:0]
4,13 VIP_PCLK
4 VIP_HCLK
4 VIP_HCTL
4 VIP_HAD0
4 VIP_HAD1
4 VIP_HAD2
4,6 VIP_HAD3
4 VIP_HAD4
4 VIP_HAD5
4 VIP_HAD6
4 VIP_HAD7
4,6,13 CCIR_DATA[11:0]
4,13 CCIR_HSYNC
4,13 CCIR_VSYNC
4,13 CCIR_CLK_IN
4,13 R_CCIR_CLK_OUT
4,13 BUFFRST_
4,13 SCL
4,13 SDA



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Size B	Document Number ROM VIP & VIDEO IF	Rev 0A
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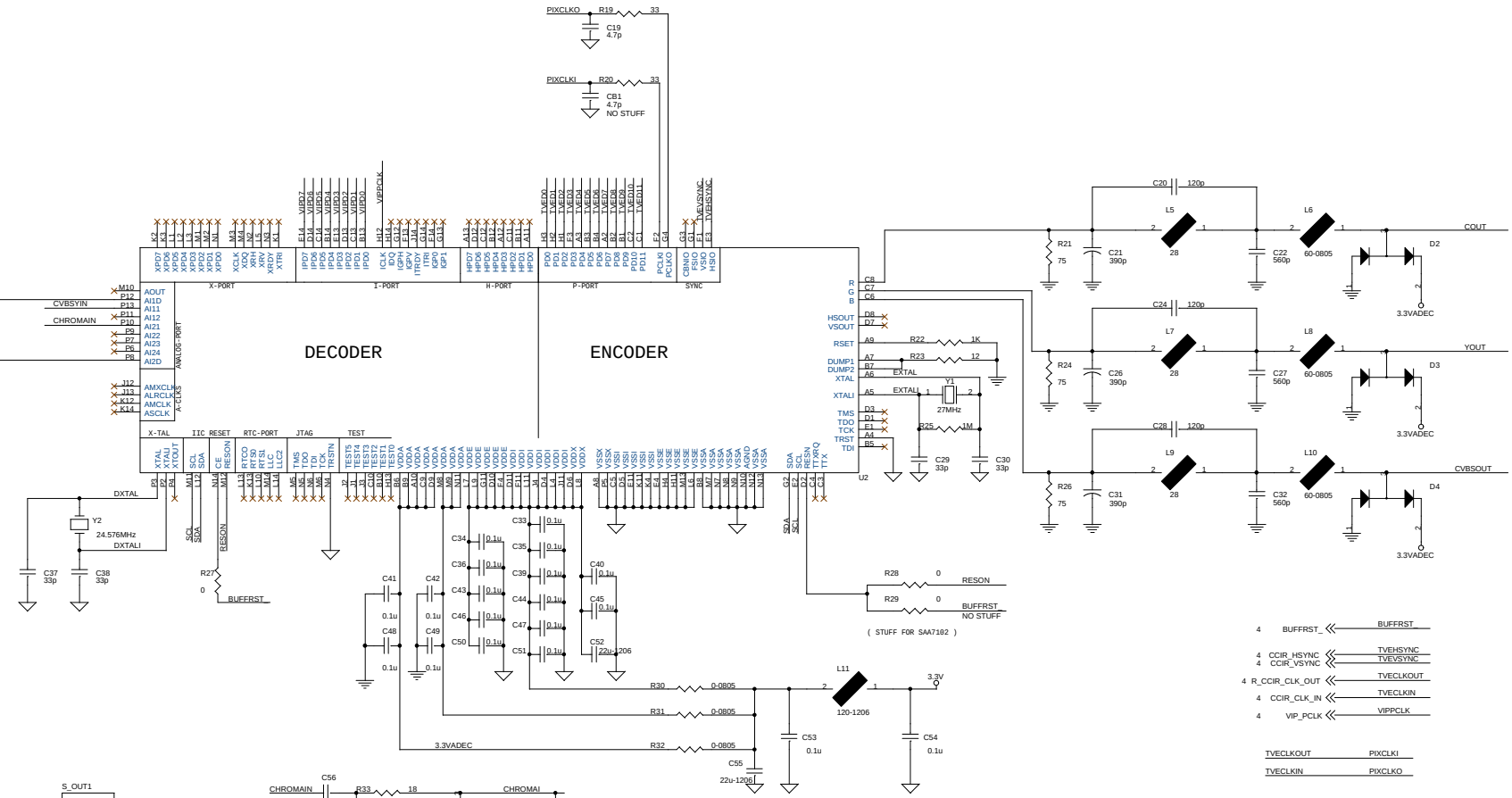

1.EXTAL,EXTALI,DXTAL AND DXTALI NETS SHOULD BE 10 mils width.

R98 and R99 closer to U2

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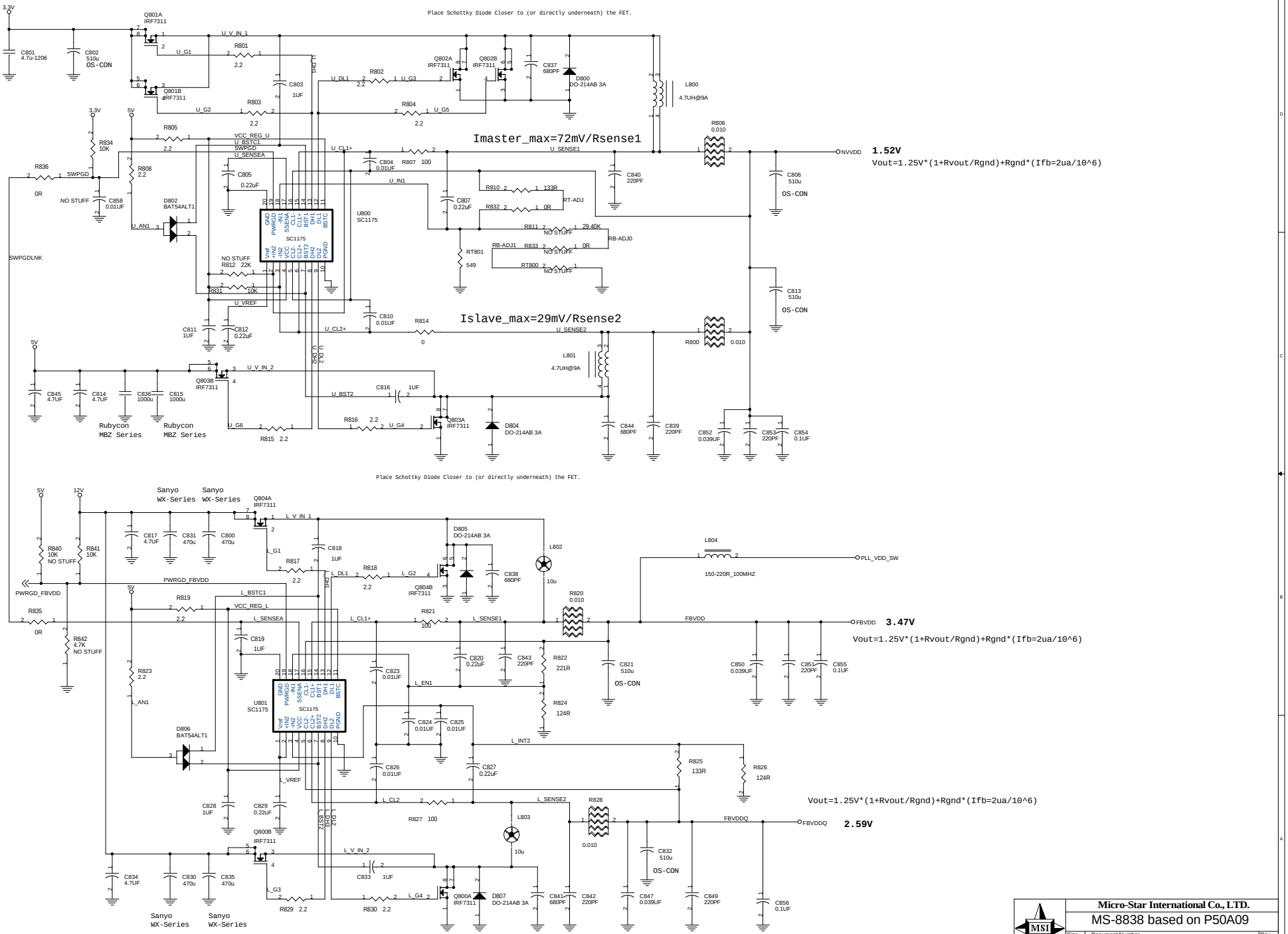

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