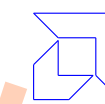


TABLE OF CONTENTS

[illegible]

GROUP NAME DESCRIPTION	
COMMON NORM DNI INT GPU BK HS BACO SUBBOM	INSTALLED IN MAIN BOM NO FN, WON'T BE IN BOM DON'T INSTALL INTERNAL BOM, WON'T BE IN PRODUCTION BOM GPU FN BRACKET HEATSINK OR FANSINK BACO circuit SUBBOM FN
2ND SOURCE	
ALT	ALTERNATIVE FN (FORMAT: ALT=ALT (PN1; PN2; ...))
SUB BOM MEM DEBUG	MEMORY SUB BOM DEBUG SUB BOM
POWER SUB BOM VDDC VDDCI WDDO 095 1V8	VDDC SUB BOM VDDCI SUB BOM WDDO SUB BOM 0.95V SUB BOM 1.8V SUB BOM

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SHEET: TOC

DATE: Fri Aug 30 17:24:57 2013

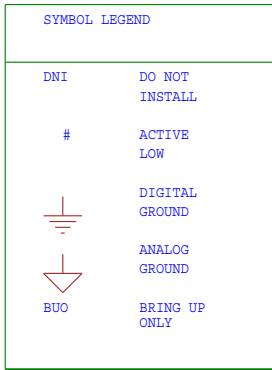
REV: 3.00

SHEET NUMBER: 1 OF 22

DOCUMENT NUMBER: 105-C870xx-00C

NOTES: NOTE

TITLE:	Samoa Pro S3 DDR3 DVI+HDMI/DP 35W(Board)
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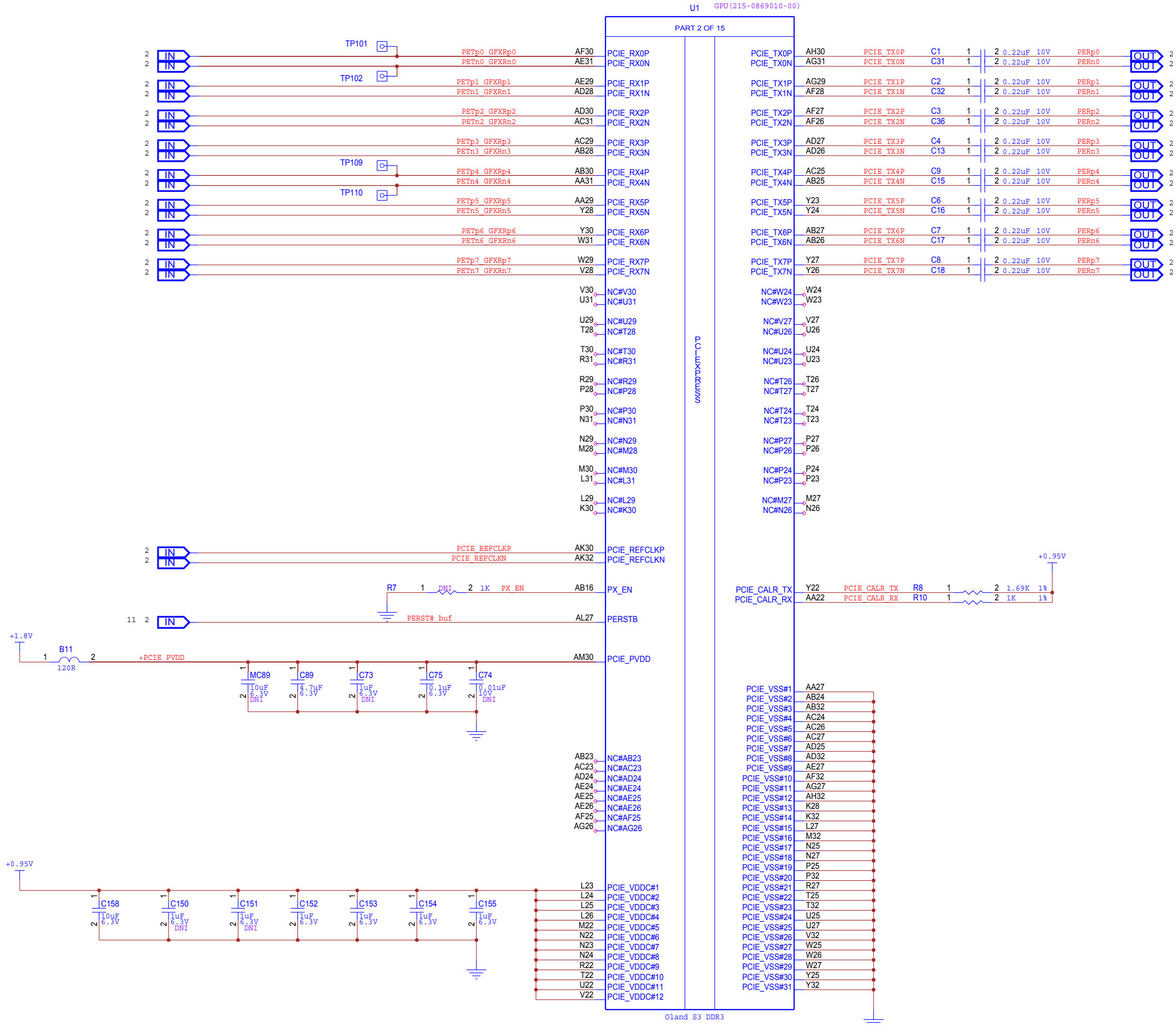


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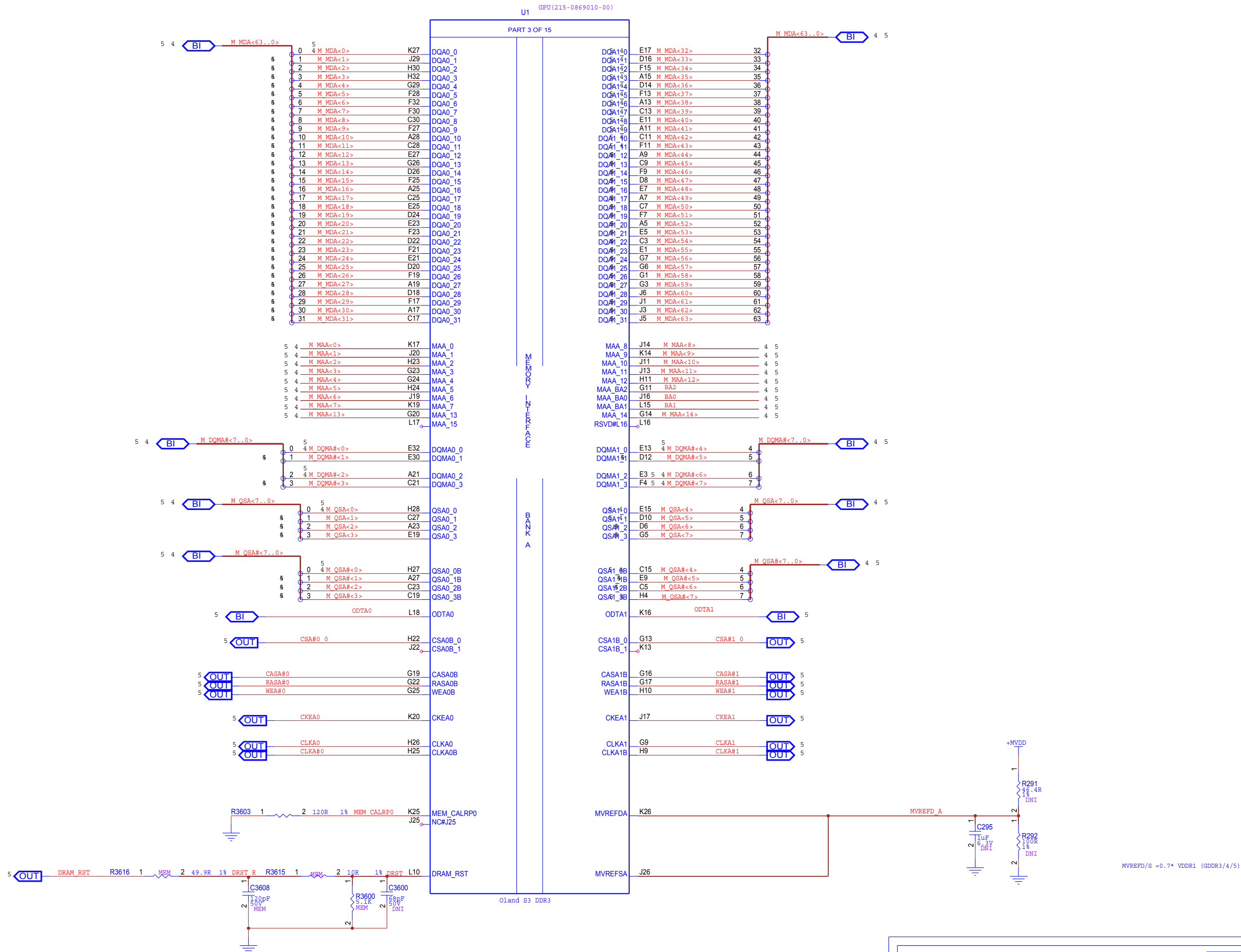
TITLE:
Samoa Pro S3 DDR3 DVI+HDMI/DP 35W(Board)

OLAND PCIe Interface

NOTE: Some of the PCIe testpoints will be available through vias on traces.



Oland S3 MEM Interface Ch A&B



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SHEET: Samoa MEM I/F CHA

DATE: Wed Oct 29 14:46:54 2014

REV: 3.00

SHEET NUMBER: <CURRENT DESIGN>SHEET>DESIGN_SHEETS>

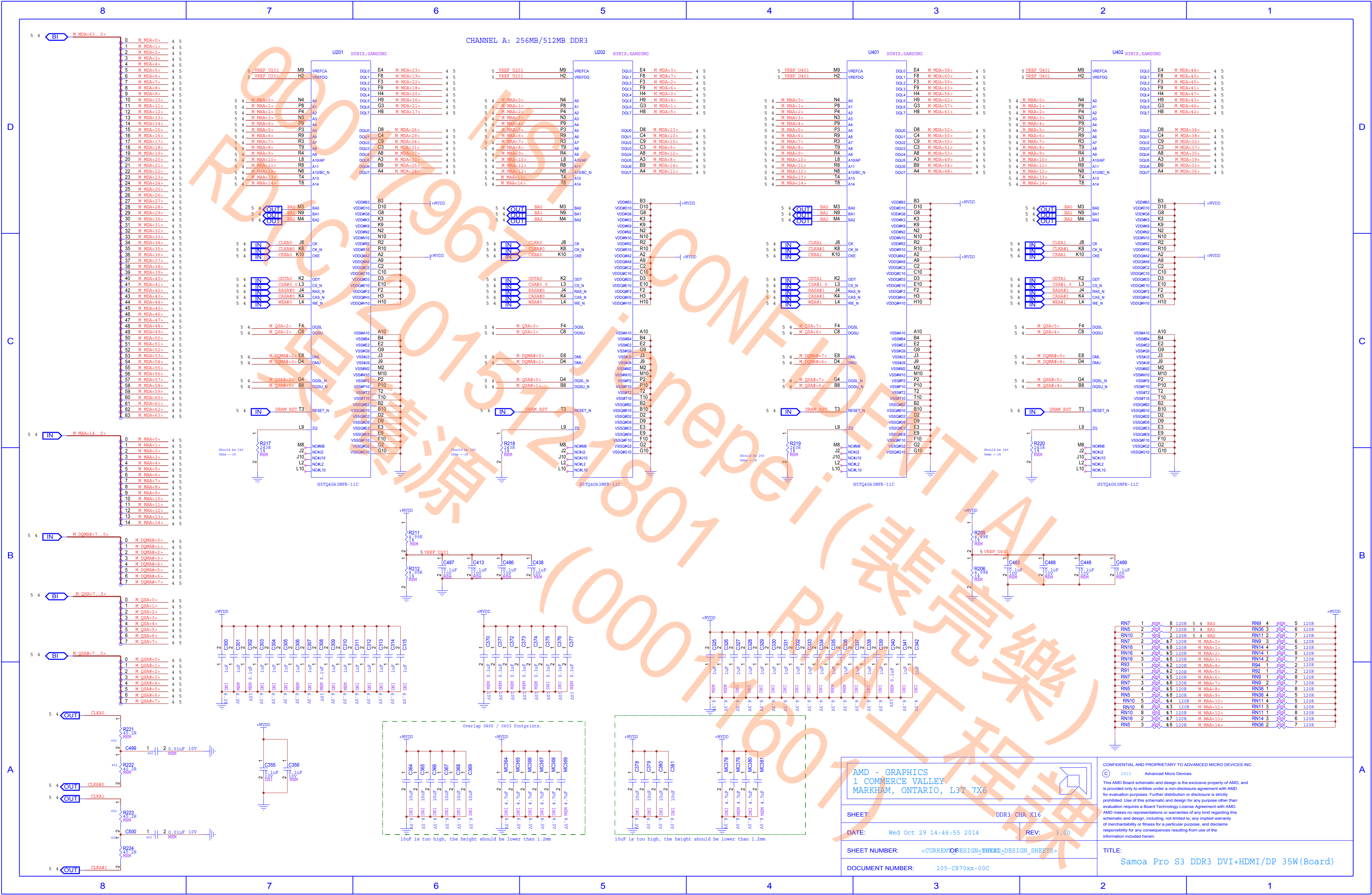
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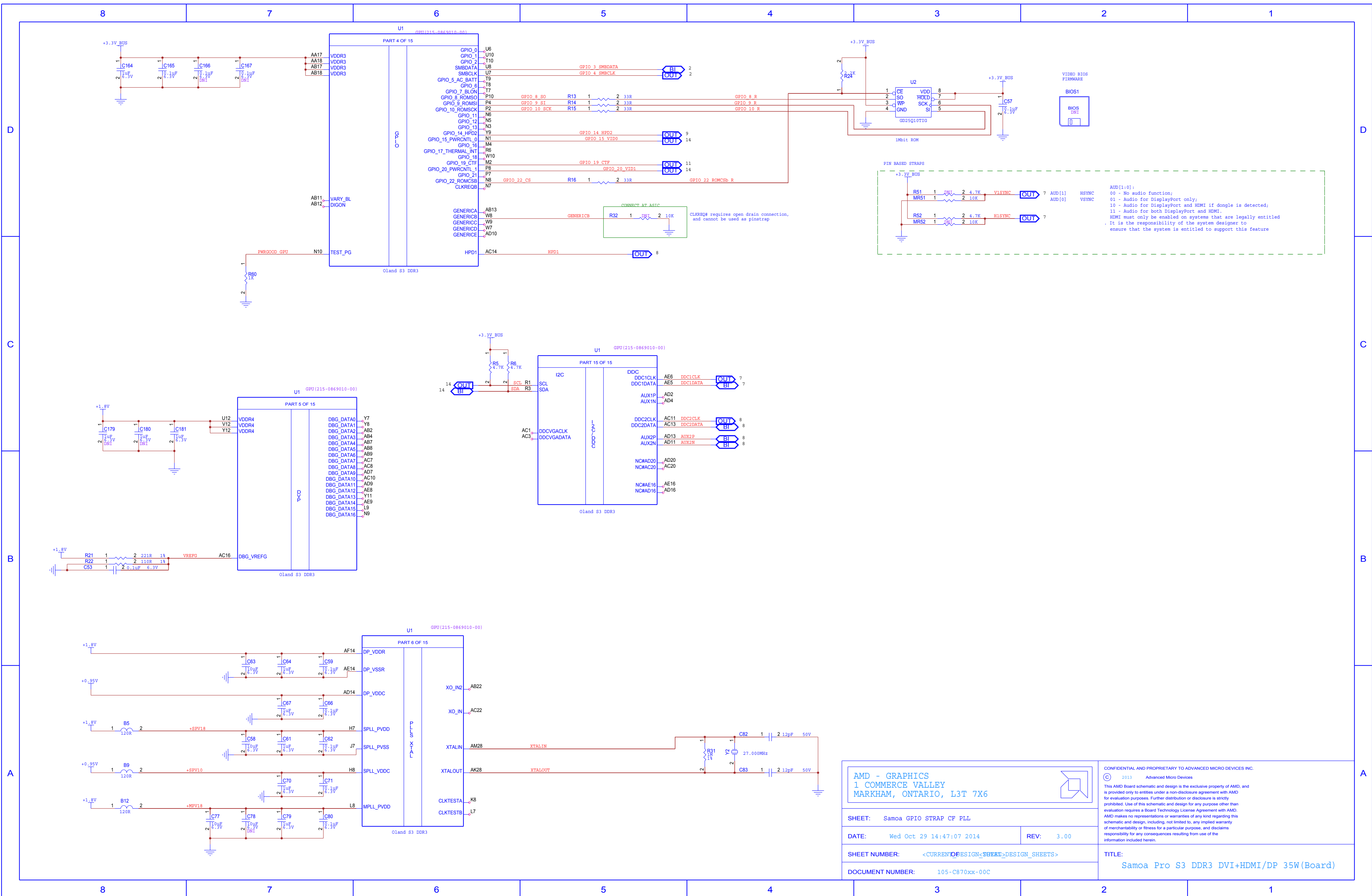
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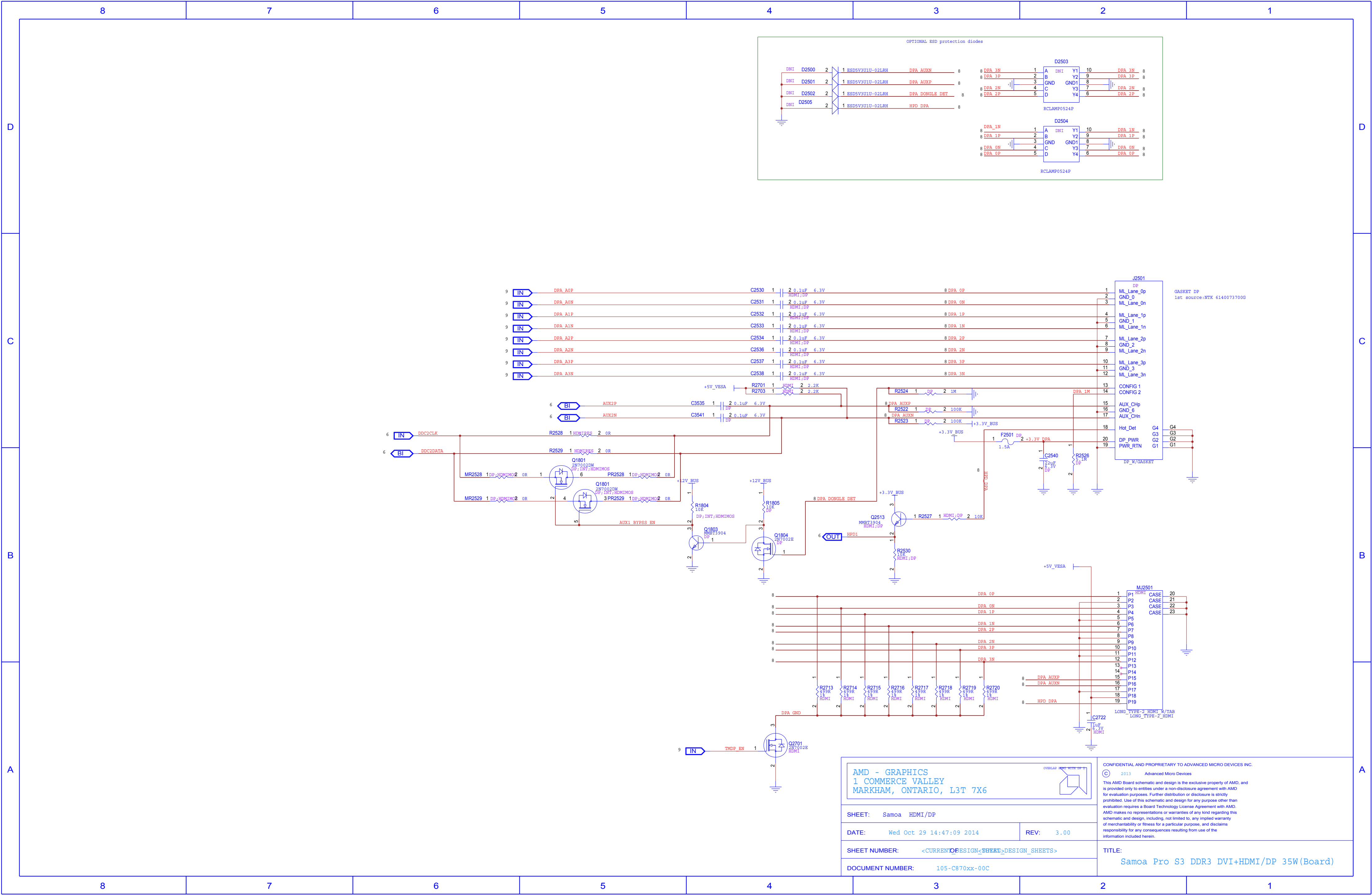
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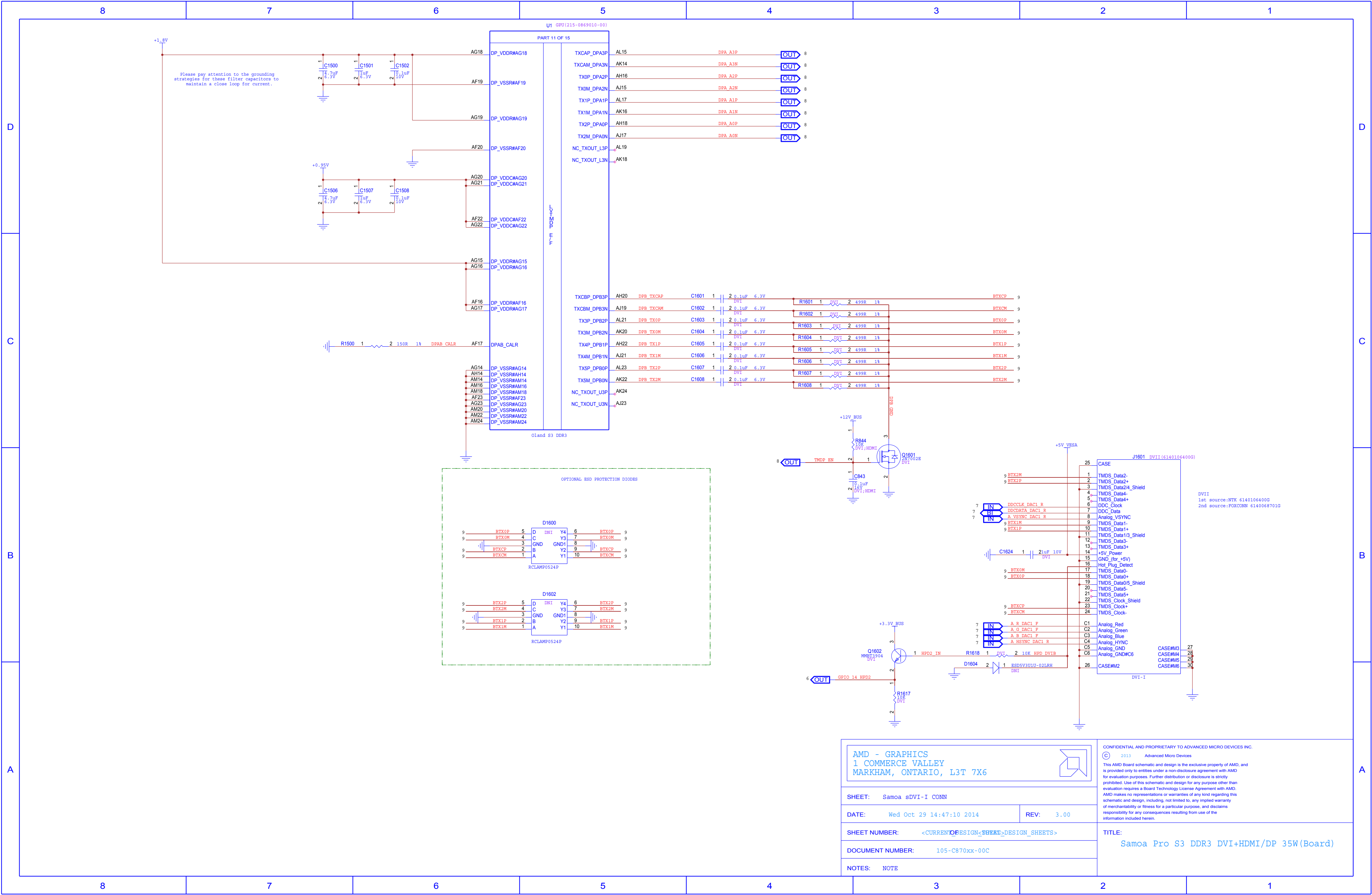
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Samoa Pro S3 DDR3 DVI+HDMI/DP 35W(Board)







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SHEET: Samoa HDMI/DP		TITLE: Samoa Pro S3 DDR3 DVI+HDMI/DP 35W (Board)	
DATE: Wed Oct 29 14:47:09 2014		REV: 3.00	
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DOCUMENT NUMBER: 105-C870xx-00C			



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SHEET: Samoa sDVI-I CONN

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DOCUMENT NUMBER: 105-C870xx-00C

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REV: 3.00

TITLE: Samoa Pro S3 DDR3 DVI+HDMI/DP 35W(Board)

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D



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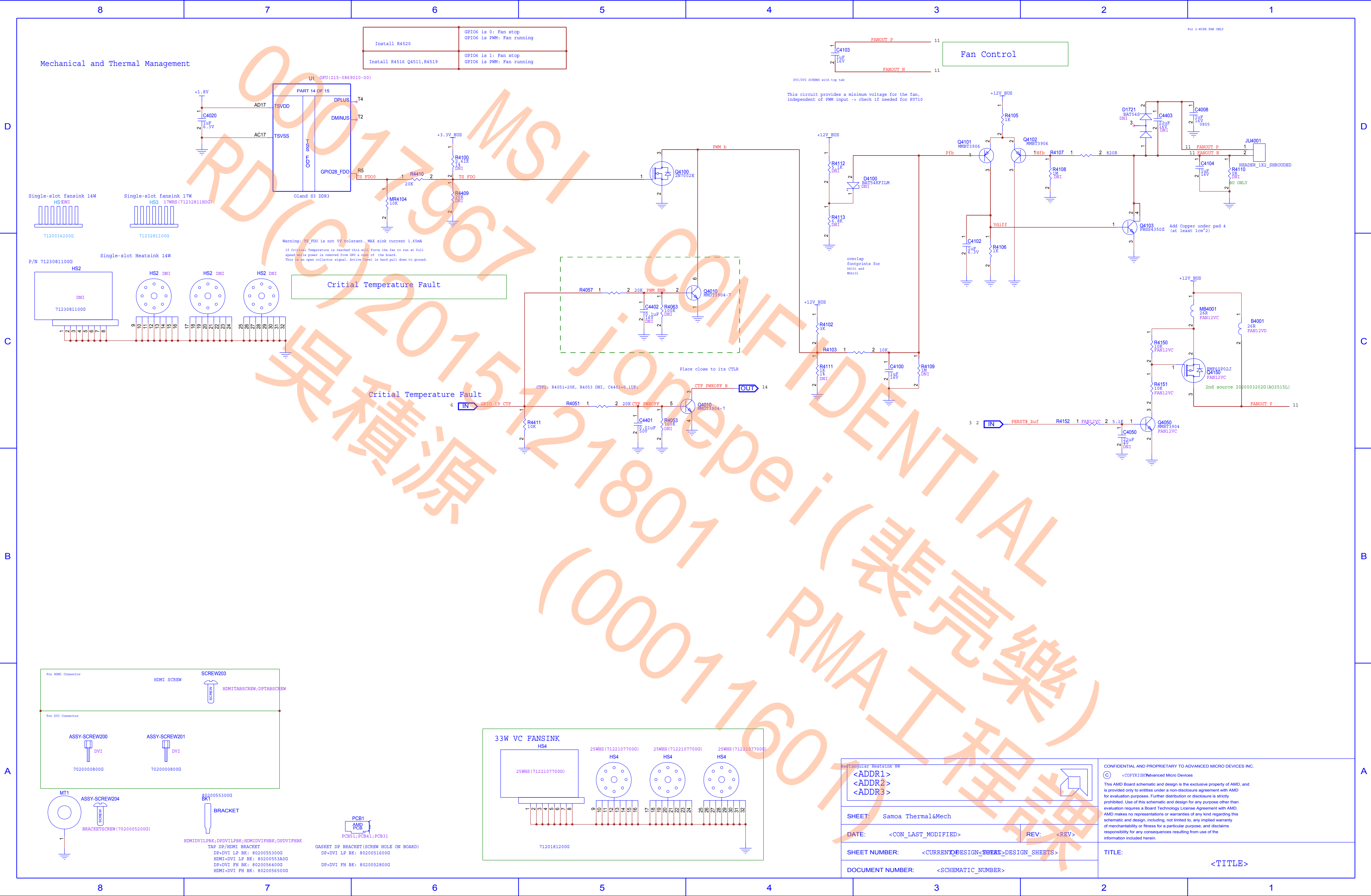
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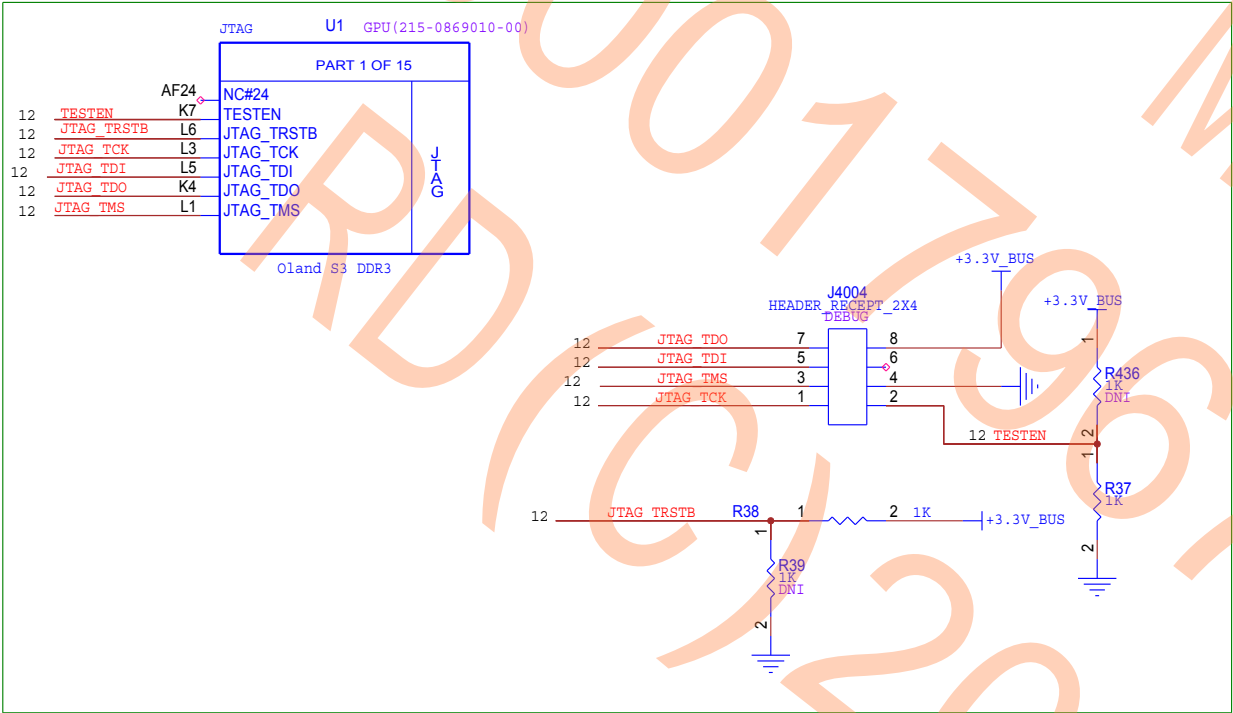
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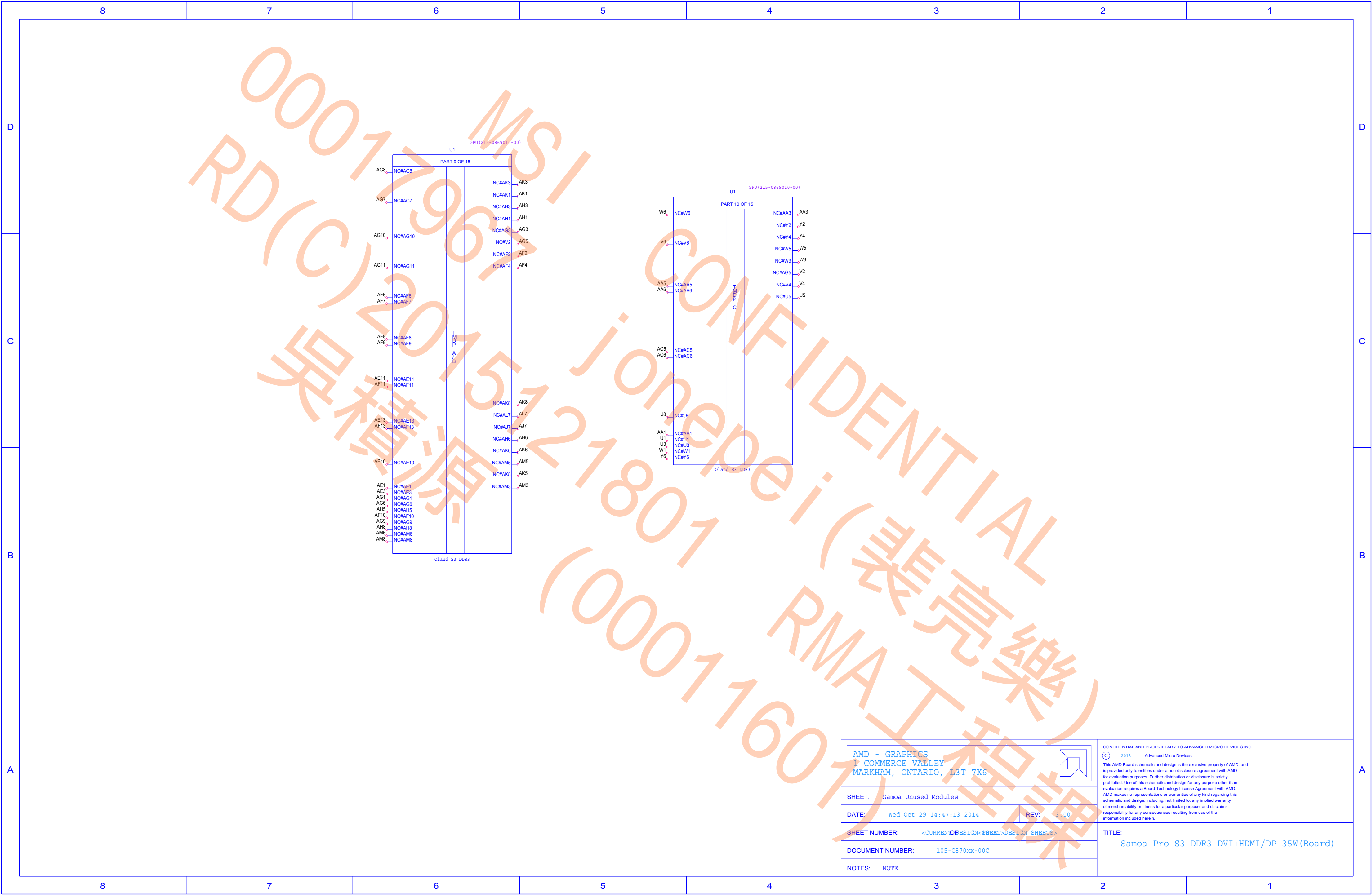
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


(19) Debug Circuits



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DOCUMENT NUMBER: 105-C870xx-00C		TITLE: Samoa Pro S3 DDR3 DVI+HDMI/DP 35W(Board)



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DOCUMENT NUMBER: 105-C870xx-00C		Samoa Pro S3 DDR3 DVI+HDMI/DP 35W (Board)
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DOCUMENT NUMBER: 105-C870xx-00C

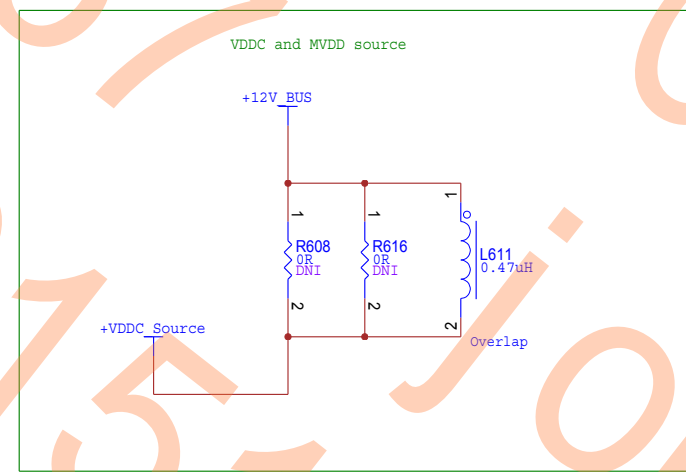
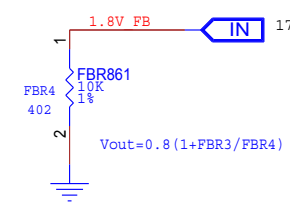
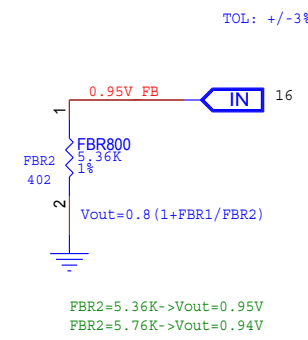
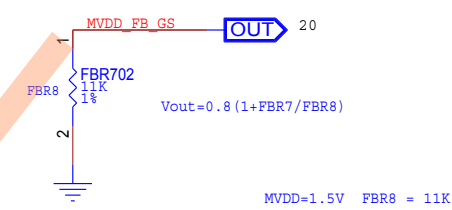
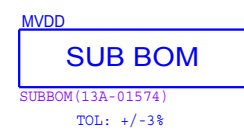
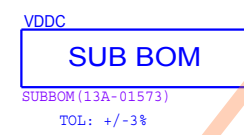
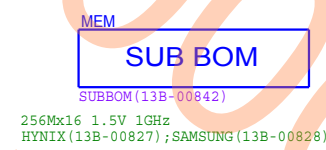
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
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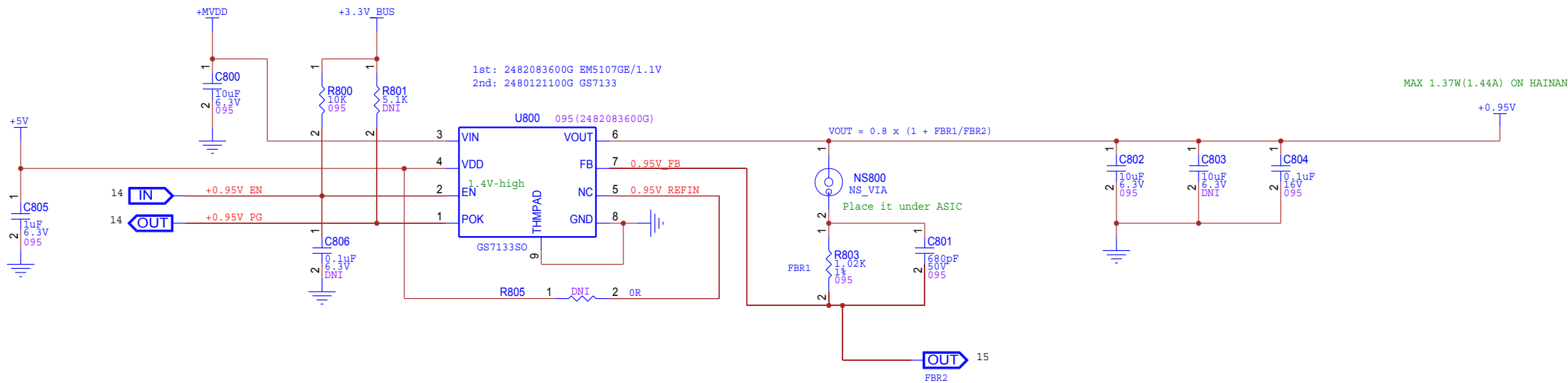


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<div>DOCUMENT NUMBER: 105-C870xx-00C</div>			
<div>NOTES: NOTE</div>			

Linear Regulators

LDO #1: Vin = +1.5V +/-2% Vout = +0.95V +/- 2%; Iout = 1.44A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

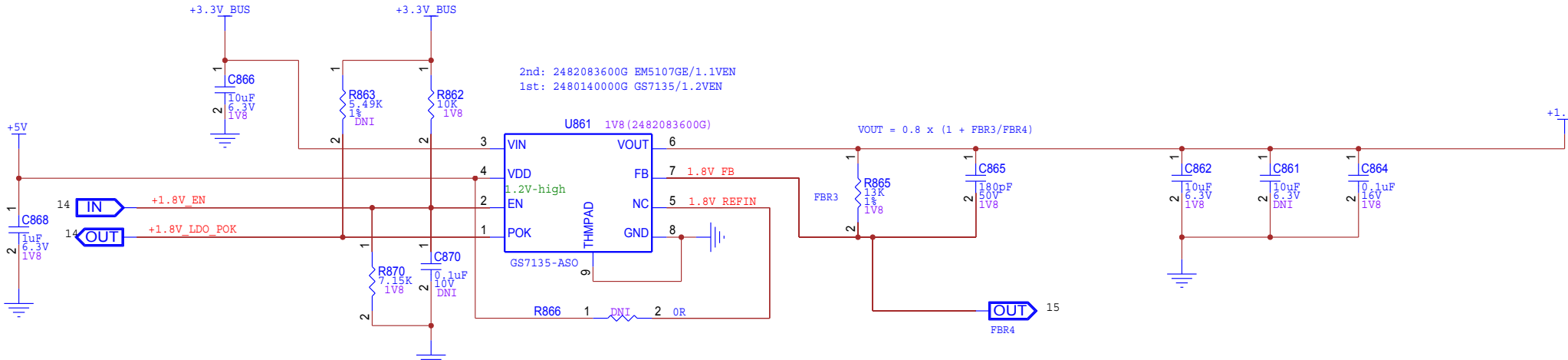


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DOCUMENT NUMBER: 105-C870xx-00C			
NOTES: NOTE			

Linear Regulators

LDO #2: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



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SHEET: 1.8V

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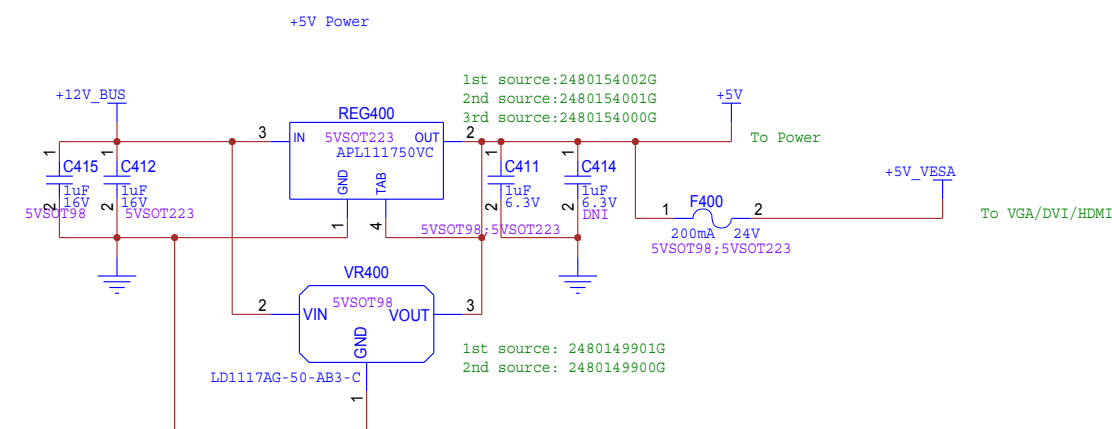
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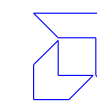
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Samoa Pro S3 DDR3 DVI+HDMI/DP 35W(Board)



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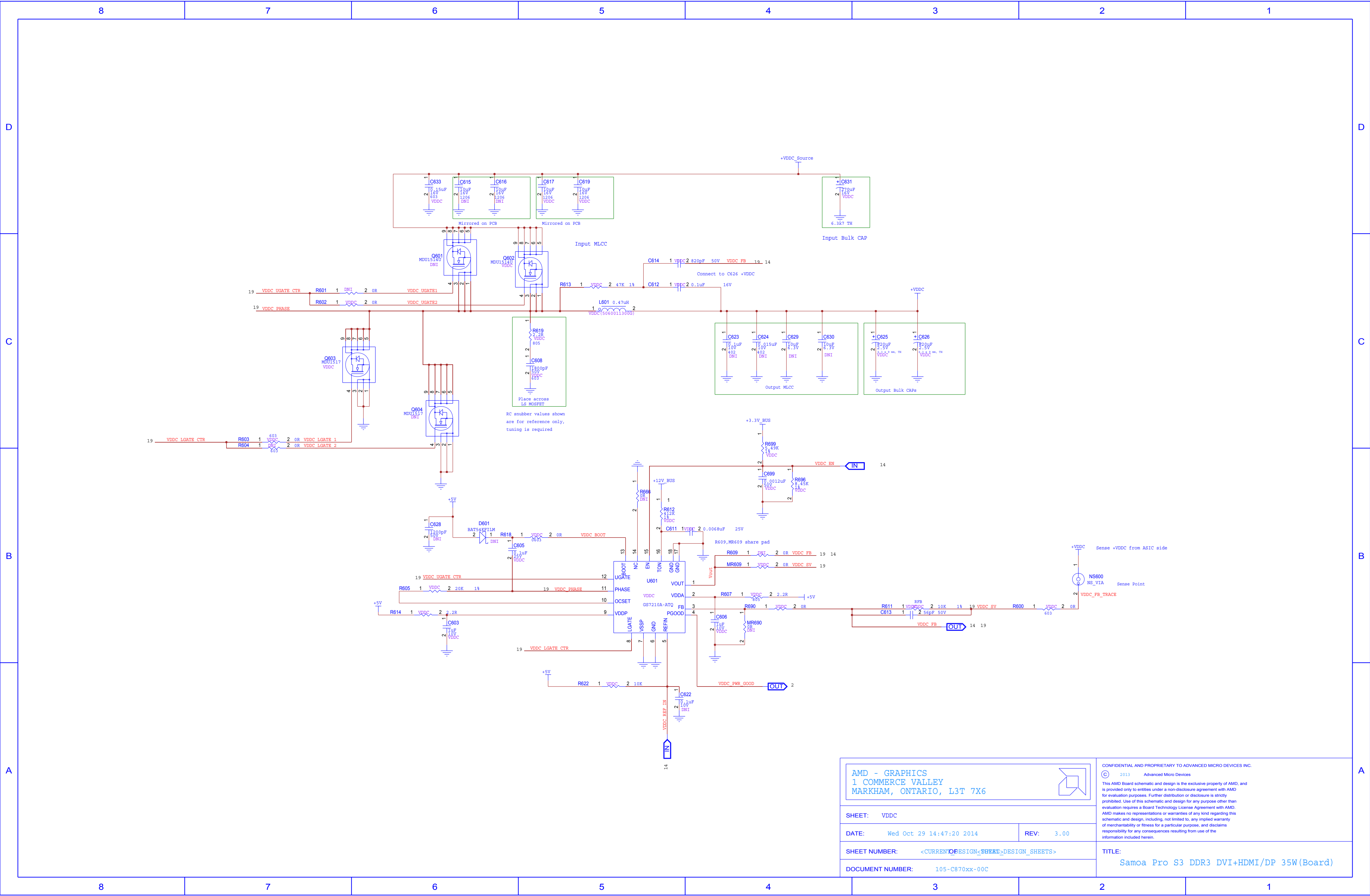
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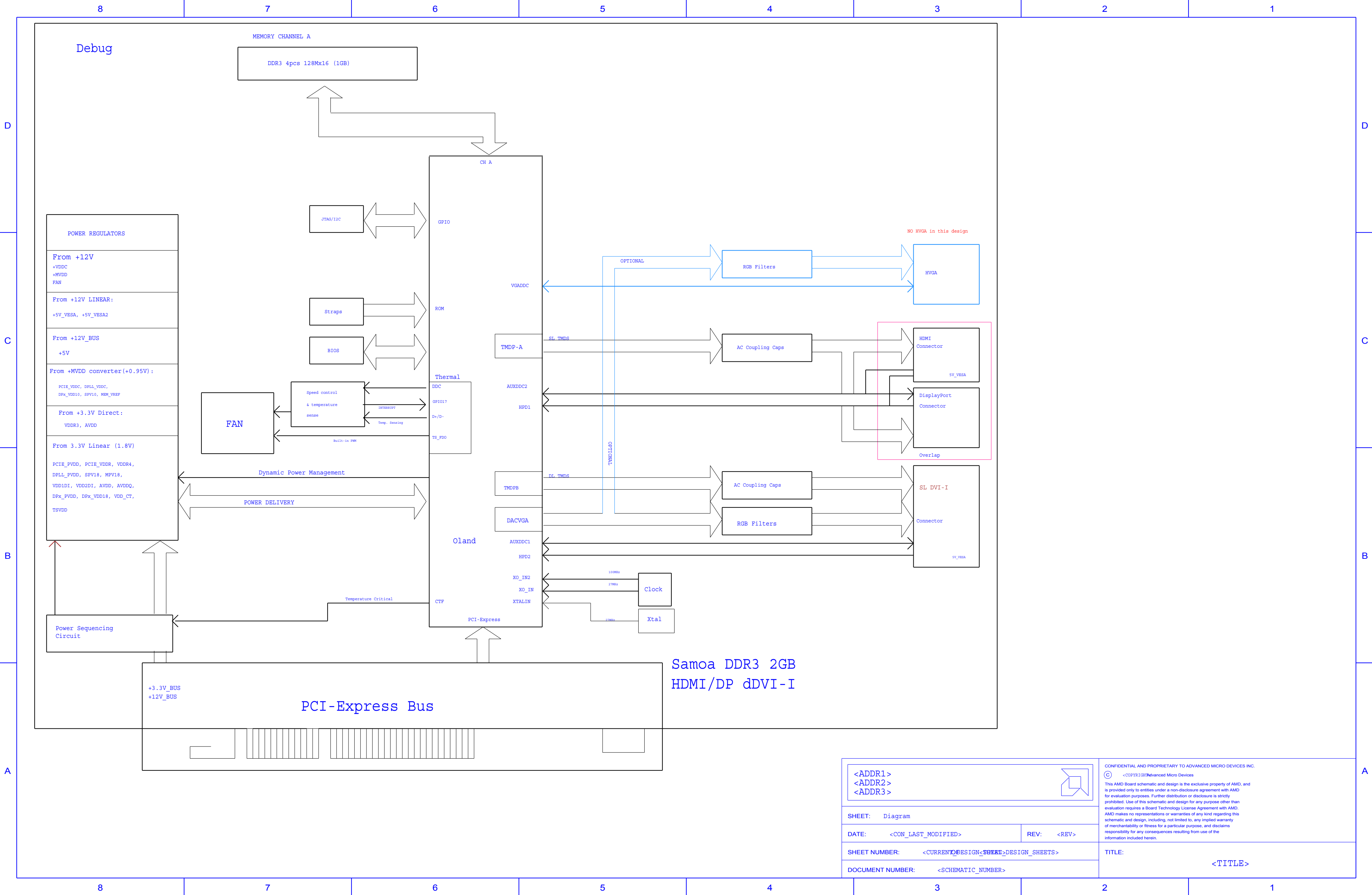
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
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TITLE: Samoa Pro S3 DDR3 DVI+HDMI/DP 35W(Board)





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<div>AMD</div>			TITLE: Samoa Pro S3 DDR3 DVI+HDMI/DP 35W(Board)						DOCUMENT NUMBER: 105-C870xx-00C			DATE: Wed Oct 29 14:47:21 2014			SHEET NUMBER: <CURRENTDESIGN<SHEET>DESIGN_SHEETS>			REV: 3.00					
REVISION HISTORY						ENGINEER: Tony Yang			NOTES: NOTE			CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. C © 2013 Advanced Micro Devices This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.						AMD - GRAPHICS 1 COMMERCE VALLEY MARKHAM, ONTARIO, L3T 7X6					
SCH Rev			PCB Rev			Date			REVISION DESCRIPTON														
1.00			00A			04/15/14			1. Initial release														
1.01			00A			06/13/14			2. calculate the VDDC Feedback value based on the latest BB														
2.00			00B			07/09/14			3. Add FAN 12 Control circuit to fix acoustic issue(P11)														
						07/15/14			4. Change 5V solution(P18)														
						07/18/14			5. Add SOT89 LDO for backup(P18)														
						07/25/14			6. Change DVI connect														
						08/11/14			7. ADD more VDDC decoupling caps														
2.01						08/13/14			8. Change VDDC FB resistors:R650 30K, R671 37.4K, R676 22K														
3.00			00C			10/27/14			9. Update MPLS value														
									10.Add MT1 for bracket lock														
									11.Change PCIe RST Power input, Add Q851,R851,R849														
8			7			6			5			4			3			2			1		