MS-V005 VER 10

ATI-PCIEXPRESS RV410 BGA 8MX32 DDRIII, VGA, SCART(VIA VT1623M), TV-OUT,DVI

COVER	1
BLOCK	2
PCI-EXPRESS CONNECTOR	3
RV410 PCIE_INTERFACE	4
RV410_MAIN	5
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RV410 GND	7
REGULATOR FOR GPU,MEMORY AND OTHERS	8-10
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VIA-VT1623M	18

CORE	425
MEMORY	430

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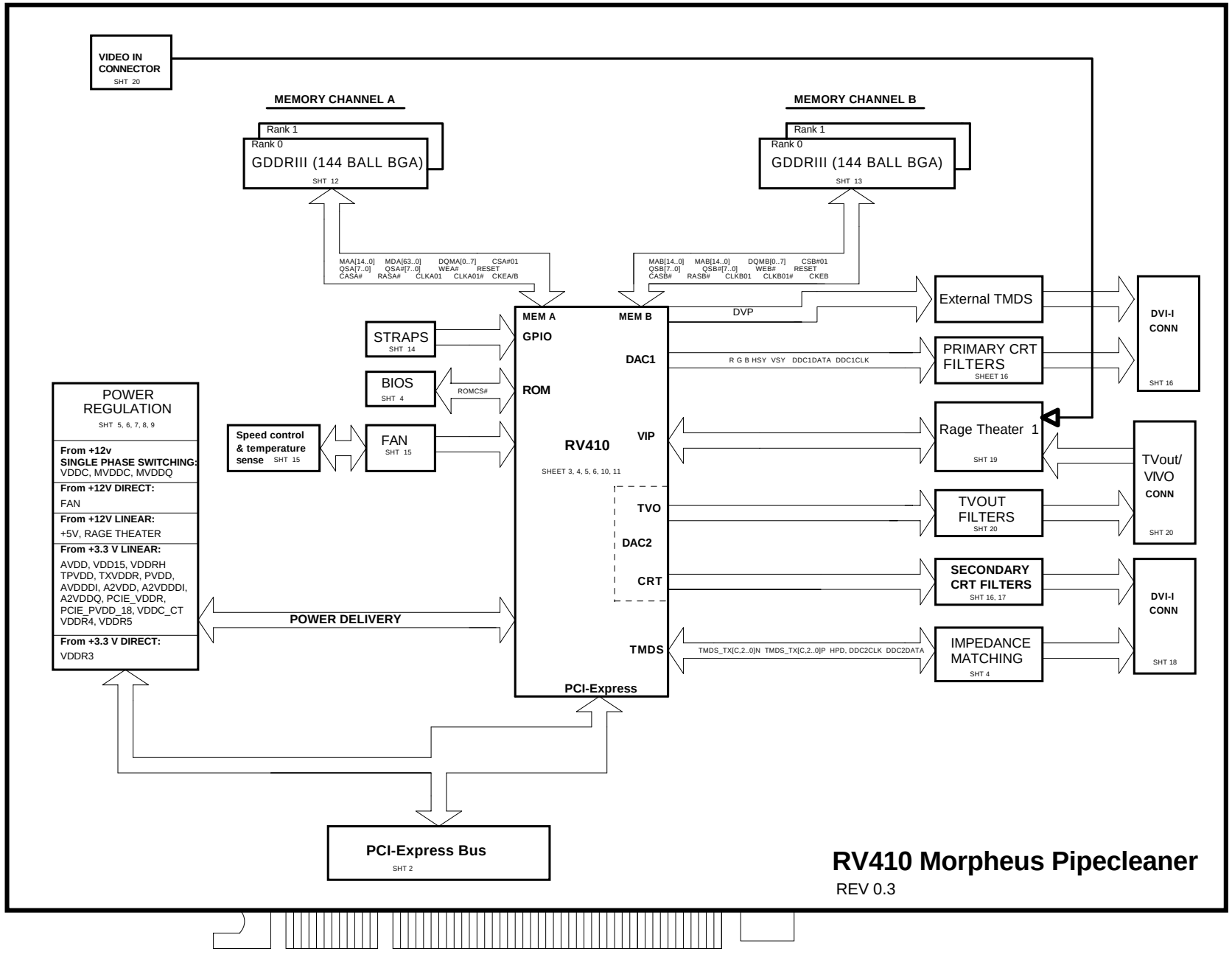

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Size C	Document Number: RV410 Block_Diagram	Rev 10
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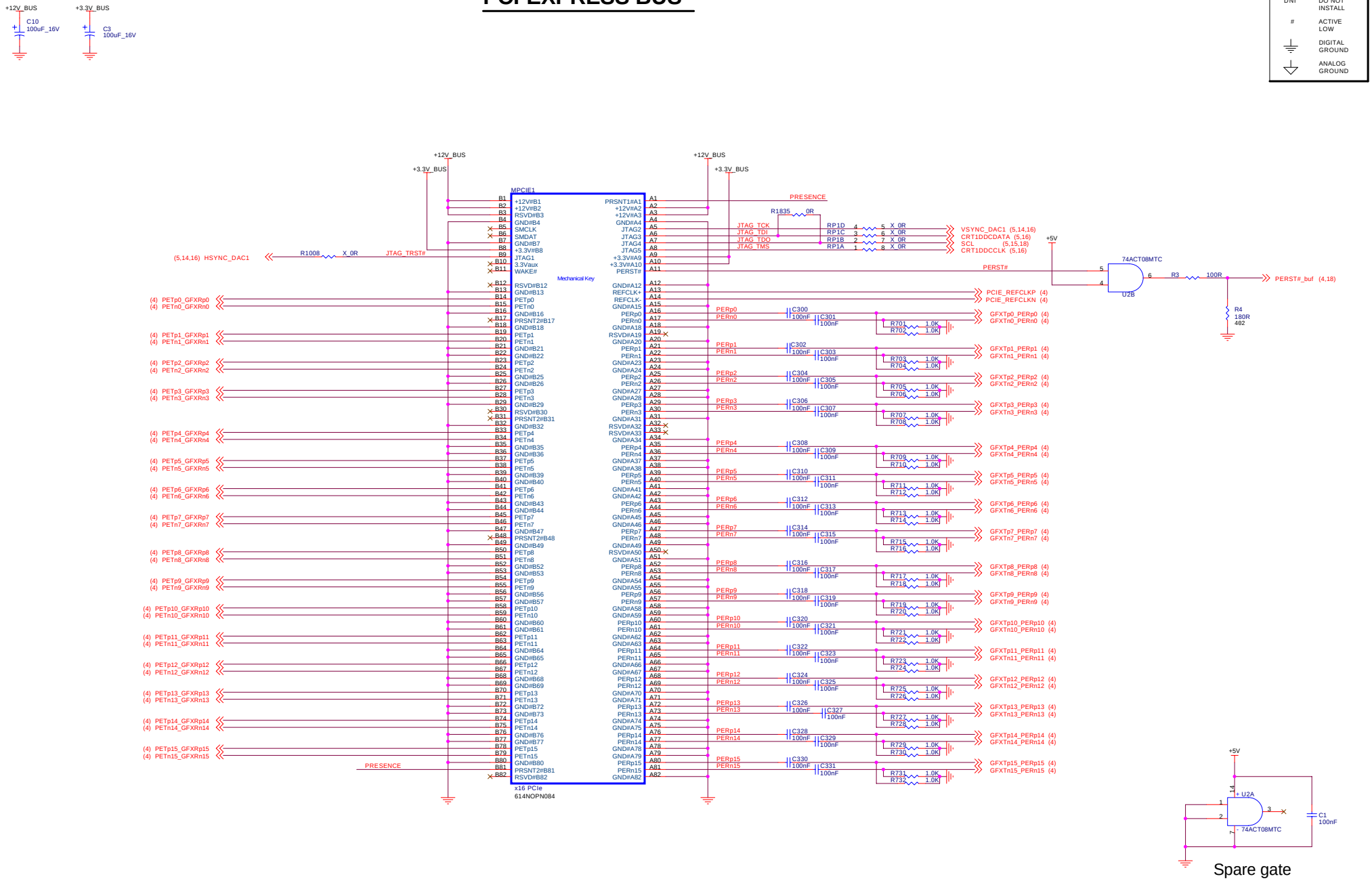
PCI-EXPRESS BUS



MS-V005 ATI RV410			
Size C	Document Number PCI-Express_Connector		Rev 10
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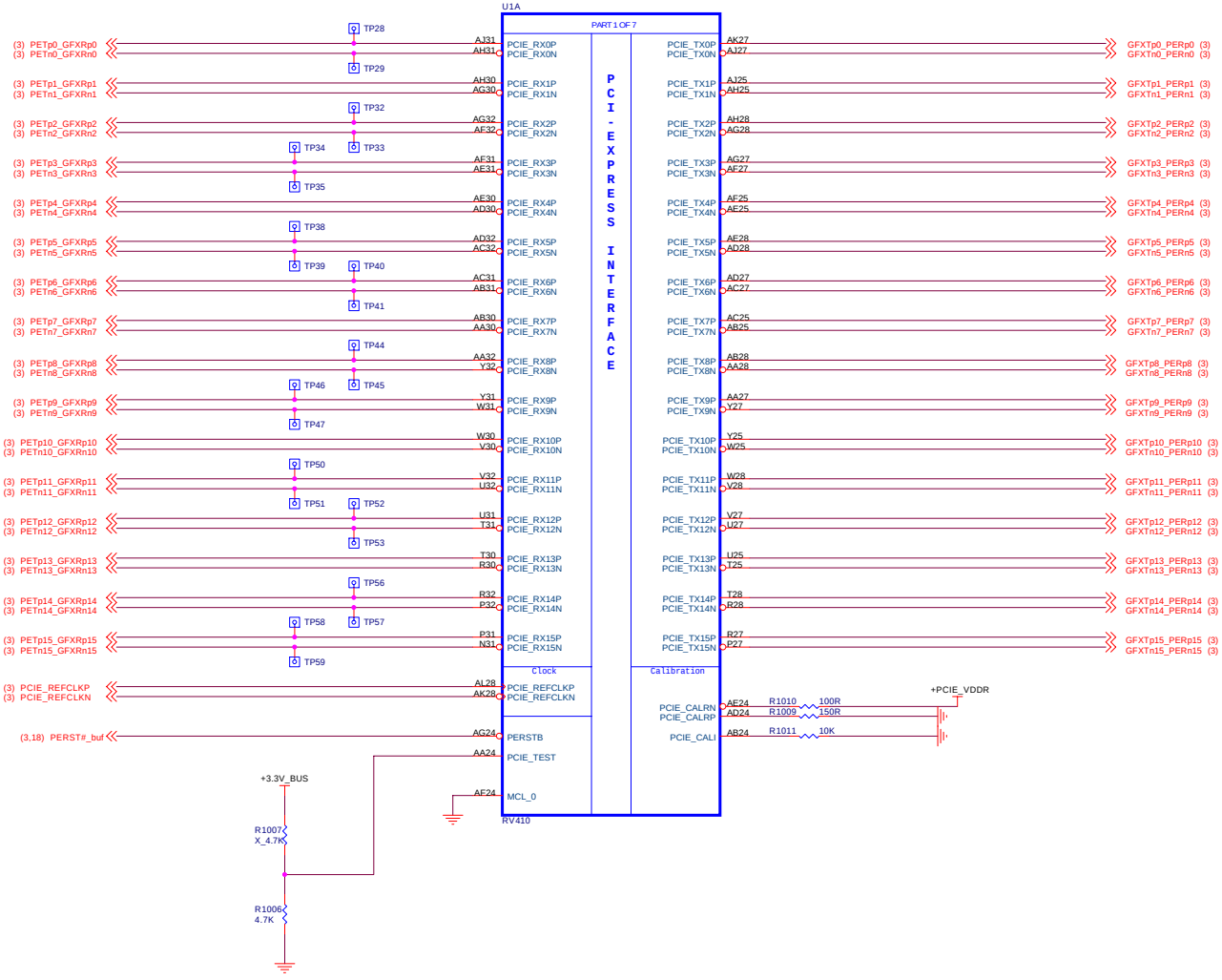
NOTE: some of the PCIE testpoints will
be available trought via on traces.



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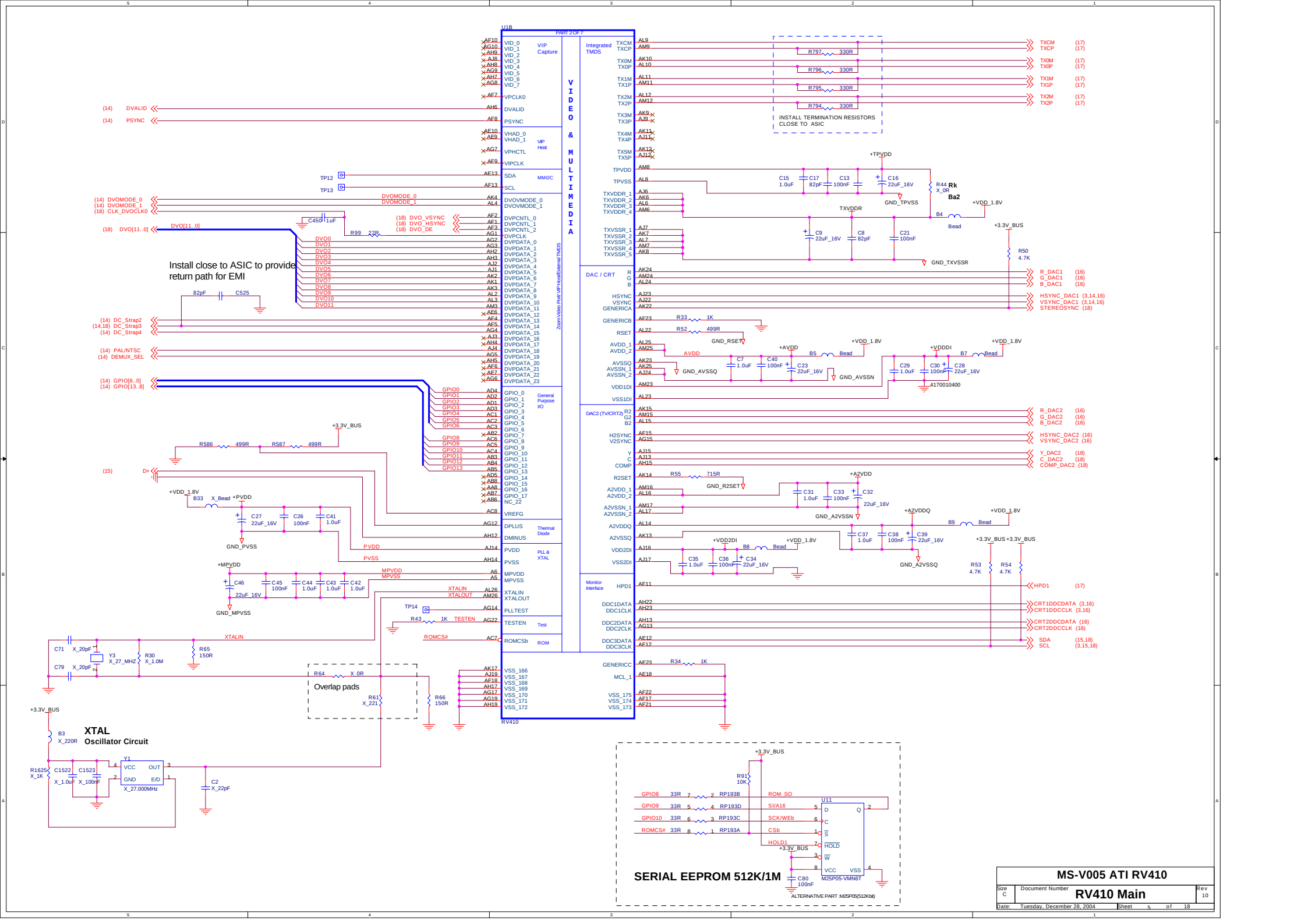
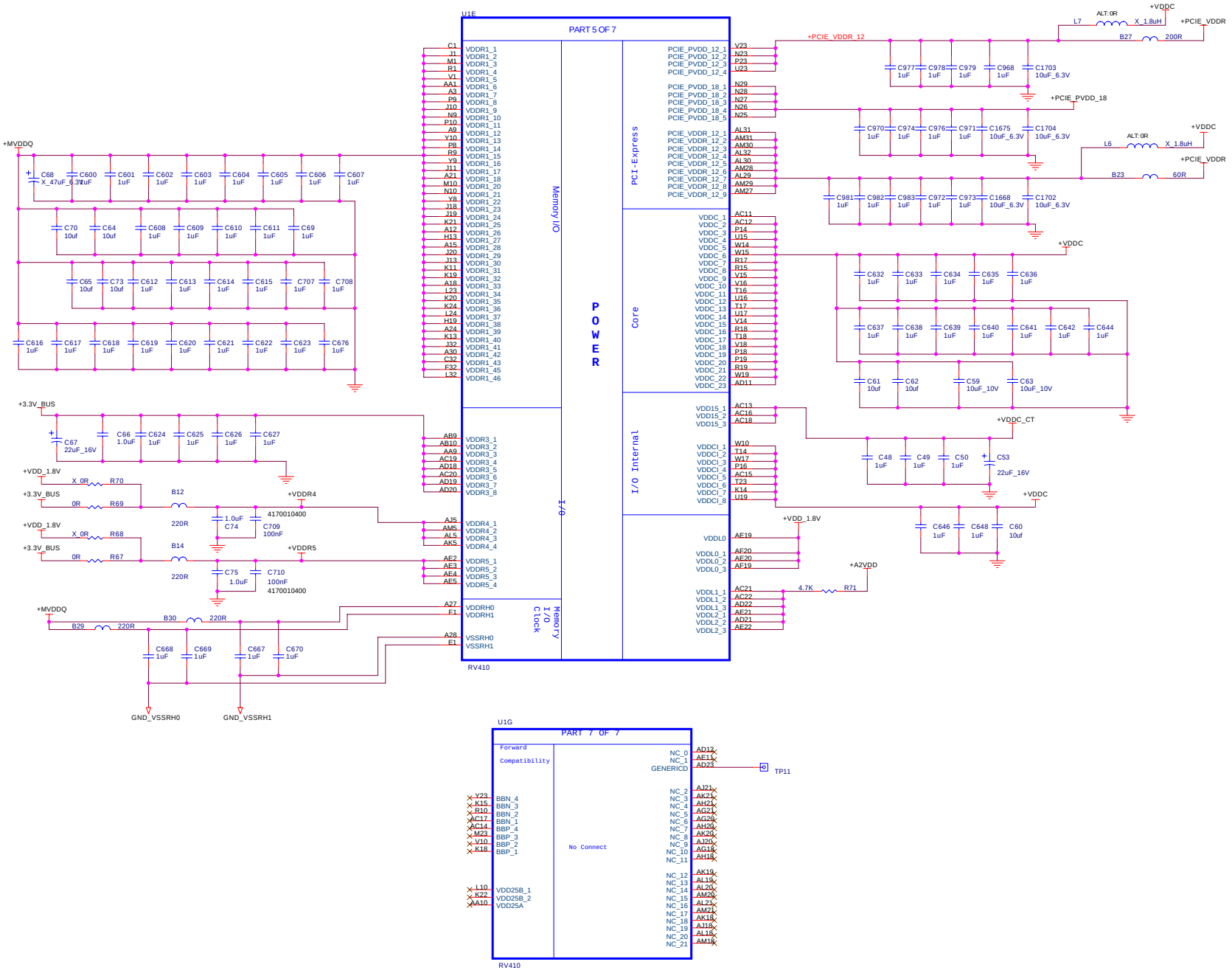

U1B
PART 2 OF 7
VIDEO & MULTIMEDIA
VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
VID_7
VIP Capture
VPCLK0
DVALID
PSYNC
VHAD_0
VHAD_1
VIP Host
VPHCTL
VIPCLK
SDA
SCL
MMI2C
DVOMODE_0
DVOMODE_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
Zoom/Video Port/ VIP Host/External TMDS
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_15
GPIO_16
GPIO_17
NC_22
General Purpose I/O
VREFG
DPLUS
DMINUS
Thermal Diode
PVDD
PVSS
PLL & XTAL
MPVDD
MPVSS
XTALIN
XTALOUT
PLLTEST
TESTEN
Test
ROMCSb
ROM
VSS_166
VSS_167
VSS_168
VSS_169
VSS_170
VSS_171
VSS_172
RV410
Integrated TMDS
TXCM
TXCP
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TX3M
TX3P
TX4M
TX4P
TX5M
TX5P
TPVDD
TPVSS
TXVDDR_1
TXVDDR_2
TXVDDR_3
TXVDDR_4
TXVSSR_1
TXVSSR_2
TXVSSR_3
TXVSSR_4
TXVSSR_5
DAC / CRT
R
G
B
HSYNC
VSYNC
GENERICA
GENERICB
RSET
AVDD_1
AVDD_2
AVSSQ
AVSSN_1
AVSSN_2
VDD1DI
VSS1DI
DAC2 (TV/CRT2)
R2
G2
B2
H2SYNC
V2SYNC
Y
C
COMP
R2SET
A2VDD_1
A2VDD_2
A2VSSN_1
A2VSSN_2
A2VDDQ
A2VSSQ
VDD2DI
VSS2DI
Monitor Interface
HPD1
DDC1DATA
DDC1CLK
DDC2DATA
DDC2CLK
DDC3DATA
DDC3CLK
GENERICC
MCL_1
VSS_175
VSS_174
VSS_173
INSTALL TERMINATION RESISTORS CLOSE TO ASIC
R797 330R
R796 330R
R795 330R
R794 330R
+TPVDD
C15 1.0uF
C17 82pF
C13 100nF
C16 22uF_16V
R44 Rk X_0R
Ba2
GND_TPVSS
+VDD_1.8V
TXVDDR
B4 Bead
C9 22uF_16V
C8 82pF
C21 100nF
GND_TXVSSR
+3.3V_BUS
R50 4.7K
GND_RSET
AVDD
+AVDD
B5 Bead
C7 1.0uF
C40 100nF
C23 22uF_16V
GND_AVSSQ
GND_AVSSN
+VDDI
B7 Bead
C29 1.0uF
C30 100nF
C28 22uF_16V
4170010400
R55 715R
GND_R2SET
+A2VDD
C31 1.0uF
C33 100nF
C32 22uF_16V
GND_A2VSSN
+A2VDDQ
B9 Bead
C37 1.0uF
C38 100nF
C39 22uF_16V
GND_A2VSSQ
+VDD2DI
B8 Bead
C35 1.0uF
C36 100nF
C34 22uF_16V
R53 4.7K
R54 4.7K
R33 1K
R52 499R
R_DAC1 (16)
G_DAC1 (16)
B_DAC1 (16)
HSYNC_DAC1 (3,14,16)
VSYNC_DAC1 (3,14,16)
STEREOSYNC (18)
R_DAC2 (16)
G_DAC2 (16)
B_DAC2 (16)
HSYNC_DAC2 (16)
VSYNC_DAC2 (16)
Y_DAC2 (18)
C_DAC2 (18)
COMP_DAC2 (18)
HPD1 (17)
CRT1DDCDATA (3,16)
CRT1DDCCLK (3,16)
CRT2DDCDATA (16)
CRT2DDCCLK (16)
SDA (15,18)
SCL (3,15,18)
(14) DVALID
(14) PSYNC
TP12
TP13
(14) DVOMODE_0
(14) DVOMODE_1
(18) CLK_DVOCLK0
(18) DVO[11..0]
DVO[11..0]
C450 1uF
R99 22R
(18) DVO_VSYNC
(18) DVO_HSYNC
(18) DVO_DE
Install close to ASIC to provide return path for EMI
82pF C525
(14) DC_Strap2
(14,18) DC_Strap3
(14) DC_Strap4
(14) PAL/NTSC
(14) DEMUX_SEL
(14) GPIO[6..0]
(14) GPIO[13..8]
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
+3.3V_BUS
R586 499R
R587 499R
(15) D+
+VDD_1.8V
B33 X_Bead
+PVDD
C27 22uF_16V
C26 100nF
C41 1.0uF
GND_PVSS
PVDD
PVSS
+MPVDD
C46 22uF_16V
C45 100nF
C44 1.0uF
C43 1.0uF
C42 1.0uF
GND_MPVSS
MPVDD
MPVSS
XTALIN
XTALOUT
TP14
R43 1K
TESTEN
ROMCS#
C71 X_20pF
C79 X_20pF
Y3 X_27_MHZ
R30 X_1.0M
R65 150R
R64 X_0R
Overlap pads
R61 X_221
R66 150R
+3.3V_BUS
B3 X_220R
XTAL
Oscillator Circuit
R1625 X_1K
C1522 X_1.0uF
C1523 X_100nF
Y1
VCC
OUT
GND
E/D
X_27.000MHz
C2 X_22pF
SERIAL EEPROM 512K/1M
R91 10K
GPIO8 33R
GPIO9 33R
GPIO10 33R
ROMCS# 33R
RP193B
RP193D
RP193C
RP193A
ROM_SO
SI/A16
SCK/WEb
CSb
HOLD1
U11
D
Q
C
S
HOLD
W
VCC
VSS
M25P05-VMN6T
C80 100nF
ALTERNATIVE PART :M25P05(512Kbit)
MS-V005 ATI RV410
Size C
Document Number
RV410 Main
Rev 10
Date: Tuesday, December 28, 2004
Sheet 5 of 18



MS-V005 ATI RV410			
Size C	Document Number RV410_Power_and_NC		Rev 10
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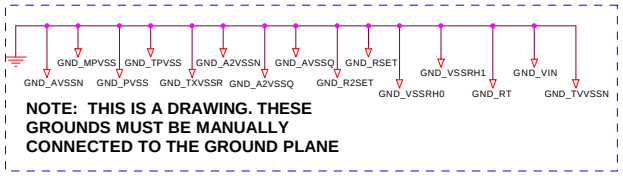

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

U1F

Part 6 of 7

PCI_EXPRESS_GND

AH27	PCIE_VSS_1	B1	VSS_1	VSS_45	AD16
AC23	PCIE_VSS_2	H1	VSS_2	VSS_44	AA6
AL27	PCIE_VSS_3	L1	VSS_3	VSS_43	P7
R23	PCIE_VSS_4	P1	VSS_4	VSS_42	P5
P25	PCIE_VSS_5	U1	VSS_5	VSS_41	M3
R25	PCIE_VSS_6	Y1	VSS_6	VSS_40	M9
T26	PCIE_VSS_7	AD7	VSS_7	VSS_39	L7
U26	PCIE_VSS_8	AE8	VSS_8	VSS_38	M7
W26	PCIE_VSS_9	AL1	VSS_9	VSS_47	AD17
Y26	PCIE_VSS_10	A2	VSS_10	VSS_48	AH11
AB26	PCIE_VSS_11	AM2	VSS_11	VSS_49	A8
AC26	PCIE_VSS_12	AD10	VSS_12	VSS_50	U7
AD25	PCIE_VSS_13	E8	VSS_13	VSS_51	C10
AE26	PCIE_VSS_14	H5	VSS_14	VSS_52	E9
AF26	PCIE_VSS_15	K10	VSS_15	VSS_53	F3
AD26	PCIE_VSS_16	M8	VSS_16	VSS_54	J9
AC25	PCIE_VSS_17	T10	VSS_17	VSS_55	N7
AH26	PCIE_VSS_18	E12	VSS_18	VSS_56	N3
AC28	PCIE_VSS_19	AC9	VSS_19	VSS_57	Y5
Y28	PCIE_VSS_20	AF14	VSS_20	VSS_58	AM13
U28	PCIE_VSS_21	AD8	VSS_21	VSS_59	AC10
P28	PCIE_VSS_22	C5	VSS_22	VSS_60	Y6
AH29	PCIE_VSS_23	F10	VSS_23	VSS_61	U6
AF28	PCIE_VSS_24	J3	VSS_24	VSS_62	E5
V29	PCIE_VSS_25	L6	VSS_25	VSS_63	AL13
AC29	PCIE_VSS_26	M6	VSS_26	VSS_64	A11
W27	PCIE_VSS_27	P6	VSS_27	VSS_65	U8
AB27	PCIE_VSS_28	AA4	VSS_28	VSS_66	U9
V26	PCIE_VSS_29	AG11	VSS_29	VSS_67	U10
AJ26	PCIE_VSS_30	V3	VSS_30	VSS_68	R6
AJ32	PCIE_VSS_31	AG16	VSS_31	VSS_69	AD6
AK29	PCIE_VSS_32	R3	VSS_32	VSS_70	V6
P26	PCIE_VSS_33	C6	VSS_33	VSS_71	AD14
P29	PCIE_VSS_34	C9	VSS_34	VSS_72	AD13
R29	PCIE_VSS_35	F6	VSS_35	VSS_73	D11
T29	PCIE_VSS_36	H7	VSS_36	VSS_74	J12
U29	PCIE_VSS_37	J6	VSS_37	VSS_75	K12
W29	PCIE_VSS_38			VSS_77	A13
Y29	PCIE_VSS_39			VSS_78	F13
AA29	PCIE_VSS_40			VSS_79	E13
AB29	PCIE_VSS_41			VSS_80	F15
AD29	PCIE_VSS_42			VSS_81	K16
AE29	PCIE_VSS_43			VSS_82	J21
AF29	PCIE_VSS_44			VSS_83	H16
AG29	PCIE_VSS_45			VSS_84	T15
AJ29	PCIE_VSS_46			VSS_85	V17
AK26	PCIE_VSS_47			VSS_86	C15
AK30	PCIE_VSS_48			VSS_87	C4
AG26	PCIE_VSS_49			VSS_88	U14
N30	PCIE_VSS_50			VSS_89	P15
R31	PCIE_VSS_51			VSS_90	A16
AF30	PCIE_VSS_52			VSS_91	E16
AC30	PCIE_VSS_53			VSS_92	G13
V31	PCIE_VSS_54			VSS_93	G16
P30	PCIE_VSS_55			VSS_94	P17
AA31	PCIE_VSS_56			VSS_95	R16
U30	PCIE_VSS_57			VSS_97	R14
AD31	PCIE_VSS_58			VSS_98	W16
AK32	PCIE_VSS_59			VSS_99	C18
AJ28	PCIE_VSS_60			VSS_100	F16
Y30	PCIE_VSS_61			VSS_101	W18
AJ30	PCIE_VSS_62			VSS_102	U18
AK31	PCIE_VSS_63			VSS_103	AE16
AA23	PCIE_VSS_64			VSS_104	AE17
AG31	PCIE_VSS_65			VSS_105	A19
N24	PCIE_VSS_66			VSS_106	H32
W23	PCIE_VSS_67			VSS_107	E19
AB23	PCIE_VSS_69			VSS_108	G19
P24	PCIE_VSS_70			VSS_109	N8
R24	PCIE_VSS_71			VSS_110	Y7
T24	PCIE_VSS_72			VSS_112	T19
U24	PCIE_VSS_73			VSS_113	V19
V24	PCIE_VSS_74			VSS_114	G21
W24	PCIE_VSS_75			VSS_115	C21
Y24	PCIE_VSS_76			VSS_116	F21
AC24	PCIE_VSS_77			VSS_117	AE14
AH24	PCIE_VSS_78			VSS_118	AK16
V25	PCIE_VSS_79			VSS_119	U5
AA25	PCIE_VSS_80			VSS_120	F22
R26	PCIE_VSS_81			VSS_121	F18
AA26	PCIE_VSS_82			VSS_122	K30
T27	PCIE_VSS_83			VSS_124	C24
AE27	PCIE_VSS_84			VSS_125	F24
				VSS_126	M24
				VSS_127	A25
				VSS_128	D30
				VSS_129	E25
				VSS_130	G25
				VSS_131	G20
				VSS_132	G22
				VSS_133	E27
				VSS_134	E28
				VSS_135	H21
				VSS_136	C27
				VSS_137	E32
				VSS_138	H28
				VSS_139	J30
				VSS_140	K17
				VSS_141	K27
				VSS_142	M32
				VSS_143	A22
				VSS_144	C20
				VSS_145	E19
				VSS_146	H20
				VSS_147	J24
				VSS_148	M28
				VSS_149	J28
				VSS_150	J16
				VSS_151	F30
				VSS_152	K23
				VSS_153	L29
				VSS_154	A31
				VSS_155	B32
				VSS_156	E30
				VSS_157	AE15
				VSS_158	AG23
				VSS_159	AD9
				VSS_160	AF16
				VSS_161	AH10
				VSS_163	AJ10
				VSS_164	AD15
				VSS_165	AH16

CORE GND

RV410

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Size: C	Document Number: RV410_Core_GND	Rev: 10
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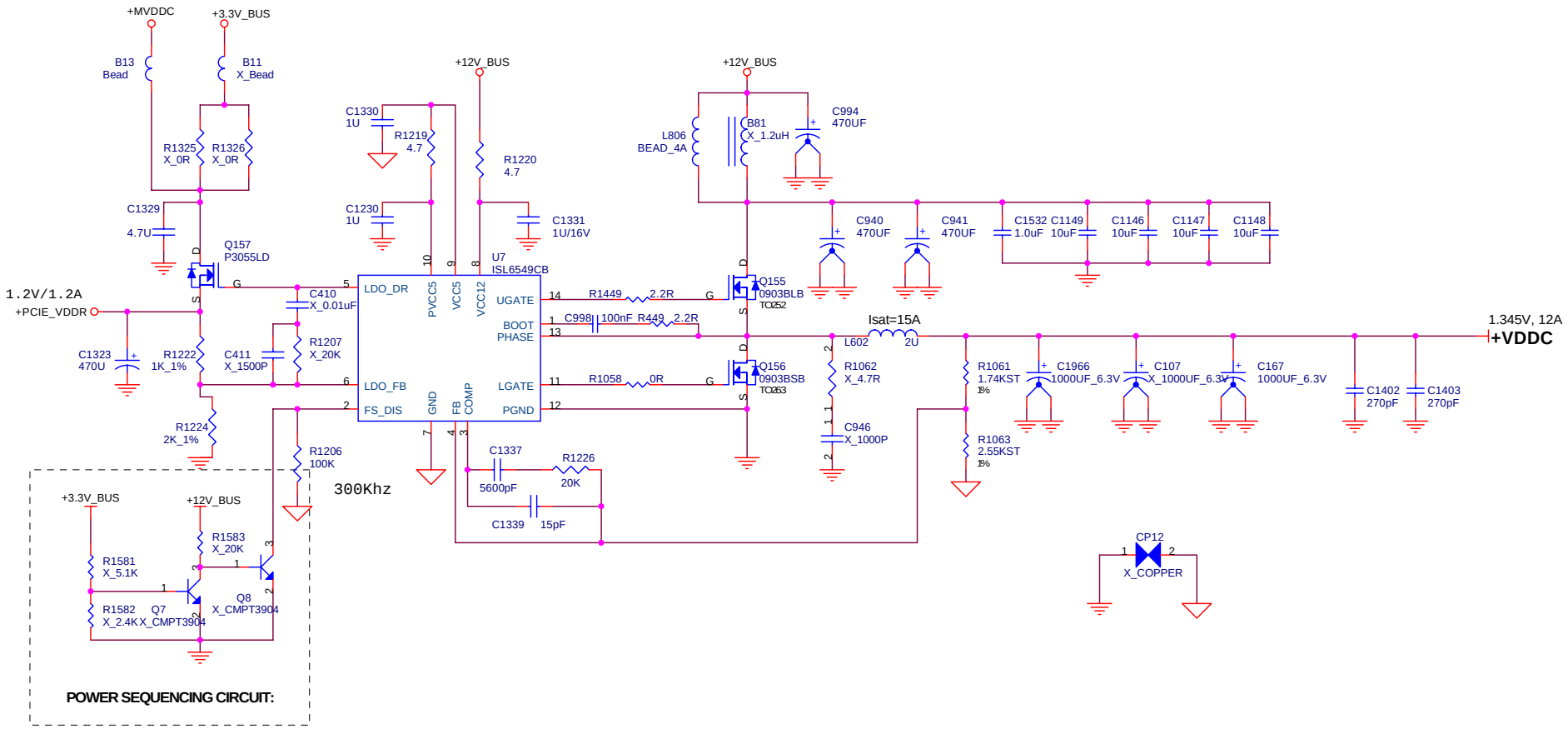
VDDC



	MS-V005 ATI RV410	
Size B	Document Number: Regulator of GPU	Rev 10
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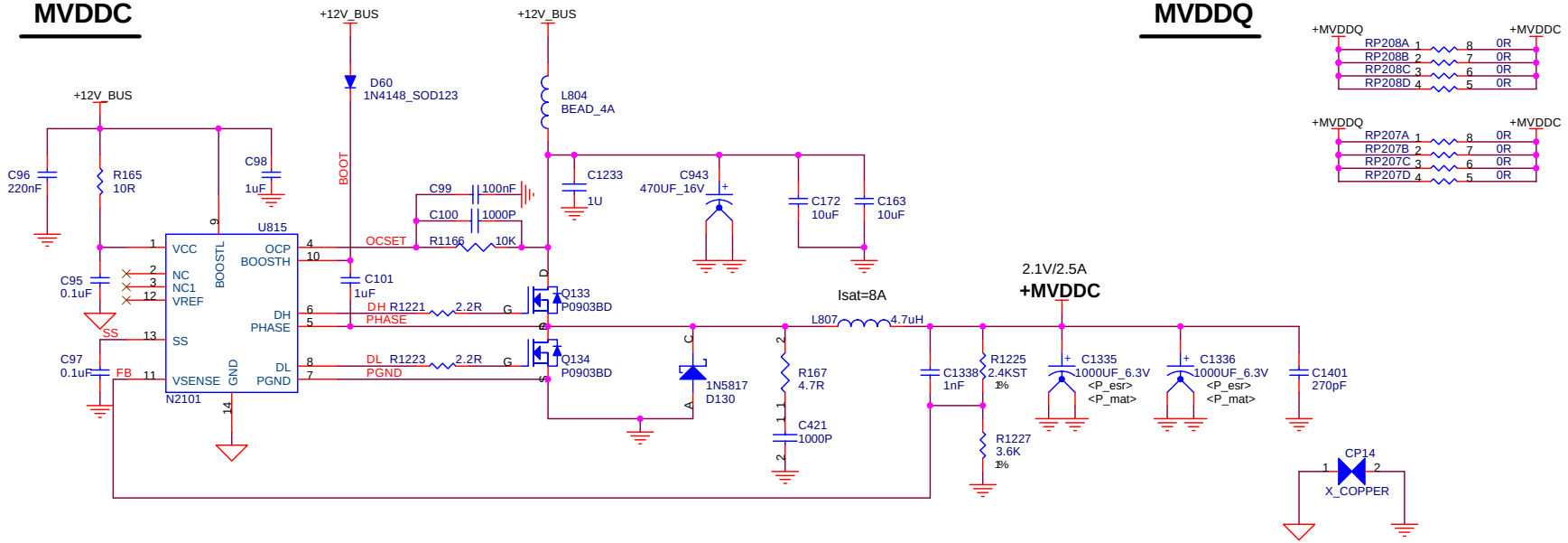

MS-V005 ATI RV410		
Size B	Document Number **Regulator of Memory**	Rev 10
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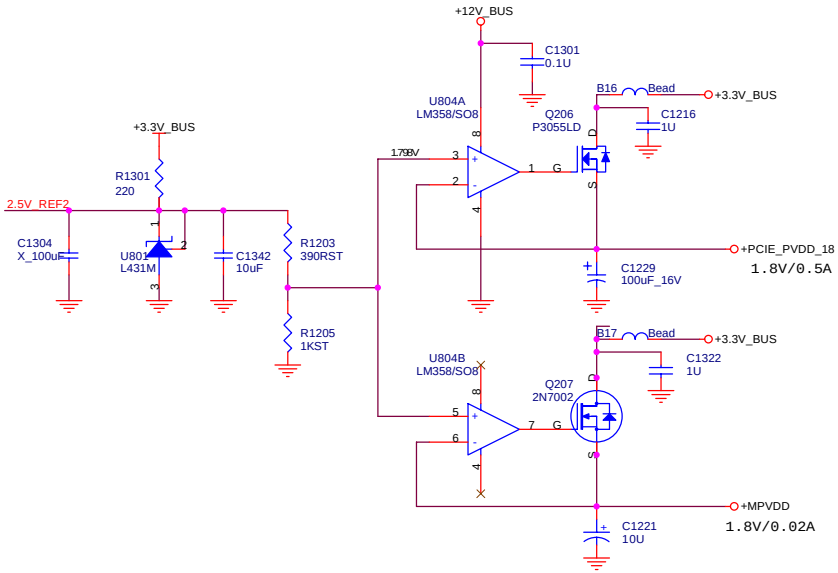

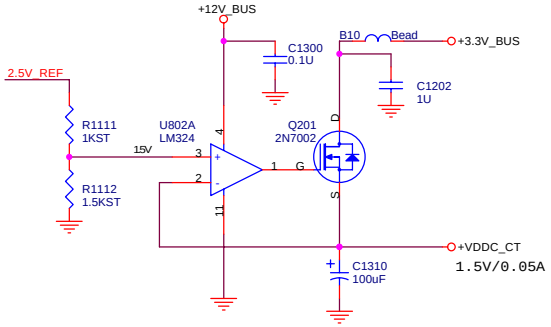

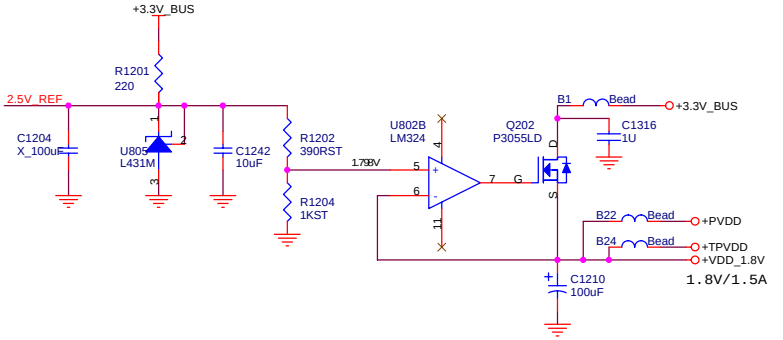

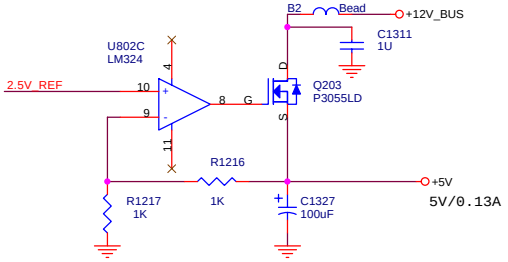

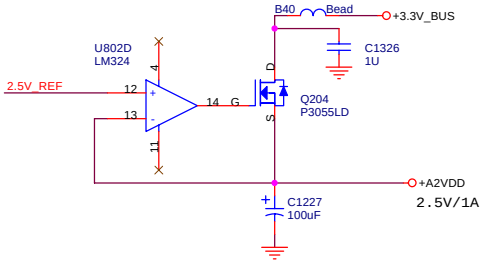

MS-V005 ATI RV410

Size	Document Number	Rev
Custom	Regulator for Others	10

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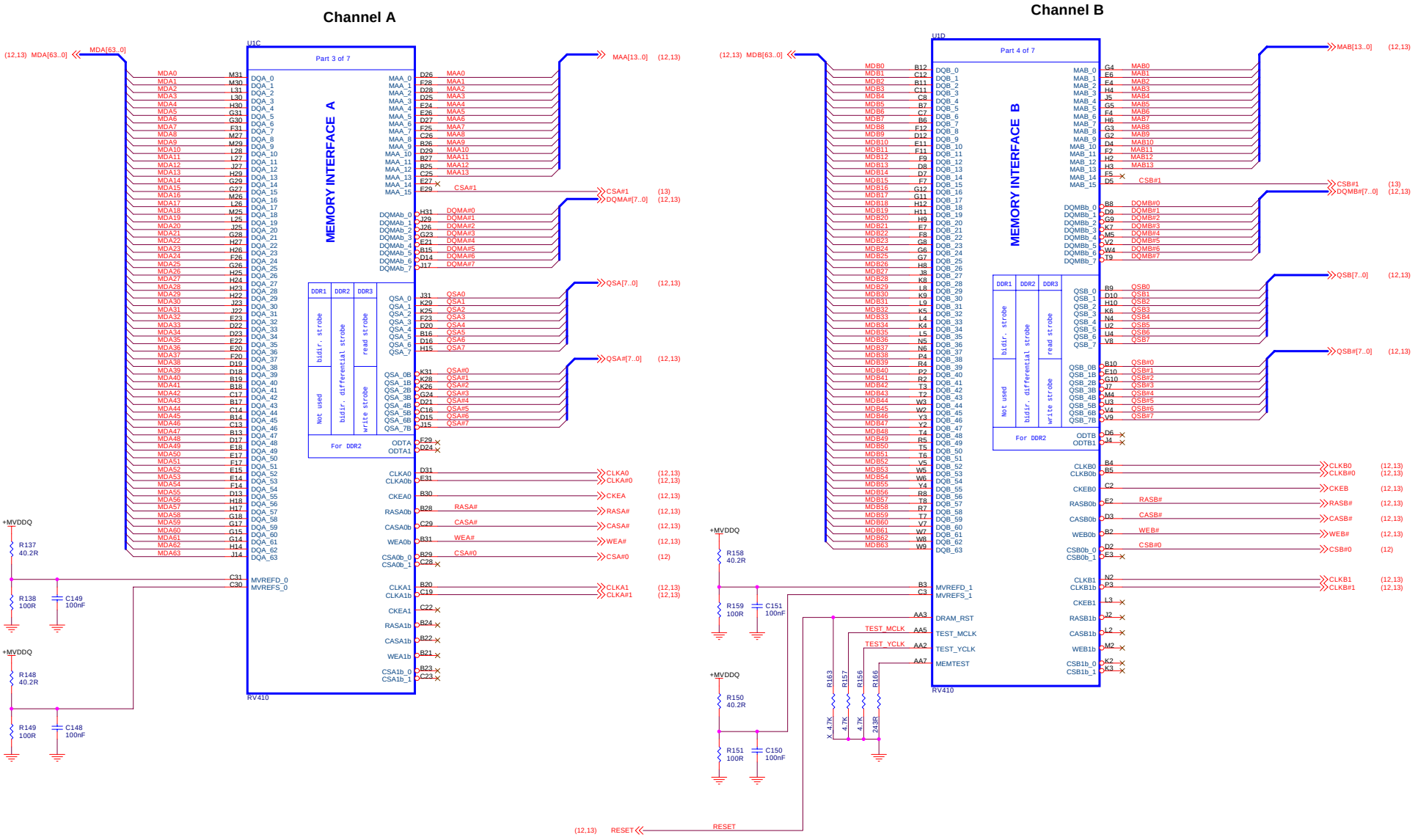
RV410 MEMORY CHANNELS A and B



MS-V005 ATI RV410			
Size C	Document Number RV410_MEM_A_B		Rev 10
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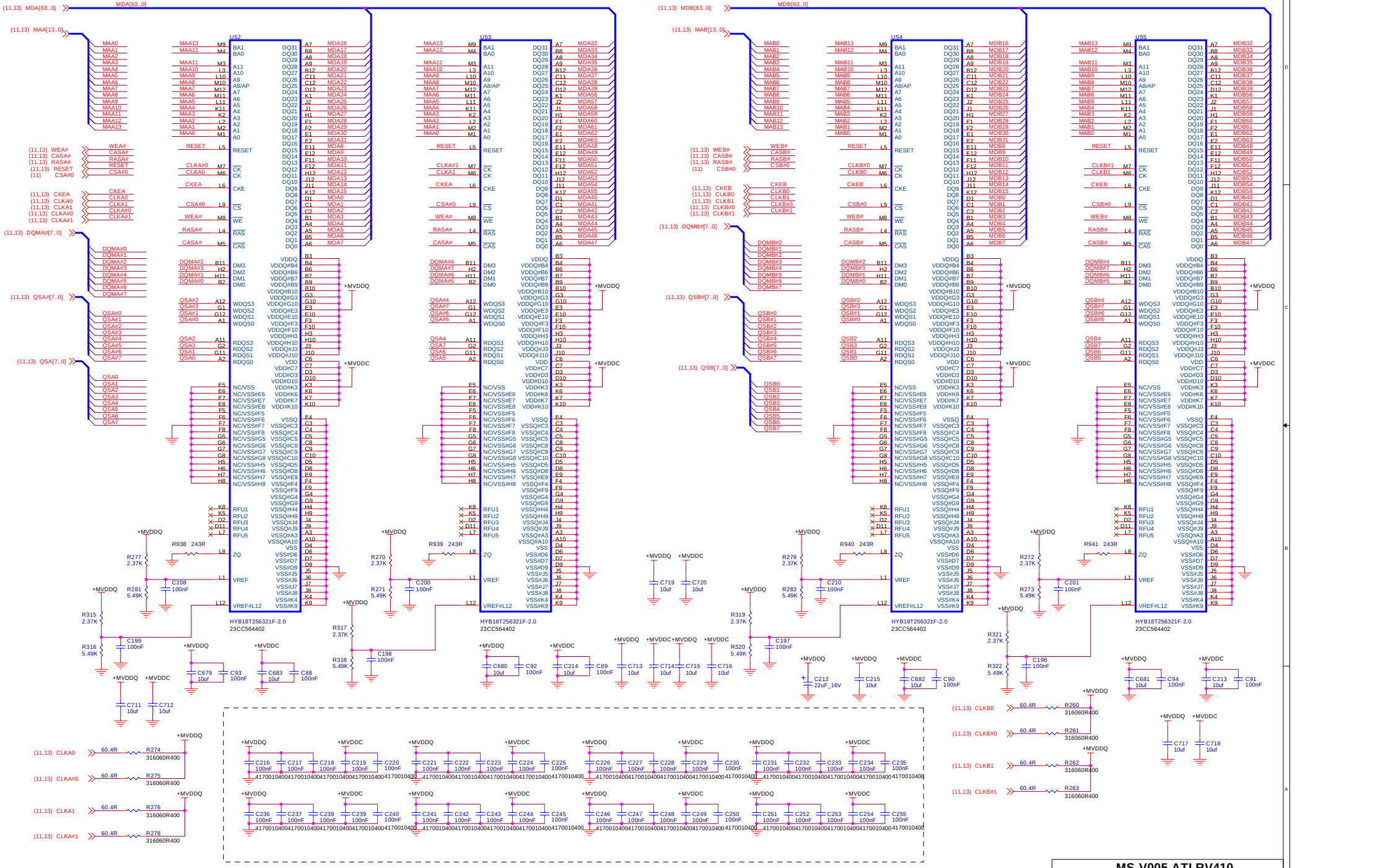
256 Mbit GDDRIII Channels A and B Rank 1

Channel A

Channel B



MS-V005 ATI RV410		
Size C	Document Number GDDRIII_A_B_Rank0	Rev 10
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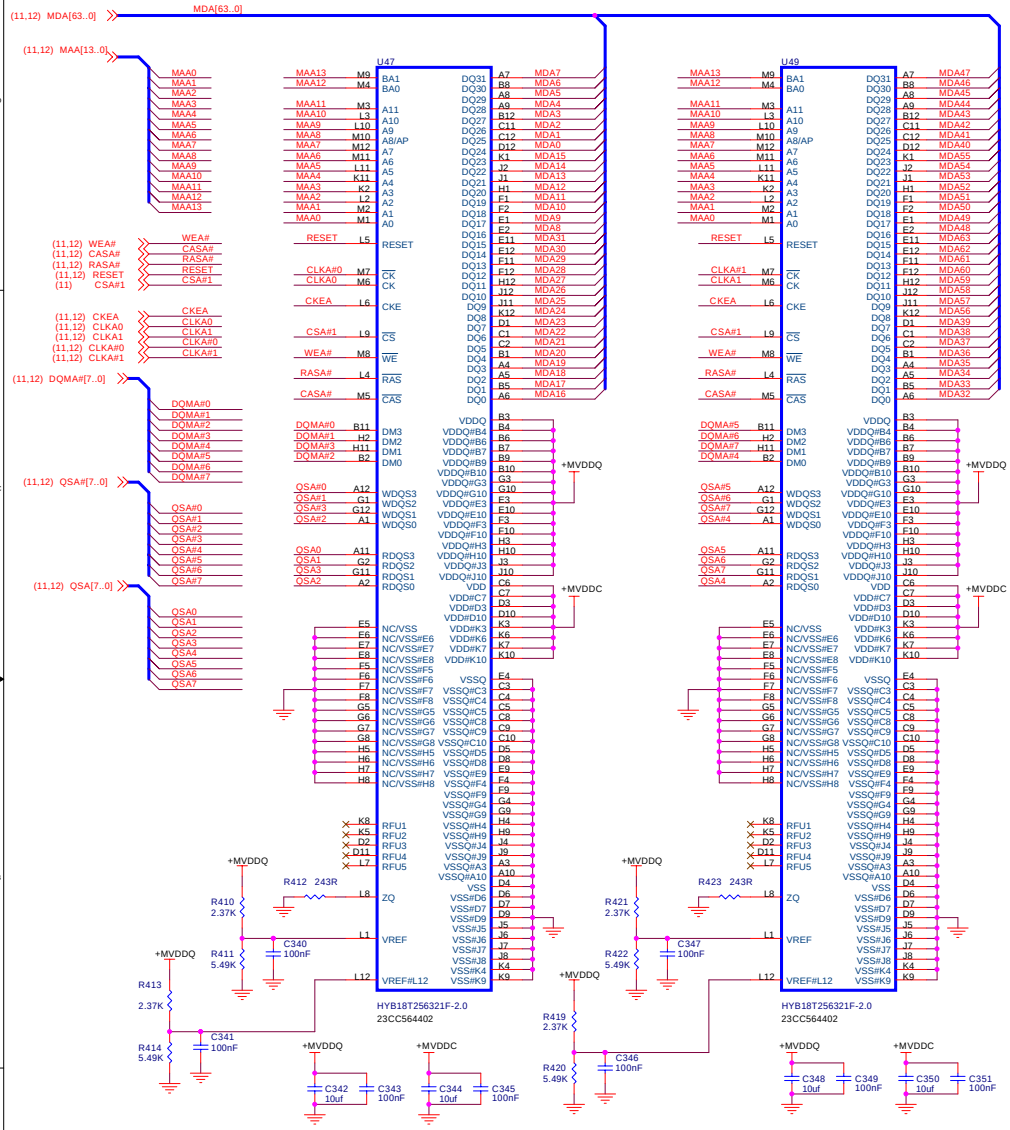
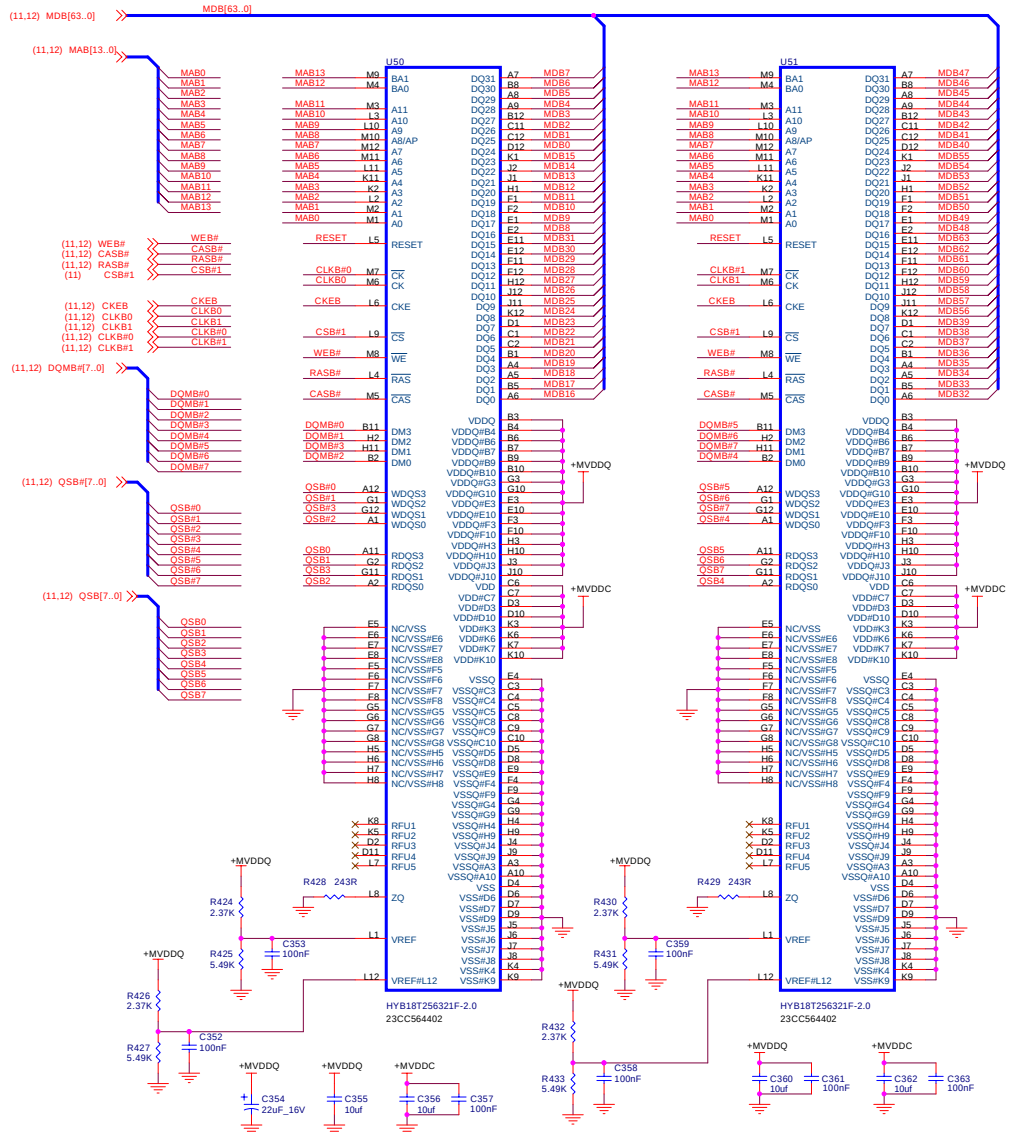
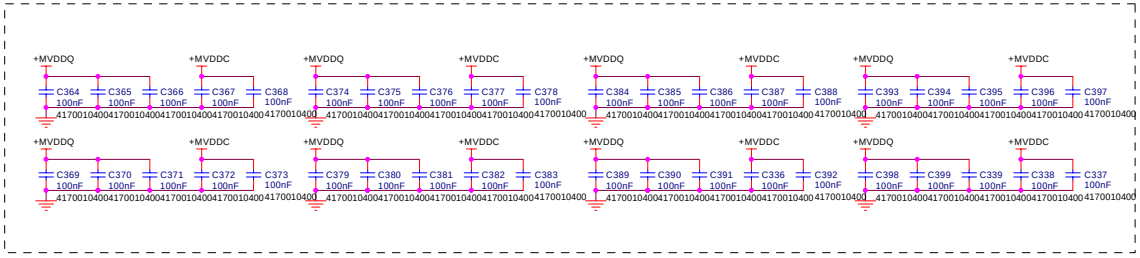
256 Mbit GDDRIII Channels A and B Rank 1

Channel A



Channel B





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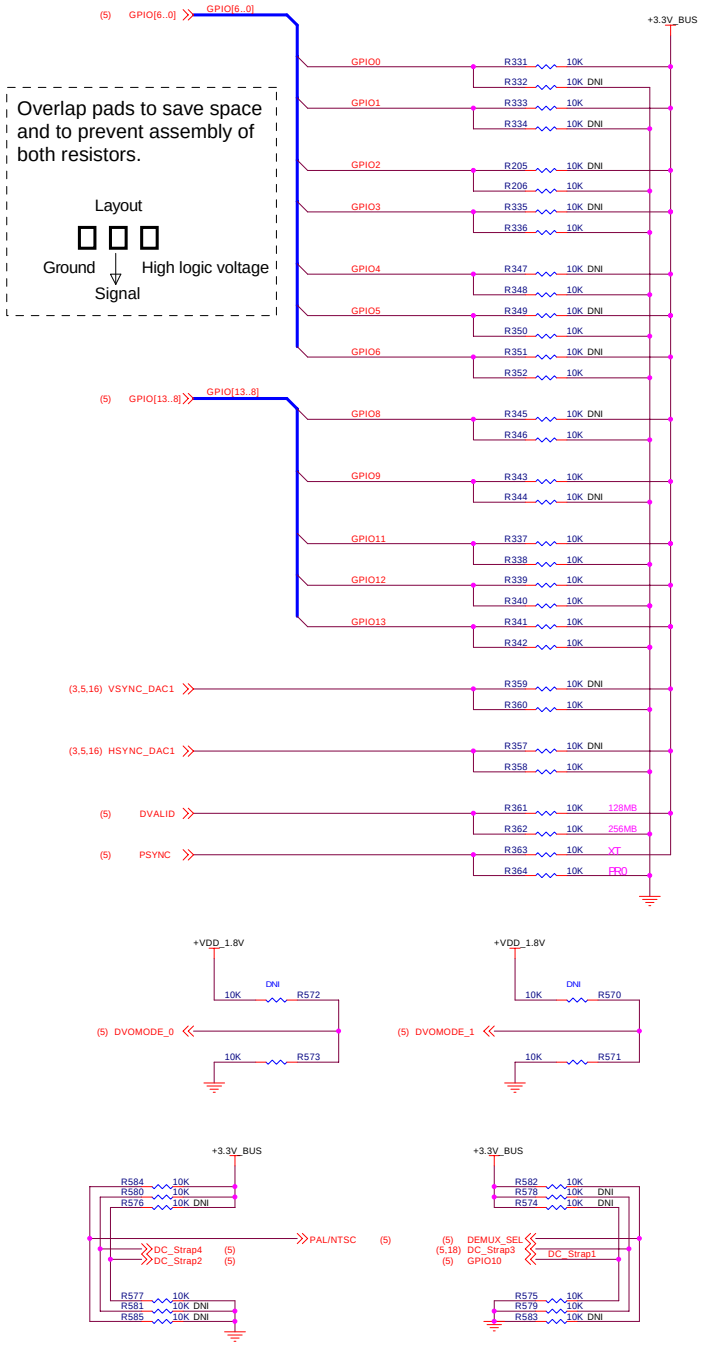
OPTION STRAPS



RV410 Shared Straps — REV. 0.5

STRAPS	PIN	DESCRIPTION	VALUE
PCIE_SWING	GPIO(0)	Transmitter Swing Control 0: 50% Tx output swing mode 1: full Tx output swing	1
TRANSMIT_DE-EMPHASIS	GPIO(1)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	1
PCIE_MODE (ATI Internal)	GPIO(3:2)	PCIE mode: 00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: RESERVED	00
TX_IEXT	GPIO(4)	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage	0
FORCE _COMPLIANCE	GPIO(5)	Force chip to get to compliance state quickly for Tester purposes 0: Normal operation 1: Force to compliance state	0
PLL_BW (ATI Internal)	GPIO(6)	0: Full PLL Bandwidth 1: Reduced PLL bandwidth	0
DEBUG_ACCESS	GPIO(8)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible 0: Disable debug access 1: Enable debug access	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type. GPIO[9,13,12,11] 000x - No ROM,CHG_ID=00 001x - No ROM, CHG_ID=01 010x - No ROM, CHG_ID=10 011x - No ROM, CHG_ID=11 1001 - 1M Serial AT25F1024 ROM (Atmel) 1010 - 1M Serial AT45DB011 ROM (Atmel) 1011 - 1M Serial M25P10 ROM (ST) 1100 - 512K Serial M25P05 ROM (ST) 1101 - 1M Serial SST45LF010 ROM (SST) 1M Serial W45B512 ROM (WinBond) 512K Serial W45B012 ROM (WinBond) 1110 - 1M Serial SST25VF010 ROM (SST) 512K Serial SST25VF512 ROM (SST) 1111 - 1M NX25F011B ROM (NexFlash) **Chip IDs:** Chip ID is based on substrate fuses and CHG_ID strap (which comes from ROM if used, or pin straps if no ROM is connected): CHG_ID = ROMIDCFG[2:1] = GPIO[13:12]	1100
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this in low during reset. **0 - Slave VIP host port devices present** **1 - No slave VIP host port devices reporting presence during reset**	1
RFU	HSYNC	RFU **0 - Normal** 1 - Not used	0

RV410 Dedicated Straps — REV. 0.2

ZV_VOLTAGE_SEL0	DVOVMODE_0	DVOVMODE_0 is for ZV_LCDCNTL and ZV_LCDDATA(11:0). **0 - 3.3 V signaling** 1 - 1.8 V signaling	0
ZV_VOLTAGE_SEL1	DVOVMODE_1	DVOVMODE_1 is for ZV_LCDDATA(23:12) **0 - 3.3 V signaling** 1 - 1.8 V signaling	0

Board Straps — REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0) **GDDR3 loading selection**	DVALID, PSYNC.	**0 0 2 loads(Dual ranks)** **0 1 1 load(Single rank)** **1 0 Reserved** **1 1 Reserved**	000
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Not detected	0
DC_Strap3	LCDDATA(14)	HDTV out detect **0 - Detected** 1 - Enabled	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off **01 - DAC2 On as CRT** 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1

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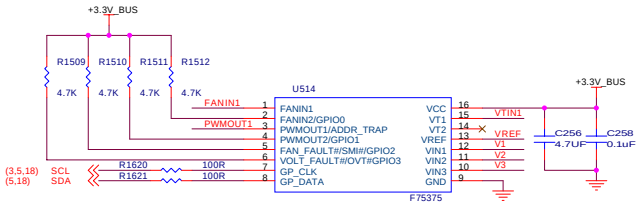
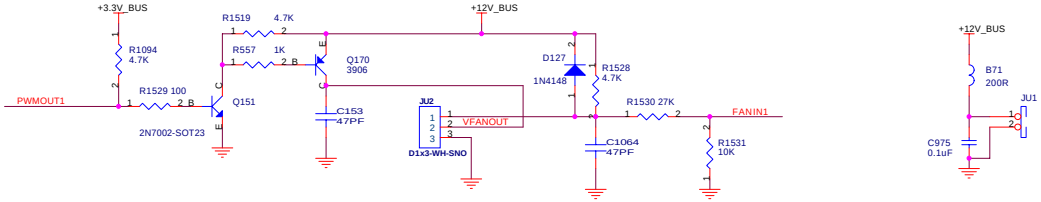
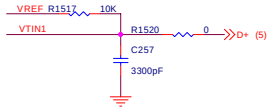
H/W MONITOR



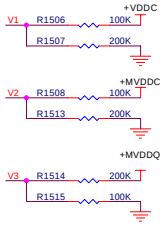
SMART FAN



TEMPERATURE SENSORING CIRCUIT

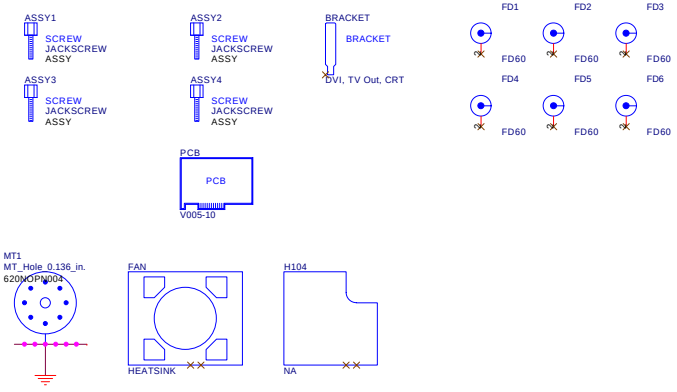


VOLTAGE SENSORING CIRCUIT



OPTION PART

MECHANICAL



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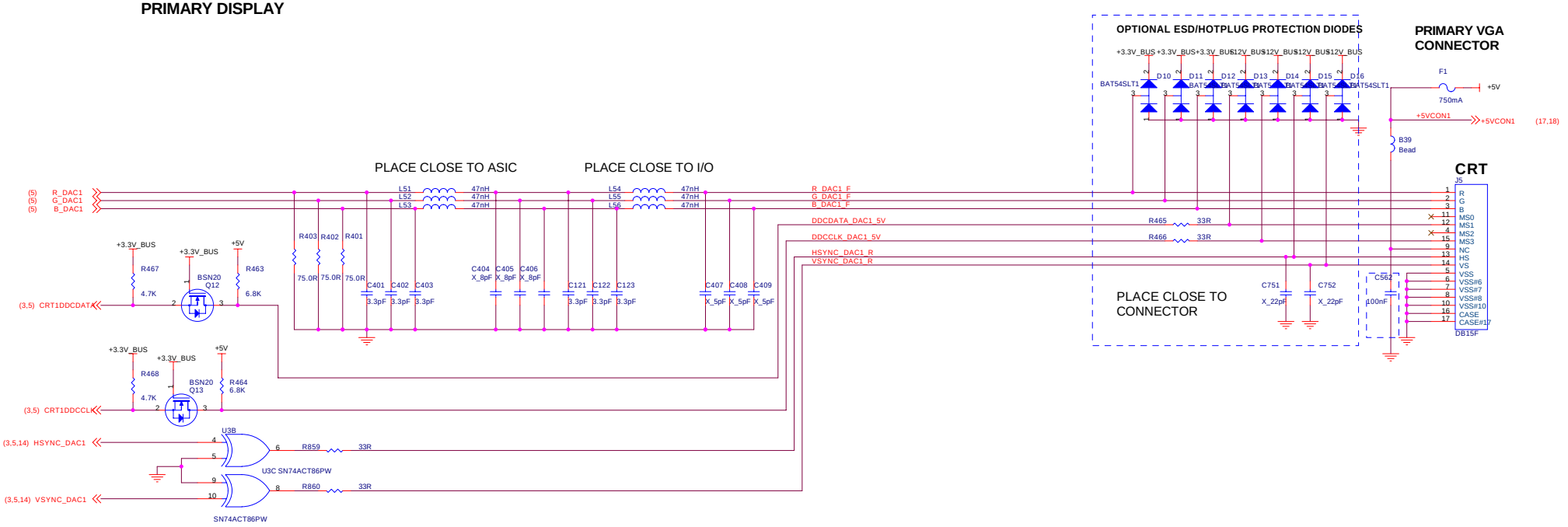
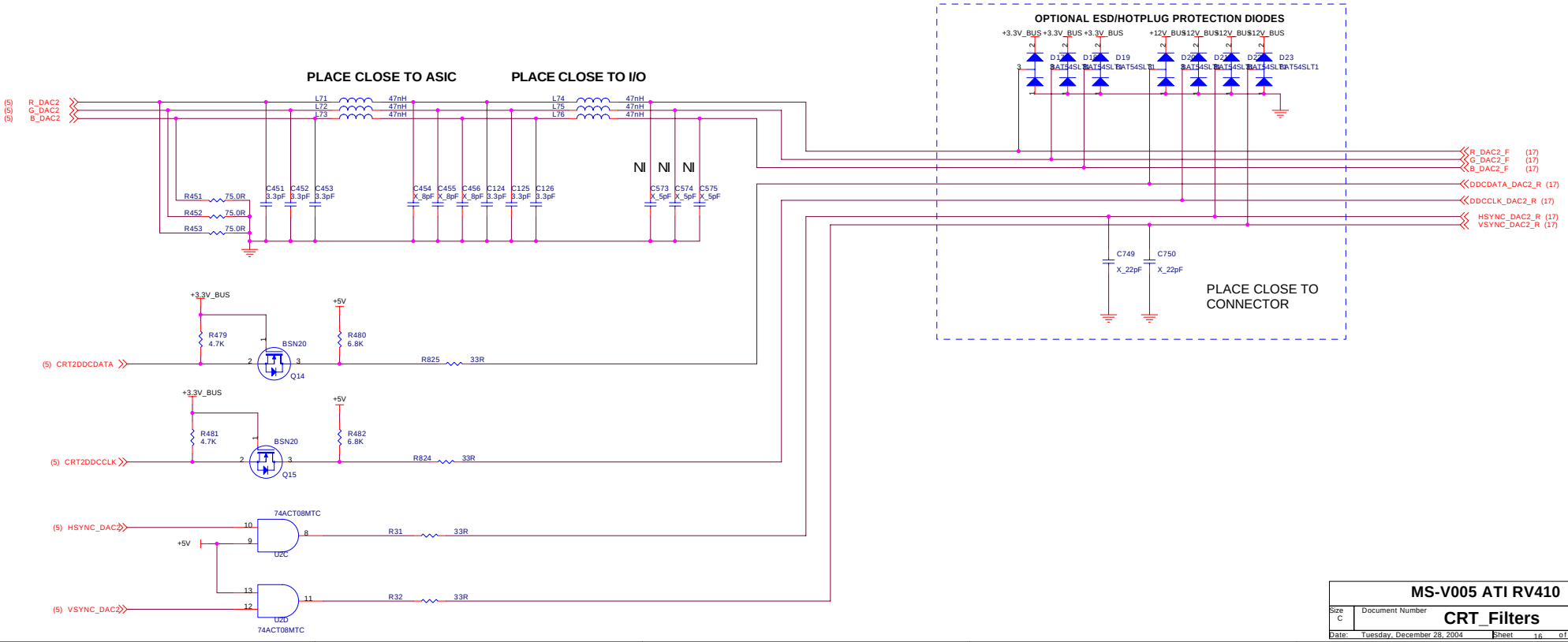
PRIMARY DISPLAY



SECONDARY DISPLAY



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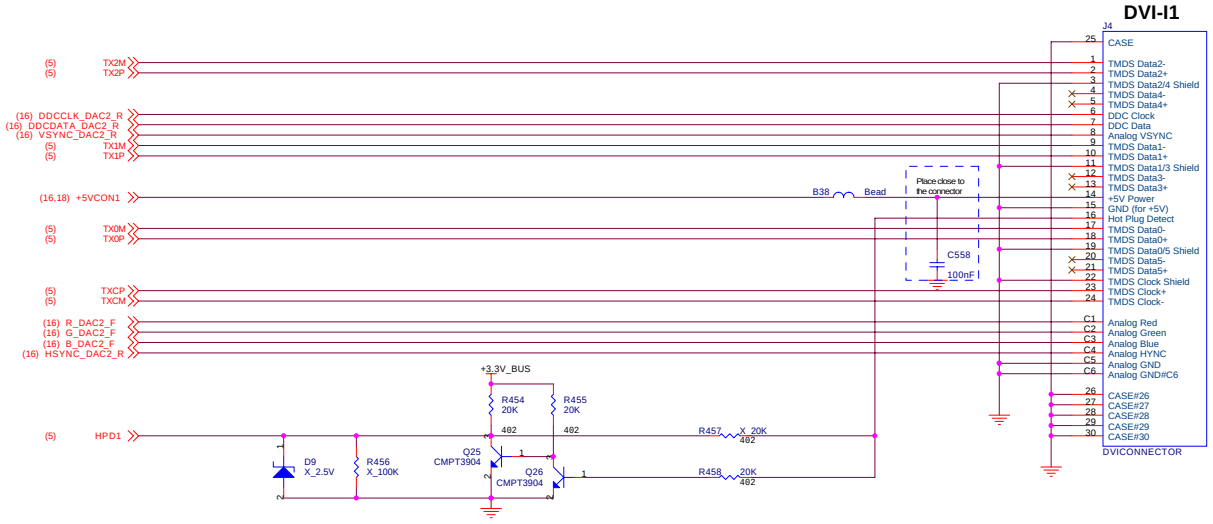
PRIMARY DVI-I CONNECTOR (DVI-I1)



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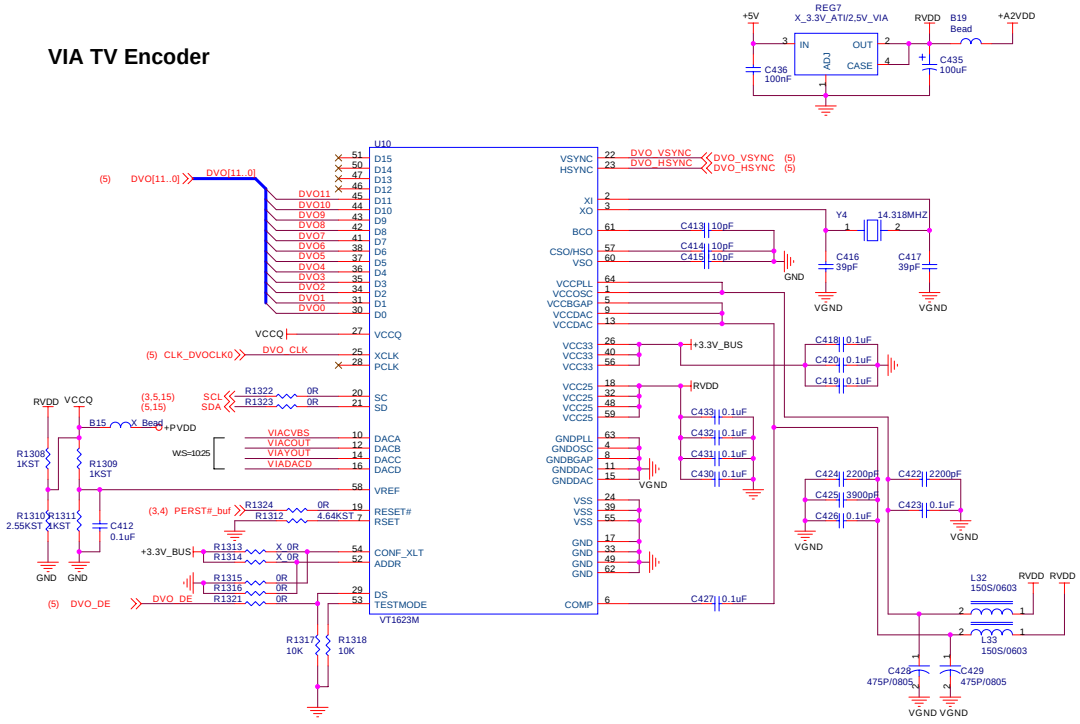
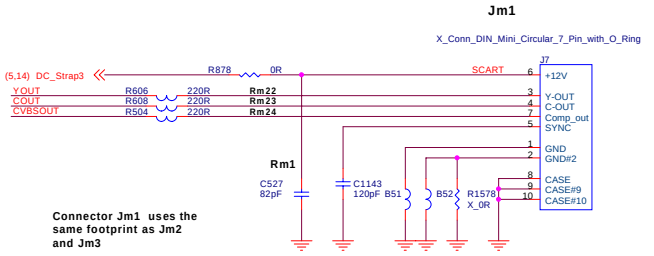
VIA TV Encoder

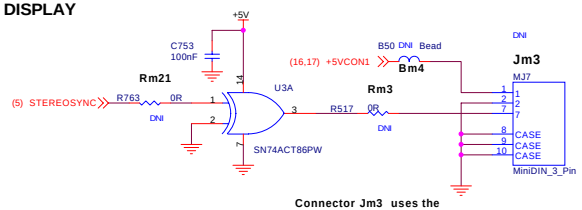


TV Out (SVHS) MiniDIN 7-pin



Connector Jm1 uses the same footprint as Jm2 and Jm3

STEREOSCOPIC DISPLAY CONNECTOR

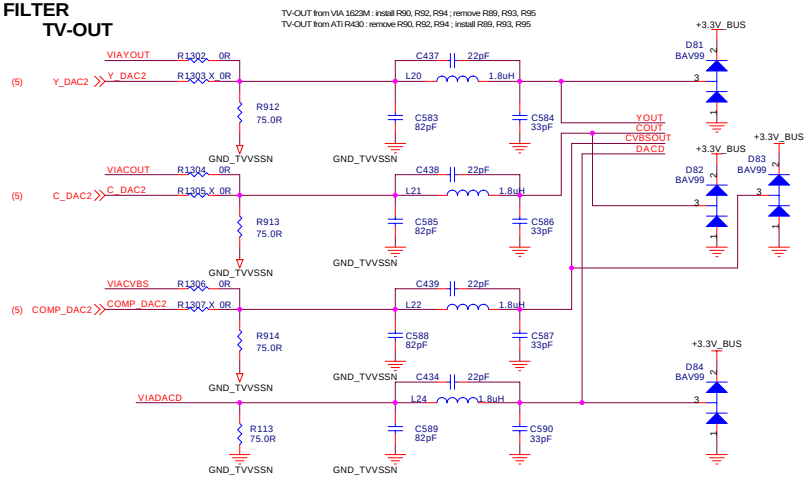


Connector Jm3 uses the same footprint as Jm1 and Jm2

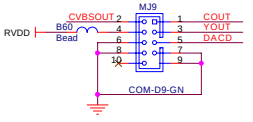
Not Installed

TV-OUT FILTER

TV-OUT



SCART



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