

GA102 DT SKU P-BOARD

350W, FH Std PCB, 384b, GDDR6X x8  
DP + DP + DP + HDMI/DP

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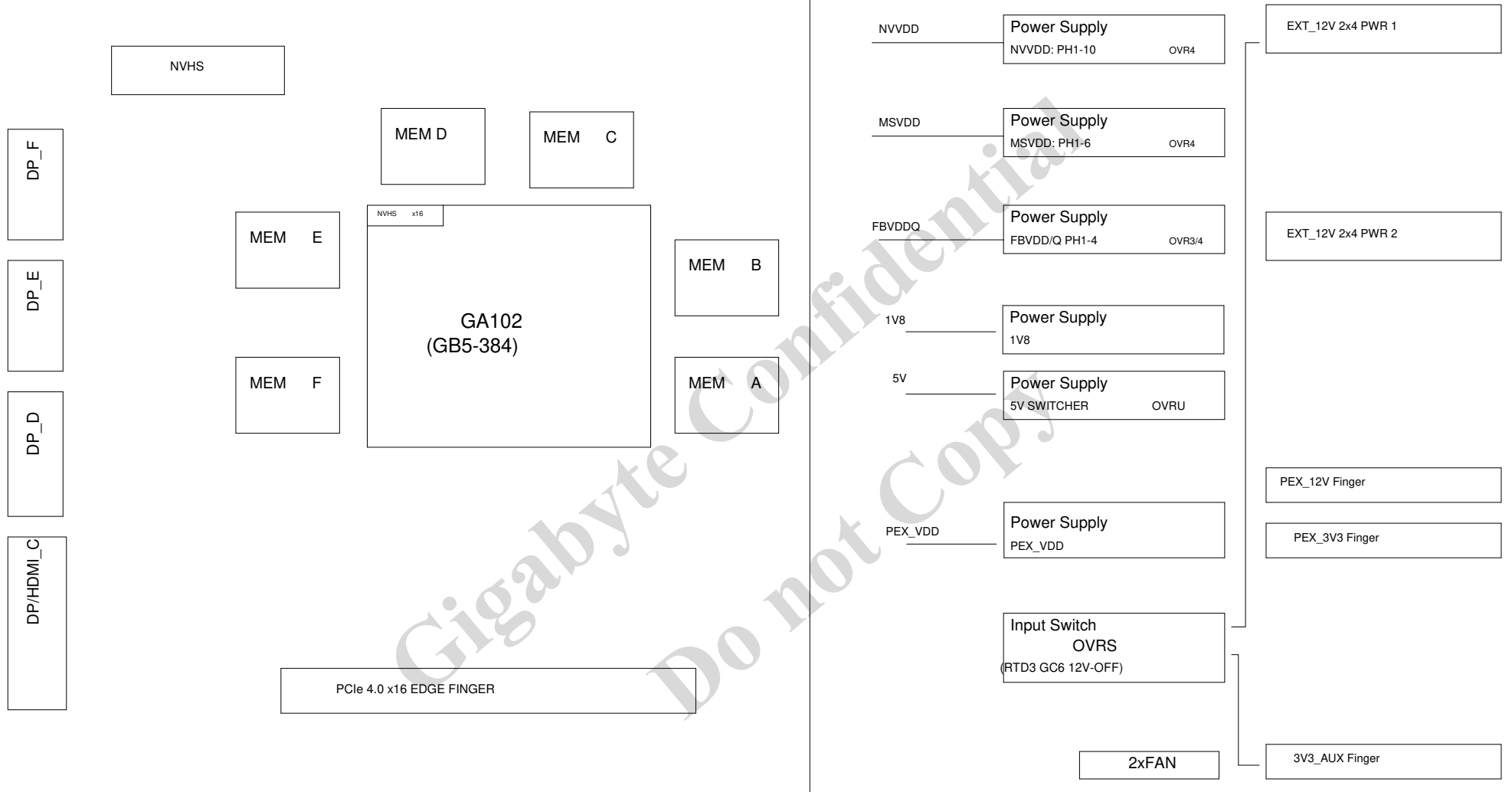
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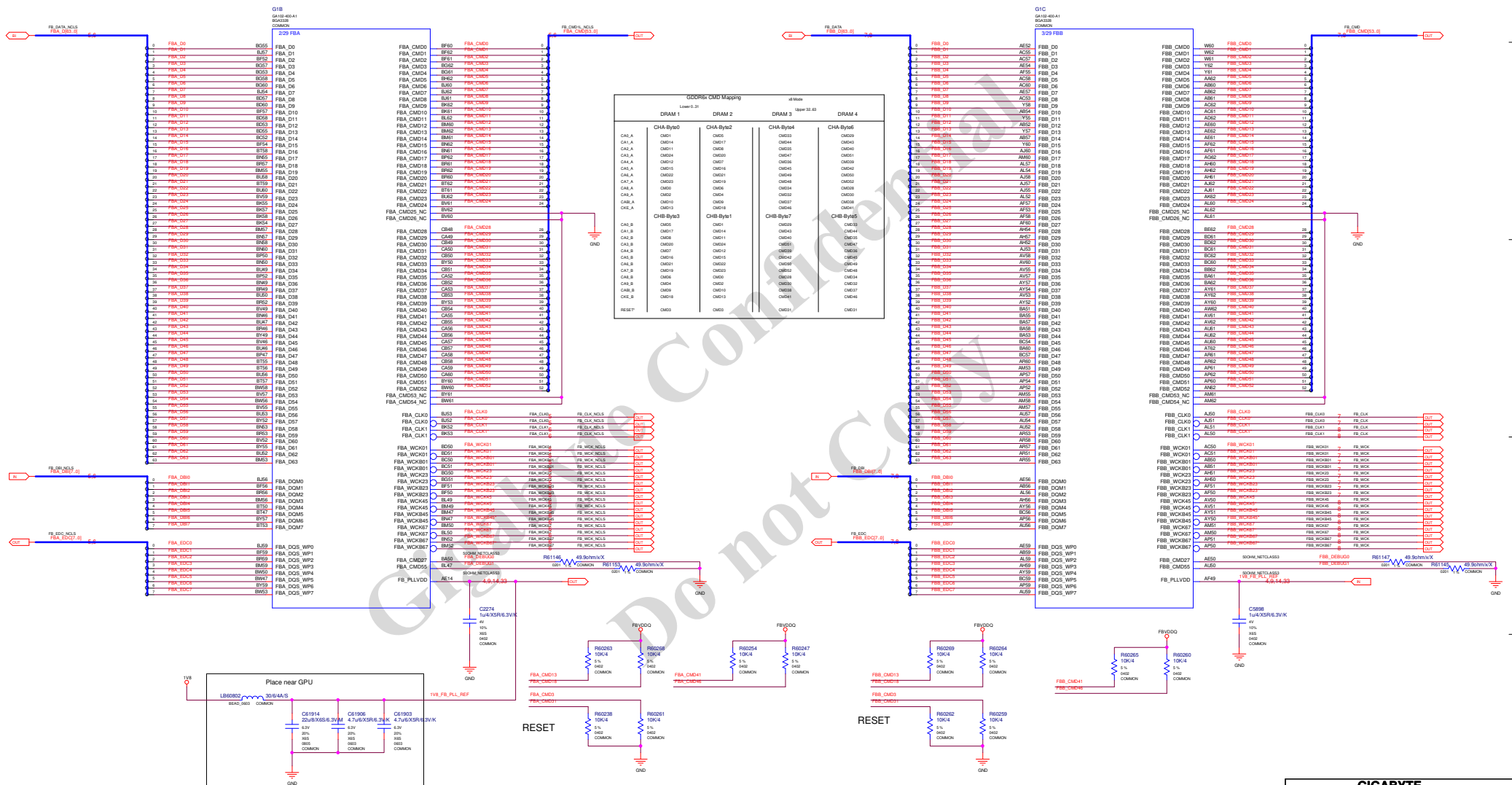
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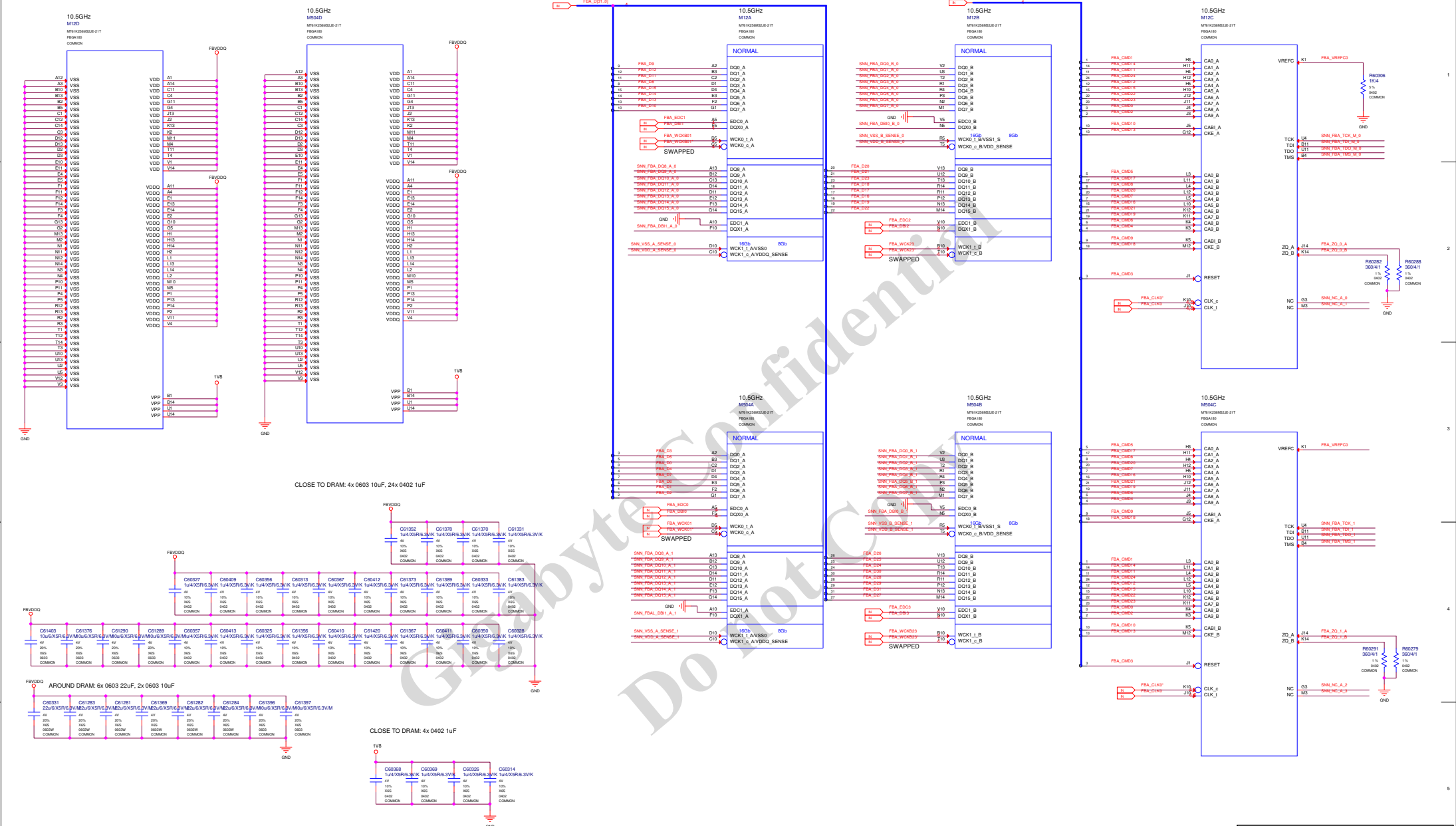
### Block Diagram







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Size	Document Number	New	



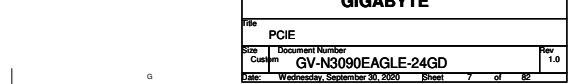
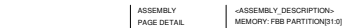
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ASSEMBLY  
PAGE DETAIL

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File: PCIE			
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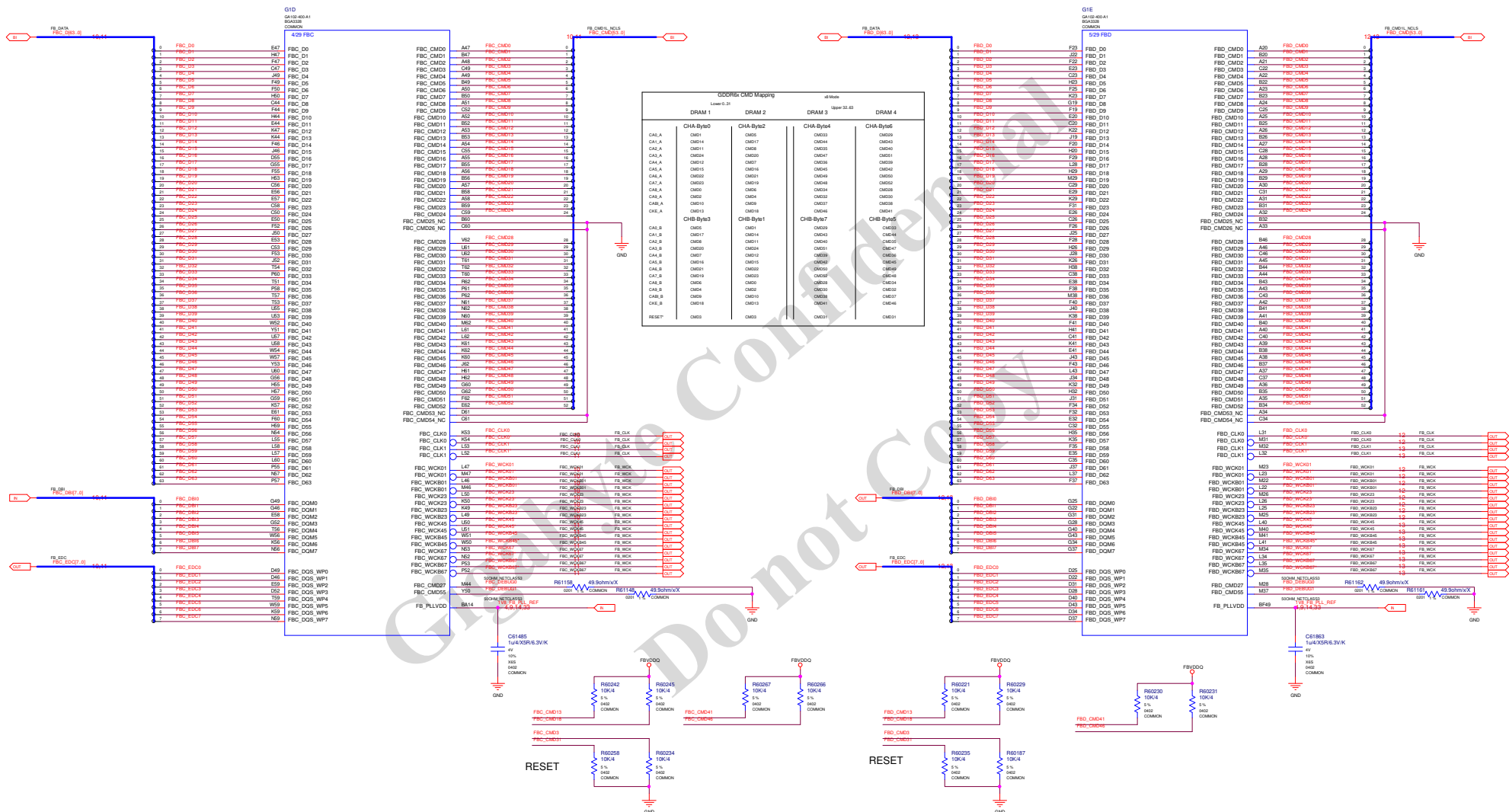








MEMORY: GPU Partition C/D
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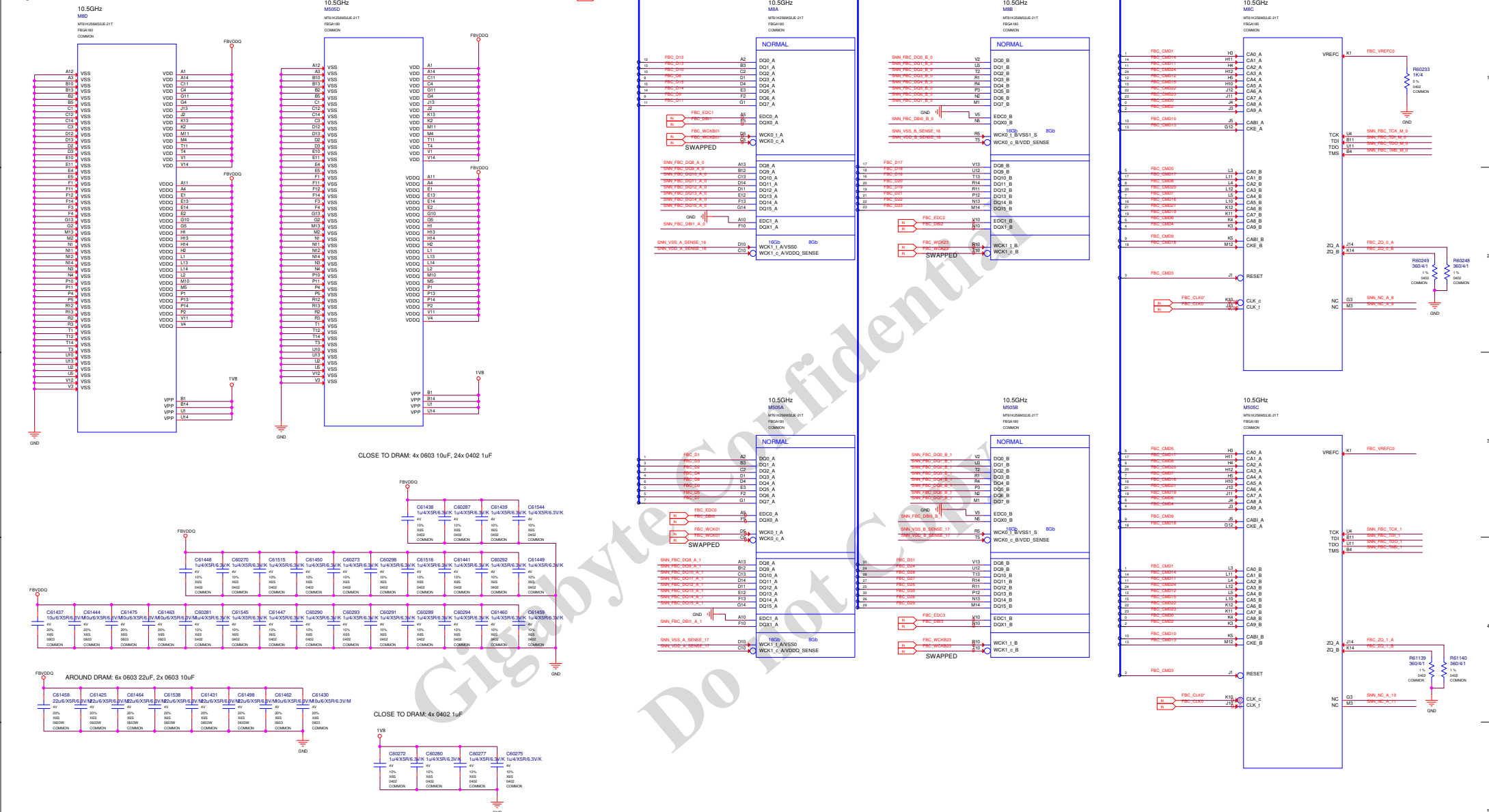


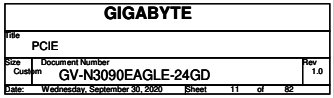
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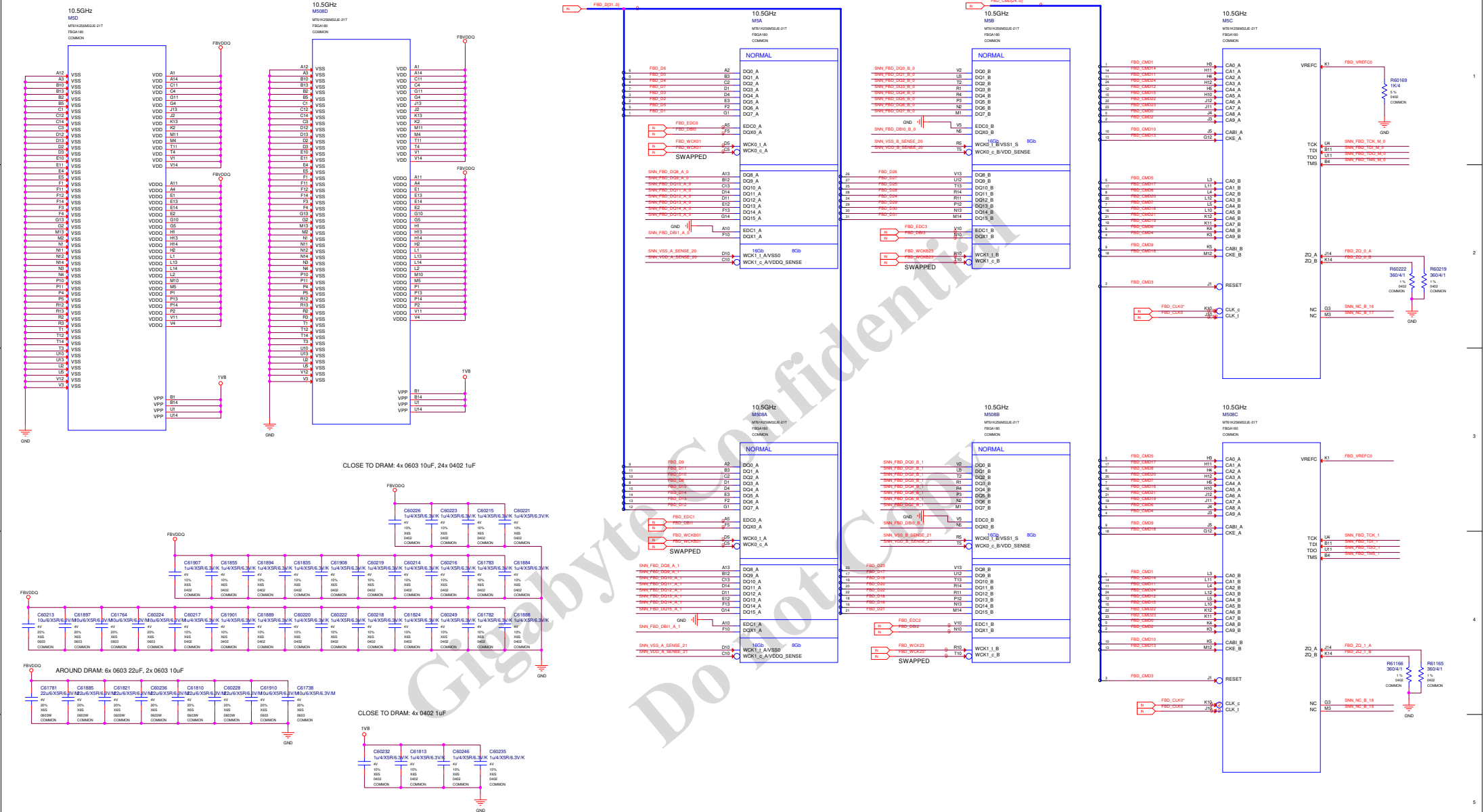
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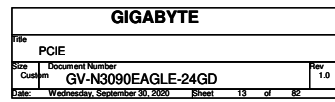
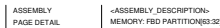
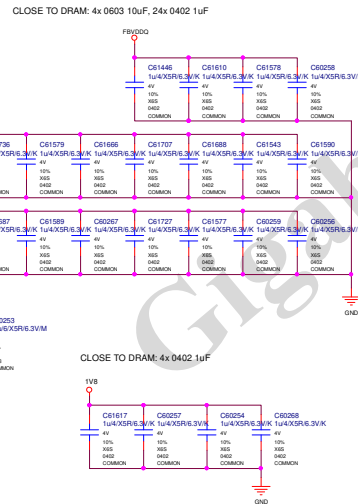




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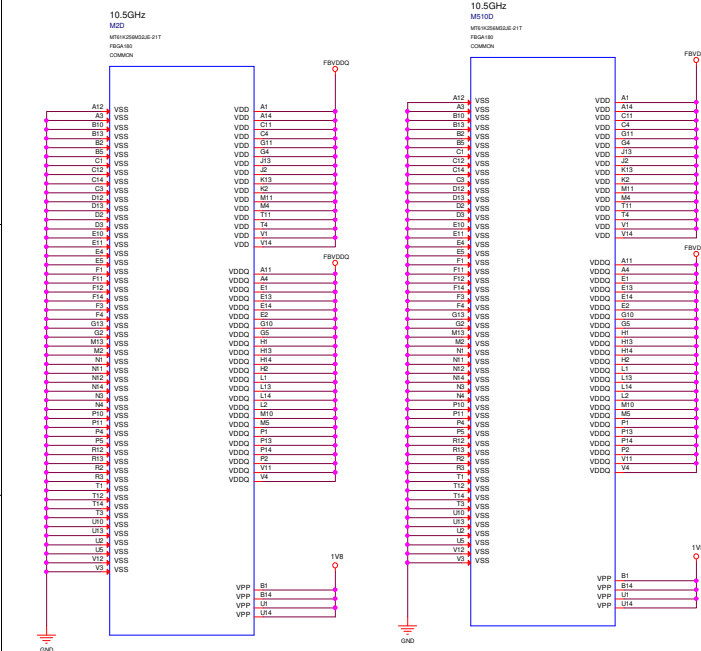
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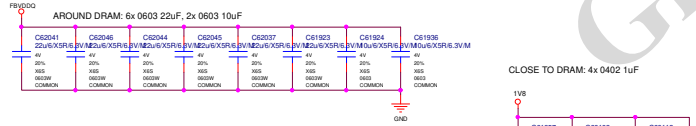
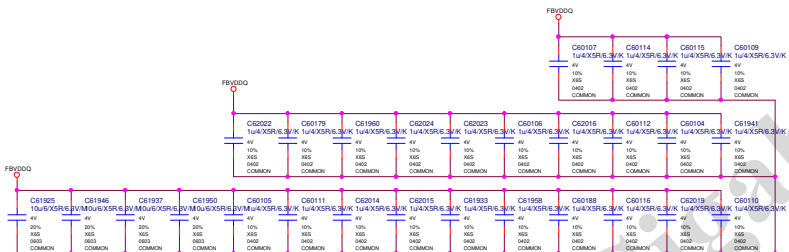




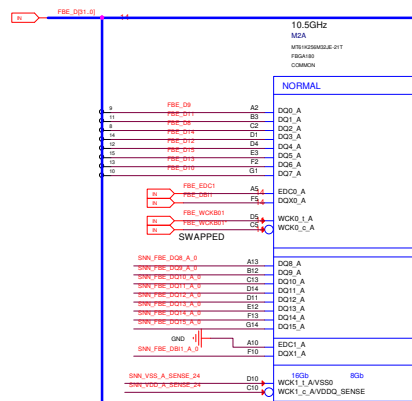
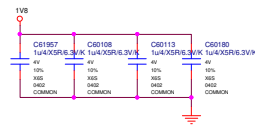




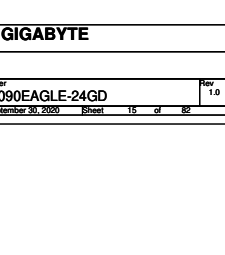
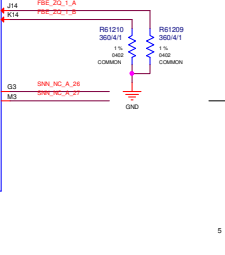
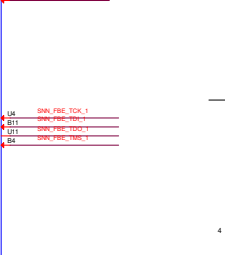
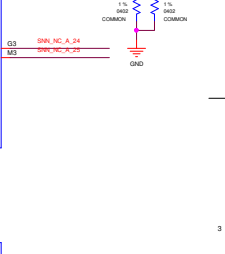
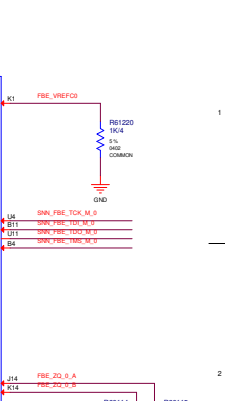
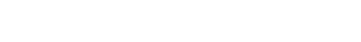
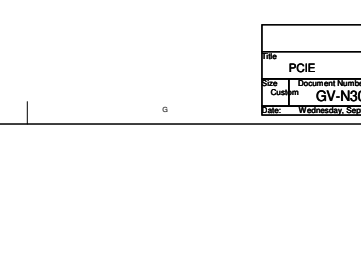
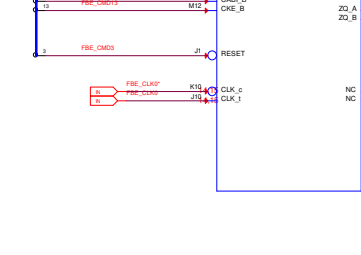
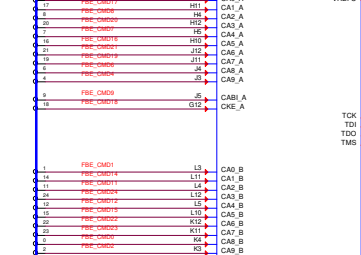
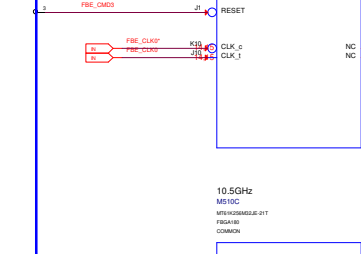
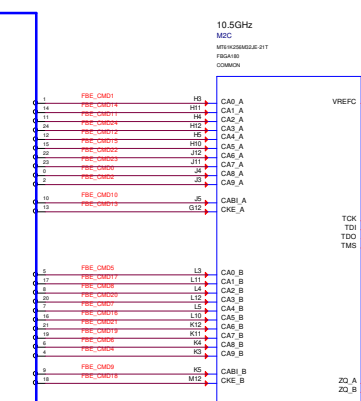
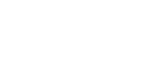
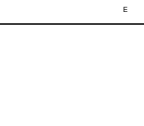
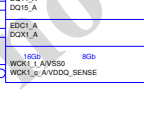
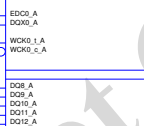
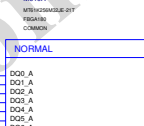
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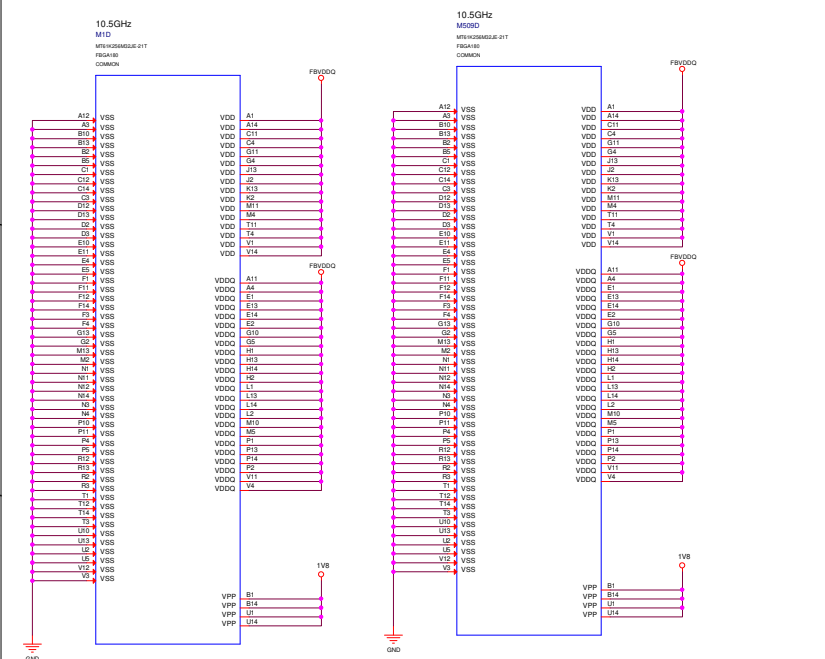


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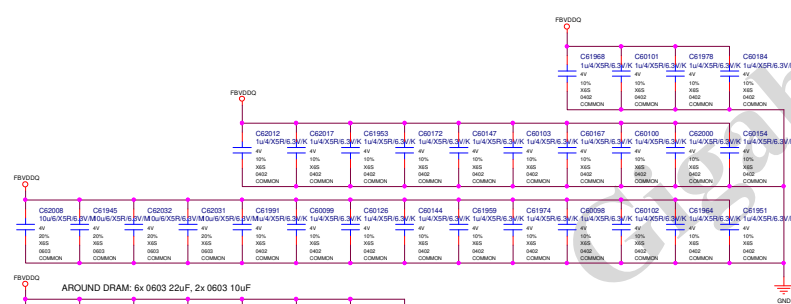
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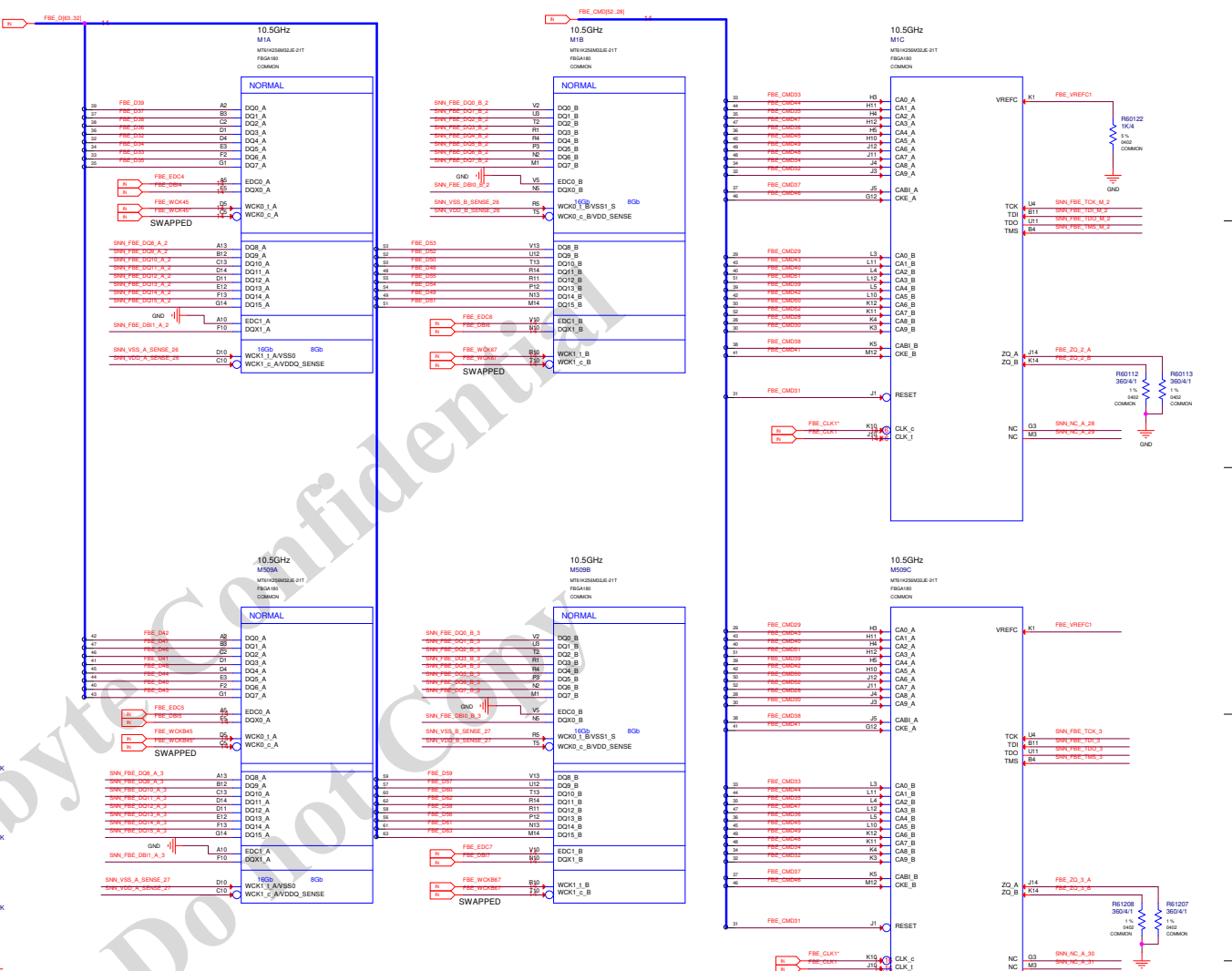
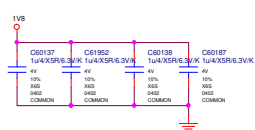
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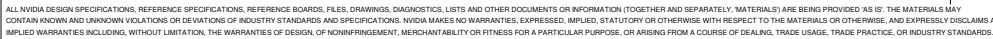


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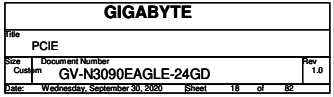


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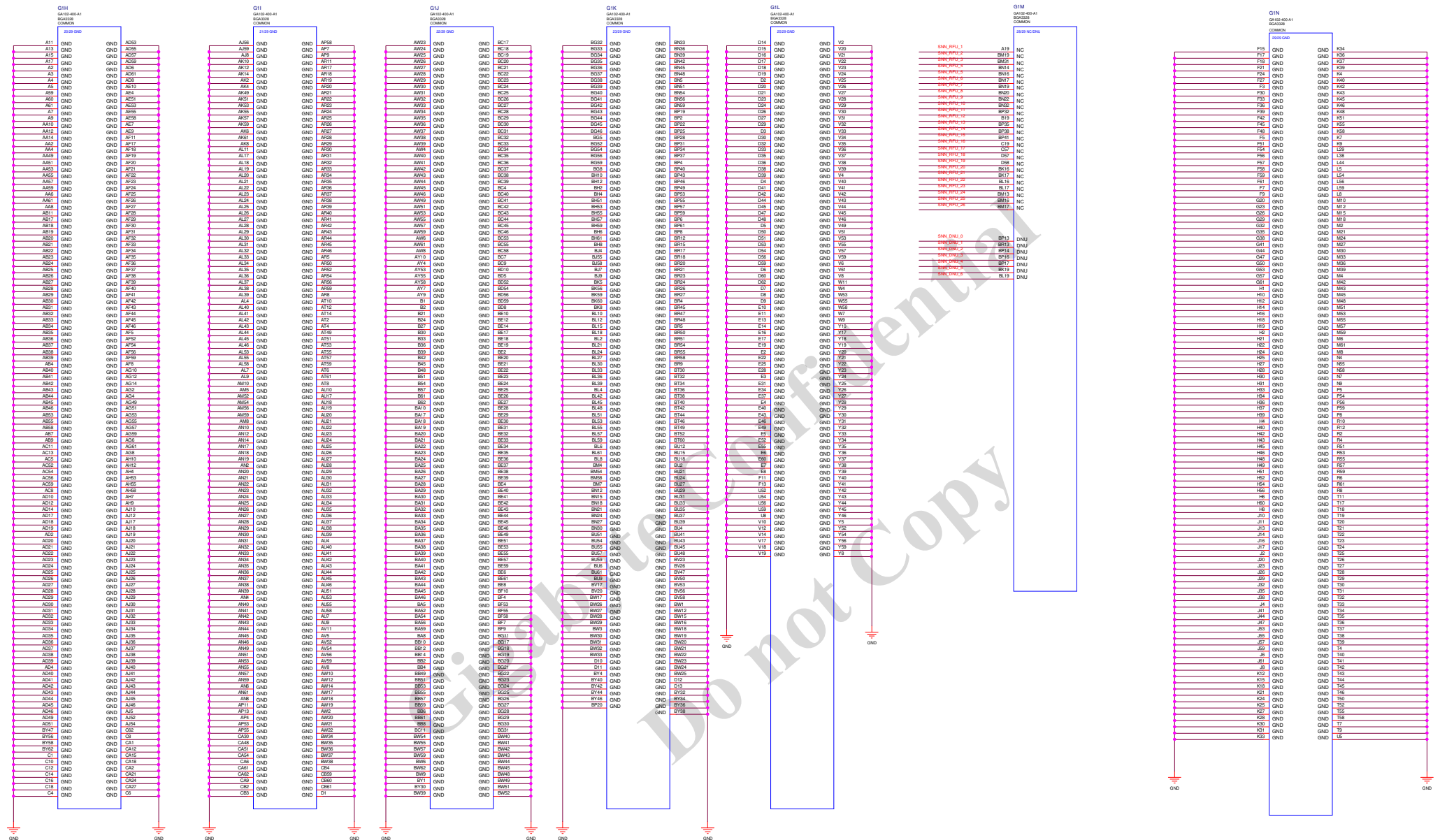




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## GPU GND, RFUs &amp; RSVD



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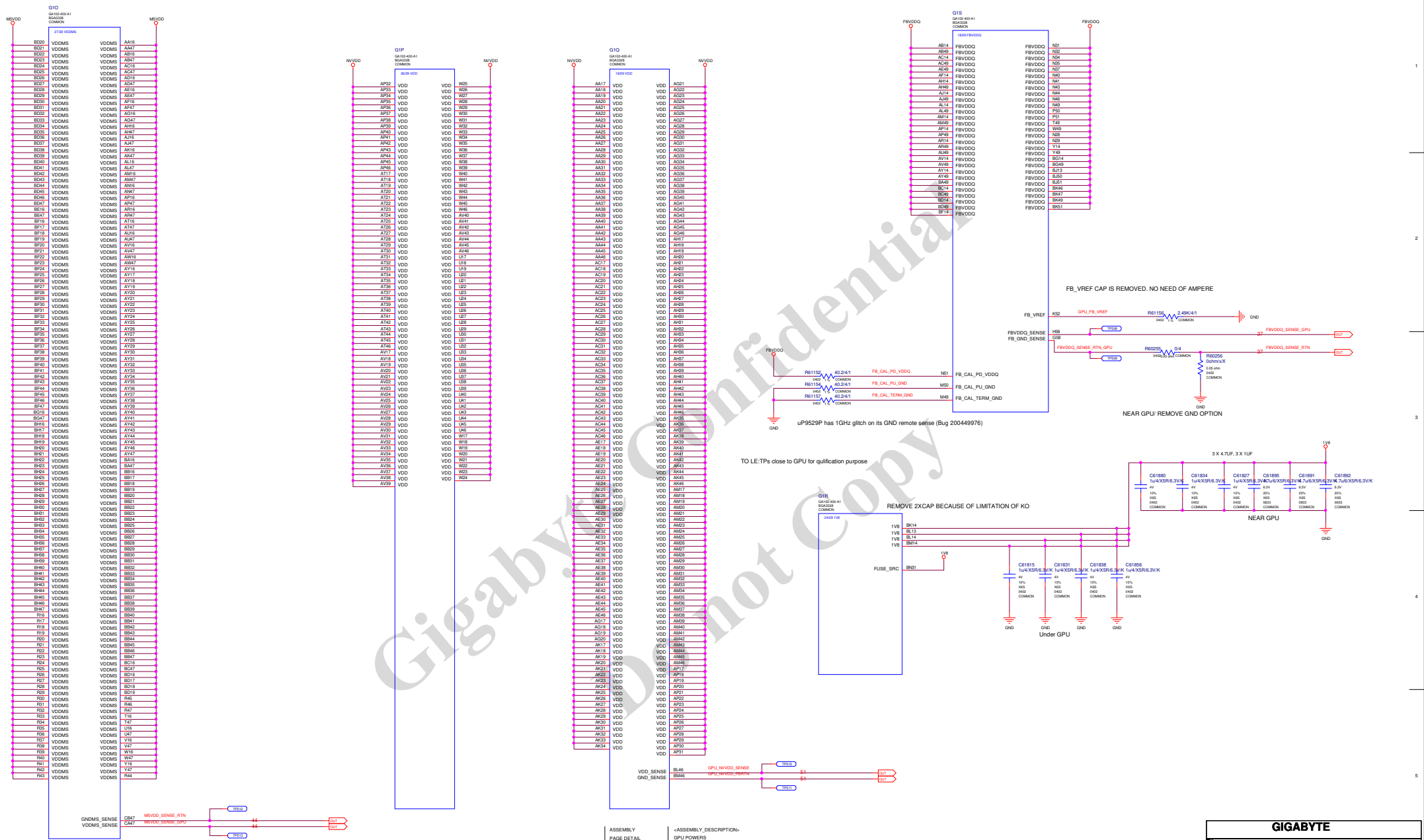
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## GPU PWR and GND

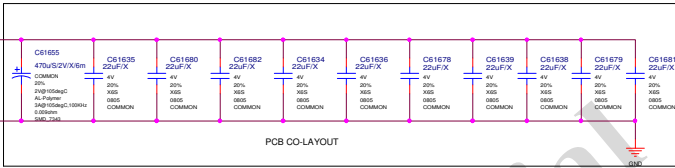
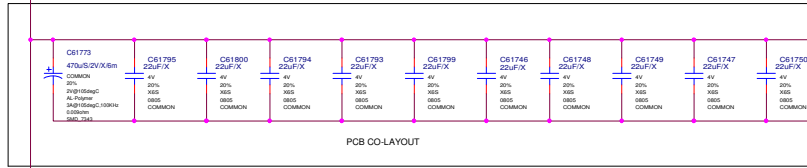


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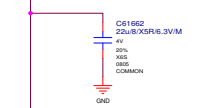
## NVVDD

## UNDER GPU

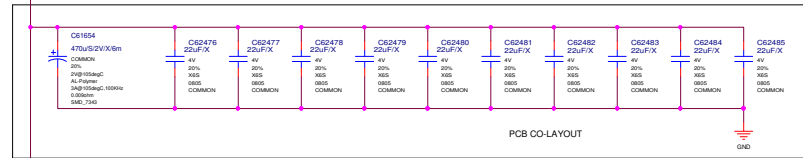
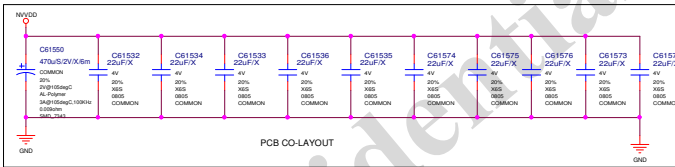
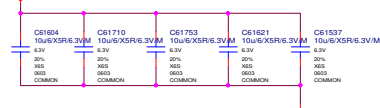
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1x 0805 22uF

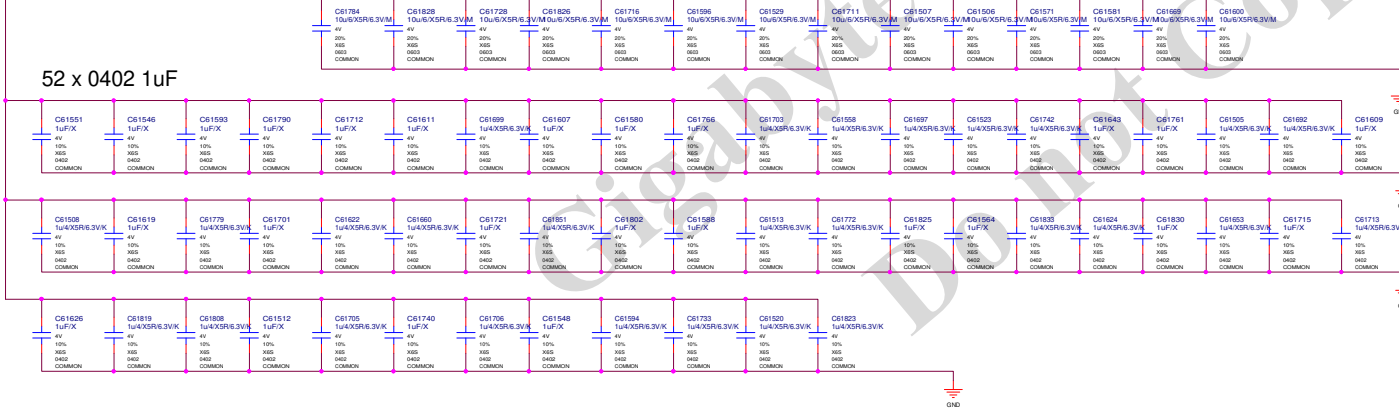


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14x 0603 10uF

52 x 0402 1uF



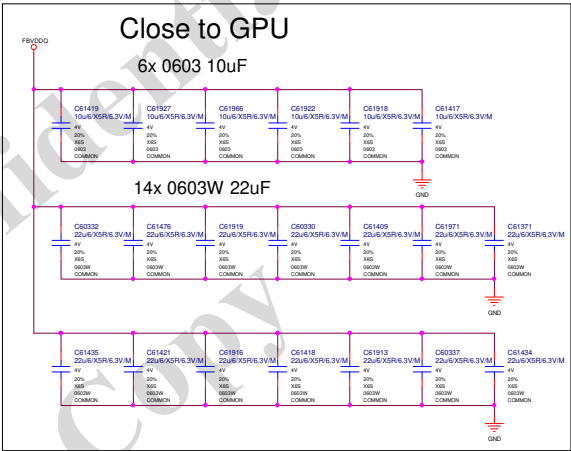
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ASSEMBLY  
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GPU NVVDD DECOUPLING

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FBVDDQ



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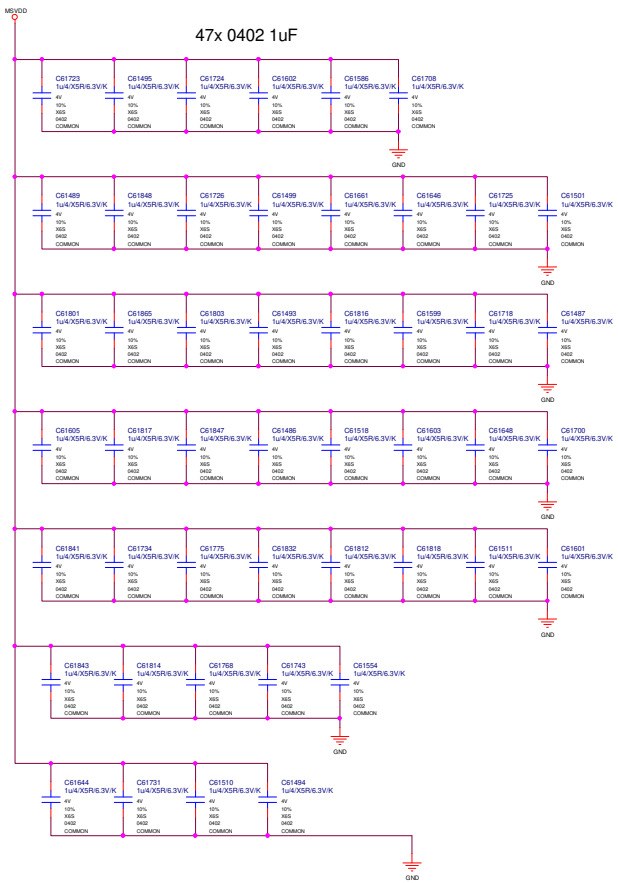
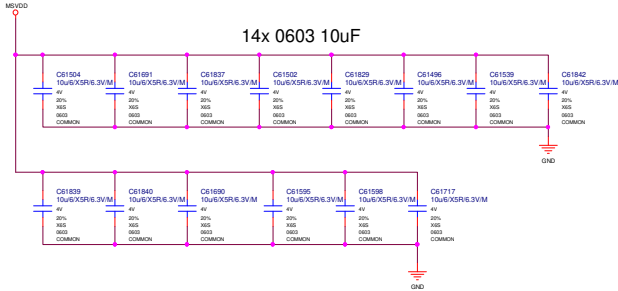
ASSEMBLY  
PAGE DETAIL

ASSEMBLY DESCRIPTION  
GPU: FBVDD DECOUPLING

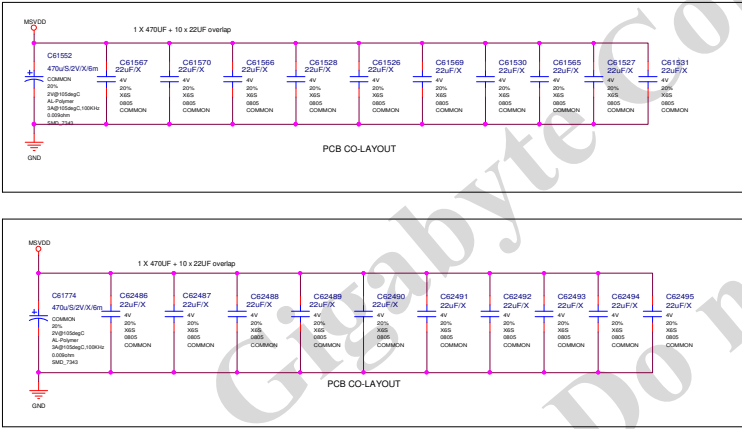
GIGABYTE			
Title			
PCIE			
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UNDER GPU

MSVDD



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

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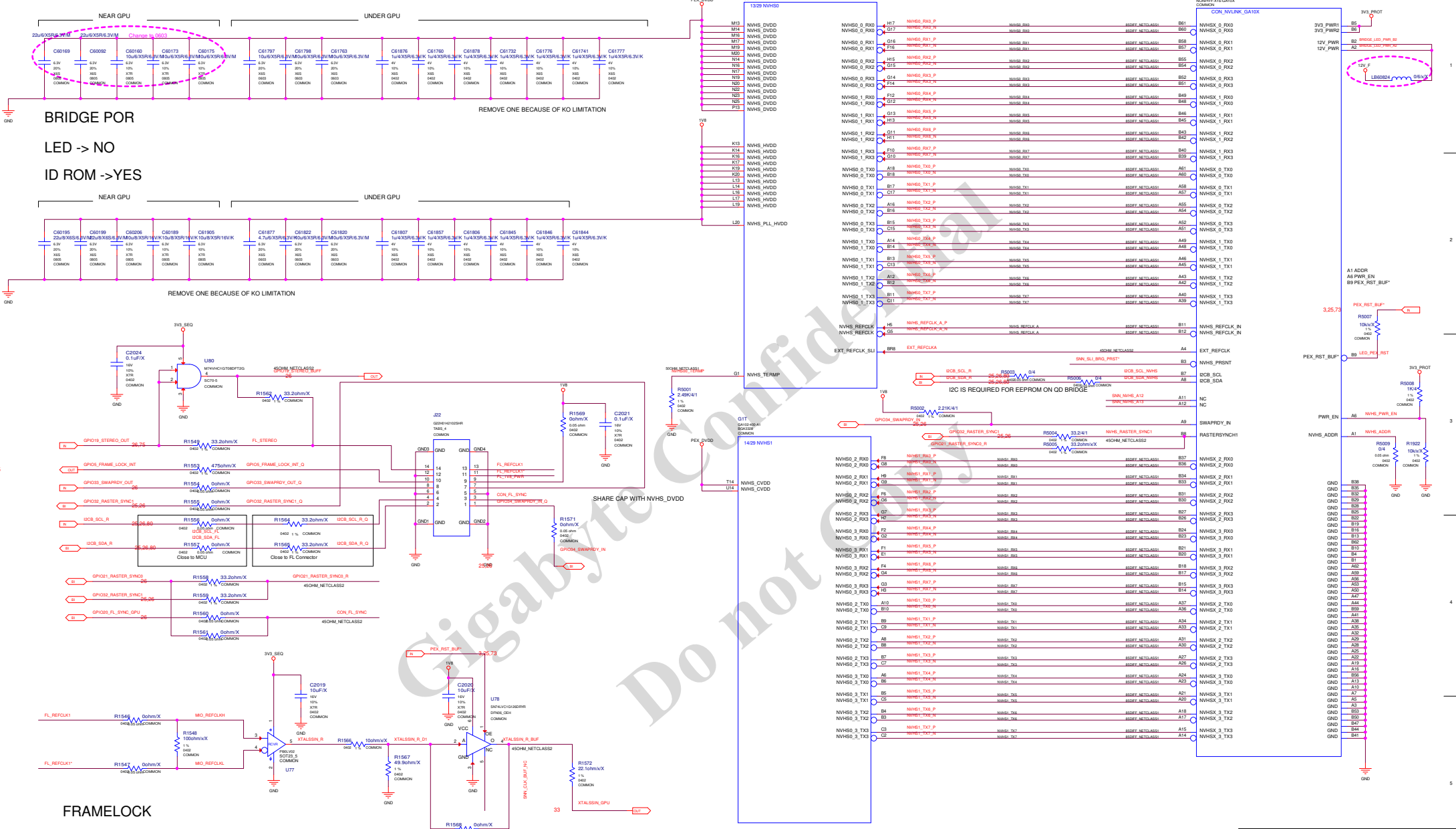
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ASSEMBLY PAGE DETAIL  
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GIGABYTE			
Title			
PCIE			
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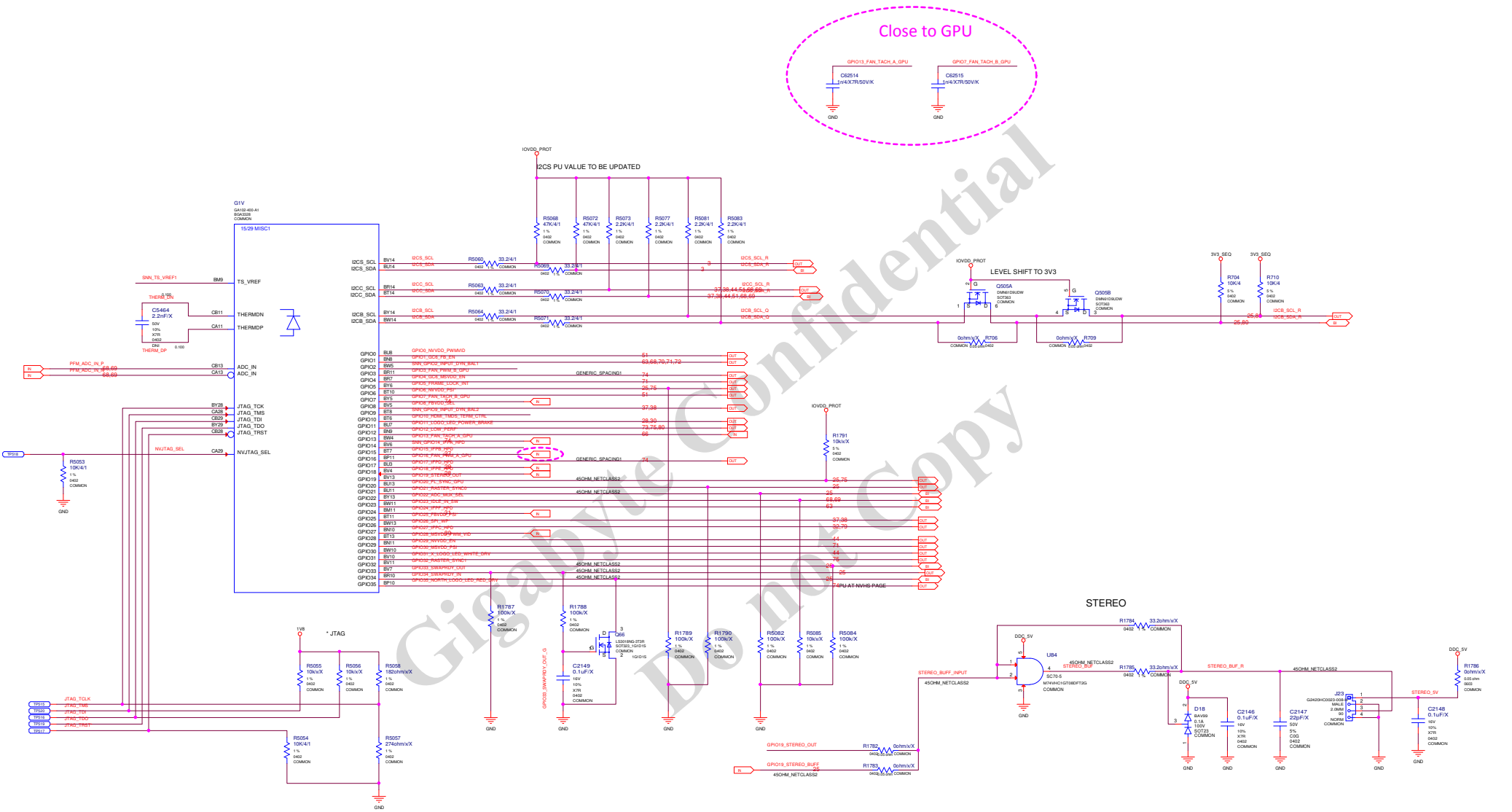


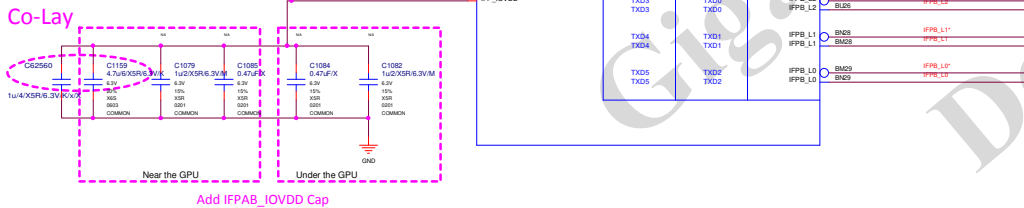
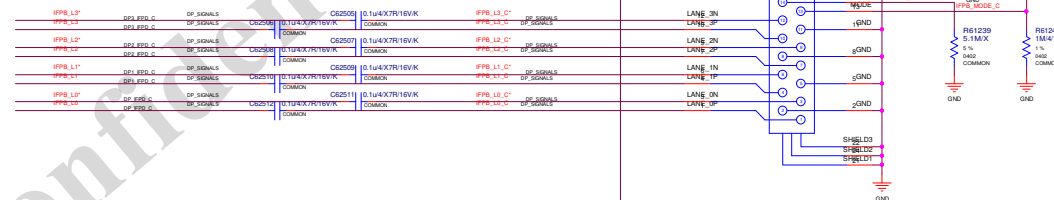
## NVHS Interface and FRAME LOCK



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MISC1: Fan, Thermal, JTAG, GPIO, STEREO



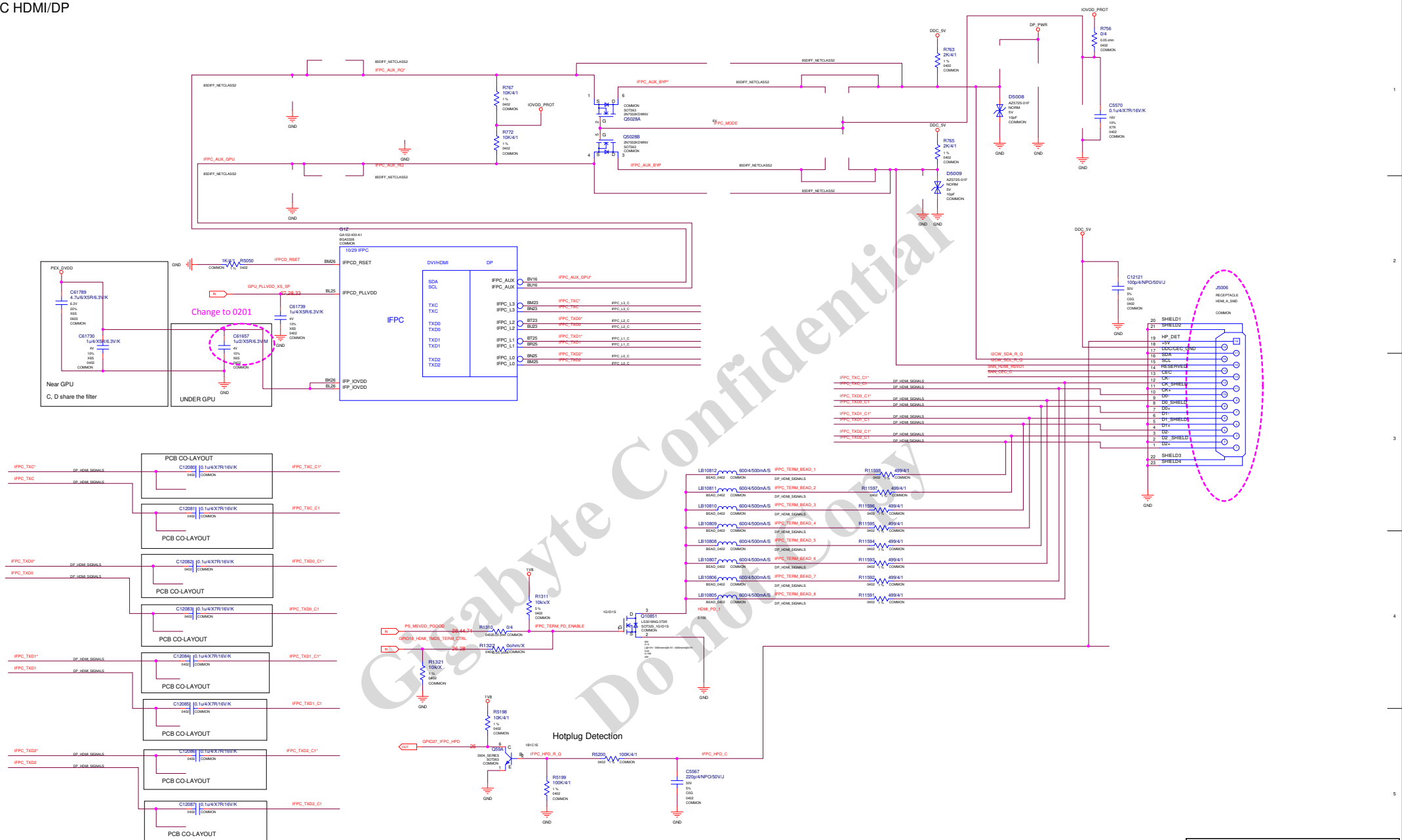




Title			
PCIE			
Size	Document Number		
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## IFPC HDMI/DP



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MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb 19Gbps
L	H	L	00010	RAMCFG TBD
H	L	L	00100	RAMCFG TBD
H	L	H	00101	RAMCFG TBD
H	L	H	00101	RAMCFG MICRON 8Gb 21Gbps

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

DEFAULT

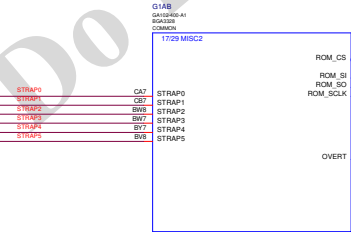
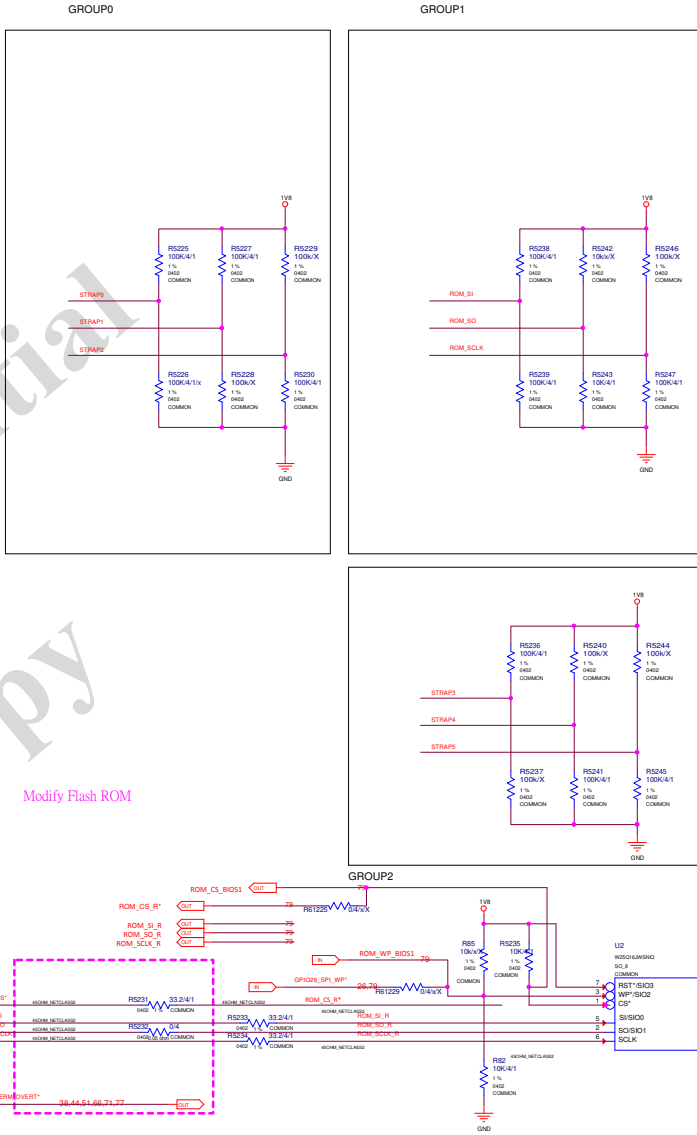
ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	H	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

- 1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

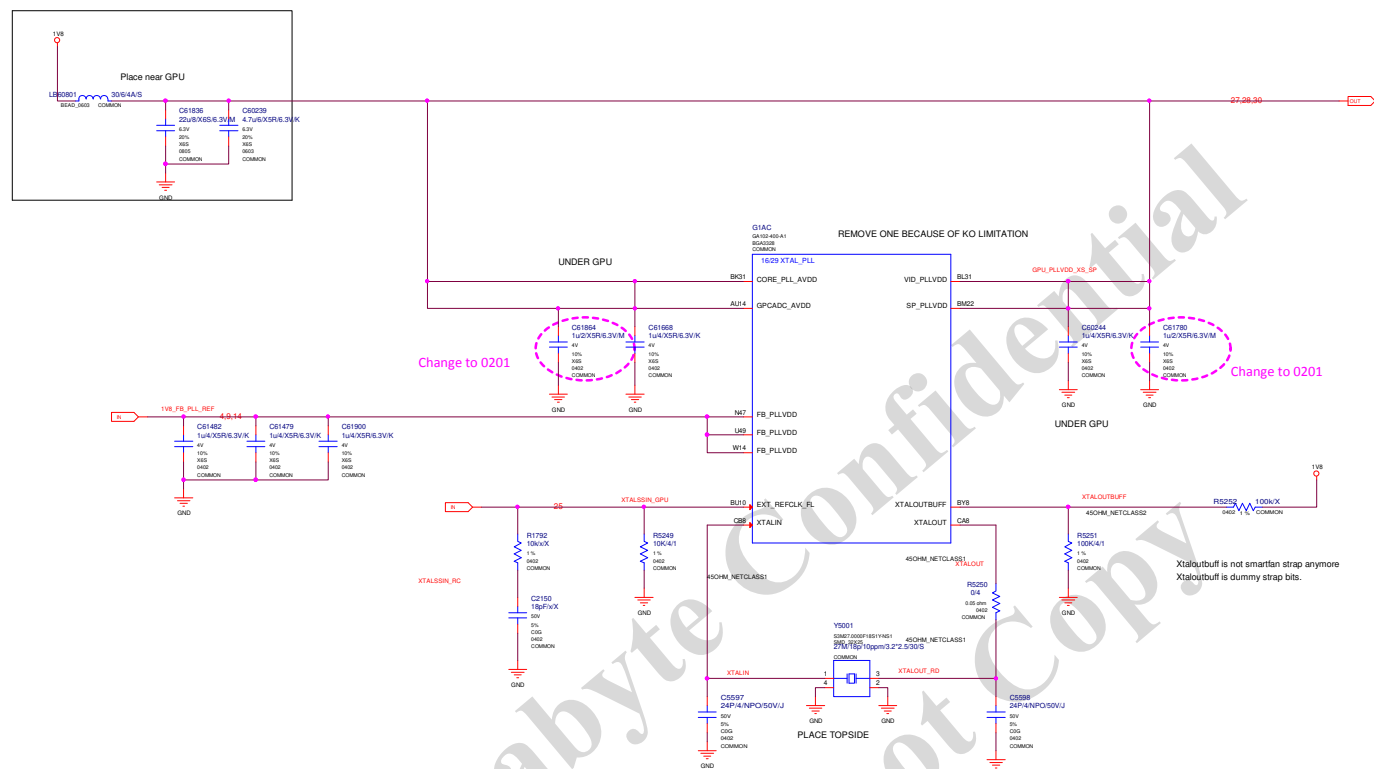


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ASSEMBLY PAGE DETAIL  
-ASSEMBLY DESCRIPTION-  
MISC ROM, STRAPS

GIGABYTE			
PCIE			
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C61780  
 1u2:XSr6.3V3M  
 4V  
 12%  
 N55  
 0402  
 QIMAMON  
 R5252  
 0402

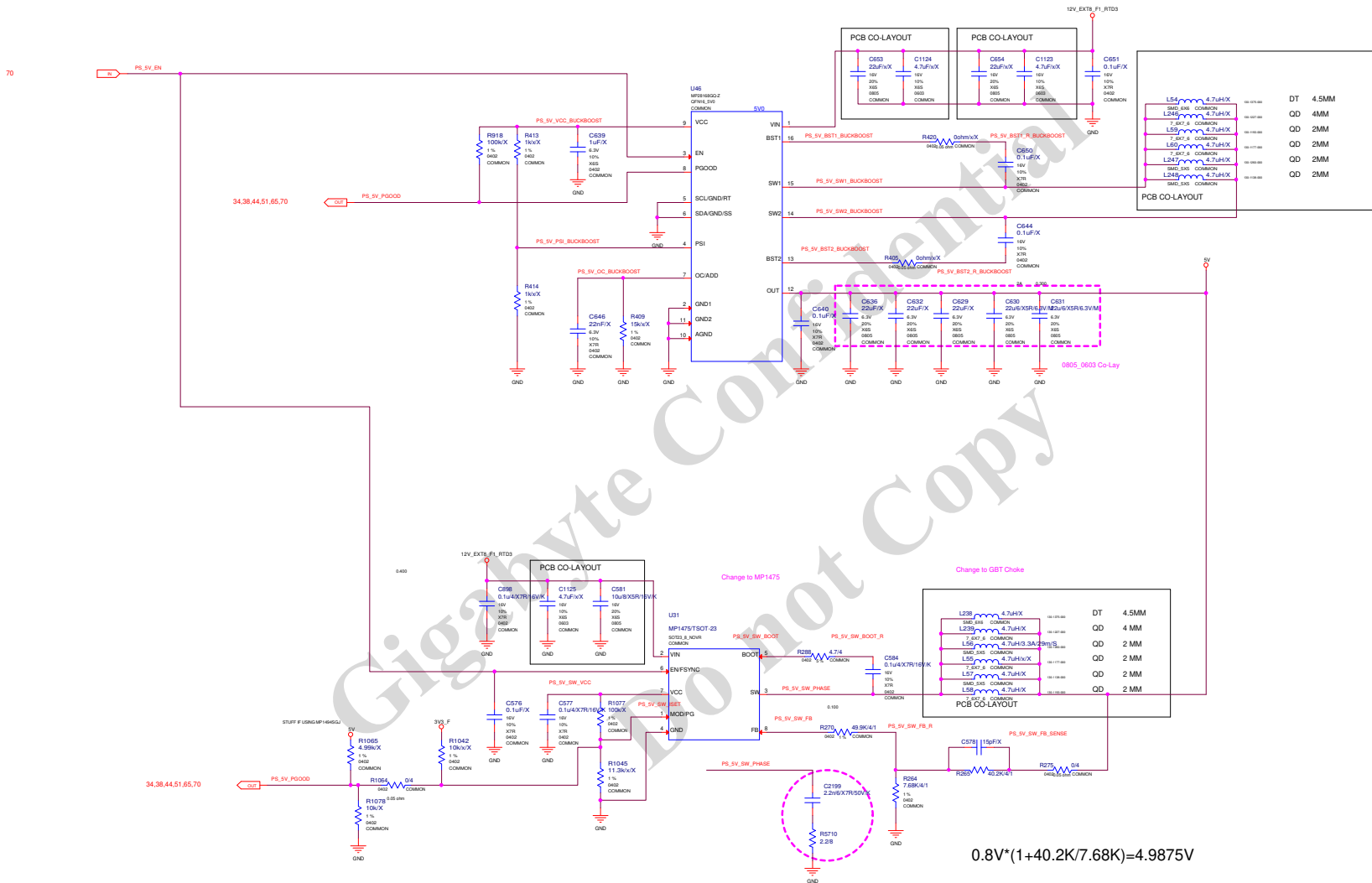
Xtaloutbuff is not smartfan strap anymore  
Xtaloutbuff is dummy strap bits.

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC. XTAL. PLL

**GIGABYTE**

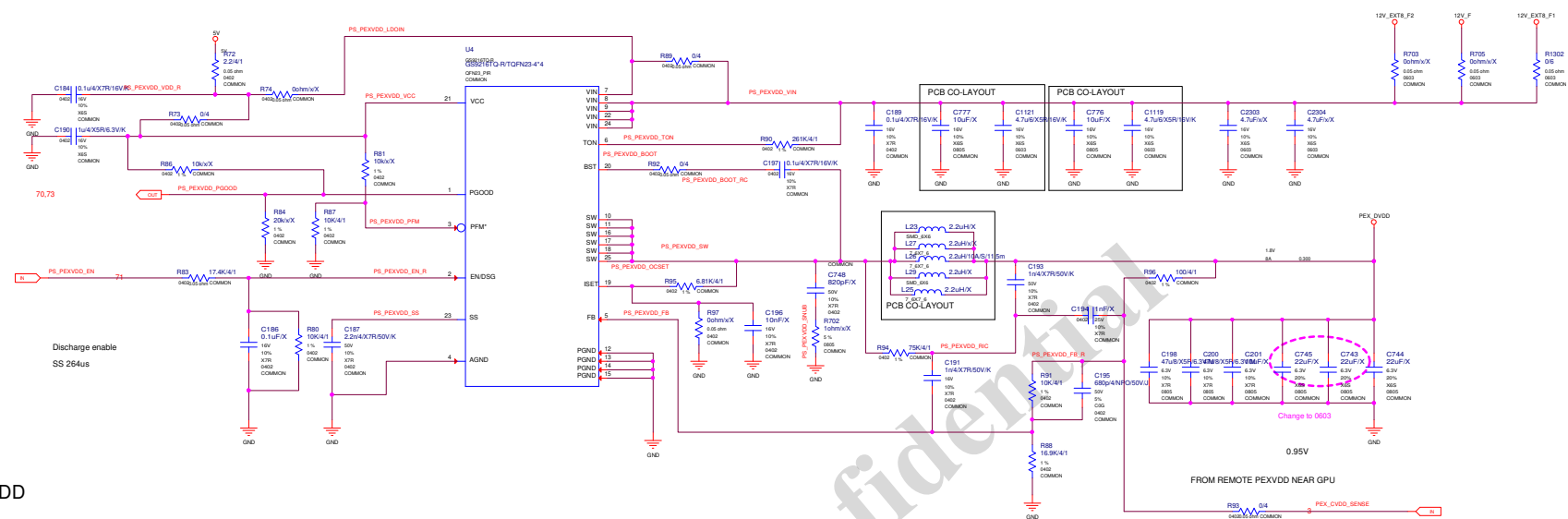
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Size	Document Number	Rev	
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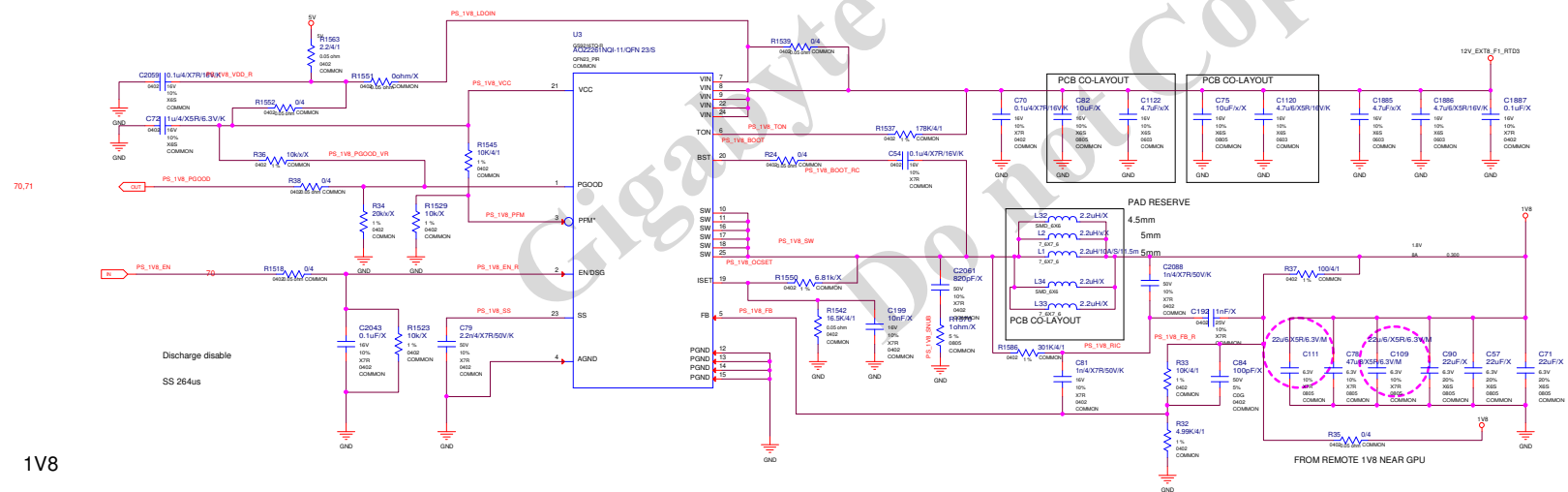
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ASSEMBLY PAGE DETAIL  
PS: 5V

GIGABYTE			
File	PCIE		
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PEX\_DVDD



1V8

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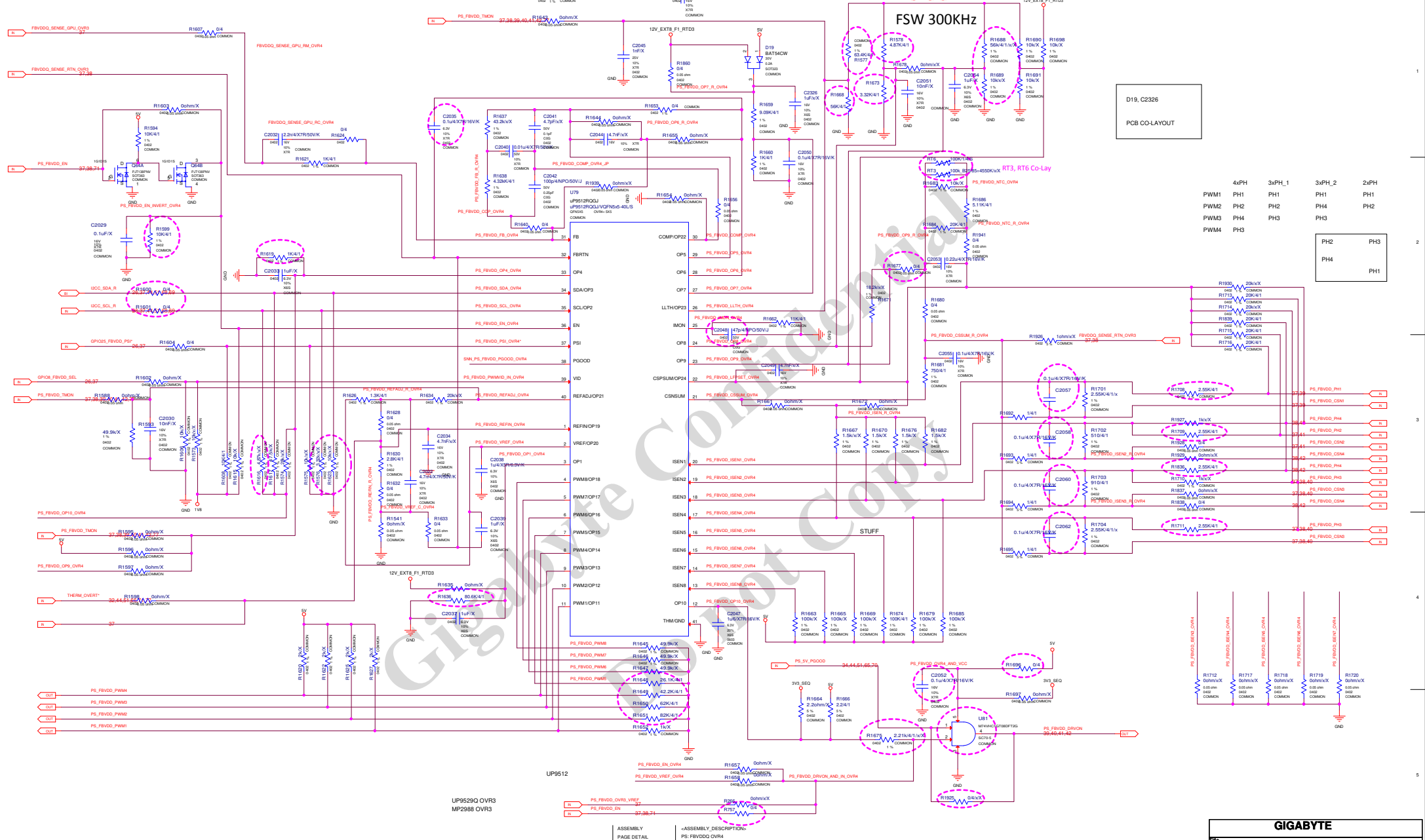
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PAGE DETAIL

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GIGABYTE			
file PCIE			
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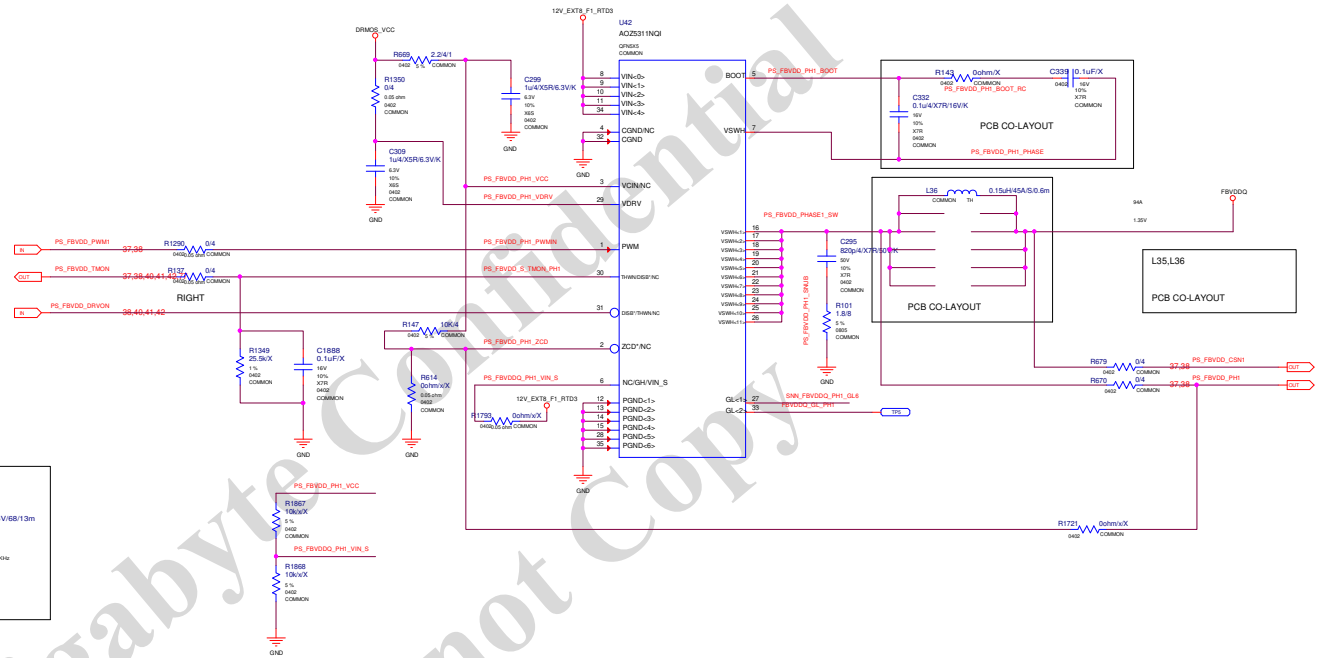
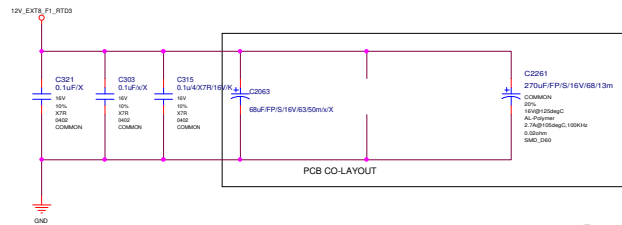
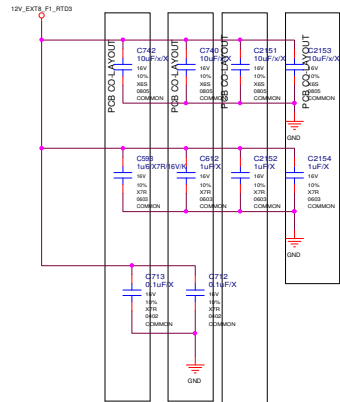
# PS:FBVDDQ OVR4



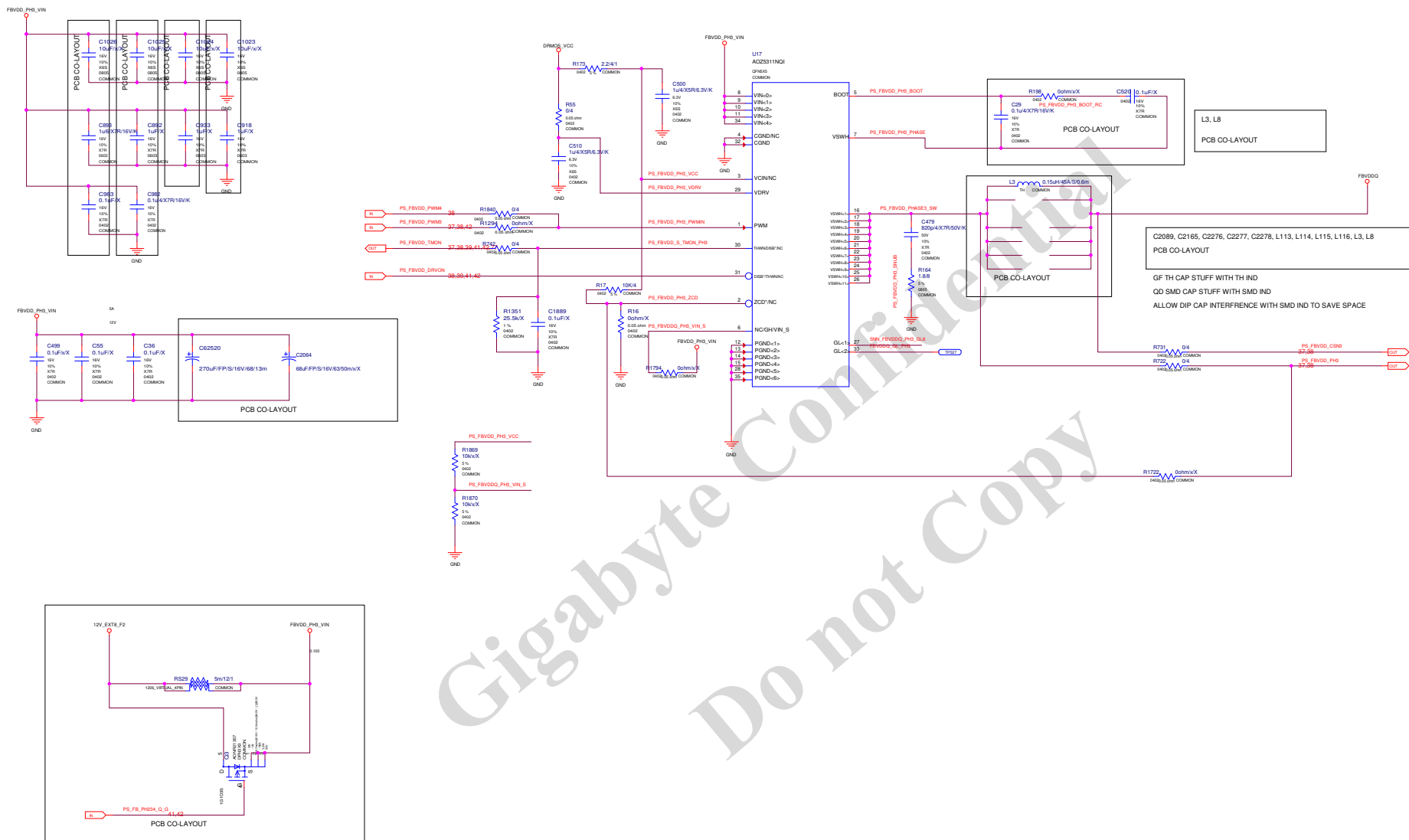
D19, C2326  
PCB CO-LAYOUT

	4xPH	3xPH_1	3xPH_2	2xPH
PWM1	PH1	PH1	PH1	PH1
PWM2	PH2	PH2	PH4	PH2
PWM3	PH4	PH3	PH3	
PWM4	PH3	PH4	PH1	

GIGABYTE			
File	PCIE		
Docu	Document Number		
Rev	1.0		
Date	Wednesday, September 20, 2000		
Sheet	38 of 82		



# PS: FBVDD PH3



## FBVDD PH3 INPUT ANTI-BACKDRIVE

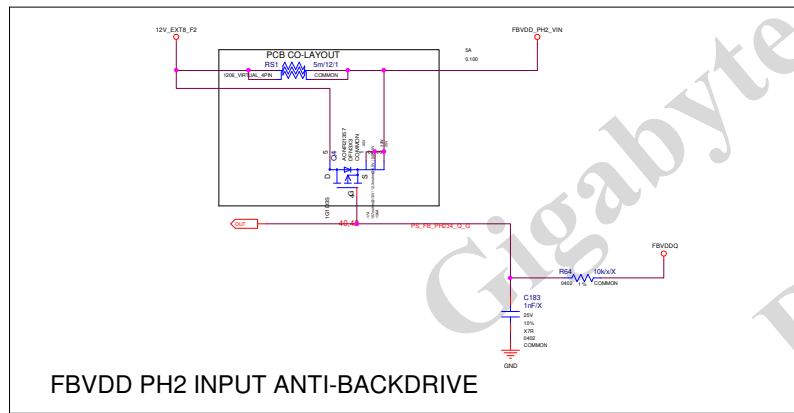
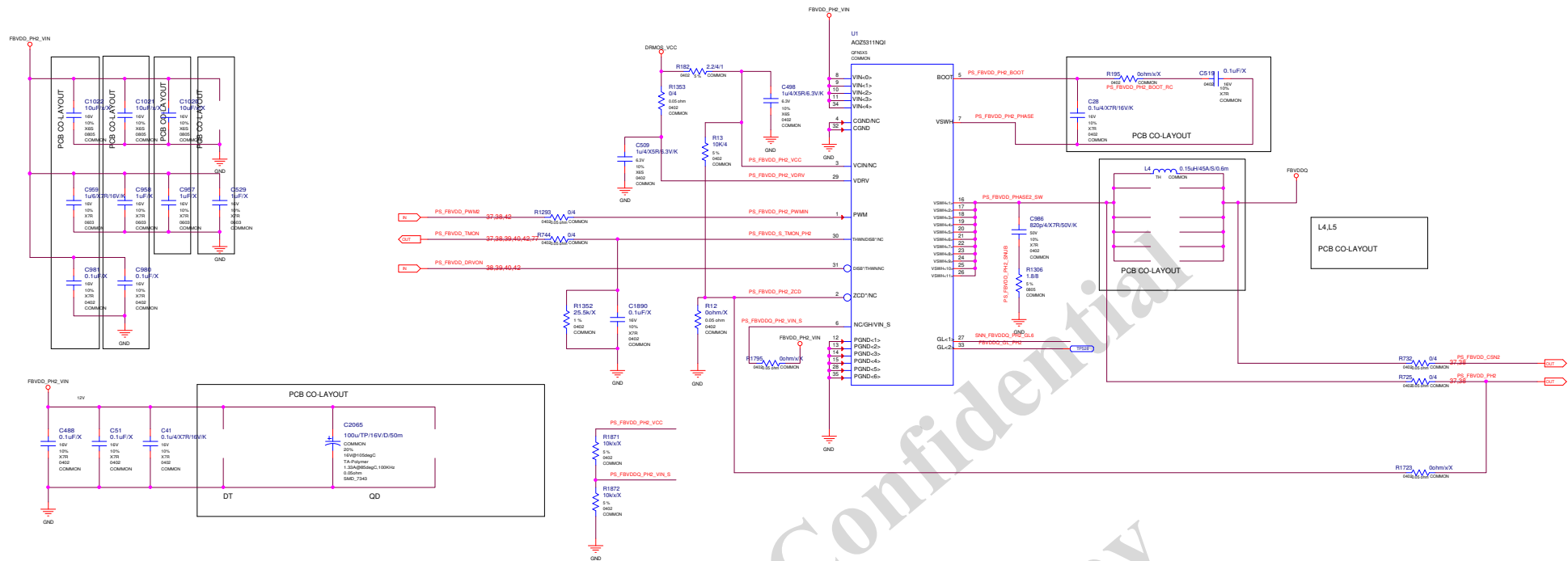
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ASSEMBLY  
PAGE DETAIL  
PS: FBVDD PH3

GIGABYTE			
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## PS: FBVDD PH2



## FBVDD PH2 INPUT ANTI-BACKDRIVE

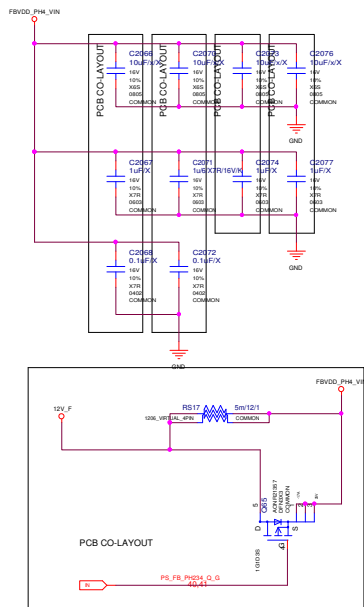
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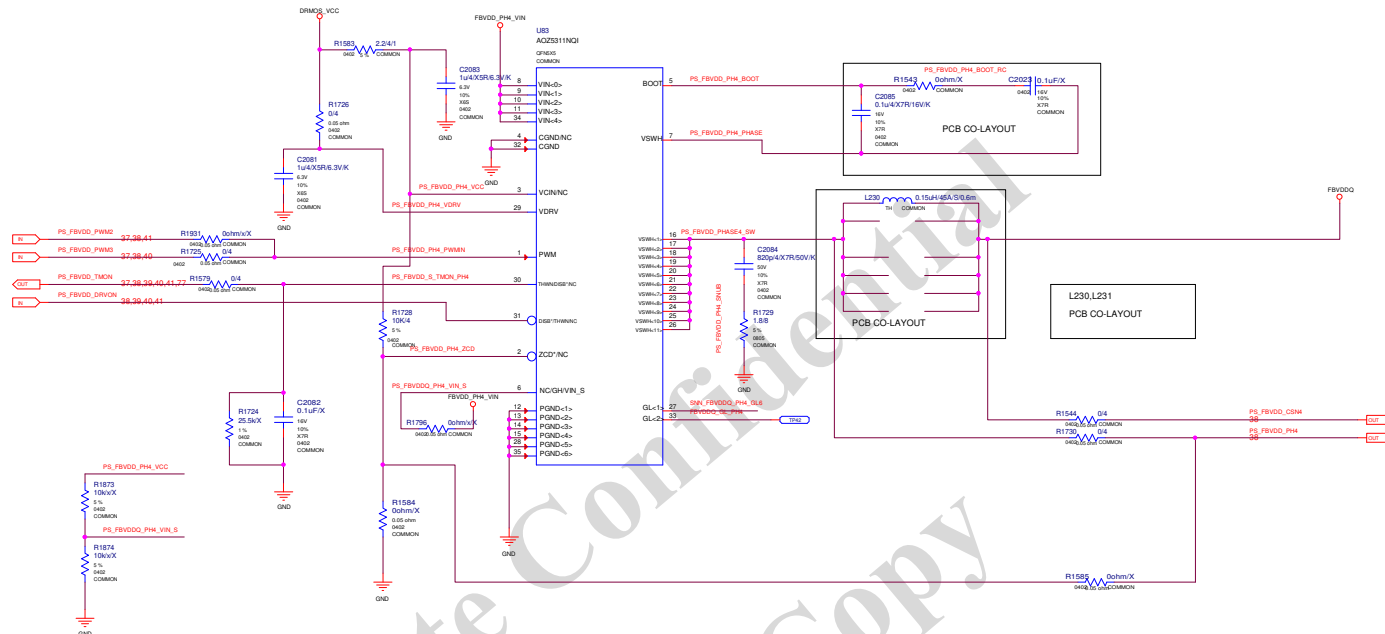
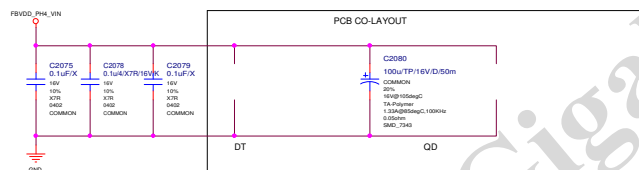
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Title: PCIE			
Size	Document Number	Rev	
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## PS: FBVDD PH4



### FBVDD PH3 INPUT ANTI-BACKDRIVE



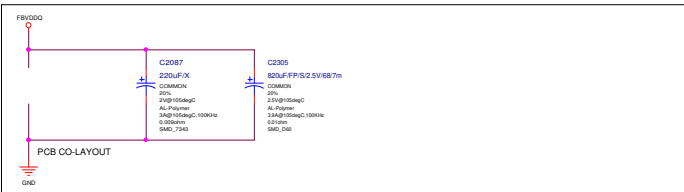
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ASSEMBLY  
PAGE DETAIL

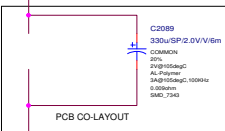
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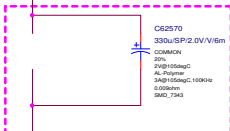
PH1 TOP



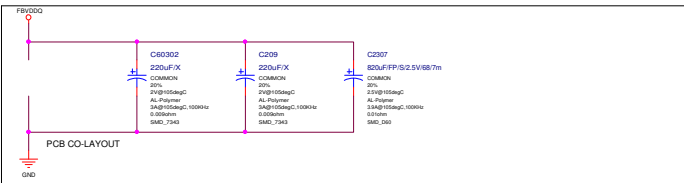
PH3 TOP



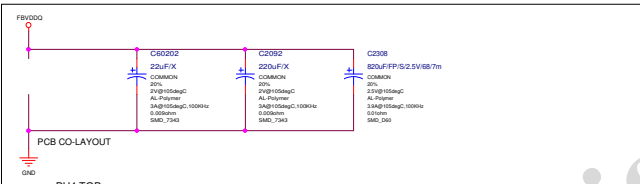
PH3 Bottom



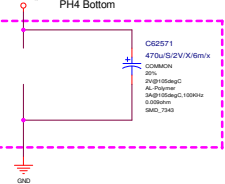
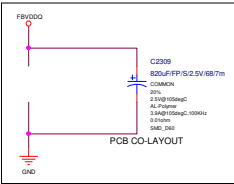
PH2 TOP



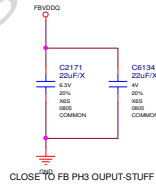
PH4 TOP



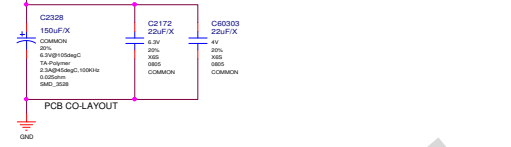
PH4 Bottom



CLOSE TO FB PH3 OUPUT-STUFF

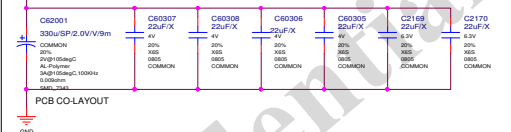


NORTHWEST BOT



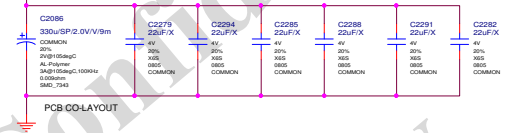
PCB CO-LAYOUT

NORTHWEST BOT



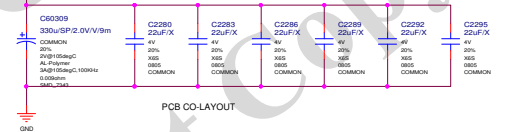
PCB CO-LAYOUT

NORTHWEST TOP



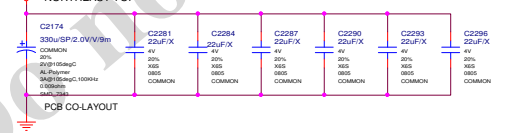
PCB CO-LAYOUT

NORTHWEST BOT



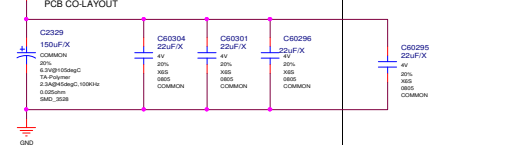
PCB CO-LAYOUT

NORTHEAST TOP

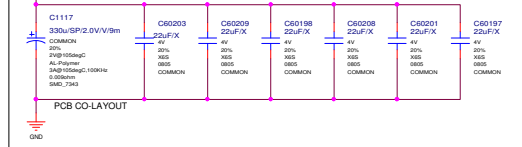


PCB CO-LAYOUT

PCB CO-LAYOUT

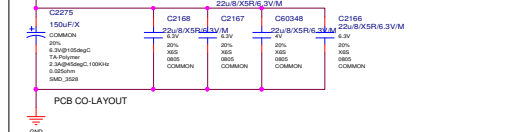


SOUTHEAST BOT



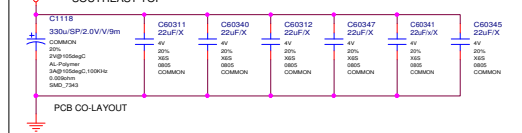
PCB CO-LAYOUT

SOUTHEAST BOT



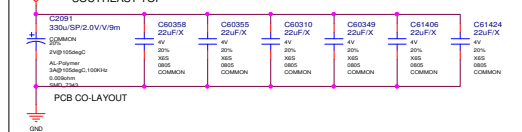
PCB CO-LAYOUT

SOUTHEAST TOP



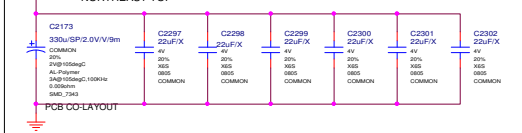
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SOUTHEAST TOP



PCB CO-LAYOUT

NORTHEAST TOP



PCB CO-LAYOUT

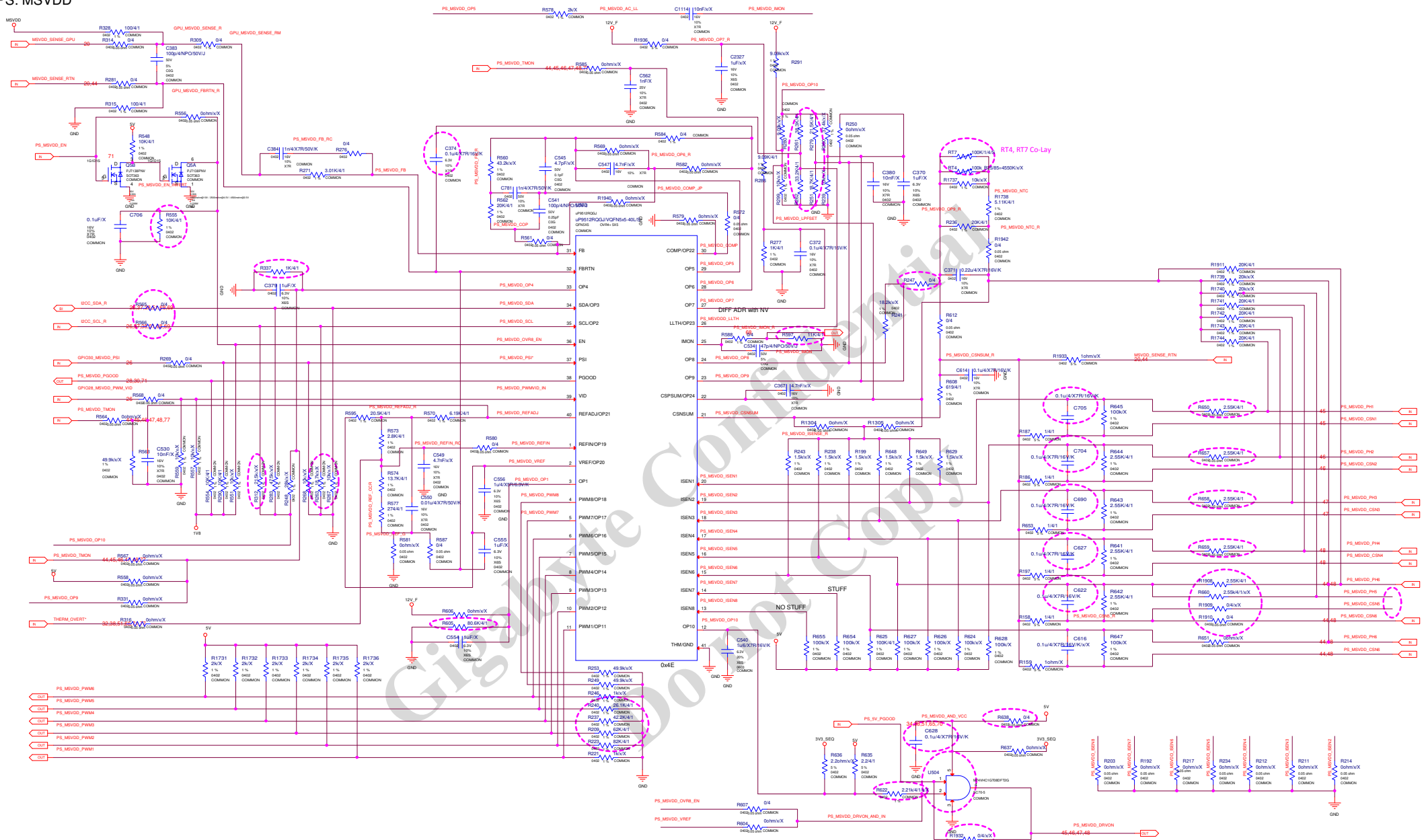
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## GIGABYTE

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## PS: MSVDD

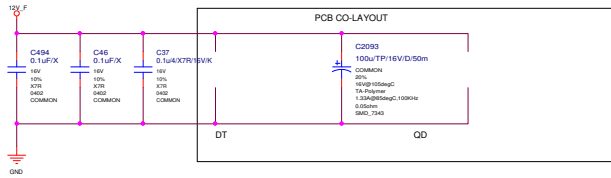


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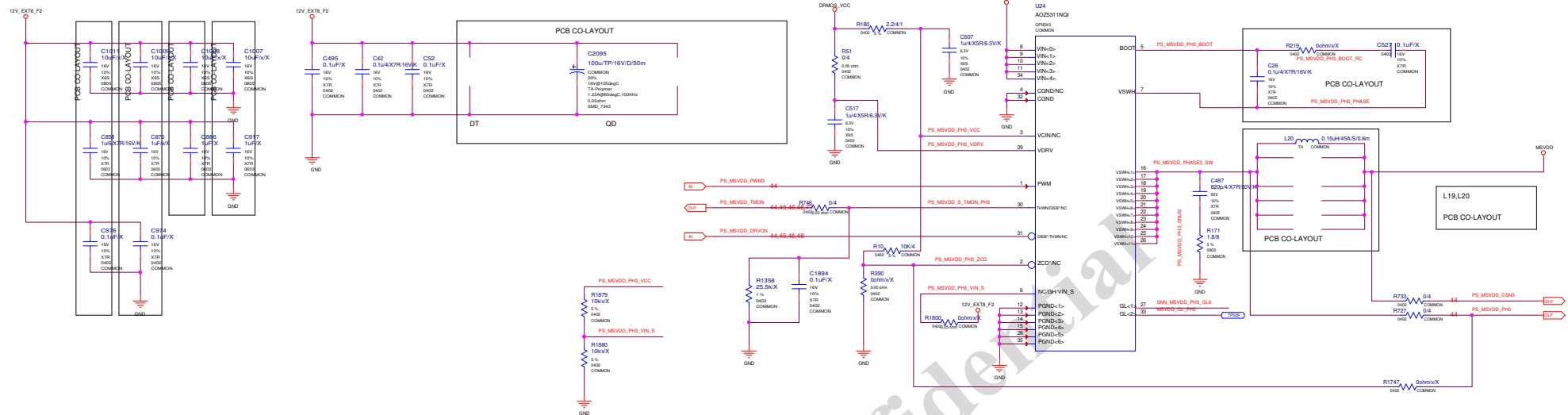
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## PS:MSVDD Phase 3, 5



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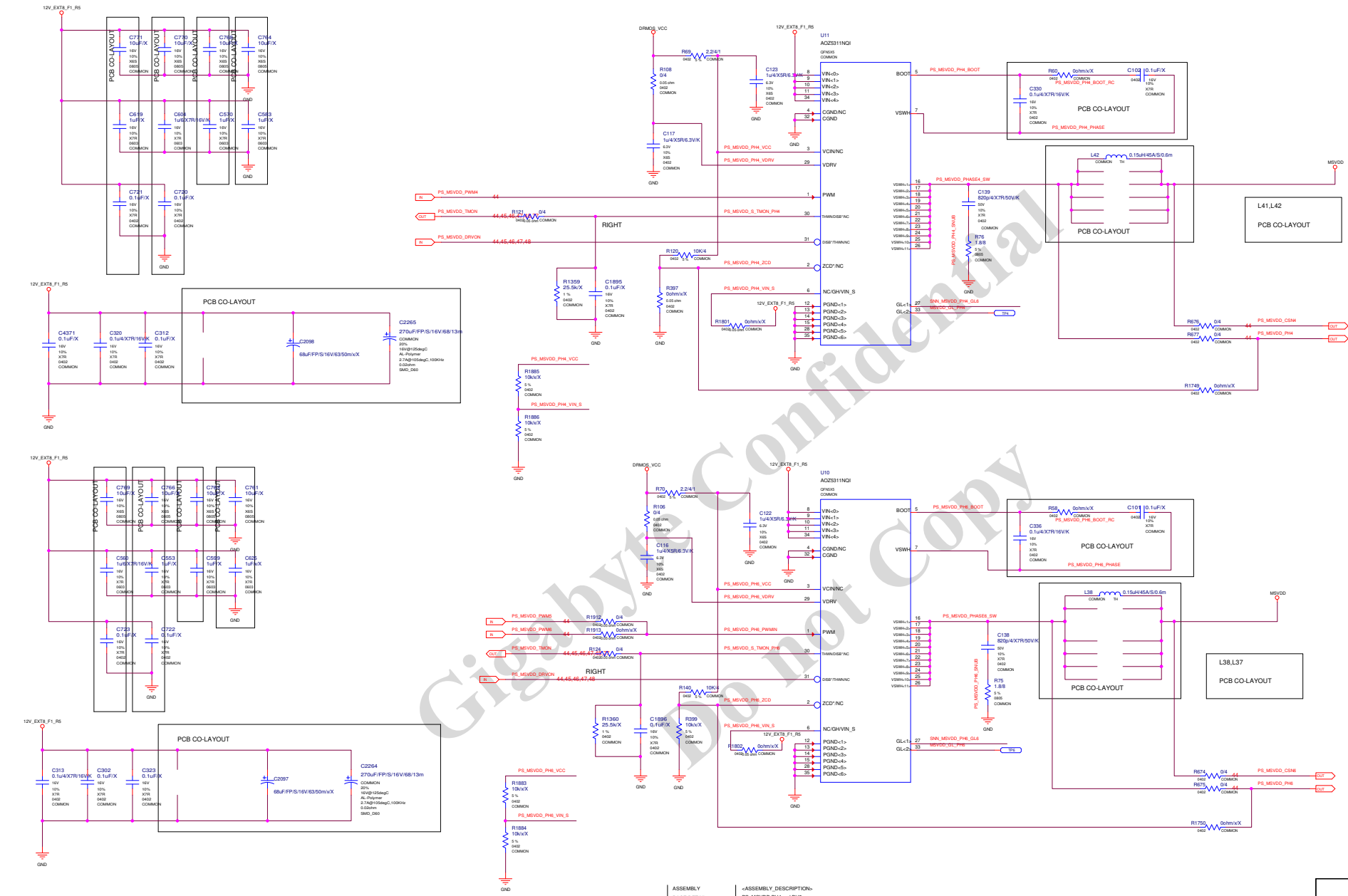
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PS: MSVDD PH 4,6

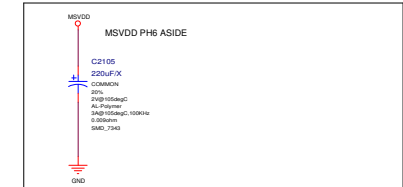
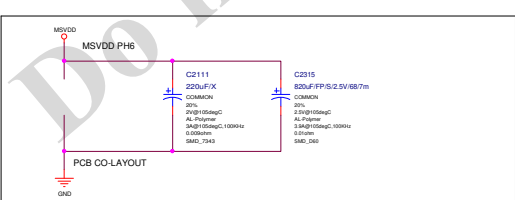
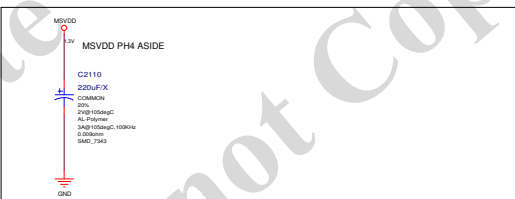
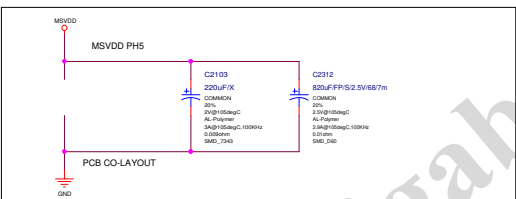
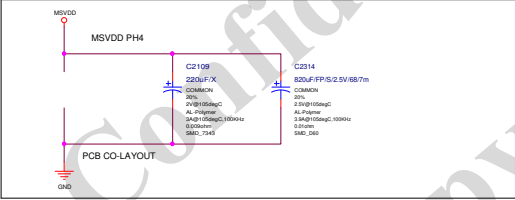
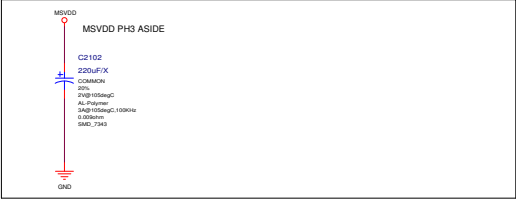
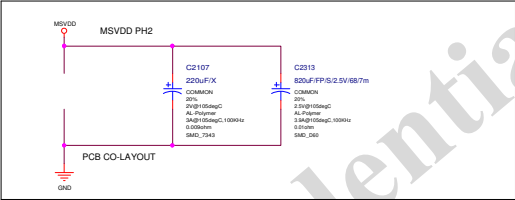
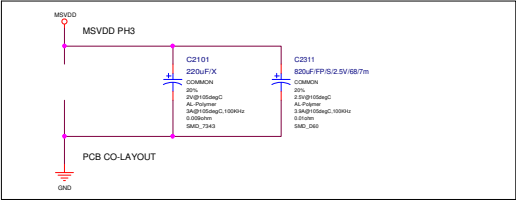
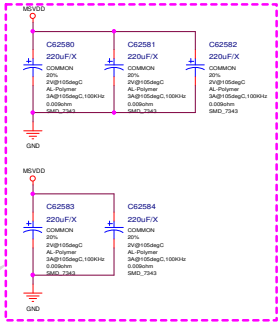
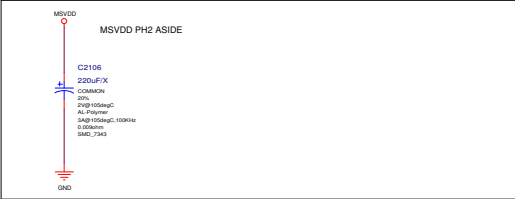
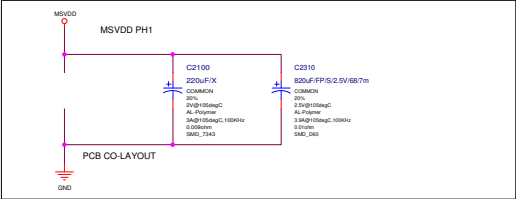


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ASSEMBLY  
PAGE DETAIL

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PS: MSVDD OUTPUT CAP(TOP)

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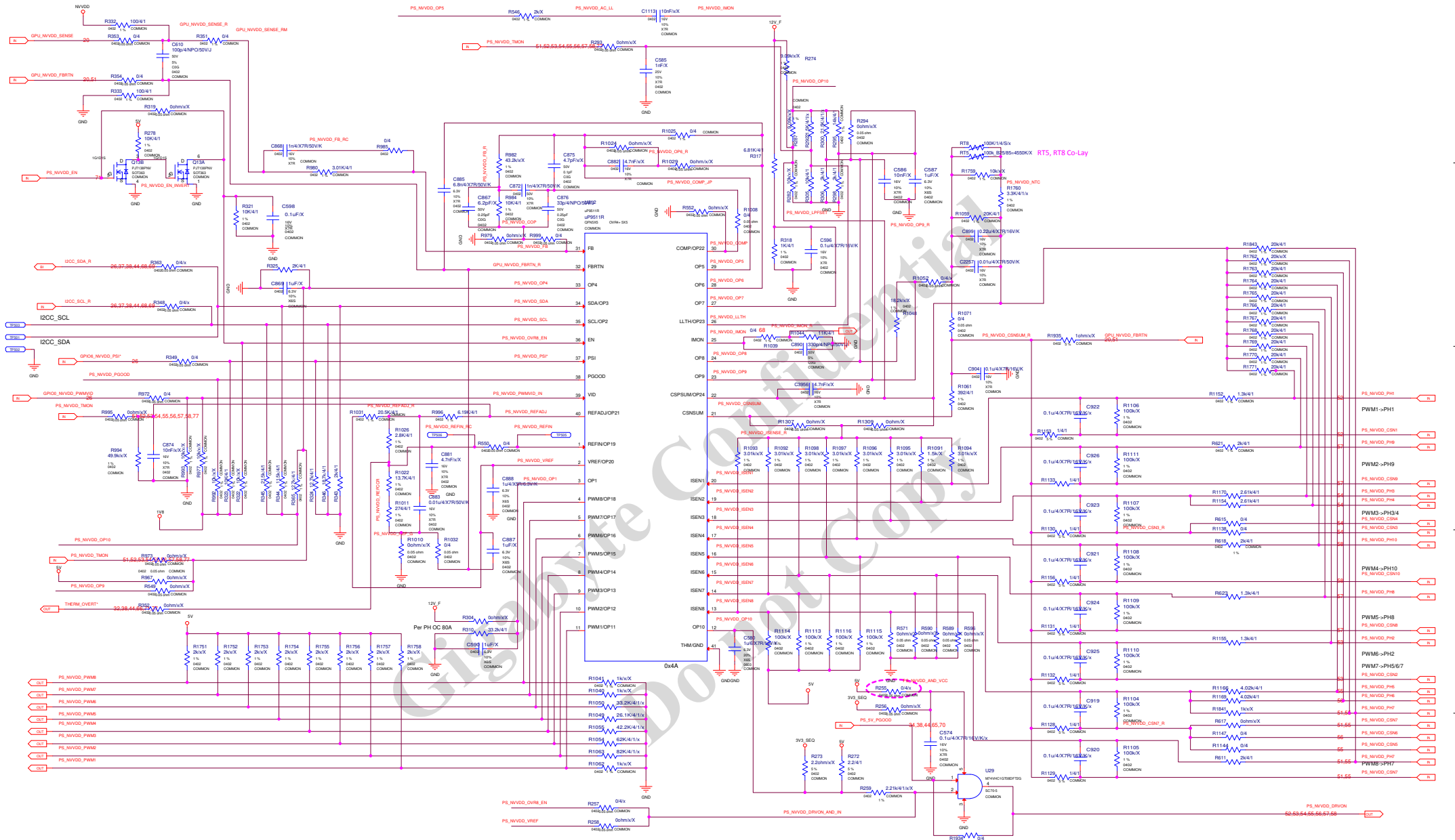
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## PS: NVVDD Controller\_OVR8



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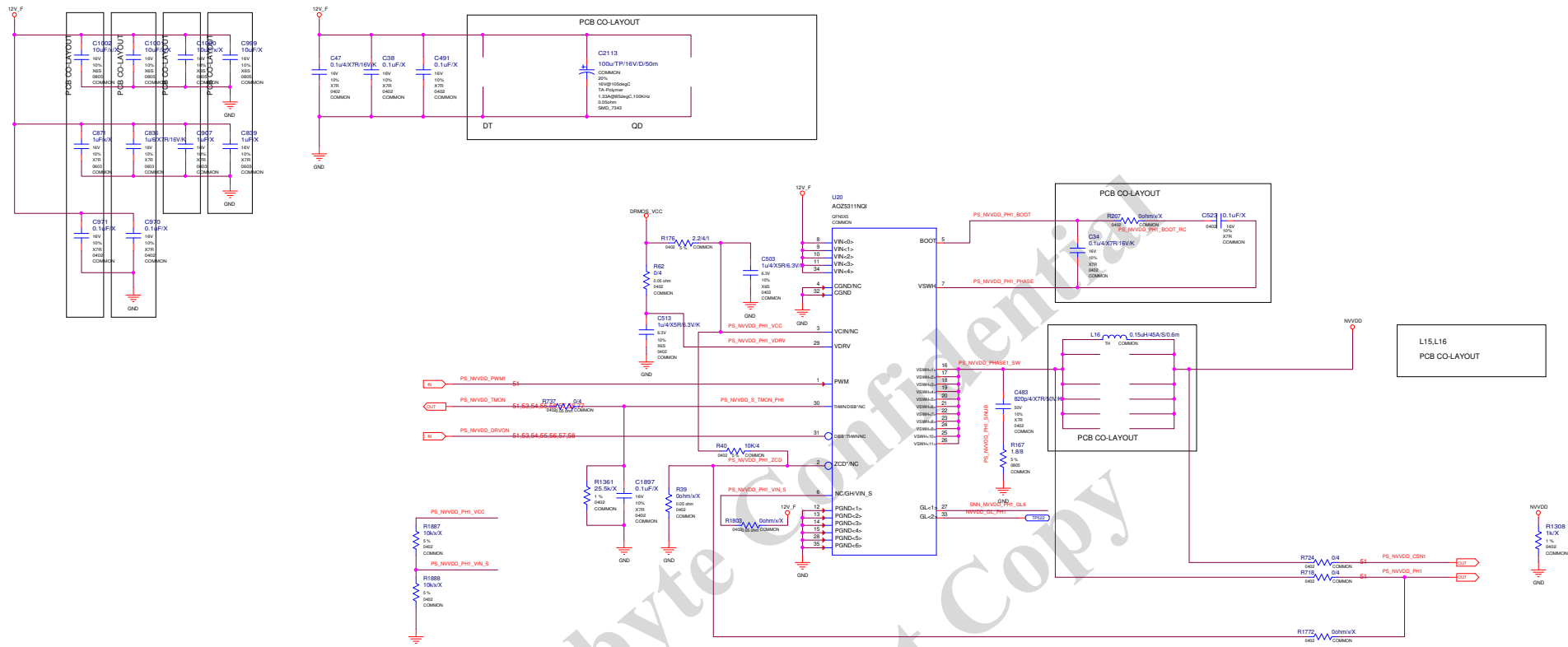
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## GIGABYTE

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## PS: NVVDD Phase 1



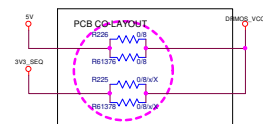
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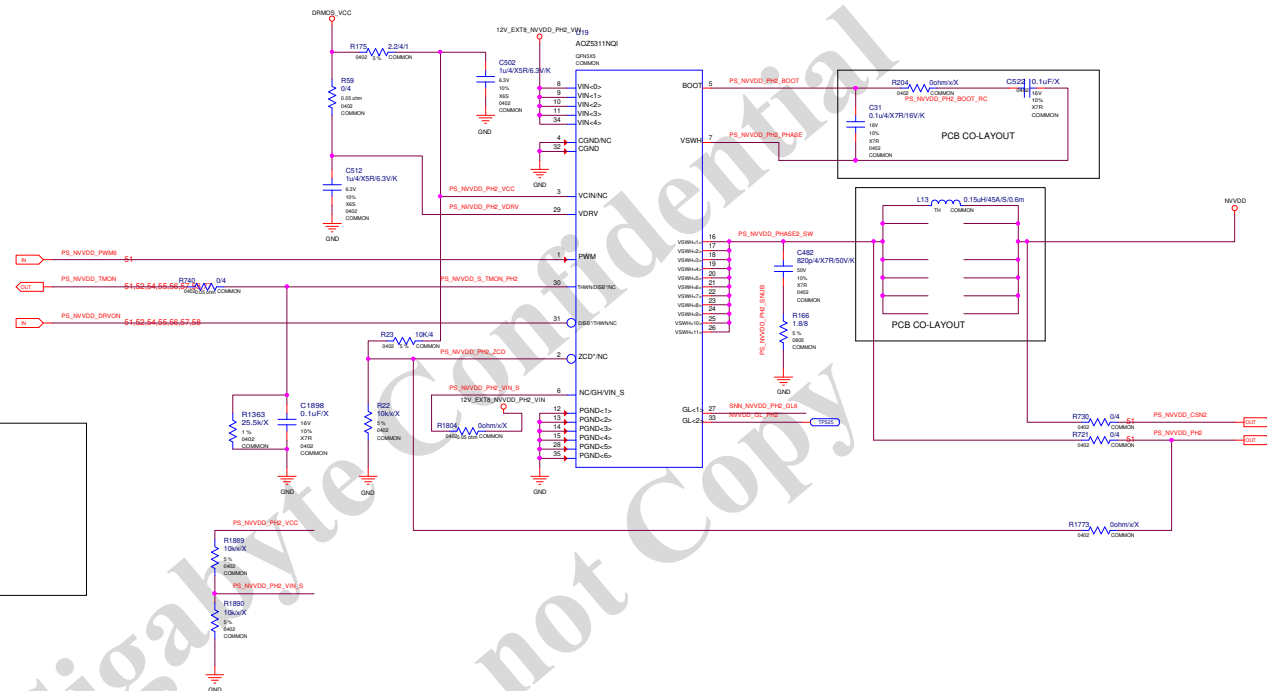
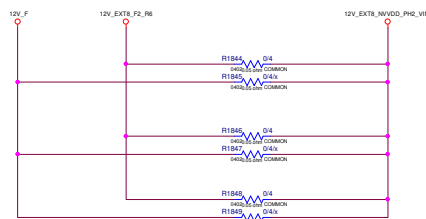
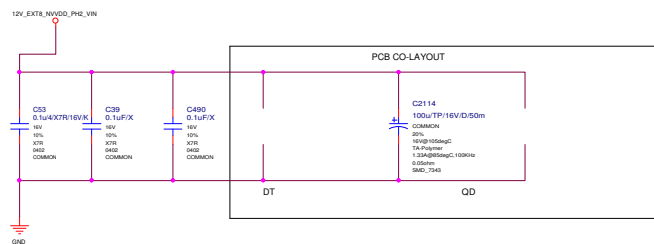
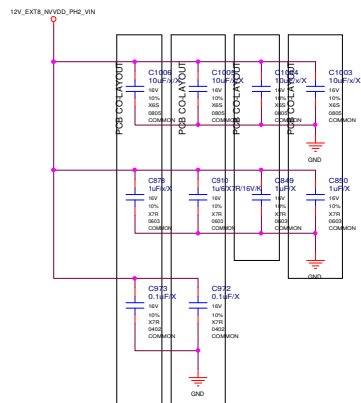
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## PS: NVVDD Phase 2 (PWM6)



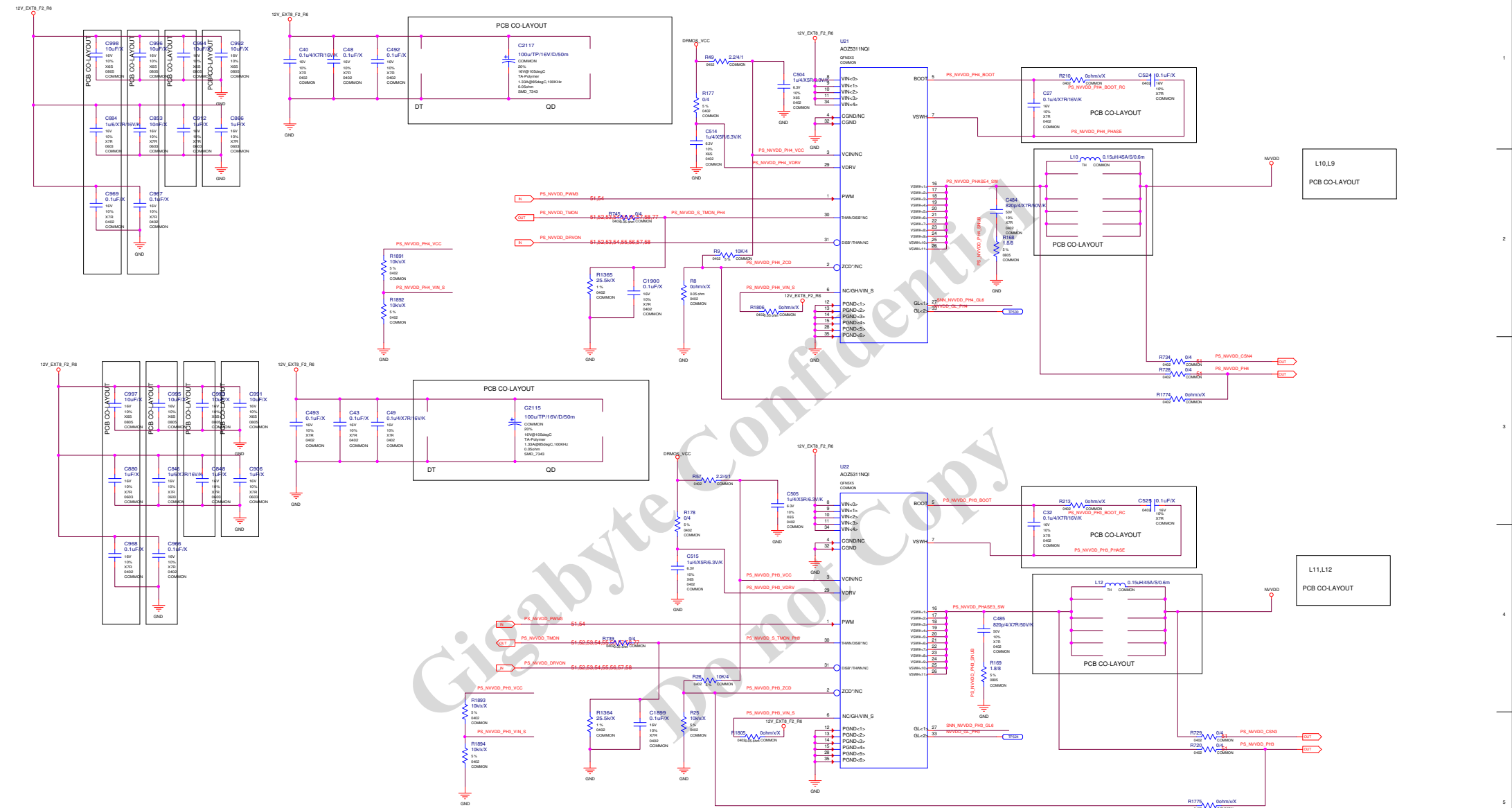
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L13,L14

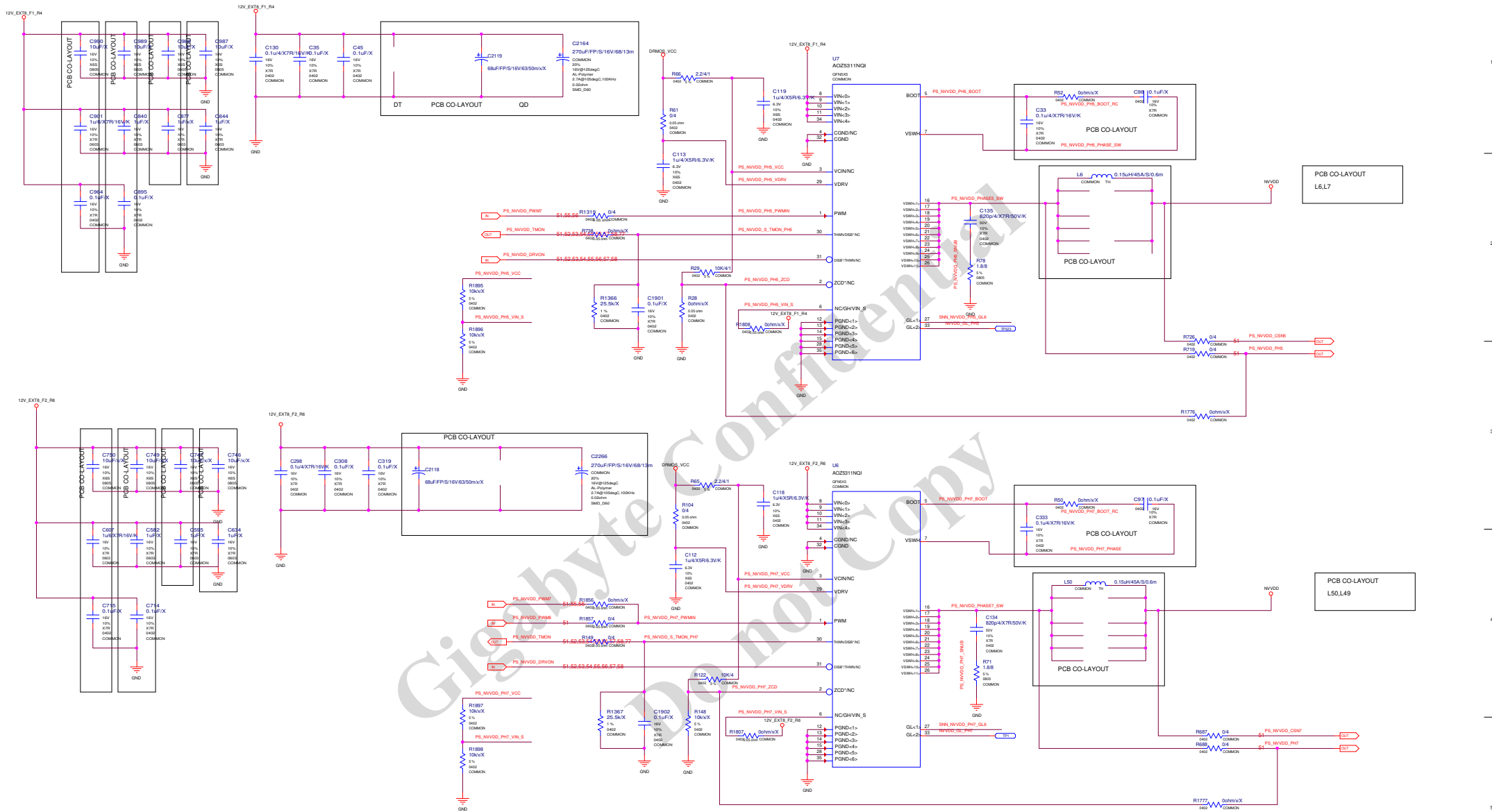
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PS: NVVDD Phase 3 (PWM3), PHASE4 (PWM3)



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## PS: NVVDD PH 5(PWM4), PH7(PWM8/4)



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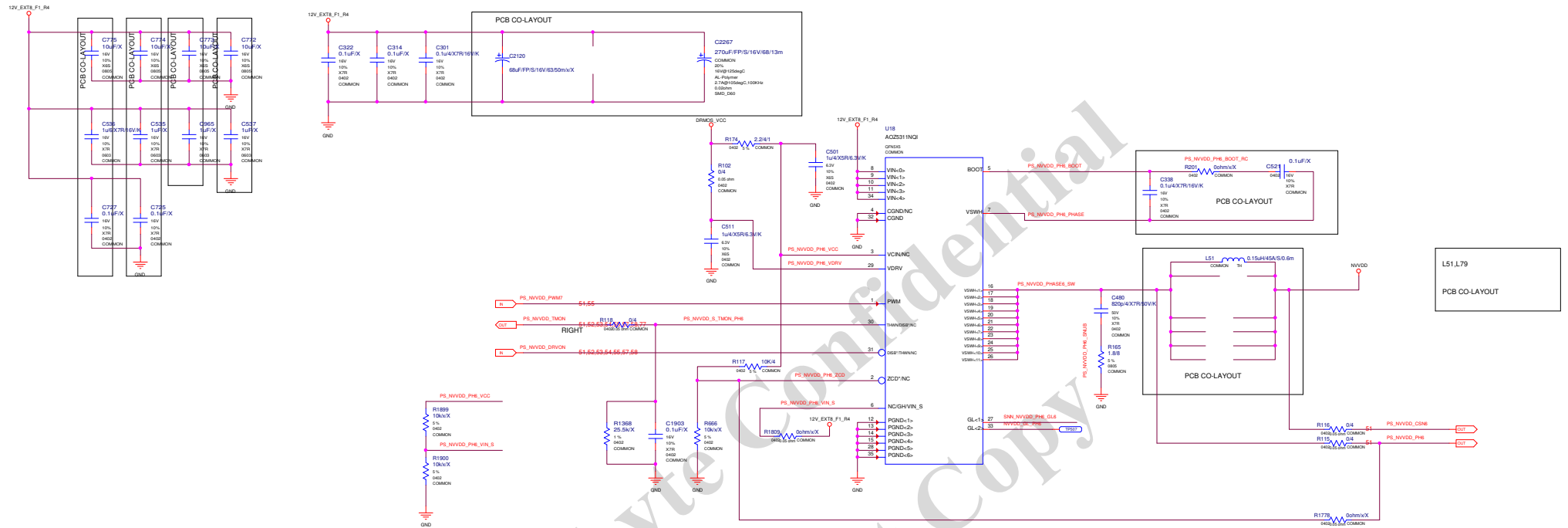
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PS: NVVDD PH5 (PWM7) and PH7 (PWM8)

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## PS: NVVDD Phase 6(PWM4)

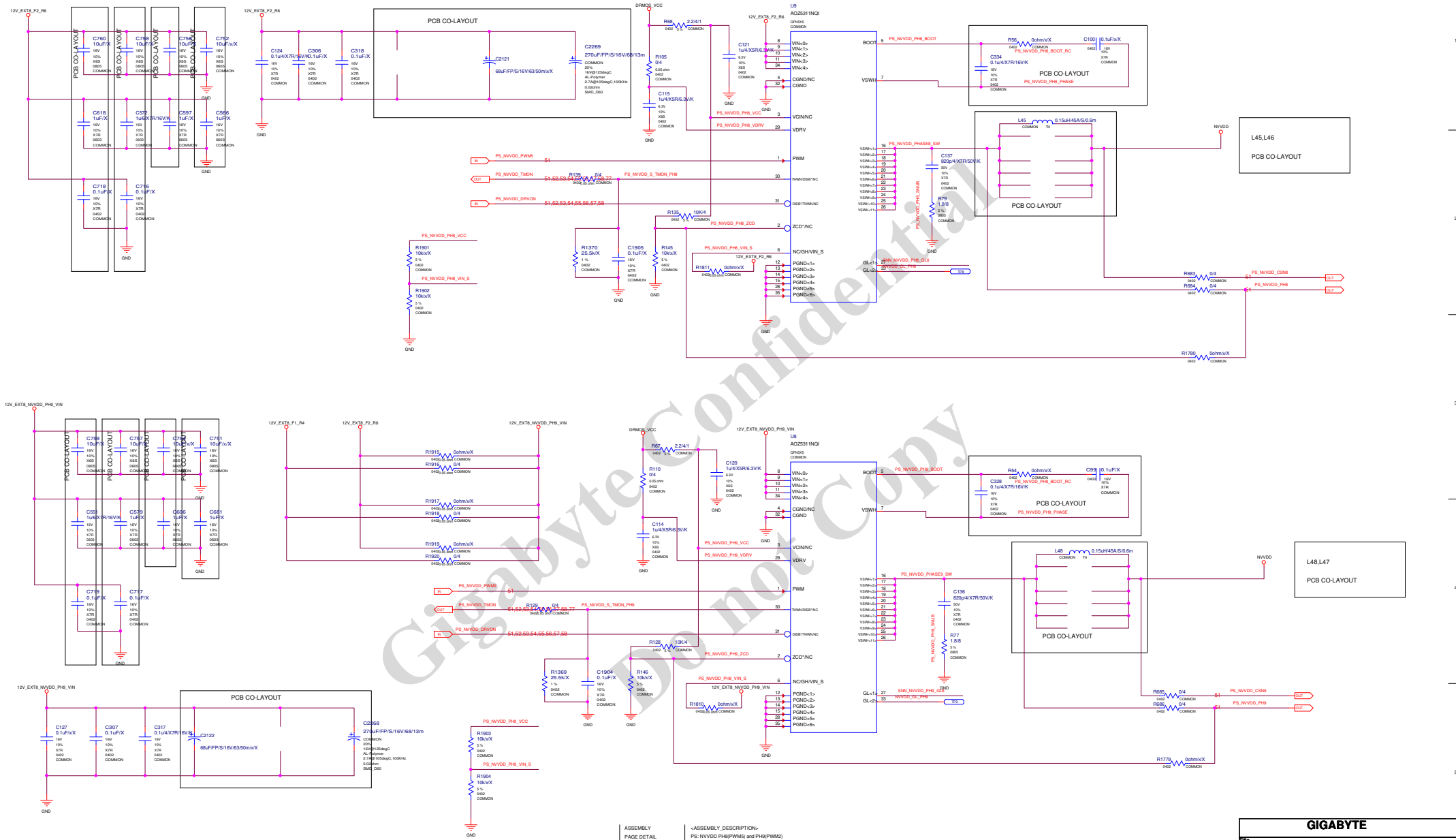


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PS: NVVDD PH 8 (PWM5), PH 9(PWM2)



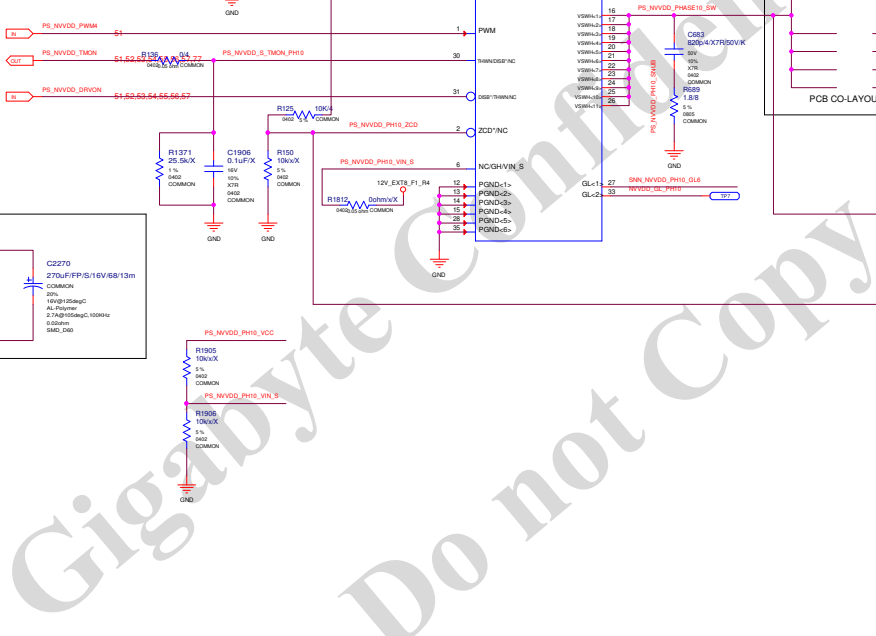
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PS: NVVDD PH8(PWM5) and PH9(PWM2)

PS: NVVDD PH8(PWM5) and PH9(PWM2)

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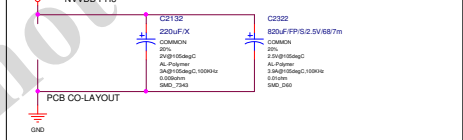
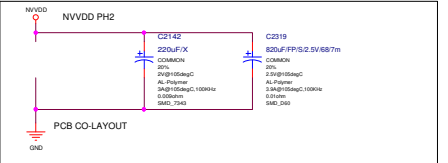
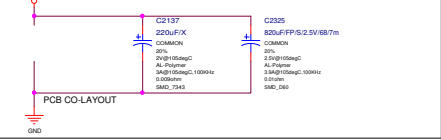
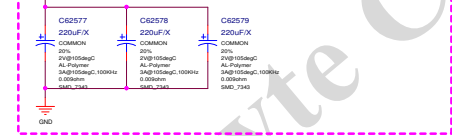
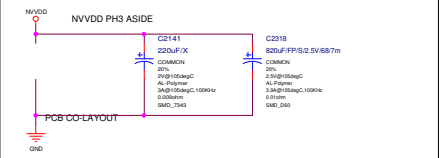
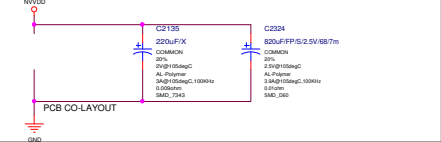
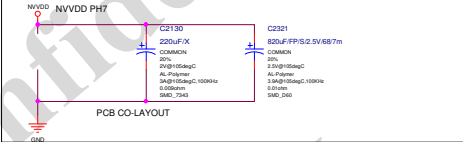
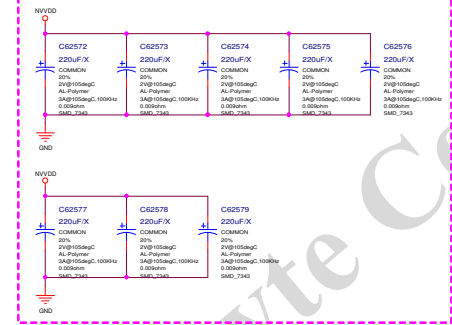
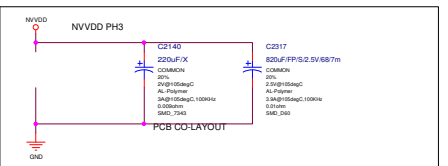
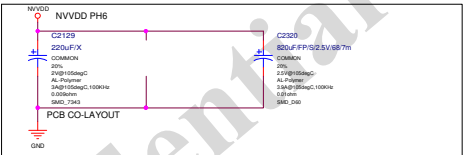
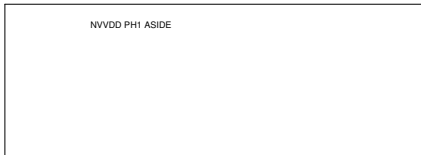
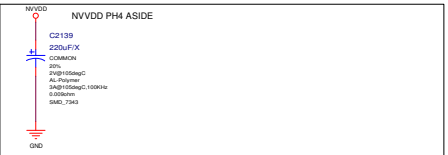
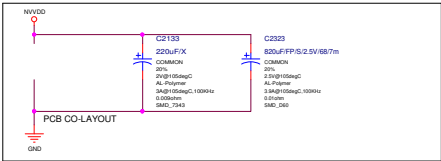
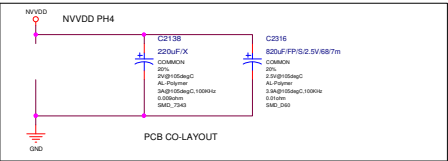
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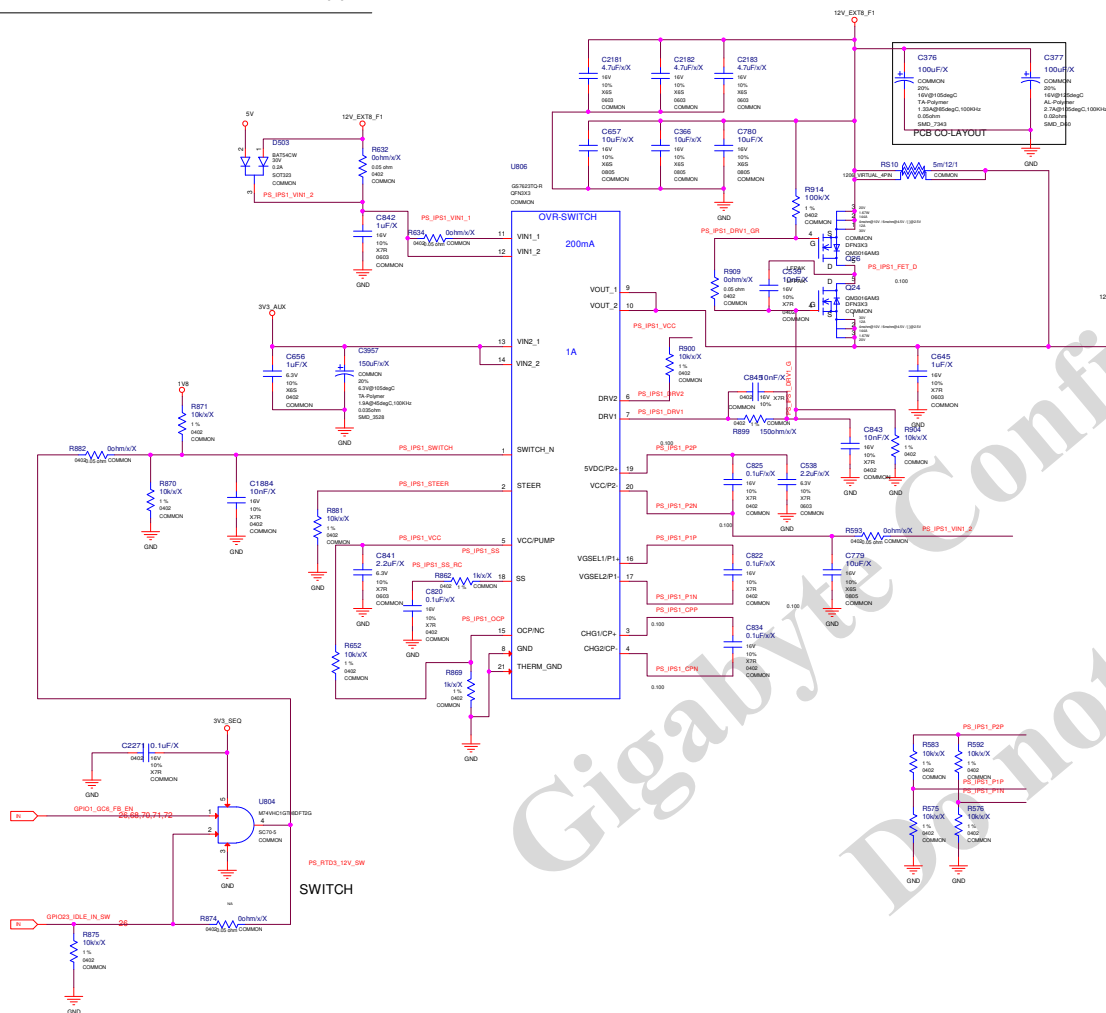
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## PS: INPUT SWITCH RTD3

### AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO23	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



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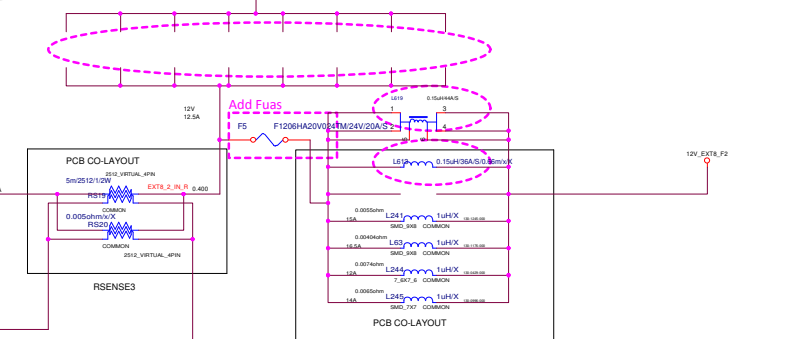
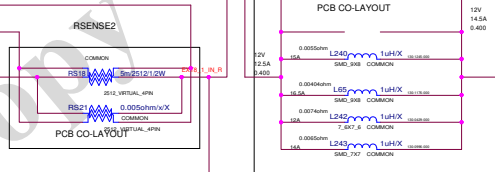
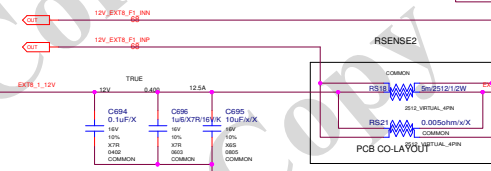
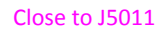
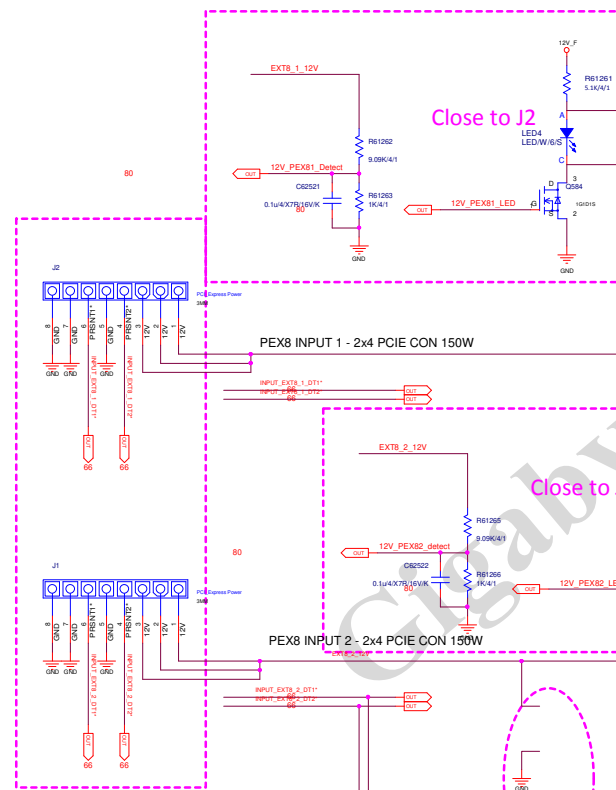
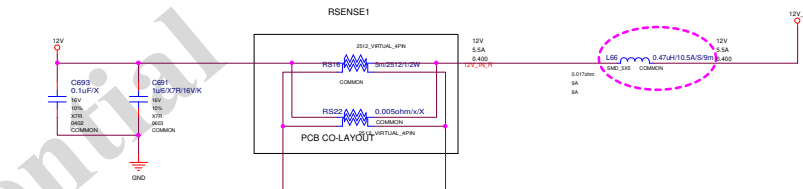
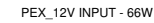
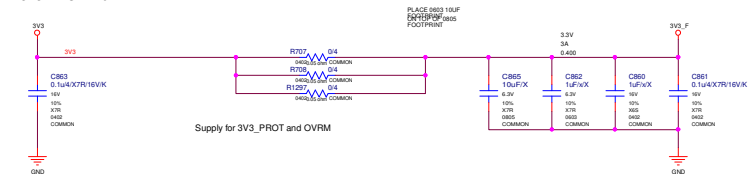
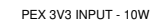
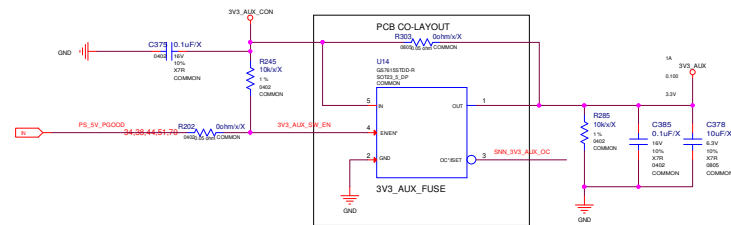
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## PS: Inputs, Filtering, and Monitoring



QD SKU CABLE

ASSEMBLY  
PAGE DETAIL

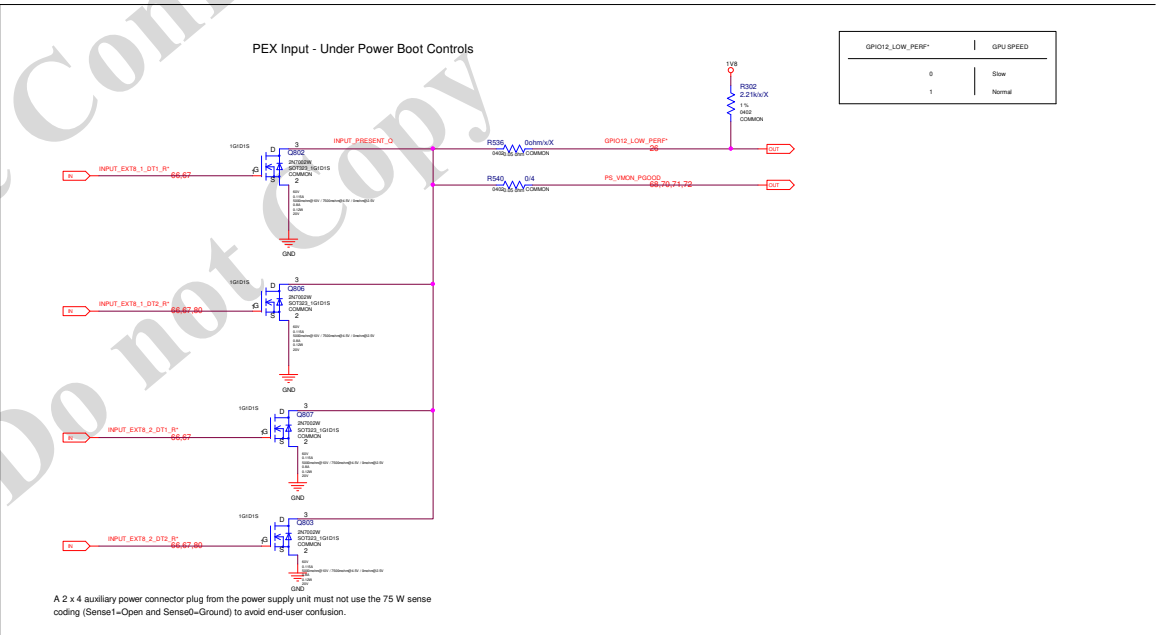
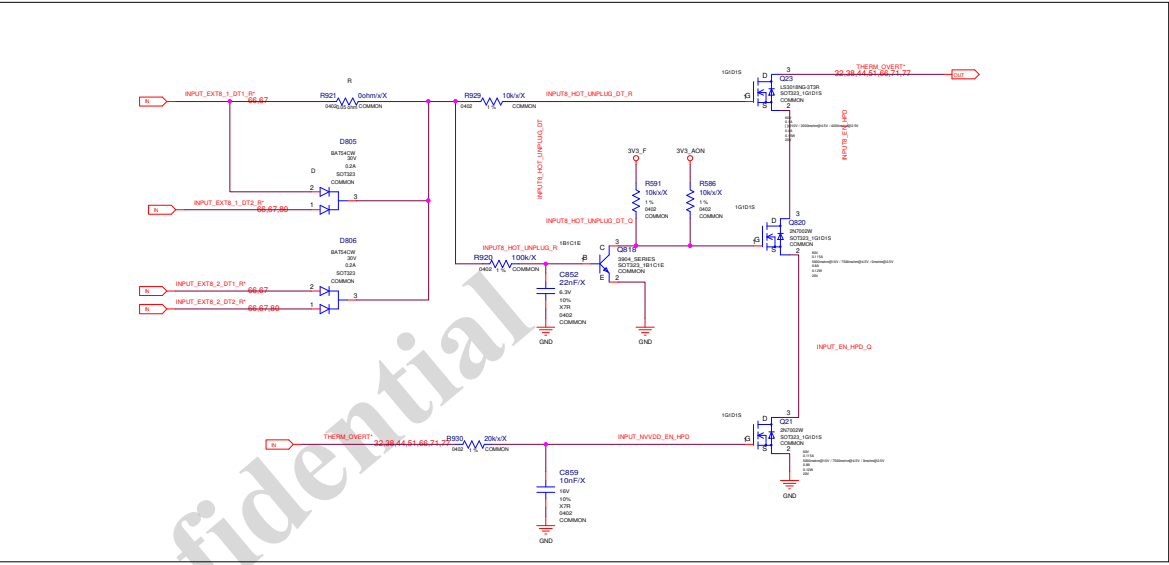
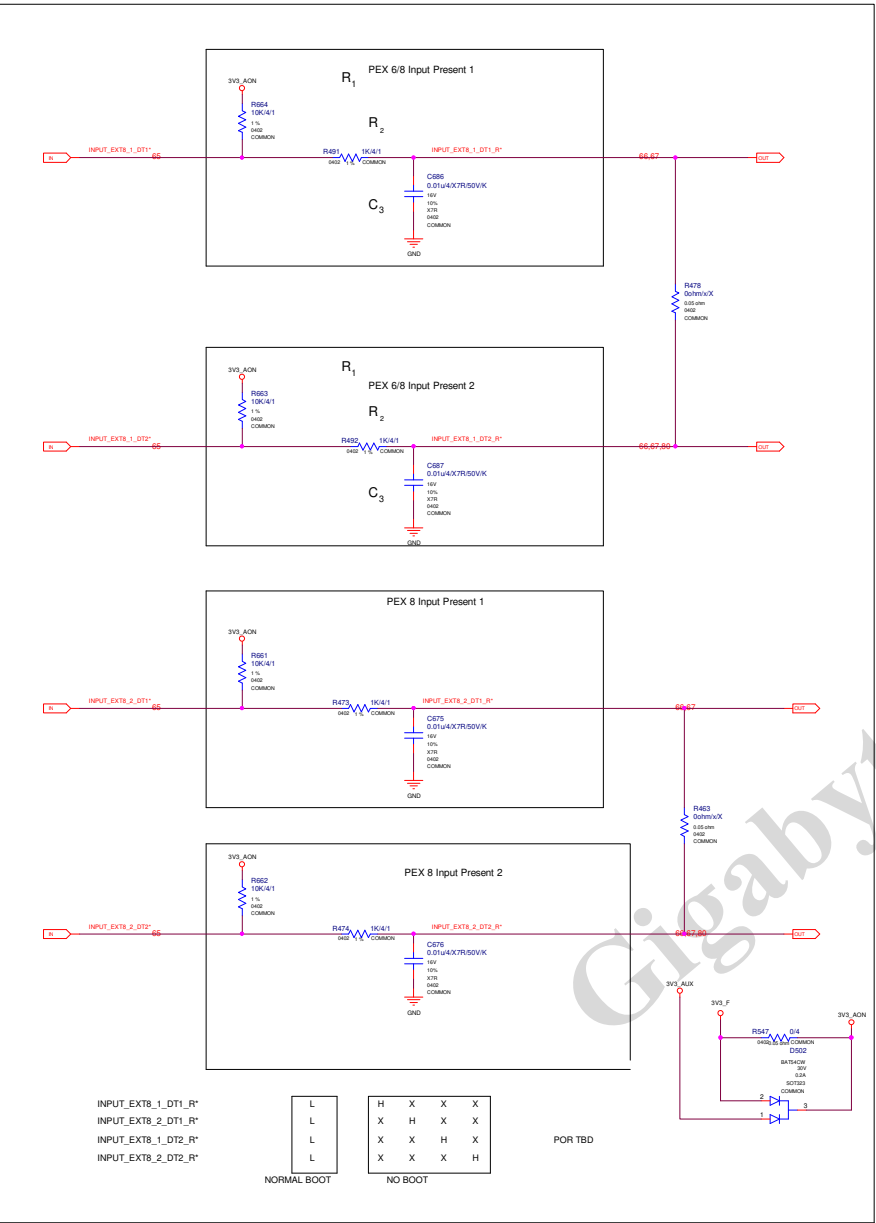
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PS: INPUTS, FILTERING, and MONITORING

## GIGABYTE

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PCIE			
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PS: 12V Current Steering & Hot Unplug Detect



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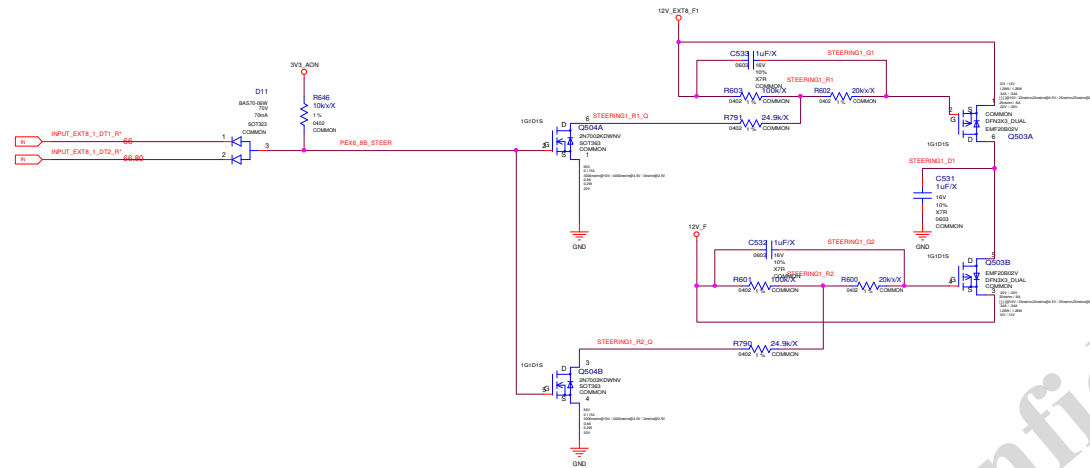
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PS: HOT UNPLUG

GIGABYTE				
File	PCIe			
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## PS: Discrete Steering

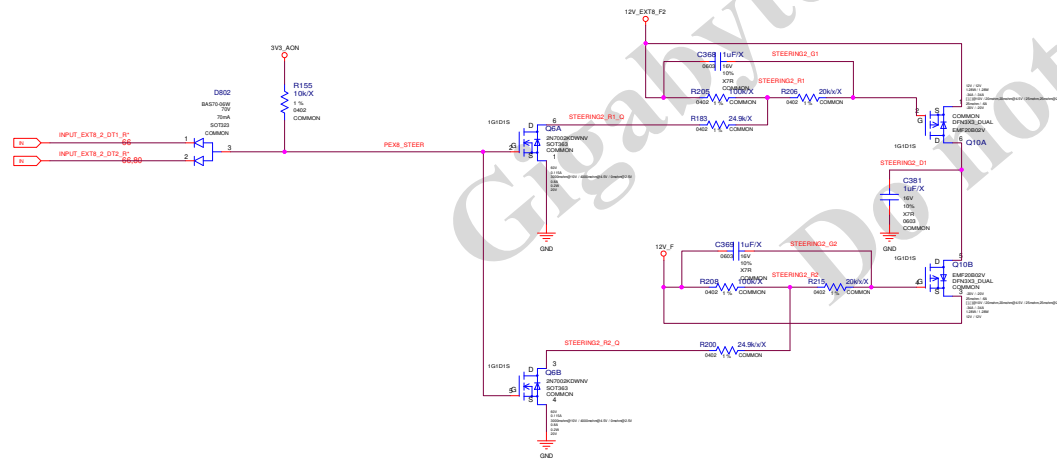
### 12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V\_EXT8\_F1



NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V\_EXT8\_F2



ASSEMBLY  
PAGE DETAIL

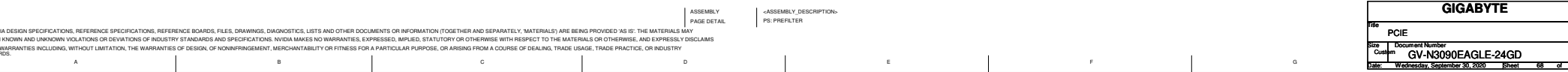
PS: Discrete Power Steering

## GIGABYTE

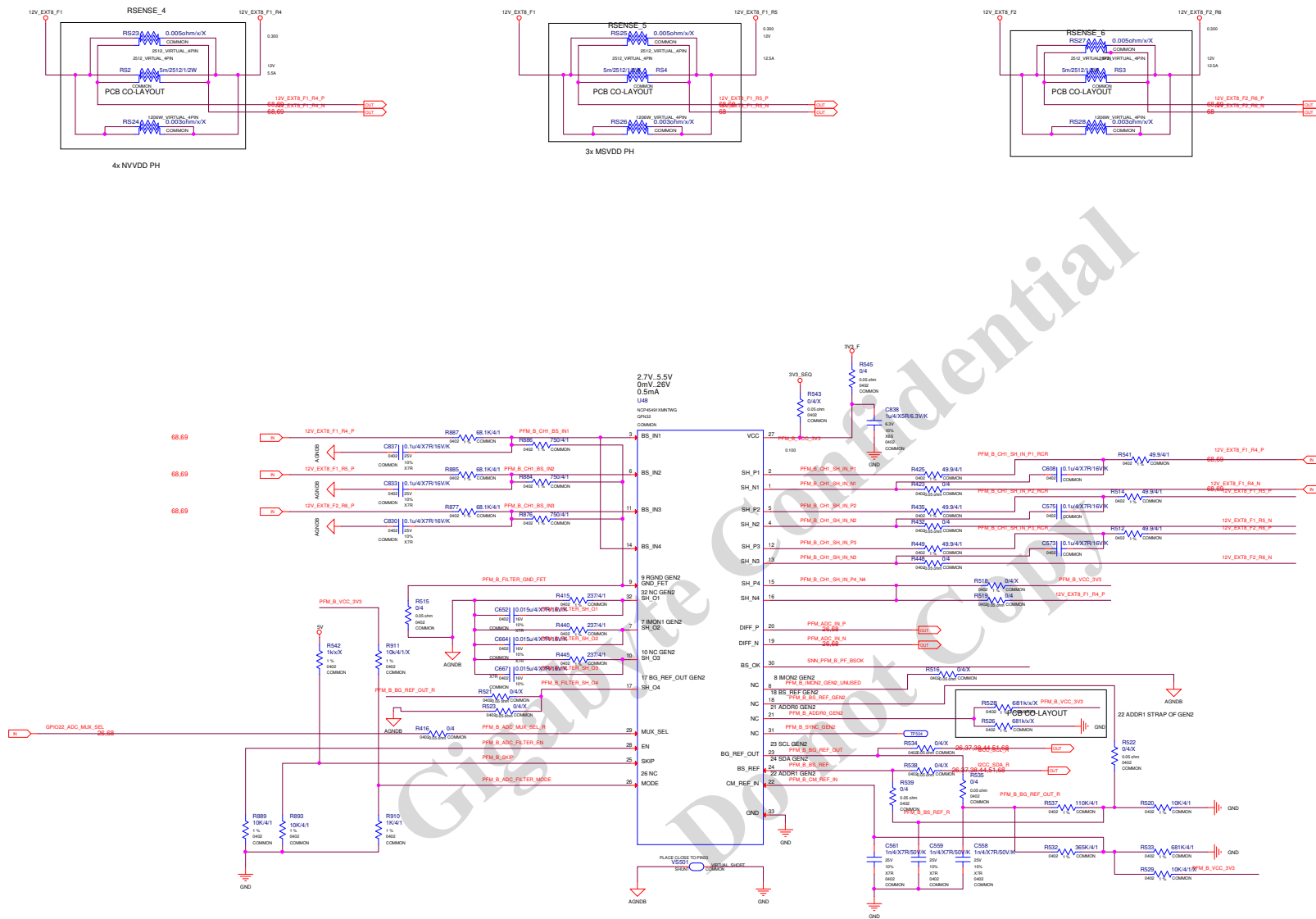
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PCIE			
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## Route the trace to PEX Golden Finger

[illegible]

PS: Pre-Filter B



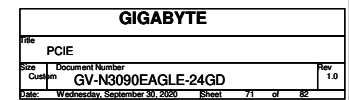
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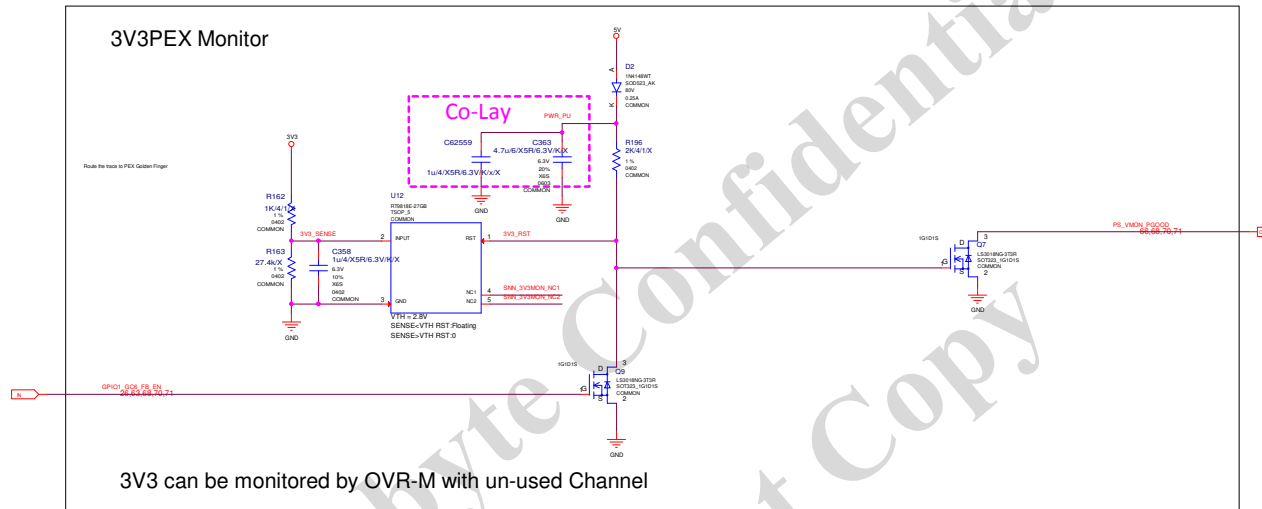
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PCIE			
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Sequence: 3V3 MONITOR



3V3 can be monitored by OVR-M with un-used Channel





2

3

4

5

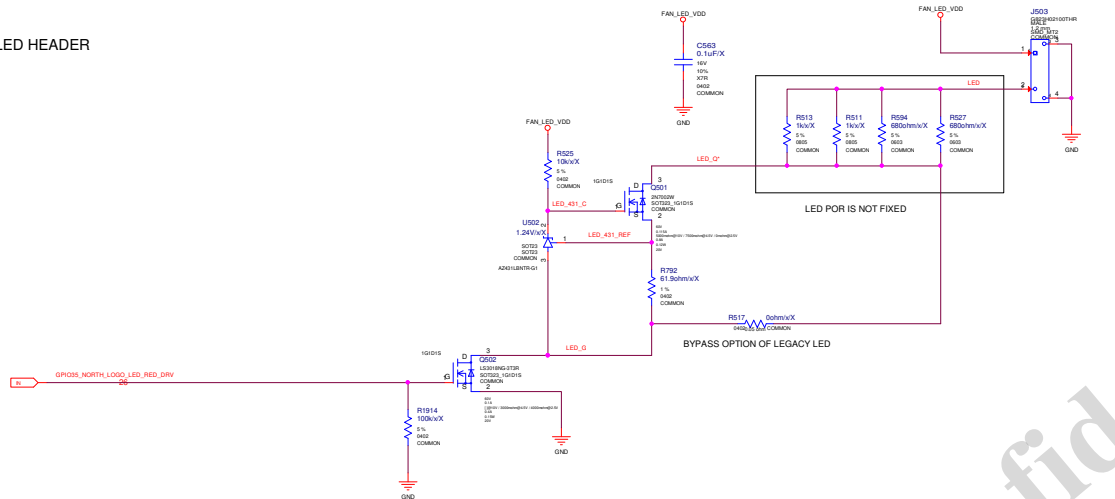
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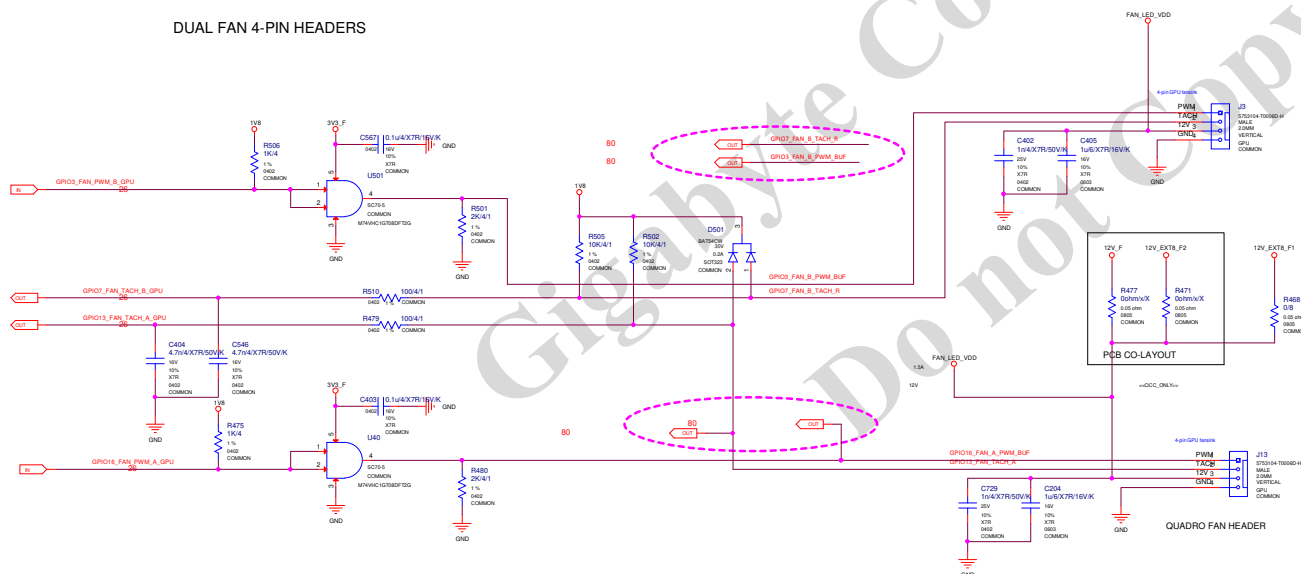
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# MISC: LED & FAN

## 2-PIN LED HEADER



## DUAL FAN 4-PIN HEADERS



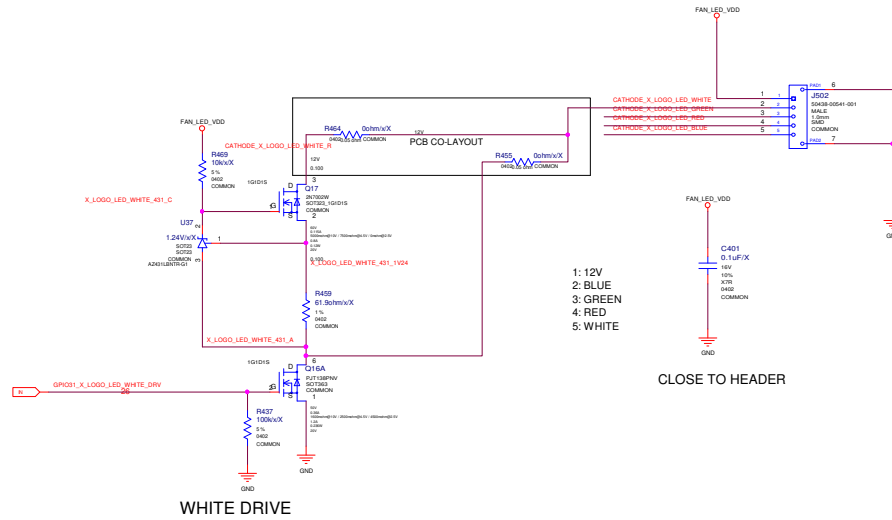
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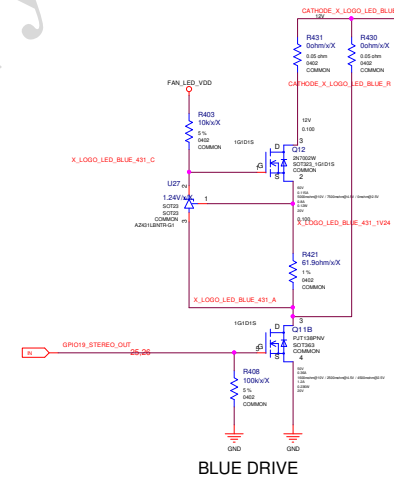
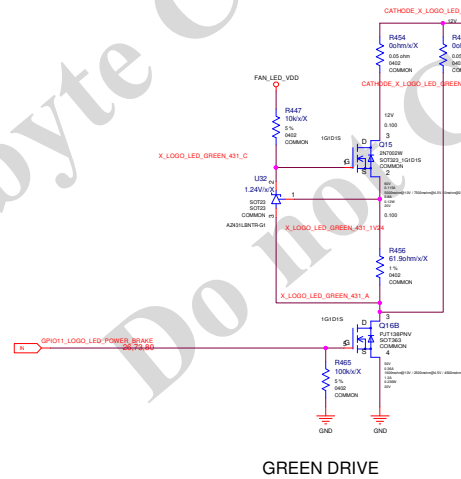
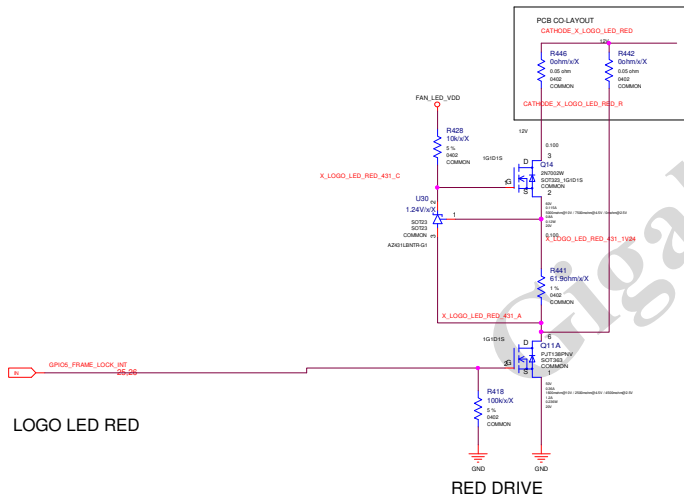
ASSEMBLY DESCRIPTION  
MISC: LED & FAN

## GIGABYTE

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CONNECTOR SIZE TO FIT LAYOUT  
ALL CIRCUIT NO STUFF BY DEFAULT  
ALINGN WITH PASH  
IF ADDITIONAL POWER CONSUPTION R  
NEEDED, IT SHOULD BE ON LED MOD.

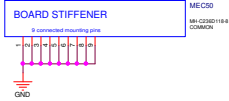


Mechanical: Mounting holes

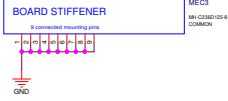
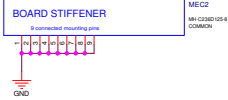
BK up



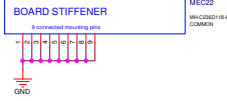
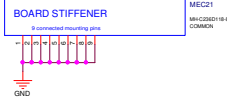
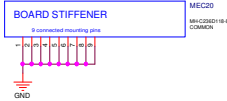
BK low



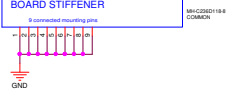
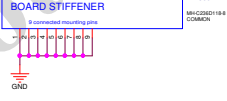
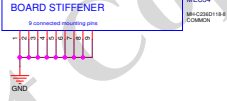
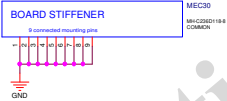
GPU



MOS



Backplane



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ASSEMBLY PAGE DETAIL  
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	VR Thermal Protection

<b>GIGABYTE</b>			
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PCI TERM

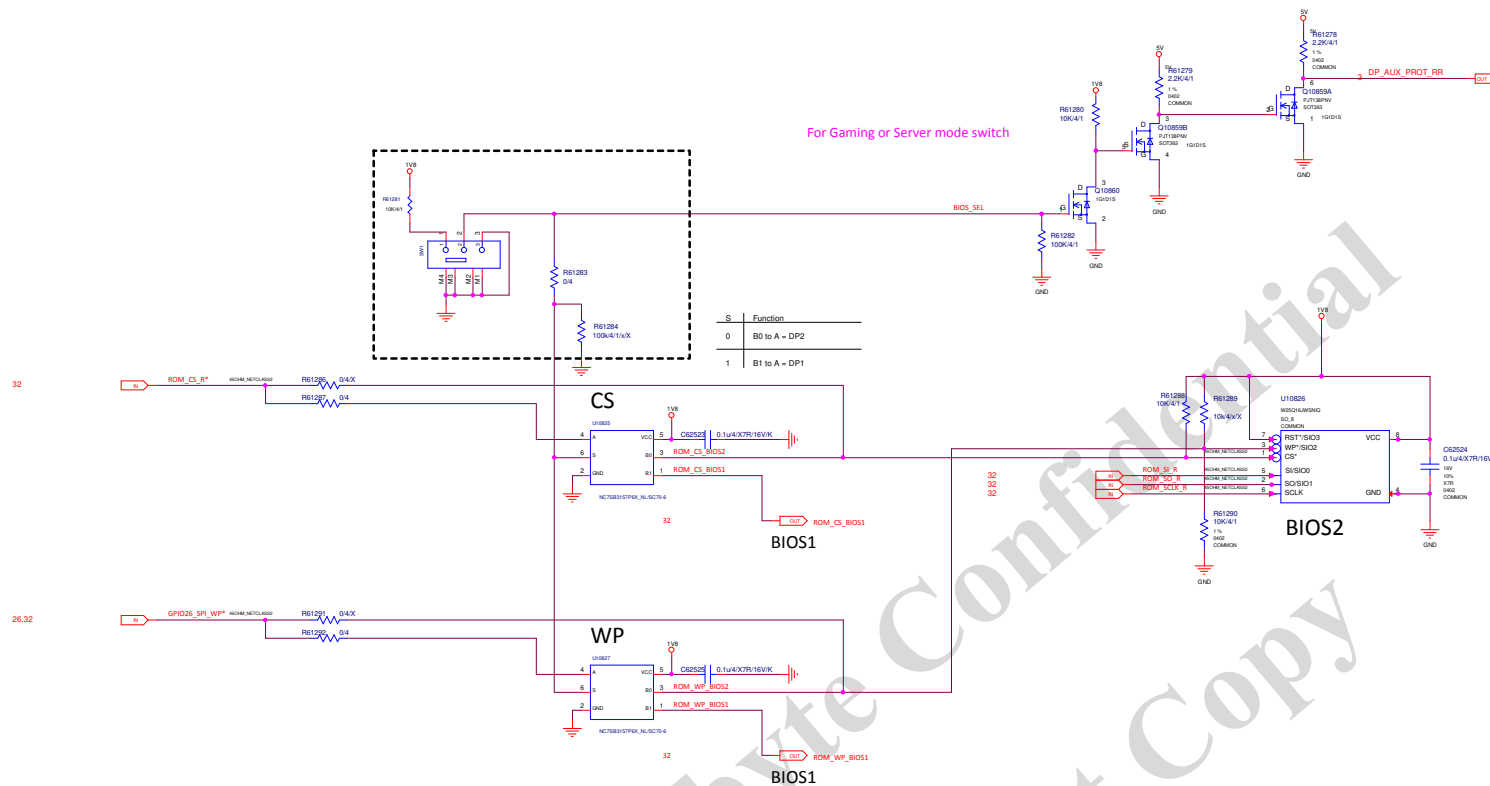


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ASSEMBLY PAGE DETAIL  
PCI TERM

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## BIOS Switch



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ASSEMBLY  
PAGE DETAIL

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MCU ZERO POWER IDLE







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History

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2018.07.21	First version

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