

G94-P545-A01 - GDDR3, DVI/VGA + DVI/VGA + HDTV/SDTV-Out

REV	VARIANT	NVPIN	ASSEMBLY
B	BASE	600-10545-0000-100	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	600-10545-0100-100	G94-400 650MHz/1000MHz 512MB 16MA32 BGA136 GDDR3, DVI+DL+DVI+DL+HDTV-Out (Bring Up SKU)
2	SKU000	600-10545-0000-100	G94-400 650MHz/1000MHz 512MB 16MA32 BGA136 GDDR3, DVI+DL+DVI+DL+HDTV-Out
3	SKU0010	600-10545-0010-100	G94-300 650MHz/800MHz 512MB 16MA32 BGA136 GDDR3, DVI+DL+DVI+DL+HDTV-Out
4	SKU020	600-10545-0020-100	G94-300 650MHz/800MHz 384MB 16MA32 BGA136 GDDR3, DVI+DL+DVI+DL+HDTV-Out
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V127-0A Base on P545

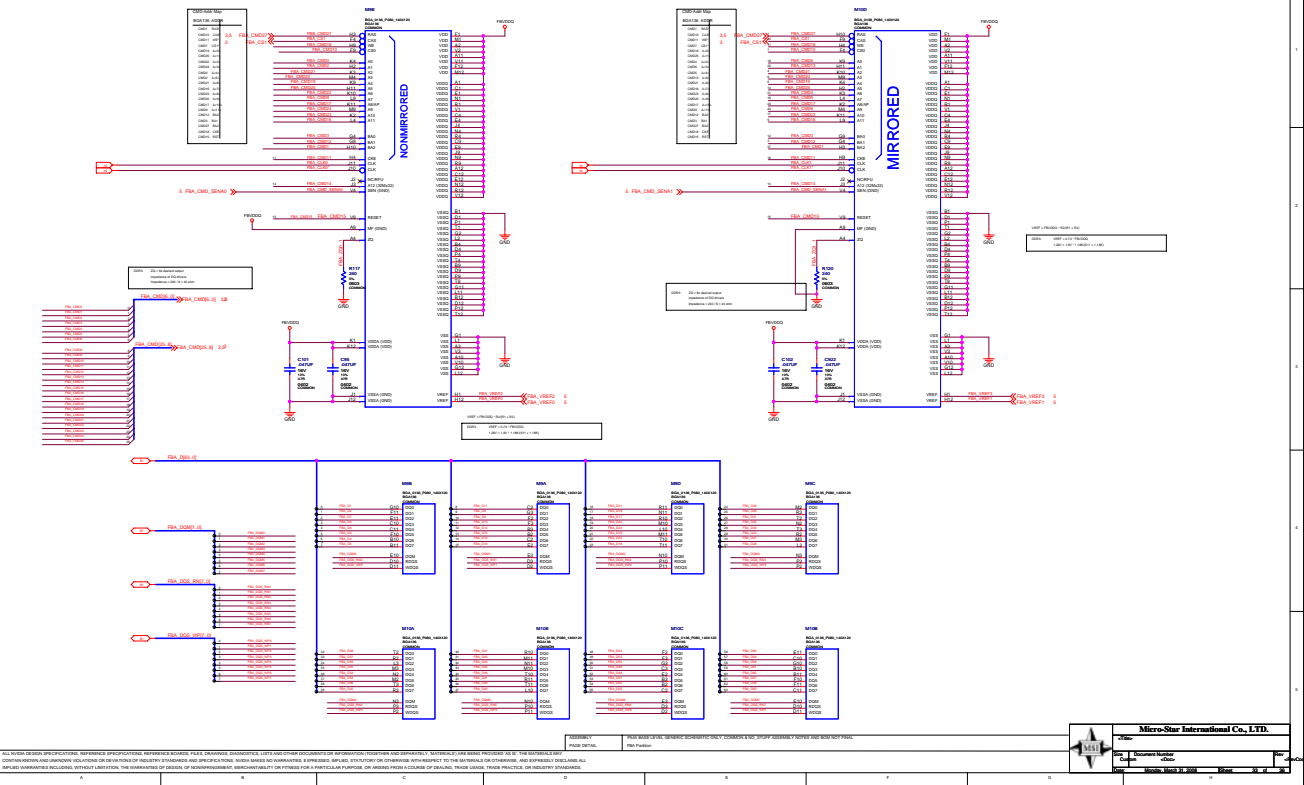
- 1.PAGE18: ADD Display port circuit
- 2.PAGE21: ADD GPIO circuit
- 3.PAGE 21: change SPDIF circuit
- 4.PAGE 27: remove PEX_VDD power switch circuit
- 5.PAGE 27: remove IFP_PLLVDD/2V5 power switch circuit cahnge APL5713 and APL5910 circuit
- 6.PAGE 28: remove FBVDDQ power switch circuit change APW7067N power circuit
- 7.PAGE 29: remove NVVDD VID circuit
- 8.PAGE 30: change NNVDD POWER APW7088 circuit
- 9.PAGE 16/17 : ADD EMI bridge R
- 10.PAGE 17 CO-LAYOUT HDIM CONNECT
- 11.PAGE 15 remove J1 D_SUB SLIM CONNECT

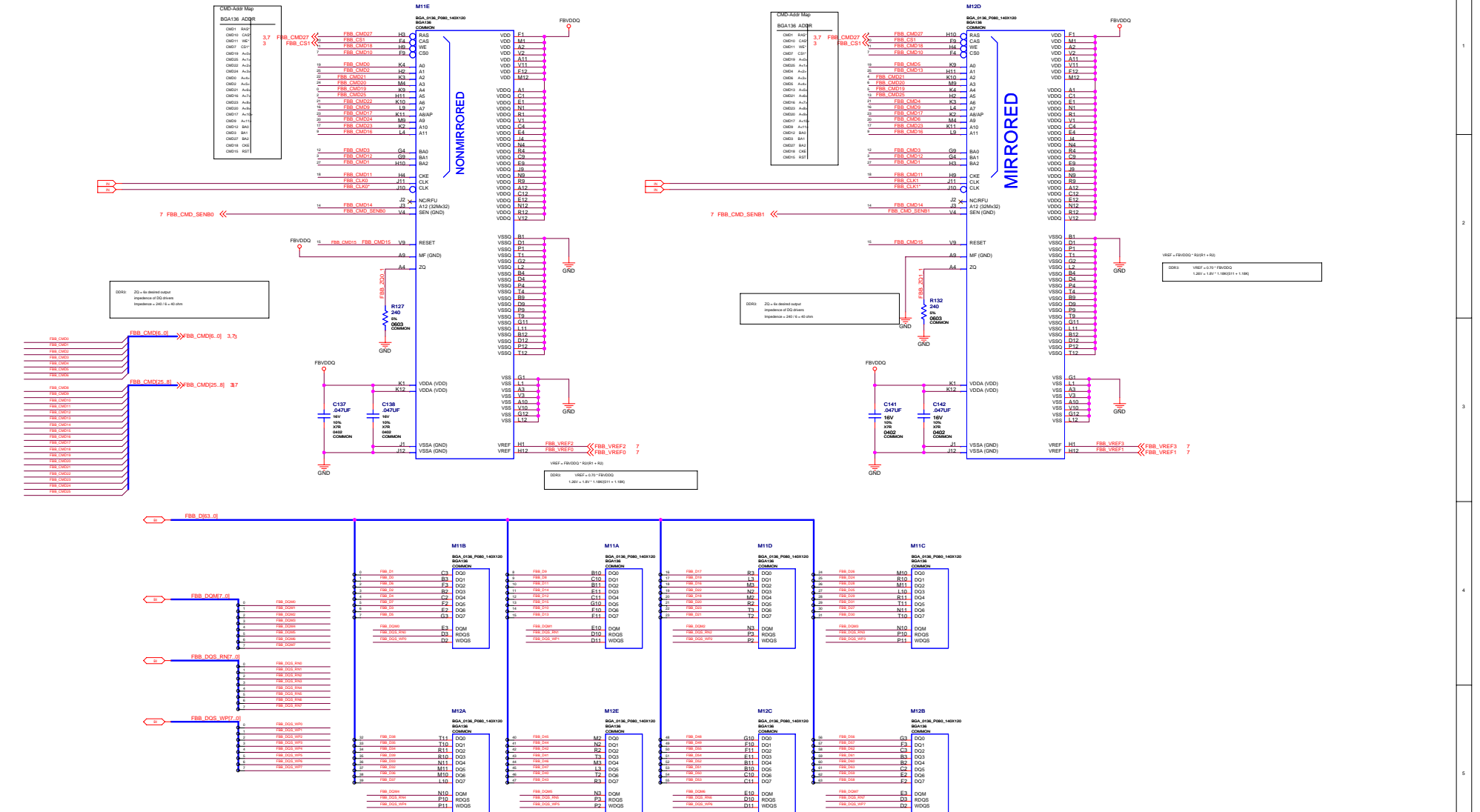
V135-0A Base on V127-0A and P545

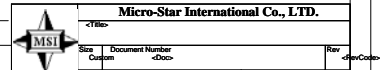
- 1.Add Page 33,34,35,36 for extend MEM
- 2.Page 3,4 FBCMD7 connect to CS1

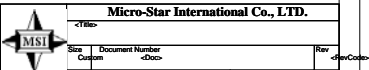
V135-100 Base on V135-0A and V127-100

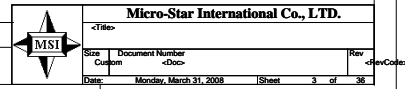
- 1.PAGE30: modify NVVDD power sequence contral circuit
- 2.PAGE28: Change L6 footprint
- 3.PAGE18: Modify DP_Power circuit and AUX channel circuit

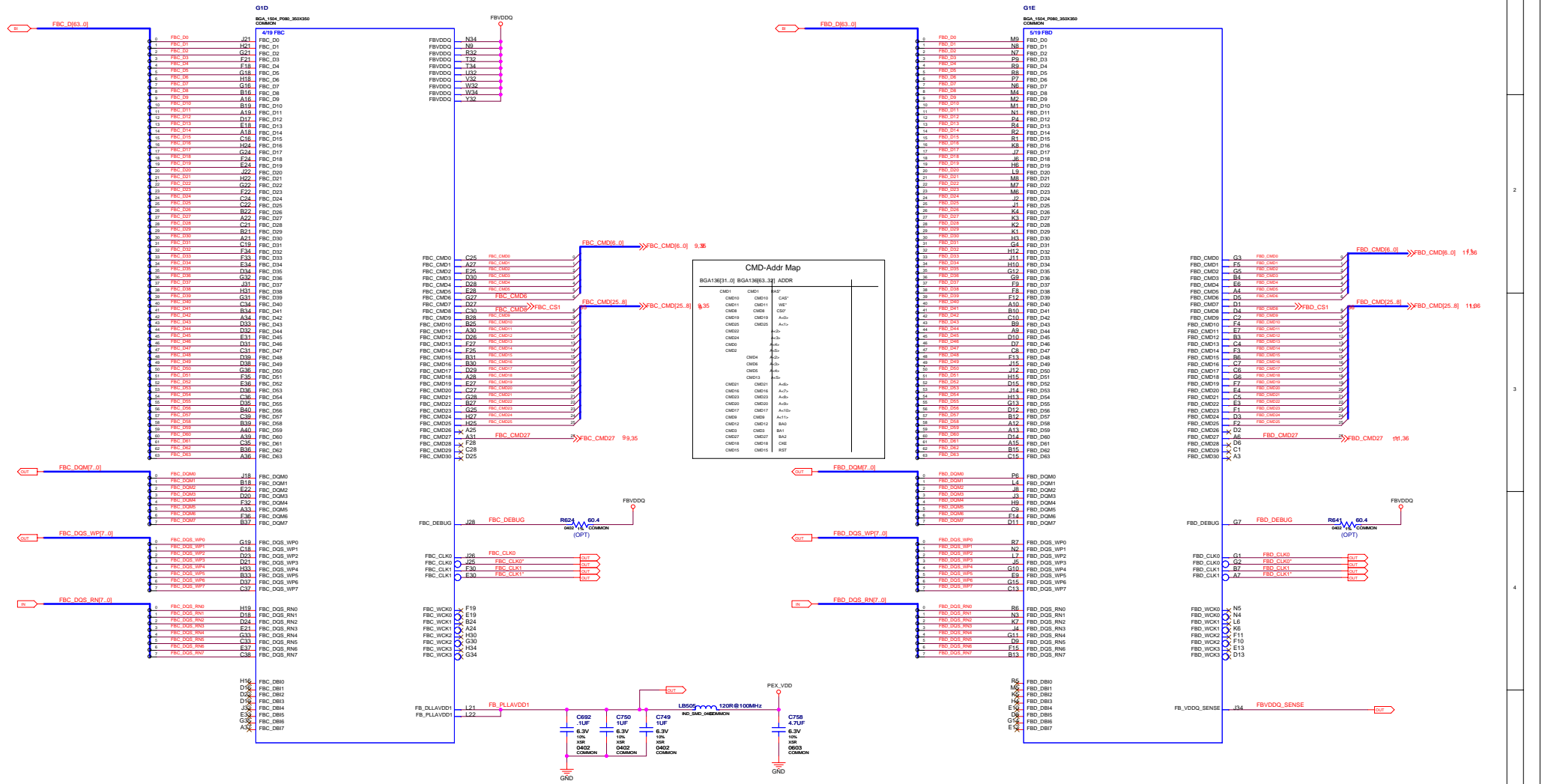




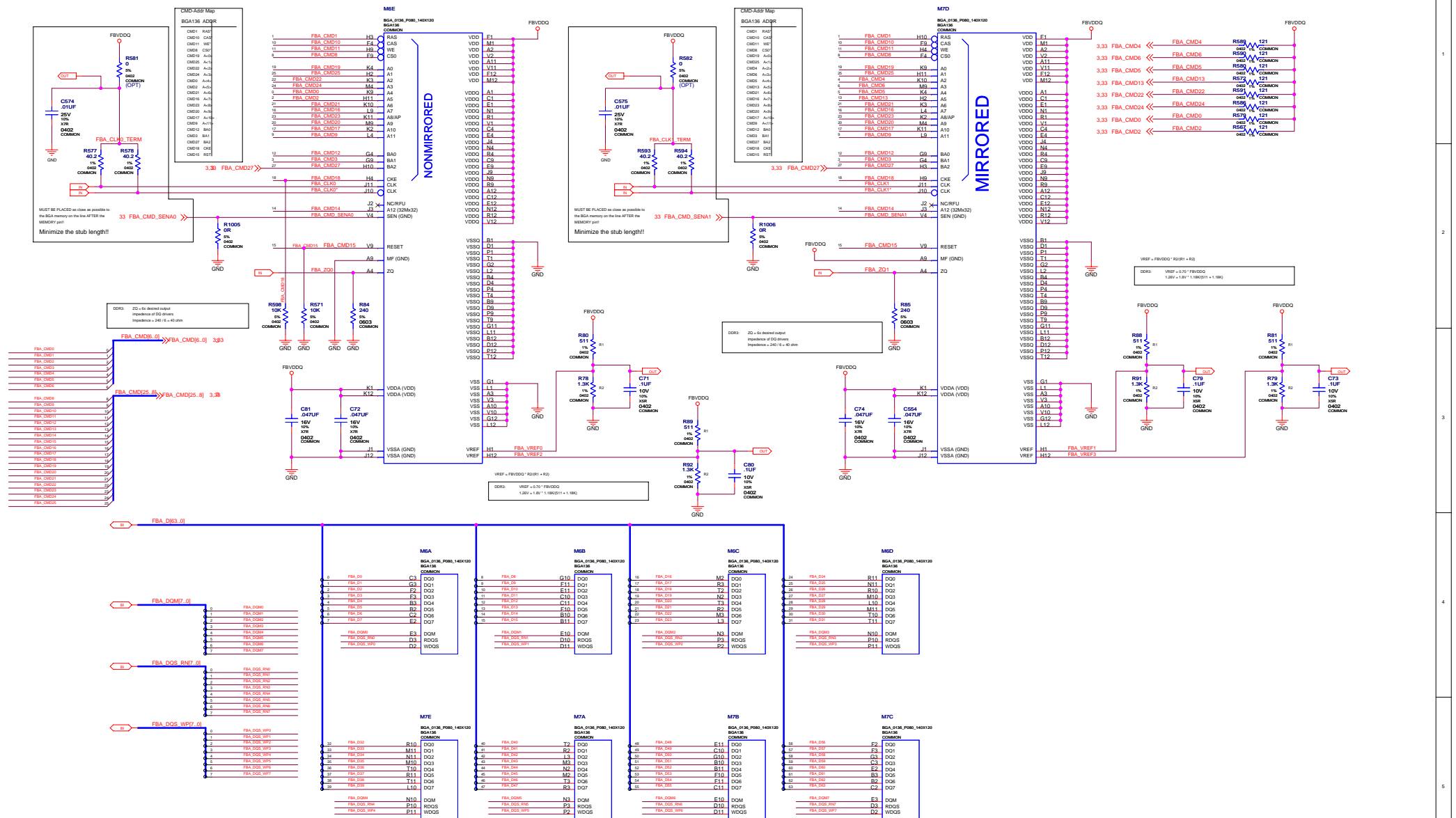


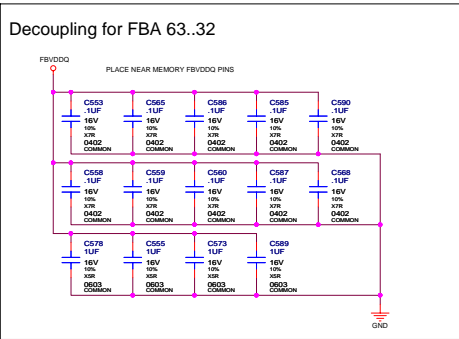
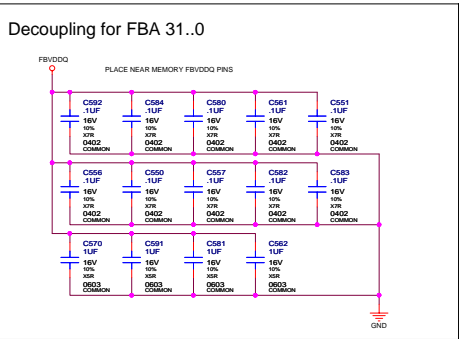







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ASSEMBLY PAGE DETAIL FBA Partition Decoupling

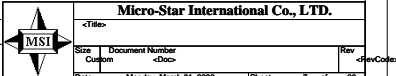


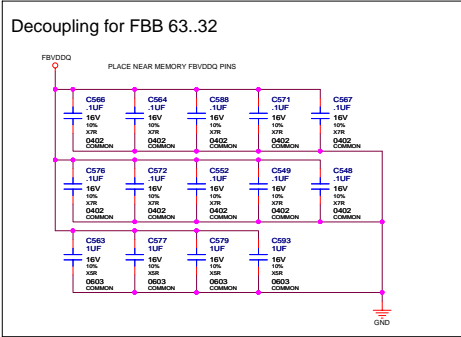
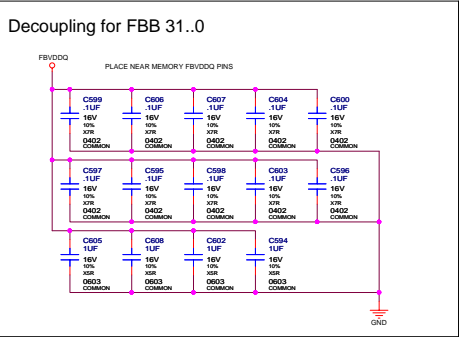
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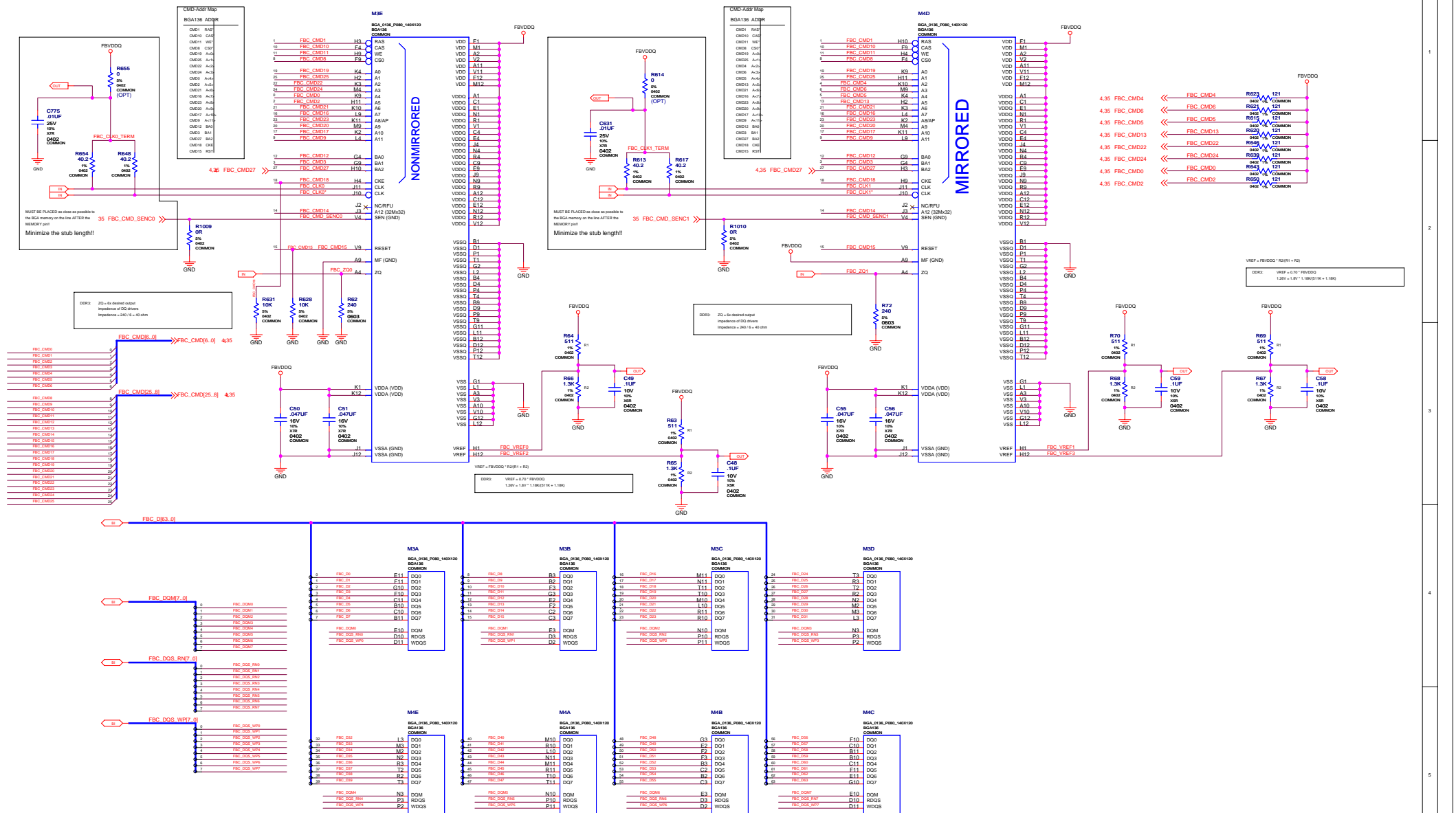
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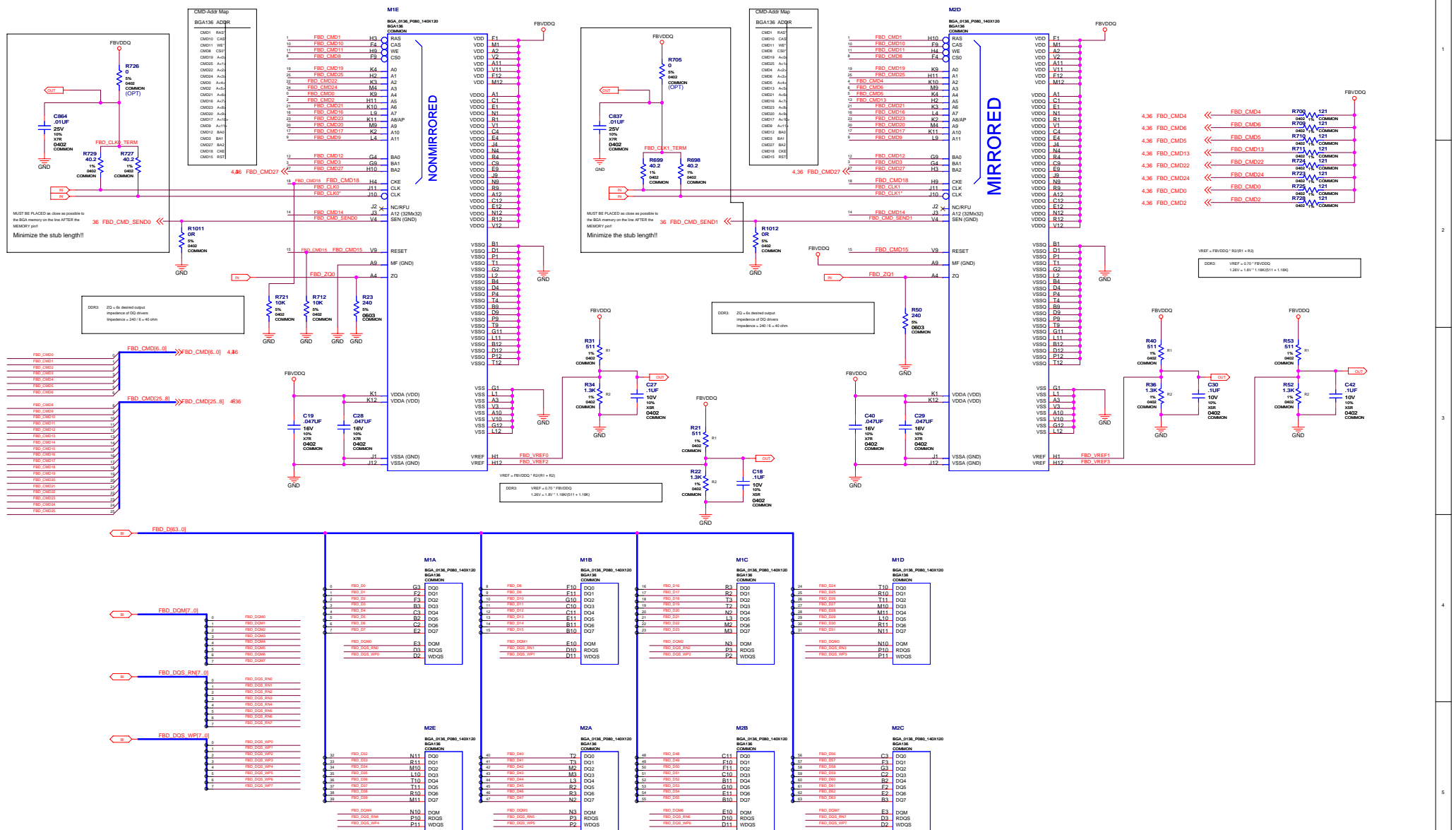
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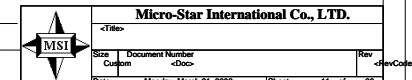
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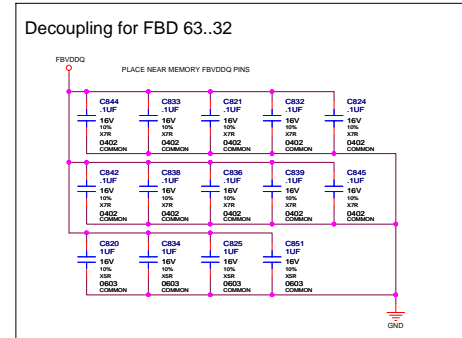


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NET RULES for FBA and FBB

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
OUT FBA_CLK0	1	800FT	FBA_CLK0
OUT FBA_CLK0P	1	800FT	FBA_CLK0
OUT FBA_CLK0_TERM	1	800M	
OUT FBA_CLK1	1	800FT	FBA_CLK1
OUT FBA_CLK1P	1	800FT	FBA_CLK1
OUT FBA_CLK1_TERM	1	800M	

NET	NV_CRITICAL_NET	IMPEDANCE
OUT FBA_DQS_WRP7_0	1	800M
IN FBA_DQS_WRP7_0	1	800M
OUT FBA_DQS_WRP7_0	1	800M
IN FBA_DQS_WRP7_0	1	800M

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
OUT FBB_CLK0	1	800FT	FBB_CLK0
OUT FBB_CLK0P	1	800FT	FBB_CLK0
OUT FBB_CLK0_TERM	1	800M	
OUT FBB_CLK1	1	800FT	FBB_CLK1
OUT FBB_CLK1P	1	800FT	FBB_CLK1
OUT FBB_CLK1_TERM	1	800M	

NET	NV_CRITICAL_NET	IMPEDANCE
OUT FBB_DQS_WRP7_0	1	800M
IN FBB_DQS_WRP7_0	1	800M
OUT FBB_DQS_WRP7_0	1	800M
IN FBB_DQS_WRP7_0	1	800M

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
IN FB_PLAVDD0	12MIL	1.1V	0.04A
IN FB_VREF	12MIL	1.20V	0.02A
IN FBA_VREF0	12MIL	1.20V	0.02A
IN FBA_VREF1	12MIL	1.20V	0.02A
IN FBA_VREF2	12MIL	1.20V	0.02A
IN FBA_VREF3	12MIL	1.20V	0.02A
IN FBA_200	12MIL	1.20V	0.02A
IN FBA_201	12MIL	1.20V	0.02A
IN FBB_VREF0	12MIL	1.20V	0.02A
IN FBB_VREF1	12MIL	1.20V	0.02A
IN FBB_VREF2	12MIL	1.20V	0.02A
IN FBB_VREF3	12MIL	1.20V	0.02A
IN FBB_200	12MIL	1.20V	0.02A
IN FBB_201	12MIL	1.20V	0.02A

NET RULES for FBC and FBD

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
OUT FBC_CLK0	1	800FT	FBC_CLK0
OUT FBC_CLK0P	1	800FT	FBC_CLK0
OUT FBC_CLK0_TERM	1	800M	
OUT FBC_CLK1	1	800FT	FBC_CLK1
OUT FBC_CLK1P	1	800FT	FBC_CLK1
OUT FBC_CLK1_TERM	1	800M	

NET	NV_CRITICAL_NET	IMPEDANCE
OUT FBC_DQS_WRP7_0	1	800M
IN FBC_DQS_WRP7_0	1	800M
OUT FBC_DQS_WRP7_0	1	800M
IN FBC_DQS_WRP7_0	1	800M

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
OUT FBC_CLK0	1	800FT	FBC_CLK0
OUT FBC_CLK0P	1	800FT	FBC_CLK0
OUT FBC_CLK0_TERM	1	800M	
OUT FBC_CLK1	1	800FT	FBC_CLK1
OUT FBC_CLK1P	1	800FT	FBC_CLK1
OUT FBC_CLK1_TERM	1	800M	

NET	NV_CRITICAL_NET	IMPEDANCE
OUT FBC_DQS_WRP7_0	1	800M
IN FBC_DQS_WRP7_0	1	800M
OUT FBC_DQS_WRP7_0	1	800M
IN FBC_DQS_WRP7_0	1	800M

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
IN FB_PLAVDD0	12MIL	1.1V	0.04A
IN FBC_VREF0	12MIL	1.20V	0.02A
IN FBC_VREF1	12MIL	1.20V	0.02A
IN FBC_VREF2	12MIL	1.20V	0.02A
IN FBC_VREF3	12MIL	1.20V	0.02A
IN FBC_200	12MIL	1.20V	0.02A
IN FBC_201	12MIL	1.20V	0.02A
IN FBD_VREF0	12MIL	1.20V	0.02A
IN FBD_VREF1	12MIL	1.20V	0.02A
IN FBD_VREF2	12MIL	1.20V	0.02A
IN FBD_VREF3	12MIL	1.20V	0.02A
IN FBD_200	12MIL	1.20V	0.02A
IN FBD_201	12MIL	1.20V	0.02A

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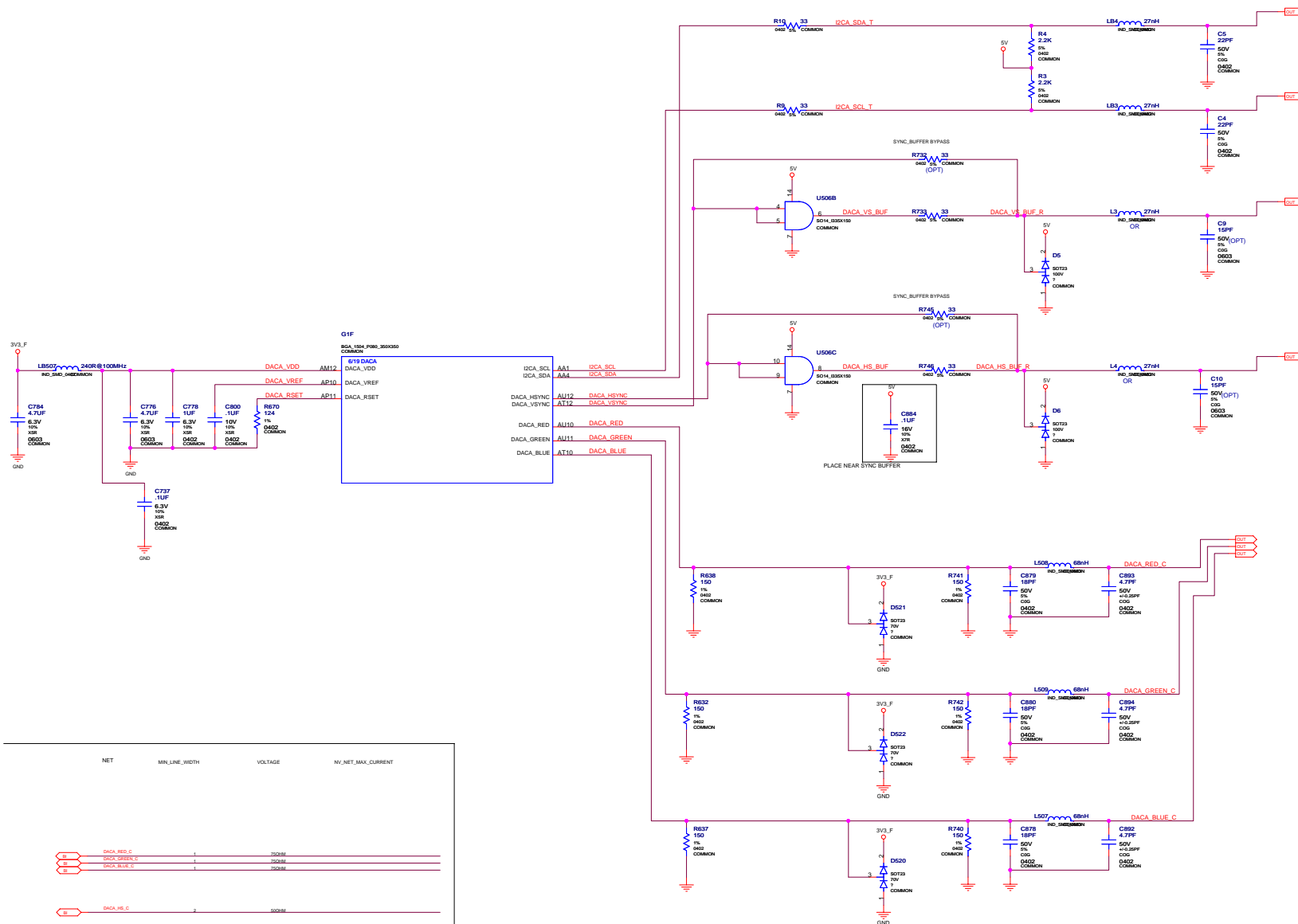
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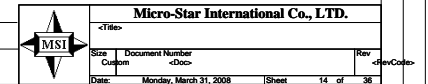
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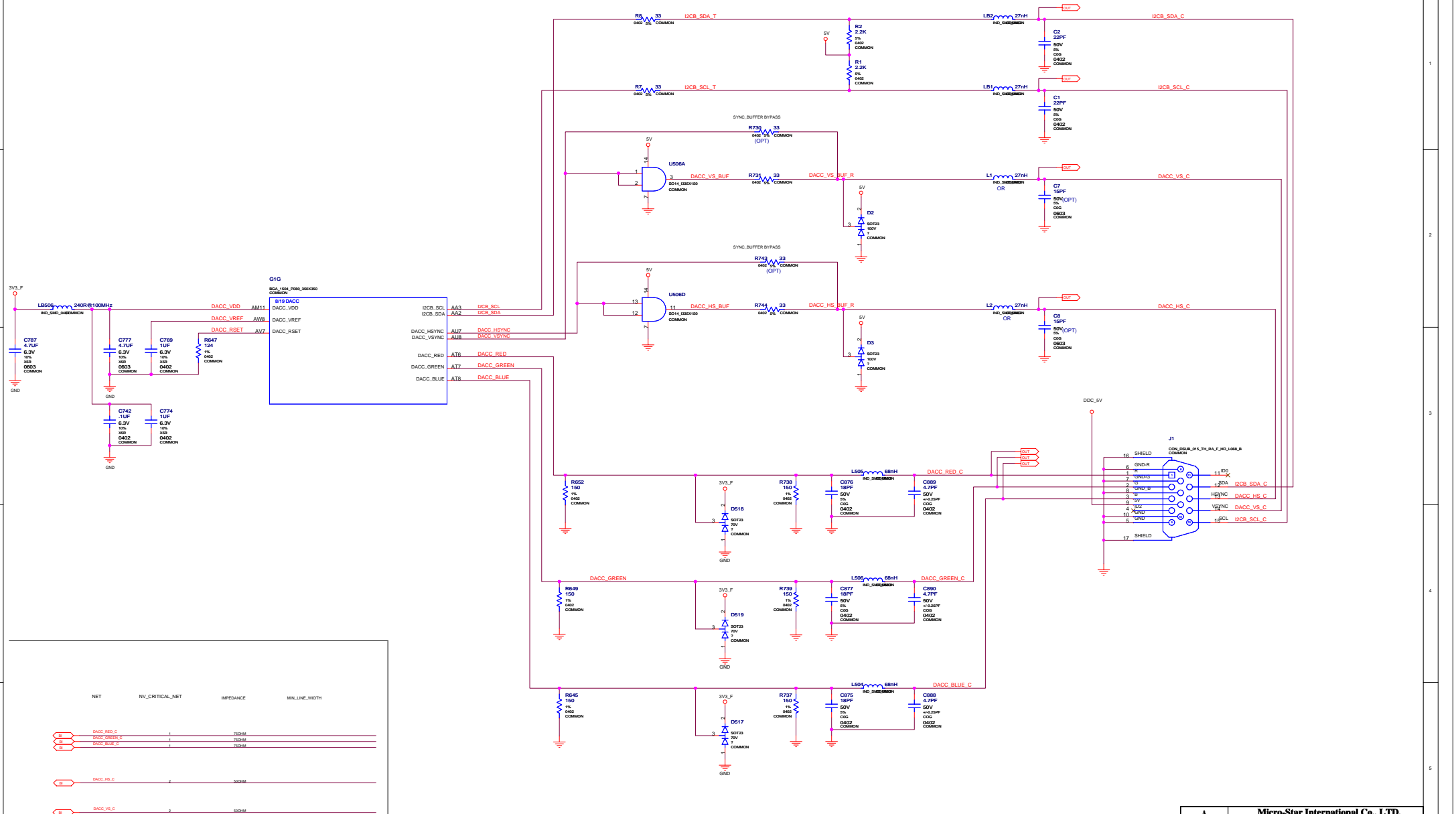
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DATA_GREEN_C	1	7500M	
DATA_BLUE_C	1	7500M	
DATA_HS_C	2	5000M	
DATA_VS_C	2	5000M	

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PAGE DETAIL	DACA interface

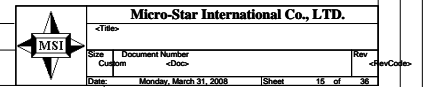


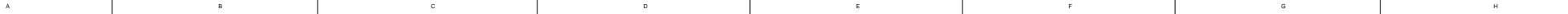
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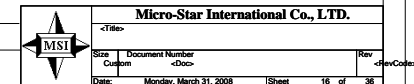
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PAGE DETAIL	DACC Interface

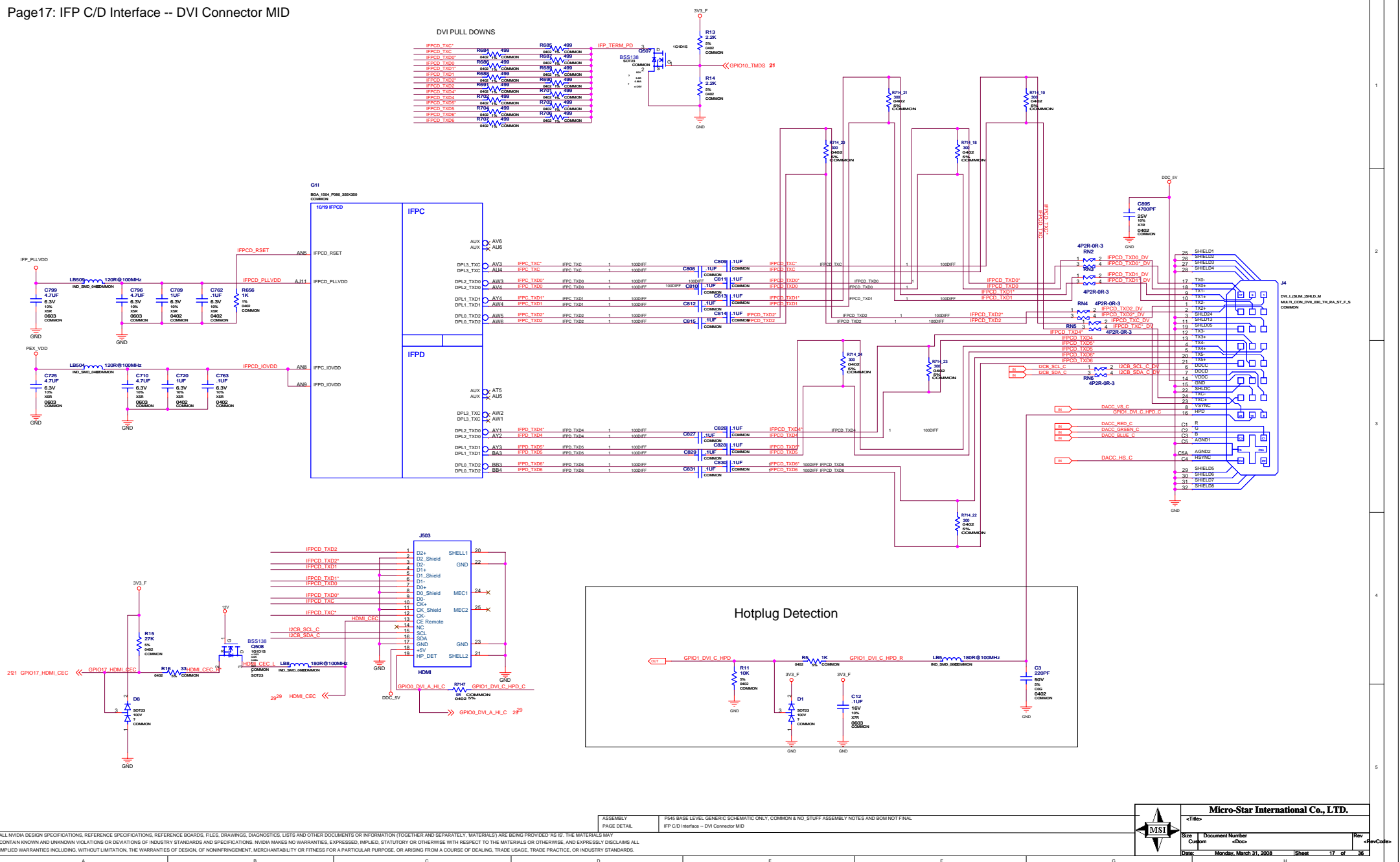


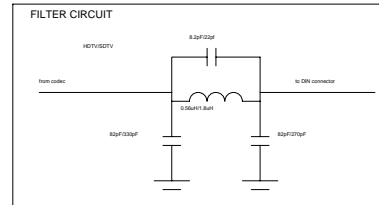
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PAGE DETAIL	IFP A/B Interface -- DVI Connector South

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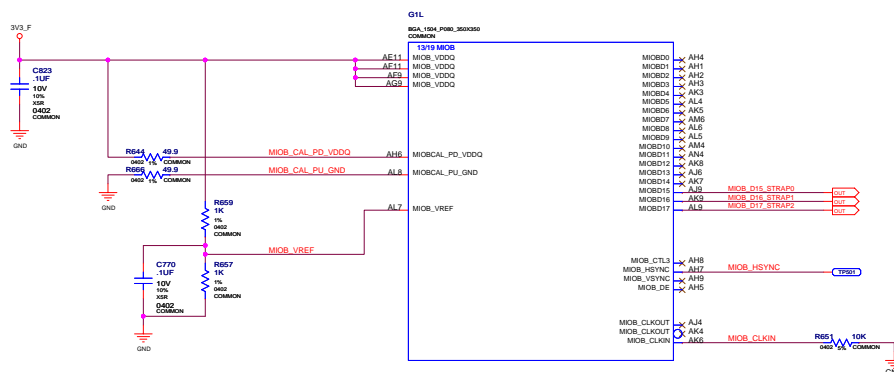
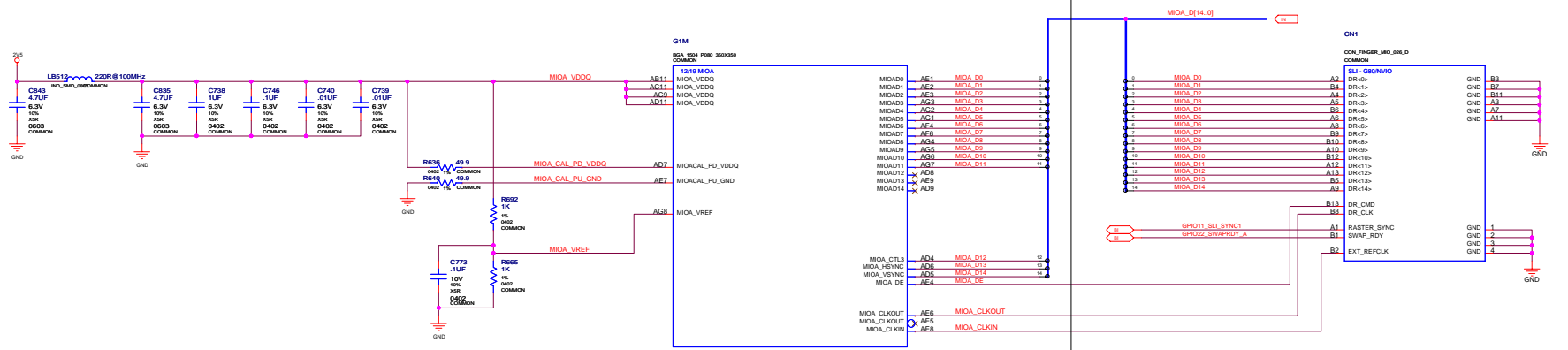






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PAGE DETAIL	DACB and HDTV/SDTV-Out





ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIO A/B Interface



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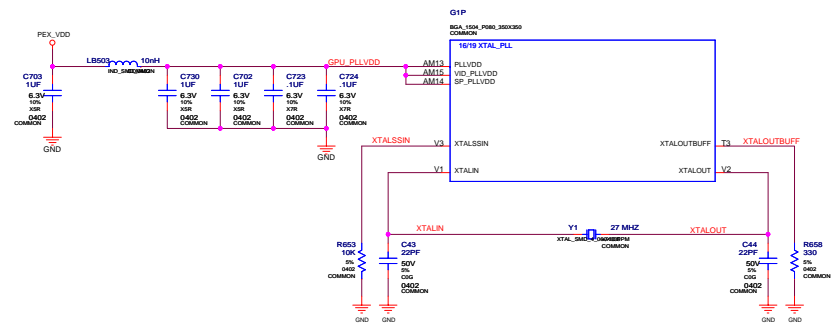
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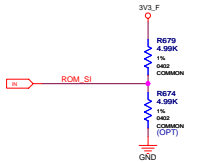
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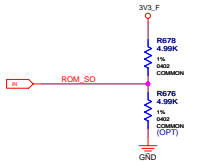
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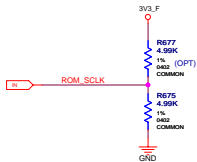
GPIO	I/O	Function
0	IN	DVI HOTPLUG DET A
1	N/A	HDMI HOTPLUG DET B
2	IN	SWAPREADY
3	N/A	NVDD PHASE CONTROL
4	IN	VOLTAGE SELECT 0
5	OUT	VOLTAGE SELECT 1
6	OUT	FBVDD VOLTAGE CONTROL
7	IN	GPIO SLOW
9	OUT	PWM FAN CONTROL
10	UNUSED	
11	N/A	SLT_RSTASYNC_SYNC
12	IN	EXT_12V DETECT
13	OUT	
14	UNUSED	
15	UNUSED	
16	IN	DP_MODE
17	IN	HDMI_F
18	UNUSED	
19	UNUSED	HDMI_CEC
20	IN	DP HOTPLUG DET F
21	UNUSED	
22	IN	SWAPREADY_A
23	OUT	UNUSED



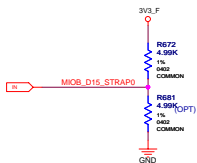
STRAP PIN	STRAP NAME	
ROM_SI	PCI_DEVID_EXT	



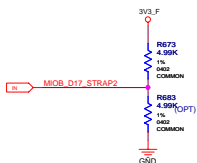
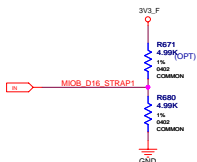
STRAP PIN	STRAP NAME	
ROM_SO	SLOT_CLK_CFG	



STRAP PIN	STRAP NAME	
ROM_SCLK	PCI_DEVID[3]	

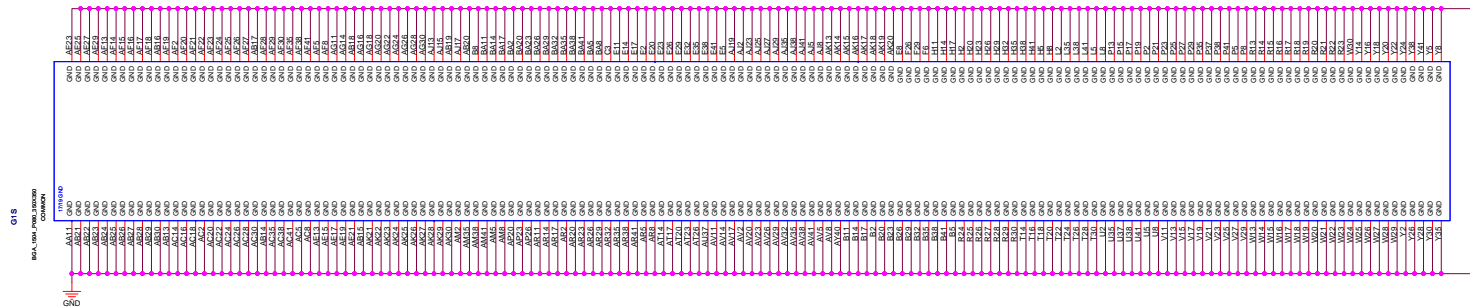
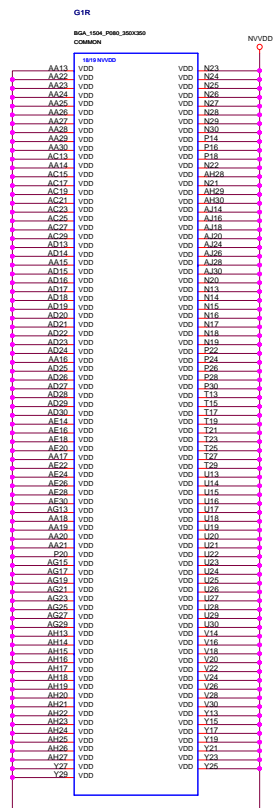


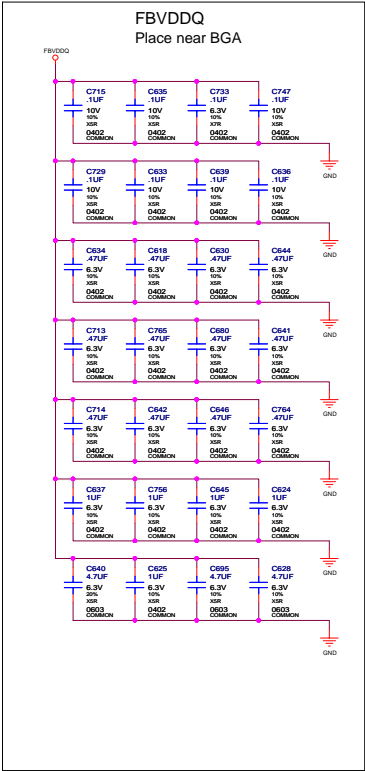
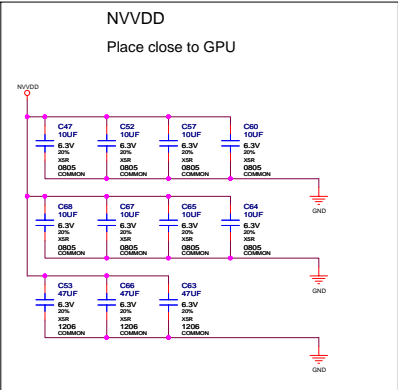
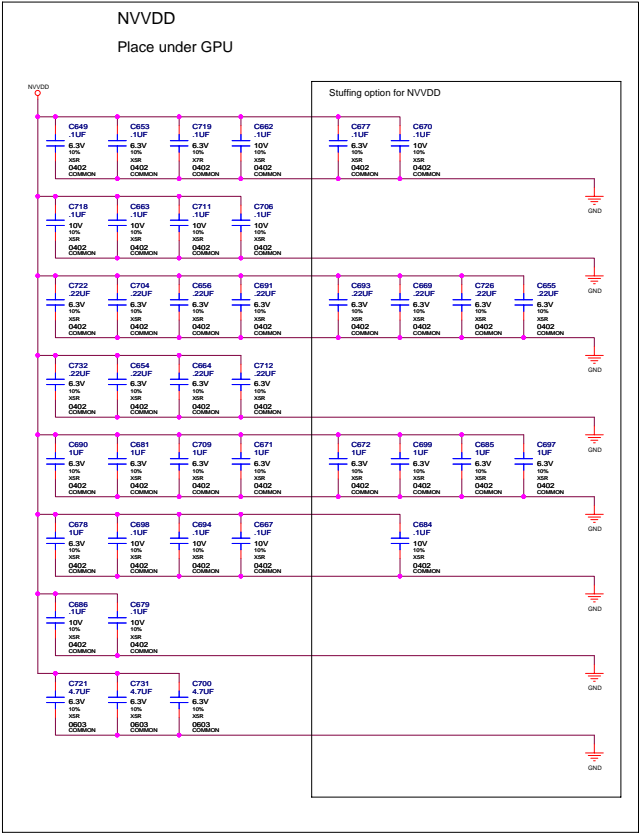
STRAP PIN	STRAP NAME	
STRAP0	RAMCFG0	
STRAP1	RAMCFG1	
STRAP2	RAMCFG2	



3V3	GND
5K	1
	0

MSI	MSI
ACM0	NC
ACM1	NC
ACM2	NC
ACM3	NC
AFS0	NC
AFS1	NC
AFS2	NC
AFS3	NC
AGS0	NC
AGS1	NC
AGS2	NC
AGS3	NC
AMS0	NC
AMS1	NC
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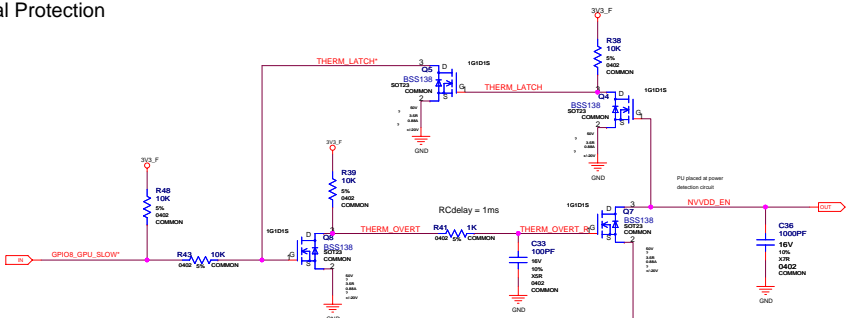


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ASSEMBLY PAGE DETAIL
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NVVDD and FBVDDQ Decoupling

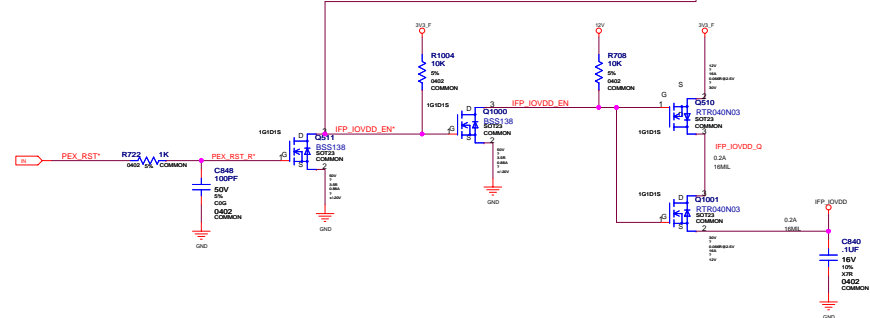
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Thermal Protection

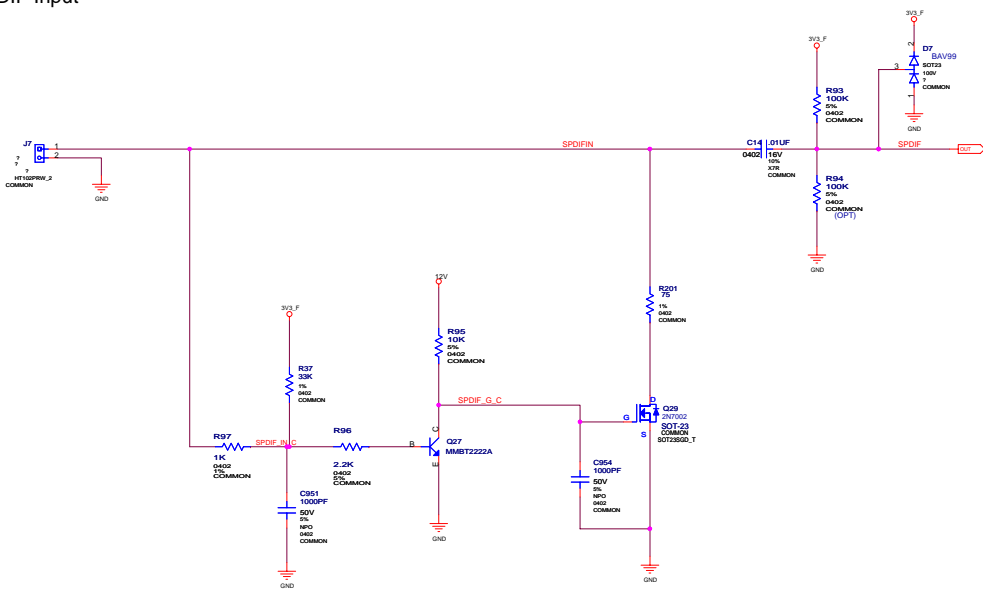


IFP_IOVDD Backdrive Prevention

Sniffing possibilities for thermal control and protection:




SPDIF Input



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ASSEMBLY PAGE DETAIL P541 BASE LEVEL GENERIC SCHMATIC ONLY. COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL SPDIF Input, Backdrive Protection, and IFP_IOVDD Power Supply



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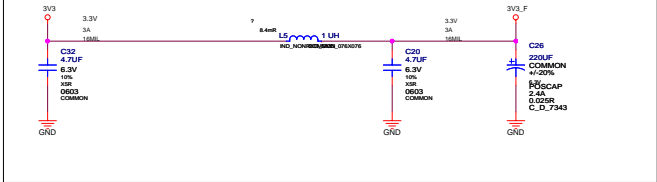
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3V3 Power Supply Filter

3V3_F = 3.3V @ 2.5A



12V Power Supply Filter

12V_F = 12V @ 5.5A

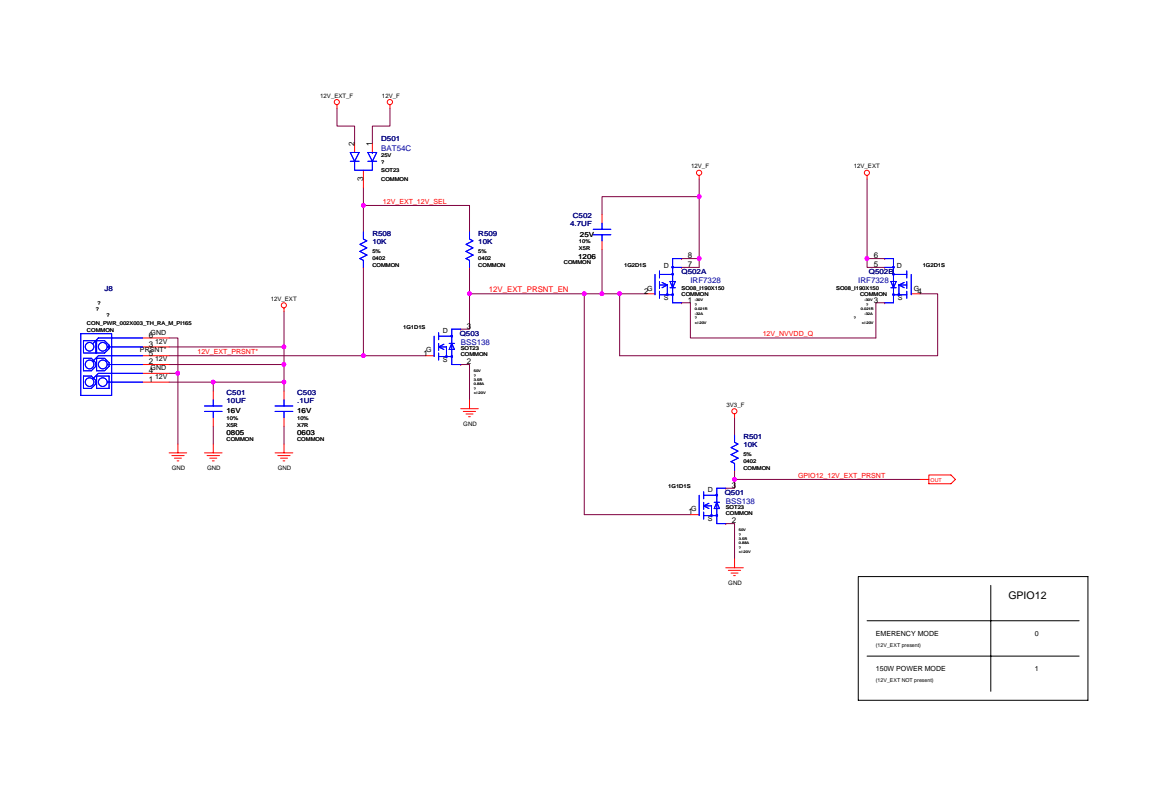


12V_EXT Power Supply Filter

12V_EXT_F = 12V @ 6.25A



INPUT POWER SELECTION for NVVDD



GPIO12	
EMERGENCY MODE (12V_EXT present)	0
150W POWER MODE (12V_EXT NOT present)	1

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V_EXT	12V	6.25A	100MIL
12V	12V	5.5A	100MIL
GND	0V	20A	100MIL

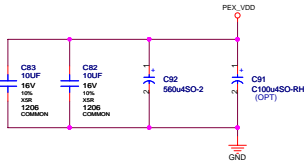


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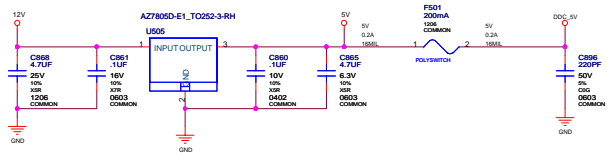
Code



5V and DDC_5V Power Supply

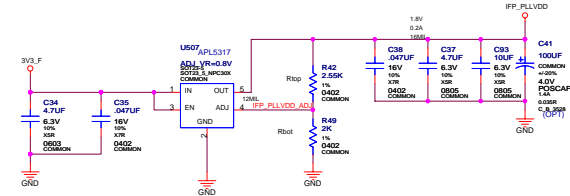
DDC_5V = 5V @ 200mA

LAYOUT NOTE: ADD MIN 203MM² COPPER AROUND THIS DPAK FOR HEAT DISSIPATION



IFP_PLLVDD Power Supply

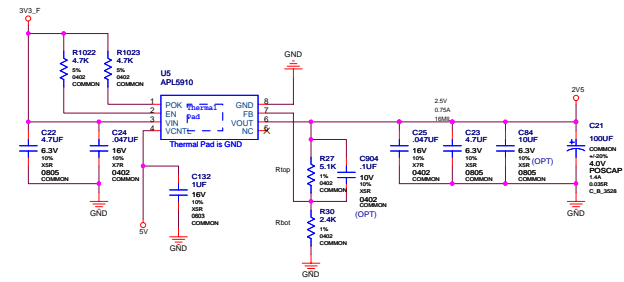
IFP_PLLVDD = 1.8V @ 200mA



$$\text{IFP_PLLVDV} = \text{VREF} * (1 + (\text{Rtop} / \text{Rbot}))$$

$$1.82\text{V} = 0.8\text{V} * (1 + (2.5\text{K}/2\text{K}))$$

2V5 Power Supply

$$2V5 = 2.5V @ 750mA$$


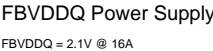
$$2.5V = 0.8V * (1 + (5.1K/2.4K))$$

ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS II: PEX_VDD, IFP_PLLVDD, 2V5, 5V, and DDC_5V Power Supply



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GPIO7	
FBVDDQ = 1.792V	0
FBVDDQ = 1.999V	1

$$\begin{aligned} \text{FBVDDQ} &= \text{VREF} * (1 + (\text{Rtop} / \text{Rbot1})) \\ 1.82\text{V} &= 0.8 * (1 + (2.55\text{K} / 2\text{K})) \\ \text{FBVDDQ} &= \text{VREF} * (1 + (\text{Rtop} / (\text{Rbot1} // \text{Rbot2}))) \\ 2.02\text{V} &= 0.8 * (1 + (2.55\text{K} / (2\text{K} // 10\text{K}))) \\ \text{FBVDD} &= 0.8\text{V} * (1 + (1.3\text{K} / (1.1\text{K} // 10\text{K})) = 1.84\text{V} \\ \text{FBVDD} &= 0.8\text{V} * (1 + 1.3\text{K} / 1.1\text{K}) = 1.745\text{V} \end{aligned}$$
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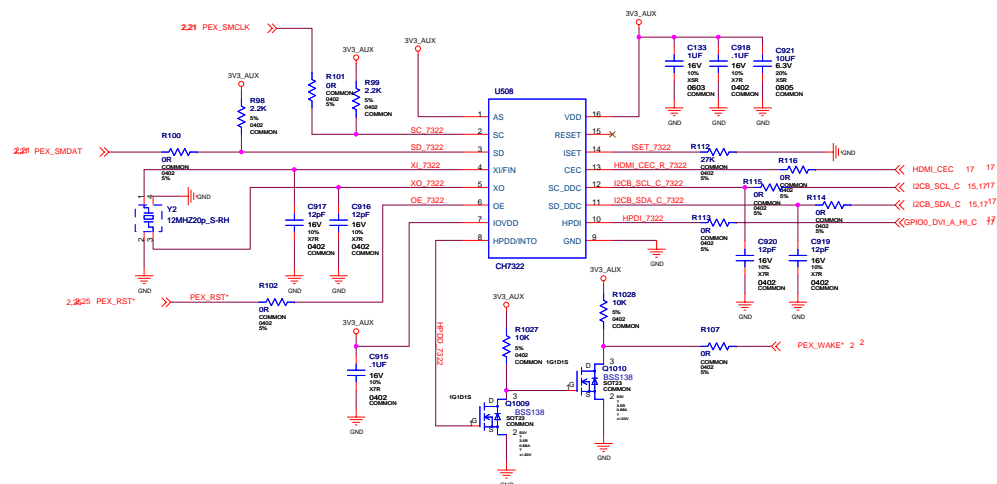
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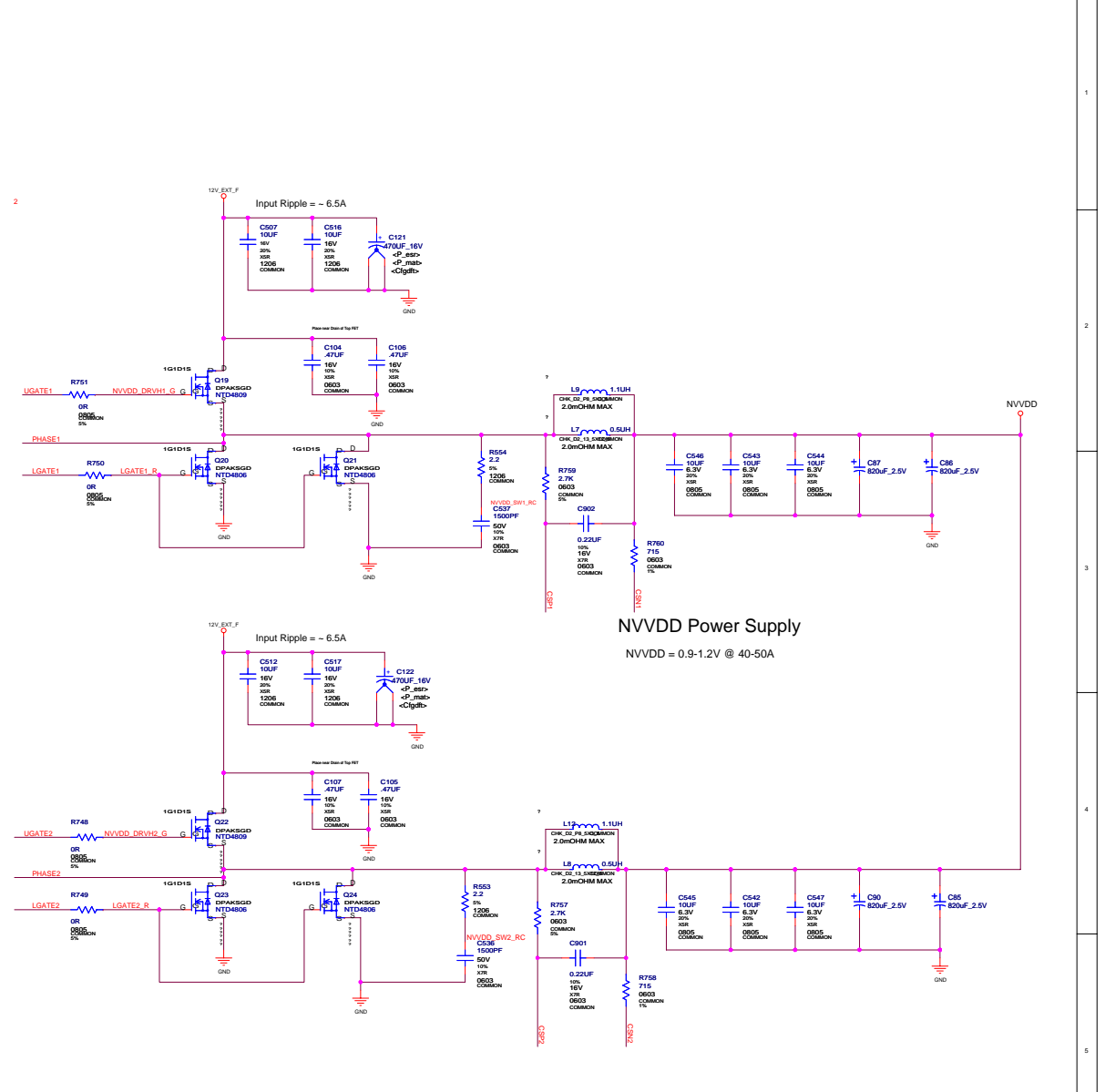
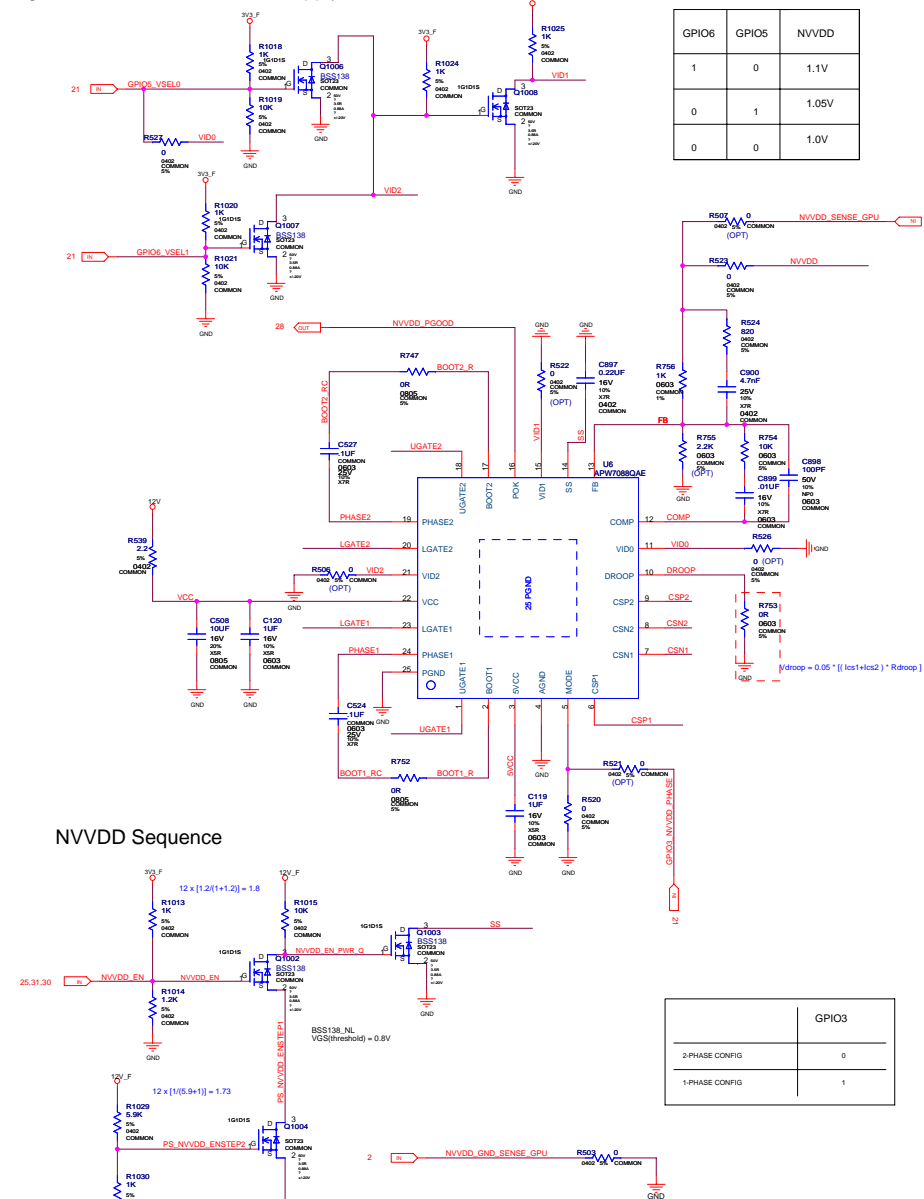
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1



NVDD Voltage Select									
NVDD range 0.80V-1.40V									
Register: ADDR08									
Control via NV_GPIOs NV_VSEL[1:0]									
VDD					NVDD				
6	5	4	3	10	Vout				G94
0	1	1	0	0	0.80V				
0	1	1	0	1	0.85V				
0	1	1	0	0	0.90V				
0	1	1	1	0	0.95V				
0	1	1	1	0	1.00V				⇒ Default
0	1	1	1	1	1.05V				⇒ Voltage1
0	1	0	0	0	1.10V				⇒ Voltage2
0	0	1	1	0	1.15V				
0	0	1	0	0	1.20V				
0	0	1	1	0	1.25V				
0	0	1	0	0	1.30V				
0	0	1	1	0	1.35V				
0	0	1	1	0	1.40V				



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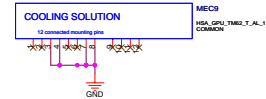
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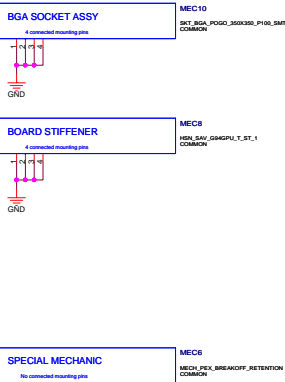


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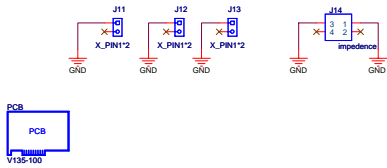
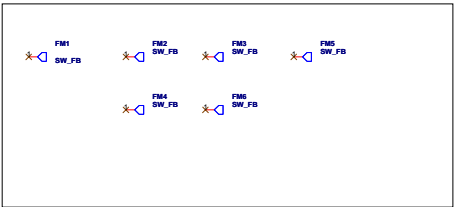
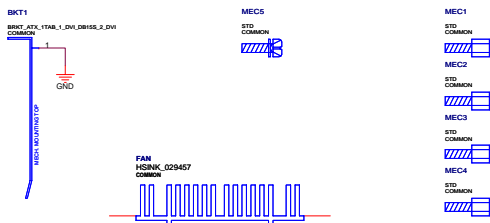
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Mechanical



Bracket



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