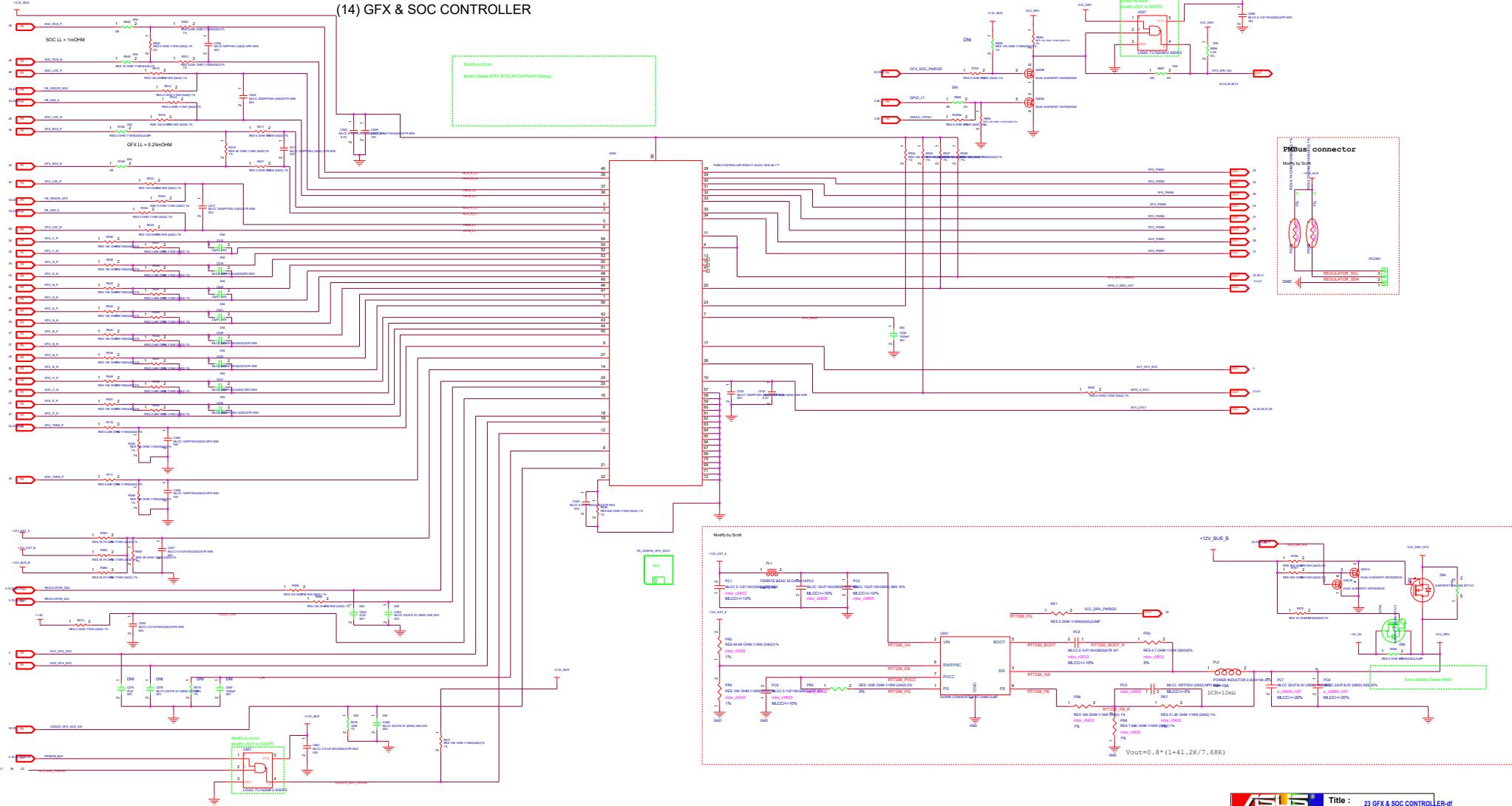
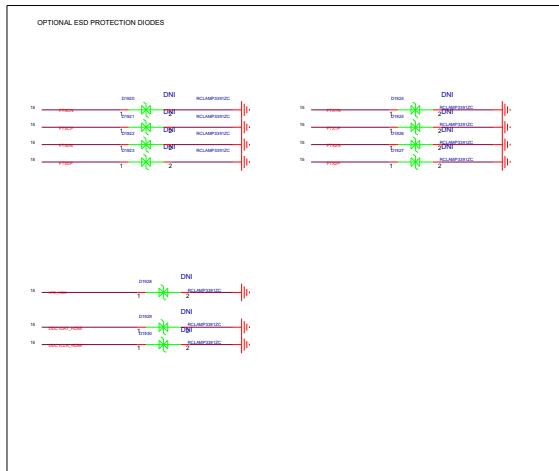
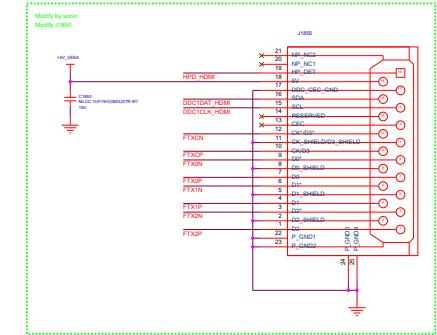
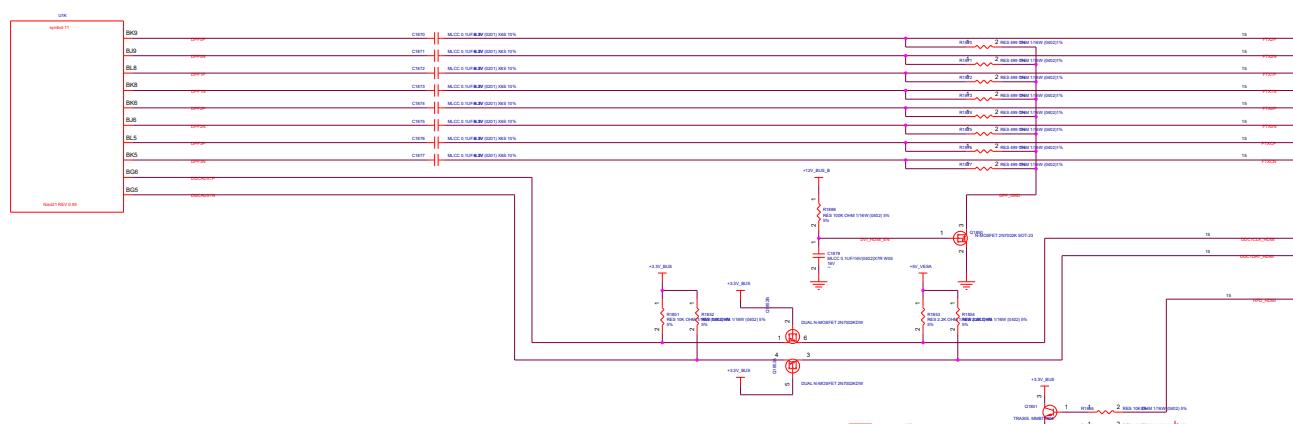
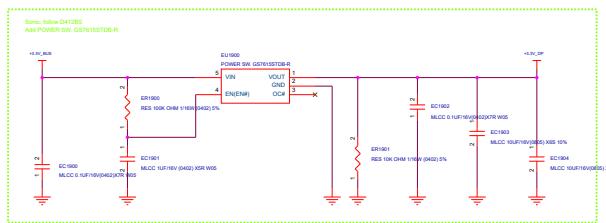
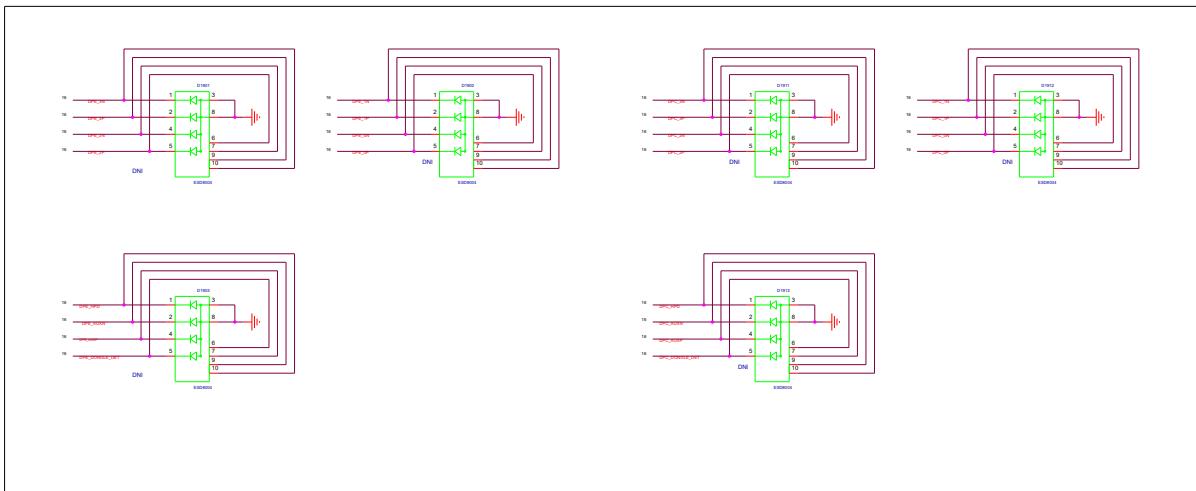
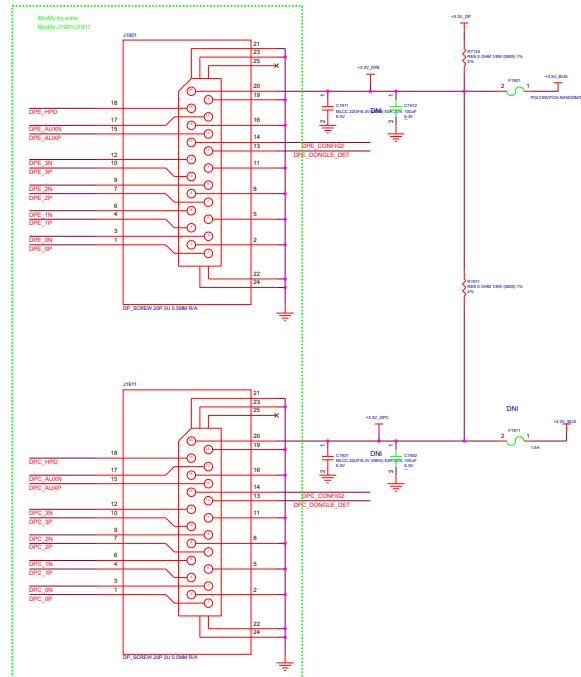
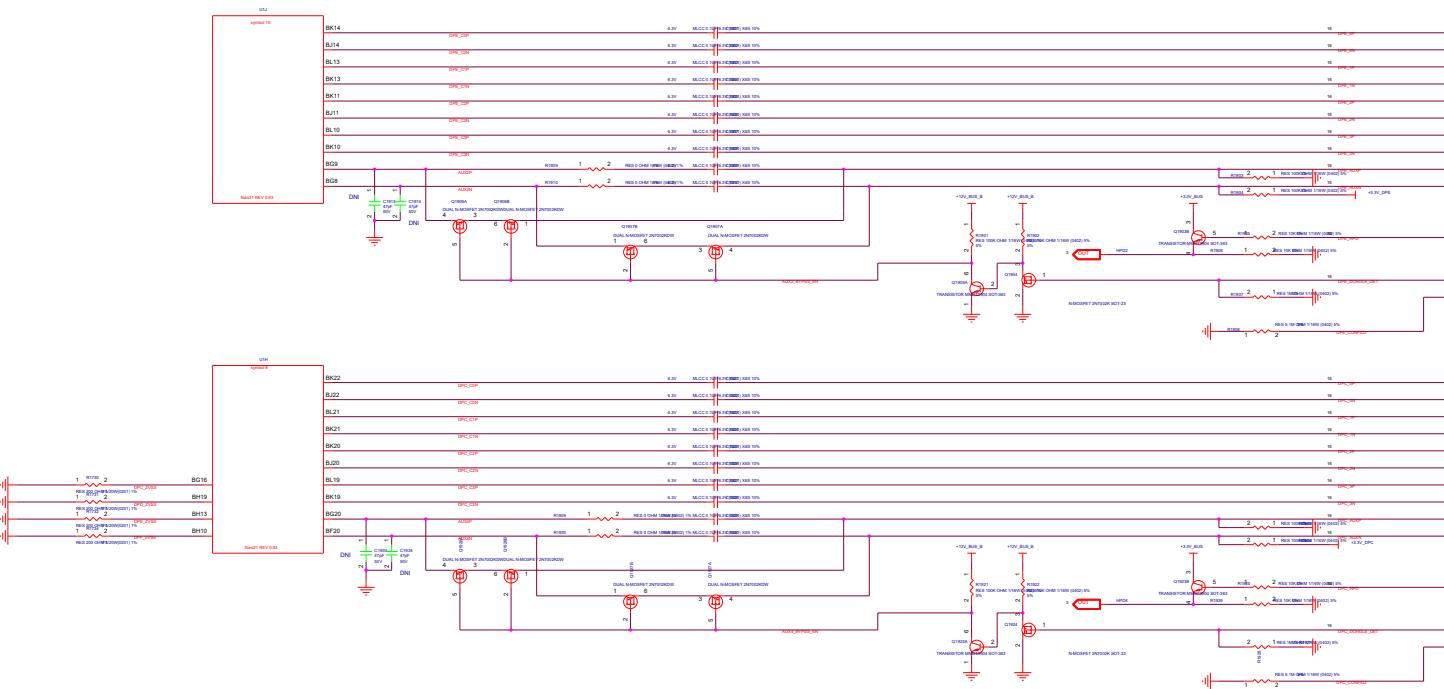
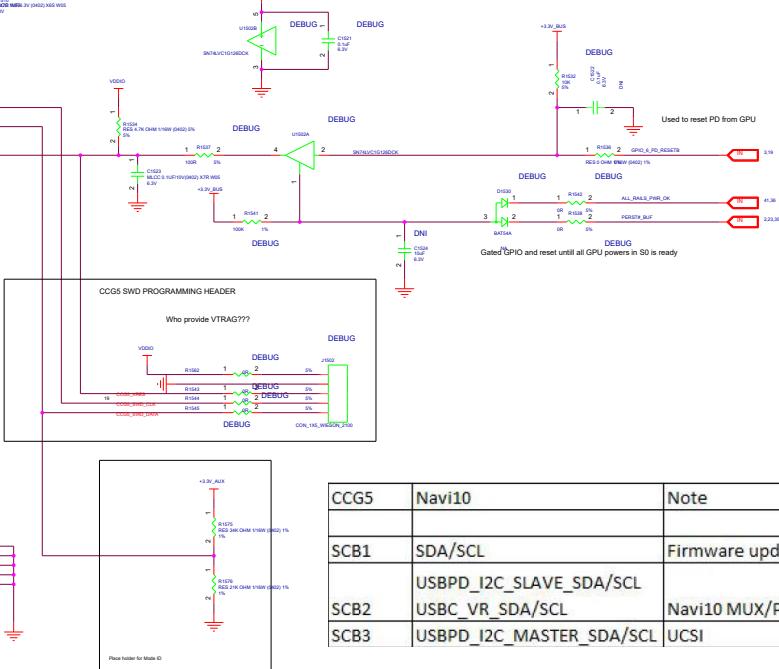
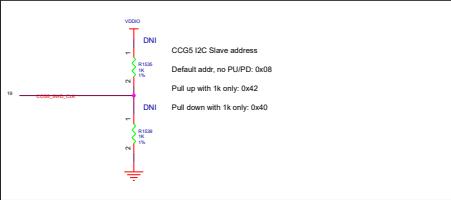
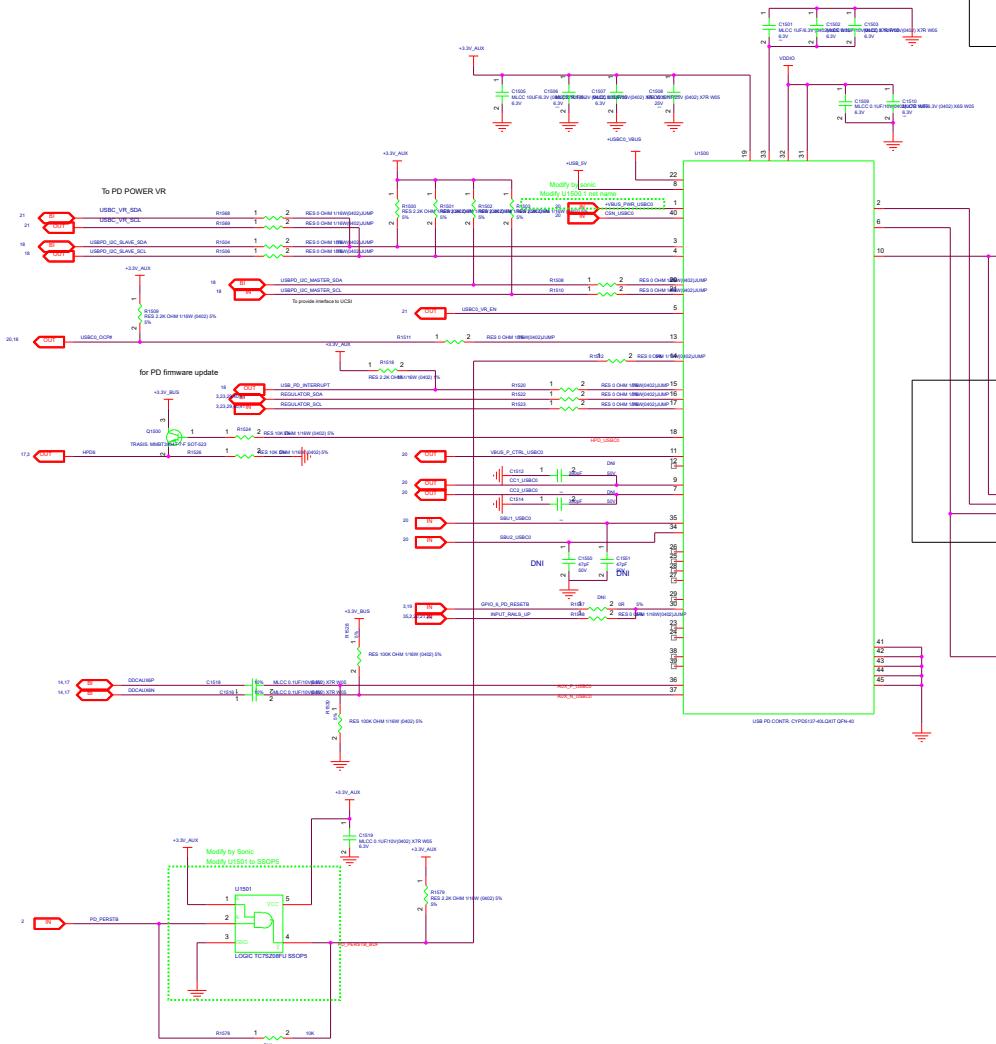


## (14) GFX & SOC CONTROLLER

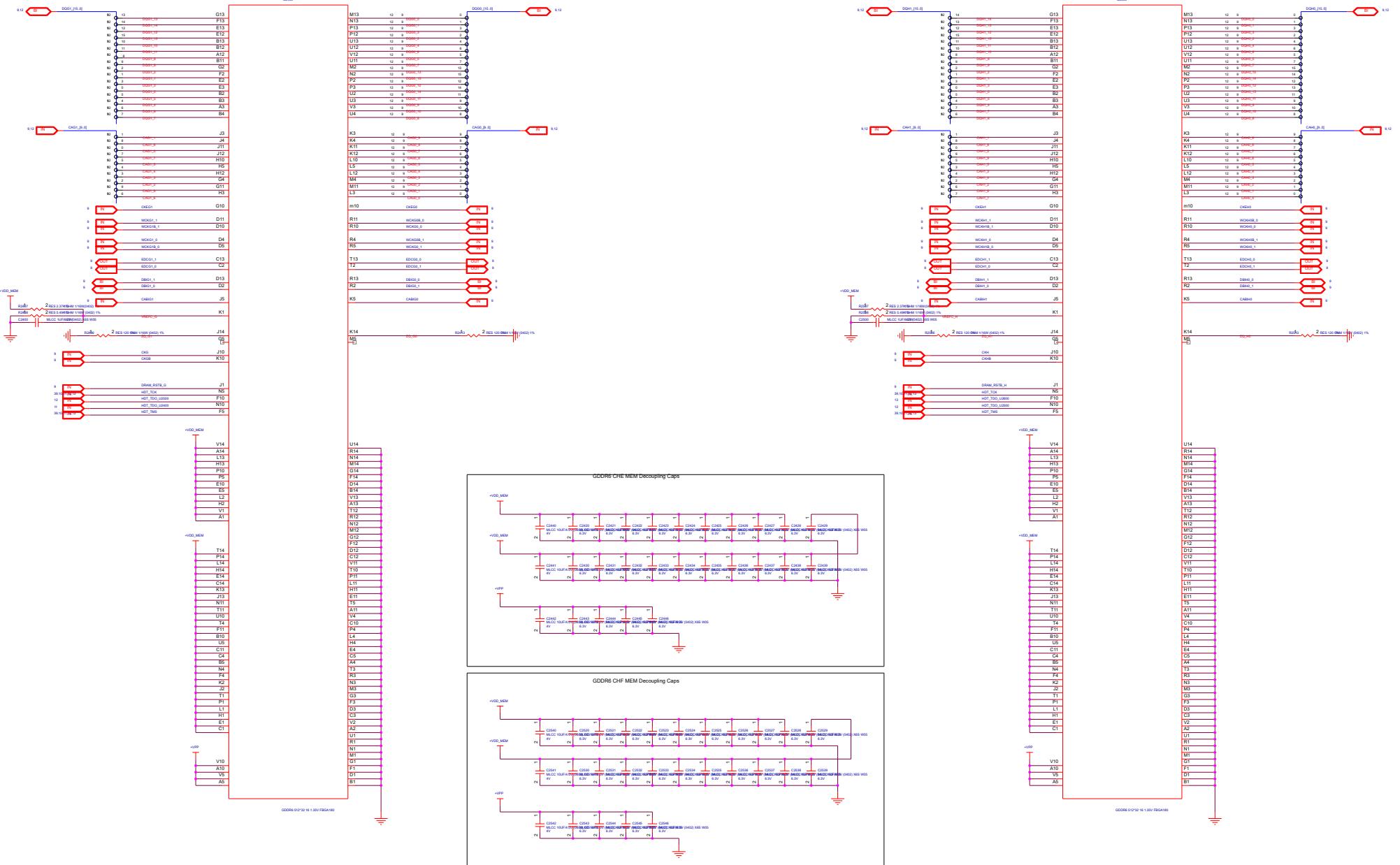


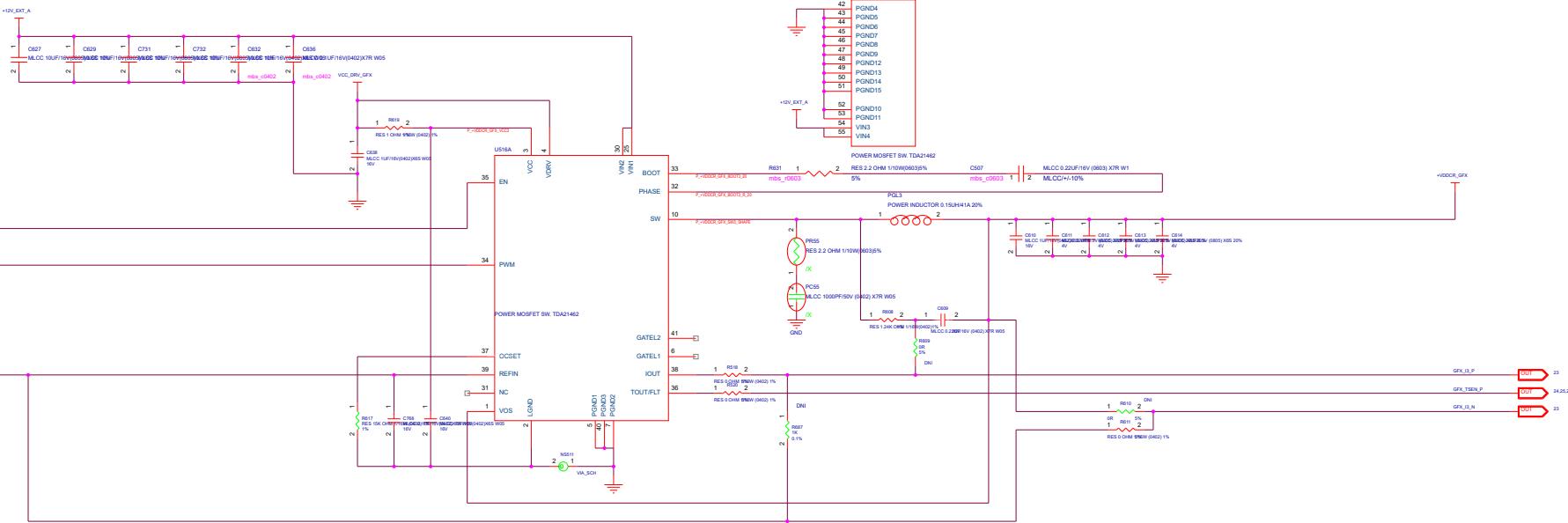


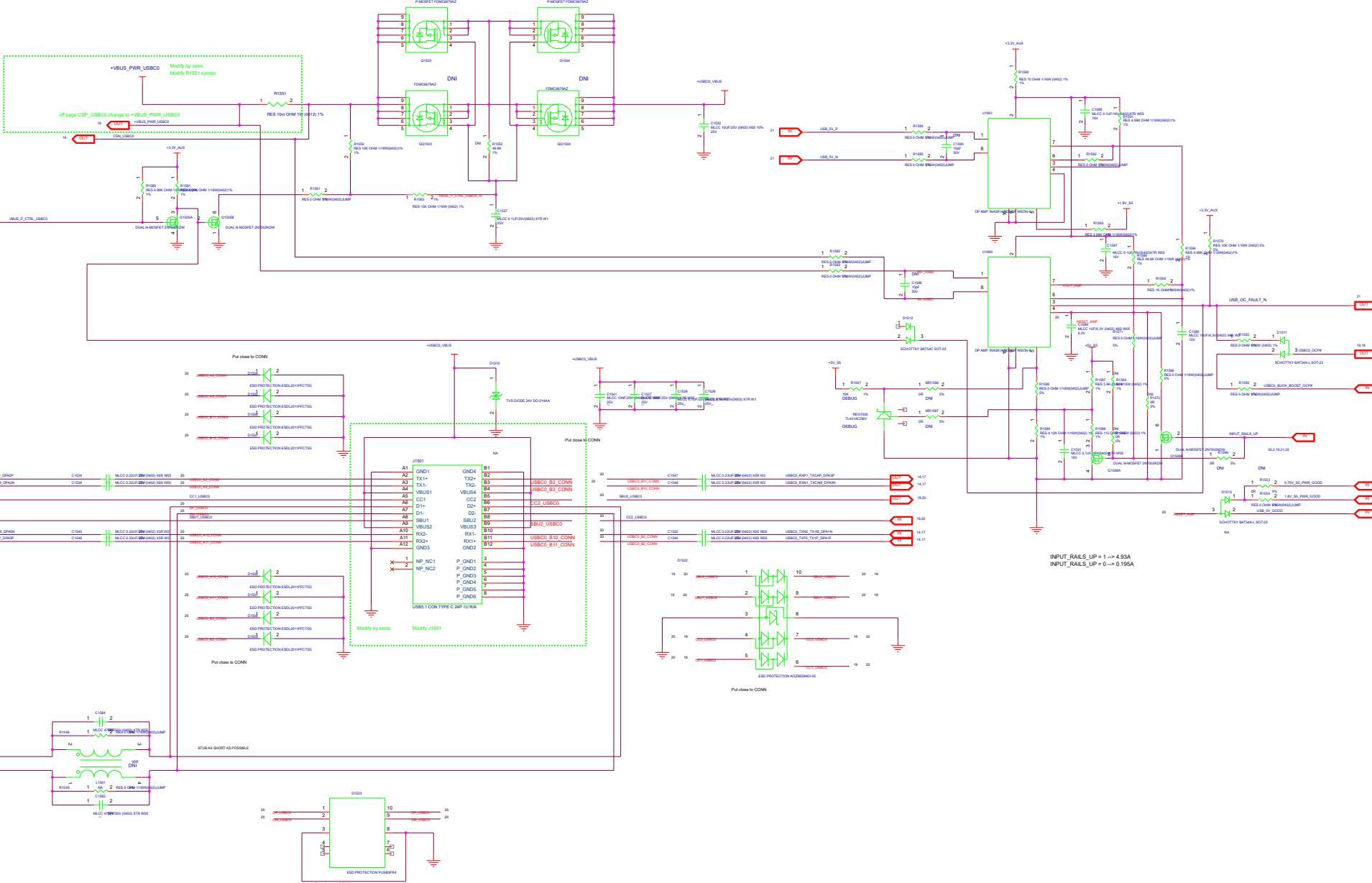


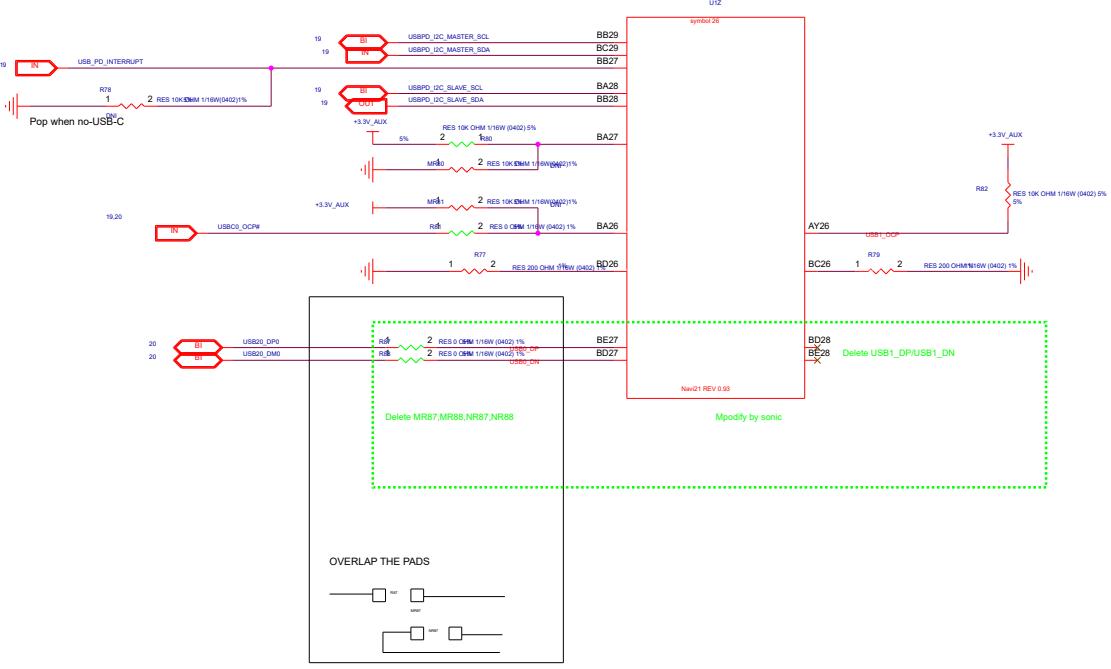


CCG5	Navi10	Note
SCB1	SDA/SCL	Firmware update/SMU
SCB2	USBPD_I2C_SLAVE_SDA/SCL USBC_VR_SDA/SCL	Navi10 MUX/PD_Regulator/re-driver
SCB3	USBPD_I2C_MASTER_SDA/SCL	UCSI



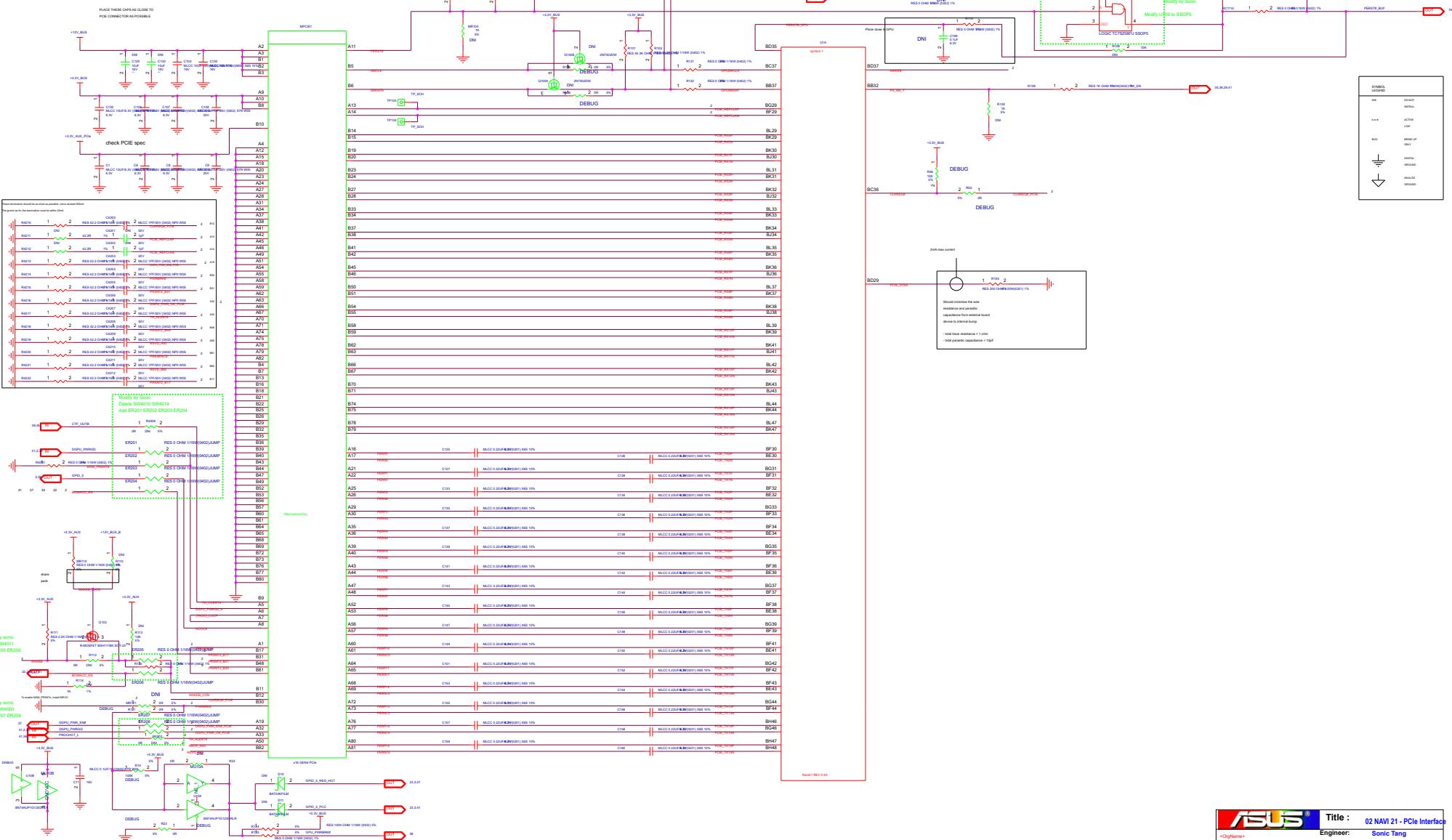


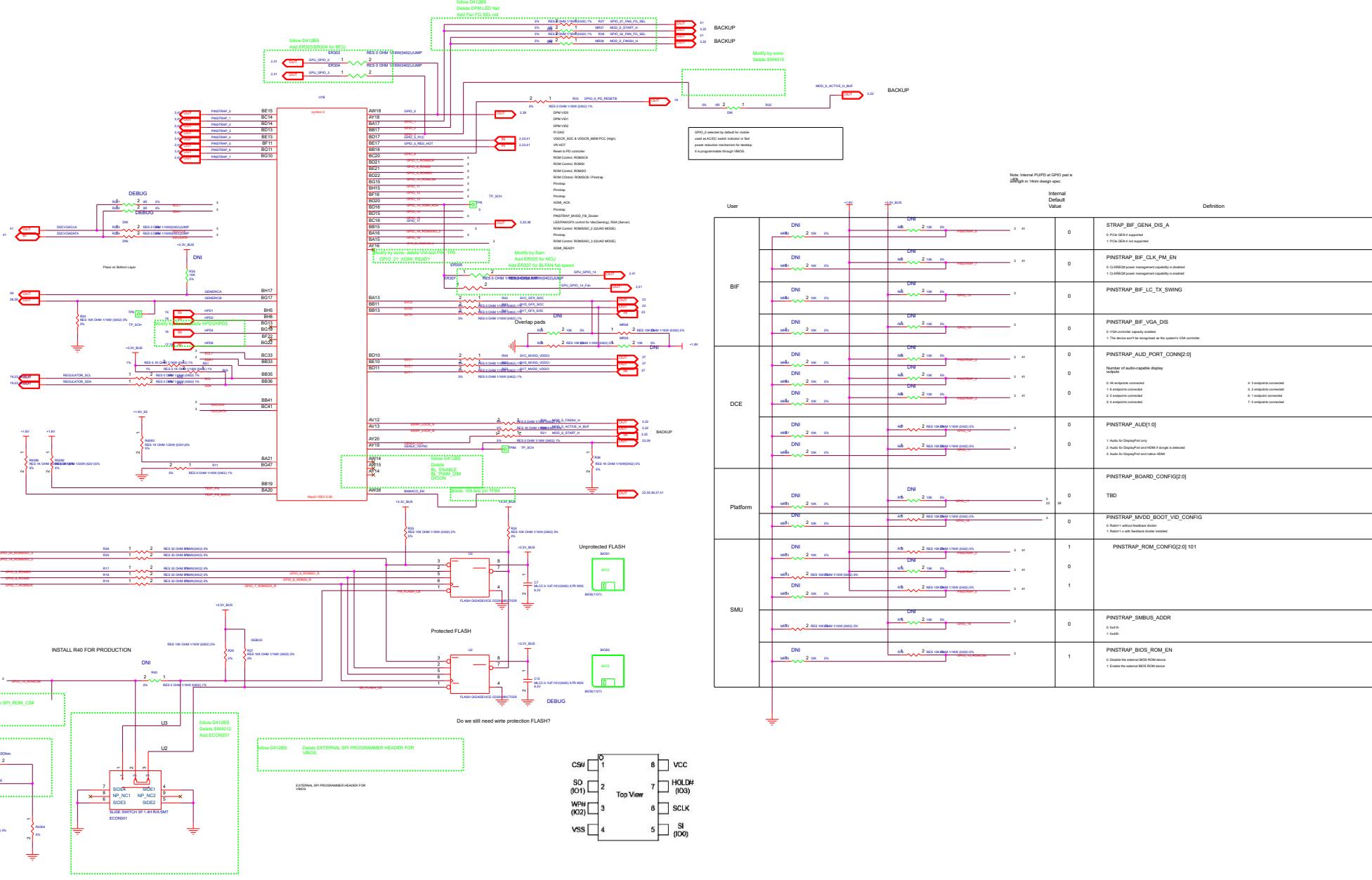


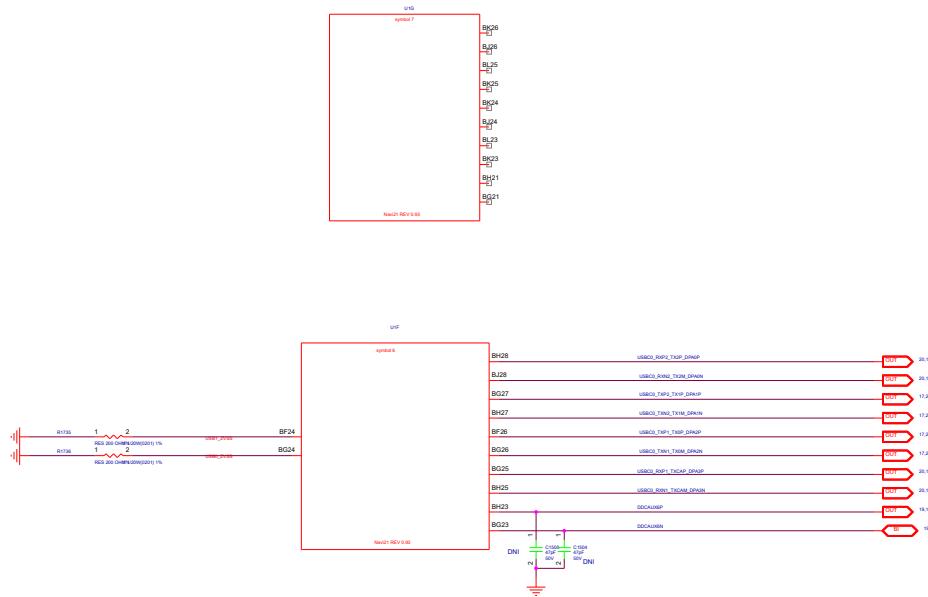


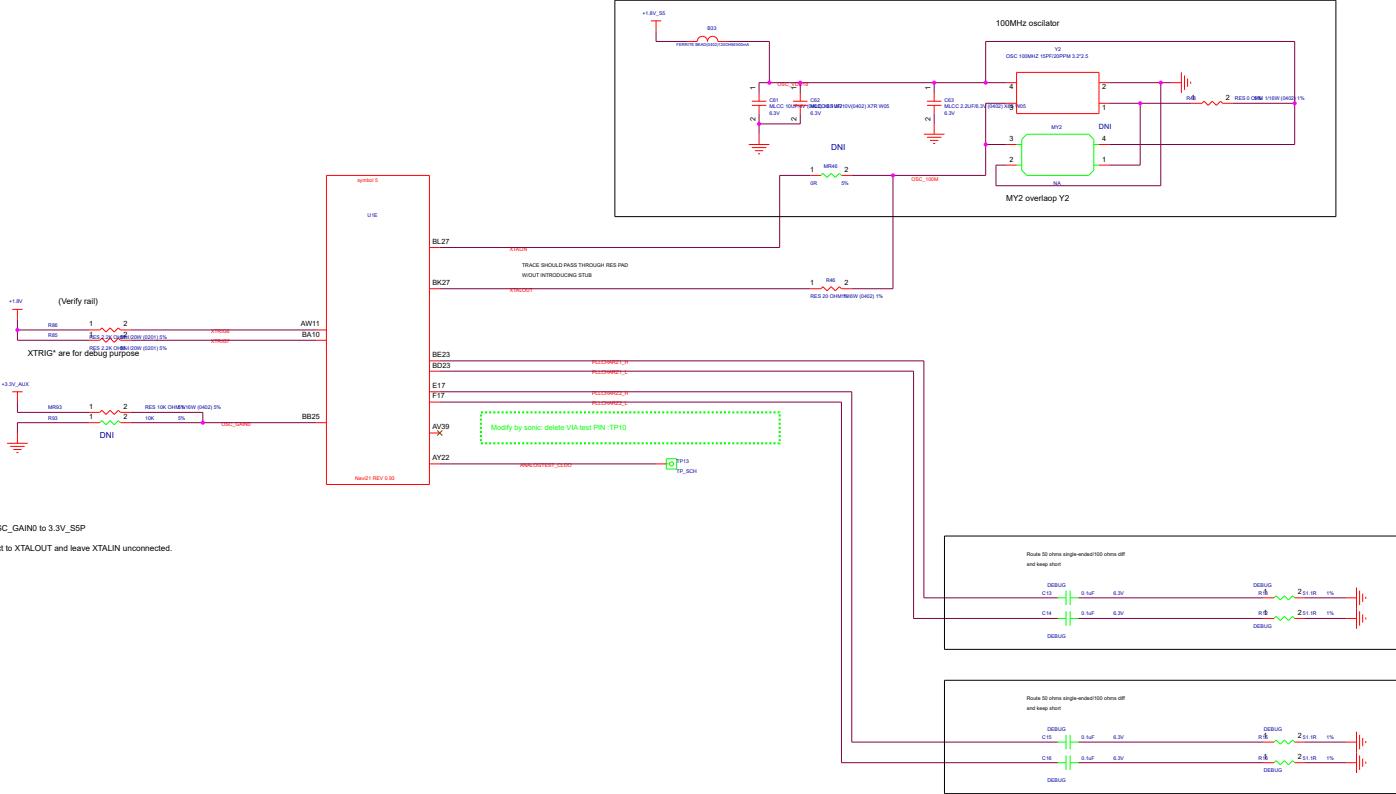
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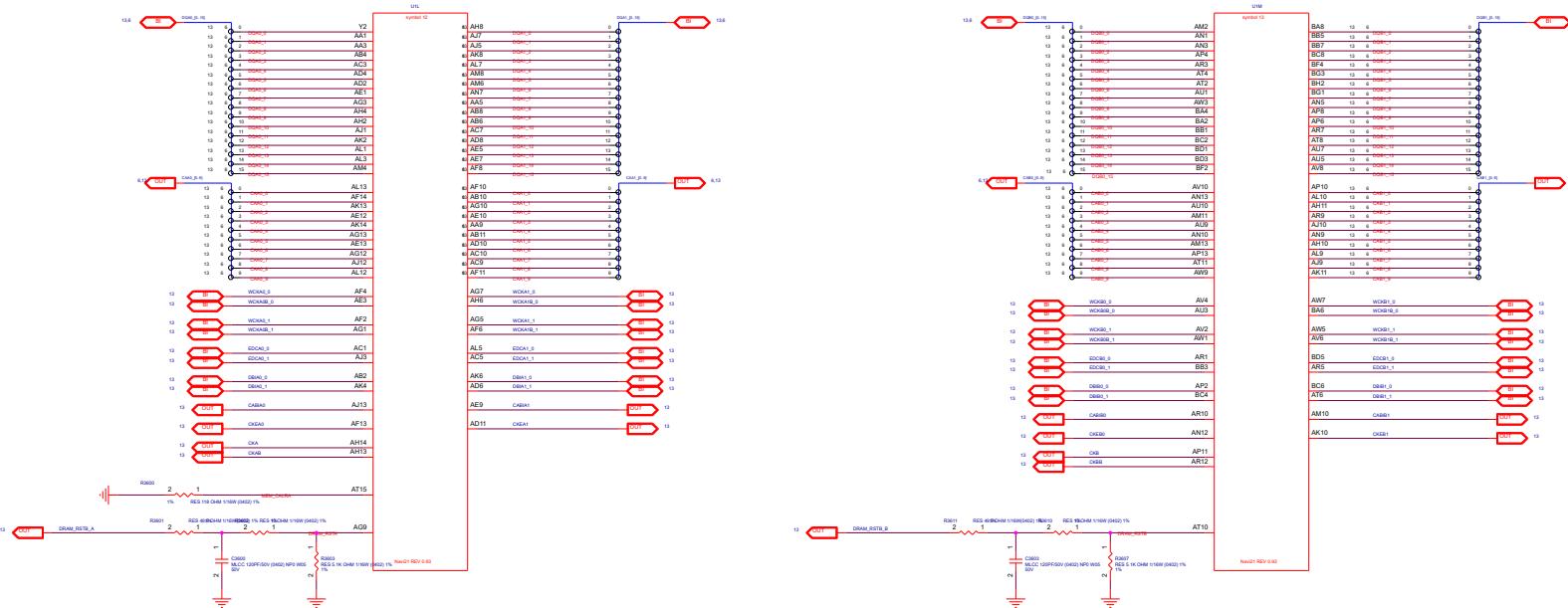


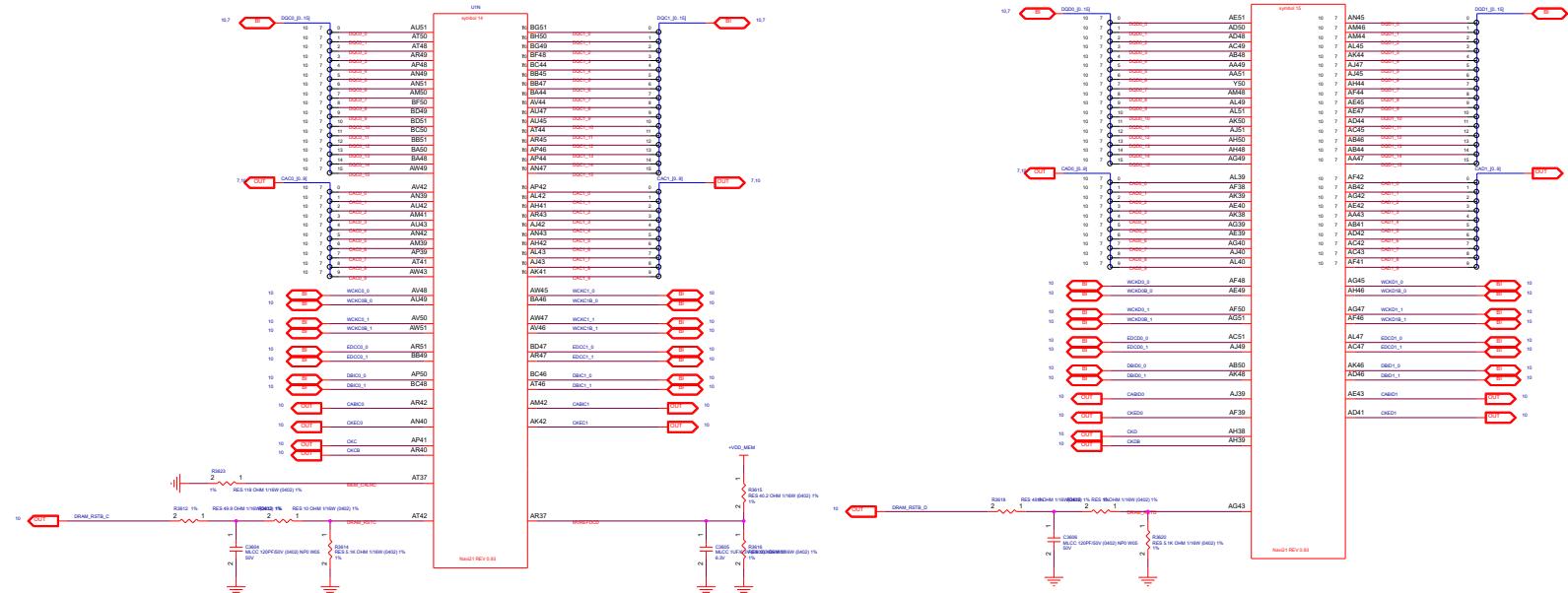


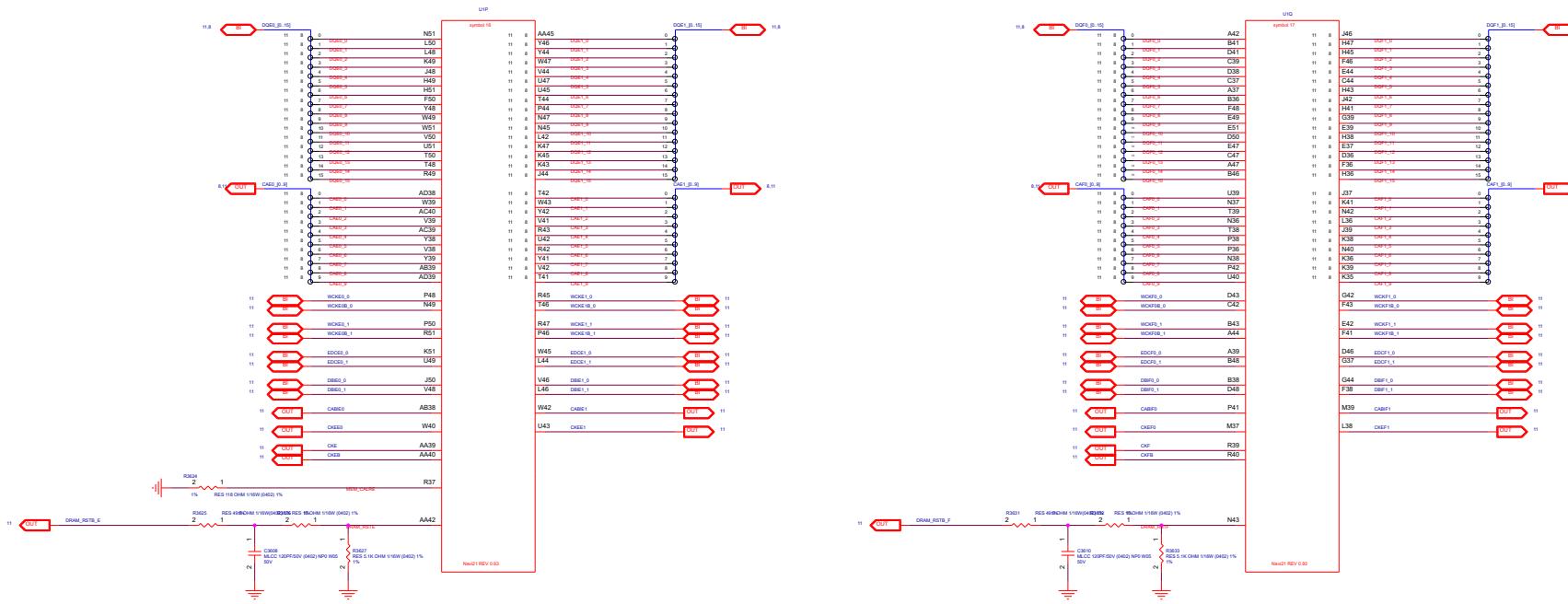


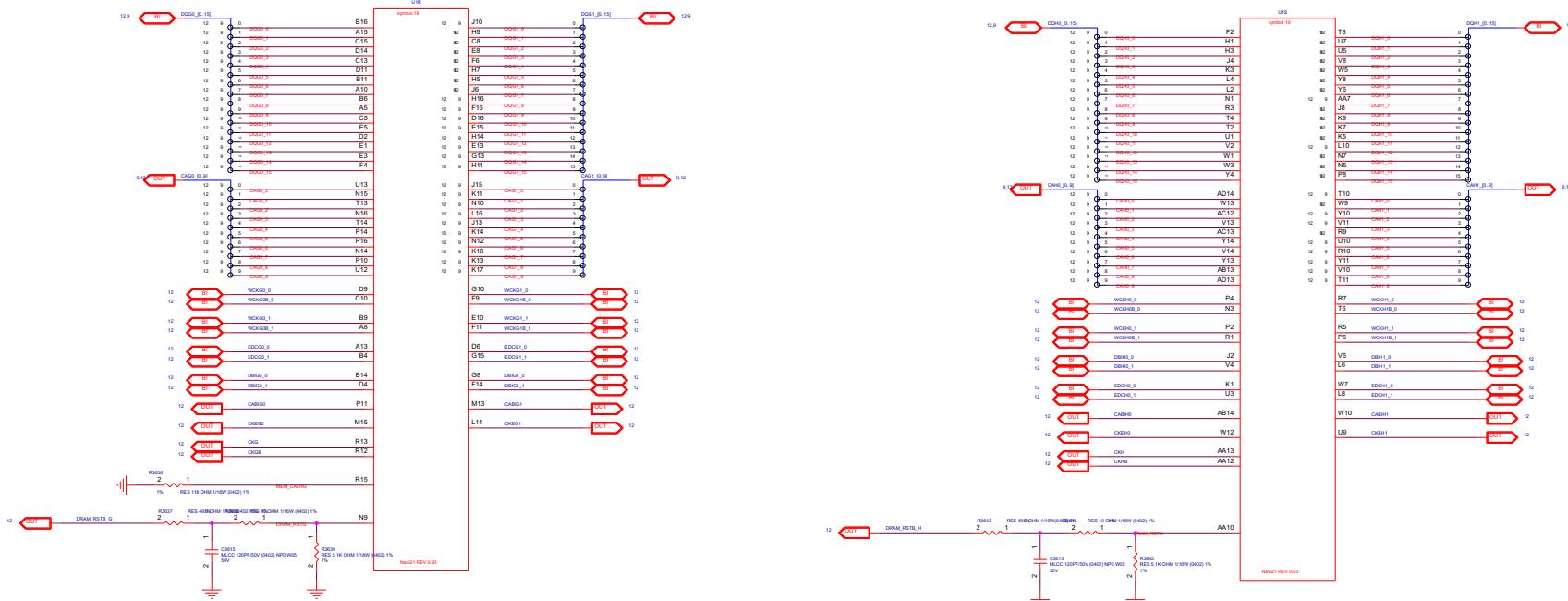


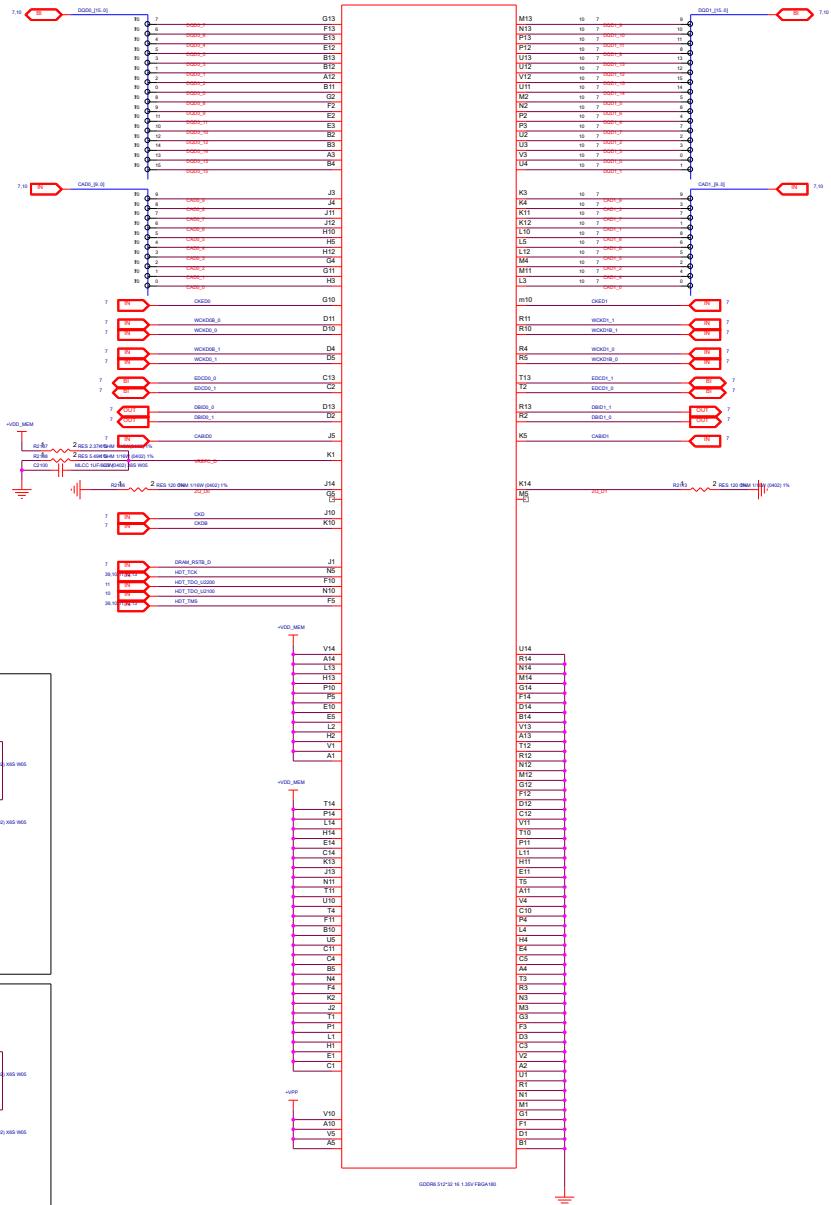
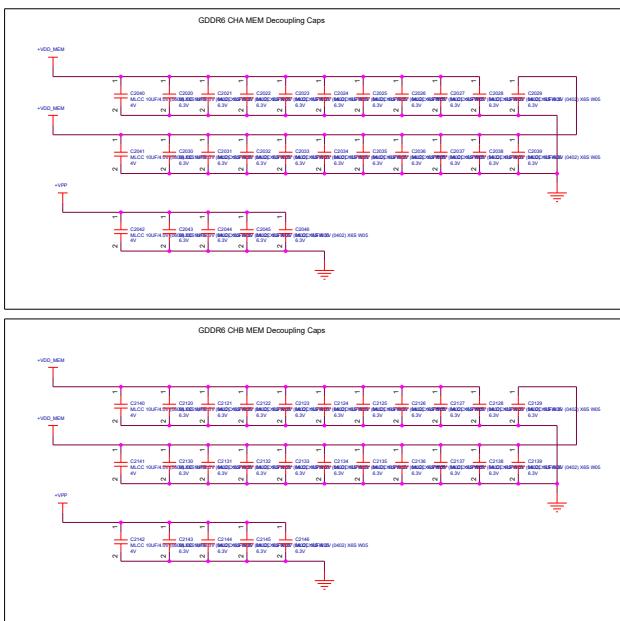
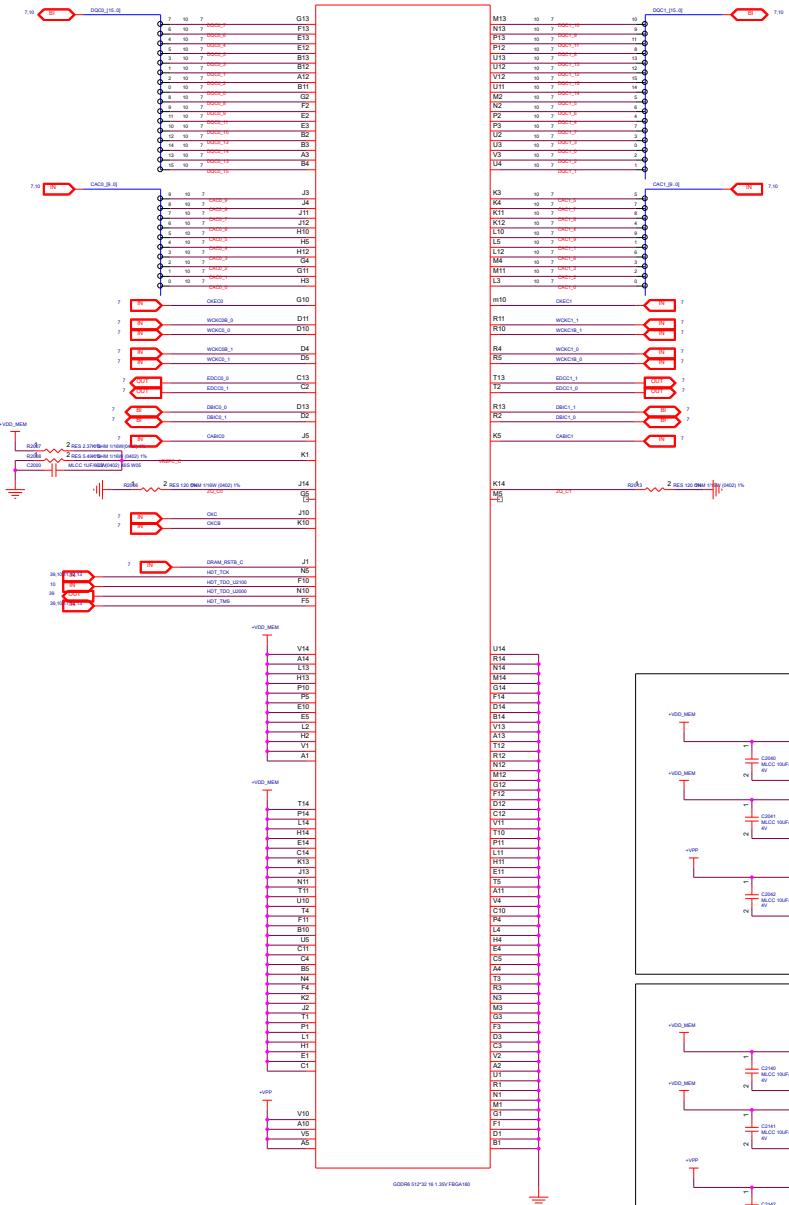


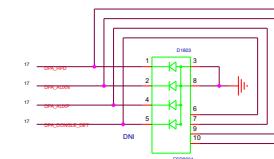
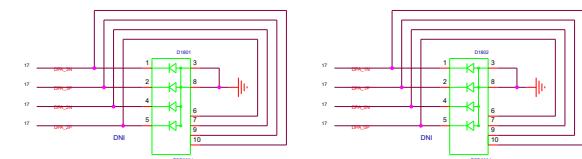
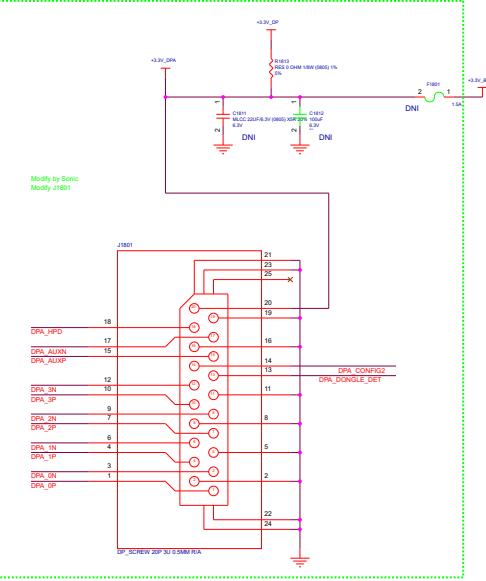
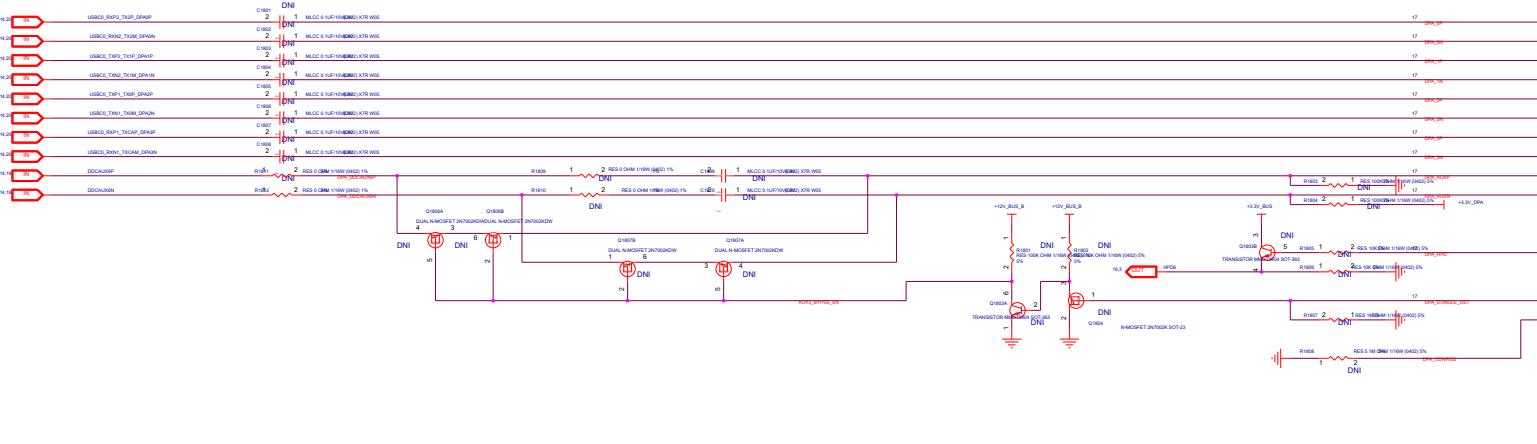


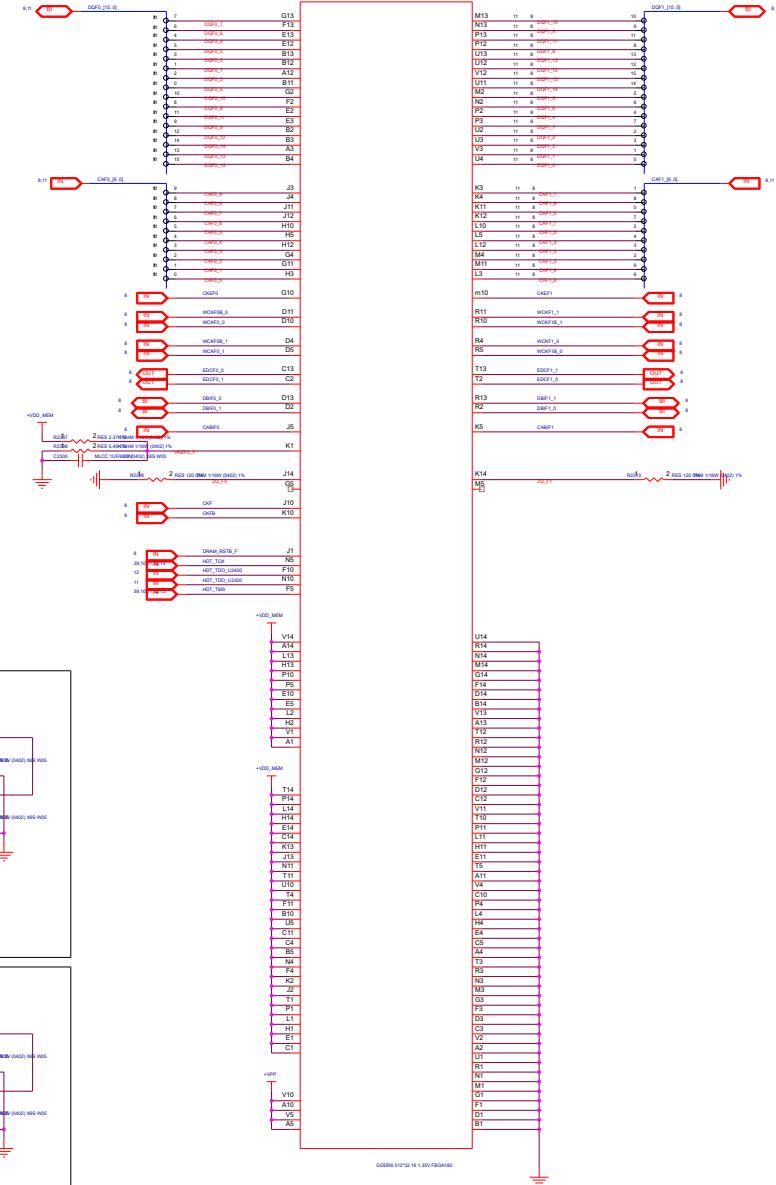
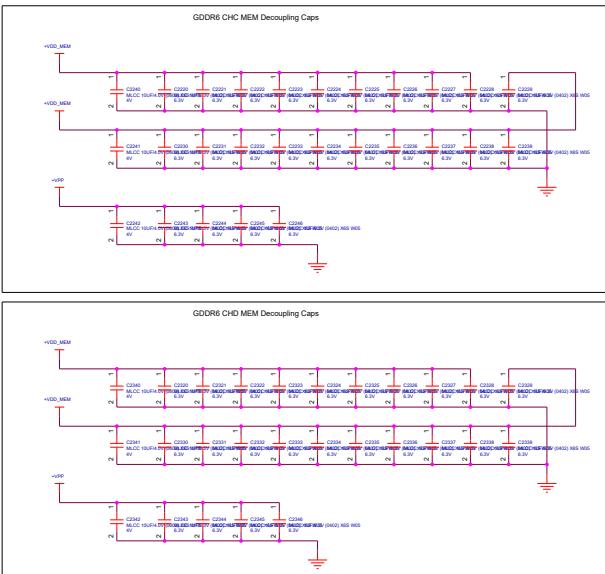
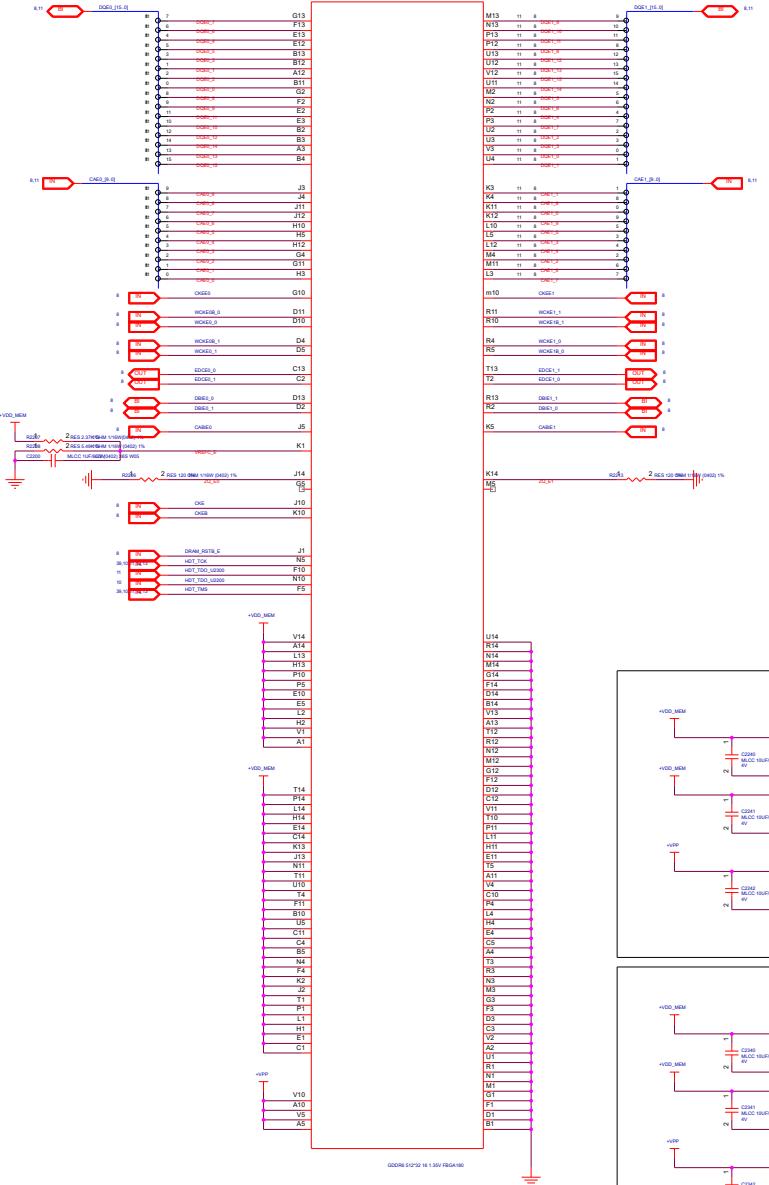


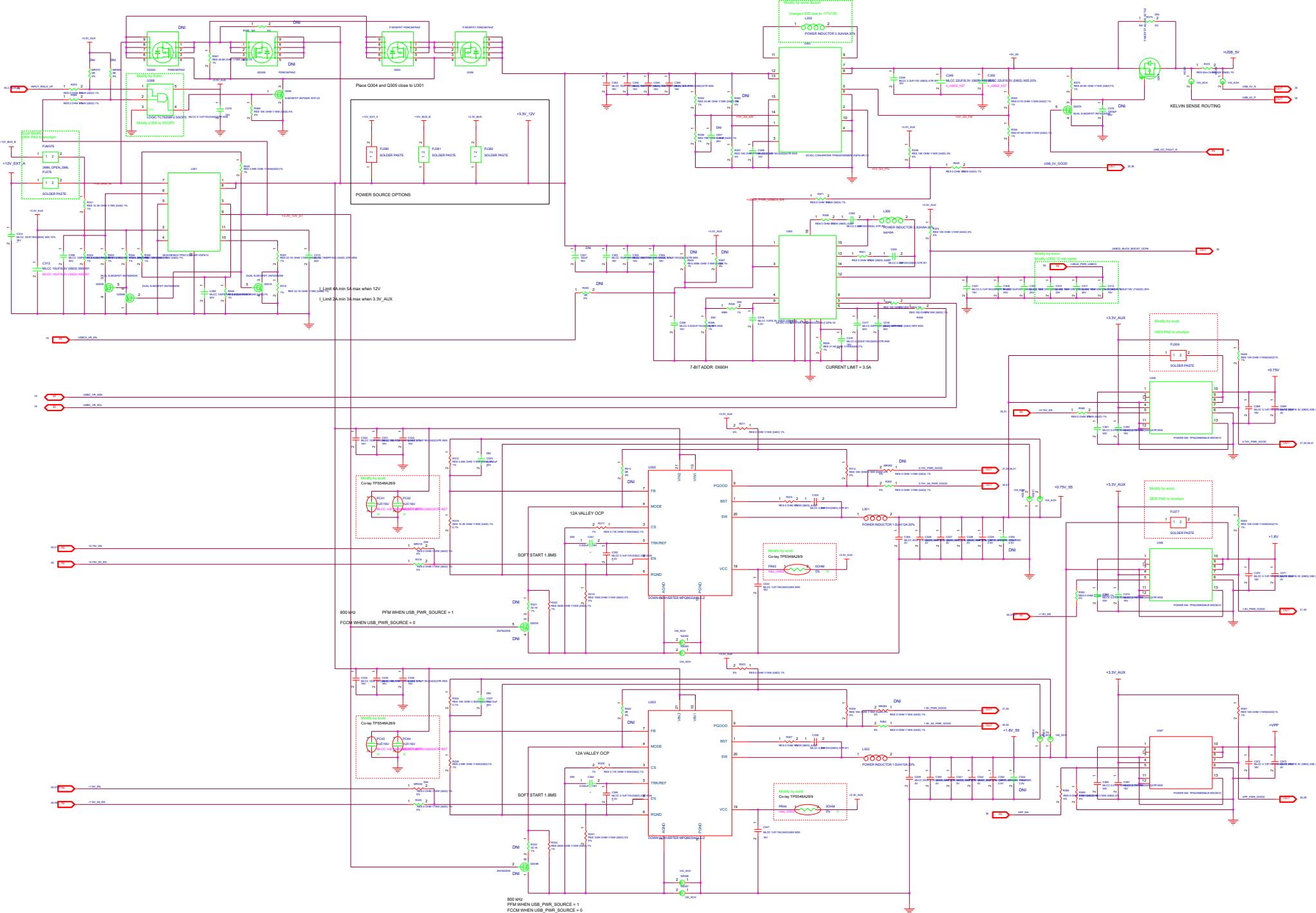


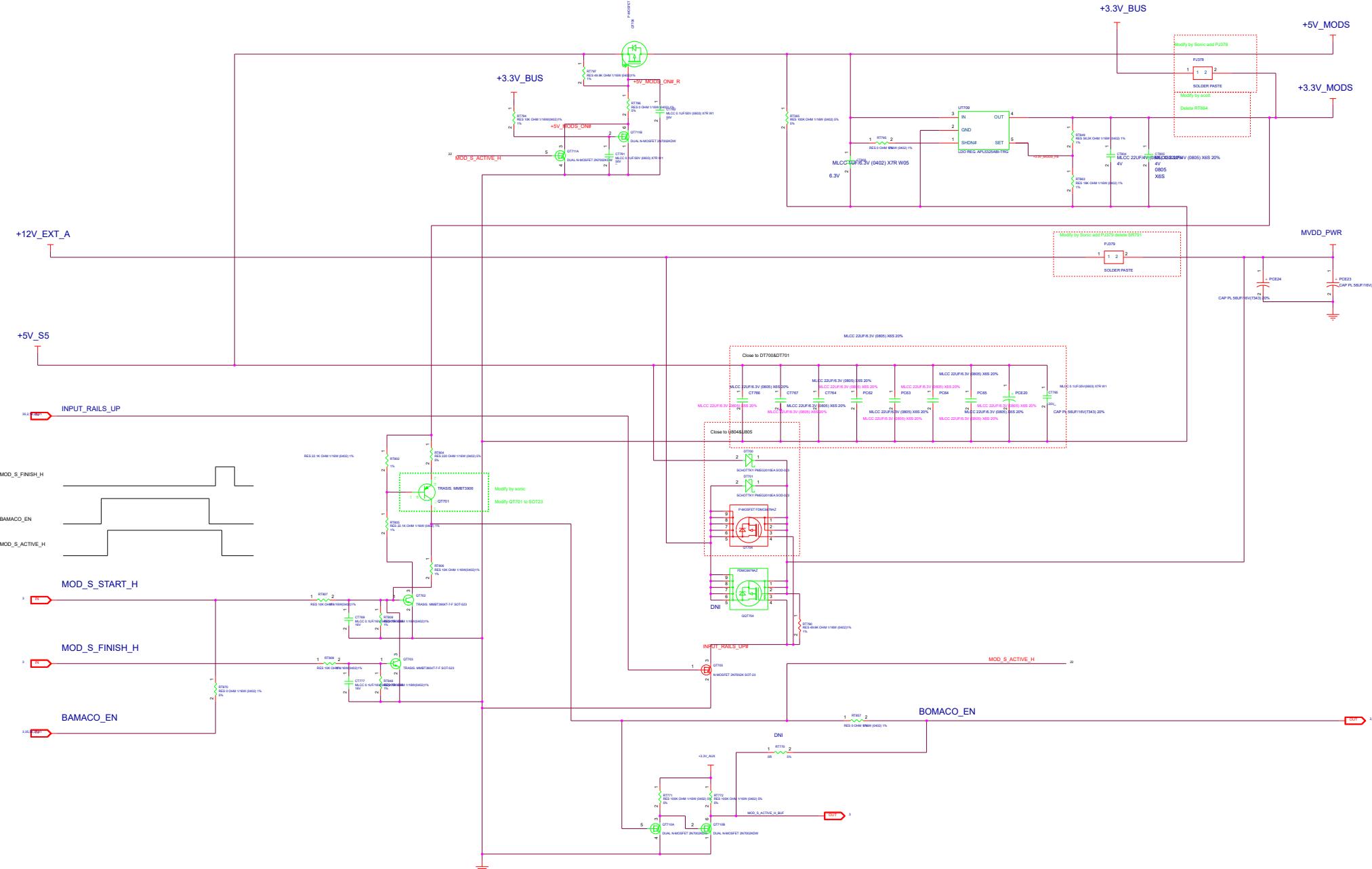


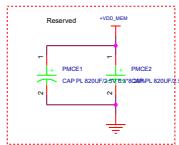


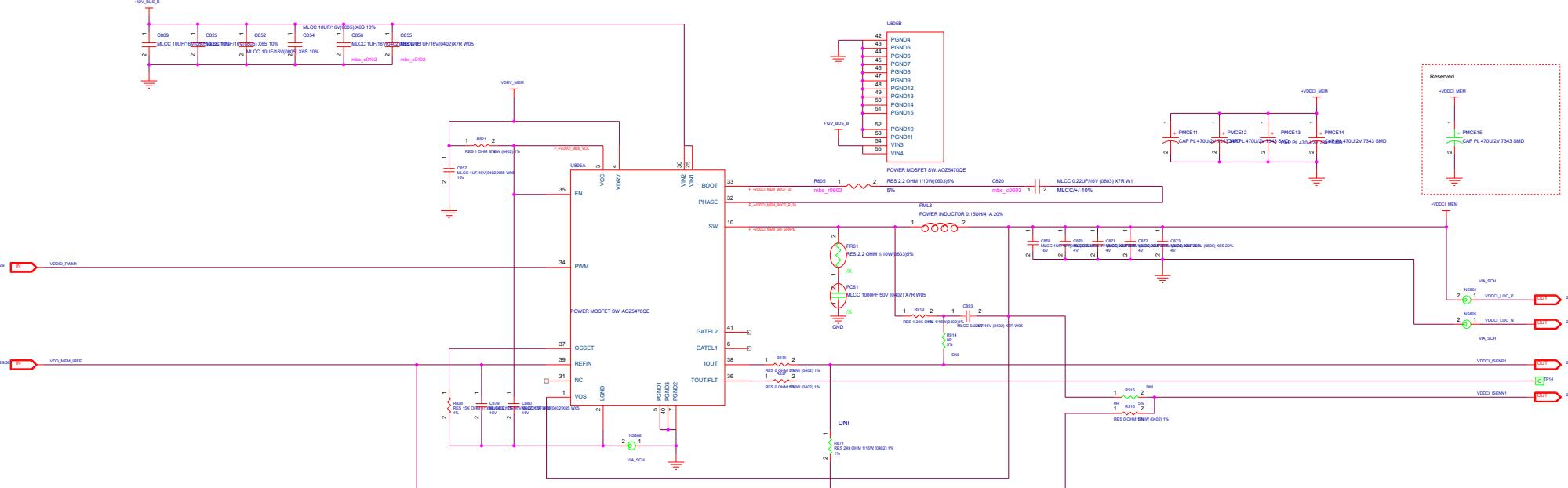


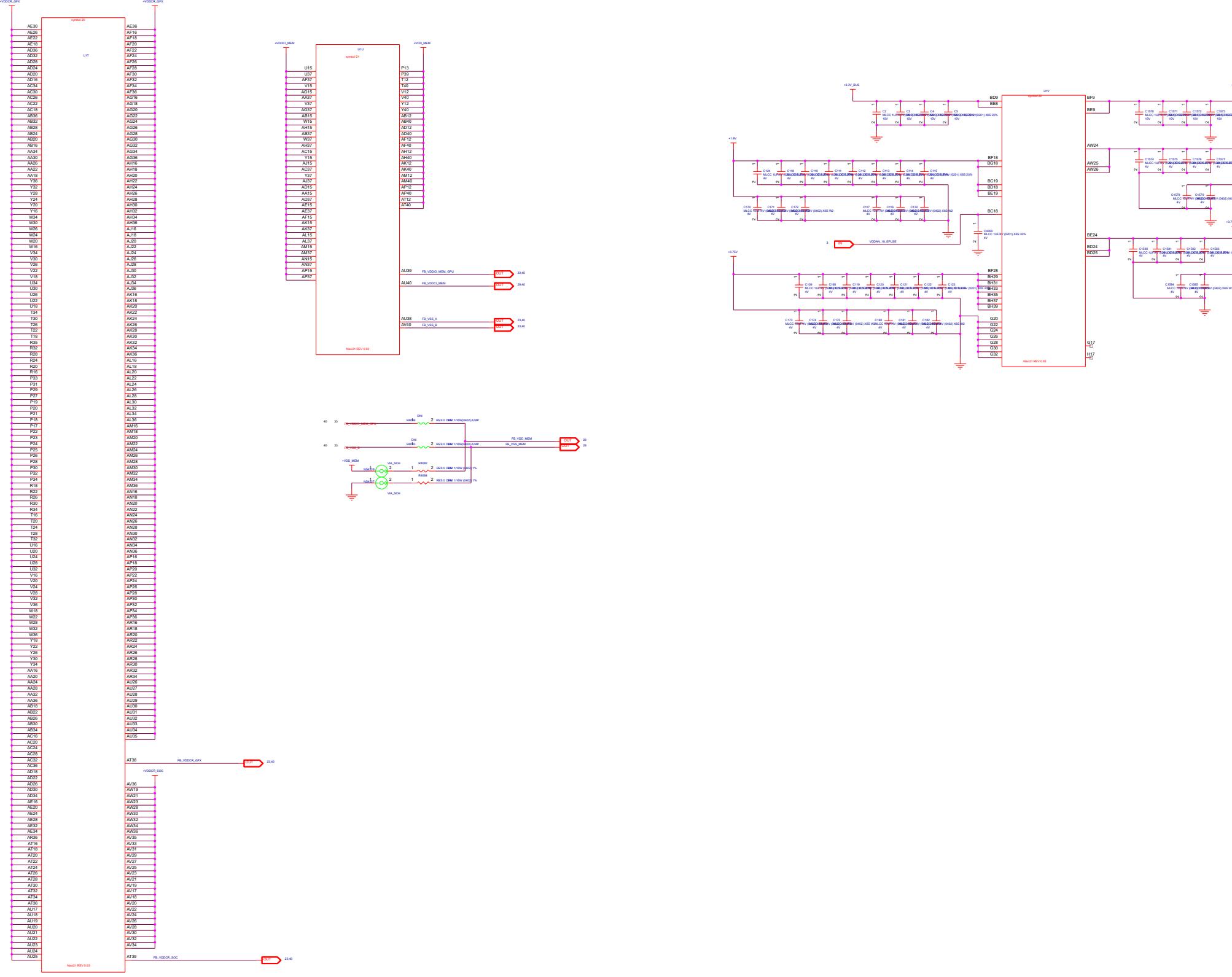


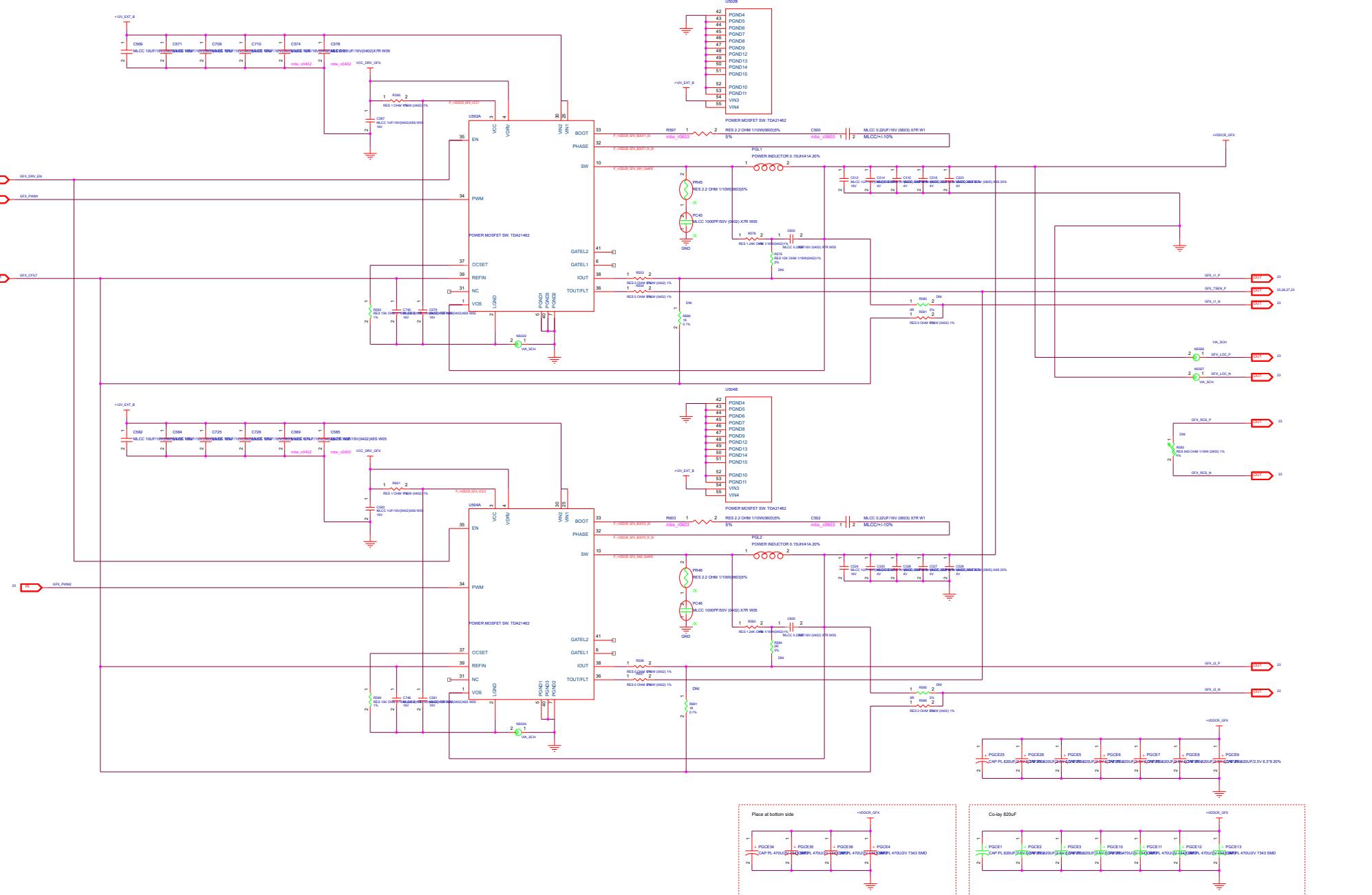


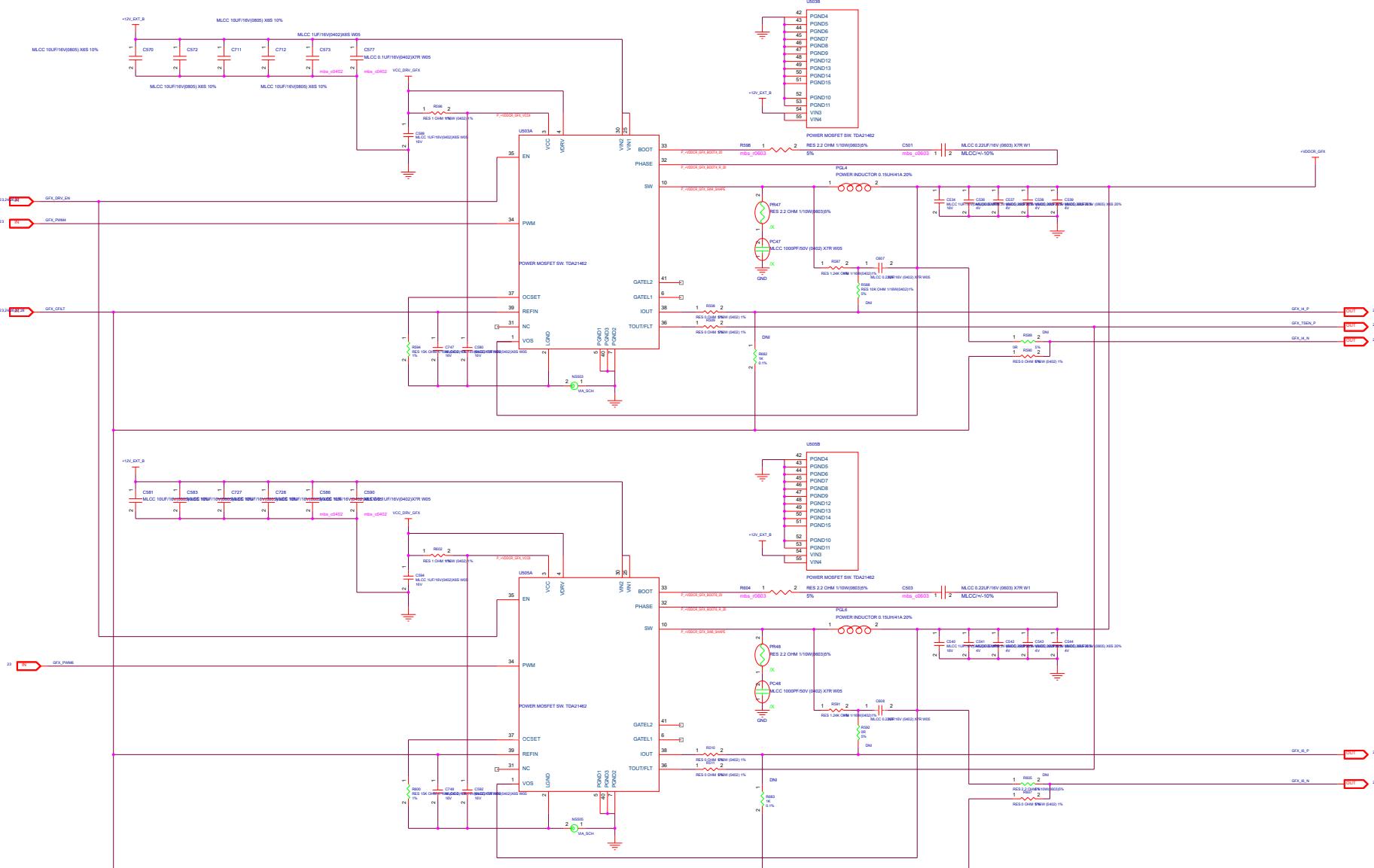


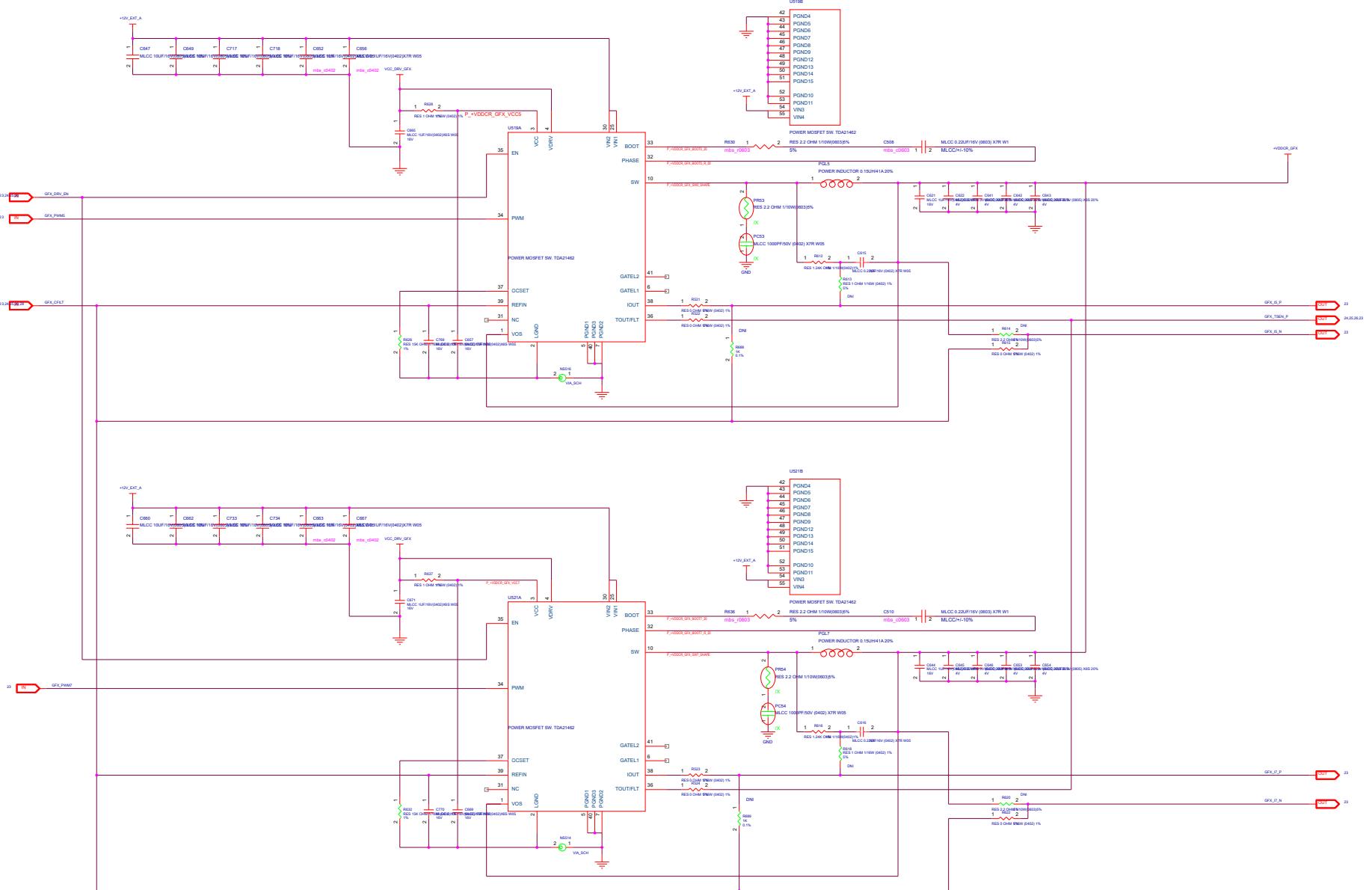


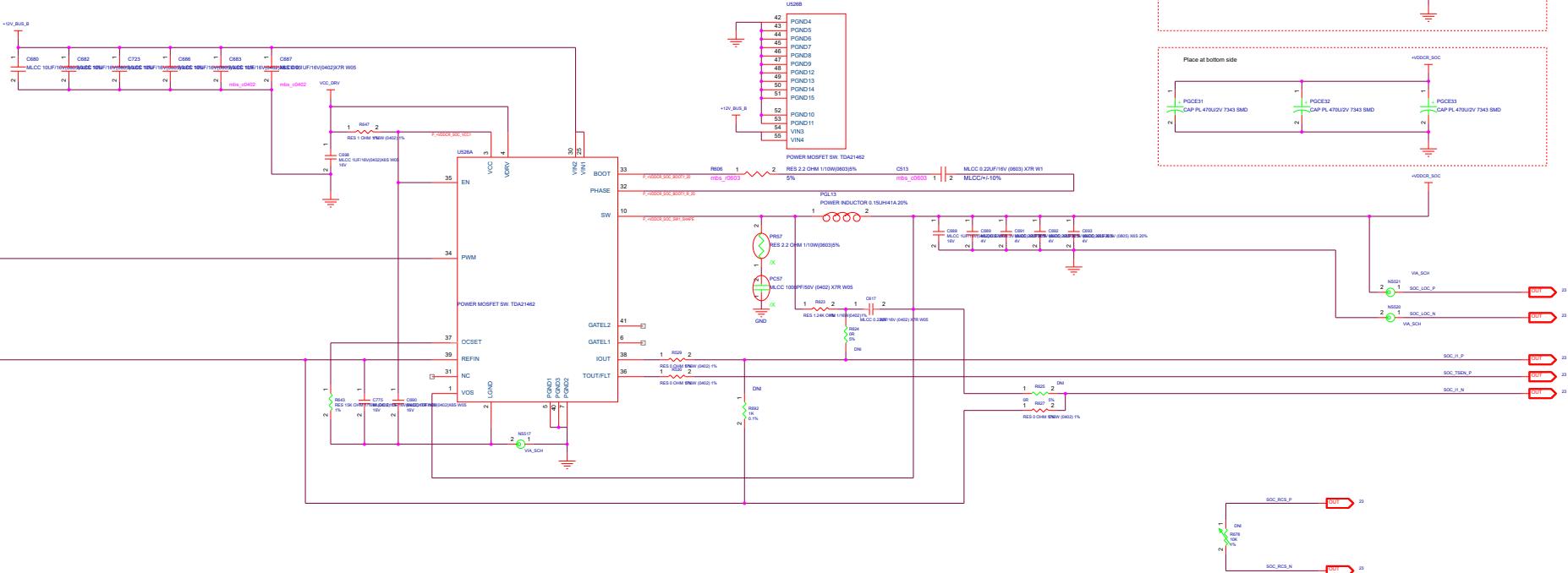




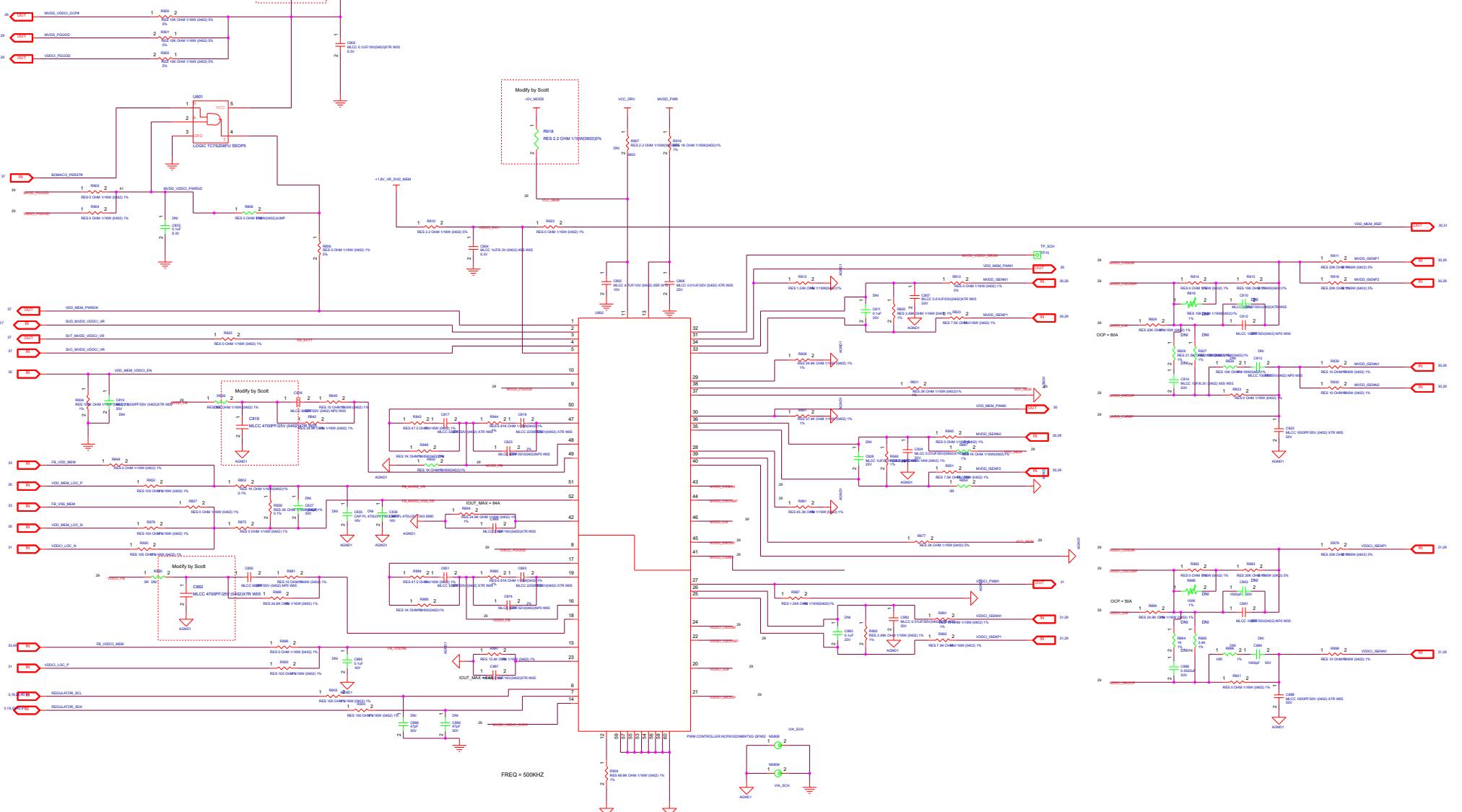


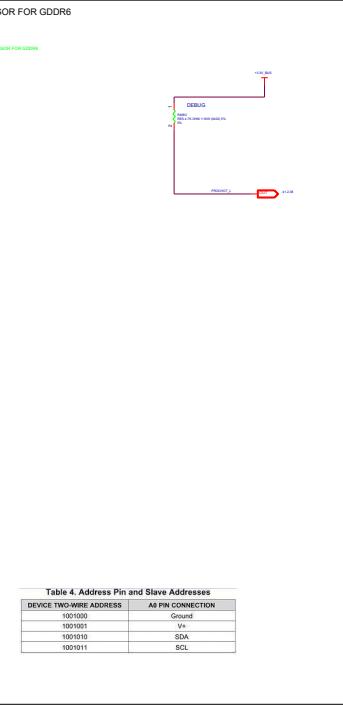
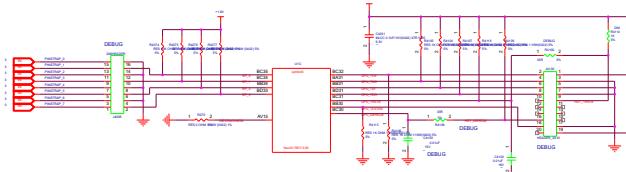
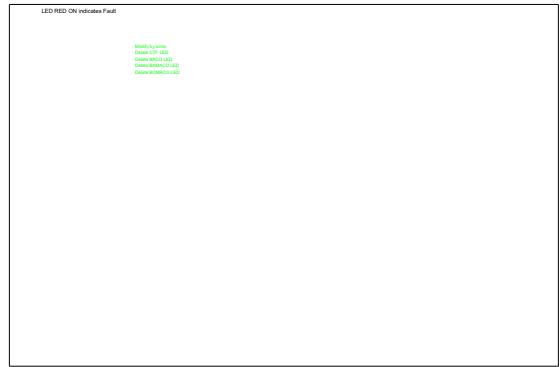






## (21) VDD\_MEM & VDDCI CONTROLLER

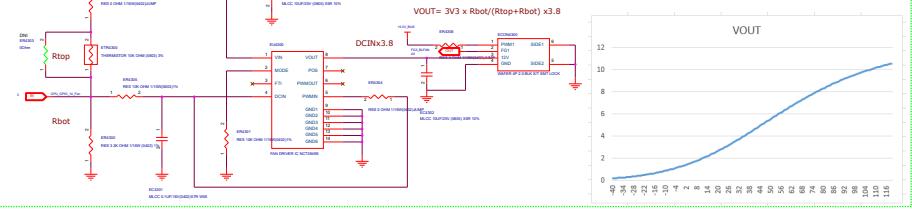
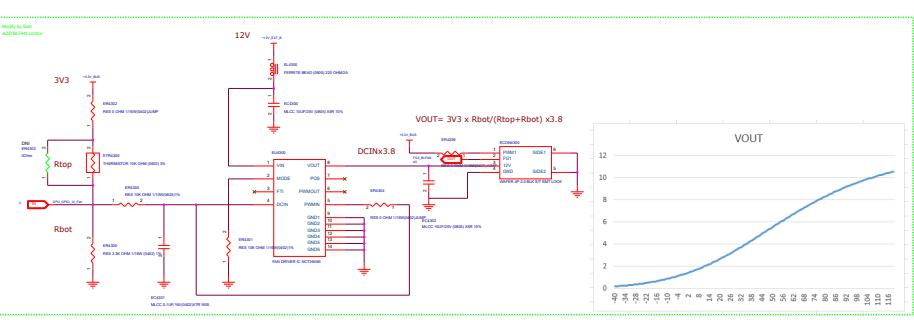
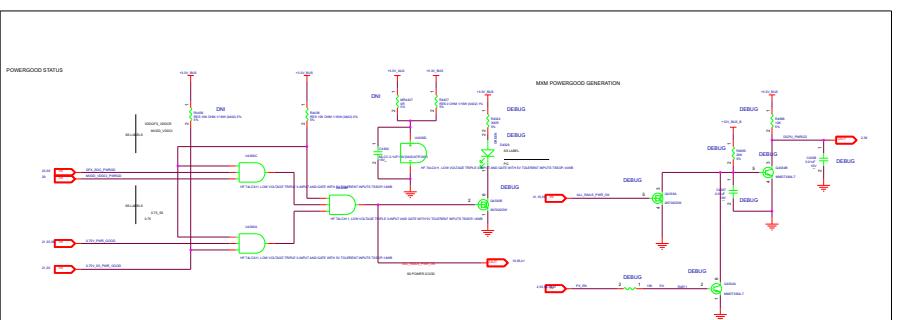




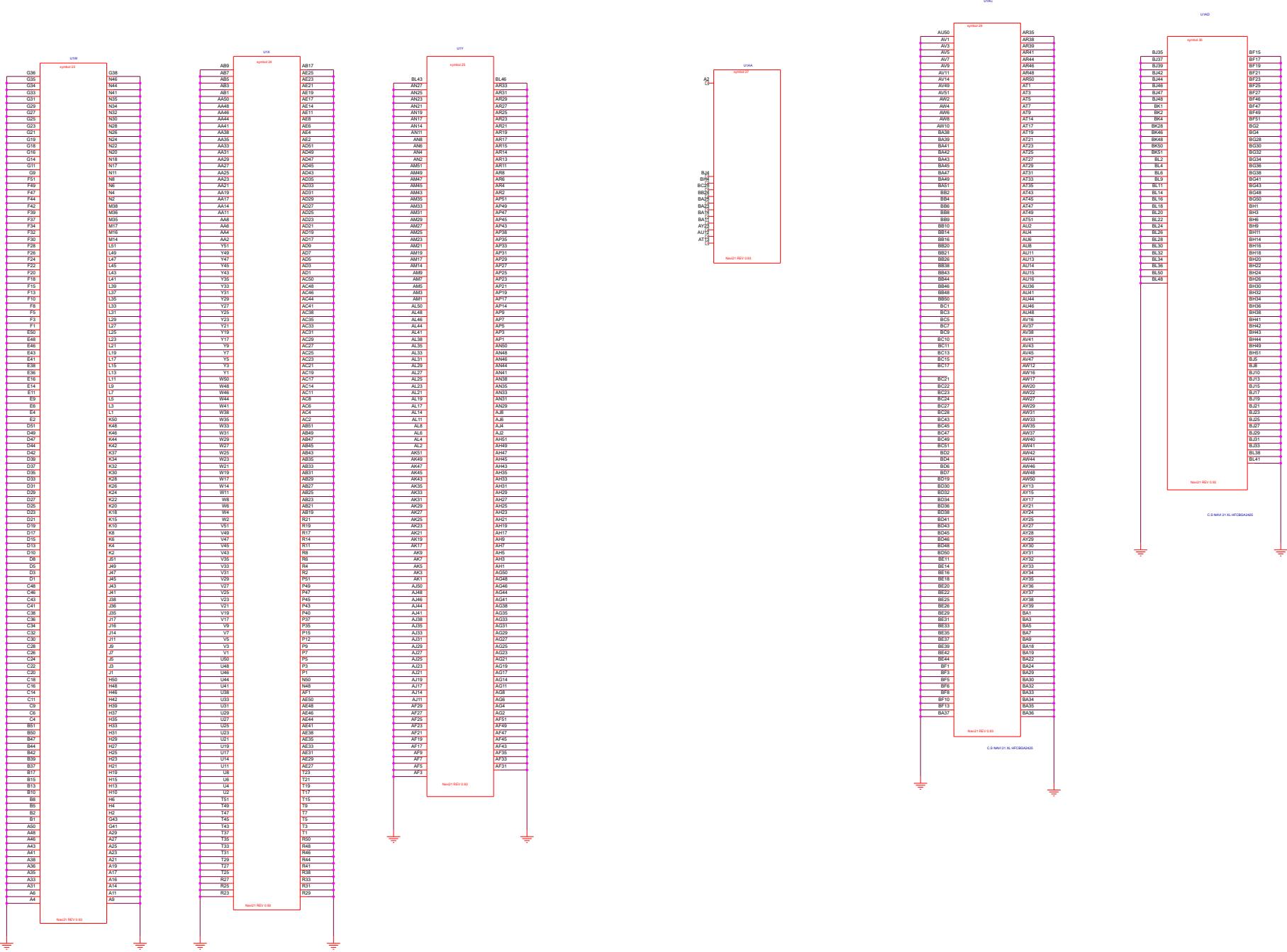
THERMAL SENSOR FOR VODMEM POWER STAGES

Ready by logic  
Done Thermal Sensor for VODMEM

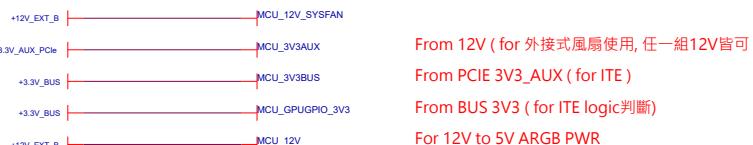
Ready by logic  
Done Thermal Sensor for GDDR6



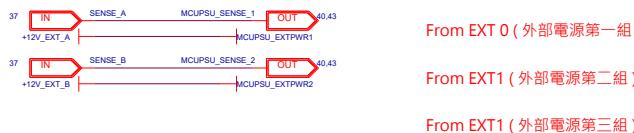
	A	02/10/2020	Initial schematic creation
1	-008	Apr 1 2020	Pg.22: Change UT109 to SOT22 package part 2400074401G for multi-sourcing
2	-008	Apr 1 2020	Pg.3640: Correct net name GPO_5_REG_HDT to GPO_5_REG_HDT
3	-008	Apr 1 2020	Pg.35: Change Q1103 to dual MOSFET part 2020008801G
4	-008	Apr 1 2020	Pg.29: Change R504 to 69.8K
5	-008	Apr 1 2020	Pg.20: DNI R1052, Invert R1503, Change R1501 to 49.8K
6	-008	Apr 1 2020	Pg.20: Invert a 150μF cap on C1589
7	-008	Apr 1 2020	Pg.20: Change R1523 to 1uF and Change R1560 to 49.8K
8	-008	Apr 1 2020	Pg.36: Add R1077 and R1078 (DNI) option
9	-008	Apr 1 2020	Pg.39: Add R4154 (DEBUG)
10	-008	Apr 1 2020	Pg.16: Add R78 (DNI)
11	-008	Apr 14 2020	Pg.3: Change R20 to 1k
12	-008	Apr 23 2020	Pg.23: Change R536, R538, R540, R542, R544, R546, R548, R551 to 10k, change R537, R539, R541, R543, R545, R547, R549, R552 to 2.49k
13	-008	Apr 23 2020	Pg.23: Change CS1 to 330pF and CS04 to 82pF
14	-008	Apr 23 2020	Pg.2: Change PCIe connector to Gen1 PN: 514NQPN038
15	-008	Apr 23 2020	Pg.23: Change GFX Load line R502, R517, R511 to 0uH and R519 to 2k
16	-008	Apr 23 2020	Pg.40: Invert D4010
17	-008	Apr 27 2020	Pg.28: Add C56
18	-008	Apr 27 2020	Pg.35: Change C7114 from 40540107090G to 42390107090G
19	-008	Apr 27 2020	Pg.23,23,37,38: Add circuits to use GENERICA, GENERICB, GENJLK, VSYNC to control fan power, GFX power, and LED
20	-008	Apr 27 2020	Pg.20: Add R1156
21	-008	Apr 28 2020	Pg.36,23,35: Add Clamp Workaround circuit for A0 bootloader hang bug
22	-008	Apr 29 2020	Pg.23: DNI R705
23	-008	Apr 29 2020	Pg.23: NAND VOAN_XGMI
24	-008	Apr 29 2020	Pg.41: Change U4300 to 25300/25100
25	-008	Apr 30 2020	Pg.5: Add MR123 option to GND_XGM_REPLACE
26	-008	May 1 2020	Pg.1: Add U4200_POWER_3.3V_AUX option
27	-008	May 1 2020	Pg.10/11/12/13: Change memory chips to Samsung 16gbps PN: Z3H416GTUJ16
28	-008	May 4 2020	Pg.25: Change R7120 to 39.2k
29	-008	May 4 2020	Pg.25: DNI R7177
30	-008	May 4 2020	Pg.28: Add R584, NR584, NR584 for SOC power option
31	-008	May 4 2020	Pg.2: DNI R4212, R4211, C421, C421 for PCIe TX filter
32	-008	May 4 2020	Pg.3: Change OC_R20, R51 to 5.1K, Inverting D412
33	-008	May 5 2020	Pg.20: Add IN4381 Reset pin delay options
34	-008	May 5 2020	Pg.21: Add 12V_BLD power option for 3V_12V_MUX input
35	-008	May 5 2020	Pg.33: Add C170, C171, C172 on +1.8V and C173, C174, C175 on +0.75V
36	-008	May 5 2020	Pg.32: DNI C1584
37	-008	May 6 2020	Pg.19: Change R1537 to 100R
38	-008	May 6 2020	Pg.2: Change PCIe Tx AC coupling caps to X5S type
39	-008	May 6 2020	Pg.3: Change C61 to X5S type
40	-008	May 12 2020	Pg.3: Change M00_5_ACTIVE_H to M00_5_ACTIVE_H_BUF
41	-008	May 12 2020	Pg.35: Change TPS52020 to TPS52021
42	-008	May 26 2020	Pg.20: Change C1589 to 1uF



## Power



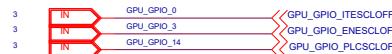
## PSU DETECT INPUT

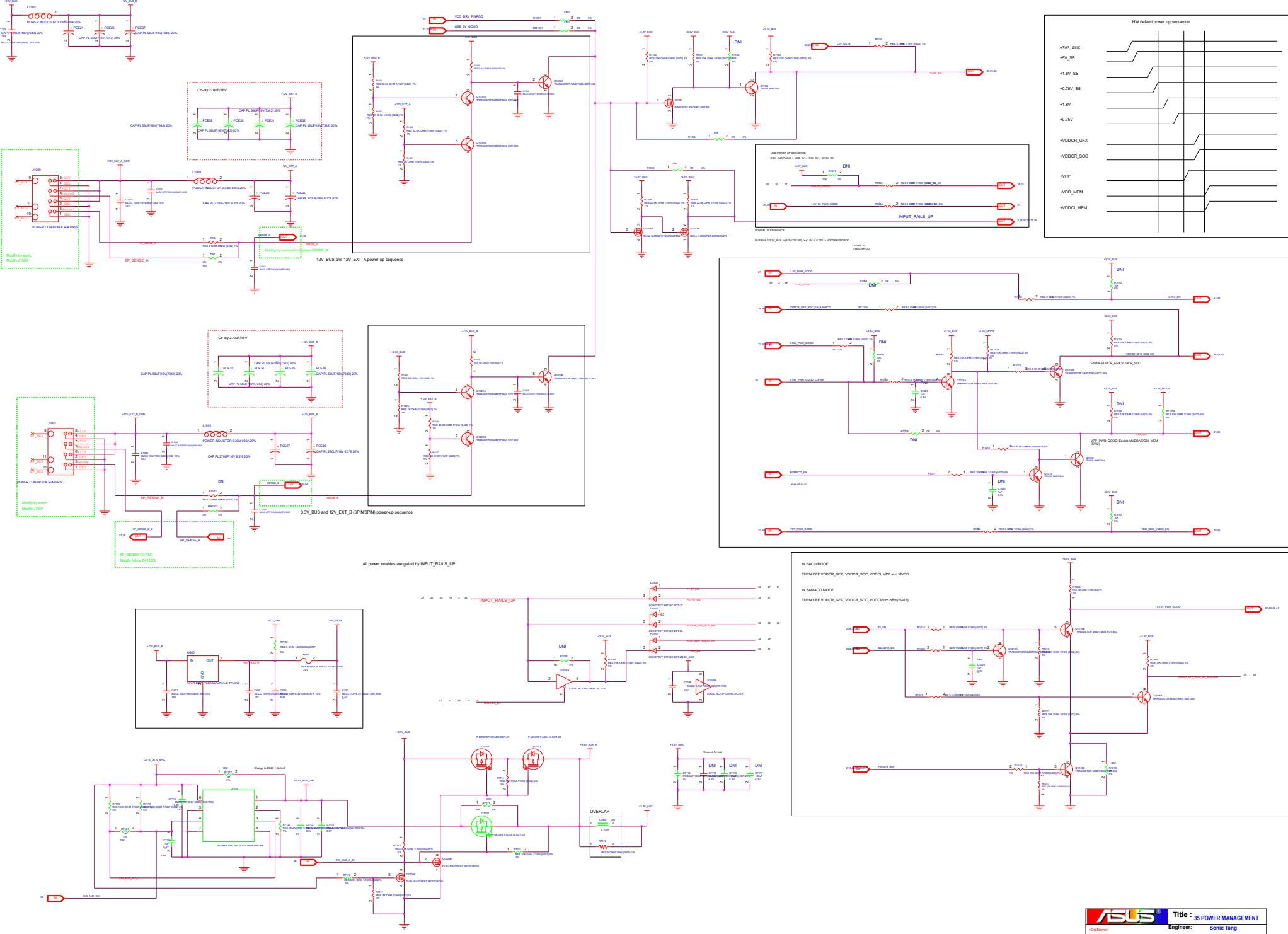


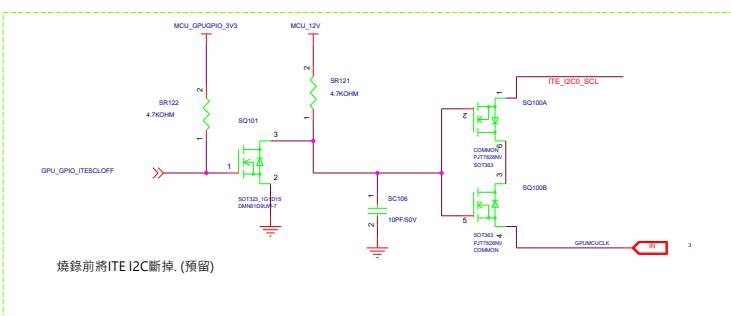
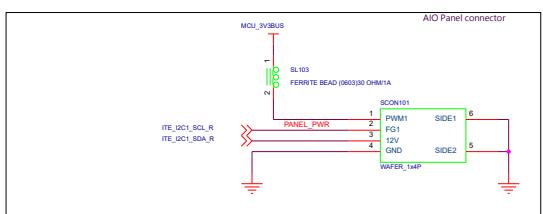
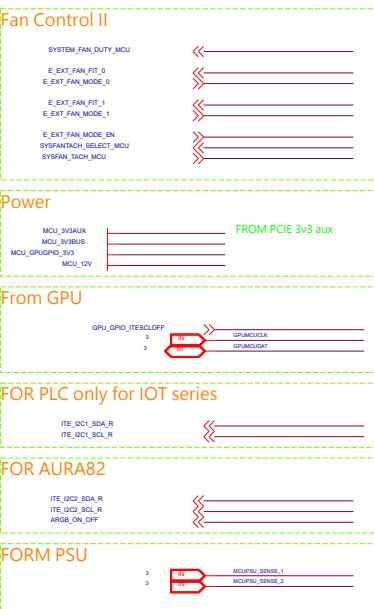
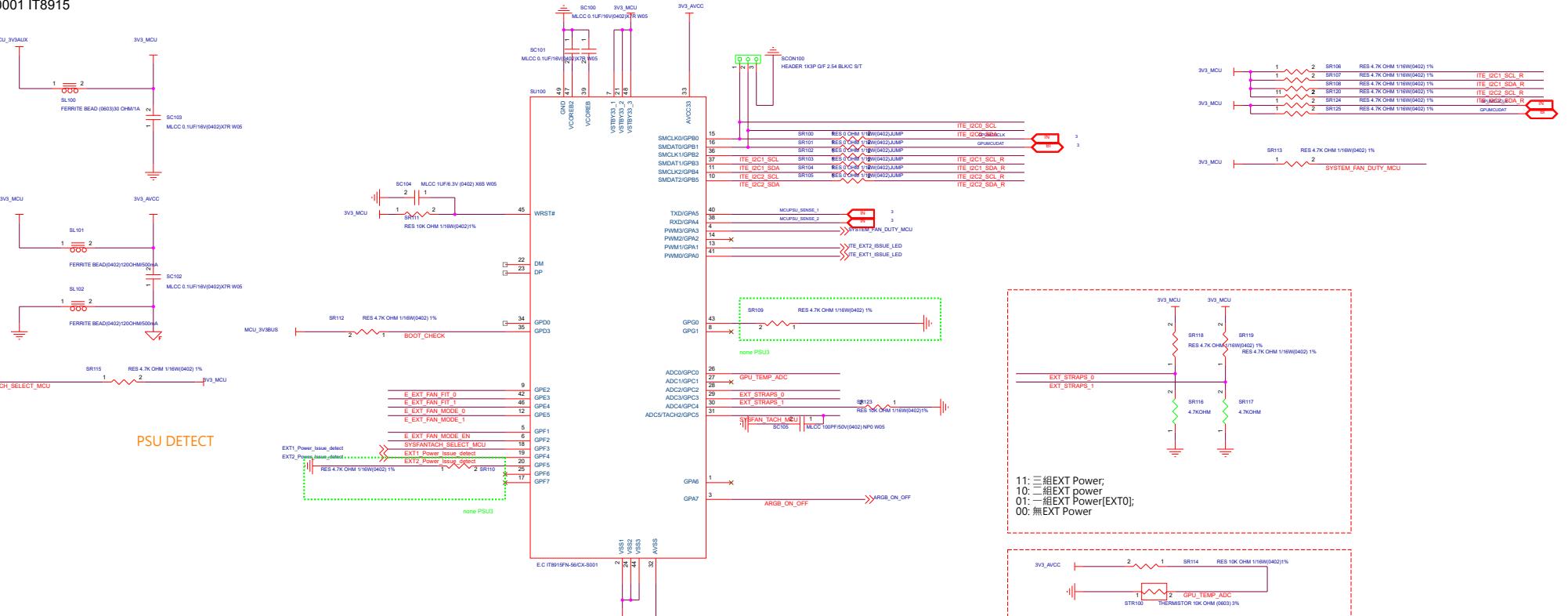
## I2C

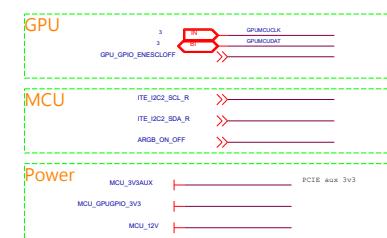
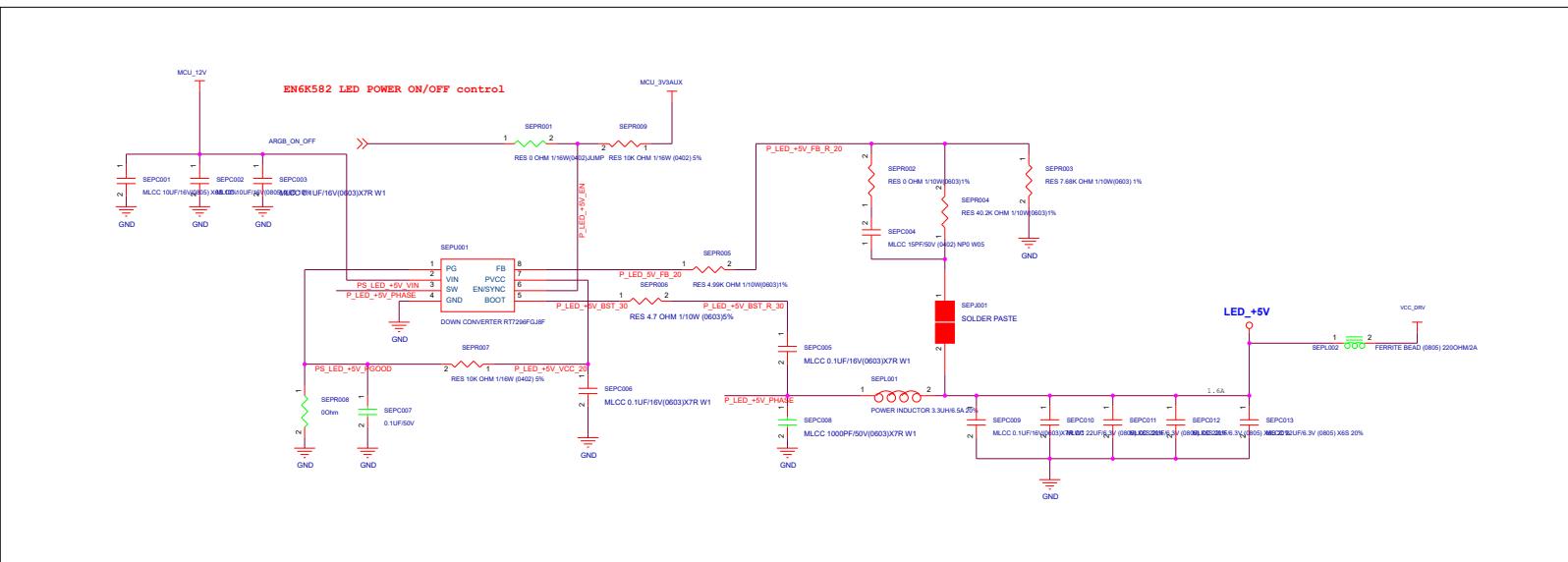
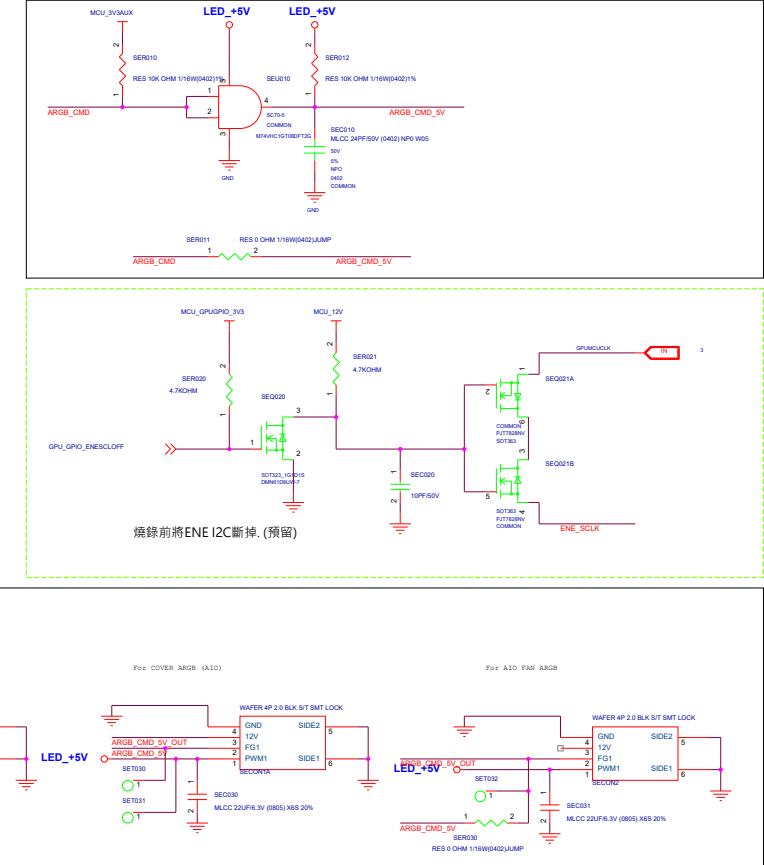
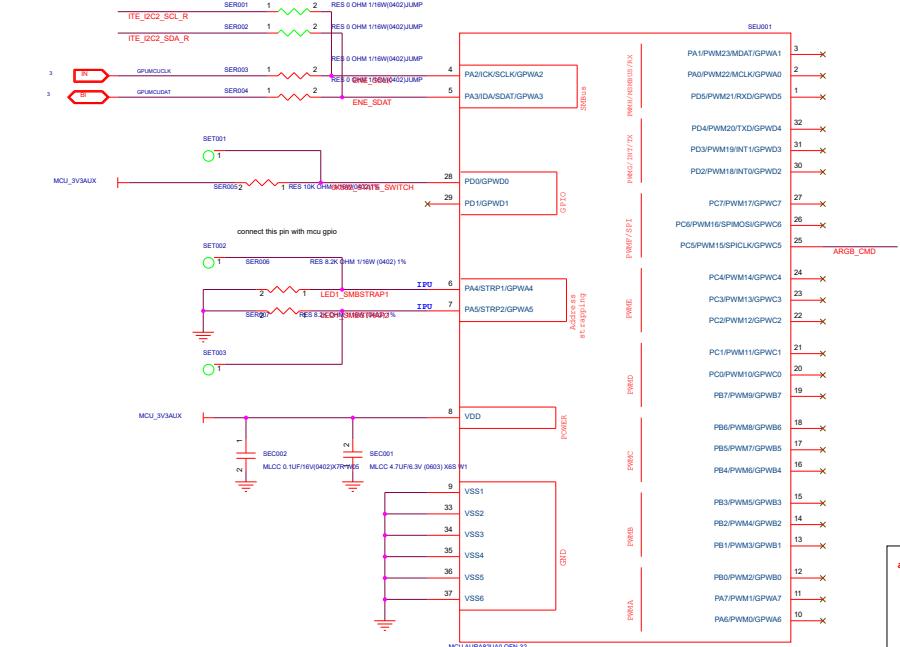


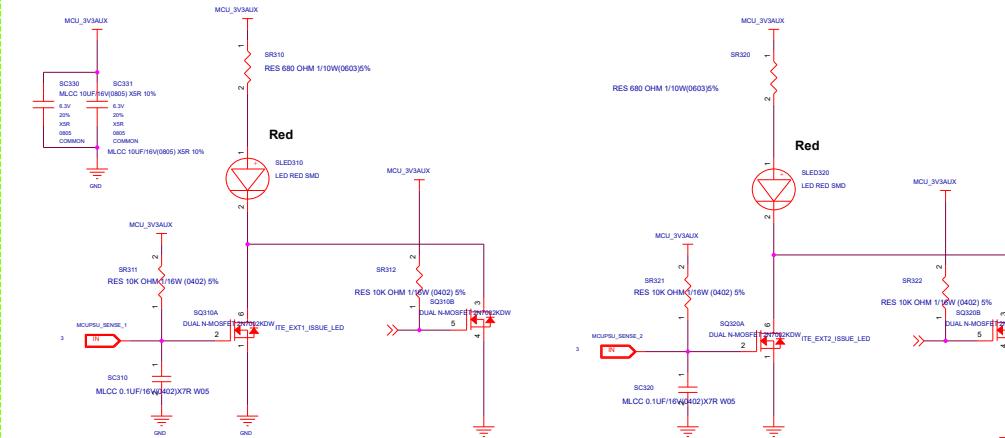
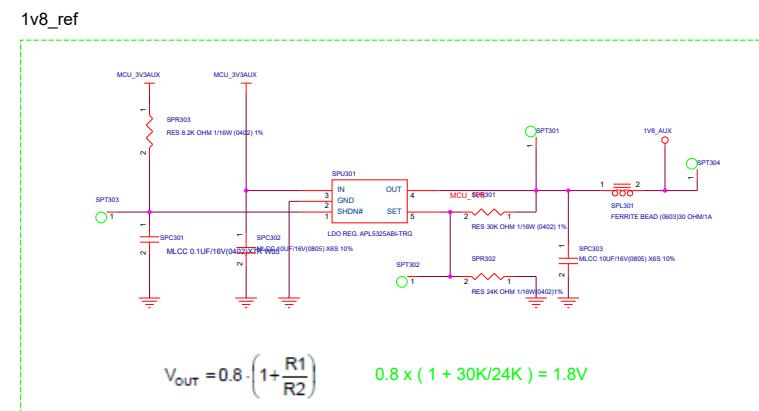
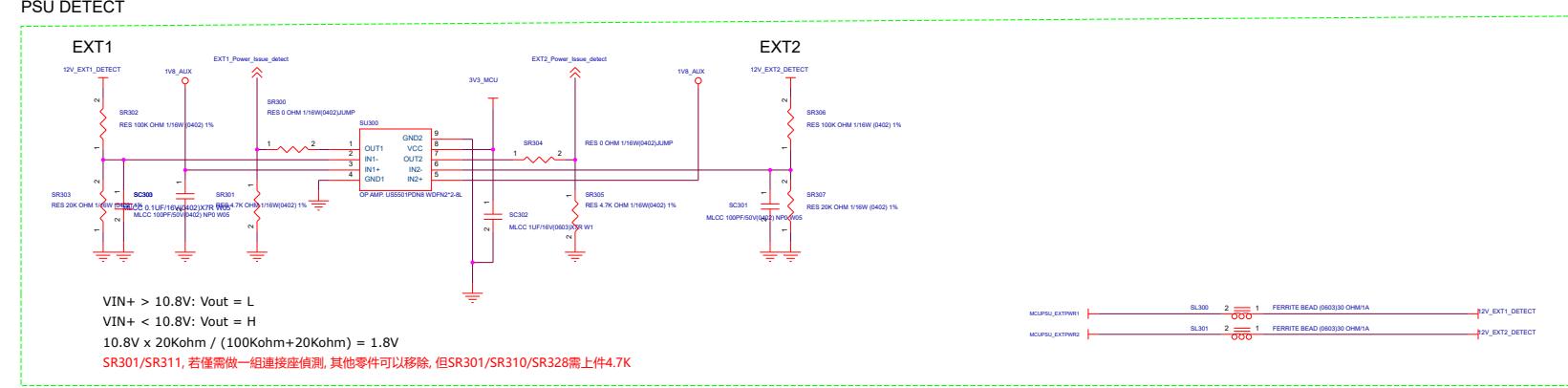
## GPU\_GPIO



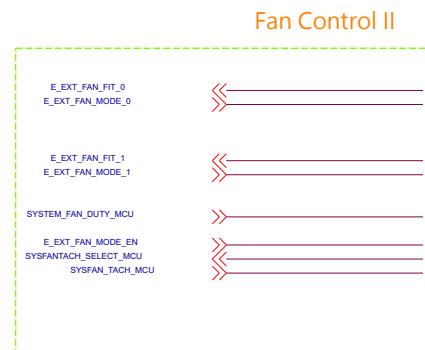
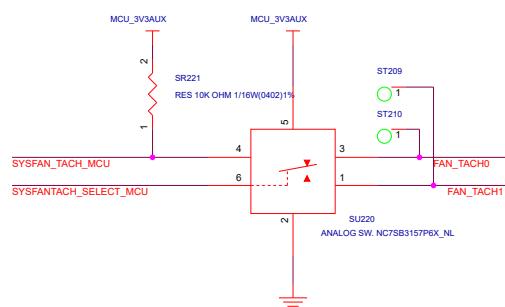
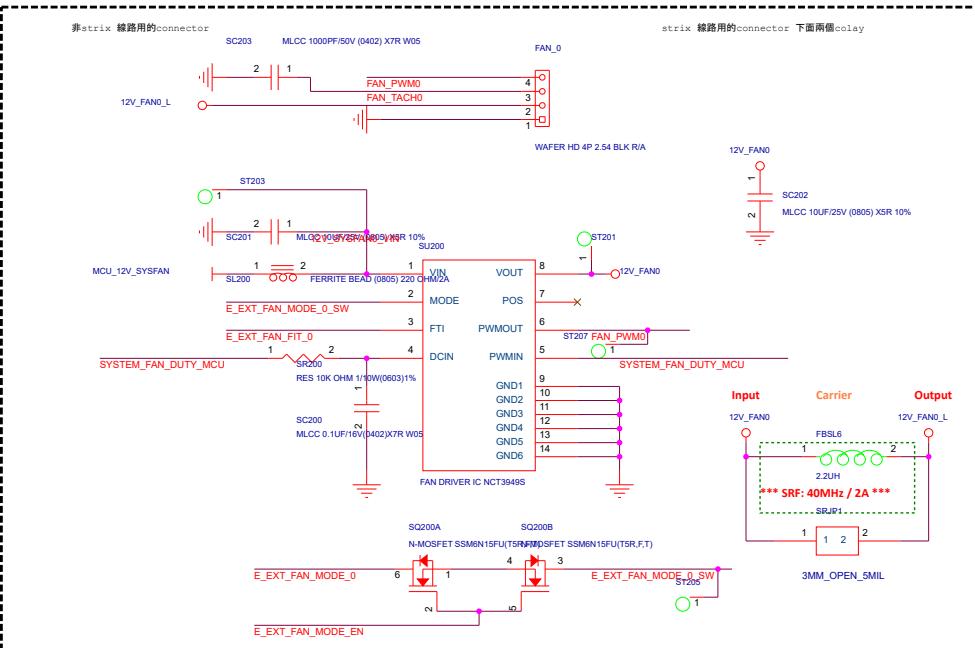








- 1.EXT power is not connected, the led is always on
- 2.EXT power is connected  
EXT 12V is over 10.8V, the led turns on  
EXT 12v is below 10.8v the led blink



# ASUS VGA PCB Logo

LOGO1  
CE  
CE



LOGO8  
UKRAINE  
UKRAINE



LOGO2  
VCCI  
VCCI



LOGO9  
PCB MADE IN CHINA  
PCB\_MADE\_IN\_CHINA

PCB MADE IN CHINA

LOGO3  
EMI\_D33005\_H  
EMI\_D33005\_H



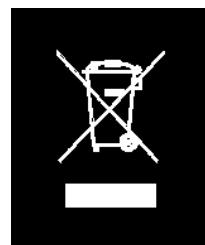
LOGO10  
MARK\_L  
S\_MARK\_L



LOGO4  
FCC  
FCC



LOGO11  
WEEE\_LOGO  
WEEE\_LOGO

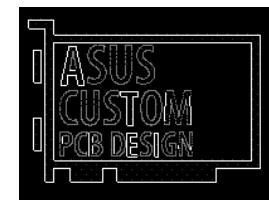


ASUS Re-design logo  
Do not place this on reference board

LOGO5  
RCM  
RCM



LOGO13  
ASUS CUSTOM  
PCB DESIGN  
ASUS\_CUSTOM\_PCB



LOGO6  
CAN ICES-3 (B) / NMB-3 (B)  
CAN\_ICES\_3B\_NMB\_3B

CAN ICES-3 (B) / NMB-3 (B)

LOGO12  
SFIS  
SFIS



LOGO7  
KC R-R-NSQ-XXXXXXXXXXXXXX  
KC\_R\_R\_LOGO



M1  
FCC\_ruler\_ASUS  
PCB\_RULER\_ASUS

Title : XX ASUS PCB Logo	
<OrgName>	Engineer: Sonic Tang
Size	Project Name
A3	D414S
Rev	1.01X
Date: Wednesday, August 26, 2020	
Sheet	50
of	50



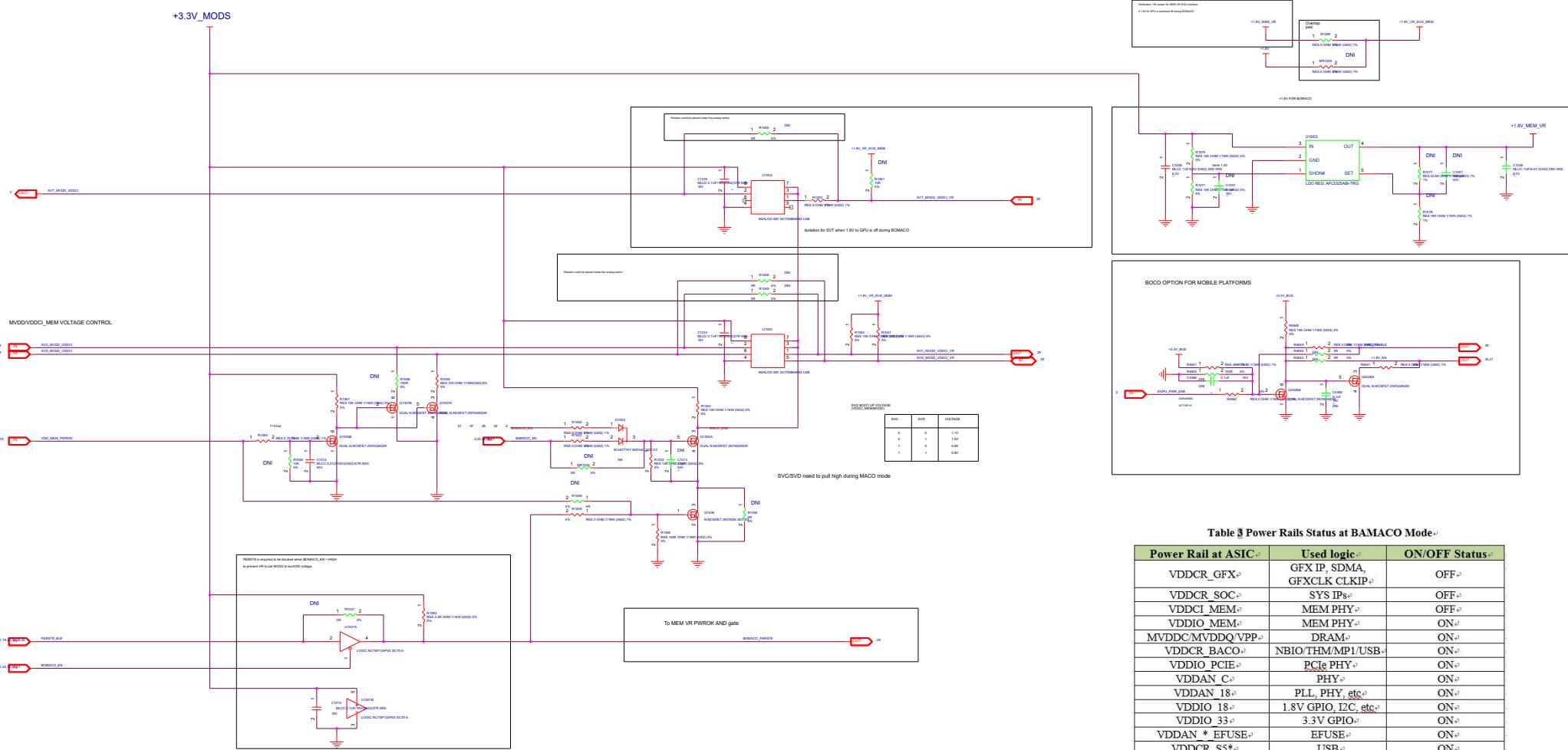


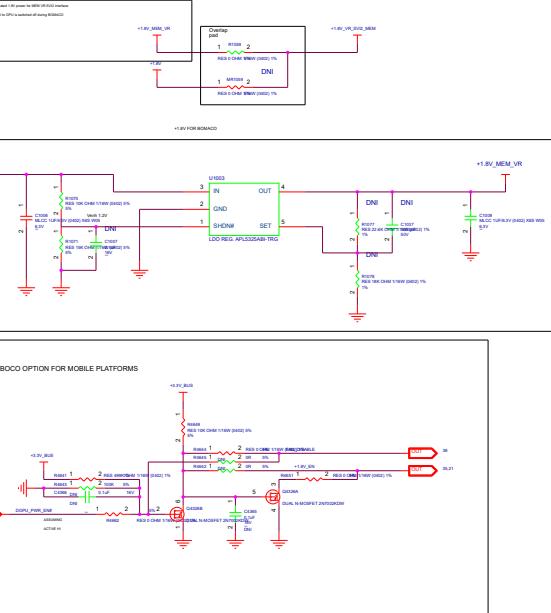
Table 3 Power Rails Status at BAMACO Mode<sup>1,2,3</sup>

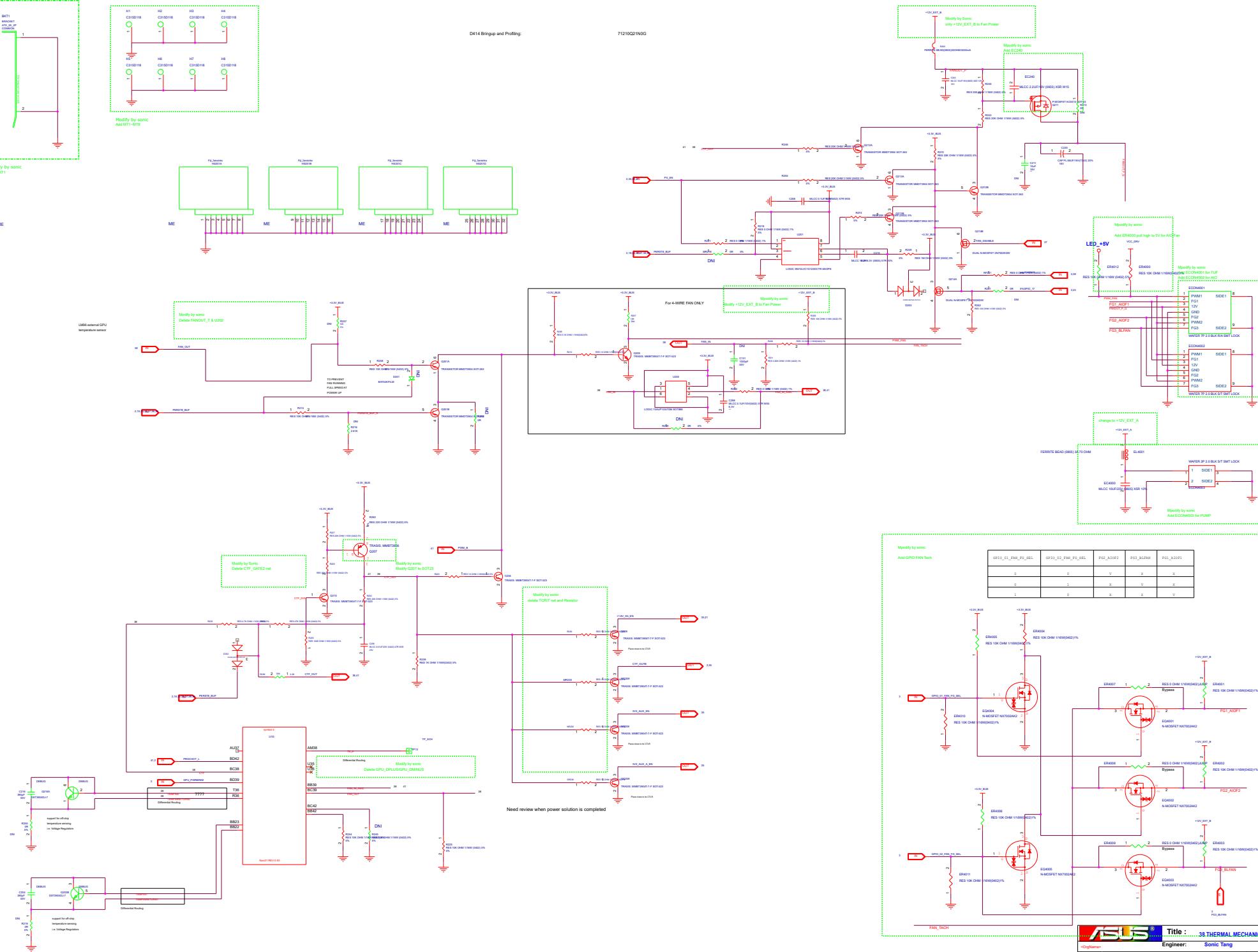
Signals <sup>1</sup>	Default <sup>2</sup>	BOCO <sup>3</sup>	BAMACO <sup>3</sup>
PX_EN <sup>1</sup>	LOW <sup>2</sup>	N/A <sup>3</sup>	N/A <sup>3</sup>
MACO_EN <sup>1</sup>	N/A <sup>2</sup>	N/A <sup>3</sup>	N/A <sup>3</sup>
PERSTb <sup>1</sup>	HIGH <sup>2</sup>	1>0>1 <sup>4</sup>	1>0>1 <sup>4</sup>
PWR_EN <sup>1</sup>	HIGH <sup>2</sup>	LOW <sup>3</sup>	LOW <sup>3</sup>
BOMACO_EN <sup>1</sup>	LOW <sup>2</sup>	LOW <sup>3</sup>	HIGH <sup>3</sup>

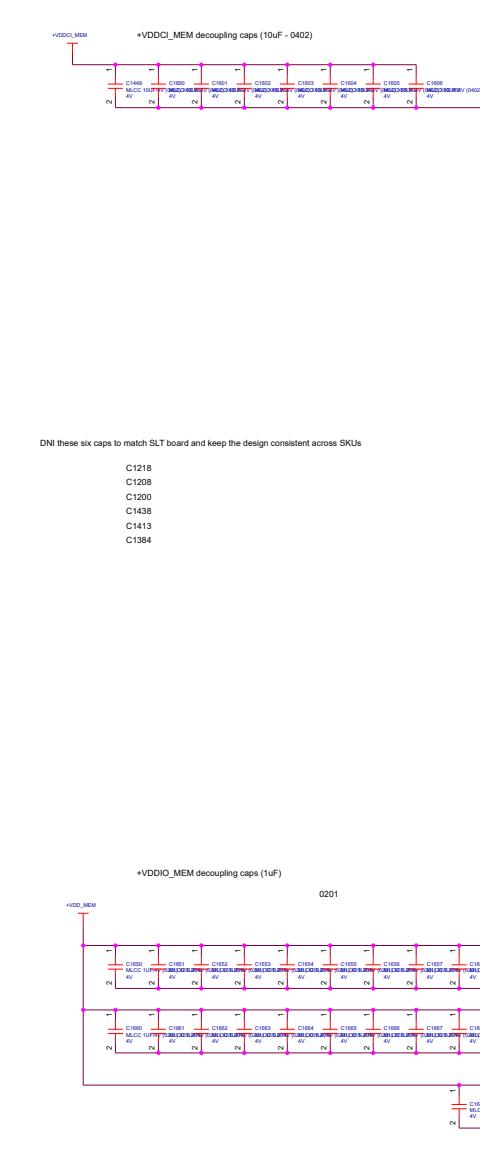
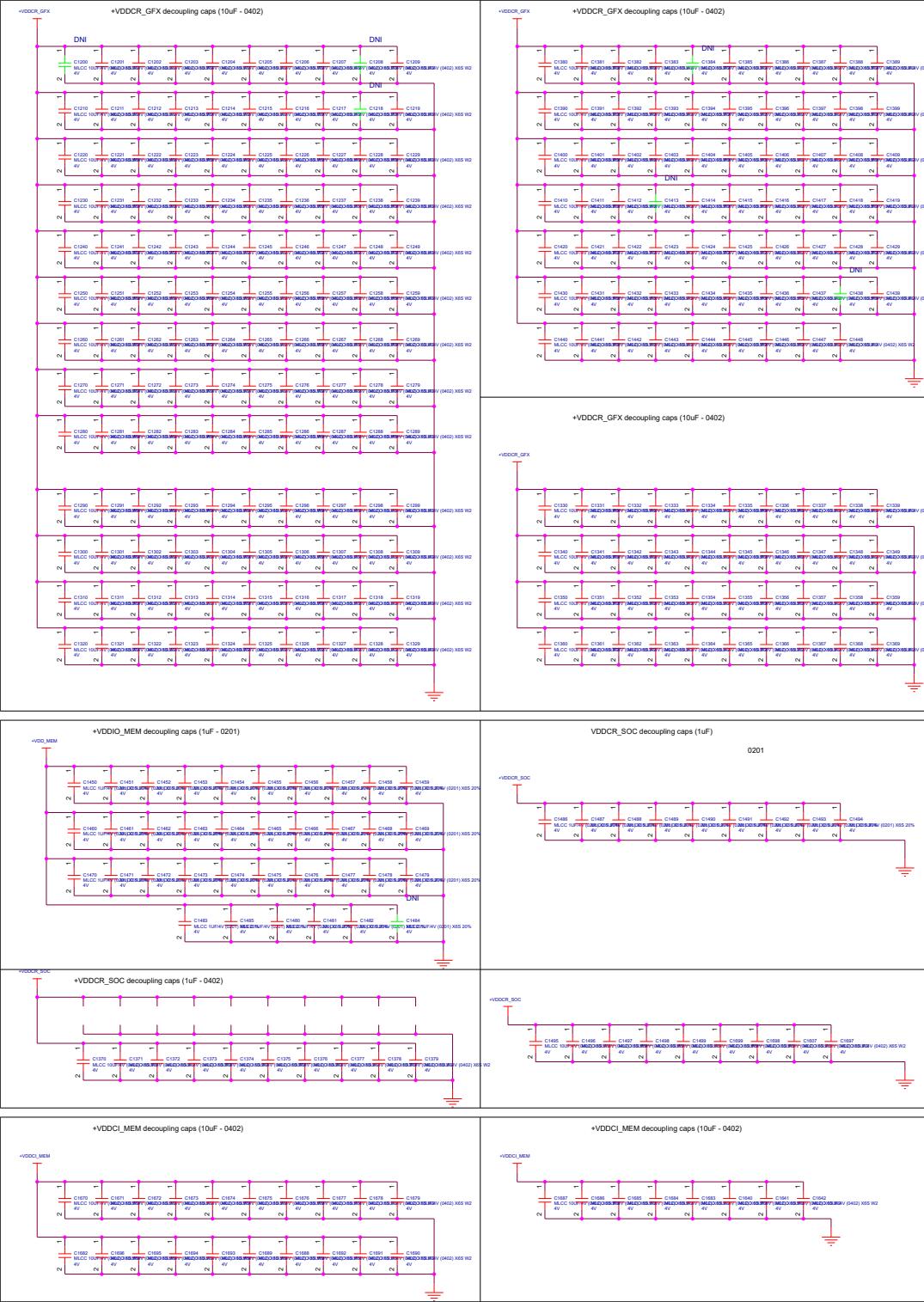
Table 4 Key Signals at Different PM Modes<sup>1,2,3</sup>

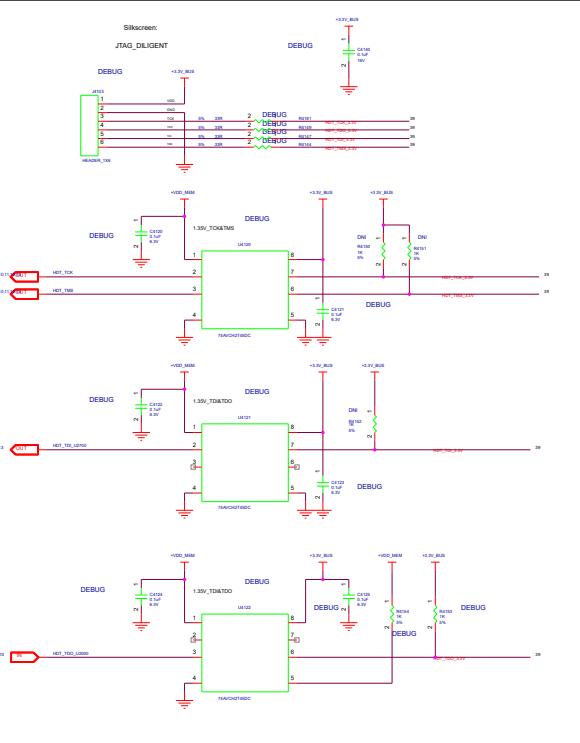
BOMACO_EN	SVC_PU/PD	SVD_PU/PD
HIGH <sup>1</sup>	PU <sup>2</sup>	PU <sup>2</sup>
LOW <sup>1</sup>	bootVID <sup>2</sup>	bootVID <sup>2</sup>

Table 5 Platform to Support BOMACO<sup>1,2,3</sup>









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