8Gb GDDR5 SGRAM B-die

16M x 32Bit x 16 Banks Graphic Double Data Rate 5 Synchronous DRAM (170Ball FBGA)

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	- First SPEC Release	Mar. 2015	-	J.Y.Lee

Table Of Contents

8Gb GDDR5 SGRAM B-die

1. FEATURES

- 1.5V ± 0.045V power supply for device operations(VDD)
  (Specific parts support 1.35V ± 0.0405V)
- 1.5V ± 0.045V power supply for I/O interface(VDDQ)
  (Specific parts support 1.35V ± 0.0405V)
- Maximum CK/$\overline{CK}$ up to 2GHz
- Maximum WCK/$\overline{WCK}$ up to 4GHz
- Maximum data rate up to 8.0Gbps/pin
- Halogen free 170 Ball FBGA(RoHS Compliant)
- Single ended interface for data, address and command
- Quarter data-rate differential clock inputs CK/$\overline{CK}$ for ADD/CMD
- Two half data-rate differential clock inputs WCK/$\overline{WCK}$,
  each associated with two data bytes(DQ, $\overline{DBI}$, EDC)
- Double Data Rate (DDR) data (WCK)
- Single data rate (SDR) command (CK)
- Double data rate (DDR) addressing (CK)
- 16 internal banks for concurrent operation
- 4 bank groups for tCCDL 3 tCK and 4 tCK
- 8n prefetch architecture: 256bit per array read or write access
- Burst length: 8 only
- Programmable CAS latency:
  9,10,11,12,13,14,15,16,17,18,19,20(tCK),.....,27(tCK)
- Programmable write latency : 1, 2, 3, 4, 5, 6 and 7(tCK)
- WRITE Data mask function via address bus
  (single/double byte mask)
- Data bus inversion(DBI) and address bus inversion(ABI)
- Input/output PLL on/off mode
- Address training: Address input monitoring by DQ pins
- WCK2CK clock training with phase information by EDC pins
- Data read and write training via READ FIFO
- READ FIFO pattern preload by LDFF command
- Direct write data load to READ FIFO by WRTR command
- Consecutive read of READ FIFO by RDTR command
- Read/Write data transmission integrity secured by cyclic
  redundancy check ; CRC-8(X^8+X^2+X+1) for EDC
- Read/write EDC on/off mode
- Programmable EDC hold pattern for CDR
- Programmable CRC read latency(CRCRL) range 0 to 3 tCK
- Programmable CRC write latency(CRCWL) range 7 to 14 tCK
- Low Power modes
- RDQS mode on EDC pin
- Auto & self refresh modes
- Auto precharge option for each burst access
- 32ms, auto refresh (16K cycles)
- On-die termination (ODT)
  ; Nominal values of 60ohm and 120ohm
- Pseudo open drain(POD-15) compatible inputs and outputs
  ; 40ohm pull down, 60ohm pull up
- ODT and output driver strength auto-calibration with external
  resistor ZQ pin(120ohm)
- Programmable termination and driver strength offsets
- Output driver strength adjustment by MRS
- Selectable external or internal VREF for data inputs
  ;Programmable offsets for internal VREF
- Separate external VREF for address / command inputsdmd
- Vendor ID, FIFO depth and Density info fields for identification
- X32/X16 mode configuration set at power-up with EDC pin
- 16bits support for vendor ID/Density/FIFO depth MRS
- Mirror function with MF pin
- Boundary scan function with SEN pin

2. ORDERING INFORMATION

Part Number	Max Freq.	Max Data Rate	VDD & VDDQ	Interface	Package
K4G80325FB-HC25	2000MHz	8.0 Gbps/pin	1.5V ± 0.045V	POD_15	170 Ball FBGA
	TBD	TBD	1.35V ± 0.0405V	POD_135	
K4G80325FB-HC28	1750MHz	7.0 Gbps/pin	1.5V ± 0.045V	POD_15	
	1500MHz	6.0 Gbps/pin	1.35V ± 0.0405V	POD_135	
K4G80325FB-HC03	1500MHz	6.0 Gbps/pin	1.5V ± 0.045V	POD_15	
	1250MHz	5.0 Gbps/pin	1.35V ± 0.0405V	POD_135	

3. GENERAL DESCRIPTION

FOR 16M x 32Bit x 16 Bank GDDR5 SGRAM
The K4G80325FB is 8,589,934,592 bits of hyper synchronous data rate Dynamic RAM organized as 16 x 8,388,608 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Data training feature with free-running write clocks allows extremely high performance up to 32GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

The GDDR5 SGRAM uses a 8n prefetch architecture and DDR interface to achieve high-speed operation. The device can be configured to operate in x32 mode or x16 (clamshell) mode. The mode is detected during device initialization. The GDDR5 interface transfers two 32 bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 8n-prefetch a single write or read access consists of a 256 bit wide, two CK clock cycle data transfer at the internal memory core and eight corresponding 32 bit wide one-half WCK clock cycle data transfers at the I/O pins.
The GDDR5 SGRAM operates from a differential clock CK and $\overline{CK}$. Commands are registered at every rising edge of CK. Addresses are registered at every rising edge of CK and every rising edge of $\overline{CK}$.

GDDR5 replaces the pulsed strobes (WDQS & RDQS) used in previous DRAMs such as GDDR4 with a free running differential forwarded clock (WCK/$\overline{WCK}$) with both input and output data registered and driven respectively at both edges of the forwarded WCK.

Read and write accesses to the GDDR5 SGRAM are burst oriented; an access starts at a selected location and consists of a total of eight data words. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command and the next rising $\overline{CK}$ edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next rising $\overline{CK}$ edge are used to select the bank and the starting column location for the burst access.

4. DEFINITION OF SIGNAL STATE TERMINOLOGY

GDDR5 SGRAM will be operated in both ODT Enable (terminated) and ODT Disable (unterminated) modes. For highest data rates it is recommended to operate in the ODT Enable mode. ODT Disable mode is designed to reduce power and may operate at reduced data rates. There exist situations where ODT Enable mode can not be guaranteed for a short period of time, i.e. during power up.

Following are four terminologies defined for the state of a device (GDDR5 SGRAM or controller) pin during operation. The state of the bus will be determined by the combination of the device pins connected to the bus in the system. For example in GDDR5 it is possible for the SGRAM pin to be tristated while the controller pin is High or ODT. In both cases the bus would be High if the ODT is enabled.

Device pin signal level:

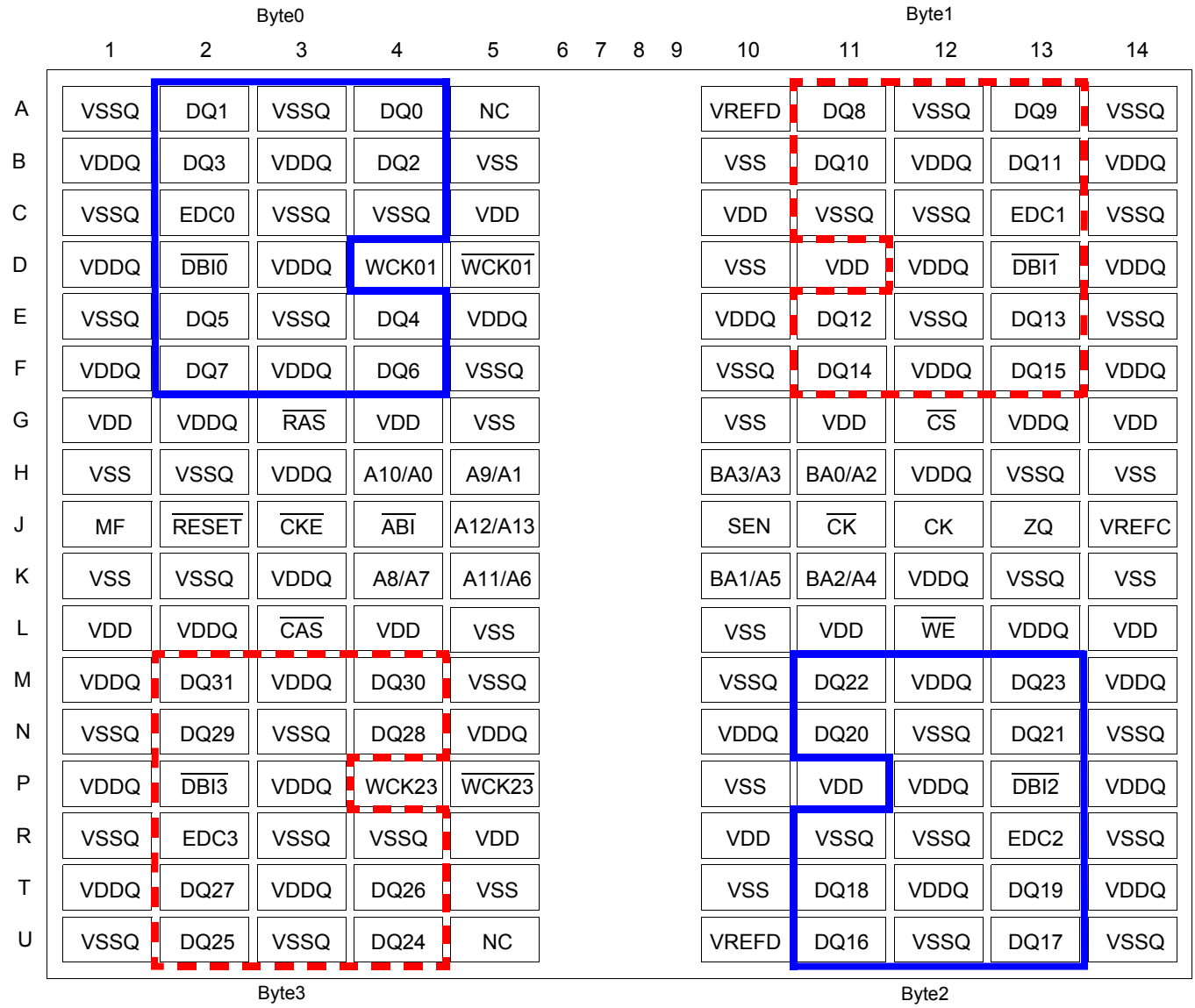
- High: A device pin is driving the Logic "1" state.
- Low: A device pin is driving the Logic "0" state.
- Hi-Z: A device pin is tristate.
- ODT: A device pin terminates with ODT setting, which could be terminating or tristate depending on MRS.

Bus signal level:

- High: One device on bus is High and all other devices on bus are either ODT or Hi-Z. The voltage level on the bus would be nominally VDDQ.
- Low: One device on bus is Low and all other devices on bus are either ODT or Hi-Z. The voltage level on the bus would be nominally VOL(DC) if ODT was enabled, or VSSQ if Hi-Z.
- Hi-Z: All devices on bus are Hi-Z. The voltage level on bus is undefined as the bus is floating.
- ODT: At least one device on bus is ODT and all others are Hi-Z. The voltage level on the bus would be nominal VDDQ.

5. PIN CONFIGURATION

5.1 GDDR5 SGRAM 170ball BGA Ball-out MF=0



NOTE : Top View (as seen through package), MF = LOW (MF = 0)
RFU is reserved for future use
NC is a not connected pin

5.2 GDDR5 SGRAM 170ball BGA Ball-out MF=1

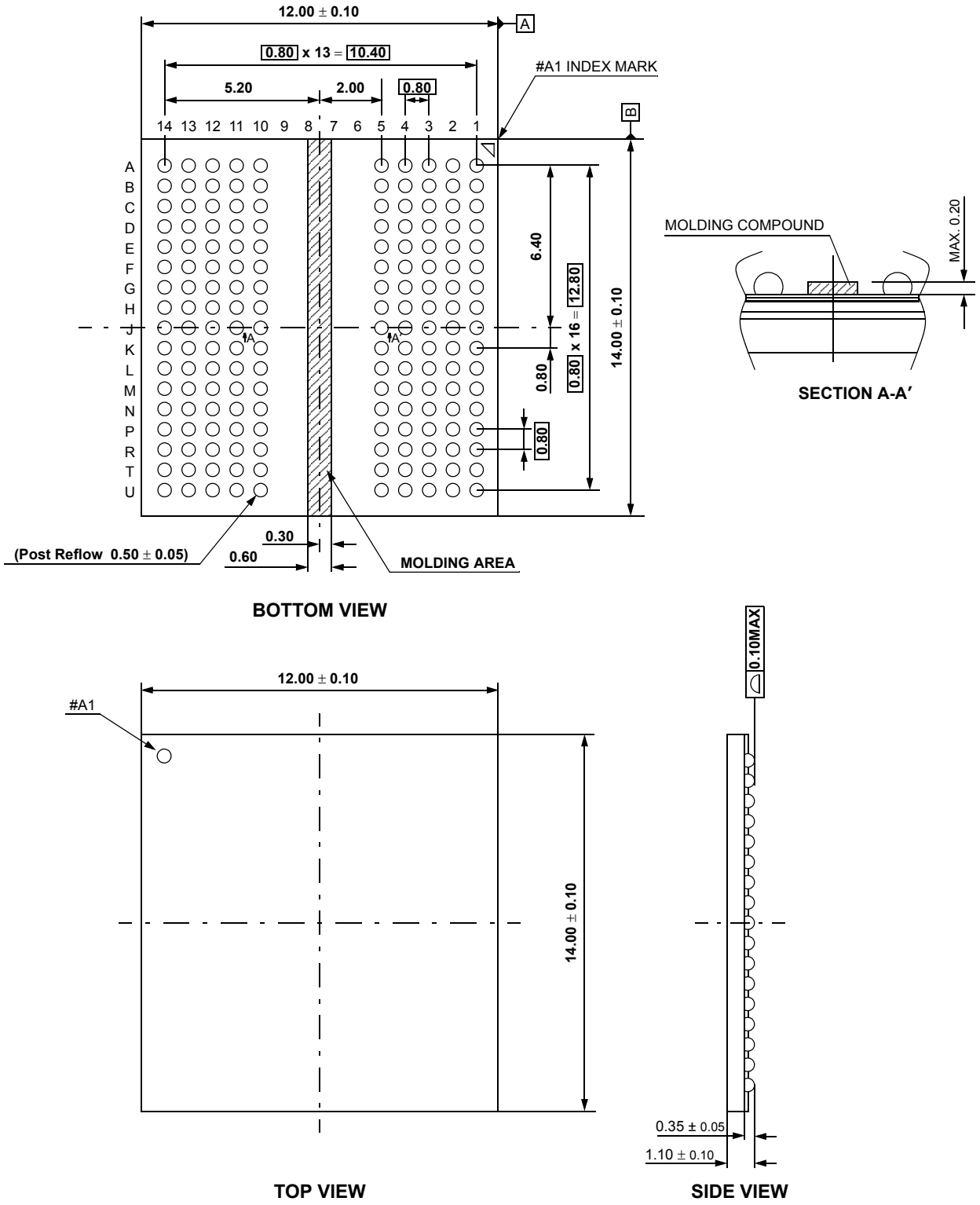
	Byte3									Byte2				
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSSQ	DQ25	VSSQ	DQ24	NC					VREFD	DQ16	VSSQ	DQ17	VSSQ
B	VDDQ	DQ27	VDDQ	DQ26	VSS					VSS	DQ18	VDDQ	DQ19	VDDQ
C	VSSQ	EDC3	VSSQ	VSSQ	VDD					VDD	VSSQ	VSSQ	EDC2	VSSQ
D	VDDQ	$\overline{\text{DBI3}}$	VDDQ	WCK23	$\overline{\text{WCK23}}$					VSS	VDD	VDDQ	$\overline{\text{DBI2}}$	VDDQ
E	VSSQ	DQ29	VSSQ	DQ28	VDDQ					VDDQ	DQ20	VSSQ	DQ21	VSSQ
F	VDDQ	DQ31	VDDQ	DQ30	VSSQ					VSSQ	DQ22	VDDQ	DQ23	VDDQ
G	VDD	VDDQ	$\overline{\text{CAS}}$	VDD	VSS					VSS	VDD	$\overline{\text{WE}}$	VDDQ	VDD
H	VSS	VSSQ	VDDQ	A8/A7	A11/A6					BA1/A5	BA2/A4	VDDQ	VSSQ	VSS
J	MF	$\overline{\text{RESET}}$	$\overline{\text{CKE}}$	$\overline{\text{ABI}}$	A12/A13					SEN	$\overline{\text{CK}}$	CK	ZQ	VREFC
K	VSS	VSSQ	VDDQ	A10/A0	A9/A1					BA3/A3	BA0/A2	VDDQ	VSSQ	VSS
L	VDD	VDDQ	$\overline{\text{RAS}}$	VDD	VSS					VSS	VDD	$\overline{\text{CS}}$	VDDQ	VDD
M	VDDQ	DQ7	VDDQ	DQ6	VSSQ					VSSQ	DQ14	VDDQ	DQ15	VDDQ
N	VSSQ	DQ5	VSSQ	DQ4	VDDQ					VDDQ	DQ12	VSSQ	DQ13	VSSQ
P	VDDQ	$\overline{\text{DBI0}}$	VDDQ	WCK01	$\overline{\text{WCK01}}$					VSS	VDD	VDDQ	$\overline{\text{DBI1}}$	VDDQ
R	VSSQ	EDC0	VSSQ	VSSQ	VDD					VDD	VSSQ	VSSQ	EDC1	VSSQ
T	VDDQ	DQ3	VDDQ	DQ2	VSS					VSS	DQ10	VDDQ	DQ11	VDDQ
U	VSSQ	DQ1	VSSQ	DQ0	NC					VREFD	DQ8	VSSQ	DQ9	VSSQ
	Byte0									Byte1				

X32 mode : On
X16 mode : On

X32 mode : On
X16 mode : Off

NOTE : Top View (as seen through package), MF = HIGH (MF = 1) - When mirrored, physical byte location is not changed but logical byte location is mirrored.

5.3 Package Outline



6. INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
WCK01, WCK01, WCK23, WCK23	Input	**Clock:** WCK and WCK are differential clock inputs. Data inputs are sampled on the crossing of the positive edge of WCK and positive edge of WCK. WCK01/WCK01 are in charge of DQ's in byte0 and byte1 and WCK23/WCK23 are in charge of DQ's in byte2 and byte3.
CK, CK	Input	**Clock:** CK and CK are differential clock inputs. CMD inputs are sampled on the positive edge of CK and ADD inputs are sampled on both positive edge of CK and positive edge of CK.
CKE	Input	**Clock Enable:** CKE Low activates, and CKE High deactivates, internal clock signals and device input buffers and output drivers. Taking CKE High provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained Low throughout read and write accesses. Input buffers, excluding CK, CK and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh. CKE which is triggered on the positive edge of RESET is used to define the resistance of on-die termination at power-up.
CS	Input	**Chip Select:** All commands are masked when CS is registered HIGH. It is possible to share CS pin between dual loads. CS is considered part of the command code.
RAS, CAS, WE	Input	**Command Inputs:** RAS, CAS and WE (along with CS, A8, A10, A11) define the command being entered.
BA0 ~ BA3	Input	**Bank Address Inputs:** BA0, BA1, BA2 and BA3 define to which bank commands are being applied.
A0 ~ A13	Input	**Address Inputs:** Provided the row address for Active command and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A8 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A8 LOW) or all banks (A8 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1,BA2, BA3. The address inputs also provide the op-code during Mode Register Set commands. Row addresses: RA0 ~ RA13, Column addresses: CA0~CA6(CA7), Column address CA8 is used for auto precharge. A10 and A11 is used for command decoding such as WRTR, RDTR, LDFF, WSM and WDM.
DQ0 ~ DQ31	Input/ Output	**Data Input/Output:** Bi-directional data bus.
EDC0 ~ EDC3	Input/ Output	**Cyclic Redundancy Code for EDC:** EDC pin outputs CRC code out of DRAM according to input/output with data. In RDQS MRS mode, EDC outputs DQ strobe instead of CRC code. EDC1 pin is used to define x32/x16 configuration at power-up. Unless RDQS, CRC and WCK2CK training are turned on, EDC hold pattern appears on the EDC pins.
DBI0 ~ DBI3	Input/ Output	**Data Bus Inversion:** It is a flag to indicate the inversion of input/output data.
NC		Not connected. Reserved for future use pin
VDDQ	Supply	DQ Power Supply
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply
VSS	Supply	Ground
VREFD VREFC	Supply	**Reference voltage:** 0.7*VDDQ, VREFD: (A,10) and (V,10) for DQ, VREFC: (J,14) for CMD and ADD
MF	Input	Mirror Function: A flag that indicates whether package is in clamshell configuration or not.
ZQ	Reference	**ZQ auto-calibration:** Resistor connection pin for auto-calibration
RESET	Input	**Reset pin:** It is used to initialize DRAM function. It is used to define the resistance of on-die termination/x16 mode by sampling CKE/EDC1 value during power-up.
SEN	Input	**Boundary Scan enable:** Boundary Scan is enabled by asserting SEN to HIGH at power-up.
ABI	Input	**Address Bus Inversion**: It is a flag to indicate the inversion of addresses

7. MIRROR FUNCTION SINGAL MAPPING

Signal Assignment in MF=0 and MF=1

Mirror Function Signal Mapping Columns 1 to 5

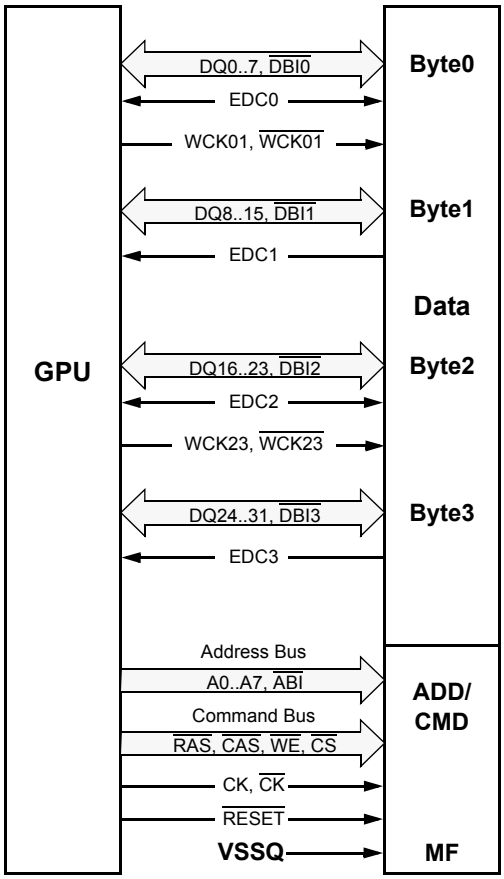
PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1
A1	VSSQ		A2	DQ1	DQ25	A3	VSSQ		A4	DQ0	DQ24	A5	NC	
B1	VDDQ		B2	DQ3	DQ27	B3	VDDQ		B4	DQ2	DQ26	B5	VSS	
C1	VSSQ		C2	EDC0	EDC3	C3	VSSQ		C4	VSSQ		C5	VDD	
D1	VDDQ		D2	$\overline{DBI0}$	$\overline{DBI3}$	D3	VDDQ		D4	WCK01	WCK23	D5	$\overline{WCK01}$	$\overline{WCK23}$
E1	VSSQ		E2	DQ5	DQ29	E3	VSSQ		E4	DQ4	DQ28	E5	VDDQ	
F1	VDDQ		F2	DQ7	DQ31	F3	VDDQ		F4	DQ6	DQ30	F5	VSSQ	
G1	VDD		G2	VDDQ		G3	$\overline{RAS}$	$\overline{CAS}$	G4	VDD		G5	VSS	
H1	VSS		H2	VSSQ		H3	VDDQ		H4	A10/A0	A8/A7	H5	A9/A1	A11/A6
J1	MF		J2	$\overline{RESET}$		J3	$\overline{CKE}$		J4	$\overline{ABI}$		J5	A12/A13	
K1	VSS		K2	VSSQ		K3	VDDQ		K4	A8/A7	A10/A0	K5	A11/A6	A9/A1
L1	VDD		L2	VDDQ		L3	$\overline{CAS}$	$\overline{RAS}$	L4	VDD		L5	VSS	
M1	VDDQ		M2	DQ31	DQ7	M3	VDDQ		M4	DQ30	DQ6	M5	VSSQ	
N1	VSSQ		N2	DQ29	DQ5	N3	VSSQ		N4	DQ28	DQ4	N5	VDDQ	
P1	VDDQ		P2	$\overline{DBI3}$	$\overline{DBI0}$	P3	VDDQ		P4	WCK23	WCK01	P5	$\overline{WCK23}$	$\overline{WCK01}$
R1	VSSQ		R2	EDC3	EDC0	R3	VSSQ		R4	VSSQ		R5	VDD	
T1	VDDQ		T2	DQ27	DQ3	T3	VDDQ		T4	DQ26	DQ2	T5	VSS	
U1	VSSQ		U2	DQ25	DQ1	U3	VSSQ		U4	DQ24	DQ0	U5	NC	

Mirror Function Signal Mapping Columns 10 to 14

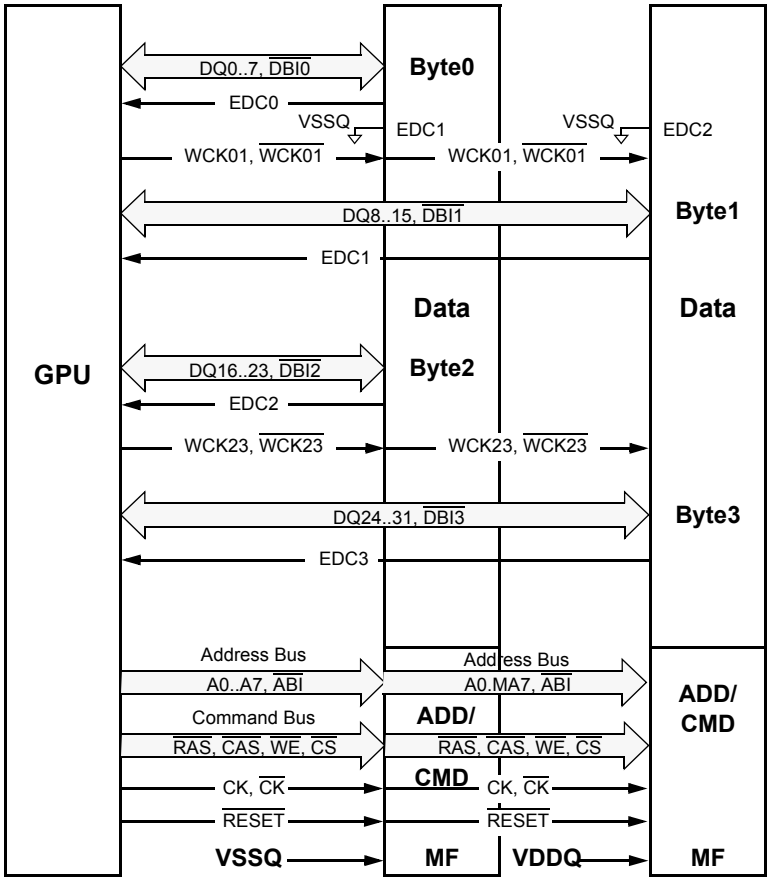
PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1
A10	VREFD		A11	DQ8	DQ16	A12	VSSQ		A13	DQ9	DQ17	A14	VSSQ	
B10	VSS		B11	DQ10	DQ18	B12	VDDQ		B13	DQ11	DQ19	B14	VDDQ	
C10	VDD		C11	VSSQ		C12	VSSQ		C13	EDC1	EDC2	C14	VSSQ	
D10	VSS		D11	VDD		D12	VDDQ		D13	$\overline{DBI1}$	$\overline{DBI2}$	D14	VDDQ	
E10	VDDQ		E11	DQ12	DQ20	E12	VSSQ		E13	DQ13	DQ21	E14	VSSQ	
F10	VSSQ		F11	DQ14	DQ22	F12	VDDQ		F13	DQ15	DQ23	F14	VDDQ	
G10	VSS		G11	VDD		G12	$\overline{CS}$	$\overline{WE}$	G13	VDDQ		G14	VDD	
H10	BA3/A3	BA1/A5	H11	BA0/A2	BA2/A4	H12	VDDQ		H13	VSSQ		H14	VSS	
J10	SEN		J11	$\overline{CK}$		J12	CK		J13	ZQ		J14	VREFC	
K10	BA1/A5	BA3/A3	K11	BA2/A4	BA0/A2	K12	VDDQ		K13	VSSQ		K14	VSS	
L10	VSS		L11	VDD		L12	$\overline{WE}$	$\overline{CS}$	L13	VDDQ		L14	VDD	
M10	VSSQ		M11	DQ22	DQ14	M12	VDDQ		M13	DQ23	DQ15	M14	VDDQ	
N10	VDDQ		N11	DQ20	DQ12	N12	VSSQ		N13	DQ21	DQ13	N14	VSSQ	
P10	VSS		P11	VDD		P12	VDDQ		P13	$\overline{DBI2}$	$\overline{DBI1}$	P14	VDDQ	
R10	VDD		R11	VSSQ		R12	VSSQ		R13	EDC2	EDC1	R14	VSSQ	
T10	VSS		T11	DQ18	DQ10	T12	VDDQ		T13	DQ19	DQ11	T14	VDDQ	
U10	VREFD		U11	DQ16	DQ8	U12	VSSQ		U13	DQ17	DQ9	U14	VSSQ	

8. x16/x32 SYSTEM CONFIGURATION

x32 Mode

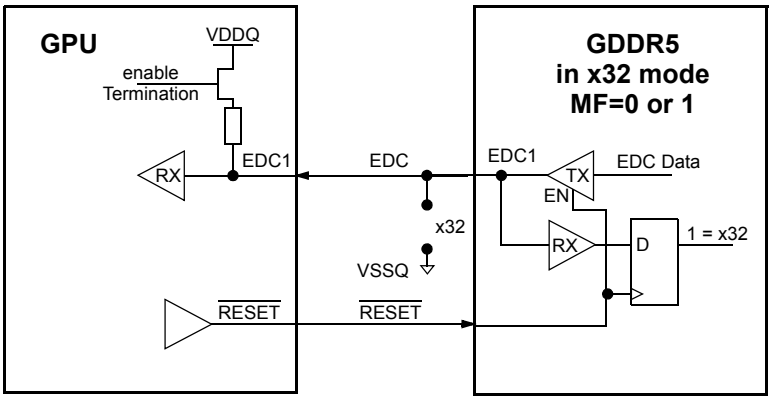


x16 Mode



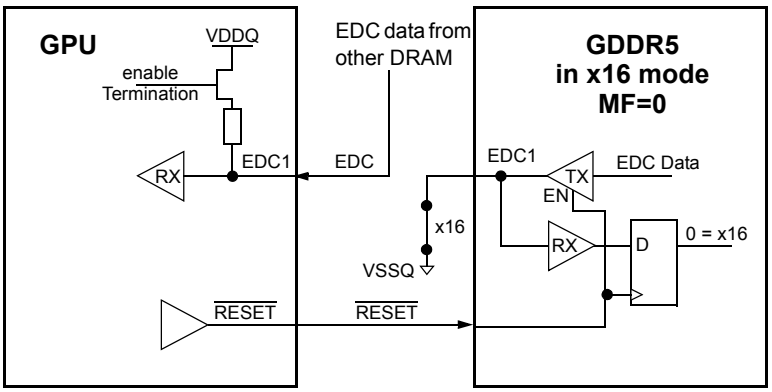
9. x16/x32 MODE SELECTION

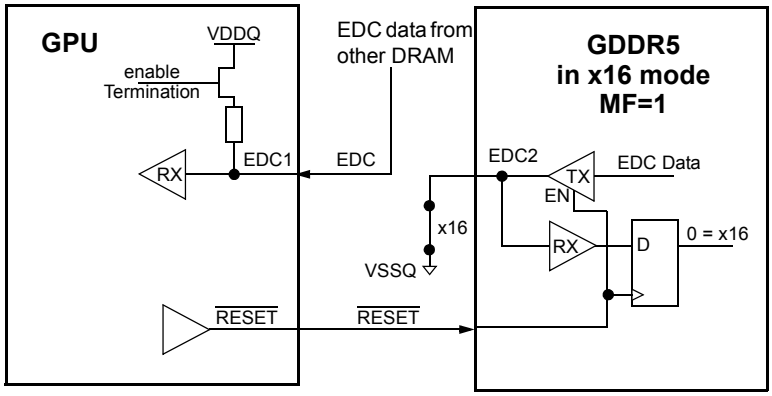
x32 Mode



x32 mode is selected at power-up when EDC1 is sampled HIGH on the rising edge of $\overline{\text{RESET}}$. The on-die termination of EDC1 on the GPU side pin has to be driven in order to be configured as x32 mode. On the DRAM side, EDC1 is not driven.
When mirrored, logically renamed EDC2 pin has to be used instead of EDC1, that is to say, the physical location of the pin for x16/x32 selection is not changed, however when mirrored, the pin name and ball name are changed from EDC1(C13) to EDC2(R13).

x16 Mode





When x16 mode is selected instead of x32 mode, only 2 bytes (byte0 and byte2 when MF=0) are enabled and A6 is used as a column address. The x16 mode is selected when EDC1 is sampled LOW on the rising edge of $\overline{\text{RESET}}$. The EDC1 is not driven by DRAM since byte 1 and byte 3 (when MF=0) are turned off always in x16 mode. The EDC1 can be disconnected from GPU and connected to ground via 10Kohm resistance.

x16/x32 mode can not be changed during operation. It is selected only at power-up according to board configuration.

[Table 1] x16 Mode and MF

MODE	MF	EDC1	EDC2
x16 non-mirrored	VSSQ	VSSQ	VDDQ
x32non-mirrored	VSSQ	VDDQ (terminatied by the system or controller)	VDDQ (terminatied by the system or controller)
x16 mirrored	VDDQ	VDDQ	VSSQ
x32 mirrored	VDDQ	VDDQ (terminatied by the system or controller)	VDDQ (terminatied by the system or controller)

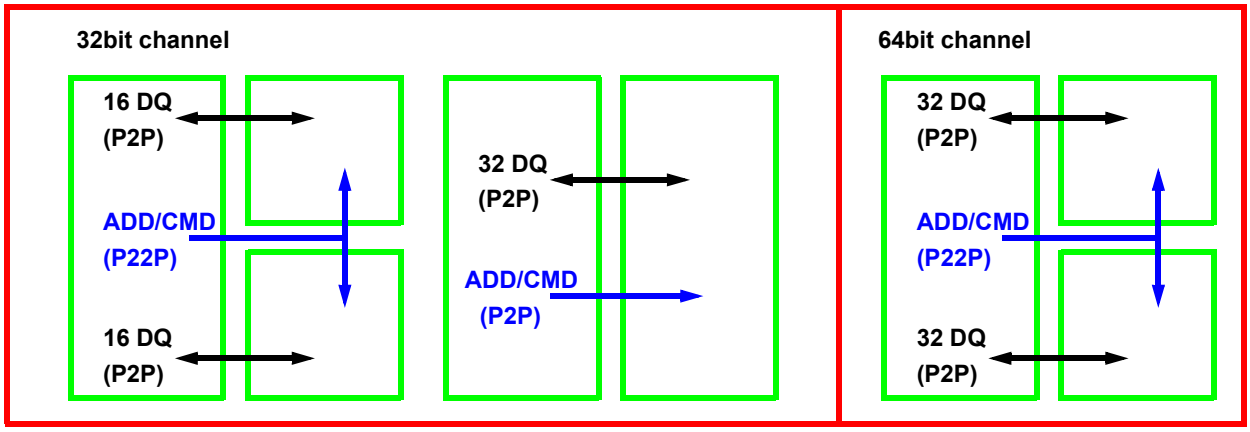


Figure 1. Example Channel Topologies

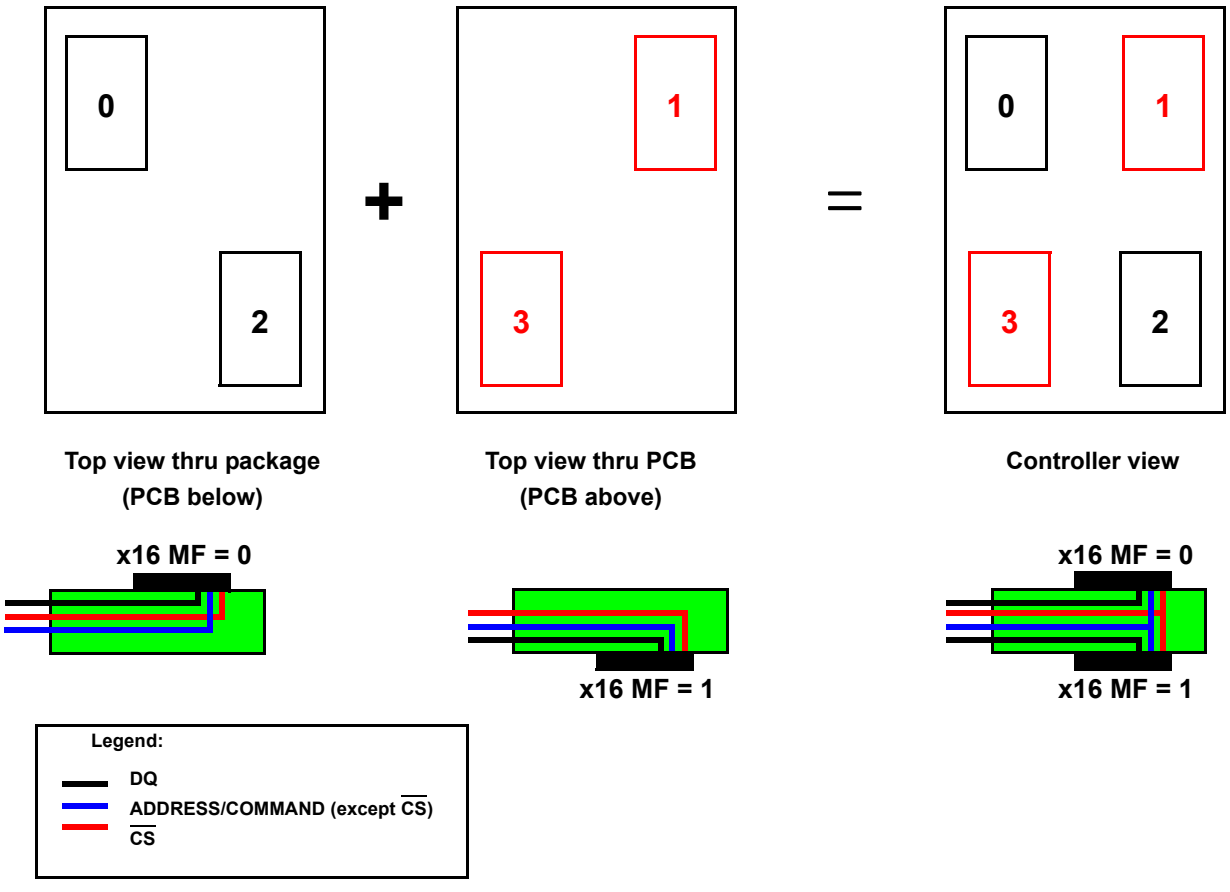


Figure 2. Byte Orientation in Clamshell Topology

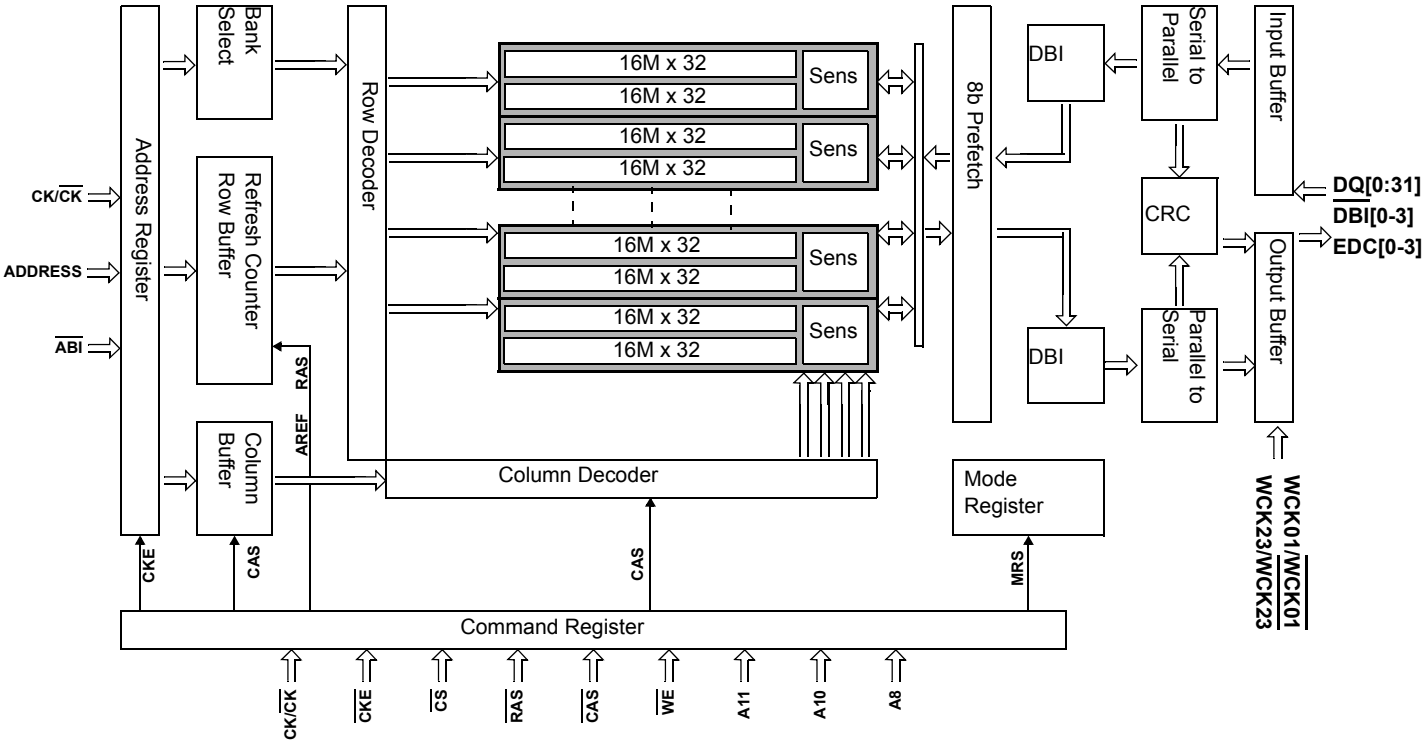


Figure 3. Block Diagram (16Mbit x32 I/O x16 Banks)

10. CLOCKING

GDDR5 command and address interface operates from a differential clock (CK and $\overline{CK}$). Commands are registered single data rate (SDR) at every rising edge of CK, and addresses are registered double data rate (DDR) at every rising edge of CK and rising edge of $\overline{CK}$. GDDR5 uses a DDR data interface and an 8n-prefetch architecture. The data interface uses two differential forwarded clocks (WCK/$\overline{WCK}$) that are source synchronous to the DQs. DDR means that the data is registered at every rising edge of WCK and rising edge of $\overline{WCK}$. WCK and $\overline{WCK}$ are continuously running and operate at twice the frequency of the command/address clock (CK/$\overline{CK}$).

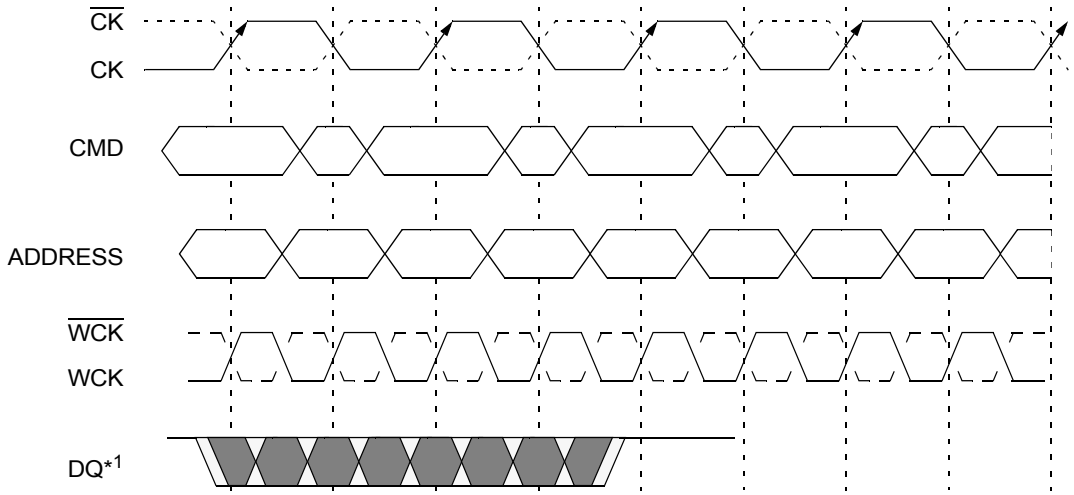


Figure 4. GDDR5 Clocking and Interface Relationship

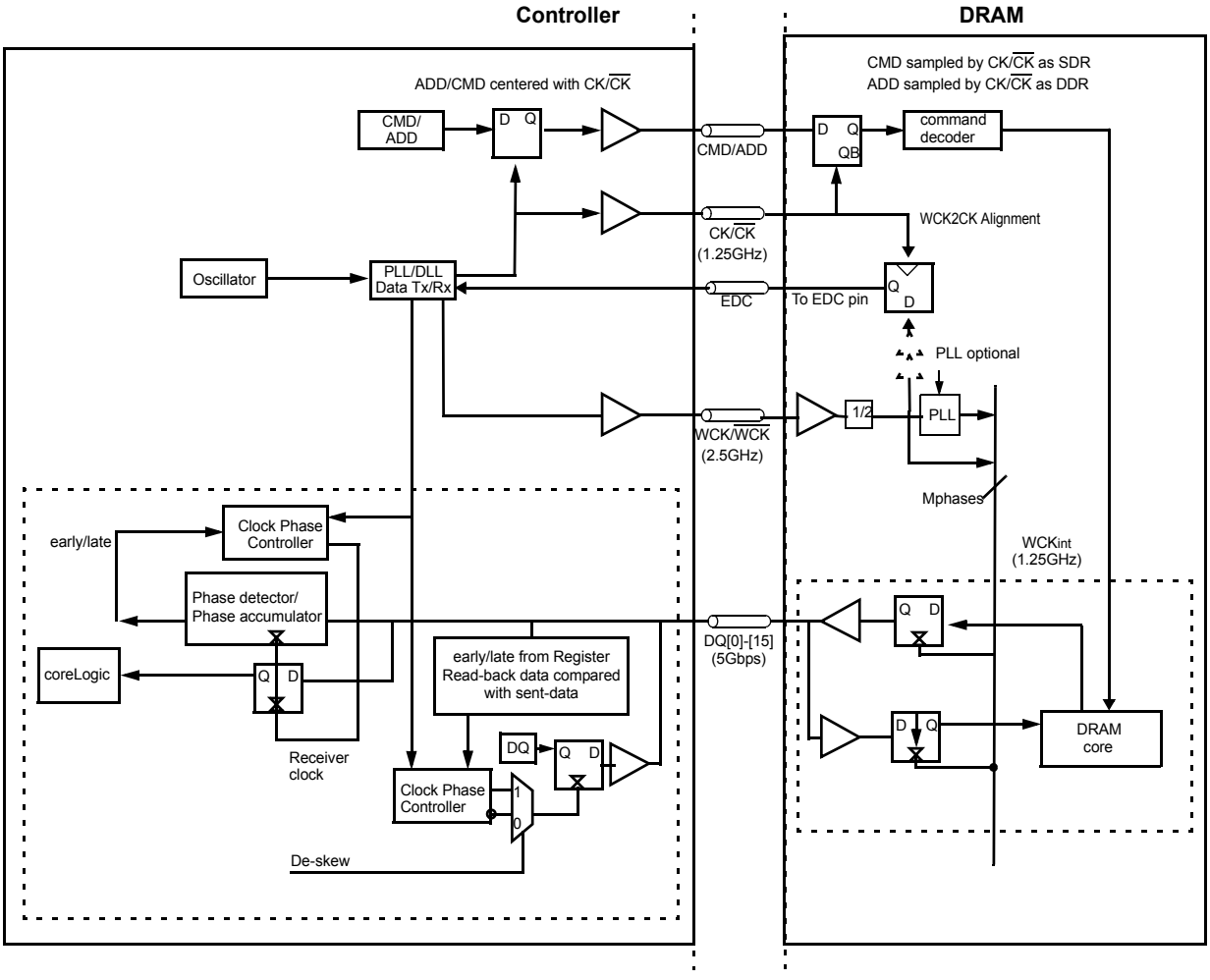


Figure 5. GDDR5 System Configuration

11. ADDRESS

11.1 Addressing

GDDR5 SGRAMs use a double data rate address scheme to reduce address pins required on the GDDR5 SGRAM as the following table. The addresses should be provided to the GDDR5 SGRAM in two parts that are latched into the memory with two consecutive rising clock edges. Command protocols incorporating signals such as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ should be issued at the first rising edge of CK and half of the addresses will be registered along with command inputs. The remaining half of the addresses will be registered at the next rising edge of $\overline{CK}$.
The use of DDR addressing allows all address values to be latched in at the same rate as the SDR commands. All addresses related to command access have been positioned for latching on the initial rising edge for faster decoding.

[Table 2] Address Pairs

Rising CK	BA3	BA2	BA1	BA0	A12	A11	A10	A9	A8
Rising $\overline{CK}$	A3	A4	A5	A2	A13	A6	A0	A1	A7

[Table 3] 8Gb GDDR5 SGRAM Addressing

CONFIGURATION	8Gb GDDR5		NOTE
	x32	x16	
Row address	A0 ~ A13	A0 ~ A13	
Column address	A0 ~ A6	A0 ~ A7	1
Bank address	BA0 ~ BA3	BA0 ~ BA3	
Autoprecharge	A8	A8	
Page Size	4K	4K	
Refresh	16K/32ms	16K/32ms	
Refresh period	1.9us	1.9us	
Bank Group	4	4	

NOTE : For 8Gb GDDR5, A7 is used as a column address for x16 mode

11.1.1 Burst Type

Read and write accesses to the 256Mx32 GDDR5 are burst-oriented, with the burst length fixed at 8 and thus not programmable in the MRS as with many other DRAMs. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accessed for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A0 ~ Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration).

11.2 Address Bus Inversion (ABI)

The GDDR5 SGRAM Address Bus Inversion (ABIdc) reduces the DC power requirements on address pins as the no. of address lines driving a low level can be limited to 4. The Address Bus Inversion function is associated with the electrical signalling on the address lines between a controller and the GDDR5 SGRAM, regardless of whether the information conveyed on the address lines is a row or column address, a mode register op-code, a data mask, or any other pattern. The $\overline{ABI}$ input pin is an active Low double data rate (DDR) signal and sampled by the GDDR5 SGRAM at the rising edge of CK and the rising edge of $\overline{CK}$ along with the address inputs.
Once enabled by the corresponding ABI Mode Register bit, the GDDR5 SGRAM will invert the pattern received on the address inputs in case $\overline{ABI}$ was sampled low, or leave the pattern non-inverted in case $\overline{ABI}$ was sampled High.

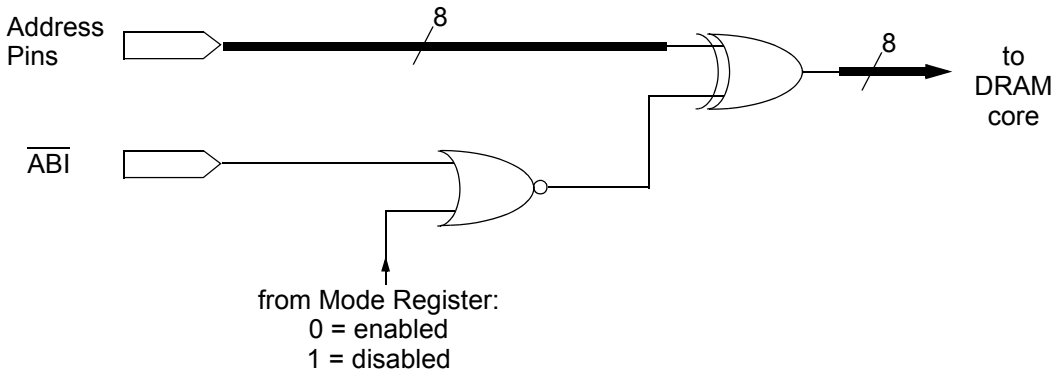


Figure 6. Example of Address Bus Inversion Logic

The flow diagram illustrates the ABIdc operation. The controller decides whether to invert or not invert the data conveyed on the address lines. The GDDR5 SGRAM has to perform the reverse operation based on the level of the $\overline{ABI}$ pin.

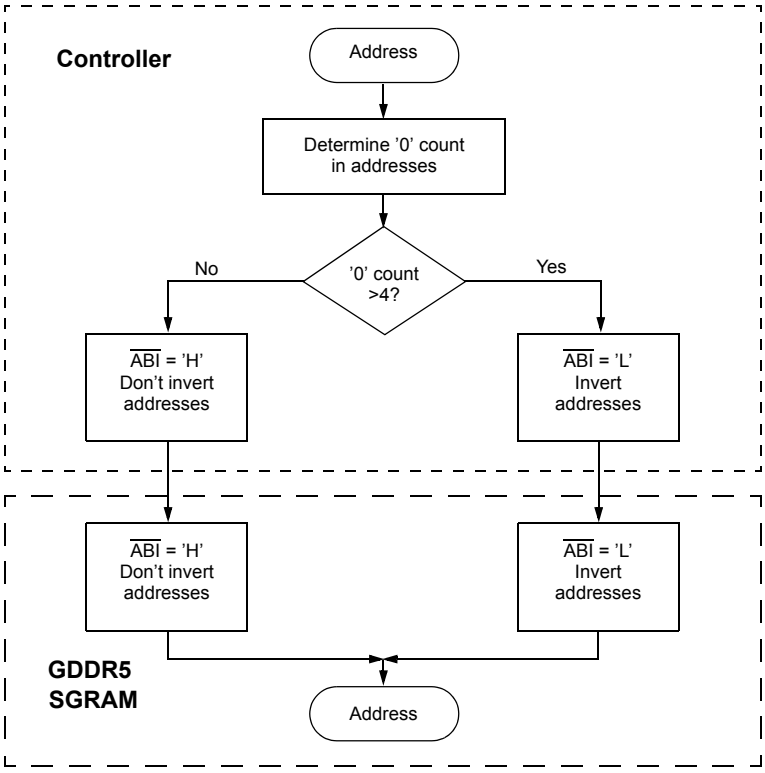


Figure 7. Address Bus Inversion (ABI) Flow Diagram

11.3 Bank Group

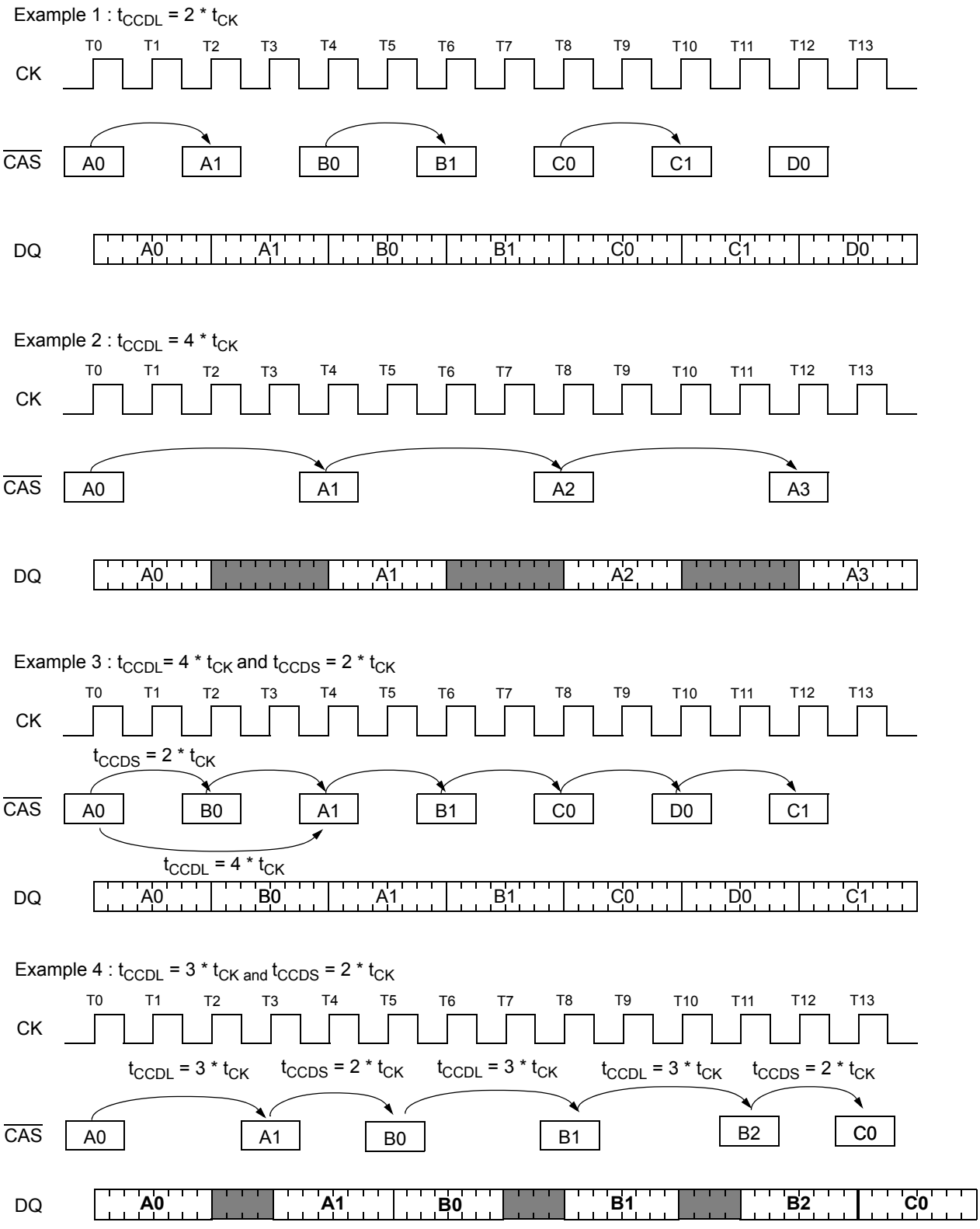
For GDDR5 SGRAM devices operating at frequencies above a certain threshold, the activity within a bank group must be restricted to ensure proper operation of GDDR5 SGRAM. The 16 banks in GDDR5 SGRAMs are divided into four bank groups. The assignment of the banks to the bank groups is shown in the following table.

[Table 4] GDDR5 SGRAM Bank Groups

Bank	Addressing				8Gb
	BA3	BA2	BA1	BA0	16 Banks
0	0	0	0	0	Group A
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	Group B
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	Group C
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	Group D
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

These bank groups allow the specification of different CAS-to-CAS command delay parameters depending on whether back-to-back column accesses are to banks within one bank group or across bank groups:
tCCDL = min. CAS-to-CAS command delay within one bank group (L = long)
tCCDS= min. CAS-to-CAS command delay between different bank groups (S = short)

Following figure shows back-to-back column accesses based on t_{CCDL} and t_{CCDS} parameters



NOTE :
1. column accesses are to open banks, and tRCD has been met
2. CL = 0 assumed
3. Ax, Bx, Cx, Dx: accesses to bank groups A, B, C or D, respectively

12. GDDR5 Commands Truth Table

Operation	Symbol	$\overline{CKE}$		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	WE	BA	A11	A10	A8	A6, A7, A9	A0~A5 (A6)	NOTE
		Previous cycle	Current cycle											
DESELECT (NOP)	DESEL	L	X	H	X	X	X	X	X	X	X	X	X	1, 2, 8
NO OPERATION (NOP)	NOP	L	X	L	H	H	H	X	X	X	X	X	X	1, 2, 8
Mode Register Set	MRS	L	L	L	L	L	L	MRA	Opcode					1, 2, 3
ACTIVE(Select bank & activate row)	ACT	L	L	L	L	H	H	BA	RA					1, 2, 4
READ (Select bank and column & start READ burst)	RD	L	L	L	H	L	H	BA	L	L	L	X	CA	1, 2, 5, 9
READ with Autopre-charge	RDA	L	L	L	H	L	H	BA	L	L	H	X	CA	1, 2, 5
Load FIFO	LDFF	L	L	L	H	L	H	X	H	L	L	X	X	1, 2, 7
READ Training	RDTR	L	L	L	H	L	H	X	H	H	L	X	X	1, 2
WRITE without Mask (Select bank and column & start write burst)	WOM	L	L	L	H	L	L	BA	L	L	L	X	CA	1, 2, 5
WRITE without Mask with Autoprecharge	WOMA	L	L	L	H	L	L	BA	L	L	H	X	CA	1, 2, 5
WRITE with single-byte mask	WSM	L	L	L	H	L	L	BA	L	H	L	X	CA	1, 2, 5
WRITE with single-byte mask with Autoprecharge	WSMA	L	L	L	H	L	L	BA	L	H	H	X	CA	1, 2, 5
WRITE with double-byte mask(WDM)	WDM	L	L	L	H	L	L	BA	H	L	L	X	CA	1, 2, 5
WRITE with double-byte mask with Autoprecharge	WDMA	L	L	L	H	L	L	BA	H	L	H	X	CA	1, 2, 5
WRITE Training	WRTR	L	L	L	H	L	L	X	H	H	L	X	X	1, 2
PRECHARGE (Deacti-vate row in bank or banks)	PRE	L	L	L	L	H	L	BA	X	X	L	X	X	1, 2
PRECHARGE ALL	PREALL	L	L	L	L	H	L	X	X	X	H	X	X	1, 2
AUTO REFRESH	REF	L	L	L	L	L	H	X	X	X	X	X	X	1, 6
POWER DOWN ENTRY	PDE	L	H	H	X	X	X	X	X	X	X	X	X	1
				L	H	H	H	X	X	X	X	X	X	1
POWER DOWN EXIT	PDX	H	L	H	X	X	X	X	X	X	X	X	X	1
				L	H	H	H							
SELF REFRESH ENTRY	SRE	L	H	L	L	L	H	X	X	X	X	X	X	1, 6
SELF REFRESH EXIT	SRX	H	L	H	X	X	X	X	X	X	X	X	X	1
				L	H	H	H							

NOTE :
1. H = Logic High Level; L = Logic Low Level; X = Don't care: Signal may be H or L, but not floating
2. Addresses shown are logical addresses; physical addresses are inverted when address bus inversion (ABI) is activated and $\overline{ABI}$=L
3. BA0.BA3 provide the Mode Register address (MRA), A0-A11 the opcode to be loaded
4. BA0.BA3 provide the bank address (BA), A0-A12 provide the row address (RA).
5. BA0.BA3 provide the bank address, A0-A5 (A6) provide the column address (CA); no sub-word addressing within a burst of 8. A6 is used as CA when x16 mode is enabled.
6. The command is Auto Refresh when $\overline{CKE}$(n) = L and Self Refresh Entry when $\overline{CKE}$(n) = H.
7. BA0-BA3 and CA are used to select burst location and data respectively
8. DESELECT and NOP are functionally interchangeable
9. In address training mode READ is decoded from the commands pins only with $\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = H

DESELECT

The DESELECT function ($\overline{CS}$ high) prevents new commands from being executed by the GDDR5(x32). The GDDR5(x32) SGRAM is effectively deselected. Operations already in progress are not affected. GDDR5 can consider DESELECT as a NOP command during functional operation.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct selected GDDR5(x32) to perform a NOP ($\overline{CS}$ LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. GDDR5 can consider NOP command as a DESELECT during functional operation.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0-A13. See mode register descriptions in the Register Definition section. The Load Mode Register command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 ,BA2 and BA3 inputs select the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1, BA2 and BA3 inputs select the bank, and the address provided on inputs A0-A5(A6) selects the starting column location. The value on input A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1, BA2 and BA3 inputs select the bank, and the address provided on inputs A0-A5(A6) selects the starting column location. The value on inputs A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the data masking information supplied on the address bus.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open rows in all banks. The bank(s) will be available for a subsequent row access in a specified time (t_{RP}) after the PRECHARGE command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0,BA1, BA2 and BA3 select the bank. Otherwise BA0, BA1, BA2 and BA3 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

READ TRAINING

In order to operate properly in high frequency, the setup and hold window of read and write should be optimized. RDTR is able to retrieve the output FIFO which has the known data pattern loaded by LDFF and WRTR command.

LOAD FIFO

In READ TRAINING, the known data pattern should be safely transferred to the output FIFO at high frequency. The data pattern can be transferred on the address bus which was optimized during address training at power-up.

WRITE TRAINING

The WRITE TRAINING should be optimized by writing data pattern directly to the output FIFO, reading the contents, and comparing the patterns. In order to find the boundary of the setup and hold window, the written DQ should be 90 degree shifted with respect to WCK/$\overline{WCK}$.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the GDDR5 DRAM even if the rest of the system is powered down. When in the self refresh mode, the GDDR5 DRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except $\overline{CKE}$ is disabled (HIGH). The PLL is automatically disabled upon entering SELF REFRESH and reset upon exiting SELF REFRESH. The on-die termination is also disabled upon entering SELF REFRESH. (tXSRD must occur before a read command can be issued, tXSNR must occur before a non-read command can be issued.) Input signals except $\overline{CKE}$ are "Don't Care" during SELF REFRESH.

AUTO REFRESH

AUTO REFRESH command is used during normal operation. This command is non persistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. The GDDR5 DRAM requires AUTO REFRESH commands at an average periodic interval of tREFI.

POWER DOWN

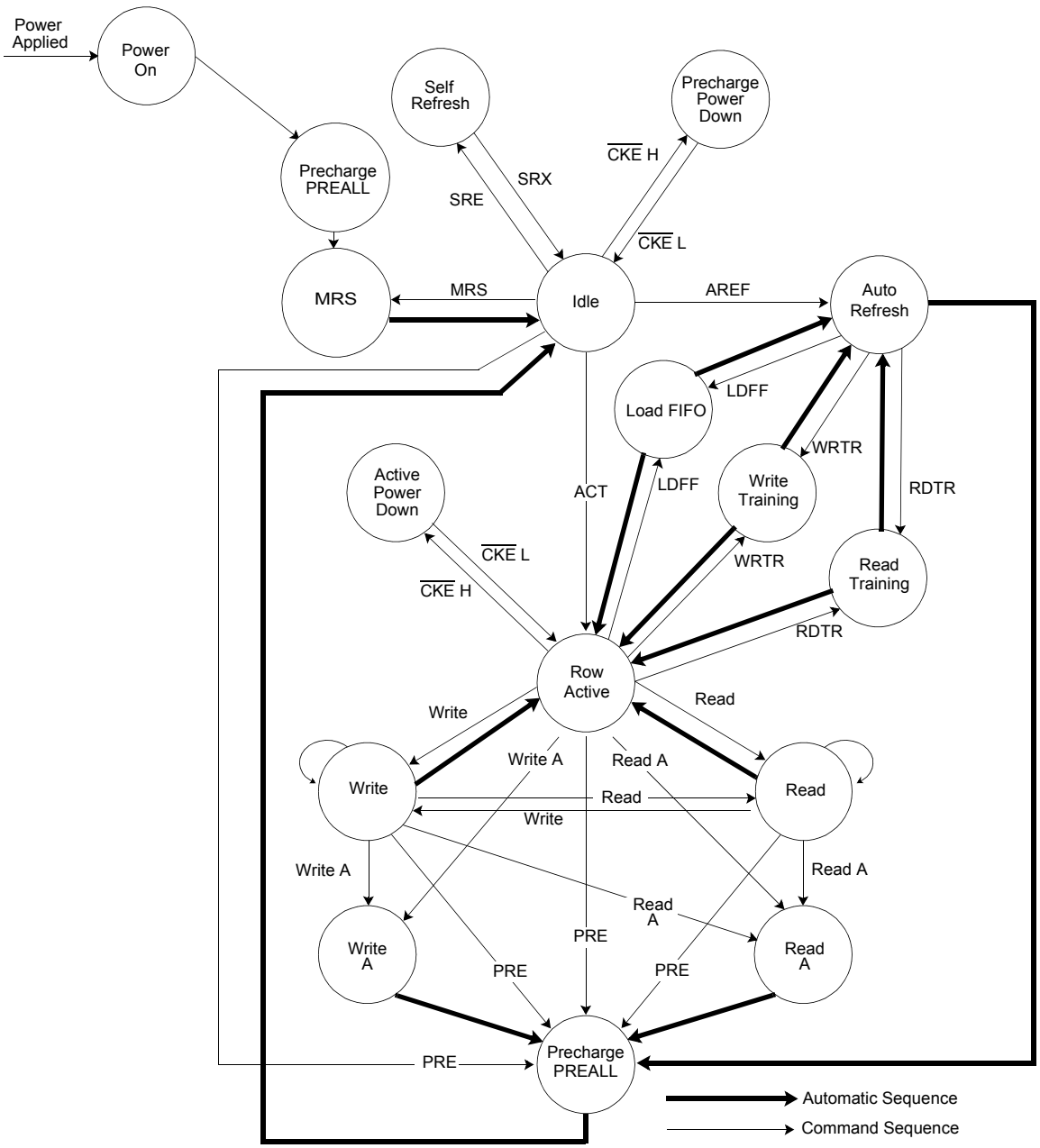
GDDR5 DRAM requires $\overline{CKE}$ to be active at all times that an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined when the read postamble is satisfied; For WRITEs, a burst completion is defined when the write postamble is satisfied. Power down is entered when $\overline{CKE}$ is registered HIGH. If power down occurs when all banks are idle, this mode is referred to precharge power down; if power down occurs when there is a row active in any banks, this mode is referred to active power down. Entering power down deactivates the input and output buffers, excluding CK, $\overline{CK}$, $\overline{RESET}$ and $\overline{CKE}$. However, power down duration is limited by the refresh requirements of the device. While in power down, $\overline{CKE}$ HIGH and a stable clock signal CK/$\overline{CK}$ must be maintained at the inputs of the GDDR5 DRAM, while all other input signals are "Don't Care".

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function, but without requiring an explicit command. This is accomplished by using A8 (A8=HIGH), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto Precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command. Auto Precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharging time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time.

13. FUNCTION DESCRIPTION

13.1 Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
SRE = Enter Self Refresh
SRX = Exit Self Refresh
AREF = Auto Refresh

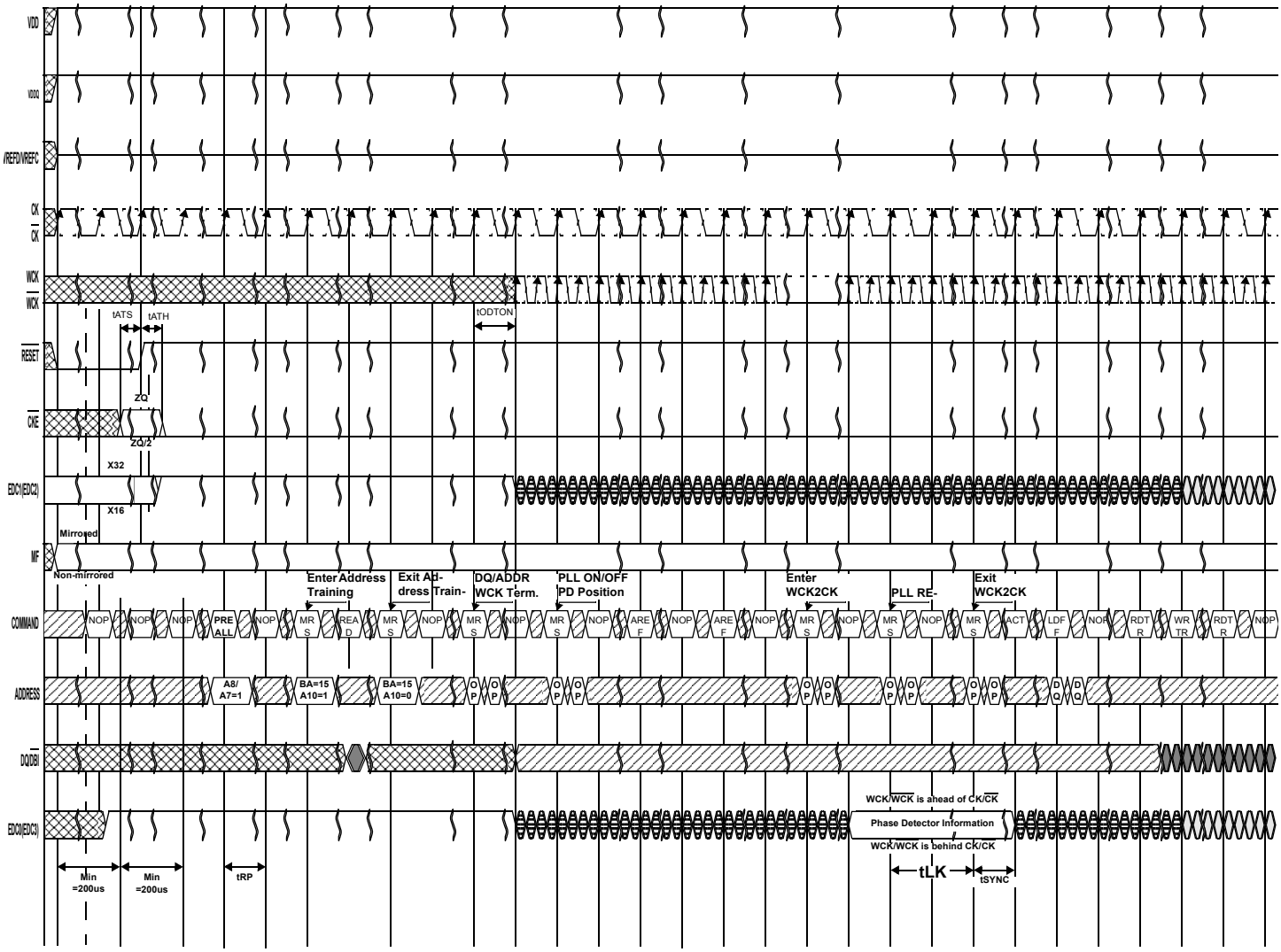
CKE H = Enter Power Down
CKE L = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

13.2 Initialization

GDDR5 SGRAMs must be powered up and initialized in a predefined manner as shown in below sequence. Operational procedures other than those specified may result in undefined operation. The Mode Registers do not have RESET default values, except for $\overline{ABI}$, ADR/CMD termination, and the EDC hold pattern. If the mode registers are not set during the initialization sequence, it may lead to unspecified operation.

Sequence	Function
1	Apply Power to VDD.
2	Apply power to VDDQ at same time or after power is applied to VDD. VDD/VDDQ power-up is defined as increase from below 300mV to target level. VDD/VDDQ must be increased monotonically during power-up.
3	Apply MF, VREFC and VREFD at same time or after power is applied to VDDQ.
4	After power is stable, provide stable clock signals CK/$\overline{CK}$.
5	Assert and hold $\overline{RESET}$ low for minimum 200us to ensure all drivers are in Hi-Z and all active terminations are off. Assert and hold NOP command.
6	Wait a minimum of 200us.
7	If boundary scan mode is necessary, SEN can be asserted HIGH to enter boundary scan mode. Boundary scan mode must be entered directly after power-up while $\overline{RESET}$ is low. Once boundary scan is executed, power-up sequence should be followed.
8	Set $\overline{CKE}$ for the desired ADD/CMD ODT settings, then bring $\overline{RESET}$ High to latch in the logic state of $\overline{CKE}$, tATS and tATH must be met during this procedure. Keep EDC1 (MF=0) / EDC2 (MF=1) at the same logic level as during power-up initialization as device functionality is not guaranteed if the I/O width has changed. See the following table for the values and logic states for $\overline{CKE}$. The rising edge of $\overline{RESET}$ will determine x32 mode or x16 mode depending on the state of EDC1(EDC2 when MF=1). In normal x32 mode, EDC1 has to be sustained HIGH until $\overline{RESET}$ is HIGH. See the following table for the values and logic states for EDC1(EDC2 when MF=1).
9	Hold the state of $\overline{CKE}$ and EDC1(EDC2 when MF=1) until tATH is satisfied.
10	Wait at least 200us referenced from the beginning of tATS.
11	Issue at least 2 NOP commands.
12	Issue a PRECHARGE ALL command followed by NOP commands until tRP is satisfied.
13	Issue MRS command to MR15. Set DRAM into address training mode. (optional)
14	Complete address training. (optional)
15	Vendor ID MRS command may be issued.
16	Issue MRS command to set WCK01/$\overline{WCK01}$ and WCK23/$\overline{WCK23}$ termination values.
17	Provide stable clock signals WCK01/$\overline{WCK01}$ and WCK23/$\overline{WCK23}$.
18	Issue MRS commands to use PLL or not and select the position of a WCK/CK phase detector. The use of PLL and the position of a phase detector should be issued before WCK2CK training. Issue MRS commands including PLL reset to the mode registers in any order. tMRD must be met during this procedure. WLmrs, CLmrs, CRCWL and CRCRL must be programmed before WCK2CK training.
19	Issue two AUTO REFRESH commands followed by Nop until tRFC is satisfied
20	WCK2CK training must be entered, sustained for at least tMRD and exited. Any command except NOP/DES is not allowed for another tMRD during tSYNC after exit of WCK2CK training. WCK2CK training can be entered during tLK. WCK2CK should not exit until PLL is locked.
21	After any necessary GDDR5 training sequences such as WCK2CK training, Read training (LDFF, RDTR) and Write training (WRTR, RDTR), the device is ready for operation.
22	In case of frequency change and abnormal operations, the power-up sequence should be executed for stable DRAM operation.

13.3 Initialization Timing



NOTE : Device functionality is not guaranteed if x32/x16 mode is not the same as during power-up initialization.

[Table 5] Address/Command termination value

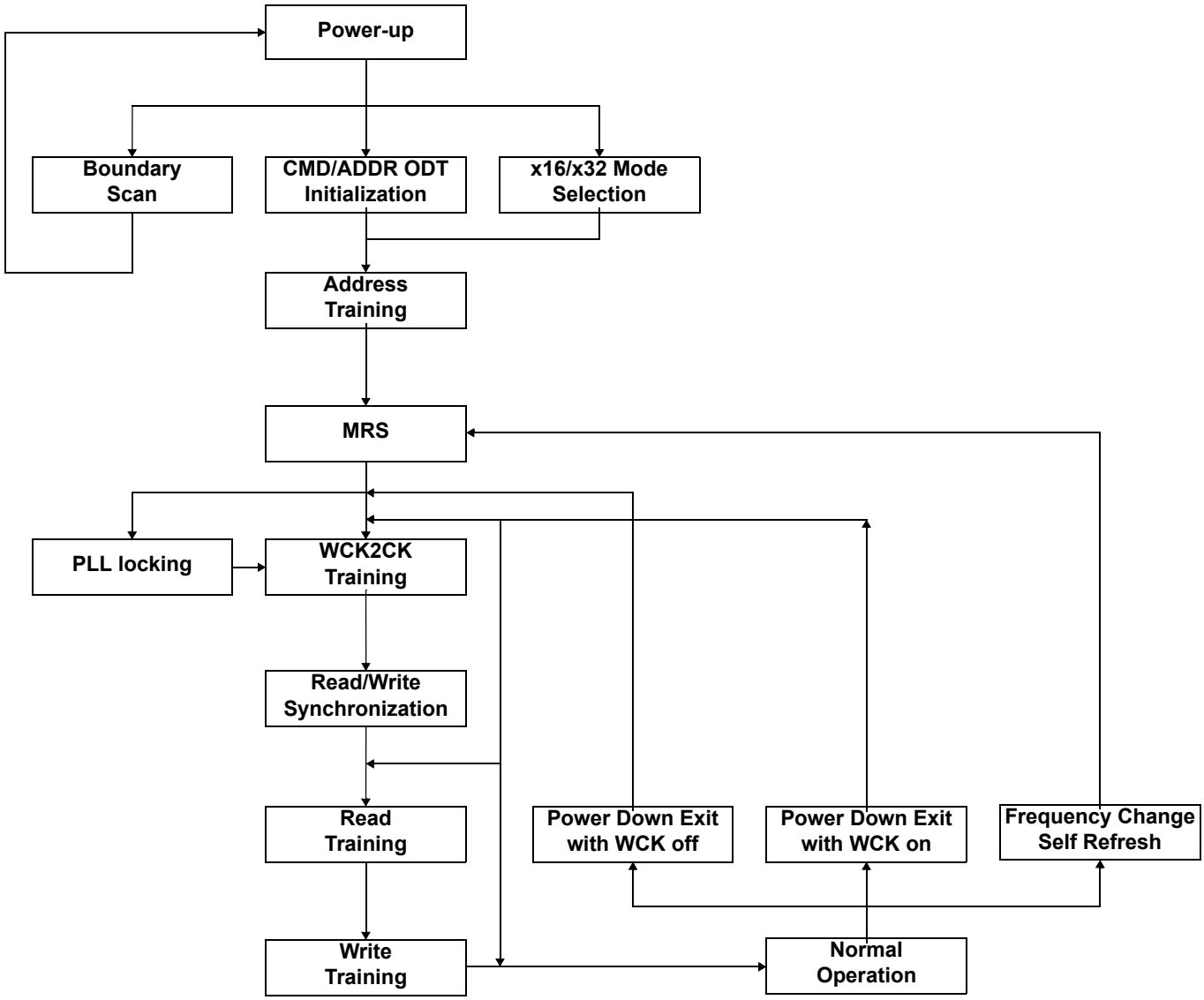
$\overline{CKE}$	ADD/CMD Termination Value (Ohms)
L	ZQ/2
H	ZQ

[Table 6] x16 Mode and MF

MODE	MF	EDC1	EDC2
x16 non-mirrored	VSSQ	VSSQ	VDDQ
x32non-mirrored	VSSQ	VDDQ (terminated by the system or controller)	VDDQ (terminated by the system or controller)
x16 mirrored	VDDQ	VDDQ	VSSQ
x32 mirrored	VDDQ	VDDQ (terminated by the system or controller)	VDDQ (terminated by the system or controller)

NOTE : EDC1 is physically same as EDC2, EDC1 is logically renamed EDC2 when mirrored

13.4 Power-up Sequence



After power-up, boundary scan mode can be entered, however, after exiting, power-up is required to get into normal operation. Command and address ODT is initialized and x16/x32 mode is configured just after power-up.
In order to optimize the timing margins on the address bus, address training is necessary in high frequency, however, it can be skipped in low frequency.
By setting MRS, DRAM can be ready to initiate PLL and training modes such as WCK2CK training, Read training, and Write training. PLL can be operated while the phase between WCK and CK is aligned. The WCK2CK training sequence is mandatory in GDDR5 since it triggers the synchronization of read and write controllers. Before PLL is locked, the WCK2CK training sequence should not be completed. After WCK is aligned with CK, Read training and Write training can be done. After training, DRAM is ready for operation.
After power down exit with WCK off, WCK2CK training is required especially in high frequency, however WCK2CK training can be skipped in low frequency. After power down exit with WCK on, WCK2CK training may be required in high frequency, however in rather low frequency, it can be skipped and both Read and Write training can be skipped.

14. REGISTER DEFINITION

14.1 MRS General Table

GDDR5 specifies 10 Mode Registers to define the specific mode of operation. MR0 to MR8 and MR15 are defined as shown in the overview below MR table. MR9 to MR14 are not defined and may be used for vendor specific features. Reprogramming the Mode Registers will not alter the contents of the memory array.

All Mode Registers are programmed via the MODE REGISTER SET (MRS) command and will retain the stored information until they are reprogrammed or the device loses power. Mode Registers must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

No default states are defined for Mode Registers except when otherwise noted. Users therefore must fully initialize all Mode Registers to the desired values e.g. upon power-up.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0.Bit A12 is not used for any mode register programming as this address input is not defined for 512M and 1G densities.
Mode Registers Overview

	BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
MR0	0	0	0	0	0	0	Write Recovery(tWR)				TM	CAS Latency(CL)				Write Latency(WL)		
MR1	0	0	0	1	0	0	0	ABI	Write DBI	Read DBI	0	Cal updat e	Addr/Cmd Ter- mination		DATA Termination		Drive Strength	
MR2	0	0	1	0	0	0	Address/Command Termination offset			DQ/$\overline{\text{DBI}}$/WCK Termination offset			Pull Up Impedance Offset			Pull Down Impedance Offset		
MR3	0	0	1	1	0	0	Bank Group		WCK Termination		INFO		RDQS Mode	WCK 2CK	WCK23 Invert	WCK01 Invert	Self Refresh	
MR4	0	1	0	0	0	0	EDC1 3 Inv	WR CRC	RD CRC	CRC Read Latency		CRC Write Latency			EDC hold pattern			
MR5	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	LP3	LP2	0
MR6	0	1	1	0	0	0	VREFD offset Upper 2 Bytes (A to F)				VREFD offset Lower 2 Bytes (M to V)				VREFD	RFU	VREFD Merge	WCK PIN
MR7	0	1	1	1	0	0	0	0	0	0	Half VREFD	Temp. Sense	DQ pre- amble	WCK2 CK Auto- Sync	LF Mode	0	0	0
MR8	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EDC Hi-Z	WR EHF	CL EHF
MR11	1	0	1	1	0	0	PASR Row Segment Mask				PASR 2 Bank Mask							
MR15	1	1	1	1	0	0	RFU	ADT	MRA MF1	MRA MF0	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

14.2 Mode Register 0 (MR0)

Mode Register 0 controls operating modes such as Write Latency, CAS latency, Write Recovery and Test Mode as shown in MR0 table
The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=0, BA2=0 and BA3=0.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	Write Recovery(tWR)				TM	CAS Latency(CL)				Write Latency(WL)		

Write Recovery (tWR)

MR8 A1	A11	A10	A9	A8	tCK
0	0	0	0	0	RFU
0	0	0	0	1	5
0	0	0	1	0	6
0	0	0	1	1	7
0	0	1	0	0	8
0	0	1	0	1	9
0	0	1	1	0	10
0	0	1	1	1	11
0	1	0	0	0	12
0	1	0	0	1	13
0	1	0	1	0	14
0	1	0	1	1	15
0	1	1	0	0	16
0	1	1	0	1	17
0	1	1	1	0	18
0	1	1	1	1	19
1	0	0	0	0	20
1	0	0	0	1	21
1	0	0	1	0	22
1	0	0	1	1	23
.....					
1	1	0	1	0	30
1	1	0	1	1	31

CAS Latency(CL)

MR8 A0	A6	A5	A4	A3	tCK
0	0	0	0	0	RFU
0	0	0	0	1	RFU
0	0	0	1	0	RFU
0	0	0	1	1	RFU
0	0	1	0	0	9
0	0	1	0	1	10
0	0	1	1	0	11
0	0	1	1	1	12
0	1	0	0	0	13
0	1	0	0	1	14
0	1	0	1	0	15
0	1	0	1	1	16
0	1	1	0	0	17
0	1	1	0	1	18
0	1	1	1	0	19
0	1	1	1	1	20
1	0	0	0	0	21
1	0	0	0	1	22
1	0	0	1	0	23
1	0	0	1	1	24
1	0	1	0	0	25
1	0	1	0	1	26
1	0	1	1	0	27
1	0	1	1	1	TBD
1	1	0	0	0	TBD
.....					
1	1	1	1	1	TBD

*Write Latency(WL)

A2	A1	A0	tCK
0	0	0	RFU
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

***NOTE** : WL=1 can be supported only at below 1Gbps.

Test mode

A7	Test Mode
0	Normal
1	Testmode

***NOTE** : Please note that the MSB is located in Mode Register 8(MR8)
If user enables DBI on mode, CL should be increased by 2tCK more than nominal CL
1) 4.0Gbps should be set by CL = 16.
2) 4.0Gbps is CL=16 with DBI off and CL=17 with DBI on

[Table 7] Cas Latency(CL) according to data rate(speed bin)

Data Rate(Speed bin, VDD)	Cas Latency(CL)		CRC Latency		Unit
	DBI off mode	DBI on mode	CRCRL	CRCWL	
8.0Gbps (VDD=1.5V)	TBD	TBD	TBD	TBD	tCK
7.0Gbps (VDD=1.5V)	22	23	3	14	tCK
6.5Gbps (VDD=1.5V)	21	22	3	14	tCK
6.0Gbps (VDD=1.5V)	20	21	3	14	tCK
5.5Gbps (VDD=1.5V)	19	20	2	14	tCK
5.0Gbps (VDD=1.5V)	18	19	2	14	tCK
4.5Gbps (VDD=1.5V)	17	18	2	13	tCK
4.0Gbps (VDD=1.5V)	16	17	2	13	tCK
3.6Gbps (VDD=1.5V)	15	16	1	12	tCK
3.0Gbps (VDD=1.5V)	13	14	1	12	tCK
2.0Gbps (VDD=1.5V)	11	11	1	10	tCK
6.0Gbps (VDD=1.35V)	22	23	3	14	tCK
5.0Gbps (VDD=1.35V)	20	21	3	14	tCK
4.0Gbps (VDD=1.35V)	18	19	2	14	tCK
3.0Gbps (VDD=1.35V)	15	16	2	13	tCK
2.0Gbps (VDD=1.35V)	12	13	1	12	tCK

***NOTE** : User should set CL for each speed bin according to the above CL table.
ex) 4.0Gbps(DBI on) part could not be able to work at longer CL(ex. CL=18,19..) than CL=17

WRITE Latency (WLmrs)

The WRITE latency (WLmrs) is the delay in clock cycles used in the calculation of the total WRITE latency (WL) between the registration of a WRITE command and the availability of the first piece of input data. This specifications should be checked for value(s) of WLmrs supported. The full WRITE latency definition can be found in the section entitled OPERATION.

When the WRITE latencies are set to small values (i.e. 1,2,... clocks), the input receivers never turn off, in turn, raising the operating power. When the WRITE latency is set to higher values (i.e. .. 6, 7 clocks) the input receivers turn on when the WRITE command is registered. Refer to datasheet for value(s) of WLmrs where the input receivers are always on or only turn on when the WRITE command is registered.

CAS Latency (CLmrs)

The CAS latency (CLmrs) is the delay in clock cycles used in the calculation of the total READ latency (CL) between the registration of a READ command and the availability of the first piece of output data. By default CLmrs is specified by bits A3-A6, defining a CLmrs range of 9 to 20 tCK. For higher frequencies, the CLmrs range may optionally be expanded by the CLEHF bit located in Mode Register 8 (MR8). With the addition of the CLEHF bit a CLmrs range of 21 to 27 t_{CK} is defined. Please note that with the presence of the CLEHF bit a change of the CAS latency may require two MRS commands.This specifications should be checked for value(s) of CLmrs supported. The full READ latency definition can be found in the section entitled OPERATION.

WRITE Recovery (WR)

The programmed WR value is used for the auto precharge feature along with tRP to determine tDAL. The WR register bits are not a required function and may be implemented at the discretion of the DRAM manufacturer.
WR must be programmed with a value greater than or equal to RU{tWR/tCK}, where RU stands for round up, tWR is the analog value from the datasheet and tCK is the operating clock cycle time.
By default WR is specified by bits A8-A11, defining a WR range of 5 to 19 t_{CK}.

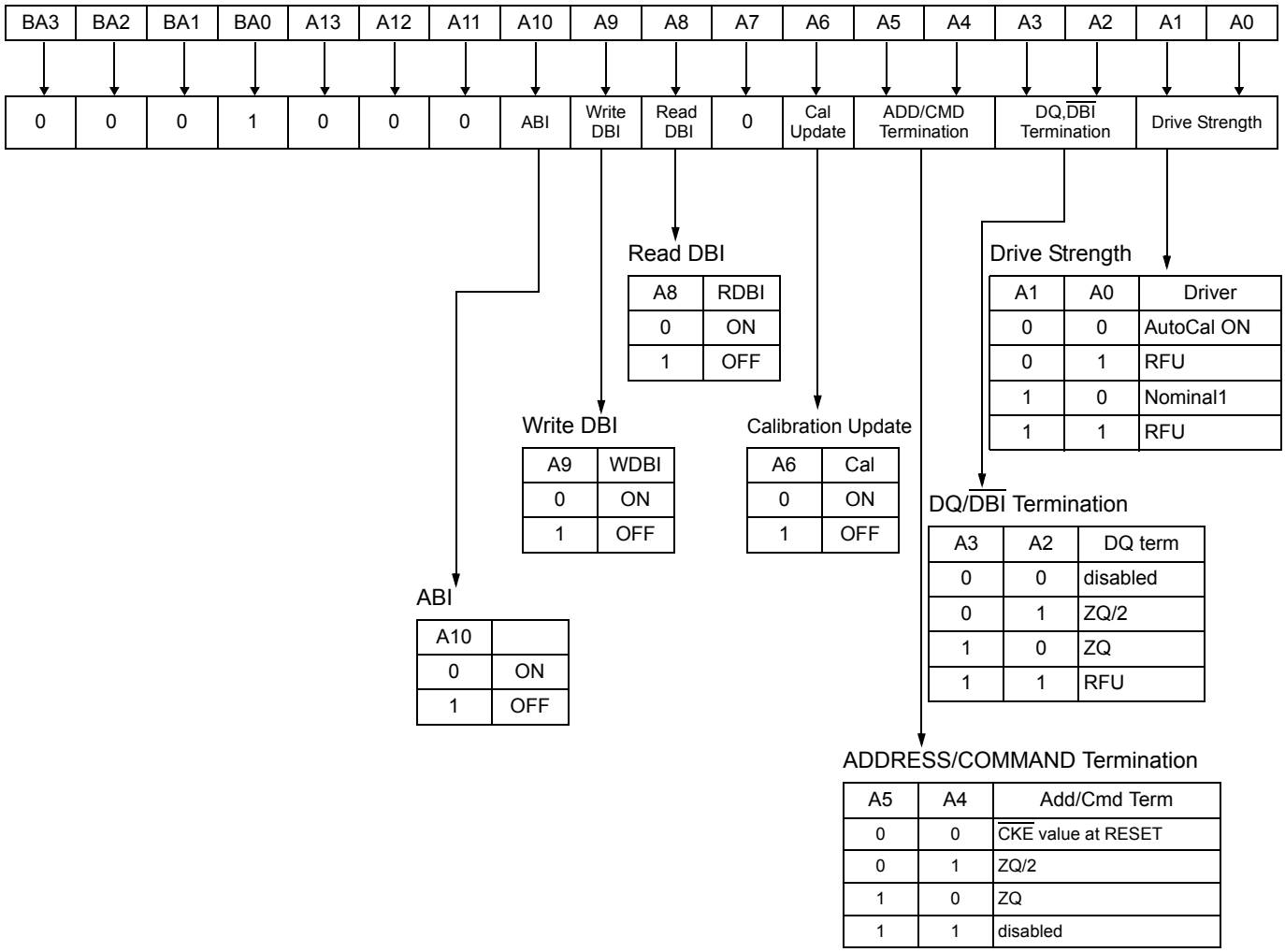
For higher frequencies, the WR range may optionally be expanded by the WREHF bit located in Mode Register 8 (MR8). With the addition of the WREHF bit a WR range of 20 to 31 t_{CK} is defined. Please note that with the presence of the WREHF bit a change of the WRITE Recovery may require two MRS commands.

Test Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A7 set to '0', and bits A0-A6 and A8-A11 set to the desired values. Programming bit A7 to '1' places the device into a test mode that is only to be used by the DRAM manufacturer. No functional operation is specified with test mode enabled.

14.3 Mode Register 1 (MR1)

Mode Register 1 controls functions like drive strength, data termination, address/command termination, Read DBI, Write DBI, ABI, control of calibration updates and PLL/DLL as shown in MR1 table.
The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=0, BA2=0 and BA3=0. Bits A0-A1, A4-A6 and A10 of this register are initialized with '0's.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.



Read DBI

A8	RDBI
0	ON
1	OFF

Drive Strength

A1	A0	Driver
0	0	AutoCal ON
0	1	RFU
1	0	Nominal1
1	1	RFU

Write DBI

A9	WDBI
0	ON
1	OFF

Calibration Update

A6	Cal
0	ON
1	OFF

DQ/$\overline{DBI}$ Termination

A3	A2	DQ term
0	0	disabled
0	1	ZQ/2
1	0	ZQ
1	1	RFU

ABI

A10	
0	ON
1	OFF

ADDRESS/COMMAND Termination

A5	A4	Add/Cmd Term
0	0	$\overline{CKE}$ value at RESET
0	1	ZQ/2
1	0	ZQ
1	1	disabled

NOTE 1: Nominal pull up/pull down resistance is 60ohm/40ohm.

Impedance Autocalibration of Output Buffer and Active Terminator

GDDR5 SGRAMs offer autocalibrating impedance output buffers and on-die terminations. This enables a user to match the driver impedance and terminations to the system within a given range. To adjust the impedance, an external precision resistor is connected between the ZQ pin and VSSQ A nominal resistor value of 120 Ohms is equivalent to the 40 Ohms Pull-down and 60 Ohms Pull-up nominal impedances of GDDR5 SGRAMs. $\overline{\text{RESET}}$, CK and $\overline{\text{CK}}$ are not internally terminated. CK and $\overline{\text{CK}}$ shall be terminated on the system using external 1% resistors to VDDQ.
The output driver and on-die termination impedances are updated during all REFRESH commands to compensate for variations in supply voltage and temperature. The impedance updates are transparent to the system.

Driver Strength

Bits A0 and A1 define the driver strength. The Auto Calibration setting enables the Auto-Calibration functionality for the Pull-down, Pull-up and Termination over process, temperature and voltage changes. The design target for the factory setting is 40 Ohm Pull-down, 60 Ohm Pull-up driver strength with nominal process, voltage and temperature conditions.The nominal option enables the factory setting for the Pull-down, Pull-up driver strength and termination. With this option enabled, driver strength and termination are expected to change with process, voltage and temperature. AC timings are only guaranteed with Auto Calibration.

Data/$\overline{\text{DBI}}$ Termination

Bits A2 and A3 define the data termination value for the on-die termination (ODT) for the DQ and $\overline{\text{DBI}}$ pins in combination with the driver strength setting. The termination can be set to a value of ZQ/2 which is intended for a single loaded system, or ZQ which is intended for a weaker termination used in a lower power or frequency applications. The data termination may also be turned off.

ADR/CMD Termination

Bits A4 and A5 define the address/command termination. The default setting ('00') provides that the address/command termination is determined by latching $\overline{\text{CKE}}$ on the rising edge of $\overline{\text{RESET}}$.
The address/command termination can also be set to a value of ZQ/2 which is intended for a single loaded system, or ZQ which is intended for double loaded configurations with two devices sharing a common address/command bus. The address/command termination may also be turned off.

Calibration Update

The Calibration Update setting enables the calibration value to be updated automatically by the auto calibration engine. The function is enabled upon power-up to reduce update induced jitter. The user may decide to suppress updates from the auto calibration engine by disabling Calibration Update (A6=1).
The calibration updates can occur with any REFRESH command. The update is not complete for a time tKO after the latching of the REFRESH command. During this tKO time, only NOP or DESELECT commands may be issued.

RDBI and WDBI

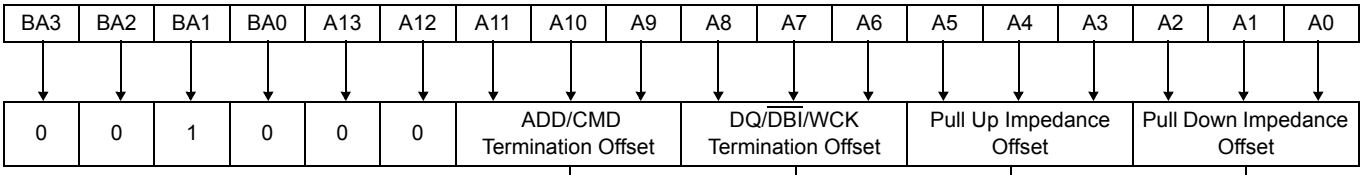
Bit A8 controls Data Bus Inversion (DBI) for READs (RDBI), and bit A9 controls Data Bus Inversion for WRITEs (WDBI). For more details on DBI see READ and WRITE Data Bus Inversion (DBI) in the section entitled OPERATION.

ABI

Address Bus Inversion (ABI) is selected independently from DBI using bit A10. When enabled any data sent over the address bus (whether opcode, addresses, LDFF data or DM) is inverted or not inverted based on the state of $\overline{\text{ABI}}$ signal. For more details on ABI see Address Bus Inversion (ABI) in the section entitled OPERATION.

14.4 Mode Register 2 (MR2)

Mode Register 2 defines the output driver (OCD) and termination offsets as shown in MR2 table. Mode Register 2 is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=1, BA2=0 and BA3=0.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.



DQ/DBI/WCK Termination Offset

A8	A7	A6	Steps
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

Pull Down Impedance Offset

A2	A1	A0	Steps
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

ADD/CMD Termination Offset

A11	A10	A9	Steps
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

Pull Up Impedance Offset

A5	A4	A3	Steps
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

Impedance Offsets

The driver and termination impedances may be offset individually for PD driver, PU driver, DQ/DBI/WCK termination and address/command termination. The offset impedance step values may be non-linear and will vary across PVT. With negative offset steps the drive strengths will be decreased and Ron will be increased. With positive offset steps the drive strengths will be increased and Ron will be decreased. With negative offset steps the termination value will be increased. With positive offset steps the termination value will be decreased. IV curves and AC timings are only guaranteed with zero offset.

14.5 Mode Register 3 (MR3)

Mode Register 3 controls functions including Bank Groups, WCK termination, self refresh, RDQS mode, DRAM Info and WCK2CK training as shown in MR3 table. Mode Register 3 is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=1, BA2=0 and BA3=0.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	Bank Group		WCK Termination		Information		RDQS mode	WCK2 CK	WCK23 invert	WCK01 invert	Self Refresh	

Bank Groups

A11	A10	Bank Group
0	0	OFF (tCCDL= tCCDS)
0	1	
1	0	ON (tCCDL=4tCK)
1	1	ON (tCCDL=3tCK)

WCK Termination

A9	A8	WCK term
0	0	disabled
0	1	ZQ/2
1	0	ZQ
1	1	RFU

Self Refresh

A1	A0	Self Refresh
0	0	32ms
0	1	RFU
1	0	RFU
1	1	Temperature Controlled

Information

A7	A6	Info
0	0	OFF
0	1	Vendor ID
1	0	Temperature Read out/ opt.
1	1	RFU

WCK01 Invert

A2	WCK01 Invert
0	OFF
1	ON

WCK23 Invert

A3	WCK23 Invert
0	OFF
1	ON

WCK2CK

A4	WCK2CK
0	OFF
1	ON

RDQS Mode

A5	RDQS mode
0	OFF
1	ON

Self Refresh
The refresh interval in self refresh mode may be set to 32ms.

WCK2CK
Bit A4 (WCK2CK) enables and disables the WCK2CK alignment training. For details on this training sequence, see the section on TRAINING.

WCK01 / WCK23 Inversion
Bits A2 and A3 control whether the internal phase of the WCK01 and WCK23 clock inputs after internal divide-by-2 shall be inverted, corresponding to a 2 U.I. phase shift. The bits are used in conjunction with WCK2CK training mode.

RDQS Mode
Bit A5 enables the RDQS mode of the GDDR5 SGRAM. In this mode the EDC pins will act as a READ strobe (RDQS). No CRC is supported in RDQS mode, and all related bits in MR4 will be ignored. A detailed description of the RDQS mode can be found in the section entitled OPERATION.

DRAM Info
Bits A6 and A7 enable the DRAM Info mode which is provided to output the Vendor ID, or optionally the current junction temperature or other vendor specific device info. The Vendor ID identifies the manufacturer of the GDDR5 SGRAM, and provides the die revision, memory density and FIFO depth.
The temperature readout provides the SGRAM's junction temperature. Vendors may require that the related on-chip temperature sensor being enabled in advance by bit A6 in MR7.

WCK Termination
Bits A8 and A9 define the termination value for the on-die termination (ODT) for the WCK01, $\overline{\text{WCK01}}$, WCK23 and $\overline{\text{WCK23}}$ pins in combination with the driver strength setting. The termination can be set to a value of ZQ/2 which is intended for a single loaded system, or ZQ which is intended for double load configurations with two devices sharing the WCK clocks. The WCK termination may also be turned off.

Bank Groups(BG)
Bit A11 enables the bank groups feature, and bit A10 specifies the min column-to-column command delay (tCCDL). With A11 set to '1', back-to-back column accesses within a bank group have to be spaced by 3 or 4 clocks as defined by bit A10, with 3 tCK being optional. With A11 set to '0', the bank groups feature is disabled and tCCDL equals tCCDS.

The datasheet specifies the operating frequency limit below which the user may run the device without activating the bank groups feature.(fCKBG)

14.6 Mode Register 4 (MR4)

Mode Register 4 defines the Error Detection Code (EDC) features of GDDR5 SGRAMs as shown in MR4 table.
The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=0, BA2=1 and BA3=0. Bits A0-A3 (EDC Hold Pattern) of this register are initialized with'1111'
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	EDC13 Inv	WR CRC	RD CRC	CRC Read Latency		CRC Write Latency			EDC Hold Pattern			

EDC13 Inv

A11	EDC13 Invert
0	OFF(Hold pattern of EDC1 /EDC3 not inverted)
1	ON (Hold pattern of EDC1 /EDC3 inverted)

Write CRC

A10	Write CRC
0	ON
1	OFF (Hold Pattern)

Read CRC

A9	Read CRC
0	ON
1	OFF (Hold Pattern)

EDC Hold Pattern

A3	A2	A1	A0	
0	0	0	0	Pattern
0	0	0	1	Pattern
0	0	1	0	Pattern
0	0	1	1	Pattern
0	1	0	0	Pattern
		. . .		
1	1	1	1	Pattern

Burst3 Burst2 Burst1 Burst0

CRC Read Latency (CRCRL)

A8	A7	CRCRL
0	0	0
0	1	1
1	0	2
1	1	3

CRC Write Latency (CRCWL)

A6	A5	A4	CRCWL
0	0	0	7
0	0	1	8
0	1	0	9
0	1	1	10
1	0	0	11
1	0	1	12
1	1	0	13
1	1	1	14

EDC Hold pattern / EDC13 Invert

The 4-bit EDC hold pattern is considered a background pattern transmitted on the EDC pins. The register is initialized with all '1's. The pattern is shifted from right to left and repeated with every clock cycle. The output timing is the same as of a READ burst. CRC bursts calculated from WRITEs or READs will replace the EDC hold pattern for the duration of those bursts, provided CRC is enabled for those bursts. With each MRS command to MR4 that changes bits A0-A3 or A9-A11, the EDC hold pattern will be undefined for tMRD. The EDC hold pattern will not be transmitted when the device is in address training mode, in WCK2CK training mode, in RDQS mode, in self refresh mode, in reset state, in power-down state with the LP2 bit set, or in scan mode. With register bit A11 set High, EDC1 and EDC3 will transmit the inverted EDC hold pattern, resulting in a pseudo-differential pattern. Please note that this function is not available in x16 configuration. Bit A11 is ignored for READ, WRITE and RDTR CRC bursts and the clock phase information in WCK2CK training mode.

CRC Write Latency (CRCWL)

The values of the CRC write latency is loaded into register bits A4-A6. The actual CRC write latency is denoted as EDCWL. EDCWL = WL + CRCWL.

CRC Read Latency (CRCRL)

The values of the CRC read latency is loaded into register bits A7-A8. The actual CRC read latency is denoted as EDCRL. EDCRL = RL + CRCRL.

Read CRC

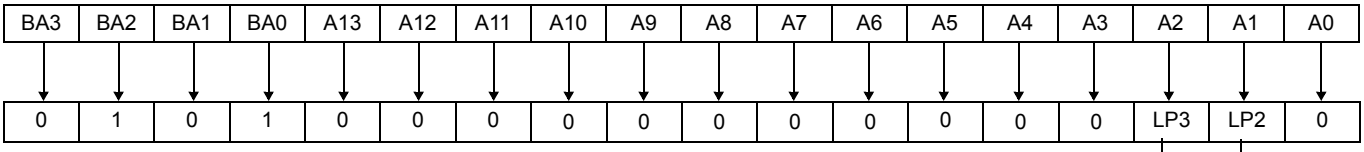
Bit A9 controls the CRC calculation for READ bursts. When enabled, the calculated CRC pattern will be transmitted on the EDC pins with the latency as programmed in the CRCRL field of this register. With Read CRC being off, no CRC will be calculated for READ bursts, and the EDC hold pattern will be transmitted instead.

Write CRC

Bit A10 controls the CRC calculation for WRITE bursts. When enabled, the calculated CRC pattern will be transmitted on the EDC pins with the latency as programmed in the CRCWL field of this register. With Write CRC being off, no CRC will be calculated for WRITE bursts, and the EDC hold pattern will be transmitted instead.

14.7 Mode Register 5 (MR5)

Mode Register 5 defines digital RAS, PLL band-width and low power modes as shown in MR5 table. The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=0, BA2=1 and BA3=0.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.



LP2(optional)

A0	LP2
0	Off
1	On / optional

LP3(0ptional)

A0	LP3
0	Off
1	On

Low Power Modes (LP2, LP3)

Bits A0-A2 control several low power modes of the GDDR5 SGRAM. The modes are independent of each other. LP2 are optional features. When bit A1 (LP2) is set, the WCK receivers may be turned off during power-down. When bit A2 (LP3) is set, RDTR, WRTR and LDFF commands are not allowed while a REF command is being executed.

14.8 Mode Register 6 (MR6)

Mode Register 6 controls the WCK2CK alignment point and defines VREFD related features such as source, level, offsets, VREFD Merge and VREFD Auto Calibration mode, as shown in MR6 table. The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=1, BA2=1 and BA3=0.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	VREFD offset Upper 2 bytes				VREFD offset Lower 2 bytes				VREFD	0	VREF Merge	0

VREFD offset Upper 2Bytes (Rows A to F)

A11	A10	A9	A8	Steps
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	RFU
1	0	0	1	-7
1	0	1	0	-6
1	0	1	1	-5
1	1	0	0	-4
1	1	0	1	-3
1	1	1	0	-2
1	1	1	1	-1

VREFD offset Lower 2Bytes (Rows M to V)

A7	A6	A5	A4	Steps
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	RFU
1	0	0	1	-7
1	0	1	0	-6
1	0	1	1	-5
1	1	0	0	-4
1	1	0	1	-3
1	1	1	0	-2
1	1	1	1	-1

VREFD

A3	VREFD
0	External Pin
1	Internal VREFD

VREF Merge

A1	Vref Merge
0	NO
1	YES

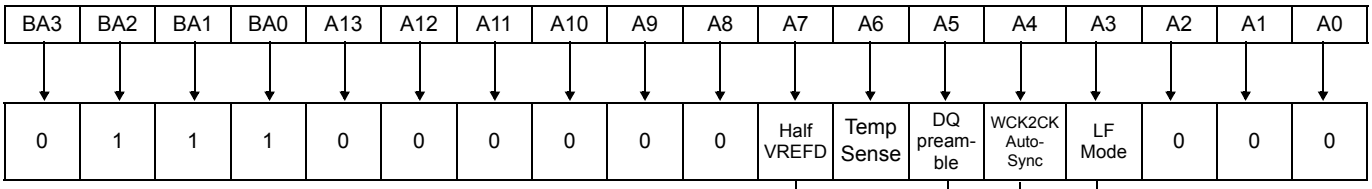
VREFD Merge
The VREFD Merge mode is enabled when bit A1 is set to '1'. The externally supplied VFRED and the internally generated Vref will be merged, resulting in the average value of both. This specifications should be checked for values of external resistors that may be connected to VREFD pins in this VREF Merge mode.

VREFD
Bit A3 selects between external and internal Vref. The bit is "Don't Care" when VREF Merge mode is selected.

VREFD Offsets
When using internal VREFD, VREFD offset mode is used to offset VREFD independently for the upper 2bytes and the lower 2bytes. The offset step values may be non-linear and will vary across PVT. When half VREFD is used, VREFD offset functionality is not supported.

14.9 Mode Register 7 (MR7)

Mode Register 7 controls features like PLL Standby, PLL Fast-Lock, PLL Delay Compensation, Low Frequency mode, Auto Synchronization, Data Preamble, and Half VREFD as shown in MR7 table. The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=1, BA2=1 and BA3=0.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.



Half VrefD

A7	Half VREFD
0	0.7*VDDQ
1	0.5*VDDQ

WCK2CK Automatic Synchronization

A4	WCK2CK Auto-Sync
0	NO
1	YES

DQ Preamble

A5	DQ Preamble
0	NO
1	YES

Low Frequency Mode

A3	LF Mode
0	High Frequency (over 2Gbps)
1	Low Frequency (under 2Gbps)

NOTE : User should change LF mode MRS set according the operation frequency

Low Frequency Mode

When Low Frequency Mode is enabled by bit A3, the clock tree is changed for low frequency operation.
User should enabled Low Frequency Mode when operating at lower than 2Gbps.

WCK2CK Auto Synchronization

GDDR5 SGRAMs may optionally support a WCK2CK automatic synchronization mode that eliminates the need for WCK2CK training upon power-down exit or for reducing WCK2CK training time at low frequency. This mode is controlled by bit A4. For a detailed description see WCK2CK Auto Synchronization in the section entitled WCK2CK
Training.

Data Preamble

When enabled by bit A5, non-gapless READ bursts will be preceded by a fixed data preamble on the DQ and $\overline{\text{DBI}}$ pins of 4 U.I. duration. The programmed READ latency does not change when the Data Preamble is enabled. The pattern is not encoded with RDBI, however, if RDBI is disabled, the $\overline{\text{DBI}}$ pins will not toggle and drive a HIGH.

Half VREFD

This optional mode allows users to adjust the Vref level in case the GDDR5 SGRAM is operated without termination: when bit A7 is set to '1', a Vref level of nominally 0.5 * VDDQ is expected at the VREFD pin or being generated internally

Temperature Sensor

The optional on-chip temperature sensor is enabled by bit A6. DRAM vendor may also have the on-chip temperature sensor enabled permanently; in this case bit A6 is "Don't care". A detailed description of the Temperature Sensor can be found in the VENDOR ID, TEMP SENSOR and SCAN section.

14.10 Mode Register 8 (MR8)

Mode Register 8 defines extensions to CAS latency(CLmrs) and Write Recovery (WR) as shown in below table. The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=0, BA2=0 and BA3=1.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EDC Hi-Z	WR EHF	CL EHF

A2	EDC Hi-Z
0	legacy
1	High Z condition

WR EHF mode

A1	WRITE Recovery Extra high Frequency
0	WR normal range (5 to 19tCK)
1	WR extended range (20 to 31tCK)

CL EHF mode

A0	CAS Latency Extra high Frequency
0	CLmrs normal range (7 to 20tCK)
1	CLmrs extended range (21 to 31tCK)

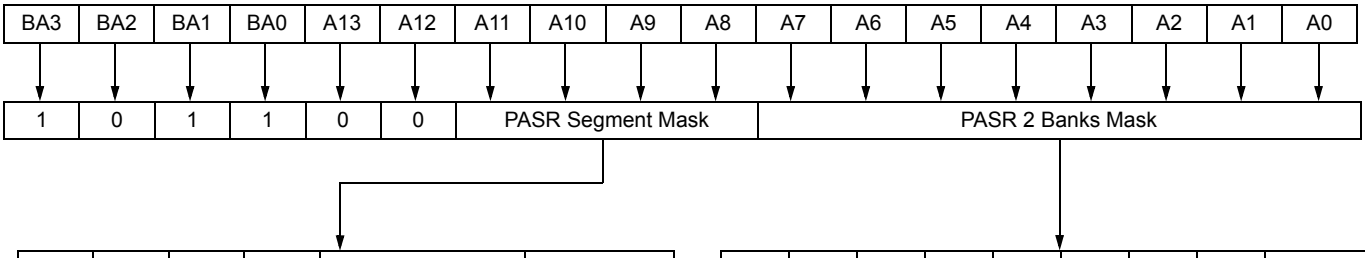
CAS Latency Extra high Frequency(CLEHF)
CAS Latency Extra High Frequency (CLEHF) Bits A0 extends the CLmrs (CAS latency) field in MR0 from 4 bits to 5 bits. See Mode Register 0 for more details.

WRITE Recovery Extra High Frequency(WREHF)
Bits A1 extends the WR(WRITE Recovery) field in MR0 from 4 bits to 5 bits. See Mode Register 0 for more details. WREHF is optional.

EDC Hi-Z
GDDR5 DRAM support an optional feature, selectable by a mode register, to override the legacy behavior of the EDC pin that is required for normal operation and instead set the output pad into a High-Z state. The EDC High-Z control is provided on MR8[A2]. With A2 = 0, this feature is off. With bit A2 set to 1, the EDC pins are High-Z state. The EDC High-Z function takes precedence over all other features that define the EDC pin's data pattern.

14.11 Mode Register 11 (MR11)

Mode Register 11 defines PASR(Partial Array Self Refresh) as shown in below table. The register is programmed via the MODE REGISTER SET(MRS) command with BA0=1, BA1=1, BA2=0, BA3=1.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

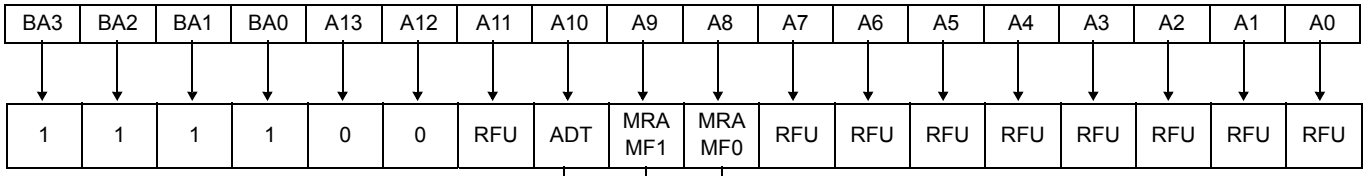


A11	A10	A9	A8	Segment Masked	8Gb R13:12
0	0	0	1	0 segment	00
0	0	1	0	1 segment	01
0	1	0	0	2 segment	10
1	0	0	0	3 segment	11

A7	A6	A5	A4	A3	A2	A1	A0	2 Banks Masked
0	0	0	0	0	0	0	1	Bank 0 & 1
0	0	0	0	0	0	1	0	Bank 2 & 3
0	0	0	0	0	1	0	0	Bank 4 & 5
0	0	0	0	1	0	0	0	Bank 6 & 7
0	0	0	1	0	0	0	0	Bank 8 & 9
0	0	1	0	0	0	0	0	Bank 10 & 11
0	1	0	0	0	0	0	0	Bank 12 & 13
1	0	0	0	0	0	0	0	Bank 14 & 15

14.12 Mode Register 15 (MR15)

Mode Register 15 controls address training mode (ADT) and access to Mode Registers 0 to 14 (MRE) as shown in MR15 table. The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=1, BA2=1 and BA3=1. Mode Register 15 is a special register that operates in SDR addressing mode. Increased setup and hold times as for command inputs are assumed to ensure the MRS command to this register is successful while address training (ADT) has not taken place and the integrity of DDR addresses may not be guaranteed. This is indicated by setting bits A0-A7 to Don't Care ("X") which are paired with the usable bits (A8-A11) and the Mode Register address (BA0-BA3).
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.



BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	0	0	RFU	ADT	MRA MF1	MRA MF0	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

Address Training

A10	ADT
0	OFF
1	ON

MR0 ~13 Access MF=1

A9	MR0~14 Access MF =1
0	Enabled
1	Disabled

MR0 ~13 Access MF=0

A8	MR0~14 Access MF =0
0	Enabled
1	Disabled

Address pairs:

Rising CK	BA3	BA2	BA1	BA0	A11	A10	A9	A8
Rising $\overline{CK}$	A3	A4	A5	A2	A6	A0	A1	A7

Address Training
Address training mode is enabled and disabled with bit A10.

Mode Register 0-14 Enable
When disabled by bit A8 (for SGRAMs configured to MF=0) or bit A9 (for SGRAMs configured to MF=1), the GDDR5 SGRAM will ignore any MODE REGISTER SET command to Mode Registers 0 to 14. If enabled, MODE REGISTER SET commands function as normal. MODE REGISTER SET commands to Mode Register 15 (this register) are not affected and will always be executed. This functional allows for individual configuration of two GDDR5 SGRAMS on a common address bus without the use of a $\overline{CS}$ pin.

15. Manufacturer's Vendor Code, Revision Identification, Density, Fifo Depth

Manufacturer can be identified by issuing MRS which generates vendor ID on the DQ bus. Revision ID can also be retrieved by the same command. The density and FIFO depth of the DRAM can also be driven on the DQ bus. Users can adapt their own control to the DRAM configuration. The information of FIFO depth is very critical in Read/Write training

Functional description
- The VID will be driven onto the DQ bus after the MRS command sets MR3 A7 to 0 and A6 to 1.
- DBI is not entered or ignored during all Vendor ID operations.
- The DQ bus will be continuously driven until an MRS command sets MR3 A7 and A6 back to 0.
- The DQ bus will be in ODT state after tWRIDOFFmax.
- The code can be sampled by the controller after waiting tWRIDONmax and before tWRIDOFFmin.
- 16bits sent on Byte 0 and 2 in x32 and x16 MF=0
- 16bits sent on Byte 1 and 3 for x16/32 MF=1

AC Timing Parameters

Parameter	Min	Max
tWRIDON	-	10ns
tWRIDOFF	-	10ns

MF=0	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
MF=1	DQ24	DQ25	DQ26	DQ27	DQ28	DQ29	DQ30	DQ31
Feature	Vendor ID				Revision ID			
	1	0	0	0	0	1	0	0

NOTE : When MF=0, byte0 is used for information. When MF=1, byte3 is used for information. It does not change physical location but logical name.

MF=0	DQ16	DQ17	Density	DQ18	DQ19	FIFO Depth	DQ20	DQ21	DQ22	DQ23
MF=1	DQ8	DQ9	Density	DQ10	DQ11	FIFO Depth	DQ12	DQ13	DQ14	DQ15
Feature	Density		-	FIFO Depth		-	RFU			
0	0	0	8G	0	1	6	1	0	0	0

NOTE : When MF=0, byte2 is used for information. When MF=1, byte1 is used for information. It does not change physical location but logical name.

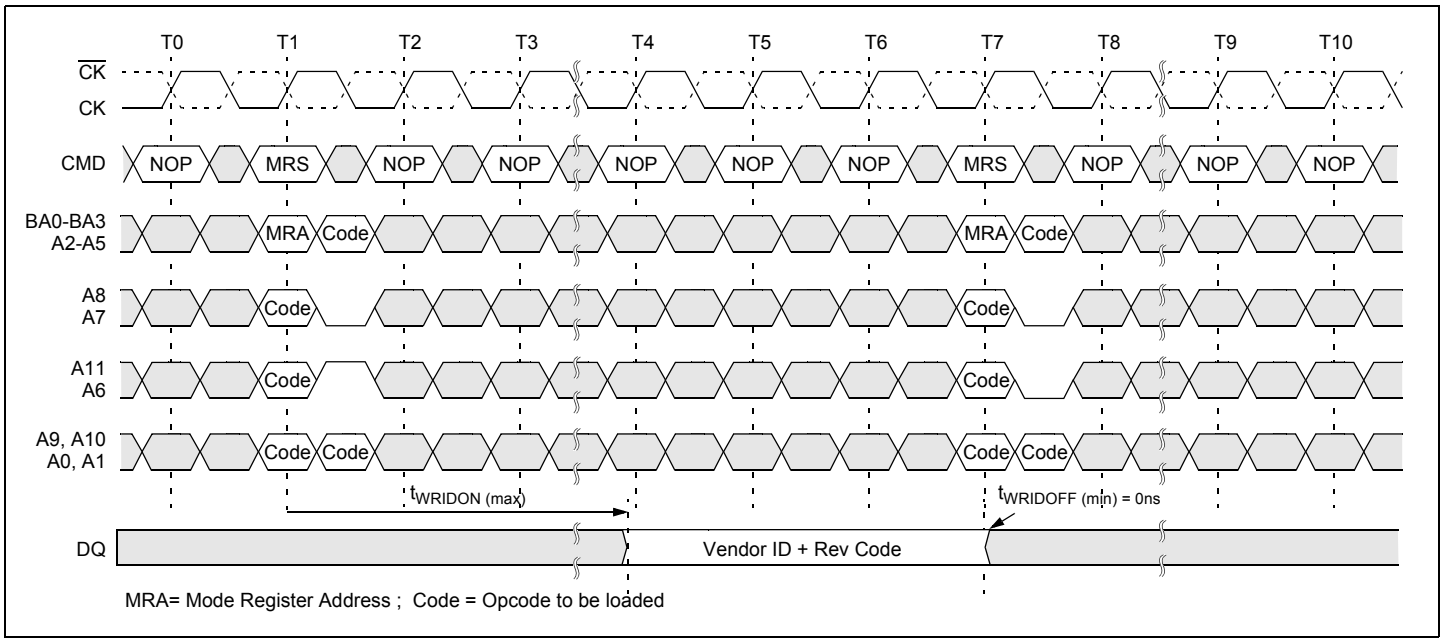


Figure 8. Vendor ID

16. TRAINING

16.1 Interface Training Sequence

Due to the high data rates of GDDR5, it is recommended that the interfaces be trained to operate with the optimal timings. GDDR5 SGRAM has features defined which allow for complete and efficient training of the I/O interface without the use of the GDDR5 SGRAM array. The interface trainings are not required for normal DRAM functionality, however interface timings will only be guaranteed after all required trainings have been executed.

A recommended order of training sequences has been chosen based on the following criteria:

The address training must be done first to allow full access to the mode registers. (MRS for address training is a special single data rate mode register set guaranteed to work without training). Address input timing shall function without training as long as tAS/H are met at the GDDR5 SGRAM.

WCK2CK training should be done before read training because a shift in WCK relative CK will cause a shift in all READ timings relative to CK.

READ training should be done before WRITE training because optimal WRITE training depends on correct READ data.

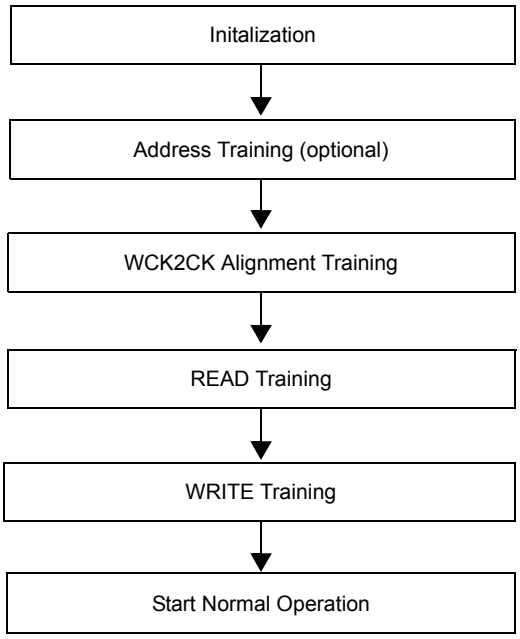
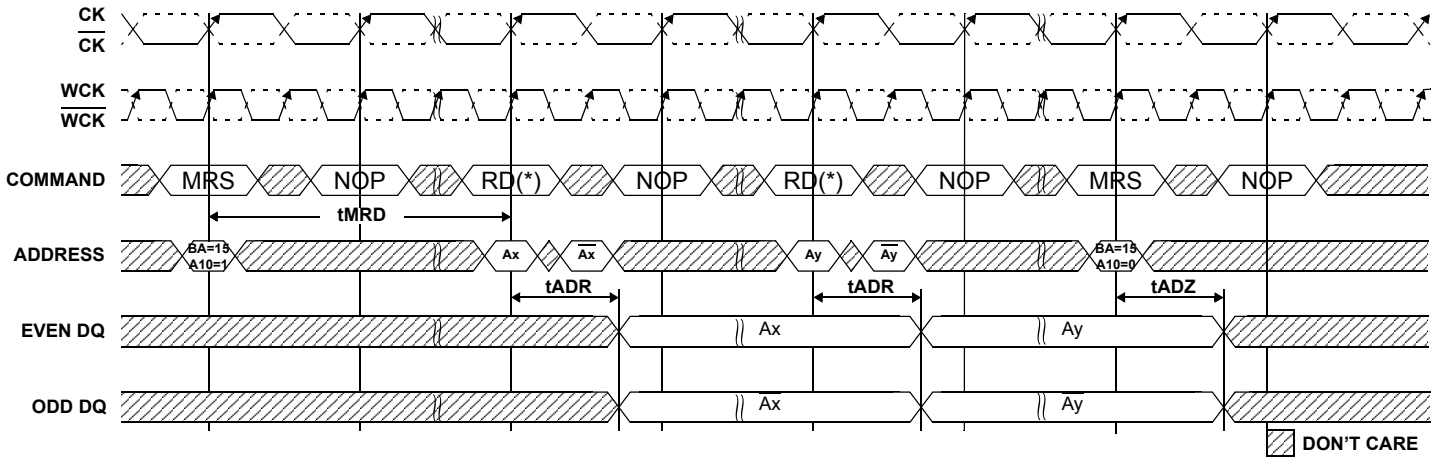


Figure 9. Interface Training Sequence

16.2 Address Training

The GDDR5 SGRAM provides means for address bus interface training. The controller may use the address training mode to improve the timing margins on the address bus. Address training mode is entered and exited via the ADT bit in Mode Register 15 (MR15). Address training mode uses an internal bridge between the GDDR5 SGRAM's address inputs and DQ/$\overline{DBI}$ outputs. It also uses a special READ command for address capture that is encoded using the SDR command pins only ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = L,H,L,H). The address values normally used to encode the commands will not be interpreted. Once the address training mode has been entered, the address values registered coincident with this special READ command will be transmitted to the controller on the DQ/$\overline{DBI}$ pins. The controller is then expected to compare the address pattern received to the expected value and to adjust the address transmit timing accordingly. The procedure may be repeated using different address pattern and interface timings. No WCK clock is required for this special READ command operation during address training mode. The latched addresses are driven out asynchronously. The only commands allowed during address training mode are this special READ, MRS (e.g. to exit address training mode) and NOP / DESELECT.

When enabled by the ABI bit in Mode Register 1, address bus inversion (ABI) is effective during address training mode. It is suggested to train the $\overline{ABI}$ pin's interface timing together with the other address lines.The timing diagram in the following Figure illustrates the typical command sequence in address training mode. The DQ/$\overline{DBI}$ output drivers are enabled as long as the ADT bit is set. The minimum spacing between consecutive special READ commands is 2 tCK.



NOTE :
1) READ command encoding: $\overline{CS}$=L, $\overline{RAS}$=H, $\overline{CAS}$=L, $\overline{WE}$=L
2) Ax = 1st half of address x sampled on rising edge of CK/$\overline{CK}$;
   $\overline{Ax}$ = 2nd half of address x, sampled on falling edge of CK/$\overline{CK}$.
3) Addresses sampled on rising edge of CK are sent back on even DQ after tADR;
   Addresses sampled on falling edge of CK are sent back on odd DQ simultaneously with addresses sent on even DQ.
4) DQs are enabled when ADT bit in MR15 set to 1 (Enter address training mode)
   DQs are disabled after tADZ when ADT bit in MR15 set to 0 (Exit address training mode)

Figure 10. Address Training

[Table 8] AC Timings in Address Training Mode

Parameter	Symbol	Min	Max	Unit
READ command to data out delay	tADR	-	2tCK+10ns	ns
ADT off to DQ in High-Z delay	tADZ	-	1tCK+10ns	ns

NOTE : High-Z could be terminated to VDDQ or unterminated

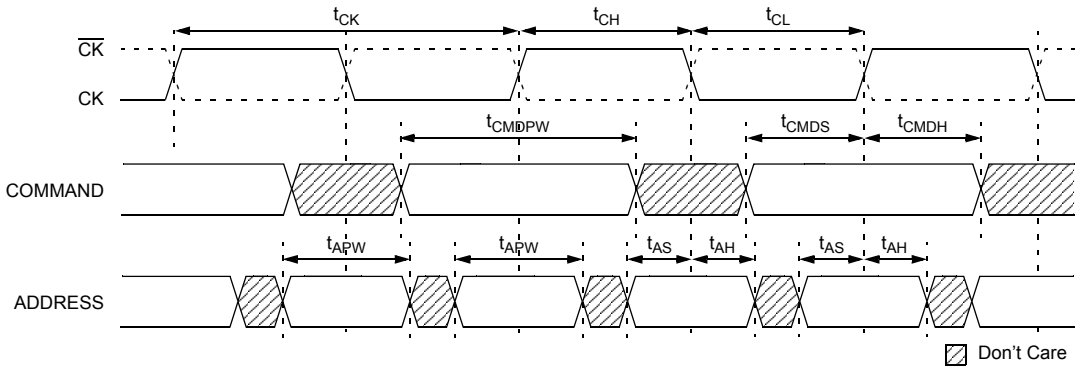


Figure 11. Command and Address Input Timing

The following table defines the correspondence between address bits and DQ/$\overline{DBI}$. Devices configured to x16 mode reflect the address on the two bytes being enabled in that mode, which are bytes 0 and 2 for MF=0 and bytes 1 and 3 for MF=1 configurations. Devices configured to x32 mode reflect the address on the same DQ as in x16 mode; in addition they are allowed but not required to reflect the address on those bytes that are disabled in x16 mode, thus reflecting each address twice.

[Table 9] GDDR5 SGRAM Address to DQ Mapping in Address Training Mode

Output	Address bits registered at rising edge of CK								
	A12	A8	A11	BA1	BA2	BA3	BA0	A9	A10
DQ	$\overline{DBI0}$	DQ22	DQ20	DQ18	DQ16	DQ6	DQ4	DQ2	DQ0
	$\overline{DBI1}$	DQ30	DQ28	DQ26	DQ24	DQ14	DQ12	DQ10	DQ8

Output	Address bits registered at rising edge of $\overline{CK}$								
	A13	A7	A6	A5	A4	A3	A2	A1	A0
DQ	$\overline{DBI2}$	DQ23	DQ21	DQ19	DQ17	DQ7	DQ5	DQ3	DQ1
	$\overline{DBI3}$	DQ31	DQ29	DQ27	DQ25	DQ15	DQ13	DQ11	DQ9

16.3 WCK2CK Training

The purpose of WCK2CK training is to align the data WCK clock with the command CK clock to aid in the GDDR5 SGRAM's internal data synchronization between the logics clocked by CK/$\overline{CK}$ and WCK/$\overline{WCK}$. This will help to define both Read and Write latencies between the GDDR5 SGRAM and memory controller. WCK2CK training mode is controlled via MRS.

Before starting WCK2CK training, the following conditions must be met:
• CK/$\overline{CK}$ clock is stable and toggling
• All address and command pin timing must be guaranteed.
• PLL on/off(MRS1 bit A7) and PLL delay compensation enable(MRS7 bit A2) are set to desired values before WCK to CK training is started
• The desired WCK2CK alignment point (MR6, bit A0) is selected by the proper value
• The EDC hold pattern (MR4, bits A0-A3) must be programmed to '1111'
• 2 Mode Register bits for internal WCK01 and WCK23 inversion (MR3, bits A2-A3) must be set to a known state
• All banks are idle and no other command execution is in progress

WCK2CK training must be done after any of the following conditions:
• Device initialization
• Any CLmrs, WLmrs, CRCRL or CRCWL latency change
• CK and WCK frequency changes
• PLL on/off(MRS1 bit A7) and PLL delay compensation mode(MRS7 bit A2) changes
• Change of the WCK2CK alignment point (MR6, bit A0)
• WCK state change from off to toggling, including self refresh exit or exit from power down when bit A1(LP2) in MR5 is set

Figure 12 and Figure 13 show example WCK2CK training sequences. WCK2CK training is entered via MRS by setting bit A4 in MR3. This will initiate the WCK divide-by-2 circuits associated with WCK01 and WCK23 clocks in the GDDR5 SGRAM. In case the divide-by-2 circuits are at opposite output phase, which is indicated by opposite "early/late" phases on the EDC pins associated with WCK01 and WCK23 (see below), they may be put in phase by using the WCK01 and WCK23 inversion bits. Alternatively, the WCK clocks may be put into a stable inactive state for this initialization event to aid in resetting all dividers to the same output phase as shown in Figure 13. The challenge of this method is to restart the WCK clocks in a way that even their first clock edges meet the WCK clock input specification. Otherwise, divide-by-2 circuits for both WCK01 and WCK23 might again have opposite phase alignment.

Figure 14 illustrates how the WCK phase information is derived. The phase detectors (PD) sample the internally divided-by-2 WCK clocks. Only one sample point is shown in the figure for clarity. In reality, when WCK2CK training mode is enabled, a sample will occur every t_{CK} and will be translated to the EDC pins accordingly. If the divided-by-2 WCK clock arrives early, then the EDC pin outputs the EDC hold pattern during the time interval specified in Figure 14. If the divided-by-2 WCK clock arrives late, then the EDC pin outputs the inverted EDC hold pattern during the time interval specified in Figure 14. This is shown in Table 10.

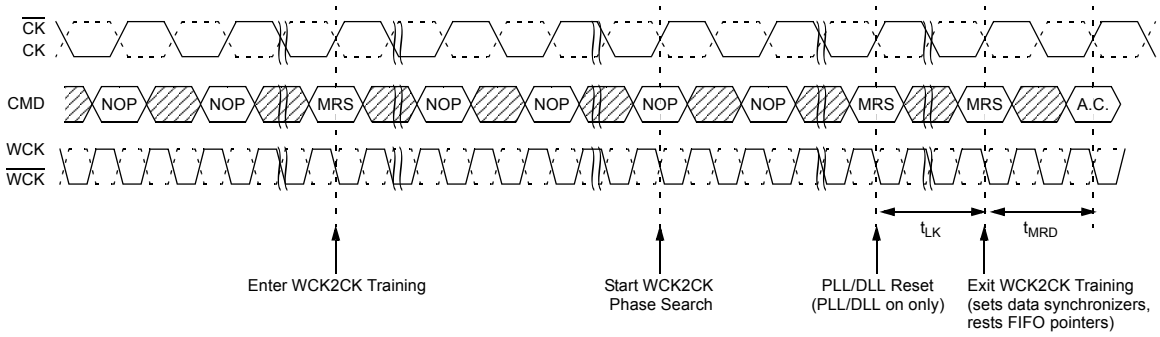


Figure 12. Example WCK2CK Training Sequence

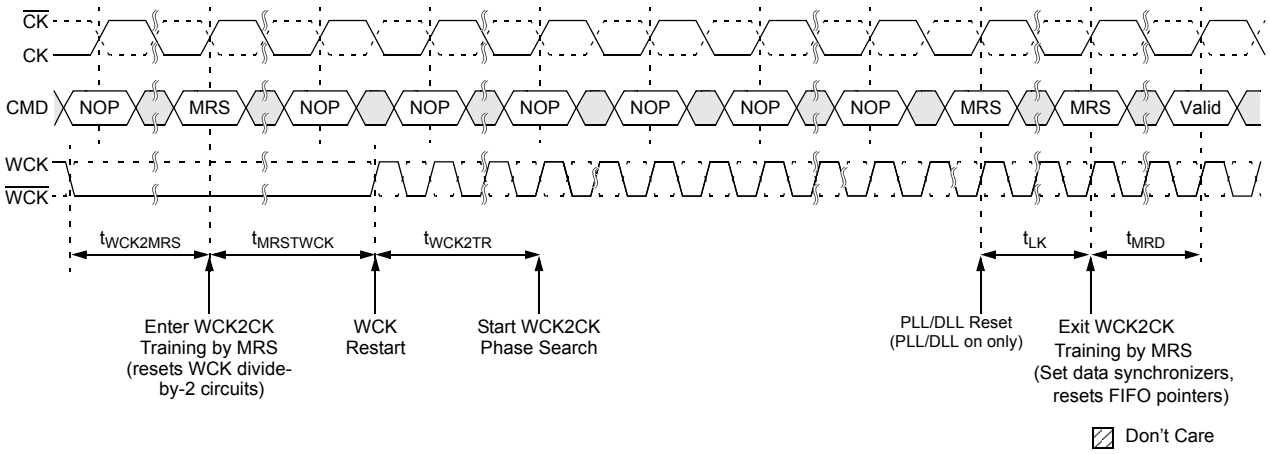


Figure 13. Example WCK2CK Training Sequence with WCK Stopping

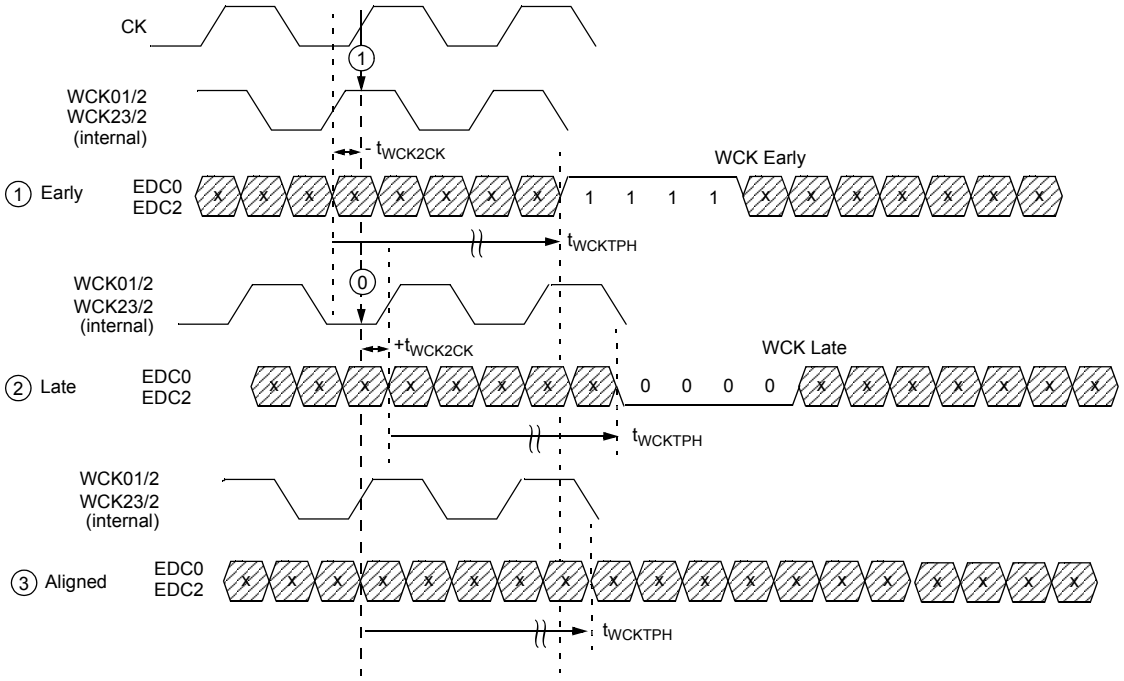


Figure 14. EDC pin Behaviour for WCK2CK Training (assumes '1111' as EDC Hold Pattern)

[Table 10] Phase Detector and EDC Pin behavior

WCK/2 value sampled by CK	WCK2CK Phase	Data on EDC Pin	Action
'1'	'Early'	EDC hold('1111')	Increase Delay on WCK
'0'	'Late'	Inverted EDC Hold('0000')	Decrease Delay on WCK

The ideal alignment is indicated by the phase detector output transitioning from "early" to "late" when the delay of the WCK phase is continuously increased. The WCK phase range for ideal alignment is specified by the parameter $t_{WCK2CKPIN}$ in the vendor's datasheet; the value(s) vary with the PLL/DLL mode (on or off) and the selected alignment point.

If enabled, the PLL/DLL shall not interfere in the behavior of the WCK2CK training. Significantly moving the phase and/or stopping the WCK during training may disturb the PLL/DLL. It is required to perform a PLL/DLL reset after the WCK2CK training has determined and selected the proper alignment between WCK and CK clocks. The PLL/DLL lock time t_{LK} must be met before exiting WCK2CK training to guarantee that the PLL/DLL is in lock such that the GDDR5 SGRAM data synchronizers are set upon WCK2CK training exit.

WCK2CK training is exited via MRS by resetting bit A4 in MR3. For proper reset of the data synchronizers it is required that the WCK and CK clocks are aligned within $t_{WCK2CKSYNC}$ at the time of the WCK2CK training exit.

After exiting WCK2CK training mode, the WCK phase is allowed to further drift from the ideal alignment point by a maximum of t_{WCK2CK}(e.g. due to voltage and temperature variation). Once this WCK phase drift exceeds t_{WCK2CK}(min) or t_{WCK2CK}(max), it is required to repeat the WCK2CK training and realign the clocks.

WCK2CK alignment at PIN Mode(optional)

The WCK and CK phase alignment point can be changed via MRS by setting bit A0 in MR6. In normal mode, when MR6 A0 is set "0", the phases of CK and WCK are aligned at CK pins and the end of WCK tree as shown in Figure 15. On the other hand, when MR6 A0 is set "1", the phases of CK and WCK are aligned at the pin as shown in Figure 16. PIN mode is supported up to the max CK clock frequency of f_{CKPIN}, and is an option to reduce the time of WCK2CK training at low frequency.

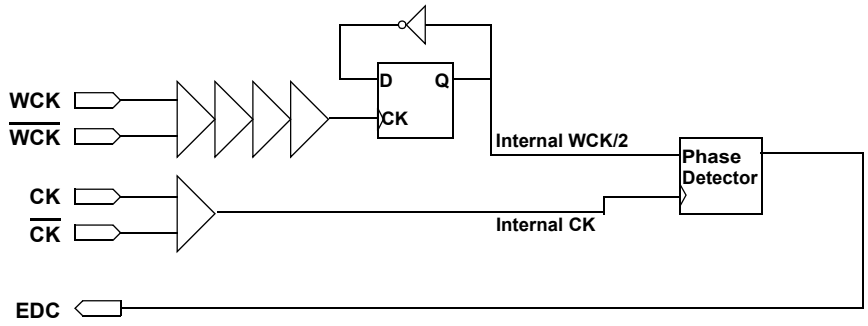


Figure 15. Normal Mode

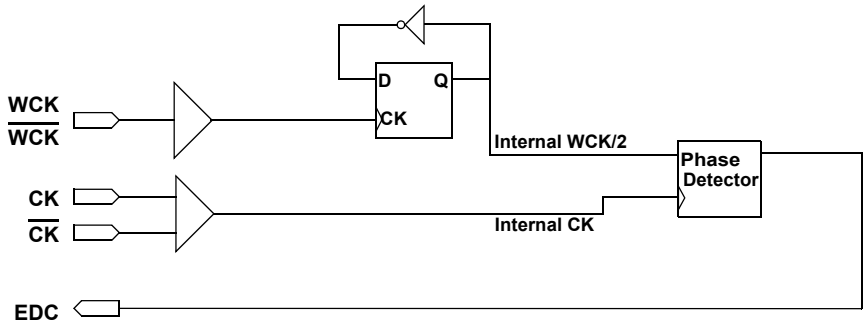


Figure 16. Pin Mode (Optional)

WCK2CK Auto Synchronization(Optional)

GDDR5 SGRAMs may optionally support a WCK2CK automatic synchronization mode that eliminates the need for WCK2CK training upon power-down exit. This mode is controlled by the autosync bit (MR7, bit A4), and is effective when the LP2 bit (MR5, bit A1) is set and the WCK clocks are stopped during power-down. Also, this mode works for both normal and PIN mode. When WCK2CK automatic synchronization mode is enabled, a full WCK2CK training including Phase search is not required after power-down exit, although WCK2CK MRS must be issued momentarily for setting the data synchronizers. However, WCK and CK clocks must meet the $t_{WCK2CKSYNC}$ specification upon power-down exit. Any allowed command may be issued after t_{XPN} or after t_{LK} in case the PLL/DLL had been enabled upon power-down entry. The PLL/DLL sequence is not affected by this mode. The use of WCK2CK automatic synchronization mode is restricted to lower operating frequencies up to $f_{CKAUTOSYNC}$ as described in vendors' datasheets.

Table 11 describes WCK2CK training methods for different frequency ranges. Each frequency range is vendor specific. Normal and PIN mode of WCK2CK training are described in Table 11. Divider initialization can be done by training with WCK2CK inversion, WCK2CK stopping, or WCK2CK auto-sync. If the user wants to use WCK2CK stop for divider initialization instead of WCK2CK auto-sync, the user must not set the WCK2CK auto-sync. Below middle frequency, the combined use of PIN and WCK2CK auto-sync modes can minimize WCK2CK training time.

[Table 11] An example of WCK2CK training simplified for Normal mode and PIN mode

	High Frequency (i.e 5Gbps)		Middle Frequency (i.e 2Gbps)		Low Frequency (i.e 400Mbps)	
Frequency (Vendor Specific)						
WCK2CK alignment mode	Normal	PIN	Normal	PIN	Normal	PIN
Phase Search	Required	Required	Required	No*	No*	No*

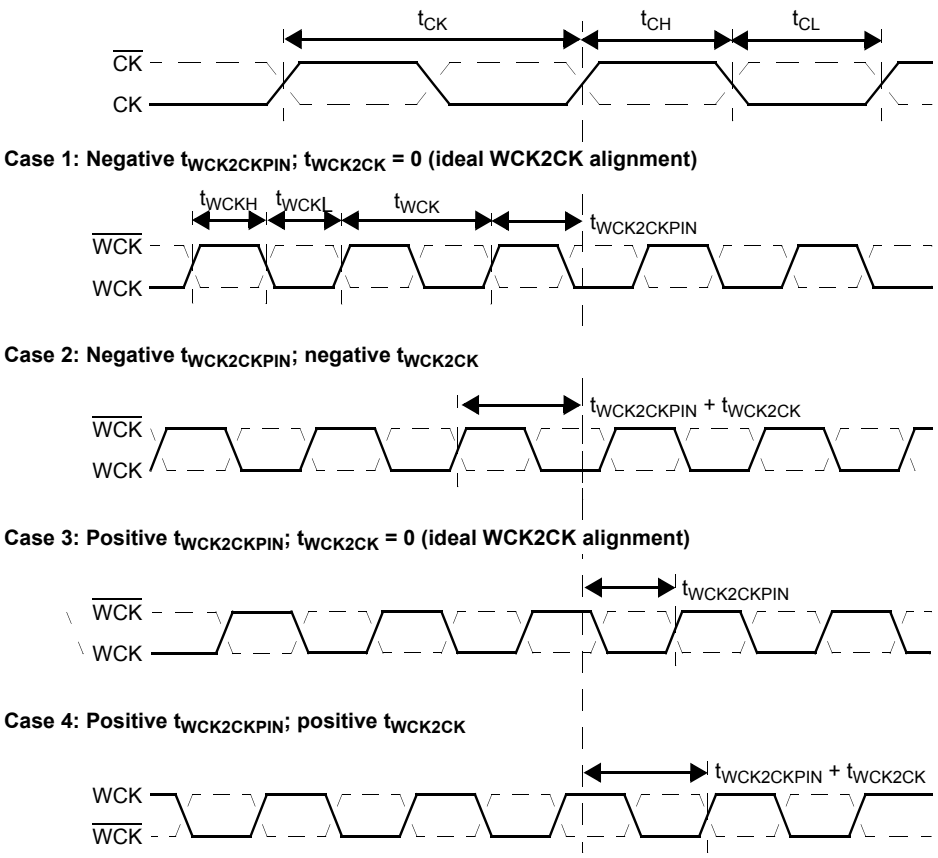
***NOTE** : The divided WCK/$\overline{WCK}$ should be aligned CK/$\overline{CK}$ by WCK2CK Auto Synchronization or WCK2CK stop mode

The following examples describe the WCK2CK training in more detail.

Example 1: outline of a basic WCK2CK training sequence without WCK clock stop:
1. Enable training mode via MRS and wait tMRD
2. Sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2;
in case the internal divide-by-2 circuits are at opposite phase use either the WCK01 or WCK23 inversion bit to flip one of the WCK divide-by-2 circuits
3. Adjust the WCK phase independently for WCK01 and WCK23 to the optimal point (“ideal alignment”)
4. Issue a PLL/DLL reset and wait for tLK (PLL/DLL on mode only)
5. While all WCK and CK are aligned, exit WCK2CK training mode via MRS
6. Wait t_{MRD} for the reset of data synchronizers

Example 2: outline of a basic WCK2CK training sequence with optional WCK clock stop:
1. Stop WCK clocks with WCK01/WCK23 LOW and $\overline{WCK01}$/$\overline{WCK23}$ HIGH
2. Wait $t_{WCKtMRS}$ for internal WCK clocks to settle
3. Enable training mode via MRS and wait tMRD for divide-by-2 circuits to reset
4. Start WCK clocks without glitches (both divide-by-2 circuits remain in sync)
5. Wait t_{WCKTTR} for internal WCK clocks to stabilize
6. Sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; adjust the WCK phase to the optimal point (“ideal alignment”)
7. Issue a PLL/DLL reset and wait t_{LK} (PLL/DLL on mode only)
8. While all WCK and CK are aligned, exit WCK2CK training mode via MRS
9. Wait tMRD for the reset of data synchronizers

READ and WRITE latency timings are defined relative to CK. Any offset in WCK and CK at the pins and/or the phase detector will be reflected in the latency timings. The parameters used to define the relationship between WCK and CK are shown in Figure 17. For more details on the impact on READ and WRITE timings see the OPERATIONS section.



NOTE : $t_{WCK2CKPIN}$ and t_{WCK2CK} parameter values could be negative or positive numbers, depending on the selected WCK2CK alignment point, PLL-on-or PLL-off mode operation and design implementation. They also vary across PVT. WCK2CK training is required to determine the correct WCK-to-CK phase for stable device operation.

Figure 17. WCK2CK timings

GDDR5 WCK2CK Training in x16 mode

For configurations with WCK clocks not shared between two GDDR5 SGRAMs. it is suggested to set the WCK phase to the ideal alignment point. However, for configurations where two GDDR5 SGRAMs(X16) share their WCK clocks as in a X16 clamshell, an offset given by the midpoint of both DRAM's ideal WCK positions may be required. The maximum allowed offset in this case is specified by parameter $t_{WCK2CKSYNC}$: it defines the WCK offset range from the ideal alignment which still guarantees a GDDR5 SGRAM device to internally synchronize its WCK and CK clocks upon training exit.
Example: outline of training sequence for x32 and x16 configurations with 2 GDDR5 SGRAMs sharing their WCK clocks (e.g. clamshell):

1. Enable training mode for both DRAMs via MRS and wait tMRD
2. For both DRAMs sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; in case the internal divide-by-2 circuits are at opposite phases use either the WCK01 or WCK23 inversion bit to flip one of the WCK divide-by-2 circuits; in case of shared $\overline{CS}$ signals use MREMF0 and MREMF1 bits in MR15 to explicitly direct the MRS command for this phase flipping to either DRAM1 or DRAM2 ("soft chip select");
3. Sweep and observe the phase on DRAM1 independently for WCK01 on EDC0 and WCK23 on EDC2; store the setting for the optimal WCK phase
4. Sweep and observe the phase on DRAM2 independently for WCK01 on EDC0 and WCK23 on EDC2; store the setting for the optimal WCK phase
5. Sweep WCK01 and WCK23 phase to midpoint of DRAM1 and DRAM2 optimal settings
6. Issue a PLL/DLL reset and wait for t_{LK} (PLL/DLL on mode only)
7. While all WCK and CK are aligned, exit WCK2CK training mode via MRS
8. Wait t_{MRD} for the reset of data synchronizers

Glitchless WCK/$\overline{WCK}$ Phase Change

During WCK-to-CK training, the phase of WCK/$\overline{WCK}$ is changed. The phase change should not cause any glitch in WCK/$\overline{WCK}$. The glitch results in phase inversion of WCK divider. The output of phase detector is also inverted.

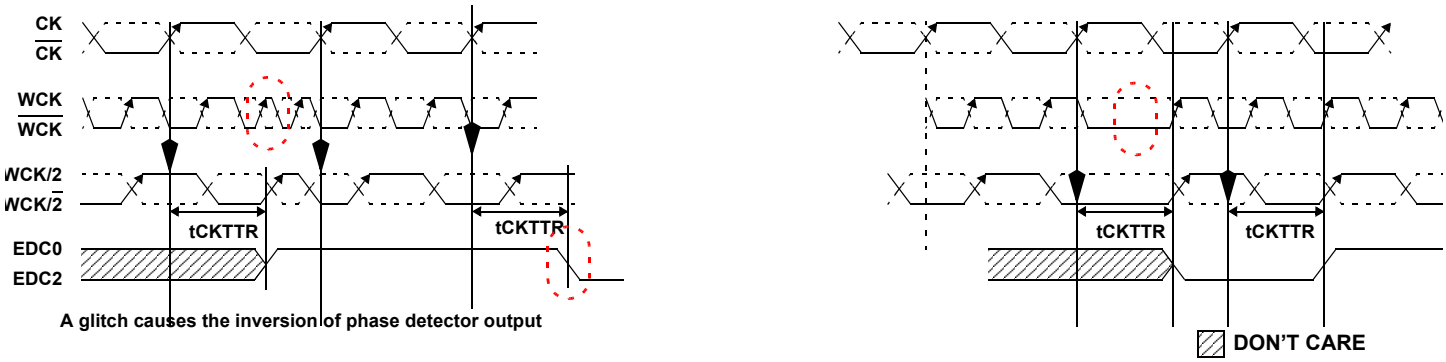


Figure 18. Glitchless WCK/$\overline{WCK}$ Phase Change

Robust Usage of Phase Detector Information

After WCK/2 and CK are closely aligned, the phase detector information may have uncertainty. The pattern on EDC pin can have an unstable value that does not reflect the phase difference between WCK/2 and CK. Users have to provide a dithering mechanism to filter out the uncertainty during WCK2Ck training.

Accuracy of WCK2CK Training with PLL

If PLL is ON, the static phase offset of PLL diminishes FIFO initialization margin between WCK/2 and CK which is tuned during WCK2CK training. In order to increase the accuracy of WCK2CK training, users have to take account of the static phase offset of PLL.

16.4 READ Training

Read training allows the memory controller to find the data-eye center (symbol training) and burst frame location (frame training) for each high-speed output of the GDDR5 SGRAM. Each pin (DQ0-DQ31, $\overline{\text{DBI0}}$ -$\overline{\text{DBI3}}$, EDC0-EDC3) can be individually trained during this sequence. Read training consists of LDFF and RDTR commands.

For Read Training the following conditions must be true(The conditions below apply to both LDFF and RDTR operations):

- at least one bank is active, or an auto refresh must be in progress and bit A2 in Mode Register 5 (MR5) is set to 0 to allow training during auto refresh (to disable this special REF enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- WCK2CK training must be complete
- the PLL/DLL must be locked, if enabled
- RDBI and WDBI must be enabled prior to and during Read Training if the training shall include the $\overline{\text{DBI}}$ pins. RDCRC and WRCRC must be enabled prior to and during Read Training if the training shall include the EDC pins.

The following commands are associated with Read Training:

- LDFF to preload the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO

Neither LDFF nor RDTR access the memory core. No MRS is required to enter Read Training.

Below figure shows an example of the internal data paths used with LDFF and RDTR. Table 12 lists AC timing parameters associated with Read Training.

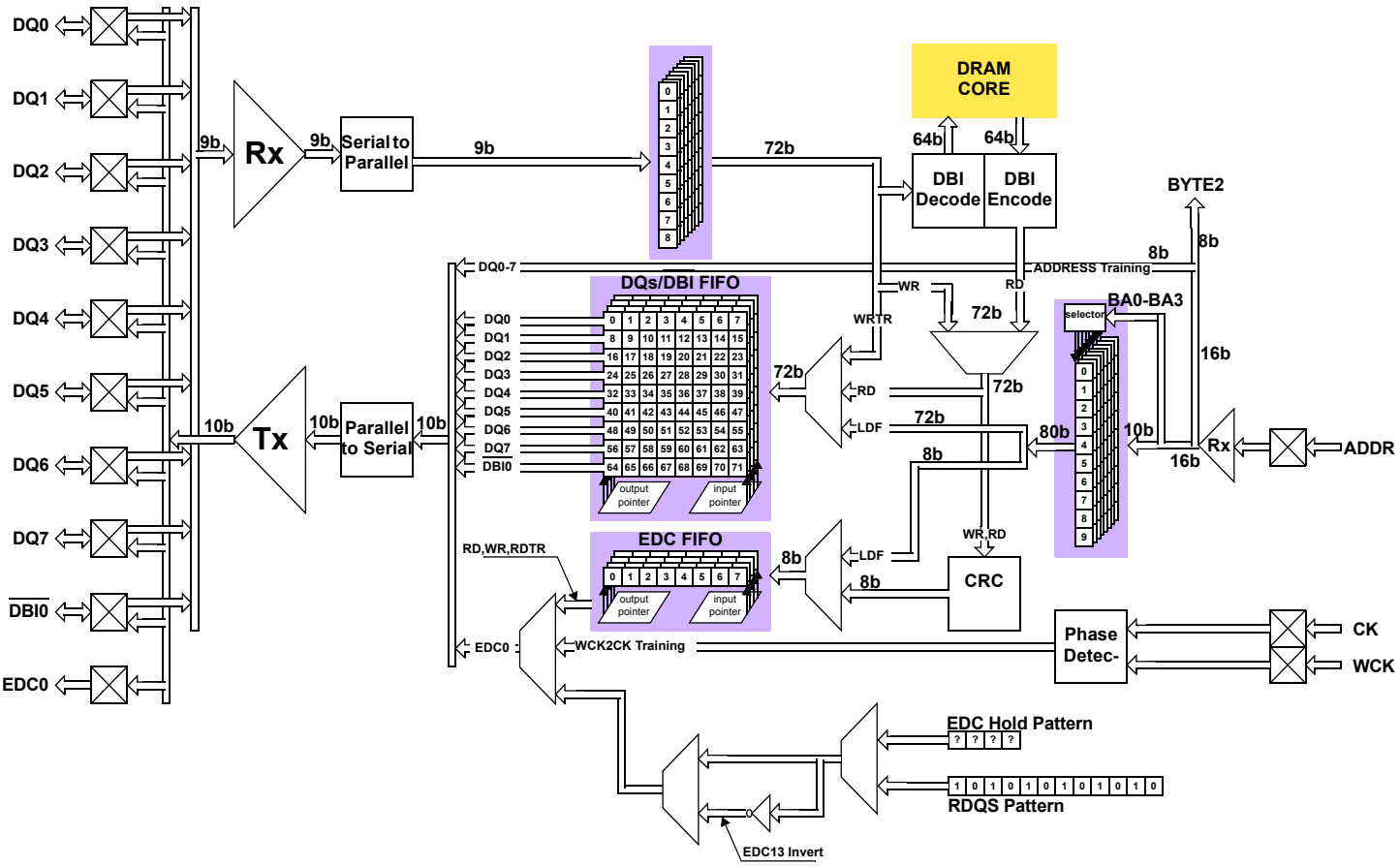
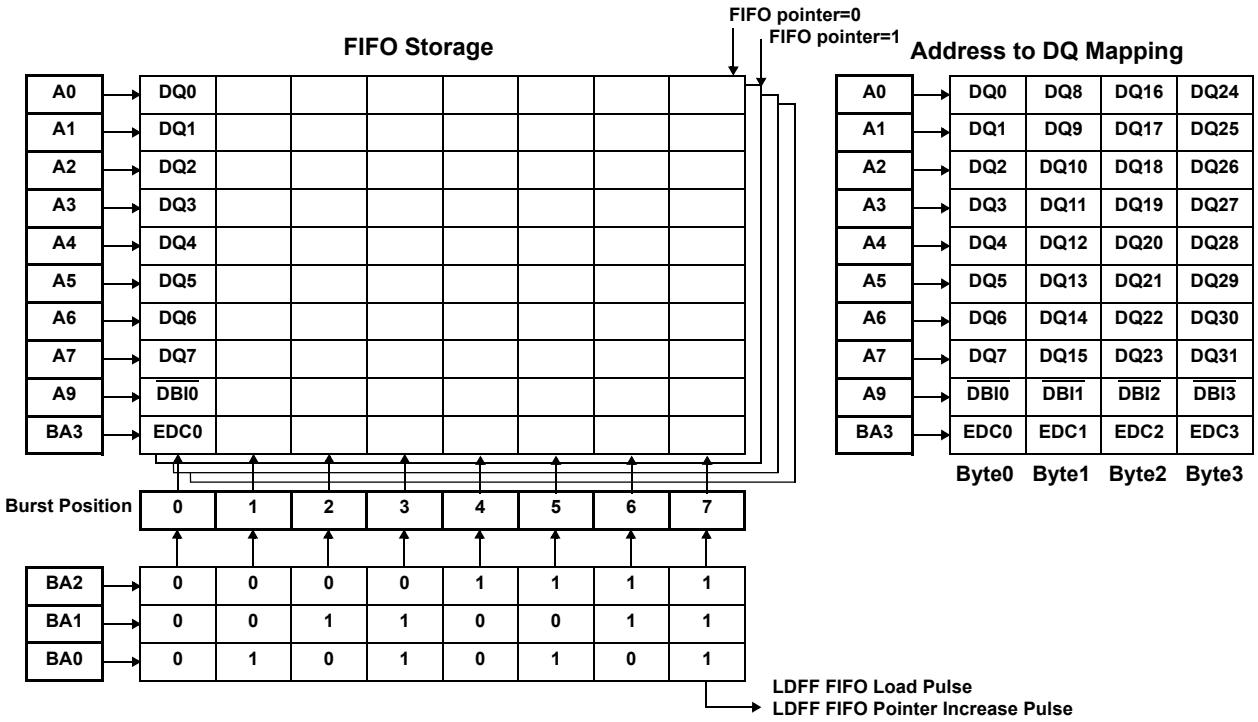


Figure 19. Data Paths used for Read and Write Training

Load FIFO (LDFF)

After power-up, the address training comes first, WCK to CK training second, and the next training should be read training. In read training, a known pattern should be transferred to DRAM so that read data can be compared with the known pattern. To transfer user specified pattern into the output FIFO of the DRAM, slow access to DRAM is necessary, however, operating frequency of WCK and CK should not be decreased because of overhead of clock frequency change. The address path can be used for the transfer of the known data pattern since address path is tuned during the address training. The path from address to output FIFO is provided when LDFF command is issued and then the output FIFO is filled with the known pattern via address one by one. $\overline{DBI}$ and EDC pins reflect the known pattern via address such as A9 and BA3. WCK is not required for LDFF operation. The BA address is used to select the position of burst to be stored (The data pattern is not loaded by LDFF command with BA address other than "111"). BA address "111" has the special meaning. It loads the known data pattern to the FIFO and the write pointer of the FIFO can be moved to the next word. By doing this, all of the FIFO depth can be filled with user supplied data pattern. When there is no LDFF command between the first LDFF command with BA address "111" and the next LDFF command with BA address "111", the second LDFF command will store the same pattern to the corresponding FIFO storage as the first burst pattern.
The number of LDFF commands depends upon the FIFO depth. The FIFO depth information can be retrieved by vendor ID MRS. In LDFF operation, address bus inversion takes place but CRC and data bus inversion are not performed.



NOTE : DQ numbering based on MF=0. When mirrored, DQ will be renamed but physical location is not changed.

Figure 20. LDFF Command Address to DQ/$\overline{DBI}$/EDC Mapping

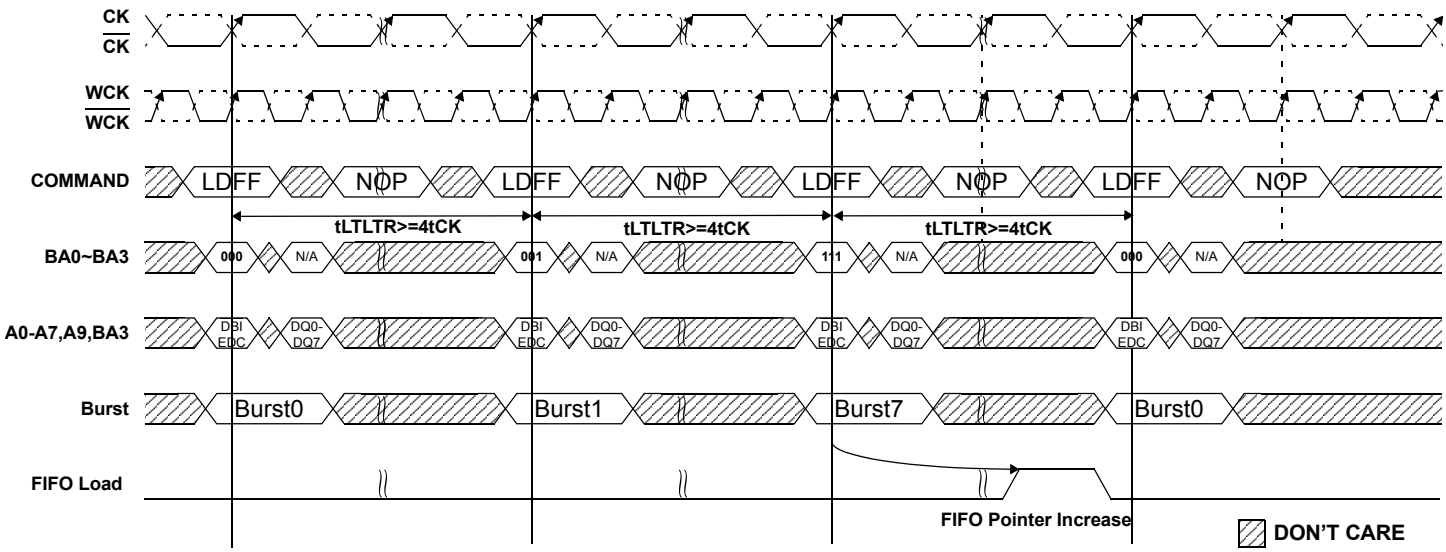


Figure 21. LDFF Timing

[Table 12] LDFF and RDTR Timing

Parameter	Symbols	Min	Max	Unit	NOTE
Active to LDFF command delay	tRCDLTR		-	ns	
Active to RDTR command delay	tRCDRTR		-	ns	
Refresh to RDTR or WRTR command delay	tREFTR		-	ns	
RDTR to RDTR command delay	tCCDS		-	tCK	
LDFF to LDFF command cycle time	tLTLTR	4	-	tCK	
LDFF(111) to LDFF command cycle time	tLTL7TR		-	tCK	1
LDFF(111) to RDTR command delay	tLTRTR		-	tCK	
Read or RDTR to LDFF command delay	tRDTLT		-	tCK	

NOTE : 1. The min value is vendor specific and does not exceed 8 tCK.

Load FIFO (LDFF)

The LDFF command is used to securely load data to the GDDR5 SGRAM Read FIFOs via the address bus. Depending on the GDDR5 SGRAM READ FIFO depth FIFO(6), any bit pattern of length 32 can be loaded uniquely to every DQ, DBI and EDC pin within a byte. The FIFO depth can be read via the Vendor ID function.

Eight LDFF commands are required to fill one FIFO stage; each LDFF command loads one burst position, and the bank addresses BA0-BA3 select the burst position from 0 to 7. The data pattern is conveyed on address pins A0-A7 for DQ0-DQ7, A9 for DBI0, and BA3 for EDC0; the data are internally replicated to all 4 bytes, as shown in blow figure.

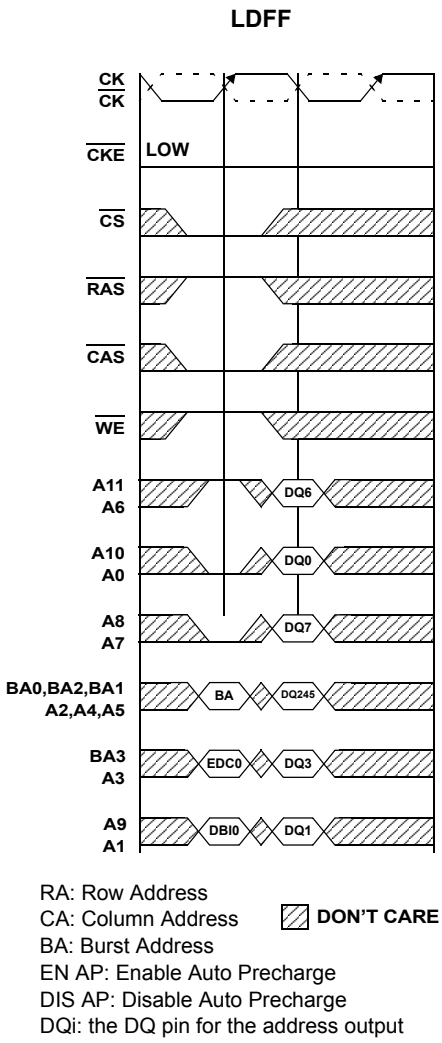
LDFF loads the DBI FIFO regardless of the WDBI and RDBI Mode Register bits. It also loads the EDC FIFO regardless of the WRCRC and RDCRC Mode Register bits, and no CRC is calculated; however, RDBI and RDCRC must be enabled to read the DBI and EDC bits, respectively, with the RDTR command.

All burst addresses 0 to 7 must be loaded; LDFF commands to burst address 0 to 6 may be issued in random order; the LDFF command to burst address 7 (LDFF7) must be the last of 8 consecutive LDFF commands, as it effectively loads the data into the FIFO and results in a FIFO pointer increment. Consecutive LDFF commands have to be spaced by at least tLTLTR, and at least tLTL7TR cycles are required after each LDFF command to burst address 7.

LDFF pattern may efficiently be replicated to the next FIFO stages by issuing consecutive LDFF commands to burst address 7 (with identical data pattern). The data pattern in the scratch memory for LDFF will be available until the first RDTR command.The DQ/DBI output buffers remain in ODT state during LDFF. An amount of LDFF commands to burst address 7 greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data input.

The total number of LDFF commands to burst address 7 modulo FIFO depth must equal the total number of RDTR commands modulo FIFO depth when used in conjunction with RDTR. No READ or WRITE commands are allowed between LDFF and RDTR.

The EDC hold pattern is driven on the EDC pins during LDFF (provided RDQS mode is not enabled).



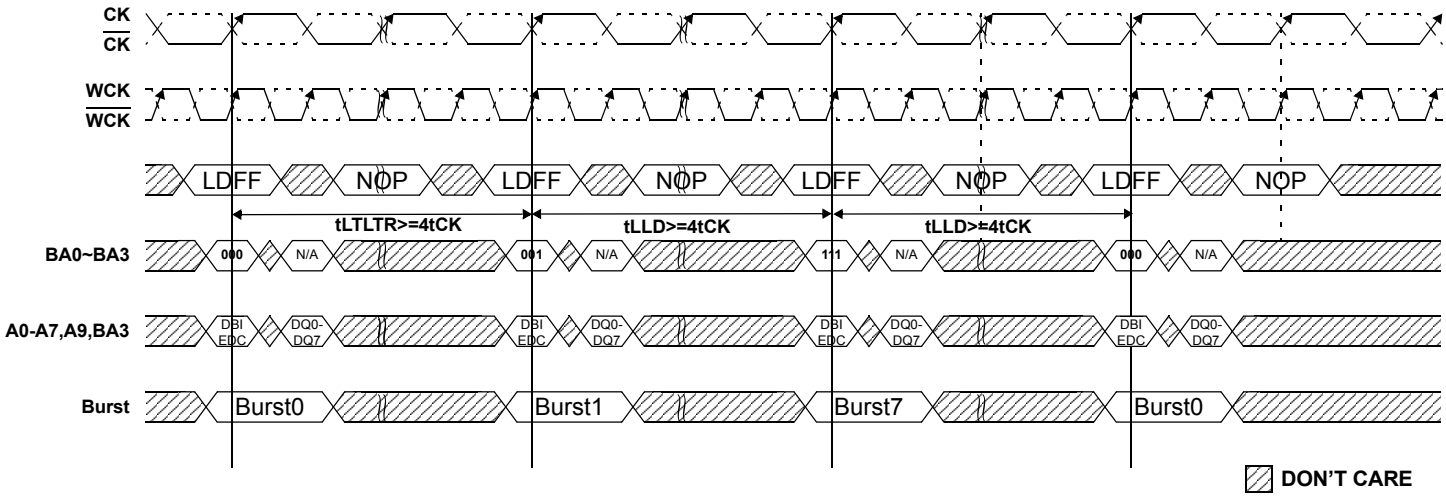


Figure 22. LDFF Timing

READ Training (RDTR)

A RDTR burst is initiated with a RDTR command as shown in Figure RDTR . No bank or column addresses are used as the data is read from the internal READ FIFO, not the array. The length of the burst initiated with a RDTR command is eight. There is no interruption nor truncation of RDTR bursts.

A RDTR command may only be issued when a bank is open or a refresh is in progress and bit A2 in MR5 is set to 0 to allow training during refresh.

RDBI and RDCRC must be enabled to read the DBI and EDC bits, respectively, with the RDTR command. If not set, the DBI pins will remain in ODT state, and the EDC pins will drive the EDC hold pattern.

In case of the RDQS mode, the EDC pin functions like with a normal READ in this mode. The DBI pin behaves like a DQ, and no encoding with DBI is performed.

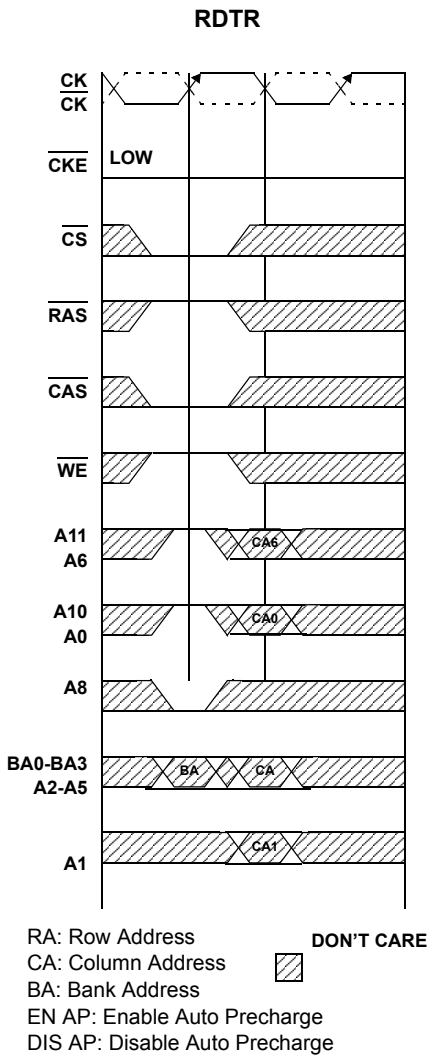
An amount of RDTR commands greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data output. The FIFO depth from which the RDTR data is read must be a number as 6. The FIFO depth is read via the Vendor ID function.

During RDTR bursts, the first valid data-out element will be available after the CAS latency (CL). The latency is the same as for READ. The data on the EDC pins comes with additional CRC latency (tCRCRD) after the CL.

Upon completion of a burst, assuming no other RDTR command has been initiated, all DQ and DBI pins will drive a value of '1' and the ODT will be enabled at a maximum of 1 tCK later. The drive value and termination value may be different due to separately defined calibration offsets. If the ODT is disabled, the pins will drive Hi-Z.

Data from any RDTR burst may be concatenated with data from a subsequent RDTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new RDTR command should be issued after the first RDTR command according to the tCCDS timing.

A WRTR can be issued any time after a RDTR command as long as the bus turn around time tRTW is met. The total number of RDTR commands modulo FIFO depth must be equal to total number of WRTR commands modulo FIFO depth when used in conjunction with WRTR. No READ or WRITE commands are allowed between WRTR and RDTR.



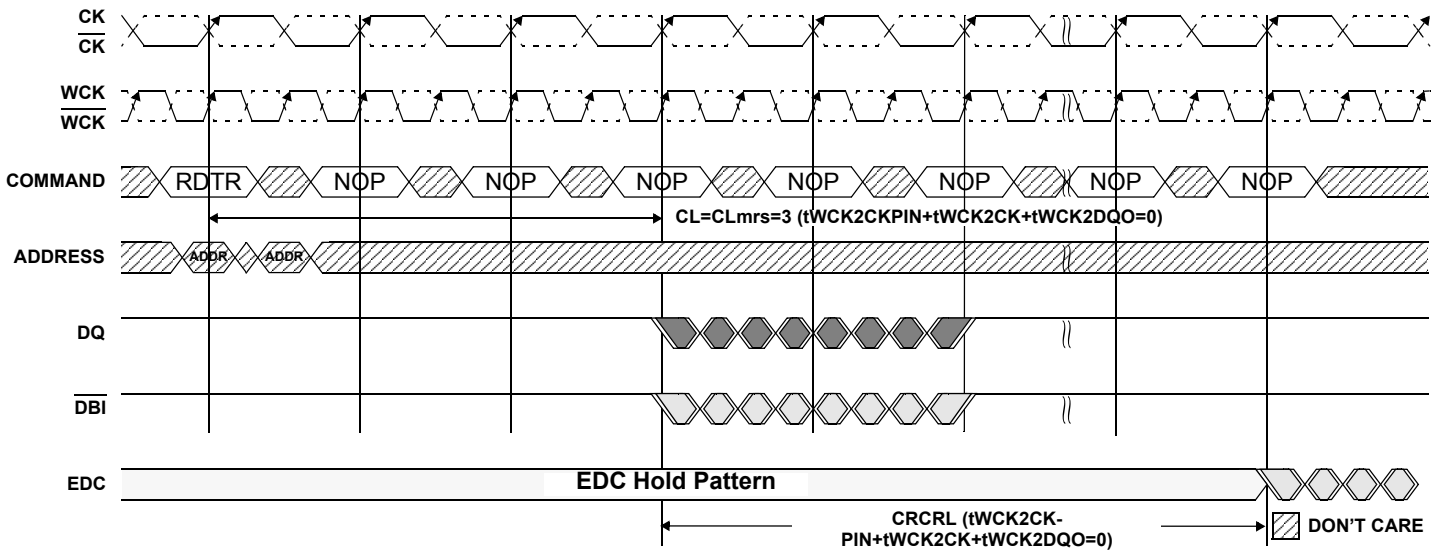


Figure 23. RDTR Timing

16.5 WRITE Training (WRTR)

Write training allows the memory controller to find the data-eye center (symbol training) and burst frame location (frame training) for each high-speed input of the GDDR5 SGRAM. Each pin (DQ0-DQ31, $\overline{DBI0}$-$\overline{DBI3}$) can be individually trained during this sequence.

For Write Training the following conditions must be true:
- at least one bank is active, or an auto refresh must be in progress and bit A2 in Mode Register 5 (MR5) is set to 0 to allow training during auto refresh (to disable this special REF enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- the PLL/DLL must be locked, if enabled.
- WCK2CK training should be complete
- Read training should be complete
- RDBI and WDBI must be enabled prior to and during Write Training if the training shall include the $\overline{DBI}$ pins. RDCRC and WRCRC must be enabled prior to and during Write Training if the training shall include the EDC pins.

The following commands are associated with Write Training:
- WRTR to write a burst of data directly into the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither WRTR nor RDTR access the memory core. No MRS is required to enter Write Training.

Data Training During AREF

During Auto Refresh period, Read and Write training can be performed for periodic data training. The WCK/$\overline{WCK}$ clock tree must be enabled to perform RDTR and WRTR commands. When entering Auto Refresh, the clock tree is enabled within tMRD. However, LDFF does not depend on the WCK/$\overline{WCK}$ clock tree.

WRITE Training (WRTR)

A WRTR burst is initiated with a WRTR command as shown in figure WRTR. No bank or column addresses are used as the data is written to the internal READ FIFO, not the array. The length of the burst initiated with a WRTR command is eight. There is no interruption nor truncation of WRTR bursts.

A WRTR command may only be issued when a bank is open or a refresh is in progress and bit A2 in MR5 is set to 0 to allow training during refresh.

WDBI and WRCRC must be enabled to write the DBI and EDC bits, respectively, with the WRTR command. If WDBI is not set, a '1' will be written to the DBI FIFO, and a '1' will be assumed for the DBI input in the CRC calculation. In contrast to a normal WRITE, no CRC is returned by the WRTR command and the EDC pins will drive the EDC hold pattern.
In case of the RDQS mode, the EDC pin functions like with a normal READ in this mode. Please note that RDCRC must be enabled to read the calculated CRC data with the RDTR command.

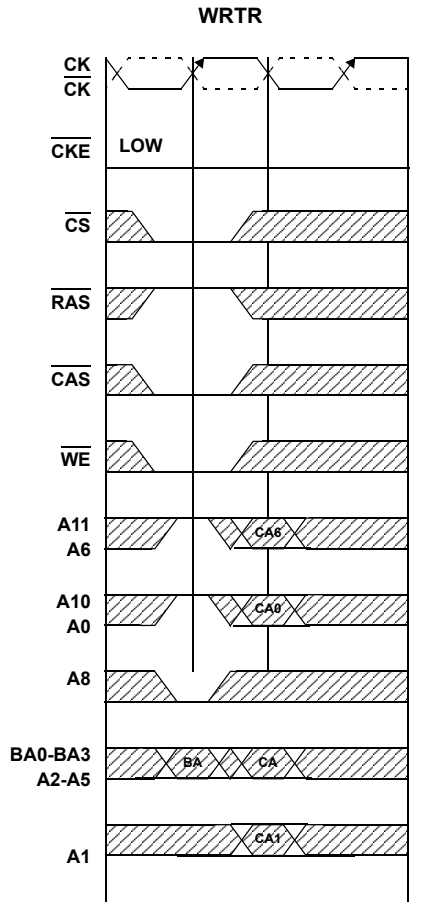
An amount of WRTR commands equal to the FIFO depth is required to fully load the FIFO; any number of WRTR commands greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data input. The FIFO depth to which the WRTR data is written must be a number as 6. The FIFO depth is read via the Vendor ID function.

During WRTR bursts, the first valid data-in element must be available at the input latch after the Write Latency (WL). The Write Latency is the same as for WRITE.

Upon completion of a burst, assuming no other WRTR data is expected on the bus the GDDR5 SGRAM DQ and DBI pins will be driven according to the ODT state. Any additional input data will be ignored.

Data from any WRTR burst may be concatenated with data from a subsequent WRTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new WRTR command should be issued after the previous WRTR command according to the tCCDS timing.

A RDTR can be issued any time after a WRTR command as long as the internal bus turn around time tRTWTR is met. The total number of WRTR commands modulo FIFO depth must equal the total number of RDTR commands modulo FIFO depth when used in conjunction with RDTR. No READ or WRITE commands are allowed between WRTR and RDTR.



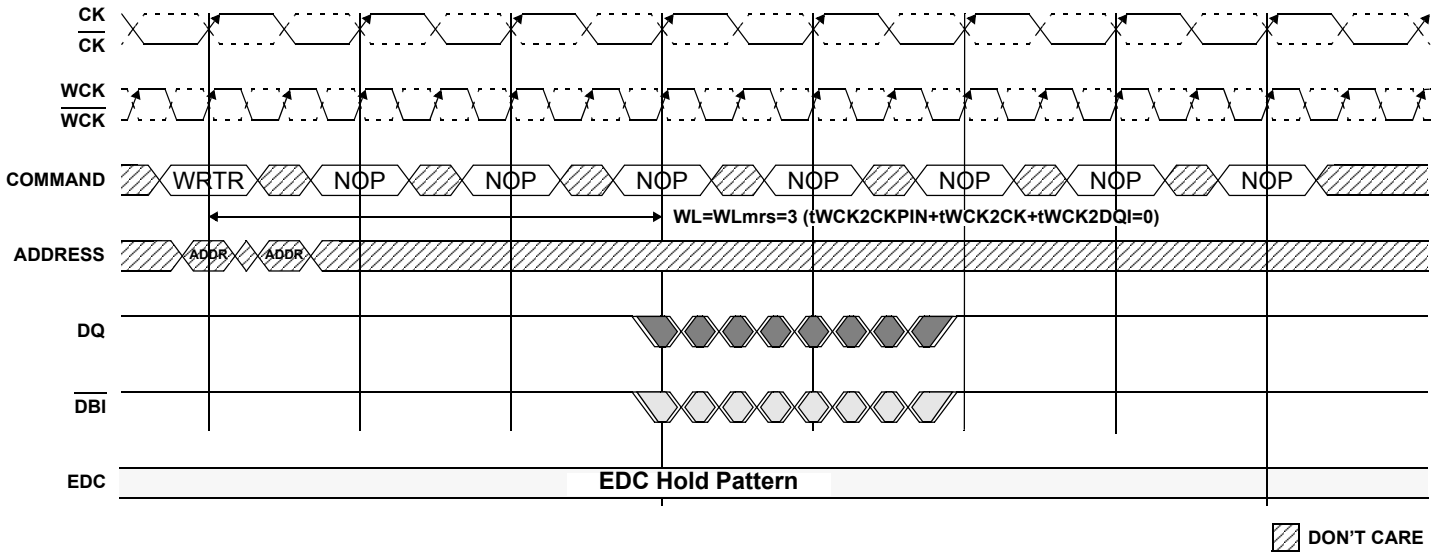
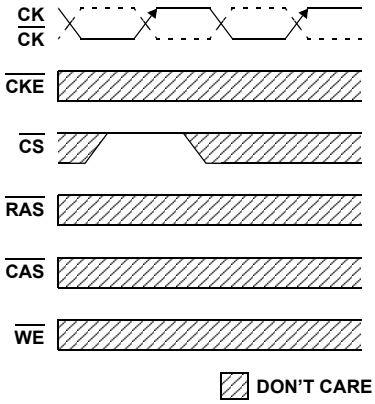


Figure 24. WRITE Training Timing

17. OPERATIONS

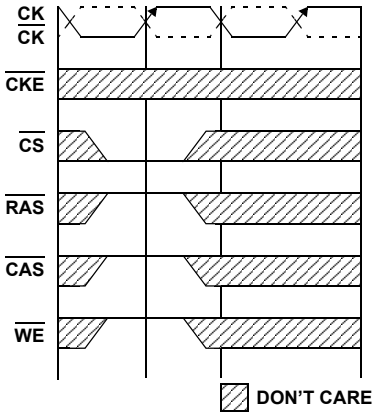
17.1 Deselect (DES)

The DESELECT function ($\overline{CS}$=HIGH) prevents new commands from being executed by the GDDR5 DRAM. The GDDR5 DRAM is effectively deselected. Operations already in progress are not affected.



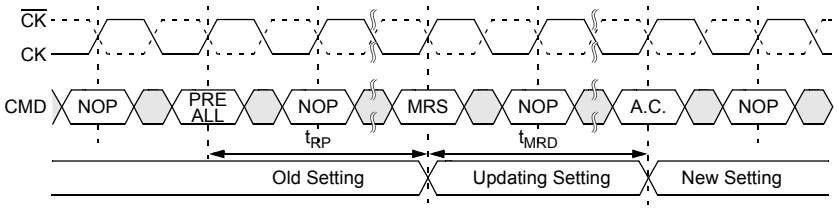
17.2 No Operation (NOP)

The NO OPERATION (NOP) command is used to instruct the selected GDDR5 DRAM to perform a NOP ($\overline{CS}$=LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.



17.3 Mode Register Set

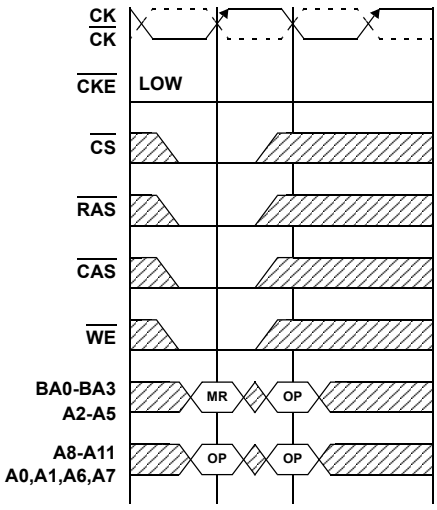
The MODE REGISTER SET command is used to load the Mode Registers of the GDDR5 SGRAM. The bank address inputs BA0-BA3 select the Mode Register, and address puts A0-A11(A12) determine the op-code to be loaded. See MODE REGISTER for a register definition. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.



A.C. = access command (any command allowed in bank idle state)

Don't Care

Mode Register Set Timings



MR: Mode Register Address
OP: Bits to be set in MR

DON'T CARE

17.4 BANK/ROW Activation

Before any READ or WRITE commands can be issued to a banks within the GDDR5 SGRAM, a row in that bank must be "opened". This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated. BA0-BA3 select the bank, and the address inputs select the row to be activated. Once a row is open, a READ or WRITE command could be issued to that row, subject to the tRCD specification.

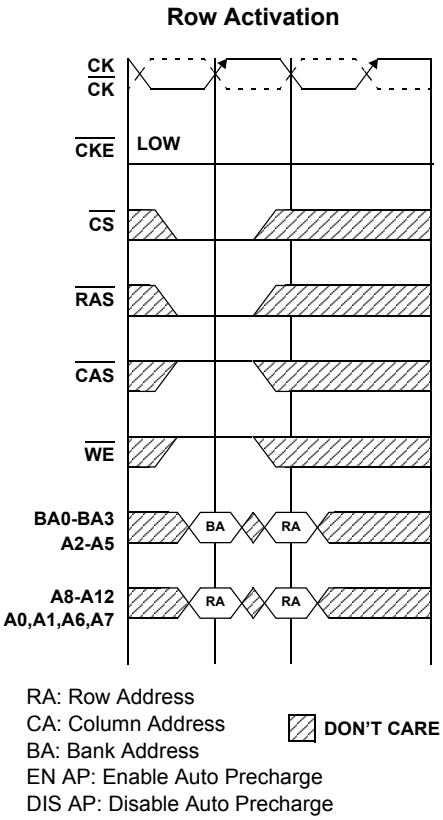
tRCD(min) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command in which a READ or WRITE command can be entered. For example, a tRCD specification of 16ns with a 800MHz clock (1.25ns period) results in 12.8 clocks rounded to 13. This is reflected in below figure, which covers any case where 12<tRCD(min)/tCK≤13. (The same is true for other AC parameters).

A subsequent ACTIVE command to another row in the same bank can only be issued after the previous active row has been "closed"(precharged). The minimum time interval between two successive ACTIVE commands on the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between two successive ACTIVE commands on different banks is defined by tRRD.

The row remains active until a PRECHARGE command (or READ or WRITE with Auto Precharge) is issued to the bank. A PRECHARGE command (or READ or WRITE with Auto Precharge) must be issued before opening a different row in the same bank.

*Note: Any system or application incorporating random access memory products should be properly designed, tested and qualified to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.



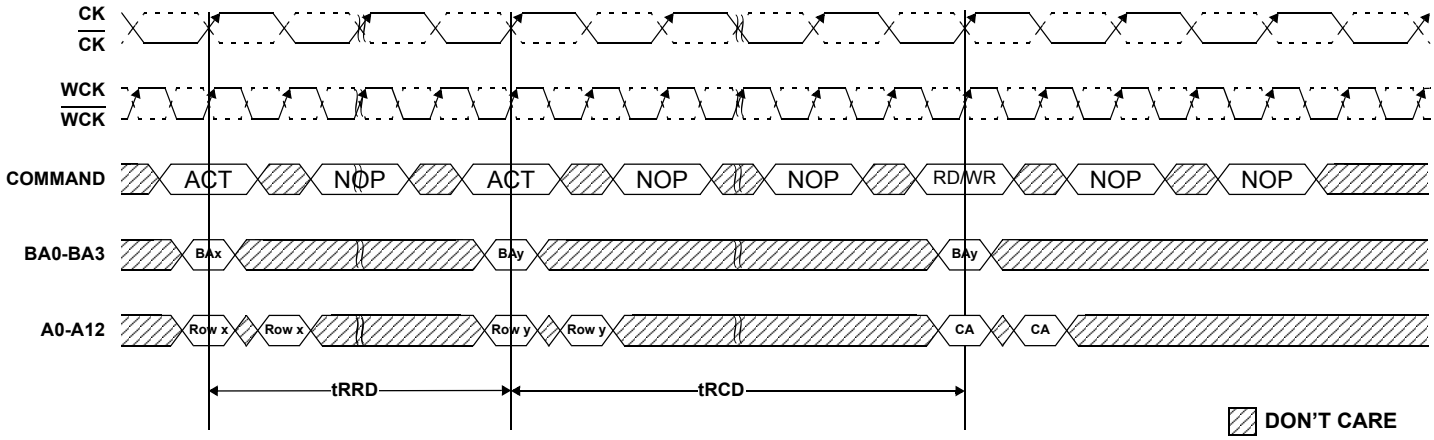


Figure 25. Bank Activation Command Cycle

17.5 Bank Restrictions (tFAW)

For eight bank GDDR5 DRAM, there should be required to limit the number of ACTIVE commands in a rolling window to ensure that the instantaneous current supplying capability of the DRAM is not exceeded. To reflect the true capability of the DRAM instantaneous current supply, the parameter tFAW (four activate window) is defined. No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW(ns) by tCK(ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an active command is issued in clock N, no more than three further activate commands may be issued in clocks N+1 through N+9.

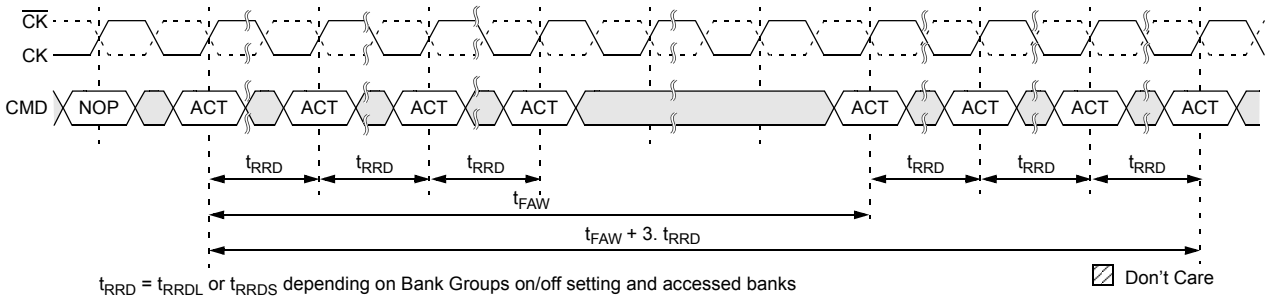


Figure 26. t_{RDD} and t_{FAW}

17.6 READ

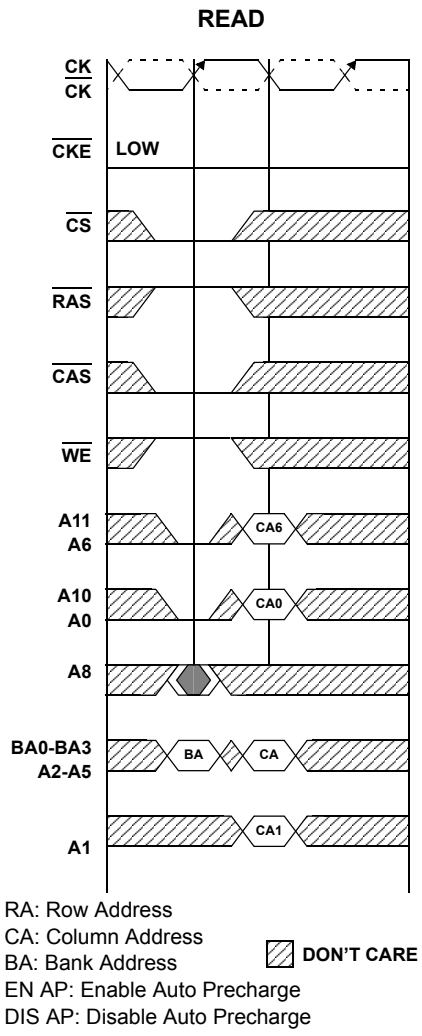
A READ burst is initiated with a READ command as shown in Figure READ. The bank and column addresses are provided with the READ command and auto precharge is either enabled or disabled for that access with the A8 address. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after tRAS(min) has been met or after the number of clock cycles programmed in the RAS field of MR5 (bits A6-A11), depending on the implementation choice per DRAM vendor. The length of the burst initiated with a READ command is eight and the column address is unique for this burst of eight. There is no interruption nor truncation of READ bursts.

During READ bursts, the first valid data-out element will be available after the CAS latency (CL). The CAS Latency is defined as CLmrs * tCK + tWCK2CKPIN + tWCK2CK + tWCK2DQO, where CLmrs is the number of clock cycles programed in MR0, tWCK2CKPIN is the phase offset between WCK and CK at the pins when phase aligned at phase detector, tWCK2CK is the alignment error between WCK and CK at the GDDR5 SGRAM phase detector, and tWCK2DQO is the WCK to DQ/DBI/EDC offset as measured at the DRAM pins. The total delay is relative to the data eye initial edge averaged over one double-byte. The maximum skew within a double-byte is defined by tDQDQO.

Upon completion of a burst, assuming no other READ command has been initiated, all DQ and DBI pins will drive a value of '1' and the ODT will be enabled at a maximum of 1 tCK later. The drive value and termination value may be different due to separately defined calibration offsets. If the ODT is disabled, the pins will drive Hi-Z.

Data from any READ burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued after the previous READ command according to the tCCD timing. If that READ command is to another bank then an ACTIVE command must precede the READ command and tRCDRD also must be met.

A WRITE can be issued any time after a READ command as long as the bus turn around time tRTW is met. If that WRITE command is to another bank, then an ACTIVE command must precede the second WRITE command and tRCDWR also must be met. A PRECHARGE can also be issued to the GDDR5 SGRAM with the same timing restriction as the new READ command if tRAS is met. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. The data inversion flag is driven on the DBI pin to identify whether the data is true or inverted data. If DBI is HIGH, the data is not inverted, and if LOW it is inverted. READ Data Inversion can be enabled (A8=0) or disabled (A8=1) using RDBI in MR1. When enabled by the RDCRC flag in MR4, EDC data is returned to the controller with a latency of (CLmrs + CRCRL) * tCK + tWCK2CKPIN + tWCK2CK + tWCK2DQO, where CRCRL is the CRC Read latency programmed in MR4.



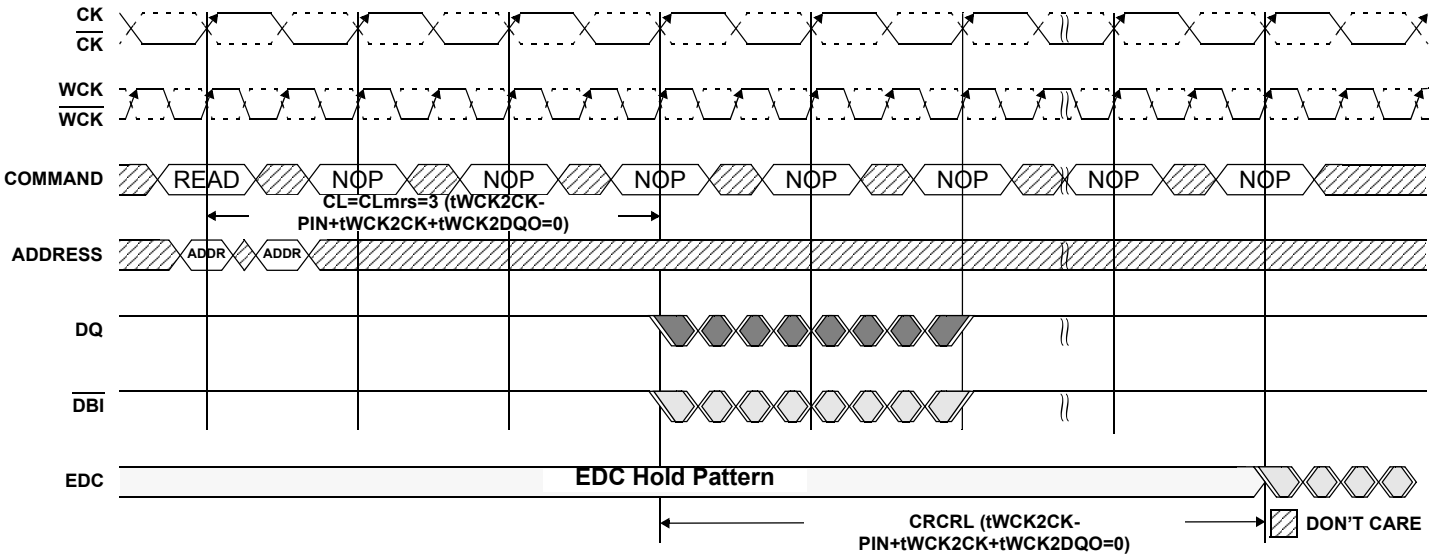
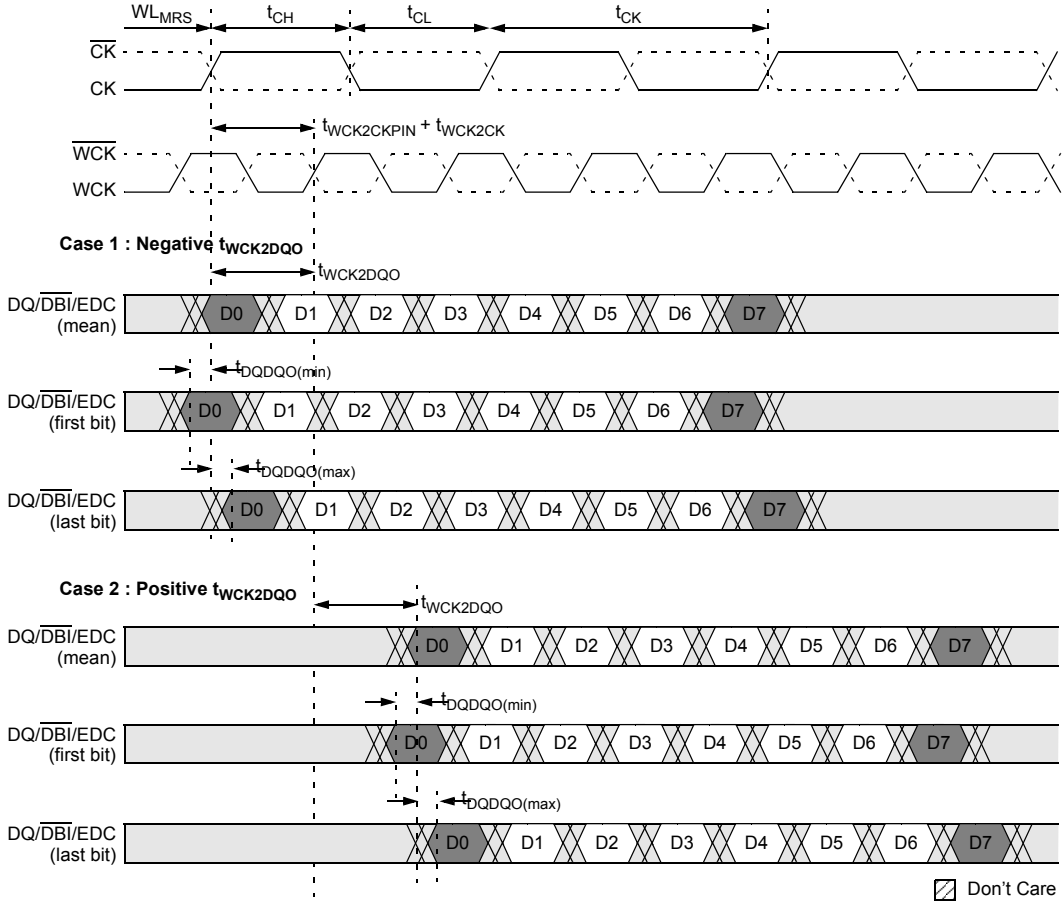
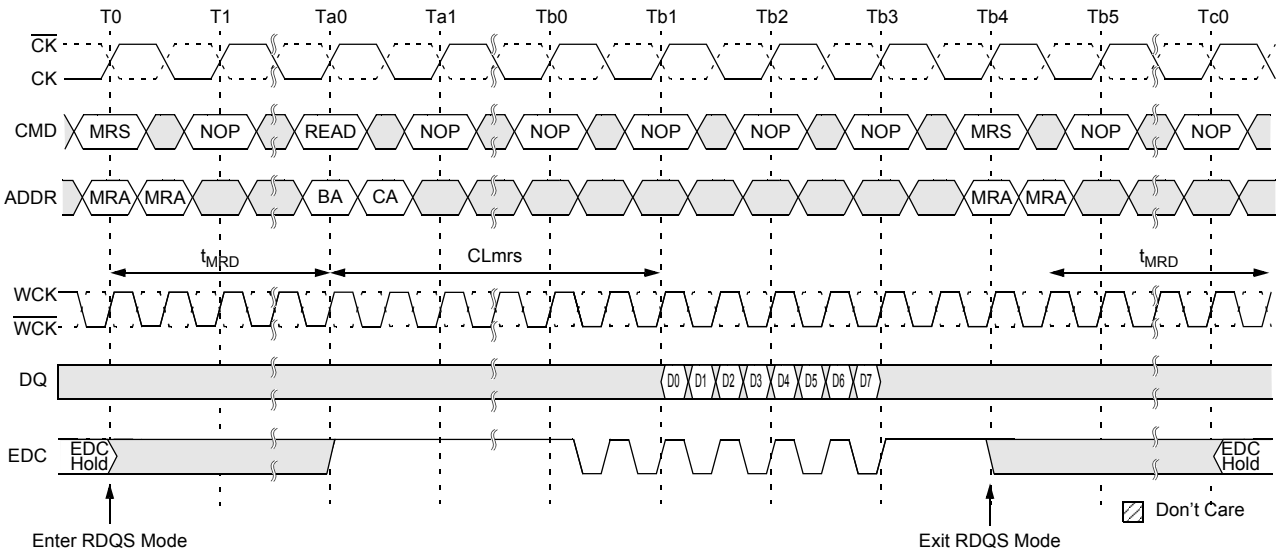


Figure 27. READ Timing



1) CL_{MRS} is the CAS latency programmed in Mode Register MR0.
2) Timings are shown with positive $t_{WCK2CKPIN}$ and t_{WCK2CK} values. See WCK-to-CK timings for $t_{WCK2CKPIN}$ and t_{WCK2CK} ranges.
3) $t_{WCK2DQO}$ parameter values could be negative or positive numbers, depending on PLL-on-or PLL -off mode operation and design implementation. They also vary across PVT. Data training is required to determine the actual $t_{WCK2DQO}$ value for stable READ operation.
4) t_{DQDQO} defines the minimum to maximum variation of $t_{WCK2DQO}$ within a double byte(x32 mode) or a single byte (x16 mode).
5) t_{DQDQO} also applies for CRC data from either WRITE or READ commands with CRC enabled, the EDC hold pattern, and the data strobe in RDQS mode.

Figure 28. READ Timing



MRA = Mode Register address and opcode ; BA = bank address ; CA = column address
$t_{WCK2CKPIN}$, t_{WCK2CK} and $t_{WCK2DQO}$ = 0 ns assumed

Figure 29. RDQS Mode Timings

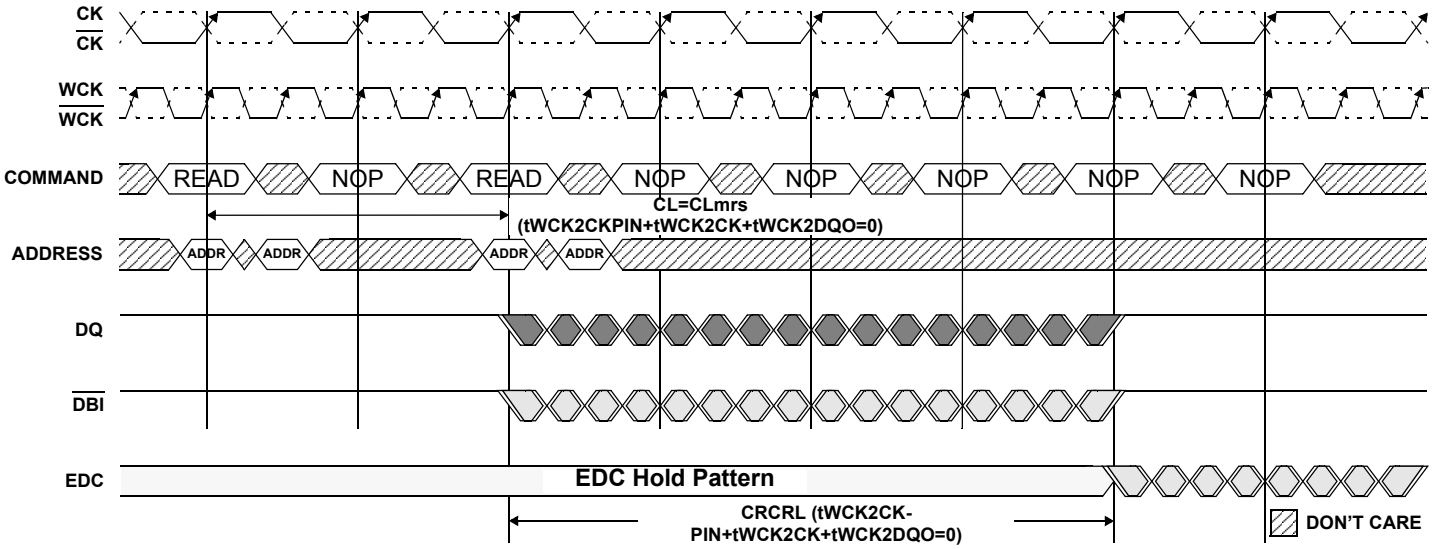


Figure 30. Consecutive READ to READ Timing

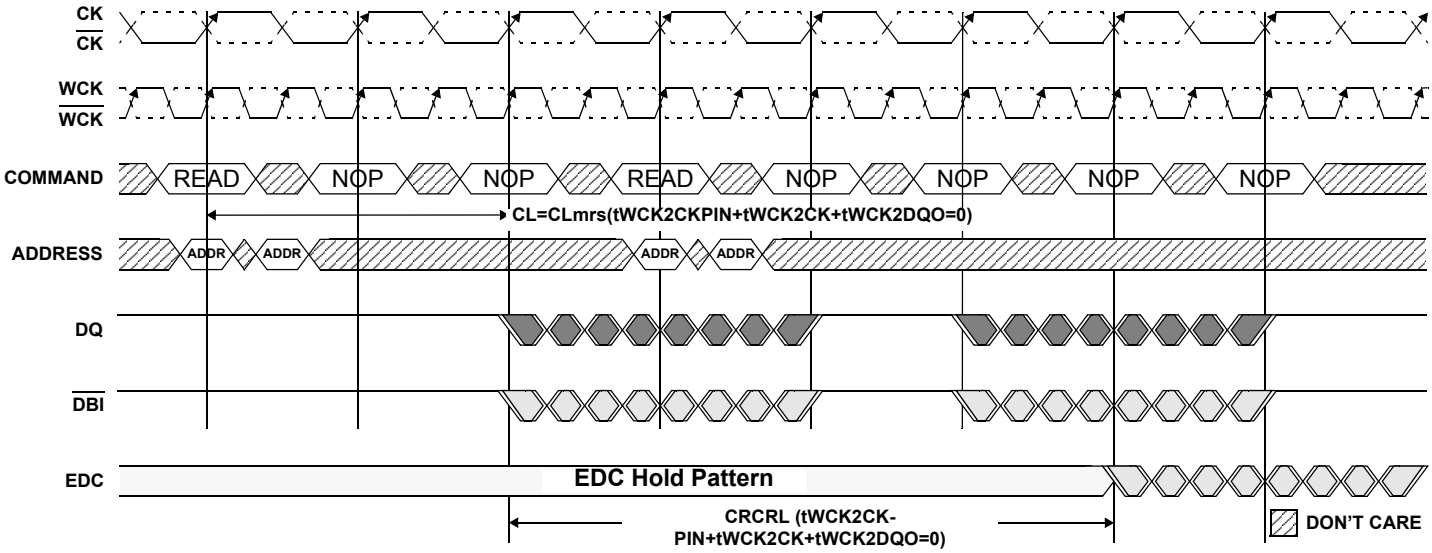


Figure 31. Non-Consecutive READ to READ Timing

17.7 WRITE

WRITE bursts are initiated with a WRITE command as shown in Figure WRITE. The bank and column addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after tRAS(min) has been met or after the number of clock cycles programmed in the RAS field of MR5 (bits A6-A11), depending on the implementation choice per DRAM vendor. The length of the burst initiated with a WRITE command is eight and the column address is unique for this burst of eight. There is no interruption nor truncation of WRITE bursts.

During WRITE bursts, the first valid data-in element must be available at the input latch after the Write Latency (WL). The Write Latency is defined as WLmrs * tCK + tWCK2CKPIN + tWCK2CK + tWCK2DQI, where WLmrs is the number of clock cycles programed in MR0, tWCK2CKPIN is the phase offset between WCK and CK at the pins when phase aligned at phase detector, tWCK2CK is the alignment error between WCK and CK at the GDDR5 SGRAM phase detector, and tWCK2DQI is the WCK to DQ/$\overline{DBI}$ offset as measured at the DRAM pins to ensure concurrent arrival at the latch. The total delay is relative to the data eye center averaged over one double-byte. The maximum skew within a double-byte is defined by tDQDQI.

The data input valid window, tDIVW, defines the time region when input data must be valid for reliable data capture at the receiver for any one worst-case channel. It accounts for jitter between data and clock at the latching point introduced in the path between the DRAM pads and the latching point. Any additional jitter introduced into the source signals (i.e. within the system before the DRAM pad) must be accounted for in the final timing budget together with the chosen PLL/DLL mode and bandwidth. tDIVW is measured at the pins. tDIVW is defined for the PLL/DLL off and on mode separately. In the case of PLL on, tDIVW must be specified for each supported bandwidth. In general tDIVW is smaller than tDIPW.

The data input pulse width, tDIPW, defines the minimum positive or negative input pulse width for any one worst-case channel required for proper propagation of an external signal to the receiver. tDIPW is measured at the pins. tDIPW is independent of the PLL/DLL mode. In general tDIPW is larger than tDIVW.

Upon completion of a burst, assuming no other WRITE data is expected on the bus the GDDR5 SGRAM DQ and $\overline{DBI}$ pins will be driven according to the ODT state. Any additional input data will be ignored. Data for any WRITE burst may not be truncated with a subsequent WRITE command.

Data from any WRITE burst may be concatenated with data from a subsequent WRITE command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new WRITE command should be issued after the previous WRITE command according to the tCCD timing. If that WRITE command is to another bank then an ACTIVE command must precede the WRITE command and tRCDWR also must be met.

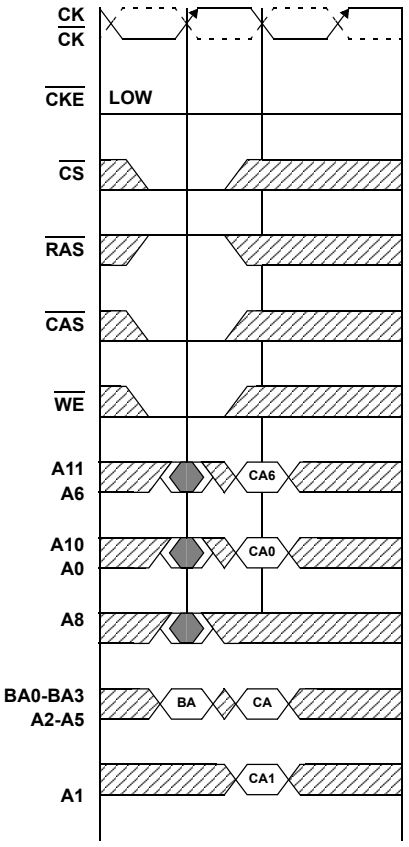
A READ can be issued any time after a WRITE command as long as the internal turn around time tWTR is met. If that READ command is to another bank, then an ACTIVE command must precede the READ command and tRCDRD also must be met.

A PRECHARGE can also be issued to the GDDR5 SGRAM with the same timing restriction as the new WRITE command if tRAS is met. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

The data inversion flag is received on the $\overline{DBI}$ pin to identify whether to store the true or inverted data. If $\overline{DBI}$ is LOW, the data will be stored after inversion inside the GDDR5 SGRAM and not inverted if $\overline{DBI}$ is HIGH. WRITE Data Inversion can be enabled (A9=0) or disabled (A9=1) using WDBI in MR1.

When enabled by the WRCRC flag in MR4, EDC data are returned to the controller with a latency of (WLmrs + CRCWL) * tCK + tWCK2CKPIN + tWCK2CK + tWCK2DQO, where CRCWL is the CRC Write latency programmed in MR4 and tWCK2DQO is the WCK to DQ/DBI/EDC phase offset at the DRAM pins.

WRITE(WOM/WSM/WDM)



RA: Row Address
CA: Column Address
BA: Bank Address
EN AP: Enable Auto Precharge
DIS AP: Disable Auto Precharge

DON'T CARE

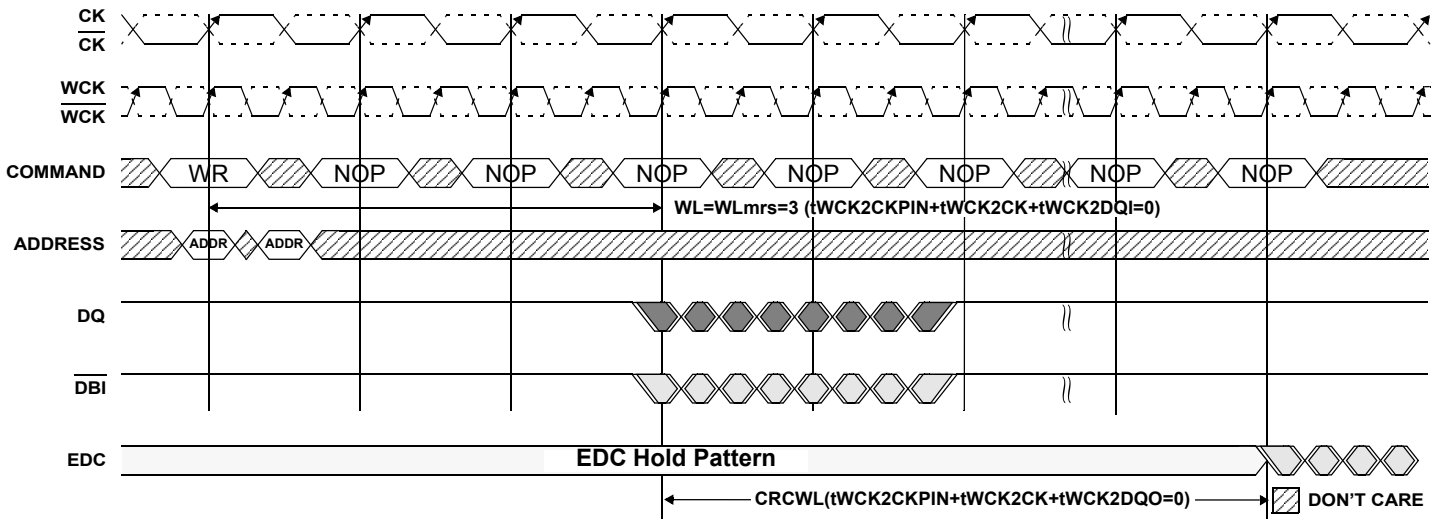
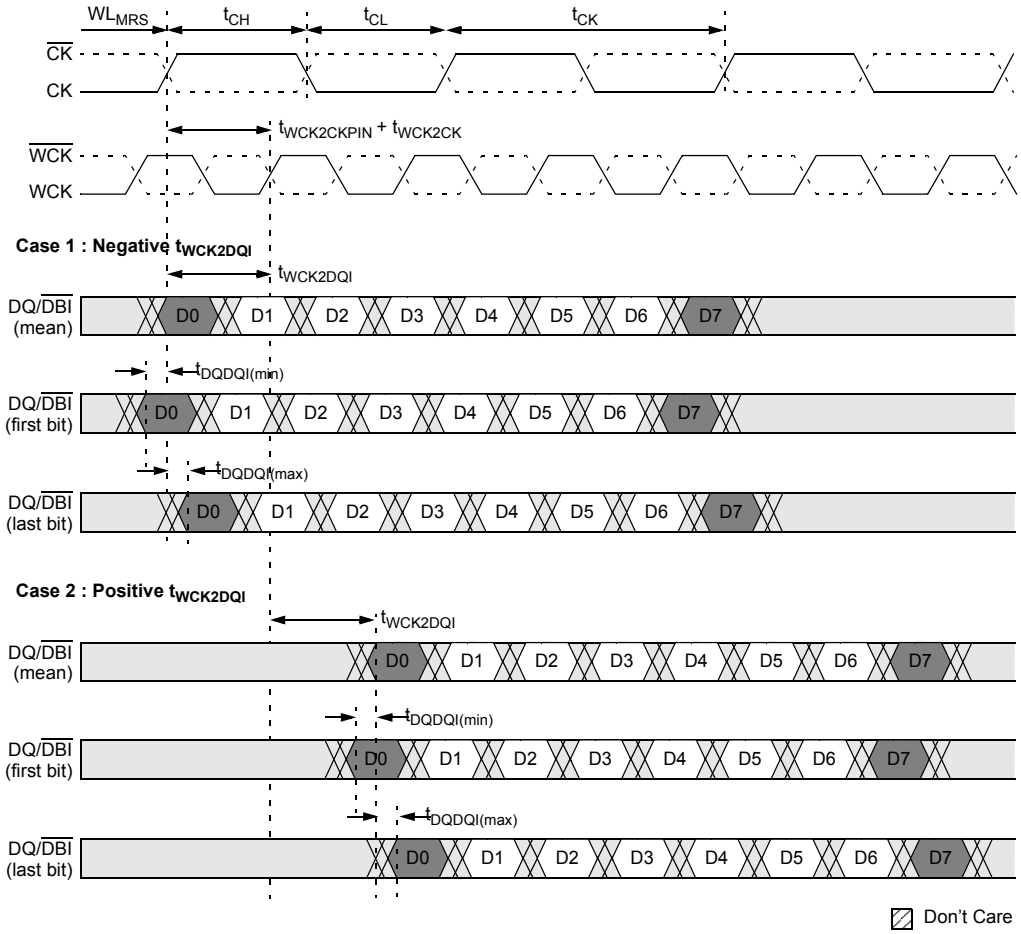


Figure 32. WRITE Timing



1) WL_{MRS} is the WRITE latency programmed in Mode Register MR0.
2) Timings are shown with positive $t_{WCK2CKPIN}$ and t_{WCK2CK} values. See WCK-to-CK timings for $t_{WCK2CKPIN}$ and t_{WCK2CK} ranges.
3) $t_{WCK2DQI}$ parameter values could be negative or positive numbers, depending on PLL-on-or PLL -off mode operation and design implementation. They also vary across PVT. Data training is required to determine the actual $t_{WCK2DQI}$ value for stable WRITE operation.
4) t_{DQDQI} defines the minimum to maximum variation of $t_{WCK2DQI}$ within a double byte(x32 mode) or a single byte (x16 mode).
5)Cf. Data Read timings for CRC return timing from WRITE commands with CRC enabled.

Figure 33. WRITE Timing

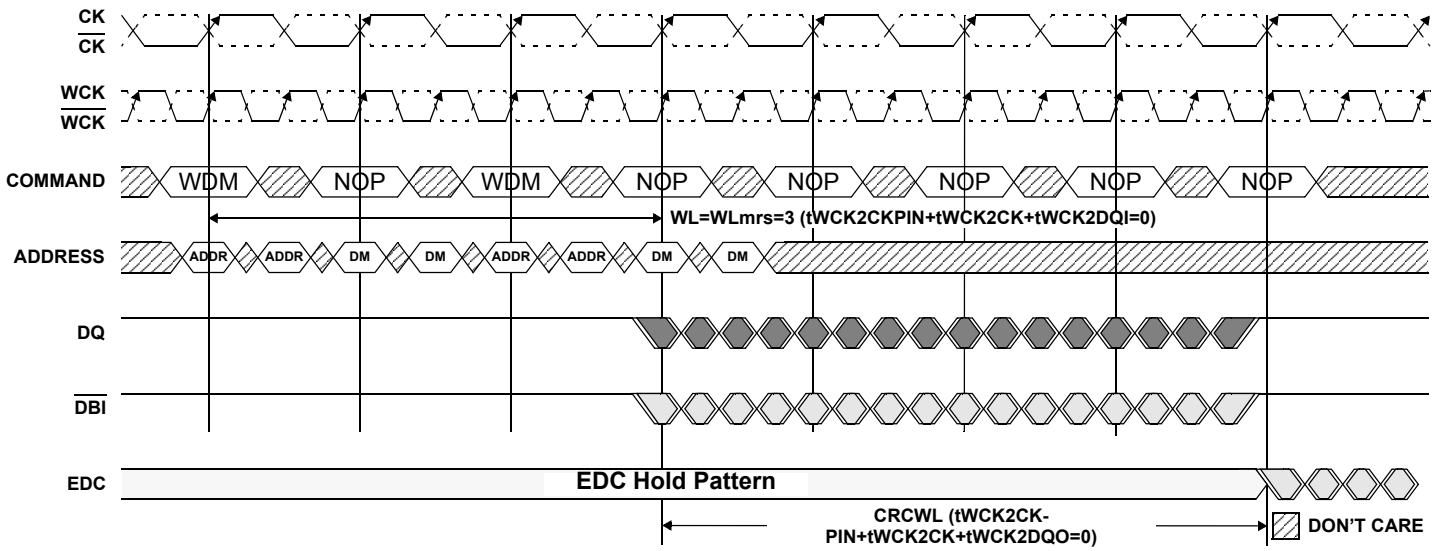


Figure 34. WRITE with Double Byte Mask

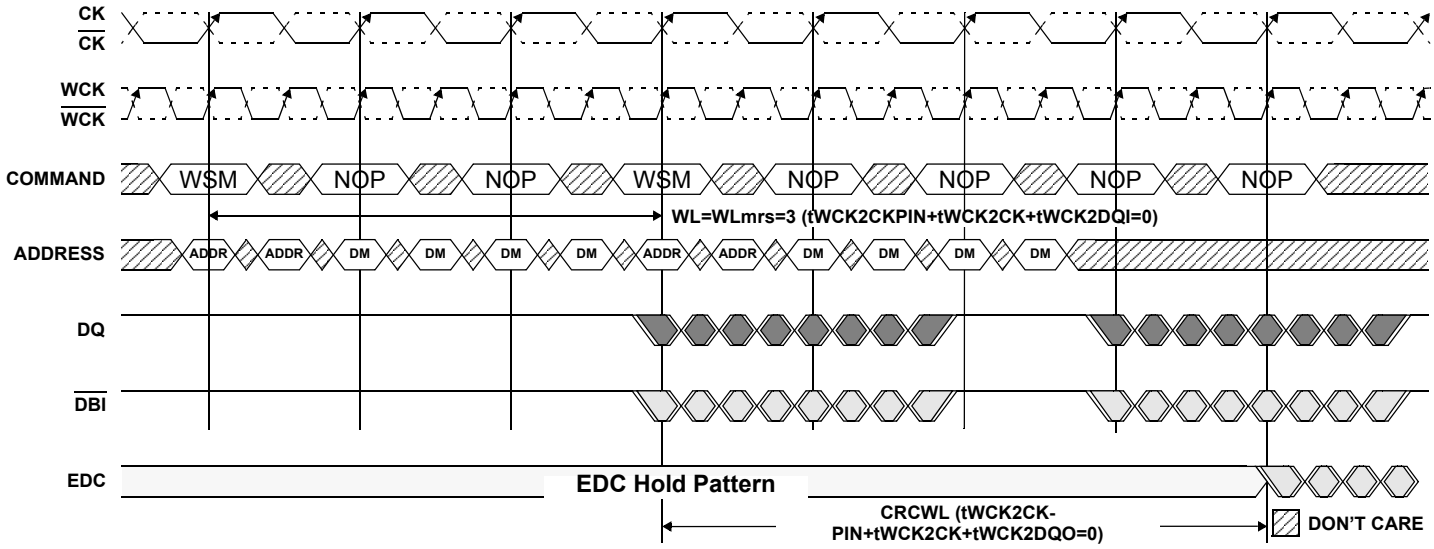


Figure 35. WRITE with Single Byte Mask

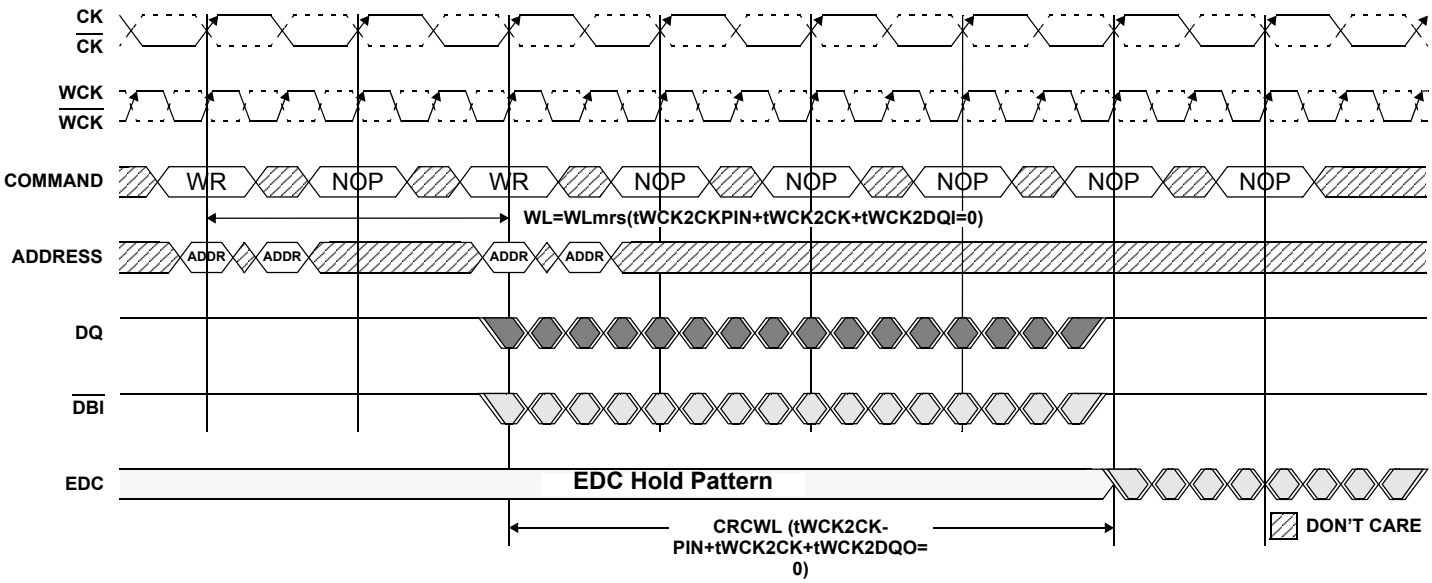


Figure 36. Consecutive WRITE to WRITE Timing

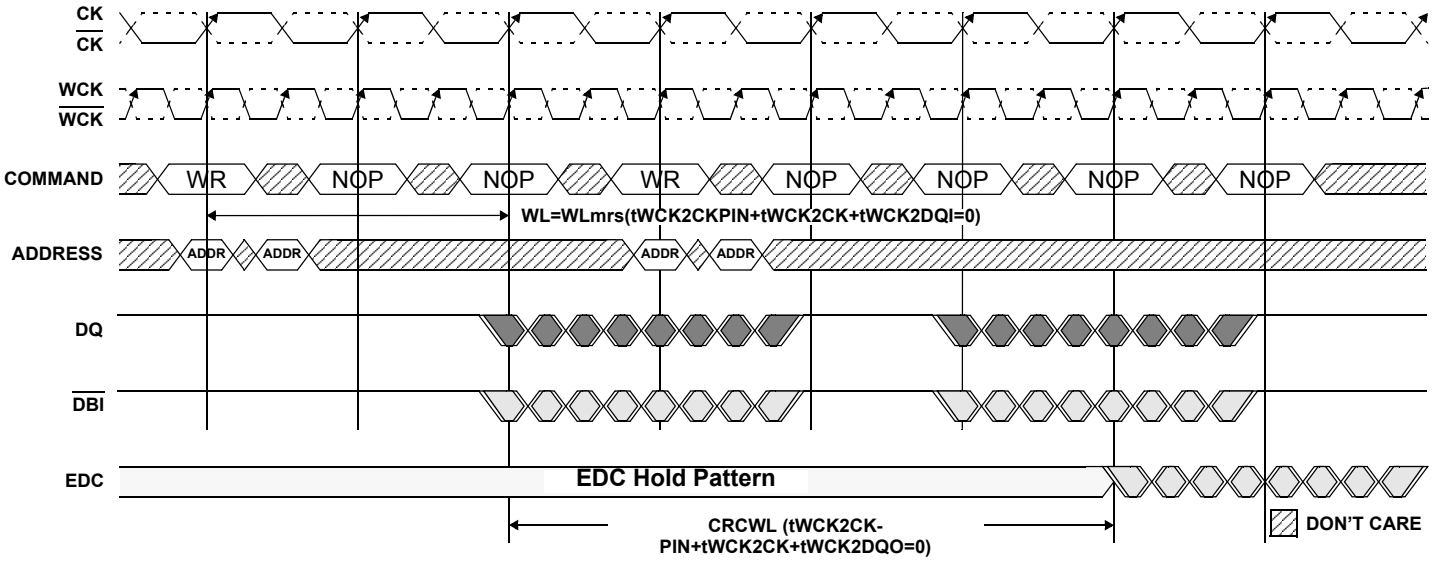


Figure 37. Non-Consecutive WRITE to WRITE Timing

17.8 WRITE Data Mask on Address Pins (DM)

The traditional method of using a DM pin for WRITE data mask must be abandoned for a new method. Due to the high data rate of GDDR5 SGRAMs, errors are expected on the interface and are not recoverable when they occur on the traditional
DM pin. In GDDR5 the DM is sent to the DRAM over the address bus during the NOPs between the WRITE command and the next command. The DM is used to mask the corresponding data according to the following table.

DM State

Function	DM Value	DQ
Write Enable	0	Valid
Write Inhibit	1	X

Three WRITE commands are required for proper DM support:

WOM: WRITE Without Mask
1 cycle command which is equivalent to a WRITE command for non-GDDR5 where the address pins only carry the WRITE address;

WDM: WRITE-With-Doublebyte-Mask
2 cycle command where the 1st cycle carries address information and the 2nd cycle carries data mask information (2 byte granularity);

WSM: WRITE-With-Singlebyte-Mask
3 cycle command where the 1st cycle carries address information, the 2nd and 3rd cycle carry data mask information

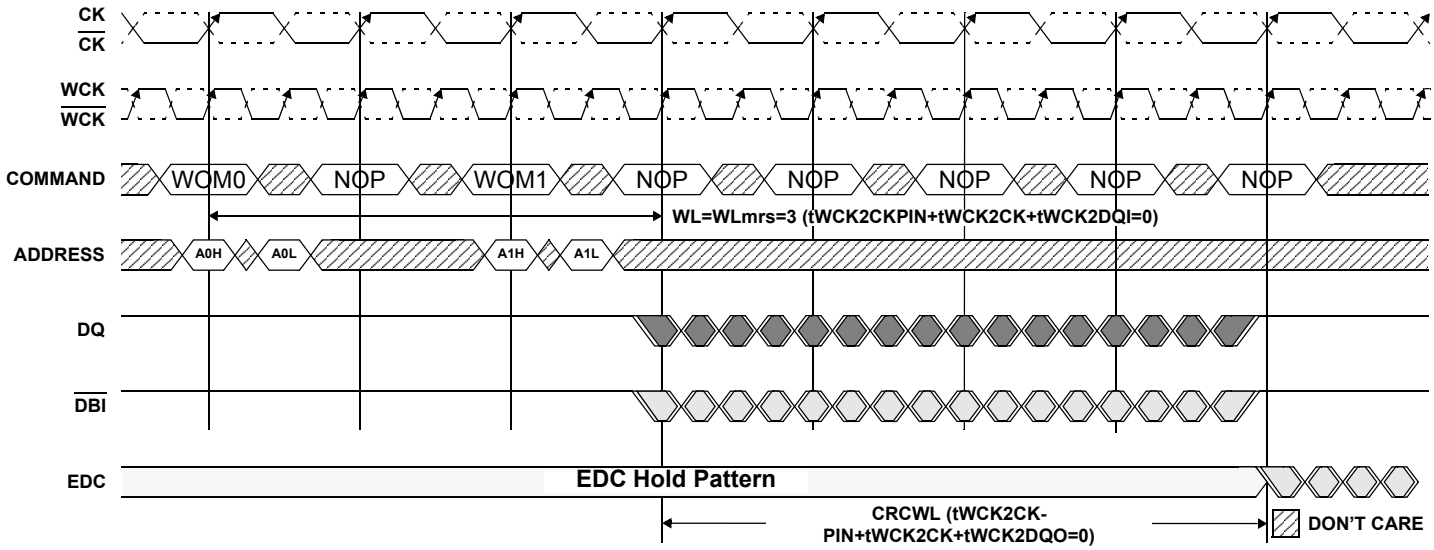


Figure 38. WOM : WRITE without Mask

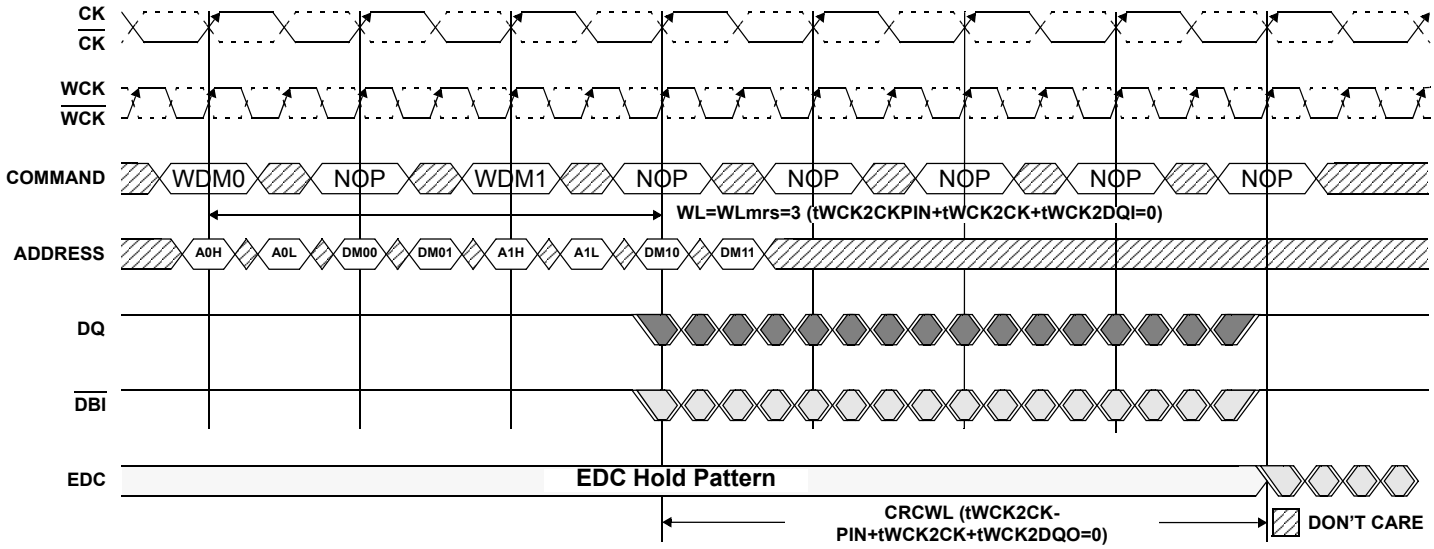


Figure 39. WDM : WRITE with Double Byte Mask

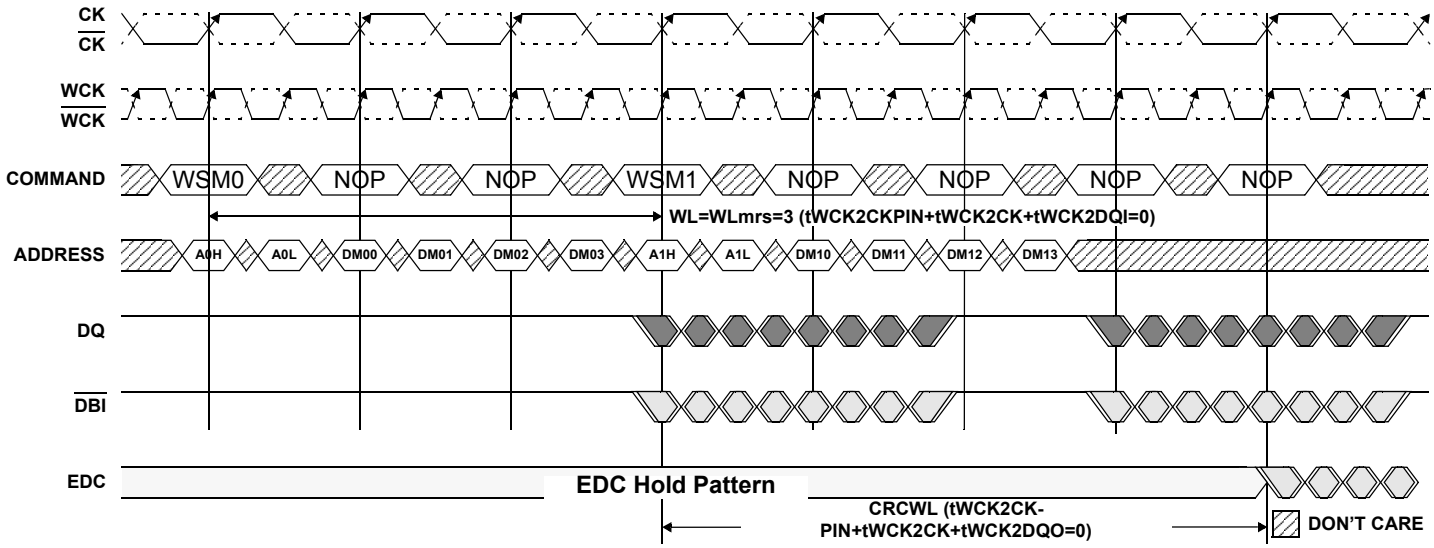


Figure 40. WSM : WRITE with Single Byte Mask

[Table 13] WDM Mapping for mirrored and non-mirrored x32 Mode

Byte and Burst Position Masked during WDM					
Address	Address CK rising edge		Address	Address $\overline{CK}$ rising edge	
	Byte	Burst		Byte	Burst
A10	DQ[15:0]	0	A0	DQ[15:0]	4
A9	DQ[15:0]	1	A1	DQ[15:0]	5
BA0	DQ[15:0]	2	A2	DQ[15:0]	6
BA3	DQ[15:0]	3	A3	DQ[15:0]	7
BA2	DQ[31:16]	0	A4	DQ[31:16]	4
BA1	DQ[31:16]	1	A5	DQ[31:16]	5
A11	DQ[31:16]	2	A6	DQ[31:16]	6
A8	DQ[31:16]	3	A7	DQ[31:16]	7

[Table 14] WDM Mapping for non-mirrored x16 Mode

Byte and Burst Position Masked during WDM					
Address	Address CK rising edge		Address	Address $\overline{CK}$ rising edge	
	Byte	Burst		Byte	Burst
A10	DQ[7:0]	0	A0	DQ[7:0]	4
A9	DQ[7:0]	1	A1	DQ[7:0]	5
BA0	DQ[7:0]	2	A2	DQ[7:0]	6
BA3	DQ[7:0]	3	A3	DQ[7:0]	7
BA2	DQ[23:16]	0	A4	DQ[23:16]	4
BA1	DQ[23:16]	1	A5	DQ[23:16]	5
A11	DQ[23:16]	2	A6	DQ[23:16]	6
A8	DQ[23:16]	3	A7	DQ[23:16]	7

[Table 15] WDM Mapping for mirrored x16 Mode

Byte and Burst Position Masked during WDM					
Address	Address CK rising edge		Address	Address $\overline{CK}$ rising edge	
	Byte	Burst		Byte	Burst
A10	DQ[15:8]	0	A0	DQ[15:8]	4
A9	DQ[15:8]	1	A1	DQ[15:8]	5
BA0	DQ[15:8]	2	A2	DQ[15:8]	6
BA3	DQ[15:8]	3	A3	DQ[15:8]	7
BA2	DQ[31:24]	0	A4	DQ[31:24]	4
BA1	DQ[31:24]	1	A5	DQ[31:24]	5
A11	DQ[31:24]	2	A6	DQ[31:24]	6
A8	DQ[31:24]	3	A7	DQ[31:24]	7

[Table 16] WSM Mapping for mirrored and non-mirrored x32 Mode

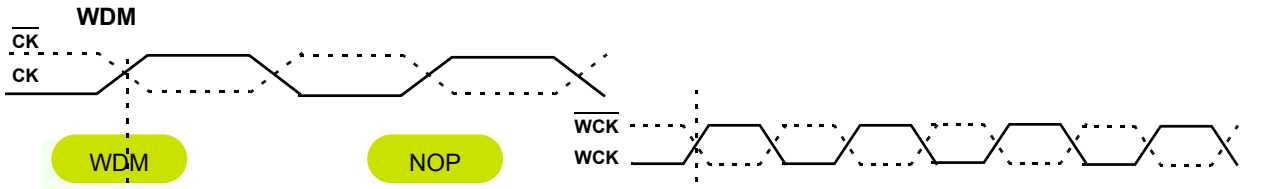
Byte and Burst Position Masked during WSM											
Address	Address CK 1st rising edge		Address	Address $\overline{CK}$ 1st rising edge		Address	Address CK 2nd rising edge		Address	Address $\overline{CK}$ 2nd rising edge	
	Byte	Burst		Byte	Burst		Byte	Burst		Byte	Burst
A10	DQ[7:0]	0	A0	DQ[7:0]	4	A10	DQ[15:8]	0	A0	DQ[15:8]	4
A9	DQ[7:0]	1	A1	DQ[7:0]	5	A9	DQ[15:8]	1	A1	DQ[15:8]	5
BA0	DQ[7:0]	2	A2	DQ[7:0]	6	BA0	DQ[15:8]	2	A2	DQ[15:8]	6
BA3	DQ[7:0]	3	A3	DQ[7:0]	7	BA3	DQ[15:8]	3	A3	DQ[15:8]	7
BA2	DQ[23:16]	0	A4	DQ[23:16]	4	BA2	DQ[31:24]	0	A4	DQ[31:24]	4
BA1	DQ[23:16]	1	A5	DQ[23:16]	5	BA1	DQ[31:24]	1	A5	DQ[31:24]	5
A11	DQ[23:16]	2	A6	DQ[23:16]	6	A11	DQ[31:24]	2	A6	DQ[31:24]	6
A8	DQ[23:16]	3	A7	DQ[23:16]	7	A8	DQ[31:24]	3	A7	DQ[31:24]	7

[Table 17] WSM Mapping for non-mirrored x16 Mode

Byte and Burst Position Masked during WSM											
Address	Address CK 1st rising edge		Address	Address $\overline{CK}$ 1st rising edge		Address	Address CK 2nd rising edge		Address	Address $\overline{CK}$ 2nd rising edge	
	Byte	Burst		Byte	Burst		Byte	Burst		Byte	Burst
A10	DQ[7:0]	0	A0	DQ[7:0]	4		-			-	
A9	DQ[7:0]	1	A1	DQ[7:0]	5		-			-	
BA0	DQ[7:0]	2	A2	DQ[7:0]	6		-			-	
BA3	DQ[7:0]	3	A3	DQ[7:0]	7		-			-	
BA2	DQ[23:16]	0	A4	DQ[23:16]	4		-			-	
BA1	DQ[23:16]	1	A5	DQ[23:16]	5		-			-	
A11	DQ[23:16]	2	A6	DQ[23:16]	6		-			-	
A8	DQ[23:16]	3	A7	DQ[23:16]	7		-			-	

[Table 18] WSM Mapping for mirrored x16 Mode

Byte and Burst Position Masked during WSM											
Address	Address CK 1st rising edge		Address	Address $\overline{CK}$ 1st rising edge		Address	Address CK 2nd rising edge		Address	Address $\overline{CK}$ 2nd rising edge	
	Byte	Burst		Byte	Burst		Byte	Burst		Byte	Burst
	-			-		A10	DQ[15:8]	0	A0	DQ[15:8]	4
	-			-		A9	DQ[15:8]	1	A1	DQ[15:8]	5
	-			-		BA0	DQ[15:8]	2	A2	DQ[15:8]	6
	-			-		BA3	DQ[15:8]	3	A3	DQ[15:8]	7
	-			-		BA2	DQ[31:24]	0	A4	DQ[31:24]	4
	-			-		BA1	DQ[31:24]	1	A5	DQ[31:24]	5
	-			-		A11	DQ[31:24]	2	A6	DQ[31:24]	6
	-			-		A8	DQ[31:24]	3	A7	DQ[31:24]	7



Command		Address Burst Position		Data Burst Position							
0	1	2	3	0	1	2	3	4	5	6	7
		A10		[15:0]							
		A9			[15:0]						
		BA0				[15:0]					
BA3	A3	BA3					[15:0]				
BA2	A4	BA2		[31:16]							
BA1	A5	BA1			[31:16]						
A11	A6	A11				[31:16]					
BA0	A2	A8					[31:16]				
A10	A0		A0					[15:0]			
A9	A1		A1						[15:0]		
A8	A7		A2							[15:0]	
			A3								[15:0]
			A4					[31:16]			
			A5						[31:16]		
			A6							[31:16]	
			A7								[31:16]
CA	CA	DM	DM	DQ	DQ	DQ	DQ	DQ	DQ	DQ	DQ

WSM

Command		Address Burst Position				Data Burst Position							
0	1	2	3	4	5	0	1	2	3	4	5	6	7
		A10				[7:0]							
		A9					[7:0]						
		BA0						[7:0]					
		BA3							[7:0]				
		BA2				[23:16]							
		BA1					[23:16]						
		A11						[23:16]					
		A8							[23:16]				
			A0							[7:0]			
			A1								[7:0]		
			A2									[7:0]	
BA3	A3		A3										[7:0]
BA2	A4		A4							[23:16]			
BA1	A5		A5								[23:16]		
A11	A6		A6									[23:16]	
BA0	A2		A7										[23:16]
A10	A0			A10		[15:8]							
A9	A1			A9			[15:8]						
A8	A7			BA0				[15:8]					
				BA3					[15:8]				
				BA2		[31:24]							
				BA1			[31:24]						
				A11				[31:24]					
				A8					[31:24]				
					A0					[15:8]			
					A1						[15:8]		
					A2							[15:8]	
					A3								[15:8]
					A4					[31:24]			
					A5						[31:24]		
					A6							[31:24]	
					A7								[31:24]
CA	CA	DM	DM	DM	DM	DQ	DQ	DQ	DQ	DQ	DQ	DQ	DQ

Figure 41. GDDR5 DM to DQ Mapping

17.9 Precharge (PRE)

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued.

Input address, A8 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, inputs BA0-BA3 select the bank. Otherwise BA0-BA3 are treated as "Don't Care".

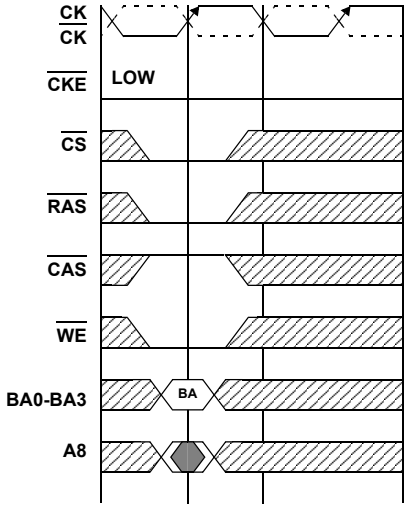
Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

17.10 AUTO Precharge

Auto Precharge is a feature which performs the same individual bank precharge function as described below, but without requiring an explicit command. This is accomplished by using A8 (A8=HIGH), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto Precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto Precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharging time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time.

PRECHARGE



RA: Row Address
CA: Column Address
BA: Bank Address
EN AP: Enable Auto Precharge
DIS AP: Disable Auto Precharge

DON'T CARE

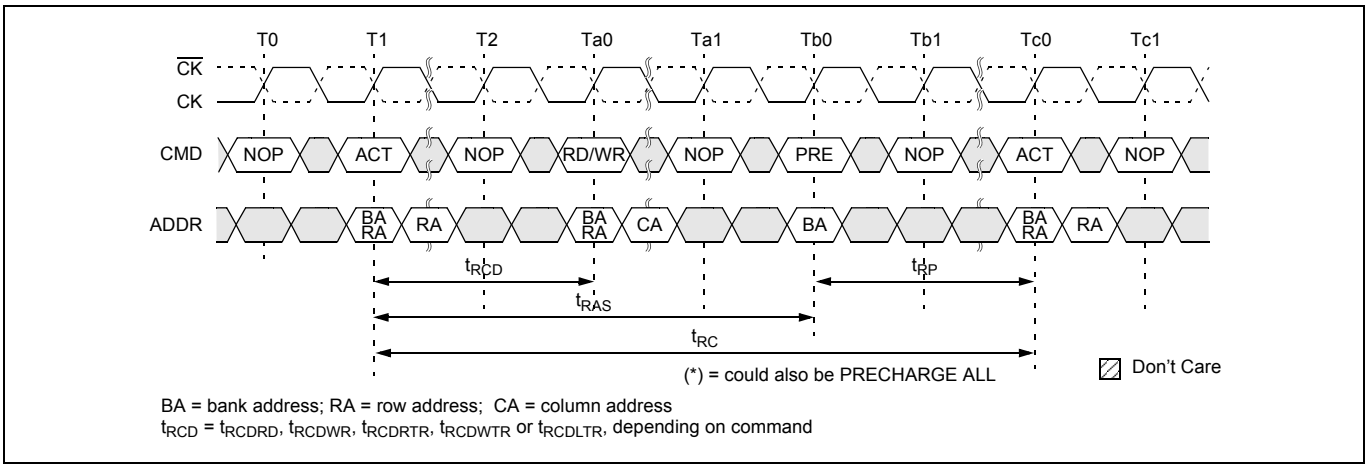


Figure 42. Active - Precharge Timings

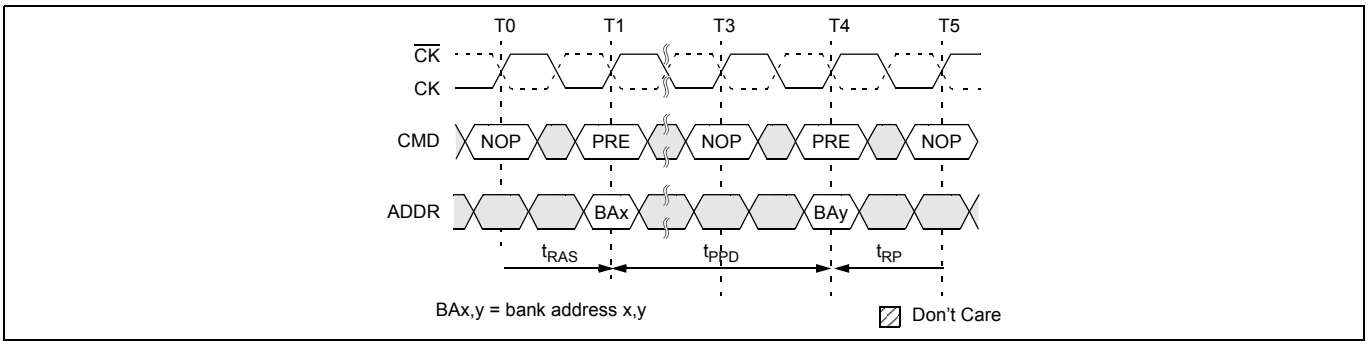
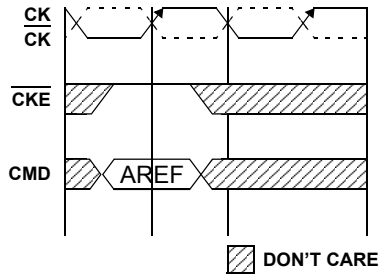


Figure 43. t_{PPD}

17.11 Power Down (PDN)

GDDR5 DRAM require $\overline{CKE}$ to be active at all times that an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined when the read postamble is satisfied; For WRITEs, a burst completion is defined when the write postamble is satisfied.
Power down mode is entered when $\overline{CKE}$ is registered HIGH. If power down occurs when all banks are idle, this mode is referred to as precharge power-down; if power down occurs when there is a row active in any banks, this mode is referred to as active power-down. Entering power down mode deactivates the input and output buffers, excluding CK, $\overline{CK}$, WCK, $\overline{WCK}$, EDC pins, RESET, and $\overline{CKE}$. While in power down, $\overline{CKE}$ HIGH and a stable clock signal must be maintained at the inputs of GDDR5 DRAM while all other input signals are "Don't Care."
For maximum power savings, the user has the option of disabling the PLL/DLL prior to entering POWER-DOWN. In that case, on exiting POWER-DOWN, WCK2CK training is required to set the internal synchronizers which will include the enabling of the PLL/DLL, PLL/DLL reset, and tLK clock cycles must occur before any READ or WRITE command can be issued.

Power Down



* AREF with $\overline{CKE}$ HIGH is SELF REFRESH

While in power-down, $\overline{CKE}$ HIGH and stable CK and WCK signals must be maintained at the device inputs. The EDC pins continuously drive the EDC hold pattern; if the controller does not require CDR, users may program the EDC hold pattern to '1111' prior to entering power-down mode. POWER-DOWN duration is limited by the refresh requirements of the device.
The POWER-DOWN state is synchronously exited when $\overline{CKE}$ is registered LOW (in conjunction with a NOP or DESELECT command). A valid executable command may be applied tXPN cycles later. The min. power-down duration is specified by tPD.

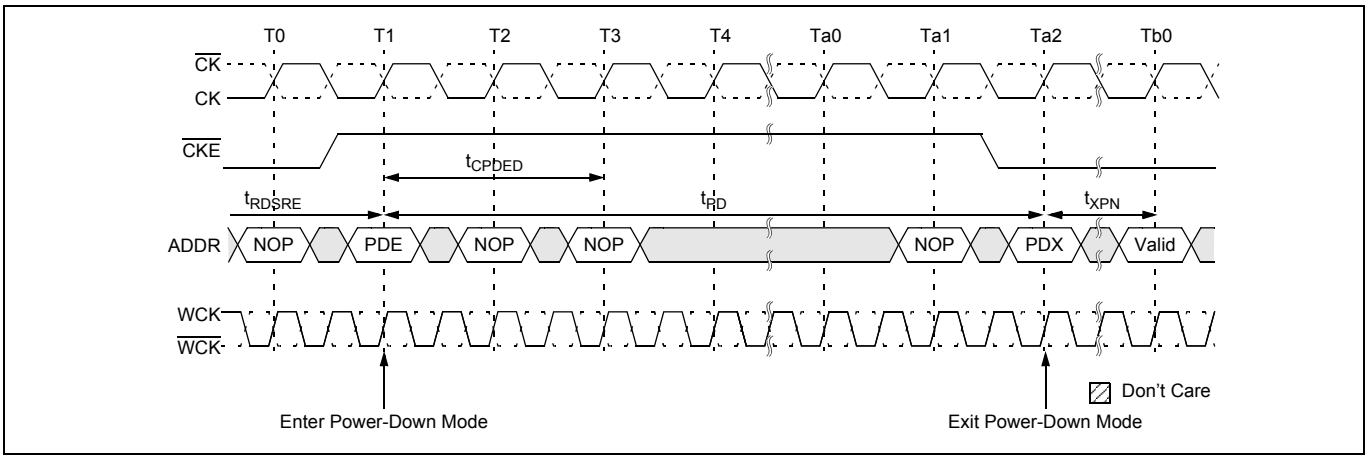


Figure 44. Power-Down Entry and Exit

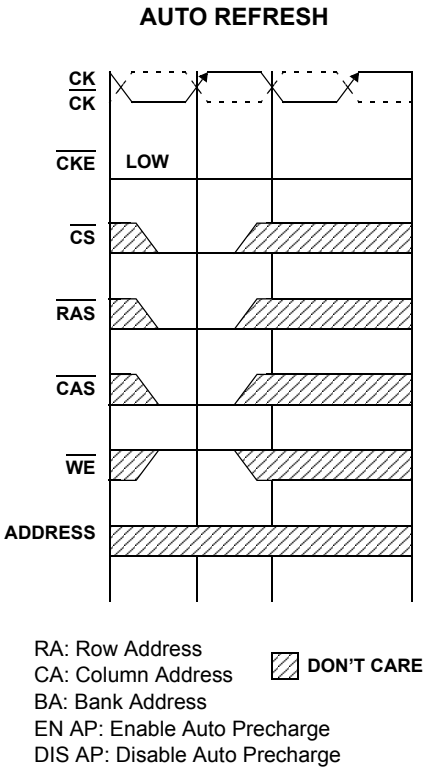
17.12 AUTO Refresh (AREF)

The REFRESH command is used during normal operation of the GDDR5 SGRAM. The command is non persistent, so it must be issued each time a refresh is required. A minimum time t_{RFC} is required between two REFRESH commands. The same rule applies to any access command after the refresh operation. All banks must be precharged prior to the REFRESH command.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during a REFRESH command. The GDDR5 SGRAM requires REFRESH cycles at an average periodic interval of t_{REFI}(max). To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to the GDDR5 SGRAM, and the maximum absolute interval between any REFRESH command and the next REFRESH command is 9*t_{REFI}.

During REFRESH, and when bit A2 in MR5 is set to 0, WRTR, RDTR, and LDFF commands are allowed at time t_{REFTR} after the REFRESH command, which enable (incremental) data training to occur in parallel with the internal refresh operation and thus without loss of performance on the interface. See READ Training and WRITE Training for details.

As impedance updates from the auto-calibration engine may occur with any REFRESH command, it is safe to only issue NOP commands during t_{KO} period to prevent false command, address or data latching resulting from impedance updates.



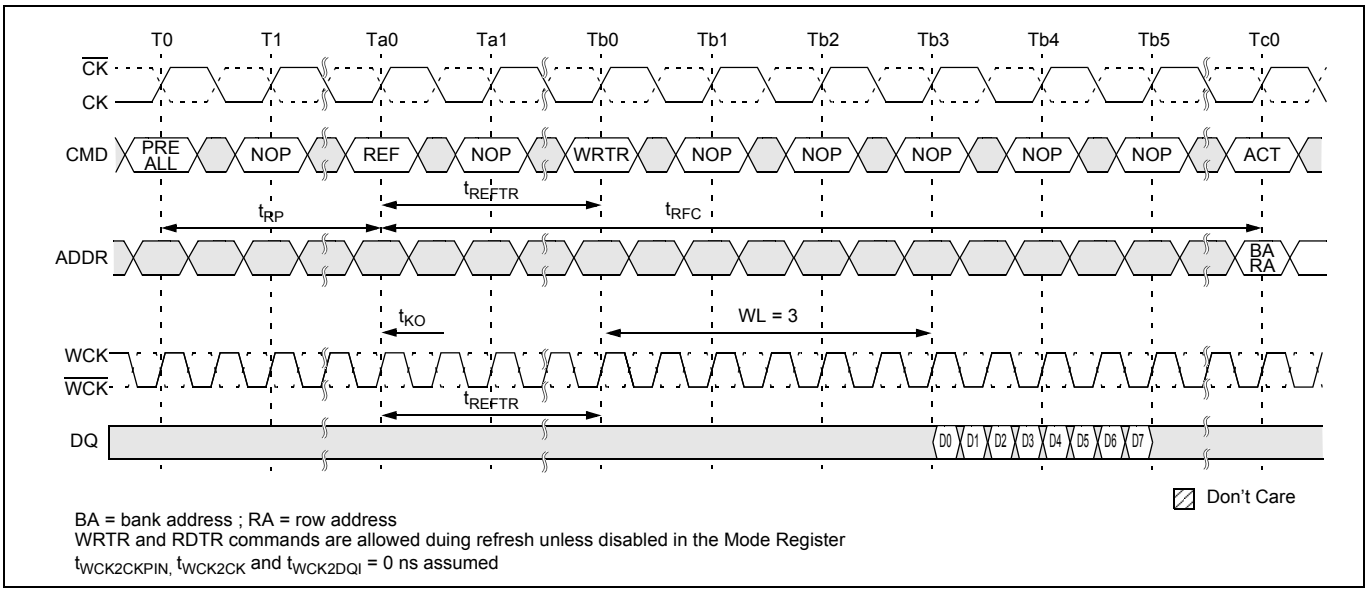


Figure 45. Auto Refresh

17.13 Self-Refresh

Self-Refresh can be used to retain data in the GDDR5 SGRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the GDDR5 SGRAM retains data without external clocking. The SELF REFRESH ENTRY command is initiated like a REFRESH command except that $\overline{CKE}$ is pulled HIGH. SELF REFRESH ENTRY is only allowed when all banks are prchaged with t_{RP} satisfied, and when the last data element or CRC data element from a preceding READ or WRITE command have been pushed out(t_{RDSRE} or t_{WRSRE}). NOP commands are required until t_{CKSRE} is met after the entering Self-Refresh. The PLL/DLL is automatically disabled upon entering Self-Refresh and is automatically enabled and reset upon exiting Self-Refresh. If the GDDR5 SGRAM enters Self-Refresh with the PLL/DLL disabled, it will exit Self-Refresh with the PLL/DLL disabled.

Once the SELF REFRESH ENTRY command is registered, $\overline{CKE}$ must be held HIGH to keep the device in Self-Refresh mode. When the device has entered the Self-Refresh mode, all external control signals, except $\overline{CKE}$ and $\overline{RESET}$ are "Don't care". For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VREFC, VREFD) must be at valid levels. The GDDR5 SGRAM initiates a minimum of one internal refresh within t_{CKE} period once it enters Self-Refresh mode. The address, command, data and WCK pins are in ODT state, and the EDC pins drive a HIGH.

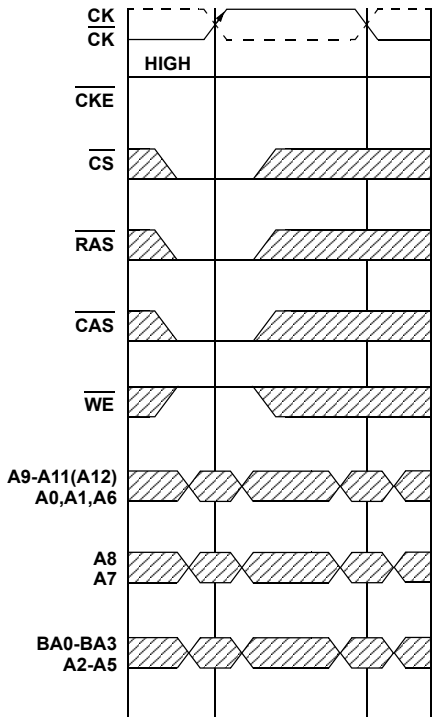
The clock is internally disabled during Self-Refresh operation to save power. The minimum time that the GDDR5 SGRAM must remain in Self-Refresh mode is t_{CKE}. The user may change the external clock frequency or halt the external CK and WCK clocks t_{CKSRE} after Self-Refresh entry is registered. However, the clocks must be restarted and stable t_{CKSRX} before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the CK and WCK clocks must be stable prior to $\overline{CKE}$ going back LOW.WCK clocks could be on or off at self refresh exit depending on the preferred method for resetting the WCK by two divider in WCK2CK training which is required upon self refresh exit. For frequency supported by each method, the vendor datasheet should be consulted. A delay of at least t_{XS} must be satisfied before a valid command can be issued to the device to allow for completion of any internal refresh in progress.

During self-Refresh the on-die termination (ODT) and driver will not be auto-calibrated. Therefore, it is recommended that the ODT and driver be recalibrated by the controller upon exiting Self-Refresh. Alternatively, if changes in voltage and temperature are tracked or known to be bounded then the vendor provided Voltage and Temperature Variation tables may be consulted to determine if recalibration is necessary.

Upon exit from Self-Refresh, the GDDR5 SGRAM can be put back into Self-Refresh mode after waiting at least t_{XS} period and issuing one extra REFRESH command.

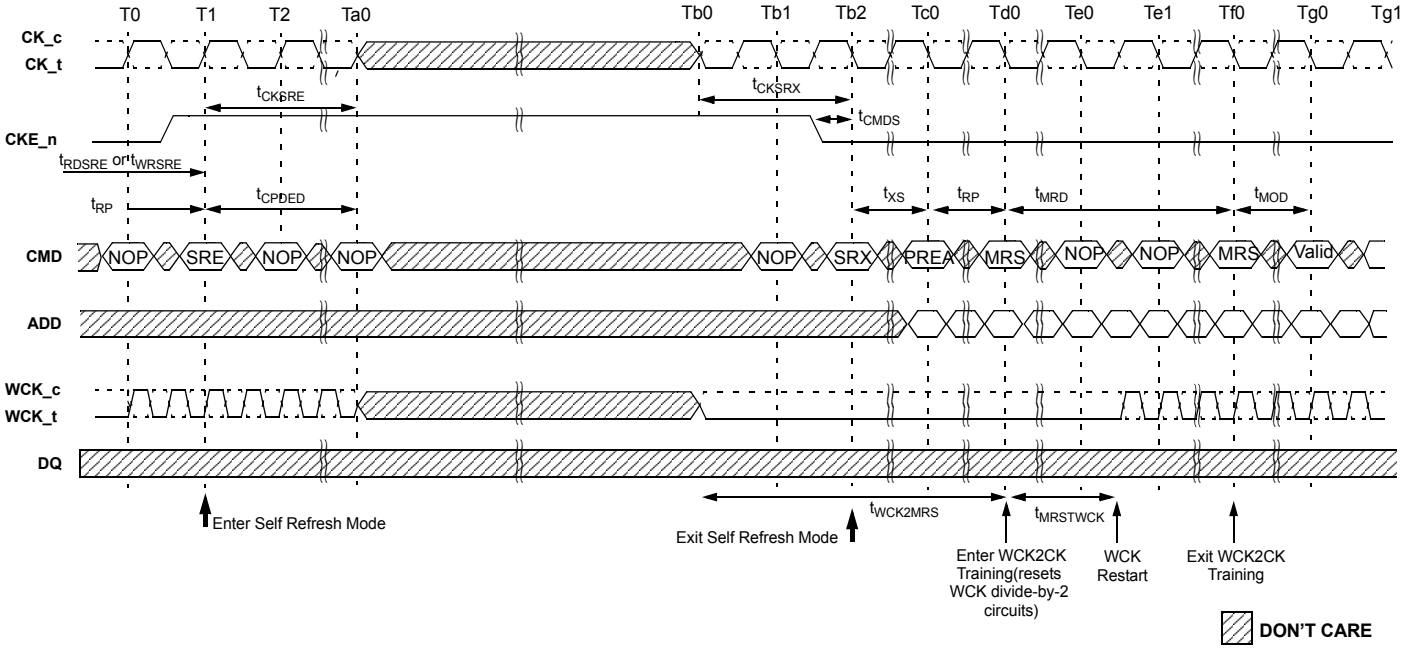
Self-Refresh



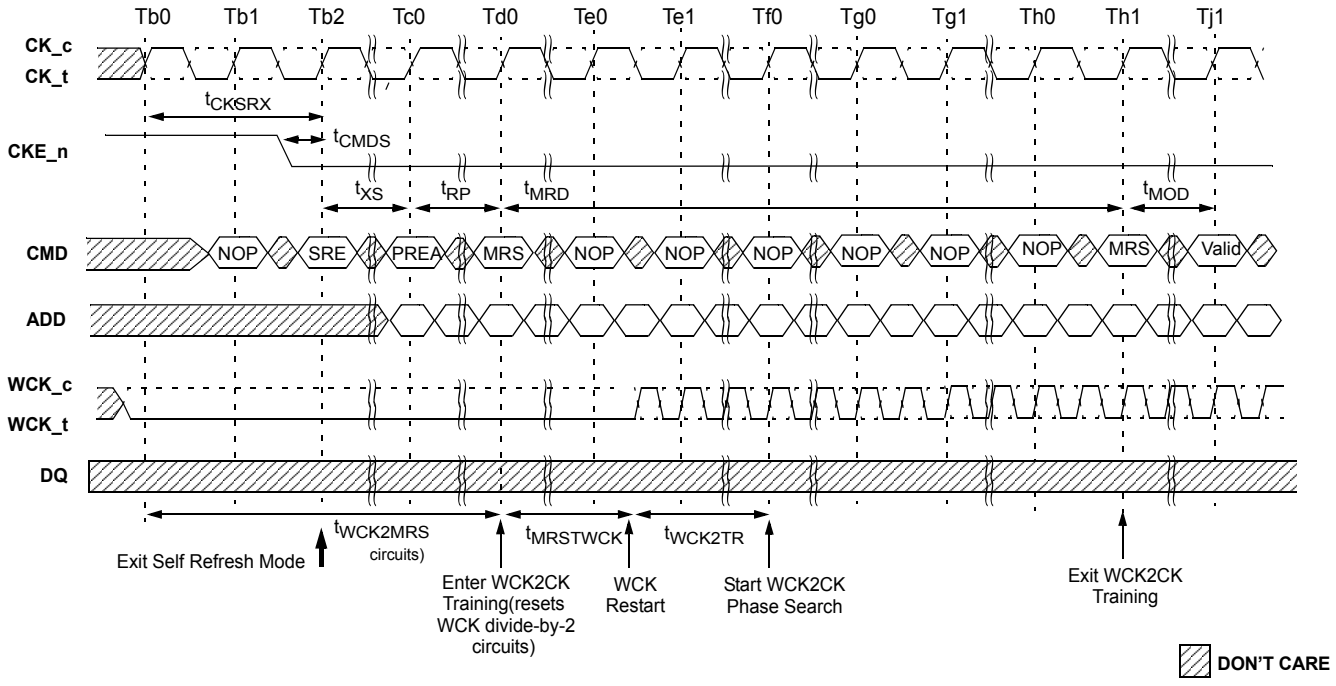
RA: Row Address
CA: Column Address
BA: Bank Address
EN AP: Enable Auto Precharge
DIS AP: Disable Auto Precharge

DON'T CARE

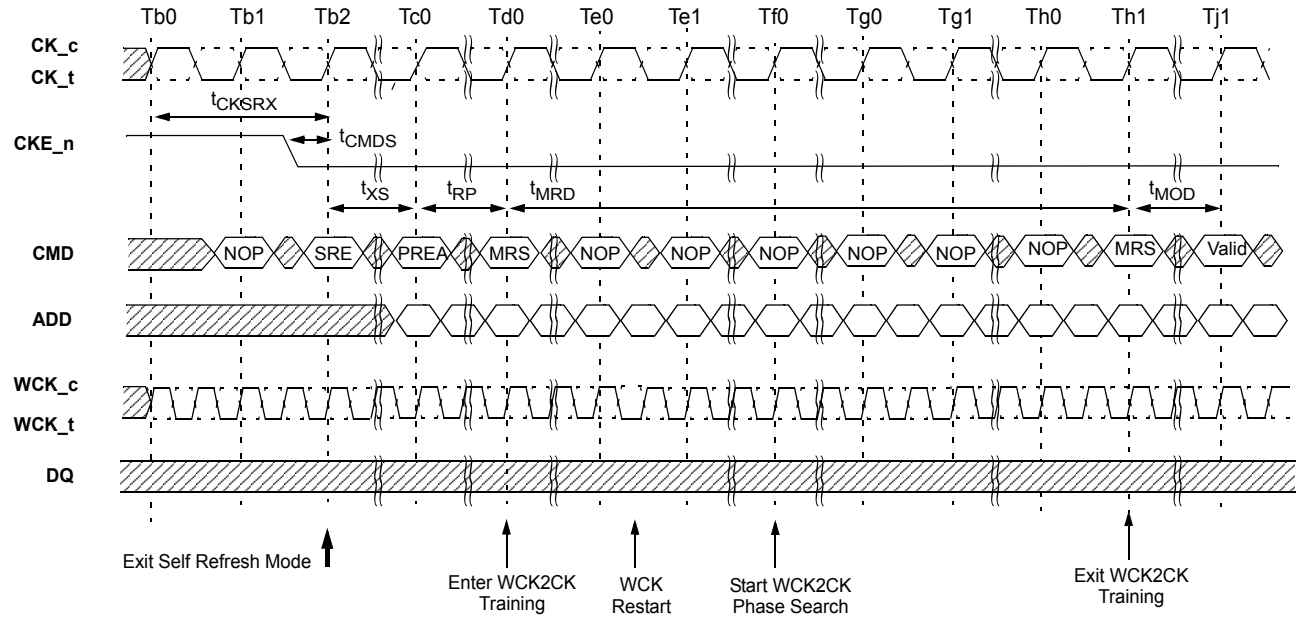
A. SRE and SRX with only WCK clock stop



B. SRX with WCK clock stop and phase Seach



C. SRX without WCK clock stop



1. At least one REFRESH command shall be issued after t_{XS} for output driver and termination impedance updates.

DON'T CARE

Figure 46. Self Refresh Entry and Exit

[Table 19] Pin States During Self Refresh

Pin	State
EDC	High
DQ/$\overline{\text{DBI}}$	ODT
ADR/CMD	ODT
$\overline{\text{CKE}}$	ODT (Driven High by Controller)
WCK/$\overline{\text{WCK}}$	ODT

17.14 Data Bus Inversion (DBI)

The GDDR5 SGRAM Data Bus Inversion (DBIdc) reduces the DC power consumption on data pins, as the number of DQ lines driving a low level can be limited to 4 within a byte. DBIdc is evaluated per byte.

There is one $\overline{DBI}$ pin per byte: $\overline{DBI0}$ is associated with DQ0-DQ7, DBI1 with DQ8-DQ15, $\overline{DBI2}$ with DQ16-DQ23 and $\overline{DBI3}$ with DQ24-DQ31. The $\overline{DBI}$ pins are bidirectional active Low double data rate (DDR) signals. For Writes, they are sampled by the GDDR5 SGRAM along with the DQ of the same byte. For Reads, they are driven by the GDDR5 SGRAM along with the DQ of the same byte.

Once enabled by the corresponding RDBI Mode Register bit, the GDDR5 SGRAM inverts read data and sets $\overline{DBI}$ Low, when the number of '0' data bits within a byte is greater than 4; otherwise the GDDR5 SGRAM does not invert the read data and sets $\overline{DBI}$ High.

Once enabled by the corresponding WDBI Mode Register bit, the GDDR5 SGRAM inverts write data received on the DQ inputs in case $\overline{DBI}$ was sampled Low, or leaves the data non-inverted in case $\overline{DBI}$ was sampled High

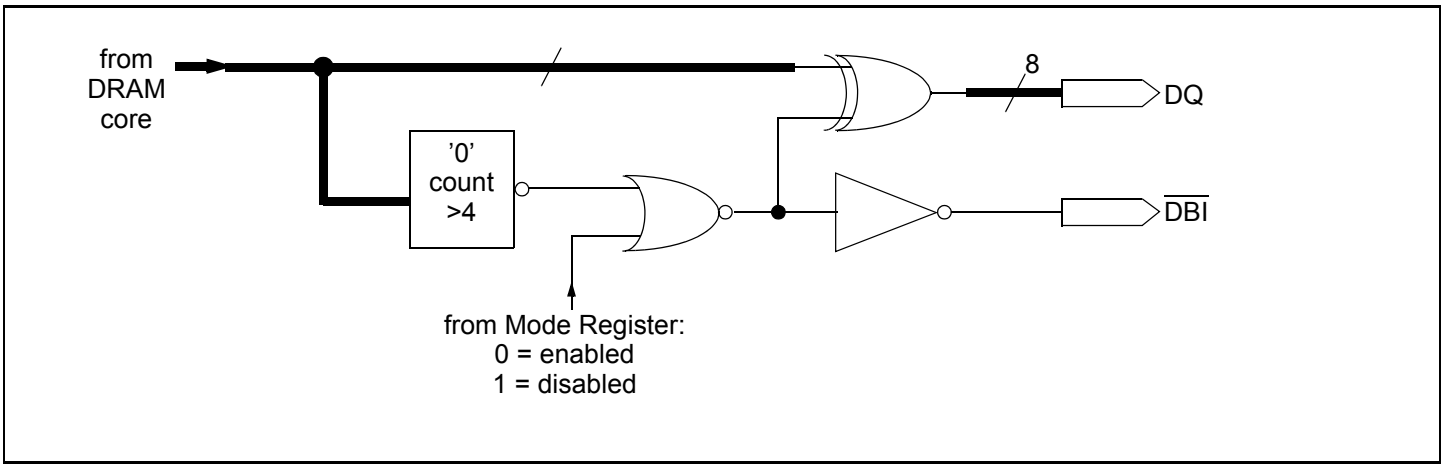


Figure 47. Example of Data Bus Inversion Logic for READs

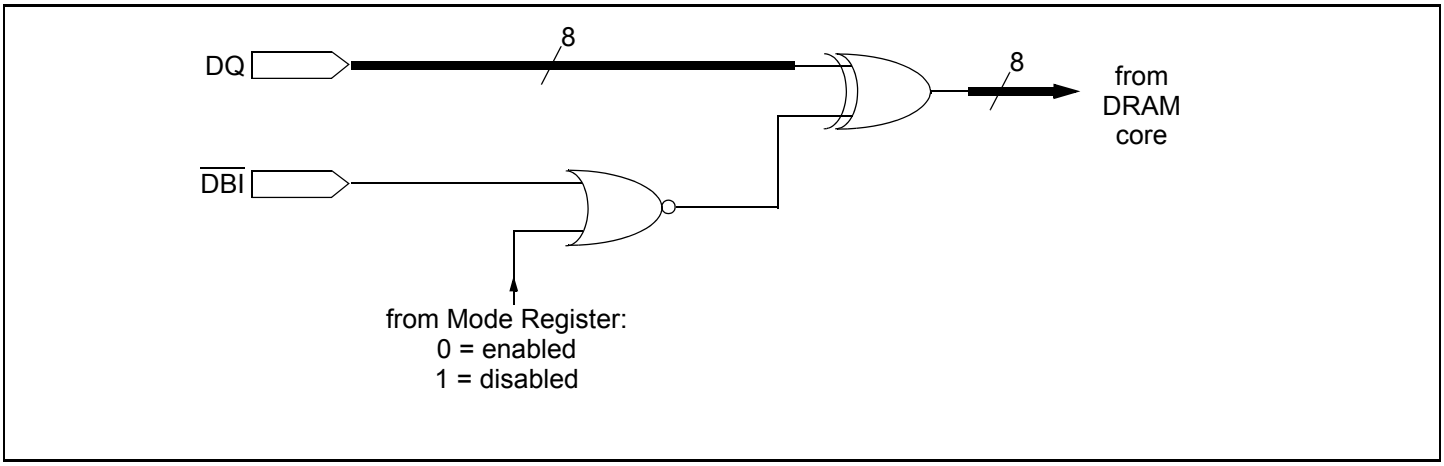


Figure 48. Example of Data Bus Inversion Logic for WRITEs

The flow diagram in the following figure illustrates the DBIdc operation. In any case, the transmitter (the controller for WRITEs, the GDDR5 SGRAM for READs) decides whether to invert or not invert the data conveyed on the DQs. The receiver (the GDDR5 SGRAM for WRITEs, the controller for READs) has to perform the reverse operation based on the level on the $\overline{DBI}$ pin.

DBI Flow Diagram

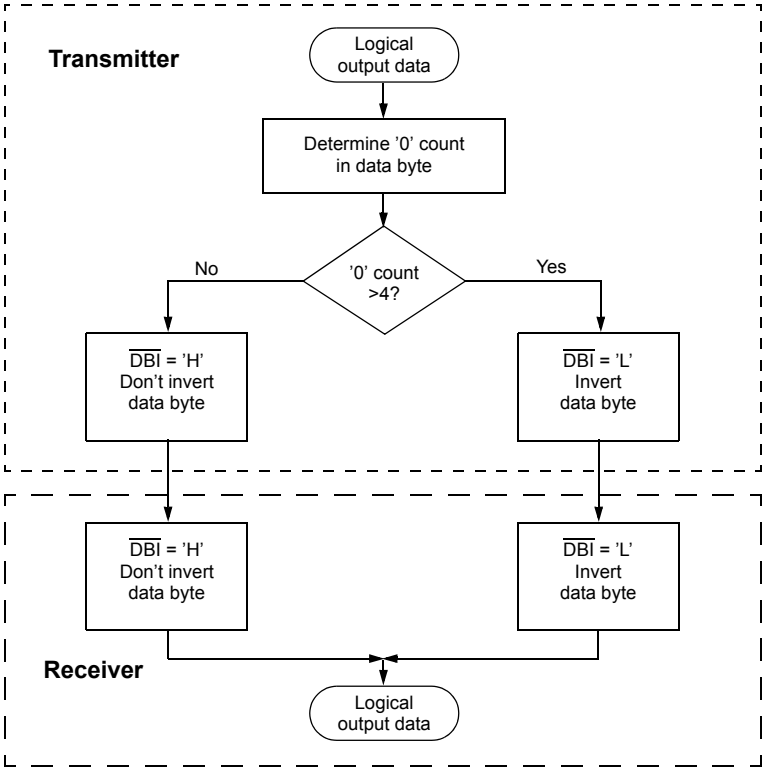


Figure 49. DBI Flow Diagram

17.15 DATA Preamble

DQ preamble is an optional feature for GDDR5 SGRAMs that is used for READ data. DQ preamble conditions the DQs for better signal integrity on the initial data of a burst. Once enabled by bit 5 in MR7, the DQ preamble will precede all READ bursts, including non-consecutive READ bursts with a minimum gap of 1 tCK as shown in below Figure. When enabled, the DQ preamble pattern applies to all DQ and DBI pins in a byte, and the same pattern is used for all bytes as shown in DQ preable table. DQ preamble is enabled or disabled for all bytes. The EDC pin in each byte is not included in the DQ preamble. If ODT is enabled, the ODT is disabled 1 tCK before the start of the preamble pattern as shown in Figure 50.

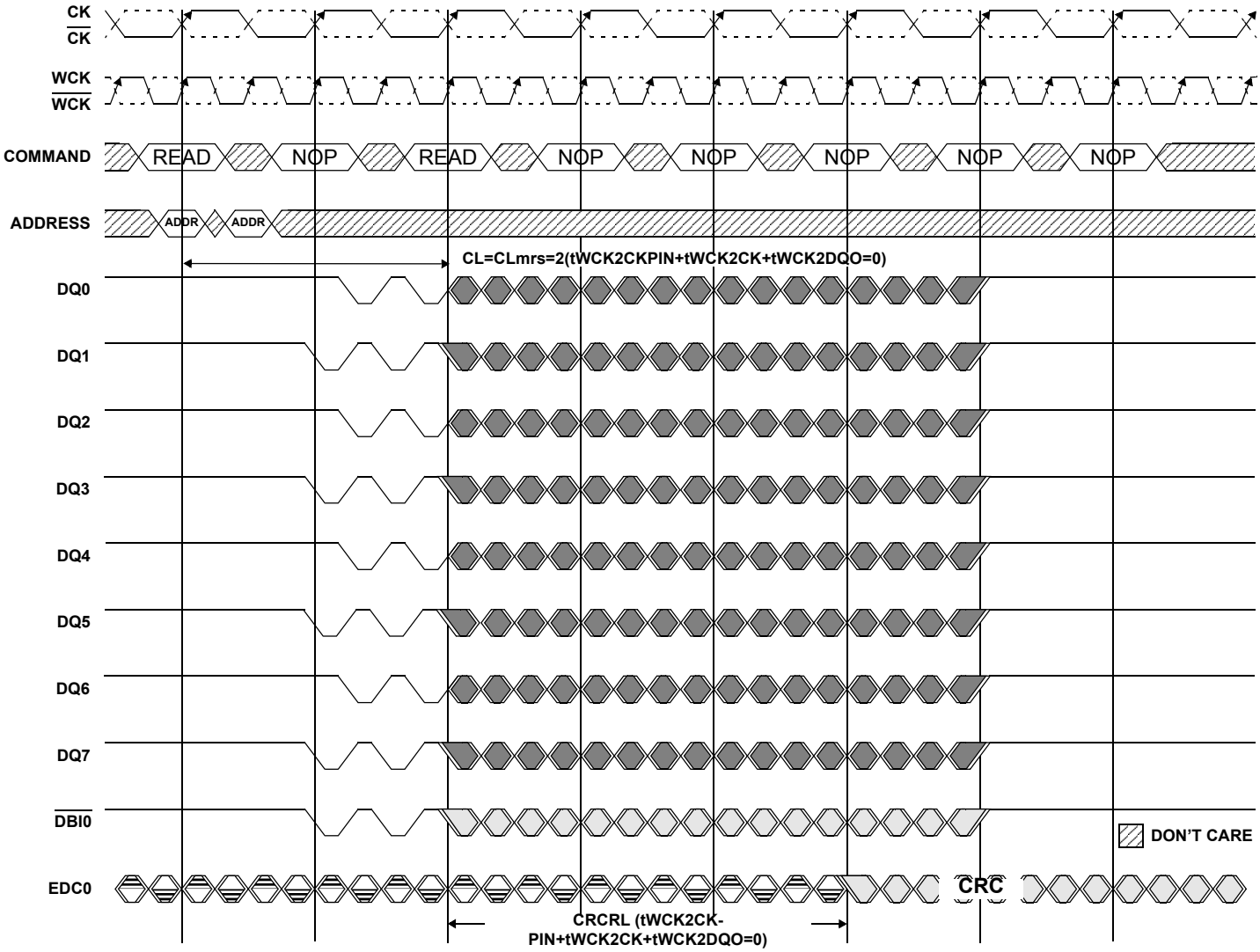


Figure 50. DATA Preamble

DQ Preamble pattern

Byte0	Byte1	Byte2	Byte3	Idle				Preamble				Burst							
DQ7	DQ15	DQ23	DQ31	1	1	1	1	0	1	0	1	X	X	X	X	X	X	X	X
DQ6	DQ14	DQ22	DQ30	1	1	1	1	1	0	1	0	X	X	X	X	X	X	X	X
DQ5	DQ13	DQ21	DQ29	1	1	1	1	0	1	0	1	X	X	X	X	X	X	X	X
DQ4	DQ12	DQ20	DQ28	1	1	1	1	1	0	1	0	X	X	X	X	X	X	X	X
DQ3	DQ11	DQ19	DQ27	1	1	1	1	0	1	0	1	X	X	X	X	X	X	X	X
DQ2	DQ10	DQ18	DQ26	1	1	1	1	1	0	1	0	X	X	X	X	X	X	X	X
DQ1	DQ9	DQ17	DQ25	1	1	1	1	0	1	0	1	X	X	X	X	X	X	X	X
DQ0	DQ8	DQ16	DQ24	1	1	1	1	1	0	1	0	X	X	X	X	X	X	X	X
$\overline{DBI0}$	$\overline{DBI1}$	$\overline{DBI2}$	$\overline{DBI3}$	1	1	1	1	0	1	0	1	X	X	X	X	X	X	X	X
		Max 0's		0	0	0	0	5	4	5	4	4	4	4	4	4	4	4	4

NOTE :
1) The number of Max's in the burst is 4 only if RDBI is enabled. Max 0°Æs is on a per byte basis and does not include the EDC pin.
2) x = Valid Data

17.16 Error Detection Code (EDC)

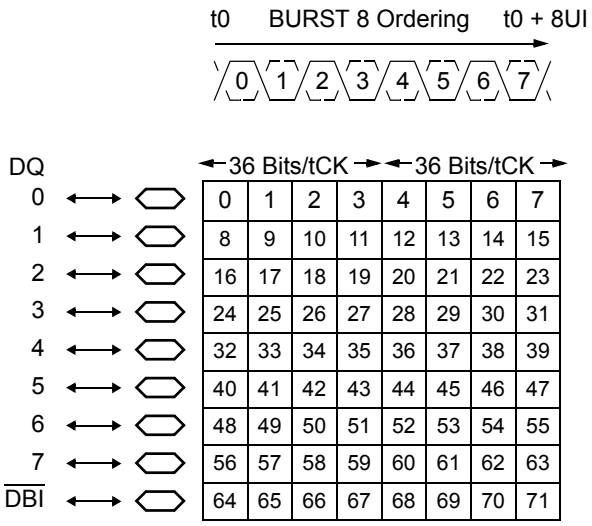
GDDR5 incorporates a unidirectional EDC algorithm for error detection on the DQ bus. The GDDR5 device generates the cyclic redundancy check, CRC data, for both READ and WRITE. The serial CRC data is then sent on the EDC pin in a per byte basis with 4 EDC pins per GDDR5 devices for the x32 and 2 EDC pins for the x16. Each EDC pin is used for an 8 bit CRC on 72 bits, this includes the 8 DQ pins and the data bit inversion pin, $\overline{DBI}$ pin.

The CRC polynomial used by the GDDR5 is an ATM-8 HEC, X^8+X^2+X+1. The following table shows the error types that are detectable and the detection rate. The starting seed value is set in hardware at "zero" in every READ and WRITE command.

Error Correction Details

Error Type	Detection Rate
Random Single Bit	100%
Random Double Bit	100%
Random Odd Count	100%
Burst <= 8	100%

The bit ordering calculation for the CRC error detection is optimized for errors in the time burst direction. The following figure shows the bit orientation on a byte lane basis.



The EDC latency is based on the CAS latency for READ data and the WRITE latency for WRITE data. The following table shows the timing parameters associated with the EDC scheme.

Mode Register 4 is used to determine the functionality of the EDC pin. Register bits A9 and A10 control the GDDR5 SGRAM's CRC calculation independently for READ and WRITE. With CRC being off, the calculated CRC pattern will be replaced by the EDC hold pattern defined in Mode Register 4 bits A0..A3.

The EDC hold pattern is considered a background pattern transmitted on the EDC pins. The register shall be initialized to all 1's upon power-up. With MR4 register bit A11(EDC13 Inv) is set High, EDC1 and EDC3 will transmit the inverted EDC hold pattern. The output timing is the same as a read burst. Other pattern like the CRC bursts calculated from write or read bursts will replace the EDC hold pattern for the duration of that burst.

When RDQS mode is enabled, CRC pattern is replaced by RDQS pattern with 4UI(1010) pre-ambles. With MR4 register bit A11(EDC13 Inv) is set High in RDQS mode, RDQS pattern is inverted on EDC1 and EDC3 pin.

The values of the EDC write latency is loaded into register 3 bits A4..A6. The values of EDC read latency is loaded into register 2 bits A7..A8.

[Table 20] EDC Timing

Description	Parameter	Value	Units
EDC Read Latency	tEDCRL	CL+CRCRL	tCK
EDC Write Latency	tEDCWL	WL+CRCWL	tCK

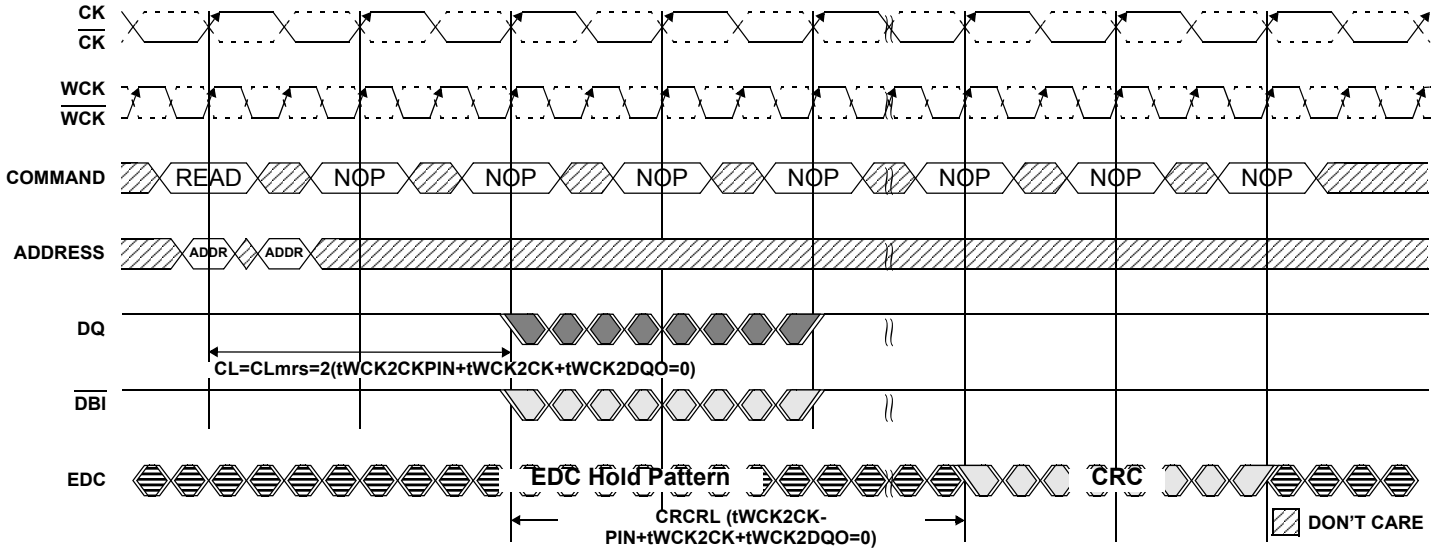


Figure 51. EDC Timing

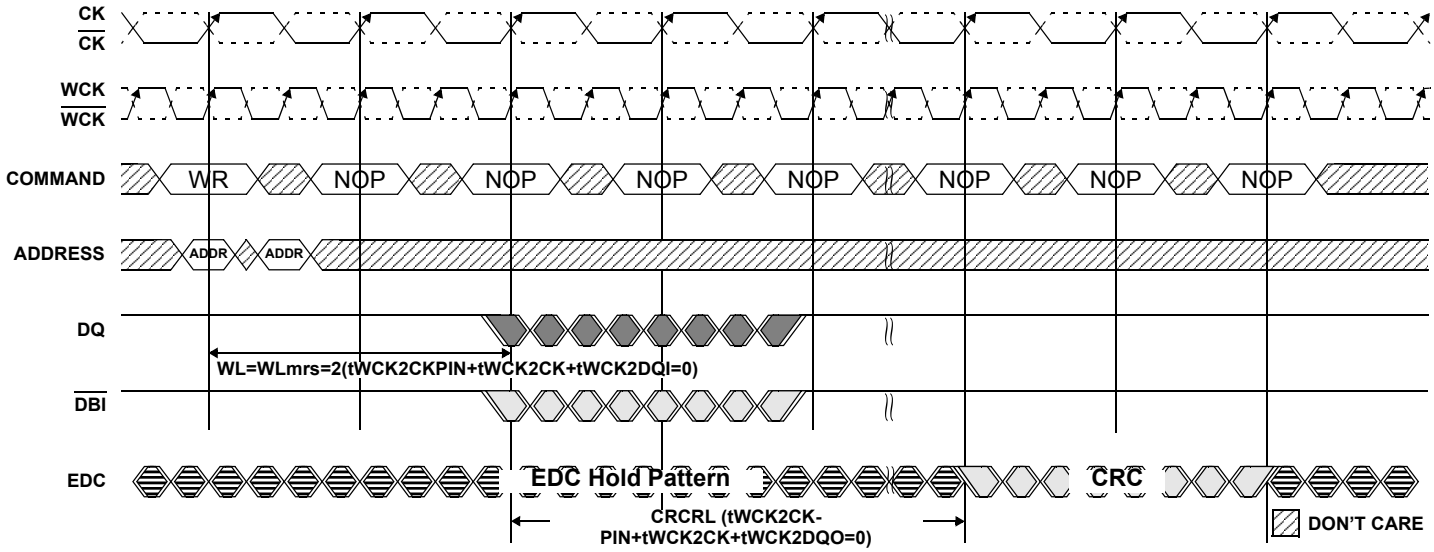


Figure 52. EDC WRITE Timing

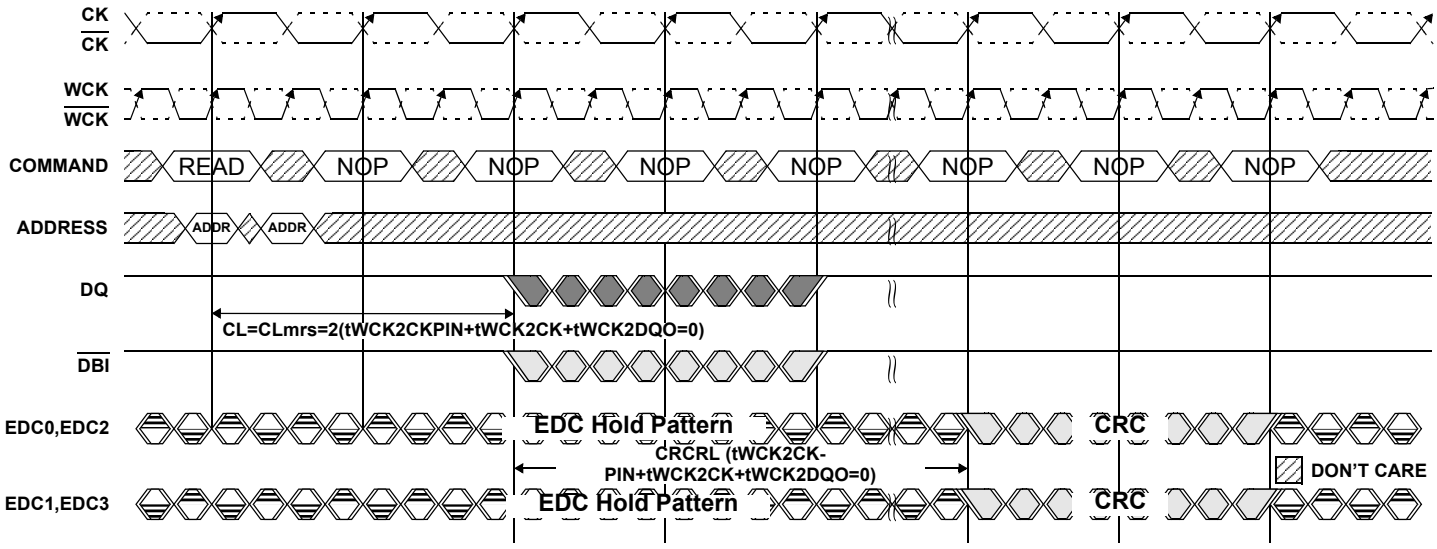


Figure 53. EDC13 Invert Mode

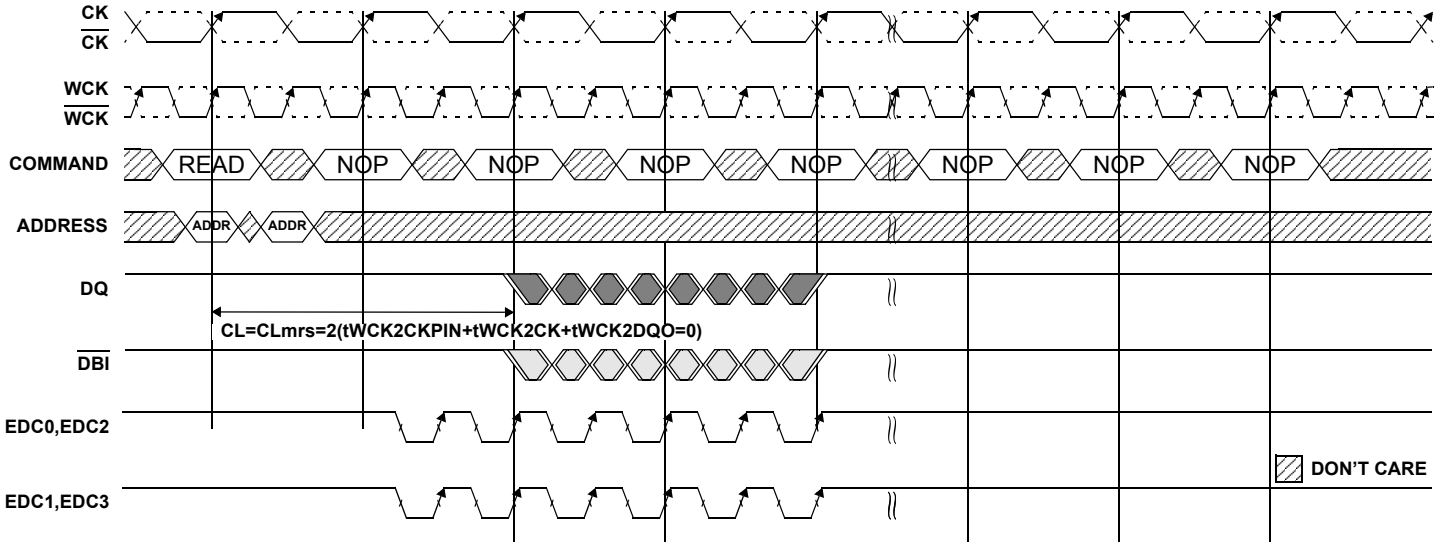


Figure 54. RDQS Mode

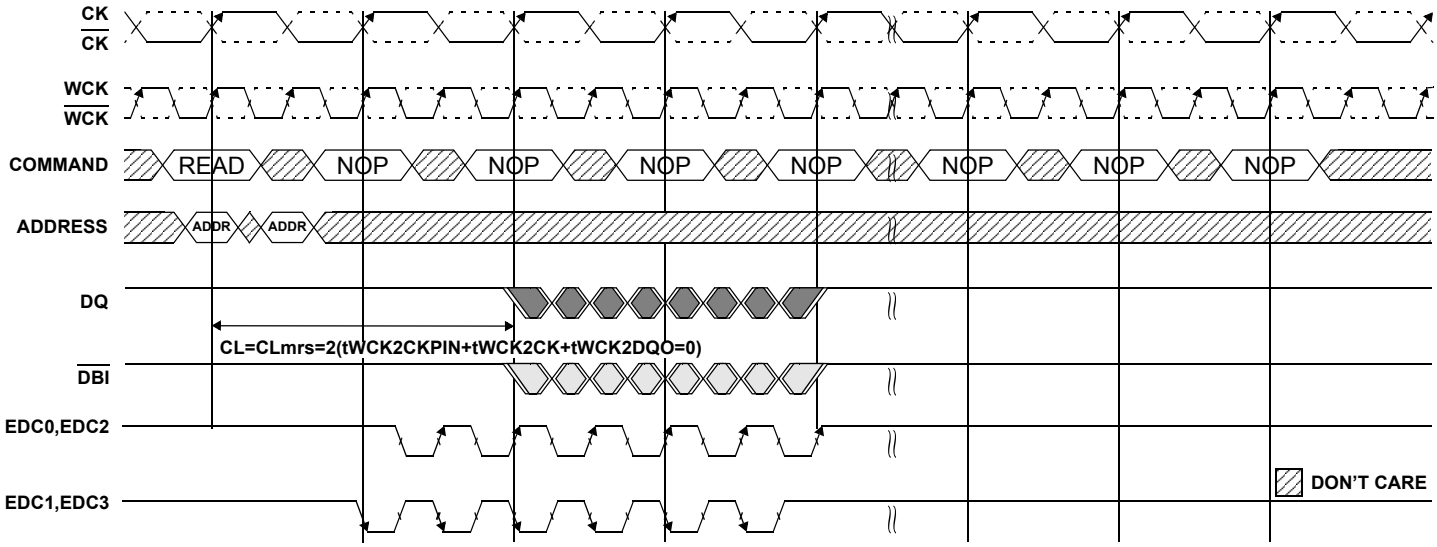


Figure 55. RDQS+EDC13 Invert Mode

17.17 Cyclic Redundancy Code Generator

Below is an example implementation of a 72 bit parallel CRC calculation based on the given polynomial: X^8+X^2+X^1+1. The indices of reg D correspond to the positions

```
CRC[0] = D[69] ^ D[68] ^ D[67] ^ D[66] ^ D[64] ^ D[63] ^ D[60] ^ D[56] ^
         D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[45] ^ D[43] ^
         D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^ D[30] ^ D[28] ^ D[23] ^
         D[21] ^ D[19] ^ D[18] ^ D[16] ^ D[14] ^ D[12] ^ D[ 8] ^ D[ 7] ^
         D[ 6] ^ D[ 0];

CRC[1] = D[70] ^ D[66] ^ D[65] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^ D[56] ^
         D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^ D[44] ^ D[43] ^
         D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^ D[30] ^ D[29] ^ D[28] ^
         D[24] ^ D[23] ^ D[22] ^ D[21] ^ D[20] ^ D[18] ^ D[17] ^ D[16] ^
         D[15] ^ D[14] ^ D[13] ^ D[12] ^ D[ 9] ^ D[ 6] ^ D[ 1] ^ D[ 0];

CRC[2] = D[71] ^ D[69] ^ D[68] ^ D[63] ^ D[62] ^ D[61] ^ D[60] ^ D[58] ^
         D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^ D[44] ^ D[43] ^
         D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^ D[29] ^ D[28] ^ D[25] ^
         D[24] ^ D[22] ^ D[17] ^ D[15] ^ D[13] ^ D[12] ^ D[10] ^ D[ 8] ^
         D[ 6] ^ D[ 2] ^ D[ 1] ^ D[ 0];

CRC[3] = D[70] ^ D[69] ^ D[64] ^ D[63] ^ D[62] ^ D[61] ^ D[59] ^ D[58] ^
         D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^ D[44] ^ D[43] ^
         D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^ D[29] ^ D[26] ^ D[25] ^
         D[23] ^ D[18] ^ D[16] ^ D[14] ^ D[13] ^ D[11] ^ D[ 9] ^ D[ 7] ^
         D[ 3] ^ D[ 2] ^ D[ 1];

CRC[4] = D[71] ^ D[70] ^ D[65] ^ D[64] ^ D[63] ^ D[62] ^ D[60] ^ D[59] ^
         D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^ D[45] ^ D[44] ^
         D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^ D[30] ^ D[27] ^ D[26] ^
         D[24] ^ D[19] ^ D[17] ^ D[15] ^ D[14] ^ D[12] ^ D[10] ^ D[ 8] ^
         D[ 4] ^ D[ 3] ^ D[ 2];

CRC[5] = D[71] ^ D[66] ^ D[65] ^ D[64] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^
         D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^ D[45] ^ D[42] ^
         D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^ D[28] ^ D[27] ^ D[25] ^
         D[20] ^ D[18] ^ D[16] ^ D[15] ^ D[13] ^ D[11] ^ D[ 9] ^ D[ 5] ^
         D[ 4] ^ D[ 3];

CRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62] ^ D[61] ^ D[58] ^ D[54] ^
         D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^ D[43] ^ D[41] ^
         D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^ D[28] ^ D[26] ^ D[21] ^
         D[19] ^ D[17] ^ D[16] ^ D[14] ^ D[12] ^ D[10] ^ D[ 6] ^ D[ 5] ^
         D[ 4];

CRC[7] = D[68] ^ D[67] ^ D[66] ^ D[65] ^ D[63] ^ D[62] ^ D[59] ^ D[55] ^
         D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[44] ^ D[42] ^
         D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^ D[29] ^ D[27] ^ D[22] ^
         D[20] ^ D[18] ^ D[17] ^ D[15] ^ D[13] ^ D[11] ^ D[ 7] ^ D[ 6] ^
         D[ 5];
```

The initial value of D[0:71] is "0" on every READ and WRITE. The CRC[0:7] is the output burst pattern on the EDC pin. The burst order is from CRC[0] to CRC[7].

17.18 CLOCK FREQUENCY CHANGE SEQUENCE

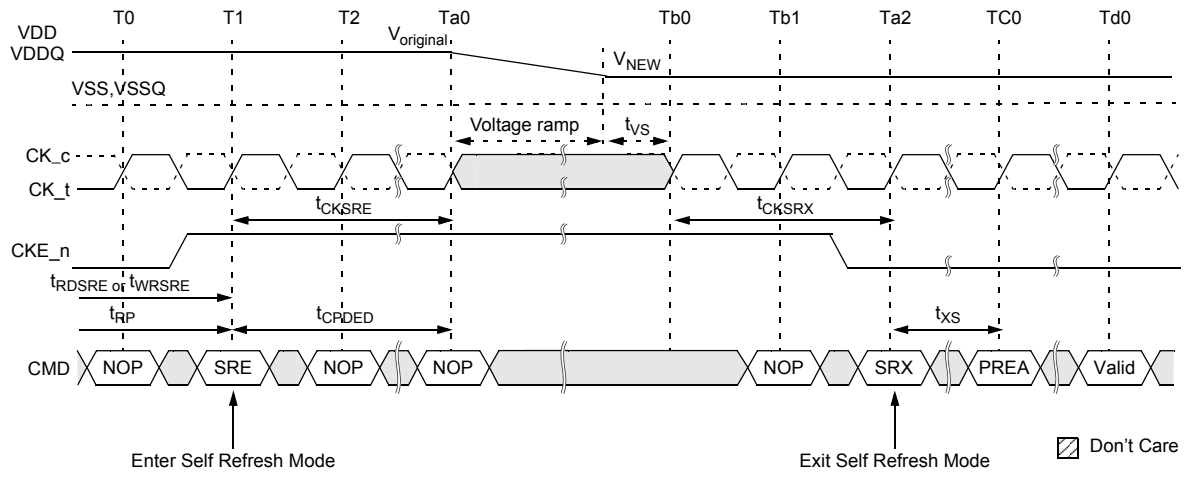
Step 1) Wait until all commands have finished, all banks are idle.
Step 2) Send NOP or DESELECT (must meet setup/hold relative to clock while clock is changing) to GDDR5 SGRAM for the entire sequence unless stated to do otherwise. The user must take care of refresh requirements.
Step 3) If the new desired clock frequency is below the min frequency supported by PLL/DLL on mode, turn the PLL/DLL off via an MRS command.
Step 4) Change the clock frequency and wait until clock is stabilized.
Step 5) If new clock frequency is within the PLL/DLL on range and the PLL/DLL on state is desired, enable the PLL/DLL via an MRS Command if it is not already enabled.
Step 6) Perform address training if required.
Step 7) Perform WCK2CK training. As defined in the WCK2CK training process, if the PLL/DLL is enabled, then complete steps 7a and 7b:
  7a) Reset the PLL/DLL by writing to the MRS register.
  7b) Wait tLK clock cycles before issuing any commands to the GDDR5 SGRAM.
Step 8) Exit WCK2CK training.
Step 9) Perform READ and WRITE training, if required.
Step 10) GDDR5 SGRAM is ready for normal operation after any necessary interface training.

17.19 DYNAMIC VOLTAGE SWITCHING (DVS)

GDDR5 SGRAM's allow the supply voltage to be changed during the course of normal operation using the GDDR5 Dynamic Voltage Switching (DVS) feature. By using DVS the GDDR5 SGRAM's power consumption can be reduced whenever only a fraction of the maximum available bandwidth is required by the current work load.
DVS requires the GDDR5 SGRAM to be properly placed into self refresh before the voltage is changed from the exising stable voltage, $V_{original}$ to the new desired voltage Vnew . The DVS procedure may also require changes to the VDD Range mode register using MR7 bits A8 and A9, depending on whether the feature is supported. The DRAM vendor's datasheet shall be consulted regarding the supported supply voltages for DVS, and any dependencies of AC timing parameters on the selected supply voltage. Clock frequency changes can also take place before or after entering self refresh mode using the standard Clock Frequency Change procedure. A clock frequency change in conjunction with DVS is required if tCK is less than tCKmin supported by Vnew . In this case normal device operation including self refresh exit is not guaranteed without a frequency change. Changing the frequency while in self refresh is the most safe procedure.
Once self refresh is entered, tCKSRE must be met before the supply voltage is allowed to transition from $V_{original}$ to V_{new}. After VDD and VDDQ are stable at V_{new}, tVS must be met to allow for internal voltages in the GDDR5 SGRAM to stabilize before self refresh mode may be exited. During the voltage transition the voltage must not go below V_{min} of the lower voltage of either $V_{original}$ or V_{new} in order to prevent false chip reset. V_{min} is the minimum voltage allowed by VDD or VDDQ in the DC operating conditions table. VREF shall continue to track VDDQ.

DVS Procedure
Step 1) Complete all operations and precharge all banks.
Step 2) Issue an MRS command to set VDD Range to proper values for V_{new}. This step is only required when the VDD Range mode register field is supported by the GDDR5 SGRAM. The DRAM vendor's datasheet should be consulted to verify if the feature is supported.
Step 3) Enter self refresh mode. Self refresh entry procedure must be met.
Step 4) Wait required time tCKSRE before changing voltage to V_{new}.
Step 5) Change VDD and VDDQ to V_{new}.
Step 6) Wait required time tVS for voltage stabilization.
Step 7) Exit self refresh. The self refresh exit procedure must be met.
Step 8) Issue MRS commands to adjust mode register settings as desired (e.g. latencies, PLL/DLL on/off, CRC on/off, RDQS mode on/off).
Step 9) Perform any interface training as required.
Step 10) Continue normal operation.

17.20 DVS Sequence

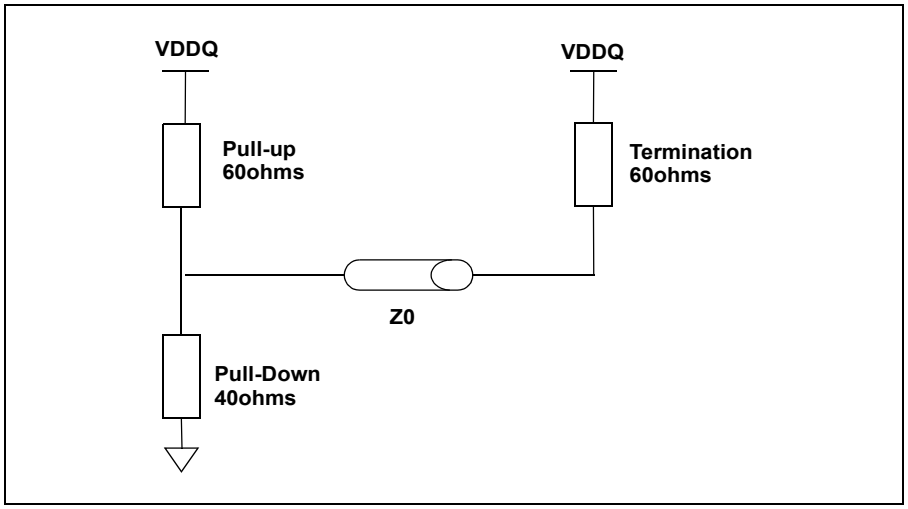


Self refresh exit requires WCK2CK training prior to any WRITE or READ operation
At least one REFRESH command shall be issued after t_{XS} for output driver and termination impedance updates
$V_{original} > V_{new}$ shown as an example of a voltage change

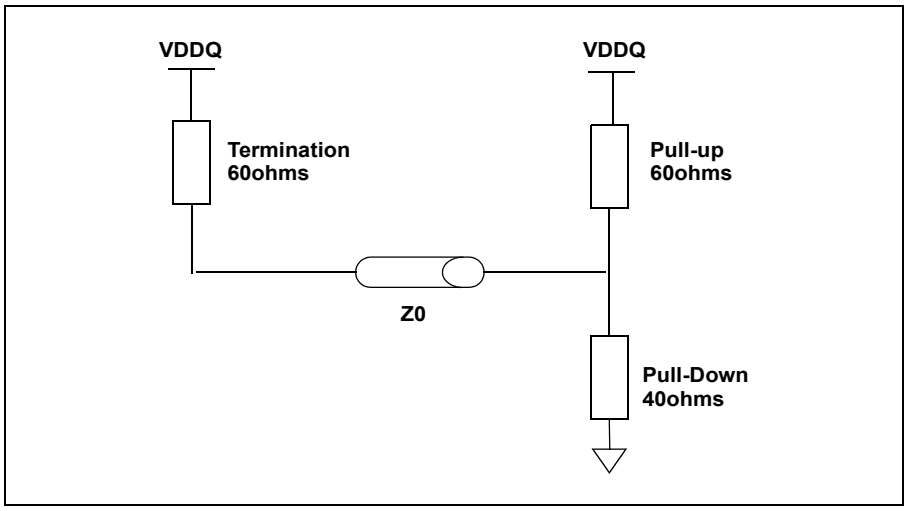
17.21 Pseudo-Open Drain (POD) On Chip Driver

128Mx32 GDDR5 driver and termination scheme.

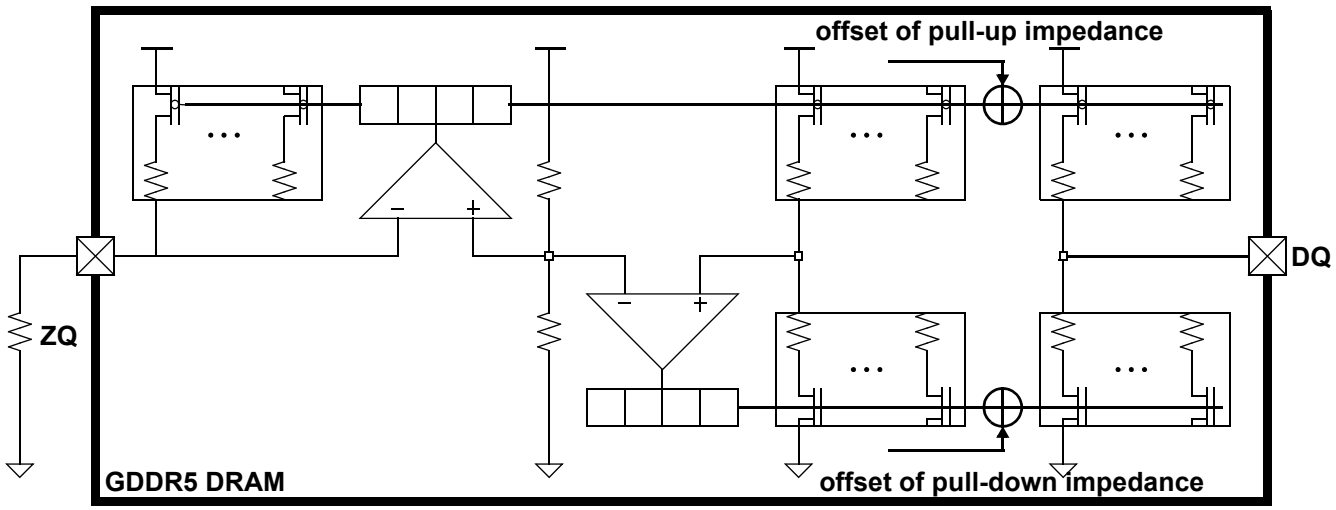
READ



WRITE



17.22 ZQ Auto Calibration



ZQ auto calibration makes pull-up impedance, pull-down impedance and ODT impedance accurate with respect to external ZQ resistance. GDDR5 DRAM has 120ohm ZQ resistance and the internal reference voltage where calibration is made is the half of VDDQ. The offset is applied to the final code which is generated from ZQ auto calibration logic.

17.23 On Die Termination

GDDR5 SGRAM supports multiple termination modes for its high speed input signals. When the termination is enabled for a receiver, an impedance defined for that termination mode is applied between that input receiver and the VDDQ supply rail. This is commonly referred to as VDDQ termination. Registers have been defined to control the termination modes.

Address/Command Termination determines the termination impedance value for the command and address signals.

Address/Command Termination Impedance

A5@MR1	A4@MR1	ADDR/CMD Termination
0	0	Impedance selected by the state of $\overline{CKE}$ on the rising edge of $\overline{RESET}$
0	1	ZQ/2
1	0	ZQ
1	1	disabled

DQ/$\overline{DBI}$ Termination determines the termination impedance for the DQ and $\overline{DBI}$ signals

DQ/$\overline{DBI}$ Termination Impedance

A3@MR1	A2@MR1	DQ/$\overline{DBI}$ Termination
0	0	disabled
0	1	ZQ/2
1	0	ZQ
1	1	Reserved

WCK/$\overline{WCK}$ Termination determines the termination impedance for the WCK and $\overline{WCK}$ signals.

WCK/$\overline{WCK}$ Termination Mode

A9@MR3	A8@MR3	WCK/$\overline{WCK}$ Termination
0	0	disabled
0	1	ZQ/2
1	0	ZQ
1	1	Reserved

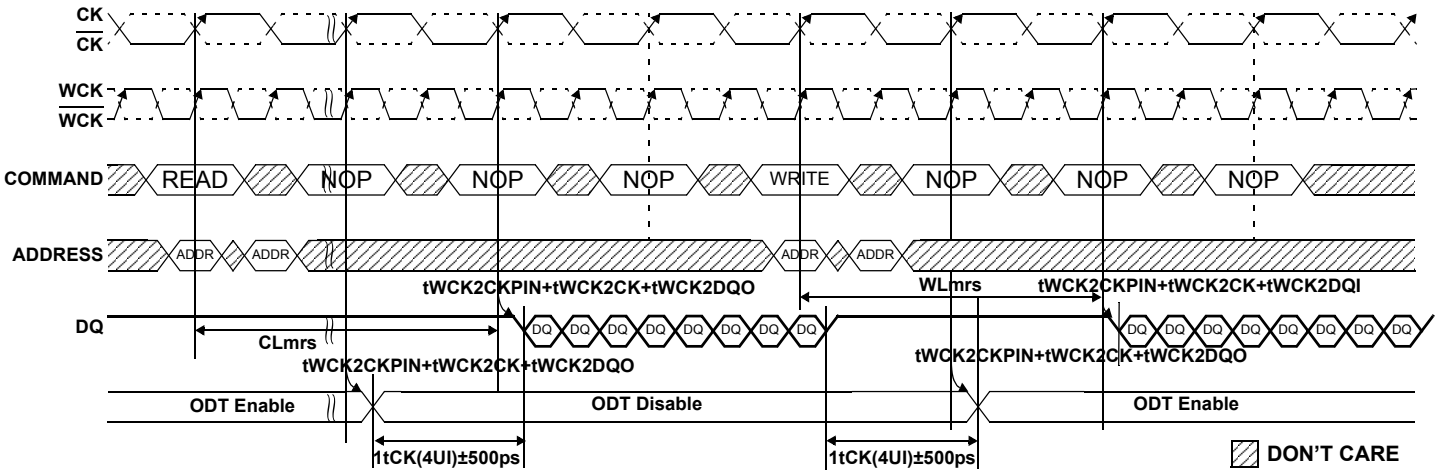
The following table has all the high speed GDDR5 SGRAM signals which include on die termination to VDDQ and whether their termination can be disabled by MRS.

[Table 21] Signals Affected by Termination Control Registers

Signal	ADD/CMD Termination		DQ/$\overline{DBI}$ Termination		WCK/$\overline{WCK}$ Termination	
	x32	x16 (MF=0)	x32	x16 (MF=0)	x32	x16 (MF=0)
$\overline{RAS}$	Yes	Yes	No	No	No	No
$\overline{CAS}$	Yes	Yes	No	No	No	No
$\overline{WE}$	Yes	Yes	No	No	No	No
$\overline{CS}$	Yes	Yes	No	No	No	No
$\overline{CKE}$	Yes	Yes	No	No	No	No
BA3/A3	Yes	Yes	No	No	No	No
BA2/A4	Yes	Yes	No	No	No	No
BA1/A5	Yes	Yes	No	No	No	No
BA0/A2	Yes	Yes	No	No	No	No
A12/A13	Yes	Yes	No	No	No	No
A11/A6	Yes	Yes	No	No	No	No
A10/A0	Yes	Yes	No	No	No	No
A9/A1	Yes	Yes	No	No	No	No
A8/A7	Yes	Yes	No	No	No	No
$\overline{ABI}$	Yes	Yes	No	No	No	No
DQ[7:0]	No	No	Yes	Yes	No	No
DQ[15:8]	No	Disabled	Yes	Disabled	No	Disabled
DQ[23:16]	No	No	Yes	Yes	No	No
DQ[31:24]	No	Disabled	Yes	Disabled	No	Disabled
$\overline{DBI0}$	No	No	Yes	Yes	No	No
$\overline{DBI1}$	No	Disabled	Yes	Disabled	No	Disabled
$\overline{DBI2}$	No	No	Yes	Yes	No	No
$\overline{DBI3}$	No	Disabled	Yes	Disabled	No	Disabled
WCK01, $\overline{WCK01}$	No	No	No	No	Yes	Yes
WCK23, $\overline{WCK23}$	No	No	No	No	Yes	Yes

17.23.1 On-Die Termination On/Off Timing

In GDDR5 SGRAM, on-die termination is required to be controlled when READ command is issued in order to turn off the termination and turn on the on-chip driver. In READ mode the on-die termination for DQ pins are disabled CL+tWCK2CKPIN+tWCK2CK+ tWCK2DQO-1clock after the READ command and stays off for a duration of BL/4+1.5 clocks. The on-die termination is turned off one clock cycle before DQ is driven and turn on half of clock cycle after DQ is off. There is no bus snoop in GDDR5 unlike GDDR4 since dual load configuration is not allowed in GDDR5.



NOTE : tWCK2CKPIN+tWCK2CK+tWCK2DQO and tWCK2CKPIN+tWCK2CK+tWCK2DQI are asynchronous due to internal WCK clock tree and buffers.

Figure 56. Data Termination Disable Timing

17.24 Boundary Scan Function

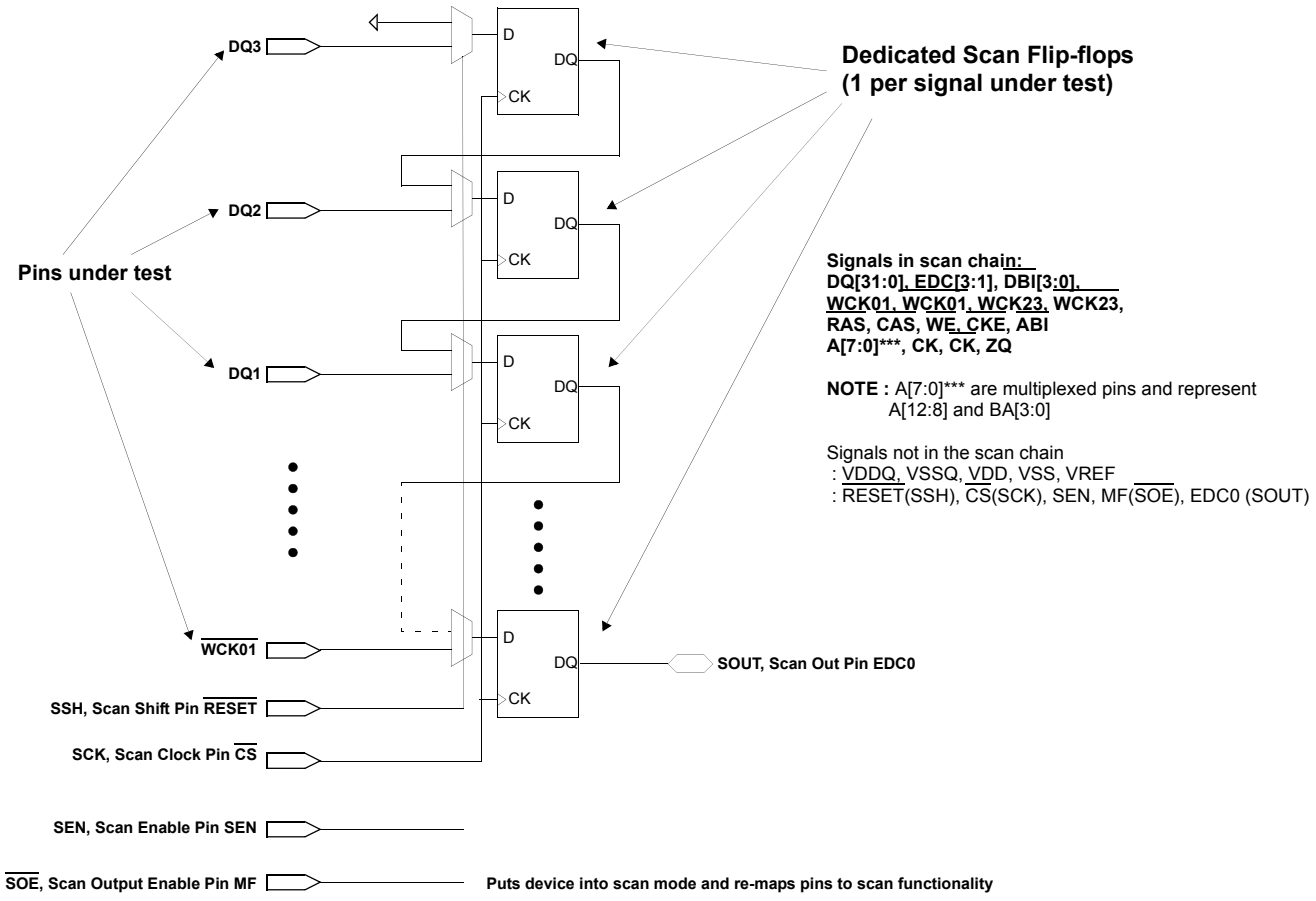


Figure 57. Boundary Scan Block Diagram

The GDDR5 SGRAM incorporates a modified boundary scan test mode. This mode does not operate in accordance with IEEE Standard 1149.-1990. To save the current GDDR5 SGRAM's ball-out, this mode will scan the parallel data input and output the scanned data on EDC0 located at C-2 controlled by an add-on pin, SEN which is located at J-10 of the 170 ball package. Scan mode is entered directly after power-up while the device is in reset state. This ensures that no unwanted access commands are being executed prior to scan mode. For normal device operation, i.e. after scan mode operation, it is required that device reinitialization occurs through device power-down and then power-up.

It is possible to operate the GDDR5 SGRAM without using the boundary scan feature. SEN should be tied Low to prevent the device from entering the boundary scan mode. The other pins which are used for scan mode ($\overline{\text{RESET}}$, MF, EDC0 and $\overline{\text{CS}}$) will be operating as normal when SEN is deasserted. In boundary scan mode, mirror function is ignored.

[Table 22] Boundary Scan Exit Order

Bit	BALL	NAME	Bit	BALL	NAME	Bit	Ball	NAME	Bit	BALL	NAME	Bit	Ball	NAME
1	D-5	$\overline{WCK01}$	13	J-3	$\overline{CKE}$	25	T-2	DQ27	37	M-11	DQ22	49	E-13	DQ13
2	D-4	WCK01	14	K-4	A8/A7	26	T-4	DQ26	38	M-13	DQ23	50	E-11	DQ12
3	D-2	$\overline{DBI0}$	15	K-5	A11/A6	27	V-2	DQ25	39	L-12	$\overline{WE}$	51	D-13	$\overline{DBI1}$
4	E-4	DQ4	16	L-3	$\overline{CAS}$	28	V-4	DQ24	40	K-10	BA1/A5	52	C-13	EDC1
5	E-2	DQ5	17	M-2	DQ31	29	V-11	DQ16	41	K-11	BA2/A4	53	B-13	DQ11
6	F-4	DQ6	18	M-4	DQ30	30	V-13	DQ17	42	J13	ZQ	54	B-11	DQ10
7	F-2	DQ7	19	N-2	DQ29	31	T-11	DQ18	43	J12	CK	55	A-13	DQ9
8	G-3	$\overline{RAS}$	20	N-4	DQ28	32	T-13	DQ19	44	J11	CK	56	A-11	DQ8
9	H-5	A9/A1	21	P-2	$\overline{DBI3}$	33	R-13	EDC2	45	H-11	BA0/A2	57	A-4	DQ0
10	H-4	A10/A0	22	P-4	WCK23	34	P-13	$\overline{DBI2}$	46	H-10	BA3/A3	58	A-2	DQ1
11	J-5	A12/A13	23	P-5	$\overline{WCK23}$	35	N-11	DQ20	47	F-13	DQ15	59	B-4	DQ2
12	J-4	$\overline{ABI}$	24	R-2	EDC3	36	N-13	DQ21	48	F-11	DQ14	60	B-2	DQ3

NOTE : When the device is in scan mode, mirror function is disabled and none of the pins are remapped.

[Table 23] Scan pin description

Package Ball	Symbol	Normal Function	Type	Description
J-2	SSH	RESET	Input	Scan Shift: capture the data input from the pad at logic LOW and shift the data on the chain at logic HIGH.
G-12	SCK	CS	Input	Scan Clock. Not a true clock, could be a single pulse or series of pulses. All scan inputs will be referenced to the rising edge of the scan clock.
C-2	SOUT	EDC0	Output	Scan Output.
J-10	SEN	RFU	Input	Scan Enable: logic HIGH enables scan mode. Scan mode is disabled at logic LOW. Must be tied to GND when not in use.
J-1	SOE	MF	Input	Scan Output Enable: enables (registered LOW) and disables (registered HIGH) SOUT data. This pin will be tied to VDD or GND through a resistor (typically 1KOhm) for normal operation. Tester needs to overdrive this pin to guarantee the required input logic level in scan mode.

NOTE :
1. When SEN is asserted, no commands are to be executed by the GDDR5 SGRAM. This applies to both user commands and manufacturing commands which may exist while $\overline{RESET}$ is deasserted.
2. All scan functionality is valid only after the appropriate power-up and initialization sequence.
3. In scan mode, all ODT will be disabled. It is not necessary for the termination to be calibrated.

[Table 24] Electrical Input Characteristics in Scan mode

Parameter/condition	Symbol	Min	Max	Units	NOTE
Input High (Logic 1) Voltage	VIH	VDDQ-0.3	-	V	1, 2, 3
Input Low (Logic 0) Voltage	VIL	-	0.3	V	1, 2, 3

NOTE :
1. The parameter applies only when SEN is asserted.
2. All voltages referenced to GND.
3. VREF must be applied and stable within the valid range.

17.24.1 Boundary Scan Exit Order

Normal Package (Top View)

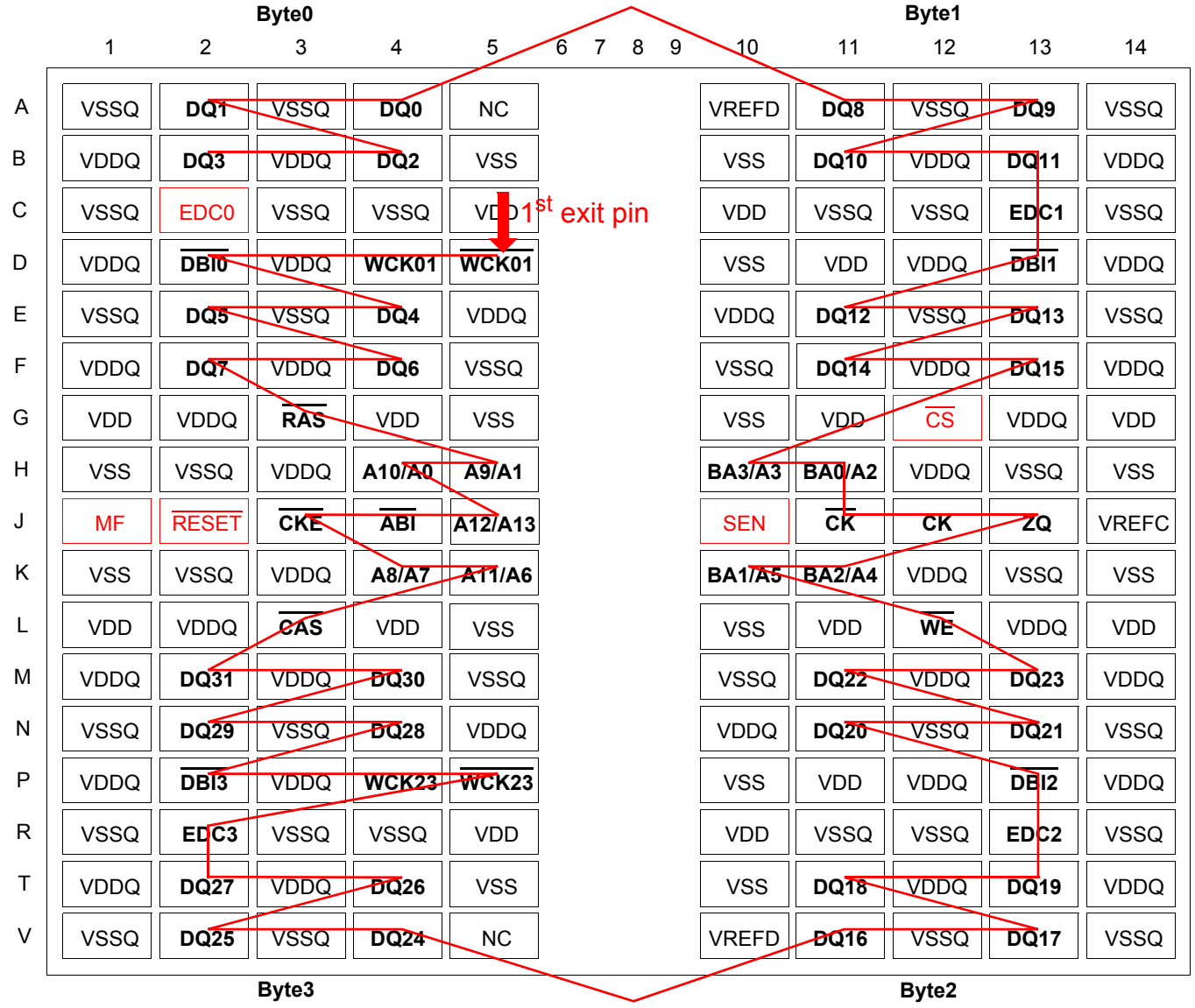


Figure 58. GDDR5 Boundary Scan Exit Order (MF=0)

[Table 25] Scan AC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Units	NOTE
Clock					
Clock cycle time	tSCK	40	-	ns	1
Scan Command Time					
Scan enable setup time	tSES	20	-	ns	1
Scan enable Hold time	tSEH	20	-	ns	1
Scan command setup time for SSH, $\overline{SOE}$ and SOUT	tSCS	14	-	ns	1
Scan command hold time for SSH, $\overline{SOE}$ and SOUT	tSCH	14	-	ns	1
Scan Capture Time					
Scan capture setup Time	tSDS	10	-	ns	1
Scan capture hold Time	tSDH	10	-	ns	1
Scan Shift Time					
Scan clock to valid scan output	tSAC	-	6	ns	1
Scan clock to scan output hold	tSOH	1.5	-	ns	1

NOTE :
1. The parameter applies only when SEN is asserted.

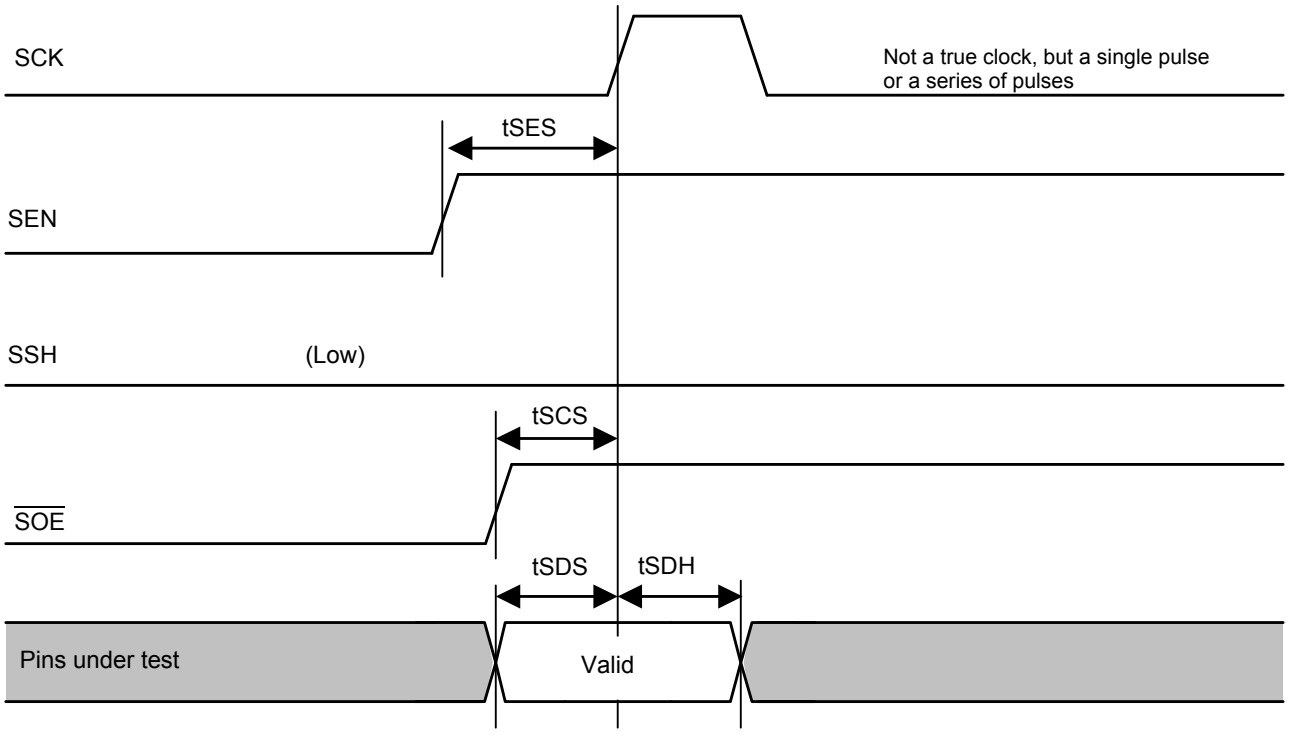


Figure 59. 1 Scan Capture Timing

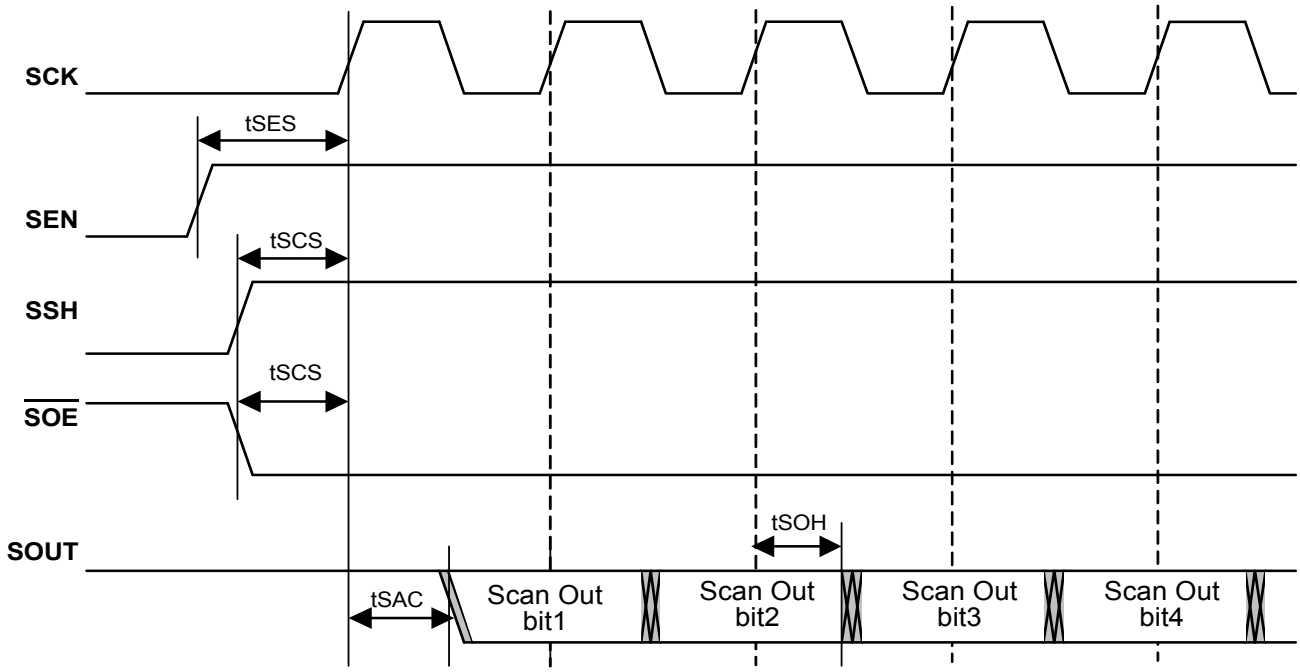


Figure 60. Scan Shift Timing

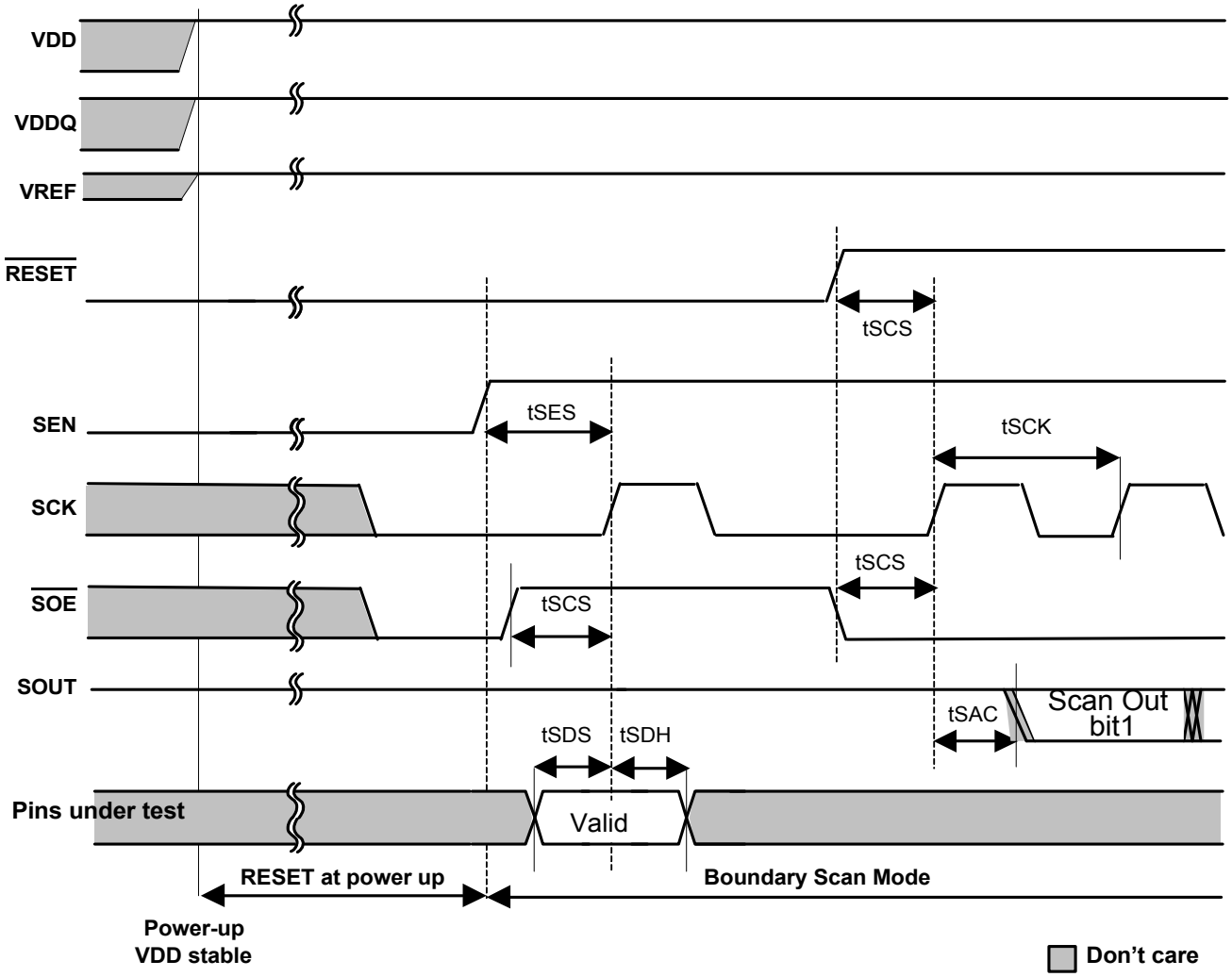


Figure 61. Scan Initialization Sequence

17.25 LOW FREQUENCY MODES

GDDR5 SGRAM's have been designed to operate over a wide range of frequencies. GDDR5 must support a continguous frequency range from tCK=20ns (200Mbps) to the maximum rated speed of the device.

Features such as PLL/DLL off mode, RDQS mode, Termination control bits, temperature sensor and the low power mode MR bits, such as MR5 bits A0-A3 and MR7 bit A3, have been developed for low power or frequency operation. Many of the low power features are optional therefore DRAM vendor datasheets should be consulted for features supported and frequency ranges supported for each feature.

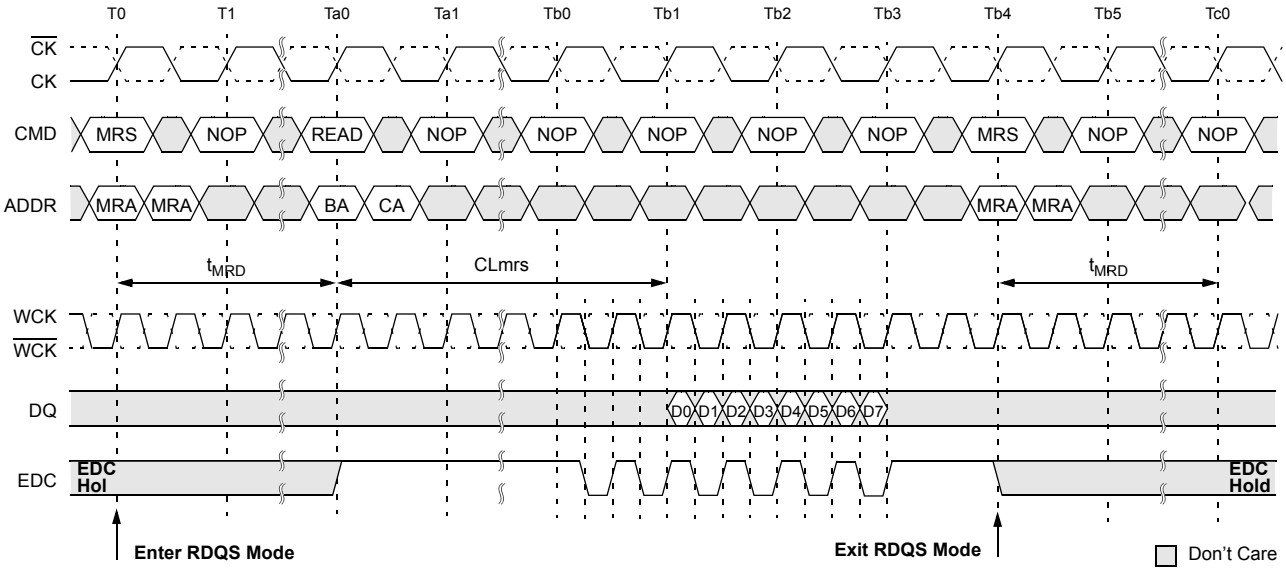
A suggested frequency vs. features table is shown in Table 26 for reference only.

[Table 26] Example of Frequency Modes

	Range		PLL mode	RD data clock	IO training	Termination	Low power bit	Low Freq. bit
	Min	Max						
High Freq.	2Gbps	5Gbps	PLL off	CDR	Full training	Full	off	off
Medium Freq.	0.7Gbps	2Gbps	PLL off	RDQS	Full training	Full/Half	off/on	off/on
Low Freq.	200Mbps	0.7Gbps	PLL off	RDQS	No training (Static offset btw. DQ & WCK)	Half/off	on	on

17.26 RDQS MODE

For device operation at lower clock frequencies the GDDR5 SGRAM may be set into RDQS mode in which a READ DATA STROBE (RDQS) in the style of GDDR4 will be sent on the EDC pins along with the READ data. The controller will use the RDQS to latch the READ data.
RDQS mode is entered by setting the RDQS Mode bit A5 in Mode Register 3 (MR3). When the bit is set, the GDDR5 SGRAM will asynchronously terminate any EDC hold pattern and drive a logic HIGH after tMRD at the latest. All features controlled by MR4 are ignored by RDQS mode.
READ commands are executed as in normal mode regarding command to data out delay and programmed READ latencies. A fixed clock?like pattern as shown in Figure 78 is driven on EDC pins in phase (edge aligned) with the DQ. Prior to the first valid data element, this fixed clock?like pattern or READ preamble is driven for 2 tWCK.
No CRC is calculated in RDQS mode, neither for READs nor for WRITEs. The CRC engine is effectively disabled, and the corresponding WRCRC and RDCRC Mode Register bits are ignored. The PLL/DLL may be on or off with RDQS mode, depending on system considerations and the PLL/DLL's minimum clock frequency.
There is no equivalent WDQS mode; WRITE commands to the GDDR5 SGRAM are not affected by RDQS mode.
RDQS mode is exited by resetting the RDQS Mode bit. In this case the GDDR5 SGRAM will asynchronously start driving the EDC hold pattern after tMRD.
The WCK2CK training should be performed prior to entering RDQS mode. No WCK2CK training can be done when the RDQS mode is active.



NOTE :
1. MRA = Mode Register address and opcode; BA = bank address; CA = column address
2. WCK and CK are shown aligned (tWCK2CKPIN=0, tWCK2CK=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
3. Before the READ command, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and tRCDRD must be met.
4. tWCK2DQO = 0 is shown for illustration purposes.

Figure 62. RDQS Mode Timings

As an optional feature of RDQS mode, EDC1 and EDC3 can be treated as pseudo-differential to EDC0 and EDC2 respectively, by setting the EDC13Inv field, bit A11 in MR4, as shown in Table 27 If the feature is not supported, then EDC13Inv is ignored.

[Table 27] EDC pin behavior in RDQS mode including optional pseudo-differential RDQS

MRS Set			READ/RDTR		NOP (except RD/RDTR/PDN/SRF)	POWER DOWN /SELF REFRESH
RDQS Mode	WCK2CK Training	EDC13 Invert	EDC02 Output	EDC13 Output	EDC0123 Output	EDC0123 Output
On	Off	Off	RDQS	RDQS	1111	High
		On	RDQS	Inverted RDQS	1111	High

18. OPERATING CONDITIONS

18.1 Absolute Maximum Ratings

[Table 28] Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ V_{DDQ} + 0.5V	V
Voltage on VDD supply relative to Vss	V_{DD}	-0.5 ~ 2.0V	V
Voltage on VDDQ supply relative to Vss	V_{DDQ}	-0.5 ~ 2.0V	V
Storage temperature	TSTG	-55 ~ +150	°C
Short Circuit Output Current	IOS	50mA	mA

NOTE : Stresses greater than those listed "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect reliability.

[Table 29] Capacitance

(VDD=1.5V, TA= 25°C)

Parameter	Symbol	Min	Max	Unit
Delta Input/Output Capacitance: DQs, DBI, EDC	DC_{io}	-0.1	+0.1	pF
Delta Input Capacitance: Command and Address	DC_{i1}	-0.1	+0.1	pF
Delta Input Capacitance: CK, $\overline{CK}$	DC_{i2}	-0.1	+0.1	pF
Delta Input Capacitance: WCK, $\overline{WCK}$	DC_{i4}	-0.1	+0.1	pF
Input/Output Capacitance: DQs, DBI, EDC	C_{IO}	1.1	1.7	pF
Input Capacitance: Command and Address	C_{i1}	1.0	1.4	pF
Input Capacitance: CK, $\overline{CK}$	C_{i2}	1.0	1.4	pF
Input Capacitance: $\overline{CKE}$	C_{i3}	1.0	1.4	pF
Input/Output Capacitance: WCK, $\overline{WCK}$	C_{i4}	0.9	1.3	pF

NOTE :
1. DCi = Ci - (min(Ci) + max(Ci))/2

[Table 30] Thermal Characteristics

Parameter	Description	Value	Units	NOTE
Theta_JA	Thermal resistance junction to ambient	28.9	°C/W	1,2,3,5
Tj_MAX	Maximum operating junction temperature	76.2	°C	4
Tc_MAX	Maximum operating case temperature	75.6	°C	4, 8
Theta_JC	Thermal resistance junction to case	4.7	°C/W	1,6
Theta_JB	Thermal resistance junction to board	15.1	°C/W	1,2,6

NOTE :
1. Measurement procedures for each parameter must follow standard procedures defined in the current JEDEC JESD-51 standard.
2. Theta_JA and Theta_JB must be measured with the high effective thermal conductivity test board defined in JESD51-7
3. Airflow information must be documented for Theta_JA.
4. TJ_MAX and TC_MAX are documented for normal operation in this table. These are not intended to reflect reliability limits.
5. Theta_JA should only be used for comparing the thermal performance of single packages and not for system related junction temperature prediction.
6. Theta_JB and Theta_JC are derived through a package thermal simulation.
7. Values are guaranteed by design but not tested in production
8. Tc_MAX shows measured case temperature when GDDR5 operates in 6Gbps.

18.2 DRAM Component Operating Temperature Range

[Table 31] Temperature Range

Symbol	Parameter	rating	Unit	NOTE
T_{OPER}	Operating Temperature Range	0 to 85	°C	1, 2

NOTE :
1. Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions

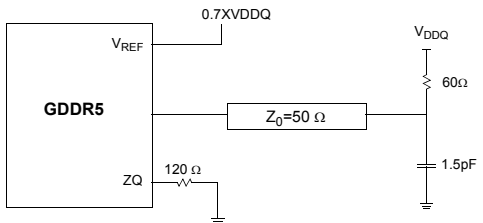
18.3 AC & DC Characteristics

[Table 32] DC Operating Conditions

Recommended operating conditions (Temp condition: 0°C ≤ Tc ≤ 85°C)

Parameter	Symbol	POD15			POD135			Unit	NOTE
		Min	Typ	Max	Min	Typ	Max		
Device Supply voltage	VDD	1.455	1.5	1.545	1.3095	1.35	1.3905	V	1
Output Supply voltage	VDDQ	1.455	1.5	1.545	1.3095	1.35	1.3905	V	1
Reference Voltage for DQ and $\overline{DBI}$ pins	VREFD	0.69*VDDQ		0.71*VDDQ	0.69*VDDQ		0.71*VDDQ	V	2,3
Reference Voltage for DQ and $\overline{DBI}$ pins	VREFD2	0.49*VDDQ		0.51*VDDQ	0.49*VDDQ		0.51*VDDQ	V	2,3,4
External Reference Voltage for address and command	VREFC	0.69*VDDQ		0.71*VDDQ	0.69*VDDQ		0.71*VDDQ	V	5
DC Input Logic HIGH Voltage for address and command	VIHA(DC)	VREFC+0.15			VREFC+0.135			V	
DC Input Logic Low Voltage for address and command	VILA(DC)			VREFC-0.15			VREFC-0.135	V	
DC Input Logic HIGH Voltage for DQ and $\overline{DBI}$ pins with VREFD	VIHD(DC)	VREFD+0.10			VREFD+0.09			V	
DC Input Logic Low Voltage for DQ and $\overline{DBI}$ pins with VREFD	VILD(DC)			VREFD-0.10			VREFD-0.09	V	
DC Input Logic HIGH Voltage for DQ and $\overline{DBI}$ pins with VREFD2	VIHD2(DC)	VREFD2+0.30			VREFD2+0.27			V	
DC Input Logic Low Voltage for DQ and $\overline{DBI}$ pins with VREFD2	VILD2(DC)			VREFD2-0.30			VREFD2-0.27	V	
Input Logic HIGH Voltage for $\overline{RESET}$, SEN, MF	VIHR	VDDQ-0.50			VDDQ-0.50			V	
Input Logic Low Voltage for $\overline{RESET}$, SEN, MF	VILR			0.30			0.30	V	
Input Logic HIGH Voltage for EDC1/2(X16 mode detect)	VIHX	VDDQ-0.3			VDDQ-0.3				8
Input Logic Low Voltage for EDC1/2(X16 mode detect)	VILX			0.3			0.3	V	8
Input Leakage Current Any Input 0V ≤ Vin ≤ VDDQ (All other pins not under test=0V)	IL	-5		5				uA	
Output Leakage Current (DQs are disabled; 0V ≤ Vout ≤ VDDQ)	Ioz	-5		5				uA	
Output Logic Low voltage	VOL(DC)			0.62			0.56	V	

NOTE :
1. GDDR5 SGRAMs are designed to tolerate PCB designs with separate VDD and VDDQ power regulators.
2. AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.
3. Source of Reference Voltage and control of Reference Voltage for DQ and $\overline{DBI}$ pins is determined by VREFD, Half VREFD, Auto, VREFD, VREFD MERGE and VREFD Offsets mode registers.
4. VREFD Offsets are not supported with VREFD2.
5. External VREFC is to be provided by the controller as there is no other alternative supply.
6. DQ/$\overline{DBI}$ input slew rate must be greater than or equal to 3V/ns for POD15 and 2.7V/ns for POD135. The slew rate is measured between VREFD crossing and VIHD(AC) or VILD(AC) or VREFD2 crossing and VIHD2(AC) or VILD2(AC).
7. ADR/CMD input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).
8. VIHX and VILX define the voltage levels for the receiver that detects x32 or x16 mode with $\overline{RESET}$ going High.



Output Load Circuit

NOTE : Outputs measured into equivalent load of 1.5pF at a driver impedance of 40 ohm (pull-down) and 60ohm (pull-up).

[Table 33] AC Operating Conditions

Recommended operating conditions (Temp condition: 0°C ≤ Tc ≤ 85°C)

Parameter	Symbol	POD15			POD135			Unit	NOTE
		Min	Typ	Max	Min	Typ	Max		
AC Input Logic HIGH Voltage for address and command	VIHA(AC)	VREFC+0.20			VREFC+0.18			V	
AC Input Logic Low Voltage for address and command	VILA(AC)			VREFC-0.20			VREFC-0.18	V	
AC Input Logic HIGH Voltage for DQ and $\overline{DBI}$ pins with VREFD	VIHD(AC)	VREFD+0.15			VREFD+0.135			V	
AC Input Logic LOW Voltage for DQ and $\overline{DBI}$ pins with VREFD	VILD(AC)			VREFD-0.15			VREFD-0.135	V	
AC Input Logic HIGH Voltage for DQ and $\overline{DBI}$ pins with VREFD2	VIHD2(AC)	VREFD2+0.40			VREFD2+0.36			V	
AC Input Logic LOW Voltage for DQ and $\overline{DBI}$ pins with VREFD2	VILD2(AC)			VREFD2-0.40			VREFD2-0.38	V	

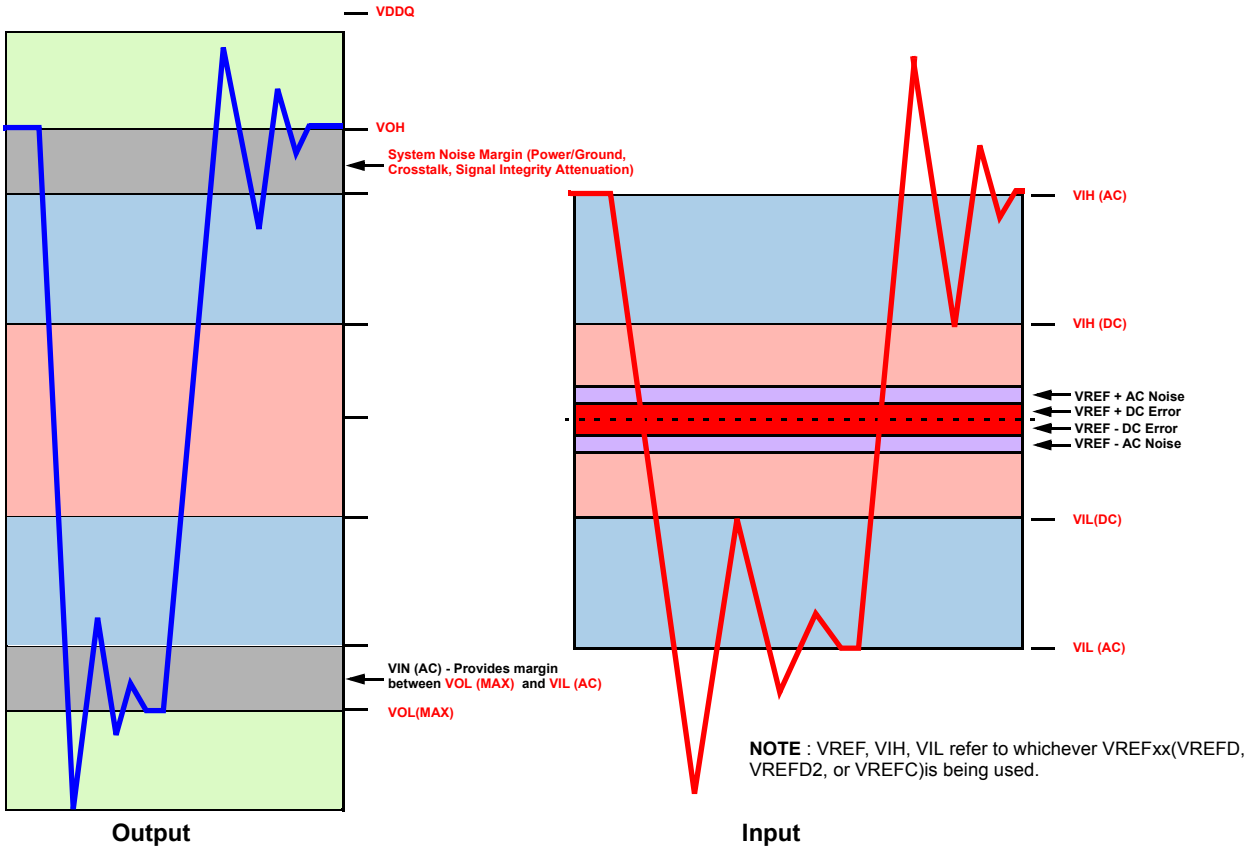
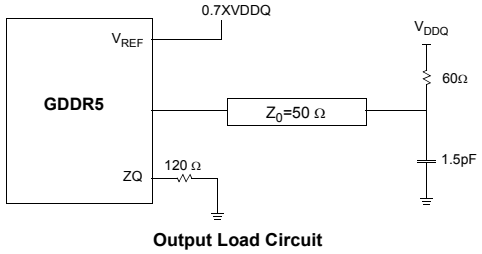


Figure 63. Voltage Waveform



Output Load Circuit

NOTE : Outputs measured into equivalent load of 1.5pF at a driver impedance of 40 ohm (pull-down) and 60ohm (pull-up).

[Table 34] Clock Input Operating Conditions

Recommended operating conditions (0°C ≤ Tc ≤ 85°C)

Parameter/ Condition	Symbol	POD15		POD135		Unit	NOTE
		Min	Max	Min	Max		
Clock Input Mid-Point Voltage; CK and $\overline{CK}$	VMP(DC)	VREFC-0.10	VREFC+0.10	VREFC-0.10	VREFC+0.10	V	1, 6
Clock Input Differential Voltage; CK and $\overline{CK}$	VIDCK(DC)	0.22		0.198		V	4. 6
Clock Input Differential Voltage; CK and $\overline{CK}$	VIDCK(AC)	0.40		0.36		V	2,4,6
Clock Input Differential Voltage; WCK and $\overline{WCK}$	VIDWCK(DC)	0.20		0.18		V	5,7
Clock Input Differential Voltage; WCK and $\overline{WCK}$	VIDWCK(AC)	0.30		0.27			2,5,7
Clock Input Voltage Level;CL and $\overline{CK}$, WCK and $\overline{WCK}$ single ended	VIN	-0.30	VDDQ+0.30	-0.30	VDDQ+0.30		
CK/$\overline{CK}$ Single ended slew rate	CKslew	3		2.7		V/ns	9
WCK/$\overline{WCK}$ Single ended slew rate	WCKSlew	3		2.7		V/ns	10
Clock Input Crossing point Voltage;CK and $\overline{CK}$	VIXCK(AC)	VREFC-0.12	VREFC+0.12	VREFC-0.108	VREFC+0.108	V	2,3,6
Clock Input Crossing point Voltage;WCK and $\overline{WCK}$	VIXWCK(AC)	VREFD-0.10	VREFD+0.10	VREFD-0.09	VREFD+0.09	V	2,3,7,8
Allowed time before ringback of CK/WCK below VIDCK/WCK(AC)	tDVAC					ps	11,12,13

NOTE :

1. This provides a minimum of 0.9V to a maximum of 1.2V, and is nominally 70% of VDDQ with POD15. If POD135, this provides a minimum of 0.845V to a maximum of 1.045V, and is nominally 70% of VDDQ. DRAM timings relative to CK cannot be guaranteed if these limits are exceeded.
2. For AC operations, all DC clock requirements must be satisfied as well.
3. The value of VIXCK and VIXWCK is expected to equal 70% VDDQ for the transmitting device and must track variations in the DC level of the same.
   In case VREFD=0.5xVDDQ, either{VREFD-0.10 ≤ VIXWCK(AC) ≤ VREFD+0.10} or (0.7xVDDQ-0.10 ≤ VIXWCK(AC) ≤ 0.7xVDDQ+0.10} is allowed.
   In case VREFC=0.5xVDDQ, either{VREFC-0.12 ≤ VIXCK(AC) ≤ VREFC+0.12} or (0.7xVDDQ-0.12 ≤ VIXCK(AC) ≤ 0.7xVDDQ+0.12} is allowed.
4. VIDCK is the magnitude of the difference between the input level in CK and the input level on $\overline{CK}$. The input reference level for signals other than CK and $\overline{CK}$ is VREFC.
5. VIDWCK is the magnitude of the difference between the input level in WCK and the input level on $\overline{WCK}$. The input reference level for signals other than WCK and $\overline{WCK}$ is either VREFD, VREFD2 or the internal VREFD.
6. The CK and $\overline{CK}$ input reference level (for timing referenced to CK and $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. Please refer to the applicable timings in the AC timings table (Table 32).
7. The WCK and $\overline{WCK}$ input reference level (for timing referenced to WCK and $\overline{WCK}$) is the point at which WCK and $\overline{WCK}$ cross.
   Please refer to the applicable timings in the AC Timings table
8. VREFD is either VREFD, VREFD2 or the internal VREFD.
9. The slew rate is measured between VREFC crossing and VIXCK(AC).
10. The slew rate is measured between VREFD crossing and VIXWCK(AC).
11. Figure 64 illustrates the exact relationship between (CK/$\overline{CK}$) or (WCK/$\overline{WCK}$) and VID(AC), VID(DC) and tDVAC
12. Ringback below VID(DC) is not allowed.
13. tDVAC is not measured in and of itself as a compliance specification, but is relied upon in measurement of clock operating conditions and clock related parameters.

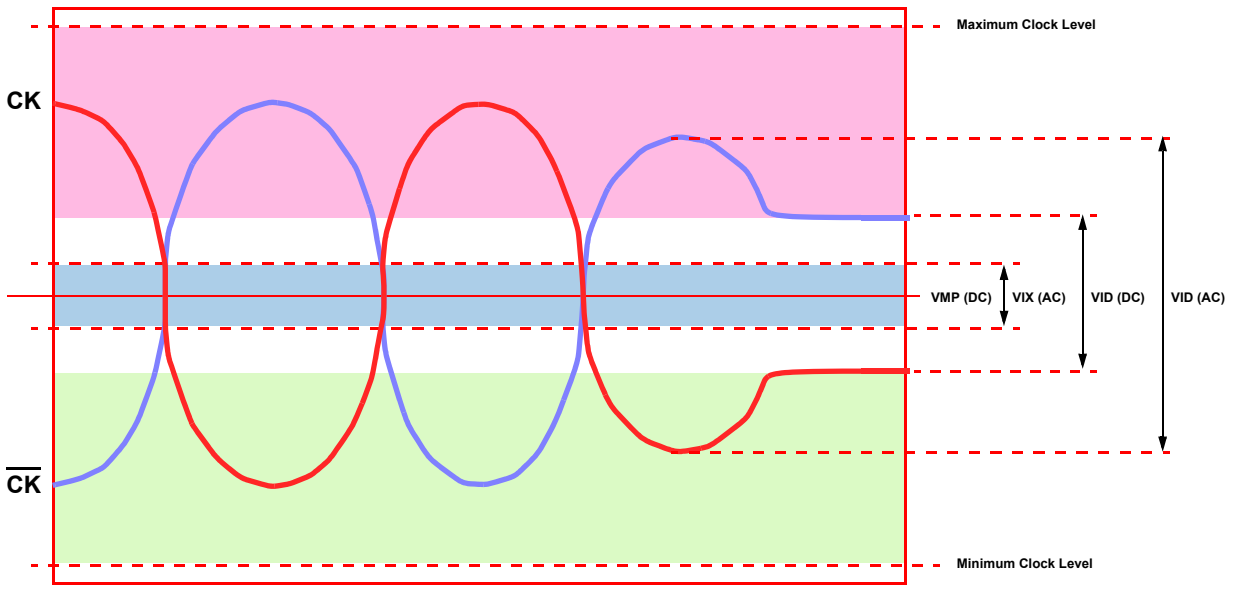


Figure 64. Clock Waveform

[Table 35] IDD Specification and Test Conditions @ VDD=1.5V ± 0.045V, VDDQ=1.5V ± 0.045V

(0°C ≤ Tc ≤ 85°C ; VDD=1.5V ± 0.045V, VDDQ=1.5V ± 0.045V)

Parameter	Symbol	Test Condition	x32 mode			Unit
			HC03	HC28	HC25	
One Bank Activate Pre-charge Current	IDD0	tCK = tCK(min); tWCK = tWCK(min); tRC = tRC(min); $\overline{CKE}$ = LOW; DQ, $\overline{DBI}$ are HIGH; random bank and row addresses (4 address inputs set LOW) with ACT command	300	320	TBD	mA
One Bank Activate Read Precharge Current	IDD1	tCK = tCK (min); tWCK = tWCK(min);tRC = tRC(min); $\overline{CKE}$ = LOW; one bank activated; single read burst with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; otherwise DQ, $\overline{DBI}$ are HIGH; random bank, row and column addresses (4 address inputs set LOW) with ACT and READ commands; IOUT = 0mA	330	360	TBD	mA
Precharge Power down Current	IDD2P	tCK = tCK (min); tWCK = tWCK(min); all banks idle;$\overline{CKE}$ = HIGH; all other inputs are HIGH; PLL/DLLs are off	180	190	TBD	mA
Precharge Standby Current	IDD2N	tCK = tCK (min); tWCK = tWCK(min); all banks idle;$\overline{CKE}$ = LOW; all other inputs are HIGH	200	210	TBD	mA
Active Power down Current	IDD3P	tCK = tCK (min); tWCK = tWCK(min); one bank active;$\overline{CKE}$ = HIGH; all other inputs are HIGH	170	170	TBD	mA
Active Standby Current	IDD3N	tCK = tCK (min); tWCK = tWCK(min); one bank active;$\overline{CKE}$ = LOW; all other inputs are HIGH	280	290	TBD	mA
Read Burst Current	IDD4R	tCK = tCK (min); tWCK = tWCK(min); $\overline{CKE}$ = LOW; one bank in each of the 4 bank groups activated; continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; random bank and column addresses (4 address inputs set LOW) with READ command; IOUT = 0mA	700	770	TBD	mA
Write Burst Current	IDD4W	tCK = tCK (min); tWCK = tWCK(min); $\overline{CKE}$ = LOW; one bank in each of the 4 bank groups activated; continuous write burst across bank groups with 50% data toggle on each data transfer, with 4 inputs per data byte set LOW; random bank and column addresses (4 address inputs set LOW) with WRITE command; no data mask	740	820	TBD	mA
Refresh Current	IDD5	tCK = tCK (min);tWCK = tWCK(min); tRFC =tRFC(min) ;$\overline{CKE}$ = LOW;DQ, $\overline{DBI}$ are HIGH; address inputs are HIGH	650	730	TBD	mA
Self Refresh Current	IDD6	$\overline{CKE}$ = HIGH; all other inputs are HIGH	100	100	TBD	mA
4Bank Interleave Read Current	IDD7	tCK = tCK(min); tWCK = tWCK(min); $\overline{CKE}$ = LOW;one bank in each of the 4 bank groups activated and precharged at tRC(min); continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; random bank, row and column addresses (4 address inputs set LOW) with ACT and READ/READA commands; IOUT = 0mA	910	1030	TBD	mA

NOTE :
1. Measured with outputs open and ODT off
2. Refresh period is 32ms.
3. Min tRC or tRFC for IDD measurements is the smallest multiple of tCK that meets the minimum of the absolute value for the respective parameter.
4. Min tRC or tRFC for IDD measurements is the smallest multiple of tCK that meets the minimum of the absolute value for there spective parameter.

Common Test conditions :
1) Device is configured to x32 mode
2) ABI and DBI are enabled
3) All ODTs are enabled with ZQ/2
4) Optional PLL/DLLs are disabled
5) CRC is enabled for READs and WRITEs, and the EDC hold pattern is programmed to '1010'
6) Bank groups are enabled if required for device operation at tCK(min)
7) Address inputs include $\overline{ABI}$ pin
8) Each data byte consists of eight DQs and one $\overline{DBI}$ pin
9) DESELECT condition during idle command cycles

[Table 36] IDD Specification and Test Conditions @ VDD=1.35V ± 0.0405V, VDDQ=1.35V ± 0.0405V

(0°C ≤ Tc ≤ 85°C ; VDD=1.35V ± 0.0405V, VDDQ=1.35V ± 0.0405V)

Parameter	Symbol	Test Condition	x32 mode			Unit
			HC03	HC28	HC25	
One Bank Activate Pre-charge Current	IDD0	tCK = tCK(min); tWCK = tWCK(min); tRC = tRC(min); $\overline{CKE}$ = LOW; DQ, $\overline{DBI}$ are HIGH; random bank and row addresses (4 address inputs set LOW) with ACT command	250	270	TBD	mA
One Bank Activate Read Precharge Current	IDD1	tCK = tCK (min); tWCK = tWCK(min);tRC = tRC(min); $\overline{CKE}$ = LOW; one bank activated; single read burst with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; otherwise DQ, $\overline{DBI}$ are HIGH; random bank, row and column addresses (4 address inputs set LOW) with ACT and READ commands; IOUT = 0mA	280	310	TBD	mA
Precharge Power down Current	IDD2P	tCK = tCK (min); tWCK = tWCK(min); all banks idle;$\overline{CKE}$ = HIGH; all other inputs are HIGH; PLL/DLLs are off	160	170	TBD	mA
Precharge Standby Current	IDD2N	tCK = tCK (min); tWCK = tWCK(min); all banks idle;$\overline{CKE}$ = LOW; all other inputs are HIGH	170	180	TBD	mA
Active Power down Current	IDD3P	tCK = tCK (min); tWCK = tWCK(min); one bank active;$\overline{CKE}$ = HIGH; all other inputs are HIGH	150	150	TBD	mA
Active Standby Current	IDD3N	tCK = tCK (min); tWCK = tWCK(min); one bank active;$\overline{CKE}$ = LOW; all other inputs are HIGH	230	250	TBD	mA
Read Burst Current	IDD4R	tCK = tCK (min); tWCK = tWCK(min); $\overline{CKE}$ = LOW; one bank in each of the 4 bank groups activated; continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; random bank and column addresses (4 address inputs set LOW) with READ command; IOUT = 0mA	560	620	TBD	mA
Write Burst Current	IDD4W	tCK = tCK (min); tWCK = tWCK(min); $\overline{CKE}$ = LOW; one bank in each of the 4 bank groups activated; continuous write burst across bank groups with 50% data toggle on each data transfer, with 4 inputs per data byte set LOW; random bank and column addresses (4 address inputs set LOW) with WRITE command; no data mask	580	650	TBD	mA
Refresh Current	IDD5	tCK = tCK (min);tWCK = tWCK(min); tRFC =tRFC(min) ;$\overline{CKE}$ = LOW;DQ, $\overline{DBI}$ are HIGH; address inputs are HIGH	550	620	TBD	mA
Self Refresh Current	IDD6	$\overline{CKE}$ = HIGH; all other inputs are HIGH	100	100	TBD	mA
4Bank Interleave Read Current	IDD7	tCK = tCK(min); tWCK = tWCK(min); $\overline{CKE}$ = LOW;one bank in each of the 4 bank groups activated and precharged at tRC(min); continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; random bank, row and column addresses (4 address inputs set LOW) with ACT and READ/ READA commands; IOUT = 0mA	730	820	TBD	mA

NOTE :
1. Measured with outputs open and ODT off
2. Refresh period is 32ms.
3. Min tRC or tRFC for IDD measurements is the smallest multiple of tCK that meets the minimum of the absolute value for the respective parameter.
4. Min tRC or tRFC for IDD measurements is the smallest multiple of tCK that meets the minimum of the absolute value for there spective parameter.

Common Test conditions :
1) Device is configured to x32 mode
2) ABI and DBI are enabled
3) All ODTs are enabled with ZQ/2
4) Optional PLL/DLLs are enabled unless otherwise noted
5) CRC is enabled for READs and WRITEs, and the EDC hold pattern is programmed to '1010'
6) Bank groups are enabled if required for device operation at tCK(min)
7) Address inputs include $\overline{ABI}$ pin
8) Each data byte consists of eight DQs and one $\overline{DBI}$ pin
9) DESELECT condition during idle command cycles

[Table 37] IDD Specification and Test Conditions @ VDD=1.5V ± 0.045V, VDDQ=1.5V ± 0.045V

(0°C ≤ Tc ≤ 85°C ; VDD=1.5V ± 0.045V, VDDQ=1.5V ± 0.045V)

Parameter	Symbol	Test Condition	x16 mode			Unit
			HC03	HC28	HC25	
One Bank Activate Pre-charge Current	IDD0	tCK = tCK(min); tWCK = tWCK(min); tRC = tRC(min); CKE = LOW; DQ, DBI are HIGH; random bank and row addresses (4 address inputs set LOW) with ACT command	250	270	TBD	mA
One Bank Activate Read Precharge Current	IDD1	tCK = tCK (min); tWCK = tWCK(min);tRC = tRC(min); CKE = LOW; one bank activated; single read burst with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; otherwise DQ, DBI are HIGH; random bank, row and column addresses (4 address inputs set LOW) with ACT and READ commands; IOUT = 0mA	270	290	TBD	mA
Precharge Power down Current	IDD2P	tCK = tCK (min); tWCK = tWCK(min); all banks idle;CKE = HIGH; all other inputs are HIGH; PLL/DLLs are off	160	160	TBD	mA
Precharge Standby Current	IDD2N	tCK = tCK (min); tWCK = tWCK(min); all banks idle;CKE = LOW; all other inputs are HIGH	170	180	TBD	mA
Active Power down Current	IDD3P	tCK = tCK (min); tWCK = tWCK(min); one bank active;CKE = HIGH; all other inputs are HIGH	140	150	TBD	mA
Active Standby Current	IDD3N	tCK = tCK (min); tWCK = tWCK(min); one bank active;CKE = LOW; all other inputs are HIGH	220	230	TBD	mA
Read Burst Current	IDD4R	tCK = tCK (min); tWCK = tWCK(min); CKE = LOW; one bank in each of the 4 bank groups activated; continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; random bank and column addresses (4 address inputs set LOW) with READ command; IOUT = 0mA	520	600	TBD	mA
Write Burst Current	IDD4W	tCK = tCK (min); tWCK = tWCK(min); CKE = LOW; one bank in each of the 4 bank groups activated; continuous write burst across bank groups with 50% data toggle on each data transfer, with 4 inputs per data byte set LOW; random bank and column addresses (4 address inputs set LOW) with WRITE command; no data mask	600	670	TBD	mA
Refresh Current	IDD5	tCK = tCK (min);tWCK = tWCK(min); tRFC =tRFC(min) ;CKE = LOW;DQ, DBI are HIGH; address inputs are HIGH	590	660	TBD	mA
Self Refresh Current	IDD6	CKE = HIGH; all other inputs are HIGH	100	100	TBD	mA
4Bank Interleave Read Current	IDD7	tCK = tCK(min); tWCK = tWCK(min); CKE = LOW;one bank in each of the 4 bank groups activated and precharged at tRC(min); continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; random bank, row and column addresses (4 address inputs set LOW) with ACT and READ/READA commands; IOUT = 0mA	700	810	TBD	mA

NOTE :
1. Measured with outputs open and ODT off
2. Refresh period is 32ms.
3. Min tRC or tRFC for IDD measurements is the smallest multiple of tCK that meets the minimum of the absolute value for the respective parameter.
4. Min tRC or tRFC for IDD measurements is the smallest multiple of tCK that meets the minimum of the absolute value for there spective parameter.

Common Test conditions :
1) Device is configured to x16 mode
2) ABI and DBI are enabled
3) All ODTs are enabled with ZQ/2
4) Optional PLL/DLLs are enabled unless otherwise noted
5) CRC is enabled for READs and WRITEs, and the EDC hold pattern is programmed to '1010'
6) Bank groups are enabled if required for device operation at tCK(min)
7) Address inputs include ABI pin
8) Each data byte consists of eight DQs and one DBI pin
9) DESELECT condition during idle command cycles

[Table 38] IDD Specification and Test Conditions @ VDD=1.35V ± 0.0405V, VDDQ=1.35V ± 0.0405V

(0°C ≤ Tc ≤ 85°C ; VDD=1.35V ± 0.0405V, VDDQ=1.35V ± 0.0405V)

Parameter	Symbol	Test Condition	x16 mode			Unit
			HC03	HC28	HC25	
One Bank Activate Pre-charge Current	IDD0	tCK = tCK(min); tWCK = tWCK(min); tRC = tRC(min); $\overline{CKE}$ = LOW; DQ, $\overline{DBI}$ are HIGH; random bank and row addresses (4 address inputs set LOW) with ACT command	210	230	TBD	mA
One Bank Activate Read Precharge Current	IDD1	tCK = tCK (min); tWCK = tWCK(min);tRC = tRC(min); $\overline{CKE}$ = LOW; one bank activated; single read burst with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; otherwise DQ, $\overline{DBI}$ are HIGH; random bank, row and column addresses (4 address inputs set LOW) with ACT and READ commands; IOUT = 0mA	220	250	TBD	mA
Precharge Power down Current	IDD2P	tCK = tCK (min); tWCK = tWCK(min); all banks idle;$\overline{CKE}$ = HIGH; all other inputs are HIGH; PLL/DLLs are off	140	140	TBD	mA
Precharge Standby Current	IDD2N	tCK = tCK (min); tWCK = tWCK(min); all banks idle;$\overline{CKE}$ = LOW; all other inputs are HIGH	140	150	TBD	mA
Active Power down Current	IDD3P	tCK = tCK (min); tWCK = tWCK(min); one bank active;$\overline{CKE}$ = HIGH; all other inputs are HIGH	120	130	TBD	mA
Active Standby Current	IDD3N	tCK = tCK (min); tWCK = tWCK(min); one bank active;$\overline{CKE}$ = LOW; all other inputs are HIGH	180	190	TBD	mA
Read Burst Current	IDD4R	tCK = tCK (min); tWCK = tWCK(min); $\overline{CKE}$ = LOW; one bank in each of the 4 bank groups activated; continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; random bank and column addresses (4 address inputs set LOW) with READ command; IOUT = 0mA	420	480	TBD	mA
Write Burst Current	IDD4W	tCK = tCK (min); tWCK = tWCK(min); $\overline{CKE}$ = LOW; one bank in each of the 4 bank groups activated; continuous write burst across bank groups with 50% data toggle on each data transfer, with 4 inputs per data byte set LOW; random bank and column addresses (4 address inputs set LOW) with WRITE command; no data mask	470	530	TBD	mA
Refresh Current	IDD5	tCK = tCK (min);tWCK = tWCK(min); tRFC =tRFC(min) ;$\overline{CKE}$ = LOW;DQ, $\overline{DBI}$ are HIGH; address inputs are HIGH	500	560	TBD	mA
Self Refresh Current	IDD6	$\overline{CKE}$ = HIGH; all other inputs are HIGH	100	100	TBD	mA
4Bank Interleave Read Current	IDD7	tCK = tCK(min); tWCK = tWCK(min); $\overline{CKE}$ = LOW;one bank in each of the 4 bank groups activated and precharged at tRC(min); continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; random bank, row and column addresses (4 address inputs set LOW) with ACT and READ/READA commands; IOUT = 0mA	560	640	TBD	mA

NOTE :
1. Measured with outputs open and ODT off
2. Refresh period is 32ms.
3. Min tRC or tRFC for IDD measurements is the smallest multiple of tCK that meets the minimum of the absolute value for the respective parameter.
4. Min tRC or tRFC for IDD measurements is the smallest multiple of tCK that meets the minimum of the absolute value for there spective parameter.

Common Test conditions :
1) Device is configured to x16 mode
2) ABI and DBI are enabled
3) All ODTs are enabled with ZQ/2
4) Optional PLL/DLLs are enabled unless otherwise noted
5) CRC is enabled for READs and WRITEs, and the EDC hold pattern is programmed to '1010'
6) Bank groups are enabled if required for device operation at tCK(min)
7) Address inputs include $\overline{ABI}$ pin
8) Each data byte consists of eight DQs and one $\overline{DBI}$ pin
9) DESELECT condition during idle command cycles

[Table 39] AC Timings @ VDD=1.5V ± 0.045V, VDDQ=1.5V ± 0.045V

PARAMETER 1, 2	Symbol	Value		Unit	NOTE
		Min	Max		
CK and WCK timings					
CK Clock cycle time	tCK	0.57	20	ns	1
CK clock high-level width	tCH	0.45	0.55	tCK	3
CK clock low-level width	tCL	0.45	0.55	tCK	3
Min. CK clock half period	tHP	min(tCH, tCL)	-	tCK	
Max. CK clock frequency with bank groups disabled	fCKBG	-	2000	MHz	4
Max. CK clock frequency with bank groups enabled and tCCDL=3*tCK	fCKBG4	-	2000	MHz	4
Max. CK clock frequency with WCK2CK alignment at pins	fCKPIN	-	500	MHz	5
Max. CK clock frequency in RDQS Mode	fCKRDQS	-	500	MHz	6
Max. CK clock frequency for WCK to CK auto synchronization in WCK2CK training mode	fCKAUTOSYNC	-	500	MHz	8
Max. CK clock frequency for device operation with Low Frequency Mode enabled	fCKLF	-	500	MHz	10
WCK clock cycle time	tWCK	0.29	10	ns	11
WCK clock high-level width	tWCKH	0.45	0.55	tWCK	12, 13
WCK clock low-level width	tWCKL	0.45	0.55	tWCK	12, 13
Min. WCK clock half period	tWCKHP	Min (tWCKH, tWCKL)	-	tWCK	
Command and Address Input Timings					
Command Input setup time	tCMDS	0.15	-	ns	14, 15
Command Input hold time	tCMDH	0.15	-	ns	14, 15
Command Input pulse width	tCMDPW	0.5	-	ns	14,15,16
Address Input setup time	tAS	0.1	-	ns	14,15,17
Address Input hold time	tAH	0.1	-	ns	14,15,17
Address Input pulse width	tAPW	0.25	-	ns	14,15, 16,17
WCK-to-CK Timings					
WCK stop to MRS delay for entering WCK-to-CK training	tWCK2MRS	3tCK+10ns	-	ns	
MRS to WCK restart delay after entering WCK-to-CK training	tMRSTWCK	3tCK+10ns	-	ns	18
WCK start to WCK phase movement delay	tWCK2TR	10	-	tCK	
WCK Phase change to phase detector out delay	tWCK2PH	10	-	ns	
WCK clock high-level width during WCK-to-CK training	tWCKHTR	0.43	0.57	tWCK	12,13,19
WCK clock low-level width during WCK to CK training	tWCKLTR	0.43	0.57	tWCK	12,13,19
WCK-to-CK offset when zero offset at phase detector	tWCK2CKPIN	-0.2	0.2	ns	20
WCK-to-CK phase offset upon WCK-to-CK training exit	tWCK2CKSYNC	-0.2	0.2	tCK	21

PARAMETER 1, 2		Symbol	Value		Unit	NOTE
			Min	Max		
WCK-to-CK Timings						
WCK-to-CK phase offset		tWCK2CK	-0.4	0.4	tCK	22
Data Input and Output Timings						
WCK to DQ/$\overline{DBI}$ offset for Input data		tWCK2DQI	0.1	1.1	ns	23
WCK to DQ/$\overline{DBI}$/EDC offset for output data		tWCK2DQO	0.4	1.4	ns	24,25
DQ/$\overline{DBI}$ Input pulse width		tDIPW	120	-	ps	26,27,28
DQ/$\overline{DBI}$ data Input valid window		tDIVW	100	-	ps	26,27,29
DQ/$\overline{DBI}$ input skew within double byte		tDQDQI	-100	100	ps	30
DQ/$\overline{DBI}$/EDC output Skew within Double byte		tDQDQO	-125	125	ps	31
Row Access Timings						
Active to Active command period		tRC	-	-	ns	
Active to Precharge command period		tRAS	-	-	ns	32
Active to Read command delay		tRCDRD	-	-	ns	
Active to Write command delay		tRCDWR	-	-	ns	
Active to RDTR command delay		tRCDRTR	-	-	ns	
Active to WRTR command delay		tRCDWTR	-	-	ns	
Active to LDFF command delay		tRCDLTR	-	-	ns	
Refresh to RDTR or WRTR command delay		tREFTR	-	-	ns	
Active Bank A to Active Bank B command delay Same Bank Group		tRRDL	-	-	ns	33
Active Bank A to Active Bank B command delay Different Bank Group		tRRDS	-	-	ns	34
Four Bank Activate Window		tFAW	-	-	ns	35
Thirtytwo Bank Activate Window		t32AW	-	-	ns	36
Read to Precharge command delay same Bank With Bank Groups enabled		tRTPL	-	-	tCK	37
Read to Precharge command delay other Bank or With Bank Groups disabled		tRTPS	-	-	tCK	38
Precharge to Precharge command delay		tPPD	-	-	ns	
Precharge command period		tRP	-	-	ns	
Write recovery time		tWR	-	-	ns	
Auto precharge write recovery + precharge time		tDAL	-	-	tCK	39
Column Access Timings						
Cas latency	DBI off	CL	-	-	ns	52
	DBI on		-	-		
RD/WR Bank A to RD/WR Bank B command delay Same Bank Group	MR3A11/A10=1/1	tCCDL	3	-	tCK	33
	MR3A11/A10=1/0		4	-		
RD/WR Bank A to RD/WR Bank B command delay Different Bank Groups		tCCDS	2	-	tCK	34,41
LDFF to LDFF command cycle time		tLTLTR	4	-	tCK	
LDFF(111) to LDFF command cycle time		tLTL7TR	4	-	tCK	42
LDFF(111) to RDTR command delay		tLTRTR	4	-	tCK	

PARAMETER 1, 2		Symbol	Value		Unit	NOTE
			Min	Max		
Read or RDTR to LDFF command delay		tRDTLT	CLmrs+5	-	tCK	
Write to LDFF command delay		tWRTLT	WLmrs+6	-	tCK	
WRTR to RDTR command delay		tWTRTR	WLmrs+4	-	tCK	
Write to WRTR command delay		tWRWTR	2	-	tCK	
Internal Write to Read command delay Same Bank Groups		tWTRL	4tCK+4	-	ns	33
Internal Write to Read command delay Different Bank Groups		tWTRS	2tCK+4	-	ns	34
Read or RDTR to Write or WRTR command delay		tRTW	CLmrs+BL/4 - WLmrs +(bus turn-around time)/tCK+3	-	tCK	43
Write Latency		tWL	2~7	-	tCK	44
Power-Down and Refresh Timings						
$\overline{CKE}$ min. high and low pulse width		tCKE	10	-	tCK	
Valid CK clocks required after self refresh entry		tCKSRE	10	-	tCK	
Valid CK clocks required before self refresh exit		tCKSRX	10	-	tCK	
Read to Self refresh entry or Power down Entry command delay		tRDSRE	CLmrs+CRCRL+6	-	tCK	45
Write to Self refresh entry or Power down Entry command delay		tWRSRE	WLmrs+ max(tDAL/tCK+6, CRCWL+6)	-	tCK	46
Refresh command period		tRFC	110	-	ns	
Exit self refresh to non-Read/Write command delay		tXS	tRFC	-	tCK	47
Refresh period		tREF	-	32	ms	
Average periodic refresh interval	8K rows	tREFI	-	-	us	48
	16K rows		-	1.9		
Min. power down entry to exit time		tPD	10	19*tREFI	ns	
Nop/Deselect commands required upon power down and self refresh entry		tCPDED	4	-	tCK	
Power-down exit time		tXPN	12	-	tCK	
Miscellaneous Timings						
Mode Register Set command period		tMRD	max(10ns/tCK,10)	-	tCK	
DVS voltage stabilization time		tVS	-	-	us	
Refresh to calibration update complete delay		tKO	-	1tCK+12ns	tCK+ns	
Active termination setup time		tATS	10	-	ns	
Active termination hold time		tATH	10	-	ns	
Read to data out delay in address training mode		tADR	-	2tCK+10ns	tCK+ns	18
Address training exit to DQ in ODT state delay		tADZ	-	1tCK+10ns	tCK+ns	
Vendor ID On		tWRIDON	-	1tCK+10ns	tCK+ns	
Vendor ID off		tWRIDOFF	-	1tCK+10ns	tCK+ns	
Temperature sensor enable delay		tTSEN	-	-	us	

[Table 40] AC Timings@ VDD=1.35V ± 0.0405V, VDDQ=1.35V ± 0.0405V

PARAMETER 1, 2	Symbol	Value		Unit	NOTE
		Min	Max		
CK and WCK timings					
CK Clock cycle time	tCK	0.8	20	ns	1
CK clock high-level width	tCH	0.45	0.55	tCK	3
CK clock low-level width	tCL	0.45	0.55	tCK	3
Min. CK clock half period	tHP	min(tCH, tCL)	-	tCK	
Max. CK clock frequency with bank groups disabled	fCKBG	-	1500	MHz	4
Max. CK clock frequency with bank groups enabled and tCCDL=3*tCK	fCKBG4	-	1500	MHz	4
Max. CK clock frequency with WCK2CK alignment at pins	fCKPIN	-	500	MHz	5
Max. CK clock frequency in RDQS Mode	fCKRDQS	-	500	MHz	6
Max. CK clock frequency for WCK to CK auto synchronization in WCK2CK training mode	fCKAUTOSYNC	-	500	MHz	8
Max. CK clock frequency for device operation with Low Frequency Mode enabled	fCKLF	-	500	MHz	10
WCK clock cycle time	tWCK	0.4	10	ns	11
WCK clock high-level width	tWCKH	0.45	0.55	tWCK	12, 13
WCK clock low-level width	tWCKL	0.45	0.55	tWCK	12, 13
Min. WCK clock half period	tWCKHP	min (tWCKL, tWCKH)	-	tWCK	
Command and Address Input Timings					
Command Input setup time	tCMDS	0.2	-	ns	14, 15
Command Input hold time	tCMDH	0.2	-	ns	14, 15
Command Input pulse width	tCMDPW	0.56	-	ns	14,15,16
Address Input setup time	tAS	0.1	-	ns	14,15,17
Address Input hold time	tAH	0.1	-	ns	14,15,17
Address Input pulse width	tAPW	0.28	-	ns	14,15, 16,17
WCK-to-CK Timings					
WCK stop to MRS delay for entering WCK-to-CK training	tWCK2MRS	3tCK+11ns	-	ns	
MRS to WCK restart delay after entering WCK-to-CK training	tMRSTWCK	3tCK+11ns	-	ns	18
WCK start to WCK phase movement delay	tWCK2TR	10	-	tCK	
WCK Phase change to phase detector out delay	tWCK2PH	11	-	ns	
WCK clock high-level width during WCK-to-CK training	tWCKHTR	0.43	0.57	tWCK	12,13,19
WCK clock low-level width during WCK to CK training	tWCKLTR	0.43	0.57	tWCK	12,13,19
WCK-to-CK offset when zero offset at phase detector	tWCK2CKPIN	-0.2	0.2	ns	20
WCK-to-CK phase offset upon WCK-to-CK training exit	tWCK2CKSYNC	-0.2	0.2	tCK	21

PARAMETER 1, 2		Symbol	Value		Unit	NOTE
			Min	Max		
WCK-to-CK Timings						
WCK-to-CK phase offset		tWCK2CK	-0.4	0.4	tCK	22
Data Input and Output Timings						
WCK to DQ/$\overline{DBI}$ offset for Input data		tWCK2DQI	0	1	ns	23
WCK to DQ/$\overline{DBI}$/EDC offset for output data		tWCK2DQO	0.2	1.2	ns	24,25
DQ/$\overline{DBI}$ Input pulse width		tDIPW	132	-	ps	26,27,28
DQ/$\overline{DBI}$ data Input valid window		tDIVW	120	-	ps	26,27,29
DQ/$\overline{DBI}$ input skew within double byte		tDQDQI	-100	100	ps	30
DQ/$\overline{DBI}$/EDC output Skew within Double byte		tDQDQO	-125	125	ps	31
Row Access Timings						
Active to Active command period		tRC	-	-	ns	
Active to Precharge command period		tRAS	-	-	ns	32
Active to Read command delay		tRCDRD	-	-	ns	
Active to Write command delay		tRCDWR	-	-	ns	
Active to RDTR command delay		tRCDRTR	-	-	ns	
Active to WRTR command delay		tRCDWTR	-	-	ns	
Active to LDFF command delay		tRCDLTR	-	-	ns	
Refresh to RDTR or WRTR command delay		tREFTR	-	-	ns	
Active Bank A to Active Bank B command delay Same Bank Group		tRRDL	-	-	ns	33
Active Bank A to Active Bank B command delay Different Bank Group		tRRDS	-	-	ns	34
Four Bank Activate Window		tFAW	-	-	ns	35
Thirtytwo Bank Activate Window		t32AW	-	-	ns	36
Read to Precharge command delay same Bank With Bank Groups enabled		tRTPL	-	-	tCK	37
Read to Precharge command delay other Bank or With Bank Groups disabled		tRTPS	-	-	tCK	38
Precharge to Precharge command delay		tPPD	-	-	ns	
Precharge command period		tRP	-	-	ns	
Write recovery time		tWR	-	-	ns	
Auto precharge write recovery + precharge time		tDAL	-	-	tCK	39
Column Access Timings						
Cas latency	DBI off	CL	-	-	ns	52
	DBI on		-	-		
RD/WR Bank A to RD/WR Bank B command delay Same Bank Group	MR3A11/A10=1/1	tCCDL	3	-	tCK	33
	MR3A11/A10=1/0		4	-		
RD/WR Bank A to RD/WR Bank B command delay Different Bank Groups		tCCDS	2	-	tCK	34,41
LDFF to LDFF command cycle time		tLTLTR	5	-	tCK	
LDFF(111) to LDFF command cycle time		tLTL7TR	5	-	tCK	42
LDFF(111) to RDTR command delay		tLTRTR	5	-	tCK	

PARAMETER 1, 2		Symbol	Value		Unit	NOTE
			Min	Max		
Read or RDTR to LDFF command delay		tRDTLT	CLmrs+6	-	tCK	
Write to LDFF command delay		tWRTLT	WLmrs+7	-	tCK	
WRTR to RDTR command delay		tWTRTR	WLmrs+5	-	tCK	
Write to WRTR command delay		tWRWTR	3	-	tCK	
Internal Write to Read command delay Same Bank Groups		tWTRL	4tCK+4	-	ns	33
Internal Write to Read command delay Different Bank Groups		tWTRS	2tCK+4	-	ns	34
Read or RDTR to Write or WRTR command delay		tRTW	CLmrs+BL/4-WLmrs+(bus turnaround time)/tCK+3	-	tCK	43
Write Latency		tWL	2~7	-	tCK	44
Power-Down and Refresh Timings						
$\overline{CKE}$ min. high and low pulse width		tCKE	10	-	tCK	
Valid CK clocks required after self refresh entry		tCKSRE	10	-	tCK	
Valid CK clocks required before self refresh exit		tCKSRX	10	-	tCK	
Read to Self refresh entry or Power down Entry command delay		tRDSRE	CLmrs+CRCRL+6	-	tCK	45
Write to Self refresh entry or Power down Entry command delay		tWRSRE	WLmrs+ max(tDAL/tCK+6, CRCWL+6)	-	tCK	46
Refresh command period		tRFC	110	-	ns	
Exit self refresh to non-Read/Write command delay		tXS	tRFC	-	tCK	47
Refresh period		tREF	-	32	ms	
Average periodic refresh interval	8K rows	tREFI	-	-	us	48
	16K rows		-	1.9		
Min. power down entry to exit time		tPD	10	19*tREFI	ns	
Nop/Deselect commands required upon power down and self refresh entry		tCPDED	4	-	tCK	
Power-down exit time		tXPN	12	-	tCK	
Miscellaneous Timings						
Mode Register Set command period		tMRD	max(10ns/tCK,10)	-	tCK	
DVS voltage stabilization time		tVS	-	-	us	
Refresh to calibration update complete delay		tKO	-	1tCK+12ns	tCK+ns	
Active termination setup time		tATS	12	-	ns	
Active termination hold time		tATH	12	-	ns	
Read to data out delay in address training mode		tADR	-	2*tCK+12ns	tCK+ns	18
Address training exit to DQ in ODT state delay		tADZ	-	1*tCK+12ns	tCK+ns	
Vendor ID On		tWRIDON	-	1*tCK+12ns	tCK+ns	
Vendor ID off		tWRIDOFF	-	1*tCK+12ns	tCK+ns	
Temperature sensor enable delay		tTSEN	-	-	us	

NOTE :

1. All parameters assume proper device initialization. And tCK max of PLL off is design target for 20ns.
2. Tests for AC timing may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.
3. CK an $\overline{CK}$ single-ended input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFC crossing and VIXCK(AC).
4. Parameter fCKBG4 is required for those devices supporting both 3*tCK and 4*tCK settings for Bank Groups. Devices supporting only 3*tCK or 4*tCK need only to specify fCKBG.
5. Parameter fCKPIN applies when the alignment point in MR6, bit A0 is set to "at pins", the phase difference between the WCK and CK clocks at the DRAM pins is within tWCK2CKSYNC or tWCK2CK for pin mode, and no phase search in WCK2CK training is performed.
6. Parameter fCKRDQS applies when RDQS Mode is enabled in MR3, bit A5.
7. Parameter fCKVREFD2 applies when the data input reference voltage in MR7, bit A7 (Half VREFD) is set to VREFD2. Half VREFD is optional.
8. Parameter fCKAUTOSYNC applies when WCK2CK Auto Synchronization is enabled in MR7, bit A4. WCK2CK Auto Synchronization is optional.
9. Parameter fCKLP1 applies when Low Power Mode LP1 is enabled in MR5, bit A0. LP1 is optional.
10. Parameter fCKLF applies when Low Frequency Mode is enabled in MR7, bit A3. Low Frequency Mode is optional.
11. By definition the nominal WCK clock cycle time always is 1/2 of the CK clock cycle time (not including jitter).
12. WCK and $\overline{WCK}$ single-ended input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFD crossing and Vixwck(AC).
13. The phase relationship between WCK/$\overline{WCK}$ and CK/$\overline{CK}$ clocks must meet the tWCK2CK specification.
14. Command and address input timings are referenced to VREFC.
15. Command and address input slew rate must be Š 3V/ns. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).
16. Command and address input pulse widths are design targets. The values will be characterized but not tested on each device.
17. Address input timings are only valid with ABI being enabled and a maximum of 4 address inputs driven LOW.
18. Parameter may be specified as a combination of tCK and ns.
19. Parameters tWCKHTR and tWCKLTR specify the max. allowed WCK clock-to-clock phase shift during WCK-to-CK training.
    For READ and WRITE bursts use tWCKH and tWCKL.
20. Parameter tWCK2CKPIN defines the WCK-to-CK phase offset range at the CK and WCK pins for ideal (phase = 0°) clock alignment at the DRAM's phase detector (when the alignment point in MR6, bit A0 is set to "at phase detector"), or at the WCK and CK pins (when the alignment point in MR6, bit A0 is set to "at pins"). The minimum and maximum values could be negative or positive numbers, depending on the selected WCK-to-CK alignment point, PLL-on or PLL-off mode and design implementation.
21. Parameter tWCK2CKSYNC defines the max. phase offset from the ideal (phase = 0°) clock alignment at the DRAM's phase detector(when the alignment point in MR6, bit A0 is set to "at phase detector"), or at the WCK and CK pins (when the alignment point in MR6, bit A0 is set to "at pins"), where the internal logic synchronizes the CK and WCK clocks; it is expected to be a fraction of tWCK2CK.
22. Parameter tWCK2CK defines the max. phase offset from the ideal (phase = 0°) clock alignment at the DRAM's phase detector (when the alignment point in MR6, bit A0 is set to "at phase detector"), or at the WCK and CK pins (when the alignment point in MR6, bit A0 is set to "at pins"), for stable device operation.
23. Parameter tWCK2DQI defines the WCK to DQ/$\overline{DBI}$ time delay range for WRITEs for PLL-on and PLL-off modes. The minimum and maximum values could be negative or positive numbers, depending on design implementation and PLL-on or PLL-off mode. They also vary across PVT. Data training is required to determine the actual tWCK2DQI value for reliable WRITE operation.
24. Parameter tWCK2DQO defines the WCK to DQ/$\overline{DBI}$ time delay range for READs for PLL-on and PLL-off modes. The minimum and maximum values could be negative or positive numbers, depending on design implementation and PLL-on or PLL-off mode.
    They also vary across PVT. Data training is required to determine the actual tWCK2DQO value for reliable READ operation.
25. Outputs measured with equivalent load (vendor specific) terminated with 60 Ohms to VDDQ.
26. DQ/$\overline{DBI}$ input timings are valid only with DBI being enabled and a maximum of 4 data inputs per byte driven LOW.
27. Data input slew rate must be Š 3V/ns. The slew rate is measured between VREFD crossing and VIHD(AC) or VILD(AC).
28. The data input pulse width, tDIPW, defines the minimum positive or negative input pulse width for any one worst-case channel required for proper propagation of an external signal to the receiver. tDIPW is measured at the pins. tDIPW is independent of the PLL/DLL mode. In general tDIPW is larger than tDIVW.
29. The data input valid window, tDIVW, defines the time region where input data must be valid for reliable data capture at the receiver for any one worst case channel. It accounts for jitter between data and clock at the latching point introduced in the path between the DRAM pads and the latching point. Any additional jitter introduced into the source signals (e.g. within the system before the DRAM pad) must be accounted for in the final timing budget together with the chosen PLL/DLL mode and bandwidth. tDIVW is measured at the pins. tDIVW is defined for PLL/DLL off and on mode separately. In the case of PLL/DLL on, tDIVW must be specified for each supported bandwidth. In general tDIVW is smaller than tDIPW.
30. tDQDQI defines the maximum skew among all DQ/$\overline{DBI}$ inputs of a double byte (when configured to x32 mode) or a single byte (when configured to x16 mode) under worst case conditions. Parameter tWCK2DQI defines the mean value of the earliest and latestDQ/$\overline{DBI}$ pin, tDQDQI(min) the negative offset to tWCK2DQI for the earliest DQ/$\overline{DBI}$ pin and tDQDQI(max) the positive offset to tWCK2DQI for the latest DQ/$\overline{DBI}$ pin.
31. tDQDQO defines the maximum skew among all DQ/$\overline{DBI}$ outputs of a double byte (when configured to x32 mode) or a single byte (when configured to x16 mode) under worst case conditions. Parameter tWCK2DQO defines the mean value of the earliest and latest DQ/$\overline{DBI}$/EDC pin, tDQDQO(min) the negative offset to tWCK2DQO for the earliest DQ/$\overline{DBI}$/EDC pin and tDQDQO(max) the positive offset to tWCK2DQO for the latest DQ/$\overline{DBI}$/EDC pin.
32. For READs and WRITEs with AUTO PRECHARGE enabled the device will hold off the internal PRECHARGE until tRAS(min) has been satisfied.
33. Parameter applies when bank groups are enabled and consecutive commands access the same bank group.
34. Parameter applies when bank groups are disabled or consecutive commands access different bank groups.
35. Not more than 4 ACTIVE commands are allowed within period.
36. Not more than 32 ACTIVE commands are allowed within t32AW period. The parameter need not to be specified in case t32AW(min) would not be greater than 8 * tFAW(min).
37. Parameter applies when bank groups are enabled and READ and PRECHARGE commands access the same bank.
38. Parameter applies when bank groups are disabled or READ and PRECHARGE commands access different banks.
39. tDAL = (tWR/tCK) + (tRP/tCK). For each of the terms, if not already an integer, round up to the next integer.
40. tCCDL is either for gapless consecutive READ or gapless consecutive WRITE commands.

41. tCCDS is either for gapless consecutive READ or RDTR (any combination), gapless consecutive WRITE, or gapless consecutive WRTR commands.
42. The min. value is vendor specific and does not exceed 8 tCK.
43. tRTW is not a device limit but determined by the system bus turnaround time. The difference between tWCK2DQO and tWCK2DQI shall be considered in the calculation of the bus turnaround time.
44. The WRITE latency WLmrs can be set to 3 .. 7 clocks. When the WRITE latency is set to small values (e.g. 3 or 4 clocks), the input buffers are always on, reducing the latency but adding power. When the WRITE latency is set to larger values (e.g. 6 or 7 clocks) the input buffers are turned on with the WRITE command, thus saving power. Vendor specifications should be checked for value(s) of WL supported and the specific value(s) of WL where the input receivers are always on or only turn on when the WRITE command is registered.
45. Read data including CRC data must have been clocked out before entering self refresh or power-down mode.
46. Write data must have been written to the memory core, and CRC data must have been clocked out before entering self refresh or power-down mode.
47. Time for WCK2CK training and data training not included.
48. A maximum of 8 consecutive REFRESH commands can be posted to a GDDR5 SGRAM device, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is 9 * tREFI.
49. Replaces parameter tLK when PLL Fast Lock has been enabled prior to the PLL/DLL enable or reset.
50. Replaces parameter tLK when PLL Standby has been enabled and the WCK clock frequency has not changed while in standby mode.
51. The PLL standby time tSTDBY is measured from self refresh entry until after self refresh exit a subsequent PLL/DLL reset is given (with PLL Standby enabled).
52. CAS latecy(CL) and CRC latency(CRCWL, CRCRL) are described based on speed bin on the Tabel 8 of page 30.

18.4 CLOCK-TO-DATA TIMING SENSITIVITY

The availability of clock-to-data (WCK2DQ) timing sensitivity information provides the controller the opportunity to anticipate the impact to timings from variations in environmental conditions (such as changes in voltage or temperature) allowing the controller to take corrective action if necessary (e.g. realigning WCK and DQ). Variations in relative timing between WCK and data are reported for READ and WRITE paths. This specification calls out one zone each for VDDQ, VDD, and Tcase temperature over a specified range. Vendors may choose to provide information for additional zones covering, in total, a wider range or a finer granularity or both.
However, within a given zone if an approximated value (i.e. the specified slope) deviates from the characterized slope to such a degree that the approximated WCK-to-DQ time delay would be in error by more than 5% of one UI relative to the characterized delay then the splitting of this zone into more than one zone is required. All zones and their associated specified slopes must form a continuous piece-wise-linear curve such that, after calibration during normal operation, traversing the approximated curve (i.e. the set of specified slopes) does not lead to time delay errors in excess of the 5% of one UI.

Table 41, Table 42 and Table 43 below describe the minimum set of defined zones

[Table 41] VDDQ Voltage Zones

	VDDQ High	VDDQ Low	NOTE
Zone_VQ1	VDDQ(max)	VDDQ(min)	1

NOTE :
1. VDDQ(max) is the maximum specified operating voltage. VDDQ(min) is the minimum specified operating voltage.

[Table 42] VDD Voltage Zones

	VDD High	VDD Low	NOTE
Zone_VD1	VDD(max)	VDD(min)	1

NOTE :
1. VDD(max) is the maximum specified operating voltage. VDD(min) is the minimum specified operating voltage.

[Table 43] Tcase Temperature Zones

	Tcase High	Tcase Low	NOTE
Zone_T1	Tcase(max)	10°C	1

NOTE :
1. Tcase(max) is the maximum specified operating temperature.

As noted, variations in relative timing are reported for READ and WRITE paths. Table 44, Table 45 and Table 46 below provide information for READ timings while Table 47, Table 48 and Table 49 provide information for WRITE timings.

[Table 44] WCK-to-Data READ Timing Sensitivity to VDDQ

Parameter	Symbol	Values	Units	NOTE
WCK2DQO Sensitivity to variations in VDDQ for zone_VQ1	$t_{O2VQSensZ1}$	300	ps/V	1, 2

NOTE :
1. Calculation of tO2VQSensZ1 is performed as follows:
   tO2VQSensZ1 equals the quantity (tWCK2DQO(Zone_VQ1(max)) - tWCK2DQO(Zone_VQ1(min)))
   divided by (VDDQ(Zone_VQ1(max)) - VDDQ(Zone_VQ1(min)))
   = (tWCK2DQO(VDDQ(max)) - tWCK2DQO(VDDQ(min))) / (VDDQ(max) - VDDQ(min)).
2. VDD=1.5V, Tcase = 85°C, worst-case process corner.

[Table 45] WCK-to-Data READ Timing Sensitivity to VDD

Parameter	Symbol	Values	Units	NOTE
WCK2DQO Sensitivity to variations in VDD for zone_VD1	$t_{O2VDSensZ1}$	100	ps/V	1, 2

NOTE :
1. Calculation of tO2VDSensZ1 is performed as follows:
   tO2VDSensZ1 equals the quantity (tWCK2DQO(Zone_VD1(max)) - tWCK2DQO(Zone_VD1(min)))
   divided by (VDD(Zone_VD1(max)) - VDD(Zone_VD1(min)))
   = (tWCK2DQO(VDD(max)) - tWCK2DQO(VDD(min))) / (VDD(max) - VDD(min)).
2. VDDQ=1.5V, Tcase = 85°C, worst-case process corner.

[Table 46] WCK-to-Data READ Timing Sensitivity to Tcase

Parameter	Symbol	Values	Units	NOTE
WCK2DQO Sensitivity to variations in Tcase for zone_T1	$t_{O2TSensZ1}$	0.6	ps/°C	1, 2

NOTE :
1. Calculation of tO2TSensZ1 is performed as follows:
   tO2TSensZ1 equals the quantity (tWCK2DQO(Zone_T1(max)) - tWCK2DQO(Zone_T1(min)))
   divided by (Tcase(Zone_T1(max)) - Tcase(Zone_T1(min)))
   = (tWCK2DQO(Tcase(max)) - tWCK2DQO(Tcase(min))) / (Tcase(max) - Tcase(min)).
2. VDDQ=1.5V, VDD(typ), worst-case process corner.

Table 47, Table 48 and Table 49 below provide information for WRITE timings.

[Table 47] WCK-to-Data WRITE Timing Sensitivity to VDDQ

Parameter	Symbol	Values	Units	NOTE
WCK2DQI Sensitivity to variations in VDDQ for zone_VQ1	$t_{I2VQSensZ1}$	140	ps/V	1, 2

NOTE :
1. Calculation of tI2VQSensZ1 is performed as follows:
   tI2VQSensZ1 equals the quantity (tWCK2DQI(Zone_VQ1(max)) - tWCK2DQI(Zone_VQ1(min)))
   divided by (VDDQ(Zone_VQ1(max)) - VDDQ(Zone_VQ1(min)))
   = (tWCK2DQI(VDDQ(max)) - tWCK2DQI(VDDQ(min))) / (VDDQ(max) - VDDQ(min)).
2. VDD=1.5V, Tcase = 85°C, worst-case process corner.

[Table 48] WCK-to-Data WRITE Timing Sensitivity to VDD

Parameter	Symbol	Values	Units	NOTE
WCK2DQI Sensitivity to variations in VDD for zone_VD1	$t_{I2VDSensZ1}$	100	ps/V	1, 2

NOTE :
1. Calculation of tO2VDSensZ1 is performed as follows:
   tI2VDSensZ1 equals the quantity (tWCK2DQI(Zone_VD1(max)) - tWCK2DQI(Zone_VD1(min)))
   divided by (VDD(Zone_VD1(max)) - VDD(Zone_VD1(min)))
   = (tWCK2DQI(VDD(max)) - tWCK2DQI(VDD(min))) / (VDD(max) - VDD(min)).
2. VDDQ=1.5V, Tcase = 85°C, worst-case process corner.

[Table 49] WCK-to-Data WRITE Timing Sensitivity to Tcase

Parameter	Symbol	Values	Units	NOTE
WCK2DQI Sensitivity to variations in Tcase for zone_T1	$t_{I2TSensZ1}$	0.4	ps/°C	1, 2

NOTE :
1. Calculation of tO2TSensZ1 is performed as follows:
   tO2TSensZ1 equals the quantity (tWCK2DQO(Zone_T1(max)) - tWCK2DQO(Zone_T1(min)))
   divided by (Tcase(Zone_T1(max)) - Tcase(Zone_T1(min)))
   = (tWCK2DQO(Tcase(max)) - tWCK2DQO(Tcase(min))) / (Tcase(max) - Tcase(min)).
2. VDDQ=1.5V, VDD(typ), worst-case process corner.