

1. del IFPAB DP CO-ALY,add
IFPDEF DP
2. Change DP to use Link-D(11/1/6)
3. add C3756,C3757., change C1,C980 to 0603 3/7

PG174-A01


TU117, 128b GDDR5 x32, 75W
DVI-D DL/DUAL+ DP + HDMI

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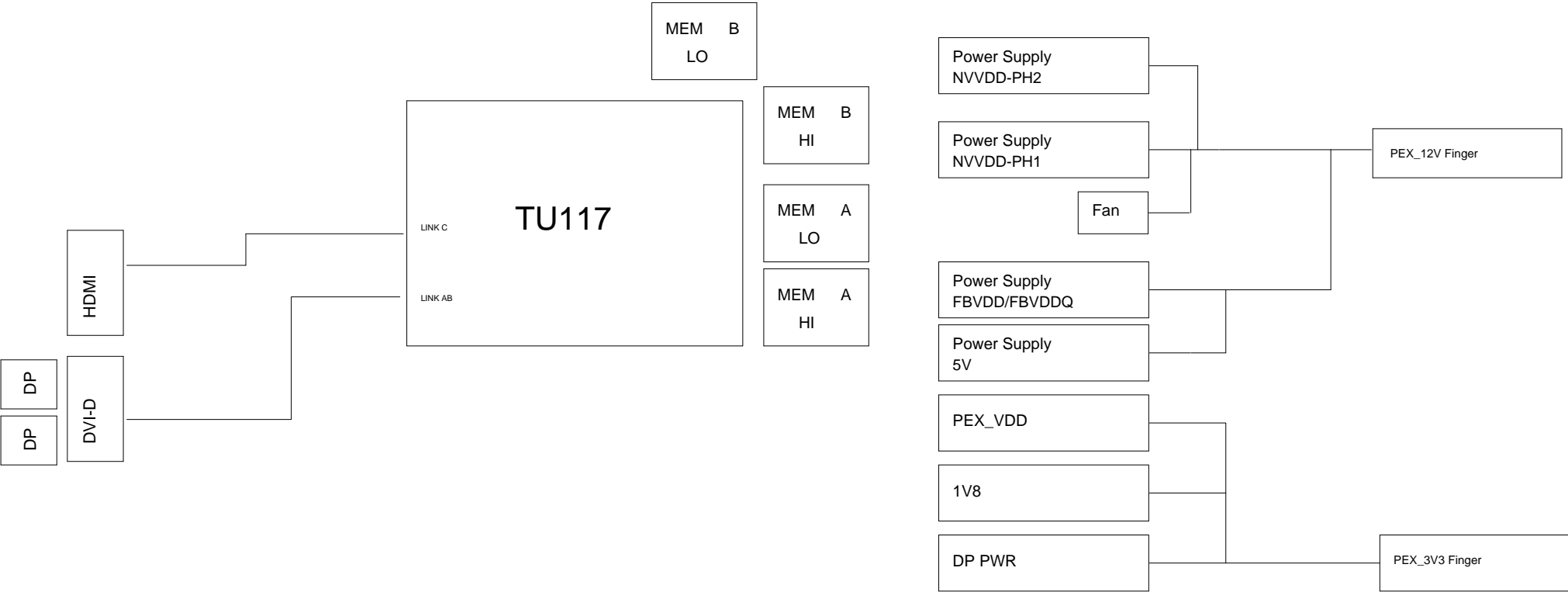
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Block Diagram

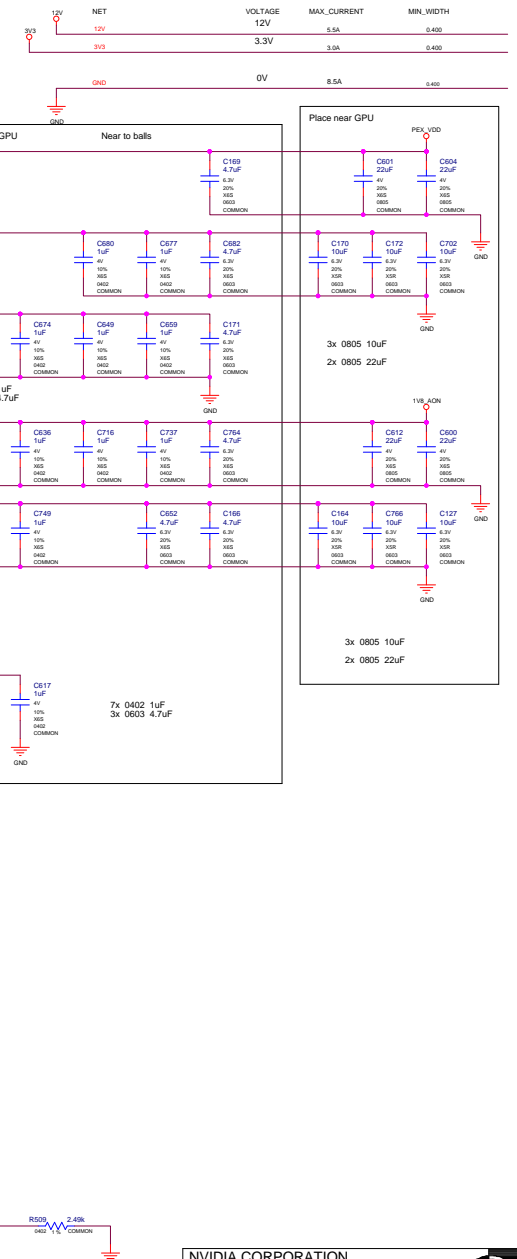


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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	Block Diagram


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NV_PN	600-1G174-BASE-A01	PAGE	2 OF 32
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PCI Express

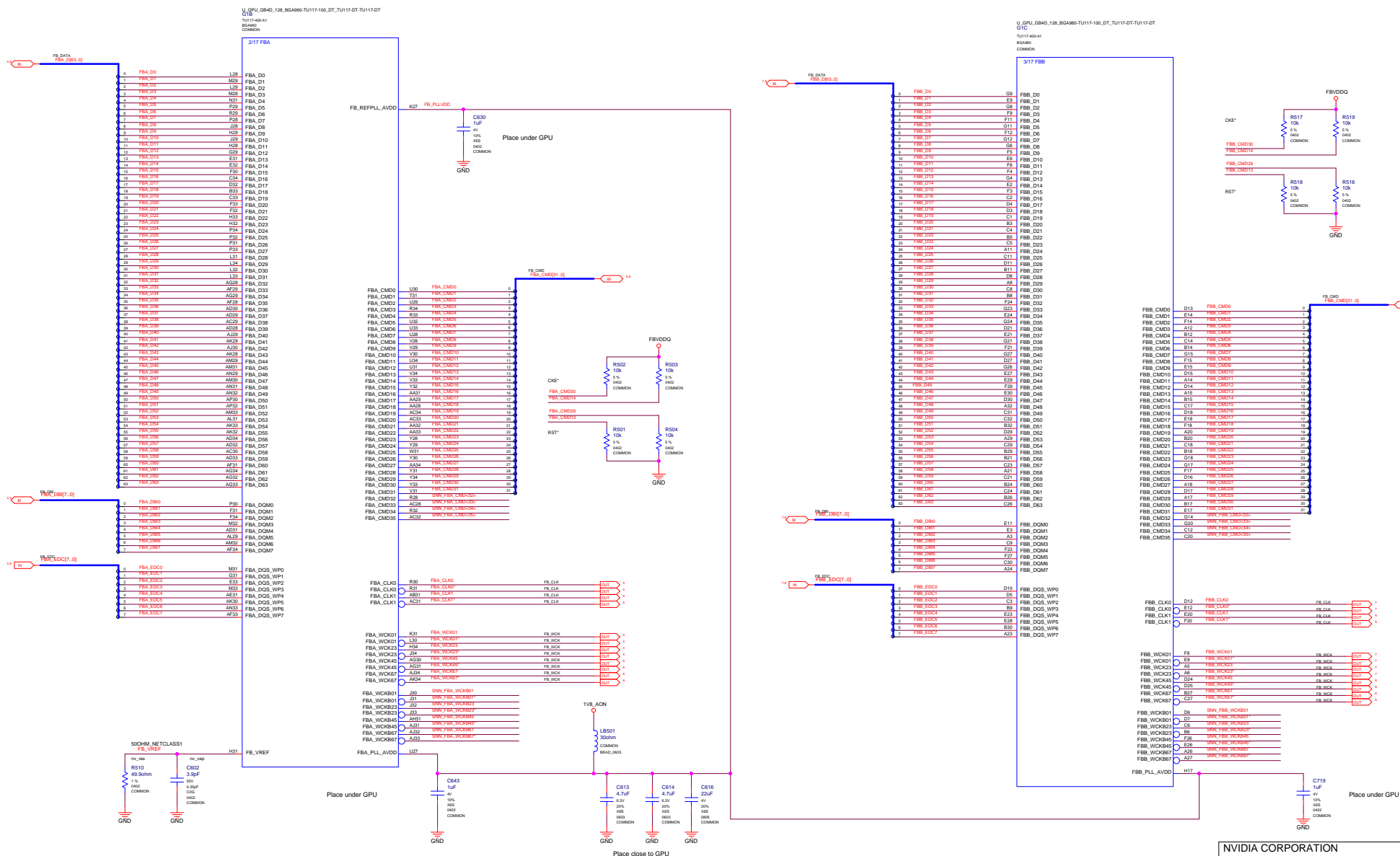


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PAGE DETAIL	PCI Express

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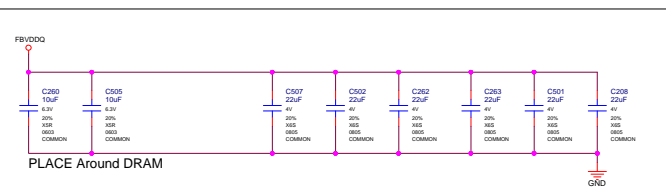
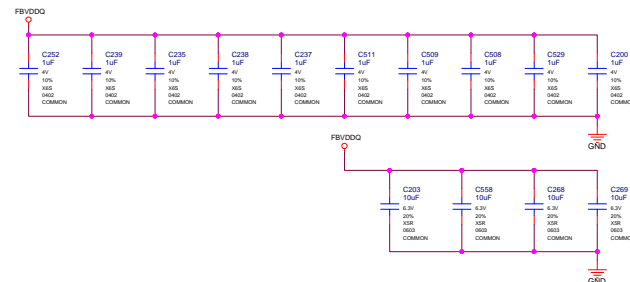
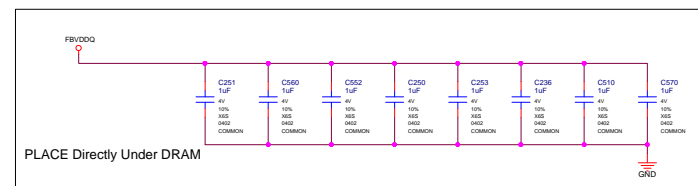
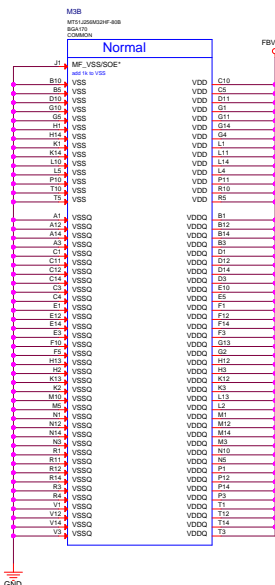
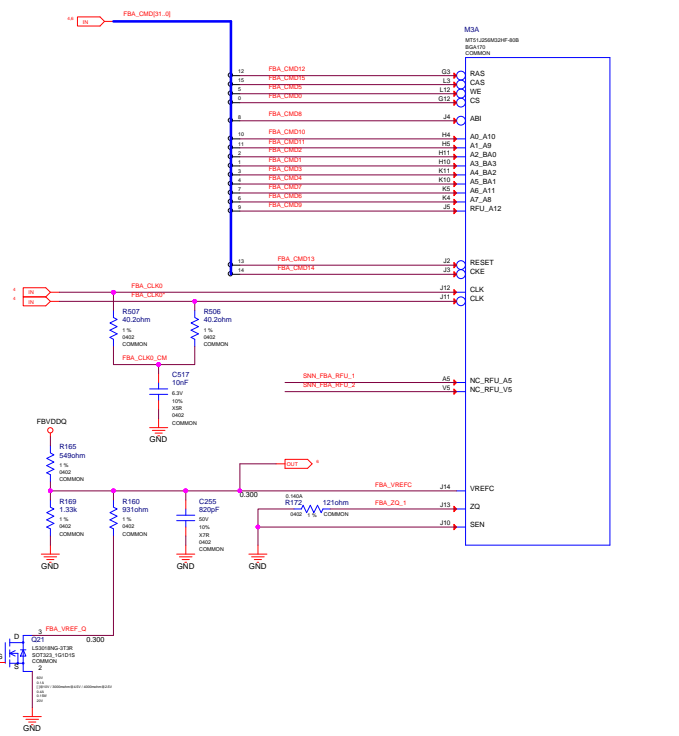
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MEMORY: GPU Partition A/B



MEMORY: FBA Partition 31..0

CMD	0.31	32.63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_AB	
CMD7	AB_A11	
CMD8	AB*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_AB	
CMD12	RAS*	
CMD13	RS1*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		AB*
CMD23		AB_A11
CMD24		A7_AB
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_AB
CMD28		RAS*
CMD29		RS1*
CMD30		CKE*
CMD31		CAS*



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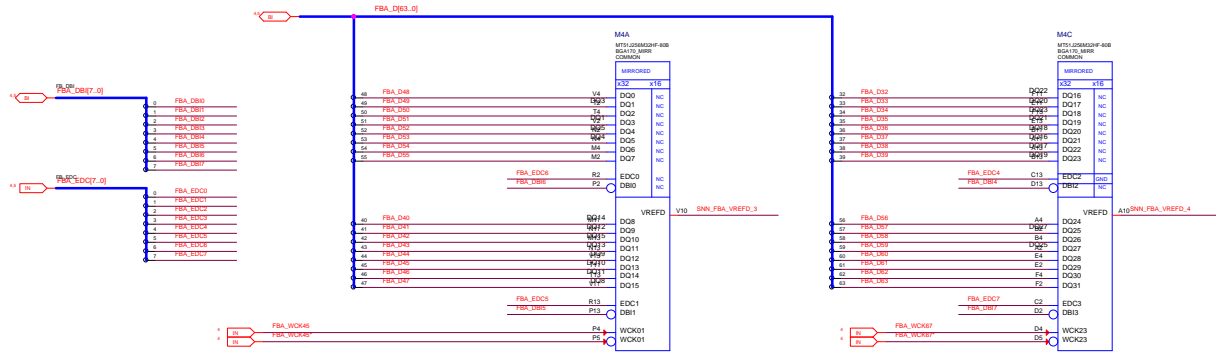
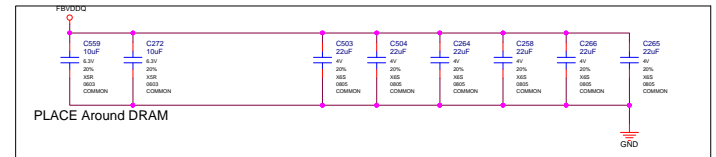
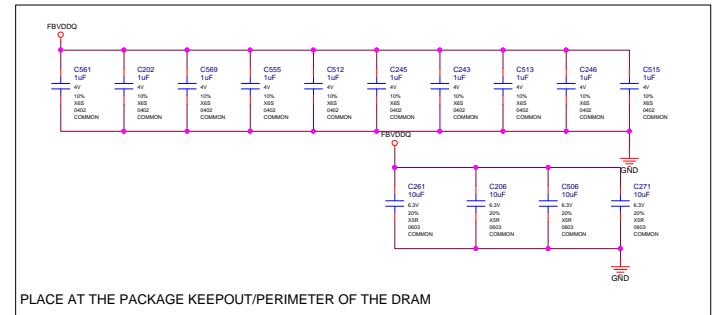
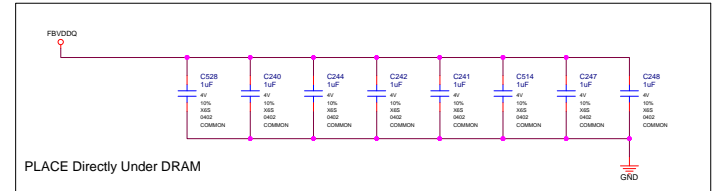
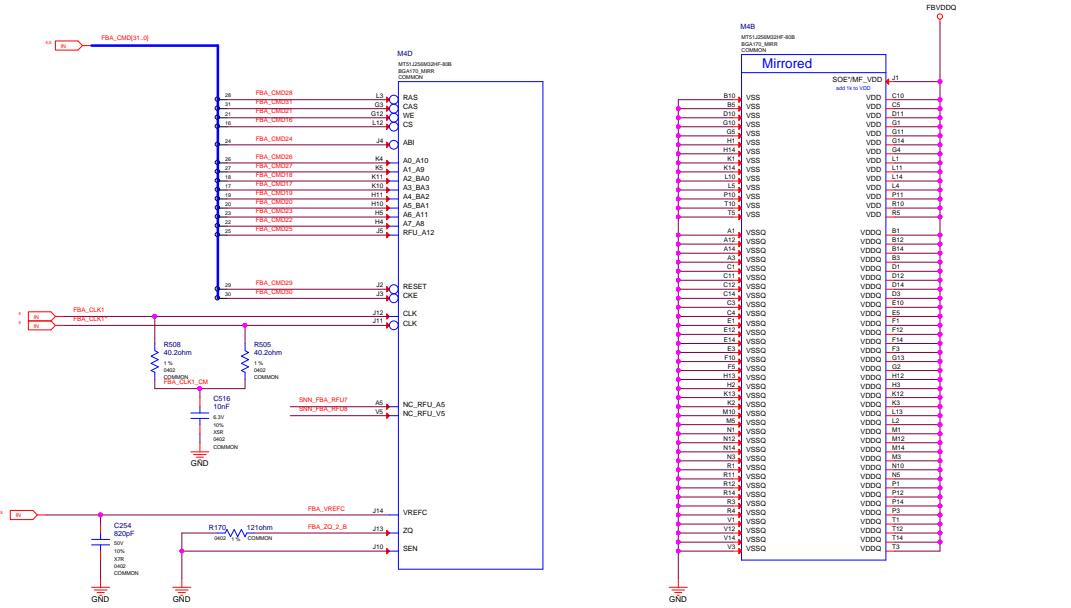
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MEMORY: FBA Partition 63..32

CMD	0..31	32..63
CMD0	C0*	
CMD1	A2..BA3	
CMD2	A2..BA0	
CMD3	A4..BA2	
CMD4	A6..BA1	
CMD5	WE*	
CMD6	A7..A8	
CMD7	AB..A11	
CMD8	AB*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A9	C0*
CMD12	RA0*	A2..BA3
CMD13	RS1*	A2..BA0
CMD14	CKE*	A4..BA2
CMD15		A6..BA1
CMD16		WE*
CMD17		A7..A8
CMD18		AB..A11
CMD19		AB*
CMD20		A12..RFU
CMD21		A0..A10
CMD22		A1..A9
CMD23		RA0*
CMD24		RS1*
CMD25		CKE*
CMD26		CAS*
CMD27		
CMD28		
CMD29		
CMD30		
CMD31		



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ASSEMBLY
PAGE DETAIL
MEMORY: FBA(63..32)

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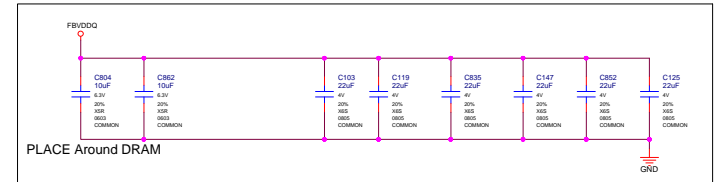
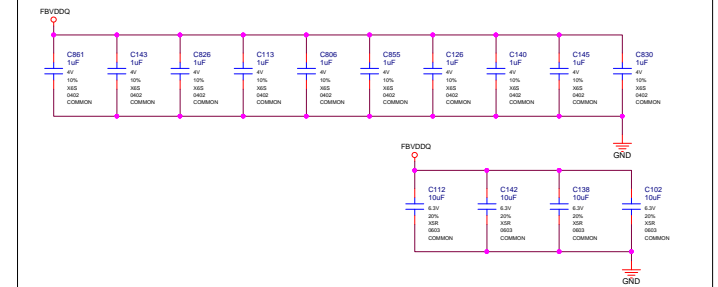
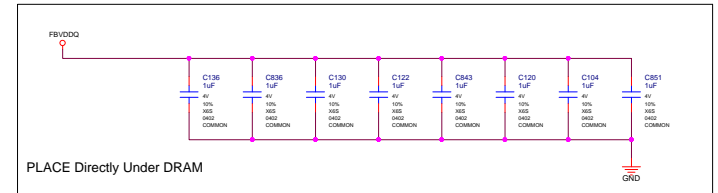
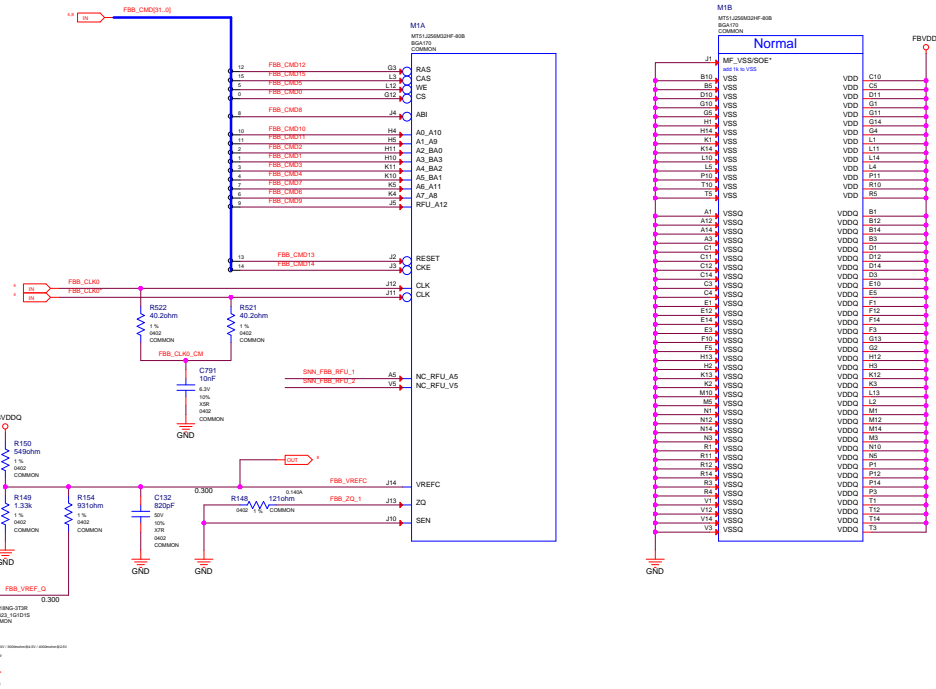
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MEMORY: FBB Partition 31..0

CMD	0.31	32.63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	AB_BA1	
CMD5	WE*	
CMD6	AT_AB	
CMD7	AG_A11	
CMD8	AB*	
CMD9	A12_RFU	
CMD10	AG_A10	
CMD11	A1_AB	
CMD12	RA5*	
CMD13	RS1*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		AB_BA1
CMD21		WE*
CMD22		AT_AB
CMD23		AB_A1
CMD24		AB*
CMD25		A12_RFU
CMD26		AG_A10
CMD27		A1_AB
CMD28		RA5*
CMD29		RS1*
CMD30		CKE*
CMD31		CAS*



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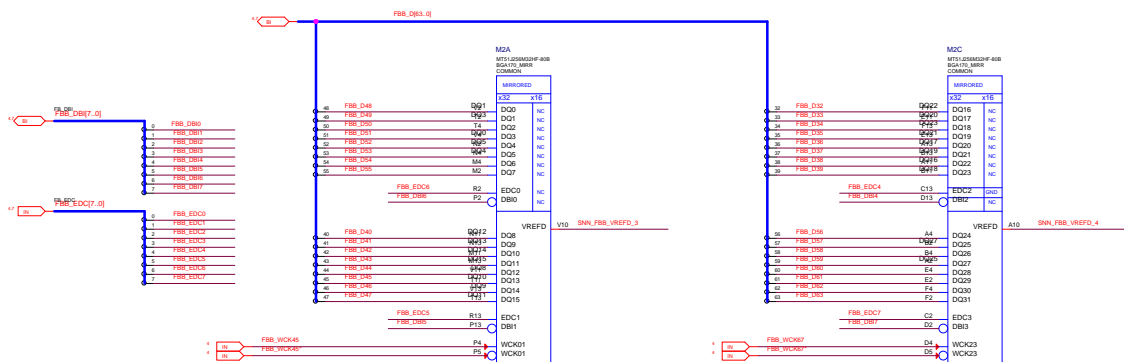
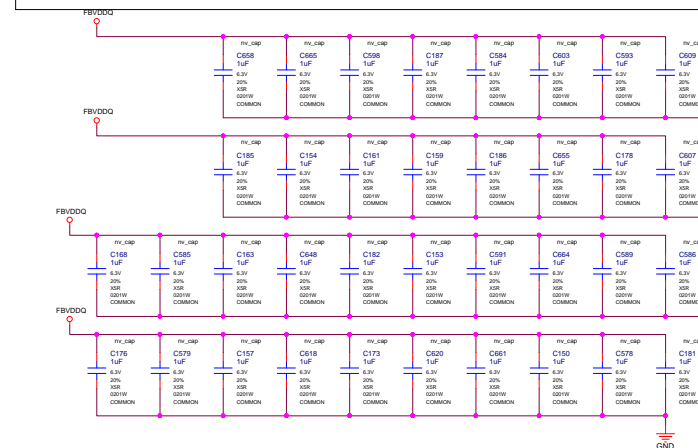
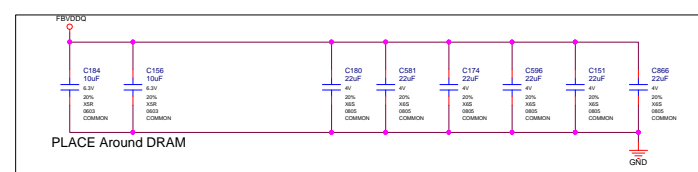
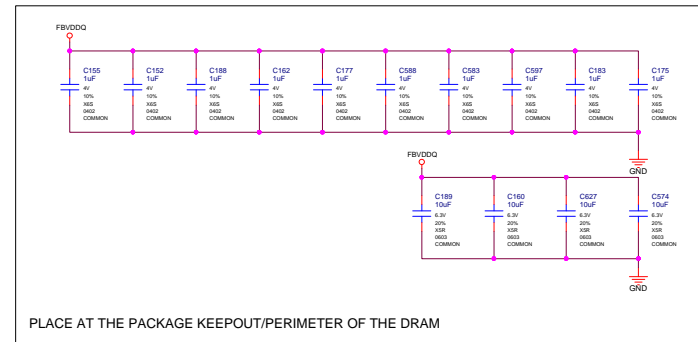
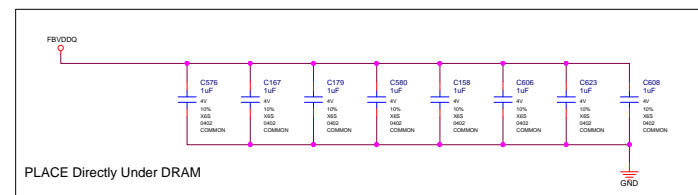
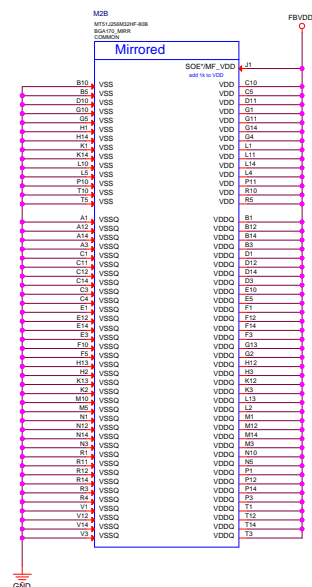
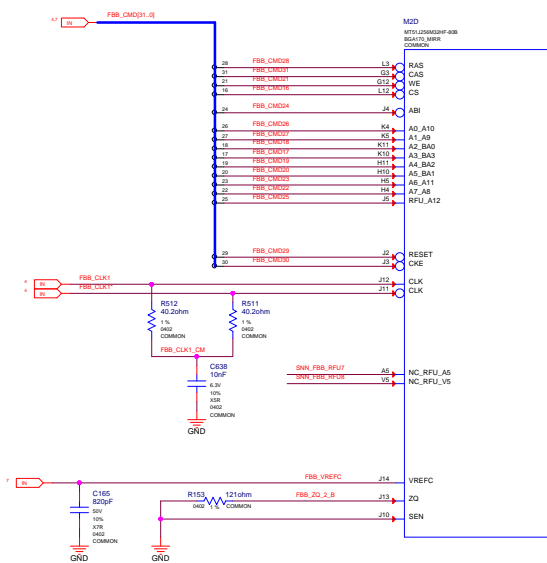
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PCB REV	PG174-A01
BOM REV	A

ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	MEMORY: FBB(31:0)

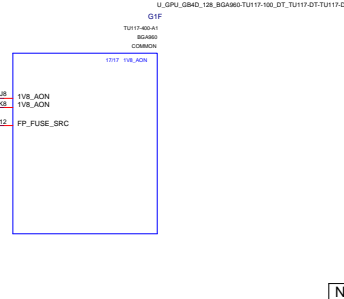
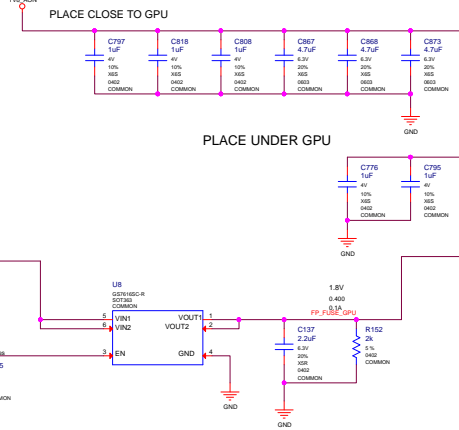
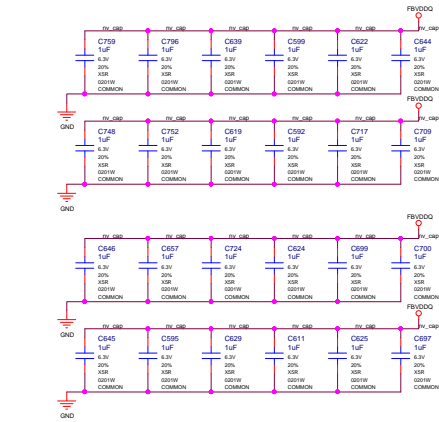
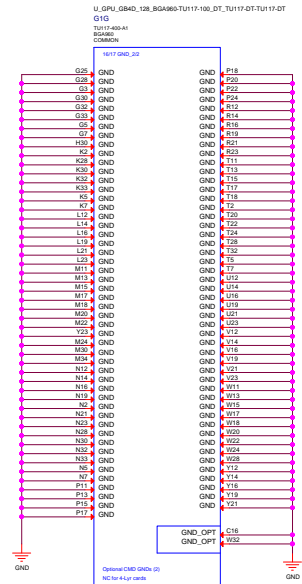
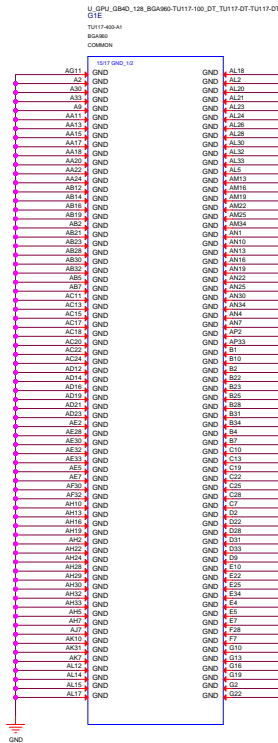
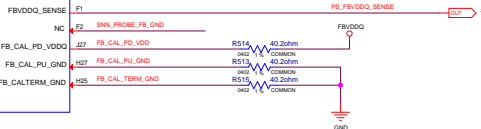
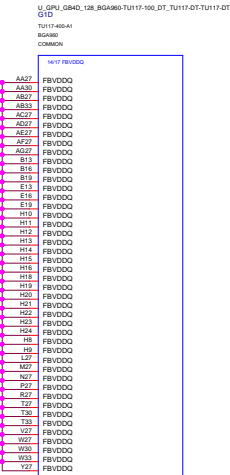
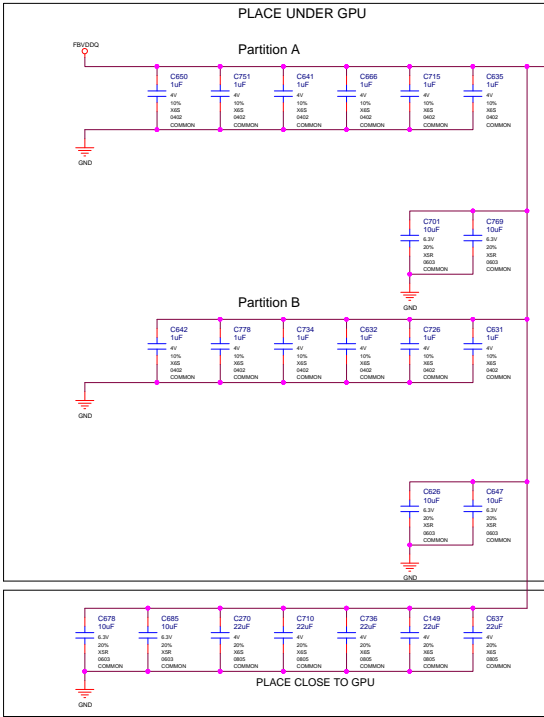
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MEMORY: FBB Partition 63..32

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3..BA3	
CMD2	A2..BA0	
CMD3	A2..BA2	
CMD4	A5..BA1	
CMD5	WE*	
CMD6	A7..A8	
CMD7	ABE..A11	
CMD8	AB*	
CMD9	A12..RFU	
CMD10	A2..A10	
CMD11	A1..A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3..BA3
CMD18		A2..BA0
CMD19		A4..BA2
CMD20		AS..BA1
CMD21		WE*
CMD22		A7..A8
CMD23		ABE..A11
CMD24		A12..RFU
CMD25		A0..A10
CMD26		A1..A9
CMD27		RAS*
CMD28		RST*
CMD29		CKE*
CMD30		CAS*
CMD31		



GPU FBVDDQ & 1V8 Decoupling



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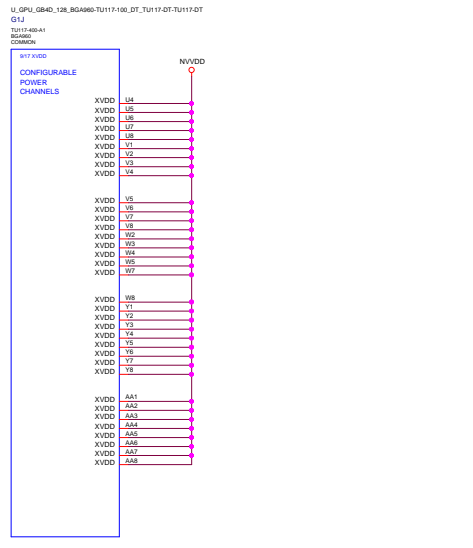
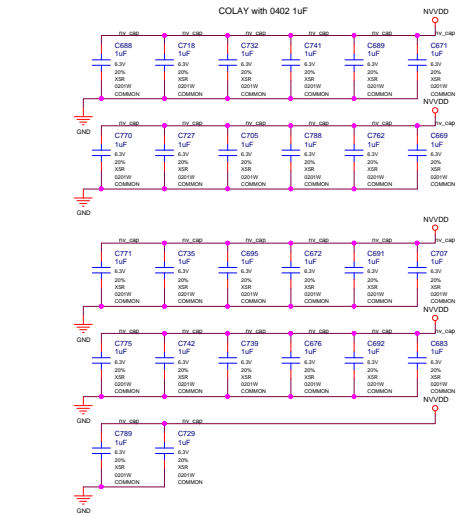
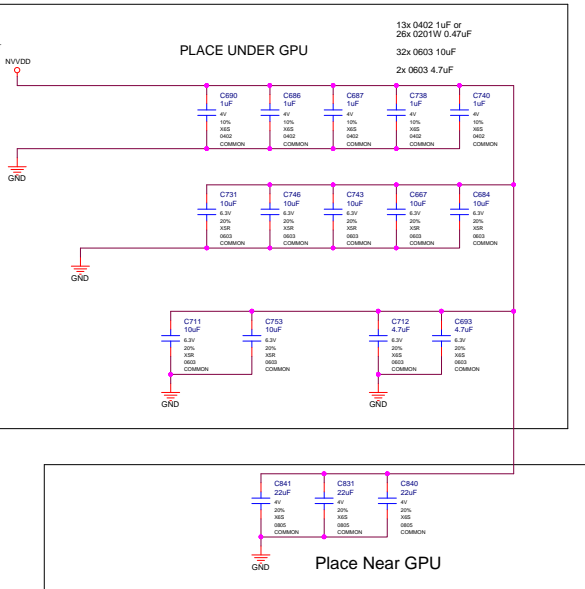
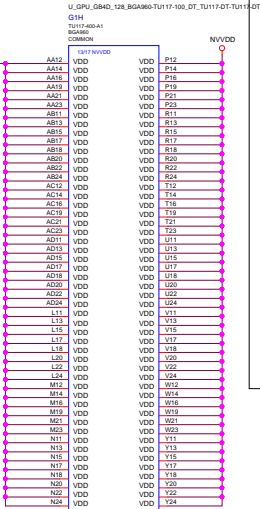
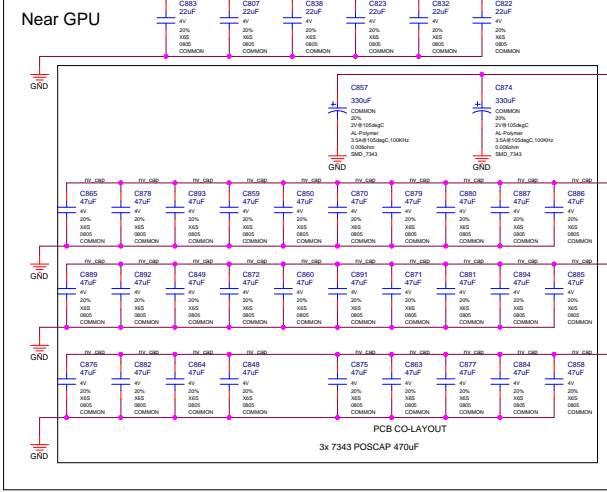
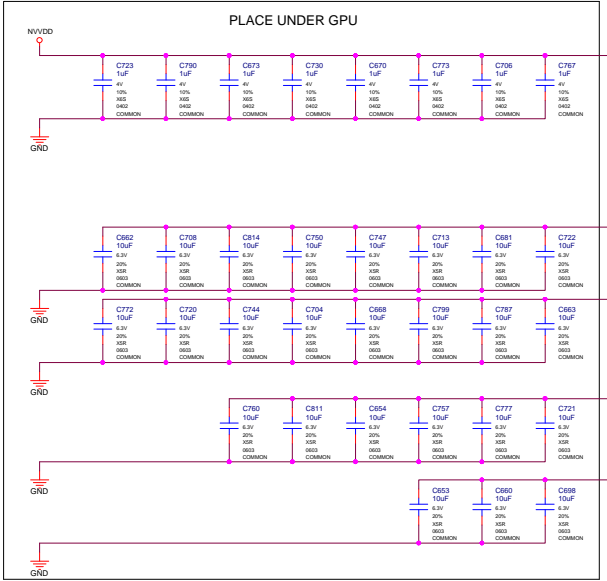
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GPU NVVDD Decoupling



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ASSEMBLY	ASSEMBLY DESCRIPTIONS
PAGE DETAIL	GPU NVVDD DECOUPLING

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PG174-A01

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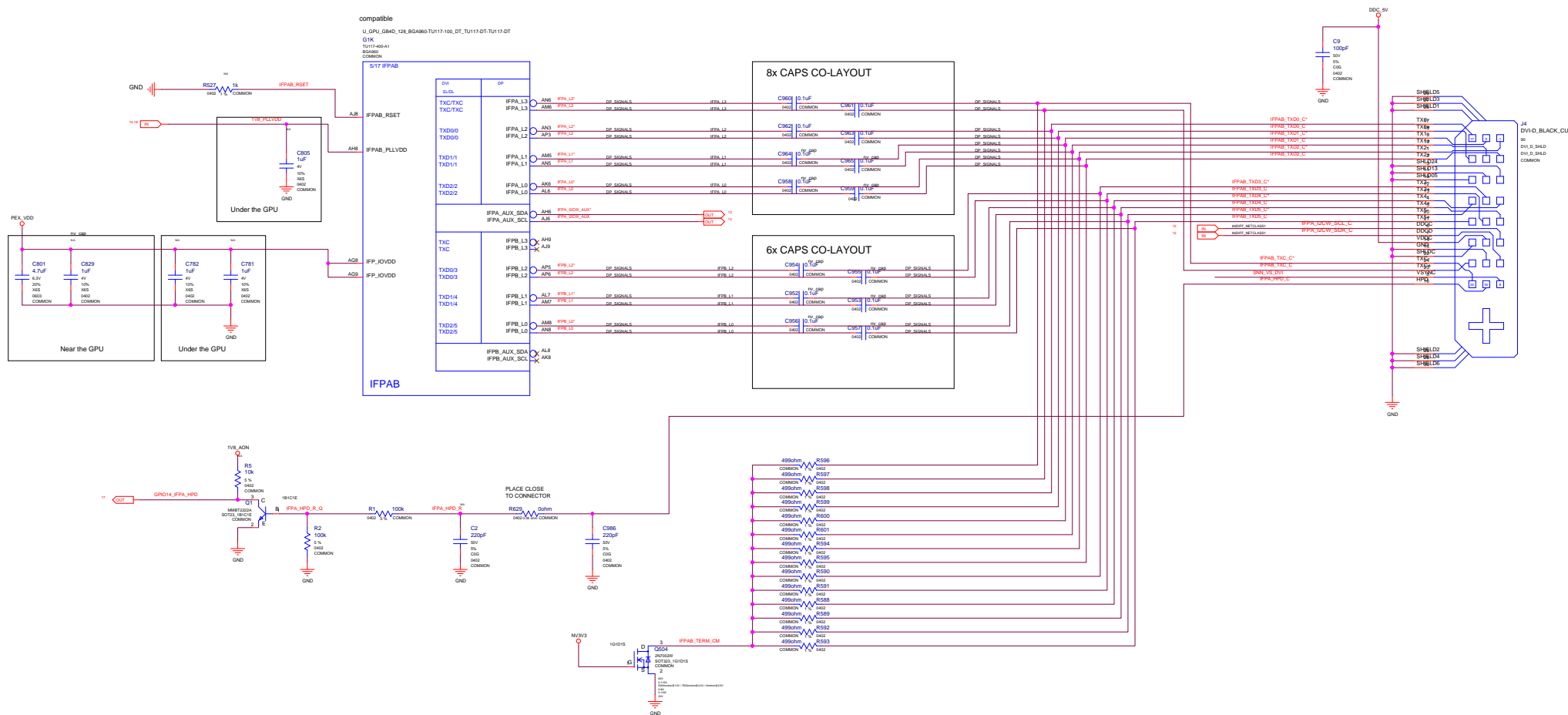
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IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



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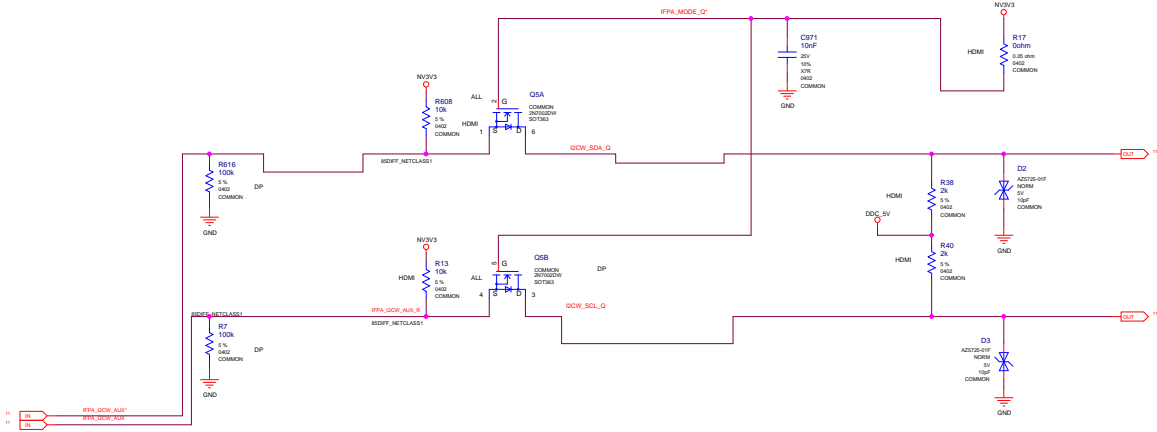
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IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

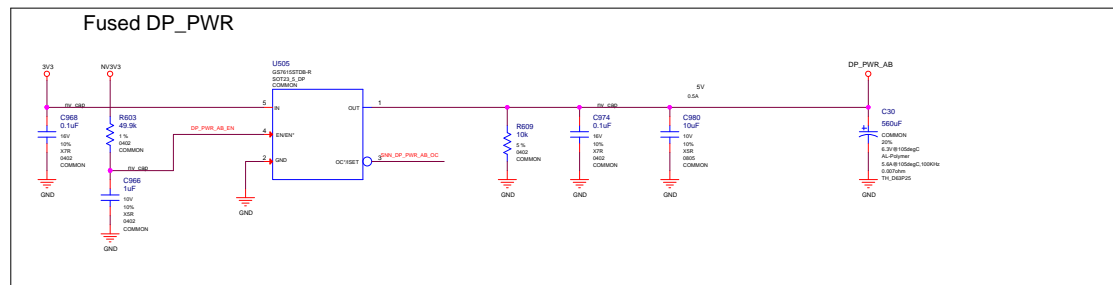
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPA DP


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NV_PN	600-1G174-BASE-A01		
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BOM REV	A	DATE	10/DEC/2018

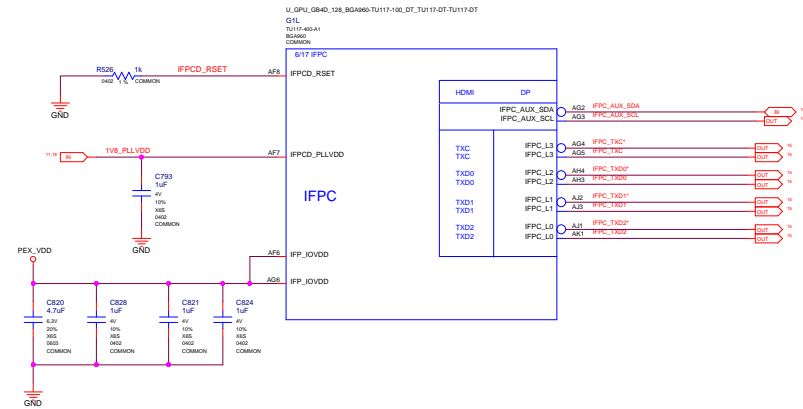
IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL DEL

Page13: IFPB DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPB DP

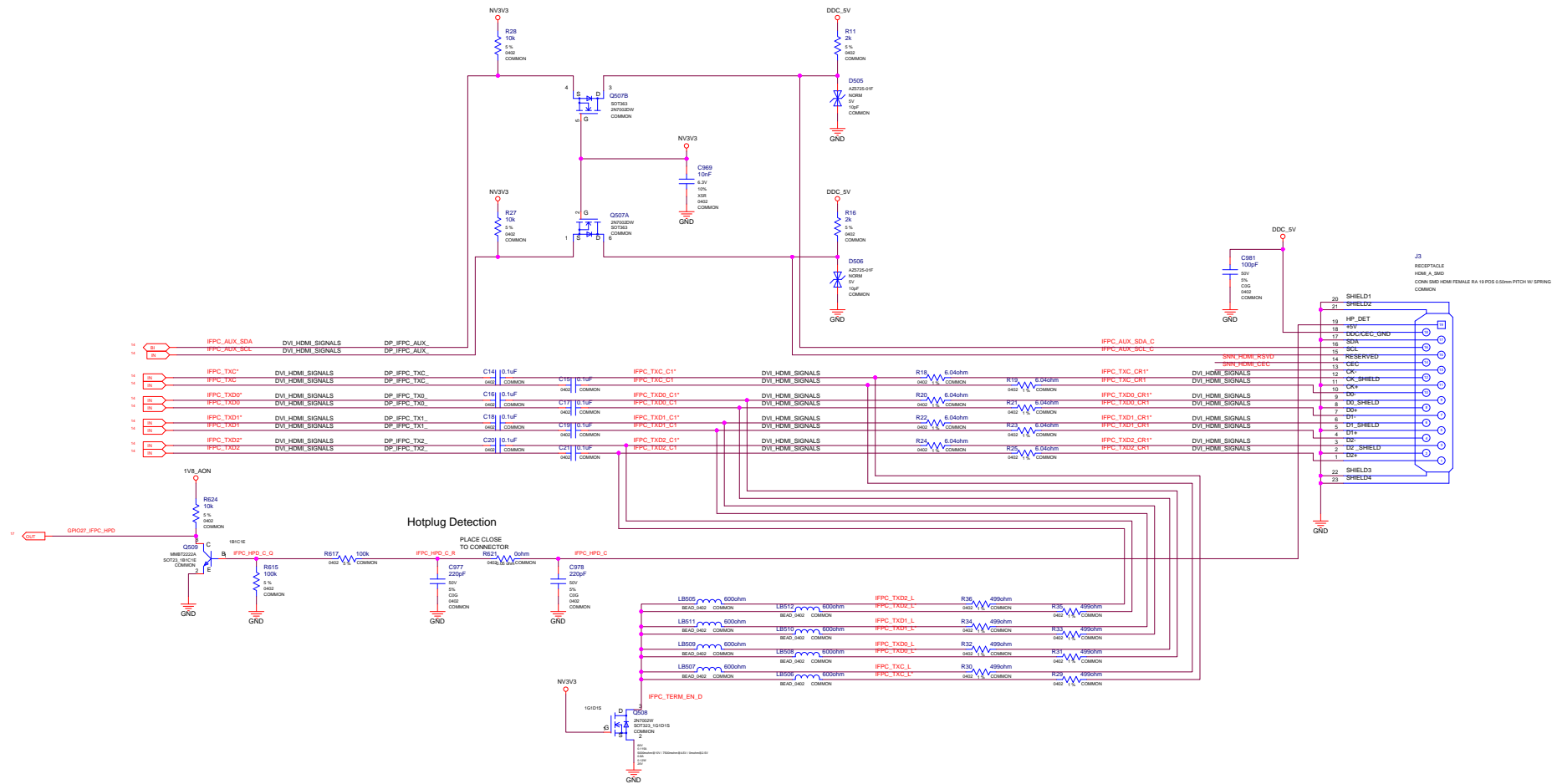
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NV_PN		600-1G174-BASE-A01		
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPC

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IFPC HDMI



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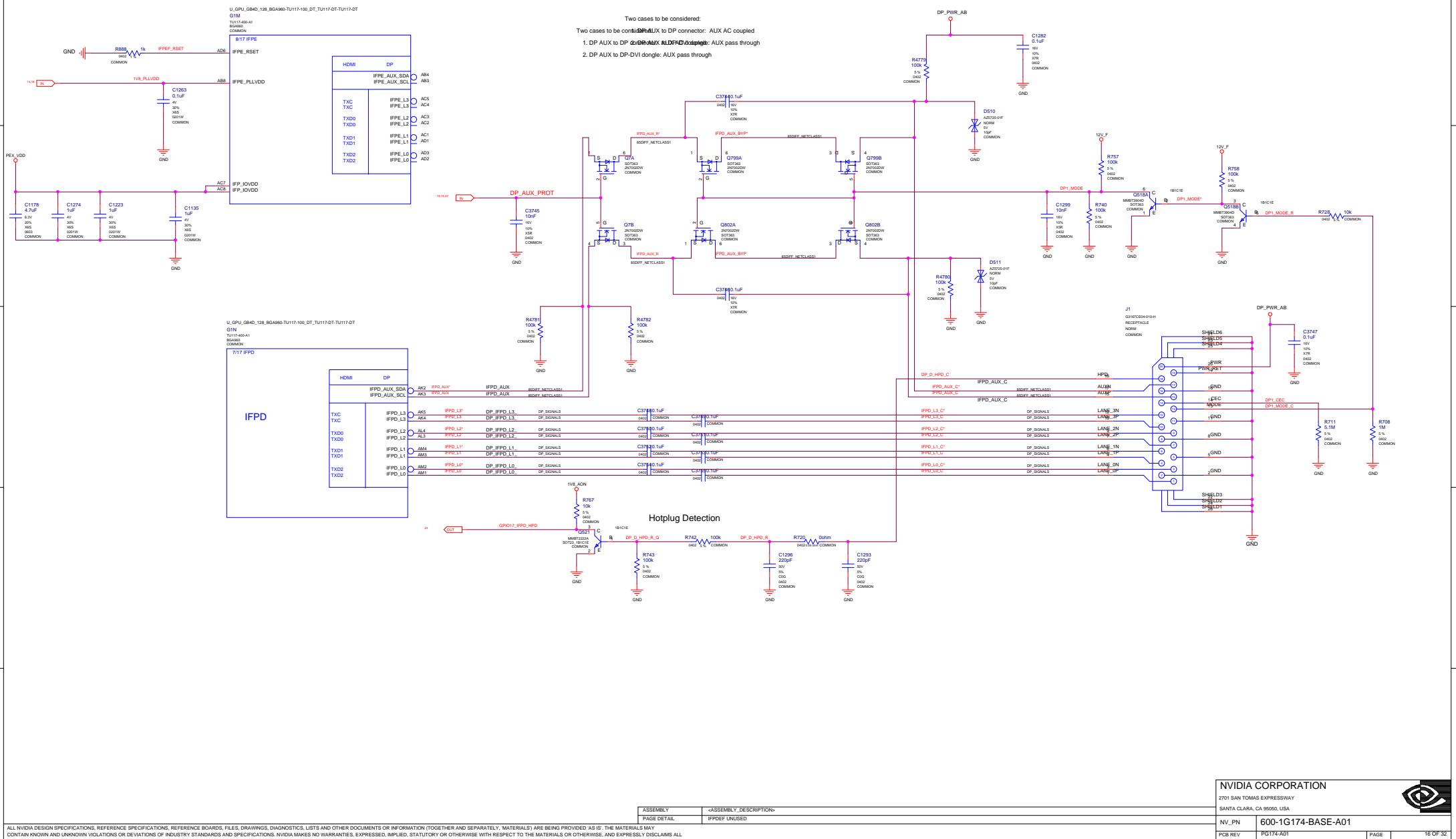


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPC HDMI

NV_PN	600-1G174-BASE-A01
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IFPDEF DP

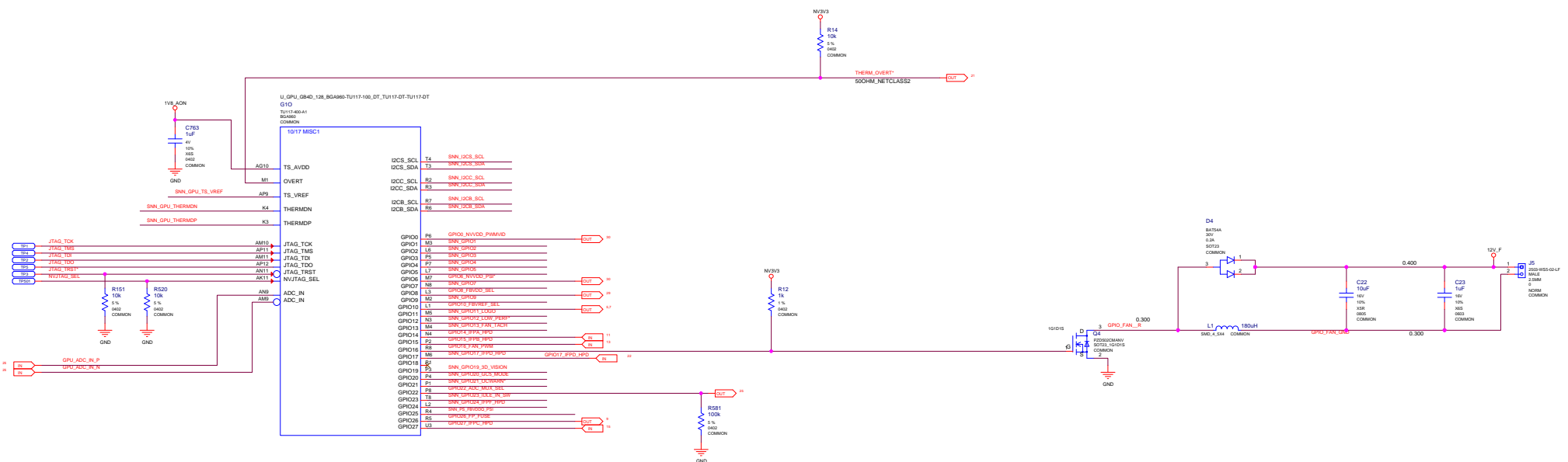


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ASSEMBLY	ASSEMBLY_DESCRIPTION
PAGE DETAIL	IFPDEF UNUSED

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
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MISC1: GPIO, Fan, Thermal, JTAG



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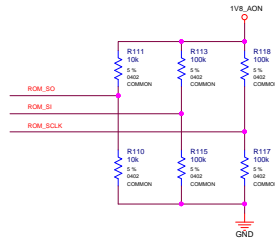
NV_PN	600-1G174-BASE-A01
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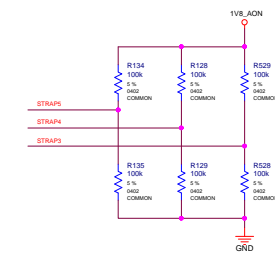
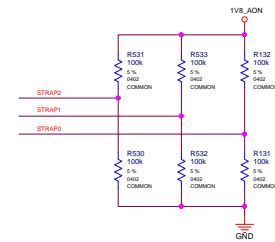
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MISC2: ROM, XTAL, Straps

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	xxx1	FS_OVERT ENABLE	Default
L	L	M	xxx0	FS_OVERT DISABLE	



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

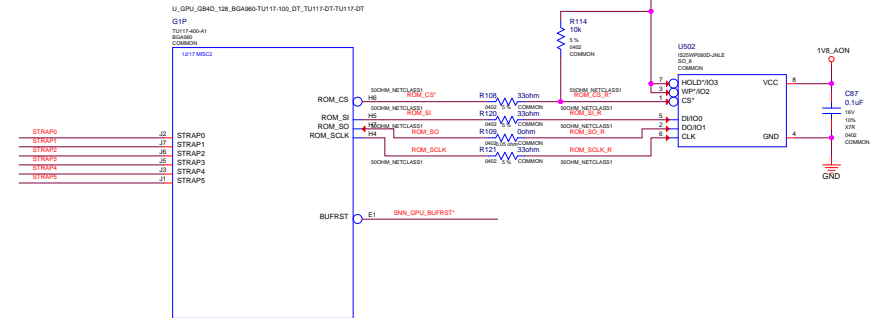


```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

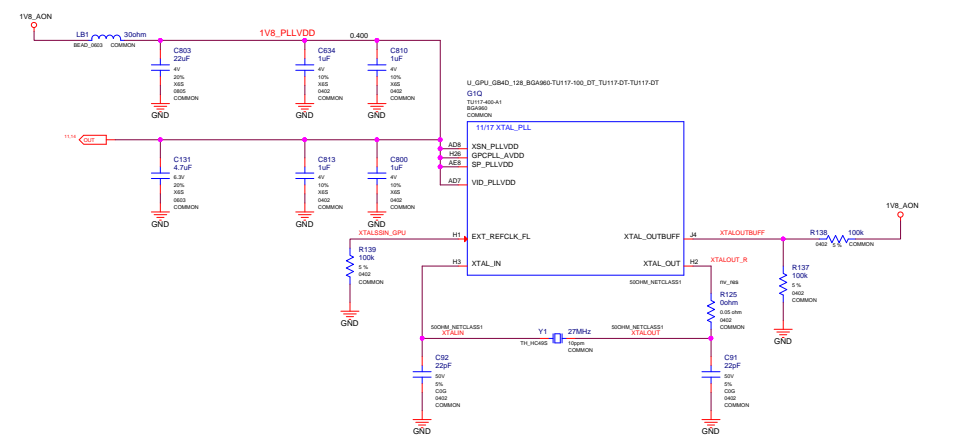
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```



Smart Fan

XTALOUTBUFF	Voltage	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	MISC2: ROM, XTAL, Straps

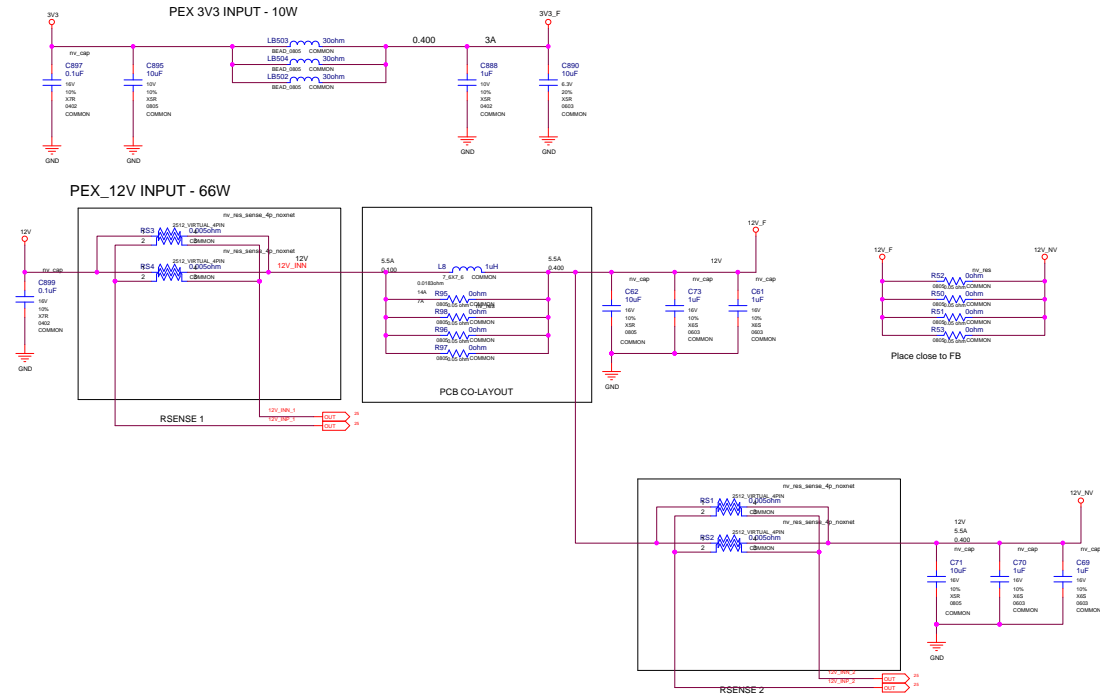
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Power Inputs and Filtering



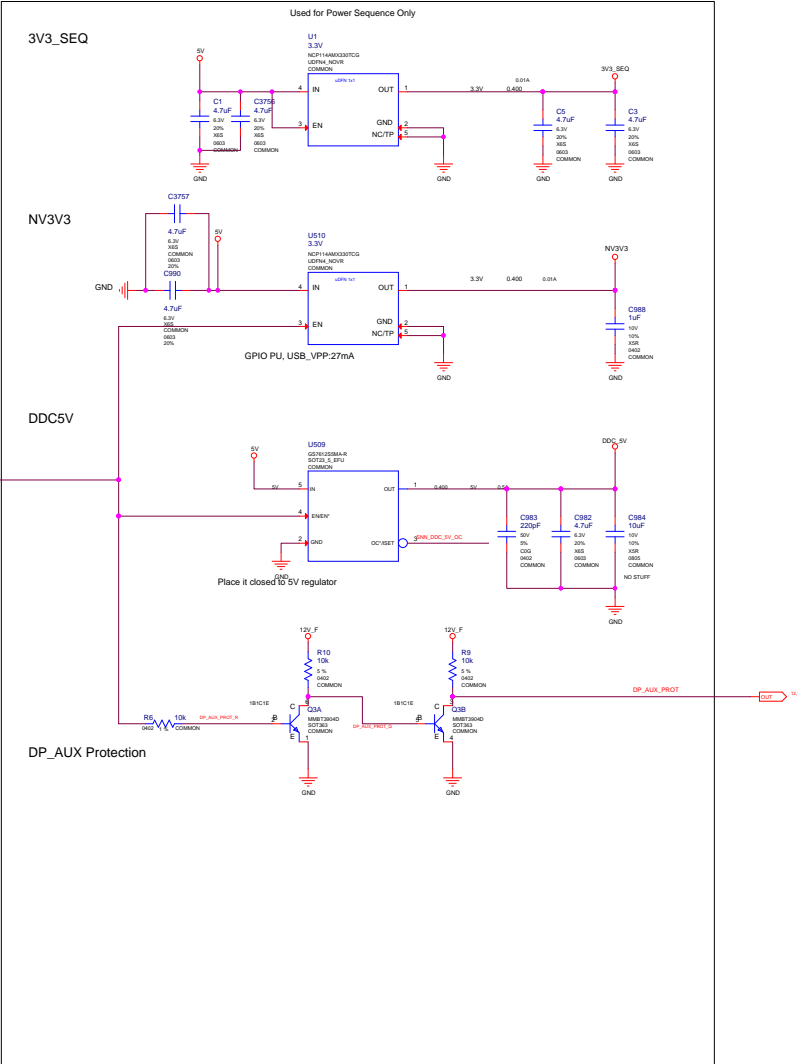
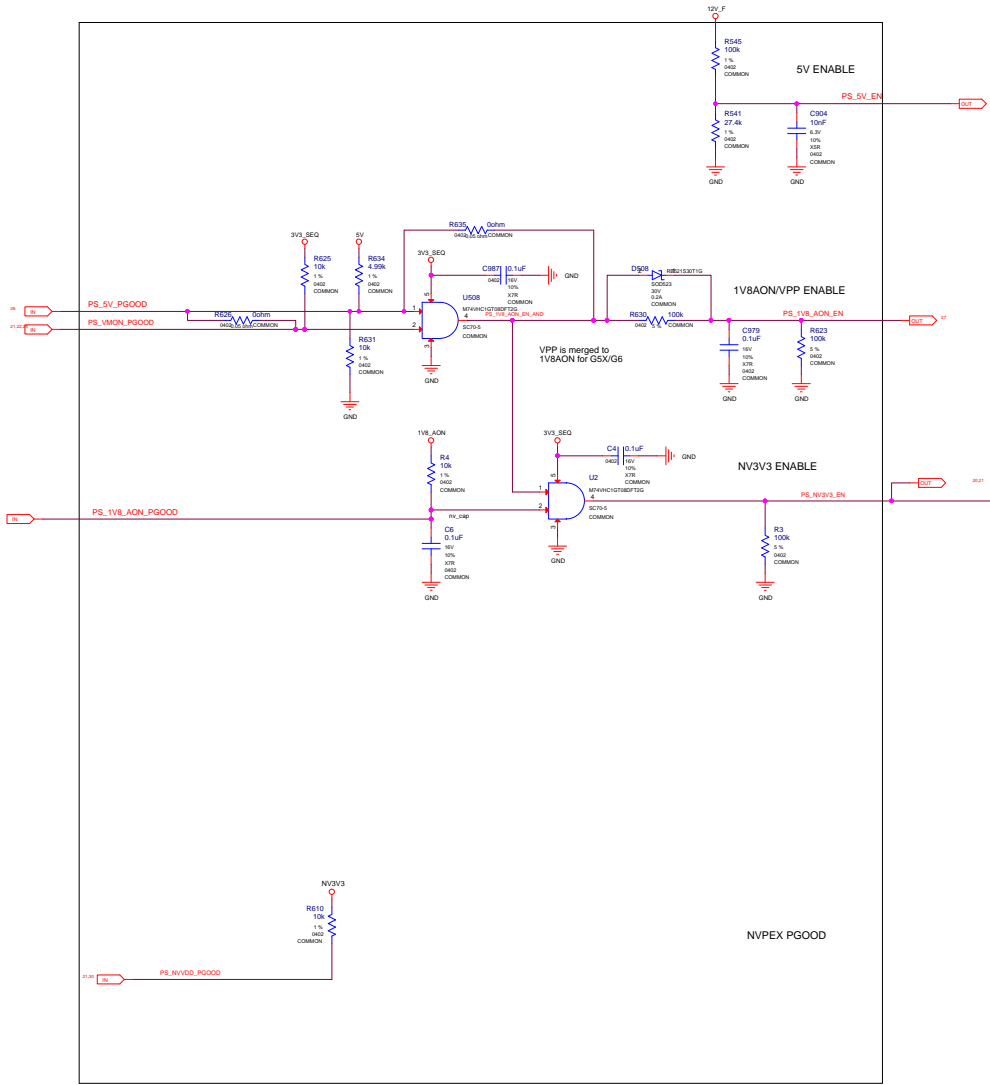
ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	Power Inputs and Filtering

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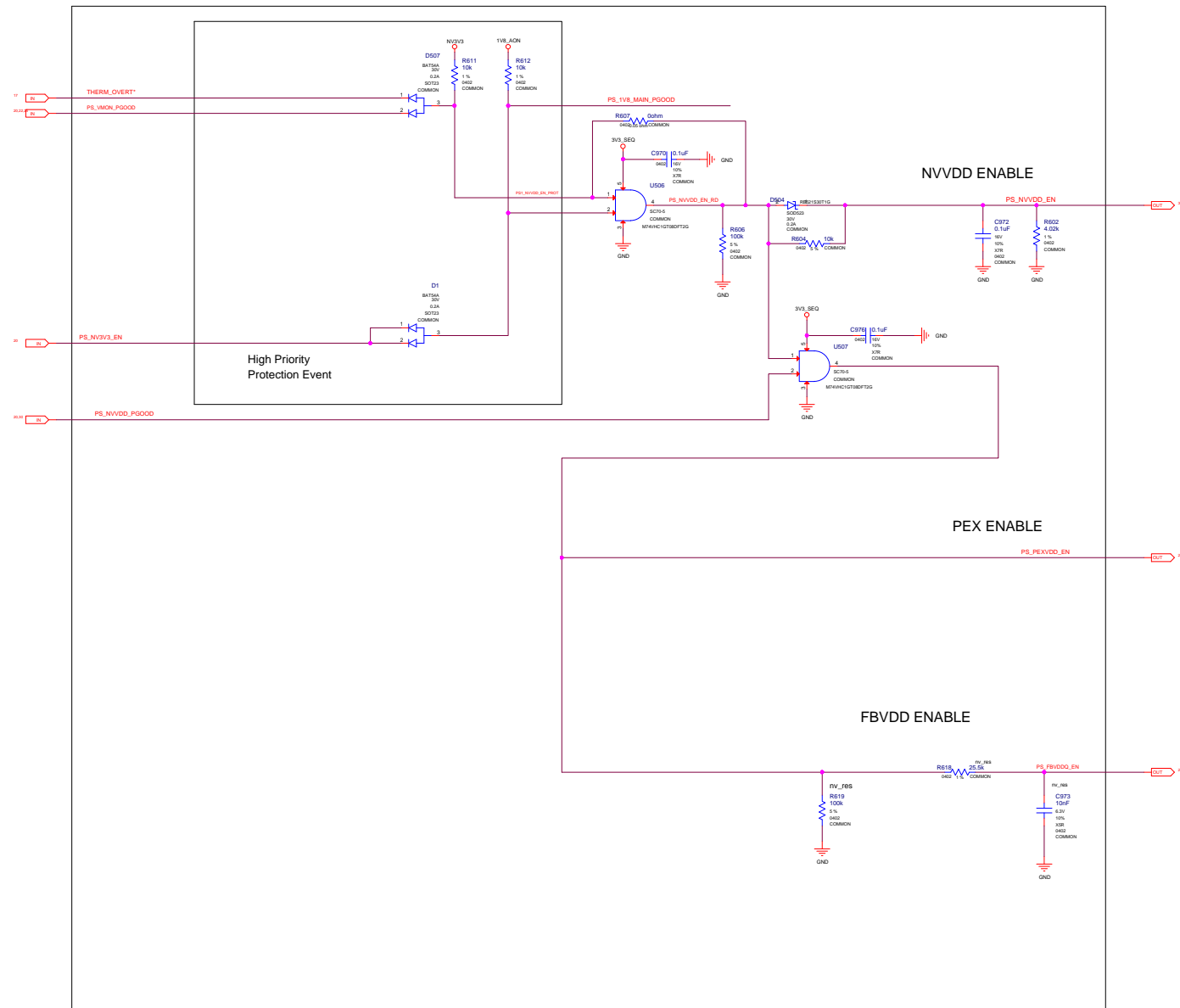
NV_PN	600-1G174-BASE-A01		
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SEQ:5V,1V8,NV3V3 ENABLE



SEQ:NV,PEX,FB ENABLE



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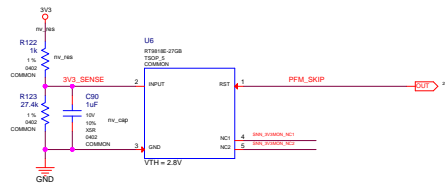
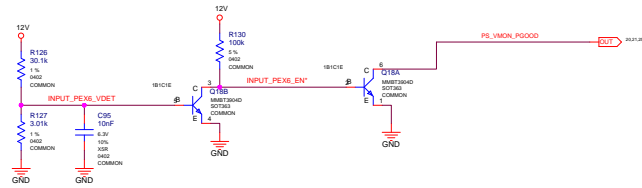


NV_PN	600-1G174-BASE-A01
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SEQUENCE:Voltage Monitor



Route the trace to PEX Golden Finger

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: VOLTAGE MONITOR

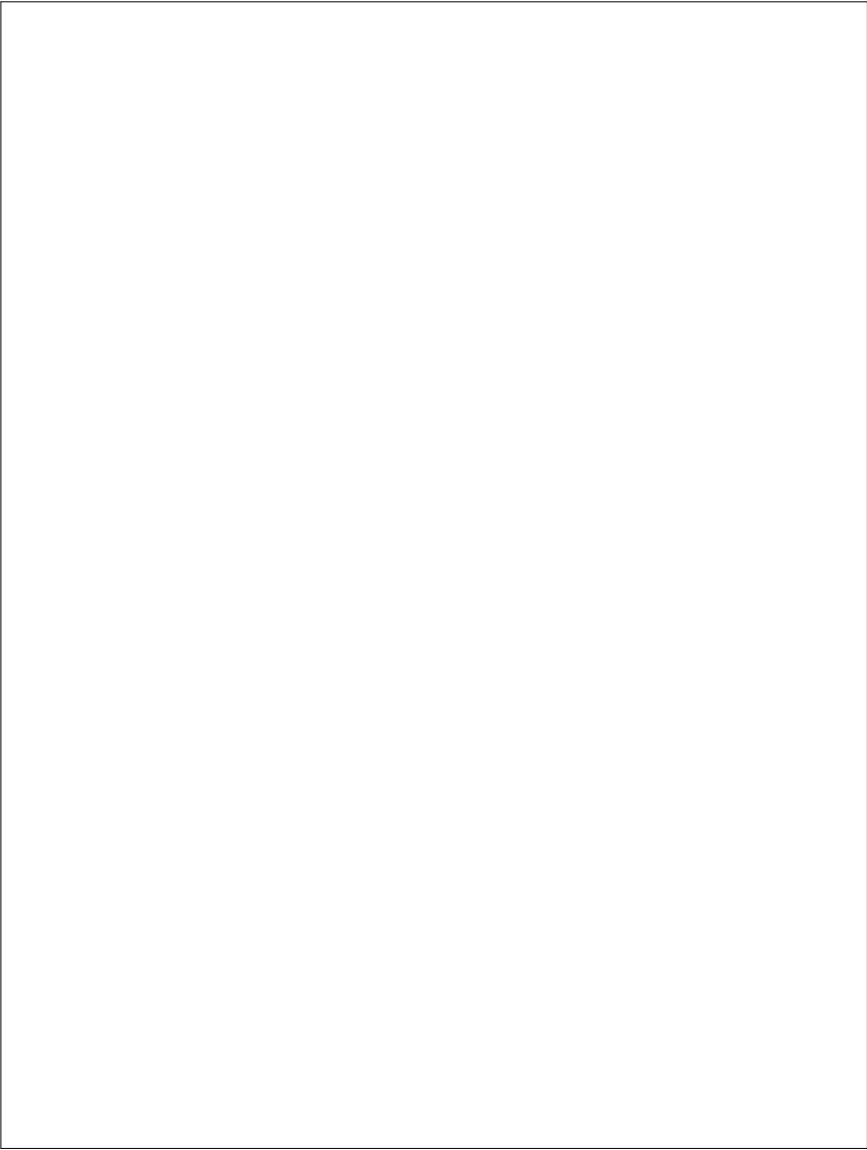
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SEQUENCE:Discharge



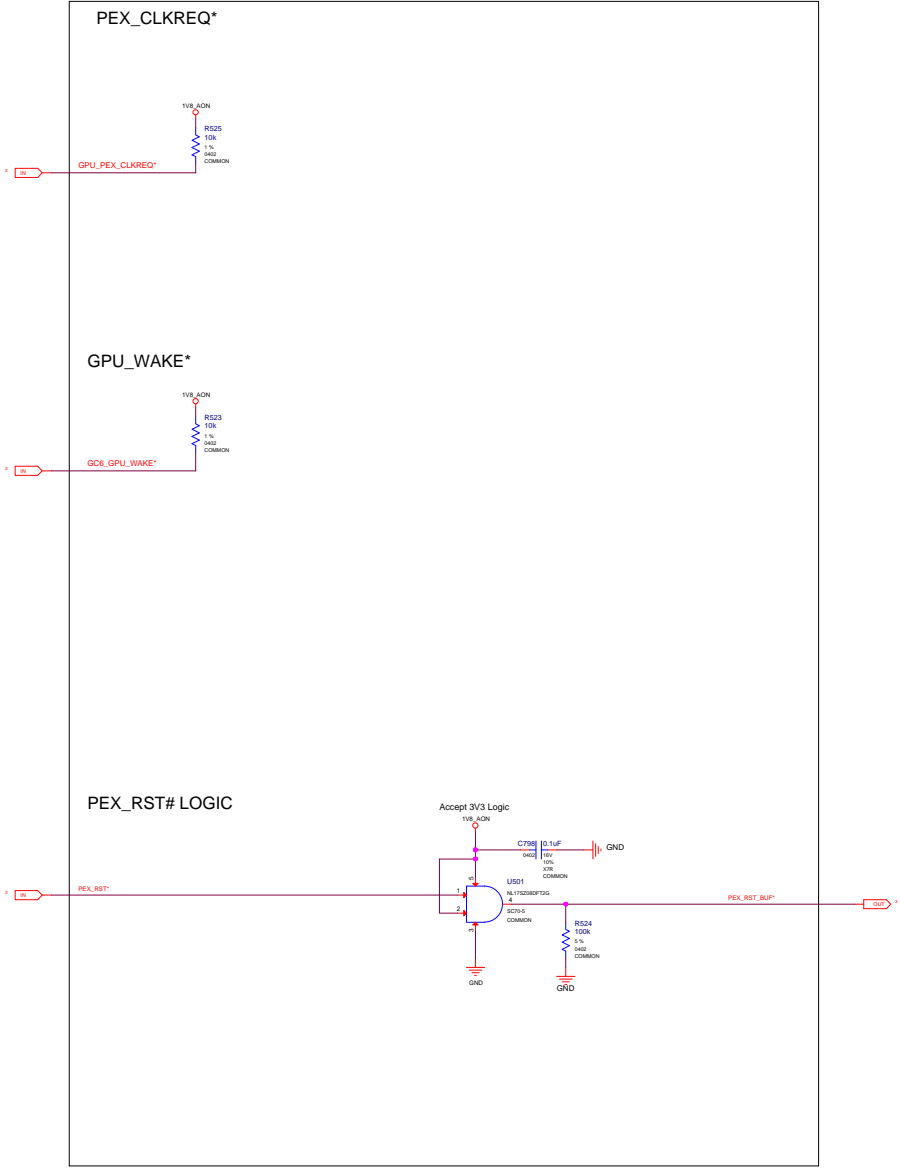
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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	SEQ: DISCHARGE

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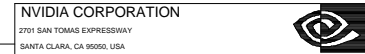


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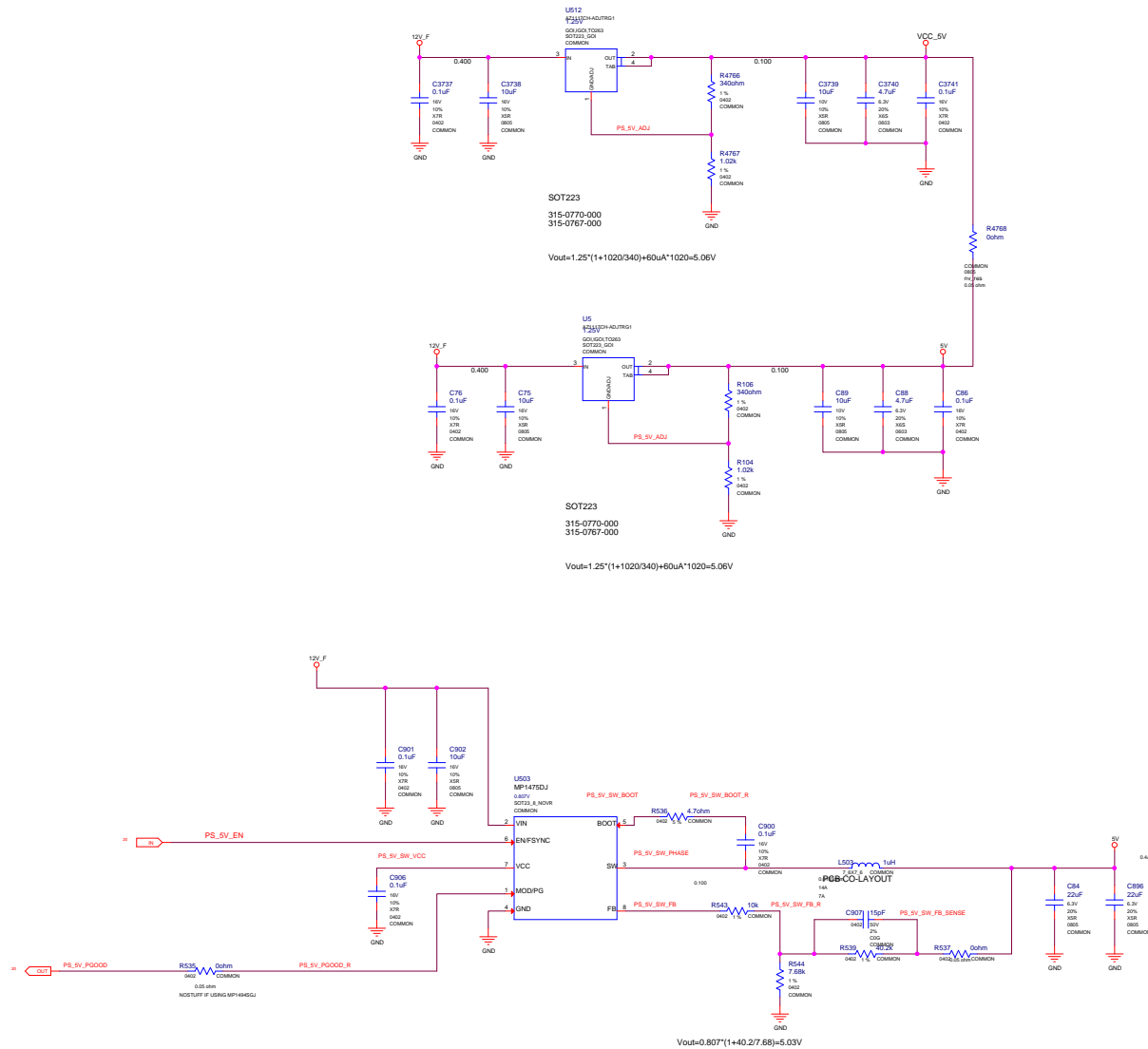
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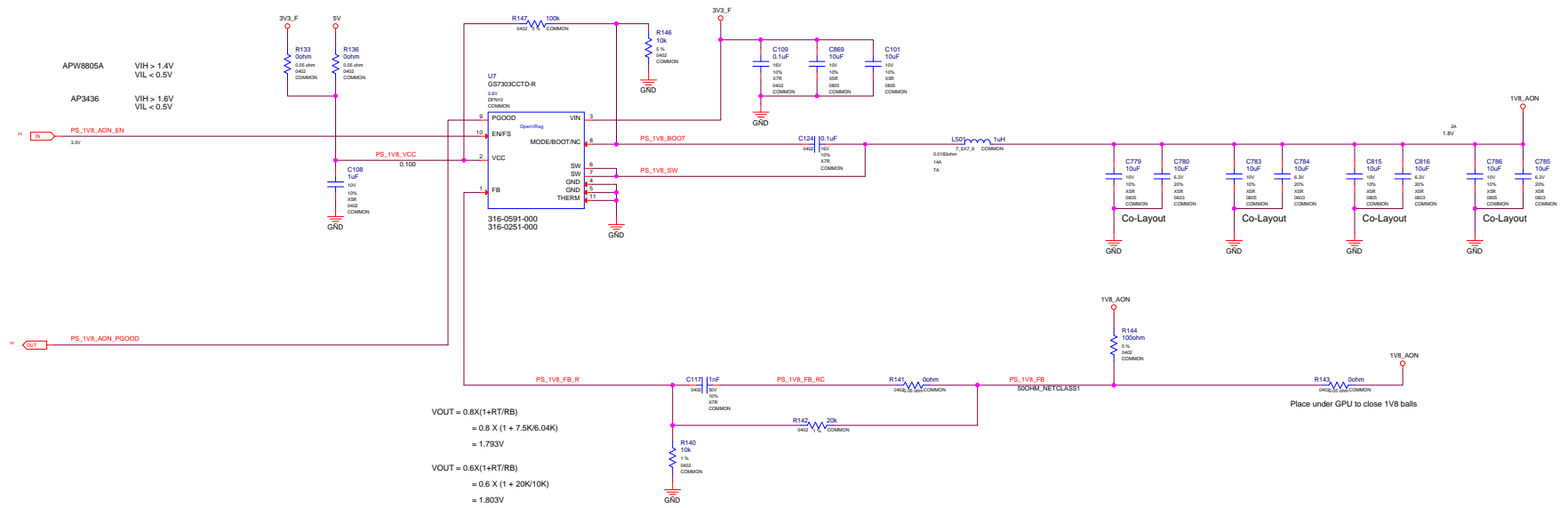
ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

NV_PN	600-1G174-BASE-A01		
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PS: 5V



PS: 1V8



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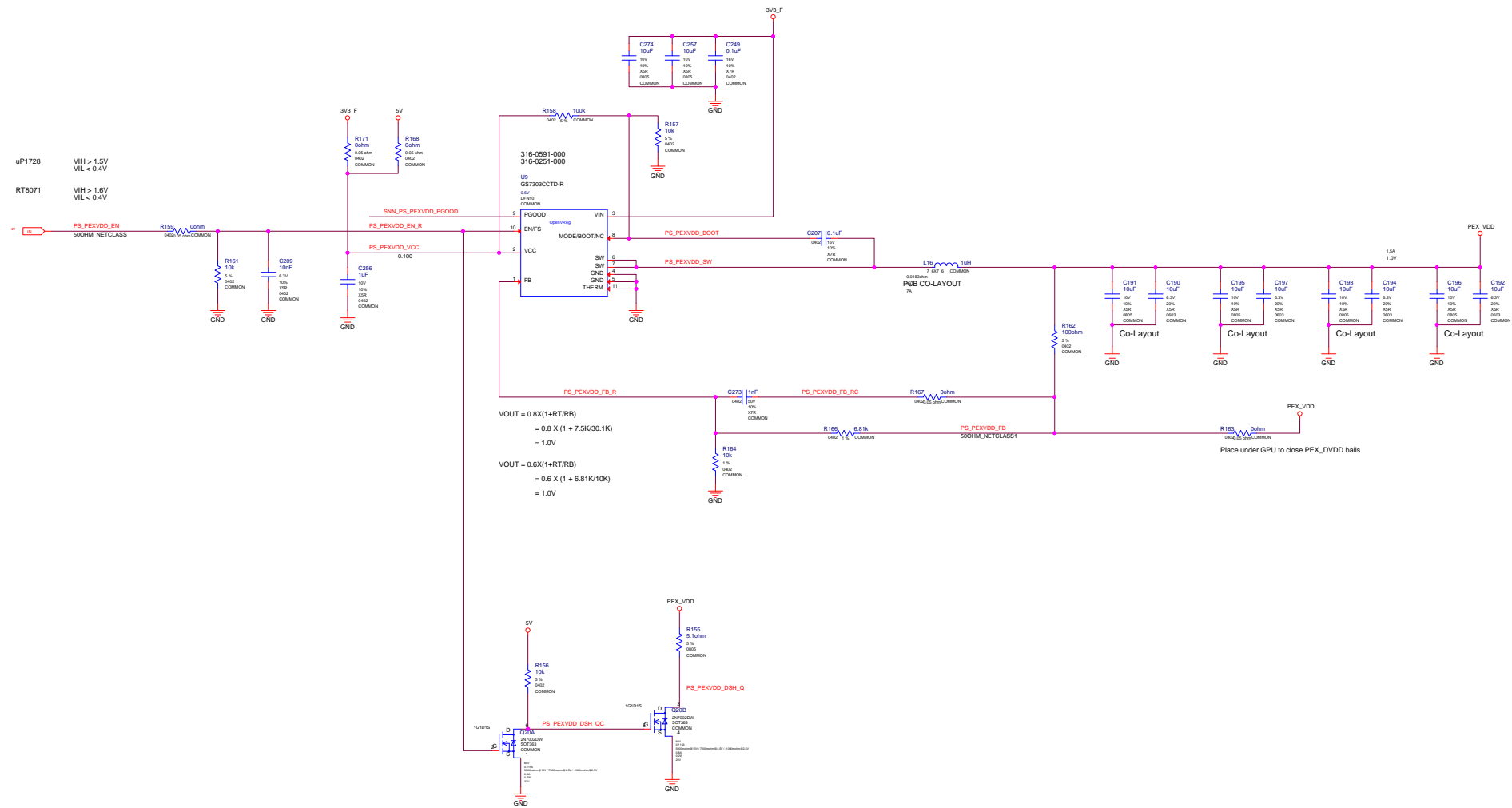
NV_PN	600-1G174-BASE-A01
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PS: PEXVDD



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS_FBVDQ

Val = Vref * (1 + R5R5)
Vref = 1.05V ± 0.0V * (1 + 1.5655)
Vref = 1.05V ± 0.0V * (1 + 1.5633)

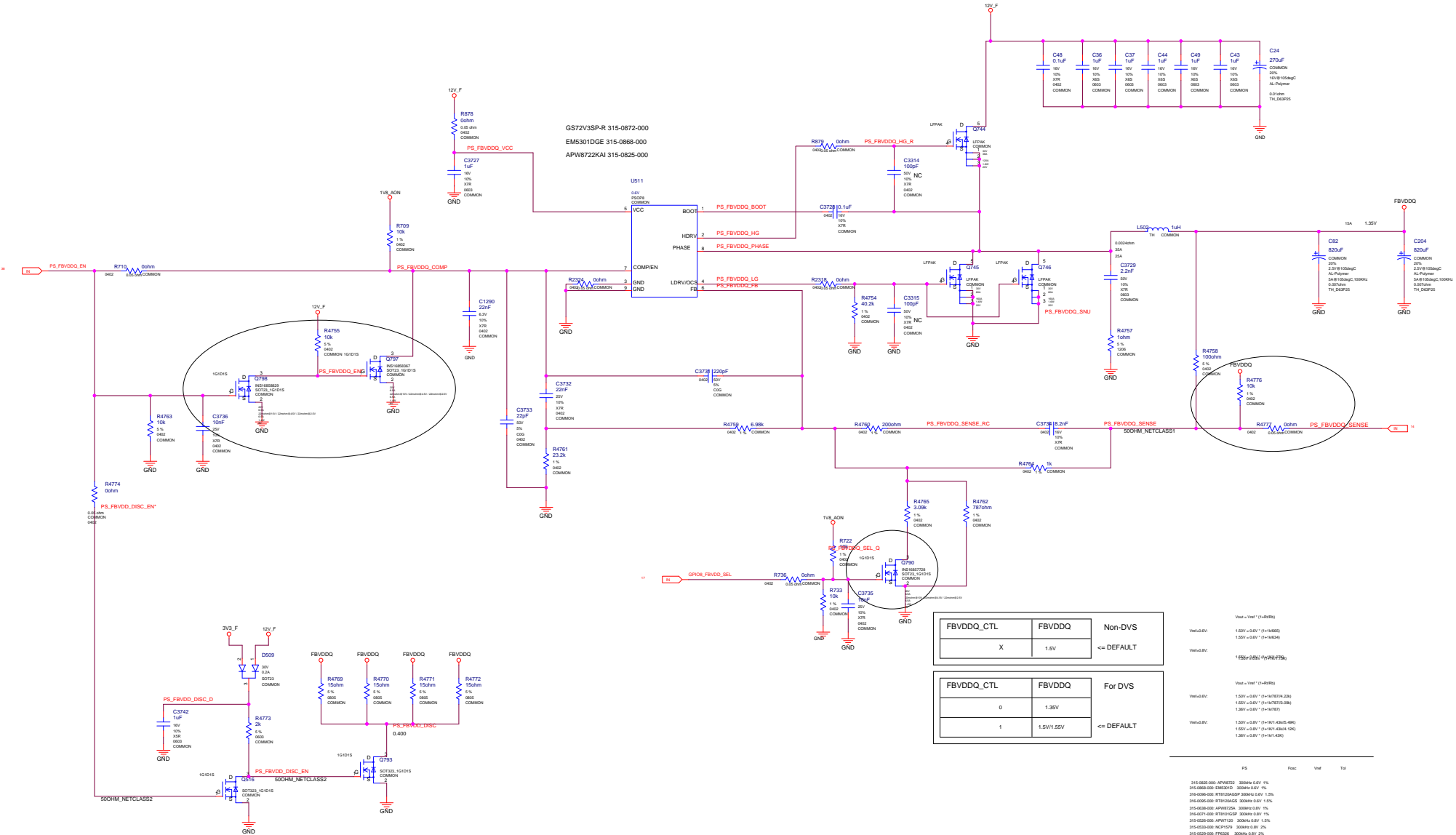
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Vref = 1.05V ± 0.0V * (1 + 1.570713, 236)
Vref = 1.05V ± 0.0V * (1 + 1.570703, 498)
Vref = 1.05V ± 0.0V * (1 + 1.570787)

Val = Vref * (1 + R5R5)
Vref = 1.05V ± 0.0V * (1 + 1.5714305, 498)
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Vref = 1.05V ± 0.0V * (1 + 1.5714304, 498)

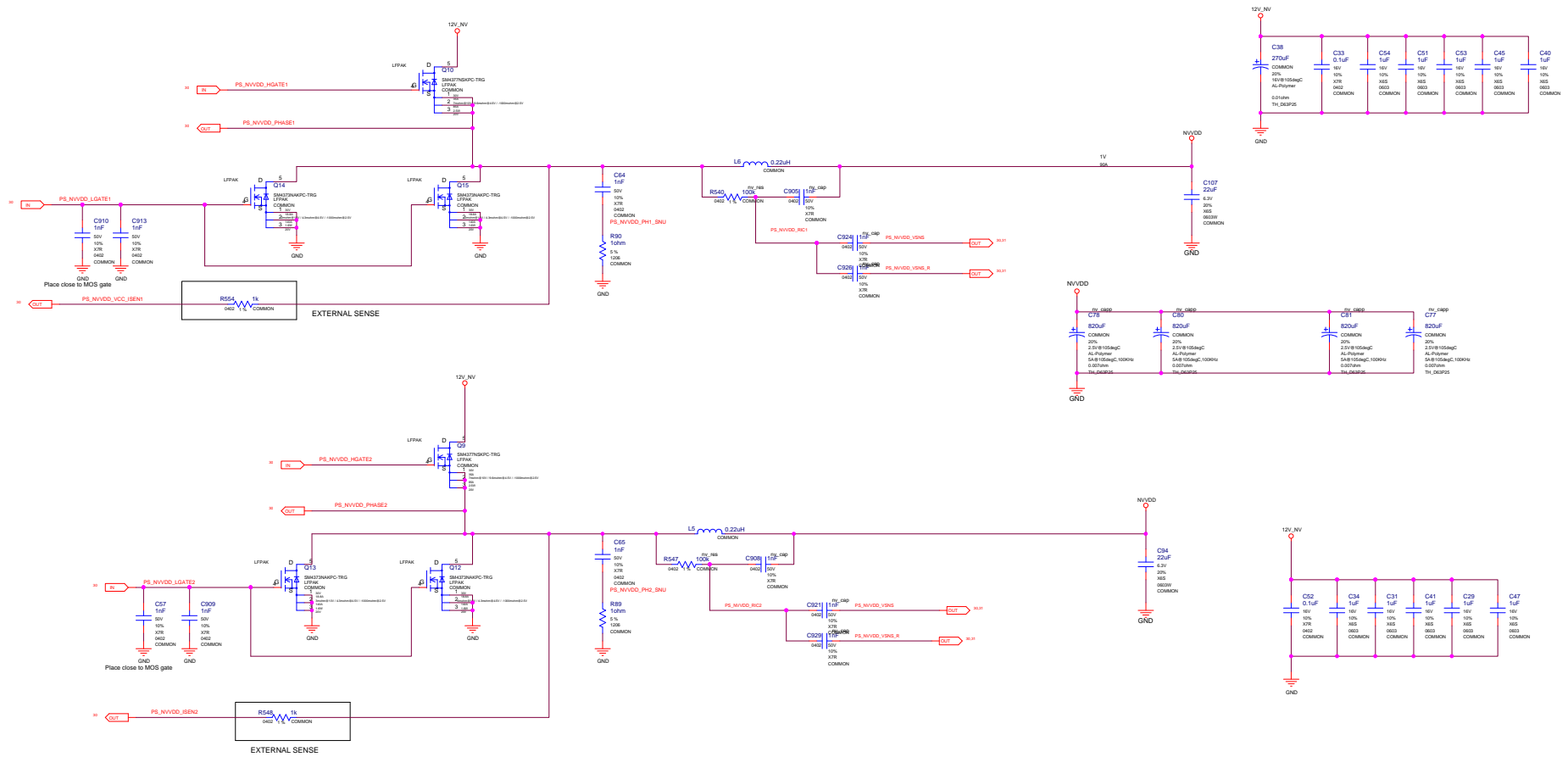
PS	Part	Val	Tol
315-0025-000	APW822	300nA ± 0.0V	1%
315-0080-000	EM520D	300nA ± 0.0V	1%
315-0080-000	RTS-D3AGCP	300nA ± 0.0V	1.5%
315-0095-000	RTS-D3AGD	300nA ± 0.0V	1.5%
315-0080-000	APW725A	300nA ± 0.0V	1%
315-0071-000	RTS-D3GSP	300nA ± 0.0V	1%
315-0055-000	APW713D	300nA ± 0.0V	1.5%
315-0050-000	NC7P175	300nA ± 0.0V	2%
315-0050-000	FPF328	300nA ± 0.0V	2%

FBVDDQ_CTL	FBVDDQ	Non-DVS
X	1.5V	<= DEFAULT

FBVDDQ_CTL	FBVDDQ	For DVS
0	1.35V	<= DEFAULT
1	1.5V/1.55V	<= DEFAULT



PS: NVVDD Phase 1,2



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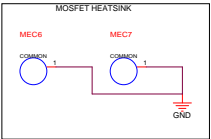
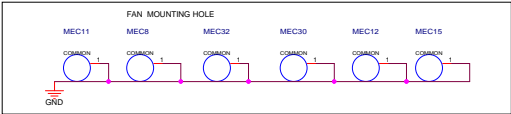
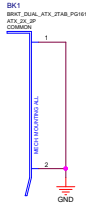


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Mechanical: Bracket/Thermal Solution

Bracket:



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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	MECH: Bracket/Thermal

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
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