

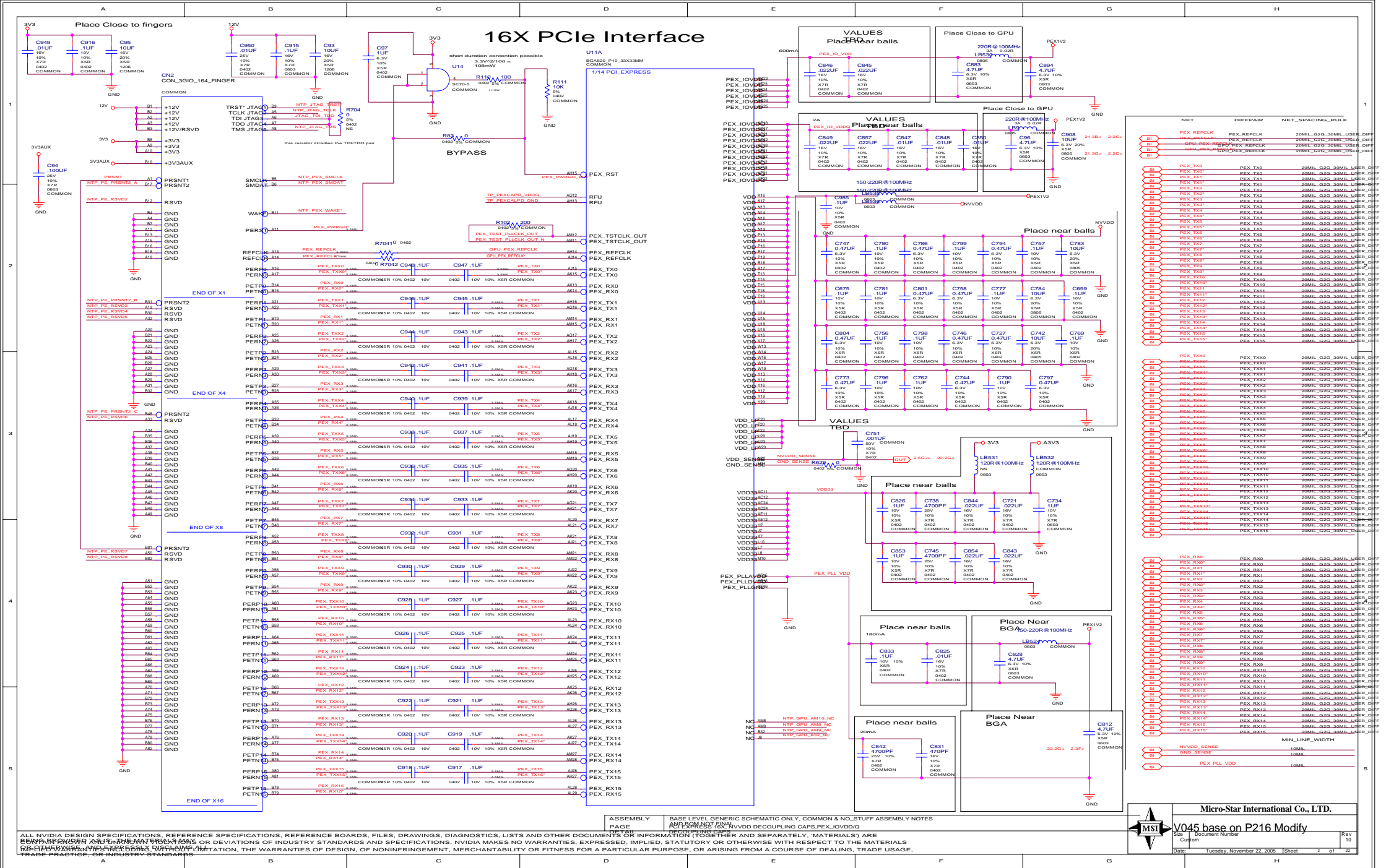
V045 -- NV43, 128/256 MB DDR3, VGA, DVI-I, SD/HDTV, VIVO

SUMMARY:

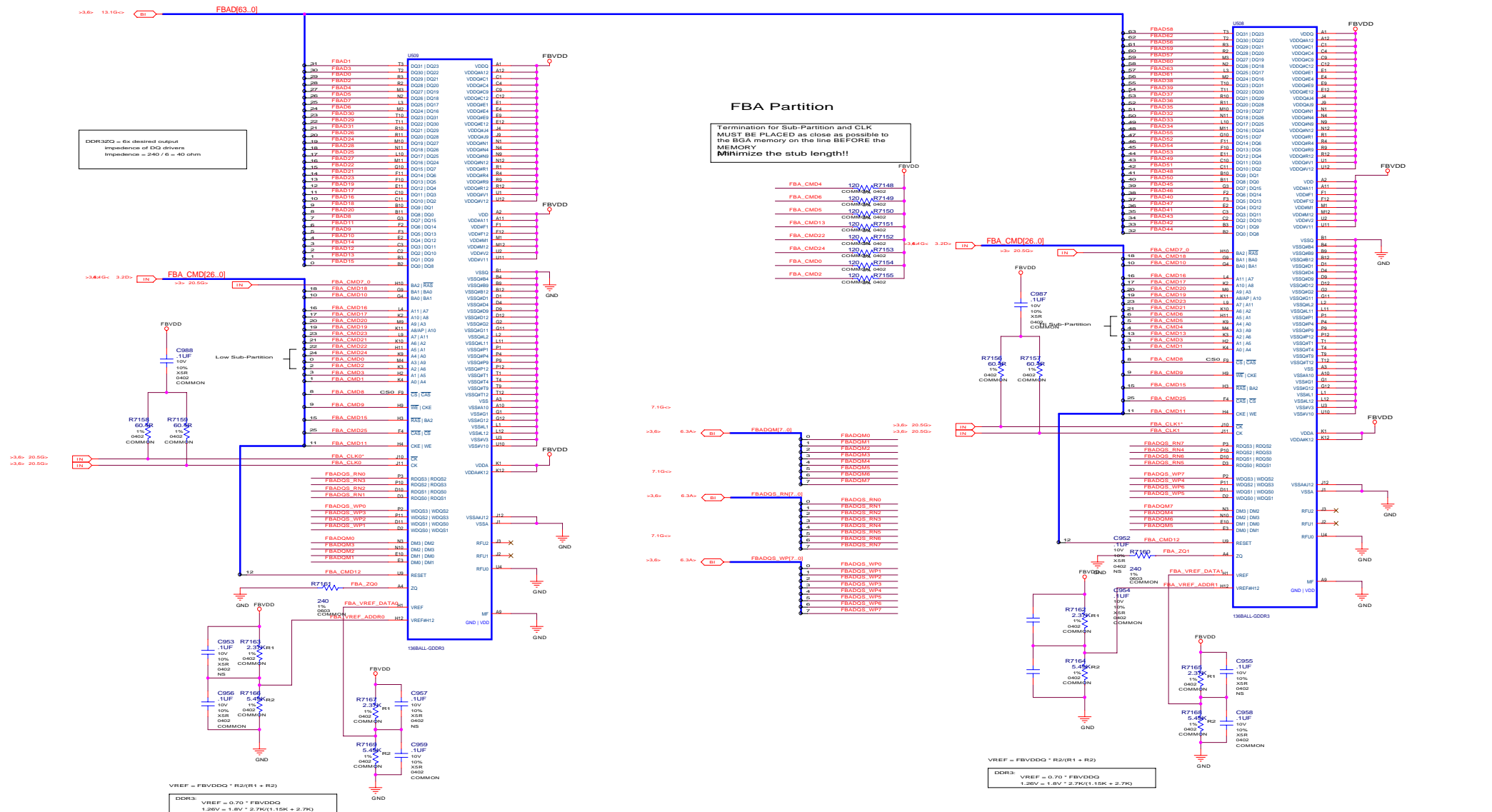
- 1. Base on V023 to Modify
- 2. BGA-136 DDRIII
- 3. Add G73 2V5 Power

SRU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10216-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
1	000	602-10216-0000-200	NV43-10216-0000-200 128MB DDR3 8MX32
2	001	602-10216-0001-200	NV43-10216-0001-200 128MB DDR3 8MX32
3	002	602-10216-0002-200	NV43-10216-0002-200 128MB DDR3 8MX32
4	003	602-10216-0003-200	NV43-10216-0003-200 128MB DDR3 8MX32
5	<UNDEFINED>	<UNDEFINED>	NV43-10216-0004-200 128MB DDR3 8MX32
6	<UNDEFINED>	<UNDEFINED>	NV43-10216-0005-200 128MB DDR3 8MX32
7	<UNDEFINED>	<UNDEFINED>	NV43-10216-0006-200 128MB DDR3 8MX32
8	<UNDEFINED>	<UNDEFINED>	NV43-10216-0007-200 128MB DDR3 8MX32
9	<UNDEFINED>	<UNDEFINED>	NV43-10216-0008-200 128MB DDR3 8MX32
10	<UNDEFINED>	<UNDEFINED>	NV43-10216-0009-200 128MB DDR3 8MX32
11	<UNDEFINED>	<UNDEFINED>	NV43-10216-0010-200 128MB DDR3 8MX32
12	<UNDEFINED>	<UNDEFINED>	NV43-10216-0011-200 128MB DDR3 8MX32
13	<UNDEFINED>	<UNDEFINED>	NV43-10216-0012-200 128MB DDR3 8MX32
14	<UNDEFINED>	<UNDEFINED>	NV43-10216-0013-200 128MB DDR3 8MX32
15	<UNDEFINED>	<UNDEFINED>	NV43-10216-0014-200 128MB DDR3 8MX32

X01

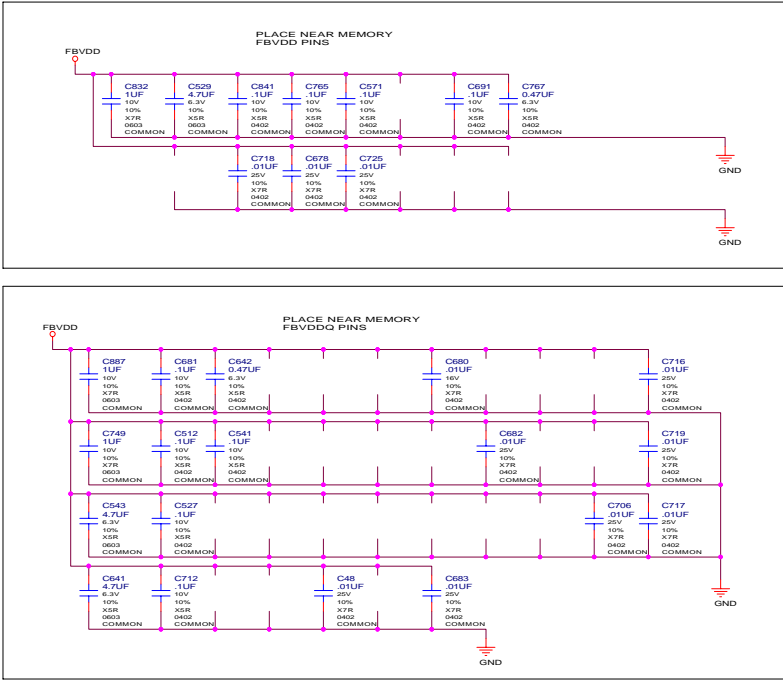


5 FrameBuffer: Partition A
8Mx32 BGA136 DDR3

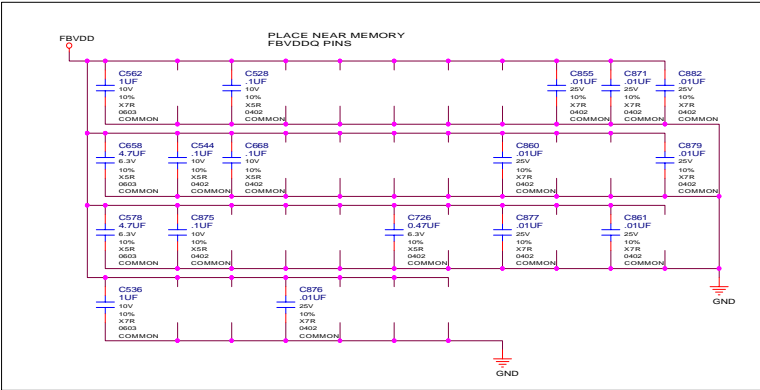
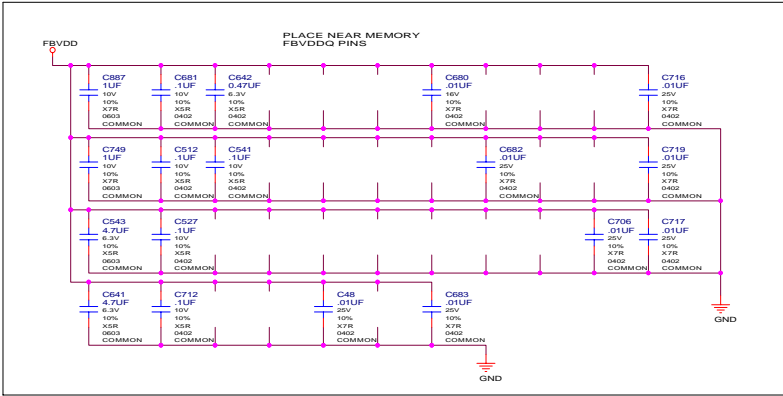
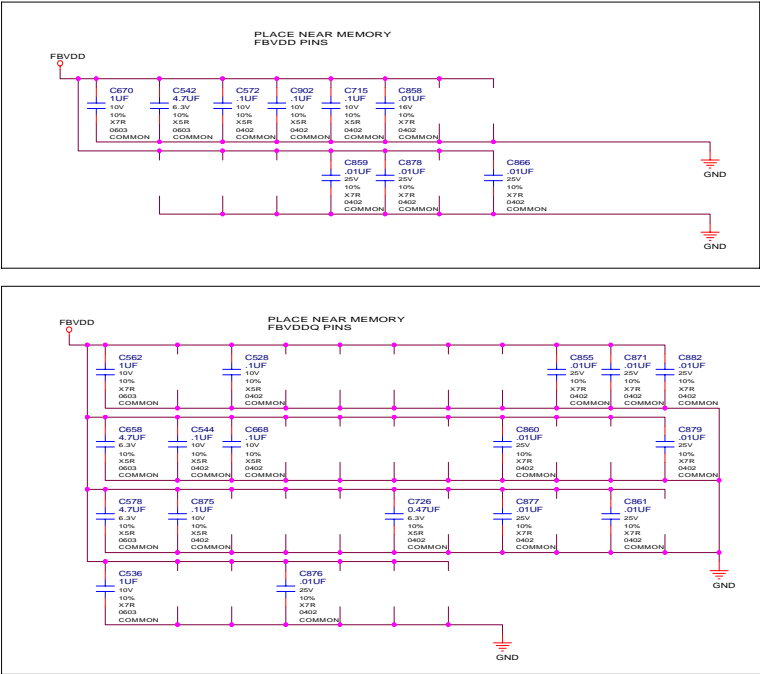


FRAME BUFFER: PARTITION A
DECOUPLING

Decoupling for FBA 0..31

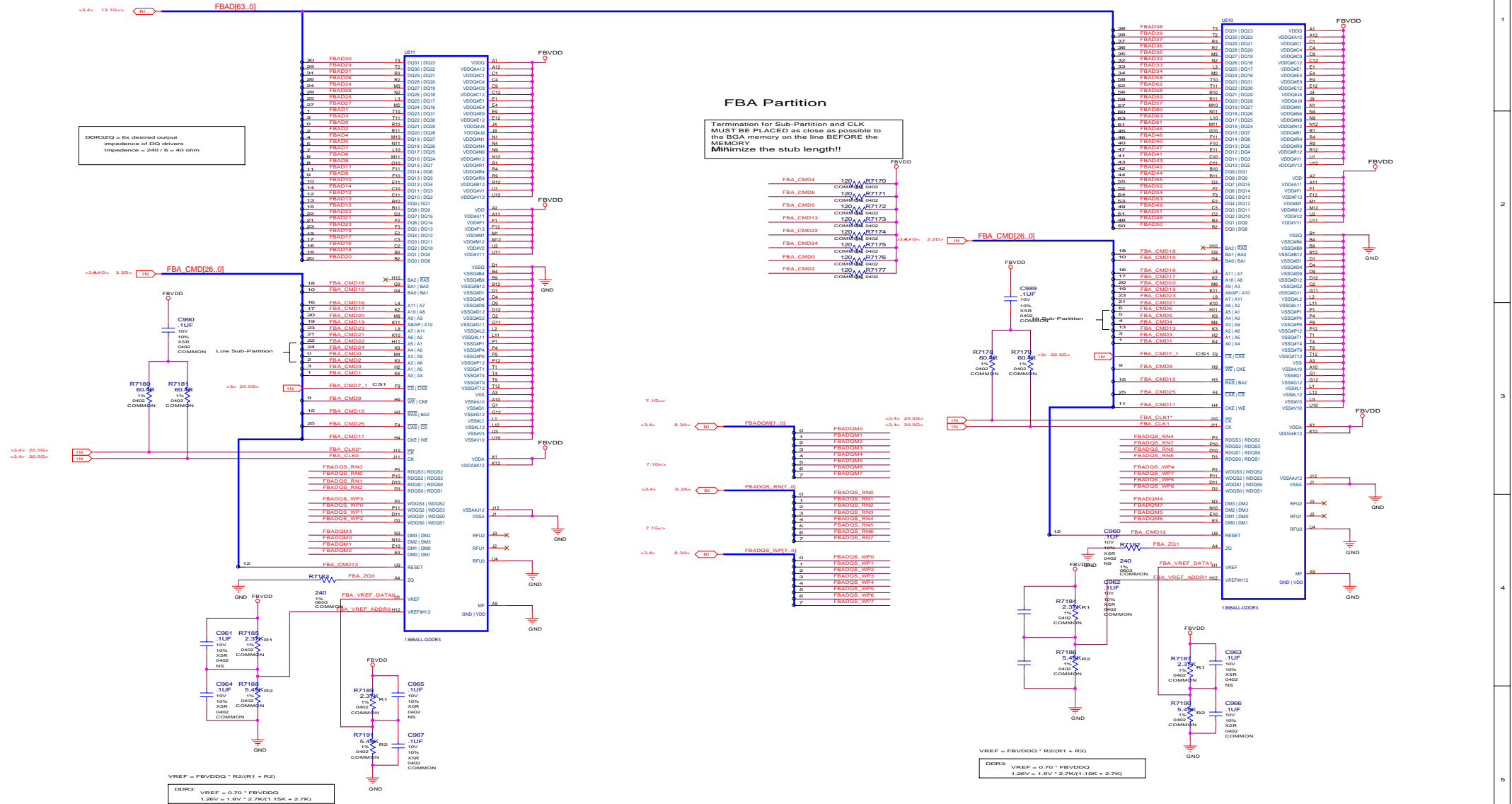


Decoupling for FBA 32..63



5 FrameBuffer: Partition A

8Mx32 BGA136 DDR3



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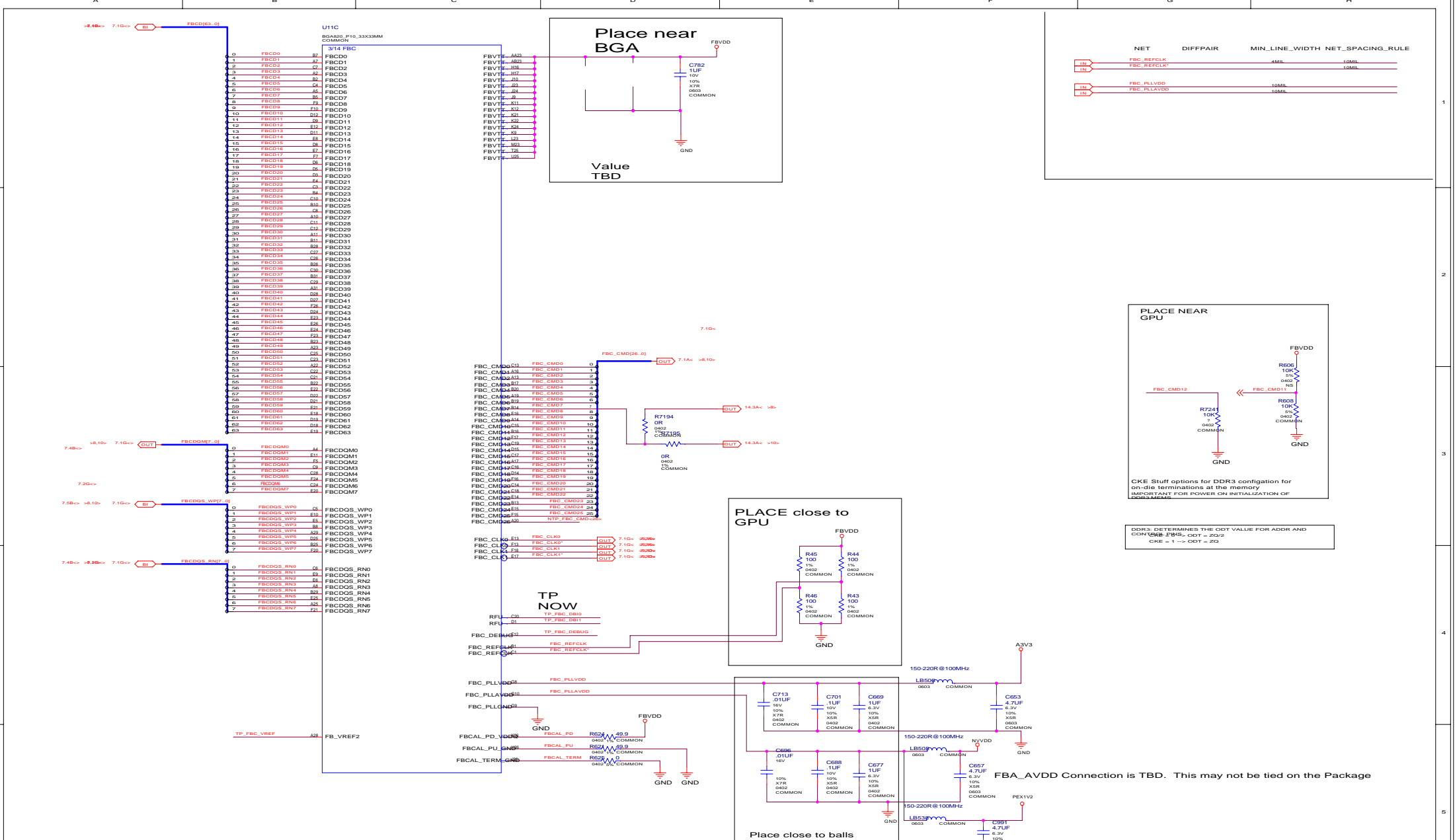
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE	AND ROM NOT FINAL FBA 8MX32 DDR3 MEMORIES, FBA COMMAND BUS PU'S, FBA



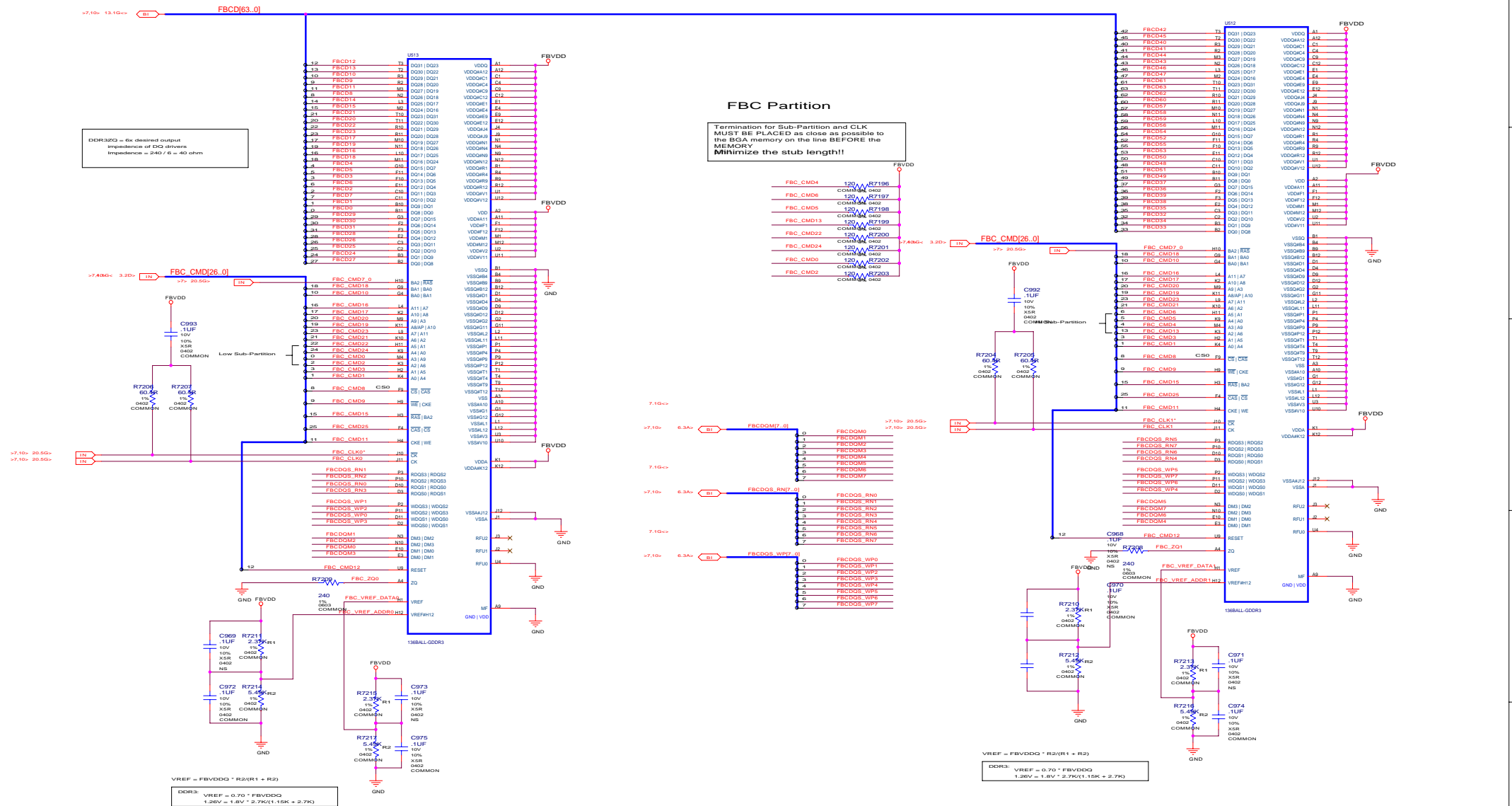
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→ V045 base on P216 Modify

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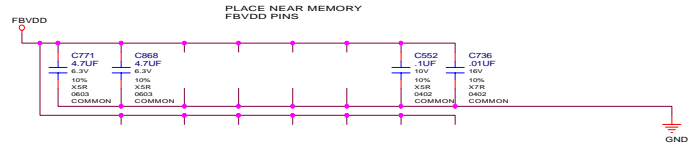


FRAMEBUFFER: PARTITION
C 8Mx32 BGA136 DDR3

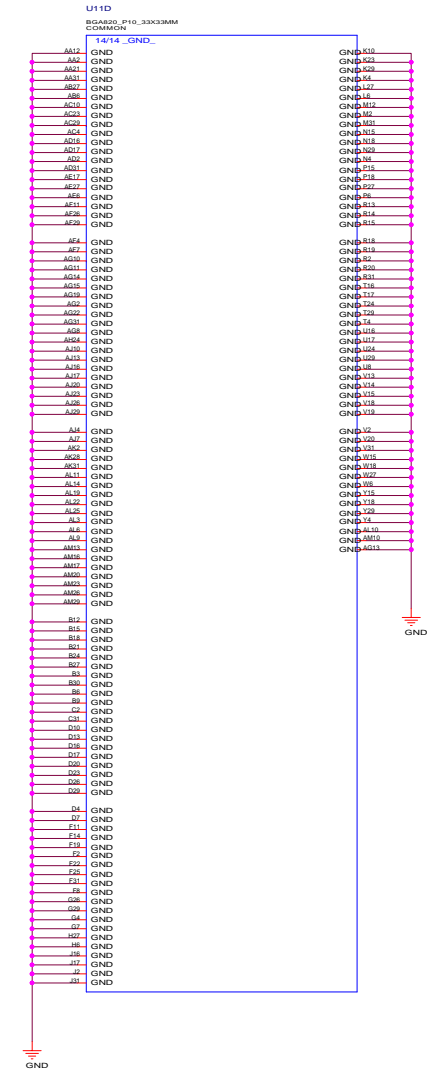
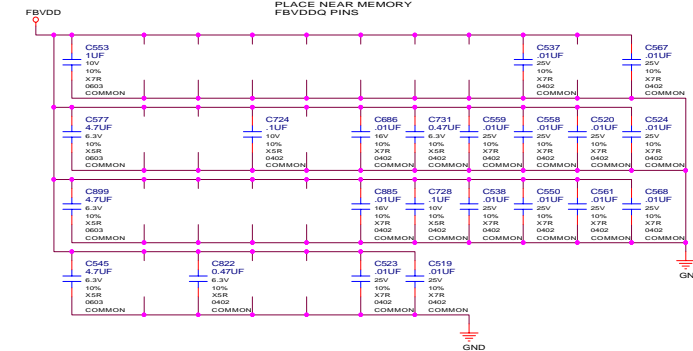
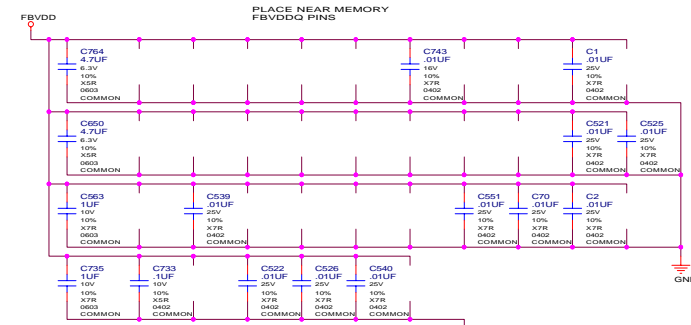
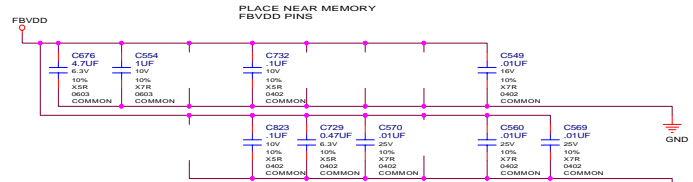


FRAMEBUFFER: PARTITION C DECOUPLING

Decoupling for FBC 0..31

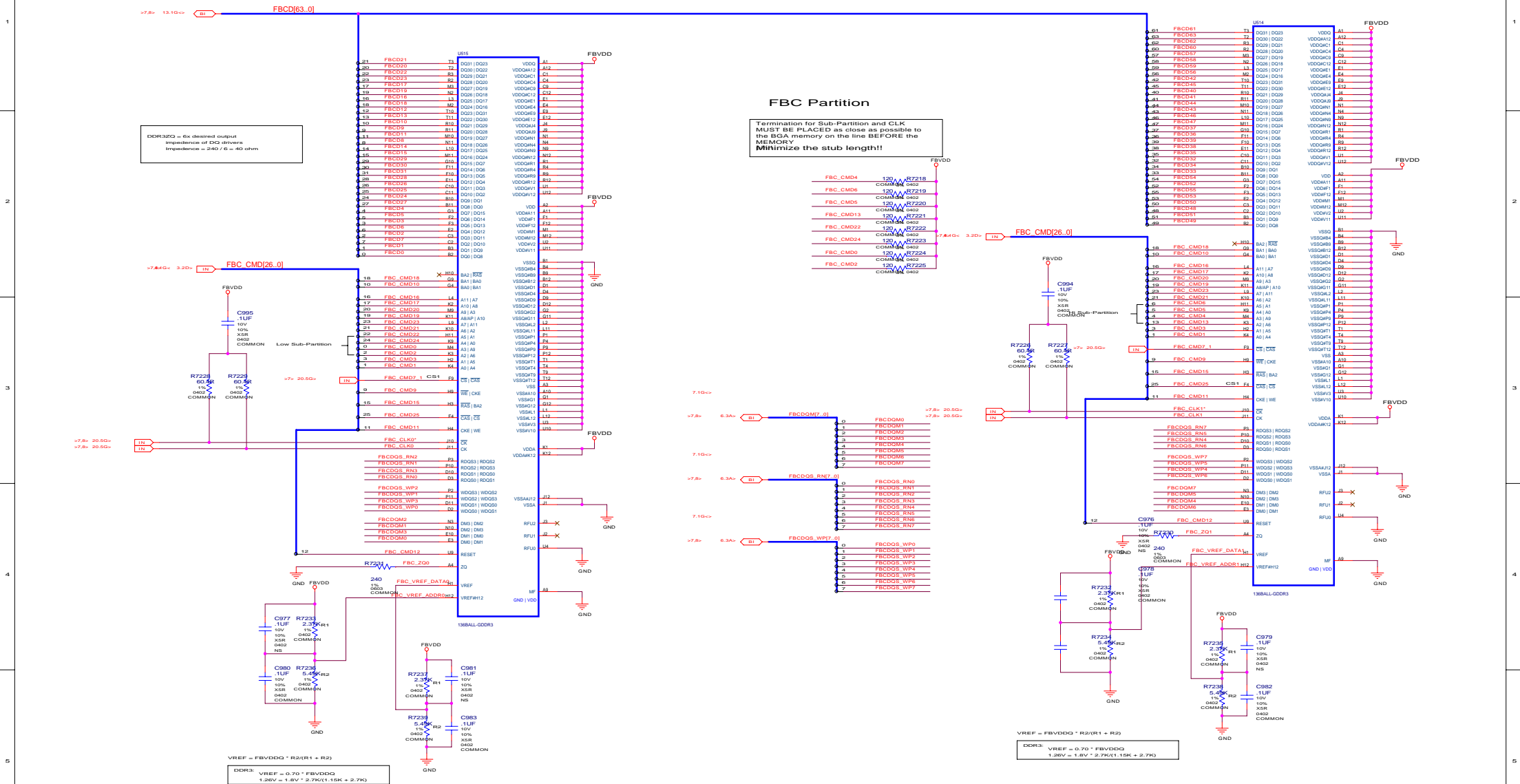


Decoupling for FBC 32..63

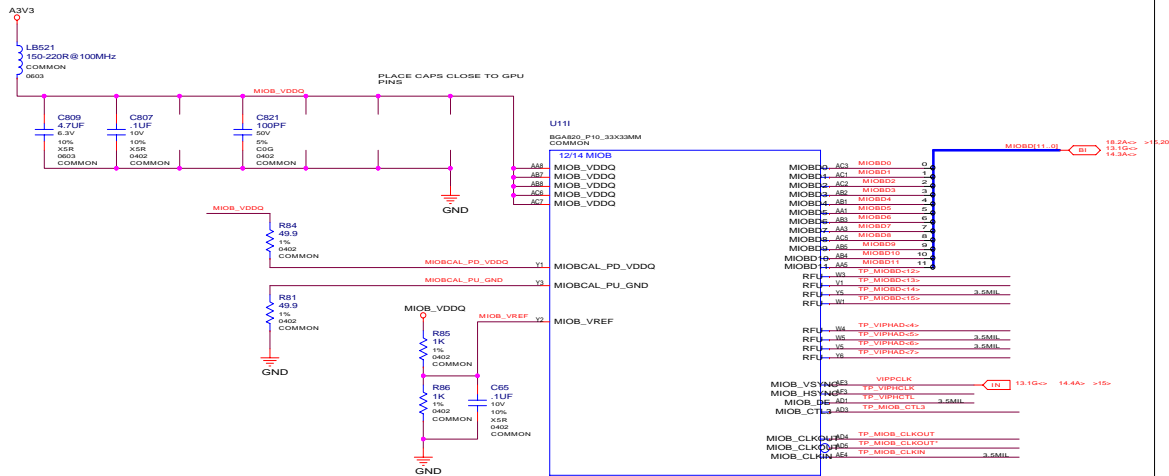


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FRAMEBUFFER: PARTITION
C 8Mx32 BGA136 DDR3

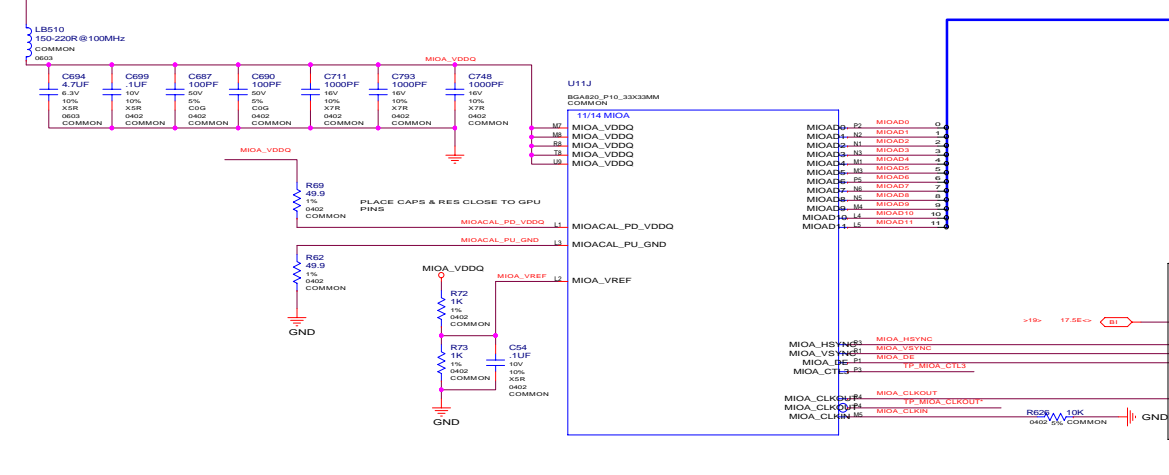


G3 VIP/MIOB

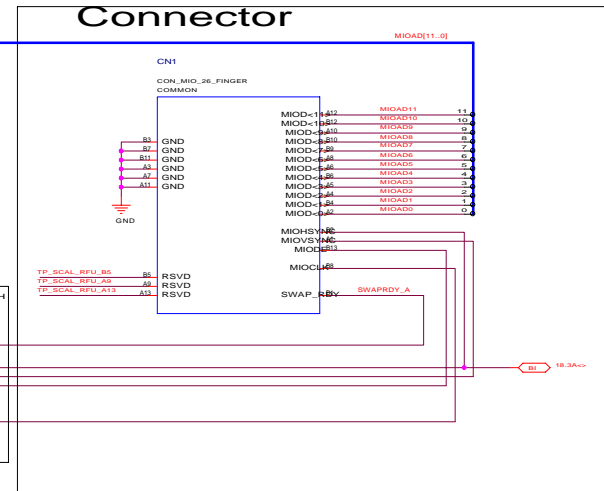


NETNAME	MIN_LINE_WIDTH	SPACING RULE
MIOB_VDDQ	3.5MIL	12MIL
MIOB_VREF	3.5MIL	12MIL
MIOA_VDDQ	3.5MIL	12MIL
MIOA_VREF	3.5MIL	12MIL

G3 MIOA

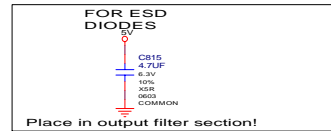


Feature Connector



DDC_5V 12MIL

DACA RGB-FILTER



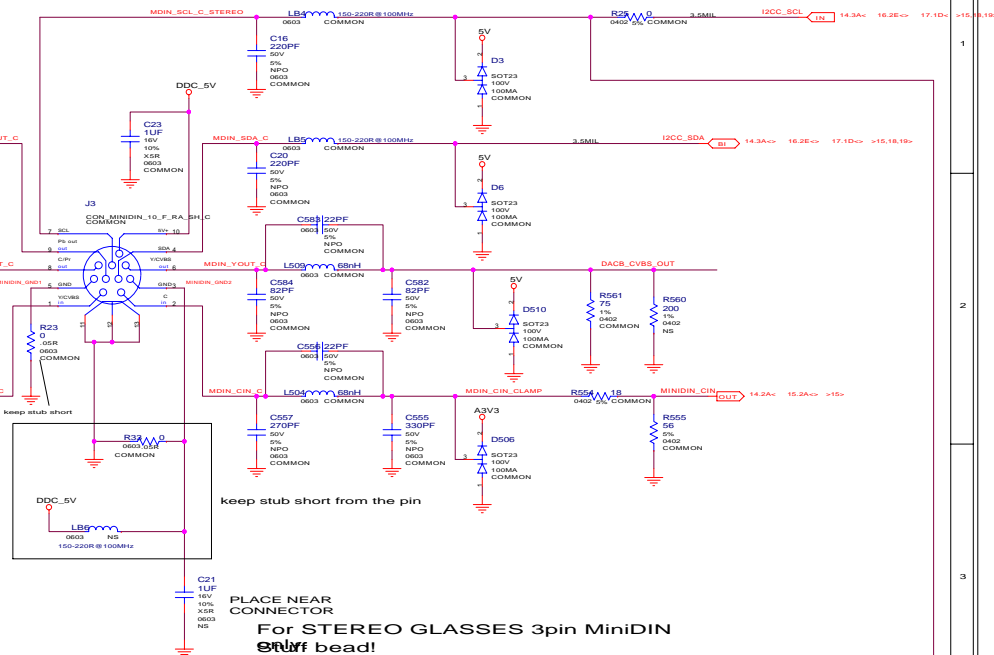
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC, COMMON & NO-START ASSEMBLY NOTES
PAGE	AND BOM NOT FINAL DATA FILTERS, DATA SYNC

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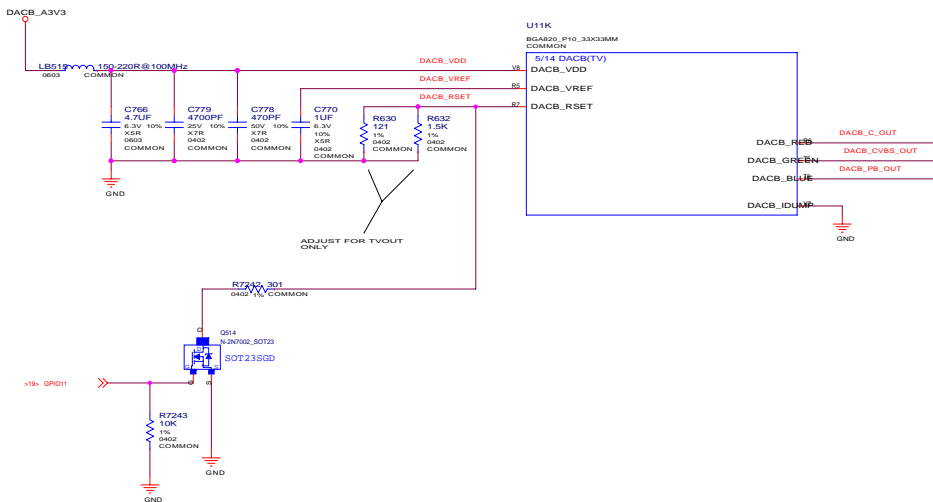
▶ V045 base on P216 Modify


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	NET_NAME	MIN_LINE_WIDTH	IMPEDANCE	NET_SPACING_RULE
	OUT	DACB_C_OUT	U11.B6.S544.1.37.50 ohm±2 %	20MIL
	OUT	DACB_CVBS_OUT	U11.TA.R561.1.37.50 ohm±2 %	20MIL
	OUT	DACB_P6_OUT	U11.TA.R541.1.37.50 ohm±2 %	20MIL
	BI	MDIN_PBOOT_C		20MIL
	BI	MDIN_VREF_C		20MIL
	BI	MDIN_VREF_C		20MIL
	BI	MDIN_VREF_C		20MIL
14 1Aa	BI	MDINDIN_Y_CVBSIN		20MIL
15 1C1	BI	MDIN_Y_CIN		20MIL
	BI	MDIN_VIN_CLAMP		20MIL
	BI	MDIN_VIN_CLAMP		20MIL
	BI	MDIN_CIN_C		20MIL
	BI	MDINDIN_CIN		20MIL
	BI	MDIN_CIN_C2_CLAMP		20MIL
14 2Aa	BI	MDIN_CIN_C		20MIL
15 2H1	BI	MDIN_CIN_C		20MIL
	IN	DACB_VDD	12MIL	
	IN	DACB_VREF	12MIL	
	IN	DACB_RESET	12MIL	



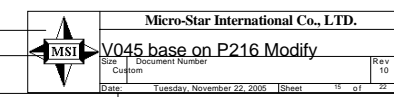
For STEREO GLASSES 3pin MiniDIN
~~only~~ bead!
And replace 0 Ohm resistor with 220PF cap!

[illegible]

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	V045 base on P216 Modify		
	Size Custom	Document Number	Rev 10
	Date: Tuesday, November 22, 2005	ISheet 14 of 22	

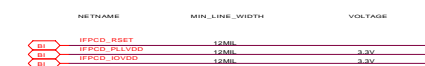
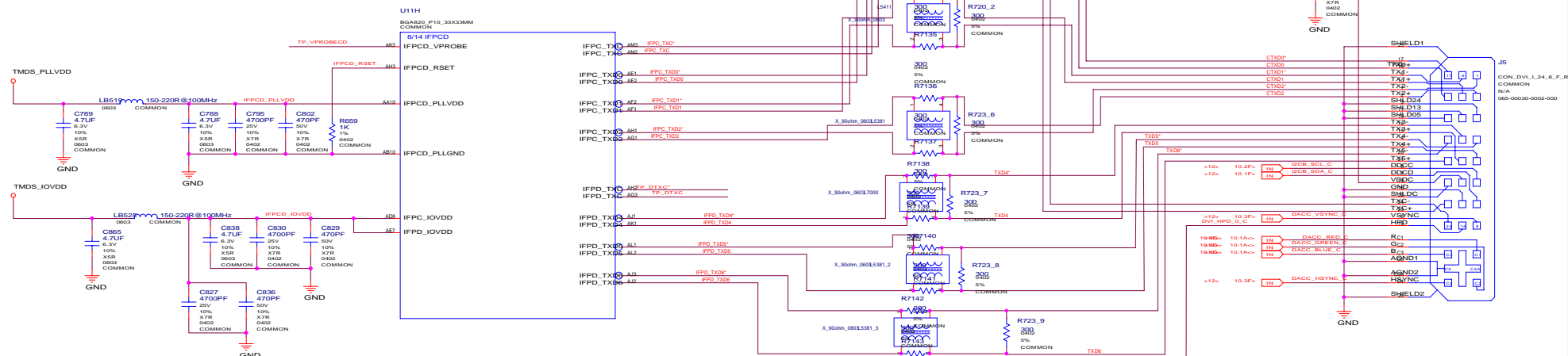
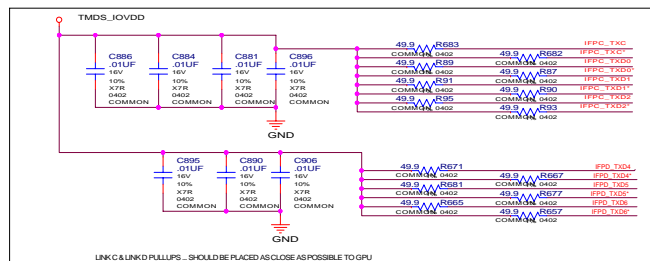
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NETNAME	MIN_LINE_WIDTH
VDDA	12MIL
B1 VDDX	12MIL
B1 VDDY	12MIL
B1	12MIL

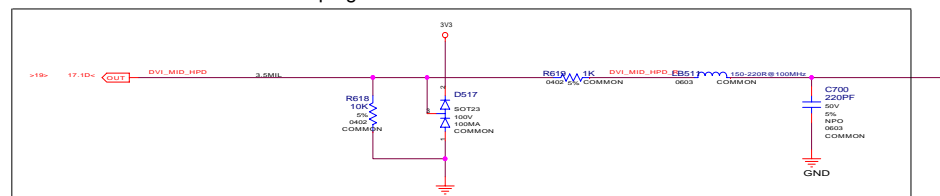


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INTERNAL TMDS .. LINK C & D



Hotplug Detection



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE	108-BCM-V01.DWG, DVI CONNECTOR

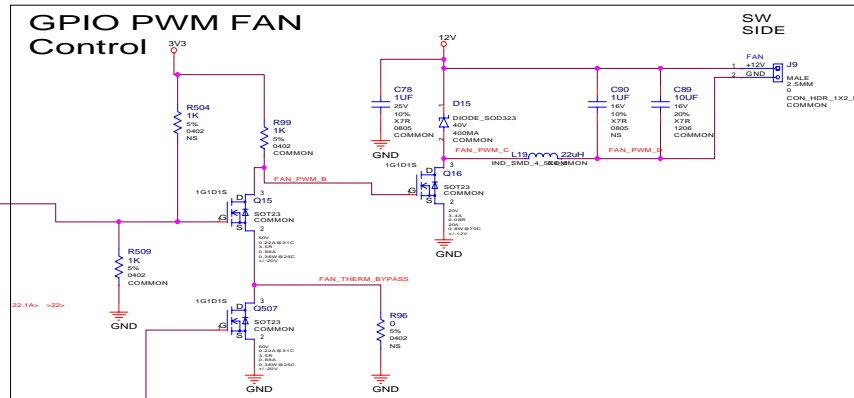
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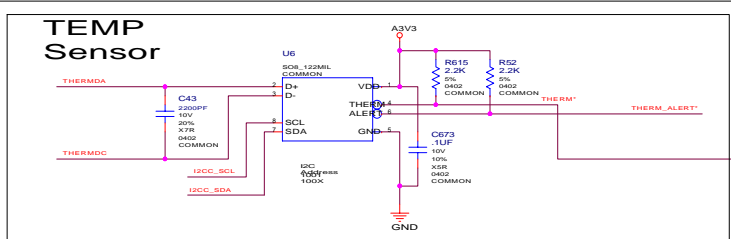
V045 base on P216 Modify

Size	Document Number	Rev
Custom		10

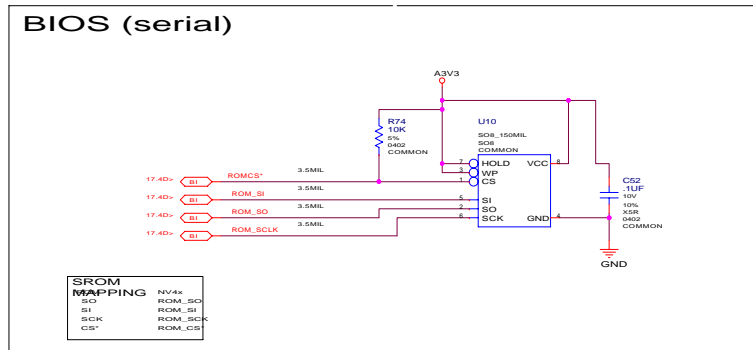
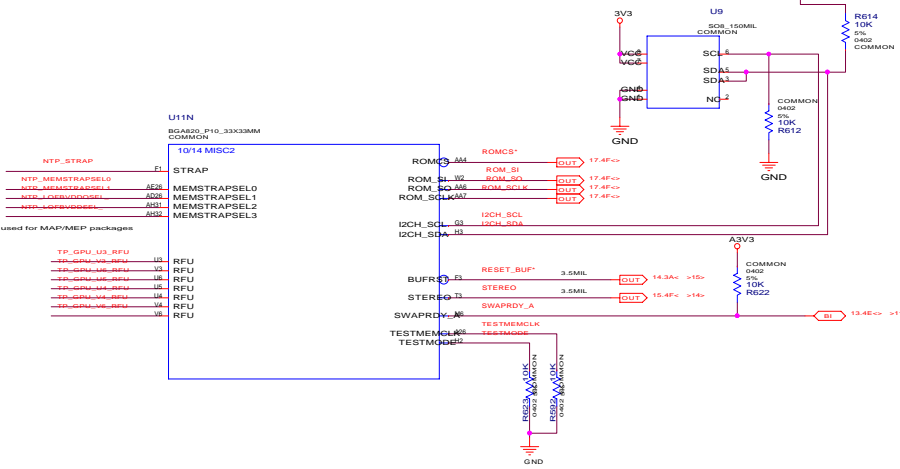
[illegible]




GPIO Assignment		
<u>Table</u>		
GPIO		FUNCTION
0	IN	DVI MID HOTPLUG
1	IN	DVI SOUTH
2	IN	HDDETECT
3	IN	RESERVED
4	IN	TUNER
5	OUT	VOLTAGE
6	OUT	WAKEUP
7	IN	RESERVED
8	IN	EXTERNAL POWER
9	OUT	RESERVED/TEMP ALERT
10	IN	RESERVED
11	IN	RESERVED
12	IN	RESERVED



AUDIO and VIDEO signals are reserved for future GPU's. NV4x will not have support for these signals



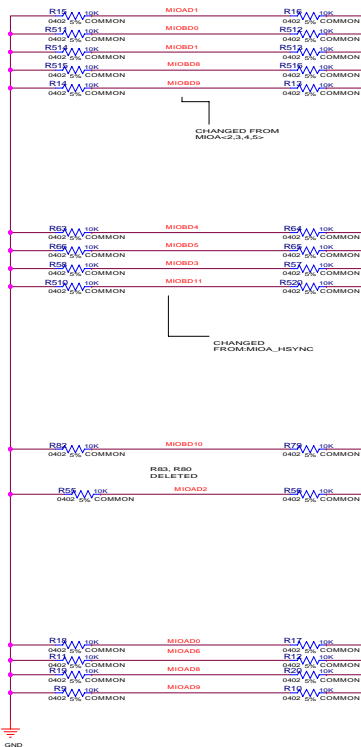
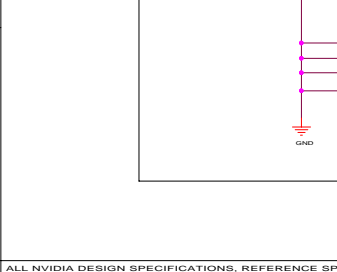
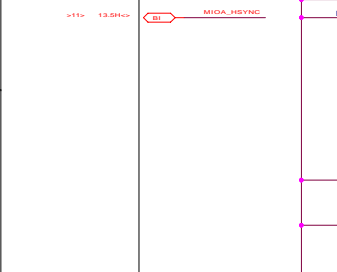
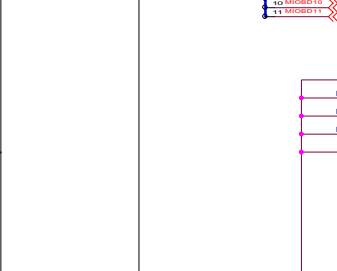
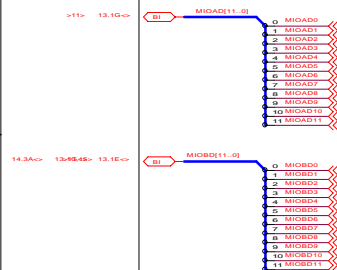
	NETNAME	MIN_LINE_WIDTH	VOLTAGE
	THERMDC	10MIL	
(B1)	THERMDA	10MIL	
(B1)			
	FAN_PWM_B	12MIL	
(B1)	FAN_PWM_C	12MIL	
(B1)	FAN_PWM_D	12MIL	

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	V045 base on P216 Modify		
	Size	Document Number	Rev
	Custom		10
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BIOS,
Straps,
Straps
Misc

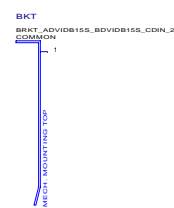
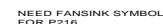
Assembly:
BIOS

Mechanical parts

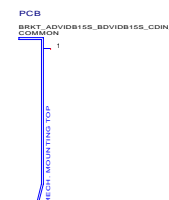


02	PCL_AD_SWAP	PCL_AD_SWAP	0	Reversed
03	SUB_VENDOR	SUB_VENDOR	0x0000	Default
04	RAM_CFG_0	RAM_CFG[3:0]	0x00000000	BKOS
05	RAM_CFG_1		0x00000000	NO
06	RAM_CFG_2		0x00000000	NO
07	RAM_CFG_3		0x00000000	NO
08	CRYSTAL_0	CRYSTAL[1:0]	0x11550000	NO
09	CRYSTAL_1		01 14.318 MHz	NO
10	TV_MODE_0	TV_MODE[1:0]	00 27.000 MHz	NO
11	AGP_ENABLE	AGP_30_6x	0	AGP=0000
12	AGP_SBA	AGP_SBA[0]	0	AGP=0000
13	AGP_FASTWR	AGP_FASTWR[0]	0	AGP=0000
14	PCL_DEVID_0	PCL_DEVID[3:0]	0000 0x140	1111 0x014F
15	PCL_DEVID_1		0000 (default 0x140)	
16	PCL_DEVID_2		0101 (0x14D)	
17	PCL_DEVID_3			
18	BUS_TYPE	BUS_TYPE[0]	0	PCI
19	FP_IFACE	FP_IFACE[0]	0	PCI
20	FB_0	FB[1:0]	0x00000000	0x00000000
21	FB_1		0x00000000	0x00000000
22	BR	BR[0]	0	BRIDGE
23	BR_128M		0	BRIDGE
24	BR_AGP		0	BRIDGE
25	BR_IO		0	BRIDGE
26	ROM_TYPE_0	ROM_TYPE[1:0]	00	Parallel
27	ROM_TYPE_1		00	Serial
28	USER_0	STRAP_USER[3:0]	0000	Default
29	USER_1		0000	Default
30	USER_2		0000	Default
31	USER_3		0000	Default

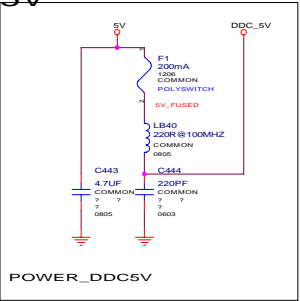
REG:	NV_STRAP_1	
Bit Signal	VALUE_ID	VALUES
11:		0 (default -- internal term on)
PEX_PLLEN_TERM100		
12:		
3GIO_PADCFG_LUT_ADR[0]		
13:		
3GIO_PADCFG_LUT_ADR[1]		
14:		
3GIO_PADCFG_LUT_ADR[2]		



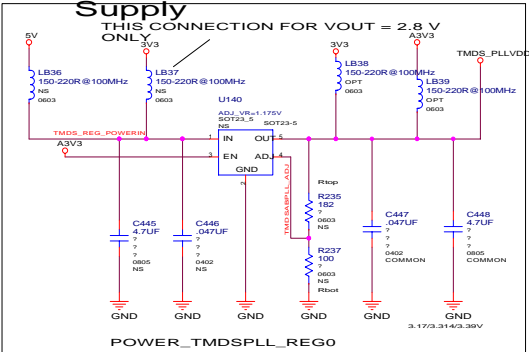
155-00002-0000-000 SCREW PHIL PAN HD SS MACH 4-40
3/16



Power Supply ...
TMDS/A3V3/FBVDD
DDC
5V

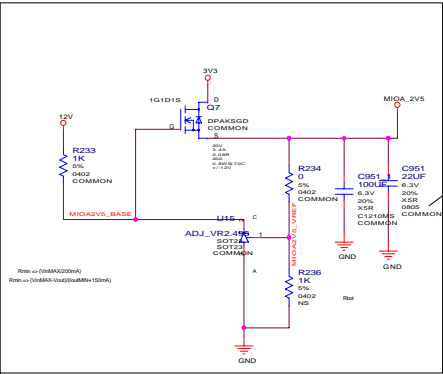


TMDS AB/CD PLL



$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$
 $3.31V = 1.175V * (1 + (100/182))$

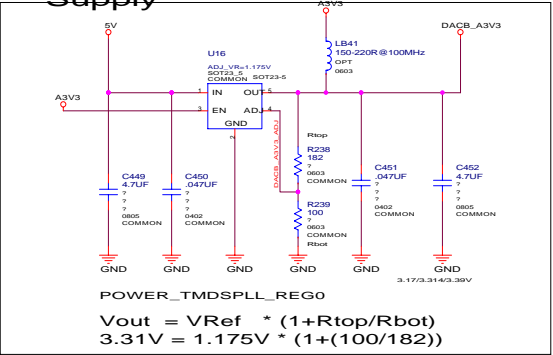
MIOA_VDDQ



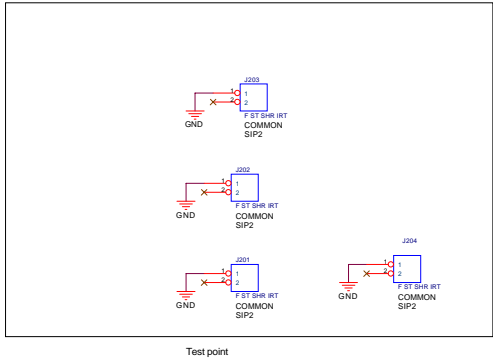
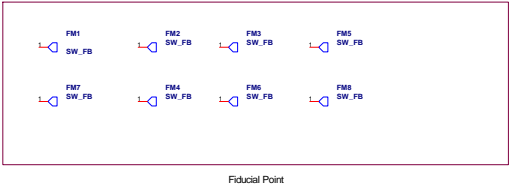
$V_{ref} = 2.5V$
 $V_{out} = 2.495(1 + R_{top}/R_{bot}) + (I_{ref} + R_{top})$
For $V_{out} = V_{ref}$ ($R_{top} = 0ohm$, $R_{bot} = NO\ STUFF$)

NETNAME	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	12MIL	5V
DDC_5V	12MIL	5V
3V3	12MIL	3.3V
TMDSAB/CD_PLL	12MIL	3.3V
TMDS_PLLVDD	12MIL	3.3V
12V	35MIL	12V
MIOA_2V5	12MIL	2.5V
GND	35MIL	0V
DACB_A3V3_ADJ	10MIL	3.3V
DACB_A3V3	12MIL	3.3V

DACB
Supply



$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$
 $3.31V = 1.175V * (1 + (100/182))$



ISL6549 for Nvidia NV4x Graphic card power ckt

