P691: G98/GT218, DDR2 MEMORY 64MX16/32MX16

Page 1: P691 Overview

Page 2: PCI Express Interface

Page 3: Frame Buffer Interface

Page 4: DDR2 Memories

Page 5: DAC A Slim VGA

Page 6: DAC B VGA Header

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Page 8: DisplayPort Connector

Page 9: IFPC, IFPE Interface, Mechanical, SPDIF

Page 10: XTAL, ROM, JTAG

Page 11: Thermal Protection, Protected 3V3, Straps

Page 12: Power Supply I: FBVDD/Q, PEX_VDD, 5V, 3V3_F

Page 13: Power Supply II: PEX_PLLVDD, NVVDD

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SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10691-BASE-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10691-0001-100	GT218-300, 550/1375/500, 256MB/64bit, 32Mx16 DDR2, DVI-DL+DP+VGA, DT
2	SKU0002	600-10691-0002-100	GT218-300, 550/1375/500, 512MB/64bit, 64Mx16 DDR2, DVI-DL+DP+VGA, DT
3	SKU0010	600-10691-0010-100	G98-400, 550/1375/500, 256MB/64bit, 32Mx16 DDR2, DVI-DL+DP+VGA, DT
4	SKU0011	600-10691-0011-100	G98-400, 550/1375/500, 512MB/64bit, 64Mx16 DDR2, DVI-DL+DP+VGA, DT
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P691 Overview

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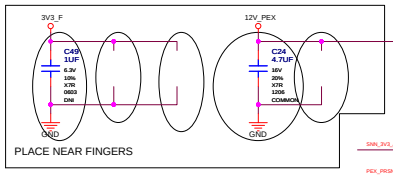
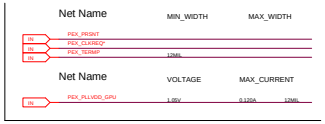
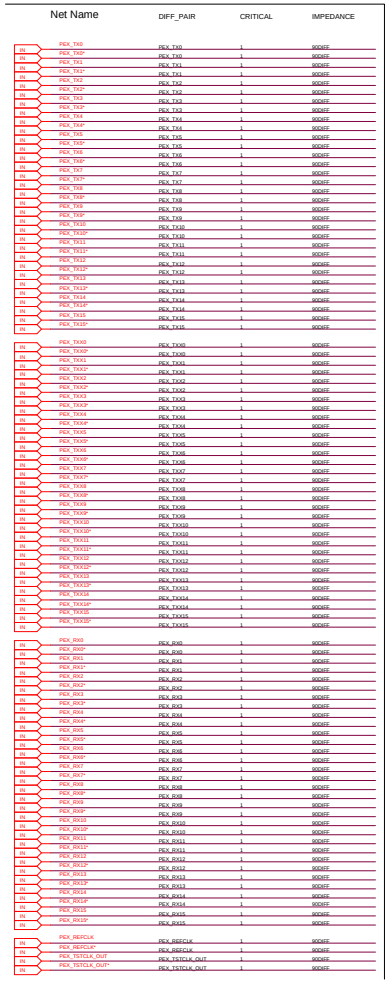
NV_PN	600-10691-BASE-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

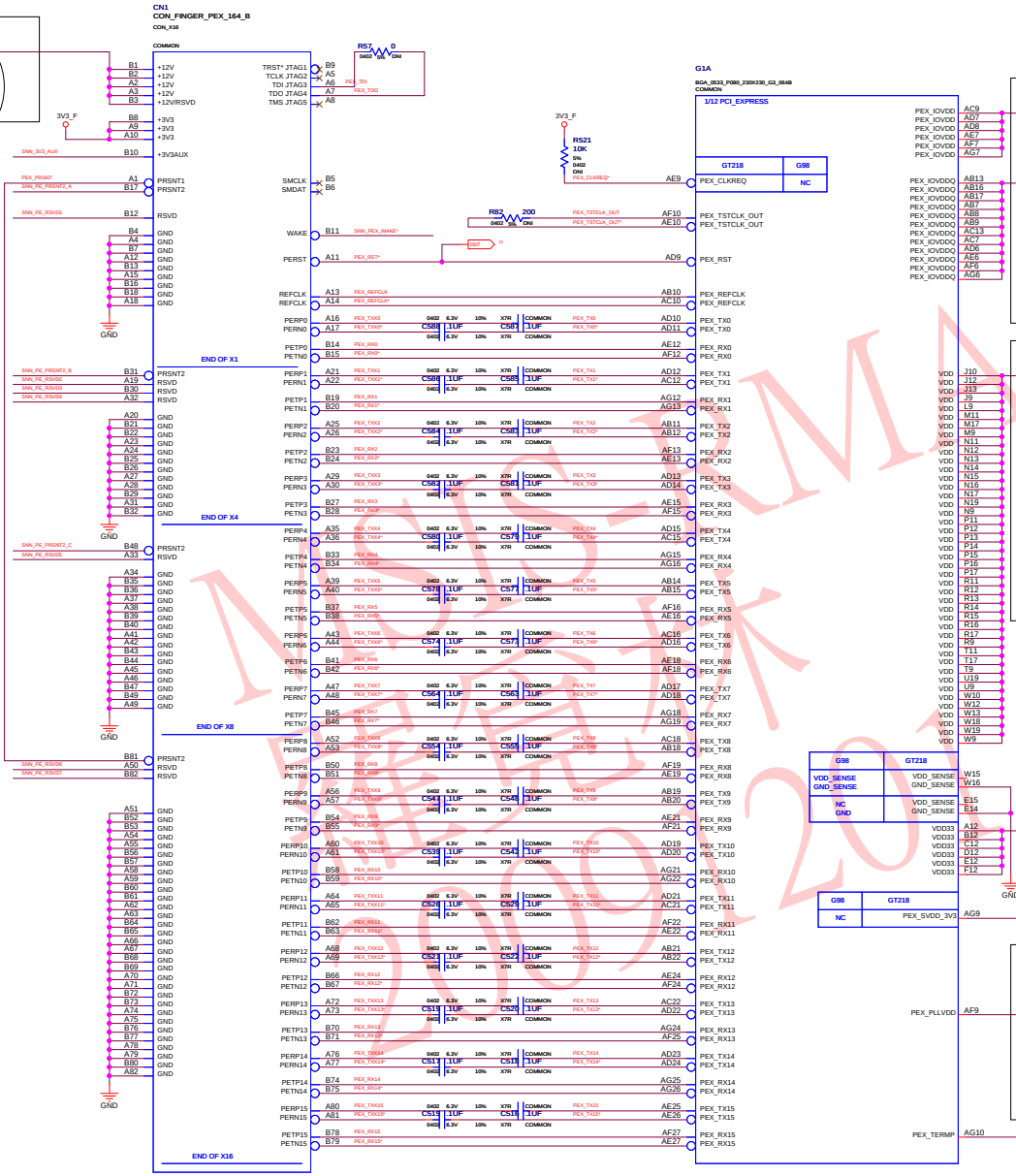
PCI Express Interface

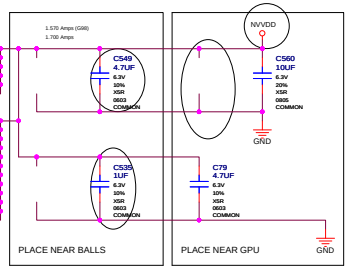


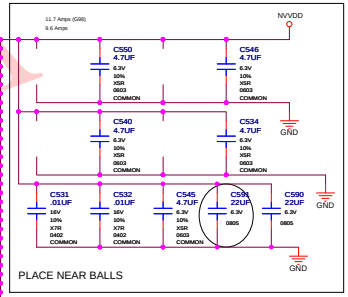


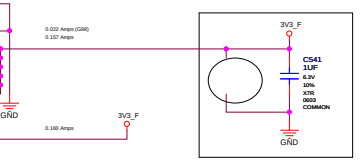
9

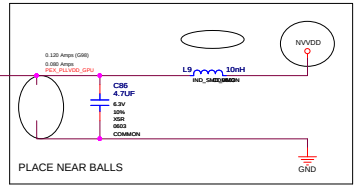












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PAGE DETAIL	PCI Express Interface

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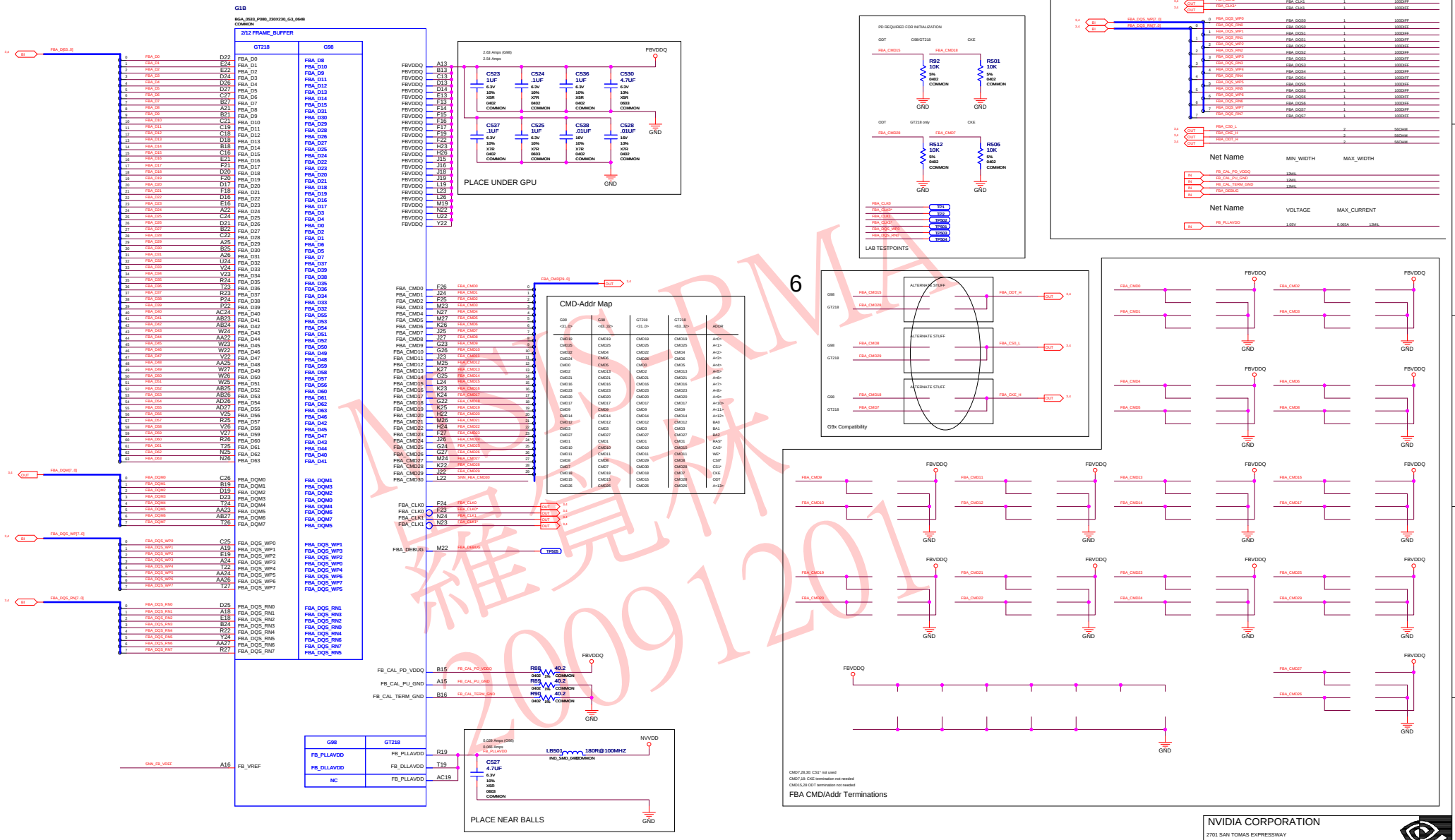
Frame Buffer Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Frame Buffer Interface

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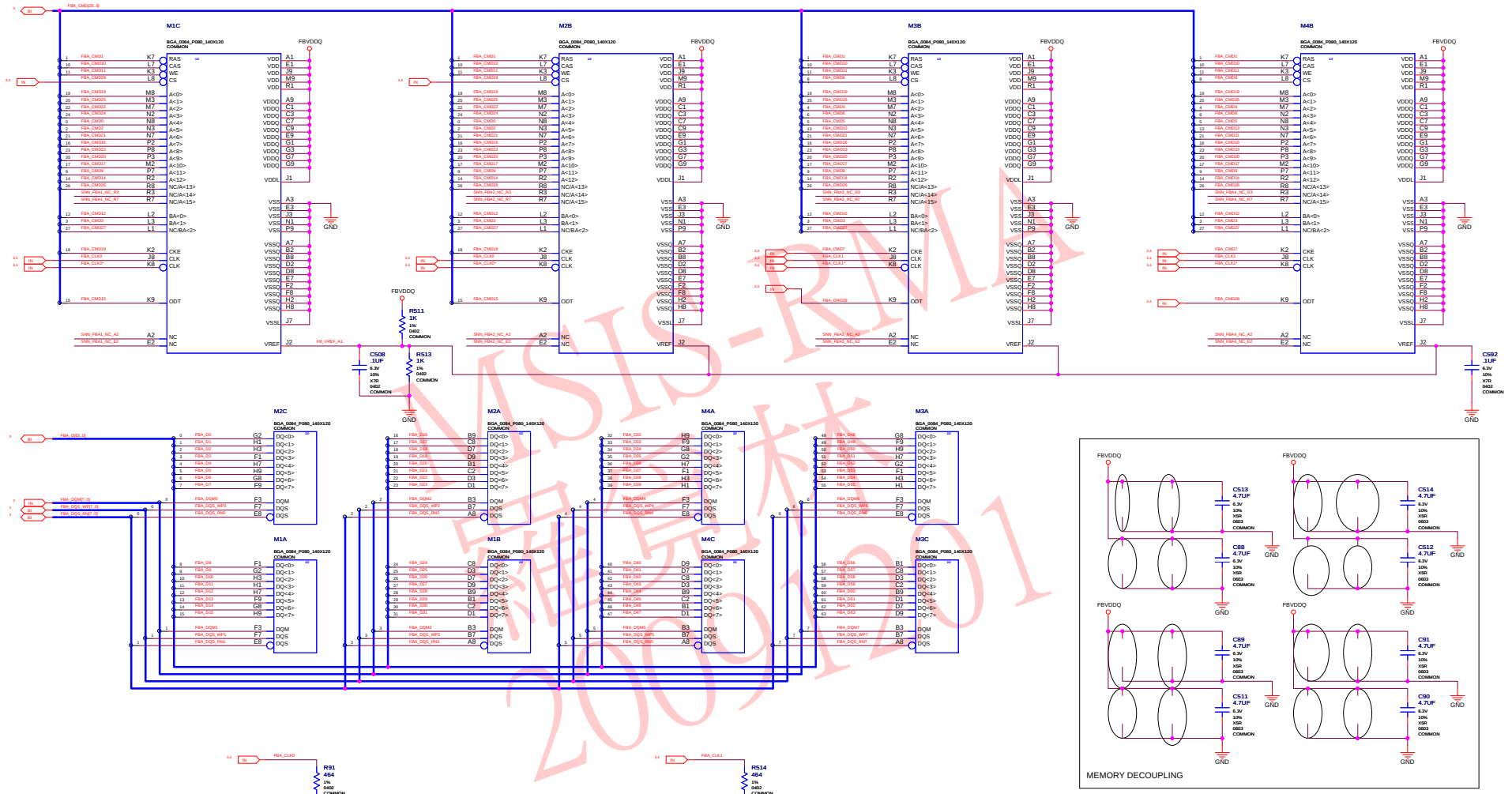
ID		PAGE	
NAME		DATE	05-FEB-2009

DDR2 Memories

Net Name	MIN_WIDTH	MAX_WIDTH
FB_VREF_A	12MIL	



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DDR2 Memories

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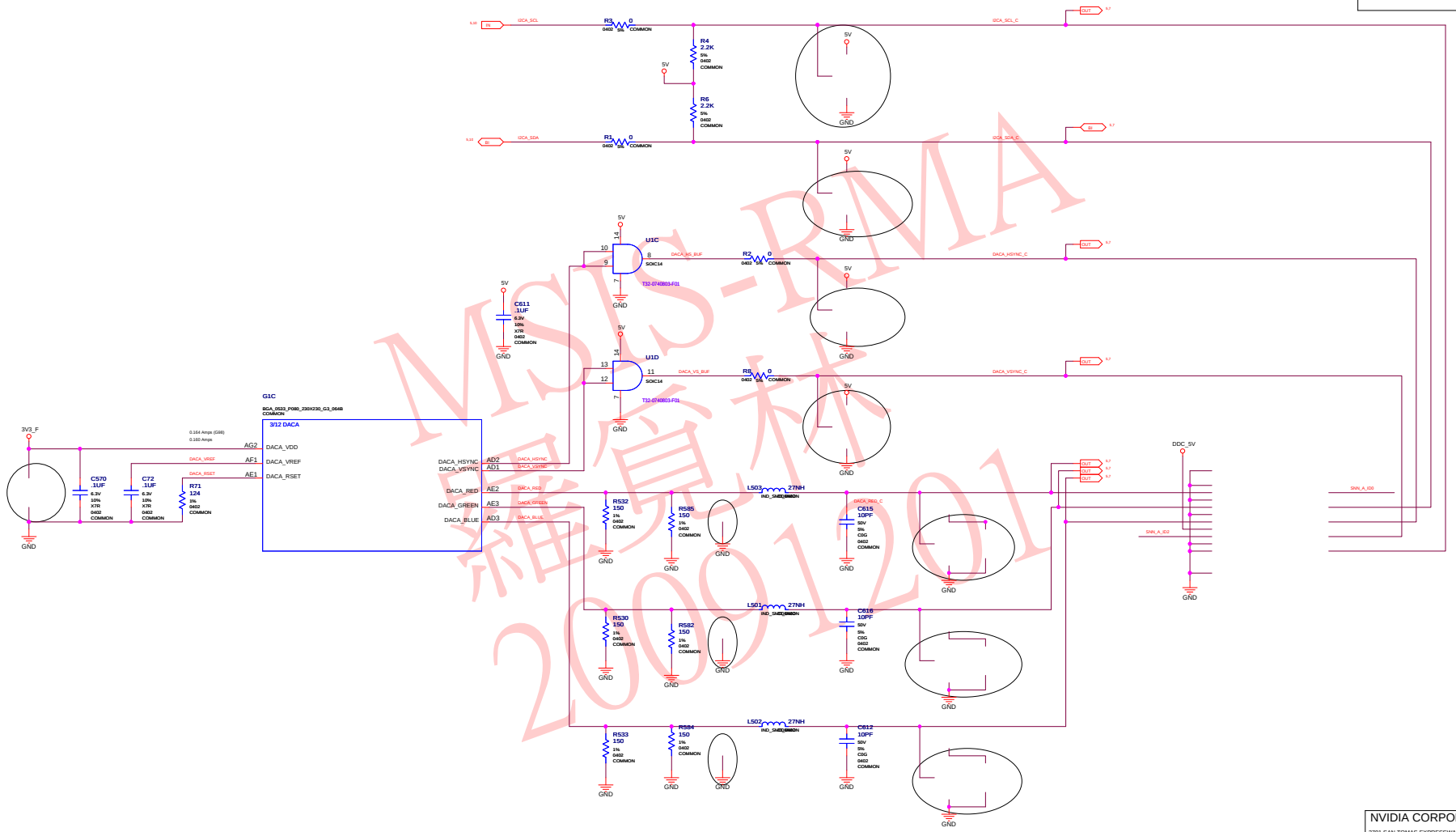
NAME		DATE	05-FEB-2009

DAC A Slim VGA

11

Net Name	CRITICAL	IMPEDANCE
DACA_RED	1	50OHM
DACA_GREEN	1	50OHM
DACA_BLUE	1	50OHM
DACA_RED_C	1	50OHM
DACA_GREEN_C	1	50OHM
DACA_BLUE_C	1	50OHM
DACA_HSYNC	2	50OHM
DACA_VSYNC	2	50OHM
DACA_HS_BUF	2	50OHM
DACA_VS_BUF	2	50OHM
DACA_HSYNC_C	2	50OHM
DACA_VSYNC_C	2	50OHM

Net Name	MIN_WIDTH	MAX_WIDTH
I2CA_SCL		
I2CA_SDA		
I2CA_SCL_C		
I2CA_SDA_C		
DACA_VREF	12MIL	
DACA_RSET	12MIL	



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DAC A Slim VGA

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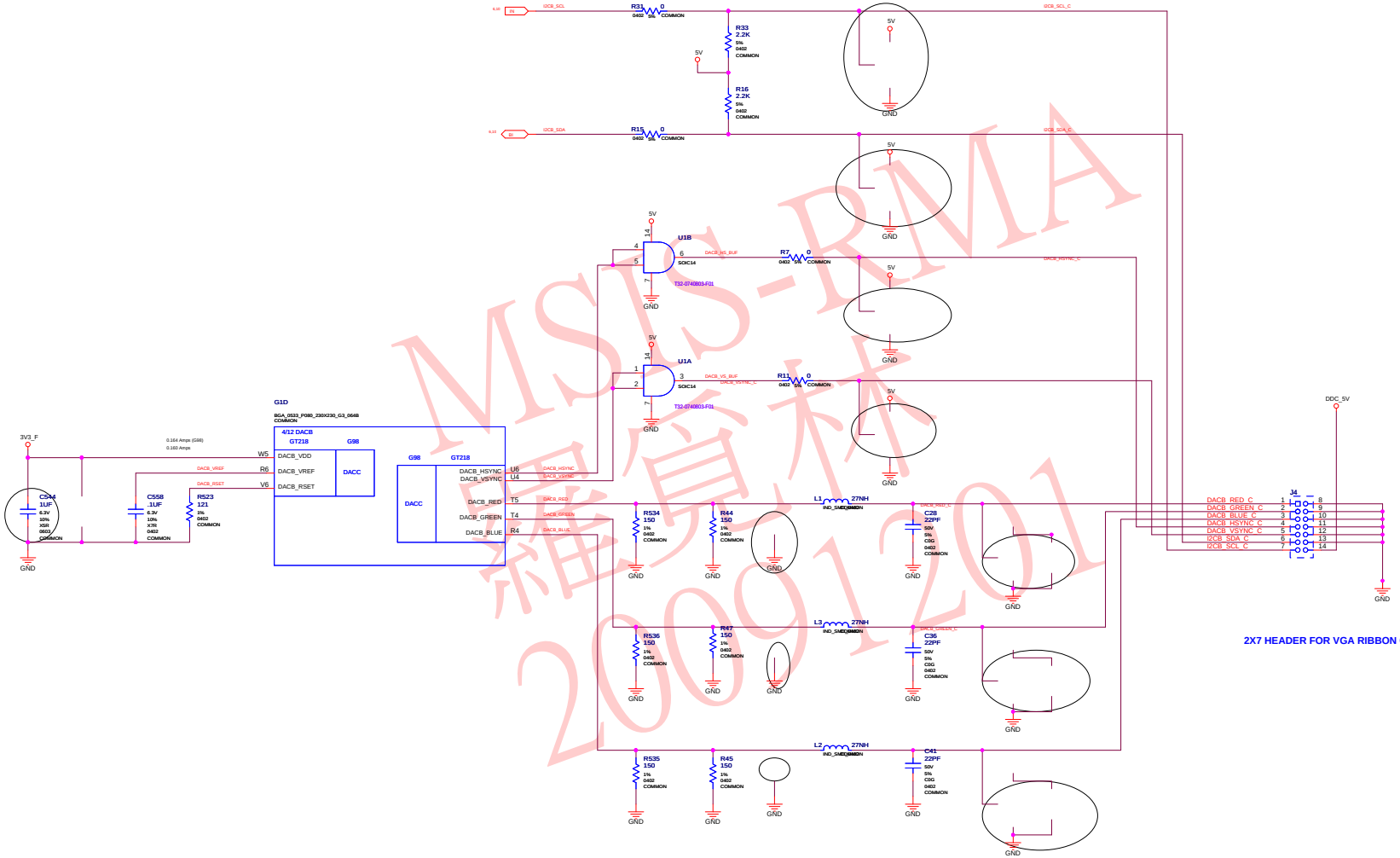
ID		PAGE	
NAME		DATE	05-FEB-2009

DAC B VGA Header

Net Name	CRITICAL	IMPEDANCE
DACB_RED	1	50OHM
DACB_GREEN	1	50OHM
DACB_BLUE	1	50OHM
DACB_RED_C	1	50OHM
DACB_GREEN_C	1	50OHM
DACB_BLUE_C	1	50OHM
DACB_HSYNC	2	50OHM
DACB_VSYNC	2	50OHM
DACB_HSYNC_C	2	50OHM
DACB_VSYNC_C	2	50OHM
DACB_HS_BUF	2	50OHM
DACB_VS_BUF	2	50OHM

Net Name	MIN_WIDTH	MAX_WIDTH
I2CB_SCL		
I2CB_SDA		
I2CB_SCL_C		
I2CB_SDA_C		
DACB_VREF	12MIL	
DACB_RSET	12MIL	

11



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DAC B VGA Header

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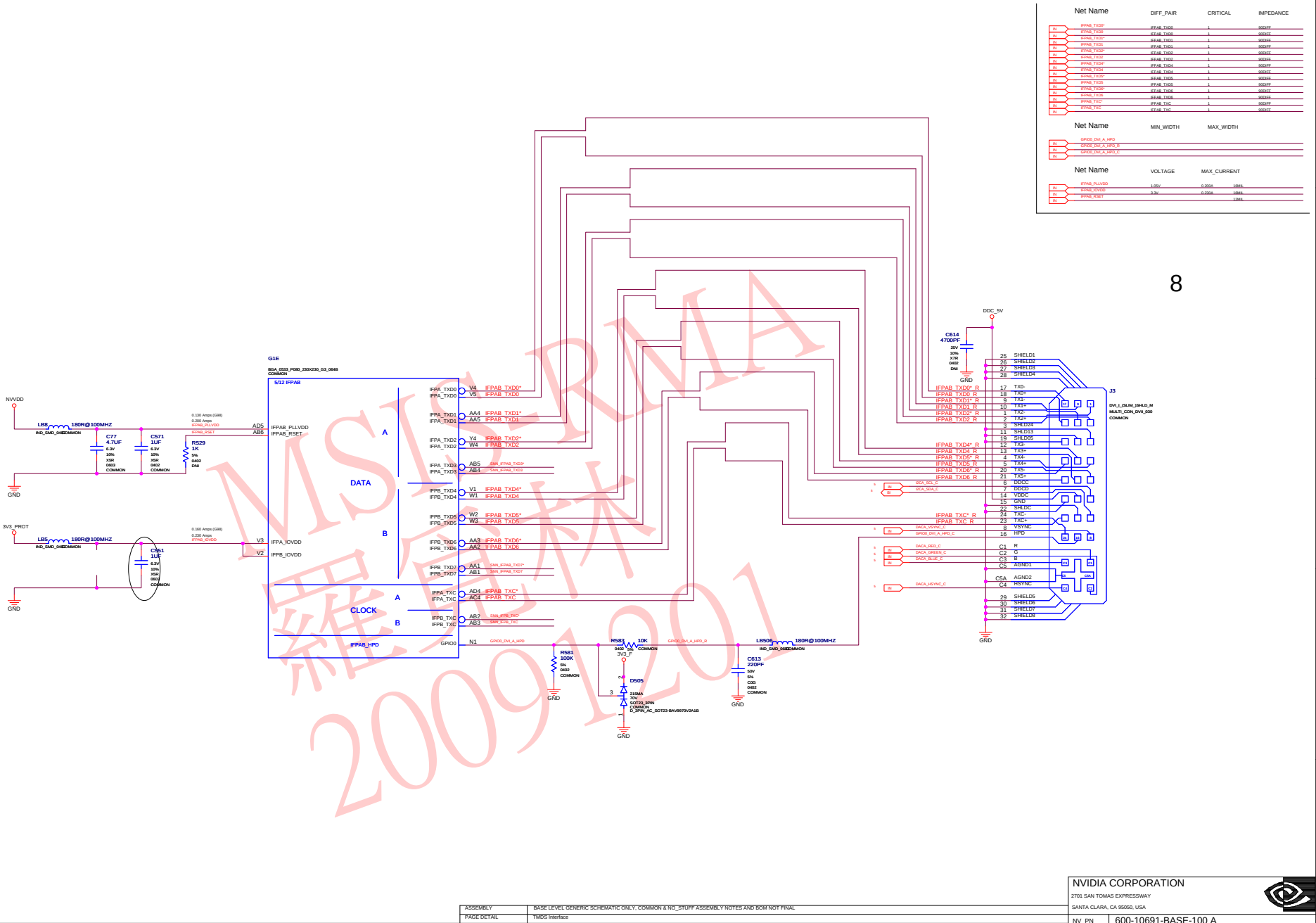
ID		PAGE	
NAME		DATE	05-FEB-2009

TMDS Interface



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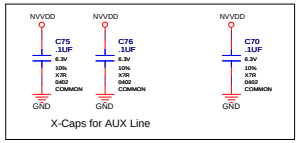
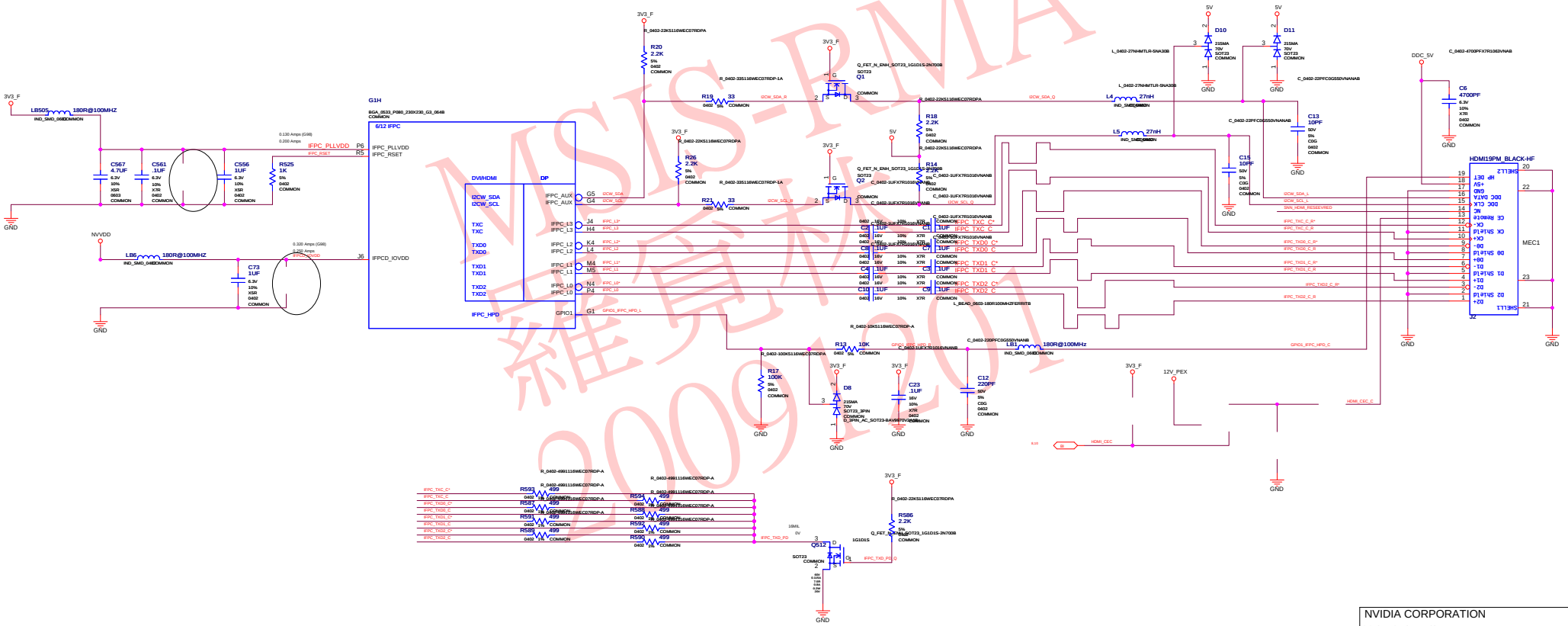
HDMI Connector

6





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PAGE DETAIL	DisplayPort Connector

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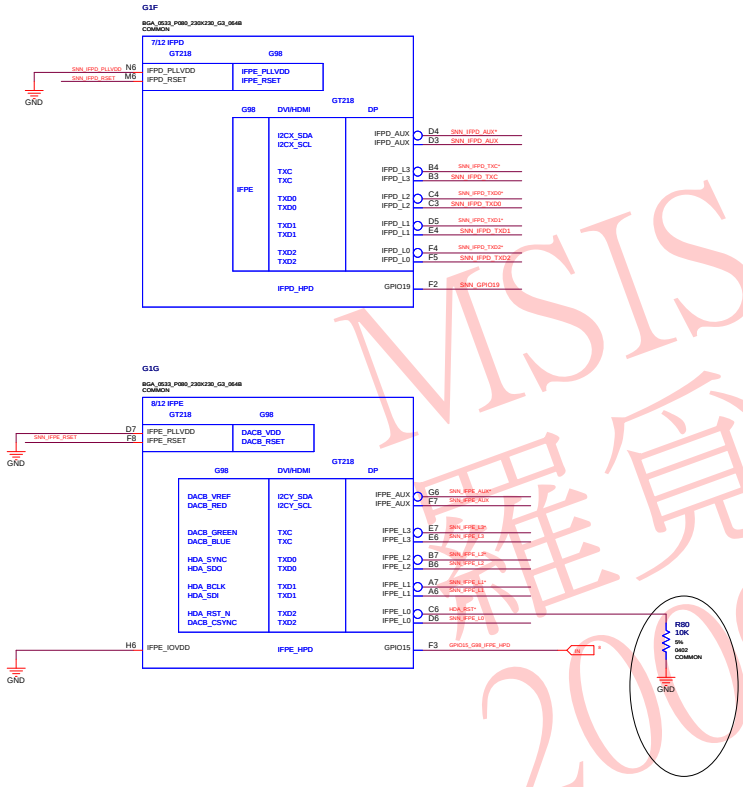
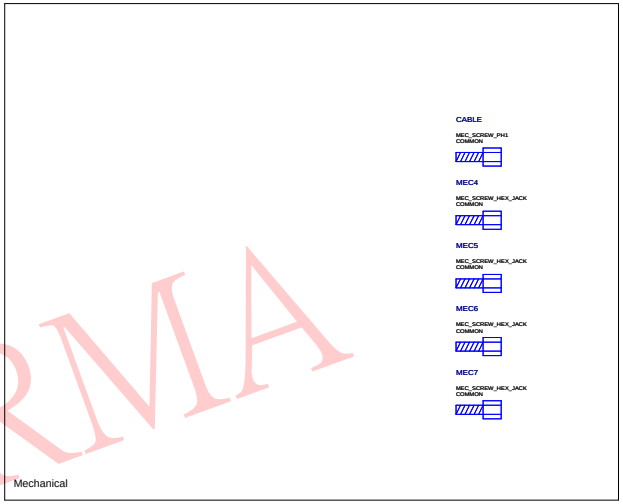
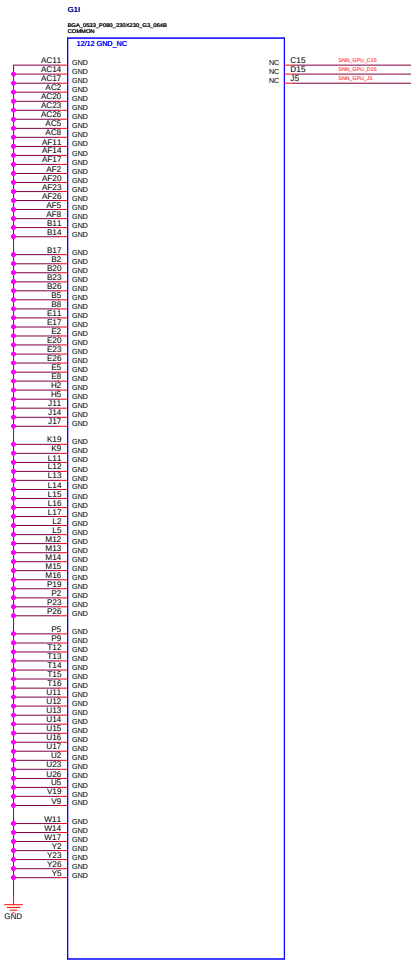
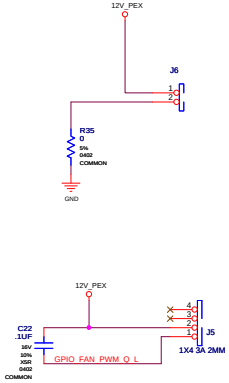
NAME		DATE	05-FEB-2009

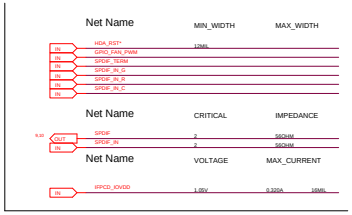
IFPC, IFPE Interface, Mechanical, SPDIF











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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPC, IFPE Interface, Mechanical, SPDIF

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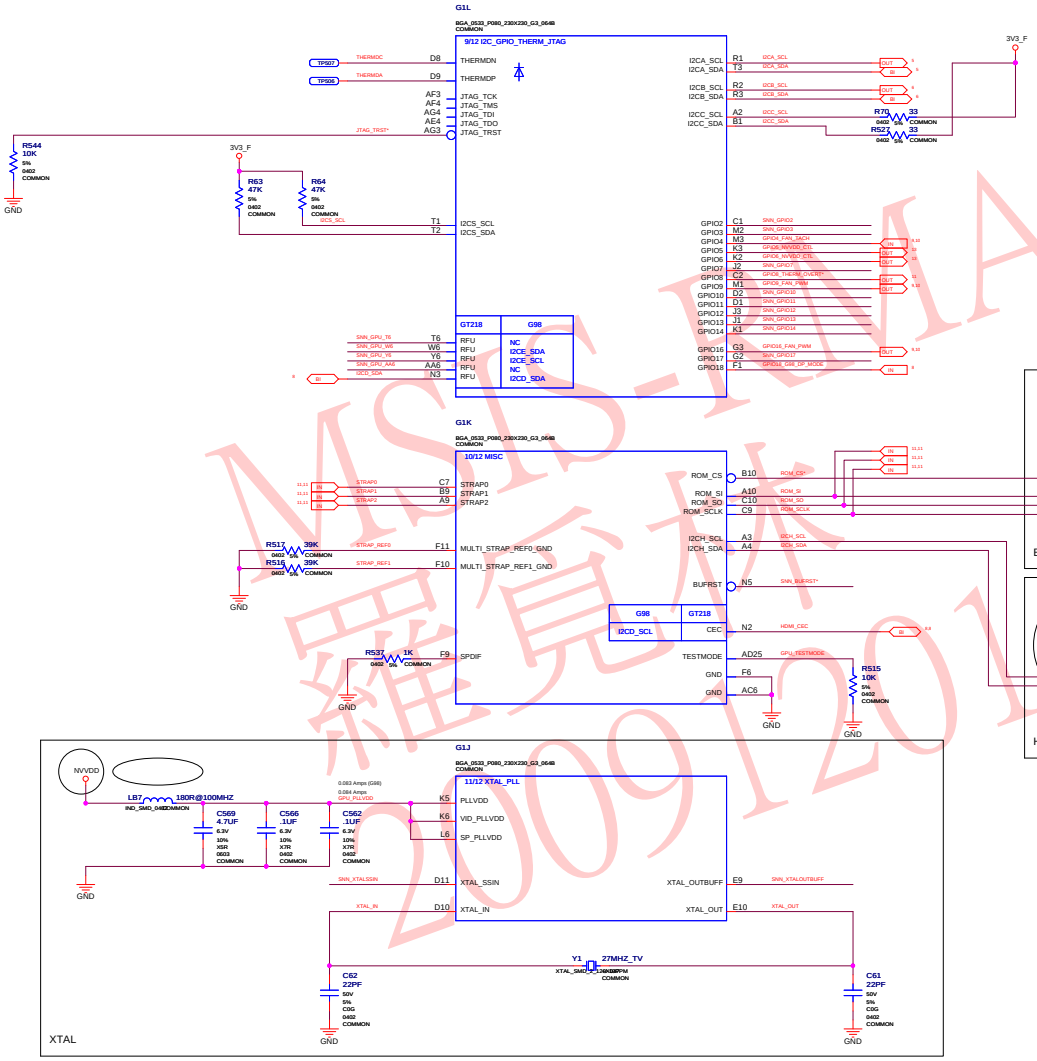
ID		PAGE	
NAME		DATE	05-FEB-2009

XTAL, ROM, JTAG



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Net Name	CRITICAL	IMPEDANCE
XTAL_OUT	1	50OHM
XTAL_IN	1	50OHM

Net Name	VOLTAGE	MAX_CURRENT
GPU_PLLVDD	1.05V	0.083A

Net Name	MIN_WIDTH	MAX_WIDTH
PEX_SMCLK		
PEX_SMDAT		
PEX_TCLK		
PEX_TMS		
PEX_TDI		
PEX_TDO		
GPIO8_FAN_TACH		
GPIO9_FAN_PWM		
GPIO16_FAN_PWM		

Net Name	MIN_WIDTH	MAX_WIDTH
I2CC_SCL		
I2CC_SDA		
I2CC_SCL_R		
I2CC_SDA_R		
I2CC_SCL_Q		
I2CC_SDA_Q		
I2CH_SCL		
I2CH_SDA		
I2CS_SCL		
I2CS_SDA		
ROM_CS*		
GPU_TESTMODE		
VID_PLLVDD		
THERMDC	12MIL	
THERMDA	12MIL	
JTAG_TCLK		
JTAG_TMS		
JTAG_TDI		
JTAG_TDO		
JTAG_TRST*		

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, ROM, JTAG

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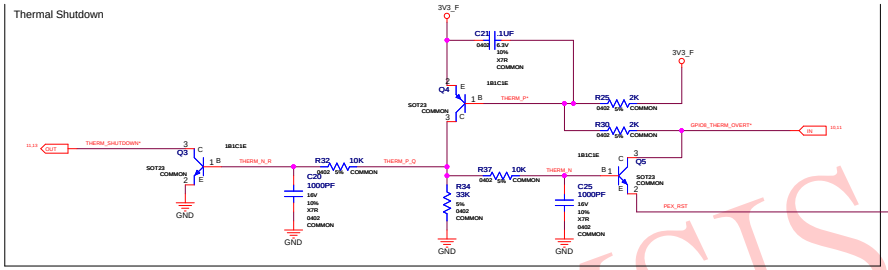
Thermal Protection, Protected 3V3, Straps

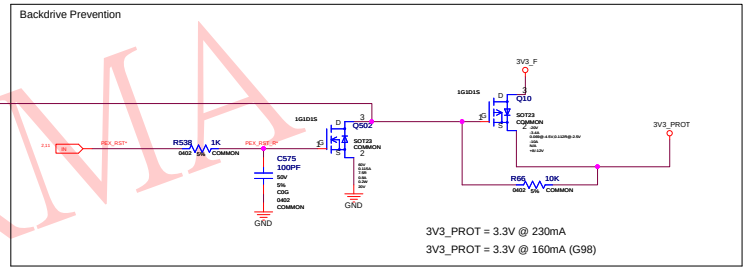
Net Name	MIN_WIDTH	MAX_WIDTH
PEX_RST		
PEX_RST_R*		
PEX_RST*		
GPIO8_THERM_OVERT*		
THERM_N_R		
THERM_P_Q		
THERM_P*		
THERM_N		
THERM_SHUTDOWN*		
ROM_SI		
ROM_SO		
ROM_SCLK		
STRAP2		
STRAP1		
STRAP0		

Net Name	VOLTAGE	MAX_CURRENT
3V3_PROT	3.3V	0.23A

Thermal Shutdown



Backdrive Prevention



GT218 Straps MLS Mode

Bit	Signal	Values			
03:	RAMCFG[3]	0000	Elpida		
		0001	Samsung, Micron		
02:	RAMCFG[2]	0010	Qimonda		
		0011	Hynix		
01:	RAMCFG[1]	0100	Nanya		
00:	RAMCFG[0]				
03:	XCLK_417	0	277 (Default)		
02:	FB[0]	0	256M (Default)		
01:	SMB_ALT_ADDR	0	0x6C		
		1	0x6C		
00:	VGA_DEVICE	0	Class code 302		
		1	Class code 300		
03:	PCI_DEVID_EXT	0	GT218-300-A1		
02:	SUB_VENDOR	0	No BIOS		
		1	BIOS		
01:	SLOT_CLK_CFG	0	Disable		
		1	Enable		
00:	PEX_PLL_EN_TERM100	0	Disable		
		1	Enable		
03:	PCI_DEVID[3]	0000	GT218-300-A1		
02:	PCI_DEVID[2]				
01:	PCI_DEVID[1]				
00:	PCI_DEVID[0]				
03:	3GIO_PADCFG_LUT_ADR[3]	0000	DSKTOP_DEFAULT	1000	DSKTOP_HTHRS
		0001	MOBILE_DEFAULT	1001	MOBILE_HTHRS_NAMP
02:	3GIO_PADCFG_LUT_ADR[2]	0010	MOBILE_NTHRS_LLAMP	1010	MOBILE_HTHRS_LLAMP
		0011	MOBILE_NTHRS_LAMP	1011	MOBILE_HTHRS_LAMP
01:	3GIO_PADCFG_LUT_ADR[1]	0100	MOBILE_NTHRS_HAMP	1100	MOBILE_HTHRS_HAMP
		0101	MOBILE_NTHRS_HHAMP	1101	MOBILE_HTHRS_HHAMP
00:	3GIO_PADCFG_LUT_ADR[0]	0110	MOBILE_NTHRS_HHHAMP	1110	MOBILE_HTHRS_HHHAMP
		0111	MOBILE_NTHRS_HHHHAMP	1111	MOBILE_HTHRS_HHHHAMP
03:	USER[3]	0000	Default		
02:	USER[2]				
01:	USER[1]				
00:	USER[0]				

Multilevel Straps

5K to GND	0000
10K to GND	0001
15K to GND	0010
20K to GND	0011
25K to GND	0100
30K to GND	0101
35K to GND	0110
45K to GND	0111
5K to VCC	1000
10K to VCC	1001
15K to VCC	1010
20K to VCC	1011
25K to VCC	1100
30K to VCC	1101
35K to VCC	1110
45K to VCC	1111

GT218 Straps BU Mode

Bit	Signal	Values	
PCI_DEVID_EXT		0	GT218-300-A1
XCLK_417		0	277 (Default)
3GIO_PADCFG_LUT_ADR[3]		0000	DSKTOP_DEFAULT
		0001	MOBILE_DEFAULT
		0010	MOBILE_NTHRS_LLAMP
		0011	MOBILE_NTHRS_LAMP
		0100	MOBILE_NTHRS_HAMP
		0101	MOBILE_NTHRS_HHAMP
		0110	MOBILE_NTHRS_HHHAMP
		0111	MOBILE_NTHRS_HHHHAMP
		1000	DSKTOP_HTHRS
		1001	MOBILE_HTHRS_NAMP
		1010	MOBILE_HTHRS_LLAMP
		1011	MOBILE_HTHRS_LAMP
		1100	MOBILE_HTHRS_HAMP
		1101	MOBILE_HTHRS_HHAMP
		1110	MOBILE_HTHRS_HHHAMP
		1111	MOBILE_HTHRS_HHHHAMP
3GIO_PADCFG_LUT_ADR[2]			
3GIO_PADCFG_LUT_ADR[1]			
3GIO_PADCFG_LUT_ADR[0]			

GT218 Straps PM Mode

Bit	Signal	Values	
PCI_DEVID_EXT		0	GT218-300-A1
XCLK_417		0	277/277 OR 417/417
PCI_DEVID[3]		0	GT218-300-A1
RAMCFG[3]		0000	Elpida
		0001	Samsung, Micron
		0010	Qimonda
		0011	Hynix
		0100	Nanya
RAMCFG[1]			
RAMCFG[0]			

Mode	REF0/REF1
MLS	Stuff
BU	No stuff
PM	Stuff one

G98 Straps MLS Mode

Bit	Signal	Values	
03:	RAMCFG[3]	0000	Elpida
		0100	Nanya
02:	RAMCFG[2]	0101	Samsung
		0110	Qimonda
01:	RAMCFG[1]	0111	Hynix
00:	RAMCFG[0]		
03:	XCLK_277	1	Enabled
02:	TVMODE[2]	001	NTSC_J
01:	TVMODE[1]		
00:	TVMODE[0]		
03:	PCI_DEVID_EXT	0	G98-409-U2
			G98-400-A2
			G98-400-U2
02:	SUB_VENDOR	1	BIOS
01:	SLOT_CLK_CFG	0	Disable
		1	Enable
00:	PEX_PLL_EN_TERM100	0	Disable
03:	PCI_DEVID[3]	0000	RFU
02:	PCI_DEVID[2]	0100	G98-409-U2
		0100	G98-400-A2
01:	PCI_DEVID[1]	0100	G98-400-U2
00:	PCI_DEVID[0]		
03:	3GIO_PADCFG_LUT_ADR[3]	0000	DSKTOP_DEFAULT
02:	3GIO_PADCFG_LUT_ADR[2]		
01:	3GIO_PADCFG_LUT_ADR[1]		
00:	3GIO_PADCFG_LUT_ADR[0]		
03:	USER[3]	0000	Default
02:	USER[2]		
01:	USER[1]		
00:	USER[0]		

Multilevel Straps

5K to GND	0000
10K to GND	0001
15K to GND	0010
20K to GND	0011
25K to GND	0100
30K to GND	0101
35K to GND	0110
45K to GND	0111
5K to VCC	1000
10K to VCC	1001
15K to VCC	1010
20K to VCC	1011
25K to VCC	1100
30K to VCC	1101
35K to VCC	1110
45K to VCC	1111

VSIS-RMA 羅宣林 20091001

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Protection, Protected 3V3, Straps

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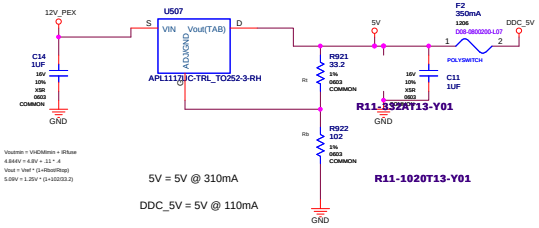
NV_PN	600-10691-BASE-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

Power Supply I: FBVDD/Q, PEX_VDD, 5V, 3V3_F

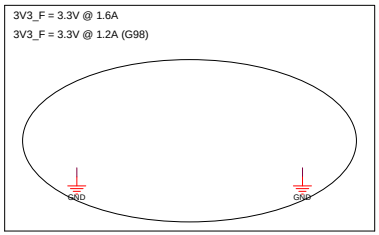
8

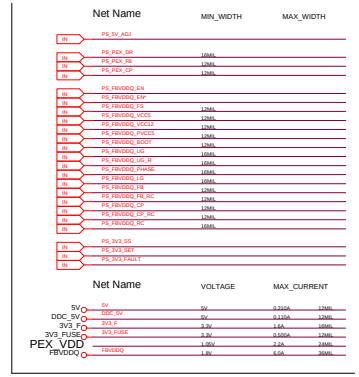


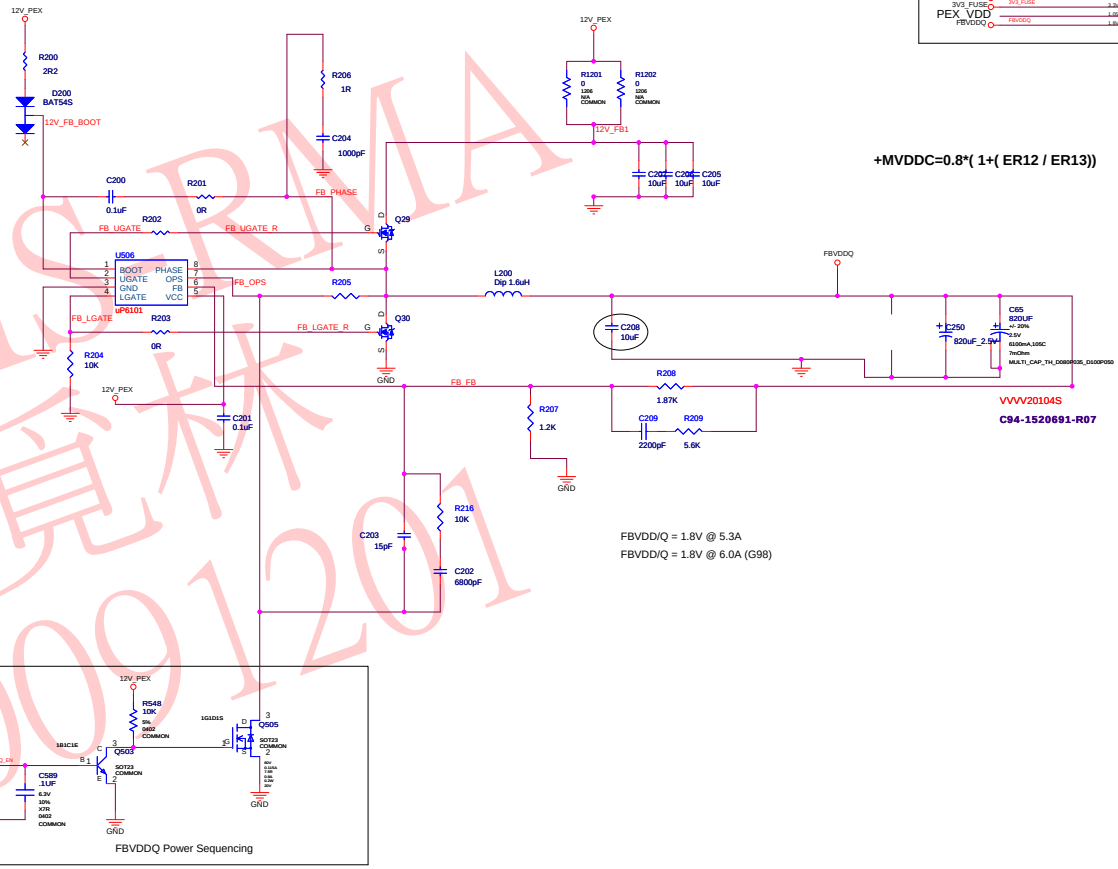
5V = 5V @ 310mA

DDC_5V = 5V @ 110mA

R11-1020T13-Y01







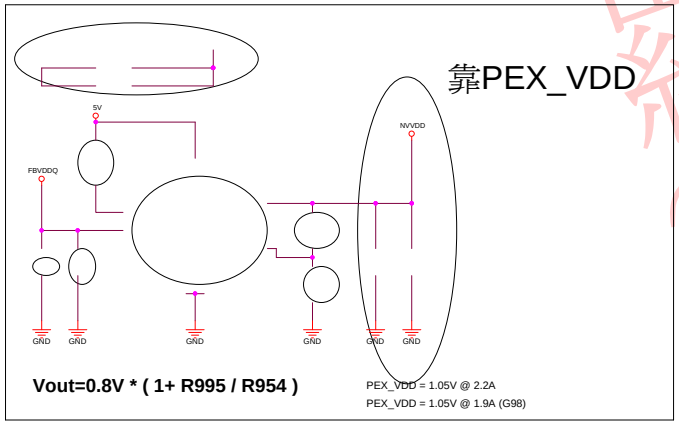
+MVDDC=0.8*(1+(ER12 / ER13))

VVVV20104S

C94-1520691-R07

FBVDDQ = 1.8V @ 5.3A

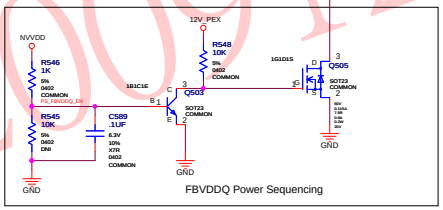
FBVDDQ = 1.8V @ 6.0A (G98)



Vout=0.8V * (1+ R995 / R954)

PEX_VDD = 1.05V @ 2.2A

PEX_VDD = 1.05V @ 1.9A (G98)



FBVDDQ Power Sequencing

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply I: FBVDDQ, PEX_VDD, 5V, 3V3_F

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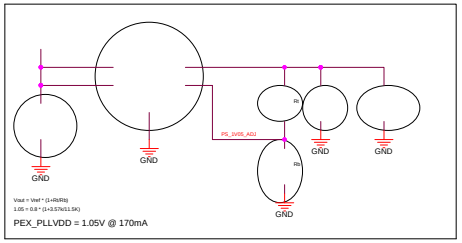
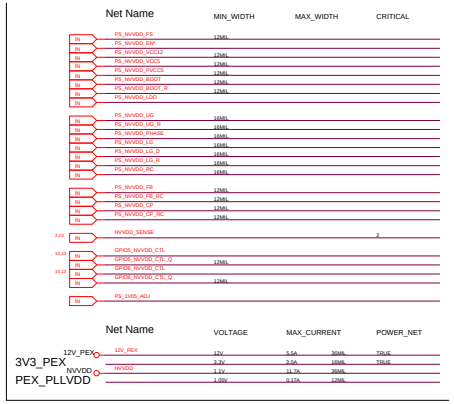
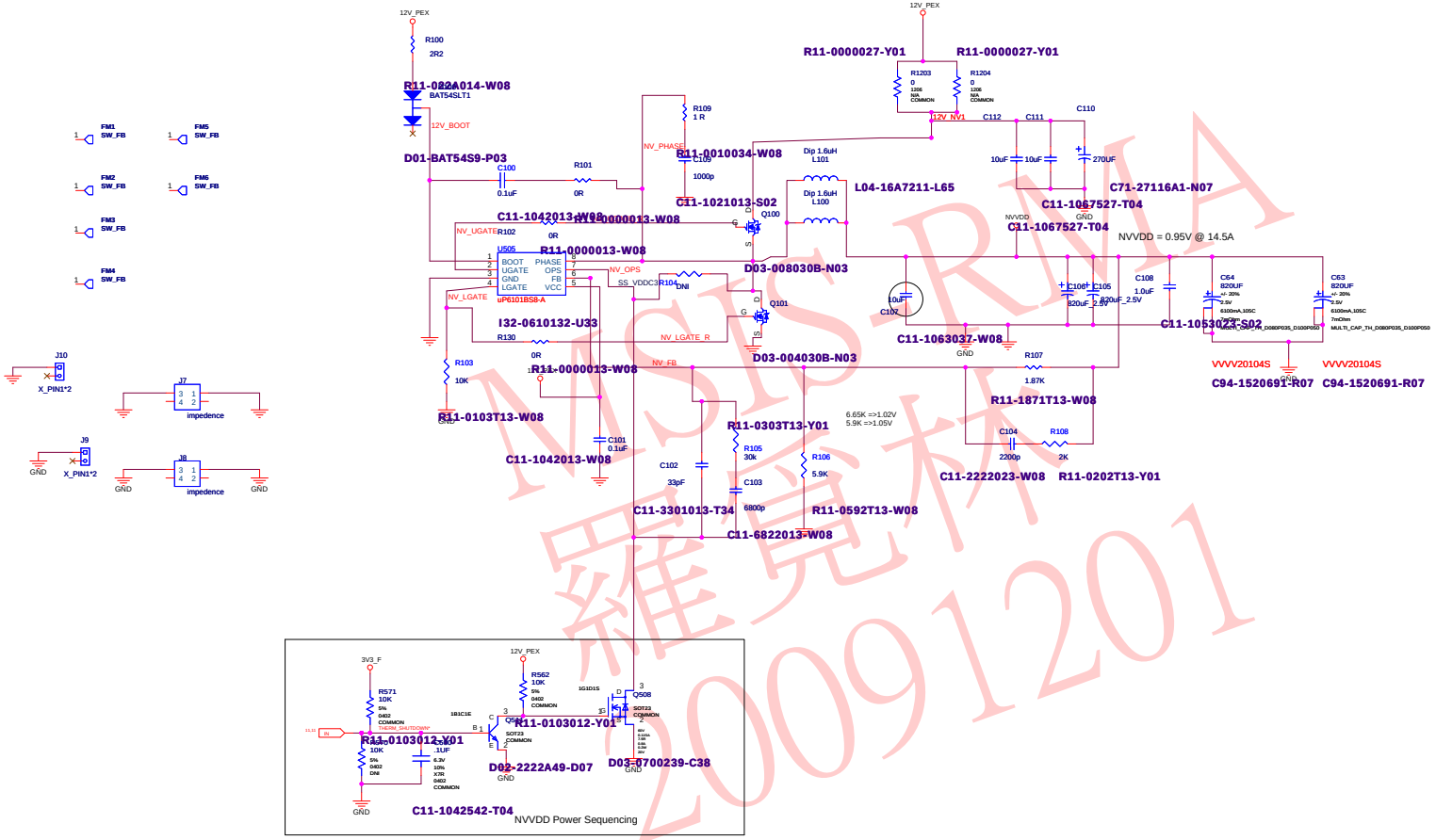
NV_PN	600-10691-BASE-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

Power Supply II: PEX_PLLVDD, NVVDD

6







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20091201

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SANTA CLARA, CA 95050, USA

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply II: PEX_PLLVDD, NVVDD

NV_PN	600-10691-BASE-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

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Title: Baseset Report
Design: p691_a01
Date: Jan 27 23:02:52 2009

Base nets and synonyms for
p691_a01_lib.P691_A01(@p691_a01_lib.p691
_a01(sch_1))
Base Signal Location([Zone][dir])

3V3_F 12.2H
3V3_FUSE 12.2H
3V3_PEX 13.2G
3V3_PROT 11.1H
5V 12.2H
12V_PEX 13.2G
DACA_BLUE 5.1G< 5.4C
DACA_BLUE_C 5.1G> 5.4F> 7.3F<
DACA_GREEN 5.1G< 5.4C
DACA_GREEN_C 5.1G> 5.4F> 7.3F<
DACA_HSYNC 5.1G< 5.4C
DACA_HSYNC_C 5.1G> 5.3F> 7.4F<
DACA_HS_BUF 5.1G< 5.3D
DACA_RED 5.1G< 5.4C
DACA_RED_C 5.1G> 5.4F> 7.3F<
DACA_RSET 5.1G< 5.4B
DACA_VREF 5.1G< 5.4B
DACA_VSYNC 5.1G< 5.4C
DACA_VSYNC_C 5.1G> 5.3F> 7.3F<
DACA_VS_BUF 5.1G< 5.3D
DACB_BLUE 6.1G< 6.4C
DACB_BLUE_C 6.1G< 6.5E
DACB_GREEN 6.1G< 6.4C
DACB_GREEN_C 6.1G< 6.4E
DACB_HSYNC 6.1G< 6.4C
DACB_HSYNC_C 6.1G< 6.3E
DACB_HS_BUF 6.1G< 6.3D
DACB_RED 6.1G< 6.4C
DACB_RED_C 6.1G< 6.4E
DACB_RSET 6.1G< 6.4B
DACB_VREF 6.1G< 6.4B
DACB_VSYNC 6.1G< 6.4C
DACB_VSYNC_C 6.1G< 6.3E
DACB_VS_BUF 6.1G< 6.3D
DDC_5V 12.2H
DP_MODE* 8.1F< 8.2G
DP_MODE_C 8.1F< 8.3H
FBA_CKE_H 3.2G> 3.3F> 4.2D<
4.2F<
FBA_CLK0 3.1G> 3.2E 3.4D>
4.2A< 4.2C< 4.5B<
FBA_CLK0* 3.1G> 3.2E 3.4D>
4.2A< 4.2C< 4.5B<
FBA_CLK1 3.1G> 3.2E 3.4D>
4.2D< 4.2F< 4.5D<
FBA_CLK1* 3.1G> 3.2E 3.4D>
4.2D< 4.2F< 4.5D<
FBA_CMD<0> 3.2C 3.2G 4.2A 4.2C
FBA_CMD<29..0> 3.1G> 3.2D> 4.1A<>
FBA_CMD<1> 3.2C 3.2G 4.1A 4.1C
4.1E 4.1G
FBA_CMD<2> 3.2C 3.2H 4.2A 4.2C
FBA_CMD<3> 3.2C 3.2H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<4> 3.2C 3.3G 4.2E 4.2G
FBA_CMD<5> 3.3C 3.3G 4.2E 4.2G
FBA_CMD<6> 3.3C 3.3H 4.2E 4.2G
FBA_CMD<7> 3.2F 3.3C 3.3E
FBA_CMD<8> 3.3C 3.3E 3.3H 4.2E
4.2G
FBA_CMD<9> 3.3C 3.3E 4.2A 4.2C
4.2E 4.2G
FBA_CMD<10> 3.3C 3.3E 4.1A 4.1C
4.1E 4.1G
FBA_CMD<11> 3.3C 3.3F 4.1A 4.1C
4.1E 4.1G
FBA_CMD<12> 3.3C 3.3F 4.2A 4.2C
4.2E 4.2G
FBA_CMD<13> 3.3C 3.3G 4.2E 4.2G
FBA_CMD<14> 3.3C 3.3G 4.2A 4.2C
4.2E 4.2G
FBA_CMD<15> 3.1E 3.2E 3.3C 4.3A
4.3C
FBA_CMD<16> 3.3C 3.3H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<17> 3.3C 3.3H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<18> 3.1F 3.3C 3.3E 4.2A
4.2C
FBA_CMD<19> 3.3C 3.4E 4.2A 4.2C
4.2E 4.2G
FBA_CMD<20> 3.3C 3.4E 4.2A 4.2C
4.2E 4.2G
FBA_CMD<21> 3.3C 3.4F 4.2A 4.2C
4.2E 4.2G
FBA_CMD<22> 3.3C 3.4F 4.2A 4.2C
FBA_CMD<23> 3.3C 3.4G 4.2A 4.2C
4.2E 4.2G
FBA_CMD<24> 3.3C 3.4G 4.2A 4.2C
FBA_CMD<25> 3.3C 3.4H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<26> 3.3C 3.4H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<27> 3.3C 3.4H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<28> 3.2E 3.2E 3.3C
FBA_CMD<29> 3.3C 3.3E 3.4H
FBA_CSD_L 3.2G> 3.3F> 4.2A<
4.2C<
FBA_D<0> 3.1B 4.3B
FBA_D<63..0> 3.1A<> 3.1G<> 4.3A<>
FBA_D<1> 3.1B 4.3B
FBA_D<2> 3.1B 4.3B
FBA_D<3> 3.1B 4.3B
FBA_D<4> 3.1B 4.3B
FBA_D<5> 3.1B 4.3B
FBA_D<6> 3.1B 4.3B
FBA_D<7> 3.1B 4.3B
FBA_D<8> 3.1B 4.4B
FBA_D<9> 3.1B 4.4B
FBA_D<10> 3.1B 4.4B
FBA_D<11> 3.2B 4.4B
FBA_D<12> 3.2B 4.4B
FBA_D<13> 3.2B 4.4B
FBA_D<14> 3.2B 4.4B
FBA_D<15> 3.2B 4.4B
FBA_D<16> 3.2B 4.3C
FBA_D<17> 3.2B 4.3C
FBA_D<18> 3.2B 4.3C
FBA_D<19> 3.2B 4.3C
FBA_D<20> 3.2B 4.3C
FBA_D<21> 3.2B 4.3C
FBA_D<22> 3.2B 4.3C
FBA_D<23> 3.2B 4.3C
FBA_D<24> 3.2B 4.4C
FBA_D<25> 3.2B 4.4C
FBA_D<26> 3.2B 4.4C
FBA_D<27> 3.2B 4.4C
FBA_D<28> 3.2B 4.4C
FBA_D<29> 3.2B 4.4C
FBA_D<30> 3.2B 4.4C
FBA_D<31> 3.2B 4.4C
FBA_D<32> 3.2B 4.3D
FBA_D<33> 3.2B 4.3D
FBA_D<34> 3.2B 4.3D
FBA_D<35> 3.2B 4.3D
FBA_D<36> 3.2B 4.3D
FBA_D<37> 3.2B 4.3D
FBA_D<38> 3.2B 4.3D
FBA_D<39> 3.2B 4.3D
FBA_D<40> 3.2B 4.4D
FBA_D<41> 3.3B 4.4D
FBA_D<42> 3.3B 4.4D
FBA_D<43> 3.3B 4.4D
FBA_D<44> 3.3B 4.4D
FBA_D<45> 3.3B 4.4D
FBA_D<46> 3.3B 4.4D
FBA_D<47> 3.3B 4.4D
FBA_D<48> 3.3B 4.3E
FBA_D<49> 3.3B 4.3E
FBA_D<50> 3.3B 4.3E
FBA_D<51> 3.3B 4.3E
FBA_D<52> 3.3B 4.3E
FBA_D<53> 3.3B 4.3E
FBA_D<54> 3.3B 4.3E
FBA_D<55> 3.3B 4.3E
FBA_D<56> 3.3B 4.4E
FBA_D<57> 3.3B 4.4E
FBA_D<58> 3.3B 4.4E
FBA_D<59> 3.3B 4.4E
FBA_D<60> 3.3B 4.4E
FBA_D<61> 3.3B 4.4E
FBA_D<62> 3.3B 4.4E
FBA_D<63> 3.3B 4.4E
FBA_DEBUG 3.2G< 3.4C
FBA_DQM<0> 3.3B 4.3B
FBA_DQM<7..0> 3.1G> 3.3A> 4.4A<
FBA_DQM<1> 3.3B 4.4B
FBA_DQM<2> 3.3B 4.3C
FBA_DQM<3> 3.3B 4.4C
FBA_DQM<4> 3.3B 4.3D
FBA_DQM<5> 3.4B 4.4D
FBA_DQM<6> 3.4B 4.3E
FBA_DQM<7> 3.4B 4.4E
FBA_DQS_RN<0> 3.1G 3.2E 3.4B 4.4B
FBA_DQS_RN<7..0> 3.1G<> 3.4A<> 4.4A<>
FBA_DQS_RN<1> 3.1G 3.4B 4.4B
FBA_DQS_RN<2> 3.1G 3.4B 4.4C
FBA_DQS_RN<3> 3.1G 3.4B 4.4C
FBA_DQS_RN<4> 3.1G 3.4B 4.4D
FBA_DQS_RN<5> 3.1G 3.4B 4.4D
FBA_DQS_RN<6> 3.1G 3.4B 4.4E
FBA_DQS_RN<7> 3.1G 3.4B 4.4E
FBA_DQS_WP<0> 3.1G 3.2E 3.4B 4.4B
FBA_DQS_WP<7..0> 3.1G<> 3.4A<> 4.4A<>
FBA_DQS_WP<1> 3.1G 3.4B 4.4B
FBA_DQS_WP<2> 3.1G 3.4B 4.4C
FBA_DQS_WP<3> 3.1G 3.4B 4.4C
FBA_DQS_WP<4> 3.1G 3.4B 4.4D
FBA_DQS_WP<5> 3.1G 3.4B 4.4D
FBA_DQS_WP<6> 3.1G 3.4B 4.4E
FBA_DQS_WP<7> 3.1G 3.4B 4.4E
FBA_ODT_H 3.2F> 3.2G> 4.3D<
4.3F<
FBVDDQ 12.2H
FB_CAL_PD_VDDQ 3.2G< 3.4C
FB_CAL_PU_GND 3.2G< 3.4C
FB_CAL_TERM_GND 3.2G< 3.4C
FB_PLLAVDD 3.2G< 3.5C
FB_VREF_A 4.1G< 4.3B
GPIO0_DVI_A_HPD 7.1G< 7.4D
GPIO0_DVI_A_HPD_C 7.1G< 7.3F
GPIO0_DVI_A_HPD_R 7.1G< 7.4E
GPIO4_FAN_TACH 9.5D> 10.1F< 10.2E<
GPIO5_NVDD_CTL 10.2E> 13.1G< 13.5D<
GPIO5_NVDD_CTL_Q 13.2G< 13.4E
GPIO6_NVDD_CTL 10.2E> 13.2G< 13.5G<
GPIO6_NVDD_CTL_Q 13.2G< 13.4F
GPIO8_THERM_OVERT* 10.2E> 11.1G< 11.2D<
GPIO9_FAN_PWM 9.5D< 10.1F< 10.2E>
GPIO15_G98_IFPE_HP 8.1F> 8.5C> 9.4D<
D
GPIO16_FAN_PWM 9.5D< 10.1F< 10.3E>
GPIO18_G98_DP_MODE 8.1F> 8.3G> 10.3E<
GPIO19_IFPD_HPD 8.1F< 8.5C
GPIO_DP_HPD 8.1F< 8.5D
GPIO_DP_HPD_C 8.1F< 8.4G
GPIO_DP_HPD_R 8.1F< 8.5E
GPIO_FAN_PWM 9.1G< 9.5E
GPU_PLLVDD 10.1F< 10.4C
GPU_TESTMODE 10.1G< 10.4E
HDA_RST* 9.1G< 9.4C
I2CA_SCL 5.1G< 5.2C< 10.2E>
I2CA_SCL_C 5.1F> 5.1G> 7.3F<
I2CA_SDA 5.1G<> 5.2C<> 10.2E<>
I2CA_SDA_C 5.1G<> 5.3F<> 7.3F<>
I2CB_SCL 6.1G< 6.2C< 10.2E>
I2CB_SCL_C 6.1G< 6.2E
I2CB_SDA 6.1G<> 6.2C<> 10.2E<>
I2CB_SDA_C 6.1G< 6.2E
I2CC_SCL 10.1G< 10.2E
I2CC_SCL_Q 10.1G< 10.2G
I2CC_SCL_R 10.1G< 10.2F
I2CC_SDA 10.1G< 10.2E
I2CC_SDA_Q 10.1G< 10.2G
I2CC_SDA_R 10.1G< 10.2F
I2CD_SCL 8.1F< 8.2G< 10.4E>
I2CD_SDA 8.1F<> 8.2G<> 10.3C<>
I2CH_SCL 10.1G< 10.3E
I2CH_SDA 10.1G< 10.3E
I2CS_SCL 10.1G< 10.2C
I2CS_SDA 10.1G< 10.2C
IFPAB_IOVDD 7.2G< 7.3C
IFPAB_PLLVDD 7.2G< 7.3C
IFPAB_RSET 7.2G< 7.3C
IFPAB_TXC 7.1G< 7.4D
IFPAB_TXC* 7.1G< 7.4D
IFPAB_TXD0 7.1G< 7.3D
IFPAB_TXD0* 7.1G< 7.3D
IFPAB_TXD1 7.1G< 7.3D
IFPAB_TXD1* 7.1G< 7.3D
IFPAB_TXD2 7.1G< 7.3D
IFPAB_TXD2* 7.1G< 7.3D
IFPAB_TXD4 7.1G< 7.3D
IFPAB_TXD4* 7.1G< 7.3D
IFPAB_TXD5 7.1G< 7.3D
IFPAB_TXD5* 7.1G< 7.3D
IFPAB_TXD6 7.1G< 7.3D
IFPAB_TXD6* 7.1G< 7.3D
IFPCD_IOVDD 9.1G< 9.3B
IFPD_AUX 8.1G< 8.4C
IFPD_AUX* 8.1G< 8.4C
IFPD_AUX_BYP 8.1G< 8.3D
IFPD_AUX_BYP* 8.1G< 8.2D
IFPD_AUX_C 8.1G< 8.4G
IFPD_AUX_C* 8.1G< 8.4G
IFPD_AUX_RC 8.1G< 8.3D
IFPD_AUX_RC* 8.1G< 8.2D
IFPD_AUX_SEL 8.1F< 8.3D
IFPD_L0 8.1G< 8.4C
IFPD_L0* 8.1G< 8.4C
IFPD_L0_C 8.1G< 8.4G
IFPD_L0_C* 8.1G< 8.4G
IFPD_L1 8.1G< 8.4C
IFPD_L1* 8.1G< 8.4C
IFPD_L1_C 8.1G< 8.4G
IFPD_L1_C* 8.1G< 8.4G
IFPD_L2 8.1G< 8.4C
IFPD_L2* 8.1G< 8.4C
IFPD_L2_C 8.1G< 8.4G
IFPD_L2_C* 8.1G< 8.4G
IFPD_L3 8.1G< 8.4C
IFPD_L3* 8.1G< 8.4C
IFPD_L3_C 8.1G< 8.4G
IFPD_L3_C* 8.1G< 8.4G
IFPD_PLLVDD 8.1F< 8.4B
IFPD_RSET 8.1F< 8.4B
IROM_VCC 10.1G< 10.2G
JTAG_TCLK 10.1G< 10.2C
JTAG_TDI 10.1G< 10.2C
JTAG_TDO 10.1G< 10.2C
JTAG_TMS 10.1G< 10.2C
JTAG_TRST* 10.1G< 10.2C
NVVDD 13.2G
NVVDD_SENSE 2.4F> 13.1G< 13.4H<
PEX_CLKREQ* 2.1D 2.1G<
PEX_PLLVDD 13.2G
PEX_PLLVDD_GPU 2.1G< 2.5F
PEX_PRSNT 2.1B 2.1G<
PEX_REFCLK 2.2C 2.5A<
PEX_REFCLK* 2.2C 2.5A<
PEX_RST 11.1G< 11.3C
PEX_RST* 2.2D> 11.1G< 11.2E<
PEX_RST_R* 11.1G< 11.2F
PEX_RX0 2.2C 2.4A<
PEX_RX0* 2.2C 2.4A<
PEX_RX1 2.2C 2.4A<
PEX_RX1* 2.2C 2.4A<
PEX_RX2 2.2C 2.4A<
PEX_RX2* 2.3C 2.4A<
PEX_RX3 2.3C 2.4A<
PEX_RX3* 2.3C 2.4A<
PEX_RX4 2.3C 2.4A<
PEX_RX4* 2.3C 2.4A<
PEX_RX5 2.3C 2.4A<
PEX_RX5* 2.3C 2.4A<
PEX_RX6 2.3C 2.5A<
PEX_RX6* 2.3C 2.5A<
PEX_RX7 2.3C 2.5A<
PEX_RX7* 2.4C 2.5A<
PEX_RX8 2.4C 2.5A<
PEX_RX8* 2.4C 2.5A<
PEX_RX9 2.4C 2.5A<
PEX_RX9* 2.4C 2.5A<
PEX_RX10 2.4C 2.5A<
PEX_RX10* 2.4C 2.5A<
PEX_RX11 2.4C 2.5A<
PEX_RX11* 2.4C 2.5A<
PEX_RX12 2.4C 2.5A<
PEX_RX12* 2.5A< 2.5C
PEX_RX13 2.5A< 2.5C
PEX_RX13* 2.5A< 2.5C
PEX_RX14 2.5A< 2.5C
PEX_RX14* 2.5A< 2.5C
PEX_RX15 2.5A< 2.5C
PEX_RX15* 2.5A< 2.5C
PEX_SMCLK 2.1D> 10.1F< 10.3B<
PEX_SMDAT 2.2D<> 10.1F<>
10.3B<>
PEX_TCLK 2.1D> 10.1F< 10.3A<
PEX_TDI 2.1D> 10.1F< 10.2A<
PEX_TDO 2.1D< 10.1F> 10.2A>
PEX_TERMP 2.1G< 2.5F
PEX_TMS 2.1D> 10.1F< 10.2A<
PEX_TRST* 2.1D> 10.1F< 10.2A<
PEX_TSTCLK_OUT 2.2D 2.5A<
PEX_TSTCLK_OUT* 2.2D 2.5A<
PEX_TX0 2.2A< 2.2D
PEX_TX0* 2.2A< 2.2D
PEX_TX1 2.2A< 2.2D
PEX_TX1* 2.2A< 2.2D
PEX_TX2 2.2A< 2.2D
PEX_TX2* 2.2A< 2.2D
PEX_TX3 2.2A< 2.3D
PEX_TX3* 2.2A< 2.3D
PEX_TX4 2.2A< 2.3D
PEX_TX4* 2.2A< 2.3D
PEX_TX5 2.2A< 2.3D
PEX_TX5* 2.2A< 2.3D
PEX_TX6 2.2A< 2.3D
PEX_TX6* 2.2A< 2.3D
PEX_TX7 2.2A< 2.3D
PEX_TX7* 2.2A< 2.3D
PEX_TX8 2.2A< 2.4D
PEX_TX8* 2.2A< 2.4D
PEX_TX9 2.3A< 2.4D
PEX_TX9* 2.3A< 2.4D
PEX_TX10 2.3A< 2.4D
PEX_TX10* 2.3A< 2.4D
PEX_TX11 2.3A< 2.4D
PEX_TX11* 2.3A< 2.4D
PEX_TX12 2.3A< 2.4D
PEX_TX12* 2.3A< 2.4D
PEX_TX13 2.3A< 2.5D
PEX_TX13* 2.3A< 2.5D
PEX_TX14 2.3A< 2.5D
PEX_TX14* 2.3A< 2.5D
PEX_TX15 2.3A< 2.5D
PEX_TX15* 2.3A< 2.5D
PEX_TX0 2.2C 2.3A<
PEX_TX0* 2.2C 2.3A<
PEX_TX1 2.2C 2.3A<
PEX_TX1* 2.2C 2.3A<
PEX_TX2 2.2C 2.3A<
PEX_TX2* 2.2C 2.3A<
PEX_TX3 2.3A< 2.3C
PEX_TX3* 2.3A< 2.3C
PEX_TX4 2.3A< 2.3C
PEX_TX4* 2.3A< 2.3C
PEX_TX5 2.3A< 2.3C
PEX_TX5* 2.3A< 2.3C
PEX_TX6 2.3A< 2.3C
PEX_TX6* 2.3A< 2.3C
PEX_TX7 2.3A< 2.3C
PEX_TX7* 2.3C 2.4A<
PEX_TX8 2.4A< 2.4C
PEX_TX8* 2.4A< 2.4C
PEX_TX9 2.4A< 2.4C
PEX_TX9* 2.4A< 2.4C
PEX_TX10 2.4A< 2.4C
PEX_TX10* 2.4A< 2.4C
PEX_TX11 2.4A< 2.4C
PEX_TX11* 2.4A< 2.4C
PEX_TX12 2.4A< 2.4C
PEX_TX12* 2.4A< 2.4C
PEX_TX13 2.4A< 2.5C
PEX_TX13* 2.4A< 2.5C
PEX_TX14 2.4A< 2.5C
PEX_TX14* 2.4A< 2.5C
PEX_TX15 2.4A< 2.5C
PEX_TX15* 2.4A< 2.5C
PEX_VDD 12.2H
PS_1V05_ADJ 13.2E 13.2G<
PS_3V3_FAULT 12.2G< 12.3F
PS_3V3_SET 12.1G< 12.3F
PS_3V3_SS 12.1G< 12.3F
PS_5V_ADJ 12.1G< 12.2B
PS_FBVDDQ_BOOT 12.1G< 12.3E
PS_FBVDDQ_CP 12.1G< 12.4E
PS_FBVDDQ_CP_RC 12.1G< 12.4E
PS_FBVDDQ_EN 12.1G< 12.5C
PS_FBVDDQ_EN* 12.1G< 12.5C
PS_FBVDDQ_FB 12.1G< 12.4E
PS_FBVDDQ_FB_RC 12.1G< 12.4G
PS_FBVDDQ_FS 12.1G< 12.4D
PS_FBVDDQ_LG 12.1G< 12.4E
PS_FBVDDQ_PHASE 12.1G< 12.4E
PS_FBVDDQ_PVCCS 12.1G< 12.3E
PS_FBVDDQ_RC 12.1G< 12.4G
PS_FBVDDQ_UG 12.1G< 12.4E
PS_FBVDDQ_UG_R 12.1G< 12.3F
PS_FBVDDQ_VCCS 12.1G< 12.3D
PS_FBVDDQ_VCC12 12.1G< 12.3E
PS_NVDD_BOOT 13.1G< 13.3C
PS_NVDD_BOOT_R 13.1G< 13.3D
PS_NVDD_CP 13.1G< 13.3C
PS_NVDD_CP_RC 13.1G< 13.4E
PS_NVDD_EN* 13.1G< 13.4B
PS_NVDD_FB 13.1G< 13.3C
PS_NVDD_FB_RC 13.1G< 13.4F
PS_NVDD_FS 13.1G< 13.3C
PS_NVDD_LDO 13.1G< 13.3C
PS_NVDD_LG 13.1G< 13.3C
PS_NVDD_LG_D 13.1G< 13.3D
PS_NVDD_LG_R 13.1G< 13.4E
PS_NVDD_PHASE 13.1G< 13.3C
PS_NVDD_PVCCS 13.1G< 13.3C
PS_NVDD_RC 13.1G< 13.4F
PS_NVDD_UG 13.1G< 13.3C
PS_NVDD_UG_R 13.1G< 13.3E
PS_NVDD_VCCS 13.1G< 13.3C
PS_NVDD_VCC12 13.1G< 13.3C
PS_PEX_CP 12.1G< 12.4B
PS_PEX_DR 12.1G< 12.3D
PS_PEX_FB 12.1G< 12.4D
ROM_CS* 10.1G< 10.3E
ROM_SCLK 10.3E< 11.1G< 11.4A>
11.4B
ROM_SI 10.3E< 11.1G< 11.3A>
11.3B
ROM_SO 10.3E< 11.1G< 11.3A>
11.3B
SNN_3V3_AUX 2.1B
SNN_AD2_7 12.3G
SNN_A_ID0 5.4G
SNN_A_ID2 5.4F
SNN_BUFRST* 10.3E
SNN_DP_CEC_C 8.4H
SNN_FBA1_NC_A2 4.3A
SNN_FBA1_NC_E2 4.3A
SNN_FBA1_NC_R3 4.2A
SNN_FBA1_NC_R7 4.2A
SNN_FBA2_NC_A2 4.3C
SNN_FBA2_NC_E2 4.3C
SNN_FBA2_NC_R3 4.2C
SNN_FBA2_NC_R7 4.2C
SNN_FBA3_NC_A2 4.3E
SNN_FBA3_NC_E2 4.3E
SNN_FBA3_NC_R3 4.2E
SNN_FBA3_NC_R7 4.2E
SNN_FBA4_NC_A2 4.3G
SNN_FBA4_NC_E2 4.3G
SNN_FBA4_NC_R3 4.2G
SNN_FBA4_NC_R7 4.2G
SNN_FBA_CMD30 3.3C
SNN_FB_VREF 3.5B
SNN_GPIO2 10.2E
SNN_GPIO3 10.2E
SNN_GPIO7 10.2E
SNN_GPIO10 10.2E
SNN_GPIO11 10.2E
SNN_GPIO12 10.2E
SNN_GPIO13 10.2E
SNN_GPIO14 10.3E
SNN_GPIO17 10.3E
SNN_GPU_AA6 10.3C
SNN_GPU_C15 9.2H
SNN_GPU_D15 9.2H
SNN_GPU_J5 9.2H
SNN_GPU_T6 10.3C
SNN_GPU_W6 10.3C
SNN_GPU_Y6 10.3C
SNN_IFPAB_TXD3 7.3D
SNN_IFPAB_TXD3* 7.3D
SNN_IFPAB_TXD7 7.4D
SNN_IFPAB_TXD7* 7.3D
SNN_IFPB_TXC 7.4D
SNN_IFPB_TXC* 7.4D
SNN_IFPC_AUX 9.3C
SNN_IFPC_AUX* 9.3C
SNN_IFPC_HPD 9.3C
SNN_IFPC_L0 9.3C
SNN_IFPC_L0* 9.3C
SNN_IFPC_L1 9.3C
SNN_IFPC_L1* 9.3C
SNN_IFPC_L2 9.3C
SNN_IFPC_L2* 9.3C
SNN_IFPC_L3 9.3C
SNN_IFPC_L3* 9.3C
SNN_IFPC_RSET 9.3B
SNN_IFPE_AUX 9.4C
SNN_IFPE_AUX* 9.4C
SNN_IFPE_L0 9.4C
SNN_IFPE_L1 9.4C
SNN_IFPE_L1* 9.4C
SNN_IFPE_L2 9.4C
SNN_IFPE_L2* 9.4C
SNN_IFPE_L3 9.4C
SNN_IFPE_L3* 9.4C
SNN_IFPE_RSET 9.4B
SNN_PEX_WAKE* 2.2C
SNN_PE_PRSNT2_A 2.1B
SNN_PE_PRSNT2_B 2.2B
SNN_PE_PRSNT2_C 2.3B
SNN_PE_RSVD1 2.2B
SNN_PE_RSVD2 2.2B
SNN_PE_RSVD3 2.2B
SNN_PE_RSVD4 2.2B
SNN_PE_RSVD5 2.3B
SNN_PE_RSVD6 2.4B
SNN_PE_RSVD7 2.4B
SNN_XTALOUTBUFF 10.5E
SNN_XTALSSIN 10.5C
SPDIF 9.1F> 9.1G> 10.4C<
SPDIF_IN 9.1C 9.1G<
SPDIF_IN_C 9.1G< 9.2C
SPDIF_IN_G 9.1G< 9.2D
SPDIF_IN_R 9.1G< 9.2D
SPDIF_TERM 9.1G< 9.2E
STRAP0 10.3C< 11.1G< 11.5A>
11.5B
STRAP1 10.3C< 11.1G< 11.4A>
11.4B
STRAP2 10.3C< 11.1G< 11.4A>
11.4B
STRAP_REF0 10.3C
STRAP_REF1 10.3C
THERMDA 10.1G< 10.2C
THERMDC 10.1G< 10.2C
THERM_N 11.1G< 11.2C
THERM_N_R 11.1G< 11.2B
THERM_P* 11.1G< 11.2C
THERM_P_Q 11.1G< 11.2B
THERM_SHUTDOWN* 11.1G< 11.2A> 13.4A<
XTAL_IN 10.1F< 10.5C
XTAL_OUT 10.1F< 10.5E

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BKT1 [9.3D]
C1 [8.4E]
C2 [8.4E]
C3 [8.4E]
C4 [8.4E]
C5 [5.5B]
C6 [8.4E]
C7 [8.4E]
C8 [8.4E]
C9 [8.4E]
C10 [8.5E]
C11 [12.2B]
C12 [8.4B]
C13 [12.2A]
C14 [12.3B]
C15 [12.3C]
C16 [12.3B]
C17 [9.4D]
C18 [13.2G]
C19 [2.1B]
C20 [8.2D]
C21 [8.3D]
C22 [6.4E]
C23 [12.5G]
C24 [12.3E]
C25 [12.3D]
C26 [12.5E]
C27 [12.4C]
C29 [13.2F]
C30 [12.3E]
C31 [6.4E]
C32 [13.2E]
C33 [12.4F]
C34 [12.5F]
C35 [13.3F]
C36 [13.2F]
C37 [13.2G]
C38 [13.2F]
C39 [13.2G]
C40 [6.5E]
C41 [13.4F]
C42 [12.4G]
C43 [2.1A]
C44 [12.2C]
C45 [2.1A]
C46 [2.1A]
C47 [9.2C]
C48 [10.3C]
C51 [12.2D]
C52 [13.3G]
C53 [10.5E]
C54 [12.4H]
C55 [11.3B]
C57 [10.5C]
C58 [12.4A]
C60 [12.4A]
C61 [12.4B]
C62 [5.3B]
C63 [5.3B]
C64 [10.4G]
C65 [10.3G]
C66 [6.4A]
C67 [7.3B]
C68 [5.4B]
C69 [9.3B]
C70 [6.4A]
C71 [13.3C]
C73 [7.3B]
C74 [2.2G]
C75 [2.1G]
C76 [11.3C]
C77 [2.5F]
C78 [2.5F]
C79 [13.3D]
C80 [4.4G]
C81 [4.4G]
C82 [4.4G]
C83 [4.4G]
C84 [4.4G]
C85 [4.4F]
C86 [4.4F]
C87 [4.4F]
C88 [4.4G]
C89 [4.4F]
C90 [4.4G]
C91 [4.4F]
C92 [3.5F]
C93 [3.5G]
C94 [3.5E]

C95 [3.5G]
C96 [3.5F]
C97 [3.5G]
C99 [8.3B]
C100 [4.4F]
C101 [8.3C]
C103 [8.3C]
C106 [10.2G]
C107 [11.2C]
C108 [13.1E]
C109 [13.1F]
C110 [13.1F]
C112 [9.2E]
C113 [9.1E]
C114 [12.4C]
C115 [13.3B]
C162 [5.2B]
C163 [5.2B]
C501 [4.4G]
C502 [3.5F]
C503 [3.5F]
C504 [4.4F]
C505 [4.4G]
C506 [4.4F]
C507 [4.4G]
C508 [4.3H]
C509 [4.3C]
C510 [4.4G]
C511 [4.4G]
C512 [4.4G]
C513 [4.4G]
C514 [4.4G]
C515 [4.4G]
C516 [2.5D]
C517 [2.5D]
C518 [2.5D]
C519 [2.5D]
C520 [2.5D]
C521 [2.5D]
C522 [2.4D]
C523 [2.4D]
C524 [3.1C]
C525 [3.1D]
C526 [3.2D]
C529 [2.4D]
C530 [3.2D]
C532 [3.5C]
C533 [2.4D]
C534 [3.1D]
C535 [2.3F]
C536 [2.2F]
C537 [2.2G]
C538 [2.3G]
C539 [2.1F]
C541 [3.1D]
C542 [3.2C]
C543 [3.2D]
C544 [2.4D]
C545 [2.3F]
C548 [2.4D]
C550 [2.3F]
C551 [2.2F]
C552 [2.3F]
C554 [2.4G]
C555 [2.4G]
C561 [2.3F]
C562 [2.4D]
C565 [2.2F]
C567 [2.2F]
C568 [2.1F]
C569 [2.4D]
C570 [2.3F]
C575 [2.2F]
C577 [6.4B]
C578 [2.4D]
C580 [2.1G]
C581 [12.4A]
C584 [2.4D]
C585 [8.4A]
C586 [10.4C]
C587 [8.4B]
C588 [10.4C]
C589 [7.3B]
C591 [8.4A]
C592 [9.3B]
C594 [10.4C]
C596 [7.3B]
C597 [2.3D]
C598 [2.3D]
C599 [5.4A]
C602 [5.4A]
C604 [2.3D]
C606 [2.3D]
C608 [2.3D]
C609 [2.3D]
C610 [11.3F]

C611 [10.2B]
C612 [2.3D]
C613 [2.3D]
C614 [2.3D]
C615 [2.3D]
C616 [2.2D]
C617 [2.2D]
C618 [2.2D]
C619 [2.2D]
C620 [2.2D]
C621 [2.2D]
C622 [13.3E]
C623 [13.4D]
C624 [13.4G]
C625 [13.4E]
C626 [12.3G]
C627 [13.4F]
C628 [12.4E]
C629 [13.2D]
C630 [6.5C]
C631 [2.1B]
C632 [13.4E]
C633 [12.5C]
C635 [12.3E]
C636 [12.3G]
C637 [12.3E]
C638 [13.4B]
C639 [12.3G]
C640 [12.3F]
C641 [8.3F]
C642 [6.5B]
C643 [8.5F]
C644 [5.3C]
C645 [5.5C]
C646 [5.5E]
C647 [7.4E]
C648 [7.2G]
C649 [5.4E]
C650 [5.4E]
CN1 [2.3C]
D1 [5.2E]
D2 [5.3E]
D3 [5.2E]
D4 [5.3E]
D5 [10.2H]
D6 [6.3E]
D7 [6.3E]
D8 [8.3H]
D9 [8.5E]
D10 [8.2E]
D11 [8.3F]
D12 [8.4F]
D13 [6.2E]
D14 [8.4E]
D15 [6.4E]
D16 [8.5E]
D17 [10.3B]
D18 [10.3B]
D20 [9.5E]
D21 [9.3F]
DS02 [13.3E]
DS03 [5.4E]
DS04 [7.4E]
DS05 [5.4E]
DS06 [5.5E]
F1 [12.2G]
FS01 [12.2B]
G1 [2.3E]
G1 [3.3C]
G1 [5.4C]
G1 [8.4C]
G1 [7.3D]
G1 [8.4C]
G1 [9.3G 9.3C 9.4C]
G1 [10.5D 10.3D 10.2D]
J1 [5.4G]
J2 [8.4H]
J3 [7.3G]
J4 [6.4G]
J5 [9.4E]
J6 [9.5F]
J7 [9.1C]
JS01 [10.2A]
L1 [6.4E]
L2 [6.4E]
L3 [6.5E]
L4 [12.4G]
L5 [12.3G]
L6 [13.3F]
L7 [13.3F]
L8 [2.5G]
L9 [2.5G]
L10 [13.3F]
L501 [5.4E]

L502 [5.5E]
L503 [5.4E]
LB1 [8.5F]
LB2 [12.2D]
LB3 [12.3A]
LB4 [12.3A]
LB5 [7.3B]
LB6 [9.3A]
LB7 [7.3B]
LB9 [10.4C]
LB501 [3.5D]
LB502 [8.4A]
LB503 [10.4C]
LB504 [7.3B]
LB505 [8.4A]
LB506 [7.4F]
M1 [4.4B 4.4C 4.2B]
M2 [4.2E 4.3E 4.4E]
M501 [4.3C 4.3B 4.2D]
M502 [4.3D 4.4D 4.2G]
MEC1 [9.3F]
MEC2 [9.3F]
MEC3 [9.3F]
MEC4 [9.4F]
MEC5 [9.4F]
MEC6 [9.3E]
MEC7 [6.4G]
Q1 [10.2F]
Q2 [8.3G]
Q3 [13.4B]
Q4 [11.2B]
Q5 [12.3B]
Q6 [12.3F 12.4F]
Q7 [13.3E]
Q8 [13.3E]
Q9 [11.2G]
Q10 [11.2F]
Q11 [11.2C]
Q12 [11.3C]
Q13 [10.2F]
Q14 [9.2D]
Q15 [9.2E]
Q16 [13.5E]
Q17 [13.5F]
Q502 [13.4B]
Q503 [12.5D]
Q504 [12.5C]
Q506 [8.2D]
Q507 [8.3D]
Q508 [8.2E]
Q509 [8.3E]
Q511 [8.3G]
R1 [5.2D]
R2 [5.3D]
R3 [5.2D]
R4 [5.3D]
R5 [5.2D]
R6 [5.2D]
R7 [6.3D]
R8 [5.3D]
R9 [6.2D]
R10 [5.3D]
R11 [6.3D]
R12 [6.3D]
R13 [8.2E]
R14 [8.3E]
R15 [13.4A]
R16 [6.2D]
R17 [6.2D]
R18 [10.2E]
R19 [8.2E]
R20 [8.3E]
R21 [8.2F]
R22 [8.2F]
R23 [8.2G]
R24 [8.2F]
R25 [12.2B]
R26 [12.2B]
R27 [13.4B]
R28 [8.2E]
R29 [8.2E]
R30 [8.3E]
R31 [8.3E]
R32 [6.2D]
R33 [6.2D]
R34 [10.2E]
R35 [6.4D]
R36 [8.4D]
R37 [6.4E]
R38 [12.3D]
R39 [10.2E]
R40 [12.5G]

R42 [13.4B]
R43 [12.5G]
R44 [12.4B]
R45 [12.5F]
R46 [12.3D]
R47 [12.5G]
R48 [12.4B]
R49 [6.4E]
R50 [6.5E]
R51 [13.3F]
R52 [12.4G]
R53 [12.2D]
R54 [2.1C]
R55 [10.3C]
R56 [10.3C]
R57 [11.3G]
R58 [11.2F]
R59 [10.4F]
R60 [10.2C]
R61 [10.2C]
R62 [10.4F]
R63 [10.3F]
R64 [11.3B]
R65 [11.4B]
R66 [5.4B]
R67 [11.3B]
R68 [11.4B]
R69 [11.3B]
R70 [11.3B]
R71 [9.1F]
R72 [13.1E]
R73 [2.2D]
R74 [3.4D]
R75 [3.4D]
R76 [3.5D]
R77 [4.5B]
R78 [3.3F]
R79 [3.3F]
R80 [3.4F]
R81 [3.4F]
R82 [3.4H]
R83 [3.4H]
R84 [13.3E]
R85 [13.3C]
R86 [13.3C]
R87 [13.5D]
R88 [13.4D]
R89 [11.2B]
R90 [11.3C]
R91 [11.3C]
R92 [11.2C]
R93 [11.2C]
R95 [13.4E]
R96 [9.4D]
R97 [9.5D]
R98 [9.5D]
R99 [9.5E]
R100 [9.5E]
R101 [10.2F]
R104 [9.2C]
R105 [9.2C]
R106 [9.2D]
R107 [9.2D]
R108 [9.1E]
R109 [9.1F]
R110 [13.4F]
R111 [10.2F]
R112 [10.2G]
R113 [13.5C]
R114 [13.4G]
R501 [3.1F]
R502 [3.5H]
R503 [3.3F]
R504 [3.5H]
R505 [3.3F]
R506 [3.2F]
R507 [3.3F]
R508 [3.1F]
R509 [3.3F]
R510 [3.2F]
R511 [3.2F]
R512 [4.3C]
R513 [3.2F]
R514 [4.3C]
R515 [4.5D]
R516 [10.4E]
R517 [10.3C]
R518 [10.3C]
R523 [2.5F]
R525 [2.1D]
R527 [6.4B]
R530 [6.4B]
R531 [11.4B]
R532 [7.3C]
R533 [5.4D]
R534 [11.4B]

R535 [11.4B]
R536 [5.4D]
R537 [5.5D]
R538 [11.4B]
R539 [11.5B]
R540 [11.5B]
R541 [6.4D]
R542 [6.4D]
R543 [6.5D]
R544 [10.2B]
R545 [10.2B]
R546 [10.2B]
R550 [8.5D]
R551 [8.5D]
R552 [10.2B]
R553 [10.3B]
R554 [10.2B]
R555 [10.2B]
R556 [13.3D]
R557 [13.4E]
R558 [13.3D]
R560 [13.4G]
R561 [13.4F]
R562 [13.4F]
R563 [13.4D]
R564 [13.4F]
R565 [12.3E]
R566 [12.5C]
R567 [13.2C]
R568 [13.3D]
R569 [12.4D]
R572 [12.4B]
R573 [12.5C]
R574 [12.5C]
R575 [8.3G]
R577 [8.3G]
R578 [8.3G]
R579 [12.3F]
R580 [12.3F]
R581 [8.3H]
R582 [8.5E]
R583 [8.5E]
R584 [7.4E]
R585 [5.4E]
R586 [7.4E]
R587 [5.5E]
R588 [5.4E]
RP1 [10.2B 10.2B 10.2B 10.2B]
RP2 [3.4G 3.4F 3.4F 3.4G]
RP3 [3.4F 3.4F 3.3F 3.3F]
RP4 [3.4F 3.4H 3.4H 3.4F]
RP5 [3.4F 3.4F 3.3H 3.3H]
RP6 [3.2G 3.2H 3.2H 3.2G]
RP7 [3.4G 3.4H 3.4H 3.4G]
RP8 [3.4G 3.4H 3.4G 3.4H]
RP9 [3.3H 3.3G 3.3G 3.3H]
RP10 [3.3H 3.3H 3.4F 3.4F]
RP11 [3.3G 3.3G 3.3G 3.3G]
RP12 [3.3G 3.3H 3.3G 3.3H]
TP1 [3.2F]
TP2 [3.2F]
TP501 [3.2F]
TP502 [3.2F]
TP503 [3.2F]
TP504 [3.2F]
TP505 [3.4D]
TP506 [10.2C]
TP507 [10.2C]
U1 [5.3D 5.3D]
U1 [6.3D 6.3D]
U2 [12.3G]
U3 [12.2B]
U4 [10.2G]
U5 [13.1E]
U501 [10.3G]
U502 [10.4G]
U503 [13.3C]
U504 [12.4D]
Y1 [10.5D]

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