

# NV11,4Mx16 DDR, RGB, INTERNAL DVI-I, AGP.

PCI DEVICE ID 0X0=0X110 FOR NV11.

STRAPS: AGP4X, SIDEBAND DIS, FAST WRITE ENA, ADP BIOS, NORMAL PCIAD, 14.318MHZ  
STRAP\_RAM\_TYPE [5:2]=1010.4MX16 DDR SDRAM

## HISTORY REV. A00:

- 1) A00: Imported P0039-C00
- 2) A00: Changed FB Memory to 4Mx16 DDR Ram
- 3) A00: Added 2.5V Power Reg for DDR RAM
- 4) A00: Changed Strap resistors.

## HISTORY REV. A01:

- Changed R212 to 110R value (RSET)

602-10044-0000-A01



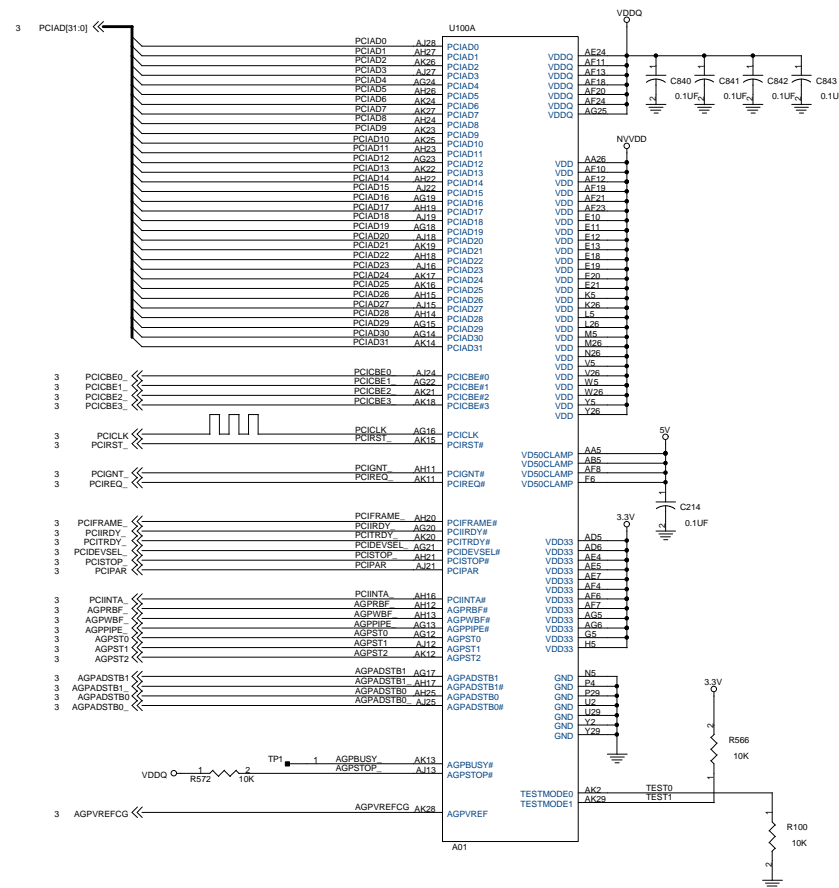
NVIDIA Corporation  
3535 Monroe St  
Santa Clara, CA 95051, USA

Size B	CAGE Code	DWG NO	Rev
Scale			Sheet 1 of 12

Thursday, April 04, 2002

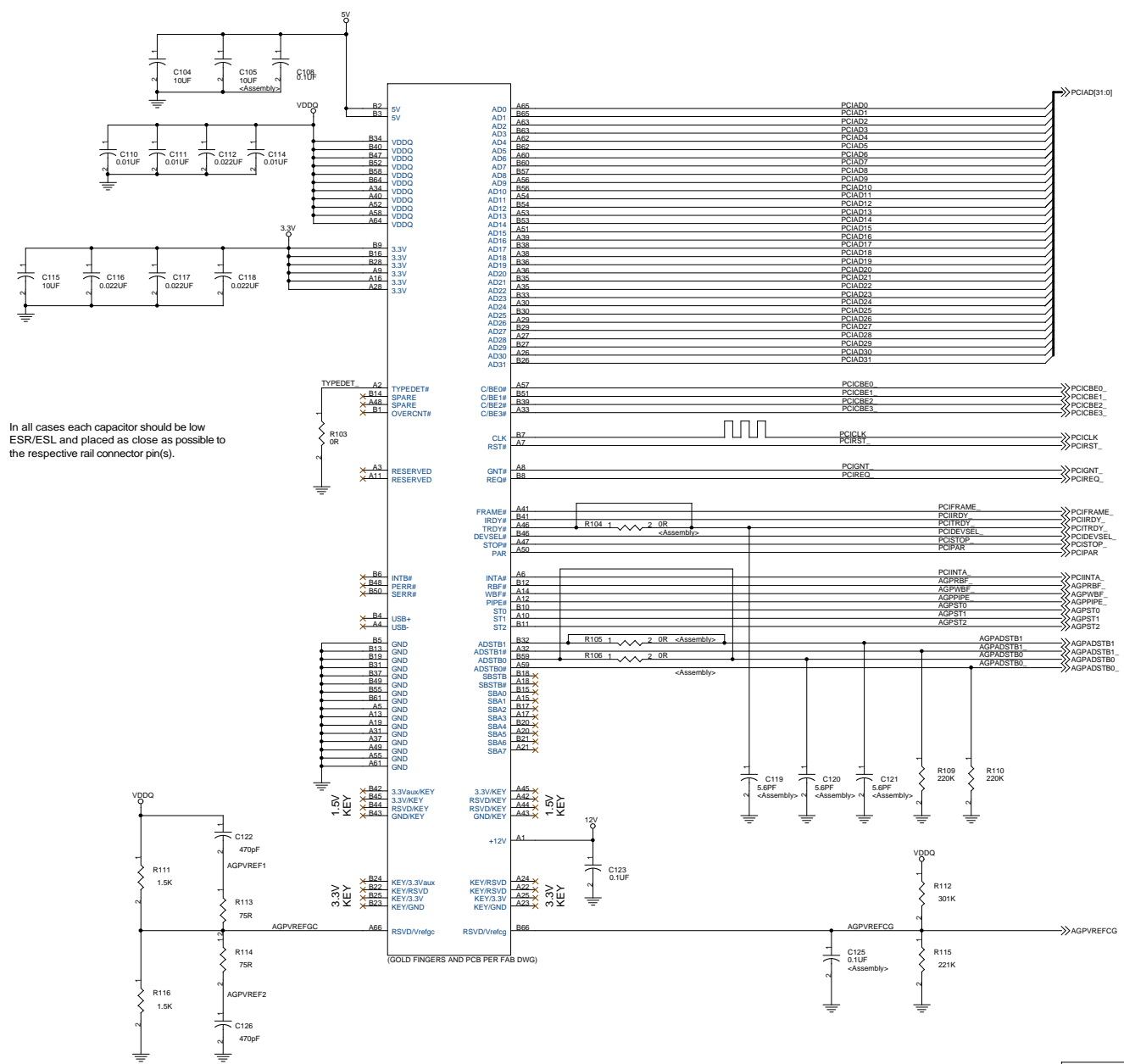
{Item}\t{Quantity}\t{Reference}\t{Source Package}\t{Value}\t{Assembly}  
{Assembly}\t{Source Package}\t{Value}\t{PN}\t{AVL1}\t{AVL2}\t{AVL3}\t{AVL4}\t{AVL5}

HEATSINK



# 1a. NVXX HOST

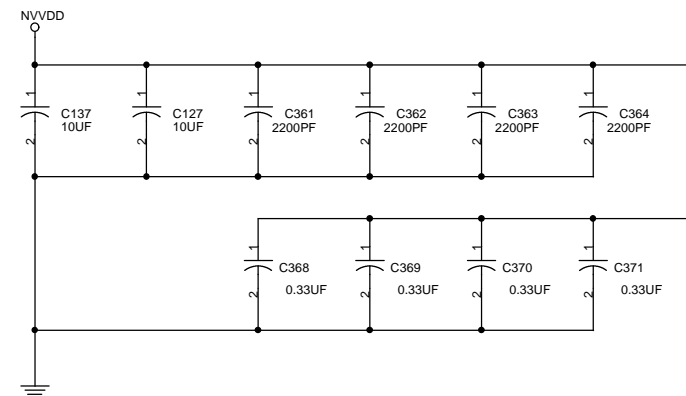
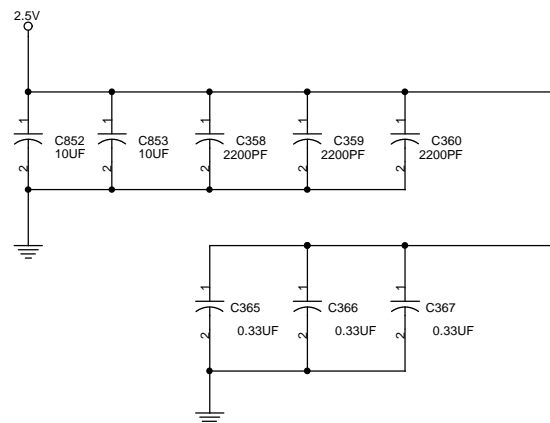
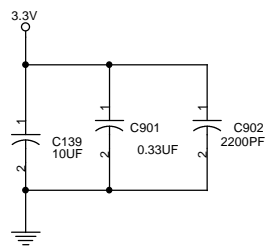
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	Size	CAGE Code	DWG NO
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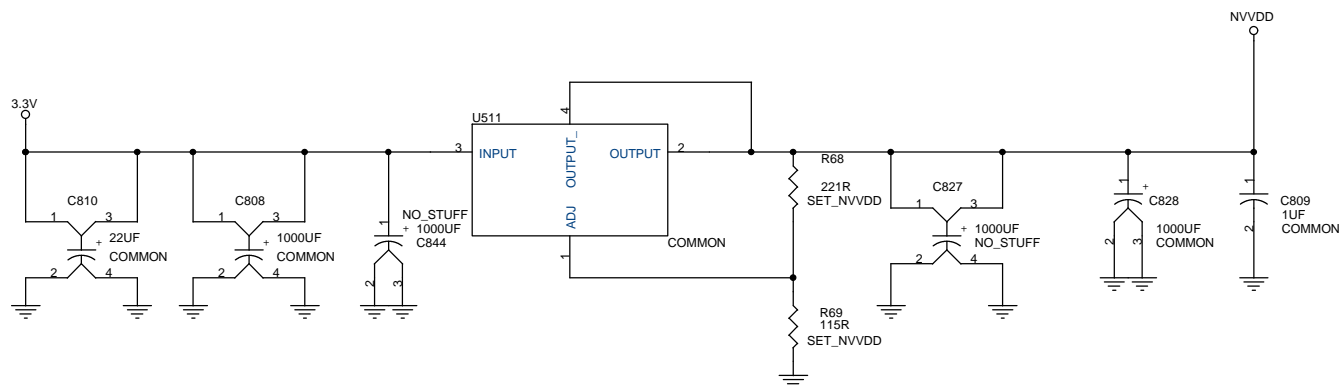
In all cases each capacitor should be low ESR/ESL and placed as close as possible to the respective rail connector pin(s).

# 1b1. AGP I/O


		NVIDIA Corporation 3535 Monroe St Santa Clara, CA 95051, USA	
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TO-263 2-pin package  
NIKO-SEM LT1084S



## 1y. NVXX DECOUPLING

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7,11,12 TVED[11:0] >>  
7,11 VIPD[7:0] >>  
7 DFPD[11:0] >>



## 1z. NVXX HOST STRAPS



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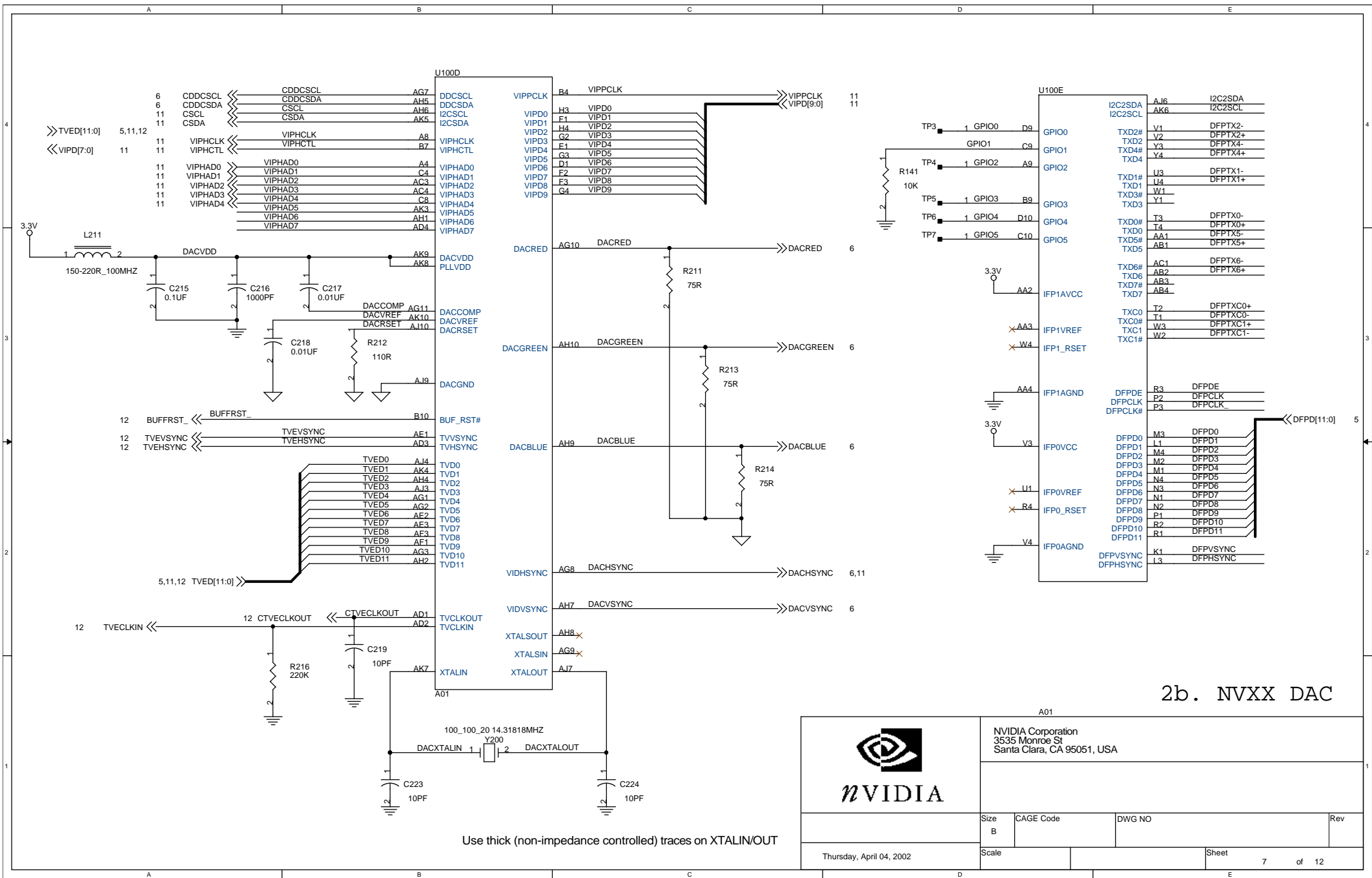
Size B	CAGE Code	DWG NO	Rev
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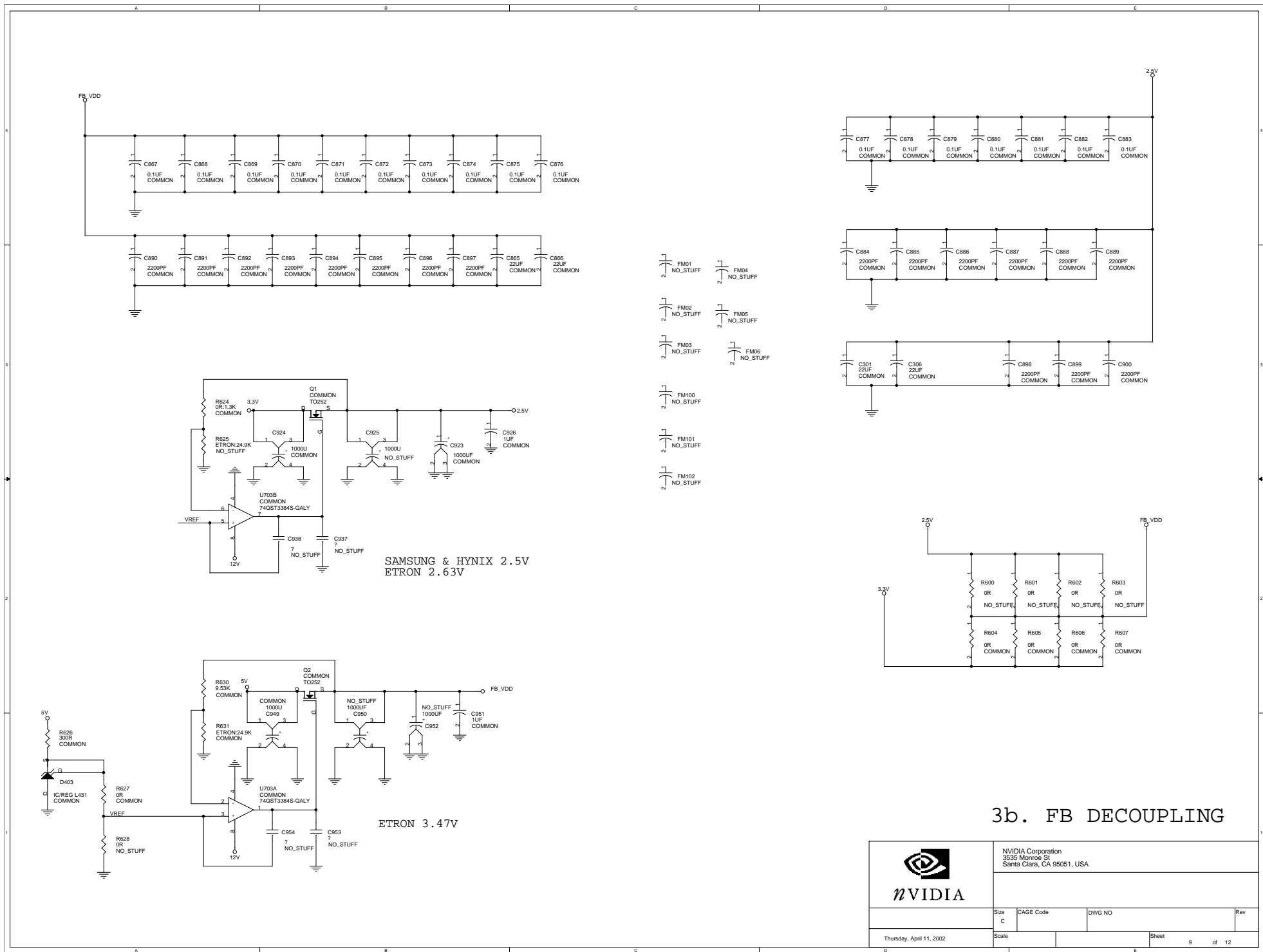
Rev

9 10 11

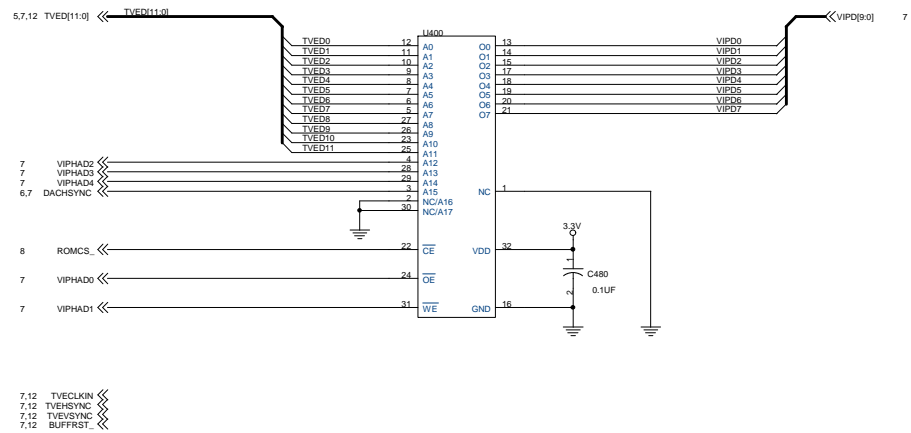













## 4a. ROM VIP & VIDEO IF

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