

# V191-31

## P684-A01 GT216 DESKTOP Low Profile

## PCI-EXPRESSx16 DL-DVI HDMI VGA DDR3

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### V191 0A pcb change list

- Page 2 : Add EC1802 for 12V input
- Page 9 : Move ESD part to I/O input and change ESD parts footprint
- Page 10 : Move ESD part to I/O input and change ESD parts footprint and change DACB DSUB Header
- Page 11 : Move ESD part to hotplug input and change ESD parts footprint and Add EMI solution
- Page 12 : Move ESD part to hotplug input and change ESD parts footprint and Add EMI solution
- Page 16 : Add Fly\_cable / MC1 HDMI screw / PCB and change EMI Spring footprint
- Page 17 : Remove J6 JTAG
- Page 18 : Add HAD\_RST\* pull down Resistor
- Page 19 : Change 5V solution to SOT223 LDO and remove U3 reserve and add C52 for 3V3 and C138 for IFP\_PLLVDD
- Page 20 : Change FBVDDQ to UP6101 and PEX\_VDD to UP7706 solution
- Page 21 : Change NVVDD to UP6101 solution and add impedance test header

### V191 30 pcb change list

- Page 9 : Add Capacitor on ESD part for RGB
- Page 10 : Remove Flycable function
- Page 11 : Move hotplug input ESD part locate to same as P684
- Page 12 : Move hotplug input ESD part locate to same as P684
- Page 18 : Remove HDCP and Biosinfo ROM
- Page 21 : change EC321,EC323 footprint size to 6.3x9

### V191 31 pcb change list

- Page 5 : Add Capacitor C649 C684 for NVVDD
- Page 16 : Change EM1 EM2 EM3 footprint for EMI
- Page 17 : Since J5 footprint issue,Revise J5 pin define to same as P684
- Page 21 : Change EL21 footprint


REV	VARIANT	NVPPN	ASSEMBLY
0	BASE	600-10684-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SRU0000	600-10684-0000-100	GT216-300 600/1000MHz 1024MB 64MBx16 BGA150 800MHz DDR3 DVI-I/DP/HDMI/VGA
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13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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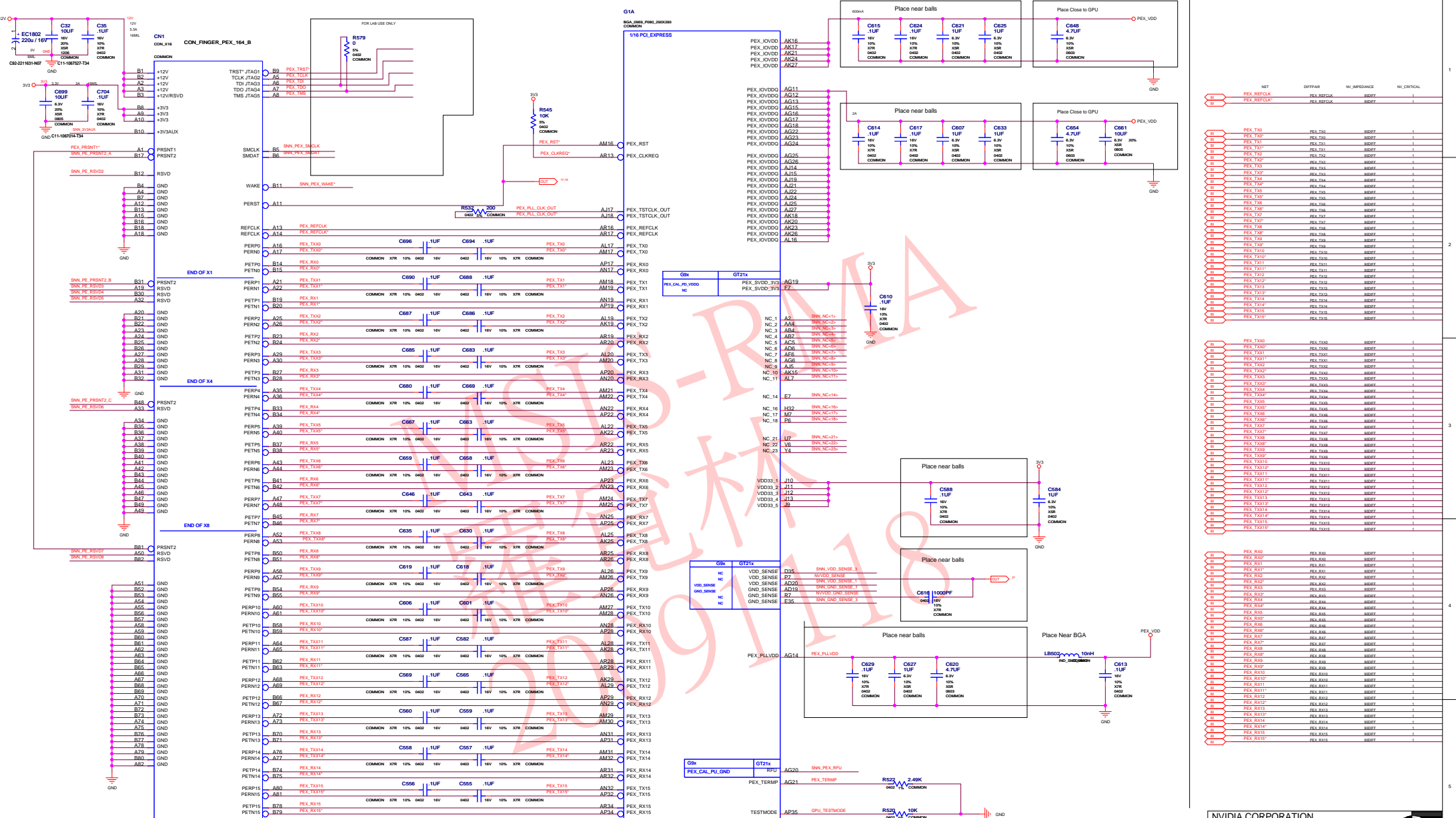
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## PCI-EXPRESS INTERFACE



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ASSEMBLY	
PAGE DETAIL	PCI-EXPRESS INTERFACE

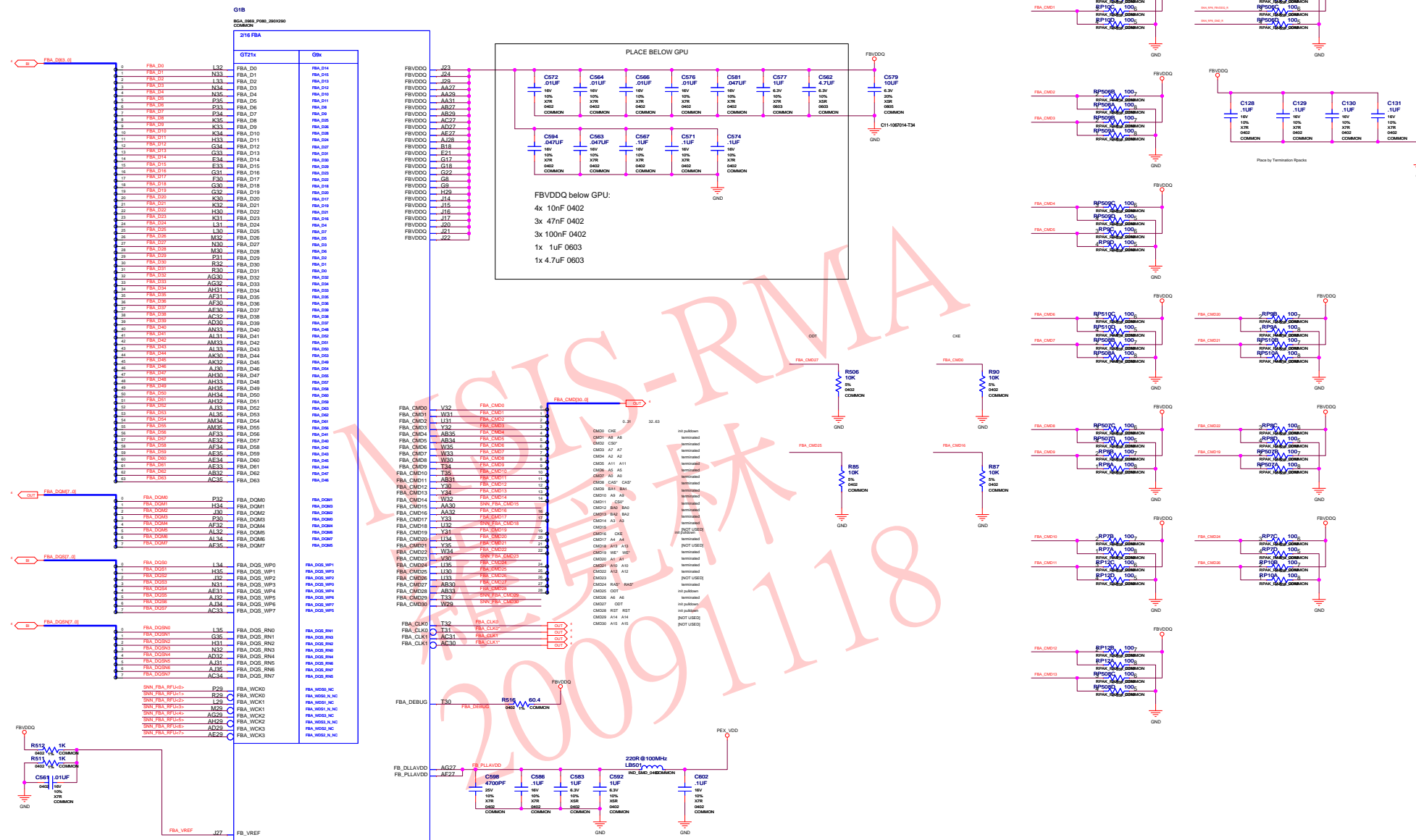
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PARTITION A FRAME BUFFER INTERFACE



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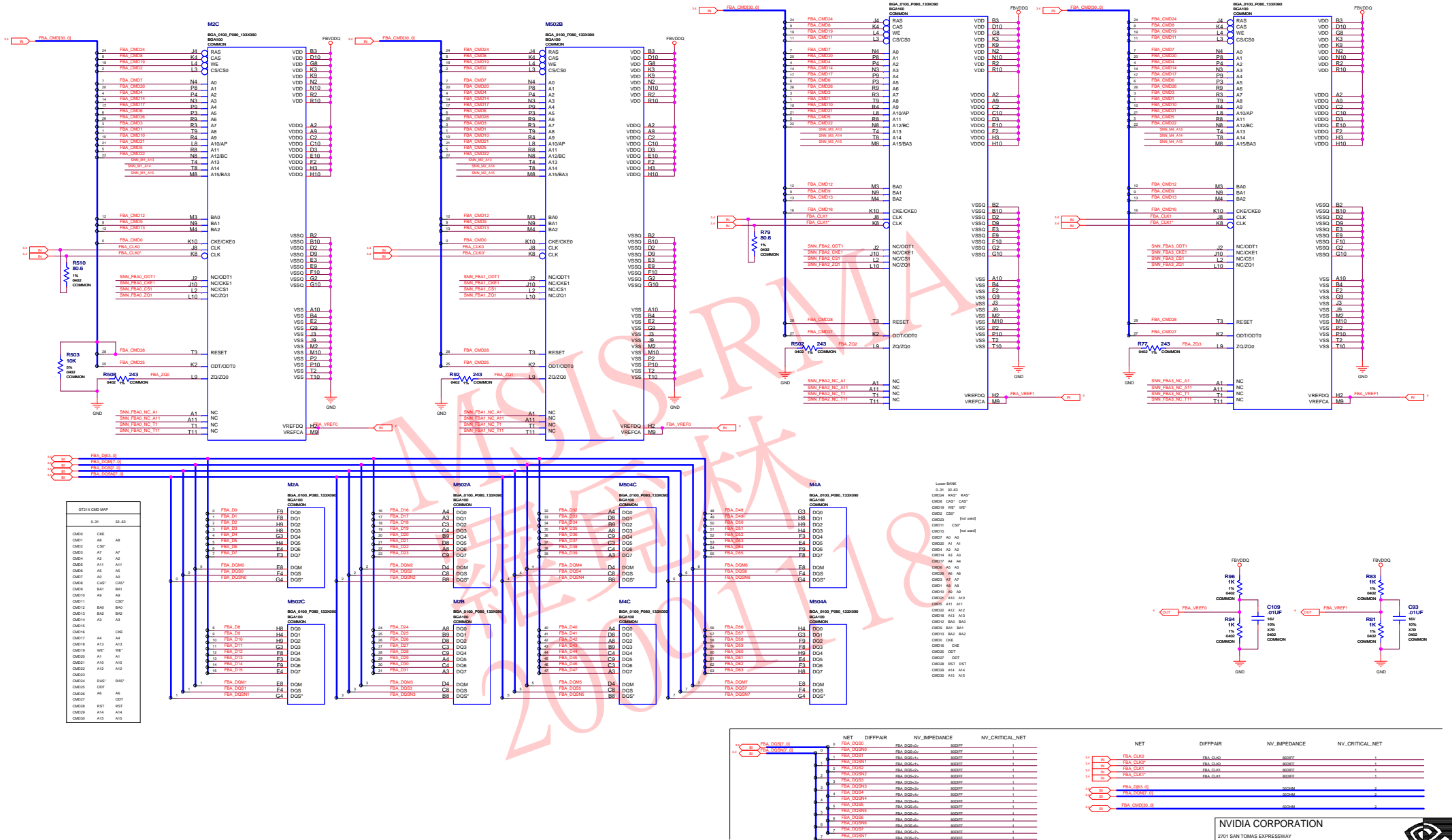
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PARTITION A MEMORY

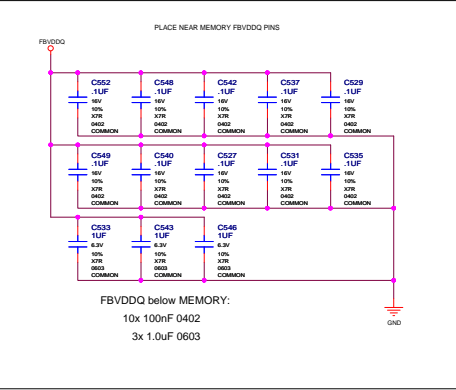


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PAGE 001		PARTITION A MEMORIES	

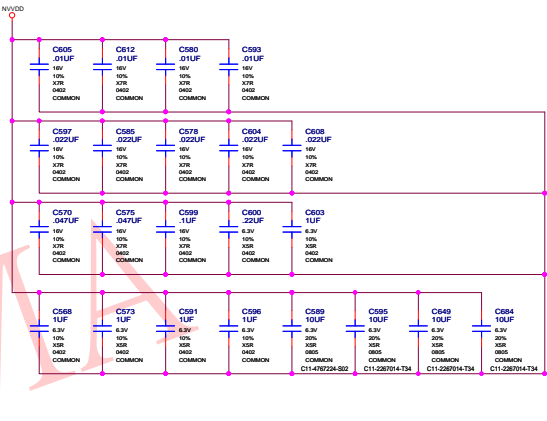
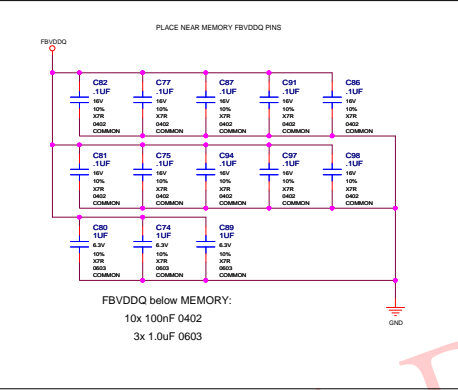
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FBA_CMD05	FBA_CMD05	1000	1
FBA_CMD06	FBA_CMD06	1000	1
FBA_CMD07	FBA_CMD07	1000	1
FBA_CMD08	FBA_CMD08	1000	1
FBA_CMD09	FBA_CMD09	1000	1
FBA_CMD10	FBA_CMD10	1000	1
FBA_CMD11	FBA_CMD11	1000	1
FBA_CMD12	FBA_CMD12	1000	1
FBA_CMD13	FBA_CMD13	1000	1
FBA_CMD14	FBA_CMD14	1000	1
FBA_CMD15	FBA_CMD15	1000	1
FBA_CMD16	FBA_CMD16	1000	1
FBA_CMD17	FBA_CMD17	1000	1
FBA_CMD18	FBA_CMD18	1000	1
FBA_CMD19	FBA_CMD19	1000	1
FBA_CMD20	FBA_CMD20	1000	1
FBA_CMD21	FBA_CMD21	1000	1
FBA_CMD22	FBA_CMD22	1000	1
FBA_CMD23	FBA_CMD23	1000	1
FBA_CMD24	FBA_CMD24	1000	1
FBA_CMD25	FBA_CMD25	1000	1
FBA_CMD26	FBA_CMD26	1000	1
FBA_CMD27	FBA_CMD27	1000	1
FBA_CMD28	FBA_CMD28	1000	1
FBA_CMD29	FBA_CMD29	1000	1
FBA_CMD30	FBA_CMD30	1000	1
FBA_CMD31	FBA_CMD31	1000	1
FBA_CMD32	FBA_CMD32	1000	1
FBA_CMD33	FBA_CMD33	1000	1
FBA_CMD34	FBA_CMD34	1000	1
FBA_CMD35	FBA_CMD35	1000	1
FBA_CMD36	FBA_CMD36	1000	1
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FBA_CMD98	FBA_CMD98	1000	1
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FBA_CMD100	FBA_CMD100	1000	1

FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS

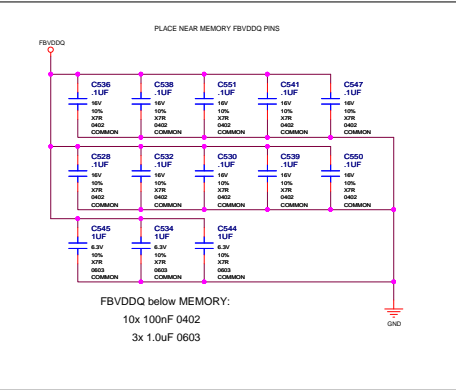
Decoupling for FBA 0..15



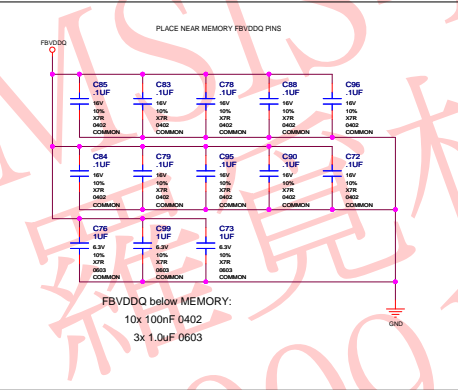
Decoupling for FBA 16..31



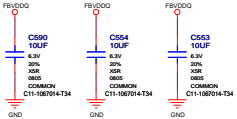
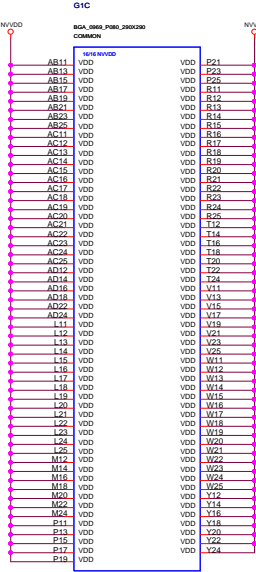
Decoupling for FBA 32..47



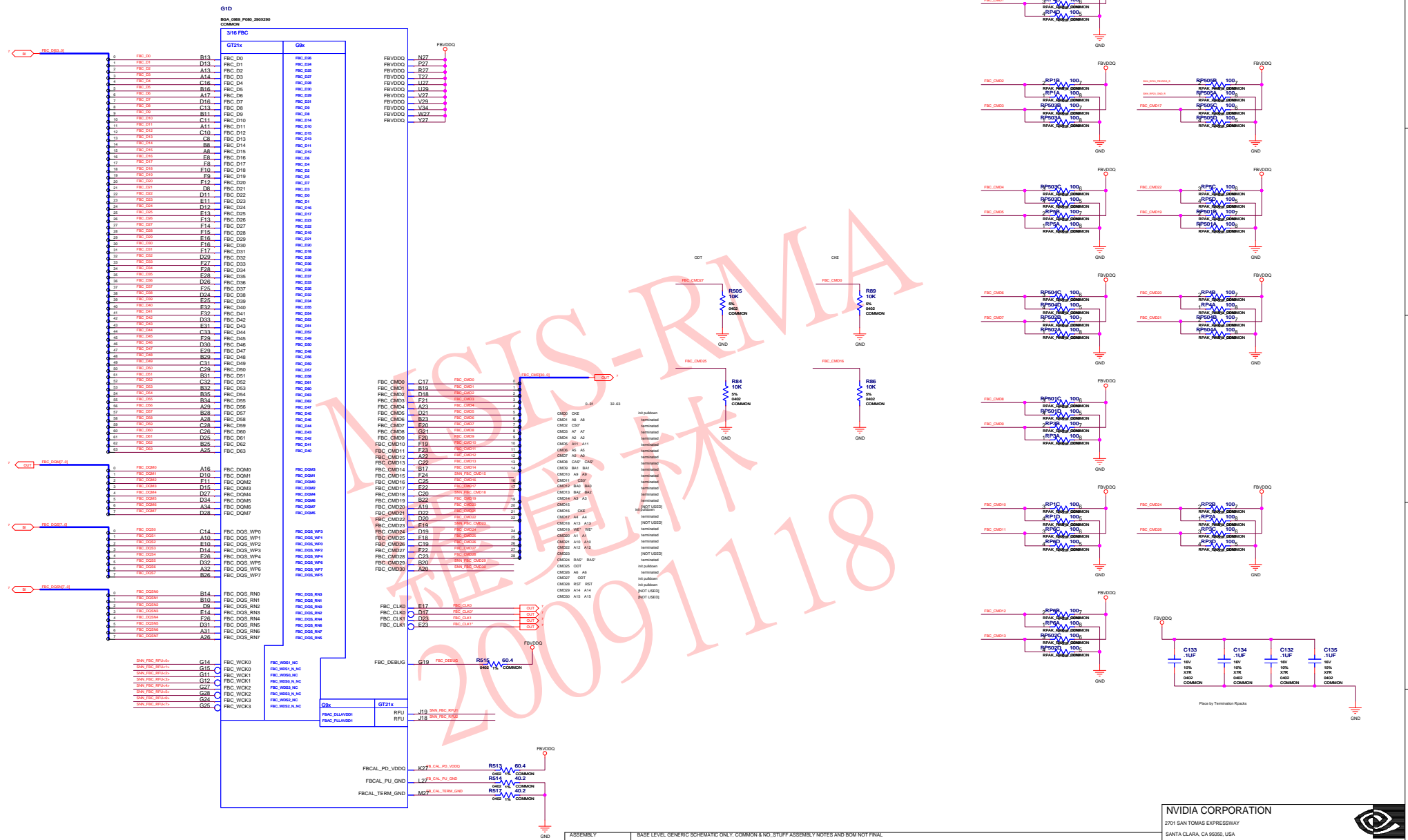
Decoupling for FBA 48..63



NVVDD under GPU:  
4x 0.01uF 0402 X7R  
5x 0.022uF 0402 X7R  
2x 0.047uF 0402 X7R  
1x 0.1uF 0402 X7R  
1x 0.22uF 0402 X7R  
4x 1.0uF 0402 X5R  
1x 2.2uF 0402 X5R  
2x 10uF 0805 X5R



## PARTITION C FRAME BUFFER INTERFACE



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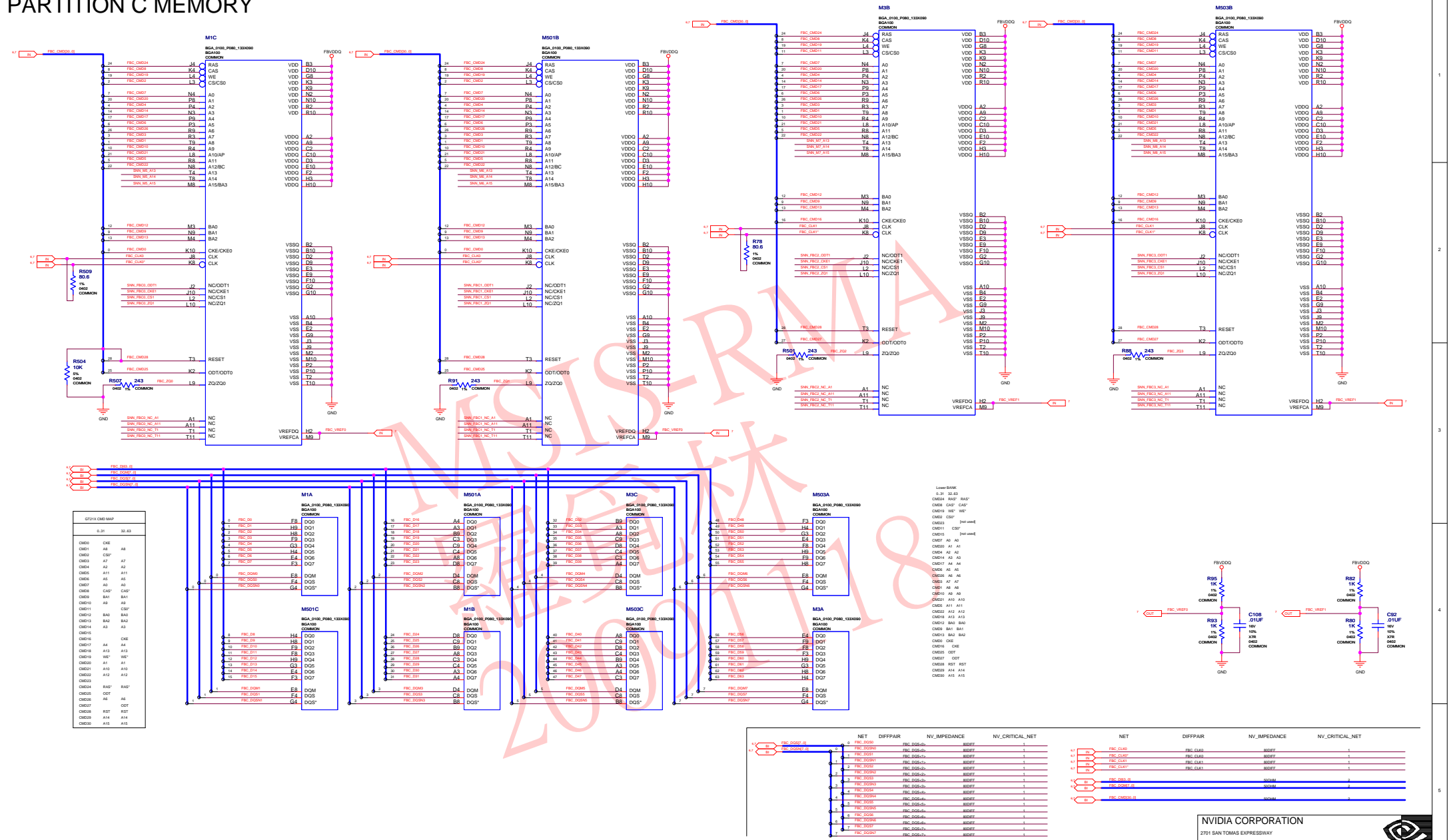
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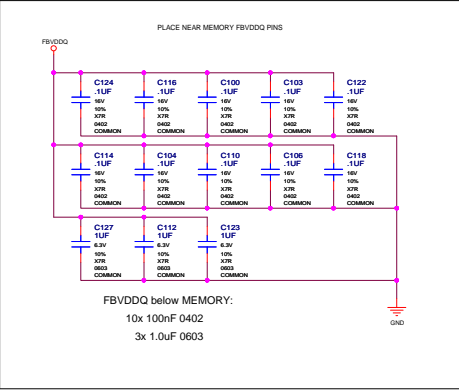
## PARTITION C MEMORY



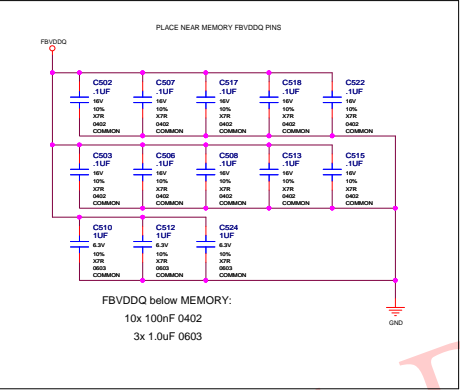
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FBC DECOUPLING CAPS & NVVDD DECOUPLING CAPS

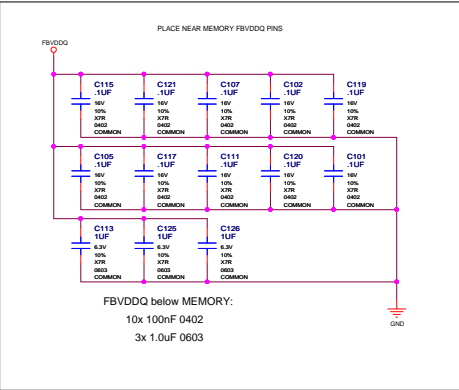
Decoupling for FBC 0..15



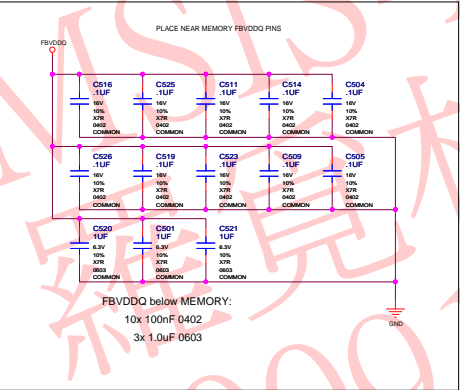
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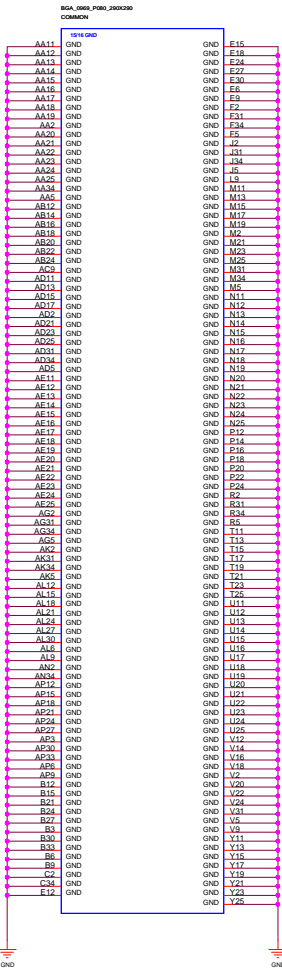
Decoupling for FBC 32..47



Decoupling for FBC 48..63

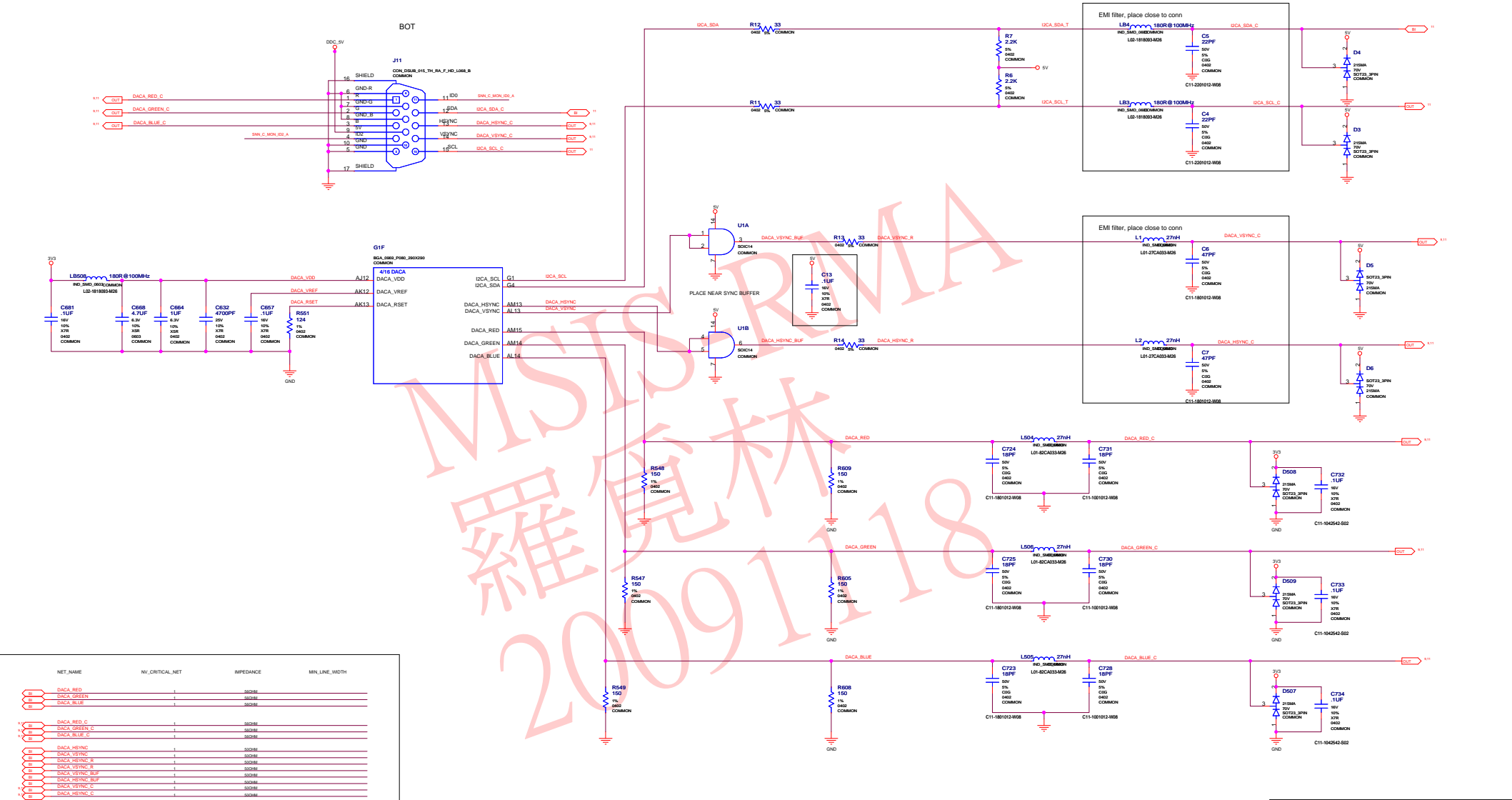


G1E

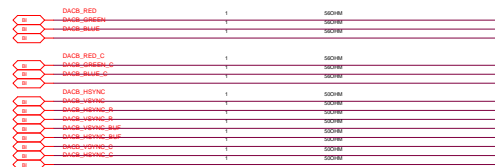
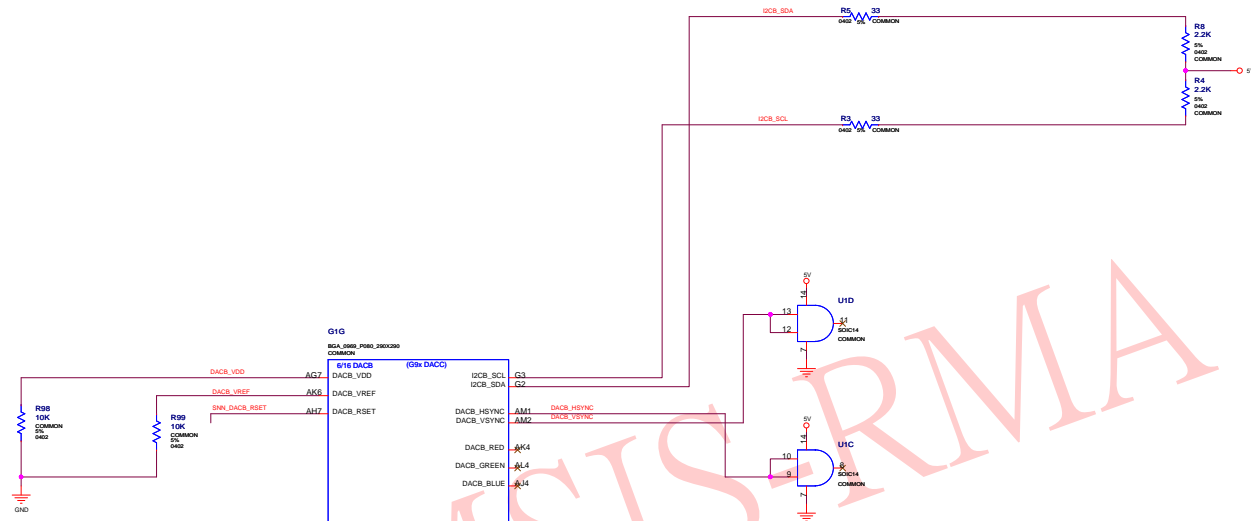




DACA (SOUTH DVI-I)



DACB (cable-up VGA)



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PAGE DETAIL	DACB (MID DVI-I)

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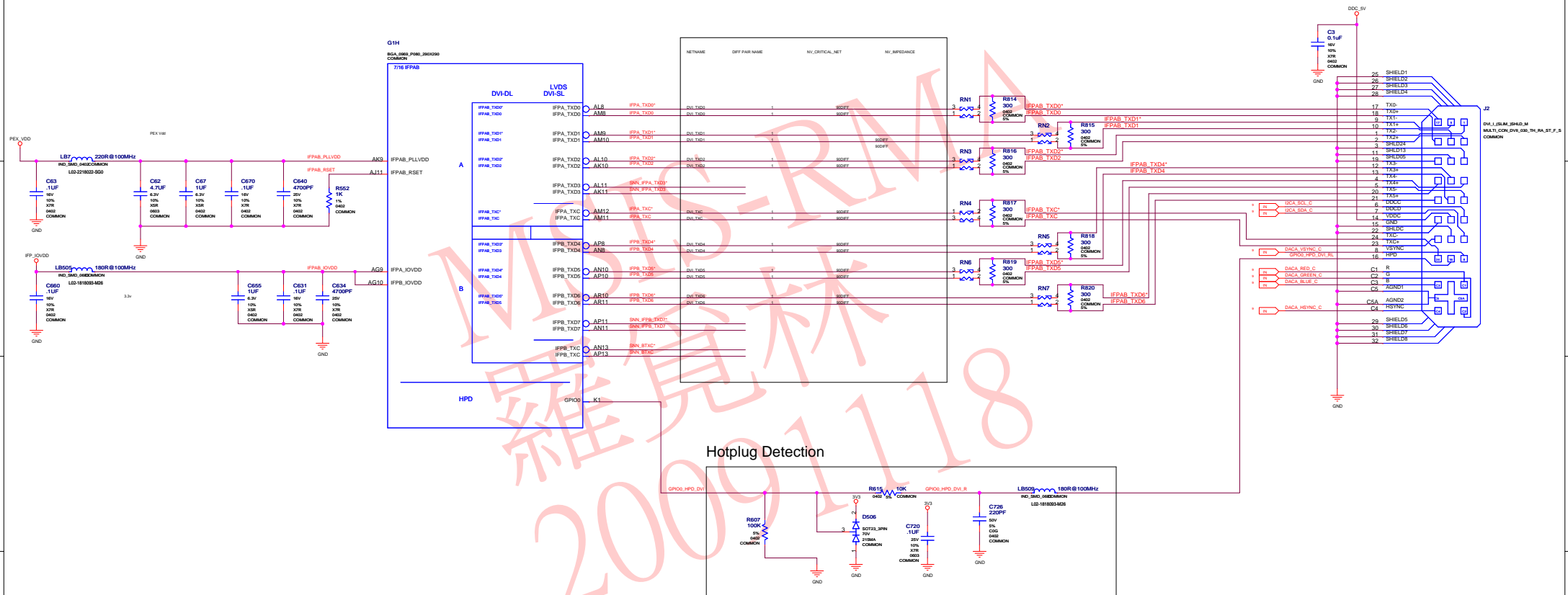


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## IFP AB (SOUTH DVI-I)



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PAGE DETAIL	IFP AB (SOUTH DVI-I)

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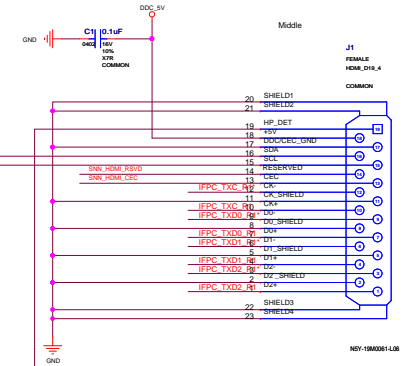
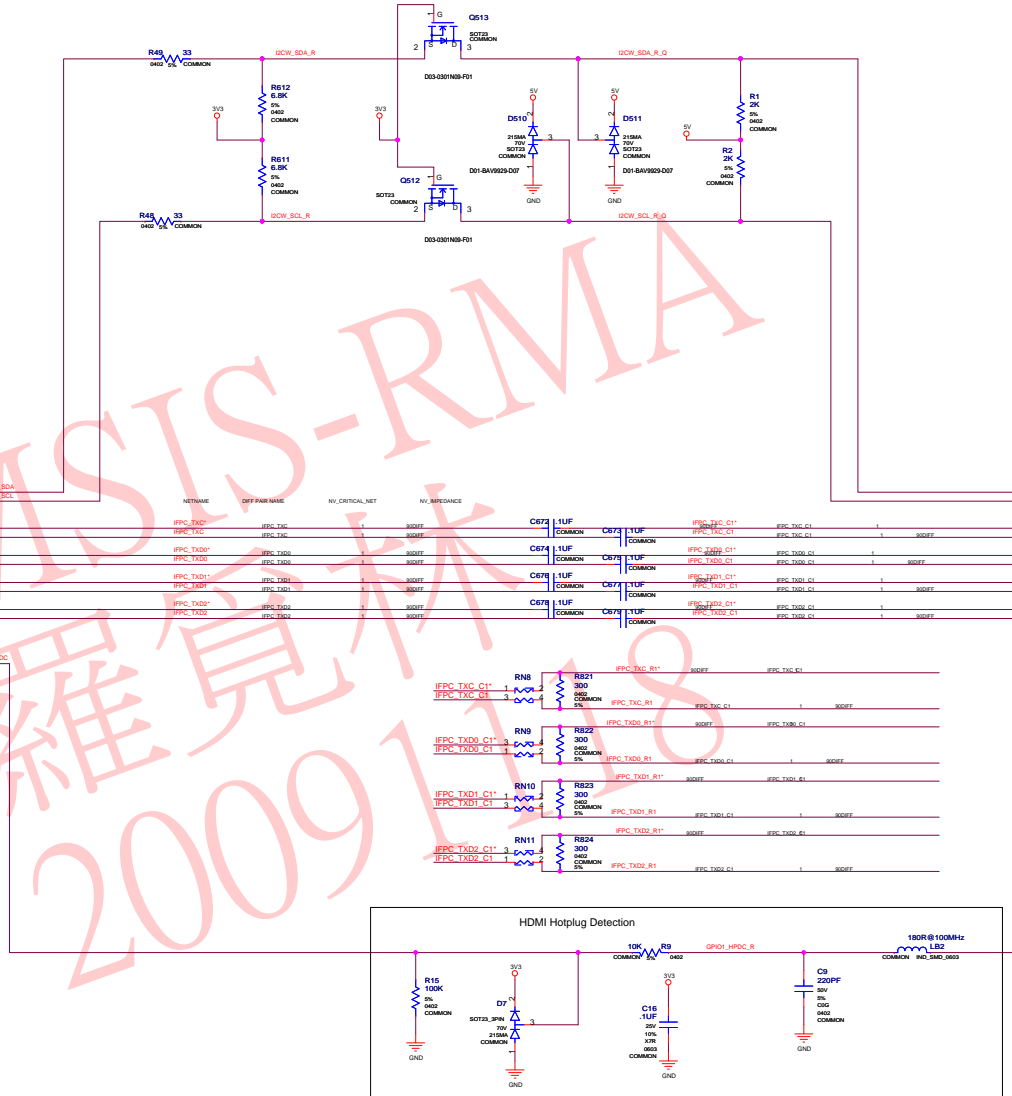
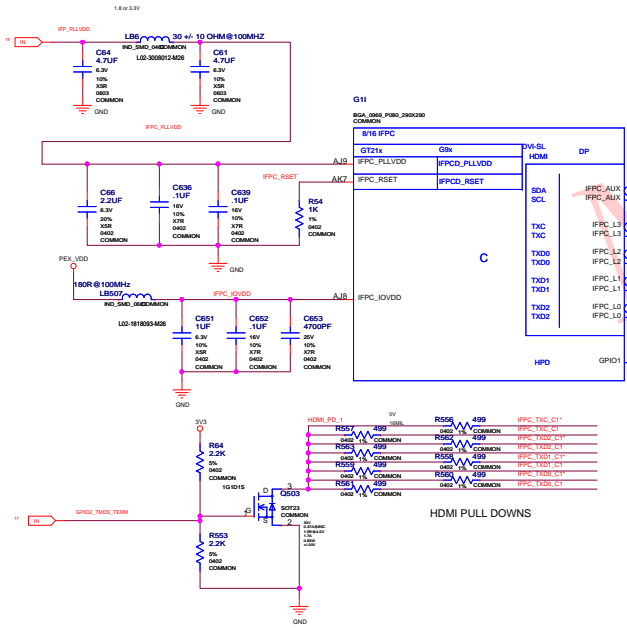
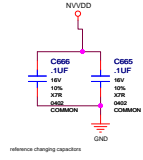
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## IFP C (NORTH HDMI)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP C (NORTH mHDMI)

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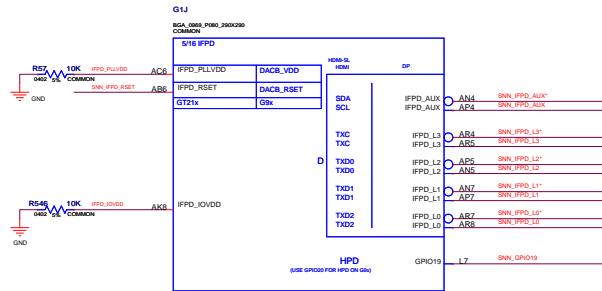
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## IFP D (UNUSED)



AS4	BNN_IPPO_AUX*
	BNN_IPPO_AUX
AB4	BNN_IPPO_L3*
AB5	BNN_IPPO_L3
AP5	BNN_IPPO_L3*
AN5	BNN_IPPO_L3
AN7	BNN_IPPO_L3*
	BNN_IPPO_L3
AB7	BNN_IPPO_L3*
AB8	BNN_IPPO_L3
L7	BNN_GPO19

	NET	PAIR	NV_CRITICAL	IMPEDANCE
1	FPE_AUX_BYP	FPE_AUX_BYP	1	
2	FPE_AUX_BYP*	FPE_AUX_BYP	1	SOIET
3		FPE_AUX_BYP		SOIET

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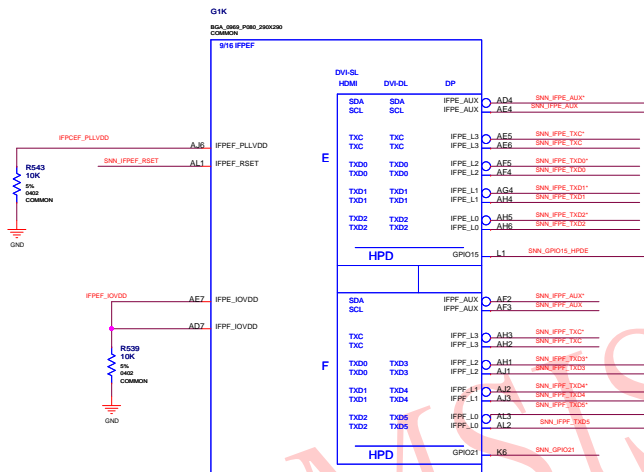
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PAGE DETAIL	IFP D (UNUSED) & MID DISPLAYPORT

## IFP EF (unused)

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PAGE DETAIL	IFP EF (MID DVI-I)

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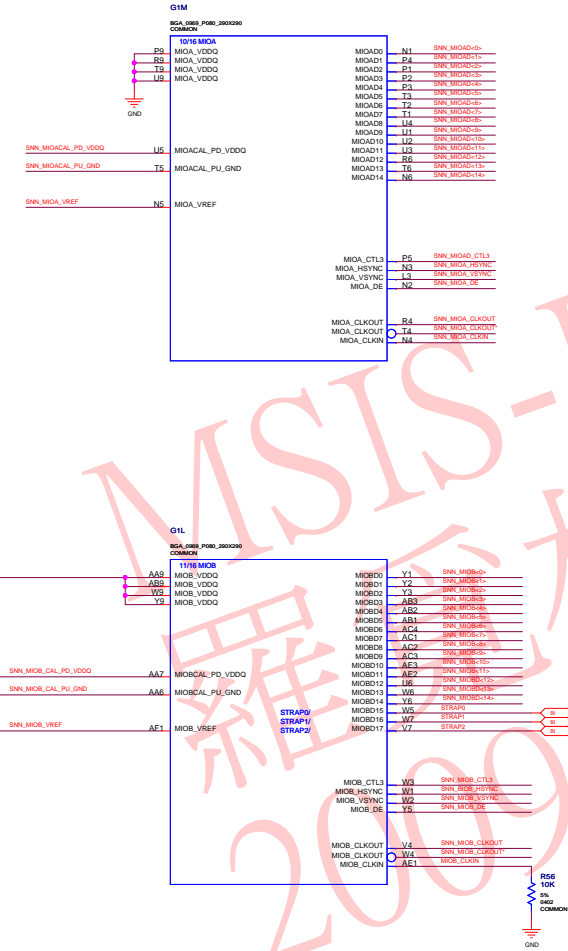
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MIOA & MIOB

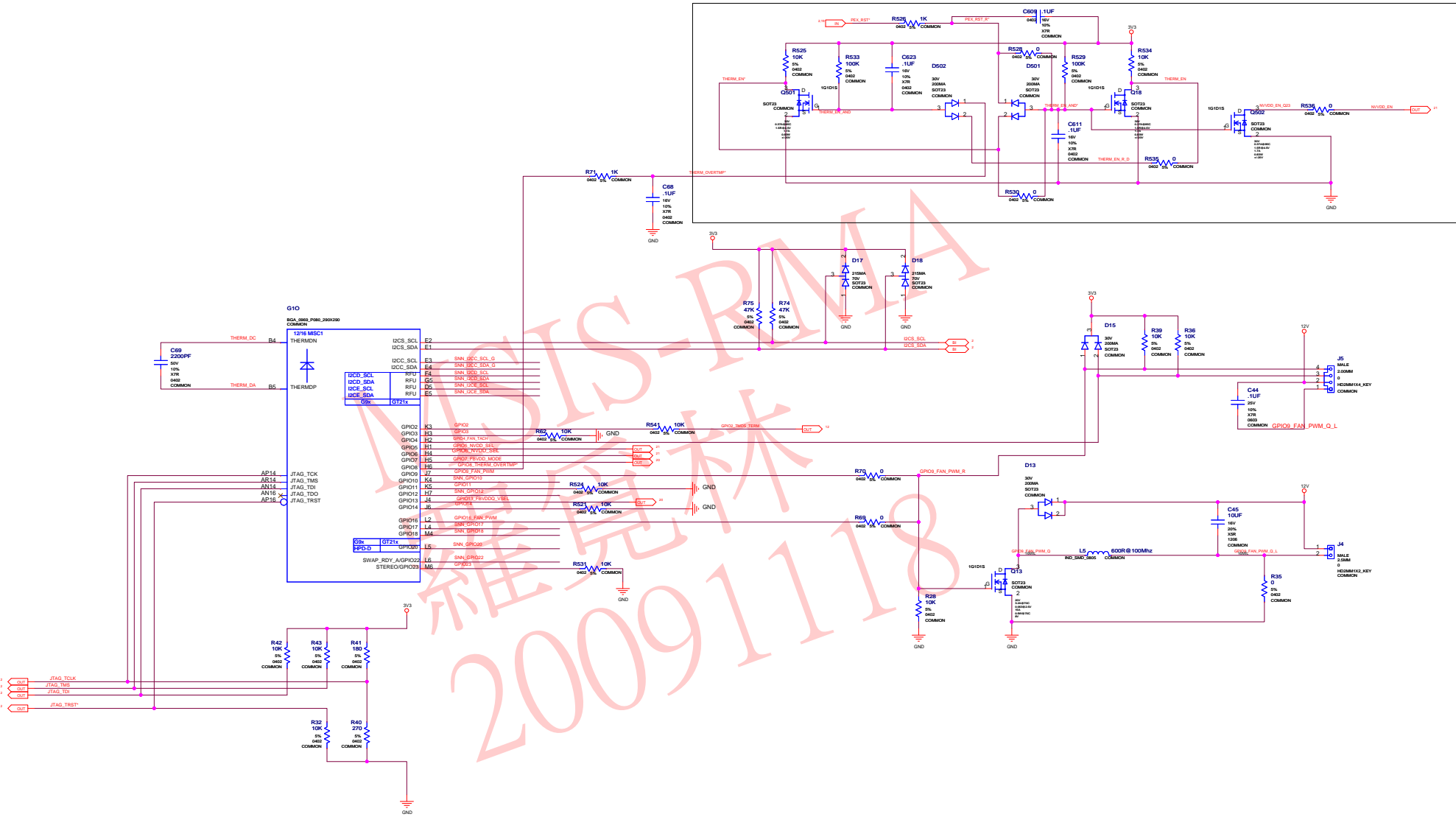


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FAN CONTROL, GPIO, JTAG

OVERTEMP LATCH

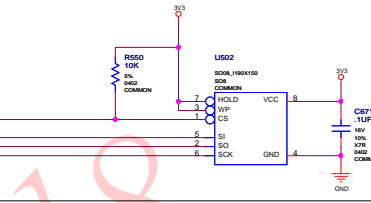
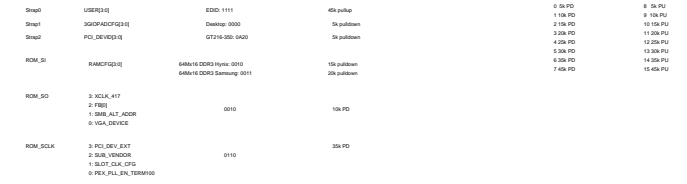


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PAGE/MATERIAL	FAN CONTROL; GPIO; JTAG

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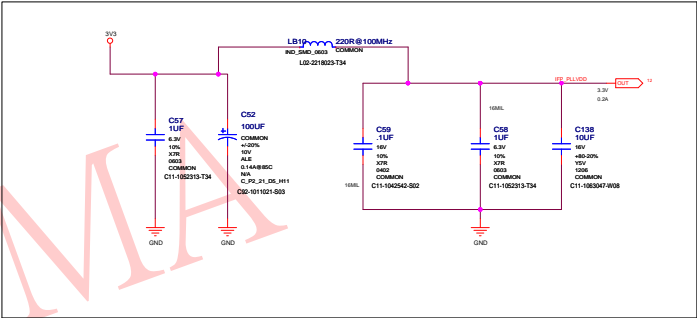
## STRAPPING OPTIONS



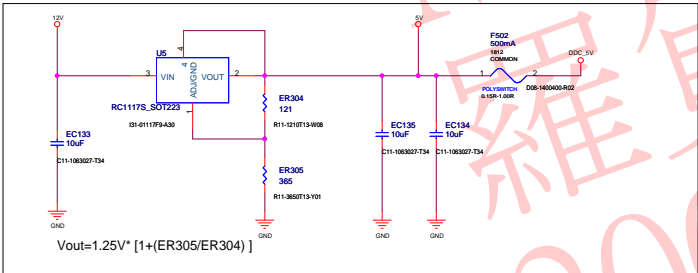
	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION STRAP MODE:	40.2K 1% TO GND	NC
BINARY BRINGUP STRAP MODE:	NC	NC
MULTILEVEL STRAP MODE:	40.2K 1% TO GND	40.2K 1% TO GND

LINEAR POWER SUPPLIES

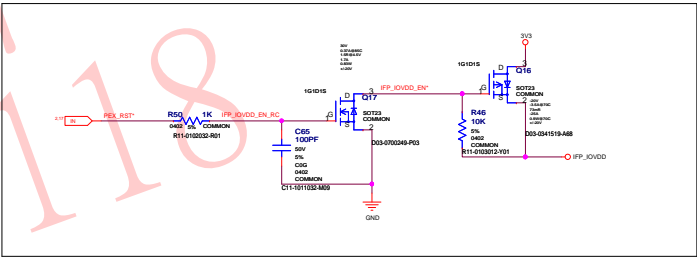
IFP\_PLLVDD SUPPLY



5V & DDC\_5V REGULATOR



IFP\_IOVDD BACKDRIVE PREVENTION



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PAGE DETAIL	LINEAR POWER SUPPLIES

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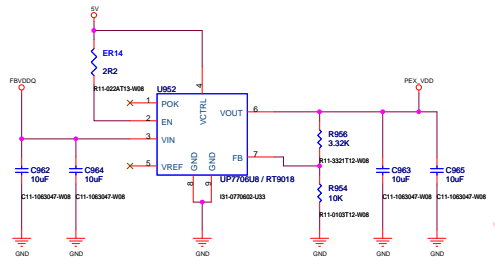
FBVDDQ/PEXVDD POWER SUPPLY

PEX\_VDD = 1.05V @ 2.7A



PEXVDD = 1.05V @ 3A

place in test surface with big pad



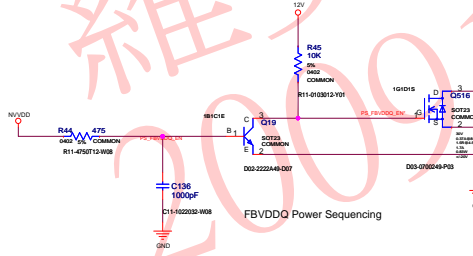
$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$   
 $1.05V = 0.8V * (1 + R574 / R573)$   
 $1.06582V = 0.8V * (1 + 105 / 316)$

**$V_{out}=0.8V * (1 + R956 / R954)$**   
 **$1.0656=0.8V * (1 + 3.32k / 10k)$**

loop = -Vocp / Rds(on) @ Lower MOSFET with 10mohm Rds(on)

Rscp (ohm)	400k	42k	39k	10k
Vocp (mV)	-375	-1300	-285	-155
Rscp (A)	37.5	25	22.5	15

ex : D03-90N031B-114 @ Lower MOSFET with 9mohm Rds(on) 1pcs  
Rscp is 10K then loop is 16.6A @ 16.6 = 150/9



$FBVDDQ = V_{ref} * (1 + R_{top} / R_{bot})$   
 $1.50V = 0.8V * (1 + R570 / R572) @ GPIO13 = 0 [DEFAULT]$   
 $1.51208V = 0.8V * (1 + 1.62k / 1.82k) @ GPIO13 = 0 [DEFAULT]$   
 **$1.512V = 0.8V * (1 + ER12 / ER13)$**   
 **$1.51208V = 0.8V * (1 + 1.62k / 1.82k)$**

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NVDD POWER SUPPLY

loop = - Vccp / Rds(on) @ Lower MOSFET with 10mohm Rds(on)

Rds(on) (mΩ)	42K	20K	10K
Vccp (mV)	-175	-100	-150
loop (A)	37.5	25	32.5

ex.: D03-90N031B-114 @ Lower MOSFET with 9mohm Rds(on) 2pcs  
Rds(on) is 26K then loop is 50A @ 50 = 225(8/9)

$1.0043 = V_{ref} * (1 + ER1686/ER5)$   
 $1.0043 = V_{ref} * (1 + 1.87k / 7.32k)$

NVDD	QF05	QF06	R1	R2	Actual
0.90V	L	L	1.02k	8.02k	0.901V
0.95V	L	H	1.02k	8.02k	0.950V
1.0V	H	L	1.02k	8.02k	1.000V
1.05V	H	H	1.02k	8.02k	1.051V

Net Name	MIN_LINE_WIDTH	VOLTAGE	IV_NET_MAX_CURRENT
NVDD	10MIL	1V	20A

PS_NVDD_VDD5	10MIL
PS_NVDD_VDD10	10MIL
PS_NVDD_VDD15	10MIL
PS_NVDD_BOOT	10MIL
PS_NVDD_LG	10MIL
PS_NVDD_PHASE	10MIL
PS_NVDD_FB	10MIL
PS_NVDD_LG_R	10MIL
PS_NVDD_LG_R	10MIL
PS_NVDD_CP_R1	10MIL
PS_NVDD_CP_R2	10MIL
PS_NVDD_FB_R	10MIL
PS_NVDD_FB	10MIL
PS_NVDD_FB	10MIL
PS_NVDD_FB	10MIL

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