

P727-A01: G96, GB1-128, GDDR3, DL-DVI, DL-DVI/VGA, SD/HDTV

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REV	VARIANT	NPVN	ASSEMBLY
B	BASE	600-10727-0000-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKJ0000	600-10727-0000-100	G96-400, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
2	SKJ0001	600-10727-0001-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
3	SKJ0002	600-10727-0002-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI
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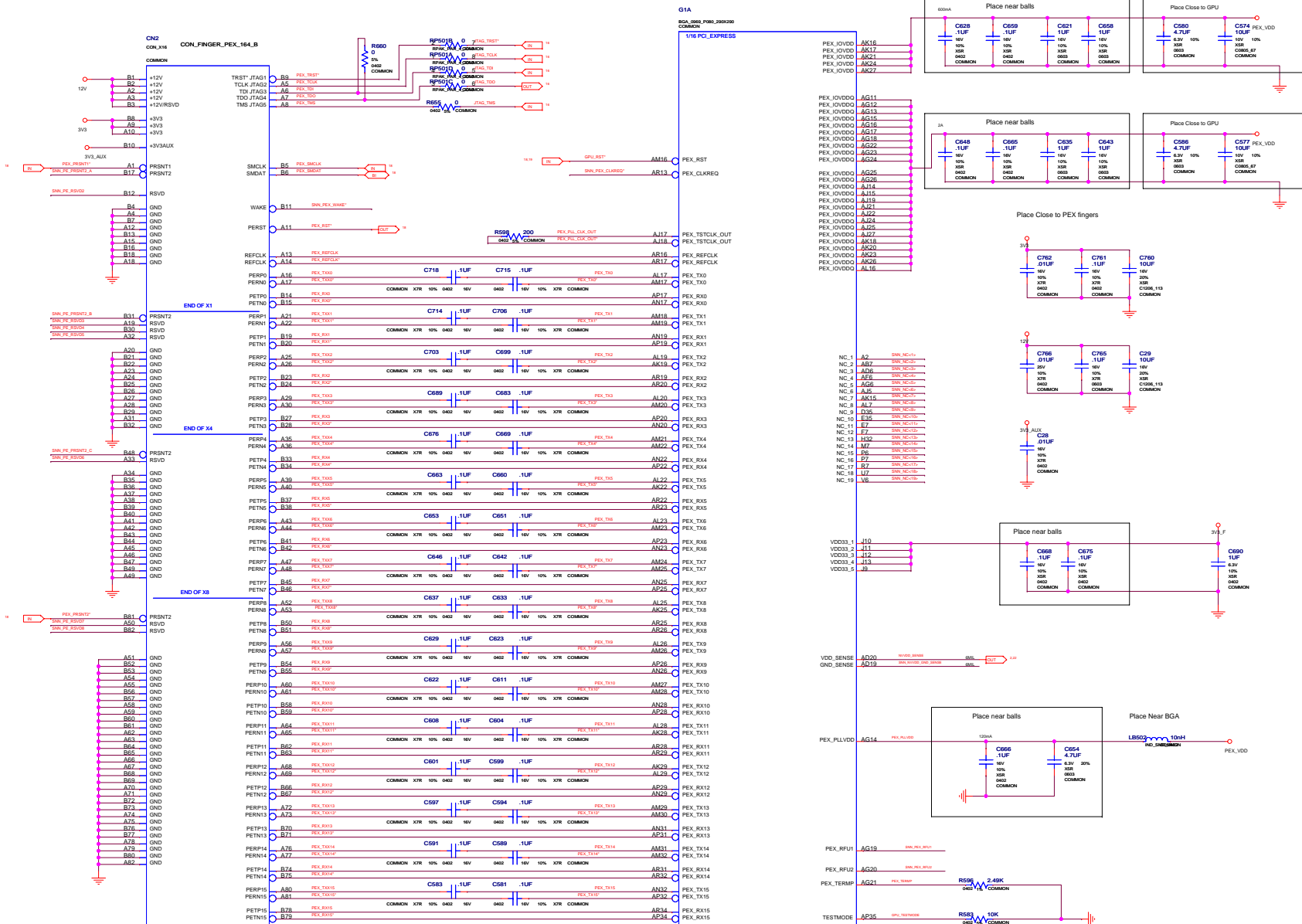
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31-OCT-2009

# 16X PEX INTERFACE



NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL
PEX_RX0	PEX_TX0	10000	1
PEX_RX1	PEX_TX1	10000	1
PEX_RX2	PEX_TX2	10000	1
PEX_RX3	PEX_TX3	10000	1
PEX_RX4	PEX_TX4	10000	1
PEX_RX5	PEX_TX5	10000	1
PEX_RX6	PEX_TX6	10000	1
PEX_RX7	PEX_TX7	10000	1
PEX_RX8	PEX_TX8	10000	1
PEX_RX9	PEX_TX9	10000	1
PEX_RX10	PEX_TX10	10000	1
PEX_RX11	PEX_TX11	10000	1
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PEX_RX15	PEX_TX15	10000	1
PEX_RX16	PEX_TX16	10000	1
PEX_RX17	PEX_TX17	10000	1
PEX_RX18	PEX_TX18	10000	1
PEX_RX19	PEX_TX19	10000	1
PEX_RX20	PEX_TX20	10000	1
PEX_RX21	PEX_TX21	10000	1
PEX_RX22	PEX_TX22	10000	1
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PEX_RX25	PEX_TX25	10000	1
PEX_RX26	PEX_TX26	10000	1
PEX_RX27	PEX_TX27	10000	1
PEX_RX28	PEX_TX28	10000	1
PEX_RX29	PEX_TX29	10000	1
PEX_RX30	PEX_TX30	10000	1
PEX_RX31	PEX_TX31	10000	1
PEX_RX32	PEX_TX32	10000	1
PEX_RX33	PEX_TX33	10000	1
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PEX_RX35	PEX_TX35	10000	1
PEX_RX36	PEX_TX36	10000	1
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PEX_RX45	PEX_TX45	10000	1
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PEX_RX51	PEX_TX51	10000	1
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PEX_RX81	PEX_TX81	10000	1
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PEX_RX88	PEX_TX88	10000	1
PEX_RX89	PEX_TX89	10000	1
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PEX_RX91	PEX_TX91	10000	1
PEX_RX92	PEX_TX92	10000	1
PEX_RX93	PEX_TX93	10000	1
PEX_RX94	PEX_TX94	10000	1
PEX_RX95	PEX_TX95	10000	1
PEX_RX96	PEX_TX96	10000	1
PEX_RX97	PEX_TX97	10000	1
PEX_RX98	PEX_TX98	10000	1
PEX_RX99	PEX_TX99	10000	1

1.0	NVDD0_SENSE	0.2V
1.0	NVDD0_SENSE	0V
1.0	PEX_PL1VDD	1.00V 1.2V
1.0	PEX_PL1VDD	1.00V 1.2V
1.0	PEX_PL1VDD	1.00V 1.2V

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PAGE DETAIL	PCI EXPRESS INTERFACE; PEX_VDD DECOUPLING CAPS



# FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3

FB\_A-CS0-LOW-32bit

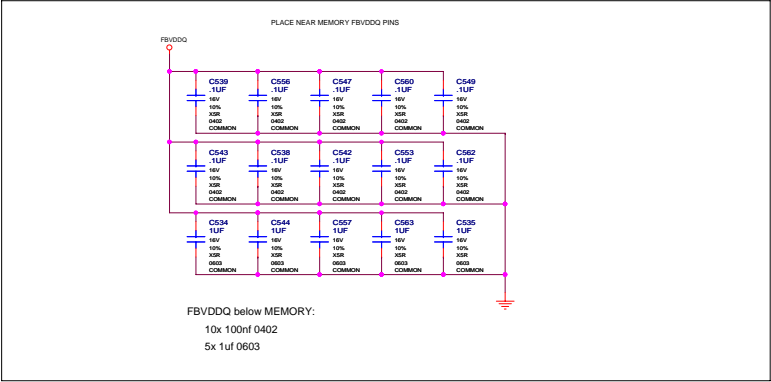
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FBA Partition

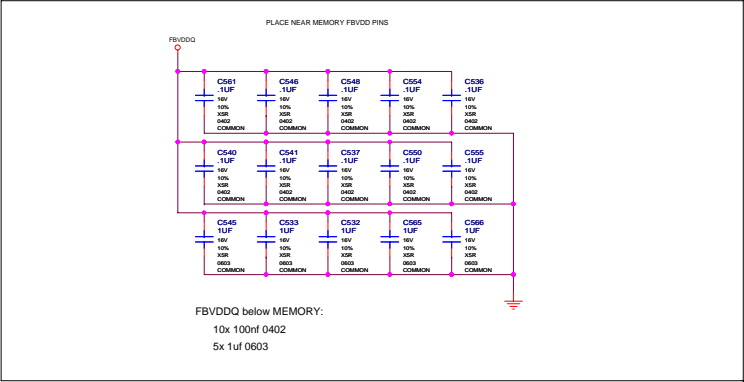
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QMC485	BA484*
QMC486	BA485*
QMC487	BA486*
QMC488	BA487*
QMC489	BA488*
QMC490	BA489*
QMC491	BA490*
QMC492	BA491*
QMC493	BA492*
QMC494	BA493*
QMC495	BA494*
QMC496	BA495*
QMC497	BA496*
QMC498	BA497*
QMC499	BA498*
QMC500	BA499*
QMC501	BA500*
QMC502	BA501*
QMC503	BA502*
QMC504	BA503*
QMC505	BA504*
QMC506	BA505*
QMC507	BA506*
QMC508	BA507*
QMC509	BA508*
QMC510	BA509*
QMC511	BA510*
QMC512	BA511*
QMC513	BA512*
QMC514	BA513*

# FRAME BUFFER: PARTITION A DECOUPLING

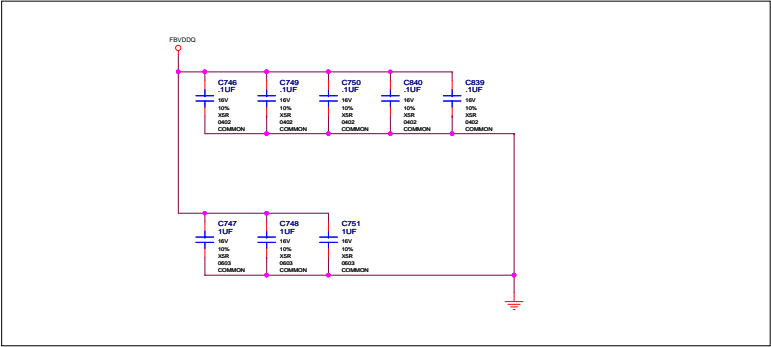
Decoupling for FBA 0..31



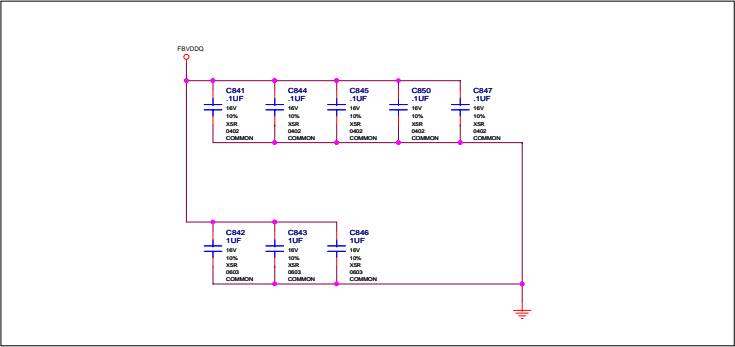
Decoupling for FBA 32..63



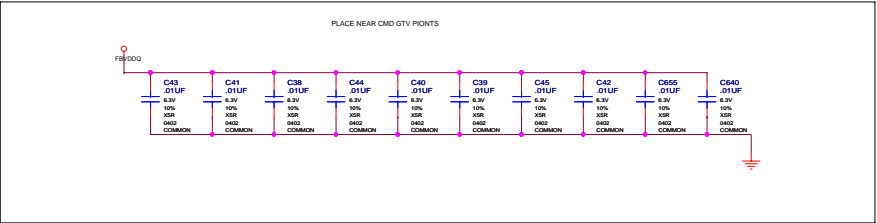
Decoupling for FBA A1 0..31



Decoupling for FBA A1 0..31



Return path coupling GND/FBVDDQ for FBA



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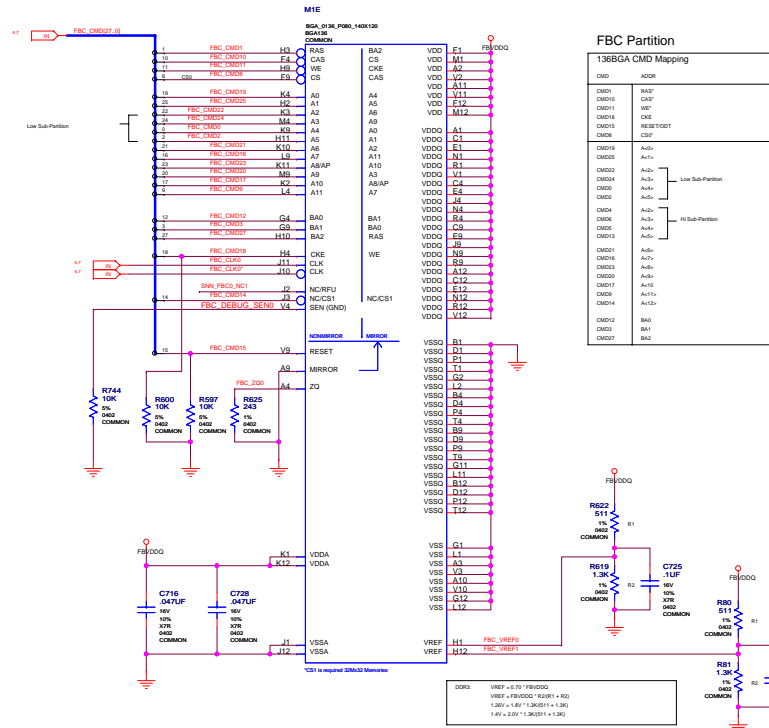
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

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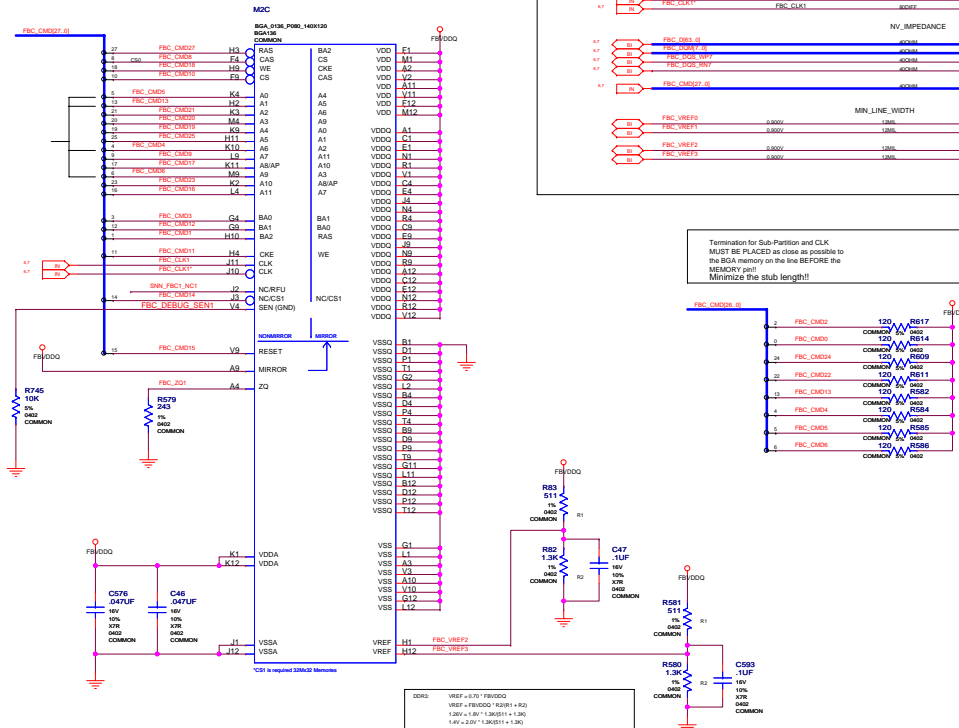


# FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3

FB\_C-CS0-LOW-32bit

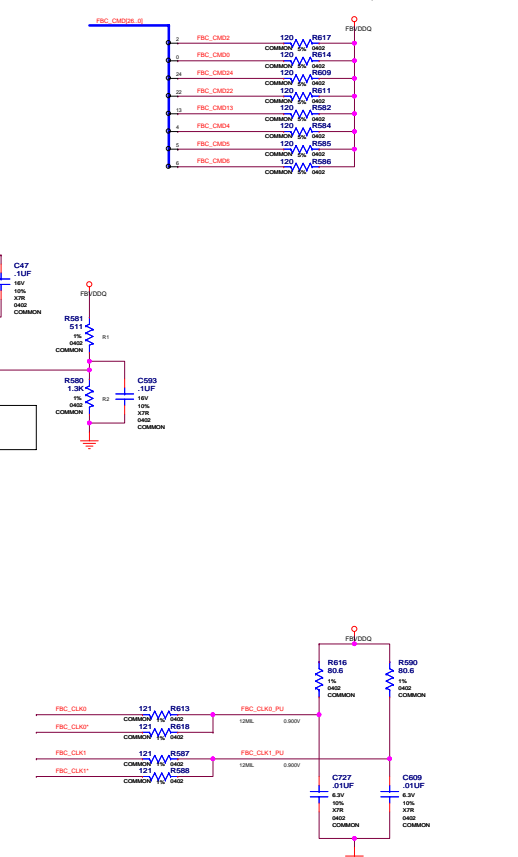


FB\_C-CS0-HI-32bit

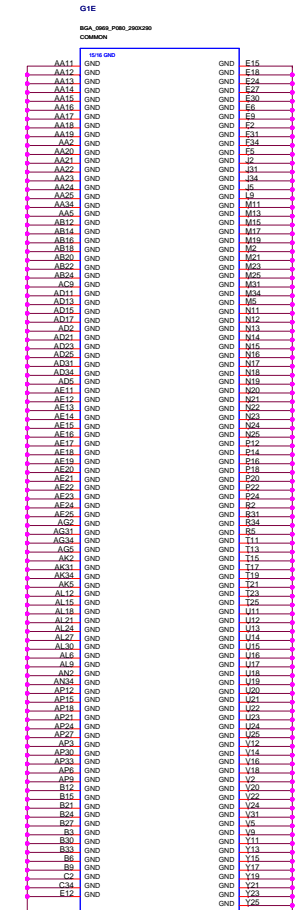
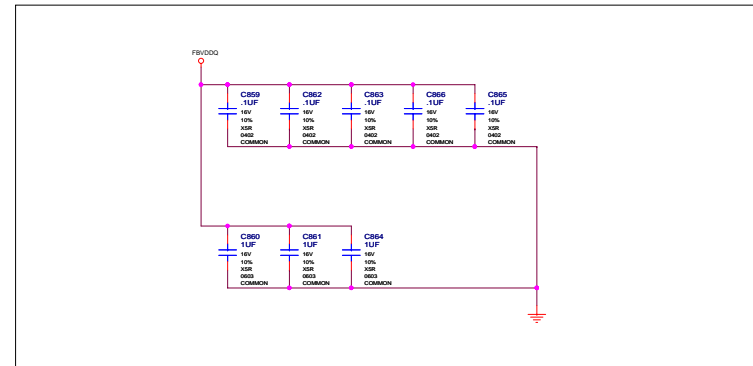
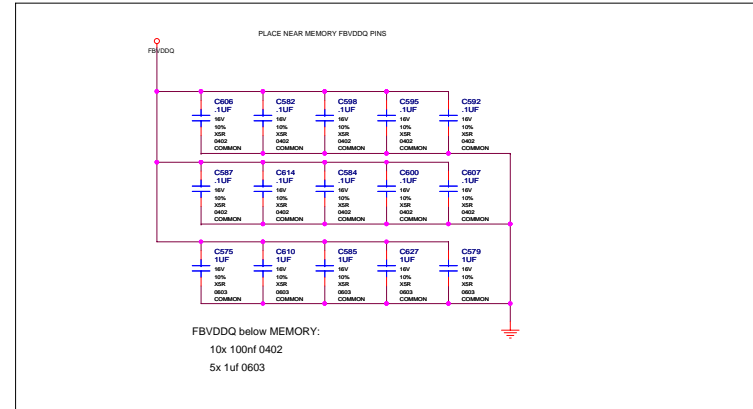
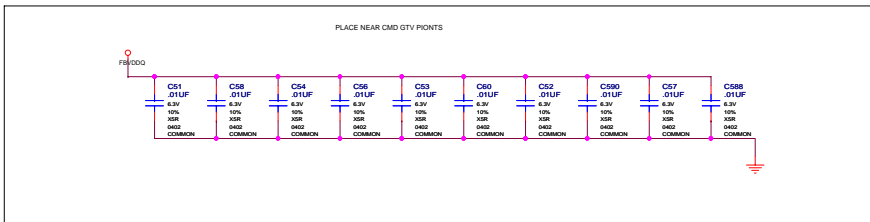
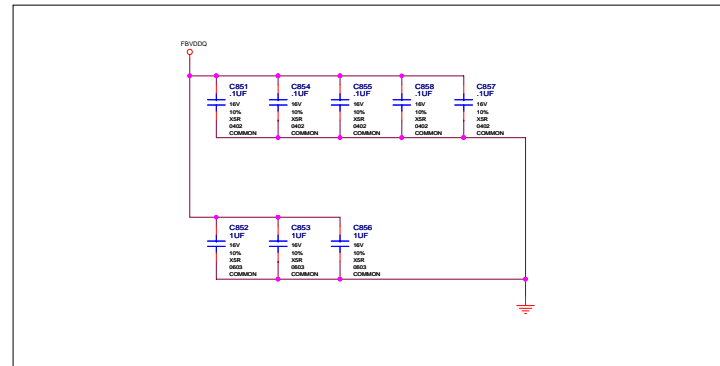
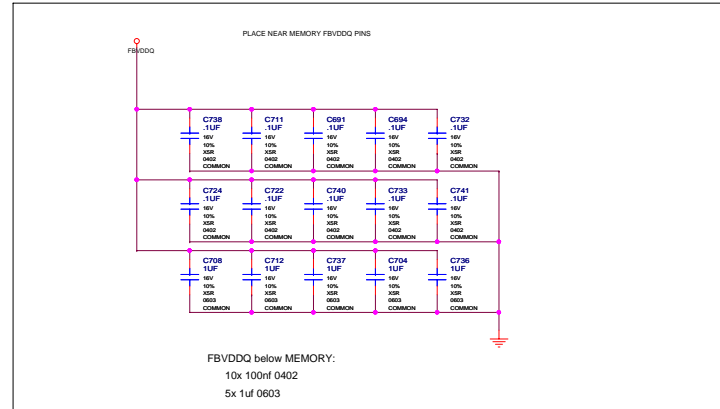


NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
FBC_CMD0	FBC_CMD0	800FT	1
FBC_CMD1	FBC_CMD1	800FT	1
FBC_CMD2	FBC_CMD2	800FT	1
FBC_CMD3	FBC_CMD3	800FT	1
FBC_CMD4	FBC_CMD4	800FT	1
FBC_CMD5	FBC_CMD5	800FT	1
FBC_CMD6	FBC_CMD6	800FT	1
FBC_CMD7	FBC_CMD7	800FT	1
FBC_CMD8	FBC_CMD8	800FT	1
FBC_CMD9	FBC_CMD9	800FT	1
FBC_CMD10	FBC_CMD10	800FT	1
FBC_CMD11	FBC_CMD11	800FT	1
FBC_CMD12	FBC_CMD12	800FT	1
FBC_CMD13	FBC_CMD13	800FT	1
FBC_CMD14	FBC_CMD14	800FT	1
FBC_CMD15	FBC_CMD15	800FT	1

Termination for Sub-Partition and CLK MUST BE PLACED as close as possible to the BGA memory on the line BEFORE the MEMORY pin!  
Minimize the stub length!




## Decoupling for FBC 0..31



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS, GPU GND CONNECTIONS

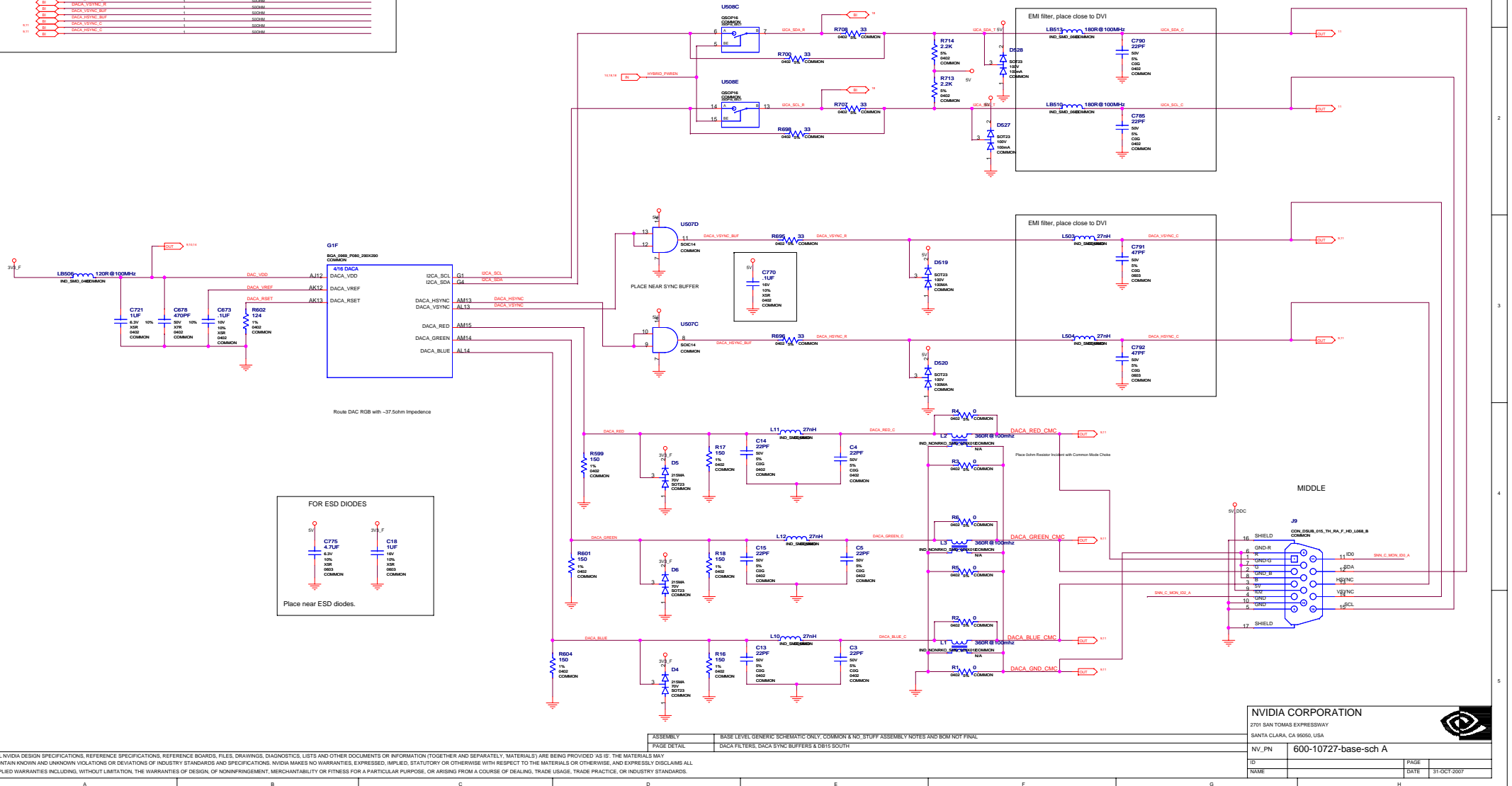
<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
<b>NV_PN</b> 600-10727-base-sch A			
<b>ID</b>		<b>PAGE</b>	
<b>NAME</b>		<b>DATE</b>	31-OCT-2007



## Primary Display (DACA), DVI-I

## DACA RGB-FILTER

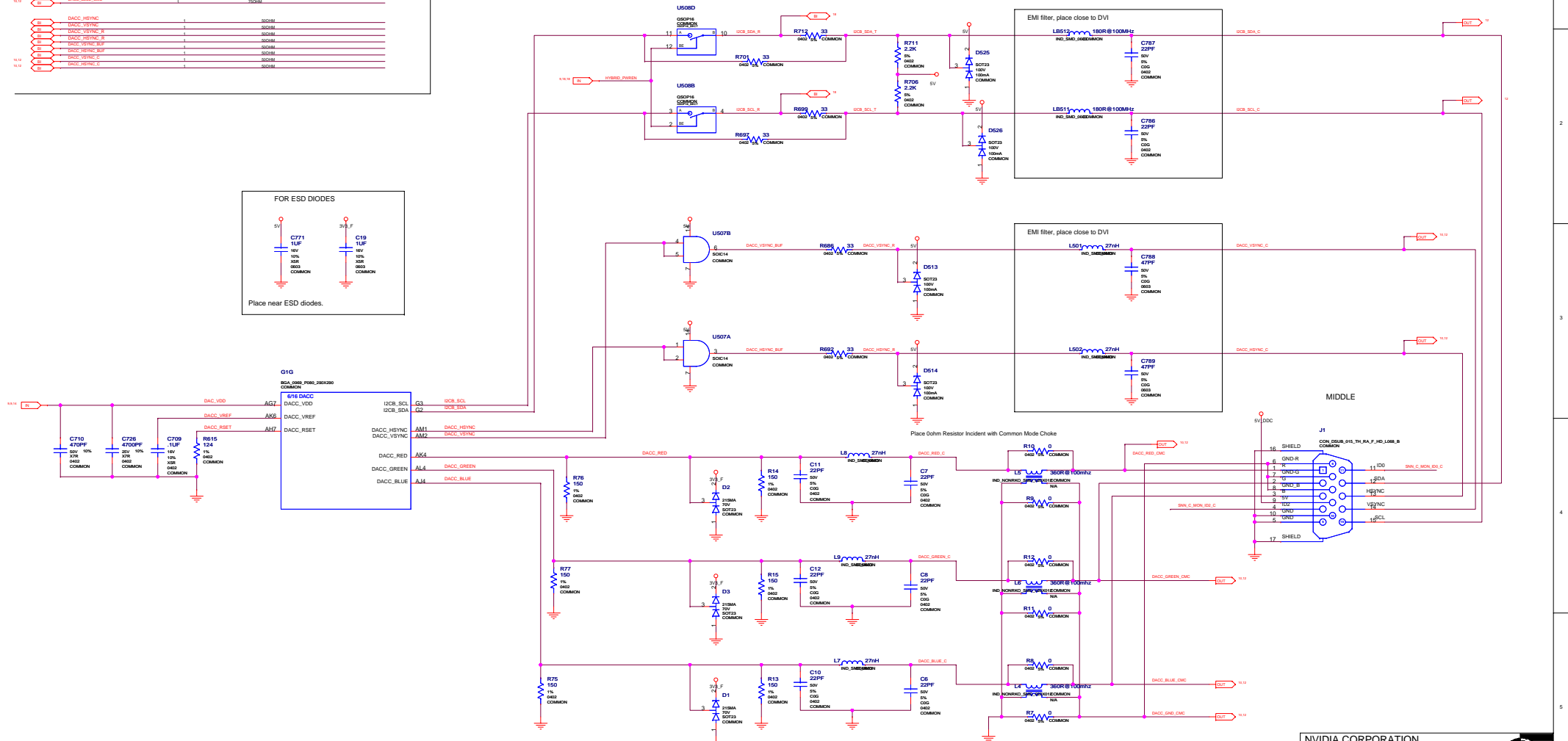
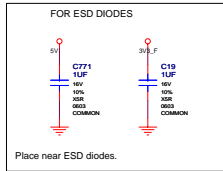
NET_NAME	INV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACA_VDD		3.3V	120u
DACA_VREF			120u
DACA_VREF			120u
DACA_RED		750m	
DACA_GREEN		750m	
DACA_BLUE		750m	
DACA_RED_C		750m	
DACA_GREEN_C		750m	
DACA_BLUE_C		750m	
DACA_GND_CMC			20
DACA_RED_CMC		750m	
DACA_GREEN_CMC		750m	
DACA_BLUE_CMC		750m	
DACA_HSYNC		500m	
DACA_VSYNC		500m	
DACA_VSYNC_B		500m	
DACA_VSYNC_R		500m	
DACA_VSYNC_G		500m	
DACA_VSYNC_C		500m	
DACA_HSYNC_C		500m	




## Secondary Display (DACC), Slim DB15

## DACC RGB-FILTER

NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACC_VREF		120Ω	120Ω
DACC_VREF		120Ω	120Ω
DACC_RED		120Ω	120Ω
DACC_GREEN		120Ω	120Ω
DACC_BLUE		120Ω	120Ω
DACC_RED_C		120Ω	120Ω
DACC_GREEN_C		120Ω	120Ω
DACC_BLUE_C		120Ω	120Ω
DACC_GND_CMC		0V	120Ω
DACC_RED_CMC		120Ω	120Ω
DACC_GREEN_CMC		120Ω	120Ω
DACC_BLUE_CMC		120Ω	120Ω
DACC_HSYNC		120Ω	120Ω
DACC_VSYNC		120Ω	120Ω
DACC_VSYNC_P		120Ω	120Ω
DACC_VSYNC_N		120Ω	120Ω
DACC_VSYNC_SEF		120Ω	120Ω
DACC_VSYNC_SEF		120Ω	120Ω
DACC_VSYNC_C		120Ω	120Ω
DACC_VSYNC_C		120Ω	120Ω

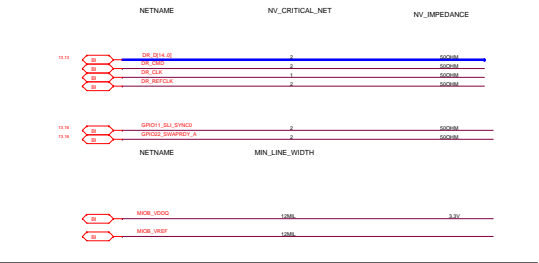
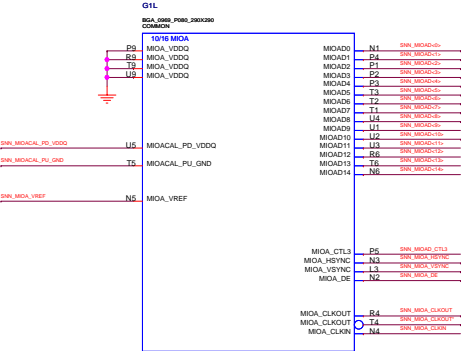


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<b>NV_PN</b> 600-10727-base-sch A			
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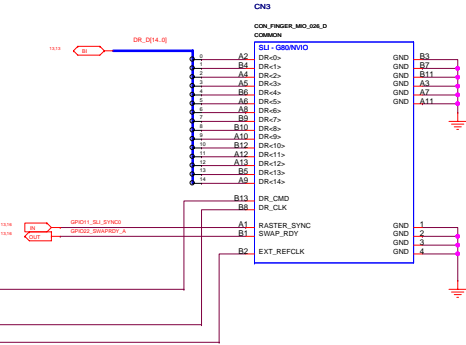
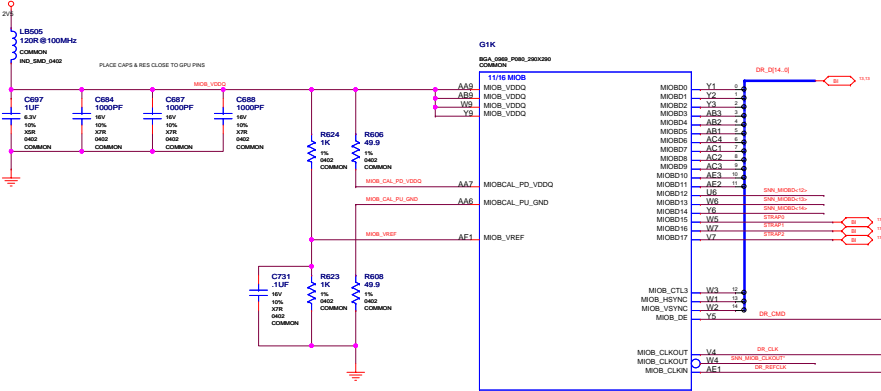
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MIOA/B SLI



SLI Connector



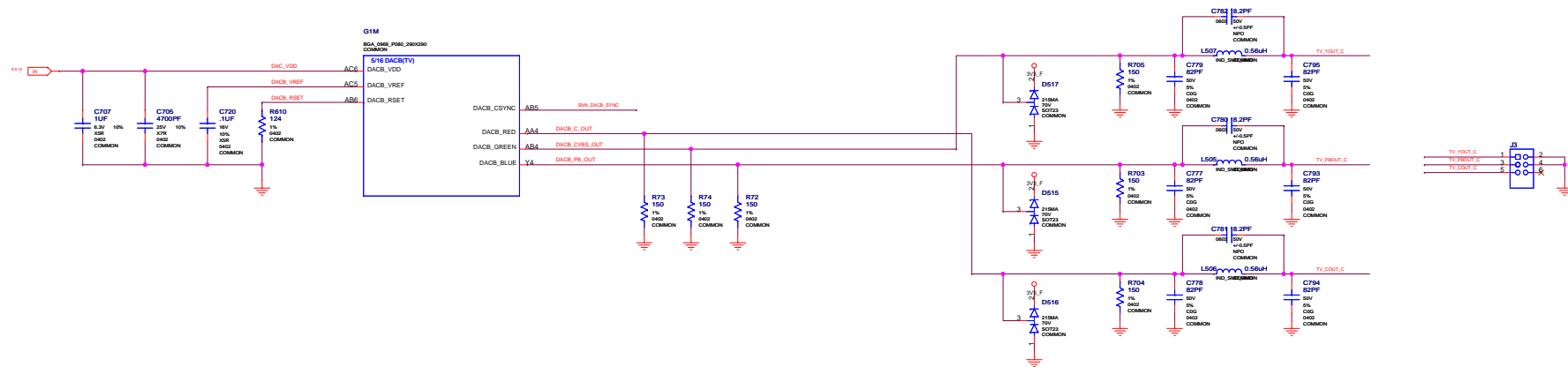
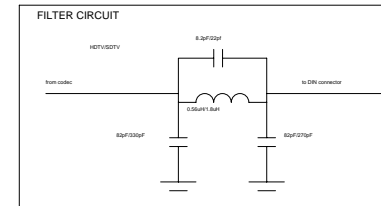
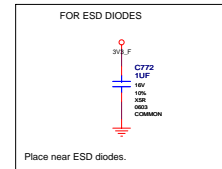
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB SLI CONNECTOR

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DACB: SD/HD VIDEO OUT CONNECTOR

	NET_NAME	MIN_LINE_WIDTH	NY_IMPEDANCE	NY_CRESTAL_NET
Q11	DACB_C_OUT		750HM	1
Q12	EDOTDOWEL_COUT		750HM	1
Q13	WACB_PNE_COUT		750HM	1
Q14				
Q1	TY_PNEUT_C		750HM	1
Q2	TY_PNEUT_C		750HM	1
Q3	TY_PNEUT_C		750HM	1
Q4				
Q5	DACB_VREF	100M		
Q6	DACB_VREF	100M		



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, MINIDIN CONNECTOR NORTH, SD/HD VIDEO OUTPUT CONNECTOR

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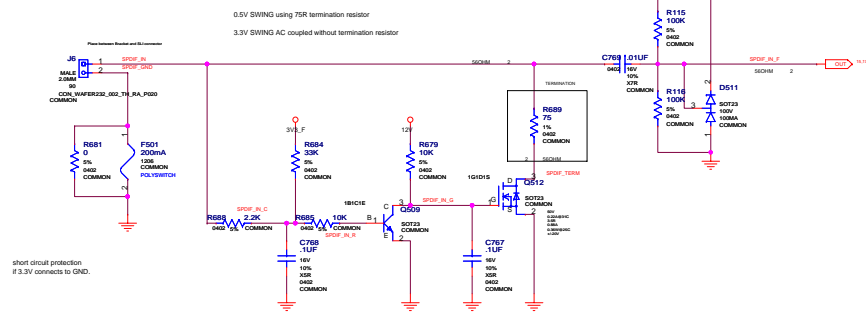


NV_PN	600-10727-base-sch A
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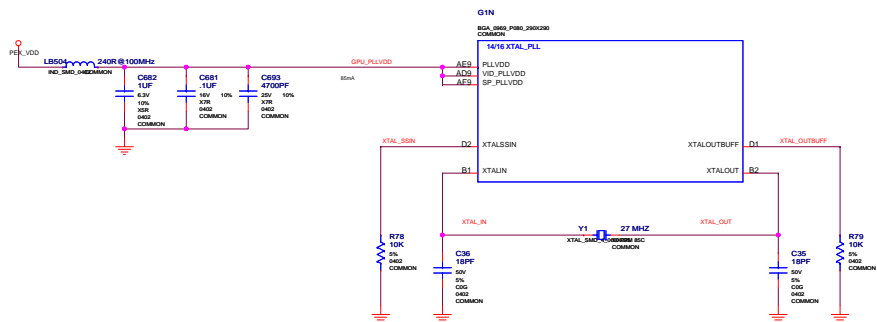
ID		PAGE	
NAME		DATE	31-OCT-2007

## XTAL/PLLVD/SPDIF IN

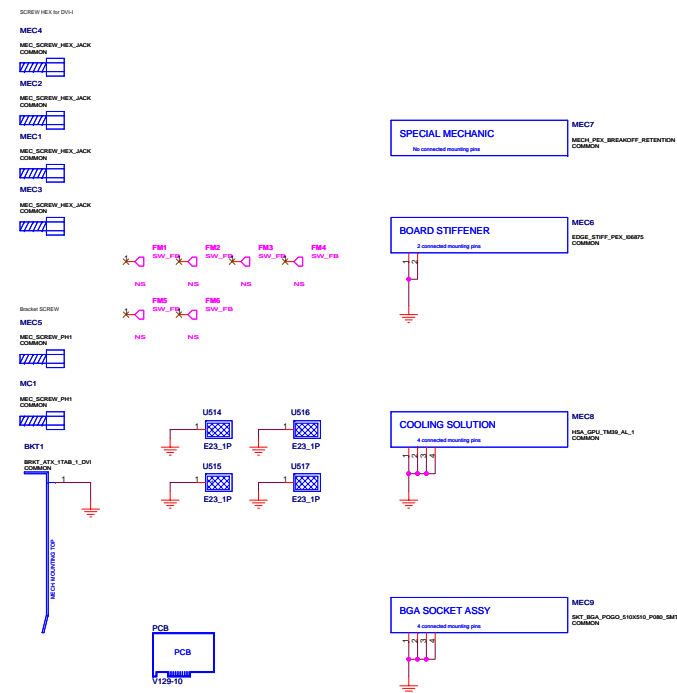
## SPDIF IN



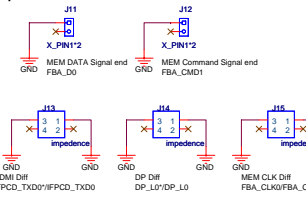
## XTAL/GPU\_PLLVDD



## MECHANICALS & THERMALS



Impedance control line



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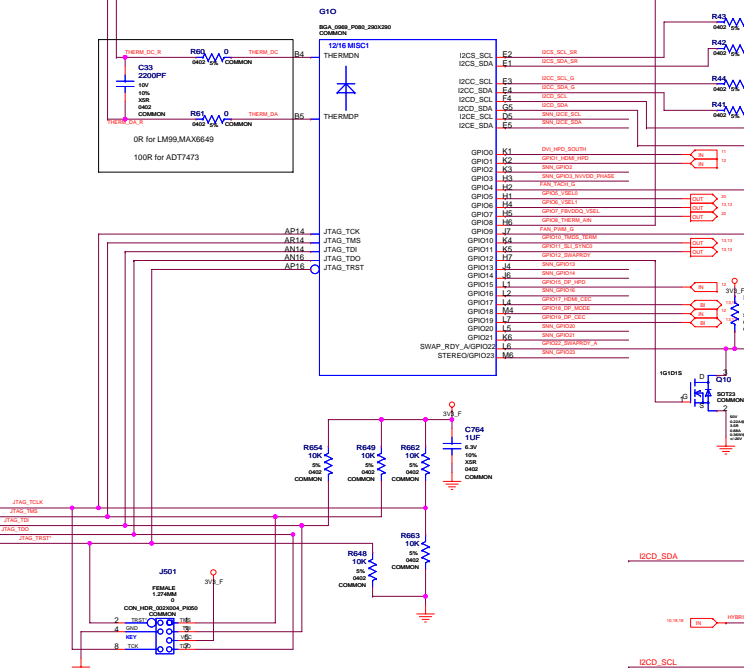
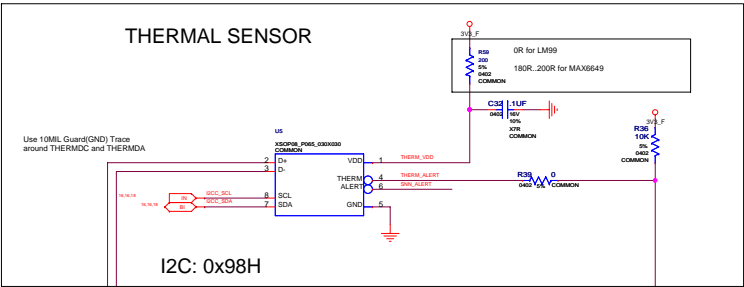


NV_PN	600-10727-base-sch A
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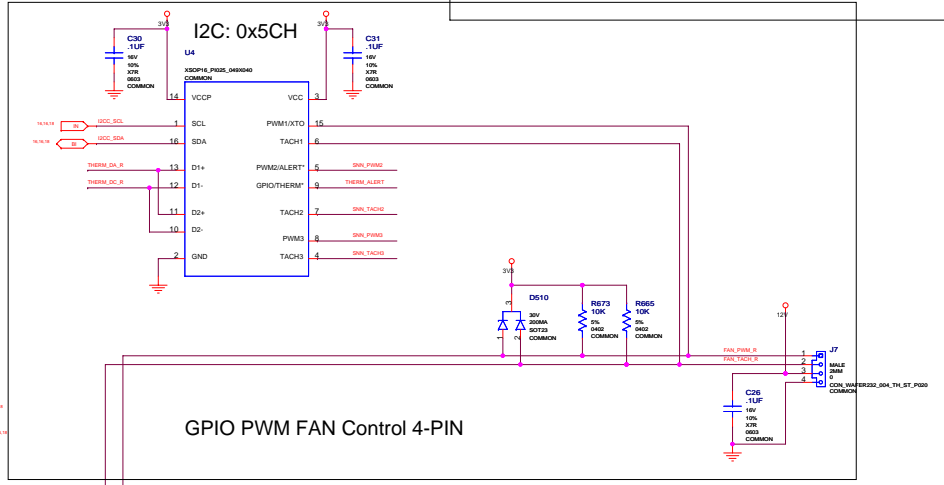
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NAME		DATE	31-OCT-2007

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF-IN, XTAL, MECHANICALS, THERMALS



**THERMAL SENSOR, FAN CONTROLLER**  
uses 3V3: always on.



NETNAME	MIN_LINE_WIDTH	VOLTAGE
THERMDC	10MIL	3V3
THERMDA	10MIL	3V3
THERMDC	10MIL	3V3
THERMDA	10MIL	3V3
THERMDC	10MIL	3V3
THERMDA	10MIL	3V3

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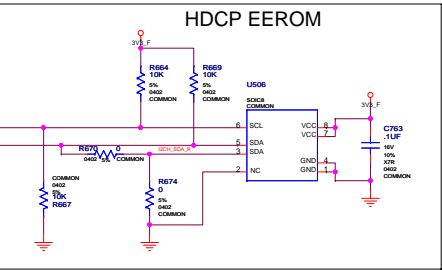
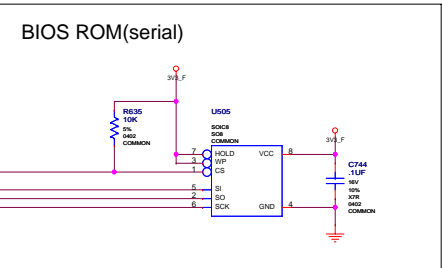
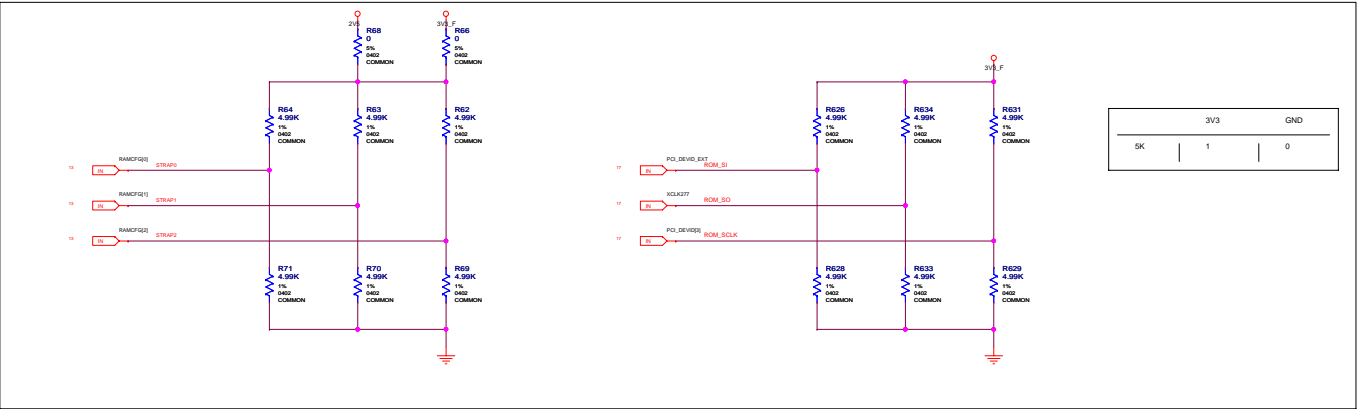
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 310FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	EXTERNAL THERMAL SENSOR, 4PIN FAN CONTROL, GPIO

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STRAPPING OPTIONS

Assembly: BIOS



NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
HDA_BCLK		50ohm	
HDA_RST		50ohm	
HDA_SDI		50ohm	
HDA_SDO		50ohm	
HDA_SYNC		50ohm	

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ASSEMBLY	BIOS ROM (serial)
PAGE DETAIL	BIOS ROM (serial) STRAPPING OPTIONS

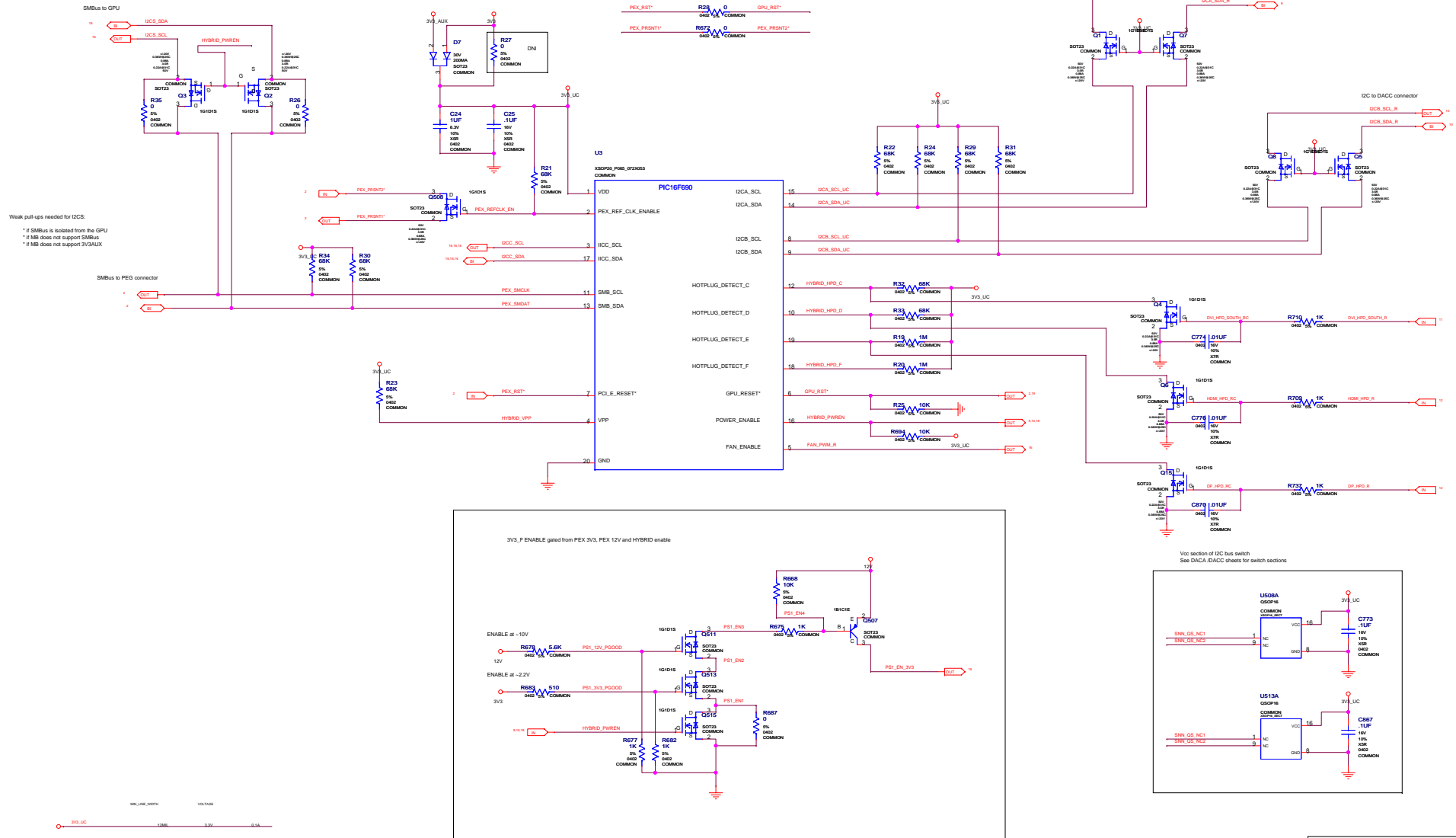
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NV_PN	600-10727-base-sch A
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## HYBRID POWER

Per Datasheet:

Vf = 400mV at 10mA  
\* expected current < 2mA

Stuff only to bypass the micro-controller



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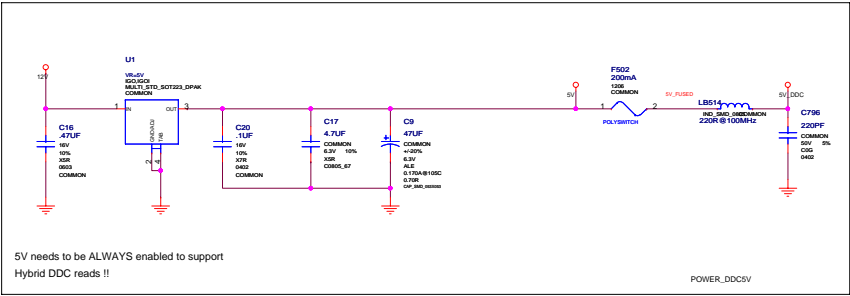
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	HYBRID POWER CIRCUIT

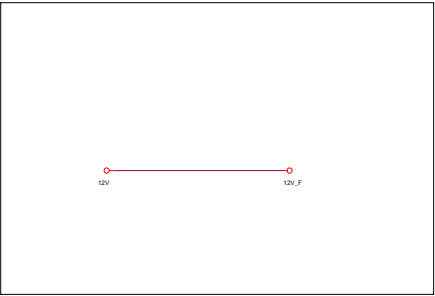
Power Supply: 5V, 5V\_DDC, TMDS, MIOA\_VDDQ

5V REGULATOR



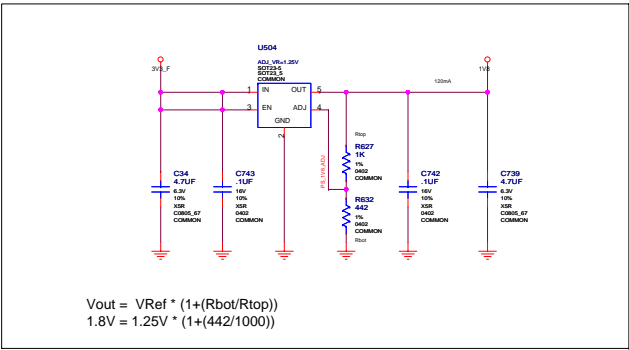
5V DDC

12V filter

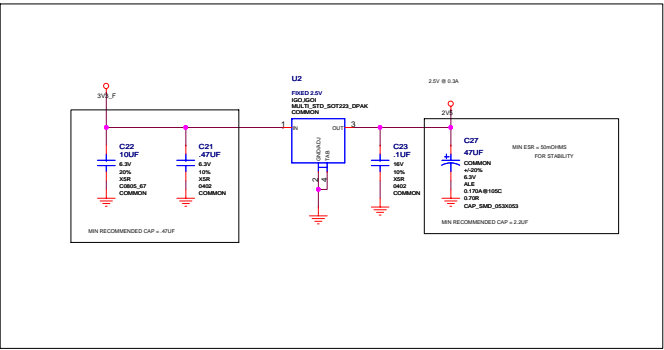


NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	0.1A	120u	5V
5V_DDC	0.1A	120u	5V
5V	0.1A	120u	5V
PL1_V16_ADJ	0.1A	120u	1.8V
1V8	0.1A	120u	1.8V
2V5	0.1A	120u	2.5V
2V5	0.1A	120u	2V
2V5_F	0.1A	120u	2.5V
2V5_F	0.1A	120u	2.5V
12V_F	0.1A	120u	12V

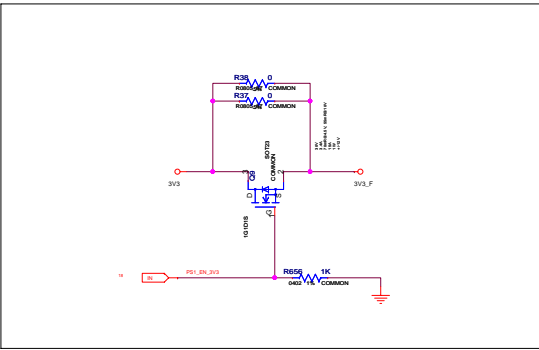
IFP PLL Supply 1.8V



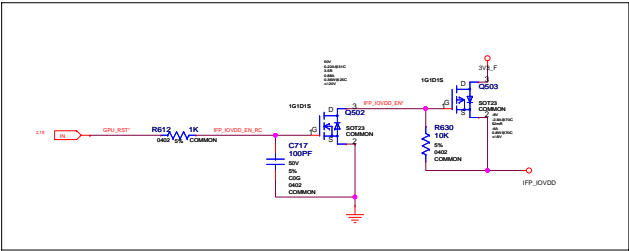
MIO\_VDD 2.5V



3V3 switch



IFP\_IOVDD BACKDRIVE PREVENTION



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 3100FF ASSEMBLY NOTES AND BOARD NOT FINAL
PAGE DETAIL	POWER SUPPLY LINEARS: 5V, DDC5V, IFPPLLVD, IFP10VDD, MIO_VDD, 3V3 FILTER, 12V FILTER

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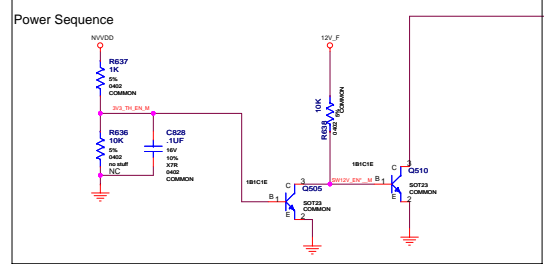
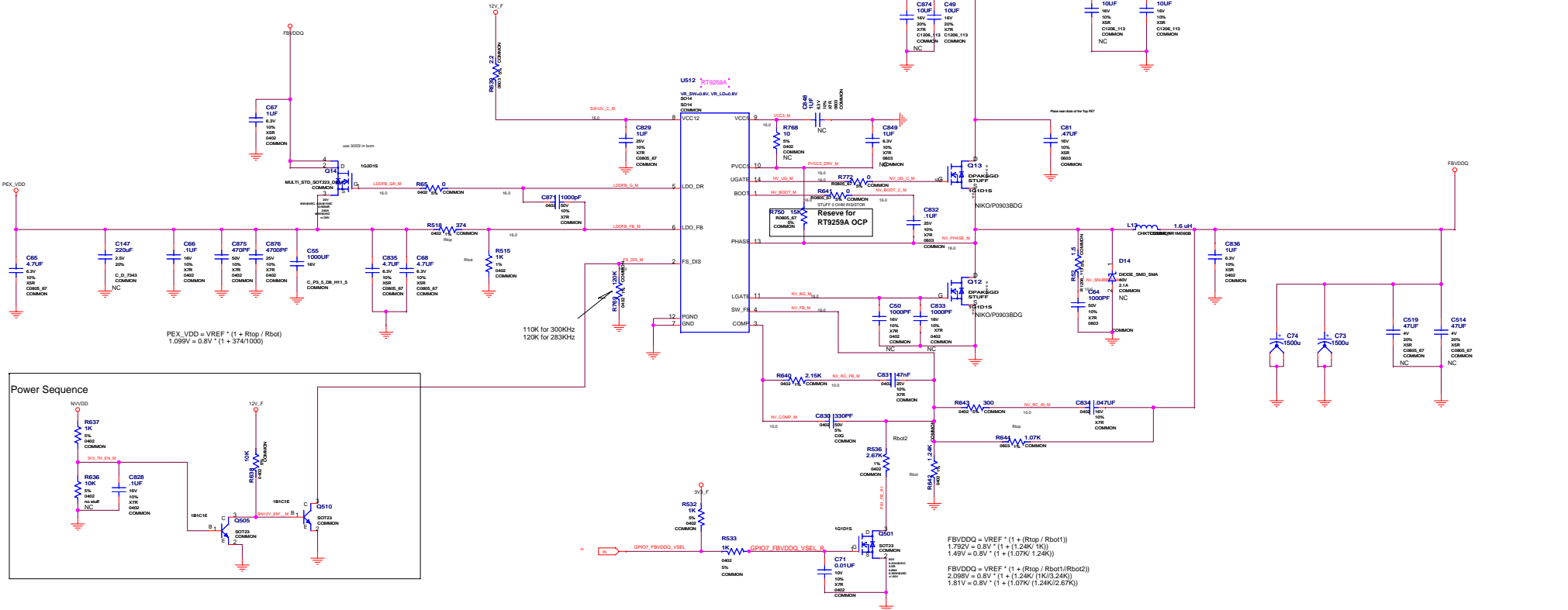
POWER SUPPLY: FBVDD/Q

NET	MIN_LENGTH	VOLTAGE	WIRE_CURRENT
FBVDDQ	12000	1.2V	15A
PEX_VDD	12000	1.2V	15A
PEX_VDD00T_0	12000	1.2V	15A
PEX_VDD00T_1	12000	1.2V	15A
PEX_VDD00T_2	12000	1.2V	15A
PEX_VDD00T_3	12000	1.2V	15A
PEX_VDD00T_4	12000	1.2V	15A
PEX_VDD00T_5	12000	1.2V	15A
PEX_VDD00T_6	12000	1.2V	15A
PEX_VDD00T_7	12000	1.2V	15A
PEX_VDD00T_8	12000	1.2V	15A
PEX_VDD00T_9	12000	1.2V	15A
PEX_VDD00T_10	12000	1.2V	15A
PEX_VDD00T_11	12000	1.2V	15A
PEX_VDD00T_12	12000	1.2V	15A
PEX_VDD00T_13	12000	1.2V	15A
PEX_VDD00T_14	12000	1.2V	15A
PEX_VDD00T_15	12000	1.2V	15A
PEX_VDD00T_16	12000	1.2V	15A
PEX_VDD00T_17	12000	1.2V	15A
PEX_VDD00T_18	12000	1.2V	15A
PEX_VDD00T_19	12000	1.2V	15A
PEX_VDD00T_20	12000	1.2V	15A
PEX_VDD00T_21	12000	1.2V	15A
PEX_VDD00T_22	12000	1.2V	15A
PEX_VDD00T_23	12000	1.2V	15A
PEX_VDD00T_24	12000	1.2V	15A
PEX_VDD00T_25	12000	1.2V	15A
PEX_VDD00T_26	12000	1.2V	15A
PEX_VDD00T_27	12000	1.2V	15A
PEX_VDD00T_28	12000	1.2V	15A
PEX_VDD00T_29	12000	1.2V	15A
PEX_VDD00T_30	12000	1.2V	15A
PEX_VDD00T_31	12000	1.2V	15A
PEX_VDD00T_32	12000	1.2V	15A
PEX_VDD00T_33	12000	1.2V	15A
PEX_VDD00T_34	12000	1.2V	15A
PEX_VDD00T_35	12000	1.2V	15A
PEX_VDD00T_36	12000	1.2V	15A
PEX_VDD00T_37	12000	1.2V	15A
PEX_VDD00T_38	12000	1.2V	15A
PEX_VDD00T_39	12000	1.2V	15A
PEX_VDD00T_40	12000	1.2V	15A
PEX_VDD00T_41	12000	1.2V	15A
PEX_VDD00T_42	12000	1.2V	15A
PEX_VDD00T_43	12000	1.2V	15A
PEX_VDD00T_44	12000	1.2V	15A
PEX_VDD00T_45	12000	1.2V	15A
PEX_VDD00T_46	12000	1.2V	15A
PEX_VDD00T_47	12000	1.2V	15A
PEX_VDD00T_48	12000	1.2V	15A
PEX_VDD00T_49	12000	1.2V	15A
PEX_VDD00T_50	12000	1.2V	15A
PEX_VDD00T_51	12000	1.2V	15A
PEX_VDD00T_52	12000	1.2V	15A
PEX_VDD00T_53	12000	1.2V	15A
PEX_VDD00T_54	12000	1.2V	15A
PEX_VDD00T_55	12000	1.2V	15A
PEX_VDD00T_56	12000	1.2V	15A
PEX_VDD00T_57	12000	1.2V	15A
PEX_VDD00T_58	12000	1.2V	15A
PEX_VDD00T_59	12000	1.2V	15A
PEX_VDD00T_60	12000	1.2V	15A
PEX_VDD00T_61	12000	1.2V	15A
PEX_VDD00T_62	12000	1.2V	15A
PEX_VDD00T_63	12000	1.2V	15A
PEX_VDD00T_64	12000	1.2V	15A
PEX_VDD00T_65	12000	1.2V	15A
PEX_VDD00T_66	12000	1.2V	15A
PEX_VDD00T_67	12000	1.2V	15A
PEX_VDD00T_68	12000	1.2V	15A
PEX_VDD00T_69	12000	1.2V	15A
PEX_VDD00T_70	12000	1.2V	15A
PEX_VDD00T_71	12000	1.2V	15A
PEX_VDD00T_72	12000	1.2V	15A
PEX_VDD00T_73	12000	1.2V	15A
PEX_VDD00T_74	12000	1.2V	15A
PEX_VDD00T_75	12000	1.2V	15A
PEX_VDD00T_76	12000	1.2V	15A
PEX_VDD00T_77	12000	1.2V	15A
PEX_VDD00T_78	12000	1.2V	15A
PEX_VDD00T_79	12000	1.2V	15A
PEX_VDD00T_80	12000	1.2V	15A
PEX_VDD00T_81	12000	1.2V	15A
PEX_VDD00T_82	12000	1.2V	15A
PEX_VDD00T_83	12000	1.2V	15A
PEX_VDD00T_84	12000	1.2V	15A
PEX_VDD00T_85	12000	1.2V	15A
PEX_VDD00T_86	12000	1.2V	15A
PEX_VDD00T_87	12000	1.2V	15A
PEX_VDD00T_88	12000	1.2V	15A
PEX_VDD00T_89	12000	1.2V	15A
PEX_VDD00T_90	12000	1.2V	15A
PEX_VDD00T_91	12000	1.2V	15A
PEX_VDD00T_92	12000	1.2V	15A
PEX_VDD00T_93	12000	1.2V	15A
PEX_VDD00T_94	12000	1.2V	15A
PEX_VDD00T_95	12000	1.2V	15A
PEX_VDD00T_96	12000	1.2V	15A
PEX_VDD00T_97	12000	1.2V	15A
PEX_VDD00T_98	12000	1.2V	15A
PEX_VDD00T_99	12000	1.2V	15A
PEX_VDD00T_100	12000	1.2V	15A

FBVDDQ: 1.2mil internal plane  
500 mil wide from VRM to MEM  
3inch from VRM to farthest MEM

FBVDDQ: 1.8-2.0V @ 9A

FBVDD/Q decap near VRM:  
1x 47uF 1206  
1x 1500uF ALE/OSCON



	GPIO7
FBVDDQ = 1.792V / 1.49V	0
FBVDDQ = 2.098V / 1.81V	1

$FBVDDQ = VREF * (1 + (Rtop / Rbot1))$   
 $1.792V = 0.8V * (1 + (1.24K / 1K))$   
 $1.49V = 0.8V * (1 + (1.07K / 1.24K))$

$FBVDDQ = VREF * (1 + (Rtop / Rbot2))$   
 $2.098V = 0.8V * (1 + (1.24K / 1K(3.24K)))$   
 $1.81V = 0.8V * (1 + (1.07K / (1.24K(2.67K))))$

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_3107 ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: FBVDDQ SINGLE PHASE SWITCHER

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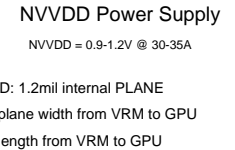
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Net Name	LINE_WIDTH	Current	Voltage
W0000	3000L	10A	1.2V
POSITIVE	3000L	1.5A	1.2000V
W0000 SENSE	3000L	0.5A	1.2V
W0000 SENSE M	3000L	0.5A	1.2V



	GPI06	GPI05
NVDD = 1.00V R7403 1.54K R7329 6.19K	0	0
NVDD = 1.05V R7403 1.54K R7329 6.19K R661 24.3K	0	1
NVDD = 1.10V R7403 1.54K R7329 6.19K R676 12.1K	1	0
NVDD = 1.15V (Undefine) R7403 1.54K R7329 6.19K R661 24.3K R676 12.1K	1	1

	GPIO5
NV/VD = 0.95V R7403 1.00K R7329 5.36K NV/VD = 1.00V R7403 1.00K R7329 5.36K R661 16.2K	1 0



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FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3

1

2

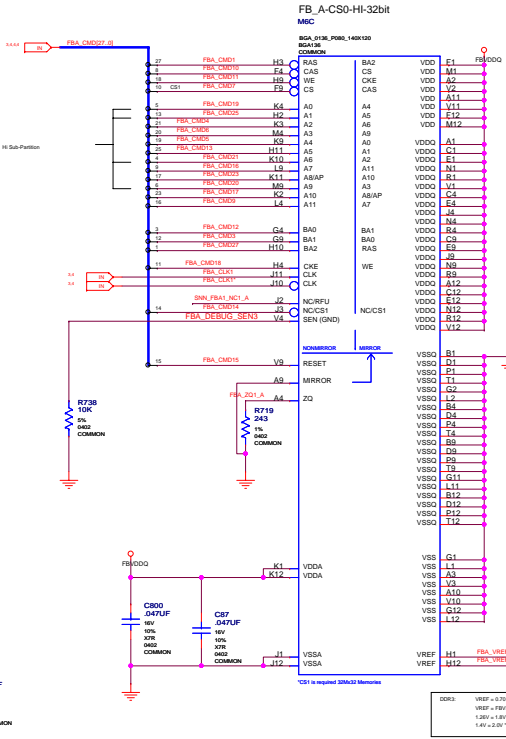
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4

5

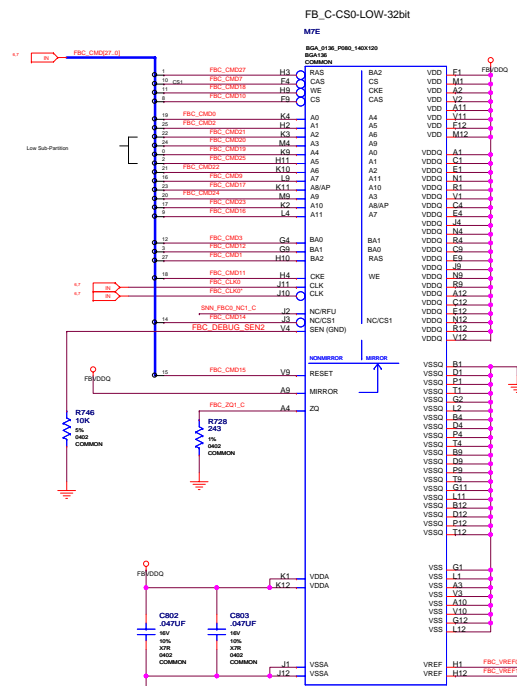
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FBA Partition	
136BGA CMD Mapping	
CMD	ADDR
CMD01	BA0*
CMD02	CAS*
CMD03	WE*
CMD04	CS*
CMD05	BA1*
CMD06	BA2*
CMD07	BA3*
CMD08	BA4*
CMD09	BA5*
CMD10	BA6*
CMD11	BA7*
CMD12	BA8*
CMD13	BA9*
CMD14	BA10*
CMD15	BA11*
CMD16	BA12*
CMD17	BA13*
CMD18	BA14*
CMD19	BA15*
CMD20	BA16*
CMD21	BA17*
CMD22	BA18*
CMD23	BA19*
CMD24	BA20*
CMD25	BA21*
CMD26	BA22*
CMD27	BA23*

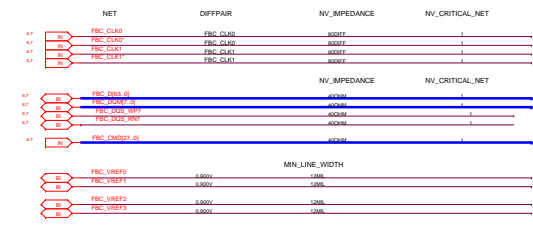
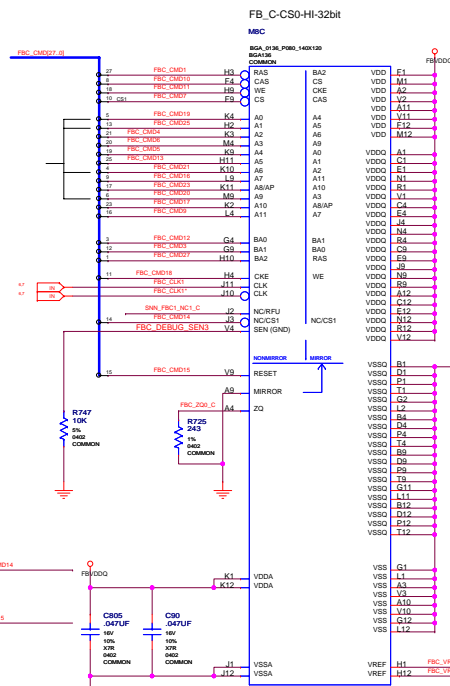


NET		DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
12	FBA_CMD0	FBA_CMD0	800PT	1
13	FBA_CMD0P	FBA_CMD0	800PT	1
14	FBA_CMD1	FBA_CMD1	800PT	1
15	FBA_CMD1P	FBA_CMD1	800PT	1
NV_IMPEDANCE NV_CRITICAL_NET				
12	FBA_CMD01_0	800PT	1	
13	FBA_CMD01P_0	800PT	1	
14	FBA_CMD02_0	800PT	1	
15	FBA_CMD02P_0	800PT	1	
16	FBA_CMD03	800PT	1	
MIN_LINE_WIDTH				
16	FBA_VREF0	2.000V	100M	
17	FBA_VREF1	2.000V	100M	
18	FBA_VREF2	2.000V	100M	
19	FBA_VREF3	2.000V	100M	

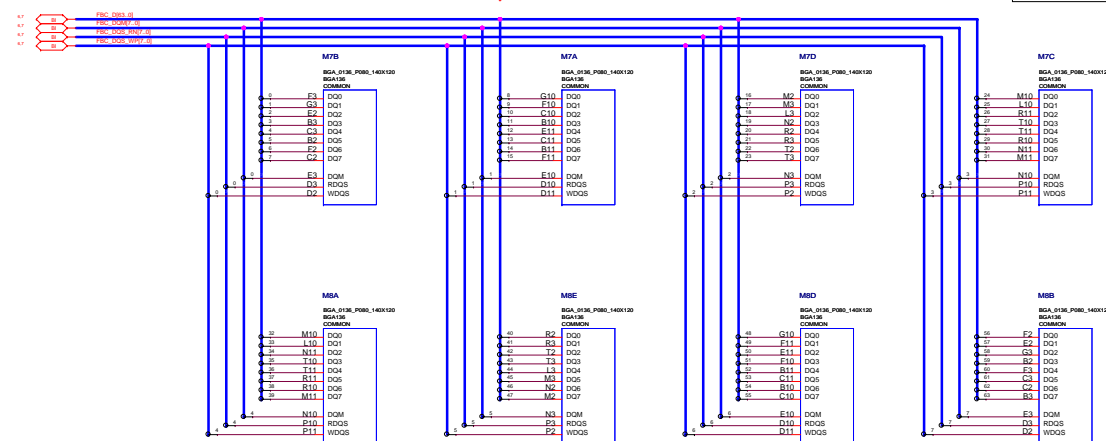
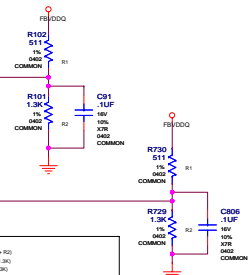
## FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3



FBC Partition			CSD
CMD	ADDR		
CMD01	R40*		
CMD02	C40*		
CMD11	WE*		
CMD18	CKE		
CMD19	RESET/ODT		
CMD6	CS0*		
CMD19	A0-0		
CMD05	A0-1		
CMD04	A0-2	} Low Sub-Partition	
CMD04	A0-3		
CMD03	A0-4		
CMD3	A0-5		
CMD4	A0-6	} H0 Sub-Partition	
CMD6	A0-6		
CMD6	A0-6		
CMD5	A0-6		
CMD13	A0-6		
CMD21	A0-6		
CMD16	A0-7		
CMD23	A0-8		
CMD20	A0-9		
CMD17	A0-10		
CMD9	A0-11		
CMD14	A0-12		
CMD12	BA0		
CMD3	BA1		
CMD27	BA2		



Termination for Sub-Partition and CLK  
MUST BE PLACED as close as possible to  
the BGA memory on the line BEFORE the  
MEMORY pin!!  
Minimize the stub length!!



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS P/U'S, FBC CLK TERMS

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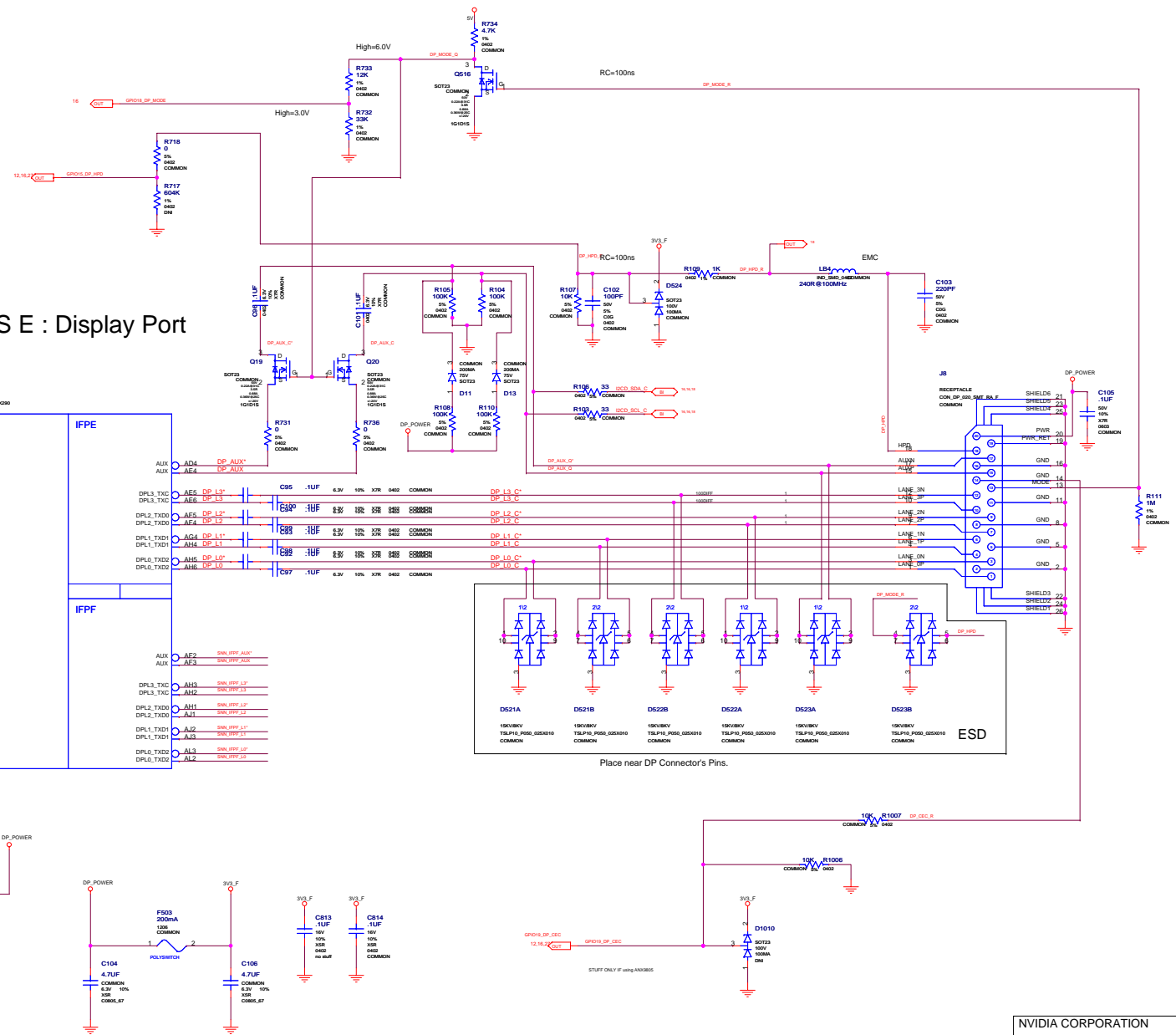


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TMDS LINK: E & F

TMDS E : Display Port



$$V_o = V_{REF} * (1 + (R_{top} / R_{bot})) + I_{adj} * R_{bot}$$

$$3.28V = 1.25V * (1 + (1.58k / 1.00k)) + 55\mu * 1.00k$$

$$3.33V = 1.25V * (1 + (1.62k / 1.00k)) + 55\mu * 1.00k$$

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK C/D, AC COUPLING, PD's, DVI CONNECTOR MID

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