E4905-A00

N18P GDDR5 X32 128BITS
PCIE AND MODULAR DISPLAY

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MICRO-STAR INT'L CO.,LTD

MS-V378

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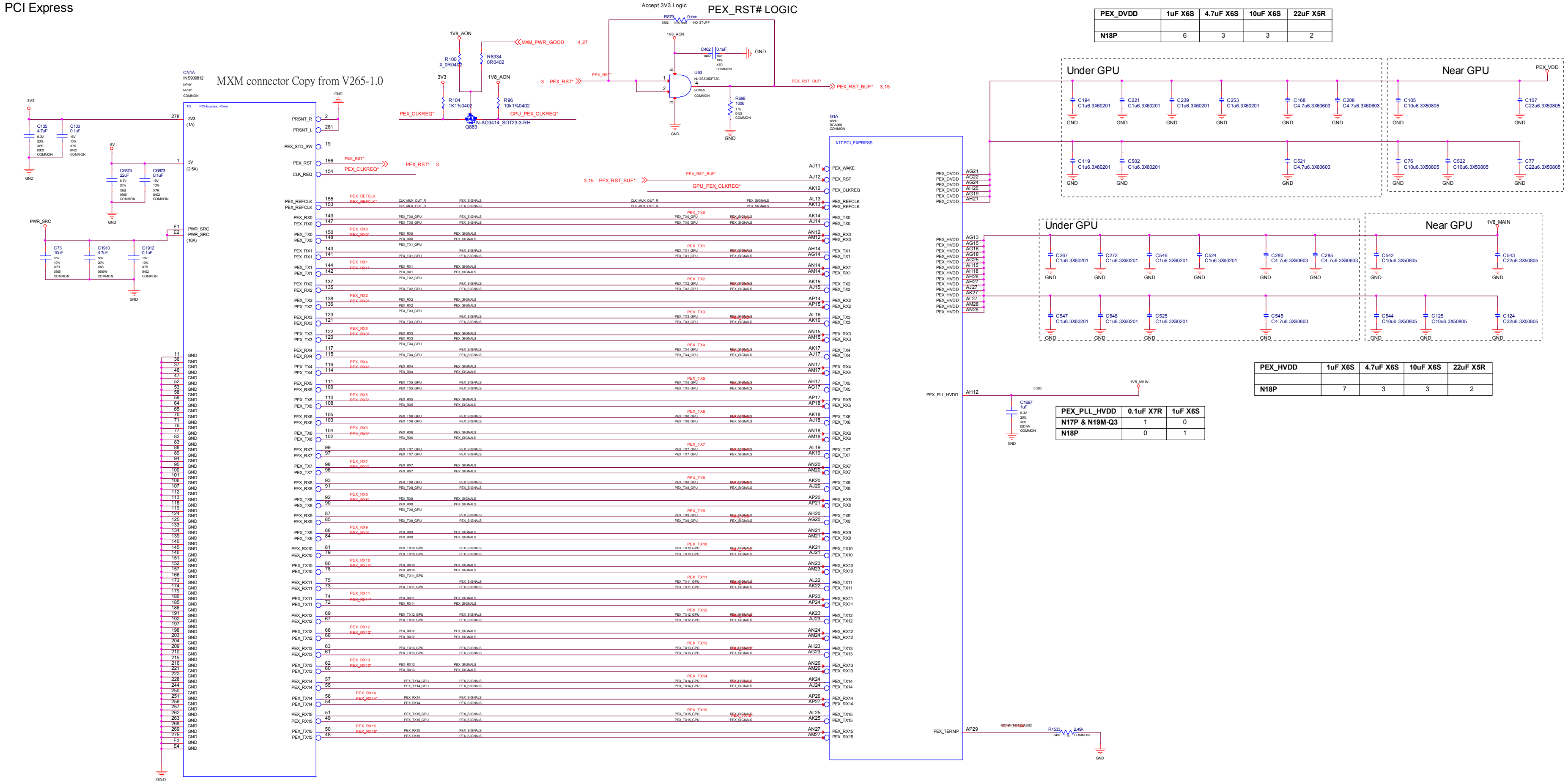
PCI Express



PEX_DVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
N18P	6	3	3	2

PEX_HVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
N18P	7	3	3	2

PEX_PLL_HVDD	0.1uF X7R	1uF X6S
N17P & N19M-Q3	1	0
N18P	0	1

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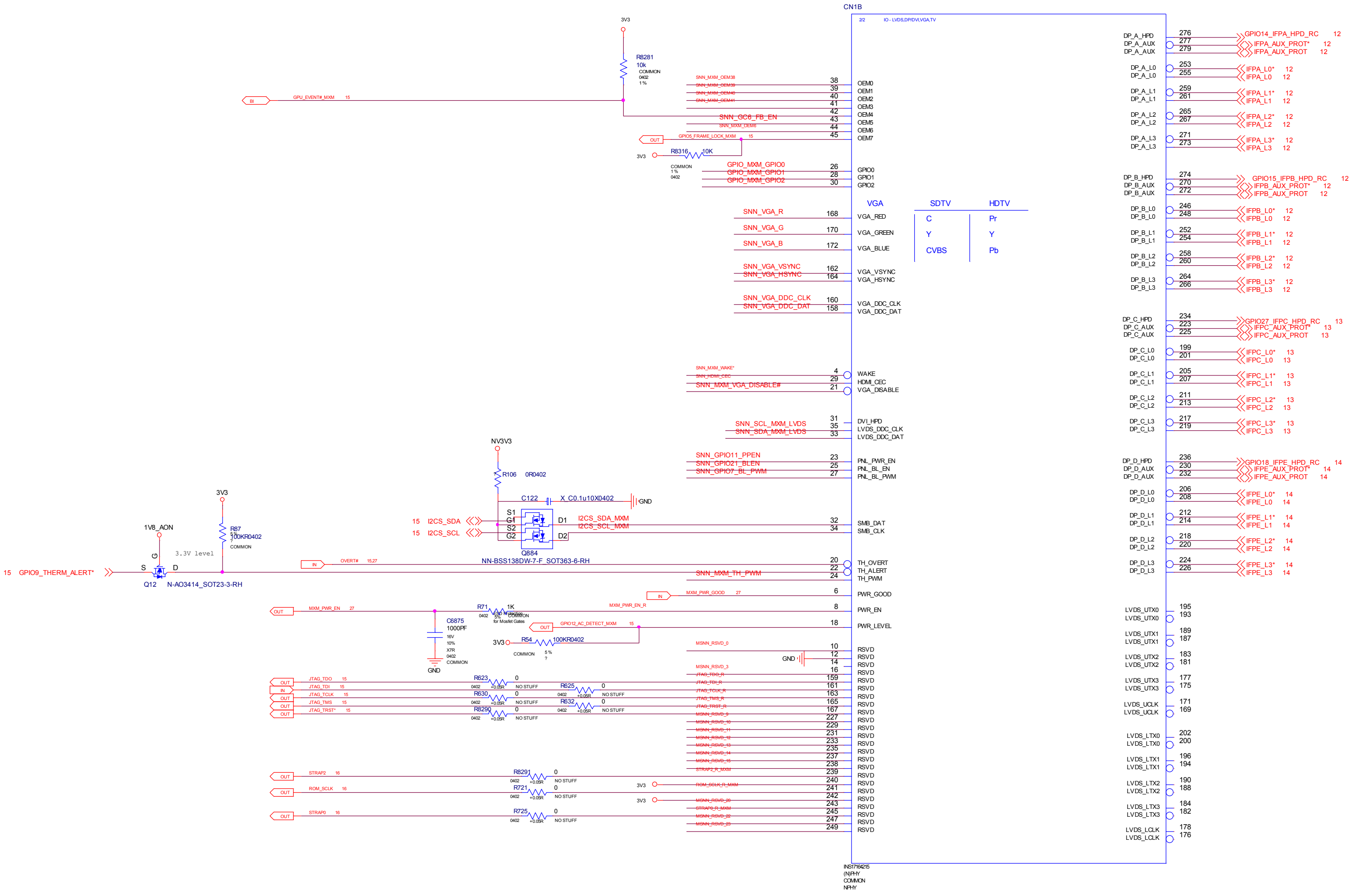
PCI EXPRESS REFCLK SOURCE & TRACES

MXM connector Copy from V265-1.0



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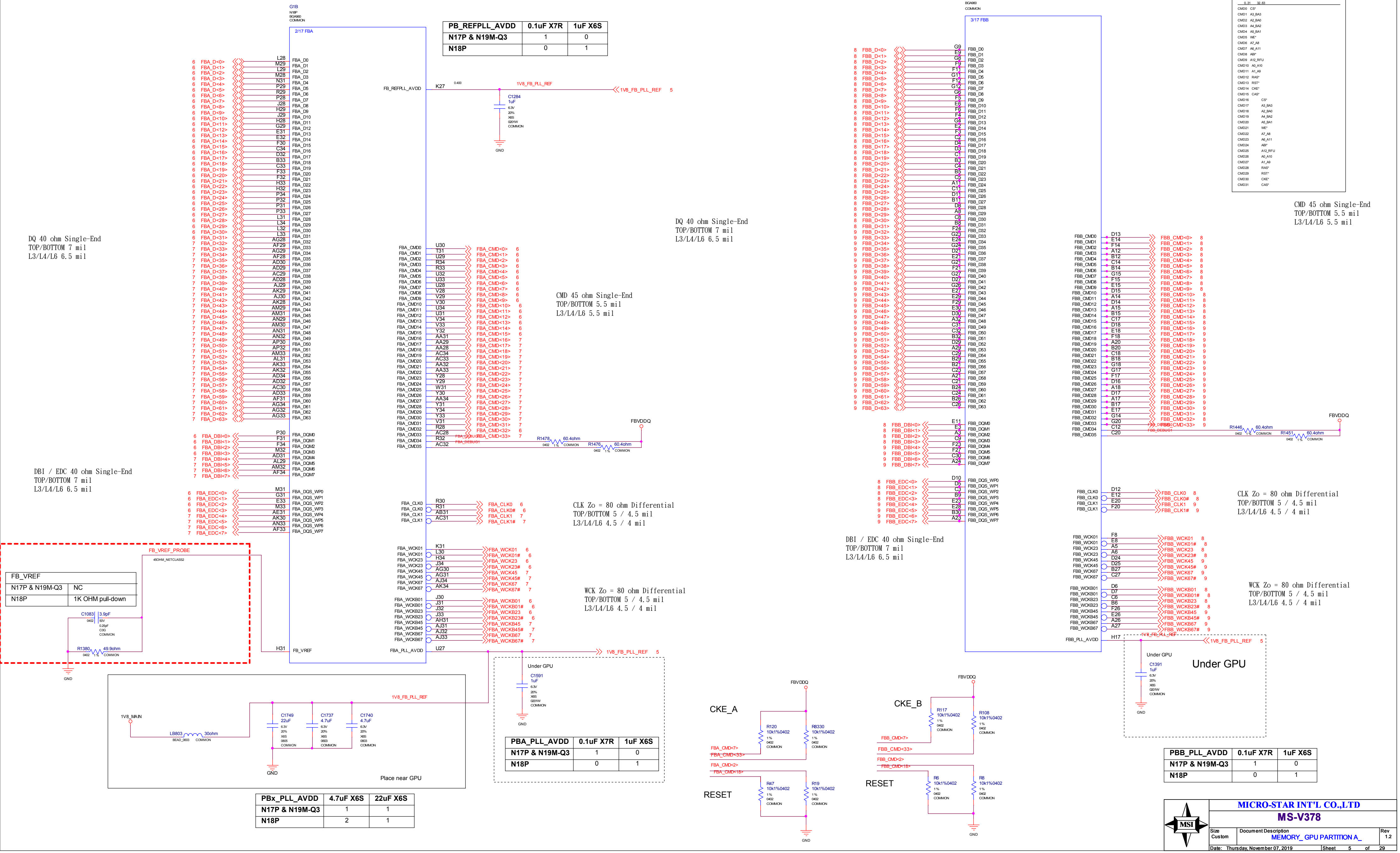
MEMORY: GPU PARTITION A/B



PB_REFPLL_AVDD	0.1uF X7R	1uF X6S
N17P & N19M-Q3	1	0
N18P	0	1

GDDR5_BGA170_MIRR COMMAND MAP

	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*

CMD 45 ohm Single-End
TOP/BOTTOM 5.5 mil
L3/L4/L6 5.5 mil

DQ 40 ohm Single-End
TOP/BOTTOM 7 mil
L3/L4/L6 6.5 mil

DQ 40 ohm Single-End
TOP/BOTTOM 7 mil
L3/L4/L6 6.5 mil

CMD 45 ohm Single-End
TOP/BOTTOM 5.5 mil
L3/L4/L6 5.5 mil

DBI / EDC 40 ohm Single-End
TOP/BOTTOM 7 mil
L3/L4/L6 6.5 mil

CLK Zo = 80 ohm Differential
TOP/BOTTOM 5 / 4.5 mil
L3/L4/L6 4.5 / 4 mil

DBI / EDC 40 ohm Single-End
TOP/BOTTOM 7 mil
L3/L4/L6 6.5 mil

CLK Zo = 80 ohm Differential
TOP/BOTTOM 5 / 4.5 mil
L3/L4/L6 4.5 / 4 mil

WCK Zo = 80 ohm Differential
TOP/BOTTOM 5 / 4.5 mil
L3/L4/L6 4.5 / 4 mil

WCK Zo = 80 ohm Differential
TOP/BOTTOM 5 / 4.5 mil
L3/L4/L6 4.5 / 4 mil

FB_VREF	
N17P & N19M-Q3	NC
N18P	1K OHM pull-down

PBA_PLL_AVDD	0.1uF X7R	1uF X6S
N17P & N19M-Q3	1	0
N18P	0	1

PBx_PLL_AVDD	4.7uF X6S	22uF X6S
N17P & N19M-Q3	1	1
N18P	2	1

PBB_PLL_AVDD	0.1uF X7R	1uF X6S
N17P & N19M-Q3	1	0
N18P	0	1

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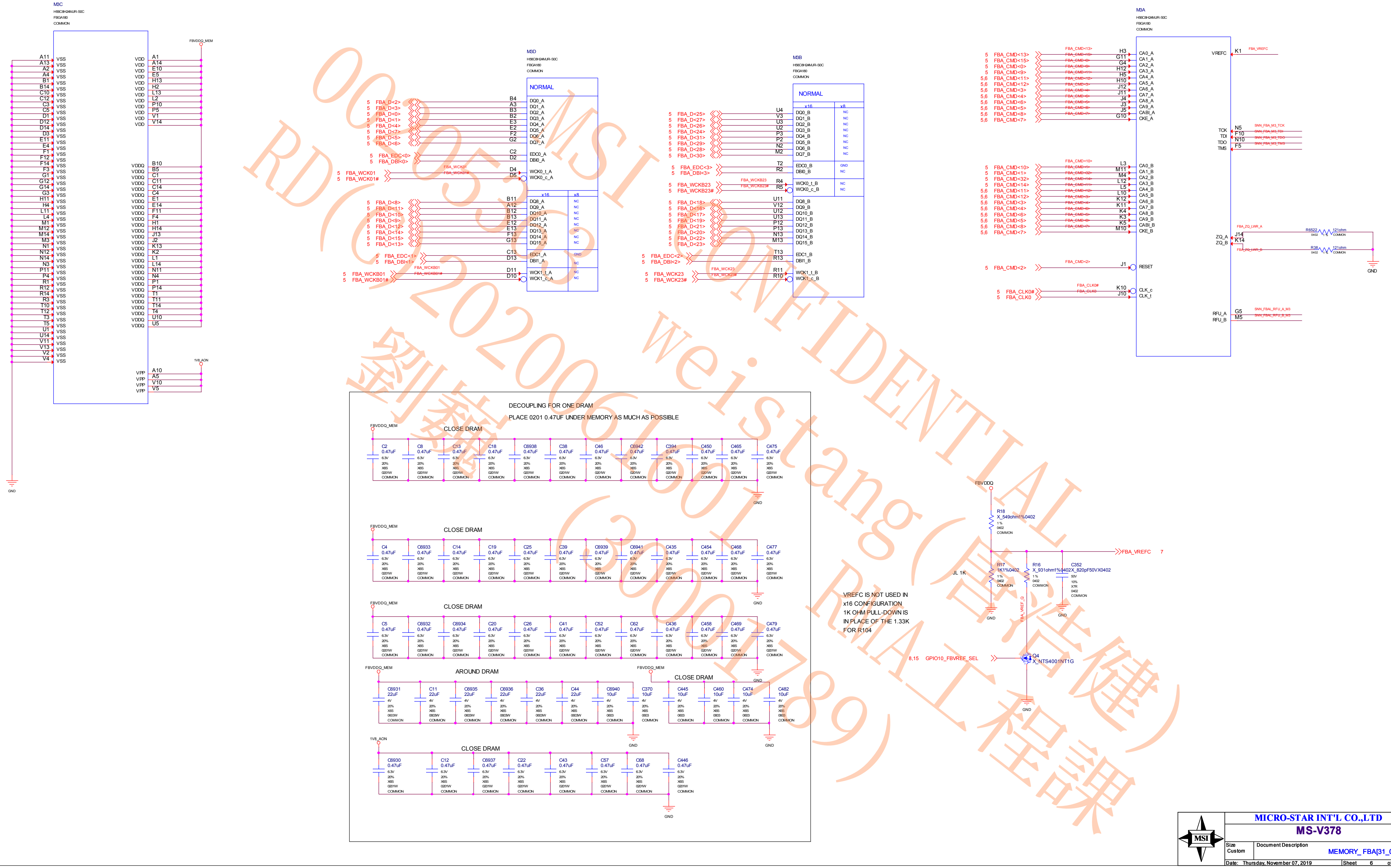
MEMORY: FBA[31:0]



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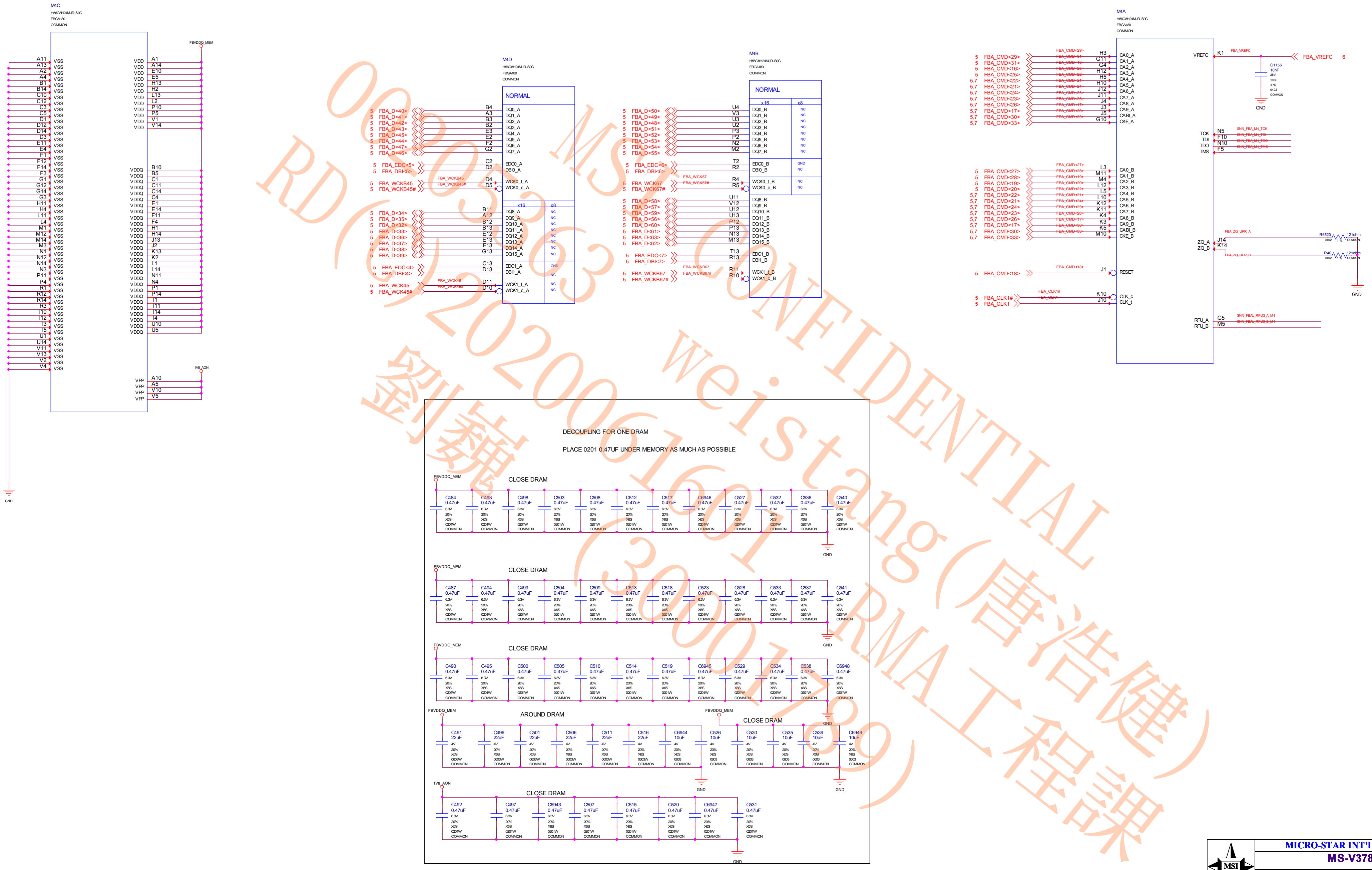
MEMORY: FBA[63:32]



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Custom	MEMORY_ FBA[63_32]	1.2

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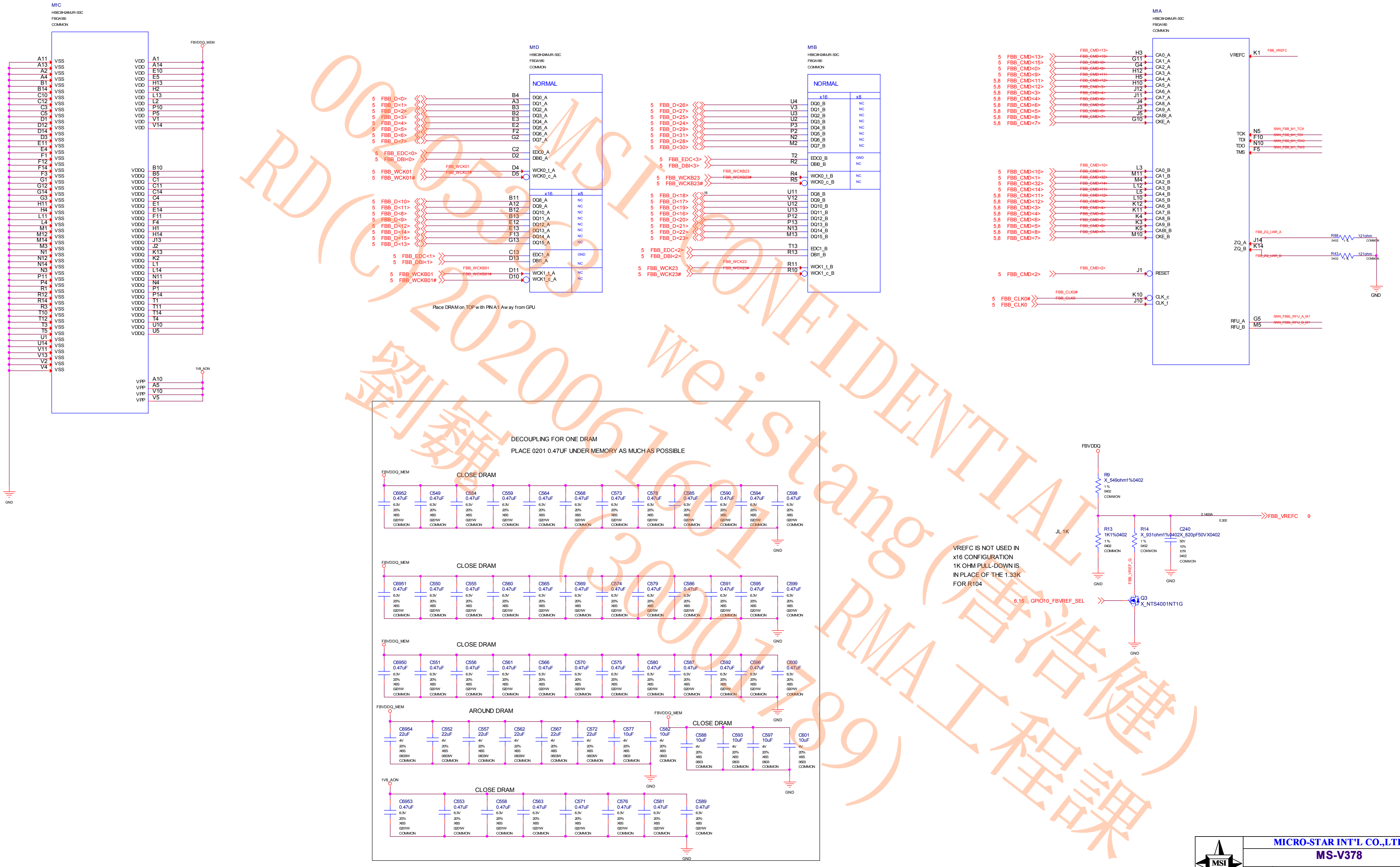
MEMORY: FBB[31:0]



Place DRAM on TOP with PIN A1 Away from GPU

DECOUPLING FOR ONE DRAM

PLACE 0201 0.47UF UNDER MEMORY AS MUCH AS POSSIBLE

VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R104

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Document Description: MEMORY_FBB[31_0]
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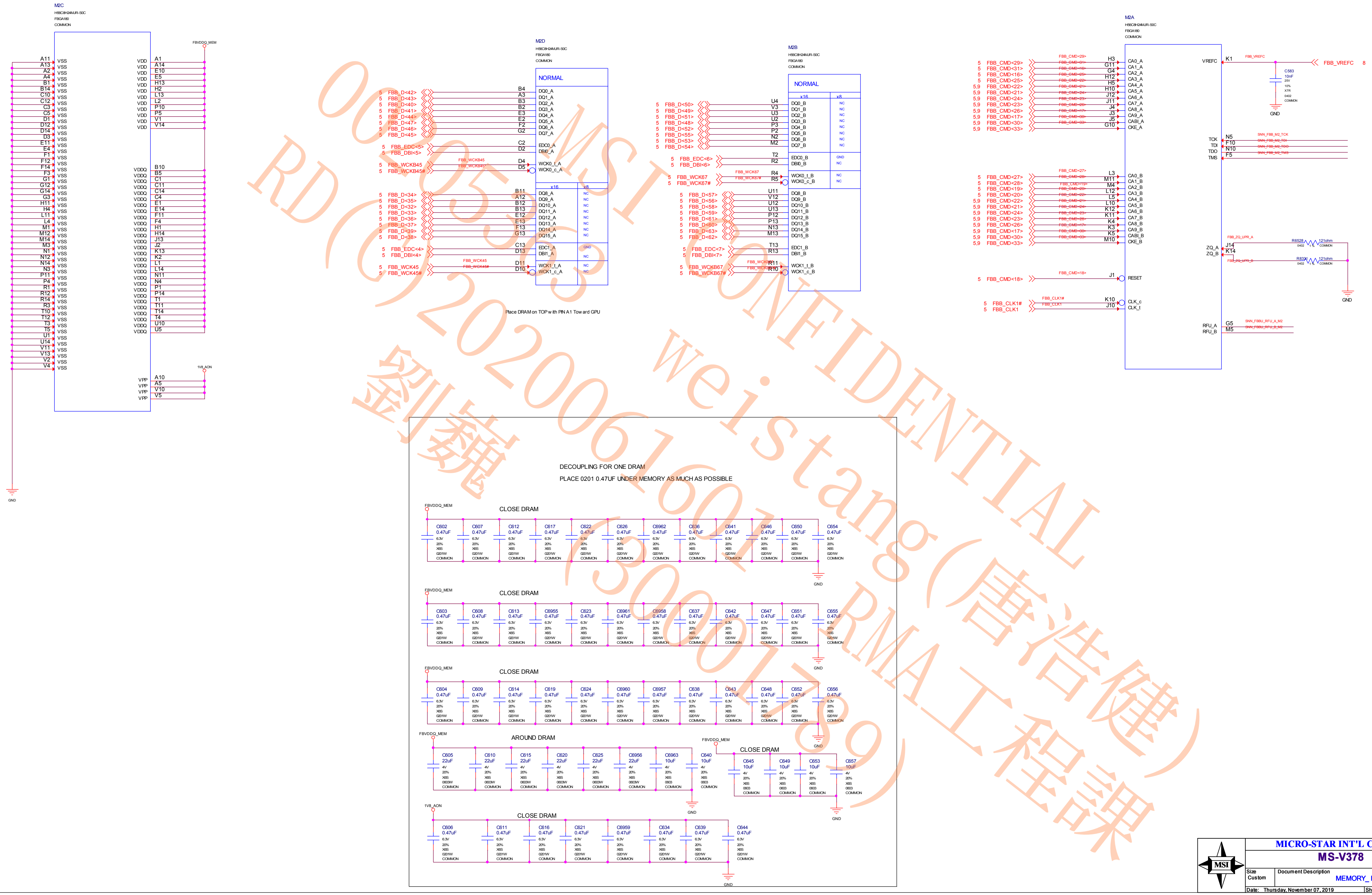
MEMORY: FBB[63:32]



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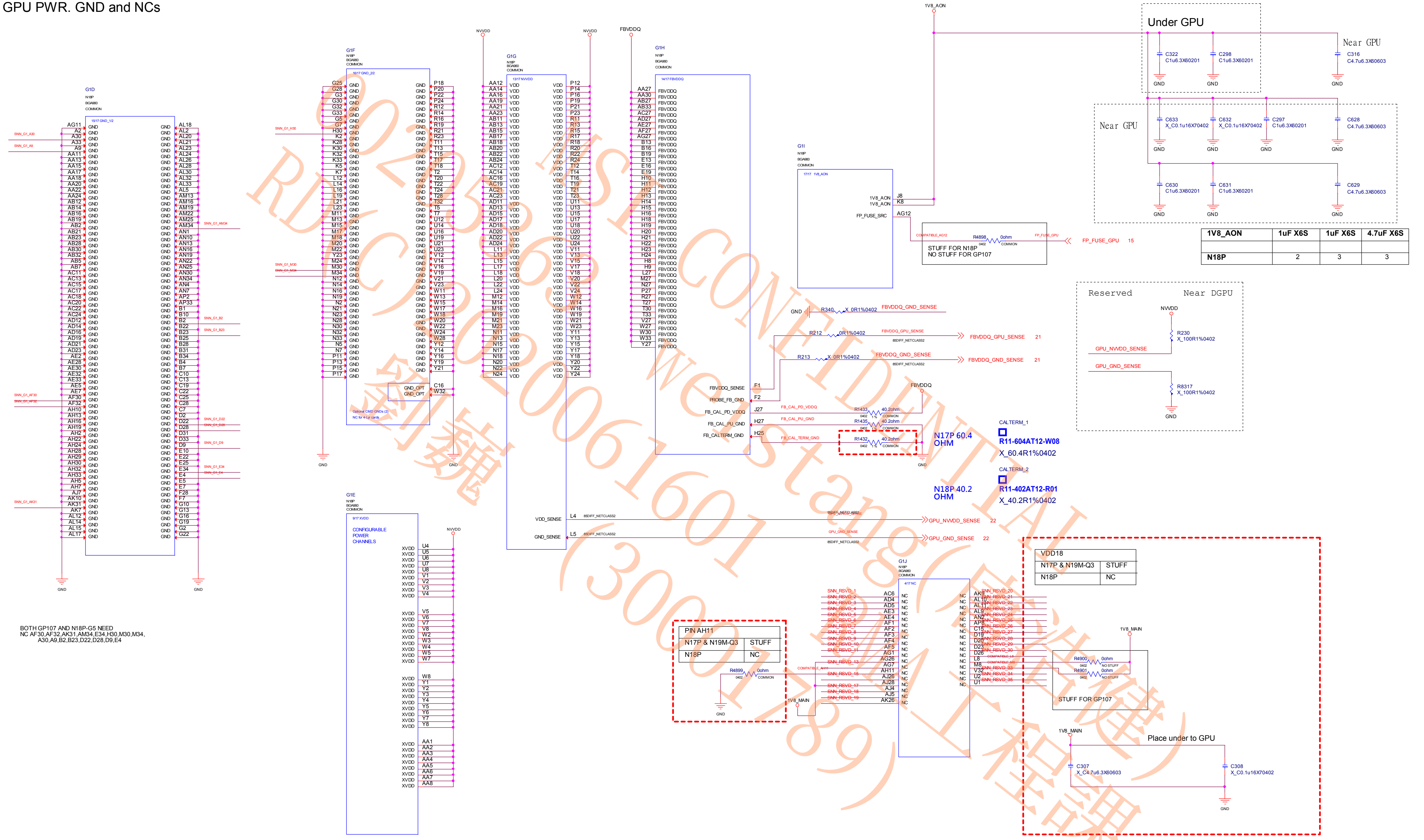
GPU PWR. GND and NCs



1V8_AON	1uF X6S	1uF X6S	4.7uF X6S
N18P	2	3	3

PIN AH11	
N17P & N19M-Q3	STUFF
N18P	NC

VDD18	
N17P & N19M-Q3	STUFF
N18P	NC

BOTH GP107 AND N18P-G5 NEED
NC AF30,AF32,AK31,AM34,E34,H30,M30,M34,
A30,A9,B2,B23,D22,D28,D9,E4

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Custom	GPU PWR. GND and NCs	1.2

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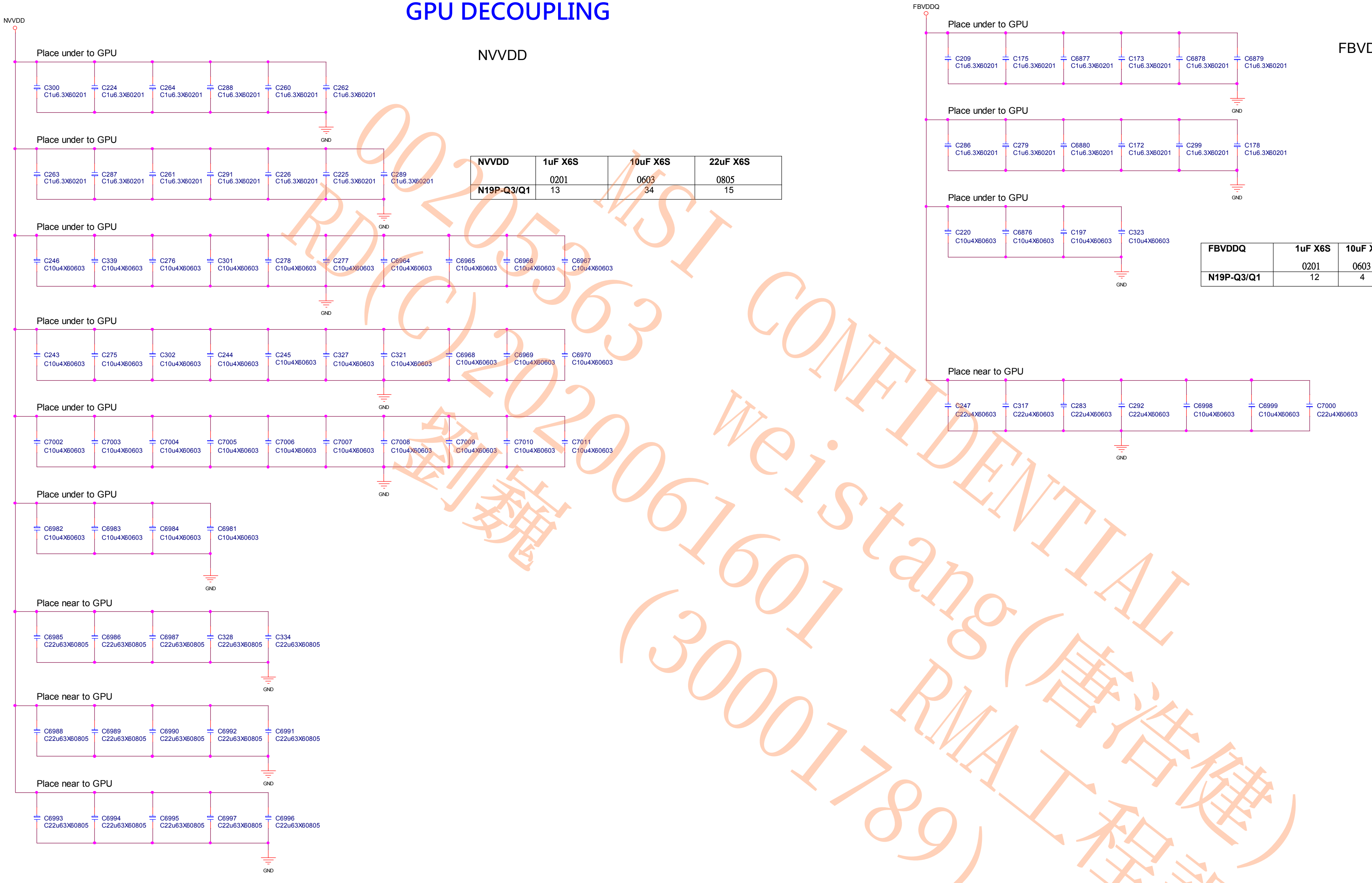
GPU DECOUPLING



NVVDD	1uF X6S 0201	10uF X6S 0603	22uF X6S 0805
N19P-Q3/Q1	13	34	15

FBVDDQ	1uF X6S 0201	10uF X6S 0603	22uF X6S 0603	10uF X6S 0603
N19P-Q3/Q1	12	4	5	2

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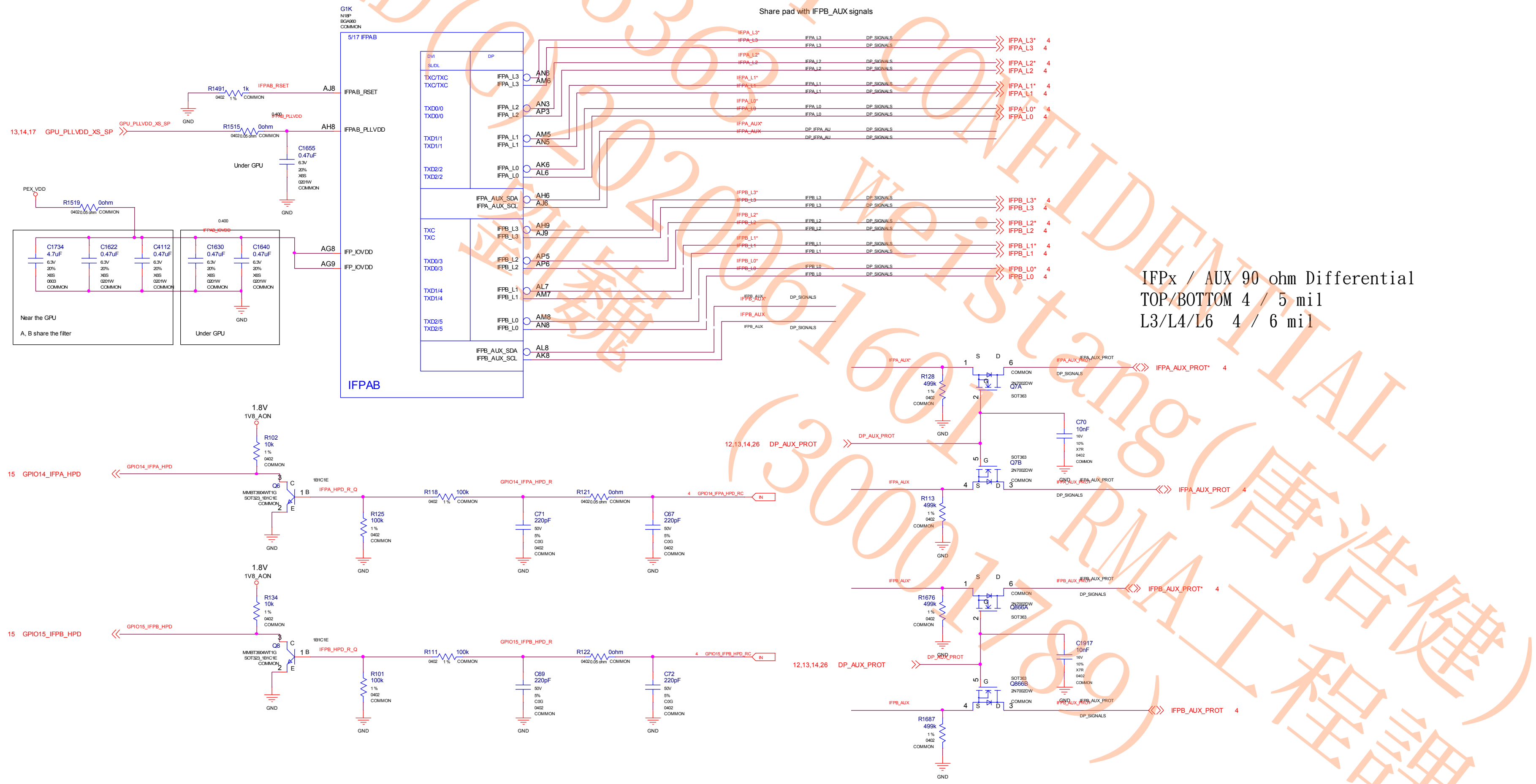
IFPAB DPIIM



IFPx / AUX 90 ohm Differential
TOP/BOTTOM 4 / 5 mil
L3/L4/L6 4 / 6 mil

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Size	Document Description	Rev
Custom	GPU IFPAB DPIIM	1.2

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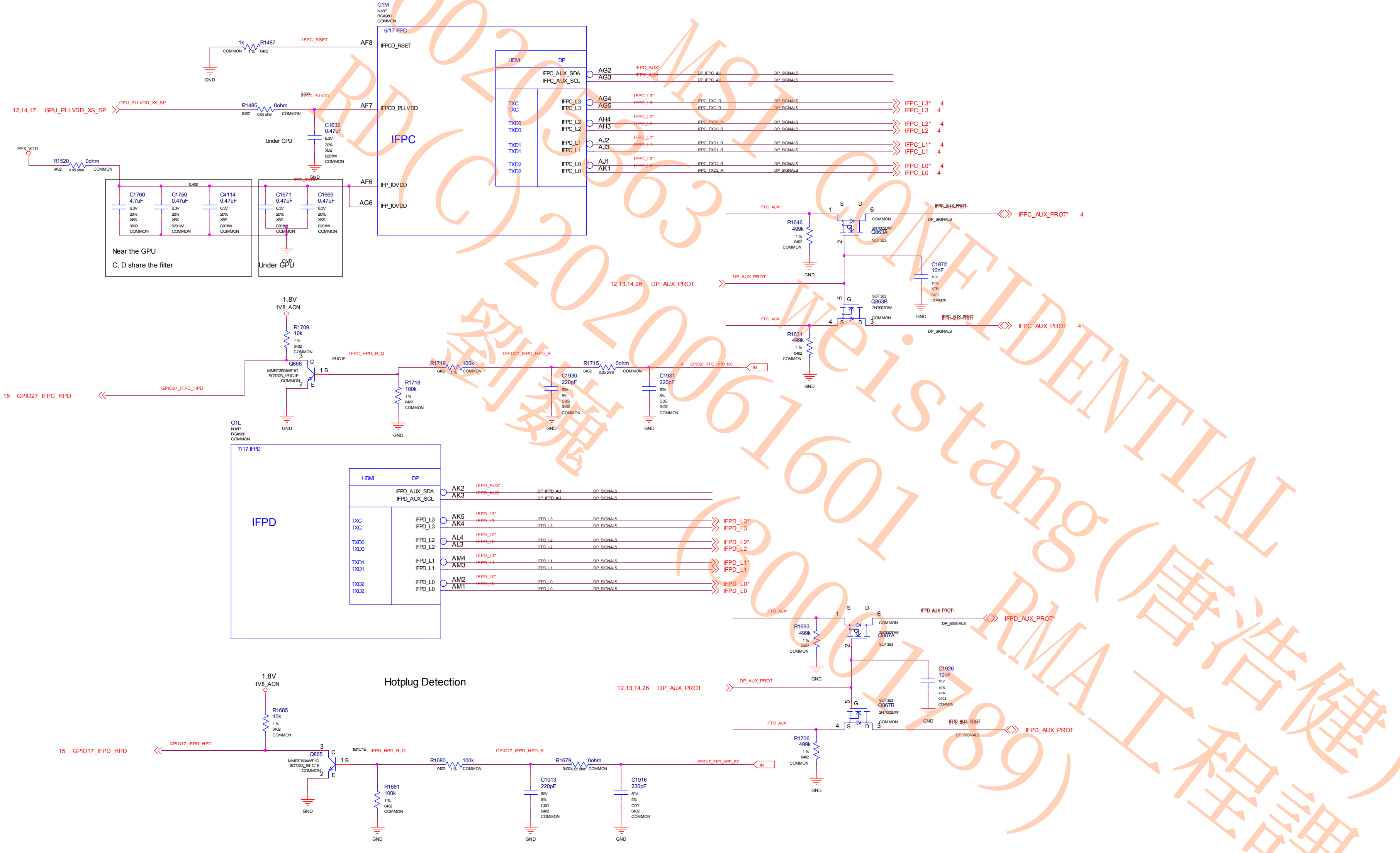
IFPCD DPIIM



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Custom	GPU IFPCD DPIIM	1.2

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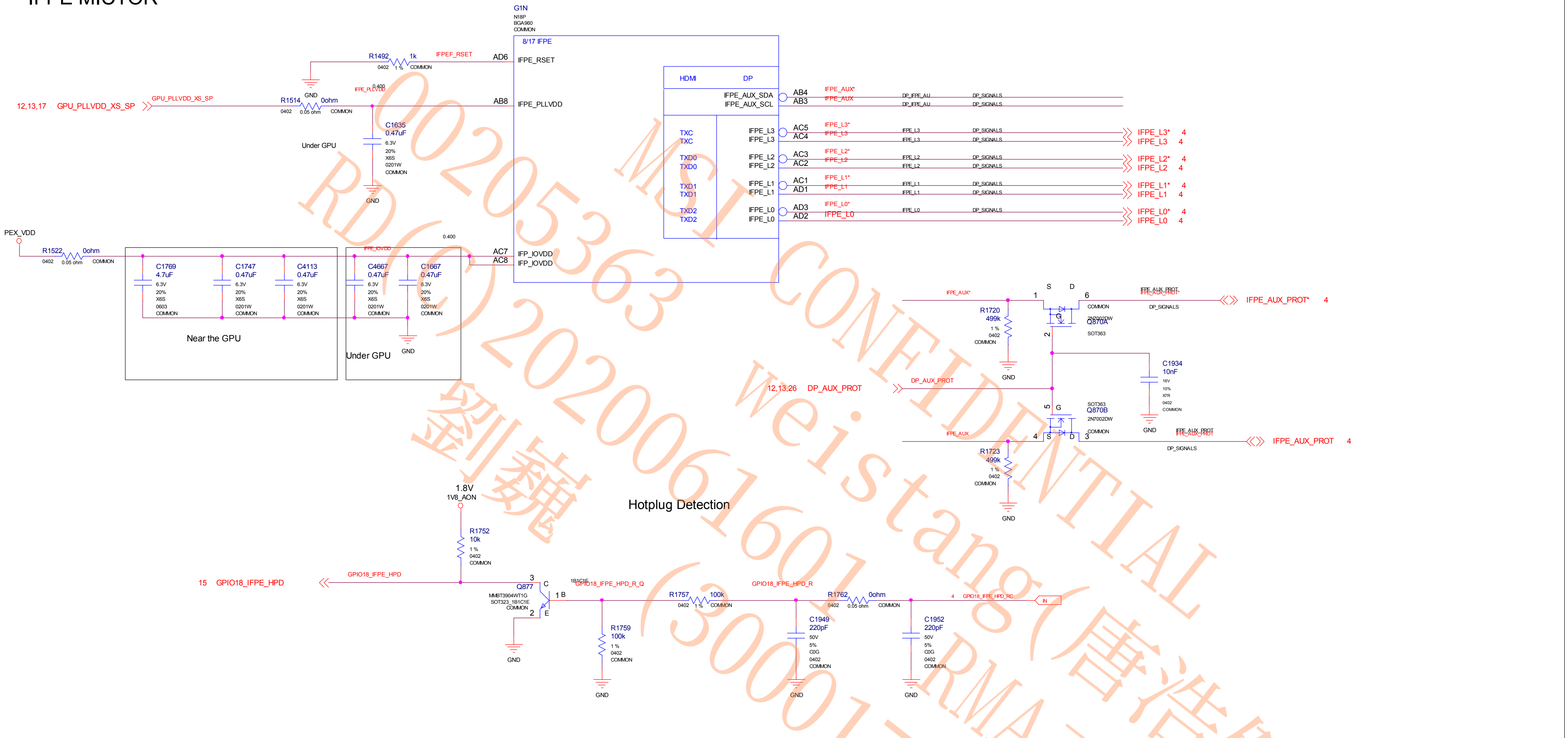
IFPE MICTOR



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Custom	GPU IFPE MICTOR	1.2

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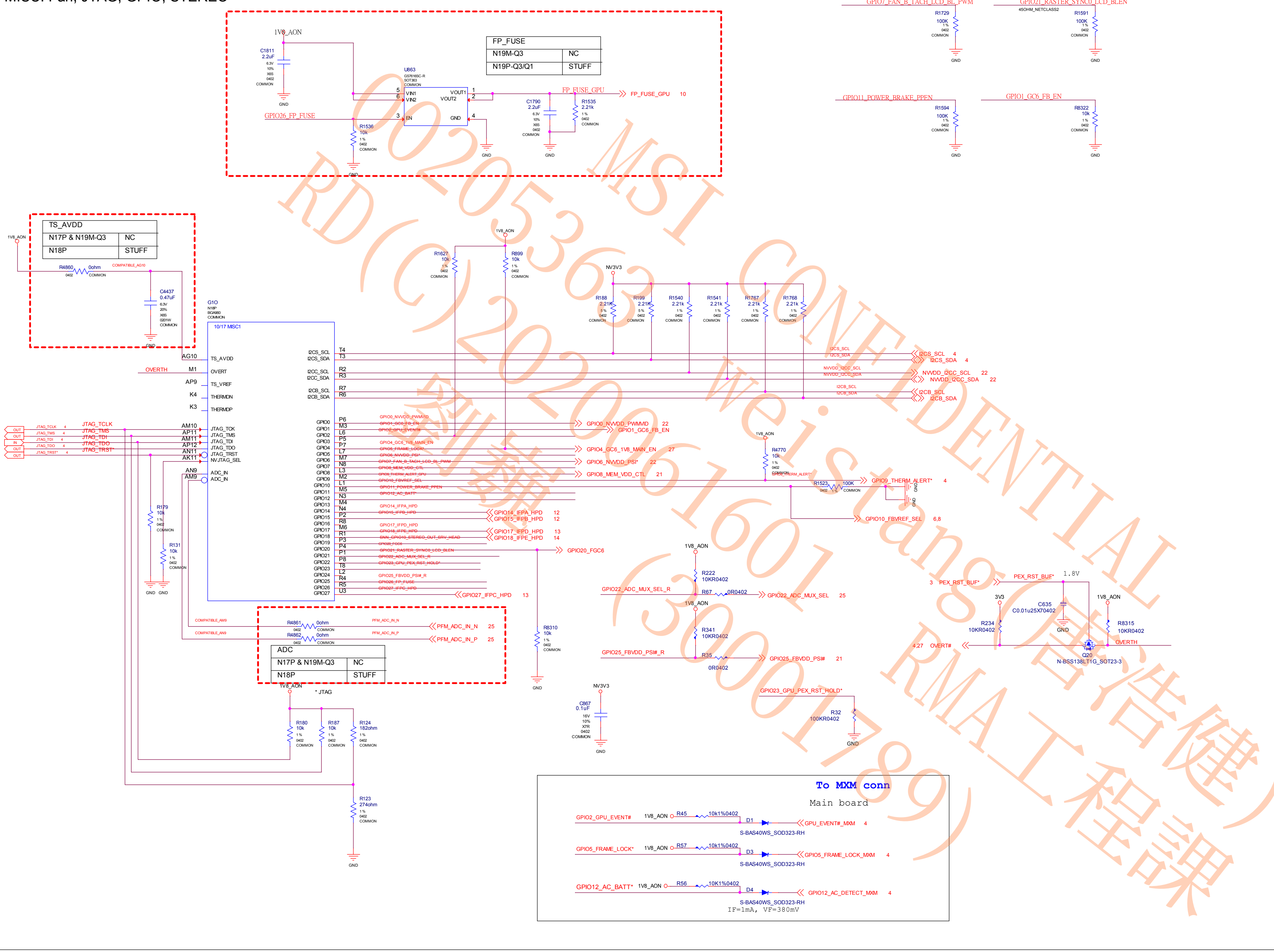
MISC: Fan, JTAG, GPIO, STEREO



FP_FUSE	
N19M-Q3	NC
N19P-Q3/Q1	STUFF

TS_AVDD	
N17P & N19M-Q3	NC
N18P	STUFF

ADC	
N17P & N19M-Q3	NC
N18P	STUFF

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Custom	GPU_ GPIO, FANS, JTAG, S	1.2

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MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

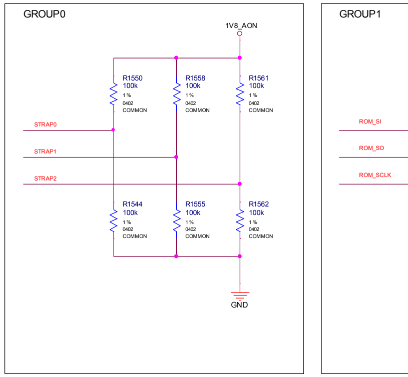
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

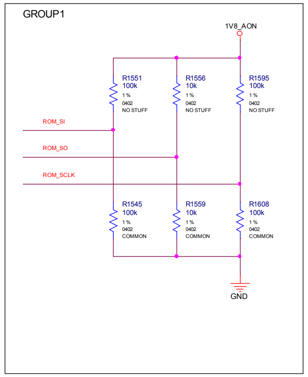
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

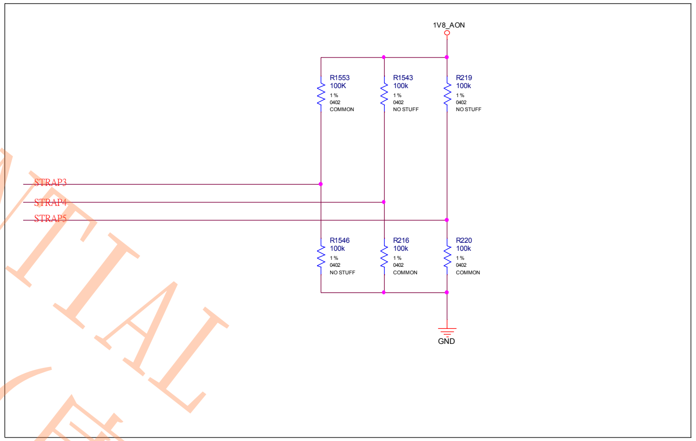
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

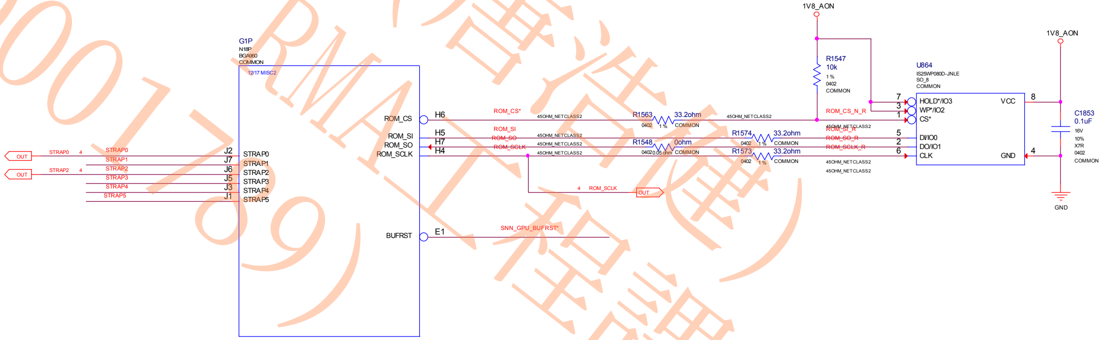
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE









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Custom	GPU_ ROM, STRAPS	1.2

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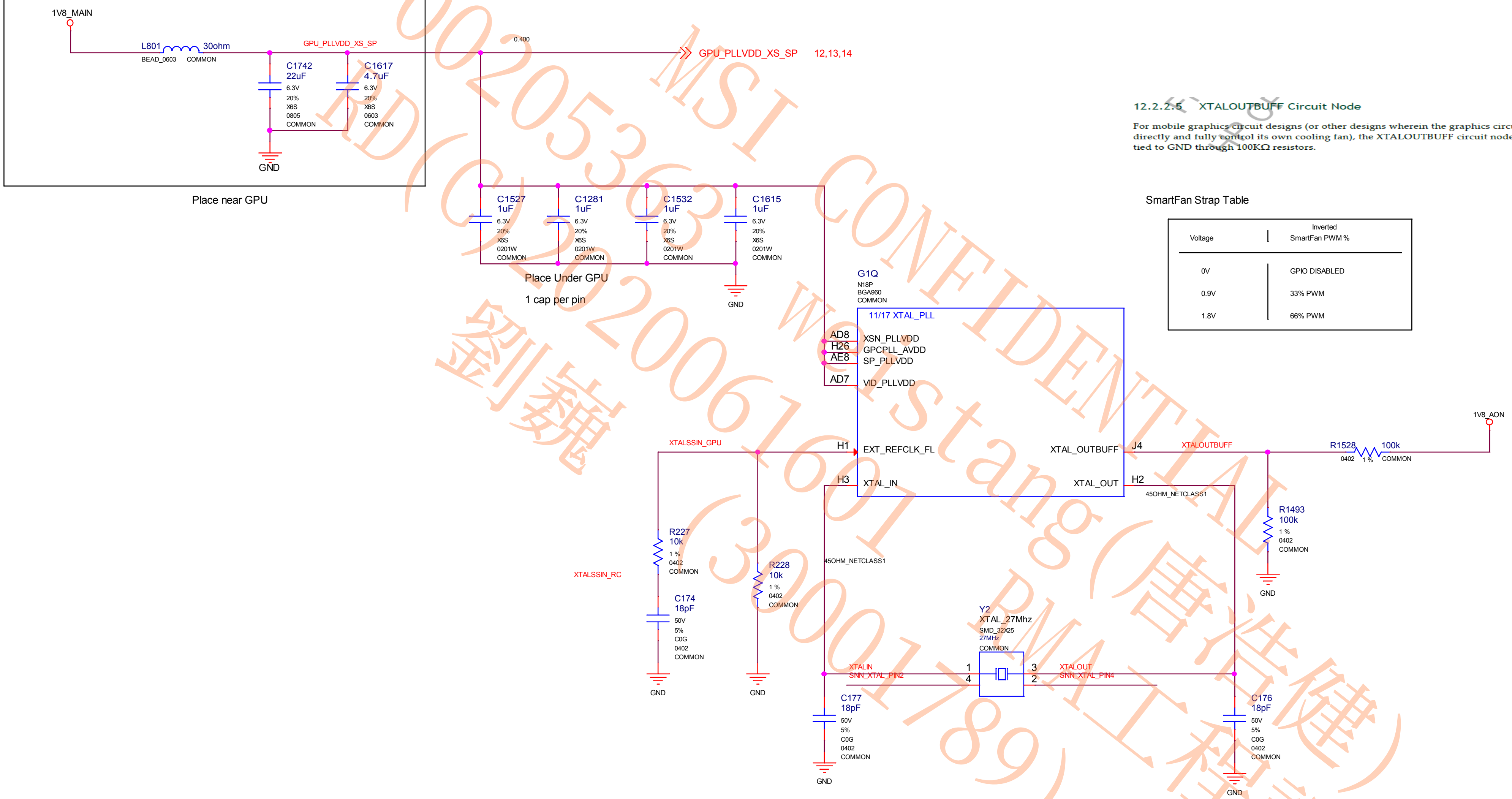
MISC2: XTAL. PLL

XSN_PLLVDD GPCPLL_AVDD SP_PLLVDD VID_PLLVDD	0.1uF X7R	1uF X6S	4.7uF X6S	22uF X6S
N17P & N19M-Q3	4	0	1	1
N18P	0	4	1	1



12.2.2.5 XTALOUTBUFF Circuit Node

For mobile graphics circuit designs (or other designs wherein the graphics circuit does not directly and fully control its own cooling fan), the XTALOUTBUFF circuit node must be tied to GND through 100KΩ resistors.

SmartFan Strap Table

Voltage	Inverted SmartFan PWM %
0V	GPIO DISABLED
0.9V	33% PWM
1.8V	66% PWM

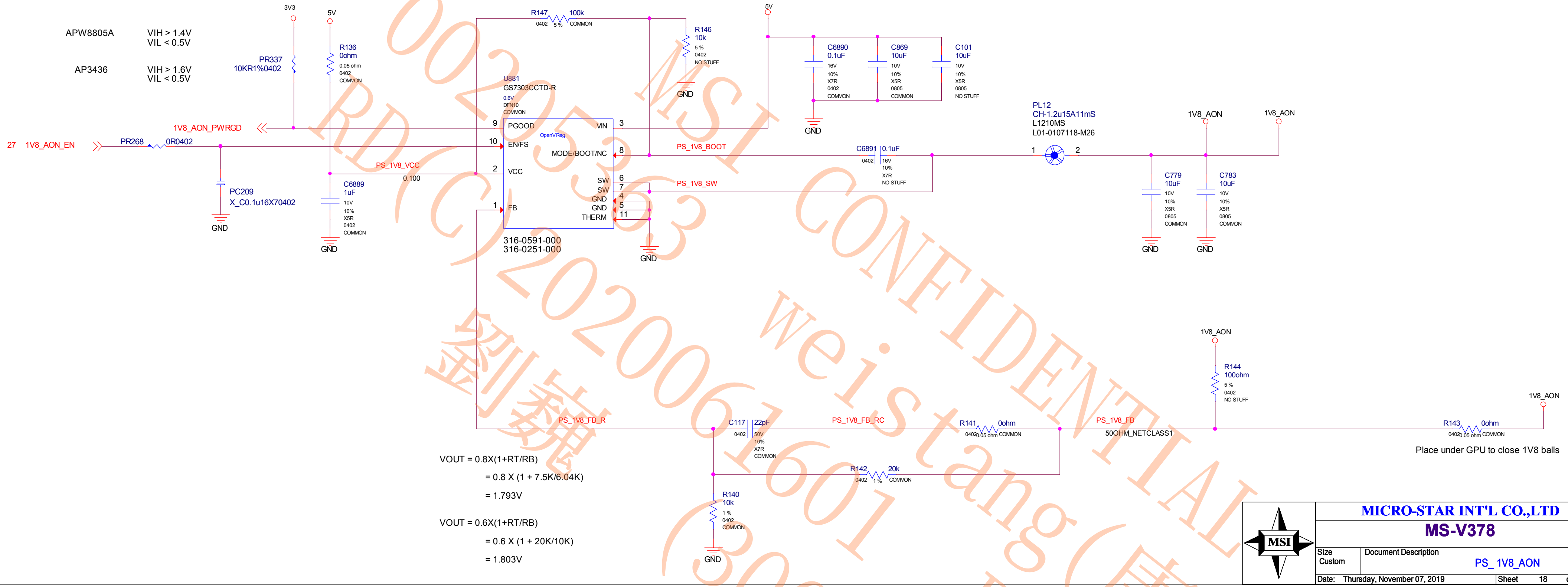
PS: 1V8_AON

Voltage = 1.8V
Current = ? A
OCP(typi) = ? A

1V8_AON

APW8805A VIH > 1.4V
VIL < 0.5V

AP3436 VIH > 1.6V
VIL < 0.5V



Place under GPU to close 1V8 balls

VOUT = 0.8X(1+RT/RB)
= 0.8 X (1 + 7.5K/6.04K)
= 1.793V

VOUT = 0.6X(1+RT/RB)
= 0.6 X (1 + 20K/10K)
= 1.803V

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Custom	PS_ 1V8_AON	1.2

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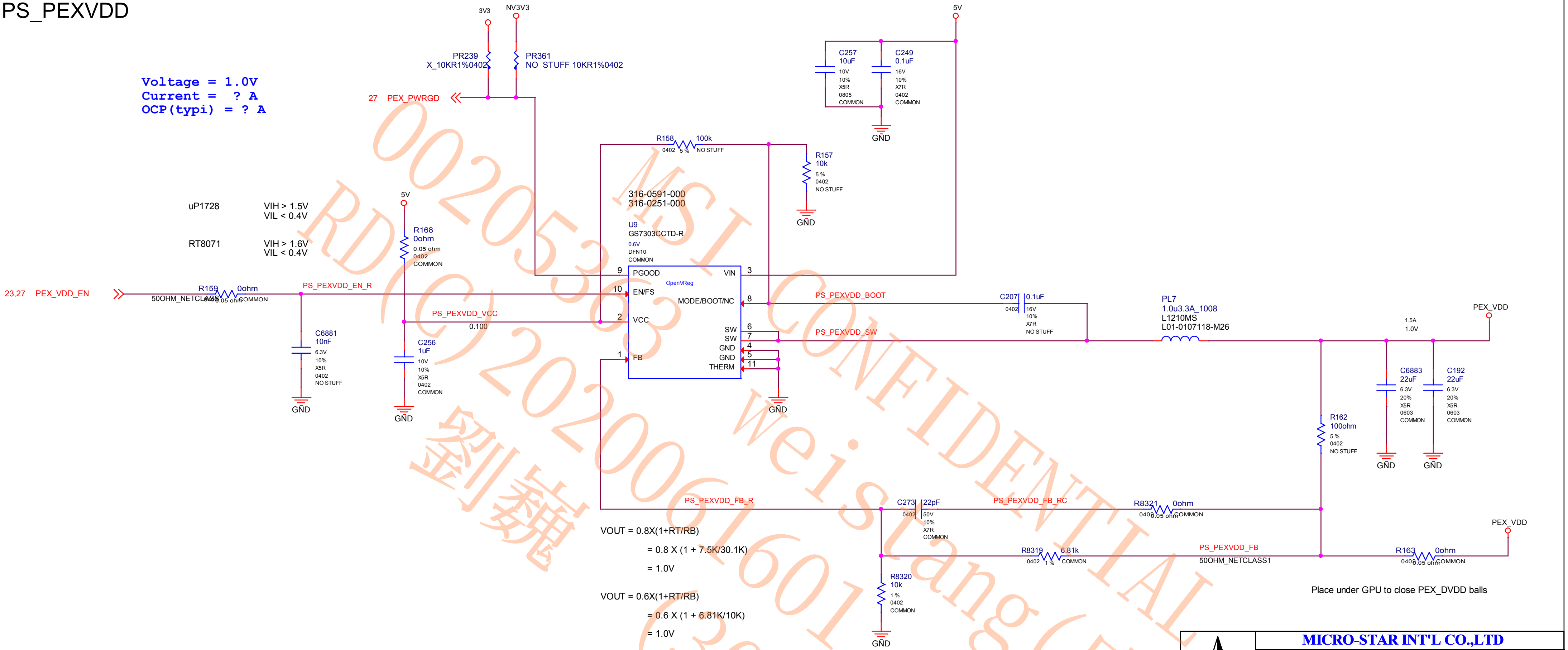
PS_PEXVDD

Voltage = 1.0V
Current = ? A
OCP(typi) = ? A



VOUT = 0.8X(1+RT/RB)

= 0.8 X (1 + 7.5K/30.1K)

= 1.0V

VOUT = 0.6X(1+RT/RB)

= 0.6 X (1 + 6.81K/10K)

= 1.0V

Place under GPU to close PEX_DVDD balls

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Custom	PS_PEXVDD	1.2

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BLANK

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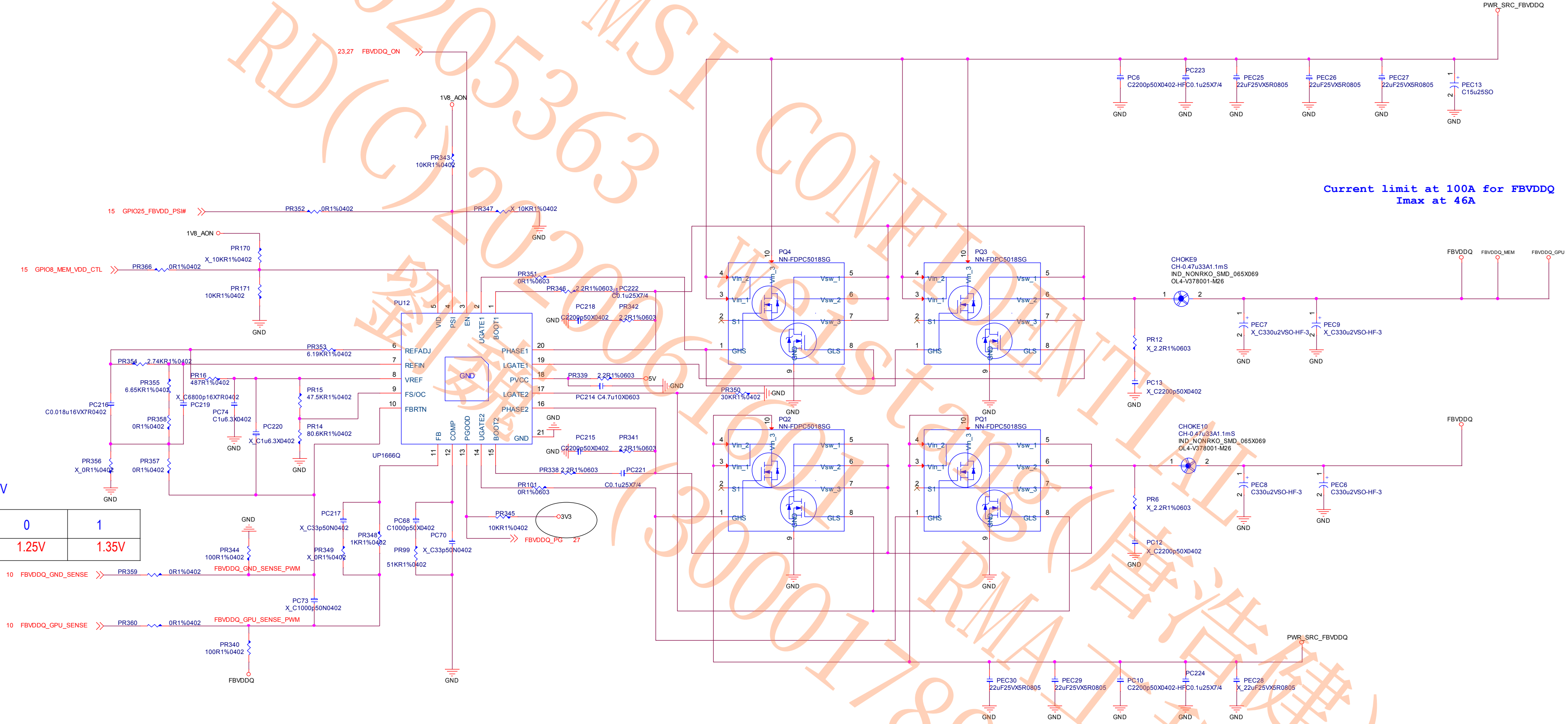
PS: FBVDD CONTROLLER



Current limit at 100A for FBVDDQ
Imax at 46A

Vboot=1.35V

VID	0	1
Vout	1.25V	1.35V

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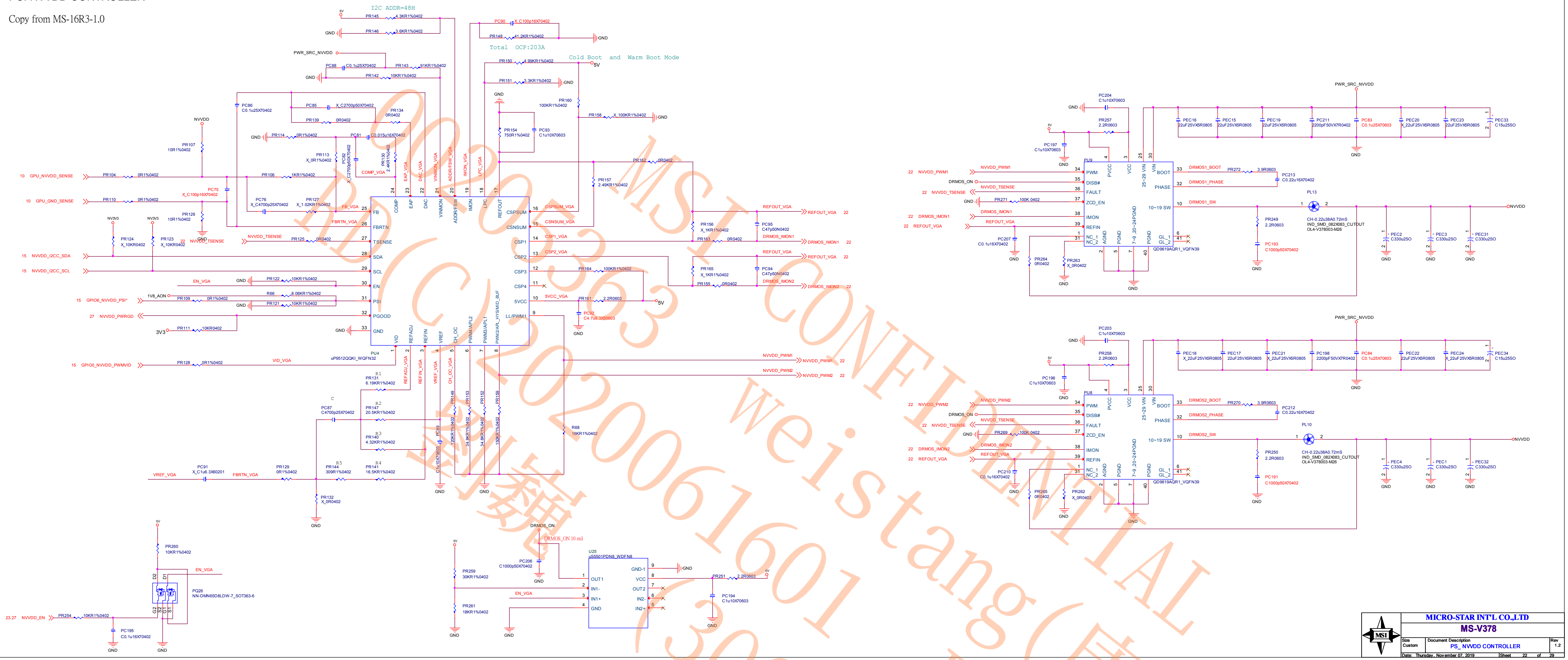
PS: NVVDD CONTROLLER

Copy from MS-16R3-1.0



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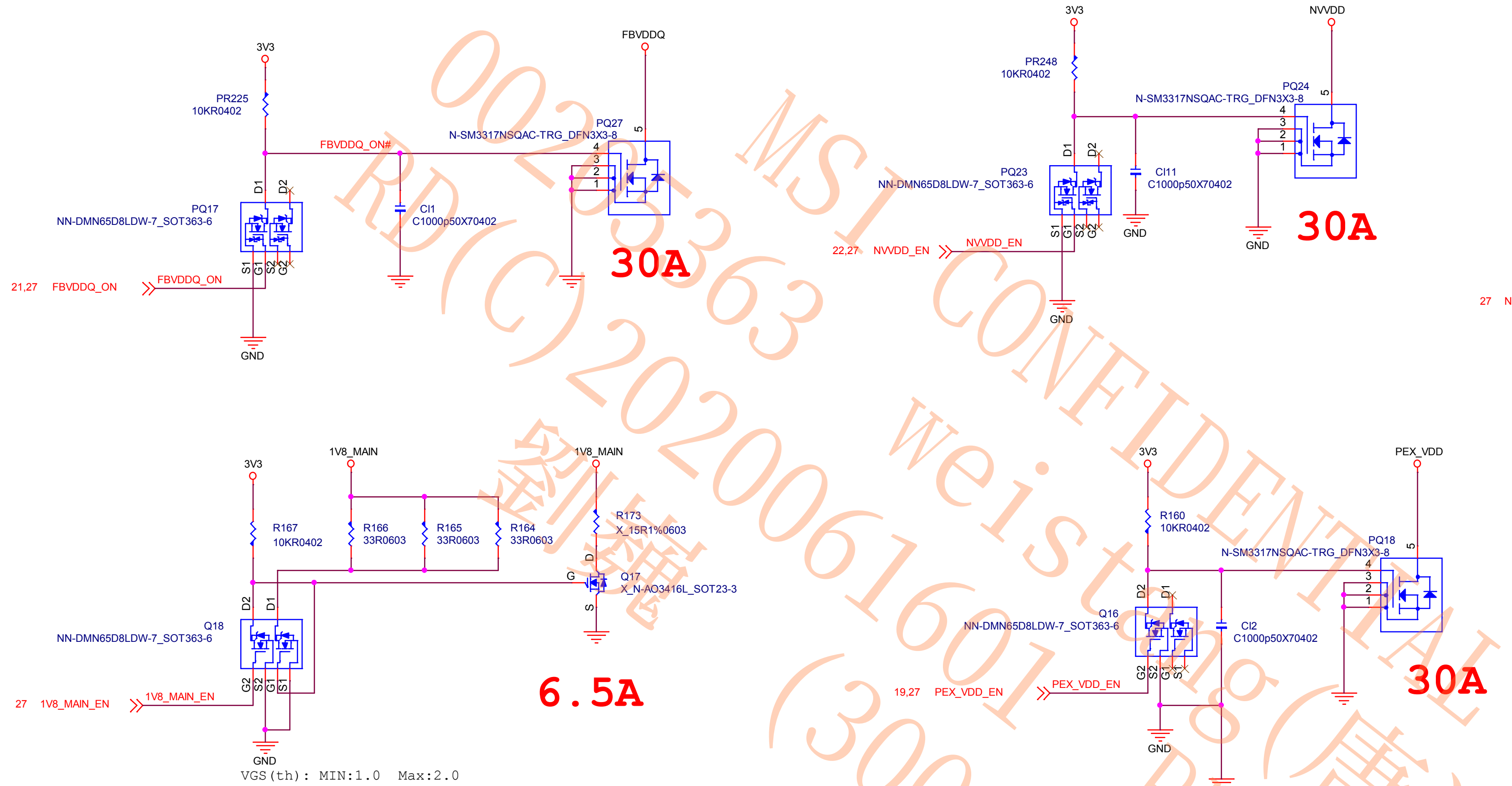
Discharge



VGS(th): MIN:1.0 Max:2.0

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Size	Document Description	Rev
Custom	DISCHARGE	1.2
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Pin Name	**N17P**	**N18P**	**N17P** Functional Description	**N17P** Recommended Default Pull-up or Pull-down	**N18P** Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM	NVVDD_PWM_VID	PWM Output to control NVVDD	0 to 1V8 PWM output	
GPIO1	GC6_FB_EN	GC6_FB_EN	FB Enable for GC6 2.1	OD, 10K pull-down	OD, 10K pull-down
GPIO2	GPU_EVENT#	GPU_EVENT#	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON	10K pull-up to 1V8 _AON
GPIO3	NVVDDS_PWM	UNUSED	PWM output to control the NVVDDS power supply	0 to 1V8 output	
GPIO4	1V8_MAIN_EN	1V8_MAIN_EN	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8 _AON	OD, 10K pull-up to 1V8 _AON
GPIO5	FRM_LCK#	FRM_LCK#	Active low Frame Lock	OD, 10K pull-up to 1V8 _AON	OD, 10K pull-up to 1V8 _AON
GPIO6	NVVDD_PSI	NVVDD_PSI	Phase shedding	10K pull-up to 1V8 _AON	10K pull-up to 1V8 _AON
GPIO7	LCD_BL_PWM	LCD_BL_PWM	Panel Backlight PWM Brighteness Control	100K pull-down	100K pull-down
GPIO8	MEM_VDD_CTL	MEM_VDD_CTL	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	THERM_ALERT	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	MEM_VREF_CTL	Memory VREF Control	100K pull-down	100K pull-down
GPIO11	LCD_VCC	LCD_VCC	Panel Power Enable	100K pull-down	100K pull-down
GPIO12	PWR_LEVEL	PWR_LEVEL	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON	10K pull-up to 1V8_AON
GPIO13	LCD_BLEN	UNUSED	Panel Backlight Enable	100K pull-down	
GPIO14	HPD_A	HPD_A	Hot Plug Detect for IFPA		10K pull-up to 1V8 _AON
GPIO15	HPD_B	HPD_B	Hot Plug Detect for IFPB		10K pull-up to 1V8 _AON
GPIO16	SYS_PEX_RST_MON#	UNUSED	System side PCIe reset monitor	10K pull-up to 1V8 _AON	
GPIO17	HPD_D	HPD_D	Hot Plug Detect for IFPD		10K pull-up to 1V8 _AON
GPIO18	HPD_E	HPD_E	Hot Plug Detect for IFPE		10K pull-up to 1V8 _AON
GPIO19	3DVision	UNUSED	3D Vision L/R signal	100K pull-down	
GPIO20	GC5_MODE	NB_GC6			10K pull-down
GPIO21	UNUSED	LCD_BLEN			100K pull-down
GPIO22	UNUSED	ADC_MUX_SEL			2.2K pull-up See Circuit
GPIO23	GPU_PEX_RST_HOLD#	RESERVED	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3	100K pull-down
GPIO24	HPD_F	UNUSED	Hot Plug Detect for IFPF		
GPIO25	UNUSED	FBVDD_PSI#			
GPIO26	UNUSED	FP_FUSE			10K pull-down
GPIO27	HPD_C	HPD_C	Hot Plug Detect for IFPC		10K pull-up to 1V8 _AON

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GPIO Functional Description
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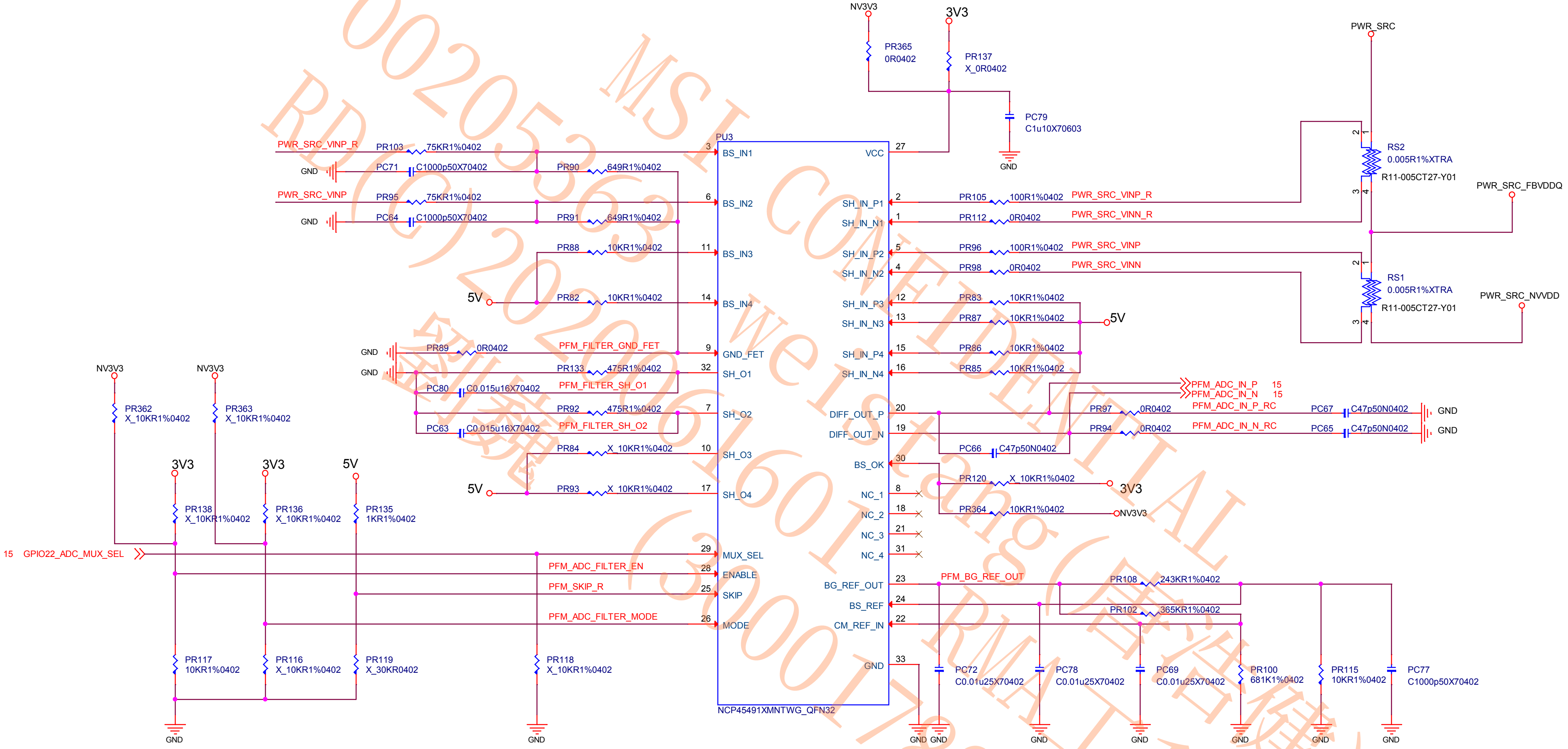
INPUT PREFILTER

On Semi	PR90,PR91	PR92,PR133	PR108	PR95,PR103	PC64,PC71
CONFIG	R954,R924	R977,R923	R950	R953,R952	C841,C836
N18P-G0	649R	475R	243K	75K	1.0nF



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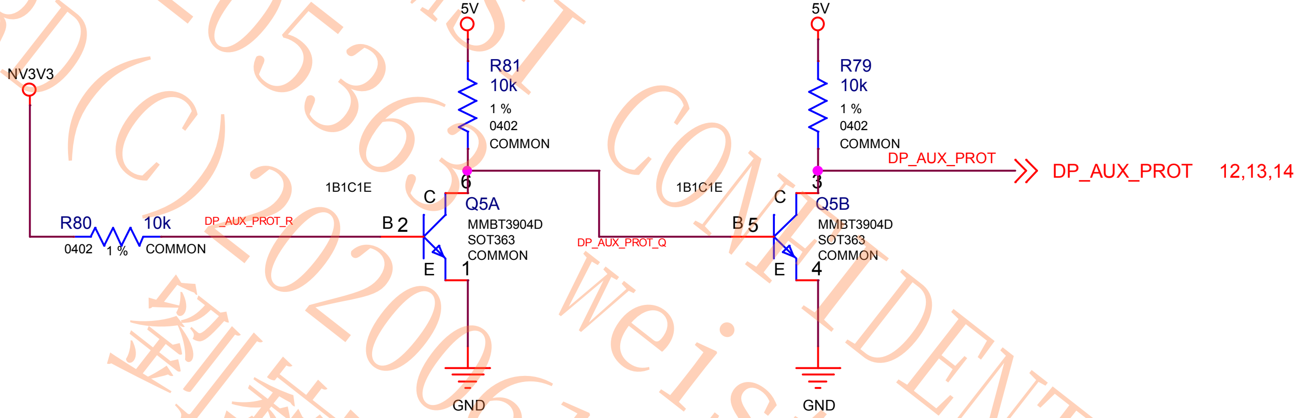
SEQUENCE:5V,1V8,NV3V3 ENABLE



DP_AUX Protection

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Size A	Document Description DP_AUX Protection	Rev 1.2

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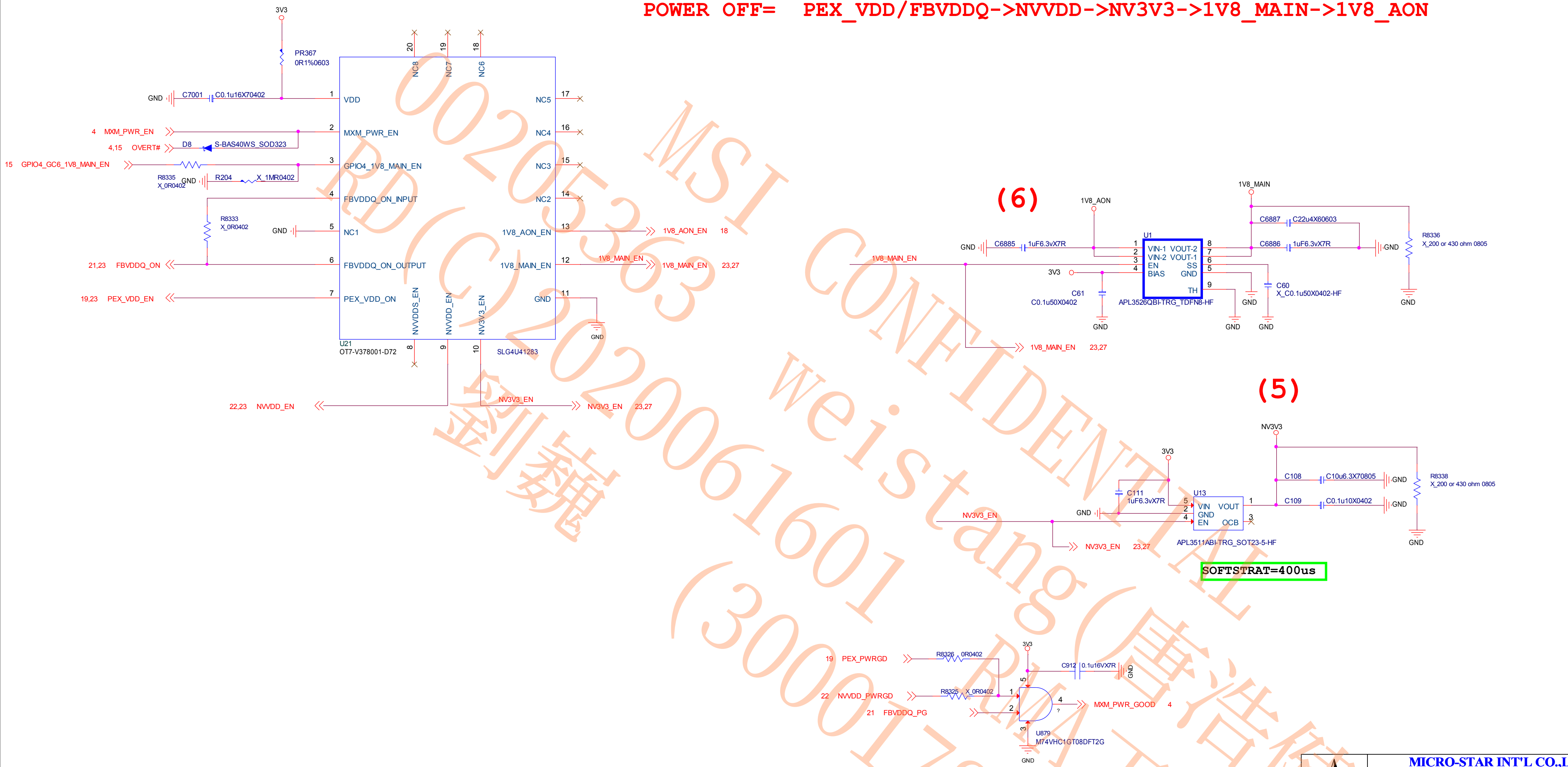
Power Sequence Control

POWER ON= 1V8_AON->1V8_MAIN->NV3V3->NVVDD->PEX_VDD->FBVDDQ->DGPU_PWRGD

POWER OFF= PEX_VDD/FBVDDQ->NVVDD->NV3V3->1V8_MAIN->1V8_AON



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SEQUENCE:DISCHARGE

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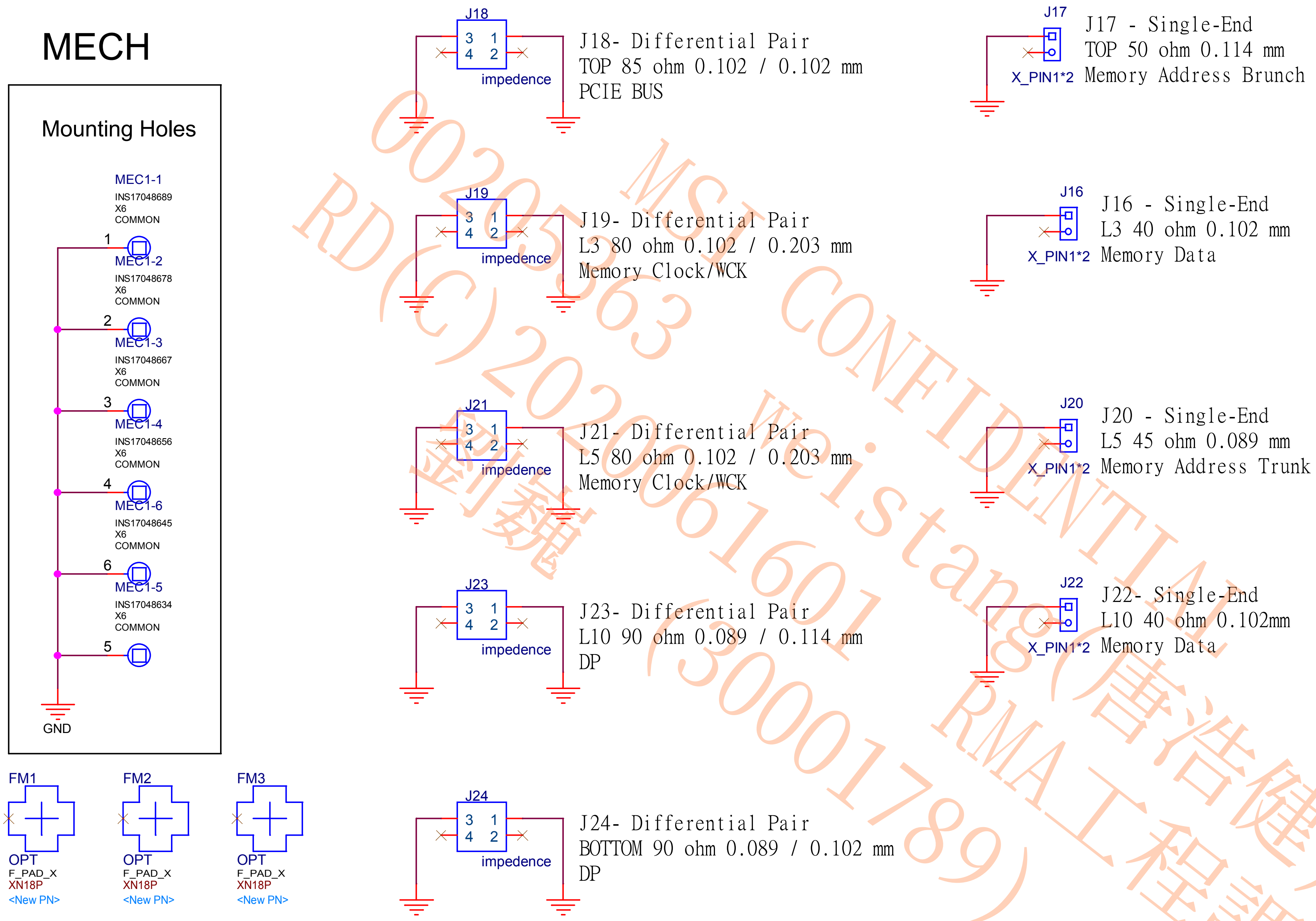
MECH



J18- Differential Pair
TOP 85 ohm 0.102 / 0.102 mm
PCIE BUS

J19- Differential Pair
L3 80 ohm 0.102 / 0.203 mm
Memory Clock/WCK

J21- Differential Pair
L5 80 ohm 0.102 / 0.203 mm
Memory Clock/WCK

J23- Differential Pair
L10 90 ohm 0.089 / 0.114 mm
DP

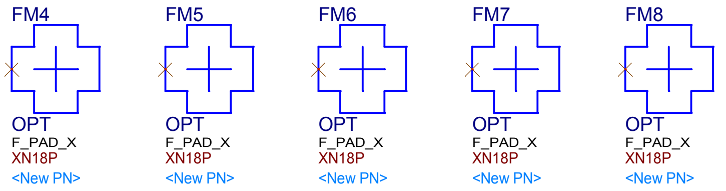
J24- Differential Pair
BOTTOM 90 ohm 0.089 / 0.102 mm
DP

J17 - Single-End
TOP 50 ohm 0.114 mm
Memory Address Brunch

J16 - Single-End
L3 40 ohm 0.102 mm
Memory Data

J20 - Single-End
L5 45 ohm 0.089 mm
Memory Address Trunk

J22- Single-End
L10 40 ohm 0.102mm
Memory Data



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