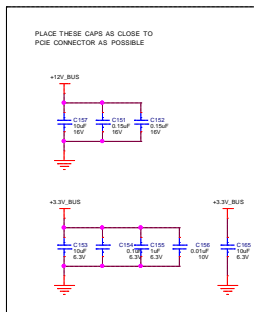
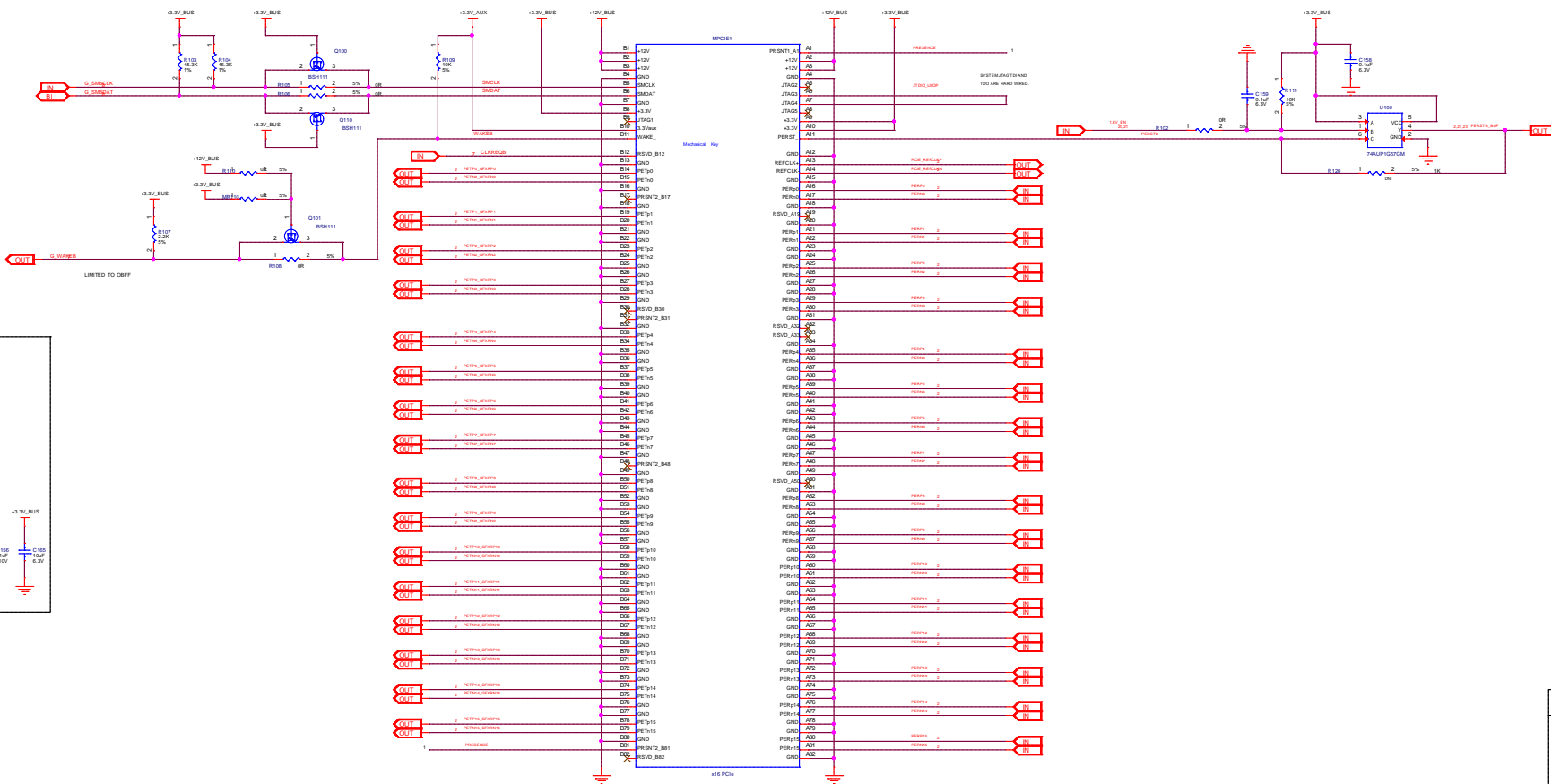


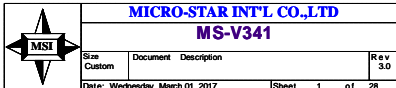


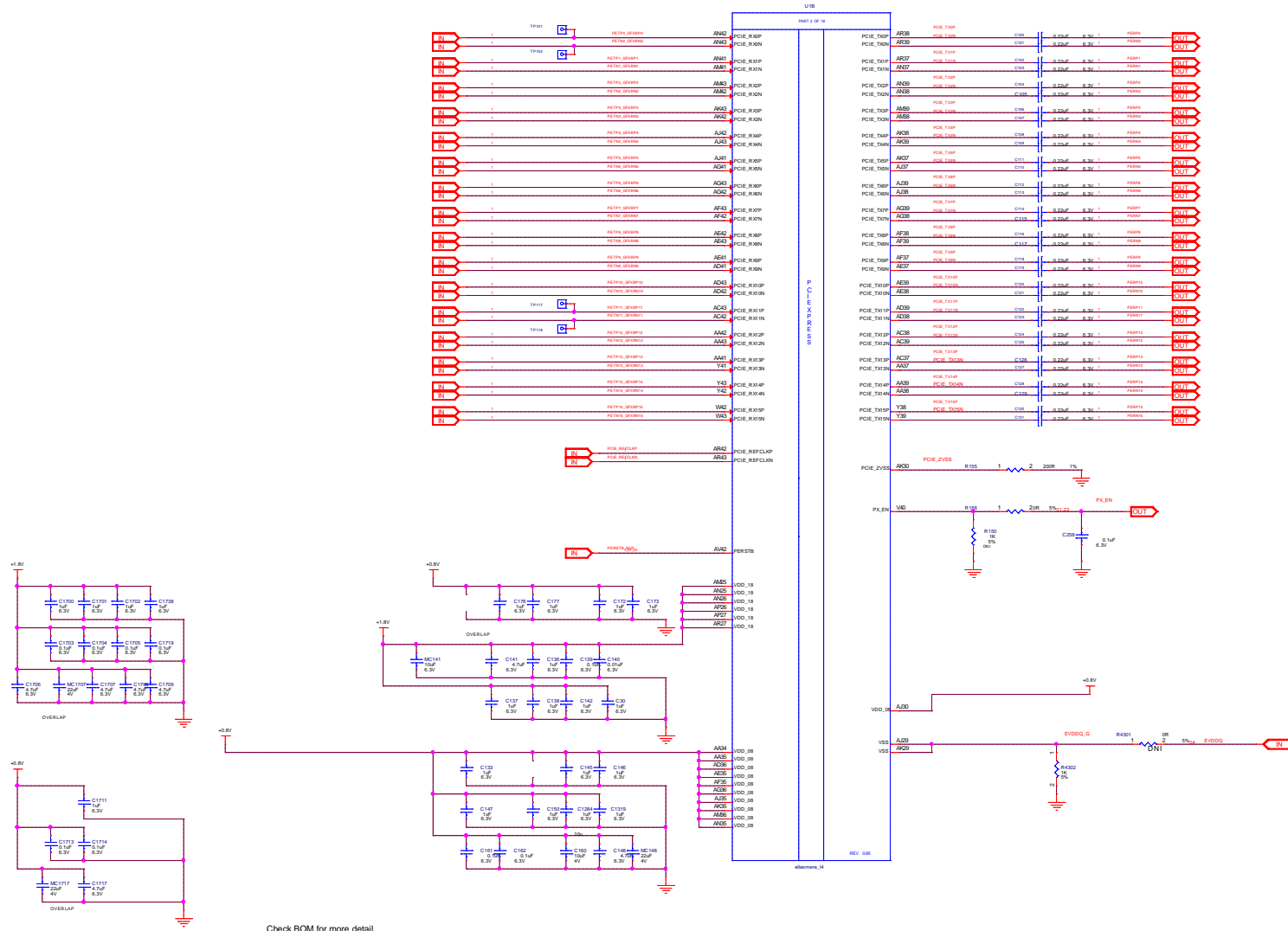
### (1) PCI-EXPRESS EDGE CONNECTOR



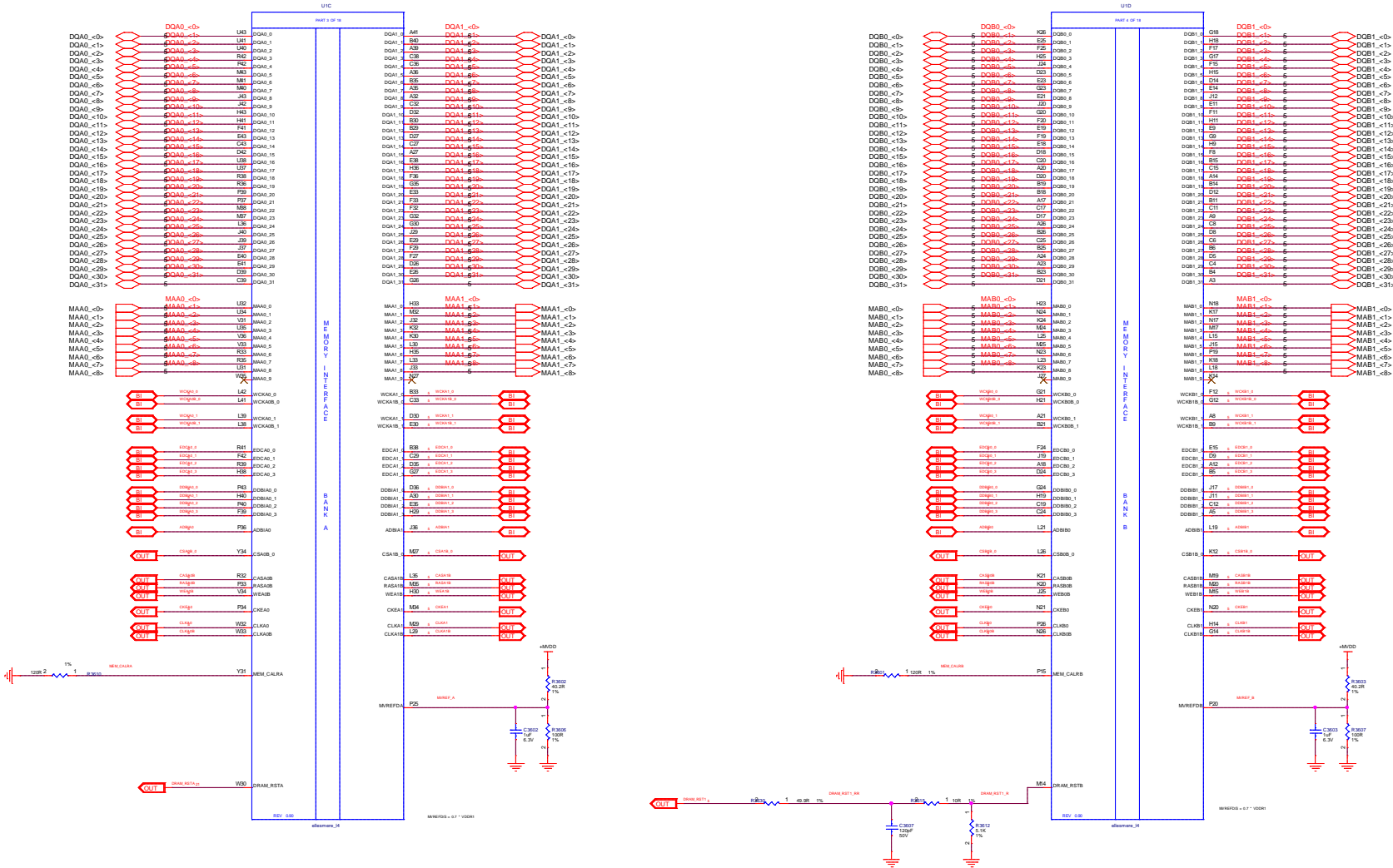
SYMBOL LEGEND	
DN1	DO NOT INSTALL
S-G#	ACTIVE LOW
BUO	BURST UP ONLY
	DIGITAL GROUND
	ANALOG GROUND



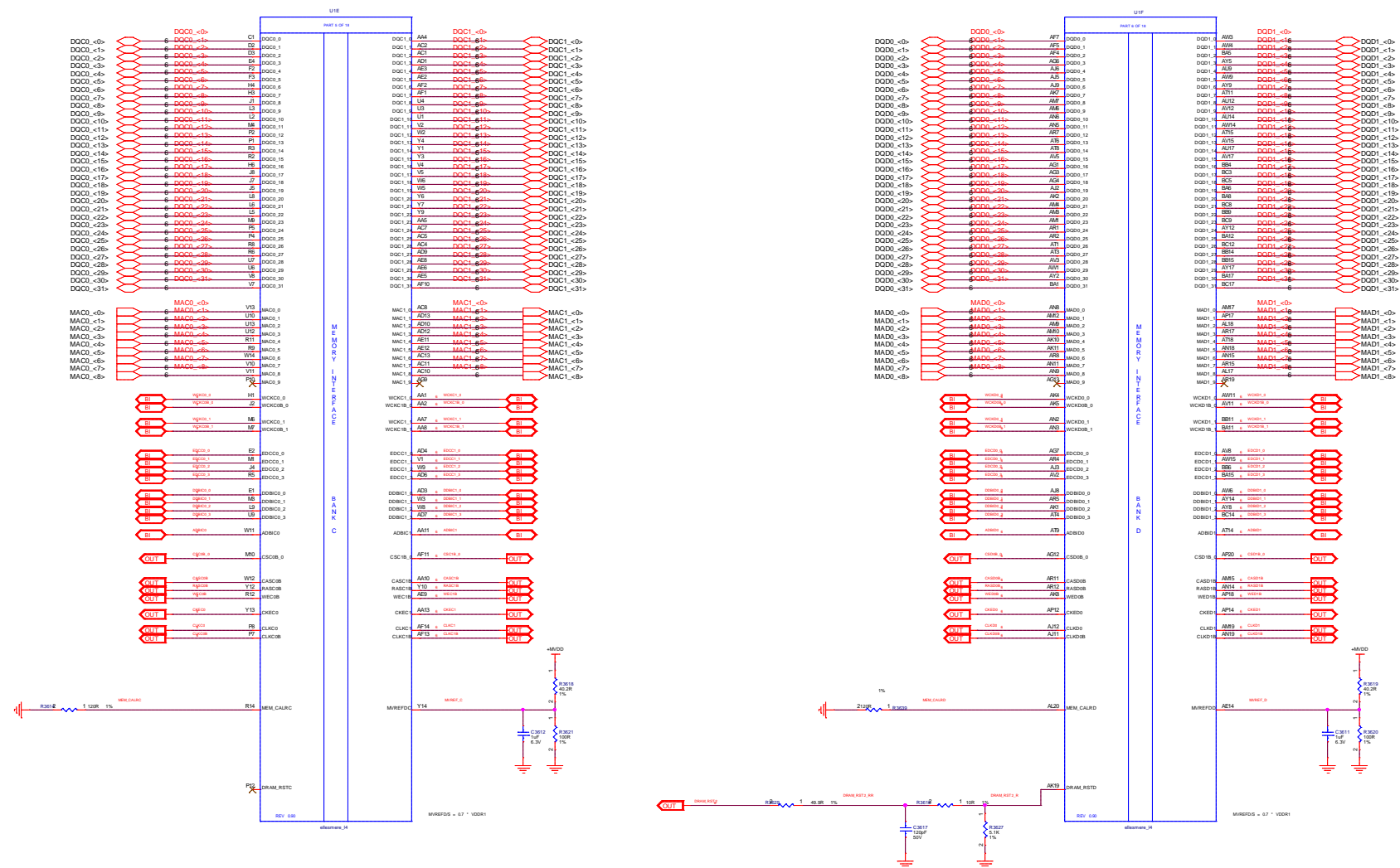
## (2) ELLESMERE PCIE INTERFACE



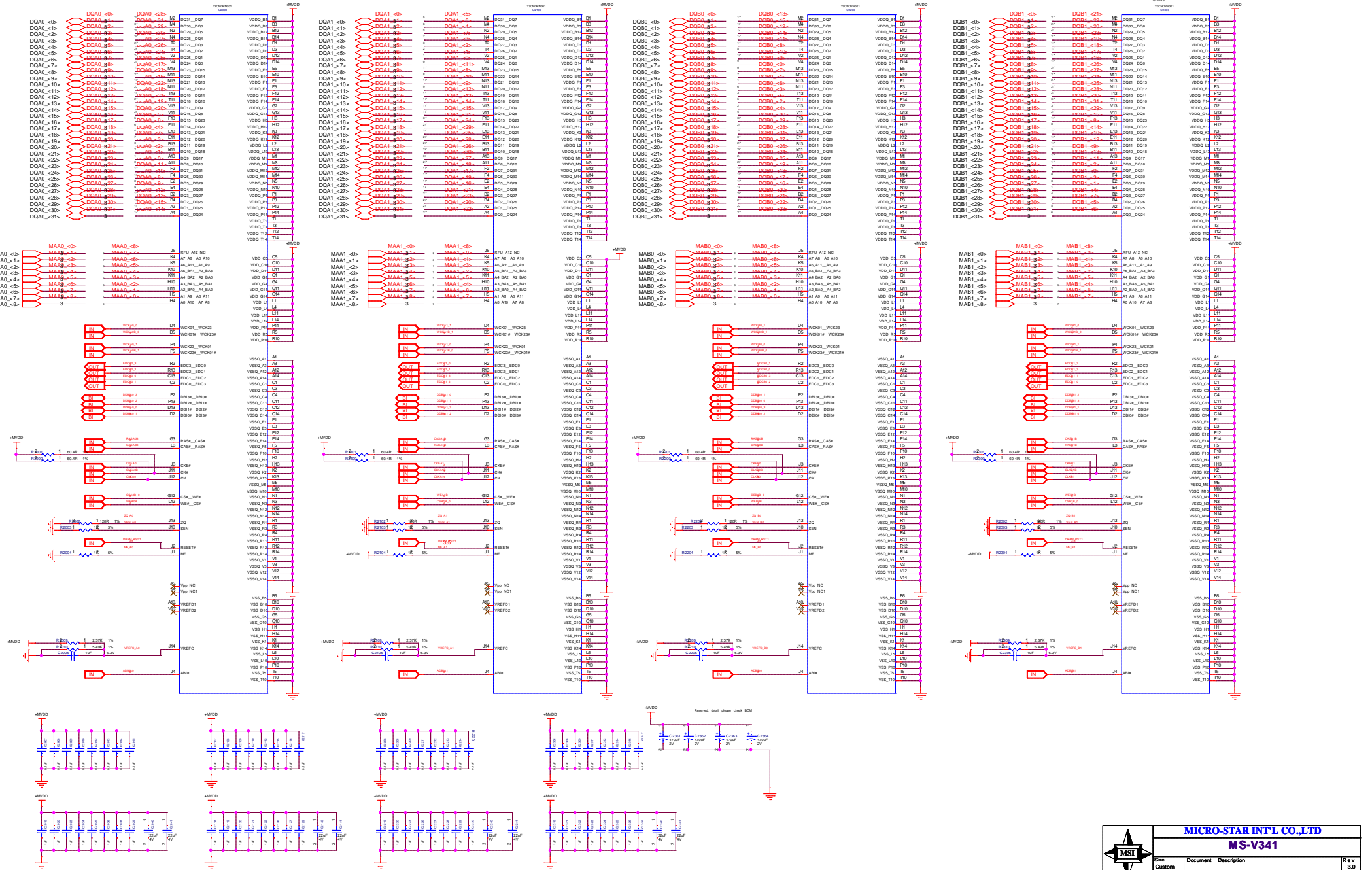
(3) ELLESMERE MEM INTERFACE CH A/B



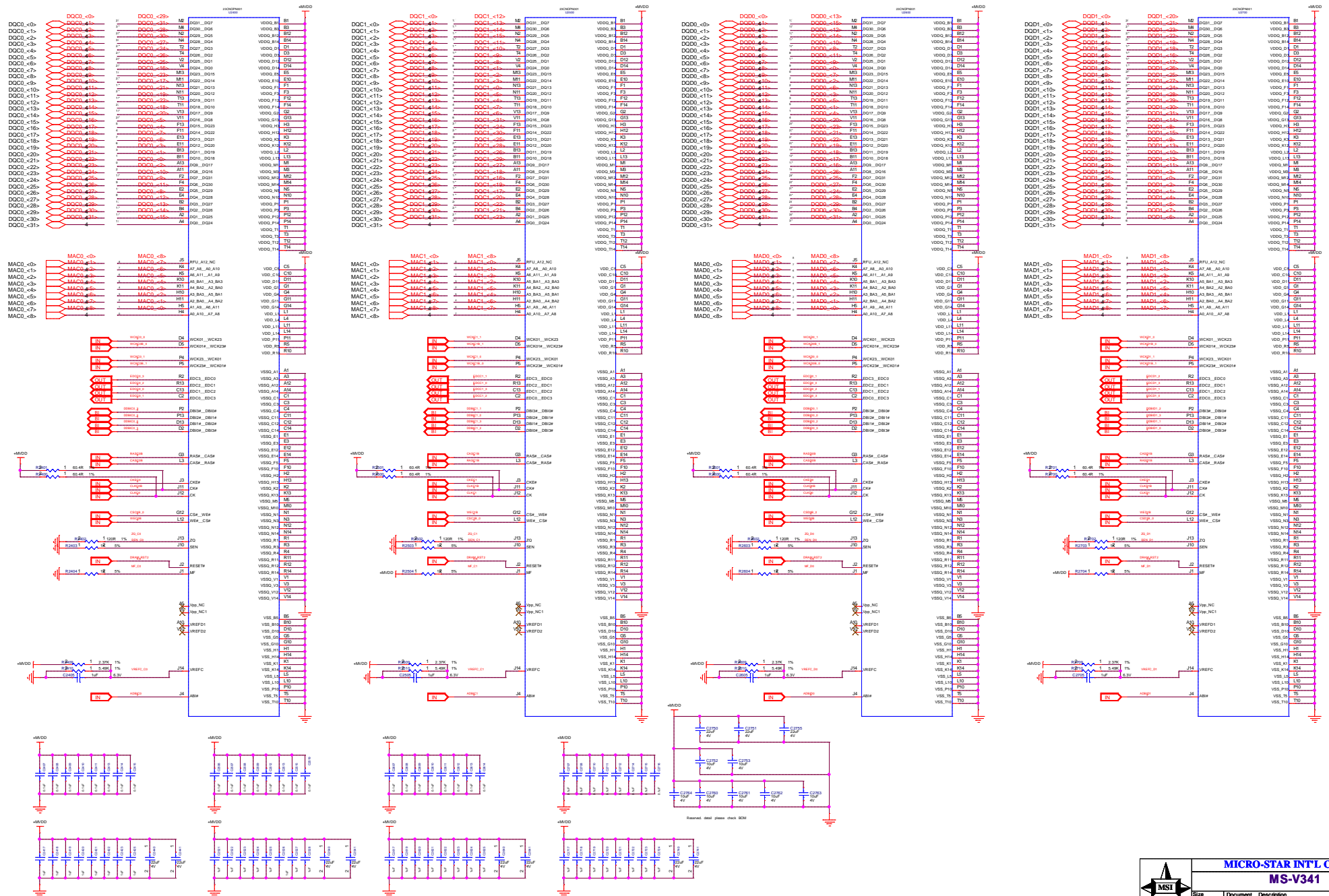
## (4) ELLESMERE MEM INTERFACE CH C/D



## (5) GDDR5 MEMORY CH A/B



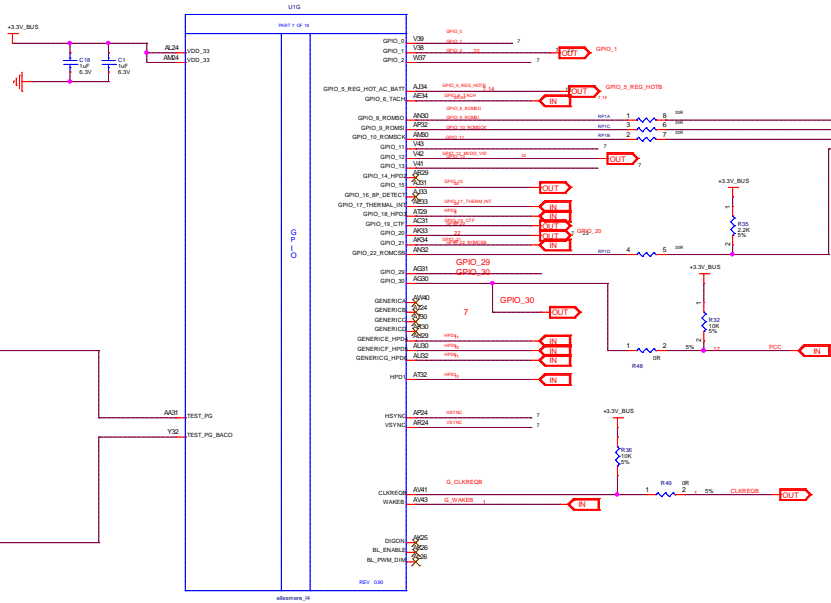
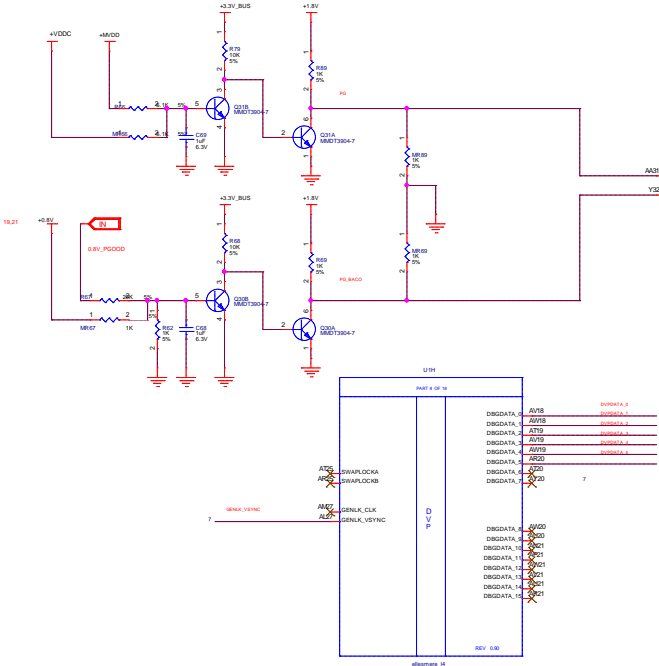
## (6) GDDR5 MEMORY CH C/D



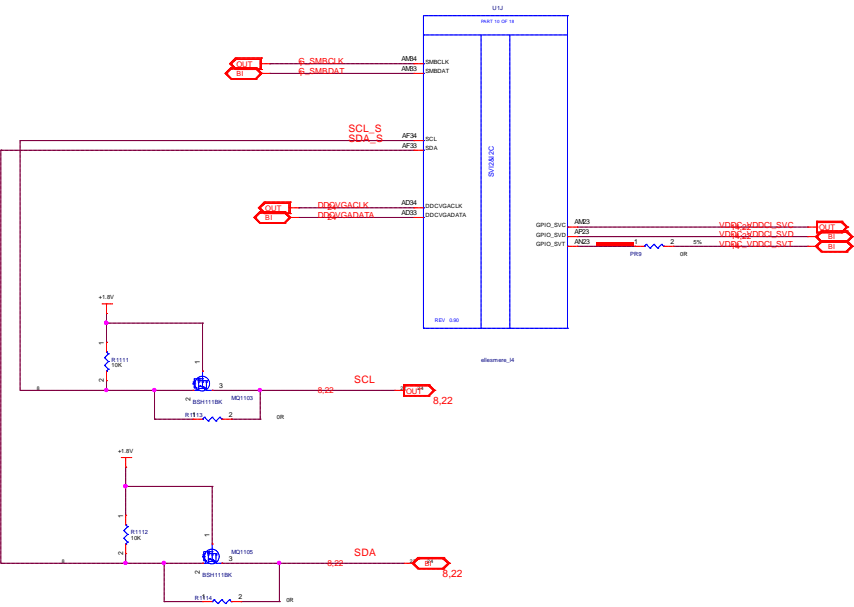


(7) ELLESMERE GPIO STRAP CF XTAL

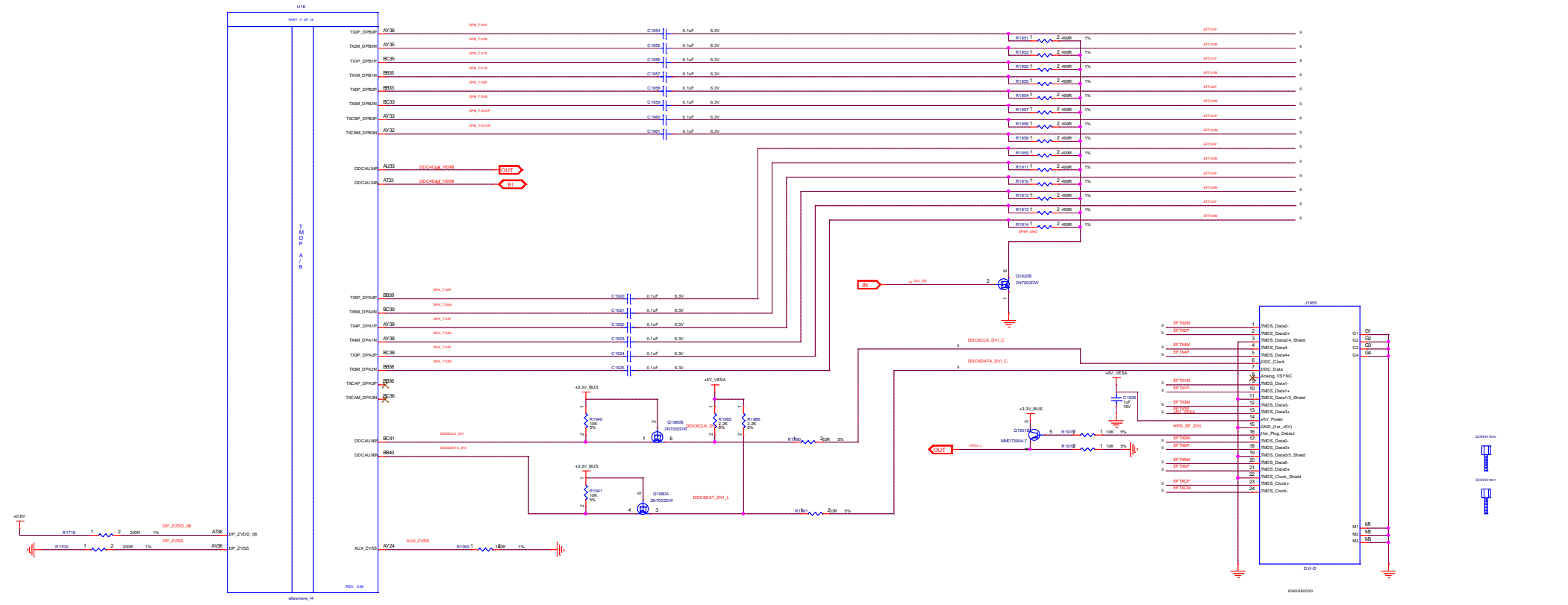
SCB02A BUS		
IC ADDRESS	FUNCTION	DEVICE
DDCVGA BUS		
IC ADDRESS	FUNCTION	DEVICE
0400	EXT TEMP SENSOR	LMP8050



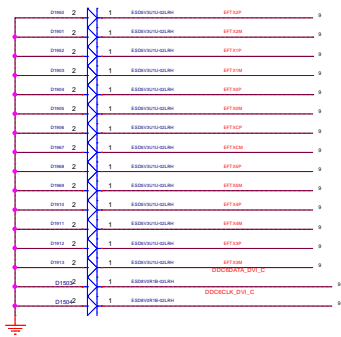
(8) ELLESMERE DAC1 LOCK

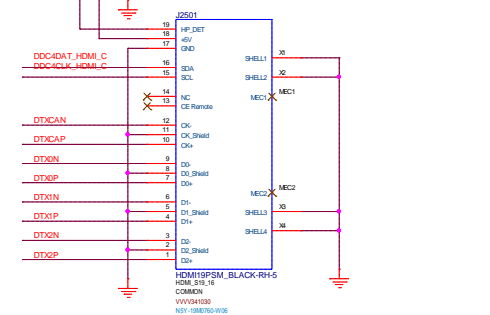
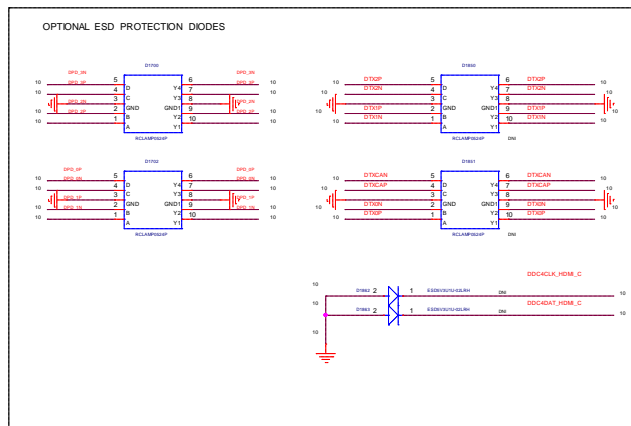
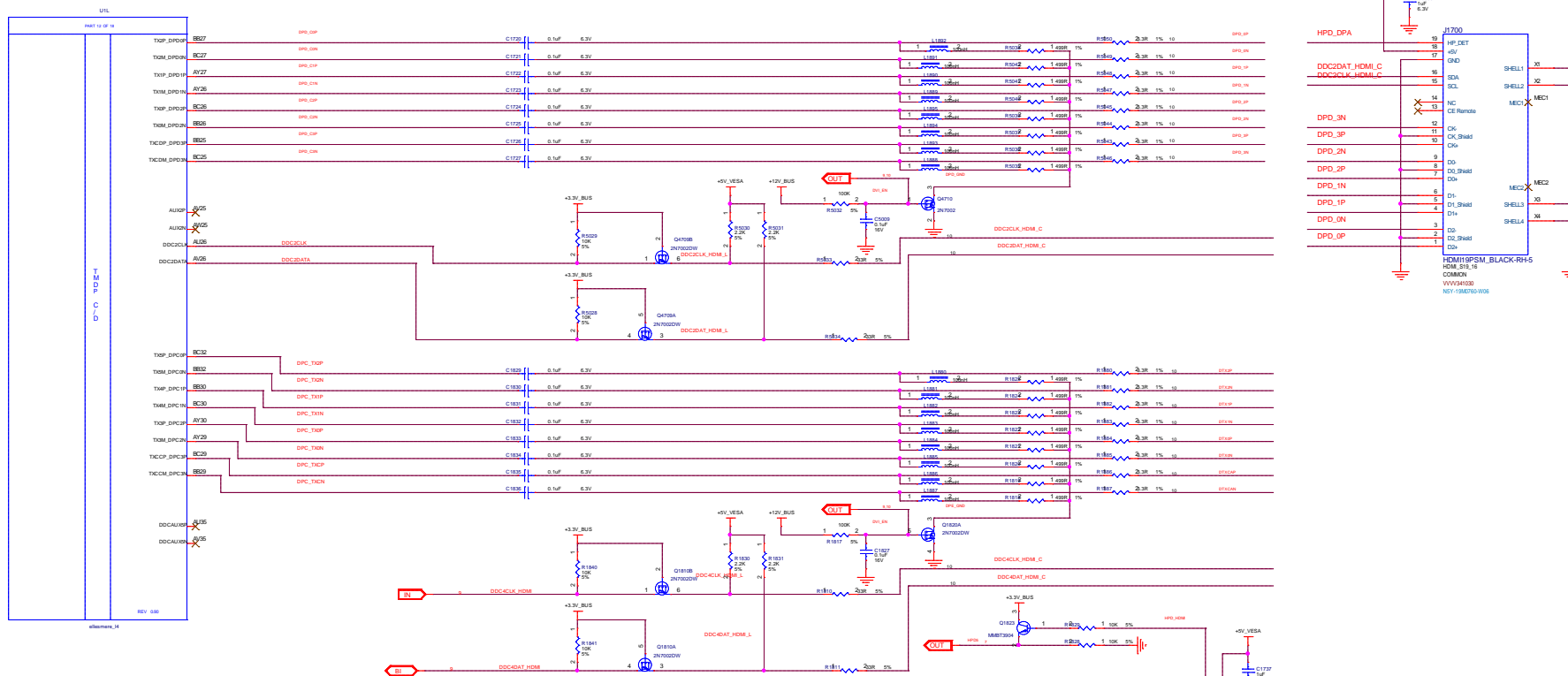


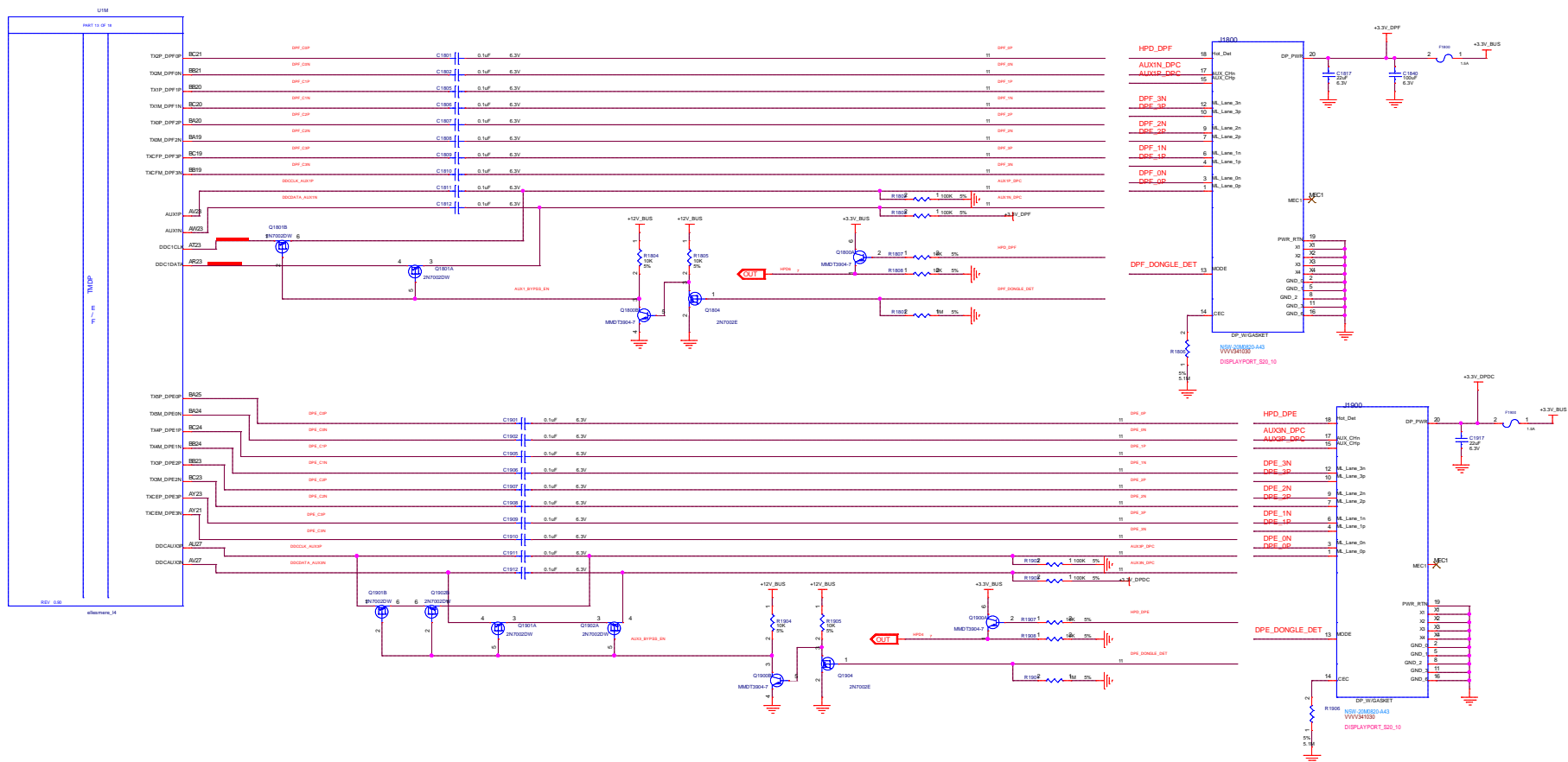




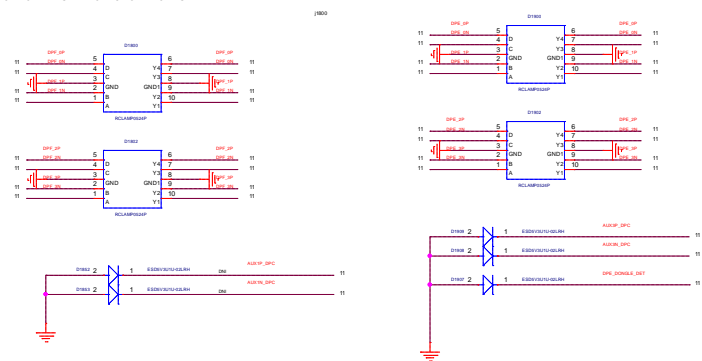
OPTIONAL ESD PROTECTION DIODES



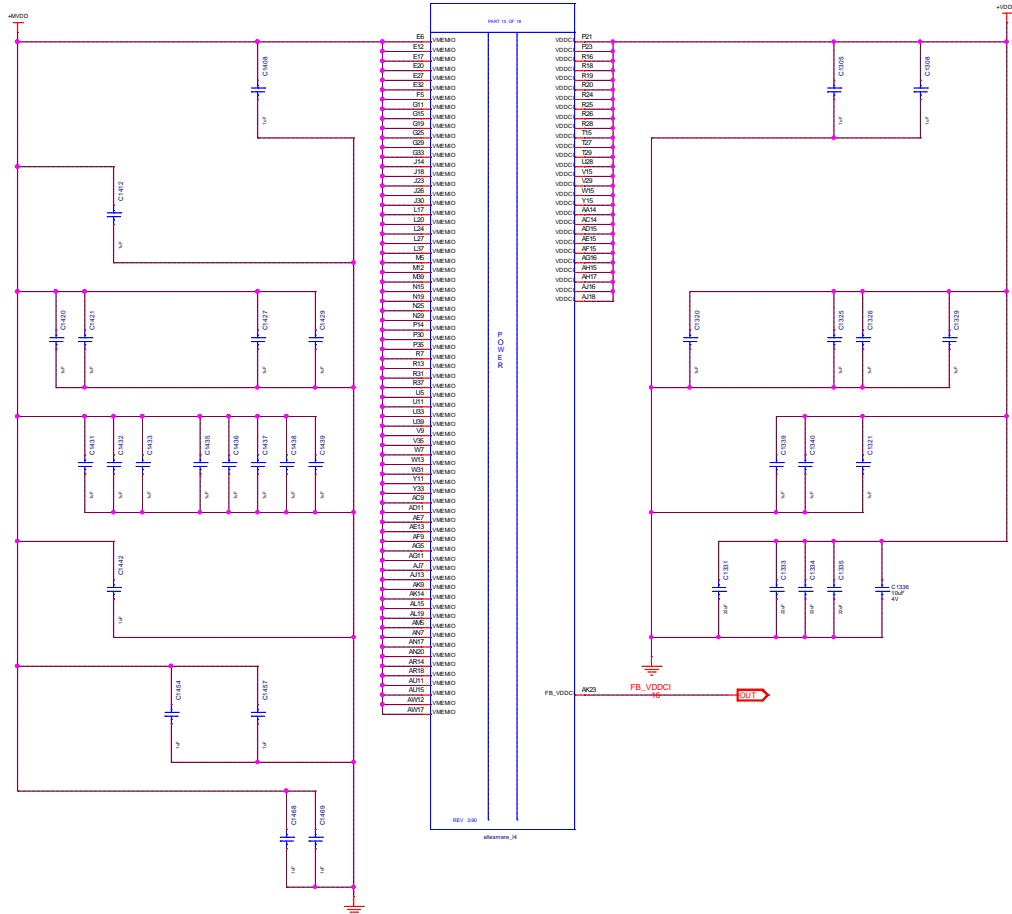
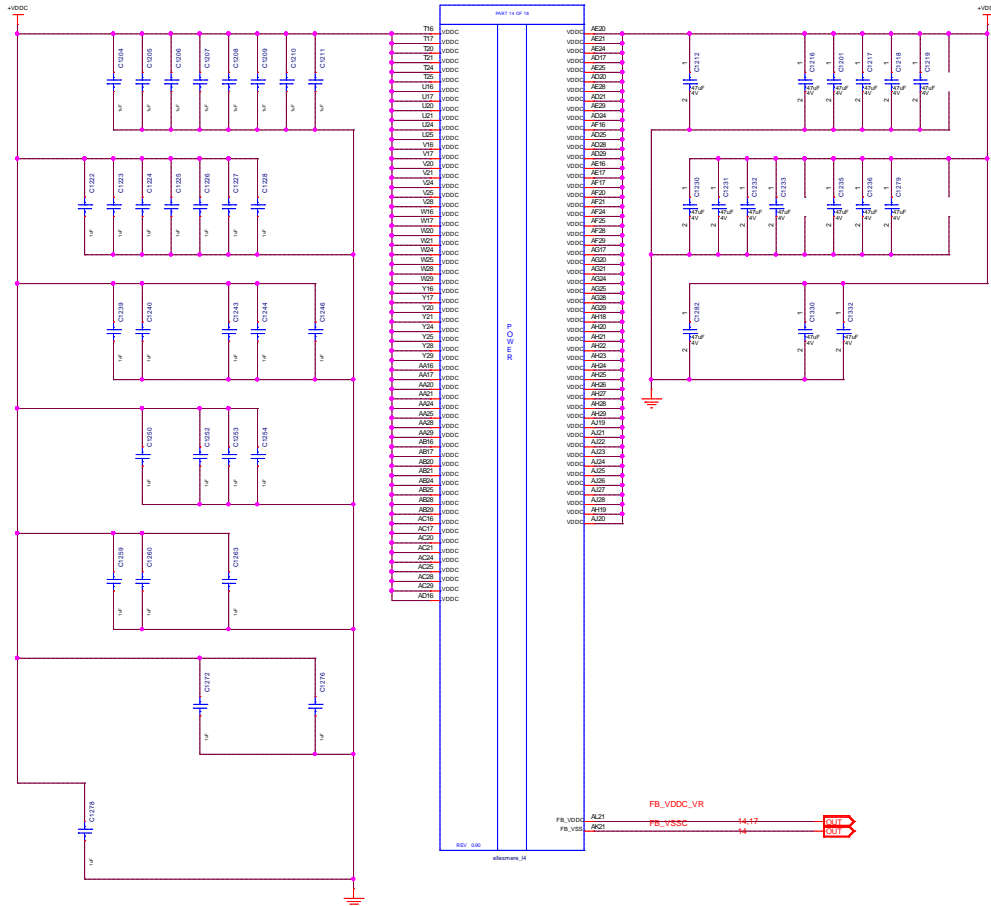




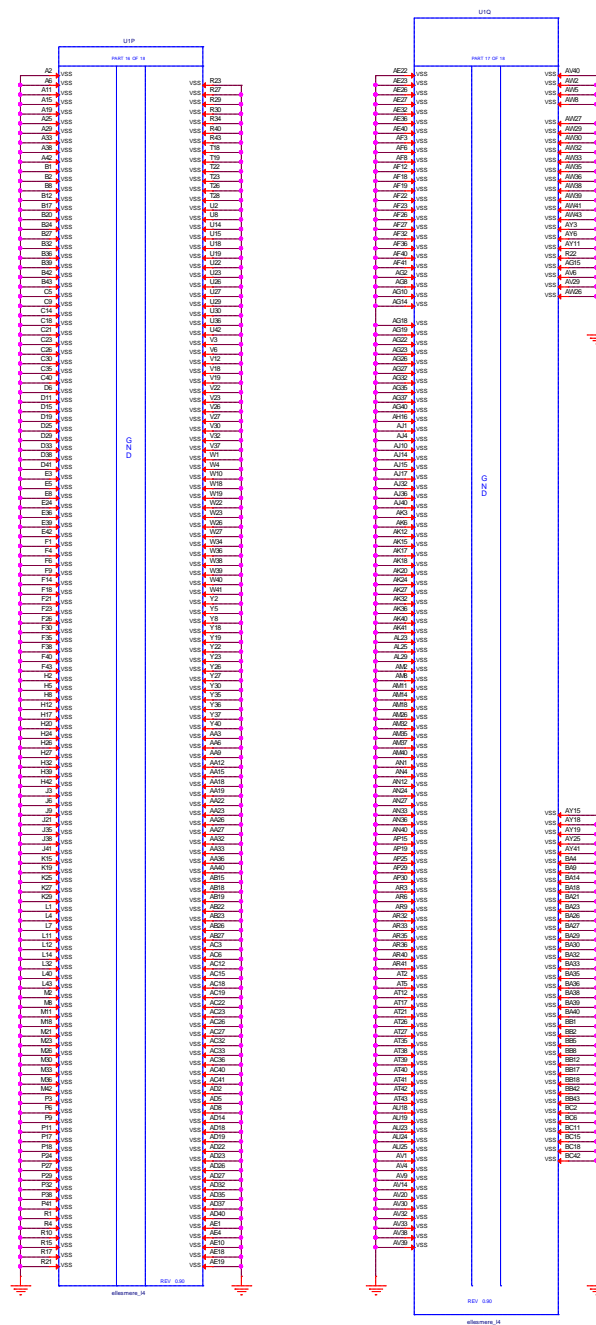
### OPTIONAL ESD PROTECTION DIODES

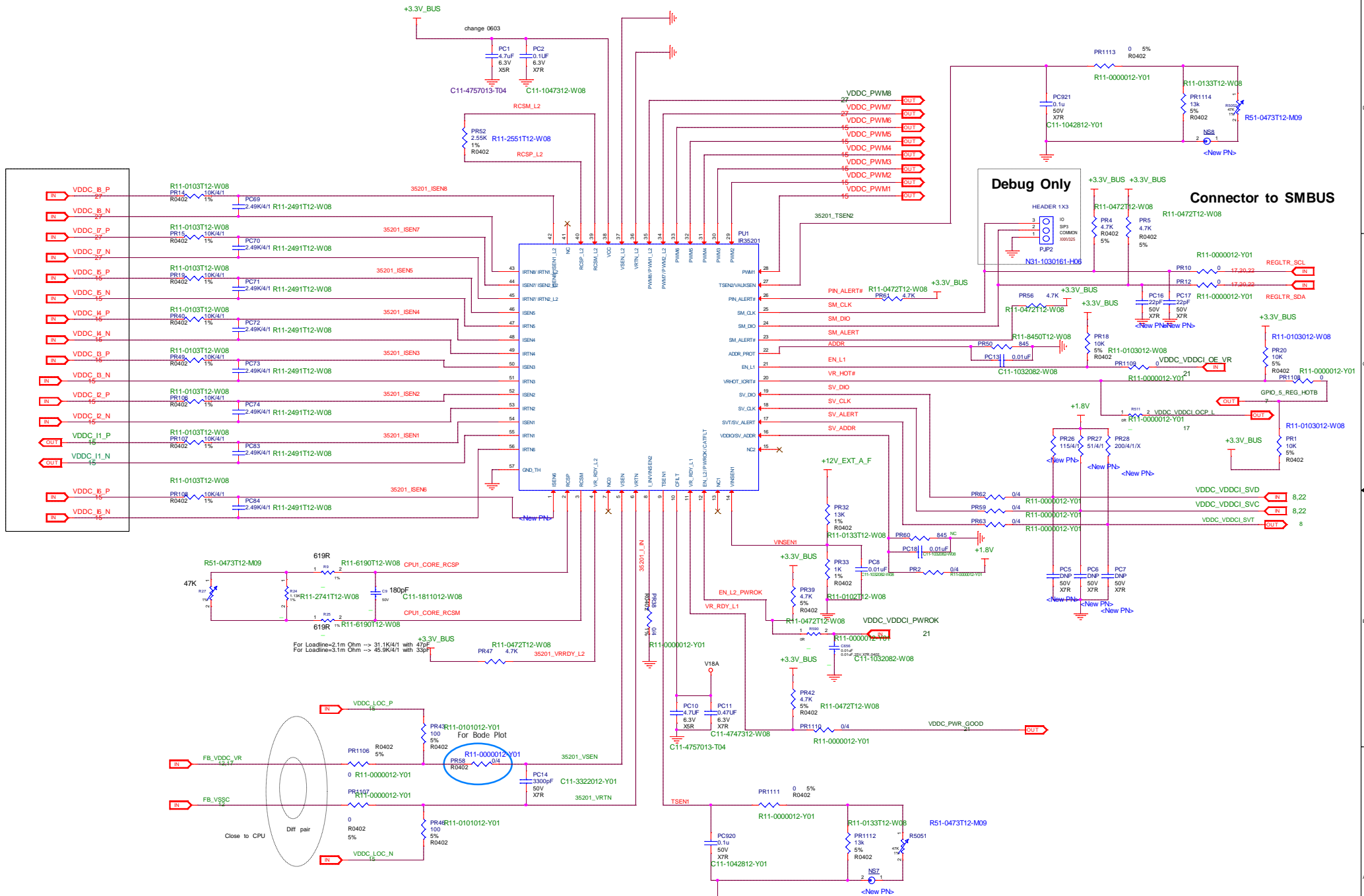


(12) ELLESMERE POWER

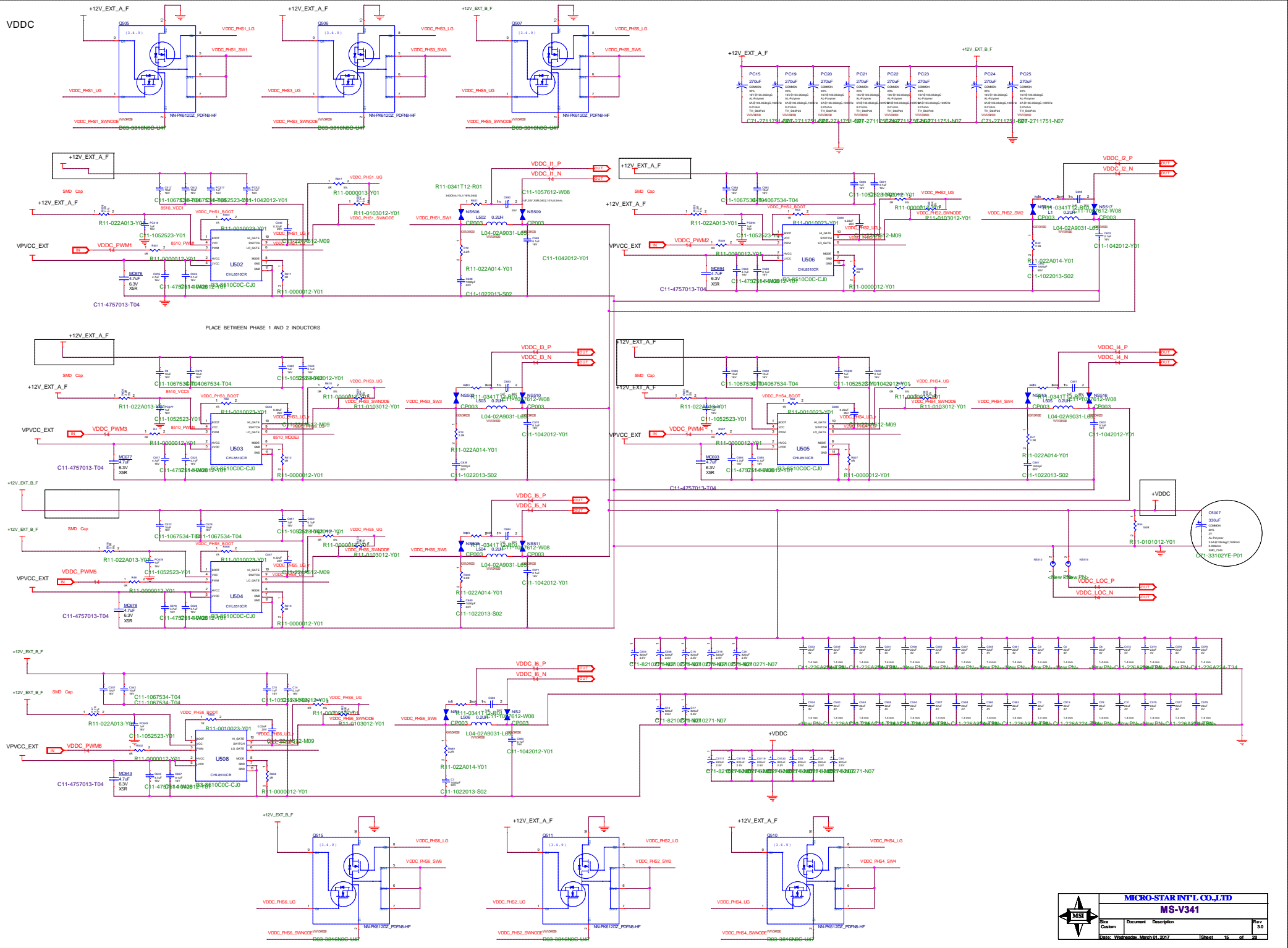


(13) ELLESMERE GROUND

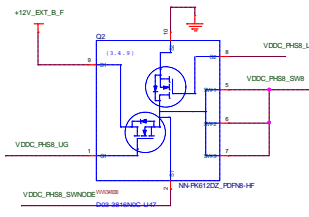
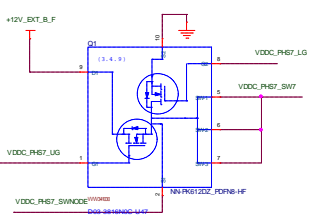
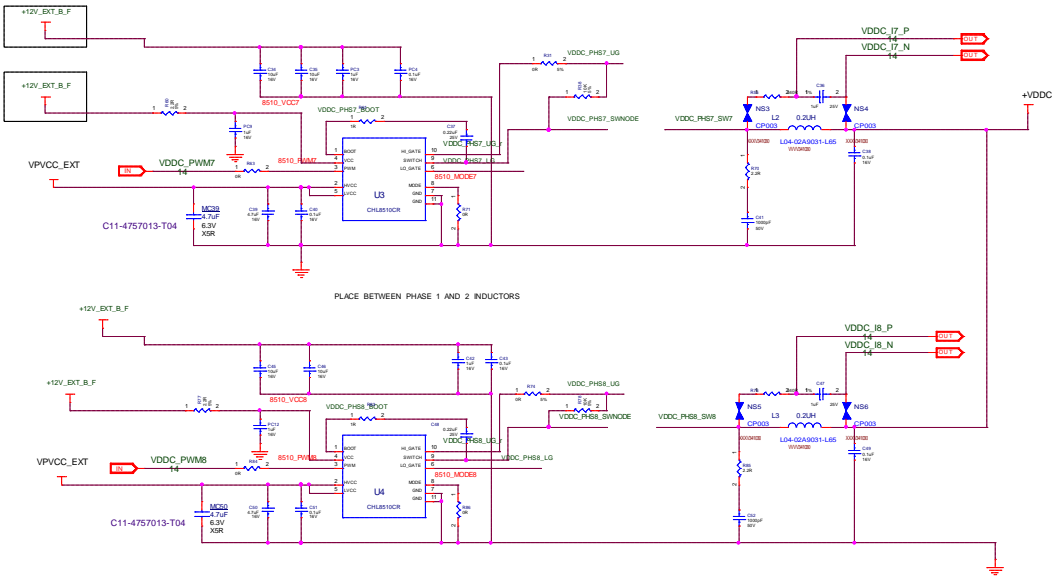




VDDC

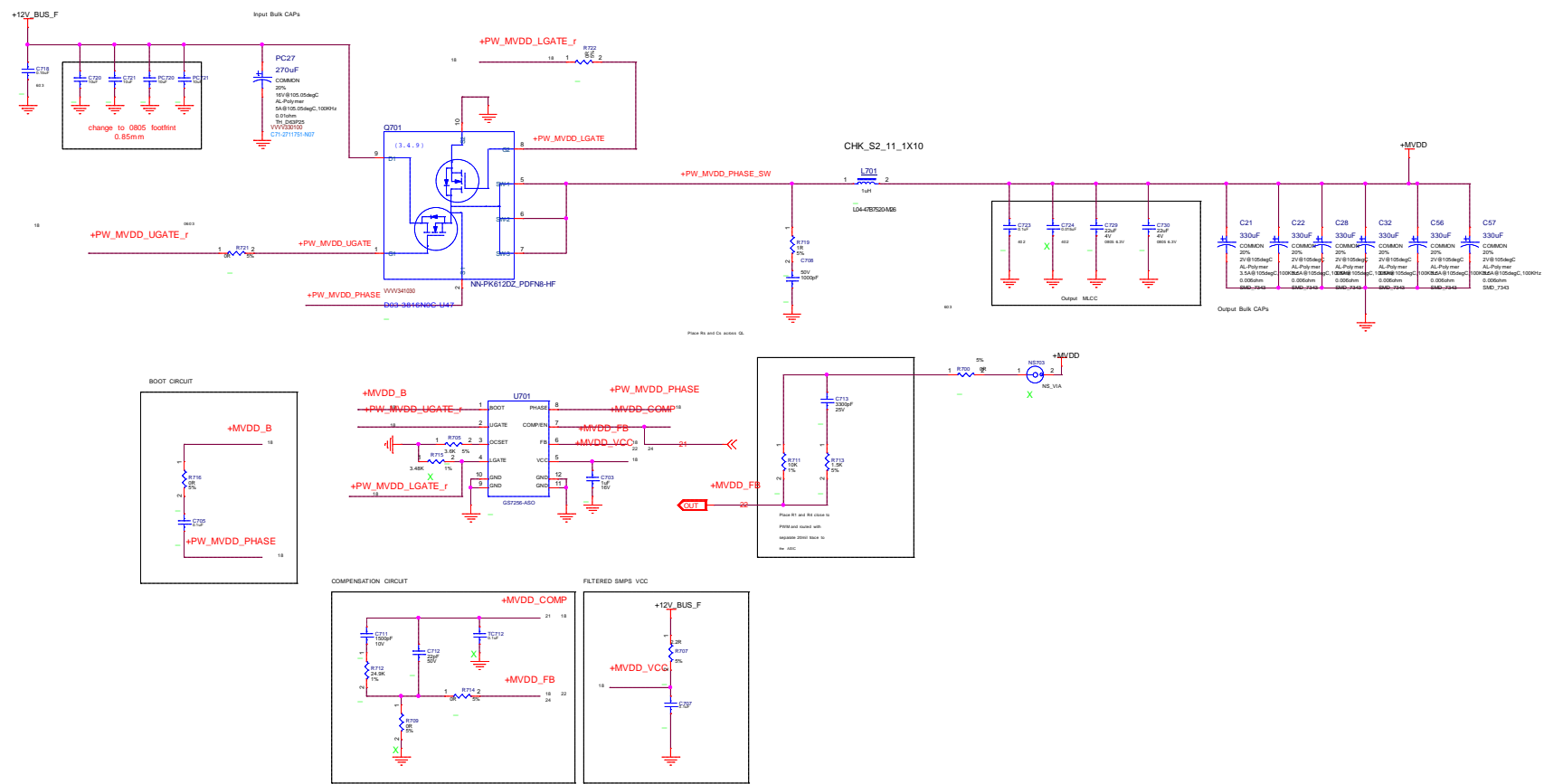




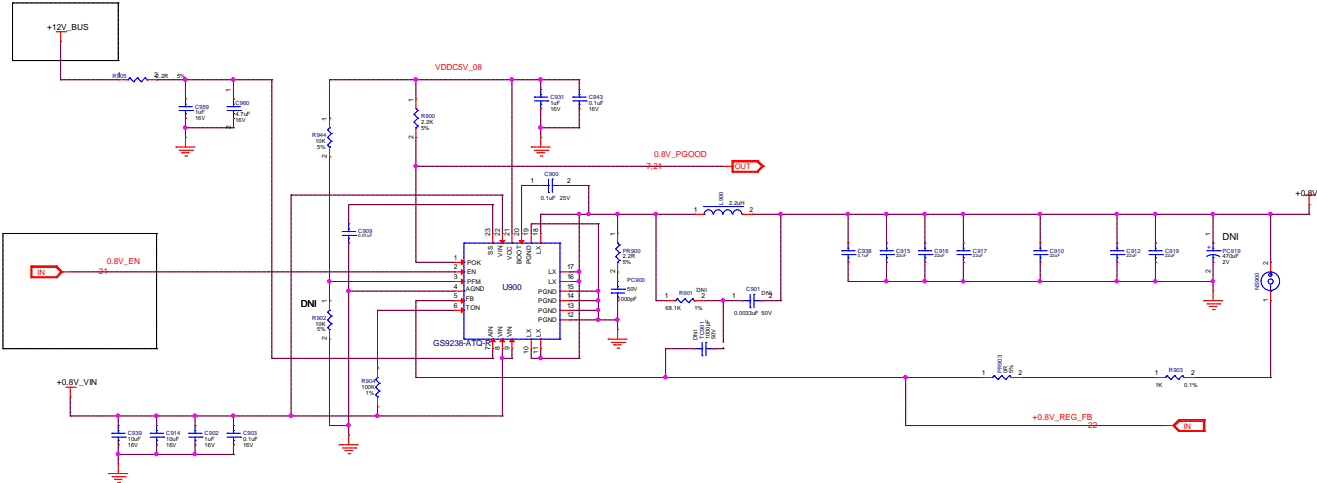








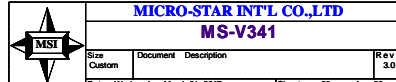
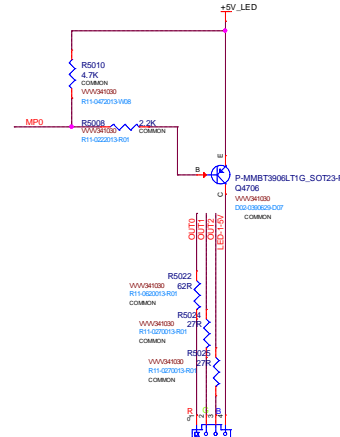
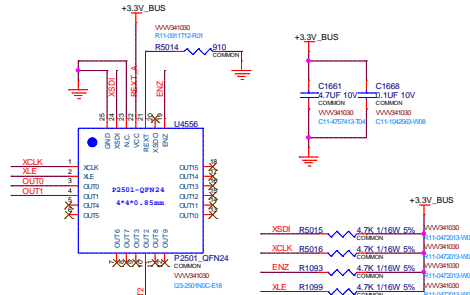
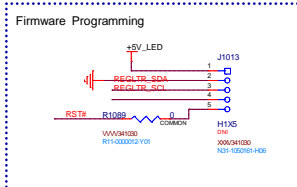
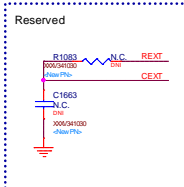
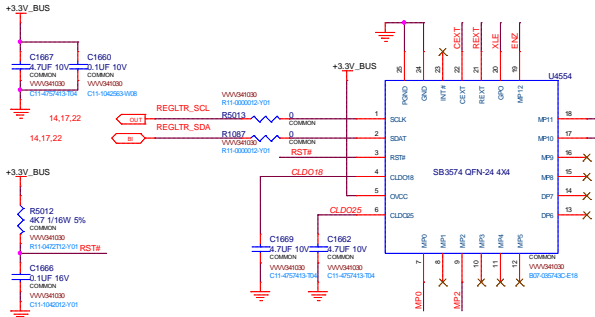
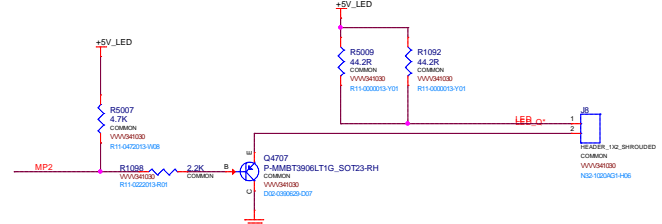
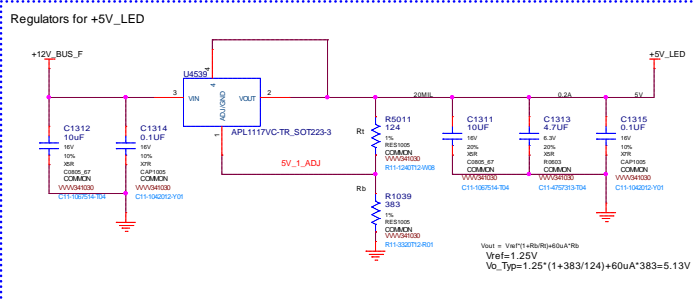
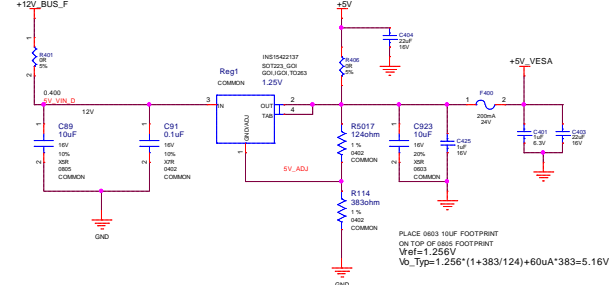
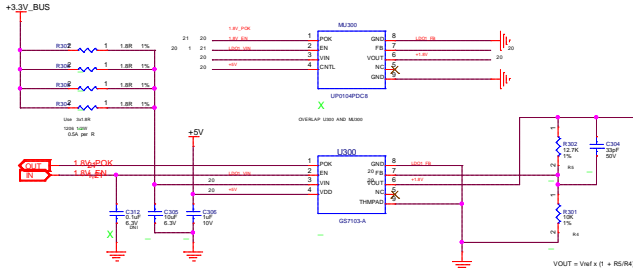
(17) 0.95V



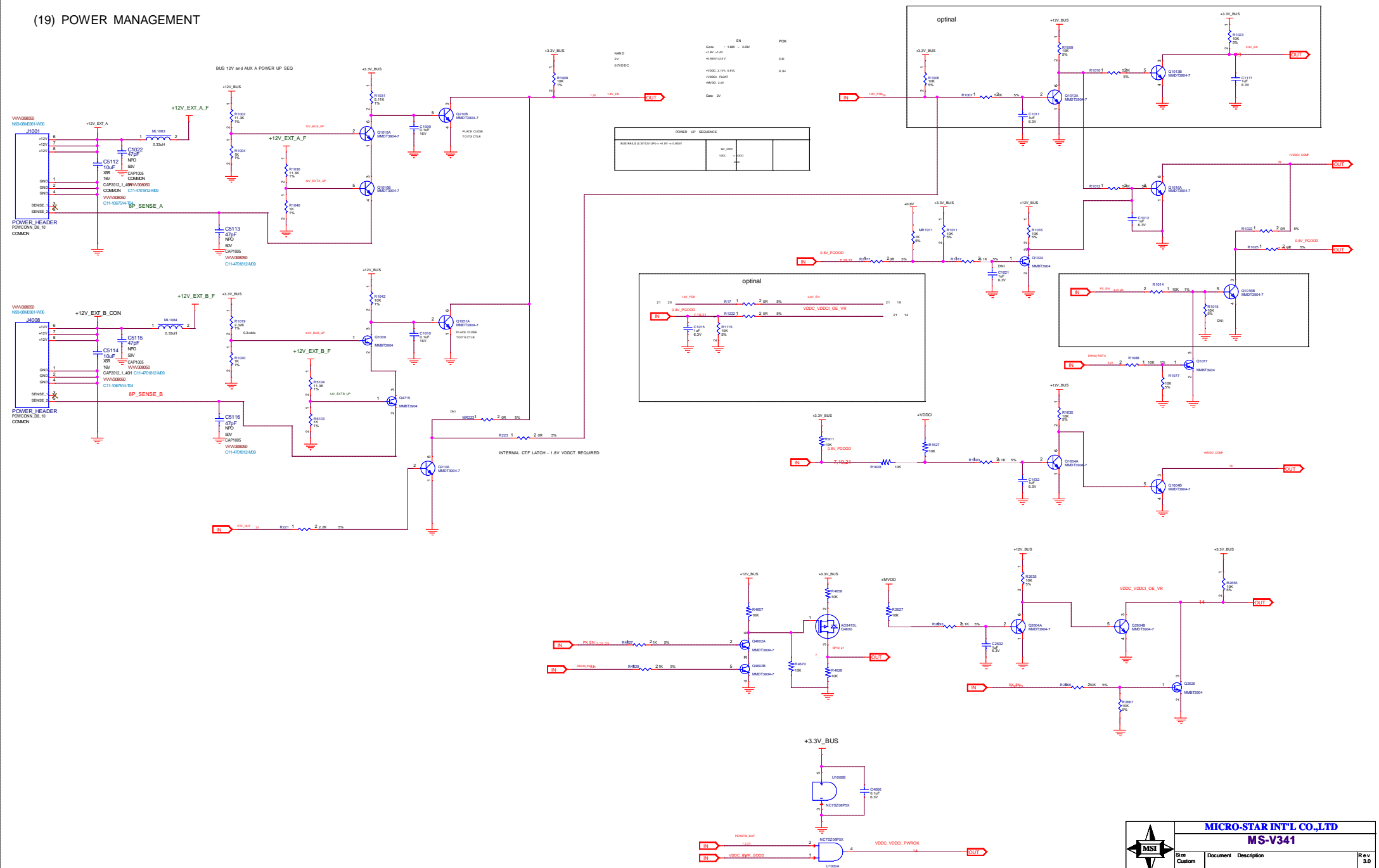
(18) SMALL RAIL REGULATORS , LED\_CONTROLLER\_ENE3574

LDO #1: VIN = 3.0V TO 3.6V MAX VOUT = +1.8V +/- 2% IOUT = 1.3A RMS MAX  
PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING

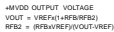
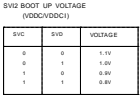
REGULATOR FOR +5V RAILS  
IOUT MAX = 150mA



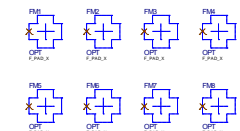
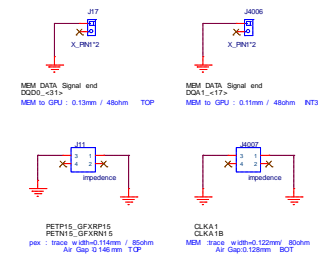
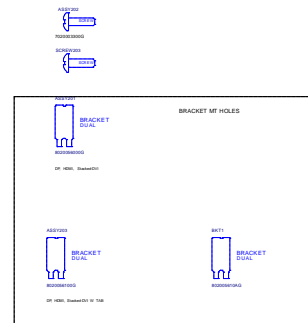
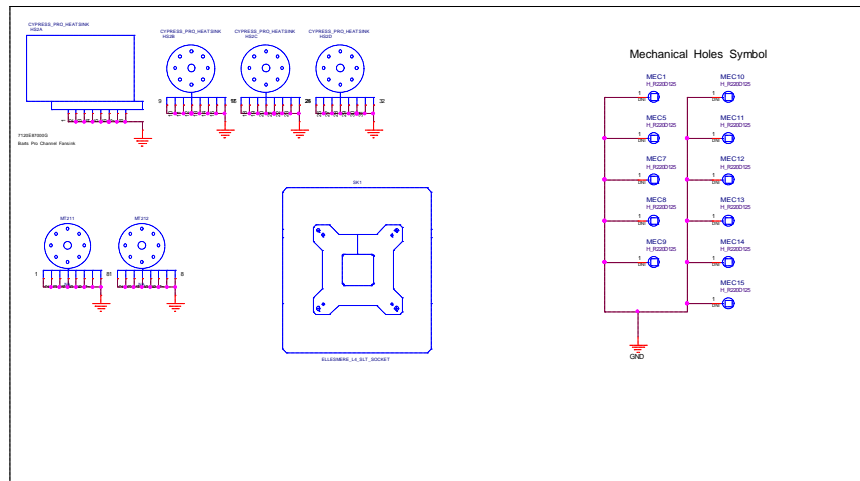
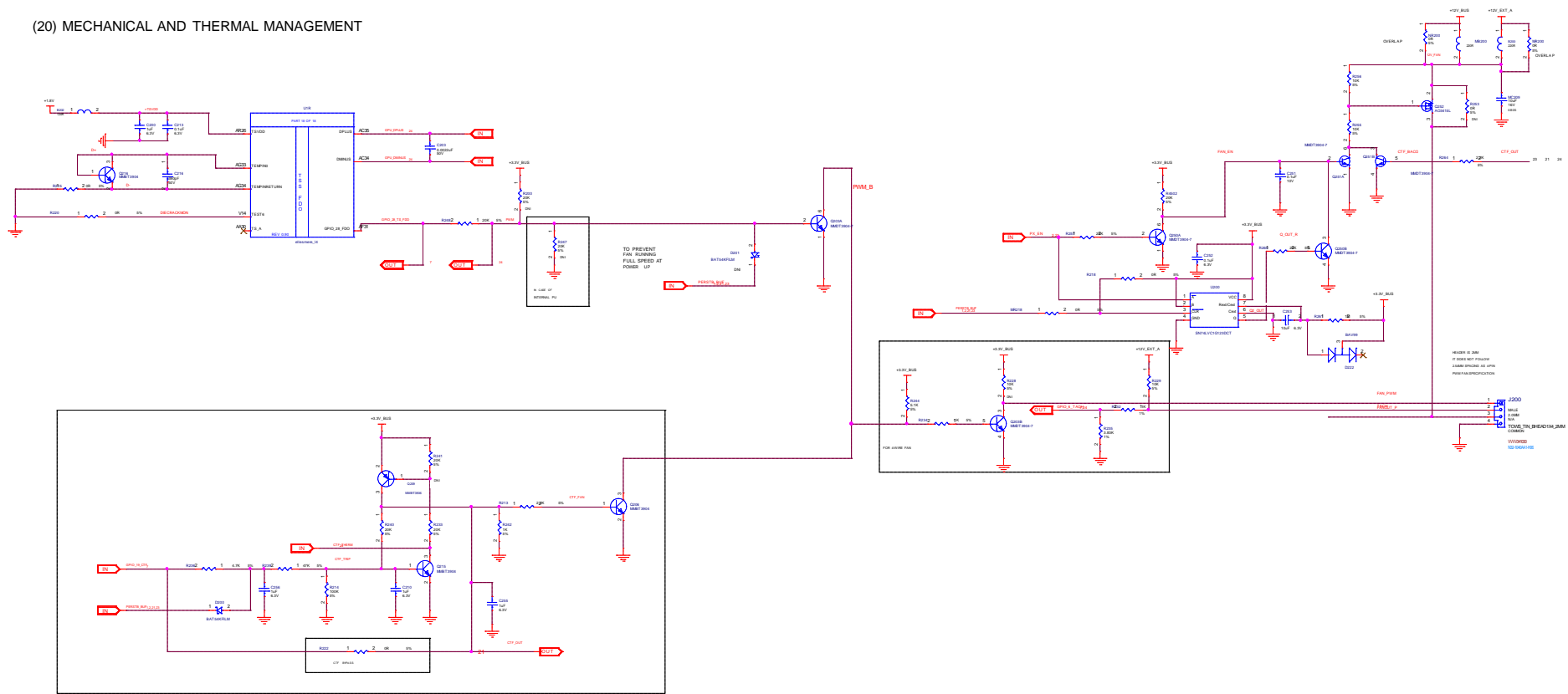
## (19) POWER MANAGEMENT



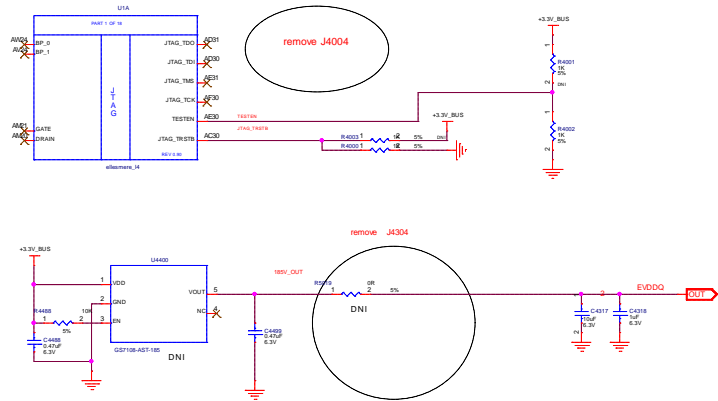




(20) MECHANICAL AND THERMAL MANAGEMENT



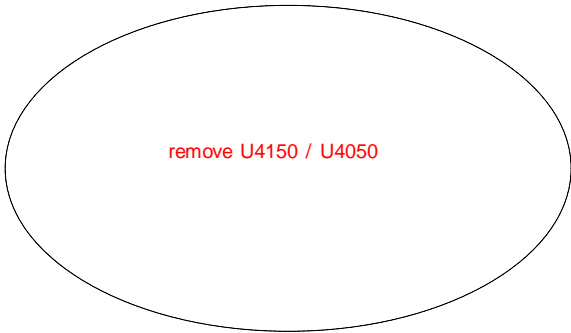
JTAG



E-FUSE CAPABILITY  
DEFAULT = GPIO-CONTROLLED  
(MANUAL OPTION AS BACK-UP)

DIGITAL POTS

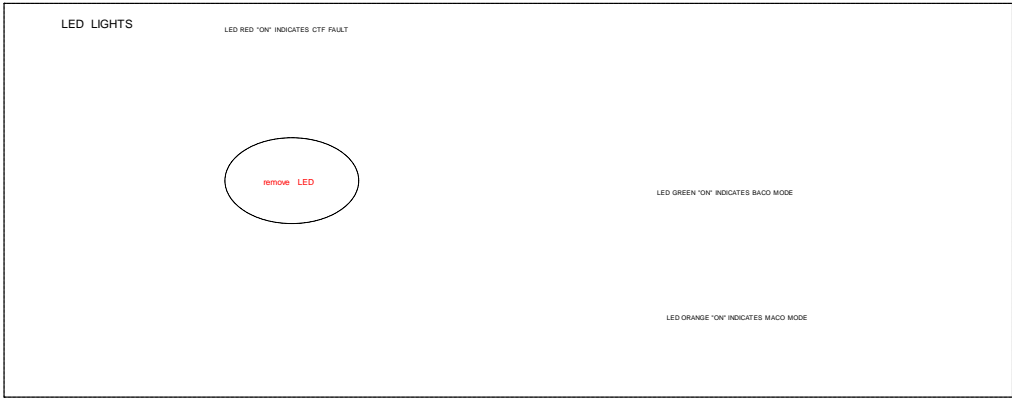
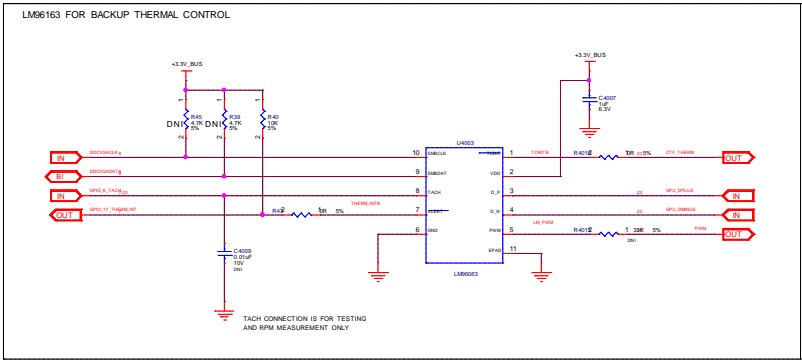
DIGITAL POTS



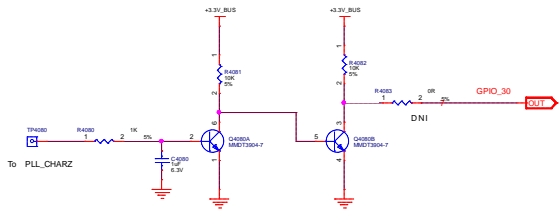
SWITCHES



BYPASS/ENABLE CTF  
MAXIMIZE FAN



VTMM - TEST CONNECTOR FOR VOLTAGE MEASUREMENTS





Page7: remove J2,J3

Page9: enable DVI

Page10: DP change to HDMI

Page15: change dual-N MOS

Page16: change dual-N MOS

Page18: change dual-N MOS

Page20: Add LED circuit

Page21: colay 8pin power connecter

Page24: remove debug circuit

V341-3.0 Ian

#### 14. VDDC change I R35201

15.更改SMD電容改DIP電容

16. 配合高度更換 output S MD 電感及電容

18. 配合高度更換 output S MD 電感及電容  
20. 背板 LED 移除

20. 背板 LED 移除  
27. 增加 7 / 8 相

21. 增加 178 倍

