

PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI  
Tall DVI-I + DP + DP + DP/HDMI + DP

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- 1 page:4-11 修改net name,加<>
  - 2 page:8 增加跨頁符號
  - 3 page:15 修改DVI footprint
  - 4 page:16/17/19 修改DP footprint
  - 5 page:18 修改HDMI footprint
  - 6 page:26/27 修改output chike footprint

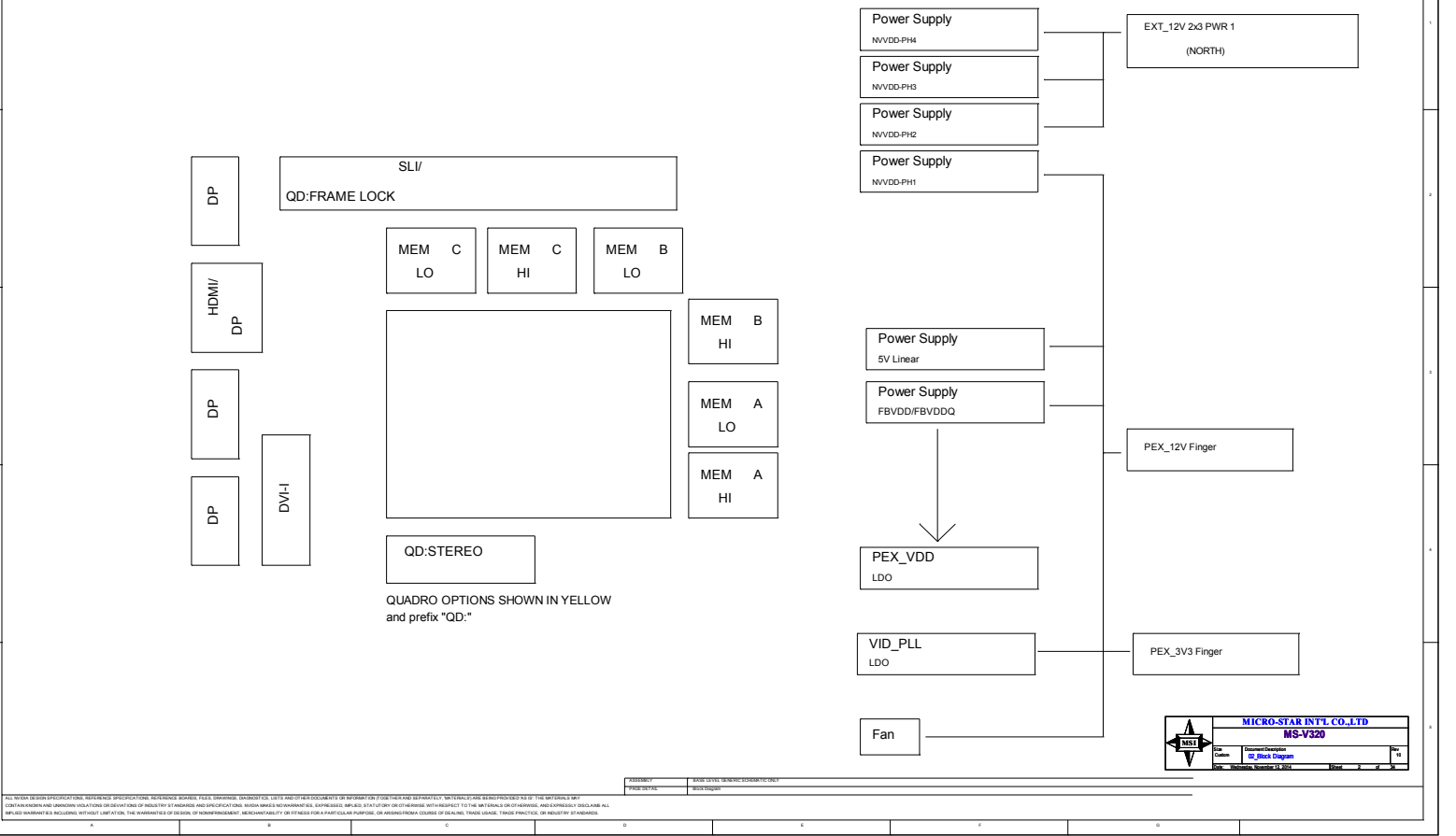


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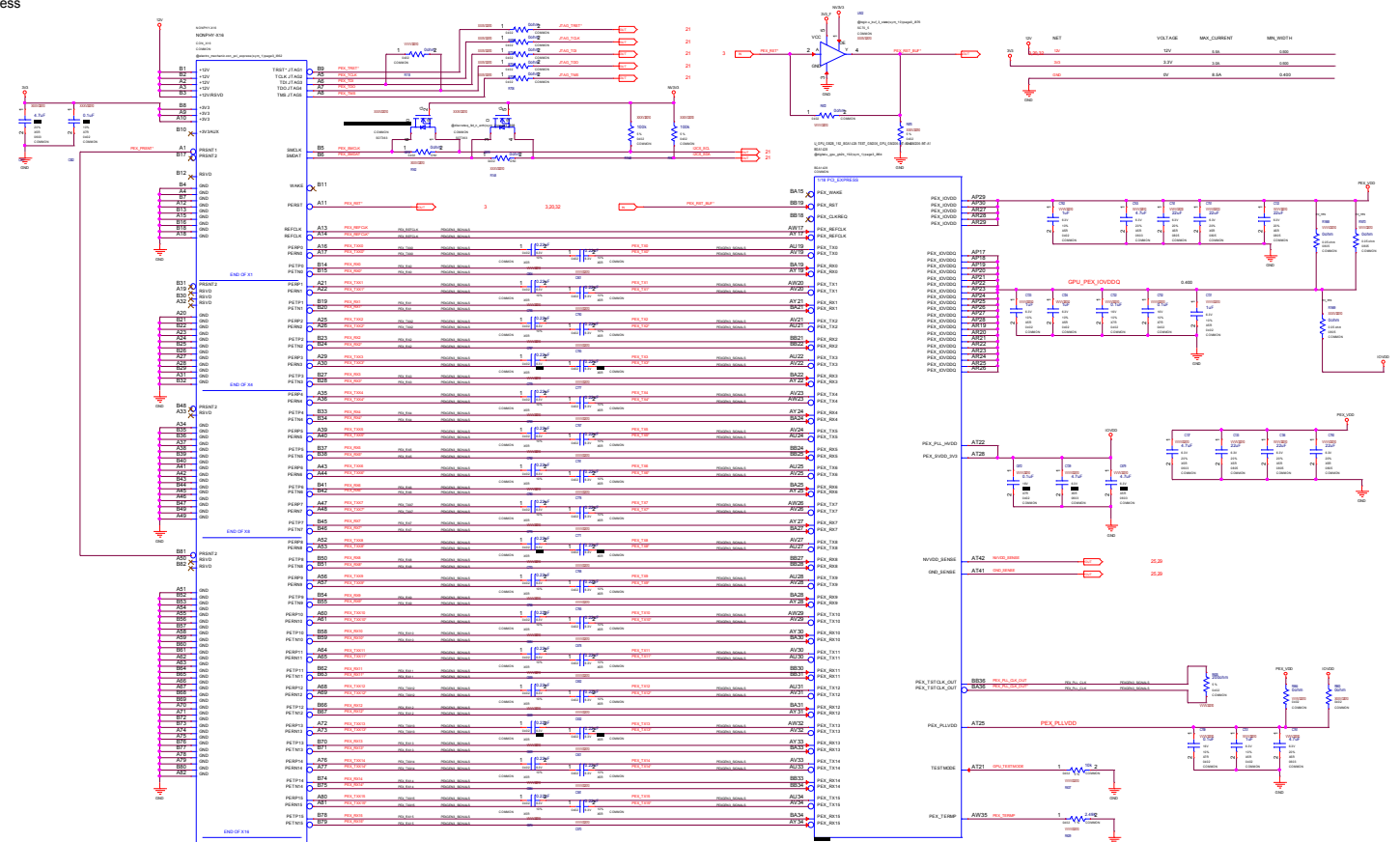
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A B C D E F G H

Block Diagram




PCI Express

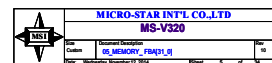


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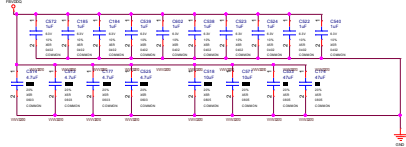
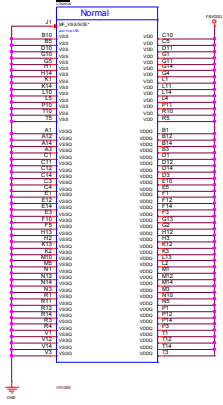
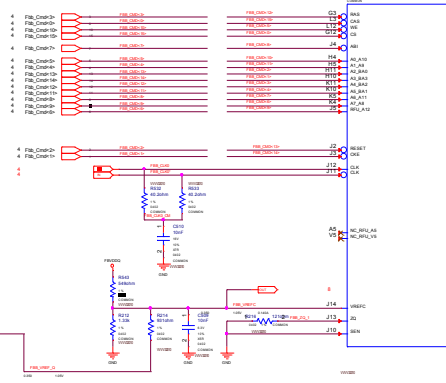
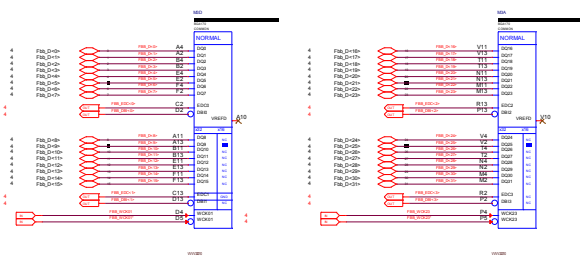
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PAGE DETAIL	PCI Express

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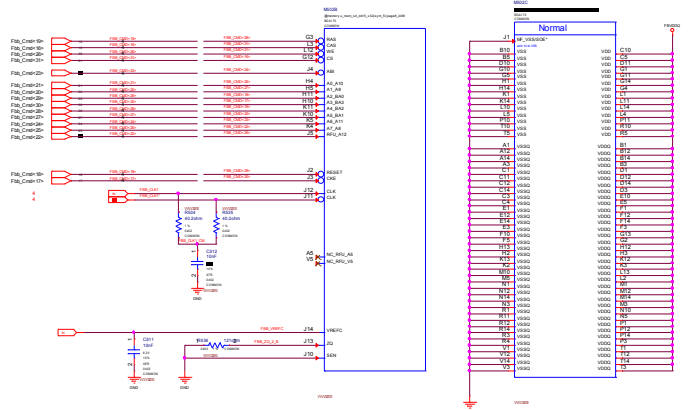
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**MS-V320**

Doc No: **07\_MEMORY\_FBBP\_31**

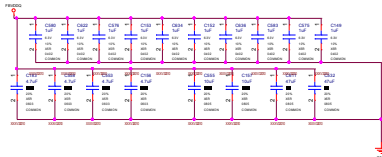
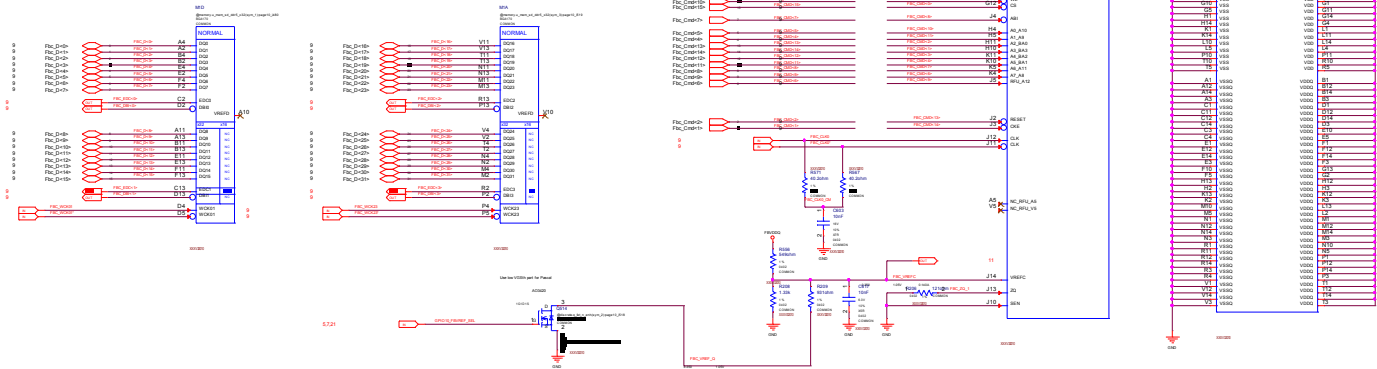
Rev: **1.0**

Date: **2023-10-10**







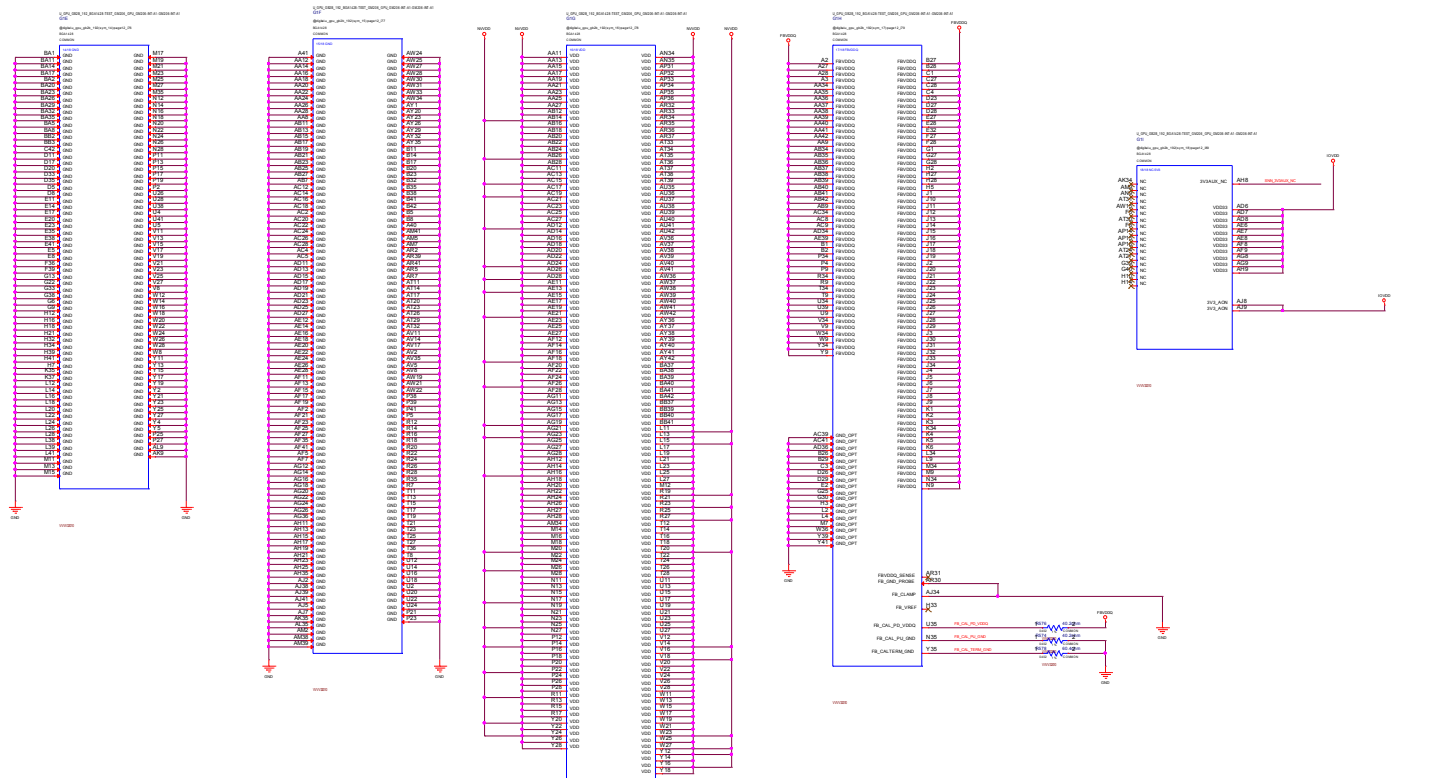


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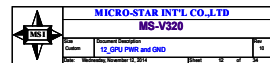




## GPU PWR and GND

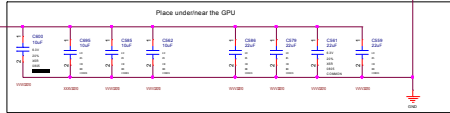
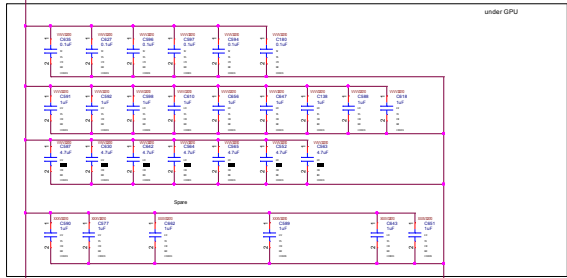


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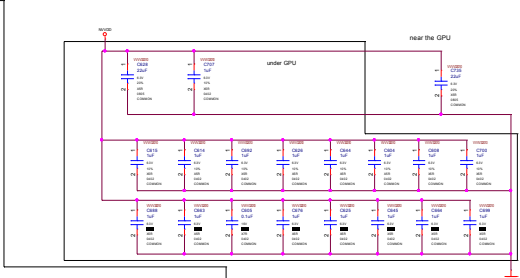
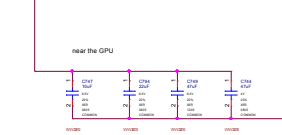
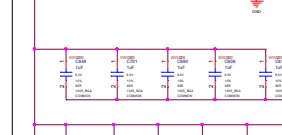
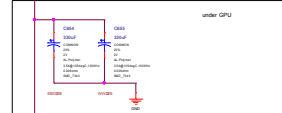


GPU Decoupling

FBVDDQ



NVDD



	Under GPU	Near GPU
NVDD	90uF + 1x 330uF	80uF
SVDD	33uF	22uF
Combined (Microel)	122uF + 1x 330uF	110uF

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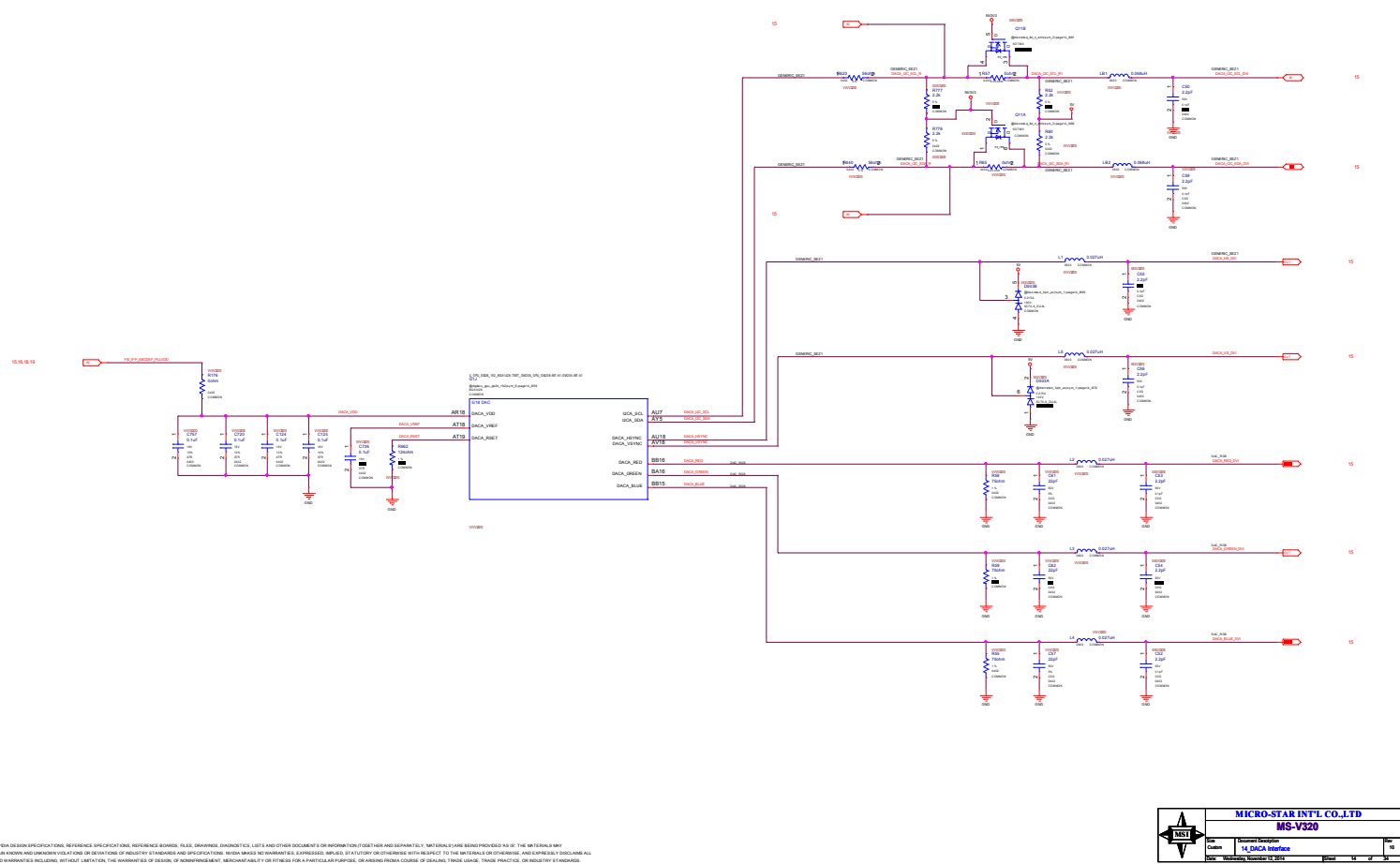
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GPU Decoupling



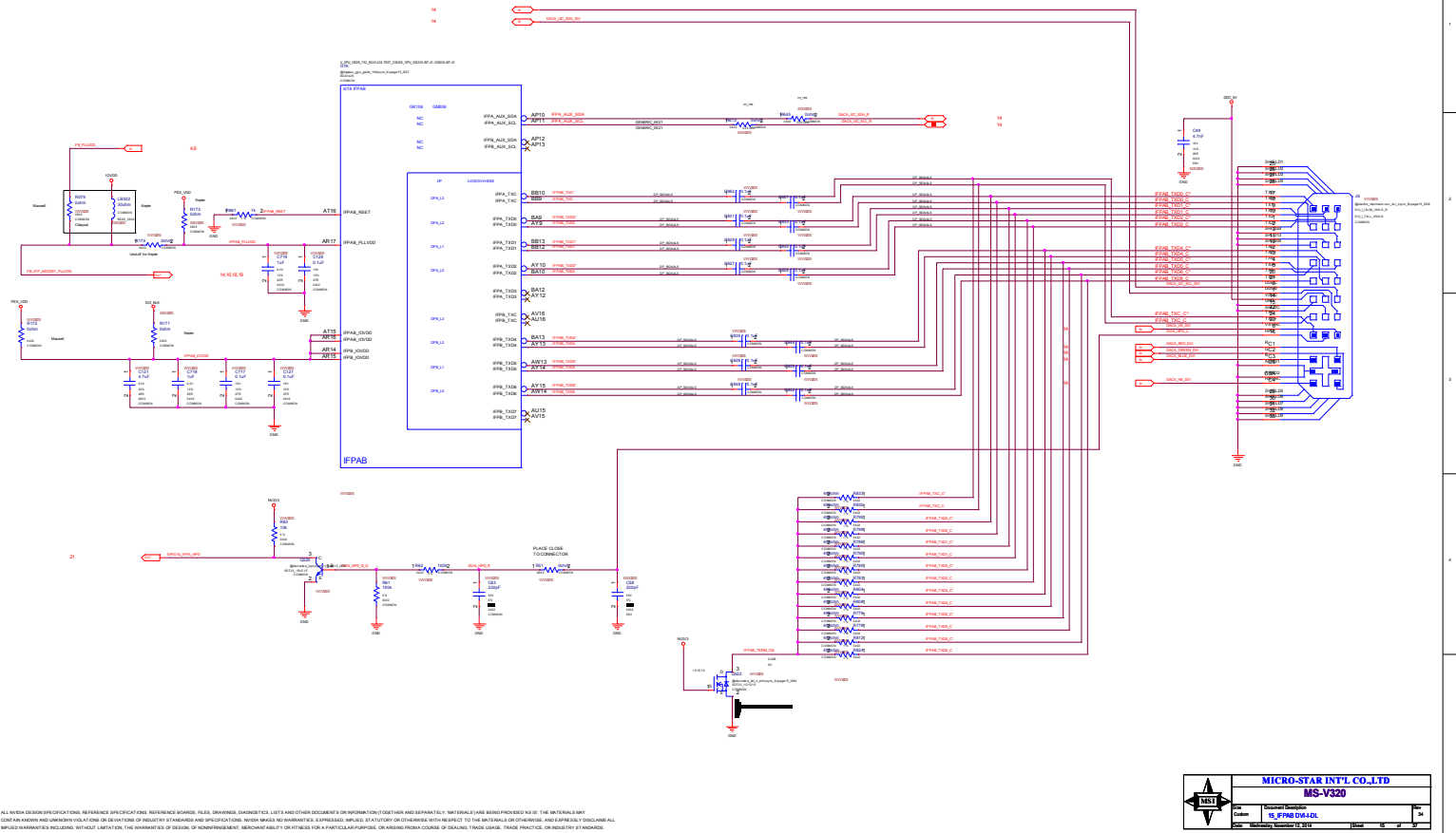
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Doc. Version	1.0

## DACA Interface



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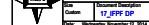
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NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
5	5VCCA_VREF	1.0A	0.300
5	5VCCA_CPL_PD_VREF	1.0A	0.300
5	5VCCA_CPL_PD_VREF	1.0A	0.300



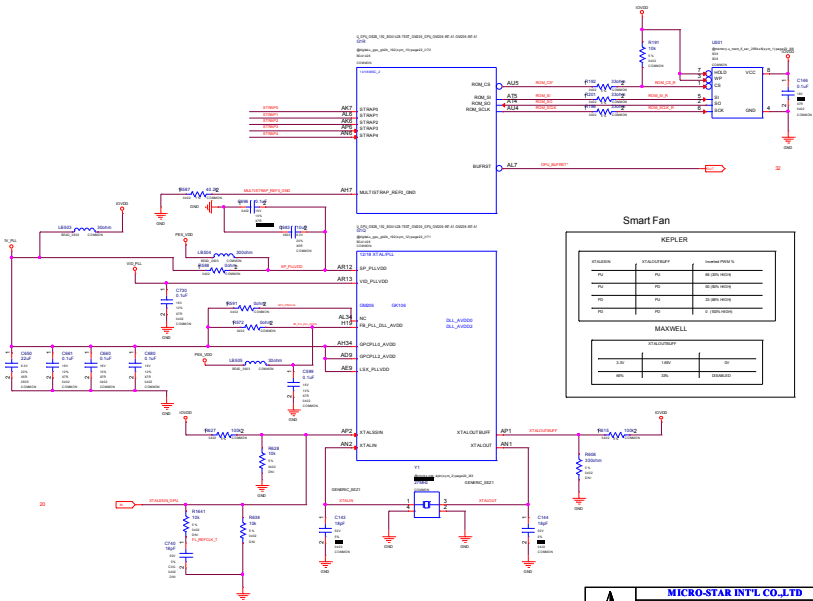
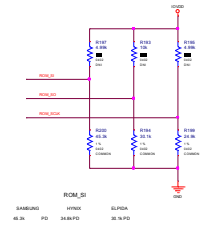
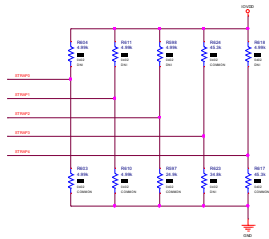


MISC2: ROM, XTAL, Straps

KEPLER		MAXWELL	
STRAP0	USER_BIT [3:0]'		
STRAP1	3IGD_PRIOCFG_LUT_ADDR'		
STRAP2	POJ_DEVID [3:0]'		
STRAP3	SOR1_EXPOSED [3:0]'		
STRAP4	DP_PLL_VCO_SELV'		
	POX_MAX_SPEED'		
	POX_SPD_CHANCE_GENV'		
ROM_SI	RAMCFG[0]'	RAMCFG[0]'	
	RAMCFG[1]'	RAMCFG[1]'	
	RAMCFG[2]'	RAMCFG[2]'	
	RAMCFG[3]'	RAMCFG[3]'	
	VGA_DEVICE'	VGA_DEVICE'	
ROM_SO	SMB_ALT_ADDR'	SMB_ALT_ADDR'	
	FB[0]_APERTURE_SIZE'	POE_CFG'	
	FB[1]_APERTURE_SIZE'	DEVID_SEL'	
ROM_SCLK	POX_PLL_PL_TERMINO2'	SOR2_EXPOSED'	
	POJ_DEVID_EXT[0]'	SOR1_EXPOSED'	
	SUB_VENDOR'	SOR2_EXPOSED'	
	POJ_DEVID_EXT[4]'	SOR0_EXPOSED'	

MULTI STRAP_0401_0402	
BOOT_PRESERVE	NO
BOOT_PRESERVE	NO
BOOT_PRESERVE	NO

STRAP0	
0x00	0x00
0x01	0x01
0x02	0x02

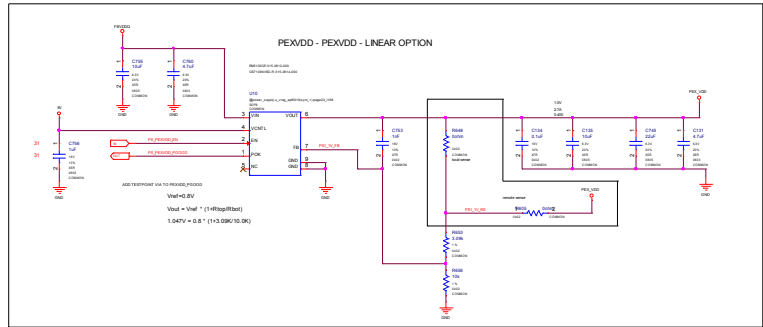
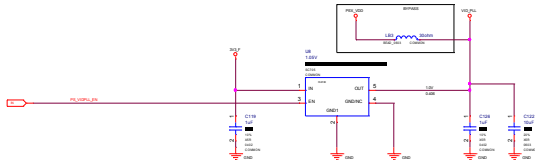
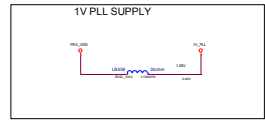


Smart Fan	
KEPLER	MAXWELL
0x00	0x00
0x01	0x01
0x02	0x02



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**MS-V320**  
Form: **MS-V320**  
Date: **2010.10.10**

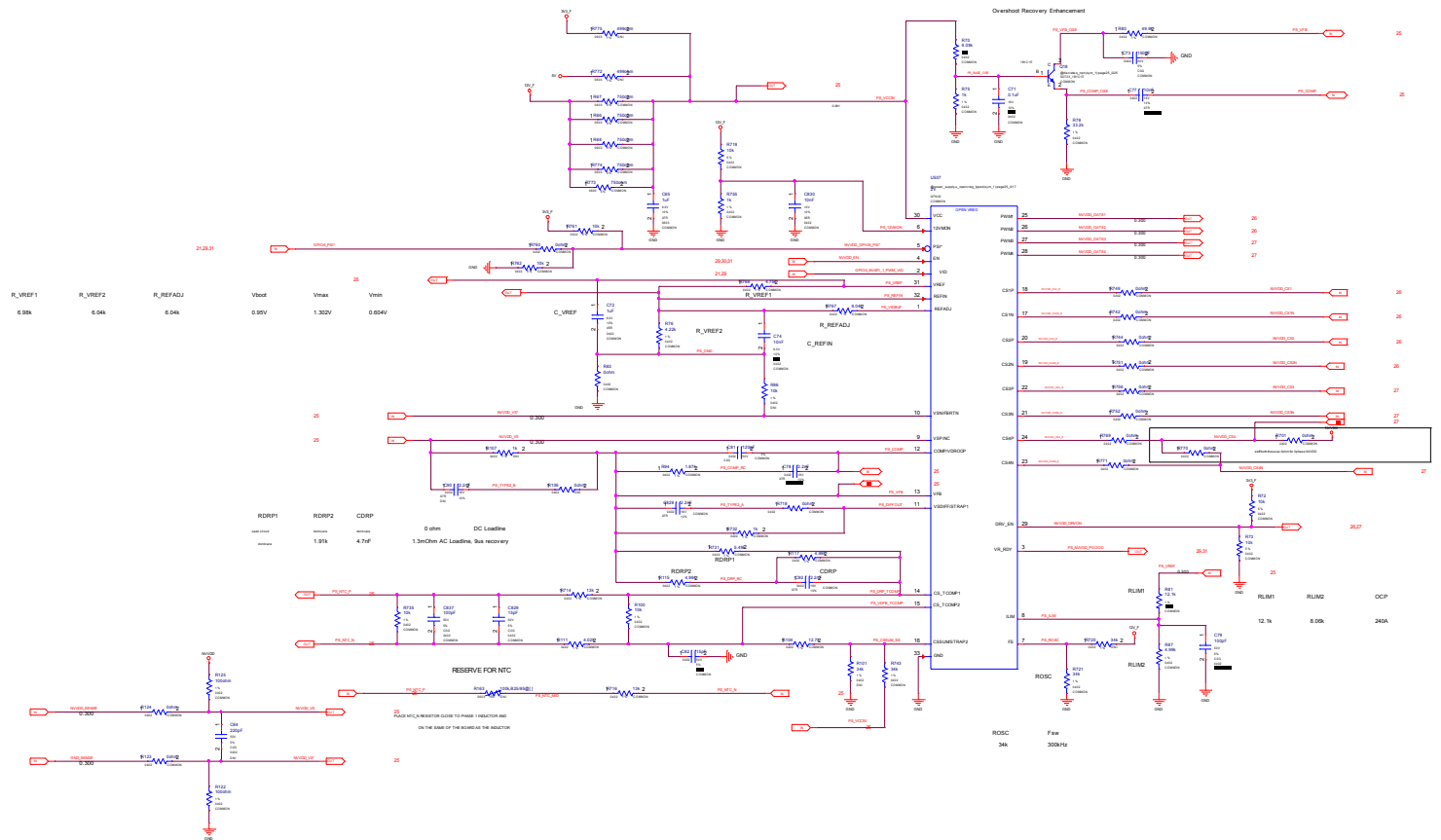
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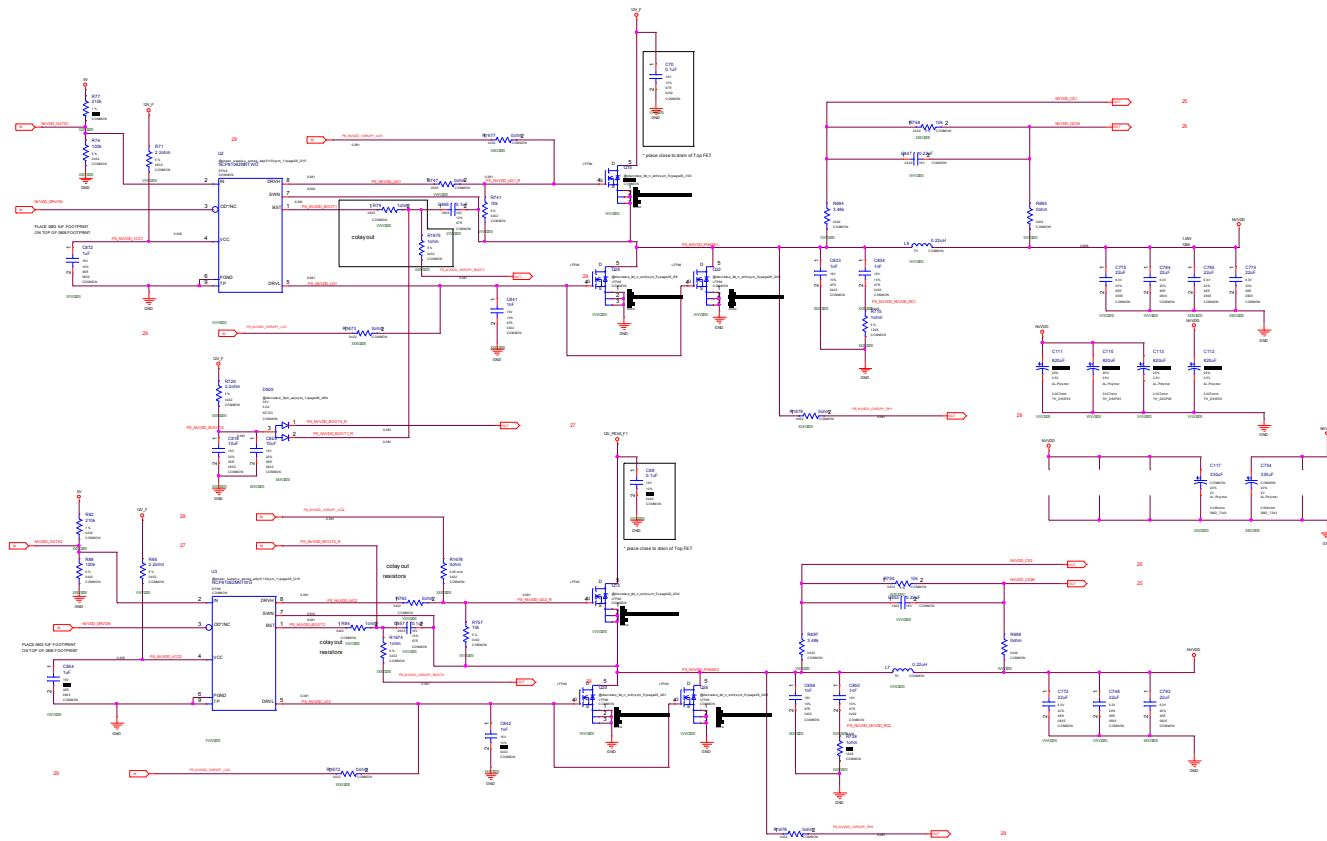


## PS: NVVDD Controller



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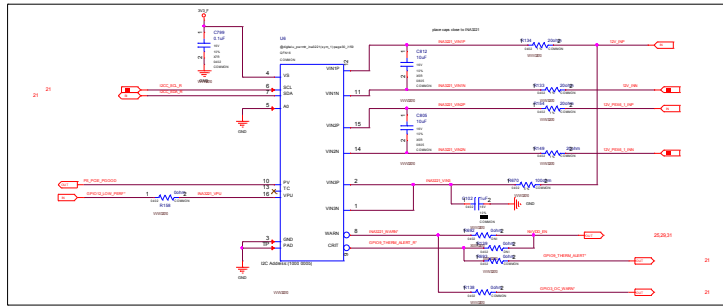


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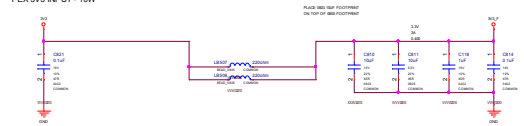




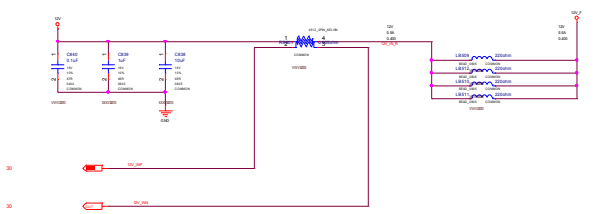
PS: Inputs, Filtering, and Monitoring



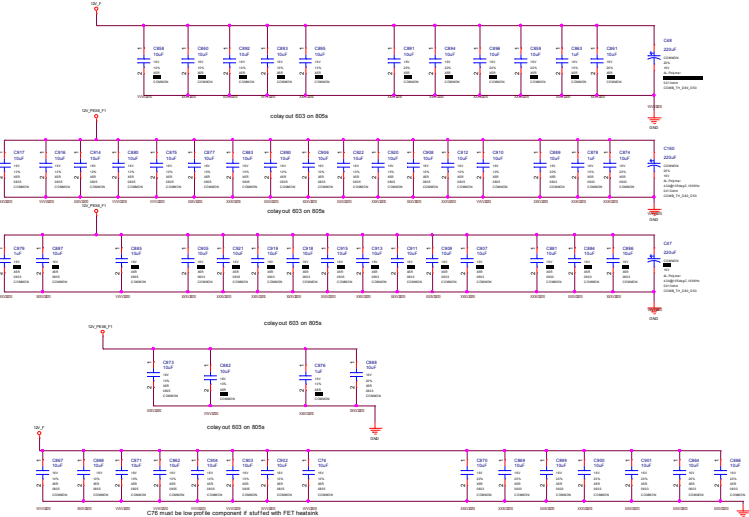
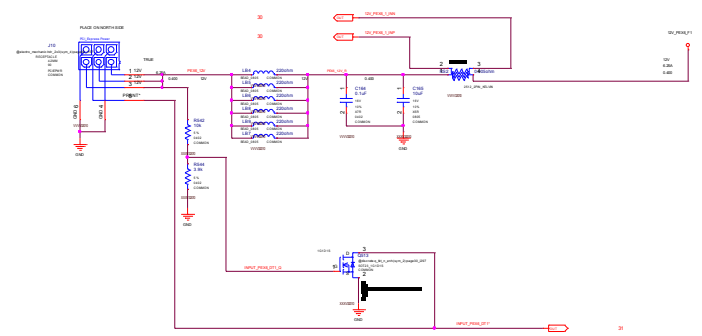
PEX\_3V3 INPUT - 10W



PEX\_12V INPUT - 60W

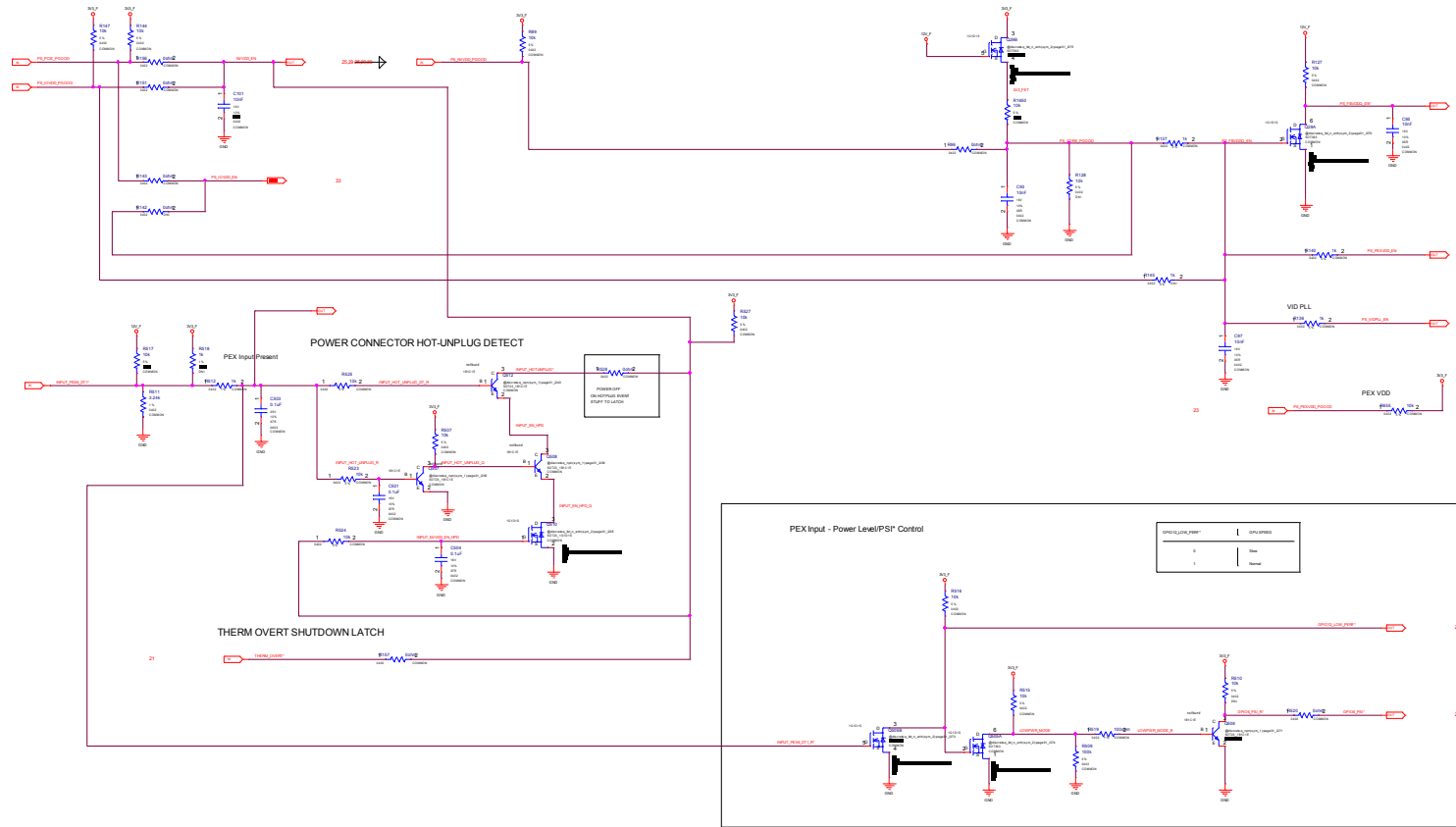


PEX\_12V INPUT - 75W

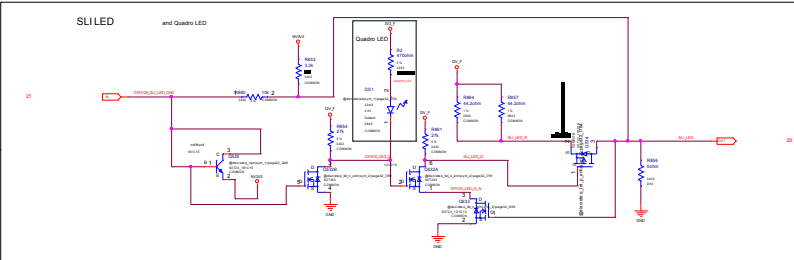
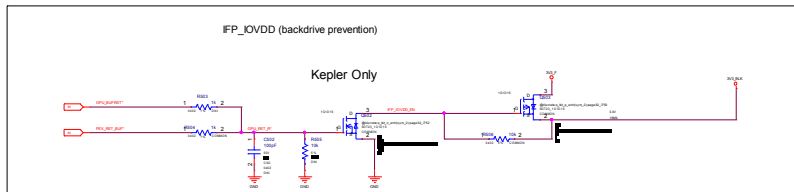
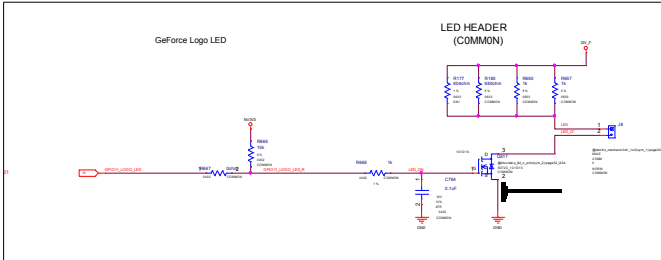


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# PS: Sequence and Shutdown

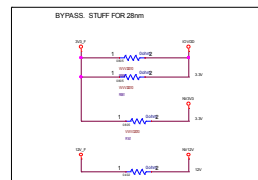
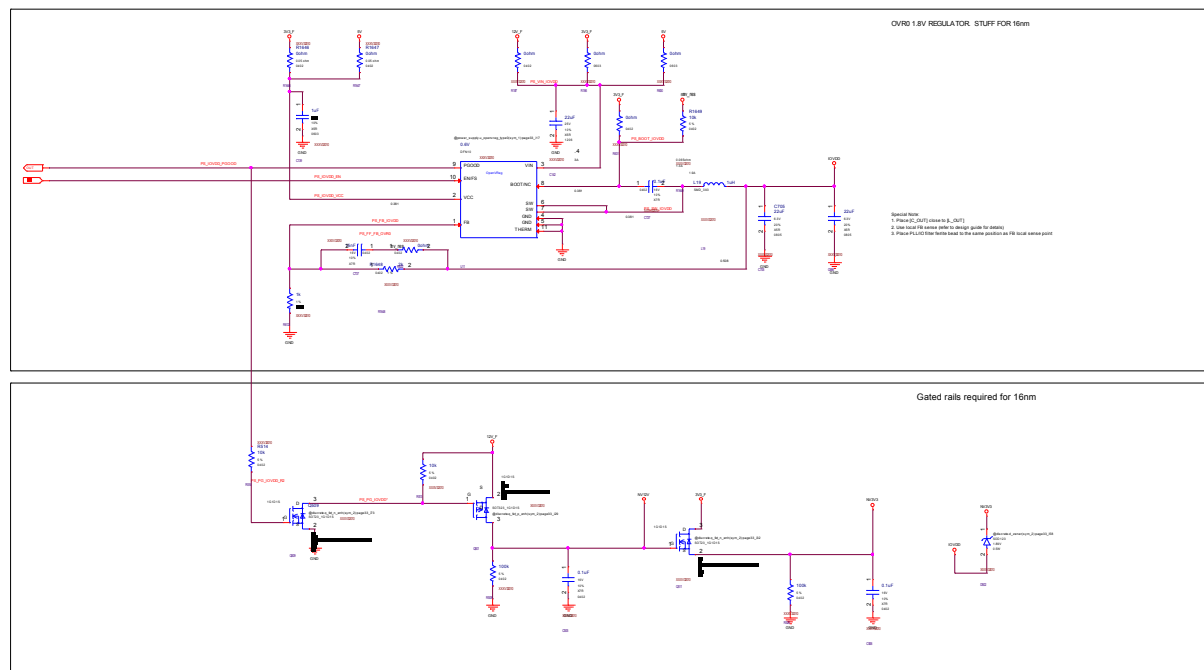


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