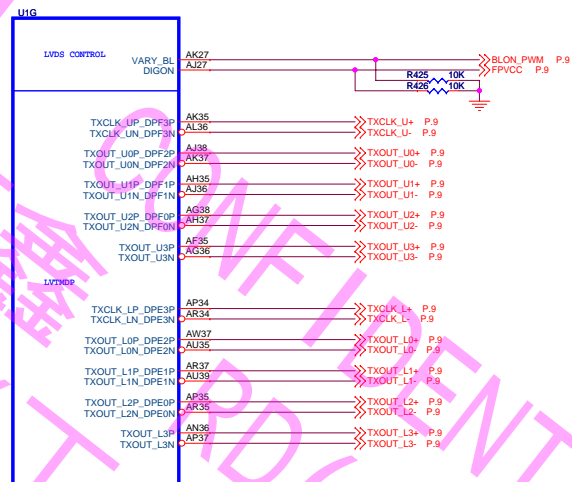


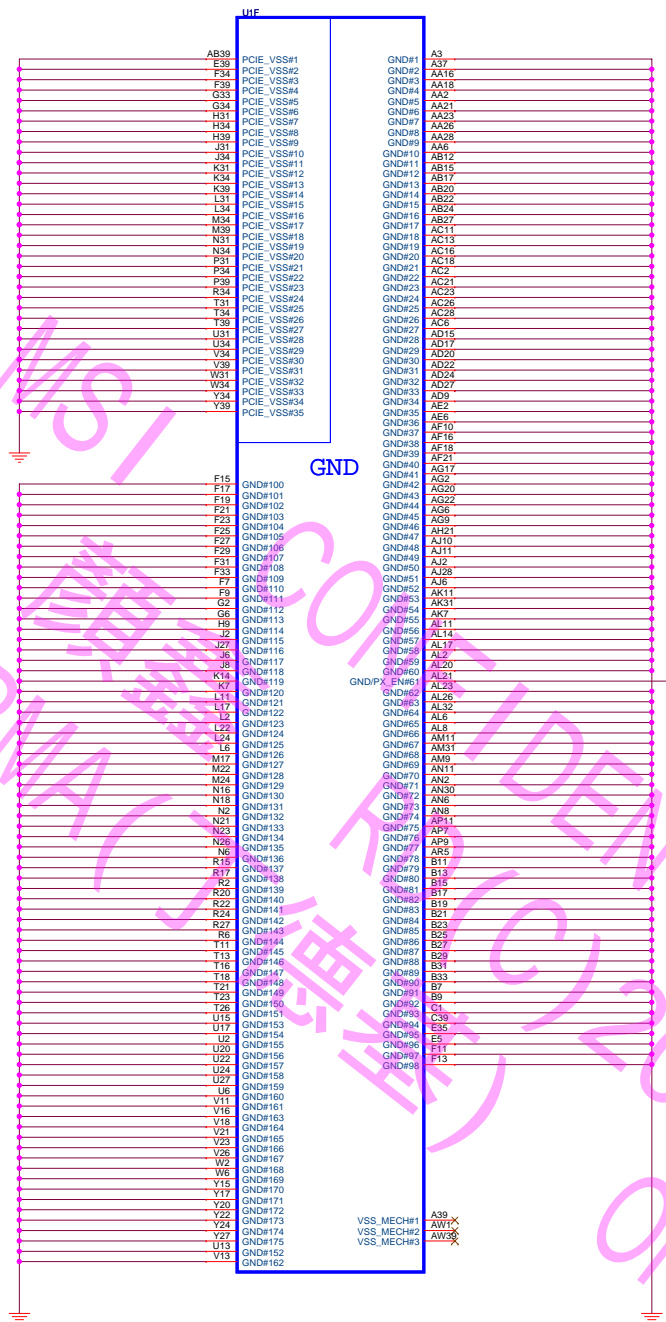


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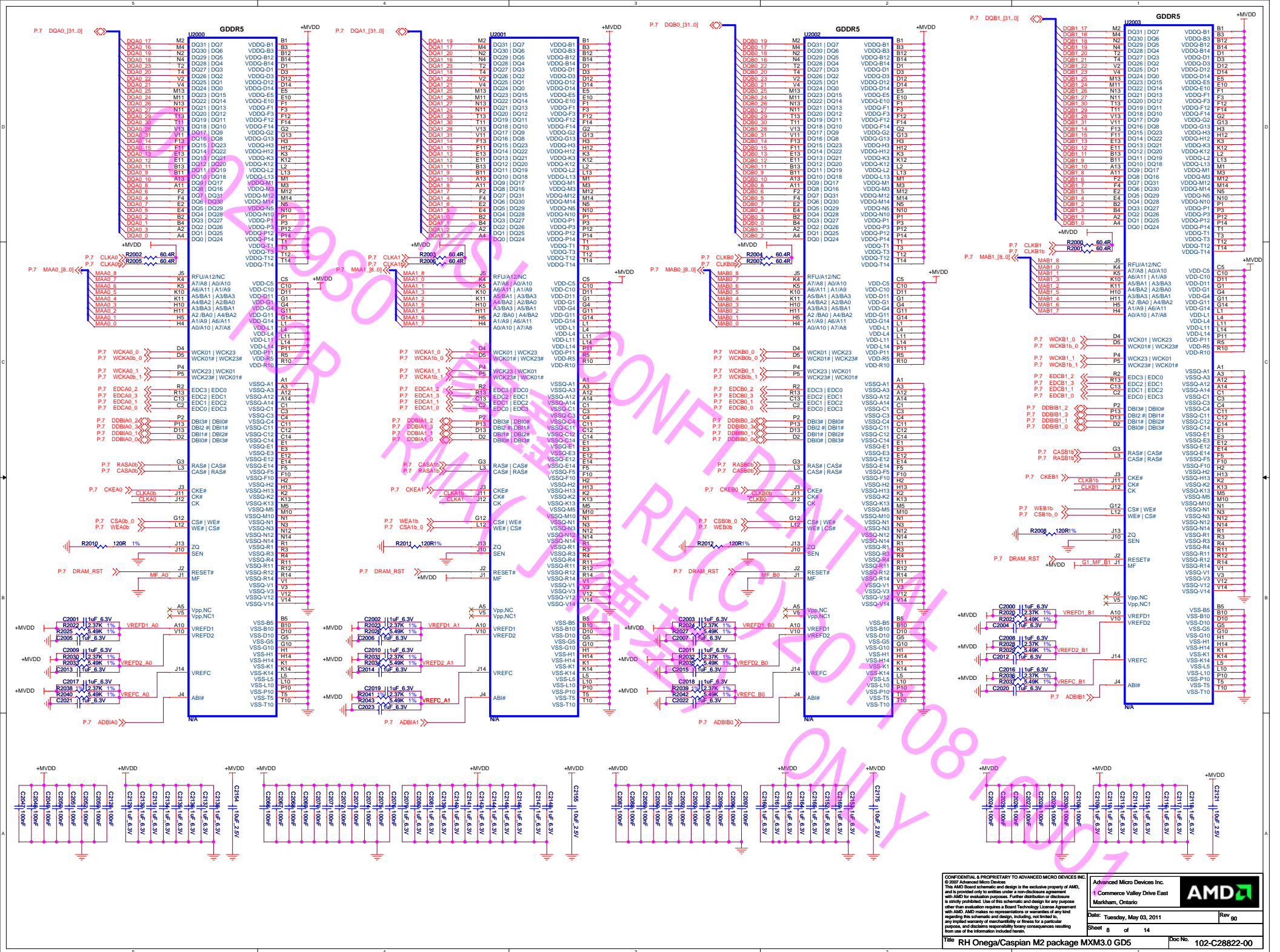


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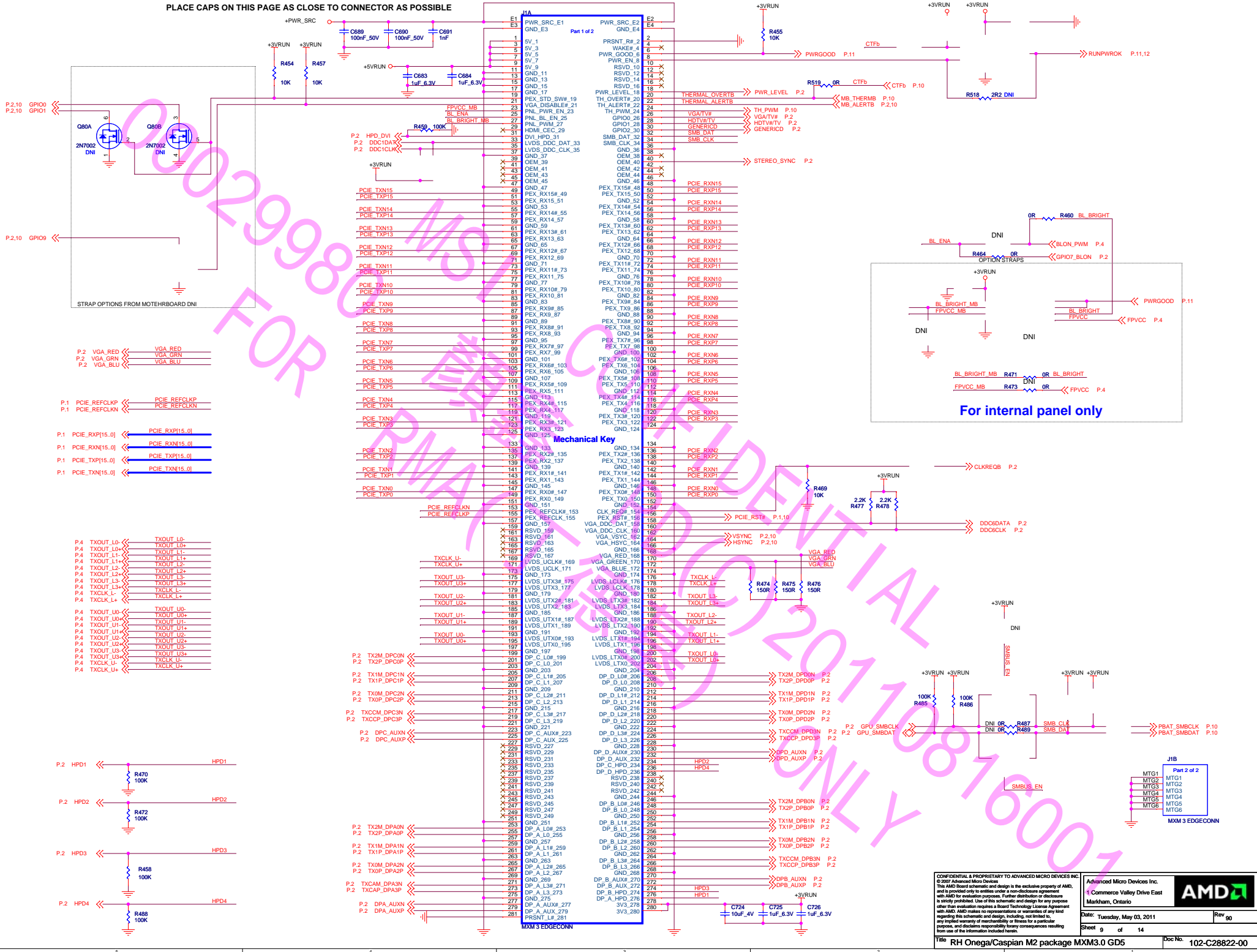




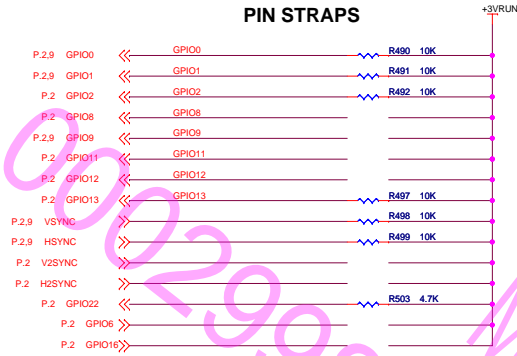




PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE



## PIN STRAPS



## CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 10K RESISTOR  
X = DESIGN DEPENDANT  
NA = NOT APPLICABLE

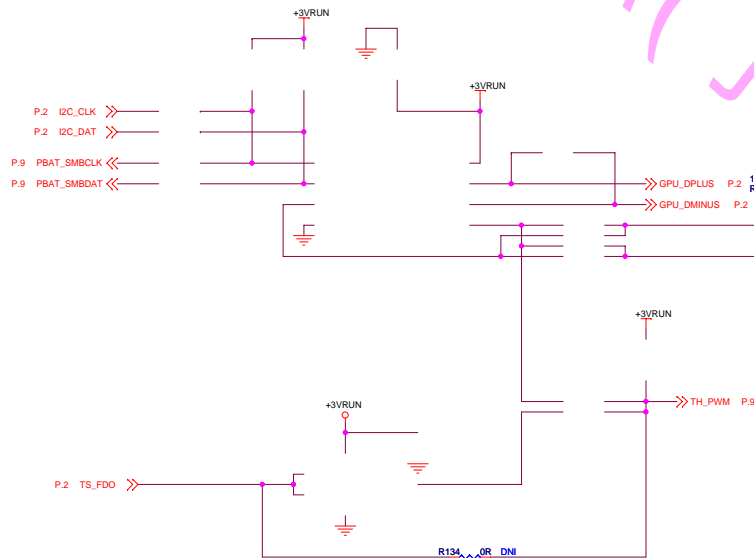
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIe FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIe GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL_ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERIC		0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSYNC	Audio function present	1
MEMORY_CINFIG	[GPIO6,GPIO16]		
HYNIX	[0:1]		
SAMSUNG	[1:0]		

## AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

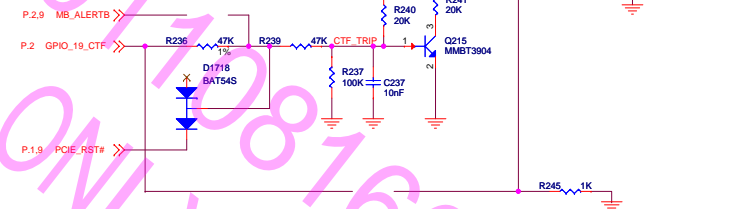
H2SYNC	GENERIC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO_28_TDO	GPIO21_BB_EN

## THERMAL SENSOR AND PWM OUTPUT



## CRITICAL TEMPERATURE FAULT

For one time CTF use R239 47k.  
For resetable CTF use R239 2k.



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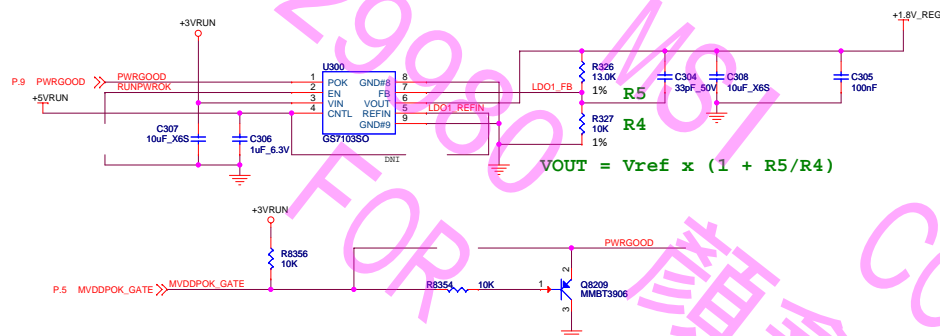
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Markham, Ontario



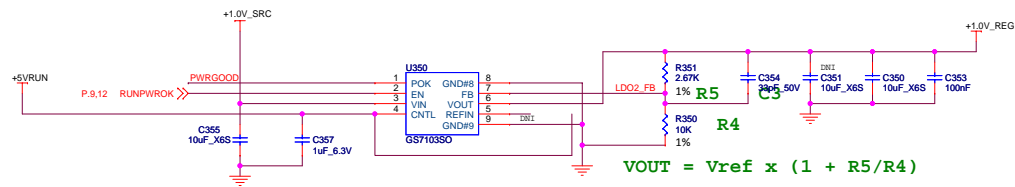
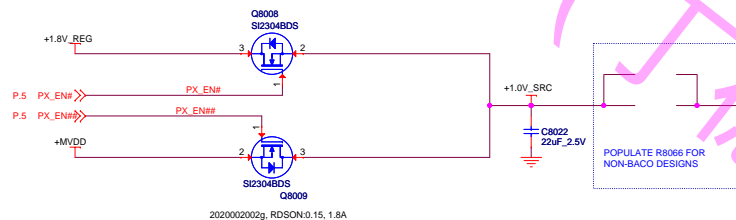
Date: Tuesday, May 03, 2011  
Rev: 90  
Sheet: 10 of 14

Title: RH Onega/Caspin M2 package MXM3.0 GD5 Doc No: 102-C28822-00

**LDO #1:** Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 0.8A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling



**LDO #2:** Vin = +1.32V to 1.84VMAX Vout = +1.0V +/- 2% Iout = 1.7A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling

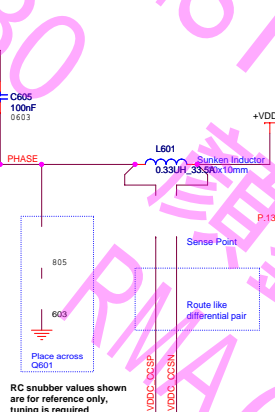
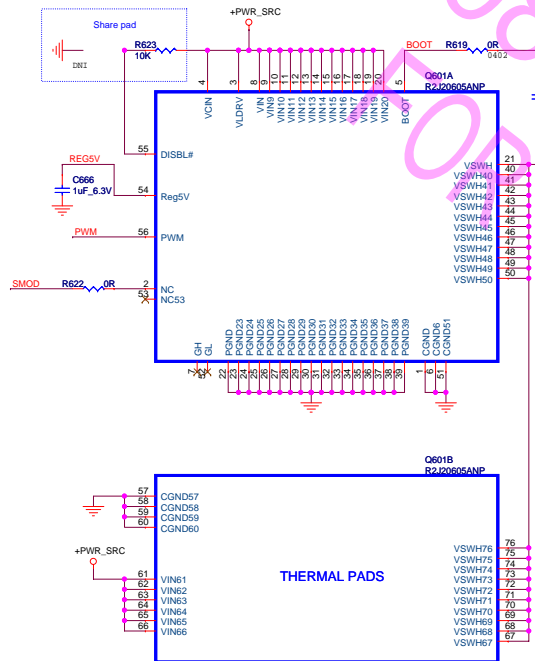
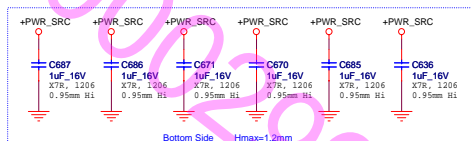
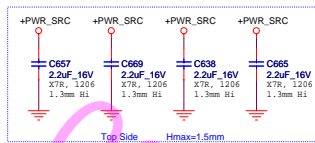


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Rev: 90  
Sheet 11 of 14  
Title: RH Omega/Caspio M2 package MXM3.0 GD5  
Doc No: 102-C28822-00

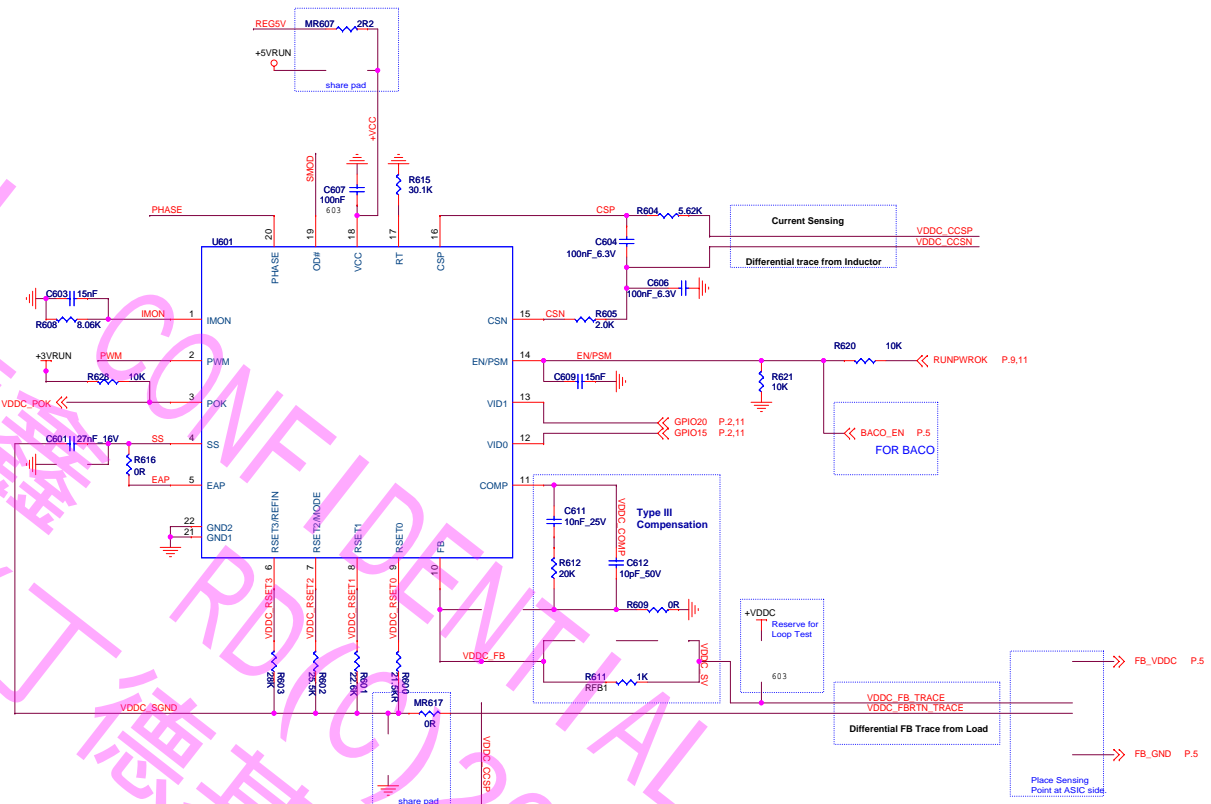
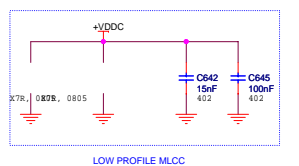
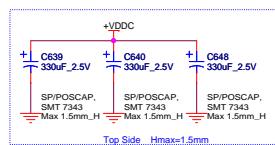


# INPUT CAP

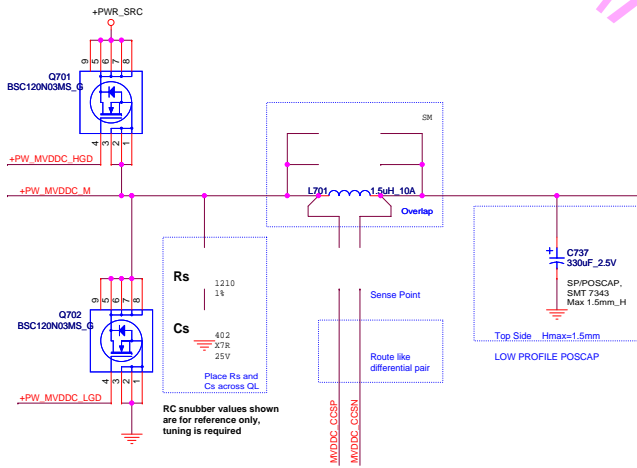
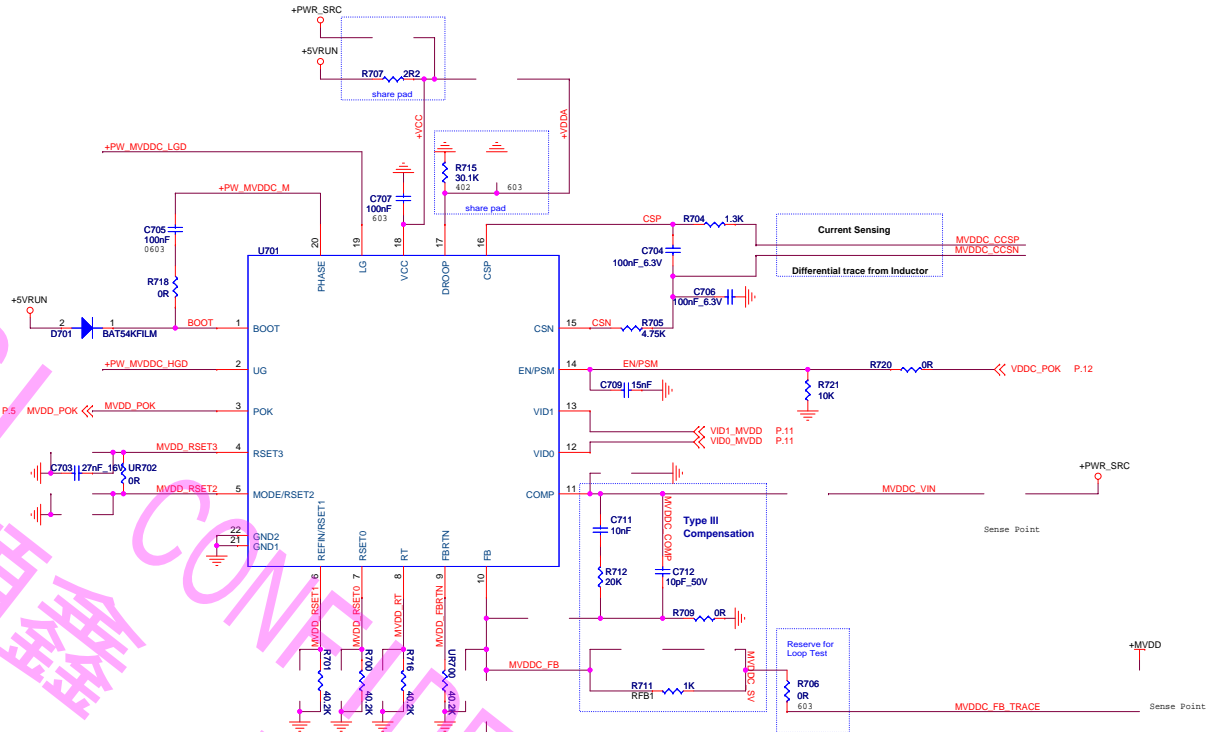
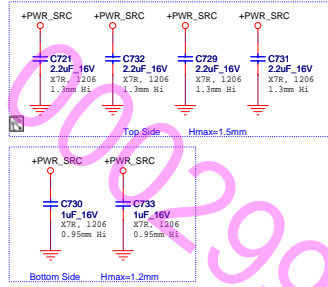


Pin	R2J2062NP	R2J2065NP
1	VLDIV	NC
2	VIN	NC
3	NC	LD0BL4
4	NC	TD0N1

# OUTPUT CAP



# INPUT CAP





## RH Onega/Caspian M2 package MXM3.0 GD5

102-C28822-00

**Tuesday, May 03, 2011**

**NOTE:** This schematic represents the PCB, it does not represent any specific SKU.  
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.  
Please contact AMD representative to obtain latest BOM closest to the application desired.

90

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/28/10	Create new SCH

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