

PG210 B00

GP107 128b GDDR5, 75W , PCB 5.7"  
DVI-D\_DL (DP + DP) + HDMI (DP) + DP

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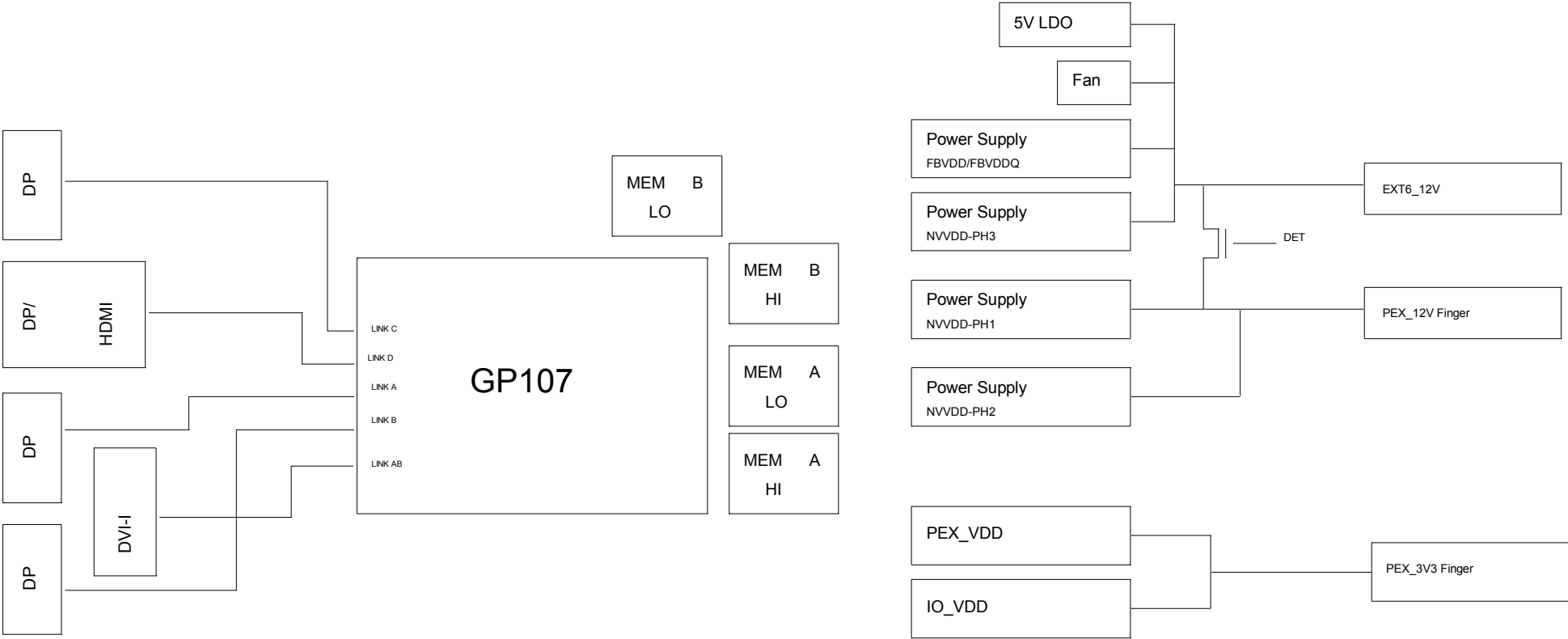
2701 SAN TOMAS EXPRESSWAY

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NV_PN	600-1G210-BASE-SCH		
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Block Diagram



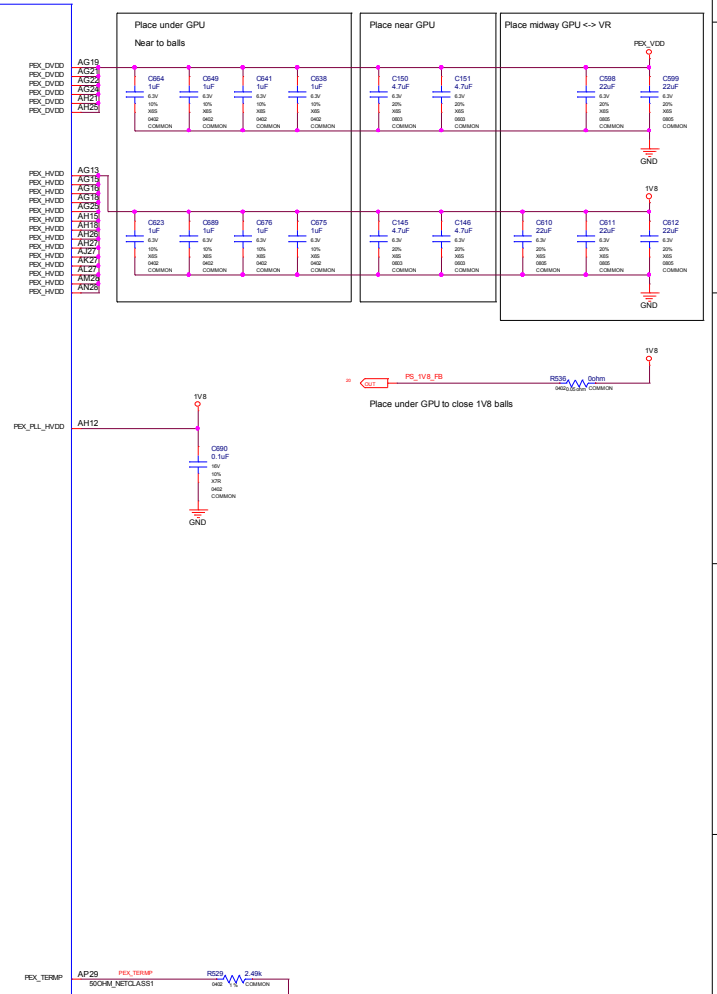
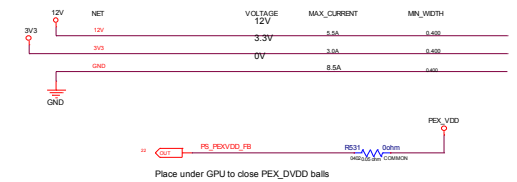
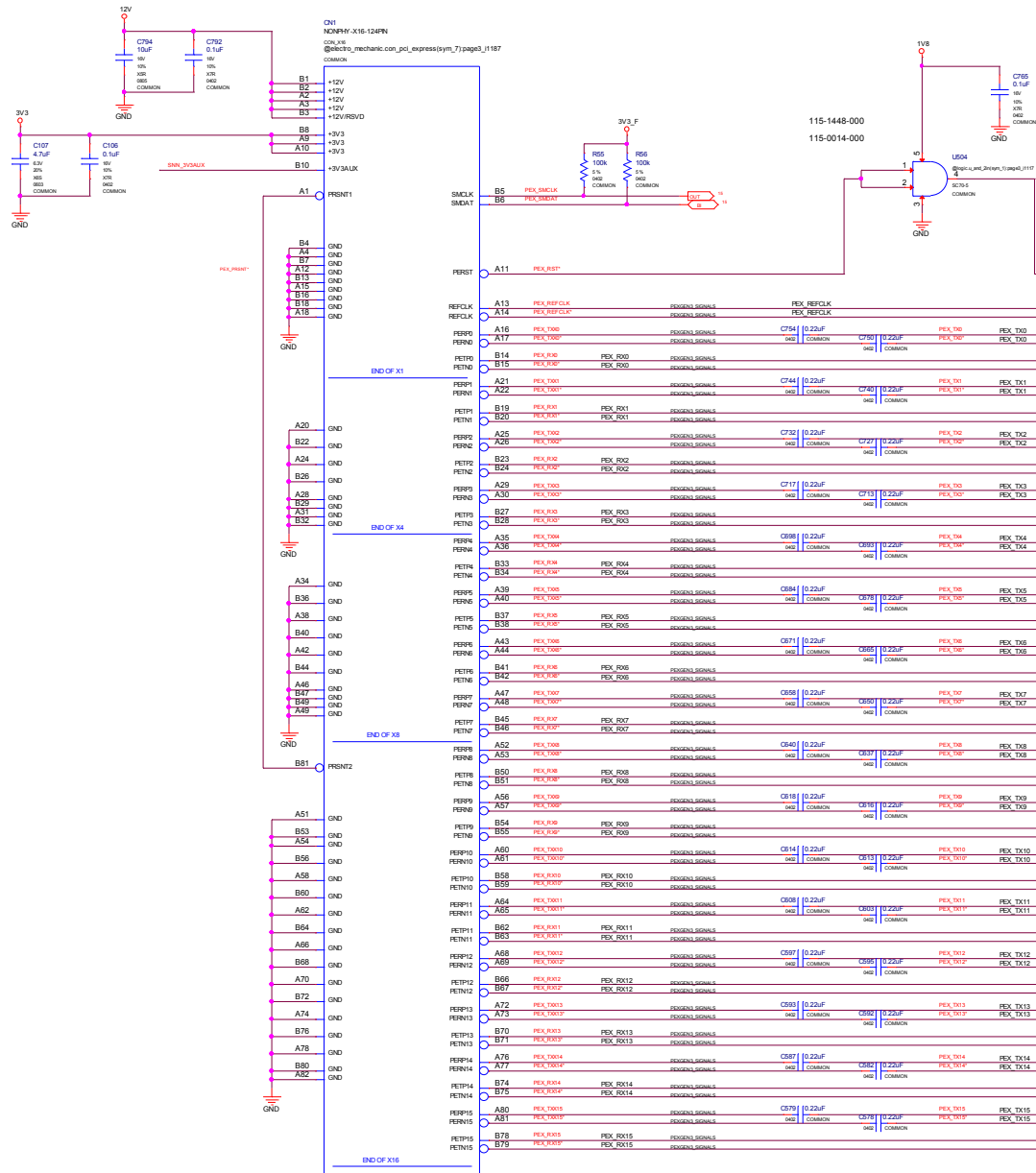
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PCI Express



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PAGE DETAIL	PCI Express

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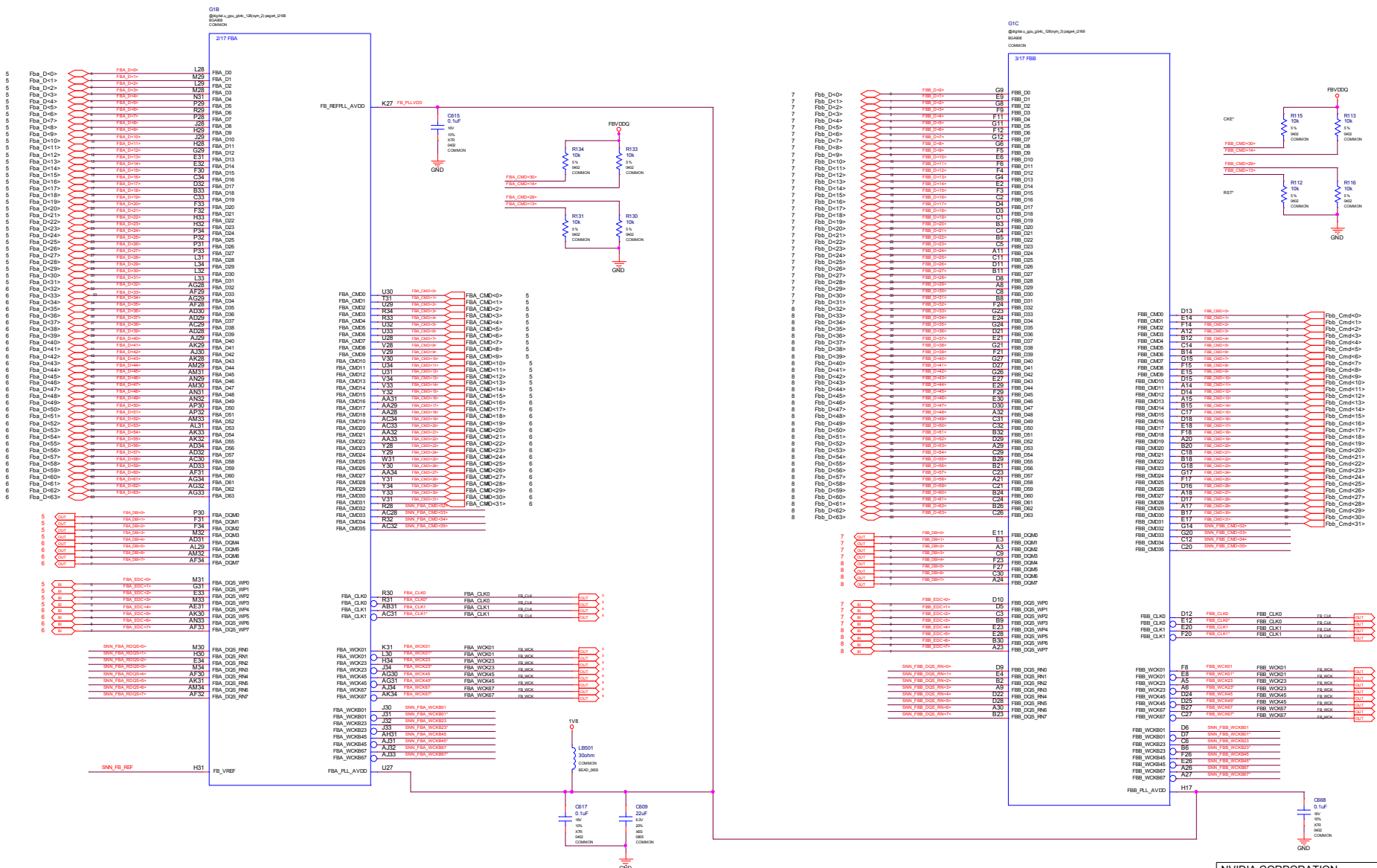


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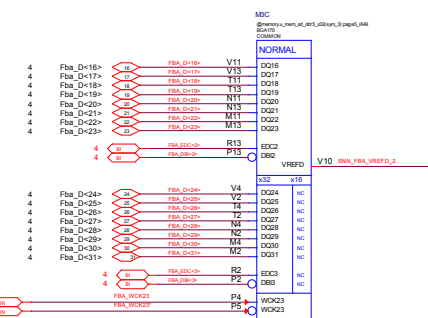
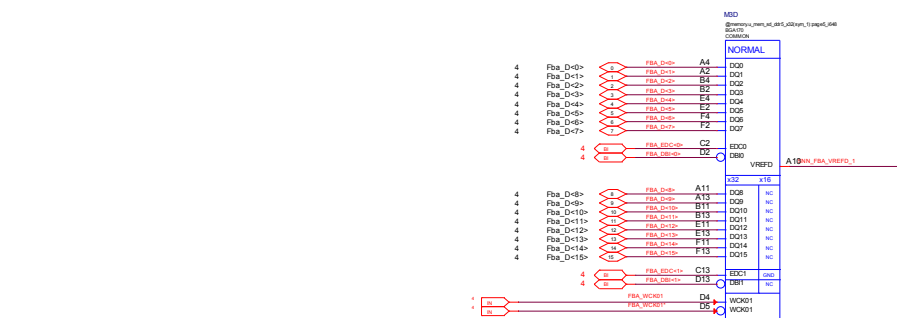
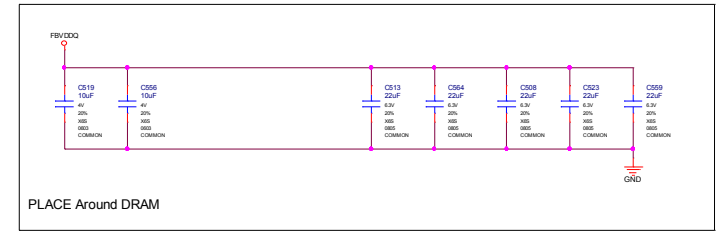
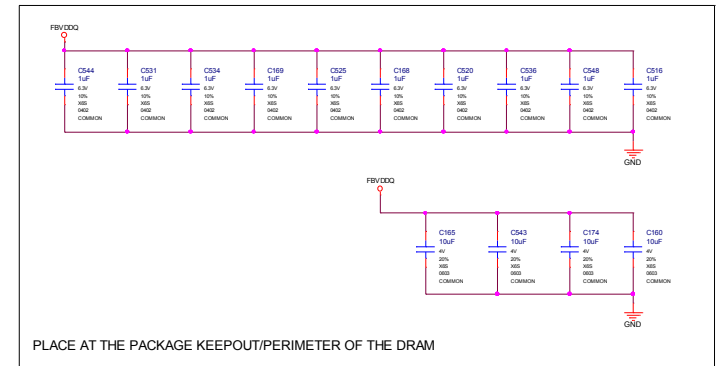
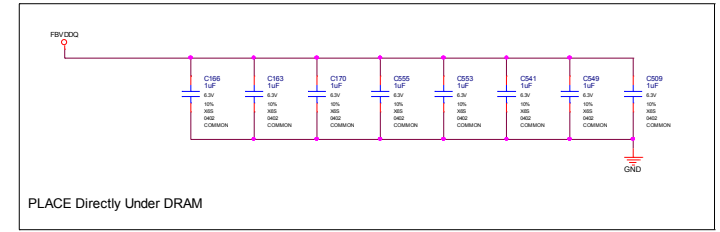
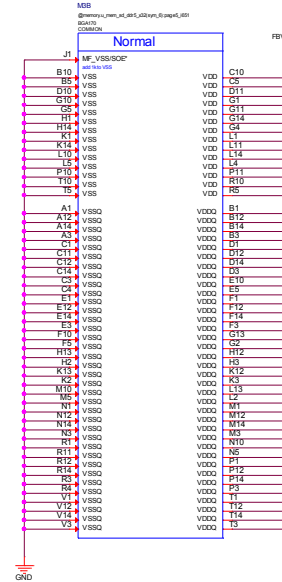
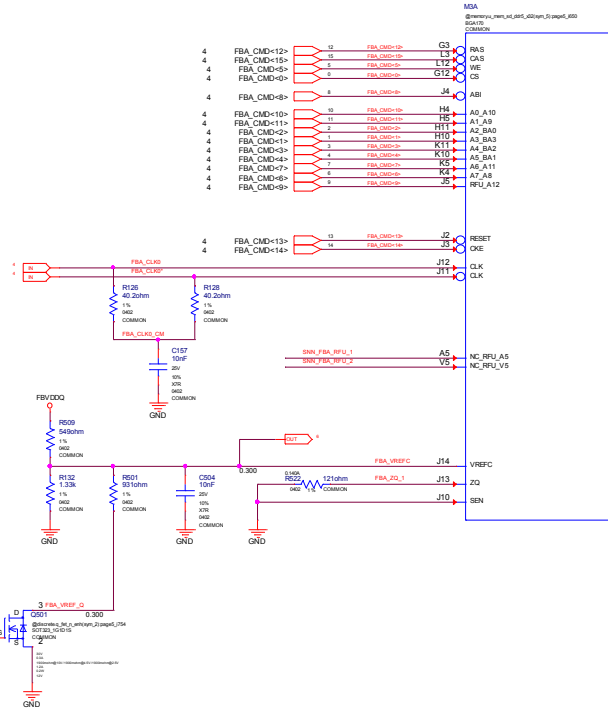
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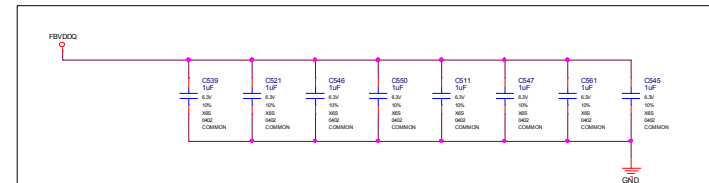
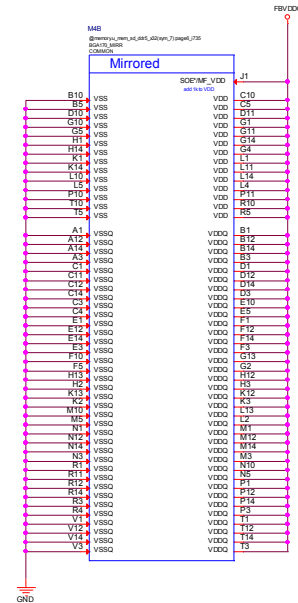
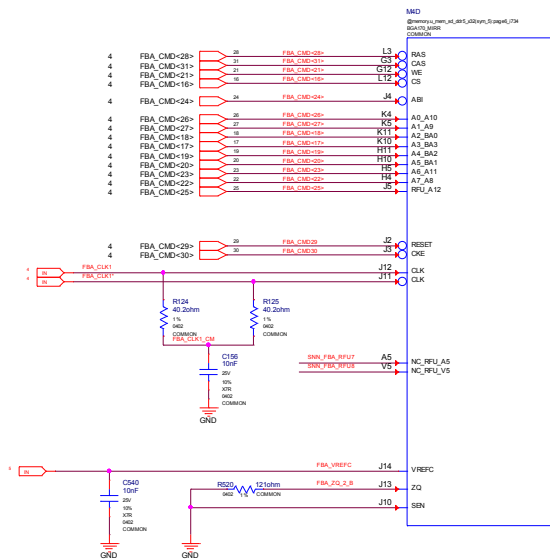
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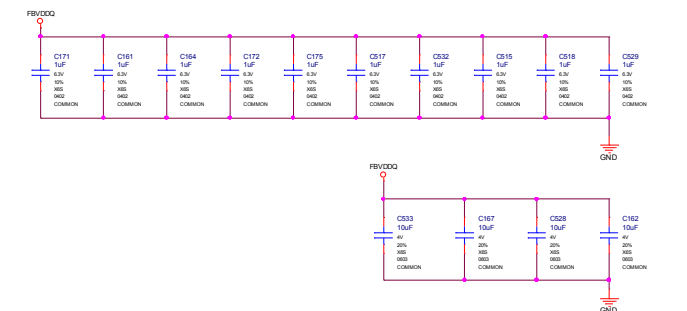
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CM00	CS*	
CM01	A3, BA3	
CM02	A2, BA2	
CM03	A4, BA2	
CM04	A2, BA1	
CM05	WE*	
CM06	A7, A8	
CM07	A6, A11	
CM08	AR*	
CM09	A12, RFU	
CM10	A0, A10	
CM11	A1, A9	
CM12	RA5*	
CM13	RS*	
CM14	CK*	
CM15	CAS*	
CM16		CS*
CM17		A3, BA3
CM18		A2, BA2
CM19		A4, BA2
CM20		A2, BA1
CM21		WE*
CM22		A7, A8
CM23		A6, A11
CM24		AR*
CM25		A12, RFU
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CM27		A1, A9
CM28		RA5*
CM29		RS*
CM30		CK*
CM31		CAS*



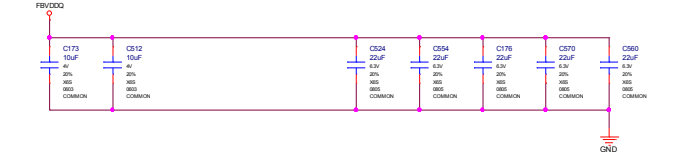
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CMD1	A3..BA3	
CMD2	A2..BA2	
CMD3	A1..BA2	
CMD4	AS..BA1	
CMD5	WE*	
CMD6	A7..A8	
CMD7	AE..A11	
CMD8	ASF	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A9	
CMD12	RA5*	
CMD13	RS1*	
CMD14	ONE*	
CMD15	CAN*	
CMD16		CS*
CMD17	A3..BA3	
CMD18	A2..BA2	
CMD19	AS..BA2	
CMD20	AE..BA1	
CMD21	WE*	
CMD22	A7..A8	
CMD23	AE..A11	
CMD24	ASF	
CMD25	A12..RFU	
CMD26	A0..A10	
CMD27	A1..A9	
CMD28	RA5*	
CMD29	RS1*	
CMD30	ONE*	
CMD31	CAN*	



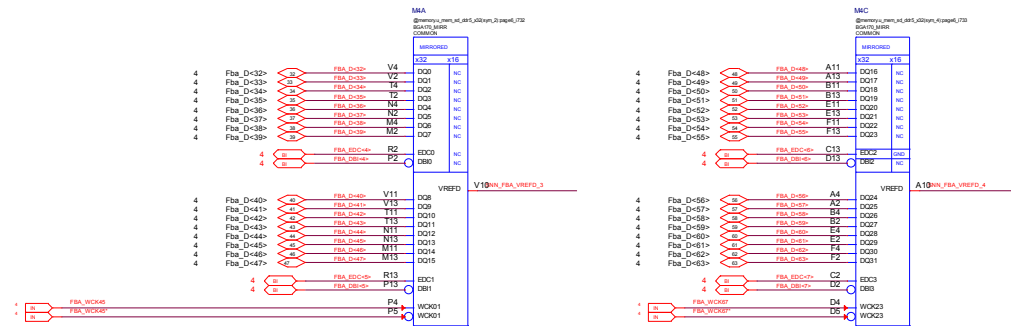
PLACE Directly Under DRAM




PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM



PLACE Around DRAM



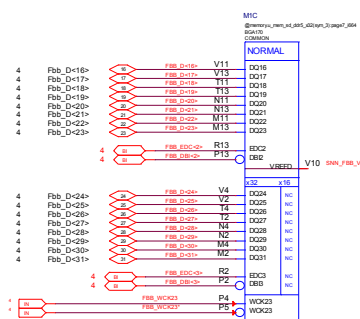
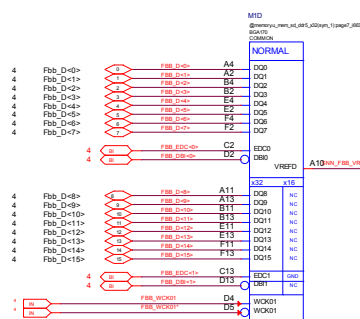
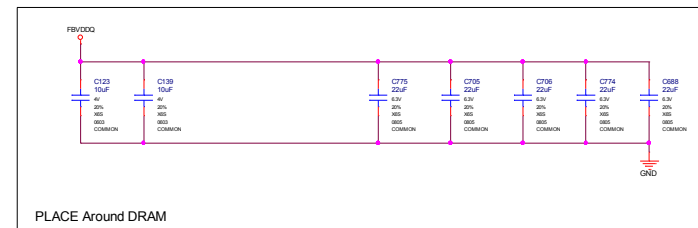
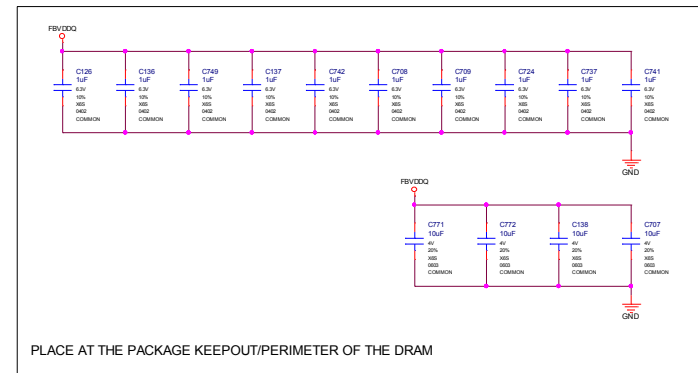
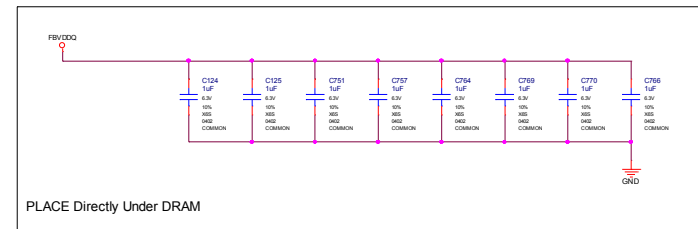
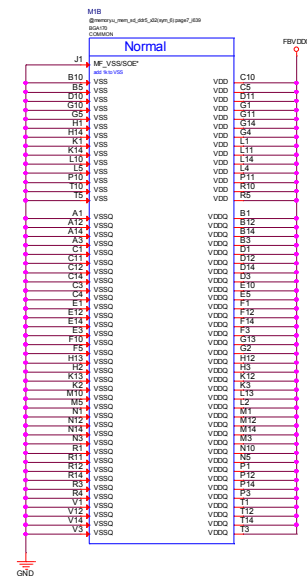
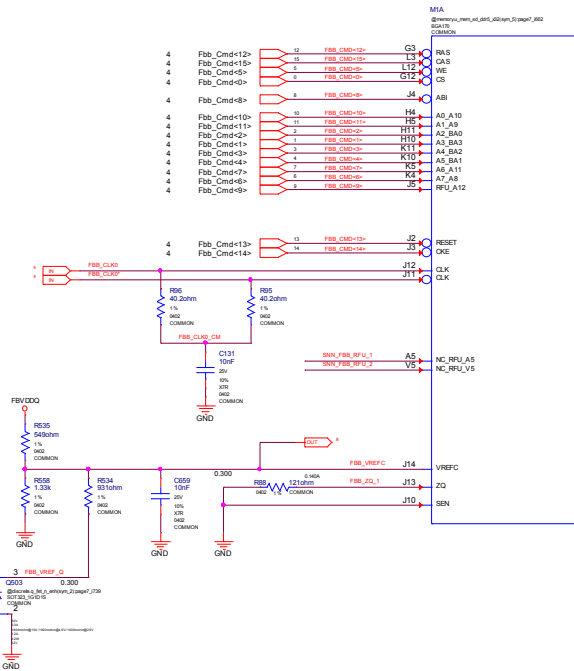
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<b>NV_PN</b>		<b>600-1G210-BASE-SCH</b>	
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MEMORY: FBB Partition 31..0

CMD	0.31	32.63
OM09	CS*	
OM01	A3_BA3	A3_BA3
OM02	A2_BA2	A2_BA2
OM03	A4_BA2	A4_BA2
OM04	AS_BA1	AS_BA1
OM05	WE*	
OM06	A7_AB	
OM07	AB_A11	
OM08	AB*	
OM09	A12_RPU	
OM10	A2_A10	
OM11	A1_A9	
OM12	RS1*	
OM13	RA*	
OM14	CK*	
OM15	CAS*	
OM16		CS*
OM17		A3_BA3
OM18		A2_BA2
OM19		A4_BA2
OM20		AS_BA1
OM21		WE*
OM22		A7_AB
OM23		AB_A11
OM24		AB*
OM25		A12_RPU
OM26		A2_A10
OM27		A1_AB
OM28		RA*
OM29		RS1*
OM30		CK*
OM31		CAS*



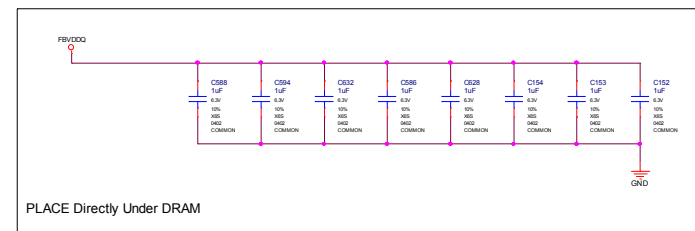
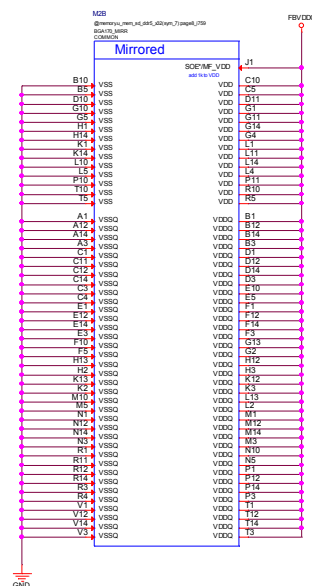
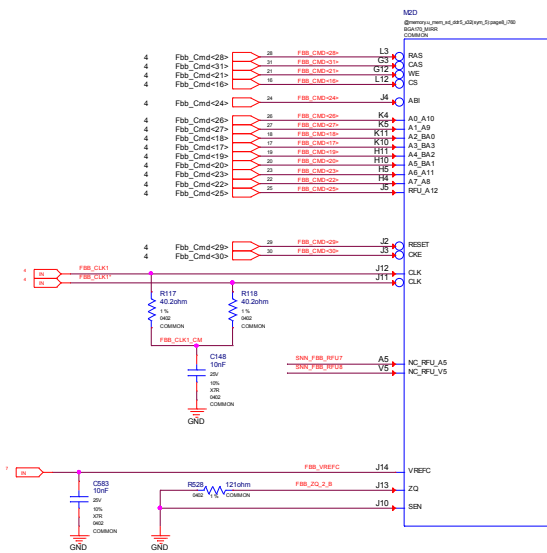
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<b>NV_PN</b>	<b>600-1G210-BASE-SCH</b>		
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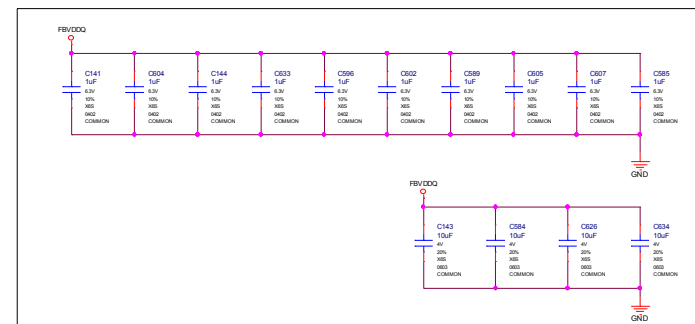
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MEMORY: FBB Partition 63..32

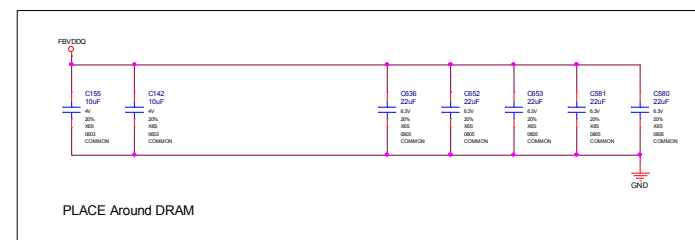
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CM01	A3..BA3	
CM02	A2..BA0	
CM03	A2..BA2	
CM04	A5..BA1	
CM05	WE*	
CM06	A7..A8	
CM07	AE..A11	
CM08	AS*	
CM09	A12..RPU	
CM10	A0..A10	
CM11	A7..A9	
CM12	RA5*	
CM13	RS1*	
CM14	OE*	
CM15	CAS*	
CM16		CS*
CM17		A3..BA3
CM18		A2..BA0
CM19		A4..BA2
CM20		AS..BA1
CM21		WE*
CM22		A7..A8
CM23		AE..A11
CM24		AS*
CM25		A12..RPU
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CM27		A7..A9
CM28		RA5*
CM29		RS1*
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CM31		CAS*



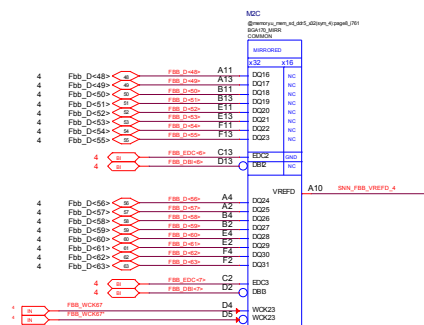
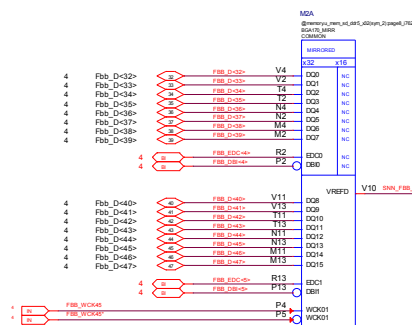
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PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM




PLACE Around DRAM



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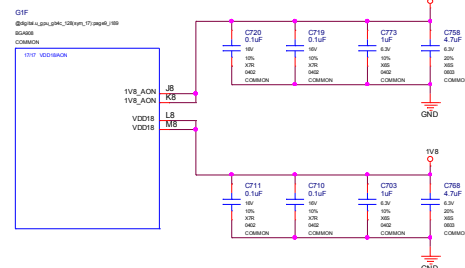
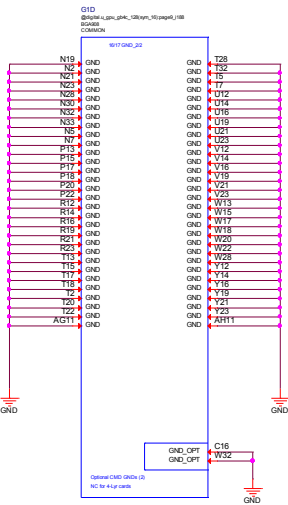
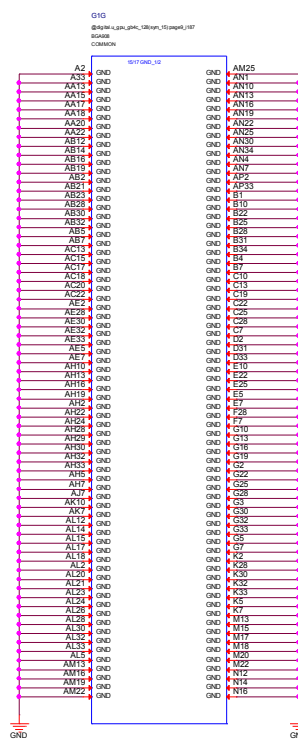
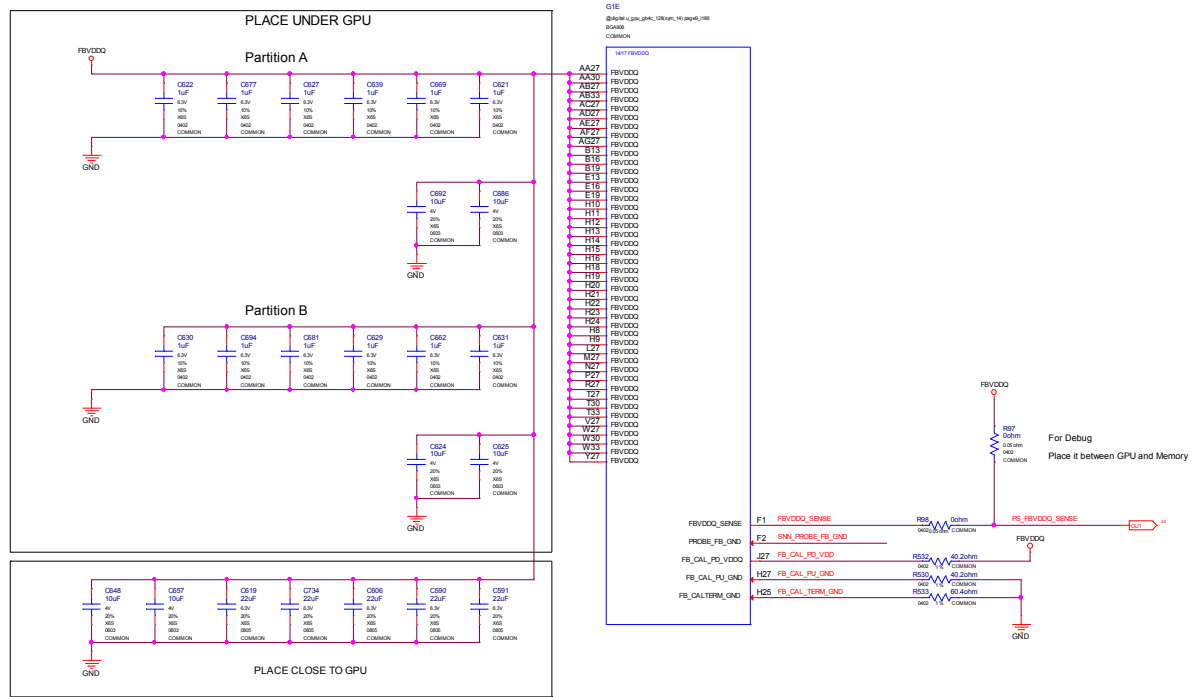
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<b>NV_PN</b> PCB REV BOM REV	<b>600-1G210-BASE-SCH</b> PG210-800 A		
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## GPU FBVDDQ & 1V8 Decoupling



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PAGE DETAIL	GPU FBVDDQ & 1V8 Decou

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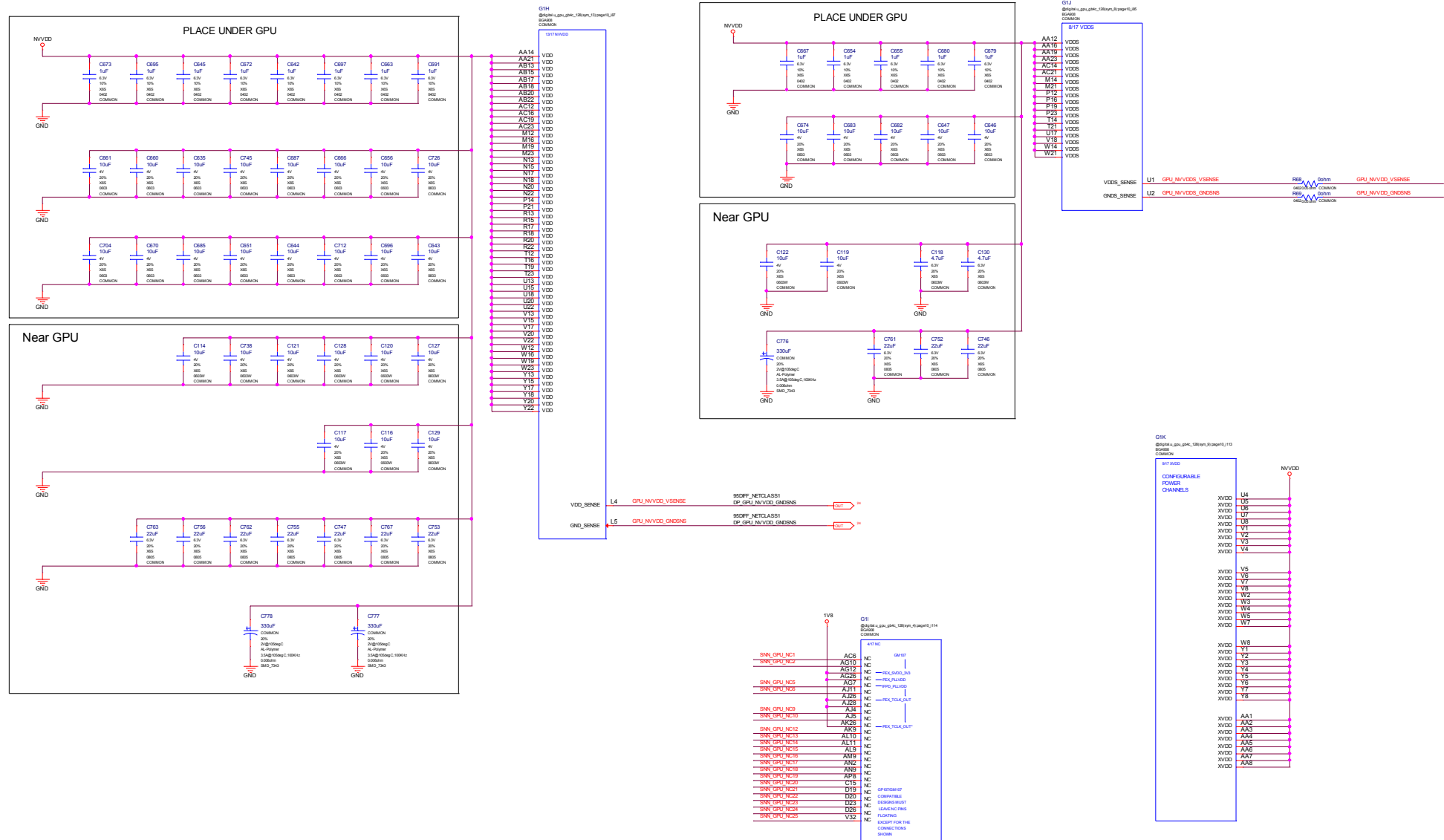


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## GPU NVVDD & NVVDDS Decoupling



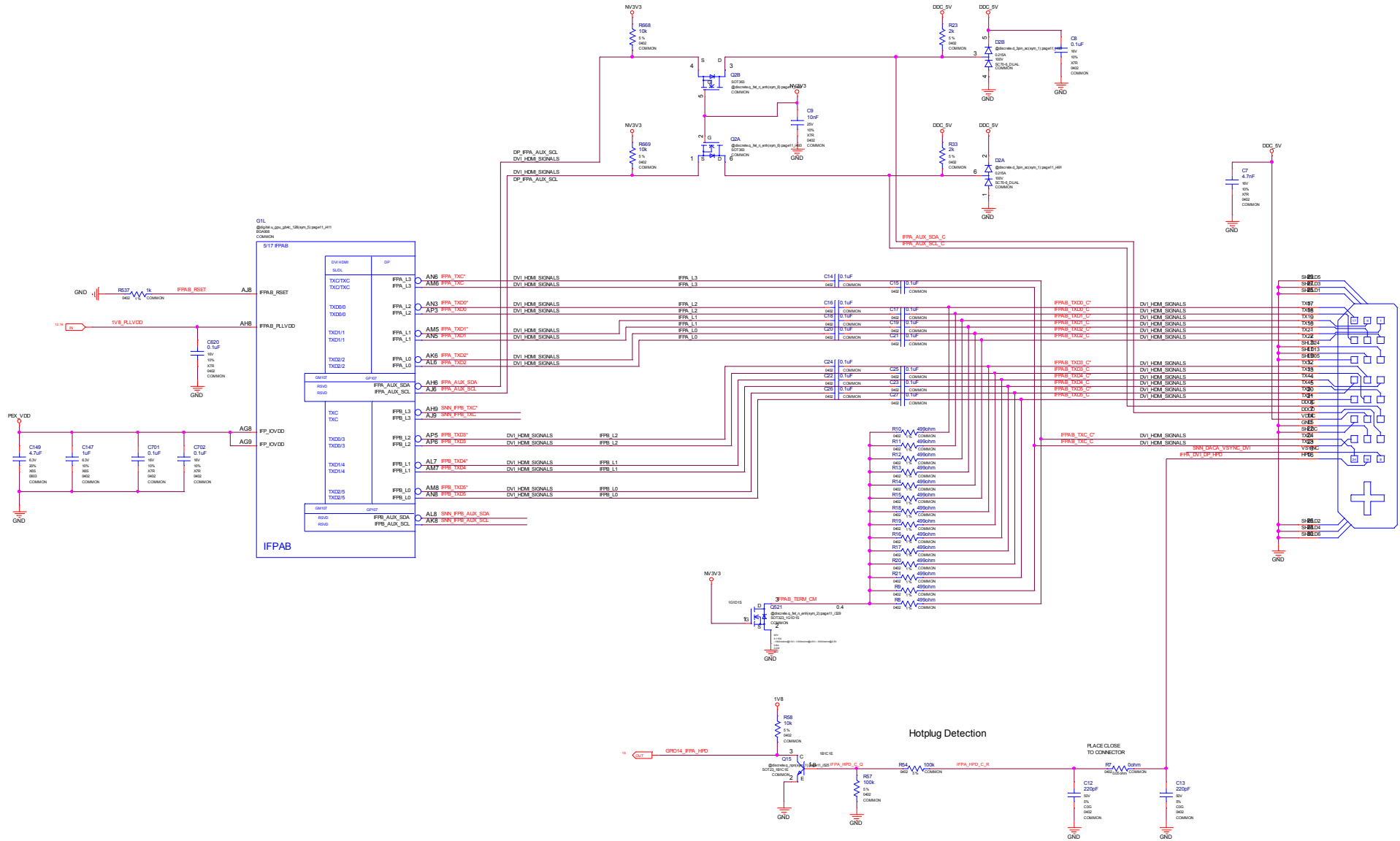
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IFPAB DVI-DL

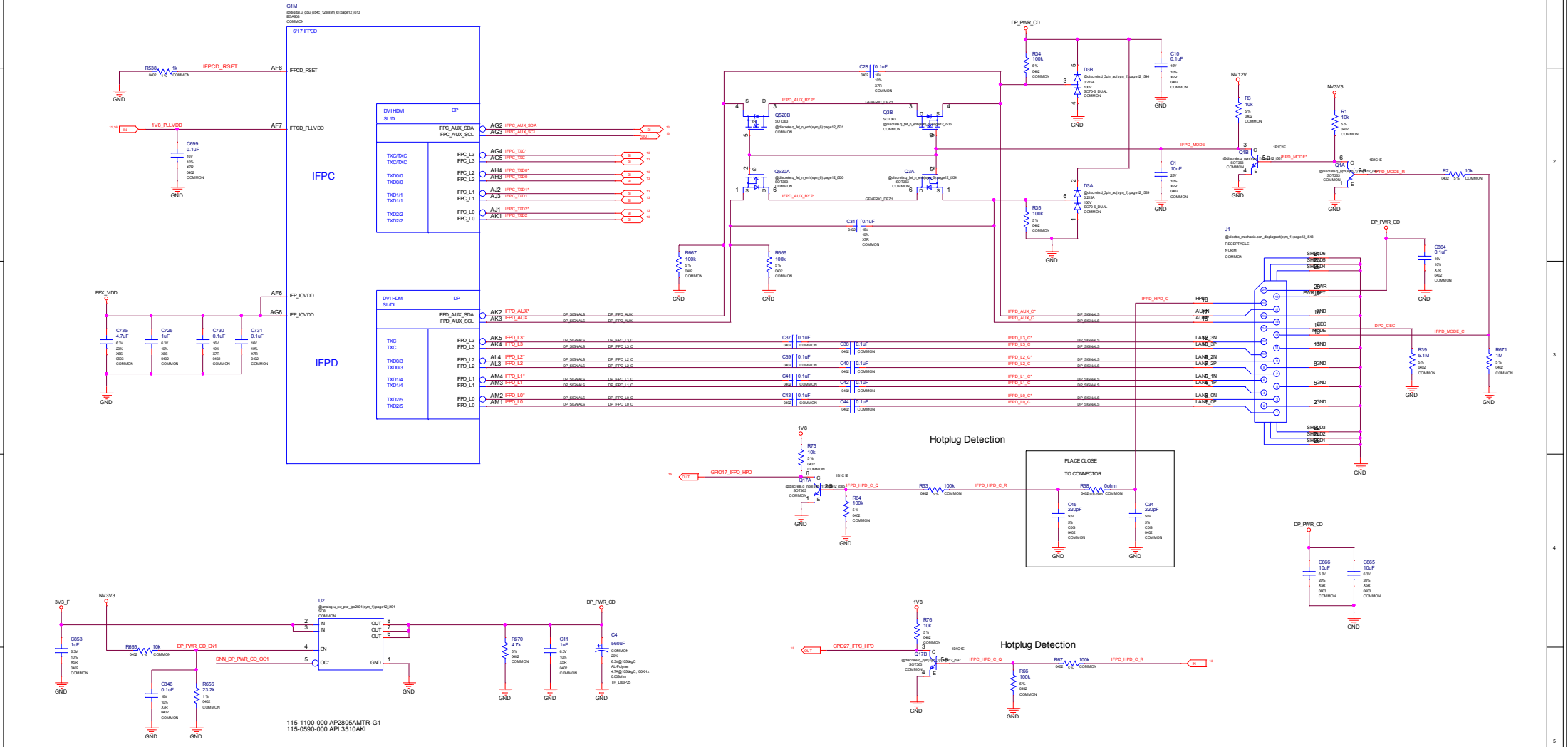


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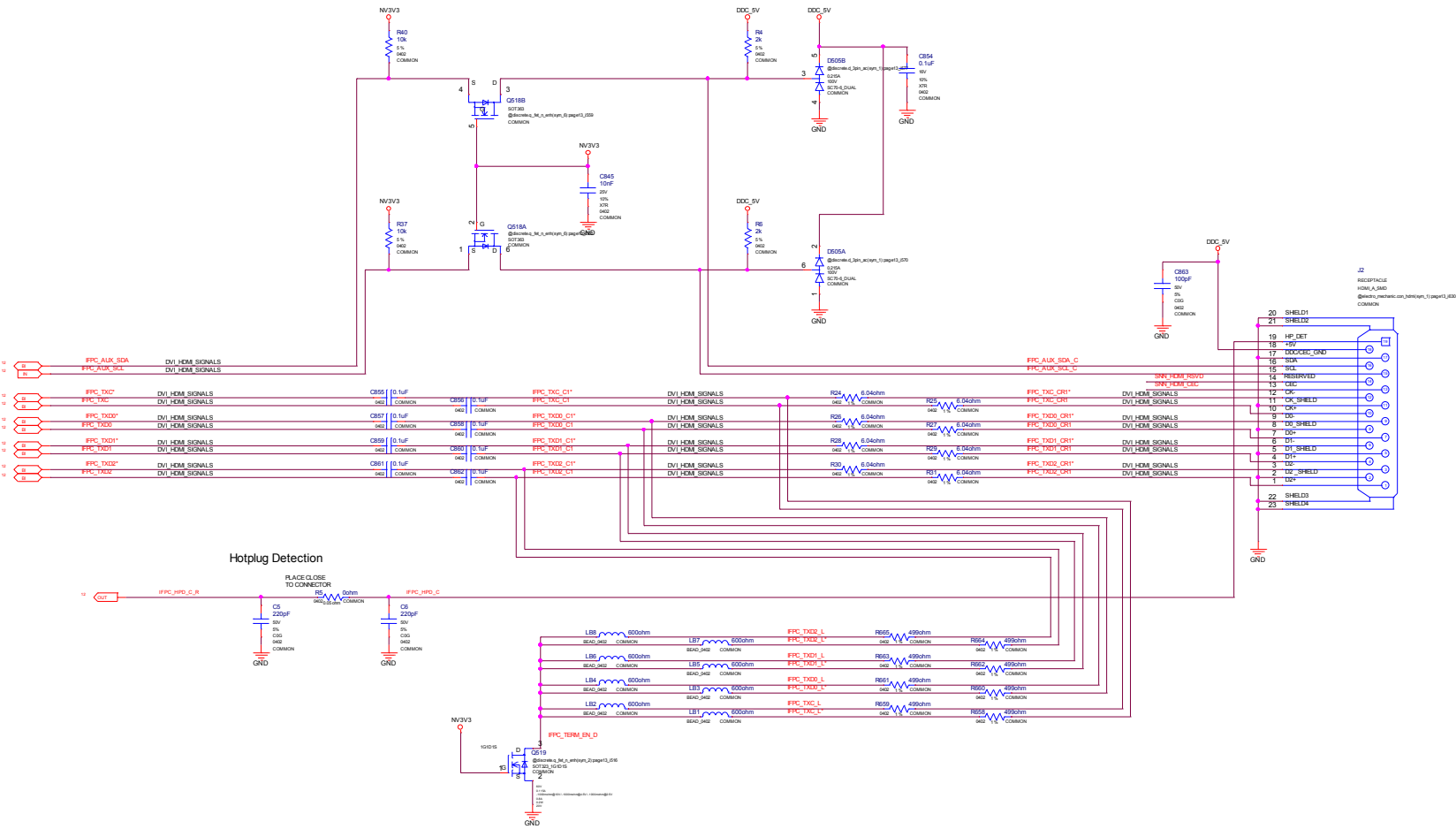
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IFPD DP



IFPC HDMI



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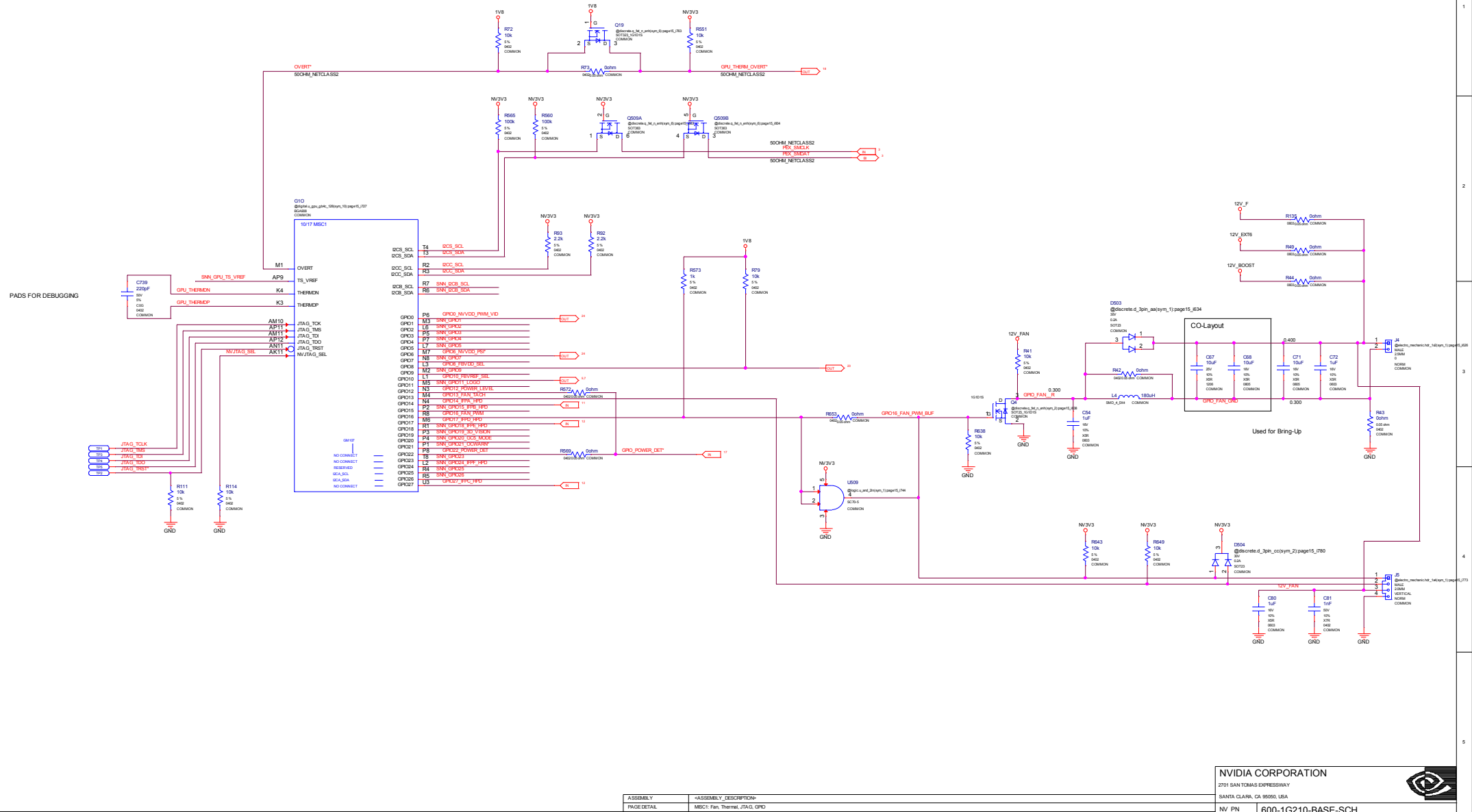
ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	IFPC HDMI

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2701 SANTOMAS EXPRESSWAY	
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MISC1: GPIO, Fan, Thermal, JTAG



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MSC1: Fan, Thermal, JTAG, I

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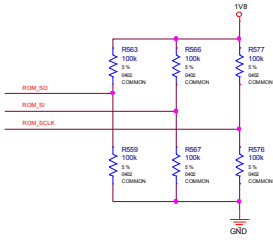
## MISC2: ROM, XTAL, Straps

ROM\_SO ROM\_SI ROM\_SCLK SOR\_EXPOSED[3:0] 1:ENABLE 0:DISABLE

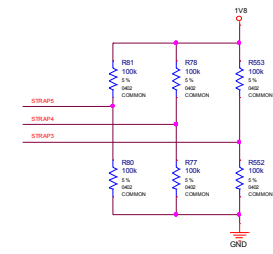
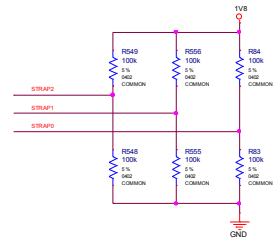
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L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

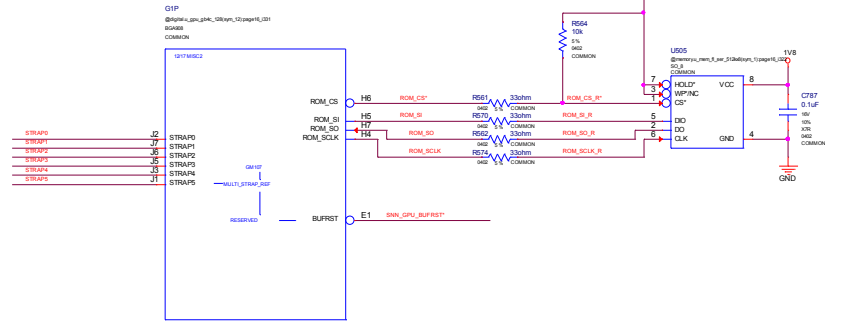
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0



H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

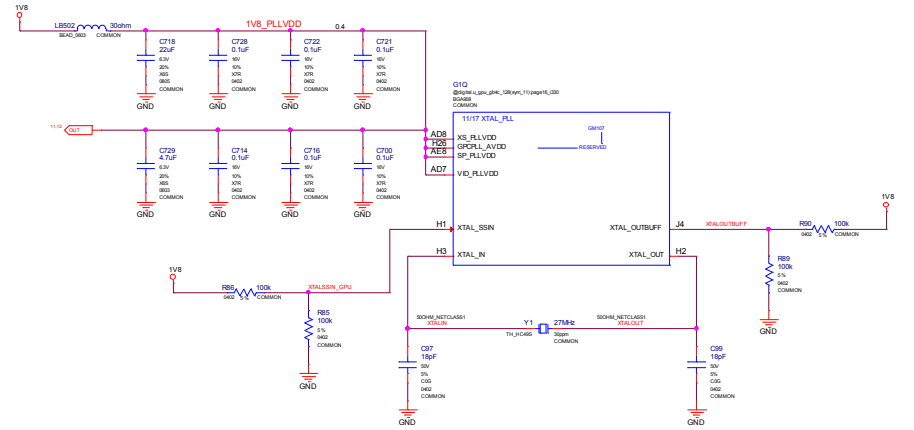


1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



### Smart Fan

XTALOUTBUFF	Voltage	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



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NV\_PN 600-1G210-BASE-SCH

PCB REV PG210-800  
ROM REV A

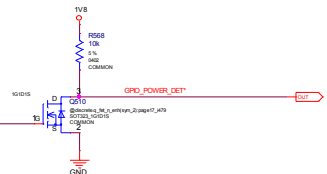
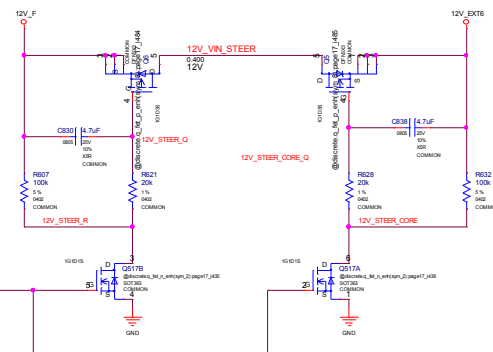
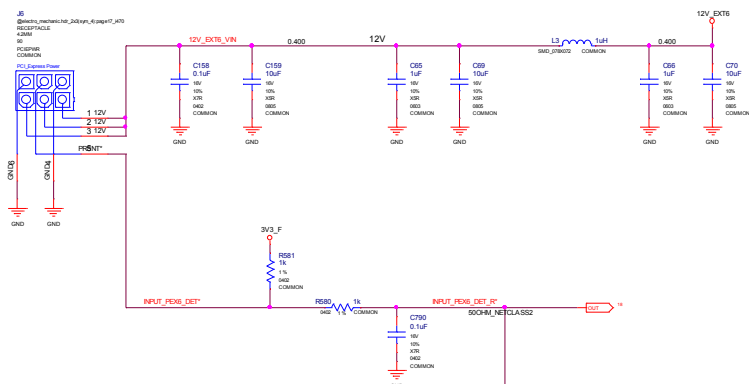
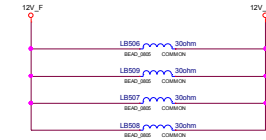
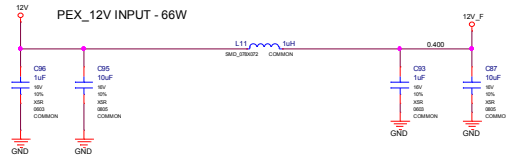
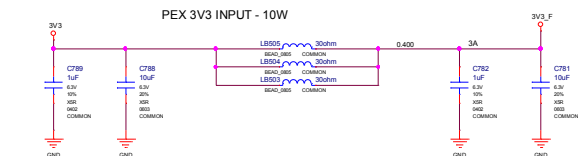
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ASSEMBLY	ASSEMBLY DESCRIPTION
PG210-800	MISC2 ROM, XTAL, Straps



## Power Inputs and Filtering



ASSEMBLY	<ASSEMBLY_DESCRIPTION
PAGE DETAIL	Power Inputs and Filtering

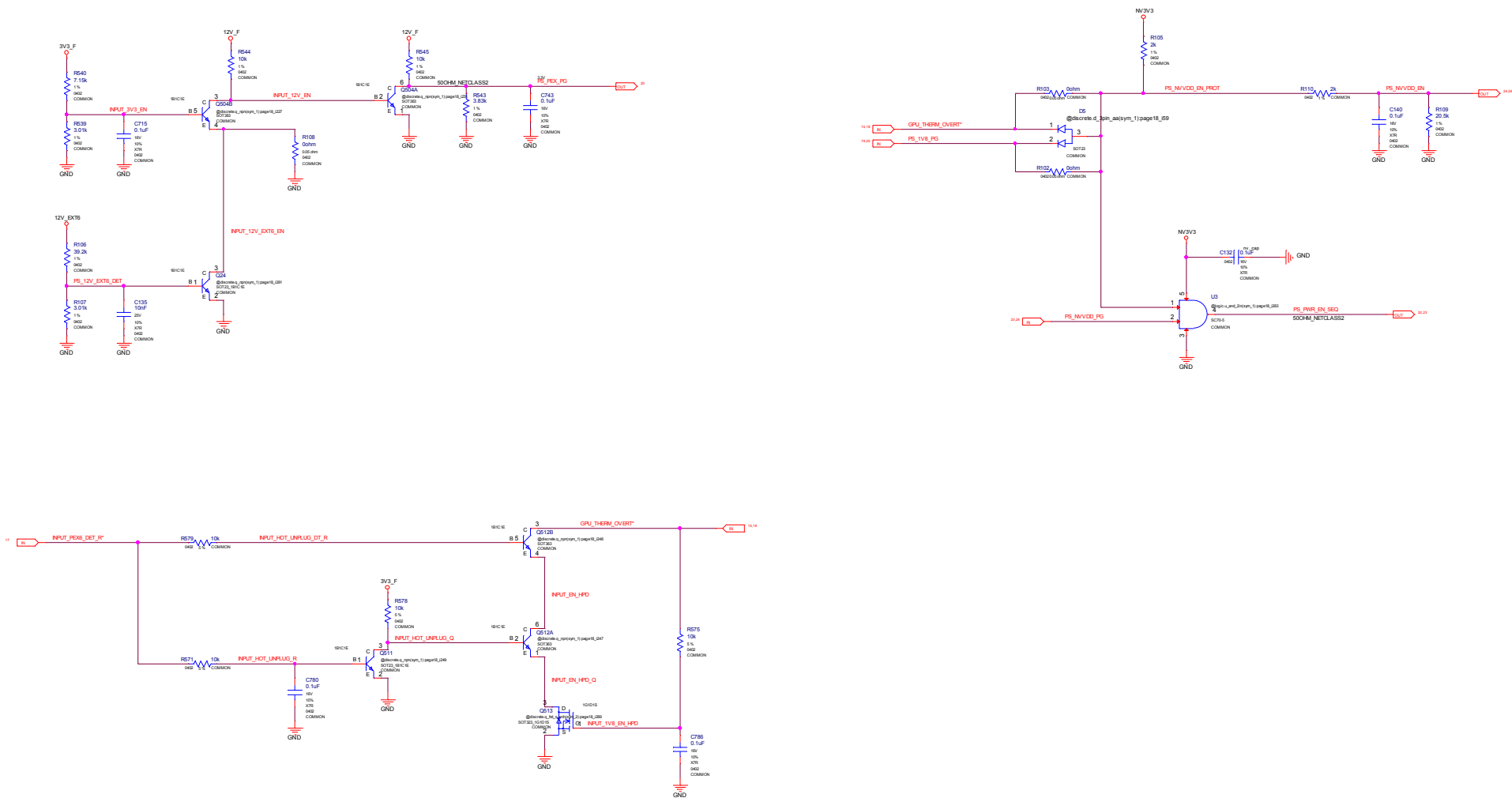
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## Power sequence



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Power Sequence

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NV_PN	600-1G210-BASE-SCH
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REV	000 13
PCB REV	PC210-H00

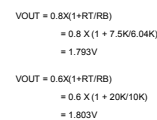
FGS REV	
BOM REV	


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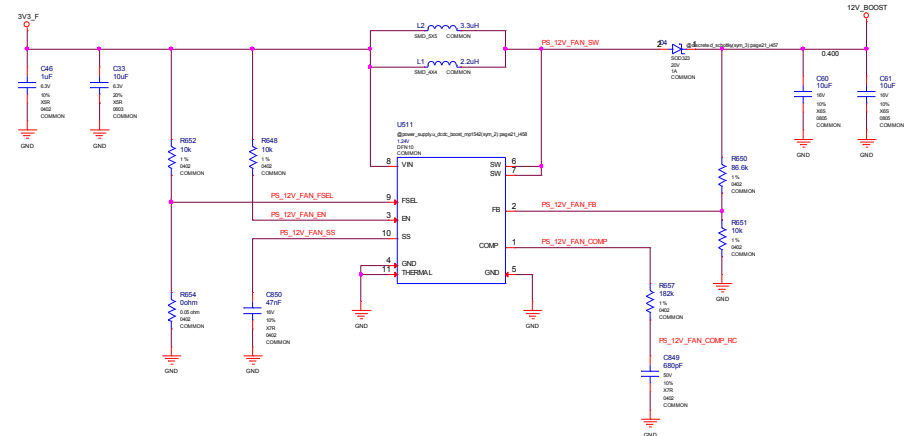
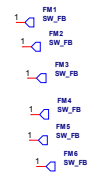
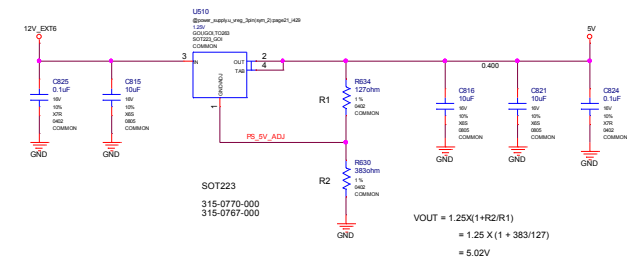
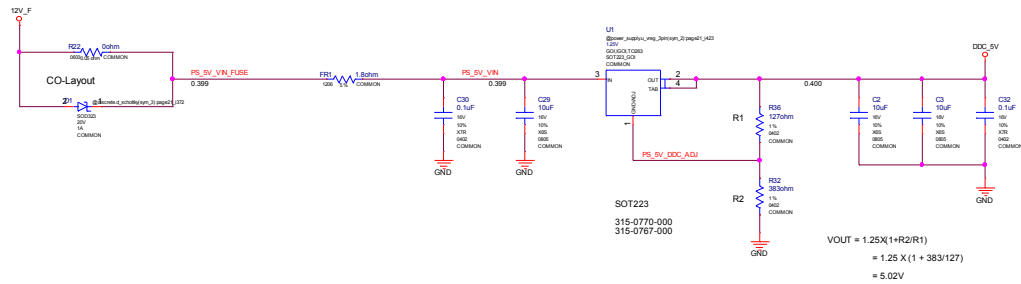




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## PSII:5V &amp; 12V\_FAN



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS1: 5V & 12V_FAN

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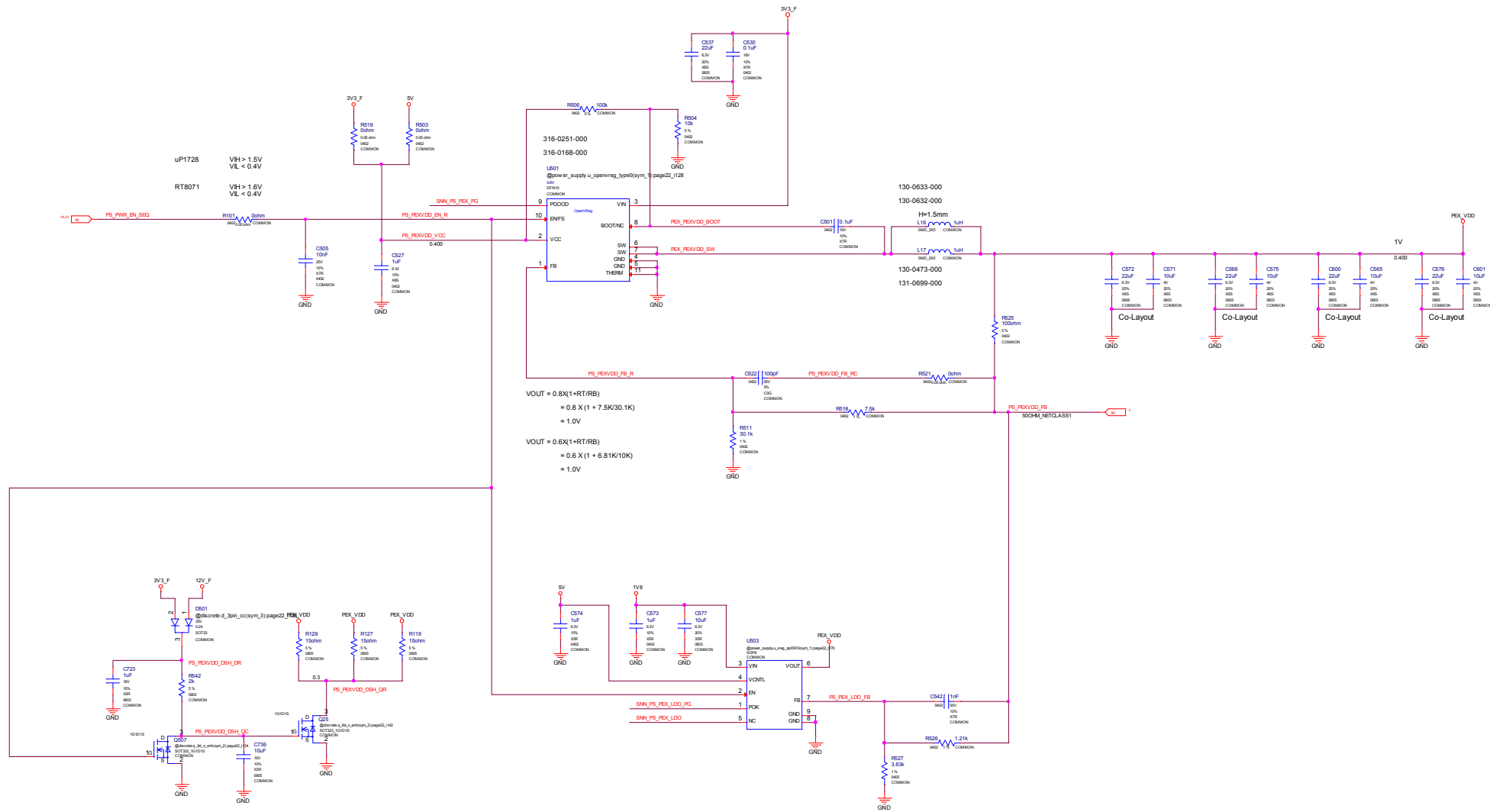
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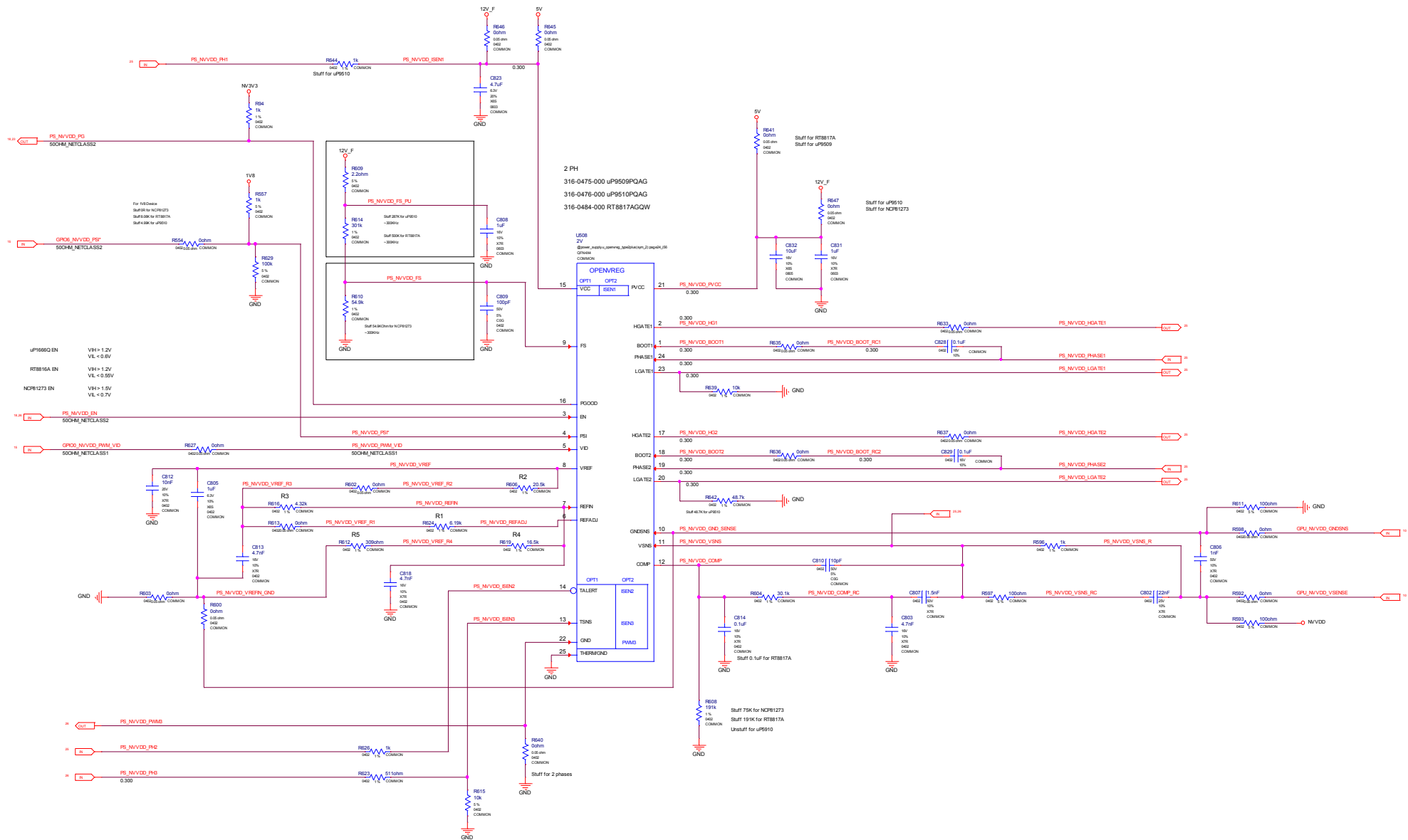
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# PS III: PEXVDD



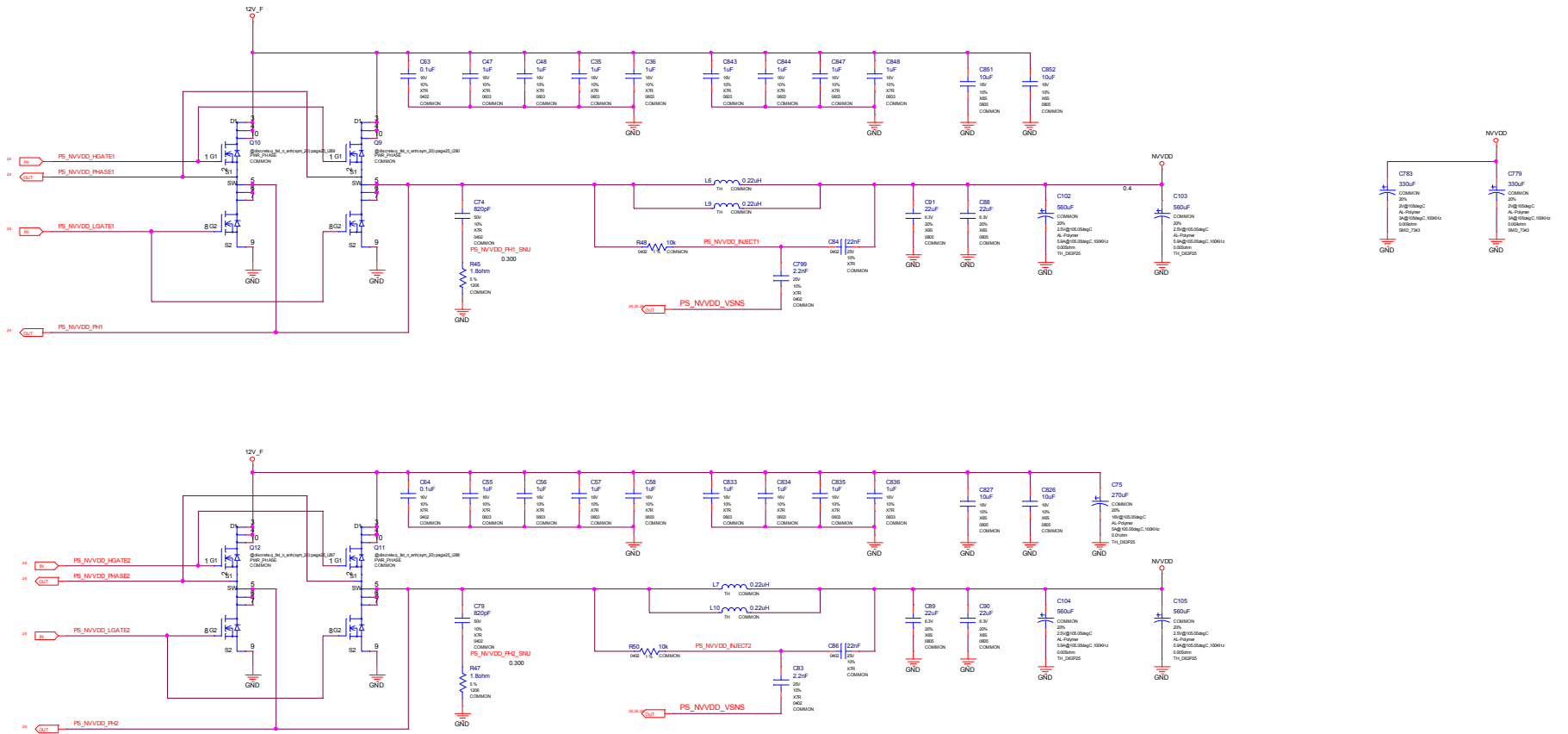


PS V: NWDD OVR2+1





PS V: NVVDD Phase 1,2



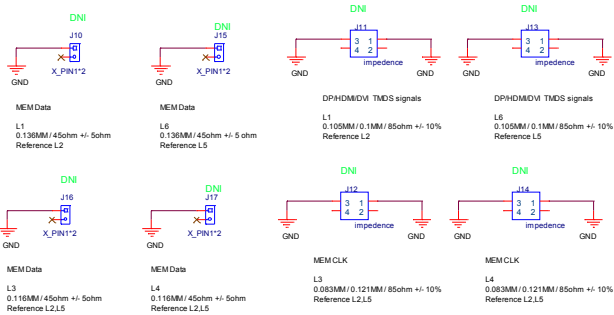
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ASSEMBLY	ASSEMBLY_DESCRIPTION
PAGE DETAIL	PS V: NVVDD Phase 1,2

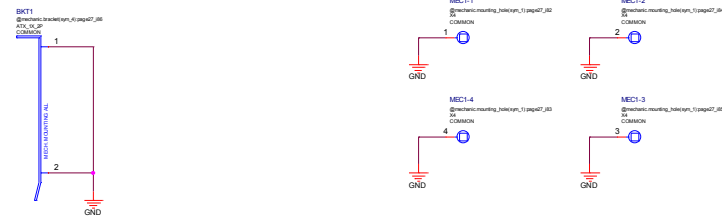
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Mechanical: Bracket/Thermal Solution



Brackets:



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH Bracket/Thermal

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