MS-V041 VER 20

NV43-PCIE NV43 256MB/128bit, BGA 16MX16 DDR2,VGA,DVI-I,TV-OUT(HT-10)

P295-A00 DESIGN NV43 300/267MHZ 128MB/256MB/512MB DDR2 84-FBGA

PAGE SUMMARY:

DDR2 84-FBGA Clock setting 350MHZ

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	602-10295-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	602-10295-0000-000	GF-6600-A04 GEN 300/267MHZ 256MB 84-FBGA DDR2 16MX16 VGA+DVI-I+HDTV
2	SKU001	602-10295-0001-000	GF-6600-A04 GEN 300/267MHZ 128MB 84-FBGA DDR2 8MX16 VGA+DVI-I+HDTV
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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REV HISTORY

A00

-08/04/2005:

1.Page18: change power solution to RT9218 for NVVDD & FBVDDQ

10S

-08/04/2005:

1.Page18: Move C913~C916 out form C910,C911 & Move C930,C931 out form C929

2.Page19: Add C940 near C36

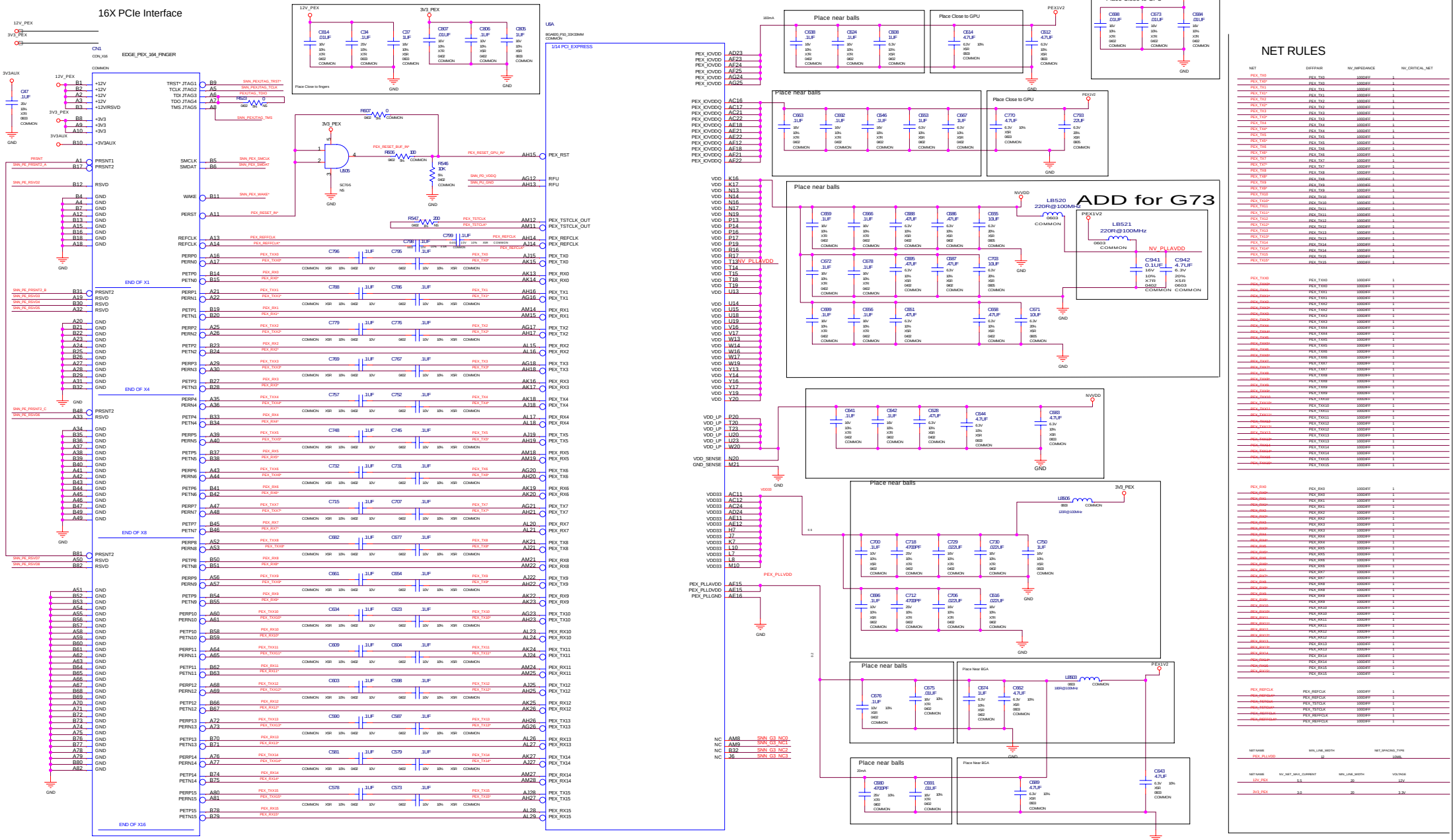
3.Page19: Remove C16, C35, C55

B00

-12/06/2005:

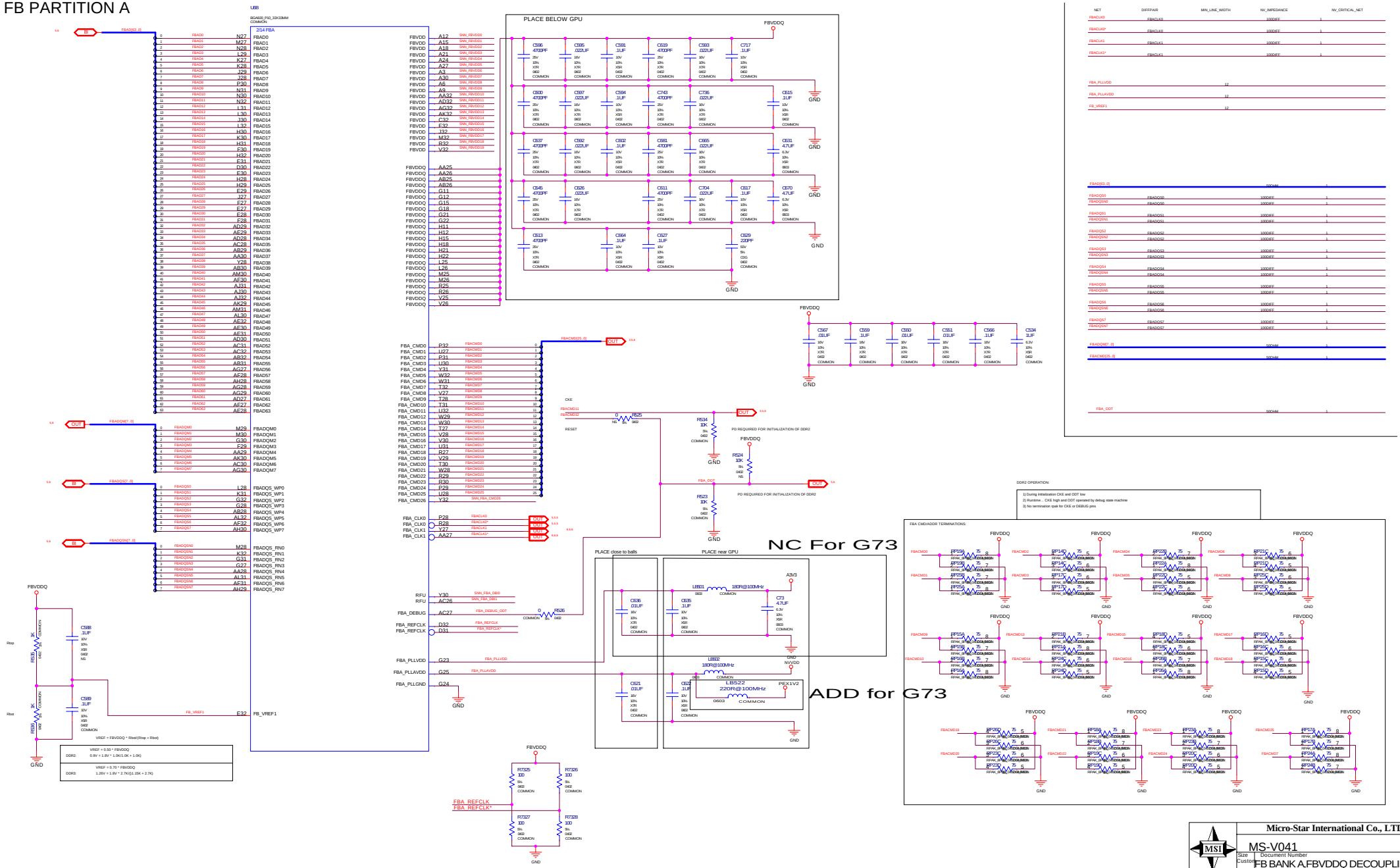
1.ADD G73 circuit

02 PCI EXPRESS, NVVDD, VDD33



03 FB BANK A, FBVDDQ DECOUPLING

FB PARTITION A



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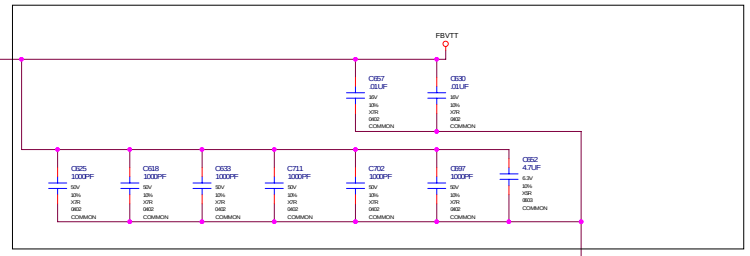
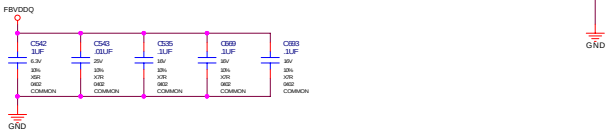
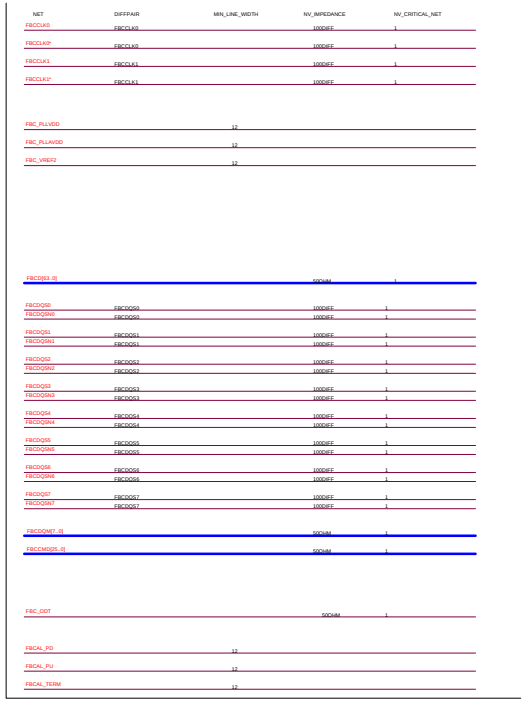
04 FB BANK C, FBVTT TERMINATIONS

FB PARTITION C

NC For G73

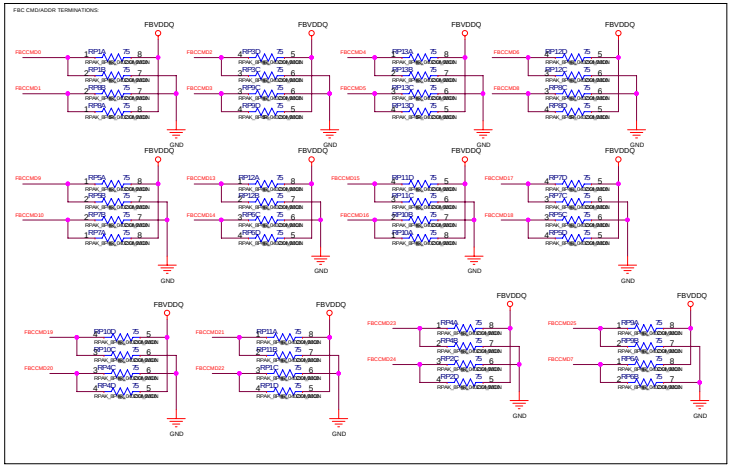


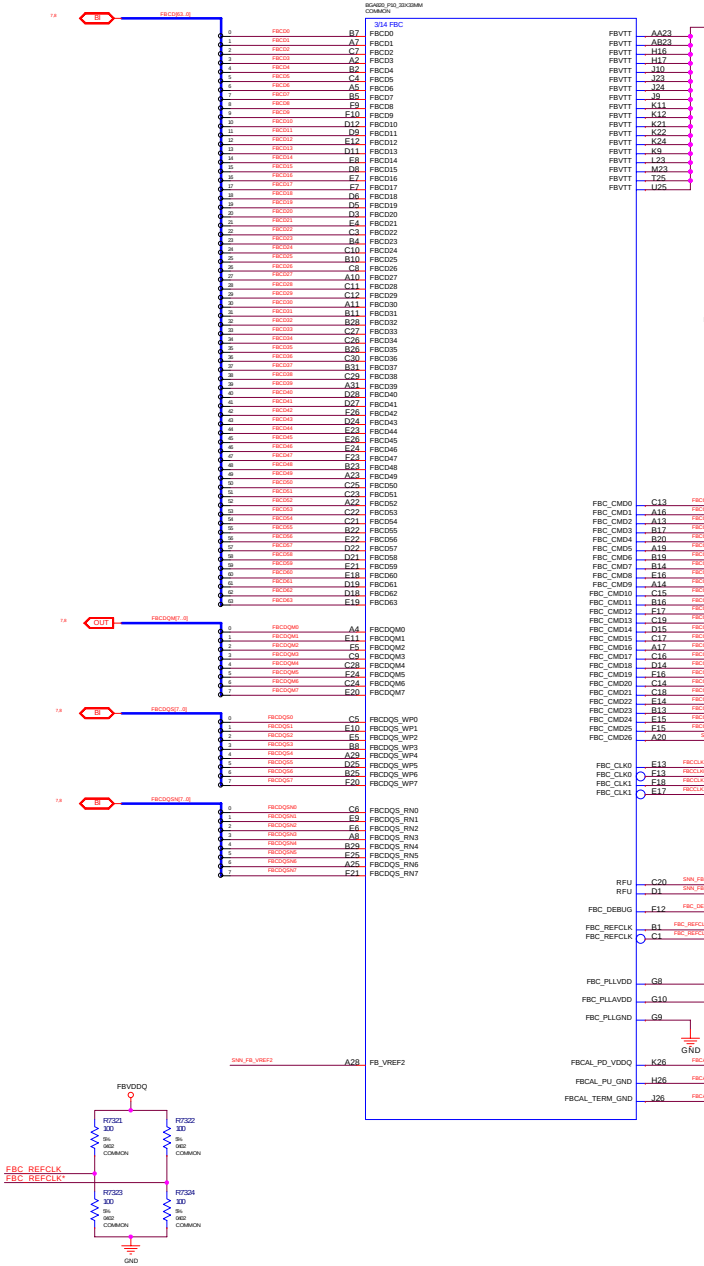


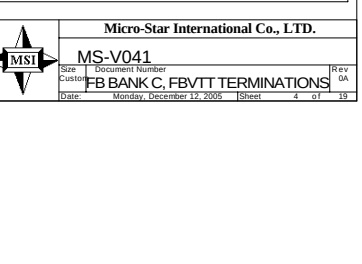


DDR2 OPERATION:

1) During initialization CKE and ODT low
2) Runtime - CKE high and ODT operated by debug state machine
3) No termination ipak for CKE or DEBUG pins



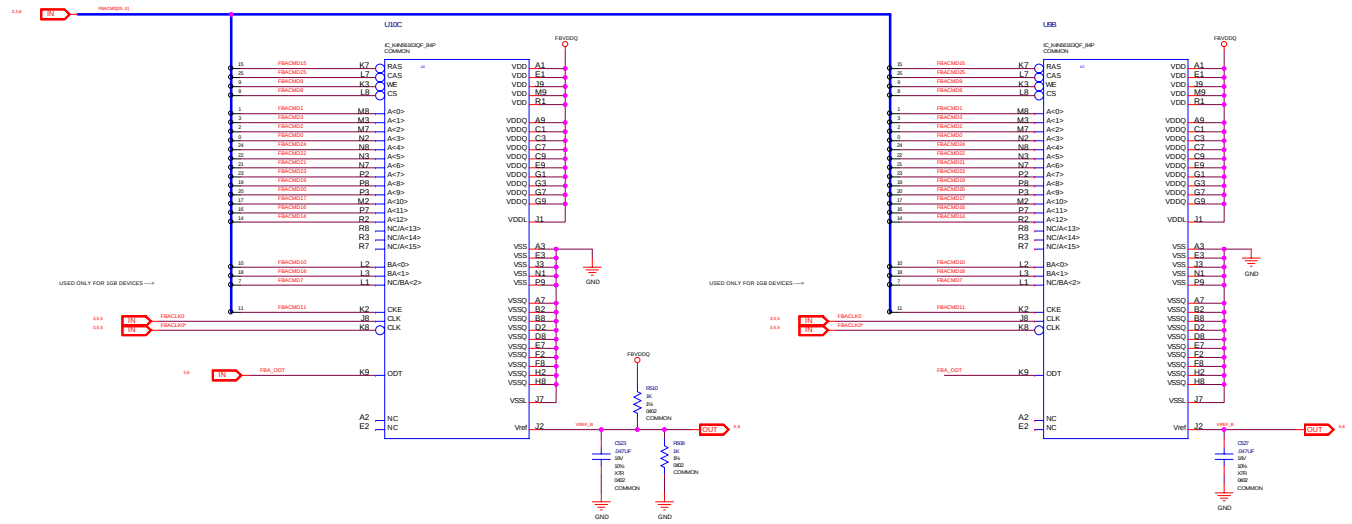


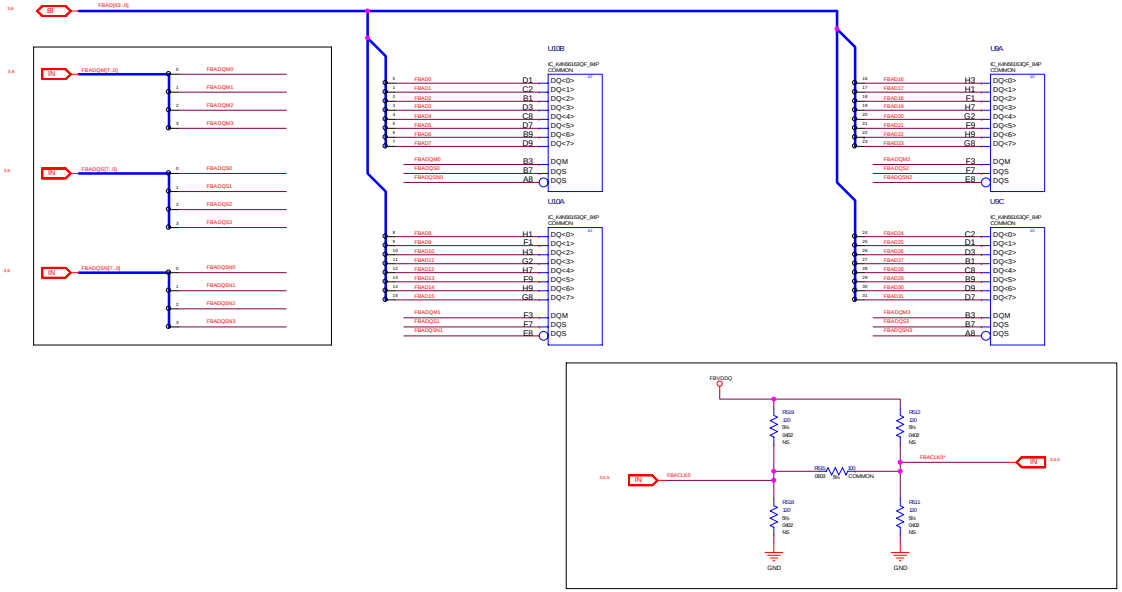


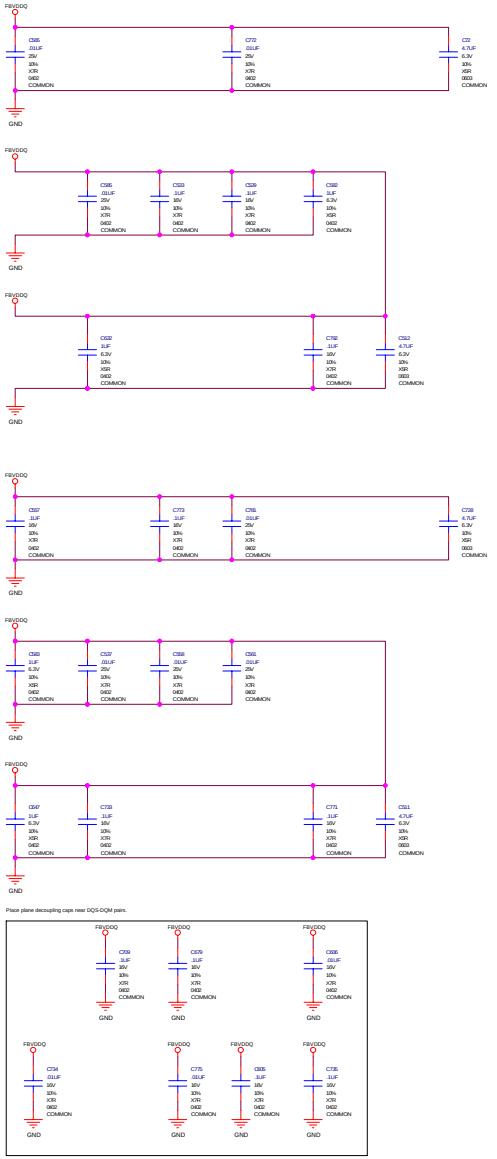
05 MEMORY PARTITION A 0..31

FBA MEMORY 1st bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY







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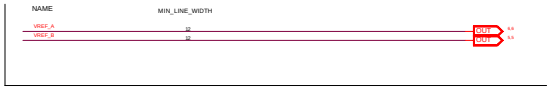
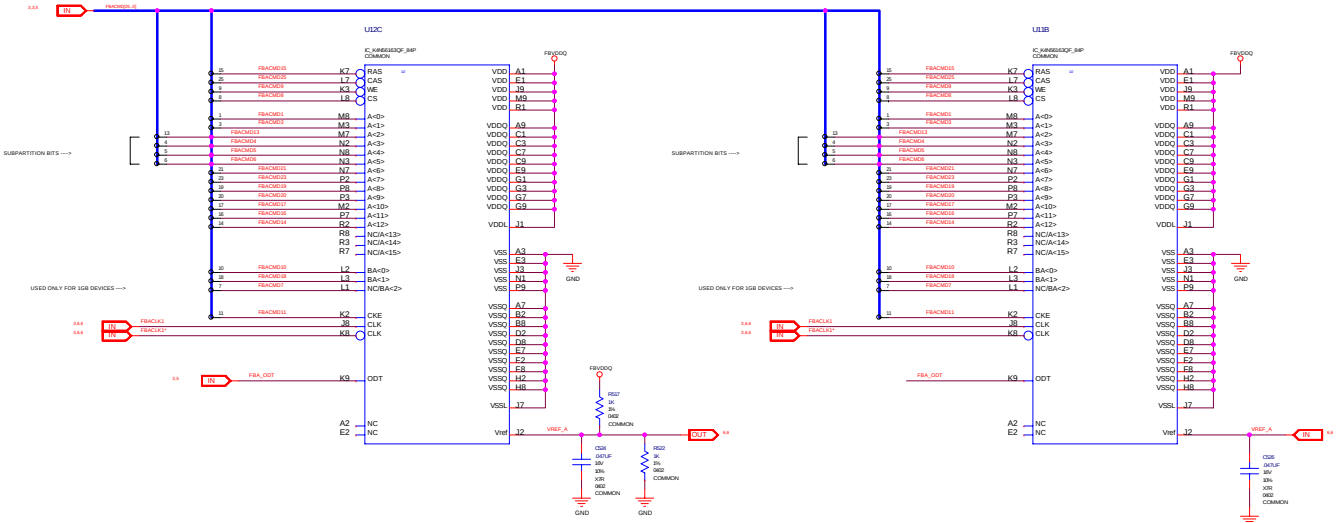
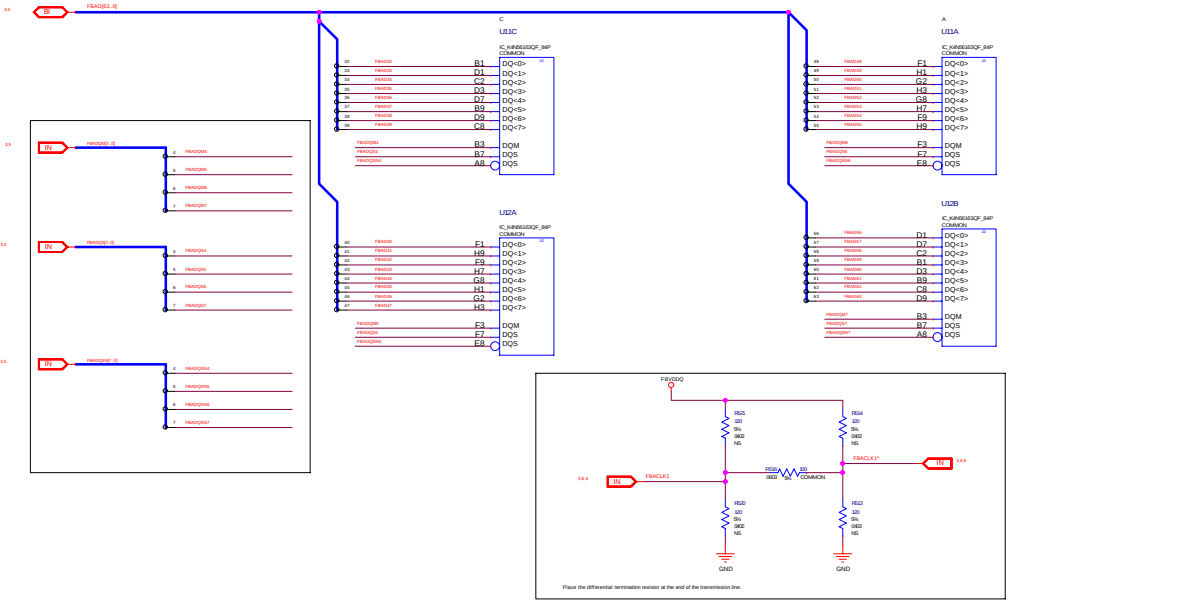
06 MEMORY PARTITION A 32..63

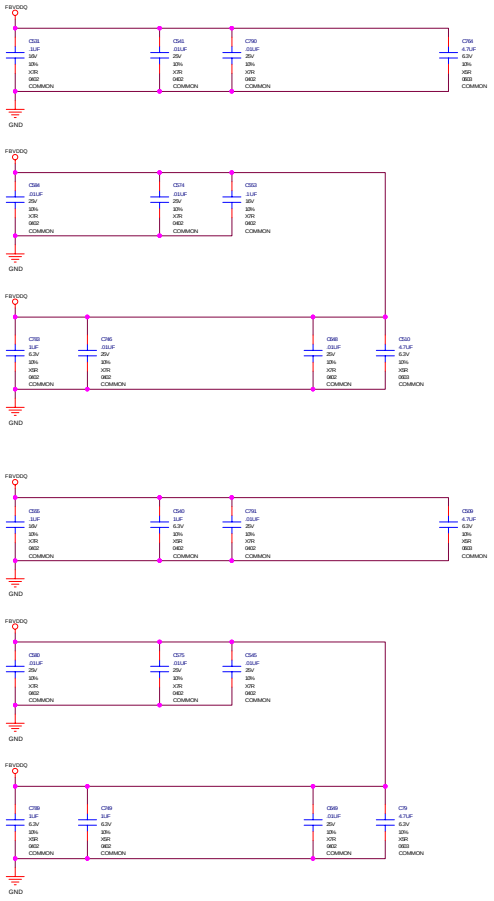
FBA MEMORY 1st bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY









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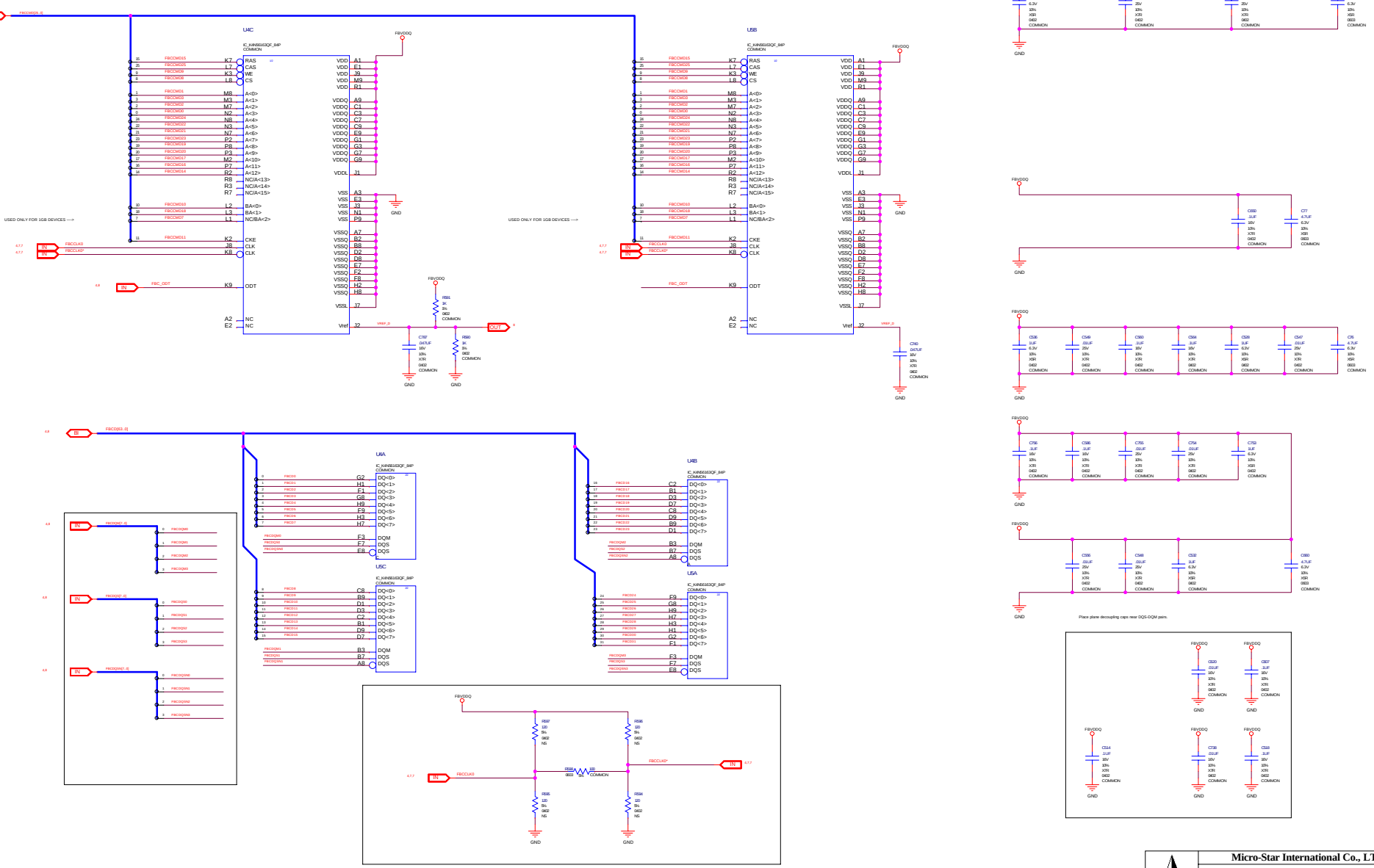
07 MEMORY PARTITION C 0..31

FBC MEMORY 2nd bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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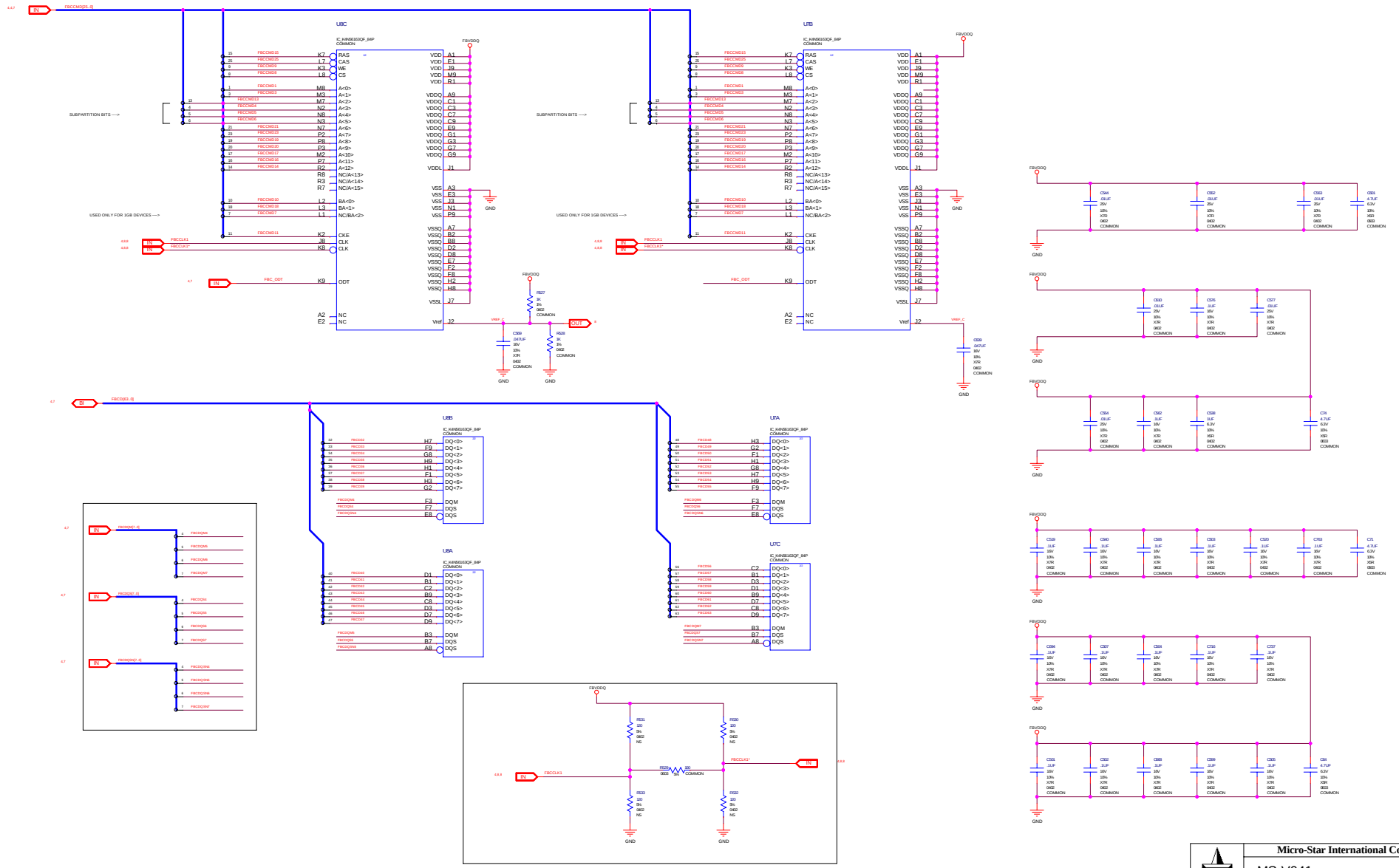
08 MEMORY PARTITION C 32..63

FBC MEMORY 2nd bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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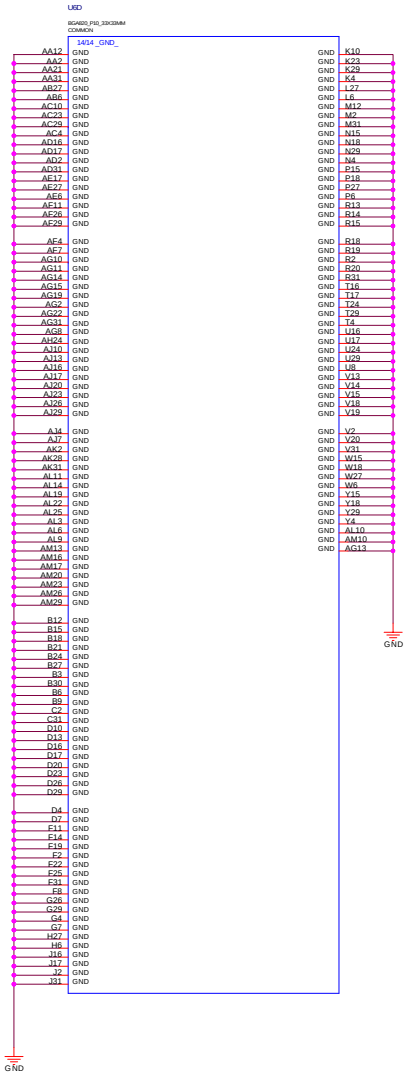
09 GPU GND



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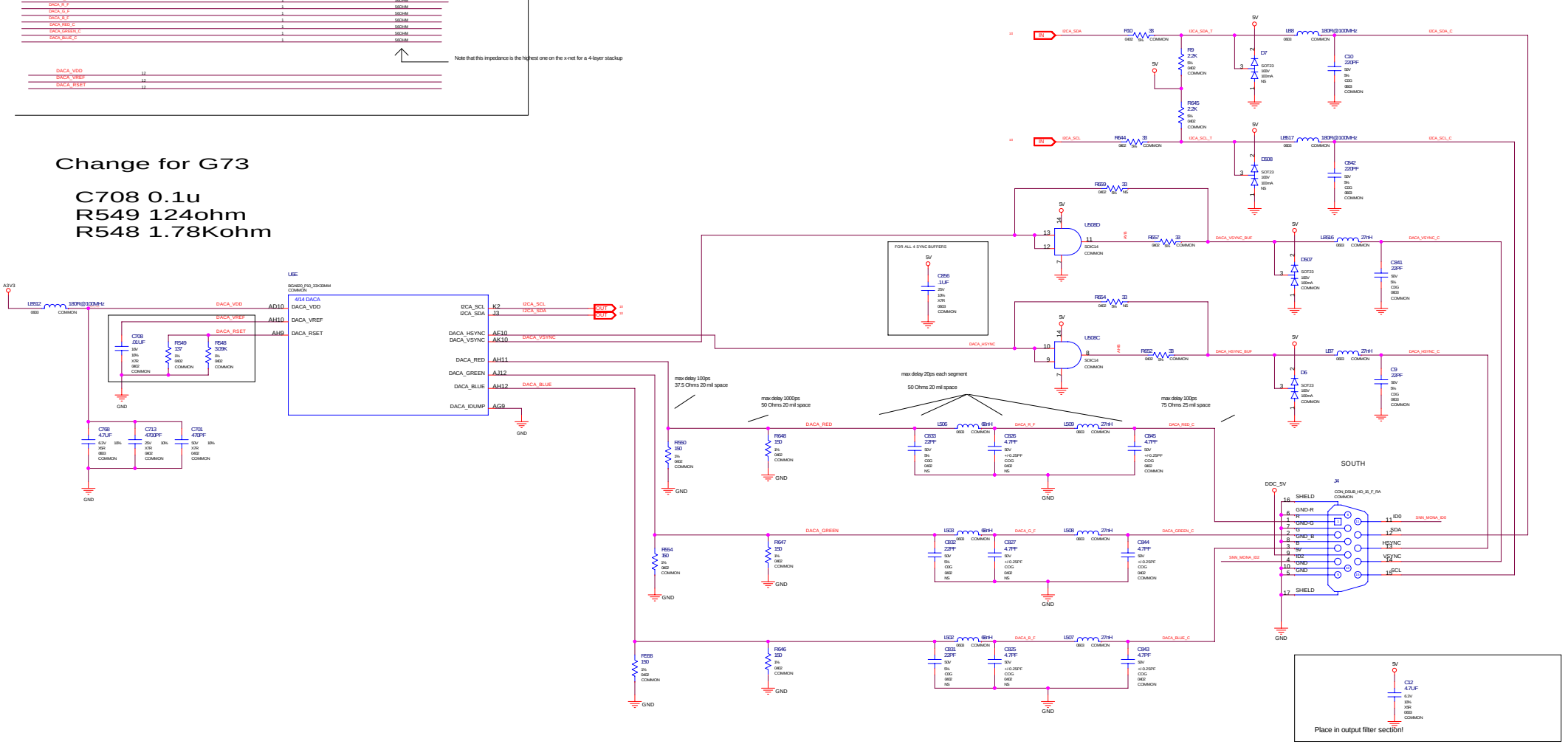
10 DACA - VGA

NET_NAME	MIN_LINE_WIDTH	NV_CRITICAL_NET	NV_IMPEDANCE
I2CA_SCL			
I2CA_SDA			
DACA_HSYNC		2	50OHM
DACA_VSYNC		2	50OHM
DACA_HSYNC_BUF		2	50OHM
DACA_VSYNC_BUF		2	50OHM
DACA_VSYNC_C		2	50OHM
DACA_HSYNC_C		2	50OHM
AVB		2	50OHM
AVB		2	50OHM
DACA_RED		1	50OHM
DACA_GREEN		1	50OHM
DACA_BLUE		1	50OHM
DACA_R_F		1	50OHM
DACA_G_F		1	50OHM
DACA_B_F		1	50OHM
DACA_RED_C		1	50OHM
DACA_GREEN_C		1	50OHM
DACA_BLUE_C		1	50OHM
DACA_VDD	12		
DACA_VREF	12		
DACA_RSET	12		

Note that this impedance is the highest one on the x-net for a 4-layer stackup

Change for G73

C708 0.1u
R549 124ohm
R548 1.78Kohm



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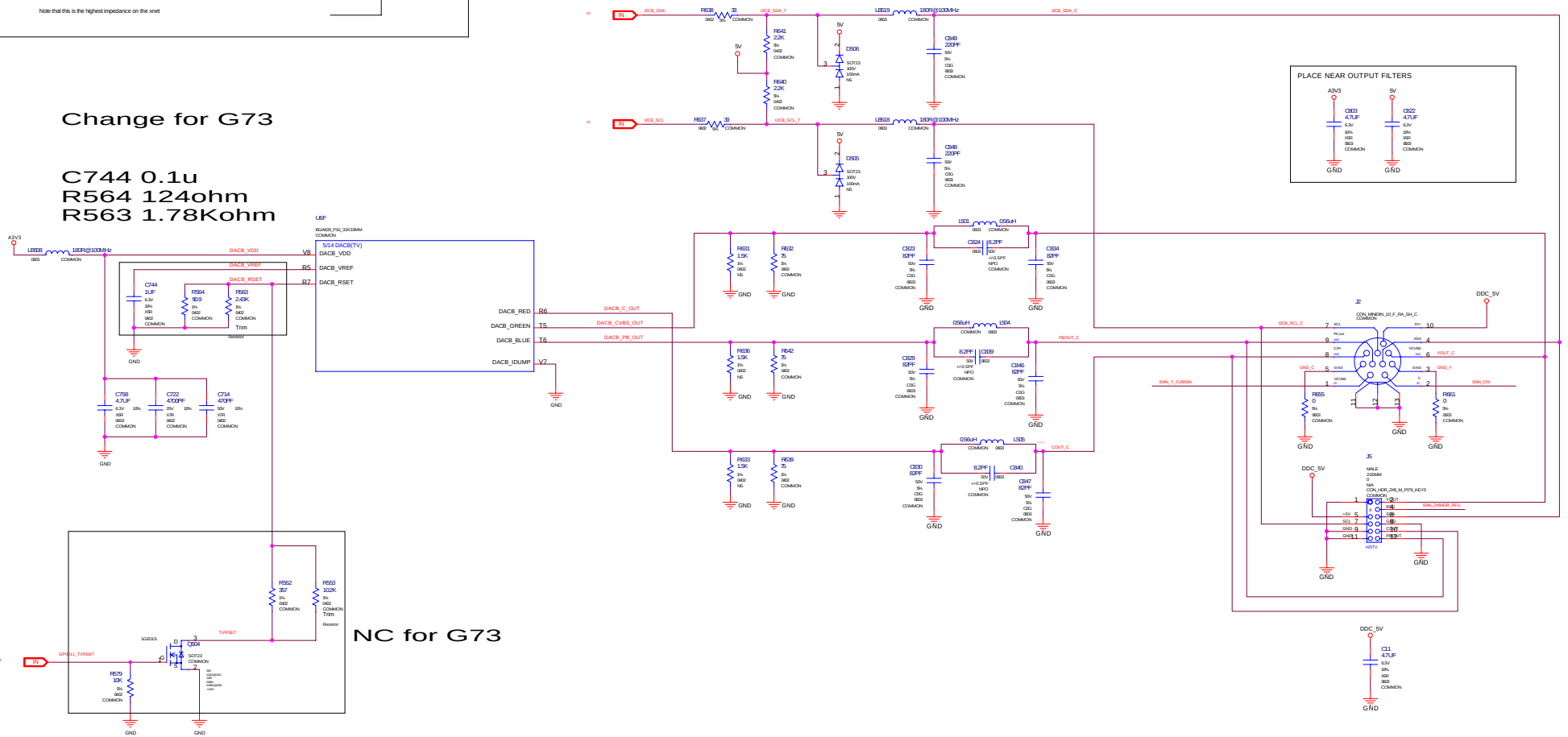
11 DACB - TVOUT, VIDEO IN

NET_NAME	MIN_LINE_WIDTH	NV_CRITICAL_NET	NV_IMPEDANCE
DACB_C_OUT		1	56OHM
DACB_CVBS_OUT		1	56OHM
DACB_PB_OUT		1	56OHM
COUT_C		1	56OHM
YOUT_C		1	56OHM
PBOUT_C		1	56OHM
DACB_VDD	12		
DACB_VREF	12		
DACB_RSET	12		
TVRSET	12		
GND_C	12		
GND_Y	12		

Note that this is the highest impedance on the xnet

Change for G73

C744 0.1u
R564 124ohm
R563 1.78Kohm



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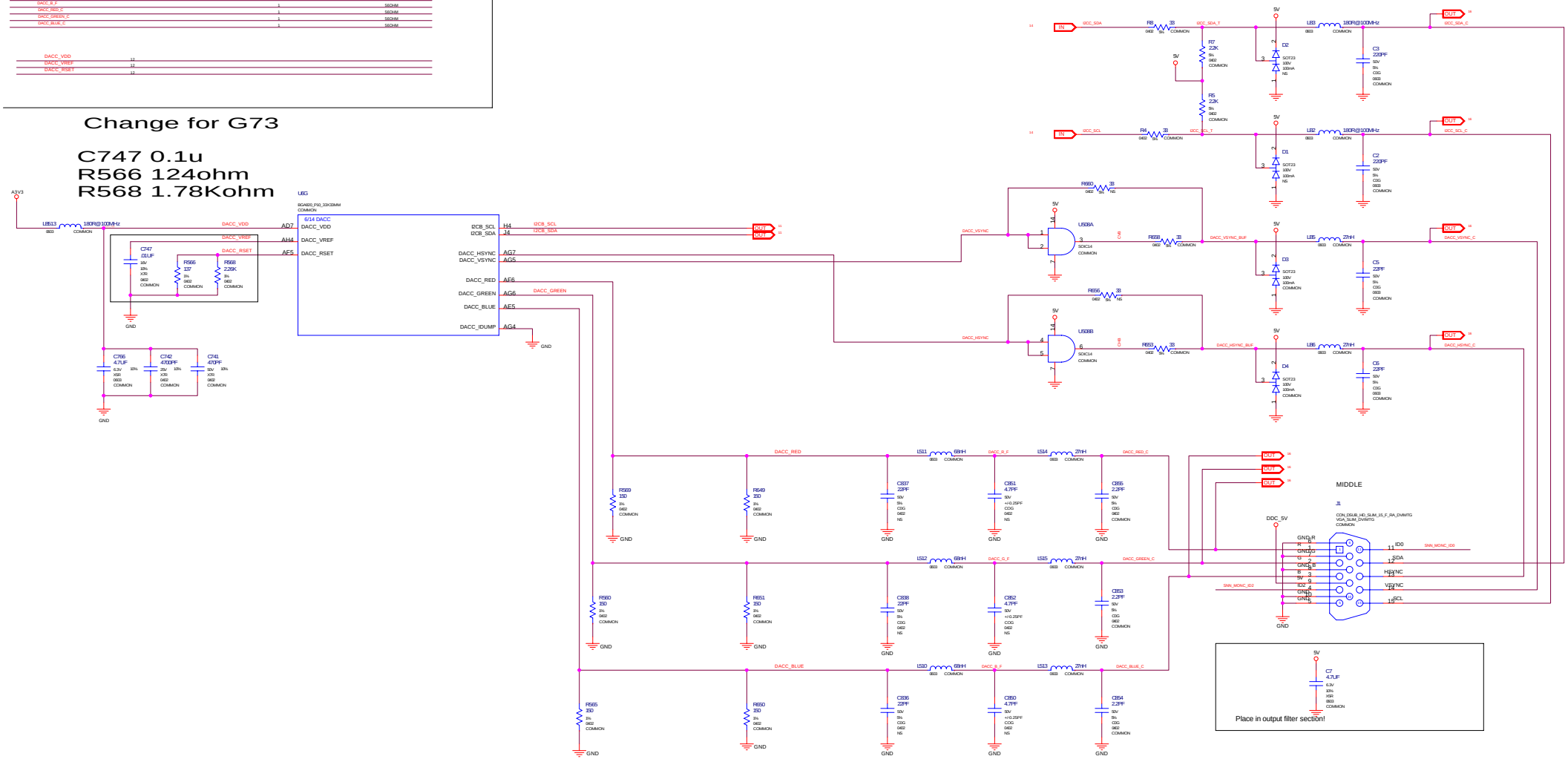
12 DACC - VGA

NET_NAME	MIN_LINE_WIDTH	NET_SPACING_RULE	NV_CRITICAL_NET	NV_IMPEDANCE
I2CB_SCL				
I2CB_SDA				
DACC_HSYNC		2		50OHM
DACC_VSYNC		2		50OHM
DACC_HSYNC_BUF		2		50OHM
DACC_VSYNC_BUF		2		50OHM
DACC_VSYNC_C		2		50OHM
DACC_HSYNC_C		2		50OHM
CHB		2		50OHM
CVB		2		50OHM
DACC_RED		1		50OHM
DACC_GREEN		1		50OHM
DACC_BLUE		1		50OHM
DACC_R_F		1		50OHM
DACC_G_F		1		50OHM
DACC_B_F		1		50OHM
DACC_RED_C		1		50OHM
DACC_GREEN_C		1		50OHM
DACC_BLUE_C		1		50OHM
DACC_VDD		12		
DACC_VREF		12		
DACC_RSET		12		

Change for G73

C747 0.1u
R566 124ohm
R568 1.78Kohm



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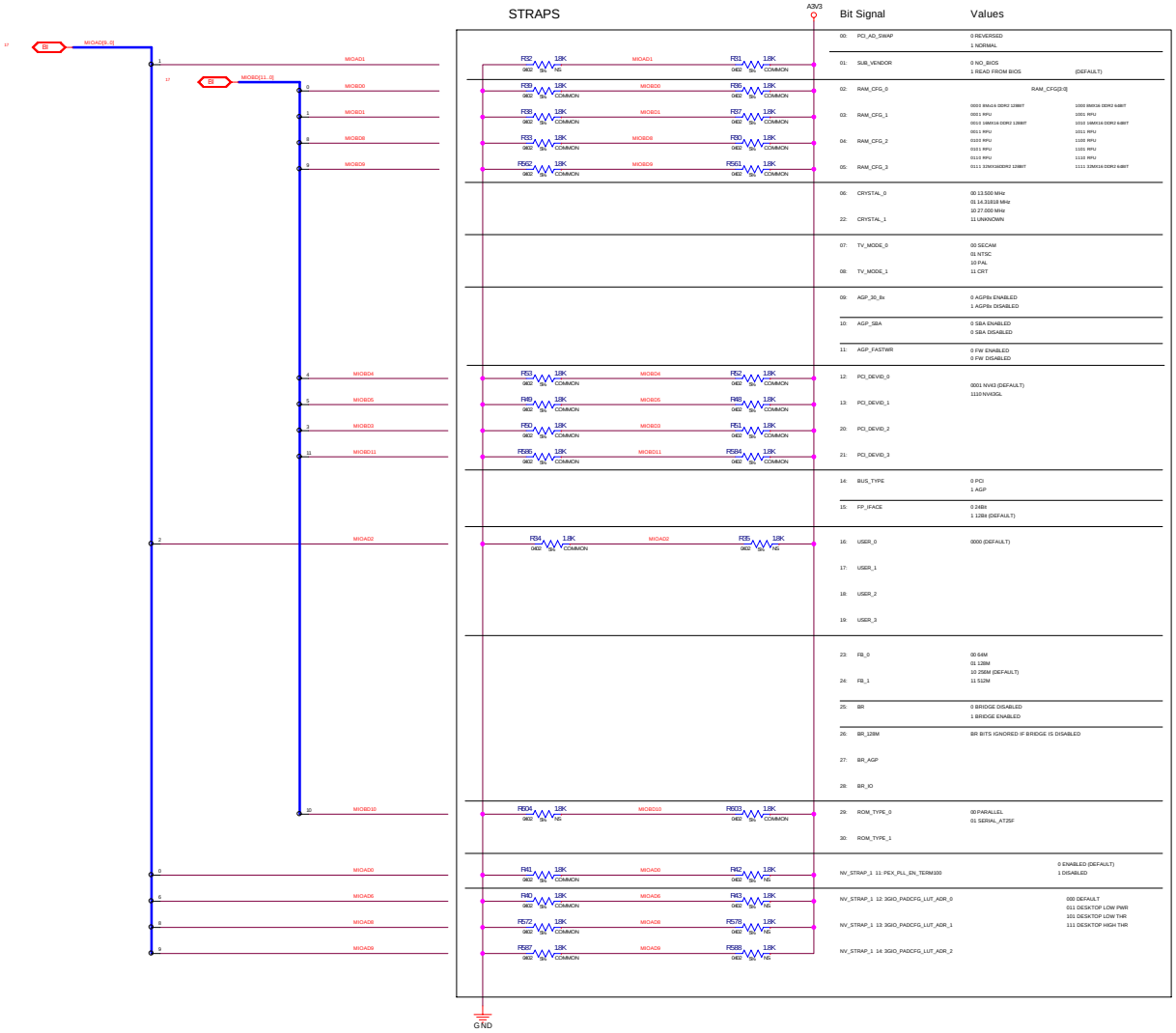
13 STRAPS, FANSINK, MECHANICALS

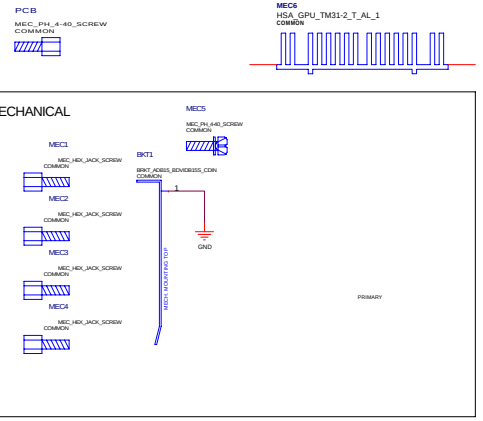
Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground — High logic voltage

Signal





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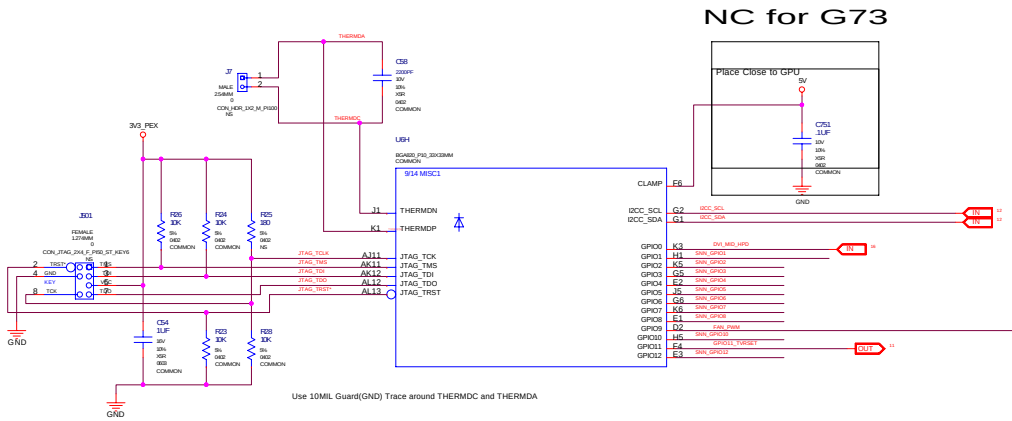
14 GPIO, HDCP, VBIOS, FAN CON

JTAG, GPIO, BIOS ROM

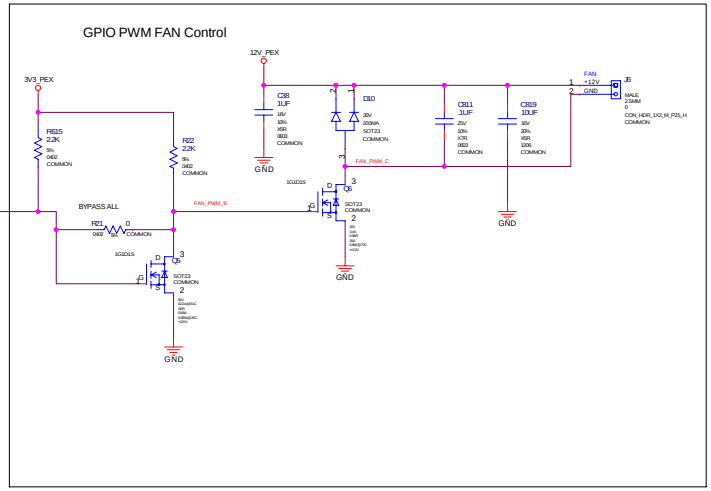


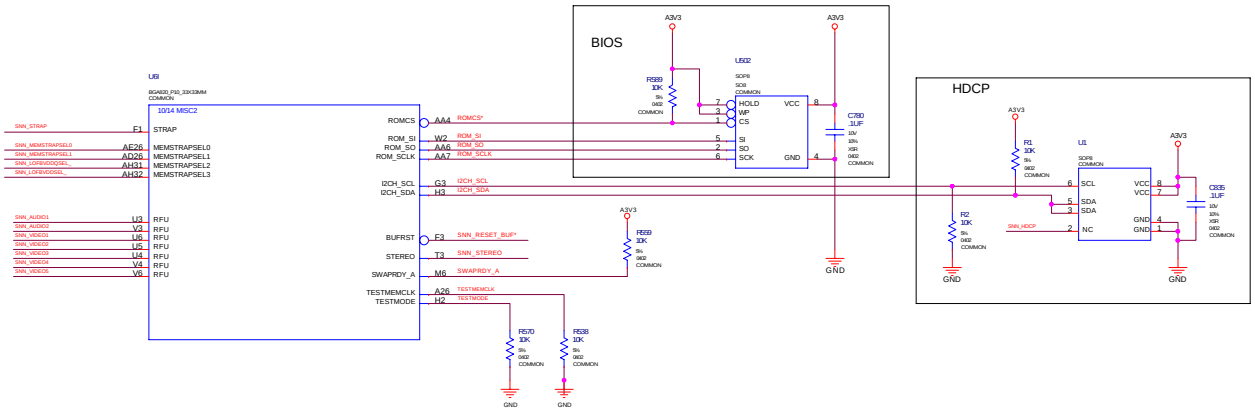
GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	RESERVED
2	IN	RESERVED
3	IN	RESERVED
4	IN	RESERVED
5	IN	RESERVED
6	IN	RESERVED
7	IN	RESERVED
8	IN	THERM ALERT/SLOW
9	OUT	FAN CONTROL
10	IN	RESERVED
11	OUT	HDTV/SDTV SELECT
12	IN	RESERVED

NET MIN_LINE_WIDTH

FAN_THERM_BYPASS 10
FAN_PWM 10
FAN_PWM_B 10
FAN_PWM_C 10
THERMDC 10
THERMDA 10





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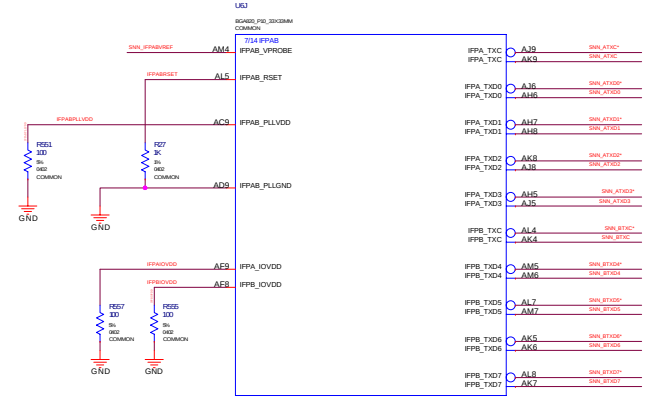
15 INTERNAL TMDS LINK A/B

NET	MIN_LINE_WIDTH
IFPABRSET	12
IFPABPLLVDD	12
IFPAIOVDD	12
IFPBIOVDD	12

INTERNAL TMDS ..LINK A/B



DISABLED

MSI	Micro-Star International Co., LTD.	
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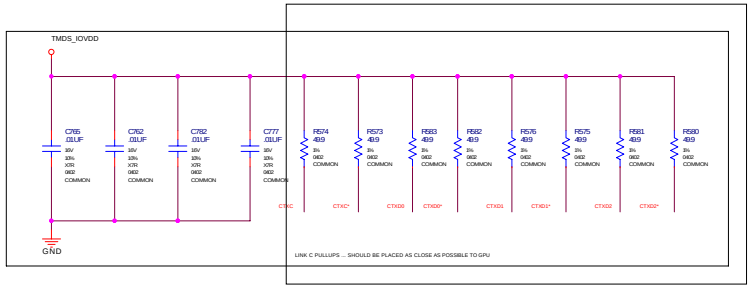
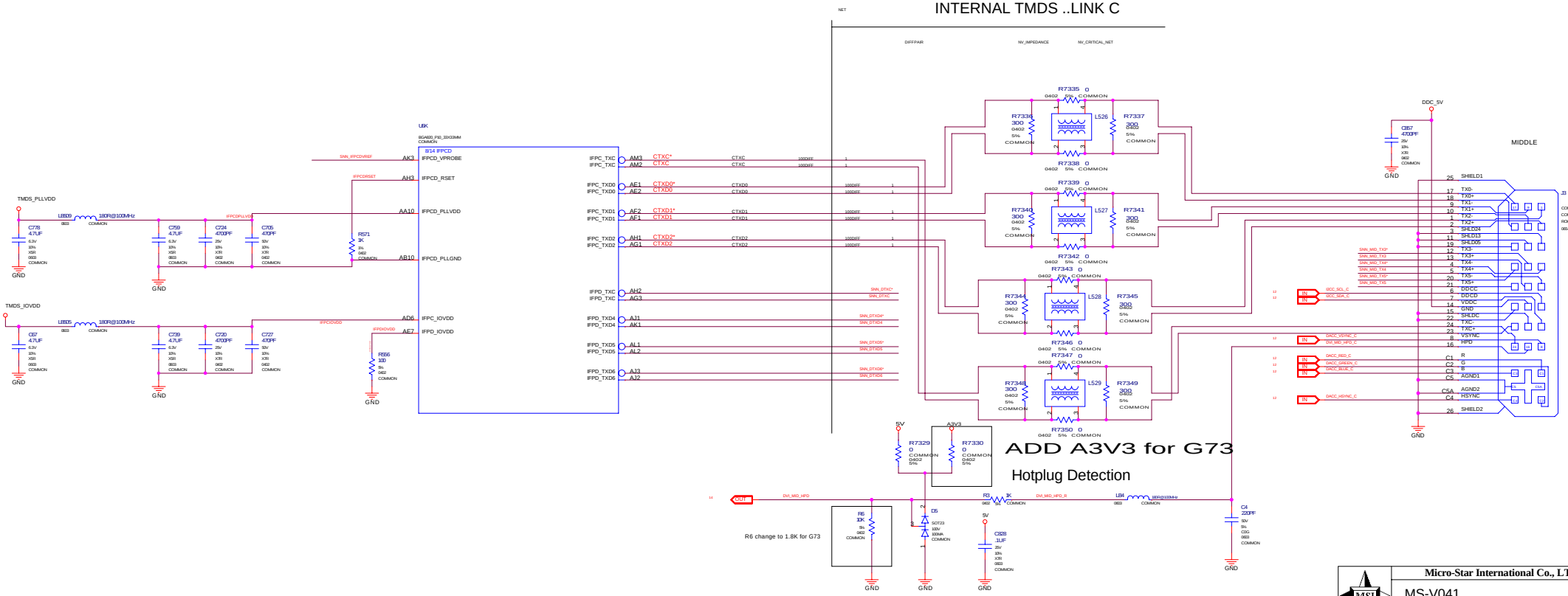
16 INTERNAL TMDS LINK C/D

NC for G73



NET	MIN_LINE_WIDTH	VOLTAGE
IFPCDVREF	12	3.3V
IFPCDPLLVDD	12	3.3V
IFPCIOVDD	12	3.3V
IFPIOVOD	12	3.3V
IFPCDRSET	12	

INTERNAL TMDS ..LINK C



R6 change to 1.8K for G73

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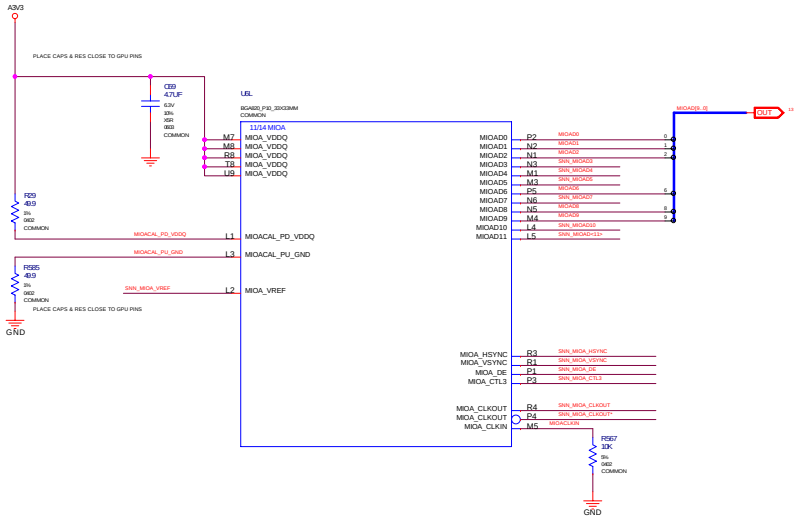
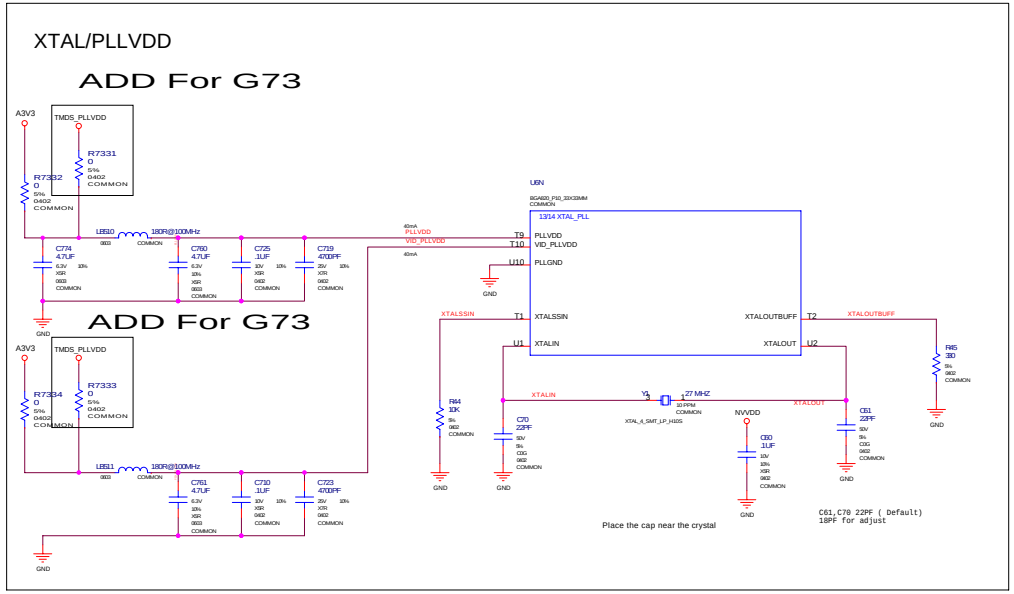
17 MIOA, MIOB, NVPLL

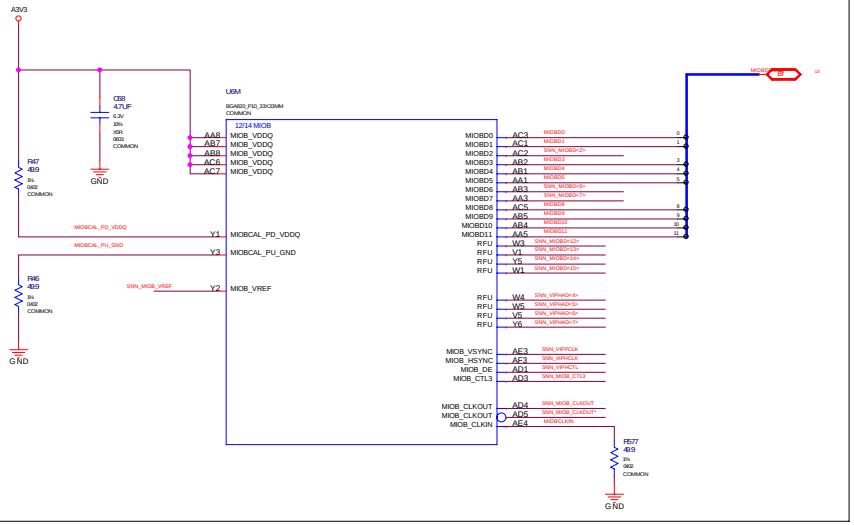
MIOA



XTAL/PLLVDD



MIOB



NET	MIN_LINE_WIDTH
VID_PLLVDD	12
XTALIN	
XTALOUT	
PLLVDD	12

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MS-V041

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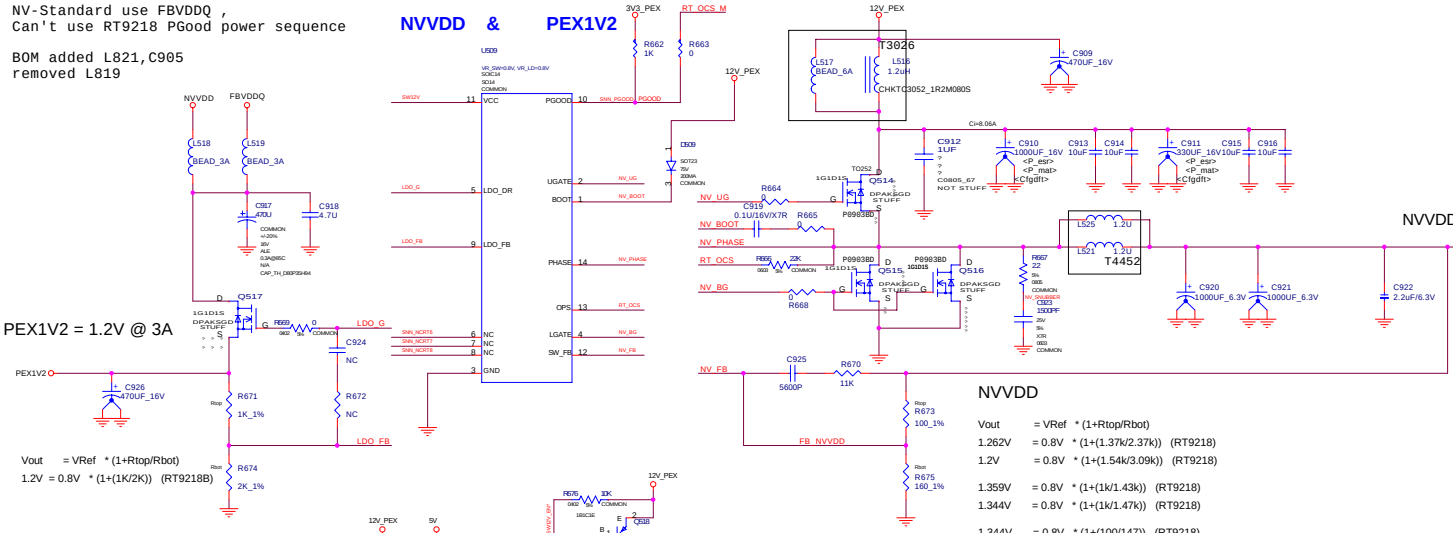
18 Power Supply (RT9218)
NVVDD,PEX1V2,FBVDDQ

NV-Standard use FBVDDQ ,
Can't use RT9218 PGood power sequence

BOM added L821,C905
removed L819

NVVDD & PEX1V2



NVVDD = 1.35V @ upto 18A

1.2V~1.4V/24A(ambient)

NVVDD = 0.8V * (1+Rt/Rb)

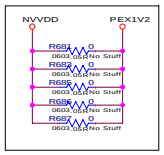
PEX1V2 = 1.2V @ 3A

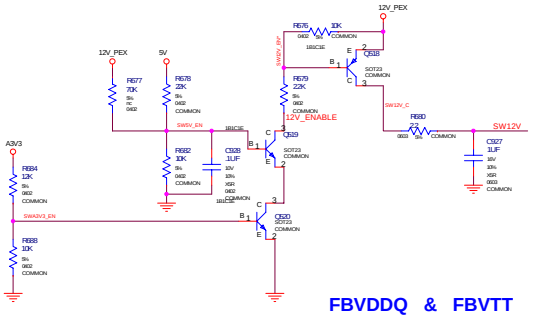
Vout = VRef * (1+Rtop/Rbot)
1.2V = 0.8V * (1+(1K/2K)) (RT9218B)

NVVDD

Vout = VRef * (1+Rtop/Rbot)
1.262V = 0.8V * (1+(1.37k/2.37k)) (RT9218)
1.2V = 0.8V * (1+(1.54k/3.09k)) (RT9218)
1.359V = 0.8V * (1+(1k/1.43k)) (RT9218)
1.344V = 0.8V * (1+(1k/1.47k)) (RT9218)
1.344V = 0.8V * (1+(100/147)) (RT9218)
1.3V = 0.8V * (1+(100/160)) (RT9218) default

1V2 NVVDD bypass



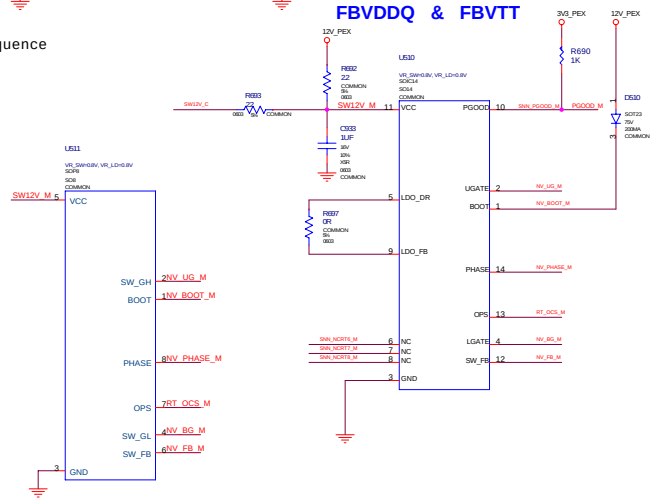


FBVDDQ & FBVTT

Choose RT9218 PGood power sequence

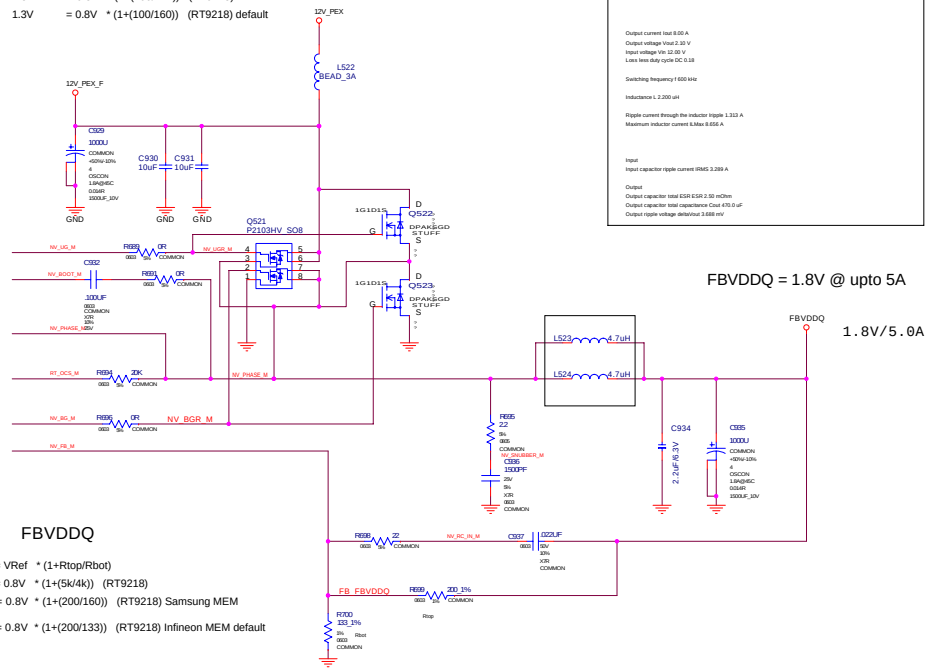
Added BOM R883,R904

Removed R905



FBVDDQ

Vout = VRef * (1+Rtop/Rbot)
1.8V = 0.8V * (1+(5k/4k)) (RT9218)
1.8V = 0.8V * (1+(200/160)) (RT9218) Samsung MEM
2.003V = 0.8V * (1+(200/133)) (RT9218) Infineon MEM default

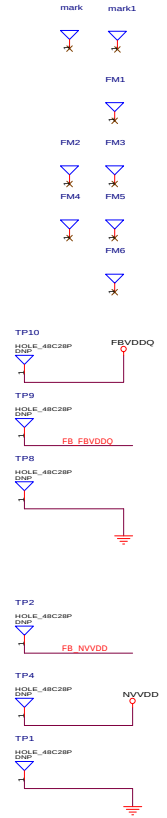


FBVDDQ = 1.8V @ upto 5A

1.8V/5.0A

Net Name	MIN_LINE_WIDTH		VOLTAGE
5V	16	3	5V
NVVDD	16	20	1.35V
12V_PEX	20	6	12V
PEX1V2	20	4	1.2V
12V_PEX_FLTRD	20	6	12V
FBVTT	20	1.5	FBVTT/2 V

DRIVE3_1V2	20	
UGATE_1	20	
LGATE_1	20	
UGATE_2	20	
LGATE_2	20	
NODE_1	20	
NODE_2	20	
12V_RR	10	
ISL12V_VCC	20	
COMP1_NVVDD	10	
FB1_NVVDD	10	
COMP2_5V	10	
FB2_5V	10	
FB3_1V2	10	
REFIN_5V	10	
ISL_REFOUT	10	
VREF_3V3	10	
FB3_RC	10	
BOOT_1	20	
BOOT_2	20	
FREQ_SET	10	
SS_NVVDD	10	
SS_5V	10	
SS_1V2	10	
UGATE_1_RG	20	
UGATE_2_RG	20	
COMP1_RC	10	
COMP2_RC	10	
NVVDD_RC	10	
5V_RC	10	
NODE_1_SNUB	20	
NODE_2_SNUB	20	
CLGATE_1	20	
BOOST	20	
5VBOOST	20	



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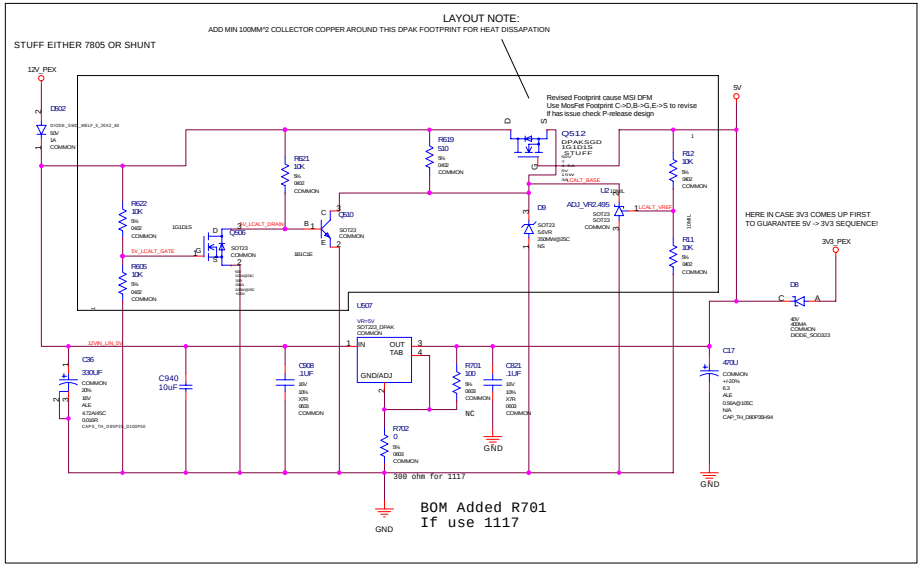
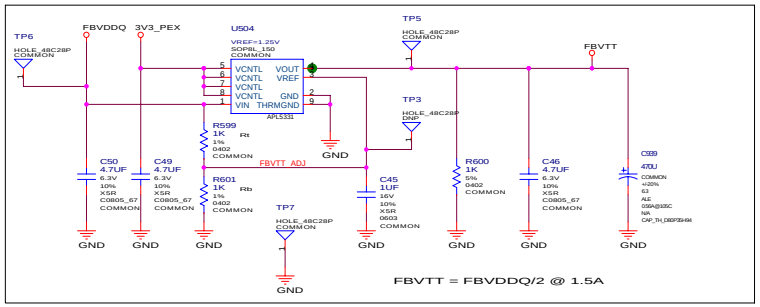
19 Others Power Supply (Linears)
5V,FBVDDQ,A3V3,3V3,TMDS_PLLVDD,TMDS_IOVDD,FBVTT

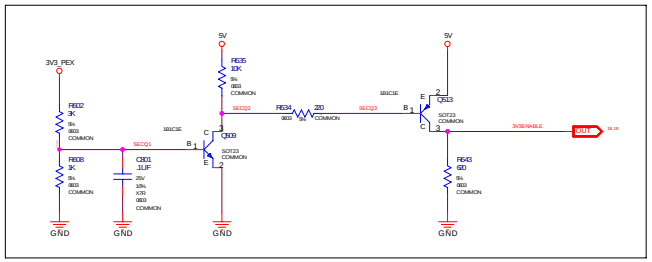
5V LOW COST REGULATOR



FBVTT TERMINATION

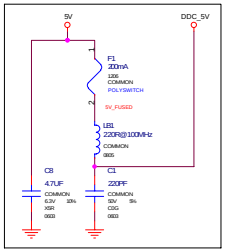


Power Sequencing

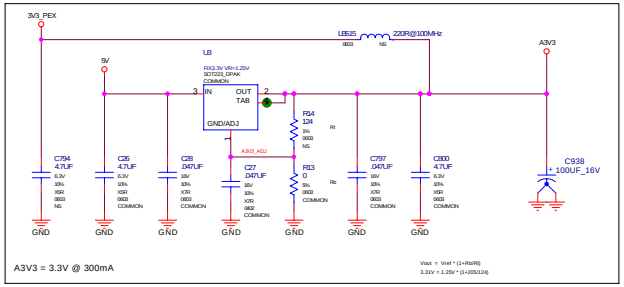


5V AND PEX3V3 UP .. ALL OTHER LINEARS UP

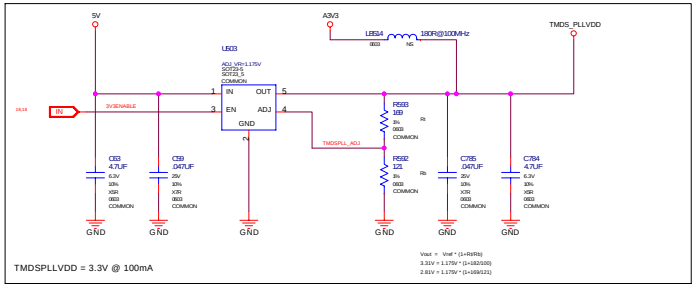
DDC 5V



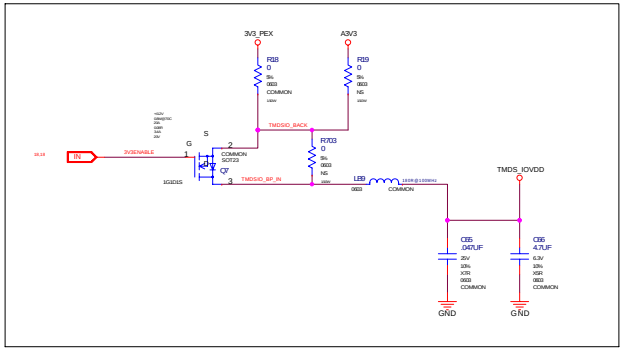
A3V3 Power Supply

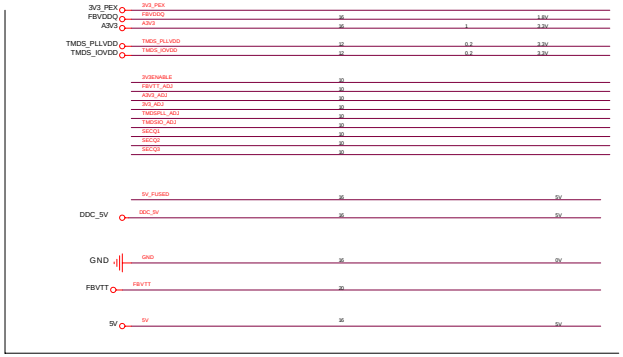


TMDS PLL Supply



TMDS IO SUPPLY WITH BACKDRIVE PROTECTION





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