

G94-P545-A01 - GDDR3, DVI/VGA + DVI/VGA + HDTV/SDTV-Out

REV	VARIANT	NVPIN	ASSEMBLY
B	BASE	600-10545-5860-100	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SRUJ000	600-10545-9100-100	G94-400 600MHz/1000MHz 512MB 18MAJ2 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out (Bring Up SRU)
2	SRU0000	600-10545-6000-100	G94-400 600MHz/1000MHz 512MB 18MAJ2 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out
3	SRU0010	600-10545-6010-100	G94-300 600MHz/800MHz 512MB 18MAJ2 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out
4	SRU0020	600-10545-6020-100	G94-200 600MHz/600MHz 384MB 18MAJ2 BGA136 GDDR3, DVI-I-CL+DVI-I-CL+HDTV-Out
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V127-0A Base on P545

- 1.PAGE18: ADD Display port circuit  
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V127-20 Base on V127-0A

- 1.PAGE30 .CO-LAYOUT RT9258 circuit

V127-0C Base on V127-20

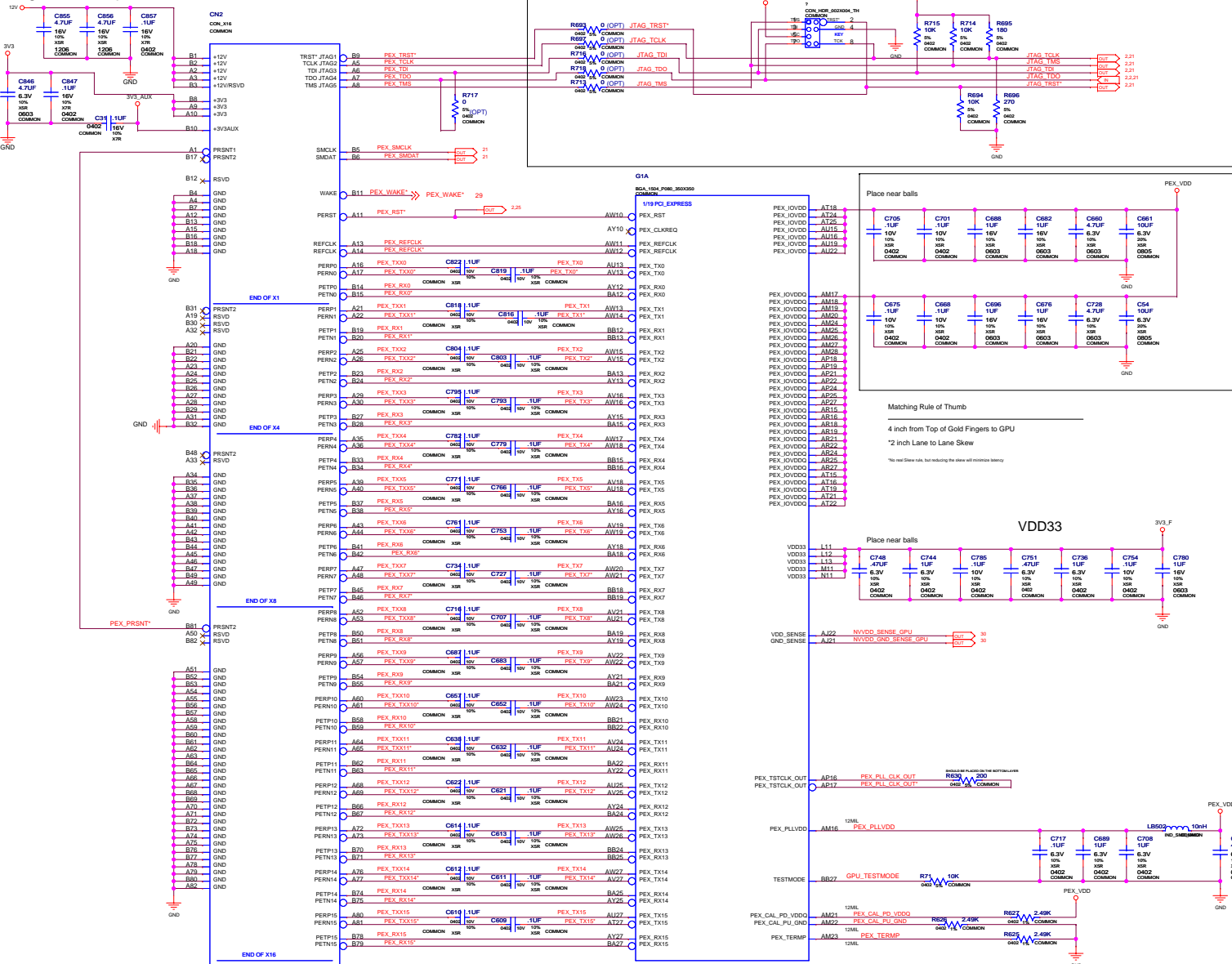
- 1.PAGE18 remove Display port co-lay circuit  
2.PAGE32 remove MEC8

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ASSEMBLY  
PAGE DETAIL

P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL  
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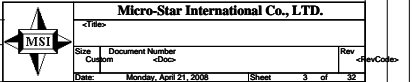
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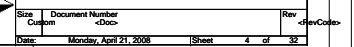
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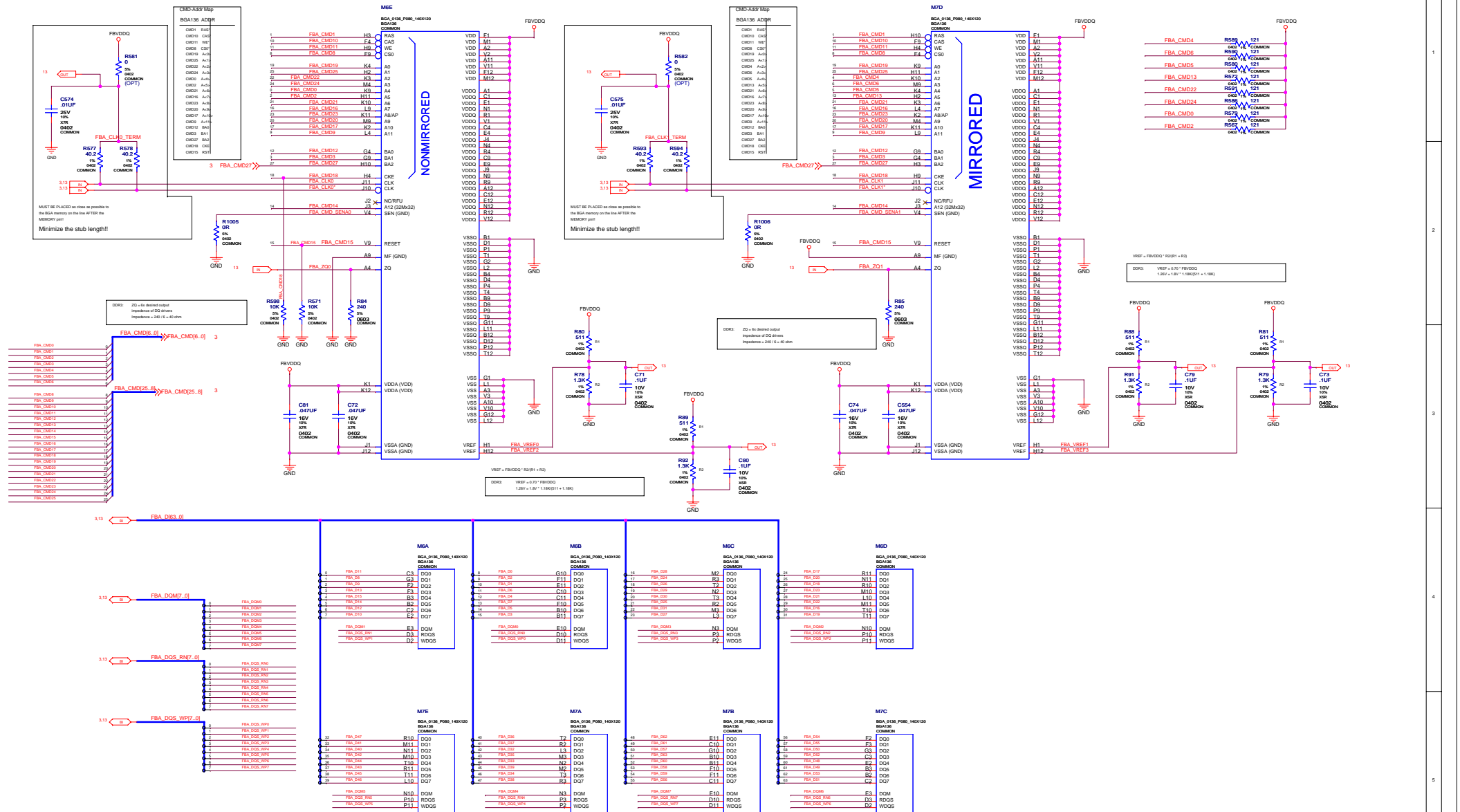
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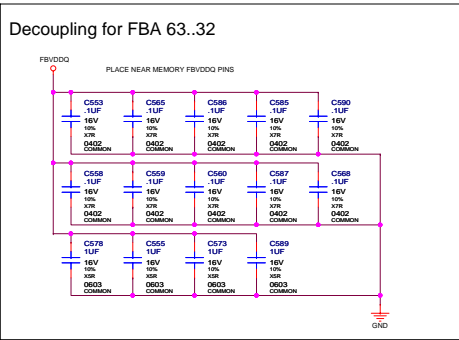
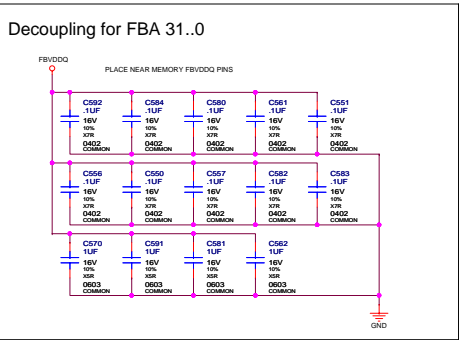
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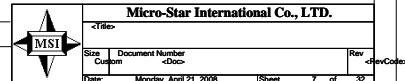
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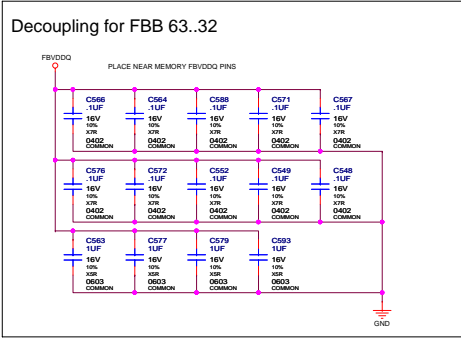
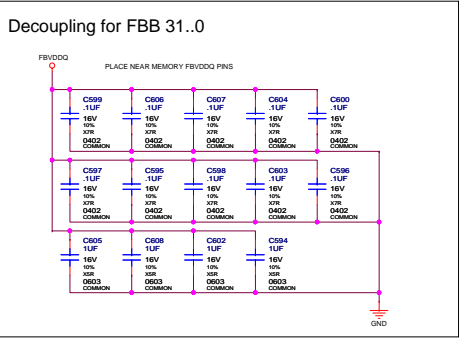
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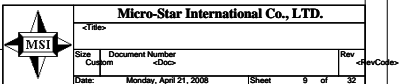
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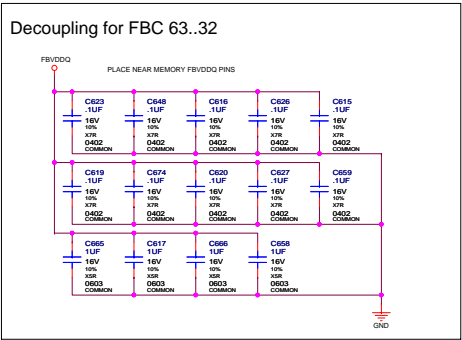
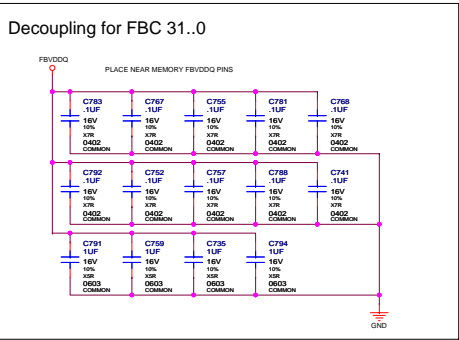


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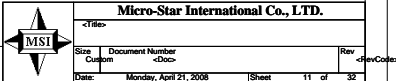
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FBC Partition Decoupling

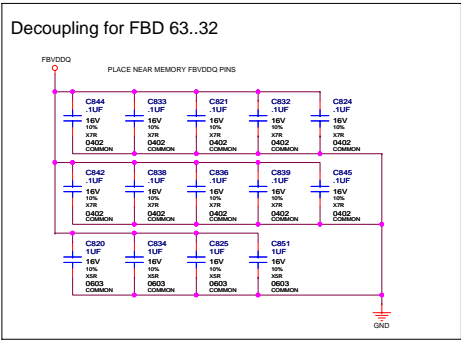
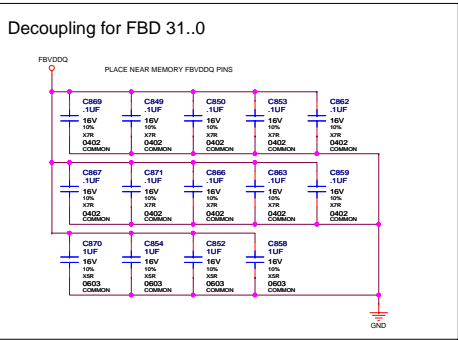


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PAGE DETAIL	FBD Partition



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FBD Partition Decoupling



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NET RULES for FBA and FBB

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
3.5	FBA_CLK0	1	RIGHT FBA_CLK0
3.5	FBB_CLK0P	1	RIGHT FBA_CLK0
3.5	FBA_CLK0_TERM	1	RIGHT FBA_CLK0
3.5	FBA_CLK1	1	RIGHT FBA_CLK1
3.5	FBB_CLK1P	1	RIGHT FBA_CLK1
3.5	FBA_CLK1_TERM	1	RIGHT FBA_CLK1

NET	NV_CRITICAL_NET	IMPEDANCE
3.5	FBA_DQS_WRP0_0	1
3.5	FBB_DQS_WRP0_0	1
3.5	FBA_DQS_WRP0_1	1
3.5	FBB_DQS_WRP0_1	1
3.5	FBA_DQS_WRP0_2	1
3.5	FBB_DQS_WRP0_2	1

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
3.7	FBA_CLK0	1	RIGHT FBA_CLK0
3.7	FBB_CLK0P	1	RIGHT FBA_CLK0
3.7	FBA_CLK0_TERM	1	RIGHT FBA_CLK0
3.7	FBA_CLK1	1	RIGHT FBA_CLK1
3.7	FBB_CLK1P	1	RIGHT FBA_CLK1
3.7	FBA_CLK1_TERM	1	RIGHT FBA_CLK1

NET	NV_CRITICAL_NET	IMPEDANCE
3.7	FBA_DQS_WRP0_0	1
3.7	FBB_DQS_WRP0_0	1
3.7	FBA_DQS_WRP0_1	1
3.7	FBB_DQS_WRP0_1	1
3.7	FBA_DQS_WRP0_2	1
3.7	FBB_DQS_WRP0_2	1

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
3	FB_PLAVDD0	1.1V	0.05A
3	FB_VREF	1.20V	0.02A
5	FBA_VREF0	1.20V	0.02A
5	FBB_VREF0P	1.20V	0.02A
5	FBA_VREF2	1.20V	0.02A
5	FBB_VREF2P	1.20V	0.02A
5	FBA_VREF5	1.20V	0.02A
5	FBB_VREF5P	1.20V	0.02A
5	FBA_200	1.20V	0.02A
5	FBB_200	1.20V	0.02A
7	FBA_VREF0	1.20V	0.02A
7	FBB_VREF0P	1.20V	0.02A
7	FBA_VREF2	1.20V	0.02A
7	FBB_VREF2P	1.20V	0.02A
7	FBA_VREF5	1.20V	0.02A
7	FBB_VREF5P	1.20V	0.02A
7	FBA_200	1.20V	0.02A
7	FBB_200	1.20V	0.02A

NET RULES for FBC and FBD

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
4.9	FBC_CLK0	1	RIGHT FBC_CLK0
4.9	FBD_CLK0P	1	RIGHT FBC_CLK0
4.9	FBC_CLK0_TERM	1	RIGHT FBC_CLK0
4.9	FBC_CLK1	1	RIGHT FBC_CLK1
4.9	FBD_CLK1P	1	RIGHT FBC_CLK1
4.9	FBC_CLK1_TERM	1	RIGHT FBC_CLK1

NET	NV_CRITICAL_NET	IMPEDANCE
4.9	FBC_DQS_WRP0_0	1
4.9	FBD_DQS_WRP0_0	1
4.9	FBC_DQS_WRP0_1	1
4.9	FBD_DQS_WRP0_1	1
4.9	FBC_DQS_WRP0_2	1
4.9	FBD_DQS_WRP0_2	1

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
4.11	FBC_CLK0	1	RIGHT FBC_CLK0
4.11	FBD_CLK0P	1	RIGHT FBC_CLK0
4.11	FBC_CLK0_TERM	1	RIGHT FBC_CLK0
3.7	FBC_CLK1	1	RIGHT FBC_CLK1
3.7	FBD_CLK1P	1	RIGHT FBC_CLK1
3.7	FBC_CLK1_TERM	1	RIGHT FBC_CLK1

NET	NV_CRITICAL_NET	IMPEDANCE
4.11	FBC_DQS_WRP0_0	1
4.11	FBD_DQS_WRP0_0	1
4.11	FBC_DQS_WRP0_1	1
4.11	FBD_DQS_WRP0_1	1
4.11	FBC_DQS_WRP0_2	1
4.11	FBD_DQS_WRP0_2	1

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
4	FB_PLAVDD0	1.1V	0.05A
9	FBC_VREF0	1.20V	0.02A
9	FBD_VREF0P	1.20V	0.02A
9	FBC_VREF2	1.20V	0.02A
9	FBD_VREF2P	1.20V	0.02A
9	FBC_VREF5	1.20V	0.02A
9	FBD_VREF5P	1.20V	0.02A
9	FBC_200	1.20V	0.02A
9	FBD_200	1.20V	0.02A
11	FBC_VREF0	1.20V	0.02A
11	FBD_VREF0P	1.20V	0.02A
11	FBC_VREF2	1.20V	0.02A
11	FBD_VREF2P	1.20V	0.02A
11	FBC_VREF5	1.20V	0.02A
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11	FBC_200	1.20V	0.02A
11	FBD_200	1.20V	0.02A

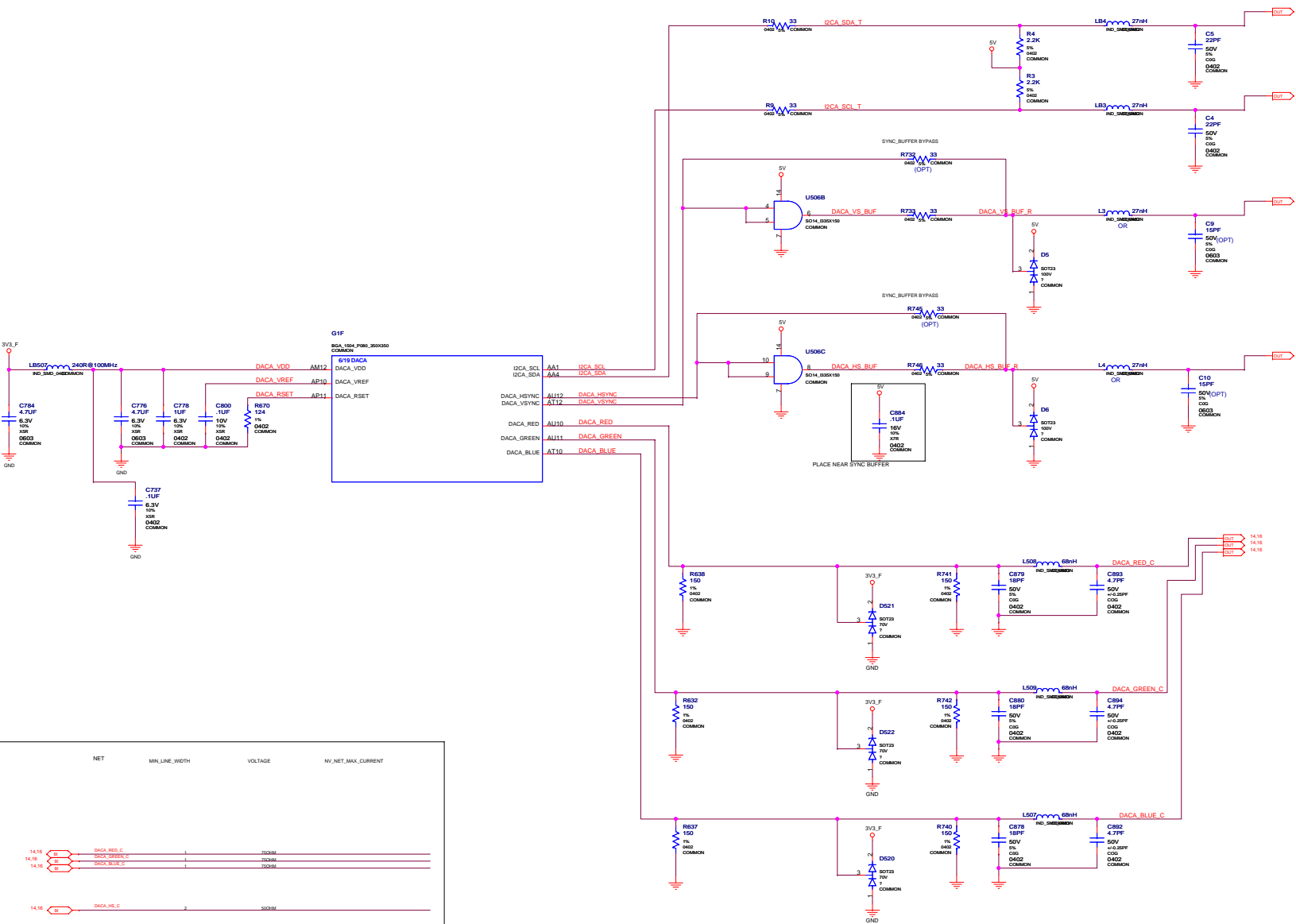
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ASSEMBLY PAGE DETAIL PCB BOARD LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO 3D/PCF ASSEMBLY NOTES AND BOARD NOT FINAL FB Net Properties



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DACA RGB-FILTER



NET	MIN_LINE_WIDTH	VOLTAGE	WIRE_MAX_CURRENT
14,16	1	3.3V	1.0000A
14,15	1	3.3V	1.0000A
14,14	1	3.3V	1.0000A
14,16	2	3.3V	1.0000A
14,15	2	3.3V	1.0000A
14,14	2	3.3V	1.0000A

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ASSEMBLY	PER BOARD LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO 3V3_F; ASSEMBLY NOTES AND BOARD FINAL
PAGE DETAIL	DACA Interface



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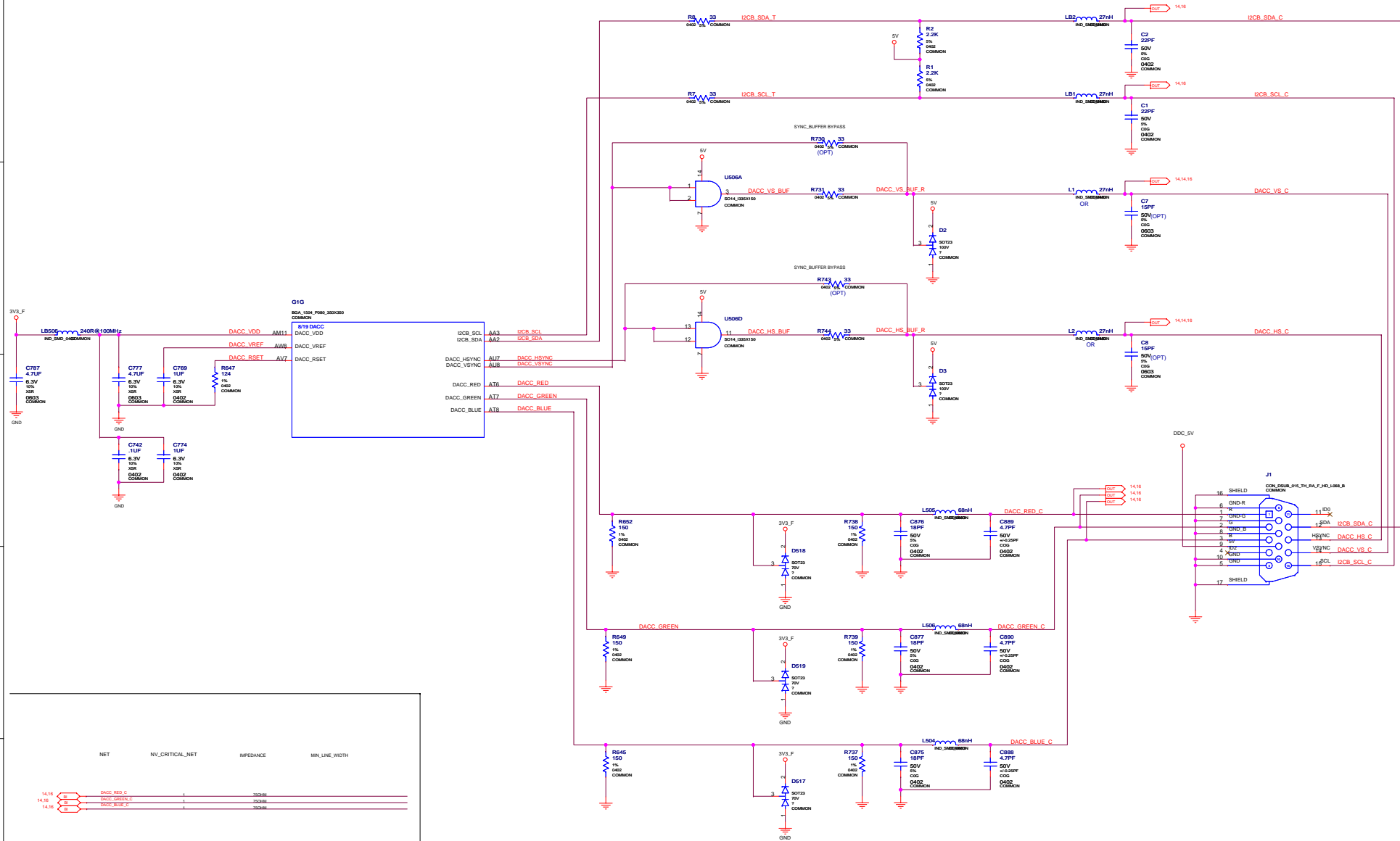
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DACC RGB-FILTER



Timing diagram for NV\_CRITICAL\_NET. The diagram shows three data bus transactions. The signals are labeled with their respective values and the bus width (e.g., 16B, 32B, 64B).

Signal	Value	Bus Width
NET	1	16B
NV_CRITICAL_NET	1	16B
IMPEDANCE	1	32B
MIN_LINE_WIDTH	1	64B
NET	2	32B
NV_CRITICAL_NET	2	32B
IMPEDANCE	2	64B
MIN_LINE_WIDTH	2	128B
NET	3	64B
NV_CRITICAL_NET	3	64B
IMPEDANCE	3	128B
MIN_LINE_WIDTH	3	256B

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PAGE DETAIL	DACC Interface



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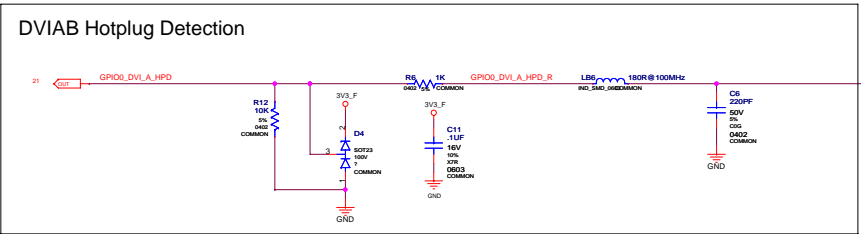
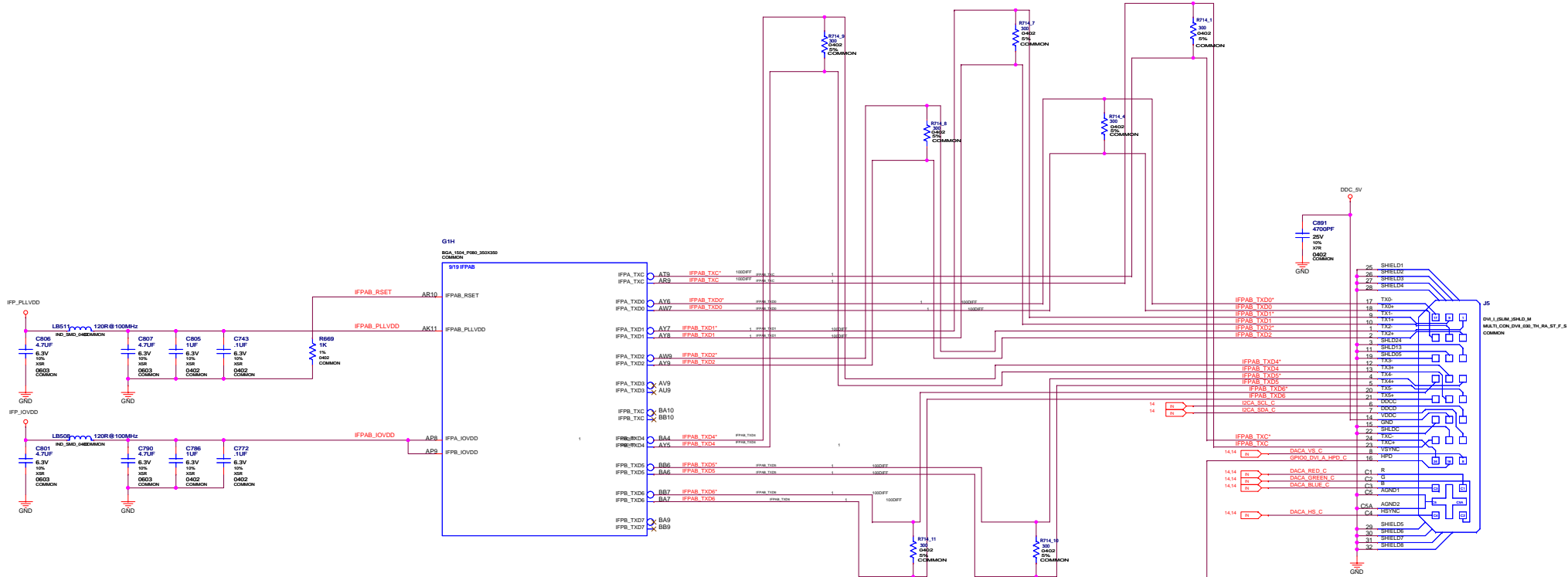
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ASSEMBLY PAGE DETAIL  
IFP A/B Interface -- DVI Connector South



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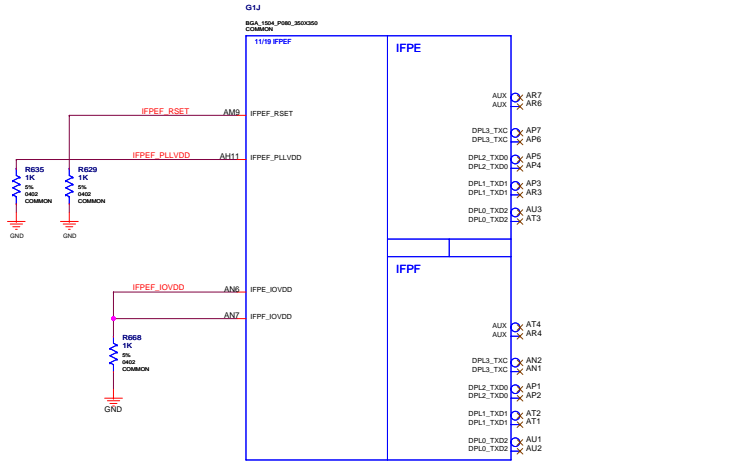
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Page18: IFP E/F Interface -- Unused  
TMDS E : Display Port



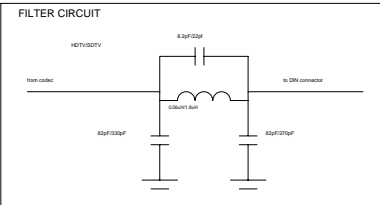
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ASSEMBLY PAGE DETAIL  
IFP E/F Interface -- Unused



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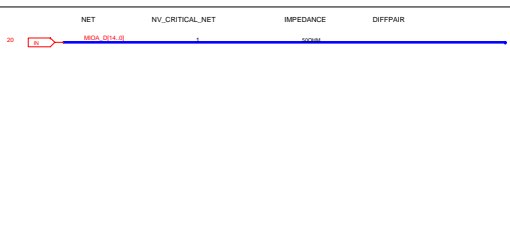
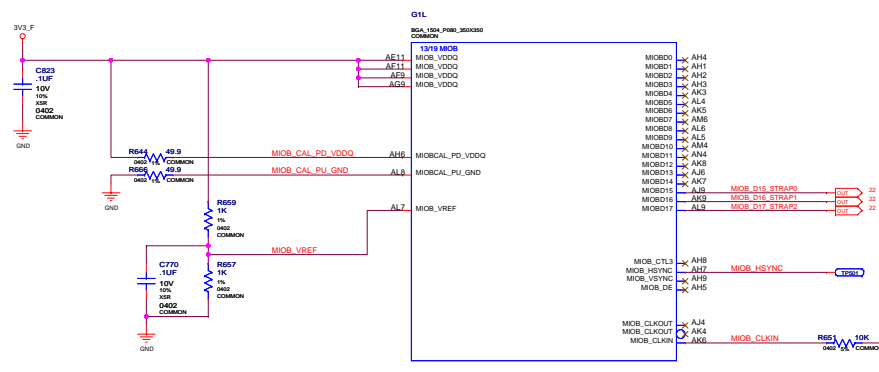
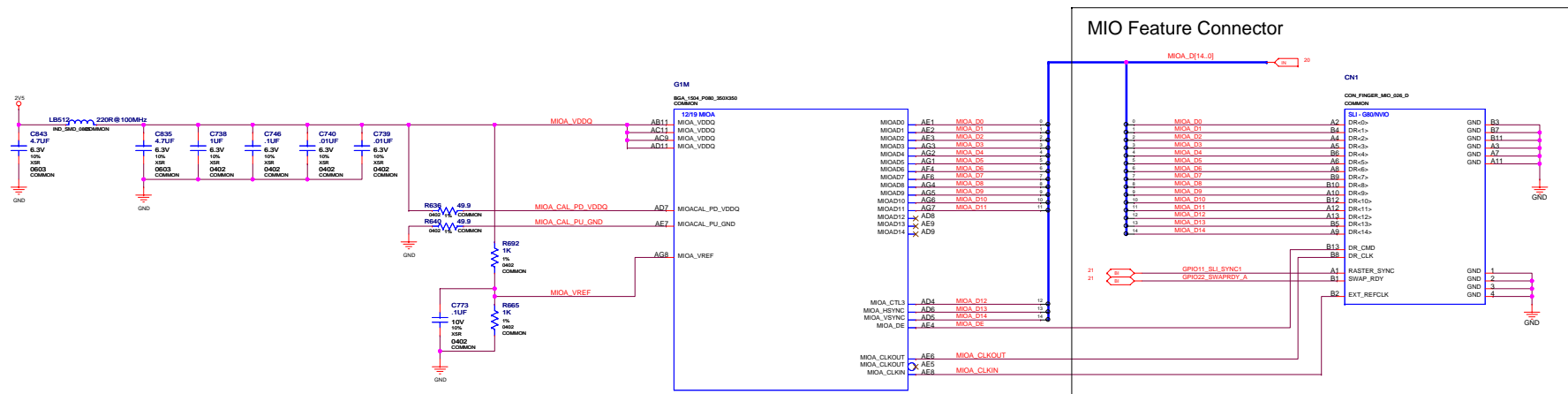
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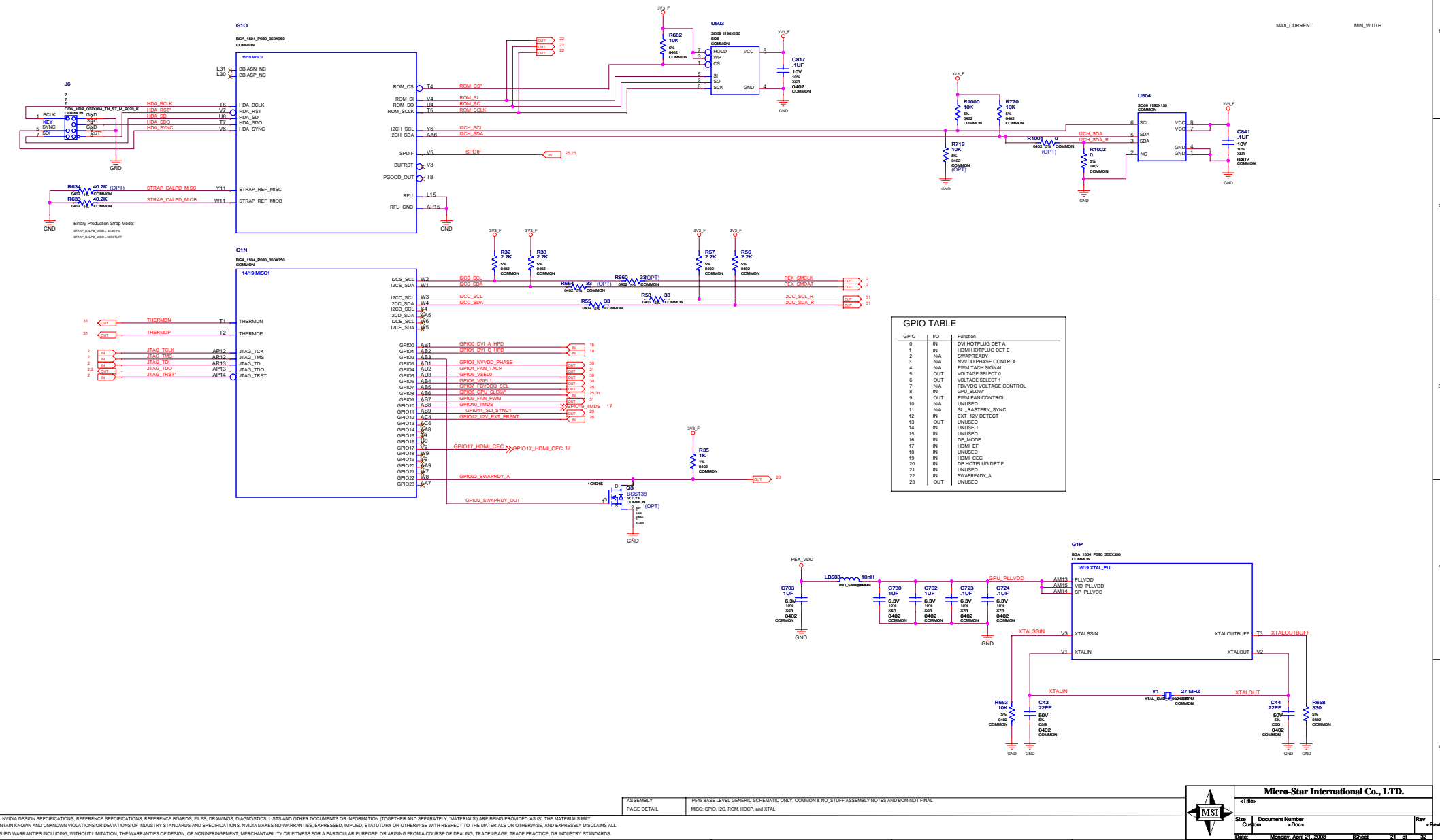


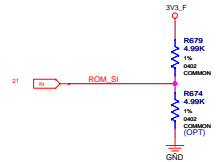
ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB and HDTV/SDTV-Out



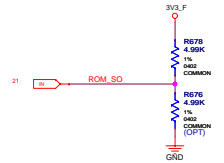
Rev	Rev Code
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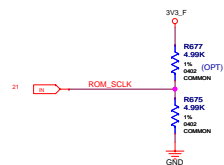




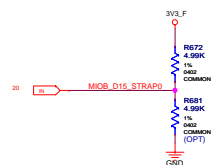
STRAP PIN	STRAP NAME
ROM_SI	PCI_DEVID_EXT



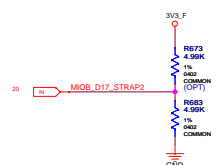
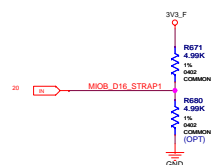
STRAP PIN	STRAP NAME
ROM_SO	SLOT_CLK_CFG



STRAP PIN	STRAP NAME
ROM_SCLK	PCI_DEVID[3]

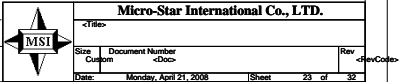


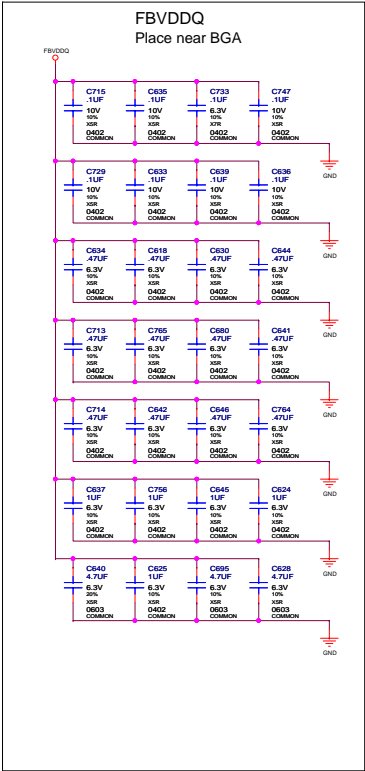
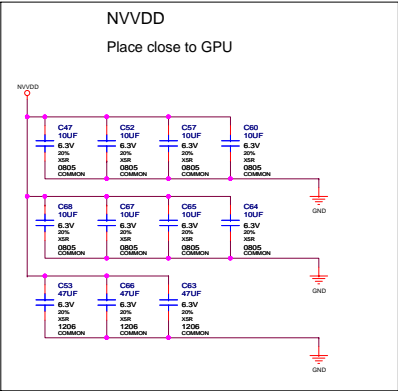
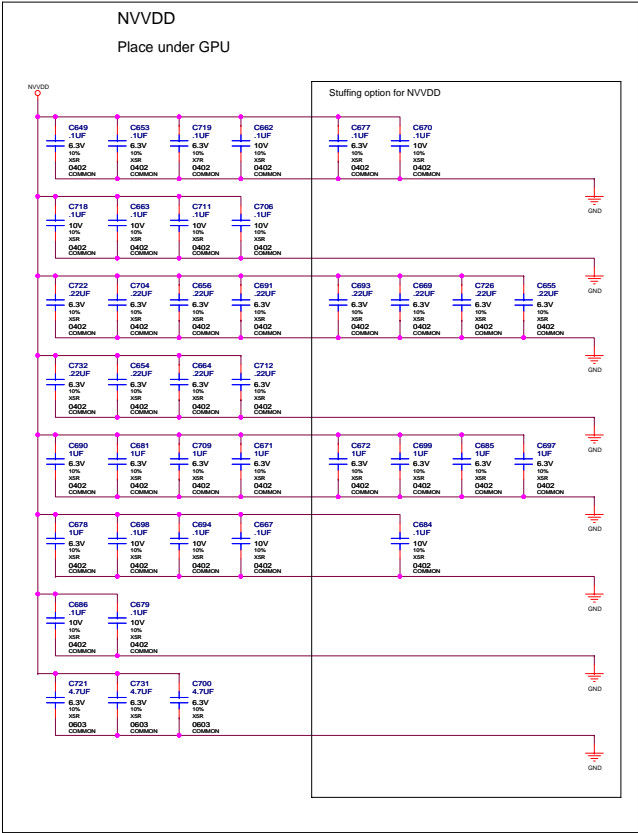
STRAP PIN	STRAP NAME
STRAP0	RAMCFG0
STRAP PIN	STRAP NAME
STRAP1	RAMCFG1
<div>* RAMCFG[2:0]</div> <div>256MB (8Mx32)</div> <div>101 --- 256-bit Qimonda 110 --- 256-bit Hynix 111 --- 256-bit Samsung</div> <div>512MB (16Mx32)</div> <div>001 --- 256-bit Qimonda 010 --- 256-bit Hynix 011 --- 256-bit Samsung</div> <div>1024MB (32Mx32)</div> <div>101 --- 256-bit Hynix 110 --- 256-bit Hynix 111 --- 256-bit Samsung</div> <div>* VBIOS will be defined on a per SKU basis.</div>	
STRAP PIN	STRAP NAME
STRAP2	RAMCFG2



3V3		GND	
5K	1	0	

GIQ	
BQ4_1004_P001_20100205	
COMMON	
ACM4	NC
ACM5	NC
ACM6	NC
AF36	NC
AF37	NC
AF38	NC
AF39	NC
AG53	NC
AG54	NC
AG55	NC
AG56	NC
AG57	NC
AL32	NC
AM50	NC
AM51	NC
AM52	NC
AM53	NC
AM54	NC
AM55	NC
AM56	NC
AR36	NC
AT19	NC
AT20	NC
AT21	NC
AU15	NC
AU17	NC
AU20	NC
AU21	NC
AU22	NC
AV15	NC
AV16	NC
AV17	NC
AV18	NC
E10	NC
E11	NC
E12	NC
F10	NC
F11	NC
F12	NC
F13	NC
F14	NC
G10	NC
G11	NC
G12	NC
G13	NC
G14	NC
G15	NC
G16	NC
G17	NC
H10	NC
H11	NC
J06	NC
J07	NC
J08	NC
L06	NC
L07	NC
L08	NC
L09	NC
M06	NC
M07	NC
P06	NC
P07	NC
P08	NC
R10	NC
R11	NC
R12	NC
T10	NC
T11	NC
U06	NC
U07	NC
Y06	NC
Y07	NC
Y08	NC





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ASSEMBLY PAGE DETAIL PCB LAYER LEVEL: GENERIC SCHEMATIC ONLY; COMMON & NO. 3(CPU) ASSEMBLY NOTES AND BOARD FINAL NVVDD and FBVDDQ Decoupling



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Date: Monday, April 21, 2008

Document Number

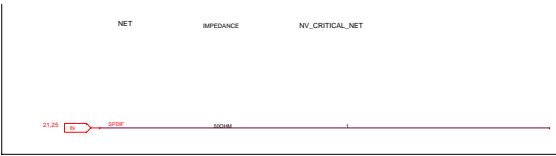
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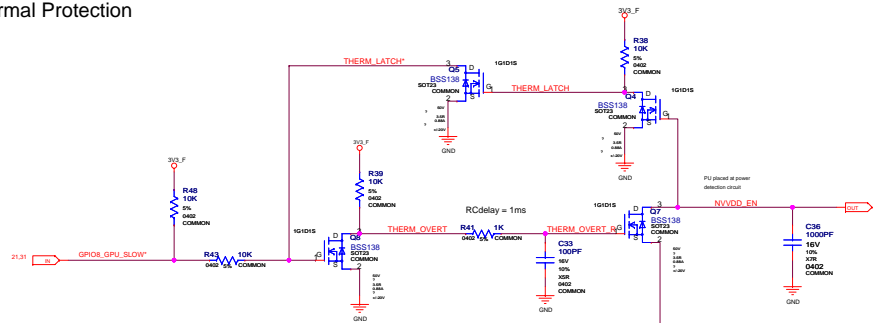
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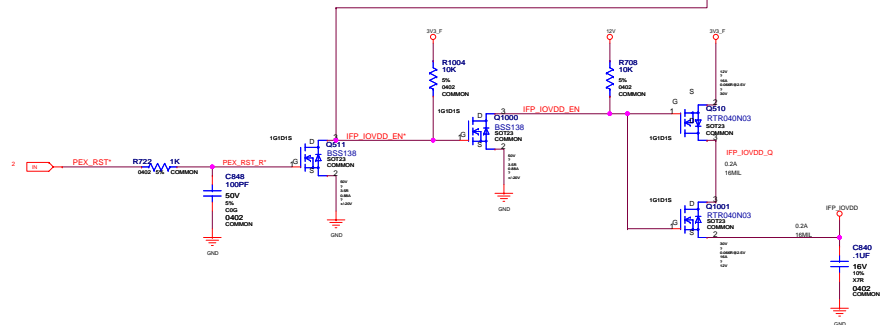


## Thermal Protection

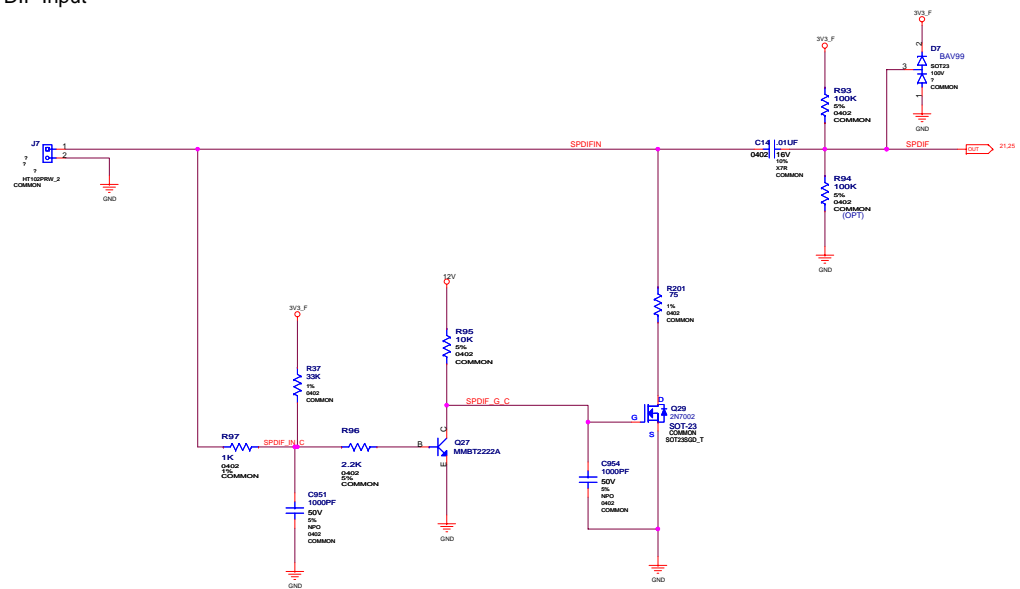


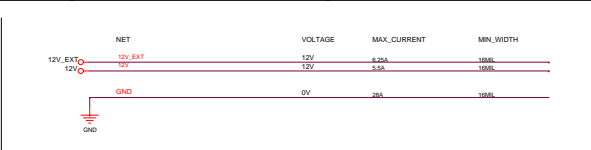
## IFP\_IOVDD Backdrive Prevention

#### Stuffing possibilities for thermal control and protection:



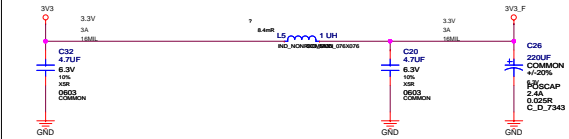
## SPDIF Input





### 3V3 Power Supply Filter

3V3\_F = 3.3V @ 2.5A



### 12V Power Supply Filter

12V\_F = 12V @ 5.5A

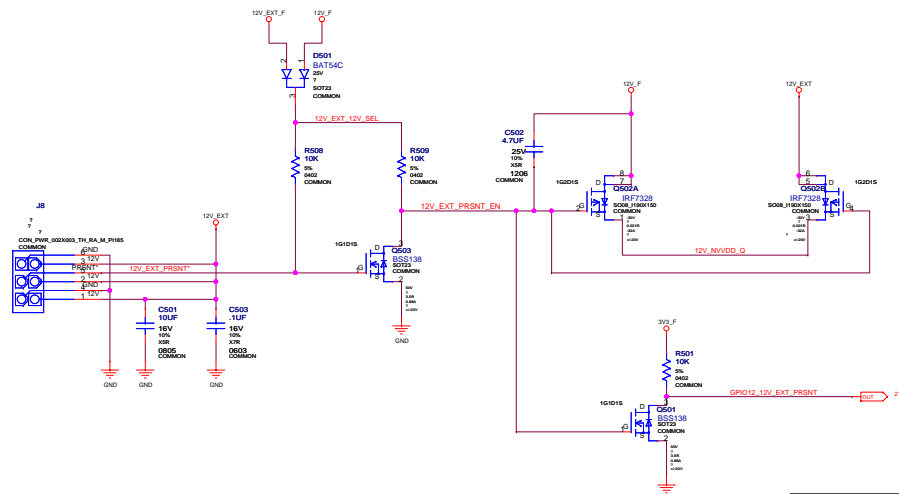


### 12V\_EXT Power Supply Filter

12V\_EXT\_F = 12V @ 6.25A



### INPUT POWER SELECTION for NVVDD

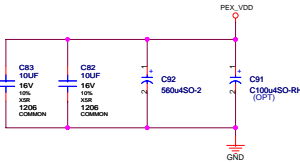


GPIO12	
EMERGENCY MODE (12V_EXT present)	0
1500W POWER MODE (12V_EXT NOT present)	1



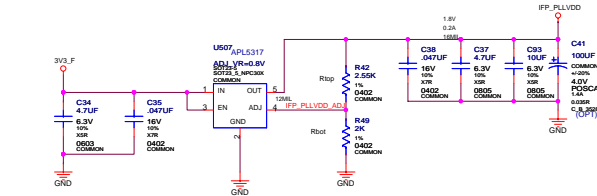
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### IFP\_PLLVDD Power Supply

IFP\_PLLVDD = 1.8V @ 200mA

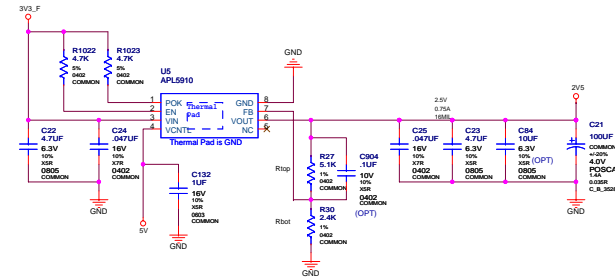
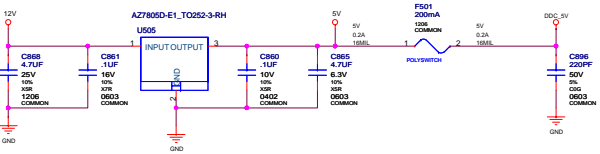


$$IFP\_PLLVD = VREF * (1 + (Rtop / Rbot))$$
$$1.82V = 0.8V * (1 + (2.5K/2K))$$

### 5V and DDC\_5V Power Supply

DDC\_5V = 5V @ 200mA

LAYOUT NOTE: ADD MIN 200MM<sup>2</sup> COPPER AROUND THIS DPAK FOR HEAT DISSIPATION

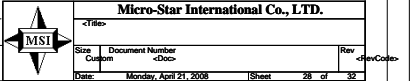


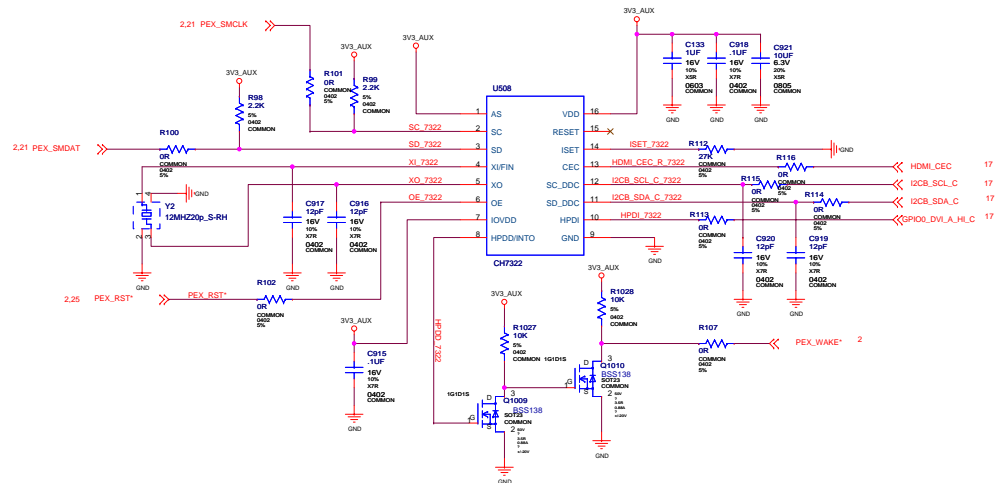
$$2V5 = VREF * (1 + (Rtop / Rbot))$$
$$2.5V = 0.8V * (1 + (5.1K/2.4K))$$

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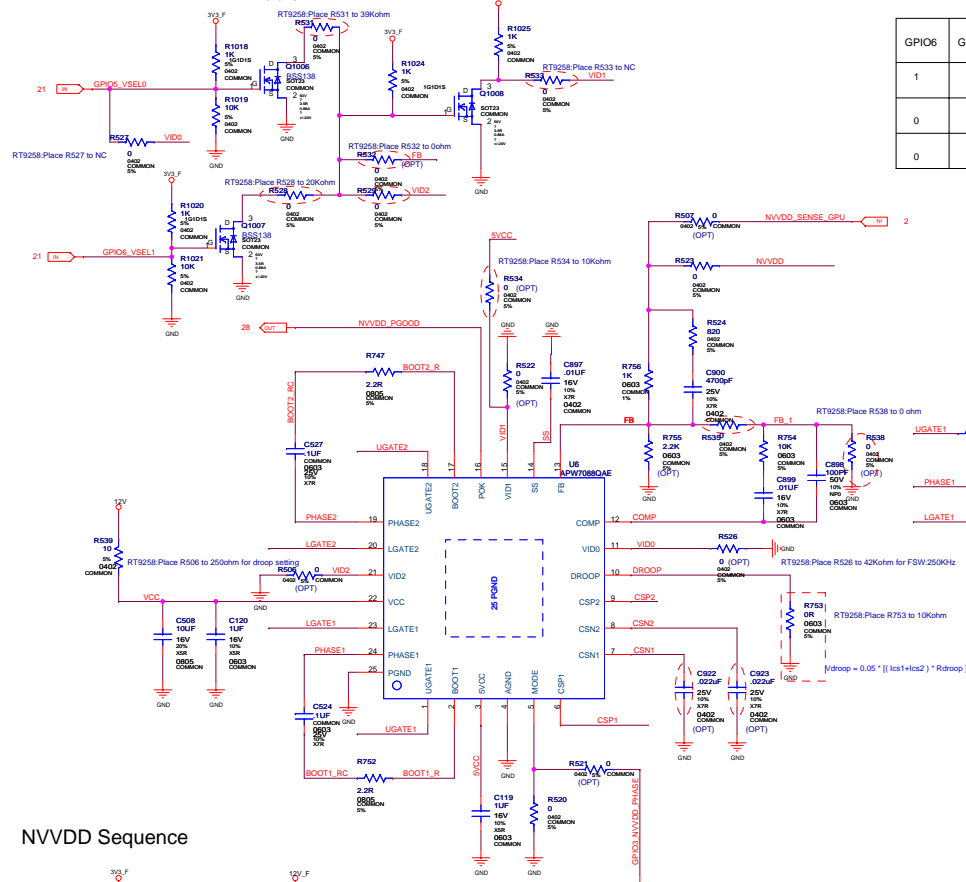
ASSEMBLY PAGE DETAIL PS II: PEX\_VDD, IFP\_PLLVDD, 2V5, 5V, and DDC\_5V Power Supply

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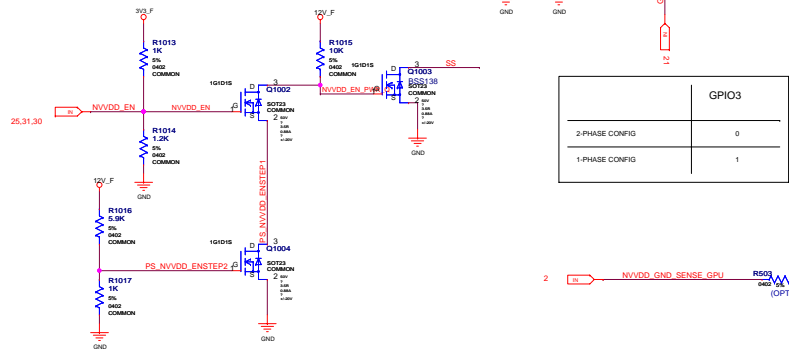




NVDD Voltage Select			
NVDD range 0.80V-1.40V			
Regulator: AOP2024			
Control via NV_GPCONF, NV_VSEL[1..0]			
VID			NVDD
6	5	4:3:2	1:0
Vout			
0 1 1 0 1 0	0.80V		
0 1 1 0 1 1	0.85V		
0 1 1 0 0 0	0.90V		
0 1 1 0 0 1	0.95V		
0 1 0 1 0 0	1.00V		
0 1 0 1 0 1	1.05V		
0 1 0 0 1 0	1.10V		
0 1 0 0 1 1	1.15V		
0 1 0 1 1 0	1.20V		
0 1 0 1 1 1	1.25V		
0 1 0 0 0 0	1.30V		
0 1 0 0 0 1	1.35V		
0 0 1 1 1 0	1.40V		
0 0 1 1 1 1	1.40V		
			G94
			⇒ Default
			⇒ Voltage1
			⇒ Voltage2



## NVVDD Sequence

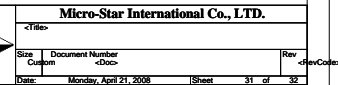


ASSEMBLY PAGE DETAIL  
 PS V: NVVDD Power Supply

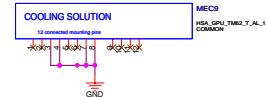
## NVVDD Power Supply

NVVDD = 0.9-1.2V @ 40-50A

ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Diode and Fan Control



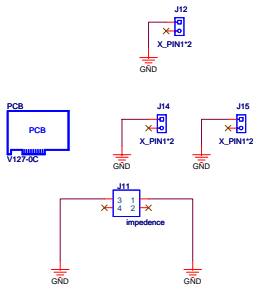
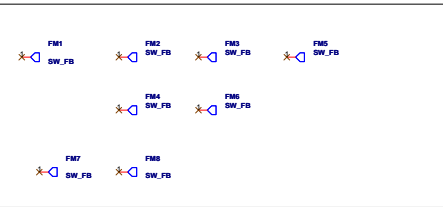
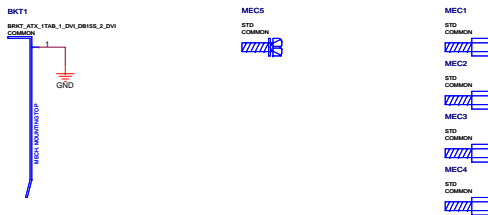
Thermal



Mechanical



Bracket



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ASSEMBLY PAGE DETAIL PCB BOARD LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO 3D/2D ASSEMBLY NOTES AND/OR NOT FINAL Thermal, Mechanical, and Bracket



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