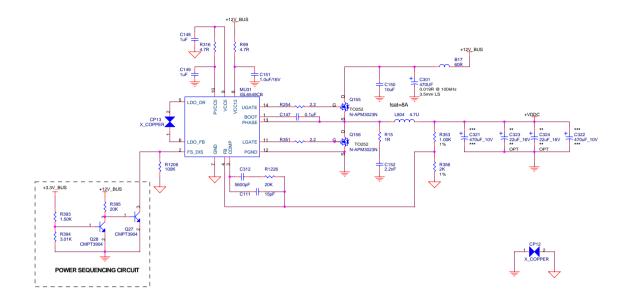
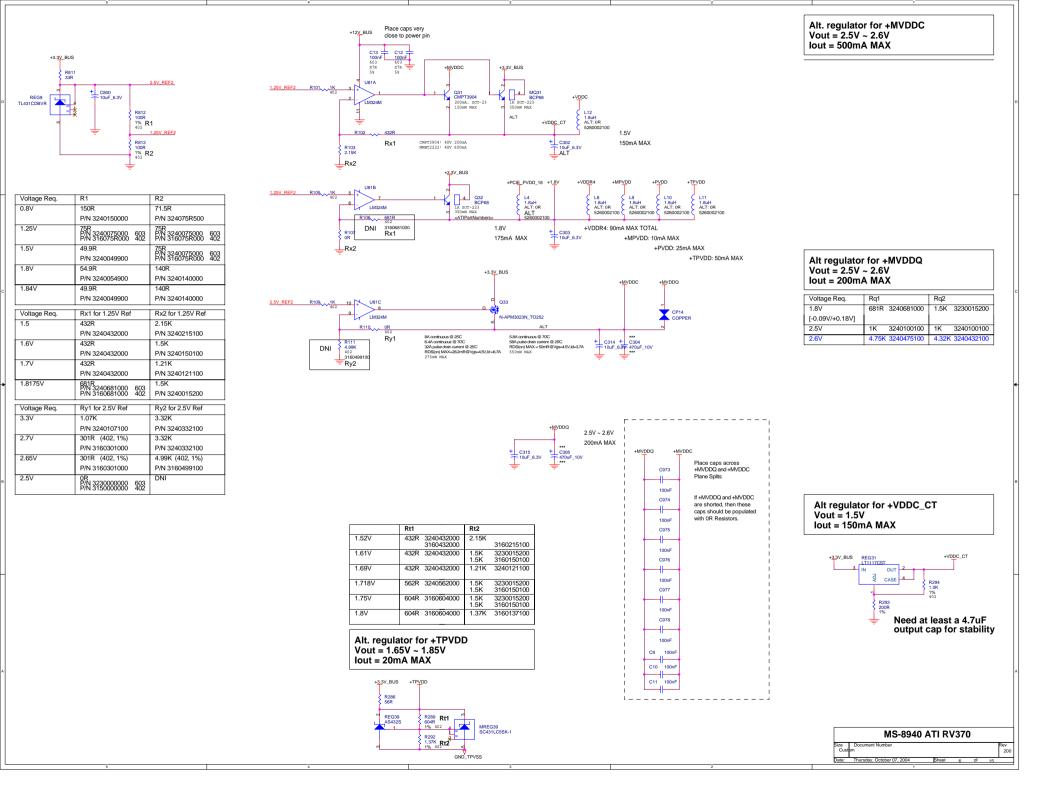


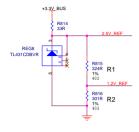
Regulator for VDDC (ASIC Core) Vout = 1.2V ~ 1.3V





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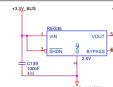






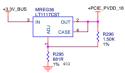


Alt. regulator for +A2VDD Vout = 2.5V lout = 120mA MAX



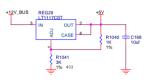
+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.

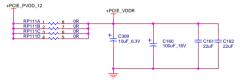
Alt. regulator for PCIE_PVDD_18 Vout = 1.85V lout = 500mA MAX



Need at least a 4.7uF output cap for stability

Regulator for +5V Vout = 5V lout = 20mA MAX





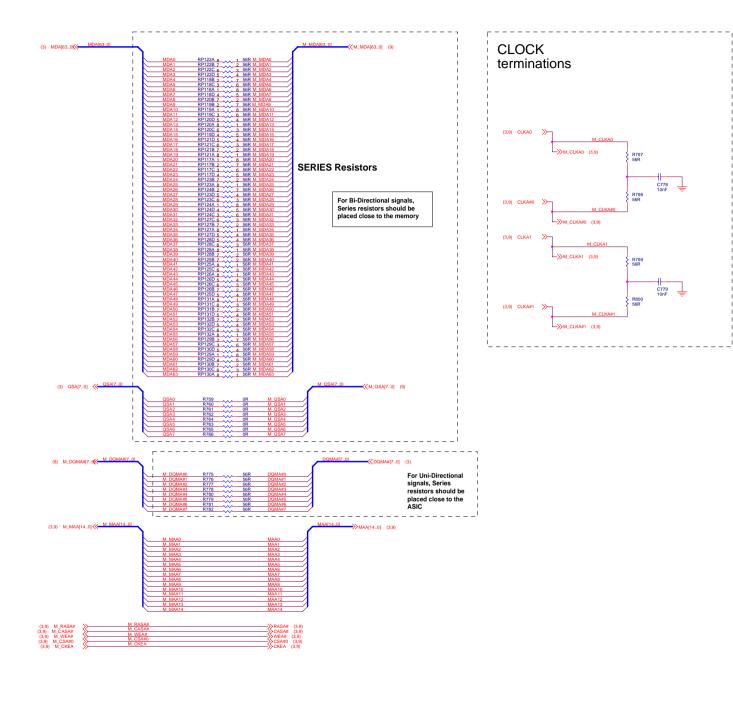
+PCIE_PVDD_18

+ C308 10uF_6.3V

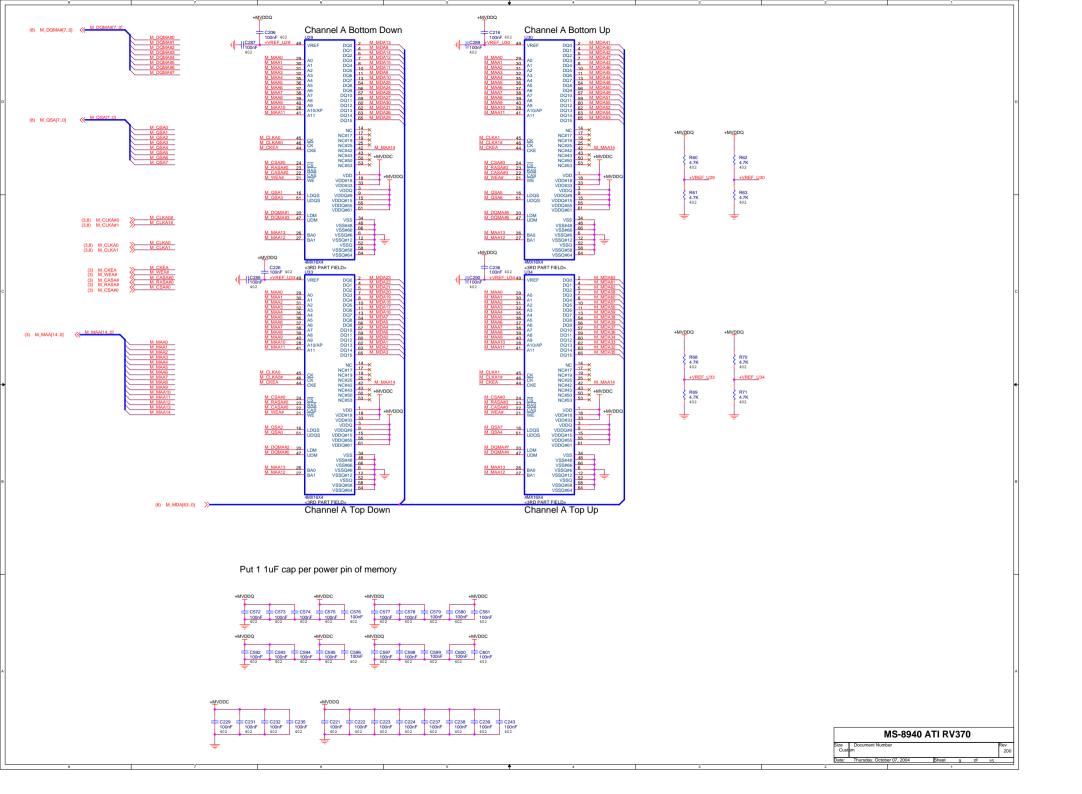
+PCIE_PVDD_12: 1.2V 250mA MAX

	Part	Vout	R1	R2
	MAX1935 0.8V Ref	1.2V	1.00K 1% ⁴⁰² ATI P/N 3160100100	2.00K 1% ⁴⁰² ATI P/N 3160200100
		1.79V	6.81K 1% ATI P/N 3160681100	5.49K 1% ⁴⁰² ATI P/N 3160549100

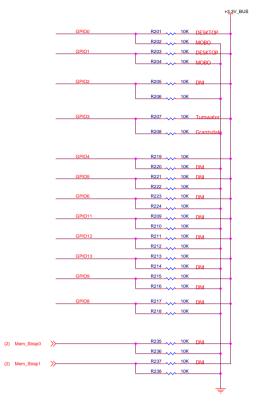
	MS-8940	ATI R	/37	0		
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Date:	Thursday, October 07, 2004	Sheet	7	of	15	



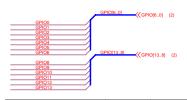
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OPTION STRAPS



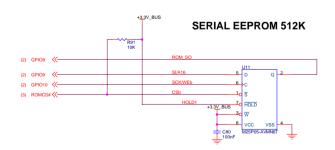




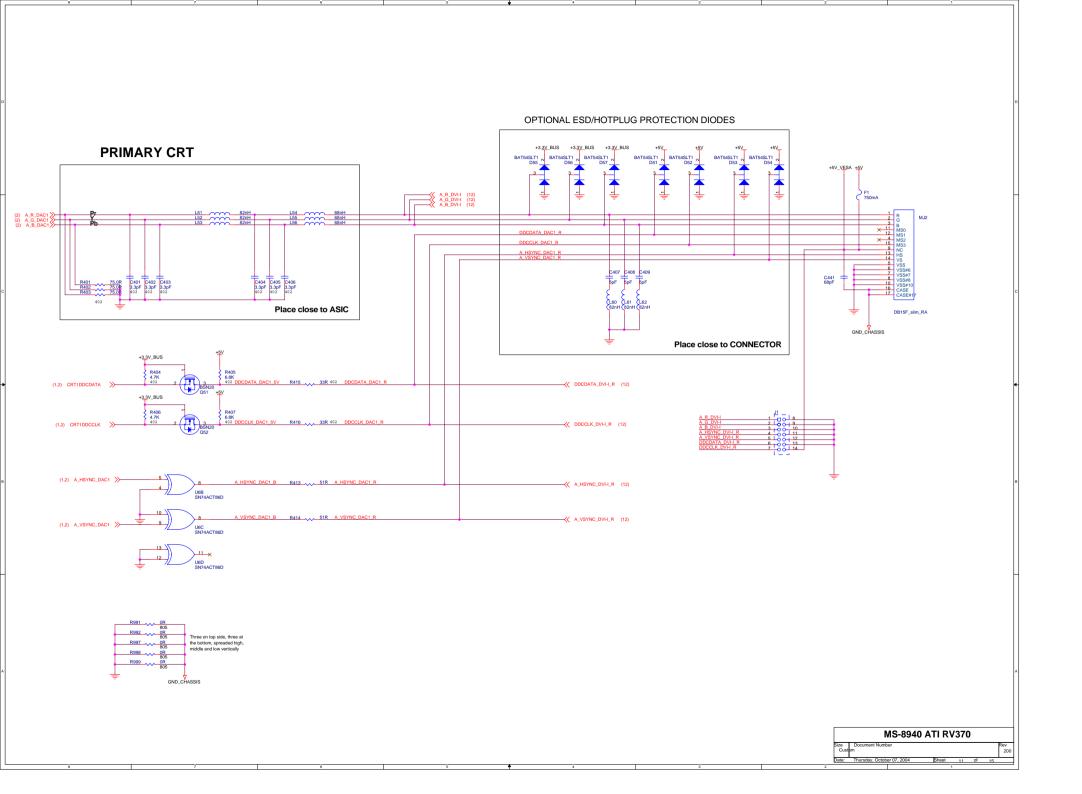
STRAP_B_PTX_PWRS_ENB GPIO0 Transmitter Power Savings Enable				
O: 50% Tx output swing for mobile mode 1: full Tx output swing 1: Tx de-emphasis deable 0: Tx de-emphasis deable 0: Tx de-emphasis deable 1: Tx de-emphasis deable 0: Tx de-emphasis	STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
O'T-K de-emphasis disabled for mobile mode 1:Tx de-emphasis enabled 1:Tx de-emphas	STRAP_B_PTX_PWRS_ENB	GPI00	0: 50% Tx output swing for mobile mode	0
OI: Nymer-compatible mode 10: PCI Express 10 mode (Tumwater) 10: PCI Express 10 mode (STRAP_B_PTX_DEEMPH_EN	GPIO1	0: Tx de-emphasis disabled for mobile mode	0
C normal node 1: extra current in Tx output stage - potential power savings for mobile mode 1: extra current in Tx output stage - potential power savings for mobile mode 1: extra current in Tx output stage - potential power savings for mobile mode C normal operational mode 1: compliance mode 1: compliance mode 1: compliance mode PLL Bandwidth C: tull PLL Bandwidth T: reduced PLL bandwi	PCIE_MODE(1:0)	GPIO(3:2)	O1: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0 mode and short-circuit internal loopback mode	00
Cr. normal operational mode 1: compliance mode PLL Bandwidth 0: hat PLL Bandwidth 0: hat PLL Bandwidth 1: resourced PLL bandwidth 2: part of PLL bandwidth 3: part of PLL bandwidth 1: resourced PLL bandwidth 1: resourced PLL bandwidth 2: part of PLL bandwidth 1: resourced PLL bandwidth 1: part of PLL bandwidth 1: resourced PLL b	STRAP_B_PTX_IEXT	GPIO4	0: normal mode	0
C. full PLL Bandwidth 1: reduced PLL bandwidth 1: reduced PLL bandwidth 1: reduced PLL bandwidth STRAP_DEBUG_ACCESS GPIO8 Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible. ROMIDCFG(3:0) GPIO(9,13:11) If no ROM attached, comtrols chip IDs. If rom attached identifies ROM type 0000- Ne ROM, CHCL_ID=0 0000- Ne ROM, CHCL_ID=0 0000- Ne ROM, CHCL_ID=0 01000- reserved 0110- reserved 1000- ROM (Ampel, chip IDs from ROM 1010- Serial AT4250011 ROM (Ampel, chip IDs from ROM 1011- Serial AT425010 ROM (ST), chip IDs from ROM 1011- Serial ROM (ST) 1011- Serial AT425010 ROM (ST), chip IDs from ROM 1011- Serial AT4	STRAP_FORCE_COMPLIANCE	GPIO5	0: normal operational mode	0
even if registers are inaccessible. ROMDCFG(3:0) GPIO(9,13:11)	STRAP_B_PPLL_BW	GPI06	0: full PLL Bandwidth	0
0000 - No ROM, CHAI, [Dis-1] 0001 - No ROM, CHAI, [Dis-1] 0001 - No ROM, CHAI, [Dis-1] 0011 - reserved 1000 - Parallel ROM, chip [Dis from ROM 1000 - Parallel ROM, chip [Dis from ROM 1010 - Serial AT-240B011 ROM (Aurell, chip [Dis from ROM 1011 - Serial AT-240B011 ROM (Aurell, chip [Dis from ROM 1011 - Serial M25910 ROM (ST), chip [Dis from ROM 1010 - Serial M25910 ROM (ST), chip [Dis from ROM 1000 - Serial M25910 ROM (ST), chip [Dis from ROM 1000 - Serial M25910 ROM (SS), chip [Dis from ROM	STRAP_DEBUG_ACCESS	GPI08		0
(VHAD0 net) 0 - Slave VIP host port devices present	ROMIDCFG(3:0)	GPIO(9,13:11)	0000 - No ROM, CHG, ID-0 0001 - No ROM, CHG, ID-0 0101 - No ROM, CHG, ID-1 0100 - reserved 0100 - Parallel ROM, ship IDis from ROM 0100 - Serial AT25+1024 ROM (Almel), chip IDis from ROM 1010 - Serial AT25+1024 ROM (Almel), chip IDis from ROM 1011 - Serial MSSP10 ROM (ST), chip IDis from ROM 1011 - Serial MSSP10 ROM (ST), chip IDis from ROM 1011 - Serial MSSP10 ROM (ST), chip IDis from ROM	
	VIP_DEVICE	DVPDATA_20 (VHAD0 net)	0 - Slave VIP host port devices present	

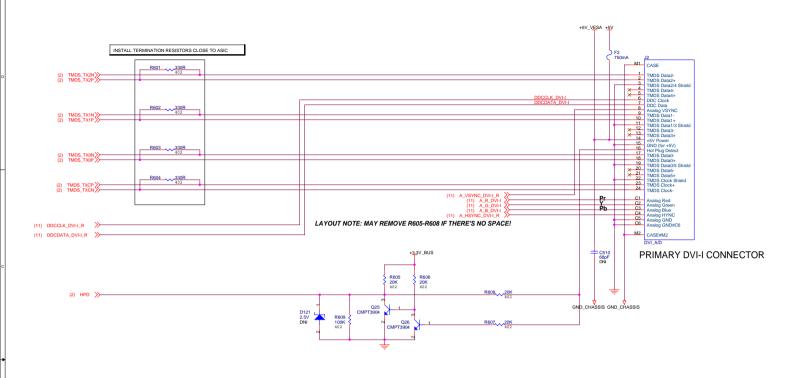
STRAP P	INTERRUPT
LOW	ENABLED (DEFAULT)
HIGH	DISABLED

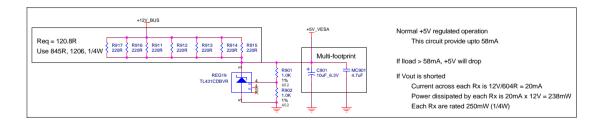
MEMORY TYPE STRAPS				
	Mem_Strap0	Mem_Strap1		
SAM	0	0		
INF	1	0		
HYN	0	1		
ELPIDA	1	1		



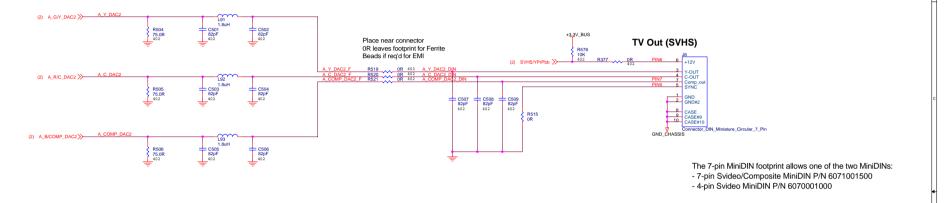
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Place Resistors close to ASIC.



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HEATSINK 7120005100 Spring push-pin



HEATSINK 71200080000 ITW push-pin

MS-8940 ATI RV370

