P672: GT215-128bit, 32Mx32 GDDR5

DL-DVI, VGA, HDMI

Page 1: TABLE OF CONTENTS
Page 2: PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS
Page 3: FBA MEMORY INTERFACE, GPU NVVDD & FBVDDQ DECOUPLING CAPS
Page 4: FBA 32Mx32 GDDR5 MEMORIES, FBA CLK TERMS
Page 5: FBA MEMORY FBVDDQ DECOUPLING CAPS
Page 6: FBC MEMORY INTERFACE
Page 7: FBC 32MX32 GDDR5 MEMORIES, FBC CLK TERMS
Page 8: FBC MEMORY FBVDDQ DECOUPLING CAPS
Page 9: DACA (PRIMARY DVI-I)
Page 10: DACB (SECONDARY VGA)
Page 11: TMDS LINK A/B: DVI-I (SOUTH)
Page 12: LINK C: HDMI (NORTH)
Page 13: LINK D (UNUSED)
Page 14: LINK E/F: (UNUSED)
Page 15: MIOA & MIOB (UNUSED)
Page 16: XTAL, MECHANICALS, THERMALS
Page 17: FAN CONTROL, THERMAL ALERT, GPIO, JTAG
Page 18: VBIOS ROM, INFOROM, STRAPPING OPTIONS
Page 19: 5V, DDC5V, IFP PLLVDD, IFP IOVDD, 3V3 FILTER, 12V FILTER
Page 20: FBVDDQ SINGLE PHASE SWITCHER, PEX_VDD LINEAR
Page 21: NVVDD DUAL PHASE SWITCHER
Page 22: BaseNet Report 1
Page 23: BaseNet Report 2
Page 24: CREFER Parts

PCB 4.0

09/01 change PAGE 04_FBA 32Mx32 GDDR5--Lower Half -------- x16 mode
Add PAGE 04_FBA 32Mx32 GDDR5--Upper Half -------- x16 mode
change PAGE 04_FBC 32Mx32 GDDR5--Lower Half -------- x16 mode
Add PAGE 07_FBC 32Mx32 GDDR5--Upper Half -------- x16 mode
Add PAGE 05 DECOUPLING CAP
Add PAGE 08 DECOUPLING CAP
Add PAGE 17 GPIO10_VREF_SEL

PCB 4.1

11/10 Add PAGE 20 C2001,C2002 for EMI
11/11 Add PAGE 20 C2003,C2004,C2005 for EMI

MSIS-RMA
羅覓林
20100119

BOM	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10672-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10672-0001-100	GT215-450, 550/1375MHz 512MB 32Mx16 BGA170 1800MHz GDDR5 DVI-I/VGA/HDMI
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

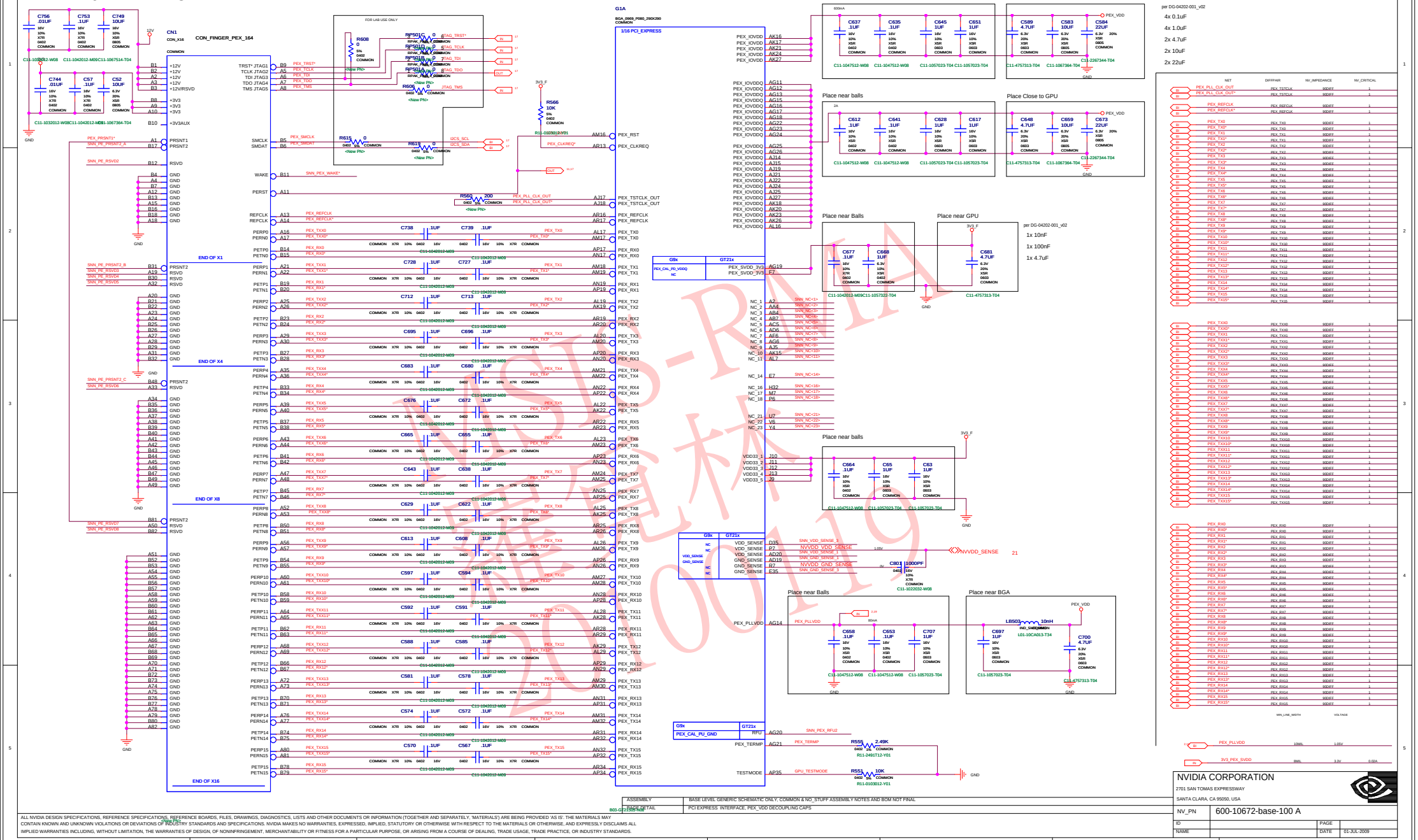
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TABLE OF CONTENTS

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

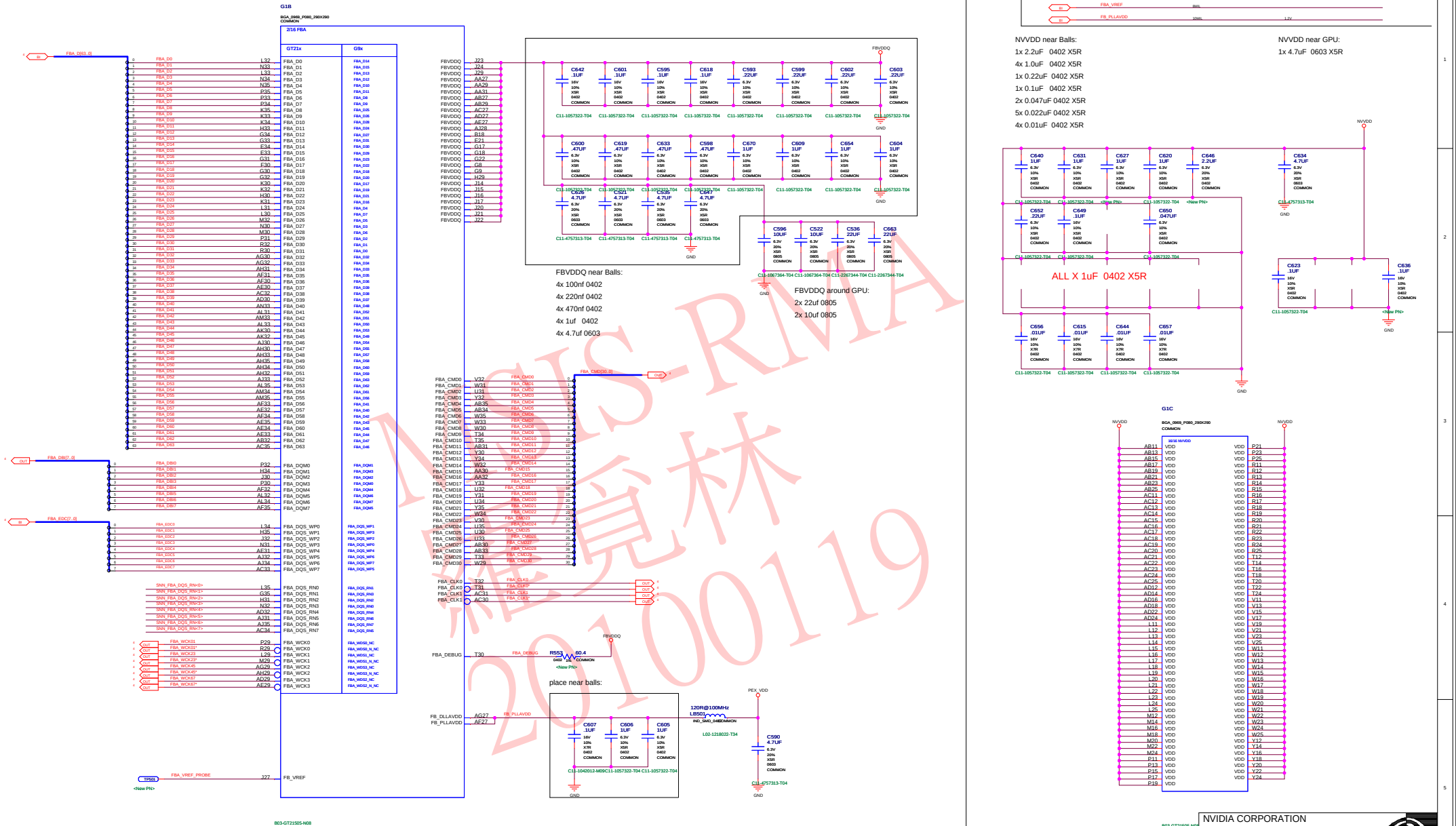
NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

PEX x16 INTERFACE



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

MEMORY Partition A - GPU, FBVDD/Q & NVVDD DECOUPLING



NVIDIS-RMA 維克林 20100119

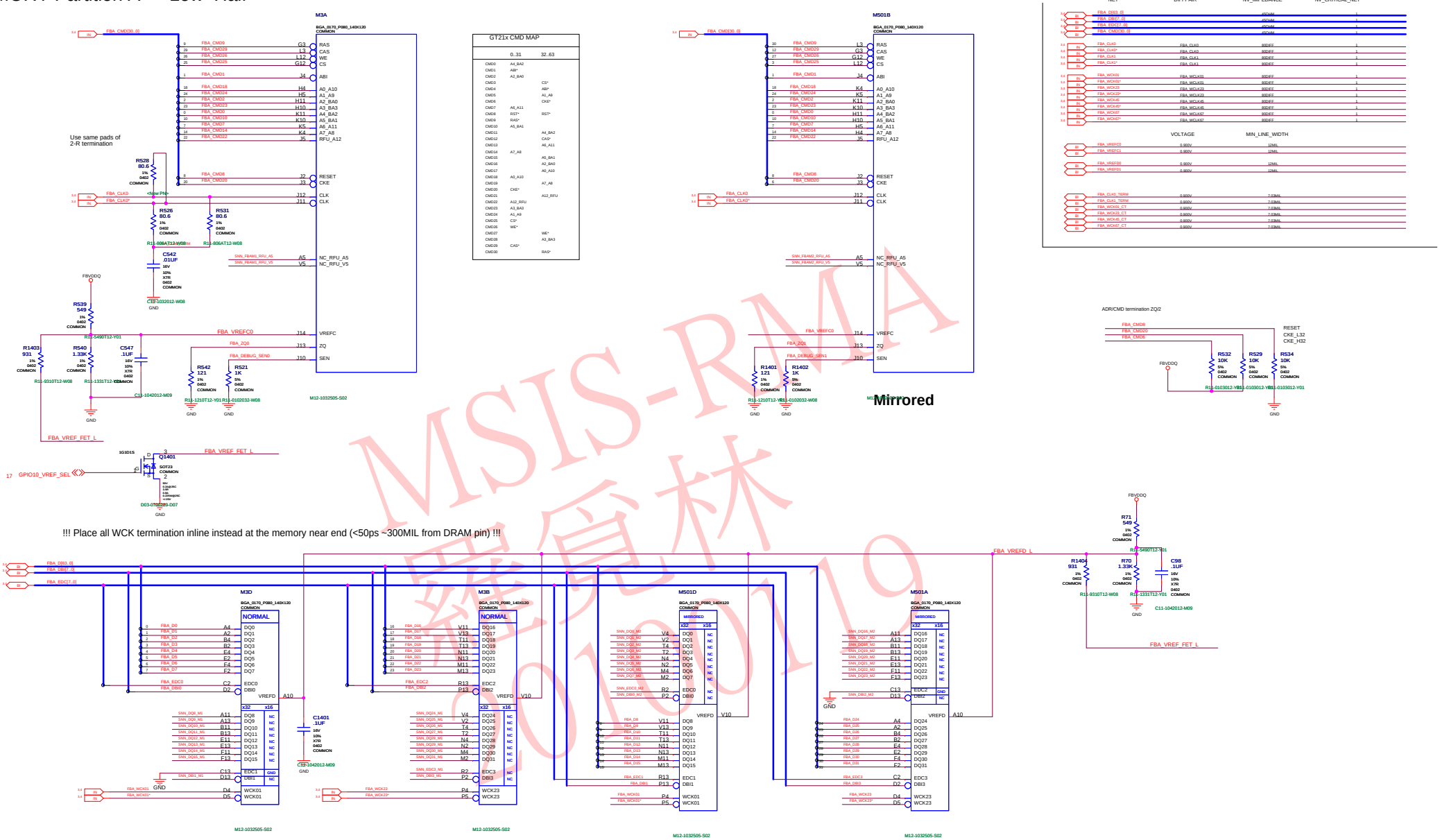
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY INTERFACE, GPU NVVDD & FBVDDQ DECOUPLING CAPS

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

MEMORY Partition A --- Low Half



MSIS-RMA 2010/10

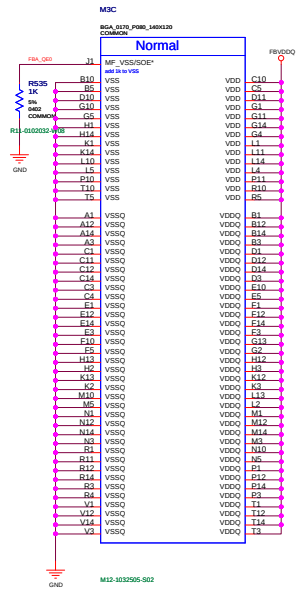
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 32Mx32 GDDR5 MEMORIES, FBA CLK TERMS

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

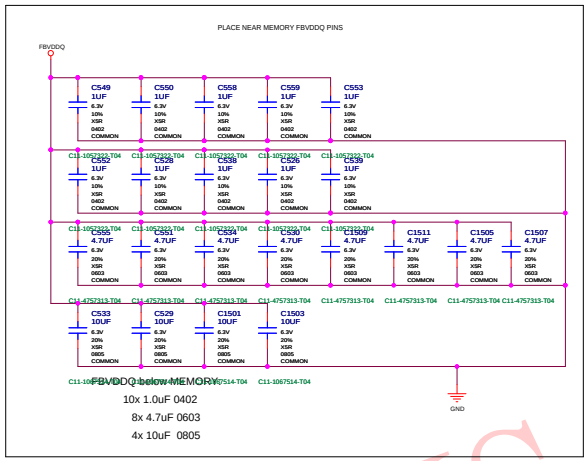
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

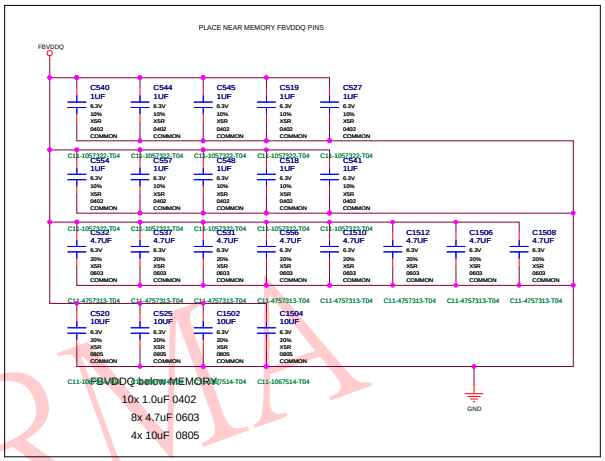
MEMORY Partition A - Decoupling

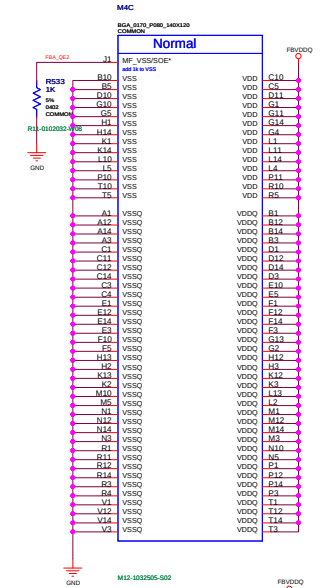


Decoupling for FBA 0..31

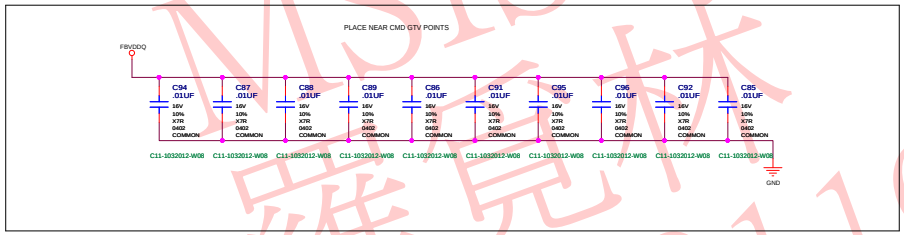


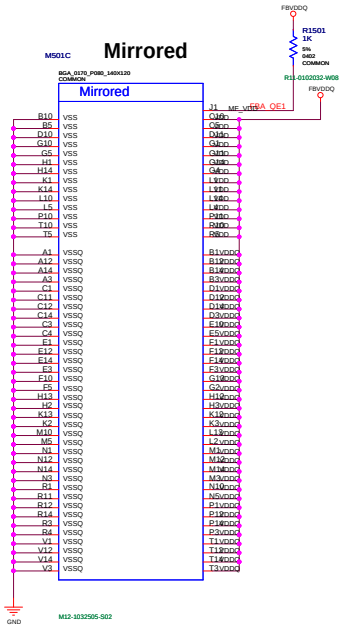
Decoupling for FBA 32..63

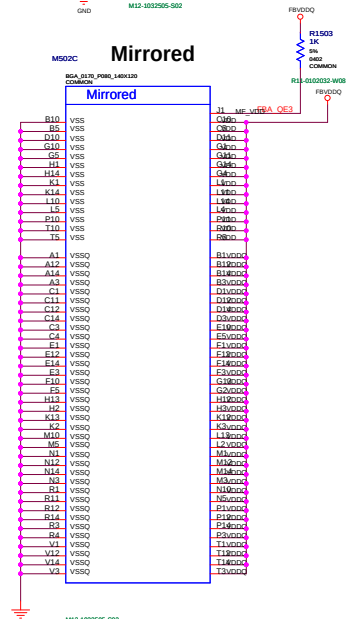




Return path coupling GND/FBVDDQ for FBA







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

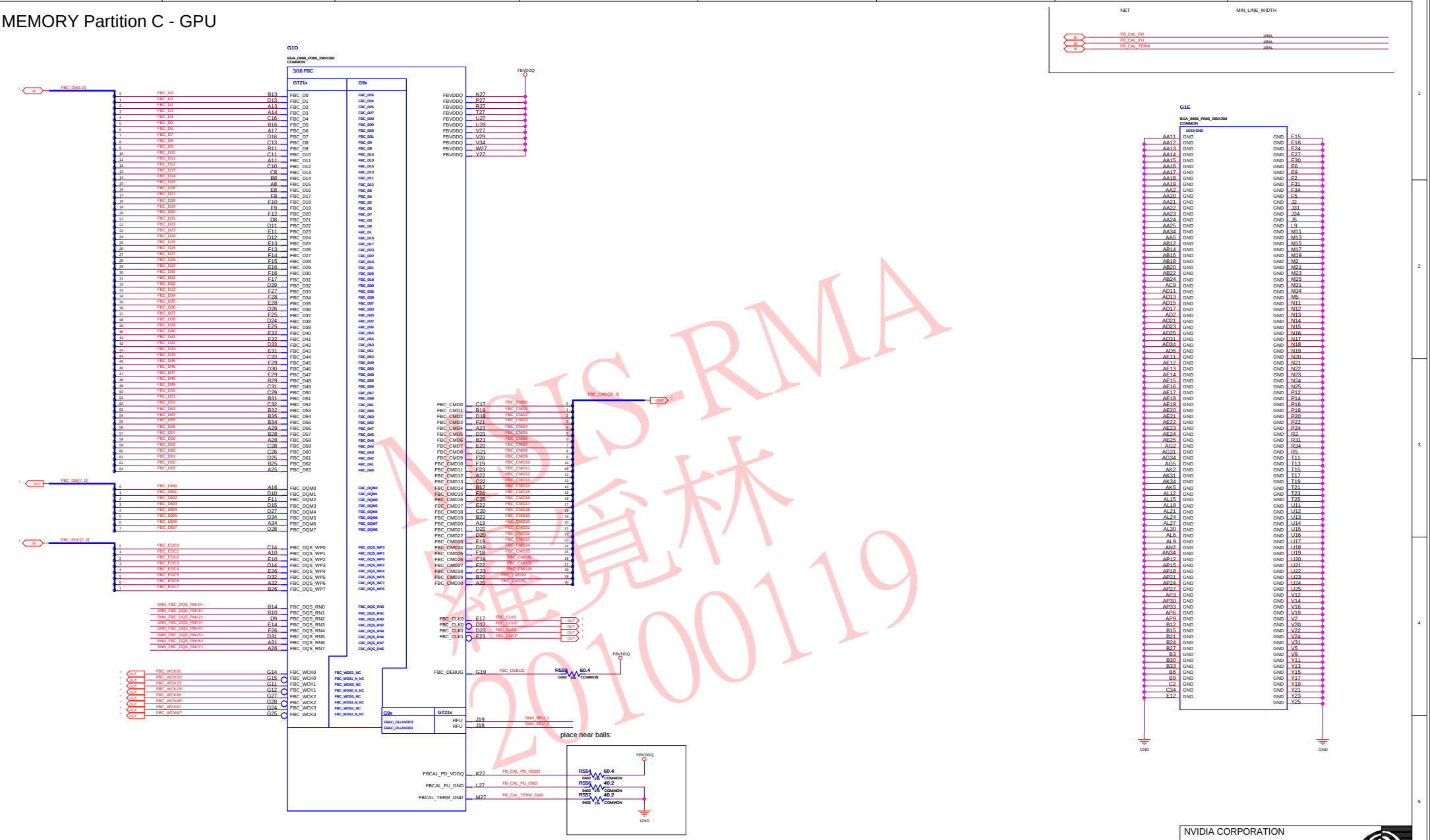
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

MSIS-RMA 羅昌林 20100119

MEMORY Partition C - GPU



MSIS-RMA 維賀林 20100119

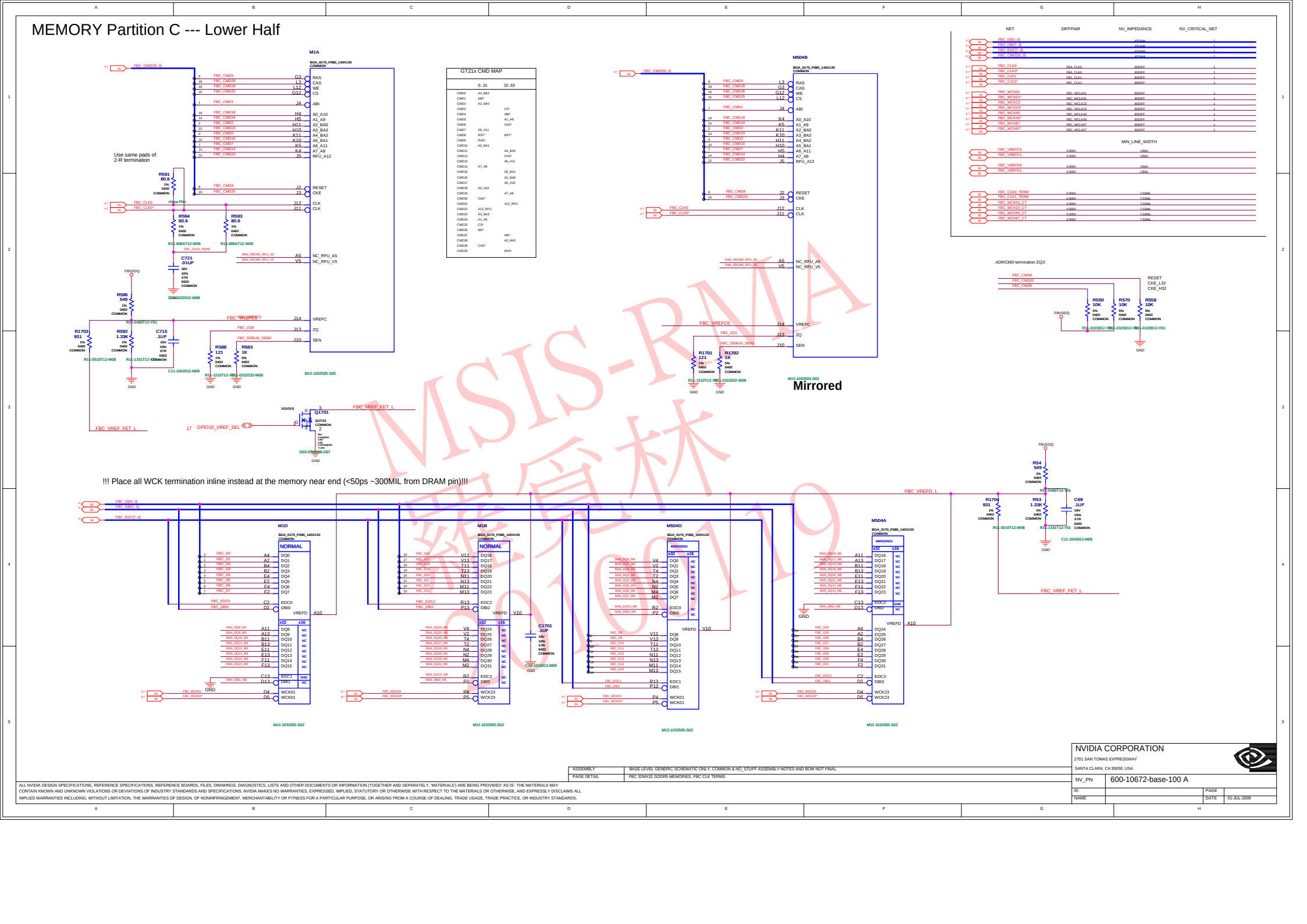
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY INTERFACE

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

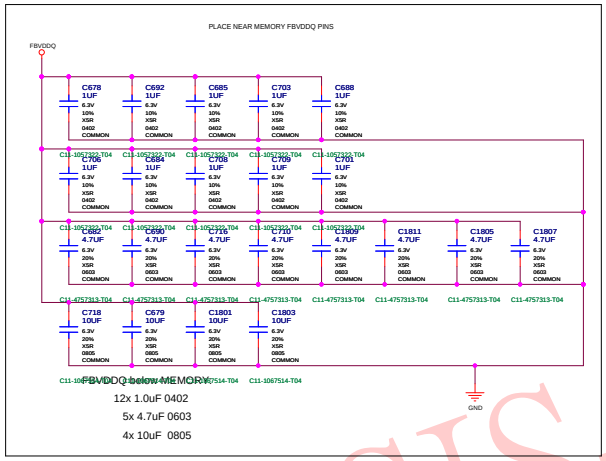
NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

MEMORY Partition C --- Lower Half

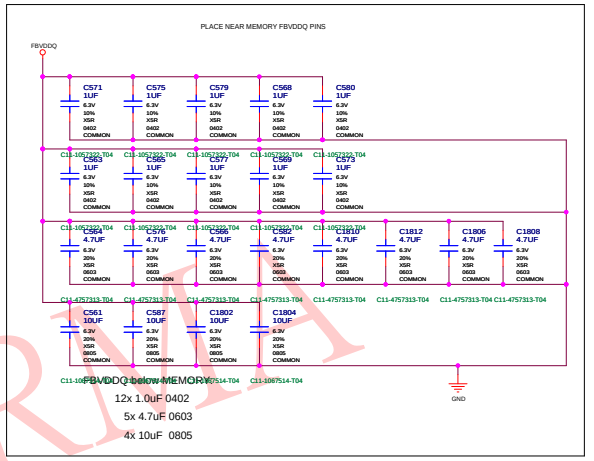


MEMORY PARTITION C DECOUPLING

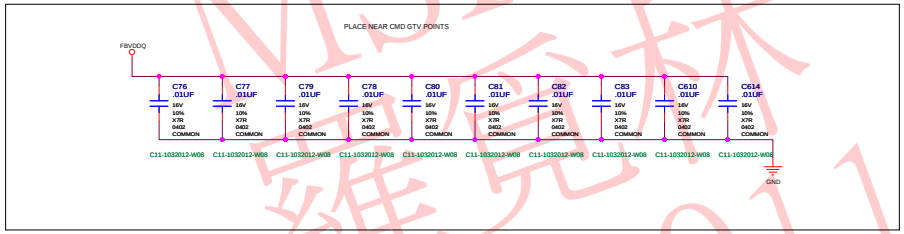
Decoupling for FBC 0..31



Decoupling for FBC 32..63



Return path coupling GND/FBVDDQ for FBC



M1C — Normal

M2C — Normal

M504C — Mirrored

M503C — Mirrored

MSIS-RMA 羅覓林 20100119

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS

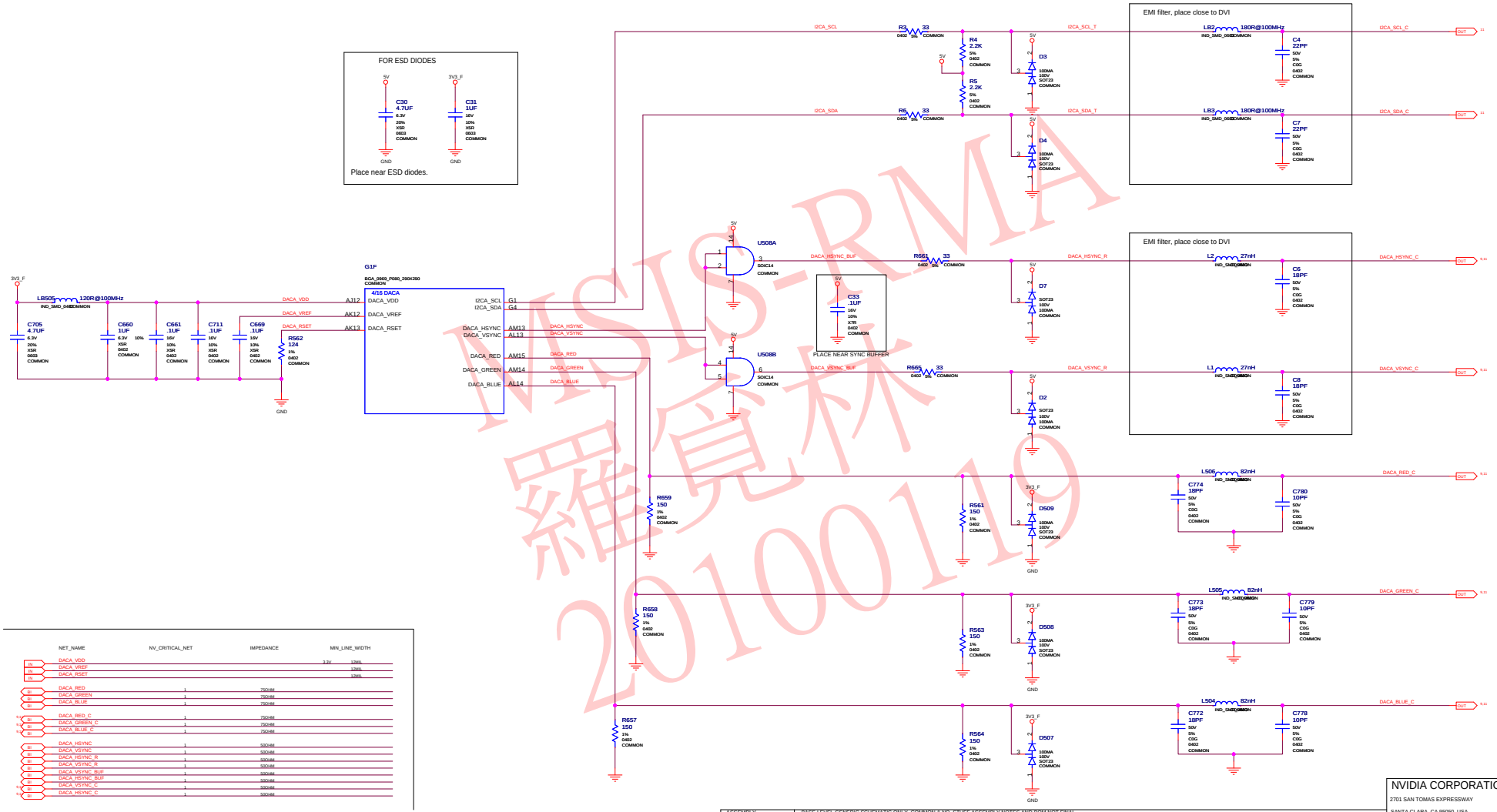
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

Primary Display (DACA), DVI-I (South)

DACA FILTER



NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACA_VDD			3.3V 12MIL
DACA_VREF			12MIL
DACA_RSET			12MIL
DACA_RED	1	75OHM	
DACA_GREEN	1	75OHM	
DACA_BLUE	1	75OHM	
DACA_RED_C	1	75OHM	
DACA_GREEN_C	1	75OHM	
DACA_BLUE_C	1	75OHM	
DACA_HSYNC	1	50OHM	
DACA_VSYNC	1	50OHM	
DACA_HSYNC_R	1	50OHM	
DACA_VSYNC_R	1	50OHM	
DACA_VSYNC_BUF	1	50OHM	
DACA_HSYNC_BUF	1	50OHM	
DACA_VSYNC_C	1	50OHM	
DACA_HSYNC_C	1	50OHM	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA (PRIMARY DVI-I)

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

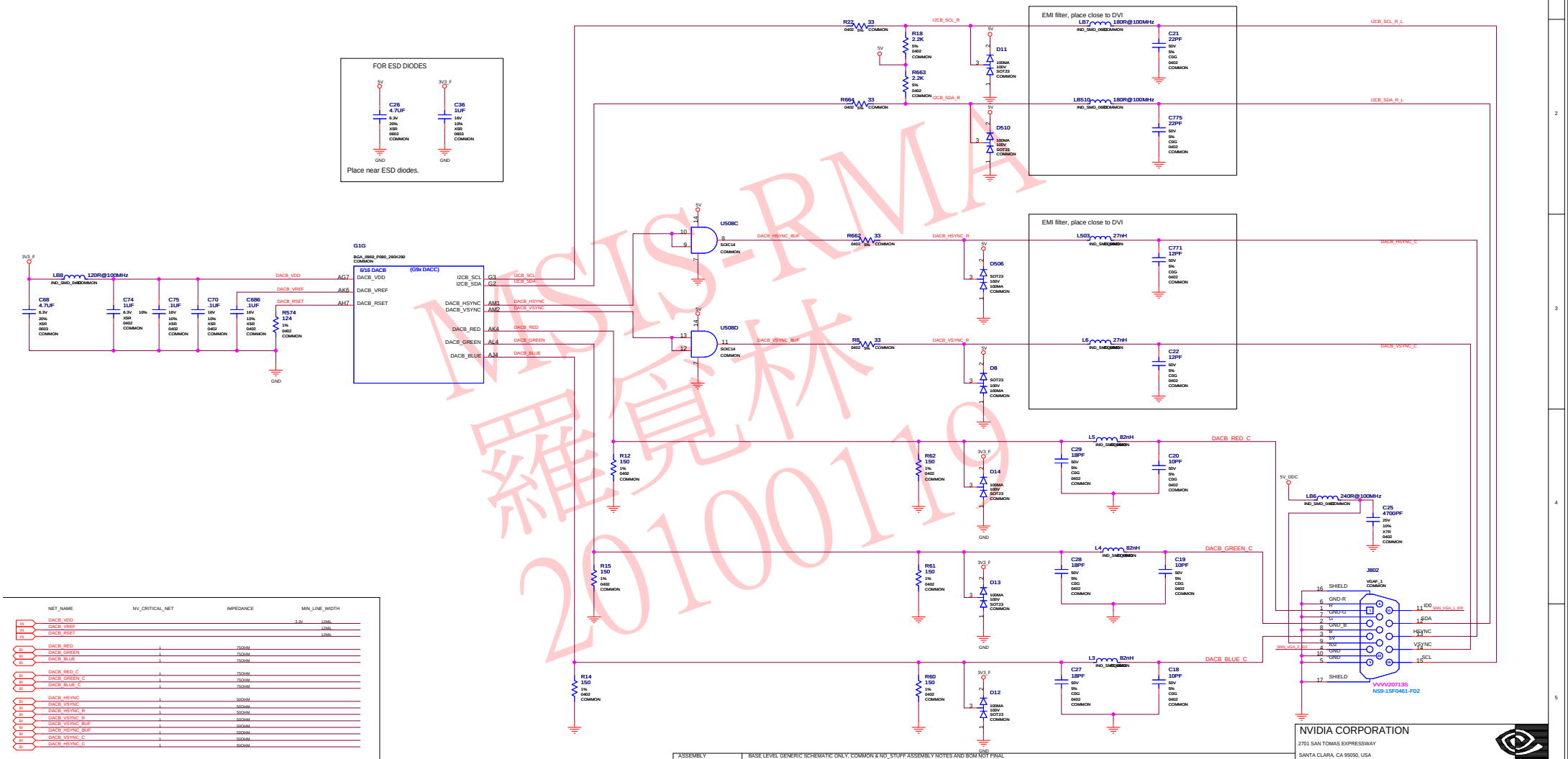
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

MSI S-RMA 羅賞林 20100119

Secondary Display (DACB), VGA (Mid)

DACB FILTER



NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACB_VDD			3.3V 12MIL
DACB_VREF			12MIL
DACB_RSET			12MIL
DACB_RED	1	75OHM	
DACB_GREEN	1	75OHM	
DACB_BLUE	1	75OHM	
DACB_RED_C	1	75OHM	
DACB_GREEN_C	1	75OHM	
DACB_BLUE_C	1	75OHM	
DACB_HSYNC	1	50OHM	
DACB_VSYNC	1	50OHM	
DACB_HSYNC_R	1	50OHM	
DACB_VSYNC_R	1	50OHM	
DACB_HSYNC_BUF	1	50OHM	
DACB_VSYNC_BUF	1	50OHM	
DACB_VSYNC_C	1	50OHM	
DACB_HSYNC_C	1	50OHM	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB (SECONDARY VGA)

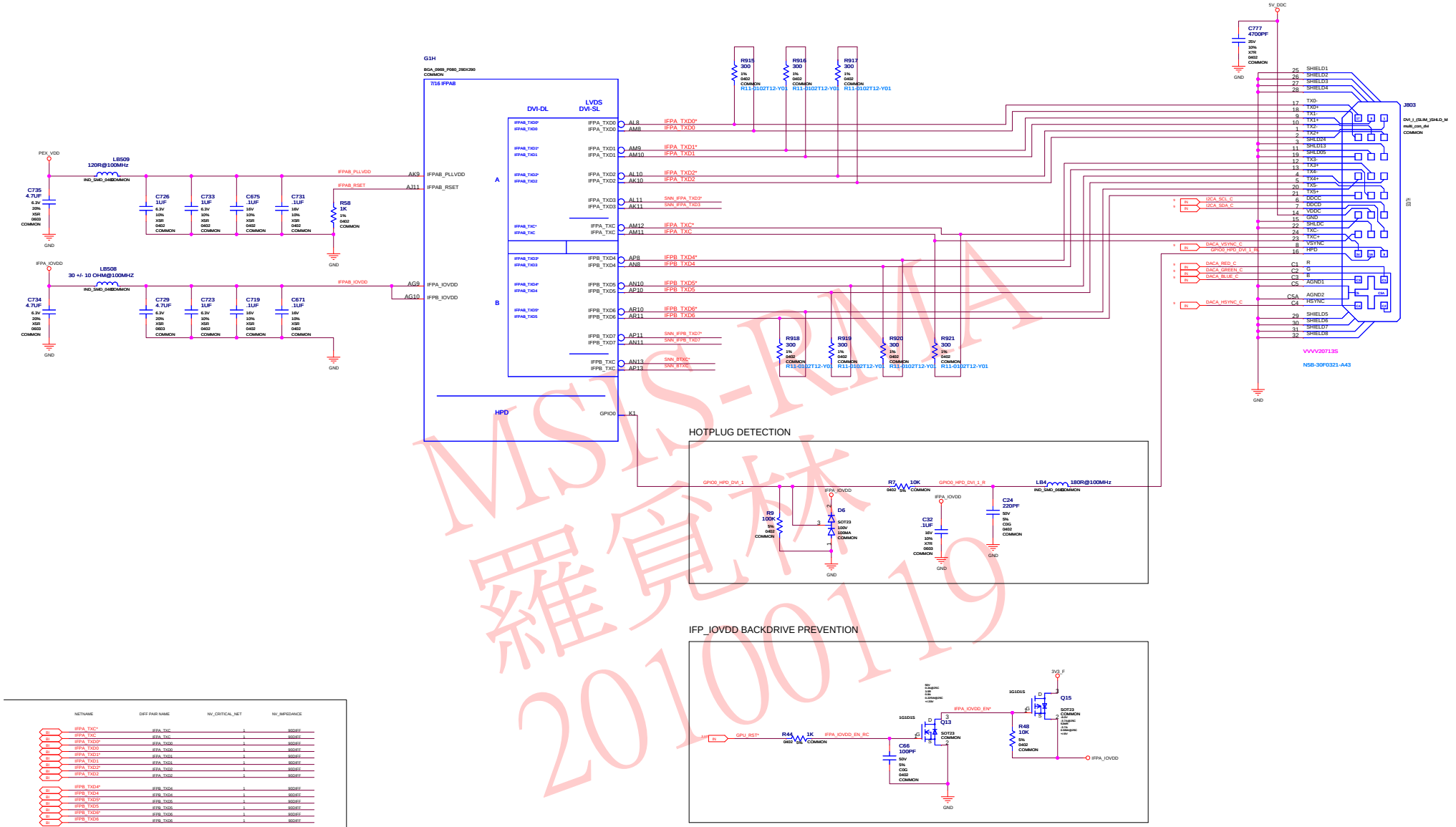
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

MSIS-RMA 羅宣林 20100119

LINK A/B: TMDS, Primary DVI-I DL (South)



MSI-RMA 羅宣林 20100119

NETNAME	DIFF PAIR NAME	NV_CRITICAL_NET	NV_IMPEDANCE
IFPA_TXC*	IFPA_TXC	1	90DIFF
IFPA_TXC	IFPA_TXC	1	90DIFF
IFPA_TXD0*	IFPA_TXD0	1	90DIFF
IFPA_TXD0	IFPA_TXD0	1	90DIFF
IFPA_TXD1*	IFPA_TXD1	1	90DIFF
IFPA_TXD1	IFPA_TXD1	1	90DIFF
IFPA_TXD2*	IFPA_TXD2	1	90DIFF
IFPA_TXD2	IFPA_TXD2	1	90DIFF
IFPB_TXD4*	IFPB_TXD4	1	90DIFF
IFPB_TXD4	IFPB_TXD4	1	90DIFF
IFPB_TXD5*	IFPB_TXD5	1	90DIFF
IFPB_TXD5	IFPB_TXD5	1	90DIFF
IFPB_TXD6*	IFPB_TXD6	1	90DIFF
IFPB_TXD6	IFPB_TXD6	1	90DIFF
IFPAB_PLLVDD	12MIL		1.05V
IFPAB_IOVDD	12MIL		3.3V
IFPAB_RSET	12MIL		

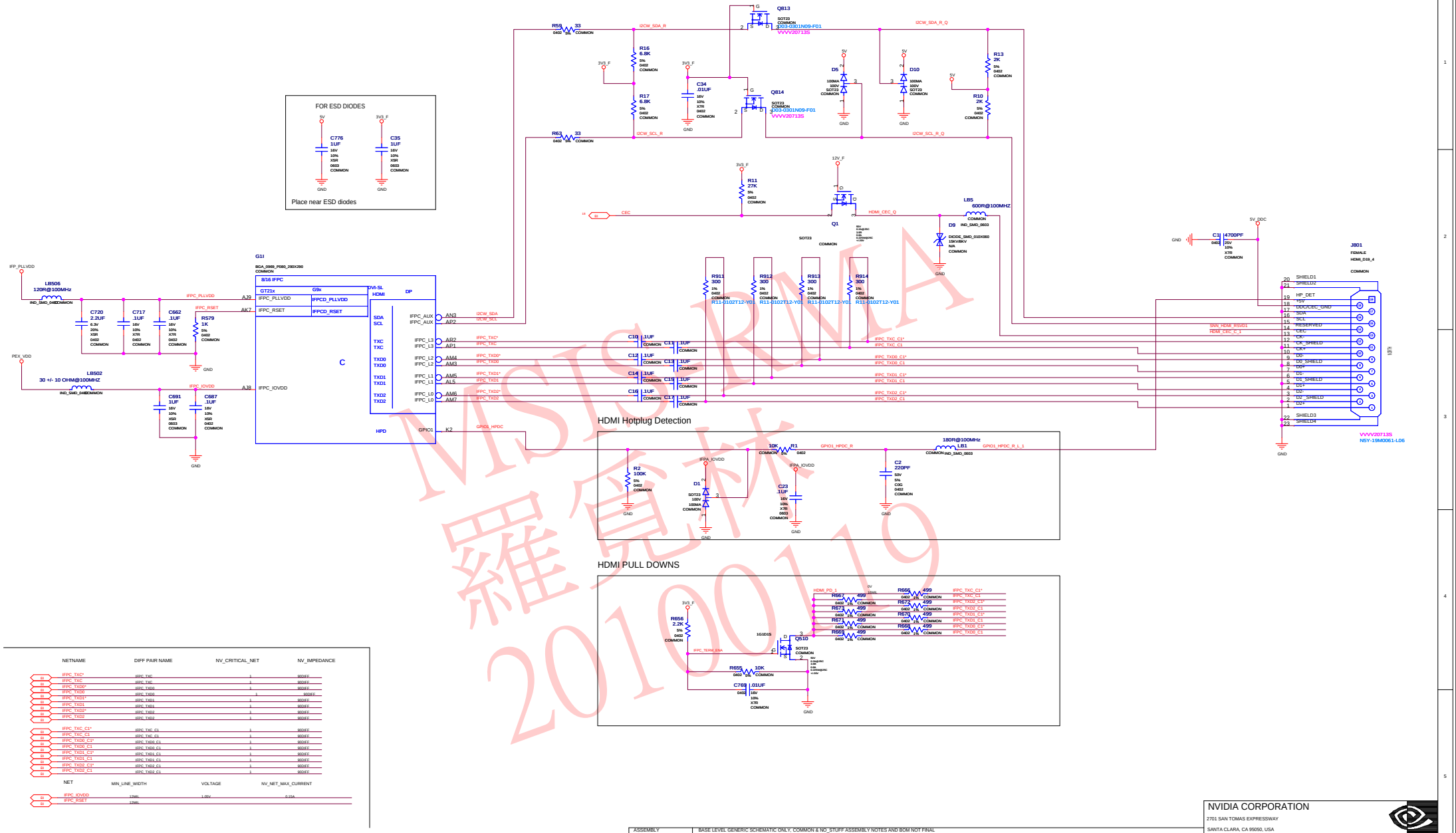
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK A/B: DVI-I (SOUTH)

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

LINK C: HDMI (North)



NETNAME	DIFF PAIR NAME	NV_CRITICAL_NET	NV_IMPEDANCE
IFPC_TXC*	IFPC_TXC	1	90DIFF
IFPC_TXC	IFPC_TXC	1	90DIFF
IFPC_TXD0*	IFPC_TXD0	1	90DIFF
IFPC_TXD0	IFPC_TXD0	1	90DIFF
IFPC_TXD1*	IFPC_TXD1	1	90DIFF
IFPC_TXD1	IFPC_TXD1	1	90DIFF
IFPC_TXD2*	IFPC_TXD2	1	90DIFF
IFPC_TXD2	IFPC_TXD2	1	90DIFF
IFPC_TXC_C1*	IFPC_TXC_C1	1	90DIFF
IFPC_TXC_C1	IFPC_TXC_C1	1	90DIFF
IFPC_TXD0_C1*	IFPC_TXD0_C1	1	90DIFF
IFPC_TXD0_C1	IFPC_TXD0_C1	1	90DIFF
IFPC_TXD1_C1*	IFPC_TXD1_C1	1	90DIFF
IFPC_TXD1_C1	IFPC_TXD1_C1	1	90DIFF
IFPC_TXD2_C1*	IFPC_TXD2_C1	1	90DIFF
IFPC_TXD2_C1	IFPC_TXD2_C1	1	90DIFF

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
IFPC_IOVDD	12Mil	1.05V	0.15A
IFPC_RSET	12Mil		

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK C: HDMI (NORTH)

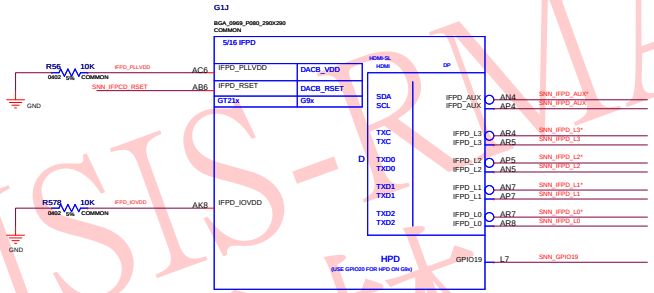
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

MSI RMA 羅宣林 20100119

LINK D: UNUSED



MSIS-RMA
羅覓林
20100119

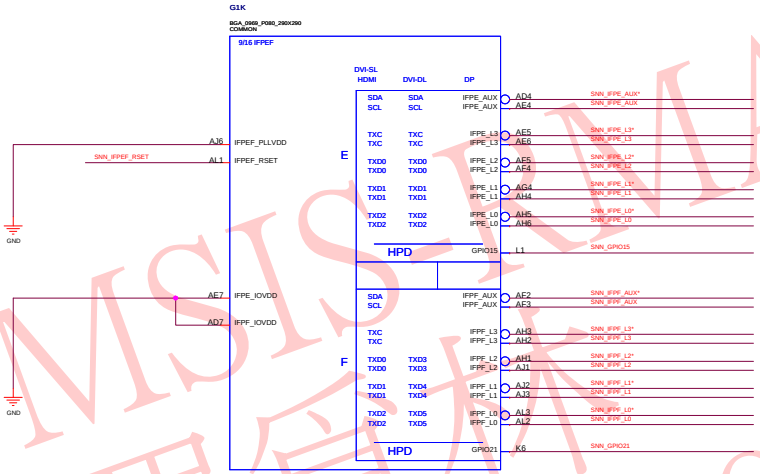
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK D (UNUSED)

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

LINK E/F: (UNUSED)



MSIS-RMA
羅覓林
20100119

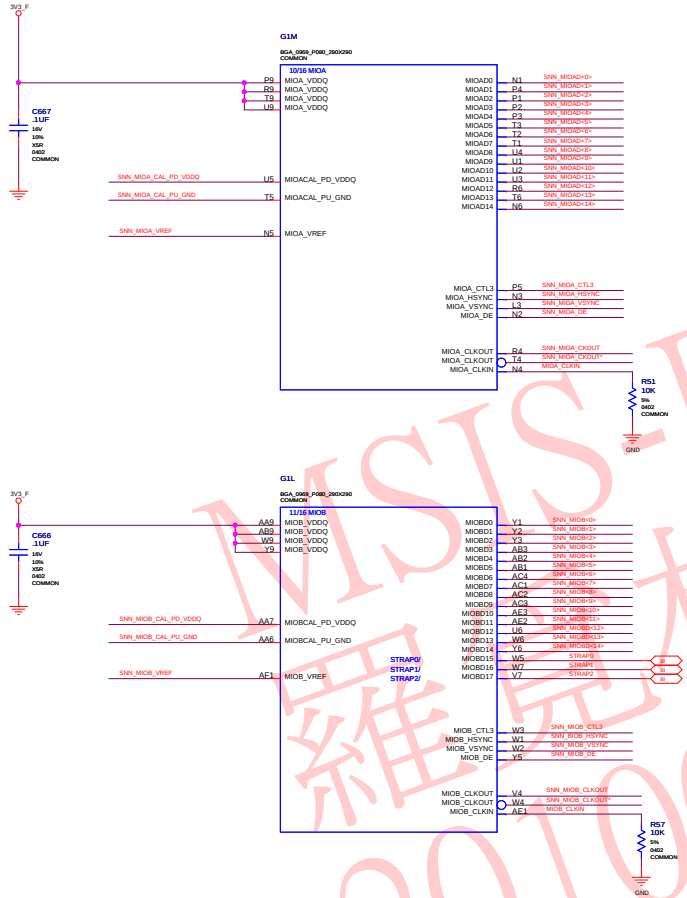
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK E/F: (UNUSED)

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

MIOA/B UNUSED



MSIS-RMA
羅景林
20100119

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB (UNUSED)

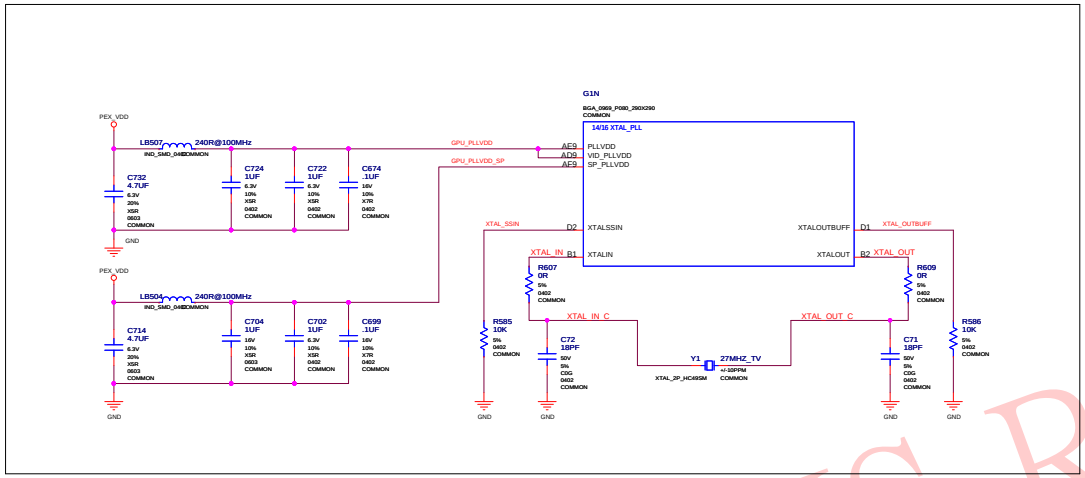
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

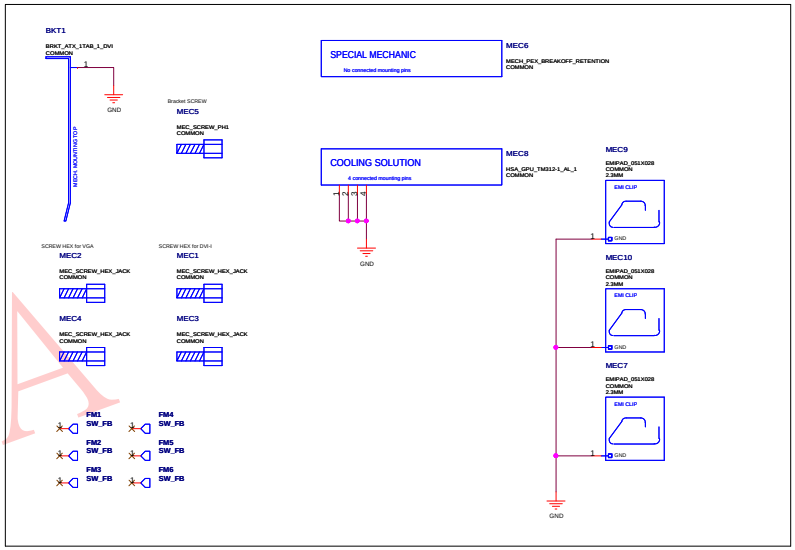
NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

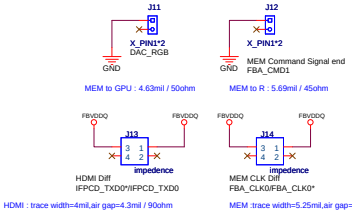
XTAL, MECHANICALS

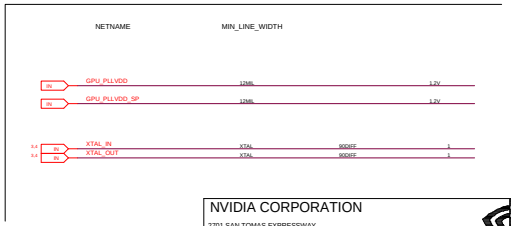
XTAL/GPU_PLLVDD



MECHANICALS & THERMALS







MSIS-RMA
羅覓林
20100119

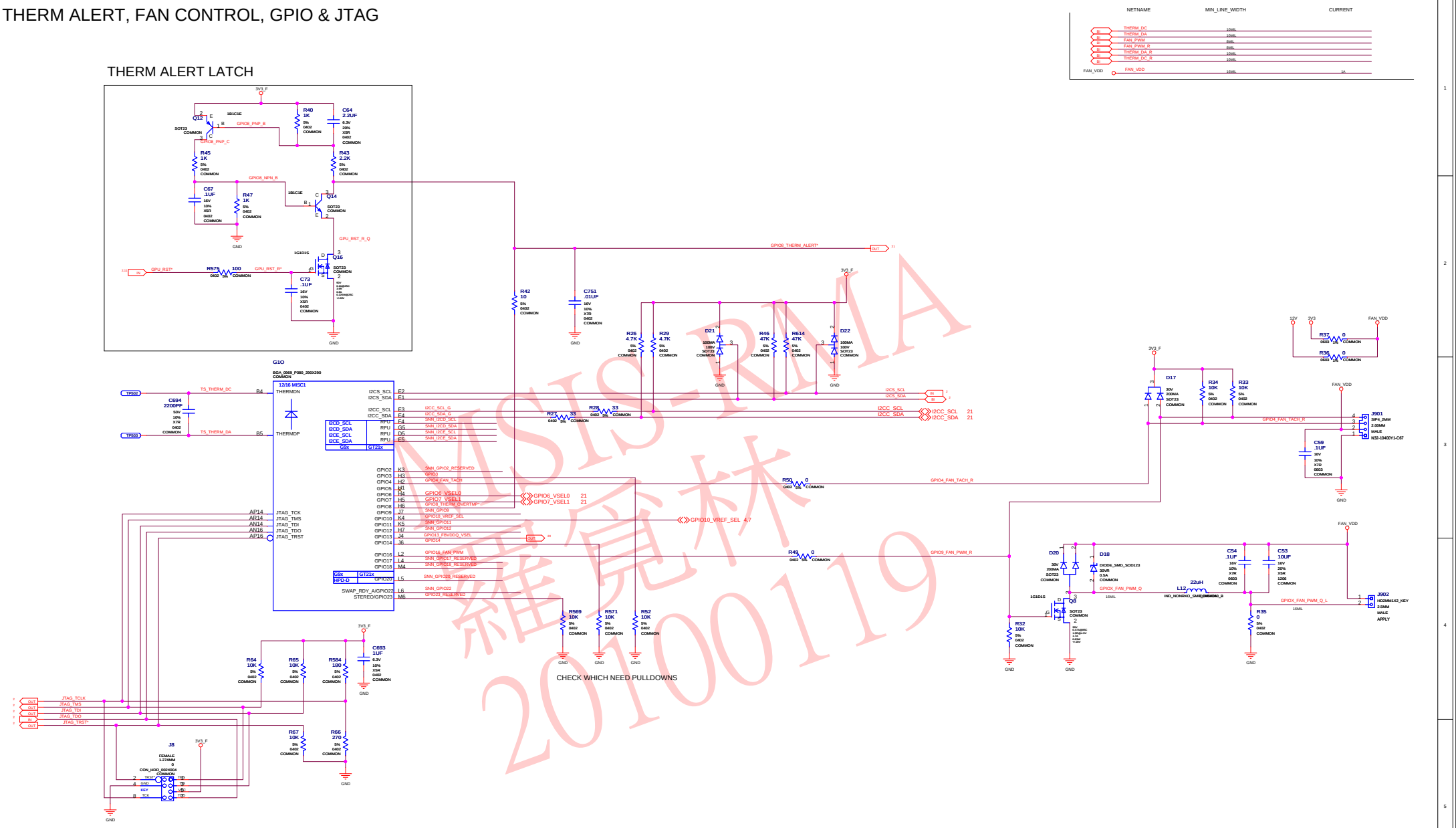
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, MECHANICALS, THERMALS

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

THERM ALERT, FAN CONTROL, GPIO & JTAG



MSIS-RMA
羅宛林
20100119

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FAN CONTROL, THERMAL ALERT, GPIO, JTAG

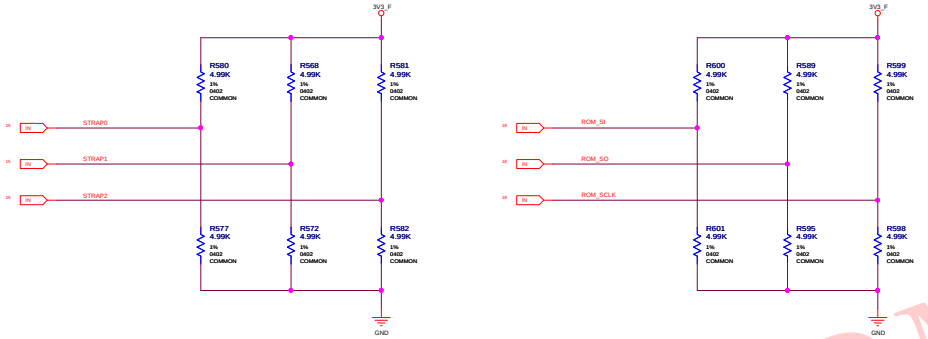
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

STRAPPING, VBIOS, INFOROM

STRAPPING OPTIONS



STRAP1[3..0] = 0x8 (3GIO_PADCFG DSKTOP default plus 0x8)

STRAP2[3..0] = 0xB (PCI_DEVID = 0xCAB)

ROM_SO[0] = 1 (VGA Device Enable)

ROM_SO[1] = 0 (SMB_ALT_ADDR, default (1GPU))

ROM_SO[2] = 0 (FB aper. size 256MB, default)

ROM_SO[3] = 0 (XCLK_417, default)

ROM_SCLK[0] = 0 (PEX_PLL_EN_TERM100 disabled, default)

ROM_SCLK[1] = 1 (SLT_CLK_CFG, default)

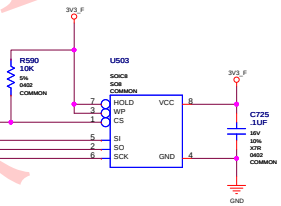
ROM_SCLK[2] = 1 (VBIOS RM present, default)

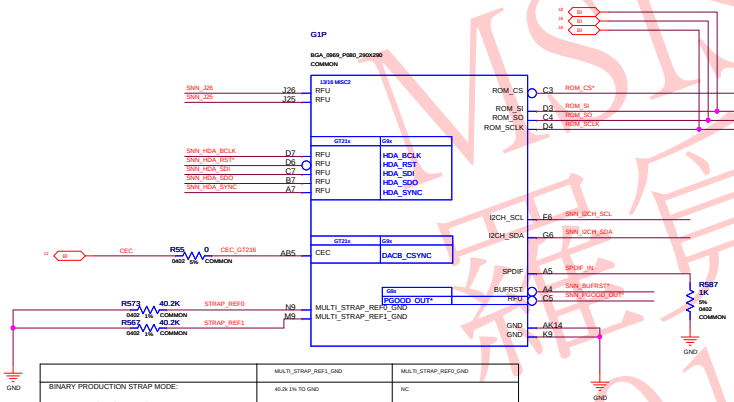
ROM_SCLK[3] = 0 (PCI_DEVID[4] = 0)

ROM_SI[3..0] = RAMCFG[3..0]

0x0001	Qimonda	128-bit, GDDR5
0x0010	Hynix	128-bit, GDDR5
0x0011	Samsung	128-bit, GDDR5

BIOS ROM(serial)





	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION STRAP MODE:	40.2k 1% TO GND	NC
BINARY BRINGUP STRAP MODE:	NC	NC
MULTI-LEVEL STRAP MODE:	40.2k 1% TO GND	40.2k 1% TO GND

MSIS-RMA 羅竟林 20100119

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

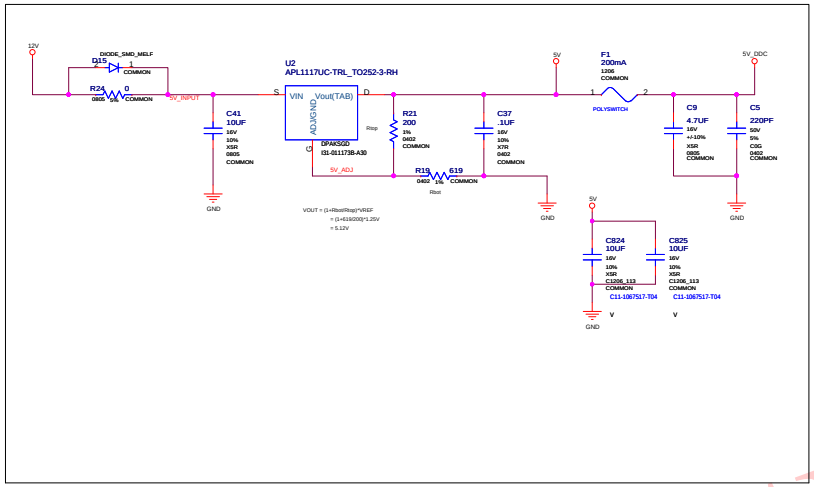
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	VBIOS ROM, INFOROM, STRAPPING OPTIONS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

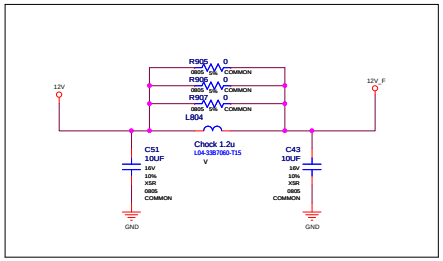
POWER SUPPLY: 5V, 5V_DDC, 1V8, INPUT FILTER

5V REGULATOR

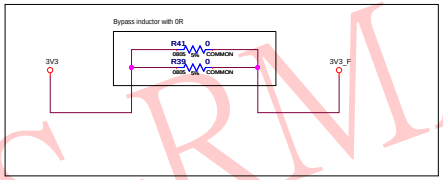


5V DDC

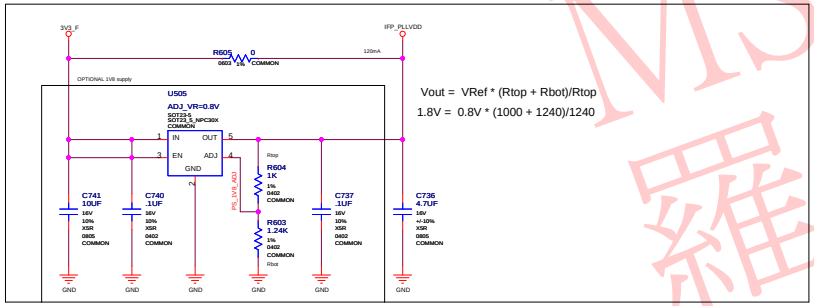
12V filter



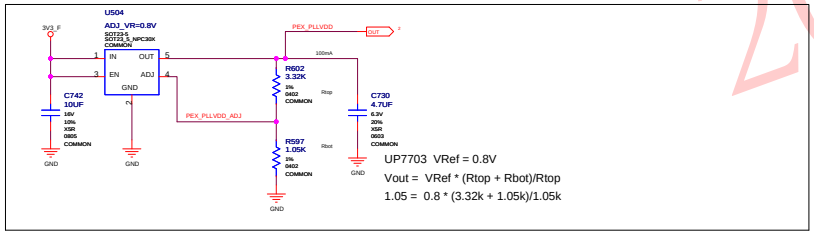
3.3V filter



IFPCEF PLLVDD supply



PEX_PLLVDD (optional)



NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	0.1A	12MIL	5V
5V_INPUT	0.2A	12MIL	5V
PS_1V8_ADJ		10MIL	1.8V
IFPA_IOVDD	0.3A	12MIL	3.2V
12V	6A	20MIL	12V
3V3	3A	12MIL	3.2V
3V3_F	4A	20MIL	3.3V
5V	0.3A	12MIL	5V
5V_DDC	0.1A	12MIL	5V
GND		10MIL	0V

MSIS-RMA
羅覓林
20100119

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	5V, DDC5V, IFP PLLVDD, IFP IOVDD, 3V3 FILTER, 12V FILTER

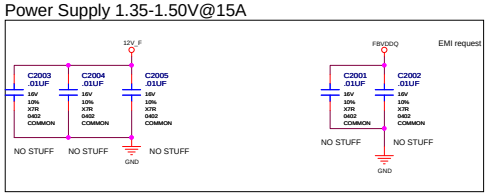
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

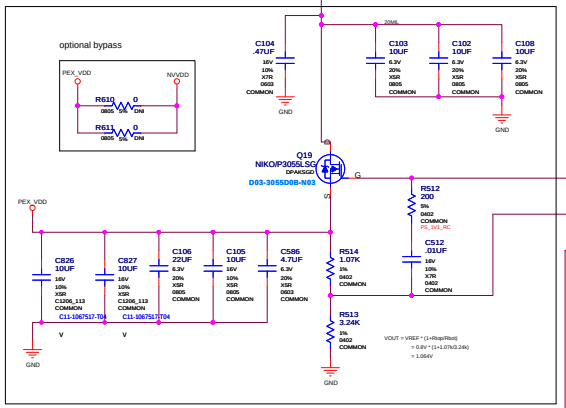
NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

POWER SUPPLY: FBVDDQ, PEX_VDD

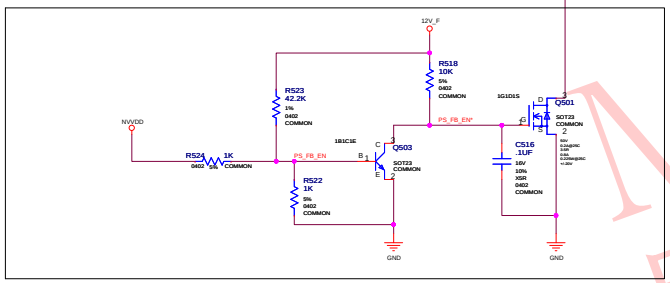
FBVDDQ Power Supply 1.35-1.50V@15A



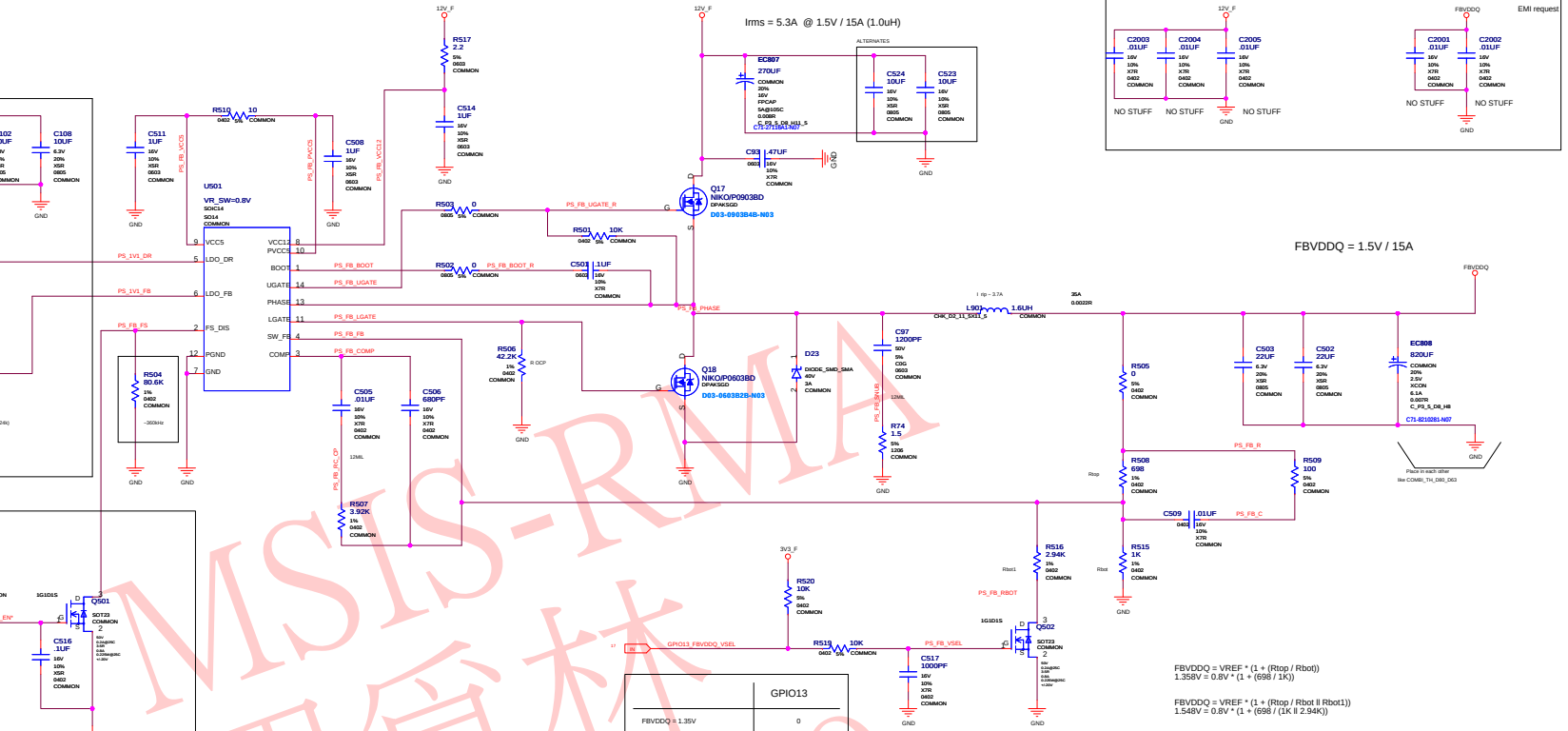
PEXVDD LINEAR



PEXVDD GATING



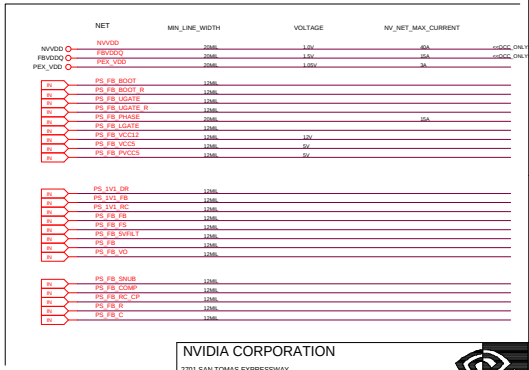
FBVDDQ = 1.5V / 15A



GPIO13	
FBVDDQ = 1.35V	0
FBVDDQ = 1.55V	1

FBVDDQ = VREF * (1 + (Rtop / Rbot))
1.358V = 0.8V * (1 + (698 / 1K))

FBVDDQ = VREF * (1 + (Rtop / Rbot ll Rbot1))
1.548V = 0.8V * (1 + (698 / (1K ll 2.94K))



MSIS-RMA
羅覓林
20100119

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBVDDQ SINGLE PHASE SWITCHER; PEX_VDD LINEAR

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

Title: Basenet Report
Design: design
Date: Jun 9 10:09:58 2009

Base nets and synonyms for
design_lib.DESIGN(@design_lib.design(sch
_1))
Base Signal Location([Zone][dir])

3V3 19.1G
3V3_F 19.1G
3V3_INFOROM 18.4F
3V3_PEX_SVDD 2.5G
3V3_PRSNT 21.2A
5V 19.1G
5V_ADJ 19.2B
5V_DDC 19.1G
5V_DDC_VGA 10.3G
5V_FUSED 19.1G
5V_INPUT 19.1A 19.1G
5V_PHASE 19.2B
12V 19.1G
12V_F 19.1G
12V_PRSNT 21.2A
CEC 12.2D 18.4B
CEC_GT216 18.4B
DACA_BLUE 9.3C 9.5A
DACA_BLUE_C 9.5A 9.5H 11.2G
DACA_GREEN 9.3C 9.5A
DACA_GREEN_C 9.4H 9.5A 11.2G
DACA_HSYNC 9.3C 9.5A
DACA_HSYNC_BUF 9.3D 9.5A
DACA_HSYNC_C 9.3H 9.5A 11.2G
DACA_HSYNC_R 9.3F 9.5A
DACA_RED 9.3C 9.5A
DACA_RED_C 9.4H 9.5A 11.2G
DACA_RSET 9.3B 9.5A
DACA_VDD 9.3B 9.5A
DACA_VREF 9.3B 9.5A
DACA_VSYNC 9.3C 9.5A
DACA_VSYNC_BUF 9.3D 9.5A
DACA_VSYNC_C 9.3H 9.5A 11.2G
DACA_VSYNC_R 9.3F 9.5A
DACB_BLUE 10.3C 10.5A
DACB_BLUE_C 10.5A 10.5G
DACB_GREEN 10.3C 10.5A
DACB_GREEN_C 10.4G 10.5A
DACB_HSYNC 10.3C 10.5A
DACB_HSYNC_BUF 10.3D 10.5A
DACB_HSYNC_C 10.3H 10.5A
DACB_HSYNC_R 10.3E 10.5A
DACB_RED 10.3C 10.5A
DACB_RED_C 10.4G 10.5A
DACB_RSET 10.3B 10.5A
DACB_VDD 10.3B 10.5A
DACB_VREF 10.3B 10.5A
DACB_VSYNC 10.3C 10.5A
DACB_VSYNC_BUF 10.3D 10.5A
DACB_VSYNC_C 10.3H 10.5A
DACB_VSYNC_R 10.3E 10.5A
FAN_PWM 17.1G
FAN_PWM_R 17.1G
FAN_VDD 17.1G
FBA_CLK0 3.4D 4.1F 4.2A
FBA_CLK0* 3.4D 4.1F 4.2A
FBA_CLK0_TERM 4.2B 4.2F
FBA_CLK1 3.4D 4.1F 4.2D
FBA_CLK1* 3.4D 4.1F 4.2D
FBA_CLK1_TERM 4.2E 4.2F
FBA_CMD<0> 3.3C 4.1B
FBA_CMD<30..0> 3.3D 4.1A 4.1D 4.1F
FBA_CMD<1> 3.3C 4.1B
FBA_CMD<2> 3.3C 4.1B
FBA_CMD<3> 3.3C 4.1E
FBA_CMD<4> 3.3C 4.1E
FBA_CMD<5> 3.3C 4.1E
FBA_CMD<6> 3.3C 4.2E 4.2G
FBA_CMD<7> 3.3C 4.1B
FBA_CMD<8> 3.3C 4.2B 4.2E 4.2G
FBA_CMD<9> 3.3C 4.1B
FBA_CMD<10> 3.3C 4.1B
FBA_CMD<11> 3.3C 4.1E
FBA_CMD<12> 3.3C 4.1E
FBA_CMD<13> 3.3C 4.1E
FBA_CMD<14> 3.3C 4.1B
FBA_CMD<15> 3.3C 4.1E
FBA_CMD<16> 3.3C 4.1E
FBA_CMD<17> 3.3C 4.1E
FBA_CMD<18> 3.3C 4.1B
FBA_CMD<19> 3.3C 4.1E
FBA_CMD<20> 3.3C 4.2B 4.2G
FBA_CMD<21> 3.3C 4.1E
FBA_CMD<22> 3.3C 4.1B
FBA_CMD<23> 3.3C 4.1B
FBA_CMD<24> 3.3C 4.1B
FBA_CMD<25> 3.3C 4.1B
FBA_CMD<26> 3.4C 4.1B
FBA_CMD<27> 3.4C 4.1E
FBA_CMD<28> 3.4C 4.1E
FBA_CMD<29> 3.4C 4.1B
FBA_CMD<30> 3.4C 4.1E
FBA_D<0> 3.1B 4.4B
FBA_D<63..0> 3.1A 4.1F 4.4A
FBA_D<1> 3.1B 4.4B
FBA_D<2> 3.1B 4.4B
FBA_D<3> 3.1B 4.4B
FBA_D<4> 3.1B 4.4B
FBA_D<5> 3.1B 4.4B
FBA_D<6> 3.1B 4.4B
FBA_D<7> 3.1B 4.4B
FBA_D<8> 3.1B 4.4B
FBA_D<9> 3.1B 4.4B
FBA_D<10> 3.1B 4.4B
FBA_D<11> 3.1A 4.5B
FBA_D<12> 3.1B 4.5B
FBA_D<13> 3.1B 4.5B
FBA_D<14> 3.1B 4.5B
FBA_D<15> 3.2B 4.5B
FBA_D<16> 3.2B 4.4C
FBA_D<17> 3.2B 4.4C
FBA_D<18> 3.2B 4.4C
FBA_D<19> 3.2B 4.4C
FBA_D<20> 3.2B 4.4C
FBA_D<21> 3.2B 4.4C
FBA_D<22> 3.2B 4.4C
FBA_D<23> 3.2B 4.4C
FBA_D<24> 3.2B 4.4C
FBA_D<25> 3.2B 4.4C
FBA_D<26> 3.2B 4.4C
FBA_D<27> 3.2B 4.5C
FBA_D<28> 3.2B 4.5C
FBA_D<29> 3.2B 4.5C
FBA_D<30> 3.2B 4.5C
FBA_D<31> 3.2B 4.5C
FBA_D<32> 3.2B 4.4D
FBA_D<33> 3.2B 4.4D
FBA_D<34> 3.2B 4.4D
FBA_D<35> 3.2B 4.4D
FBA_D<36> 3.2B 4.4D
FBA_D<37> 3.2B 4.4D
FBA_D<38> 3.2B 4.4D
FBA_D<39> 3.2B 4.4D
FBA_D<40> 3.2B 4.4D
FBA_D<41> 3.2B 4.4D
FBA_D<42> 3.2B 4.5D
FBA_D<43> 3.2B 4.5D
FBA_D<44> 3.3B 10.5A
FBA_D<45> 3.3B 4.5D
FBA_D<46> 3.3B 4.5D
FBA_D<47> 3.3B 4.5D
FBA_D<48> 3.3B
FBA_D<49> 3.3B
FBA_D<50> 3.3B
FBA_D<51> 3.3B
FBA_D<52> 3.3B
FBA_D<53> 3.3B
FBA_D<54> 3.3B
FBA_D<55> 3.3B
FBA_D<56> 3.3B
FBA_D<57> 3.3B
FBA_D<58> 3.3B
FBA_D<59> 3.3B
FBA_D<60> 3.3B
FBA_D<61> 3.3B
FBA_D<62> 3.3B
FBA_D<63> 3.3B
FBA_DBI<0> 3.3B 4.4B
FBA_DBI<7..0> 3.3A 4.1F 4.4A
FBA_DBI<1> 3.3B 4.5B
FBA_DBI<2> 3.3B 4.4C
FBA_DBI<3> 3.3B 4.5C
FBA_DBI<4> 3.3B 4.4D
FBA_DBI<5> 3.3B 4.5D
FBA_DBI<6> 3.3B 4.4E
FBA_DBI<7> 3.3B 4.5E
FBA_DEBUG 3.4D
FBA_DEBUG_SEN0 4.3B
FBA_DEBUG_SEN1 4.3E
FBA_EDC<0> 3.4B 4.4B
FBA_EDC<7..0> 3.4A 4.1F 4.4A
FBA_EDC<1> 3.4B 4.5B
FBA_EDC<2> 3.4B 4.4C
FBA_EDC<3> 3.4B 4.5C
FBA_EDC<4> 3.4B 4.4D
FBA_EDC<5> 3.4B 4.5D
FBA_EDC<6> 3.4B 4.4E
FBA_EDC<7> 3.4B 4.5E
FBA_VREF 3.1F
FBA_VREFC0 4.1F 4.2B
FBA_VREFC1 4.1F 4.2E
FBA_VREFD0 4.2F 4.4F
FBA_VREFD1 4.2F 4.4F
FBA_VREF_PROBE 3.5B
FBA_WCK01 3.4A 4.1F 4.5A
FBA_WCK01* 3.4A 4.1F 4.5A
FBA_WCK01_CT 4.2F 4.5B
FBA_WCK23 3.4A 4.1F 4.5C
FBA_WCK23* 3.4A 4.1F 4.5C
FBA_WCK23_CT 4.2F 4.5C
FBA_WCK45 3.4A 4.1F 4.5D
FBA_WCK45* 3.4A 4.1F 4.5D
FBA_WCK45_CT 4.2F 4.5D
FBA_WCK67 3.4A 4.1F 4.5E
FBA_WCK67* 3.4A 4.1F 4.5E
FBA_WCK67_CT 4.2F 4.5E
FBA_ZQ0 4.2B
FBA_ZQ1 4.2E
FBC_CLK0 6.4D 7.1G 7.2A
FBC_CLK0* 6.4D 7.1G 7.2A
FBC_CLK0_TERM 7.2B 7.2G
FBC_CLK1 6.4D 7.1G 7.2D
FBC_CLK1* 6.4D 7.1G 7.2D
FBC_CLK1_TERM 7.2E 7.2G
FBC_CMD<0> 6.3C 7.1B
FBC_CMD<30..0> 6.3D 7.1A 7.1D 7.1G
FBC_CMD<1> 6.3C 7.1B
FBC_CMD<2> 6.3C 7.1B
FBC_CMD<3> 6.3C 7.1E
FBC_CMD<4> 6.3C 7.1E
FBC_CMD<5> 6.3C 7.1E
FBC_CMD<6> 6.3C 7.2E 7.2G
FBC_CMD<7> 6.3C 7.1B
FBC_CMD<8> 6.3C 7.2B 7.2E 7.2G
FBC_CMD<9> 6.3C 7.1B
FBC_CMD<10> 6.3C 7.1B
FBC_CMD<11> 6.3C 7.1E
FBC_CMD<12> 6.3C 7.1E
FBC_CMD<13> 6.3C 7.1E
FBC_CMD<14> 6.3C 7.1B
FBC_CMD<15> 6.3C 7.1E
FBC_CMD<16> 6.3C 7.1E
FBC_CMD<17> 6.3C 7.1E
FBC_CMD<18> 6.3C 7.1B
FBC_CMD<19> 6.3C 7.1E
FBC_CMD<20> 6.3C 7.2B 7.2G
FBC_CMD<21> 6.3C 7.1E
FBC_CMD<22> 6.3C 7.1B
FBC_CMD<23> 6.4C 7.1B
FBC_CMD<24> 6.4C 7.1B
FBC_CMD<25> 6.4C 7.1B
FBC_CMD<26> 6.4C 7.1B
FBC_CMD<27> 6.4C 7.1E
FBC_CMD<28> 6.4C 7.1E
FBC_CMD<29> 6.4C 7.1B
FBC_CMD<30> 6.4C 7.1E
FBC_D<0> 6.1A 7.4B
FBC_D<63..0> 6.1A 7.1G 7.4A
FBC_D<1> 6.1A 7.4B
FBC_D<2> 6.1A 7.4B
FBC_D<3> 6.1A 7.4B
FBC_D<4> 6.1A 7.4B
FBC_D<5> 6.1A 7.4B
FBC_D<6> 6.1A 7.4B
FBC_D<7> 6.1A 7.4B
FBC_D<8> 6.1A 7.4B
FBC_D<9> 6.1A 7.4B
FBC_D<10> 6.1A 7.4B
FBC_D<11> 6.1A 7.4B
FBC_D<12> 6.1A 7.5B
FBC_D<13> 6.1A 7.5B
FBC_D<14> 6.1A 7.5B
FBC_D<15> 6.2A 7.5B
FBC_D<16> 6.2A 7.4C
FBC_D<17> 6.2A 7.4C
FBC_D<18> 6.2A 7.4C
FBC_D<19> 6.2A 7.4C
FBC_D<20> 6.2A 7.4C
FBC_D<21> 6.2A 7.4C
FBC_D<22> 6.2A 7.4C
FBC_D<23> 6.2A 7.4C
FBC_D<24> 6.2A 7.4C
FBC_D<25> 6.2A 7.4C
FBC_D<26> 6.2A 7.4C
FBC_D<27> 6.2A 7.4C
FBC_D<28> 6.2A 7.5C
FBC_D<29> 6.2A 7.5C
FBC_D<30> 6.2A 7.5C
FBC_D<31> 6.2A 7.5C
FBC_D<32> 6.2A 7.4D
FBC_D<33> 6.2A 7.4D
FBC_D<34> 6.2A 7.4D
FBC_D<35> 6.2A 7.4D
FBC_D<36> 6.2A 7.4D
FBC_D<37> 6.2A 7.4D
FBC_D<38> 6.2A 7.4D
FBC_D<39> 6.2A 7.4D
FBC_D<40> 6.2A 7.4D
FBC_D<41> 6.2A 7.4D
FBC_D<42> 6.2A 7.4D
FBC_D<43> 6.2A 7.4D
FBC_D<44> 6.2A 7.5D
FBC_D<45> 6.3A 7.5D
FBC_D<46> 6.3A 7.5D
FBC_D<47> 6.3A 7.5D
FBC_D<48> 6.3A
FBC_D<49> 6.3A
FBC_D<50> 6.3A
FBC_D<51> 6.3A
FBC_D<52> 6.3A
FBC_D<53> 6.3A
FBC_D<54> 6.3A
FBC_D<55> 6.3A
FBC_D<56> 6.3A
FBC_D<57> 6.3A
FBC_D<58> 6.3A
FBC_D<59> 6.3A
FBC_D<60> 6.3A
FBC_D<61> 6.3A
FBC_D<62> 6.3A
FBC_D<63> 6.3A
FBC_DBI<0> 6.3A 7.4B
FBC_DBI<7..0> 6.3A 7.1G 7.4A
FBC_DBI<1> 6.3A 7.5B
FBC_DBI<2> 6.3A 7.4C
FBC_DBI<3> 6.3A 7.5C
FBC_DBI<4> 6.3A 7.4D
FBC_DBI<5> 6.3A 7.5D
FBC_DBI<6> 6.3A 7.4E
FBC_DBI<7> 6.3A 7.5E
FBC_DEBUG 6.4C
FBC_DEBUG_SEN0 7.3B
FBC_DEBUG_SEN1 7.3E
FBC_EDC<0> 6.4A 7.4B
FBC_EDC<7..0> 6.4A 7.1G 7.4A
FBC_EDC<1> 6.4A 7.5B
FBC_EDC<2> 6.4A 7.4C
FBC_EDC<3> 6.4A 7.5C
FBC_EDC<4> 6.4A 7.4D
FBC_EDC<5> 6.4A 7.5D
FBC_EDC<6> 6.4A 7.4E
FBC_EDC<7> 6.4A 7.5E
FBC_VREFC0 7.1G 7.2B
FBC_VREFC1 7.1G 7.2E
FBC_VREFD0 7.1G 7.4F
FBC_VREFD1 7.2G 7.4F
FBC_WCK01 6.4A 7.1G 7.5A
FBC_WCK01* 6.4A 7.1G 7.5A
FBC_WCK01_CT 7.2G 7.5B
FBC_WCK23 6.4A 7.1G 7.5C
FBC_WCK23* 6.4A 7.1G 7.5C
FBC_WCK23_CT 7.2G 7.5C
FBC_WCK45 6.4A 7.1G 7.5D
FBC_WCK45* 6.4A 7.1G 7.5D
FBC_WCK45_CT 7.2G 7.5D
FBC_WCK67 6.4A 7.1G 7.5E
FBC_WCK67* 6.5A 7.1G 7.5E
FBC_WCK67_CT 7.2G 7.5F
FBC_ZQ0 7.2B
FBC_ZQ1 7.3E
FBVDDQ 20.4A
FB_CAL_PD 6.1G
FB_CAL_PD_VDDQ 6.5C
FB_CAL_PU 6.1G
FB_CAL_PU_GND 6.5C
FB_CAL_TERM 6.1G
FB_CAL_TERM_GND 6.5C
FB_PLLAVDD 3.1F 3.5C
GPIO0_HPD_DVI_1 11.3D
GPIO0_HPD_DVI_1_R 11.3E
GPIO0_HPD_DVI_1_RL 11.2G
GPIO1_HPDC 12.3C
GPIO1_HPDC_R 12.3E
GPIO1_HPDC_R_L_1 12.3F
GPIO9 17.3C
GPIO4_FAN_TACH 17.3C
GPIO4_FAN_TACH_R 17.3F 17.3H
GPIO5_VSEL0 17.3D 21.1A
GPIO5_VSEL_R 21.1A
GPIO6_VSEL1 17.3D 21.4A
GPIO6_VSEL1_R 21.4A
GPIO7_VSEL2 17.3D 21.3A
GPIO9_NPN_B 17.2B
GPIO9_PNP_B 17.1B
GPIO9_PNP_C 17.1B
GPIO9_THERM_ALERT* 17.2E 21.3A
GPIO9_THERM_OVERTM 17.3C
I²*
GPIO9_FAN_PWM_R 17.3H 17.4F
GPIO10_VREF_SEL 17.3C
GPIO13_FBVDDQ_VSEL 17.4D 20.4E
GPIO14 17.4C
GPIO16_FAN_PWM 17.4C
GPIO23_RESERVED 17.4C
GPIOX_FAN_PWM_Q 17.4G
GPIOX_FAN_PWM_Q_L 17.4H
GPU_PLLVDD 16.1B 16.5G
GPU_PLLVDD_SP 16.1B 16.5G
GPU_RST* 2.2D 11.5D 17.2A
GPU_RST_R* 17.2B
GPU_RST_R_Q 17.2B
GPU_TESTMODE 2.5E
HDMI_CEC_C_1 12.3G
HDMI_CEC_Q 12.2E
HDMI_PD_1 12.4E
I2CA_SCL 9.2D 9.3C
I2CA_SCL_C 9.2H 11.2G
I2CA_SCL_T 9.2F
I2CA_SDA 9.2D 9.3C
I2CA_SDA_C 9.2H 11.2G
I2CA_SDA_T 9.2F
I2CB_SCL 10.3C
I2CB_SCL_R 10.2E
I2CB_SCL_R_L 10.2H
I2CB_SDA 10.3C
I2CB_SDA_R 10.2E
I2CB_SDA_R_L 10.2H
I2CC_SCL 17.3F 18.4D
I2CC_SCL_G 17.3C
I2CC_SCL_ROM 18.4E
I2CC_SDA 17.3F 18.4D
I2CC_SDA_G 17.3C
I2CC_SDA_ROM 18.4E
I2CS_SCL 2.1C 17.3F
I2CS_SDA 2.2C 17.3F
I2CW_SCL 12.2C
I2CW_SCL_R 12.1D 12.1G
I2CW_SCL_R_Q 12.1F 12.1H
I2CW_SDA 12.2C
I2CW_SDA_R 12.1D 12.1G
I2CW_SDA_R_Q 12.1F 12.1H
IFPAB_IOVDD 11.2B 11.5A
IFPAB_PLLVDD 11.2B 11.5A
IFPAB_RSET 11.2B 11.5A
IFPA_IOVDD 19.1G
IFPA_IOVDD_EN* 11.4E
IFPA_IOVDD_EN_RC 11.4E
IFPA_TXC 11.2D 11.5A
IFPA_TXC* 11.2D 11.4A
IFPA_TXD0 11.1D 11.5A
IFPA_TXD0* 11.1D 11.5A
IFPA_TXD1 11.1D 11.5A
IFPA_TXD1* 11.1D 11.5A
IFPA_TXD2 11.2D 11.5A
IFPA_TXD2* 11.2D 11.5A
IFPA_TXD4 11.2D 11.5A
IFPA_TXD4* 11.2D 11.5A
IFPB_TXD5 11.2D 11.5A
IFPB_TXD5* 11.2D 11.5A
IFPB_TXD6 11.2D 11.5A
IFPB_TXD6* 11.2D 11.5A
IFPC_IOVDD 12.3B 12.5A
IFPC_PLLVDD 12.2B
IFPC_RSET 12.2B 12.5A
IFPC_TERM_ENA 12.4D
IFPC_TXC 12.3C 12.4A
IFPC_TXC* 12.3C 12.4A
IFPC_TXC_C1 12.3E 12.4F 12.5A
IFPC_TXC_C1* 12.3E 12.4F 12.5A
IFPC_TXD0 12.3C 12.5A
IFPC_TXD0* 12.3C 12.5A
IFPC_TXD0_C1 12.3E 12.4F 12.5A
IFPC_TXD0_C1* 12.3E 12.4F 12.5A
IFPC_TXD1 12.3C 12.5A
IFPC_TXD1* 12.3C 12.5A
IFPC_TXD1_C1 12.3E 12.4F 12.5A
IFPC_TXD1_C1* 12.3E 12.4F 12.5A
IFPC_TXD2 12.3C 12.5A
IFPC_TXD2* 12.3C 12.5A
IFPC_TXD2_C1 12.3E 12.4F 12.5A
IFPC_TXD2_C1* 12.3E 12.4F 12.5A
IFPD_IOVDD 13.3D
IFPD_PLLVDD 13.2D
IFPEF_IOVDD 14.3C
IFPEF_PLLVDD 14.2C
JTAG_TCLK 2.1C 17.4A
JTAG_TDI 2.1C 17.4A
JTAG_TDO 2.1C 17.5A
JTAG_TMS 2.1C 17.4A
JTAG_TRST* 2.1C 17.5A
MIOA_CLKIN 15.2D
MIOA_VDDQ 15.1B
MIOB_CLKIN 15.4D
NVVDD 20.4A
NVVDD_BOOT1 21.3D 21.5A
NVVDD_BOOT1_C 21.3D 21.5A
NVVDD_BOOT2 21.3D 21.5A
NVVDD_BOOT2_C 21.3D 21.5A
NVVDD_CMP 21.4C 21.5B
NVVDD_CSN 21.4D
NVVDD_CSP 21.4D
NVVDD_EAP 21.4C 21.5B
NVVDD_ENA 21.3C
NVVDD_ENA1 21.2A
NVVDD_ENA2 21.2B
NVVDD_ENA3 21.2A
NVVDD_FB 21.5B 21.5C
NVVDD_FBRTN 21.4C 21.5B
NVVDD_FB_R 21.5B 21.5D
NVVDD_GND_SENSE 2.4F 21.4A
NVVDD_IOFS 21.3C
NVVDD_LG1 21.3D 21.5A
NVVDD_LG2 21.3D 21.5A
NVVDD_PH1 21.3D 21.5A
NVVDD_PH2 21.3D 21.5A
NVVDD_PSI 21.3C
NVVDD_PSI_R 21.1B
NVVDD_RB1 21.4B
NVVDD_RC1 21.4C 21.5B
NVVDD_RC2 21.5B 21.5C
NVVDD_REFIN 21.3C 21.5B
NVVDD_RSET 21.3C
NVVDD_SENSE 2.4F 21.4A
NVVDD_SNUB1 21.3G 21.5B
NVVDD_SNUB2 21.5B 21.5G
NVVDD_SS 21.4C 21.5B
NVVDD_UG1 21.3D 21.5A
NVVDD_UG1_R 21.3E 21.5A
NVVDD_UG2 21.3D 21.5A
NVVDD_UG2_R 21.4E 21.5A
NVVDD_VCC9 21.3C 21.5A
NVVDD_VCC12 21.2C 21.5A
NVVDD_VID 21.3C
NVVDD_VREF 21.4C 21.5B
PEX_CLKREQ* 2.1D
PEX_PLLVDD 2.4E 2.5G 19.5B
PEX_PLLVDD_ADJ 19.5A
PEX_PLL_CLK_OUT 2.1G 2.2C
PEX_PLL_CLK_OUT* 2.1G 2.2C
PEX_PRSNT1* 2.1A
PEX_REFCLK 2.1G 2.2B
PEX_REFCLK* 2.1G 2.2B
PEX_RX0 2.2B 2.4G
PEX_RX0* 2.2B 2.4G
PEX_RX1 2.2B 2.4G
PEX_RX1* 2.2B 2.4G
PEX_RX2 2.2B 2.4G
PEX_RX2* 2.3B 2.4G
PEX_RX3 2.3B 2.4G
PEX_RX3* 2.3B 2.4G
PEX_RX4 2.3B 2.4G
PEX_RX4* 2.3B 2.4G
PEX_RX5 2.3B 2.4G
PEX_RX5* 2.3B 2.4G
PEX_RX6 2.3B 2.4G
PEX_RX6* 2.3B 2.4G
PEX_RX7 2.4B 2.4G
PEX_RX7* 2.4B 2.4G
PEX_RX8 2.4B 2.4G
PEX_RX8* 2.4B 2.4G
PEX_RX9 2.4B 2.4G
PEX_RX9* 2.4B 2.4G
PEX_RX10 2.4B 2.4G
PEX_RX10* 2.4B 2.4G
PEX_RX11 2.4B 2.4G
PEX_RX11* 2.4B 2.4G
PEX_RX12 2.4B 2.5G
PEX_RX12* 2.5B 2.5G
PEX_RX13 2.5B 2.5G
PEX_RX13* 2.5B 2.5G
PEX_RX14 2.5B 2.5G
PEX_RX14* 2.5B 2.5G
PEX_RX15 2.5B 2.5G
PEX_RX15* 2.5B 2.5G
PEX_SMCLK 2.1B
PEX_SMDAT 2.1B
PEX_TCK 2.1B
PEX_TDI 2.1B
PEX_TDO 2.1B
PEX_TERMP 2.5E
PEX_TMS 2.1B
PEX_TRST* 2.1B
PEX_TX0 2.1G 2.2D
PEX_TX0* 2.1G 2.2C
PEX_TX1 2.1C 17.4A
PEX_TX1* 2.1G 2.2C
PEX_TX2 2.2D 2.2G
PEX_TX2* 2.2C 2.2G
PEX_TX3 2.2G 2.3D
PEX_TX3* 2.2G 2.3C
PEX_TX4 2.2G 2.3D
PEX_TX4* 2.2G 2.3C
PEX_TX5 2.2G 2.3D
PEX_TX5* 2.2G 2.3C
PEX_TX6 2.2G 2.3D
PEX_TX6* 2.2G 2.3C
PEX_TX7 2.2G 2.3D
PEX_TX7* 2.2G 2.3C
PEX_TX8 2.2G 2.4B
PEX_TX8* 2.2G 2.4C
PEX_TX9 2.2G 2.4D
PEX_TX9* 2.2G 2.4C
PEX_TX10 2.2G 2.4D
PEX_TX10* 2.2G 2.4C
PEX_TX11 2.2G 2.4D
PEX_TX11* 2.2G 2.4C
PEX_TX12 2.2G 2.4D
PEX_TX12* 2.2G 2.4B
PEX_TX13 2.2G 2.5B
PEX_TX13* 2.2G 2.5B
PEX_TX14 2.2G 2.5B
PEX_TX14* 2.4G 2.5B
PEX_TX15 2.4G 2.5B
PEX_TX15* 2.4G 2.5B
PEX_VDD 20.4A
PS_1V1_DR 20.2C 20.5A
PS_1V1_FB 20.2C 20.5A
PS_1V1_RC 20.2B 20.5A
PS_1V8_ADJ 19.1G 19.4B
PS_FB 20.5A
PS_FB_5VFILT 20.5A
PS_FB_BOOT 20.2D 20.4A
PS_FB_BOOT_R 20.2D 20.4A
PS_FB_C 20.3G 20.5A
PS_FB_COMP 20.2D 20.5A
PS_FB_EN 20.4B
PS_FB_EN* 20.3B
PS_FB_FB 20.2D 20.5A
PS_FB_FS 20.2C 20.5A
PS_FB_LGATE 20.2D 20.5A
PS_FB_PHASE 20.2E 20.5A
PS_FB_PVCCS 20.2D 20.5A
PS_FB_R 20.3G 20.5A
PS_FB_RBOT 20.4F
PS_FB_RC_CP 20.3D 20.5A
PS_FB_SNUB 20.3F 20.5A
PS_FB_UGATE 20.2D 20.5A
PS_FB_UGATE_R 20.2E 20.5A
PS_FB_VCCS 20.2C 20.5A
PS_FB_VCC12 20.2D 20.5A
PS_FB_VO 20.5A
PS_FB_VSEL 20.4F
ROM_CS* 18.3C
ROM_SCLK 18.2D 18.3C 18.3C
ROM_SI 18.2D 18.3C 18.3C
ROM_SO 18.2D 18.3C 18.3C
SNN_BIOB_HSYNC 15.4D
SNN_BTXC 11.3D
SNN_BTXC* 11.3D
SNN_BUFRST* 18.4C
SNN_FBAM0_RFU_A5 4.2B
SNN_FBAM0_RFU_V5 4.2B
SNN_FBAM1_RFU_A5 4.2E
SNN_FBAM1_RFU_V5 4.2E
SNN_FBA_DQS_RN<0> 3.4B
SNN_FBA_DQS_RN<1> 3.4B
SNN_FBA_DQS_RN<2> 3.4B
SNN_FBA_DQS_RN<3> 3.4B
SNN_FBA_DQS_RN<4> 3.4B
SNN_FBA_DQS_RN<5> 3.4B
SNN_FBA_DQS_RN<6> 3.4B

NVISI-RMA 羅冠林 20091

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	<edit here to insert page detail>

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME	<ENGINEER>	DATE	01-JUL-2009

SNN_FBA_DQS_RN<7> 3.4B
SNN_FBCM0_RFU_A5 7.2B
SNN_FBCM0_RFU_V5 7.2B
SNN_FBCM1_RFU_A5 7.2E
SNN_FBCM1_RFU_V5 7.2E
SNN_FBC_DQS_RN<0> 6.4A
SNN_FBC_DQS_RN<1> 6.4A
SNN_FBC_DQS_RN<2> 6.4A
SNN_FBC_DQS_RN<3> 6.4A
SNN_FBC_DQS_RN<4> 6.4A
SNN_FBC_DQS_RN<5> 6.4A
SNN_FBC_DQS_RN<6> 6.4A
SNN_FBC_DQS_RN<7> 6.4A
SNN_GND_SENSE_1 2.4E
SNN_GND_SENSE_3 2.4E
SNN_GPIO2_RESERVED 17.3C
SNN_GPIO9 17.3C
SNN_GPIO11 17.3C
SNN_GPIO12 17.3C
SNN_GPIO15 14.3E
SNN_GPIO17_RESERVE 17.4C
D
SNN_GPIO18_RESERVE 17.4C
D
SNN_GPIO19 13.3E
SNN_GPIO20_RESERVE 17.4C
D
SNN_GPIO21 14.3E
SNN_GPIO22 17.4C
SNN_HDA_BCLK 18.3B
SNN_HDA_RST* 18.3B
SNN_HDA_SDI 18.3B
SNN_HDA_SDO 18.3B
SNN_HDA_SYNC 18.3B
SNN_HDMI_RSVD1 12.2G
SNN_I2CD_SCL 17.3C
SNN_I2CD_SDA 17.3C
SNN_I2CE_SCL 17.3C
SNN_I2CE_SDA 17.3C
SNN_I2CH_SCL 18.4C
SNN_I2CH_SDA 18.4C
SNN_IFPA_TXD3 11.2D
SNN_IFPA_TXD3* 11.2D
SNN_IFPB_TXD7 11.2D
SNN_IFPB_TXD7* 11.2D
SNN_IFPCD_RSET 13.2C
SNN_IFPD_AUX 13.2E
SNN_IFPD_AUX* 13.2E
SNN_IFPD_L0 13.3E
SNN_IFPD_L0* 13.3E
SNN_IFPD_L1 13.3E
SNN_IFPD_L1* 13.3E
SNN_IFPD_L2 13.3E
SNN_IFPD_L2* 13.3E
SNN_IFPD_L3 13.3E
SNN_IFPD_L3* 13.3E
SNN_IFPEF_RSET 14.2C
SNN_IFPE_AUX 14.2E
SNN_IFPE_AUX* 14.2E
SNN_IFPE_L0 14.3E
SNN_IFPE_L0* 14.3E
SNN_IFPE_L1 14.3E
SNN_IFPE_L1* 14.2E
SNN_IFPE_L2 14.2E
SNN_IFPE_L2* 14.2E
SNN_IFPE_L3 14.2E
SNN_IFPE_L3* 14.2E
SNN_IFPF_AUX 14.3E
SNN_IFPF_AUX* 14.3E
SNN_IFPF_L0 14.3E
SNN_IFPF_L0* 14.3E
SNN_IFPF_L1 14.3E
SNN_IFPF_L1* 14.3E
SNN_IFPF_L2 14.3E
SNN_IFPF_L2* 14.3E
SNN_IFPF_L3 14.3E
SNN_IFPF_L3* 14.3E
SNN_J25 18.3B
SNN_J26 18.3B
SNN_MIOAD<0> 15.1D
SNN_MIOAD<1> 15.1D
SNN_MIOAD<2> 15.1D
SNN_MIOAD<3> 15.1D
SNN_MIOAD<4> 15.2D
SNN_MIOAD<5> 15.2D
SNN_MIOAD<6> 15.2D
SNN_MIOAD<7> 15.2D
SNN_MIOAD<8> 15.2D
SNN_MIOAD<9> 15.2D
SNN_MIOAD<10> 15.2D
SNN_MIOAD<11> 15.2D
SNN_MIOAD<12> 15.2D
SNN_MIOAD<13> 15.2D
SNN_MIOAD<14> 15.2D
SNN_MIOA_CAL_PD_VD 15.2B
DQ

SNN_MIOA_CAL_PU_GN 15.2B
D
SNN_MIOA_CKOUT 15.2D
SNN_MIOA_CKOUT* 15.2D
SNN_MIOA_CTL3 15.2D
SNN_MIOA_DE 15.2D
SNN_MIOA_HSYNC 15.2D
SNN_MIOA_VREF 15.2B
SNN_MIOA_VSYNC 15.2D
SNN_MIOB<0> 15.3D
SNN_MIOB<1> 15.3D
SNN_MIOB<2> 15.3D
SNN_MIOB<3> 15.3D
SNN_MIOB<4> 15.3D
SNN_MIOB<5> 15.3D
SNN_MIOB<6> 15.3D
SNN_MIOB<7> 15.3D
SNN_MIOB<8> 15.3D
SNN_MIOB<9> 15.3D
SNN_MIOB<10> 15.3D
SNN_MIOB<11> 15.3D
SNN_MIOBD<12> 15.3D
SNN_MIOBD<13> 15.3D
SNN_MIOBD<14> 15.3D
SNN_MIOB_CAL_PD_VD 15.3B
DQ
SNN_MIOB_CAL_PU_GN 15.3B
D
SNN_MIOB_CLKOUT 15.4D
SNN_MIOB_CLKOUT* 15.4D
SNN_MIOB_CTL3 15.4D
SNN_MIOB_DE 15.4D
SNN_MIOB_VREF 15.4B
SNN_MIOB_VSYNC 15.4D
SNN_NC<1> 2.2E
SNN_NC<2> 2.2E
SNN_NC<3> 2.2E
SNN_NC<4> 2.2E
SNN_NC<5> 2.3E
SNN_NC<6> 2.3E
SNN_NC<7> 2.3E
SNN_NC<8> 2.3E
SNN_NC<9> 2.3E
SNN_NC<10> 2.3E
SNN_NC<11> 2.3E
SNN_NC<14> 2.3E
SNN_NC<16> 2.3E
SNN_NC<17> 2.3E
SNN_NC<18> 2.3E
SNN_NC<21> 2.3E
SNN_NC<22> 2.3E
SNN_NC<23> 2.3E
SNN_NCP1402_NC 19.2A
SNN_PCA9515 12.1G
SNN_PCA9515_EN 12.1H
SNN_PEX_RFU2 2.5E
SNN_PEX_WAKE* 2.2B
SNN_PE_PRSNT2_A 2.1A
SNN_PE_PRSNT2_B 2.2A
SNN_PE_PRSNT2_C 2.3A
SNN_PE_RSVD2 2.2A
SNN_PE_RSVD3 2.2A
SNN_PE_RSVD4 2.2A
SNN_PE_RSVD5 2.2A
SNN_PE_RSVD6 2.3A
SNN_PE_RSVD7 2.4A
SNN_PE_RSVD8 2.4A
SNN_PGOOD_OUT* 18.4C
SNN_RFU_1 6.5D
SNN_RFU_2 6.5D
SNN_VDD_SENSE_1 2.4E
SNN_VDD_SENSE_3 2.4E
SNN_VGA_1_ID0 10.9H
SNN_VGA_1_ID2 10.4G
SNN_VGA_2_ID0 10.4H
SNN_VGA_2_ID2 10.5G
SPDIF_IN 18.4C
STRAP0 15.4E 18.2B
STRAP1 15.4E 18.2B
STRAP2 15.4E 18.2B
STRAP_REF0 18.4B
STRAP_REF1 18.4B
THERM_DA 17.1G
THERM_DA_R 17.1G
THERM_DC 17.1G
THERM_DC_R 17.1G
TS_THERM_DA 17.3B
TS_THERM_DC 17.3B
XTAL_IN 16.2C 16.5G
XTAL_OUT 16.2D 16.5G
XTAL_OUTBUFF 16.2D 16.5G
XTAL_SSIN 16.2B 16.5G

MSIS-RMA
羅覓林
20100119

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	<edit here to insert page detail>

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME	<ENGINEER>	DATE	01-JUL-2009

Title: Cnxf Part
Report
Design: design
Date: Jun 9
10:09:58 2009

BKT1001 [16.1F]
C1 [21.4E]
C2 [21.4F]
C3 [10.3H]
C4 [21.2F]
C5 [20.2H]
C6 [20.2B]
C7 [10.2G]
C8 [10.2G]
C9 [20.2H]
C10 [12.2A]
C11 [12.2A]
C12 [20.4C]
C13 [15.2B]
C14 [10.2C]
C15 [10.2C]
C16 [19.2A]
C17 [19.2C]
C18 [19.2C]
C43 [21.2A]
C47 [21.2A]
C52 [21.1B]
C53 [21.4B]
C83 [21.4E]
C85 [21.3D]
C89 [20.2F]
C91 [20.2E]
C94 [21.2C]
C98 [20.1E]
C100 [9.3G]
C148 [21.2C]
C149 [21.3D]
C150 [21.2D]
C153 [21.2F]
C155 [21.4F]
C158 [21.2G]
C161 [21.5H]
C163 [21.3H]
C164 [21.5H]
C165 [21.4H]
C190 [9.3G]
C191 [21.3B]
C250 [21.4C]
C256 [21.4D]
C257 [21.4D]
C258 [12.1D]
C259 [17.2D]
C506 [20.1F]
C507 [20.1F]
C511 [21.3G]
C521 [21.4H]
C531 [21.4H]
C532 [20.2E]
C535 [20.3D]
C536 [20.3D]
C537 [20.2D]
C538 [20.3G]
C539 [20.2G]
C540 [20.2G]
C541 [20.2C]
C543 [20.2D]
C546 [21.4G]
C548 [20.4F]
C552 [21.4F]
C1001 [12.2G]
C1002 [9.2G]
C1004 [9.2G]
C1010 [12.3E]
C1011 [11.3F]
C1013 [12.3E]
C1015 [9.2B]
C1016 [11.3E]
C1017 [9.3E]
C1018 [19.1C]
C1019 [19.1C]
C1020 [19.1C]
C1021 [19.1B]
C1022 [19.1A]
C1031 [11.5E]
C1033 [2.3E]
C1034 [10.3A]
C1035 [11.2A]
C1038 [2.1A]
C1039 [16.2D]
C1040 [16.2C]
C1042 [11.2A]
C1044 [9.3A]
C1045 [10.3B]
C1046 [7.3A]

C1048 [16.2B]
C1049 [2.1A]
C1050 [10.3A]
C1051 [11.2B]
C1054 [10.3A]
C1055 [11.2B]
C1056 [7.4G]
C1057 [2.2A]
C1058 [9.3B]
C1059 [7.5B]
C1060 [7.5D]
C1061 [18.4F]
C1062 [7.5E]
C1063 [7.5F]
C1064 [7.5G]
C1065 [7.3D]
C1066 [4.5B]
C1067 [4.5F]
C1068 [4.3A]
C1069 [4.3D]
C1070 [17.4G]
C1071 [17.4H]
C1072 [4.5D]
C1073 [19.2D]
C1074 [4.5E]
C1075 [4.5G]
C1077 [21.5G]
C1084 [20.2A]
C1092 [21.4C]
C1094 [21.3H]
C1512 [21.5C]
C1517 [20.2B]
C1518 [20.2A]
C1519 [20.2A]
C1523 [20.2B]
C1524 [20.2B]
C1525 [20.2B]
C1526 [20.2C]
C1533 [21.2F]
C1551 [19.2E]
C1555 [5.1E]
C1556 [5.2C]
C1557 [5.2E]
C1558 [5.2F]
C1559 [5.3D]
C1560 [2.5C]
C1561 [5.2C]
C1562 [5.3E]
C1563 [5.3E]
C1564 [2.5C]
C1565 [5.1F]
C1566 [5.1C]
C1567 [5.2D]
C1568 [5.2E]
C1569 [5.2C]
C1570 [5.3C]
C1571 [2.5C]
C1572 [5.1F]
C1573 [5.2F]
C1574 [2.5C]
C1575 [5.2E]
C1576 [4.2E]
C1577 [5.3D]
C1578 [17.3H]
C1579 [5.3D]
C1580 [4.2B]
C1581 [5.2C]
C1582 [5.2E]
C1583 [2.5C]
C1584 [5.3D]
C1585 [2.5C]
C1586 [5.2C]
C1587 [5.2E]
C1588 [5.2C]
C1589 [5.1C]
C1590 [5.2F]
C1591 [5.2E]
C1592 [5.2C]
C1593 [5.2C]
C1594 [5.3C]
C1595 [2.4C]
C1596 [5.1C]
C1597 [5.3C]
C1598 [5.2C]
C1599 [5.3C]
C1600 [5.1D]
C1601 [5.2E]
C1602 [5.1E]
C1603 [5.1E]
C1604 [5.2E]
C1605 [2.4C]
C1606 [5.1C]
C1607 [5.2C]
C1609 [4.4G]
C1610 [2.4C]
C1611 [2.4C]

C1612 [2.4C]
C1613 [2.4C]
C1614 [7.2E]
C1615 [2.4C]
C1616 [2.4C]
C1617 [2.1G]
C1618 [2.4C]
C1619 [2.1G]
C1620 [8.2E]
C1621 [2.4C]
C1622 [8.2E]
C1623 [8.3D]
C1624 [8.3E]
C1625 [8.2F]
C1626 [3.2D]
C1627 [2.1F]
C1628 [8.2F]
C1629 [2.3C]
C1630 [2.3C]
C1631 [3.2E]
C1632 [8.2E]
C1633 [8.1F]
C1634 [8.3D]
C1635 [8.1F]
C1636 [3.5D]
C1637 [2.3C]
C1638 [3.2D]
C1639 [8.2E]
C1640 [3.2D]
C1641 [2.1F]
C1642 [2.3C]
C1643 [8.3E]
C1644 [8.2F]
C1645 [3.2E]
C1646 [8.2F]
C1647 [8.1E]
C1648 [2.3C]
C1649 [3.1D]
C1650 [2.3C]
C1651 [8.1E]
C1652 [3.1E]
C1653 [3.5D]
C1654 [8.3D]
C1655 [3.1E]
C1656 [3.1E]
C1657 [3.2E]
C1658 [3.2D]
C1659 [3.1D]
C1660 [2.3C]
C1661 [3.2D]
C1662 [3.2D]
C1663 [3.2D]
C1664 [2.1E]
C1665 [8.1F]
C1666 [3.5D]
C1667 [8.2F]
C1668 [8.2E]
C1669 [8.2E]
C1670 [2.3C]
C1671 [3.2G]
C1672 [2.1F]
C1673 [3.2F]
C1674 [3.3F]
C1675 [3.5E]
C1676 [3.2D]
C1677 [3.3G]
C1678 [3.2H]
C1679 [3.2H]
C1680 [3.2G]
C1681 [3.2G]
C1682 [3.2E]
C1683 [3.1D]
C1684 [3.2F]
C1685 [2.1F]
C1686 [3.2G]
C1687 [2.3C]
C1688 [3.2G]
C1689 [3.3G]
C1690 [3.2H]
C1691 [3.1D]
C1692 [2.1E]
C1693 [3.2H]
C1694 [2.3C]
C1695 [3.2E]
C1696 [2.1F]
C1697 [3.2G]
C1698 [3.2E]
C1699 [3.2F]
C1700 [3.1E]
C1701 [3.2G]
C1702 [2.1F]
C1703 [3.3F]
C1704 [3.2H]
C1705 [2.2C]
C1706 [2.1F]
C1707 [3.2F]

C1708 [3.2F]
C1709 [2.4E]
C1710 [3.2E]
C1711 [3.2F]
C1712 [2.2C]
C1713 [3.2G]
C1714 [9.3A]
C1715 [9.3A]
C1716 [2.3E]
C1717 [8.2C]
C1718 [2.4E]
C1720 [15.3B]
C1721 [2.1F]
C1722 [9.3B]
C1723 [8.2C]
C1724 [8.3C]
C1725 [8.3C]
C1726 [2.2F]
C1727 [2.2E]
C1729 [12.2A]
C1730 [2.2C]
C1731 [8.3C]
C1732 [11.2B]
C1733 [11.2B]
C1734 [11.2A]
C1735 [8.2C]
C1736 [2.1G]
C1737 [2.2C]
C1739 [11.2B]
C1740 [2.2E]
C1742 [2.1G]
C1743 [8.2C]
C1744 [8.2C]
C1745 [8.2C]
C1746 [8.1C]
C1747 [2.4F]
C1748 [2.2C]
C1749 [2.2C]
C1750 [11.2B]
C1751 [3.2E]
C1753 [17.3B]
C1754 [10.3B]
C1755 [8.2C]
C1756 [8.2C]
C1757 [8.1C]
C1758 [8.1C]
C1760 [2.4F]
C1761 [11.2A]
C1762 [8.2C]
C1763 [8.3D]
C1765 [19.5B]
C1766 [8.3C]
C1767 [12.3A]
C1768 [12.3B]
C1770 [8.1C]
C1771 [2.4G]
C1772 [16.2B]
C1773 [16.2B]
C1774 [8.1C]
C1775 [8.2C]
C1776 [2.1A]
C1777 [8.2C]
C1779 [2.3F]
C1780 [16.2B]
C1781 [16.2B]
C1782 [16.2B]
C1783 [16.2A]
C1784 [7.2B]
C1785 [16.2A]
C1786 [17.1B]
C1787 [19.4B]
C1788 [19.5A]
C1789 [2.1A]
C1790 [19.4B]
C1791 [19.4A]
C1792 [2.1A]
C1793 [2.1A]
C1794 [17.2B]
C1796 [19.4A]
C1799 [17.2B]
C1800 [18.3F]
C1801 [17.4C]
C1818 [9.2C]
C1820 [12.2C]
C1821 [10.5F]
C1822 [10.4F]
C1823 [10.4F]
C1824 [12.5E]
C1825 [9.5F]
C1826 [9.4F]
C1827 [9.4F]
C1828 [10.3G]
C1829 [12.2B]
C1832 [10.5G]
C1833 [10.4G]
C1834 [10.4G]

C1835 [9.5G]
C1836 [9.4G]
C1837 [9.4G]
C1838 [11.1G]
C1839 [12.1H]
C1840 [12.3E]
C1841 [12.3E]
C1842 [12.3E]
C1843 [12.3E]
C1844 [12.3E]
C1845 [12.3E]
C1846 [12.3E]
C1847 [12.3E]
C1848 [10.3G]
CN1002 [2.3B]
D1 [10.2F]
D2 [9.3F]
D3 [21.5G]
D4 [21.3G]
D5 [20.2E]
D6 [21.2D]
D7 [10.2F]
D8 [21.2D]
D9 [9.3F]
D10 [19.2B]
D507 [18.4E]
D1003 [9.2F]
D1004 [10.3F]
D1005 [9.2F]
D1006 [11.3E]
D1010 [12.3D]
D1011 [10.3F]
D1012 [12.2F]
D1013 [19.1A]
D1014 [17.4G]
D1505 [17.4F]
D1506 [17.3G]
D1508 [17.2E]
D1509 [17.2E]
D1510 [10.5F]
D1511 [10.4F]
D1512 [10.4F]
D1513 [9.5F]
D1514 [9.4F]
D1515 [9.4F]
D1517 [12.1E]
D1518 [12.1F]
F1001 [19.1C]
G1001 [2.3D]
G1001 [3.3C 3.4G]
G1001 [6.3H 6.3C]
G1001 [9.3C]
G1001 [10.3C]
G1001 [11.2C]
G1001 [12.3B]
G1001 [13.3D]
G1001 [14.3D]
G1001 [15.2C 15.4C]
G1001 [16.2C]
G1001 [17.3B]
G1001 [18.4C]
J1 [10.4H]
J2 [10.5H]
J3 [12.3H]
J4 [17.3H]
J1004 [11.2G]
J1005 [17.5G]
J1007 [17.4H]
J1501 [18.4E]
L1 [9.3F]
L2 [9.3F]
L3 [20.2F]
L4 [19.2B]
L6 [21.5G]
L9 [21.3G]
L10 [20.2F]
L12 [21.3G]
L1003 [19.2E]
L1004 [17.4G]
L1005 [19.1E]
L1006 [21.4G]
L1501 [10.3F]
L1502 [10.5F]
L1503 [10.4F]
L1504 [10.4F]
L1505 [9.5F]
L1506 [9.4F]
L1507 [9.4F]
L1508 [10.3F]
LB1 [12.2A]
LB5 [10.2F]
LB6 [10.2F]
LB8 [10.3G]
LB1001 [12.3F]
LB1002 [9.2F]
LB1003 [9.2F]

LB1004 [11.3F]
LB1007 [12.2F]
LB1009 [10.3A]
LB1010 [11.2A]
LB1012 [9.3A]
LB1501 [3.5E]
LB1502 [11.2A]
LB1503 [2.4F]
LB1505 [12.3A]
LB1506 [16.2A]
LB1507 [16.1A]
M1001 [7.2C 7.4B 7.4D]
M1001 [8.2A]
M1002 [7.4E 7.4F 7.2F]
M1002 [8.2H]
M1003 [4.2C 4.4B 4.4C]
M1003 [5.2A]
M1004 [4.4E 4.2F 4.4F]
M1004 [5.2H]
MEC5 [16.1G]
MEC1001 [16.2F]
MEC1002 [16.2F]
MEC1003 [16.1G]
MEC1004 [16.2F]
MEC1009 [16.2F]
MEC1010 [16.1F]
MEC1012 [16.2H]
MEC1016 [16.2H]
MEC1020 [16.2H]
Q1 [20.4B]
Q2 [21.2B]
Q3 [21.2A]
Q4 [12.1E 12.1E]
Q7 [21.5F]
Q8 [21.4F]
Q14 [21.4B]
Q15 [21.3A]
Q16 [21.2B]
Q18 [21.1B]
Q22 [20.3E]
Q23 [20.2B]
Q24 [20.2E]
Q26 [21.3F]
Q27 [21.3F]
Q28 [21.3F]
Q29 [21.5F]
Q505 [20.3C]
Q507 [20.4F]
Q1001 [12.4E]
Q1005 [12.2E]
Q1006 [11.4E]
Q1010 [18.4E]
Q1011 [18.4E]
Q1512 [17.4F]
Q1514 [17.1B]
Q1515 [17.2B]
Q1516 [17.2B]
Q1517 [11.4F]
R1 [21.4G]
R2 [21.4G]
R3 [20.4A]
R4 [20.3B]
R5 [20.4B]
R6 [35.3D]
R7 [17.2H]
R8 [17.3H]
R10 [10.2E]
R15 [10.2E]
R16 [10.2E]
R17 [10.2E]
R18 [14.3C]
R20 [14.2C]
R29 [21.2A]
R30 [21.1A]
R33 [21.4A]
R34 [21.3A]
R36 [21.1A]
R37 [21.4A]
R38 [21.3A]
R39 [21.3B]
R41 [21.3B]
R42 [21.3B]
R43 [21.3B]
R44 [21.3B]
R45 [21.3C]
R60 [21.4F]
R61 [15.1B]
R62 [21.3C]
R65 [21.5D]
R72 [21.3E]
R91 [21.4B]
R92 [21.4C]

R95 [21.3E]
R96 [21.4E]
R97 [21.3F]
R127 [20.2E]
R128 [20.3F]
R165 [18.4F]
R170 [20.2B]
R171 [20.3B]
R172 [20.2B]
R173 [20.2A]
R174 [20.2A]
R179 [21.4E]
R181 [21.4E]
R182 [21.4F]
R510 [21.4B]
R512 [21.4C]
R515 [21.5E]
R531 [21.3G]
R534 [21.2C]
R540 [20.2D]
R541 [20.2D]
R548 [20.3C]
R549 [20.3D]
R551 [20.2D]
R552 [20.3G]
R554 [20.3G]
R555 [20.3G]
R556 [20.1C]
R559 [20.4F]
R560 [20.4G]
R562 [20.1D]
R563 [20.4E]
R564 [20.4F]
R569 [21.5G]
R694 [9.3E]
R706 [9.3E]
R1001 [12.4F]
R1002 [12.4E]
R1003 [12.4F]
R1004 [12.4E]
R1005 [12.4F]
R1006 [12.4E]
R1007 [12.4F]
R1008 [12.4E]
R1009 [9.2E]
R1011 [10.3E]
R1012 [9.2E]
R1013 [9.2E]
R1019 [9.2E]
R1022 [12.3E]
R1023 [11.3E]
R1024 [10.3E]
R1025 [11.3E]
R1026 [12.3D]
R1031 [12.2E]
R1048 [19.2B]
R1049 [19.1B]
R1050 [19.1A]
R1051 [19.2E]
R1052 [19.2E]
R1053 [17.5B]
R1054 [17.4B]
R1055 [17.4B]
R1056 [17.5B]
R1057 [2.1B]
R1058 [2.2C]
R1059 [11.5E]
R1064 [18.4B]
R1066 [7.3A]
R1067 [7.3B]
R1069 [7.2A]
R1071 [15.4D]
R1074 [18.4D]
R1075 [7.4G]
R1076 [7.3G]
R1078 [7.5B]
R1079 [7.5C]
R1080 [4.5A]
R1081 [4.5C]
R1082 [7.5B]
R1083 [7.5C]
R1084 [7.5D]
R1085 [7.5F]
R1086 [4.5D]
R1087 [4.5E]
R1088 [7.5D]
R1089 [7.5F]
R1090 [7.4G]
R1091 [7.5G]
R1093 [7.2D]
R1094 [7.3D]
R1096 [7.3E]
R1097 [4.5B]
R1098 [4.5B]
R1099 [4.5F]
R1100 [4.5E]

R1101 [7.5B]
R1102 [7.5C]
R1103 [4.3E]
R1104 [4.2A]
R1105 [4.3A]
R1109 [4.3D]
R1110 [4.3B]
R1111 [4.2D]
R1112 [17.4G]
R1113 [7.5D]
R1114 [7.5E]
R1116 [4.5G]
R1117 [4.4G]
R1118 [4.5D]
R1119 [4.5D]
R1120 [4.5C]
R1121 [4.5C]
R1122 [4.4G]
R1135 [18.4F]
R1507 [21.3E]
R1509 [21.5C]
R1520 [21.4C]
R1522 [21.1A]
R1529 [21.4C]
R1532 [21.1B]
R1541 [20.3B]
R1567 [21.1A]
R1570 [21.2A]
R1571 [21.2A]
R1573 [19.1E]
R1575 [19.1E]
R1577 [19.1E]
R1578 [4.3B]
R1580 [4.2B]
R1581 [4.2E]
R1582 [4.3H]
R1583 [4.2B]
R1584 [4.2E]
R1585 [4.2B]
R1586 [4.2E]
R1587 [4.3G]
R1589 [4.3E]
R1590 [4.3G]
R1595 [17.3G]
R1596 [17.3G]
R1597 [17.4F]
R1601 [4.3G]
R1602 [7.2E]
R1603 [7.2E]
R1604 [7.2E]
R1605 [2.5E]
R1606 [17.3D]
R1607 [17.3D]
R1608 [7.3E]
R1609 [17.2D]
R1610 [17.2D]
R1611 [3.4D]
R1612 [7.2G]
R1613 [6.5D]
R1614 [2.5E]
R1615 [6.5D]
R1616 [6.5D]
R1617 [7.2H]
R1618 [2.2C]
R1619 [6.4D]
R1620 [9.4E]
R1621 [9.3B]
R1622 [7.2G]
R1623 [9.4E]
R1624 [9.5E]
R1625 [11.2B]
R1627 [18.4B]
R1628 [13.3C]
R1630 [12.3B]
R1631 [18.4B]
R1632 [13.2C]
R1633 [7.3B]
R1634 [10.4D]
R1635 [2.1C]
R1636 [17.4E]
R1637 [10.3B]
R1638 [10.5D]
R1639 [17.4D]
R1640 [2.1B]
R1641 [16.2D]
R1642 [10.4D]
R1644 [17.4D]
R1645 [17.3E]
R1646 [17.4D]
R1647 [16.2C]
R1648 [7.2B]
R1649 [7.2B]
R1650 [7.2B]
R1651 [19.5B]
R1652 [19.5B]
R1653 [17.1B]

R1655 [19.4B]
R1656 [17.4D]
R1657 [19.4B]
R1658 [17.2E]
R1659 [17.1B]
R1660 [17.2C]
R1661 [18.2B]
R1662 [19.3B]
R1663 [18.2C]
R1664 [17.1B]
R1665 [18.1C]
R1666 [18.1B]
R1667 [17.2B]
R1668 [18.1C]
R1669 [17.2E]
R1670 [18.2D]
R1671 [18.2C]
R1672 [18.1D]
R1673 [17.2B]
R1674 [11.5F]
R1675 [18.1E]
R1676 [18.2E]
R1677 [18.2E]
R1678 [18.1E]
R1679 [18.3E]
R1680 [2.1D]
R1681 [17.4B]
R1687 [12.1D]
R1688 [12.1D]
R1689 [12.1D]
R1690 [12.1D]
R1691 [10.5E]
R1692 [10.4E]
R1693 [10.4E]
R1700 [9.5D]
R1701 [9.4D]
R1702 [9.4D]
R1703 [12.4E]
R1704 [12.4D]
R1707 [12.1F]
R1708 [12.1F]
RP1 [2.1C 2.1C 2.1C 2.1C]
TP1501 [3.5B]
TP1502 [17.3A]
TP1503 [17.3A]
U1 [19.2B]
U8 [21.3D]
U502 [20.2C]
U507 [9.3D 9.3D]
U507 [10.3D 10.3D]
U1001 [12.1G]
U1003 [19.1B]
U1006 [18.4F]
U1504 [19.5A]
U1505 [19.4A]
U1506 [18.3E]
Y1001 [16.2C]
Y1002 [16.2C]

MIS-MA 羅覺林 20100119

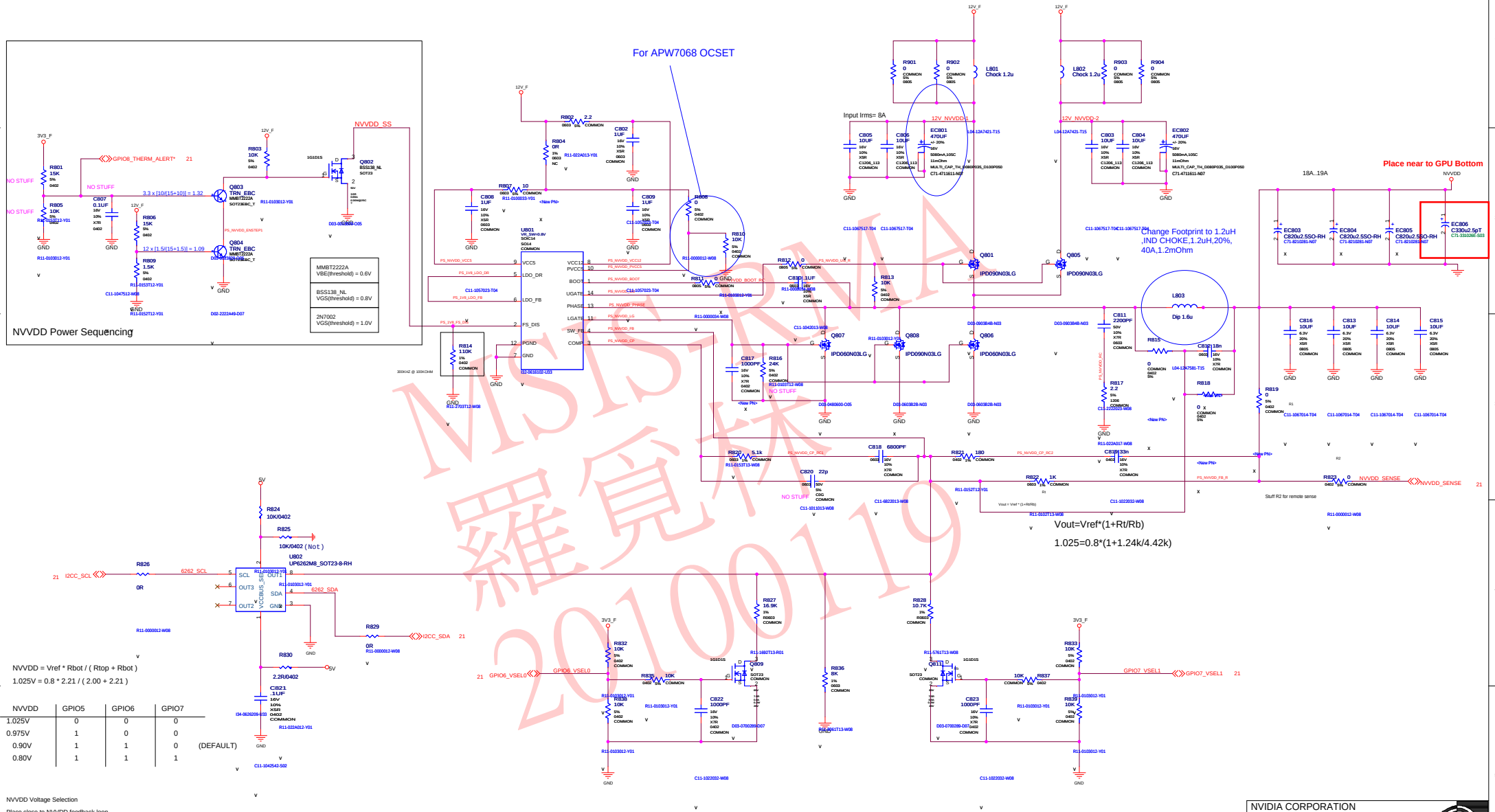
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	<edit here to insert page detail>

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME	<ENGINEER>	DATE	01-JUL-2009

Power Supply III: NVVDD



NVVDD	GPIO5	GPIO6	GPIO7
1.025V	0	0	0
0.975V	1	0	0
0.90V	1	1	0
0.80V (DEFAULT)	1	1	1

MSI-RMA 羅宜林 20100119

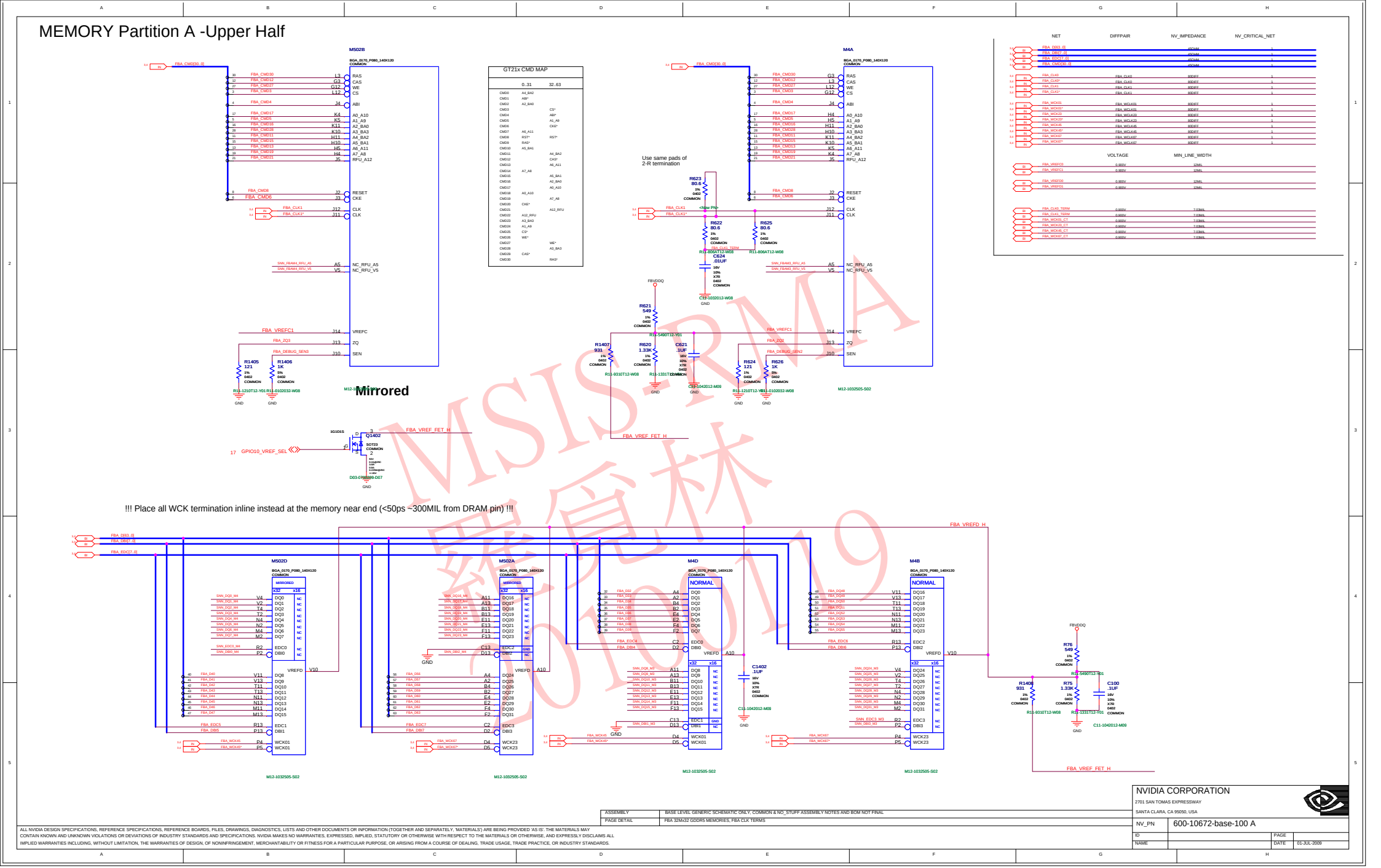
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	NVVDD POWER SUPPLY

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10681-base-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

MEMORY Partition A -Upper Half



!!! Place all WCK termination inline instead at the memory near end (<50ps ~300MIL from DRAM pin) !!!

MSIS-RMA 寒宜林 20100119

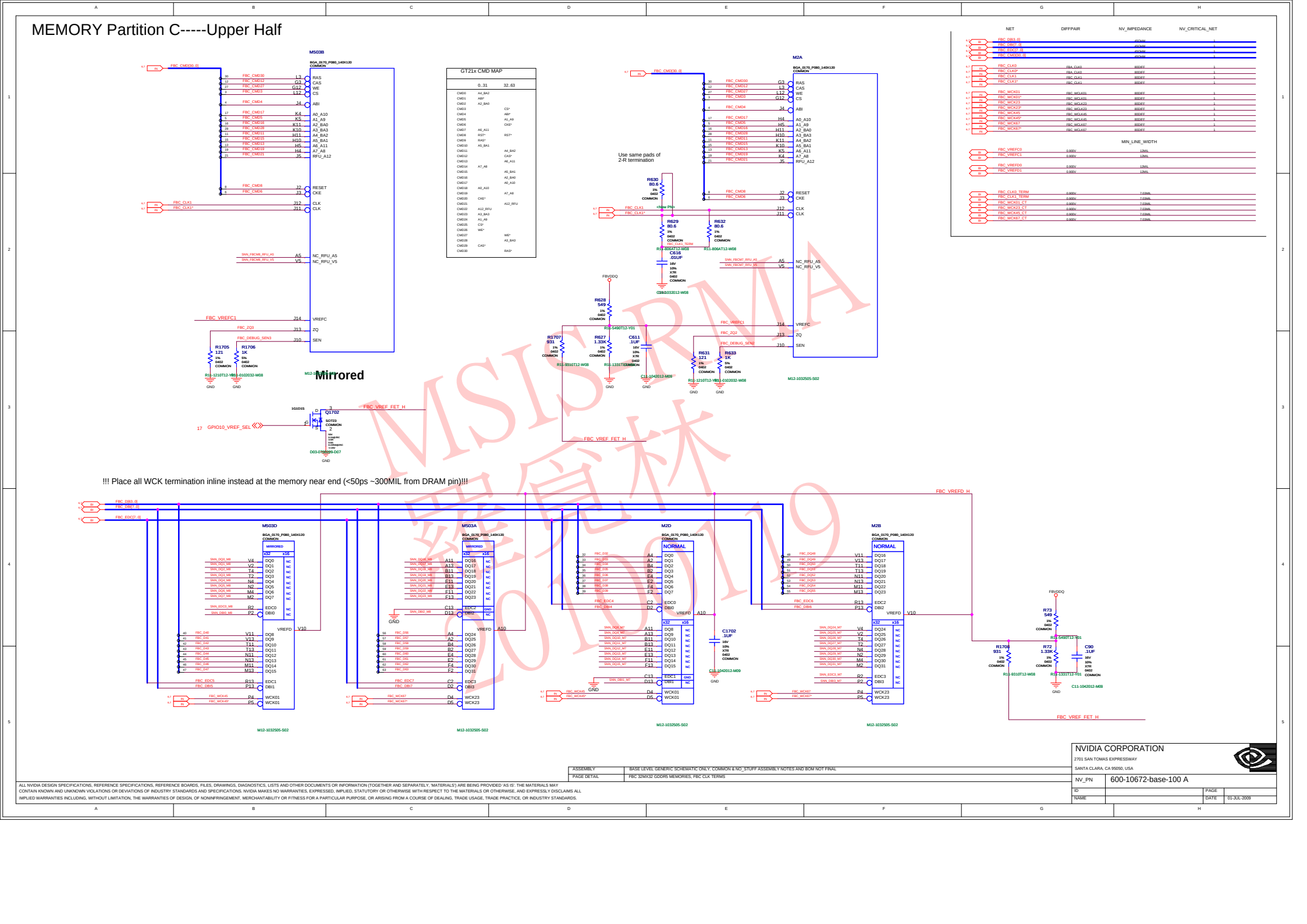
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 32Mx32 GDDR5 MEMORIES, FBA CLK TERMS

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

MEMORY Partition C-----Upper Half



MSI RMA 20100119 羅宗林

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 32MX32 GDDR5 MEMORIES, FBC CLK TERMS

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009