```
PRIMARY ** VGA1 DAC A ** I2C A(1).
SECONDARY ** VGA2 DAC_B ** I2C_B(0).
VIDCAP ** VIP 7114 I2C_C(2).
9pin DIN ** RGB2 I2C_C(2).
I2C x(Old H/W number).
                                  See PDS for Hookup
```

# P73, NV17, 4/8Mx16 DDR, 32/64MB, Dual RGB, TV-out, Video Capture, AGP4X

PCI DEVICE ID = 0X172 FOR GF4-MX420-XX.



#### P73-A00-X01

Created SCH from P78-X16 for I/O Netlist only

#### P73-A00-X02

CREATED NX16 MEMORY, DECOUPLING FROM P78

#### P73-A00-X03

ADDED MEM & CORE FROM P70 PS FOR ISL6529 SAA7114 DECAPS ADDED AND CHANGED TO 0402

#### P73-A00-X04

PCB Footprint for RAM added

#### P73-A00-X05

#### P73-A00-X06

PCB Footprint for Inductor, Stacked DB15, ISL6529 added PCB Footprint for L305, L307, L308, L316-L324 changed to 0603 from 0805. Added X-Comp R750, R751.

#### P73-A00-X07

TV-XTAL should be 18pf CL. Each memory with separate clock

#### P73-A00-X08

U700-Parallel ROM and C700 decap Removed for space

#### P73-A00-X09

0603 to 0402 Package Changes for 49 components

#### P73-A00-X10

Design Review Updates

0603 to 0402 Package Changes for 33 components

0805 to 0603 Package Changes for 17 components

0402 to 0603 Package Changes for 10 components

#### Removed 25 components P73-A00-X11

Swaps in Memory termination RN201, RN203, RN205, RN207

### P73-A00-X12

C606, C615 TH replacements, Removed for want of space.

# P73-A00-X13

Memory bus swaps on 1/11/02-Swap 2

## P73-A00-X14

Memory bus swaps on 1/12/02-Swap 3

## P73-A00-X15

Memory bus byte swaps as per NV17-Ball

## P73-A00-X16

Memory bus byte and bit swaps as per layout

TV Filter moved to VGA2 page with more routing notes

## P73-A00-X17

The C397, C311, C318 changed to 0603 from 0402 for two trace routing near GPU break out. P300-2 Mounting pins removed from CGND

#### P73-A00-X18

Added X Components C824 to C830 to FBVDDQ

Added X Components C831 to C832 to FBVDDQ

R610, R612 for FBVDDQ re-fixed to have <5K for Rfb

## P73-A00-X20- X-Rel Candidate

Clean-up for Agile upload Memory de-coupling values modified as per layout.

#### P73-A00-X21- ECO-3893

Q600 Should be FET istead of BJT

## P73-A00-X22-

Corrected NV17-S sku in the table in this page

#### P73-A01-X01

The RED and GREEN signal to TV filter interchanged. Corrected by swapping CVBS\_YOUT

#### P73-A01-X02

Corrected by swapping CVBS YOUT and COUT at DIN

Type 3 Compensation Values for ISL6529 changed

R614---NS---8.06K

C618---33nF---70nF R611---16 2K---6 65K

C619---33nF----1.8nF

AGPSTOP to 3.3V R616 -47R inseries to 12V for ISL6529 is too high, changed to 4.7R

R616 -4.7R inseries to 12V for ISL6529 is changed to OR

R624 - Added 2.2R inseries to 5V for ISL6529.

ISL6529 Compensation Res to be Type 2 with Snubber coponents stuffed. Values under test.

## P73-A01-X04-For X-Rel

The Type 2 Compensation works better than Type 3 Compensation. C616. R614 No Stuff, R614 Nostuff, C618 3300pf, R611 16.2K,

C619 33pF, R616 0R

Snubber values are R626 2.2R, C617 2200PF

## P73-A01-X05-ECO4193

The Type 3 Compensation works better than Type 2 Compensation in the new layout with new values tried at Intersil. C616-47nF. R614-10R, C618 1000pf, R611-10K, C619 1500pF.

#### P73-A01-X06

NVVDD & FBVDDQ Voltage tolerance note updated for Vref +/-2%, Adj resistors 1%.

The NVPN for caps C329, C331, C332, C334, C335, C337, C338, C340, C341, C343, C344, C346 changed from 0603

## P73-A02-X01

Add Schmitt Inverter buffer to PCIRST signal. Added U101.

## P73-A02-X02 X-Released

Add D-FF buffer to PCIRST\_ signal. Added U101.

Add R325, series termination res to XTALBUFF signal

Add R111, C145 smoothing ckt to PCIRST.

Add R112 to by pass D-FF ckt

### P73-A03-X01 X-Released

Add R113 & R114 to D-FF ckt and Asynchronously Reset the o/p D-FF using PCIRST\_

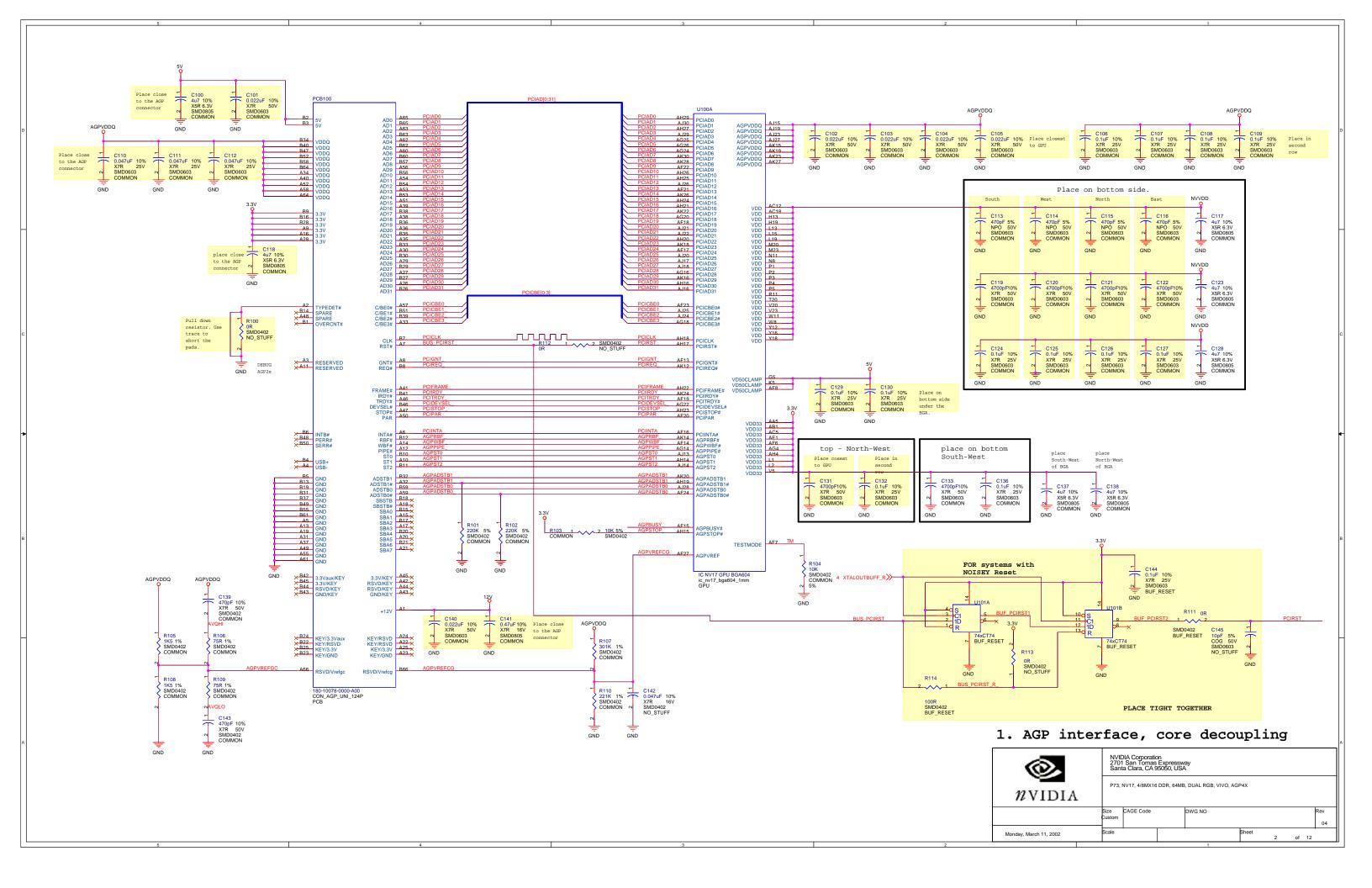
Stuff Option	Meaning				
COMMON	Common to all assemblies and 1st VGA comps				
NO STUFF	Not present in any assembly				
VIDCAP	Video In or Video Capture				
VGA2	2nd VGA Components and Conenctor				
DSUB	Standard single VGA Connector				
TV	Second DAC channel goes to Svideo connector as TV Out				
TVO	4pin DIN for TV Only				
1117	Fixed 1117 linear regulator for A3.3V				
1117_ADJ	Adjustable 1117 linear regulator for A3.3V				
NO_1117	Connect A3.3V to 3.3V. No 1117 regulator.				
OLAMB4	\(\( \( \Lambda \) \( \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\				
CLAMP1	VGA1 Sync/I2C Clamping diodes				
RGB_PROT	RGB Protection diodes on primary DAC outputs				
CLAMP2	VGA2 Sync/I2C Clamping diodes				
RGB2_PROT	RGB Protection diodes on secondary DAC outputs				
CLAMP3	VIDCAP I2C/Video In Clamping diodes				
TVCLAMP	TV Red/Green Clamping diodes				
GPU	GPU ONLY				
NV17-S	IDSTRAP OPTION-172H				
MEMORY	Memory only				
M2-8V	Memory PS output 2.8V				
M2-5V	Memory PS output 2.5V				
BUF_RESET	PCIRST through D-FF Circuit				

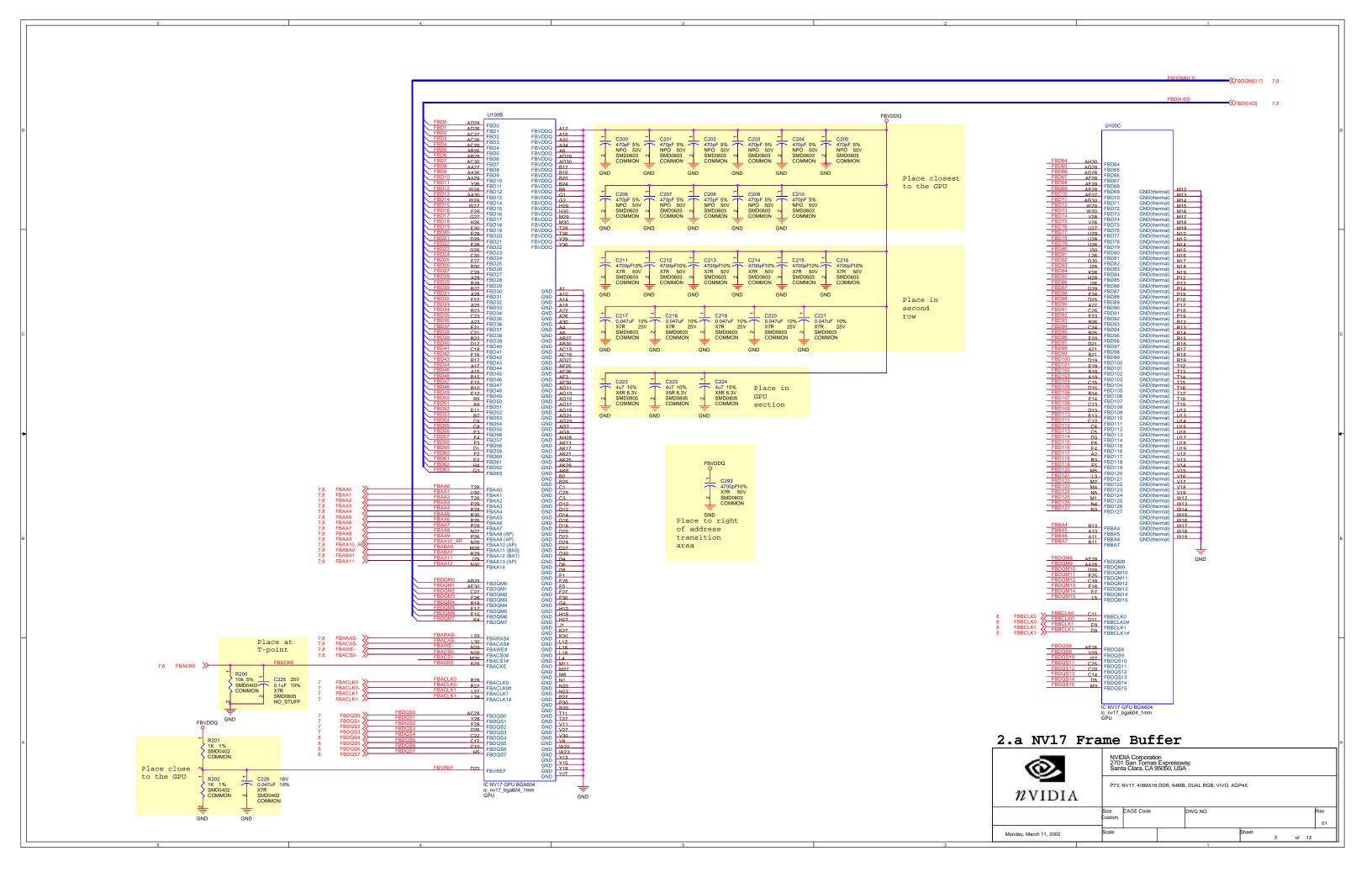
## PAGE OVERVIEW

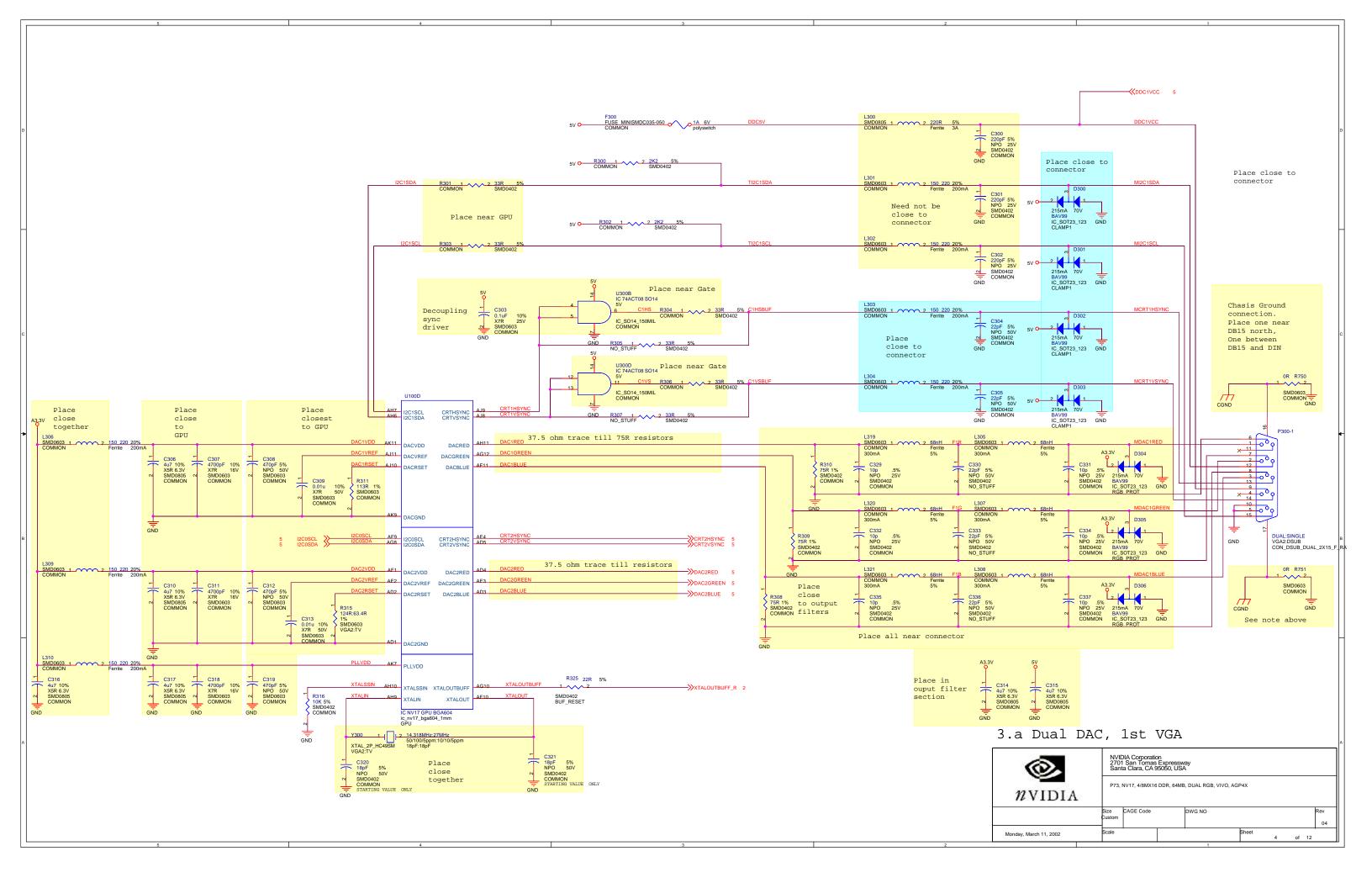
- 1 top (this) page
- 2 1. AGP interface, core decoupling
- 3 2.a NV17 Frame Buffer
- 4 3.a Dual DAC, 1st VGA
- 5 3.b Dual DAC, 2nd VGA
- 6. 3.c TMDS NV17
- 7 4.a Frame Buffer 0..31
- 8 4.b Frame Buffer 32...63 9 5. TV-out, video capture, stereo
- 10 6. Power supply
- 11 7. BIOS, Strapping

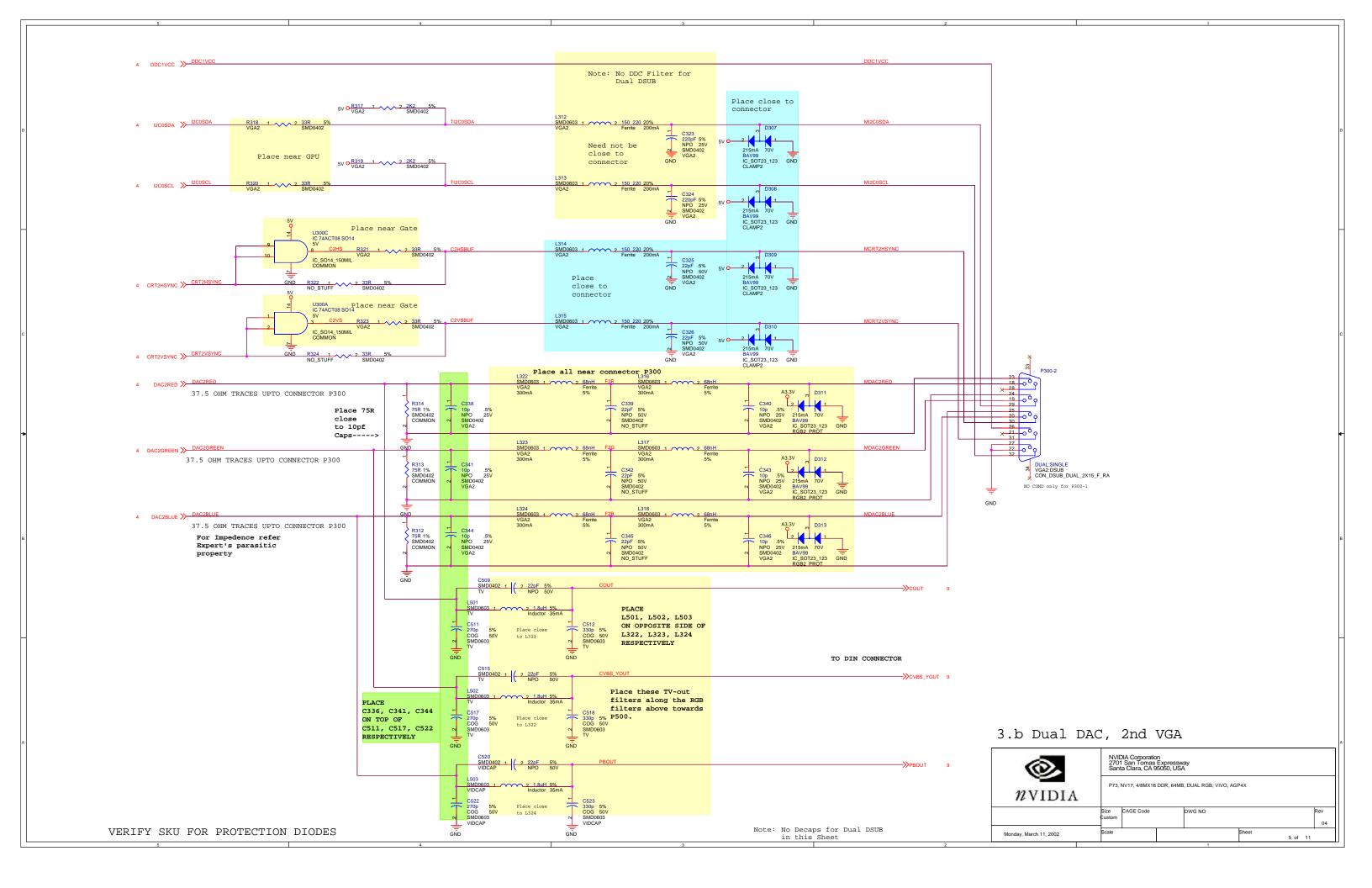
140-10073-0000-A03 602-10073-0000-A03

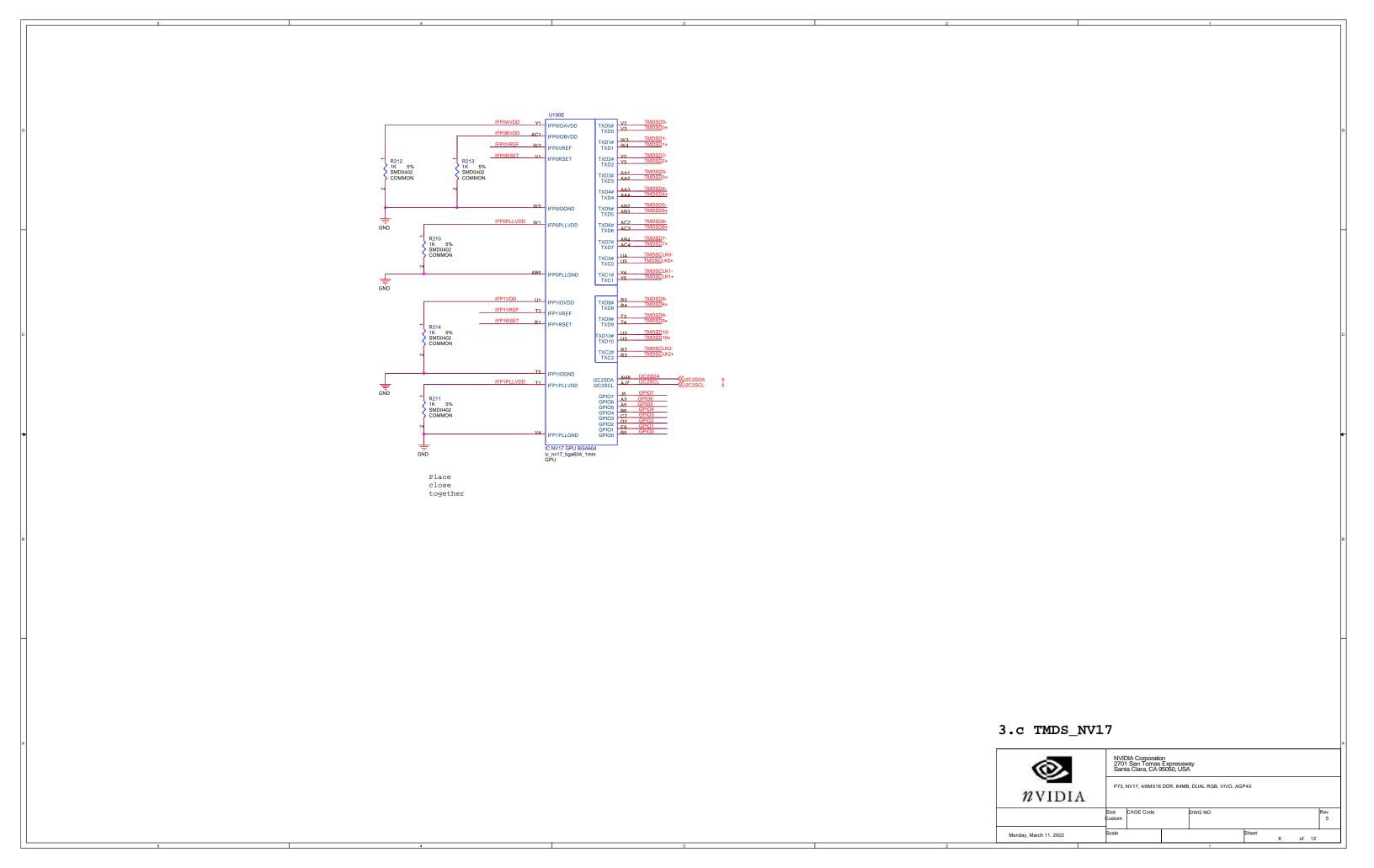
(A)	NVIE 3535 Sant	DIA Corporation Monroe St a Clara, CA 9	n 5051, USA	<b>A</b>					
	P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X								
NVIDIA									
	Size	CAGE Code		DWG NO					Rev
	Custor	n							06
Monday, March 11, 2002	Scale				Sheet	1	of	11	

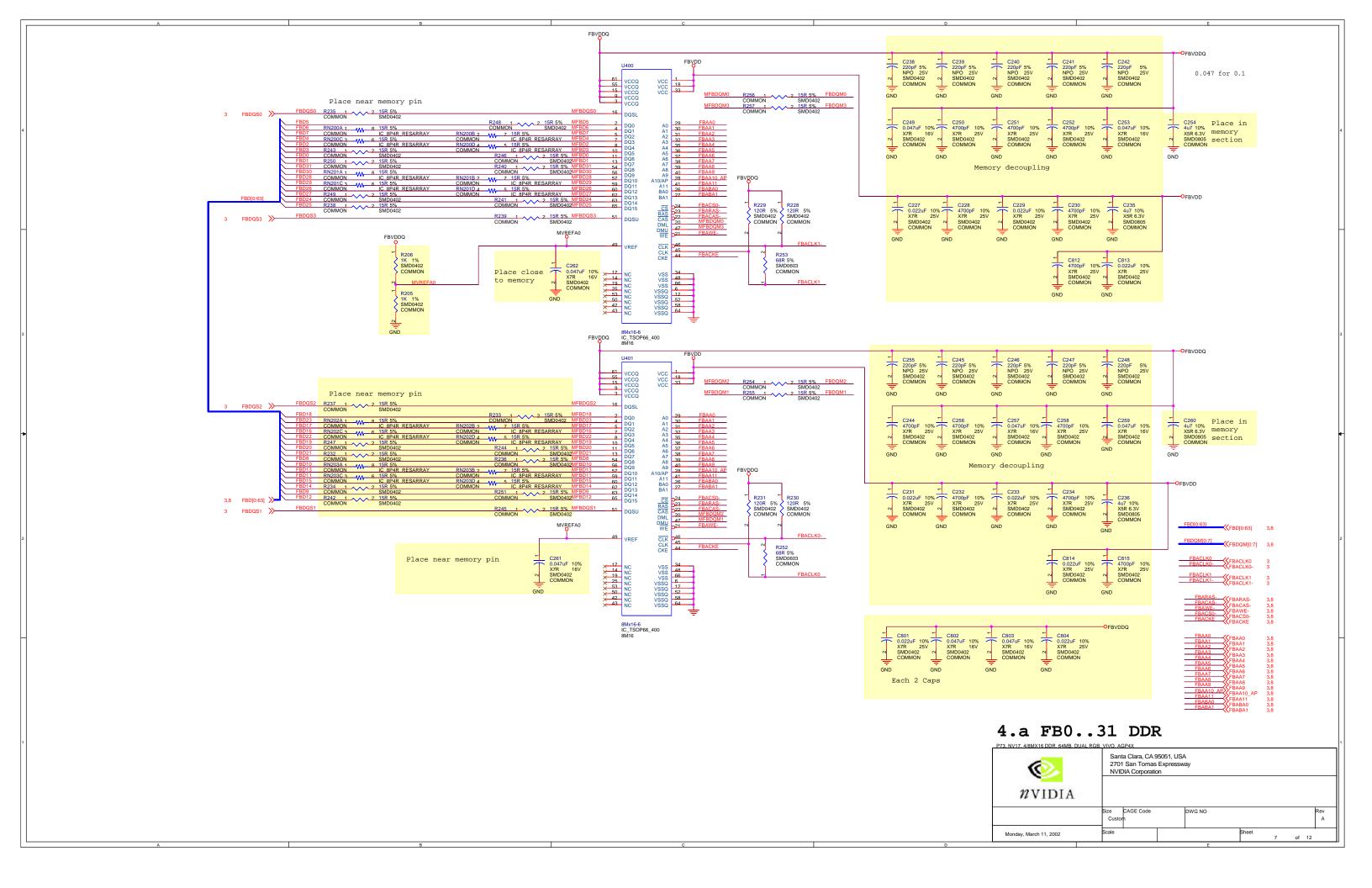


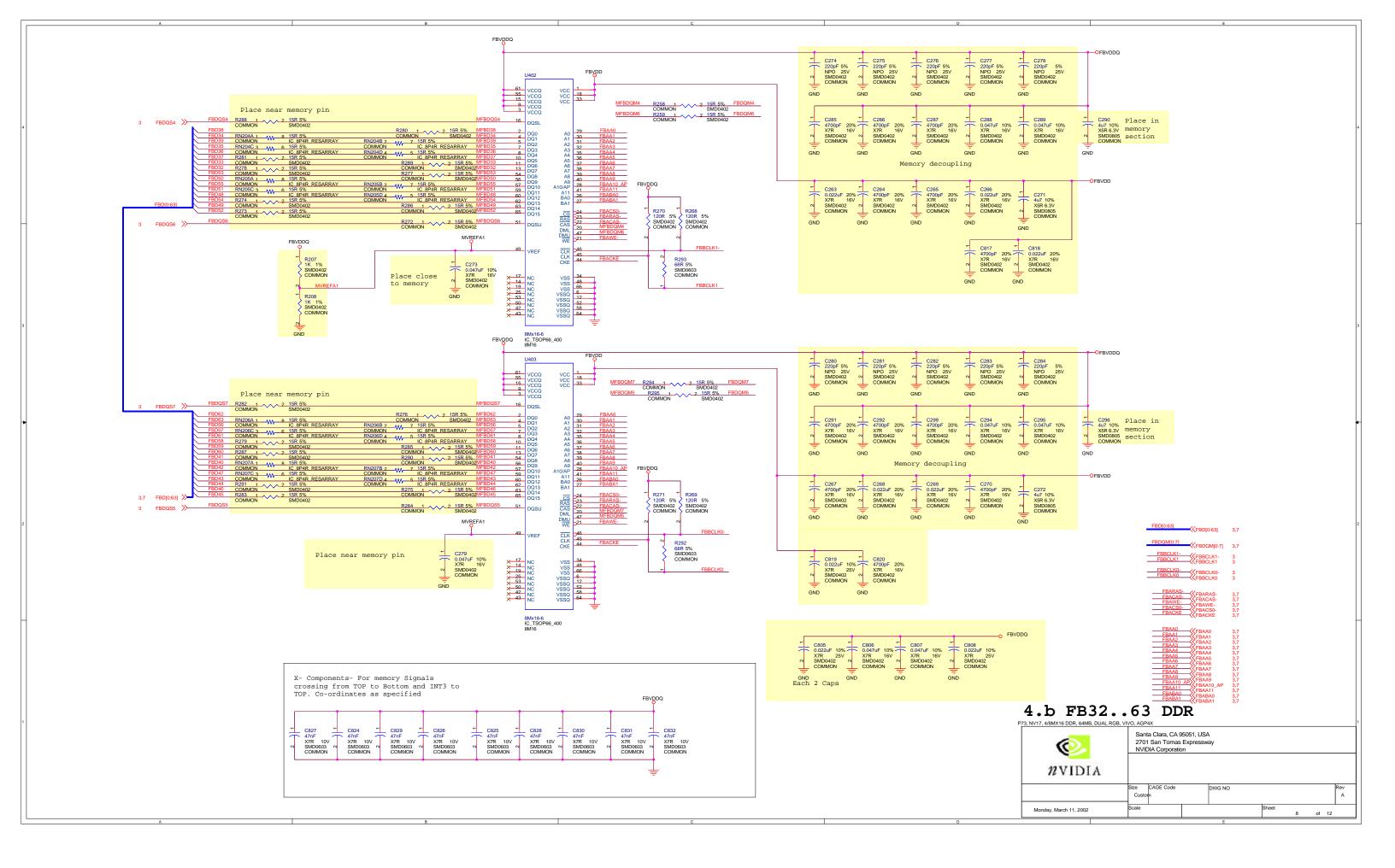


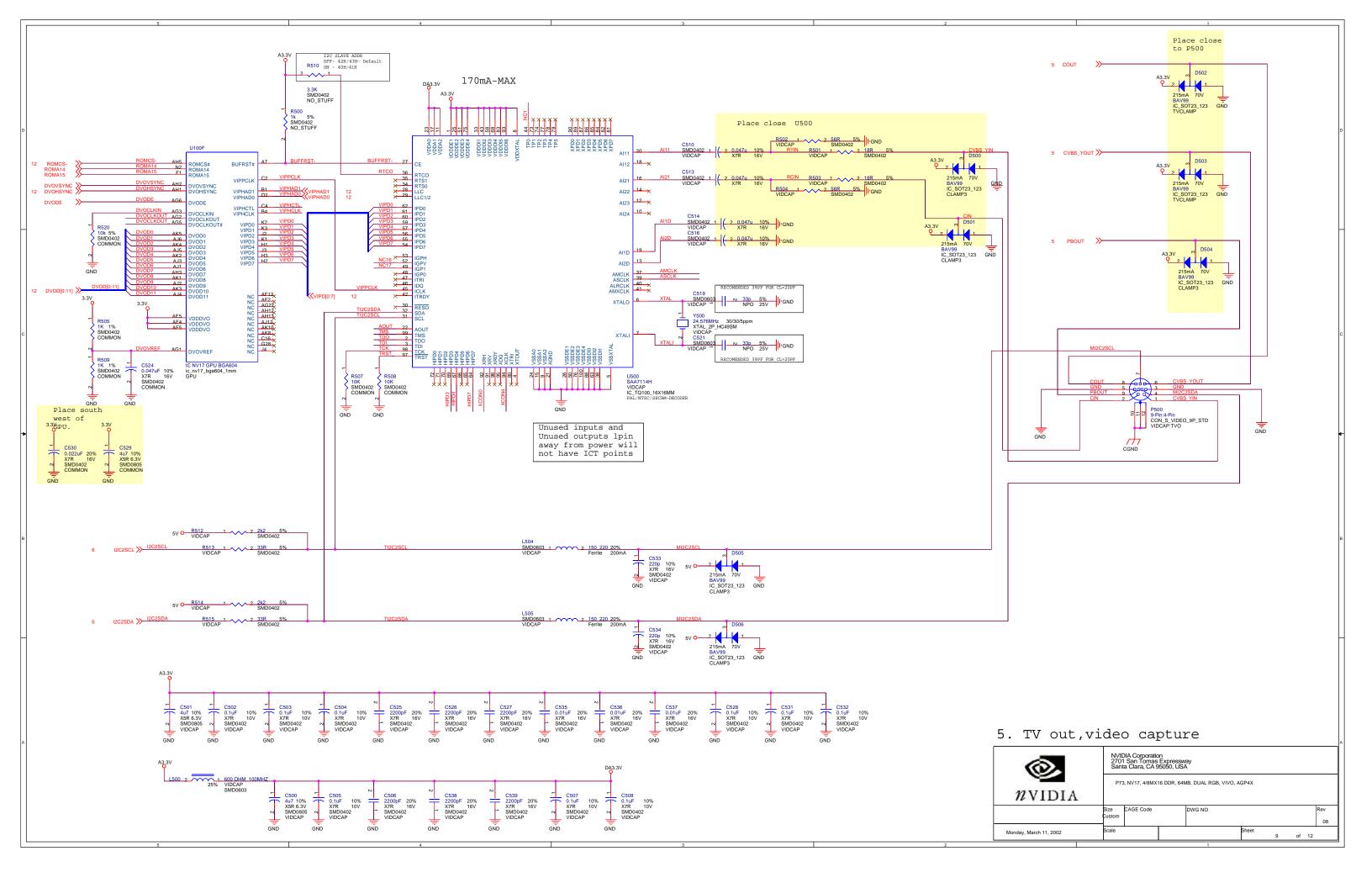


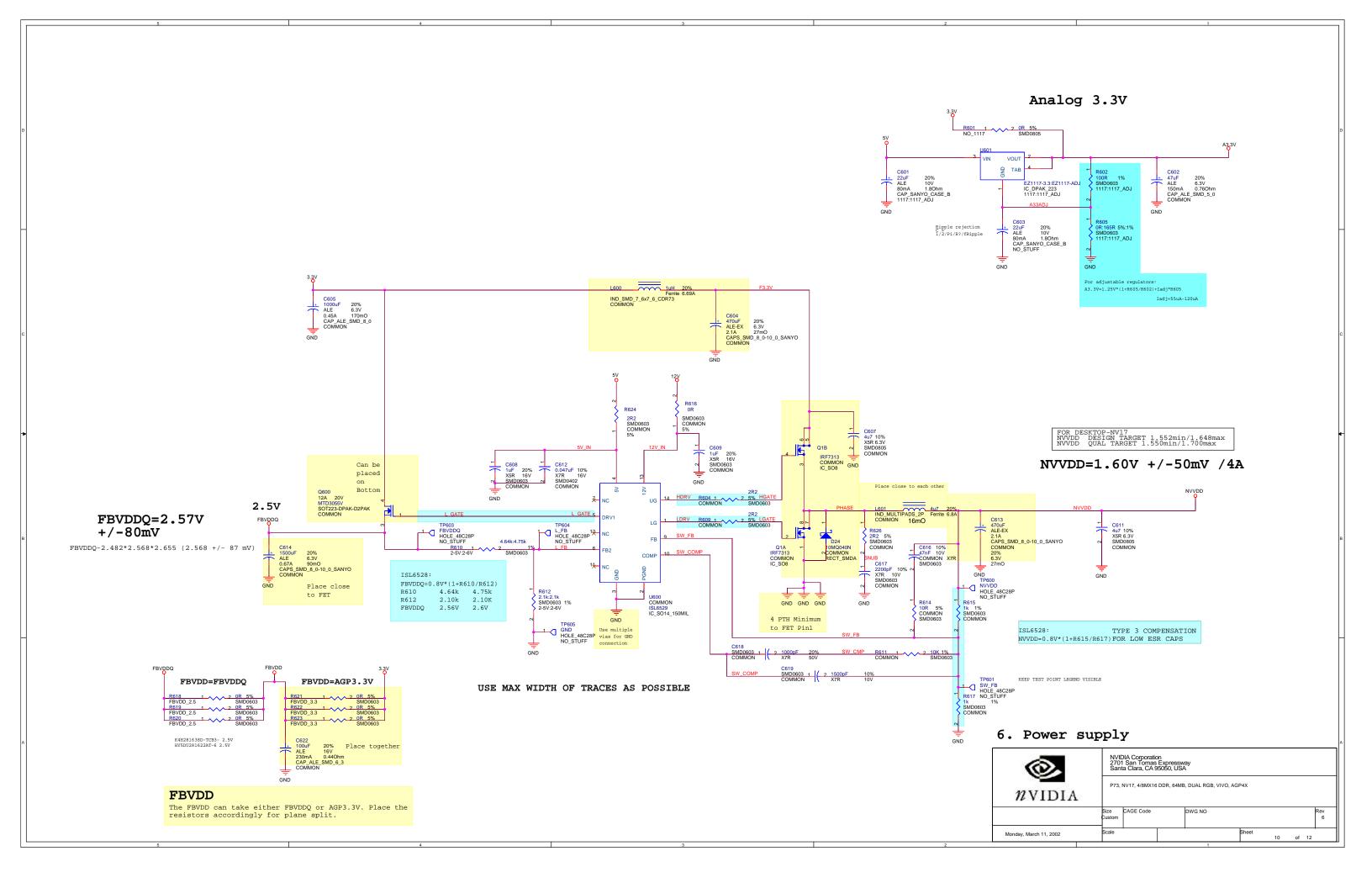


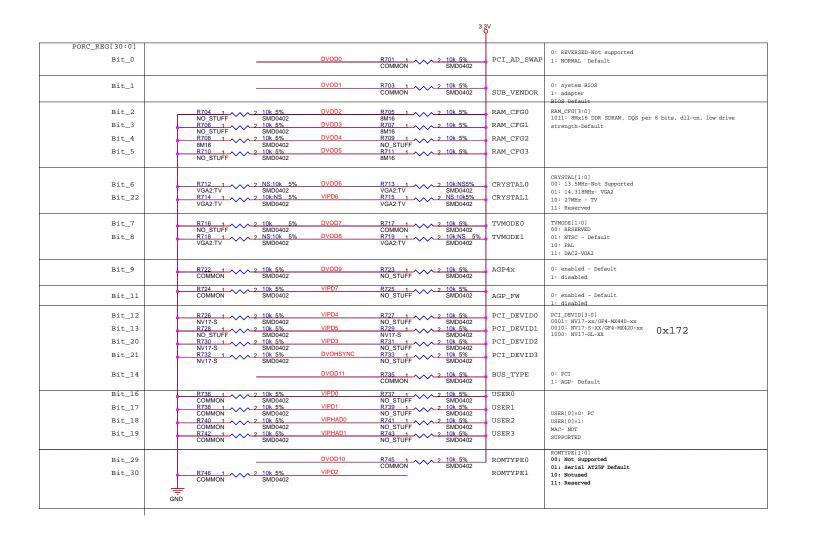


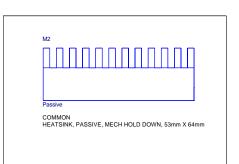


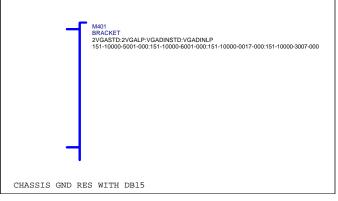


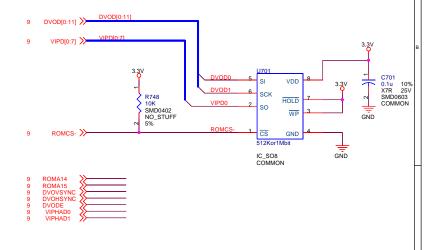












# 7. BIOS, Strapping, Mech

	NVIE 2701 Sant	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA									
$n_{\text{VIDIA}}$	P73,	P73, NV17, 4/8MX16 DDR, 64MB, DUAL RGB, VIVO, AGP4X									
	Size Custom	CAGE Code		DWG NO					Rev 08		
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