PG142-B00

DP + DP + DP + HDMI/DP

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47	SEQ: 5V, 1V8, 3V3_SEQ
48	SEQ: NVVDD, PEX, FBVDDQ ENABLE
49	SEQ: MISC
50	SEQ: VOLTAGE MONITOR
51	FAN & LED
52	PS:OVRM_PWR_SENSE
53	MECH
54	PTC

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Page2: Block Diagram

DP

DP

DP

DP

HDMI

CO-LAYOUT

POWER SUPPLY

MEM D LO

MEM D HI

GA10X GPU

MEM C LO

MEM C HI

MEM B LO

MEM A HI

MEM A LO

MEM B HI

NVVDD — Power Supply — NVVDD: PH1-7 OVR4i

EXT_12V

BALANCE

FBVDDQ — Power Supply — FBVDD/Q PH1-2 OVR3

PEX_12V Finger

1V8 — Power Supply — 1V8 Switcher

5V — Power Supply — 5V SWITCHER OVRU

PEX_VDD — Power Supply — PEX_VDD Switcher

PEX_3V3 Finger

Input Switch
OVRS
(RTD3 GC6 12V-OFF)

LED

2x FAN

3V3_AUX Finger

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Page3: PCI Express

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.406
3V3	3.3V	3.0A	0.125
GND	0V	8.5A	0.245

CN1
CON_X16
NO STUFF
CON_PCIEXP_X16_EDGE

END OF X1 / END OF X4 / END OF X8 / END OF X16

G1A
BGA2714
COMMON
1/24 PCI_EXPRESS

Place under GPU
6x 0402 1uF
2x 0603 4.7uF

Place between GPU and PS
1x 0805 10uF
1x 0805 22uF

1x 0805 47uF
Placed by PEX_VDD PS

9x 0402 1uF
2x 0603 4.7uF

2x 0805 10uF
1x 0805 22uF

3x 0805 47uF
Placed by 1v8 PS

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Page4: PCIE GEN4 RC TERMINATIONS

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Page5: MEMORY: GPU Partition A/B

//syseng/Projects/GA1xx/GA1XX_CMD-Mapping.xlsx

compatible

G1B

BGA2714
COMMON

2/24 FBA

FB_DATA
FBA_D[63..0]

FB_DBI
FBA_DBI[7..0]

FB_EDC
FBA_EDC[7..0]

FB_CMD
FBA_CMD[52..0]

0	FBA_D0	AC51	FBA_D0
1	FBA_D1	AB48	FBA_D1
2	FBA_D2	AC52	FBA_D2
3	FBA_D3	AC49	FBA_D3
4	FBA_D4	AF52	FBA_D4
5	FBA_D5	AC54	FBA_D5
6	FBA_D6	AE51	FBA_D6
7	FBA_D7	AF51	FBA_D7
8	FBA_D8	W51	FBA_D8
9	FBA_D9	W50	FBA_D9
10	FBA_D10	W53	FBA_D10
11	FBA_D11	Y54	FBA_D11
12	FBA_D12	Y52	FBA_D12
13	FBA_D13	Y51	FBA_D13
14	FBA_D14	Y49	FBA_D14
15	FBA_D15	AB51	FBA_D15
16	FBA_D16	AM54	FBA_D16
17	FBA_D17	AL51	FBA_D17
18	FBA_D18	AM52	FBA_D18
19	FBA_D19	AJ54	FBA_D19
20	FBA_D20	AM47	FBA_D20
21	FBA_D21	AM51	FBA_D21
22	FBA_D22	AP50	FBA_D22
23	FBA_D23	AM49	FBA_D23
24	FBA_D24	AF54	FBA_D24
25	FBA_D25	AF49	FBA_D25
26	FBA_D26	AH51	FBA_D26
27	FBA_D27	AF47	FBA_D27
28	FBA_D28	AJ52	FBA_D28
29	FBA_D29	AJ51	FBA_D29
30	FBA_D30	AH48	FBA_D30
31	FBA_D31	AJ49	FBA_D31
32	FBA_D32	BA49	FBA_D32
33	FBA_D33	BD47	FBA_D33
34	FBA_D34	BD54	FBA_D34
35	FBA_D35	BD52	FBA_D35
36	FBA_D36	BC51	FBA_D36
37	FBA_D37	BD51	FBA_D37
38	FBA_D38	BF51	FBA_D38
39	FBA_D39	BD49	FBA_D39
40	FBA_D40	BG52	FBA_D40
41	FBA_D41	BG51	FBA_D41
42	FBA_D42	BG54	FBA_D42
43	FBA_D43	BF49	FBA_D43
44	FBA_D44	BJ54	FBA_D44
45	FBA_D45	BG50	FBA_D45
46	FBA_D46	BJ52	FBA_D46
47	FBA_D47	BK53	FBA_D47
48	FBA_D48	AP51	FBA_D48
49	FBA_D49	AP53	FBA_D49
50	FBA_D50	AR52	FBA_D50
51	FBA_D51	AR54	FBA_D51
52	FBA_D52	AU51	FBA_D52
53	FBA_D53	AR51	FBA_D53
54	FBA_D54	AV51	FBA_D54
55	FBA_D55	AR49	FBA_D55
56	FBA_D56	AV49	FBA_D56
57	FBA_D57	AV54	FBA_D57
58	FBA_D58	AY51	FBA_D58
59	FBA_D59	AV52	FBA_D59
60	FBA_D60	AY48	FBA_D60
61	FBA_D61	BA54	FBA_D61
62	FBA_D62	BA52	FBA_D62
63	FBA_D63	BA51	FBA_D63

0	FBA_DBI0	AE50	FBA_DQM0
1	FBA_DBI1	AB50	FBA_DQM1
2	FBA_DBI2	AL50	FBA_DQM2
3	FBA_DBI3	AH50	FBA_DQM3
4	FBA_DBI4	BC50	FBA_DQM4
5	FBA_DBI5	BF50	FBA_DQM5
6	FBA_DBI6	AU50	FBA_DQM6
7	FBA_DBI7	AY50	FBA_DQM7

0	FBA_EDC0	AE53	FBA_DQS_WP0
1	FBA_EDC1	AB53	FBA_DQS_WP1
2	FBA_EDC2	AL53	FBA_DQS_WP2
3	FBA_EDC3	AH53	FBA_DQS_WP3
4	FBA_EDC4	BC53	FBA_DQS_WP4
5	FBA_EDC5	BF53	FBA_DQS_WP5
6	FBA_EDC6	AU53	FBA_DQS_WP6
7	FBA_EDC7	AY53	FBA_DQS_WP7

FBA_CMD0	Y53	FBA_CMD0	0
FBA_CMD1	AA56	FBA_CMD1	1
FBA_CMD2	AB55	FBA_CMD2	2
FBA_CMD3	AB56	FBA_CMD3	3
FBA_CMD4	AC56	FBA_CMD4	4
FBA_CMD5	AC53	FBA_CMD5	5
FBA_CMD6	AD56	FBA_CMD6	6
FBA_CMD7	AE55	FBA_CMD7	7
FBA_CMD8	AE56	FBA_CMD8	8
FBA_CMD9	AF56	FBA_CMD9	9
FBA_CMD10	AF53	FBA_CMD10	10
FBA_CMD11	AG56	FBA_CMD11	11
FBA_CMD12	AH55	FBA_CMD12	12
FBA_CMD13	AH56	FBA_CMD13	13
FBA_CMD14	AJ56	FBA_CMD14	14
FBA_CMD15	AJ53	FBA_CMD15	15
FBA_CMD16	AK56	FBA_CMD16	16
FBA_CMD17	AL55	FBA_CMD17	17
FBA_CMD18	AL56	FBA_CMD18	18
FBA_CMD19	AM56	FBA_CMD19	19
FBA_CMD20	AM53	FBA_CMD20	20
FBA_CMD21	AN56	FBA_CMD21	21
FBA_CMD22	AP55	FBA_CMD22	22
FBA_CMD23	AP56	FBA_CMD23	23
FBA_CMD24	AR56	FBA_CMD24	24
FBA_CMD25_NC	AR53		
FBA_CMD26_NC	AT56		
FBA_CMD27	AR55	FBA_DEBUG0	
FBA_CMD28	BM56	FBA_CMD28	28
FBA_CMD29	BM55	FBA_CMD29	29
FBA_CMD30	BL56	FBA_CMD30	30
FBA_CMD31	BK55	FBA_CMD31	31
FBA_CMD32	BK56	FBA_CMD32	32
FBA_CMD33	BJ56	FBA_CMD33	33
FBA_CMD34	BJ55	FBA_CMD34	34
FBA_CMD35	BH56	FBA_CMD35	35
FBA_CMD36	BG53	FBA_CMD36	36
FBA_CMD37	BG56	FBA_CMD37	37
FBA_CMD38	BF56	FBA_CMD38	38
FBA_CMD39	BF55	FBA_CMD39	39
FBA_CMD40	BE56	FBA_CMD40	40
FBA_CMD41	BD53	FBA_CMD41	41
FBA_CMD42	BD56	FBA_CMD42	42
FBA_CMD43	BC56	FBA_CMD43	43
FBA_CMD44	BC55	FBA_CMD44	44
FBA_CMD45	BB56	FBA_CMD45	45
FBA_CMD46	BA53	FBA_CMD46	46
FBA_CMD47	BA56	FBA_CMD47	47
FBA_CMD48	AY56	FBA_CMD48	48
FBA_CMD49	AY55	FBA_CMD49	49
FBA_CMD50	AW56	FBA_CMD50	50
FBA_CMD51	AV53	FBA_CMD51	51
FBA_CMD52	AV56	FBA_CMD52	52
FBA_CMD53_NC	AU56		
FBA_CMD54_NC	AU55		
FBA_CMD55	AV55	FBA_DEBUG1	

R702 0R 5%

FBA_CLK0	AP48	FBA_CLK0	6
FBA_CLK0	AP47	FBA_CLK0*	6
FBA_CLK1	AR48	FBA_CLK1	7
FBA_CLK1	AR47	FBA_CLK1*	7

FB_CLK → OUT

FBA_WCK01	AE48	FBA_WCK01	6
FBA_WCK01	AE47	FBA_WCK01*	6
FBA_WCKB01	AC48	FBA_WCKB01	6
FBA_WCKB01	AC47	FBA_WCKB01*	6
FBA_WCK23	AL48	FBA_WCK23	6
FBA_WCK23	AL47	FBA_WCK23*	6
FBA_WCKB23	AJ48	FBA_WCKB23	6
FBA_WCKB23	AJ47	FBA_WCKB23*	6
FBA_WCK45	BA47	FBA_WCK45	7
FBA_WCK45	BA48	FBA_WCK45*	7
FBA_WCKB45	BC48	FBA_WCKB45	7
FBA_WCKB45	BC47	FBA_WCKB45*	7
FBA_WCK67	AU48	FBA_WCK67	7
FBA_WCK67	AU47	FBA_WCK67*	7
FBA_WCKB67	AV48	FBA_WCKB67	7
FBA_WCKB67	AV47	FBA_WCKB67*	7

FB_WCK → OUT

FB_PLLVDD	AC46		
FB_PLLVDD	AE11		
FB_PLLVDD	AP46		

1V8_FB_PLL 5,10 → IN

C851 1uF 6.3V 10% X6S 0402 COMMON
C930 1uF 6.3V 10% X6S 0402 COMMON
C996 1uF 6.3V 10% X6S 0402 COMMON

BN37	GND		
BN38	GND		
BN39	GND		
BN4	GND		
BN40	GND		
BN41	GND		
BN42	GND		
BN43	GND		

GA1XX GDDR6 CMD Mapping

Lower 0..31	DRAM1	CHA-Byte 0,1	Upper 32..63	DRAM2	CHA-Byte 4,5
CA0_A	CMD1		CMD33		
CA1_A	CMD13		CMD45		
CA2_A	CMD12		CMD35		
CA3_A	CMD24		CMD46		
CA4_A	CMD11		CMD36		
CA5_A	CMD15		CMD43		
CA6_A	CMD22		CMD48		
CA7_A	CMD23		CMD47		
CA8_A	CMD0		CMD34		
CA9_A	CMD2		CMD32		
CABI_A	CMD10		CMD37		
CKE_A	CMD14		CMD44		
		CHB-Byte 2,3			CHB-Byte 6,7
CA0_B	CMD5		CMD29		
CA1_B	CMD18		CMD52		
CA2_B	CMD7		CMD40		
CA3_B	CMD20		CMD50		
CA4_B	CMD8		CMD39		
CA5_B	CMD16		CMD42		
CA6_B	CMD21		CMD49		
CA7_B	CMD19		CMD51		
CA8_B	CMD6		CMD28		
CA9_B	CMD4		CMD30		
CABI_B	CMD9		CMD38		
CKE_B	CMD17		CMD41		
RESET*	CMD3		CMD31		

CKE_A
FBA_CMD14
FBA_CMD44

RST*
FBA_CMD3
FBA_CMD31

CKE_B
FBA_CMD17
FBA_CMD41

FBVDDQ

R696 10k 5% 0402 COMMON
R291 10k 5% 0402 COMMON
R716 10k 5% 0402 COMMON
R681 10k 5% 0402 COMMON
R300 10k 5% 0402 COMMON
R707 10k 5% 0402 COMMON

1V8 → LB501 30ohm COMMON BEAD_0603 → 1V8_FB_PLL 5,10 → OUT

C992 4.7uF 6.3V 20% X6S 0603 COMMON
C1016 4.7uF 6.3V 20% X6S 0603 COMMON
C988 22uF 4V 20% X6S 0805 COMMON

2x 0603 4.7uF
1x 0805 22uF
Near the GPU

G1C

BGA2714
COMMON

3/24 FBB

FB_DATA
FBB_D[63..0]

FB_DBI
FBB_DBI[7..0]

FB_EDC
FBB_EDC[7..0]

FB_CMD
FBB_CMD[52..0]

0	FBB_D0	D37	FBB_D0
1	FBB_D1	J37	FBB_D1
2	FBB_D2	G37	FBB_D2
3	FBB_D3	F37	FBB_D3
4	FBB_D4	H38	FBB_D4
5	FBB_D5	E38	FBB_D5
6	FBB_D6	F40	FBB_D6
7	FBB_D7	D40	FBB_D7
8	FBB_D8	F34	FBB_D8
9	FBB_D9	J34	FBB_D9
10	FBB_D10	D34	FBB_D10
11	FBB_D11	G34	FBB_D11
12	FBB_D12	E35	FBB_D12
13	FBB_D13	K34	FBB_D13
14	FBB_D14	H35	FBB_D14
15	FBB_D15	K35	FBB_D15
16	FBB_D16	G47	FBB_D16
17	FBB_D17	E44	FBB_D17
18	FBB_D18	F46	FBB_D18
19	FBB_D19	F44	FBB_D19
20	FBB_D20	E46	FBB_D20
21	FBB_D21	C47	FBB_D21
22	FBB_D22	E47	FBB_D22
23	FBB_D23	C49	FBB_D23
24	FBB_D24	G40	FBB_D24
25	FBB_D25	C41	FBB_D25
26	FBB_D26	E41	FBB_D26
27	FBB_D27	F41	FBB_D27
28	FBB_D28	F43	FBB_D28
29	FBB_D29	C44	FBB_D29
30	FBB_D30	H41	FBB_D30
31	FBB_D31	H44	FBB_D31
32	FBB_D32	L51	FBB_D32
33	FBB_D33	L52	FBB_D33
34	FBB_D34	N51	FBB_D34
35	FBB_D35	L49	FBB_D35
36	FBB_D36	L54	FBB_D36
37	FBB_D37	N47	FBB_D37
38	FBB_D38	P51	FBB_D38
39	FBB_D39	P49	FBB_D39
40	FBB_D40	T51	FBB_D40
41	FBB_D41	P52	FBB_D41
42	FBB_D42	P54	FBB_D42
43	FBB_D43	U47	FBB_D43
44	FBB_D44	U51	FBB_D44
45	FBB_D45	U52	FBB_D45
46	FBB_D46	U54	FBB_D46
47	FBB_D47	U49	FBB_D47
48	FBB_D48	D52	FBB_D48
49	FBB_D49	C53	FBB_D49
50	FBB_D50	C54	FBB_D50
51	FBB_D51	C55	FBB_D51
52	FBB_D52	D55	FBB_D52
53	FBB_D53	D54	FBB_D53
54	FBB_D54	F56	FBB_D54
55	FBB_D55	F49	FBB_D55
56	FBB_D56	G53	FBB_D56
57	FBB_D57	H49	FBB_D57
58	FBB_D58	H51	FBB_D58
59	FBB_D59	G51	FBB_D59
60	FBB_D60	H52	FBB_D60
61	FBB_D61	H54	FBB_D61
62	FBB_D62	K48	FBB_D62
63	FBB_D63	K51	FBB_D63

0	FBB_DBI0	F38	FBB_DQM0
1	FBB_DBI1	F35	FBB_DQM1
2	FBB_DBI2	G46	FBB_DQM2
3	FBB_DBI3	G43	FBB_DQM3
4	FBB_DBI4	N50	FBB_DQM4
5	FBB_DBI5	T50	FBB_DQM5
6	FBB_DBI6	E49	FBB_DQM6
7	FBB_DBI7	K50	FBB_DQM7

0	FBB_EDC0	C38	FBB_DQS_WP0
1	FBB_EDC1	C35	FBB_DQS_WP1
2	FBB_EDC2	D46	FBB_DQS_WP2
3	FBB_EDC3	D43	FBB_DQS_WP3
4	FBB_EDC4	N53	FBB_DQS_WP4
5	FBB_EDC5	T53	FBB_DQS_WP5
6	FBB_EDC6	E53	FBB_DQS_WP6
7	FBB_EDC7	K53	FBB_DQS_WP7

FBB_CMD0	B37	FBB_CMD0	0
FBB_CMD1	A37	FBB_CMD1	1
FBB_CMD2	A38	FBB_CMD2	2
FBB_CMD3	D38	FBB_CMD3	3
FBB_CMD4	A39	FBB_CMD4	4
FBB_CMD5	B40	FBB_CMD5	5
FBB_CMD6	A40	FBB_CMD6	6
FBB_CMD7	A41	FBB_CMD7	7
FBB_CMD8	D41	FBB_CMD8	8
FBB_CMD9	A42	FBB_CMD9	9
FBB_CMD10	B43	FBB_CMD10	10
FBB_CMD11	A43	FBB_CMD11	11
FBB_CMD12	A44	FBB_CMD12	12
FBB_CMD13	D44	FBB_CMD13	13
FBB_CMD14	A45	FBB_CMD14	14
FBB_CMD15	B46	FBB_CMD15	15
FBB_CMD16	A46	FBB_CMD16	16
FBB_CMD17	A47	FBB_CMD17	17
FBB_CMD18	D47	FBB_CMD18	18
FBB_CMD19	A48	FBB_CMD19	19
FBB_CMD20	B49	FBB_CMD20	20
FBB_CMD21	A49	FBB_CMD21	21
FBB_CMD22	B50	FBB_CMD22	22
FBB_CMD23	A50	FBB_CMD23	23
FBB_CMD24	C50	FBB_CMD24	24
FBB_CMD25_NC	A51		
FBB_CMD26_NC	B52		
FBB_CMD27	C52	FBB_DEBUG0	
FBB_CMD28	Y56	FBB_CMD28	28
FBB_CMD29	W56	FBB_CMD29	29
FBB_CMD30	W55	FBB_CMD30	30
FBB_CMD31	V56	FBB_CMD31	31
FBB_CMD32	U53	FBB_CMD32	32
FBB_CMD33	U56	FBB_CMD33	33
FBB_CMD34	T56	FBB_CMD34	34
FBB_CMD35	T55	FBB_CMD35	35
FBB_CMD36	R56	FBB_CMD36	36
FBB_CMD37	P53	FBB_CMD37	37
FBB_CMD38	P56	FBB_CMD38	38
FBB_CMD39	N56	FBB_CMD39	39
FBB_CMD40	N55	FBB_CMD40	40
FBB_CMD41	M56	FBB_CMD41	41
FBB_CMD42	L53	FBB_CMD42	42
FBB_CMD43	L56	FBB_CMD43	43
FBB_CMD44	K56	FBB_CMD44	44
FBB_CMD45	K55	FBB_CMD45	45
FBB_CMD46	J56	FBB_CMD46	46
FBB_CMD47	H53	FBB_CMD47	47
FBB_CMD48	H56	FBB_CMD48	48
FBB_CMD49	G56	FBB_CMD49	49
FBB_CMD50	G55	FBB_CMD50	50
FBB_CMD51	E56	FBB_CMD51	51
FBB_CMD52	B54	FBB_CMD52	52
FBB_CMD53_NC	B53		
FBB_CMD54_NC	A52		
FBB_CMD55	E55	FBB_DEBUG1	

R675 0R 5%

FBB_CLK0	K44	FBB_CLK0	8
FBB_CLK0	J44	FBB_CLK0*	8
FBB_CLK1	J46	FBB_CLK1	9
FBB_CLK1	K46	FBB_CLK1*	9

FB_CLK → OUT

FBB_WCK01	J40	FBB_WCK01	8
FBB_WCK01	K40	FBB_WCK01*	8
FBB_WCKB01	K38	FBB_WCKB01	8
FBB_WCKB01	J38	FBB_WCKB01*	8
FBB_WCK23	J43	FBB_WCK23	8
FBB_WCK23	K43	FBB_WCK23*	8
FBB_WCKB23	K41	FBB_WCKB23	8
FBB_WCKB23	J41	FBB_WCKB23*	8
FBB_WCK45	P47	FBB_WCK45	9
FBB_WCK45	P48	FBB_WCK45*	9
FBB_WCKB45	T48	FBB_WCKB45	9
FBB_WCKB45	T47	FBB_WCKB45*	9
FBB_WCK67	K47	FBB_WCK67	9
FBB_WCK67	J47	FBB_WCK67*	9
FBB_WCKB67	L47	FBB_WCKB67	9
FBB_WCKB67	L48	FBB_WCKB67*	9

FB_WCK → OUT

FB_PLLVDD	L17		

1V8_FB_PLL 5,10 → IN

C712 1uF 6.3V 10% X6S 0402 COMMON

BN44	GND		
BN45	GND		
BN46	GND		
BN47	GND		
BN48	GND		
BN6	GND		
BN9	GND		
BP1	GND		

CKE_B
FBB_CMD17
FBB_CMD41

FBVDDQ

R666 10k 5% 0402 COMMON
R311 10k 5% 0402 COMMON
R679 10k 5% 0402 COMMON
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R671 10k 5% 0402 COMMON

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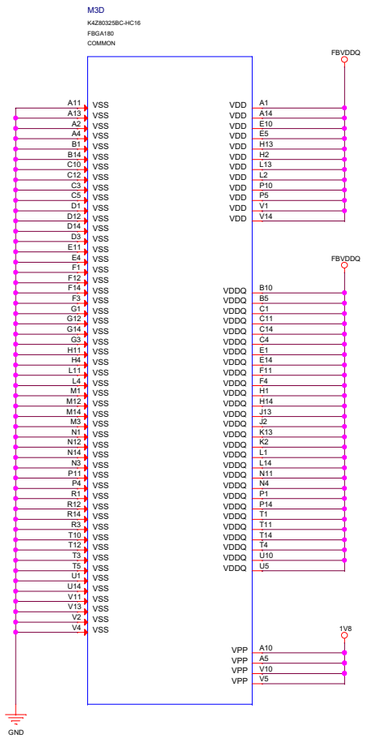
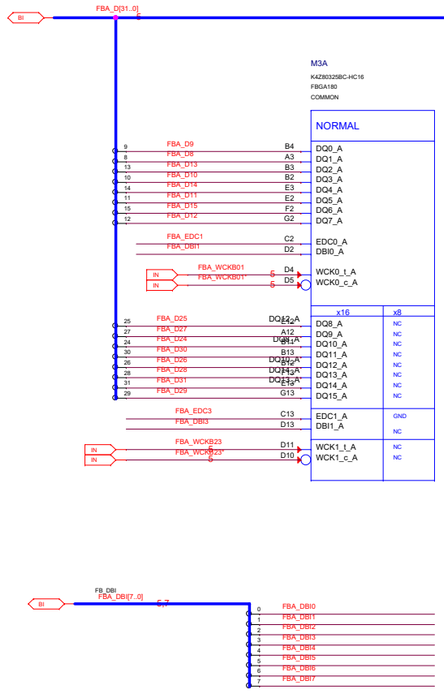
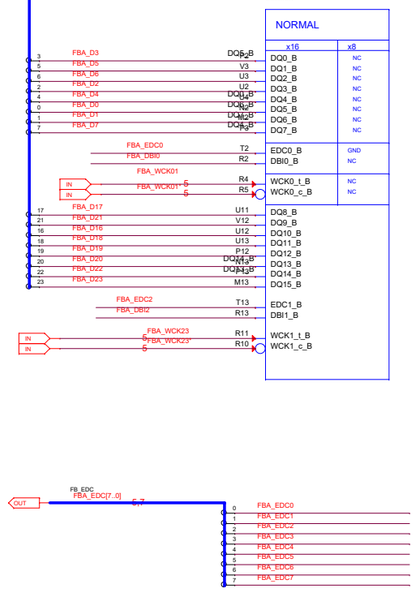
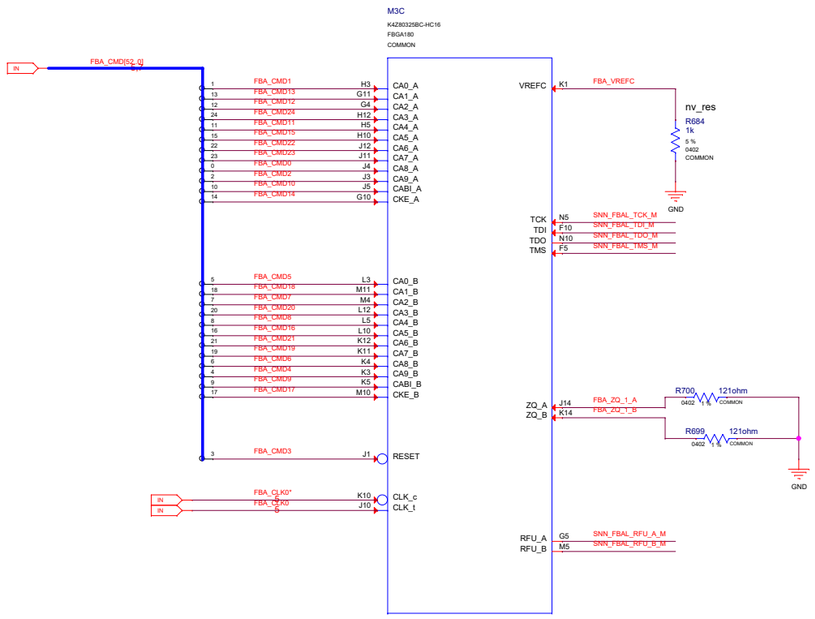
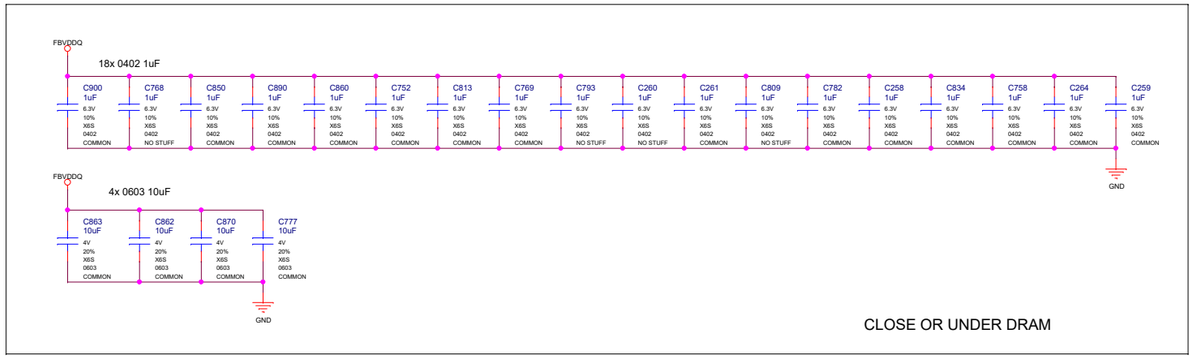


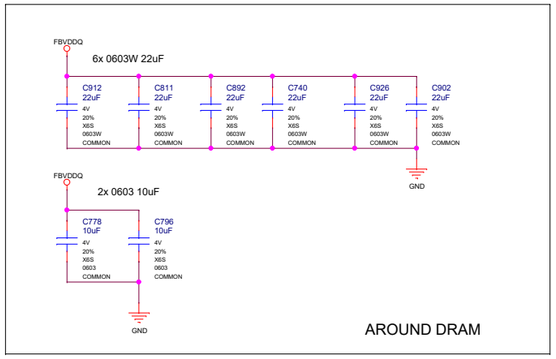


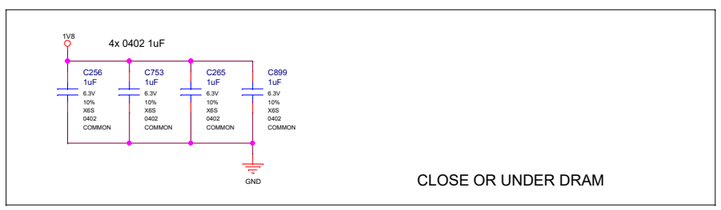




decap via : at least 2 gnd vias and 2 power vias for each cap







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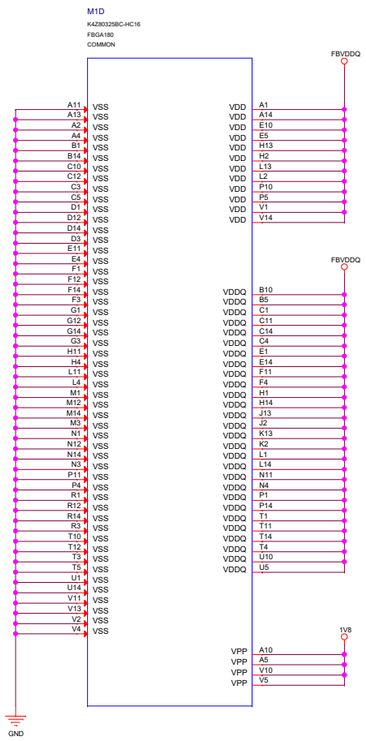

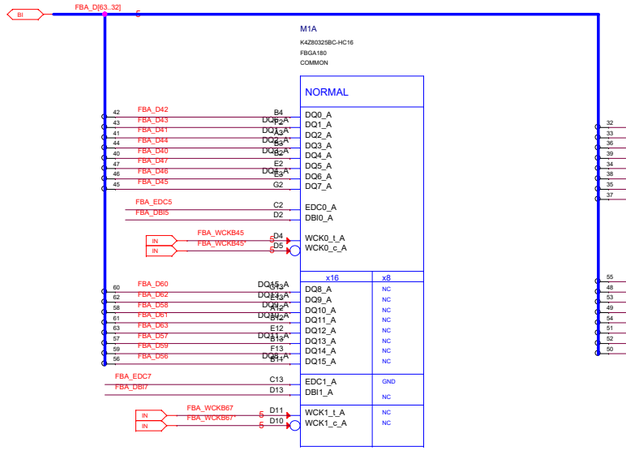

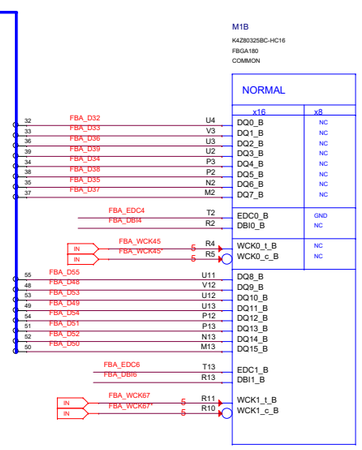

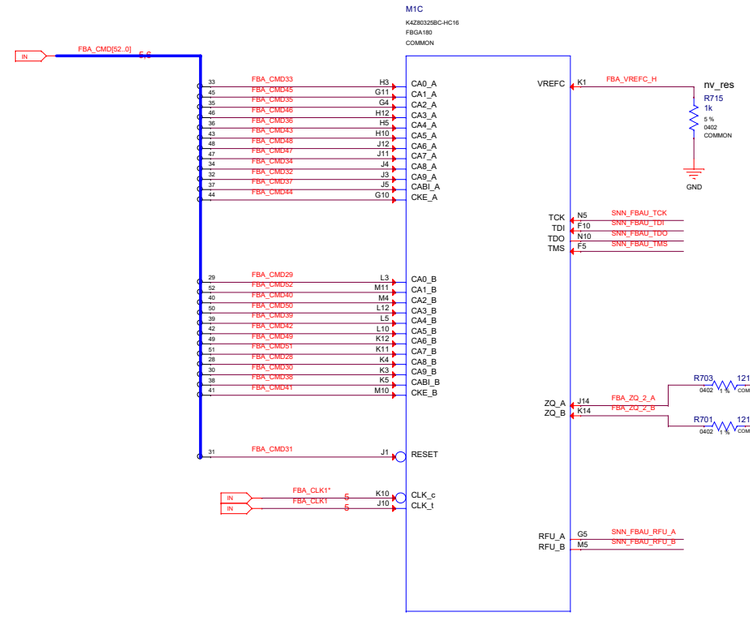

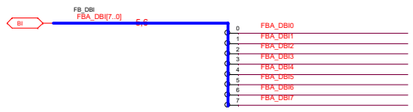

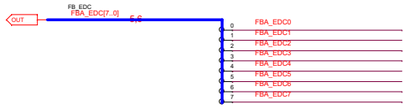

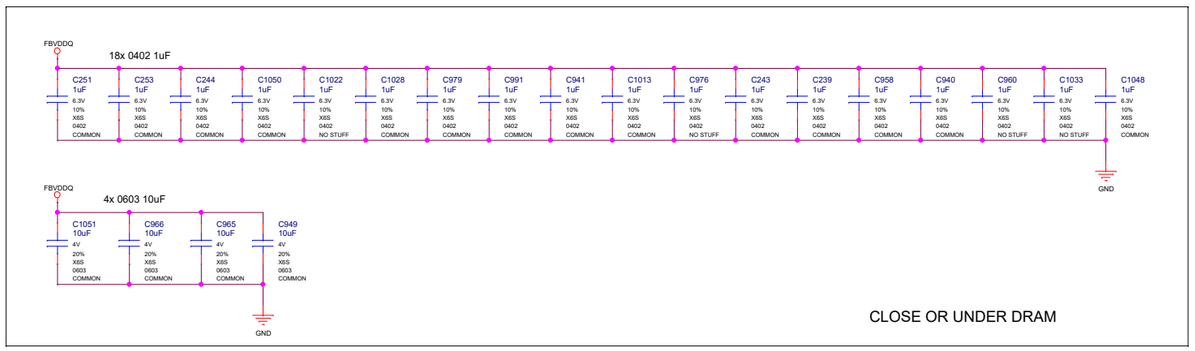

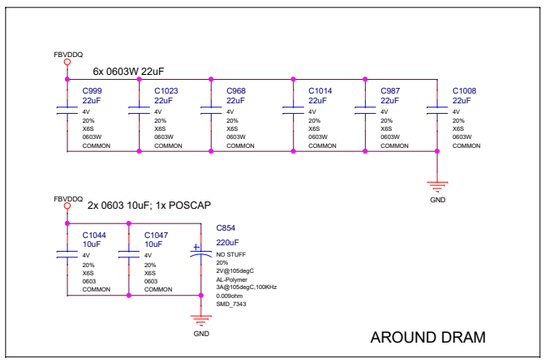

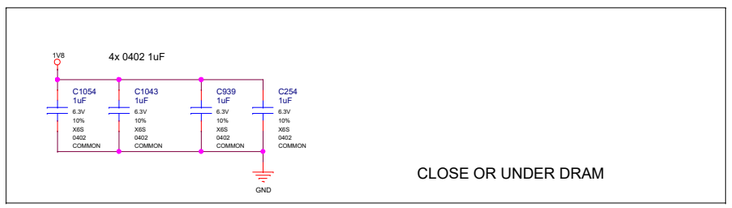

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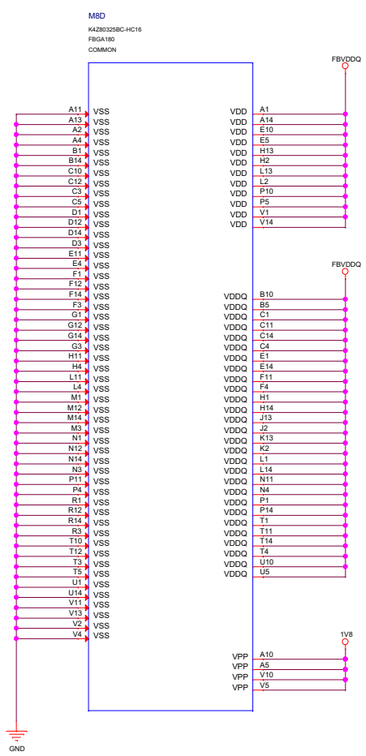

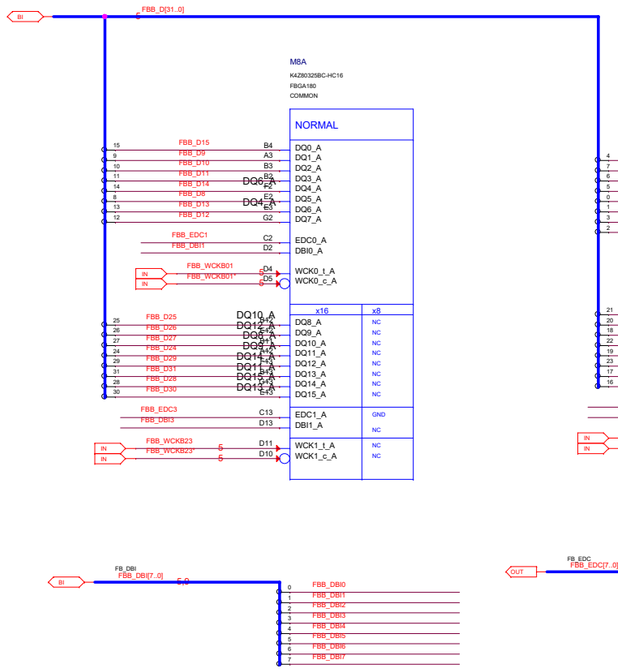

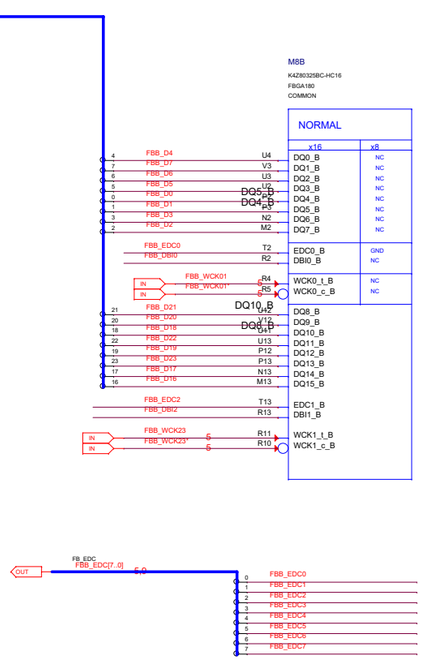

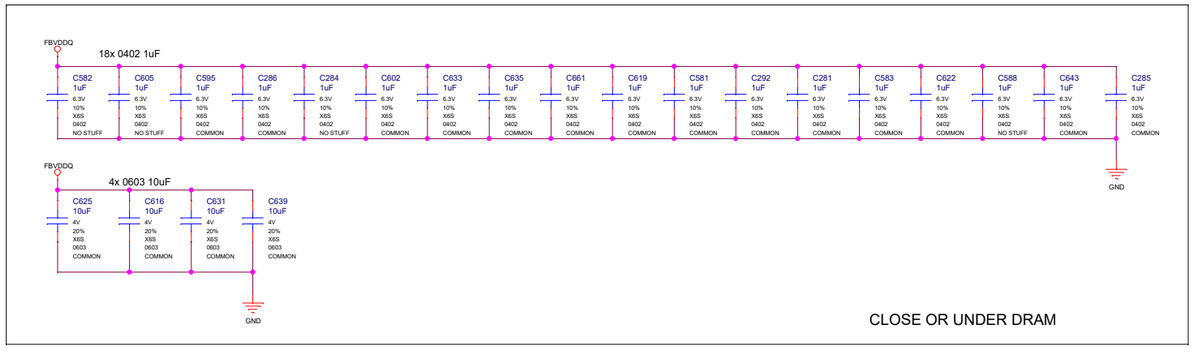

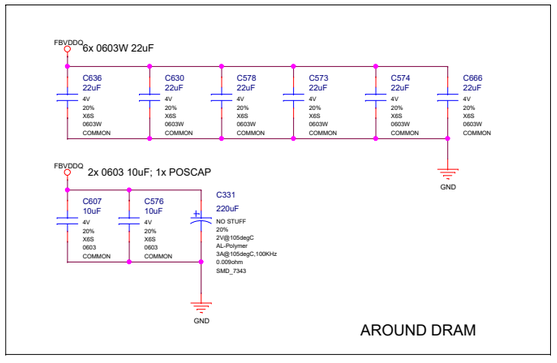

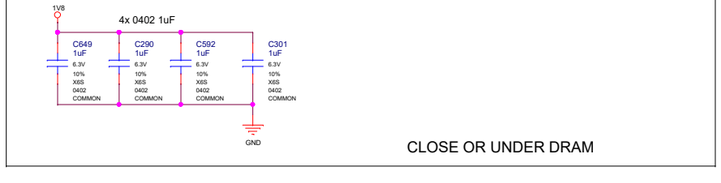

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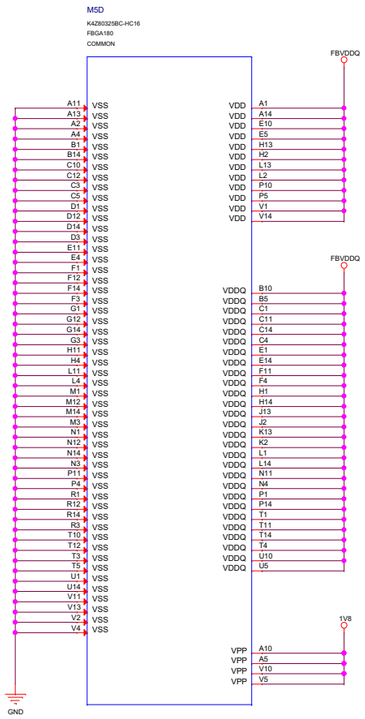

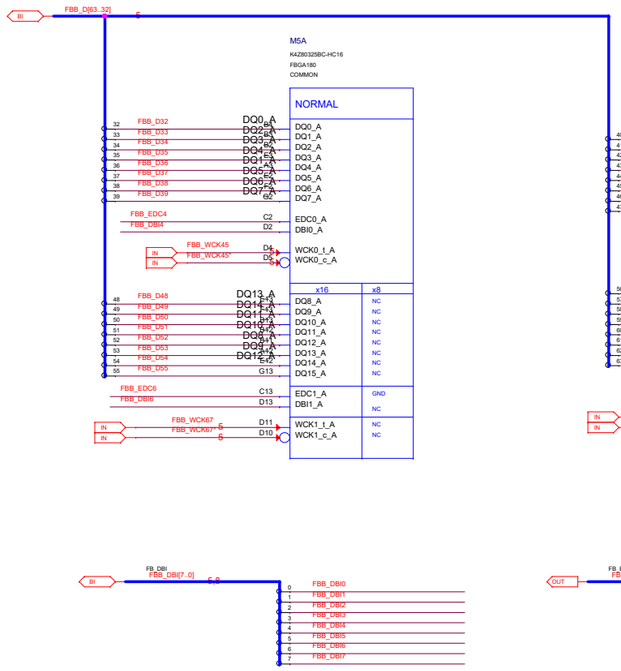

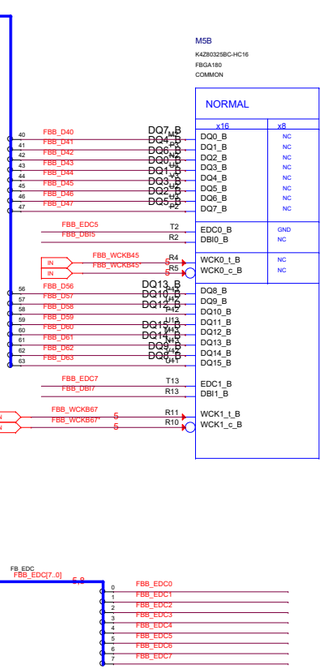

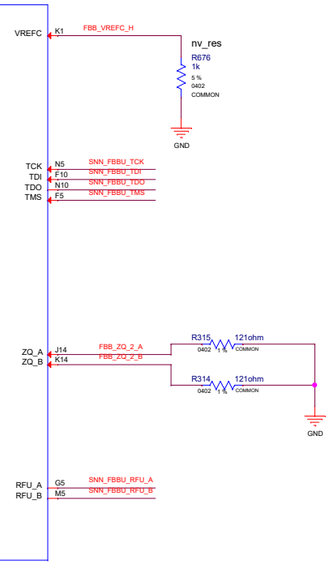

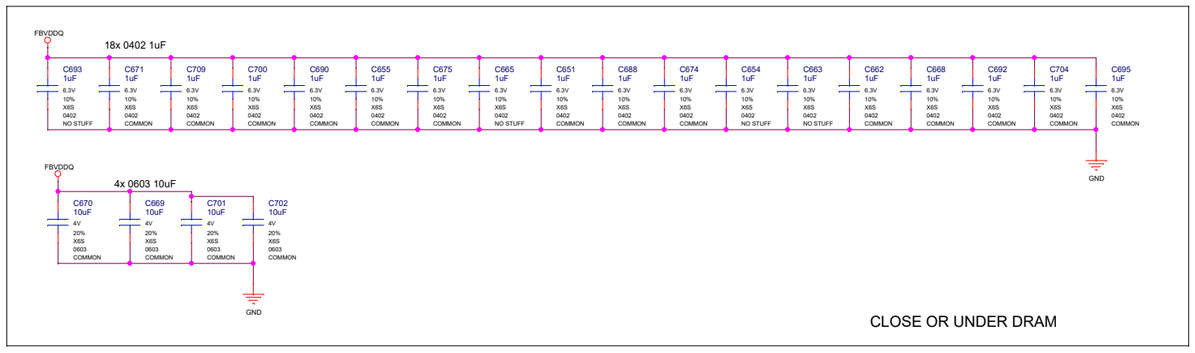

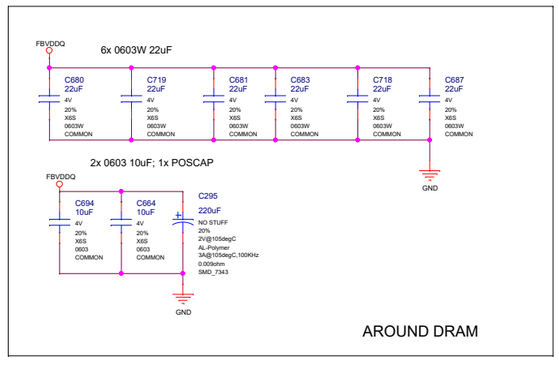

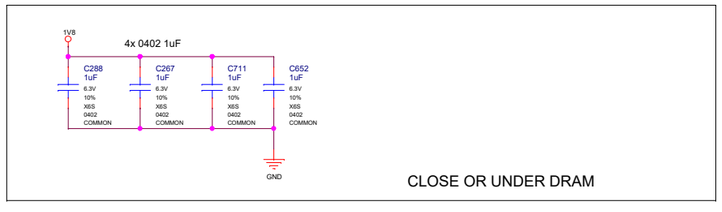

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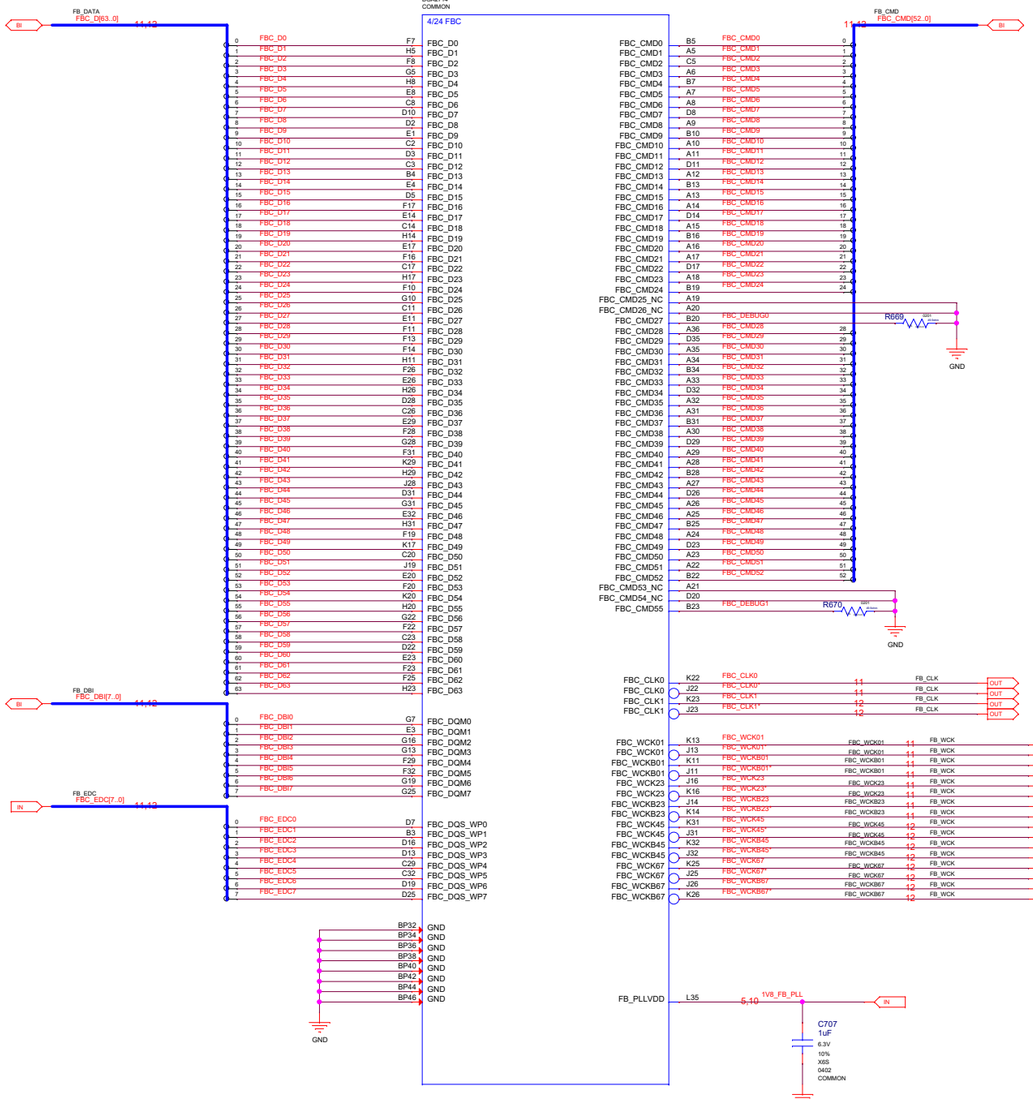

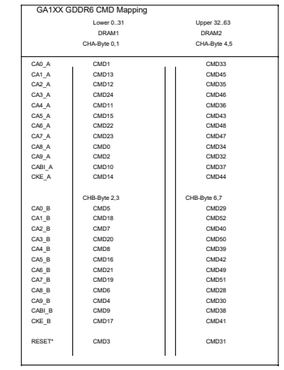

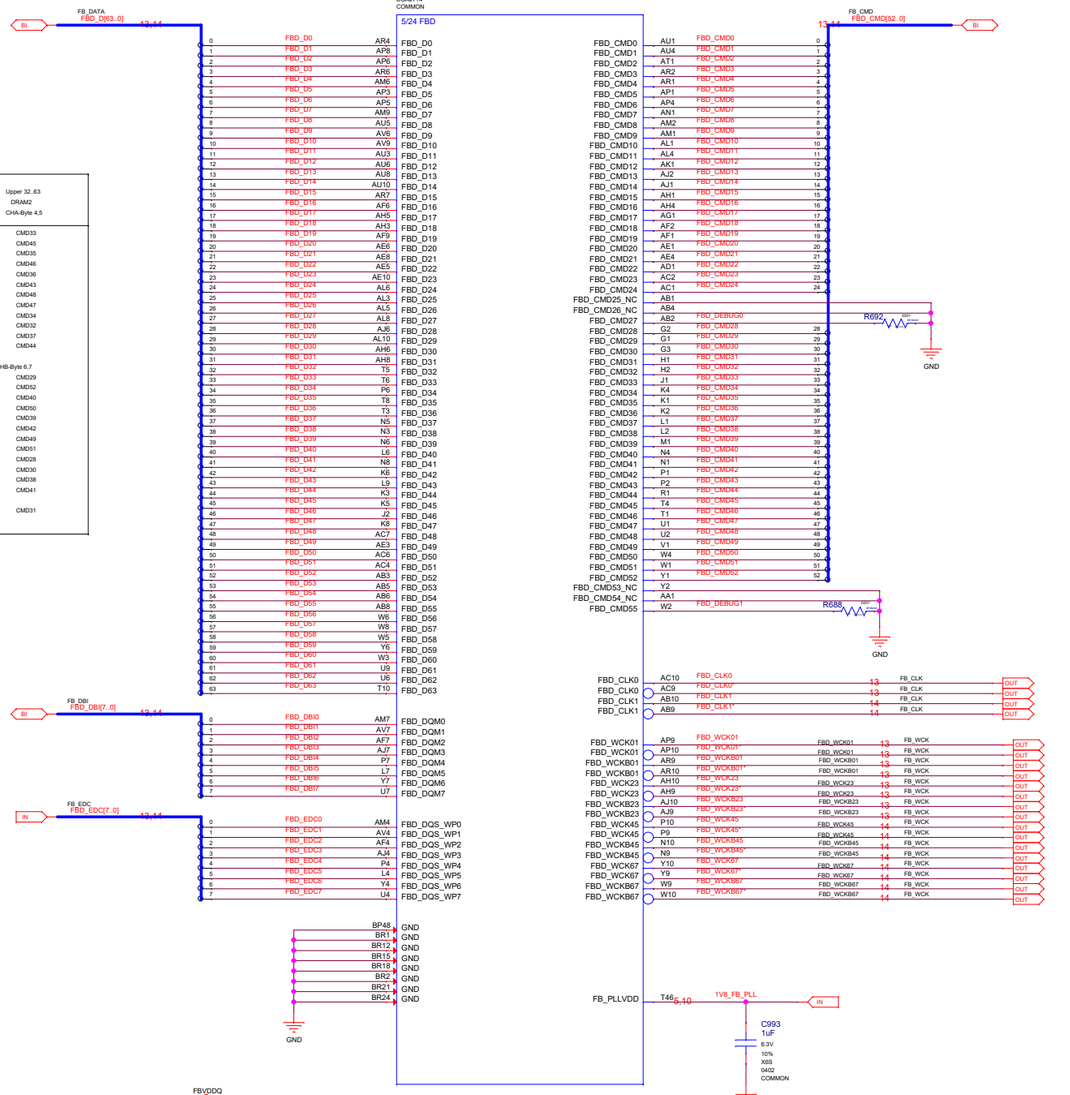

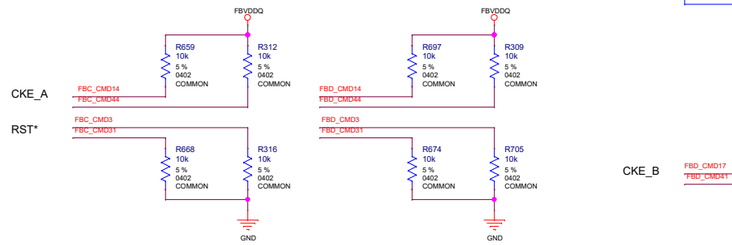

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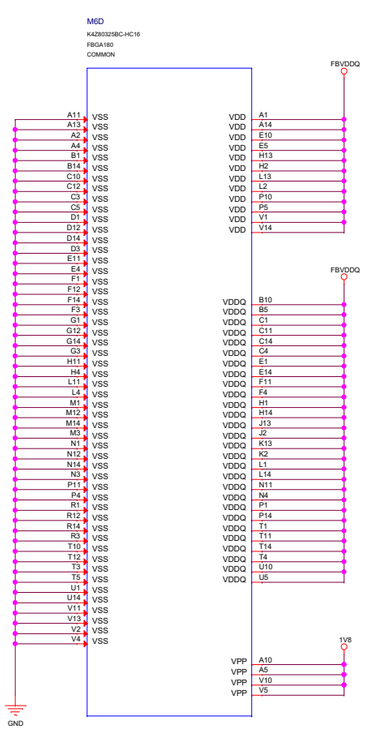

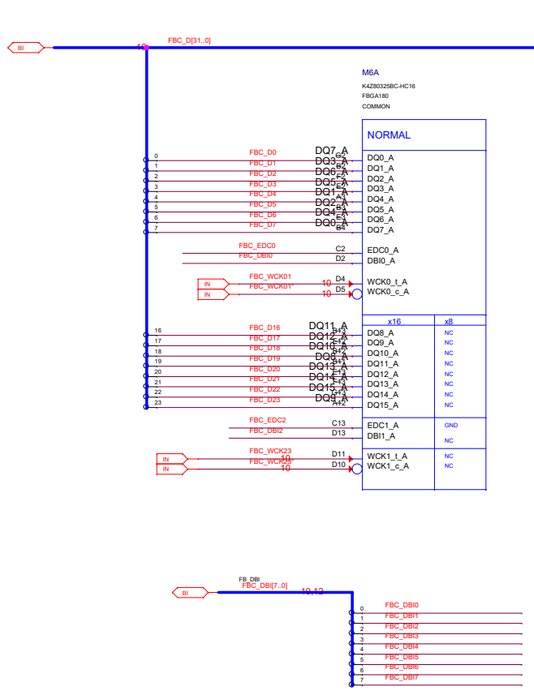

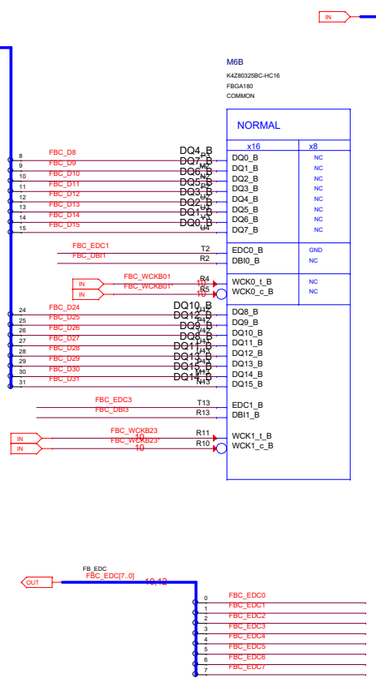

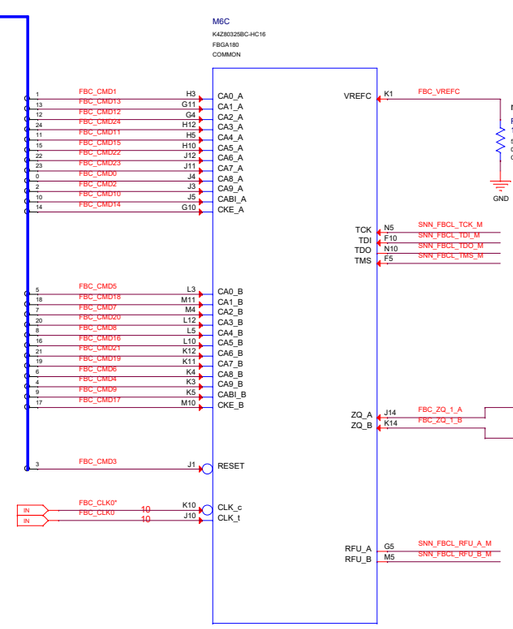

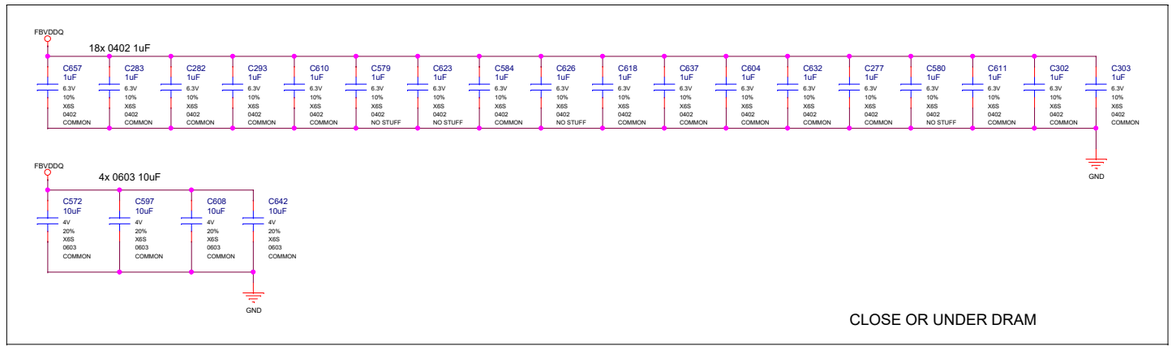

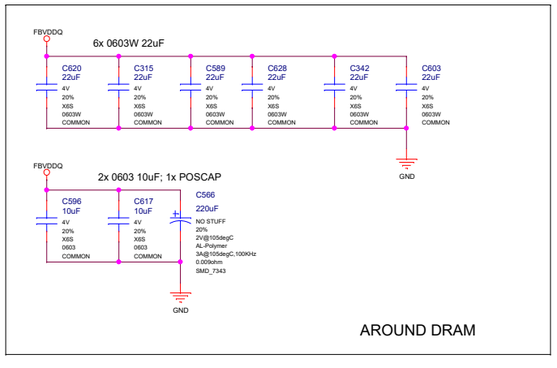

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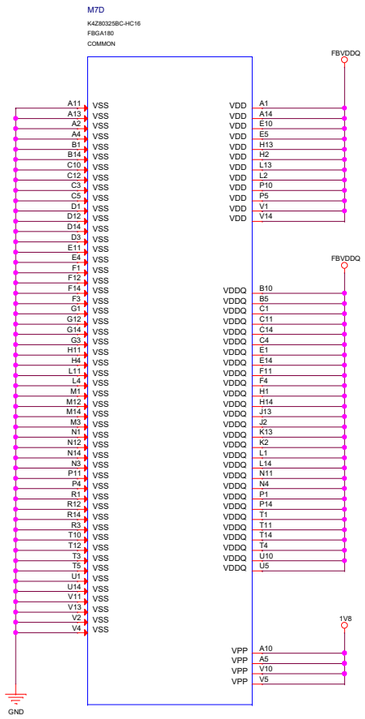

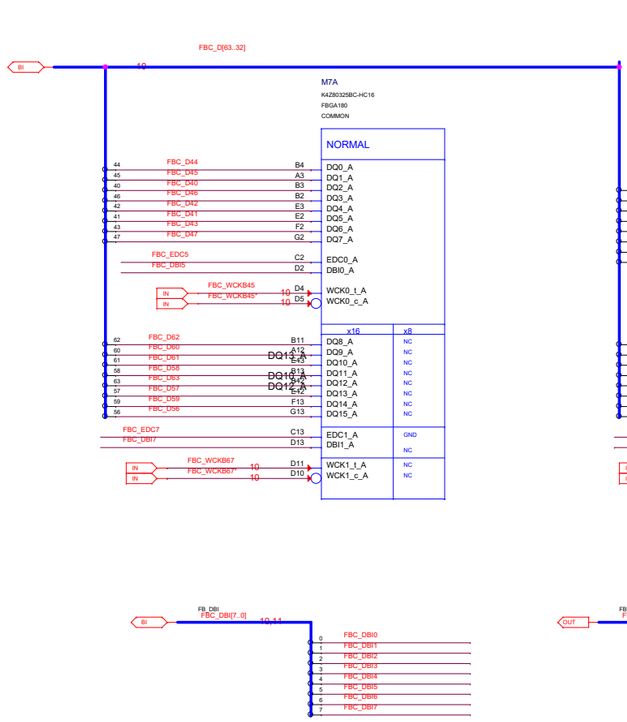

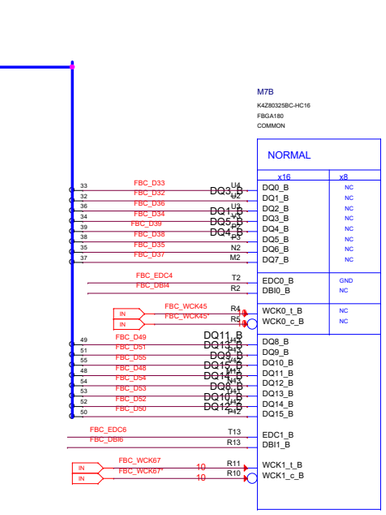

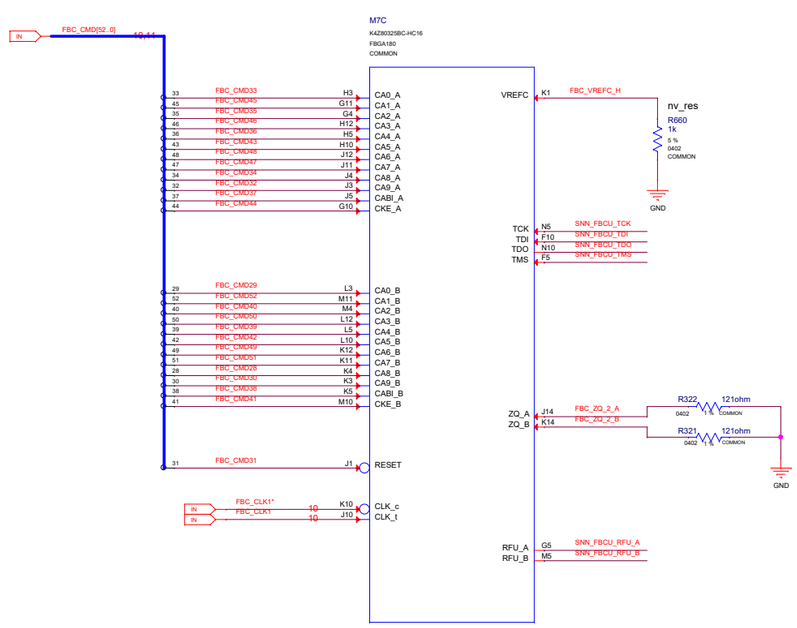

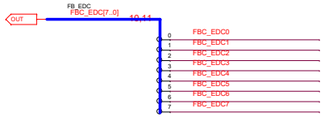

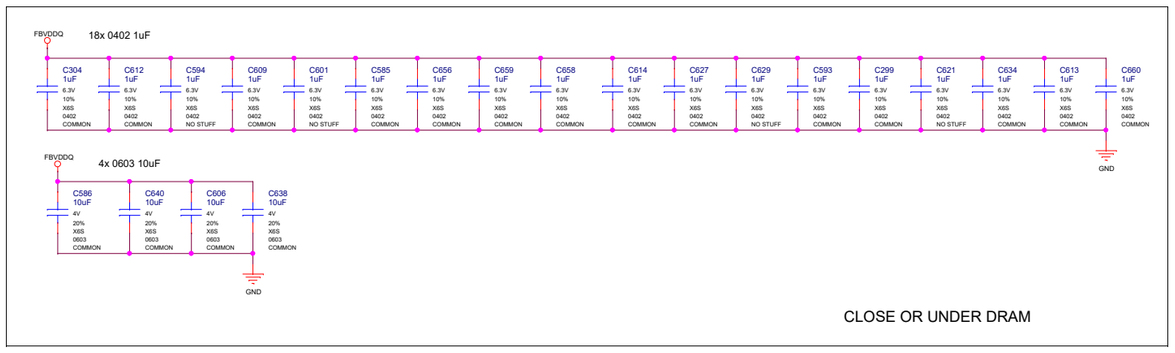

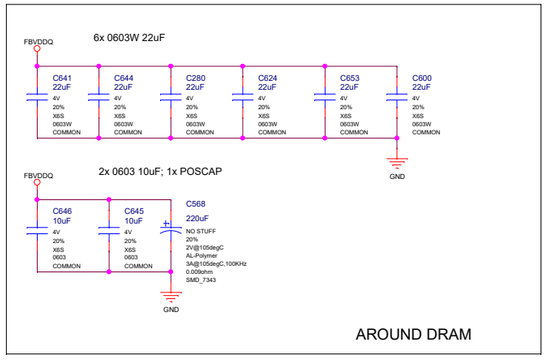

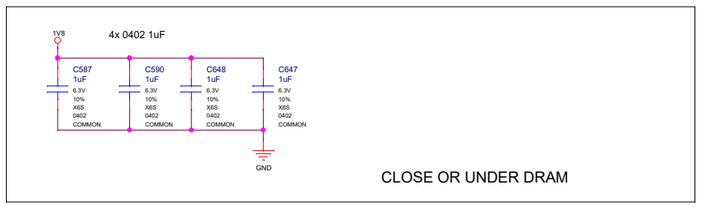

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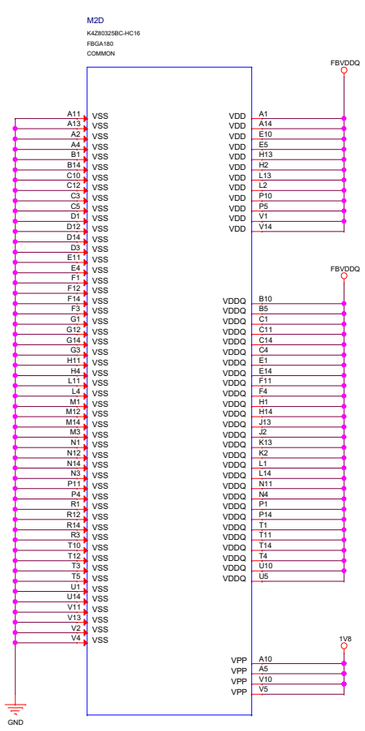

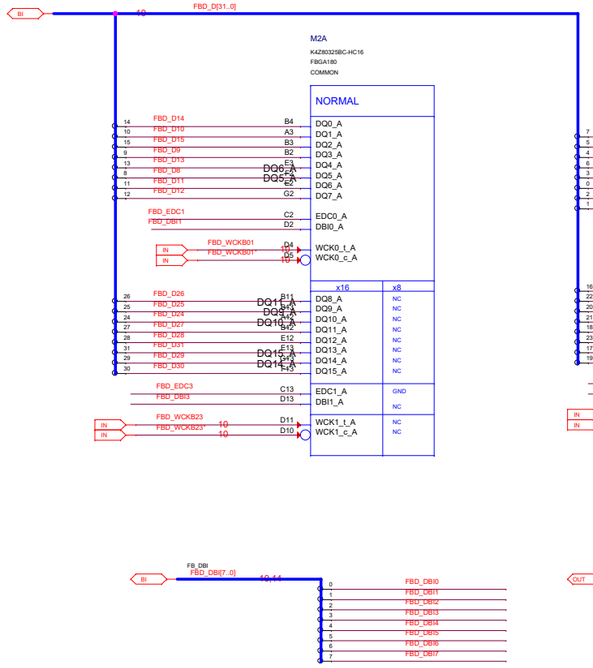

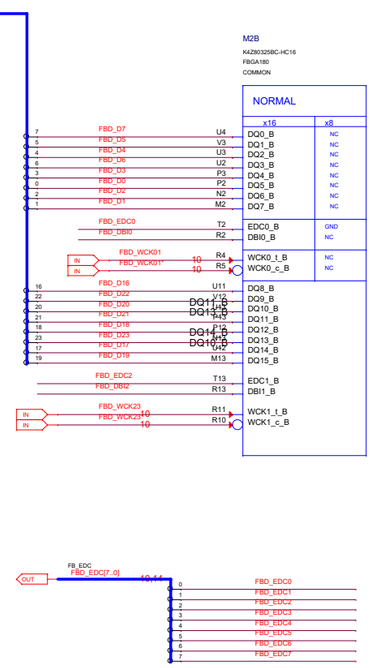

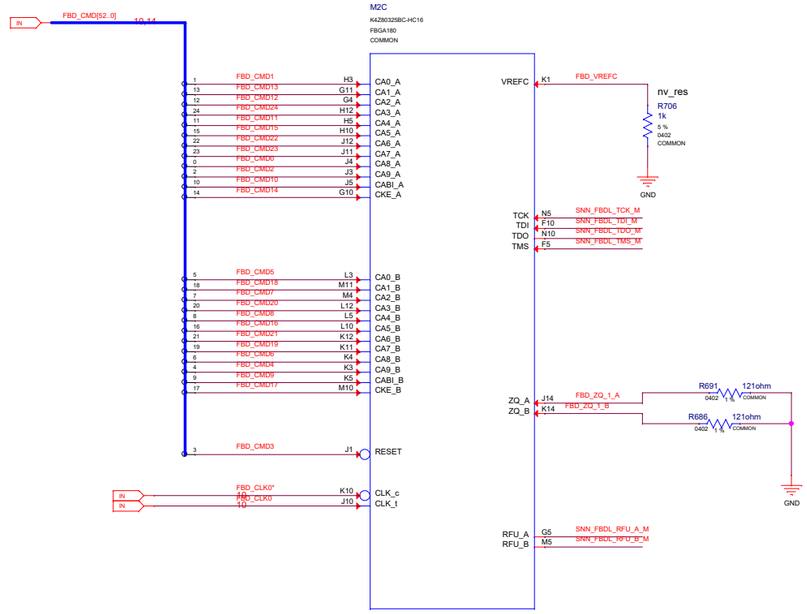

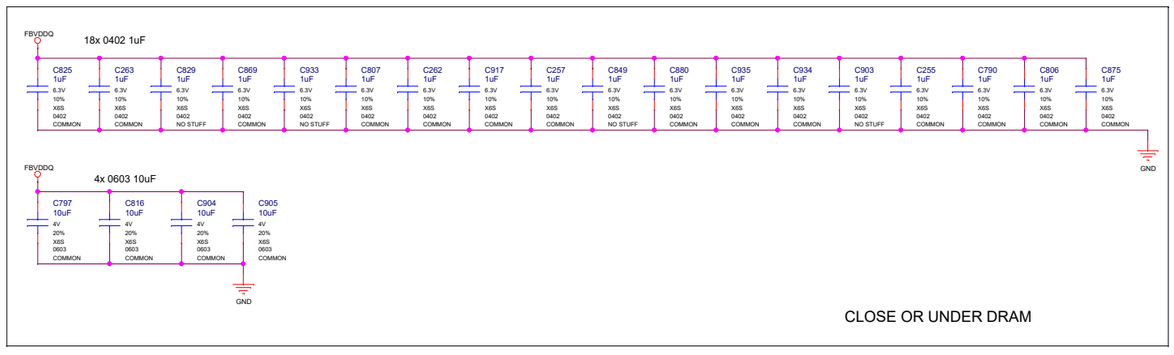

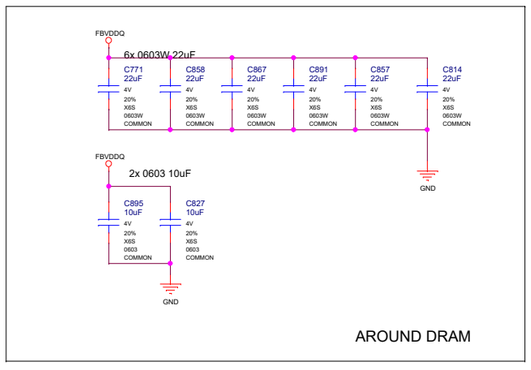

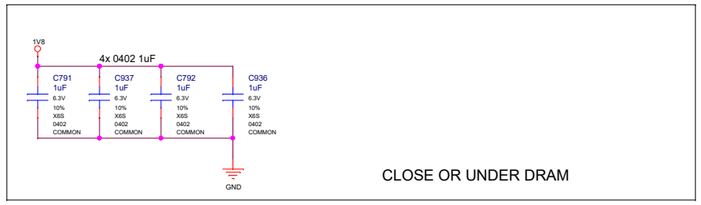

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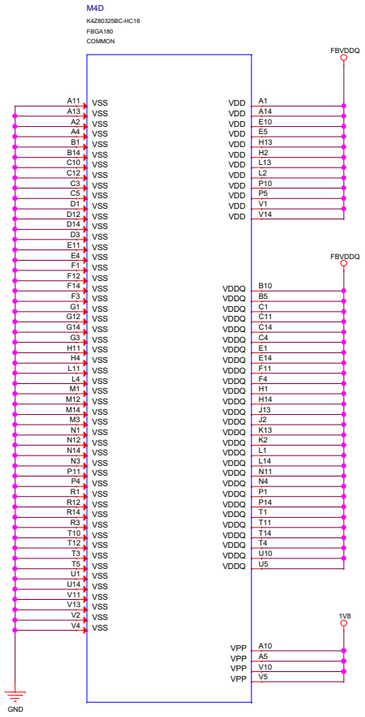

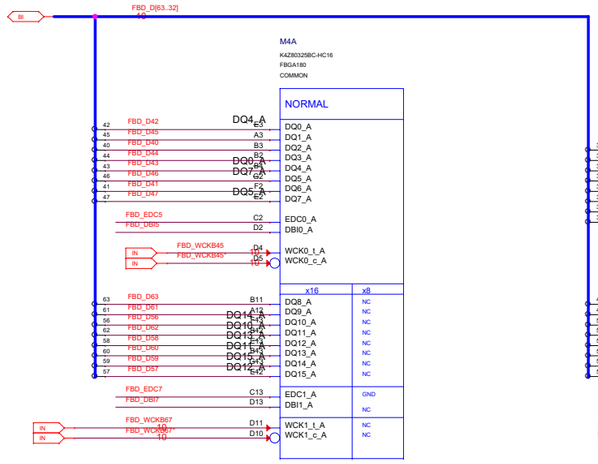

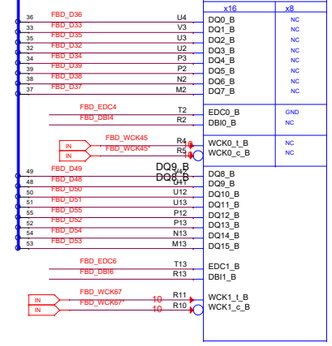

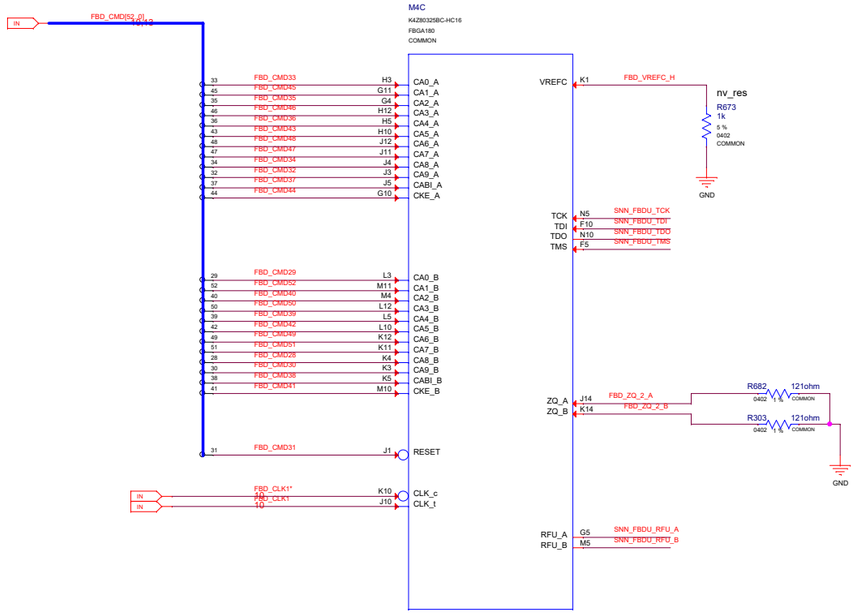

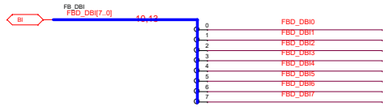

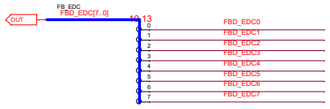

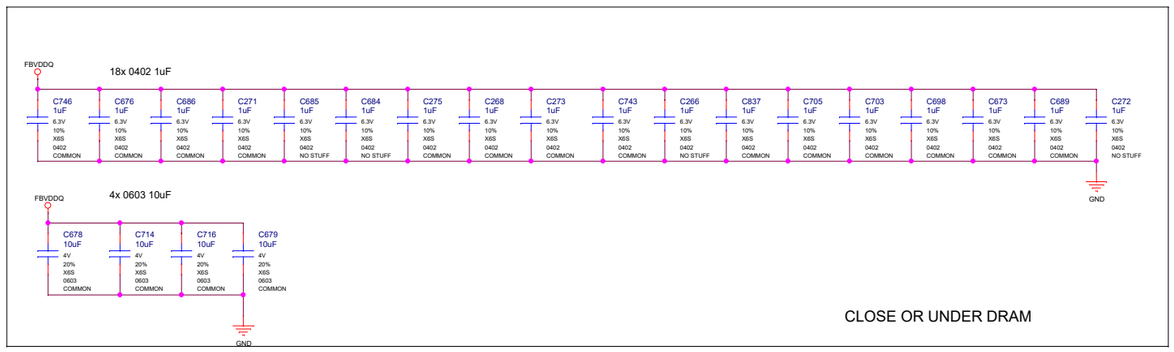

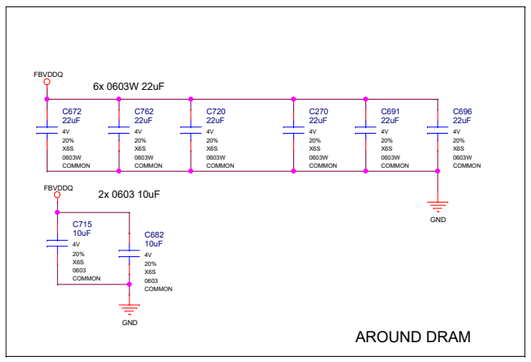

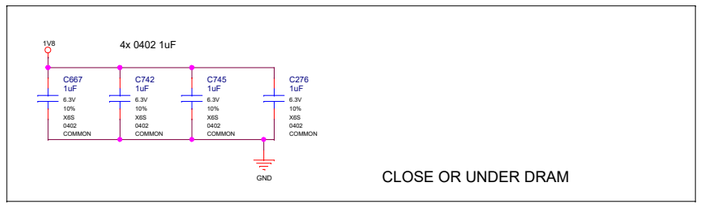

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AN40	GND	GND	AW31
AN41	GND	GND	AW32
AN42	GND	GND	AW33
AN43	GND	GND	AW34
AN44	GND	GND	AW35
AN47	GND	GND	AW36
AN49	GND	GND	AW37
AN51	GND	GND	AW38
AN53	GND	GND	AW39
AN55	GND	GND	AW4
AN8	GND	GND	AW40
AN9	GND	GND	AW41
AP2	GND	GND	AW42
AP49	GND	GND	AW43
AP52	GND	GND	AW47
AP54	GND	GND	AW49
AP7	GND	GND	AW51
AR13	GND	GND	AW53
AR14	GND	GND	AW55
AR15	GND	GND	AW6
AR16	GND	GND	AW8
AR17	GND	GND	AY47
AR18	GND	GND	AY49
AR19	GND	GND	AY52
AR20	GND	GND	AY54
AR21	GND	GND	B1
AR22	GND	GND	B11
AR23	GND	GND	B12
AR24	GND	GND	B14
AR25	GND	GND	B15
AR26	GND	GND	B17
AR27	GND	GND	B18
AR28	GND	GND	B2
AR29	GND	GND	B21
AR3	GND	GND	B24
AR30	GND	GND	B26
AR31	GND	GND	B27
AR32	GND	GND	B29
AR33	GND	GND	B30
AR34	GND	GND	B32
AR35	GND	GND	B33
AR36	GND	GND	B35
AR37	GND	GND	B36
AR38	GND	GND	AR40
AR39	GND	GND	AR41

G1H — BGA2714 COMMON — 21/24 GND_3/5

B39	GND	GND	BE6
B41	GND	GND	BE8
B42	GND	GND	BF52
B44	GND	GND	BF54
B45	GND	GND	BG12
B47	GND	GND	BG15
B48	GND	GND	BG18
B51	GND	GND	BG21
B55	GND	GND	BG24
B56	GND	GND	BG30
B6	GND	GND	BG33
B8	GND	GND	BG36
B9	GND	GND	BG39
BA14	GND	GND	BG42
BA15	GND	GND	BG49
BA16	GND	GND	BG55
BA17	GND	GND	BH2
BA18	GND	GND	BH4
BA19	GND	GND	BH51
BA20	GND	GND	BH53
BA21	GND	GND	BH55
BA22	GND	GND	BH6
BA23	GND	GND	BH8
BA24	GND	GND	BJ12
BA25	GND	GND	BJ14
BA26	GND	GND	BJ15
BA27	GND	GND	BJ17
BA28	GND	GND	BJ18
BA29	GND	GND	BJ20
BA30	GND	GND	BJ21
BA31	GND	GND	BJ23
BA32	GND	GND	BJ24
BA33	GND	GND	BJ31
BA34	GND	GND	BJ33
BA35	GND	GND	BJ35
BA36	GND	GND	BJ37
BA37	GND	GND	BJ39
BA38	GND	GND	BJ41
BA39	GND	GND	BJ43
BA40	GND	GND	BJ45
BA41	GND	GND	BJ53
BA42	GND	GND	BJ9
BA43	GND	GND	BK31
BA50	GND	GND	BK33
BA55	GND	GND	BK35
BB47	GND	GND	BK37
BB49	GND	GND	BK39
BB51	GND	GND	BK41
BB53	GND	GND	BK43
BB55	GND	GND	BK45
BC14	GND	GND	BK54
BC15	GND	GND	BL12
BC16	GND	GND	BL15
BC17	GND	GND	BL18
BC18	GND	GND	BL2
BC19	GND	GND	BL21
BC20	GND	GND	BL24
BC21	GND	GND	BL30
BC22	GND	GND	BL32
BC23	GND	GND	BL34
BC24	GND	GND	BL36
BC25	GND	GND	BL38
BC26	GND	GND	BL4
BC27	GND	GND	BL40
BC28	GND	GND	BL42
BC29	GND	GND	BL44
BC30	GND	GND	BL46
BC31	GND	GND	BL55
BC32	GND	GND	BL6
BC33	GND	GND	BL9
BC34	GND	GND	BM14
BC35	GND	GND	BM17
BC36	GND	GND	BM20
BC37	GND	GND	BM23
BC38	GND	GND	BM30
BC39	GND	GND	BM32
BC40	GND	GND	BM34
BC41	GND	GND	BM36
BC42	GND	GND	BM38
BC43	GND	GND	BM40
BC49	GND	GND	BM42
BC52	GND	GND	BM44
BC54	GND	GND	BM46
BD15	GND	GND	BM48
BD16	GND	GND	BN10
BD19	GND	GND	BN11
BD20	GND	GND	BN12
BD23	GND	GND	BN13
BD24	GND	GND	BN14
BD27	GND	GND	BN15
BD30	GND	GND	BN16
BD33	GND	GND	BN17
BD34	GND	GND	BN18
BD37	GND	GND	BN19
BD38	GND	GND	BN20
BD41	GND	GND	BN21
BD42	GND	GND	BN22
BD48	GND	GND	BN23
BD50	GND	GND	BN24
BD55	GND	GND	BN30
BE10	GND	GND	BN31
BE2	GND	GND	BN32
BE4	GND	GND	BN33
BE49	GND	GND	BN34
BE51	GND	GND	BN35
BE53	GND	GND	BN36
BE55	GND	GND	BR30

G1I — BGA2714 COMMON — 17/24 VDD_1/2 — NVVDD

AB14	VDD	VDD	AF29
AB15	VDD	VDD	AF30
AB16	VDD	VDD	AF31
AB17	VDD	VDD	AF32
AB18	VDD	VDD	AF33
AB19	VDD	VDD	AF34
AB20	VDD	VDD	AF35
AB21	VDD	VDD	AF36
AB22	VDD	VDD	AF37
AB23	VDD	VDD	AF38
AB24	VDD	VDD	AF39
AB25	VDD	VDD	AF40
AB26	VDD	VDD	AF41
AB27	VDD	VDD	AF42
AB28	VDD	VDD	AF43
AB29	VDD	VDD	AH14
AB30	VDD	VDD	AH15
AB31	VDD	VDD	AH16
AB32	VDD	VDD	AH17
AB33	VDD	VDD	AH18
AB34	VDD	VDD	AH19
AB35	VDD	VDD	AH20
AB36	VDD	VDD	AH21
AB37	VDD	VDD	AH22
AB38	VDD	VDD	AH23
AB39	VDD	VDD	AH24
AB40	VDD	VDD	AH25
AB41	VDD	VDD	AH26
AB42	VDD	VDD	AH27
AB43	VDD	VDD	AH28
AC14	VDD	VDD	AH29
AD15	VDD	VDD	AH30
AD16	VDD	VDD	AH31
AD17	VDD	VDD	AH32
AD18	VDD	VDD	AH33
AD19	VDD	VDD	AH34
AD20	VDD	VDD	AH35
AD21	VDD	VDD	AH36
AD22	VDD	VDD	AH37
AD23	VDD	VDD	AH38
AD24	VDD	VDD	AH39
AD25	VDD	VDD	AH40
AD26	VDD	VDD	AH41
AD27	VDD	VDD	AH42
AD28	VDD	VDD	AH43
AD29	VDD	VDD	AK14
AD30	VDD	VDD	AK15
AD31	VDD	VDD	AK16
AD32	VDD	VDD	AK17
AD33	VDD	VDD	AK18
AD34	VDD	VDD	AK19
AD35	VDD	VDD	AK20
AD36	VDD	VDD	AK21
AD37	VDD	VDD	AK22
AD38	VDD	VDD	AK23
AD39	VDD	VDD	AK24
AD40	VDD	VDD	AK25
AD41	VDD	VDD	AK26
AD42	VDD	VDD	AK27
AD43	VDD	VDD	AK28
AF14	VDD	VDD	AK29
AF15	VDD	VDD	AK30
AF16	VDD	VDD	AK31
AF17	VDD	VDD	AK32
AF18	VDD	VDD	AK33
AF19	VDD	VDD	AK34
AF20	VDD	VDD	AK35
AF21	VDD	VDD	AK36
AF22	VDD	VDD	AK37
AF23	VDD	VDD	V29
AF24	VDD	VDD	V30
AF25	VDD	VDD	V31
AF26	VDD	VDD	V32
AF27	VDD	VDD	V33
AF28	VDD	VDD	V34
T29	VDD	VDD	V35
T30	VDD	VDD	V36
T31	VDD	VDD	V37
T32	VDD	VDD	V38
T33	VDD	VDD	V39
T34	VDD	VDD	V40
T35	VDD	VDD	V41
T36	VDD	VDD	V42
T37	VDD	VDD	V43
T38	VDD	VDD	Y14
T39	VDD	VDD	Y15
T40	VDD	VDD	Y16
T41	VDD	VDD	Y17
T42	VDD	VDD	Y18
T43	VDD	VDD	Y19
V14	VDD	VDD	Y20
V15	VDD	VDD	Y21
V16	VDD	VDD	Y22
V17	VDD	VDD	Y23
V18	VDD	VDD	Y24
V19	VDD	VDD	Y25
V20	VDD	VDD	Y26
V21	VDD	VDD	Y27
V22	VDD	VDD	Y28
V23	VDD	VDD	Y29
V24	VDD	VDD	Y30
V25	VDD	VDD	Y31
V26	VDD	VDD	Y32
V27	VDD	VDD	Y33
V28	VDD		

G1J — BGA2714 COMMON — 20/24 NC/1V8

SNN_GPU_1	AV1	NC	
SNN_GPU_2	AV2	NC	
SNN_GPU_3	BG9	NC	
SNN_GPU_4	BH10	NC	
SNN_GPU_5	BH11	NC	
SNN_GPU_6	BH14	NC	
SNN_GPU_7	BJ16	NC	
SNN_GPU_8	BJ7	NC	
SNN_GPU_9	BJ8	NC	
SNN_GPU_10	BK16	NC	
SNN_GPU_11	BN49	NC	
SNN_GPU_12	BP50	NC	
SNN_GPU_13	BR50	NC	
SNN_GPU_14	BR51	NC	
SNN_GPU_15	BT51	NC	
SNN_GPU_16	D50	NC	
SNN_GPU_17	E50	NC	
SNN_GPU_18	F50	NC	
SNN_GPU_19	G50	NC	
SNN_GPU_20	G6	NC	
SNN_GPU_21	N49	NC	
		1V8	BF10
		1V8	BF11
		1V8	BG10
		1V8	BG11
RSVD_1	A4	SNN_GPU_RSVD_1	
RSVD_2	A53	SNN_GPU_RSVD_2	
RSVD_3	BN1	SNN_GPU_RSVD_3	
RSVD_4	BN56	SNN_GPU_RSVD_4	
RSVD_5	BT4	SNN_GPU_RSVD_5	
RSVD_6	BT53	SNN_GPU_RSVD_6	
RSVD_7	D1	SNN_GPU_RSVD_7	
RSVD_8	D56	SNN_GPU_RSVD_8	
FUSE_SRC			BH25

G1K — BGA2714 COMMON — 18/24 VDD_2/2 — NVVDD

AK38	VDD	VDD	AP39
AK39	VDD	VDD	AP40
AK40	VDD	VDD	AP41
AK41	VDD	VDD	AP42
AK42	VDD	VDD	AP43
AK43	VDD	VDD	P14
AM14	VDD	VDD	P15
AM15	VDD	VDD	P16
AM16	VDD	VDD	P17
AM17	VDD	VDD	P18
AM18	VDD	VDD	P19
AM19	VDD	VDD	P20
AM20	VDD	VDD	P21
AM21	VDD	VDD	P22
AM22	VDD	VDD	P23
AM23	VDD	VDD	P24
AM24	VDD	VDD	P25
AM25	VDD	VDD	P26
AM26	VDD	VDD	P27
AM27	VDD	VDD	P28
AM28	VDD	VDD	P29
AM29	VDD	VDD	P30
AM30	VDD	VDD	P31
AM31	VDD	VDD	P32
AM32	VDD	VDD	P33
AM33	VDD	VDD	P34
AM34	VDD	VDD	P35
AM35	VDD	VDD	P36
AM36	VDD	VDD	P37
AM37	VDD	VDD	P38
AM38	VDD	VDD	P39
AM39	VDD	VDD	P40
AM40	VDD	VDD	P41
AM41	VDD	VDD	P42
AM42	VDD	VDD	P43
AM43	VDD	VDD	T14
AP14	VDD	VDD	T15
AP15	VDD	VDD	T16
AP16	VDD	VDD	T17
AP17	VDD	VDD	T18
AP18	VDD	VDD	T19
AP19	VDD	VDD	T20
AP20	VDD	VDD	T21
AP21	VDD	VDD	T22
AP22	VDD	VDD	T23
AP23	VDD	VDD	T24
AP24	VDD	VDD	T25
AP25	VDD	VDD	T26
AP26	VDD	VDD	T27
AP27	VDD	VDD	T28
AP28	VDD	VDD	T34
AP29	VDD	VDD	Y35
AP30	VDD	VDD	Y36
AP31	VDD	VDD	Y37
AP32	VDD	VDD	Y38
AP33	VDD	VDD	Y39
AP34	VDD	VDD	Y40
AP35	VDD	VDD	Y41
AP36	VDD	VDD	Y42
AP37	VDD	VDD	Y43
AP38	VDD		
VDD_SENSE		BT48	
GND_SENSE		BR48	

G1L — BGA2714 COMMON — 19/24 FBVDDQ — FBVDDQ

AB11	FBVDDQ	FBVDDQ	L19
AB46	FBVDDQ	FBVDDQ	L20
AC11	FBVDDQ	FBVDDQ	L22
AE46	FBVDDQ	FBVDDQ	L23
AF11	FBVDDQ	FBVDDQ	L25
AF46	FBVDDQ	FBVDDQ	L26
AH11	FBVDDQ	FBVDDQ	L28
AH46	FBVDDQ	FBVDDQ	L29
AJ11	FBVDDQ	FBVDDQ	L31
AJ46	FBVDDQ	FBVDDQ	L32
AL11	FBVDDQ	FBVDDQ	L34
AL46	FBVDDQ	FBVDDQ	L37
AM11	FBVDDQ	FBVDDQ	L38
AM46	FBVDDQ	FBVDDQ	L40
AP11	FBVDDQ	FBVDDQ	L41
AR11	FBVDDQ	FBVDDQ	L43
AR46	FBVDDQ	FBVDDQ	L44
AU11	FBVDDQ	FBVDDQ	L46
AU46	FBVDDQ	FBVDDQ	N11
AV11	FBVDDQ	FBVDDQ	N46
AV46	FBVDDQ	FBVDDQ	P11
AY46	FBVDDQ	FBVDDQ	P46
BA46	FBVDDQ	FBVDDQ	T11
BC46	FBVDDQ	FBVDDQ	U11
K10	FBVDDQ	FBVDDQ	U46
L11	FBVDDQ	FBVDDQ	W11
L13	FBVDDQ	FBVDDQ	W46
L14	FBVDDQ	FBVDDQ	Y11
L16	FBVDDQ	FBVDDQ	Y46

FBVDDQ_SENSE — E54 — PS_FBVDDQ_SENSE — TP7 NO STUFF — OUT

FB_VREF — W49 — FB_VREF — R689 2.49k 0402 1% COMMON — GND

FBVDDQ

FB_CAL_PD_VDDQ — W47 — FB_CAL_PD_VDDQ — R685 /0/ res 40.2ohm 0402 1% COMMON

FB_CAL_PU_GND — Y47 — FB_CAL_PU_GND — R694 40.2ohm 0402 1% COMMON

FB_CALTERM_GND — W48 — FB_CAL_TERM_GND — R690 40.2ohm 0402 1% COMMON

GND

GPU_NVVDD_SENSE — 34 — GPU_NVVDD_FBRTN — TP503 NO STUFF — TP504 NO STUFF — OUT — OUT

1V8

Place Under GPU

C1007 1uF 6.3V 10% X6S 0402 COMMON

C1042 1uF 6.3V 10% X6S 0402 COMMON

GND

2x 0402 1uF

Place Near GPU

C1095 4.7uF 6.3V 20% X6S 0603 COMMON

C1108 4.7uF 6.3V 20% X6S 0603 COMMON

C1032 1uF 6.3V 10% X6S 0402 COMMON

C210 1uF 6.3V 10% X6S 0402 COMMON

C1130 1uF 6.3V 10% X6S 0402 COMMON

GND

2x 0603 4.7uF
3x 0402 1uF

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND

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Colorful Co.,Ltd
深圳市七彩虹科技发展有限公司

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G1M

BGA2714
COMMON

23/24 GND_4/5

BR6	GND	GND	F30
BR9	GND	GND	F33
BT2	GND	GND	F36
BT3	GND	GND	F39
C1	GND	GND	F4
C10	GND	GND	F42
C13	GND	GND	F45
C16	GND	GND	F47
C19	GND	GND	F48
C22	GND	GND	F51
C25	GND	GND	F53
C28	GND	GND	F55
C31	GND	GND	F6
C34	GND	GND	F9
C37	GND	GND	G11
C4	GND	GND	G14
C40	GND	GND	G17
C43	GND	GND	G20
C46	GND	GND	G23
C56	GND	GND	G26
C7	GND	GND	G29
D12	GND	GND	G32
D15	GND	GND	G35
D18	GND	GND	G38
D21	GND	GND	G4
D24	GND	GND	G41
D27	GND	GND	G44
D30	GND	GND	G49
D33	GND	GND	G52
D36	GND	GND	G54
D39	GND	GND	G8
D4	GND	GND	H10
D42	GND	GND	H12
D45	GND	GND	H13
D48	GND	GND	H15
D49	GND	GND	H16
D51	GND	GND	H18
D53	GND	GND	H19
D6	GND	GND	H21
D9	GND	GND	H22
E10	GND	GND	H24
E13	GND	GND	H25
E16	GND	GND	H27
E19	GND	GND	H28
E2	GND	GND	H3
E22	GND	GND	H30
E25	GND	GND	H32
E28	GND	GND	H33
E31	GND	GND	H34
E34	GND	GND	H36
E37	GND	GND	H37
E40	GND	GND	H39
E43	GND	GND	H4
E5	GND	GND	H40
E52	GND	GND	H42
E7	GND	GND	H43
F1	GND	GND	H45
F12	GND	GND	H46
F15	GND	GND	H47
F18	GND	GND	H48
F2	GND	GND	H50
F21	GND	GND	H55
F24	GND	GND	H6
F27	GND		

GND GND

G1N

BGA2714
COMMON

24/24 GND_5/5

H7	GND	GND	R41
H9	GND	GND	R42
J10	GND	GND	R43
J17	GND	GND	R44
J20	GND	GND	R47
J29	GND	GND	R49
J35	GND	GND	R51
J4	GND	GND	R53
J49	GND	GND	R55
J51	GND	GND	R6
J53	GND	GND	R8
J55	GND	GND	T2
J5	GND	GND	T49
J8	GND	GND	T52
K12	GND	GND	T54
K15	GND	GND	T7
K18	GND	GND	T9
K19	GND	GND	U10
K21	GND	GND	U13
K24	GND	GND	U14
K27	GND	GND	U15
K28	GND	GND	U16
K30	GND	GND	U17
K33	GND	GND	U18
K36	GND	GND	U19
K37	GND	GND	U20
K39	GND	GND	U21
K42	GND	GND	U22
K45	GND	GND	U23
K49	GND	GND	U24
K52	GND	GND	U25
K54	GND	GND	U26
K7	GND	GND	U27
K9	GND	GND	U28
L10	GND	GND	U29
L3	GND	GND	U3
L5	GND	GND	U30
L50	GND	GND	U31
L55	GND	GND	U32
L8	GND	GND	U33
M10	GND	GND	U34
M2	GND	GND	U35
M4	GND	GND	U36
M47	GND	GND	U37
M49	GND	GND	U38
M51	GND	GND	U39
M53	GND	GND	U40
M55	GND	GND	U41
M6	GND	GND	U42
M8	GND	GND	U43
N14	GND	GND	U44
N16	GND	GND	U48
N18	GND	GND	U5
N2	GND	GND	U50
N20	GND	GND	U55
N22	GND	GND	U8
N24	GND	GND	V10
N26	GND	GND	V2
N28	GND	GND	V4
N29	GND	GND	V47
N31	GND	GND	V49
N33	GND	GND	V51
N35	GND	GND	V53
N37	GND	GND	V55
N39	GND	GND	V6
N41	GND	GND	V8
N43	GND	GND	W13
N48	GND	GND	W14
N52	GND	GND	W15
N54	GND	GND	W16
N7	GND	GND	W17
P3	GND	GND	W18
P5	GND	GND	W19
P50	GND	GND	W20
P55	GND	GND	W21
P6	GND	GND	W22
R10	GND	GND	W23
R13	GND	GND	W24
R14	GND	GND	W25
R15	GND	GND	W26
R16	GND	GND	W27
R17	GND	GND	W28
R18	GND	GND	W29
R19	GND	GND	W30
R2	GND	GND	W31
R20	GND	GND	W32
R21	GND	GND	W33
R22	GND	GND	W34
R23	GND	GND	W35
R24	GND	GND	W36
R25	GND	GND	W37
R26	GND	GND	W38
R27	GND	GND	W39
R28	GND	GND	W40
R29	GND	GND	W41
R30	GND	GND	W42
R31	GND	GND	W43
R32	GND	GND	W44
R33	GND	GND	W52
R34	GND	GND	W54
R35	GND	GND	W7
R36	GND	GND	Y3
R37	GND	GND	Y48
R38	GND	GND	Y5
R39	GND	GND	Y50
R4	GND	GND	Y55
R40	GND	GND	Y8

GND GND

G1O

BGA2714
COMMON

22/24 VDDMS

NVVDD NVVDD

AY27	VDDMS	VDDMS	AB13
AY28	VDDMS	VDDMS	AB44
AY29	VDDMS	VDDMS	AD13
AY30	VDDMS	VDDMS	AD44
AY31	VDDMS	VDDMS	AF13
AY32	VDDMS	VDDMS	AF44
AY33	VDDMS	VDDMS	AH13
AY34	VDDMS	VDDMS	AH44
AY35	VDDMS	VDDMS	AK13
AY36	VDDMS	VDDMS	AK44
AY37	VDDMS	VDDMS	AM13
AY38	VDDMS	VDDMS	AM44
AY39	VDDMS	VDDMS	AP13
AY40	VDDMS	VDDMS	AP44
AY41	VDDMS	VDDMS	AT13
AY42	VDDMS	VDDMS	AT14
AY43	VDDMS	VDDMS	AT15
AY44	VDDMS	VDDMS	AT16
BA13	VDDMS	VDDMS	AT17
BA44	VDDMS	VDDMS	AT18
BB13	VDDMS	VDDMS	AT19
BB14	VDDMS	VDDMS	AT20
BB15	VDDMS	VDDMS	AT21
BB16	VDDMS	VDDMS	AT22
BB17	VDDMS	VDDMS	AT23
BB18	VDDMS	VDDMS	AT24
BB19	VDDMS	VDDMS	AT25
BB20	VDDMS	VDDMS	AT26
BB21	VDDMS	VDDMS	AT27
BB22	VDDMS	VDDMS	AT28
BB23	VDDMS	VDDMS	AT29
BB24	VDDMS	VDDMS	AT30
BB25	VDDMS	VDDMS	AT31
BB26	VDDMS	VDDMS	AT32
BB27	VDDMS	VDDMS	AT33
BB28	VDDMS	VDDMS	AT34
BB29	VDDMS	VDDMS	AT35
BB30	VDDMS	VDDMS	AT36
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BB34	VDDMS	VDDMS	AT40
BB35	VDDMS	VDDMS	AT41
BB36	VDDMS	VDDMS	AT42
BB37	VDDMS	VDDMS	AT43
BB38	VDDMS	VDDMS	AT44
BB39	VDDMS	VDDMS	AU13
BB40	VDDMS	VDDMS	AU44
BB41	VDDMS	VDDMS	AV13
BB42	VDDMS	VDDMS	AV14
BB43	VDDMS	VDDMS	AV15
BB44	VDDMS	VDDMS	AV16
BC13	VDDMS	VDDMS	AV17
BC44	VDDMS	VDDMS	AV18
BD13	VDDMS	VDDMS	AV19
BD14	VDDMS	VDDMS	AV20
BD17	VDDMS	VDDMS	AV21
BD18	VDDMS	VDDMS	AV22
BD21	VDDMS	VDDMS	AV23
BD22	VDDMS	VDDMS	AV24
BD25	VDDMS	VDDMS	AV25
BD26	VDDMS	VDDMS	AV26
BD29	VDDMS	VDDMS	AV27
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BD31	VDDMS	VDDMS	AV29
BD32	VDDMS	VDDMS	AV30
BD35	VDDMS	VDDMS	AV31
BD36	VDDMS	VDDMS	AV32
BD39	VDDMS	VDDMS	AV33
BD40	VDDMS	VDDMS	AV34
BD43	VDDMS	VDDMS	AV35
BD44	VDDMS	VDDMS	AV36
N13	VDDMS	VDDMS	AV37
N15	VDDMS	VDDMS	AV38
N17	VDDMS	VDDMS	AV39
N19	VDDMS	VDDMS	AV40
N21	VDDMS	VDDMS	AV41
N23	VDDMS	VDDMS	AV42
N25	VDDMS	VDDMS	AV43
N27	VDDMS	VDDMS	AV44
N30	VDDMS	VDDMS	AW13
N32	VDDMS	VDDMS	AW44
N34	VDDMS	VDDMS	AY13
N36	VDDMS	VDDMS	AY14
N38	VDDMS	VDDMS	AY15
N40	VDDMS	VDDMS	AY16
N42	VDDMS	VDDMS	AY17
N44	VDDMS	VDDMS	AY18
P13	VDDMS	VDDMS	AY19
P44	VDDMS	VDDMS	AY20
T13	VDDMS	VDDMS	AY21
T44	VDDMS	VDDMS	AY22
V13	VDDMS	VDDMS	AY23
V44	VDDMS	VDDMS	AY24
Y13	VDDMS	VDDMS	AY25
Y44	VDDMS	VDDMS	AY26

VDDMS_SENSE	BP49	34
GNDMS_SENSE	BR49	34

TP501 NO STUFF
GPU_MSVDD_SENSE
GPU_MSVDD_FBRTN
OUT
OUT
TP502 NO STUFF

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND 2

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Page17: XVDD

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND 3 (XVDD)

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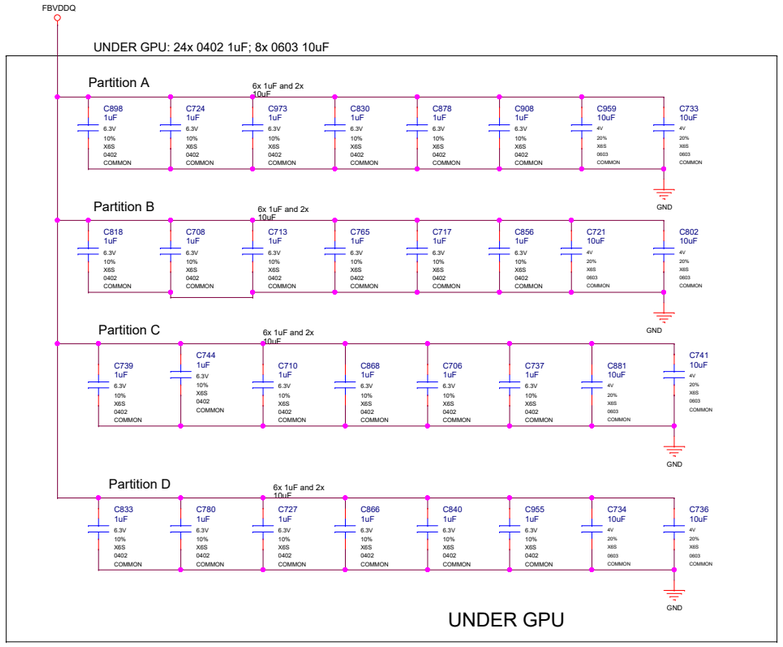
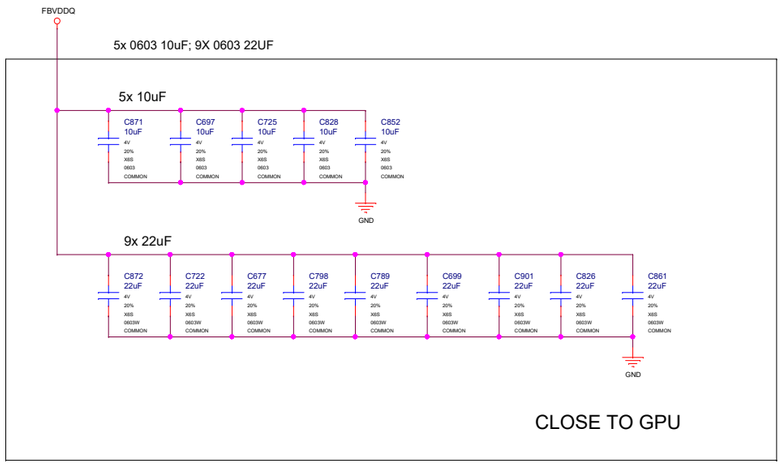
Page18: GPU DECOUPLING FBVDDQ

FBVDDQ





ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING FBVDDQ

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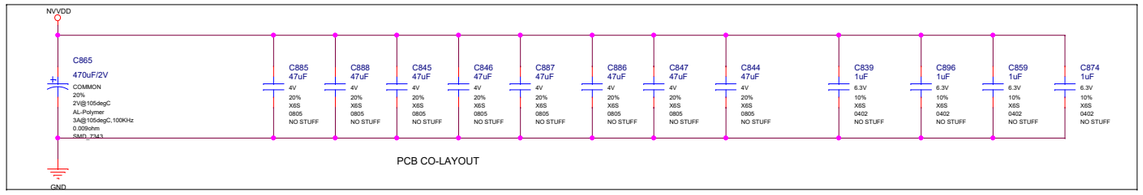
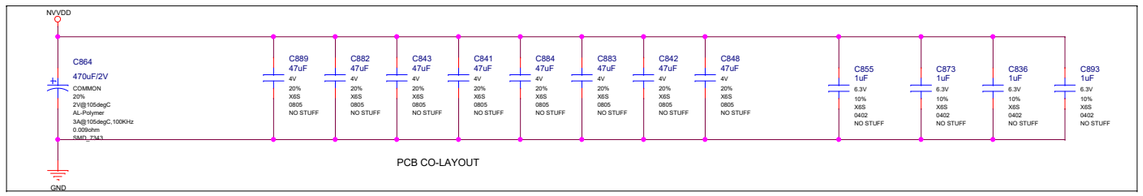
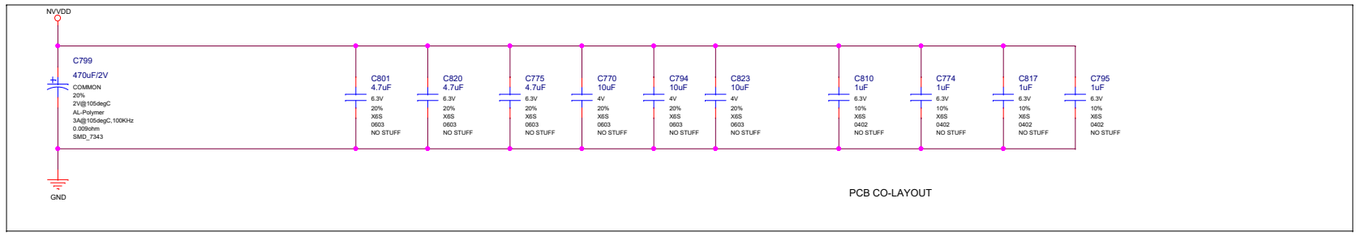
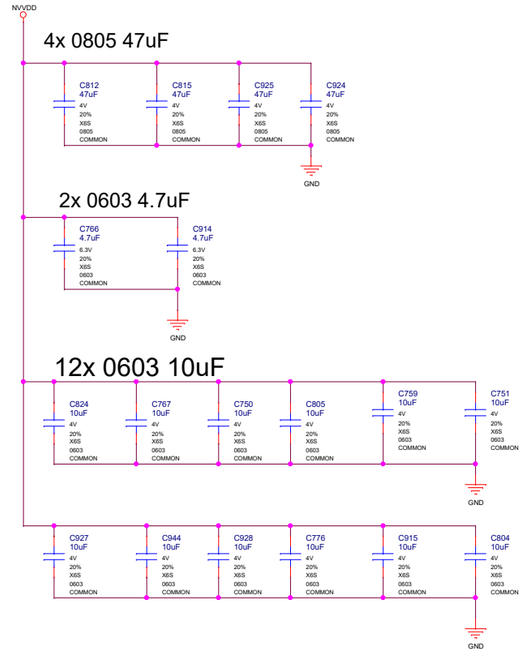
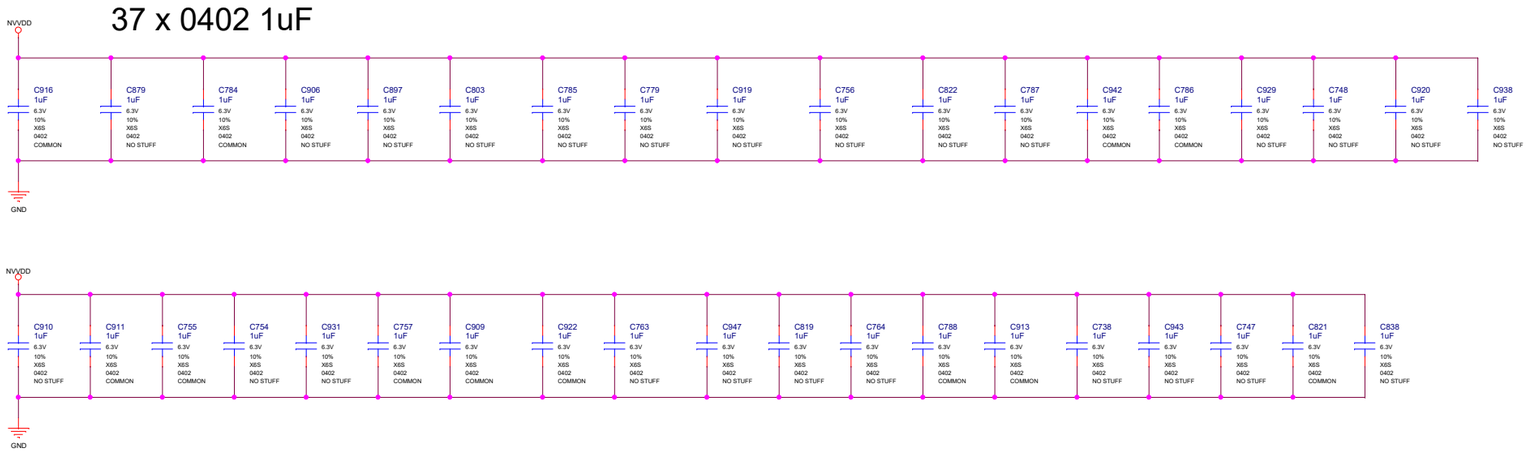
Page19: GPU DECOUPLING NVVDD











UNDER GPU

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING NVVDD

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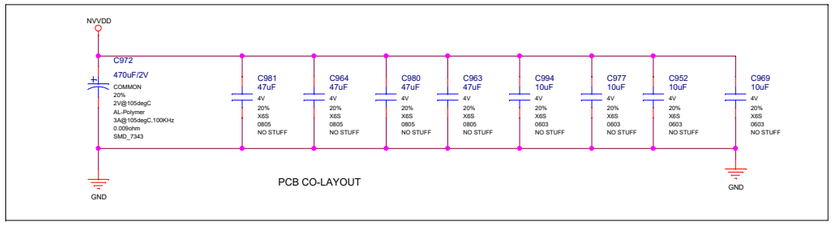
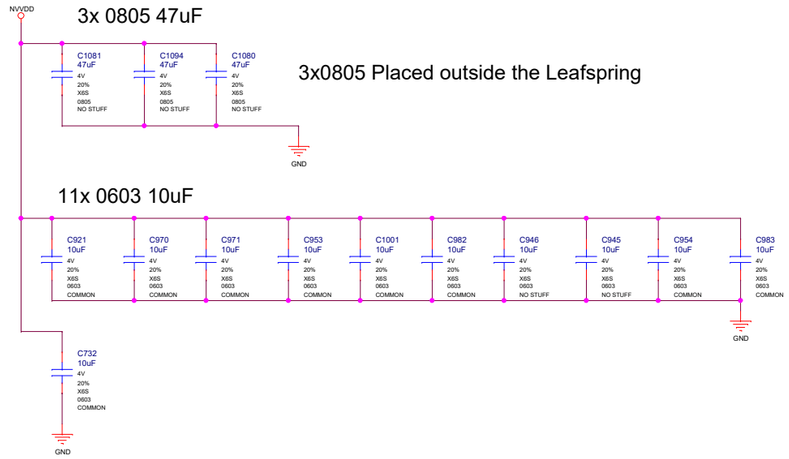
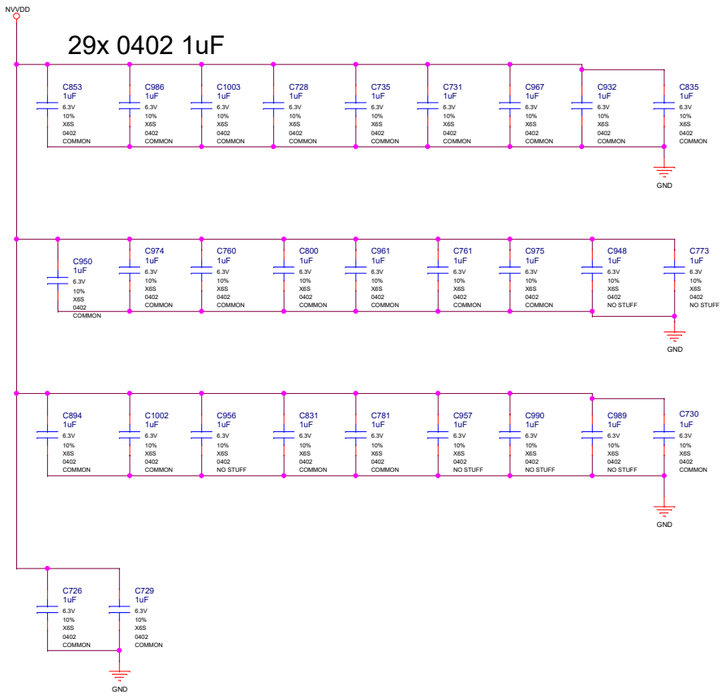
Page20: GPU DECOUPLING NVVDD







UNDER GPU

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING NVVDD

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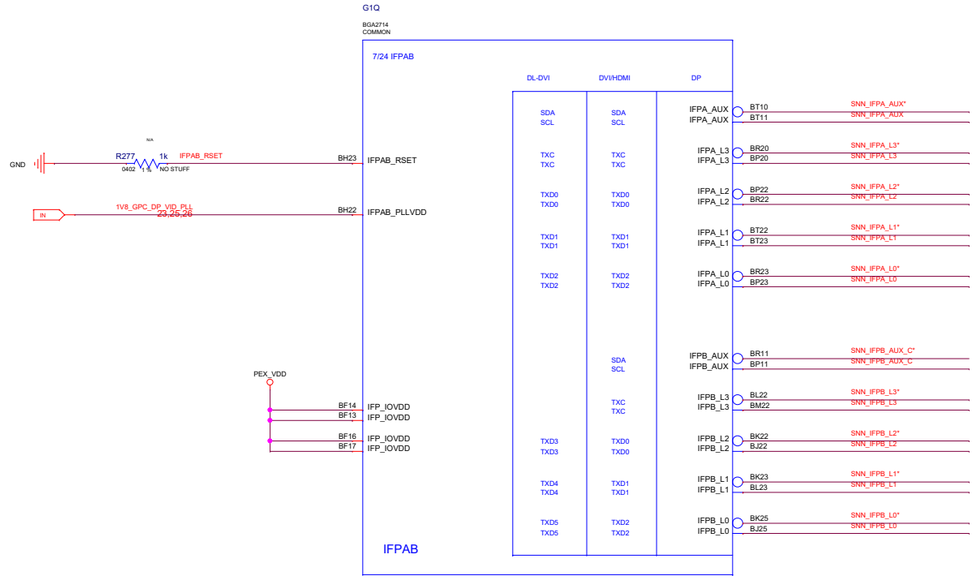
Page21: IFPAB DVI-D-DL



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPAB NC

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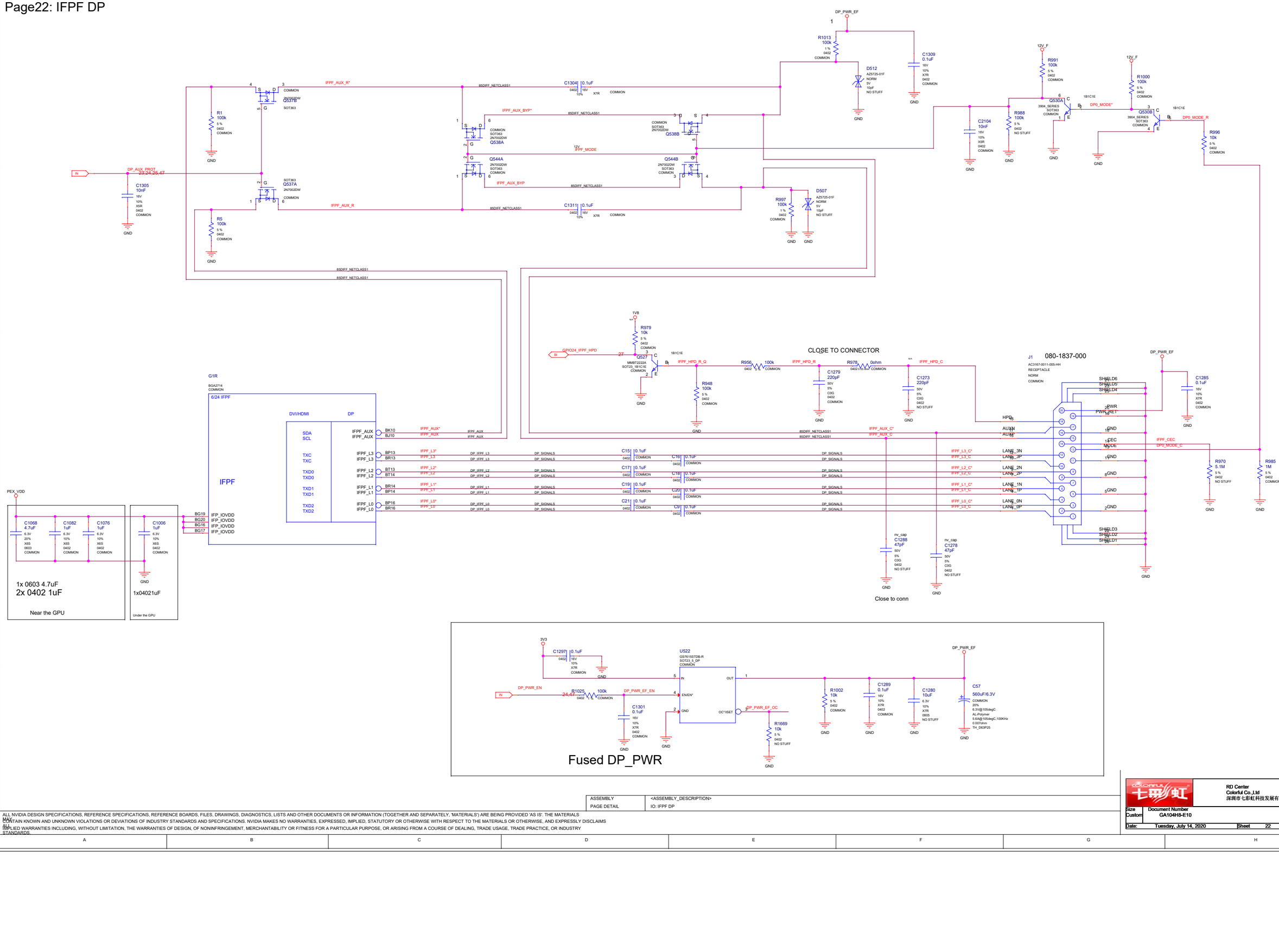
Page22: IFPF DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPF DP

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Page23: IFPE DP

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPE DP

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Page24: IFPD DP

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

1x 0402 1uF

(was 1x 0201W 0.47uF)

Close to conn

Close to conn

Hotplug Detection

Fused DP_PWR

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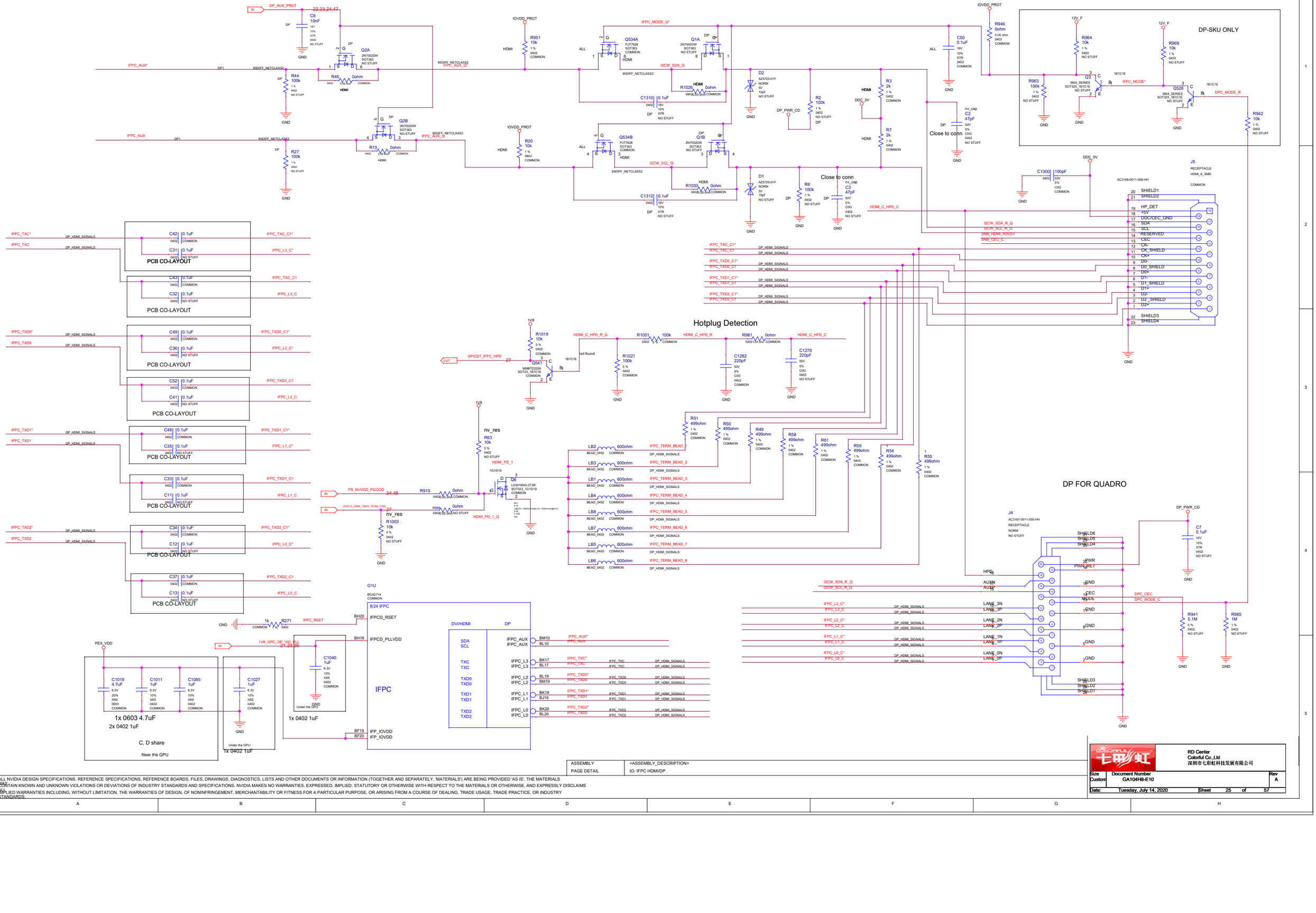
27-JUN-2020

Page25: IFPC HDMI/DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPC HDMI/DP

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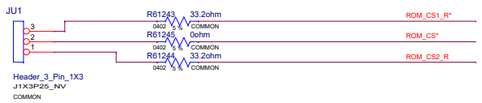
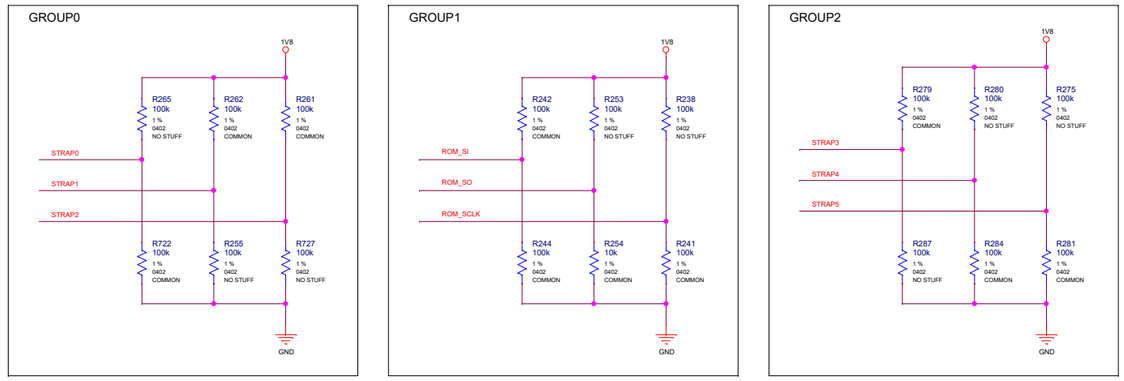
Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
		TBD		

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

JU1按下高频 Pin(1,2) 相连 BIOS2(U16)
JU1弹起 低频Pin(2,3) 相连 BIOS1(U10828)





ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
H	H	M	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

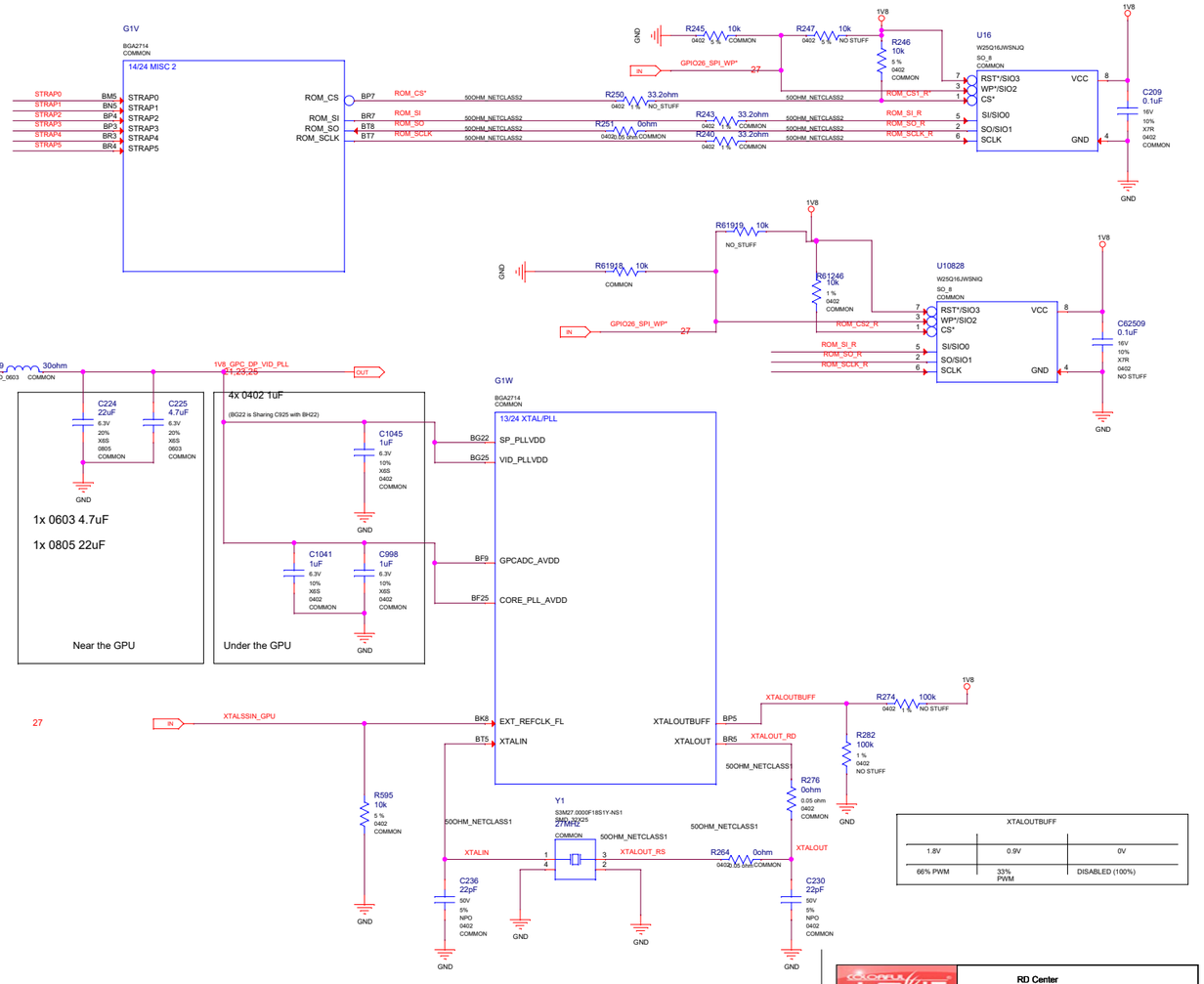
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

DEFAULT



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: ROM, XTAL,STRAPS

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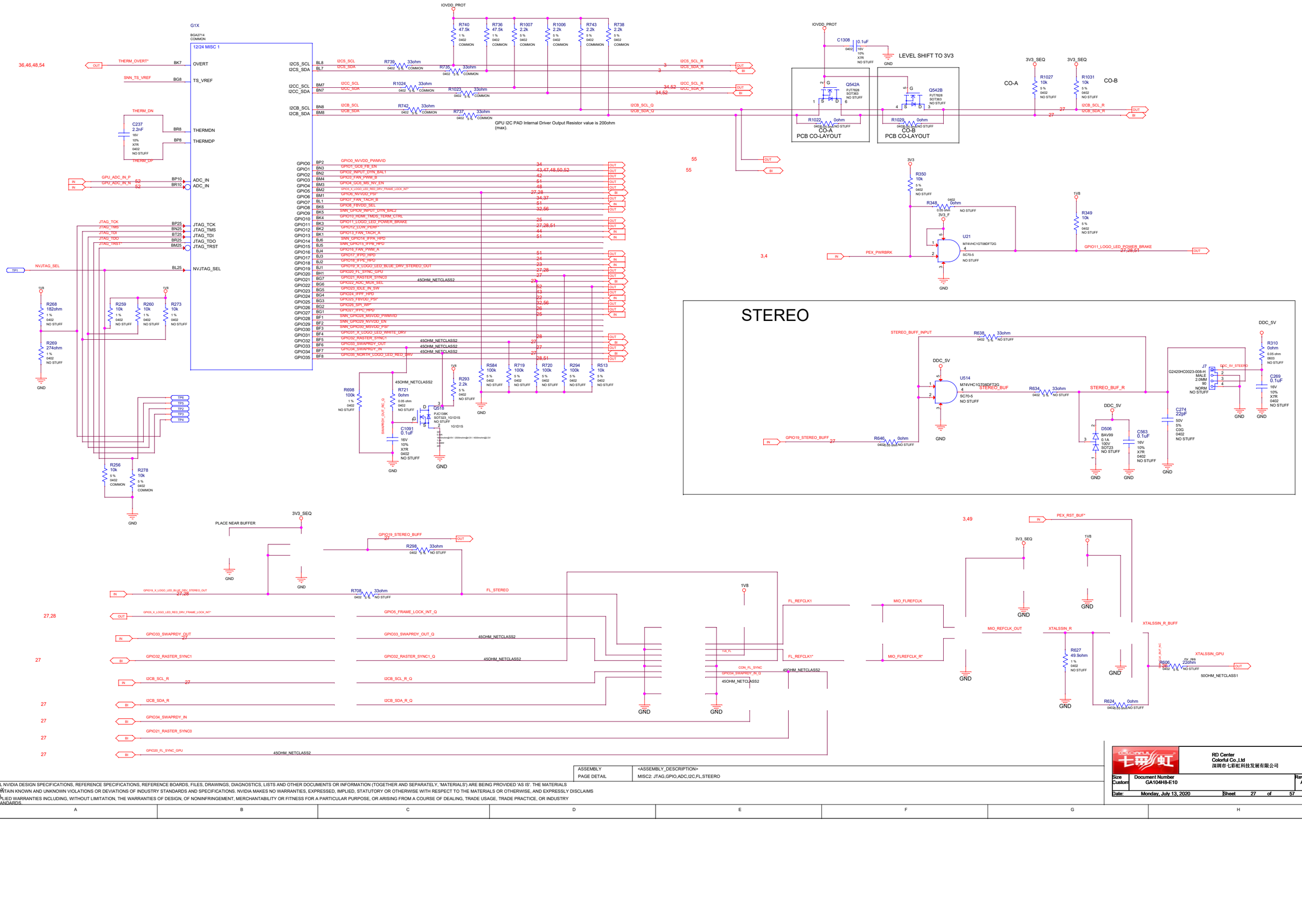
Page27: MISC1: JTAG, GPIO, ADC, I2C, OVERT



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PAGE DETAIL	MISC2: JTAG,GPIO,ADC,I2C,FL,STEERO

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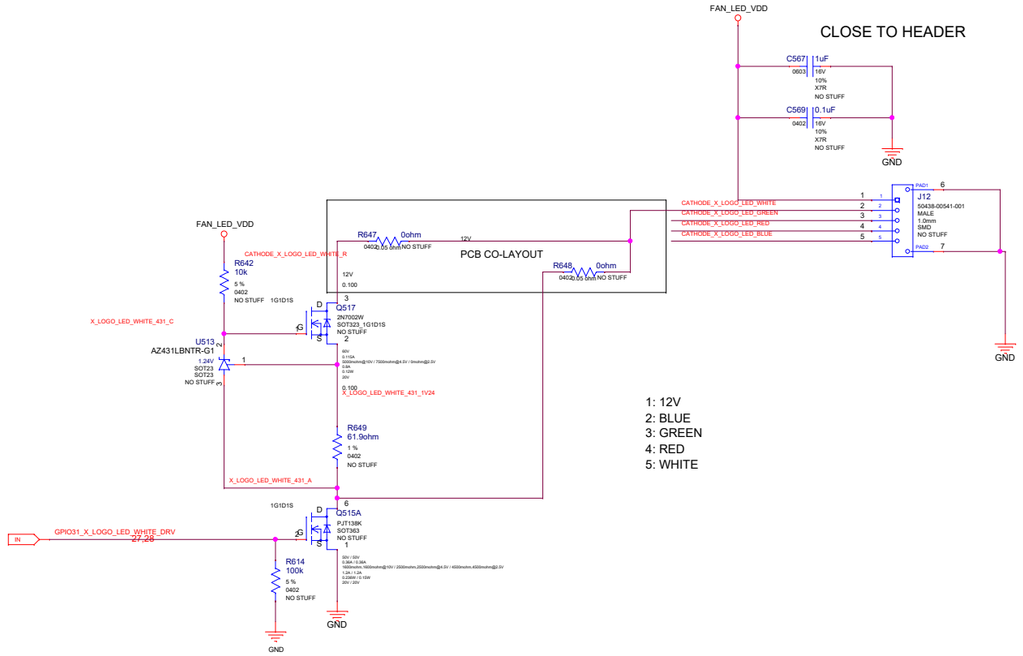
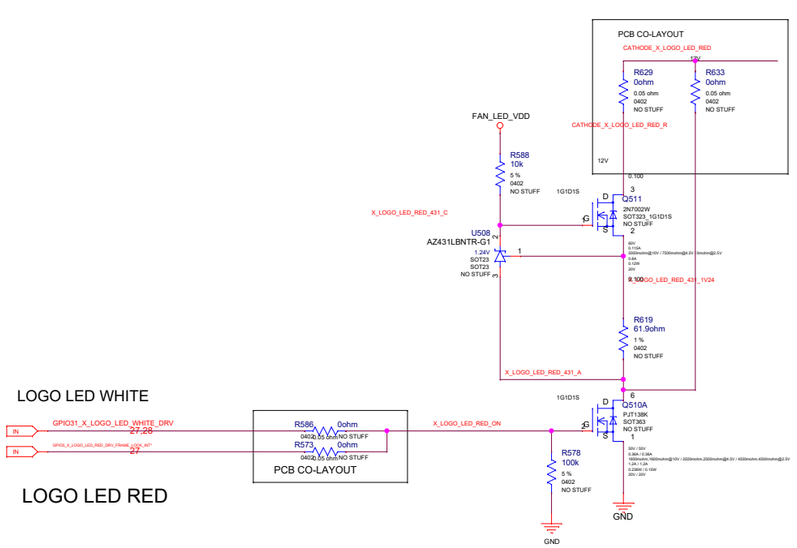
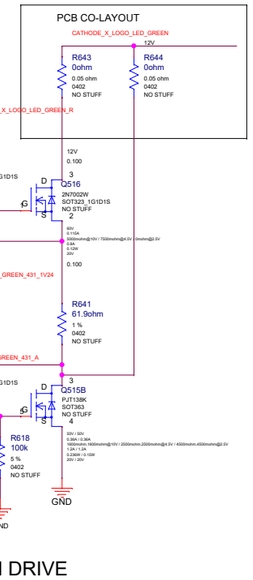
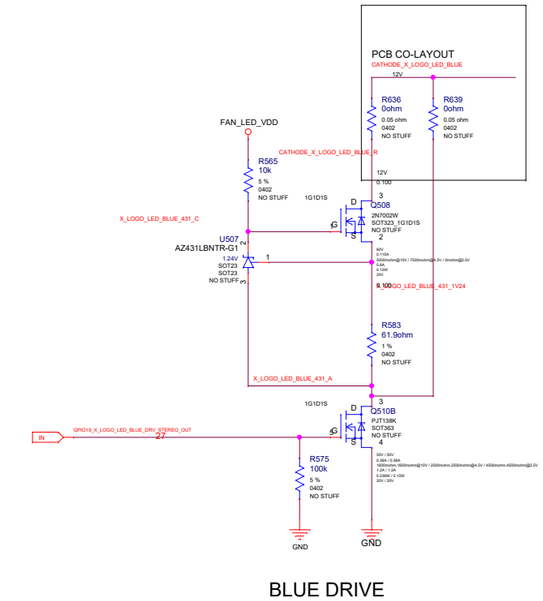
Page28: RGB









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PAGE DETAIL	MISC3: RGB

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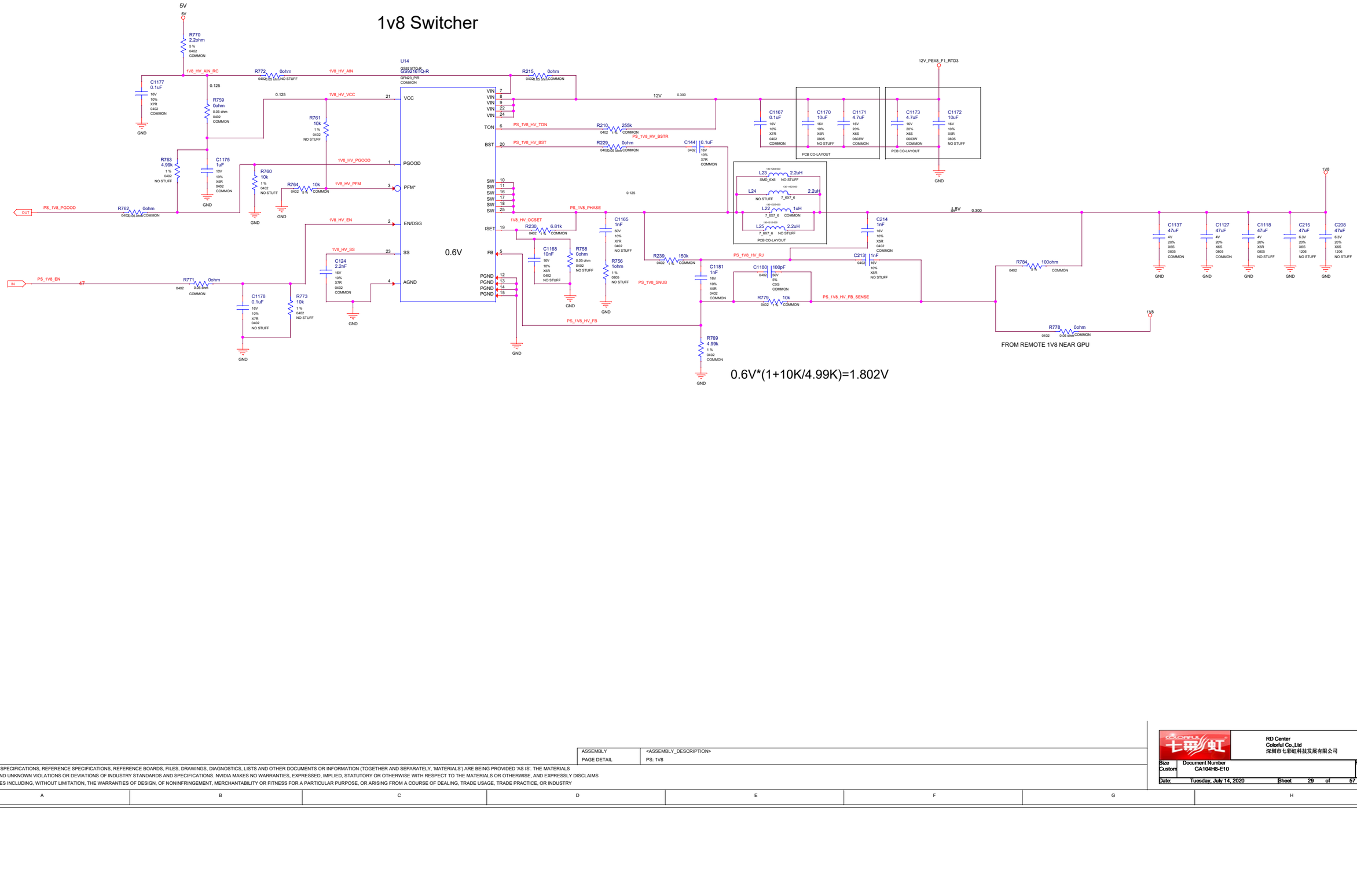
Page29: PS: 1V8

1v8 Switcher



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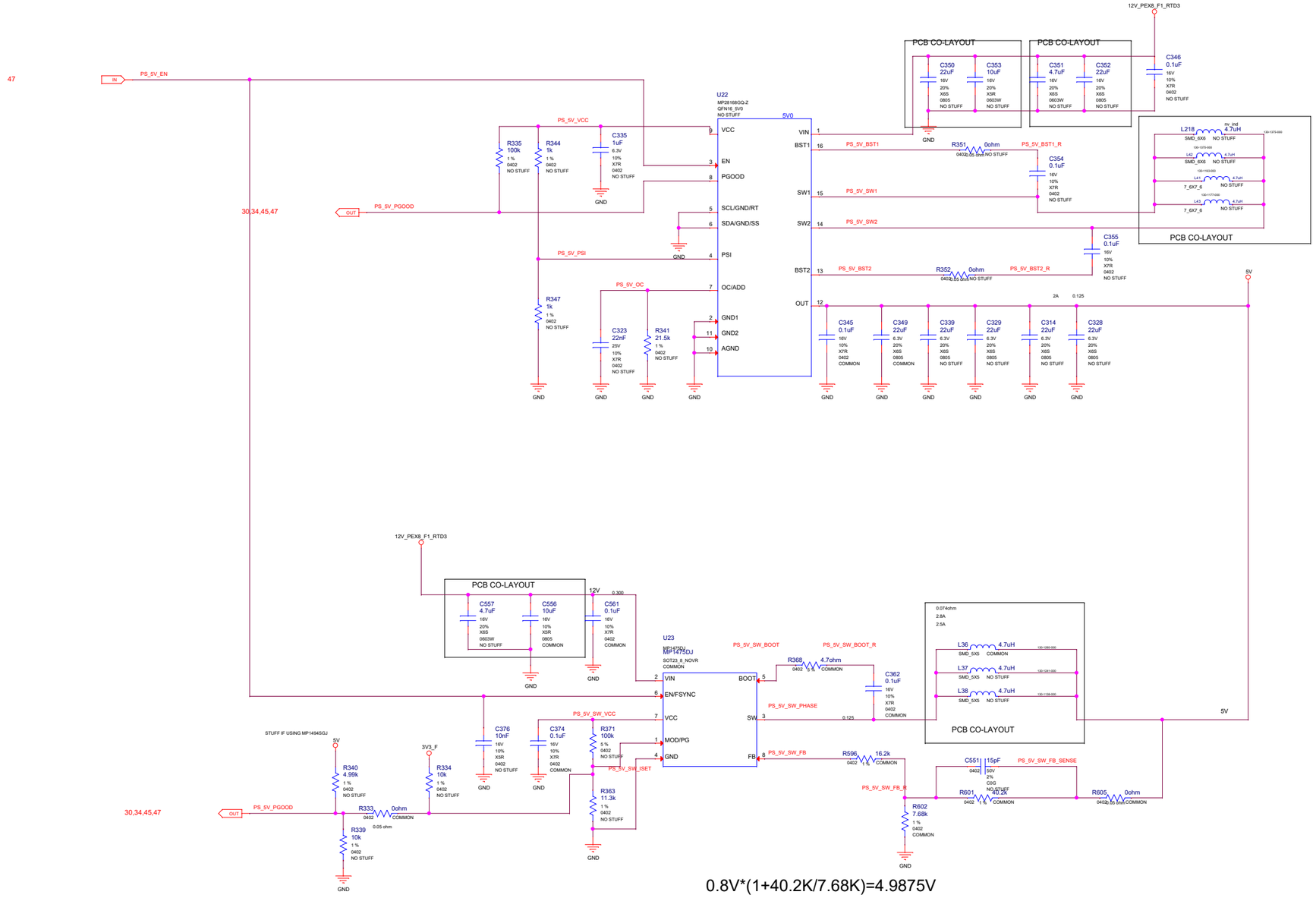
Page30: PS: 5V



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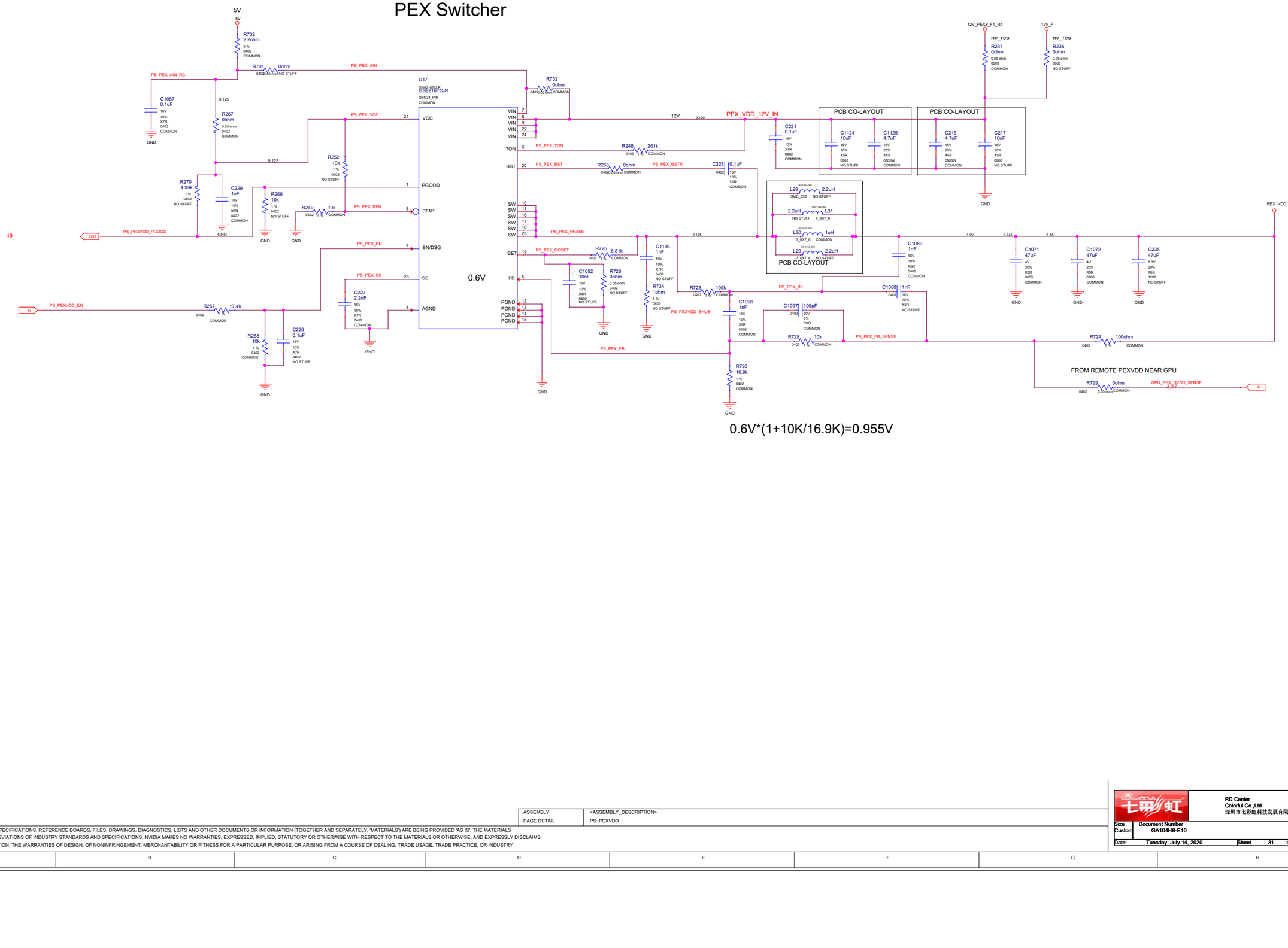
Page31: PS: PEXVDD

PEX Switcher



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PAGE DETAIL	PS: PEXVDD

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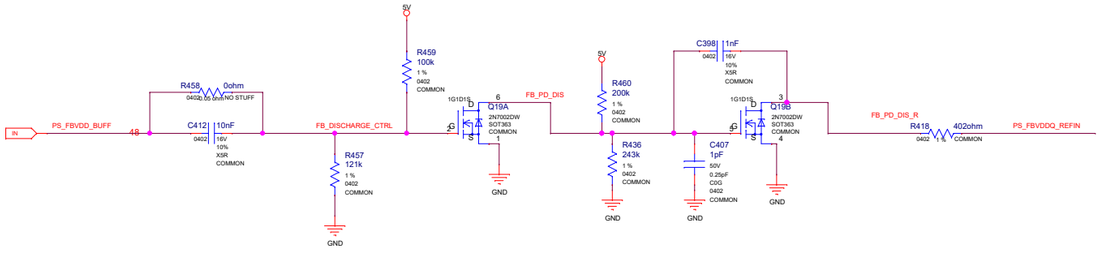
Page32: PS: FBVDDQ



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Page33: PS: FBVDDQ PH2

FBVDD PH2 INPUT ANTI-BACKDRIVE

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDDQ PH2

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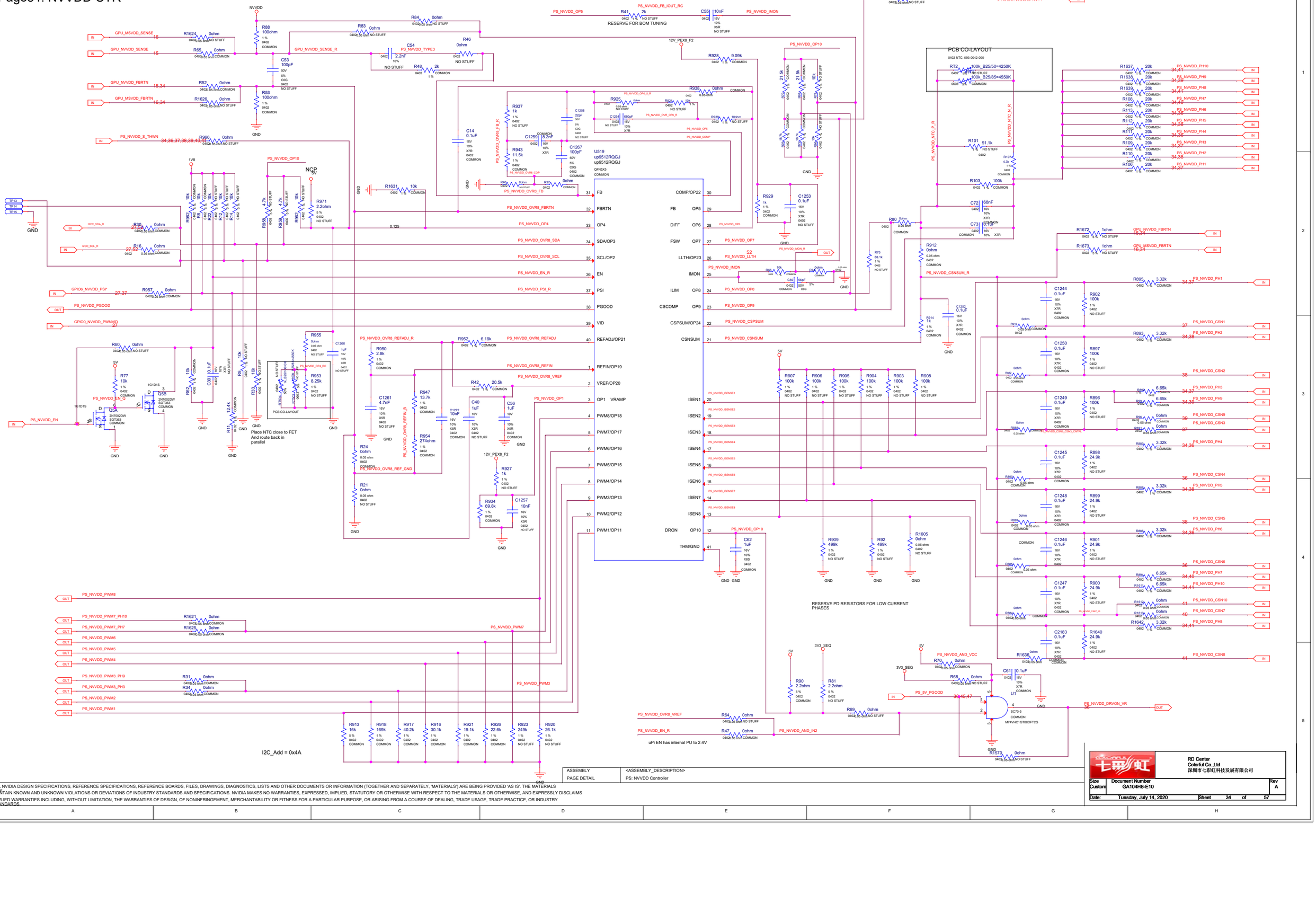
Page34: NVVDD CTR



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Controller

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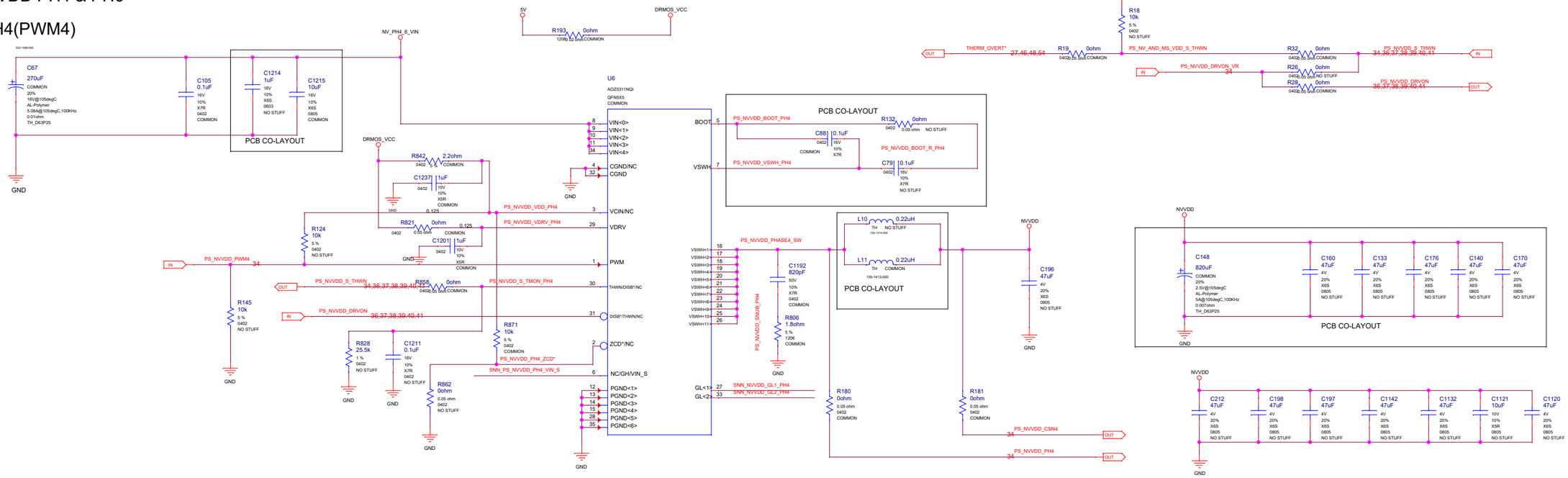
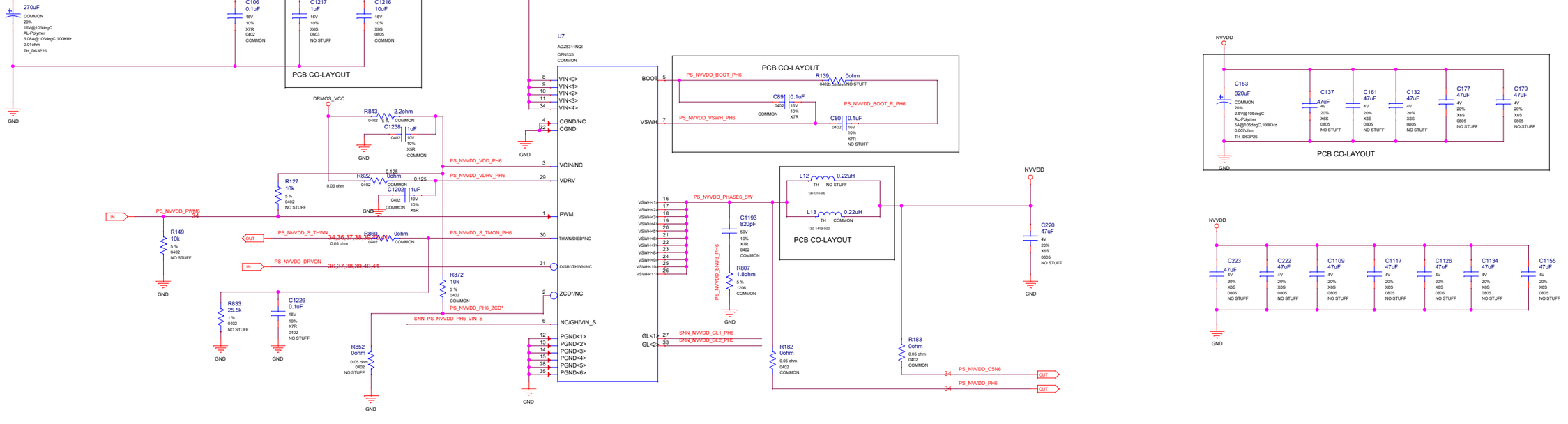
Page36: NVVDD PH4 & PH6

NVVDD PH4(PWM4)



NVVDD PH6(PWM6)



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PAGE DETAIL	PS: NVVDD PH4, PH6

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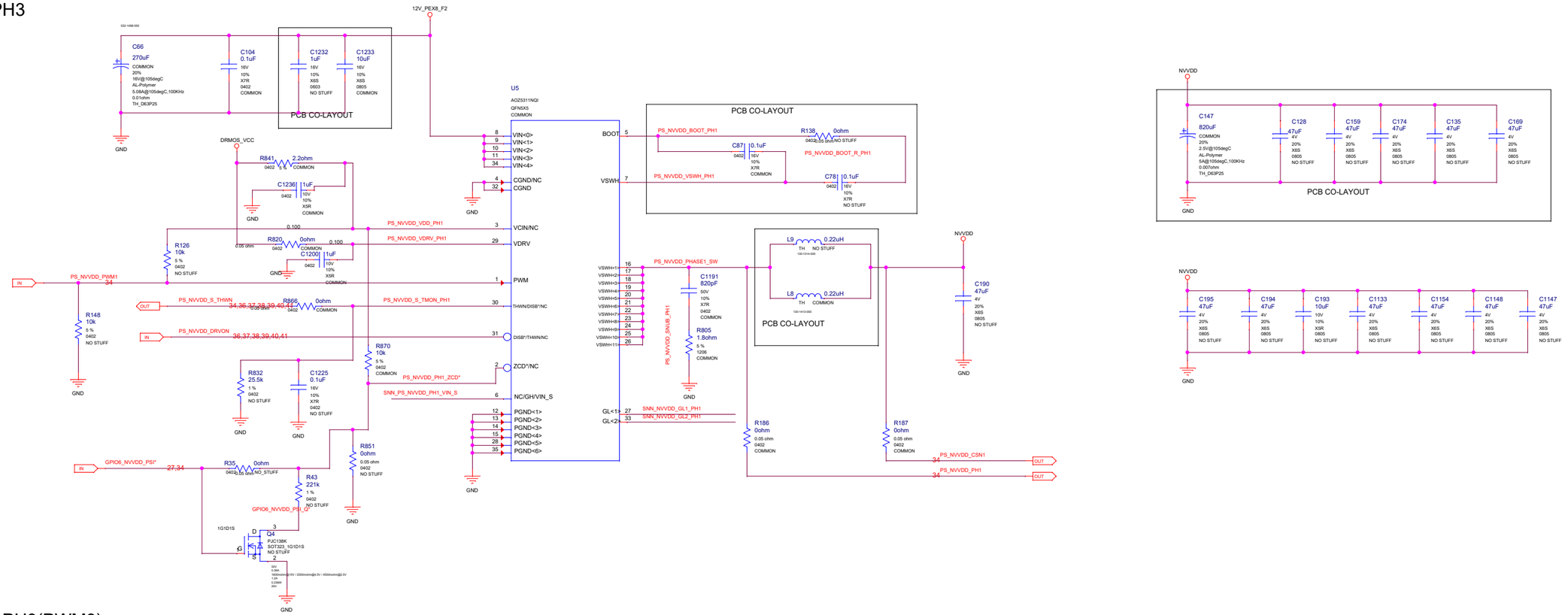
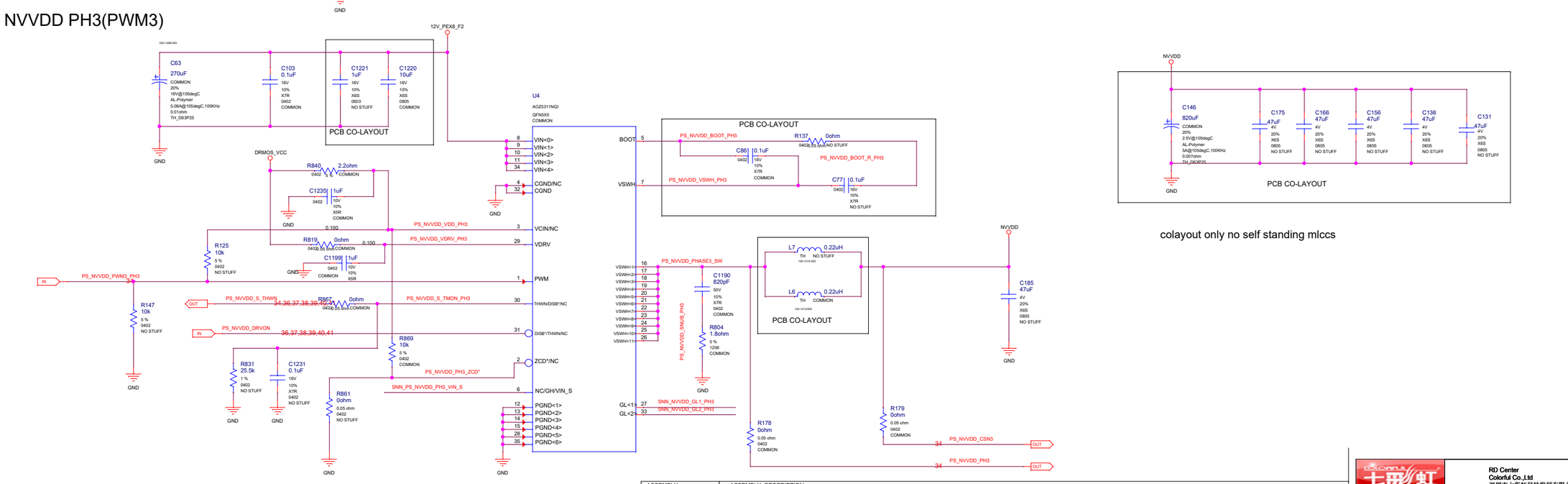
Page37: NVVDD PH1 & PH3

NVVDD PH1(PWM1)



NVVDD PH3(PWM3)



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD PH1, PH3

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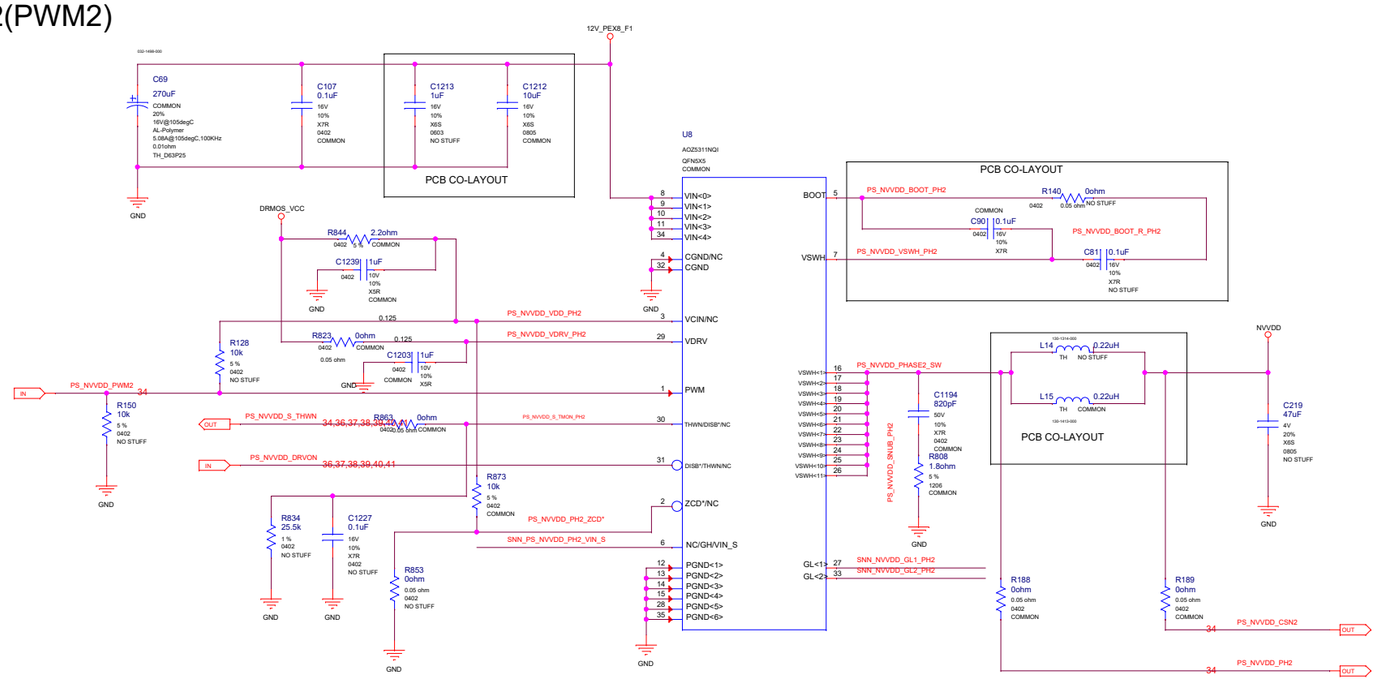
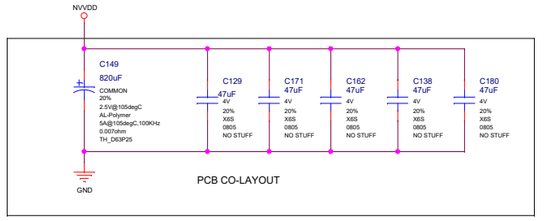
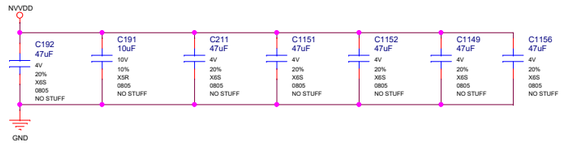
Page38: NVVDD PH2 & PH5

NVVDD PH2(PWM2)







NVVDD PH5(PWM5)

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PAGE DETAIL	PS: NVVDD PH2, PH5

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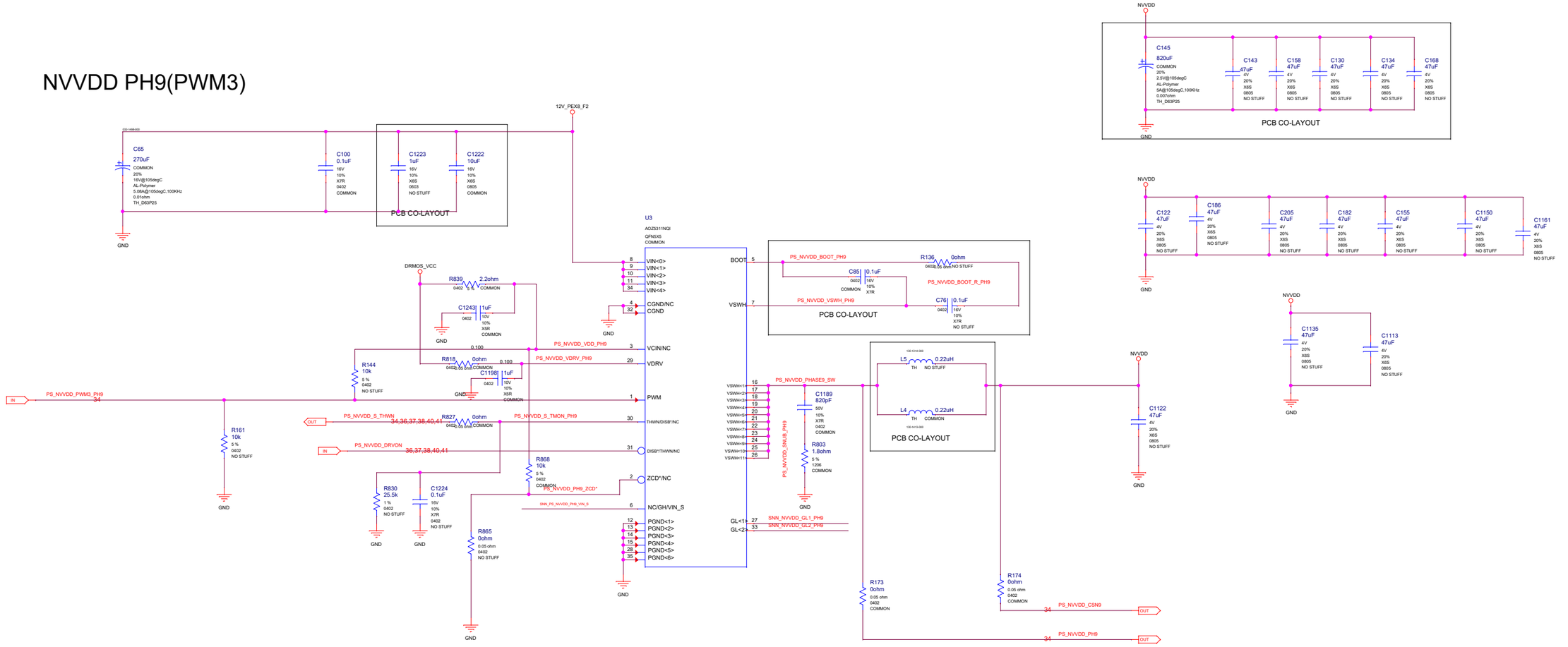
Page39: NVVDD PH9

NVVDD PH9(PWM3)



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PAGE DETAIL	PS: NVDD PH9

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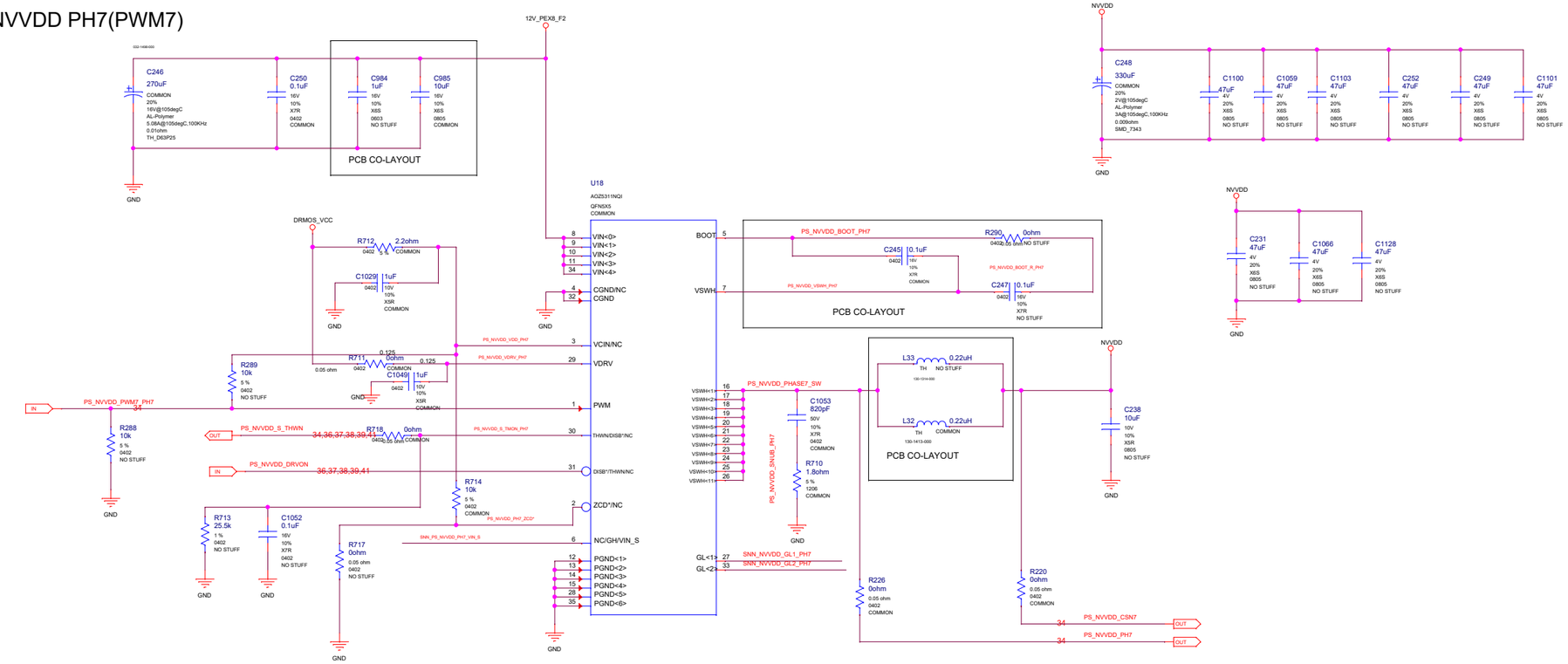
Page40: NVVDD PH7

NVVDD PH7(PWM7)



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD PH7

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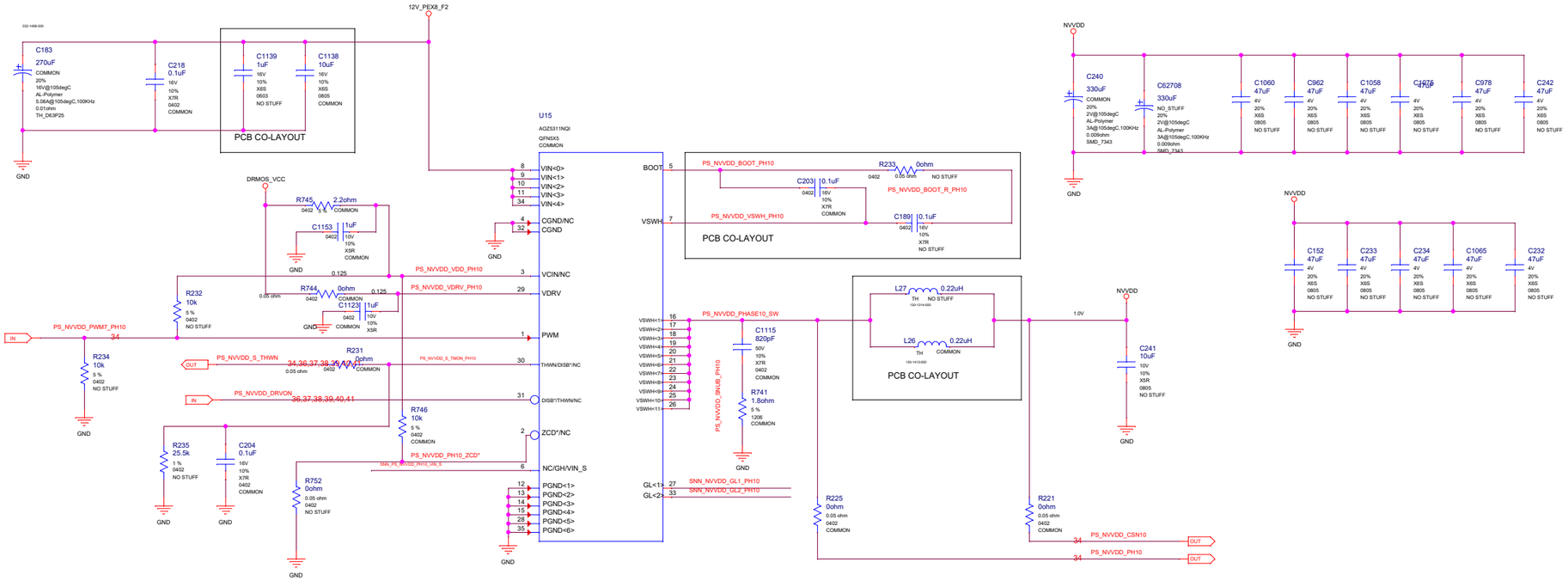
Page41: NVVDD PH10 & 8

NVVDD PH10(PWM7)



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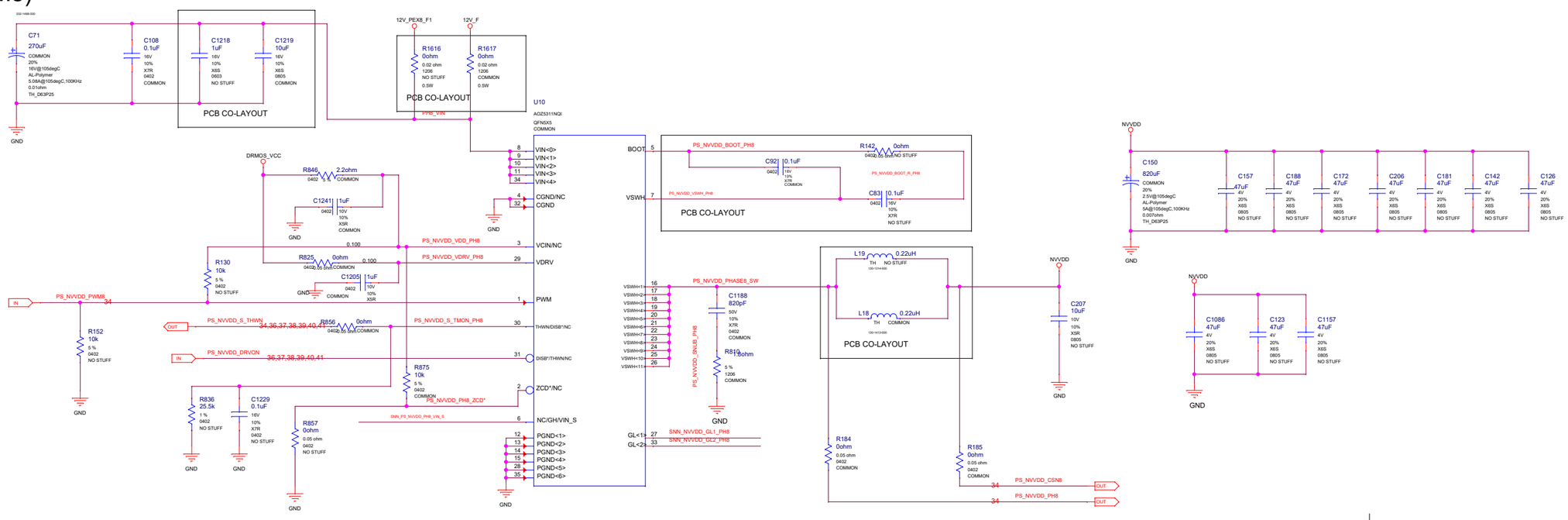

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PAGE DETAIL	PS: NVDD PH10, PH8

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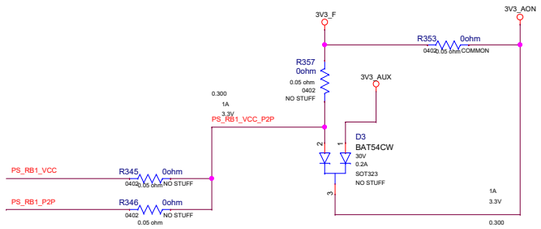
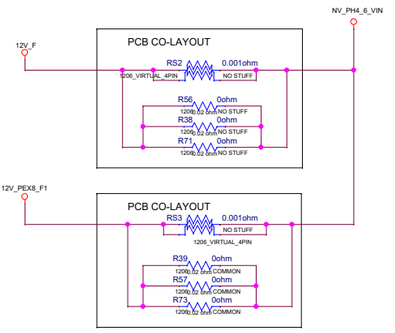
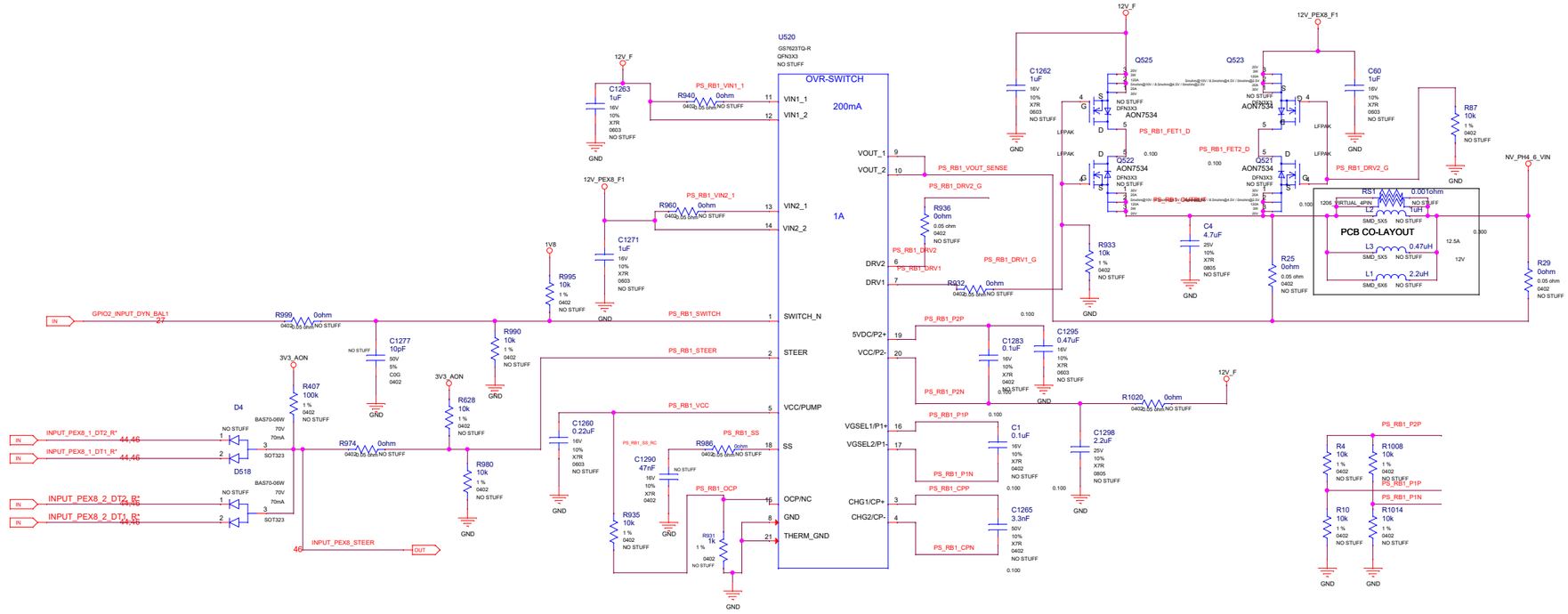
Page42: Input Power Balancing Switcher







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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: OVRS_INPUT POWER BALANCE

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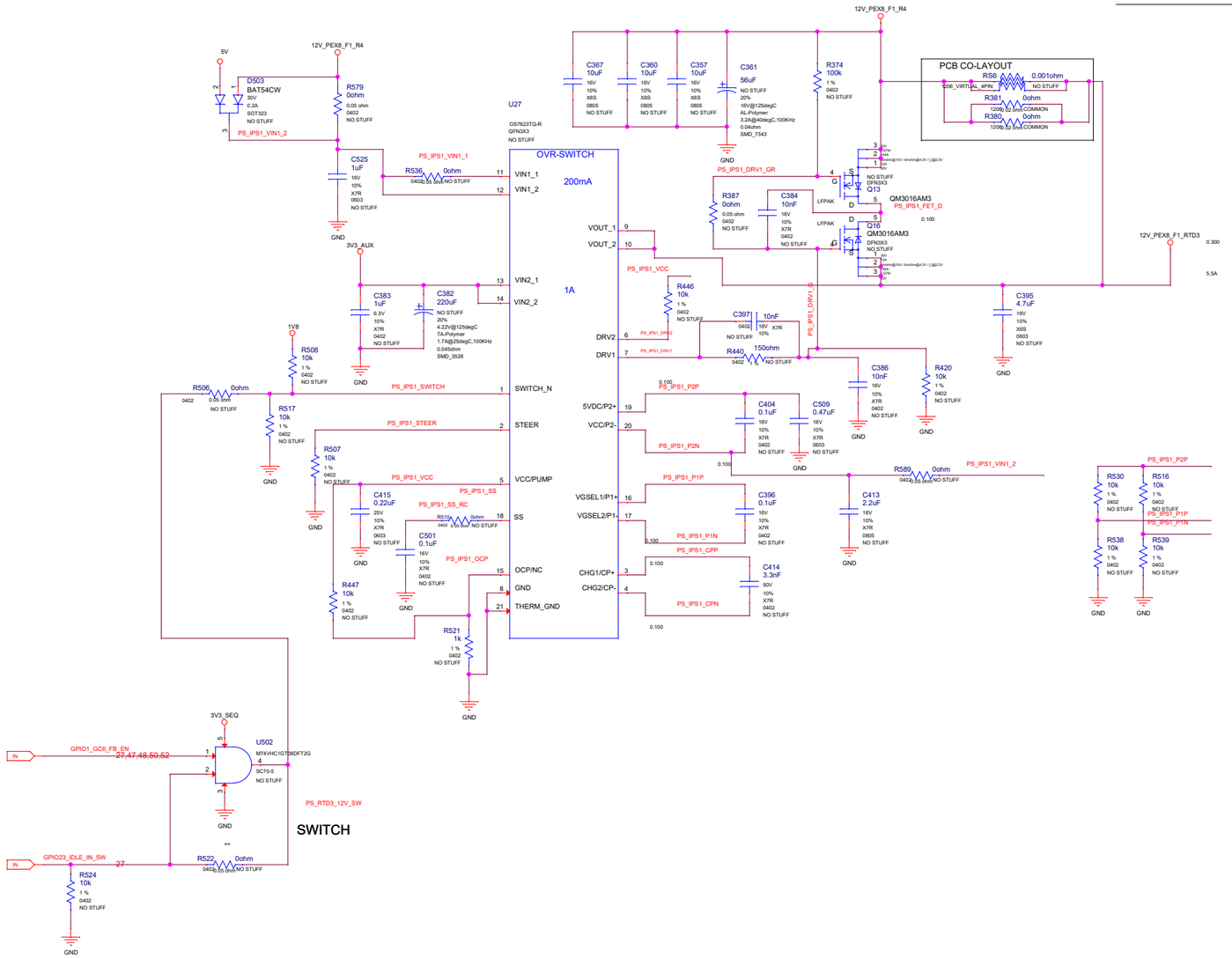
Page43: INPUT SWITCH RTD3 (12V & 3V3_A SWITCHER)

AND GATE LOGIC

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V
0	1	0	12V
1	0	0	12V
1	1	1	3V3A

SWITCH	VOUT
0	VOUT = VIN1
1	VOUT = VIN2



ASSEMBLY <ASSEMBLY_DESCRIPTION>

PAGE DETAIL PS: RDT3_12V & 3V3_A Switcher

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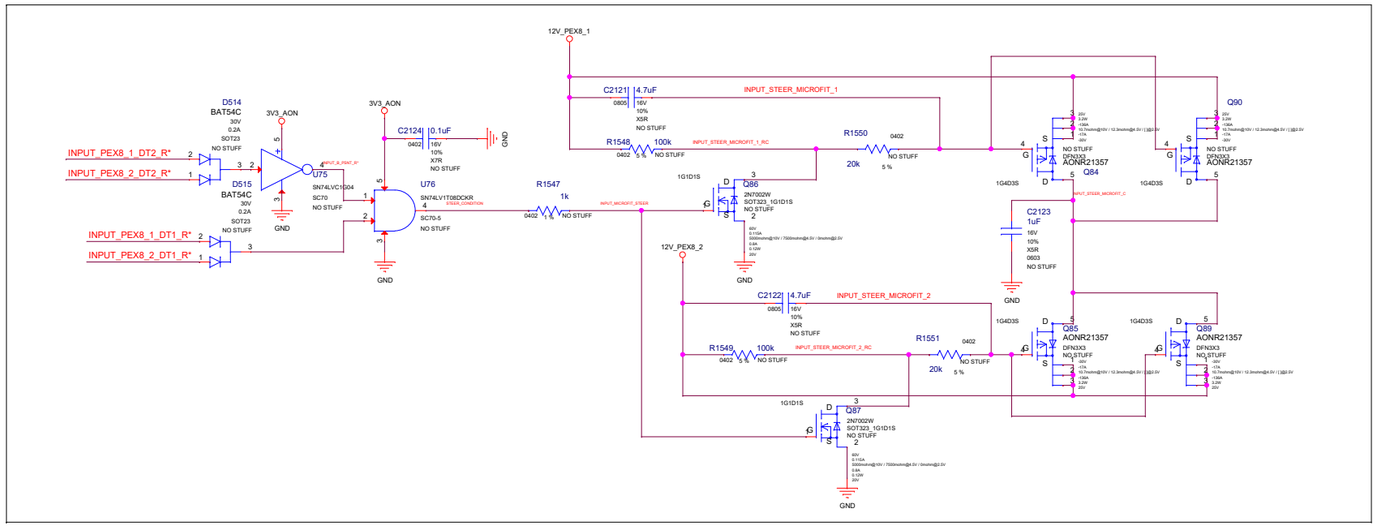
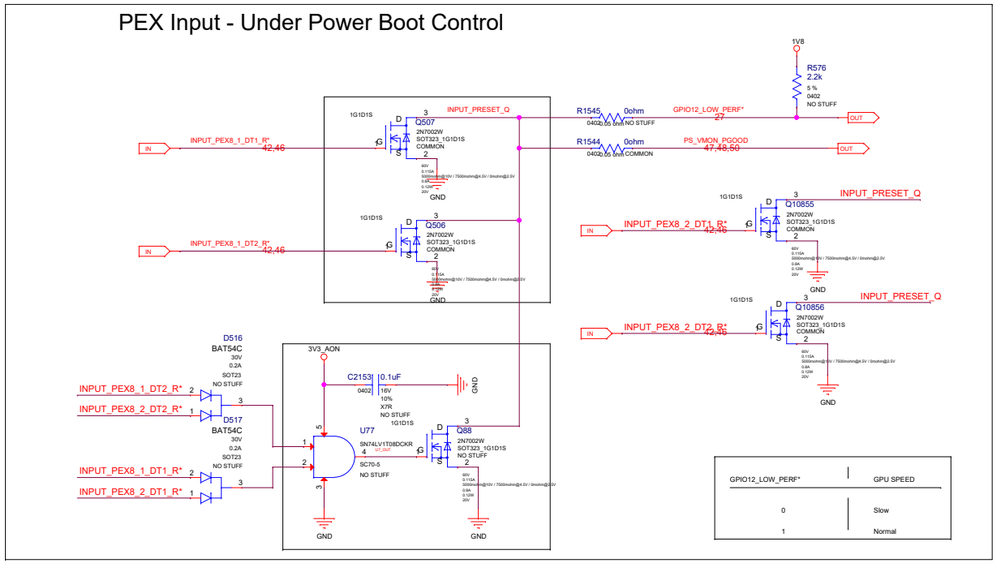
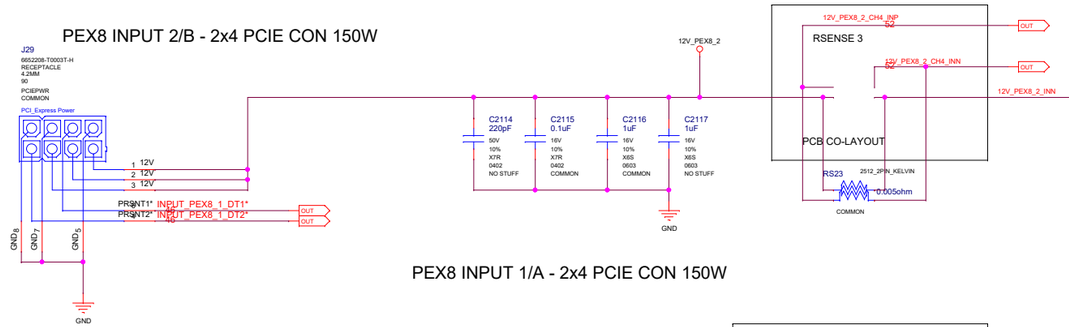
Page44: 12V_EXT_INPUT, FILTERING & UNDER POWER BOOT



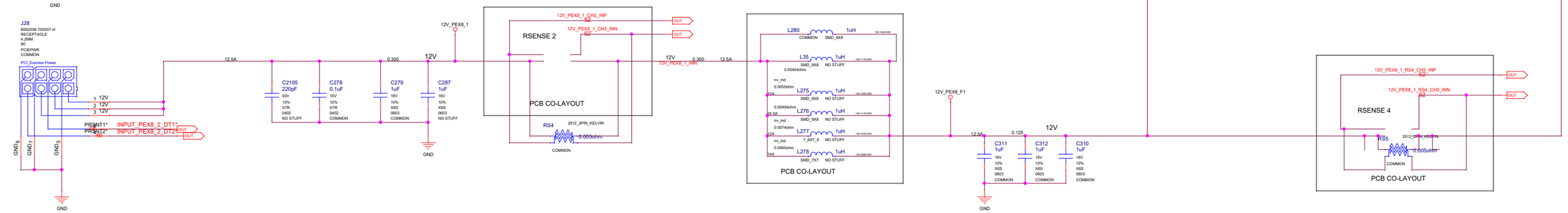
PEX Input - Under Power Boot Control



PEX8 INPUT 2/B - 2x4 PCIE CON 150W



PEX8 INPUT 1/A - 2x4 PCIE CON 150W



$CDS_IMAGE|clipboard_0_2.jpg|3896|1097

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUTS, FILTERING and MONITORING

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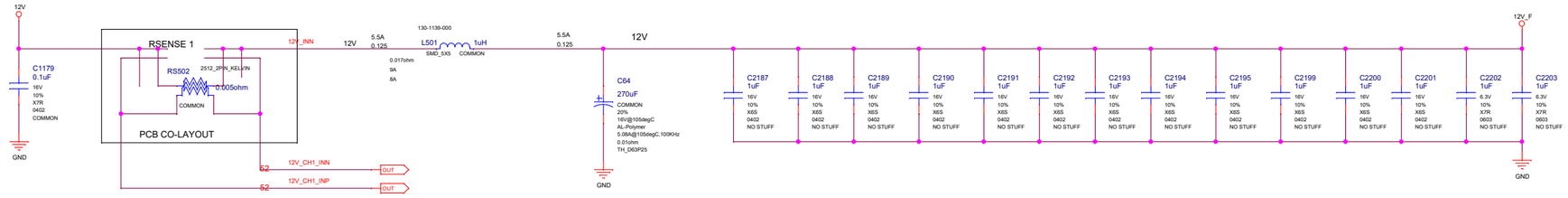
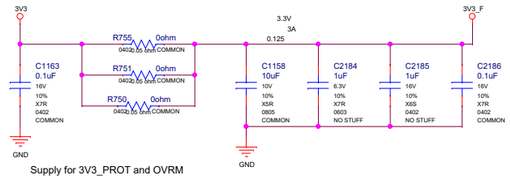
Page45: PEX_INPUT & FILTERING, PEX_3V3, 3V3_AUX

PEX_12V INPUT - 66W

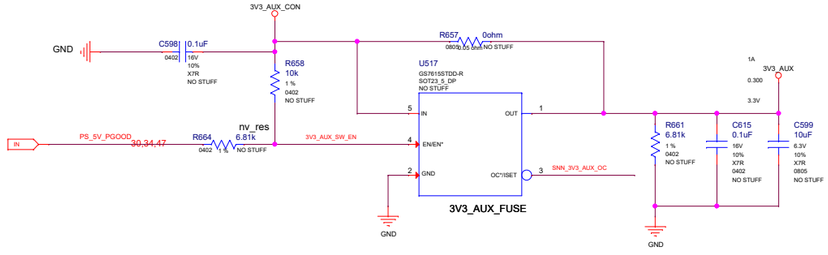


PEX 3V3 INPUT - 10W



Supply for 3V3_PROT and OVRM

3V3_AUX



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEX_12V, PEX_3V3 AND A3V3_AUX

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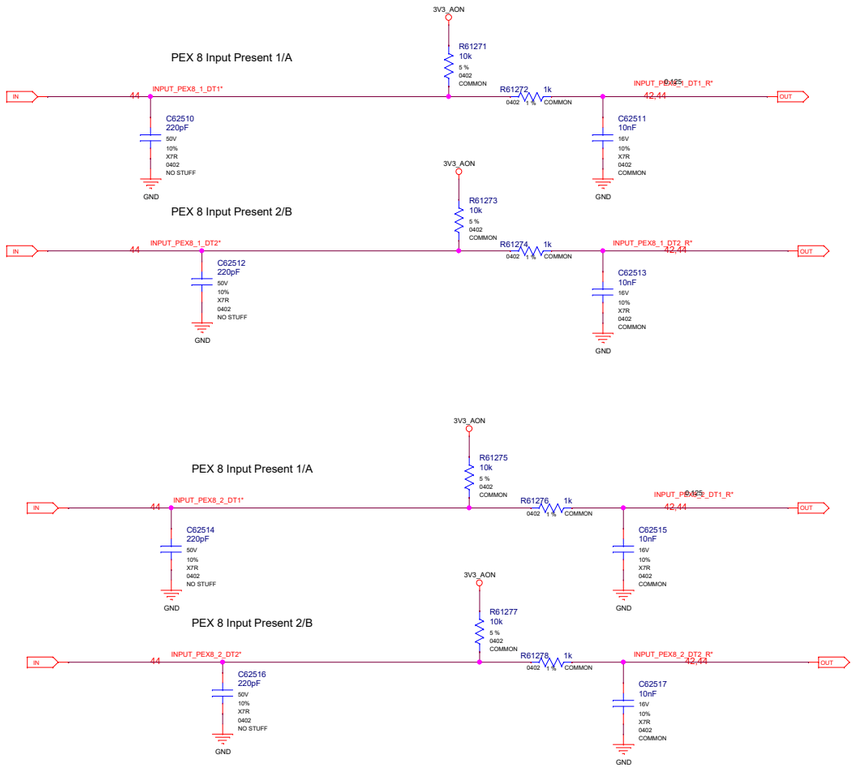
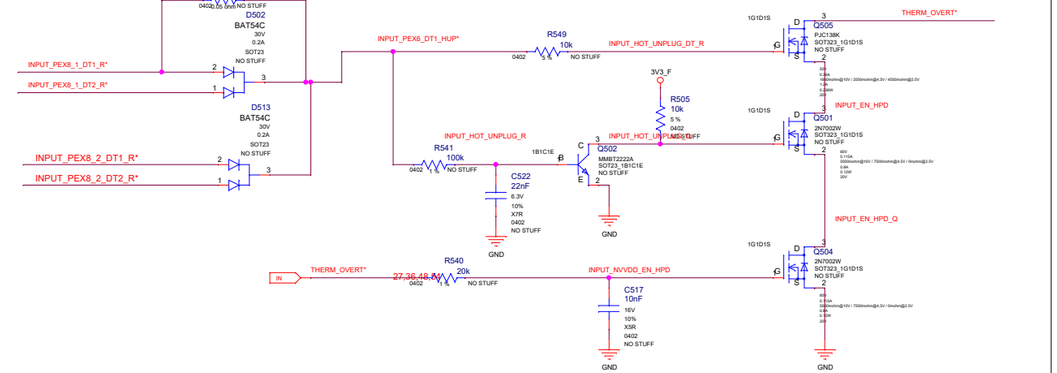
Page46: STEERING, UPB, HOT UNPLUG

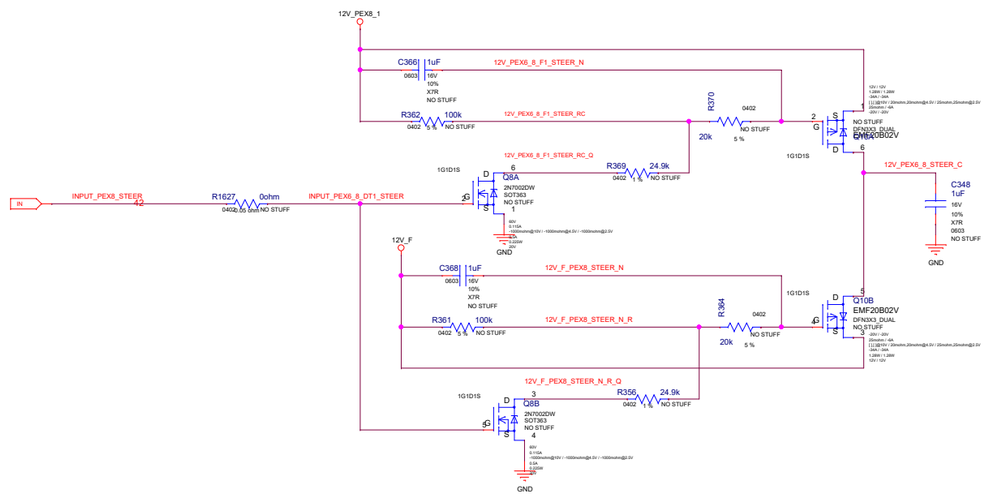


POWER CONNECTOR HOT-UNPLUG DETECT



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: STEERING, UPB, HOT UNPLUG

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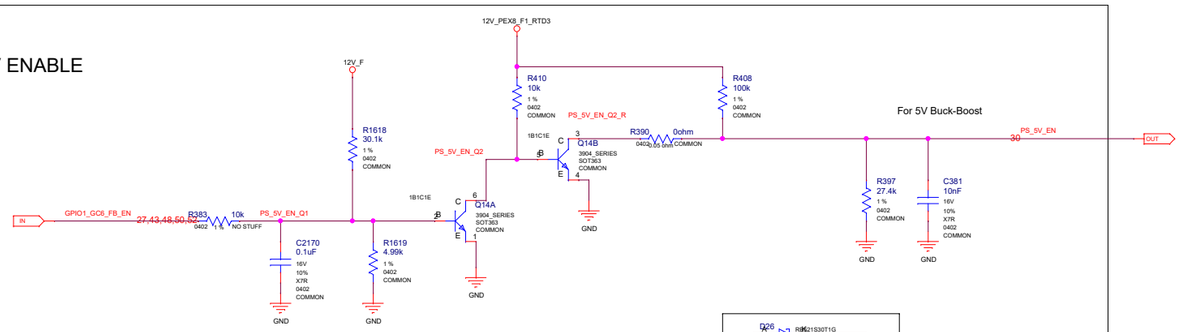
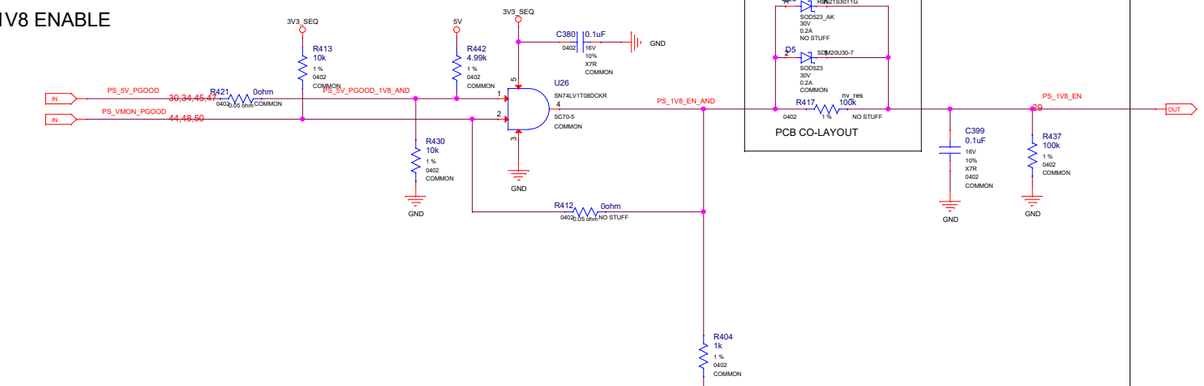
Page47: SEQ: 5V, 1V8, 3V3_SEQ, DDC_5V, DP_AUX_PROT

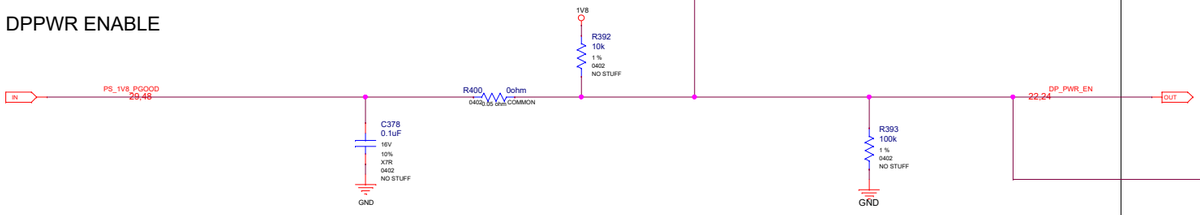
5V ENABLE



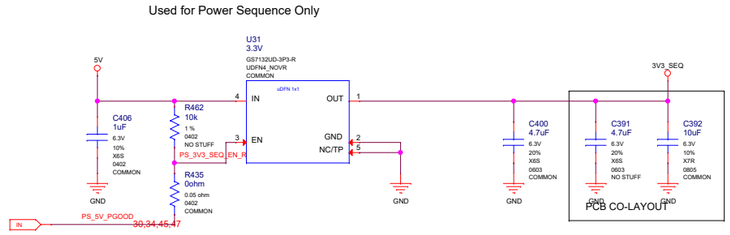
1V8 ENABLE



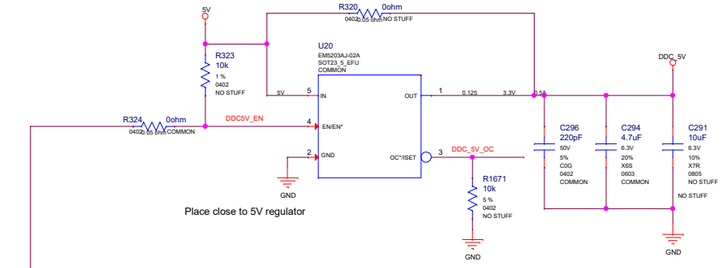
DPPWR ENABLE



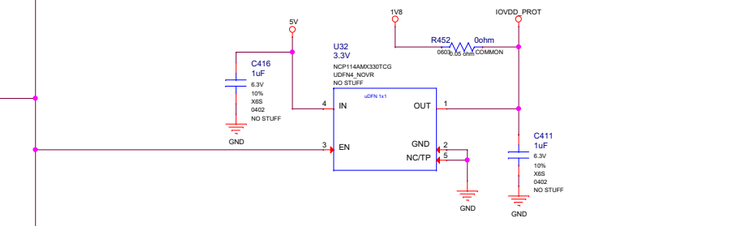
3V3_SEQ



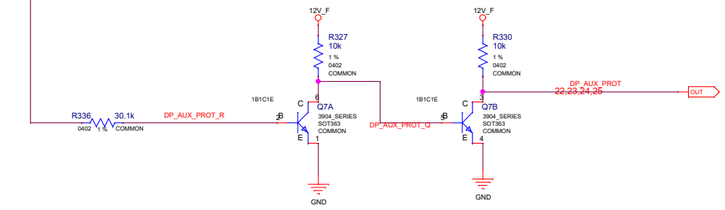
DDC_5V



IOVDD_PROT



DP_AUX PROTECTION



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: 5V, 1V8, 3V3_SEQ

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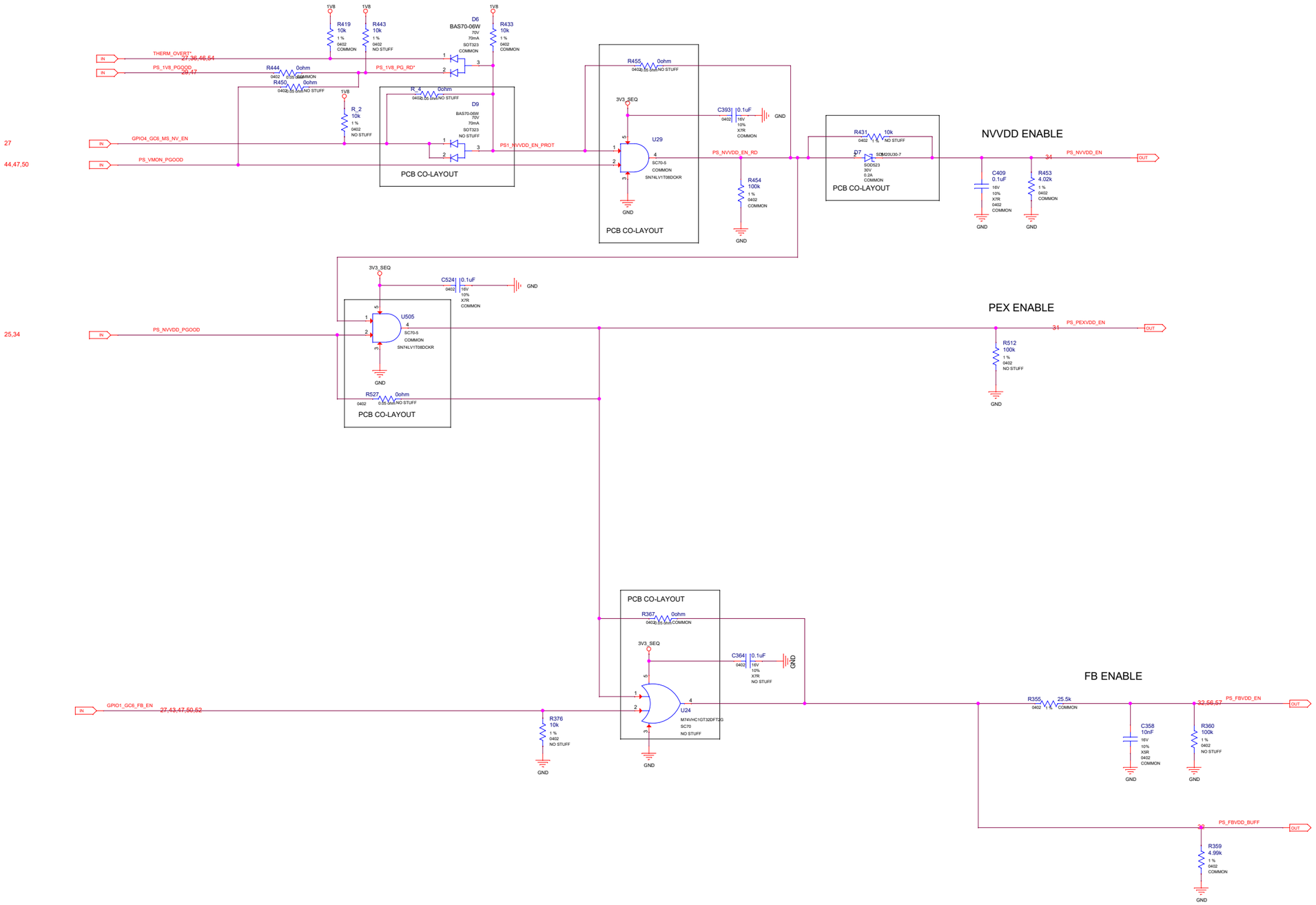
Page48: SEQ:NVVDD, PEX, FBVDDQ ENABLE



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NVVDD, PEX, FBVDDQ ENABLE

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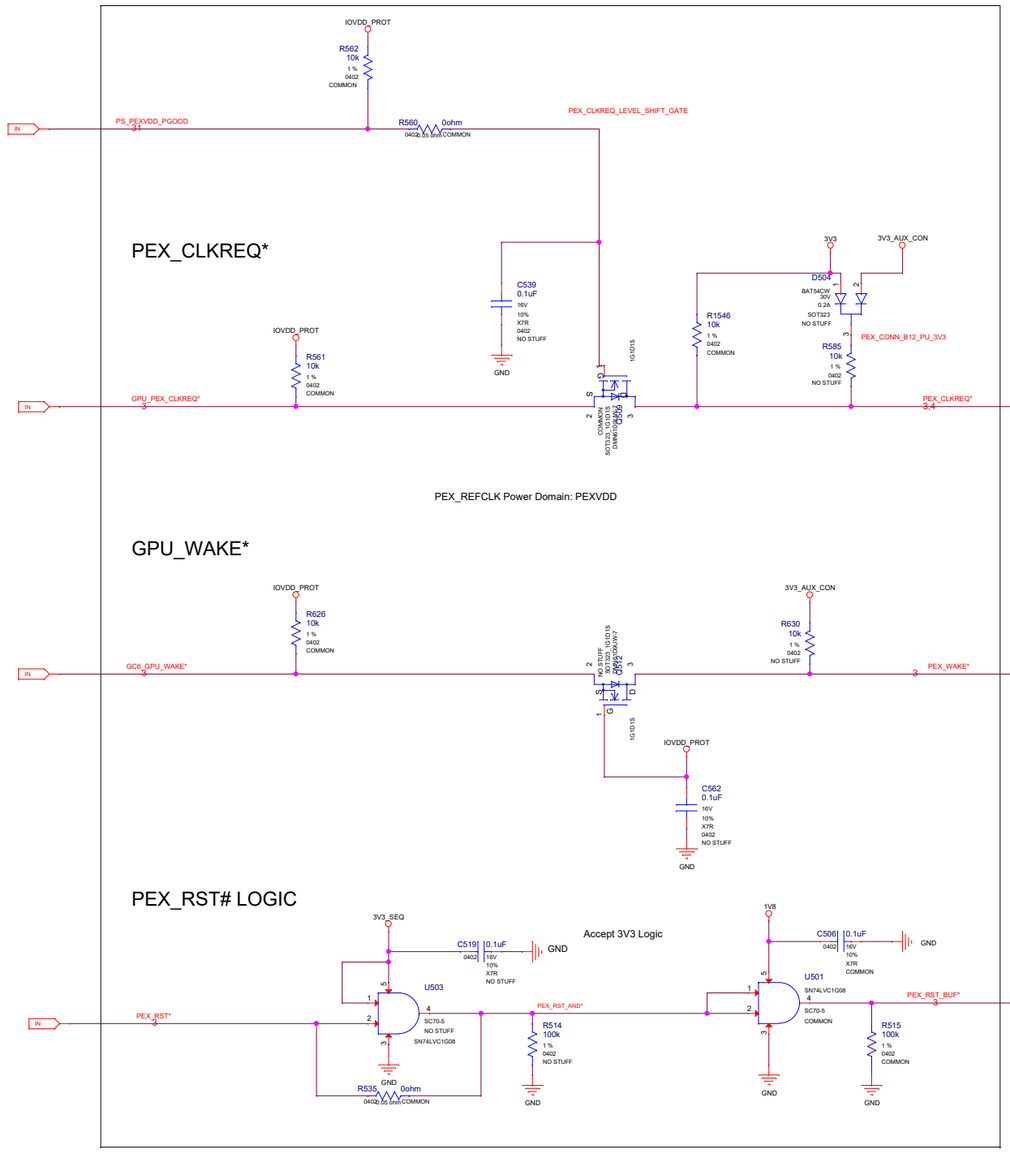
Page49: SEQ:MISC



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: MISC

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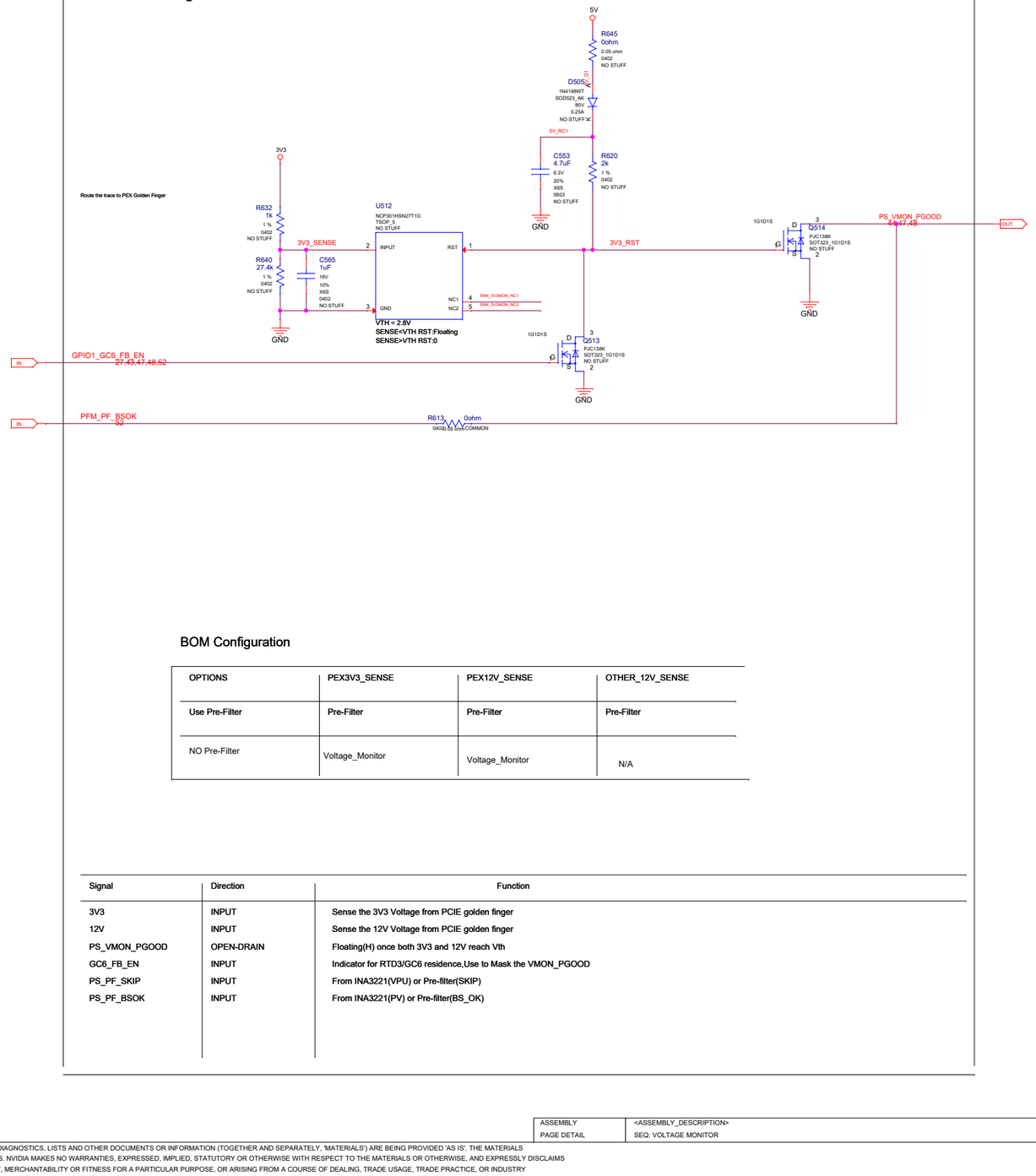
Page 50: SEQUENCE:Voltage Monitor

3V3PEX Voltage Monitor



BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: VOLTAGE MONITOR

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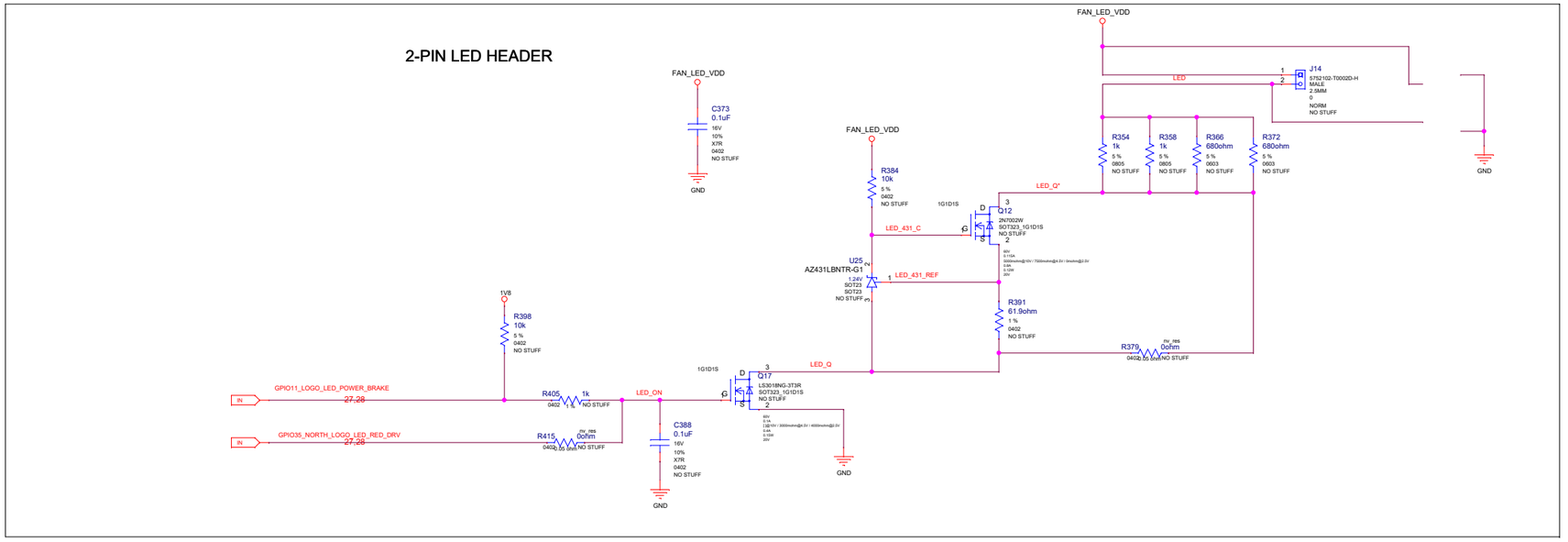
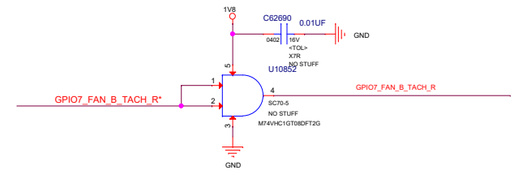
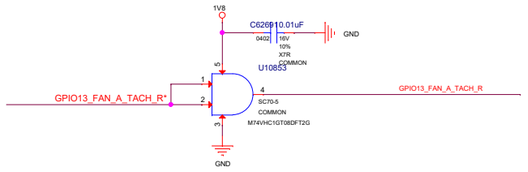
Page51: FAN&LED

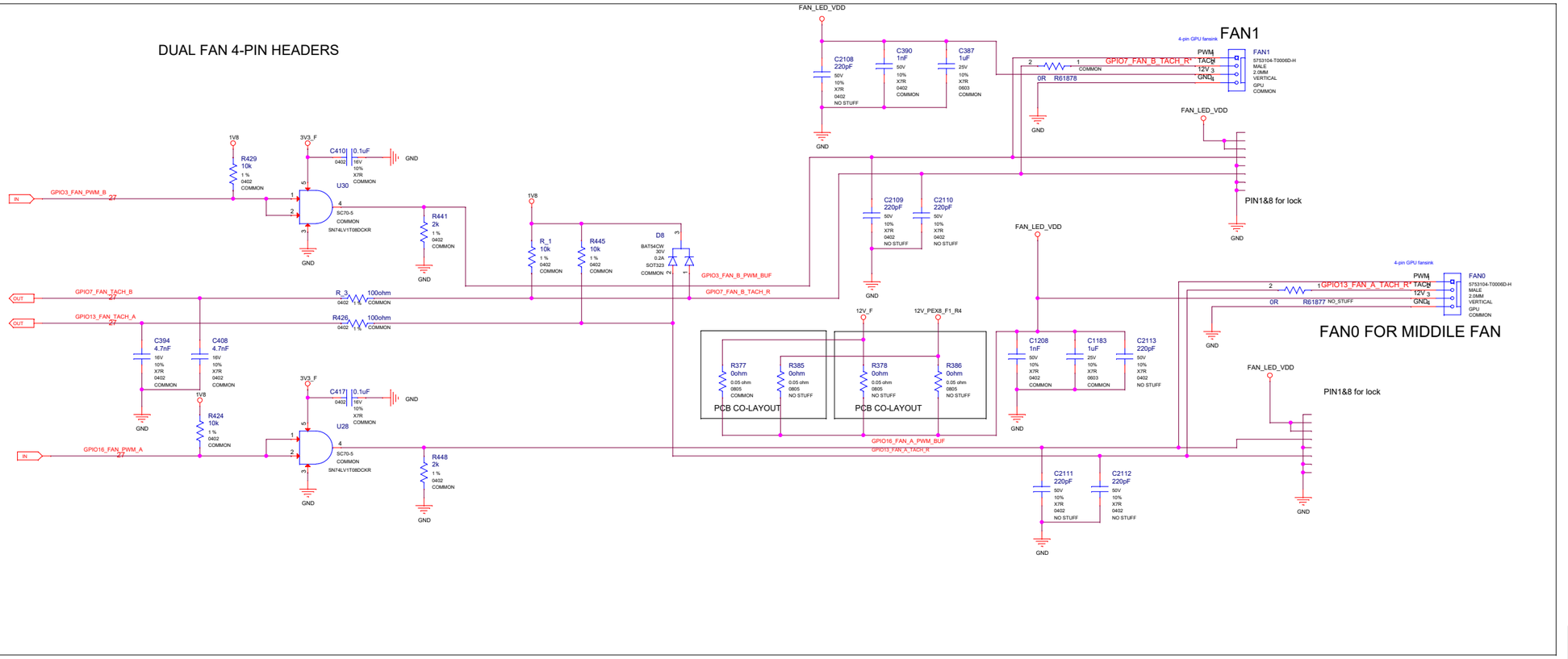
2-PIN LED HEADER







DUAL FAN 4-PIN HEADERS



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	FAN & LED

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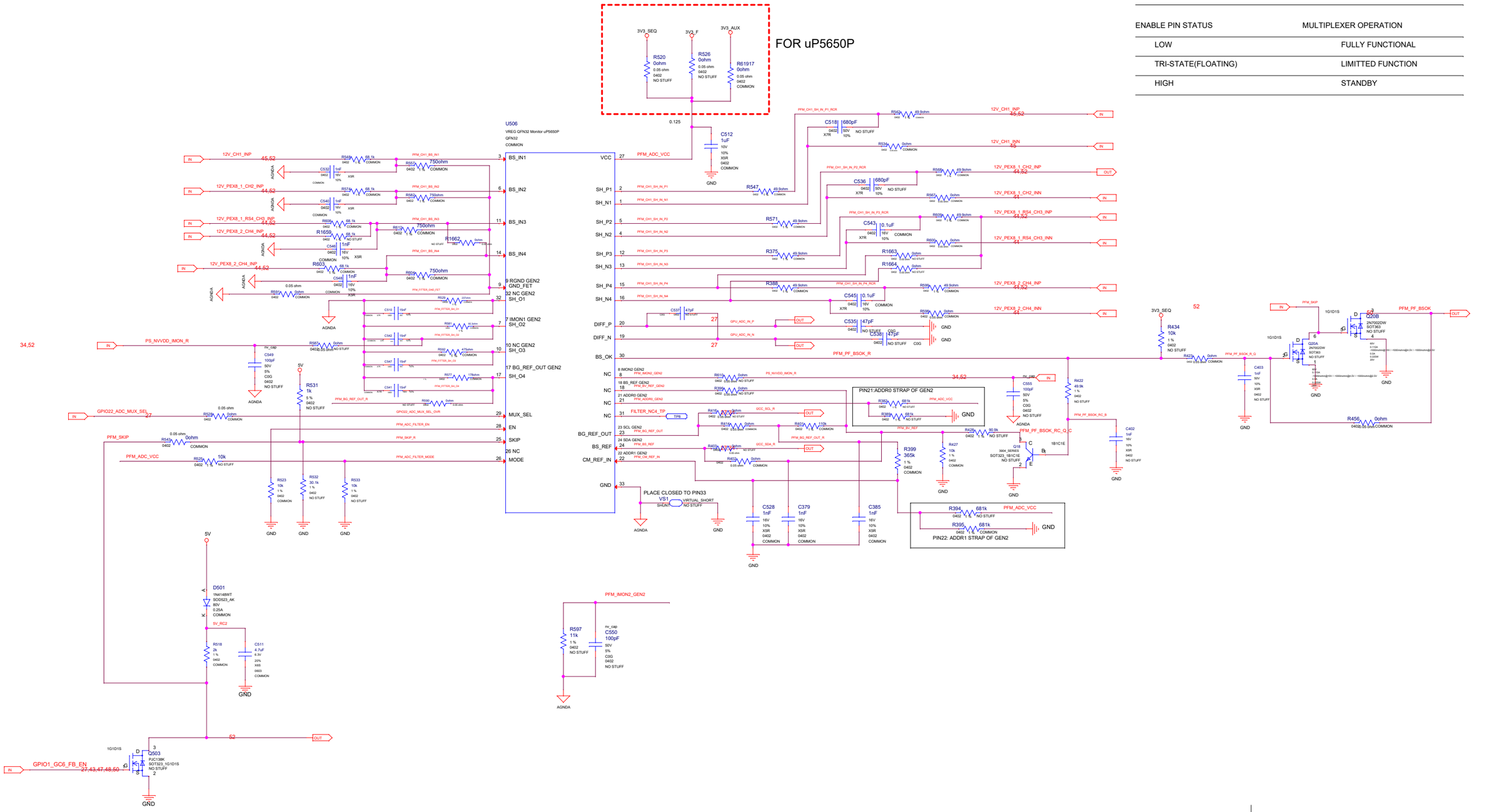
Page52: OVRM_PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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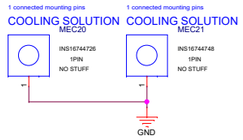
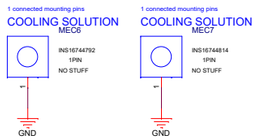
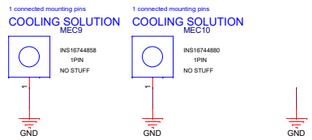
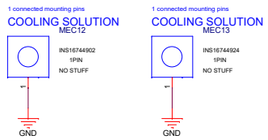
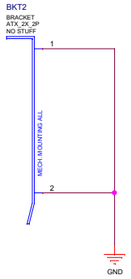


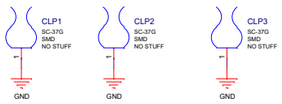






GPU Stiffner back side





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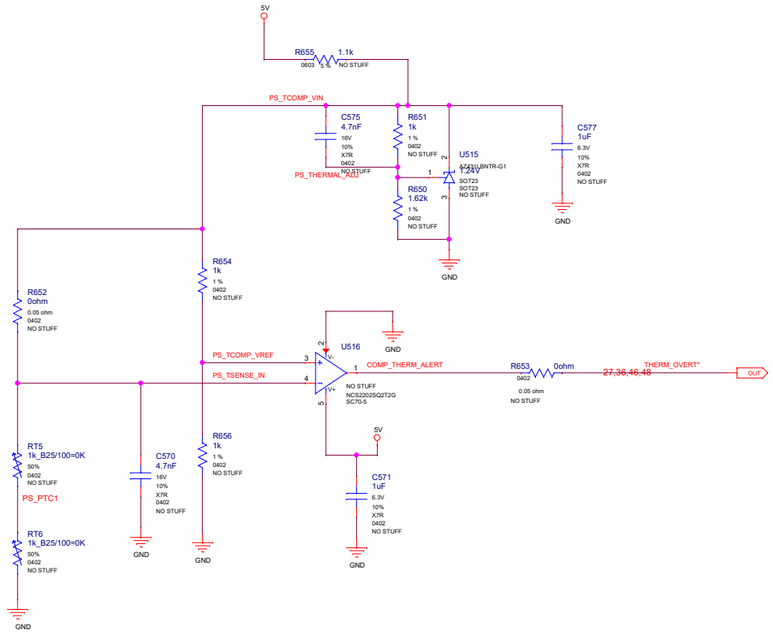

Close to FBVDD MOS

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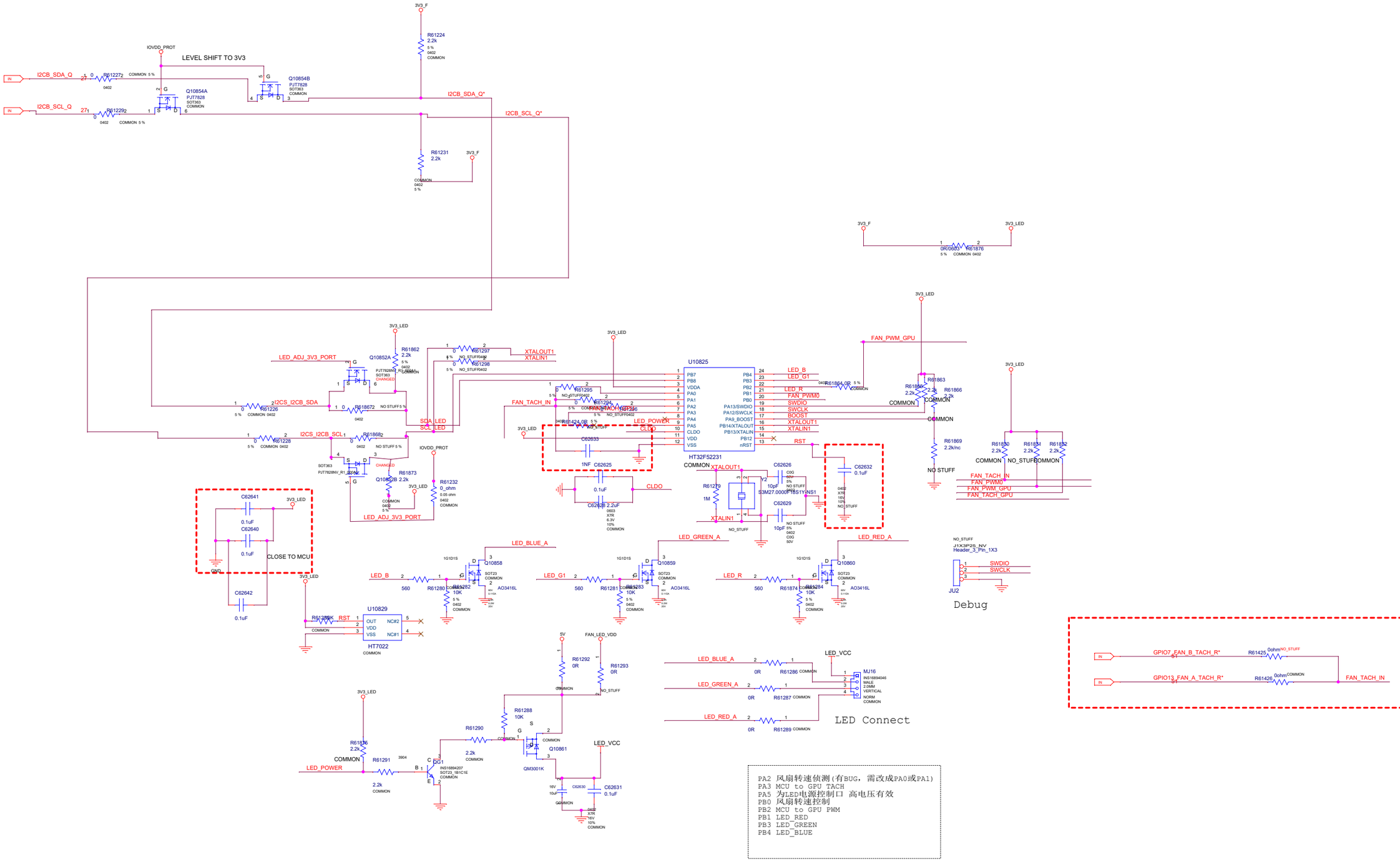

PA2 风扇转速侦测(有BUG，需改成PA0或PA1)
PA3 MCU to GPU TACH
PA5 为LED电源控制口 高电压有效
PB0 MCU to GPU PWM
PB2 MCU to GPU PWM
PB1 LED_RED
PB3 LED_GREEN
PB4 LED_BLUE

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PS: FBVDDQ OVR2+1

NCP81273 EN VIH >1.5V, VIL < 0.7V
UP9509/10 EN VIH >1.2V, VIL < 0.6V
RT8817A EN VIH >1.2V, VIL < 0.6V

12V uP9510 NCP81273

5V uP9509 RT8813 RT8817

PCB CO-LAYOUT

U10854 UP9509S
UP9509S
QFN4X4
COMMON

OPENVREG
OPT1 OPT2
VCC ISEN1

OPT1 OPT2
TALERT ISEN2
TSNS ISEN3
GND PWM3
THERM/GND

Set OCP per phase =100A

Roc=500mV/((OCP*Rds(on)*1.5-40mV)/360*255(uA)/8 + 5uA)

Set SS

Stuff for 2 phases

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