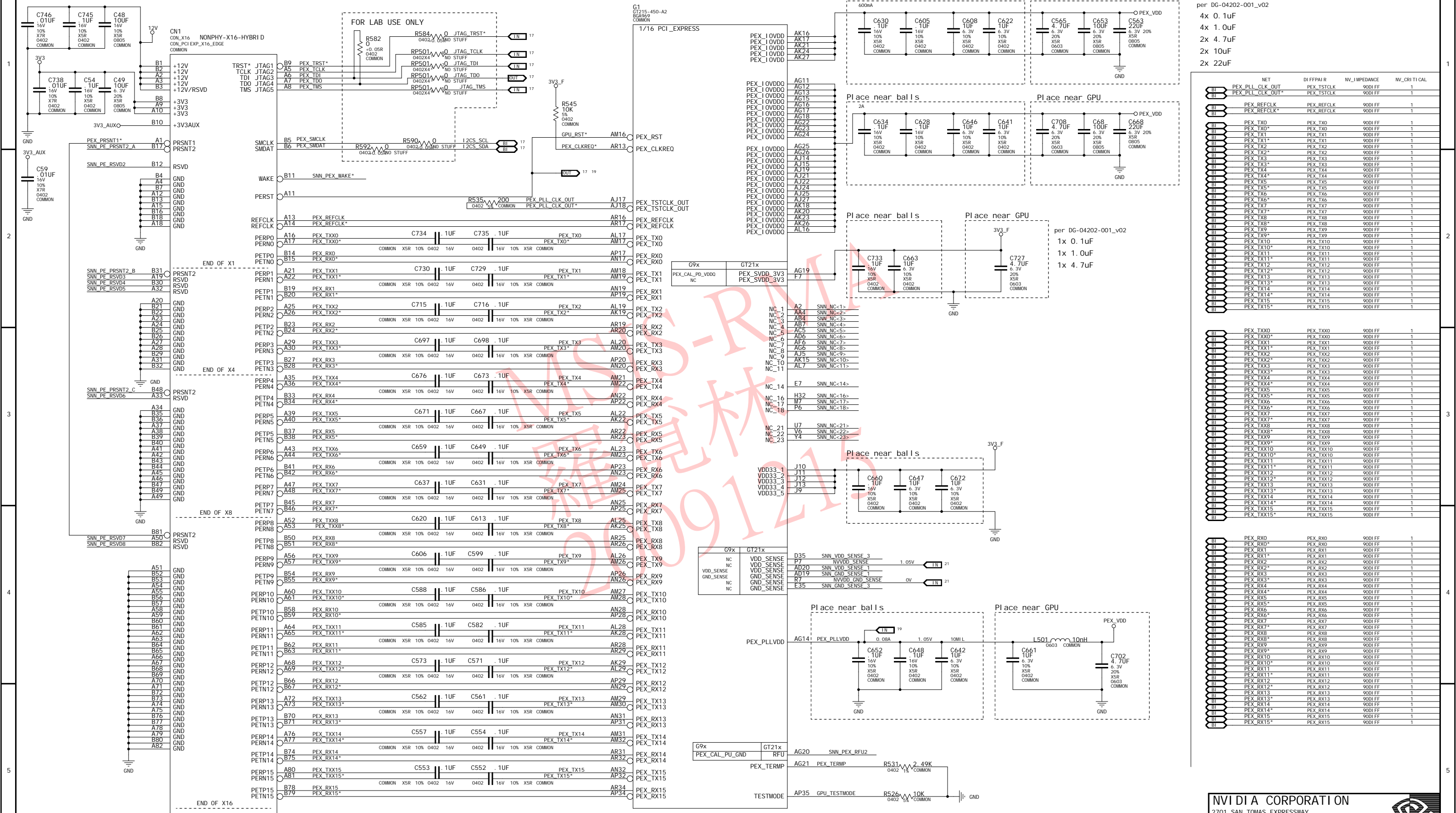



P673: GT215 128-bit, 32Mx32/64Mx16 GDDR5
DL-DVI, VGA, HDMI

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Page 2: PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS
Page 3: Frame Buffer Interface
Page 4: Frame Buffer Partition A - Lower Half
Page 5: Frame Buffer Partition A - Upper Half
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Page 9: DACA FOR SOUTH DVI-I
Page 10: DACB FOR MID VGA
Page 11: LINK A/B FOR SOUTH DUAL-LINK DVI-I
Page 12: LINK C FOR NORTH HDMI
Page 13: LINK D UNUSED
Page 14: LINK E/F UNUSED
Page 15: MIOA AND MIOB UNUSED
Page 16: XTAL AND MECHANICAL AND THERMAL PARTS
Page 17: THERMAL ALERT, FAN CONTROL, GPIO, INFOROM, AND JTAG
Page 18: STRAPPING AND VBIOS ROM
Page 19: 5V, 5VDDC, IFP_PLLVDD, IFP_IOVDD, 3V3 FILTER, AND 12V FILTER
Page 20: FBVDDQ SINGLE PHASE SWITCHER, PEX_VDD LINEAR
Page 21: NVVDD DUAL-PHASE SWITCHER

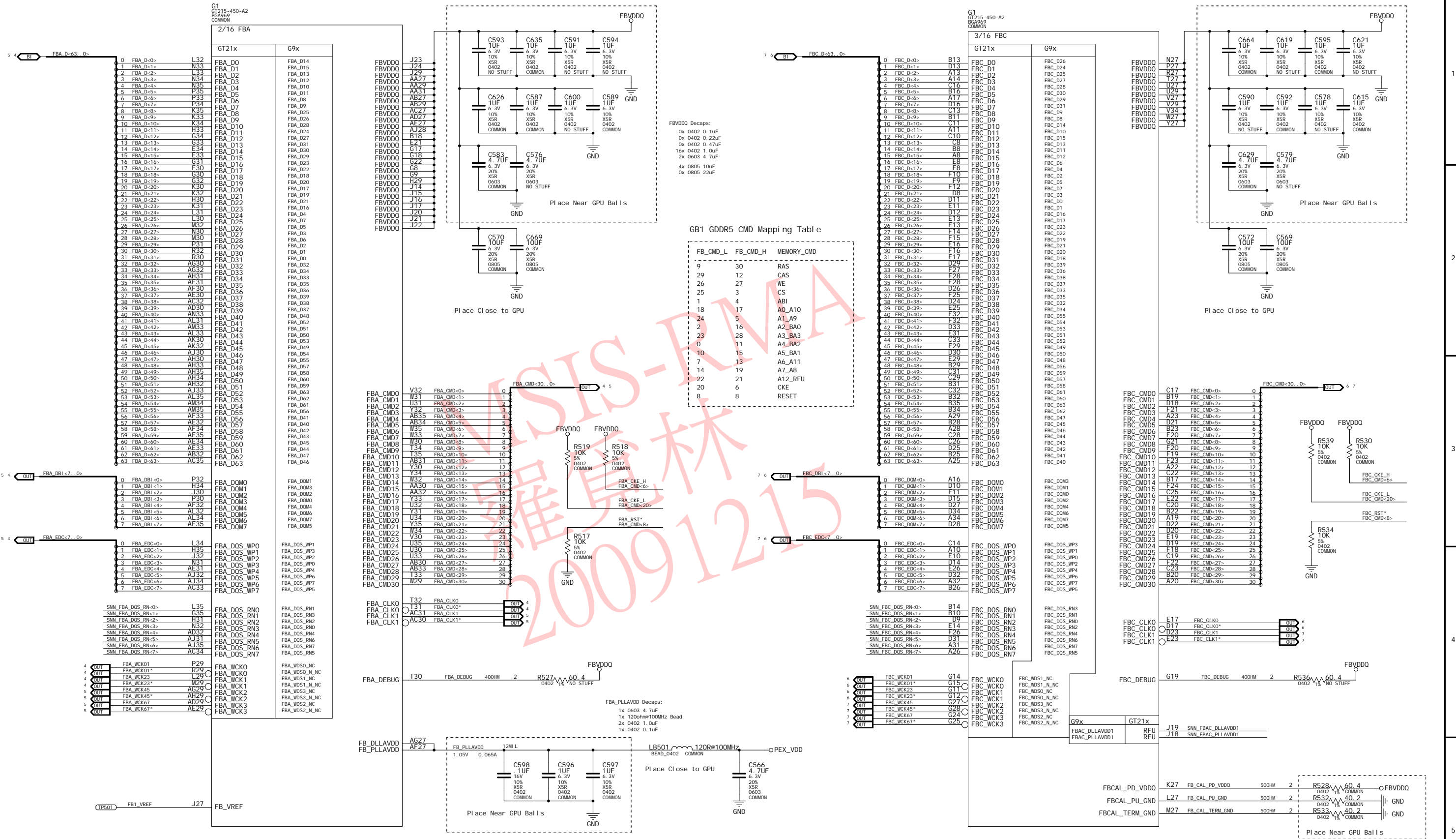
SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10673-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10673-0001-100	GT215-450, 575/1443MHz 1024MB 64Mx16 BGA170 1800MHz GDDR5 DVI-I/VGA/HDMI
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	SKU0005	600-10673-0005-100	GT215-450, 575/1443MHz 512MB 32Mx32 BGA170 1800MHz GDDR5 DVI-I/VGA/HDMI
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

2. PEX x16 Interface

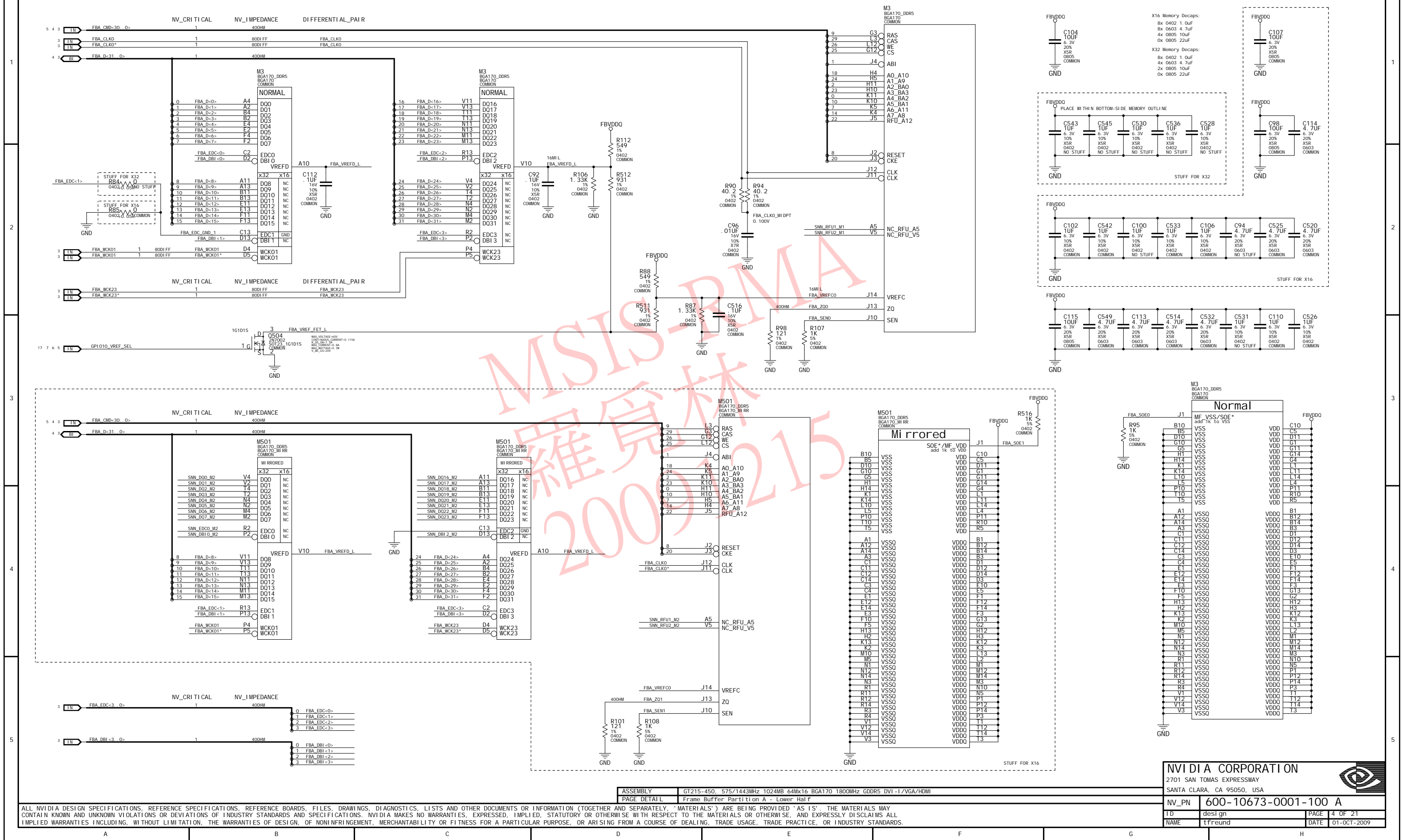


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NV_PN		600-10673-0001-100 A	
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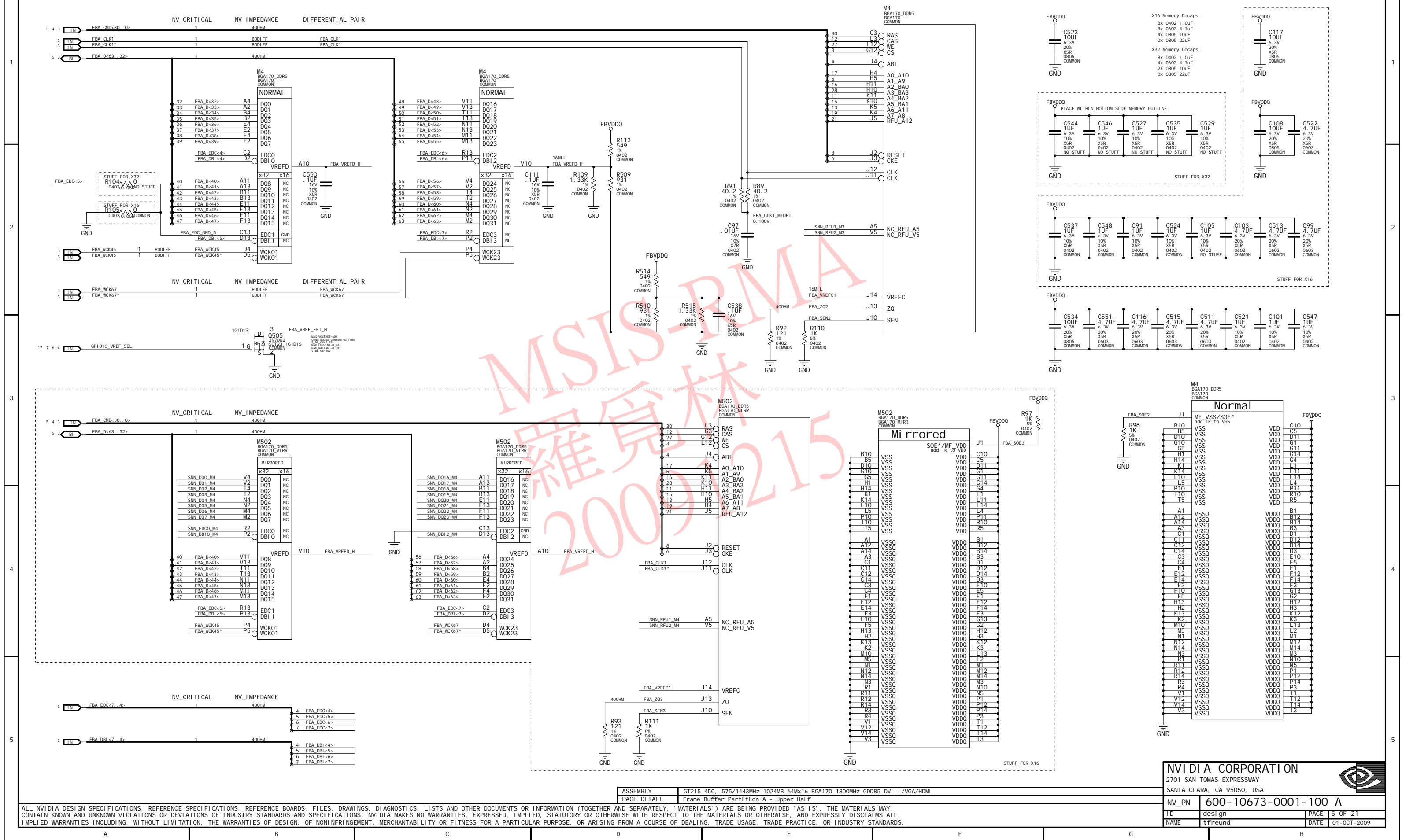
3. Frame Buffer Interface



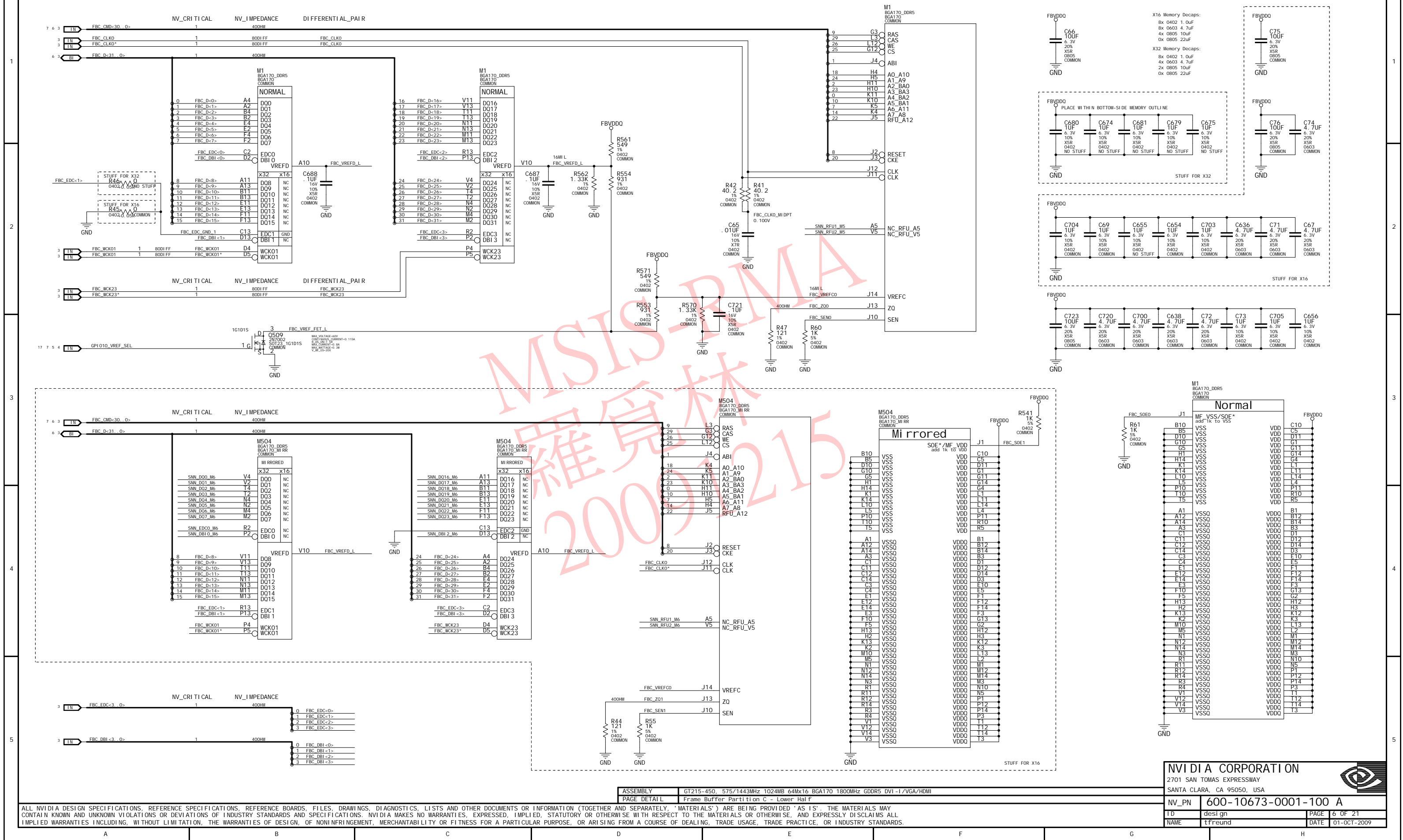
4. Frame Buffer Partition A - Lower Half



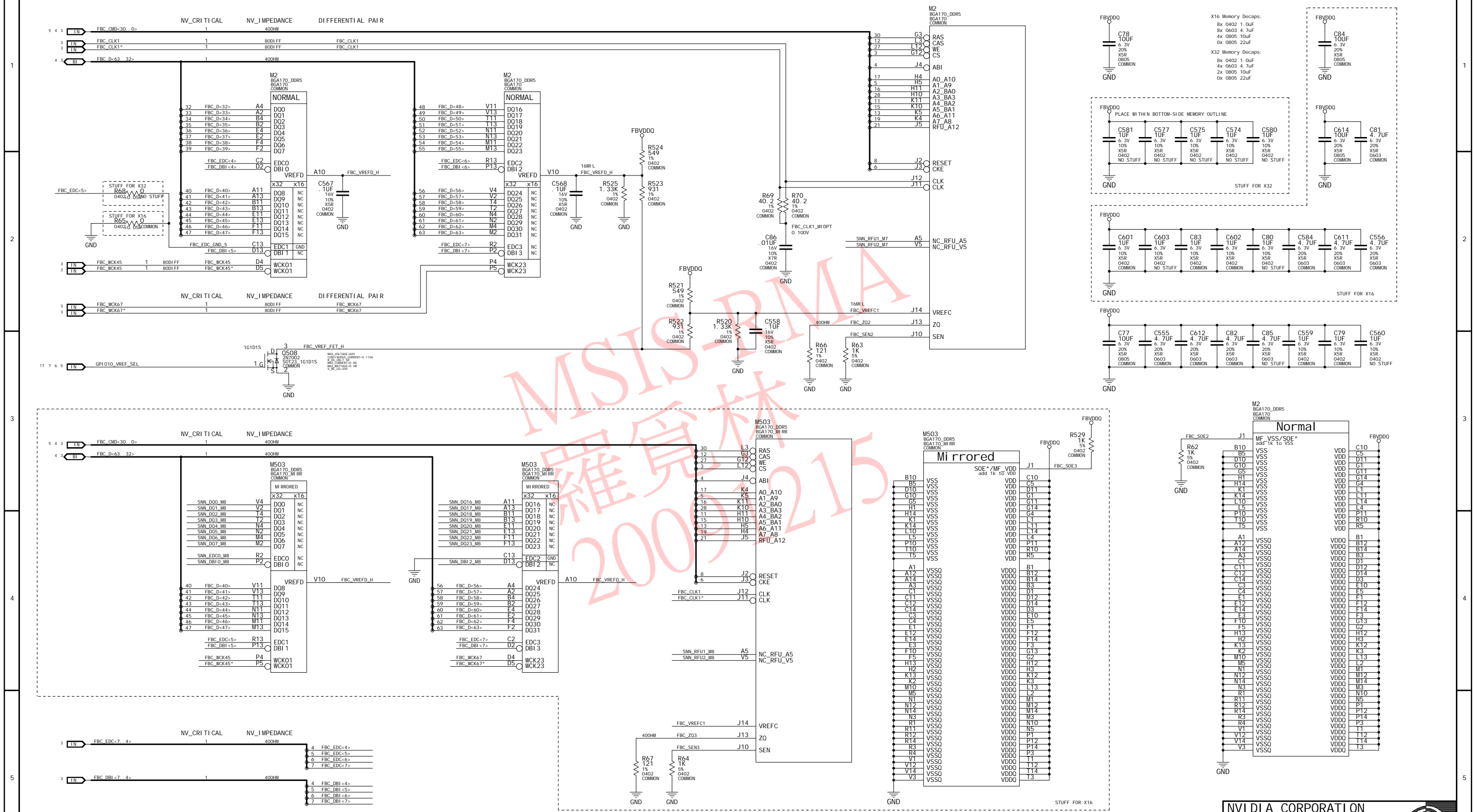
5. Frame Buffer Partition A - Upper Half



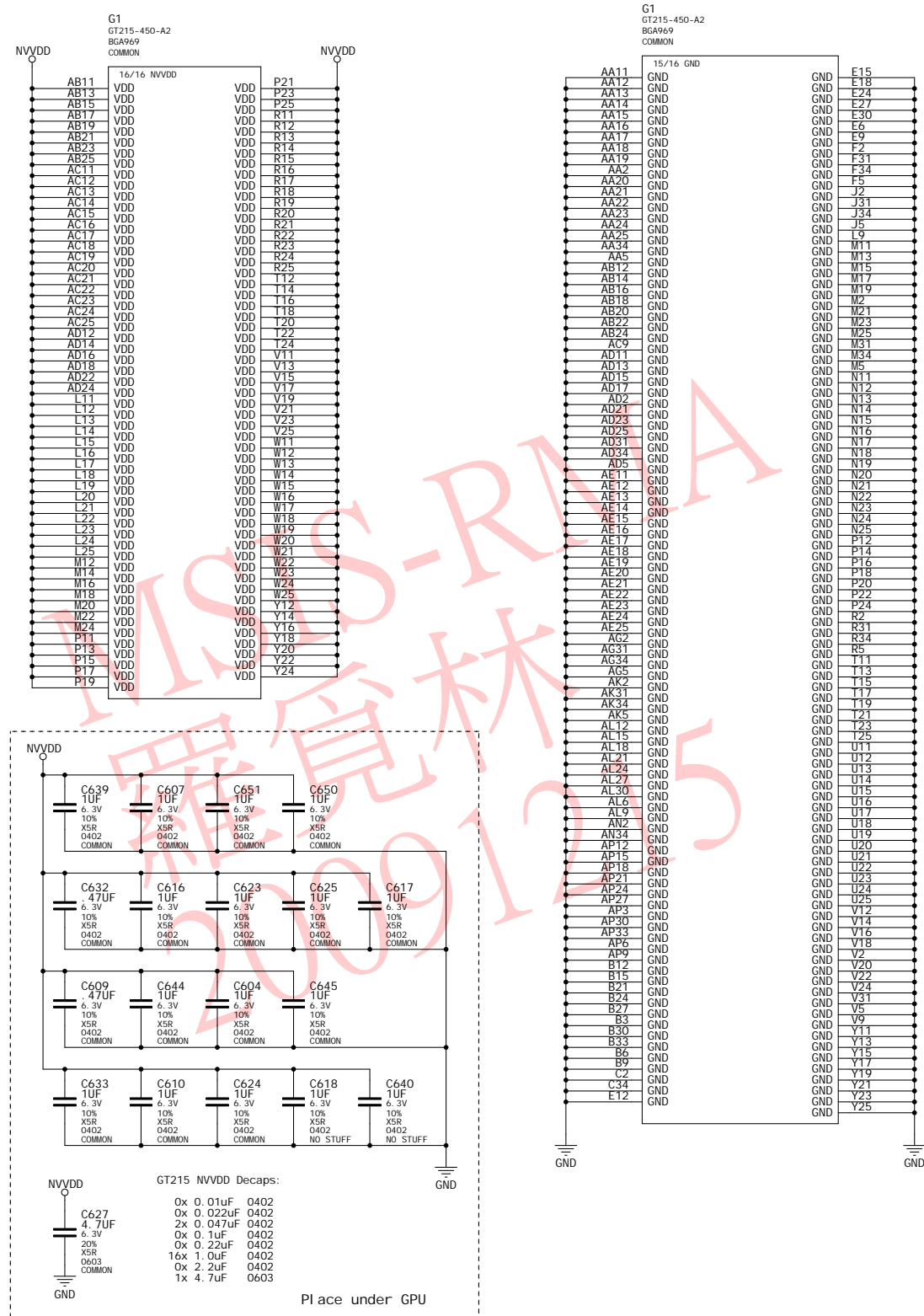
6. Frame Buffer Partition C - Lower Half



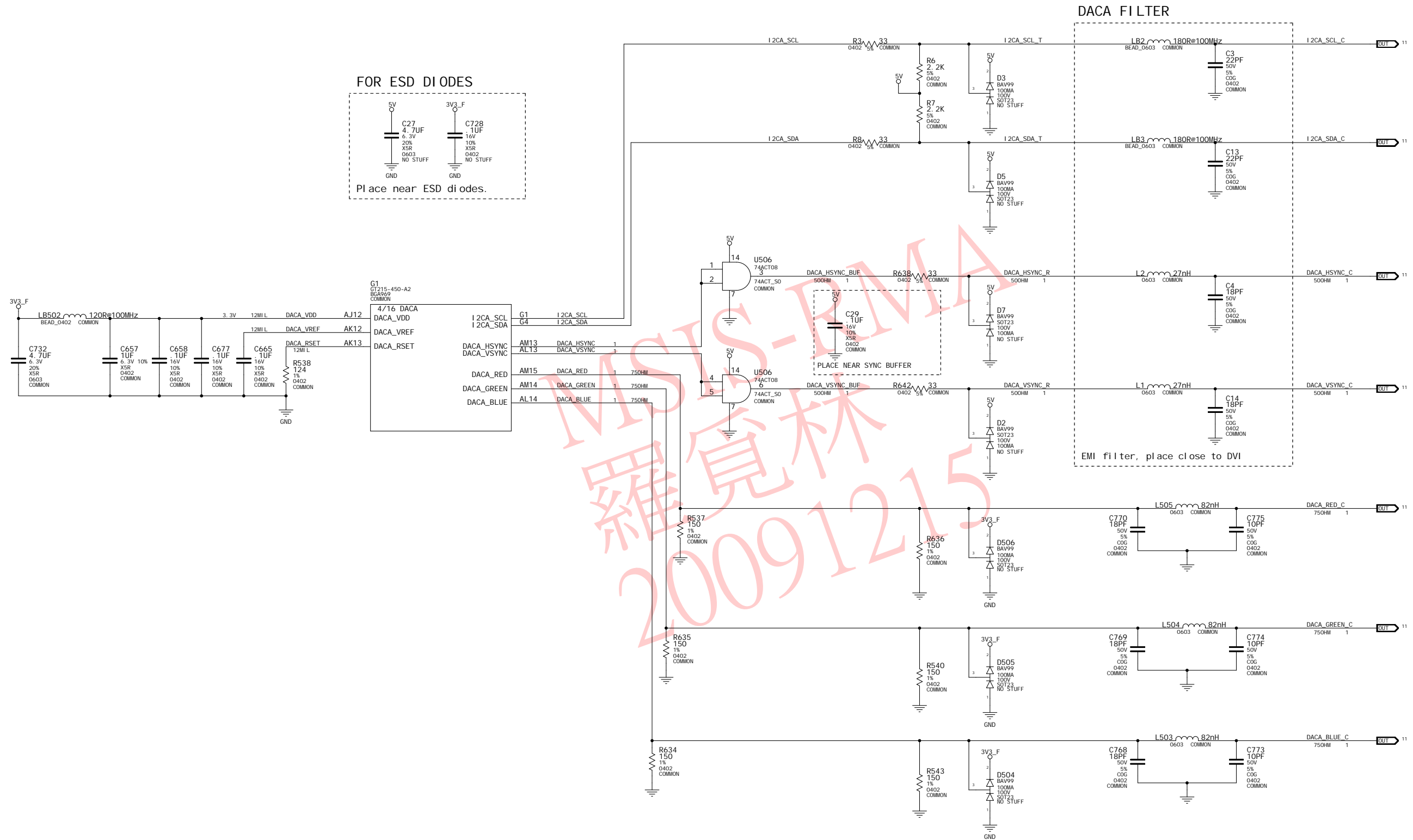
7. Frame Buffer Partition C - Upper Half



8. NVVDD Decoupling



9. DACA for South DVI -I



ASSEMBLY	GT215-450, 575/1443MHz 1024MB 64Mx16 BGA170 1800MHz GDDR5 DVI -I /VGA/HDMI
PAGE DETAIL	DACA FOR SOUTH DVI -I

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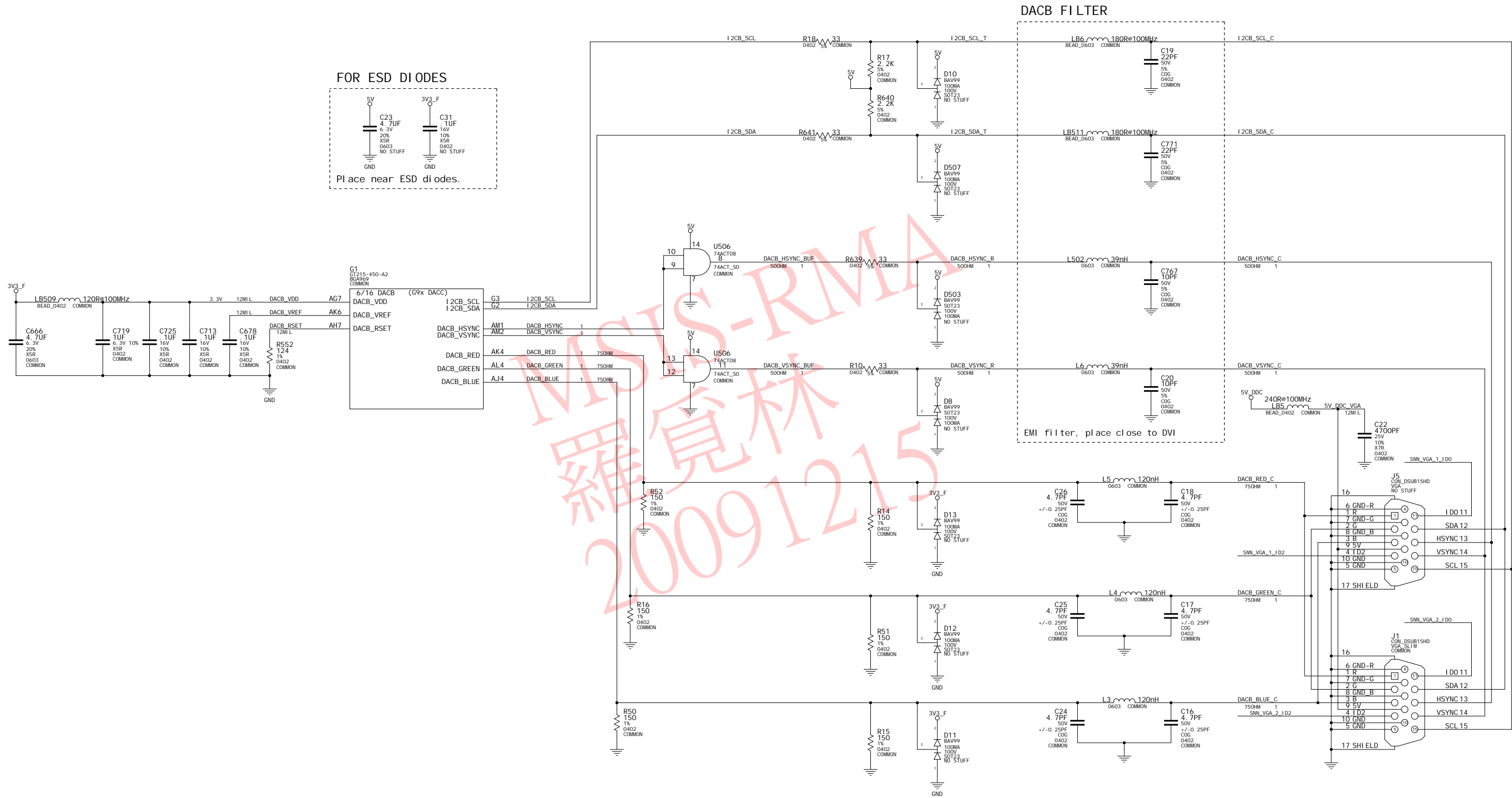
SANTA CLARA, CA 95050, USA

NV_PN	600-10673-0001-100 A
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NAME	tfreund	DATE	01-OCT-2009
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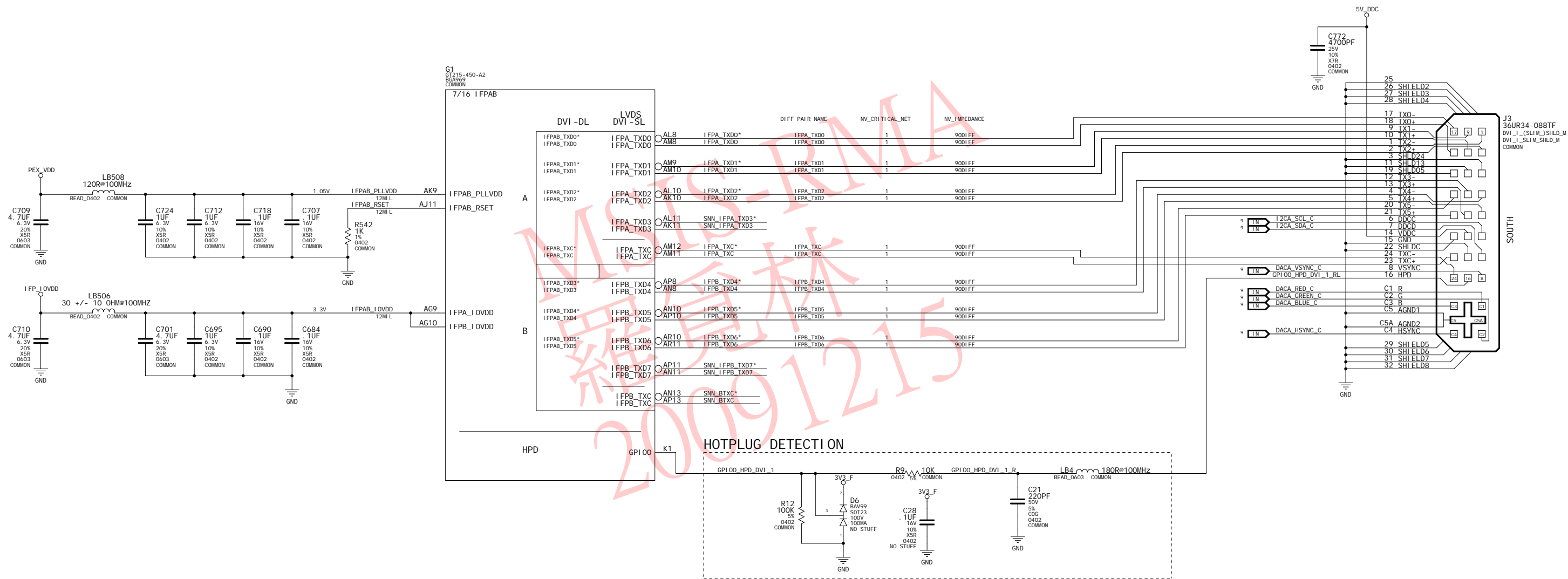
10. DACB for Mi d VGA



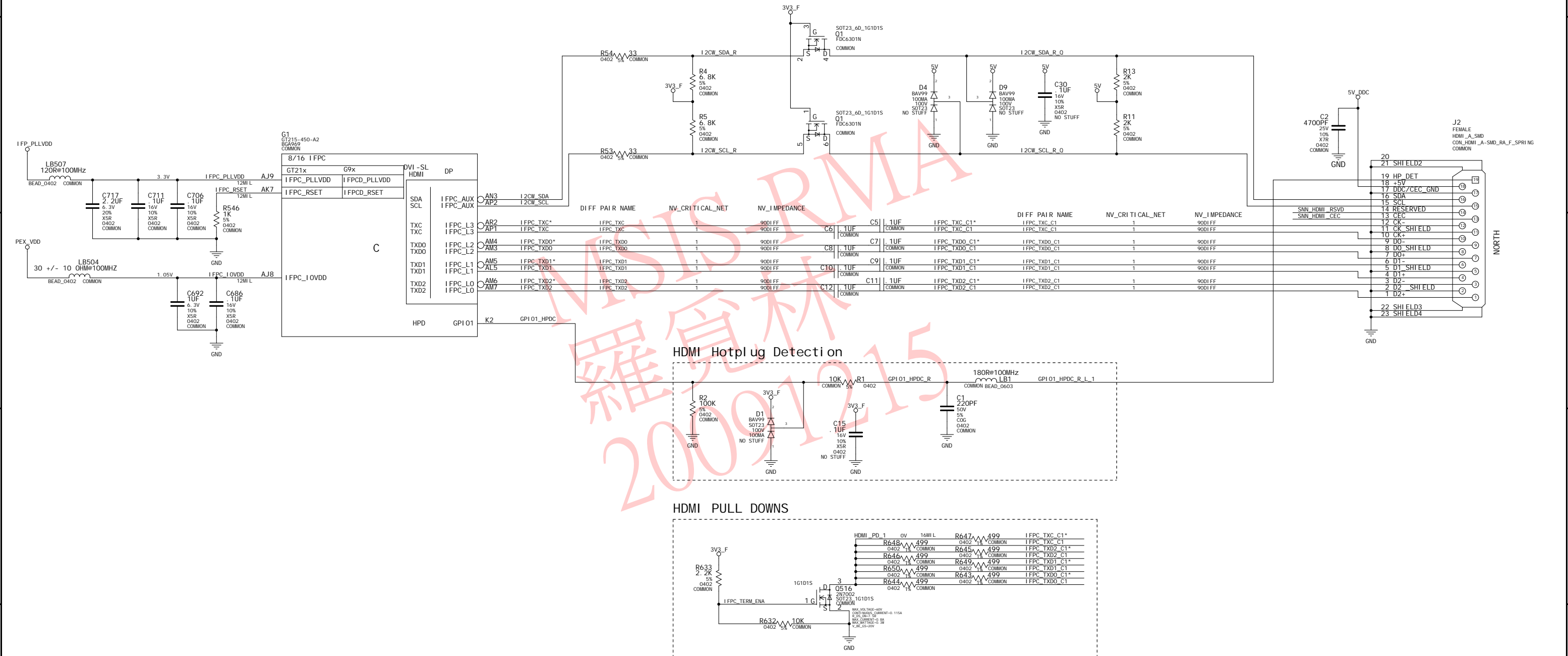
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11. Link A/B for South Dual-Link DVI-I



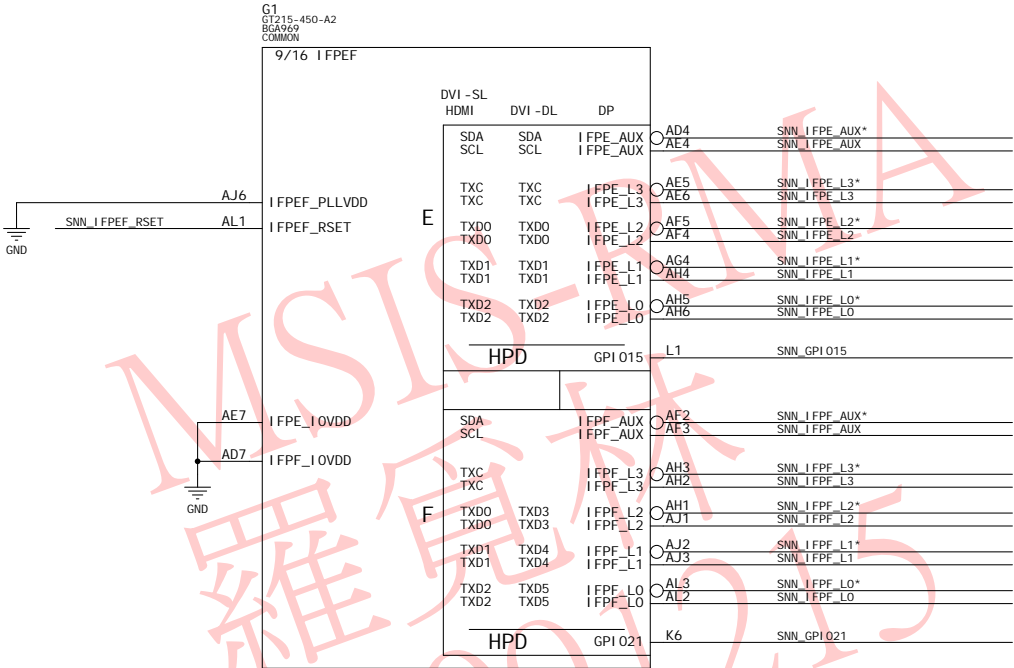
12. Link C for North HDMI



5



14. Link E/F Unused



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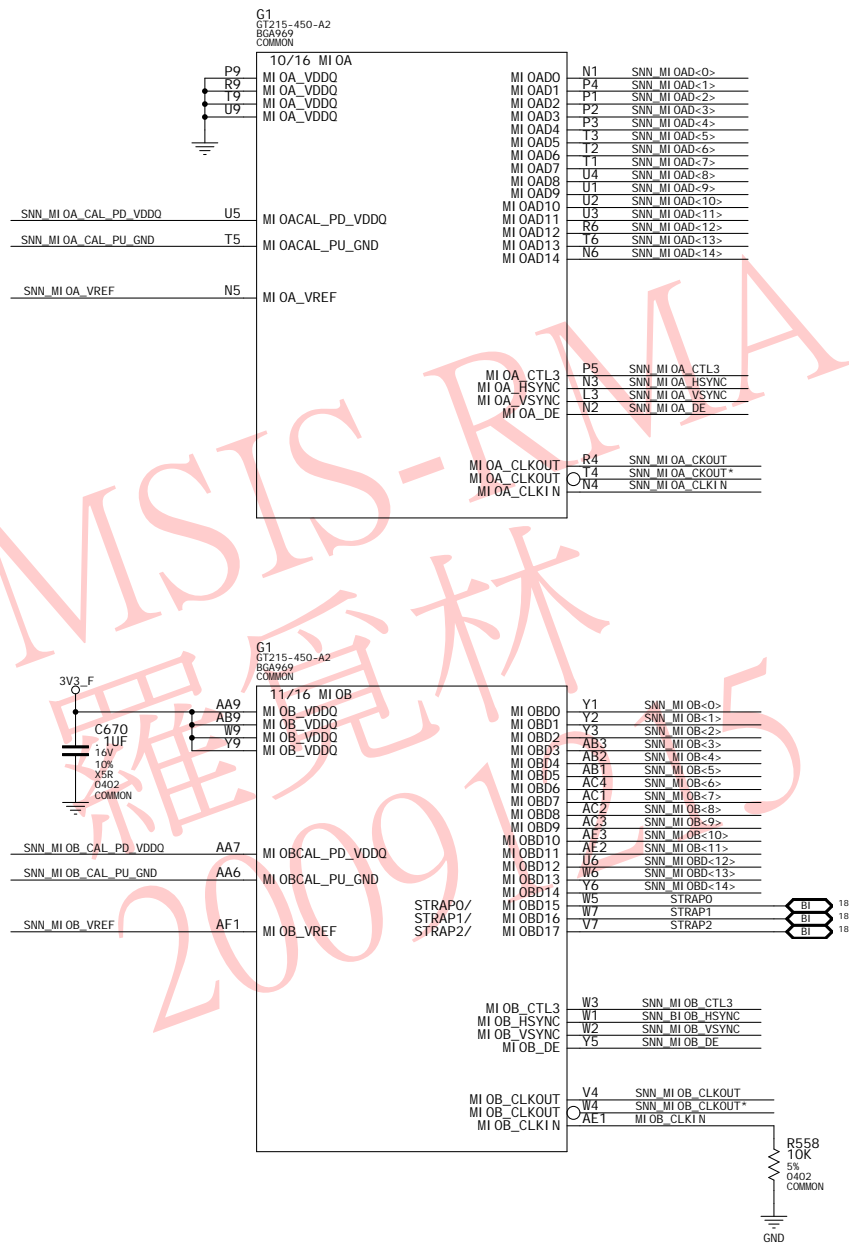


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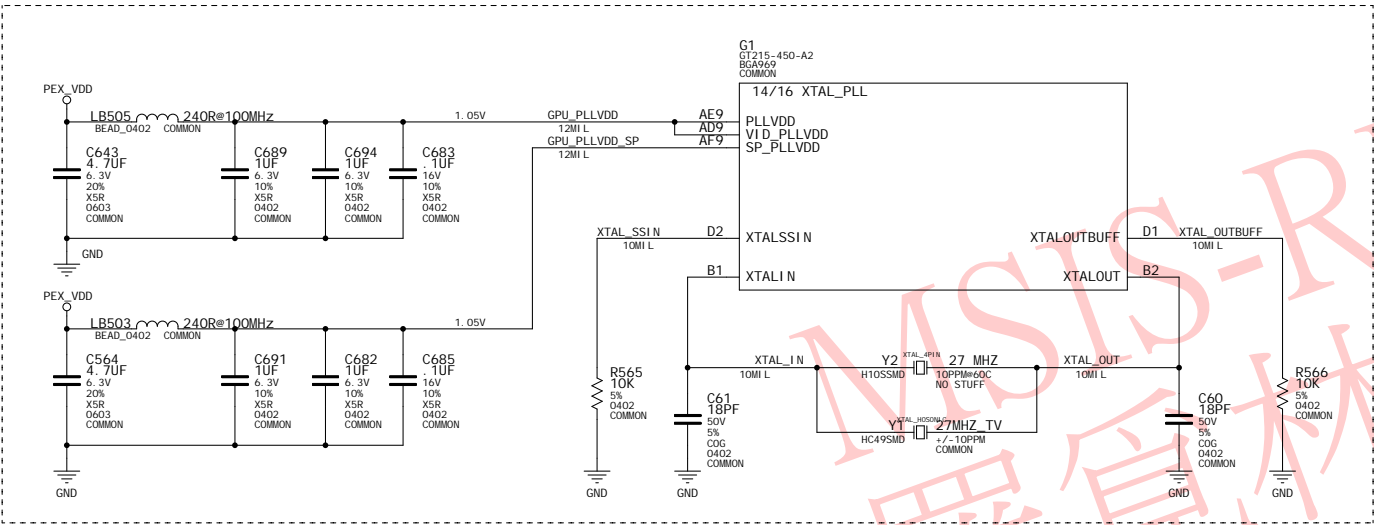
15. MI 0A and MI 0B Unused



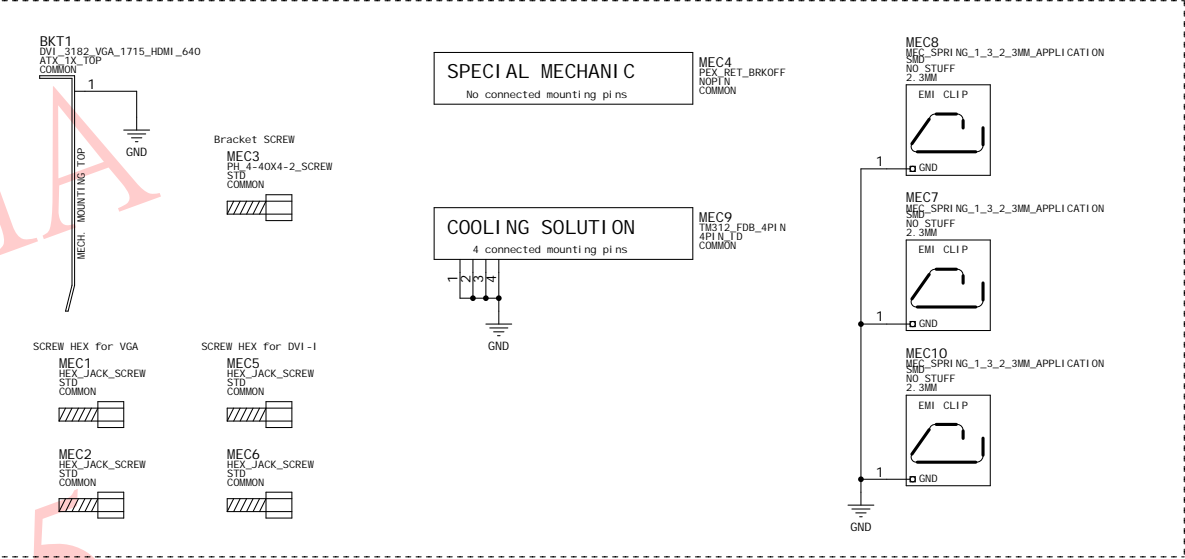
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16. XTAL and Mechanical and Thermal Parts

XTAL/GPU_PLLVDD



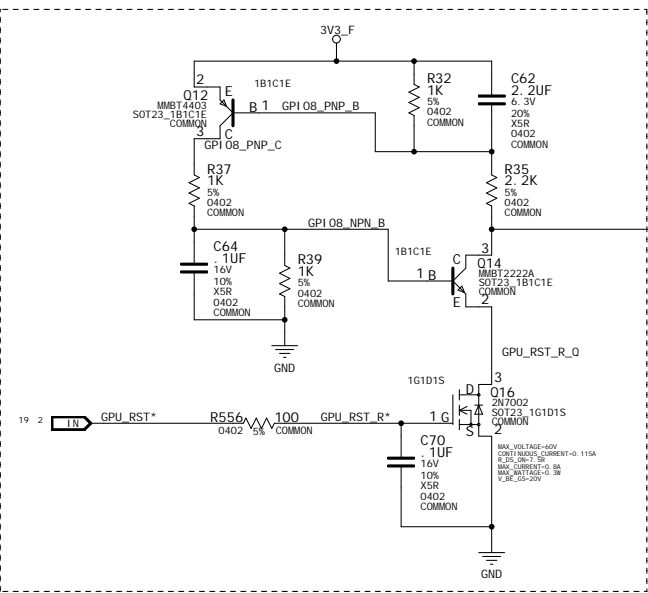
MECHANICAL AND THERMAL PARTS



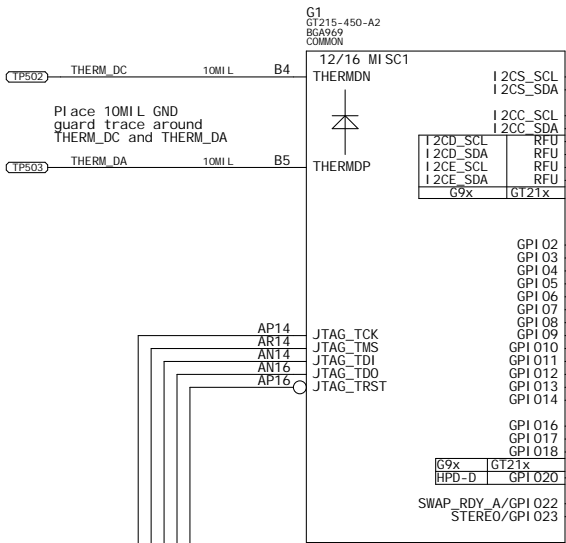
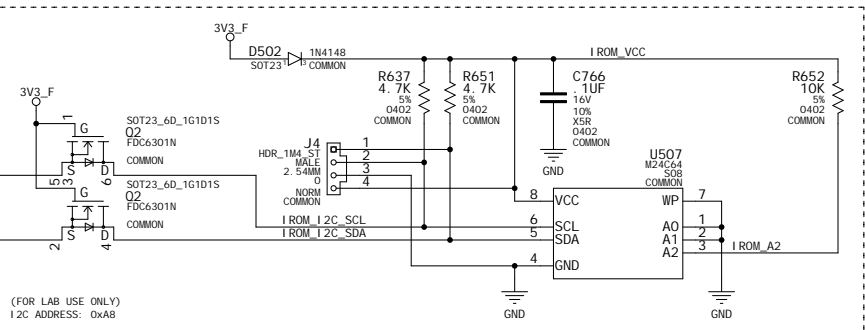
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17. Thermal Alert, Fan Control, GPIO, InfoROM, and JTAG

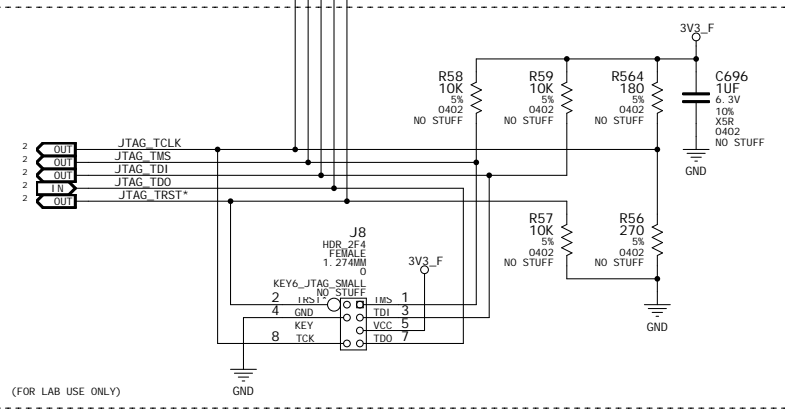
THERM ALERT LATCH



INFOROM



JTAG



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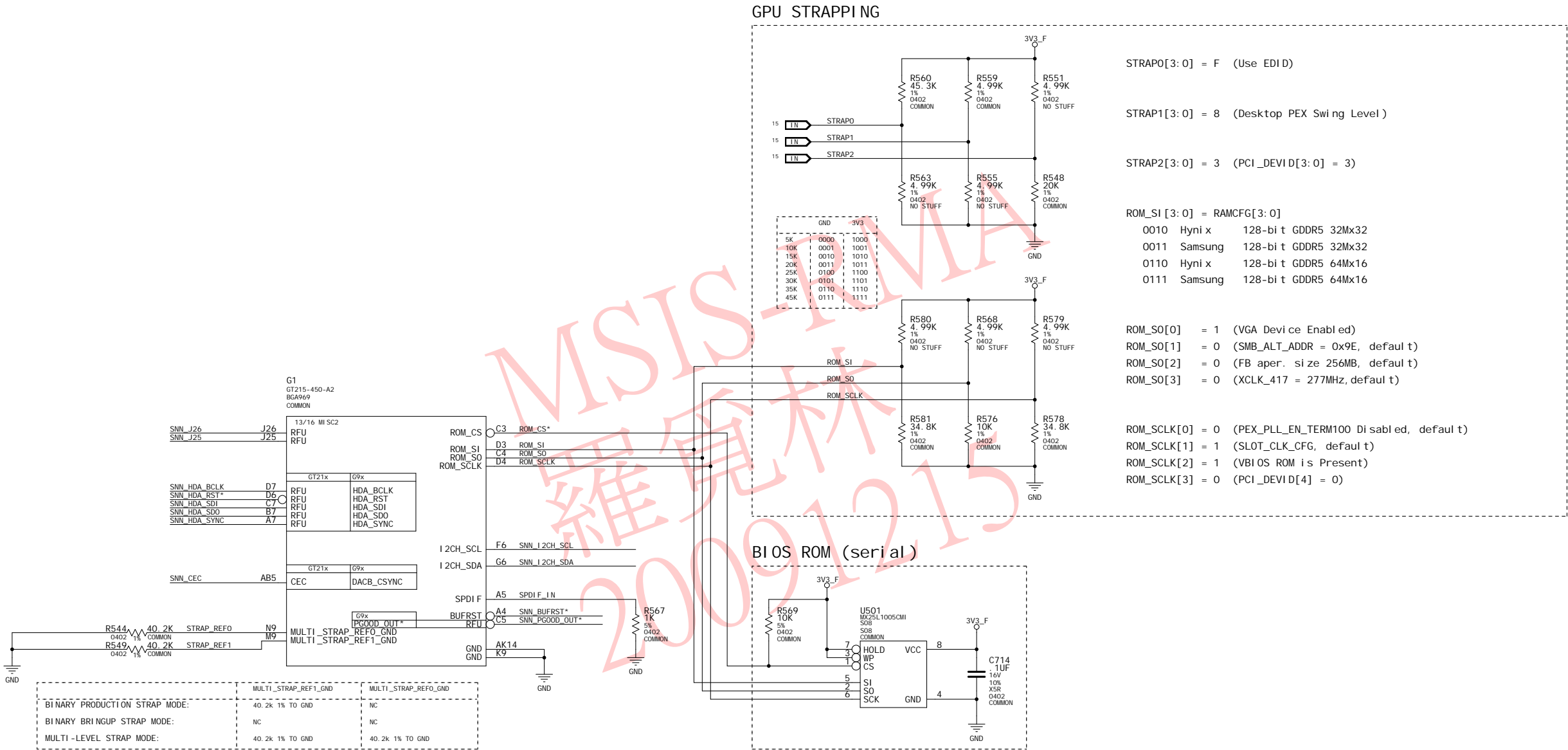


ASSEMBLY	GT215-450, 575/1443MHz 1024MB 64Mx16 BGA170 1800MHz GDDR5 DVI-I/VGA/HDMI
PAGE DETAIL	THERMAL ALERT, FAN CONTROL, GPIO, INFOROM, AND JTAG

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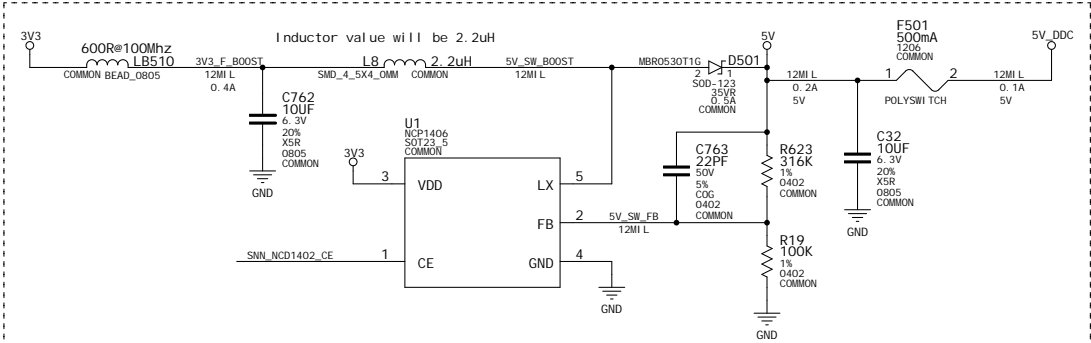
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18. Strapping and VBIOS ROM

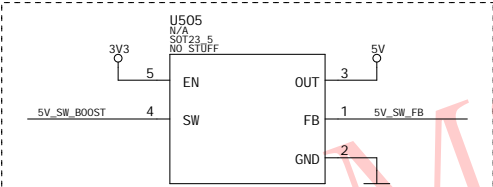


19. 5V, 5VDDC, 1FP_PLLVDD, 1FP_IOVDD, 3.3V Filter, and 12V Filter

5V BOOST REGULATOR

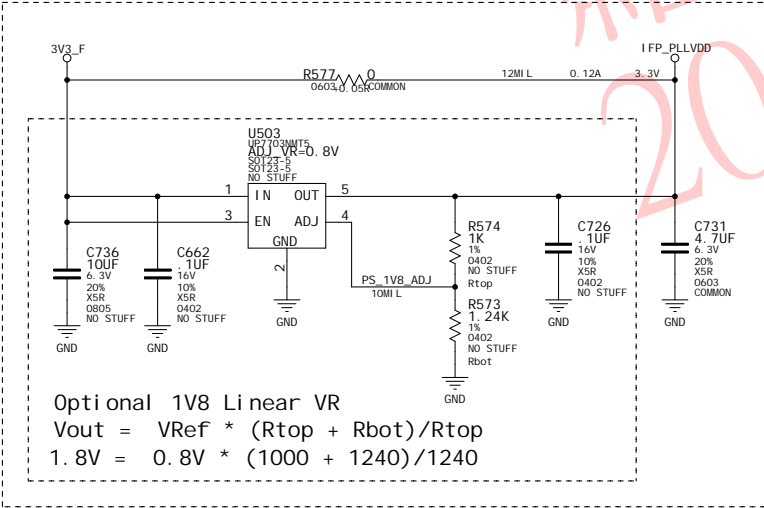


$$V_{out} = V_{Ref} * (1 + (R_{top}/R_{bot}))$$
$$5.0V = 1.19V * (1 + (316 / 100))$$



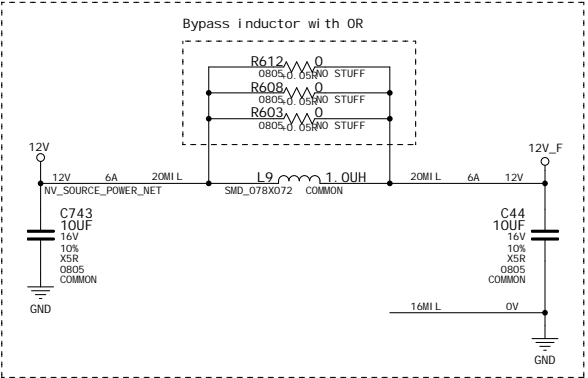
Alternate 5V Boost VR
Change inductor to 10uH

1FP_PLLVDD SUPPLY FOR 1FPC

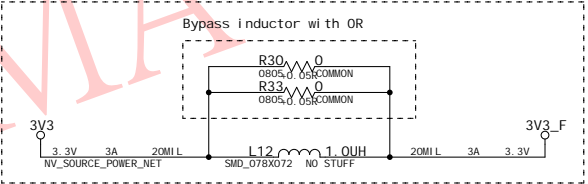


Optional 1V8 Linear VR
$$V_{out} = V_{Ref} * (R_{top} + R_{bot})/R_{top}$$
$$1.8V = 0.8V * (1000 + 1240)/1240$$

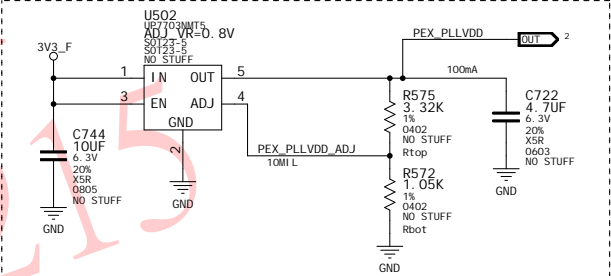
12V FILTER



3.3V FILTER

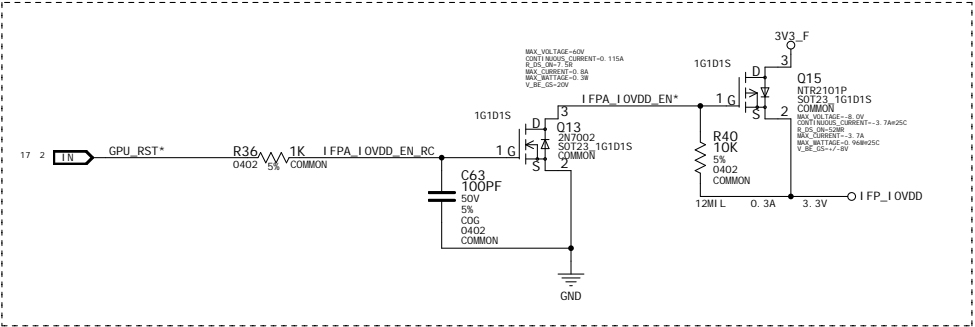


PEX_PLLVDD (OPTIONAL)



$$V_{out} = V_{Ref} * (R_{top} + R_{bot})/R_{top}$$
$$1.05 = 0.80 * (3.32 + 1.05)/1.05$$

1FP_IOVDD BACKDRIVE PREVENTION FOR 1FPA/B



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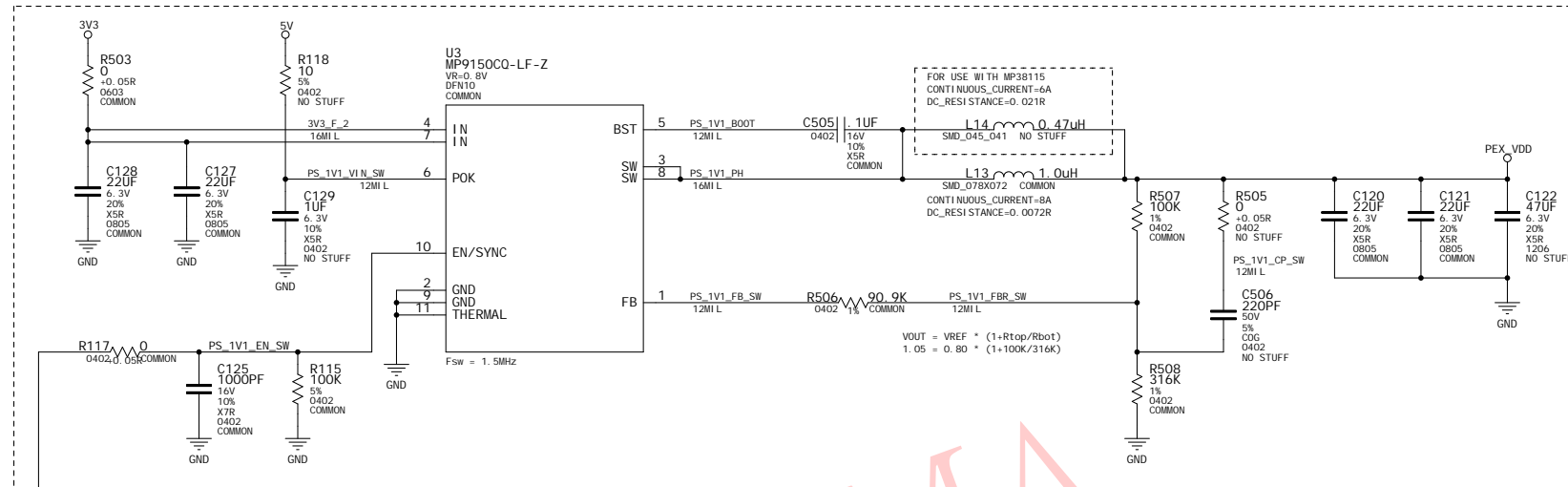


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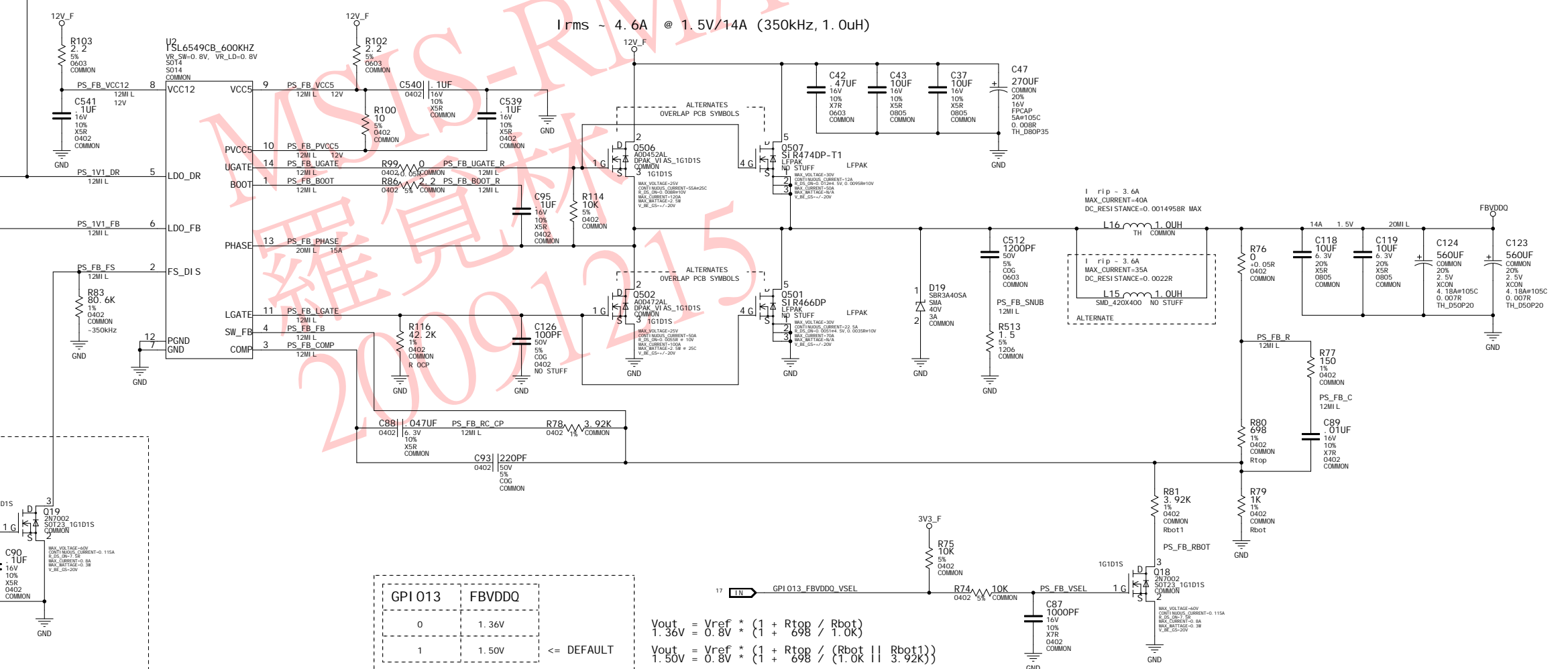
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FBVDDQ Power Supply 1.35-1.50V@14A



The schematic diagram illustrates the power supply section of the ADXL345 evaluation board. It shows the connection from a 5V regulator to the ADXL345 and the ADXL345 to the ADXL345 evaluation board. The schematic includes components like capacitors (C507, C503, C504, C502, C510, C509, C508, C501), resistors (R502, R501, R504), and the ADXL345 chip. The output voltage is calculated as $V_{OUT} = V_{REF} * (1 + R_{top}/R_{bot}) = 1.05 = 0.80 * (1 + 1.05/3.24)$.



GPI 013	FBVDDQ
0	1.36V
1	1.50V

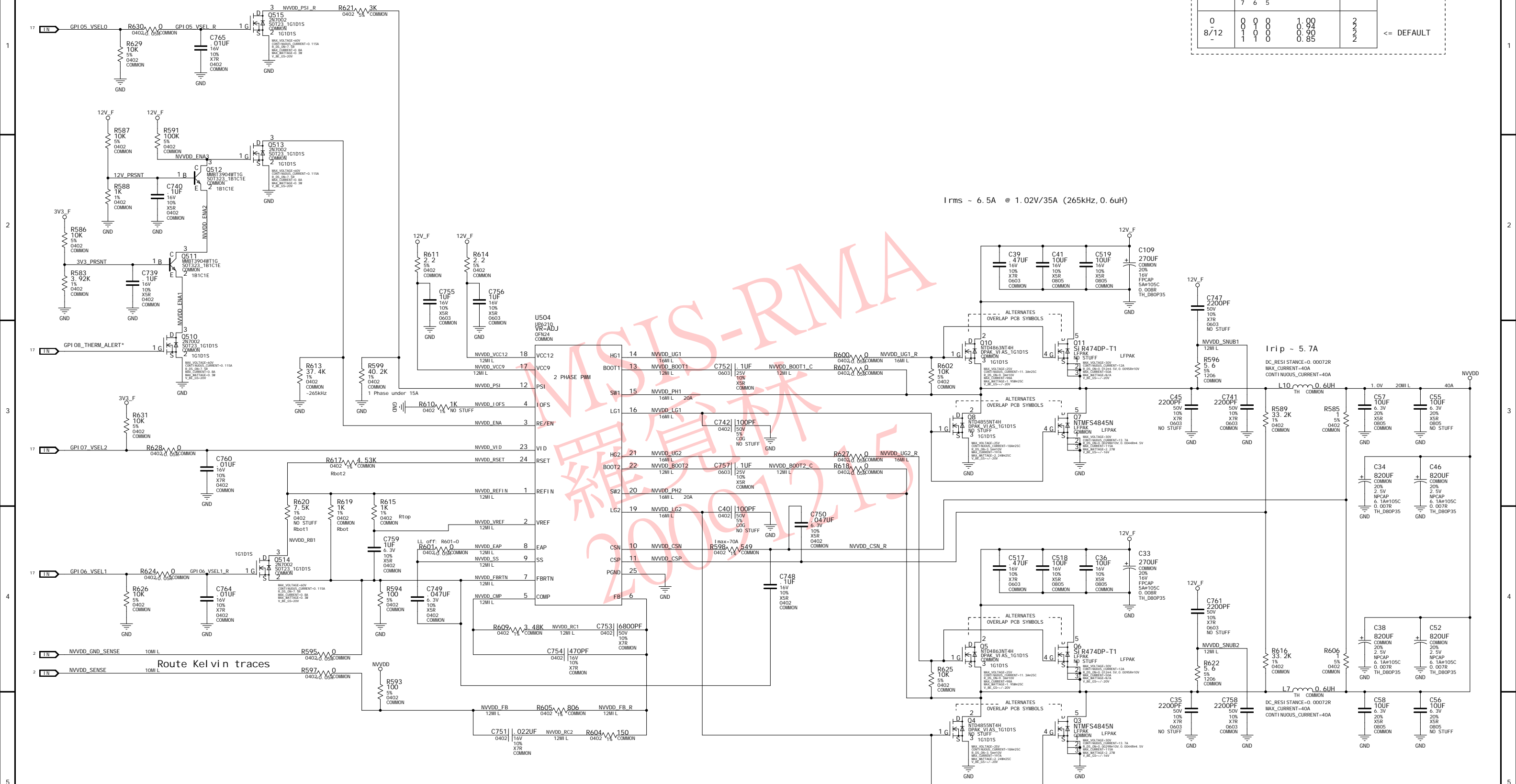
<= DEFAULT

$$\begin{aligned} V_{out} &= V_{ref} * (1 + R_{top} / R_{bot}) \\ 1.36V &= 0.8V * (1 + R_{698} / 1.0K) \\ V_{out} &= V_{ref} * (1 + R_{top} / (R_{bot} || R_{bot1})) \\ 1.50V &= 0.8V * (1 + R_{698} / (1.0K || 3.92K)) \end{aligned}$$

NVVDD Power Supply 35A@1.0V

PSTATE	GPI0 7 6 5	Vout#0-1 load	Phases
0	0 0 0	1.00	2
8/12	1 0 0	0.94	2
-	1 1 0	0.85	2

<= DEFAULT



Route Kelvin traces

ASSEMBLY	
PAGE DETAIL	NVDD DUAL-PHASE SWITCHER

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