P2131_A00

GK208 GDDR5 X16 64BIT
DVI-I/DVI-D/SlimVGA + HDMI/DP + VGA

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Page2: PCI Express

CN1
NONPHY-X16-124PIN
CON_X16

PLACE DECOUPLING CAPS NEAR PCI-E CONN FINGERS

12V_PEX: C668 1UF 16V 10% X5R 0603 COMMON; C667 10UF 16V 10% X5R 1206 COMMON; C48 0.1UF/NS 16V 10% X7R 0402 COMMON
3V3_PEX: C57 1UF 16V 10% X5R 0603 COMMON; C58 10UF/NS 6.3V 20% X5R 0805 COMMON; C666 0.1UF/NS 16V 10% X7R 0402 COMMON

12V_PEX	12V_PEX	12.0V	0.600MM TRUE	5.5A
3V3_PEX	3V3_PEX	3.3V	0.400MM TRUE	3A

B1	+12V	COMMON
B2	+12V	
A2	+12V	
A3	+12V	
B3	+12V/RSVD	
B8	+3V3	
A9	+3V3	
A10	+3V3	
B10	+3V3AUX	SNN_3V3_AUX
A1	PRSNT1	PEX_PRSNT*
B4, A4, B7, A12, B13, A15, B16, B18, A18	GND	
A20, B22, A24, B26, A28, B29, A31, B32	GND	END OF X1
A34, B36, A38, B40, A42, B44, A46, B47, B49, A49	GND	END OF X4
A51, B53, A54, B56, A58, B60, A62, B64, A66, B68, A70, B72, A74, B76, A78, B80, A82	GND	END OF X8
B81	PRSNT2	END OF X16

SMCLK	B5	PEX_SMCLK	R61 0 0402 +0.05% COMMON	R55 0 0402 +0.05% COMMON	I2CS_SCL	OUT 12		
SMDAT	B6	PEX_SMDAT			I2CS_SDA	BI 12		
PERST	A11	PEX_RST*	OUT 13					
REFCLK	A13	PEX_REFCLK	PEX_REFCLK	PEXGEN3_SIGNALS				
REFCLK	A14	PEX_REFCLK*	PEX_REFCLK	PEXGEN3_SIGNALS				
PERP0	A16	PEX_TX0	PEX_TX0	PEXGEN3_SIGNALS	C652 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX0	PEX_TX0
PERN0	A17	PEX_TX0*	PEX_TX0	PEXGEN3_SIGNALS	C651 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX0	PEX_TX0*
PETP0	B14	PEX_RX0	PEX_RX0	PEXGEN3_SIGNALS				
PETN0	B15	PEX_RX0*	PEX_RX0	PEXGEN3_SIGNALS				
PERP1	A21	PEX_TX1	PEX_TX1	PEXGEN3_SIGNALS	C646 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX1	PEX_TX1
PERN1	A22	PEX_TX1*	PEX_TX1	PEXGEN3_SIGNALS	C644 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX1	PEX_TX1*
PETP1	B19	PEX_RX1	PEX_RX1	PEXGEN3_SIGNALS				
PETN1	B20	PEX_RX1*	PEX_RX1	PEXGEN3_SIGNALS				
PERP2	A25	PEX_TX2	PEX_TX2	PEXGEN3_SIGNALS	C632 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX2	PEX_TX2
PERN2	A26	PEX_TX2*	PEX_TX2	PEXGEN3_SIGNALS	C628 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX2	PEX_TX2*
PETP2	B23	PEX_RX2	PEX_RX2	PEXGEN3_SIGNALS				
PETN2	B24	PEX_RX2*	PEX_RX2	PEXGEN3_SIGNALS				
PERP3	A29	PEX_TX3	PEX_TX3	PEXGEN3_SIGNALS	C622 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX3	PEX_TX3
PERN3	A30	PEX_TX3*	PEX_TX3	PEXGEN3_SIGNALS	C616 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX3	PEX_TX3*
PETP3	B27	PEX_RX3	PEX_RX3	PEXGEN3_SIGNALS				
PETN3	B28	PEX_RX3*	PEX_RX3	PEXGEN3_SIGNALS				
PERP4	A35	PEX_TX4	PEX_TX4	PEXGEN3_SIGNALS	C602 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX4	PEX_TX4
PERN4	A36	PEX_TX4*	PEX_TX4	PEXGEN3_SIGNALS	C600 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX4	PEX_TX4*
PETP4	B33	PEX_RX4	PEX_RX4	PEXGEN3_SIGNALS				
PETN4	B34	PEX_RX4*	PEX_RX4	PEXGEN3_SIGNALS				
PERP5	A39	PEX_TX5	PEX_TX5	PEXGEN3_SIGNALS	C589 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX5	PEX_TX5
PERN5	A40	PEX_TX5*	PEX_TX5	PEXGEN3_SIGNALS	C586 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX5	PEX_TX5*
PETP5	B37	PEX_RX5	PEX_RX5	PEXGEN3_SIGNALS				
PETN5	B38	PEX_RX5*	PEX_RX5	PEXGEN3_SIGNALS				
PERP6	A43	PEX_TX6	PEX_TX6	PEXGEN3_SIGNALS	C576 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX6	PEX_TX6
PERN6	A44	PEX_TX6*	PEX_TX6	PEXGEN3_SIGNALS	C572 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX6	PEX_TX6*
PETP6	B41	PEX_RX6	PEX_RX6	PEXGEN3_SIGNALS				
PETN6	B42	PEX_RX6*	PEX_RX6	PEXGEN3_SIGNALS				
PERP7	A47	PEX_TX7	PEX_TX7	PEXGEN3_SIGNALS	C563 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX7	PEX_TX7
PERN7	A48	PEX_TX7*	PEX_TX7	PEXGEN3_SIGNALS	C562 0.22UF 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX7	PEX_TX7*
PETP7	B45	PEX_RX7	PEX_RX7	PEXGEN3_SIGNALS				
PETN7	B46	PEX_RX7*	PEX_RX7	PEXGEN3_SIGNALS				
PERP8	A52	PEX_TX8	PEX_TX8	PEXGEN3_SIGNALS	C560 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX8	PEX_TX8
PERN8	A53	PEX_TX8*	PEX_TX8	PEXGEN3_SIGNALS	C559 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX8	PEX_TX8*
PETP8	B50	PEX_RX8	PEX_RX8	PEXGEN3_SIGNALS				
PETN8	B51	PEX_RX8*	PEX_RX8	PEXGEN3_SIGNALS				
PERP9	A56	PEX_TX9	PEX_TX9	PEXGEN3_SIGNALS	C556 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX9	PEX_TX9
PERN9	A57	PEX_TX9*	PEX_TX9	PEXGEN3_SIGNALS	C553 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX9	PEX_TX9*
PETP9	B54	PEX_RX9	PEX_RX9	PEXGEN3_SIGNALS				
PETN9	B55	PEX_RX9*	PEX_RX9	PEXGEN3_SIGNALS				
PERP10	A60	PEX_TX10	PEX_TX10	PEXGEN3_SIGNALS	C550 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX10	PEX_TX10
PERN10	A61	PEX_TX10*	PEX_TX10	PEXGEN3_SIGNALS	C549 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX10	PEX_TX10*
PETP10	B58	PEX_RX10	PEX_RX10	PEXGEN3_SIGNALS				
PETN10	B59	PEX_RX10*	PEX_RX10	PEXGEN3_SIGNALS				
PERP11	A64	PEX_TX11	PEX_TX11	PEXGEN3_SIGNALS	C547 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX11	PEX_TX11
PERN11	A65	PEX_TX11*	PEX_TX11	PEXGEN3_SIGNALS	C546 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX11	PEX_TX11*
PETP11	B62	PEX_RX11	PEX_RX11	PEXGEN3_SIGNALS				
PETN11	B63	PEX_RX11*	PEX_RX11	PEXGEN3_SIGNALS				
PERP12	A68	PEX_TX12	PEX_TX12	PEXGEN3_SIGNALS	C544 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX12	PEX_TX12
PERN12	A69	PEX_TX12*	PEX_TX12	PEXGEN3_SIGNALS	C543 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX12	PEX_TX12*
PETP12	B66	PEX_RX12	PEX_RX12	PEXGEN3_SIGNALS				
PETN12	B67	PEX_RX12*	PEX_RX12	PEXGEN3_SIGNALS				
PERP13	A72	PEX_TX13	PEX_TX13	PEXGEN3_SIGNALS	C541 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX13	PEX_TX13
PERN13	A73	PEX_TX13*	PEX_TX13	PEXGEN3_SIGNALS	C540 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX13	PEX_TX13*
PETP13	B70	PEX_RX13	PEX_RX13	PEXGEN3_SIGNALS				
PETN13	B71	PEX_RX13*	PEX_RX13	PEXGEN3_SIGNALS				
PERP14	A76	PEX_TX14	PEX_TX14	PEXGEN3_SIGNALS	C538 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX14	PEX_TX14
PERN14	A77	PEX_TX14*	PEX_TX14	PEXGEN3_SIGNALS	C535 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX14	PEX_TX14*
PETP14	B74	PEX_RX14	PEX_RX14	PEXGEN3_SIGNALS				
PETN14	B75	PEX_RX14*	PEX_RX14	PEXGEN3_SIGNALS				
PERP15	A80	PEX_TX15	PEX_TX15	PEXGEN3_SIGNALS	C530 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX15	PEX_TX15
PERN15	A81	PEX_TX15*	PEX_TX15	PEXGEN3_SIGNALS	C528 0.22UF/NS 0402 6.3V COMMON	PEXGEN3_SIGNALS	PEX_TX15	PEX_TX15*
PETP15	B78	PEX_RX15	PEX_RX15	PEXGEN3_SIGNALS				
PETN15	B79	PEX_RX15*	PEX_RX15	PEXGEN3_SIGNALS				

G1A
BGA595
COMMON

1/14 PCI_EXPRESS

	GK208/GF117/GF119	
PEX_WAKE	NC	SNN_PEX_WAKE* AB6
PEX_RST		AC7
PEX_CLKREQ		SNN_PEX_CLKREQ* AC6
PEX_REFCLK		AE8
PEX_REFCLK		AD8
PEX_TX0		AC9
PEX_TX0		AB9
PEX_RX0		AG6
PEX_RX0		AG7
PEX_TX1		AB10
PEX_TX1		AC10
PEX_RX1		AF7
PEX_RX1		AE7
PEX_TX2		AD11
PEX_TX2		AC11
PEX_RX2		AE9
PEX_RX2		AF9
PEX_TX3		AC12
PEX_TX3		AB12
PEX_RX3		AG9
PEX_RX3		AG10
PEX_TX4		AB13
PEX_TX4		AC13
PEX_RX4		AF10
PEX_RX4		AE10
PEX_TX5		AD14
PEX_TX5		AC14
PEX_RX5		AE12
PEX_RX5		AF12
PEX_TX6		AC15
PEX_TX6		AB15
PEX_RX6		AG12
PEX_RX6		AG13
PEX_TX7		AB16
PEX_TX7		AC16
PEX_RX7		AF13
PEX_RX7		AE13
PEX_TX8	NC	AD17
PEX_TX8	NC	AC17
PEX_RX8	NC	AE15
PEX_RX8	NC	AF15
PEX_TX9	NC	AC18
PEX_TX9	NC	AB18
PEX_RX9	NC	AG15
PEX_RX9	NC	AG16
PEX_TX10	NC	AB19
PEX_TX10	NC	AC19
PEX_RX10	NC	AF16
PEX_RX10	NC	AE16
PEX_TX11	NC	AD20
PEX_TX11	NC	AC20
PEX_RX11	NC	AE18
PEX_RX11	NC	AF18
PEX_TX12	NC	AC21
PEX_TX12	NC	AB21
PEX_RX12	NC	AG18
PEX_RX12	NC	AG19
PEX_TX13	NC	AD23
PEX_TX13	NC	AE23
PEX_RX13	NC	AF19
PEX_RX13	NC	AE19
PEX_TX14	NC	AF24
PEX_TX14	NC	AE24
PEX_RX14	NC	AE21
PEX_RX14	NC	AF21
PEX_TX15	NC	AG24
PEX_TX15	NC	AG25
PEX_RX15	NC	AG21
PEX_RX15	NC	AG22
GF119	GF117 GK208	

PEX_IOVDD: AA22, AB23, AC24, AD25, AE26, AE27
PEX_IOVDDQ: AA10, AA12, AA13, AA16, AA18, AA19, AA20, AA21, AB22, AC23, AD24, AE25, AF26, AF27

PLACE NEAR BALLS: C593 1UF 6.3V 10% X5R 0402 COMMON; C585 1UF 6.3V 10% X5R 0402 COMMON; C591 4.7UF/NS 6.3V 20% X5R 0603 COMMON
PLACE NEAR BGA: C613 4.7UF 6.3V 20% X5R 0603 COMMON; C94 10UF 6.3V 20% X5R 0805 COMMON; C555 10UF 6.3V 20% X5R 0805 COMMON; C95 22UF 6.3V 20% X5R 0805 COMMON; C611 22UF 6.3V 20% X5R 0805 COMMON
PEX_VDD

PLACE NEAR BALLS: C579 1UF 6.3V 10% X5R 0402 COMMON; C605 1UF 6.3V 10% X5R 0402 COMMON; C591 4.7UF 6.3V 20% X5R 0603 COMMON
PLACE NEAR BGA: C92 4.7UF/NS 6.3V 20% X5R 0603 COMMON; C618 10UF 6.3V 20% X5R 0805 COMMON; C93 10UF 6.3V 20% X5R 0805 COMMON; C574 22UF 6.3V 20% X5R 0805 COMMON; C612 22UF 6.3V 20% X5R 0805 COMMON
PEX_VDD

Place 10uF and 22uF in midway between GPU and Power Supply

PEX_PLL_HVDD: AA8, AA9
PEX_SVDD_3V3: AB8
3V3_PEX
0.189A
C607 0.1UF 16V 10% X7R 0402 COMMON
C603 4.7UF 6.3V 20% X5R 0603 COMMON
C630 4.7UF/NS 6.3V 20% X5R 0603 COMMON
PLACE NEAR BALLS
PLACE NEAR BGA

VDD_SENSE: F2 — NET: NVVDD_SENSE — NV_NETCLASS: GENERIC_SEZ1 — OUT 17
GND_SENSE: F1 — SNN_GND_SENSE

PEX_TSTCLK_OUT: AF22 PEX_PLL_CLK_OUT — PEXGEN3_SIGNALS — R136 200/NS 0402 1% COMMON
PEX_TSTCLK_OUT: AE22 PEX_PLL_CLK_OUT* — PEXGEN3_SIGNALS

PEX_PLLVDD: AA14 PEX_PLLVDD, AA15 PEX_PLLVDD — 0.30D 0.130A — PLACE NEAR BALLS 1.05V
C582 0.1UF 16V 10% X7R 0402 COMMON
C564 1UF 6.3V 10% X5R 0402 COMMON
PLACE NEAR BGA
C558 4.7UF 6.3V 20% X5R 0603 COMMON
C557 10UF/NS 10V 20% X5R 0805 COMMON
R529 0 0603 +0.05W COMMON
PEX_VDD

TESTMODE: AD9 GPU_TESTMODE — R531 10K 0402 1% COMMON

PEX_TERMP: AF25 PEX_TERMP — R528 2.49K 0402 1% COMMON

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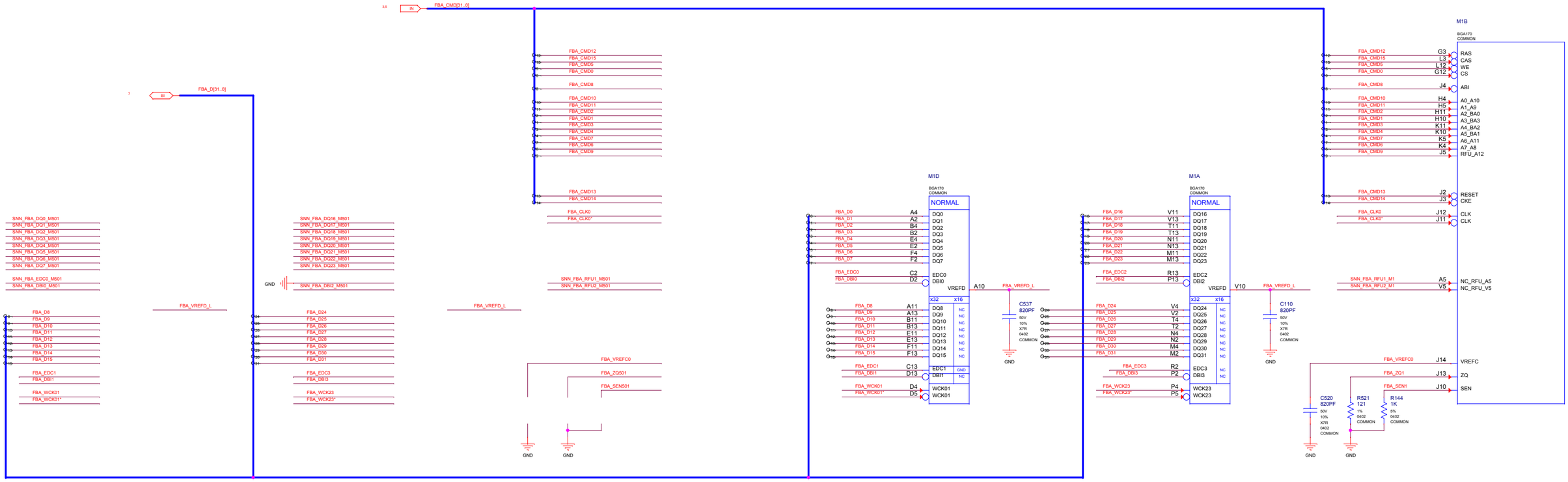
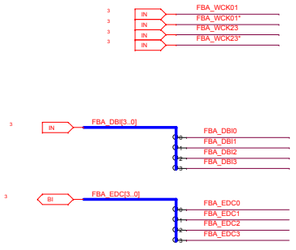
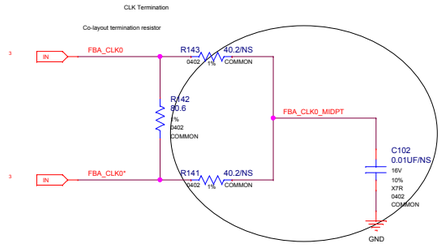
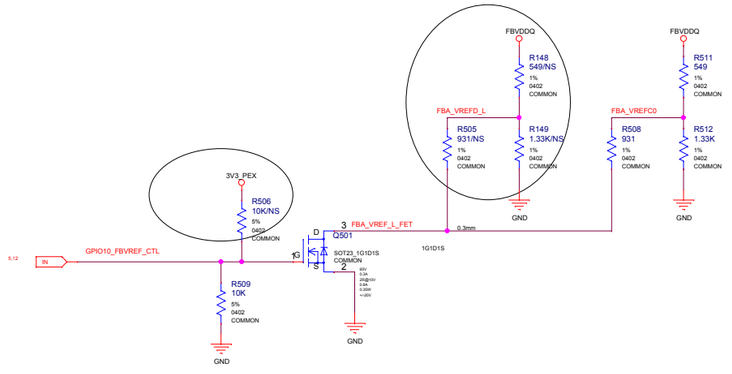


CMD	31..0	63..32
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	A8*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		A8*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*







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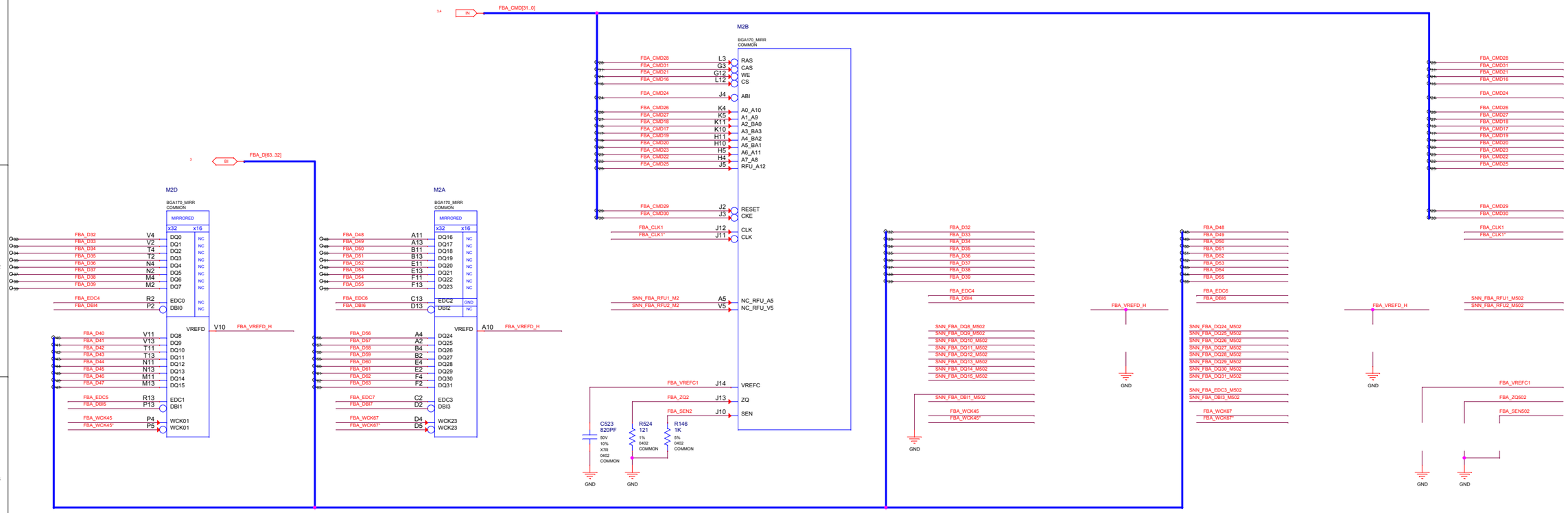
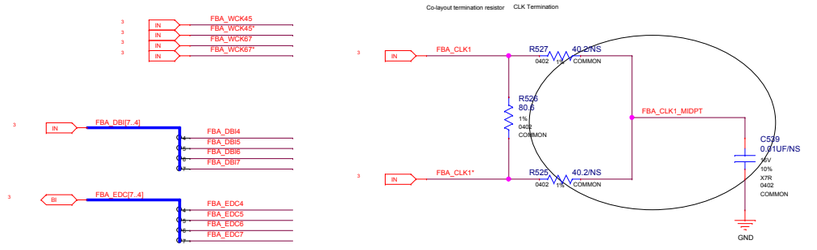
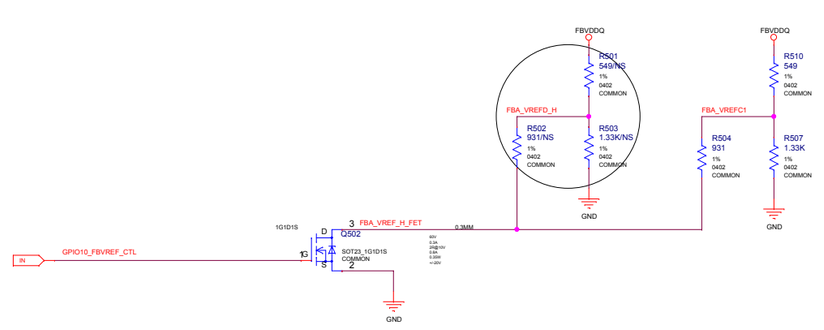
Page5: FBA Partition 63..32







CMD	31..0	63..32
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*

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ASSEMBLY	
PAGE DETAIL	FB Partition A bits 63..32

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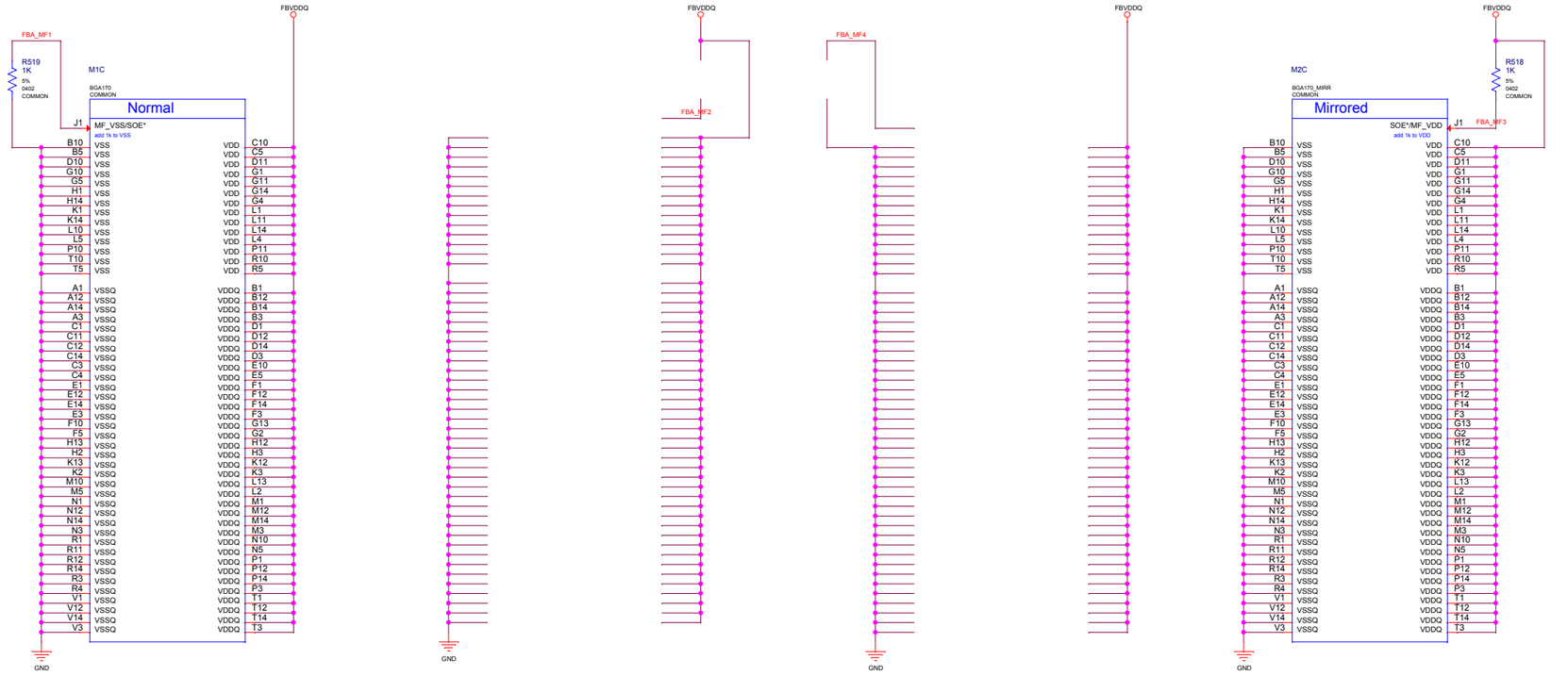
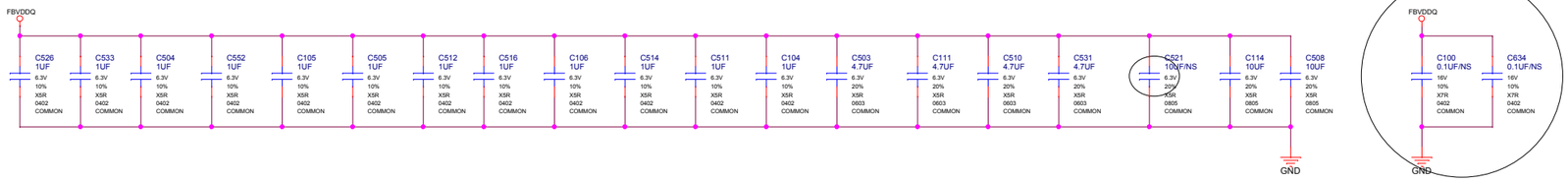
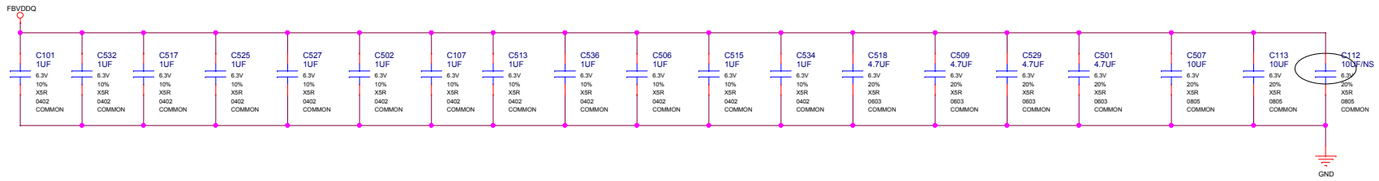
Page6: DECOUPLING for DRAMs



DECOUPLING FOR M1 and M501 DEVICE



DECOUPLING FOR M2 and M502 DEVICE



PLACE 1uF CAPS CLOSEST TO THE MEMORY DEVICES

PLACE LARGER CAPACITORS SLIGHTLY FARTHER AWAY

ASSEMBLY	
PAGE DETAIL	DECOUPLING for DRAMs

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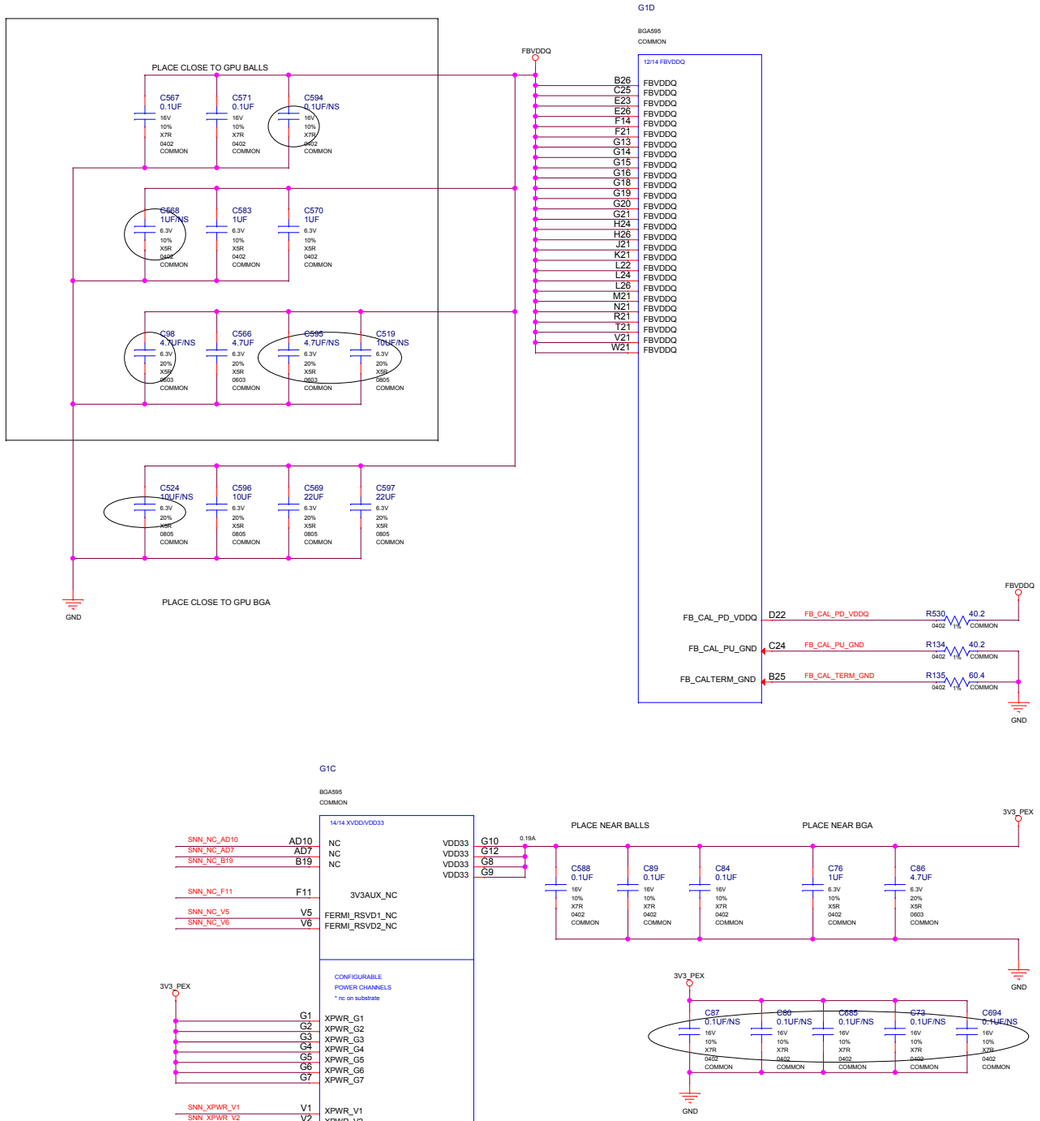
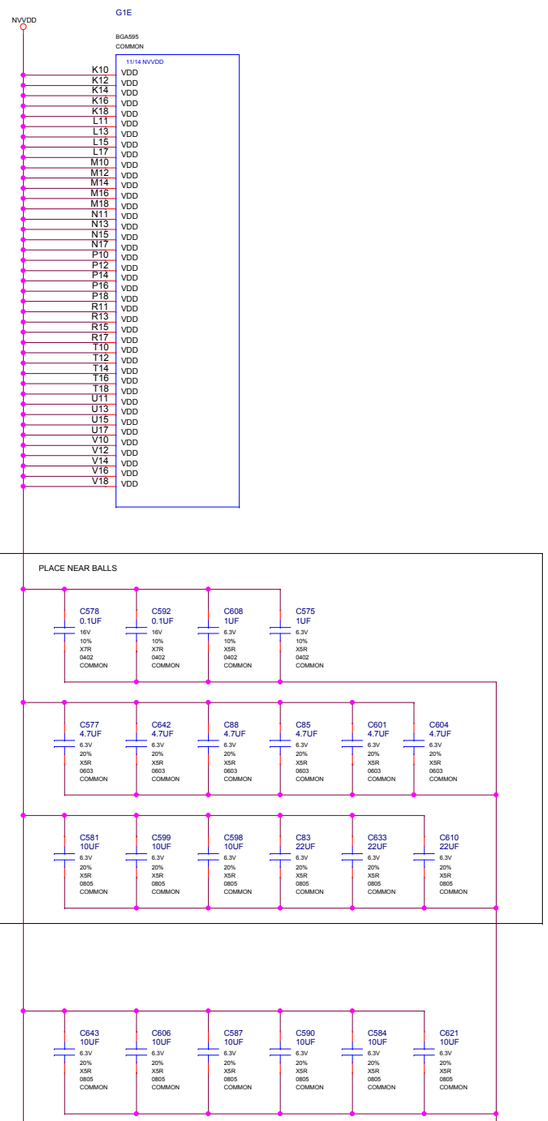
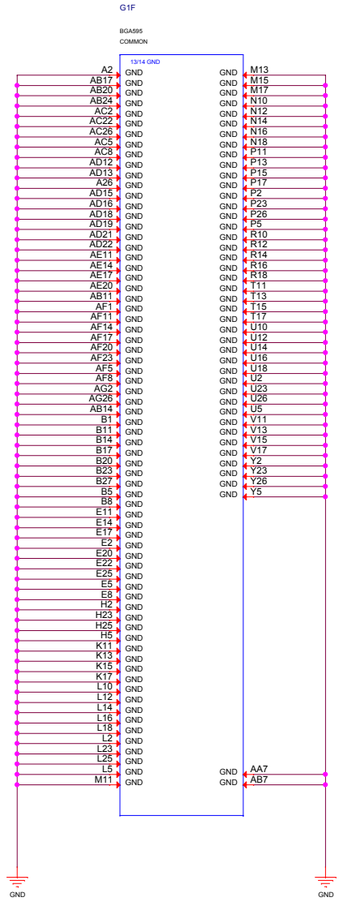
Page7: POWER/DECOUPLING: NVVDD,FBVDDQ,VDD33,GND







** XPWR pins are configurable.

These pins are not connected on the substrate.

Therefore, XPWR pins can be assigned as needed,

to improve Top layer routing, power delivery.

Connection will be modified according to Layout.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	POWER/DECOUPLING: NVVDD, FBVDDQ, VDD33, GND

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Page8: IFPAB TMDS DUAL LINK

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPA/B TMDS DUAL LINK

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Page9: IFPC HDMI/DP,DP_PWR

Fused DP_PWR, STUFF FOR DP SKU

Resistor for discharging DP POSCAP

DP SKU PLACE BACKSIDE

Hotplug Detection

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPC HDMI/DP, DP_PWR

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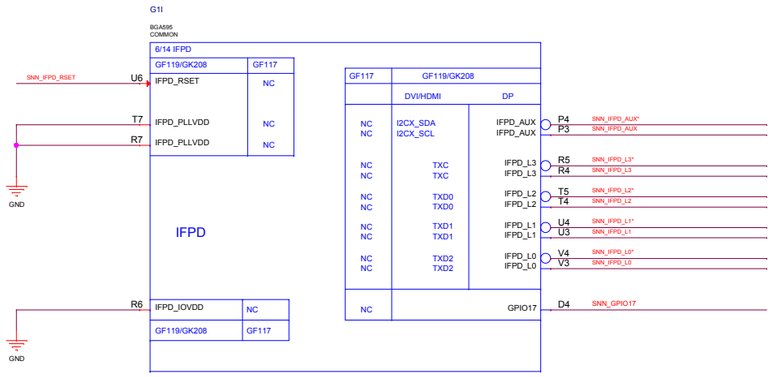
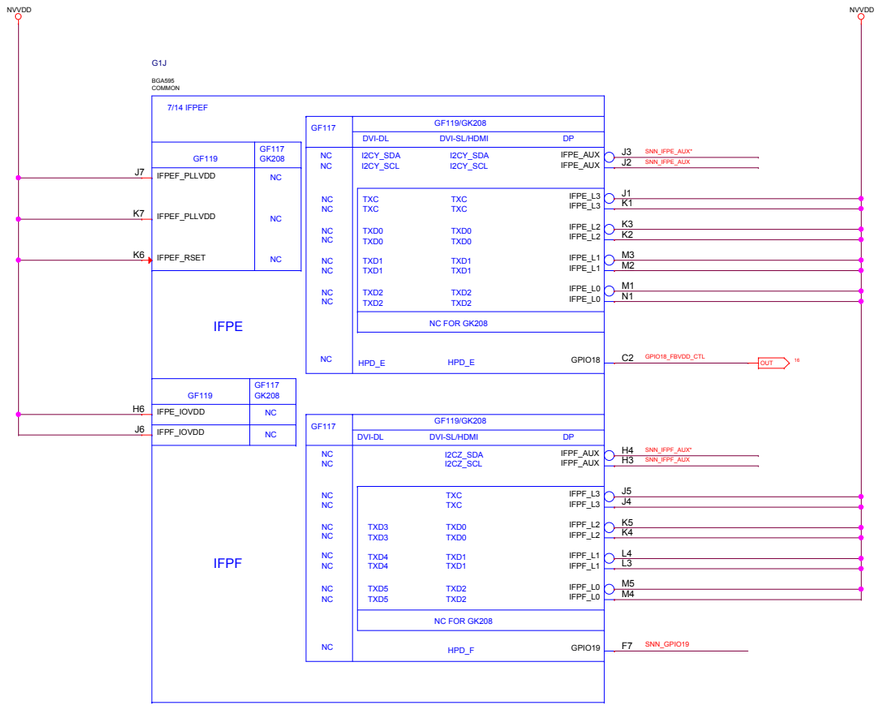
Page10: UNUSED IFPD,IFPE & IFPF





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	UNUSED IFPD, IFPE & IFPF

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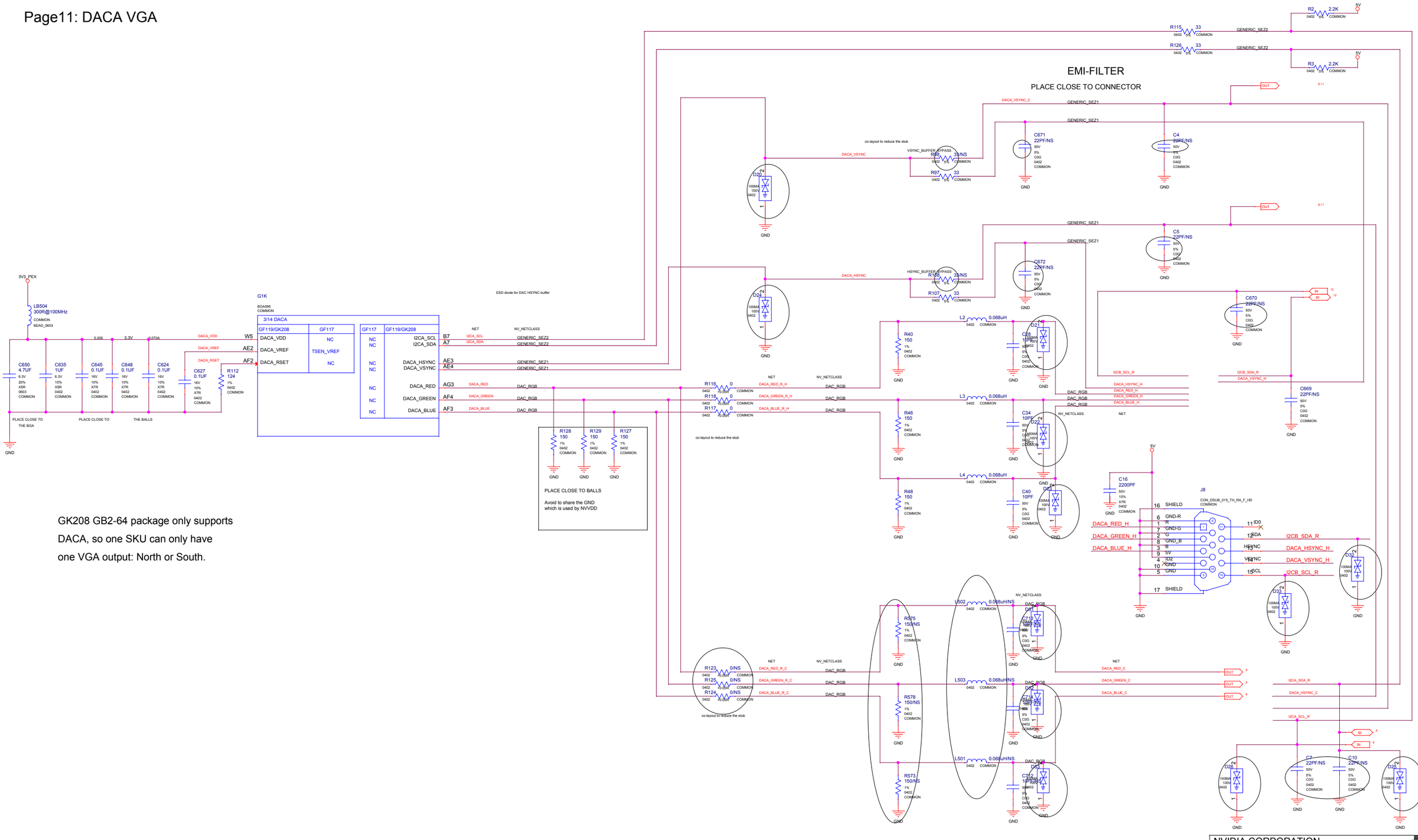
Page11: DACA VGA

GK208 GB2-64 package only supports DACA, so one SKU can only have one VGA output: North or South.



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DACA VGA

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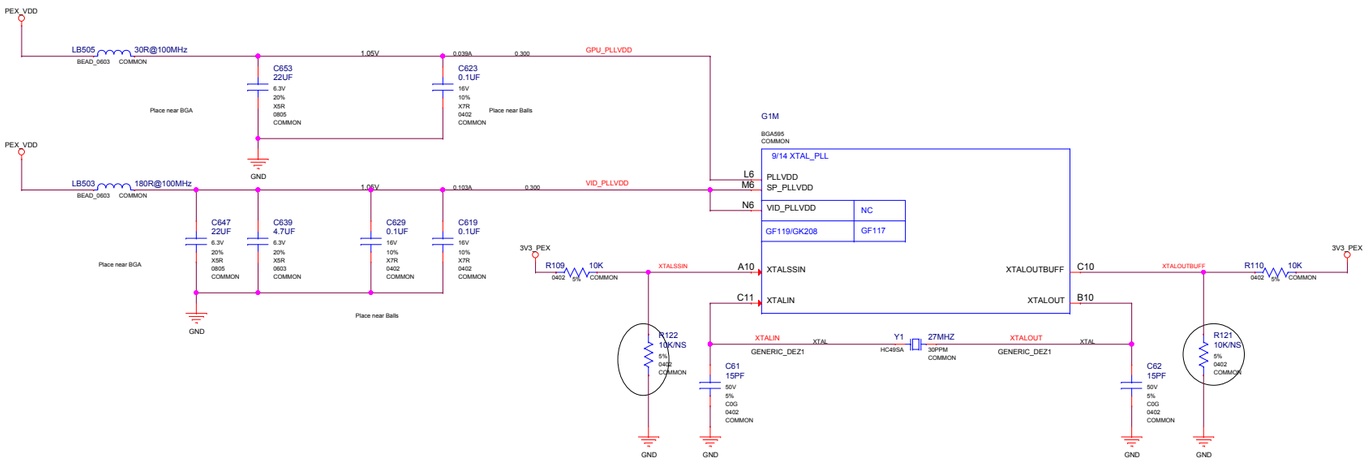
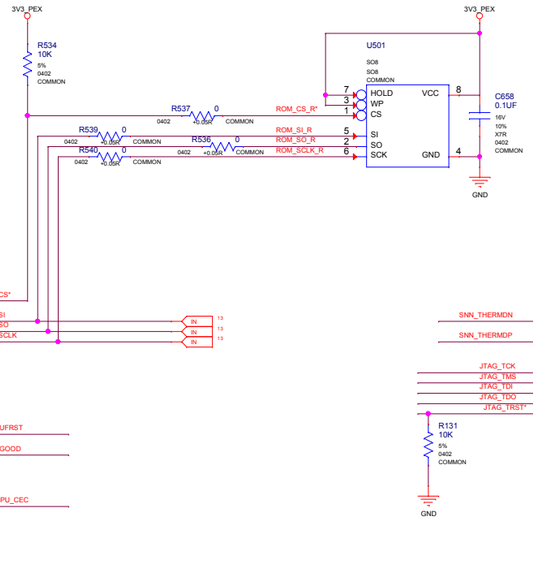
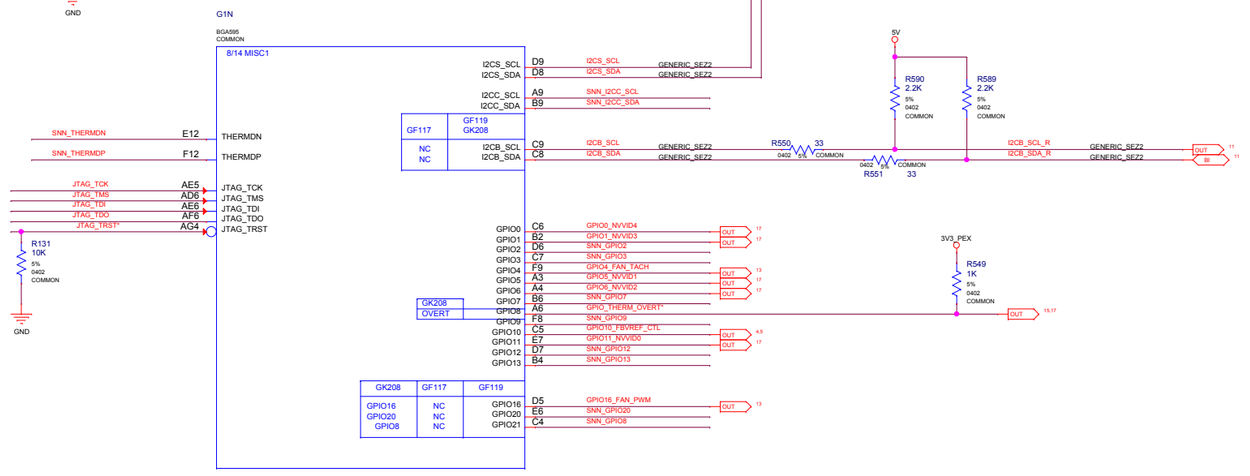
Page12: BIOS,JTAG,GPIO & XTAL

Smart Fan

XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	BIOS, JTAG, GPIO & XTAL

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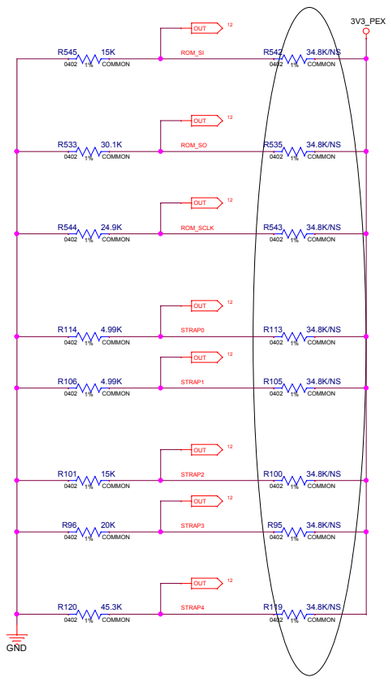
Page13: PCI-E Reset, STRAPS & FAN

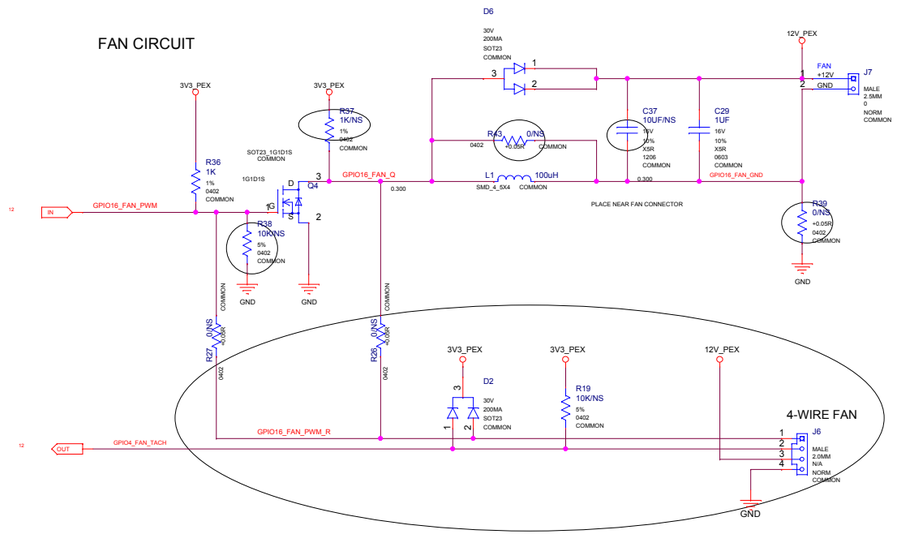
Multilevel Straps			
0000	5.1K to GND	1000	5.1K to VCC
0001	10K to GND	1001	10K to VCC
0010	15K to GND	1010	15K to VCC
0011	20K to GND	1011	20K to VCC
0100	24.9K to GND	1100	24.9K to VCC
0101	30.1K to GND	1101	30.1K to VCC
0110	34.8K to GND	1110	34.8K to VCC
0111	45.3K to GND	1111	45.3K to VCC

GK208 Straps



Bit	Signal	Values				
03:	RAMCFG[3]					ROM_SI
02:	RAMCFG[2]	0000	Reserved			
		0001	128Mx16 GDDR5 X16 64bit Elpida			
01:	RAMCFG[1]	0010	128Mx16 GDDR5 X16 64bit Hynix A-die			
		0011	128Mx16 GDDR5 X16 64bit Samsung D-die			
00:	RAMCFG[0]					
03:	FB[1]	01	128MB			ROM_SO
		10	256MB			
02:	FB[0]					
01:	SMB_ALT_ADDR	0	DISABLED	1	ENABLED	
00:	VGA_DEVICE	0	DISABLED	1	ENABLED	
03:	PCI_DEVID_EXT	SKU0	0	SKU1	TBD	ROM_SCLK
02:	SUB_VENDOR	0	NO_BIOS	1	BIOS	
01:	PCI_DEVID_EXT_BIT5	SKU0	0	SKU1	TBD	
00:	PEX_PLL_EN_TERM100	0	DISABLED	1	ENABLED	
03:	USER[3]	0000	INIT			Strap0
02:	USER[2]					
01:	USER[1]					
00:	USER[0]					
03:	3GIO_PADCFG_LUT_ADR[3]	0000	DSKTOP_DEFAULT	1000	DSKTOP_HTHRS	Strap1
		0001	MOBILE_DEFAULT	1001	MOBILE_HTHRS_NAMP	
02:	3GIO_PADCFG_LUT_ADR[2]	0010	MOBILE_NTHRS_LLAMP	1010	MOBILE_HTHRS_LLAMP	
		0011	MOBILE_NTHRS_LAMP	1011	MOBILE_HTHRS_LAMP	
01:	3GIO_PADCFG_LUT_ADR[1]	0100	MOBILE_NTHRS_HAMP	1100	MOBILE_HTHRS_HAMP	
		0101	MOBILE_NTHRS_HHAMP	1101	MOBILE_HTHRS_HHAMP	
00:	3GIO_PADCFG_LUT_ADR[0]	0110	MOBILE_NTHRS_HHHAMP	1110	MOBILE_HTHRS_HHHAMP	
		0111	MOBILE_NTHRS_HHHHAMP	1111	MOBILE_HTHRS_HHHHAMP	
03:	PCI_DEVID[3]	SKU0	0010			Strap2
02:	PCI_DEVID[2]					
01:	PCI_DEVID[1]					
00:	PCI_DEVID[0]	SKU1	TBD			
03:	SOR3_EXPOSED	0	DISABLED	1	ENABLED	Strap3
02:	SOR2_EXPOSED	0	DISABLED	1	ENABLED	
01:	SOR1_EXPOSED	0	DISABLED	1	ENABLED	
00:	SOR0_EXPOSED	0	DISABLED	1	ENABLED	
02:	PCIE_SPEED_CHANGE_GEN3	0	DISABLED	1	ENABLED	Strap4
01:	PCIE_MAX_SPEED	0	GEN1	1	GEN23	
00:	DP_PLL_VDD_3V3	0	USE1V8	1	USE3V3	

FAN CIRCUIT



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PCI-E Reset, STRAPS & FAN

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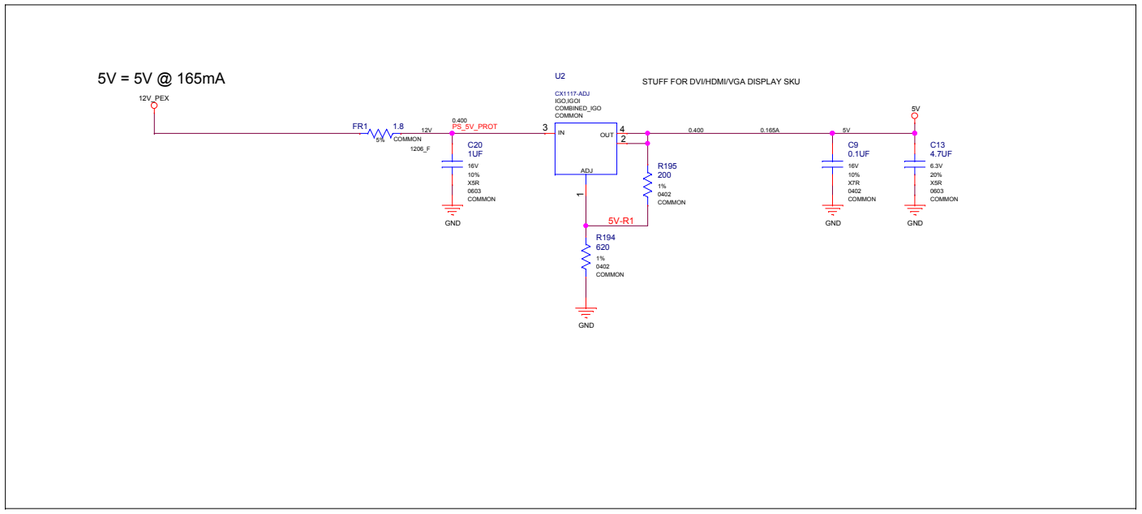
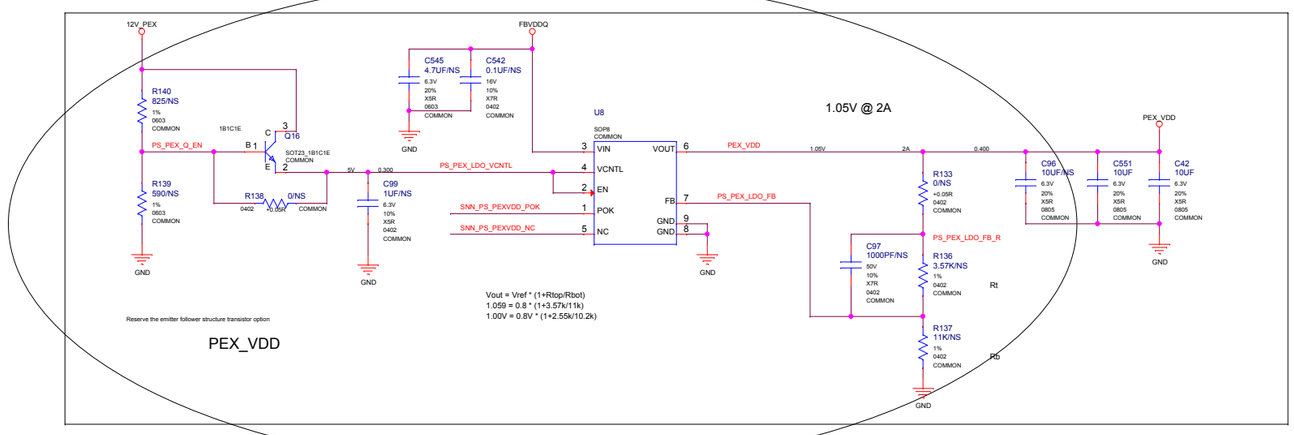
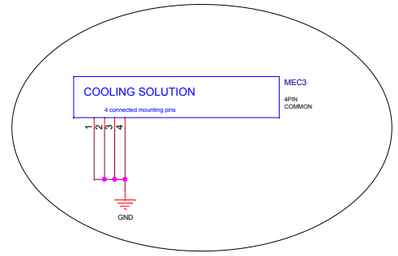
Page14: PS 5V,PEXVDD







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 5V, PEXVDD

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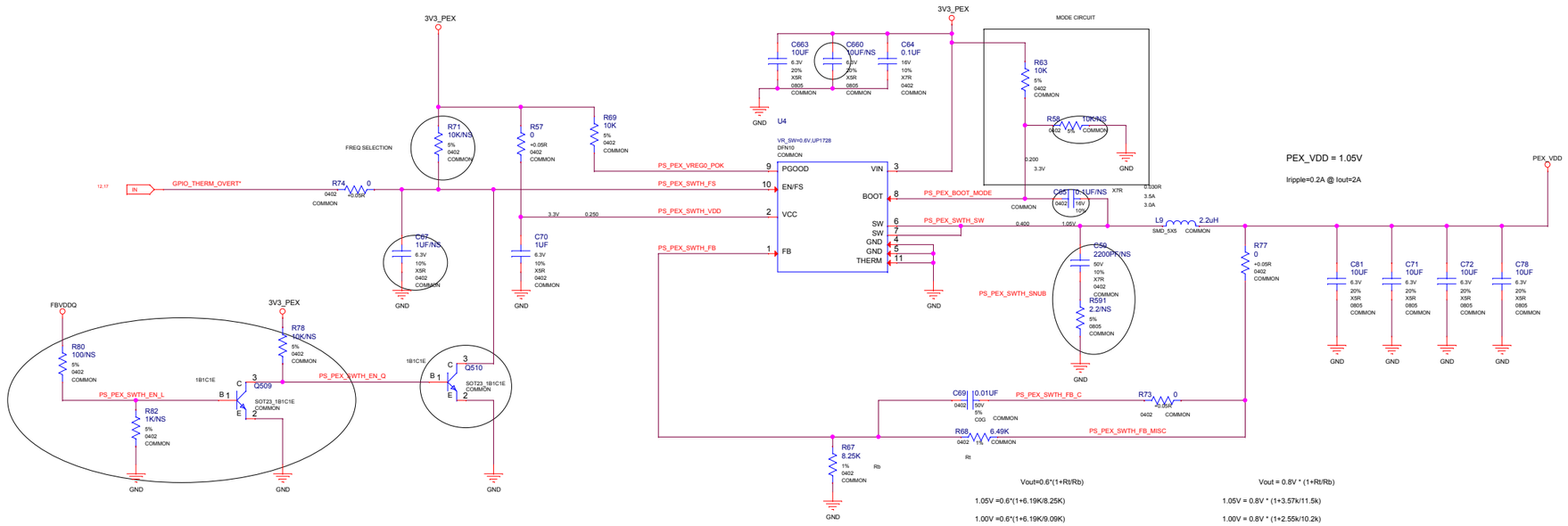
Page15:PEX_VDD Open VR Type0



OPEN VREG TYPE-0

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PEX_VDD: Open VR Type0

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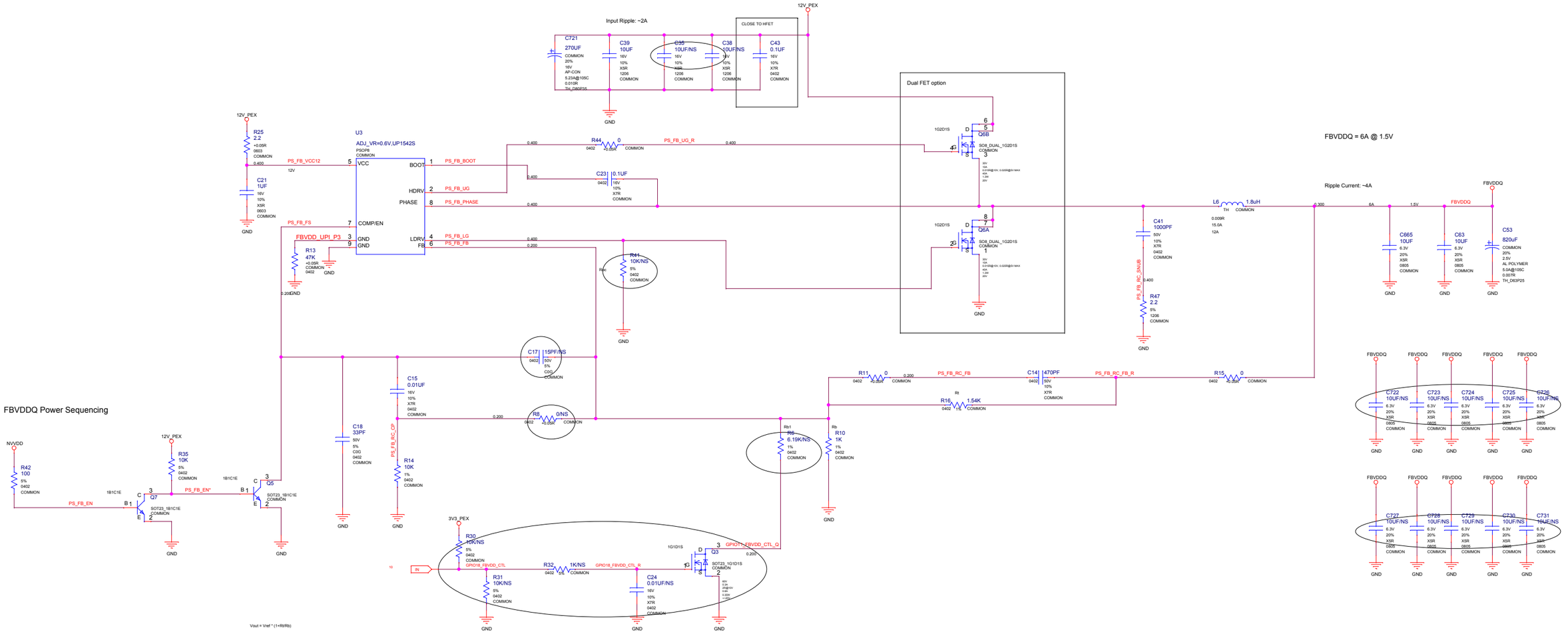
Page16: PS FBVDDQ



Vout = Vref * (1+Rt/(Rb1//Rb)

GPIO[9]	FBVDDQ@GPU
0	1.35V
BOOT --> 1	1.5V

WILL FINE TUNE BASED ON SENSE POINT

Vout = Vref * (1+Rt/Rb)

Vref=0.6V: 1.5V = 0.6V * (1+1.87k/1.5K/6.19k)
1.35V = 0.6V * (1+1.87k/1.5K)

Vref=0.8V: 1.5V = 0.8V * (1+1.37K/2k//7.15K)
1.35V = 0.8V * (1+1.37k/2K)

Vref=0.5V: 1.5V = 0.5V * (1+1.87k/1.1K/6.19K)
1.35V = 0.5V * (1+1.87k/1.1K)

PS	Fosc	Vref	Tol
315-0601-000: APW8720	300kHz	0.5V	1%
316-0096-000: RT8120AGSP	300kHz	0.6V	1.5%
315-0644-000: EM5303A	300kHz	0.6V	1.5%
316-0095-000: RT8120AGS	300kHz	0.6V	1.5%
315-0638-000: APW8725A	300kHz	0.8V	1%
316-0071-000: RT8101GSP	300kHz	0.8V	1%
315-0526-000: APW7120	300kHz	0.8V	1.5%
315-0533-000: NCP1579	300kHz	0.8V	2%
315-0529-000: FP6326	300kHz	0.8V	2%

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: FBVDDQ

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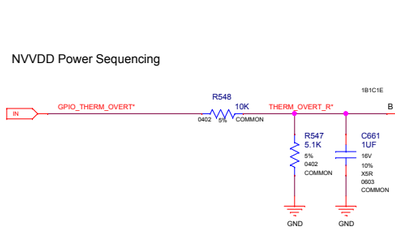
Page17: PS NVVDD

NVVDD Power Sequencing



Vout = Vref * (1+Rtop/Rbot)

VID[4:0]	NVVDD
00000	0.775OV
00001	0.7875V
00010	0.8000V
00011	0.8125V
00100	0.8250V
00101	0.8375V
00110	0.8500V
00111	0.8625V
01000	0.8750V
01001	0.8875V
DEFAULT — 01010	0.9000V
01011	0.9125V
01100	0.9250V
01101	0.9375V
01110	0.9500V
01111	0.9625V
10000	0.9750V
10001	0.9875V
10010	1.0000V
10011	1.0125V
10100	1.0250V
10101	1.0375V
10110	1.0500V
10111	1.0625V
11000	1.0750V
11001	1.0875V
11010	1.1000V
11011	1.1125V
11100	1.1250V
11101	1.1375V
11110	1.1500V
11111	1.1625V

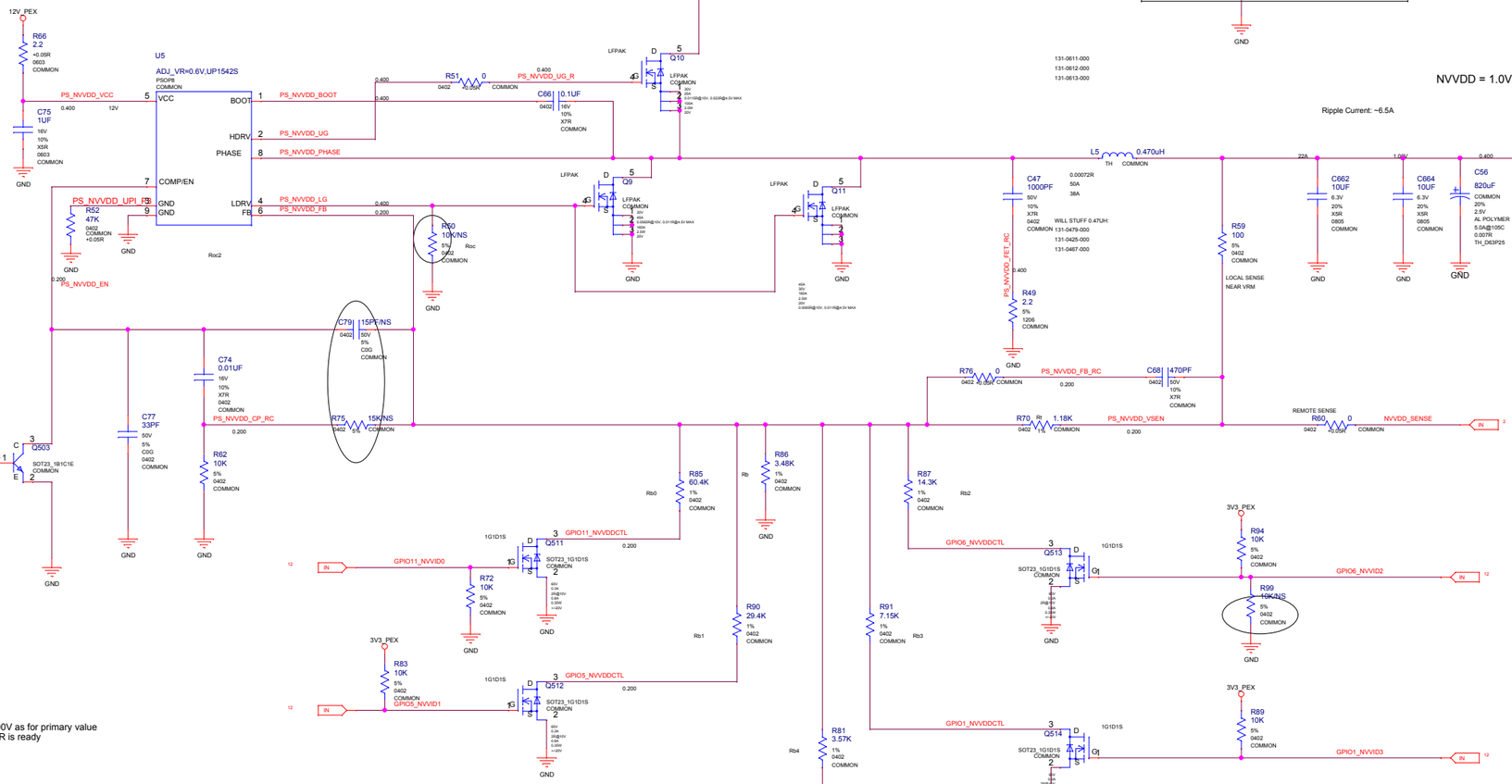
Bootup Voltage set to 0.9000V as for primary value
It will be changed when POR is ready

PWM Freq Vref(V)
RT8120AGS: 300kHz, 0.6V
EM5303AGE: 300kHz, 0.6V
RT8105GS: 300kHz, 0.8V
RT8101: 300kHz, 0.8V
APW7165AKAE: 300kHz, 0.8V
APW7129KE: 300kHz, 0.8V
NCP1579DR2G: 275kHz, 0.8V

Vout = Vref * (1+Rb/Rb)
0.775V = 0.5V * (1+1.54/2.8k)
0.776V = 0.6V * (1+1.18k/4.02k)

Vref	Rb1	Rb2	Rb3	Rb4	Rb5
0.5V	61.9k	30.9k	15.4k	7.68k	3.83k
0.6V	60.4k	29.4k	14.3k	7.15k	3.57k

values for Rb1, Rb2
Rb3, Rb4 and Rb5
will be calculated based
on the needed voltages



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD

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