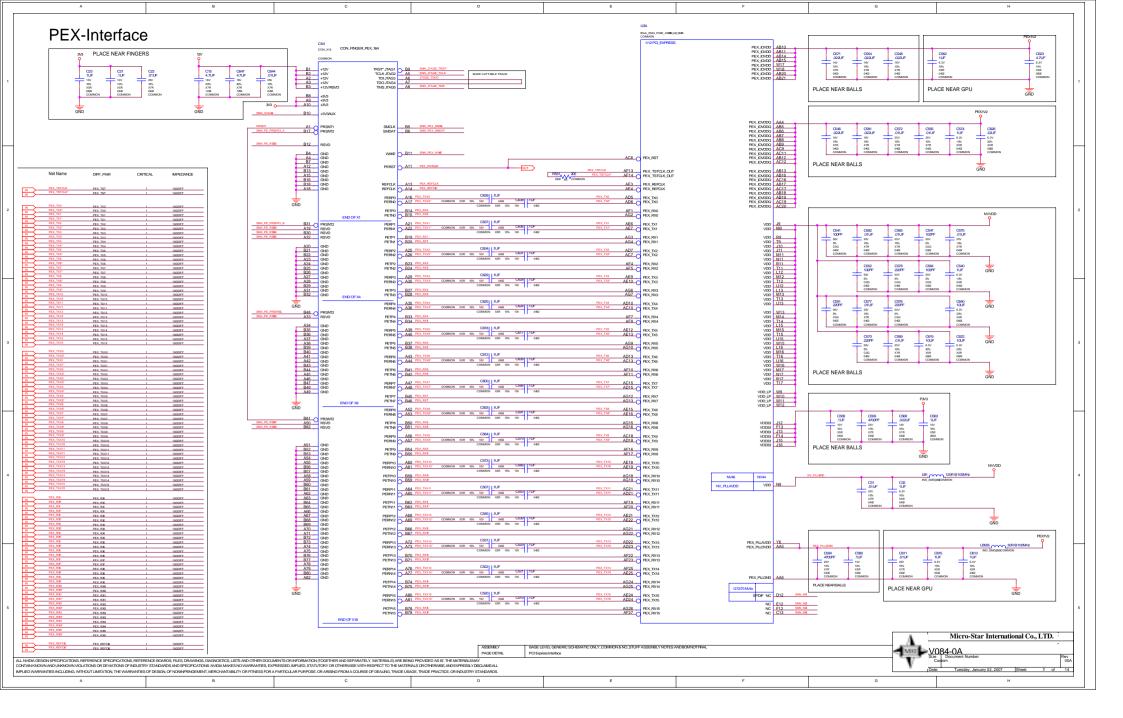
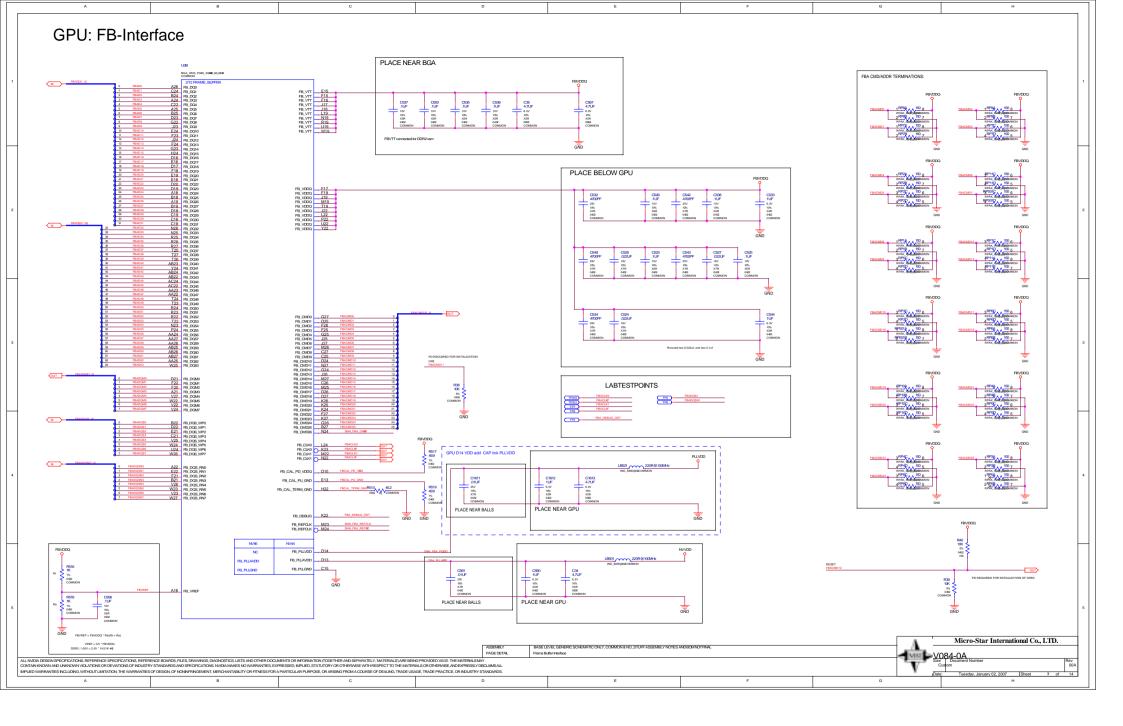
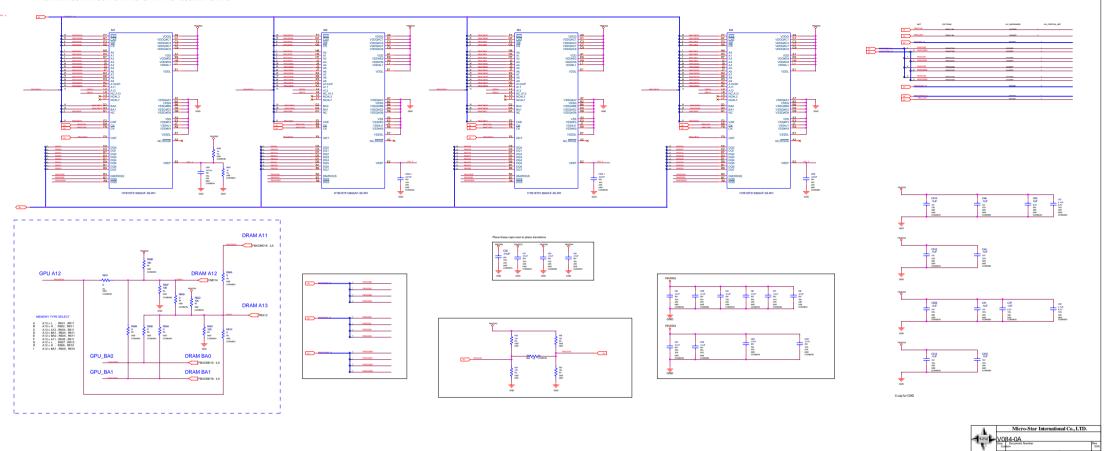
V084: G72, DDR2 MEMORY 32Mx8 base on V056 - 1.0 Page1: V084 Overview Page2: PCI Express Interface Page3: Frame Buffer Interface Page4: Memory 1st bank 0..31 Page5: Memory 1st bank 32..63 Page6: DACA Page7: DACB Page8: DACB,MINIDIN Page9: TMDS Interface Page10: MIOA, MIOB Interface, LPC-ROM Page11: STRAPS, Mechanical Parts Page12: XTAL, GPIO, BIOS, FAN, JTAG, THERMAL Page13: PowerSupplyI: NVVDD, PLLVDD Page14: PowerSupplyII: 5V, DDC5V, F3V3,FBVDDQ M/FN 600 10381 0000000 600 10381 0001400 600 10381 0001400 600 10381 0001400 600 10381 0000400 4UNDEFNED Micro-Star International Co., LTD. ALL INIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FLES, DRAWNINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS: THE MATERIAL SIA CONTINUOMINATO LINEAD VINITATION OF REALIZED STANDARD AND STREET TO THE WITHOUT STANDARD AND STREET AND STANDARD AND STREET AND STANDARD AND STREET AND STANDARD AND STREET AND STANDARD AN





Memory Bit 0..31
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TOMEMORY



Memory Bit 32..63
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TOMEMORY

