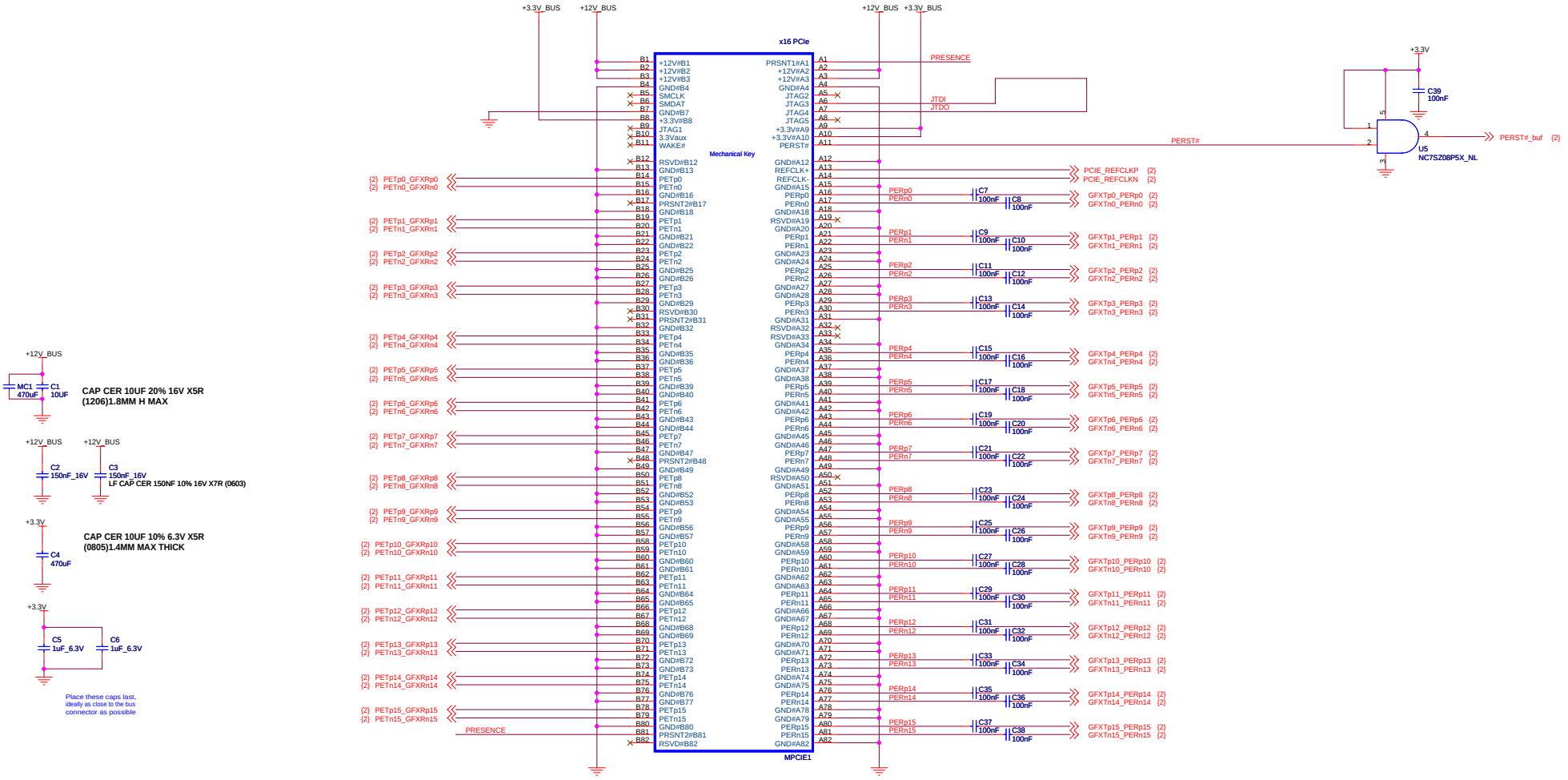
REAL

PCI-EXPRESS EDGE CONNECTOR

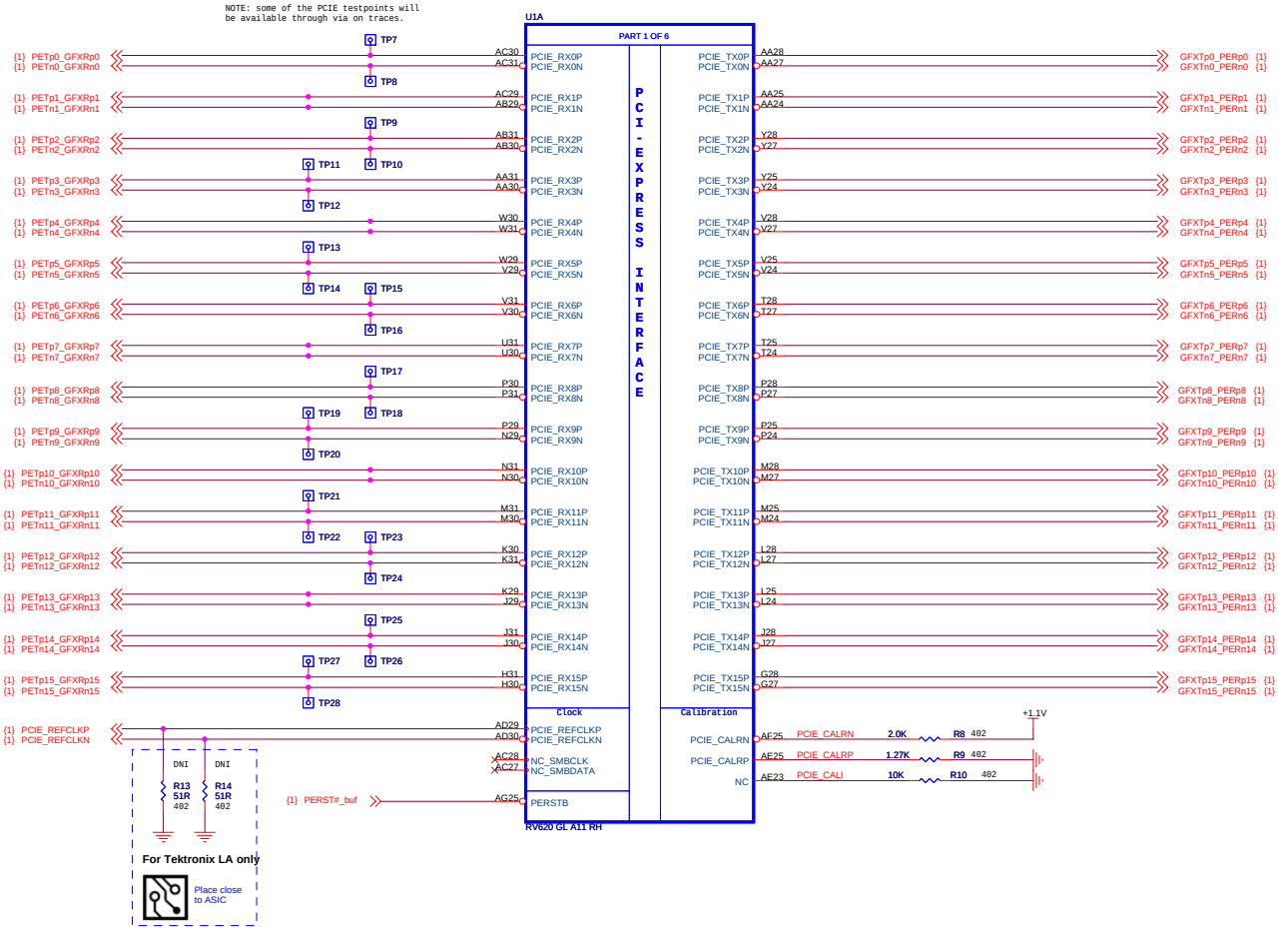


SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Thursday, May 15, 2008
Rev	17
Sheet	1 of 20
Title	RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No.	105-B350xx-00C



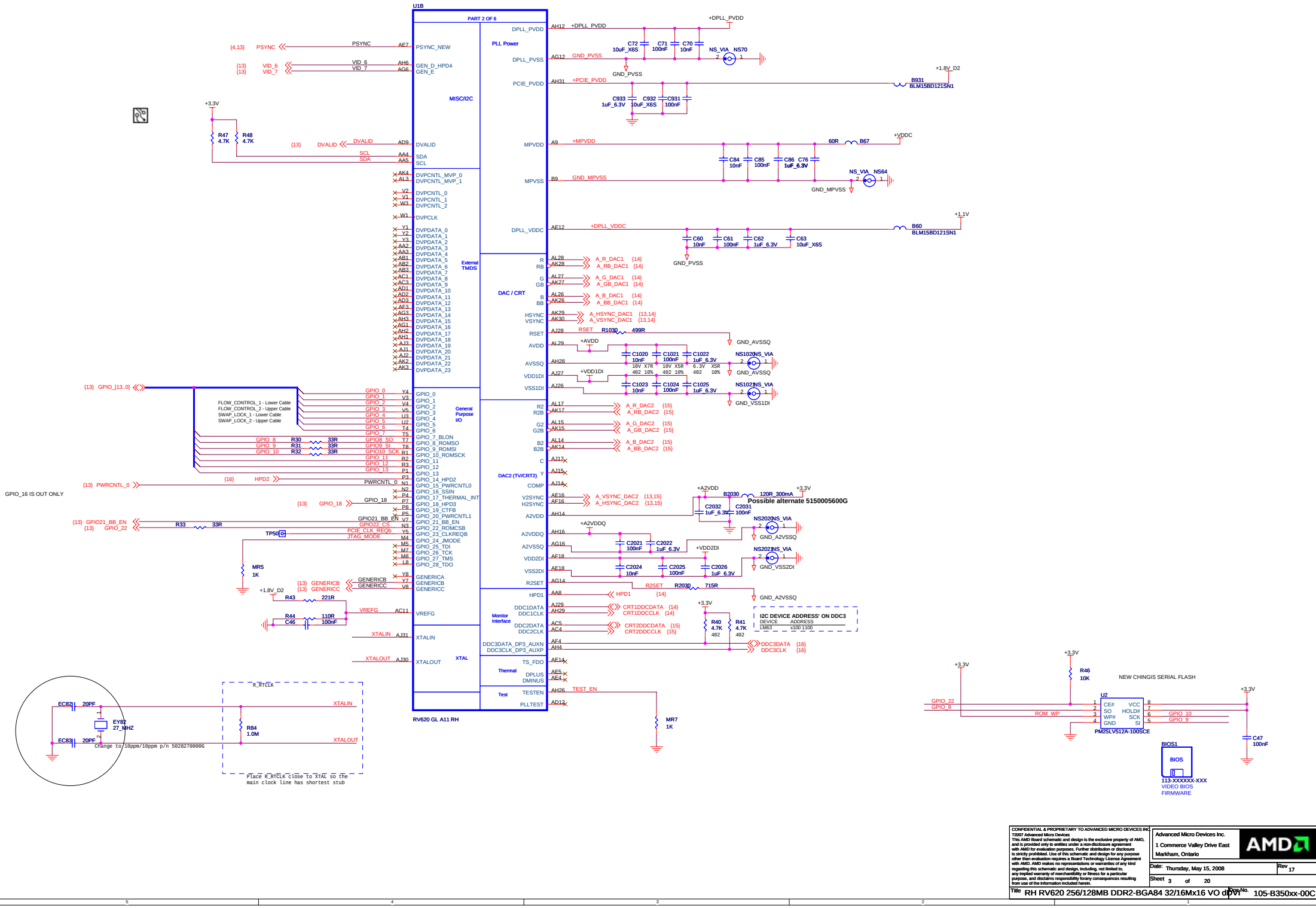
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, May 15, 2008 Rev 17

Sheet 2 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

Doc No. 105-B350xx-00C



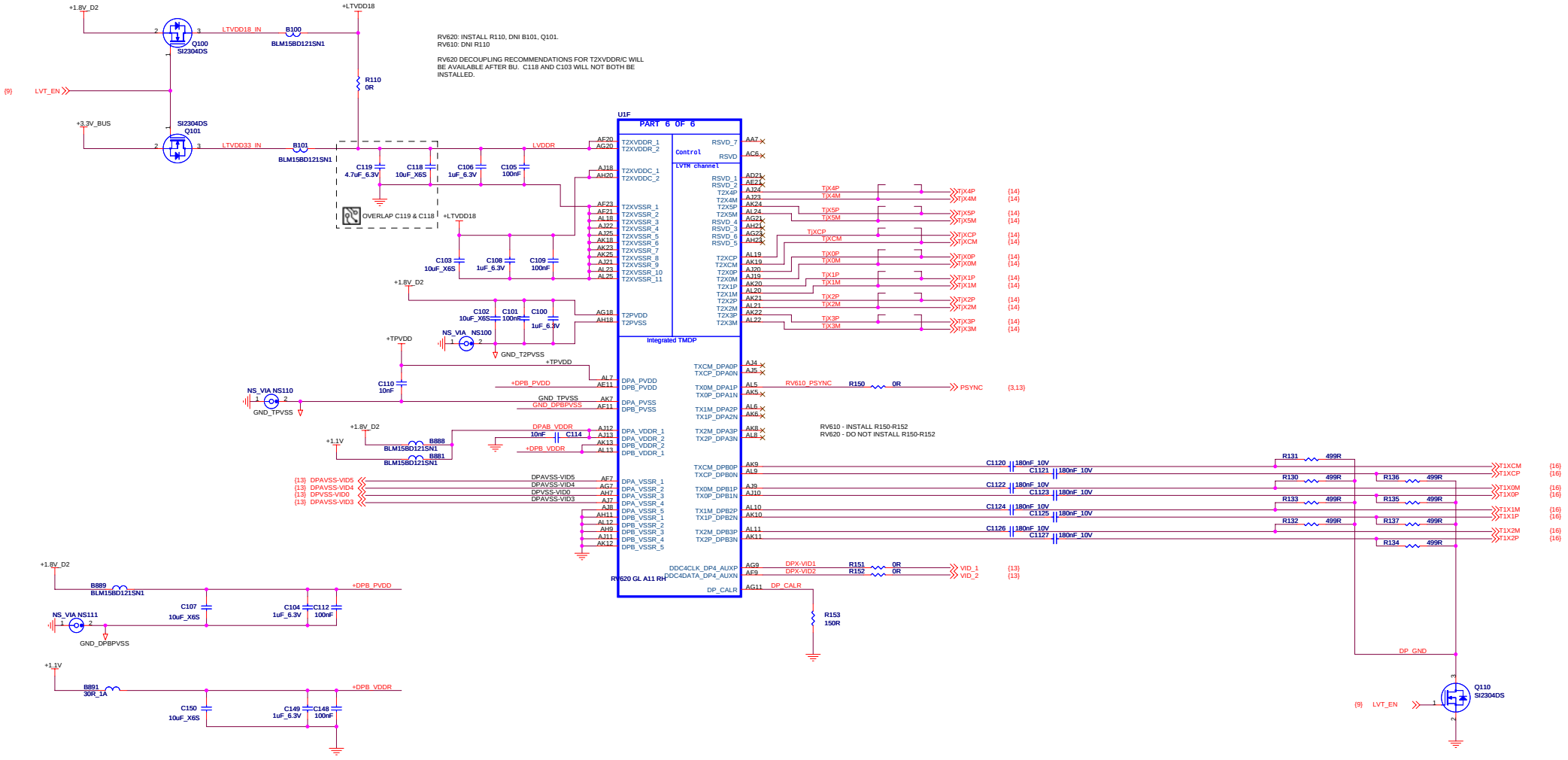
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

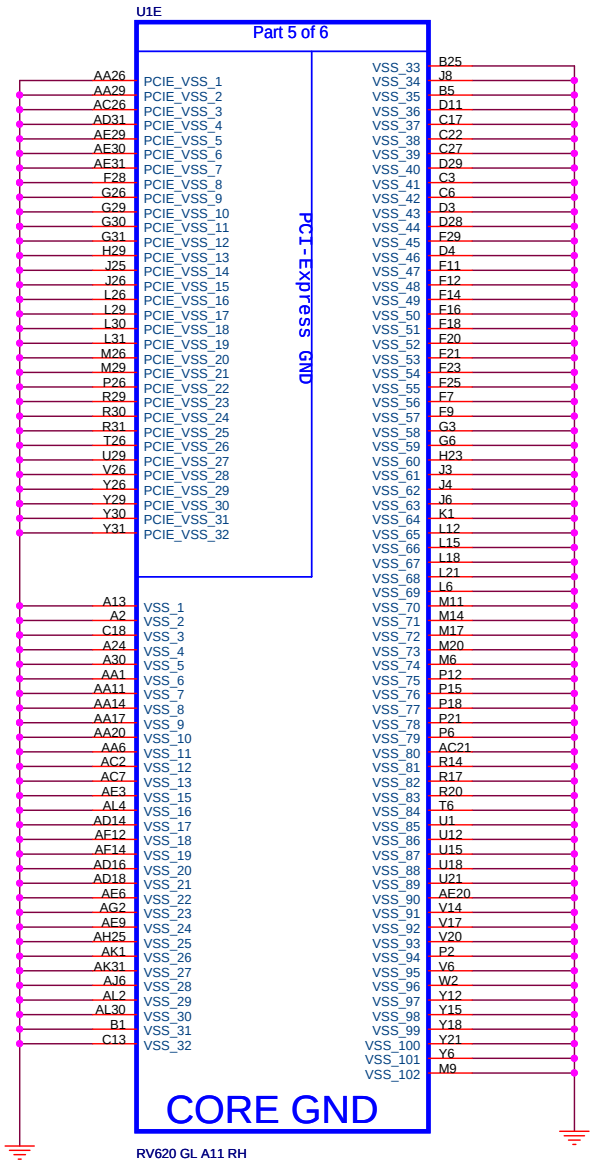
Date: Thursday, May 15, 2008 Rev 17

Sheet 3 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dpvi

Doc No. 105-B350xx-00C


RV620: INSTALL R110, DNI B101, Q101.
RV610: DNI R110
RV620 DECOUPLING RECOMMENDATIONS FOR T2XVDDR/C WILL BE AVAILABLE AFTER BU. C118 AND C103 WILL NOT BOTH BE INSTALLED.
U1F
PART 6 OF 6
Integrated TMDP
RV620 GL A11 RH
OVERLAP C119 & C118
RV610 - INSTALL R150-R152
RV620 - DO NOT INSTALL R150-R152
Q100 SI2304DS
Q101 SI2304DS
Q110 SI2304DS
B100 BLM15BD121SN1
B101 BLM15BD121SN1
B881 BLM15BD121SN1
B888 BLM15BD121SN1
B889 BLM15BD121SN1
B891 30R_1A
NS_VIA NS100
NS_VIA NS110
NS_VIA NS111
R110 0R
R150 0R
R151 0R
R152 0R
R153 150R
+1.8V_D2
+3.3V_BUS
+LTVDD18
+1.1V
+TPVDD
+DPB_PVDD
+DPB_VDDR
LVDDR
LTVDD18_IN
LTVDD33_IN
LVT_EN
GND_TPVSS
GND_DPBPVSS
DP_GND
DP_CALR
PSYNC
DPX-VID1
DPX-VID2
RV610_PSYNC
DPAB_VDDR
DPAVSS-VID5
DPAVSS-VID4
DPVSS-VID0
DPAVSS-VID3
TJX4P
TJX4M
TJX5P
TJX5M
TJXCP
TJXCM
TJX0P
TJX0M
TJX1P
TJX1M
TJX2P
TJX2M
TJX3P
TJX3M
T1XCM
T1XCP
T1X0M
T1X0P
T1X1M
T1X1P
T1X2M
T1X2P
VID_1
VID_2
C119 4.7uF_6.3V
C118 10uF_X6S
C106 1uF_6.3V
C105 100nF
C103 10uF_X6S
C108 1uF_6.3V
C109 100nF
C102 10uF_X6S
C101 100nF
C100 1uF_6.3V
C110 10nF
C107 10uF_X6S
C104 1uF_6.3V
C112 100nF
C150 10uF_X6S
C149 1uF_6.3V
C148 100nF
C114 10nF
C1120 180nF_10V
C1121 180nF_10V
C1122 180nF_10V
C1123 180nF_10V
C1124 180nF_10V
C1125 180nF_10V
C1126 180nF_10V
C1127 180nF_10V
R131 499R
R130 499R
R133 499R
R132 499R
R136 499R
R135 499R
R137 499R
R134 499R
Control
LVTM channel
T2XVDDR_1
T2XVDDR_2
T2XVDDC_1
T2XVDDC_2
T2XVSSR_1
T2XVSSR_2
T2XVSSR_3
T2XVSSR_4
T2XVSSR_5
T2XVSSR_6
T2XVSSR_7
T2XVSSR_8
T2XVSSR_9
T2XVSSR_10
T2XVSSR_11
T2PVDD
T2PVSS
DPA_PVDD
DPB_PVDD
DPA_PVSS
DPB_PVSS
DPA_VDDR_1
DPA_VDDR_2
DPB_VDDR_2
DPB_VDDR_1
DPA_VSSR_1
DPA_VSSR_2
DPA_VSSR_3
DPA_VSSR_4
DPA_VSSR_5
DPB_VSSR_1
DPB_VSSR_2
DPB_VSSR_3
DPB_VSSR_4
DPB_VSSR_5
RSVD_7
RSVD
RSVD_1
RSVD_2
RSVD_3
RSVD_4
RSVD_5
RSVD_6
T2X4P
T2X4M
T2X5P
T2X5M
T2XCP
T2XCM
T2X0P
T2X0M
T2X1P
T2X1M
T2X2P
T2X2M
T2X3P
T2X3M
TXCM_DPA0P
TXCP_DPA0N
TX0M_DPA1P
TX0P_DPA1N
TX1M_DPA2P
TX1P_DPA2N
TX2M_DPA3P
TX2P_DPA3N
TXCM_DPB0P
TXCP_DPB0N
TX0M_DPB1P
TX0P_DPB1N
TX1M_DPB2P
TX1P_DPB2N
TX2M_DPB3P
TX2P_DPB3N
DDC4CLK_DP4_AUXP
DDC4DATA_DP4_AUXN
DP_CALR
CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.
©2007 Advanced Micro Devices
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario
Date: Thursday, May 15, 2008
Rev 17
Sheet 4 of 20
Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No. 105-B350xx-00C

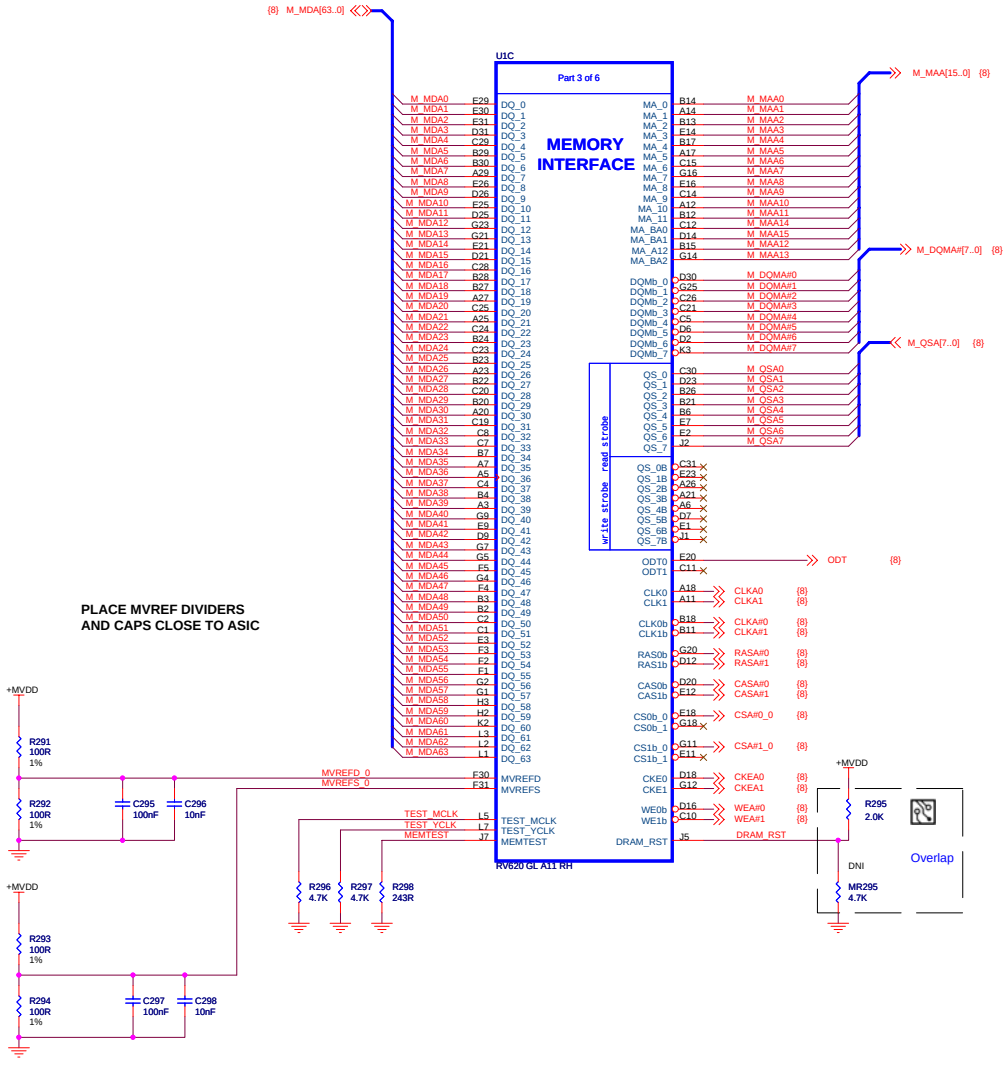


Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, May 15, 2008 Rev 17

Sheet 5 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI Doc No. 105-B350xx-00C



DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

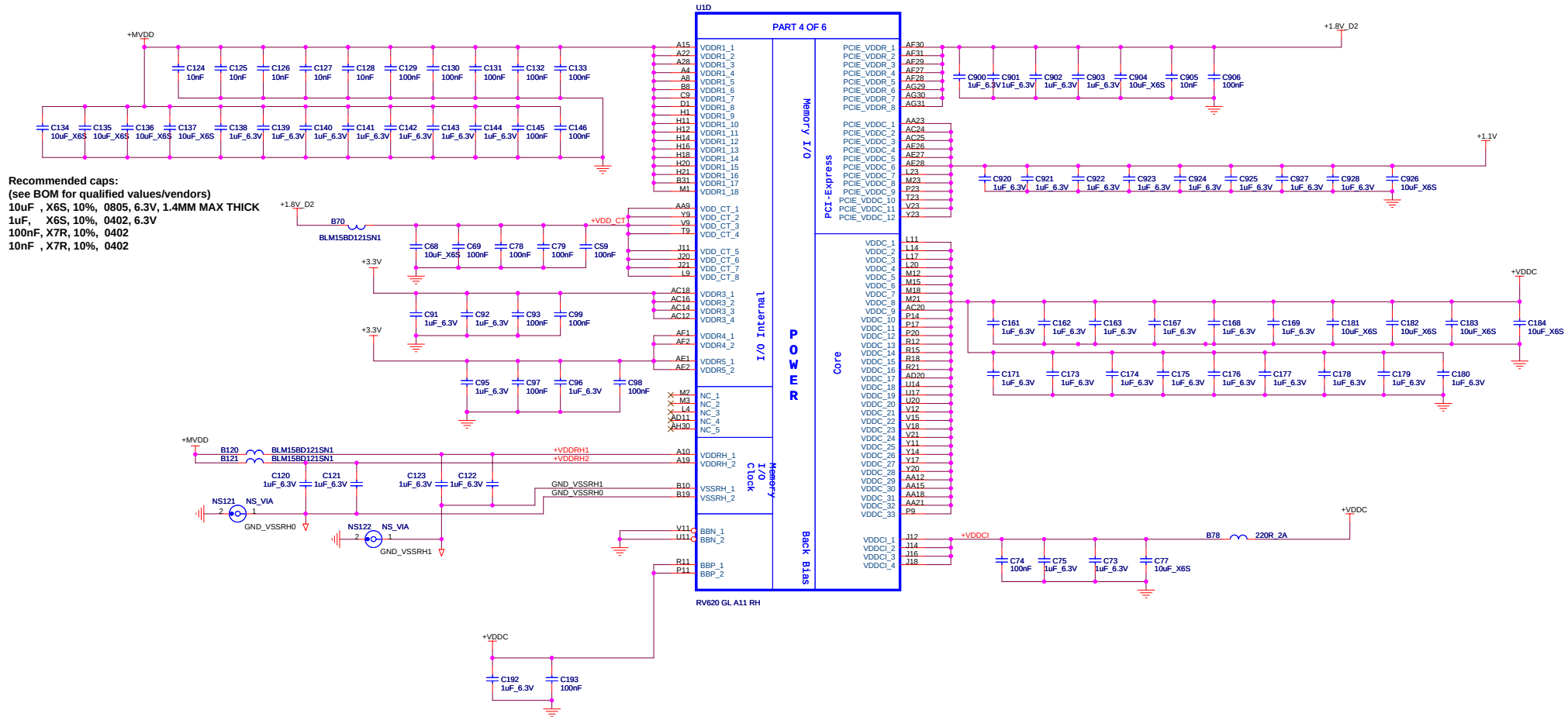
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, May 15, 2008 Rev 17

Sheet 6 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVT

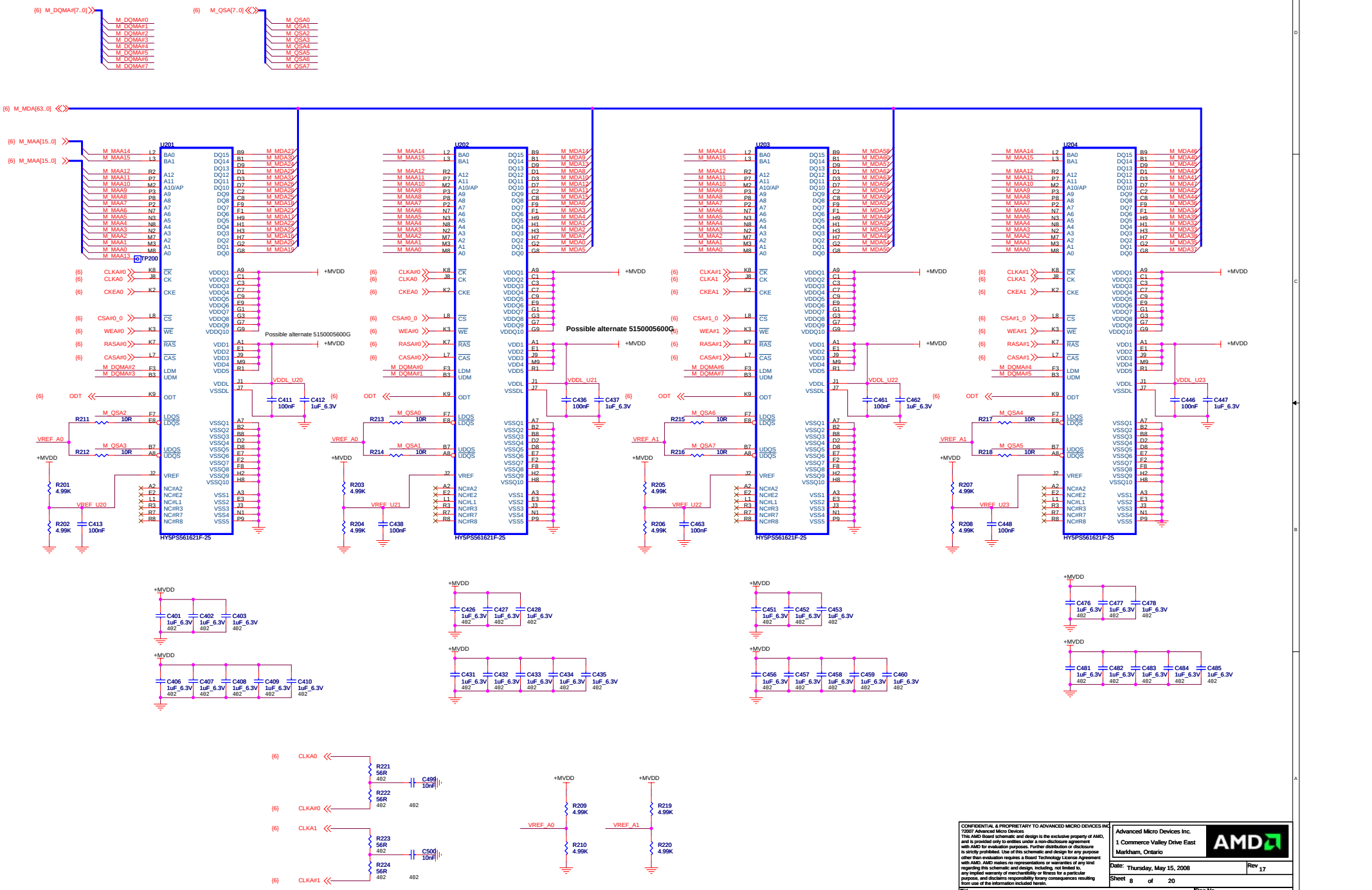
Doc No. 105-B350xx-00C



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Thursday, May 15, 2008
Rev	17
Sheet	7 of 20
Title	RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No.	105-B350xx-00C

CHANNEL A: RANK 0 128MB DDR2



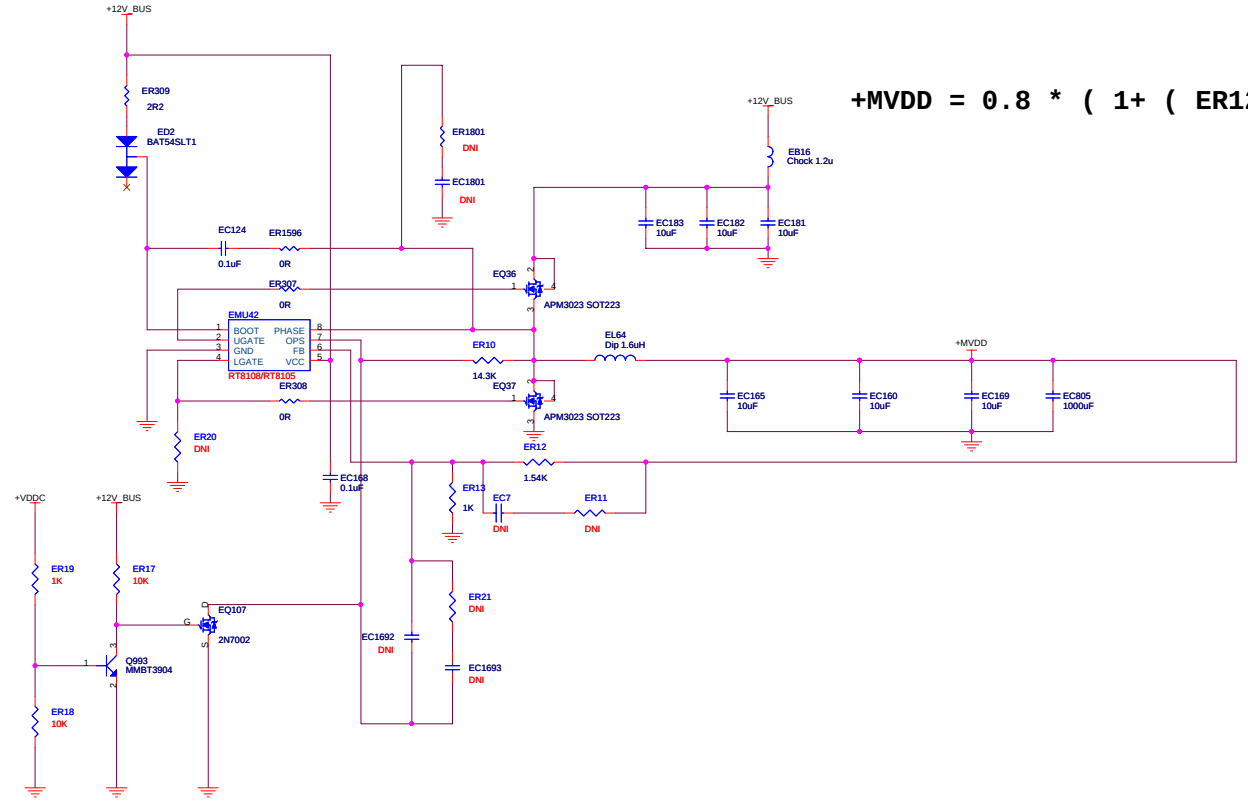
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, May 15, 2008 Rev 17

Sheet 8 of 20

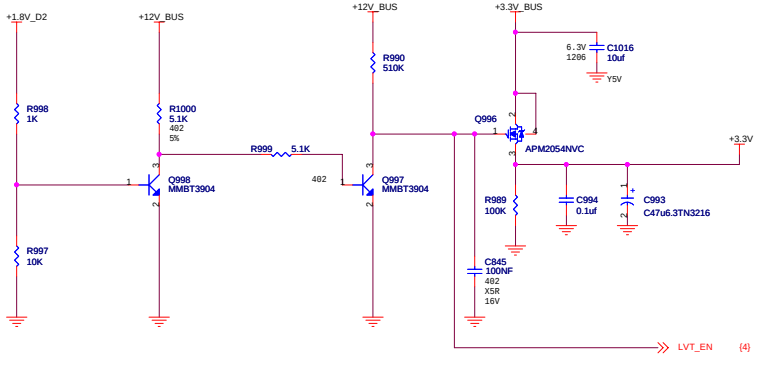
Title: RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

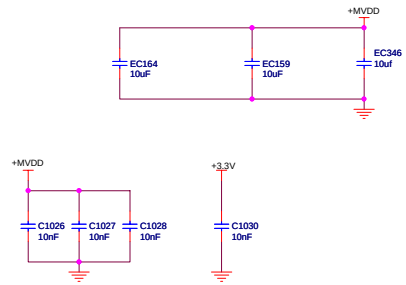
Doc No. 105-B350xx-00C

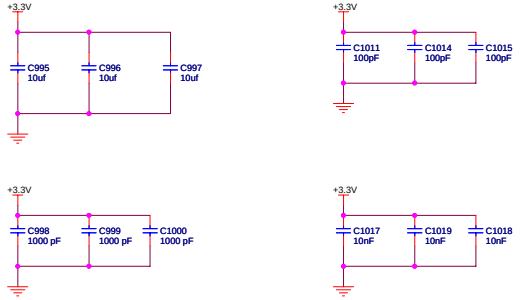


+MVDD = 0.8 * (1+ (ER12 / ER13))

Memory Power Seq







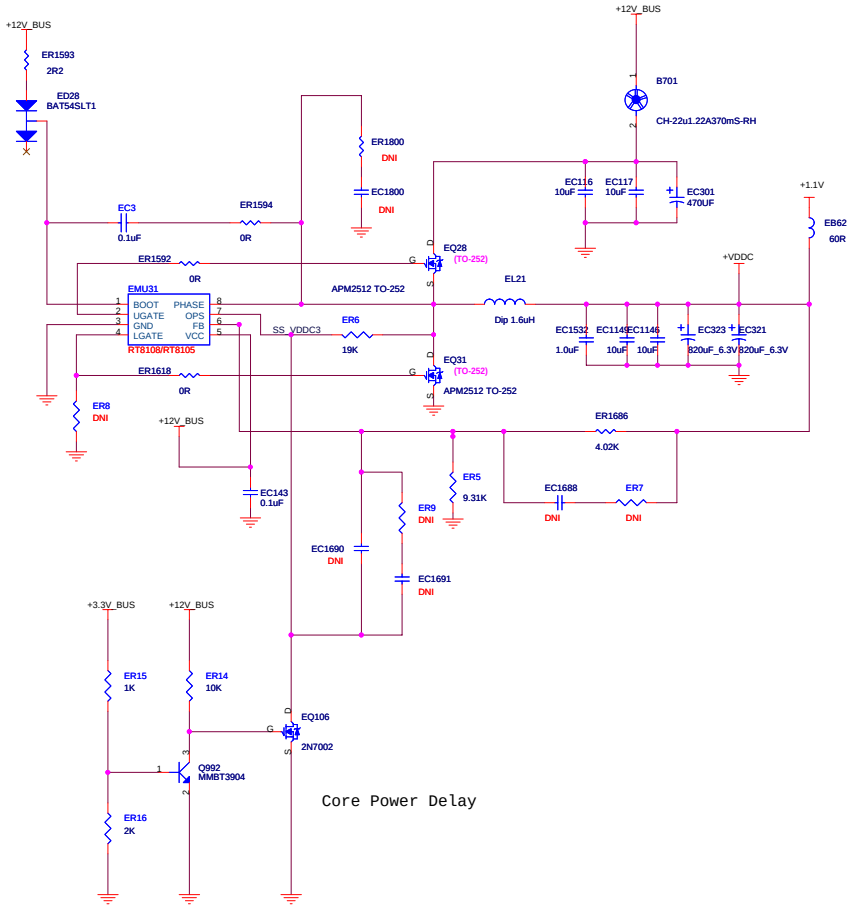
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, May 15, 2008 Rev 17

Sheet 9 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

Doc No. 105-B350xx-00C



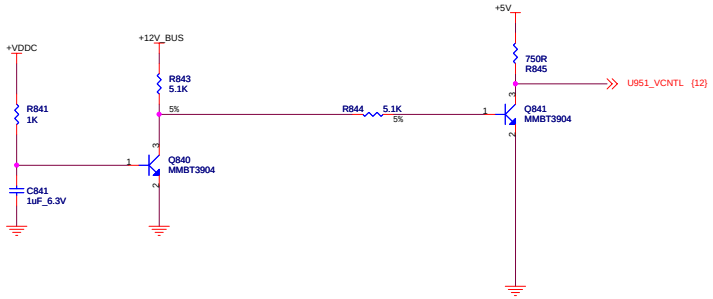
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, May 15, 2008 Rev 17

Sheet 10 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO DDR

Doc No. 105-B350xx-00C



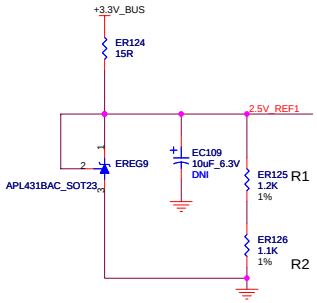
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

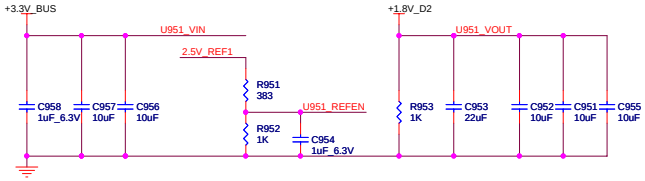
Date: Thursday, May 15, 2008 Rev 17

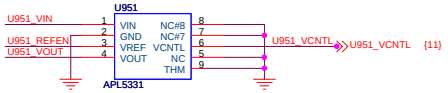
Sheet 11 of 20

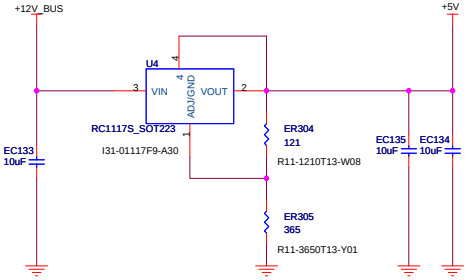
Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO DDR

Doc No. 105-B350xx-00C

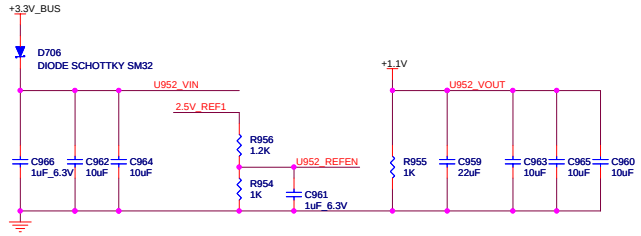


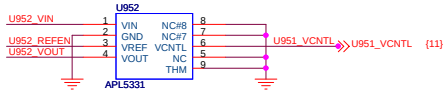




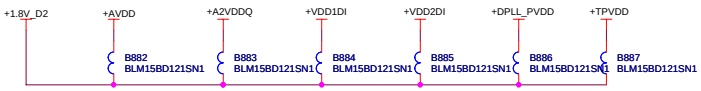


Vout=1.25V* [1+(ER305/ER304)]





Shared Power Rails



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, May 15, 2008 | Rev 17

Sheet 12 of 20

Title: RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI | Doc No. 105-B350xx-00C

PIN BASED STRAPS

RV610: INSTALL MR58
RV620: INSTALL R58

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - ATI Internal Use Only - Reserved (Default: 00)

GPIO(4) - DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(7) - TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

GPIO(8) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0] IF BIOS_ROM_EN=1 [default] (GPIO_22)
tmel - AT25F512A (512 kbit)0010
AT25F1024A (1 Mbit)0011
ST Microelectronics- M25P05A (512 kbit) 0100
M25P10A (1 Mbit) 0101
M25P20 (2 Mbit) 0101
Chingis (formerly PMC) -
Pm25LV512 (512 kbit) 0100
Pm25LV010 (1 Mbit) 0101

If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. (Config 3 = don care).
x000 128MB
x001 256MB
x010 64MB
x011 32MB
x100 512MB
x101 1GB
x110 2GB
x111 4GB

GENERICC, GENERICB - ATI Internal Use Only - Reserved (Default: 0)

VSYNC - VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - ATI Internal Use Only - Reserved (Default 0)

PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO_21 - ATI Internal Use Only - Reserved (Default: 0)

VID_0 - ATI Internal Use Only - Reserved (Default: 0)

VID_1 - MSI_DIS (Default: 0)

VID_2 - ATI Internal Use Only - Reserved (Default: 0)

VID_3 - ATI Internal Use Only - Reserved (Default: 0)

VID_4 - ATI Internal Use Only - Reserved (Default: 0)

VID_5 - 64BAR_EN_A (Default: 0)
Enable 64-bit BARS

VID_6:7 - ATI Internal Use Only - Reserved (Default: 00)

VSYNC - DDR2 VENDOR SELECT ATI Board Feature I
(see GPIO_18)

HSYNC2 - ATI Internal Use Only - Reserved (Default: 0)

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

GPIO_15 - FOR FUTURE EXPANSION

GPIO_22_ROMCSb - Enable external BIOS ROM device (Default 1)

GPIO_18 - DDR2 MEM VENDOR [V2SYNC:GPIO_18] ATI Board Feature I
QUIMONDA [0:0]
HYNIX [0:1]
SAMSUNG [1:0]

RV610: (DEFAULT) MR70, R73, MR74, MR75 INSTALLED

RV620: MR70, MR73, MR74, MR75 MUST BE INSTALLED

{3} GPIO_[13..0]

GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground — High logic voltage

Signal

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, May 15, 2008 Rev 17

Sheet 13 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI Doc No. 105-B350xx-00C

Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)

{3} A_R_DAC1
{3} A_RB_DAC1
{3} A_G_DAC1
{3} A_GB_DAC1
{3} A_B_DAC1
{3} A_BB_DAC1

R1029 37.4R
R1028 37.4R
R1027 37.4R
R1003 75R
R1002 75R
R1001 75R

A_R_DAC1_M L1004 47nH
A_G_DAC1_M L1005 47nH
L1006 47nH

C1001 8.0pF 402
C1002 8.0pF 402
C1003 8.0pF 402
C1005 8.0pF 402
C1006 8.0pF 402
C1004 8.0pF 402

+3.3V
BAT54SLT1 ED62
BAT54SLT1 ED63
BAT54SLT1 ED64

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F

DDCDATA_DAC1_R
DDCCLK_DAC1_R
A_HSYNC_DAC1_R
A_VSYNC_DAC1_R

+5V
+5V_VESA
EF1 0.2A

Place close to Connector
SHOULD BE A LOW INDUCTANCE PATH TO PIN 5

C1010 100nF

MJ1001
1 R
2 G
3 B
11 MS0
12 MS1
4 MS2
15 MS3
9 NC
13 HS
14 VS
5 VSS
6 VSS#6
7 VSS#7
8 VSS#8
10 VSS#10
16 CASE
17 CASE#17
G3179C219-005

SLIM VGA

+3.3V
R1004 10K 402
{3} CRT1DDCDATA
BSH111 Q1001
+5V
R1005 1.9K 402
DDCDATA_DAC1_5V
R1006 33R
DDCDATA_DAC1_R

+3.3V
R1007 10K 402
{3} CRT1DDCCLK
BSH111 Q1002
+5V
R1008 1.9K 402
DDCCLK_DAC1_5V
R1009 33R
DDCCLK_DAC1_R

C1999 100nF
+5V
{3,13} A_HSYNC_DAC1
A_HSYNC_DAC1_B
U1999A SN74HCT125D
R1010 33R 402
A_HSYNC_DAC1_R

SN74HCT125D U1999B
{3,13} A_VSYNC_DAC1
A_VSYNC_DAC1_B
R1011 33R 402
A_VSYNC_DAC1_R

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

{4} TjX2M
{4} TjX2P
R107 0R
R108 0R
{4} TjX4M
{4} TjX4P
R109 0R
R111 0R
{4} TjX1M
{4} TjX1P
R112 0R
R114 0R
{4} TjX3M
{4} TjX3P
R115 0R
R116 0R
{4} TjX0M
{4} TjX0P
R117 0R
R118 0R
{4} TjX5M
{4} TjX5P
R119 0R
R120 0R
{4} TjXCP
{4} TjXCM
R121 0R
R122 0R

R102 100R
R104 100R
R101 100R
R103 100R
R100 100R
R105 100R
R106 100R

DDCCLK_DAC1_R
DDCDATA_DAC1_R
A_VSYNC_DAC1_R
A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
A_HSYNC_DAC1_R

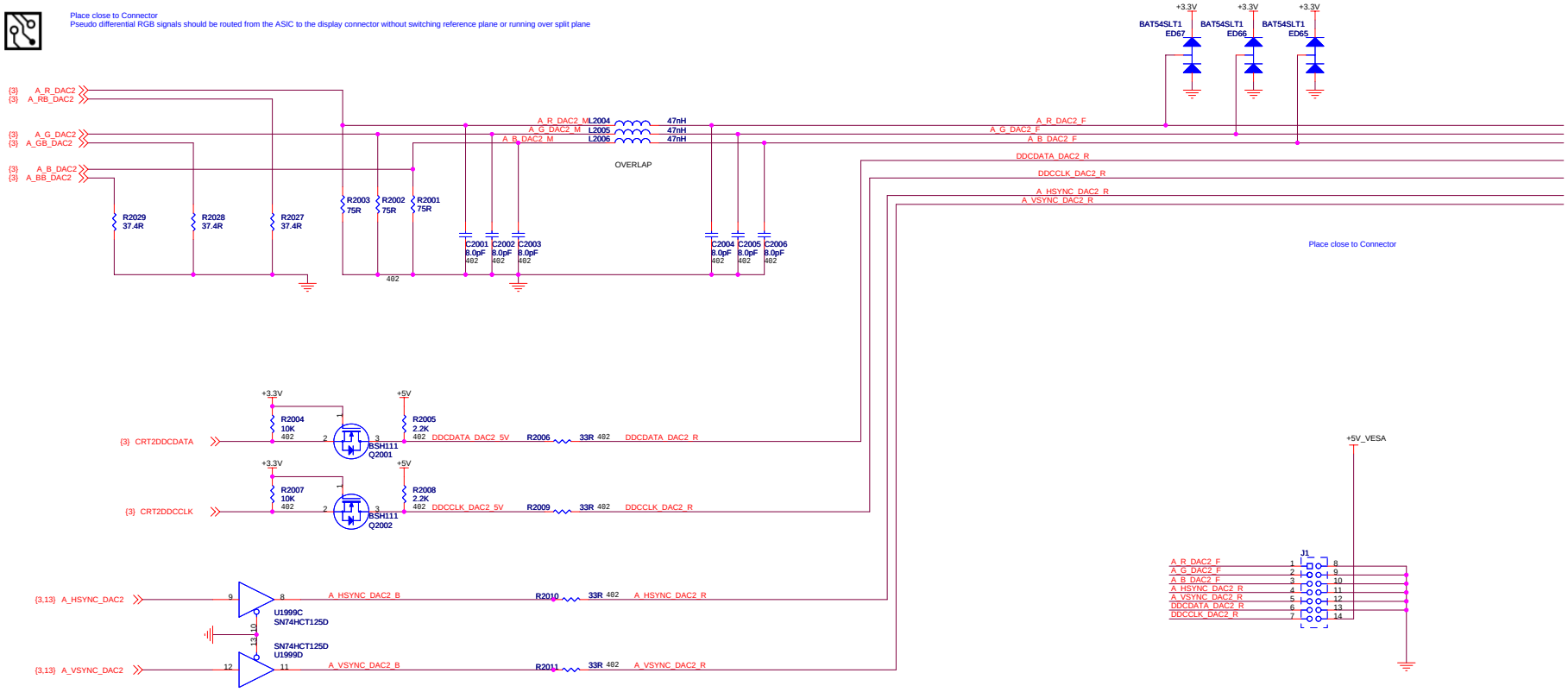
+3.3V
Q1021 MMBT3904
R1022 10K
HPD_DVI1
{3} HPD1
R1023 10K

+5V_VESA
J1001
25 CASE
1 TMDS Data2-
2 TMDS Data2+
3 TMDS Data2/4 Shield
4 TMDS Data4-
5 TMDS Data4+
6 DDC Clock
7 DDC Data
8 Analog VSYNC
9 TMDS Data1-
10 TMDS Data1+
11 TMDS Data1/3 Shield
12 TMDS Data3-
13 TMDS Data3+
14 +5V Power
15 GND (for +5V)
16 Hot Plug Detect
17 TMDS Data0-
18 TMDS Data0+
19 TMDS Data0/5 Shield
20 TMDS Data5-
21 TMDS Data5+
22 TMDS Clock Shield
23 TMDS Clock+
24 TMDS Clock-
C1 Analog Red
C2 Analog Green
C3 Analog Blue
C4 Analog HYNC
C5 Analog GND
C6 Analog GND#C6
26 CASE#26
27 CASE#27
28 CASE#28
29 CASE#29
30 CASE#30
DVI_CONNECTOR

TMDS_2(Daul_Link) + DAC_1-CRT

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

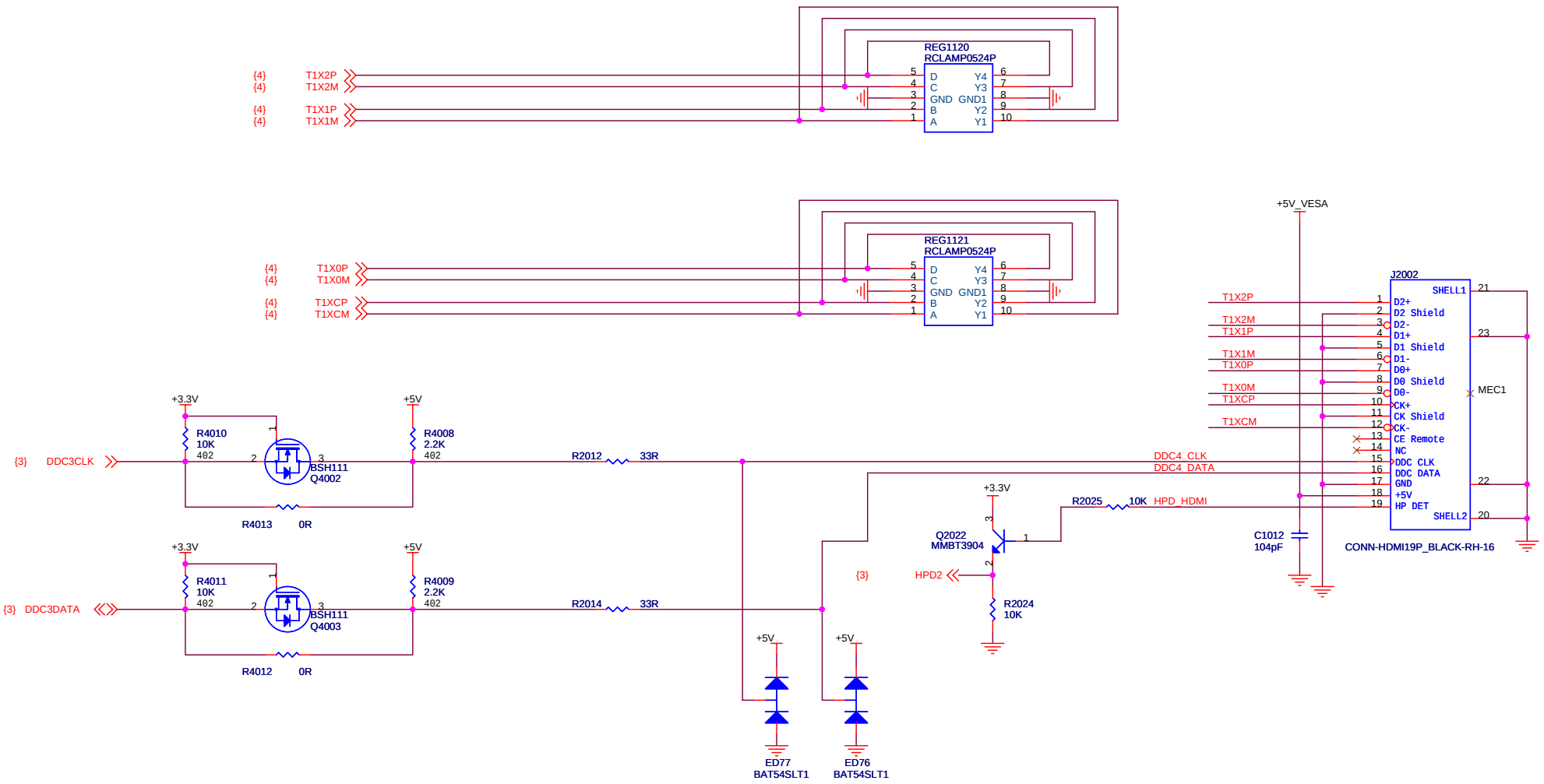
Date: Thursday, May 15, 2008
Rev 17
Sheet 14 of 20
Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No. 105-B350xx-00C



TMDS_1(Single_Link) + DAC_2-CRT

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Thursday, May 15, 2008
Rev	17
Sheet	15 of 20
Title	RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No.	105-B350xx-00C

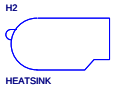


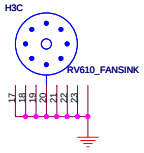
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

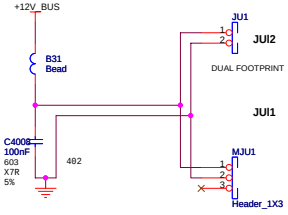
Date: Thursday, May 15, 2008 Rev 17

Sheet 16 of 20

Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI Doc No. 105-B350xx-00C





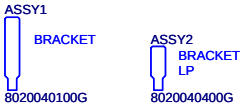


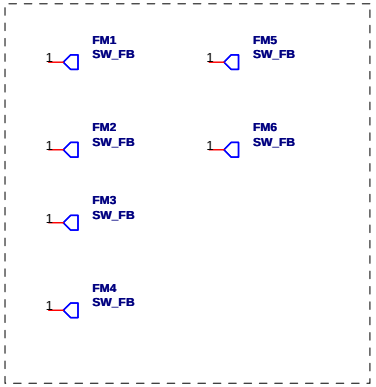
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

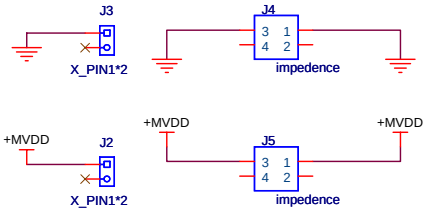
Date: Thursday, May 15, 2008 | Rev 17

Sheet 17 of 20

Title: RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI | Doc No. 105-B350xx-00C







Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, May 15, 2008 | Rev 17

Sheet 18 of 20

Title: RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI | Doc No. 105-B350xx-00C

<variant name>

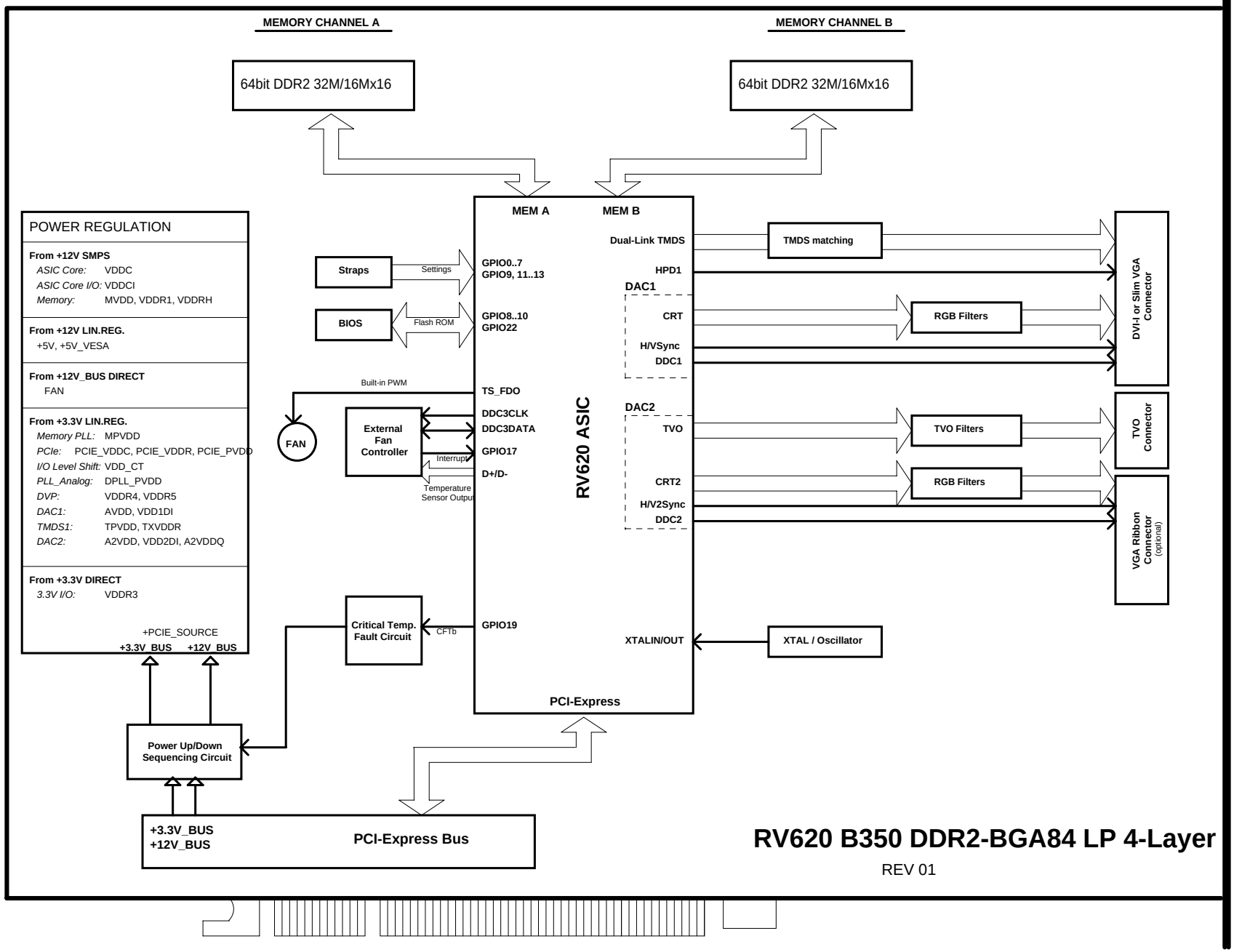
Title	Schematic No.	Date:
RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI	105-B350xx-00C	**Thursday, May 15, 2008**

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 17

Sch Rev	PCB Rev	Date	REAL REVISION DESCRIPTION
01	00A	2007.05.07	START NEW SCHEMATIC. DERIVED FROM B170 (RV610) SCHEMATIC.
02	00A	2007.05.17	p. 4 MR155/R155 FIX SHORT
03	00A	2007.05.17	RM R7, NR7, R5, MB60, MR45, R45, R890, R1248, R1247, R1242, R1243, C853, C863; ADD R2, B890, MR890, C846; CHANGE R1022, R1023;
04	00A	2007.05.22	REMOVE GND_TXVSSR, GND_PVSS; AG23 NOW NC - WAS SCHEM MISTAKE; ADD R858 FOR BUO; R858 CHANGE TO 1210;
05	00A	2007.05.24	CTF: ADD Q1252, R1254, R1255, R1256, R1258, Q1253, Q1254, CHANGE U1250 TO SINGLE FF; UPDATE BLOCK DIAGRAM.
06	00A	2007.05.25	LVTM: ADD R110, RM R109, MR109, R108, R107;
07	00A	2007.05.28	LVTM: ADD C118, RM C104; REMOVE MR85, MR86 FOR SIMPLIFICATION;
08	00A	2007.05.28	XTALIN/OUT: LAYOUT EASEMENT; REMOVE MR108 (R849 ALREADY THERE); LVTM: ADD C119 (LOWER COST OPTION); POWER SUPPLY: REMOVE R706, MR707, R606 & MR607;
09	00A	2007.05.29	REMOVAL OF +5V: ADD R861, MR861, R862, REG861, R869, R863, R867; REMOVE MU830, U830, C830. R833, R834, C831, R832, MR832, R831, MR831; CONNECT DDC TO 5V_VESA;
010	00A	2007.05.30	CHNG C858 TO 3.3VBUS; CONNECTION TO R845 CHNG; ADD R870, MR870, C867;
011	00A	2007.05.30	REMOVE R4033; REMOVE B201-204; ADD R30-33 [PLACE NEAR ASIC]; REMOVE R3004, R3005;
012	00A	2007.05.31	REMOVE C164-C166, C170, C172 PER SIMULATION RESULTS - THESE CAPS DO NOT IMPROVE DECOUPLING. RM TP860 (LAYOUT CONSTRAINTS. ALREADY ICT TP ON THAT NET);
013	00A	2007.05.31	RM R154-R157, MR154-157 -> FUNCTIONALITY TAKEN BY EXISTING STRAPS. LAYOUT USE PLACE OF M/R154-7; ADD R7; RM MR706, MR606, B889, R863; ADD D861;
014	00A	2007.05.32	ADD SOCKET SK1
015	00A	2007.06.1	SK? CORRECTED TO SK1.
016	00B	2007.06.25	NO NETLIST CHANGES; - MOUNTING HOLES CHANGED TO 3.175mm;
017	00C	2007.10.01	p. 1 - CONNECT B7 TO GND (SEE PA RV6XX H1) - REMOVE R2. IT IS ALWAYS POPULATED, NO NEED TO ZERO OHM. THIS BOARD DOES NOT SUPPORT JTAG DEBUG; p. 11 - REMOVE R839. THIS CIRCUIT IS VERIFIED, THERE IS NO NEED TO BE ABLE TO DISCONNECT IT; p. 12 - REMOVE R870 - THIS OPTION NOT USED, VCNTRL MUST BE HIGHER THAN +3.3V; - MR870 REMOVED - ALWAYS POPULATED, DO NOT NEED ZERO OHM RESISTOR OPTION; - REMOVE R860 - WAS BRING UP ONLY OPTION; p. 17 - REPLACED FAN CIRCUIT WITH ONE THAT HAS FEEDBACK: - ADD R4033, R4031, R4019, R4034, R4006, R4035, Q4004, R4035, Q40002. R4009, R4011, Q4003, R4012, R4013;



RV620 B350 DDR2-BGA84 LP 4-Layer

REV 01

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Thursday, May 15, 2008	Rev 17
Sheet 20 of 20	
Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI	Doc No. 105-B350xx-00C