Title
PCI-E RV380/370 256M pterm TSOP V-VV-DI

Schematic No.
105-A334xx-10

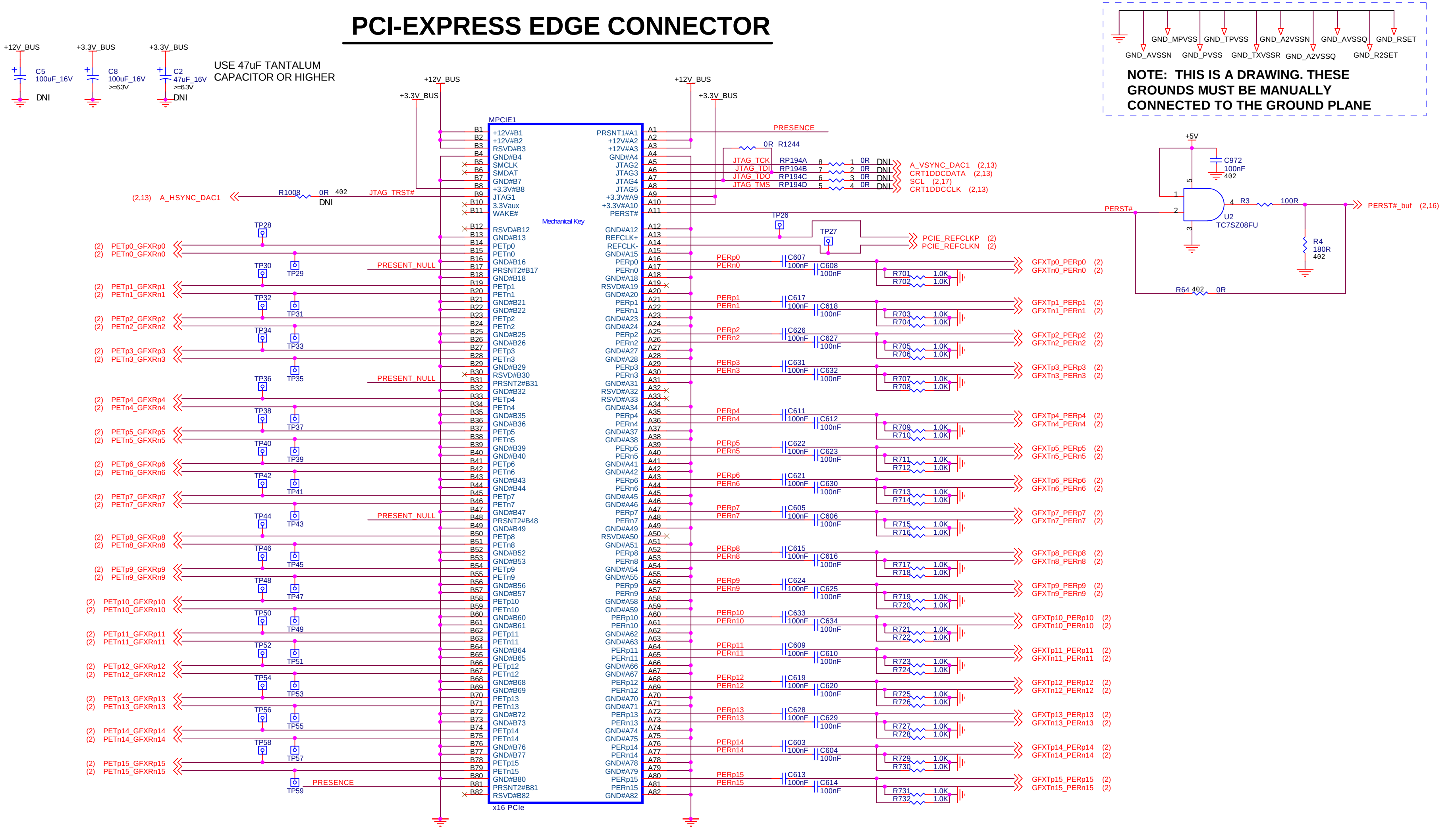
Date:
Saturday, July 31, 2004

REVISION HISTORY

Rev
7

Sch Rev		Date	REVISION DESCRIPTION
0	00A	2003-11-24	PRELIMINARY BASED ON 105-A297xx-00A 03-11-24 - (pg 02) Swap DVI DDC clock and data lines
1	00B	2003-12-29	- (pg 07) Add R1043 for power dissipation - (Layout) Move C284, blocking Grantsdale PCIE connector latch
2	00C	2004-03-09	- (Layout) Move fan connector to shorten fan power wire - (Layout) Correct C151 overlap - (pg02, 10) Fix pull-up +VDD_DVO to +VDDR4 - (pg04) Remove CP2, 3, 4, 5, 6 and 8 for dual footprint manufacturing issues (Capacitor packs sharing with 402 footprints) - (pg05) Remove dual-package FET for VDDC - (pg06) Remove C986, C987, C988, C989, C990, C991, C992 and C993) - (pg06) Change R297 to 1206 footprint - (pg07) Add MC917 as multi-footprint for C917, remove L3 (redundant option) - (pg13, 15) +5V supply with current limiting for VESA DDC spec, remove F1, B21 - (Layout/EMI) Connect L60, L61, L62, L80, L81, L82, C502, C504, C506, R513 and R514 to Digital Gnd instead of Chassis Gnd
3	00D	2004-04-01	- (pg04) Delete redundant dual footprint cap arrays (CP9, CP10 and CP11) - (pg05) Add MR357 and MR269 for power sequencing and delete redundant power sequence circuit (R153, R393~R398, Q27~Q30) - (pg05, layout) Improve RC snapper circuits (R15 and C156) layout on PWM - (pg05, layout) Correct overlapping component MU42 and D2 - (pg07) Delete redundant dual footprint caps (MC308 and MC160), delete redundant power sequencing (VDDC_GODD, VDDC_GOOD2 and VDDC_GOOD_PU, see pg05), change MREG37 reference to 1.8V - (pg07) Delete redundant regulators (REG8, U82, Q35, Q36, Q37, MQ37, R814~R816, R116~R119, R121~R123, R125~131, MR128, C14, C15 and C308) - (pg12) Correct some unused straps pull-up to +VDDR4 (R227, R229 and R231) - (pg13, layout) Move JU2 to the left to allow 2 more resistors for Chassis Digital Ground Short (R989 and R990) - (pg14) Add optional TVO filter MC502, MC504 and MC506 to chassis ground, add MR514 to place it below MiniDIN connector - (pg15) Change J2 to fully-shielded DVI connector - (layout) Improve thermal connection to MREG37 - (layout) Ground fill between TMDS pairs
4	00E	2004-04-08	- (pg13) Delete chassis gnd to digital ground resistors, change VGA and Slim-VGA connector chassis gnd to digital gnd - (pg14) Change VO filter, VO and VIVO connector to digital ground only - (pg15) Change DVI connector to digital gnd only - (pg16) Change VINGND of RT to digital gnd thru bead - (pg18) Change mounting hole to digital gnd, remove MT2 - (layout) Remove ground fill between TMDS pairs - (layout) Cut back +3.3V_BUS and +PCIE_VDDR power plans on layer 3 - (pg14) Remove R514, R513 and MR513
5	00F	2004-04-14	-00F revision was created based on customer's request to avoid confusion - (pg15) Add R926, R927, R928 and R929 to meet 70% derating spec of the power dissipation of resistors
6	00	2004-04-28	- Release to 00
7	10	2004-07-07	- (pg1) Add common mode resistors - (pg4) Change C62 to 603 footprint

PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
⏚	DIGITAL GROUND
▽	ANALOG GROUND

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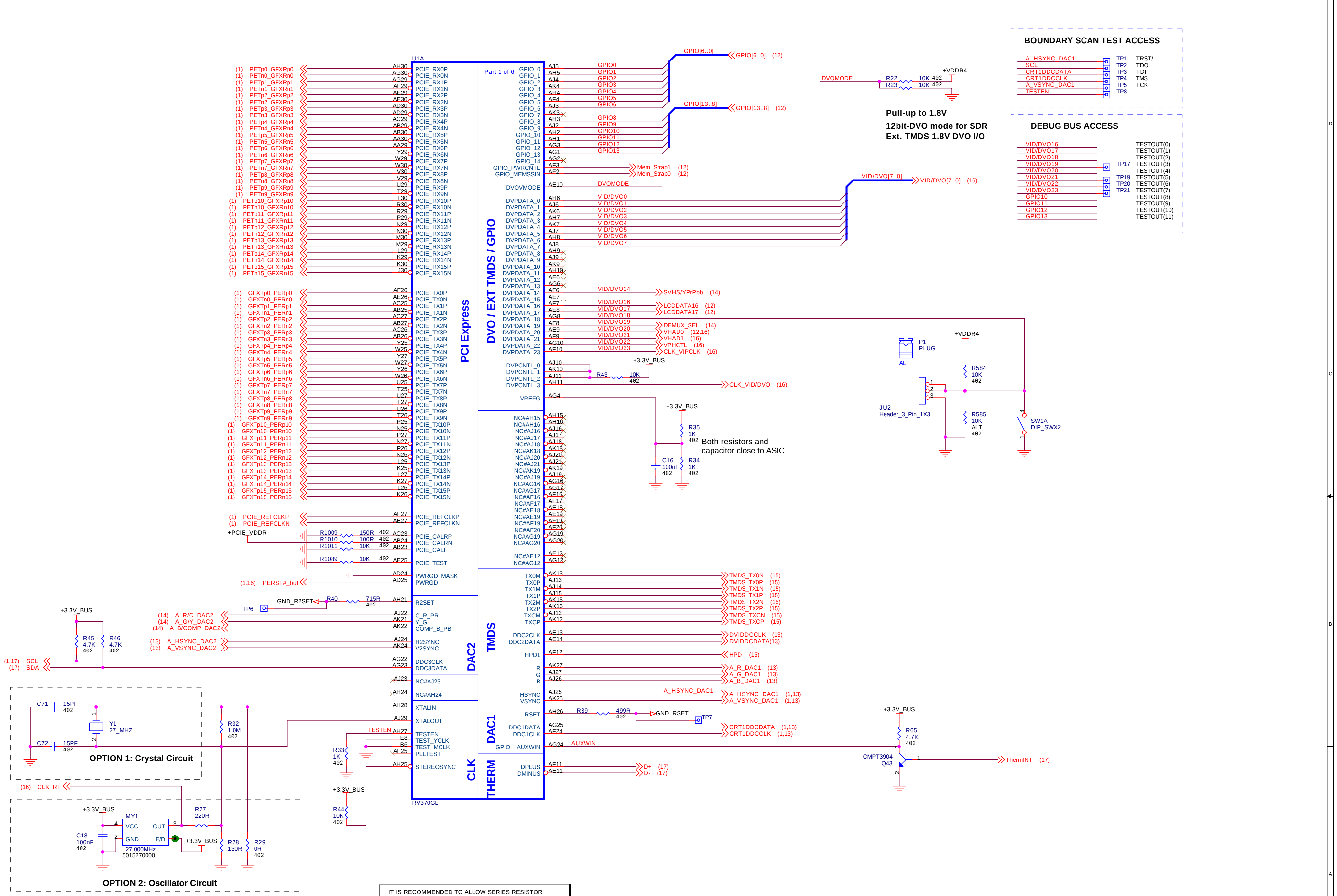

IT IS RECOMMENDED TO ALLOW SERIES RESISTOR
FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS
TO ADDRESS ANY LAYOUT NOISE RELATED
SIGNAL DAMPING REQUIREMENTS

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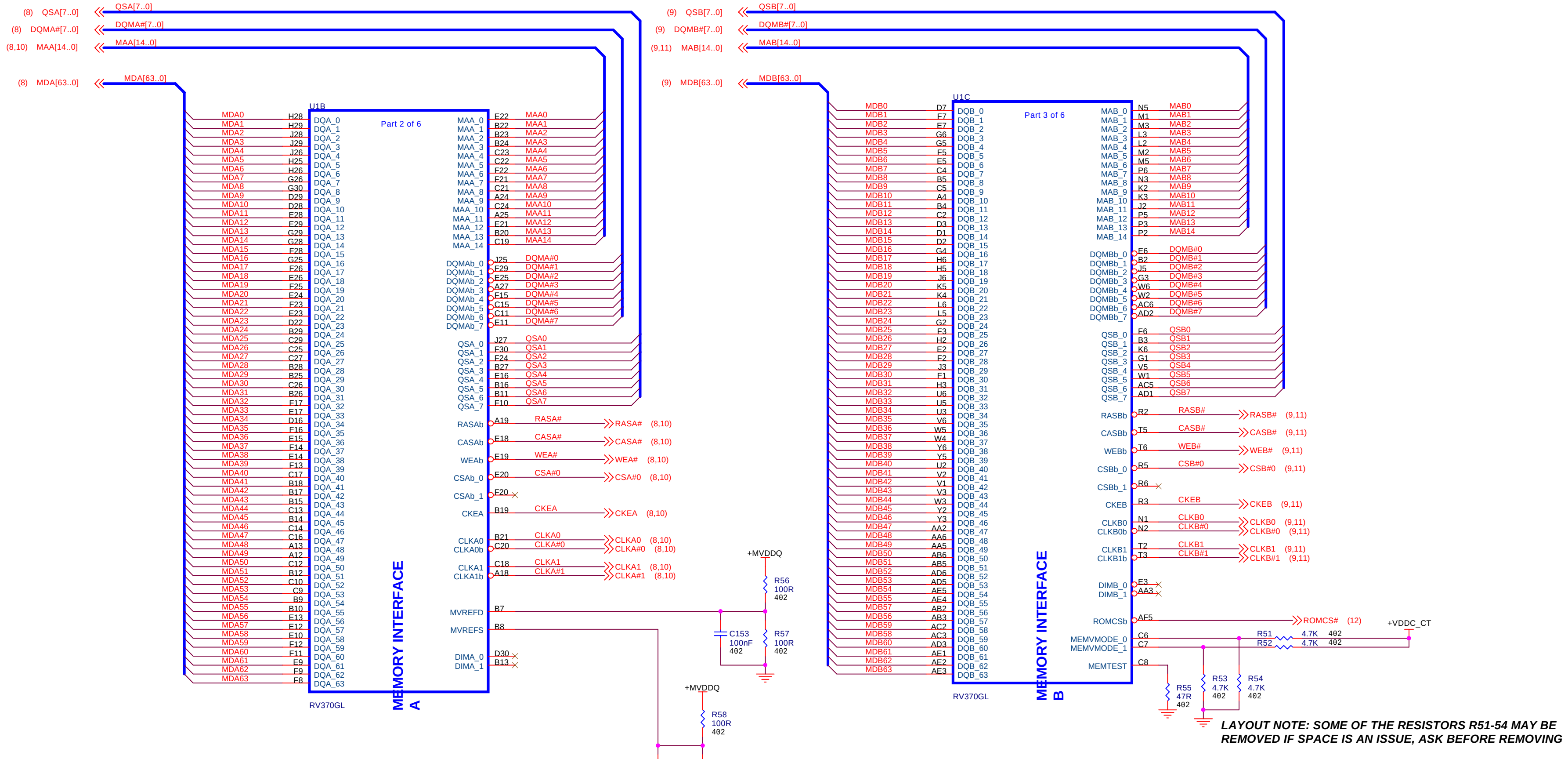

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

MEMORY CHANNEL A

MEMORY CHANNEL B

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

PLACE C351/152 VERY CLOSE TO ASIC

R56/57/58/59 CLOSE TO ASIC AS WELL

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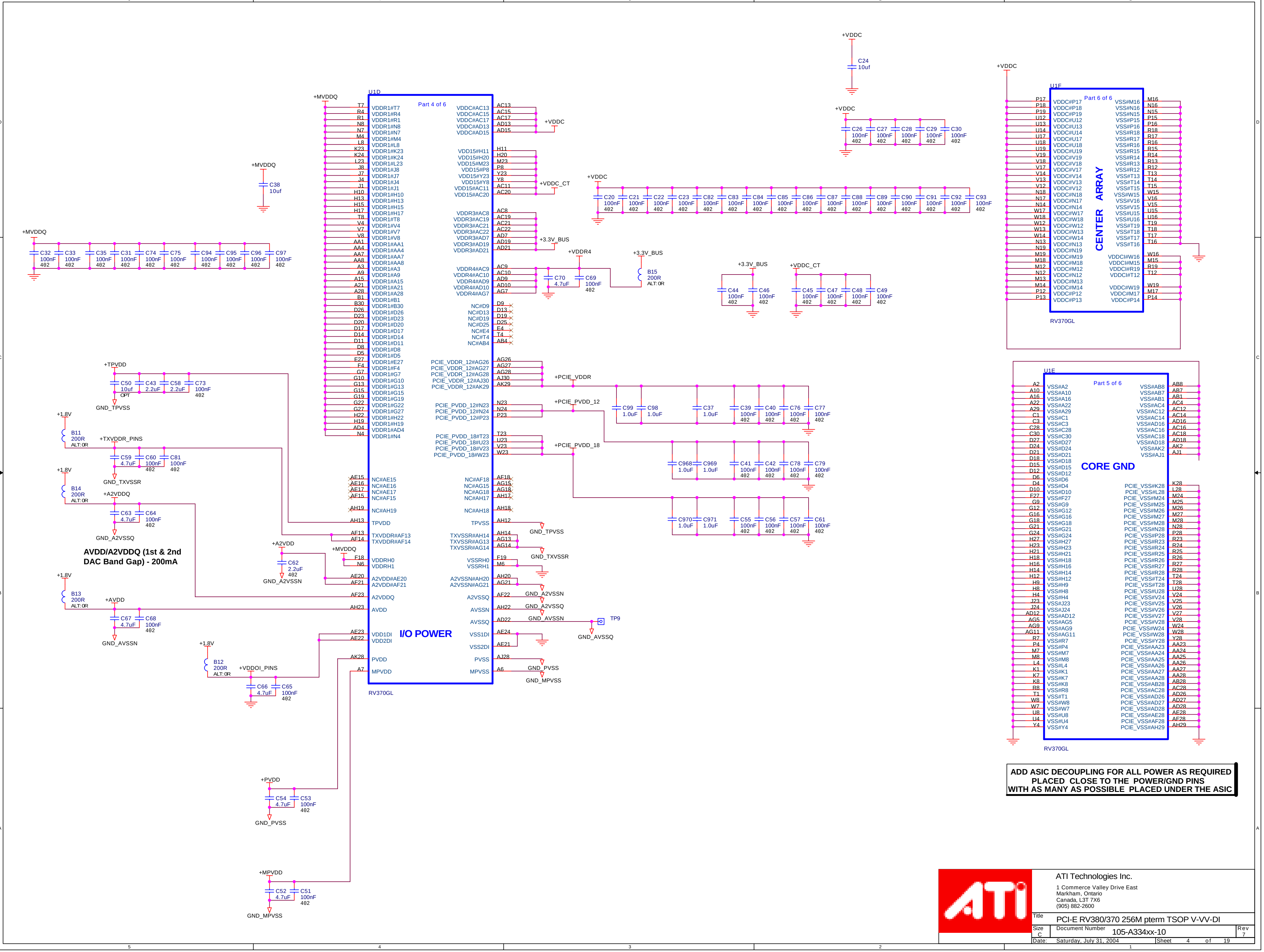

ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC

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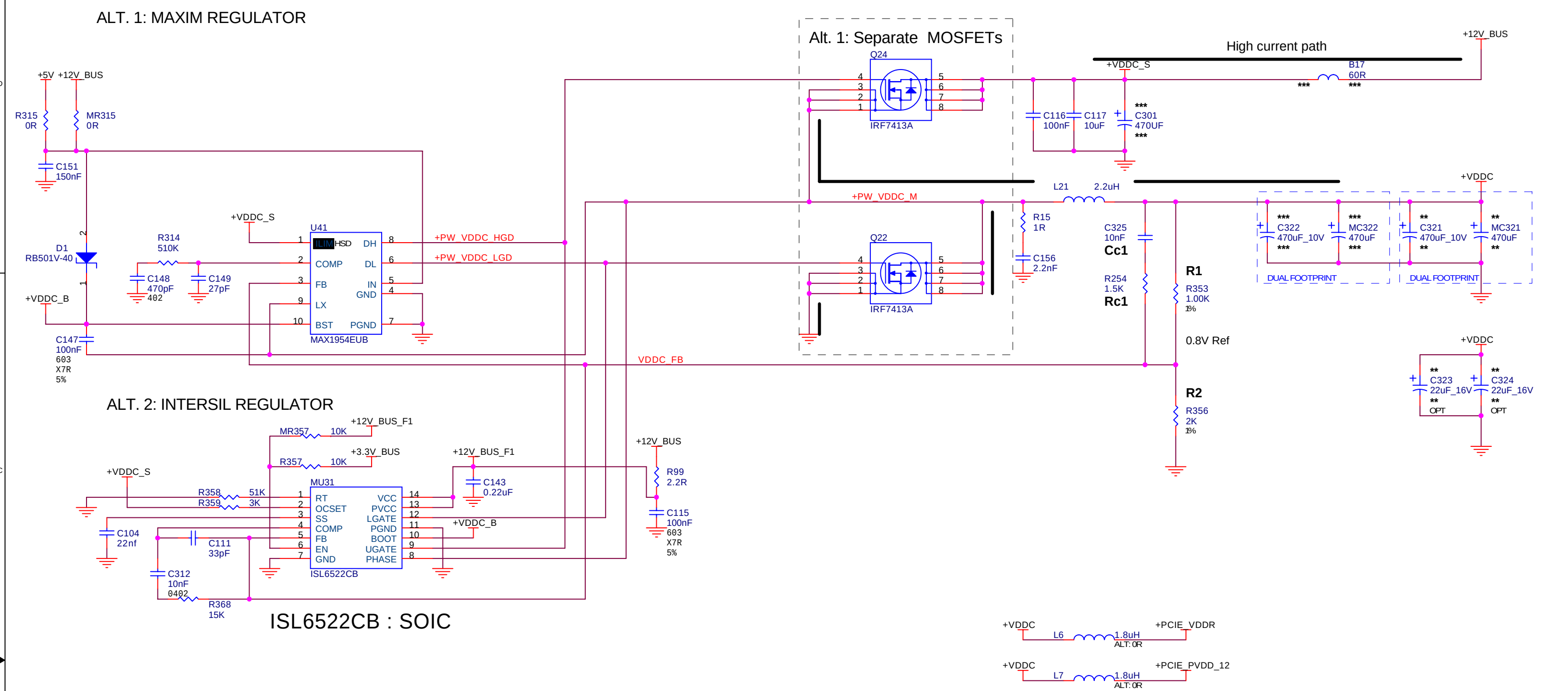
Regulator for VDDC (ASIC Core)

Vout = 1.2V ~ 1.3V



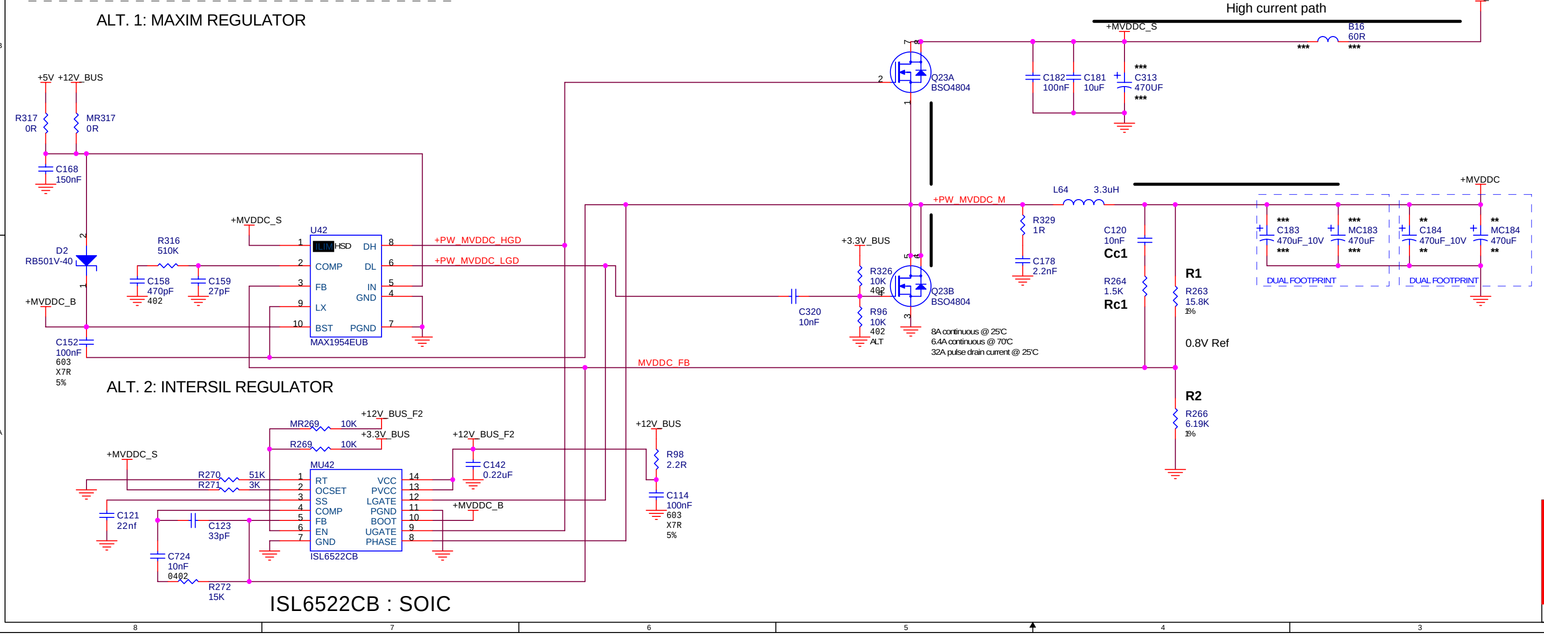
***	Indicate number of power via required for the connection

Part	NOTES
MAX1954	Do not install Cc1, Rc1
ISL6522	Install Cc1, Rc1

Part	Vout	R1	R2
MAX1954 ISL6522 0.8V Ref	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
0.8V Ref	1.25V	1.00K 1% ATI P/N 3240100100	1.78K 1% ATI P/N 3240178100
0.8V Ref	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100

Regulator for MVDDC (Memory Core)

Vout = 2.5V ~ 3.3V



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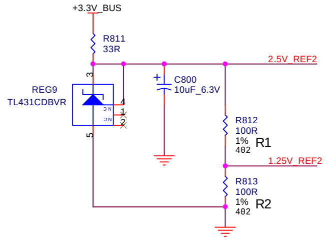
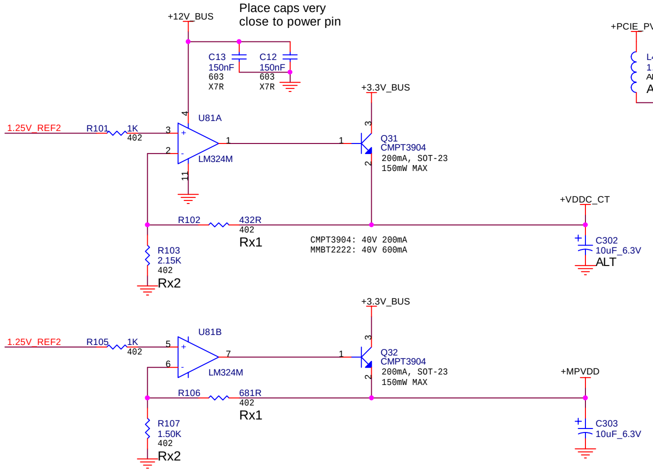


Voltage Req.	R1	R2
0.8V	150R P/N 3160150000 402	71.5R P/N 324075R500
1.25V	100R P/N 3160100000 402	100R P/N 3160100000 402
1.5V	100R P/N 3160100000 402	150R P/N 3160150000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.55	475R (402, 1%) P/N 3160475000	2K (402, 1%) P/N 3160200100
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240015200

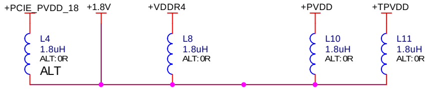
Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.85V	715R (402, 1%) P/N 3160715000	4.99K (402, 1%) P/N 3160499100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.61V	221R (402, 1%) P/N 3160221000	4.99K (402, 1%) P/N 3160499100
2.5V	0R P/N 3230000000 603 P/N 3150000000 402	DNI



1.5V

70mA MAX

+MPVDD: 10mA MAX



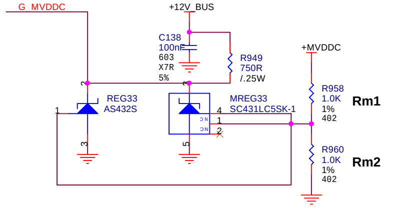
Rails derived from +VDDR4
+AVDD: 10mA MAX
+A2VDDQ: 20mA MAX
+VDDOI_PINS: 20mA MAX
+TXVDDR_PINS: 20mA MAX

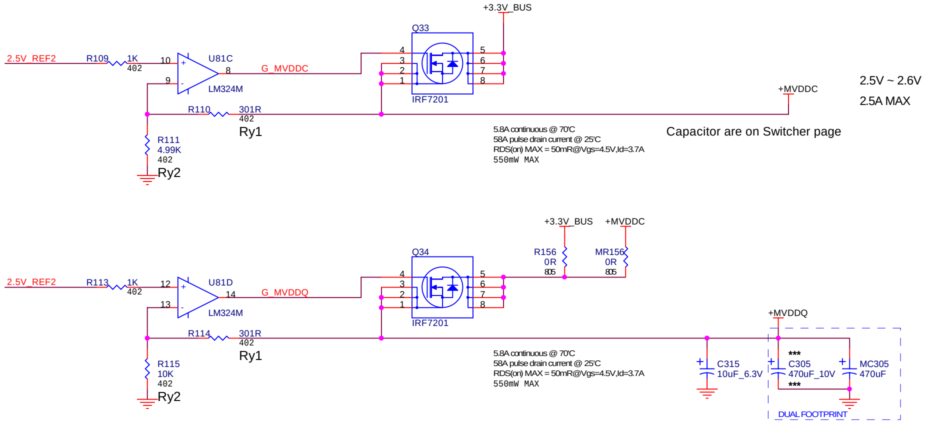
+PVDD: 25mA MAX

+TPVDD: 50mA MAX

Alt. regulator for +MVDDC
Vout = 2.5V ~ 2.6V
Iout = 500mA MAX

Voltage Req.	Rm1	Rm2
3.34V [-0.04V/+0.04V]	4.32K	2.55K
3.45V [-0.04V/+0.04V]	4.32K	2.43K
2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100





Capacitor are on Switcher page

2.5V ~ 2.6V

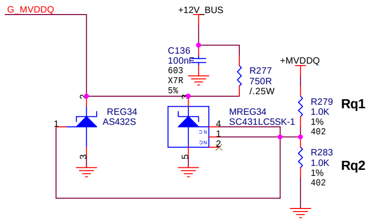
2.5A MAX

2.5V ~ 2.6V

1A MAX

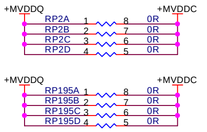
Alt regulator for +MVDDQ
Vout = 2.5V ~ 2.6V
Iout = 200mA MAX

Voltage Req.	Rq1	Rq2
1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
2.5V	1K 3240100100	1K 3240100100
2.6V	4.75K 3240475100	4.32K 3240432100

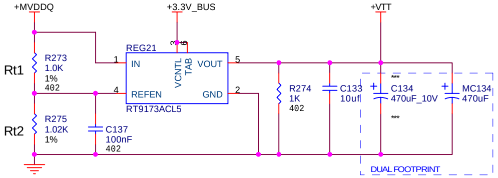


Regulator for +VTT (Termination)
Vout = 1.25V ~ 1.3V with +2.5V +MVDDQ
Iout = 1000mA MAX

+MVDDQ = +2.5V	Rt1	Rt2
1.25V	1K 3240100100	1K 3240100100
1.3V	1.0K 3240100100 603 3160100100 402	1.02K 3240102100



	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100

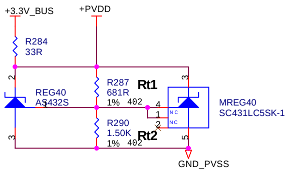


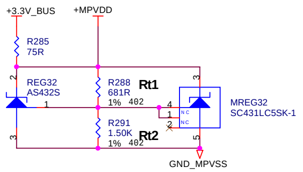
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX

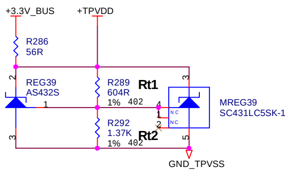
Alt regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX

Alt. regulator for +TPVDD
Vout = 1.65V ~ 1.85V
Iout = 20mA MAX

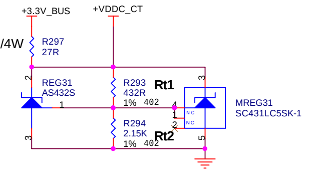
Alt regulator for +VDDC_CT
Vout = 1.5V
Iout = 70mA MAX







1206 1/4W



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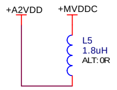
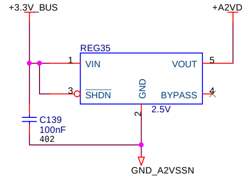
2.5V

120mA

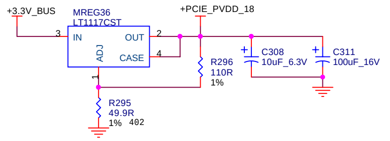


Alt. regulator for +A2VDD
Vout = 2.5V
Iout = 120mA MAX



+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.

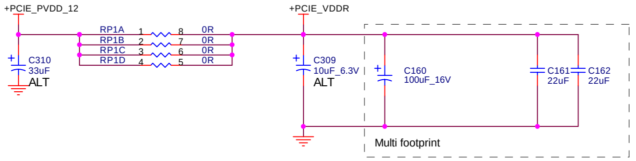
Alt. regulator for PCIE_PVDD_18
Vout = 1.85V
Iout = 500mA MAX



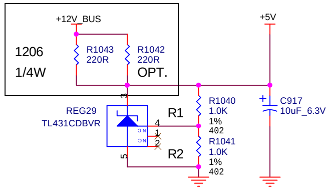
Need at least a 10uF Tant.
output cap for stability
Min. Load Current: 10mA

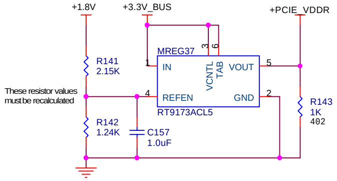
+PCIE_PVDD_12: 1.2V 250mA MAX

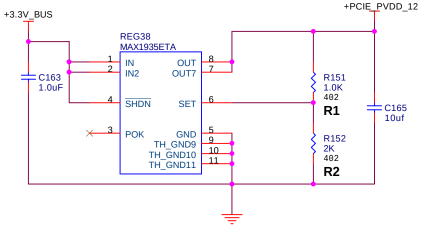
+PCIE_VDDR: 1.2V 1300mA MAX

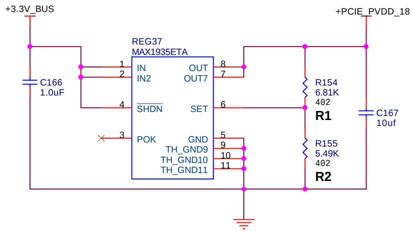


Regulator for +5V
Vout = 5V
Iout = 20mA MAX









Part	**Vout**	**R1**	**R2**
MAX1935 0.8V Ref	1.2V	1.00K 1% 402 ATI P/N 3160100100	2.00K 1% 402 ATI P/N 3160200100
	1.79V	6.81K 1% ATI P/N 3160681100	5.49K 1% 402 ATI P/N 3160549100

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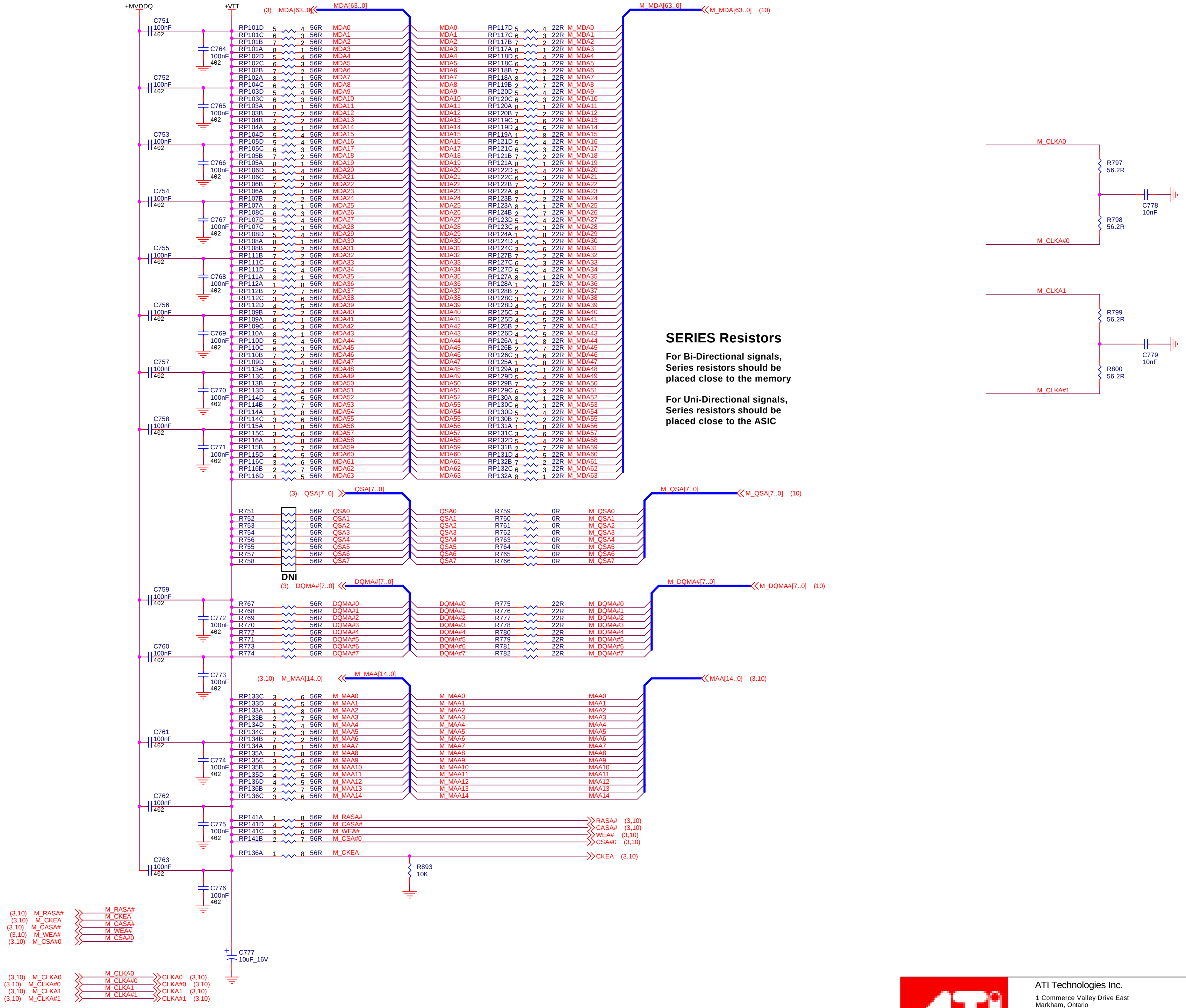

SERIES Resistors

For Bi-Directional signals,
Series resistors should be
placed close to the memory

For Uni-Directional signals,
Series resistors should be
placed close to the ASIC

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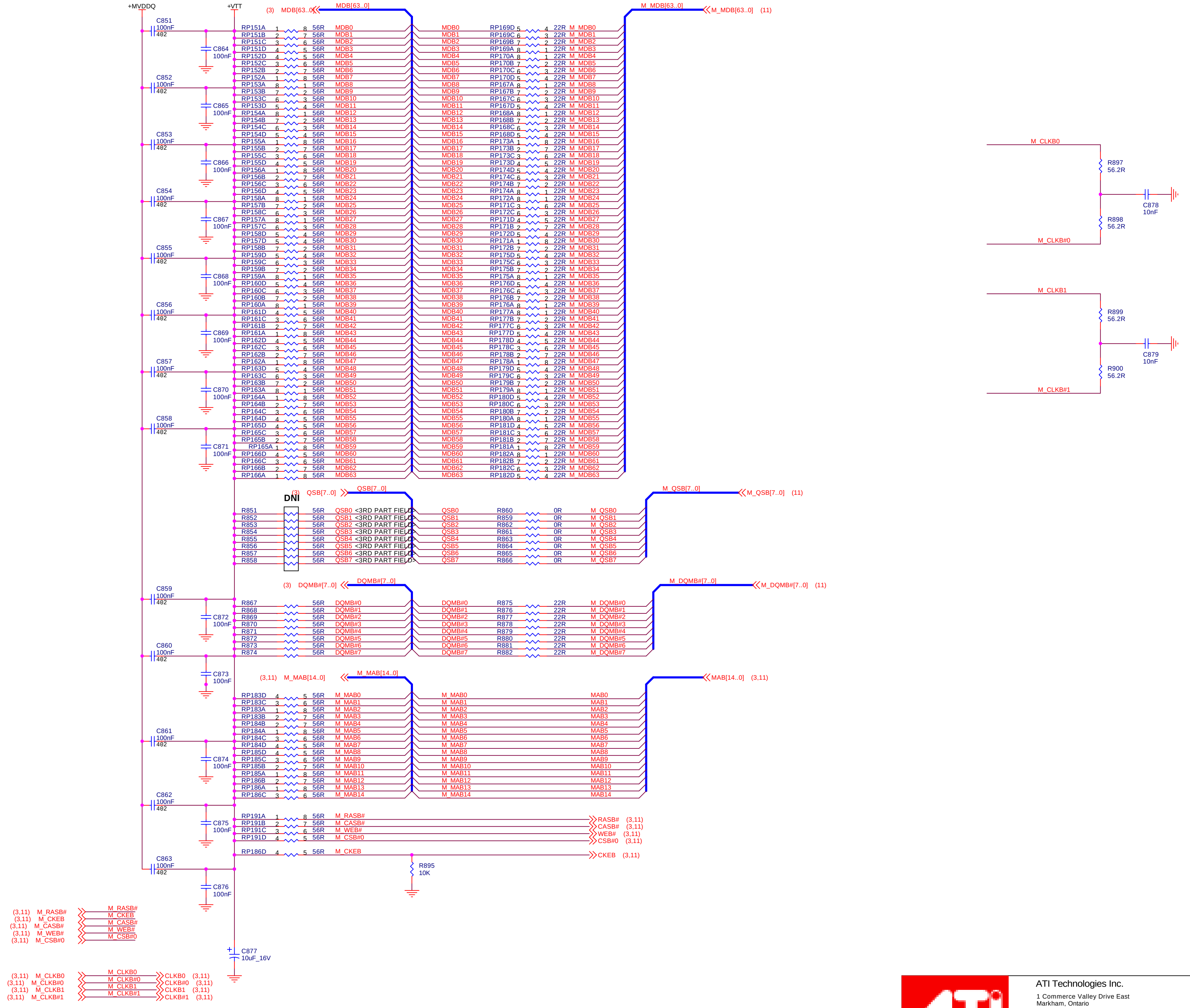

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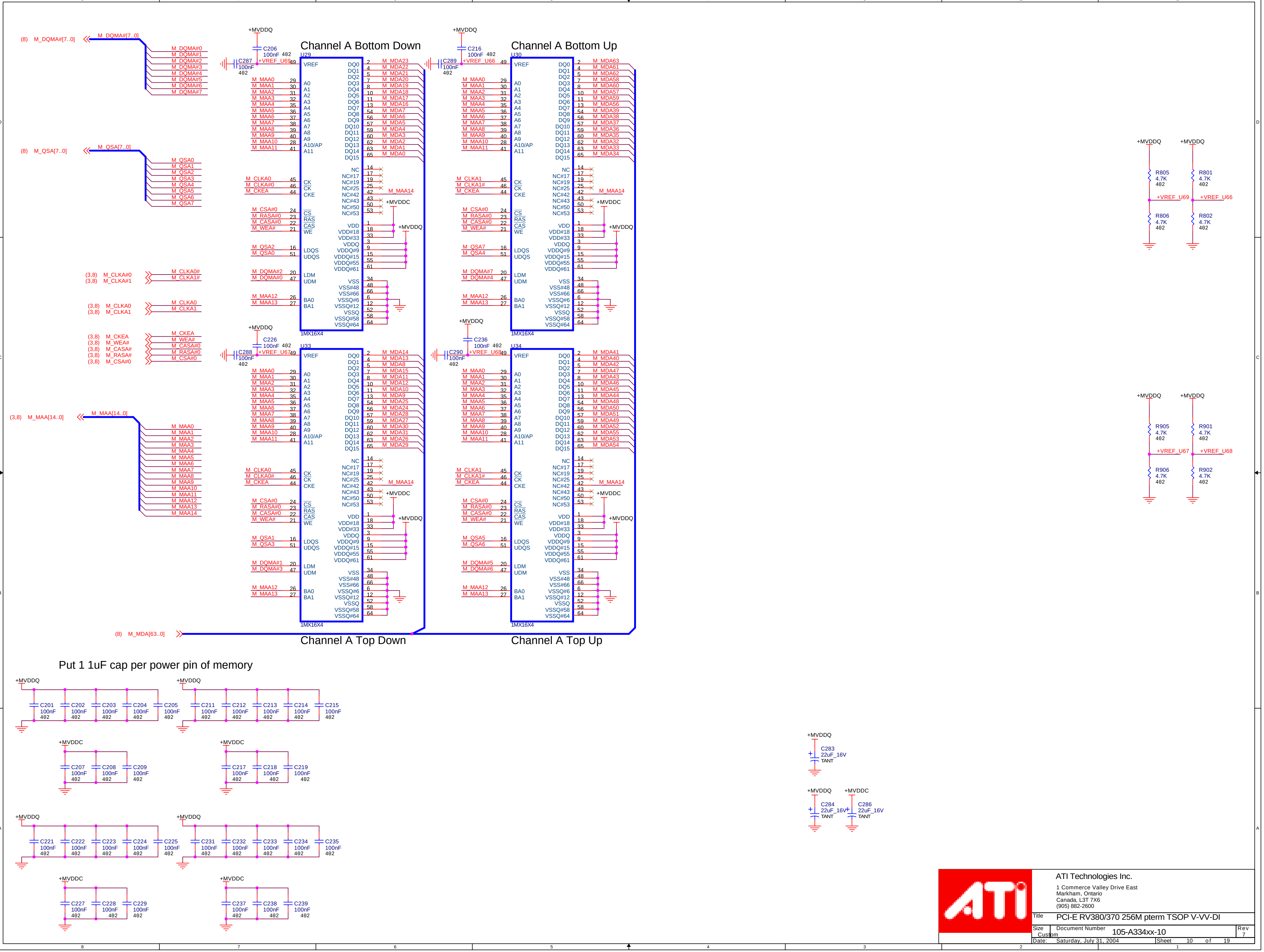

Channel A Bottom Down

Channel A Bottom Up

Channel A Top Down

Channel A Top Up

Put 1 1uF cap per power pin of memory

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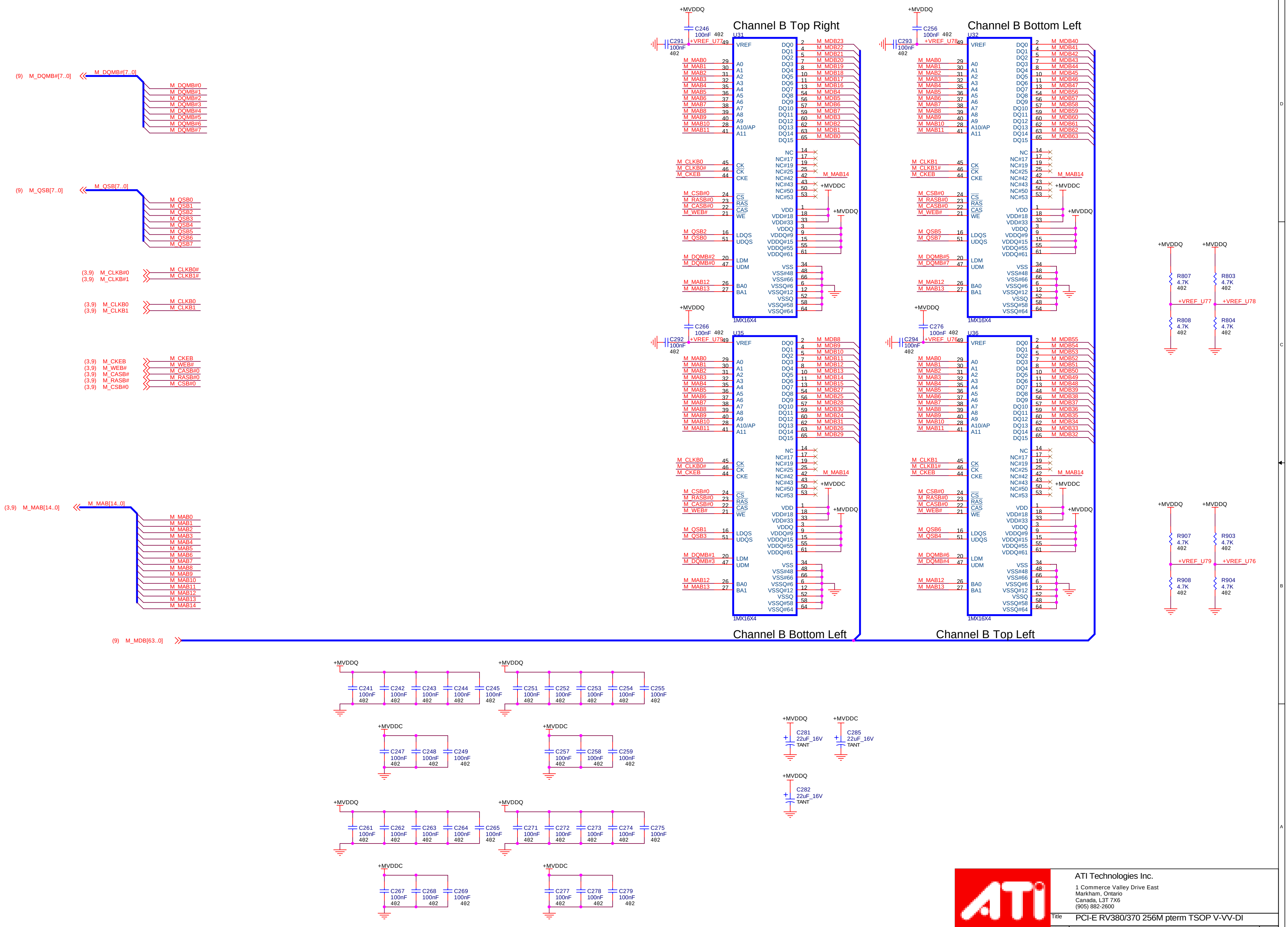

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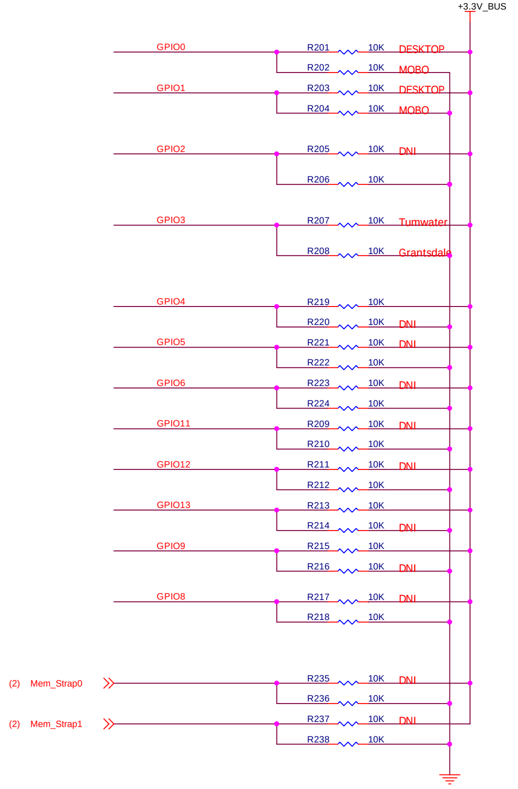
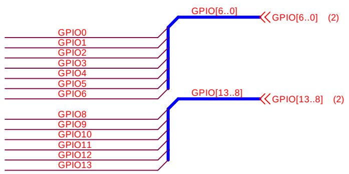
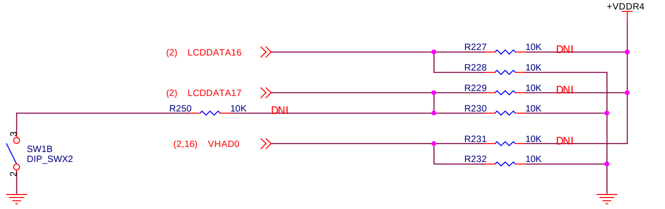
OPTION STRAPS





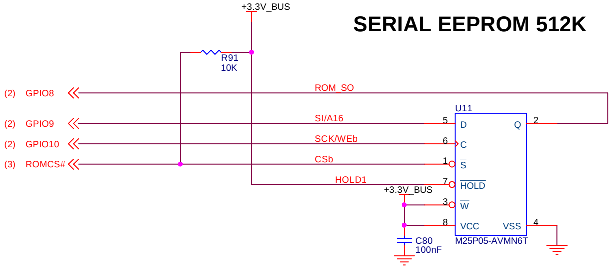
STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	



STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K



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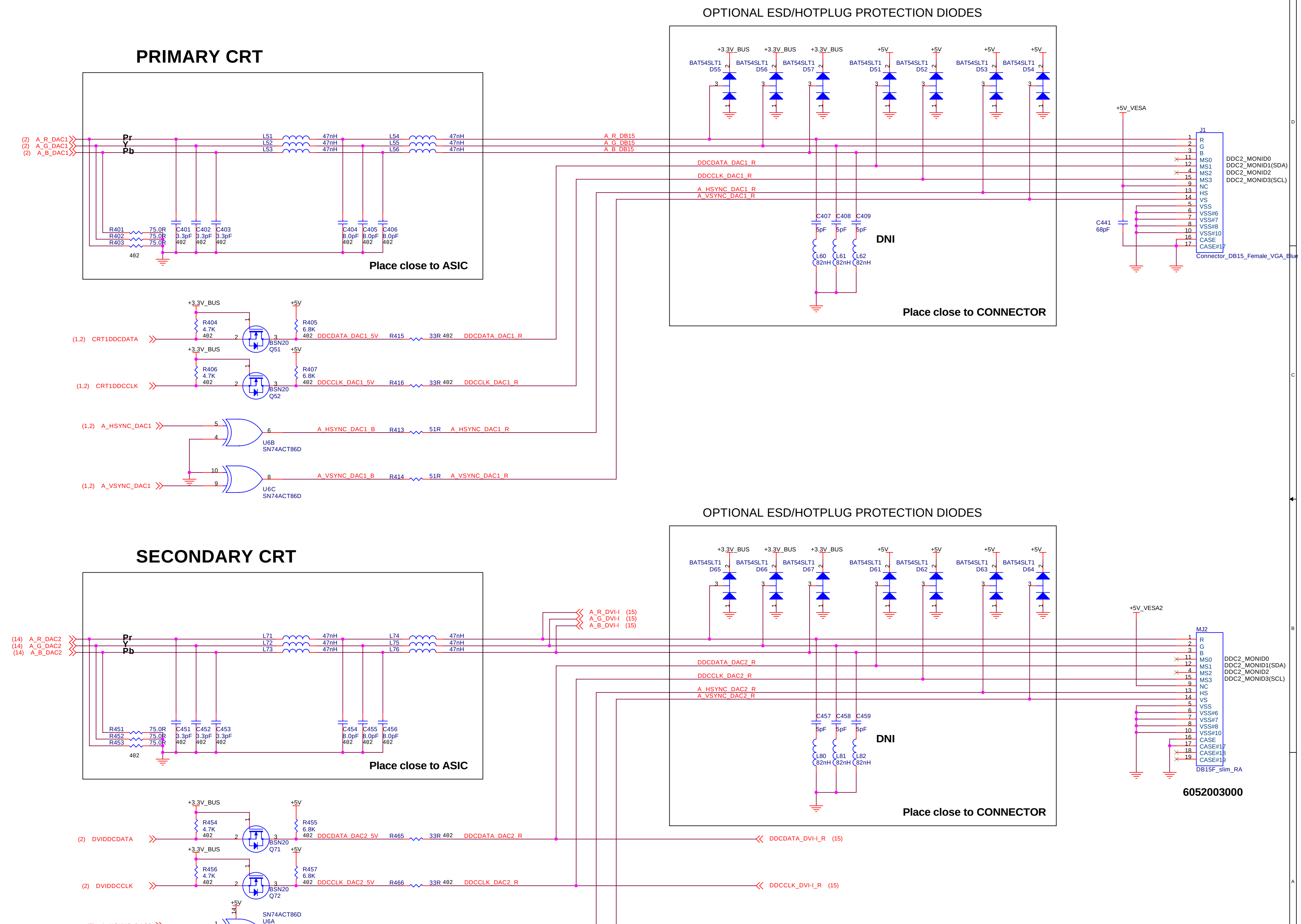

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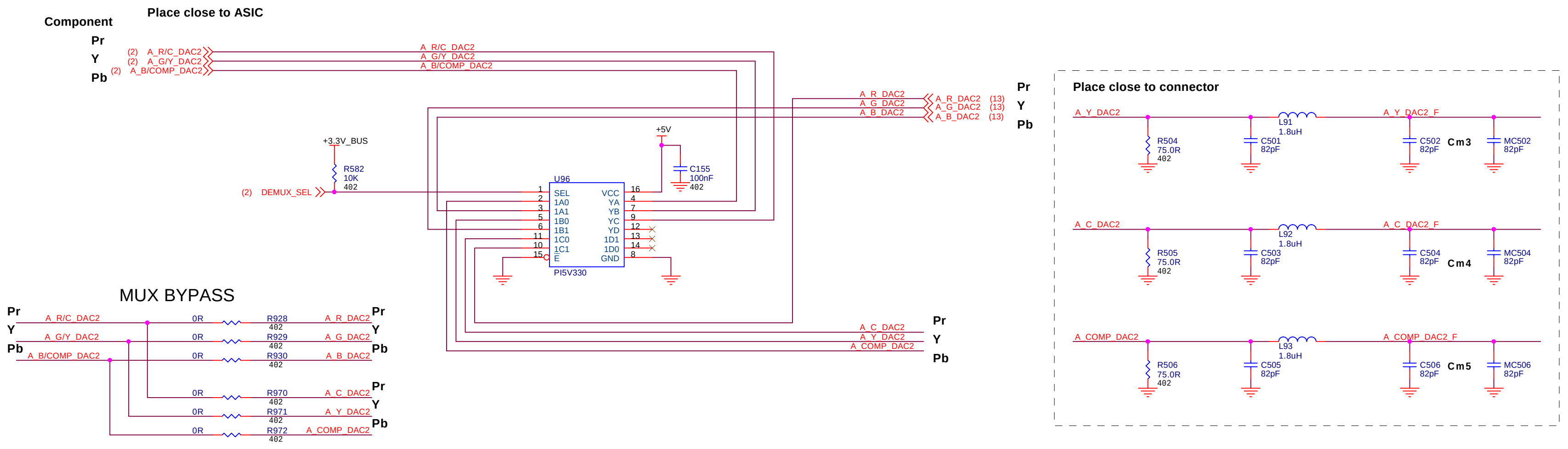
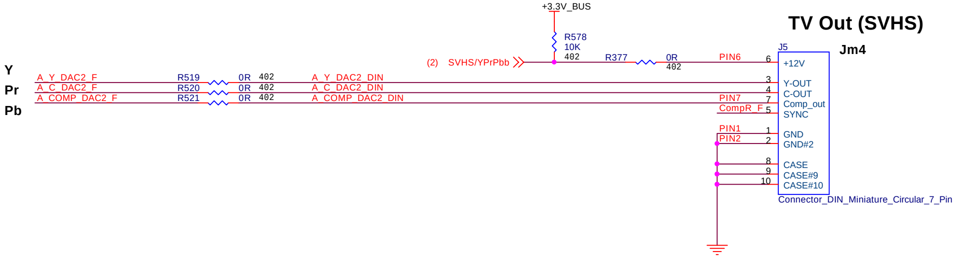
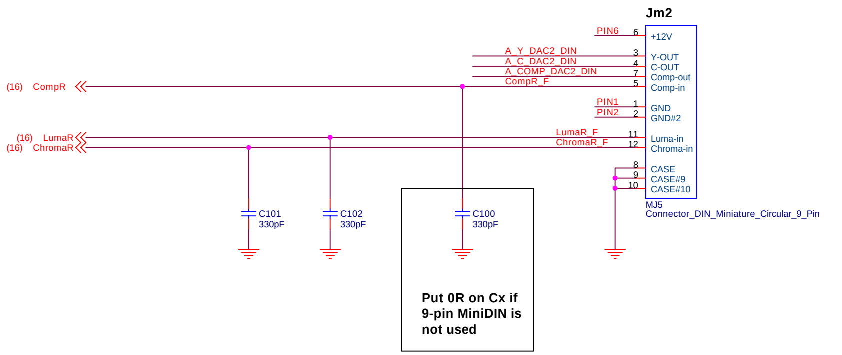


TV Out (SVHS)



VIVO MiniDIN 9-pin



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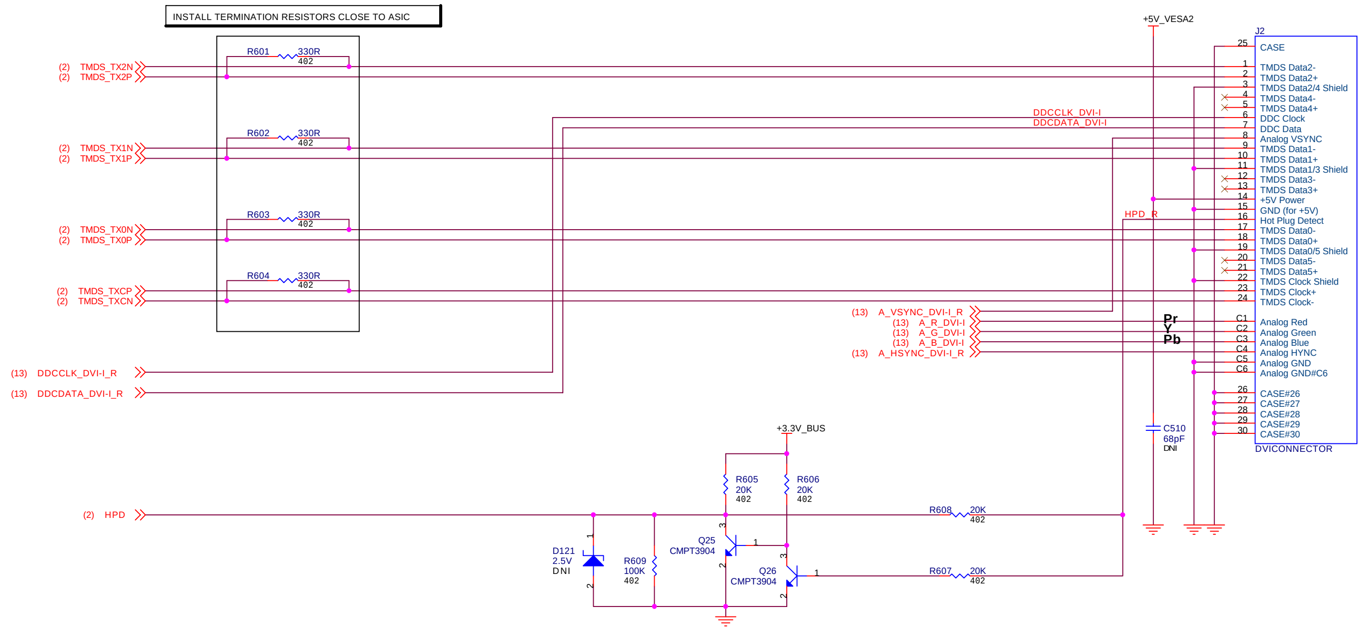
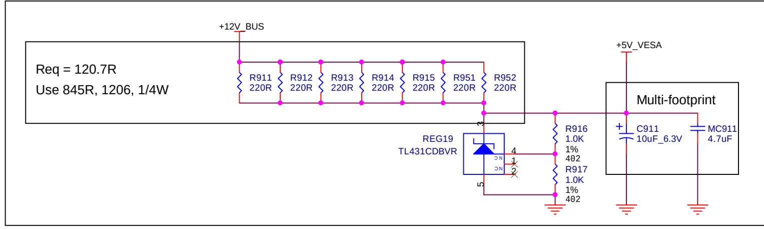
PRIMARY DVI-I CONNECTOR





Normal +5V regulated operation

This circuit provide upto 55mA

If Iload > 55mA, +5V will drop

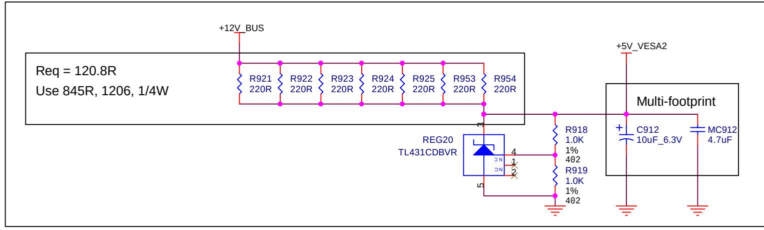
If Vout is shorted

Current across each Rx is 12V/845R = 14.2mA

Power dissipated by each Rx is 14.2mA x 12V = 171mW

Each Rx are rated 250mW (1/4W)

Derating 250mW by 70% is 175mW (1/4W)



Normal +5V regulated operation

This circuit provide upto 55mA

If Iload > 55mA, +5V will drop

If Vout is shorted

Current across each Rx is 12V/845R = 14.2mA

Power dissipated by each Rx is 14.2mA x 12V = 171mW

Each Rx are rated 250mW (1/4W)

Derating 250mW by 70% is 175mW (1/4W)

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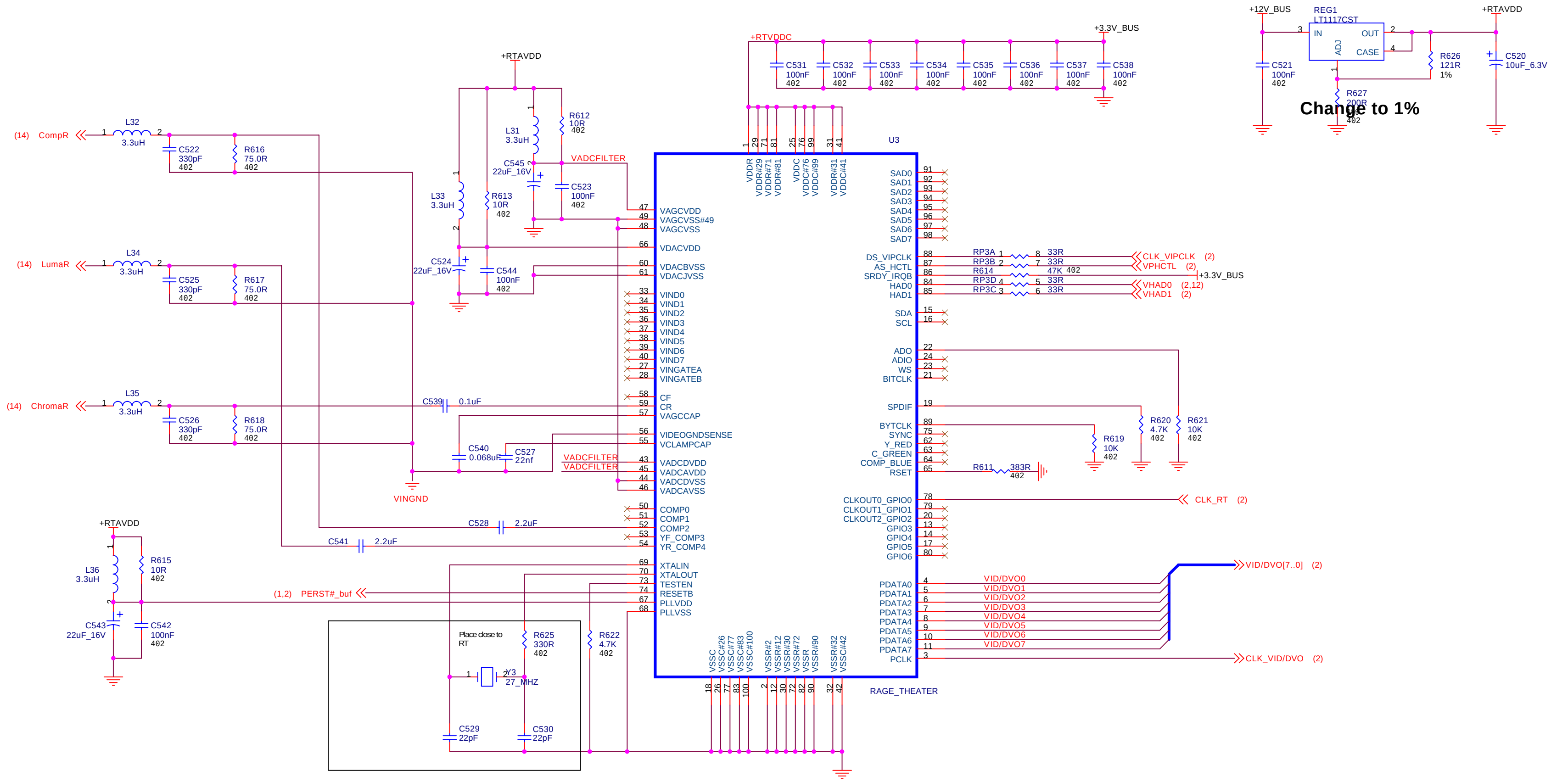
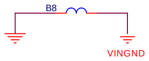
+RTAVDD
Vout = 3.3V
Iout = 125mA MAX, 80mA RMS

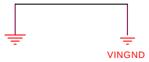


Footprint can be replaced with zero ohm or other.



IMPORTANT

Put 2D line as close as possible to pin 56 of Rage Theater



Layout Guide line of THEATER

#1 : C27 and C28 have to be placed as close as possible to the respective pins of Rage THEATER

#2 : VINGND should be seperated from Digital or Chassis Ground and have no loops

#3 : VINGND should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

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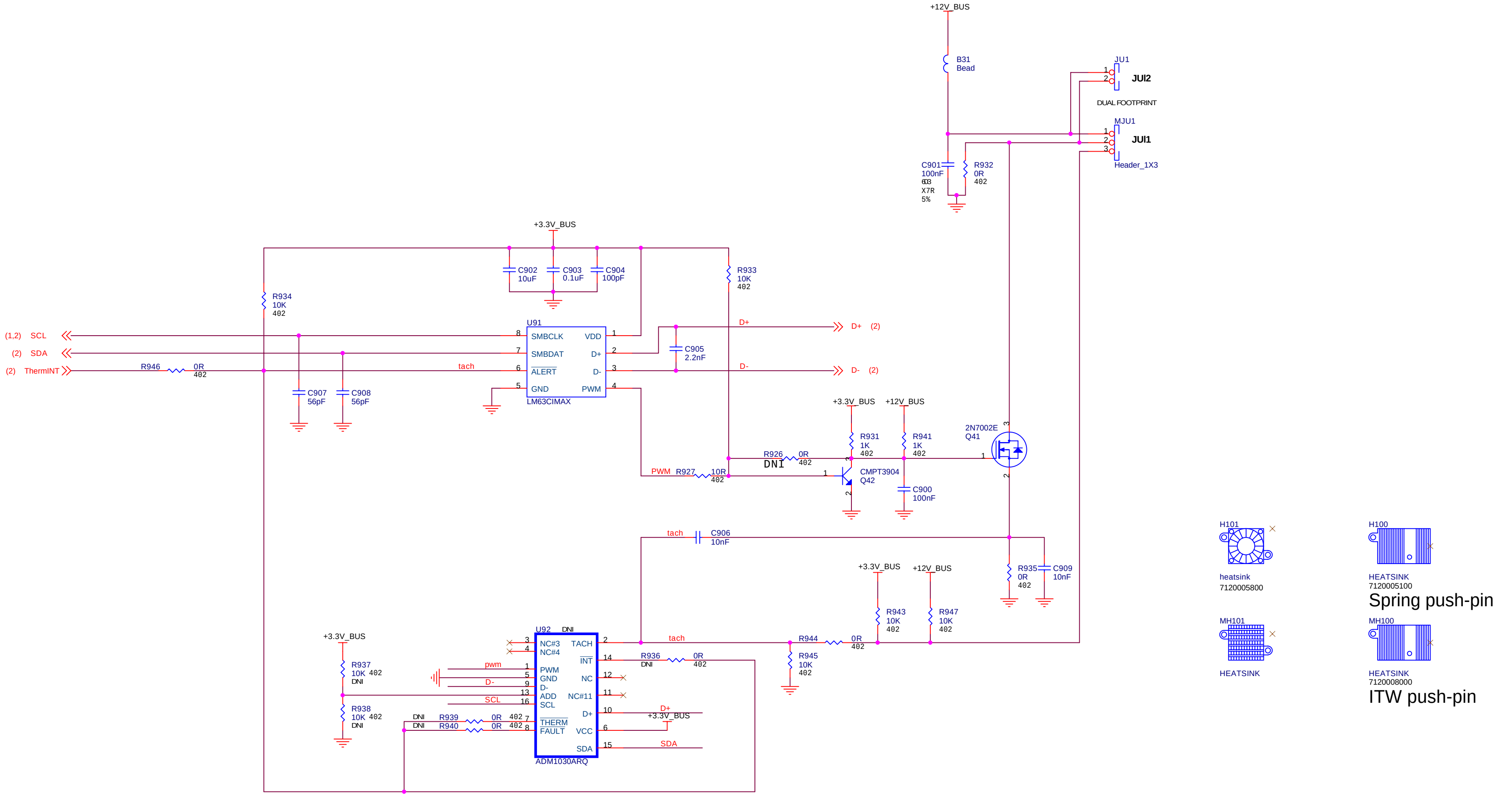
TEMPERATURE SENSE AND SPEED CONTROLLED FAN



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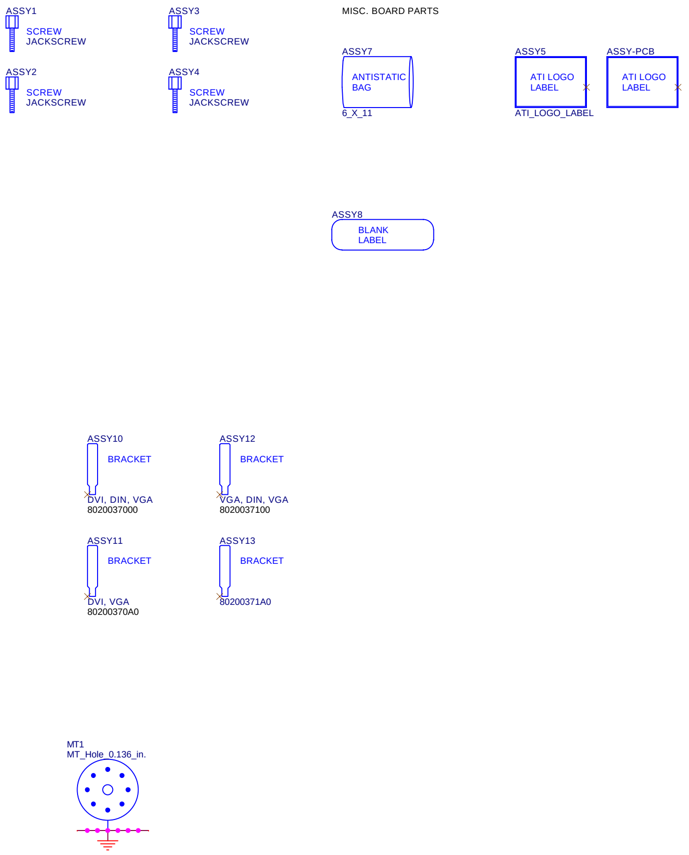
MISC. BOARD PARTS



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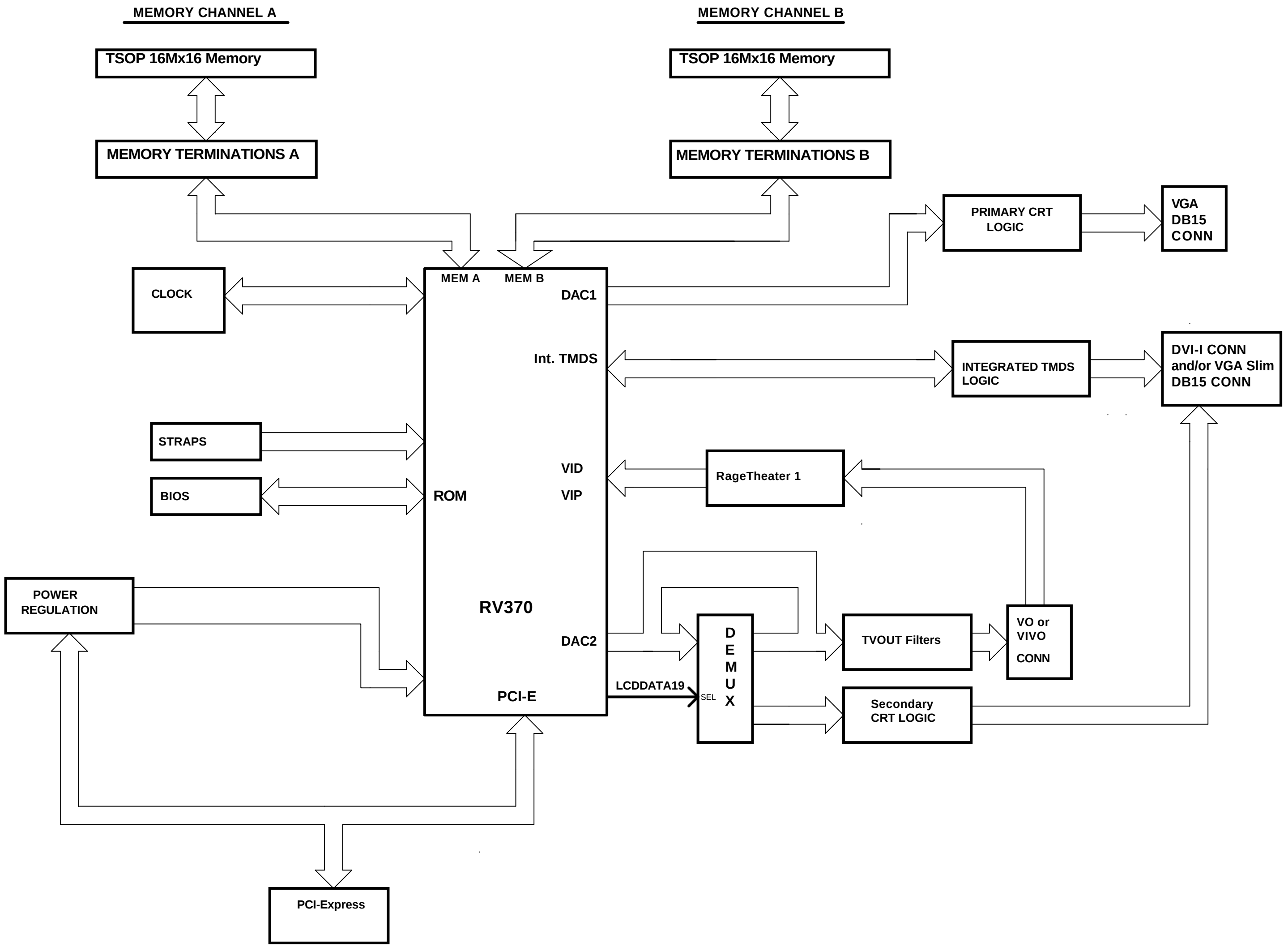

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