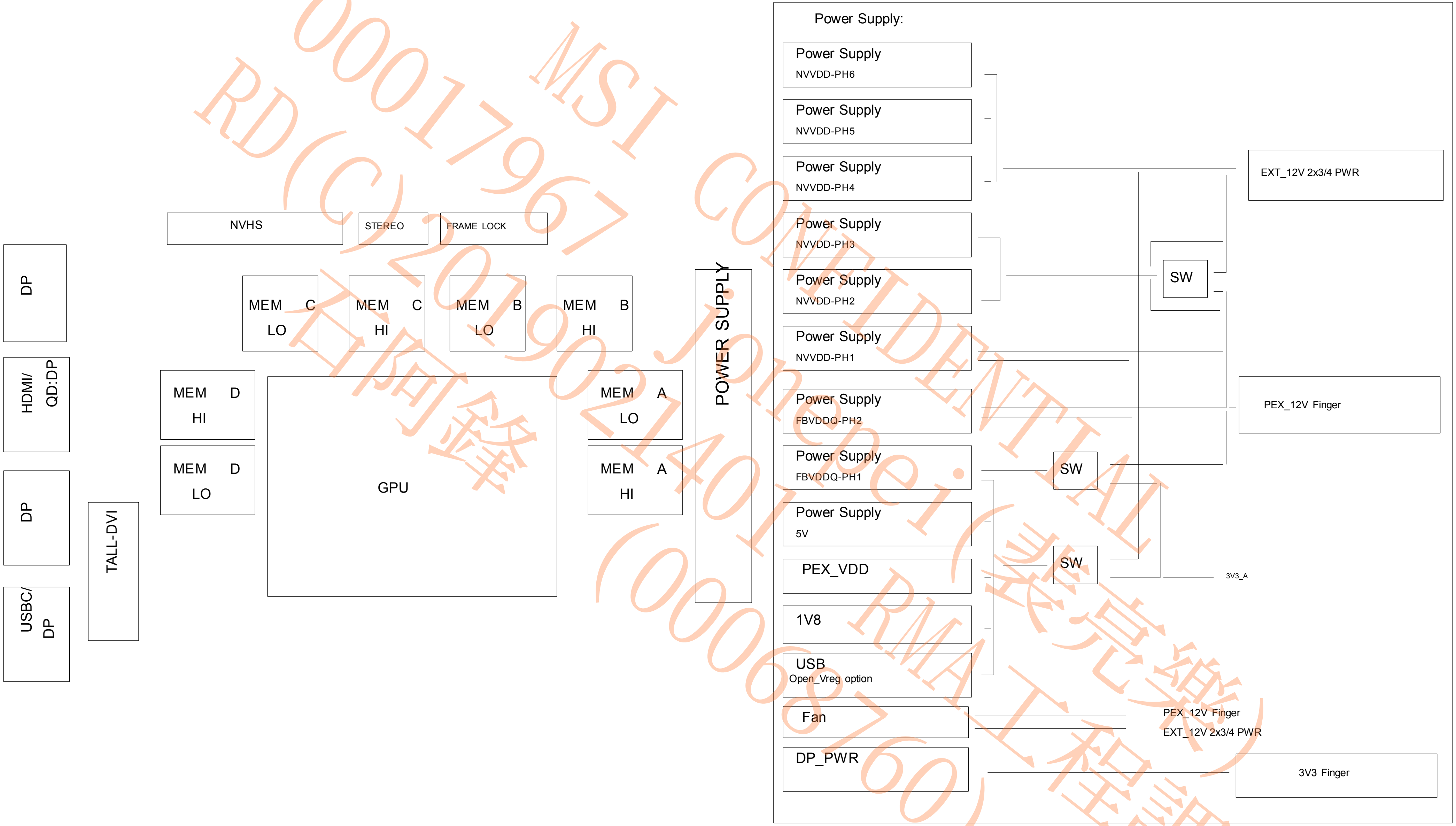
PG160-B02

8GB GDDR6, 256b, X16
Tall DVI-D + USBC/DP + DP + HDMI/DP + DP

TABLE OF CONTENTS

MICRO-STAR INT'L CO.,LTD
MS-V375
Size: Custom | Document Description: Table of Contents | Rev: 4.0
Date: Friday, November 09, 2018 | Sheet 1 of 54

Page2: Block Diagram



MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Document Description: Block Diagram	Rev: 4.0
Date: Friday, November 09, 2018	Sheet 2 of 54	

Page3: PCI Express

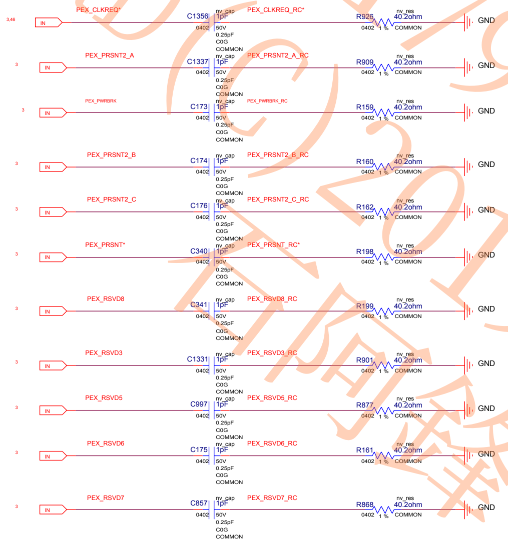
MICRO-STAR INT'L CO.,LTD

MS-V375

Size: Custom | Document Description: PCI Express | Rev 4.0

Date: Friday, November 09, 2018 | Sheet 3 of 54

Page4: PCIE RC TERM

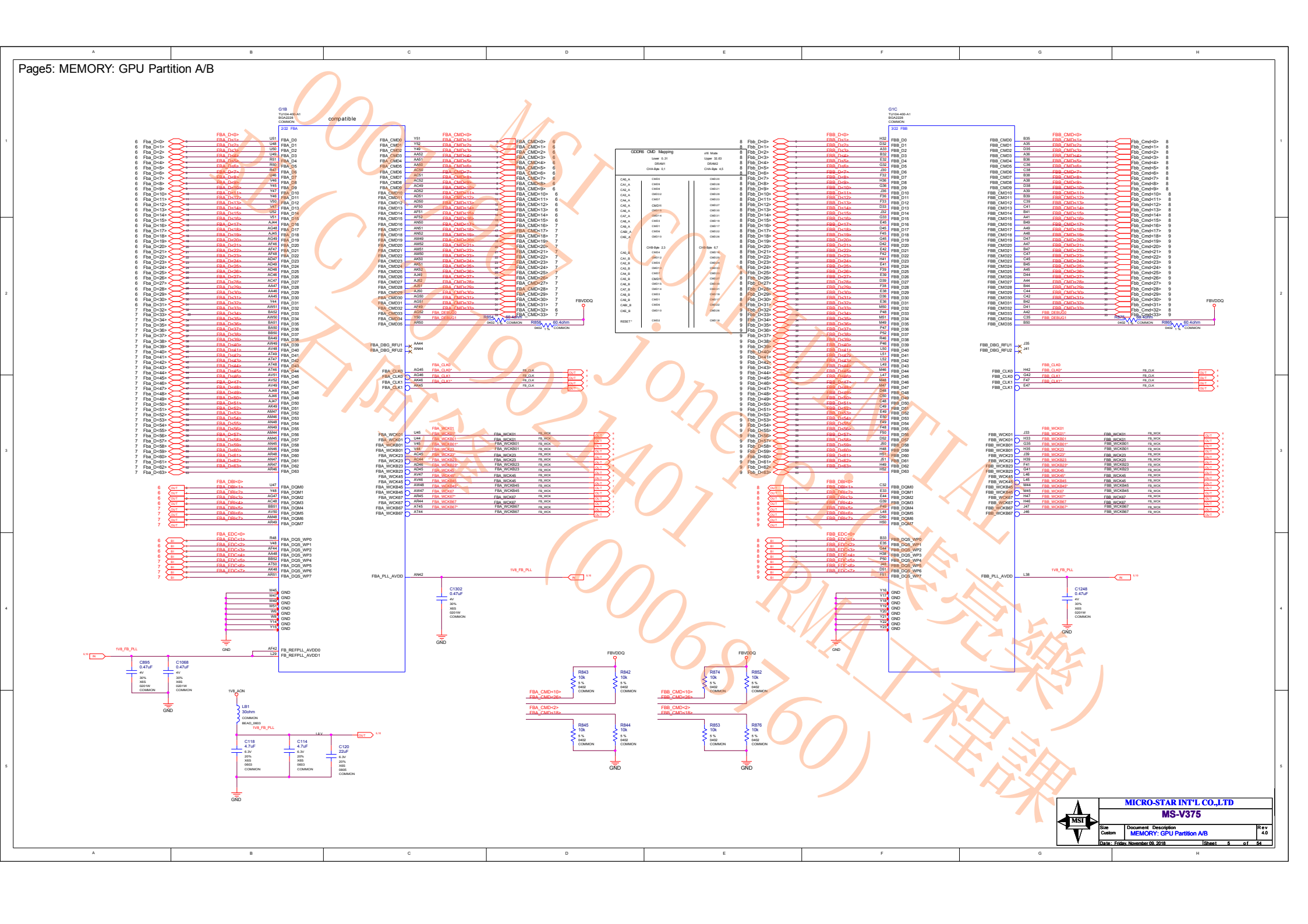


MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	PCI Termination	4.0

Date: Friday, November 09, 2018 Sheet 4 of 54


Page5: MEMORY: GPU Partition A/B
G1B
TU104-400-A1
BGA2228
COMMON
3/22 FBA
compatible
G1C
TU104-400-A1
BGA2228
COMMON
3/22 FBB
GDDR6 CMD Mapping
Lower 0..31
DRAM1
CHA-Byte 0,1
Upper 32..63
DRAM2
CHA-Byte 4,5
x16 Mode
CHB-Byte 2,3
CHB-Byte 6,7
FBVDDQ
1V8_FB_PLL
1V8_AON
GND
COMMON
MICRO-STAR INT'L CO.,LTD
MS-V375
Size
Custom
Document Description
MEMORY: GPU Partition A/B
Rev
4.0
Date: Friday, November 09, 2018
Sheet 5 of 54

Page6: MEMORY: FBA Partition 31..0

MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	MEMORY: FBA Partition 31..0	4.0

Date: Friday, November 09, 2018 | Sheet 6 of 54

Page7: MEMORY: FBA Partition 63..32

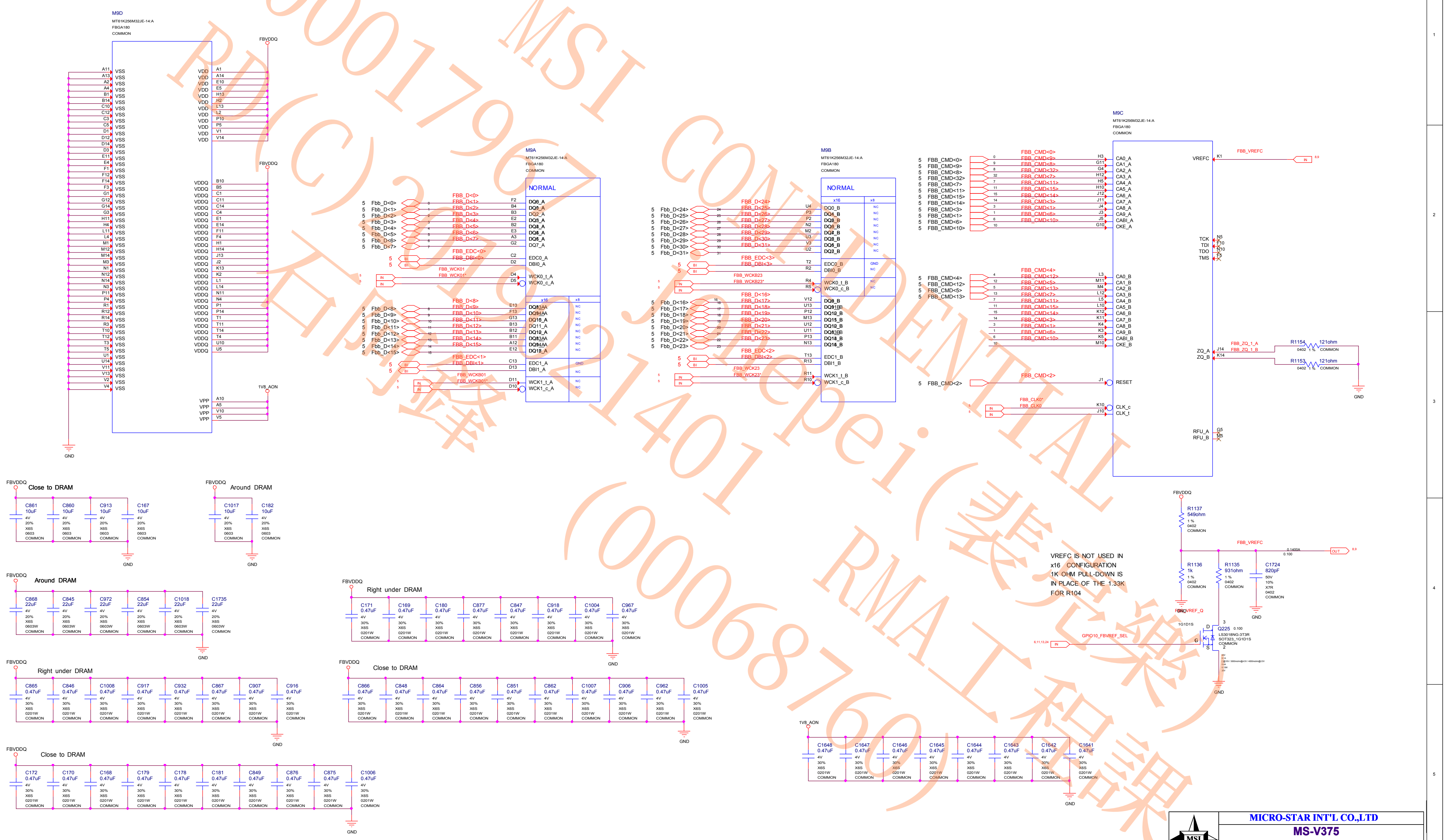
MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	MEMORY: FBA Partition 63..32	4.0

Date: Friday, November 09, 2018 Sheet 7 of 54

Page8: MEMORY: FBB Partition 31..0

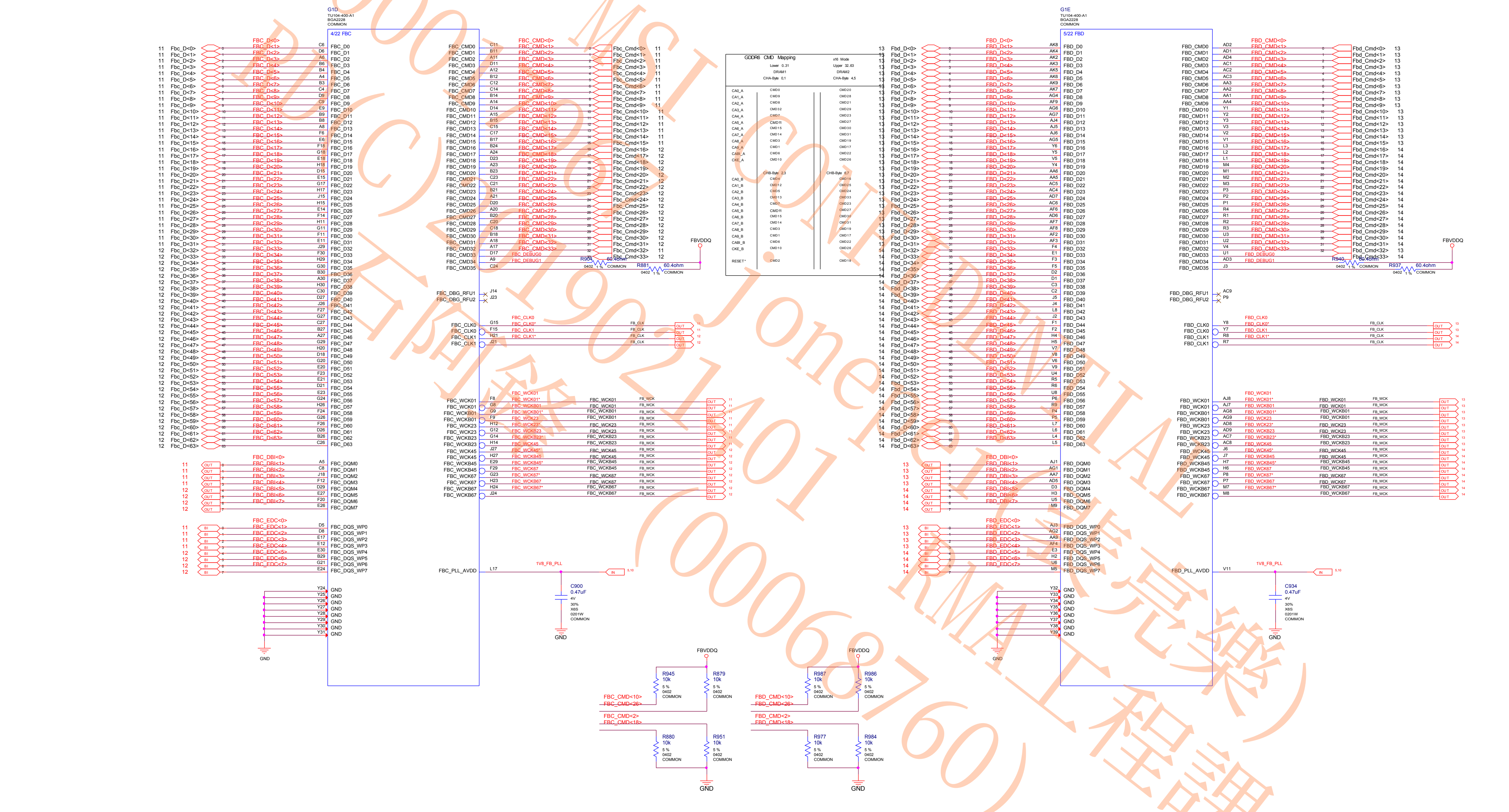


MICRO-STAR INT'L CO.,LTD	
MS-V375	
Size: Custom	Document Description: MEMORY: FBB Partition 31..0
Rev: 4.0	
Date: Friday, November 09, 2018	Sheet 8 of 54

Page9: MEMORY: FBB Partition 63..32

MICRO-STAR INT'L CO.,LTD
MS-V375
Size: Custom | Document Description: MEMORY: FBB Partition 63..32 | Rev 4.0
Date: Friday, November 09, 2018 | Sheet 9 of 54

Page10: MEMORY: GPU Partition C/D



MICRO-STAR INT'L CO.,LTD	
MS-V375	
Size: Custom	Document Description: MEMORY: GPU Partition C/D	Rev 4.0
Date: Friday, November 09, 2018	Sheet 10 of 54

Page11: MEMORY: FBC Partition 31..0

MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Document Description: MEMORY: FBC Partition 31..0	Rev 4.0
Date: Friday, November 09, 2018	Sheet 11 of 54	

Page12: MEMORY: FBC Partition 63..32

MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	MEMORY: FBC Partition 63..32	4.0

Date: Friday, November 09, 2018 Sheet 12 of 54

Page13: MEMORY: FBD Partition 31..0

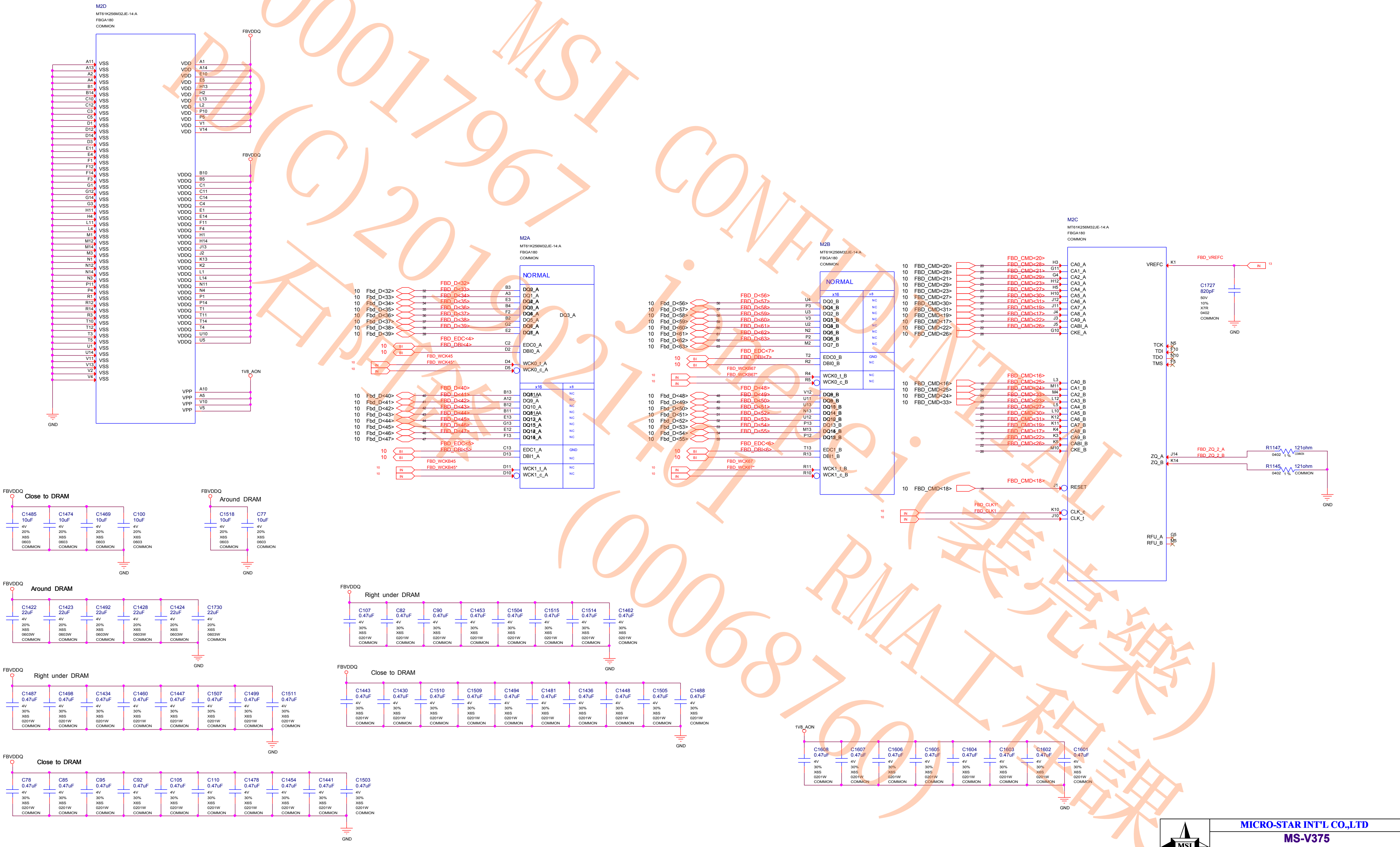
MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	MEMORY: FBD Partition 31..0	4.0

Date: Friday, November 09, 2018 Sheet 13 of 54

Page14: MEMORY: FBD Partition 63..32



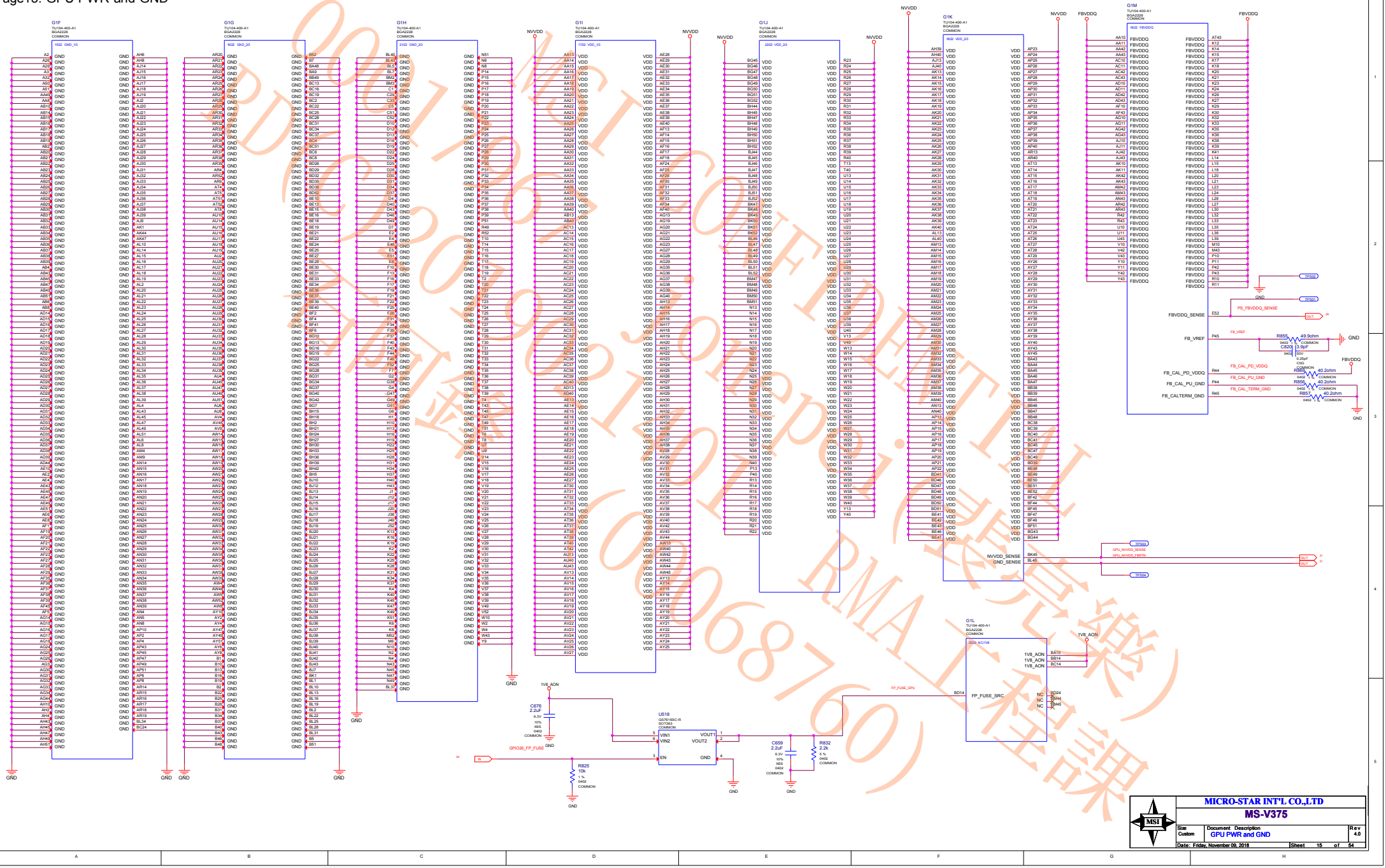
MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	MEMORY: FBD Partition 63..32	4.0

Date: Friday, November 09, 2018 Sheet 14 of 54

Page15: GPU PWR and GND



Page16: GPU Decoupling 1

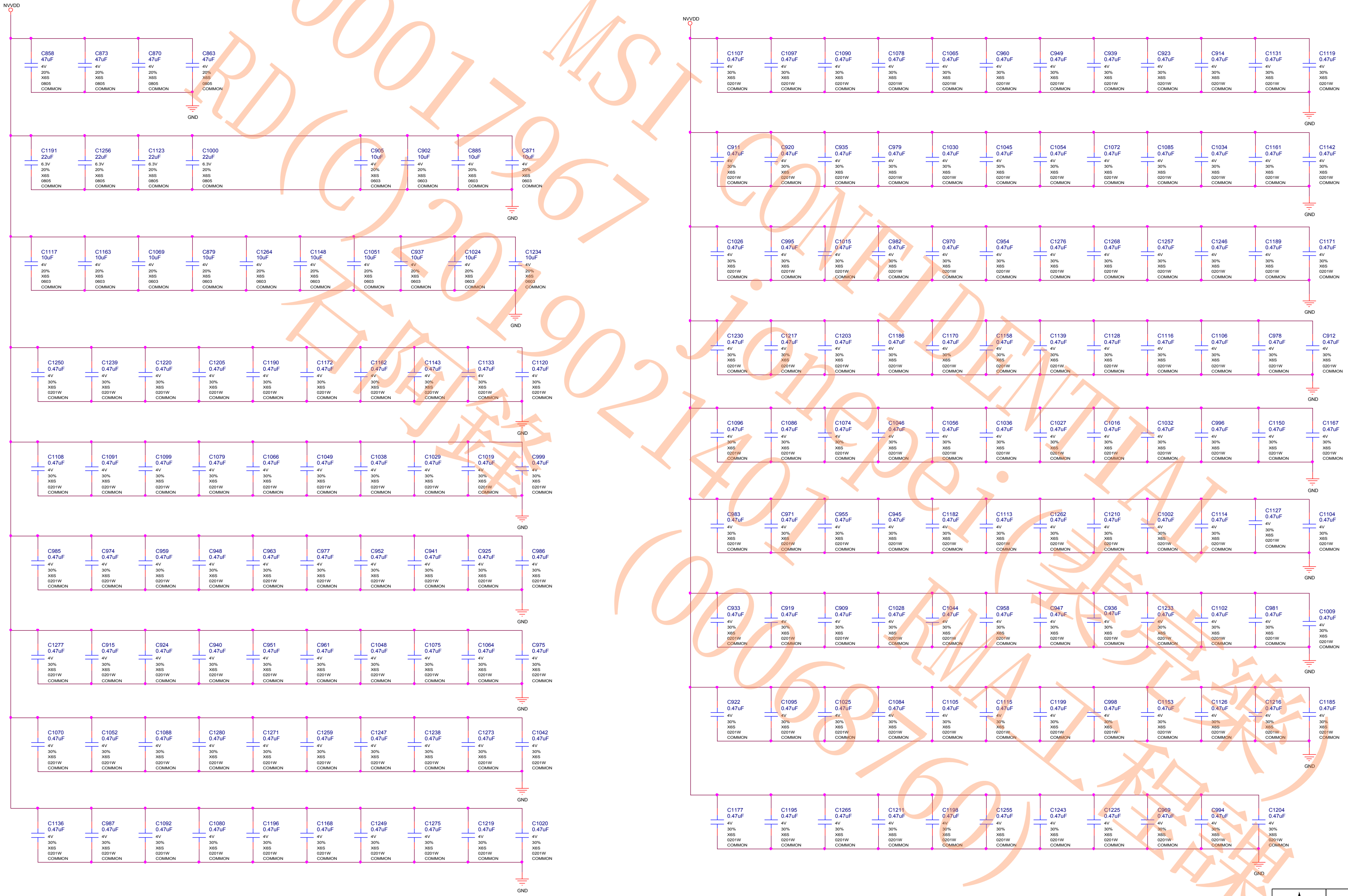
MICRO-STAR INT'L CO.,LTD
MS-V375

Size	Document Description	Rev
Custom	GPU Decoupling	4.0

Date: Friday, November 09, 2018 | Sheet 16 of 54

Page17: GPU Decoupling 2

NVVDD



MICRO-STAR INT'L CO.,LTD

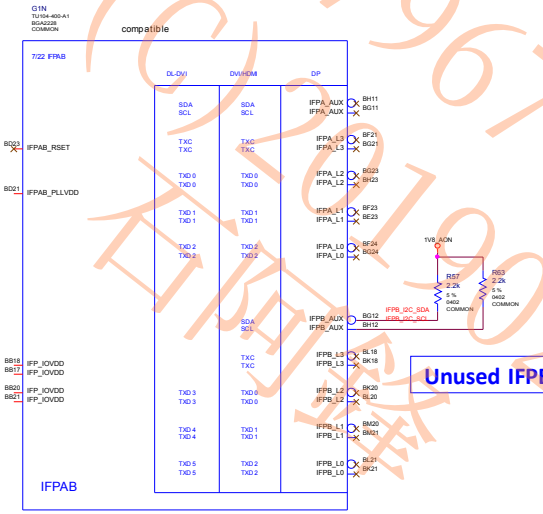
MS-V375

Size	Document Description	Rev
Custom	GPU Decoupling	4.0

Date: Friday, November 09, 2018 Sheet 17 of 54

Page18: IFPAB DVI-D-DL

delete Link AB ◦



Unused IFPB_I2C* leaving Pull high resistor to 1.8V ◦

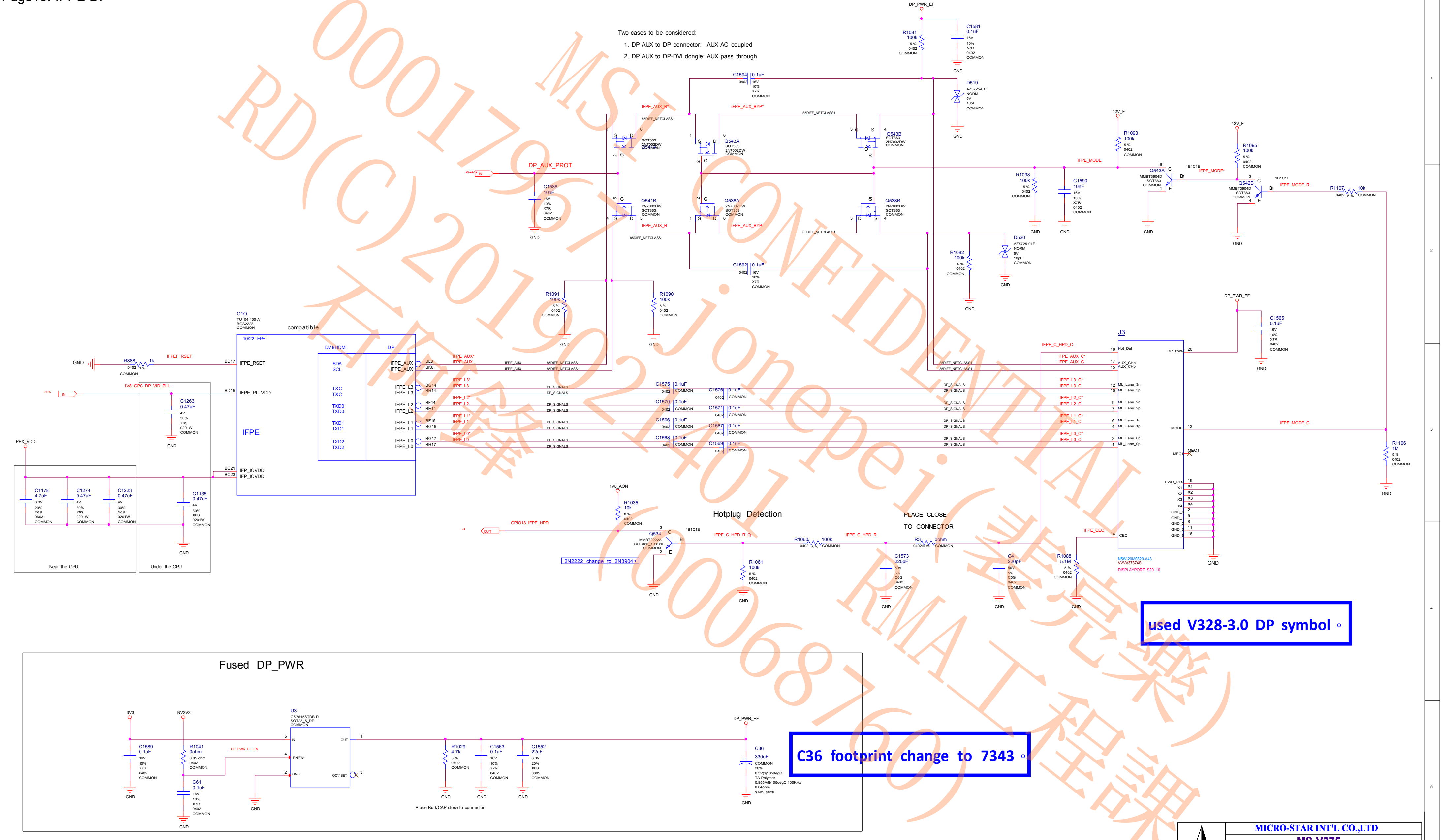
9.3 UNUSED PINS

If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF) can be left unconnected if neither of IFPx /IFPy is in use. For example, If neither link of the IFPA/IFPB macro is to be used, then IFPAB_PLLVDD and IFPAB_RSET should be left disconnected, and all signals and references associated with Link A and Link B should also be left unconnected.

IFP_IOVDD rail can be unconnected if no IFP link is used.If any IFP is used, all IFP_IOVDD balls must be connected to power rail.

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
Size: Custom	Document Description: IFPAB DVI-D-DL	Rev: 4.0
Date: Friday, November 09, 2018	Sheet 18 of 54	

Page19: IFPE DP



MICRO-STAR INT'L CO.,LTD

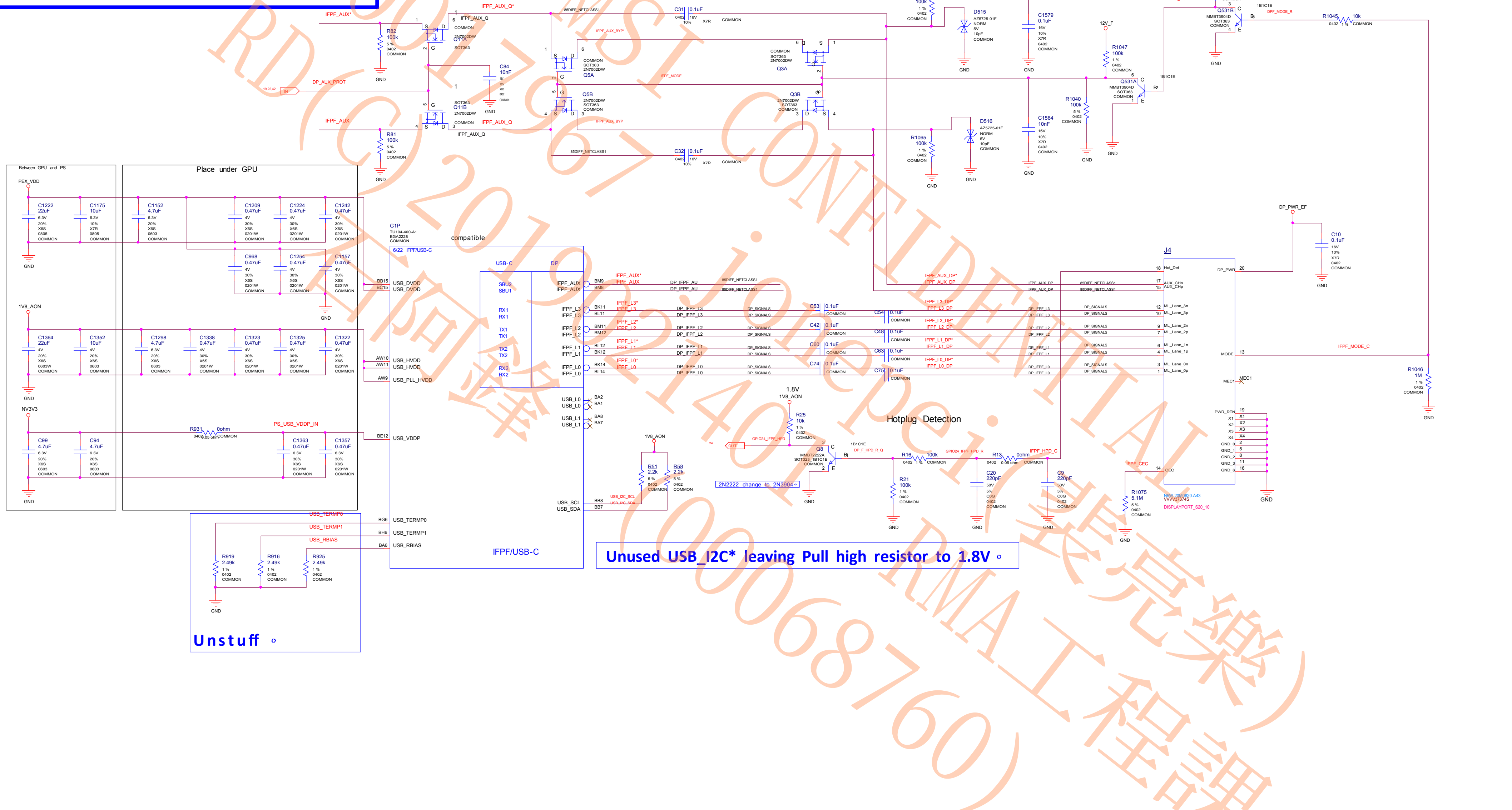
MS-V375

Size	Document Description	Rev
Custom	IFPE DP	4.0

Date: Friday, November 09, 2018 Sheet 19 of 54

Page20: IFPF USB-C

1 .used V328-3 0 DP symbol stuff ed DP MI。
2 .delete USB C。



MICRO-STAR INT'L CO.,LTD

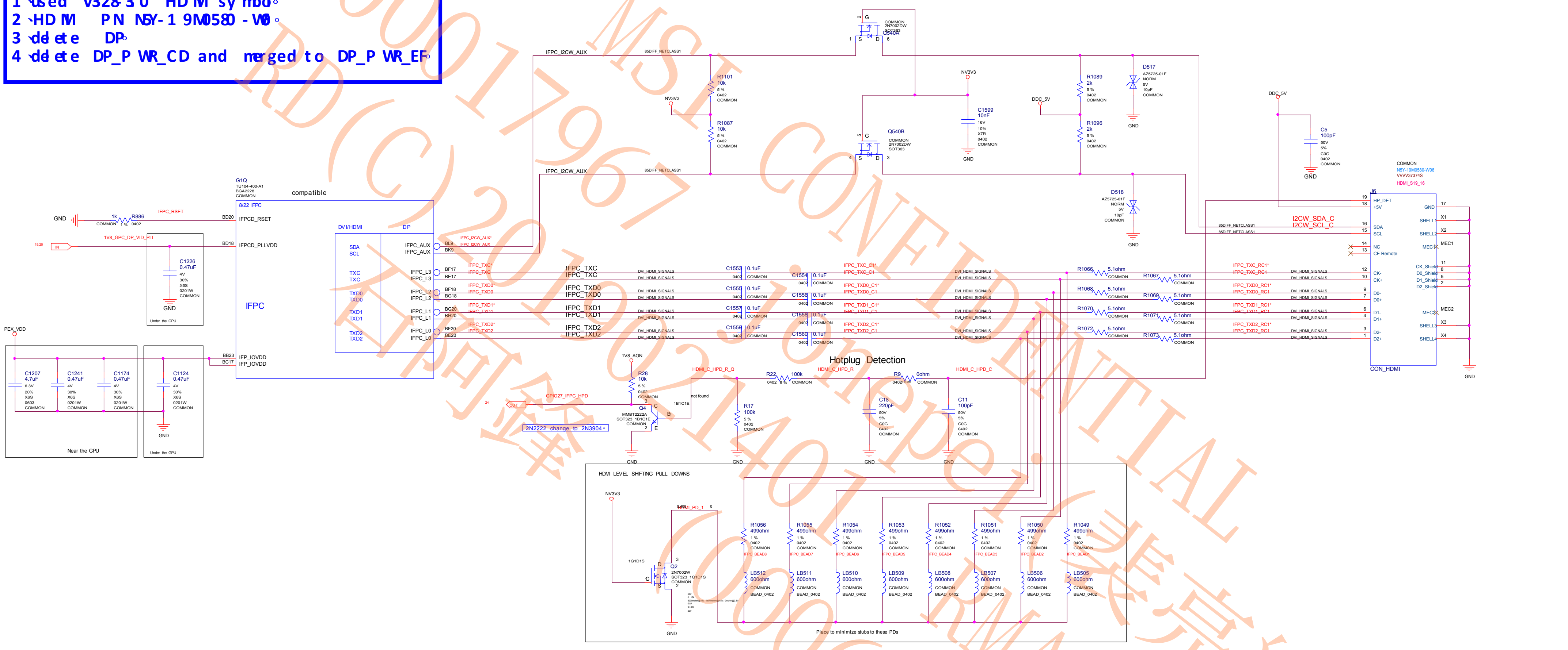
MS-V375

Size	Document Description	Rev
Custom	IFPF USBC	4.0
Date: Friday, November 09, 2018	Sheet 20 of 54	

21-JUN-2018

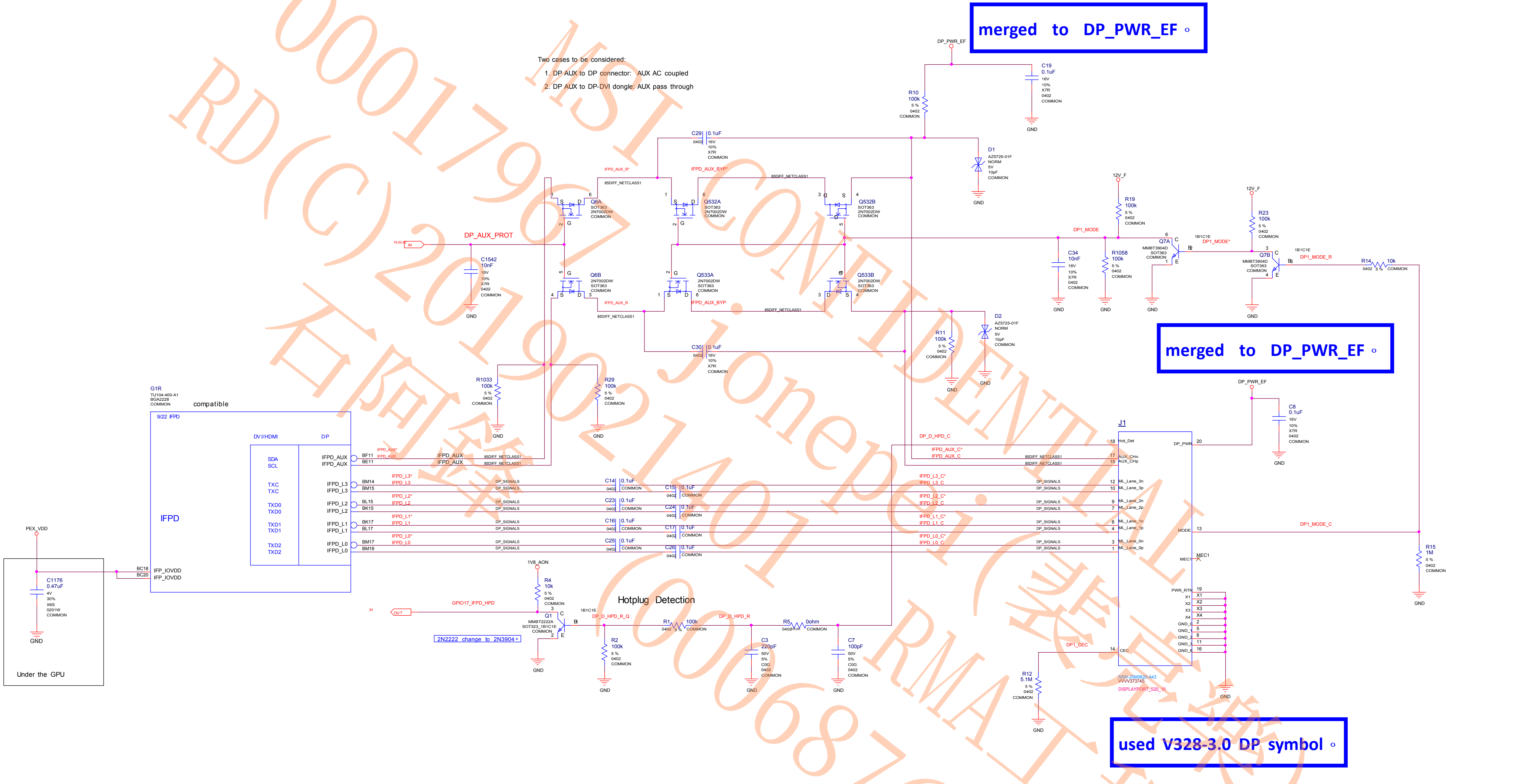
Page21: IFPC HDMI/DP

1 used V328-3 0 HDMI symbol。
2 HDMI PN N5Y-19M0580-W0。
3 delete DP。
4 delete DP_PWR_CD and merged to DP_PWR_EF。



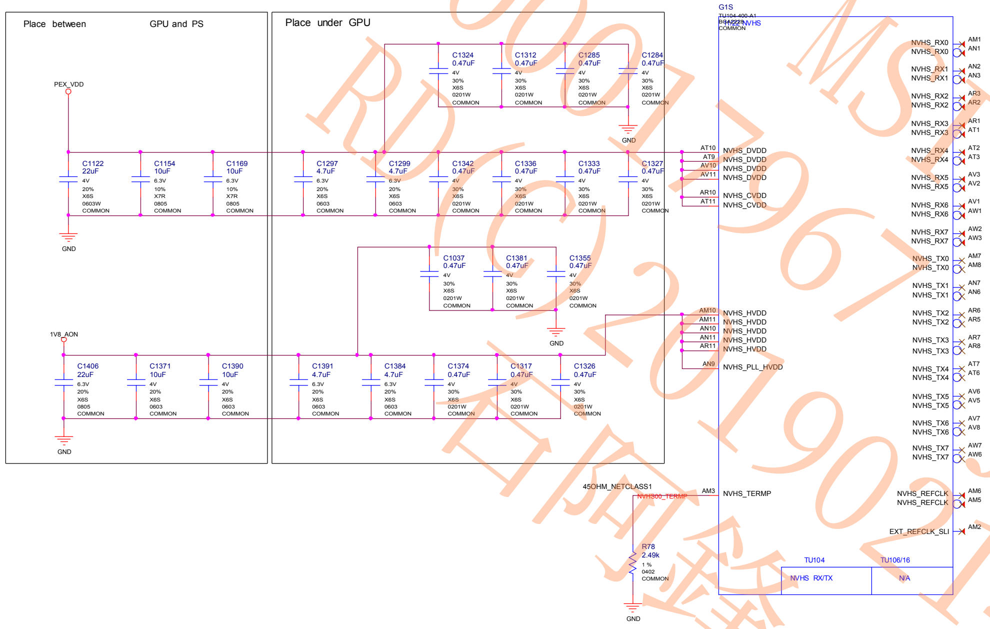
MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Document Description: IFPC HDMI 2.0	Rev: 4.0
Date: Friday, November 09, 2018	Sheet 21 of 54	

Page22: IFPD DP



MICRO-STAR INT'L CO.,LTD			
MS-V375			
Size: Custom	Document Description: IFPD DP		Rev 4.0
Date: Friday, November 09, 2018		Sheet 22 of 54	

Page23: NVHS Interface and Frame Lock



delete Frame Lock。

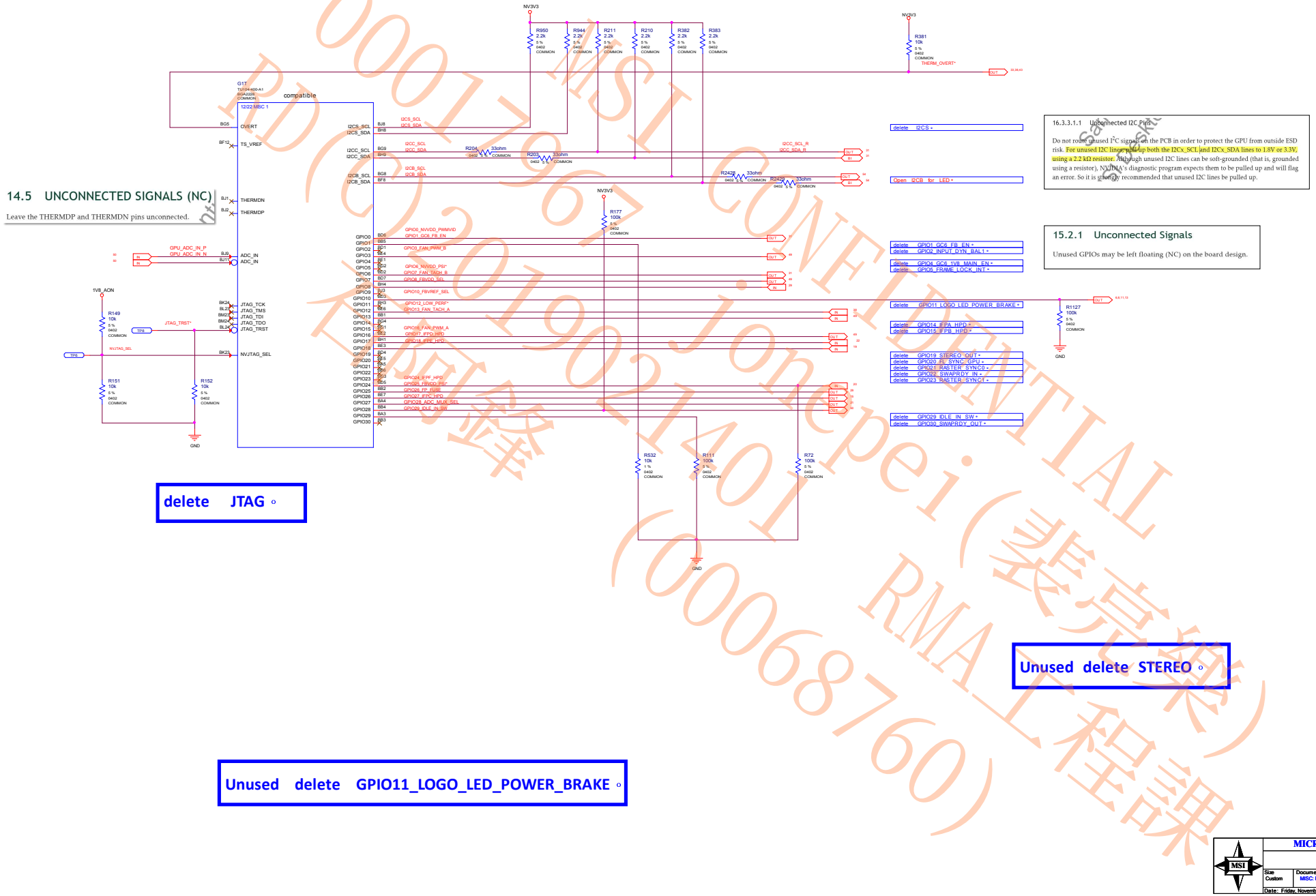
MICRO-STAR INT'L CO.,LTD

MS-V375

Size: Custom | Document Description: NVHS Interface | Rev 4.0

Date: Friday, November 09, 2018 | Sheet 23 of 54

Page24: MISC1: Fan, Thermal, JTAG, GPIO



14.5 UNCONNECTED SIGNALS (NC)

Leave the THERMDP and THERMDN pins unconnected.

16.3.3.1.1 Unconnected I2C Pins

Do not route unused I^2C signals on the PCB in order to protect the GPU from outside ESD risk. For unused I2C lines, pull up both the I2Cx_SCL and I2Cx_SDA lines to 1.8V or 3.3V, using a 2.2 kΩ resistor. Although unused I2C lines can be soft-grounded (that is, grounded using a resistor), NVDIA's diagnostic program expects them to be pulled up and will flag an error. So it is strongly recommended that unused I2C lines be pulled up.

15.2.1 Unconnected Signals

Unused GPIOs may be left floating (NC) on the board design.

delete JTAG ◦

Unused delete STEREO ◦

Unused delete GPIO11_LOGO_LED_POWER_BRAKE ◦

MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Document Description: MISC: Fan, Thermal, JTAG, GPIO, STEREO	Rev: 4.0
Date: Friday, November 09, 2018	Sheet 24 of 54	

Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

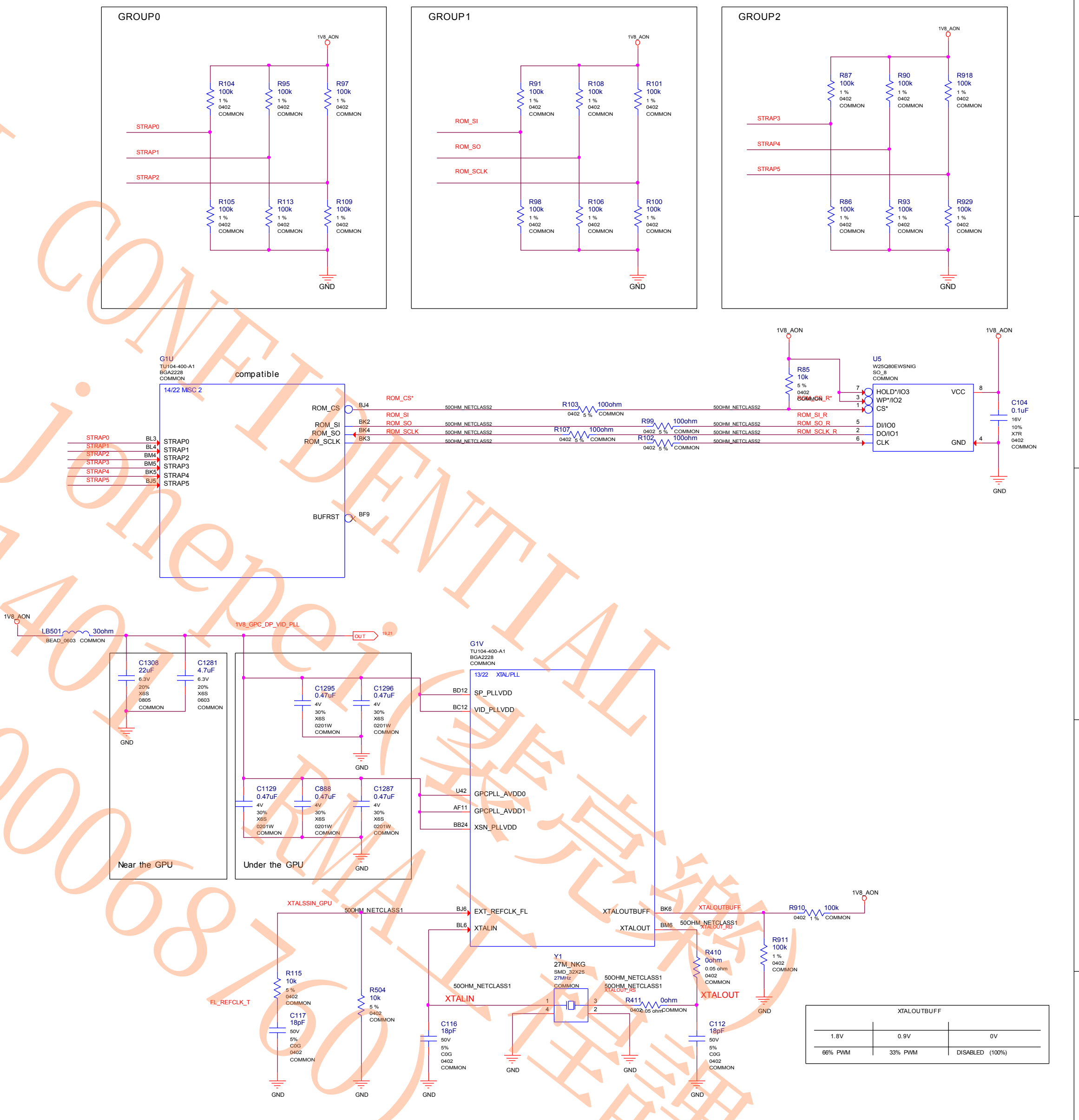
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

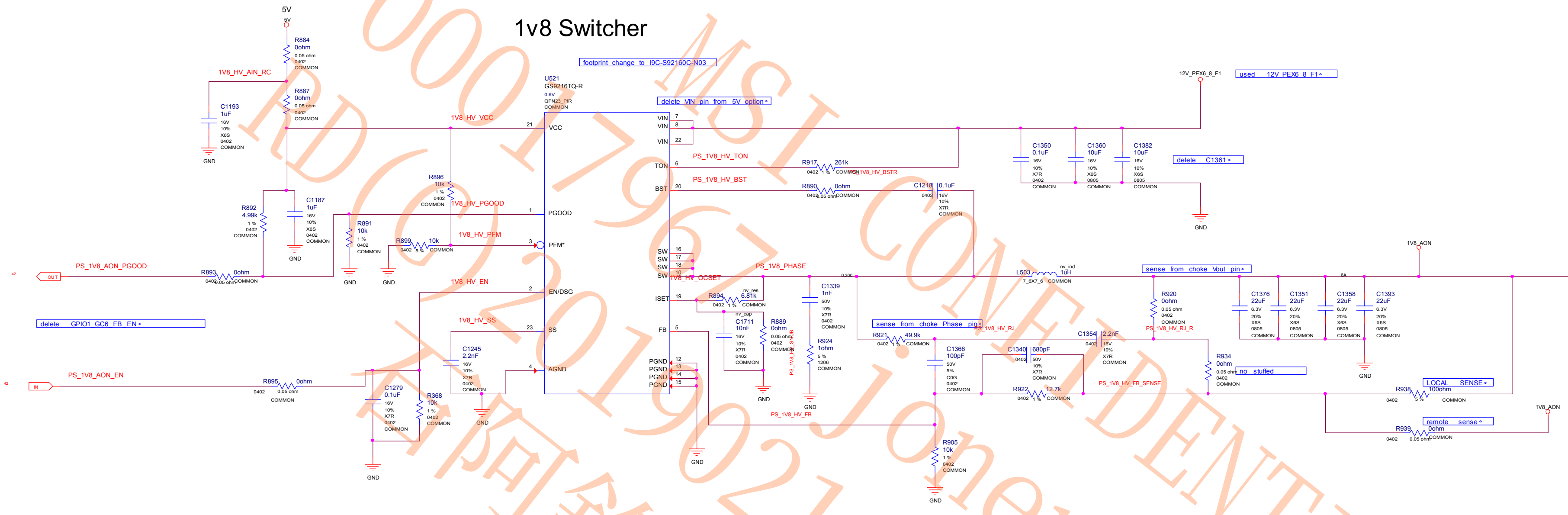
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Document Description: MISC: ROM, Straps	Rev 4.0
Date: Friday, November 09, 2018	Sheet 25 of 54	

Page26: PS: 1V8 PLL, 1V8_AON



1 L503 PN L04-01074K0-L65 / footprint : CHK_S2_7_3X6_61
2 delete colayout PWM ouput choke
3 delete 1V8_MAIN and merged to 1V8_AON

MICRO-STAR INT'L CO.,LTD

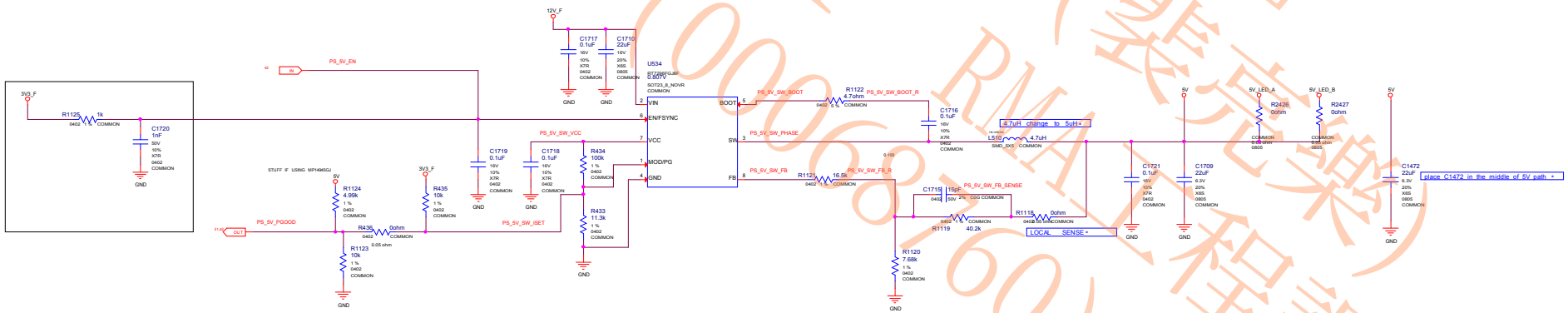
MS-V375

Size	Document Description	Rev
Custom	PS: 1V8 PLL, 1V8_AON	4.0

Date: Friday, November 09, 2018 Sheet 26 of 54

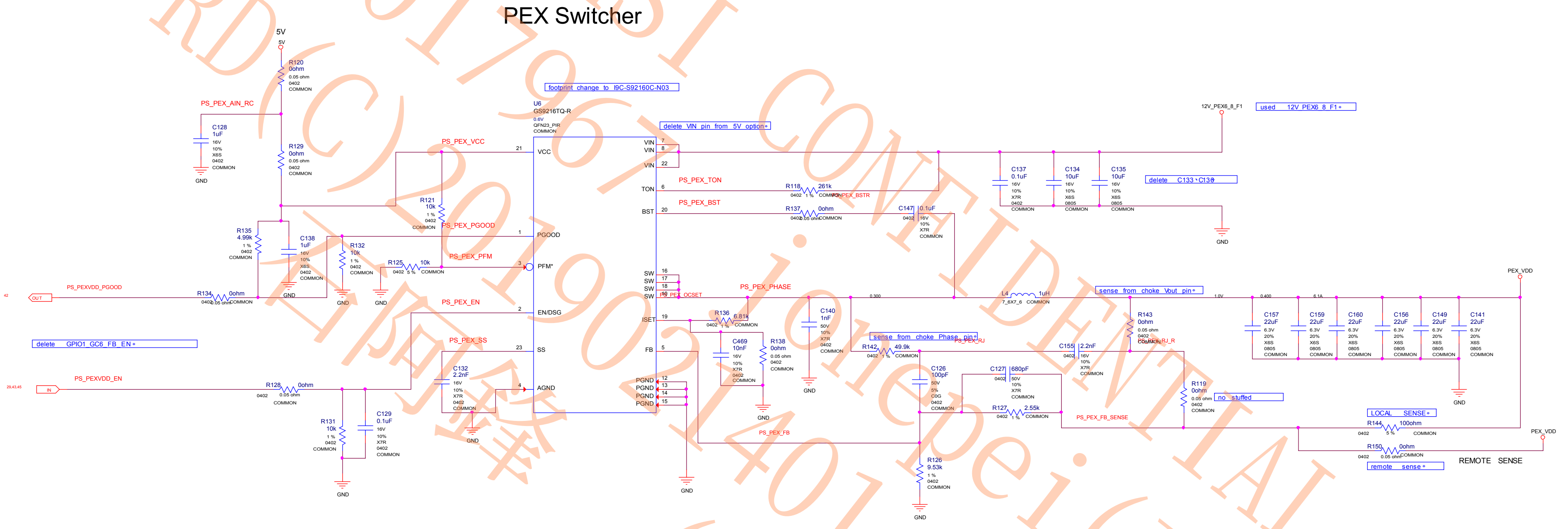
Page27: PS: 5V

1 L510 P/N L04-0507010-L65 / footprint : CHK_S2_5_4X5_23
2 delete colayout PWM ouput choke.
3 unused RTD3 delete Buck-Boost regulator.



MICRO-STAR INT'L CO.,LTD
MS-V375
Size: Custom | Document Description: PS: 5V | Rev: 4.0
Date: Friday, November 09, 2018 | Sheet 27 of 54

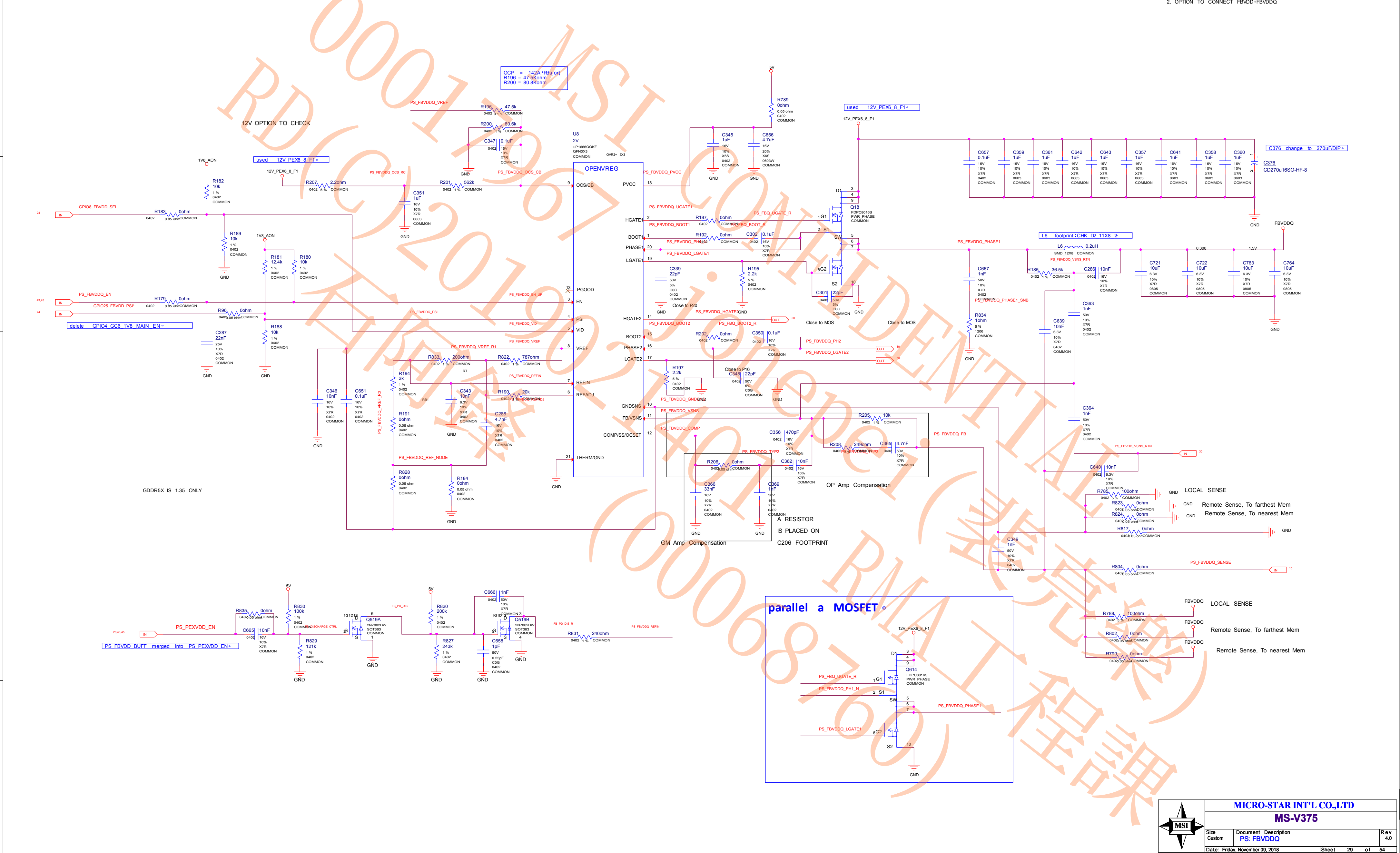
Page28: PS: PEXVDD



1 L4 PN L04-01074K0-L65 / footprint : CHK_S2_7_3X6_61
2 delete col ayout PWM ouput choke

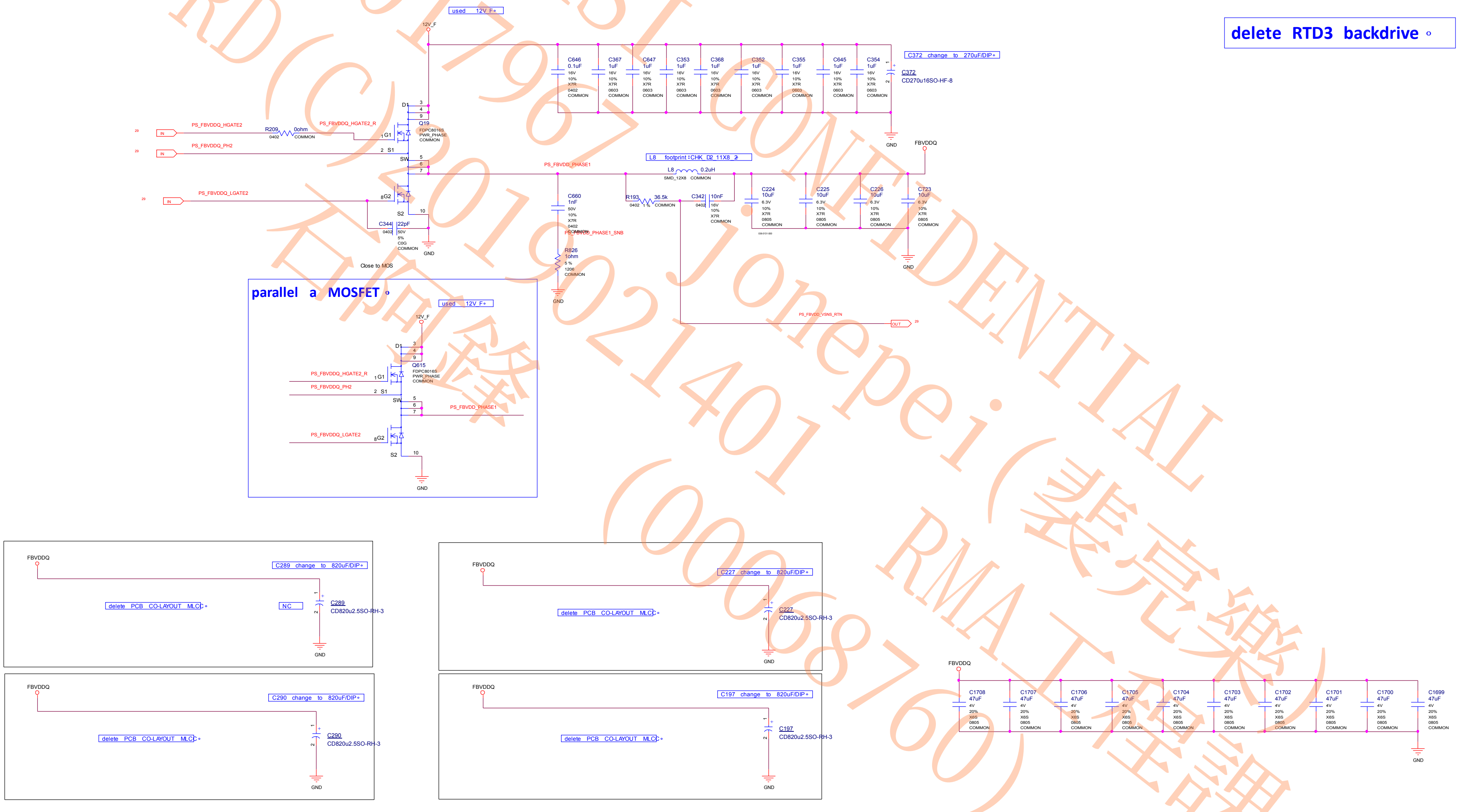
MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Document Description: PS: PEXVDD	Rev 4.0
Date: Friday, November 09, 2018	Sheet 28 of 54	

Page29: PS: FBVDDQ



MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Document Description: PS: FBVDDQ	Rev 4.0
Date: Friday, November 09, 2018	Sheet 29 of 54	

Page30: PS: FBVDDQ PH2

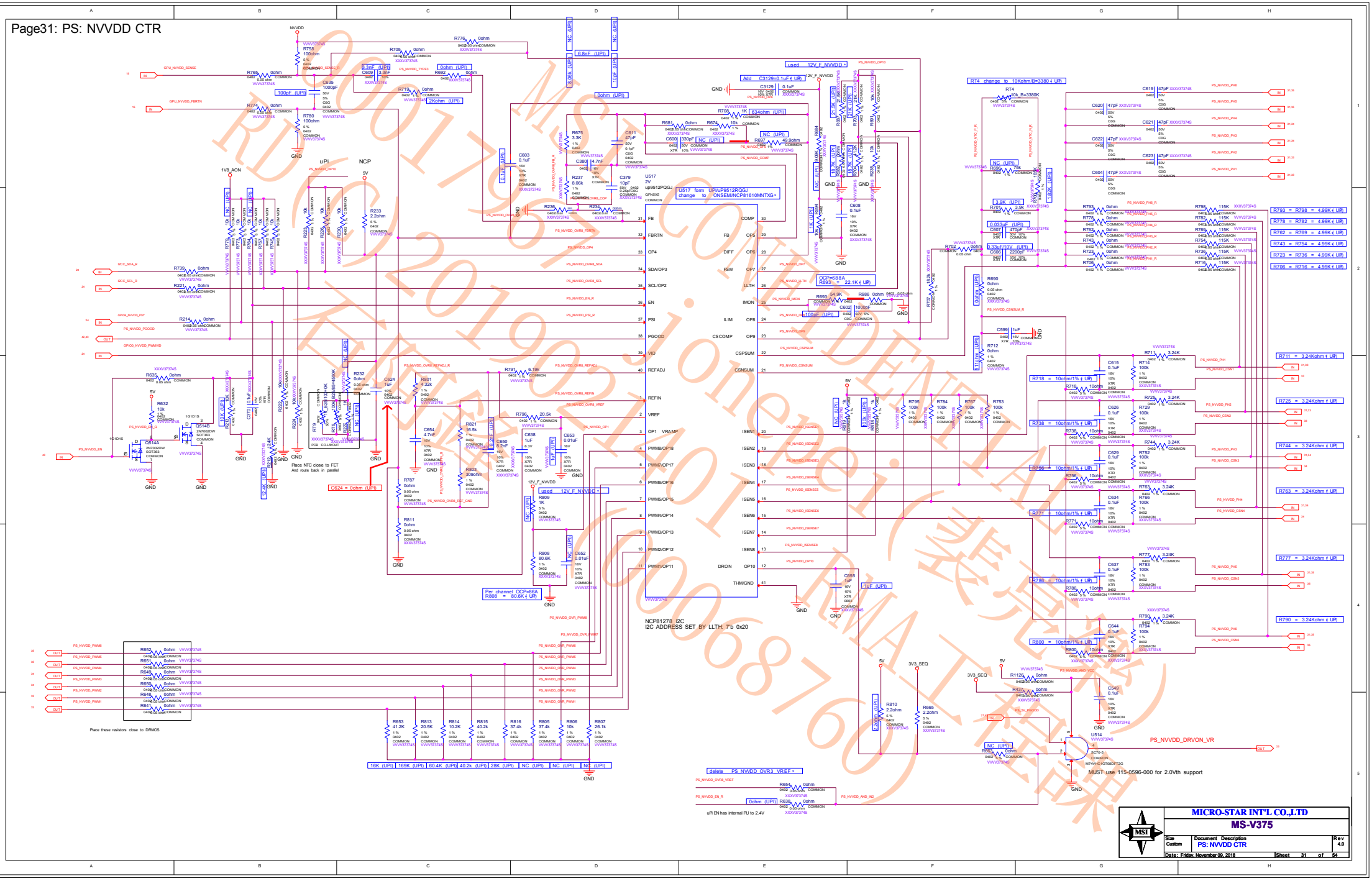


MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	PS: FBVDDQ PH2	4.0

Date: Friday, November 09, 2018 Sheet 30 of 54

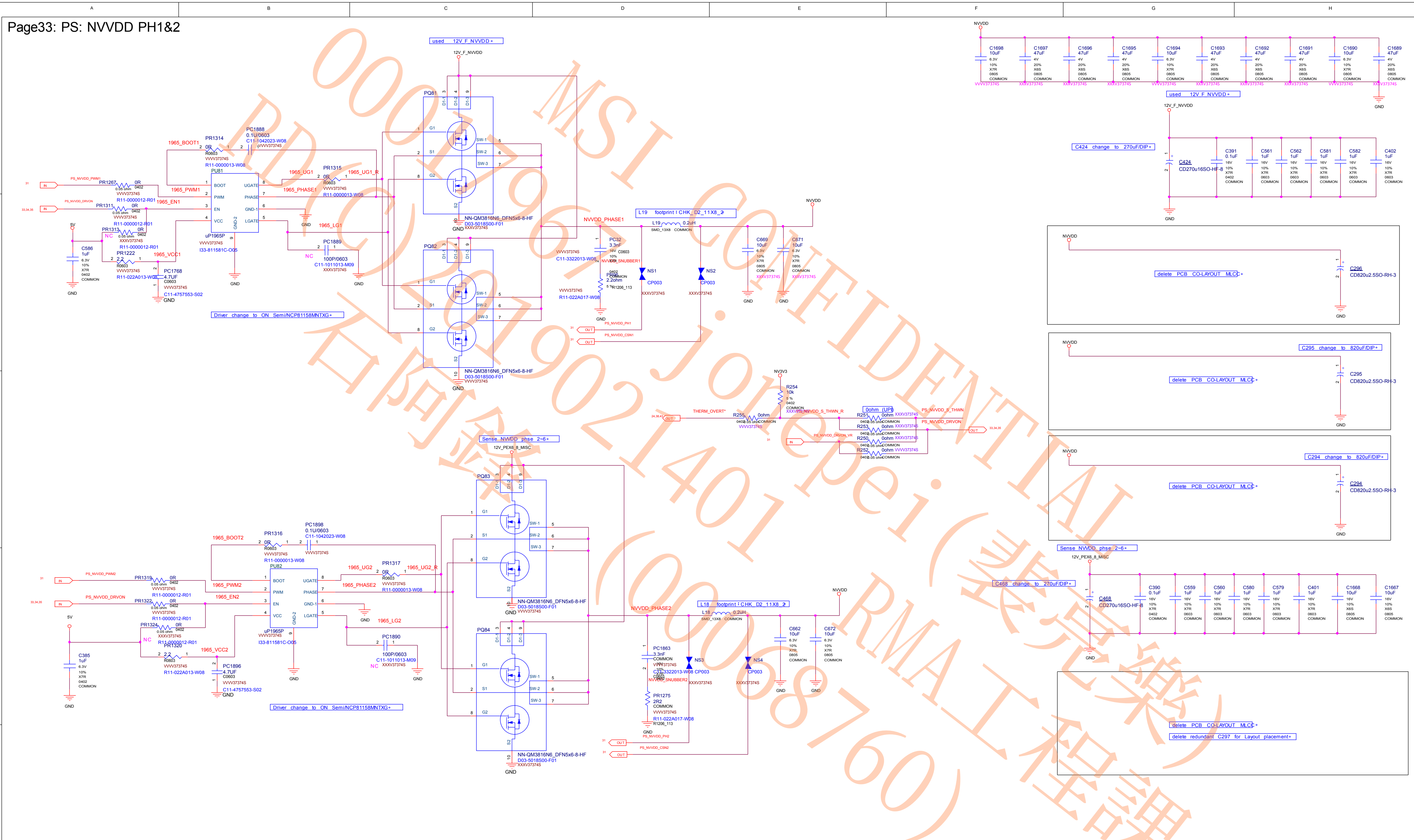

Page31: PS: NVVDD CTR
NVVDD
GPU_NVVDD_SENSE
GPU_NVVDD_FBRTN
uPI
NCP
1V8_AON
5V
U517
upi9512RQGJ
U517 form UPI/upi9512RQGJ change to ONSEMI/NCP81610MNTXG
NCP81278 I2C
I2C ADDRESS SET BY LLTH 7'b 0x20
Place NTC close to FET
And route back in parallel
C624 = 0ohm (UPI)
Place these resistors close to DRMOS
Per channel OCP=86A
R808 = 80.6K (UPI)
OCP=688A
R693 = 22.1K (UPI)
used 12V_F_NVVDD *
Add C3129=0.1uF (UPI)
delete PS_NVVDD_OVR3_VREF *
uR EN has internal PU to 2.4V
MUST use 115-0596-000 for 2.0Vth support
PS_NVVDD_DRVON_VR
MICRO-STAR INT'L CO.,LTD
MS-V375
Size Custom
Document Description
PS: NVVDD CTR
Rev 4.0
Date: Friday, November 09, 2018
Sheet 31 of 54

Page32: PS: NVVDD CTR OVR3i

delete all unused

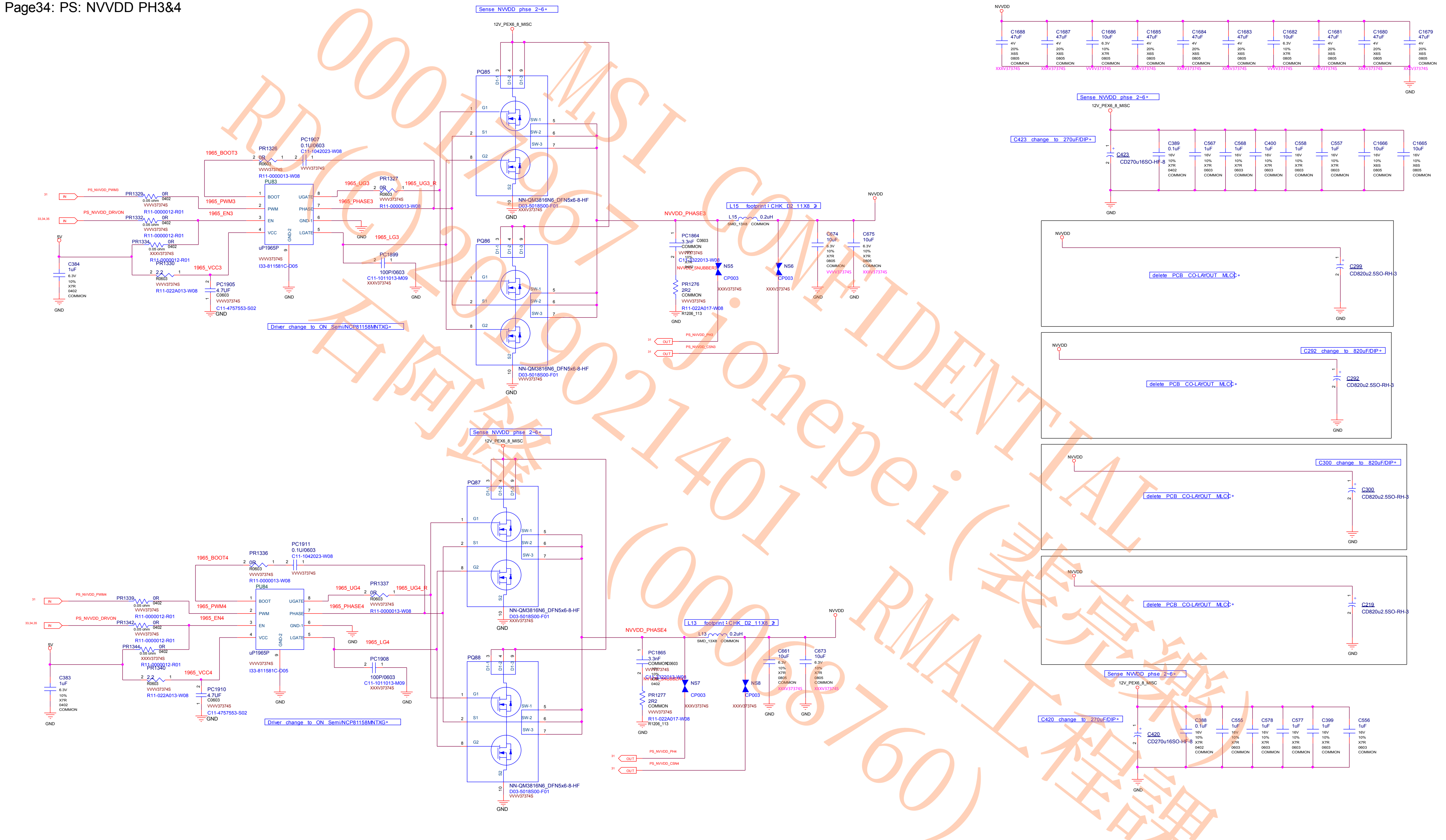
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
Size: Custom	Document Description: PS: NVVDD CTR OVR3i	Rev: 4.0
Date: Friday, November 09, 2018	Sheet 32 of 54	

Page33: PS: NVVDD PH1&2



MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Document Description: PS: NVVDD PH1&2	Rev 4.0
Date: Friday, November 09, 2018	Sheet 33 of 54	

Page34: PS: NVVDD PH3&4



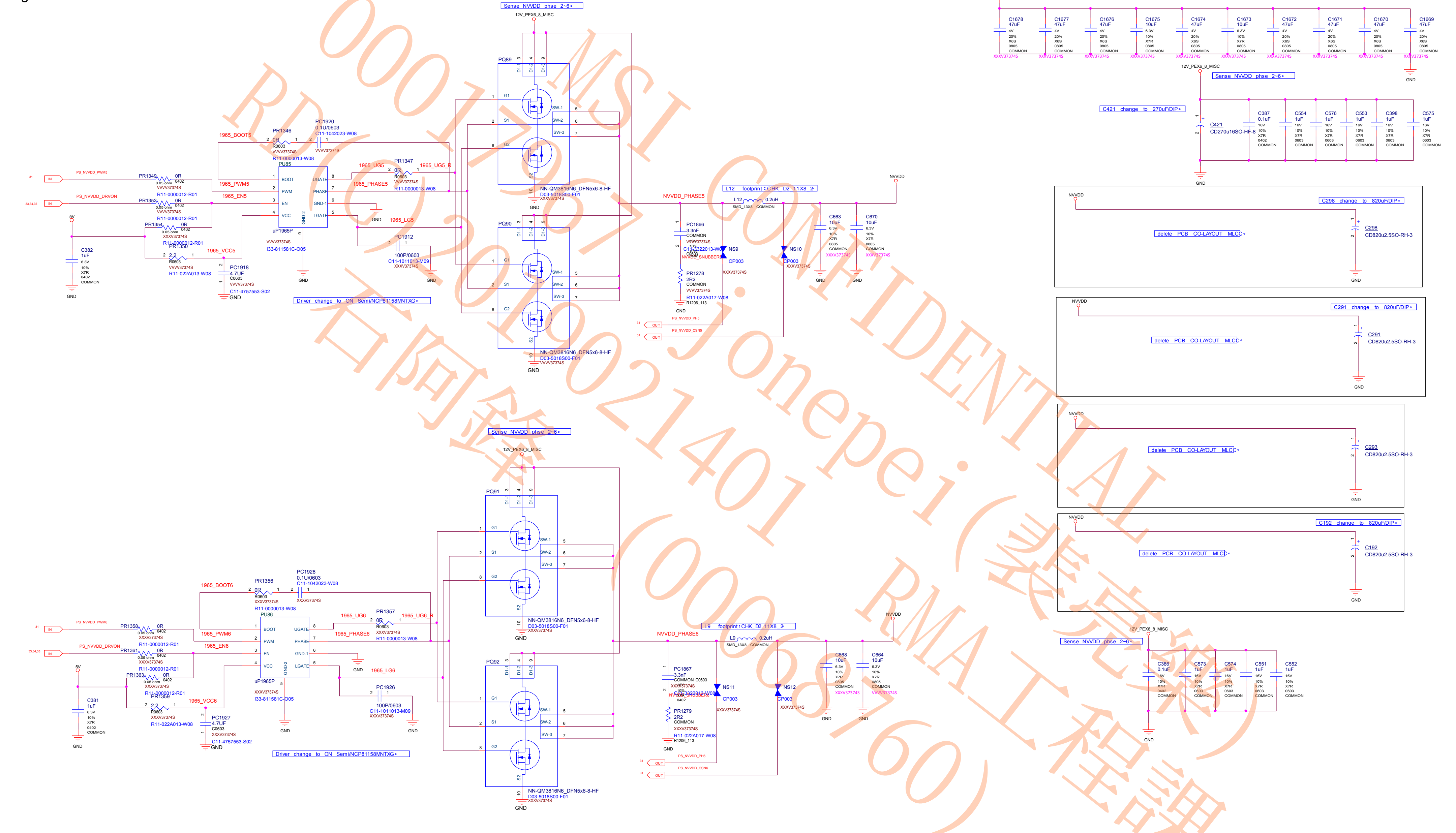
MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	PS: NVVDD PH3&4	4.0

Date: Friday, November 09, 2018 Sheet 34 of 54

Page35: PS: NVVDD PH5&6



MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	PS: NVVDD PH5&6	4.0

Date: Friday, November 09, 2018 | Sheet 35 of 54

Page36: Input Power Balancing Switcher

removed U511 for fixed NVVDD 12Vi nput:
1、merged 3V3_AON to 3V3_F。
2、unused and delete 3V3_AUX。
3、unused and delete 3V3_AUX_CON。
4、NVVDD_DYN_VIN merged to 12V_PEX6_8_F1。

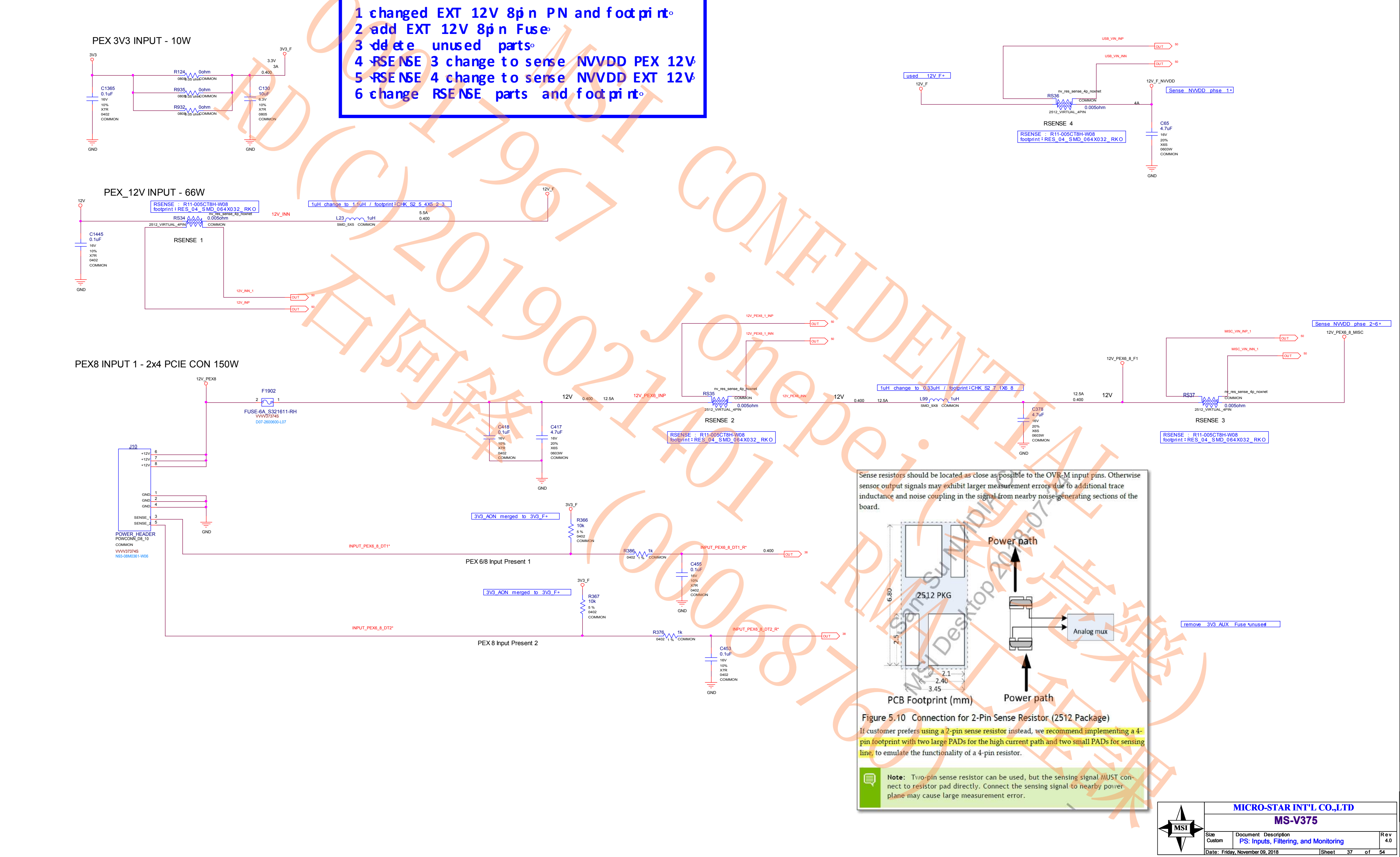
delete GPIO2_INPUT_DYN_BAL1 。

delete INPUT_PEX6_DT1_STEER 。

MICRO-STAR INT'L CO.,LTD
MS-V375
Size: Custom | Document Description: Input Power Balancing Switcher | Rev: 4.0
Date: Friday, November 09, 2018 | Sheet 36 of 54

Page37: PS: Inputs, Filtering, and Monitoring

1 changed EXT 12V 8pin PN and footprint。
2 add EXT 12V 8pin Fuse。
3 ddete unused parts。
4 RSENSE 3 change to sense NVVDD PEX 12V。
5 RSENSE 4 change to sense NVVDD EXT 12V。
6 change RSENSE parts and footprint。



Sense resistors should be located as close as possible to the OVR-M input pins. Otherwise sensor output signals may exhibit larger measurement errors due to additional trace inductance and noise coupling in the signal from nearby noise-generating sections of the board.

Figure 5.10 Connection for 2-Pin Sense Resistor (2512 Package)

If customer prefers using a 2-pin sense resistor instead, we recommend implementing a 4-pin footprint with two large PADs for the high current path and two small PADs for sensing line, to emulate the functionality of a 4-pin resistor.

Note: Two-pin sense resistor can be used, but the sensing signal MUST connect to resistor pad directly. Connect the sensing signal to nearby power plane may cause large measurement error.

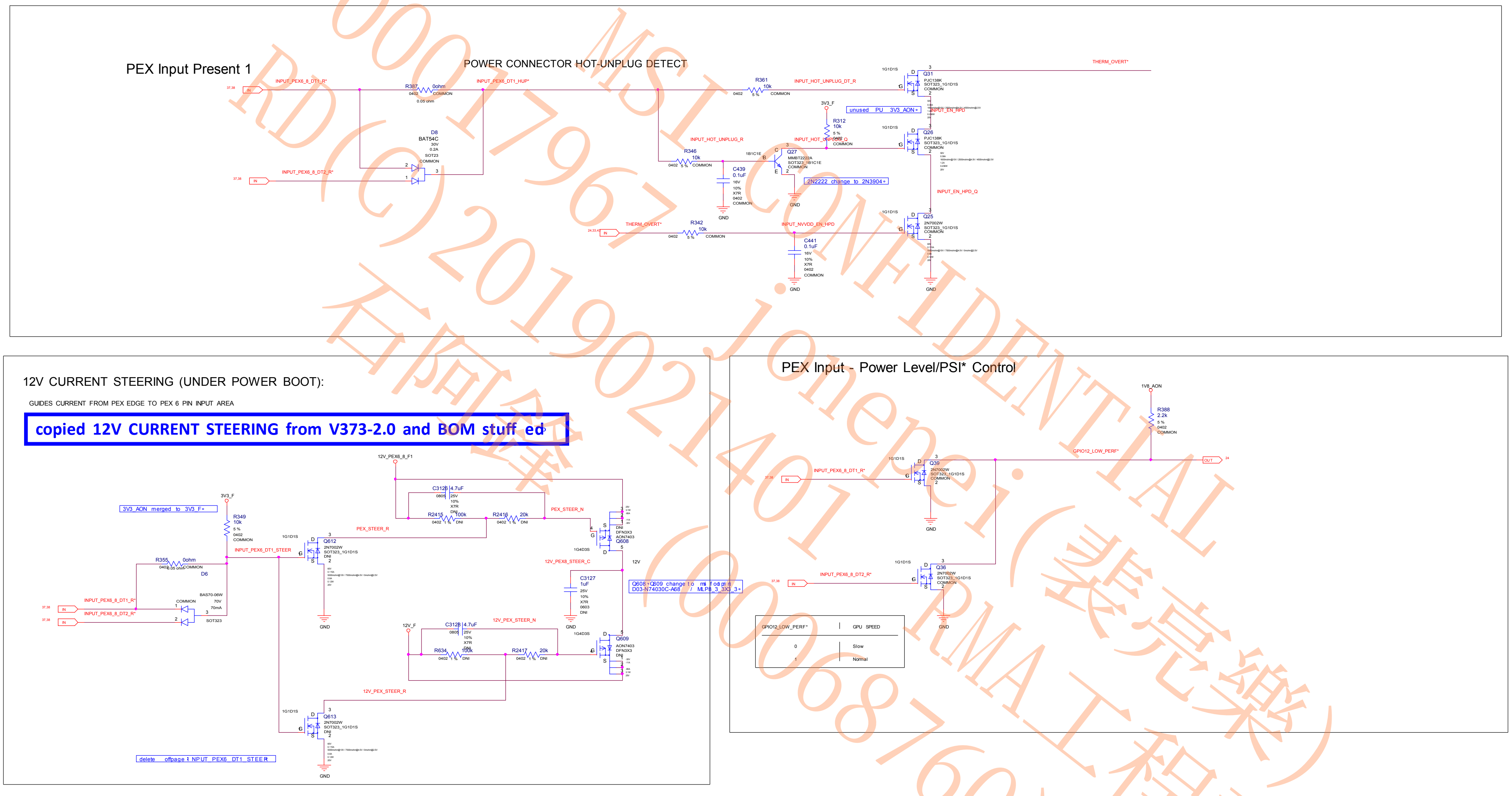
MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	PS: Inputs, Filtering, and Monitoring	4.0

Date: Friday, November 09, 2018 Sheet 37 of 54

Page38: PS: STEERING, UNDER POWER BOOT & HOT-UNPLUG



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	PS: STEERING, UNDER POWER BOOT & HOT-UNPLUG	4.0

Date: Friday, November 09, 2018 Sheet 38 of 54

Page39: BUCKBOOST

delete regulator for USBC_VBUS。

Unused USB_I2C* leaving Pull high resistor to 1.8V。

MICRO-STAR INT'L CO.,LTD
MS-V375
Size: Custom | Document Description: BUCKBOOST | Rev: 4.0
Date: Friday, November 09, 2018 | Sheet 39 of 54

Page40: PPC

delete PPC。

Unused USB_I2C* leaving Pull high resistor to 1.8V。

Unused IFPB_I2C* leaving Pull high resistor to 1.8V。

delete GPIO24_IFPF_HPD。

delete PEX_RST_BUF*。

delete GPIO1_GC6_FB_EN。

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Size	Document Description	Rev
Custom	PPC	4.0

Date: Friday, November 09, 2018 Sheet 40 of 54

Page41: 12V & 3V3_A SWITCHER

unused and delete all ◦

delete GPIO1_GC6_FB_EN *

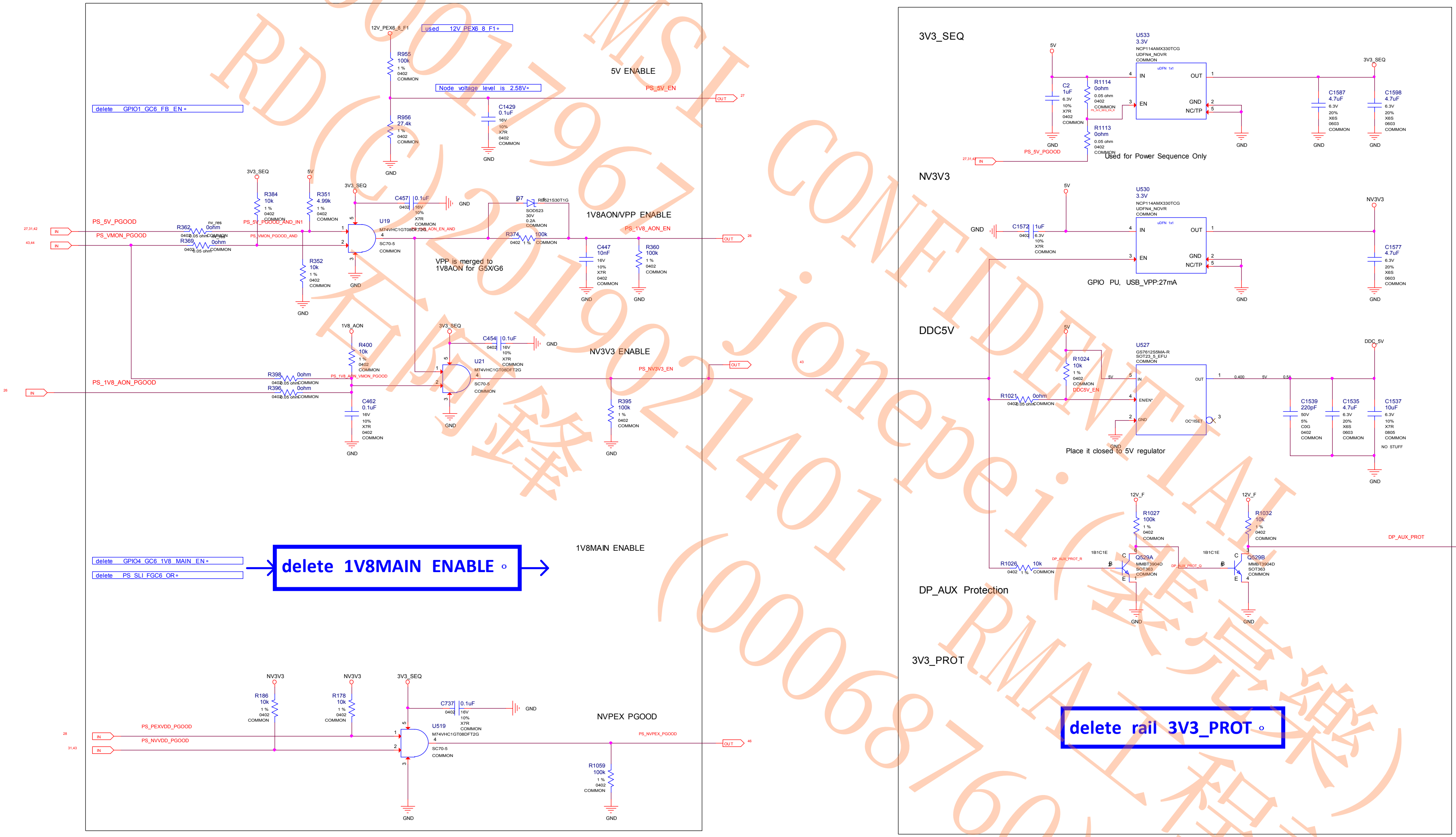
delete GPIO29_IDLE_IN_SW *

delete off-page 2PS_RTD_SWT.CH

unused and delete C404 *

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
Size: Custom	Document Description: 12V & 3V3_A SWITCHER	Rev: 4.0
Date: Friday, November 09, 2018	Sheet 41 of 54	

Page42: SEQ:5V,1V8,NV3V3 ENABLE



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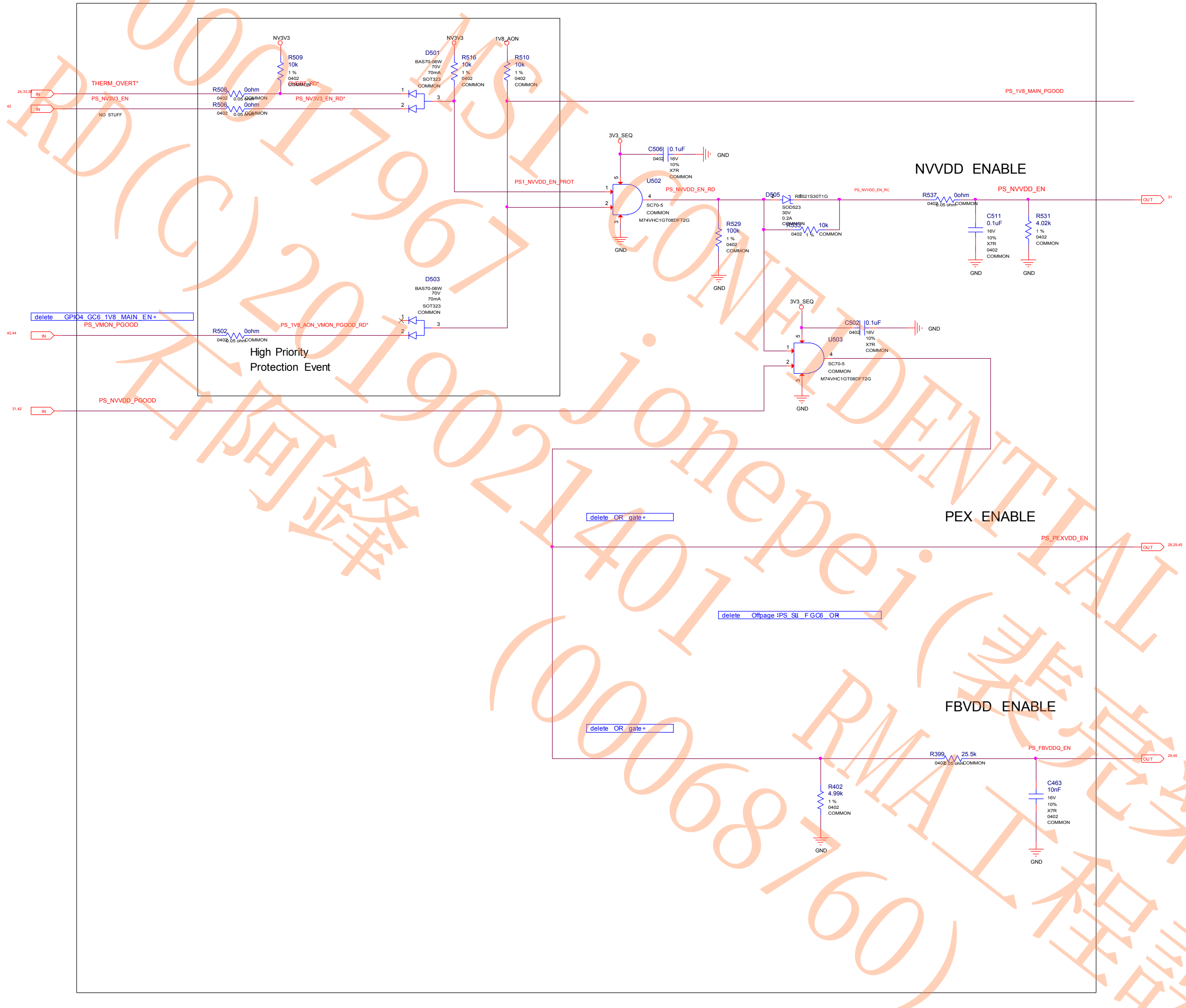
Size	Document Description	Rev
Custom	SEQ:5V,1V8,NV3V3 ENABLE	4.0

Date: Friday, November 09, 2018 | Sheet 42 of 54

Page43: SEQ:NV,PEX,FB ENABLE



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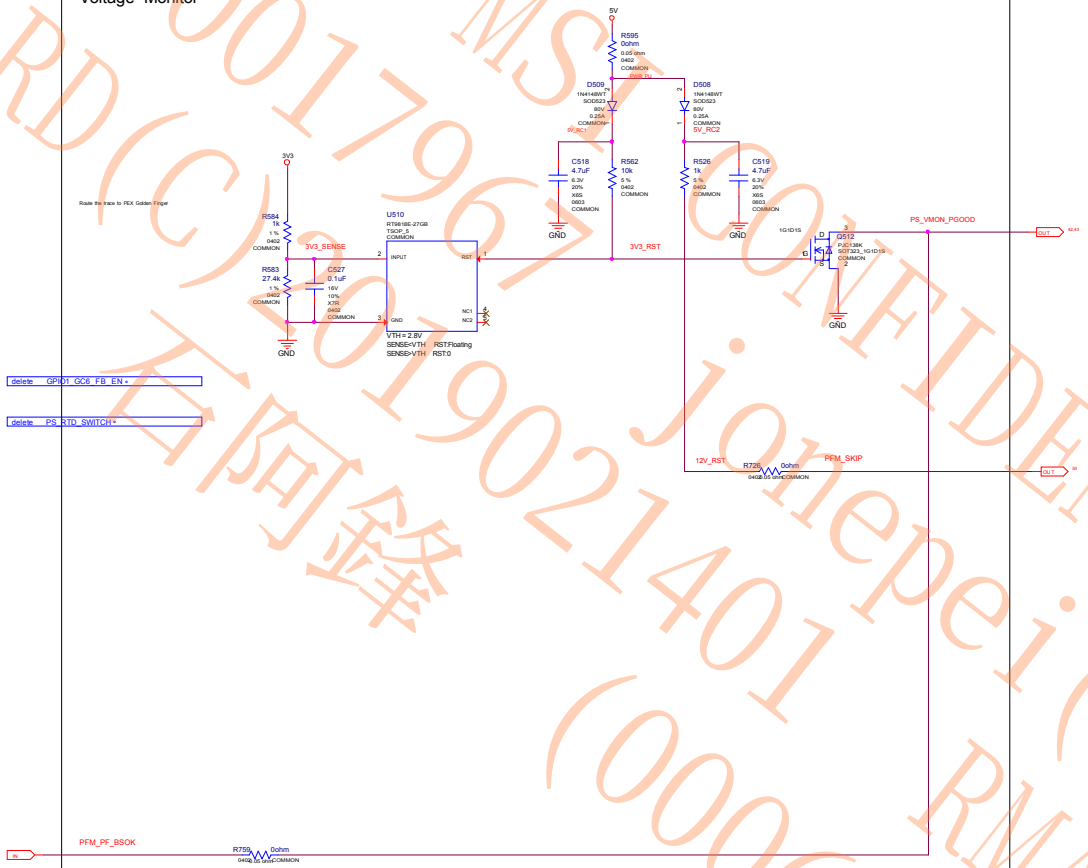
Size	Document Description	Rev
Custom	SEQ:NV,PEX,FB ENABLE	4.0

Date: Friday, November 09, 2018 — Sheet 43 of 54

Page44: SEQUENCE:Voltage Monitor

delete unused parts。

Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

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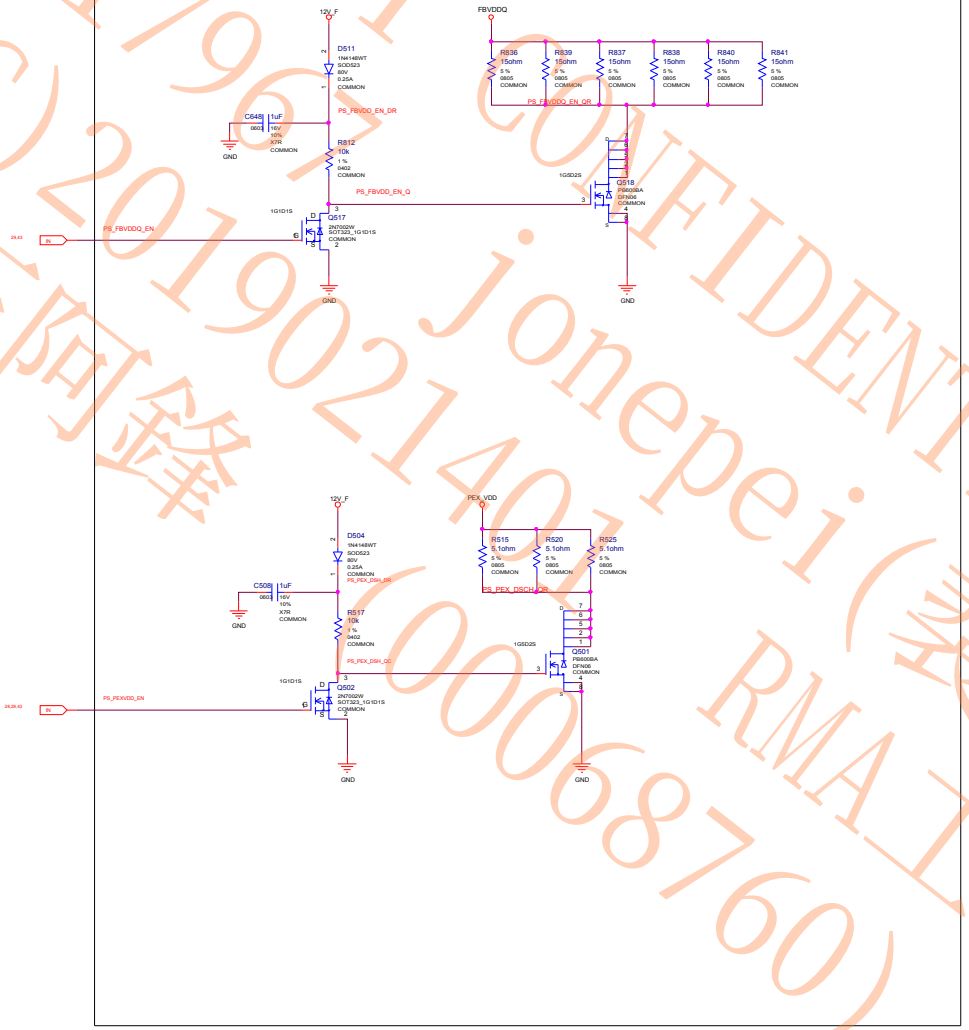
MS-V375

Size: Custom | Document Description: SEQUENCE:Voltage Monitor | Rev: 4.0

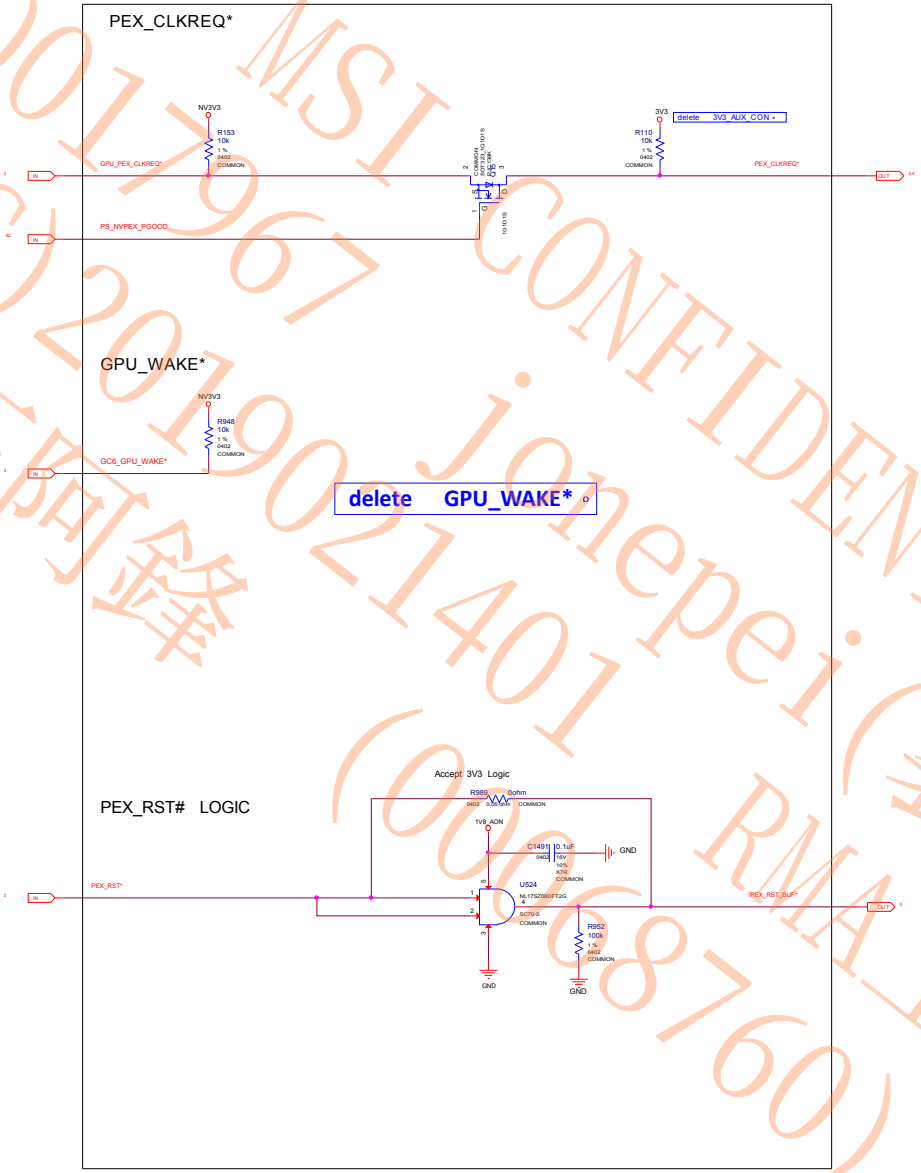
Date: Friday, November 09, 2018 | Sheet 44 of 54

Page45: SEQUENCE:Discharge



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
Size: Custom	Document Description: SEQUENCE:Discharge	Rev: 4.0
Date: Friday, November 09, 2018	Sheet 45 of 54	

Page46: SEQUENCE:MISC



MICRO-STAR INT'L CO.,LTD	
MS-V375	
Size: Custom	Document Description: SEQUENCE:MISC
Rev: 4.0	
Date: Friday, November 09, 2018	Sheet 46 of 54

Page47: LOGO LED

delete all unused

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MS-V375

Size	Document Description	Rev
Custom	LOGO LED	4.0

Date: Friday, November 09, 2018 Sheet 47 of 54

Page48: LED DRIVER & Boost

delete all unused

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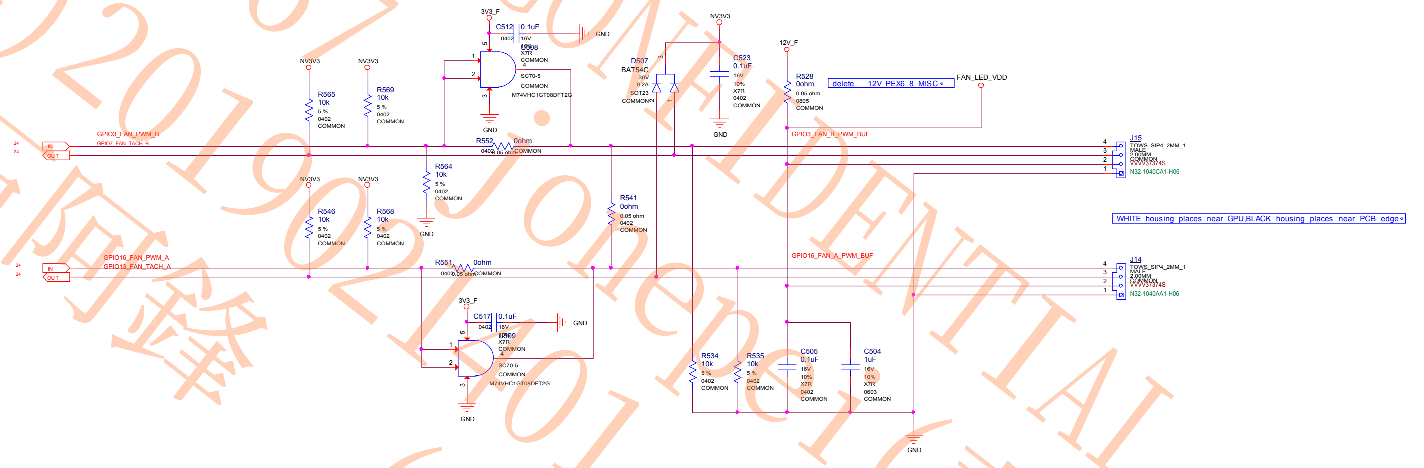
MS-V375
Size: Custom | Document Description: LED DRIVER & Boost | Rev: 4.0
Date: Friday, November 09, 2018 | Sheet 48 of 54

Page49: DUAL FAN

copied V373-2.0 housing PN and footprint。



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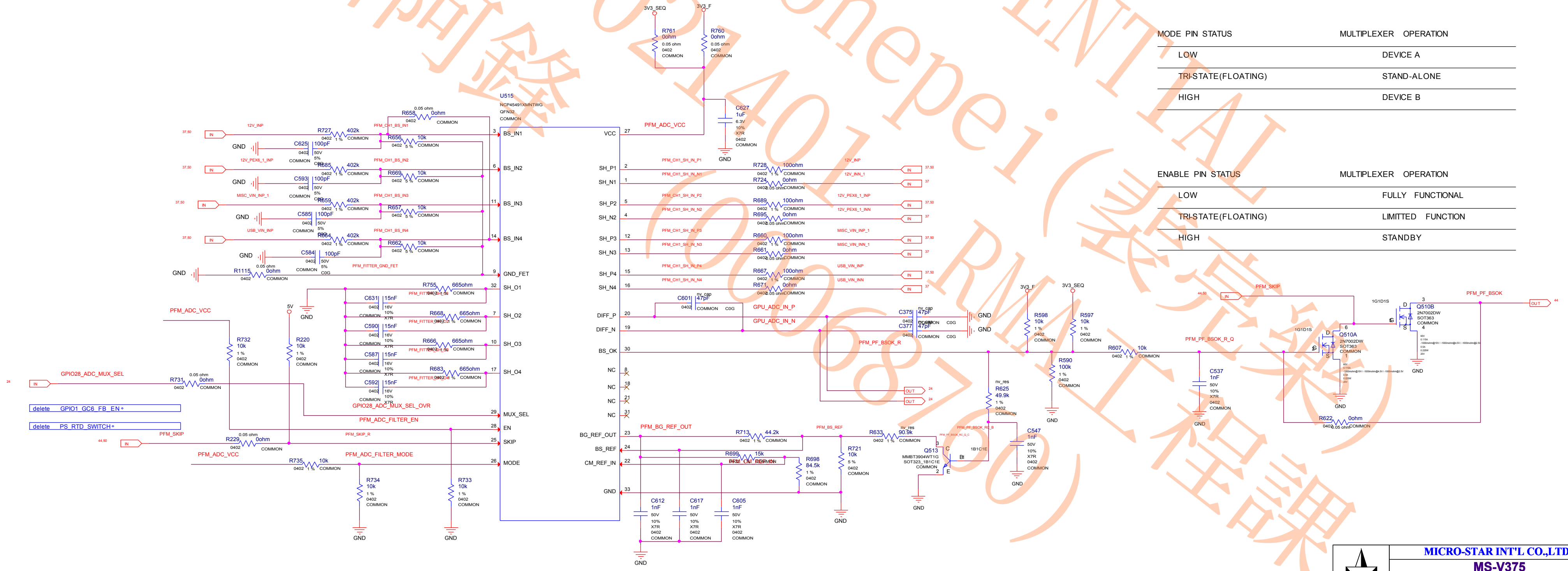
MS-V375

Size	Document Description	Rev
Custom	DUAL FAN	4.0

Date: Friday, November 09, 2018 Sheet 49 of 54

Page50: PWR SENSE



MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY

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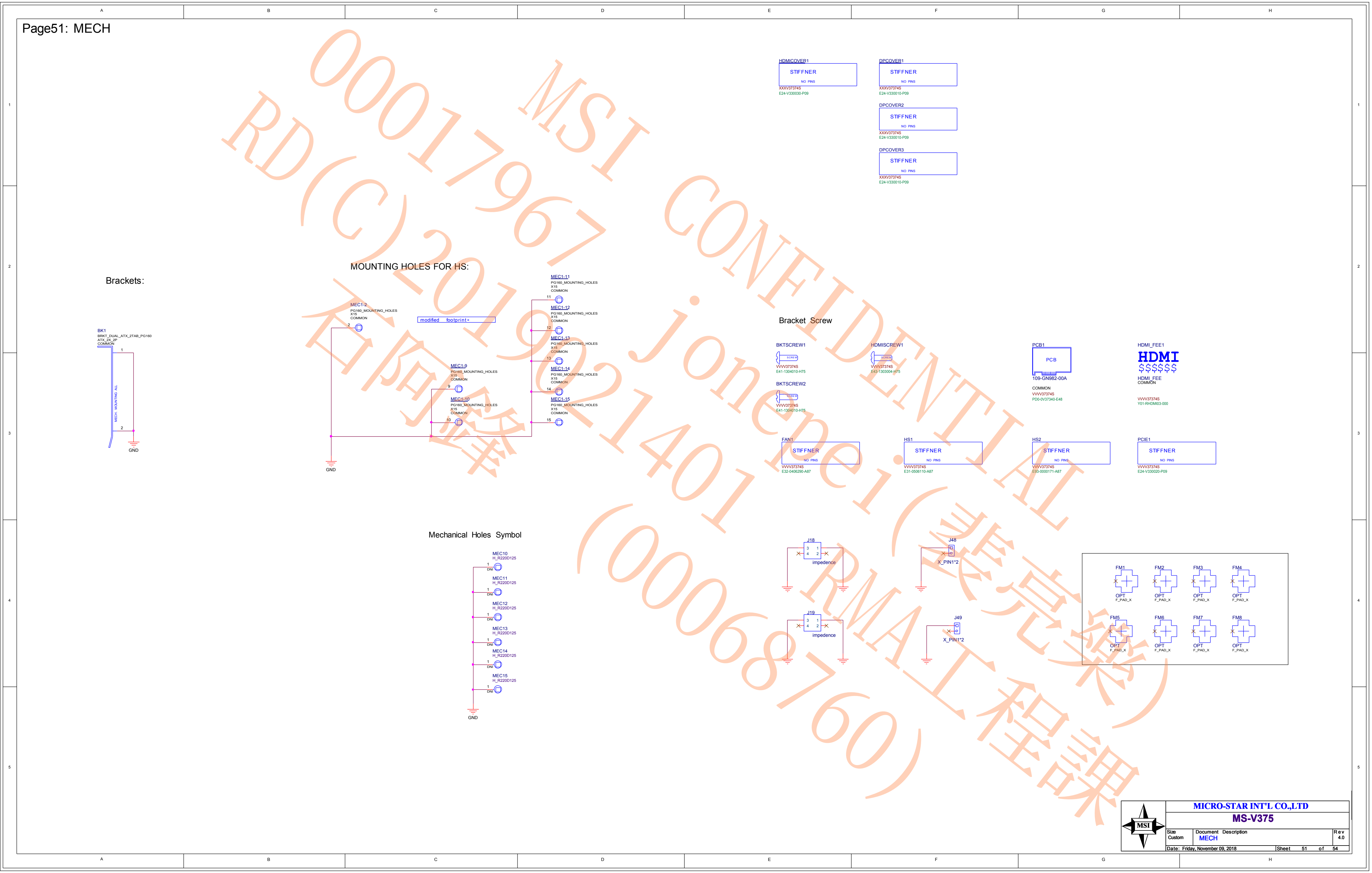
MS-V375

Size	Document Description	Rev
Custom	PWR SENSE	4.0

Date: Friday, November 09, 2018 Sheet 50 of 54

Page51: MECH



Page52: PTC

improved FBVDDQ PSU parts don't require a PTC

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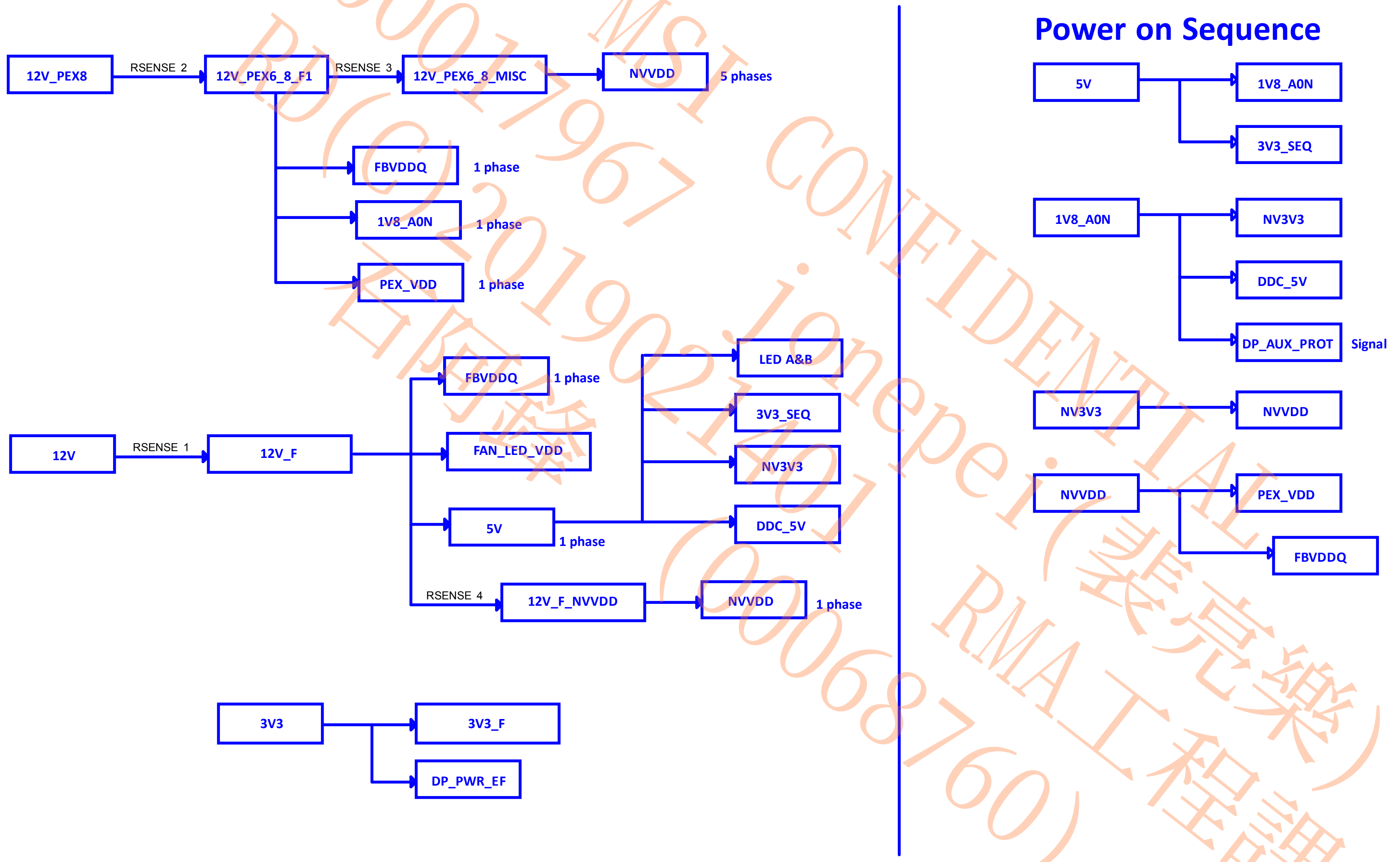
MS-V375

Size	Document Description	Rev
Custom	PTC	4.0

Date: Friday, November 09, 2018 Sheet 52 of 54

PAGE 53: Power Delivery



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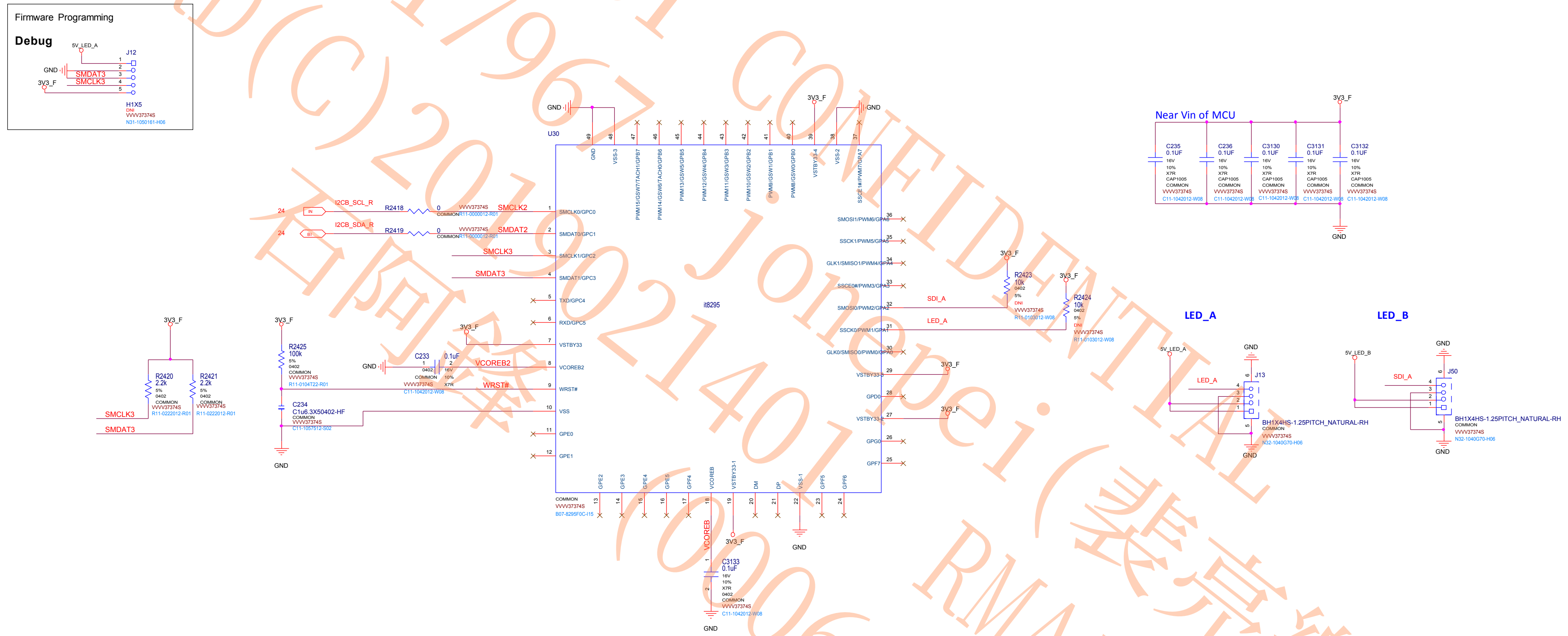
MS-V375
Power Delivery

Page54: LED_CONTROLLER_IT8295



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MS-V375

Size: Custom | Document Description: LOGO LED | Rev 4.0

Date: Friday, November 09, 2018 | Sheet 54 of 54