MS8874

P70, NV17, 2M/4MX32 DDR, 32MB/64MB, RGB, TV-out, video capture, stereo, Hardware Monitor, AGP4X

PCI DEVICE ID 0X0=0X171 FOR NV17-128D.

HISTORY:

X00:
first version for layout start. No video capture, no stereo. NO DRC CHECK.

X01:
fixed PCB footprints for IC_SO14_150MIL and CON_DVI-I_RA
added end-termination r-packs for address-status-bus
changed RGB filter to integrated 5-pole only
added video capture, BIOS, Strapping
changed RefDes
NO DRC CHECK

X02:
added missing end termination for FBBAx
changed stereo 3pin header
added clamp diodes for TV-out and video capture
changed topology for 2nd DDC (VGA / DVI)
NO DRC CHECK

X03:
splitted analog/digital suply for SAA7113 (no component change)
Fixed some RefDes
Changed the strapping resistors cases to 0402
NO DRC CHECK

X04:
changed C617 to SMD0603
changed U502 and U503 to TSSOP14
added CKE connection to the memories
added D505 to the stereo section
changed L501, L502, L503 to 0603
NO DRC CHECK

X05:
changed U601 to SOT223-DPAK-D2PAK
added bracket
changed L600 to IND_CDR73
added VIP connector
NO DRC CHECK

X06:
deleted VIP
changed TPs to HOLE_48C28P
changed switcher gate circuit (no component change)
added C641 and C642 to the linear voltage regulator
pinswap of memory termination
NO DRC CHECK

X07:
deleted page 10: 5.b ViVo
changed filter topology for RGB
added return traces for RGB
NO DRC CHECK

X08:
added TV filter caps with reference to GND (C511,C517,C522)
separated RGB returns (NOTE: there will be a change for DAC2)
NO DRC CHECK

X09:
added net names to unused panel signals (test points)
NO DRC CHECK

X10:
added decoupling for DVO rail (C529 and C530)
added GND connection to pin 1 of U700
added R520 pull down for DVOCLKIN
DRC CHECK DONE

X11:
changed caps in power section to the combined footprints

X12:
data bus swappings

X13:
swapped CLKs for U201 and U202

X14:
connected the RGB returns of VGA2 together

X15:
update materials

X16:
update stuffings

X17-A01:
release A01
changed DVOVDD from VID3.3V to A3.3V
add linear regulator for NV17's VDD33
connected the IFP-RSETs to GND
deleted C134 and C135

X18:
change to target release A02
changed I2C assignments
added I2C filter components for ViVo (L506,L507,R521-R524,D506,D507,C531,C532)

X19:
added R243-R250 for clock pull-up.

X20-A02:
material changes.

X21-A03:
fixed values and descriptions for R609, R613 and C640
changed the RGB filter topology:
- delete R325-R330
- connect all DACRTN to GND
- move the 75R termination resistors to the connector
changed RGB clamping to A3.3V
add testpoint net XTALOUTBUFF
changed XTAL-load caps C320 and C321 to 18pF
removed obsolete 0603 0Ohm resistors
NO_STUFFed the stereo 3-pin header.

X22-A03:
changed bulk decoupling in VGA section from 3.3V to A3.3V
fixed DAC1BLUE (net name was missing)

X23-A03:
changed VDD33 to A3.3V

X24-A03:
added C643 for memory core decoupling

X25-A03:
changed the long body VGA connector to a three pin type
changed C425 connection for fan decoupling

```
EDIT FROM NV17
(P70), 8861


0. ADD RE1,CE1 ON PCICLK

1. REMOVE DVI :P400
   CONNECTOR  PAGE8

2. ADD PH 7108 PAGE 9


3. ADD AV_IN , S_IN, AV_OUT ,S_OUT

   PAGE10

4. C611,C612,C627,C628,C641,C642 from
   SMD TO DIP CAP

   L600,L601FROM SMD
   TO  DIP CHOKE

   PAGE11

5. BIOS STRAPPING~~DEL R700,R734,R747

   PAGE12
```

PAGE OVERVIEW

1 top (this) page
2 1. AGP interface, core decoupling
3 2.a NV17 Frame Buffer
4 2.b Frame Buffer 0..63
5 2.b Frame Buffer 64...127
6 3.a Dual DAC, 1st VGA
7 3.b Dual DAC, 2nd VGA
8 4. Panel
9 5.a TV-out, video capture, stereo
10 6. Power supply
11 7. BIOS, Strapping
12 8. Hareware Monitor

Stuffing Options	Meaning
COMMON	common components for all skus
NO_STUFF	no assembly at all
XTAL_27	stuff the 27MHz xtal for the GPU
XTAL_14	stuff the 14.318MHz xtal for the GPU
VIVO	stuff video I/O
VIDCAP	stuff video capture
TV_OUT	stuff TV-out
DVI-I	stuff the DVI-I option
DVI	stuff the DVI-D option
2NDVGA	stuff a second VGA
NO_DVI	don't stuff any DVI
SYNC_DRIVER2	stuff the termination resistors for the DACB syncs
SYNC_DRIVER	stuff the sync driver chip
NO_SYNC_DRIVER2	bypass the sync driver for the DAC B syncs
NO_SYNC_DRIVER	bypass the sync driver for the DAC A syncs
STEREOSYNCS	stuff the switchable stereo sync circuit
STEREOSYNC2	sync stereo to DAC B
STEREOSYNC1	sync stereo to DAC A
STEREO	stuff the generic stereo circuit
SI2C_PROT	stuff the protection diodes for syncs and I2C at DAC A
RGB_PROT	stuff the protection diodes for RGB at DAC A
2NDVGA_RGB_PROT	stuff the protection diodes for RGB at DAC B
2NDSI2C_PROT	stuff the protection diodes for syncs and I2C at DAC B
SET_NVVDD_ISL	set NVVDD voltage at Intersil switcher
SET_NVVDD_IRU	set NVVDD voltage at IR/Uniseml switcher
SET_FBVDDQ_ISL	set FBVDDQ voltage at Intersil switcher
SET_FBVDDQ_IRU	set FBVDDQ voltage at IR/Uniseml switcher
NO_1117	bypass the A3.3V regulator to AGP3.3V
ISL	stuff the Intersil switcher
IRU	stuff the IR/Unisem switcher
FBVDD_3.3	connect FBVVDD with AGP3.3V
FBVDD_2.5	connect FBVVDD with FBVDDQ
1117_ADJ	stuff the adjustable regulator for A3,3V
1117	stuff the fixed regulator for A3,3V
PASSIVE_HS	have passive heatsink
FAN	fan sink and components
BRCKT_VGA_TV_VGA	Bracket VGA-TV-VGA
BRCKT_VGA_TV_DVI	Bracket VGA-TV-DVI
BRCKT_VGA_TV	Bracket VGA-TV
BRCKT_VGA	Bracket VGA
MEMSTRAP1111	strap memory to 1111
MEM-64B	stuff 64 bit memory - 2pcs
MEM-128B	stuff 128 bit memory - 4pcs
NV17-128D	stuff NV17-128D

Item\tQty\tRefDes\tDescription\tAssembly\tNVPN\tNotes\tValue\tParam_voltage\tParam_material\tParam_tolerance\tParam_power\tParam_esr\tParam_ripple\tParam_current\tPCB Footprint
{Item}\t{Qty}\t{Reference}\t{Description}\t{Assembly}\t{NVPN}\t{Notes}\t{Value}\t{P_volt}\t{P_mat}\t{P_tol}\t{P_pow}\t{P_esr}\t{P_ripple}\t{P_current}\t{PCB Footprint}

140-10070-0000-A03
602-10070-0000-A03

Micro-Star International Co., LTD.
<Title>
Size: Custom | Document Number: <Doc> | Rev: <RevCod
Date: Wednesday, March 13, 2002 | Sheet 1 of 13

R9002 1 2

R9003 1 2

S3 1 2

S1 1 2

C9000 1 2

R9001 1 2

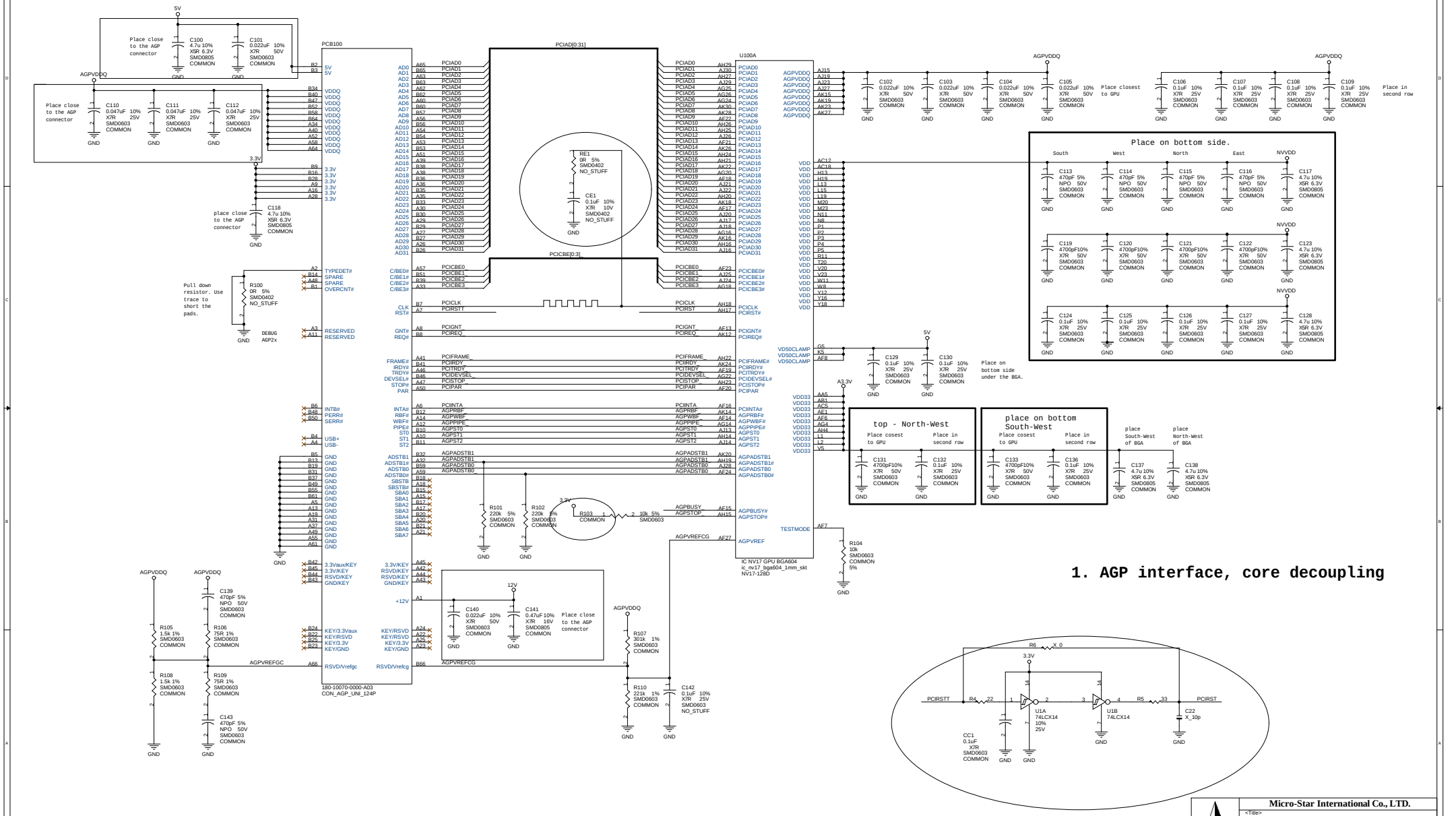
S4 1 2

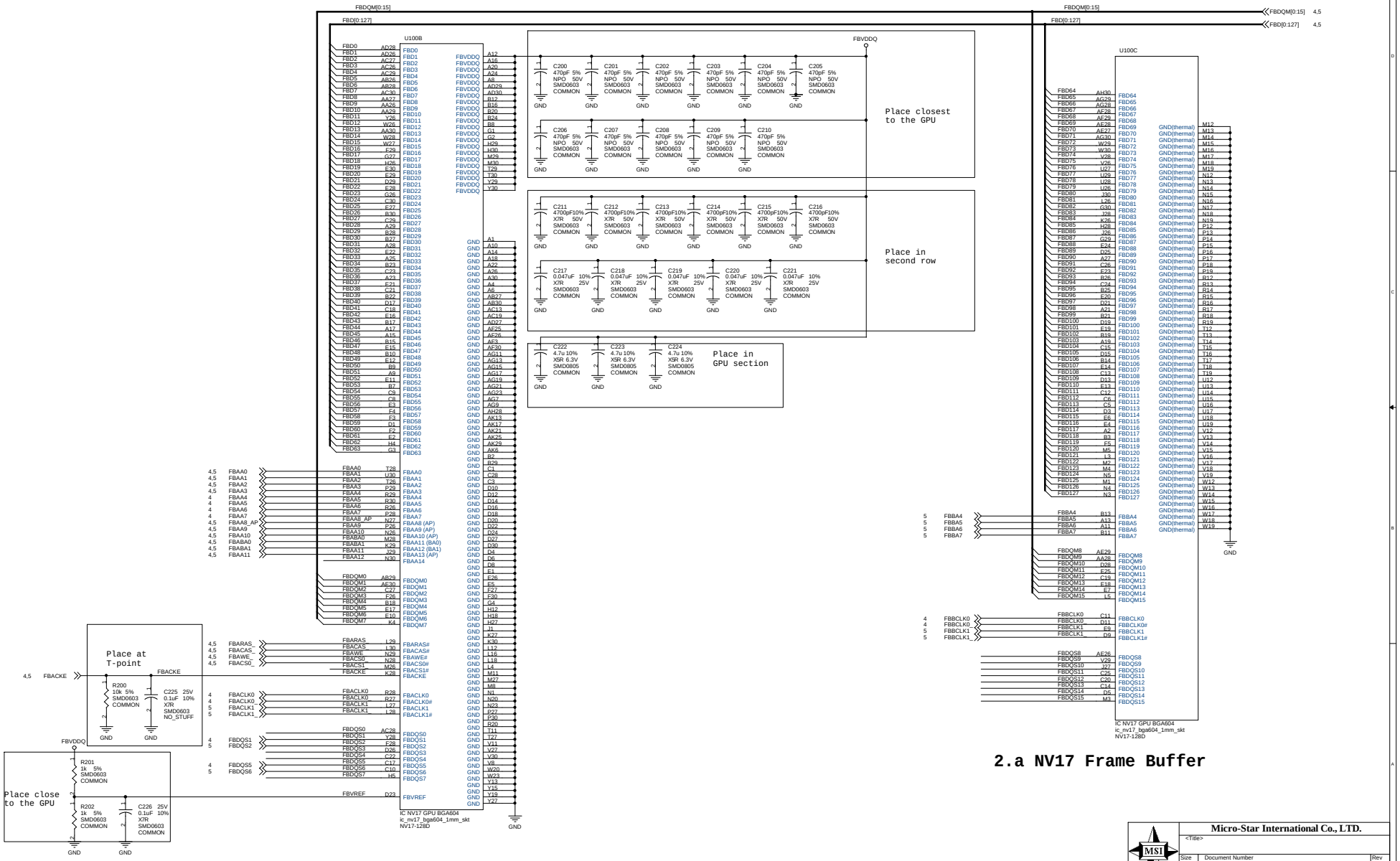
R9000 1 2

S2 1 2

BRACKET 1 2

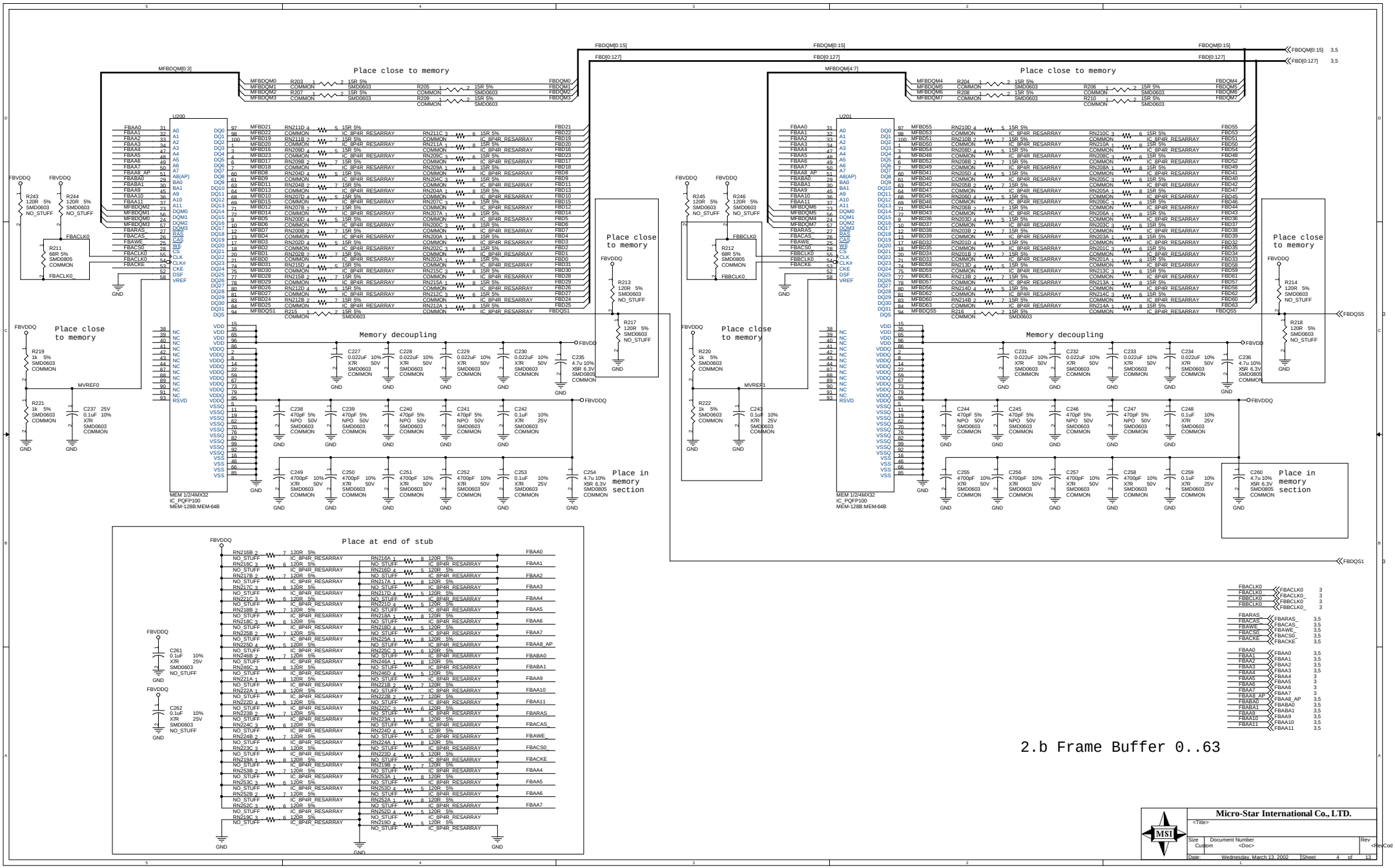
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, March 13, 2002	Sheet 1 of 1	

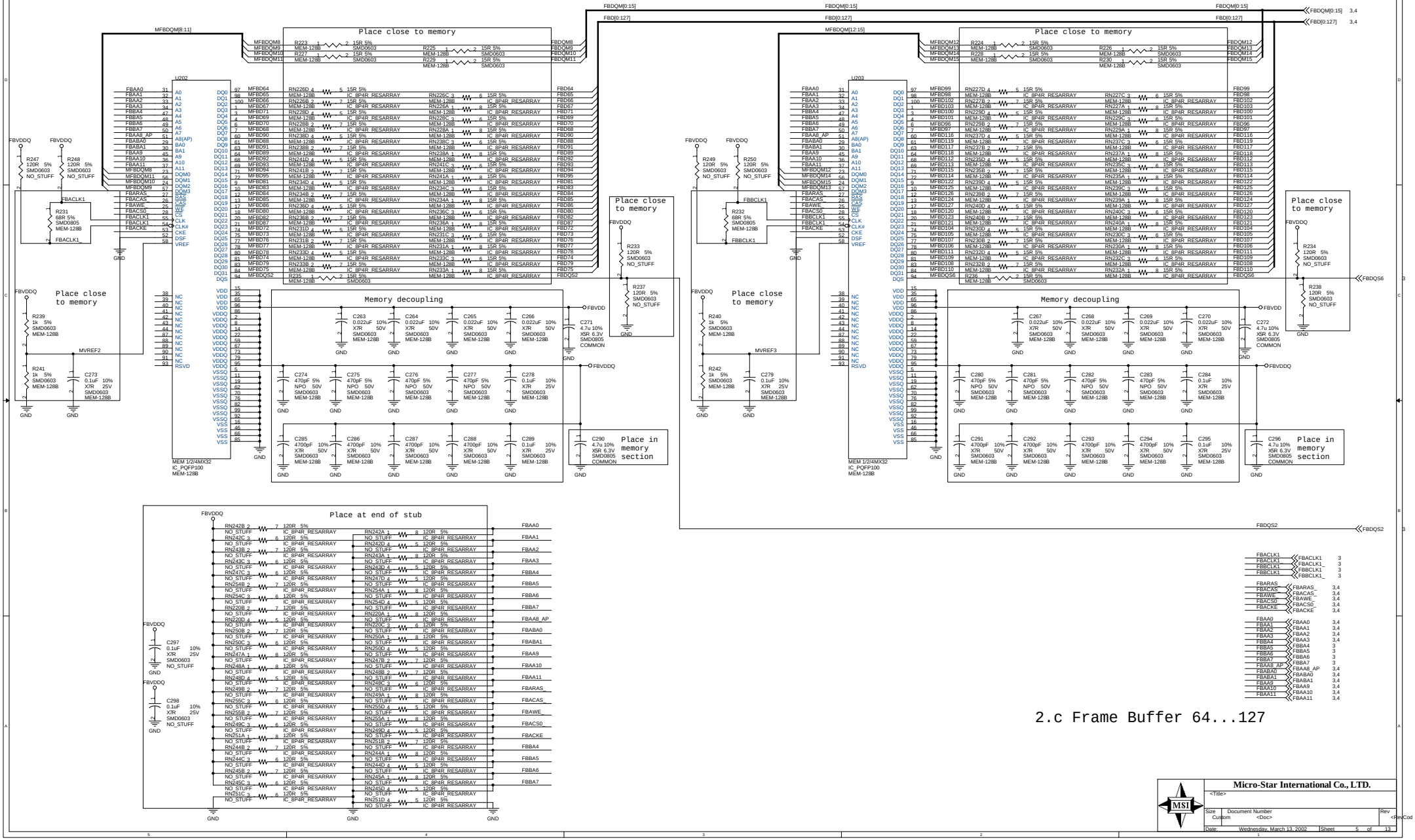

PCB100
U100A
PCIAD[0:31]
PCICBE[0:3]
IC NV17 GPU BGA604
ic_nv17_bga604_1mm_skt
NV17-128D
180-10070-0000-A03
CON_AGP_UNI_124P
Place on bottom side.
top - North-West
place on bottom
South-West
1. AGP interface, core decoupling
Micro-Star International Co., LTD.
<Title>
Document Number
Custom
<Doc>
Wednesday, March 13, 2002
Sheet 2 of 13

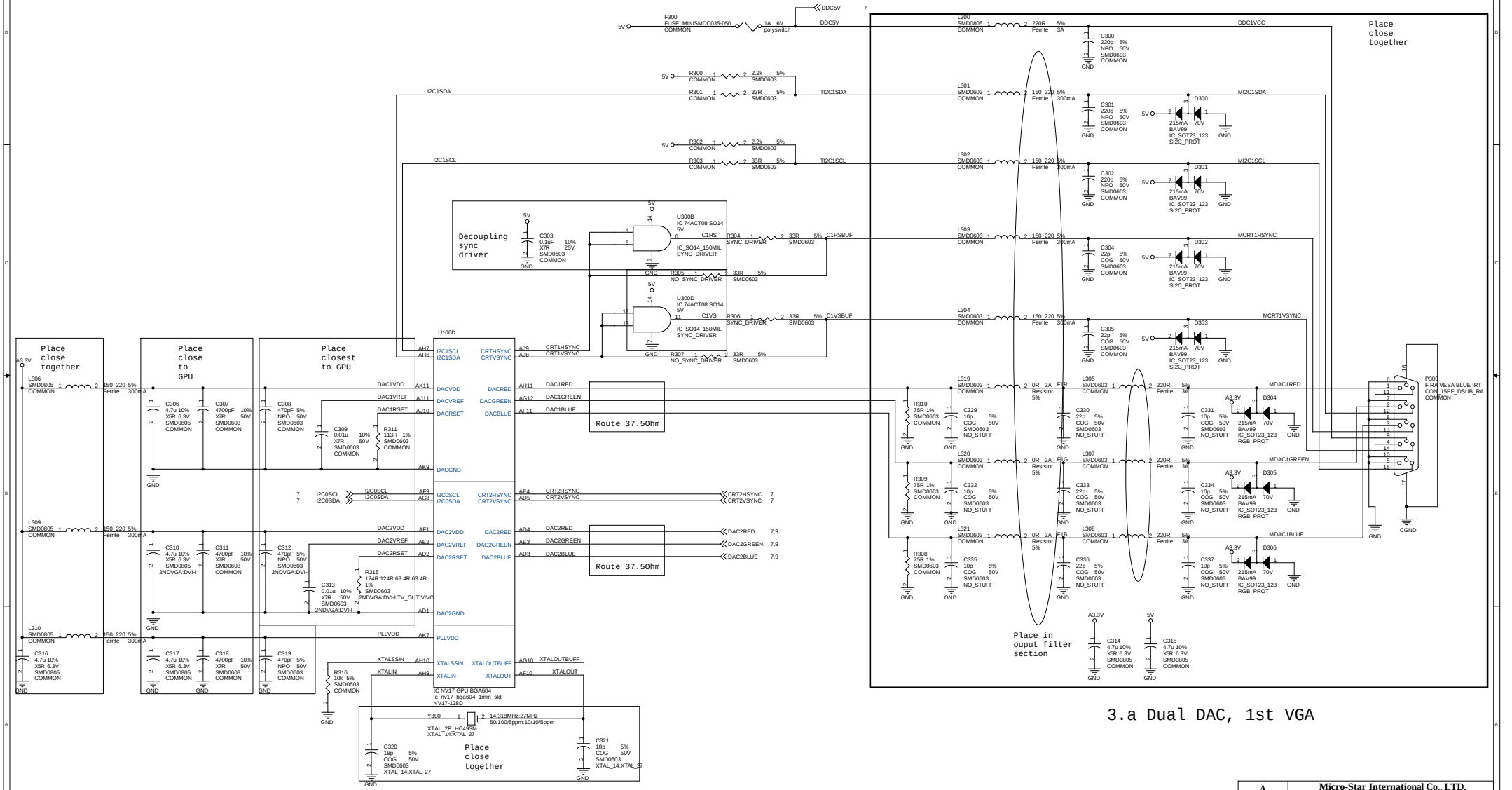


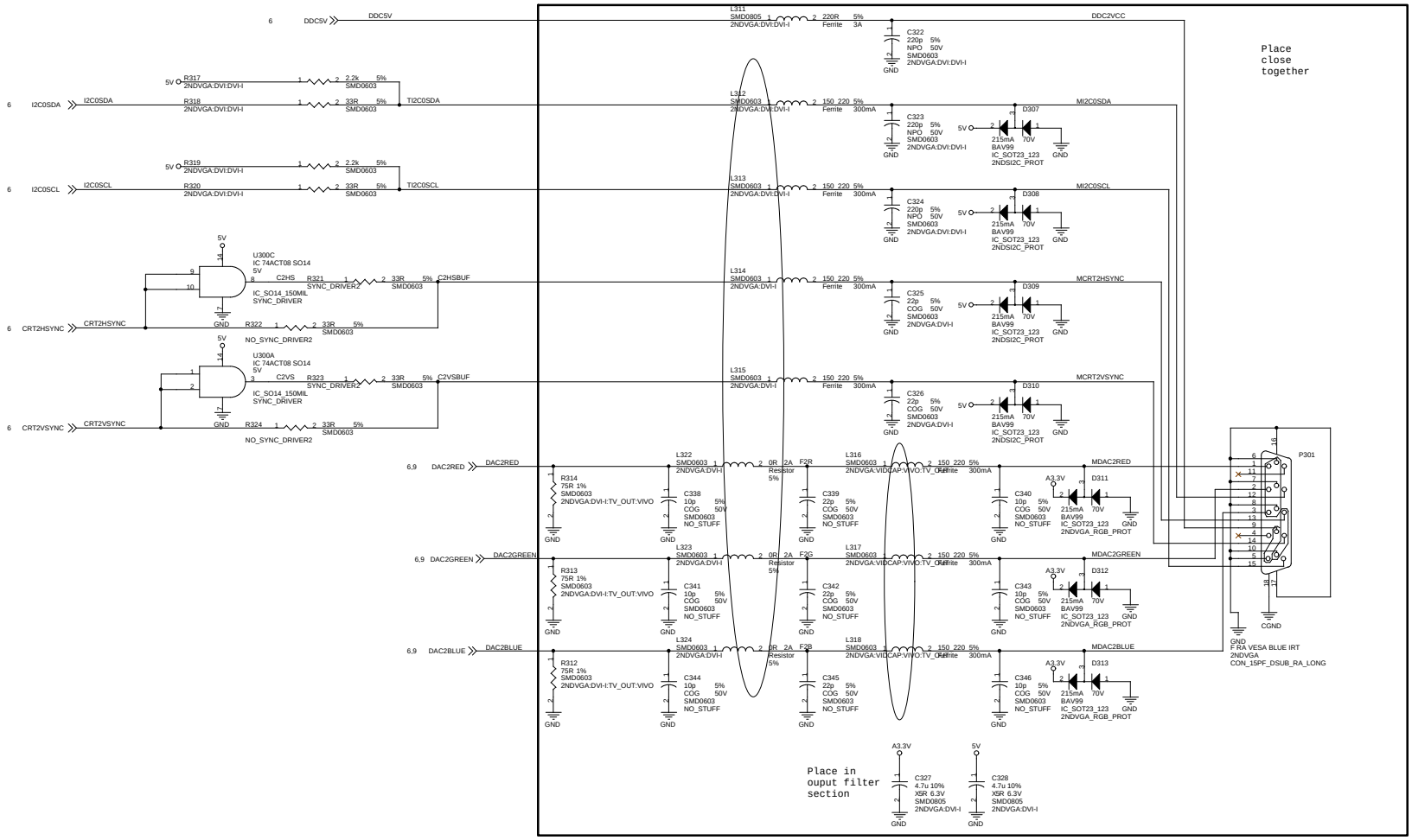
2.a NV17 Frame Buffer

Micro-Star International Co., LTD.		
<Title>		
Size: Custom	Document Number: <Doc>	Rev: <RevCod
Date: Wednesday, March 13, 2002	Sheet 3 of 13	


Place close to memory
Memory decoupling
Place close to memory
Place close to memory
Place close to memory
Memory decoupling
Place close to memory
Place close to memory
Place in memory section
Place in memory section
Place at end of stub
2.b Frame Buffer 0..63
Micro-Star International Co., LTD.
<Title>
Size Custom
Document Number <Doc>
Rev <RevCod
Date: Wednesday, March 13, 2002
Sheet 4 of 13

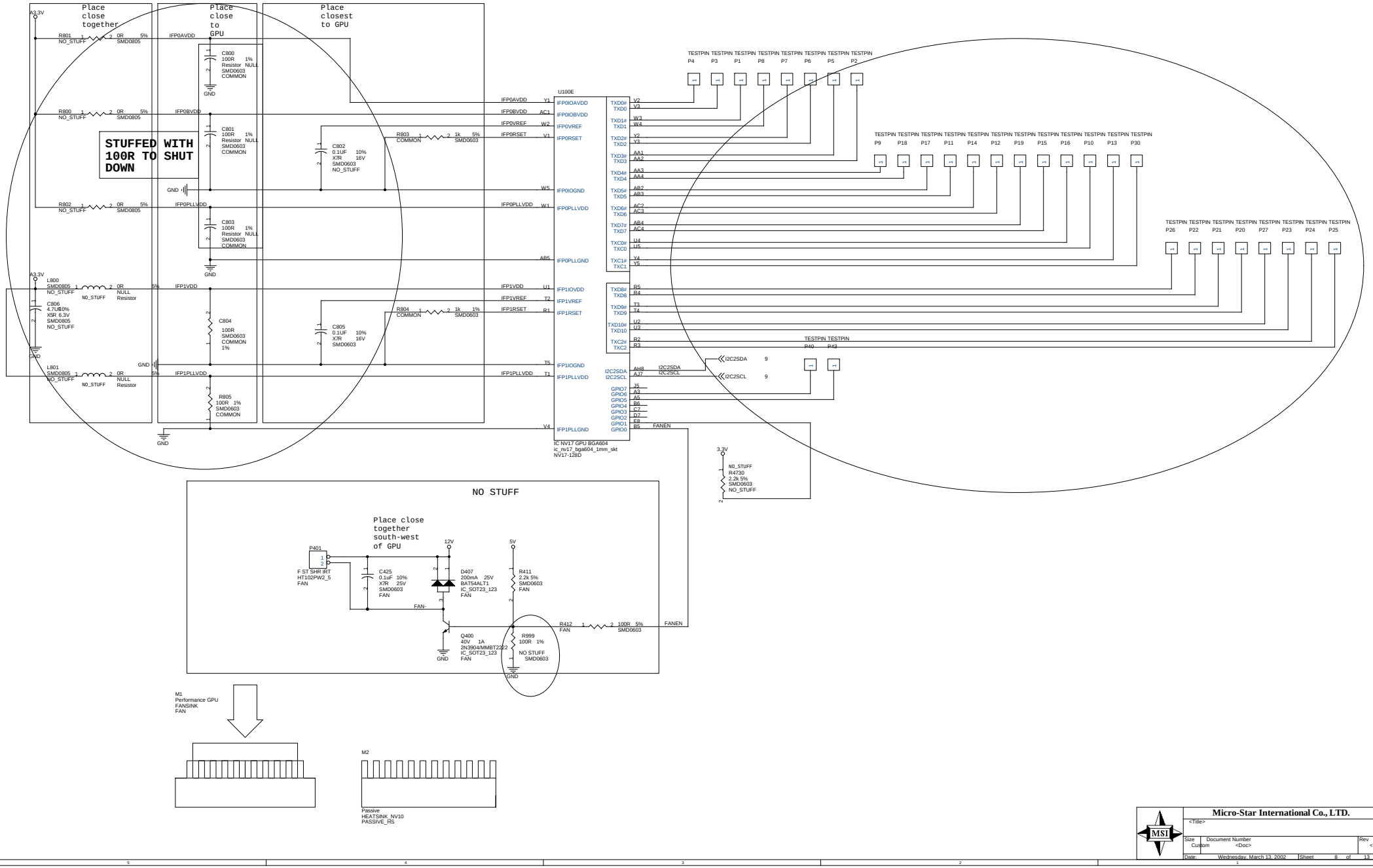

Place close to memory
Memory decoupling
Place close to memory
Place in memory section
Place at end of stub
MEM 1/2/4MX32
IC_PQFP100
MEM-128B
2.c Frame Buffer 64...127
Micro-Star International Co., LTD.
<Title>
Size Custom
Document Number <Doc>
Rev <RevCod
Date: Wednesday, March 13, 2002
Sheet 5 of 13

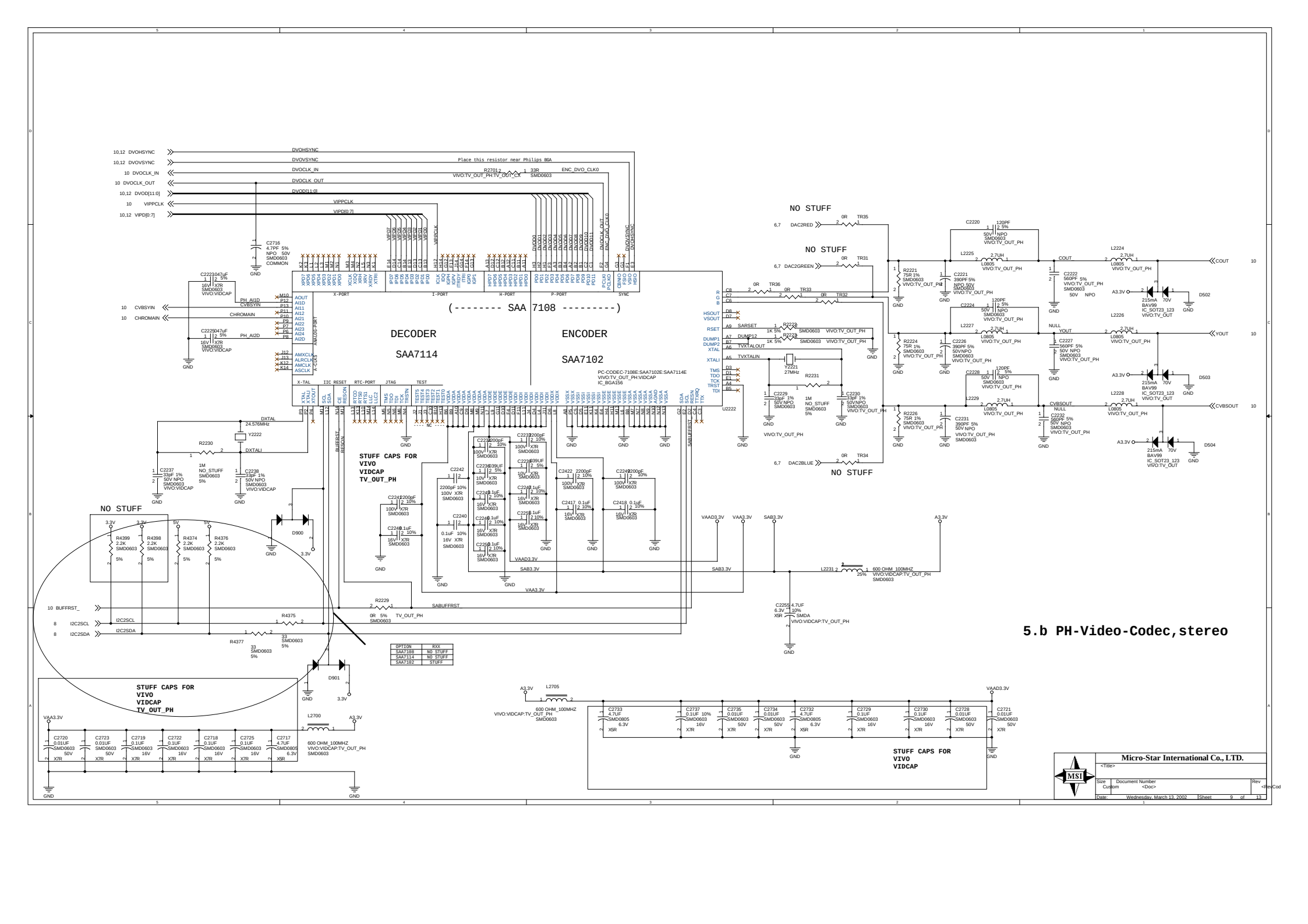

Place close together
Place close to GPU
Place closest to GPU
Decoupling sync driver
Route 37.50hm
Route 37.50hm
Place close together
Place in ouput filter section
Place close together
3.a Dual DAC, 1st VGA
Micro-Star International Co., LTD.
<Title>
Size Custom
Document Number <Doc>
Rev <RevCod
Date: Wednesday, March 13, 2002
Sheet 6 of 13

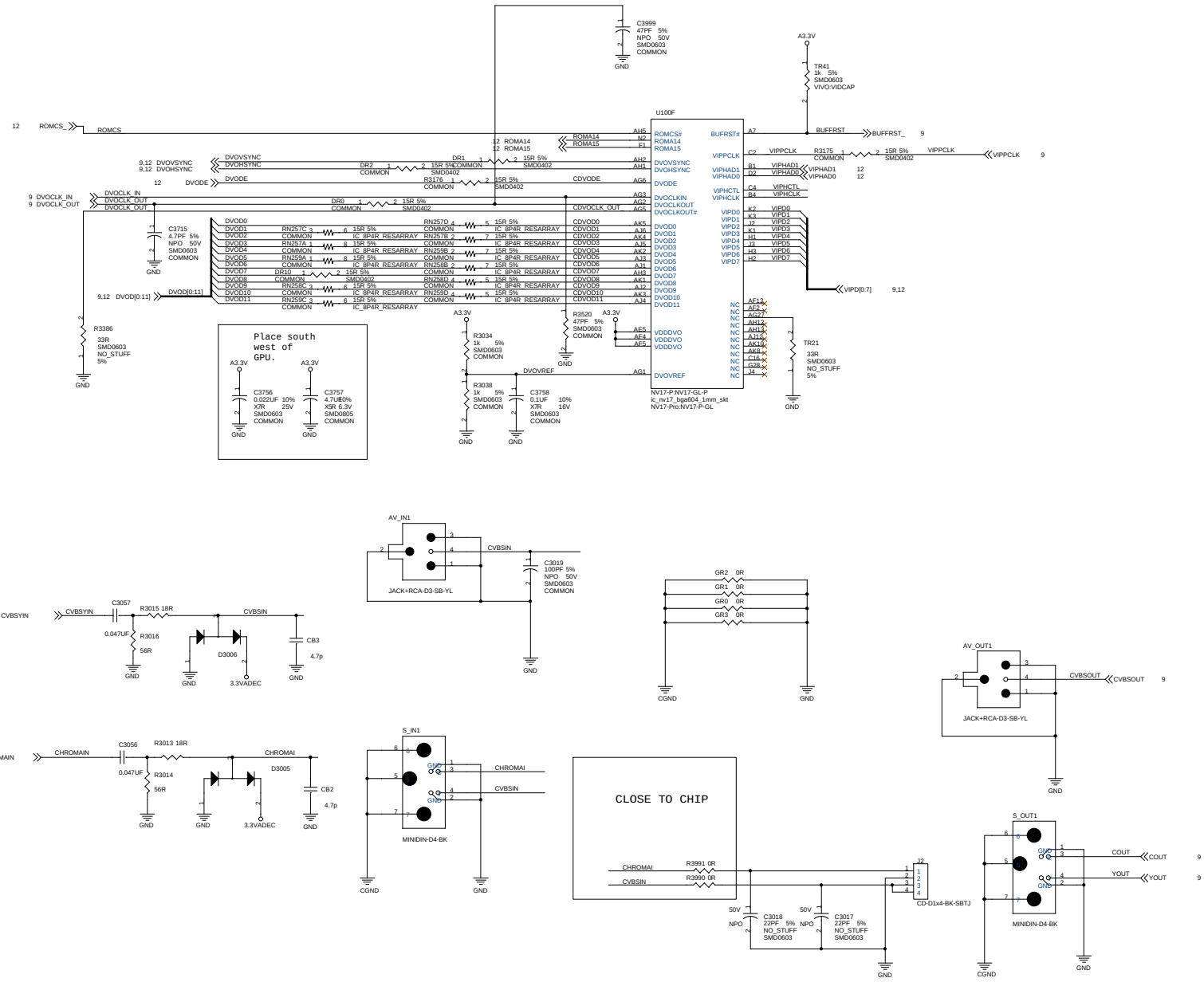


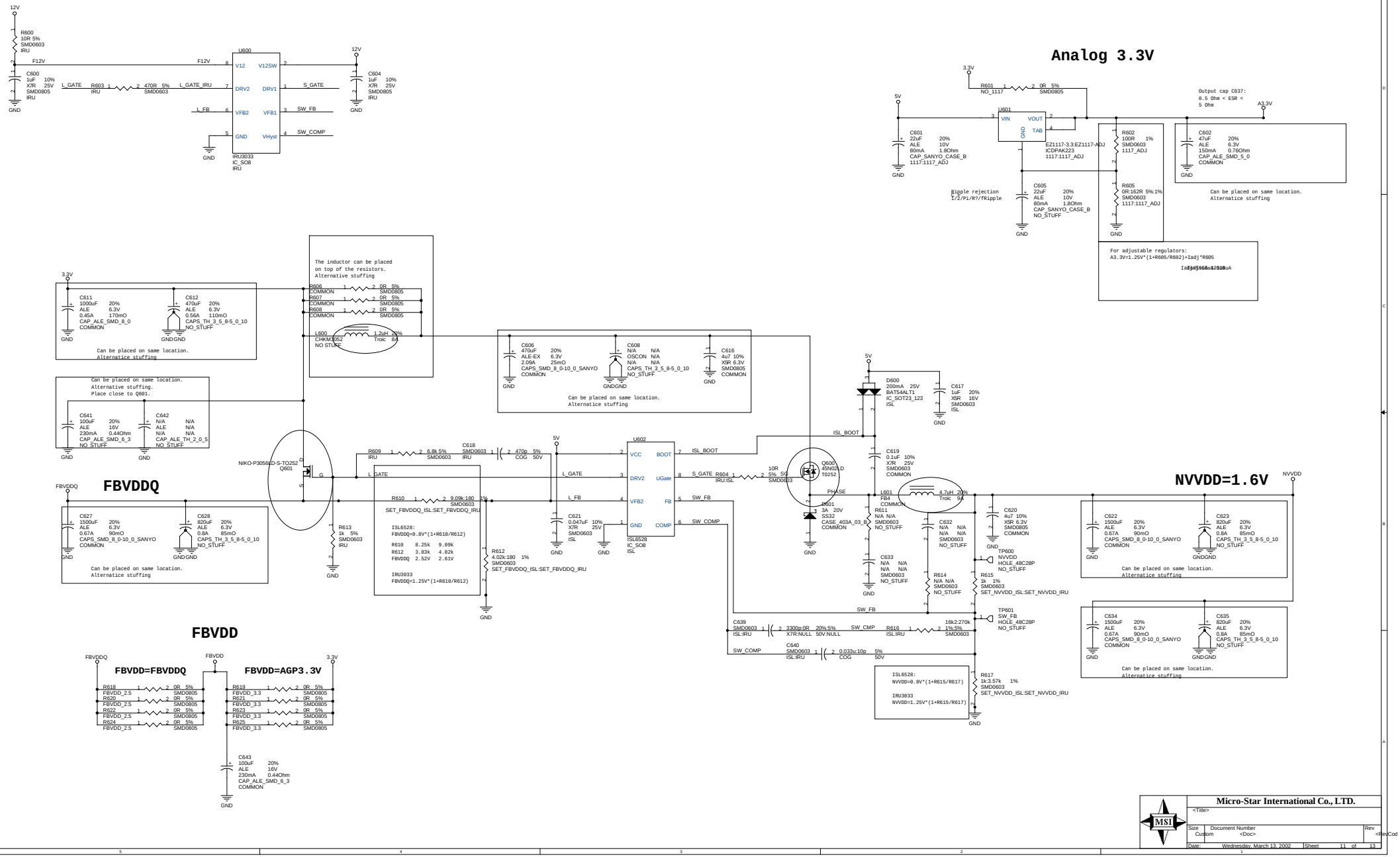
3.b Dual DAC, 2nd VGA

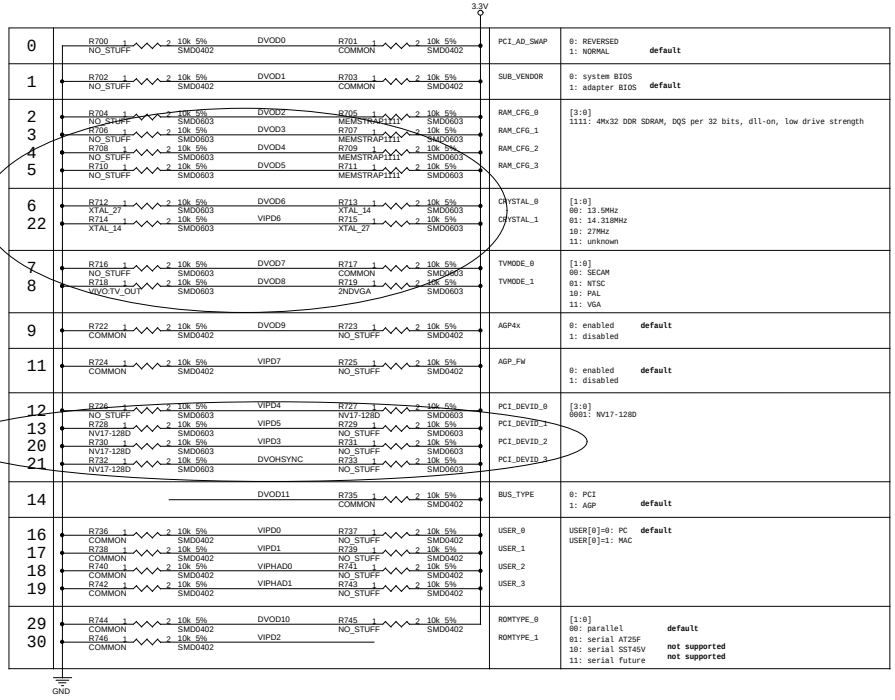
Micro-Star International Co., LTD.	
<Title>	
Size: Custom	Document Number: <Doc>
Rev: <RevCod	
Date: Wednesday, March 13, 2002	Sheet 7 of 12


Place close together
Place close to GPU
Place closest to GPU
STUFFED WITH 100R TO SHUT DOWN
U100E
IC NV17 GPU BGA604
ic_nv17_bga604_1mm_skt
NV17-128D
NO STUFF
Place close together south-west of GPU
M1
Performance GPU FANSINK
FAN
M2
Passive
HEATSINK_NV10
PASSIVE_HS
Micro-Star International Co., LTD.
<Title>
Size Custom
Document Number <Doc>
Rev <RevCod
Date: Wednesday, March 13, 2002
Sheet 8 of 13

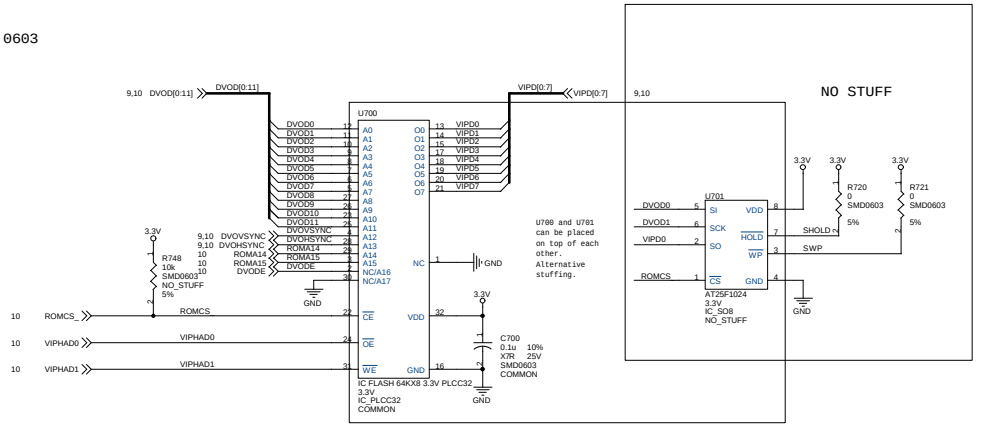

DECODER
SAA7114
ENCODER
SAA7102
(-------- SAA 7108 ---------)
NO STUFF
STUFF CAPS FOR VIVO VIDCAP TV_OUT_PH
STUFF CAPS FOR VIVO VIDCAP
5.b PH-Video-Codec,stereo
Micro-Star International Co., LTD.
<Title>
Size Custom
Document Number <Doc>
Rev <RevCod
Date: Wednesday, March 13, 2002
Sheet 9 of 13


U100F
NV17-P:NV17-GL-P
ic_nv17_bga604_1mm_skt
NV17-Pro:NV17-P-GL
Place south
west of
GPU.
AV_IN1
JACK+RCA-D3-SB-YL
S_IN1
MINIDIN-D4-BK
CLOSE TO CHIP
CD-D1x4-BK-SBTJ
AV_OUT1
S_OUT1
5.c TV out,video capture
Micro-Star International Co., LTD.
<Title>
Size
Custom
Document Number
<Doc>
Rev
<RevCod
Date:
Wednesday, March 13, 2002
Sheet
10
of
13


Analog 3.3V
FBVDDQ
FBVDD
NVVDD=1.6V
FBVDD=FBVDDQ
FBVDD=AGP3.3V
Micro-Star International Co., LTD.
<Title>
Size: Custom
Document Number: <Doc>
Rev: <RevCod
Date: Wednesday, March 13, 2002
Sheet 11 of 13



CHANGE 0402 TO 0603



7. BIOS, Strapping

Micro-Star International Co., LTD.	
<Title>	
Size: Custom	Document Number: <Doc>
Rev: <RevCod	
Date: Wednesday, March 13, 2002	Sheet 12 of 13

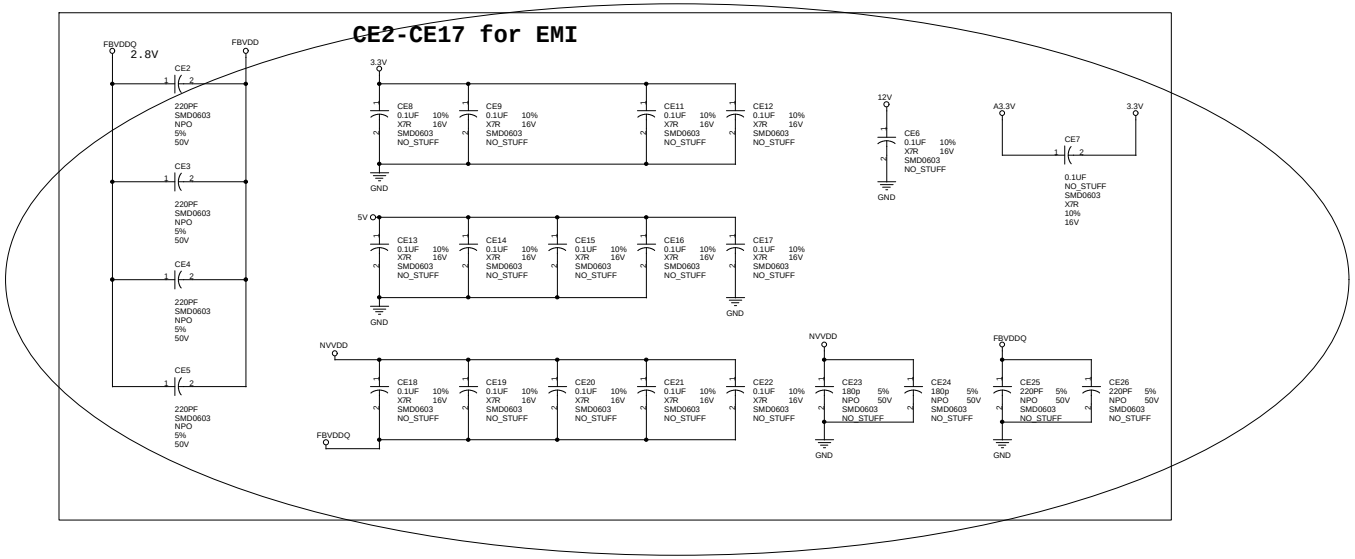
FM4 FM5 FM11 FM1 FM10 FM7

220PF F_PAD_VGA NPO 5% 50V

FM3 FM12 FM9 FM2 FM6 FM8

220PF F_PAD_VGA NPO 5% 50V

CE2-CE17 for EMI



Micro-Star International Co., LTD.		
8874 base on P75, NV17-Pro		
Size: Custom	Document Number	Rev: 00A
Date: Wednesday, March 13, 2002	Sheet 13 of 13	