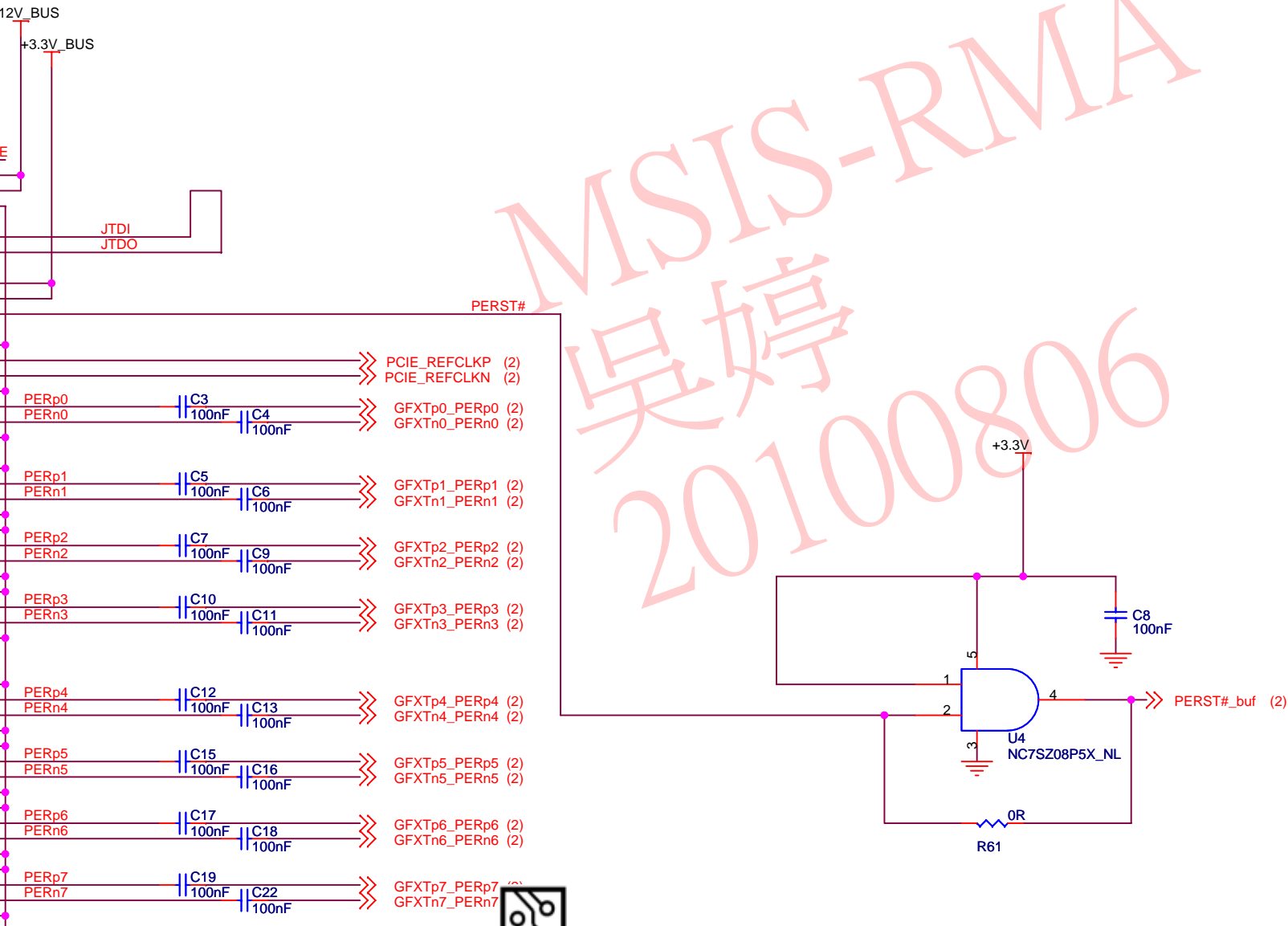
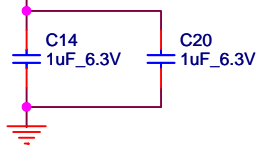


RV710 CUSTOM

VGA(header) + TVO + DVI

ECTOR





Place these caps last,
ideally as close to the bus
connector as possible

- (2) PETp8_GFXRp8
- (2) PETn8_GFXRn8
- (2) PETp9_GFXRp9
- (2) PETn9_GFXRn9
- (2) PETp10_GFXRp10
- (2) PETn10_GFXRn10
- (2) PETp11_GFXRp11
- (2) PETn11_GFXRn11
- (2) PETp12_GFXRp12
- (2) PETn12_GFXRn12
- (2) PETp13_GFXRp13
- (2) PETn13_GFXRn13
- (2) PETp14_GFXRp14
- (2) PETn14_GFXRn14
- (2) PETp15_GFXRp15
- (2) PETn15_GFXRn15

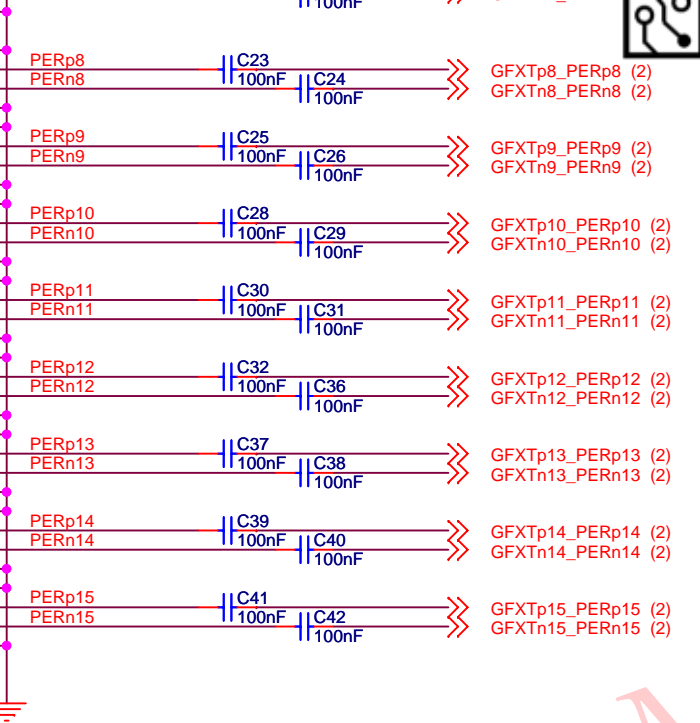
- B49 GND#B49
- B50 PETp8
- B51 PETn8
- B52 GND#B52
- B53 GND#B53
- B54 PETp9
- B55 PETn9
- B56 GND#B56
- B57 GND#B57
- B58 PETp10
- B59 PETn10
- B60 GND#B60
- B61 GND#B61
- B62 PETp11
- B63 PETn11
- B64 GND#B64
- B65 GND#B65
- B66 PETp12
- B67 PETn12
- B68 GND#B68
- B69 GND#B69
- B70 PETp13
- B71 PETn13
- B72 GND#B72
- B73 GND#B73
- B74 PETp14
- B75 PETn14
- B76 GND#B76
- B77 GND#B77
- B78 PETp15
- B79 PETn15
- B80 GND#B80
- B81 PRSNT2#B81
- B82 RSVD#B82

PRESENCE

- GND#A49 A49
- RSVD#A50 A50
- GND#A51 A51
- PERp8 A52
- PERn8 A53
- GND#A54 A54
- GND#A55 A55
- PERp9 A56
- PERn9 A57
- GND#A58 A58
- GND#A59 A59
- PERp10 A60
- PERn10 A61
- GND#A62 A62
- GND#A63 A63
- PERp11 A64
- PERn11 A65
- GND#A66 A66
- GND#A67 A67
- PERp12 A68
- PERn12 A69
- GND#A70 A70
- GND#A71 A71
- PERp13 A72
- PERn13 A73
- GND#A74 A74
- GND#A75 A75
- PERp14 A76
- PERn14 A77
- GND#A78 A78
- GND#A79 A79
- PERp15 A80
- PERn15 A81
- GND#A82 A82

MPCIE1

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SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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NOTE: some of the PCIe testpoints will
be available through via on traces.



D

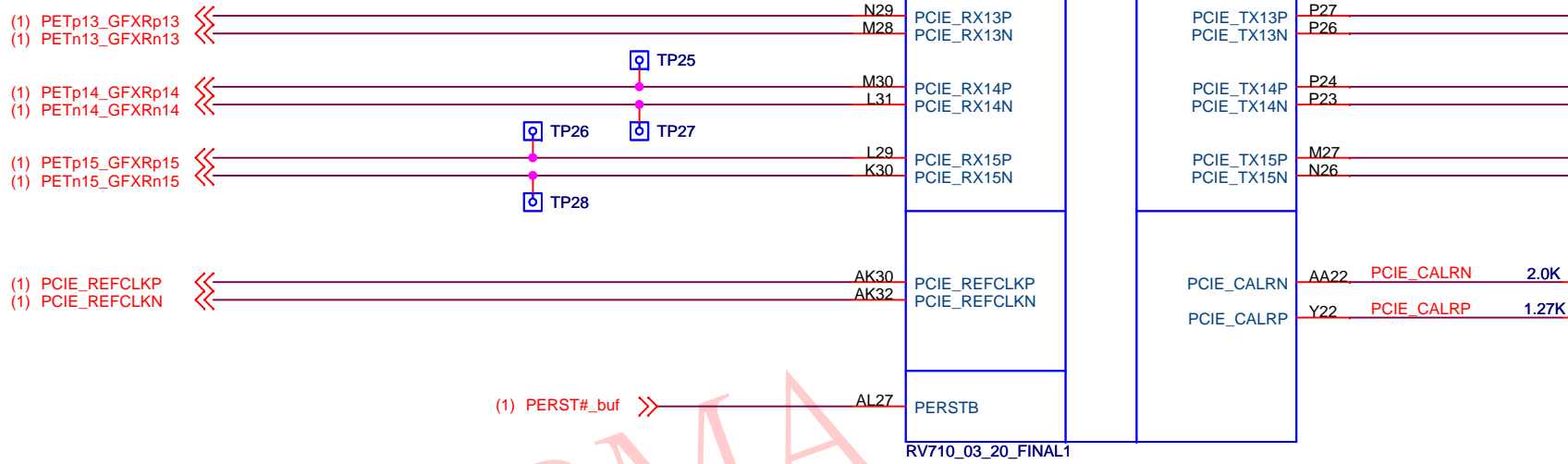
C

- GFXTp0_PERp0 (1)
GFXTn0_PERn0 (1)
- GFXTp1_PERp1 (1)
GFXTn1_PERn1 (1)
- GFXTp2_PERp2 (1)
GFXTn2_PERn2 (1)
- GFXTp3_PERp3 (1)
GFXTn3_PERn3 (1)
- GFXTp4_PERp4 (1)
GFXTn4_PERn4 (1)
- GFXTp5_PERp5 (1)
GFXTn5_PERn5 (1)
- GFXTp6_PERp6 (1)
GFXTn6_PERn6 (1)
- GFXTp7_PERp7 (1)
GFXTn7_PERn7 (1)
- GFXTp8_PERp8 (1)
GFXTn8_PERn8 (1)
- GFXTp9_PERp9 (1)
GFXTn9_PERn9 (1)
- GFXTp10_PERp10 (1)
GFXTn10_PERn10 (1)
- GFXTp11_PERp11 (1)
GFXTn11_PERn11 (1)
- GFXTp12_PERp12 (1)
GFXTn12_PERn12 (1)

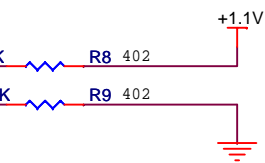
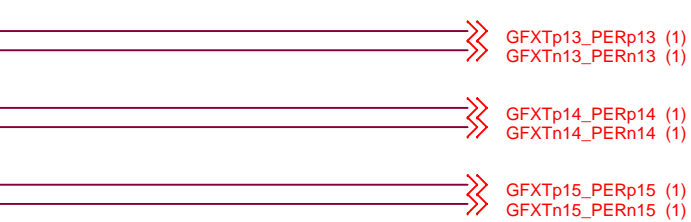
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U1B

PART 2 OF 10

DVP PORT

DAC1

U1 DVPCLK
 AC7 DVP_CNTL_0
 Y2 DVP_CNTL_1
 U5 DVP_CNTL_2
 AA1 DVP_CNTL_MVP_0
 Y4 DVP_CNTL_MVP_1

Y7 DVPDATA_0
 V2 DVPDATA_1
 Y8 DVPDATA_2
 V4 DVPDATA_3
 AB7 DVPDATA_4
 AB8 DVPDATA_5
 W3 DVPDATA_6
 AB9 DVPDATA_7
 W5 DVPDATA_8
 AC6 DVPDATA_9
 W6 DVPDATA_10
 AD7 DVPDATA_11
 AA3 DVPDATA_12
 AC8 DVPDATA_13
 AA5 DVPDATA_14
 AE8 DVPDATA_15
 AA6 DVPDATA_16
 AE9 DVPDATA_17
 AB4 DVPDATA_18
 AD9 DVPDATA_19
 AB2 DVPDATA_20
 AC10 DVPDATA_21
 AC5 DVPDATA_22
 DVPDATA_23

I/O

DAC2

R AM26 A_R_DAC1 (16)
 RB AK26 A_RB_DAC1 (16)
 G AL25 A_G_DAC1 (16)
 GB AJ25 A_GB_DAC1 (16)

B AH24 A_B_DAC1 (16)
 BB AG25 A_BB_DAC1 (16)

HSYNC AH26 A_HSYNC_DAC1 (10,16)
 VSYNC AJ27 A_VSYNC_DAC1 (10,16)

AVDD AG24 +AVDD

AVSSQ AE22

VDD1DI AE23 +VDD1DI

VSS1DI AD23

RSET AD22 RSET R12 499R

R2 AM12 A_R_DAC2 (17)
 R2B AK12 A_RB_DAC2 (17)

G2 AL11 A_G_DAC2 (17)
 G2B AJ11 A_GB_DAC2 (17)

B2 AK10 A_B_DAC2 (17)
 B2B AL9 A_BB_DAC2 (17)

H2SYNC AL13 A_HSYNC_DAC2 (17)
 V2SYNC AJ13 A_VSYNC_DAC2 (17)

C AH12

Y AM10

COMP AJ9

C1050 10nF 10V X7R 402 10%
 C1051 100nF 10V X5R 402 10%
 C1052 1uF_6.3V 6.3V 402

C1053 10nF 10V X7R 402 10%
 C1054 100nF 10V X5R 402 10%
 C1055 1uF_6.3V 6.3V 402

Place very close to ASIC balls

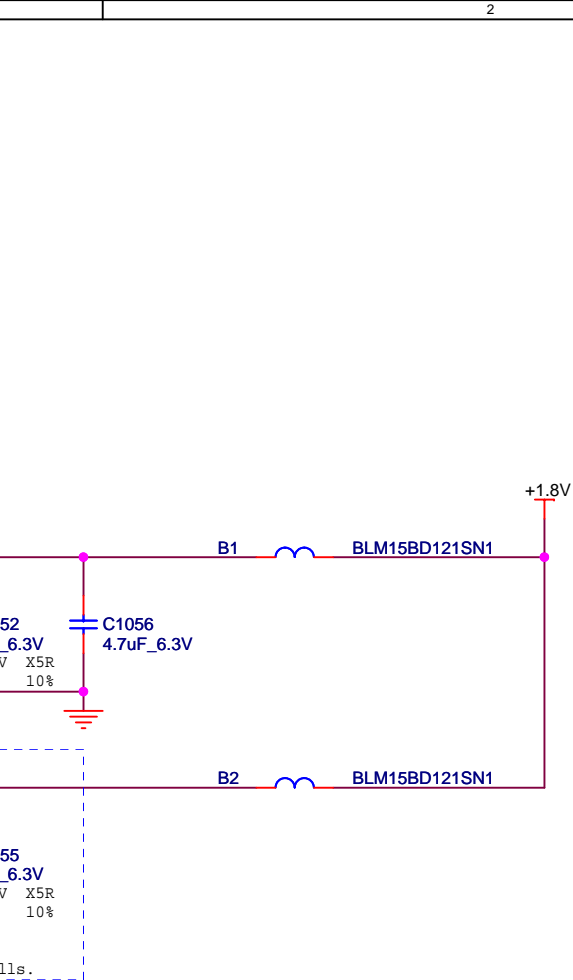
(10) GPIO_0
 (10) GPIO_1
 (10) GPIO_2
 (1) GPIO_3
 (1) GPIO_4
 (10) GPIO_5
 (10) GPIO_7
 (10) GPIO_8
 (10) GPIO_9
 (10) GPIO_11
 (10) GPIO_12
 (10) GPIO_13
 (10) GPIO_16

GPIO_22 R16 33R GPIO_22 CS

JTAG_TRSTB

R62 1K

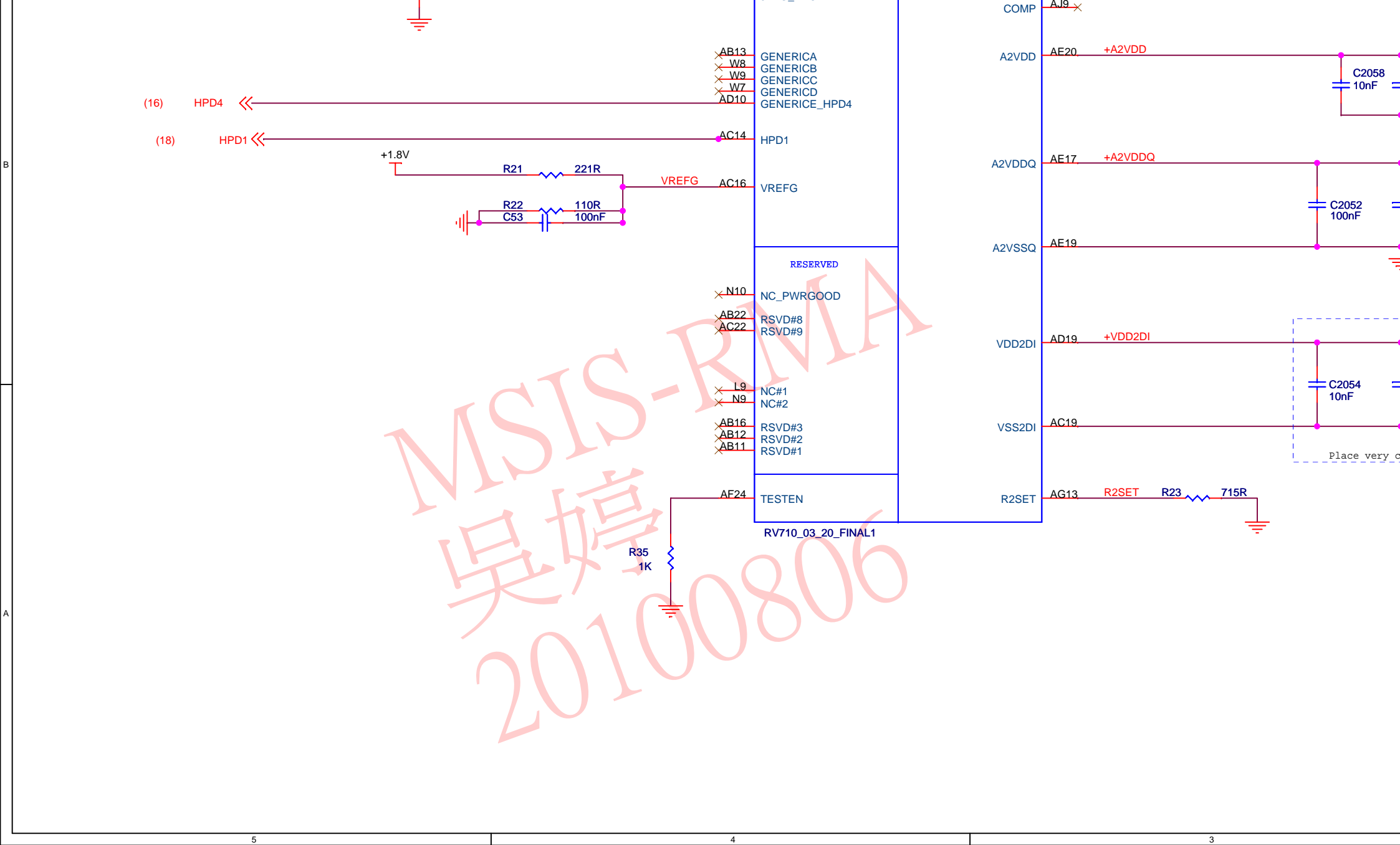
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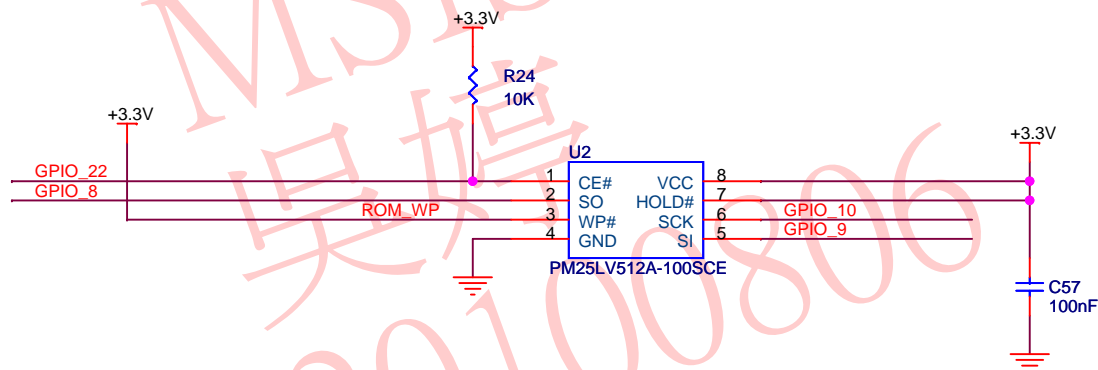
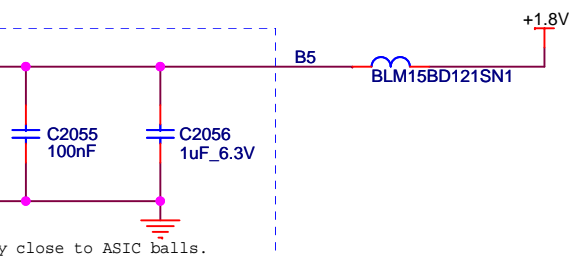
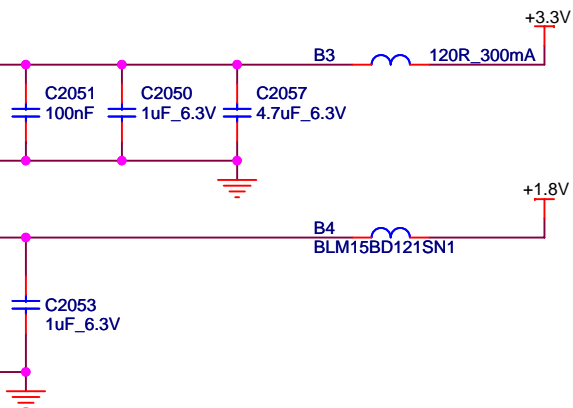


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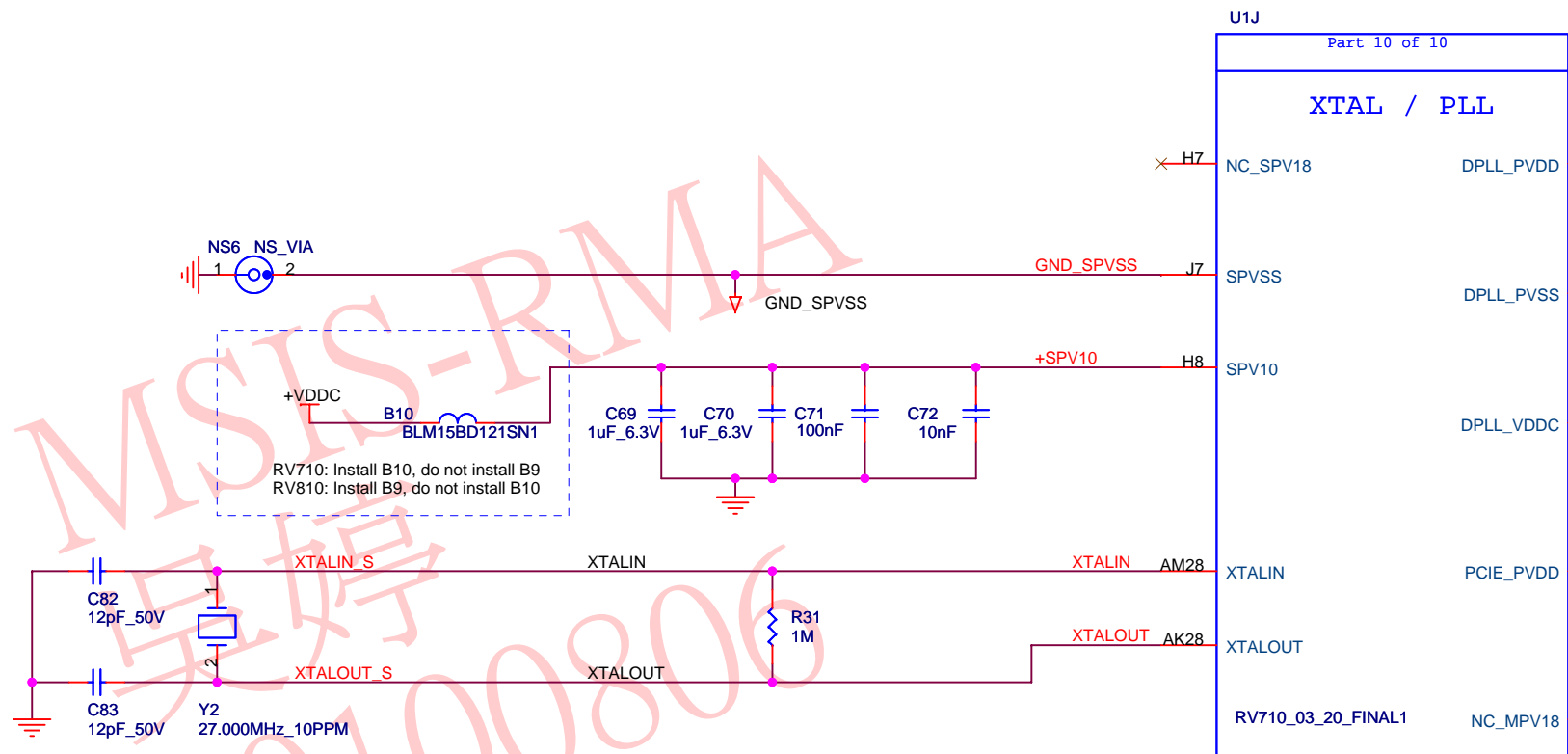
D

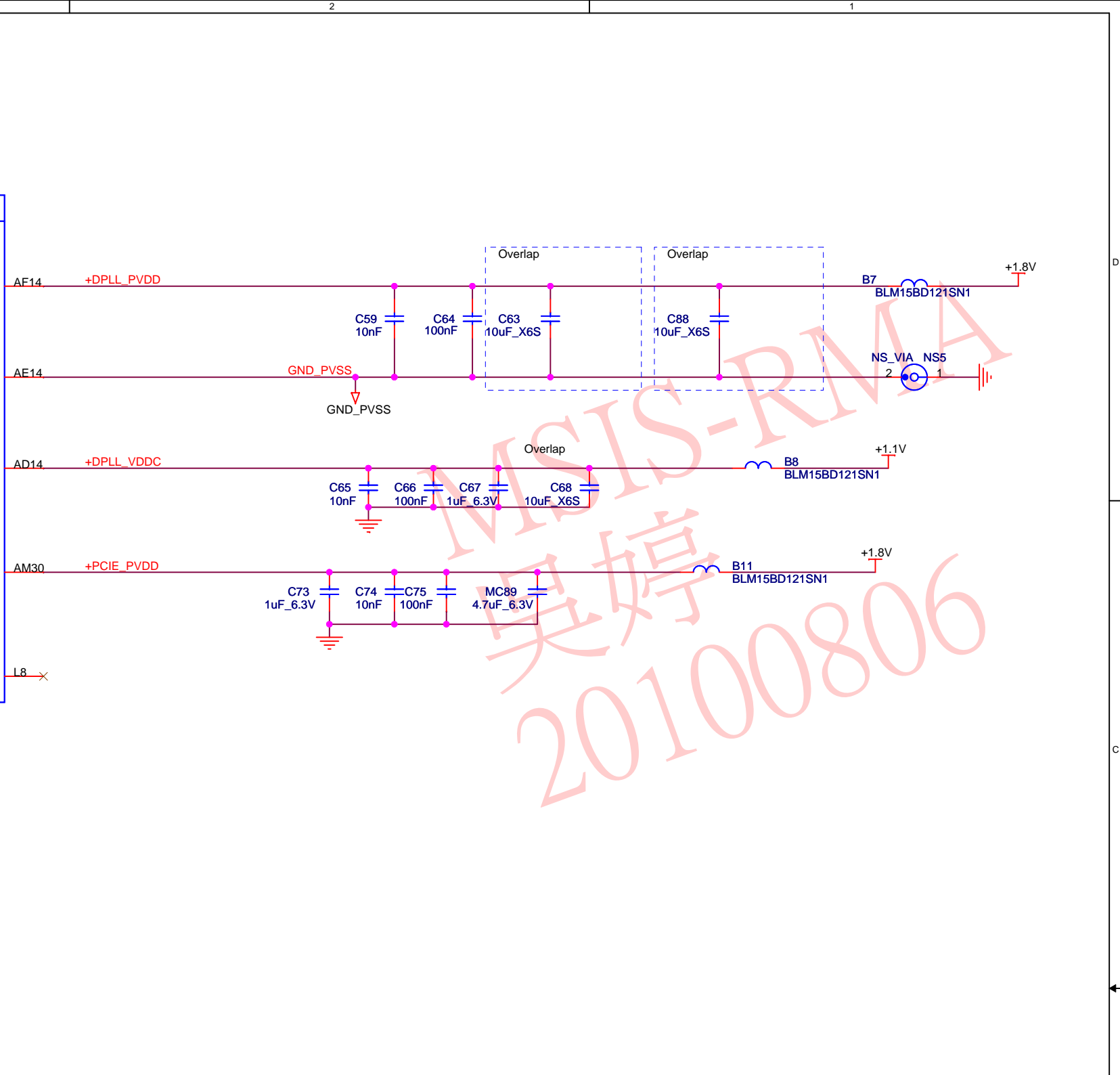
C





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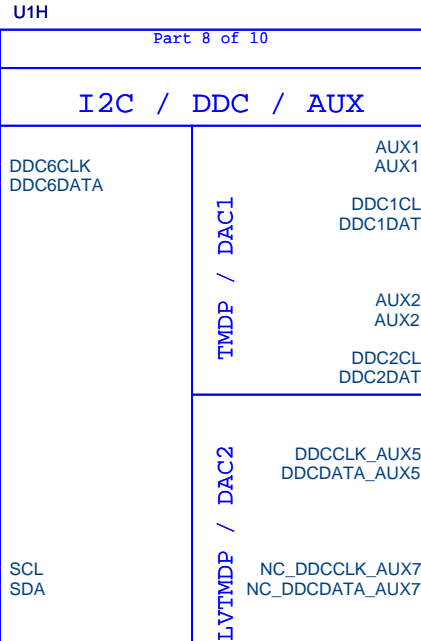
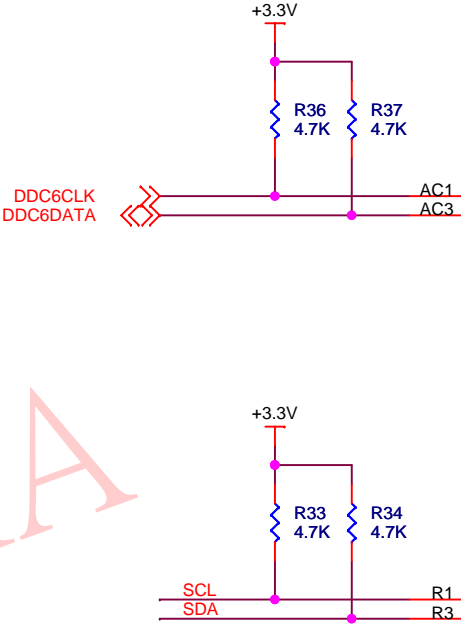


DDC6 BUS:

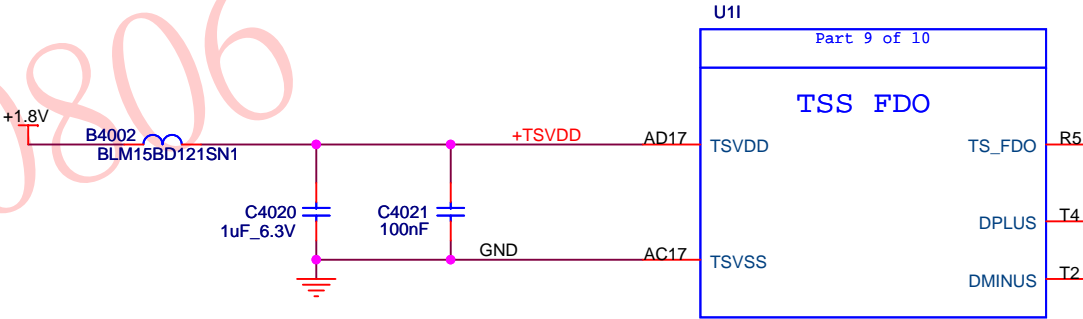
I2C Address	Function	Device
0x90	I2C VDDC Control	DS4402
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A




RV710_03_20_FINAL1



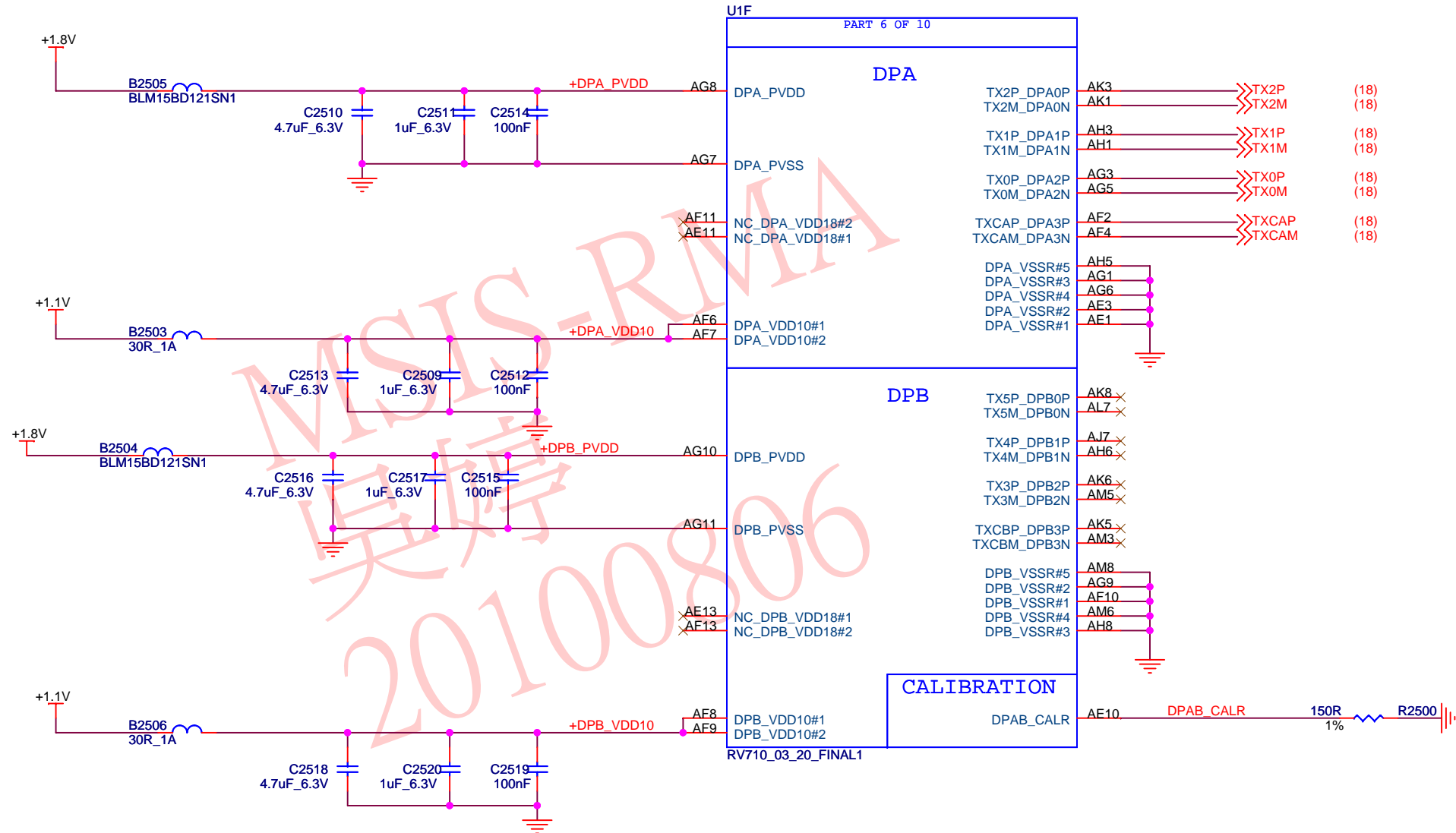
RV710_03_20_FINAL1



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TMDP INTERFACE



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Title RH LP RV710 DDR2 VOLTAGE REGULATOR


5

4

3

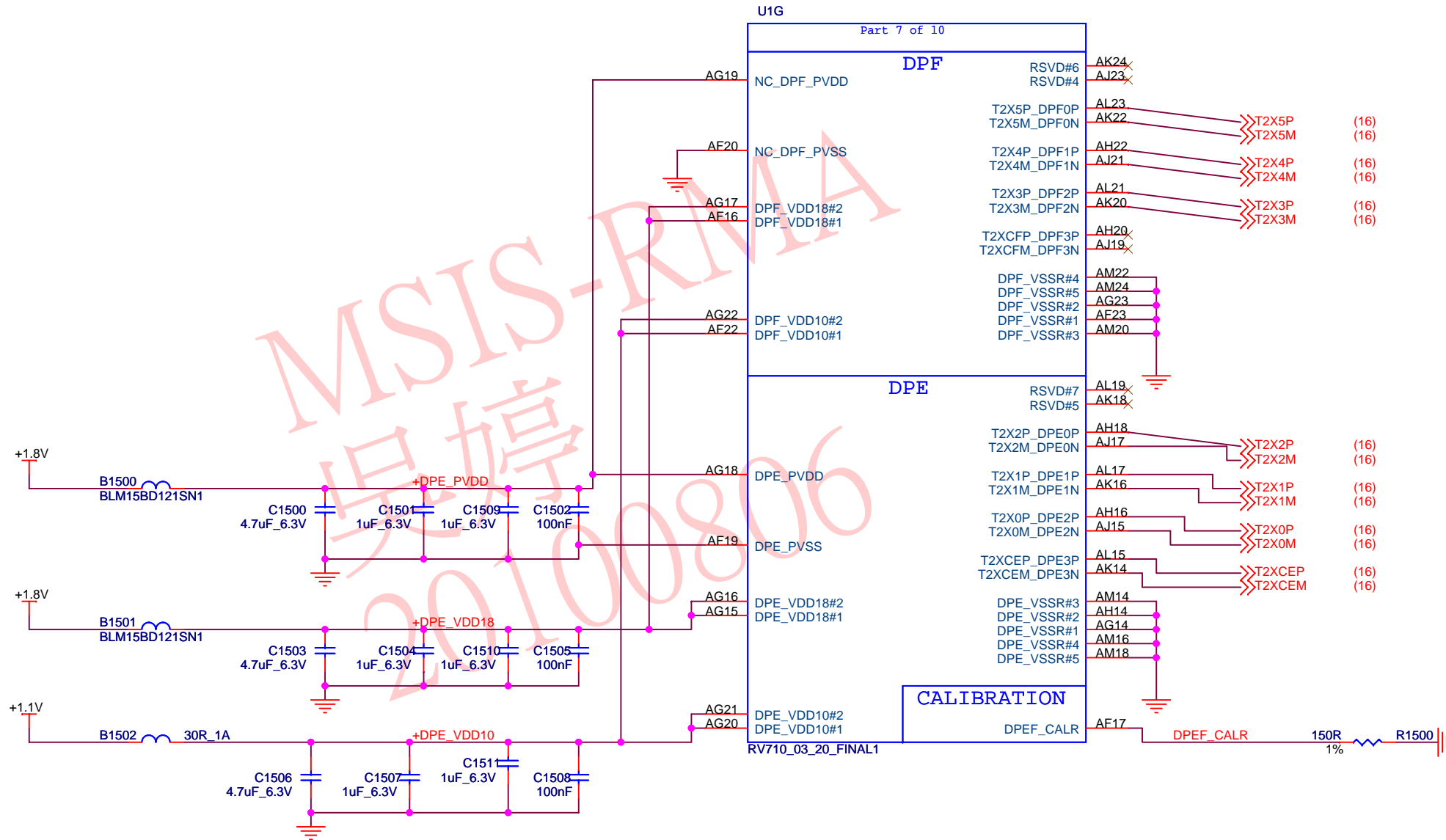
2

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LVTMDP INTERFACE



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3

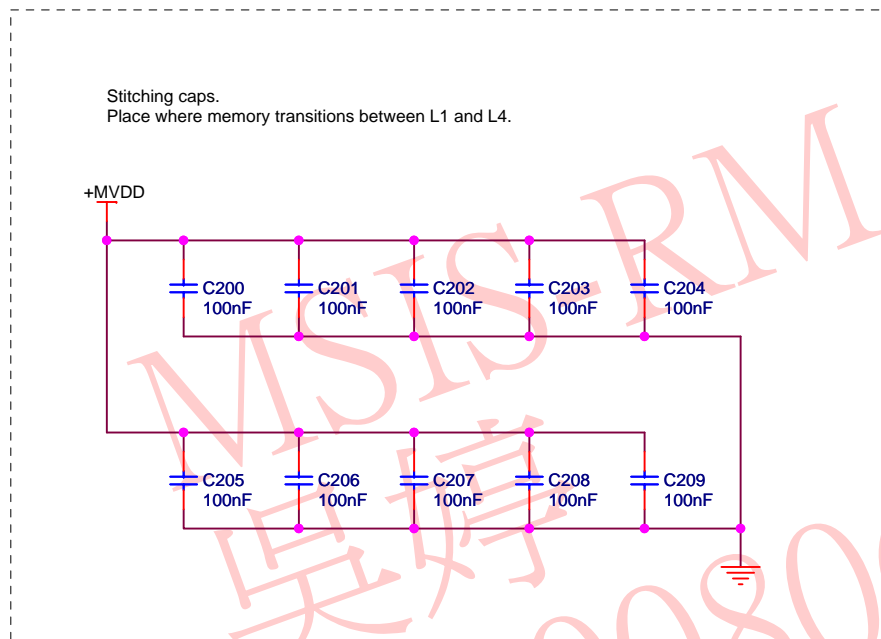
2

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		1	

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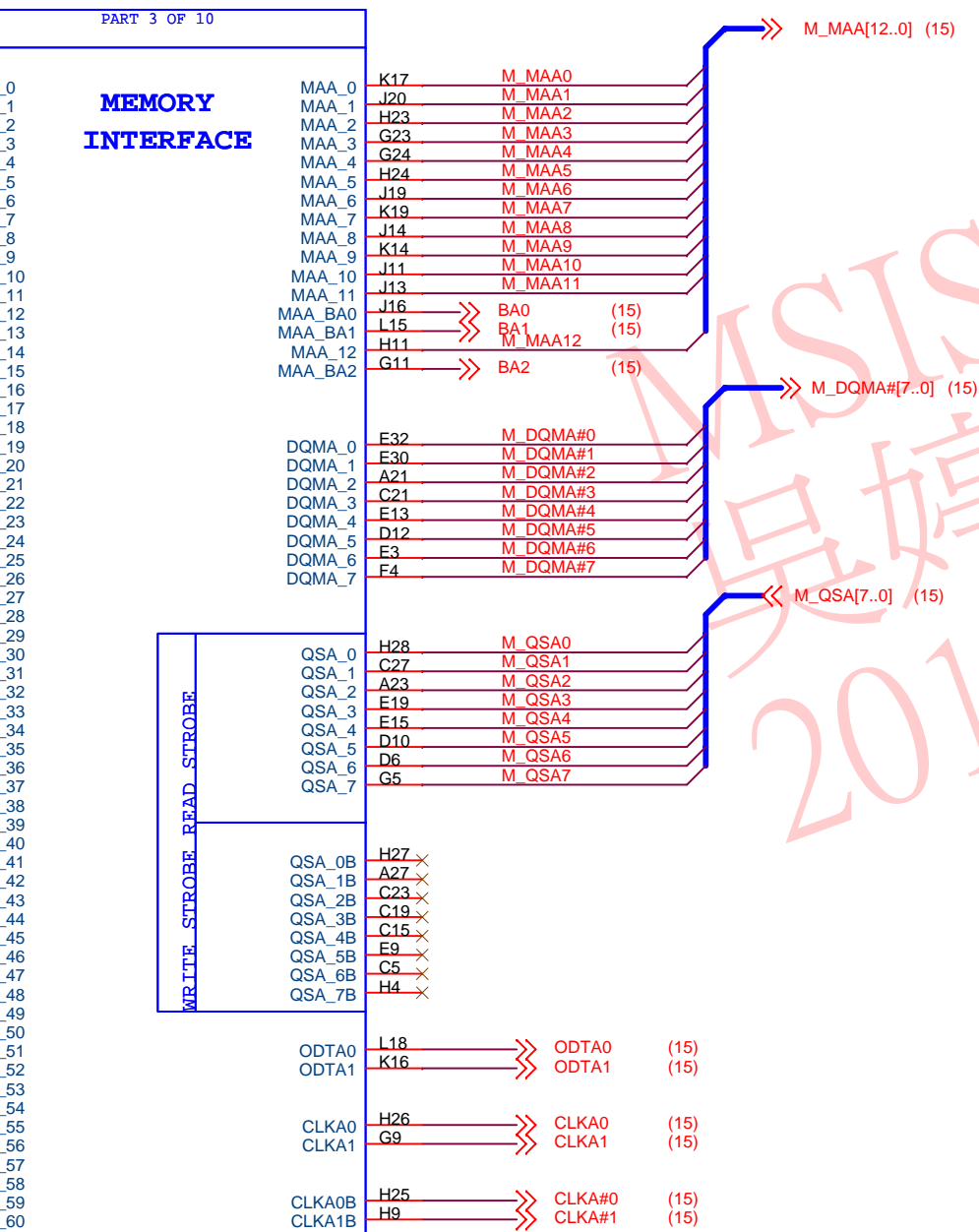
(15) M_MDA[63..0] <<>



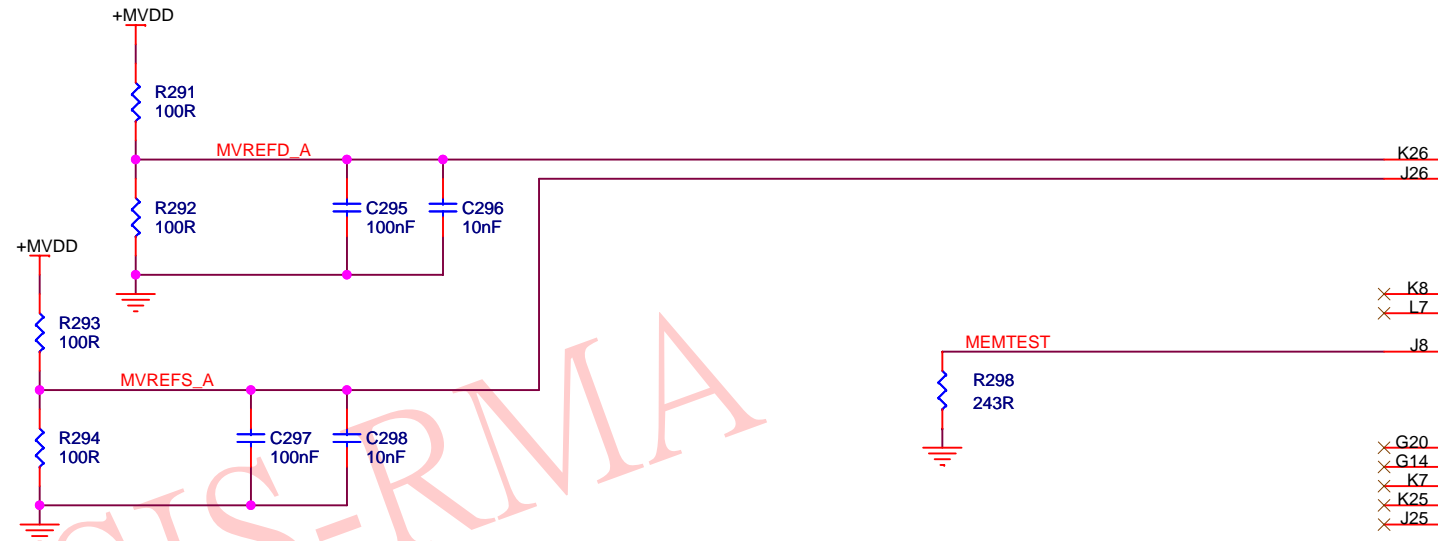
U1C

M_MDA0	K27	DQA_0
M_MDA1	J29	DQA_1
M_MDA2	H30	DQA_2
M_MDA3	H32	DQA_3
M_MDA4	G29	DQA_4
M_MDA5	F28	DQA_5
M_MDA6	F32	DQA_6
M_MDA7	F30	DQA_7
M_MDA8	C30	DQA_8
M_MDA9	F27	DQA_9
M_MDA10	A28	DQA_10
M_MDA11	C28	DQA_11
M_MDA12	E27	DQA_12
M_MDA13	G26	DQA_13
M_MDA14	D26	DQA_14
M_MDA15	F25	DQA_15
M_MDA16	A25	DQA_16
M_MDA17	C25	DQA_17
M_MDA18	E25	DQA_18
M_MDA19	D24	DQA_19
M_MDA20	E23	DQA_20
M_MDA21	F23	DQA_21
M_MDA22	D22	DQA_22
M_MDA23	F21	DQA_23
M_MDA24	E21	DQA_24
M_MDA25	D20	DQA_25
M_MDA26	F19	DQA_26
M_MDA27	A19	DQA_27
M_MDA28	D18	DQA_28
M_MDA29	F17	DQA_29
M_MDA30	A17	DQA_30
M_MDA31	C17	DQA_31
M_MDA32	E17	DQA_32
M_MDA33	D16	DQA_33
M_MDA34	F15	DQA_34
M_MDA35	A15	DQA_35
M_MDA36	D14	DQA_36
M_MDA37	F13	DQA_37
M_MDA38	A13	DQA_38
M_MDA39	C13	DQA_39
M_MDA40	E11	DQA_40
M_MDA41	A11	DQA_41
M_MDA42	C11	DQA_42
M_MDA43	F11	DQA_43
M_MDA44	A9	DQA_44
M_MDA45	C9	DQA_45
M_MDA46	F9	DQA_46
M_MDA47	D8	DQA_47
M_MDA48	E7	DQA_48
M_MDA49	A7	DQA_49
M_MDA50	C7	DQA_50
M_MDA51	F7	DQA_51
M_MDA52	A5	DQA_52
M_MDA53	E5	DQA_53
M_MDA54	C3	DQA_54
M_MDA55	E1	DQA_55
M_MDA56	G7	DQA_56
M_MDA57	G6	DQA_57
M_MDA58	G1	DQA_58
M_MDA59	G3	DQA_59
M_MDA60	J6	DQA_60
M_MDA61	J1	DQA_60

MEMORY INTERFACE



M_MDA60	J6	DQA_60
M_MDA61	J1	DQA_61
M_MDA62	J3	DQA_62
M_MDA63	J5	DQA_63



DIVIDER RESISTORS	DDR2
MVREF TO 1.8V	100R
MVREF TO GND	100R

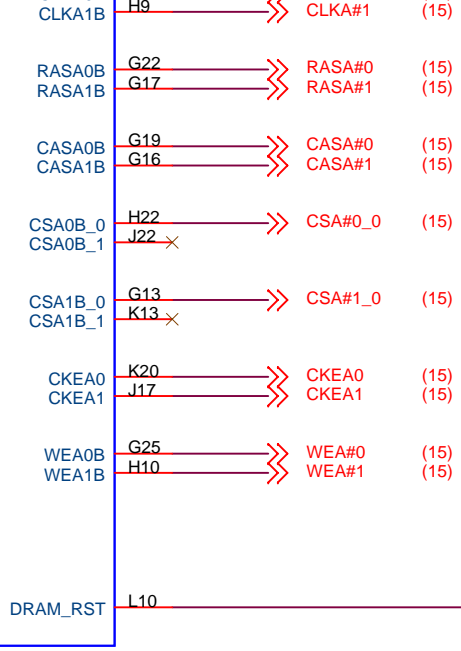
61
62
_63

EFDA
EFSA

ESTA
ESTB

_CALRP1


MAA_13
MAA_14
MEM_CALRN1
MEM_CALRP0
MEM_CALRNO
_03_20_FINAL1

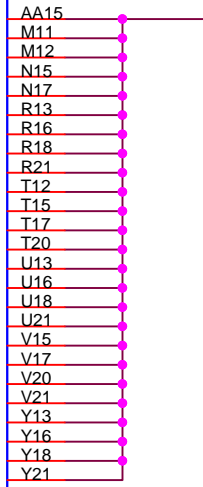
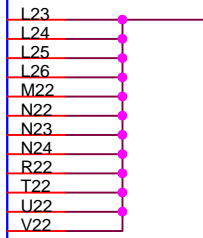
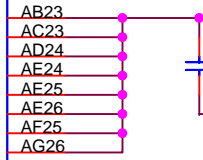
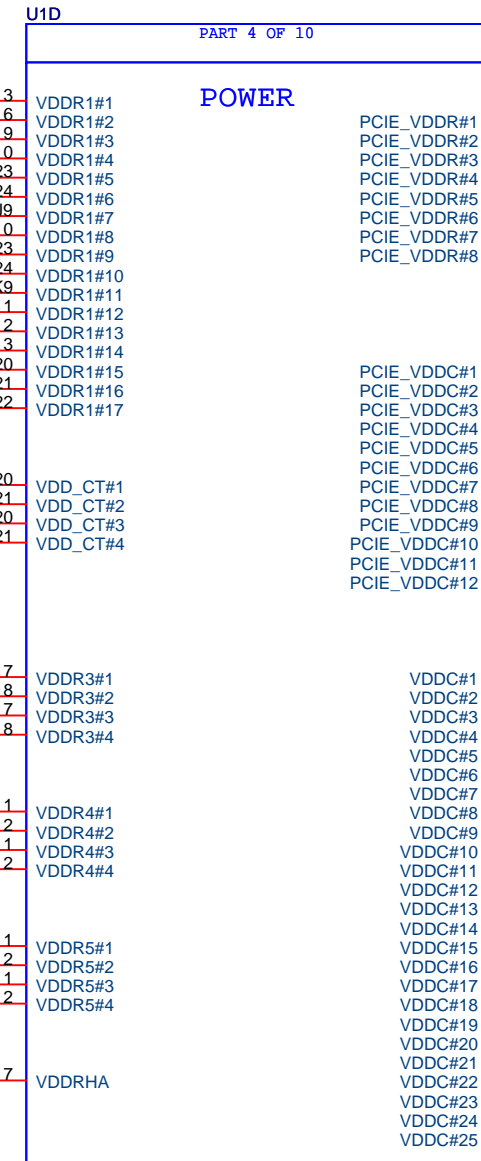
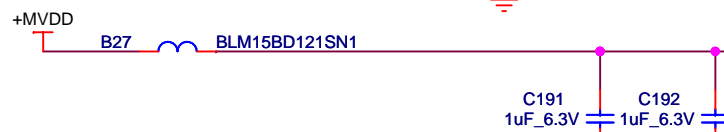
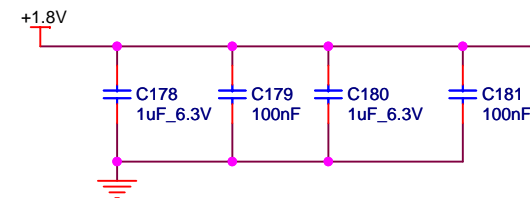
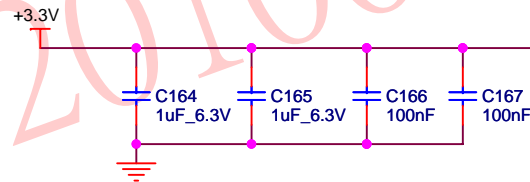
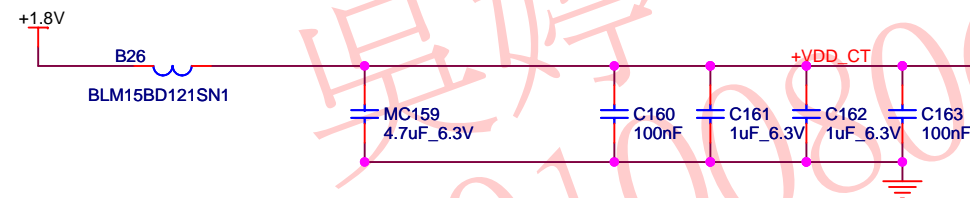
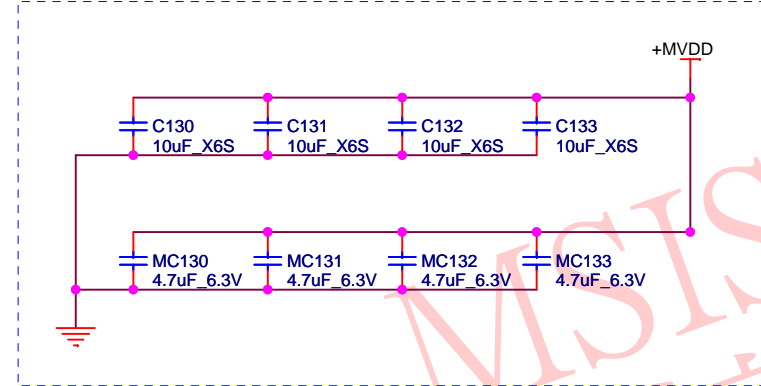
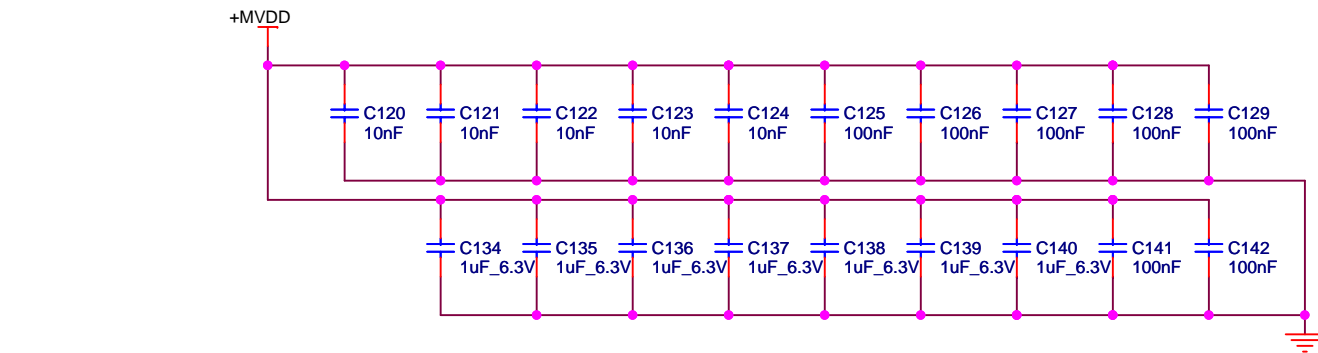


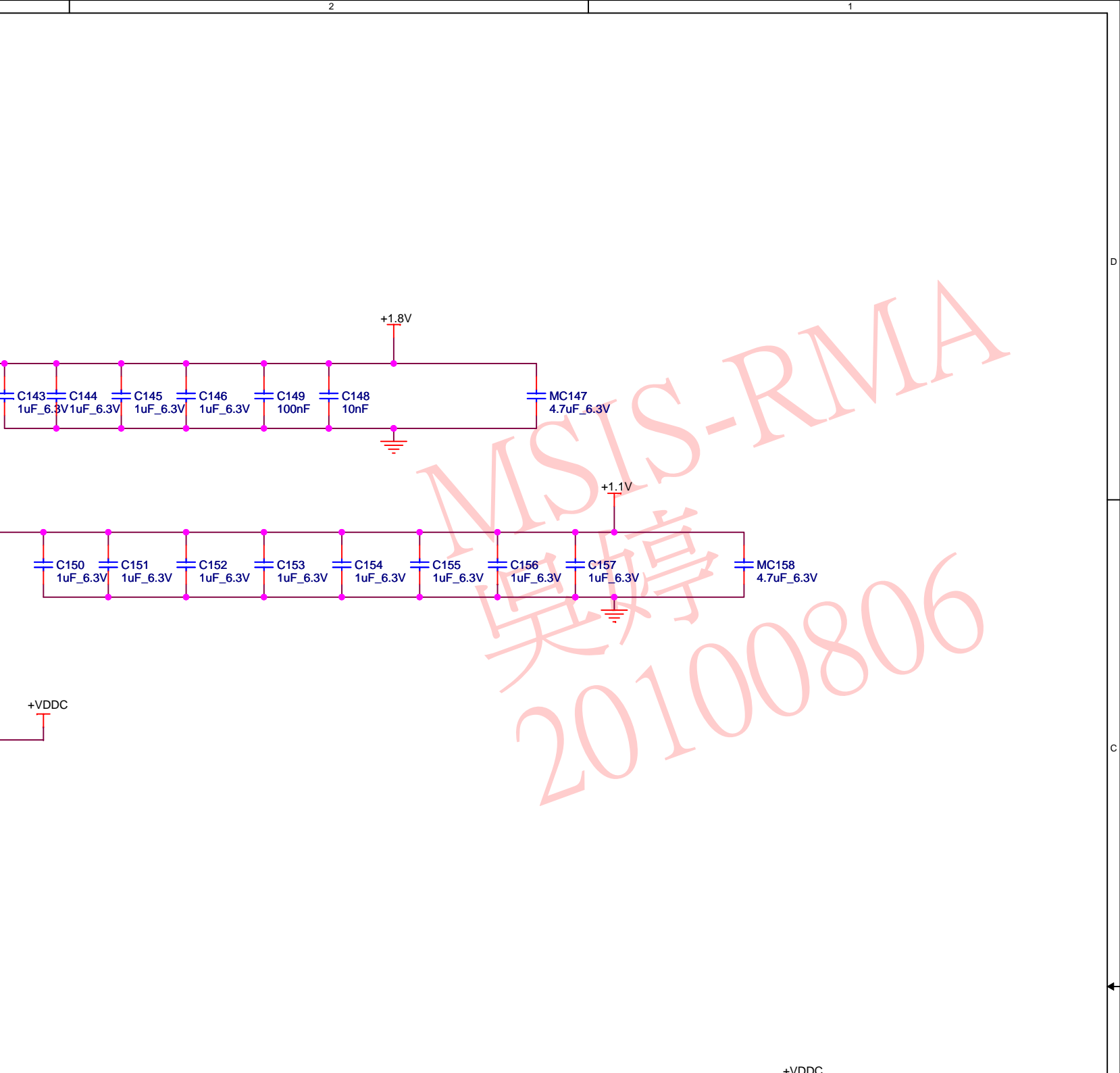
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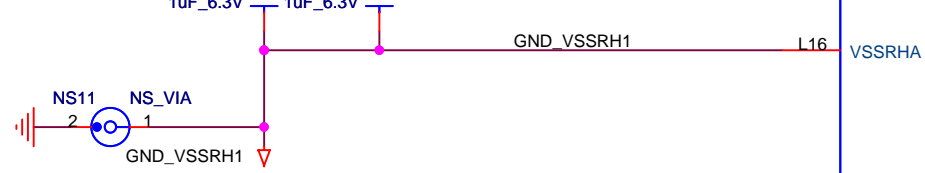
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	Title RH LP RV710 DDR2 VGA (header) TVO DVI		Doc No. 105-B750XX-00A	





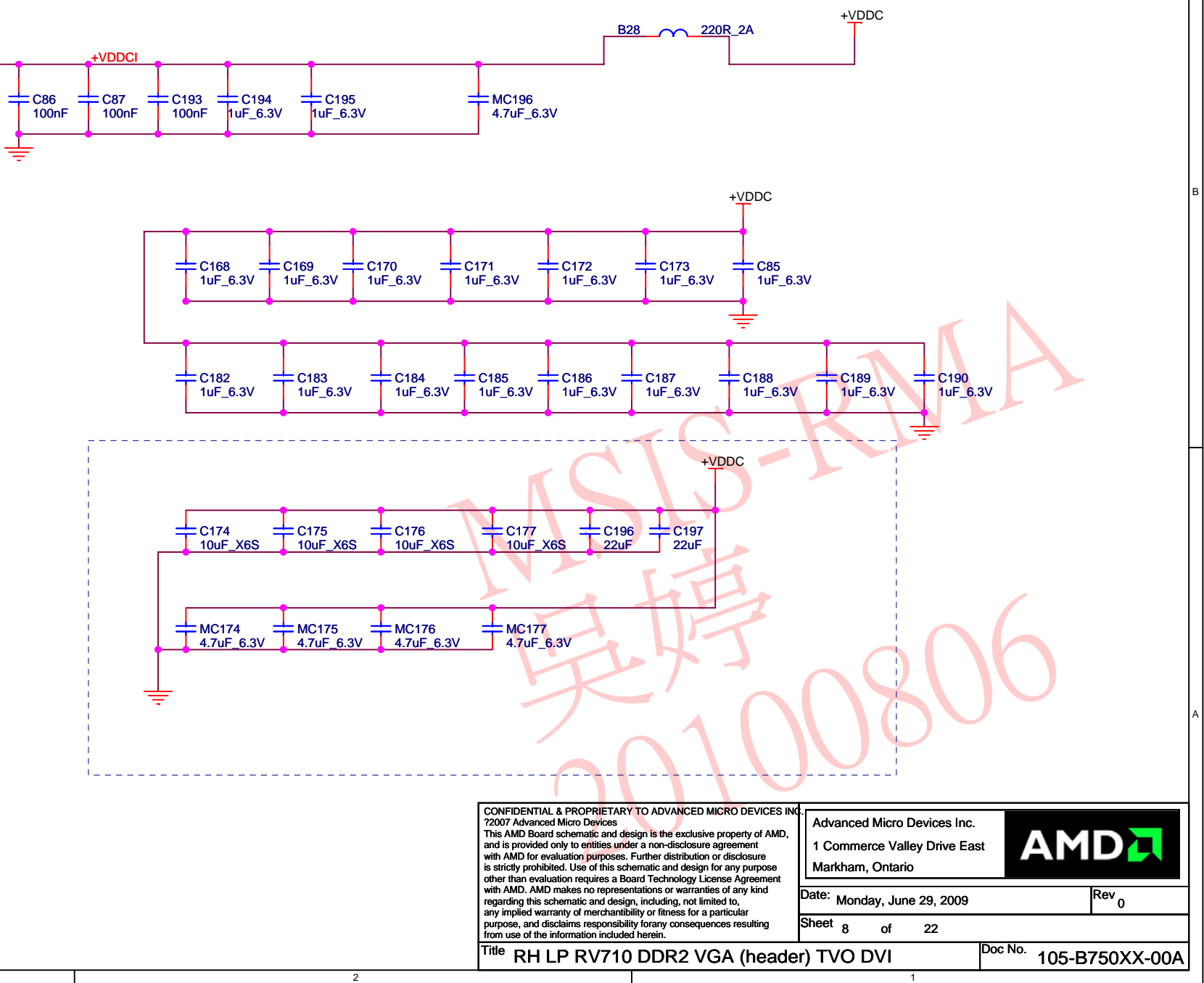


VDDCI#1
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VDDCI#3
VDDCI#4
VDDCI#5
VDDCI#6
VDDCI#7
VDDCI#8

M13
M15
M16
M17
M18
M20
M21
N20

RV710_03_20_FINAL1

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U1E

PART 5 OF 10

GND

AA27
AB24
AB32
AC24
AC26
AC27
AD25
AD32
AE27
AE32
AG27
AH32
K28
K32
L27
M32
N25
N27
P25
P32
R27
T25
T32
U25
U27
V32
W25
W26
W27
Y25
Y32

PCIE_VSS#1
PCIE_VSS#2
PCIE_VSS#3
PCIE_VSS#4
PCIE_VSS#5
PCIE_VSS#6
PCIE_VSS#7
PCIE_VSS#8
PCIE_VSS#9
PCIE_VSS#10
PCIE_VSS#11
PCIE_VSS#12
PCIE_VSS#13
PCIE_VSS#14
PCIE_VSS#15
PCIE_VSS#16
PCIE_VSS#17
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PCIE_VSS#31

GND#33
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GND#77
GND#78
GND#79
GND#80
GND#81
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GND#83
GND#84
GND#85
GND#86
GND#87
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GND#89

F18
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F20
F22
F24
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F6
F8
G10
G27
G31
G8
H14
H17
H2
H20
H6
J27
J31
K11
K2
K22
K6
M6
N11
N12
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N16
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P6
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R12
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U3
U9
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Y17
Y20
Y6
T11
R11

A3
A30
AA13
AA16
AB10
AB15
AB6
AC9
AD6
AD8
AE7
AG12
AH10
AH28
B10
B12
B14
B16
B18
B20
B22
B24
B26
B6
B8
C1
C32
E28
F10
F12
F14
F16

GND#1
GND#2
GND#3
GND#4
GND#5
GND#6
GND#7
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GND#20
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GND#22
GND#23
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GND#25
GND#26
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GND#28
GND#29
GND#30
GND#31
GND#32

VSS_MECH#1
VSS_MECH#2
VSS_MECH#3

A32
AM1
AM32

RV710_03_20_FINAL1

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Title RH LP RV710 DDR2 VOLTAGE REGULATOR


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	VGA (header) TVO DVI			Doc No. 105-B750XX-00A

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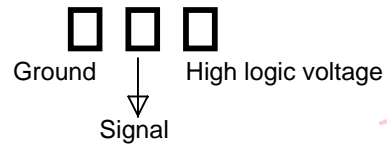
PIN BASED STRAPS

Pull-Down Resistors are for BU until built-in pull-downs are verified.



Overlap pads to save space and to prevent assembly of both resistors.

Layout



PIN BASED STRAPS

VIP_DEVICE_STRAP_EN
0: Driver would ignore the value sampled at
1: Driver would use the value sampled at t
whether or not a VIP slave device (e.g. Th
(i.e. 0 indicates yes, 1 indicates no).

VGA DISABLE : 1 for disable (set to 0 for



	1
ed on VHAD_0 during reset at reset from VHAD_0 to determine . Theater chip) is connected	
for normal operation)	D
er Power Savings Enable) le for Desktop)	
ter De-emphasis Enable) mode tting for Desktop)	
nable)	
5P05A (ST) 5P10A (ST) 5P20 (ST) 5P40 (ST) 5P80 (ST) 25LV512 (Chingis) 25LV010 (Chingis)	C
nent capability nent capability	
logic must not affect this signal	B
1 - NTSC TVO	

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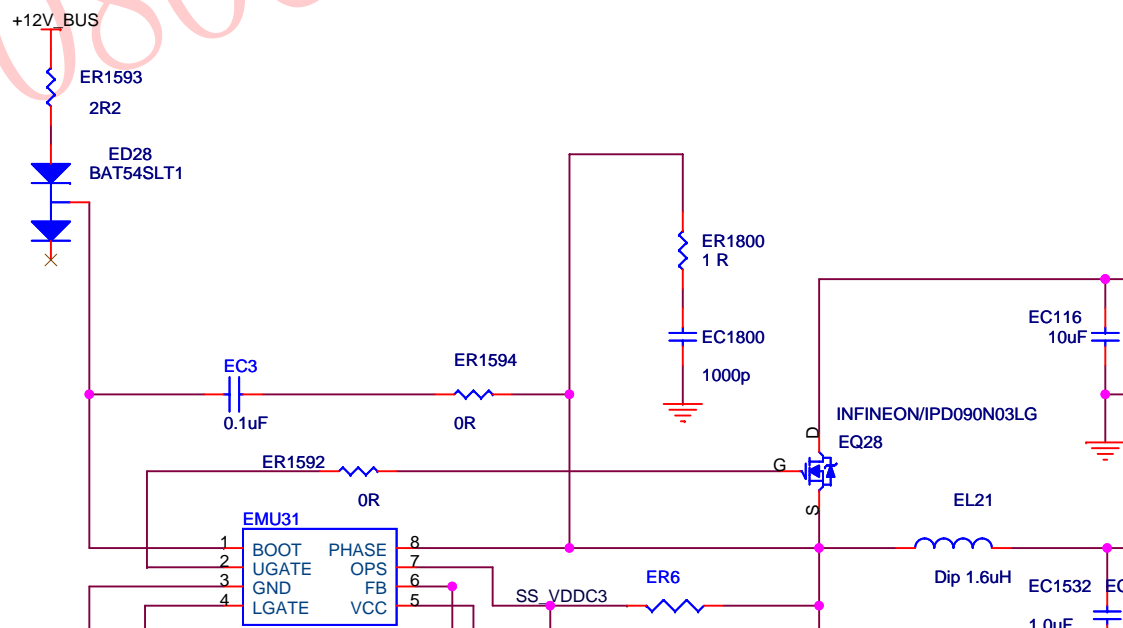
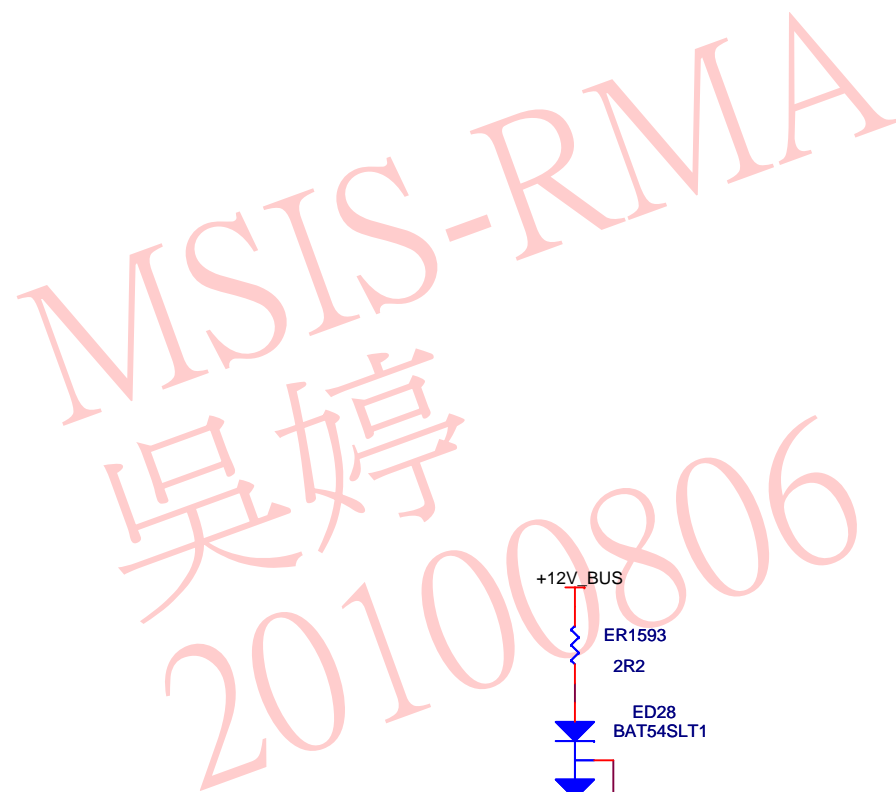
3

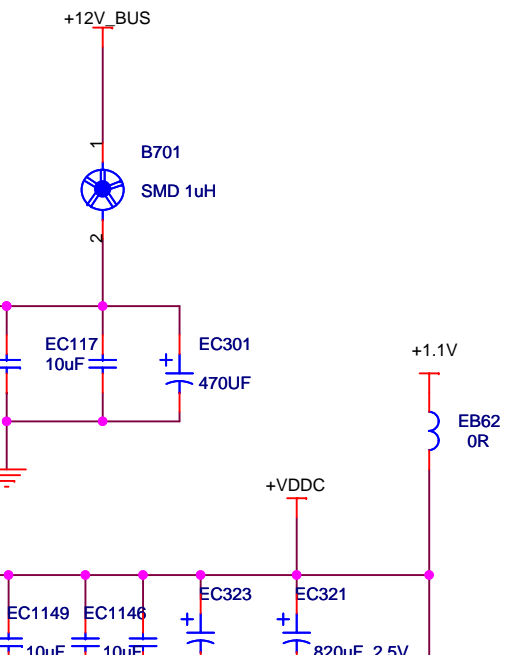
2

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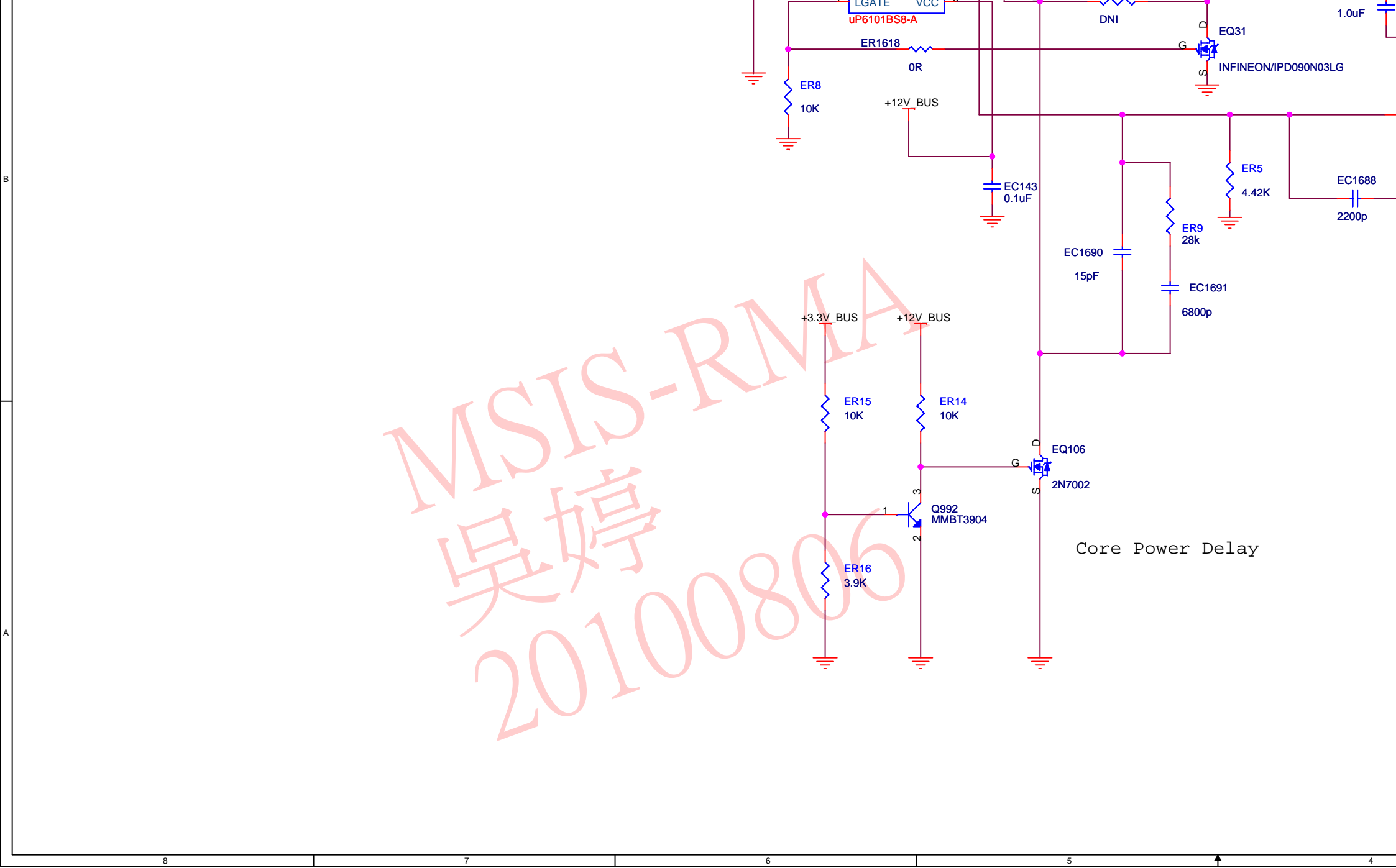


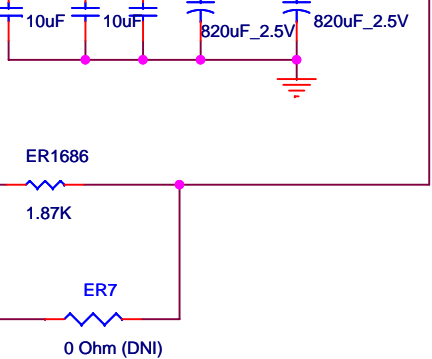


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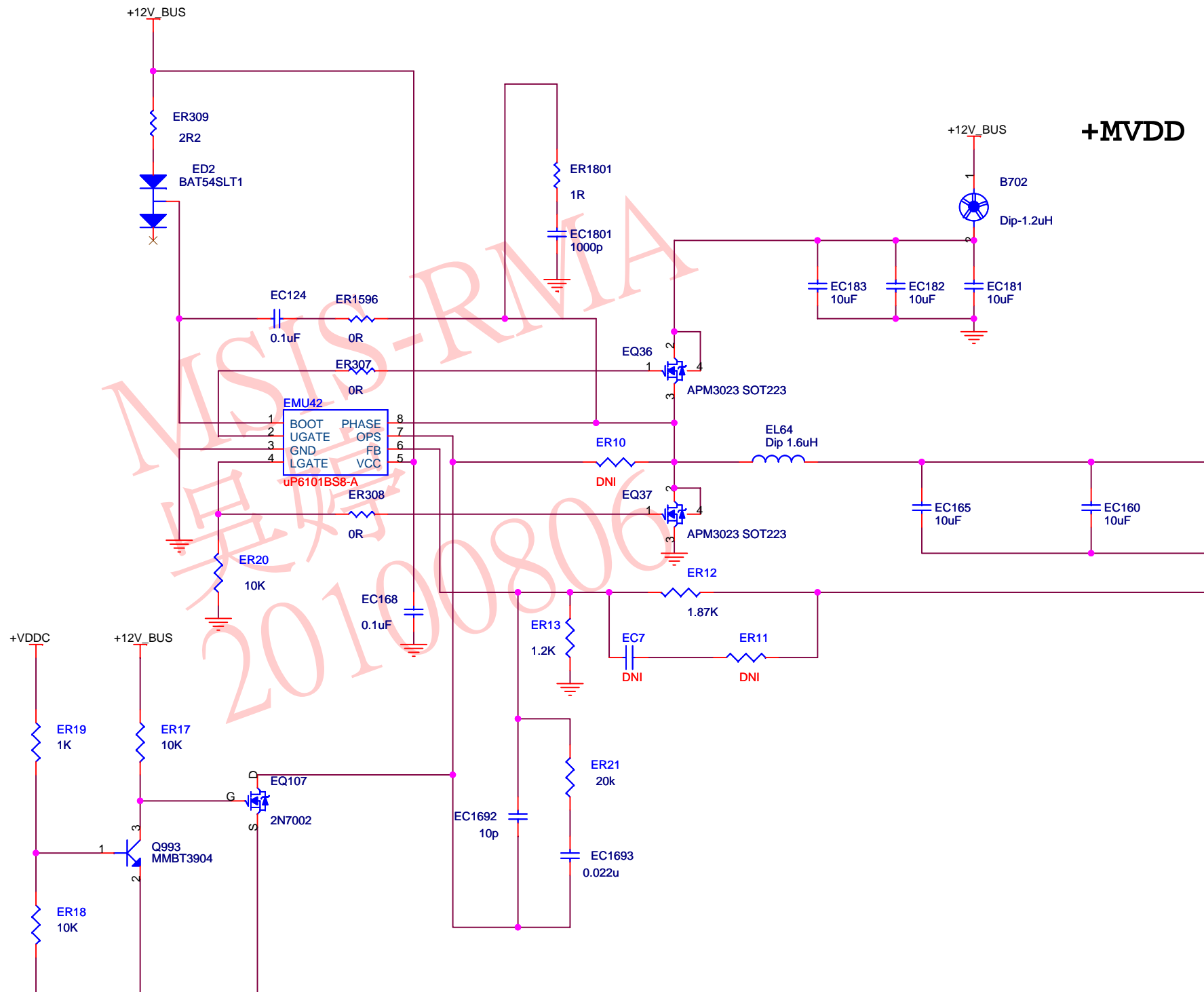
3

2

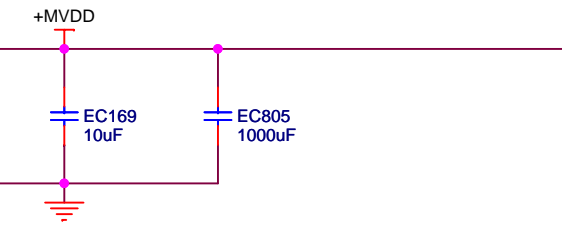
1

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$$= 0.8 * (1 + (ER12 / ER13))$$

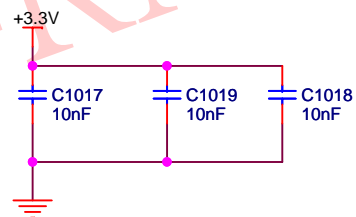
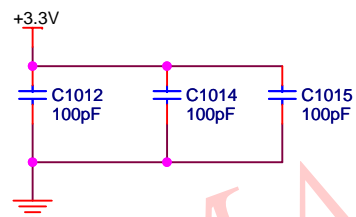
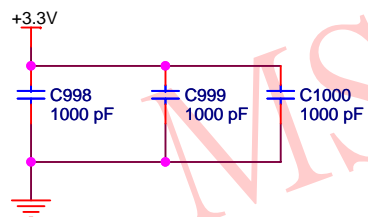
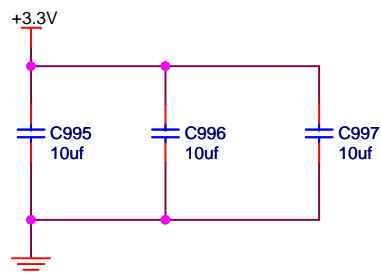
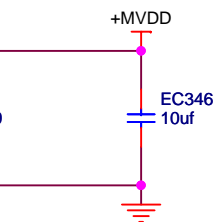


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Title RH LP RV710 DDR2 VGA (header) TVO DVI

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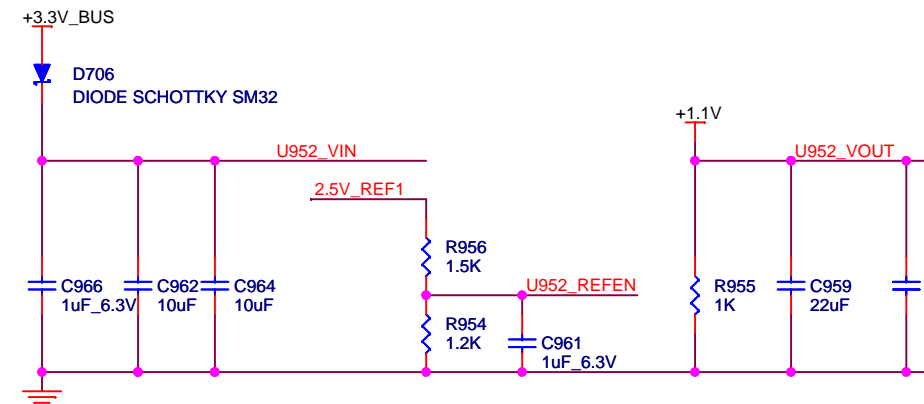
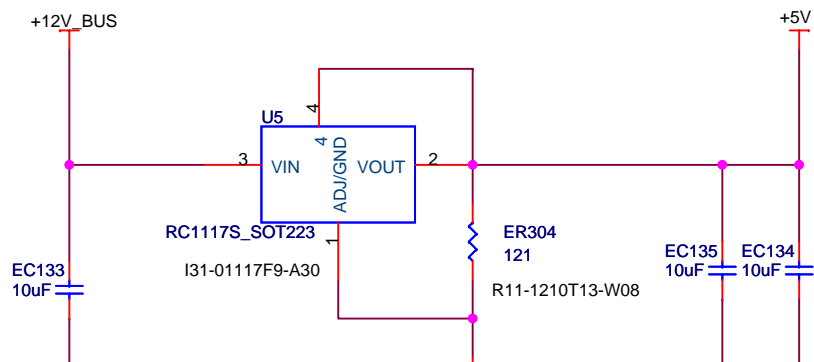
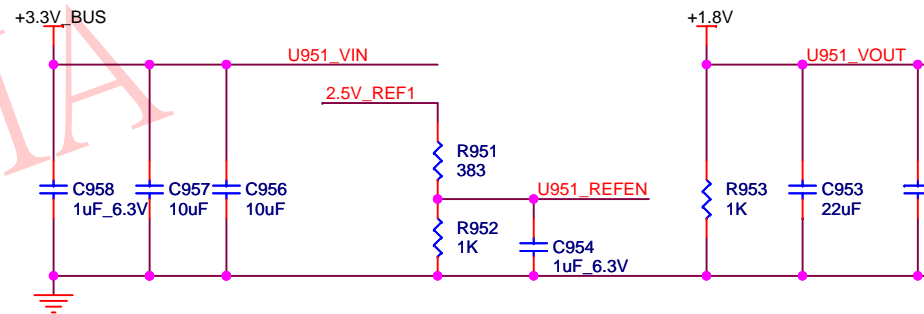
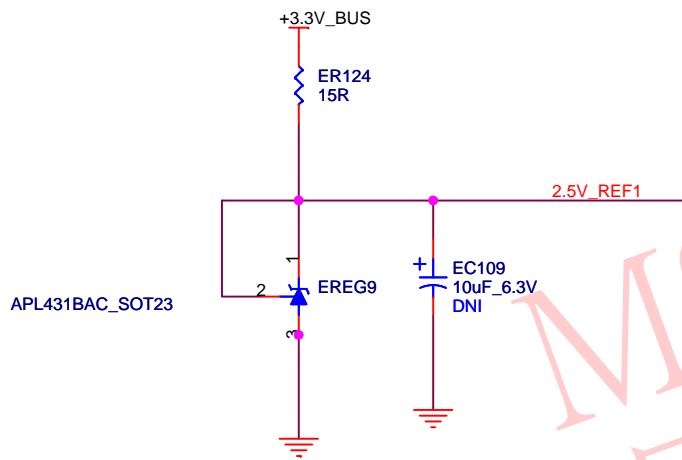
3

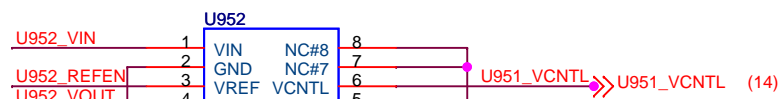
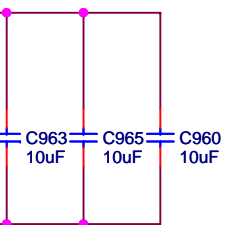
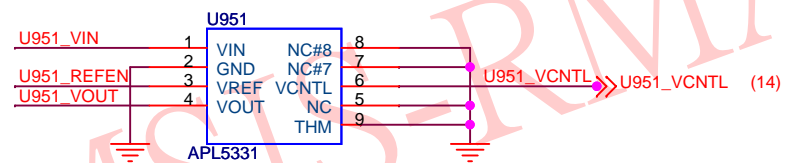
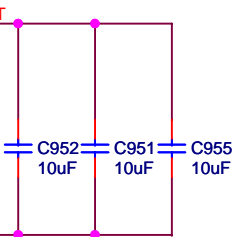
2

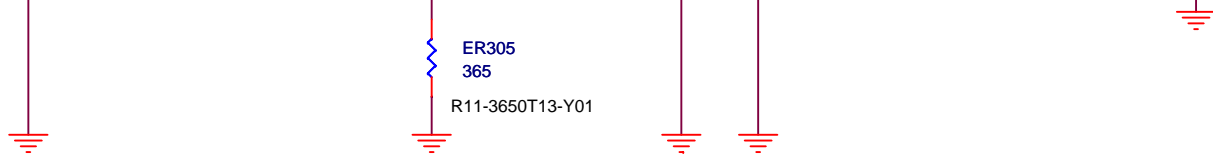
1

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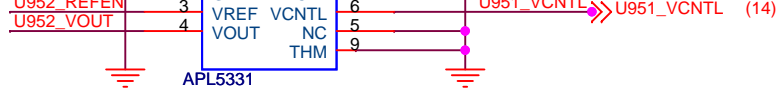







$$V_{out}=1.25V* [1+(ER305/ER304)]$$

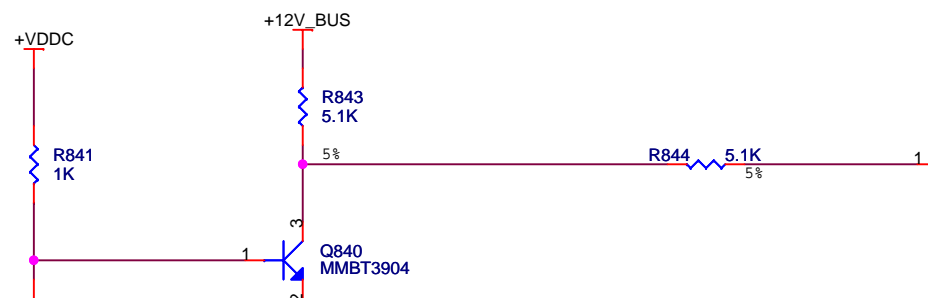
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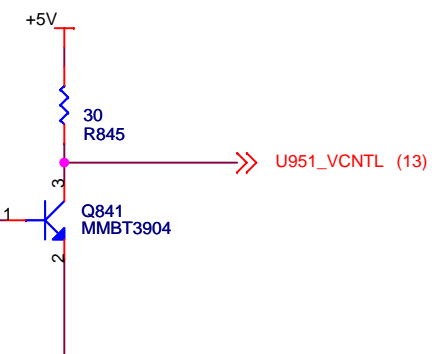


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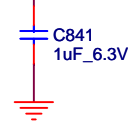




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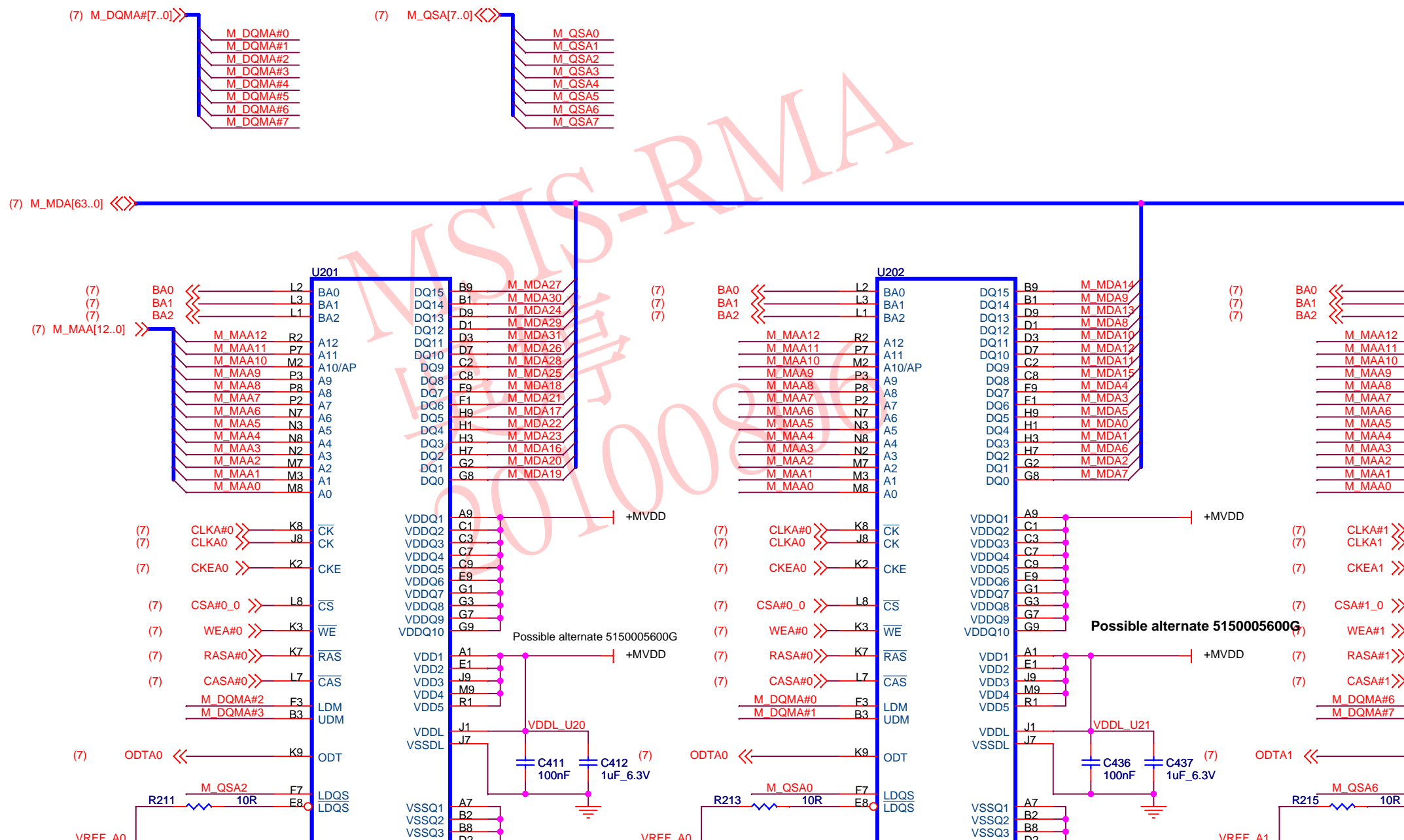
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2

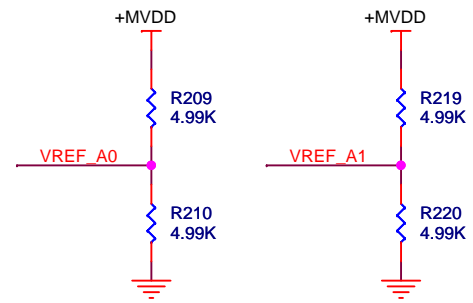
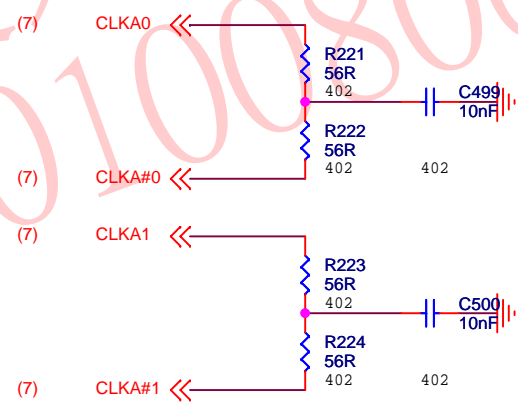
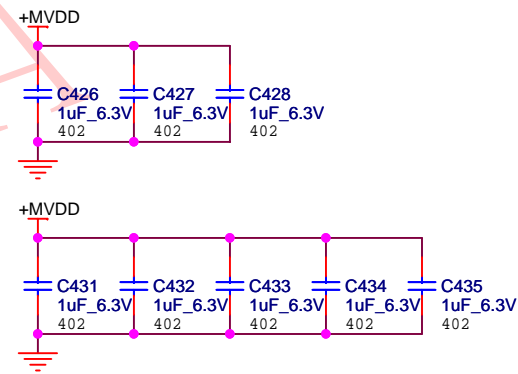
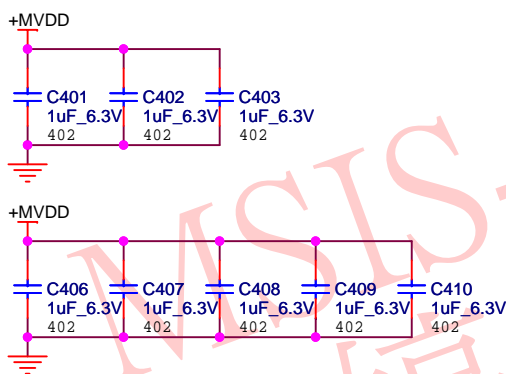
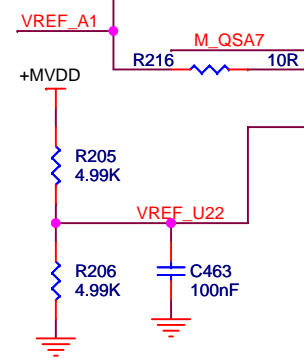
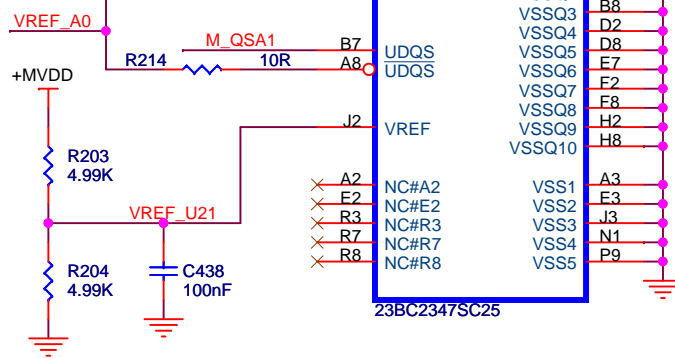
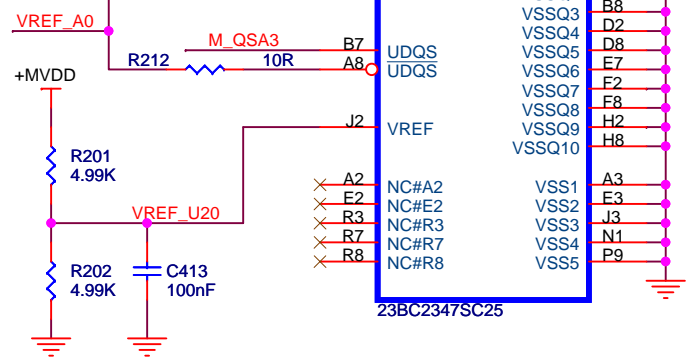
1

CHANNEL A: RANK 0 512MB DD

MAX DENSITY: 64Mx16







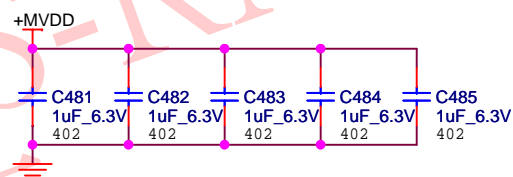
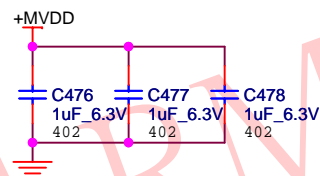
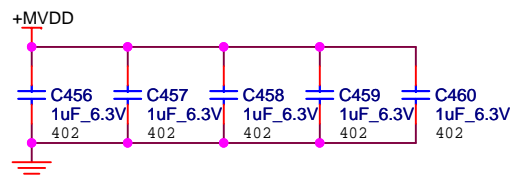
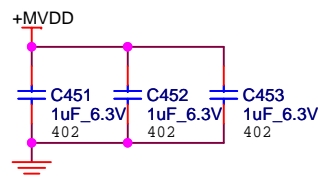
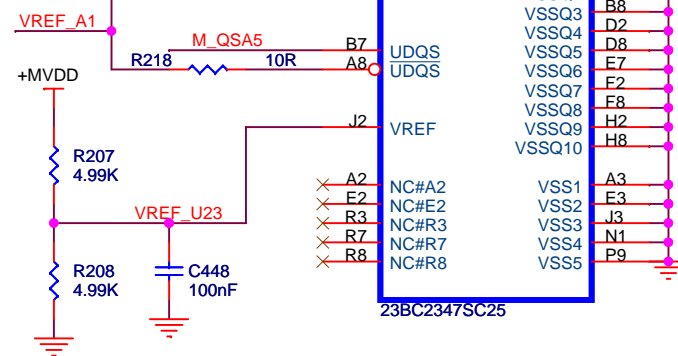
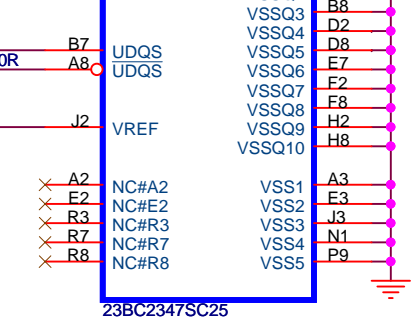
8


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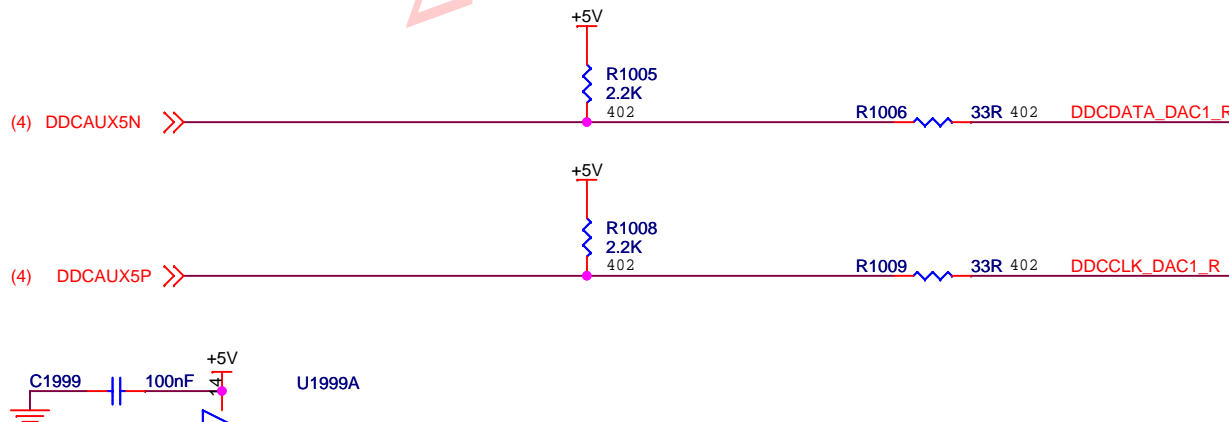
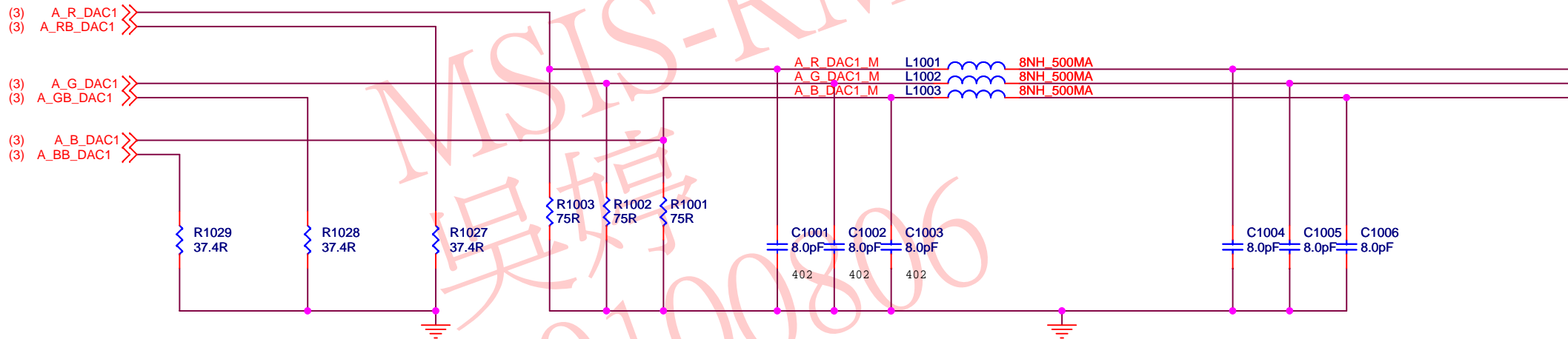
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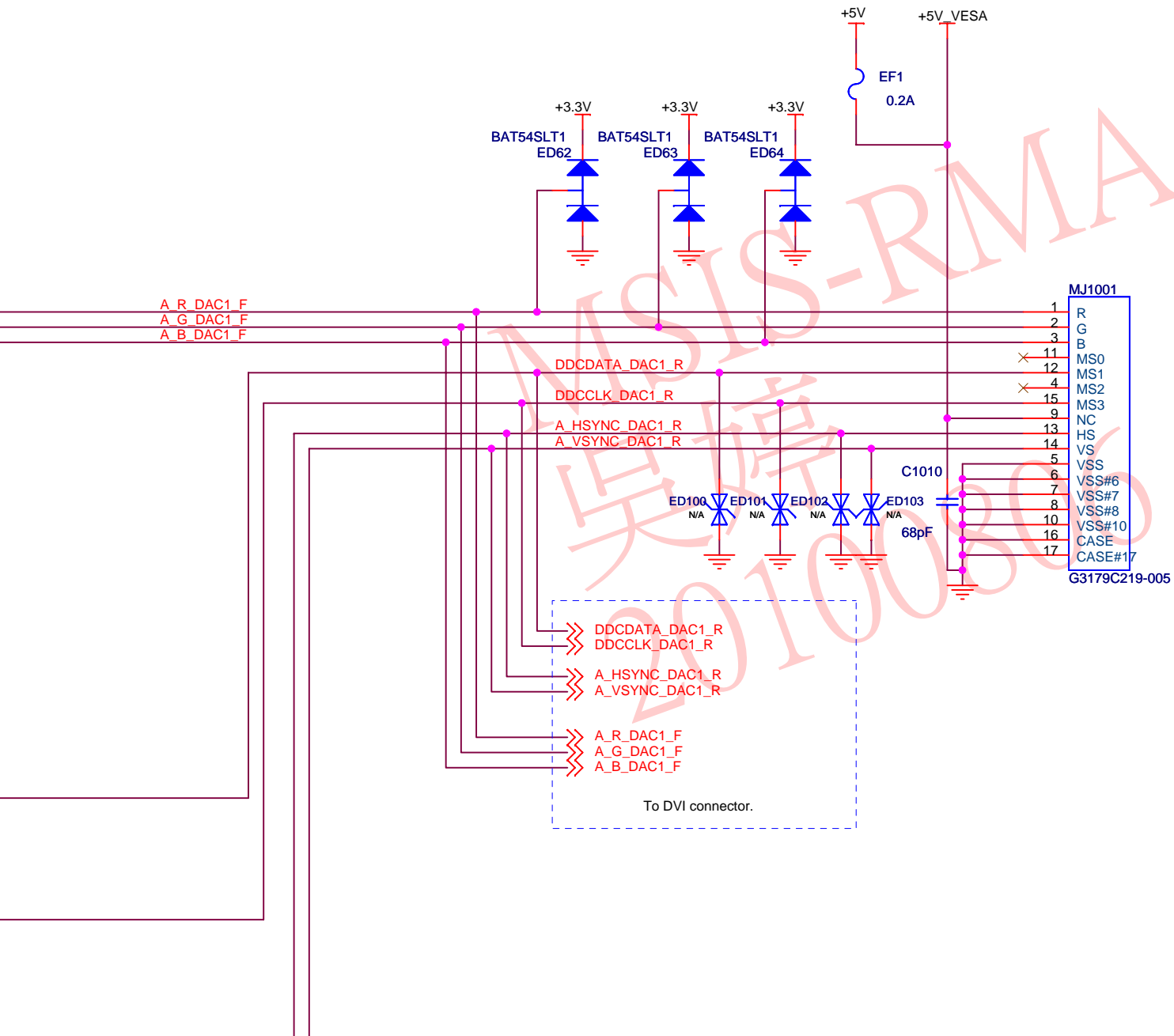
DAC 1 OUTPUT



Place close to Connector

Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)

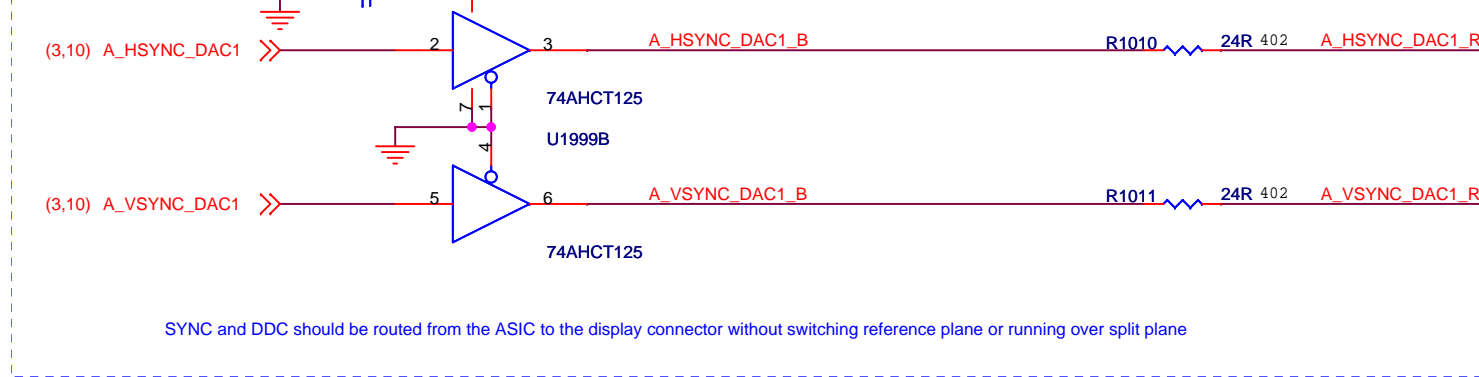




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(12,18) ALL_RAILS_UP



1



3

2



U1601

SI2304DS

+3.3V

3

Q1602
MMBT3904

1

HPD4_IN R1618

10K

(3)

HPD4



2

R1617
10K

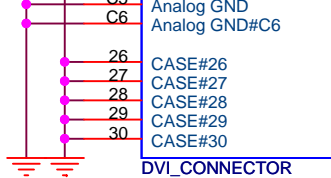


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Date: Monday, June 29, 2009

Rev 0

Sheet 16 of 22

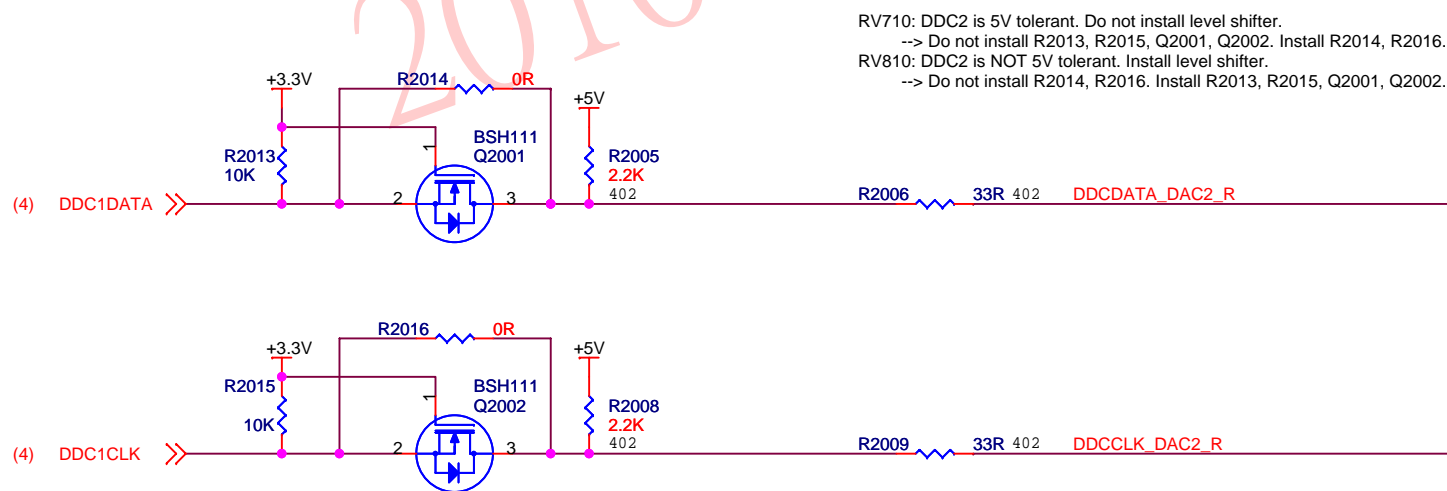
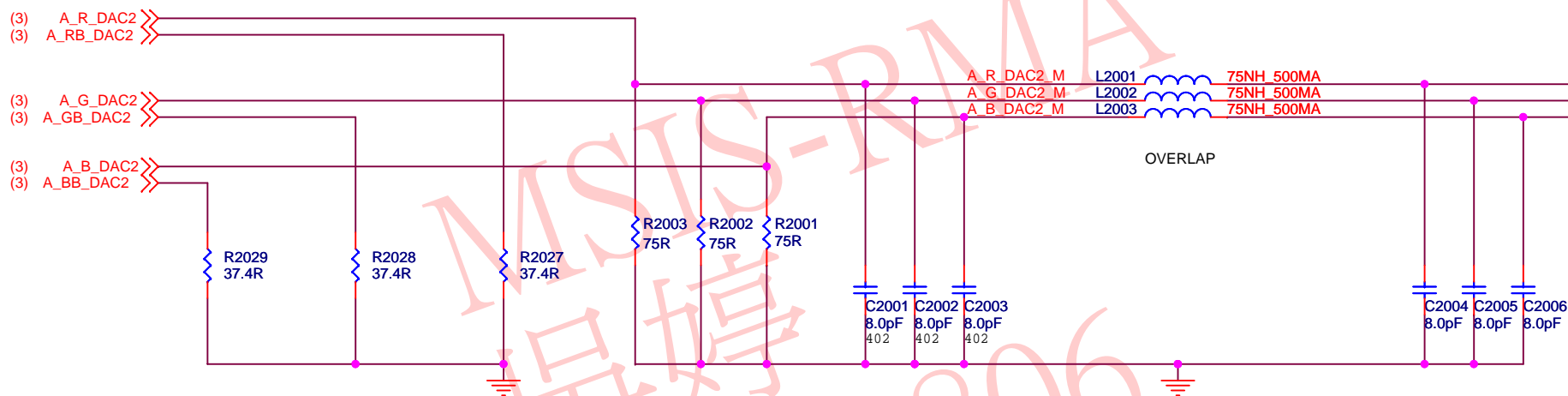
Title RH LP RV710 DDR2 VGA (header) TVO DVI

Doc No. 105-B750XX-00A

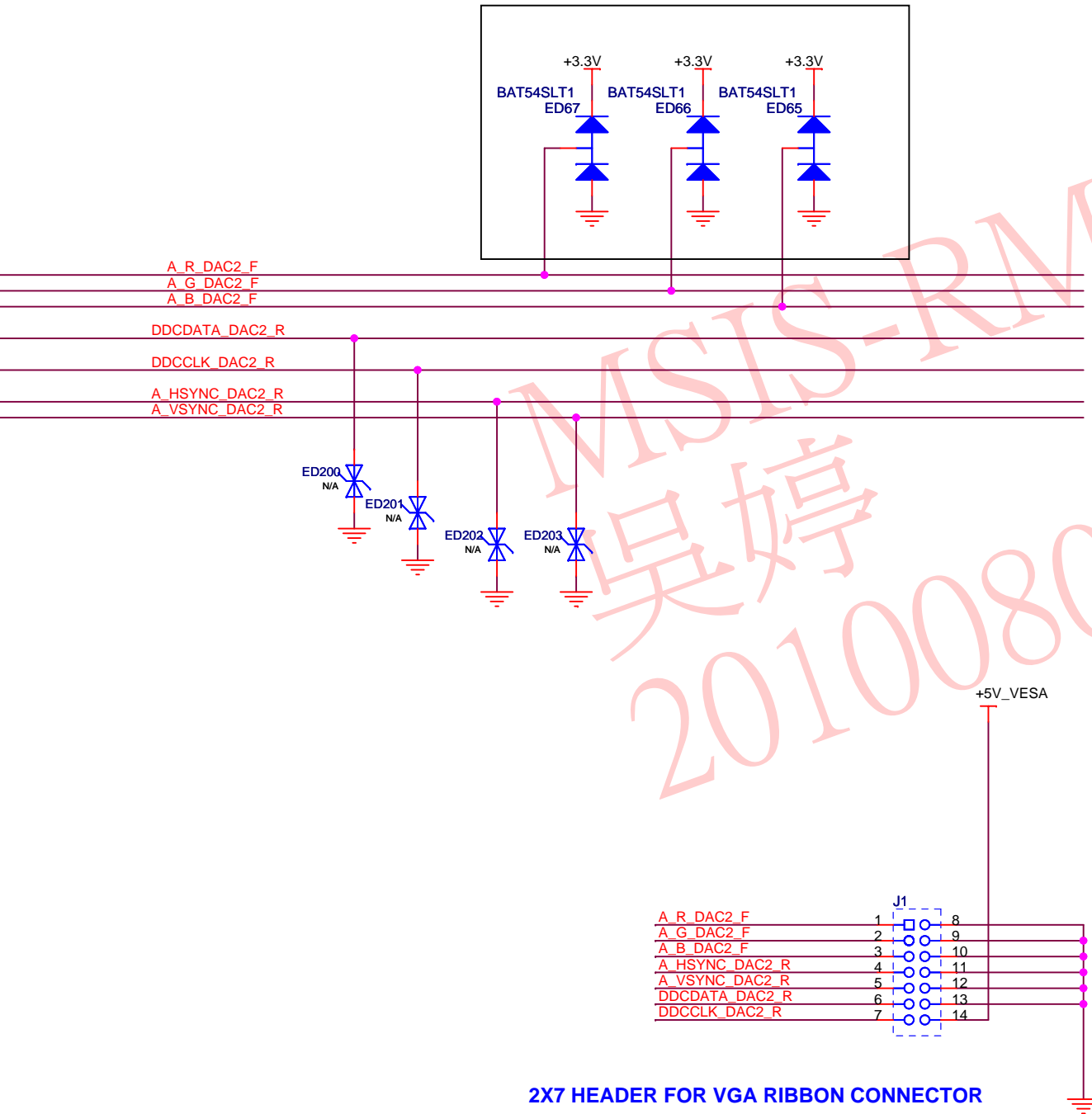
DAC 2 OUTPUT



Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane



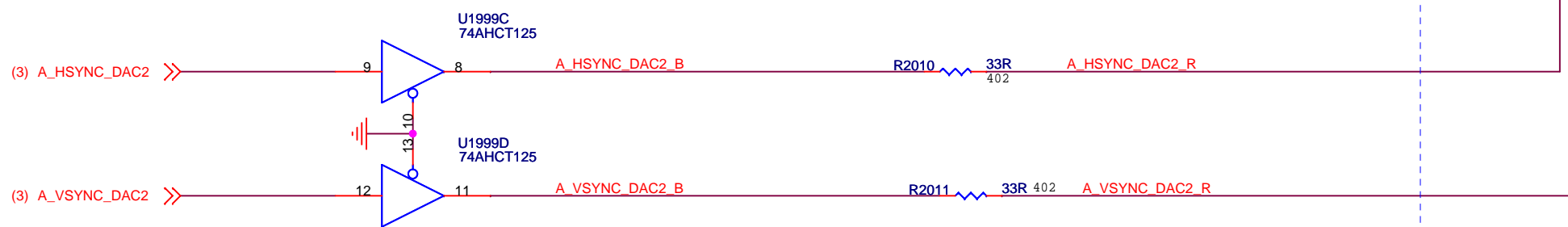
For ESD use



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SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

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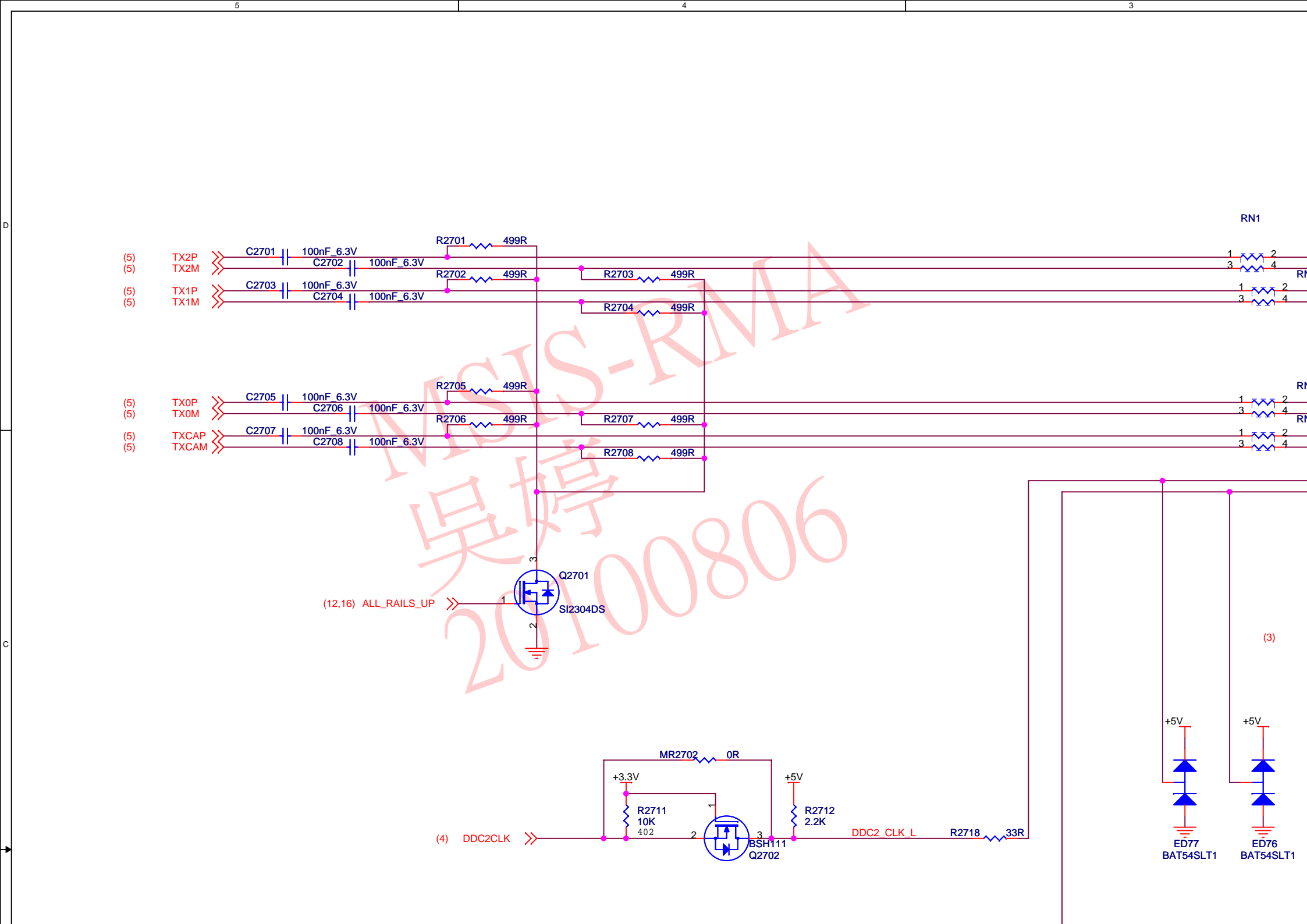
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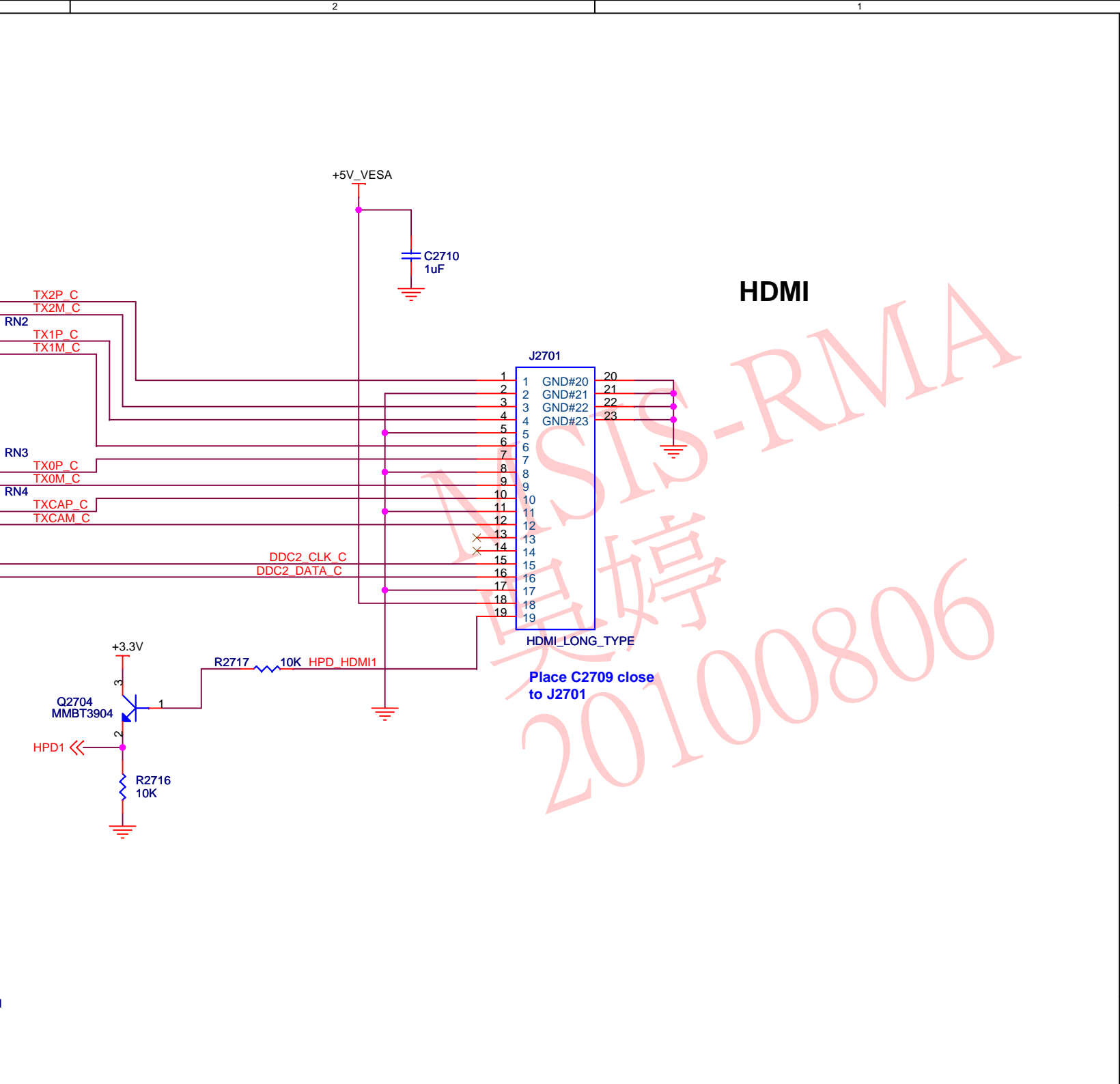
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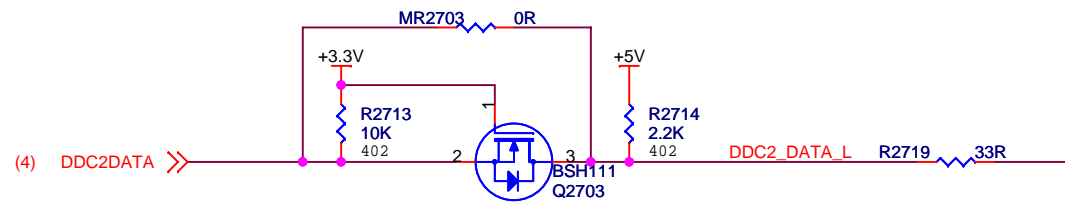


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Title RH LP RV710 DDR2 VGA (header) TVO DVI	Doc No. 105-B750XX-00A
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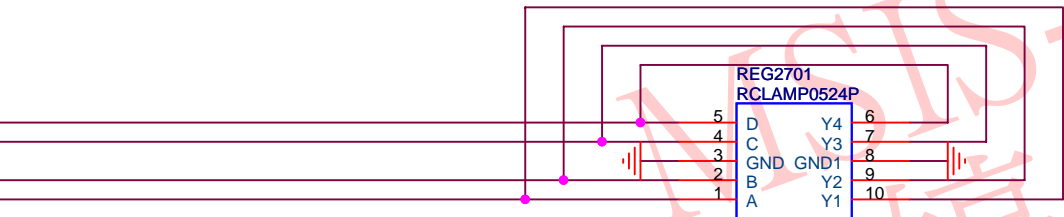
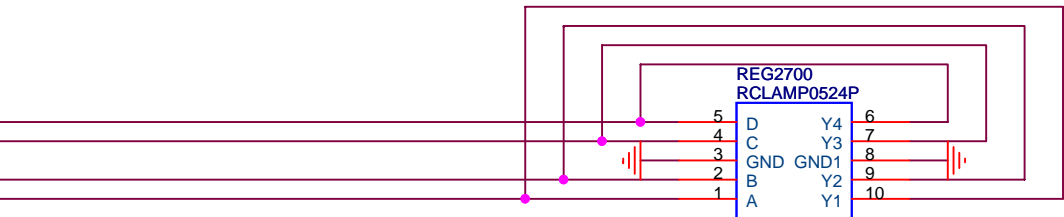



TX2P_C >>
TX2M_C >>
TX1P_C >>
TX1M_C >>

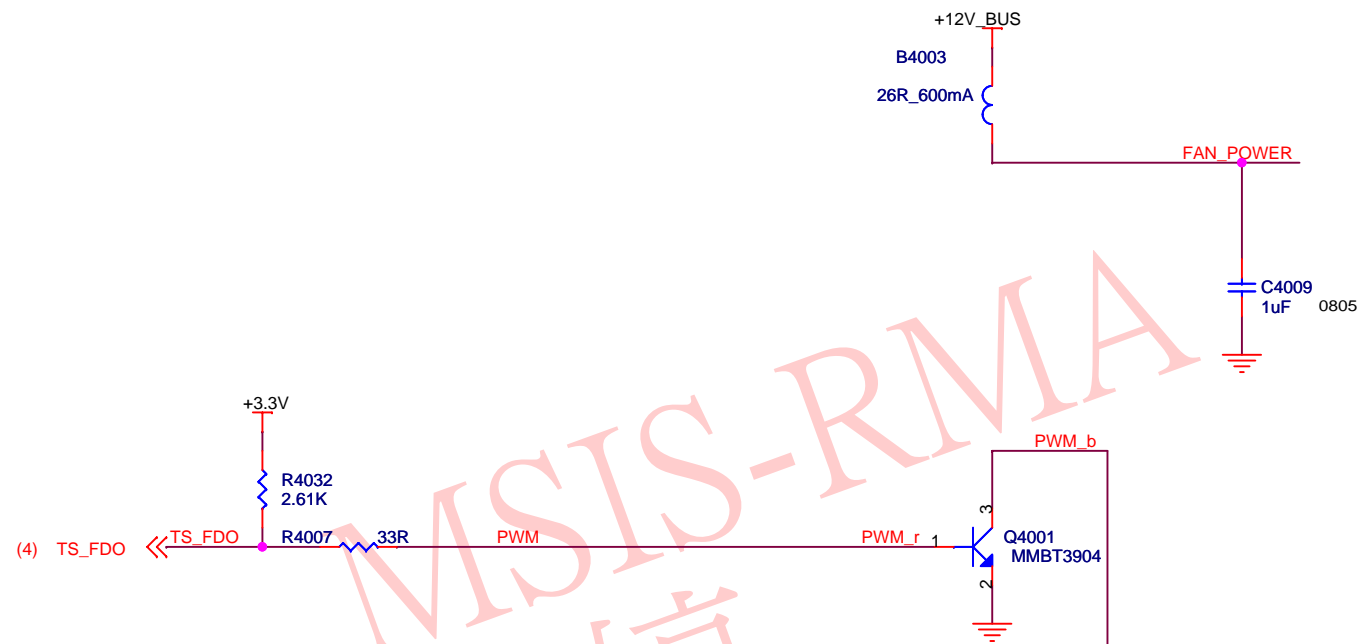
TX0P_C >>
TX0M_C >>
TXCAP_C >>
TXCAM_C >>

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Optional ESD protection diodes



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Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

Fan Control

R4010 0R

DNI

+12V

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D

C

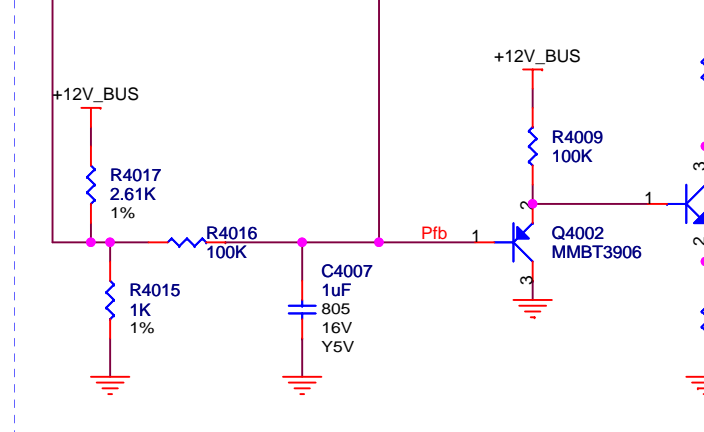
rol (Legacy)

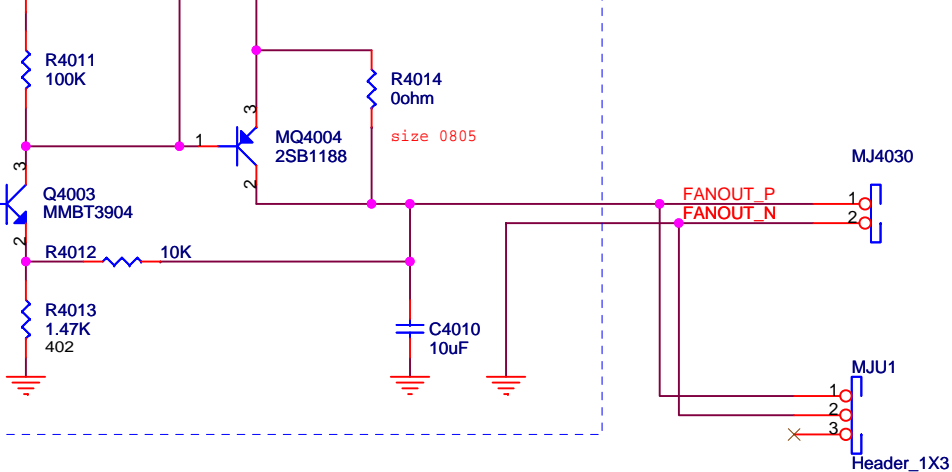
For 2-WIRE FAN ONLY

FAN_POWER


12V_BUS

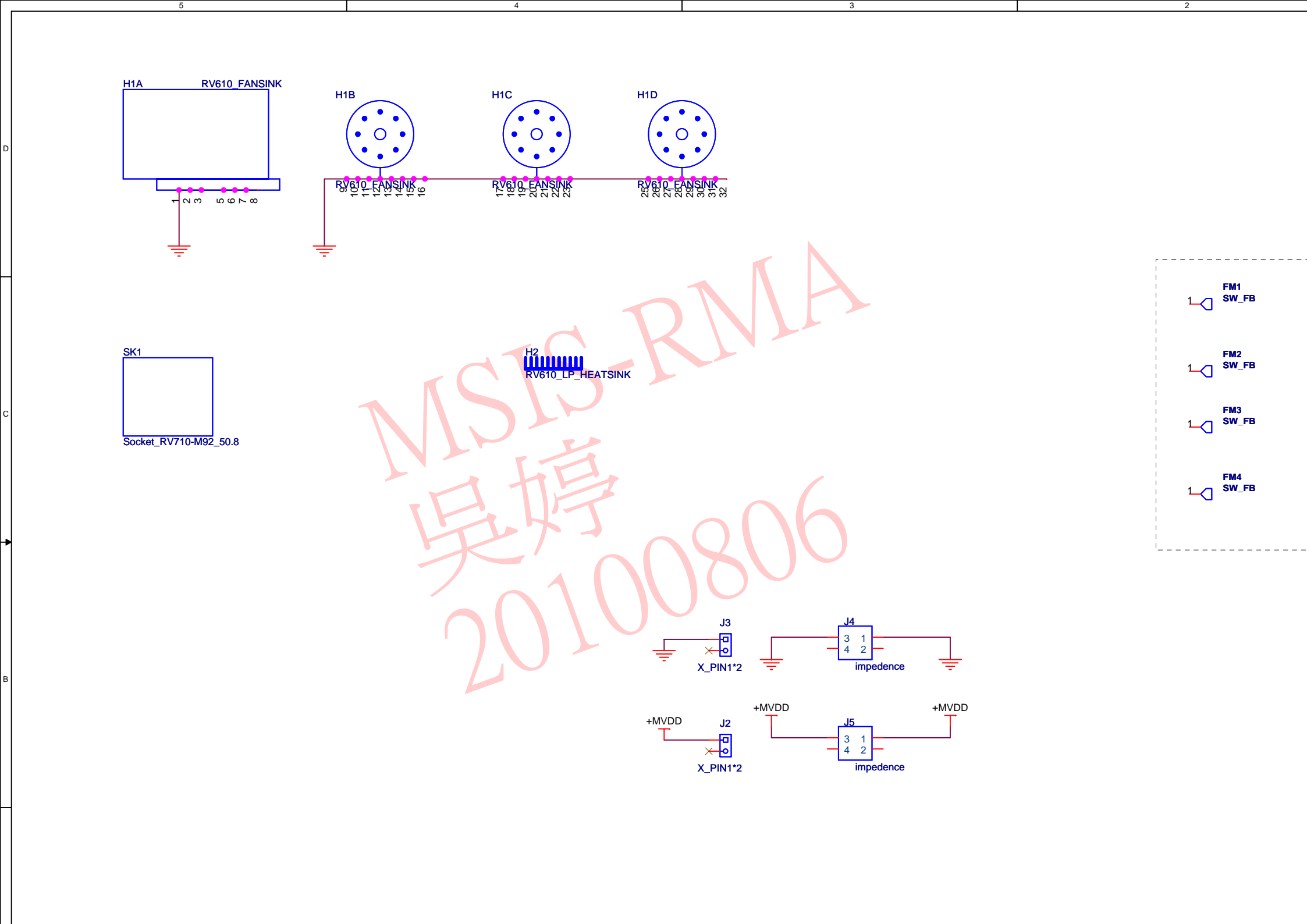
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Date: Monday, June 29, 2009				Rev 0	
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Title RH LP RV710 DDR2 VGA (header) TVO DVI				Doc No. 105-B750XX-00A	



D

C

B

FM5
SW_FB

FM6
SW_FB

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Title RH LP RV710 DDR2 VOLTAGE REGULATOR


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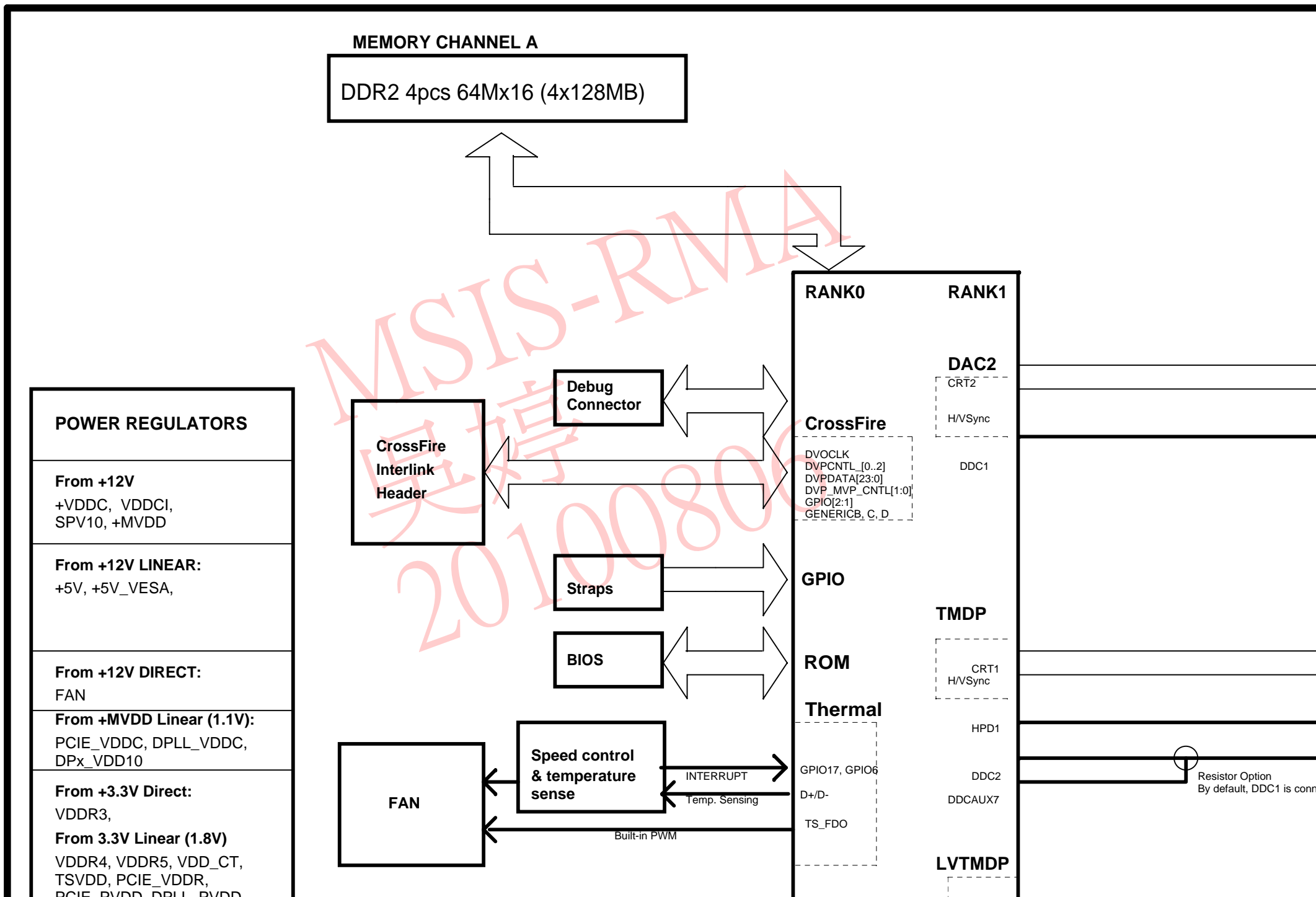
3

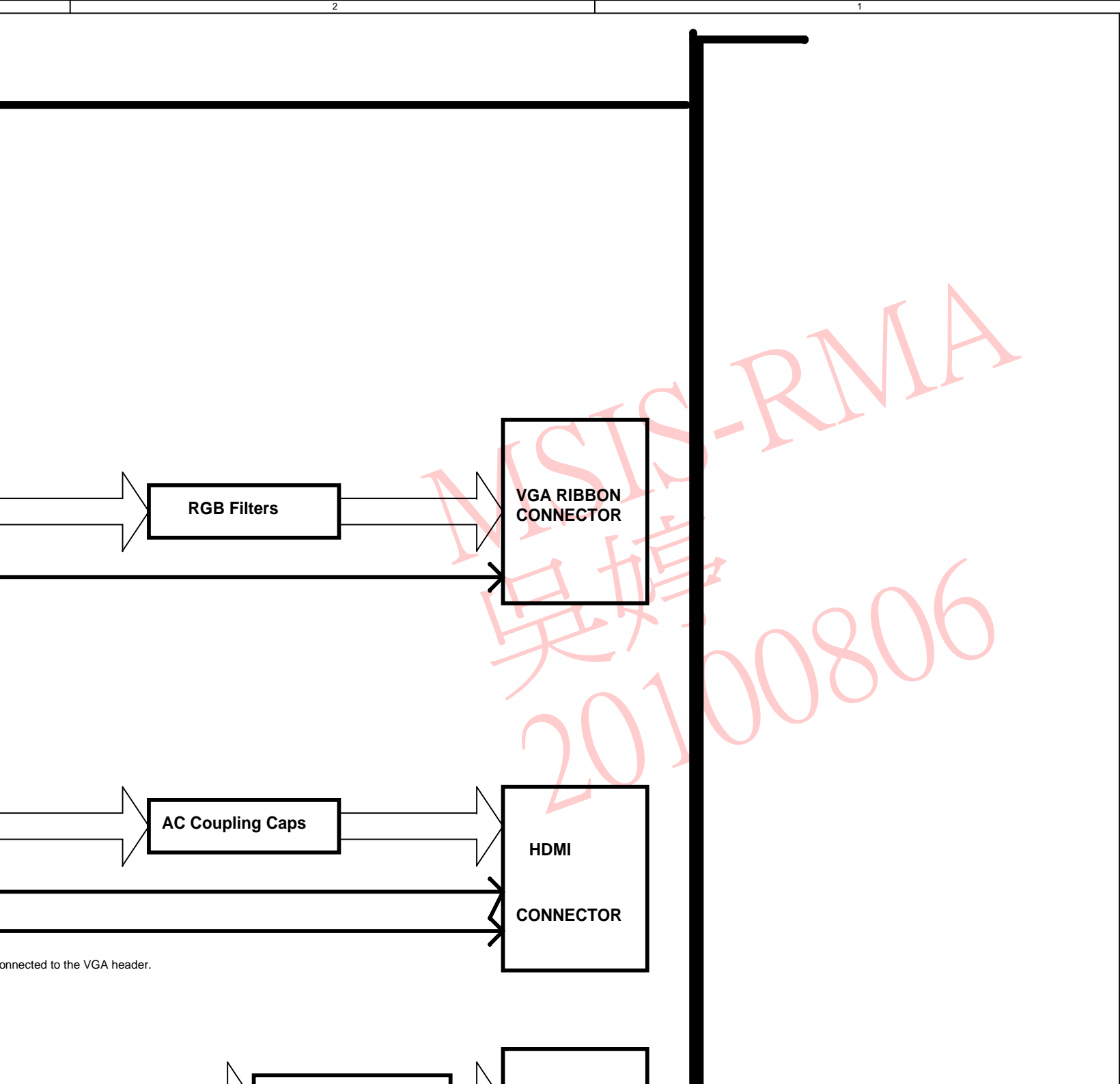
2

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Sheet 20 of 22			
VGA (header) TVO DVI		Doc No. 105-B750XX-00A	
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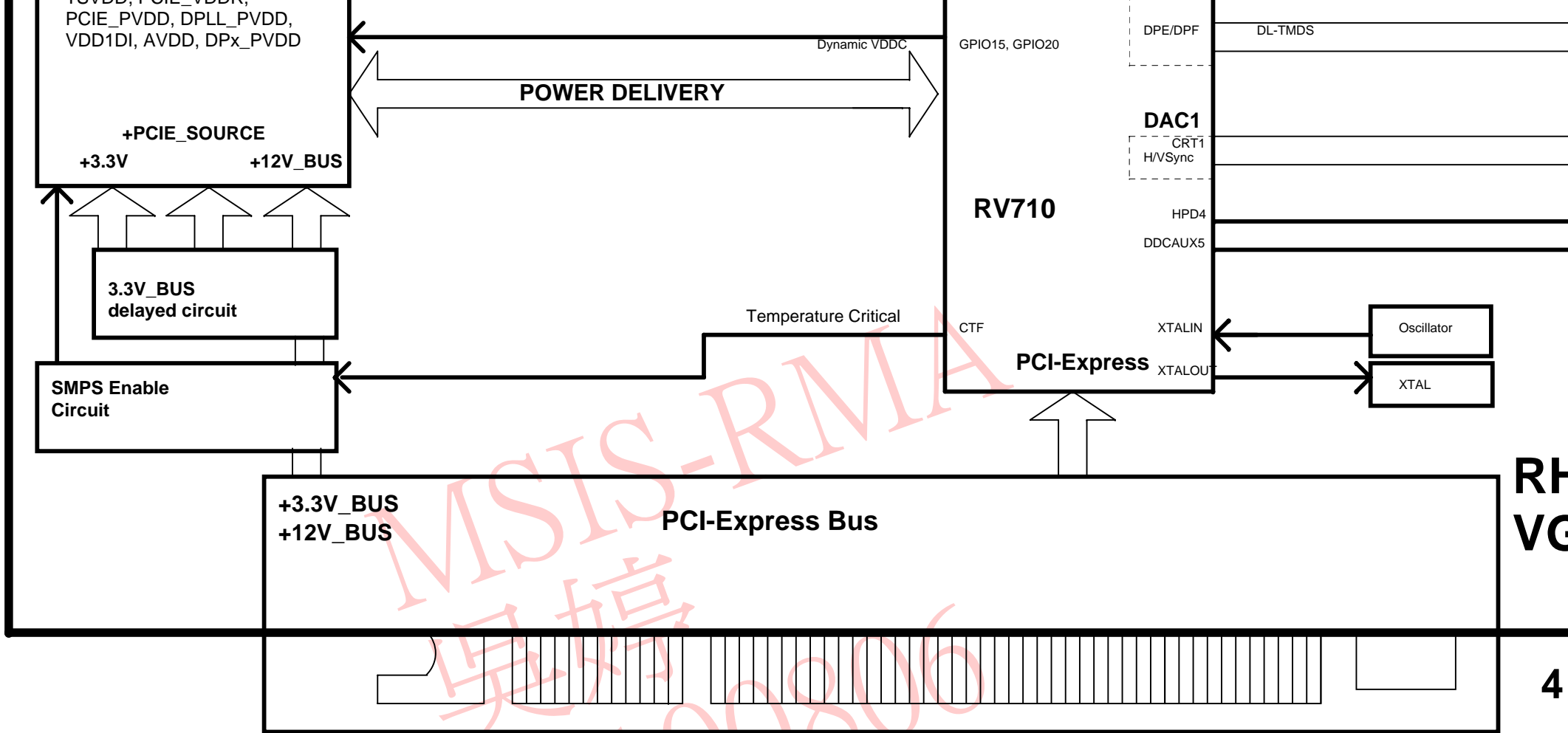


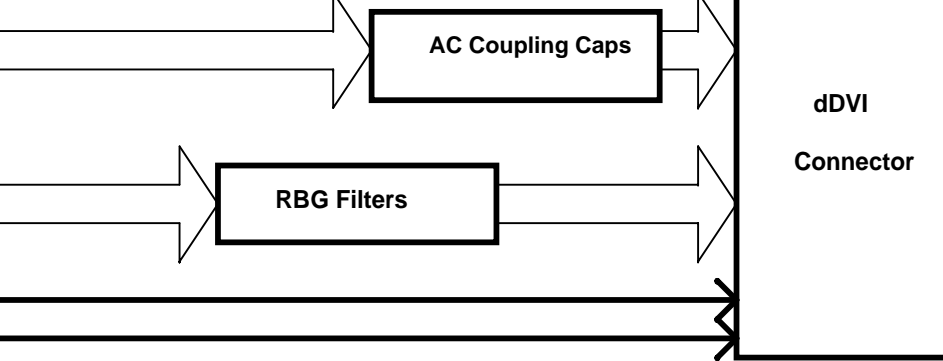


D

C

←






RH PCIE RV710 DDR3 VGA(header) + TVO + DVI

REV 1

4 Layer PCB

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	Title RH LP RV710 DDR3 VGA (header) TVO DVI		Doc No. 105-B750XX-00A	

			Title		Schematic No.		Date:			
			RH LP RV710 DDR2 VGA (header) TVO DVI		105-B750XX-00A		Monday, June 29, 2009			
			REVISION HISTORY					NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.		Rev 0
Sch Rev	PCB Rev	Date	RV710 ENGINEERING BOARD						REVISION DESCRIPTION	
01	00A	2008.04.02	INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.							
<div>MSIS-RMA 吳婷 20100806</div>										