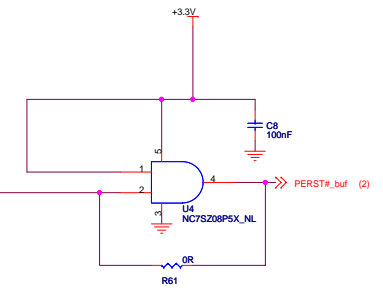
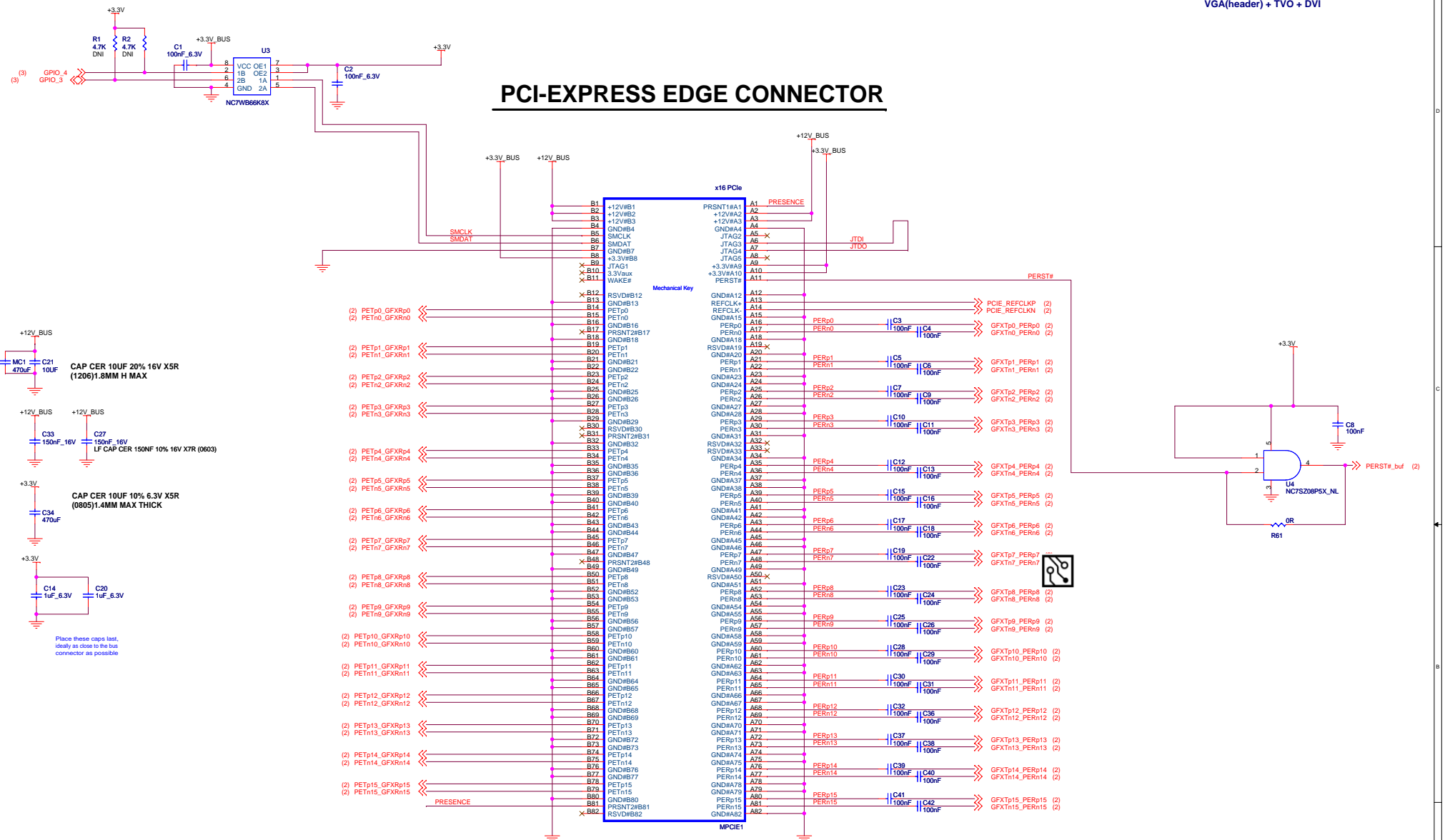
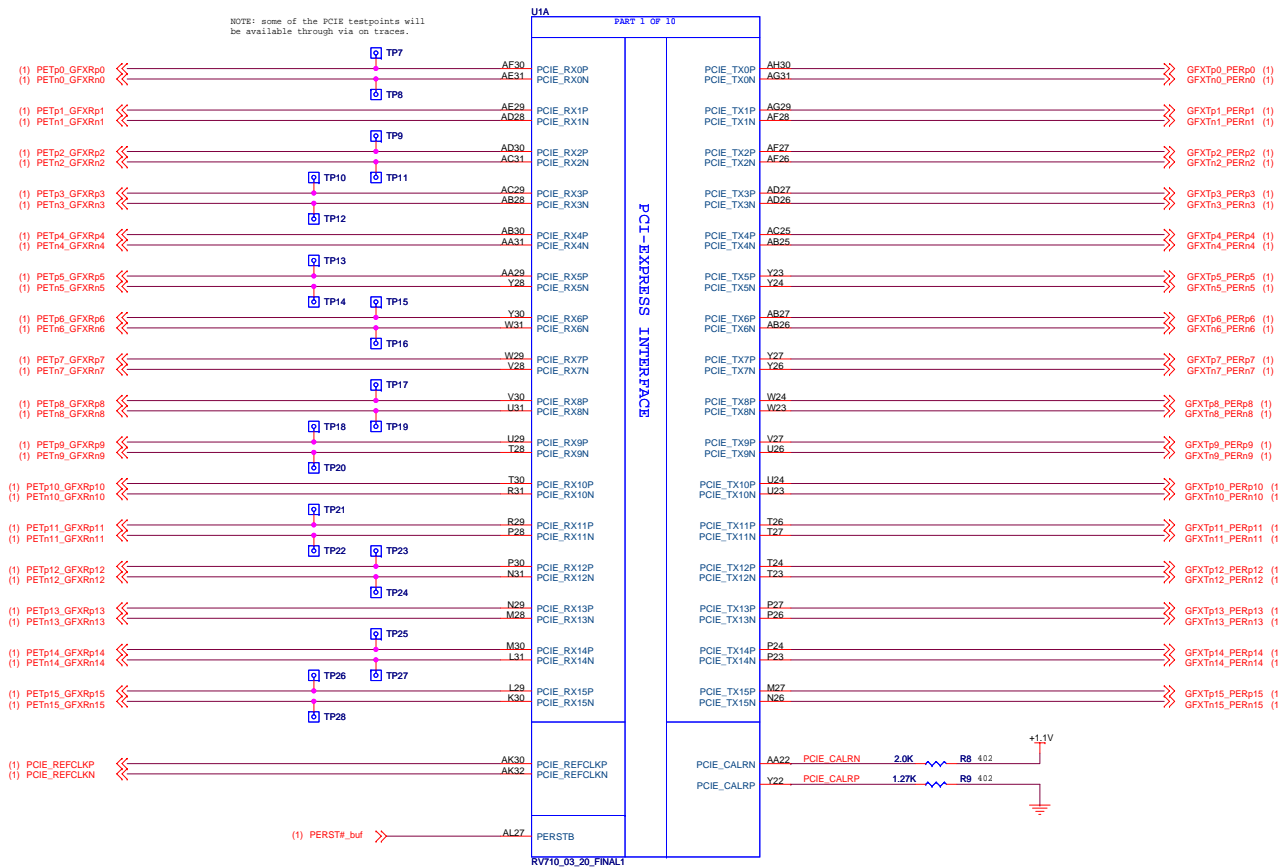


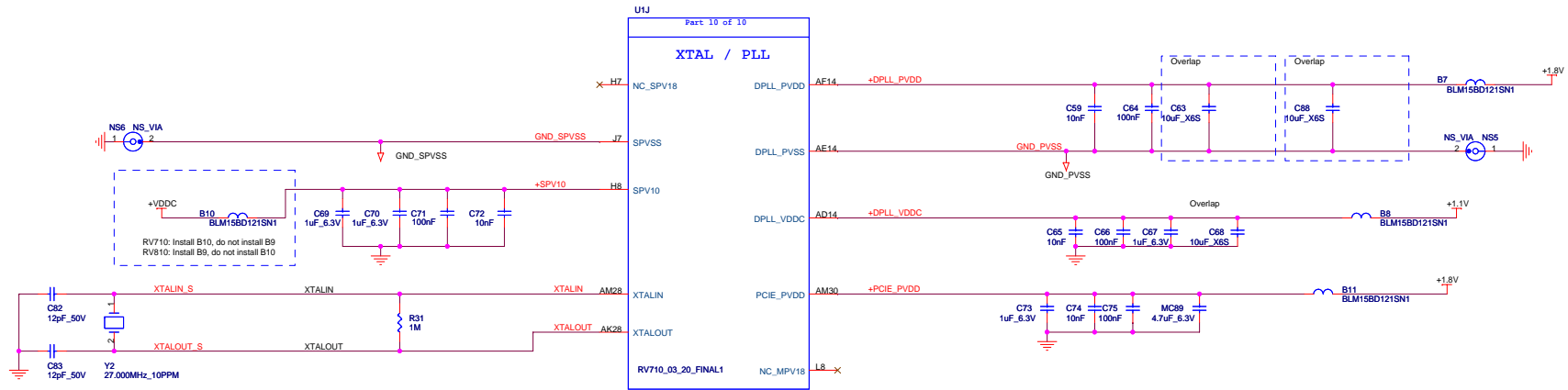
# PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND





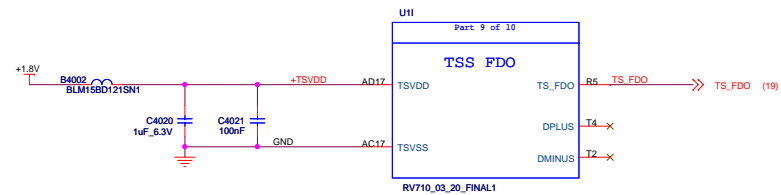
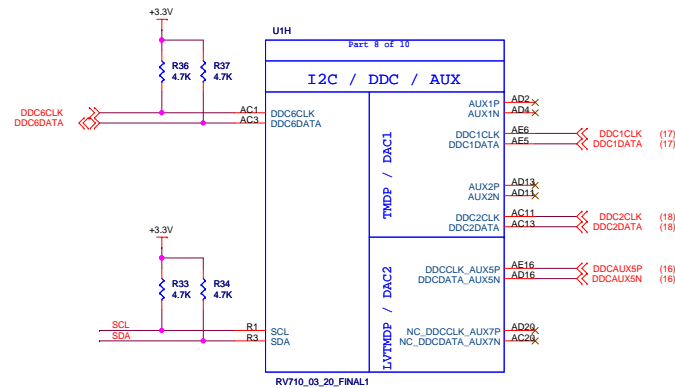


DDC6 BUS:

I2C Address	Function	Device
0x90	I2C VDDC Control	DS4402
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A

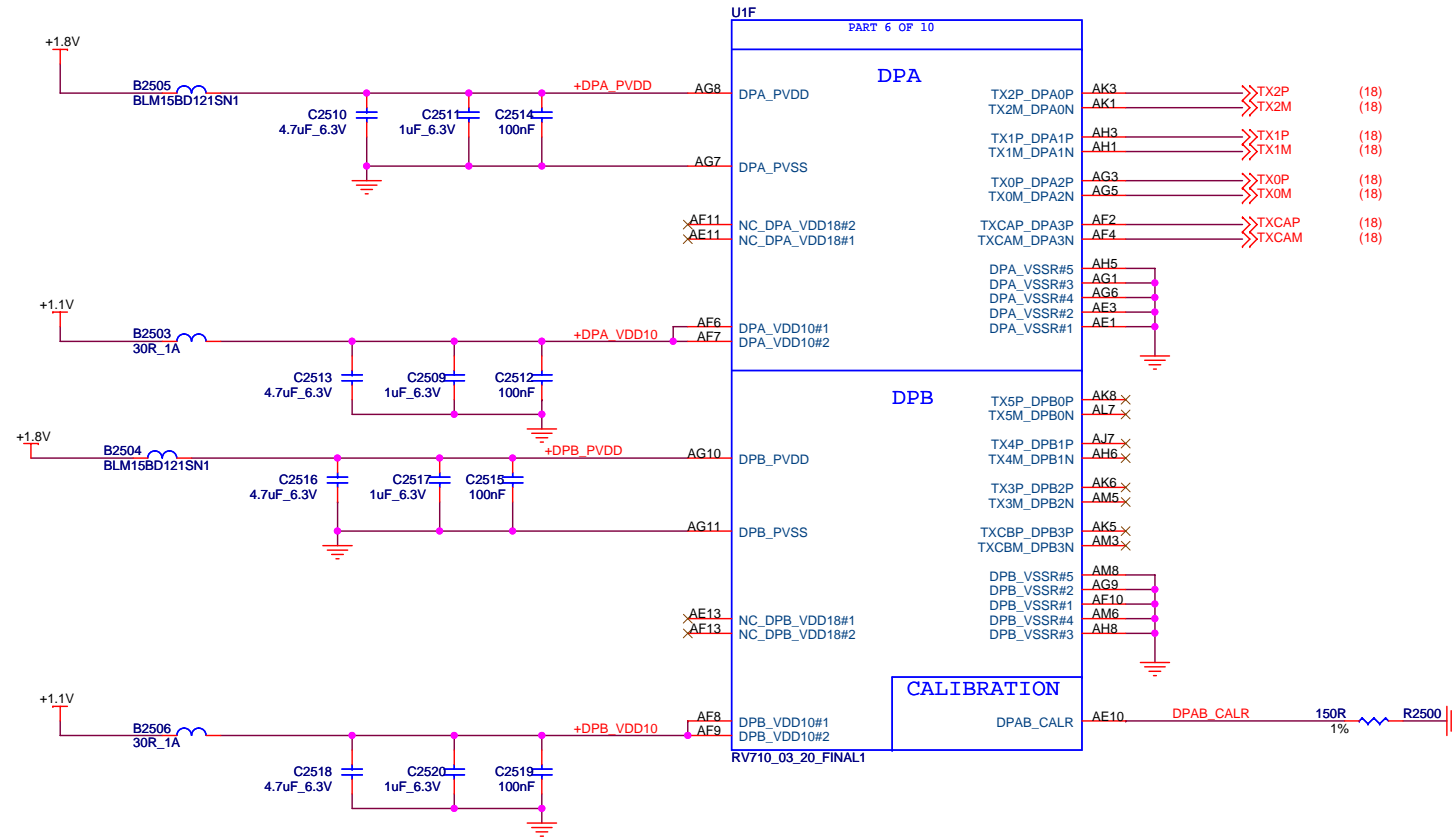


CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
7207 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic or design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.


Advanced Micro Devices Inc.  
1 Commerce Valley Drive East  
Markham, Ontario  
Date: Thursday, October 23, 2008 Rev 0  
Sheet 4 of 22



# TMDP INTERFACE

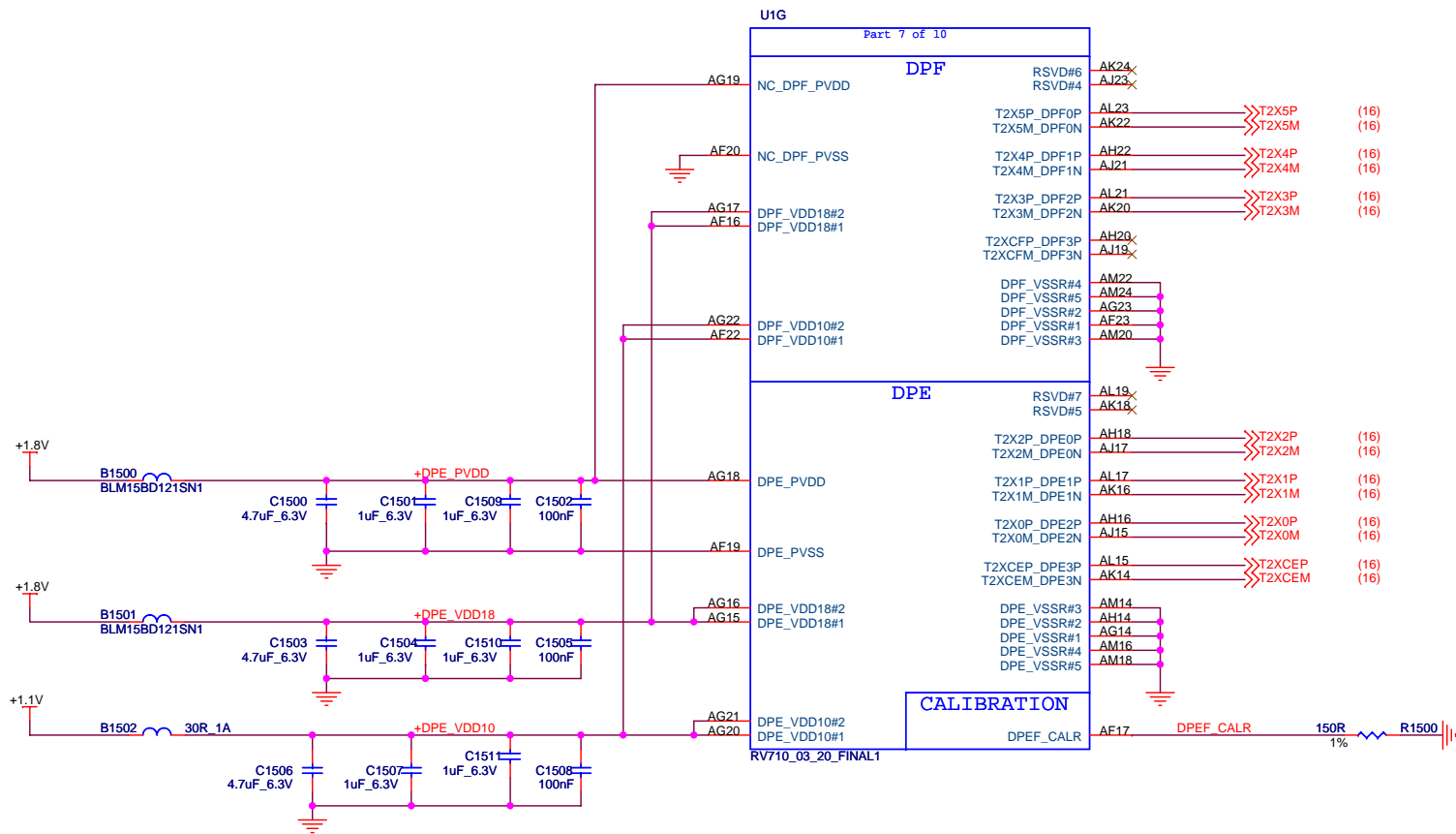


CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
 ?2007 Advanced Micro Devices  
 This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.


Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario			
Date: Thursday, October 23, 2008			Rev 0
Sheet 5 of 22			
TVO DVI		Doc No. 105-B750XX-00A	

Title RH LP RV710 DDR2 VGA (header) TVO DVI

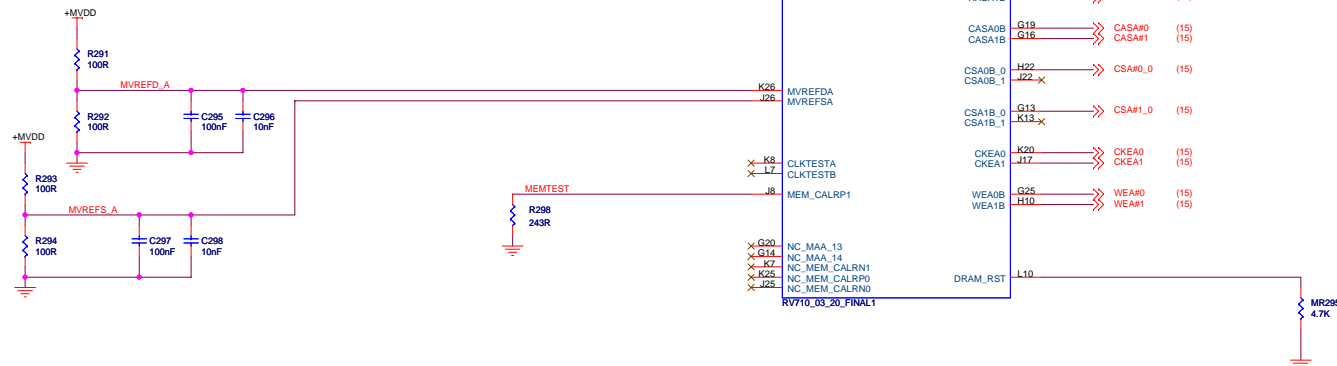
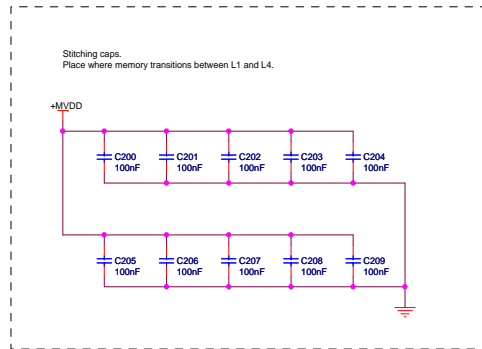
# LVTMDP INTERFACE



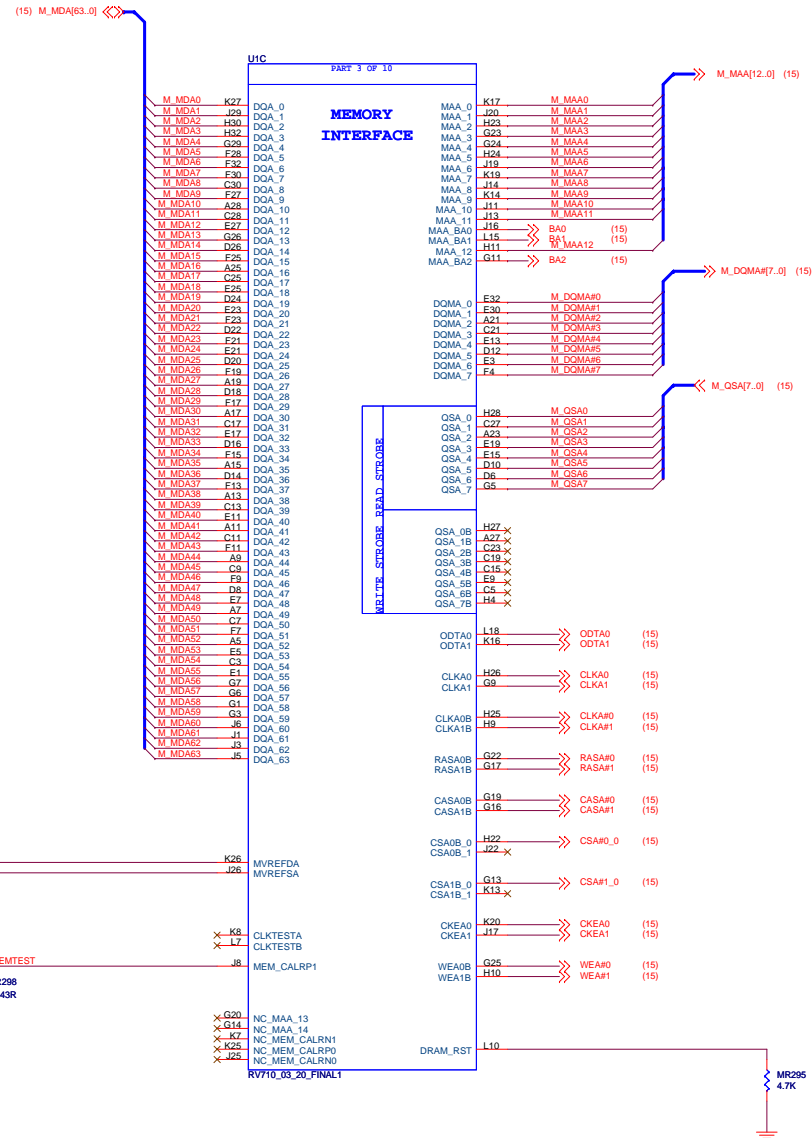
CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
©2007 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario		
Date: Thursday, October 23, 2008	Rev 0	
Sheet 6 of 22		
Title RH LP RV710 DDR2 VGA (header) TVO DVI		Doc No. 105-B750XX-00A

## MEMORY INTERFACE



DIVIDER RESISTORS	DDR2
MVREF TO 1.8V	100R
MVREF TO GND	100R



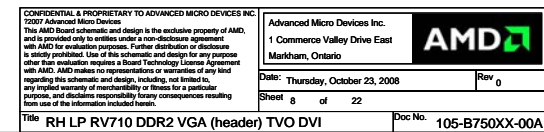
CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
72007 Advanced Micro Devices

This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting

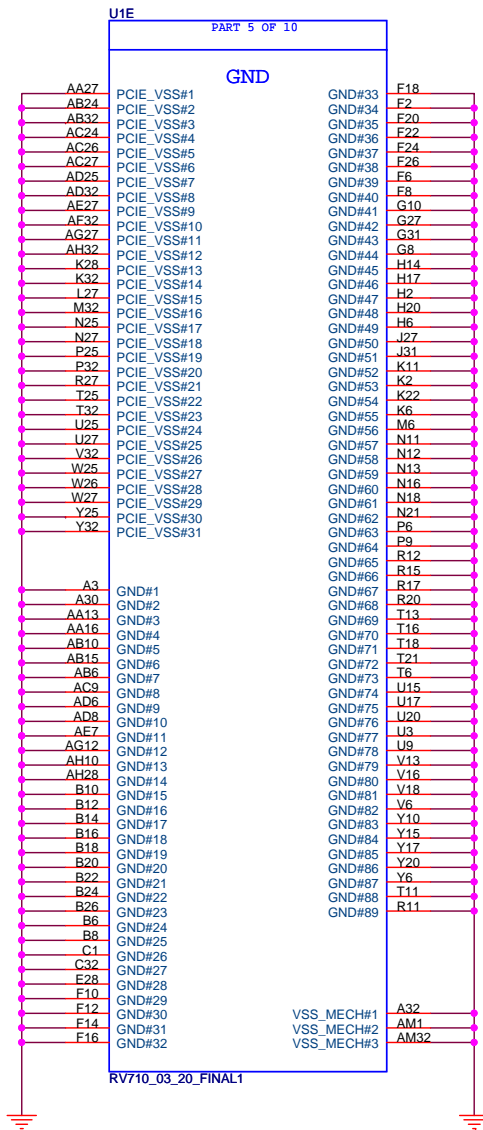
Advanced Micro Devices Inc.  
1 Commerce Valley Drive East  
Markham, Ontario

Date: Thursday, October 23, 2008	Rev 0
Sheet 7 of 22	

Title		RH LP RV710 DDR2 VGA (header) TVO DVI		Doc No.		105-B750XX-00A	
-------	--	---------------------------------------	--	---------	--	----------------	--







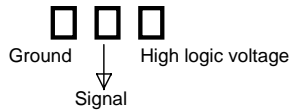
## PIN BASED STRAPS

Pull-Down Resistors are for BU until built-in pull-downs are verified.

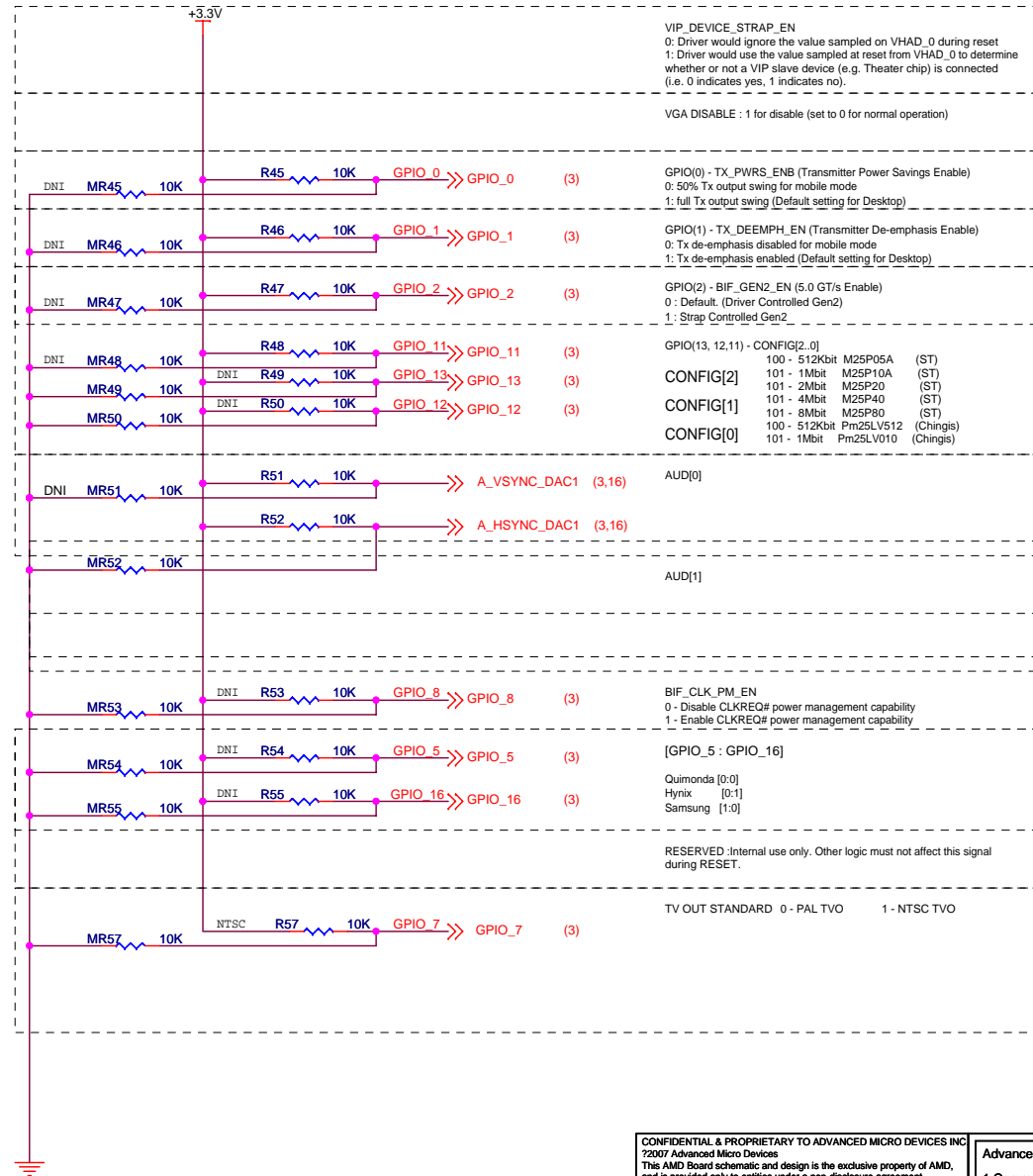


Overlap pads to save space  
and to prevent assembly of  
both resistors.

Layout



## PIN BASED STRAPS




CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
©2007 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario		
Date: Thursday, October 23, 2008	Rev 0	
Sheet 10 of 22		Doc No. 105-B750XX-00A

Title RH LP RV710 DDR2 VGA (header) TVO DVI



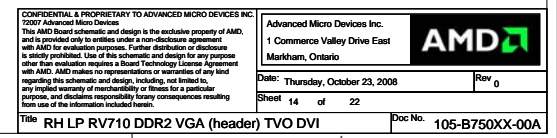
Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario			
Date: Thursday, October 23, 2008		Rev 0	
Sheet 11 of 22			



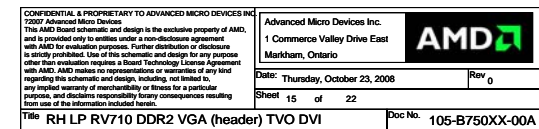


$$V_{out} = 1.25V * [1 + (R_{305}/R_{304})]$$





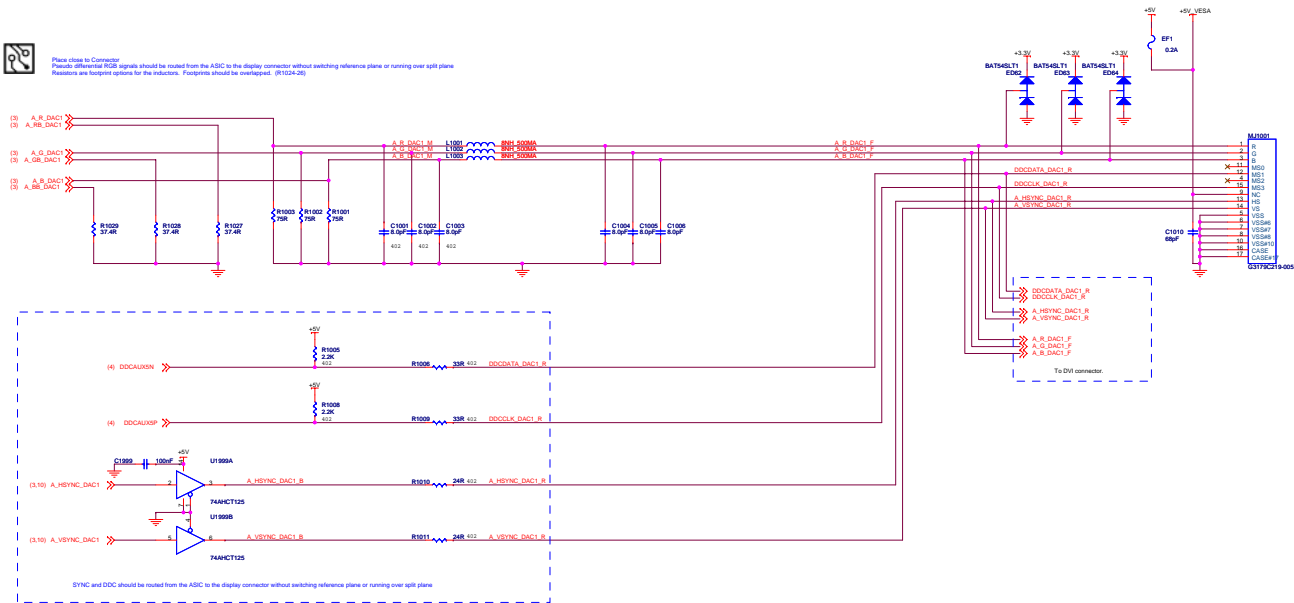
**MAX DENSITY: 64Mx16**



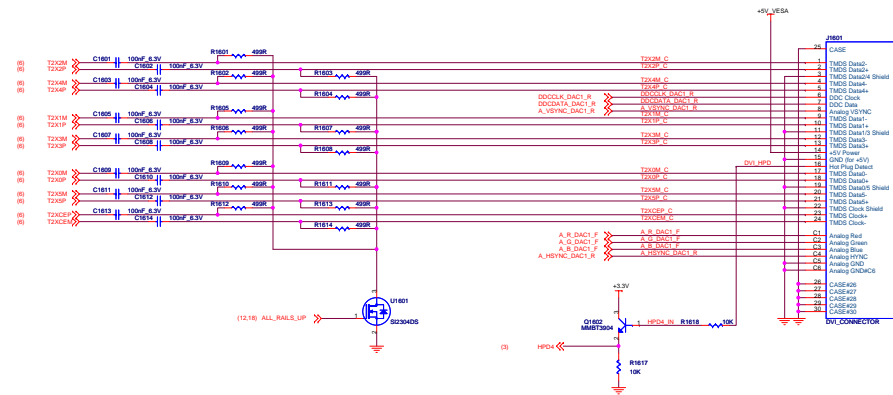
## DAC 1 OUTPUT



Place close to Connector  
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane  
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)

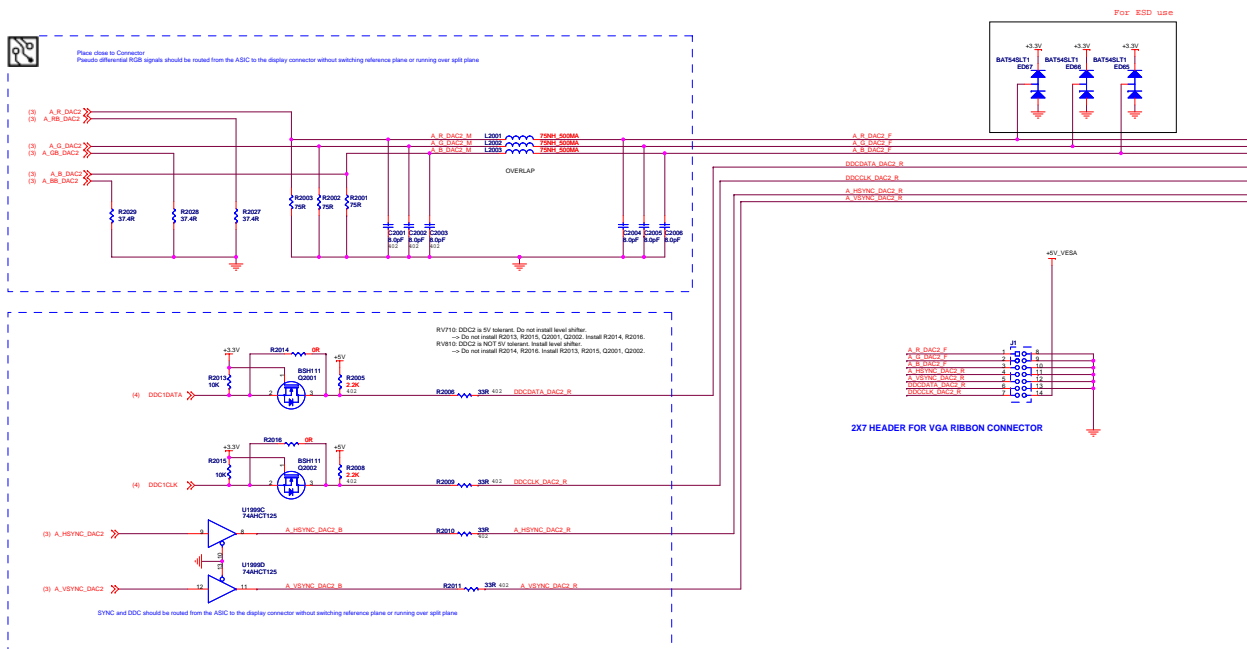


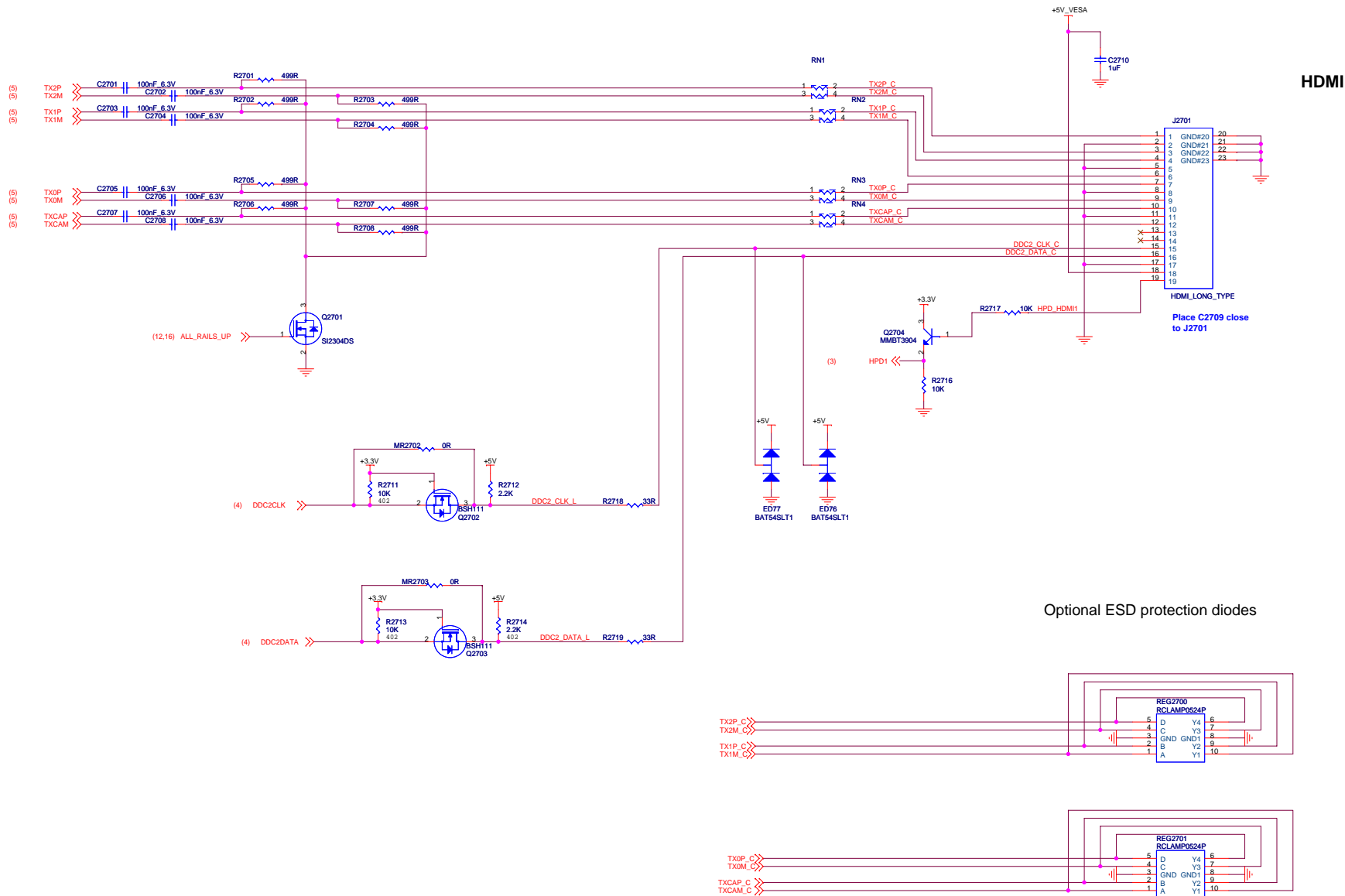
## DPE / DPF OUTPUT





## DAC 2 OUTPUT

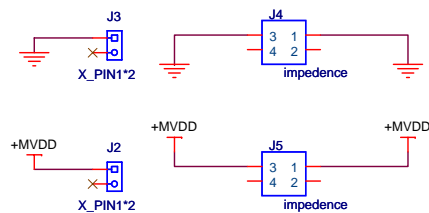
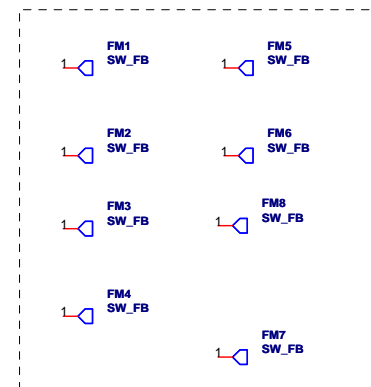
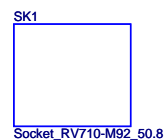
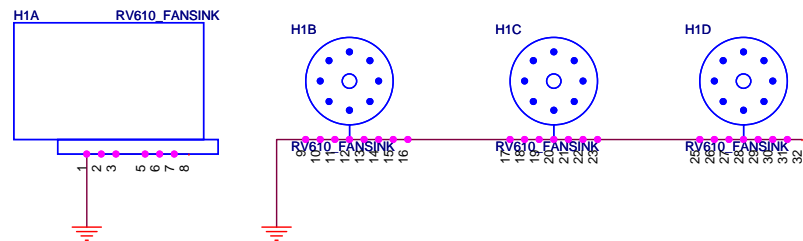


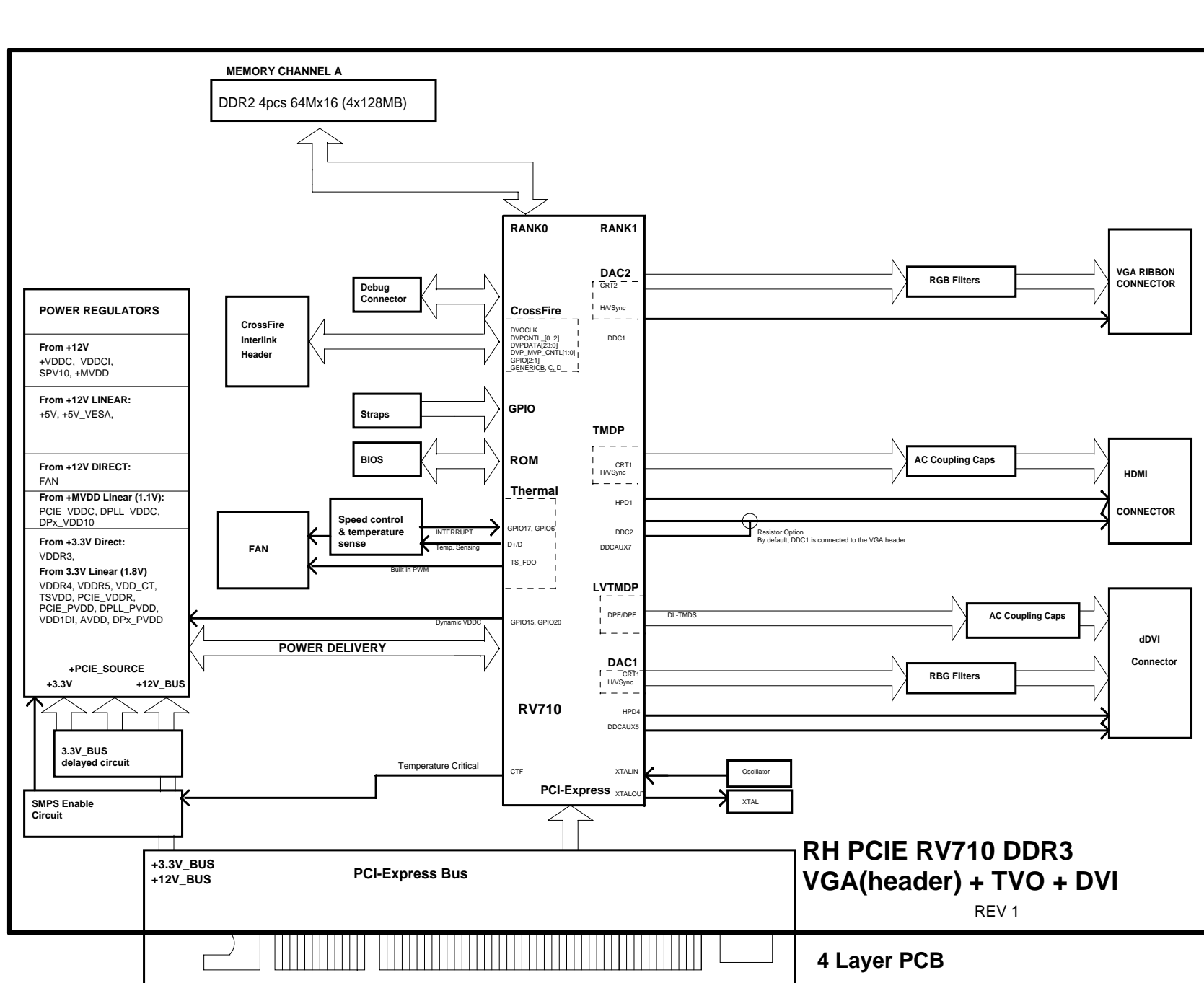


CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
 7207 Advanced Micro Devices  
 This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

Advanced Micro Devices Inc.  
 1 Commerce Valley Drive East  
 Markham, Ontario  
 Date: Thursday, October 23, 2008 Rev 0  
 Sheet 18 of 22  
 Title RH LP RV710 DDR2 VGA (header) TVO DVI Doc No. 105-B750XX-00A







**RH PCIE RV710 DDR3  
VGA(header) + TVO + DVI**  
REV 1

**4 Layer PCB**

<div>AMD</div>			Title		Schematic No.		Date:	
			RH LP RV710 DDR2 VGA (header) TVO DVI		105-B750XX-00A		Thursday, October 23, 2008	
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.					Rev 0
Sch Rev	PCB Rev	Date	RV710 ENGINEERING BOARD REVISION DESCRIPTION					
01	00A	2008.04.02	INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.					