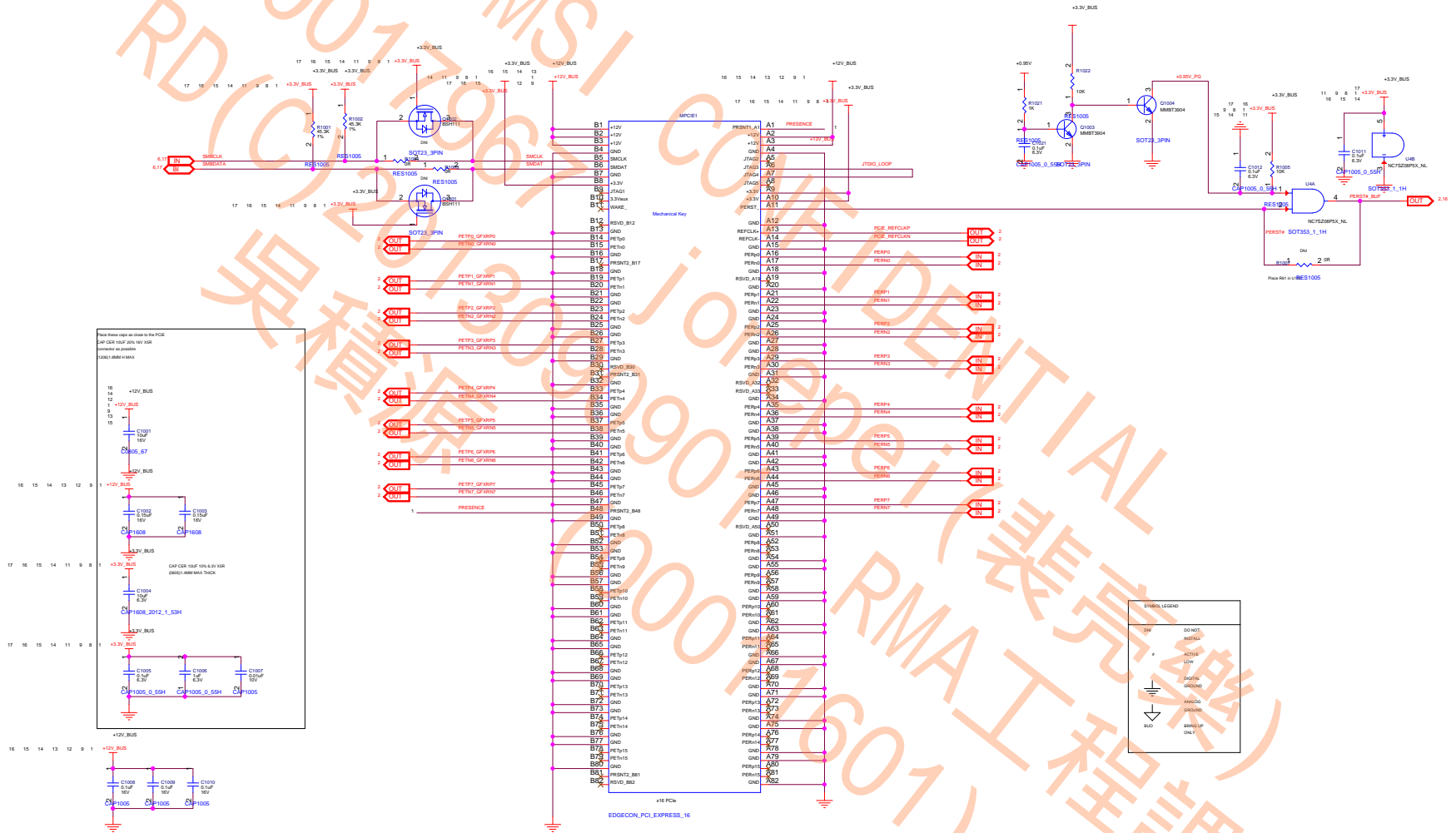
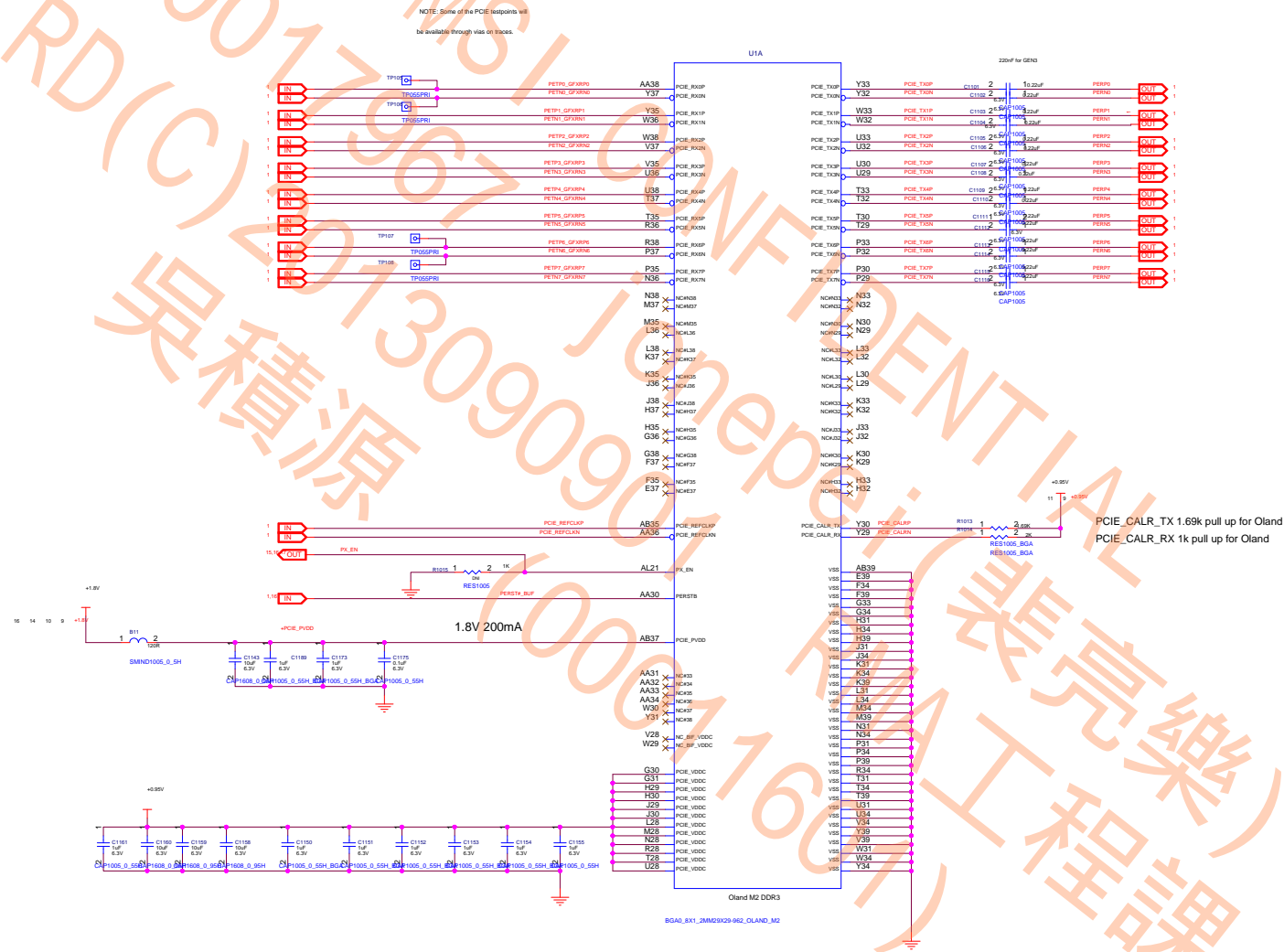


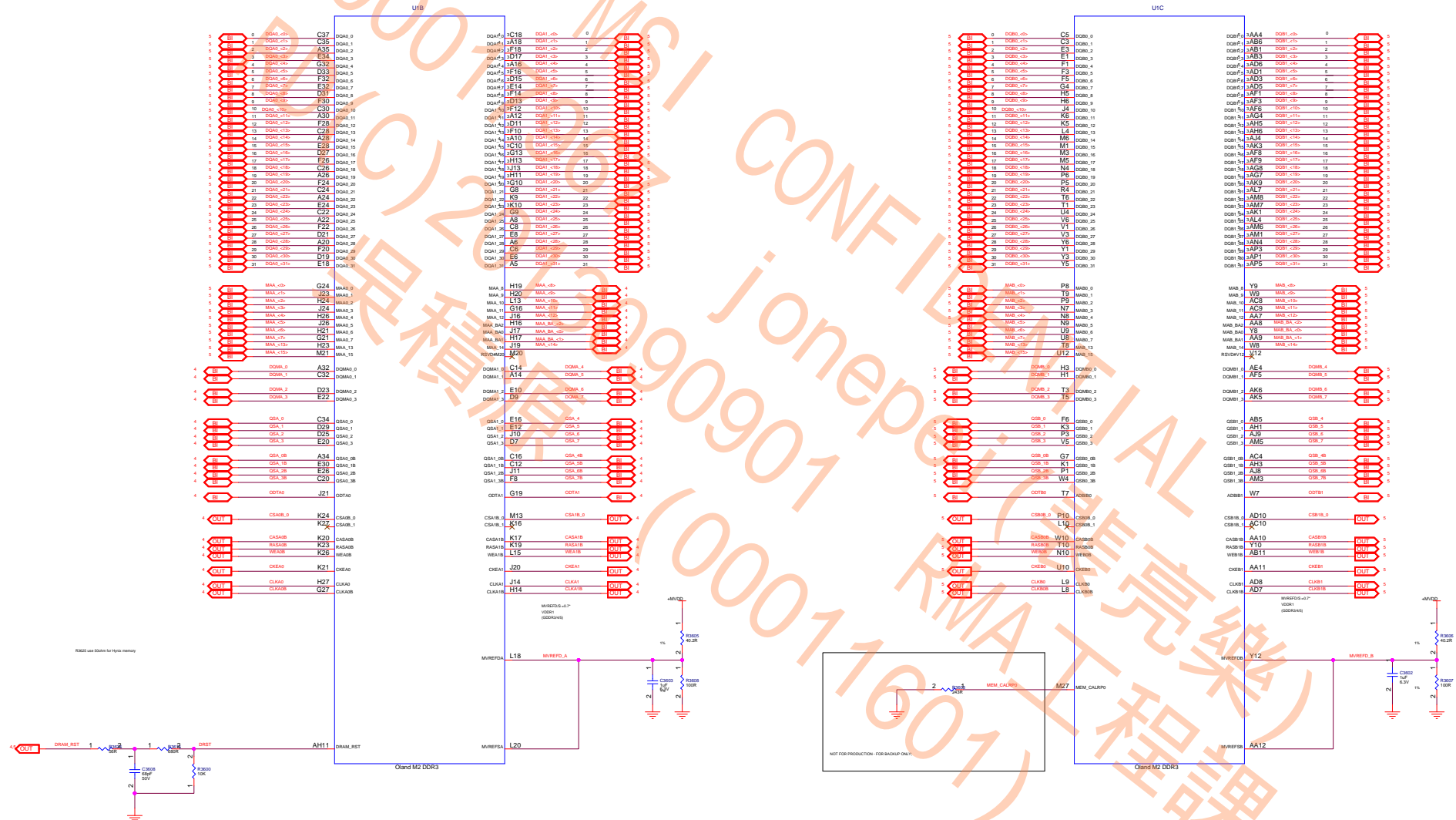
PCI-EXPRESS EDGE CONNECTOR



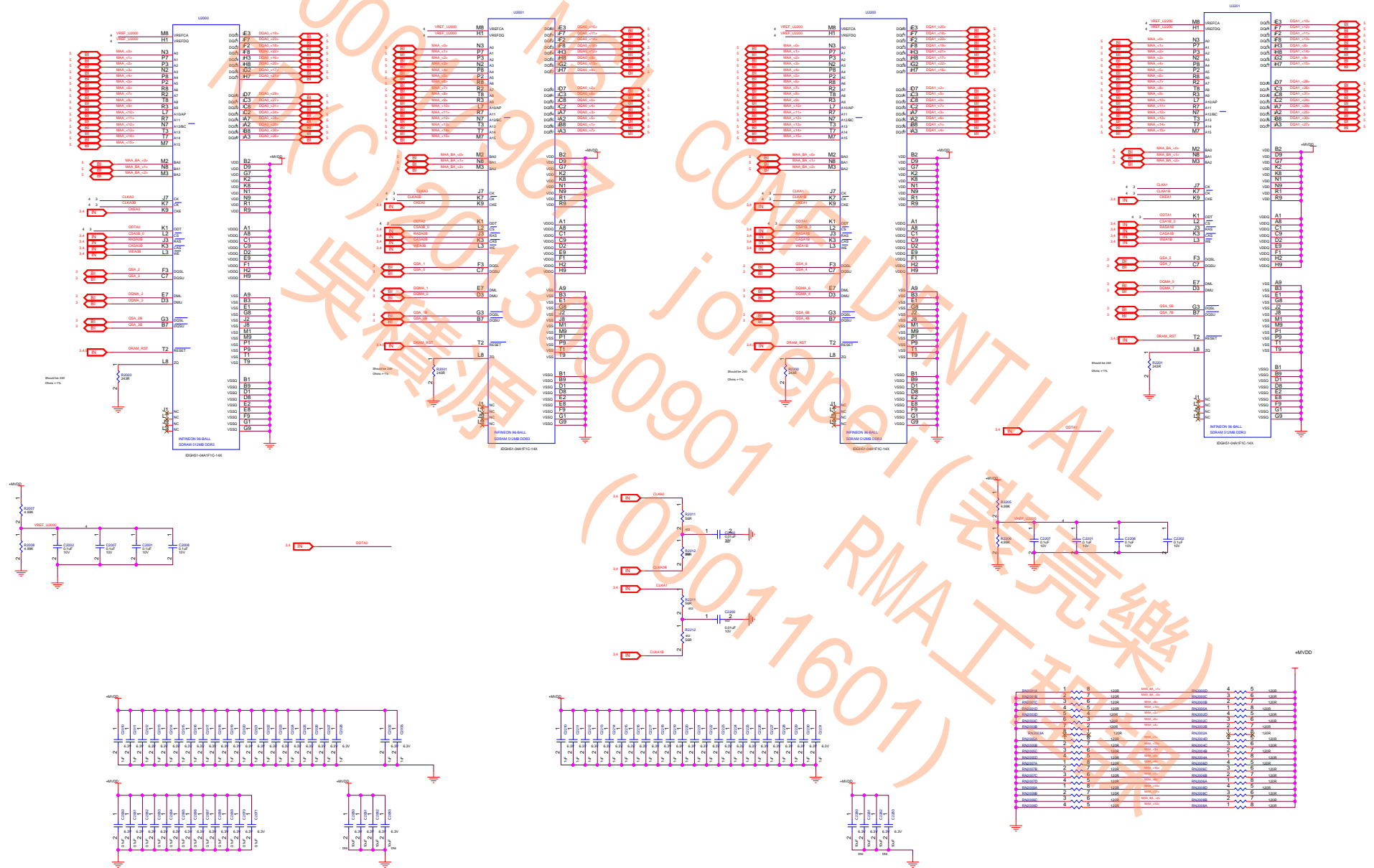
Oland XT M2 PCIe Interface

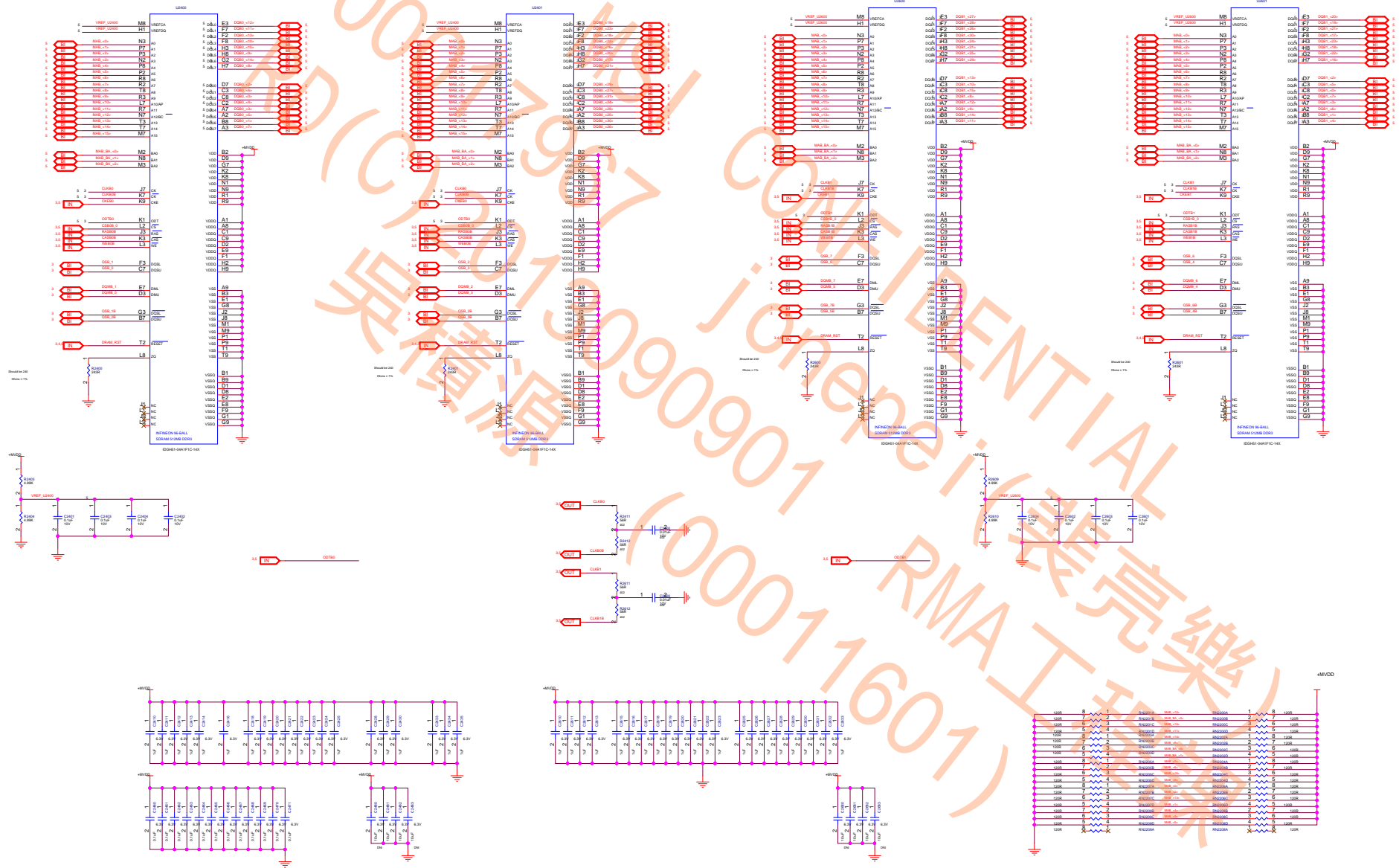


(3)Oland XT MEM Interface Ch A&B

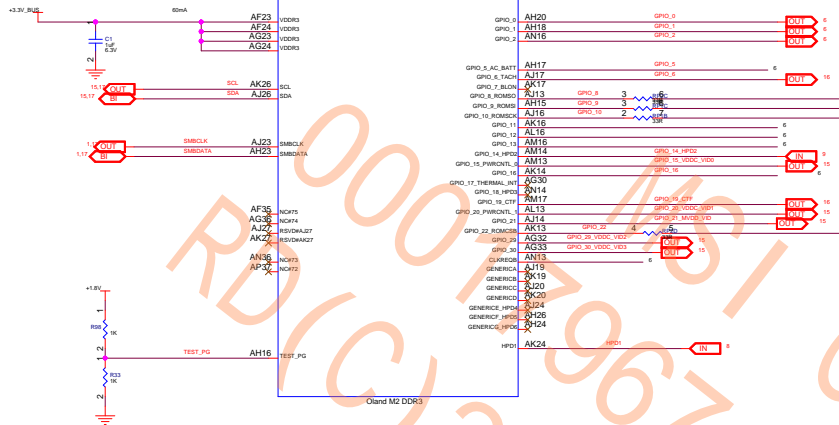


(4) DDR3 Memory Channel A

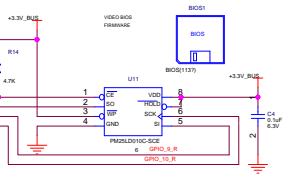




Oland XT M2 GPIOs Strap CF XTAL OSC



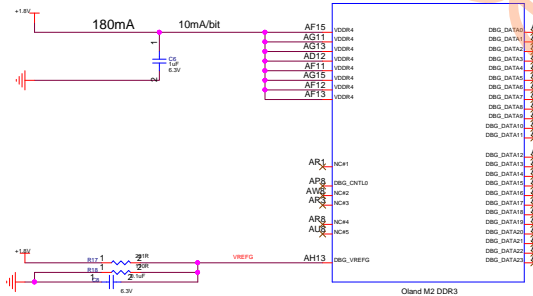
PN 2280079000 for 1Mbit (PM2SLV010A-100SC)



PN BASED STRAPS

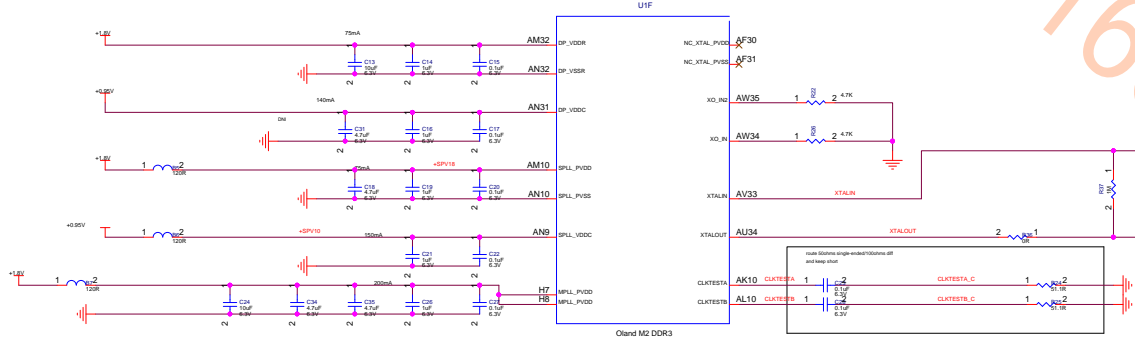


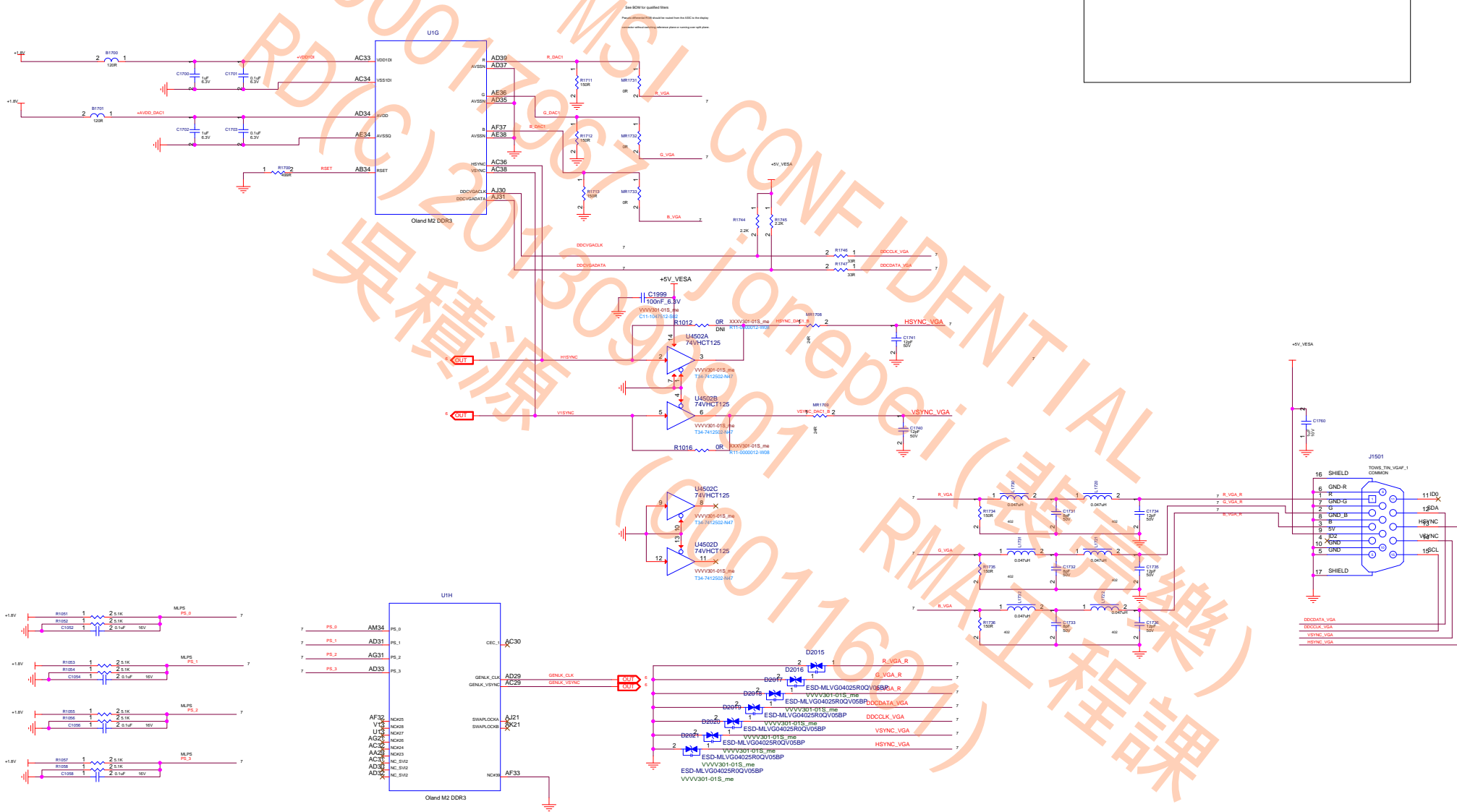
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STRAP_TX_DEEMPH_EN	TX Deemphasis Enabled
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STRAP_TX_DEEMPH_1	TX Deemphasis Disabled
STRAP_TX_DEEMPH_2	TX Deemphasis Disabled
STRAP_TX_DEEMPH_3	TX Deemphasis Disabled
STRAP_TX_DEEMPH_4	TX Deemphasis Disabled
STRAP_TX_DEEMPH_5	TX Deemphasis Disabled
STRAP_TX_DEEMPH_6	TX Deemphasis Disabled
STRAP_TX_DEEMPH_7	TX Deemphasis Disabled
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STRAP_TX_DEEMPH_9	TX Deemphasis Disabled
STRAP_TX_DEEMPH_10	TX Deemphasis Disabled
STRAP_TX_DEEMPH_11	TX Deemphasis Disabled
STRAP_TX_DEEMPH_12	TX Deemphasis Disabled
STRAP_TX_DEEMPH_13	TX Deemphasis Disabled
STRAP_TX_DEEMPH_14	TX Deemphasis Disabled
STRAP_TX_DEEMPH_15	TX Deemphasis Disabled
STRAP_TX_DEEMPH_16	TX Deemphasis Disabled
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STRAP_TX_DEEMPH_100	TX Deemphasis Disabled

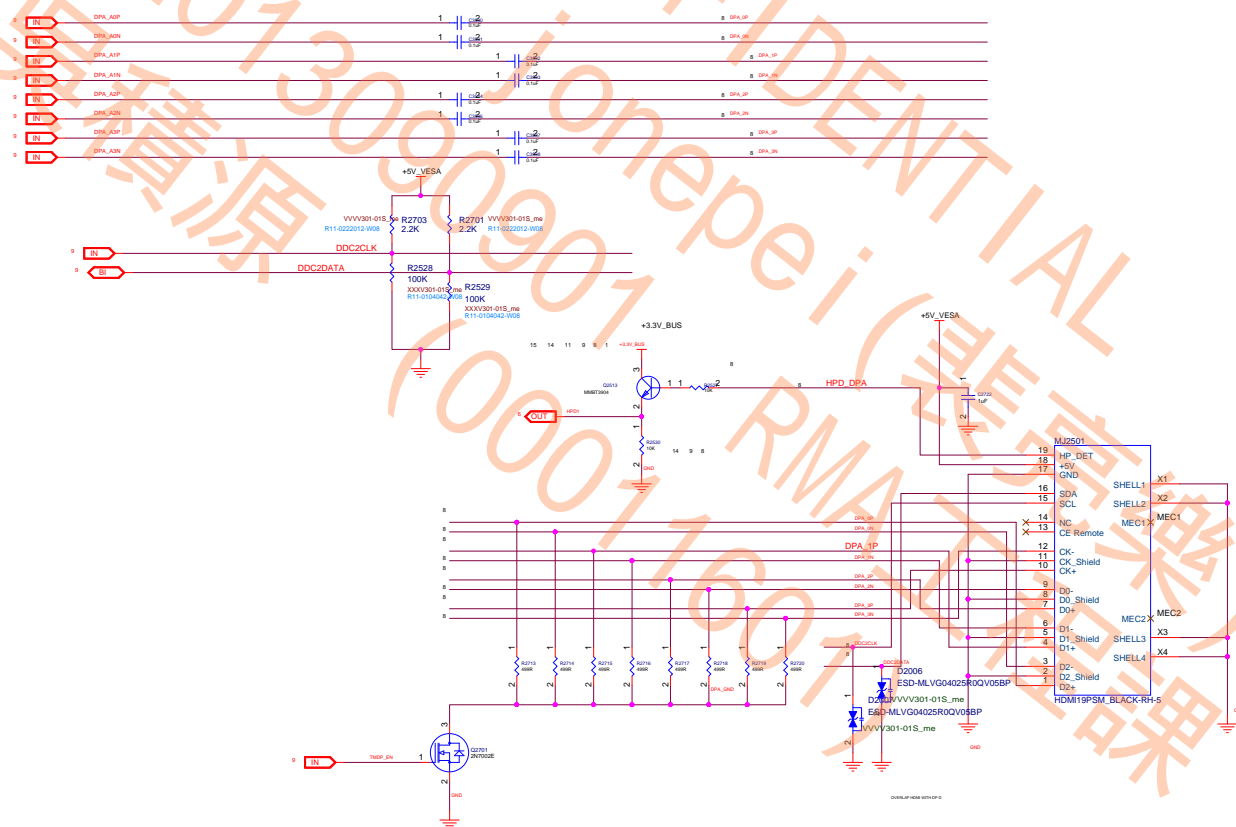
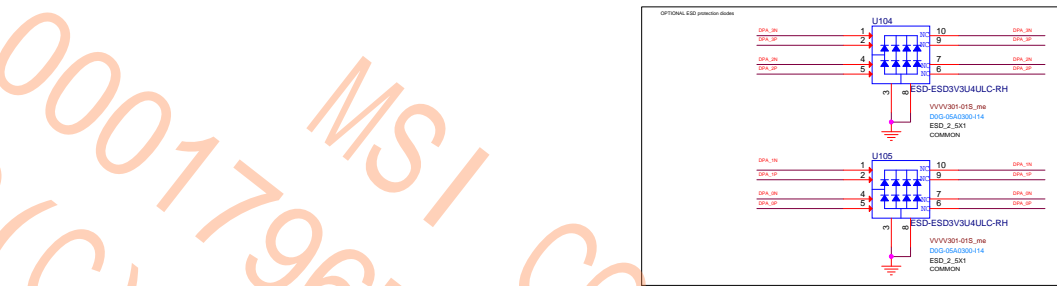


Place the crossover
resistors near the ASIC and
not the connector

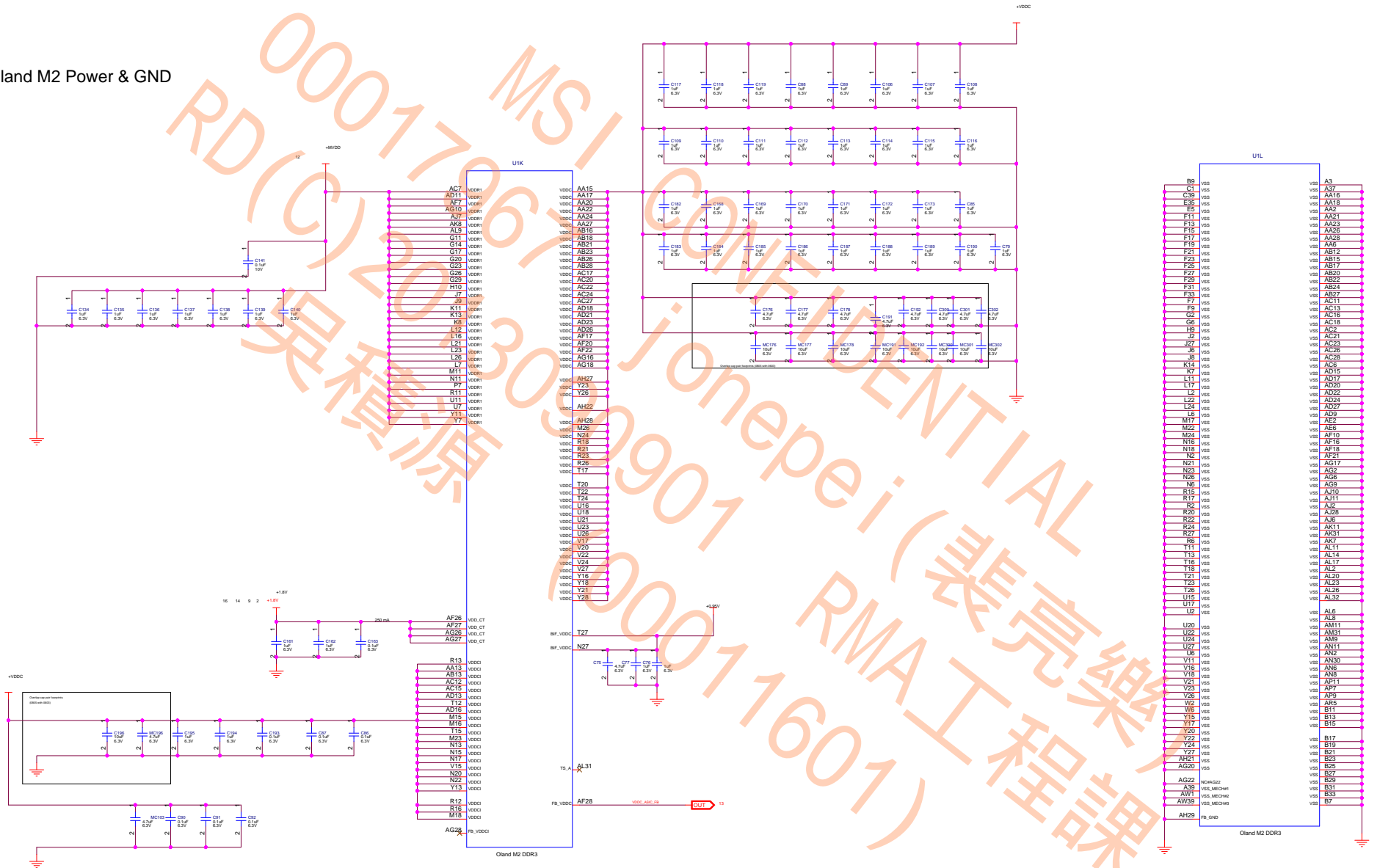
Please pay attention to the
strategies for these filter capacitors to
maintain a close loop for current.





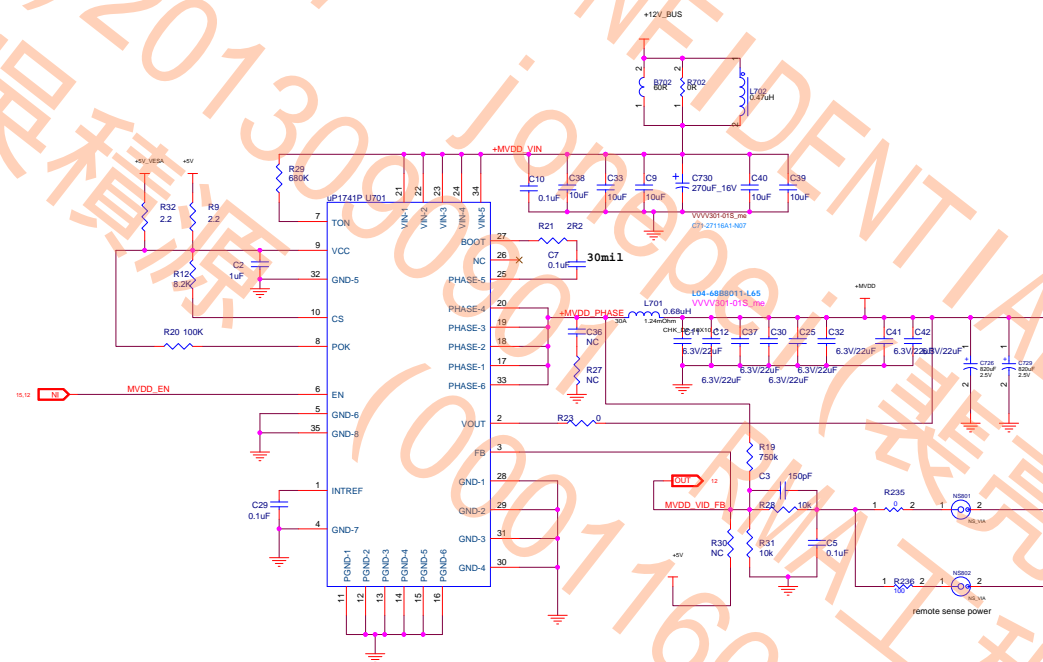


Oland M2 Power & GND



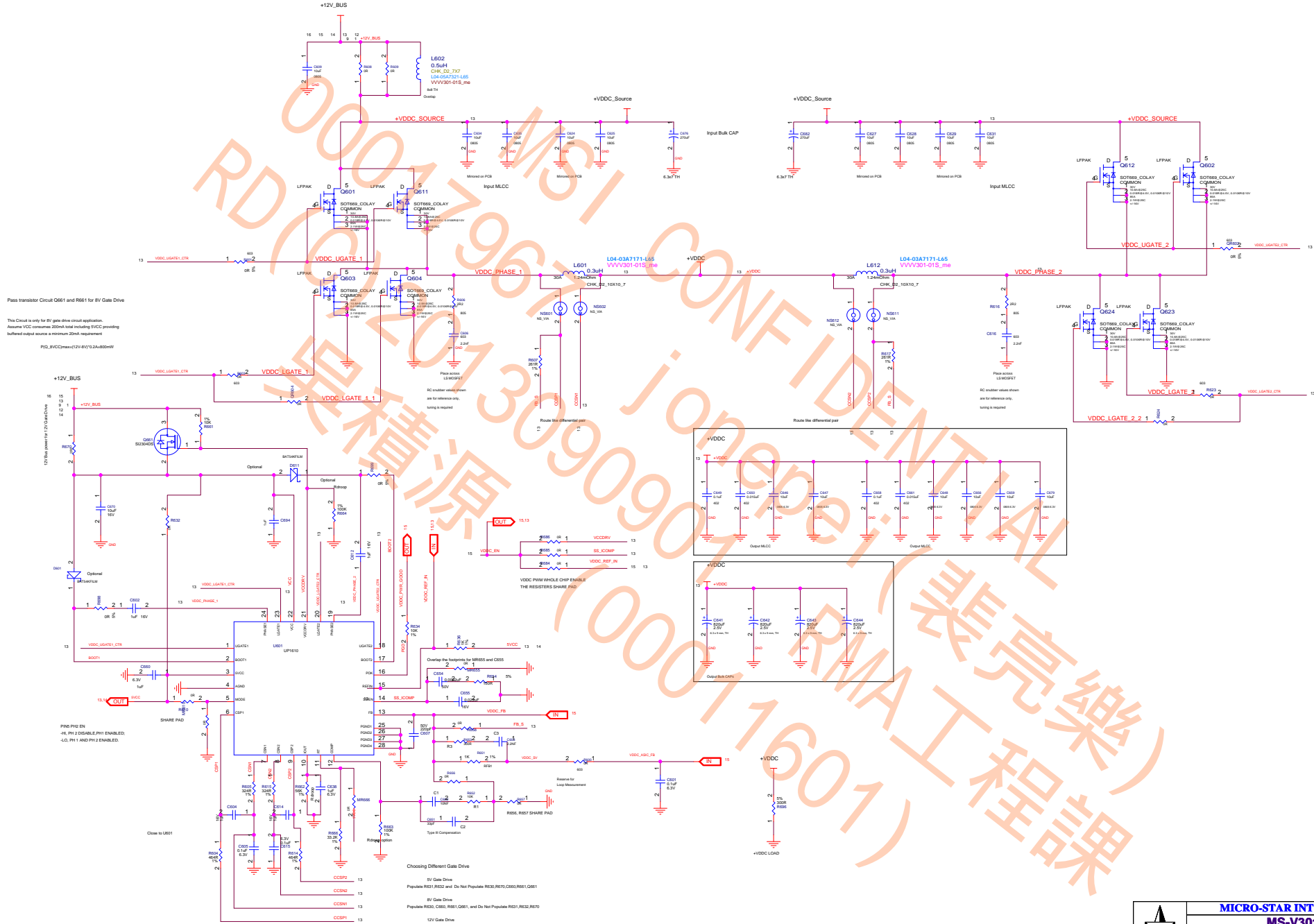


MVDD



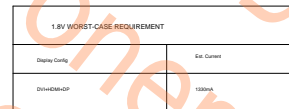
MICRO-STAR INT'L CO.,LTD
MS-V301

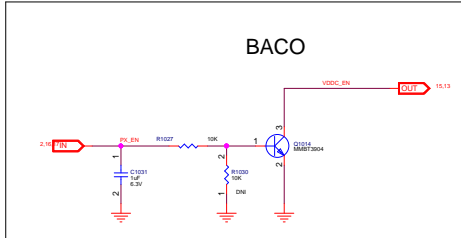
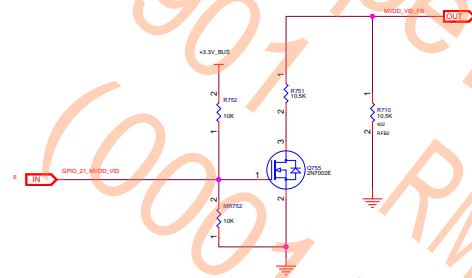
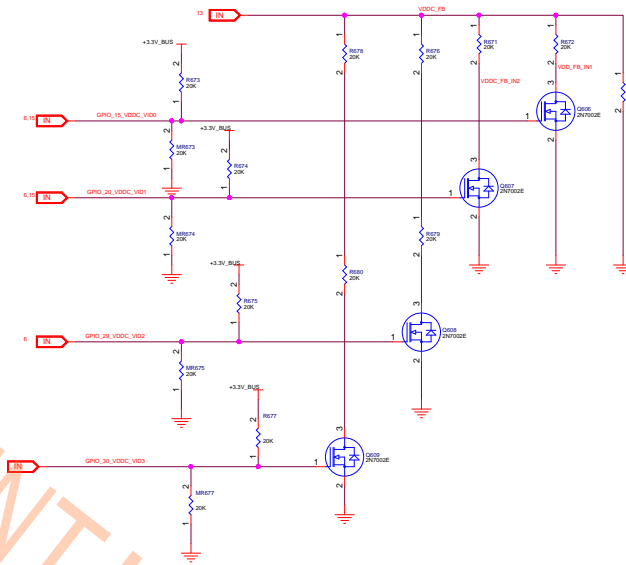
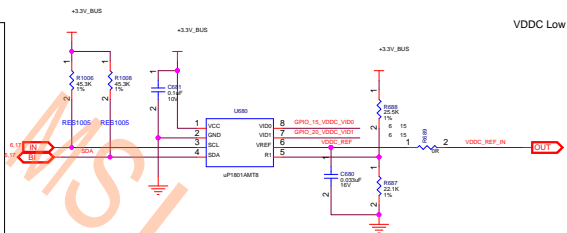
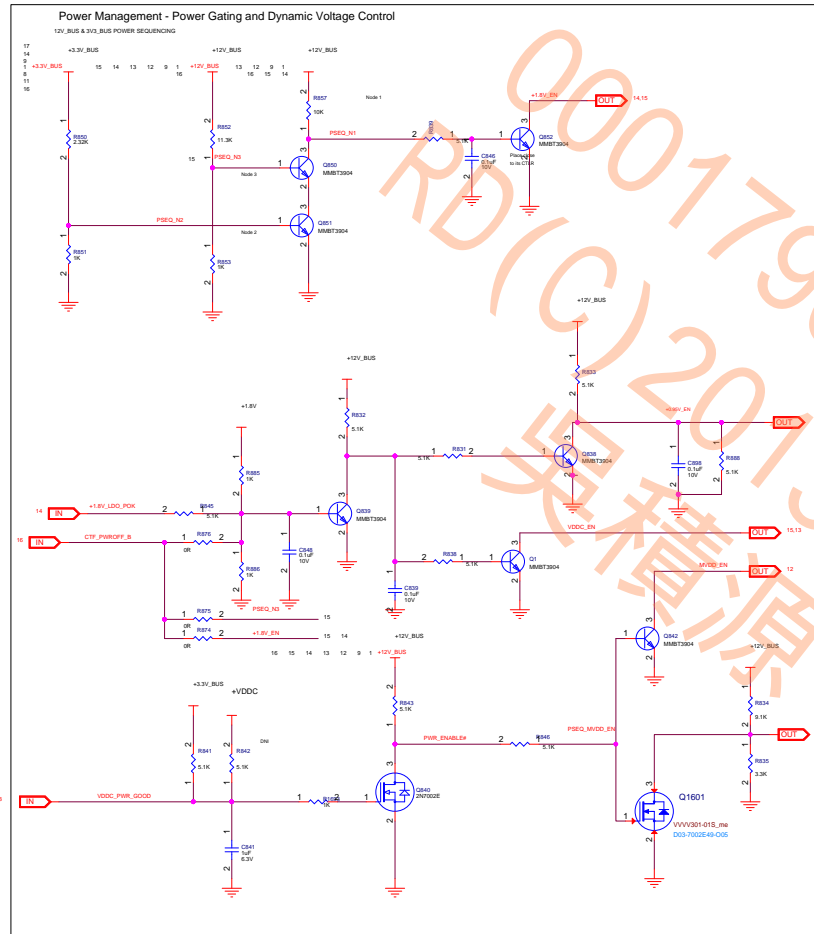
Size Custom	Document Description MVDD	Rev 1.1
Date: Tuesday, August 06, 2013		Sheet 12 of 20



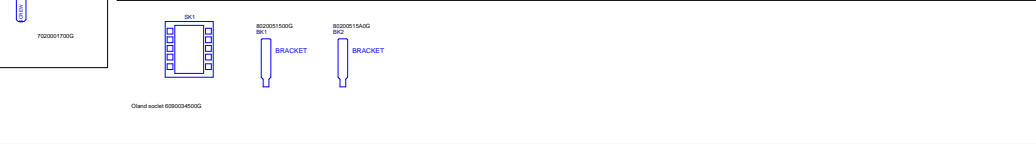
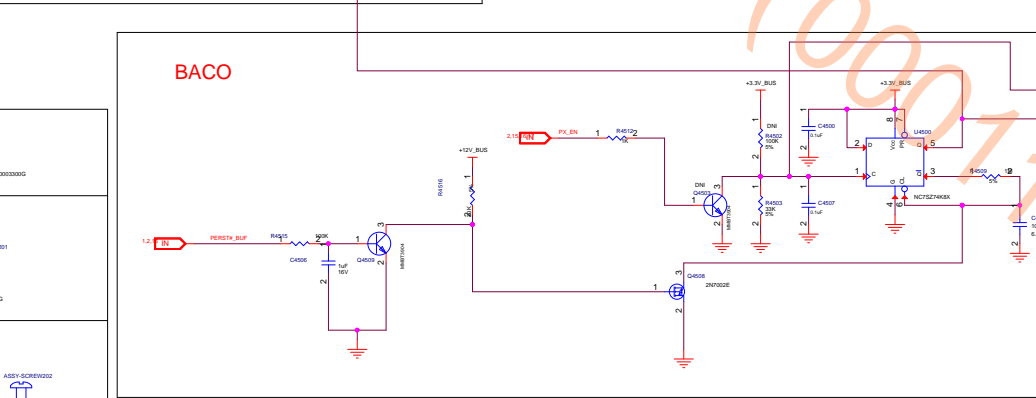
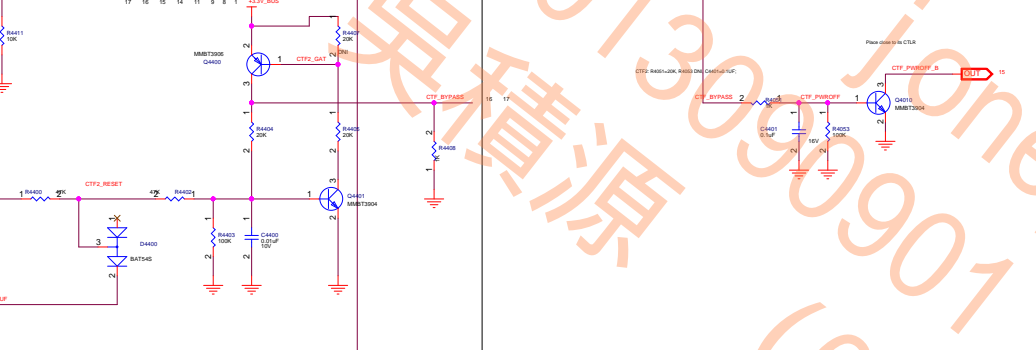
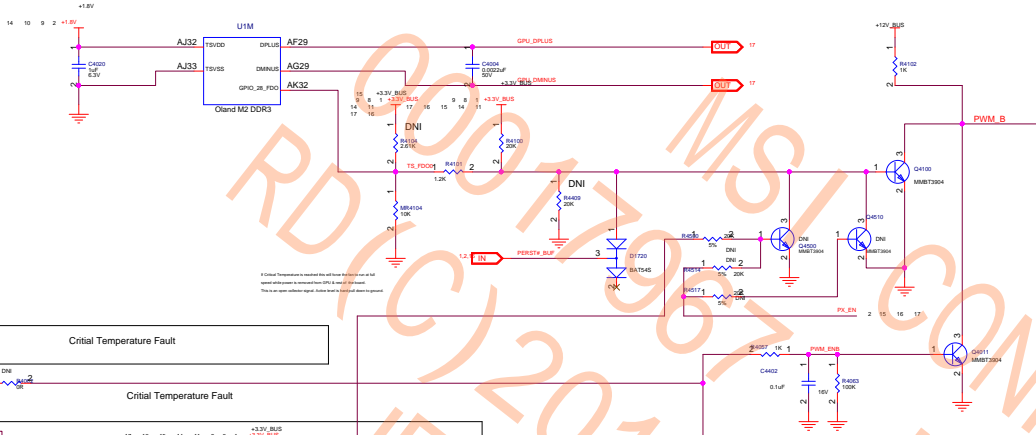
LDO #1: $V_{in} = 3.00V$ to $3.60V$ ($3.3V \pm 9\%$) $V_{out} = +1.8V \pm 2\%$ $I_{out} = 1.6A$ (TYP) RMS MAX
 PCB: 50 to 70mm sq, copper area for cooling

Regulators for +5V, +5V_VESA and +5V_VESA2

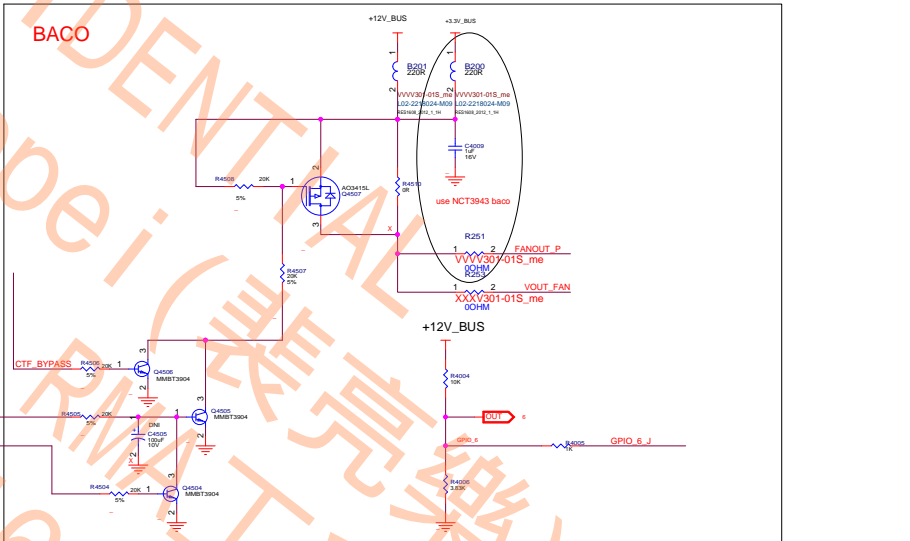
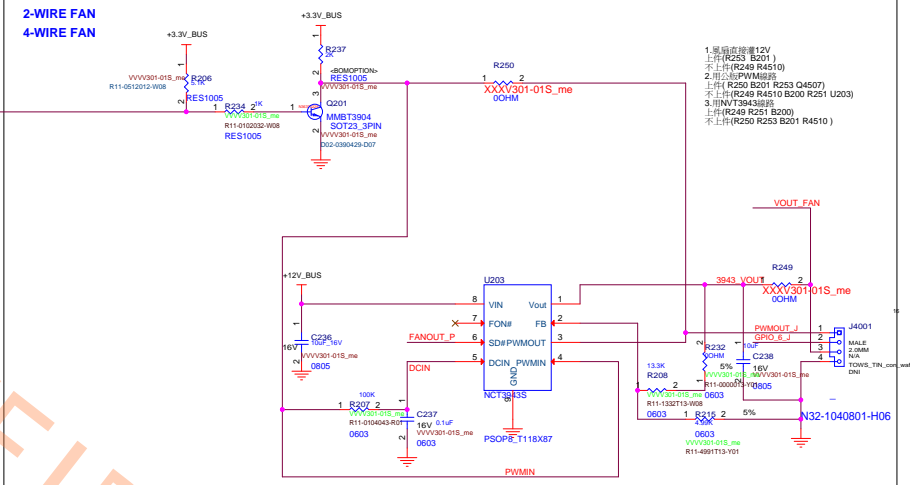




Mechanical and Thermal Management



Fan Control (New)



[illegible]

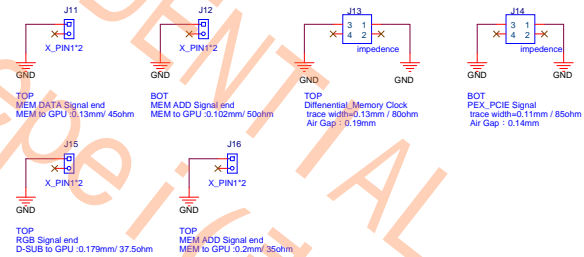
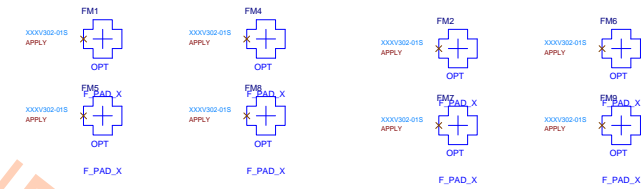
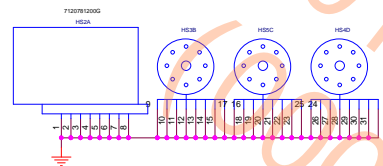
VERDE XT FANBANK H518

VERDE XT FANBANK H51C

VERDE XT FANBANK H51D

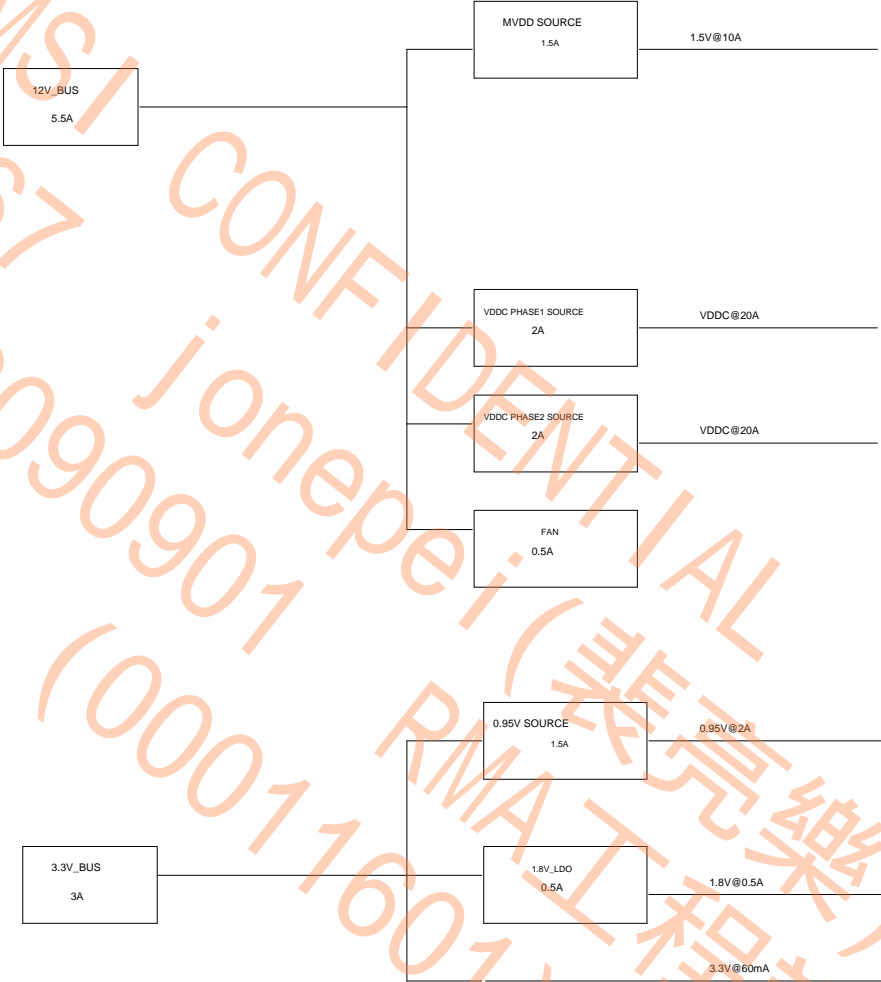
VERDE XT FANBANK H51D

7121000100G



DN11	HPD1	DDCALUX1
HEMMDP	HPD1	DDCALUX2

GPIO15	VDDC_VDD	
GPIO28	VDDC_VDD1	
GPIO29	VDDC_VDD2	
GPIO30	VDDC_VDD3	
GPIO21	MVDD_VDD	



TITLE Client via DDR3 2GB SL_DV1-hiHDMI+VcrGA			SCHEMATIC NO. 105-C060XX-00		DATE	
REVISION HISTORY			NOTE THIS SCHEMATIC REPRESENTS THE PCL IT DOES NOT REPRESENT ANY SPECIFIC I/O THIS SCHEMATIC IS A GENERALIZATION OF THE PCL IT DOES NOT REPRESENT ANY SPECIFIC I/O PLEASE CONTACT THE MANUFACTURER TO OBTAIN THE PCL IT DOES NOT REPRESENT ANY SPECIFIC I/O			REV P00
SDH REV	PCB REV	DATE	REVISION DESCRIPTION			
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02	002	20100601	Updated PCB AT schematic based on C060 C060C060			
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