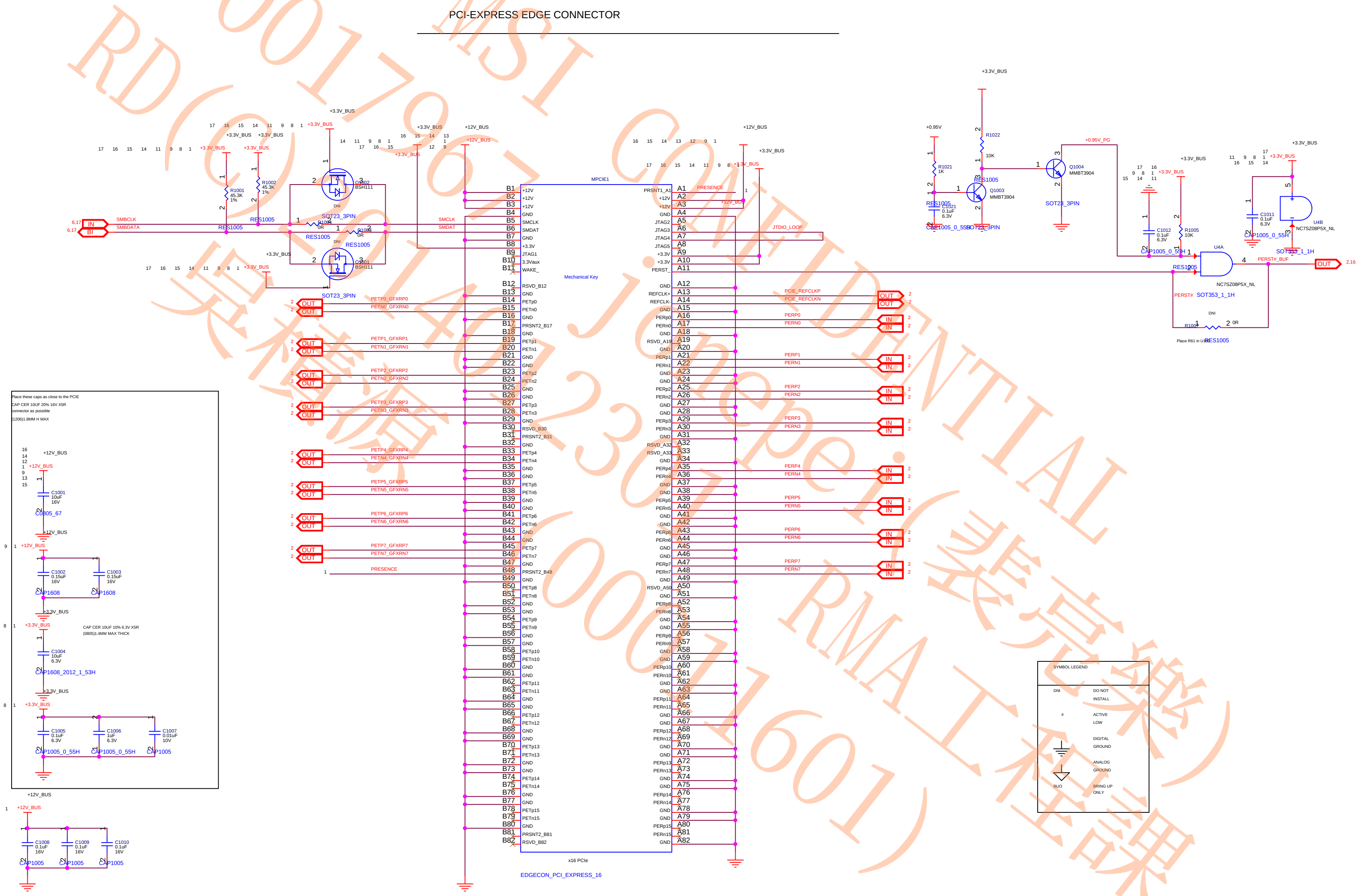
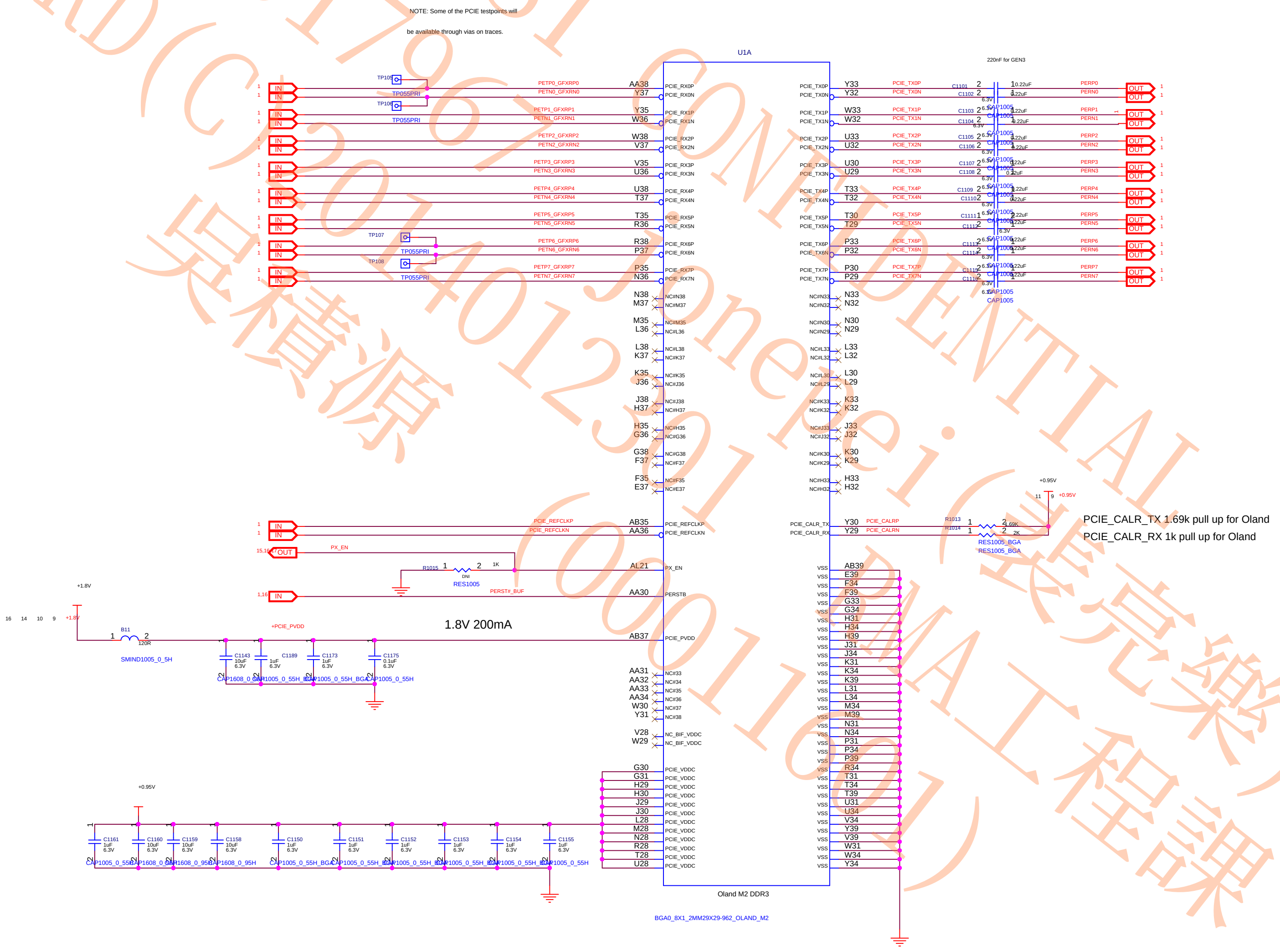
PCI-EXPRESS EDGE CONNECTOR



MICRO-STAR INT'L CO.,LTD	
MS-V301	
Size: Custom	Document Description: PCI-E Edge Connector
Rev	1.1
Date: Tuesday, August 06, 2013	Sheet 1 of 20

Oland XT M2 PCIe Interface


NOTE: Some of the PCIE testpoints will
be available through vias on traces.
U1A
220nF for GEN3
PCIE_RX0P
PCIE_RX0N
PCIE_TX0P
PCIE_TX0N
PETP0_GFXRP0
PETN0_GFXRN0
PERP0
PERN0
TP055PRI
PCIE_REFCLKP
PCIE_REFCLKN
PX_EN
PERSTB
PERST#_BUF
PCIE_PVDD
+PCIE_PVDD
1.8V 200mA
+1.8V
+0.95V
SMIND1005_0_5H
120R
RES1005
PCIE_CALR_TX
PCIE_CALR_RX
PCIE_CALRP
PCIE_CALRN
RES1005_BGA
PCIE_CALR_TX 1.69k pull up for Oland
PCIE_CALR_RX 1k pull up for Oland
NC_BIF_VDDC
PCIE_VDDC
VSS
CAP1005
Oland M2 DDR3
BGA0_8X1_2MM29X29-962_OLAND_M2

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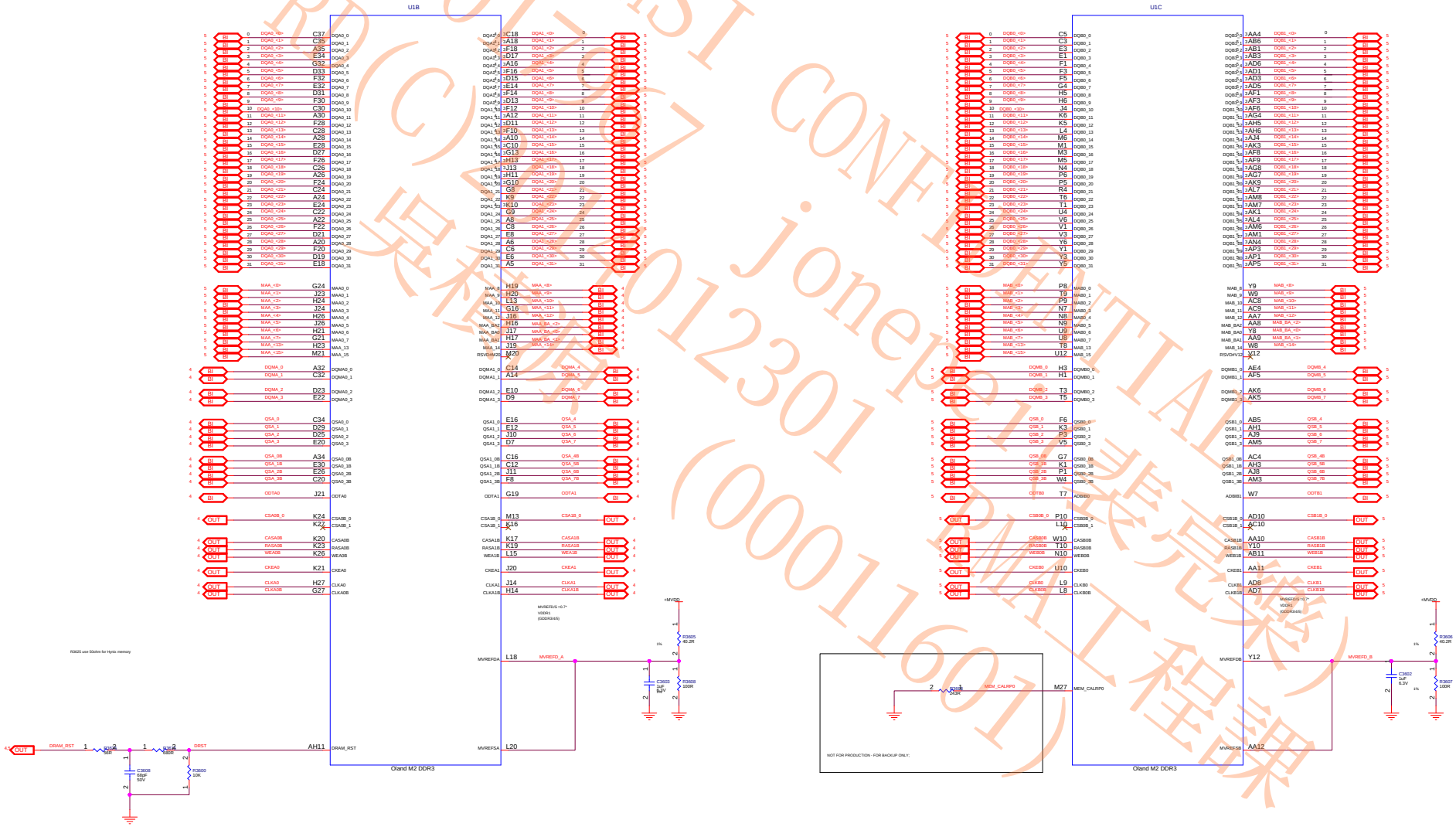
MS-V301

Size	Document Description	Rev
Custom	Oland PCIE Interface	1.1

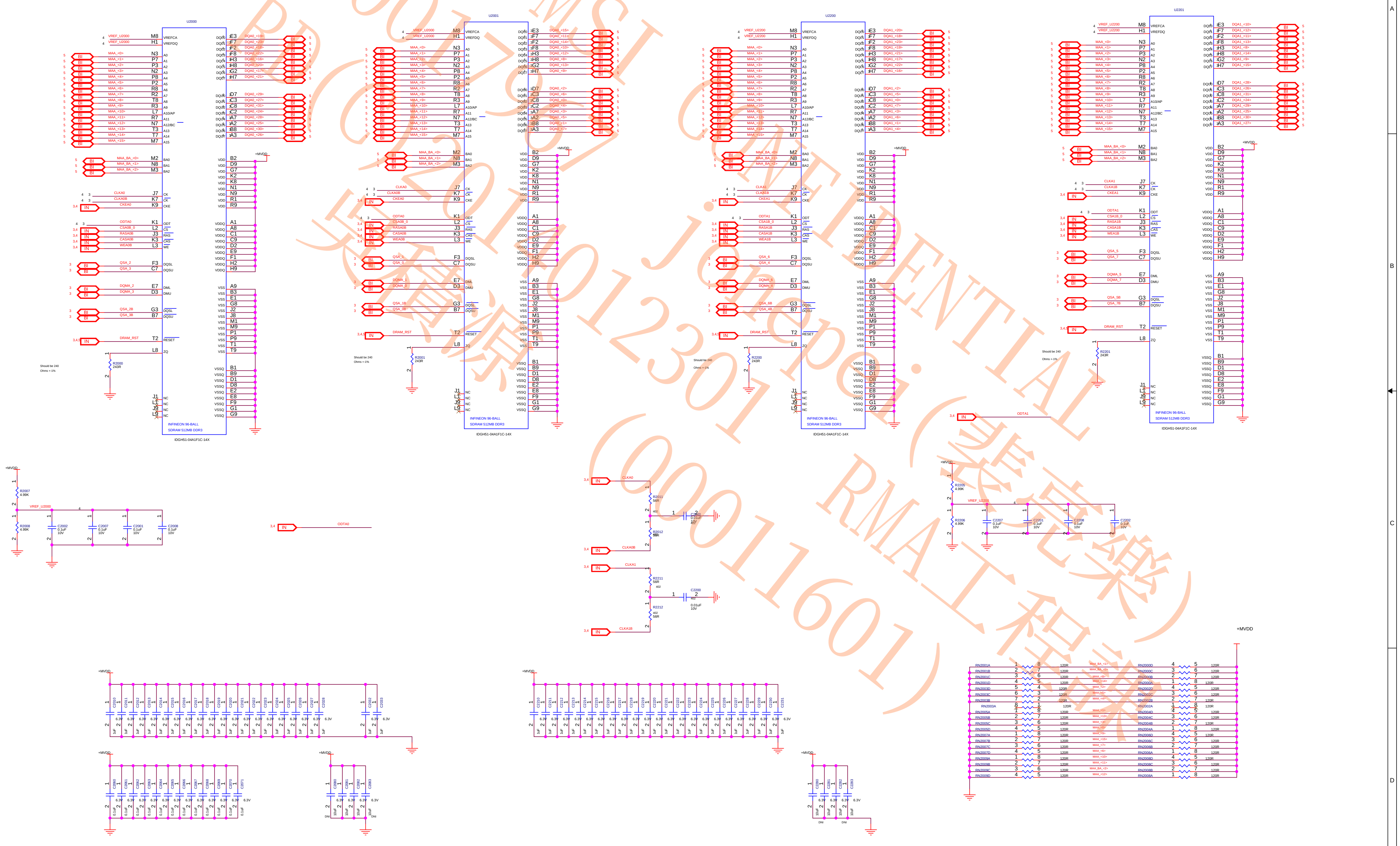
Date: Tuesday, August 06, 2013 Sheet 2 of 20

(3)Oland XT MEM Interface Ch A&B



MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: Oland MEMORY INTERFACE	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 3 of 20	

(4) DDR3 Memory Channel A



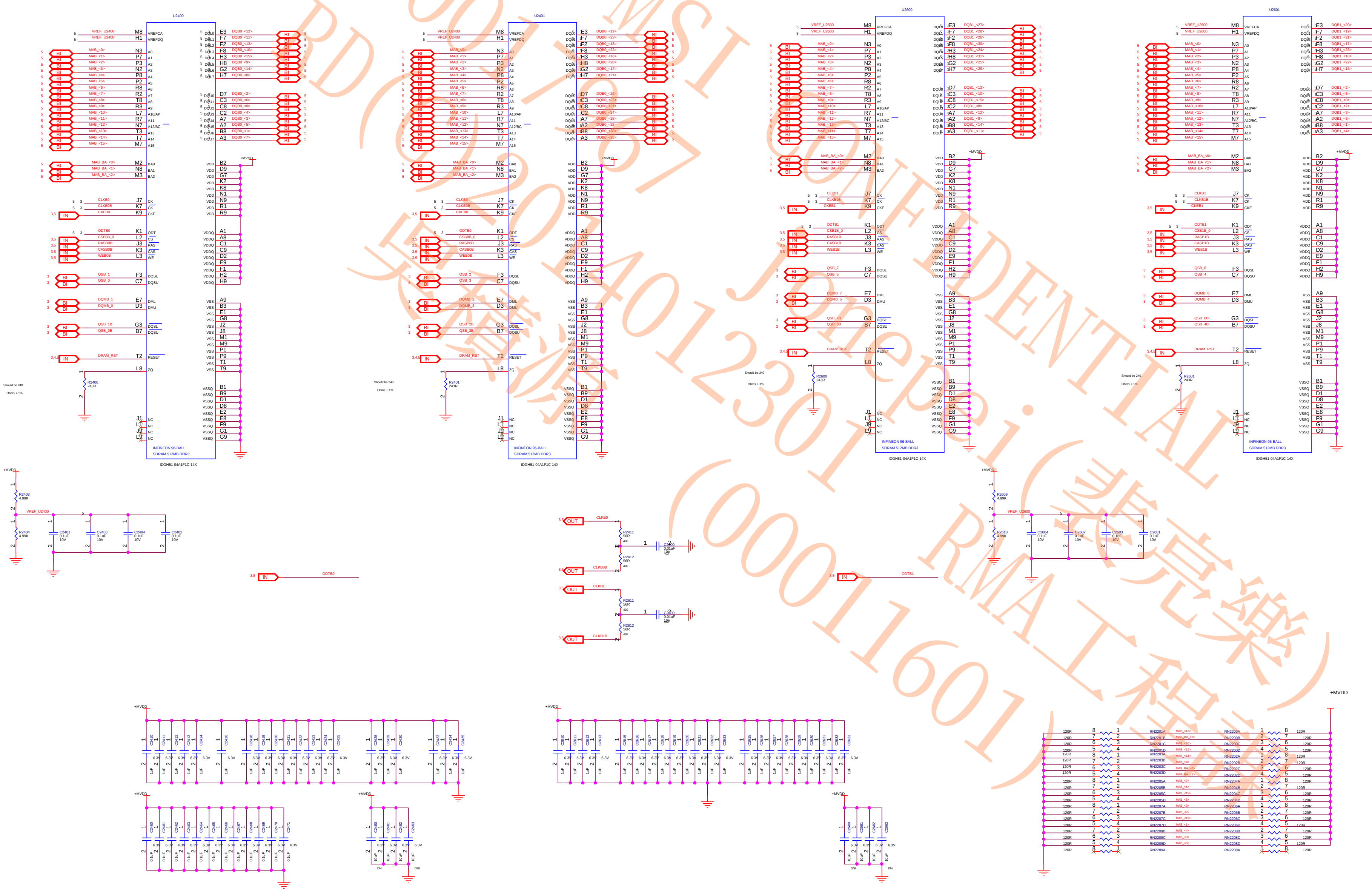
MICRO-STAR INT'L CO.,LTD

MS-V301

Size	Document Description	Rev
Custom	DDR3 CHA	1.1

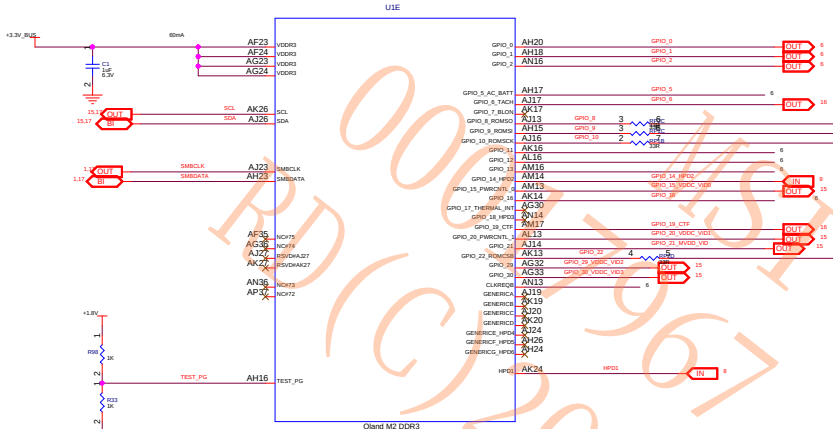
Date: Tuesday, August 06, 2013 Sheet 4 of 20

(5) DDR3 Memory Channel B

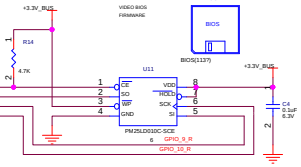


MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: DDR3 CHB	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 5 of 20	

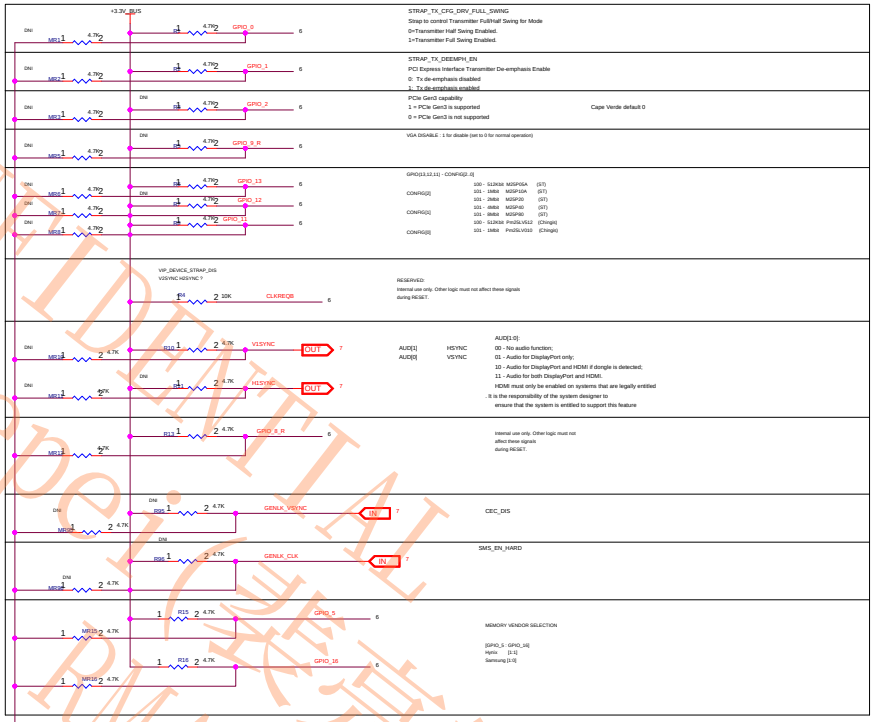
Oland XT M2 GPIOs Strap CF XTAL OSC

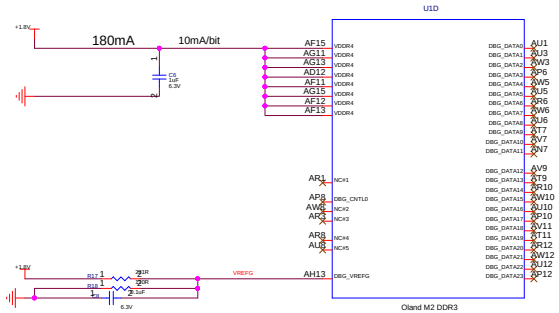


PN 2280007900G for 1Mbit (PM25LV010A-100SCE)



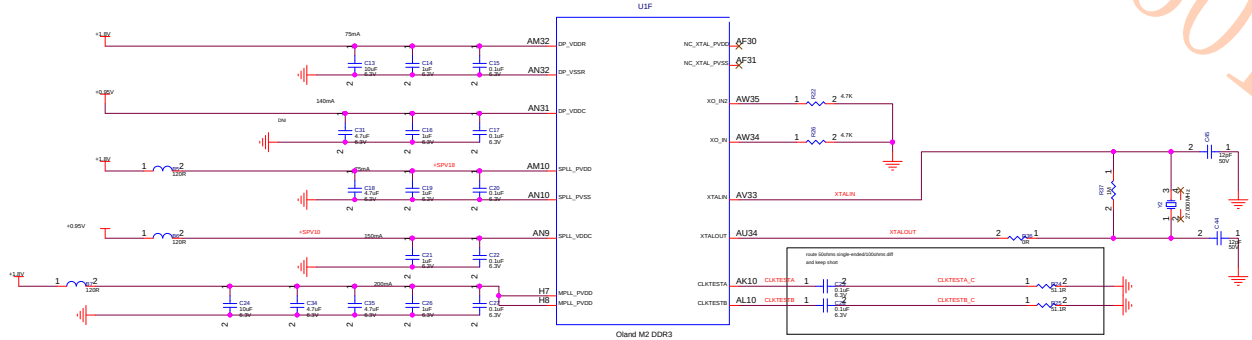
PIN BASED STRAPS



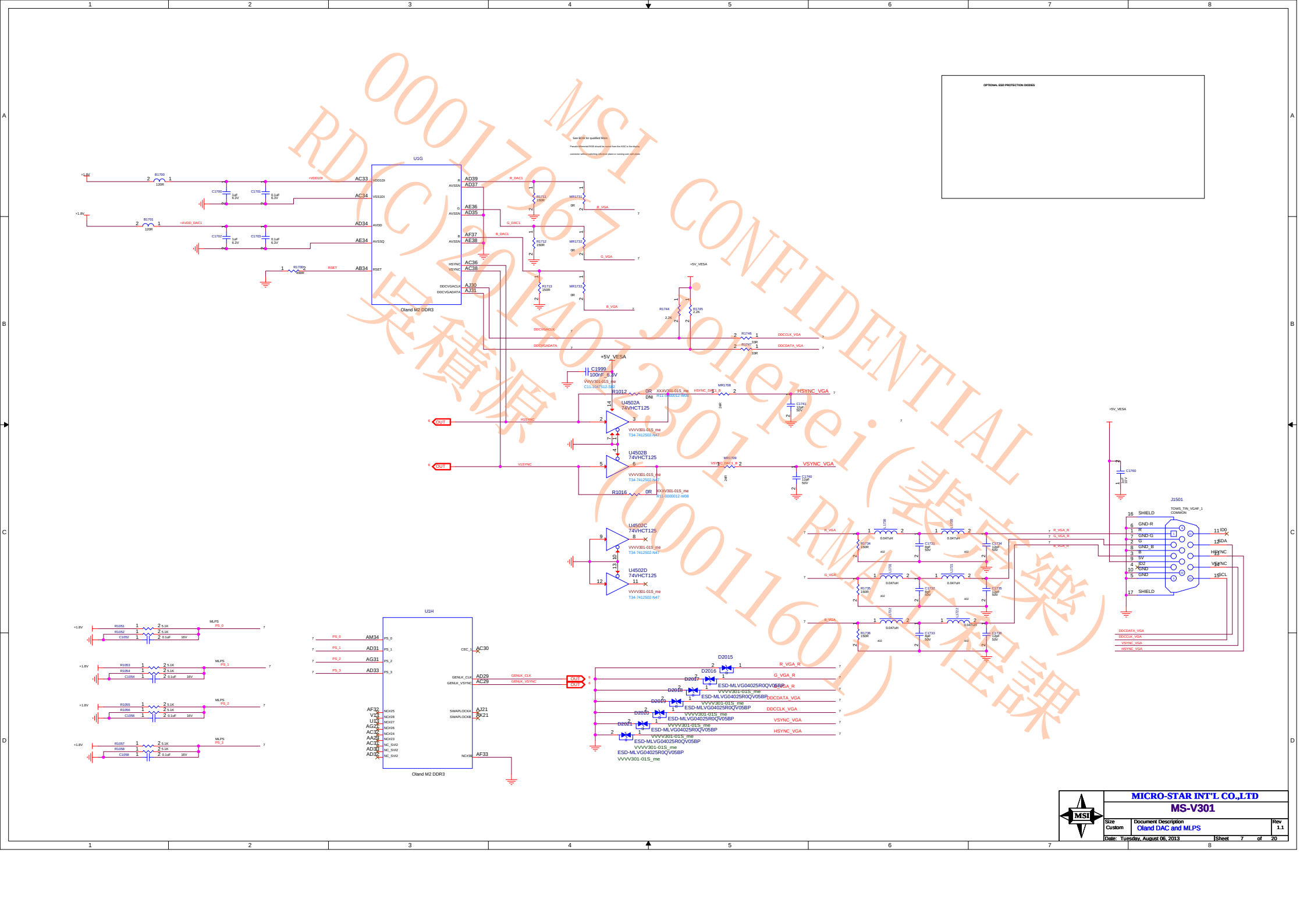


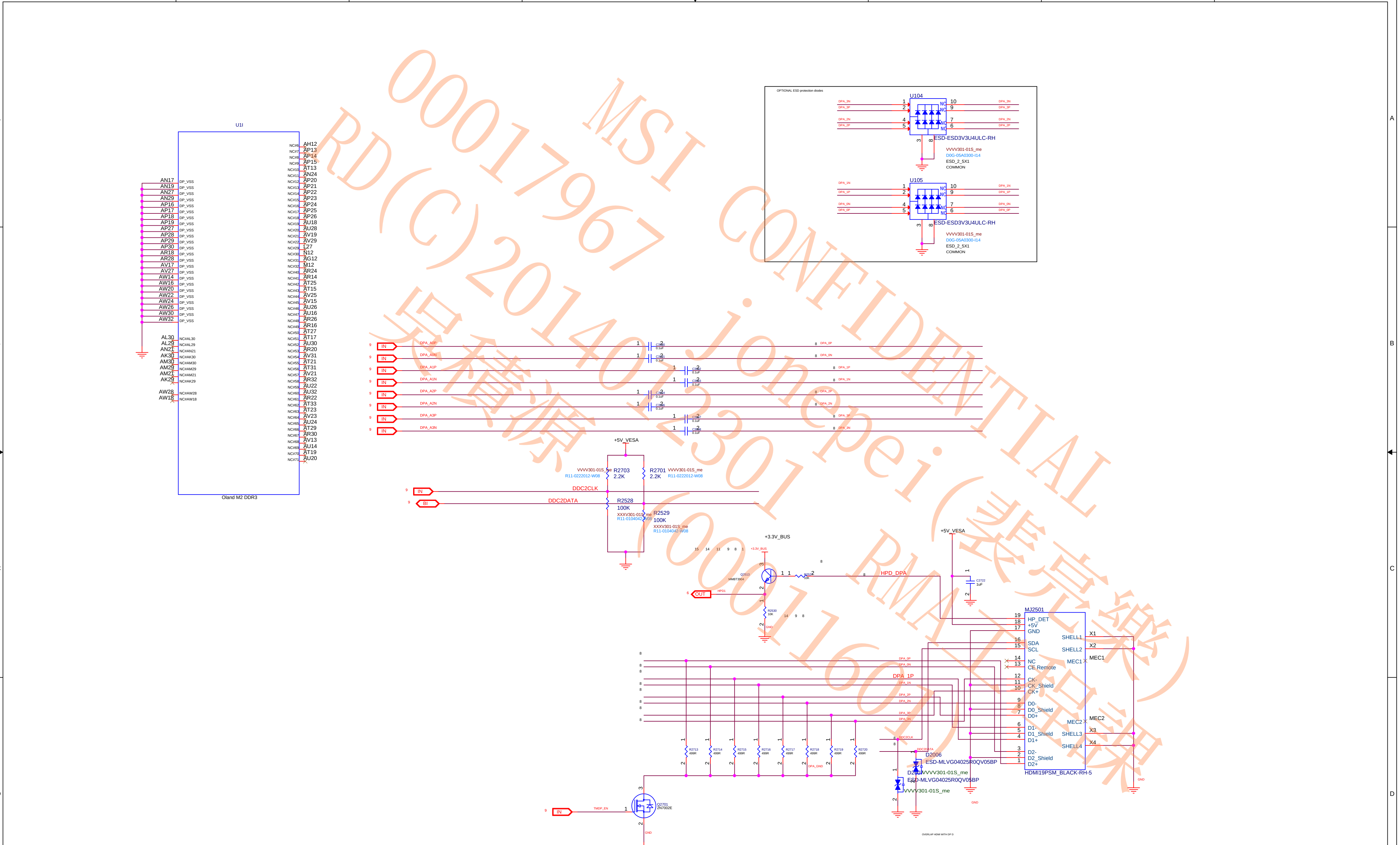
Place the crossfire
testpoints near the ASIC and
not the connector

Please pay attention to the grounding
strategies for these filter capacitors to
maintain a close loop for current.

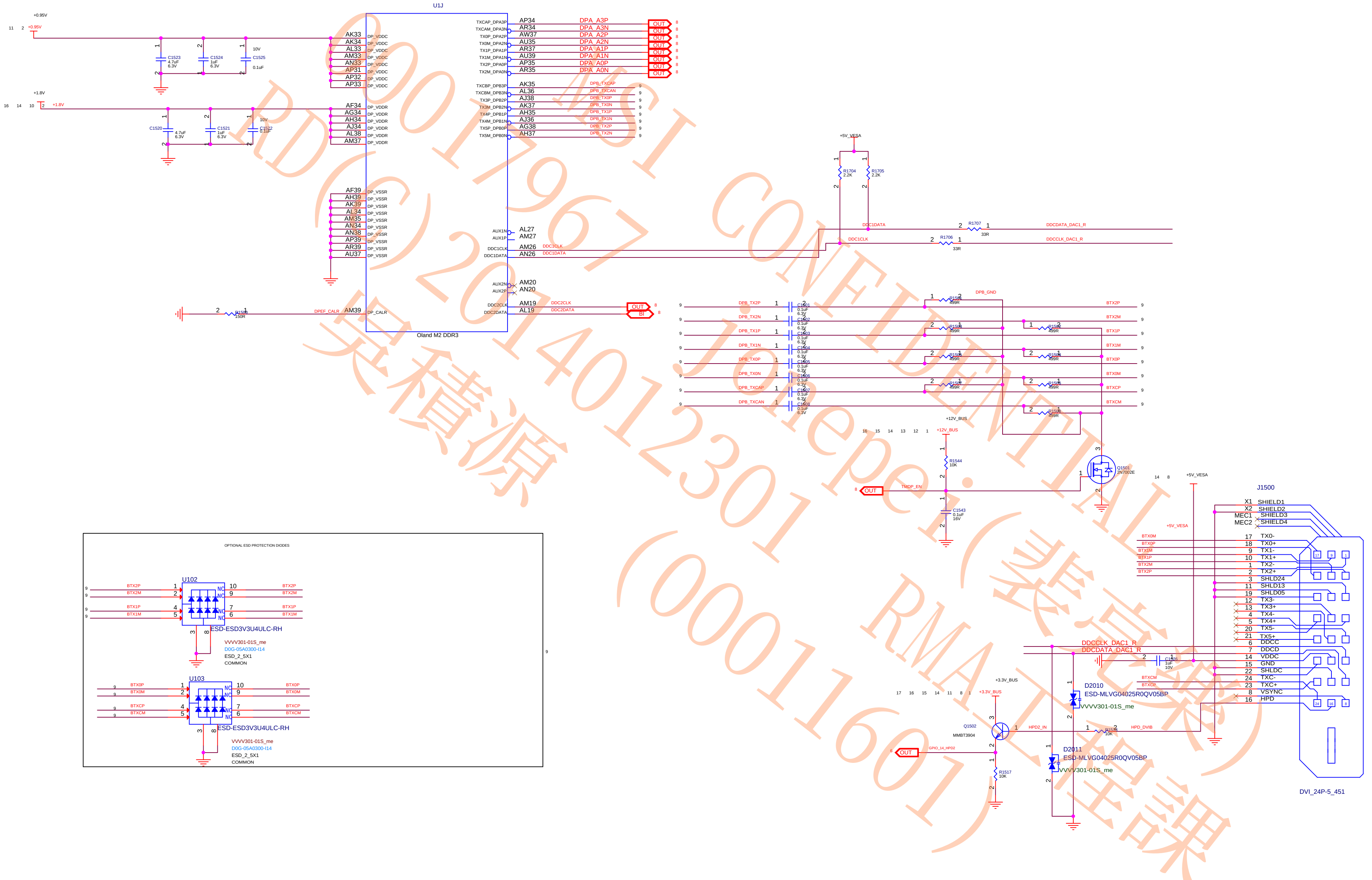


MICRO-STAR INT'L CO.,LTD			
MS-V301			
Size: Custom	Document Description: Oland GPIO STRAP PLL		Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 6 of 20		


OPTIONAL ESD PROTECTION DIODES
U1G
Oland M2 DDR3
U1H
Oland M2 DDR3
U4502A 74VHCT125
U4502B 74VHCT125
U4502C 74VHCT125
U4502D 74VHCT125
+5V_VESA
HSYNC_VGA
VSYNC_VGA
DDCCLK_VGA
DDCDATA_VGA
J1501
TOWS_TIN_VGAF_1
COMMON
ESD-MLVG04025R0QV05BP
MICRO-STAR INT'L CO.,LTD
MS-V301
Oland DAC and MLPS
Rev 1.1
Date: Tuesday, August 06, 2013
Sheet 7 of 20



MICRO-STAR INT'L CO.,LTD	
MS-V301	
Size: Custom	Document Description: Oland Connector HDMI/DP	Rev 1.1
Date: Tuesday, August 06, 2013	Sheet 8 of 20


U1J
Oland M2 DDR3
+0.95V
+1.8V
C1523 4.7uF 6.3V
C1524 1uF 6.3V
C1525 0.1uF 10V
C1520 4.7uF 6.3V
C1521 1uF 6.3V
C1522 0.1uF 10V
DP_VDDC
DP_VDDR
DP_VSSR
DP_CALR
DPEF_CALR
R1500 150R
DPA_A3P
DPA_A3N
DPA_A2P
DPA_A2N
DPA_A1P
DPA_A1N
DPA_A0P
DPA_A0N
DPB_TXCAP
DPB_TXCAN
DPB_TX0P
DPB_TX0N
DPB_TX1P
DPB_TX1N
DPB_TX2P
DPB_TX2N
DDC1CLK
DDC1DATA
DDC2CLK
DDC2DATA
+5V_VESA
R1704 2.2K
R1705 2.2K
R1707 33R
R1706 33R
DDCDATA_DAC1_R
DDCCLK_DAC1_R
DPB_GND
BTX2P
BTX2M
BTX1P
BTX1M
BTX0P
BTX0M
BTXCP
BTXCM
+12V_BUS
R1544 10K
C1543 0.1uF 16V
TMDP_EN
Q1501 2N7002E
J1500
SHIELD1
SHIELD2
SHIELD3
SHIELD4
TX0-
TX0+
TX1-
TX1+
TX2-
TX2+
SHLD24
SHLD13
SHLD05
TX3-
TX3+
TX4-
TX4+
TX5-
TX5+
DDCC
DDCD
VDDC
GND
SHLDC
TXC-
TXC+
VSYNC
HPD
DVI_24P-5_451
D2010 ESD-MLVG04025R0QV05BP
VVVV301-01S_me
D2011 ESD-MLVG04025R0QV05BP
+3.3V_BUS
Q1502 MMBT3904
HPD2_IN
HPD_DVIB
R1516 10K
R1517 10K
GPIO_14_HPD2
OPTIONAL ESD PROTECTION DIODES
U102
ESD-ESD3V3U4ULC-RH
D0G-05A0300-I14
ESD_2_5X1
COMMON
U103
ESD-ESD3V3U4ULC-RH
D0G-05A0300-I14
ESD_2_5X1
COMMON

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Size	Document Description	Rev
Custom	Oland TMDP sDVI	1.1

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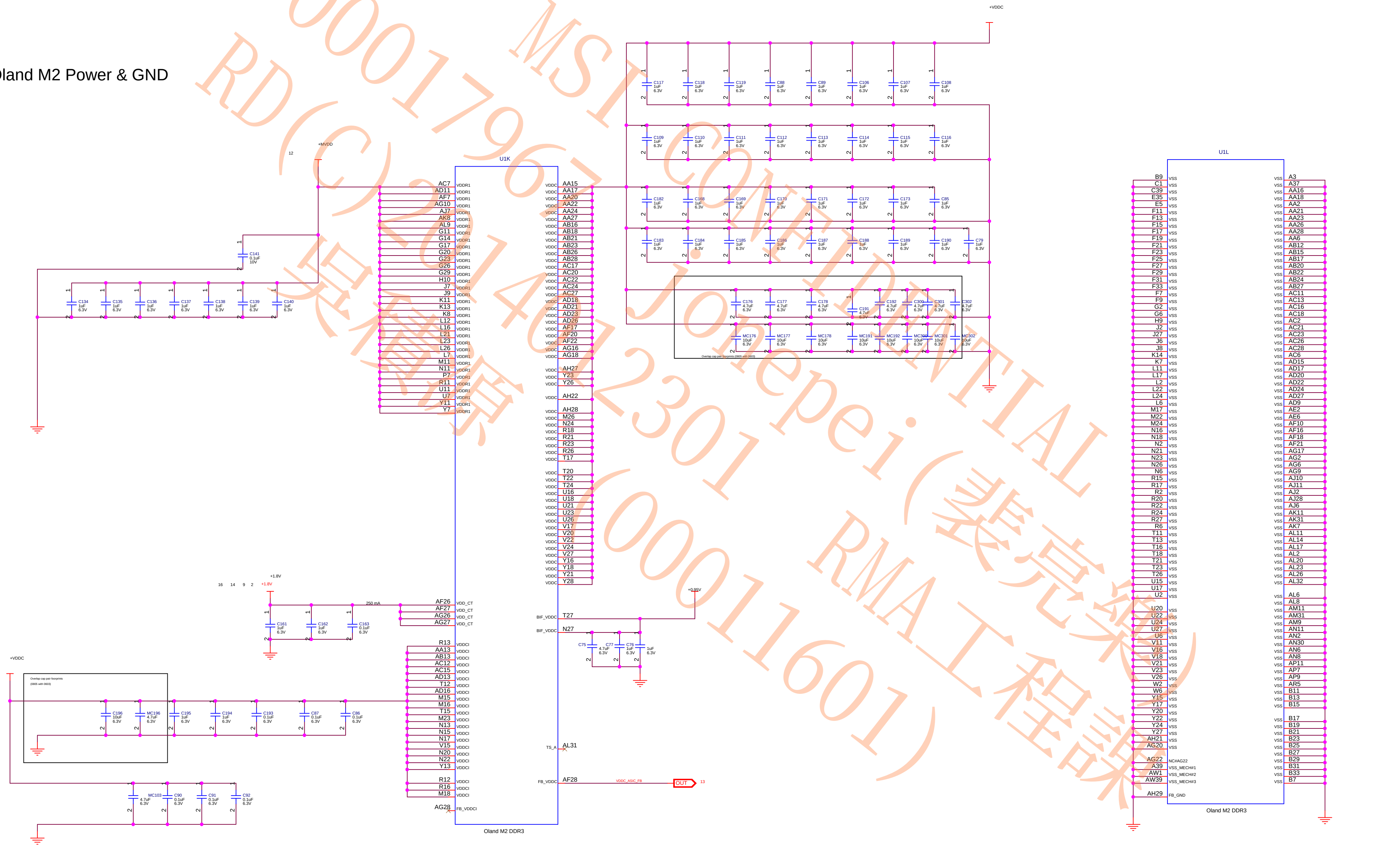
Oland M2 Power & GND

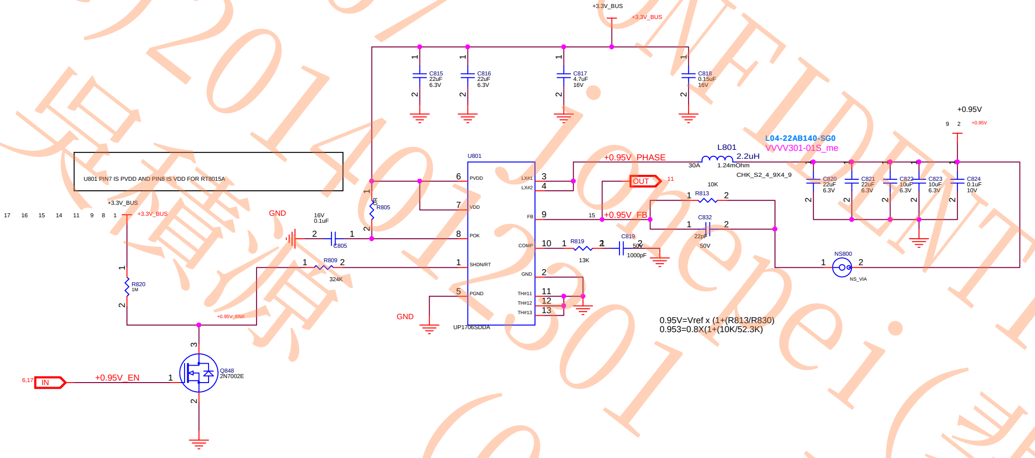


MICRO-STAR INT'L CO.,LTD

MS-V301

Size	Document Description	Rev
Custom	Oland Power&GND	1.1

Date: Tuesday, August 06, 2013 Sheet 10 of 20


+3.3V_BUS
C815 22uF 6.3V
C816 22uF 6.3V
C817 4.7uF 16V
C818 0.1uF 16V
+0.95V
L04-22AB140-SG0
VVVV301-015_me
L801 2.2uH
30A 1.24mOhm
CHK_S2_4_9X4_9
+0.95V_PHASE
U801
PVDD
VDD
POK
SHDN/RT
PGND
LX#1
LX#2
FB
COMP
GND
THH1
THH2
THH3
UP1706SDDA
OUT
+0.95V_FB
R813 10K
C832 22pF 50V
R819 13K
C819 1000pF 50V
C820 22uF 6.3V
C821 22uF 6.3V
C822 10uF 6.3V
C823 10uF 6.3V
C824 0.1uF 10V
NS800
NS_VIA
U801 PIN7 IS PVDD AND PIN8 IS VDD FOR RT8015A
R805
C805 16V 0.1uF
GND
R809 324K
R820 1M
+0.95V_EN
IN
Q848 2N7002E
0.95V=Vref x (1+(R813/R830)
0.953=0.8X(1+(10K/52.3K)

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Size	Document Description	Rev
Custom	0.95V	1.1

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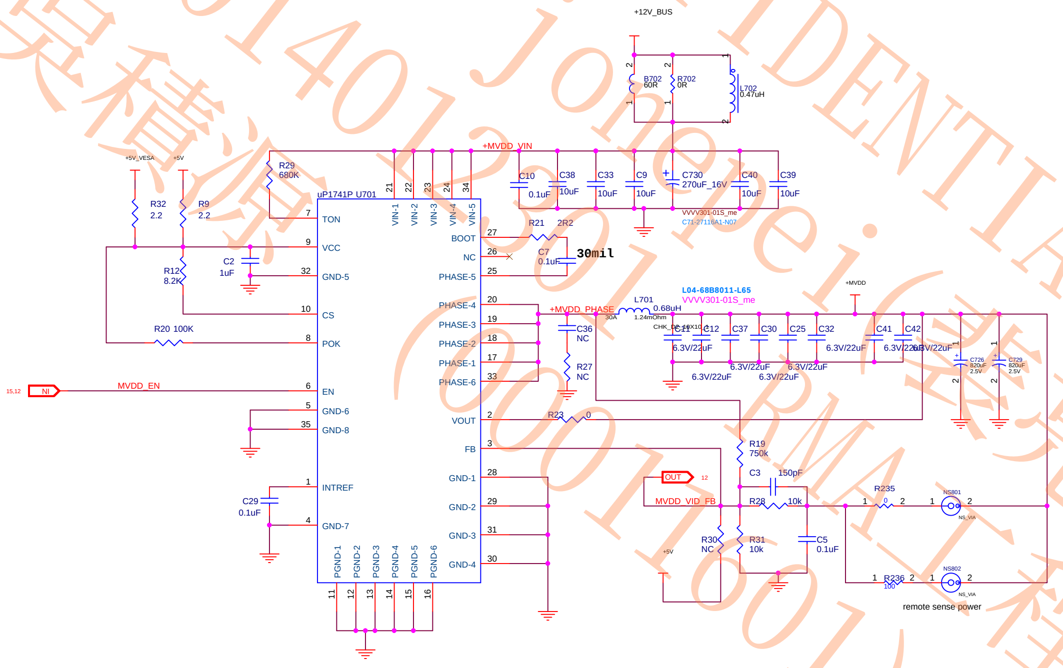
MVDD



+12V_BUS
R702 0R
L702 0.47uH
+MVDD_VIN
C10 0.1uF
C38 10uF
C33 10uF
C9 10uF
C730 270uF_16V
C40 10uF
C39 10uF
+5V_VESA
+5V
R32 2.2
R9 2.2
R29 680K
uP1741P U701
TON
VCC
GND-5
CS
POK
EN
GND-6
GND-8
INTREF
GND-7
VIN-1
VIN-2
VIN-3
VIN-4
VIN-5
BOOT
NC
PHASE-5
PHASE-4
PHASE-3
PHASE-2
PHASE-1
PHASE-6
VOUT
FB
GND-1
GND-2
GND-3
GND-4
PGND-1
PGND-2
PGND-3
PGND-4
PGND-5
PGND-6
R21 2R2
C7 0.1uF
30mil
C2 1uF
R12 8.2K
R20 100K
MVDD_EN
C29 0.1uF
+MVDD_PHASE
L701 0.68uH
C36 NC
R27 NC
L04-68B8011-L65
VVVV301-01S_me
C41
C42
C37
C30
C25
C32
6.3V/22uF
+MVDD
R23 0
R19 750k
C3 150pF
R28 10k
R235
OUT
MVDD_VID_FB
R30 NC
R31 10k
C5 0.1uF
R236
remote sense power

MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: MVDD	Rev: 1.1
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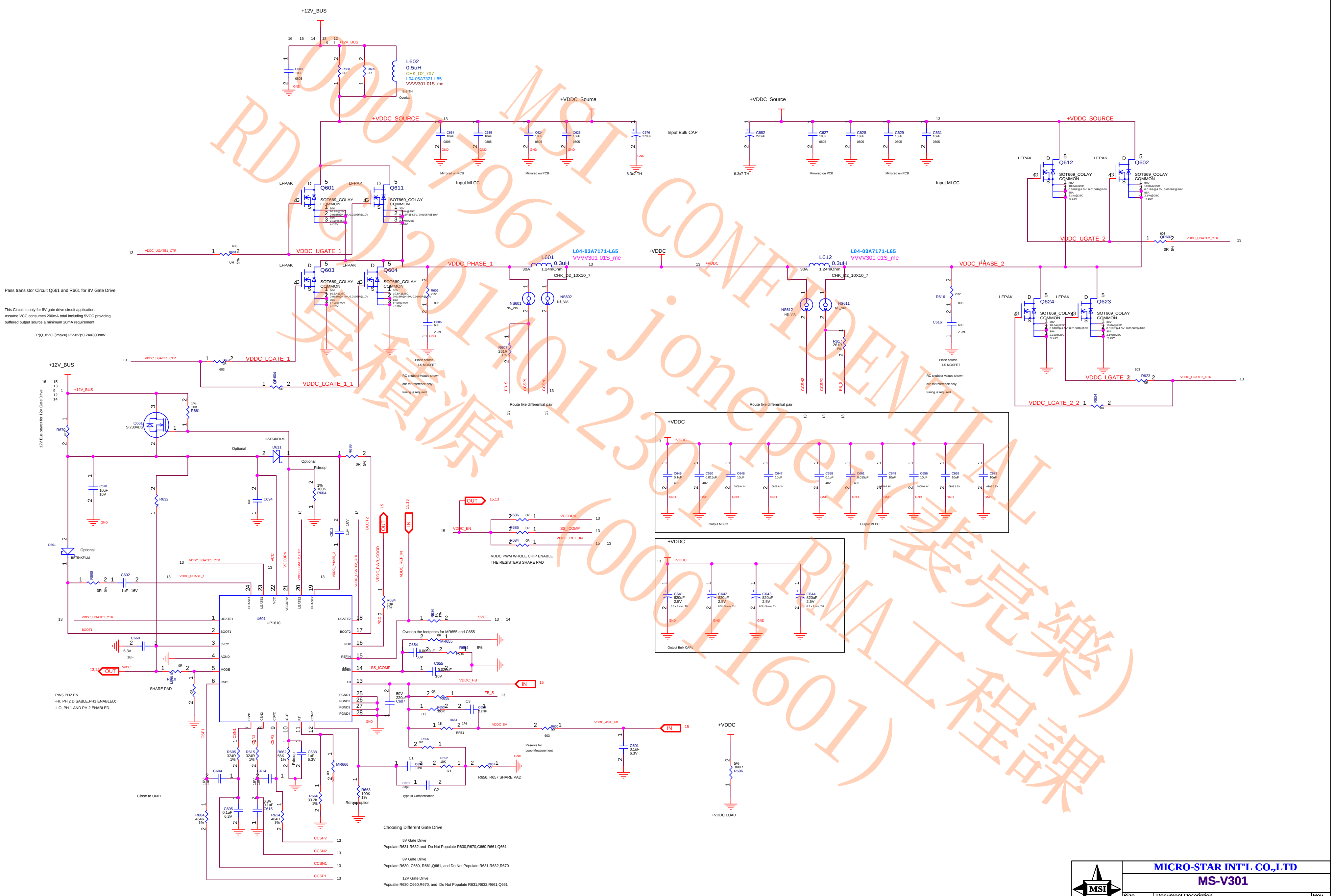
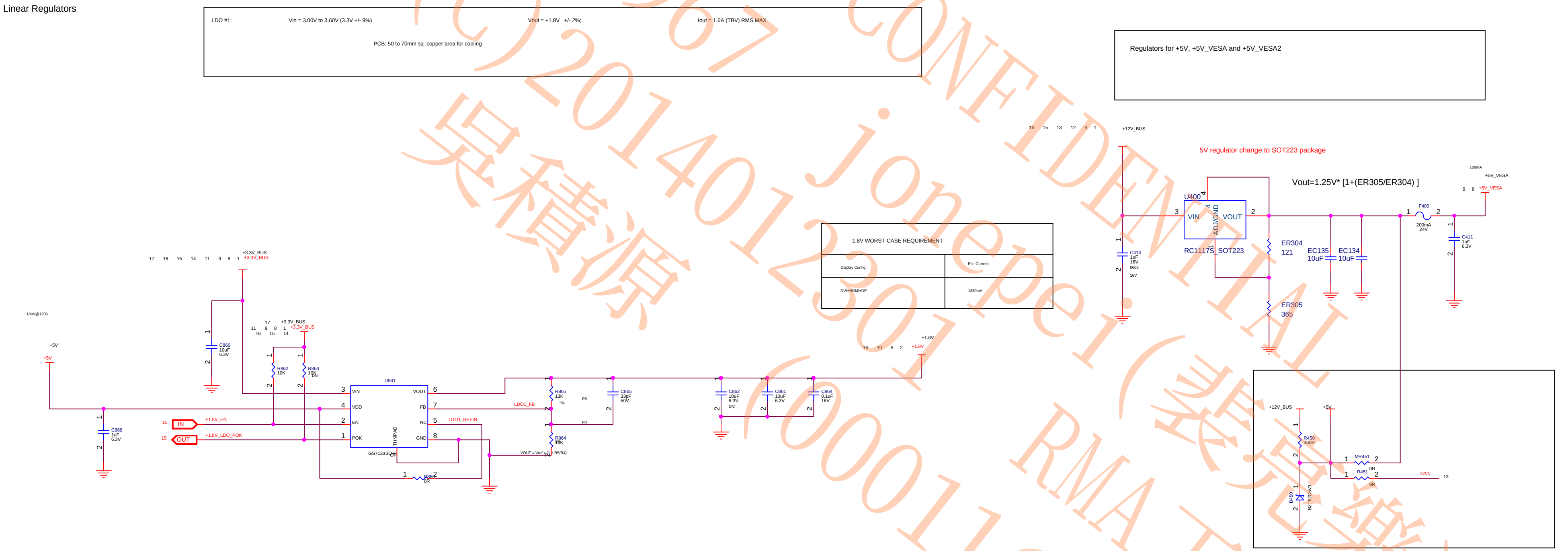
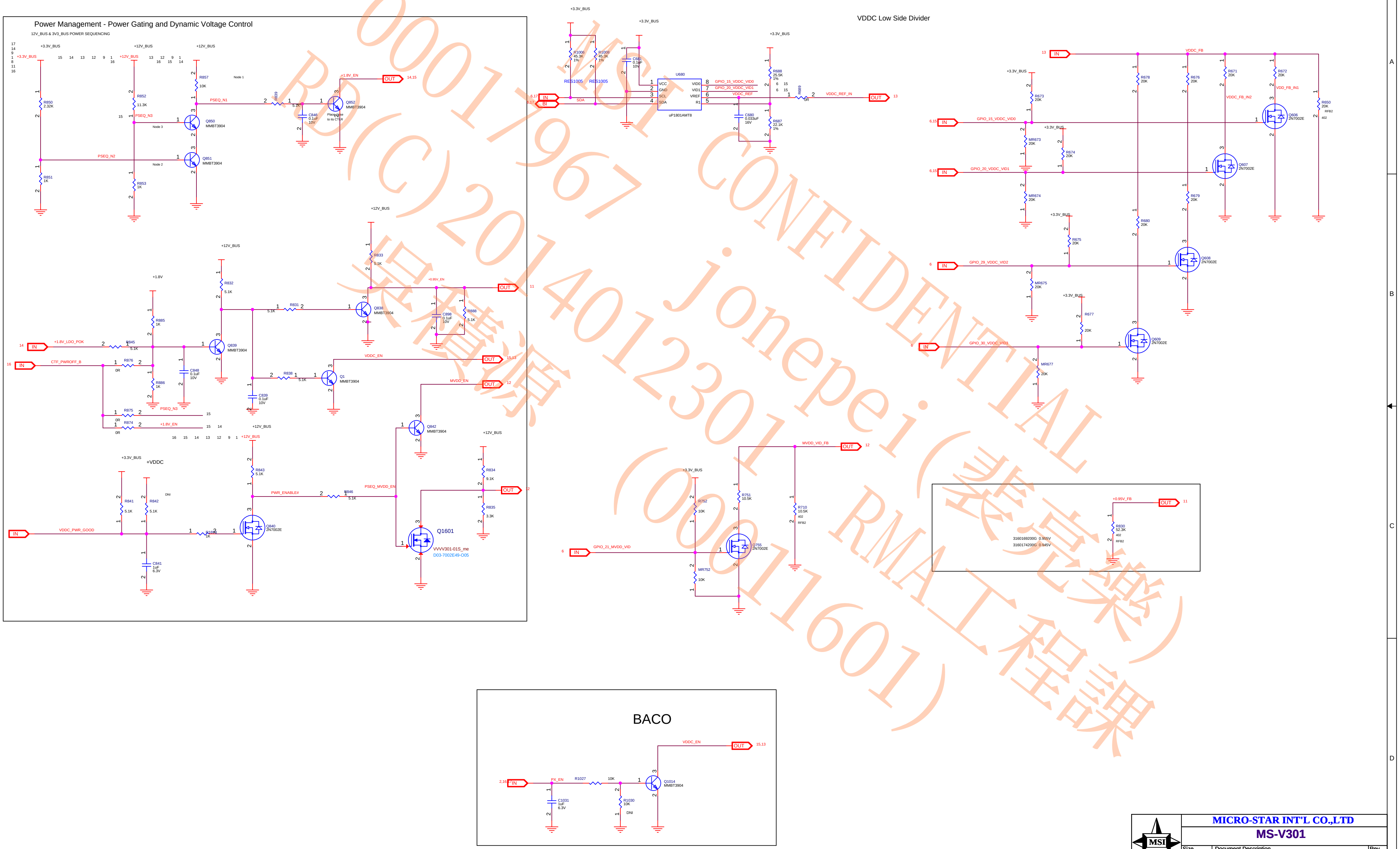

+12V_BUS
+VDDC_SOURCE
+VDDC_Source
Input Bulk CAP
Input MLCC
Mirrored on PCB
VDDC_UGATE_1
VDDC_PHASE_1
VDDC_LGATE_1
VDDC_UGATE_2
VDDC_PHASE_2
VDDC_LGATE_2
L601 0.3uH
L612 0.3uH
L04-03A7171-L65
VVVV301-01S_me
CHK_D2_10X10_7
L602 0.5uH
CHK_D2_7X7
L04-05A7321-L65
Pass transistor Circuit Q661 and R661 for 8V Gate Drive
This Circuit is only for 8V gate drive circuit application.
Assume VCC consumes 200mA total including 5VCC providing
buffered output source a minimum 20mA requirement
P(Q_8VCC)max=(12V-8V)*0.2A=800mW
12V Bus power for 12V Gate Drive
Place across LS MOSFET
RC snubber values shown are for reference only, tuning is required
Route like differential pair
Output MLCC
Output Bulk CAPs
VDDC PWM WHOLE CHIP ENABLE
THE RESISTERS SHARE PAD
U601
UP1610
Overlap the footprints for MR655 and C655
PIN5 PH2 EN
-HI, PH 2 DISABLE,PH1 ENABLED;
-LO, PH 1 AND PH 2 ENABLED.
SHARE PAD
Close to U601
Reserve for Loop Measurement
R656, R657 SHARE PAD
Type III Compensation
Rdroop option
+VDDC LOAD
Choosing Different Gate Drive
5V Gate Drive
Populate R631,R632 and Do Not Populate R630,R670,C660,R661,Q661
8V Gate Drive
Populate R630, C660, R661,Q661, and Do Not Populate R631,R632,R670
12V Gate Drive
Populate R630,C660,R670, and Do Not Populate R631,R632,R661,Q661

MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: VDDC	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 13 of 20	


Linear Regulators
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling
Regulators for +5V, +5V_VESA and +5V_VESA2
1.8V WORST-CASE REQUIREMENT
Display Config
Est. Current
DVI+HDMI+DP
1330mA
5V regulator change to SOT223 package
Vout=1.25V* [1+(ER305/ER304)]
U400
VIN
VOUT
ADJ/GND
RC1117S_SOT223
ER304
121
ER305
365
EC135
10uF
EC134
10uF
F400
200mA
24V
C410
1uF
16V
C411
1uF
6.3V
+12V_BUS
+5V_VESA
+3.3V_BUS
+1.8V
+5V
U861
VIN
VOUT
VDD
FB
EN
NC
POK
GND
THMPAD
GS7133SO-R
LDO1_FB
LDO1_REFIN
+1.8V_EN
+1.8V_LDO_POK
IN
OUT
R862
10K
R863
10K
R865
13K
1%
R864
10K
C865
33pF
50V
C866
10uF
6.3V
C868
1uF
6.3V
C862
10uF
6.3V
C861
10uF
6.3V
C864
0.1uF
16V
VOUT = Vref x (1 + R5/R4)
R450
MR451
R451
0R
D450
SVCC

MICRO-STAR INT'L CO.,LTD		
MS-V301		
Size: Custom	Document Description: Linear Regulators	Rev: 1.1
Date: Tuesday, August 06, 2013	Sheet 14 of 20	


Power Management - Power Gating and Dynamic Voltage Control
12V_BUS & 3V3_BUS POWER SEQUENCING
VDDC Low Side Divider
BACO
uP1801AMT8
Q1601
VVV301-01S_me
D03-7002E49-O05
+3.3V_BUS
+12V_BUS
+1.8V
+VDDC
PSEQ_N1
PSEQ_N2
PSEQ_N3
+1.8V_EN
+1.8V_LDO_POK
CTF_PWROFF_B
VDDC_EN
MVDD_EN
+0.95V_EN
PWR_ENABLE#
PSEQ_MVDD_EN
VDDC_PWR_GOOD
GPIO_15_VDDC_VID0
GPIO_20_VDDC_VID1
GPIO_29_VDDC_VID2
GPIO_30_VDDC_VID3
VDDC_REF
VDDC_REF_IN
VDDC_FB
VDDC_FB_IN1
VDDC_FB_IN2
MVDD_VID_FB
GPIO_21_MVDD_VID
+0.95V_FB
PX_EN
316016920OG 0.955V
316017420OG 0.945V

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Size	Document Description	Rev
Custom	PWR MGMT & SEQ	1.1

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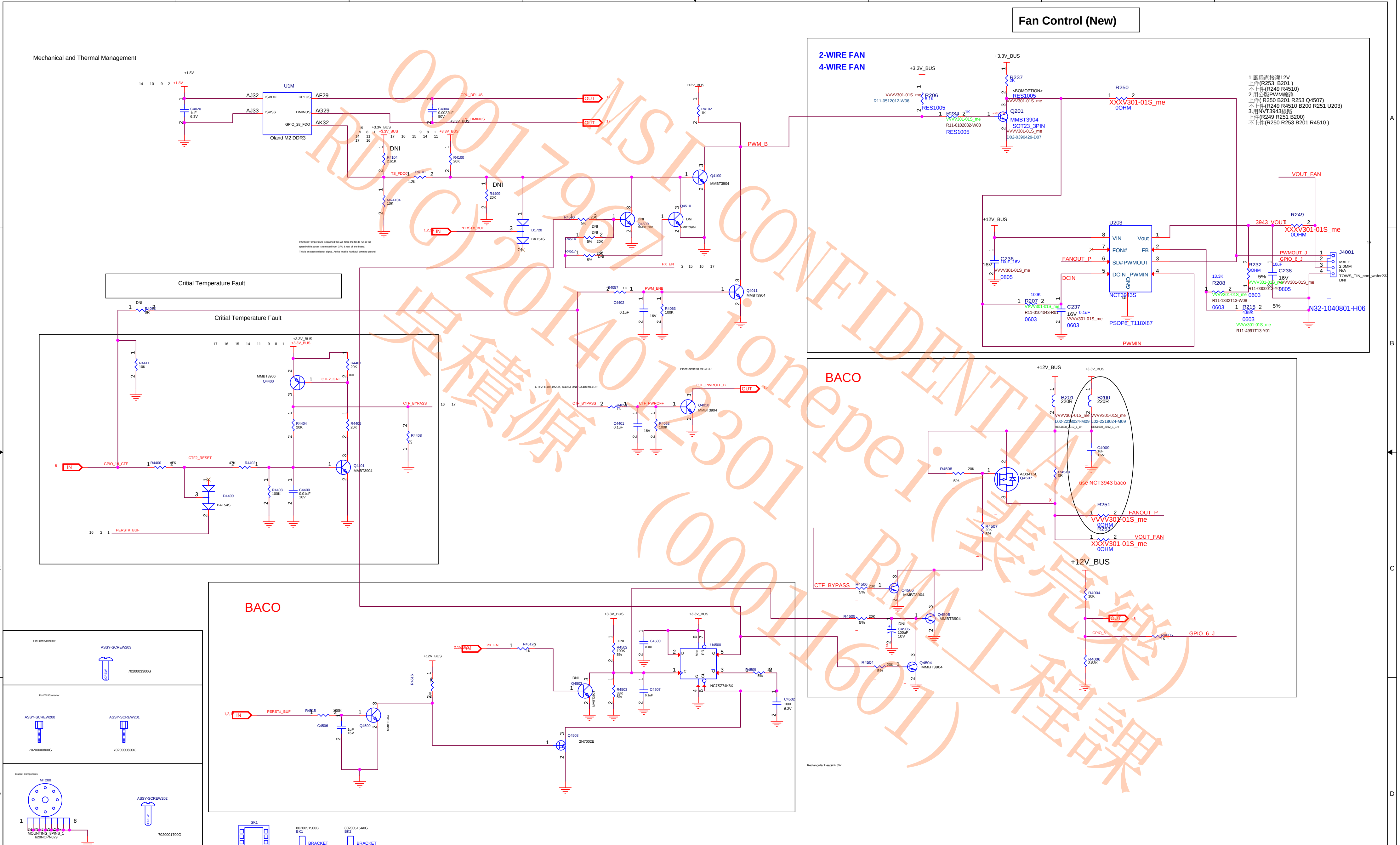

MICRO-STAR INT'L CO.,LTD

MS-V301

Size	Document Description	Rev
Custom	Mech/Thermal Management	1.1

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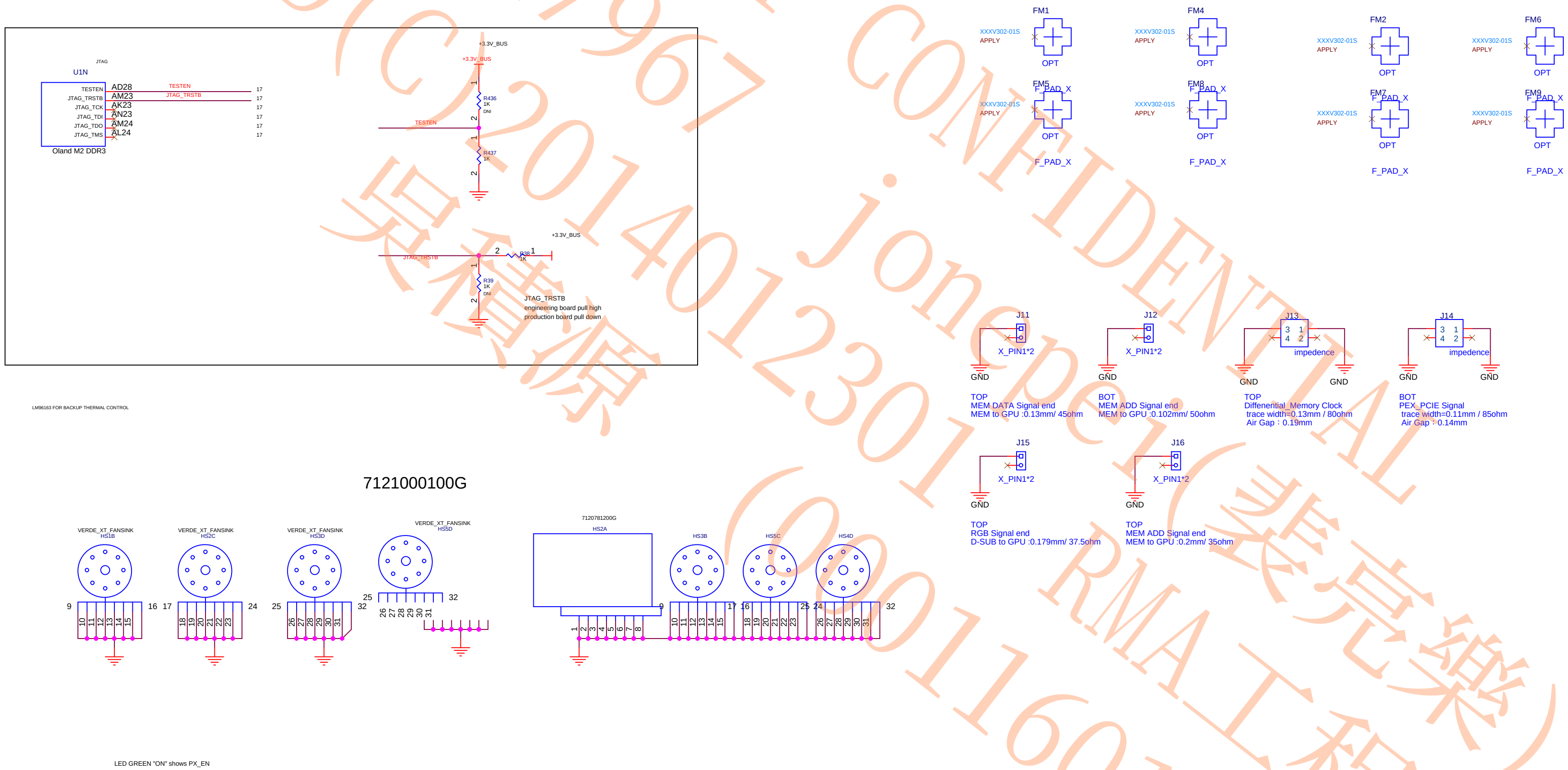
(19) Debug Circuits


JTAG
U1N
TESTEN AD28
JTAG_TRSTB AM23
JTAG_TCK AK23
JTAG_TDI AN23
JTAG_TDO AM24
JTAG_TMS AL24
Oland M2 DDR3
TESTEN
JTAG_TRSTB
+3.3V_BUS
R436 1K DNI
R437 1K
R38 1K
R39 1K DNI
JTAG_TRSTB
engineering board pull high
production board pull down
LM96163 FOR BACKUP THERMAL CONTROL
7121000100G
VERDE_XT_FANSINK HS1B
VERDE_XT_FANSINK HS2C
VERDE_XT_FANSINK HS3D
VERDE_XT_FANSINK HS5D
7120781200G HS2A
HS3B
HS5C
HS4D
LED GREEN "ON" shows PX_EN
FM1 FM4 FM2 FM6
FM5 FM8 FM7 FM9
XXXV302-01S
APPLY
OPT
F_PAD_X
J11 X_PIN1*2 GND
TOP
MEM DATA Signal end
MEM to GPU :0.13mm/ 45ohm
J12 X_PIN1*2 GND
BOT
MEM ADD Signal end
MEM to GPU :0.102mm/ 50ohm
J13 impedence GND
TOP
Differential_Memory Clock
trace width=0.13mm / 80ohm
Air Gap : 0.19mm
J14 impedence GND
BOT
PEX_PCIE Signal
trace width=0.11mm / 85ohm
Air Gap : 0.14mm
J15 X_PIN1*2 GND
TOP
RGB Signal end
D-SUB to GPU :0.179mm/ 37.5ohm
J16 X_PIN1*2 GND
TOP
MEM ADD Signal end
MEM to GPU :0.2mm/ 35ohm

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Size	Document Description	Rev
Custom	Debug Circuit	1.1

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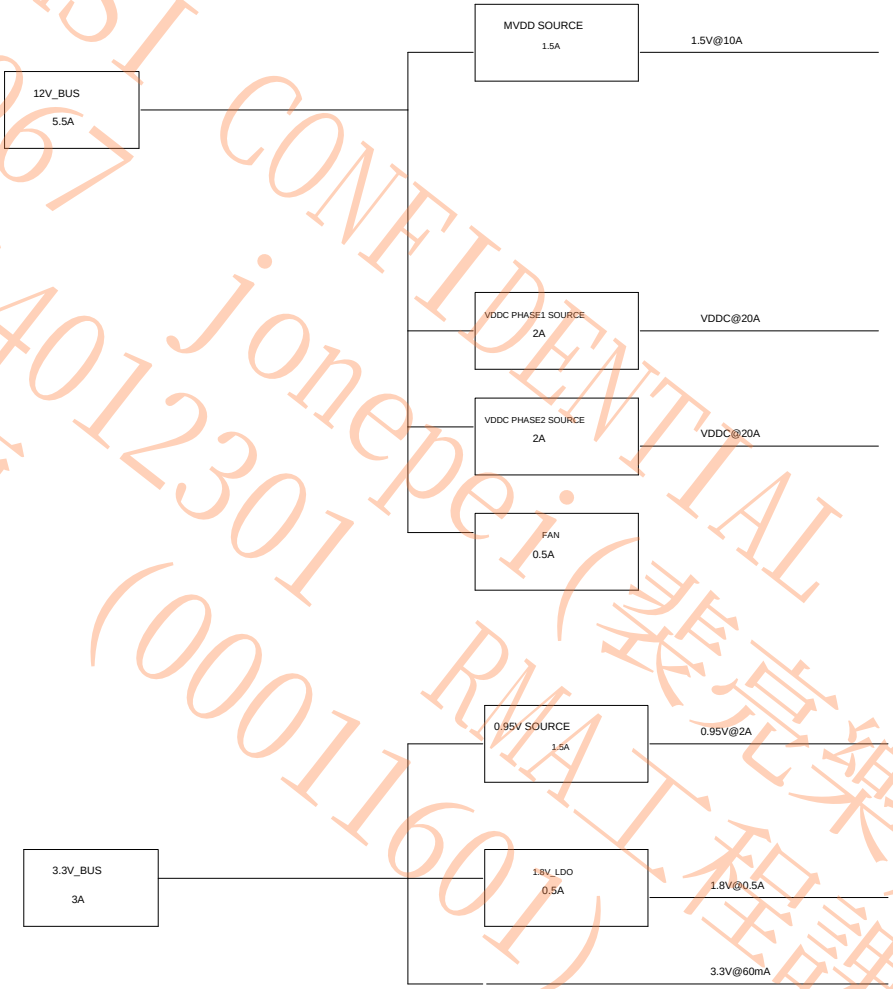
DVI-I	HPD2	DDC/AUX1
HDMI/DP	HPD1	DDC/AUX2

GPIO15	VDDC_VID0	
GPIO20	VDDC_VID1	
GPIO29	VDDC_VID2	
GPIO30	VDDC_VID3	
GPIO21	MVDD_VID	



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	GPIO DDC HPD map	1.1

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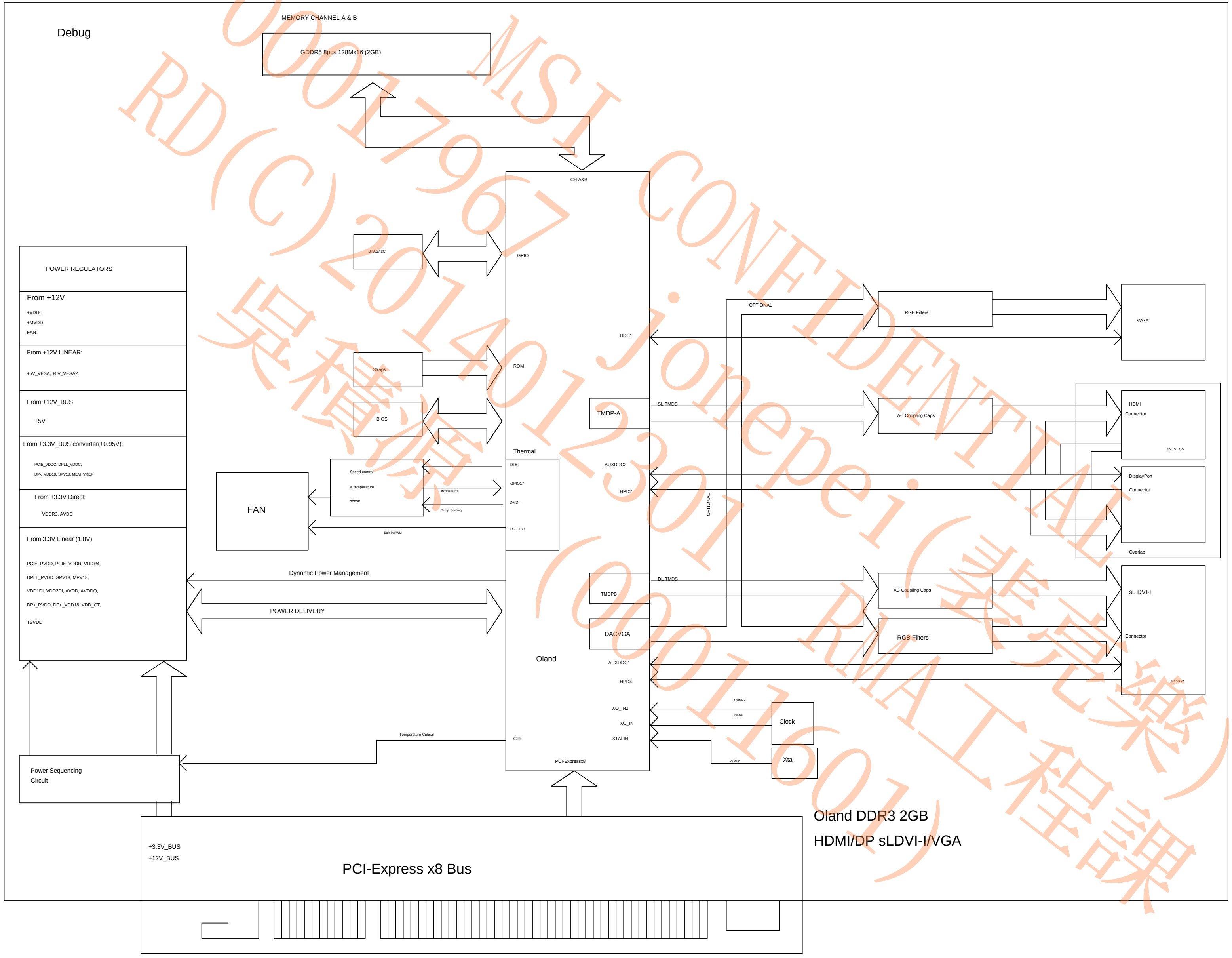
Debug
MEMORY CHANNEL A & B
GDDR5 8pcs 128Mx16 (2GB)
CH A&B
JTAG/I2C
GPIO
POWER REGULATORS
From +12V
+VDDC
+MVDD
FAN
From +12V LINEAR:
+5V_VESA, +5V_VESA2
From +12V_BUS
+5V
From +3.3V_BUS converter(+0.95V):
PCIE_VDDC, DPLL_VDDC,
DPx_VDD10, SPV10, MEM_VREF
From +3.3V Direct:
VDDR3, AVDD
From 3.3V Linear (1.8V)
PCIE_PVDD, PCIE_VDDR, VDDR4,
DPLL_PVDD, SPV18, MPV18,
VDD1DI, VDD2DI, AVDD, AVDDQ,
DPx_PVDD, DPx_VDD18, VDD_CT,
TSVDD
Straps
ROM
BIOS
FAN
Speed control
& temperature
sense
INTERRUPT
Temp. Sensing
Built-in PWM
Thermal
DDC
GPIO17
D+D-
TS_FDO
Dynamic Power Management
POWER DELIVERY
Temperature Critical
CTF
Oland
PCI-Expressx8
Power Sequencing
Circuit
DDC1
TMDP-A
SL TMDS
AUXDDC2
HPD2
OPTIONAL
TMDPB
DL TMDS
DACVGA
AUXDDC1
HPD4
XO_IN2
XO_IN
XTALIN
100MHz
27MHz
Clock
Xtal
RGB Filters
sVGA
AC Coupling Caps
HDMI
Connector
5V_VESA
DisplayPort
Connector
Overlap
AC Coupling Caps
RGB Filters
sL DVI-I
Connector
5V_VESA
+3.3V_BUS
+12V_BUS
PCI-Express x8 Bus
Oland DDR3 2GB
HDMI/DP sLDVI-I/VGA

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MS-V301		
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TITLE	SCHEMATIC NO.	DATE
Oland xto DDR3 2GB SL_DVI-I+HDMI/DP+sVGA	105-C662XX-00	

REVISION HISTORY

NOTE:
THIS SCHEMATIC REPRESENTS THE PCB, IT DOES NOT REPRESENT ANY SPECIFIC SKU.
FOR STUFFING OPTIONS (COMPONENT VALUES, DNI PLEASE CONSULT THE PRODUCT SPECIFIC BOM.
PLEASE CONTACT AMD REPRESENTATIVE TO OBTAIN LASTEST BOM CLOSEST TO THE APPLICATION DESIRED.

REV P00

SCH REV	PCB REV	DATE	REVISION DESCRIPTION
00	00A	2012/08/20	Initial Oland XT schematic based on C552 C550&C469
00	00	2013/03/27	Upgrade PCB to 00 without Schematic change
01			
		2013/07/02	1. Page 03~05 : Add <> in memory DQA_ 2. Page 07: chagne connector to black type 3. Page 08: remove DP & add ESD 4. Page 09 : add ESD 5. Page 11 : U801 change to UP1706 6. Page 12 : U701 change to UP1741P 7. Page 13 : U601 change to UP1610 8. Page 15 : add MVDD_EN circuit , add SCL SDA pull high R 9. Page 16 : add NCT3943 in FAN control

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Size	Document Description	Rev
Custom	History	1.1

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