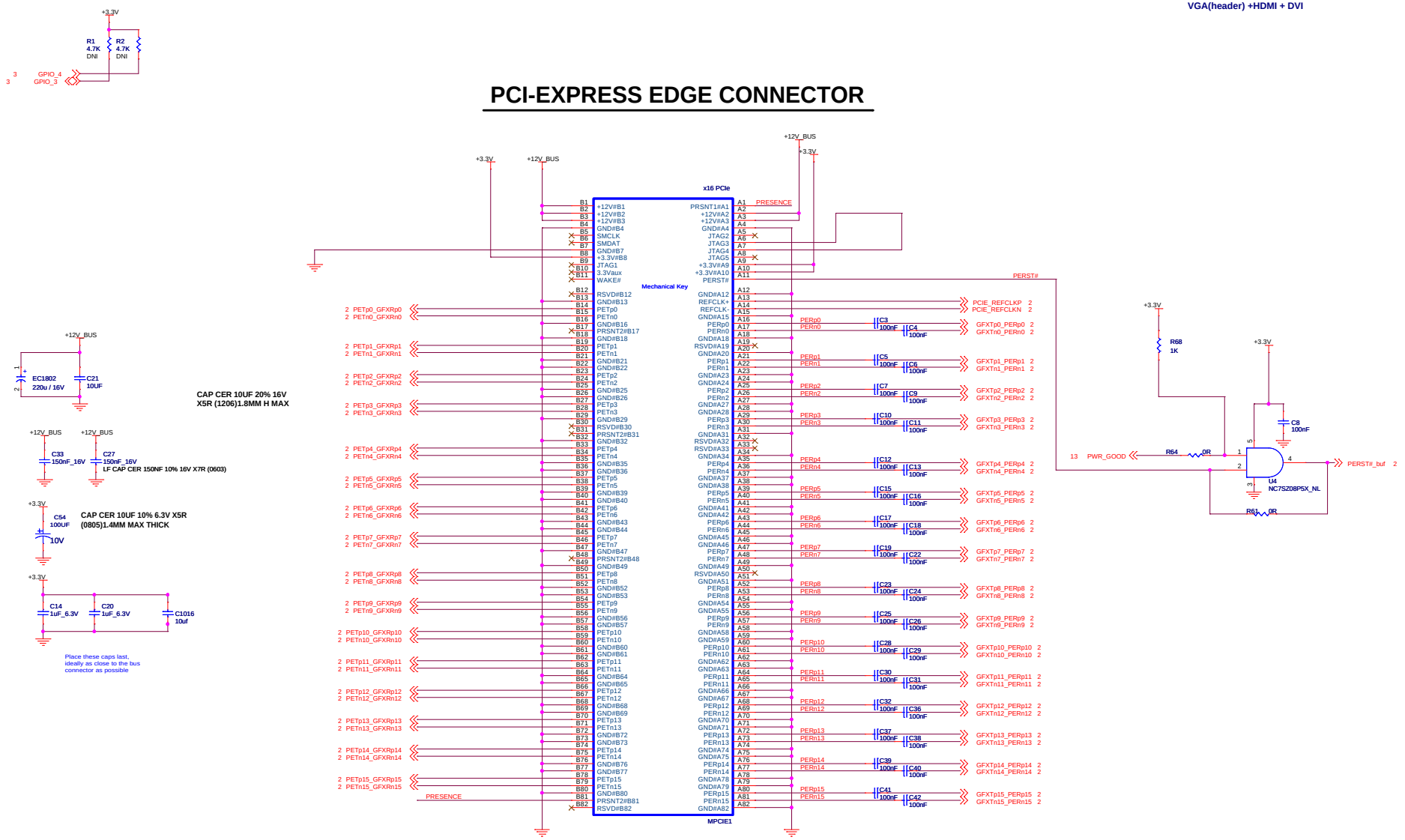
RV710 CLASH

VGA(header) +HDMI + DVI

PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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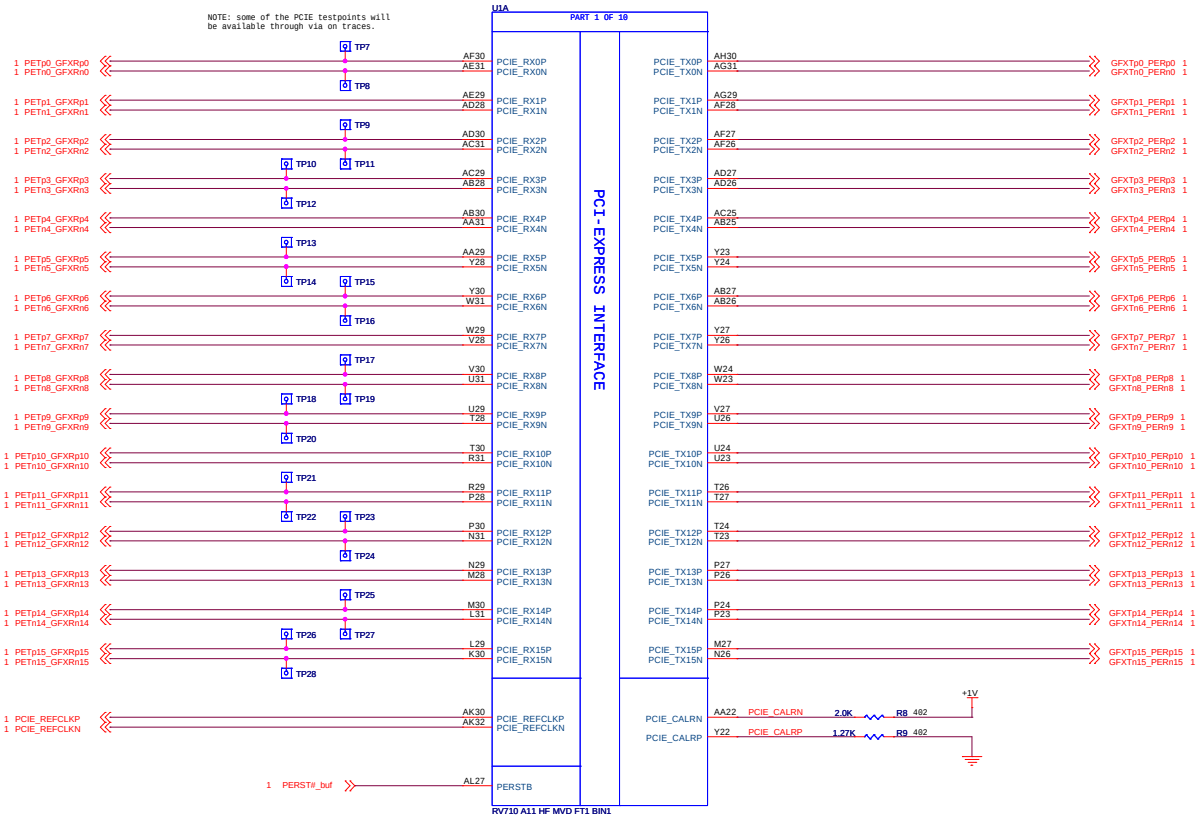
(2) RV710 PCIE Interface



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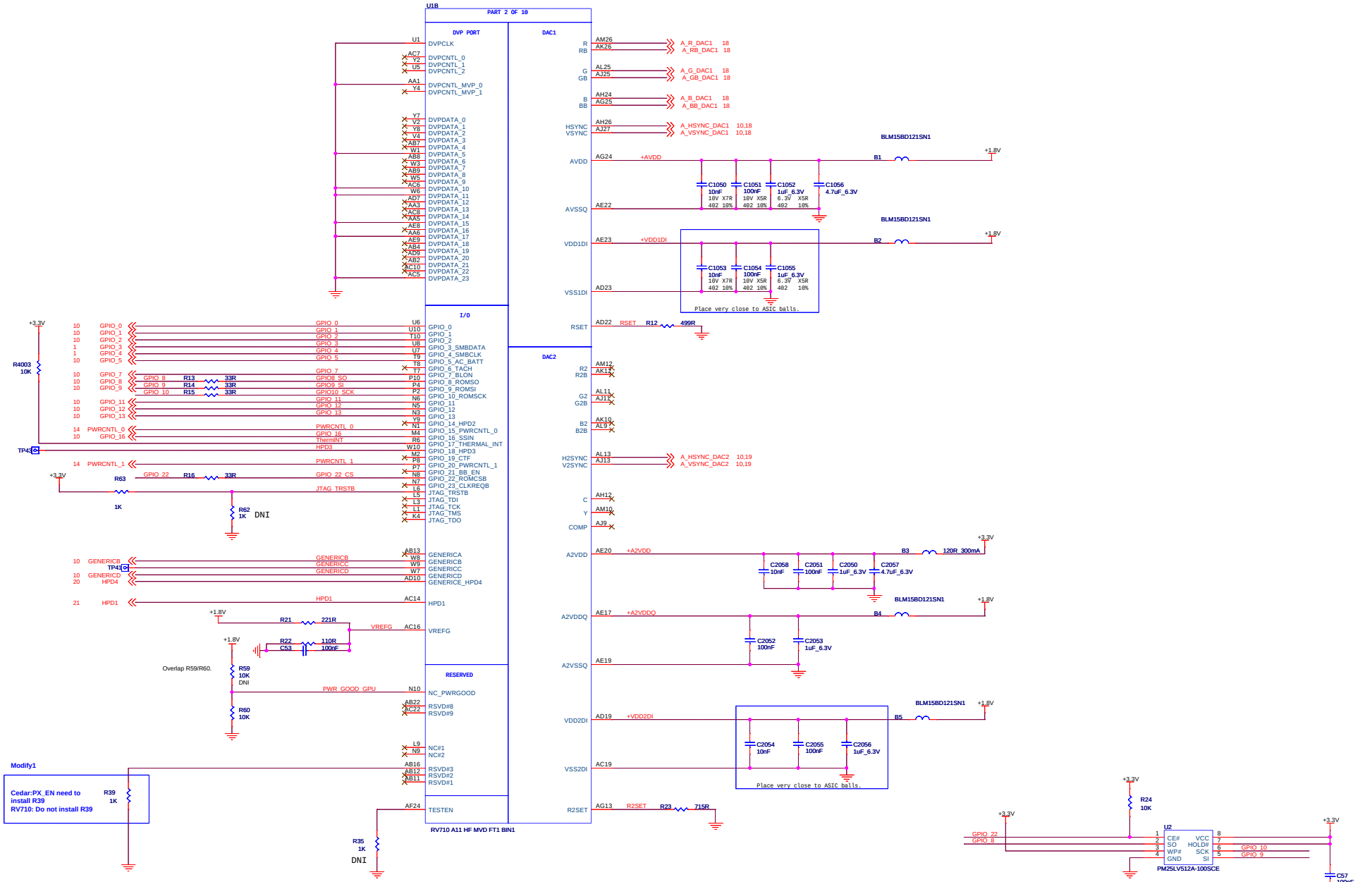
(3) RV710 Main



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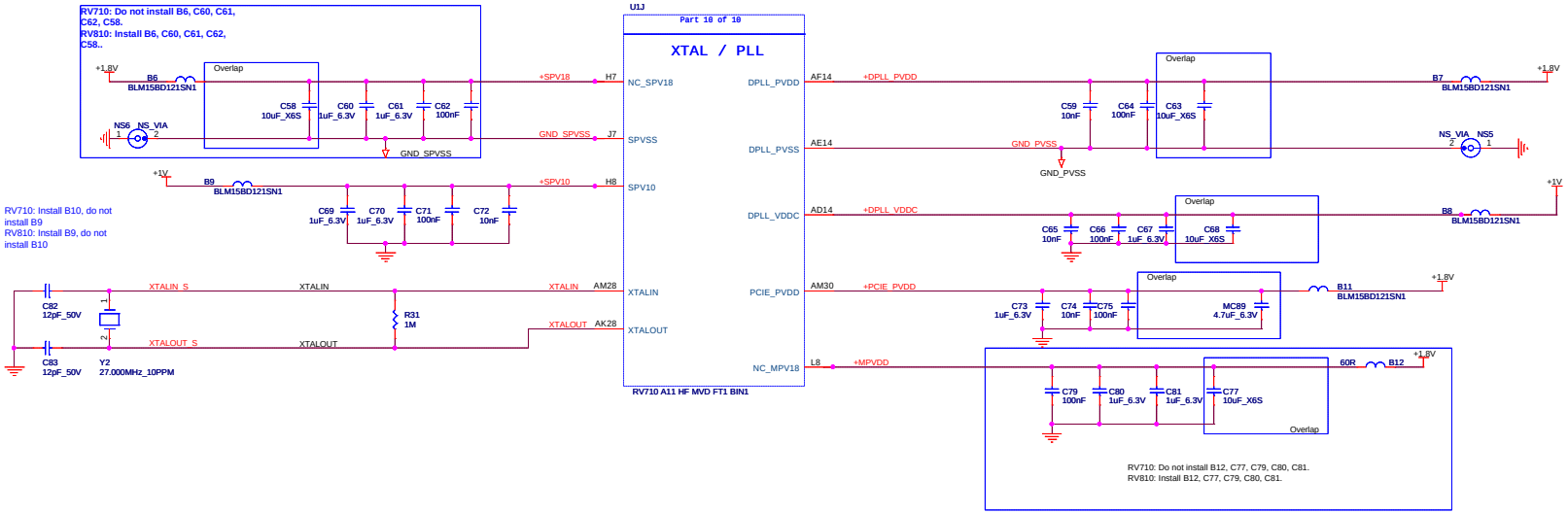
(04) RV710 GPIOs CF XTAL

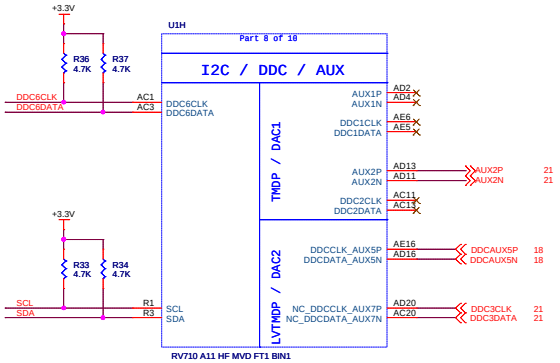


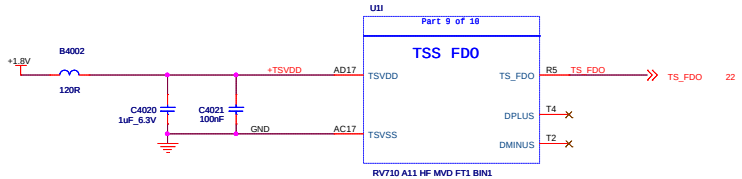
DDC6 BUS:

I2C Address	Function	Device
0x90	I2C VDDC Control	DS4402
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A





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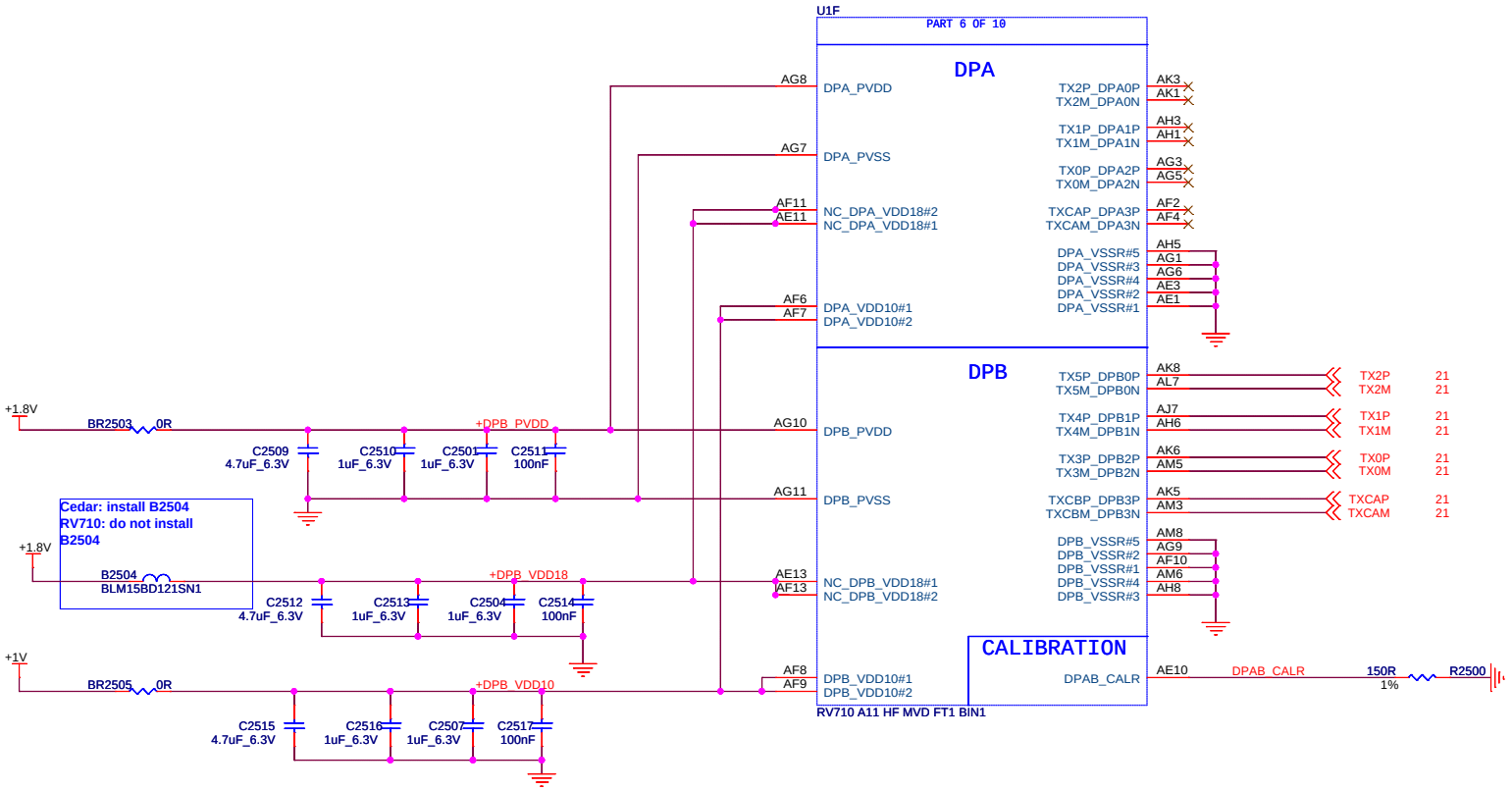
(05) RV710 TMDP A&B

TMDP INTERFACE



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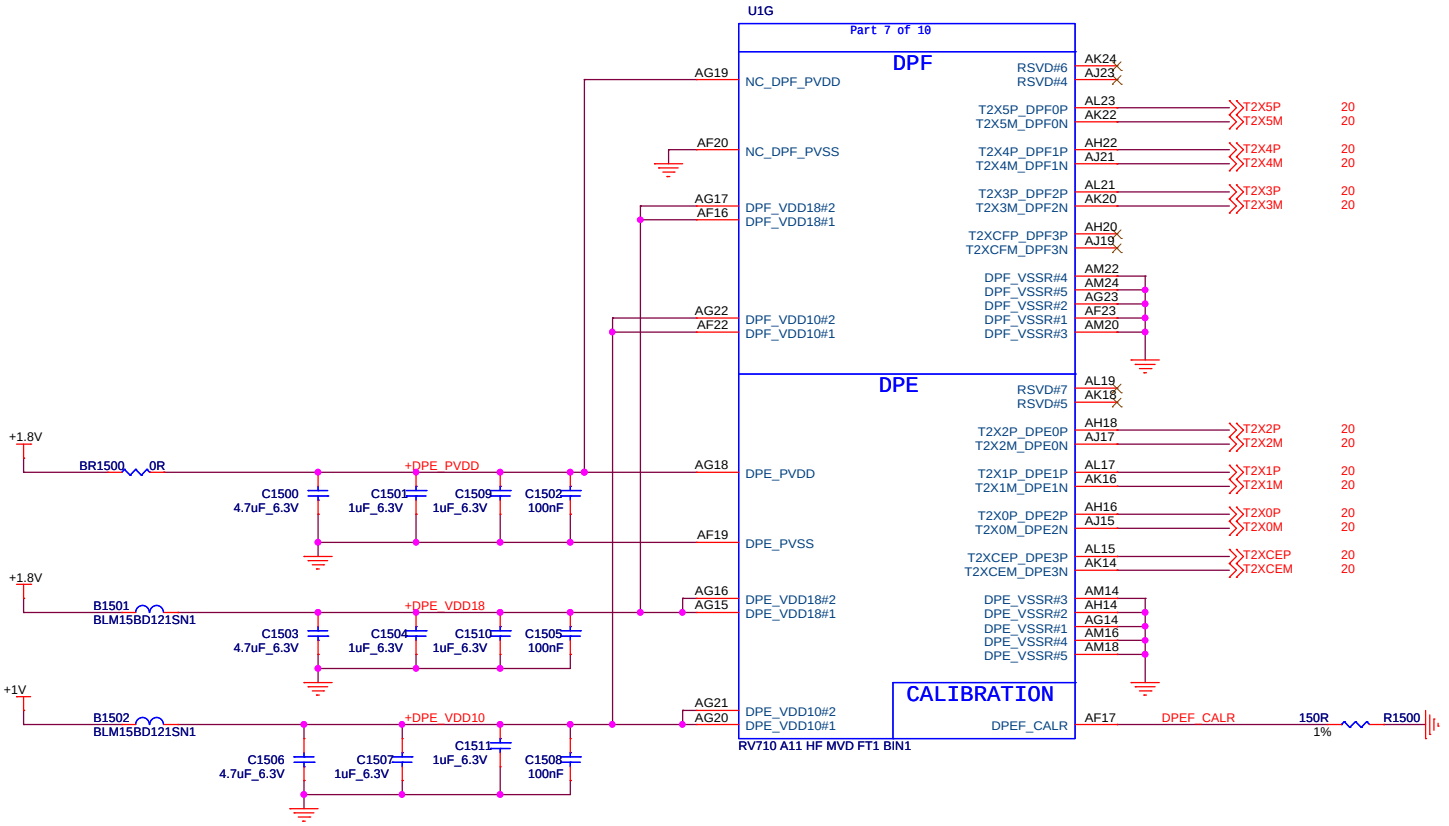
(06) RV710 TMDP E&F

LVTMDP INTERFACE



1A

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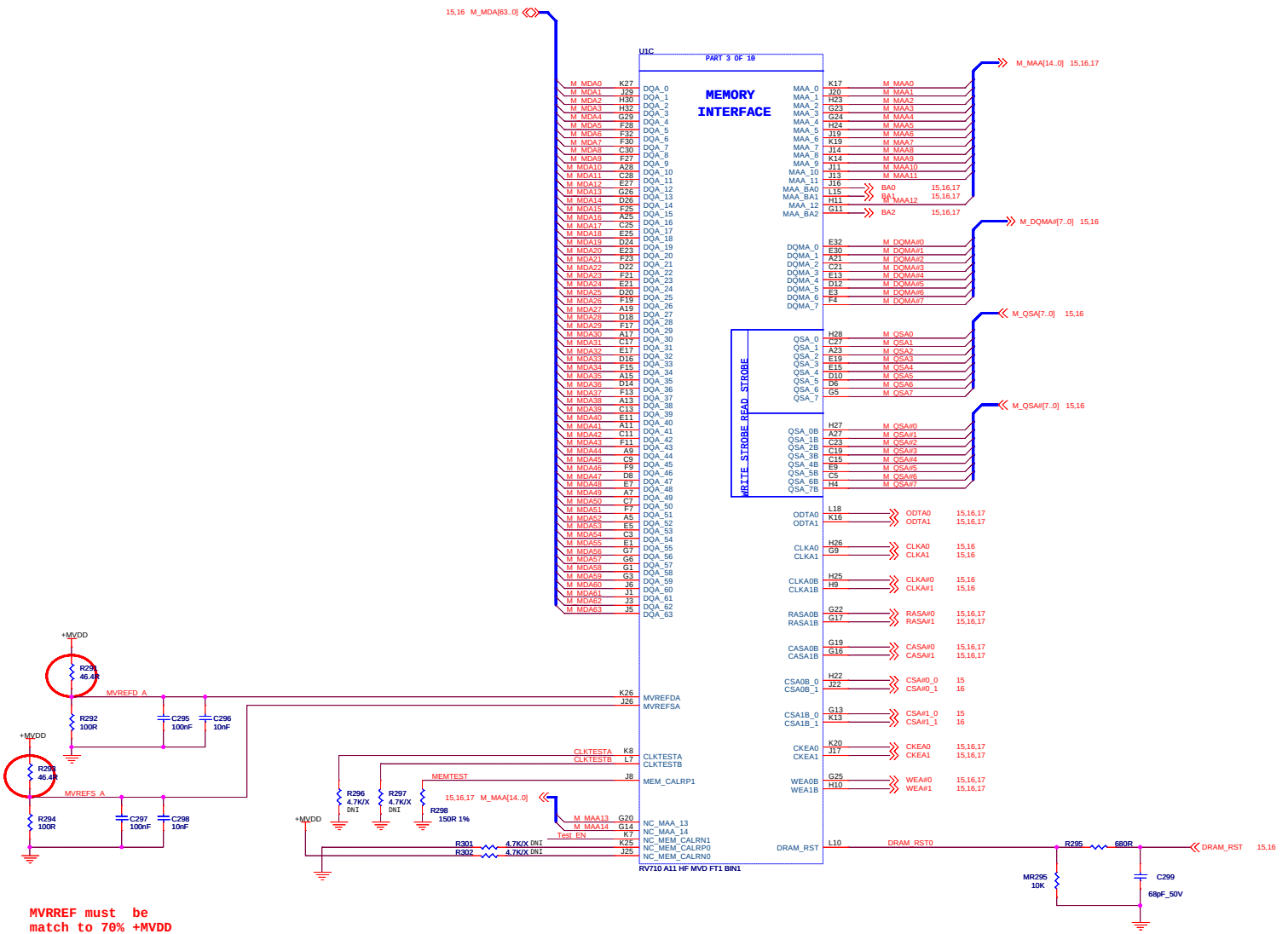
(07) RV710 MEM Interface Ch A

MEMORY INTERFACE

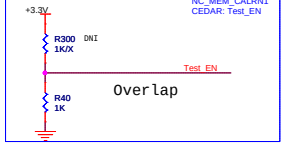


MVRREF must be match to 70% +MVDD

DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R

Modify5

RV710:
NC_MEM_CALRN1
CEDAR: Test_EN



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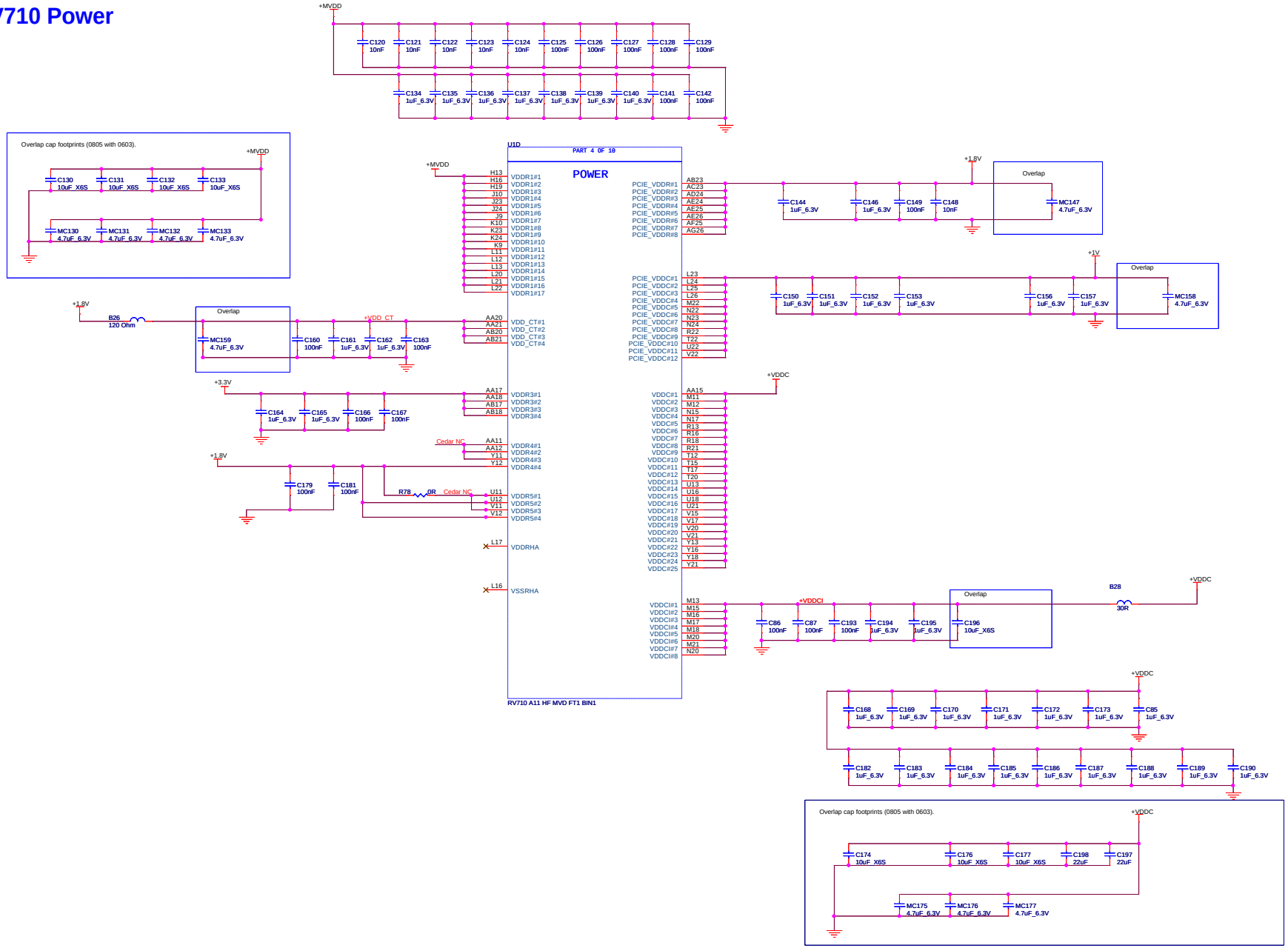
(08) RV710 Power



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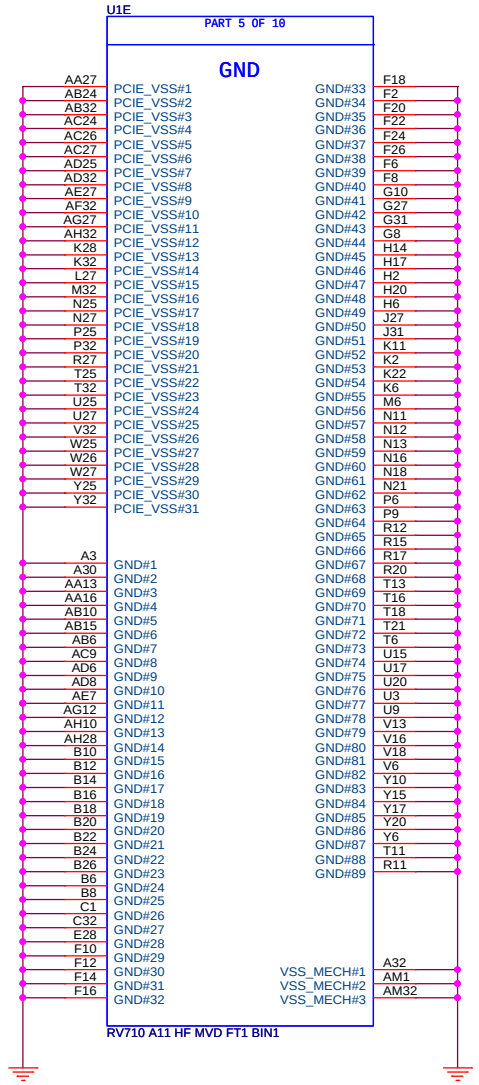
(09) RV710 GND



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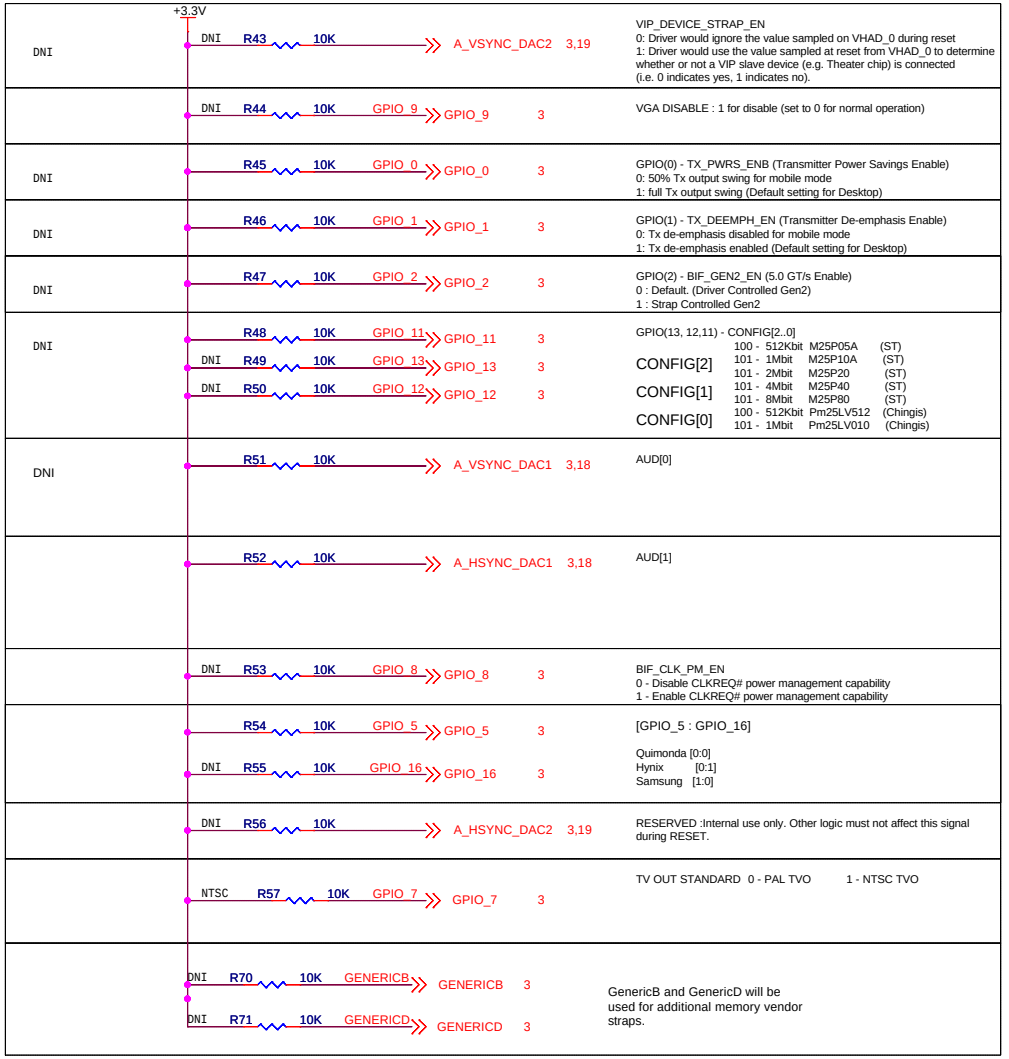
(10) RV710 STRAPS

PIN BASED STRAPS



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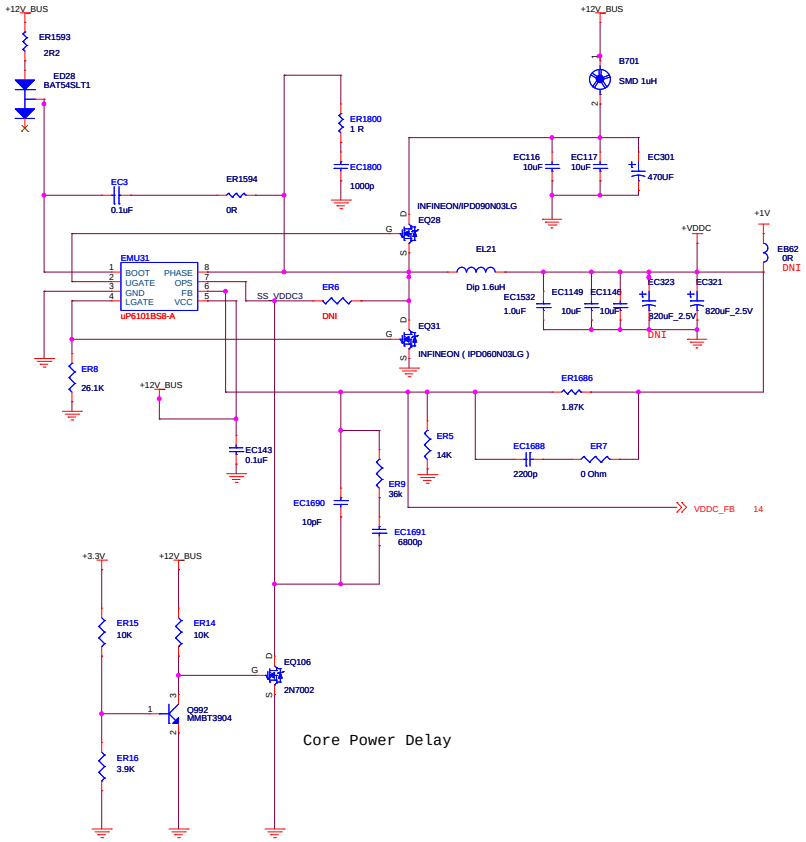
(11) VDDC



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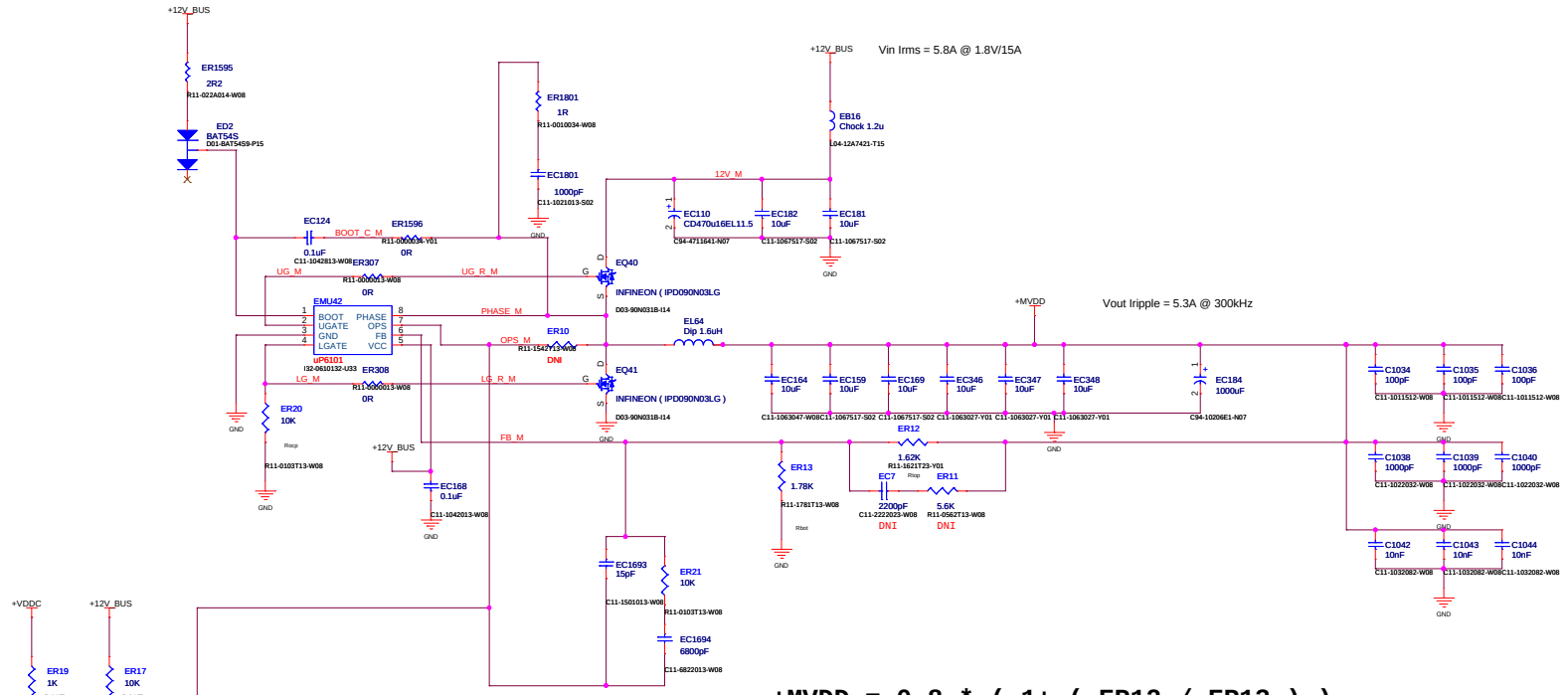
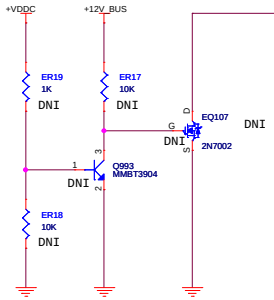
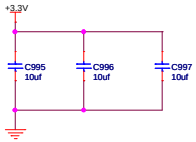
(12) MVDD

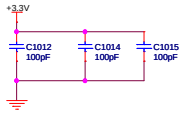


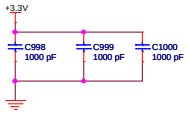
+MVDD = 0.8 * (1+ (ER12 / ER13))

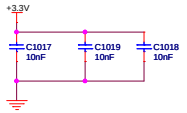


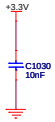
Memory Power Seq











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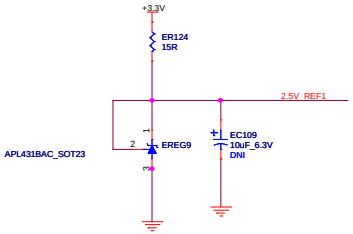
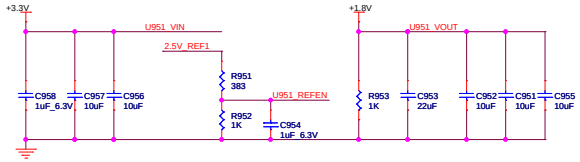
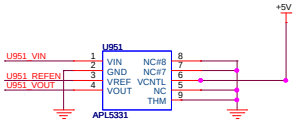
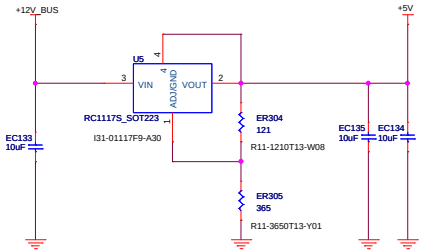
(13) Linear Regulators

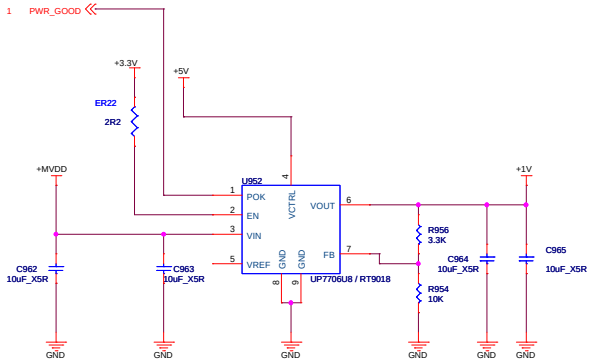








Vout=1.25V* [1+(ER305/ER304)]



Vout=0.8V * (1+ R956 / R954)

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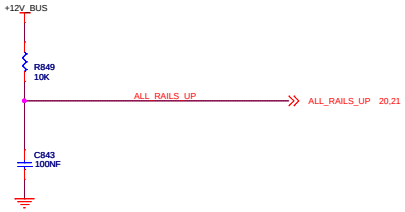
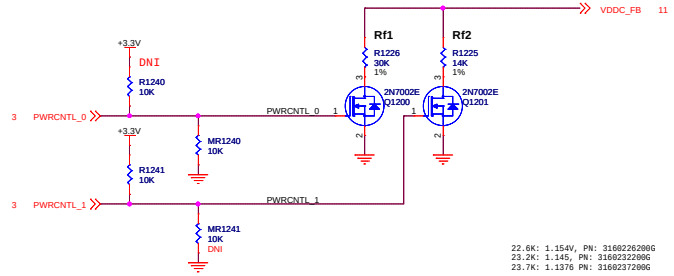
(14) Power Management



Power Play

VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=		Rf1= Rf2=	Rf1= Rf2=	
0	0					
0	1					
1	0					
1	1	1	0	1		Power-up Default



MVDD Voltage Settings Using GPIOs

PWRCNTL_2 GPIO_6	Output Voltage (V) Rf1= Rf2=		Rf1= Rf2=	Rf1= Rf2=	
0					
1	1	0	1		Power-up Default

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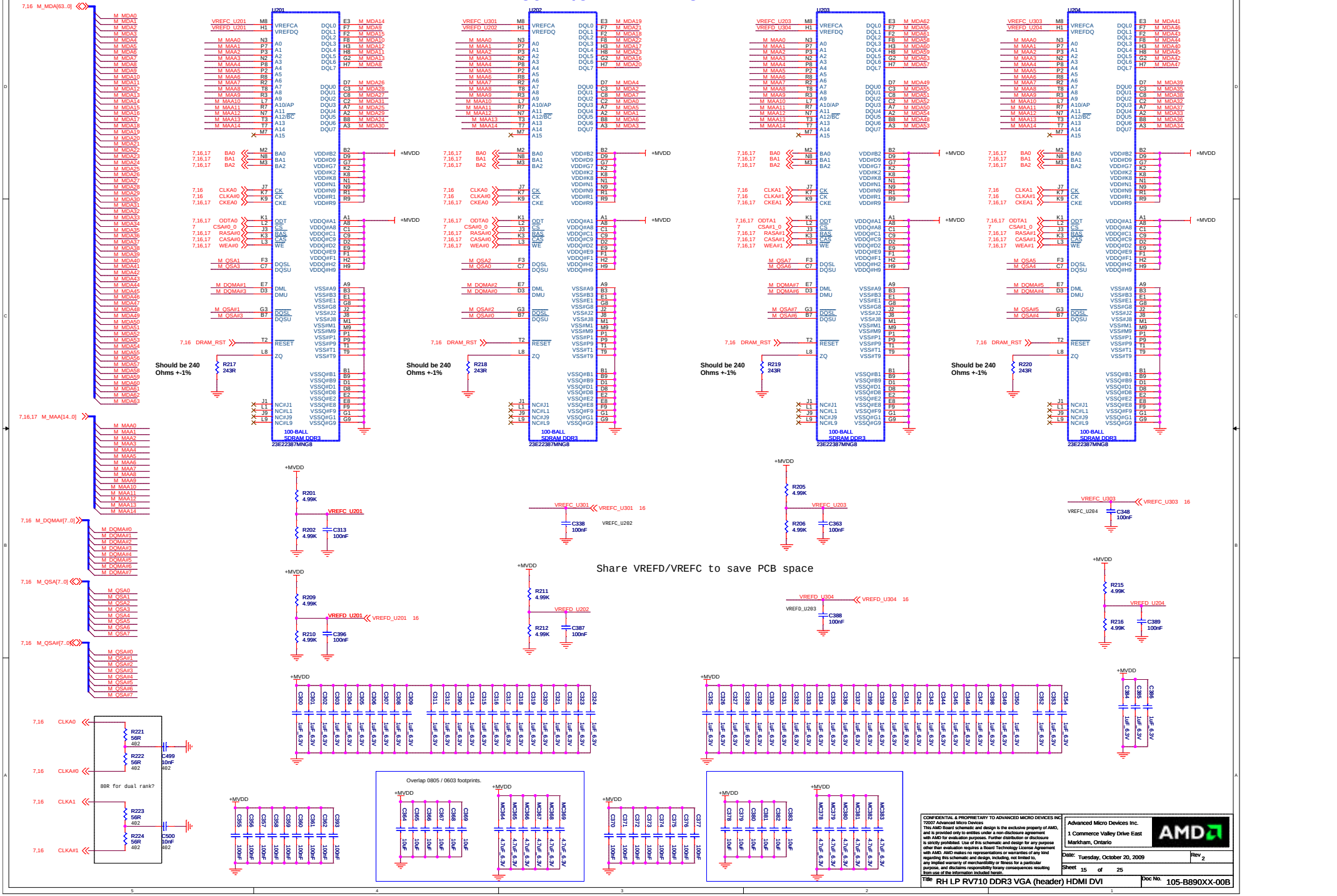
(15) DDR3 RANK1

RANK1: 256MB/512MB DDR3



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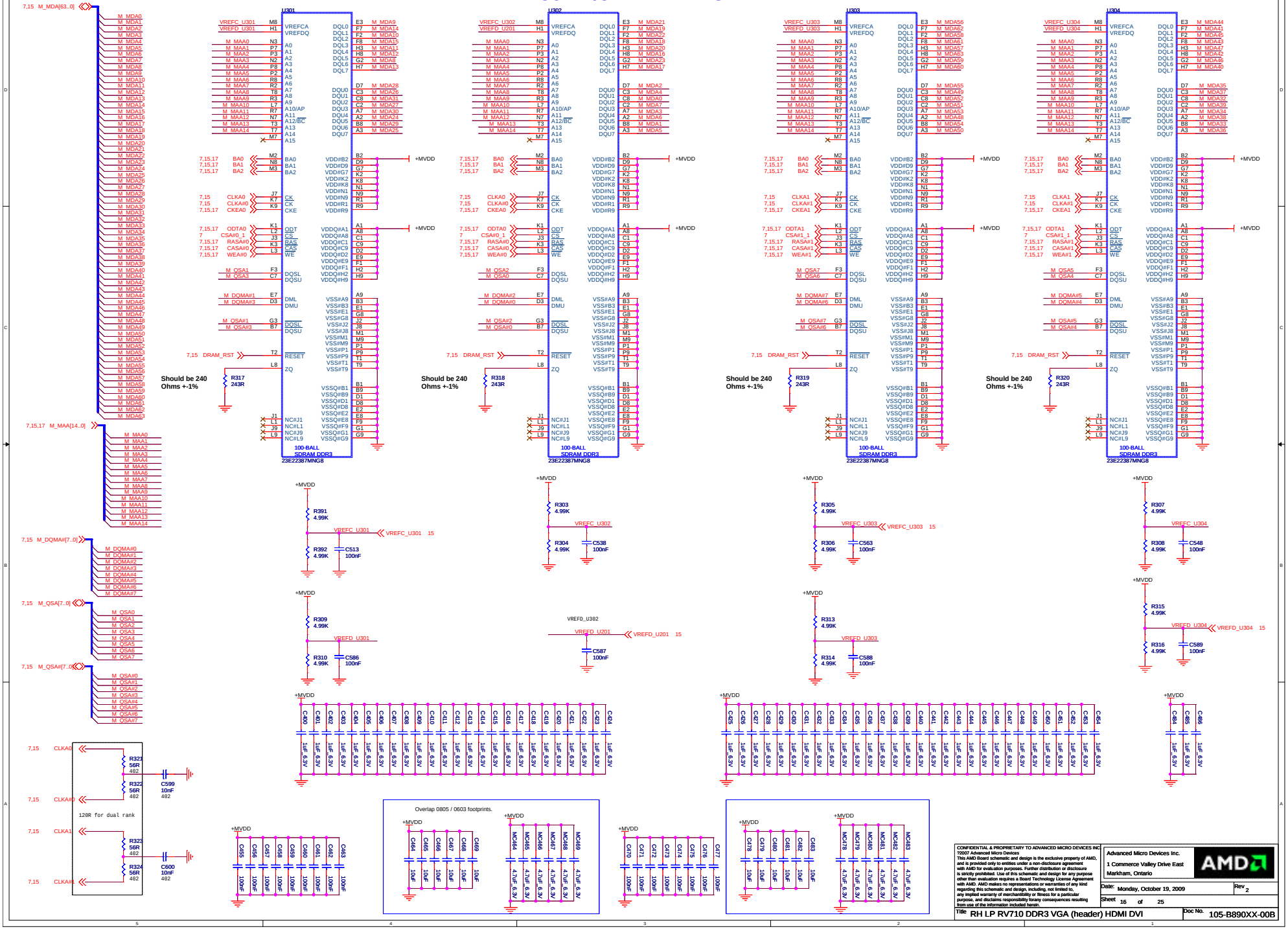
(16) DDR3 RANK2

RANK2: 256MB/512MB DDR3



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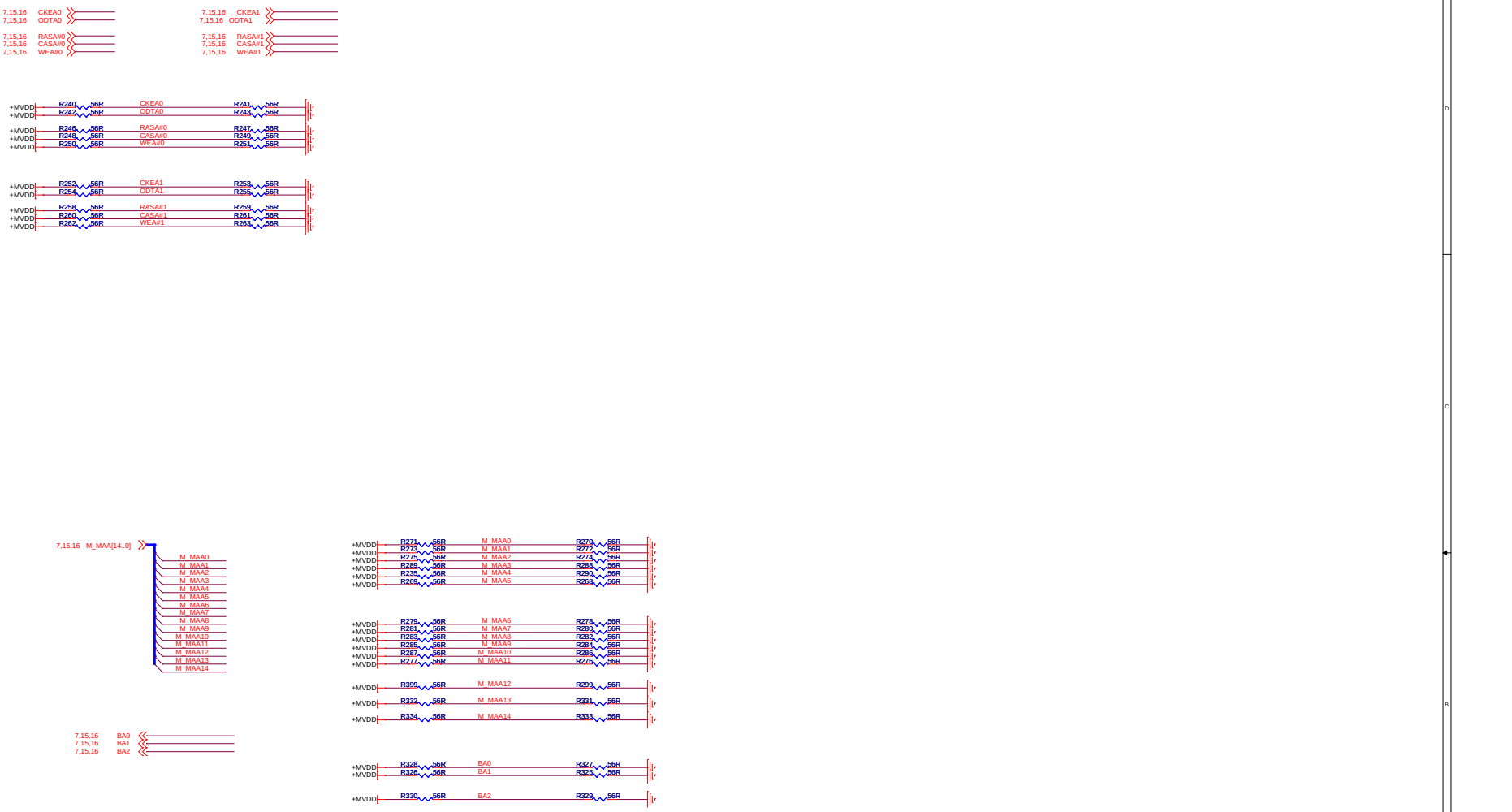
(17) DDR3 Termination



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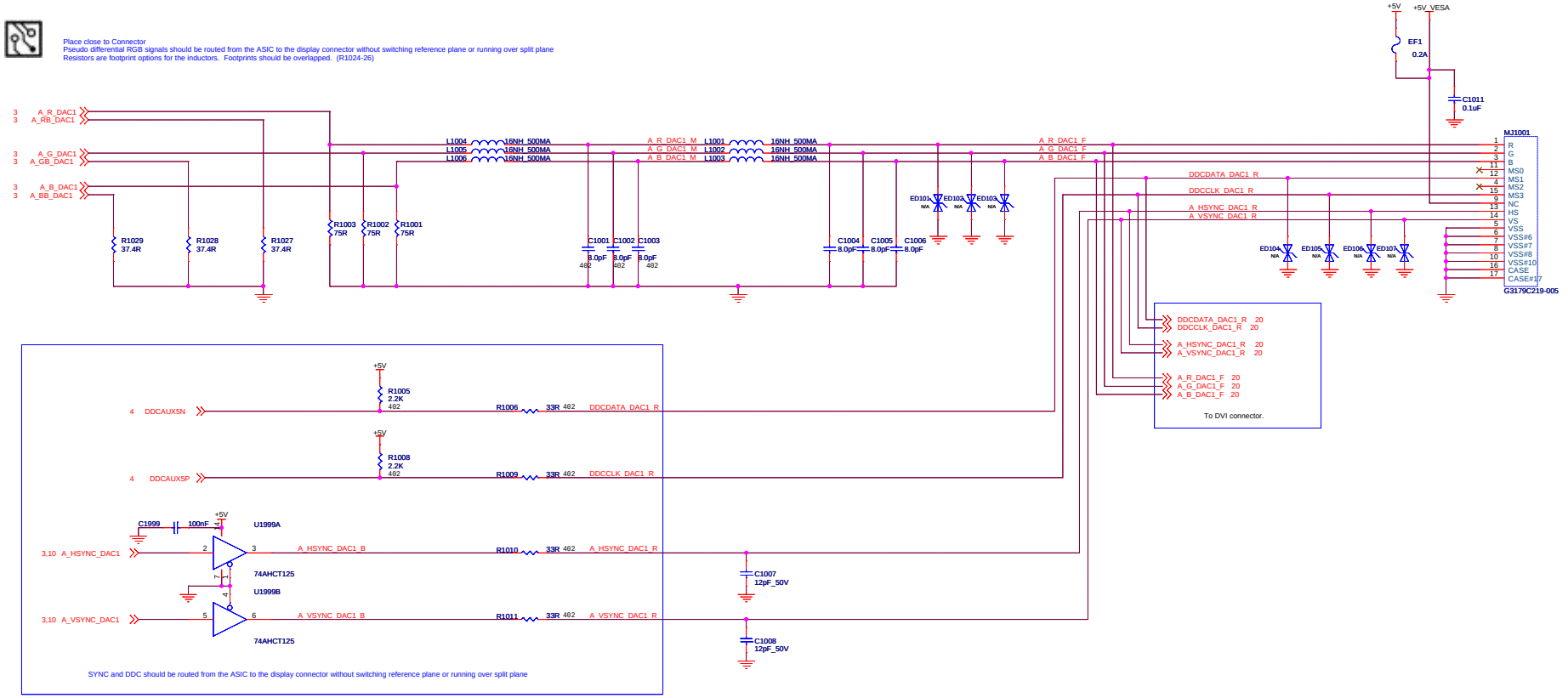
(18) DAC1 OUTPUT

DAC 1 OUTPUT



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(19) DAC2 OUTPUT

DAC 2 OUTPUT

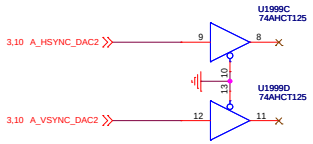
Optional ESD Protection Diods

Place near D2002, D2003, D2004, D2005

Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane

RV710: DDC2 is 5V tolerant. Do not install level shifter.
--> Do not install R2013, R2015, Q2001, Q2002. Install R2014, R2016.
RV810: DDC2 is NOT 5V tolerant. Install level shifter.
--> Do not install R2014, R2016. Install R2013, R2015, Q2001, Q2002.

Remove VGA RIBBON CONNECTOR
2009/09/23



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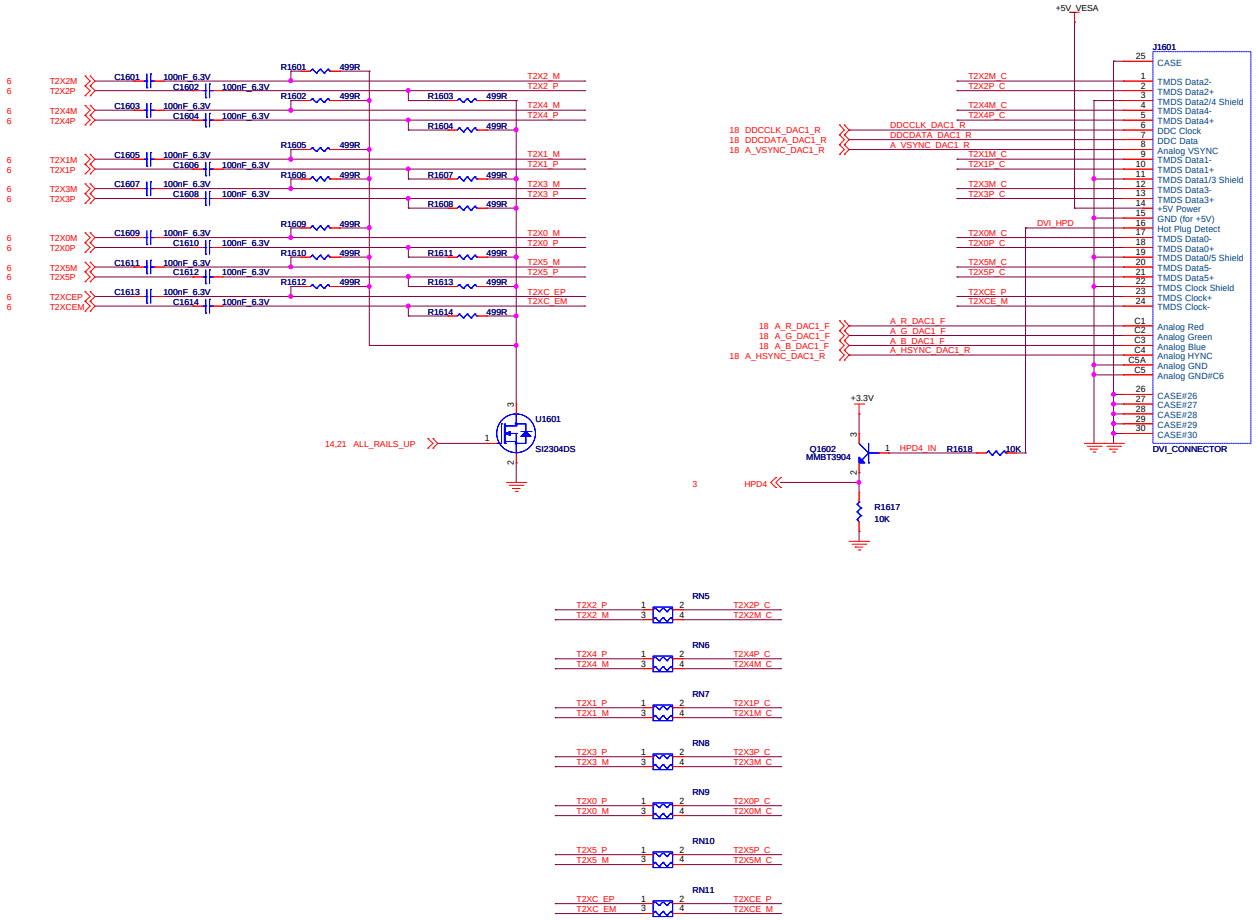
(20) DVI OUTPUT

DPE / DPF OUTPUT



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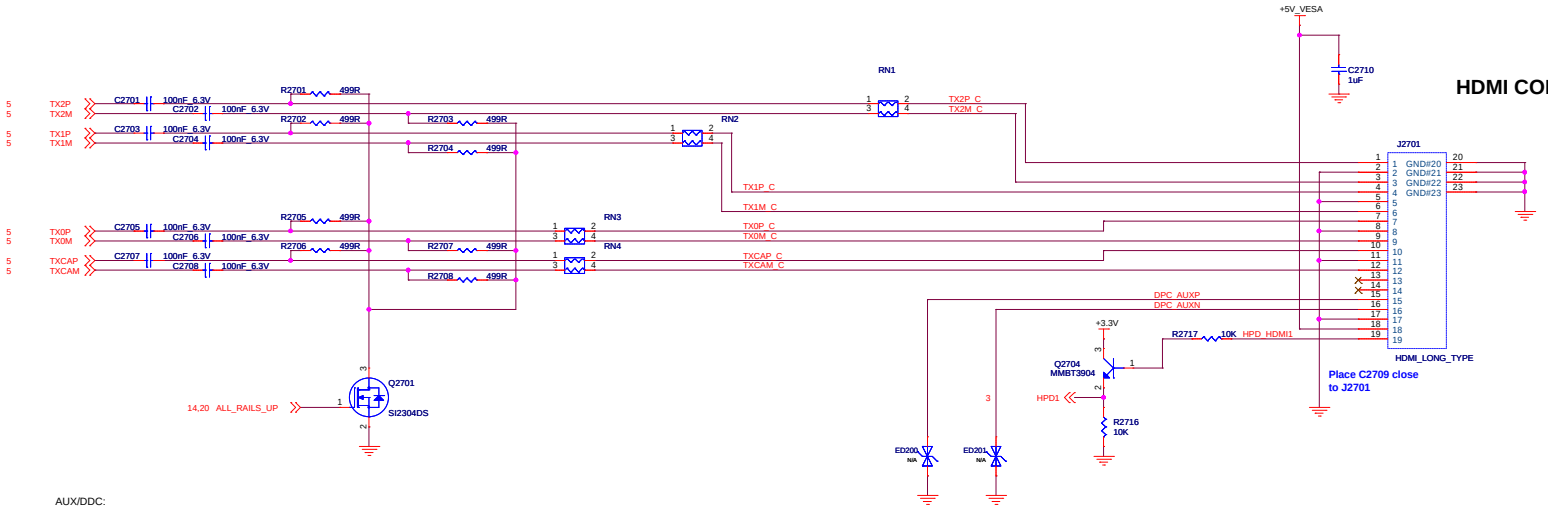
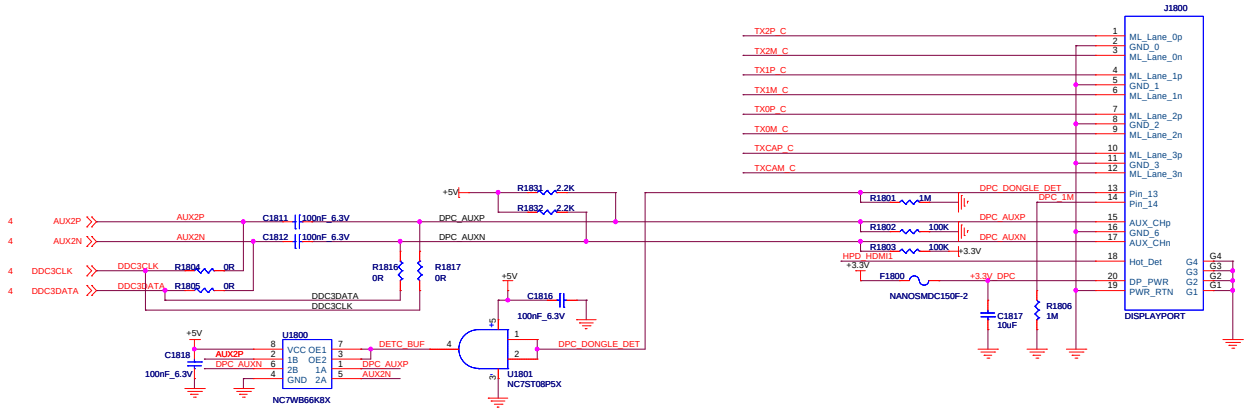
(21) HDMI OUTPUT

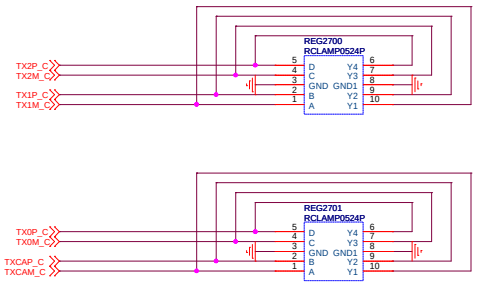
TMDP-B OUTPUT



AUX/DDC:
FOR 740/730, INSTALL 0R ON ASIC-SIDE OF AC COUPLING CAPS ONLY;
FOR JUNIPER, INSTALL 0R ON CONNECTOR SIDE OF AC COUPLING CAPS ONLY;



Optional ESD protection diodes



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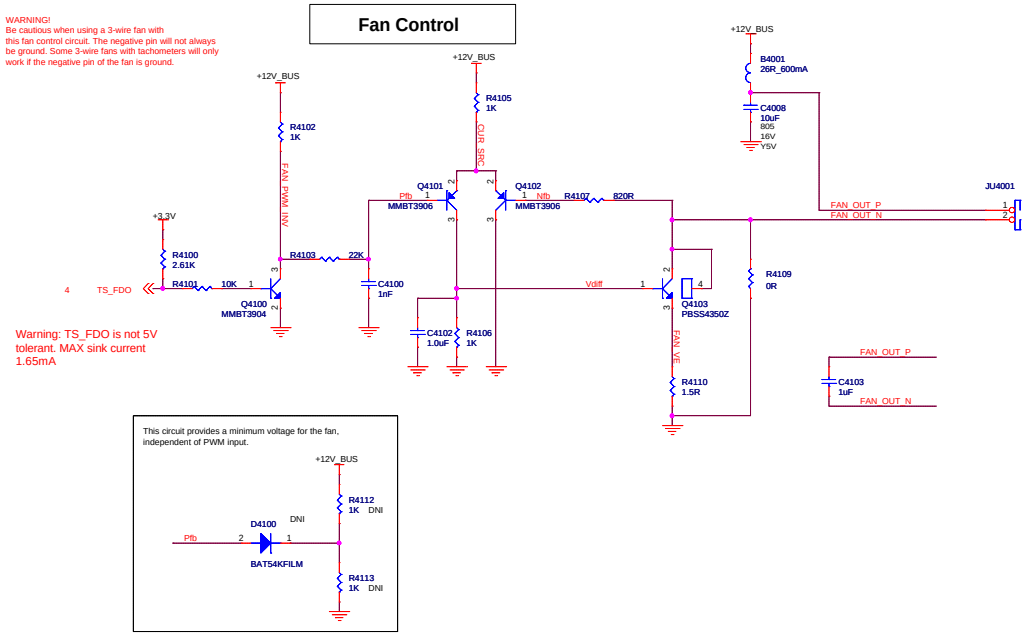
(22) Thermal Management



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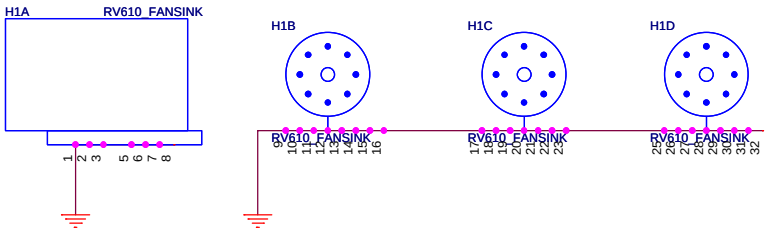
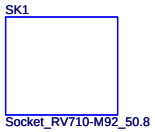
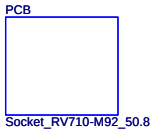
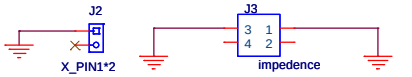
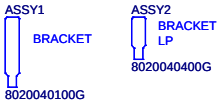


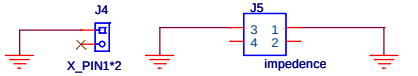
7120036200G

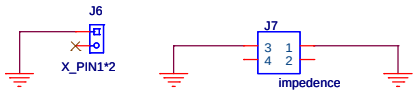


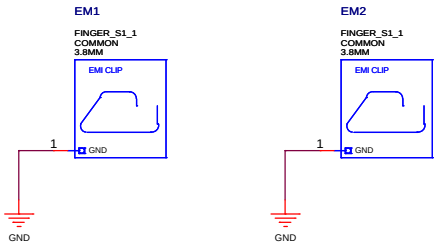












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Title RH LP RV710 DDR3 VGA (header) HDMI DVI

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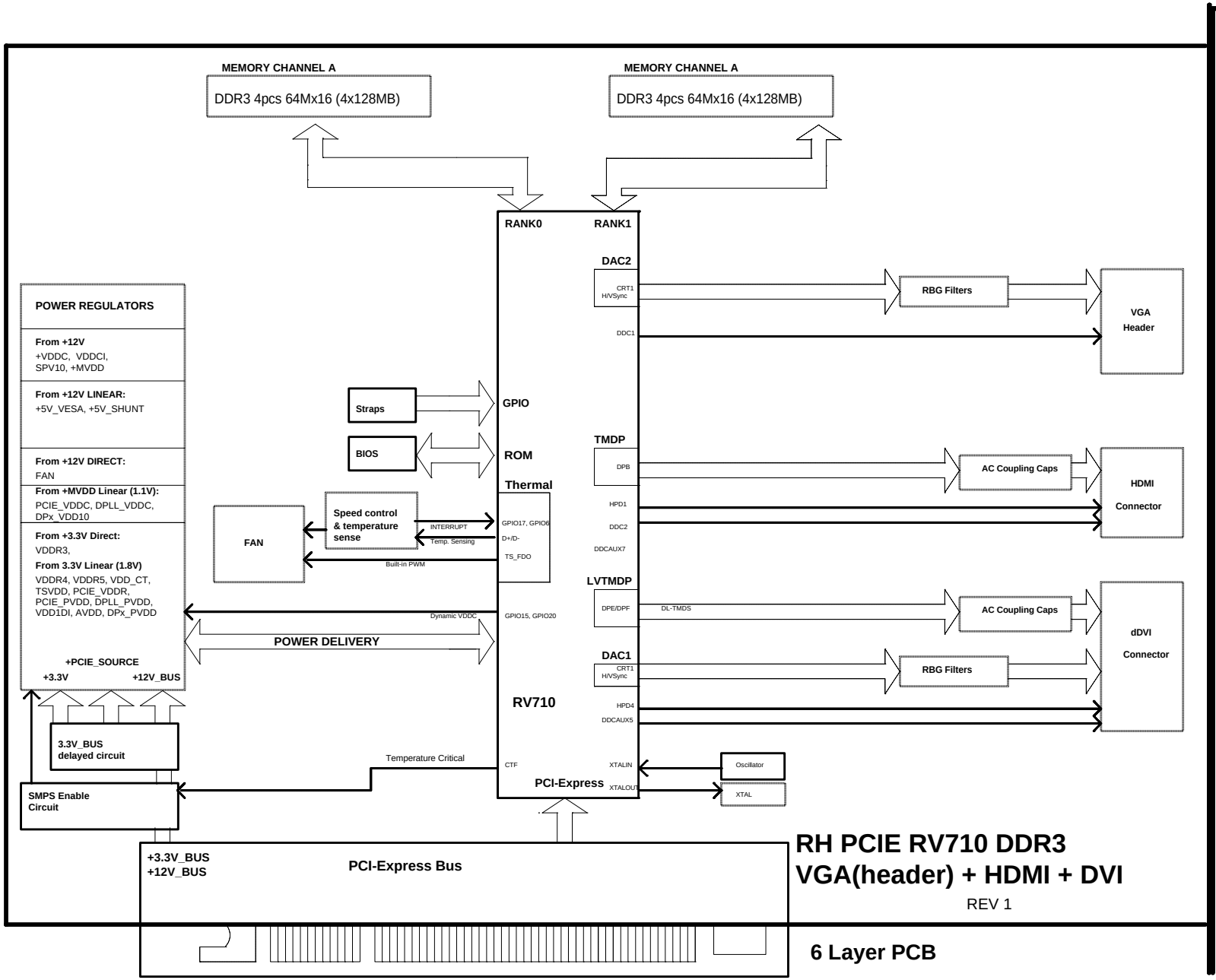

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Title	RH LP RV710 DDR3 VGA (header) HDMI DVI
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Title	Schematic No.	Date:
RH LP RV710 DDR3 VGA (header) HDMI DVI	105-B890XX-00B	Monday, October 19, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI s? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

RV710 ENGINEERING BOARD

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	2008.12.30	INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.
1	00B	2009.01.22	Sch no change. just modify HDMI connnecro location on PCB