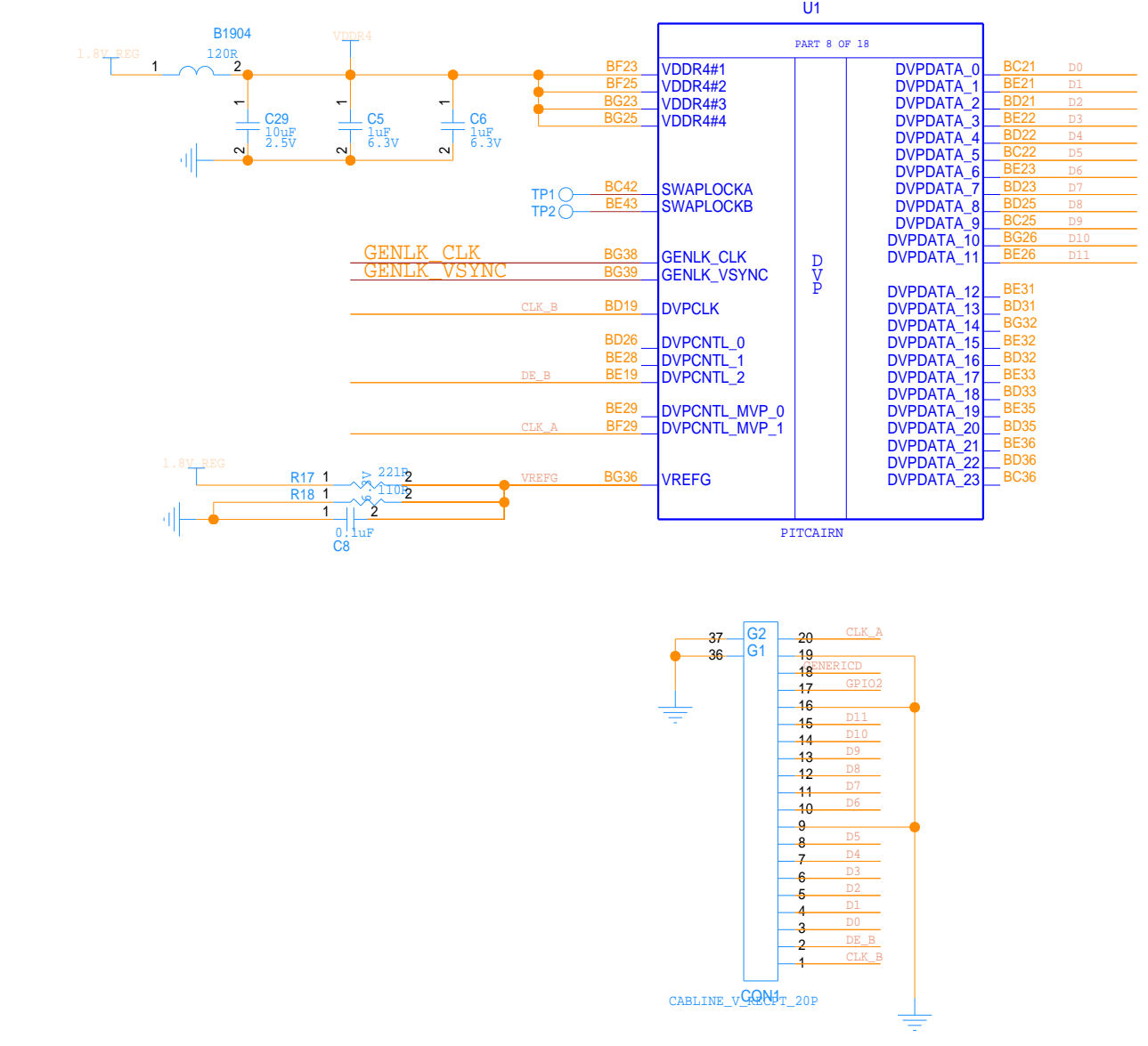
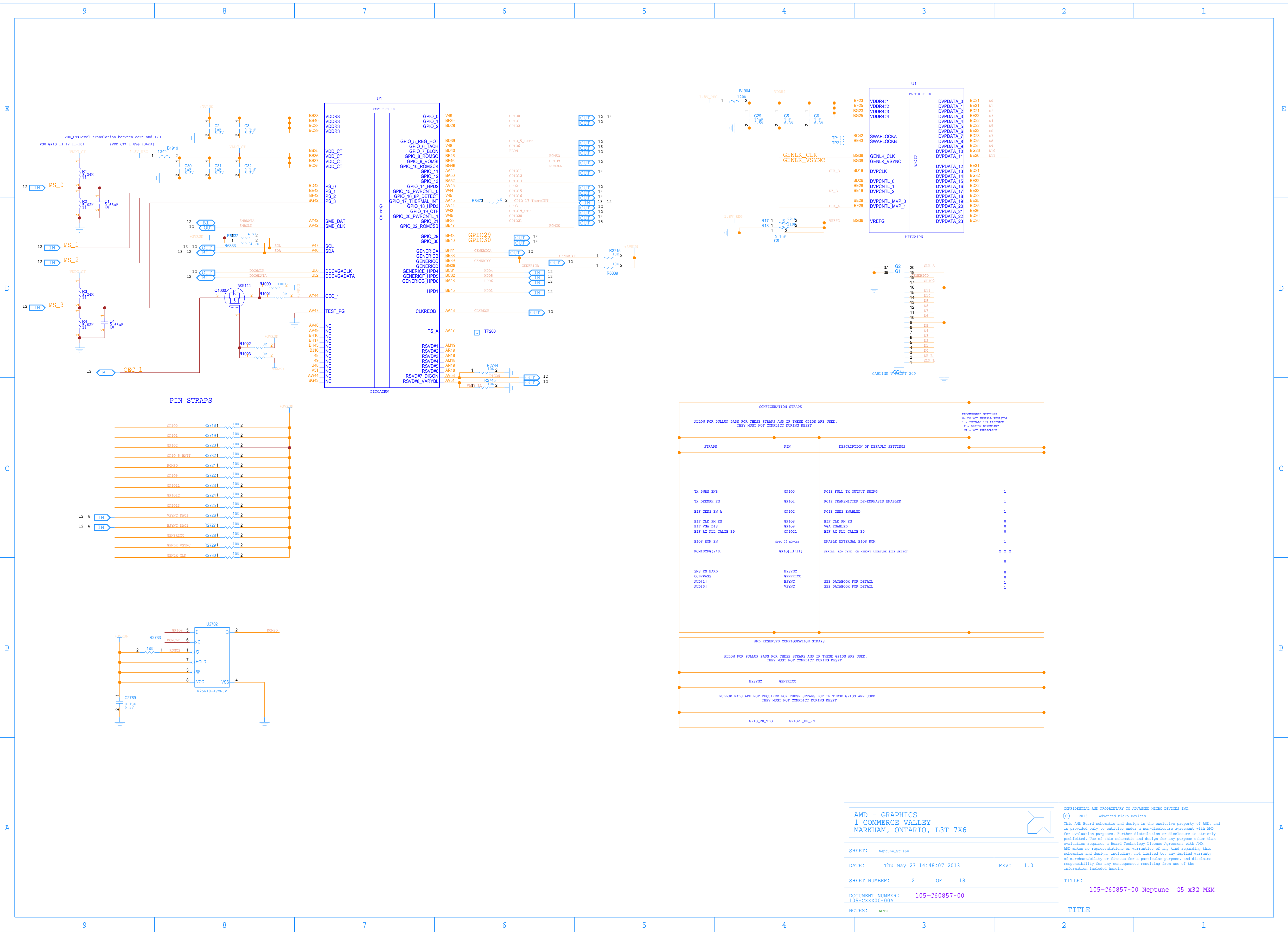


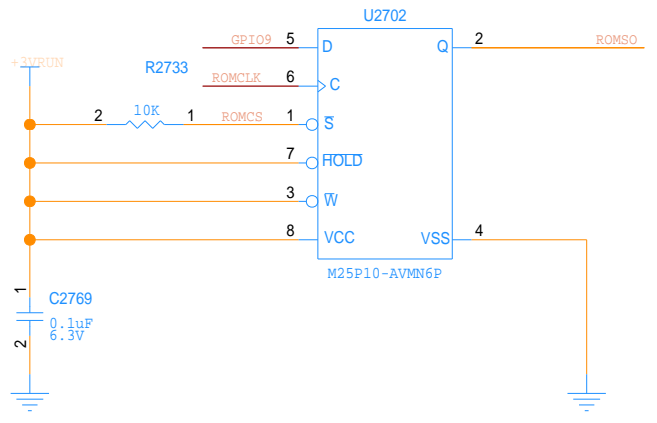


TITLE



CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PRRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
RIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
RIF_CLK_PM_EN	GPIO8	RIF_CLK_PM_EN	0
RIF_VGA_DIS	GPIO9	VGA ENABLED	0
RIF_FX_PLL_CALIB_BP	GPIO21	RIF_FX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO12_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDPG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
HSYNC_HARD	HSYNC	HSYNC	0
CONFPASS	GENERIC0	GENERIC0	0
AUD[1]	HSYNC	SEE DATABASE FOR DETAIL	1
AUD[0]	VSYS	SEE DATABASE FOR DETAIL	1
AMD RESERVED CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
HSYNC	GENERIC0		
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
GPIO28_TDO	GPIO21_BB_EN		

PIN STRAPS			
GPIO0	R27181	10K	2
GPIO1	R27181	10K	2
GPIO2	R27201	10K	2
GPIO5_BATT	R27321	10K	2
ROMCS	R27211	10K	2
GPIO9	R27221	10K	2
GPIO11	R27231	10K	2
GPIO12	R27241	10K	2
GPIO13	R27251	10K	2
VSYS_DAC1	R27261	10K	2
VSYS_DAC1	R27271	10K	2
GENERIC0	R27281	10K	2
GENLK_VSYNC	R27291	10K	2
GENLK_CLK	R27301	10K	2



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SHEET: Neptune_Straps

DATE: Thu May 23 14:48:07 2013

SHEET NUMBER: 2 OF 18

DOCUMENT NUMBER: 105-C60857-00

NOTES: NOTE

REV: 1.0

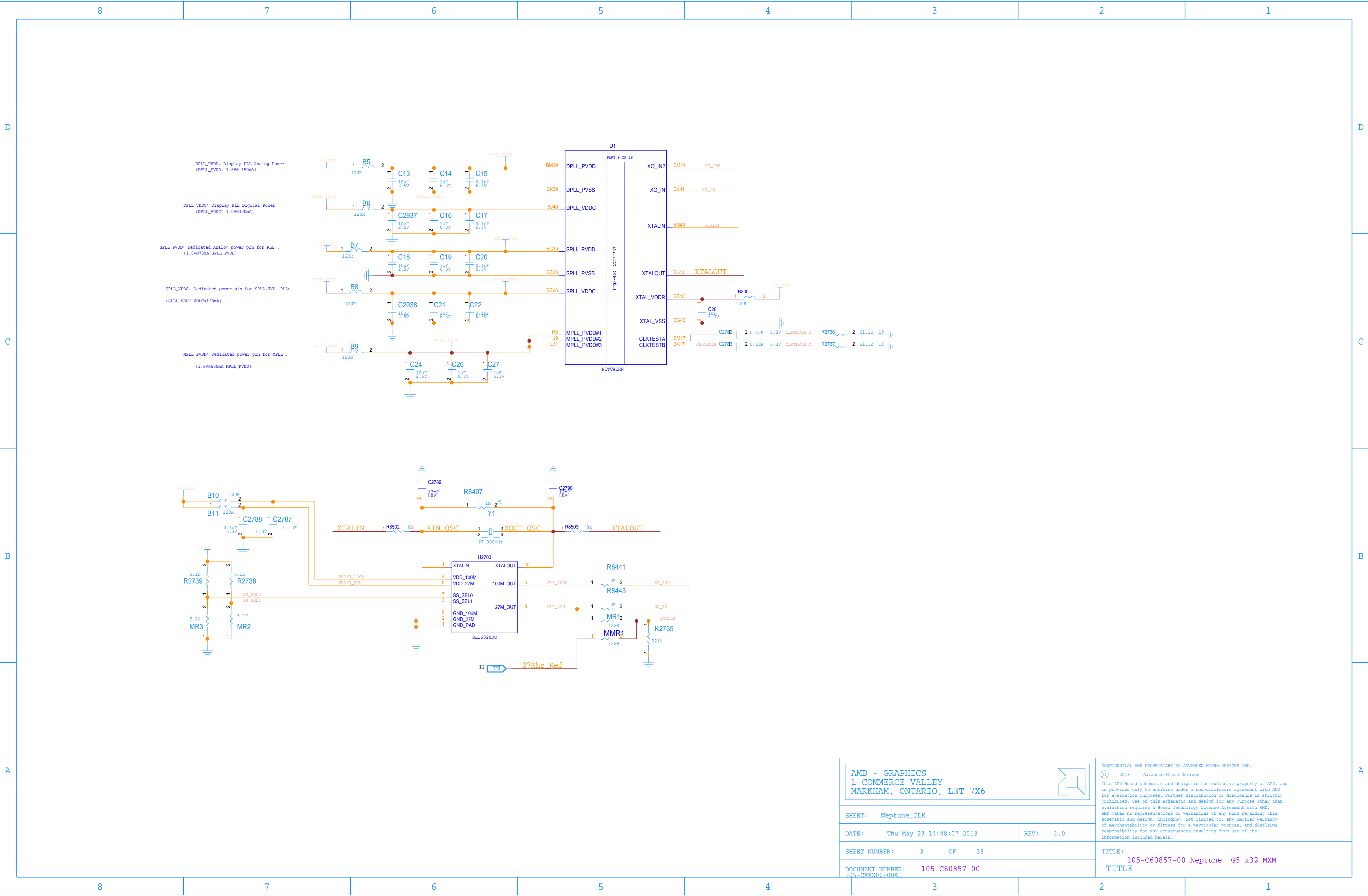
TITLE: 105-C60857-00 Neptune G5 x32 MXM

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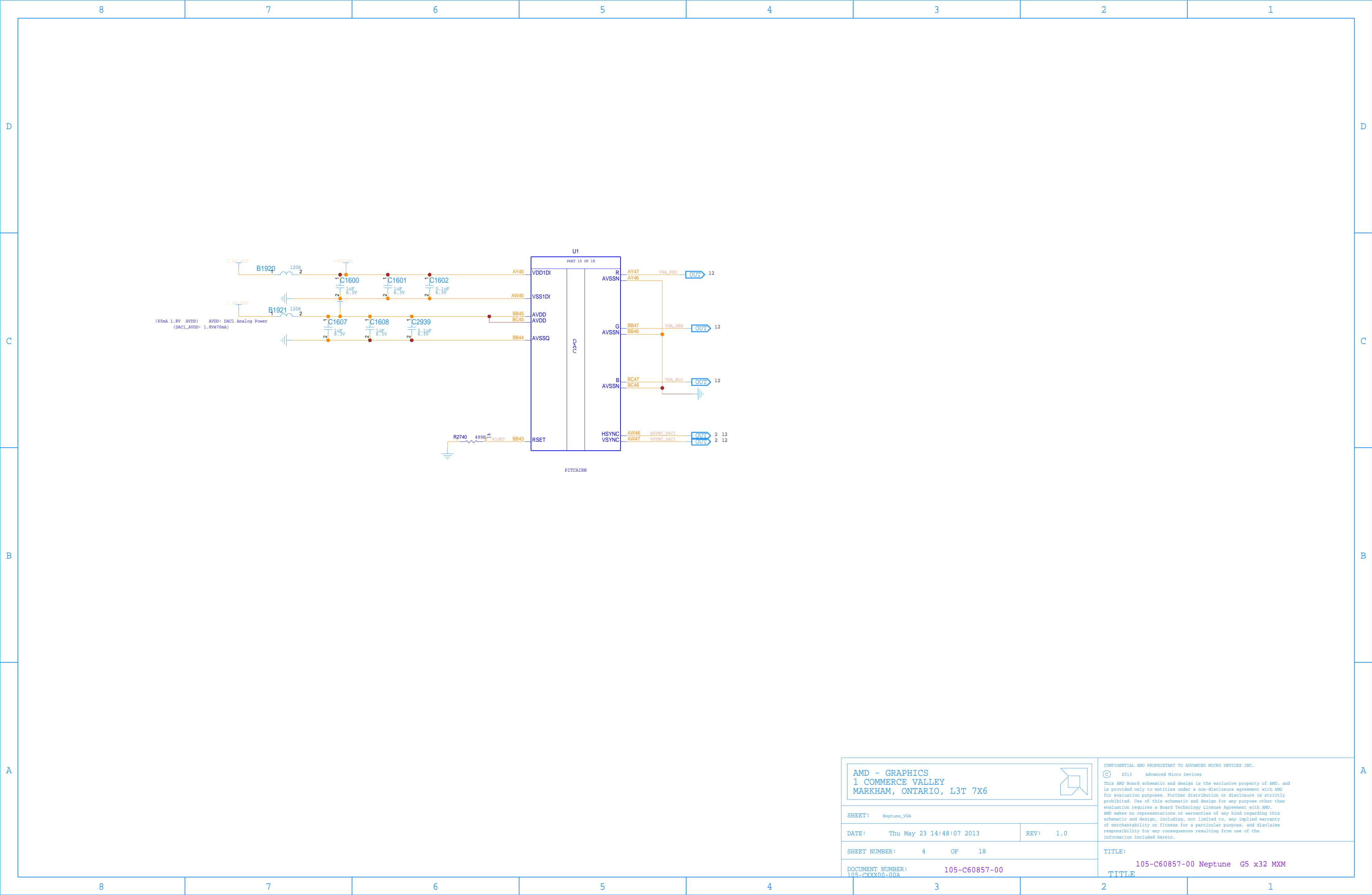
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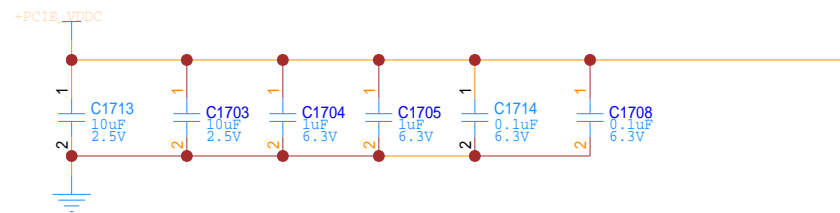
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SHEET: Neptune_CLK		TITLE: 105-C60857-00 Neptune G5 x32 MXM	
DATE: Thu May 23 14:48:07 2013		REV: 1.0	
SHEET NUMBER: 3 OF 18		TITLE: 105-C60857-00 Neptune G5 x32 MXM	
DOCUMENT NUMBER: 105-C60857-00		TITLE: 105-C60857-00 Neptune G5 x32 MXM	

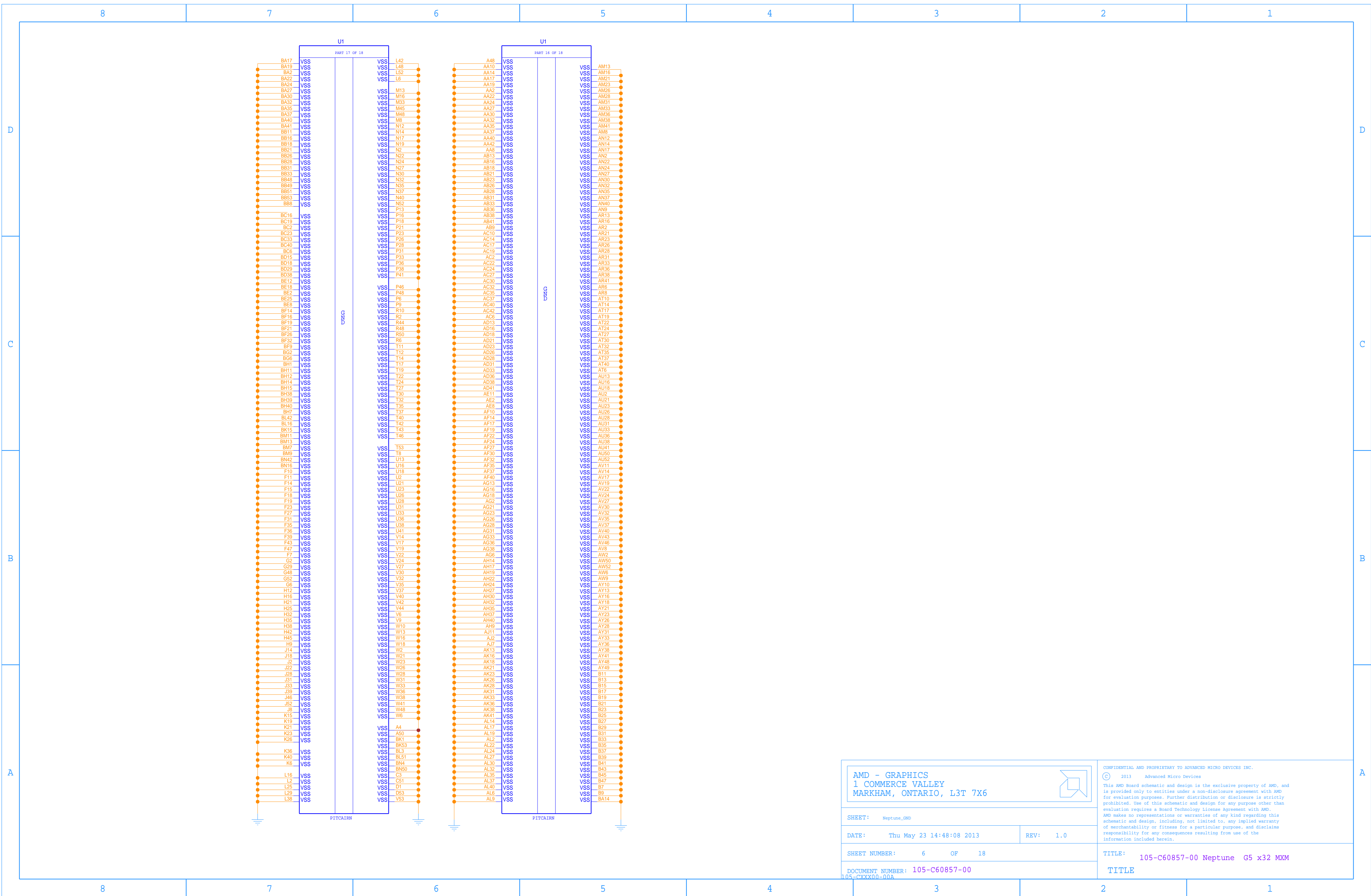


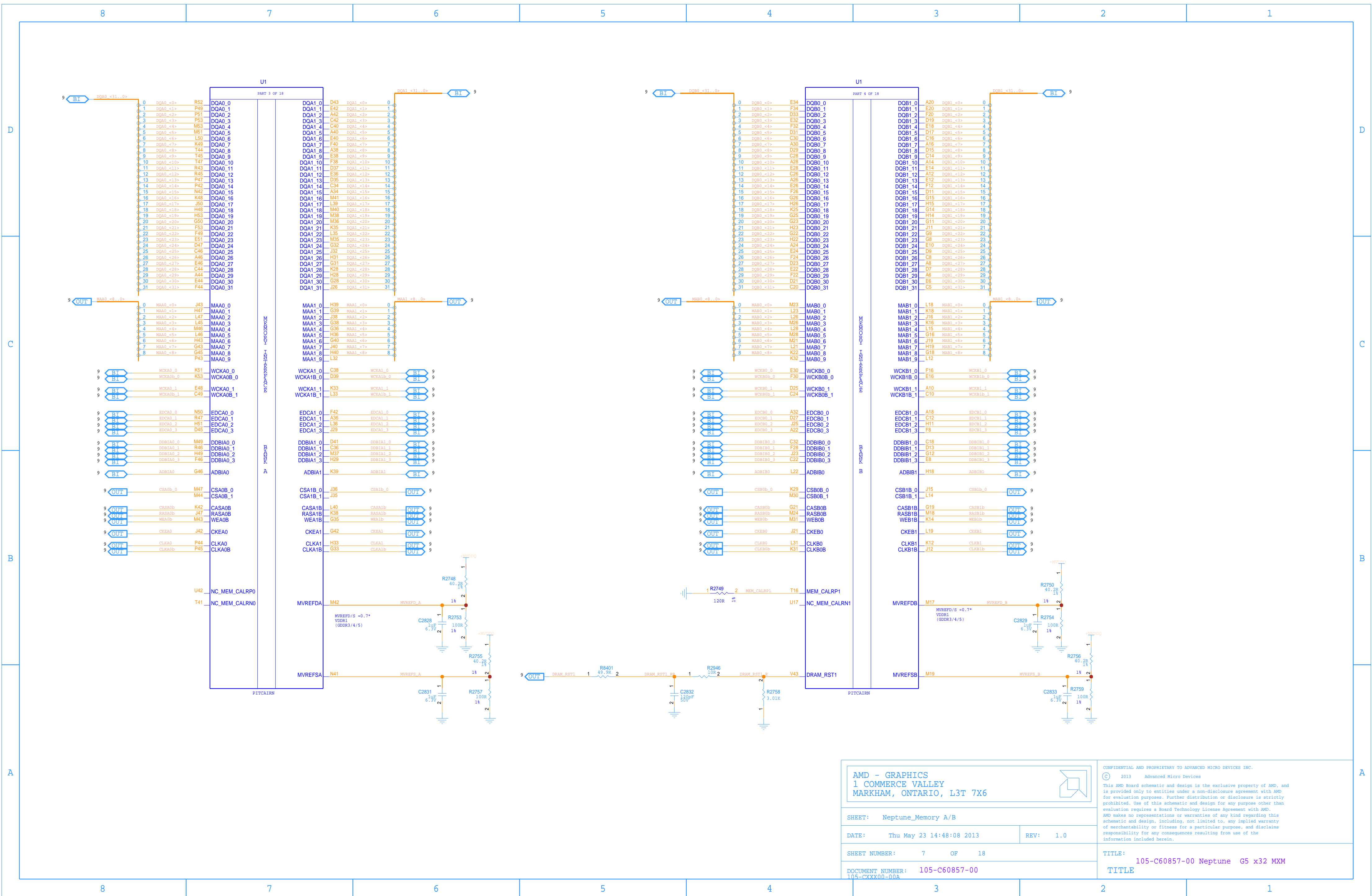
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SHEET: Neptune_VGA		REV: 1.0	
DATE: Thu May 23 14:48:07 2013		TITLE: 105-C60857-00 Neptune G5 x32 MXM	
SHEET NUMBER: 4 OF 18		TITLE	
DOCUMENT NUMBER: 105-CXXX00-00A		105-C60857-00	



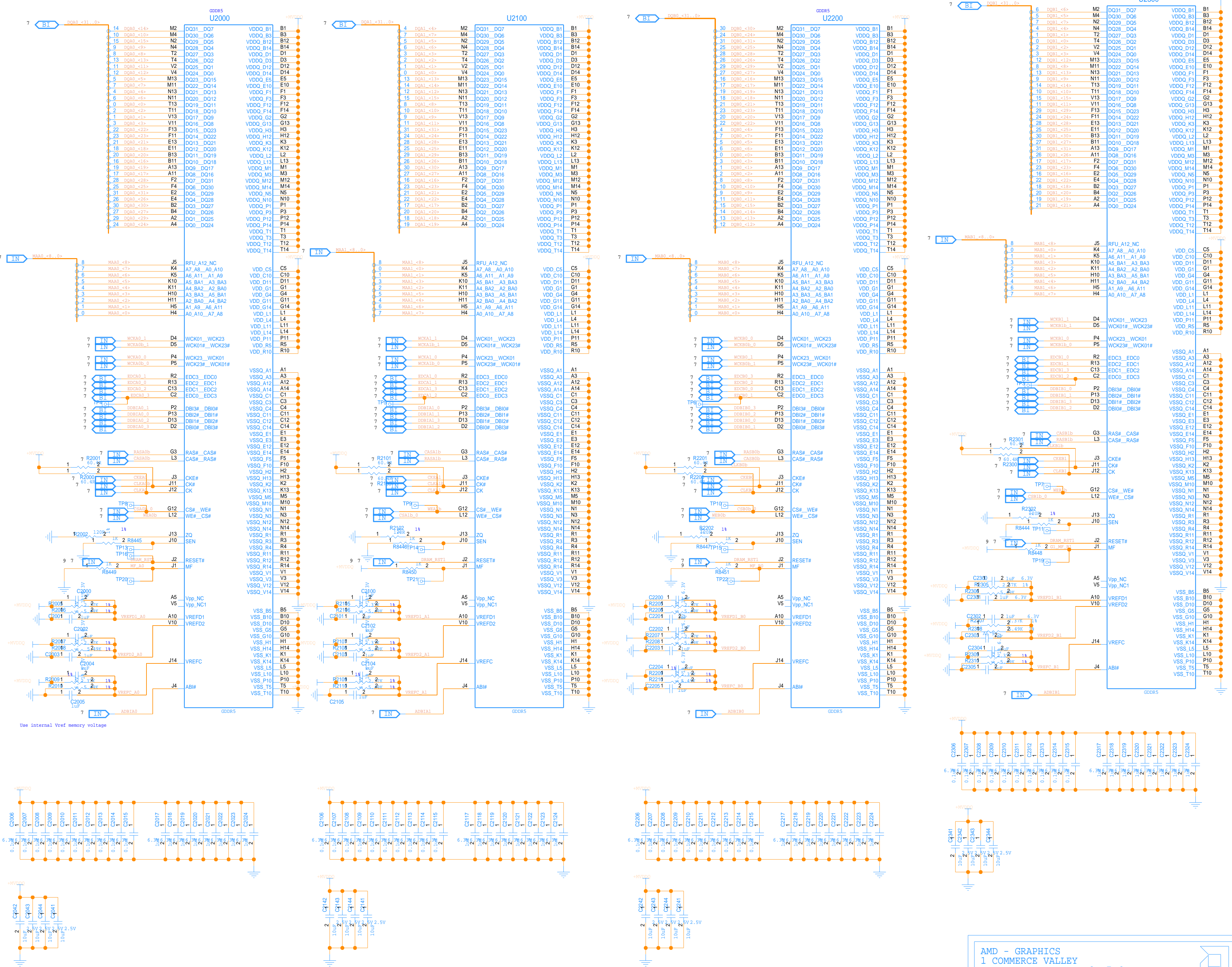
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TITLE:
105-C60857-00 Neptune G5 x32 MXM
TITLE
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(5) GDDR5 Memory Channel A&B



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SHEET: GDDR5 32MX32 A

DATE: Thu May 23 14:48:10 2013

REV: 1.0

SHEET NUMBER: 9 OF 18

DOCUMENT NUMBER: 105-C60857-00

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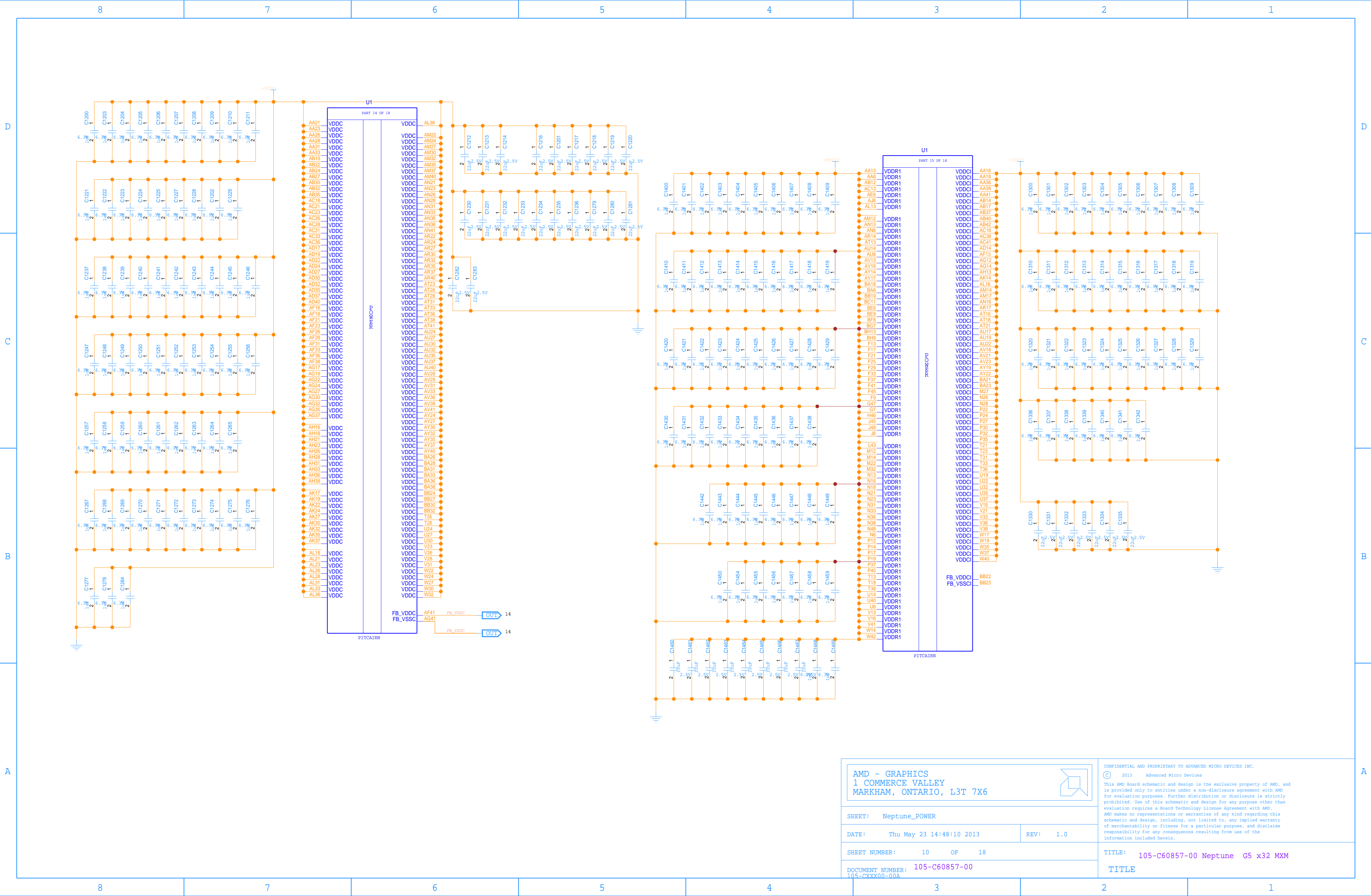
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TITLE:

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SHEET: Neptune_POWER

DATE: Thu May 23 14:48:10 2013

SHEET NUMBER: 10 OF 18

DOCUMENT NUMBER: 105-C60857-00

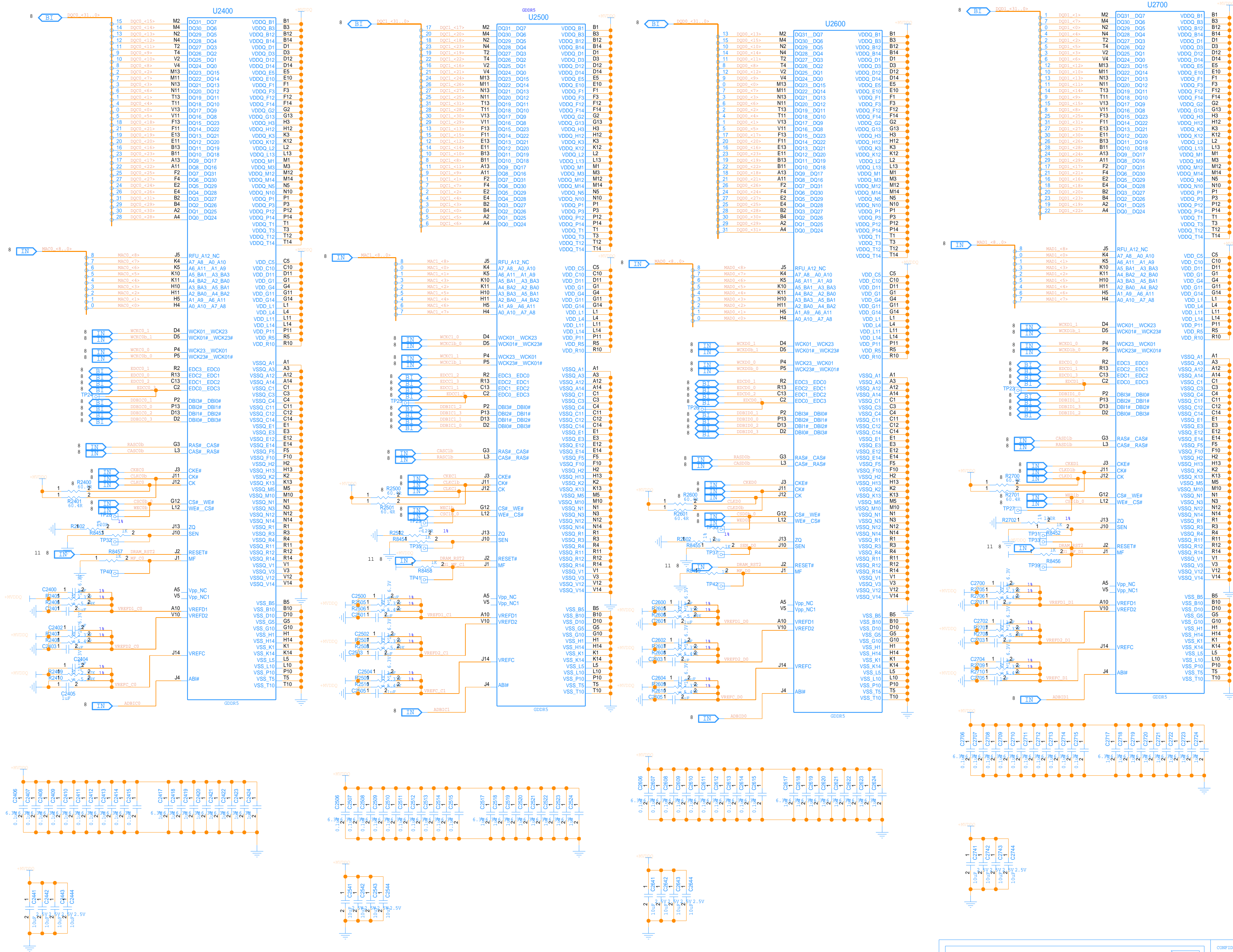
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TITLE: 105-C60857-00 Neptune G5 x32 MXM

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TITLE

(6) GDDR5 Memory Channel C&D



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SHEET: GDDR5 32MX32 E

DATE: Thu May 23 14:48:11 2013

SHEET NUMBER: 11 OF

DOCUMENT NUMBER: 105-C60857-00

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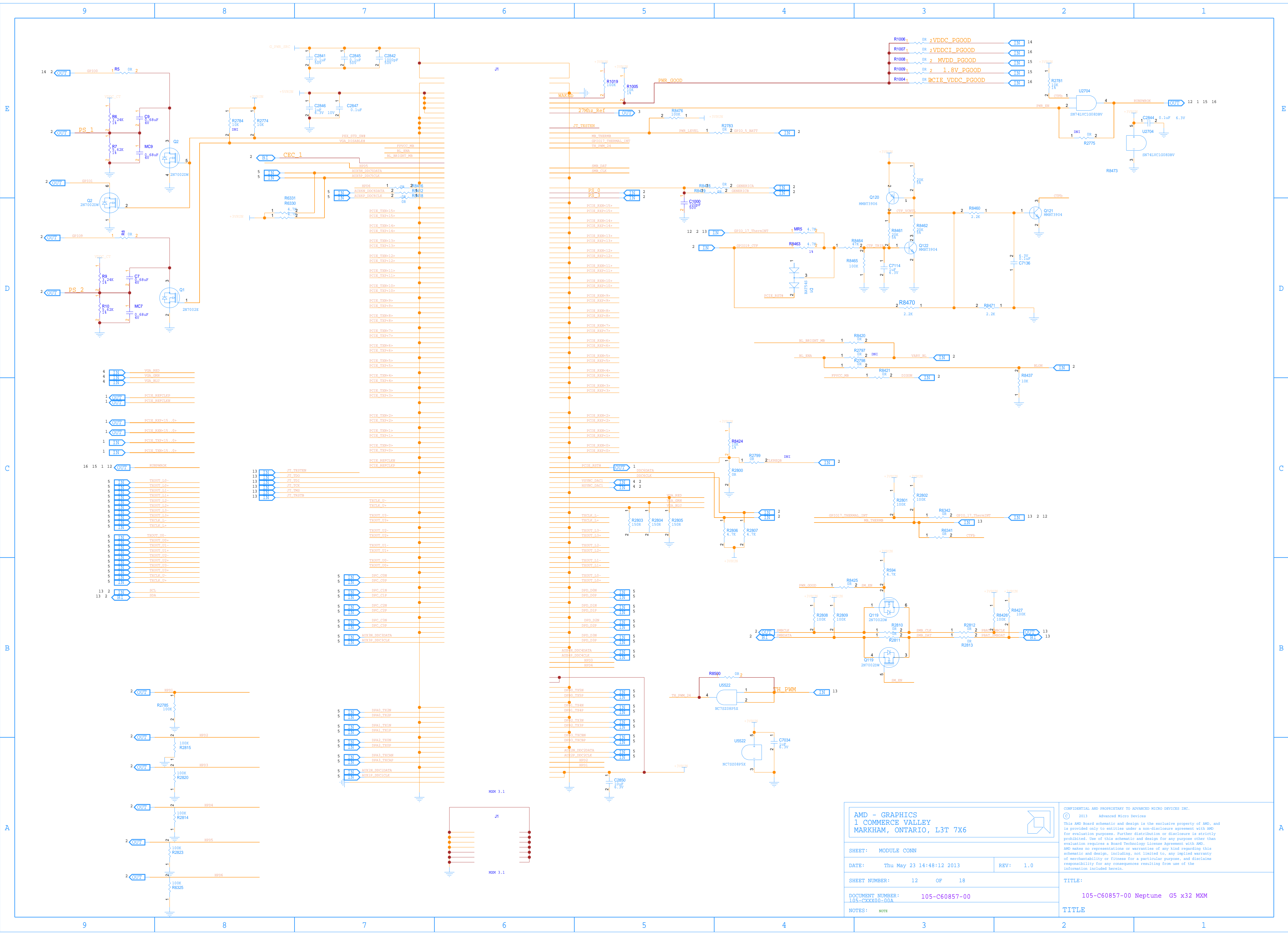
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SHEET: MODULE CONN

DATE: Thu May 23 14:48:12 2013

SHEET NUMBER: 12 OF 18

DOCUMENT NUMBER: 105-C60857-00

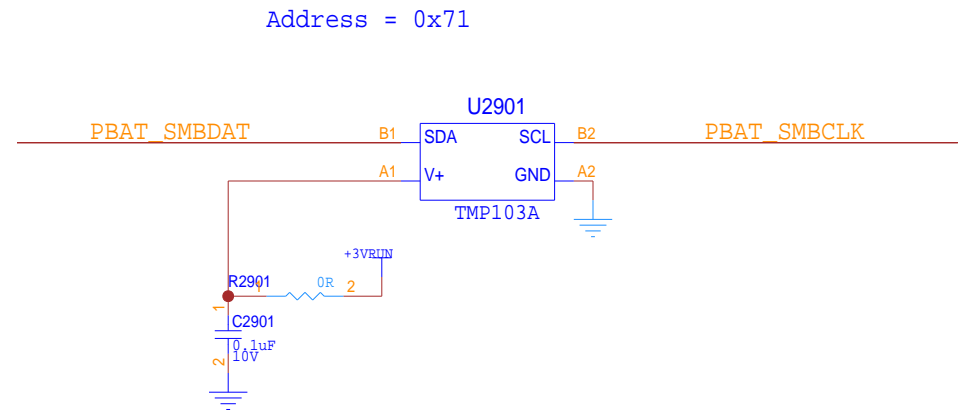
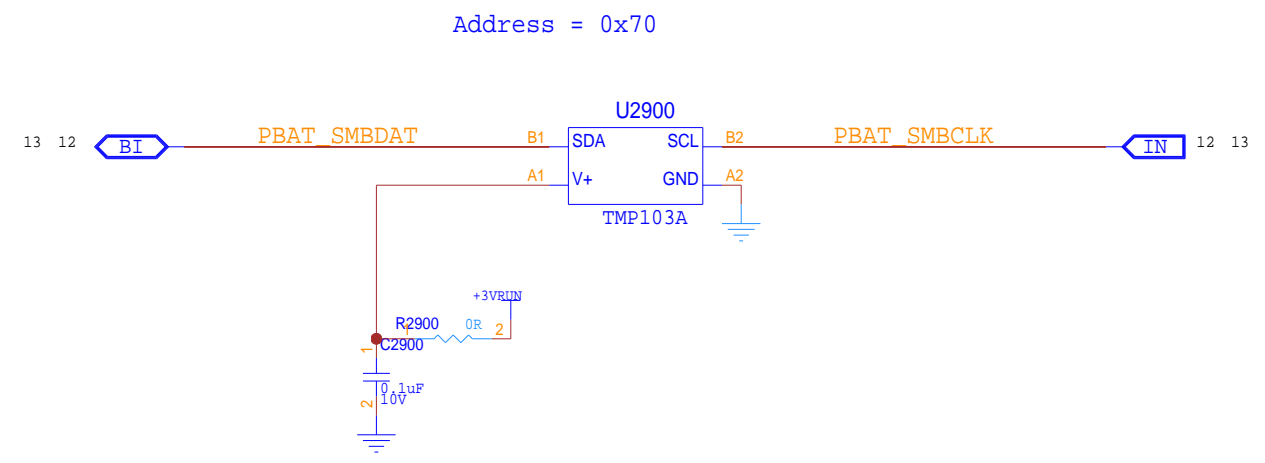
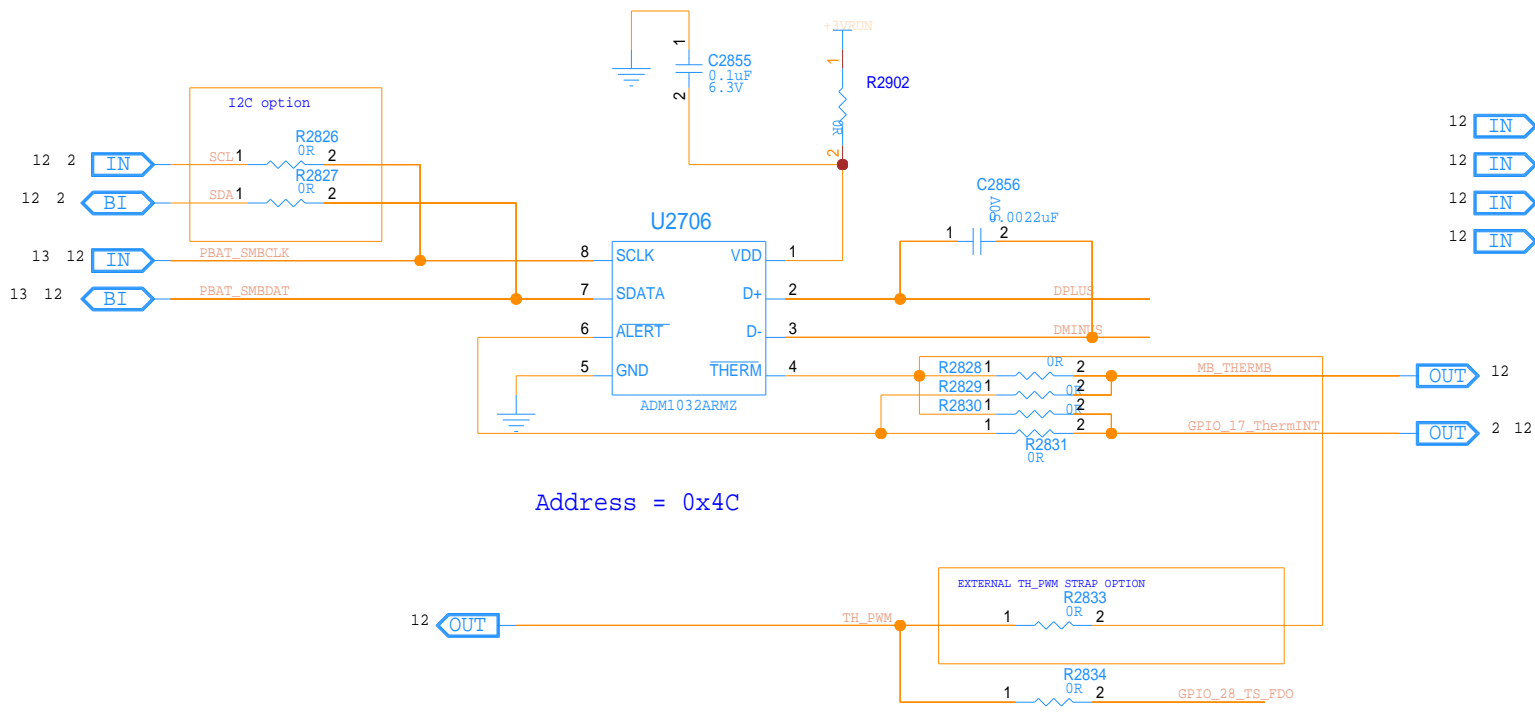
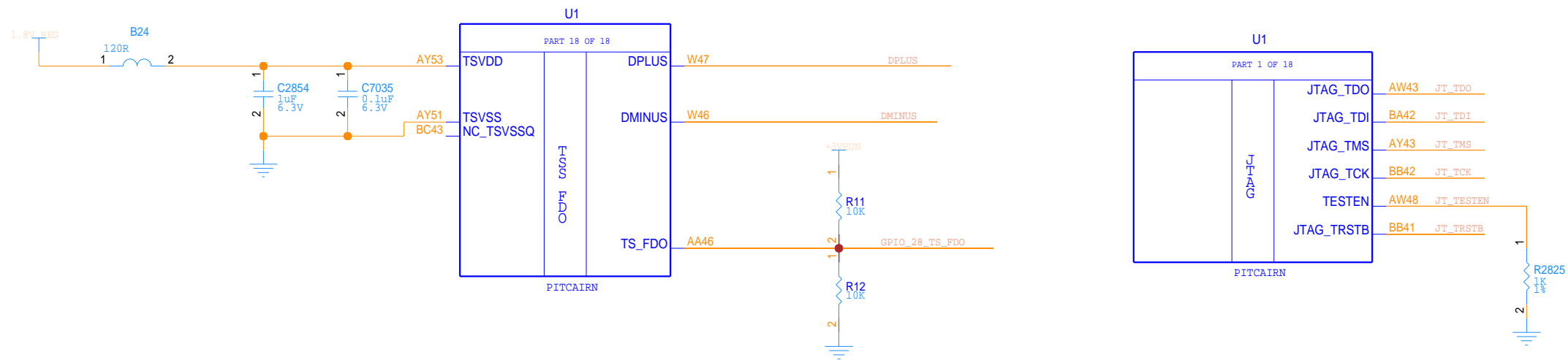
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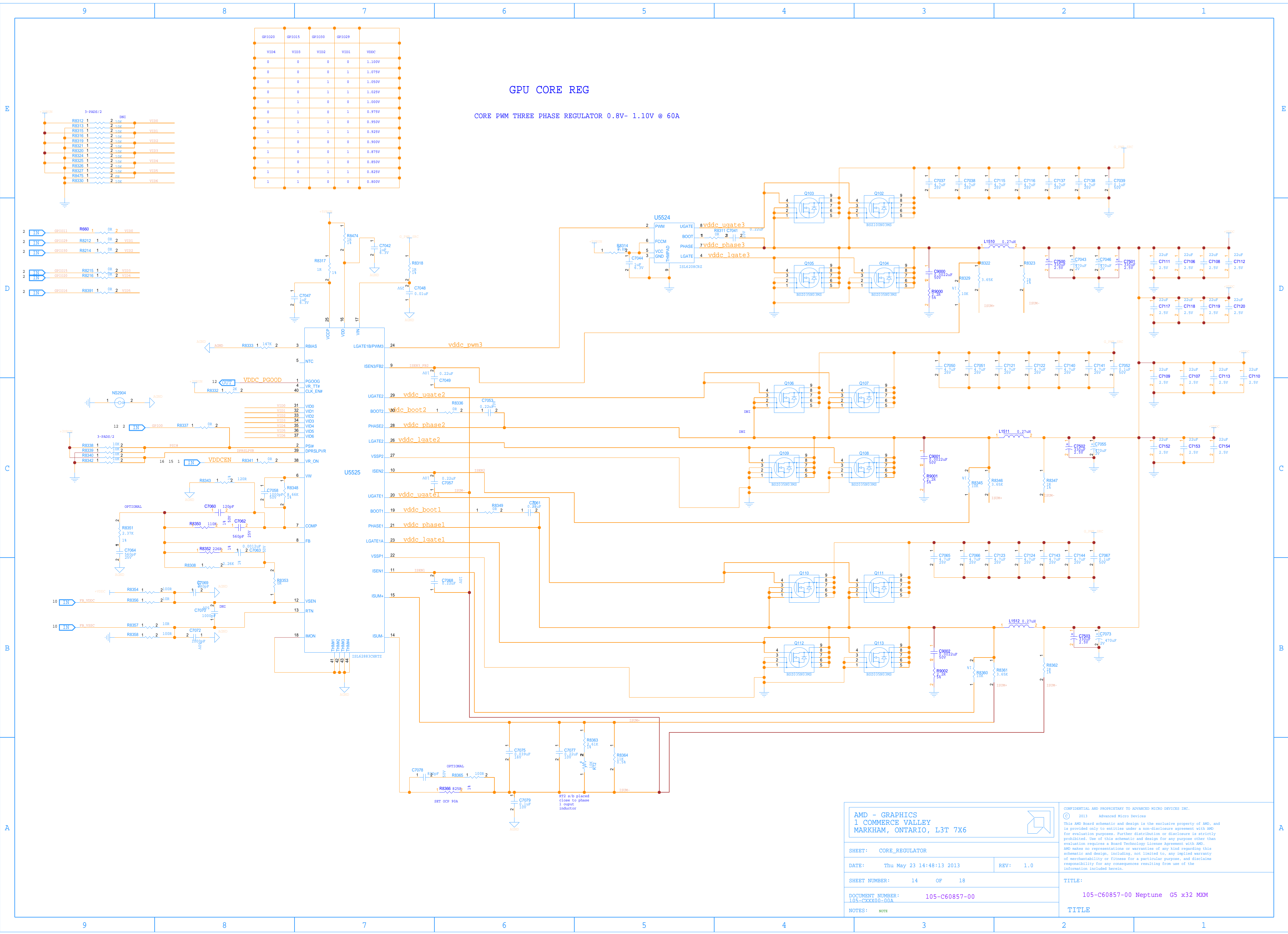
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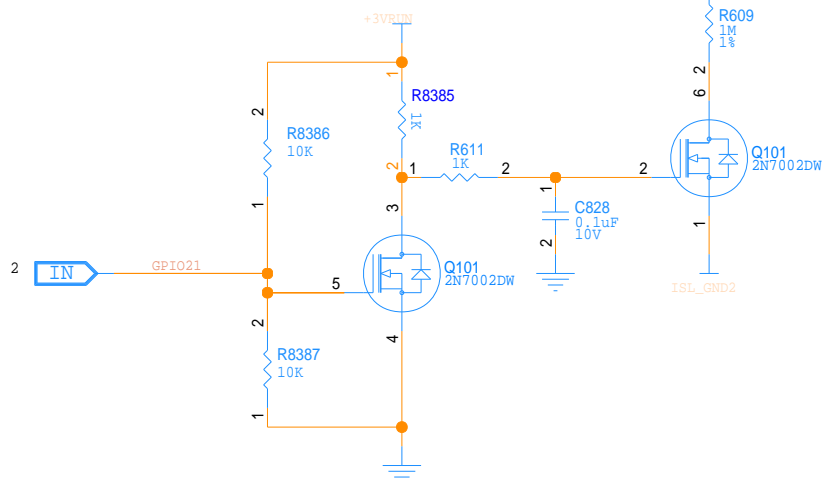
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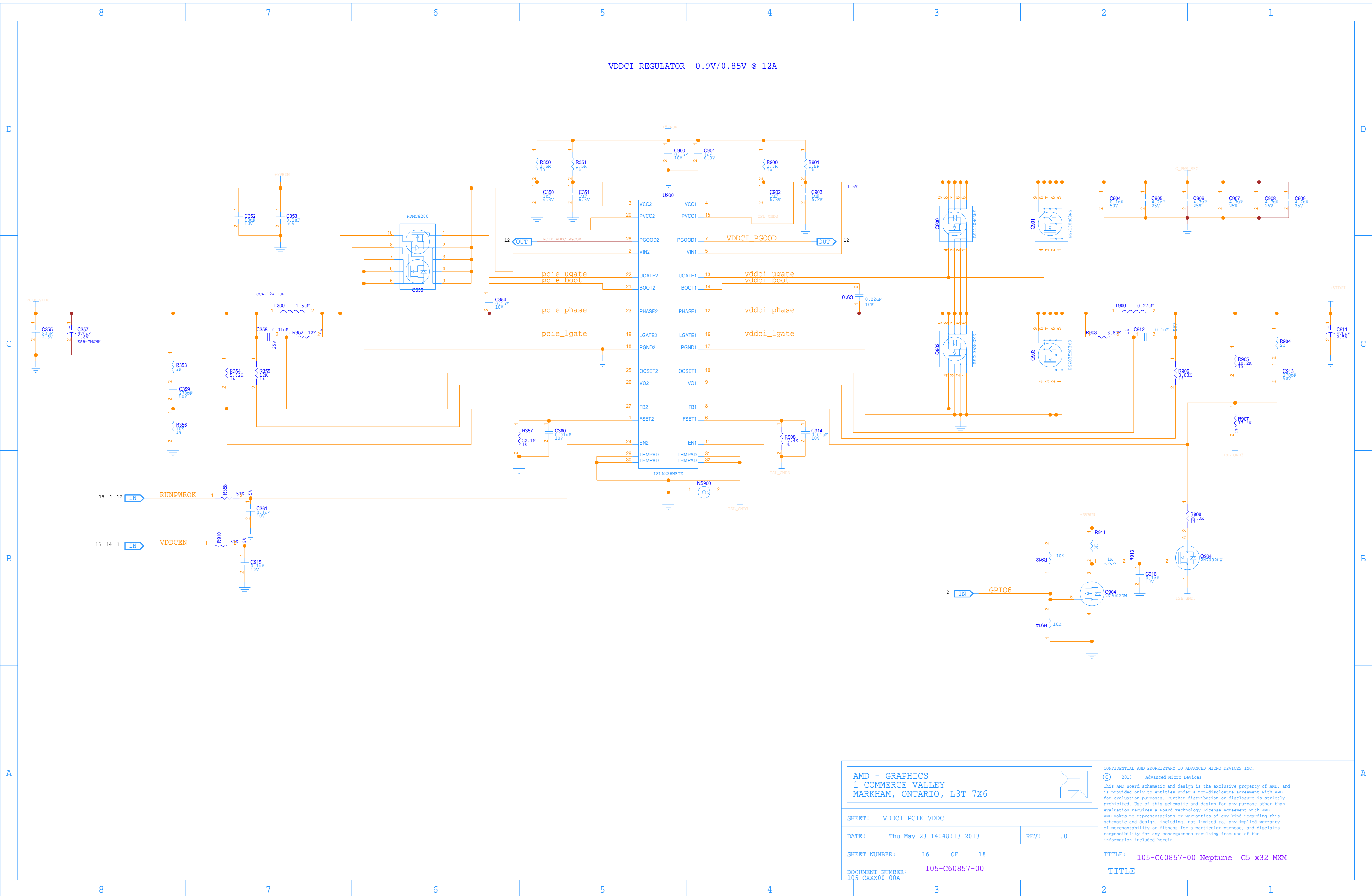


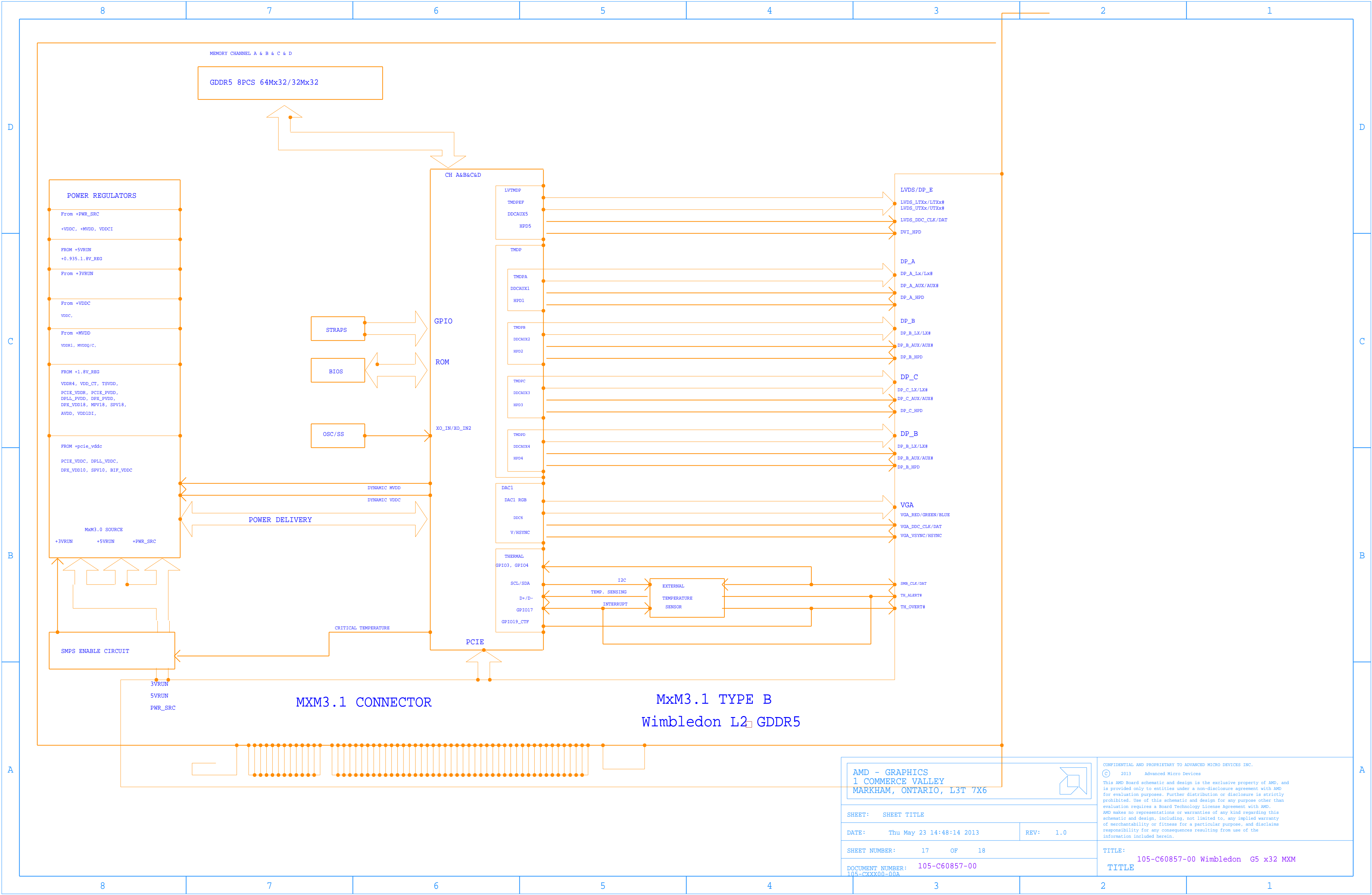
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SHEET: THERM & MISC		TITLE: 105-C60857-00 Neptune G5 x32 MXM	
DATE: Thu May 23 14:48:12 2013		REV: 1.0	
SHEET NUMBER: 13 OF 18		TITLE: 105-C60857-00 Neptune G5 x32 MXM	
DOCUMENT NUMBER: 105-C60857-00		TITLE: 105-C60857-00 Neptune G5 x32 MXM	





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SHEET: MEM & IO_REGULATOR								
DATE:	Thu May 23 14:48:13 2013		REV:	1.0				
SHEET NUMBER:	15	OF	18	TITLE:				
DOCUMENT NUMBER:	105-C60857-00		105-C60857-00 Neptune G5 x32 MXM					
NOTES:	NOTE		TITLE					





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DOCUMENT NUMBER: 105-CXXX00-00A								

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TITLE REVISION HISTORY				ENGINEER: XXX				NOTES: NOTE				CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. C • 2013 Advanced Micro Devices This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.				AMD - GRAPHICS 1 COMMERCE VALLEY MARKHAM, ONTARIO, L3T 7X6											
SCH Rev		PCB Rev		Date		REVISION DESCRIPTON																					
0		00A		03/12/12		Initial release on Base C429 rev.00																					
01		00		05/22/13		HWQ finihsed, release sch to rev.00																					
8				7		6		5		4		3		2		1											