P216-A03 DESIGN -- NV43, 128 MB DDR3, VGA, DVI-I, SD/HDTV, VIVO

PAGE SUMMARY:

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10216-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	000	602-10216-0000-300	NV43-U 500/500MHz 128MB DDR3 8MX32 DVI+VGA+HDTVOUT
2	001	602-10216-0001-300	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
3	002	602-10216-0002-300	NV43-U 350/350MHZ 128MB DDR3 8MX32 DVI+VGA+HDTVOUT
4	003	602-10216-0003-300	NV43-U 400/400MHZ 128MB DDR3 8MX32 DVI+VGA+HDTVOUT
5	004	602-10216-0004-300	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+DVI+HDTVOUT
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

X13

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	TABLE OF CONTENTS & REVISION HISTORY

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10216-0001-300		
ID	p216	PAGE	1 OF 25
NAME	bnichols	DATE	9-SEP-2004

16X PCIe Interface

Place Close to fingers

CN2 NONAME-X16 CON_PCIEXP_X16_EDGE COMMON

U11 NV43-U-A1 BGA820 COMMON — 1/14 PCI_EXPRESS

U14 SN74LVC1G08 SC70-5 COMMON

short duration contention possible
3.3V*2/100 = 108mW

BYPASS

this resistor straddles the TDI/TDO pair

VALUES TBD
Place near balls

Place Close to GPU

Place near balls

Place Near BGA
150-220R@100MHz

VALUES TBD

Place near balls

Place near balls

Place Near BGA

NET	DIFFPAIR	NET_SPACING_RULE
PEX_REFCLK	PEX_REFCLK	20MIL_G2G_30MIL_USER_DIFF
PEX_REFCLK*	PEX_REFCLK*	20MIL_G2G_30MIL_USER_DIFF
GPU_PEX_REFCLK	GPU_PEX_REFCLK	20MIL_G2G_30MIL_USER_DIFF
GPU_PEX_REFCLK*	GPU_PEX_REFCLK	20MIL_G2G_30MIL_USER_DIFF
PEX_TX0	PEX_TX0	20MIL_G2G_30MIL_USER_DIFF
PEX_TX0*	PEX_TX0	20MIL_G2G_30MIL_USER_DIFF
PEX_TX1	PEX_TX1	20MIL_G2G_30MIL_USER_DIFF
PEX_TX1*	PEX_TX1	20MIL_G2G_30MIL_USER_DIFF
PEX_TX2	PEX_TX2	20MIL_G2G_30MIL_USER_DIFF
PEX_TX2*	PEX_TX2	20MIL_G2G_30MIL_USER_DIFF
PEX_TX3	PEX_TX3	20MIL_G2G_30MIL_USER_DIFF
PEX_TX3*	PEX_TX3	20MIL_G2G_30MIL_USER_DIFF
PEX_TX4	PEX_TX4	20MIL_G2G_30MIL_USER_DIFF
PEX_TX4*	PEX_TX4	20MIL_G2G_30MIL_USER_DIFF
PEX_TX5	PEX_TX5	20MIL_G2G_30MIL_USER_DIFF
PEX_TX5*	PEX_TX5	20MIL_G2G_30MIL_USER_DIFF
PEX_TX6	PEX_TX6	20MIL_G2G_30MIL_USER_DIFF
PEX_TX6*	PEX_TX6	20MIL_G2G_30MIL_USER_DIFF
PEX_TX7	PEX_TX7	20MIL_G2G_30MIL_USER_DIFF
PEX_TX7*	PEX_TX7	20MIL_G2G_30MIL_USER_DIFF
PEX_TX8	PEX_TX8	20MIL_G2G_30MIL_USER_DIFF
PEX_TX8*	PEX_TX8	20MIL_G2G_30MIL_USER_DIFF
PEX_TX9	PEX_TX9	20MIL_G2G_30MIL_USER_DIFF
PEX_TX9*	PEX_TX9	20MIL_G2G_30MIL_USER_DIFF
PEX_TX10	PEX_TX10	20MIL_G2G_30MIL_USER_DIFF
PEX_TX10*	PEX_TX10	20MIL_G2G_30MIL_USER_DIFF
PEX_TX11	PEX_TX11	20MIL_G2G_30MIL_USER_DIFF
PEX_TX11*	PEX_TX11	20MIL_G2G_30MIL_USER_DIFF
PEX_TX12	PEX_TX12	20MIL_G2G_30MIL_USER_DIFF
PEX_TX12*	PEX_TX12	20MIL_G2G_30MIL_USER_DIFF
PEX_TX13	PEX_TX13	20MIL_G2G_30MIL_USER_DIFF
PEX_TX13*	PEX_TX13	20MIL_G2G_30MIL_USER_DIFF
PEX_TX14	PEX_TX14	20MIL_G2G_30MIL_USER_DIFF
PEX_TX14*	PEX_TX14	20MIL_G2G_30MIL_USER_DIFF
PEX_TX15	PEX_TX15	20MIL_G2G_30MIL_USER_DIFF
PEX_TX15*	PEX_TX15	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX0	PEX_TXX0	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX0*	PEX_TXX0	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX1	PEX_TXX1	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX1*	PEX_TXX1	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX2	PEX_TXX2	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX2*	PEX_TXX2	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX3	PEX_TXX3	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX3*	PEX_TXX3	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX4	PEX_TXX4	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX4*	PEX_TXX4	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX5	PEX_TXX5	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX5*	PEX_TXX5	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX6	PEX_TXX6	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX6*	PEX_TXX6	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX7	PEX_TXX7	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX7*	PEX_TXX7	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX8	PEX_TXX8	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX8*	PEX_TXX8	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX9	PEX_TXX9	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX9*	PEX_TXX9	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX10	PEX_TXX10	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX10*	PEX_TXX10	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX11	PEX_TXX11	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX11*	PEX_TXX11	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX12	PEX_TXX12	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX12*	PEX_TXX12	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX13	PEX_TXX13	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX13*	PEX_TXX13	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX14	PEX_TXX14	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX14*	PEX_TXX14	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX15	PEX_TXX15	20MIL_G2G_30MIL_USER_DIFF
PEX_TXX15*	PEX_TXX15	20MIL_G2G_30MIL_USER_DIFF
PEX_RX0	PEX_RX0	20MIL_G2G_30MIL_USER_DIFF
PEX_RX0*	PEX_RX0	20MIL_G2G_30MIL_USER_DIFF
PEX_RX1	PEX_RX1	20MIL_G2G_30MIL_USER_DIFF
PEX_RX1*	PEX_RX1	20MIL_G2G_30MIL_USER_DIFF
PEX_RX2	PEX_RX2	20MIL_G2G_30MIL_USER_DIFF
PEX_RX2*	PEX_RX2	20MIL_G2G_30MIL_USER_DIFF
PEX_RX3	PEX_RX3	20MIL_G2G_30MIL_USER_DIFF
PEX_RX3*	PEX_RX3	20MIL_G2G_30MIL_USER_DIFF
PEX_RX4	PEX_RX4	20MIL_G2G_30MIL_USER_DIFF
PEX_RX4*	PEX_RX4	20MIL_G2G_30MIL_USER_DIFF
PEX_RX5	PEX_RX5	20MIL_G2G_30MIL_USER_DIFF
PEX_RX5*	PEX_RX5	20MIL_G2G_30MIL_USER_DIFF
PEX_RX6	PEX_RX6	20MIL_G2G_30MIL_USER_DIFF
PEX_RX6*	PEX_RX6	20MIL_G2G_30MIL_USER_DIFF
PEX_RX7	PEX_RX7	20MIL_G2G_30MIL_USER_DIFF
PEX_RX7*	PEX_RX7	20MIL_G2G_30MIL_USER_DIFF
PEX_RX8	PEX_RX8	20MIL_G2G_30MIL_USER_DIFF
PEX_RX8*	PEX_RX8	20MIL_G2G_30MIL_USER_DIFF
PEX_RX9	PEX_RX9	20MIL_G2G_30MIL_USER_DIFF
PEX_RX9*	PEX_RX9	20MIL_G2G_30MIL_USER_DIFF
PEX_RX10	PEX_RX10	20MIL_G2G_30MIL_USER_DIFF
PEX_RX10*	PEX_RX10	20MIL_G2G_30MIL_USER_DIFF
PEX_RX11	PEX_RX11	20MIL_G2G_30MIL_USER_DIFF
PEX_RX11*	PEX_RX11	20MIL_G2G_30MIL_USER_DIFF
PEX_RX12	PEX_RX12	20MIL_G2G_30MIL_USER_DIFF
PEX_RX12*	PEX_RX12	20MIL_G2G_30MIL_USER_DIFF
PEX_RX13	PEX_RX13	20MIL_G2G_30MIL_USER_DIFF
PEX_RX13*	PEX_RX13	20MIL_G2G_30MIL_USER_DIFF
PEX_RX14	PEX_RX14	20MIL_G2G_30MIL_USER_DIFF
PEX_RX14*	PEX_RX14	20MIL_G2G_30MIL_USER_DIFF
PEX_RX15	PEX_RX15	20MIL_G2G_30MIL_USER_DIFF
PEX_RX15*	PEX_RX15	20MIL_G2G_30MIL_USER_DIFF

MIN_LINE_WIDTH

NVVDD_SENSE	10MIL	
GND_SENSE	10MIL	
PEX_PLL_VDD	10MIL	

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	PCI EXPRESS 16X, NVVDD DECOUPLING CAPS,PEX_IOVDD/Q DECOUPLING CAPS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10216-0001-300		
ID	p216	PAGE	2 OF 25
NAME	bnichols	DATE	9-SEP-2004

U11
NV43-U-A1
BGA820
COMMON

ALL FBVDD PINS ARE NC ON NV43 DESKTOP G3 PACKAGE

2/14 FBA

4.4B<> 4.1G<>	BI	FBAD<63..0>	0	FBAD<0>	N27
			1	FBAD<1>	M27
			2	FBAD<2>	N26
			3	FBAD<3>	L29
			4	FBAD<4>	K27
			5	FBAD<5>	K28
			6	FBAD<6>	J29
			7	FBAD<7>	J28
			8	FBAD<8>	P30
			9	FBAD<9>	N31
			10	FBAD<10>	N30
			11	FBAD<11>	N32
			12	FBAD<12>	L31
			13	FBAD<13>	L30
			14	FBAD<14>	J30
			15	FBAD<15>	L32
			16	FBAD<16>	H30
			17	FBAD<17>	K30
			18	FBAD<18>	H31
			19	FBAD<19>	F30
			20	FBAD<20>	H32
			21	FBAD<21>	E31
			22	FBAD<22>	D30
			23	FBAD<23>	E30
			24	FBAD<24>	H28
			25	FBAD<25>	H29
			26	FBAD<26>	E29
			27	FBAD<27>	J27
			28	FBAD<28>	F27
			29	FBAD<29>	E27
			30	FBAD<30>	E28
			31	FBAD<31>	F28
			32	FBAD<32>	AD29
			33	FBAD<33>	AE29
			34	FBAD<34>	AD28
			35	FBAD<35>	AE28
			36	FBAD<36>	AB29
			37	FBAD<37>	AA30
			38	FBAD<38>	Y28
			39	FBAD<39>	AB30
			40	FBAD<40>	AM30
			41	FBAD<41>	AF30
			42	FBAD<42>	AJ31
			43	FBAD<43>	AJ30
			44	FBAD<44>	AJ32
			45	FBAD<45>	AK29
			46	FBAD<46>	AM31
			47	FBAD<47>	AL30
			48	FBAD<48>	AE32
			49	FBAD<49>	AE30
			50	FBAD<50>	AE31
			51	FBAD<51>	AD30
			52	FBAD<52>	AC31
			53	FBAD<53>	AG32
			54	FBAD<54>	AB32
			55	FBAD<55>	AB31
			56	FBAD<56>	AG27
			57	FBAD<57>	AF28
			58	FBAD<58>	AH28
			59	FBAD<59>	AG28
			60	FBAD<60>	AG29
			61	FBAD<61>	AD27
			62	FBAD<62>	AF27
			63	FBAD<63>	AE28
4.4B<> 4.1G<>	OUT	FBADQM<7..0>	0	FBADQM<0>	M29
			1	FBADQM<1>	M30
			2	FBADQM<2>	G30
			3	FBADQM<3>	F29
			4	FBADQM<4>	AA29
			5	FBADQM<5>	AK30
			6	FBADQM<6>	AC30
			7	FBADQM<7>	AG30
4.5B<> 4.1G<>	BI	FBADQS_WP<7..0>	0	FBADQS_WP<0>	L28
			1	FBADQS_WP<1>	K31
			2	FBADQS_WP<2>	G32
			3	FBADQS_WP<3>	G28
			4	FBADQS_WP<4>	AB28
			5	FBADQS_WP<5>	AL32
			6	FBADQS_WP<6>	AF32
			7	FBADQS_WP<7>	AH30
4.4B<> 4.1G<>	BI	FBADQS_RN<7..0>	0	FBADQS_RN<0>	M28
			1	FBADQS_RN<1>	K32
			2	FBADQS_RN<2>	G31
			3	FBADQS_RN<3>	G27
			4	FBADQS_RN<4>	AA28
			5	FBADQS_RN<5>	AL31
			6	FBADQS_RN<6>	AF31
			7	FBADQS_RN<7>	AH29

FBVDD	A12	NTP_GPU_A12	
FBVDD	A15	NTP_GPU_A15	
FBVDD	A18	NTP_GPU_A18	
FBVDD	A21	NTP_GPU_A21	
FBVDD	A24	NTP_GPU_A24	
FBVDD	A27	NTP_GPU_A27	
FBVDD	A3	NTP_GPU_A3	
FBVDD	A30	NTP_GPU_A30	
FBVDD	A6	NTP_GPU_A6	
FBVDD	A9	NTP_GPU_A9	
FBVDD	AA32	NTP_GPU_AA32	
FBVDD	AD32	NTP_GPU_AD32	
FBVDD	AG32	NTP_GPU_AG32	
FBVDD	AK32	NTP_GPU_AK32	
FBVDD	C32	NTP_GPU_C32	
FBVDD	F32	NTP_GPU_F32	
FBVDD	J32	NTP_GPU_J32	
FBVDD	M32	NTP_GPU_M32	
FBVDD	R32	NTP_GPU_R32	
FBVDD	V32	NTP_GPU_V32	
FBVDDQ	AA25		
FBVDDQ	AA26		
FBVDDQ	AB25		
FBVDDQ	AB26		
FBVDDQ	G11		
FBVDDQ	G12		
FBVDDQ	G15		
FBVDDQ	G18		
FBVDDQ	G21		
FBVDDQ	G22		
FBVDDQ	H11		
FBVDDQ	H12		
FBVDDQ	H15		
FBVDDQ	H18		
FBVDDQ	H21		
FBVDDQ	H22		
FBVDDQ	L25		
FBVDDQ	L26		
FBVDDQ	M25		
FBVDDQ	M26		
FBVDDQ	R25		
FBVDDQ	R26		
FBVDDQ	V25		
FBVDDQ	V26		

FBA_CMD0	P32	FBA_CMD<0>	FBA_CMD<26..0>	OUT	4.1A< 4.1G<
FBA_CMD1	U27	FBA_CMD<1>	1		
FBA_CMD2	P31	FBA_CMD<2>	2		
FBA_CMD3	U30	FBA_CMD<3>	3		
FBA_CMD4	Y31	FBA_CMD<4>	4		
FBA_CMD5	W32	FBA_CMD<5>	5		
FBA_CMD6	W31	FBA_CMD<6>	6		
FBA_CMD7	T32	NTP_FBA_CMD<7>			
FBA_CMD8	V27	FBA_CMD<8>	8		
FBA_CMD9	T28	FBA_CMD<9>	9		
FBA_CMD10	T31	FBA_CMD<10>	10		
FBA_CMD11	U32	FBA_CMD<11>	11		
FBA_CMD12	W29	FBA_CMD<12>	12		
FBA_CMD13	W30	FBA_CMD<13>	13		
FBA_CMD14	T27	FBA_CMD<14>	14		
FBA_CMD15	V28	FBA_CMD<15>	15		
FBA_CMD16	V30	FBA_CMD<16>	16		
FBA_CMD17	U31	FBA_CMD<17>	17		
FBA_CMD18	R27	FBA_CMD<18>	18		
FBA_CMD19	V29	FBA_CMD<19>	19		
FBA_CMD20	T30	FBA_CMD<20>	20		
FBA_CMD21	W28	FBA_CMD<21>	21		
FBA_CMD22	R29	FBA_CMD<22>	22		
FBA_CMD23	R30	FBA_CMD<23>	23		
FBA_CMD24	P29	FBA_CMD<24>	24		
FBA_CMD25	U28	FBA_CMD<25>	25		
FBA_CMD26	Y32	NTP_FBA_CMD<26>			
FBA_CLK0	P28	FBA_CLK0		OUT	
FBA_CLK0	R28	FBA_CLK0*		OUT	
FBA_CLK1	P27	FBA_CLK1		OUT	
FBA_CLK1	AA27	FBA_CLK1*		OUT	
RFU	Y30	TP_FBA_DBI0			
RFU	AC26	TP_FBA_DBI1			
FBA_DEBUG	AC27	TP_FBA_DEBUG			
FBA_REFCLK	D32	FBA_REFCLK			
FBA_REFCLK	D31	FBA_REFCLK*			
FBA_PLLVDD	G23	FBA_PLLVDD			
FBA_PLLAVDD	G25	FBA_PLLAVDD			
FBA_PLLGND	G24				
FBA_VREF	E32	FB_VREF1			

TP NOW

PLACE BELOW GPU

FBVDD
C754 0.47UF 6.3V 10% X5R 0402 COMMON
C708 0.47UF 6.3V 10% X5R 0402 COMMON
C806 .1UF 10V 10% X5R 0402 COMMON
C730 .1UF 10V 10% X5R 0402 COMMON
C50 .1UF 10V 10% X5R 0402 COMMON
C5 .1UF 10V 10% X5R 0402 COMMON
C68 .1UF 10V 10% X5R 0402 COMMON
C6 .1UF 10V 10% X5R 0402 COMMON
C824 1UF 10V 10% X7R 0603 COMMON
C705 0.47UF 6.3V 10% X5R 0402 COMMON
C750 0.47UF 6.3V 10% X5R 0402 COMMON
C707 .1UF 10V 10% X5R 0402 COMMON
C755 .1UF 10V 10% X5R 0402 COMMON
C697 1UF 10V 10% X7R 0603 COMMON
C792 .1UF 10V 10% X5R 0402 COMMON
C704 .1UF 10V 10% X5R 0402 COMMON
C698 .1UF 10V 10% X5R 0402 COMMON
C722 0.47UF 6.3V 10% X5R 0402 COMMON
C800 0.47UF 6.3V 10% X5R 0402 COMMON
GND

NET	DIFFPAIR	MIN_LINE_WIDTH	NET_SPACING_RULE
FBA_REFCLK		4MIL	10MIL
FBA_REFCLK*		4MIL	10MIL
FBA_PLLVDD		10MIL	
FBA_PLLAVDD		10MIL	

FBVDD
C740 10UF 6.3V 20% X5R 0805 COMMON
C856 10UF 6.3V 20% X5R 0805 COMMON
C594 10UF 6.3V 20% X5R 0805 COMMON
C597 10UF 6.3V 20% X5R 0805 COMMON
GND

PLACE MIDWAY BETWEEN GPU AND MEMORY

PLACE NEAR GPU

FBVDD
R638 10K 5% 0402 NO STUFF
FBA_CMD<11>
R640 10K 5% 0402 COMMON
GND

CKE Stuff options for DDR3 configation for on-die terminations at the memory
IMPORTANT FOR POWER ON INITIALIZATION OF DDR3 MEMS

DDR3: DETERMINES THE ODT VALUE FOR ADDR AND CONTROL PINS
CKE = 0 --> ODT = ZQ/2
CKE = 1 --> ODT = ZQ

PLACE close to GPU

4.2A< 4.1G<
4.2D< 4.1G<
4.1G< 4.2D<
FBVDD
R596 100 1% 0402 NO STUFF
R599 100 1% 0402 NO STUFF
R593 100 1% 0402 COMMON
R601 100 1% 0402 COMMON
GND

FB_DLLVDD
ON NV3x version's of G3
FB_DLLVDD will be routed on FB_PLLVDD

PLACE close to balls

FBA_PLLVDD
150-220R@100MHz
A3V3
LB507 BEAD_0603 COMMON
C689 .01UF 16V 10% X7R 0402 COMMON
C685 .1UF 10V 10% X5R 0402 COMMON
C674 1UF 6.3V 10% X5R 0402 COMMON
C654 4.7UF 6.3V 10% X5R 0603 COMMON
GND

FBA_PLLAVDD
150-220R@100MHz
NVVDD
LB509 BEAD_0603 COMMON
C710 .01UF 16V 10% X7R 0402 COMMON
C692 .1UF 10V 10% X5R 0402 COMMON
C672 1UF 6.3V 10% X5R 0402 COMMON
C662 4.7UF 6.3V 10% X5R 0603 COMMON
GND

FBA_AVDD is TBD. This may not be hooked up on the Package.

FBVDD
Rtop 1K 1% 0402 COMMON
R602
C652 .1UF 10V 10% X5R 0402 NO STUFF
Rbot 2.55K 1% 0402 CHANGED
R607
C660 .1UF 10V 10% X5R 0402 COMMON
GND

VREF = FBVDDQ * Rbot/(Rtop + Rbot)

VREF = 0.70 * FBVDDQ
DDR3: 1.26V = 1.8V * 2.7K/(1.15K + 2.7K)

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	FBA MEMORY INTERFACE, GPU FBVDD/Q DECOUPLING CAPS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10216-0001-300		
ID	p216	PAGE	3 OF 25
NAME	bnichols	DATE	9-SEP-2004

FrameBuffer: Partition A 8Mx32 BGA144 DDR3

A-CSO-LOW-32bit

U8 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

4.1G< 3.2D> IN FBA_CMD<26..0>

15	FBA_CMD<15>	M5	RAS
25	FBA_CMD<25>	N6	CAS
9	FBA_CMD<9>	N9	WE
8 CSO	FBA_CMD<8>	M10	CS
1	FBA_CMD<1>	N2	A0
3	FBA_CMD<3>	N3	A1
2	FBA_CMD<2>	M3	A2
0	FBA_CMD<0>	L3	A3
24	FBA_CMD<24>	L12	A4
22	FBA_CMD<22>	M12	A5
21	FBA_CMD<21>	N12	A6
23	FBA_CMD<23>	N13	A7
19	FBA_CMD<19>	N11	A8
20	FBA_CMD<20>	M11	A9
17	FBA_CMD<17>	M4	A10
16	FBA_CMD<16>	N4	A11
14	FBA_CMD<14>	L9	NC/A<12>
10	FBA_CMD<10>	N5	BA<0>
18	FBA_CMD<18>	N10	BA<1>
	TP_FBA0_BA<2>	L6	NC/BA<2>
11	FBA_CMD<11>	M7	CKE
	FBA_CLK0	N7	CLK
	FBA_CLK0*	N8	CLK
	TP_FBA0_NC1	E3	NC/RFU
	TP_FBA0_NC2	E12	NC/RFU
	TP_FBA0_NC3	M8	NC/RFU
12	FBA_CMD<12>	M6	RESET
	FBA_ZQ0	M9	ZQ

Low Sub-Partition

4.1G< 3.3D> IN
4.1G< 3.4D> IN

R643 10K 5% 0402 COMMON — GND
R61 240 1% 0603 COMMON — GND

THERM: F6 F7 F8 F9 G6 G7 G8 G9 H6 H7 H8 H9 J6 J7 J8 J9

FBVDD: D7 D8 E4 E11 L4 L7 L8 L11

VDDQ: C4 C5 C7 C8 C10 C11 F4 F11 G4 G11 H4 H11 J4 J11 K4 K11

VSSQ: B4 B11 D4 D5 D6 D9 D10 D11 E6 E9 F5 F10 G5 G10 H5 H10 J5 J10 K5 K10 — GND

VSS: E5 E7 E8 E10 K6 K7 K8 K9 L5 L10

VREF: M2 FBA_VREF_DATA0, M13 FBA_VREF_ADDR0

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: ZQ = 6x desired output
impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

VREF:
M2 - DATA
M13 - ADDR

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 2.7K/(1.15K + 2.7K)

FBA Partition

Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!

FBA_CMD<26..0>

2	FBA_CMD<2>	R627	120 COMMON 5% 0402
0	FBA_CMD<0>	R628	120 COMMON 5% 0402
24	FBA_CMD<24>	R611	120 COMMON 5% 0402
22	FBA_CMD<22>	R610	120 COMMON 5% 0402
13	FBA_CMD<13>	R674	120 COMMON 5% 0402
4	FBA_CMD<4>	R675	120 COMMON 5% 0402
5	FBA_CMD<5>	R647	120 COMMON 5% 0402
6	FBA_CMD<6>	R646	120 COMMON 5% 0402
	FBA_CLK0	R68	60.4 CHANGED 1% 0402
	FBA_CLK0*	R67	60.4 CHANGED 1% 0402
	FBA_CLK1	R94	60.4 CHANGED 1% 0402
	FBA_CLK1*	R92	60.4 CHANGED 1% 0402

Hi Sub-Partition

4.1G< 3.4D> IN
4.1G< 3.4D> IN

FBVDD

R639 1K 1% 0402 COMMON — R1
R635 2.55K 1% 0402 CHANGED — R2
C772 .1UF 10V 10% X5R 0402 NO STUFF
C753 .1UF 10V 10% X5R 0402 COMMON
GND

R597 1K 1% 0402 COMMON — R1
R605 2.55K 1% 0402 CHANGED — R2
C648 .1UF 10V 10% X5R 0402 NO STUFF
C655 .1UF 10V 10% X5R 0402 COMMON
GND

A-CSO-HI-32bit

U12 DDR3BGA144 PACK_TYPE=BGA144 VERSION=BGA144 CHANGED

FBA_CMD<26..0>

15	FBA_CMD<15>	M5	RAS
25	FBA_CMD<25>	N6	CAS
9	FBA_CMD<9>	N9	WE
8 CSO	FBA_CMD<8>	M10	CS
1	FBA_CMD<1>	N2	A0
3	FBA_CMD<3>	N3	A1
13	FBA_CMD<13>	M3	A2
4	FBA_CMD<4>	L3	A3
5	FBA_CMD<5>	L12	A4
6	FBA_CMD<6>	M12	A5
21	FBA_CMD<21>	N12	A6
23	FBA_CMD<23>	N13	A7
19	FBA_CMD<19>	N11	A8
20	FBA_CMD<20>	M11	A9
17	FBA_CMD<17>	M4	A10
16	FBA_CMD<16>	N4	A11
14	FBA_CMD<14>	L9	NC/A<12>
10	FBA_CMD<10>	N5	BA<0>
18	FBA_CMD<18>	N10	BA<1>
	TP_FBA1_BA<2>	L6	NC/BA<2>
11	FBA_CMD<11>	M7	CKE
	FBA_CLK1	N7	CLK
	FBA_CLK1*	N8	CLK
	TP_FBA1_NC1	E3	NC/RFU
	TP_FBA1_NC2	E12	NC/RFU
	TP_FBA1_NC3	M8	NC/RFU
	FBA_CMD<12>	M6	RESET
	FBA_ZQ1	M9	ZQ

4.1G< 3.4D> IN
4.1G< 3.4D> IN

R88 240 1% 0603 COMMON — GND

THERM: F6 F7 F8 F9 G6 G7 G8 G9 H6 H7 H8 H9 J6 J7 J8 J9

FBVDD: D7 D8 E4 E11 L4 L7 L8 L11

VDDQ: C4 C5 C7 C8 C10 C11 F4 F11 G4 G11 H4 H11 J4 J11 K4 K11

VSSQ: B4 B11 D4 D5 D6 D9 D10 D11 E6 E9 F5 F10 G5 G10 H5 H10 J5 J10 K5 K10 — GND

VSS: E5 E7 E8 E10 K6 K7 K8 K9 L5 L10

VREF: M2 FBA_VREF_DATA1, M13 FBA_VREF_ADDR1

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: ZQ = 6x desired output
impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 2.7K/(1.15K + 2.7K)

FBVDD

R689 1K 1% 0402 COMMON — R1
R684 2.55K 1% 0402 CHANGED — R2
C907 .1UF 10V 10% X5R 0402 NO STUFF
C898 .1UF 10V 10% X5R 0402 COMMON
GND

R642 1K 1% 0402 COMMON — R1
R644 2.55K 1% 0402 CHANGED — R2
C803 .1UF 10V 10% X5R 0402 NO STUFF
C818 .1UF 10V 10% X5R 0402 COMMON
GND

144BGA CMD Mapping

CMD	ADDR	
CMD15	RAS*	
CMD25	CAS*	
CMD9	WE*	
CMD11	CKE	
CMD12	RESET	
CMD8	CS0*	
CMD7	CS1**notused	
CMD1	A<0>	
CMD3	A<1>	
CMD2	A<2>	Low Sub-Partition
CMD0	A<3>	Low Sub-Partition
CMD24	A<4>	Low Sub-Partition
CMD22	A<5>	Low Sub-Partition
CMD13	A<2>	Hi Sub-Partition
CMD4	A<3>	Hi Sub-Partition
CMD5	A<4>	Hi Sub-Partition
CMD6	A<5>	Hi Sub-Partition
CMD21	A<6>	
CMD23	A<7>	
CMD19	A<8>	
CMD20	A<9>	
CMD17	A<10	
CMD16	A<11>	
CMD14	A<12>	
CMD10	BA0	
CMD18	BA1	

FBA Data

4.1G<> 3.1A<> BI FBAD<63..0>

4.1G<> 3.3A<> BI FBADQM<7..0>

4.1G<> 3.4A<> BI FBADQS_RN<7..0>

4.1G<> 3.3A<> BI FBADQS_WP<7..0>

U8 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

0	FBAD<0>	L2	DQ0
1	FBAD<1>	K2	DQ1
2	FBAD<2>	G2	DQ2
3	FBAD<3>	J2	DQ3
4	FBAD<4>	F2	DQ4
5	FBAD<5>	F3	DQ5
6	FBAD<6>	G3	DQ6
7	FBAD<7>	K3	DQ7
	FBADQM<0>	J3	DQM
	FBADQS_RN<0>	H3	DQSR
	FBADQS_WP<0>	H2	DQSW

U8 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

8	FBAD<8>	E2	DQ0
9	FBAD<9>	D2	DQ1
10	FBAD<10>	C2	DQ2
11	FBAD<11>	D3	DQ3
12	FBAD<12>	B5	DQ4
13	FBAD<13>	B6	DQ5
14	FBAD<14>	B7	DQ6
15	FBAD<15>	C6	DQ7
	FBADQM<1>	C3	DQM
	FBADQS_RN<1>	B3	DQSR
	FBADQS_WP<1>	B2	DQSW

U8 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

16	FBAD<16>	B10	DQ0
17	FBAD<17>	B8	DQ1
18	FBAD<18>	B9	DQ2
19	FBAD<19>	C13	DQ3
20	FBAD<20>	C9	DQ4
21	FBAD<21>	D12	DQ5
22	FBAD<22>	E13	DQ6
23	FBAD<23>	D13	DQ7
	FBADQM<2>	C12	DQM
	FBADQS_RN<2>	B12	DQSR
	FBADQS_WP<2>	B13	DQSW

U8 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

24	FBAD<24>	F12	DQ0
25	FBAD<25>	G12	DQ1
26	FBAD<26>	G13	DQ2
27	FBAD<27>	F13	DQ3
28	FBAD<28>	J13	DQ4
29	FBAD<29>	K12	DQ5
30	FBAD<30>	L13	DQ6
31	FBAD<31>	K13	DQ7
	FBADQM<3>	J12	DQM
	FBADQS_RN<3>	H12	DQSR
	FBADQS_WP<3>	H13	DQSW

U12 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

32	FBAD<32>	G12	DQ0
33	FBAD<33>	L13	DQ1
34	FBAD<34>	K12	DQ2
35	FBAD<35>	J13	DQ3
36	FBAD<36>	G13	DQ4
37	FBAD<37>	K13	DQ5
38	FBAD<38>	F12	DQ6
39	FBAD<39>	F13	DQ7
	FBADQM<4>	J12	DQM
	FBADQS_RN<4>	H12	DQSR
	FBADQS_WP<4>	H13	DQSW

U12 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

40	FBAD<40>	D2	DQ0
41	FBAD<41>	B7	DQ1
42	FBAD<42>	B6	DQ2
43	FBAD<43>	B5	DQ3
44	FBAD<44>	C6	DQ4
45	FBAD<45>	E2	DQ5
46	FBAD<46>	D3	DQ6
47	FBAD<47>	C2	DQ7
	FBADQM<5>	C3	DQM
	FBADQS_RN<5>	B3	DQSR
	FBADQS_WP<5>	B2	DQSW

U12 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

48	FBAD<48>	B9	DQ0
49	FBAD<49>	B8	DQ1
50	FBAD<50>	C9	DQ2
51	FBAD<51>	B10	DQ3
52	FBAD<52>	D12	DQ4
53	FBAD<53>	C13	DQ5
54	FBAD<54>	D13	DQ6
55	FBAD<55>	E13	DQ7
	FBADQM<6>	C12	DQM
	FBADQS_RN<6>	B12	DQSR
	FBADQS_WP<6>	B13	DQSW

U12 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

56	FBAD<56>	L2	DQ0
57	FBAD<57>	F3	DQ1
58	FBAD<58>	G2	DQ2
59	FBAD<59>	K2	DQ3
60	FBAD<60>	F2	DQ4
61	FBAD<61>	K3	DQ5
62	FBAD<62>	J2	DQ6
63	FBAD<63>	G3	DQ7
	FBADQM<7>	J3	DQM
	FBADQS_RN<7>	H3	DQSR
	FBADQS_WP<7>	H2	DQSW

NET / DIFFPAIR / MIN_LINE_WIDTH / SPACING

		NET	DIFFPAIR	MIN_LINE_WIDTH	SPACING
4.2A< 3.3D>	IN	FBA_CLK0	FBA_CLK0	5MIL	15MIL_G2G_25MIL
4.2A< 3.4D>	IN	FBA_CLK0*	FBA_CLK0	5MIL	15MIL_G2G_25MIL
4.2D< 3.4D>	IN	FBA_CLK1	FBA_CLK1	5MIL	15MIL_G2G_25MIL
4.2D< 3.4D>	IN	FBA_CLK1*	FBA_CLK1	5MIL	15MIL_G2G_25MIL
4.1A< 3.2D>	IN	FBA_CMD<26..0>			15MIL
4.4B<> 3.1A<>	BI	FBAD<63..0>			15MIL
4.4B<> 3.3A>	BI	FBADQM<7..0>			15MIL
4.4B<> 3.4A<>	BI	FBADQS_RN<0>	FBADQS_RN0		15MIL
4.5B<> 3.3A<>	BI	FBADQS_WP<0>	FBADQS_WP0		15MIL
4.4B<> 3.4A<>	BI	FBADQS_RN<1>	FBADQS_RN1		15MIL
4.5B<> 3.3A<>	BI	FBADQS_WP<1>	FBADQS_WP1		15MIL
4.4B<> 3.4A<>	BI	FBADQS_RN<2>	FBADQS_RN2		15MIL
4.5B<> 3.3A<>	BI	FBADQS_WP<2>	FBADQS_WP2		15MIL
4.4B<> 3.4A<>	BI	FBADQS_RN<3>	FBADQS_RN3		15MIL
4.5B<> 3.3A<>	BI	FBADQS_WP<3>	FBADQS_WP3		15MIL
4.4B<> 3.4A<>	BI	FBADQS_RN<4>	FBADQS_RN4		15MIL
4.5B<> 3.3A<>	BI	FBADQS_WP<4>	FBADQS_WP4		15MIL
4.4B<> 3.4A<>	BI	FBADQS_RN<5>	FBADQS_RN5		15MIL
4.5B<> 3.3A<>	BI	FBADQS_WP<5>	FBADQS_WP5		15MIL
4.4B<> 3.4A<>	BI	FBADQS_RN<6>	FBADQS_RN6		15MIL
4.5B<> 3.3A<>	BI	FBADQS_WP<6>	FBADQS_WP6		15MIL
4.4B<> 3.4A<>	BI	FBADQS_RN<7>	FBADQS_RN7		15MIL
4.5B<> 3.3A<>	BI	FBADQS_WP<7>	FBADQS_WP7		15MIL
	BI	FBA_VREF_DATA0		12MIL	
	BI	FBA_VREF_ADDR0		12MIL	
	BI	FBA_VREF_DATA1		12MIL	
	BI	FBA_VREF_ADDR1		12MIL	

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	FBA 8Mx32 DDR3 MEMORIES, FBA COMMAND BUS PU'S, FBA CLK PU'S

NVIDIA CORPORATION
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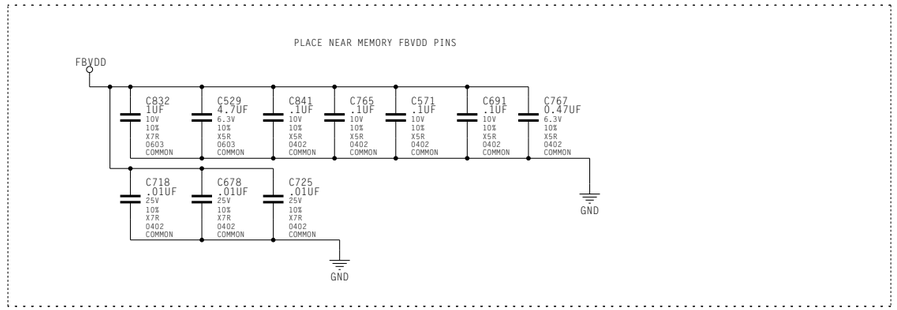
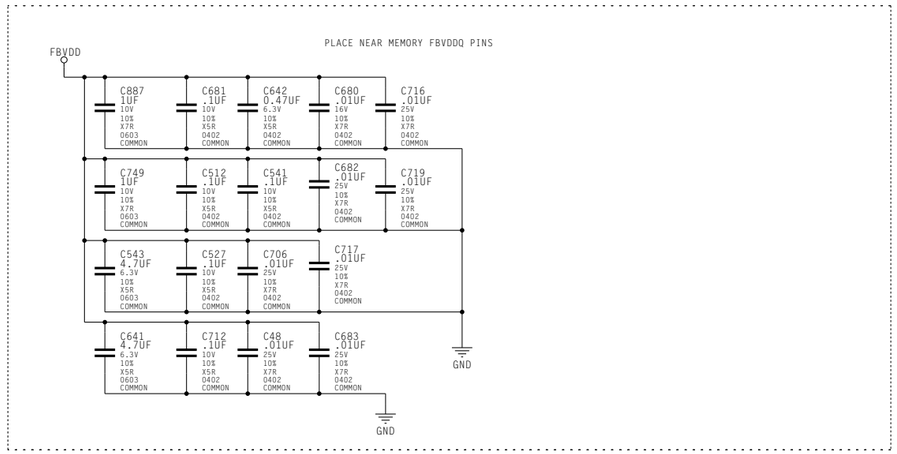
NV_PN	602-10216-0001-300		
ID	p216	PAGE	4 OF 25
NAME	bnichols	DATE	9-SEP-2004

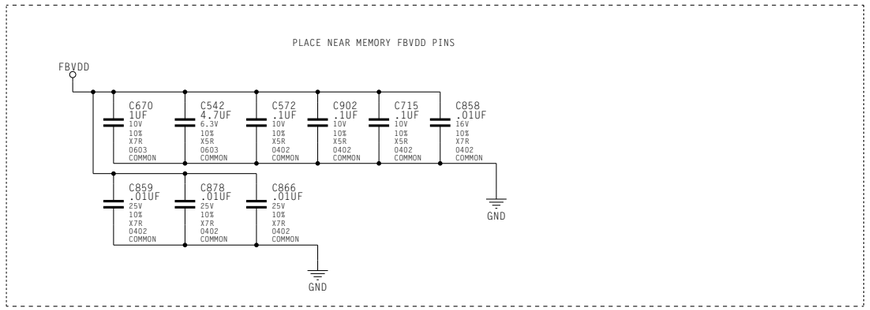
FRAME BUFFER: PARTITION A DECOUPLING

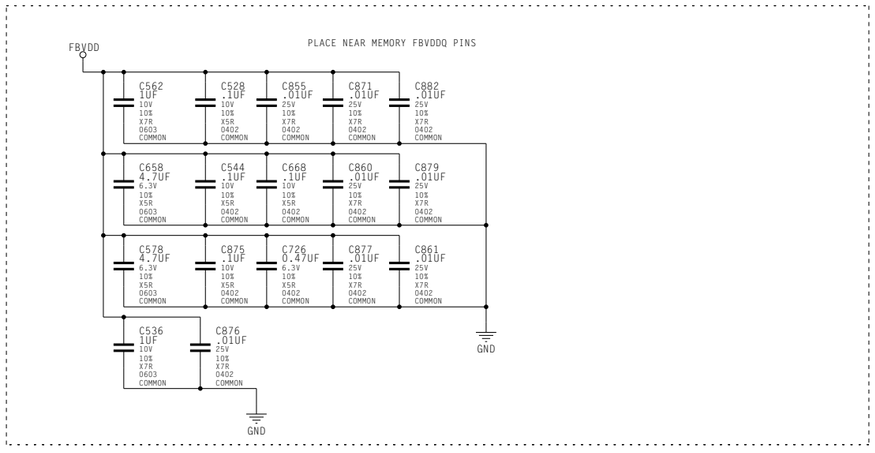
Decoupling for FBA 0..31





Decoupling for FBA 32..63





ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	FBA MEMORY FBVDD/Q DECOUPLING CAPS

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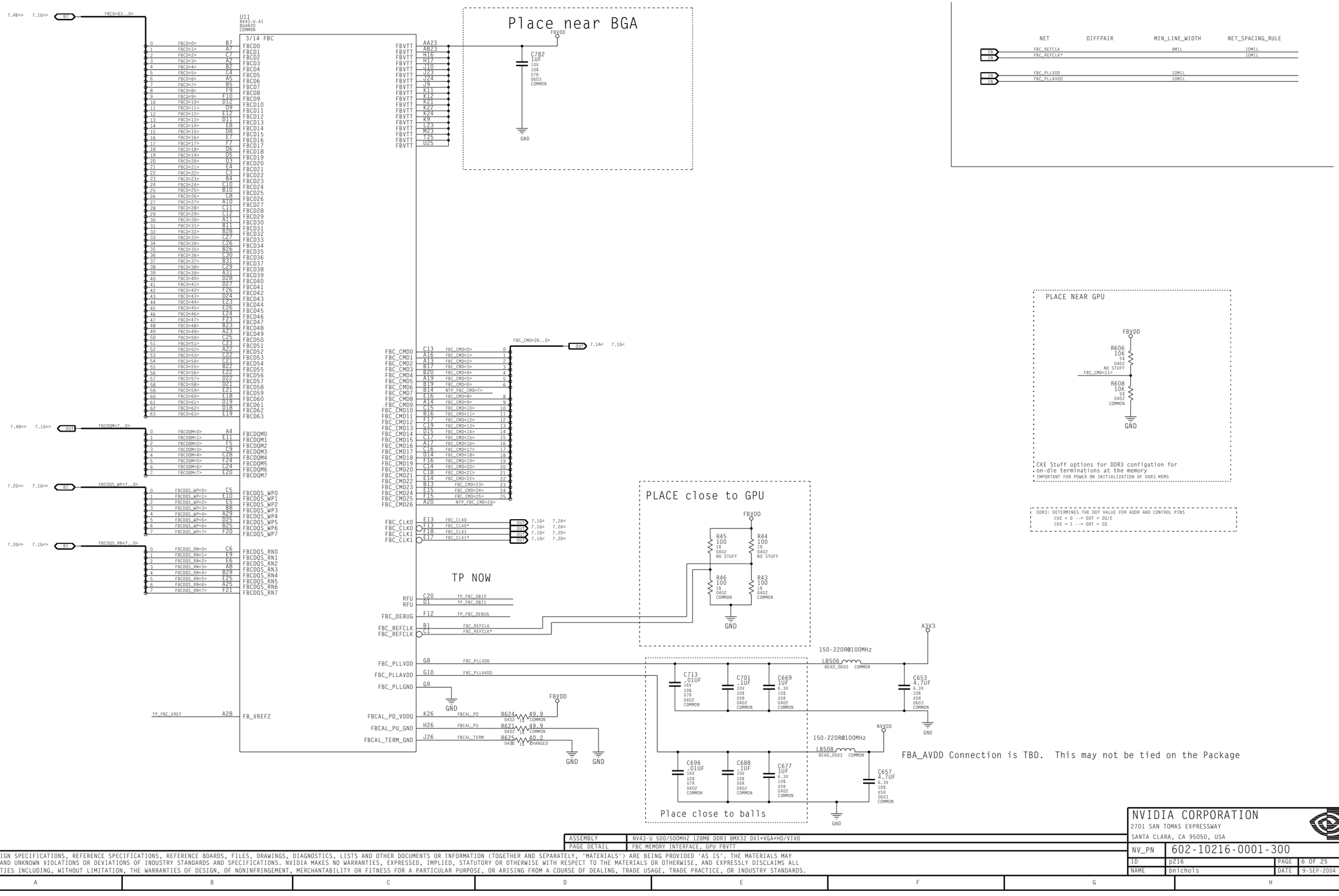
NV_PN	602-10216-0001-300		
ID	p216	PAGE	5 OF 25
NAME	bnichols	DATE	9-SEP-2004



ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	FBC MEMORY INTERFACE, GPU FBVTT

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SANTA CLARA, CA 95050, USA

NV_PN	602-10216-0001-300		
ID	p216	PAGE	6 OF 25
NAME	bnichols	DATE	9-SEP-2004

FRAMEBUFFER: PARTITION C 8Mx32 BGA144 DDR3

A-CS0-LOW-32bit

U3 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

FBVDD

7.1G< 6.3D> IN FBC_CMD<26..0>

15	FBC_CMD<15>	M5	RAS
25	FBC_CMD<25>	N6	CAS
9	FBC_CMD<9>	N9	WE
8 CS0	FBC_CMD<8>	M10	CS
1	FBC_CMD<1>	N2	A0
3	FBC_CMD<3>	N3	A1
2	FBC_CMD<2>	M3	A2
0	FBC_CMD<0>	L3	A3
24	FBC_CMD<24>	L12	A4
22	FBC_CMD<22>	M12	A5
21	FBC_CMD<21>	N12	A6
23	FBC_CMD<23>	N13	A7
19	FBC_CMD<19>	N11	A8
20	FBC_CMD<20>	M11	A9
17	FBC_CMD<17>	M4	A10
16	FBC_CMD<16>	N4	A11
14	FBC_CMD<14>	L9	NC/A<12>
10	FBC_CMD<10>	N5	BA<0>
18	FBC_CMD<18>	N10	BA<1>
	TP_FBCO_BA<2>	L6	NC/BA<2>
11	FBC_CMD<11>	M7	CKE
	FBC_CLK0	N7	CLK
	FBC_CLK0*	N8	CLK
	TP_FBCO_NC1	E3	NC/RFU
	TP_FBCO_NC2	E12	NC/RFU
	TP_FBCO_NC3	M8	NC/RFU
12	FBC_CMD<12>	M6	RESET
	FBC_ZQO	M9	ZQ
		F6 F7 F8 F9 G6 G7 G8 G9 H6 H7 H8 H9 J6 J7 J8 J9	THERM
		B4 B11 D4 D5 D6 D9 D10 D11 E6 E9 F5 F10 G5 G10 H5 H10 J5 J10 K5 K10	VSSQ
		C4 C5 C7 C8 C10 C11 F4 F11 G4 G11 H4 H11 J4 J11 K4 K11	VDDQ
		D7 D8 E4 E11 L4 L7 L8 L11	VDD
		E5 E7 E8 E10 K6 K7 K8 K9 L5 L10	VSS
		M2 FBC_VREF_DATA0; M13 FBC_VREF_ADDR0	VREF

Low Sub-Partition

R501 10K 5% 0402 COMMON

R1 240 1% 0603 COMMON

DDR3: ZQ = 6x desired output impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

VREF = FBVDDQ * R2/(R1 + R2)

VREF:
M2 - DATA
M13 - ADDR

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 2.7K/(1.15K + 2.7K)

FBC Partition

Termination for Sub-Partition and CLK MUST BE PLACED as close as possible to the BGA memory on the line BEFORE the MEMORY pin!! Minimize the stub length!!

FBC_CMD<26..0>

2	FBC_CMD<2>	120 1% COMMON	R532 0402
0	FBC_CMD<0>	120 1% COMMON	R538 0402
24	FBC_CMD<24>	120 1% COMMON	R539 0402
22	FBC_CMD<22>	120 1% COMMON	R533 0402
13	FBC_CMD<13>	120 1% COMMON	R530 0402
4	FBC_CMD<4>	120 1% COMMON	R536 0402
5	FBC_CMD<5>	120 1% COMMON	R537 0402
6	FBC_CMD<6>	120 1% COMMON	R531 0402
	FBC_CLK0	60.4 1% CHANGED	R5 0402
	FBC_CLK0*	60.4 1% CHANGED	R4 0402
	FBC_CLK1	60.4 1% CHANGED	R7 0402
	FBC_CLK1*	60.4 1% CHANGED	R6 0402

HI Sub-Partition

A-CS0-HI-32bit

U4 DDR3BGA144 PACK_TYPE=BGA144 VERSION=BGA144 CHANGED

FBVDD

FBC_CMD<26..0>

15	FBC_CMD<15>	M5	RAS
25	FBC_CMD<25>	N6	CAS
9	FBC_CMD<9>	N9	WE
8 CS0	FBC_CMD<8>	M10	CS
1	FBC_CMD<1>	N2	A0
3	FBC_CMD<3>	N3	A1
13	FBC_CMD<13>	M3	A2
4	FBC_CMD<4>	L3	A3
5	FBC_CMD<5>	L12	A4
6	FBC_CMD<6>	M12	A5
21	FBC_CMD<21>	N12	A6
23	FBC_CMD<23>	N13	A7
19	FBC_CMD<19>	N11	A8
20	FBC_CMD<20>	M11	A9
17	FBC_CMD<17>	M4	A10
16	FBC_CMD<16>	N4	A11
14	FBC_CMD<14>	L9	NC/A<12>
10	FBC_CMD<10>	N5	BA<0>
18	FBC_CMD<18>	N10	BA<1>
	FBC_FBC1_BA<2>	L6	NC/BA<2>
11	FBC_CMD<11>	M7	CKE
	FBC_CLK1	N7	CLK
	FBC_CLK1*	N8	CLK
	TP_FBC1_NC1	E3	NC/RFU
	TP_FBC1_NC2	E12	NC/RFU
	TP_FBC1_NC3	M8	NC/RFU
	FBC_CMD<12>	M6	RESET
	FBC_ZQ1	M9	ZQ
		F6 F7 F8 F9 G6 G7 G8 G9 H6 H7 H8 H9 J6 J7 J8 J9	THERM
		B4 B11 D4 D5 D6 D9 D10 D11 E6 E9 F5 F10 G5 G10 H5 H10 J5 J10 K5 K10	VSSQ
		C4 C5 C7 C8 C10 C11 F4 F11 G4 G11 H4 H11 J4 J11 K4 K11	VDDQ
		D7 D8 E4 E11 L4 L7 L8 L11	VDD
		E5 E7 E8 E10 K6 K7 K8 K9 L5 L10	VSS
		M2 FBC_VREF_DATA1; M13 FBC_VREF_ADDR1	VREF

R2 240 1% 0603 COMMON

DDR3: ZQ = 6x desired output impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 2.7K/(1.15K + 2.7K)

144BGA CMD Mapping

CMD	ADDR
CMD15	RAS*
CMD25	CAS*
CMD9	WE*
CMD11	CKE
CMD12	RESET
CMD8	CS0*
CMD7	CS1**notused
CMD1	A<0>
CMD3	A<1>
CMD2	A<2>
CMD0	A<3>
CMD24	A<4>
CMD22	A<5>
CMD13	A<2>
CMD4	A<3>
CMD5	A<4>
CMD6	A<5>
CMD21	A<6>
CMD23	A<7>
CMD19	A<8>
CMD20	A<9>
CMD17	A<10
CMD16	A<11>
CMD14	A<12>
CMD10	BA0
CMD18	BA1

Low Sub-Partition

HI Sub-Partition

NET	DIFFPAIR	MIN_LINE_WIDTH	SPACING
FBC_CLK0	FBC_CLK0	5MIL	15MIL_G2G_25MIL
FBC_CLK0*	FBC_CLK0	5MIL	15MIL_G2G_25MIL
FBC_CLK1	FBC_CLK1	5MIL	15MIL_G2G_25MIL
FBC_CLK1*	FBC_CLK1	5MIL	15MIL_G2G_25MIL
FBC_CMD<26..0>			15MIL
FBCD<63..0>			15MIL
FBCDQM<7..0>			15MIL
FBCDQS_RN<0>	FBCDQS_RN0		15MIL
FBCDQS_WP<0>	FBCDQS_RN0		15MIL
FBCDQS_RN<1>	FBCDQS_RN1		15MIL
FBCDQS_WP<1>	FBCDQS_RN1		15MIL
FBCDQS_RN<2>	FBCDQS_RN2		15MIL
FBCDQS_WP<2>	FBCDQS_RN2		15MIL
FBCDQS_RN<3>	FBCDQS_RN3		15MIL
FBCDQS_WP<3>	FBCDQS_RN3		15MIL
FBCDQS_RN<4>	FBCDQS_RN4		15MIL
FBCDQS_WP<4>	FBCDQS_RN4		15MIL
FBCDQS_RN<5>	FBCDQS_RN5		15MIL
FBCDQS_WP<5>	FBCDQS_RN5		15MIL
FBCDQS_RN<6>	FBCDQS_RN6		15MIL
FBCDQS_WP<6>	FBCDQS_RN6		15MIL
FBCDQS_RN<7>	FBCDQS_RN7		15MIL
FBCDQS_WP<7>	FBCDQS_RN7		15MIL
FBC_VREF_DATA0		12MIL	
FBC_VREF_ADDR0		12MIL	
FBC_VREF_DATA1		12MIL	
FBC_VREF_ADDR1		12MIL	

R524 1K 1% 0402 COMMON; C513 .1UF 10V 10% X5R 0402 NO STUFF

R525 2.55K 1% 0402 CHANGED; C514 .1UF 10V 10% X5R 0402 COMMON

R527 1K 1% 0402 COMMON; C516 .1UF 10V 10% X5R 0402 NO STUFF

R526 2.55K 1% 0402 CHANGED; C515 .1UF 10V 10% X5R 0402 COMMON

R528 1K 1% 0402 COMMON; C517 .1UF 10V 10% X5R 0402 NO STUFF

R529 2.55K 1% 0402 CHANGED; C518 .1UF 10V 10% X5R 0402 COMMON

R523 1K 1% 0402 COMMON; C511 .1UF 10V 10% X5R 0402 NO STUFF

R522 2.55K 1% 0402 CHANGED; C510 .1UF 10V 10% X5R 0402 COMMON

FBCD<63..0>

U3 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

0	FBCD<0>	C9	DQ0
1	FBCD<1>	B9	DQ1
2	FBCD<2>	B8	DQ2
3	FBCD<3>	D13	DQ3
4	FBCD<4>	E13	DQ4
5	FBCD<5>	C13	DQ5
6	FBCD<6>	D12	DQ6
7	FBCD<7>	B10	DQ7
	FBCDQM<0>	C12	DQM
	FBCDQS_RN<0>	B12	DQSR
	FBCDQS_WP<0>	B13	DQSW
8	FBCD<8>	K3	DQ0
9	FBCD<9>	J2	DQ1
10	FBCD<10>	L2	DQ2
11	FBCD<11>	F2	DQ3
12	FBCD<12>	K2	DQ4
13	FBCD<13>	G2	DQ5
14	FBCD<14>	G3	DQ6
15	FBCD<15>	F3	DQ7
	FBCDQM<1>	J3	DQM
	FBCDQS_RN<1>	H3	DQSR
	FBCDQS_WP<1>	H2	DQSW
16	FBCD<16>	G12	DQ0
17	FBCD<17>	F12	DQ1
18	FBCD<18>	F13	DQ2
19	FBCD<19>	G13	DQ3
20	FBCD<20>	K12	DQ4
21	FBCD<21>	L13	DQ5
22	FBCD<22>	J13	DQ6
23	FBCD<23>	K13	DQ7
	FBCDQM<2>	J12	DQM
	FBCDQS_RN<2>	H12	DQSR
	FBCDQS_WP<2>	H13	DQSW
24	FBCD<24>	B6	DQ0
25	FBCD<25>	B5	DQ1
26	FBCD<26>	B7	DQ2
27	FBCD<27>	C6	DQ3
28	FBCD<28>	C2	DQ4
29	FBCD<29>	E2	DQ5
30	FBCD<30>	D3	DQ6
31	FBCD<31>	D2	DQ7
	FBCDQM<3>	C3	DQM
	FBCDQS_RN<3>	B3	DQSR
	FBCDQS_WP<3>	B2	DQSW

U4 DDR3BGA144 BGA144 VERSION=BGA144 CHANGED

32	FBCD<32>	B5	DQ0
33	FBCD<33>	C6	DQ1
34	FBCD<34>	B6	DQ2
35	FBCD<35>	B7	DQ3
36	FBCD<36>	D3	DQ4
37	FBCD<37>	E2	DQ5
38	FBCD<38>	C2	DQ6
39	FBCD<39>	D2	DQ7
	FBCDQM<4>	C3	DQM
	FBCDQS_RN<4>	B3	DQSR
	FBCDQS_WP<4>	B2	DQSW
40	FBCD<40>	L2	DQ0
41	FBCD<41>	K2	DQ1
42	FBCD<42>	G2	DQ2
43	FBCD<43>	F3	DQ3
44	FBCD<44>	K3	DQ4
45	FBCD<45>	J2	DQ5
46	FBCD<46>	F2	DQ6
47	FBCD<47>	G3	DQ7
	FBCDQM<5>	J3	DQM
	FBCDQS_RN<5>	H3	DQSR
	FBCDQS_WP<5>	H2	DQSW
48	FBCD<48>	B10	DQ0
49	FBCD<49>	C9	DQ1
50	FBCD<50>	B8	DQ2
51	FBCD<51>	B9	DQ3
52	FBCD<52>	D12	DQ4
53	FBCD<53>	C13	DQ5
54	FBCD<54>	E13	DQ6
55	FBCD<55>	D13	DQ7
	FBCDQM<6>	C12	DQM
	FBCDQS_RN<6>	B12	DQSR
	FBCDQS_WP<6>	B13	DQSW
56	FBCD<56>	K12	DQ0
57	FBCD<57>	G12	DQ1
58	FBCD<58>	F12	DQ2
59	FBCD<59>	L13	DQ3
60	FBCD<60>	G13	DQ4
61	FBCD<61>	J13	DQ5
62	FBCD<62>	K13	DQ6
63	FBCD<63>	F13	DQ7
	FBCDQM<7>	J12	DQM
	FBCDQS_RN<7>	H12	DQSR
	FBCDQS_WP<7>	H13	DQSW

7.1G< 6.1A< B1 FBCD<63..0>

7.1G< 6.3A< B1 FBCDQM<7..0>

7.2G< 7.1G< 6.4A< B1 FBCDQS_RN<7..0>

7.2G< 7.1G< 6.3A< B1 FBCDQS_WP<7..0>

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	FBC 8MX32 DDR3 MEMORIES, FBC CMD BUS PU'S, FBC CLK PU's

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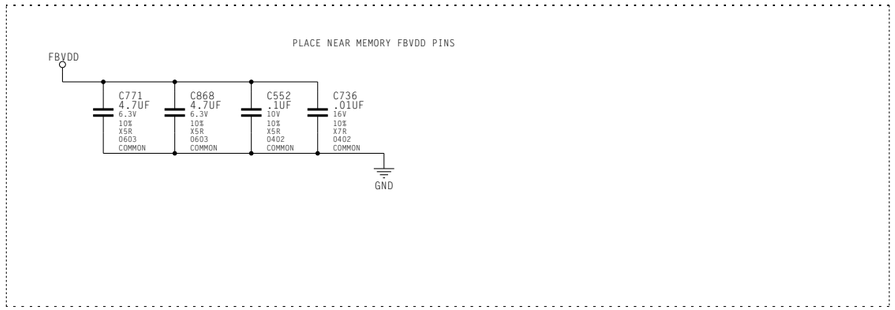
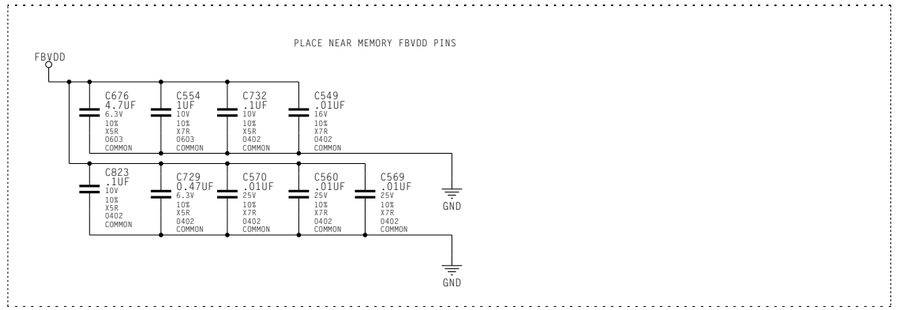
NV_PN	602-10216-0001-300		
ID	p216	PAGE	7 OF 25
NAME	bnichols	DATE	9-SEP-2004

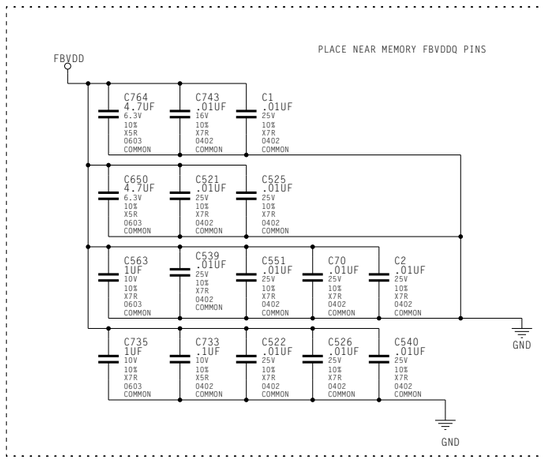
FRAMEBUFFER: PARTITION C DECOUPLING

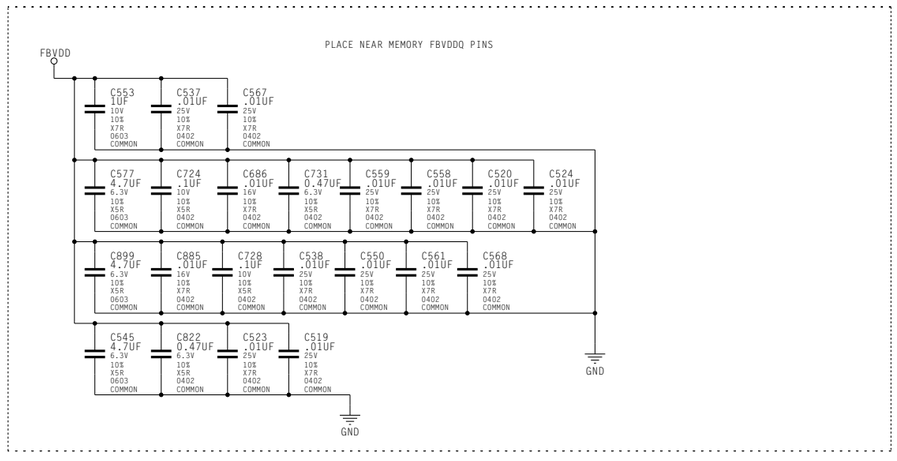
Decoupling for FBC 0..31



Decoupling for FBC 32..63







U11
NV43-U-A1
BGA820
COMMON

14/14 _GND_

AA12	GND	K10	GND
AA2	GND	K23	GND
AA21	GND	K29	GND
AA31	GND	K4	GND
AB27	GND	L27	GND
AB6	GND	L6	GND
AC10	GND	M12	GND
AC23	GND	M2	GND
AC29	GND	M31	GND
AC4	GND	N15	GND
AD16	GND	N18	GND
AD17	GND	N29	GND
AD2	GND	N4	GND
AD31	GND	P15	GND
AE17	GND	P18	GND
AE27	GND	P27	GND
AE6	GND	P6	GND
AF11	GND	R13	GND
AF26	GND	R14	GND
AF29	GND	R15	GND
AF4	GND	R18	GND
AF7	GND	R19	GND
AG10	GND	R2	GND
AG11	GND	R20	GND
AG14	GND	R31	GND
AG15	GND	T16	GND
AG19	GND	T17	GND
AG2	GND	T24	GND
AG22	GND	T29	GND
AG31	GND	T4	GND
AG8	GND	U16	GND
AH24	GND	U17	GND
AJ10	GND	U24	GND
AJ13	GND	U29	GND
AJ16	GND	U8	GND
AJ17	GND	V13	GND
AJ20	GND	V14	GND
AJ23	GND	V15	GND
AJ26	GND	V18	GND
AJ29	GND	V19	GND
AJ4	GND	V2	GND
AJ7	GND	V20	GND
AK2	GND	V31	GND
AK28	GND	W15	GND
AK31	GND	W18	GND
AL11	GND	W27	GND
AL14	GND	W6	GND
AL19	GND	Y15	GND
AL22	GND	Y18	GND
AL25	GND	Y29	GND
AL3	GND	Y4	GND
AL6	GND	ALI0	GND
AL9	GND	AMI0	GND
AM13	GND	AQ13	GND
AM16	GND		
AM17	GND		
AM20	GND		
AM23	GND		
AM26	GND		
AM29	GND		
B12	GND		
B15	GND		
B18	GND		
B21	GND		
B24	GND		
B27	GND		
B3	GND		
B30	GND		
B6	GND		
B9	GND		
C2	GND		
C31	GND		
D10	GND		
D13	GND		
D16	GND		
D17	GND		
D20	GND		
D23	GND		
D26	GND		
D29	GND		
D4	GND		
D7	GND		
F11	GND		
F14	GND		
F19	GND		
F2	GND		
F22	GND		
F25	GND		
F31	GND		
F8	GND		
G26	GND		
G29	GND		
G4	GND		
G7	GND		
H27	GND		
H6	GND		
J16	GND		
J17	GND		
J2	GND		
J31	GND		

GND
GND

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	FBC MEMORY FBVDD/Q DECOUPLING CAPS, GPU GND CONNECTIONS

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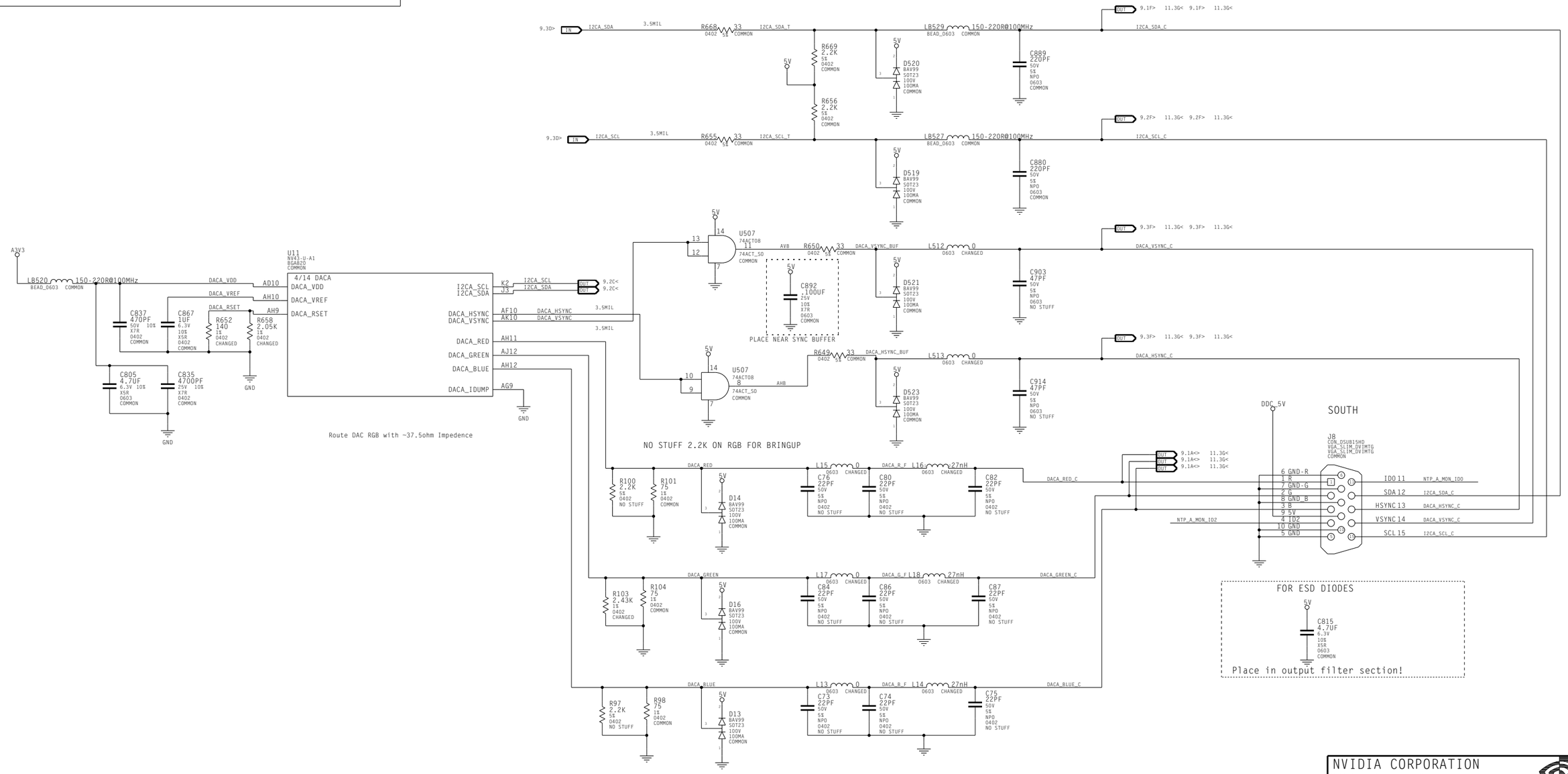
NV_PN	602-10216-0001-300		
ID	p216	PAGE	8 OF 25
NAME	bnichols	DATE	9-SEP-2004

Primary Display (DACA), Slim DB15

DACA RGB-FILTER

NET_NAME	NET_SPACING_RULE	IMPEDANCE	MIN_LINE_WIDTH
IN DACA_VDD			12MIL
IN DACA_VREF			12MIL
IN DACA_RSET			12MIL
B! DACA_RED	20MIL	U11_AH11-R101_1:37.50 ohm:2 %	
B! DACA_GREEN	20MIL	U11_AJ12-R104_1:37.50 ohm:2 %	
B! DACA_BLUE	20MIL	U11_AH12-R98_1:37.50 ohm:2 %	
B! DACA_R_F	20MIL	L15_2:L16_1:75.00 ohm:2 %	
B! DACA_G_F	20MIL	L17_2:L18_1:75.00 ohm:2 %	
B! DACA_B_F	20MIL	L13_2:L14_1:75.00 ohm:2 %	
11.3G< 9.4F> B! DACA_RED_C	20MIL	L16_2:J8_1:75.00 ohm:2 %	
11.3G< 9.4F> B! DACA_GREEN_C	20MIL	L18_2:J8_2:75.00 ohm:2 %	
11.3G< 9.4F> B! DACA_BLUE_C	20MIL	L14_2:J8_3:75.00 ohm:2 %	
DDC_5V DDC_5V			12MIL



ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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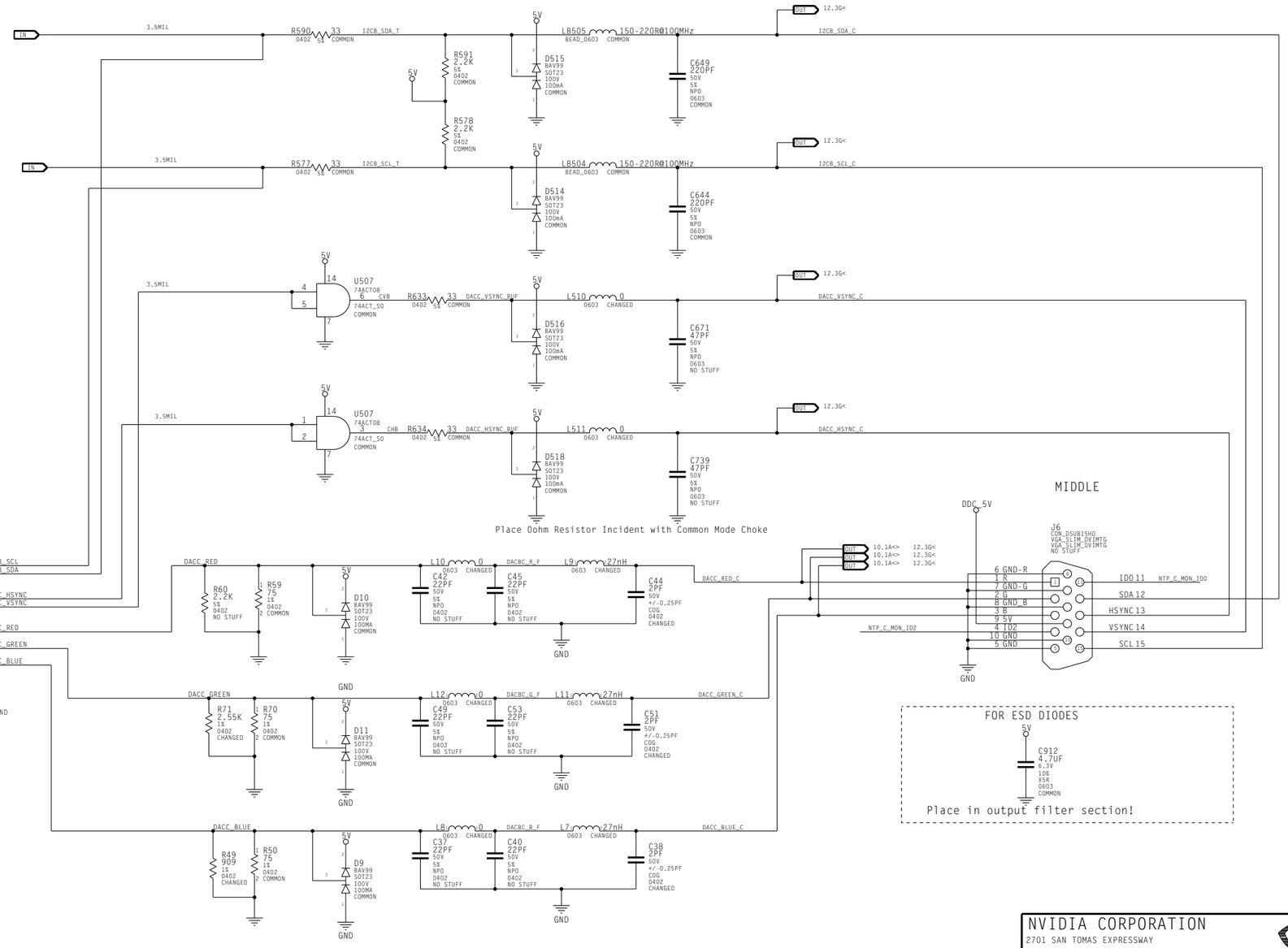
NV_PN	602-10216-0001-300		
ID	p216	PAGE	9 OF 25
NAME	bnichols	DATE	9-SEP-2004

Secondary Display (DACC), Slim DB15

NET_NAME	NET_SPACING_RULE	IMPEDANCE	MIN_LINE_WIDTH
DACC_VDD			12MIL
DACC_VREF			12MIL
DACC_RSET			12MIL
DACC_RED	20MIL	U11_AF6:R59_1:37.50 ohm:2 %	
DACC_GREEN	20MIL	U11_AG6:R70_1:37.50 ohm:2 %	
DACC_BLUE	20MIL	U11_AE5:R50_1:37.50 ohm:2 %	
DACBC_R_F	20MIL	L10_2:L9_1:75.00 ohm:2 %	
DACBC_G_F	20MIL	L12_2:L11_1:75.00 ohm:2 %	
DACBC_B_F	20MIL	L8_2:L7_1:75.00 ohm:2 %	
DACC_RED_C	20MIL	L9_2:J6_1:75.00 ohm:2 %	
DACC_GREEN_C	20MIL	L11_2:J6_2:75.00 ohm:2 %	
DACC_BLUE_C	20MIL	L7_2:J6_3:75.00 ohm:2 %	

DACC RGB-FILTER



ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID

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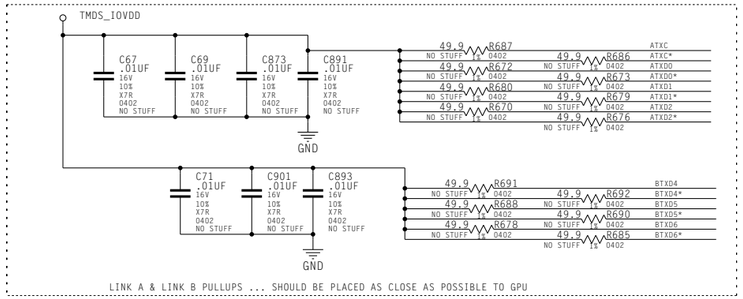
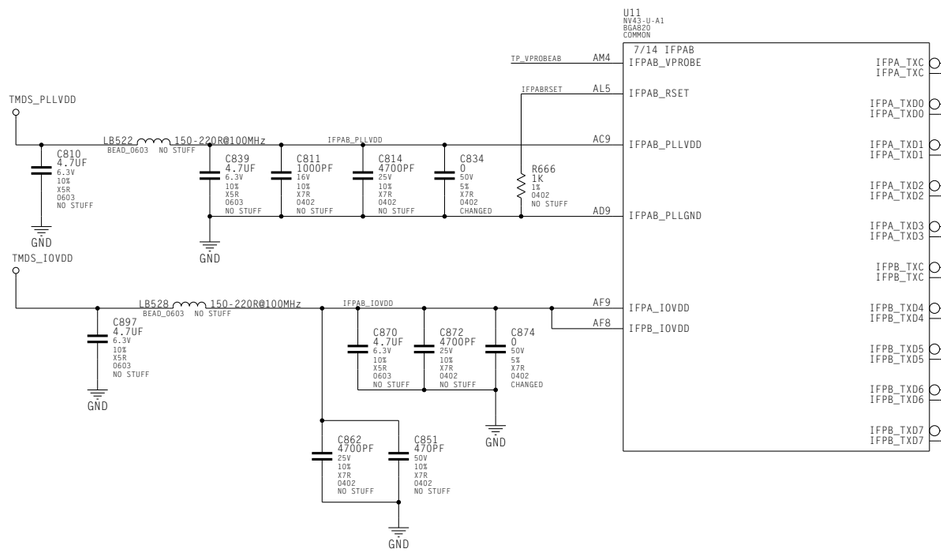
NV_PN	602-10216-0001-300		
ID	p216	PAGE	10 OF 25
NAME	bnichols	DATE	9-SEP-2004

INTERNAL TMDS .. LINK A & B

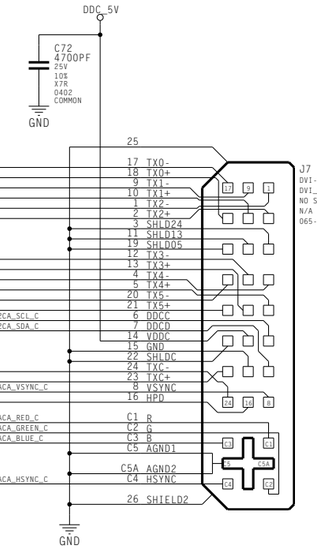


NOTE: GPU HAS ON DIE PULL UPS ON TMOS LINES .. EXTERNAL PULLUPS ADDED (FOR CYA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE

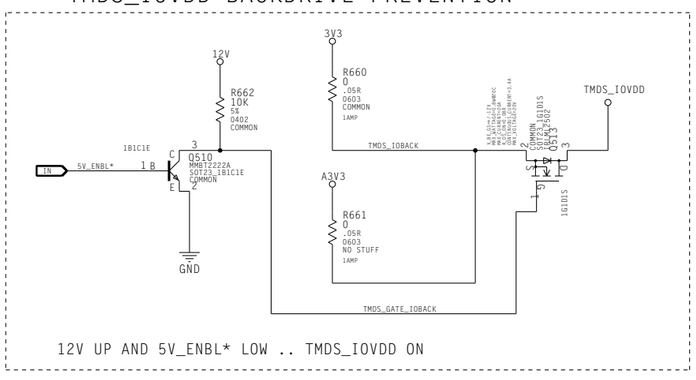


NETNAME	DIFF PAIR NAME	MIN_LINE_WIDTH	SPACING RULE
IFPA_TXC	AJ9 ATXC*	ATXC 3.5MIL	25MIL
IFPA_TXC	AK9 ATXC	ATXC 3.5MIL	25MIL
IFPA_TXD0	AJ6 ATXD0*	ATXD0 3.5MIL	25MIL
IFPA_TXD0	AH6 ATXD0	ATXD0 3.5MIL	25MIL
IFPA_TXD1	AH7 ATXD1*	ATXD1 3.5MIL	25MIL
IFPA_TXD1	AH8 ATXD1	ATXD1 3.5MIL	25MIL
IFPA_TXD2	AK8 ATXD2*	ATXD2 3.5MIL	25MIL
IFPA_TXD2	AJ8 ATXD2	ATXD2 3.5MIL	25MIL
IFPA_TXD3	AH5 TP_ATXD3*		
IFPA_TXD3	AJ5 TP_ATXD3		
IFPB_TXC	AL4 TP_BTXC*		
IFPB_TXC	AK4 TP_BTXC		
IFPB_TXD4	AM5 BTXD4*	ATXD4 3.5MIL	25MIL
IFPB_TXD4	AM6 BTXD4	ATXD4 3.5MIL	25MIL
IFPB_TXD5	AL7 BTXD5*	ATXD5 3.5MIL	25MIL
IFPB_TXD5	AM7 BTXD5	ATXD5 3.5MIL	25MIL
IFPB_TXD6	AK5 BTXD6*	ATXD6 3.5MIL	25MIL
IFPB_TXD6	AK6 BTXD6	ATXD6 3.5MIL	25MIL
IFPB_TXD7	AL8 TP_BTXD7*		
IFPB_TXD7	AK7 TP_BTXD7		

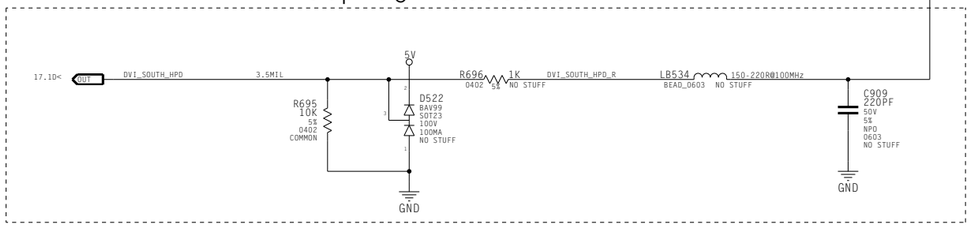
FOR MICROSTRIP 100 OHM DIFFERENTIAL IMPEDANCE



TMDS_IOVDD BACKDRIVE PREVENTION



Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
TMDS_PLLVDD	12MIL	3.3V
IFPAB_PLLVDD	12MIL	3.3V
TMDS_IOVDD	12MIL	3.3V
IFPAB_IOVDD	12MIL	3.3V
IFPABRSET	12MIL	
TMDS_IOBACK	12MIL	

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	TMDS LINK A/B & PU's, TMDS IO BACKDRIVE PREVENTION,DVI CONNECTOR SOUTH

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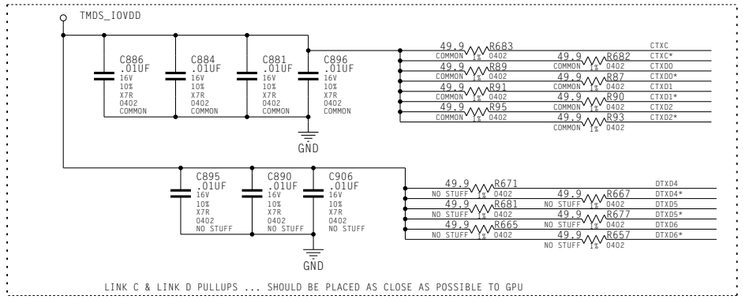
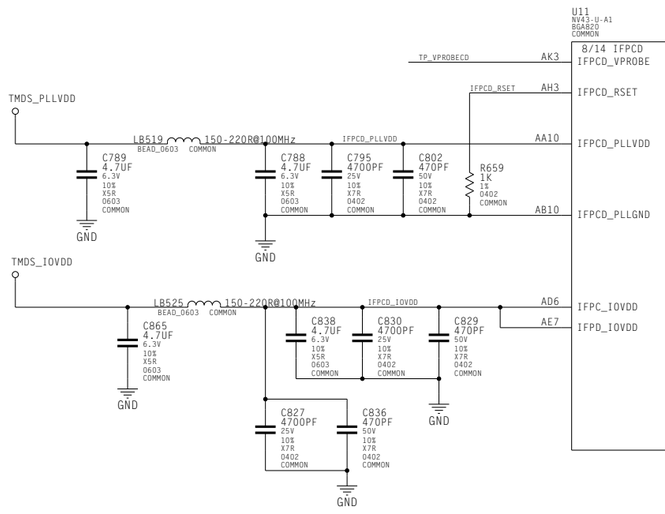
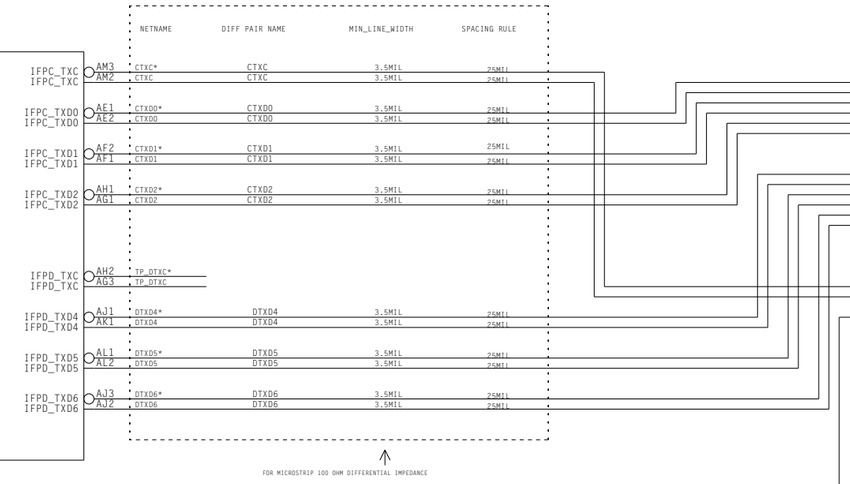
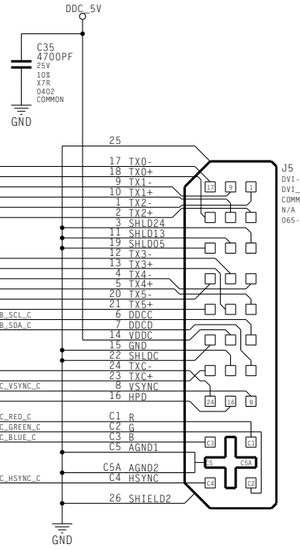
NV_PN	602-10216-0001-300		
ID	p216	PAGE	11 OF 25
NAME	bnichols	DATE	9-SEP-2004

INTERNAL TMDS .. LINK C & D

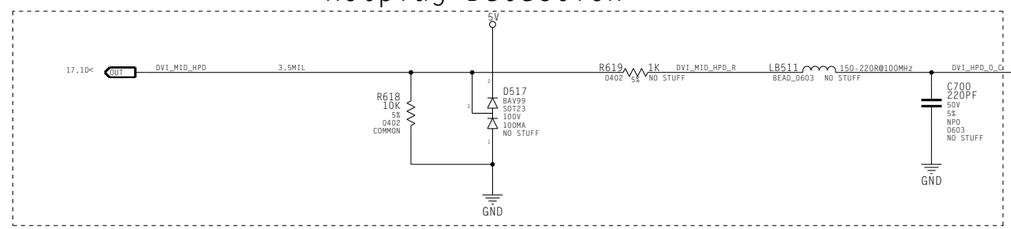








Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
IFPCD_RSET	12MIL	
IFPCD_PLLVDD	12MIL	3.3V
IFPCD_IOVDD	12MIL	3.3V

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	TMDS LINK C/D & PU's,DVI CONNECTOR MID

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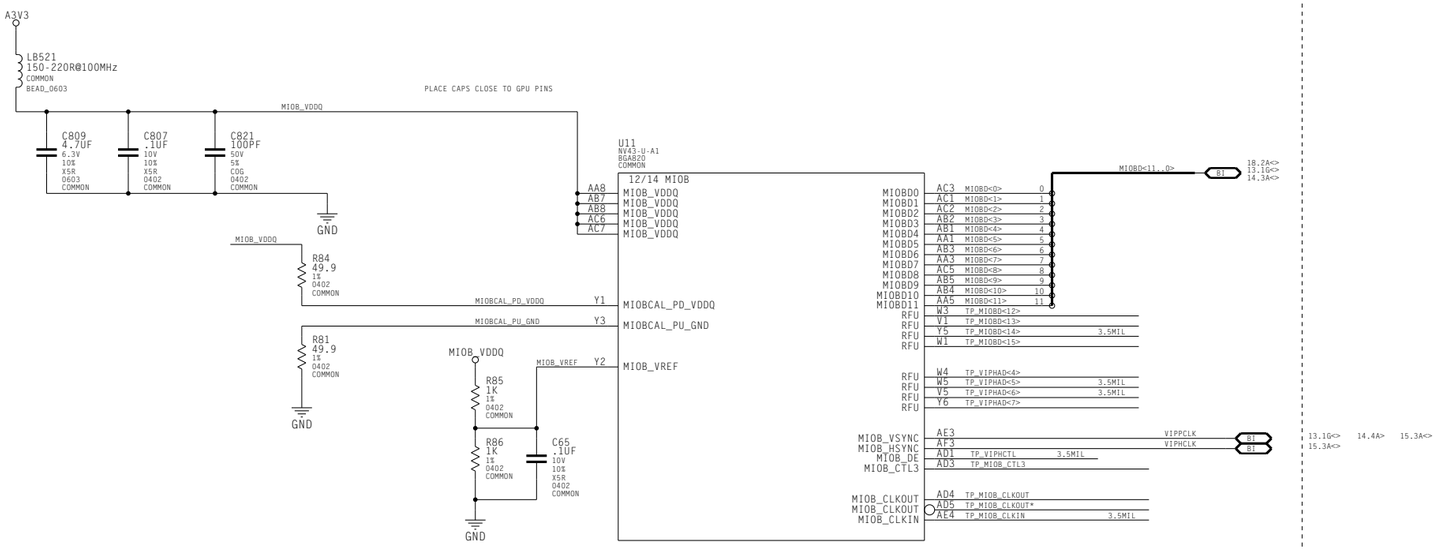
NV_PN	602-10216-0001-300		
ID	p216	PAGE	12 OF 25
NAME	bnichols	DATE	9-SEP-2004

G3 VIP/MIOB



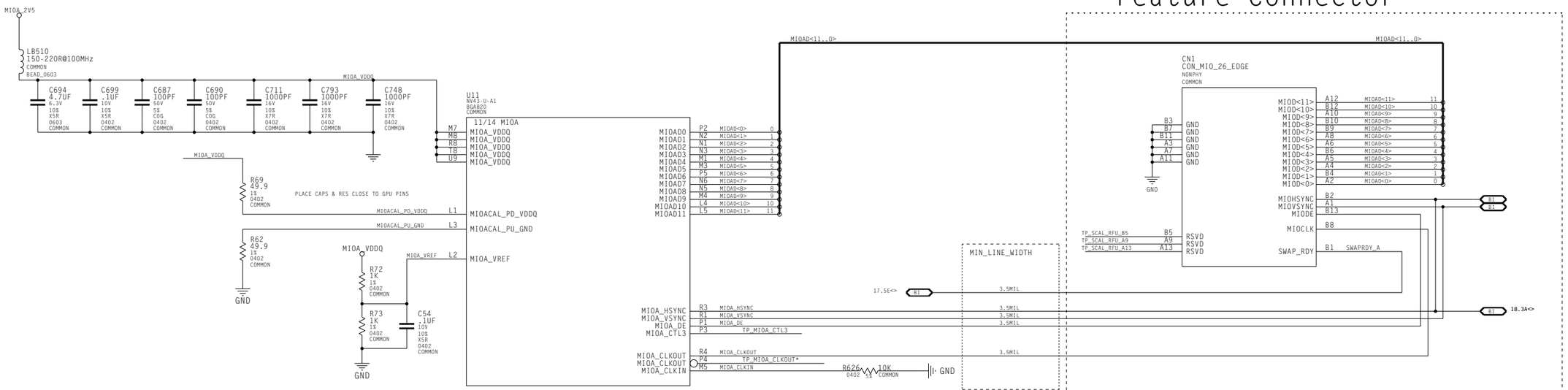
NETNAME | MIN_LINE_WIDTH | SPACING RULE

14.3A<> 18.2A<> 13.1E<> 18.2A<>	BI	MIOBD<7..0>	3.5MIL	15MIL
	BI	MIOBD<11..10>	3.5MIL	10MIL
14.4A> 13.2E<> 15.3A<>	BI	VIPPCLK	3.5MIL	20MIL_G2G_30MIL
18.1A<>	BI	MIOAD<11..0>	3.5MIL	15MIL
	BI	MIOA_CLKOUT		20MIL_G2G_30MIL
	BI	MIOA_CLKOUT*		20MIL_G2G_30MIL

NETNAME | MIN_LINE_WIDTH

MIOB_VDDQ	MIOB_VDDQ		12MIL
	BI	MIOB_VREF	12MIL
MIOA_VDDQ	MIOA_VDDQ		12MIL
	BI	MIOA_VREF	12MIL

G3 MIOA



Feature Connector

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	MIOA & MIOB, FEATURE CONNECTOR

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NV_PN	602-10216-0001-300		
ID	p216	PAGE	13 OF 25
NAME	bnichols	DATE	9-SEP-2004

PHILIPS VIDEO CAPTURE

NETNAME	MIN_LINE_WIDTH
VDDA	12MIL
VDDX	12MIL
VDDE	12MIL

SAA 7115
I2C ADDRESS 0X42

SAA7114 RESET (IMMEDIATE)

SAA7115 RESET (100US DELAY)

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	PHILIPS SAA7115 VIDEO DECODER

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NV_PN	602-10216-0001-300		
ID	p216	PAGE	14 OF 25
NAME	bnichols	DATE	9-SEP-2004

DACB .. MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES

NET_NAME	MIN_LINE_WIDTH	IMPEDANCE	NET_SPACING_RULE
OUT DACB_C_OUT		U11_R6:R644_1:37.50_ohm:2_%	20MIL
OUT DACB_CVBS_OUT		U11_T5:R561_1:37.50_ohm:2_%	20MIL
OUT DACB_PB_OUT		U11_T6:R541_1:37.50_ohm:2_%	20MIL
BI MDIN_PBout_C			20MIL
BI MDIN_Cout_C			20MIL
BI MDIN_Yout_C			20MIL
14.1A< BI MINIDIN_Y_CVBSin			20MIL
BI MDIN_Yin_C			20MIL
BI MDIN_Yin_clamp			20MIL
BI MDIN_Cin_C			20MIL
14.2A< BI MINIDIN_Cin			20MIL
15.2H> BI MDIN_Cin_clamp			20MIL
IN DACB_VDD	12MIL		
IN DACB_VREF	12MIL		
IN DACB_RSET	12MIL		

SYNC STRIPPER

PLACE RESISTORS AS CLOSE AS POSSIBLE
TO EXISTING SYNC LINES .. AVOID EXTRA STUBS ON GPU SIDE

14.4A> 13.1G<> 13.2E<> BI VIPPCLK — R113 0 5% 0402 NO STUFF — SS_V_EN
13.2E<> BI VIPHCLK — R116 0 5% 0402 NO STUFF — SS_H_EN

DACB_A3V3
R117 150 5% 0402 NO STUFF
C106 .1UF 10V 10% X5R 0402 NO STUFF
1B1C1E
Q23 MMBT4403 SOT23_1B1C1E NO STUFF

SS_EN — R112 100 5% 0402 NO STUFF — SS_EN_B

1G1D1S
Q22 BSS138 SOT23_1G1D1S NO STUFF
Q19 BSS138 SOT23_1G1D1S NO STUFF
MAX_VOLTAGE=50V CONTINUOUS_CURRENT=0.22A@31C P_DS_ON=3.5R MAX_CURRENT=0.88A MAX_WATTAGE=0.364W@25C V_BE_GS=+/-20V

SS_GPIO_EN

Ion = 410mA
NODE SET TO ~410 MV

SS_C
R118 7.15K 1% 0402 NO STUFF
R119 1K 1% 0402 NO STUFF
SS_REF

17.2D> IN GPIO10_4B0P — R122 10K 5% 0402 NO STUFF
Q24 BSS138 SOT23_1G1D1S NO STUFF

5V — PLACE CLOSE TO OPAMP
C100 .1UF 10V 10% X5R 0402 NO STUFF
U15 ADB091ARTZ SOT23_5 NO STUFF
R120 0 5% 0402 NO STUFF — SS_OP_PB — S_OP_PB_B
R123 0 5% 0402 NO STUFF
KEEP THIS LOOP CLOSE TOGETHER
DACB_A3V3
C101 .1UF 10V 10% X5R 0402 NO STUFF
1B1C1E
Q20 MMBT2222A SOT23_1B1C1E NO STUFF
DACB_PB_OUT
MAKE SURE EMITTER IS AS CLOSE AS POSSIBLE TO TO PB_OUT TO MINIMIZE STUB LENGTH

5V — PLACE CLOSE TO OPAMP
C99 .1UF 10V 10% X5R 0402 NO STUFF
U16 ADB091ARTZ SOT23_5 NO STUFF
R121 0 5% 0402 NO STUFF — SS_OP_PR — SS_OP_PR_B
R124 0 5% 0402 NO STUFF
KEEP THIS LOOP CLOSE TOGETHER
DACB_A3V3
C102 .1UF 10V 10% X5R 0402 NO STUFF
1B1C1E
Q21 MMBT2222A SOT23_1B1C1E NO STUFF
DACB_C_OUT
MAKE SURE EMITTER IS AS CLOSE AS POSSIBLE TO TO C_OUT TO MINIMIZE STUB LENGTH

DACB_A3V3
LB515 150-220R@100MHz BEAD_0603 COMMON
C766 4.7UF 6.3V 10% X5R 0603 COMMON
C779 4700PF 25V 10% X7R 0402 COMMON
C778 470PF 50V 10% X7R 0402 COMMON
C770 1UF 6.3V 10% X5R 0402 COMMON
R630 90.9 1% 0402 COMMON
R632 1.78K 1% 0402 COMMON
GND

U11 NV43-U-A1 BGA820 COMMON
5/14 DACB(TV)
DACB_VDD V8 — DACB_VREF R5 — DACB_RSET R7
DACB_RED R6 DACB_C_OUT
DACB_GREEN T5 DACB_CVBS_OUT
DACB_BLUE T6 DACB_PB_OUT
DACB_IDUMP V7
GND

DACB_PB_OUT — R540 200 1% 0402 NO STUFF — R541 75 1% 0402 COMMON
DACB_C_OUT — R543 200 1% 0402 NO STUFF — R544 75 1% 0402 COMMON
MINIDIN_Y_CVBSin 15.1A<> 14.1A<> OUT — R556 18 5% 0402 COMMON — R557 56 5% 0402 COMMON

5V — D501 BAV99 SOT23 100V 100MA COMMON
5V — D502 BAV99 SOT23 100V 100MA COMMON
A3V3 — D508 BAV99 SOT23 100V 100MA COMMON

C508 8.2PF 0603 50V +/-0.5PF NPO CHANGED — L502 0.56uH 0603 CHANGED — MDIN_PBout_C
C507 82PF 50V 5% NPO 0603 COMMON
C509 82PF 50V 5% NPO 0603 COMMON
C534 8.2PF 0603 50V +/-0.5PF NPO CHANGED — L503 0.56uH 0603 CHANGED — MDIN_Cout_C
C533 82PF 50V 5% NPO 0603 COMMON
C535 82PF 50V 5% NPO 0603 COMMON
C575 22PF 0603 50V 5% NPO COMMON — L508 1.8uH 0603 COMMON — MDIN_Yin_C
C574 330PF 50V 5% NPO 0603 COMMON
C576 270PF 50V 5% NPO 0603 COMMON

MDIN_SCL_C_STEREO — LB4 150-220R@100MHz BEAD_0603 COMMON
C16 220PF 50V 5% NPO 0603 COMMON
SCL_C_STEREO — R25 0 5% 0402 COMMON — 3.5MIL — I2CC_SCL — IN 14.3A< 16.2E<> 17.1D<
5V — D3 BAV99 SOT23 100V 100MA COMMON

DDC_5V
C23 1UF 16V 10% X5R 0603 COMMON

J3 MINIDIN_10_VIVO X4A0 COMMON
7 — 10 — 9 Pb out — SDA 4 — C/Pr out — 8 — Y/CVBS out 6 — 1 Y/CVBS in — 5 GND — GND 3 — C in 2 — 11 — 12 — 13
MINIDIN_GND1 — MINIDIN_GND2

R23 0 05R 0603 COMMON — keep stub short

DDC_5V — LB6 BEAD_0603 NO STUFF 150-220R@100MHz
C21 1UF 16V 10% X5R 0603 NO STUFF — PLACE NEAR CONNECTOR

MDIN_SDA_C — LB5 150-220R@100MHz BEAD_0603 COMMON — 3.5MIL — I2CC_SDA — BI 14.3A<> 16.2E<> 17.1D<>
C20 220PF 50V 5% NPO 0603 COMMON
5V — D6 BAV99 SOT23 100V 100MA COMMON

C583 8.2PF 0603 50V +/-0.5PF NPO CHANGED — L509 0.56uH 0603 CHANGED — MDIN_Yout_C — DACB_CVBS_OUT
C584 82PF 50V 5% NPO 0603 COMMON
C582 82PF 50V 5% NPO 0603 COMMON
C556 22PF 0603 50V 5% NPO COMMON — L504 1.8uH 0603 COMMON — MDIN_Cin_C
C557 270PF 50V 5% NPO 0603 COMMON
C555 330PF 50V 5% NPO 0603 COMMON
5V — D510 BAV99 SOT23 100V 100MA COMMON
R561 75 1% 0402 COMMON
R560 200 1% 0402 NO STUFF

keep stub short from the pin

MDIN_Cin_clamp — R554 18 5% 0402 COMMON — MINIDIN_Cin — OUT 14.2A< 15.2A<>
A3V3 — D506 BAV99 SOT23 100V 100MA COMMON
R555 56 5% 0402 COMMON

For STEREO GLASSES 3pin MiniDIN only:
Stuff bead!
And replace 0 Ohm resistor with 22OPF cap!

STEREO GLASSES BUFFER

Place close to MiniDIN connector!

5V — R3 10K 5% 0402 NO STUFF
17.5D> IN STEREO — R8 0 5% 0402 NO STUFF — STEREO_5V
5V — U1 SN74LVC1G08 SC70-5 NO STUFF — STEREO_BUF — R24 33 5% 0402 NO STUFF — SCL_C_STEREO
5V — C11 .1UF 10V 10% X5R 0402 NO STUFF

FOR DEBUG PURPOSES ONLY .. DEFAULT IS NO STUFF

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	DACB FILTERS, SYNC STRIPPER, MINIDIN CONNECTOR NORTH

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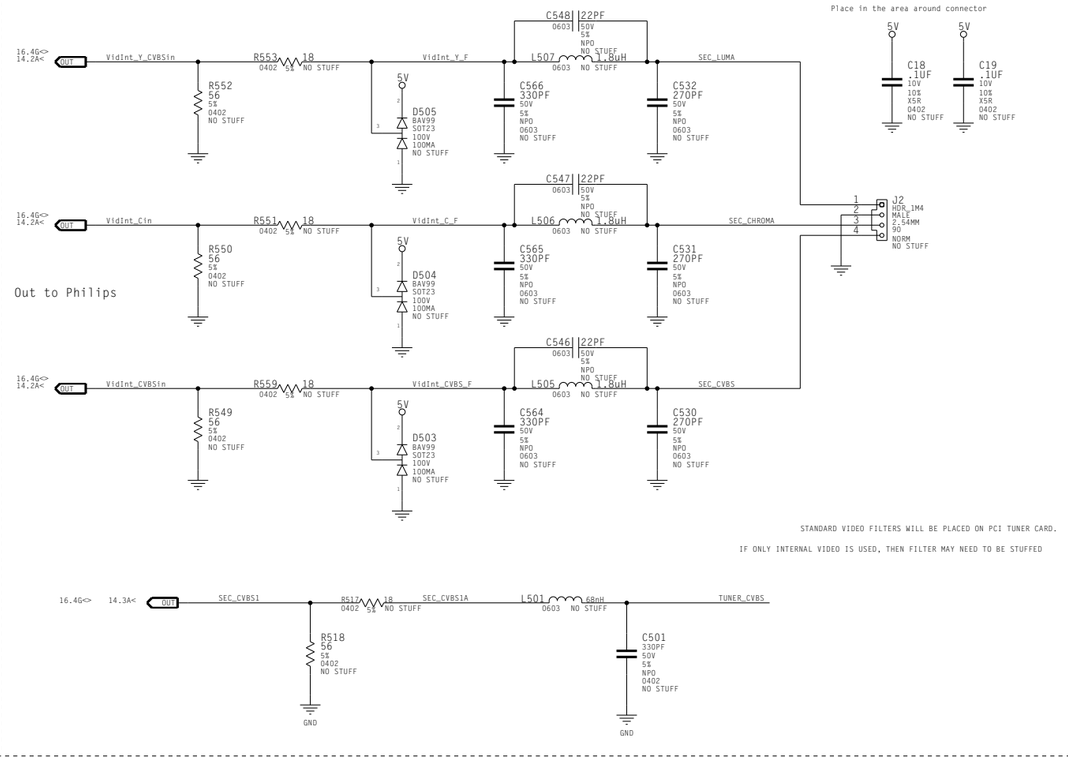
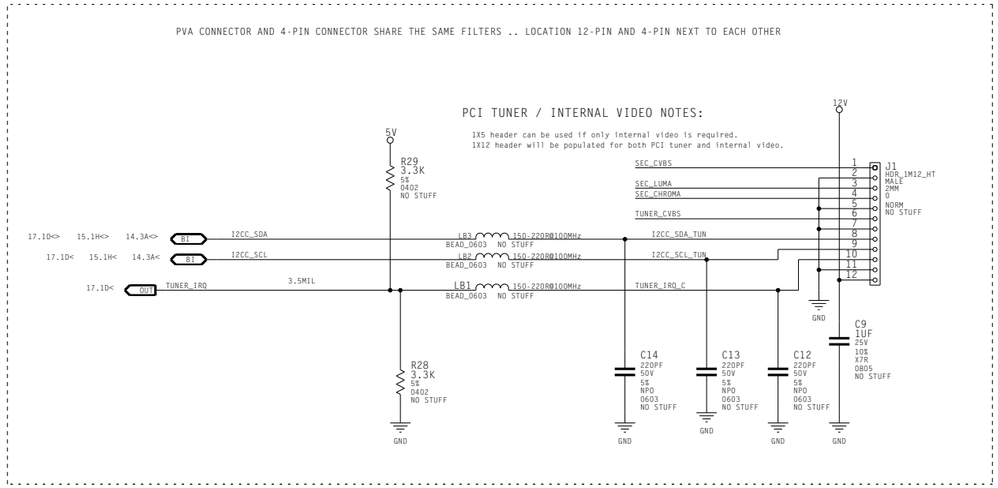
NV_PN	602-10216-0001-300		
ID	p216	PAGE	15 OF 25
NAME	bnichols	DATE	9-SEP-2004

4-Pin Video In, 12-pin Video In connectors

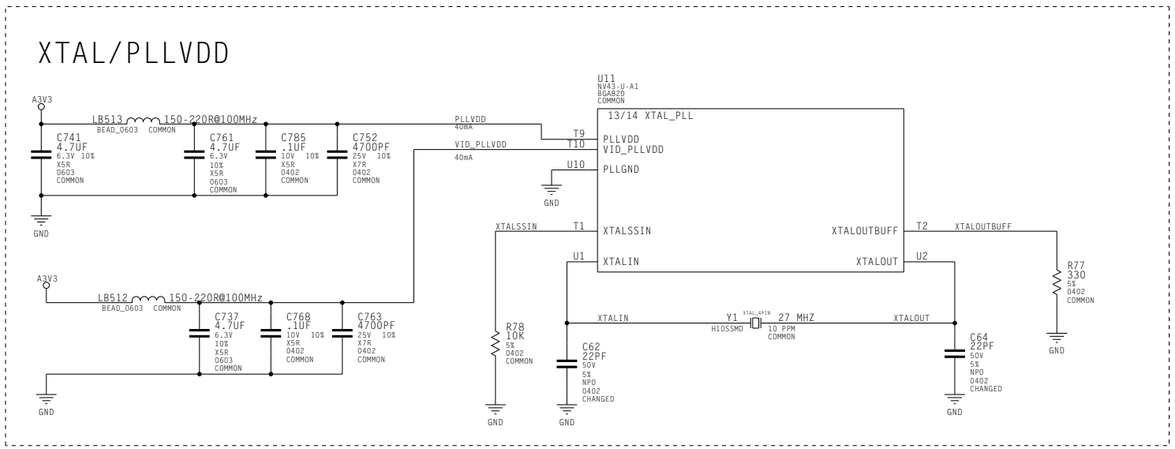
EXTERNAL 4-PIN VIDEO IN CONNECTOR



EXTERNAL 12-PIN PVA CONNECTOR



XTAL/PLLVDD



NETNAME	MIN_LINE_WIDTH	NET_SPACING_RULE
16.1A> 14.2A< BI VidInt_Y_CVBSin		20MIL
16.2A> 14.2A< BI VidInt_Cin		20MIL
16.2A> 14.2A< BI VidInt_CVBSin		20MIL
3.5MIL		
16.3A> 14.3A< BI SEC_CVBS1		20MIL
BI VidInt_Y_F		20MIL
BI VidInt_C_F		20MIL
BI VidInt_CVBS_F		20MIL
BI SEC_CVBS1A		20MIL
BI SEC_LUMA		20MIL
BI SEC_CHROMA		20MIL
BI SEC_CVBS		20MIL
BI TUNER_CVBS		20MIL
IN XTALIN	5MIL	
IN XTALOUT	5MIL	
IN PLLVDD	12MIL	
IN VID_PLLVDD	12MIL	

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	4-PIN & 12-PIN VIDEO HEADERS, XTAL

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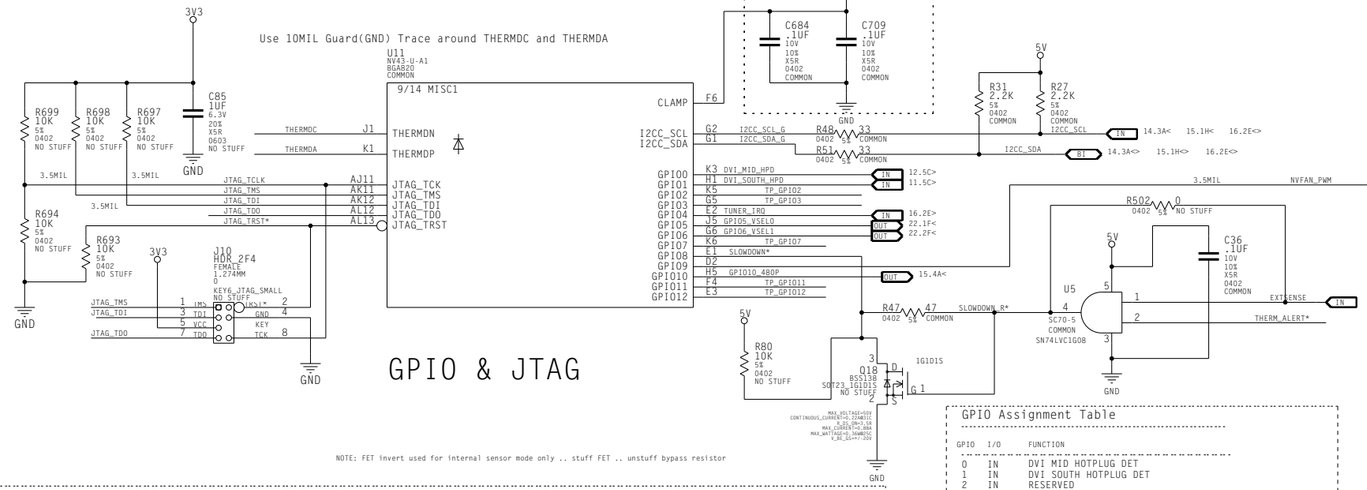
NV_PN	602-10216-0001-300		
ID	p216	PAGE	16 OF 25
NAME	bnichols	DATE	9-SEP-2004

GPIO & JTAG



NOTE: FET invert used for internal sensor mode only .. stuff FET .. unstuff bypass resistor

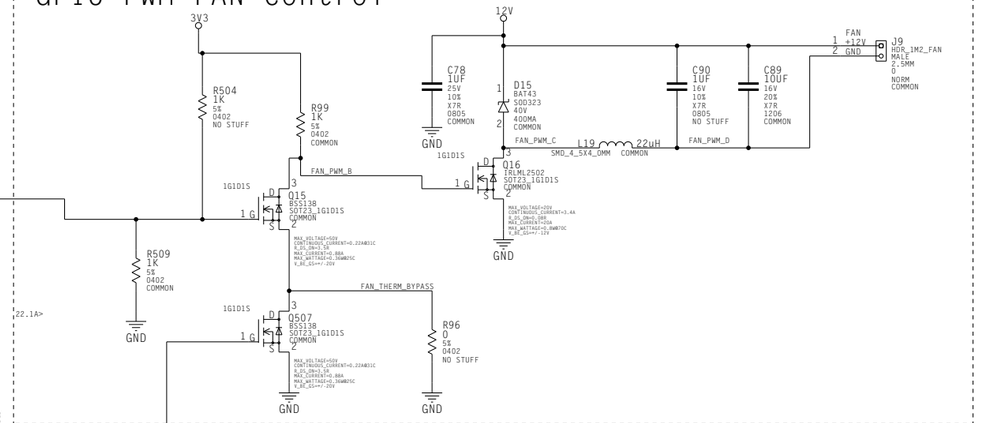
GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	DVI SOUTH HOTPLUG DET
2	IN	RESERVED
3	IN	RESERVED
4	IN	TUNER IRQ
5	OUT	NVVDD VOLTAGE SELECT 0
6	OUT	NVVDD VOLTAGE SELECT 1
7	IN	RESERVED
8	IN	EXTERNAL POWER PRESENT/THERM ALERT
9	OUT	PWM FAN
10	OUT	HD 480P SYNC STRIPPER SELECT
11	IN	RESERVED
12	IN	RESERVED

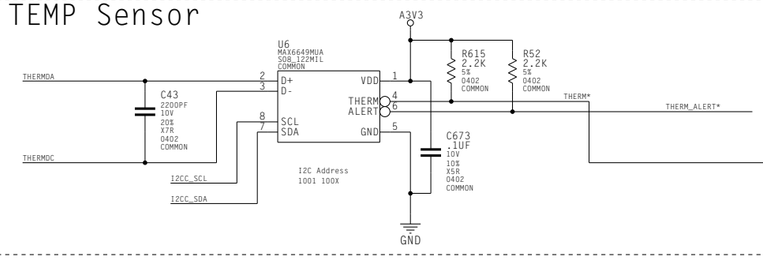
NOTE: THERM_ALERT* is generated when over temp condition is detected

GPIO PWM FAN Control

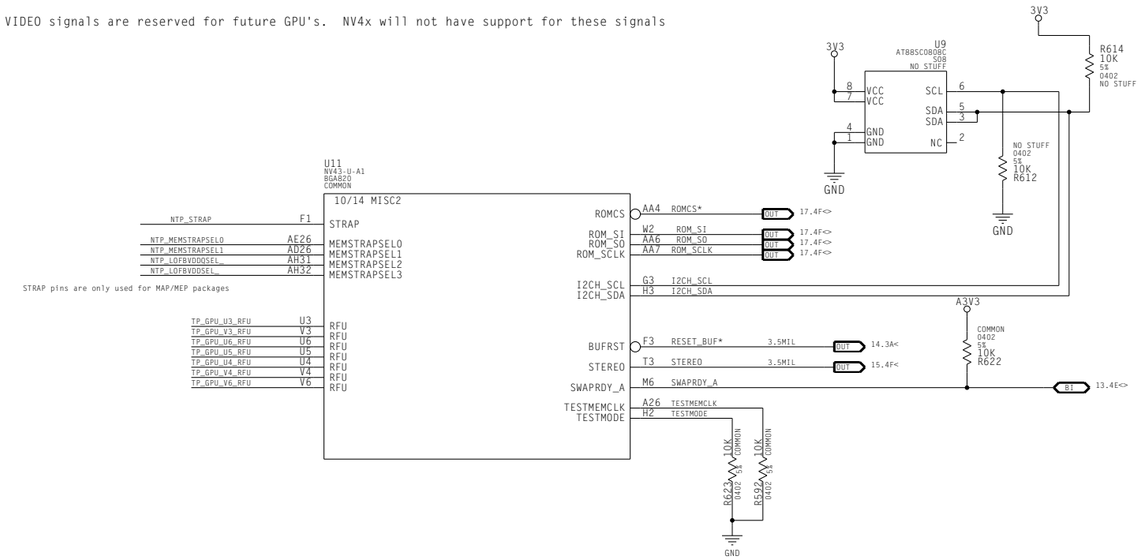
SW SIDE



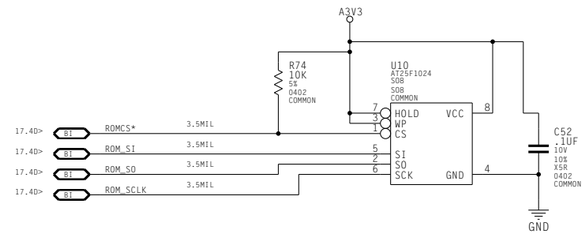
TEMP Sensor



AUDIO and VIDEO signals are reserved for future GPU's. NV4x will not have support for these signals



BIOS (serial)



SROM MAPPING

ROM	NV4x
SO	ROM_SO
SI	ROM_SI
SCK	ROM_SCK
CS*	ROM_CS*

NETNAME	MIN_LINE_WIDTH	VOLTAGE
THERMDC	10MIL	
THERMDA	10MIL	
FAN_PWM_B	12MIL	
FAN_PWM_C	12MIL	
FAN_PWM_D	12MIL	

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	JTAG, BIOS ROM, HDCP ROM, FAN CONTROL, TEMP SENSOR & GPIO's

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NV_PN	602-10216-0001-300		
ID	p216	PAGE	17 OF 25
NAME	bnichols	DATE	9-SEP-2004

BIOS, Straps, Misc

Straps

Assembly: BIOS

13.1G<> BI MIOAD<11..0>

0 MIOAD<0>
1 MIOAD<1>
2 MIOAD<2>
3 MIOAD<3>
4 MIOAD<4>
5 MIOAD<5>
6 MIOAD<6>
7 MIOAD<7>
8 MIOAD<8>
9 MIOAD<9>
10 MIOAD<10>
11 MIOAD<11>

14.3A<> 13.1G<> 13.1E<> BI MIOBD<11..0>

0 MIOBD<0>
1 MIOBD<1>
2 MIOBD<2>
3 MIOBD<3>
4 MIOBD<4>
5 MIOBD<5>
6 MIOBD<6>
7 MIOBD<7>
8 MIOBD<8>
9 MIOBD<9>
10 MIOBD<10>
11 MIOBD<11>

STUFF 2.0K

BOND OPTION 0 = DISCRETE

A3V3

R15 10K 0402 5% NO STUFF — MIOAD<1> — R16 2K 0402 5% CHANGED
R511 10K 0402 5% NO STUFF — MIOBD<0> — R512 2K 0402 5% CHANGED
R514 10K 0402 5% NO STUFF — MIOBD<1> — R513 2K 0402 5% CHANGED
R515 10K 0402 5% NO STUFF — MIOBD<8> — R516 2K 0402 5% CHANGED
R14 2K 0402 5% CHANGED — MIOBD<9> — R13 10K 0402 5% NO STUFF

CHANGED FROM MIOA<2,3,4,5>

R63 2K 0402 5% CHANGED — MIOBD<4> — R64 10K 0402 5% NO STUFF
R66 2K 0402 5% CHANGED — MIOBD<5> — R65 10K 0402 5% NO STUFF
R58 2K 0402 5% CHANGED — MIOBD<3> — R57 10K 0402 5% NO STUFF

13.5H<> BI MIOA_HSYNC

R510 2K 0402 5% CHANGED — MIOBD<11> — R520 10K 0402 5% NO STUFF

CHANGED FROM:MIOA_HSYNC

R82 10K 0402 5% NO STUFF — MIOBD<10> — R79 2K 0402 5% CHANGED

R83, R80 DELETED

R55 2K 0402 5% CHANGED — MIOAD<2> — R56 10K 0402 5% NO STUFF

R18 2K 0402 5% CHANGED — MIOAD<0> — R17 10K 0402 5% NO STUFF
R11 2K 0402 5% CHANGED — MIOAD<6> — R12 10K 0402 5% NO STUFF
R19 2K 0402 5% CHANGED — MIOAD<8> — R20 10K 0402 5% NO STUFF
R9 2K 0402 5% CHANGED — MIOAD<9> — R10 10K 0402 5% NO STUFF

GND

NV_STRAP_0

BIT	FUNCTION	MAP/MCP/SQUISH PIN (STL Name)	NORMAL PIN (STL Name)	REQUIRED ON BOARD?
0	PCI_AD	NV_PEXTDEV_BOOT_0_STRAP_PCI_AD_NORMAL	NV_PEXTDEV_BOOT_0_STRAP_PCI_AD_NORMAL	PCI/AGP_ONLY
1	SUB_VENDOR	MISC0[0] (ctrl=a_data[0])	MISC0[0] (ctrl=a_data[0])	NO
2	RAMCFG[0]	MISC0[1] (ctrl=a_data[1])	MISC0[1] (ctrl=a_data[1])	NO
3	RAMCFG[1]	MISC0[2] (ctrl=a_data[2])	MISC0[2] (ctrl=a_data[2])	NO
4	RAMCFG[2]	MISC0[3] (ctrl=a_data[3])	MISC0[3] (ctrl=a_data[3])	NO
5	RAMCFG[3]	MISC0[4] (ctrl=a_data[4])	MISC0[4] (ctrl=a_data[4])	NO
6	CRYSTAL0	MISC0[5] (ctrl=a_data[5])	MISC0[5] (ctrl=a_data[5])	NO
7	TVMODE[0]	MISC0[6] (ctrl=a_data[6])	MISC0[6] (ctrl=a_data[6])	NO
8	TVMODE[1]	MISC0[7] (ctrl=a_data[7])	MISC0[7] (ctrl=a_data[7])	NO
9	AGPRX	MISC0[8] (ctrl=a_data[8])	MISC0[8] (ctrl=a_data[8])	NO
10	AGP_SBA	NV_PEXTDEV_BOOT_0_STRAP_AGP_SBA_DISABLED	NV_PEXTDEV_BOOT_0_STRAP_AGP_SBA_DISABLED	NO
11	AGP_FASTWR	NV_PEXTDEV_BOOT_0_STRAP_AGP_FASTWR_DISABLED	NV_PEXTDEV_BOOT_0_STRAP_AGP_FASTWR_DISABLED	NO
12	PCI_DEVID[0]	MISC0[9] (ctrl=a_data[9])	MISC0[9] (ctrl=a_data[9])	NO
13	PCI_DEVID[1]	MISC0[10] (ctrl=a_data[10])	MISC0[10] (ctrl=a_data[10])	NO
14	AGP	NV_PEXTDEV_BOOT_0_STRAP_BUS_TYPE_AGP	NV_PEXTDEV_BOOT_0_STRAP_BUS_TYPE_AGP	PCI/AGP_ONLY
15	FP_IFACE	NV_PEXTDEV_BOOT_0_STRAP_FP_IFACE_12BIT	NV_PEXTDEV_BOOT_0_STRAP_FP_IFACE_12BIT	NO
16	USER[0]	MISC0[11] (ctrl=a_data[11])	MISC0[11] (ctrl=a_data[11])	NO
17	USER[1]	MISC0[12] (ctrl=a_data[12])	MISC0[12] (ctrl=a_data[12])	NO
18	USER[2]	MISC0[13] (ctrl=a_data[13])	MISC0[13] (ctrl=a_data[13])	NO
19	USER[3]	MISC0[14] (ctrl=a_data[14])	MISC0[14] (ctrl=a_data[14])	NO
20	PCI_DEVID[2]	MISC0[15] (ctrl=a_data[15])	MISC0[15] (ctrl=a_data[15])	NO
21	PCI_DEVID[3]	MISC0[16] (ctrl=a_data[16])	MISC0[16] (ctrl=a_data[16])	NO
22	CRYSTAL1	MISC0[17] (ctrl=a_data[17])	MISC0[17] (ctrl=a_data[17])	NO
23	FB[0]			NO
24	FB[1]			NO
25	BR	ROM_SI (Rom_si)	ROM_SI (Rom_si)	MCH1P
26	BR_128M	NV_PEXTDEV_BOOT_0_STRAP_BR_REG_128M_DISABLED	NV_PEXTDEV_BOOT_0_STRAP_BR_REG_128M_DISABLED	NO
27	BR_AGP	NV_PEXTDEV_BOOT_0_STRAP_BR_AGP_DEV_DISABLED	NV_PEXTDEV_BOOT_0_STRAP_BR_AGP_DEV_DISABLED	NO
28	BR_ID	NV_PEXTDEV_BOOT_0_STRAP_BR_ID_DEV_DISABLED	NV_PEXTDEV_BOOT_0_STRAP_BR_ID_DEV_DISABLED	NO
29	ROMTYPE[0]	MISC0[18] (ctrl=a_data[18])	MISC0[18] (ctrl=a_data[18])	YES
30	ROMTYPE[1]	MISC0[19] (ctrl=a_data[19])	MISC0[19] (ctrl=a_data[19])	YES

NV_STRAP_1

BIT	FUNCTION	MAP/MCP/SQUISH PIN (STL Name)	NORMAL PIN (STL Name)	REQUIRED ON BOARD?
0	1394	NV_PEXTDEV_BOOT_1_STRAP_1_1394_DISABLED	NV_PEXTDEV_BOOT_1_STRAP_1_1394_DISABLED	NO
1	1394_PHY	NV_PEXTDEV_BOOT_1_STRAP_1_1394_PHY_DISABLED	NV_PEXTDEV_BOOT_1_STRAP_1_1394_PHY_DISABLED	NO
2	1394_PHY_PWRCLASS[0]	[]	[]	NO
3	1394_PHY_PWRCLASS[1]	[]	[]	NO
4	VGA_DEVICE	NV_PEXTDEV_BOOT_1_STRAP_1_VGA_DEVICE_ENABLED	NV_PEXTDEV_BOOT_1_STRAP_1_VGA_DEVICE_ENABLED	NO
5	MEM_LIB_SWAP	NV_PEXTDEV_BOOT_1_STRAP_1_MEM_LIB_SWAP_DISABLED	NV_PEXTDEV_BOOT_1_STRAP_1_MEM_LIB_SWAP_DISABLED	NO
6	MEM_LIB_SCRATCH	NV_PEXTDEV_BOOT_1_STRAP_1_MEM_LIB_SCRATCH_DISABLED	NV_PEXTDEV_BOOT_1_STRAP_1_MEM_LIB_SCRATCH_DISABLED	NO
7	BR_BASIC_BIOSTIMLY	NV_PEXTDEV_BOOT_1_STRAP_1_BR_BASIC_BIOSTIMLY_ENABLED	NV_PEXTDEV_BOOT_1_STRAP_1_BR_BASIC_BIOSTIMLY_ENABLED	NO
8	SUBSYSTEM_USER	NV_PEXTDEV_BOOT_1_STRAP_1_SUBSYSTEM_USER_DISABLED	NV_PEXTDEV_BOOT_1_STRAP_1_SUBSYSTEM_USER_DISABLED	NO
9	I_BOARD	NV_PEXTDEV_BOOT_1_STRAP_1_I_BOARD_D	NV_PEXTDEV_BOOT_1_STRAP_1_I_BOARD_D	NO
10	FPR_FACE	NV_PEXTDEV_BOOT_1_STRAP_1_FPR_FACE_12BIT	NV_PEXTDEV_BOOT_1_STRAP_1_FPR_FACE_12BIT	NO
11	PEX_Pll_EN_TERM100	MISC0[20] (ctrl=a_data[0])	MISC4[0] (ctrl=a_data[0])	YES
12	I2GIO_PADCFG_LUT_ADR[0]	MISC0[21] (ctrl=a_data[1])	MISC4[1] (ctrl=a_data[1])	YES
13	I2GIO_PADCFG_LUT_ADR[1]	MISC0[22] (ctrl=a_data[2])	MISC4[2] (ctrl=a_data[2])	YES
14	I2GIO_PADCFG_LUT_ADR[2]	MISC0[23] (ctrl=a_data[3])	MISC4[3] (ctrl=a_data[3])	YES

REG: NV_PEXTDEV_BOOT_0

Bit	Signal	VALUE_ID	VALUEs	
00:	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED 1 NORMAL	
01:	SUB_VENDOR	SUB_VENDOR	0 NO_BIOS 1 read from BIOS	
02:	RAM_CFG_0	RAM_CFG[3:0]	0000 RFU 0001 RFU 0010 RFU 0011 RFU 0100 RFU 0101 8Mx32DDR3,INFINEON/SAMSUNG 0110 RFU 0111 8Mx32DDR3,SAMSUNG (SCREENED)	1000 RFU 1001 RFU 1010 RFU 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 RFU
03:	RAM_CFG_1			
04:	RAM_CFG_2			
05:	RAM_CFG_3			
06:	CRYSTAL_0	CRYSTALL[1:0]	00 13.500 Mhz 01 14.31818 Mhz 10 27.000 Mhz 11 unknown	
22:	CRYSTAL_1			
07:	TV_MODE_0	TV_MODE[1:0]	00 SECAM 01 NTSC 10 PAL 11 CRT	
08:	TV_MODE_1			
09:	AGPRXenable	AGP_30_8x	0 AGP8x enabled 1 AGP4x disabled	
10:	AGP_SBA	AGP_SBA[0]	0 SBA enabled 1 SBA disabled	
11:	AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled	
12:	PCI_DEVID_0	PCI_DEVID[3:0]	0000 0x140 ... 1111 0x014F 0000 (default 0x140)	
13:	PCI_DEVID_1		0101 (0x145)	
20:	PCI_DEVID_2			
21:	PCI_DEVID_3			
14:	BUS_TYPE	BUS_TYPE[0]	0 PCI 1 AGP	
15:	FP_IFACE	FP_IFACE[0]	0 24Bit 1 12Bit (DEFAULT)	
23:	FB_0	FB[1:0]	00 64M 01 128M 10 256M (DEFAULT) 11 512M	
24:	FB_1			
25:	BR	BR[0]	0 BRIDGE disabled 1 BRIDGE enabled	
26:	BR_128M	BR bits are ignored if BRIDGE is disabled		
27:	BR_AGP			
28:	BR_ID			
29:	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F 10 Serial_SST45VF 11 RFU	
30:	ROM_TYPE_1			
16:	USER_0	STRAP_USER[3:0]	0000 (default)	
17:	USER_1			
18:	USER_2			
19:	USER_3			

REG: NV_STRAP_1

Bit	Signal	VALUE_ID	VALUEs
11:	PEX_PLL_EN_TERM100		0 (default -- internal term on)
12:	3GIO_PADCFG_LUT_ADR[0]		
13:	3GIO_PADCFG_LUT_ADR[1]		
14:	3GIO_PADCFG_LUT_ADR[2]		

Mechanical parts

155-00003-0000-000
SCREW HEX JACK 4-40 x 12.1MM STANDARD

MEC1 HEX_JACK_SCREW STD COMMON
MEC2 HEX_JACK_SCREW STD COMMON
MEC3 HEX_JACK_SCREW STD COMMON
MEC4 HEX_JACK_SCREW STD COMMON

151-10001-0006-001 -- > DB15-DVI-MDIN

BKT1 DB153152_DVI1552_MDIN490_TAB AT4_1X_TOP COMMON
1
GND
MECH. MOUNTING TOP

155-00001-000
MEC5 PH_4.40X3/16_SCREW STD COMMON

095-0001-005
MEC6 NVTM32_DOOM3 GPU COMMON

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	BIOS STRAPS & MECHANICALS

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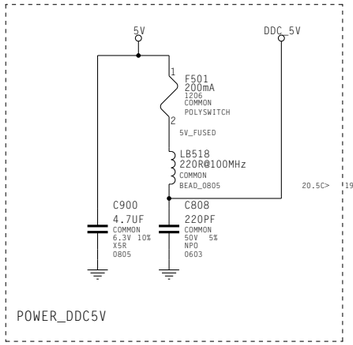
SANTA CLARA, CA 95050, USA

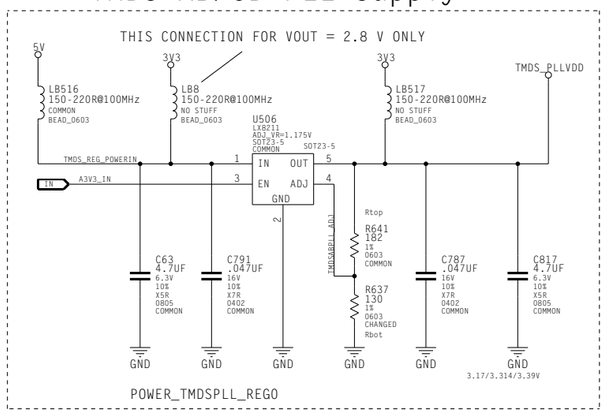
NV_PN	602-10216-0001-300		
ID	p216	PAGE	18 OF 25
NAME	bnichols	DATE	9-SEP-2004

Power Supply ... TMDS/A3V3/FBVDD

DDC 5V

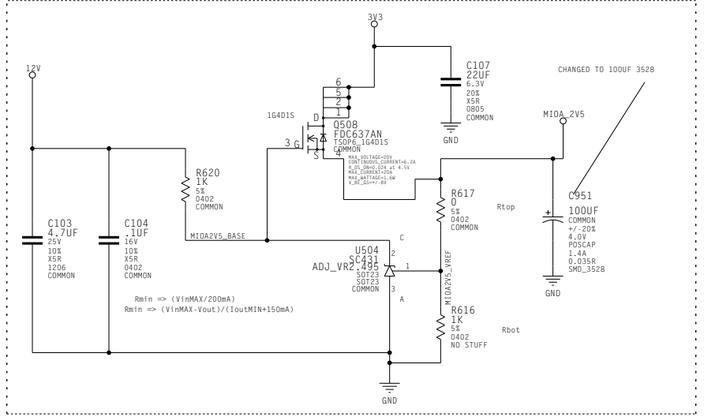


TMDS AB/CD PLL Supply



Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+(100/182))

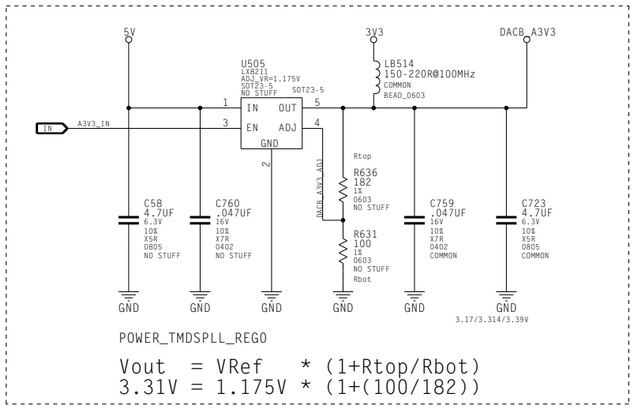
MIOA_VDDQ



Vref = 2.5V
Vout = 2.495(1+Rtop/Rbot) + (Iref + Rtop)
For Vout = Vref (Rtop = 0ohm, Rbot = NO STUFF)

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
BI 5V_FUSED		12MIL	5V
DDC_5V		12MIL	5V
3V3		12MIL	3.3V
5V		25MIL	5V
BI TMDSABPLL_ADJ		10MIL	3.3V
TMDS_PLLVDD		12MIL	3.3V
12V	5.5A	35MIL	12V
MIOA_2V5	1A	12MIL	2.5V
BI MIOA2V5_VREF		10MIL	
GND		35MIL	0V
BI DACB_A3V3_ADJ		10MIL	3.3V
DACB_A3V3		12MIL	3.3V

DACB Supply



Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+(100/182))

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	POWER SUPPLY: DDC5V, TMDS PLL VDD LINEAR, DACB VDD LINEAR,

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SANTA CLARA, CA 95050, USA

NV_PN	602-10216-0001-300		
ID	p216	PAGE	19 OF 25
NAME	bnichols	DATE	9-SEP-2004

Power Supply .. ISL6549 5V/A3V3

A3V3: 3.3V@1A

5V_OUT: 5V@1A

FETS ARE GOOD FOR 6A OUTPUT

LAYOUT NOTE:
HAVE LARGE D2PAK PAD FOR UP TO 2W DISSIPATION HERE!
BULK ON 5V RAIL DECOUPLES THIS CONNECTION

TRY TO GET SANYO CV-EX SERIES HERE .. NMR!

NEED 1100PF X7R 5% VALUE .. NMR!

ALTERNATE Analog 3.3V Power Supply

PLACE CLOSE TO ISL6549 A3V3 OUTPUT
USE CAPS FROM ISL6549 A3V3 OUTPUT STAGE
STUFF ONLY IF ISL6549 NOT STUFFED
PLACE WITHIN 2cm AREA

Vout = VRef * (1+Rbot/Rtop)
3.31V = 1.25V * (1+1650/1000)

LOW COST ALTERNATE 5V REGULATOR

ALL RESISTOR VALUES NEED ADJUSTMENT FOR BOM

LAYOUT NOTE:
ADD MIN 100MM^2 COLLECTOR COPPER AROUND THIS DPAK FOOTPRINT FOR HEAT DISSAPATION

ALWAYS STUFF

STUFF ONLY ZENER OR 3-PIN REGULATOR!

HERE IN CASE 3V3 COMES UP FIRST!

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	POWER SUPPLY: 5V & A3V3 SWITCHER AND LINEAR's

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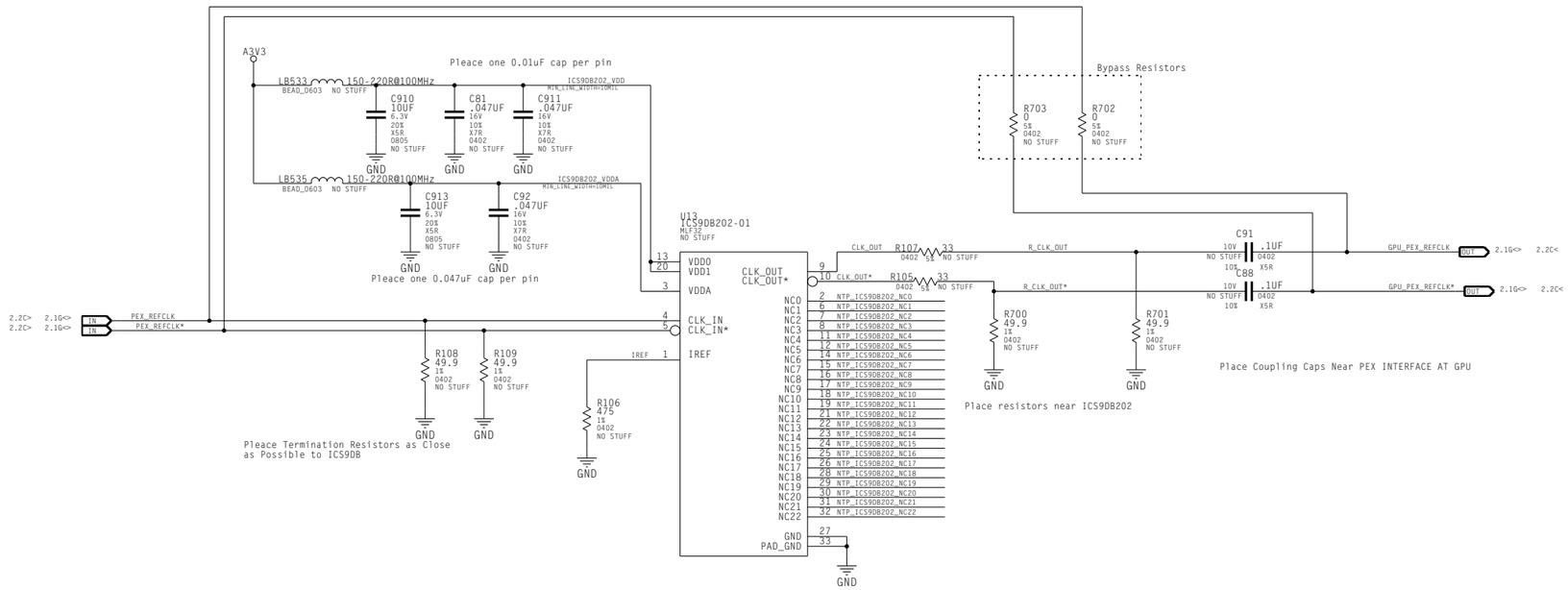
NV_PN	602-10216-0001-300		
ID	p216	PAGE	20 OF 25
NAME	bnichols	DATE	9-SEP-2004

GPU PEX Reference Clock ZDB

NET	DIFFPAIR	NET_SPACING_RULE
R_CLK_OUT	R_CLK_OUT	20MIL_G2G_30MIL_USER_DIFF
R_CLK_OUT*	R_CLK_OUT	20MIL_G2G_30MIL_USER_DIFF
CLK_OUT	CLK_OUT	20MIL_G2G_30MIL_USER_DIFF
CLK_OUT*	CLK_OUT	20MIL_G2G_30MIL_USER_DIFF



ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	PEX ZERO DELAY BUFFER

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NV_PN	602-10216-0001-300		
ID	p216	PAGE	21 OF 25
NAME	bnichols	DATE	9-SEP-2004

External Power Connector

12V RAIL SWITCH

PEX1V2 = 1.2V @ 2.2A

NVVDD Voltage Selection

Place close to NVVDD feedback loop!

NV_VSEL1	NV_VSEL0	NVVDD
0	0	1.1V
0	1	1.2V (default)
1	0	1.3V
1	1	1.4V

NVVDD = 1.2-1.4V@32A

NVVDD = 0.6v * (Rt+Rb)/Rb
1.40V = 0.6V * (1.18k+887)/887
1.20V = 0.6V * (1.18k+887||1.91k)/(887||1.91k)

FBVDD,FBVDDQ: 1.8-2.2V@6.5A

1V2 = 0.6V * (Rt+Rb)/Rb
1.2V = 0.6V * (1+1)/1
1.25V = 0.6V * (1.1+1.02)/1.02
1.3V = 0.6V * (1.4+1.21)/1.21

REFIN = 3.3V * Rb/(Rt+Rb)
3.3V = 3.3V * 0/(1k+ 0)

REFOUT: Phase control
HI: 0 degree phase
Float:180 degree phase

VOUT = REFIN * (Rt+Rb)/Rb
2.041 = 1.65 * (365 + 1.54k)/1.54k

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	POWER SUPPLY: ISL6534 NVVDD, FBVDD, PEX1V2

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NV_PN	602-10216-0001-300		
ID	p216	PAGE	22 OF 25
NAME	bnichols	DATE	9-SEP-2004

*** Signal Cross-Reference for the entire design ***

5V_ENBL*	11.5A< 20.5G>
5V_FUSED	19.1A 19.1G<>
A3V3_IN	19.2B< 19.4A< 20.5C> 20.5C>
CLK_OUT	21.1G<> 21.3D
CLK_OUT*	21.1G<> 21.3D
DACA_BLUE	9.1A<> 9.5D
DACA_BLUE_C	9.1A<> 9.4F> 11.3G<
DACA_R_F	9.1A<> 9.5E
DACA_GREEN	9.1A<> 9.4D
DACA_GREEN_C	9.1A<> 9.4F> 11.3G<
DACA_G_F	9.1A<> 9.4E
DACA_HSYNC_C	9.3F> 9.3F> 11.3G<
DACA_RED	9.1A<> 9.4D
DACA_RED_C	9.1A<> 9.4F> 11.3G<
DACA_RSET	9.1A< 9.3B
DACA_R_F	9.1A<> 9.4E
DACA_VDD	9.1A< 9.3B
DACA_VREF	9.1A< 9.3B
DACA_VSYNC_C	9.3F> 9.3F> 11.3G<
DACBC_B_F	10.1A<> 10.5E
DACBC_G_F	10.1A<> 10.4E
DACBC_R_F	10.1A<> 10.4E
DACB_A3V3_ADJ	19.2G<> 19.4B
DACB_CVBS_OUT	15.1A> 15.2G 15.5D
DACB_C_OUT	15.1A> 15.2C 15.4C 15.5D
DACB_PB_OUT	15.1A> 15.1C 15.3C 15.5D
DACB_RSET	15.2A< 15.5B
DACB_VDD	15.2A< 15.4B
DACB_VREF	15.2A< 15.5B
DACC_BLUE	10.1A<> 10.4C 10.5D
DACC_BLUE_C	10.1A<> 10.4G> 12.3G<
DACC_GREEN	10.1A<> 10.4C 10.4D
DACC_GREEN_C	10.1A<> 10.4G> 12.3G<
DACC_HSYNC_C	10.3F> 12.3G<
DACC_RED	10.1A<> 10.4C 10.4D
DACC_RED_C	10.1A<> 10.4G> 12.3G<
DACC_RSET	10.1A<> 10.4A
DACC_VDD	10.1A<> 10.4A
DACC_VREF	10.1A<> 10.4A
DACC_VSYNC_C	10.3F> 12.3G<
DVI_MID_HPD	12.5C> 17.1D<
DVI_SOUTH_HPD	11.5C> 17.1D<
EXTSENSE	17.2E< 22.1A>
FAN_PWM_B	17.1F 17.5G<>
FAN_PWM_C	17.1G 17.5G<>
FAN_PWM_D	17.1G 17.5G<>
FBAD<0>	3.1B 4.4C
FBAD<63..0>	3.1A<> 4.1G<> 4.4B<>
FBAD<1>	3.1B 4.4C
FBAD<2>	3.1B 4.4C
FBAD<3>	3.1B 4.4C
FBAD<4>	3.1B 4.4C
FBAD<5>	3.1B 4.4C
FBAD<6>	3.1B 4.4C
FBAD<7>	3.1B 4.4C
FBAD<8>	3.1B 4.4D
FBAD<9>	3.1B 4.4D
FBAD<10>	3.1B 4.4D
FBAD<11>	3.1B 4.4D
FBAD<12>	3.1B 4.4D
FBAD<13>	3.1B 4.4D
FBAD<14>	3.1B 4.4D
FBAD<15>	3.1B 4.4D
FBAD<16>	3.1B 4.4E
FBAD<17>	3.1B 4.4E
FBAD<18>	3.1B 4.4E
FBAD<19>	3.1B 4.4E
FBAD<20>	3.1B 4.4E
FBAD<21>	3.1B 4.4E
FBAD<22>	3.1B 4.4E
FBAD<23>	3.2B 4.4E
FBAD<24>	3.2B 4.4E
FBAD<25>	3.2B 4.4E
FBAD<26>	3.2B 4.4E
FBAD<27>	3.2B 4.4E
FBAD<28>	3.2B 4.4E
FBAD<29>	3.2B 4.4E
FBAD<30>	3.2B 4.4E
FBAD<31>	3.2B 4.4E
FBAD<32>	3.2B 4.5C
FBAD<33>	3.2B 4.5C
FBAD<34>	3.2B 4.5C
FBAD<35>	3.2B 4.5C
FBAD<36>	3.2B 4.5C
FBAD<37>	3.2B 4.5C
FBAD<38>	3.2B 4.5C
FBAD<39>	3.2B 4.5C
FBAD<40>	3.2B 4.5D
FBAD<41>	3.2B 4.5D
FBAD<42>	3.2B 4.5D
FBAD<43>	3.2B 4.5D
FBAD<44>	3.2B 4.5D
FBAD<45>	3.2B 4.5D
FBAD<46>	3.2B 4.5D
FBAD<47>	3.2B 4.5D
FBAD<48>	3.2B 4.5E
FBAD<49>	3.2B 4.5E
FBAD<50>	3.2B 4.5E
FBAD<51>	3.2B 4.5E
FBAD<52>	3.2B 4.5E
FBAD<53>	3.3B 4.5E
FBAD<54>	3.3B 4.5E
FBAD<55>	3.3B 4.5E
FBAD<56>	3.3B 4.5E
FBAD<57>	3.3B 4.5E
FBAD<58>	3.3B 4.5E
FBAD<59>	3.3B 4.5E
FBAD<60>	3.3B 4.5E
FBAD<61>	3.3B 4.5E
FBAD<62>	3.3B 4.5E
FBAD<63>	3.3B 4.5E
FBADQM<0>	3.3B 4.4B 4.4C
FBADQM<7..0>	3.3A> 4.1G<> 4.4B<>
FBADQM<1>	3.3B 4.4B 4.4D
FBADQM<2>	3.3B 4.4B 4.4E
FBADQM<3>	3.3B 4.4B 4.4E
FBADQM<4>	3.3B 4.4B 4.5C
FBADQM<5>	3.3B 4.4B 4.5D
FBADQM<6>	3.3B 4.4B 4.5E
FBADQM<7>	3.3B 4.4B 4.5E
FBADQS_RN<0>	3.4B 4.1G<> 4.4B 4.4C
FBADQS_RN<7..0>	3.4A<> 4.4B<>
FBADQS_RN<1>	3.4B 4.1G<> 4.4B 4.4D
FBADQS_RN<2>	3.4B 4.1G<> 4.4B 4.4E
FBADQS_RN<3>	3.4B 4.1G<> 4.4B 4.4E
FBADQS_RN<4>	3.4B 4.1G<> 4.4B 4.5C
FBADQS_RN<5>	3.4B 4.1G<> 4.5B 4.5D
FBADQS_RN<6>	3.4B 4.1G<> 4.5B 4.5E
FBADQS_RN<7>	3.4B 4.1G<> 4.5B 4.5E
FBADQS_WP<0>	3.3B 4.1G<> 4.4C 4.5B
FBADQS_WP<7..0>	3.3A<> 4.5B<>
FBADQS_WP<1>	3.3B 4.1G<> 4.4D 4.5B
FBADQS_WP<2>	3.3B 4.1G<> 4.4E 4.5B
FBADQS_WP<3>	3.3B 4.1G<> 4.4E 4.5B
FBADQS_WP<4>	3.3B 4.1G<> 4.5B 4.5C
FBADQS_WP<5>	3.3B 4.1G<> 4.5B 4.5D
FBADQS_WP<6>	3.3B 4.1G<> 4.5B 4.5E
FBADQS_WP<7>	3.4B 4.1G<> 4.5B 4.5E
FBA_CLKO	3.3D> 4.1G< 4.2A< 4.2D
FBA_CLKO*	3.4D> 4.1G< 4.2A< 4.2D
FBA_CLK1	3.4D> 4.1G< 4.2D 4.2D<
FBA_CLK1*	3.4D> 4.1G< 4.2D 4.2D<
FBA_CMD<0>	3.2C 4.1B 4.1D
FBA_CMD<26..0>	3.2D> 4.1A< 4.1C 4.1D 4.1G<
FBA_CMD<1>	3.3C 4.1B 4.1E
FBA_CMD<2>	3.3C 4.1B 4.1D
FBA_CMD<3>	3.3C 4.1B 4.1E
FBA_CMD<4>	3.3C 4.1E 4.2D
FBA_CMD<5>	3.3C 4.1E 4.2D
FBA_CMD<6>	3.3C 4.1E 4.2D
FBA_CMD<8>	3.3C 4.1B 4.1E
FBA_CMD<9>	3.3C 4.1B 4.1E
FBA_CMD<10>	3.3C 4.2B 4.2E
FBA_CMD<11>	3.3C 3.3G 4.2B 4.2E
FBA_CMD<12>	3.3C 4.2B 4.2E
FBA_CMD<13>	3.3C 4.1D 4.1E
FBA_CMD<14>	3.3C 4.1B 4.1E
FBA_CMD<15>	3.3C 4.1B 4.1E
FBA_CMD<16>	3.3C 4.1B 4.1E
FBA_CMD<17>	3.3C 4.1B 4.1E
FBA_CMD<18>	3.3C 4.2B 4.2E
FBA_CMD<19>	3.3C 4.1B 4.1E
FBA_CMD<20>	3.3C 4.1B 4.1E
FBA_CMD<21>	3.3C 4.1B 4.1E
FBA_CMD<22>	3.3C 4.1B 4.1D
FBA_CMD<23>	3.3C 4.1B 4.1E
FBA_CMD<24>	3.3C 4.1B 4.1D
FBA_CMD<25>	3.3C 4.1B 4.1E
FBA_PLLAVDD	3.1F< 3.4C
FBA_PLLVDD	3.1F< 3.4C 3.4E
FBA_REFCLK	3.1F< 3.4C
FBA_REFCLK*	3.1F< 3.4C
FBA_VREF_ADDR0	4.2G<> 4.3C
FBA_VREF_ADDR1	4.2G<> 4.3F
FBA_VREF_DATA0	4.2G<> 4.3C
FBA_VREF_DATA1	4.2G<> 4.3F
FBCD<0>	6.1B 7.4C
FBCD<63..0>	6.1A<> 7.1G<> 7.48<>
FBCD<1>	6.1B 7.4C
FBCD<2>	6.1B 7.4C
FBCD<3>	6.1B 7.4C
FBCD<4>	6.1B 7.4C
FBCD<5>	6.1B 7.4C
FBCD<6>	6.1B 7.4C
FBCD<7>	6.1B 7.4C
FBCD<8>	6.1B 7.4D
FBCD<9>	6.1B 7.4D
FBCD<10>	6.1B 7.4D
FBCD<11>	6.1B 7.4D
FBCD<12>	6.1B 7.4D
FBCD<13>	6.1B 7.4D
FBCD<14>	6.1B 7.4D
FBCD<15>	6.1B 7.4D
FBCD<16>	6.1B 7.4E
FBCD<17>	6.1B 7.4E
FBCD<18>	6.1B 7.4E
FBCD<19>	6.1B 7.4E
FBCD<20>	6.1B 7.4E
FBCD<21>	6.1B 7.4E
FBCD<22>	6.2B 7.4E
FBCD<23>	6.2B 7.4E
FBCD<24>	6.2B 7.4E
FBCD<25>	6.2B 7.4E
FBCD<26>	6.2B 7.4E
FBCD<27>	6.2B 7.4E
FBCD<28>	6.2B 7.4E
FBCD<29>	6.2B 7.4E
FBCD<30>	6.2B 7.4E
FBCD<31>	6.2B 7.4E
FBCD<32>	6.2B 7.5C
FBCD<33>	6.2B 7.5C
FBCD<34>	6.2B 7.5C
FBCD<35>	6.2B 7.5C
FBCD<36>	6.2B 7.5C
FBCD<37>	6.2B 7.5C
FBCD<38>	6.2B 7.5C
FBCD<39>	6.2B 7.5C
FBCD<40>	6.2B 7.5D
FBCD<41>	6.2B 7.5D
FBCD<42>	6.2B 7.5D
FBCD<43>	6.2B 7.5D
FBCD<44>	6.2B 7.5D
FBCD<45>	6.2B 7.5D
FBCD<46>	6.2B 7.5D
FBCD<47>	6.2B 7.5D
FBCD<48>	6.2B 7.5E
FBCD<49>	6.2B 7.5E
FBCD<50>	6.2B 7.5E
FBCD<51>	6.2B 7.5E
FBCD<52>	6.3B 7.5E
FBCD<53>	6.3B 7.5E
FBCD<54>	6.3B 7.5E
FBCD<55>	6.3B 7.5E
FBCD<56>	6.3B 7.5E
FBCD<57>	6.3B 7.5E
FBCD<58>	6.3B 7.5E
FBCD<59>	6.3B 7.5E
FBCD<60>	6.3B 7.5E
FBCD<61>	6.3B 7.5E
FBCD<62>	6.3B 7.5E
FBCD<63>	6.3B 7.5E
FBCDQM<0>	6.3B 7.4B 7.4C
FBCDQM<7..0>	6.3A> 7.1G<> 7.4B<>
FBCDQM<1>	6.3B 7.4B 7.4D
FBCDQM<2>	6.3B 7.4B 7.4E
FBCDQM<3>	6.3B 7.4B 7.4E
FBCDQM<4>	6.3B 7.4B 7.5C
FBCDQM<5>	6.3B 7.4B 7.5D
FBCDQM<6>	6.3B 7.4B 7.5E
FBCDQM<7>	6.3B 7.4B 7.5E
FBCDQS_RN<0>	6.4B 7.1G<> 7.4B 7.4C
FBCDQS_RN<7..0>	6.4A<> 7.4B<>
FBCDQS_RN<1>	6.4B 7.1G<> 7.4B 7.4D
FBCDQS_RN<2>	6.4B 7.1G<> 7.4B 7.4E
FBCDQS_RN<3>	6.4B 7.1G<> 7.4B 7.4E
FBCDQS_RN<4>	6.4B 7.1G<> 7.4B 7.5C
FBCDQS_RN<5>	6.4B 7.1G<> 7.4B 7.5D
FBCDQS_RN<6>	6.4B 7.2G<> 7.5B 7.5E
FBCDQS_RN<7>	6.4B 7.2G<> 7.5B 7.5E
FBCDQS_WP<0>	6.3B 7.1G<> 7.4C 7.5B
FBCDQS_WP<7..0>	6.3A<> 7.5B<>
FBCDQS_WP<1>	6.3B 7.1G<> 7.4D 7.5B
FBCDQS_WP<2>	6.3B 7.1G<> 7.4E 7.5B
FBCDQS_WP<3>	6.3B 7.1G<> 7.4E 7.5B
FBCDQS_WP<4>	6.3B 7.1G<> 7.5B 7.5C
FBCDQS_WP<5>	6.3B 7.2G<> 7.5B 7.5D
FBCDQS_WP<6>	6.4B 7.2G<> 7.5B 7.5E
FBCDQS_WP<7>	6.4B 7.2G<> 7.5B 7.5E
FBC_CLK0	6.4D> 7.1G< 7.2A< 7.2D
FBC_CLK0*	6.4D> 7.1G< 7.2A< 7.2D
FBC_CLK1	6.4D> 7.1G< 7.2D< 7.2D
FBC_CLK1*	6.4D> 7.1G< 7.2D< 7.2D
FBC_CMD<0>	6.3C 7.1B 7.1D
FBC_CMD<26..0>	6.3D> 7.1A< 7.1C 7.1D 7.1G<
FBC_CMD<1>	6.3C 7.1B 7.1E
FBC_CMD<2>	6.3C 7.1B 7.1D
FBC_CMD<3>	6.3C 7.1B 7.1E
FBC_CMD<4>	6.3C 7.1D 7.1E
FBC_CMD<5>	6.3C 7.1E 7.2D
FBC_CMD<6>	6.3C 7.1E 7.2D
FBC_CMD<8>	6.3C 7.1B 7.1E
FBC_CMD<9>	6.3C 7.1B 7.1E
FBC_CMD<10>	6.3C 7.2B 7.2E
FBC_CMD<11>	6.3C 6.3G 7.2B 7.2E
FBC_CMD<12>	6.3C 7.2B 7.2E
FBC_CMD<13>	6.3C 7.1D 7.1E
FBC_CMD<14>	6.3C 7.1B 7.1E
FBC_CMD<15>	6.3C 7.1B 7.1E
FBC_CMD<16>	6.3C 7.1B 7.1E
FBC_CMD<17>	6.3C 7.1B 7.1E
FBC_CMD<18>	6.3C 7.2B 7.2E
FBC_CMD<19>	6.3C 7.1B 7.1E
FBC_CMD<20>	6.3C 7.1B 7.1E
FBC_CMD<21>	6.3C 7.1B 7.1E
FBC_CMD<22>	6.3C 7.1B 7.1D
FBC_CMD<23>	6.3D 7.1B 7.1E
FBC_CMD<24>	6.3D 7.1B 7.1D
FBC_CMD<25>	6.3D 7.1B 7.1E
FBC_PLLAVDD	6.1F< 6.4C
FBC_PLLVDD	6.1F< 6.4C
FBC_REFCLK	6.1F< 6.4C
FBC_REFCLK*	6.1F< 6.4C
FBC_VREF_ADDR0	7.2G<> 7.3C
FBC_VREF_ADDR1	7.2G<> 7.3F
FBC_VREF_DATA0	7.2G<> 7.3C
FBC_VREF_DATA1	7.2G<> 7.3F
GND_SENSE	2.3E 2.5G<>
GPIO5_VSELO	17.1D> 22.1F<
GPIO6_VSEL1	17.1D> 22.2F<
GPIO10_480P	15.4A< 17.2D>
GPU_PEX_REFCLK	2.1G<> 2.2C< 21.3G>
GPU_PEX_REFCLK*	2.1G<> 2.2C< 21.3G>
I2CA_SCL	9.2C< 9.3D>
I2CA_SCL_C	9.2F> 9.2F> 11.3G<
I2CA_SDA	9.2C< 9.3D>
I2CA_SDA_C	9.1F> 9.1F> 11.3G<
I2CB_SCL	10.2C<
I2CB_SCL_C	10.2F> 12.3G<
I2CB_SDA	10.2C<
I2CB_SDA_C	10.1F> 12.3G<
I2CC_SCL	14.3A< 15.1H< 16.2E<> 17.1D< 17.3B
I2CC_SDA	14.3A<> 15.1H<> 16.2E<> 17.1D<> 17.3B
IFPABRSET	11.2B 11.4G<>
IFPAB_IOVDD	11.3B 11.4G<>
IFPAB_PLLVDD	11.2B 11.4G<>
IFPCD_IOVDD	12.3B 12.4G<>
IFPCD_PLLVDD	12.2B 12.4G<>
IFPCD_RSET	12.2C 12.4G<>
MDIN_CIN_C	15.2A<> 15.2F
MDIN_CIN_CLAMP	15.2A<> 15.2G
MDIN_COUT_C	15.1A<> 15.2E
MDIN_PBOUT_C	15.1A<> 15.1E
MDIN_YIN_C	15.1A<> 15.2E
MDIN_YIN_CLAMP	15.1A<> 15.2D
MDIN_YOUT_C	15.1A<> 15.2F
MINIDIN_CIN	14.2A< 15.2A<> 15.2H>
MINIDIN_Y_CVBSIN	14.1A< 15.1A<> 15.2C>
MIOA2V5_VREF	19.1G<> 19.2E
MIOAD<0>	13.4D 13.4G 18.1B 18.5B
MIOAD<11..0>	13.1G<> 13.3D 13.3G 18.1A<>
MIOAD<1>	13.4D 13.4G 18.1B 18.2B
MIOAD<2>	13.4D 13.4G 18.1B 18.4B
MIOAD<3>	13.4D 13.4G 18.1B
MIOAD<4>	13.4D 13.4G 18.1B
MIOAD<5>	13.4D 13.4G 18.1B
MIOAD<6>	13.4D 13.4G 18.1B 18.5B
MIOAD<7>	13.4D 13.4G 18.1B
MIOAD<8>	13.4D 13.4G 18.1B 18.5B
MIOAD<9>	13.4D 13.4G 18.1B 18.5B
MIOAD<10>	13.4D 13.4G 18.1B
MIOAD<11>	13.4D 13.4G 18.2B
MIOA_CLKOUT	13.1G<> 13.5D
MIOA_CLKOUT*	13.1G<>
MIOA_HSYNC	13.5H> 18.3A<>
MIOA_VREF	13.1G<> 13.4C
MIOA_VSYNC	13.4H<>
MIOBD<0>	13.1D 14.3D 18.2B 18.2B
MIOBD<7..0>	13.1G<> 14.3A<>
MIOBD<11..0>	13.1E<> 18.2A<>
MIOBD<1>	13.2D 14.3D 18.2B 18.2B
MIOBD<2>	13.2D 14.3D 18.2B
MIOBD<3>	13.2D 14.3D 18.2B 18.3B
MIOBD<4>	13.2D 14.3D 18.2B 18.3B
MIOBD<5>	13.2D 14.3D 18.2B 18.3B
MIOBD<6>	13.2D 14.3D 18.2B
MIOBD<7>	13.2D 14.3D 18.2B
MIOBD<8>	13.2D 18.2B 18.2B
MIOBD<9>	13.2D 18.2B 18.3B
MIOBD<10>	13.2D 18.2B 18.4B
MIOBD<11..10>	13.1G<>
MIOBD<11>	13.2D 18.2B 18.3B
MIOB_VREF	13.1G<> 13.2C
NVVDD_SENSE	2.3F> 2.5G<> 22.2G<
PEX_PLL_VDD	2.4E 2.5G<>
PEX_REFCLK	2.1G<> 2.2C> 21.3B<
PEX_REFCLK*	2.1G<> 2.2C> 21.3B<
PEX_RX0	2.2B 2.4G<>
PEX_RX0*	2.2B 2.4G<>
PEX_RX1	2.2B 2.4G<>
PEX_RX1*	2.2B 2.4G<>
PEX_RX2	2.2B 2.4G<>
PEX_RX2*	2.3B 2.4G<>
PEX_RX3	2.3B 2.4G<>
PEX_RX3*	2.3B 2.4G<>
PEX_RX4	2.3B 2.4G<>
PEX_RX4*	2.3B 2.4G<>
PEX_RX5	2.3B 2.4G<>
PEX_RX5*	2.3B 2.4G<>
PEX_RX6	2.3B 2.4G<>
PEX_RX6*	2.3B 2.4G<>
PEX_RX7	2.3B 2.4G<>
PEX_RX7*	2.4B 2.4G<>
PEX_RX8	2.4B 2.4G<>
PEX_RX8*	2.4B 2.4G<>
PEX_RX9	2.4B 2.4G<>
PEX_RX9*	2.4B 2.4G<>
PEX_RX10	2.4B 2.4G<>
PEX_RX10*	2.4B 2.4G<>
PEX_RX11	2.4B 2.4G<>
PEX_RX11*	2.4B 2.5G<>
PEX_RX12	2.4B 2.5G<>
PEX_RX12*	2.5B 2.5G<>
PEX_RX13	2.5B 2.5G<>
PEX_RX13*	2.5B 2.5G<>
PEX_RX14	2.5B 2.5G<>
PEX_RX14*	2.5B 2.5G<>
PEX_RX15	2.5B 2.5G<>
PEX_RX15*	2.5B 2.5G<>
PEX_TX0	2.1G<> 2.2C
PEX_TX0*	2.1G<> 2.2C
PEX_TX1	2.1G<> 2.2C
PEX_TX1*	2.2C 2.2G<>
PEX_TX2	2.2C 2.2G<>
PEX_TX2*	2.2C 2.2G<>
PEX_TX3	2.2G<> 2.3C
PEX_TX3*	2.2G<> 2.3C
PEX_TX4	2.2G<> 2.3C
PEX_TX4*	2.2G<> 2.3C
PEX_TX5	2.2G<> 2.3C
PEX_TX5*	2.2G<> 2.3C
PEX_TX6	2.2G<> 2.3C
PEX_TX6*	2.2G<> 2.3C
PEX_TX7	2.2G<> 2.3C
PEX_TX7*	2.2G<> 2.3C
PEX_TX8	2.2G<> 2.4C
PEX_TX8*	2.2G<> 2.4C
PEX_TX9	2.2G<> 2.4C
PEX_TX9*	2.2G<> 2.4C
PEX_TX10	2.2G<> 2.4C
PEX_TX10*	2.2G<> 2.4C
PEX_TX11	2.2G<> 2.4C
PEX_TX11*	2.2G<> 2.4C
PEX_TX12	2.2G<> 2.4C
PEX_TX12*	2.2G<> 2.4C
PEX_TX13	2.2G<> 2.5C
PEX_TX13*	2.2G<> 2.5C
PEX_TX14	2.2G<> 2.5C
PEX_TX14*	2.2G<> 2.5C
PEX_TX15	2.2G<> 2.5C
PEX_TX15*	2.2G<> 2.5C
PEX_TXX0	2.2B 2.3G<>
PEX_TXX0*	2.2B 2.3G<>
PEX_TXX1	2.2B 2.3G<>
PEX_TXX1*	2.2B 2.3G<>
PEX_TXX2	2.2B 2.3G<>
PEX_TXX2*	2.2B 2.3G<>
PEX_TXX3	2.3B 2.3G<>
PEX_TXX3*	2.3B 2.3G<>
PEX_TXX4	2.3B 2.3C<>
PEX_TXX4*	2.3B 2.3C<>
PEX_TXX5	2.3B 2.3G<>
PEX_TXX5*	2.3B 2.3G<>
PEX_TXX6	2.3B 2.3G<>
PEX_TXX6*	2.3B 2.3G<>
PEX_TXX7	2.3B 2.3G<>
PEX_TXX7*	2.3B 2.3G<>
PEX_TXX8	2.3G<> 2.4B
PEX_TXX8*	2.3G<> 2.4B
PEX_TXX9	2.3G<> 2.4B
PEX_TXX9*	2.3G<> 2.4B
PEX_TXX10	2.3G<> 2.4B
PEX_TXX10*	2.3G<> 2.4B
PEX_TXX11	2.3G<> 2.4B
PEX_TXX11*	2.3G<> 2.4B
PEX_TXX12	2.3G<> 2.4B
PEX_TXX12*	2.3G<> 2.4B
PEX_TXX13	2.3G<> 2.5B
PEX_TXX13*	2.3G<> 2.5B
PEX_TXX14	2.3G<> 2.5B
PEX_TXX14*	2.4G<> 2.5B
PEX_TXX15	2.4G<> 2.5B
PEX_TXX15*	2.4G<> 2.5B
PLLVDD	16.4B 16.5G<
RESET_BUF*	14.3A<> 17.4D>
ROMCS*	17.4D> 17.4F<>
ROM_SCLK	17.4D> 17.4F<>
ROM_SI	17.4D> 17.4F<>
ROM_SO	17.4D> 17.4F<>
R_CLK_OUT	21.1G<> 21.3E
R_CLK_OUT*	21.1G<> 21.3E
SEC_CHROMA	16.2C 16.2G 16.5G<>
SEC_CVBS	16.2C 16.2G 16.5G<>
SEC_CVBS1	14.3A< 16.3A> 16.4G<>
SEC_CVBS1A	16.3B 16.4G<>
SEC_LUMA	16.1C 16.2G 16.5G<>
STEREO	15.4F< 17.5D>
SWAPRDY_A	13.4E<> 17.5E<>
THERMDA	17.1B 17.3A 17.5G<>
THERMDC	17.1B 17.3A 17.5G<>
TMDSABPLL_ADJ	19.1G<> 19.2C
TMDS_IOBACK	11.4G<> 11.5B
TUNER_CVBS	16.2G 16.3C 16.5G<>
TUNER_IRQ	16.2E> 17.1D<
VDDA	14.1F 14.1G<>
VDDE	14.1G<> 14.4G
VDDX	14.1G<> 14.3G
VIDINT_CIN	14.2A< 16.2A> 16.4G<>
VIDINT_CVBSIN	14.2A< 16.2A> 16.4G<>
VIDINT_CVBS_F	16.2B 16.4G<>
VIDINT_C_F	16.2B 16.4G<>
VIDINT_Y_CVBSIN	14.2A< 16.1A> 16.4G<>
VIDINT_Y_F	16.1B 16.4G<>
VID_PLLVDD	16.4B 16.5G<
VIPHCLK	13.2E<> 15.3A<>
VIPPCLK	13.1G<> 13.2E<> 14.4A> 15.3A<>
XTALIN	16.5C 16.5G<
XTALOUT	16.5D 16.5G<

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	SIGNAL CROSS REFERENCE 1

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10216-0001-300		
ID	p216	PAGE	23 OF 25
NAME	bnichols	DATE	9-SEP-2004

*** Part Cross-Reference for the entire design ***

BKT1	BRACKET	18.2F
C1	C	8.3A
C2	C	8.3B
C3	C_POL	22.1C
C4	C_POL	22.1D
C5	C	3.1D
C6	C	3.1D
C7	C_POL	22.1D
C8	C_POL	22.1E
C9	C	16.2G
C10	C	22.1B
C11	C	15.4G
C12	C	16.2G
C13	C	16.2G
C14	C	16.2G
C15	C	22.2F
C16	C	15.1F
C17	C_POL	20.3H
C18	C	16.1D
C19	C	16.1D
C20	C	15.2F
C21	C	15.3F
C22	C_POL	20.1E
C23	C	15.1E
C24	C_POL	22.3H
C25	C_POL	22.3H
C26	C_POL	22.2A
C27	C_POL	22.3H
C28	C_POL	22.3H
C29	C	14.2D
C30	C	14.2C
C31	C	20.2B
C32	C	20.2A
C33	C	20.1D
C34	C	22.4E
C35	C	12.2G
C36	C	17.1E
C37	C	10.5E
C38	C	10.5F
C39	C_POL	20.2A
C40	C	10.5E
C41	C	22.3C
C42	C	10.4E
C43	C	17.3B
C44	C	10.4F
C45	C	10.4E
C46	C_POL	22.5H
C47	C_POL	22.5H
C48	C	5.4C
C49	C	10.4E
C50	C	3.1E
C51	C	10.4F
C52	C	17.4H
C53	C	10.4E
C54	C	13.5C
C55	C	20.2B
C56	C	20.2B
C57	C	20.2A
C58	C	19.4A
C59	C_POL	22.5G
C60	C_POL	22.5G
C61	C	20.4B
C62	C	16.5C
C63	C	19.2B
C64	C	16.5D
C65	C	13.2C
C66	C_POL	22.3A
C67	C	11.1D
C68	C	3.1D
C69	C	11.1E
C70	C	8.3B
C71	C	11.1E
C72	C	11.2G
C73	C	9.5E
C74	C	9.5E
C75	C	9.5F
C76	C	9.4E
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C78	C	17.1G
C79	C_POL	22.3A
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C81	C	21.2C
C82	C	9.4F
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C85	C	17.1A
C86	C	9.4E
C87	C	9.4F
C88	C	21.3F
C89	C	17.1H
C90	C	17.1H
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C93	C	2.1B
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C95	C	2.1A
C96	C	2.1F
C97	C	2.1C
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C100	C	15.3C
C101	C	15.3D
C102	C	15.4D
C103	C	19.2D
C104	C	19.2D
C105	C_POL	22.4A
C106	C	15.3B
C107	C	19.1E
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C502	C	20.3G
C503	C	20.3G
C504	C	20.3G
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C507	C	15.2D
C508	C	15.1D
C509	C	15.2E
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C511	C	7.3G
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C513	C	7.3D
C514	C	7.3D
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C516	C	7.3D
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C518	C	7.3G
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C520	C	8.3E
C521	C	8.3A
C522	C	8.3A
C523	C	8.3D
C524	C	8.3E
C525	C	8.3A
C526	C	8.3B
C527	C	5.4B
C528	C	5.3F
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C532	C	16.1C
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C535	C	15.2E
C536	C	5.4E
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C539	C	8.3A
C540	C	8.3B
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C548	C	16.1C
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C557	C	15.2F
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C563	C	8.3A
C564	C	16.2B
C565	C	16.2B
C566	C	16.1B
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C568	C	8.3E
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C570	C	8.2D
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C572	C	5.2F
C573	C	20.2E
C574	C	15.2D
C575	C	15.2D
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C578	C	5.4E
C579	C	22.3F
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C584	C	15.2F
C585	C	20.1F
C586	C	22.3D
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C589	C	20.3G
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C605	C	14.2B
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C616	C	14.2E
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C633	C	14.4G
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C636	C	22.3F
C637	C	22.5E
C638	C	22.5G
C639	C	22.1G
C640	C	22.3F
C641	C	5.4B
C642	C	5.3C
C643	C	14.4F
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C646	C	14.4F
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C649	C	10.2F
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C653	C	6.4F
C654	C	3.4F
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C658	C	5.3E
C659	C	2.2G
C660	C	3.4A
C661	C	14.4F
C662	C	3.4F
C663	C	22.4C
C664	C	22.4D
C665	C	22.4D
C666	C	22.4D
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C668	C	5.3F
C669	C	6.4E
C670	C	5.2E
C671	C	10.3F
C672	C	3.4E
C673	C	17.3C
C674	C	3.4E
C675	C	2.2E
C676	C	8.1D
C677	C	6.5E
C678	C	5.2C
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C681	C	5.3B
C682	C	5.3C
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C689	C	3.4E
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C692	C	3.4E
C693	C	14.4E
C694	C	13.4A
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C697	C	3.2E
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C703	C	14.4G
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C705	C	3.2D
C706	C	5.4C
C707	C	3.2E
C708	C	3.1D
C709	C	17.1D
C710	C	3.4E
C711	C	13.4B
C712	C	5.4B
C713	C	6.4E
C714	C	14.4F
C715	C	5.2F
C716	C	5.3C
C717	C	5.4C
C718	C	5.2B
C719	C	5.3C
C720	C	14.4F
C721	C	2.3F
C722	C	3.2E
C723	C	19.4C
C724	C	8.3D
C725	C	5.2C
C726	C	5.4F
C727	C	2.2F
C728	C	8.3D
C729	C	8.2D
C730	C	3.1E
C731	C	8.3E
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C734	C	2.3G
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C738	C	2.3F
C739	C	10.3F
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C744	C	2.3F
C745	C	2.4F
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C791	C	19.2C
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C795	C	12.2B
C796	C	2.3F
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C798	C	2.2F
C799	C	2.2F
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C801	C	2.2F
C802	C	12.2B
C803	C	4.3G
C804	C	2.2E
C805	C	9.3A
C806	C	3.1E
C807	C	13.1A
C808	C	19.2A
C809	C	13.1A
C810	C	11.2A
C811	C	11.2B
C812	C	2.5G
C814	C	11.2B
C815	C	9.4G
C816	C	20.4B
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C818	C	4.3G
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C822	C	8.3D
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C824	C	3.1D
C825	C	2.4F
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C828	C	2.4F
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C832	C	5.2B
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C843	C	2.4F
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C847	C	2.1F
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C849	C	2.1E
C850	C	2.1F
C851	C	11.3B
C852	C	10.4A
C853	C	2.4F
C854	C	2.4F
C855	C	5.3F
C856	C	3.2G
C857	C	2.1F
C858	C	5.2F
C859	C	5.2E
C860	C	5.3F
C861	C	5.4F
C862	C	11.3B
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C865	C	12.3B
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C869	C	10.4A
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C872	C	11.3B
C873	C	11.1E
C874	C	11.3B
C875	C	5.4F
C876	C	5.4F
C877	C	5.4F
C878	C	5.2F
C879	C	5.3F
C880	C	9.2F
C881	C	12.1E
C882	C	5.3F
C883	C	2.1F
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C887	C	5.3B
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C892	C	9.3E
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C894	C	2.1G
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C898	C	4.3G
C899	C	8.3D
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C901	C	11.1E
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C903	C	9.3F
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C905	C	22.3B
C906	C	12.1E
C907	C	4.3G
C908	C	2.1G
C909	C	11.5F
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C911	C	21.2C
C912	C	10.4G
C913	C	21.3C
C914	C	9.3F
C915	C	2.1B
C916	C	2.1A
C917	C	2.5C
C918	C	2.5C
C919	C	2.5C
C920	C	2.5C
C921	C	2.5C
C922	C	2.5C
C923	C	2.4C
C924	C	2.4C
C925	C	2.4C
C926	C	2.4C
C927	C	2.4C
C928	C	2.4C
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C935	C	2.3C
C936	C	2.3C
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C938	C	2.3C
C939	C	2.3C
C940	C	2.3C
C941	C	2.3C
C942	C	2.3C
C943	C	2.2C
C944	C	2.2C
C945	C	2.2C
C946	C	2.2C
C947	C	2.2C

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	PART CROSS REFERENCE 1

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10216-0001-300		
ID	p216	PAGE	24 OF 25
NAME	bnichols	DATE	9-SEP-2004

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C948  C        2.2C
C949  C        2.1A
C950  C        2.1B
C951  C_POL    19.2F
CN1   CON_MIO_26 13.3F
CN2   CON_PCI_EXPRESS 2.1A
D1    D_SCHOTTKY 22.2B
D2    D_ZENER   20.5F
D3    D_3PIN_AC 15.1G
D4    D_SCHOTTKY 20.4G
D5    D_SCHOTTKY 22.3F
D6    D_3PIN_AC 15.2G
D7    D_3PIN_CC 22.4C
D8    D_3PIN_CC 22.4C
D9    D_3PIN_AC 10.5E
D10   D_3PIN_AC 10.4E
D11   D_3PIN_AC 10.4E
D12   D         20.4C
D13   D_3PIN_AC 9.5D
D14   D_3PIN_AC 9.4D
D15   D_SCHOTTKY 17.1G
D16   D_3PIN_AC 9.4D
D501  D_3PIN_AC 15.2D
D502  D_3PIN_AC 15.2D
D503  D_3PIN_AC 16.2B
D504  D_3PIN_AC 16.2B
D505  D_3PIN_AC 16.1B
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D521  D_3PIN_AC 9.3E
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F501  F_POLYSW  19.1A
J1    HDR_1X12  16.2H
J2    HDR_1X4   16.2D
J3    CON_MINIDIN_1D 15.2E
J4    HDR_2X3   22.1B
J5    CON_DVI_I 12.2H
J6    CON_DSUB15HD 10.4G
J7    CON_DVI_I 11.2H
J8    CON_DSUB15HD 9.4G
J9    HDR_1X2   17.1H
J10   HDR_2X4   17.1A
L1    L         22.1A
L2    L         22.1D
L3    L         20.2G
L4    L         22.2F
L5    L         20.1E
L6    L         22.4F
L7    L         10.5E
L8    L         10.5E
L9    L         10.4E
L10   L         10.4E
L11   L         10.4E
L12   L         10.4E
L13   L         9.5E
L14   L         9.5E
L15   L         9.4E
L16   L         9.4E
L17   L         9.4E
L18   L         9.4E
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L502  L         15.1D
L503  L         15.2D
L504  L         15.2F
L505  L         16.2C
L506  L         16.2C
L507  L         16.1C
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LB1   L         16.2F
LB2   L         16.2F
LB3   L         16.2F
LB4   L         15.1F
LB5   L         15.1F
LB6   L         15.3E
LB7   L         20.4C
LB8   L         19.1B
LB9   L         2.1F
LB501 L         14.3H
LB502 L         14.1G
LB503 L         14.4H
LB504 L         10.2E
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LB506 L         6.4F
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LB508 L         6.5F
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LB511 L         12.5F
LB512 L         16.5A
LB513 L         16.4A
LB514 L         19.4B
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LB515 L         15.4A
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LB517 L         19.1C
LB518 L         19.2A
LB519 L         12.2B
LB520 L         9.3A
LB521 L         13.1A
LB522 L         11.2A
LB524 L         2.4G
LB525 L         12.3B
LB526 L         10.4A
LB527 L         9.2E
LB528 L         11.3A
LB529 L         9.2E
LB530 L         2.1F
LB531 L         2.3F
LB532 L         2.3G
LB533 L         21.2C
LB534 L         11.5F
LB535 L         21.3C
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MEC2  MEC_SCREW 18.2E
MEC3  MEC_SCREW 18.3E
MEC4  MEC_SCREW 18.3E
MEC5  MEC_SCREW 18.3F
MEC6  HEATSINK  18.3G
Q1    Q_FET_P_ENH 22.2B
Q2    Q_NPN     20.4E
Q3    Q_FET_N_ENH 20.3D
Q4    Q_FET_N_ENH 22.3F
Q5    Q_FET_N_ENH 22.3E
Q6    Q_FET_N_ENH 20.5E
Q7    Q_FET_N_ENH 22.2E
Q8    Q_FET_N_ENH 20.2E
Q9    Q_FET_N_ENH 22.4E
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Q12   Q_FET_N_ENH 22.5B
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Q14   Q_FET_N_ENH 22.3B
Q15   Q_FET_N_ENH 17.1F
Q16   Q_FET_N_ENH 17.1G
Q17   Q_FET_N_ENH 22.2F
Q18   Q_FET_N_ENH 17.2D
Q19   Q_FET_N_ENH 15.3B
Q20   Q_NPN     15.3C
Q21   Q_NPN     15.4C
Q22   Q_FET_N_ENH 15.3A
Q23   Q_PNP     15.3B
Q24   Q_FET_N_ENH 15.4A
Q501  Q_FET_N_ENH 22.1A
Q502  Q_FET_N_ENH 22.2A
Q503  Q_NPN     20.4F
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Q505  Q_FET_N_ENH 22.1G
Q506  Q_FET_N_ENH 22.1G
Q507  Q_FET_N_ENH 17.2F
Q508  Q_FET_N_ENH 19.1E
Q509  Q_FET_N_ENH 20.4B
Q510  Q_NPN     11.5A
Q511  Q_NPN     20.4A
Q512  Q_NPN     20.4A
Q513  Q_FET_N_ENH 11.5B
R1    R         7.2B
R2    R         7.2E
R3    R         15.4F
R4    R         7.2D
R5    R         7.2D
R6    R         7.2D
R7    R         7.2D
R8    R         15.4F
R9    R         18.5B
R10   R         18.5C
R11   R         18.5B
R12   R         18.5C
R13   R         18.3C
R14   R         18.3B
R15   R         18.2B
R16   R         18.2C
R17   R         18.5C
R18   R         18.5B
R19   R         18.5B
R20   R         18.5C
R21   R         22.2B
R22   R         20.5F
R23   R         15.2E
R24   R         15.4H
R25   R         15.1G
R26   R         20.4F
R27   R         17.1D
R28   R         16.2F
R29   R         16.2F
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R31   R         17.1D
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R33   R         15.3E
R34   R         20.4D
R35   R         20.5D
R36   R         22.5F
R37   R         22.3G
R38   R         22.4B
R39   R         22.4C
R40   R         22.5B
R41   R         22.4B
R42   R         22.4F
R43   R         6.4E
R44   R         6.4E
R45   R         6.4E
R46   R         6.4E
R47   R         17.2D
R48   R         17.1C
```

```
R49   R         10.5D
R50   R         10.5D
R51   R         17.1C
R52   R         17.2C
R53   R         22.3B
R54   R         22.3B
R55   R         18.4B
R56   R         18.4C
R57   R         18.3C
R58   R         18.3B
R59   R         10.4D
R60   R         10.4D
R61   R         4.2B
R62   R         13.4B
R63   R         18.3B
R64   R         18.3C
R65   R         18.3C
R66   R         18.3B
R67   R         4.2D
R68   R         4.2D
R69   R         13.4B
R70   R         10.4D
R71   R         10.4D
R72   R         13.4B
R73   R         13.5B
R74   R         17.4G
R75   R         20.5C
R76   R         20.4C
R77   R         16.4D
R78   R         16.5C
R79   R         18.4C
R80   R         17.2C
R81   R         13.2B
R82   R         18.4B
R83   R         2.1C
R84   R         13.2B
R85   R         13.2B
R86   R         13.2B
R87   R         12.1F
R88   R         4.2E
R89   R         12.1F
R90   R         12.1F
R91   R         12.1F
R92   R         4.2D
R93   R         12.1F
R94   R         4.2D
R95   R         12.1F
R96   R         17.2G
R97   R         9.5D
R98   R         9.5D
R99   R         17.1F
R100  R         9.4D
R101  R         9.4D
R102  R         2.2C
R103  R         9.4D
R104  R         9.4D
R105  R         21.3E
R106  R         21.3D
R107  R         21.3E
R108  R         21.3C
R109  R         21.3C
R110  R         2.1C
R111  R         2.1D
R112  R         15.3B
R113  R         15.3A
R114  R         14.4C
R115  R         14.3C
R116  R         15.3A
R117  R         15.3B
R118  R         15.3B
R119  R         15.3B
R120  R         15.3C
R121  R         15.4C
R122  R         15.4A
R123  R         15.3B
R124  R         15.4B
R501  R         7.2B
R502  R         17.1D
R503  R         22.1A
R504  R         17.1F
R505  R         22.1G
R506  R         22.1G
R507  R         22.2G
R508  R         22.1G
R509  R         17.1F
R510  R         18.3B
R511  R         18.2B
R512  R         18.2C
R513  R         18.2C
R514  R         18.2B
R515  R         18.2B
R516  R         18.2C
R517  R         16.3B
R518  R         16.3B
R519  R         22.1B
R520  R         18.3C
R522  R         7.3G
R523  R         7.3G
R524  R         7.3C
R525  R         7.3C
R526  R         7.3D
R527  R         7.3D
R528  R         7.3F
R529  R         7.3F
R530  R         7.1D
R531  R         7.2D
R532  R         7.1D
R533  R         7.1D
R534  R         22.1B
R535  R         22.2A
R536  R         7.1D
```

```
R537  R         7.2D
R538  R         7.1D
R539  R         7.1D
R540  R         15.2C
R541  R         15.2C
R542  R         22.3F
R543  R         15.2C
R544  R         15.2C
R545  R         20.2D
R546  R         20.2E
R547  R         22.3E
R548  R         20.3F
R549  R         16.2A
R550  R         16.2A
R551  R         16.2B
R552  R         16.1A
R553  R         16.1B
R554  R         15.2G
R555  R         15.2G
R556  R         15.2D
R557  R         15.2C
R558  R         20.3G
R559  R         16.2B
R560  R         15.2G
R561  R         15.2G
R562  R         22.4E
R563  R         22.2E
R564  R         20.2G
R565  R         20.2C
R566  R         20.2G
R567  R         20.2F
R568  R         20.2E
R569  R         20.2C
R570  R         20.3C
R571  R         20.1D
R572  R         20.2C
R573  R         22.4D
R574  R         22.3G
R575  R         22.1C
R576  R         22.3G
R577  R         10.2D
R578  R         10.2E
R579  R         22.3G
R580  R         22.5F
R581  R         22.4F
R582  R         14.3C
R583  R         22.1C
R584  R         14.2F
R585  R         22.1G
R586  R         22.1H
R587  R         14.2F
R588  R         22.3F
R589  R         22.1H
R590  R         10.2D
R591  R         10.2E
R592  R         17.5D
R593  R         3.4D
R594  R         22.4B
R595  R         22.4G
R596  R         3.4D
R597  R         4.3D
R598  R         22.4B
R599  R         3.4D
R600  R         22.1G
R601  R         3.4D
R602  R         3.4A
R603  R         14.2E
R604  R         22.3B
R605  R         4.3D
R606  R         6.3G
R607  R         3.5A
R608  R         6.3G
R609  R         22.3C
R610  R         4.1D
R611  R         4.1D
R612  R         17.4D
R613  R         14.4B
R614  R         17.3E
R615  R         17.2C
R616  R         19.2E
R617  R         19.2E
R618  R         12.5D
R619  R         12.5E
R620  R         19.2E
R621  R         6.5D
R622  R         17.5D
R623  R         17.5C
R624  R         6.5D
R625  R         6.5D
R626  R         13.5E
R627  R         4.1D
R628  R         4.1D
R629  R         2.3E
R630  R         15.5B
R631  R         19.4B
R632  R         15.5B
R633  R         10.3E
R634  R         10.3E
R635  R         4.3C
R636  R         19.4B
R637  R         19.2C
R638  R         3.3H
R639  R         4.3C
R640  R         3.3H
R641  R         19.2C
R642  R         4.3G
R643  R         4.2B
R644  R         4.3G
R645  R         20.4B
R646  R         4.2D
R647  R         4.2D
```

```
R648  R         20.4A
R649  R         9.3E
R650  R         9.3E
R651  R         20.4A
R652  R         9.3B
R653  R         10.4B
R654  R         10.4B
R655  R         9.2D
R656  R         9.2E
R657  R         12.1F
R658  R         9.3B
R659  R         12.2C
R660  R         11.4B
R661  R         11.5B
R662  R         11.4A
R663  R         20.4A
R664  R         20.4A
R665  R         12.1F
R666  R         11.2C
R667  R         12.1F
R668  R         9.2D
R669  R         9.2E
R670  R         11.1F
R671  R         12.1F
R672  R         11.1F
R673  R         11.1F
R674  R         4.1D
R675  R         4.2D
R676  R         11.1F
R677  R         12.1F
R678  R         11.1F
R679  R         11.1F
R680  R         11.1F
R681  R         12.1F
R682  R         12.1F
R683  R         12.1F
R684  R         4.3F
R685  R         11.1F
R686  R         11.1F
R687  R         11.1F
R688  R         11.1F
R689  R         4.3F
R690  R         11.1F
R691  R         11.1F
R692  R         11.1F
R693  R         17.1A
R694  R         17.1A
R695  R         11.5D
R696  R         11.5E
R697  R         17.1A
R698  R         17.1A
R699  R         17.1A
R700  R         21.3E
R701  R         21.3E
R702  R         21.2E
R703  R         21.2E
R704  R         2.1B
TP1   TESTPOINT 20.5A
TP501 TESTPOINT 20.3H
TP502 TESTPOINT 22.3G
TP503 TESTPOINT 22.5E
TP504 TESTPOINT 22.3G
TP505 TESTPOINT 20.5A
TP506 TESTPOINT 22.5E
TP507 TESTPOINT 20.3G
TP508 TESTPOINT 20.5A
U1    U_AND_2IN 15.4G
U2    U_SHNTREG_TL431 20.4F
U3    U_MEM_SD_DDR3_X32 7.1B 7.4C 7.4D 7.4E 7.4F
U4    U_MEM_SD_DDR3_X32 7.1E 7.5C 7.5D 7.5E 7.5F
U5    U_AND_2IN 17.2D
U6    U_TEMP_AD1032 17.2B
U7    U_VREG_3PIN 20.4C
U8    U_MEM_SD_DDR3_X32 4.1B 4.4C 4.4D 4.4E 4.4F
U9    U_MEM_EE_CRYPT_8X128 17.3D
U10   U_MEM_FL_SER_128KX8 17.4G
U11   U_GPU_G3  2.1D 3.1B 6.1B 8.1G 9.3B 10.4B
                11.2C 12.2C 13.1C 13.4C 15.4C 16.4C
                17.1B 17.4B
U12   U_MEM_SD_DDR3_X32 4.1E 4.5C 4.5D 4.5E 4.5F
U13   U_CLK_PLL_9DB202 21.3D
U14   U_AND_2IN 2.1C
U15   U_OPAMP   15.3C
U16   U_OPAMP   15.4C
U501  U_SWREG_ISL6549 20.2D
U502  U_SWREG_ISL6534 22.2C
U503  U_VDEC_SAA71XX 14.1D
U504  U_SHNTREG_TL431 19.2E
U505  U_VREG_5PIN 19.4B
U506  U_VREG_5PIN 19.1C
U507  U_AND_2IN 9.3D 10.3E
Y1    XTAL_4PIN 16.5C
Y501  XTAL      14.2C
```

ASSEMBLY	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HD/VIVO
PAGE DETAIL	PART CROSS REFERENCE 2

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NV_PN	602-10216-0001-300		
ID	p216	PAGE	25 OF 25
NAME	bnichols	DATE	9-SEP-2004