

P626-A01: GT216, DDR2 MEMORY 32MX16/64MX16

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REV	VARIANT	NVFN	ASSEMBLY
B	BASE	600-10626-BASE-100	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10626-0000-100	GT216-205, 475MHz/500MHz, 1024MB 64MX16 DDR2 BGAB4 DVI-DL_VGA
2	SKU0001	600-10626-0001-100	GT216-205, 475MHz/500MHz, 1024MB 64MX16 DDR2 BGAB4 DVI-DL_HDMI
3	SKU0002	600-10626-0002-100	GT216-205, 475MHz/500MHz, 512MB 32MX16 DDR2 BGAB4 DVI-DL_VGA
4	SKU0005	600-10626-0005-100	GT216-305, 600MHz/500MHz, 1024MB 64MX16 DDR2 BGAB4 DVI-DL_VGA
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PAGE 201 Overview

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600-10626-BASE-100 B

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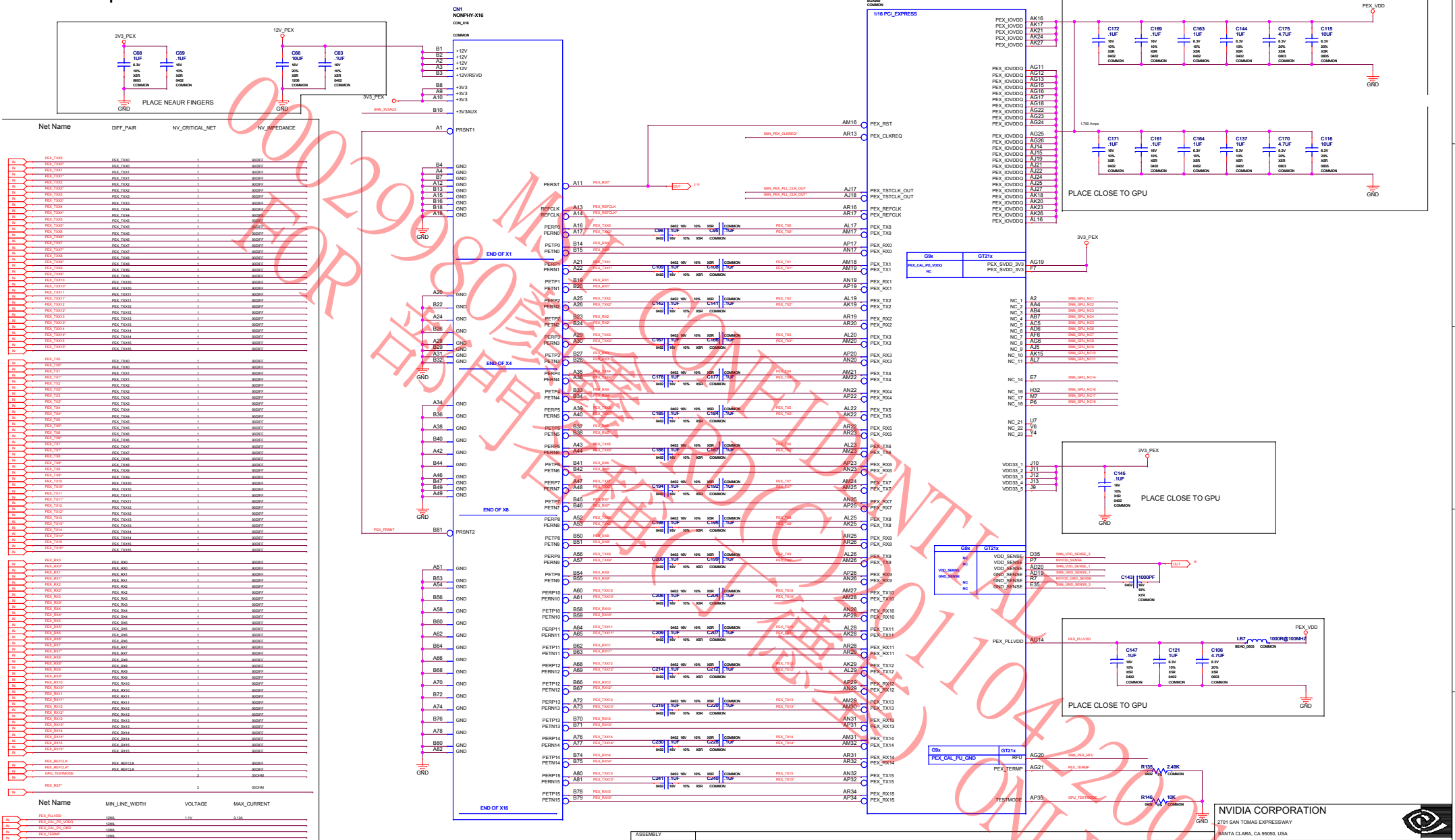
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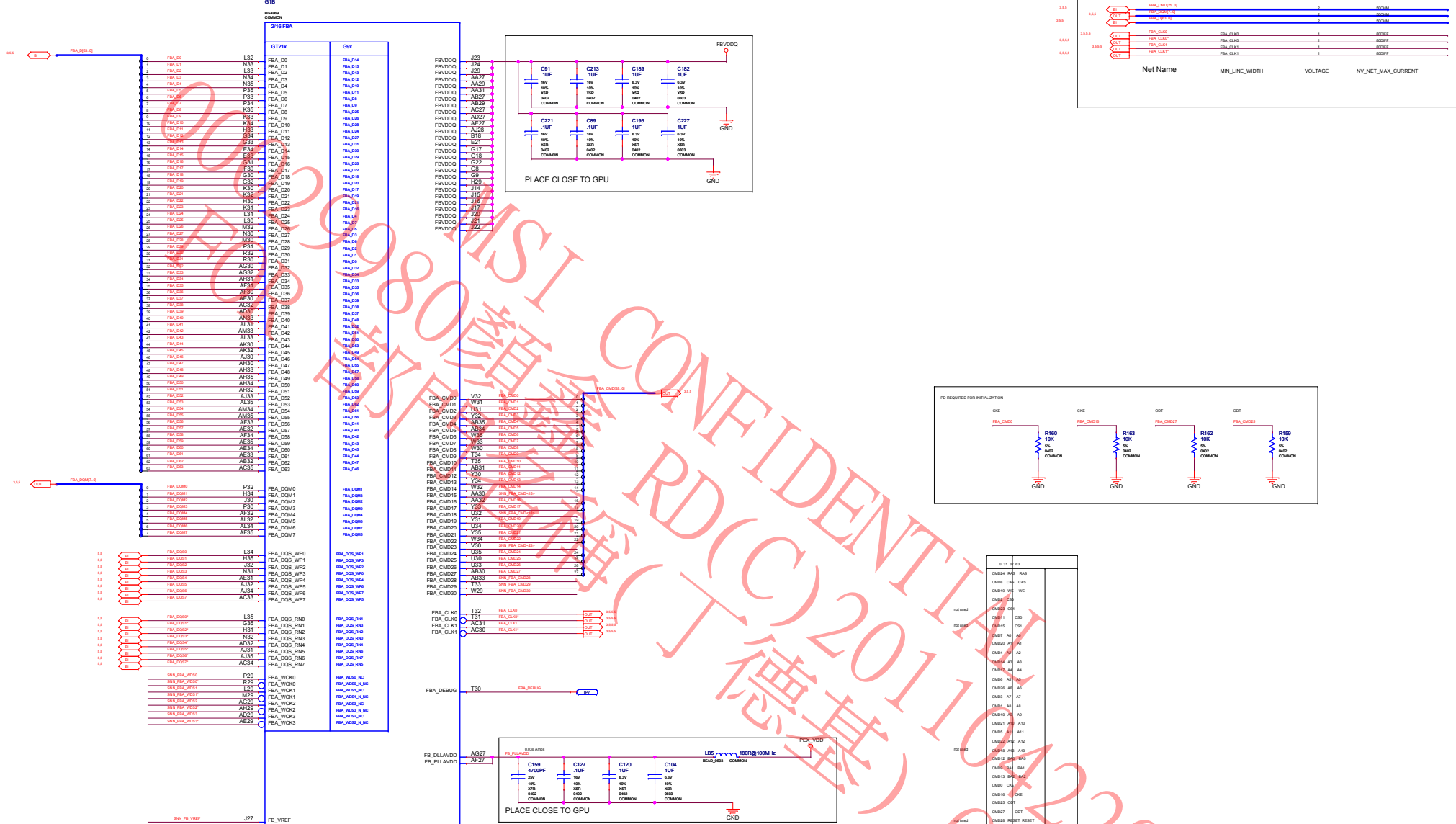
PCI Express Interface



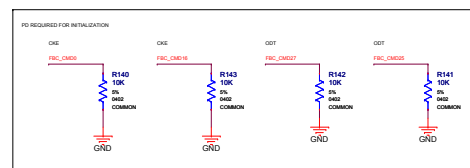
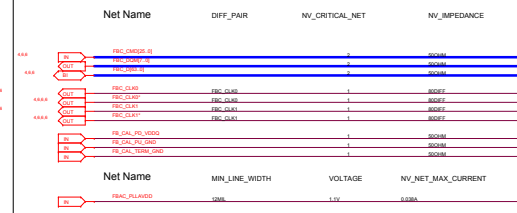
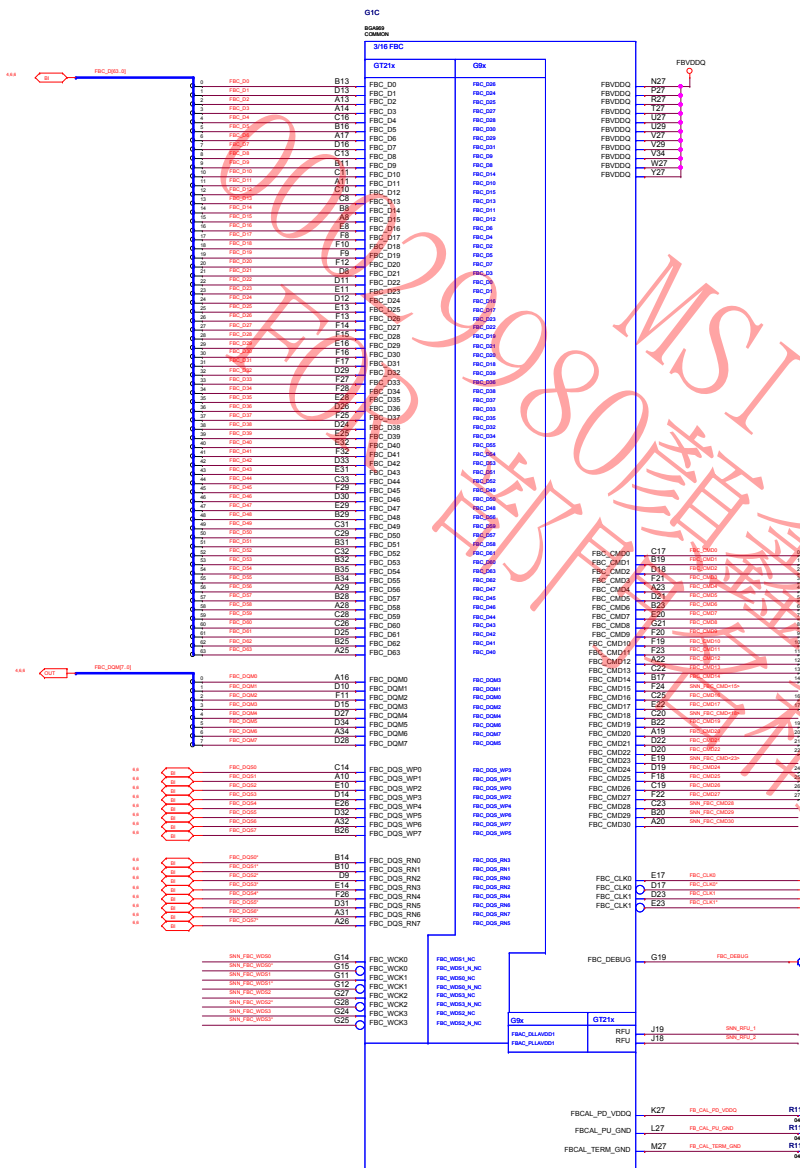
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Partition A Frame Buffer Interface



Partition C Frame Buffer Interface



	0-15	16-31
	CD00A	0000
	CD00B	0001
	CD00C	0002
	CD00D	0003
not used	CD00E	0004
	CD00F	0005
	CD00G	0006
	CD00H	0007
	CD00I	0008
	CD00J	0009
	CD00K	000A
	CD00L	000B
	CD00M	000C
	CD00N	000D
	CD00O	000E
	CD00P	000F
	CD00Q	0010
	CD00R	0011
	CD00S	0012
	CD00T	0013
	CD00U	0014
	CD00V	0015
	CD00W	0016
	CD00X	0017
	CD00Y	0018
	CD00Z	0019
	CD00A	001A
	CD00B	001B
	CD00C	001C
	CD00D	001D
	CD00E	001E
	CD00F	001F
	CD00G	0020
	CD00H	0021
	CD00I	0022
	CD00J	0023
	CD00K	0024
	CD00L	0025
	CD00M	0026
	CD00N	0027
	CD00O	0028
	CD00P	0029
	CD00Q	002A
	CD00R	002B
	CD00S	002C
	CD00T	002D
	CD00U	002E
	CD00V	002F
	CD00W	0030
	CD00X	0031
	CD00Y	0032
	CD00Z	0033
	CD00A	0034
	CD00B	0035
	CD00C	0036
	CD00D	0037
	CD00E	0038
	CD00F	0039
	CD00G	003A
	CD00H	003B
	CD00I	003C
	CD00J	003D
	CD00K	003E
	CD00L	003F
	CD00M	0040
	CD00N	0041
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	CD00P	0043
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	CD00R	0045
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	CD00V	0049
	CD00W	004A
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	CD00I	01DC

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Partition C Memories

GT21x CMD MAP

Net Name

MIN_LINE_WIDTH

DIFF_PAIR

NV_CRITICAL_NET

NV_IMPEDANCE

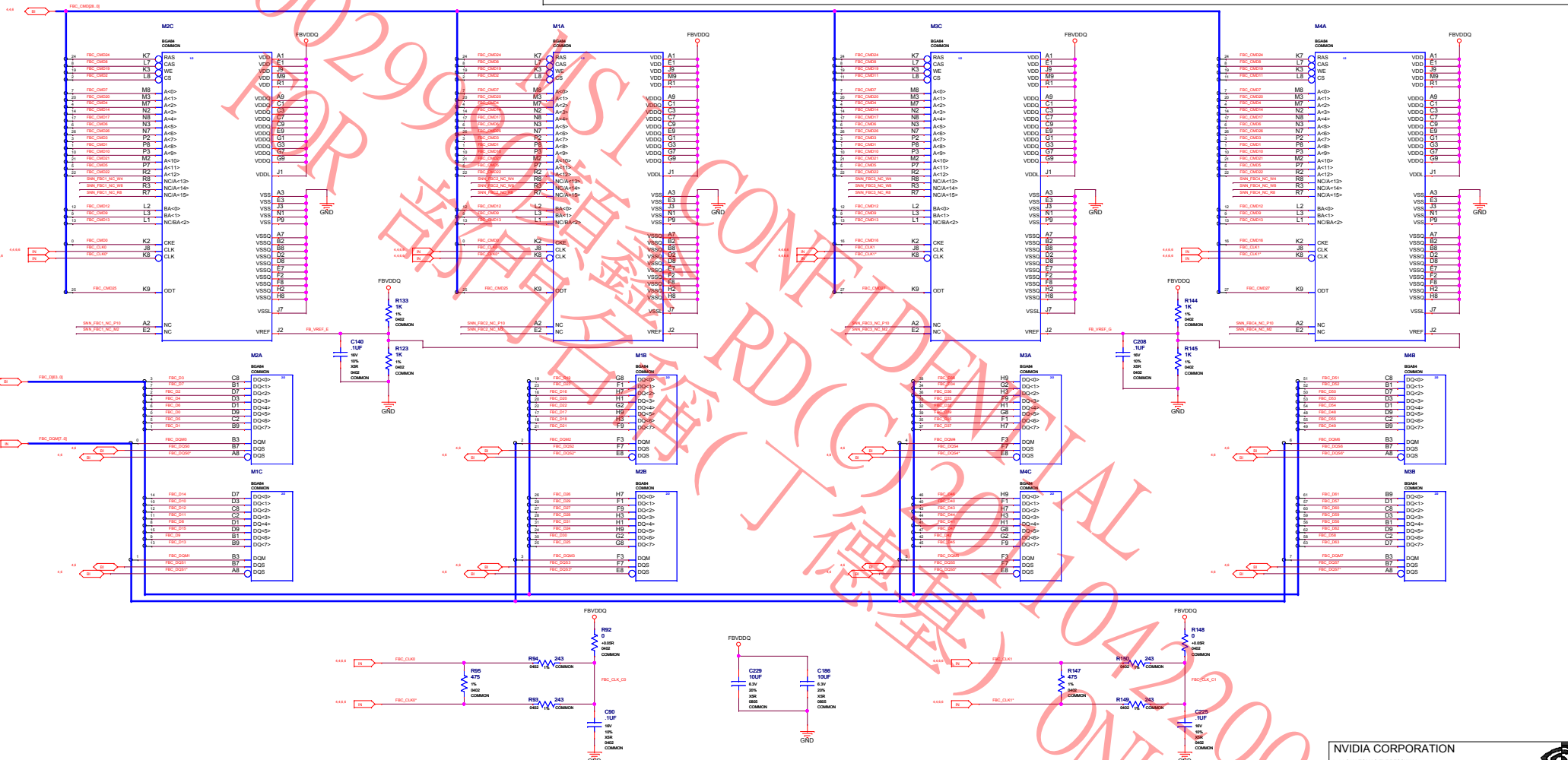
Net Name

MIN_LINE_WIDTH

DIFF_PAIR

NV_CRITICAL_NET

NV_IMPEDANCE



ASSEMBLY BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STOP ASSEMBLY NOTES AND ISOM NOT FINAL
PAGE DETAIL FBC T623KX32 DQDR3 MEMORIES; FBC CMD BUS PINS; FBC CLK TERMS

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NAME

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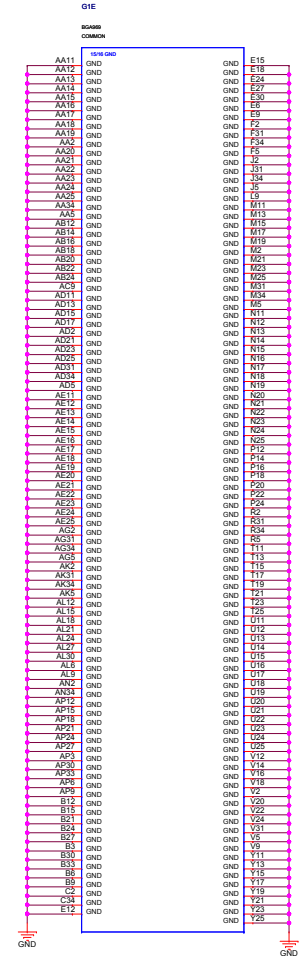
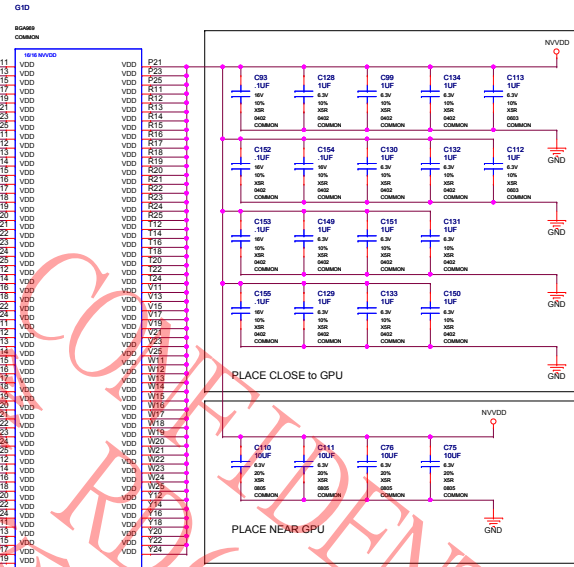
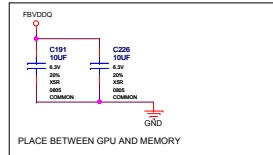
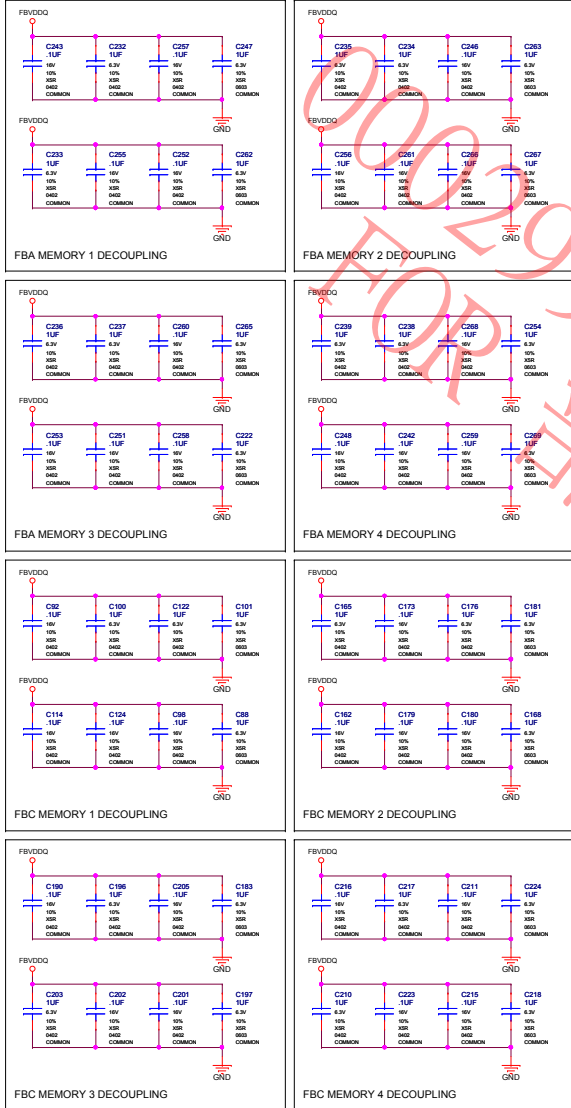
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DATE

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Decoupling Caps

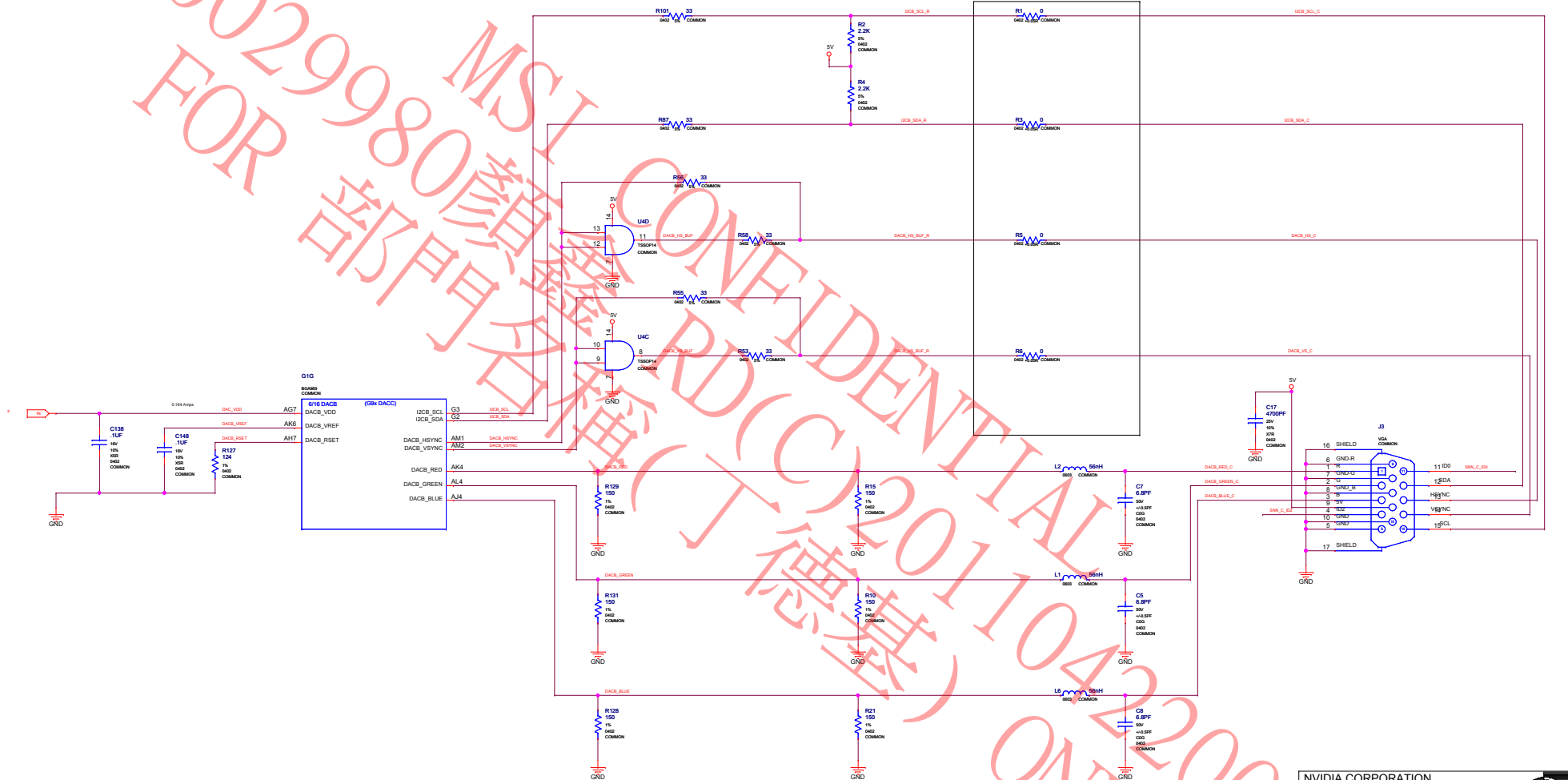


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Decoupling Caps

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2701 SAN TOMAS EXPRESSWAY	
SANTA CLARA, CA 95050, USA	
NV_PN	600-10626-BASE-100 B
ID	PAGE
NAME	DATE 23 OCT 2009

DACB, D-SUB Connector



	Net Name	NV_CRITICAL_NET	NV_IMPEDANCE
10	DACR_VEN12C	2	500OH
10	DACR_VEN12D	2	500OH
10	DACR_VEN_BUF_0	2	500OH
10	DACR_VEN_BUF_1	2	500OH
10	DACR_VEN_BUF_2	2	500OH
10	DACR_VEN_BUF_3	2	500OH
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10	DACR_VEN_44	2	500OH
10	DACR_VEN_45	2	500OH
10	DACR_VEN_46	2	500OH
10	DACR_VEN_47	2	500OH
10	DACR_VEN_48	2	500OH
10	DACR_VEN_49	2	500OH
10	DACR_VEN_50	2	500OH
10	DACR_VEN_51	2	500OH
10	DACR_VEN_52	2	500OH
10	DACR_VEN_53	2	500OH
10	DACR_VEN_54	2	500OH
10	DACR_VEN_55	2	500OH
10	DACR_VEN_56	2	500OH
10	DACR_VEN_57	2	500OH
10	DACR_VEN_58	2	500OH
10	DACR_VEN_59	2	500OH
10	DACR_VEN_60	2	500OH
10	DACR_VEN_61	2	500OH
10	DACR_VEN_62	2	500OH
10	DACR_VEN_63	2	500OH
10	DACR_VEN_64	2	500OH
10	DACR_VEN_65	2	500OH
10	DACR_VEN_66	2	500OH
10	DACR_VEN_67	2	500OH
10	DACR_VEN_68	2	500OH
10	DACR_VEN_69	2	500OH
10	DACR_VEN_70	2	500OH
10	DACR_VEN_71	2	500OH
10	DACR_VEN_72	2	500OH
10	DACR_VEN_73	2	500OH
10	DACR_VEN_74	2	500OH
10	DACR_VEN_75	2	500OH
10	DACR_VEN_76	2	500OH
10	DACR_VEN_77	2	500OH
10	DACR_VEN_78	2	500OH
10	DACR_VEN_79	2	500OH
10	DACR_VEN_80	2	500OH
10	DACR_VEN_81	2	500OH
10	DACR_VEN_82	2	500OH
10	DACR_VEN_83	2	500OH

Net Name	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
IN	0.008		
IN	0.008		
IN	0.008		
IN	0.008	3.3V	0.100A

ASSEMBLY	BASIC LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB, DB15 Connector

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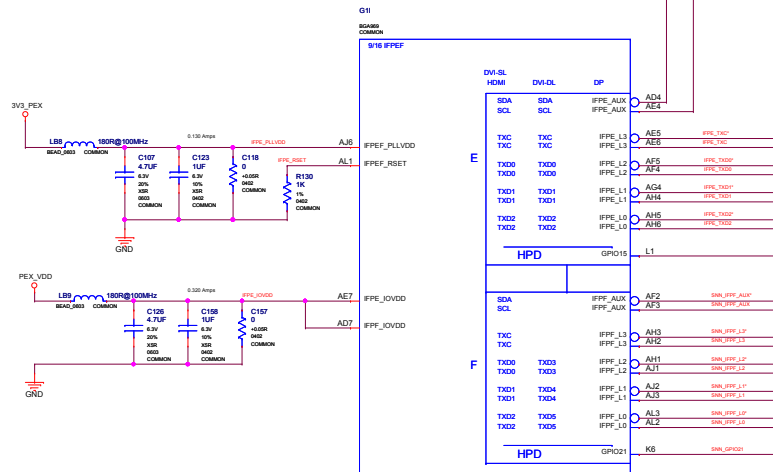
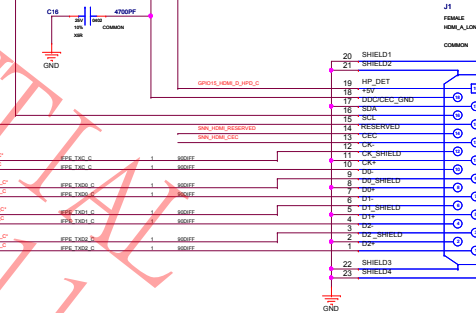
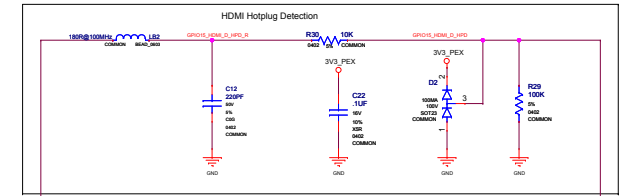
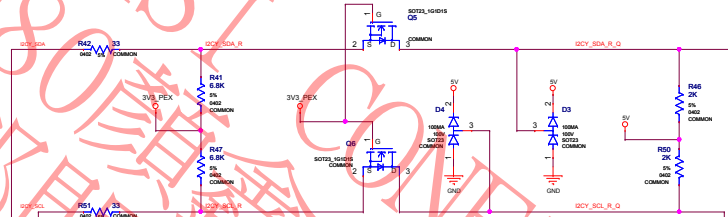
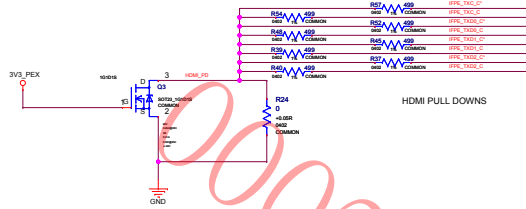
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A horizontal number line with tick marks at 0, 2, 4, 6, 8, and 10. A vertical line is drawn at the tick mark for 4. The segment of the number line from 0 to 4 is labeled with the letter 'A' below it. The segment of the number line from 4 to 10 is labeled with the letter 'B' below it.

HDMI .. Link E

Net Name	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
#REF_556T	12MIL		
#REF_7JLWDD	55MIL	1.6V	0.130A
#REF_7JXVDD	55MIL	1.1V	0.302A



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PAGE DETAIL	HDMI .. LINK E

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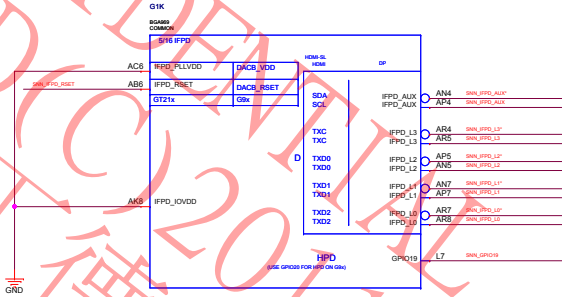
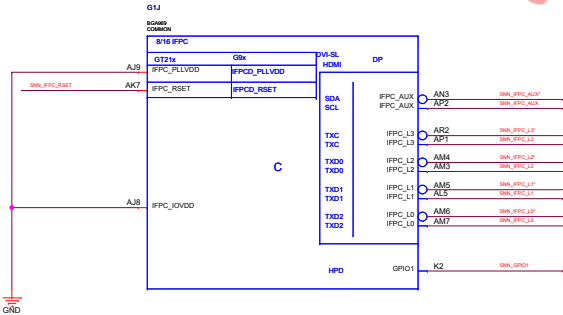
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A number line from 0 to 10. A vertical line is drawn at 5, and a horizontal line is drawn at 5. The intersection is labeled 'H'.



IFPC,IFPD

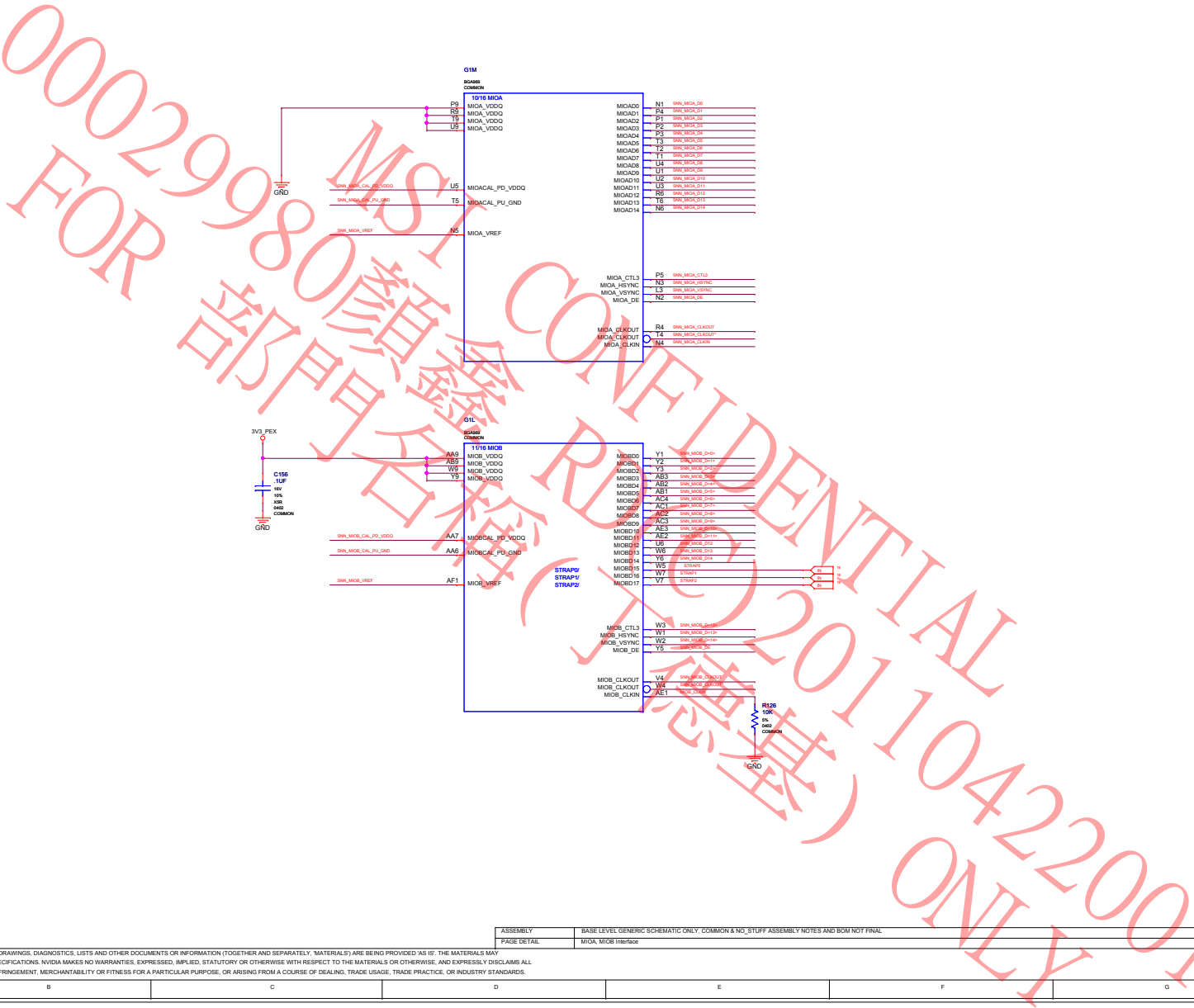


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PAGE DETAIL	IFPC/IFPD

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MIOA, MIOB Interface

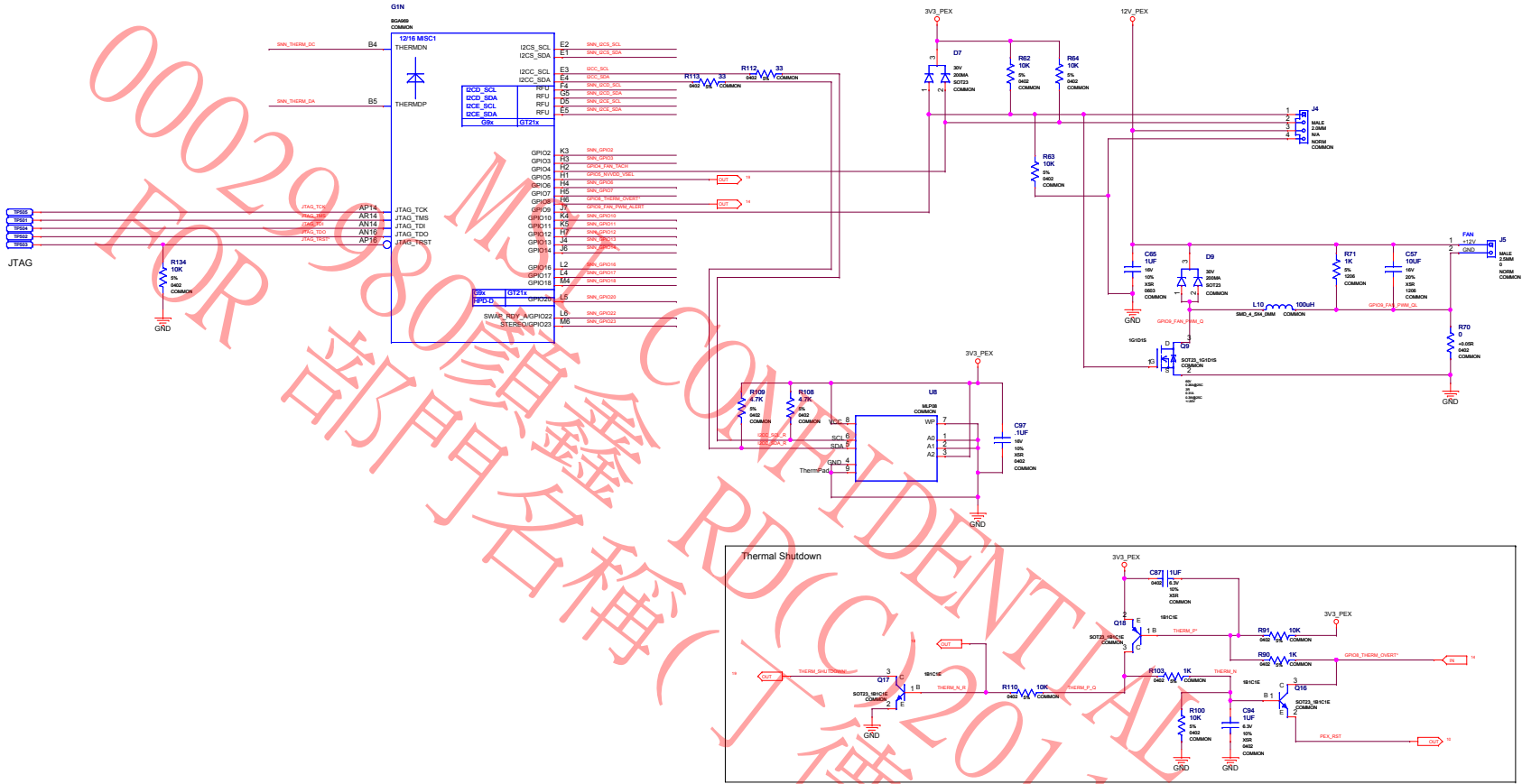


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PAGE DETAIL	MIOA, MIOB Interface

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Thermal Sensors, GPIOs, JTAG, Fan



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PAGE DETAIL	Thermal Sensors, GPIOs, JTAG, AND Fan

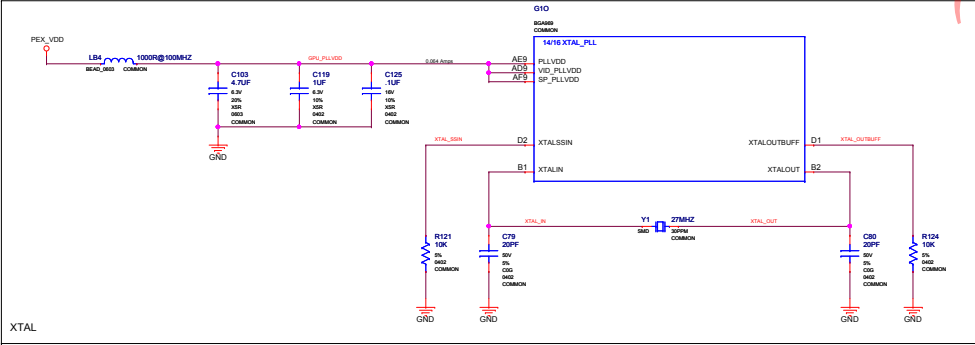
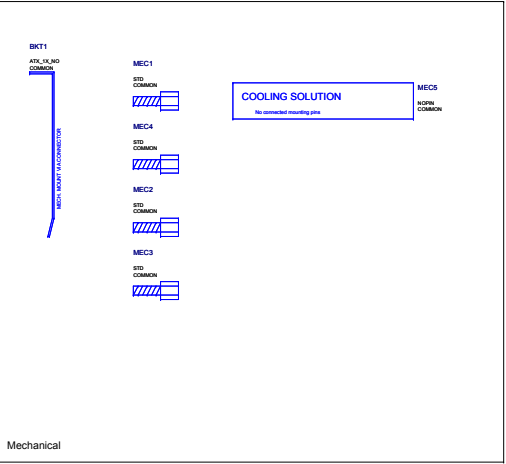
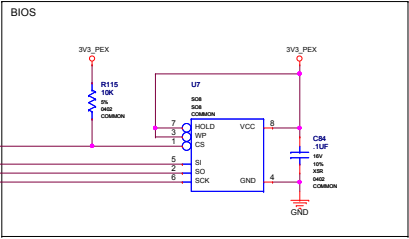
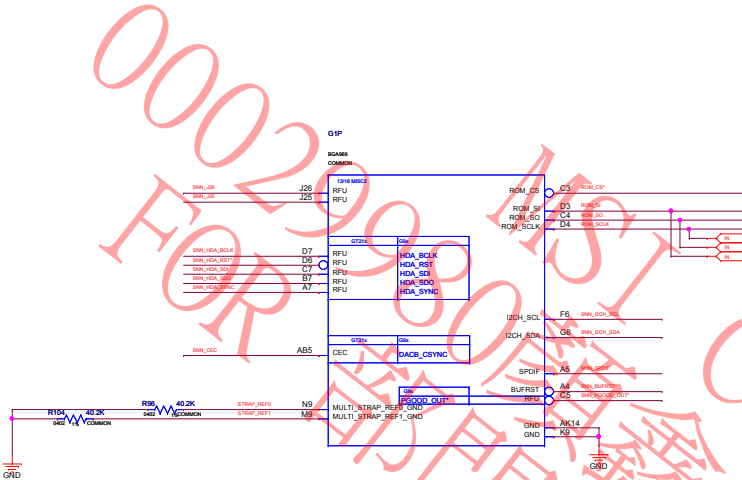
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BIOS, HDCP,XTAL, Mechanical

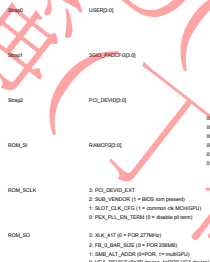


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PAGE DETAIL	BIOS, HDCP, XTAL AND MECHANICAL


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Straps



	1111 CDO	45x PD
	1000 OT	5x PD
	0001 C7238-05-0421 0000C7238-05-0420	15x PD 5x PD
0001 12000 6000x E CDO2 Korea/France		
0001 10000 6000x E CDO2 Germany		
0101 12000 6000x E CDO2 Germany		
0011 12000 6000x E CDO2 France		
0101 12000 6000x E CDO2 France		
0101 12000 6000x E CDO2 Ireland		
0101 12000 6000x E CDO2 Ireland		
	0110	35x PD
	0201	10x PD
	010 PD 2x	8 PDx
	010 PD 10x	9 PDx
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1422

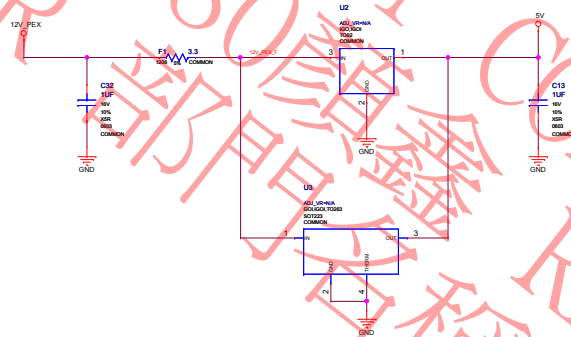
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Power Supply I: 5V

Figure 10: Net Name Legend

Net Name	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
12V_PEX	10000	12V	5.0A
GND	10000	0V	0.0A



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The schematic diagram illustrates a power supply circuit. It begins with a 12V_PEX input connected to a fuse F1 (3.3A). A capacitor C12 (10µF, 6V, 10%, 0603) is connected between the input and ground. The output of the fuse is connected to a 3.3V regulator U1 (AMS1117-3.3), which is also connected to ground. The output of the regulator is connected to a 12V_VDD input. This input is connected to a 12V_VDD output, which is then connected to a 2V_VDD input. A capacitor C13 (10µF, 10V, 10%, 0603) is connected between the 2V_VDD input and ground. The output of the 2V_VDD input is connected to a 2V_VDD output, which is then connected to a 2V_VDD input. A capacitor C14 (10µF, 10V, 10%, 0603) is connected between the 2V_VDD input and ground. The output of the 2V_VDD input is connected to a 2V_VDD output, which is then connected to a 2V_VDD input. A capacitor C15 (10µF, 10V, 10%, 0603) is connected between the 2V_VDD input and ground.

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PAGE DETAIL	Power Supply 1: 5V

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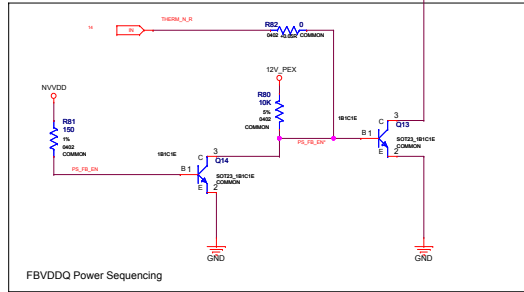
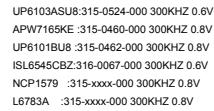
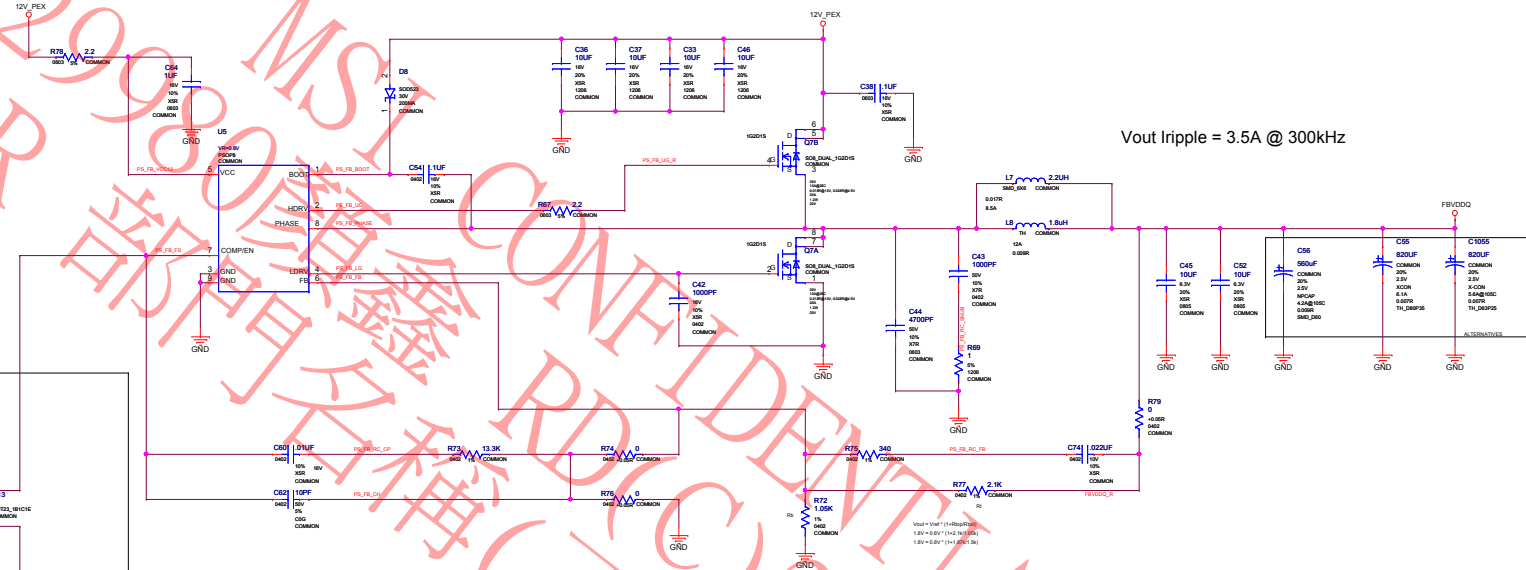
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PAGE DETAIL	Power Supply 1: 5V

Power Supply II: FBVDDQ


$$V_{in} I_{rms} = 2.3A @ 1.8V/6A$$


Vout Irripple = 3.5A @ 300kHz

[illegible]

Power Supply III: NVVDD

Vin Irms = 6.4A @ 0.925V/21A
Vin Irms = 7.4A @ 0.875V/25A

UP6103ASU8:315-0524-000 300KHz 0.6V
APW7165KE :315-0460-000 300KHz 0.8V
UP6101BU8 :315-0462-000 300KHz 0.8V
ISL6545CBZ:316-0067-000 300KHz 0.6V
NCP1579 :315-xxxx-000 300KHz 0.8V
L6783A :315-xxxx-000 300KHz 0.8V

NVVDD Power Sequencing

Net Name	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
----------	----------------	---------	--------------------

NVVDD	10MIL	0.925V	25A
PL_NVVDD_VCC12	10MIL		
PL_NVVDD_BOOT	10MIL		
PL_NVVDD_CP	10MIL		
PL_NVVDD_PHASE	10MIL		
PL_NVVDD_L2	10MIL		
PL_NVVDD_L3	10MIL		
PL_NVVDD_L4	10MIL		
PL_NVVDD_L5	10MIL		
PL_NVVDD_L6	10MIL		
PL_NVVDD_L7	10MIL		
PL_NVVDD_L8	10MIL		
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PL_NVVDD_L13	10MIL		
PL_NVVDD_L14	10MIL		
PL_NVVDD_L15	10MIL		
PL_NVVDD_L16	10MIL		
PL_NVVDD_L17	10MIL		
PL_NVVDD_L18	10MIL		
PL_NVVDD_L19	10MIL		
PL_NVVDD_L20	10MIL		

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PAGE DETAIL Power Supply IE NVVDD

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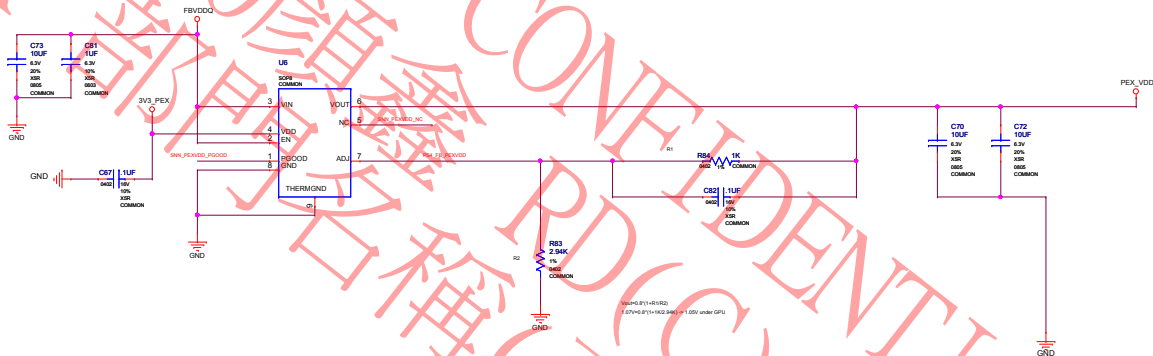
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Power Supply IV: PEXVDD



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PAGE DETAIL	Power Supply: PEXVDD

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