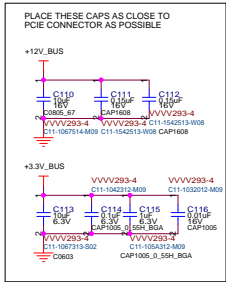




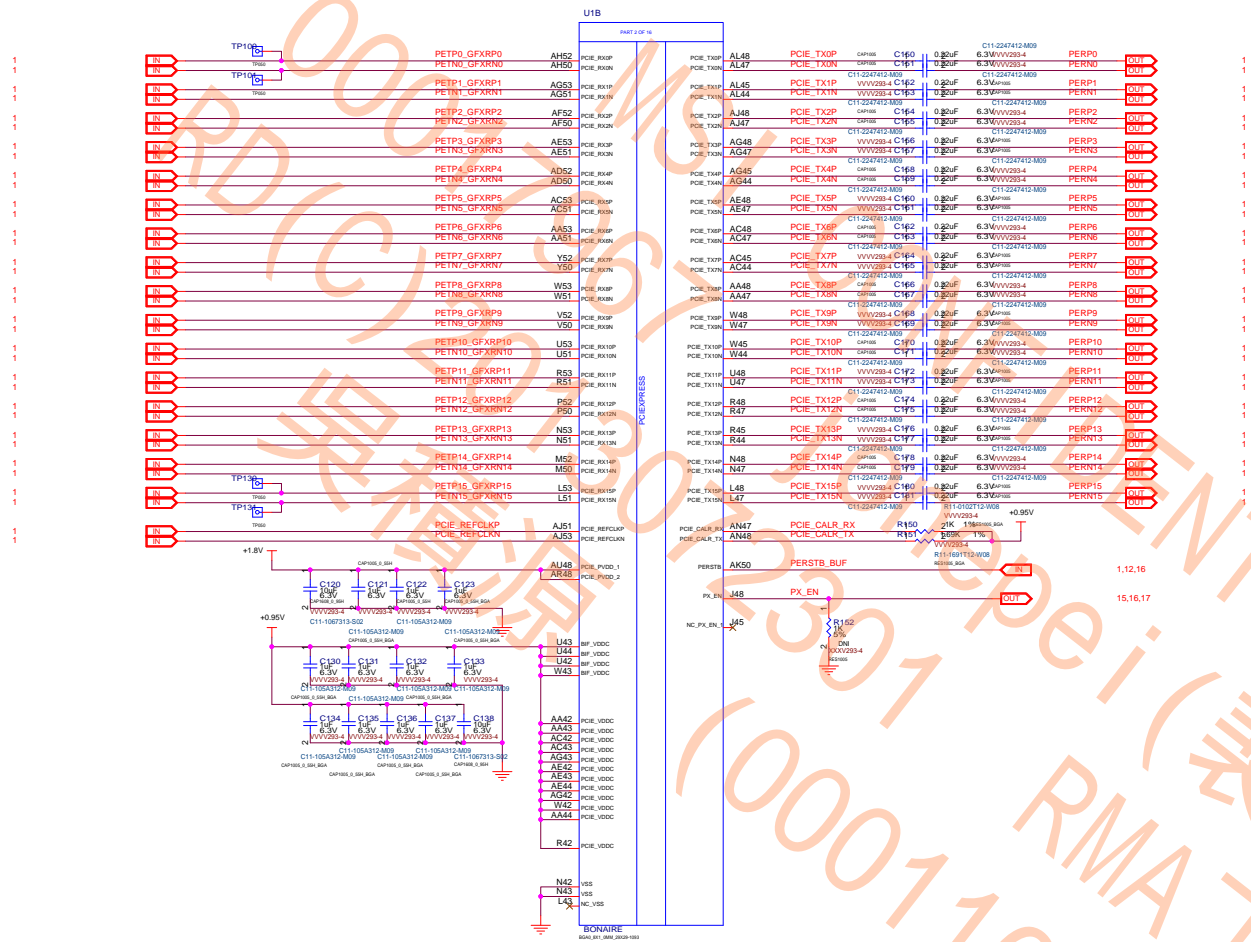
(1) PCI-EXPRESS EDGE CONNECTOR



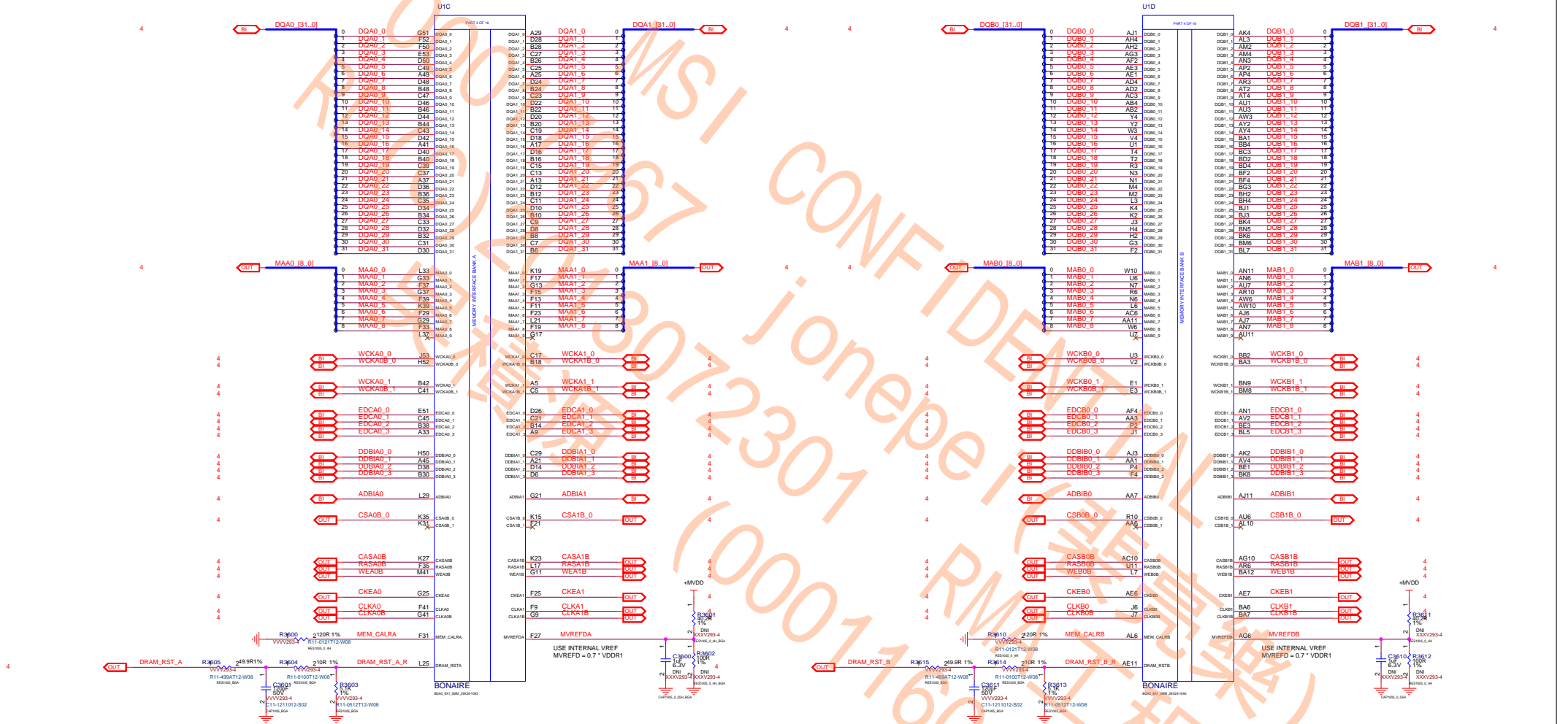
DNI	DO NOT INSTALL
b or #	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND



(2) BONAIRE PCIE INTERFACE



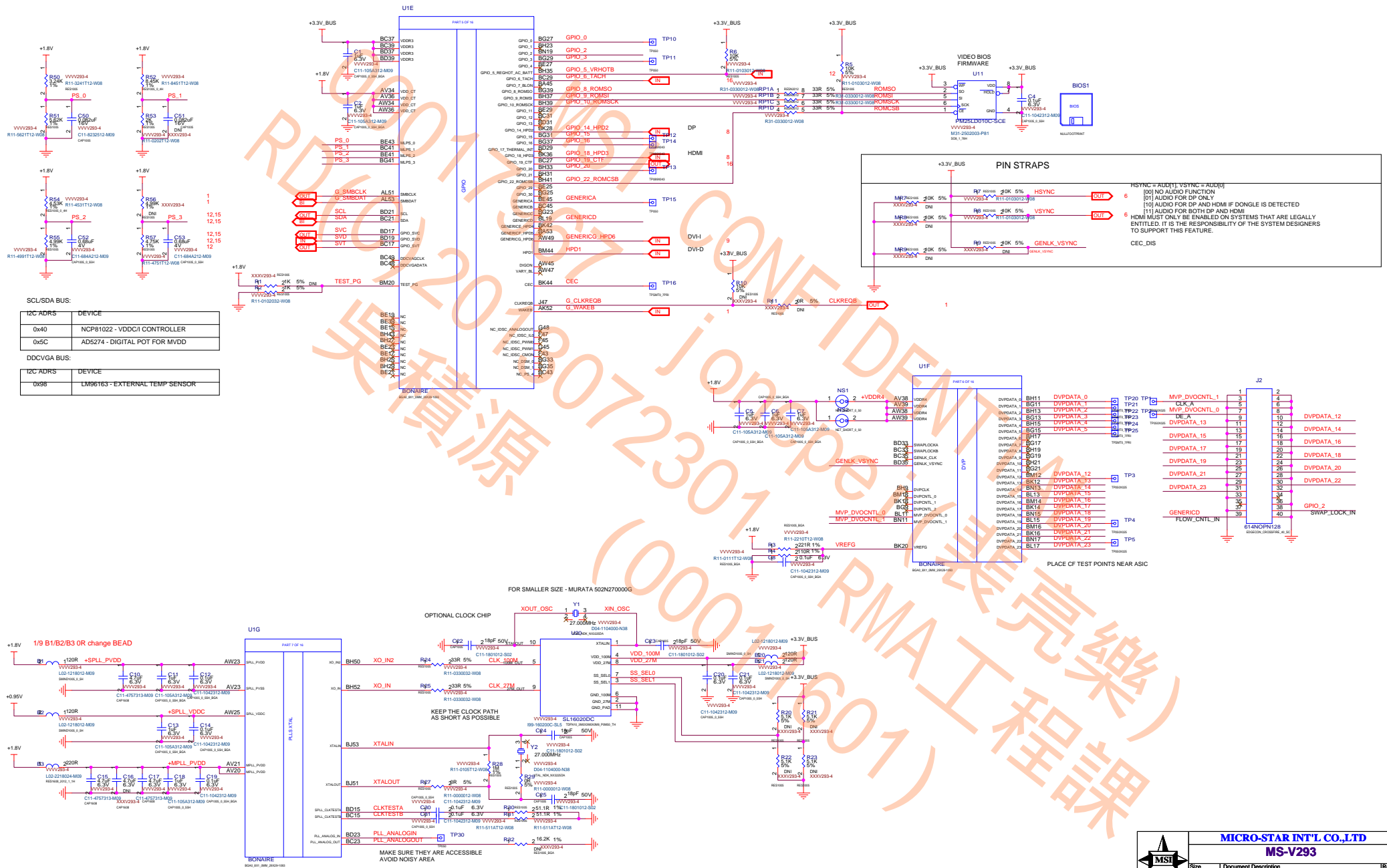
(3) BONAIRE MEMORY INTERFACE



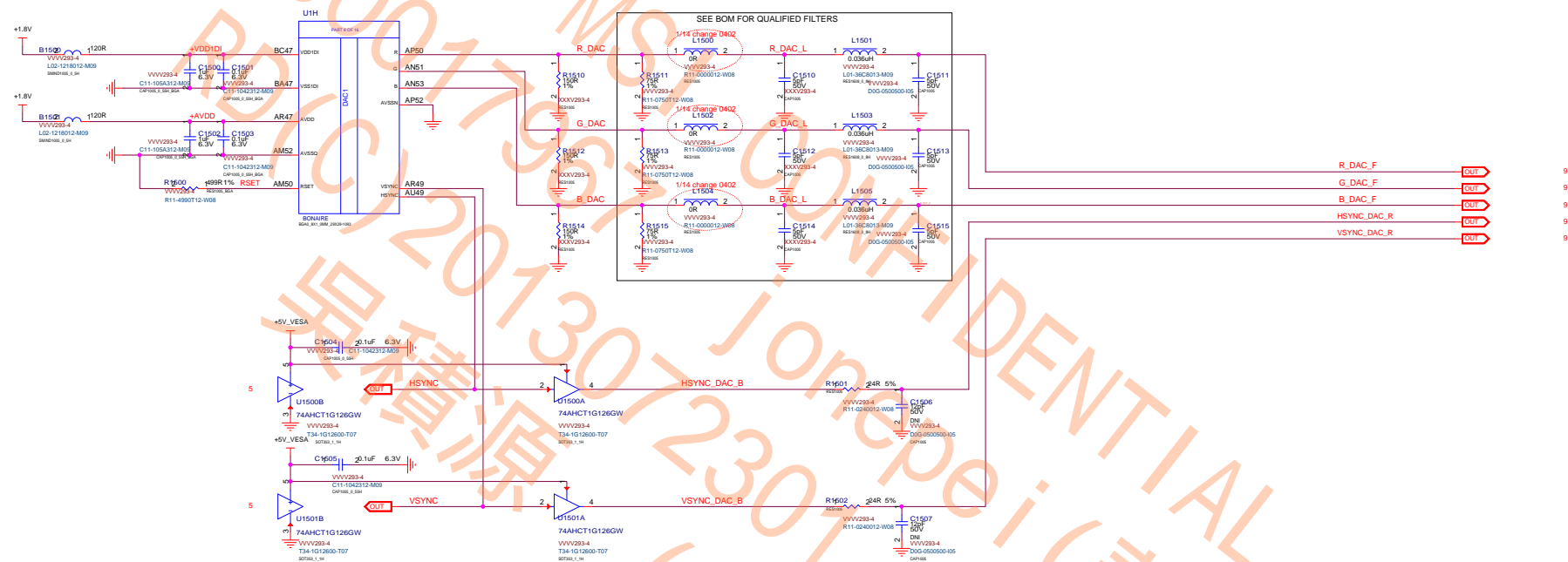
(4) GDDR5 CHAB x32



(5) BONAIRE GPIO MLPS CF PLL XTAL



(6) BONAIRE DAC



OPTIONAL ESD PROTECTION DIODES

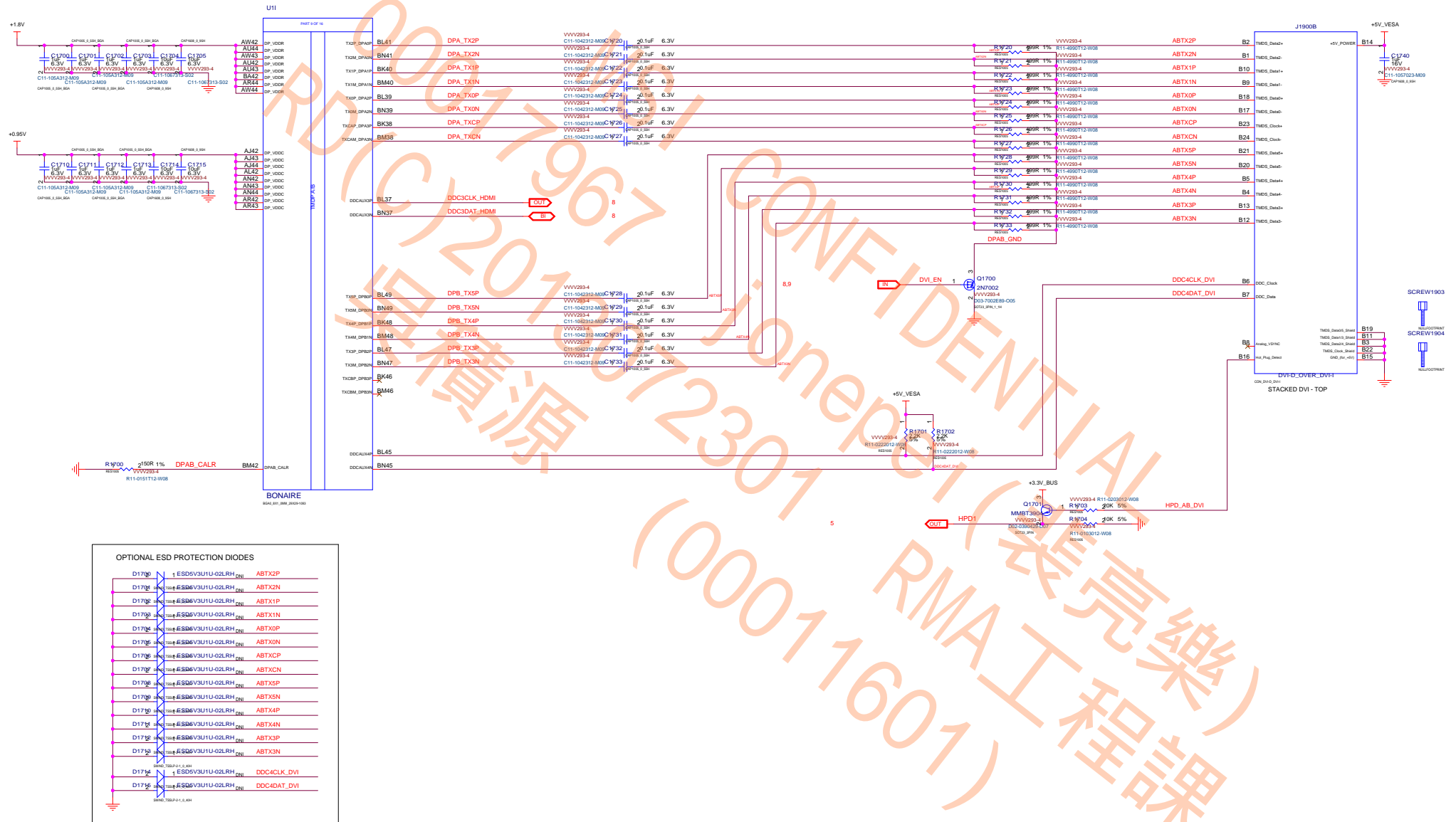


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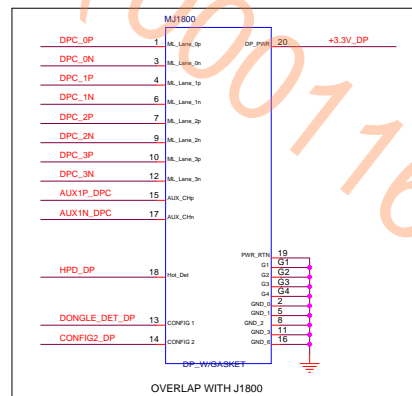
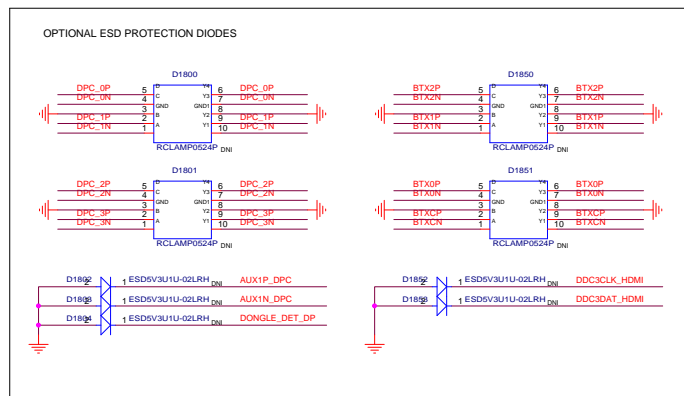
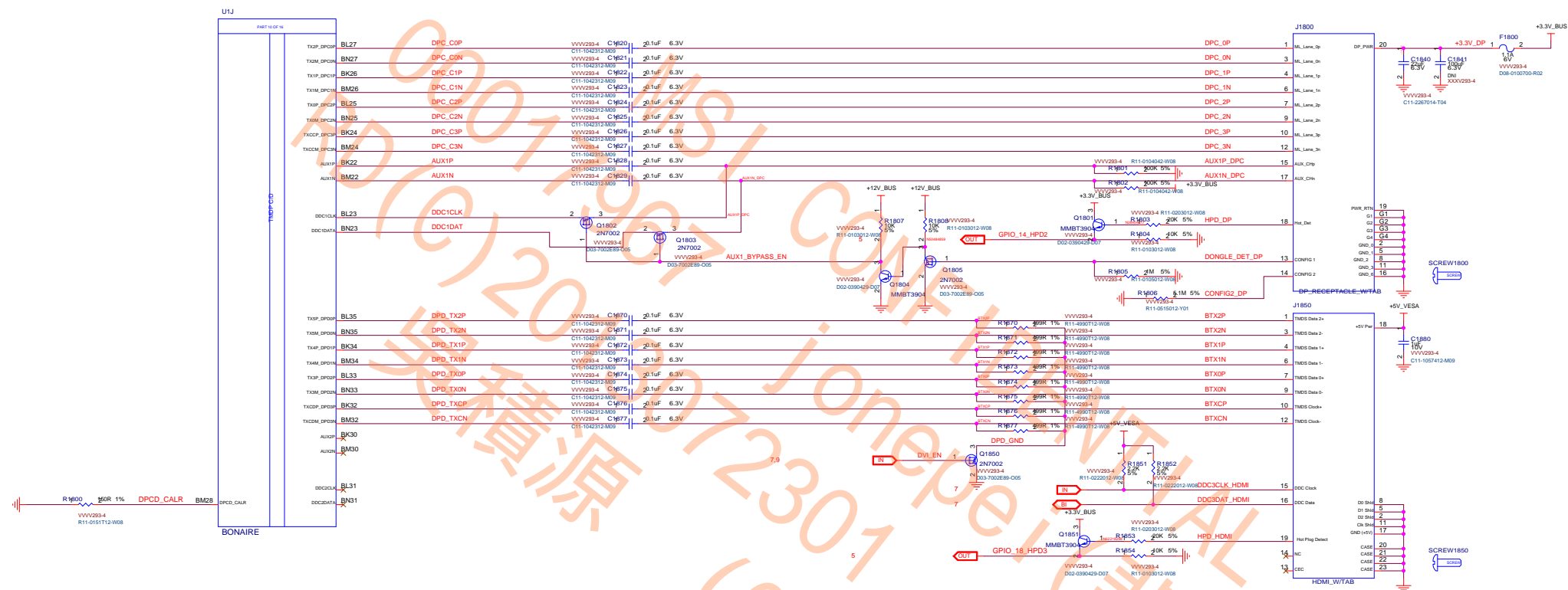
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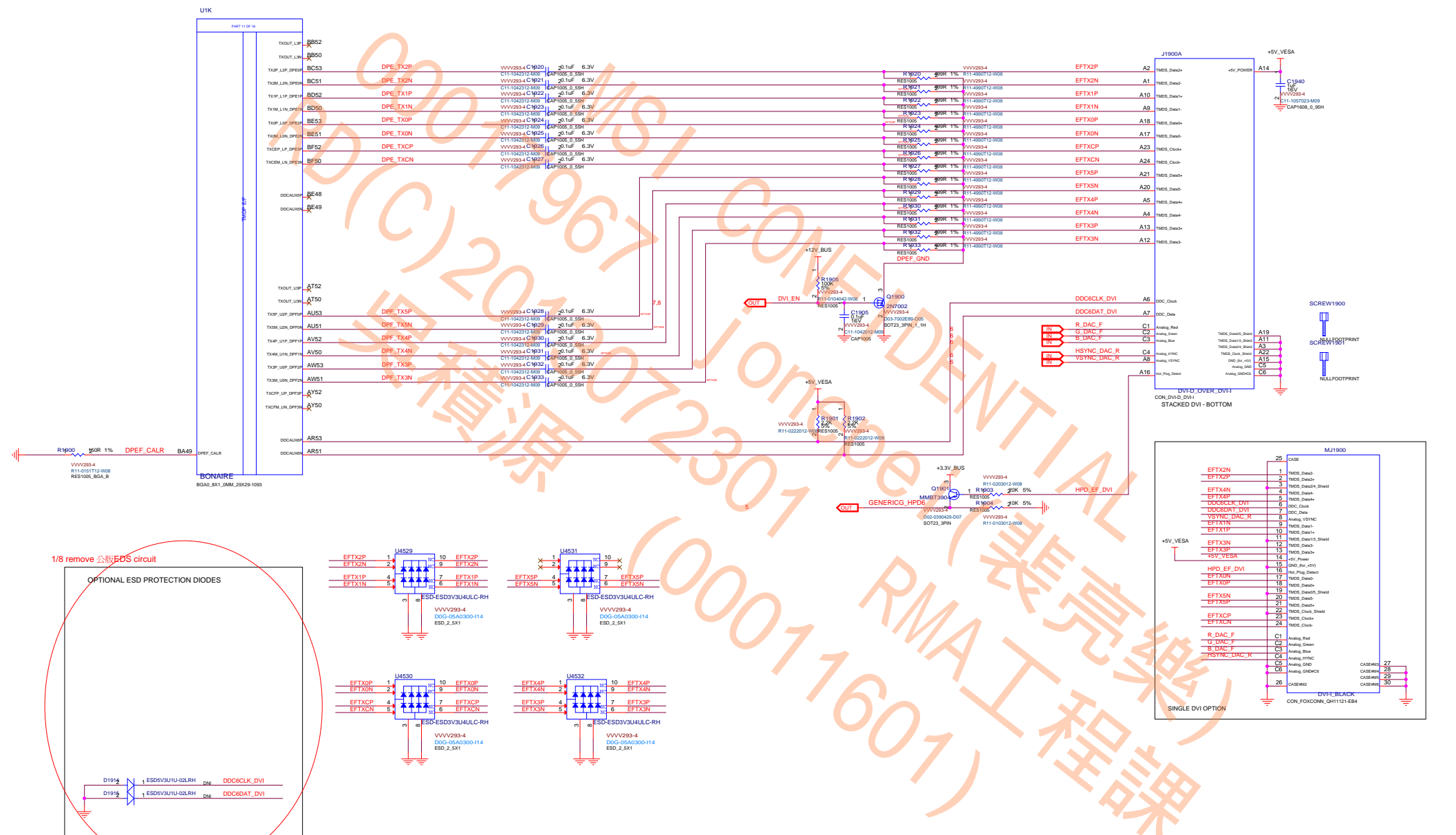
(7) BONAIRE TMDPAB dDVI



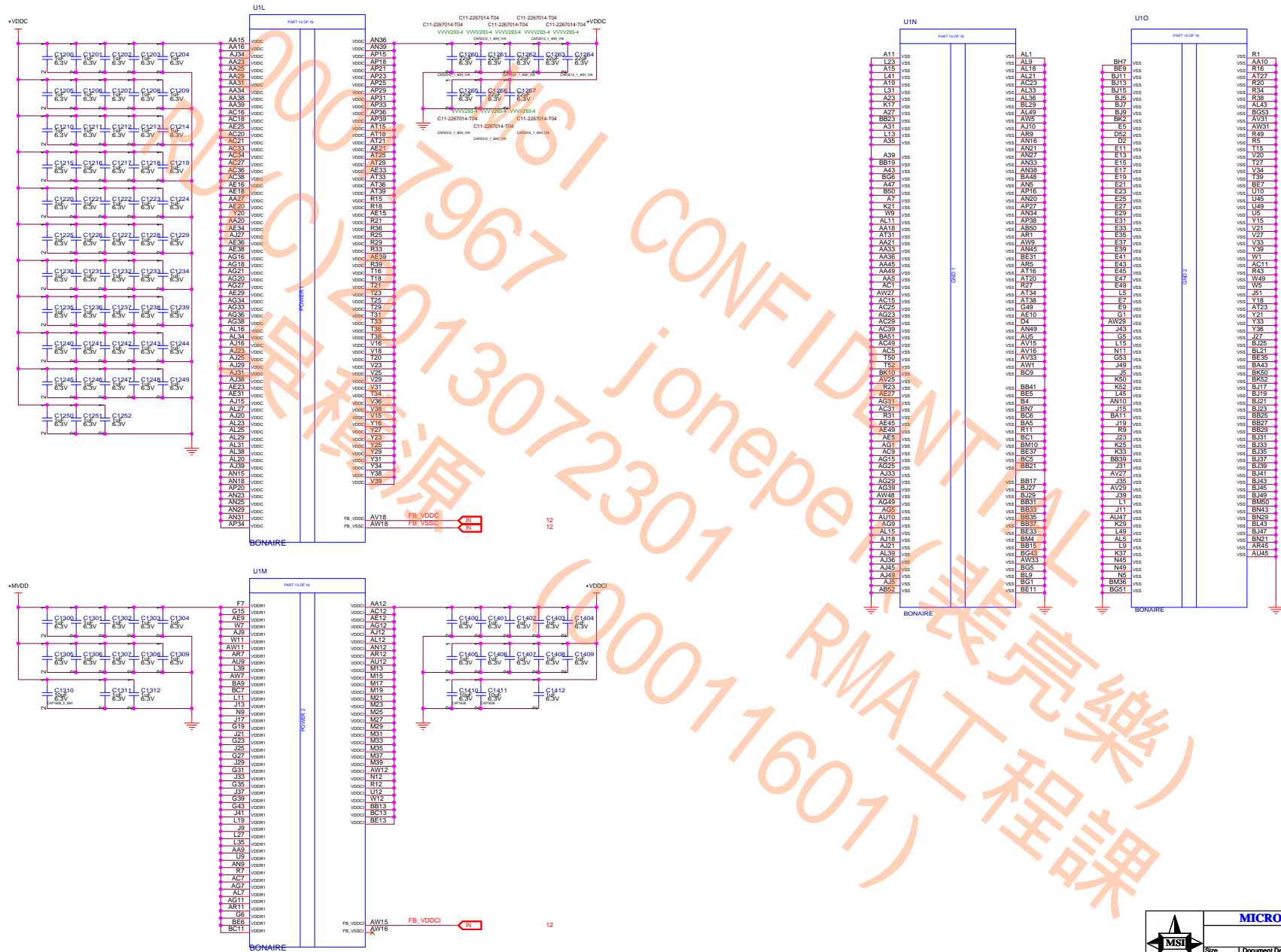
(8) BONAIRE TMDPCD DP HDMI



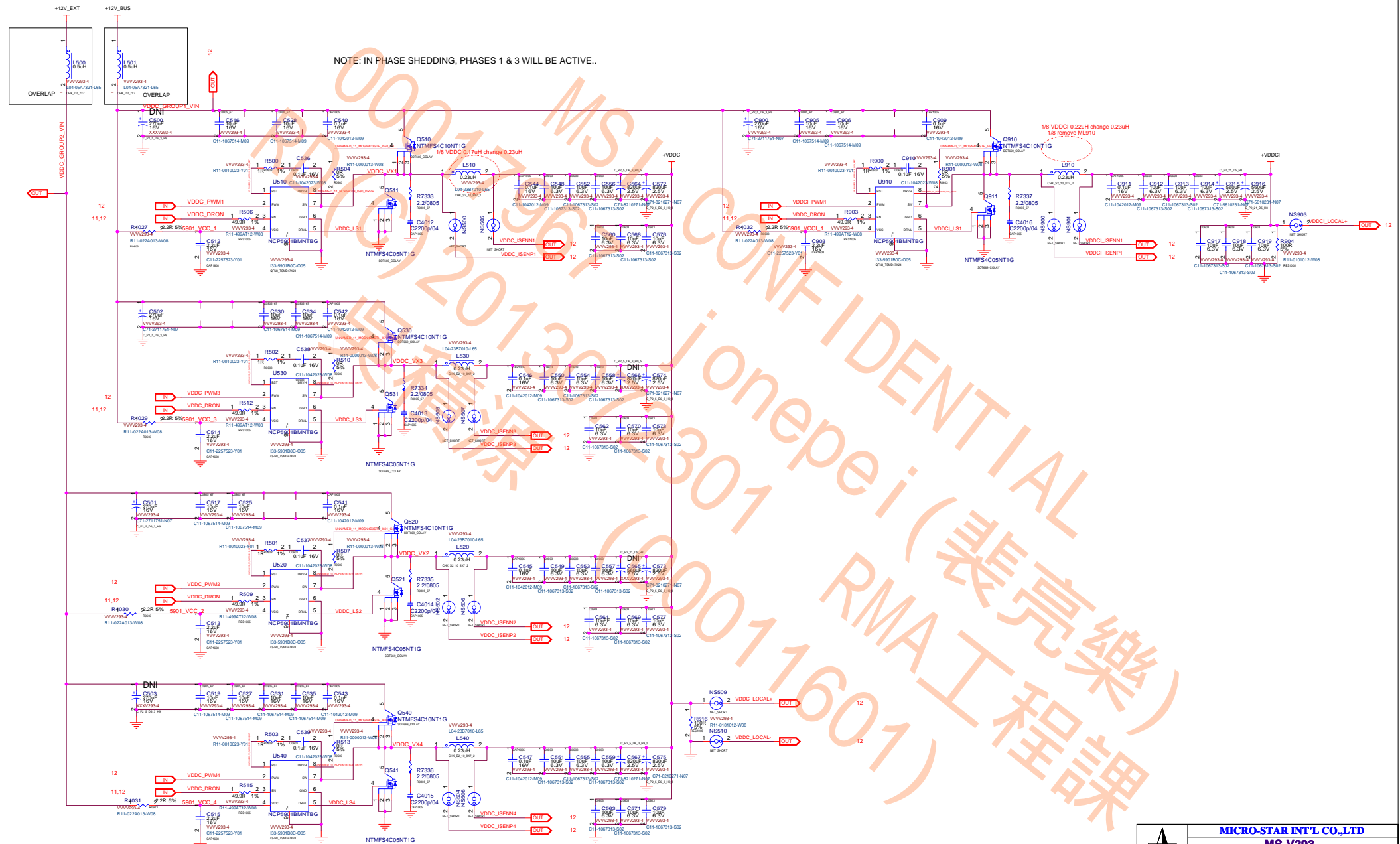
(9) BONAIRE TMDPEF dDVI



(10) BONAIRE POWER AND GROUND



(11) VDDC_VDDCI_01

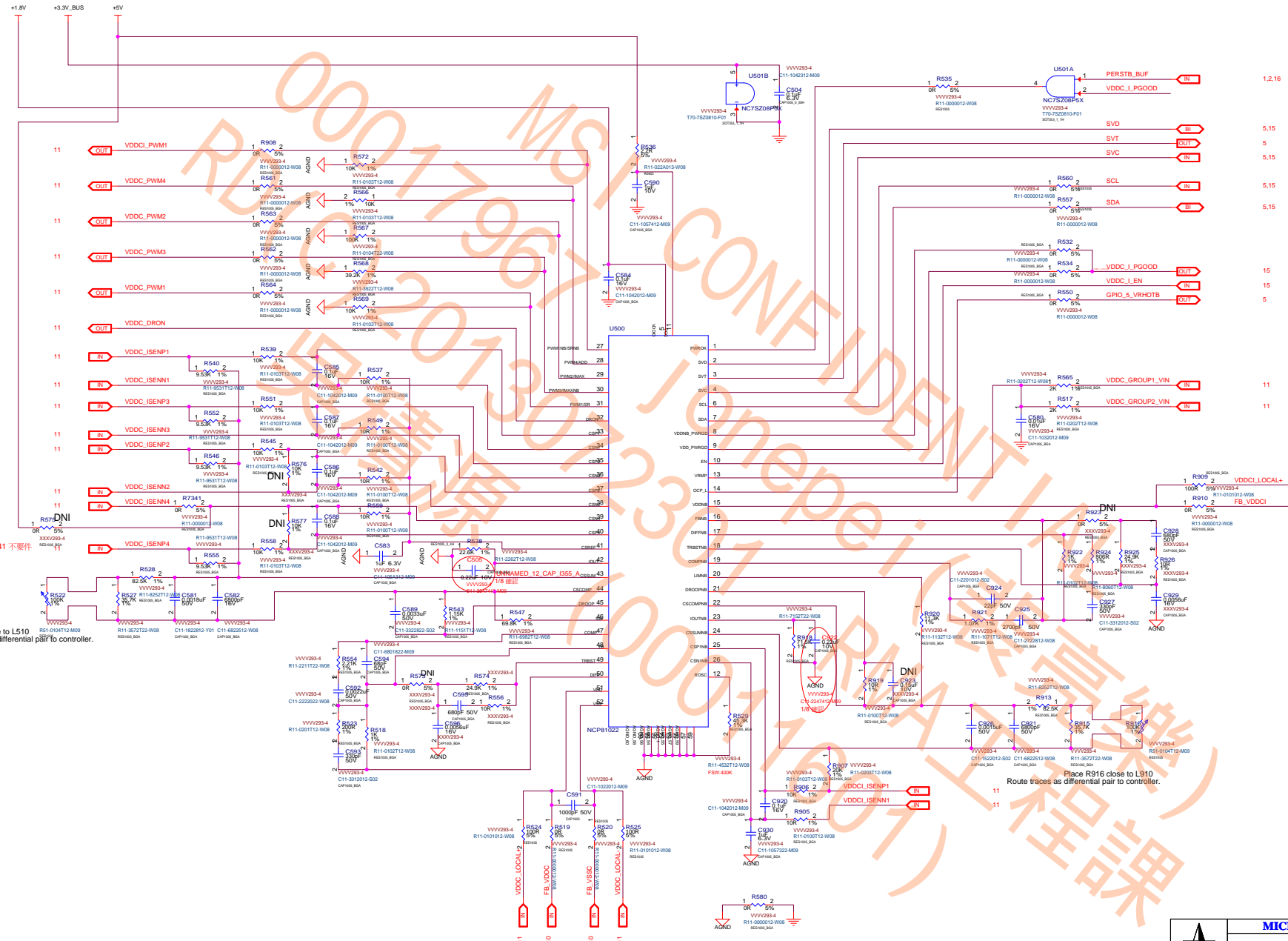


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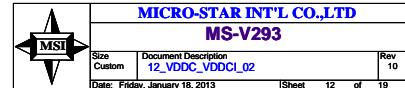
Size Custom	Document Description 11_VDDC_VDDCI_01	Rev 10
Date: Friday, January 18, 2013		Sheet 11 of 19

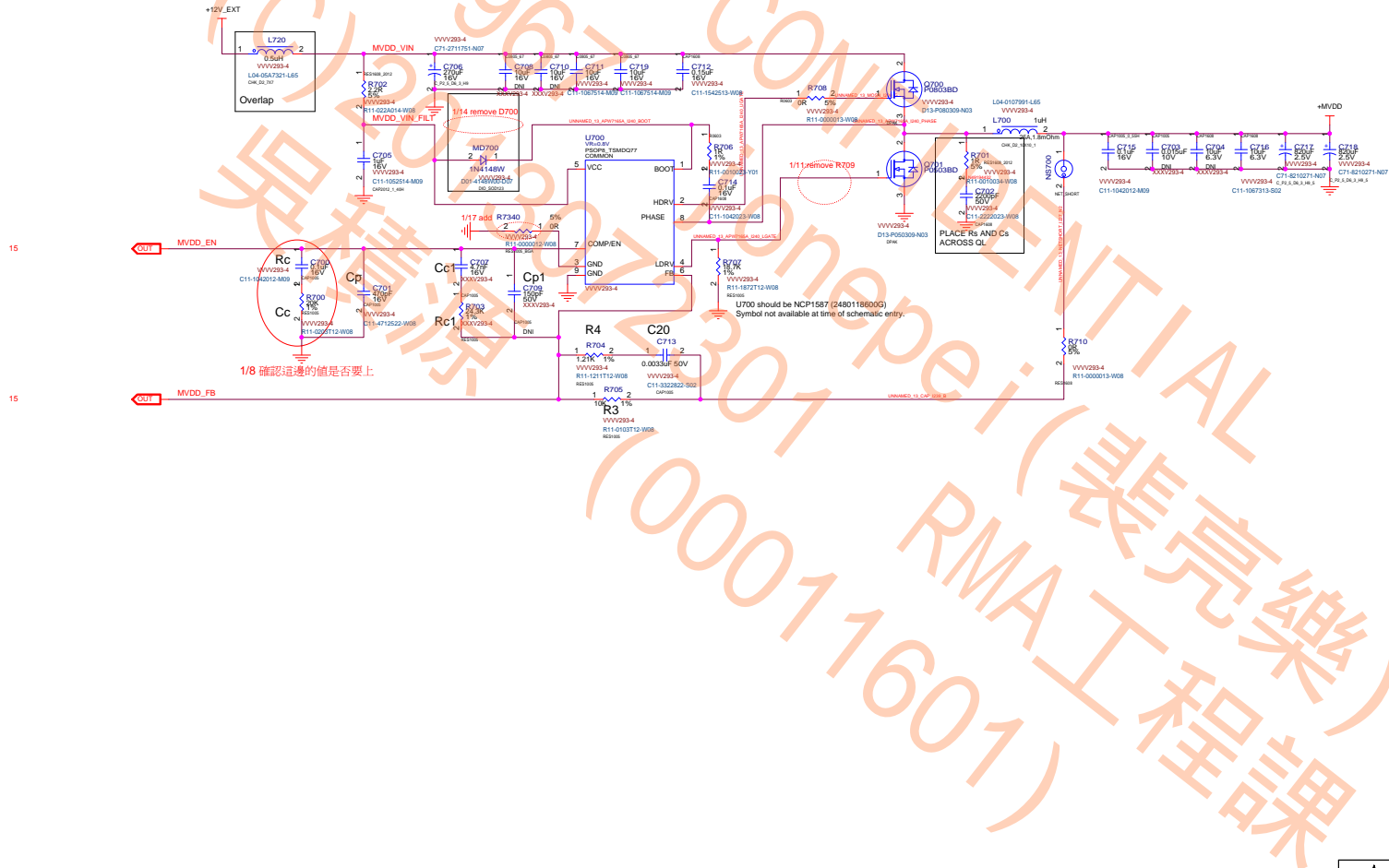
(12) VDDC_VDDCI_02



Place R522 close to L510
Route traces as differential pair to controller.

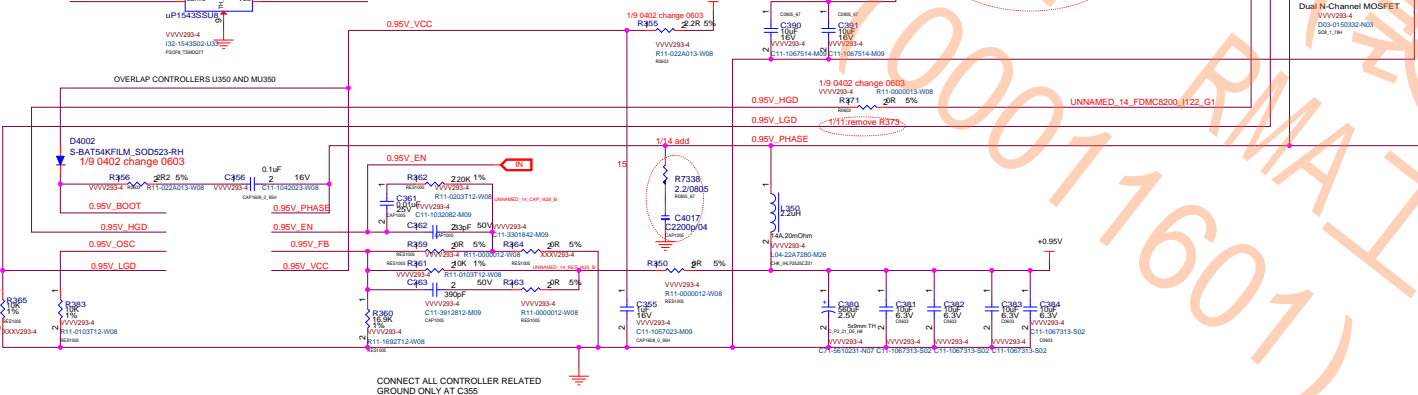
Route traces as differential pair to controller.





[illegible][illegible]

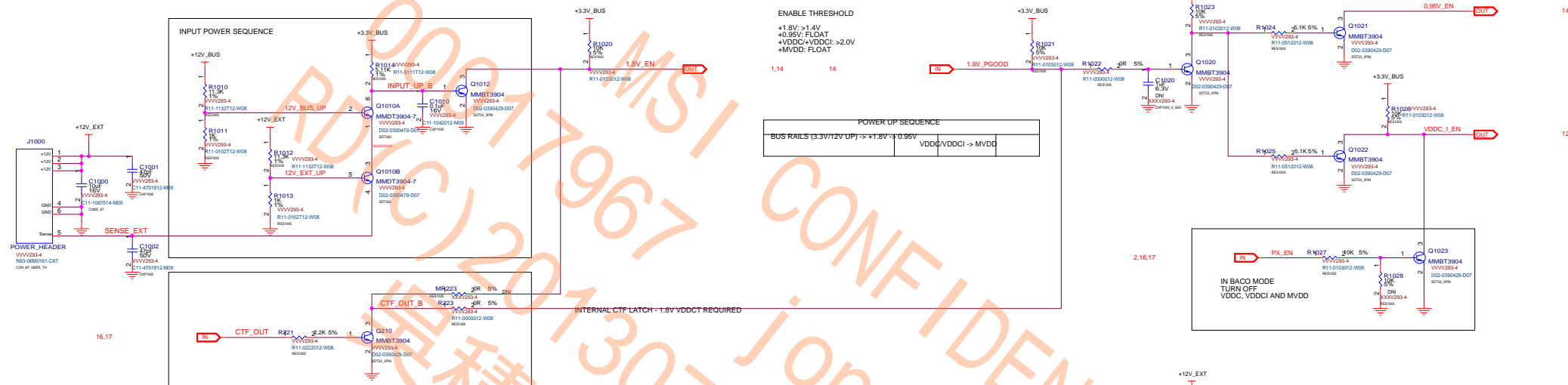
		U350			
0.95V_BOOT	1	BOOT	PHASE	8	0.95V_PHASE
0.95V_HGD	2	UGATE	COMP	7	0.95V_EN
0.95V_OSC	3	GND	FB	6	0.95V_FB
0.95V_LGD	4	LGATE	VCC	5	0.95V_VCC



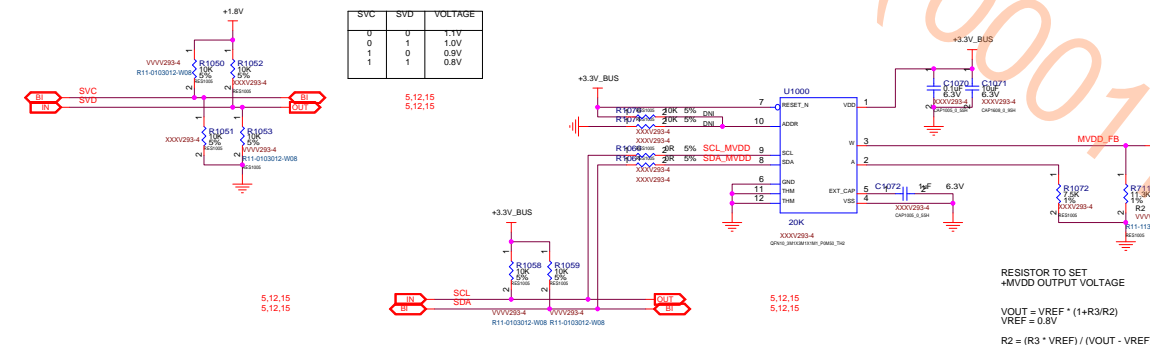
CONNECT ALL CONTROLLER RELATED
GROUND ONLY AT C355



(15) POWER MANAGEMENT

SVI2 BOOT UP VOLTAGE (VDDC/VDDCI)

SVC	SVD	VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

RESISTOR TO SET
+MVDD OUTPUT VOLTAGE

$$V_{OUT} = V_{REF} * (1 + R3/R2)$$

$$V_{REF} = 0.8V$$

$$R2 = (R3 * VR$$

$$R2 = (R3 * VREF) / (VOUT - VREF)$$



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	Size

Document Description

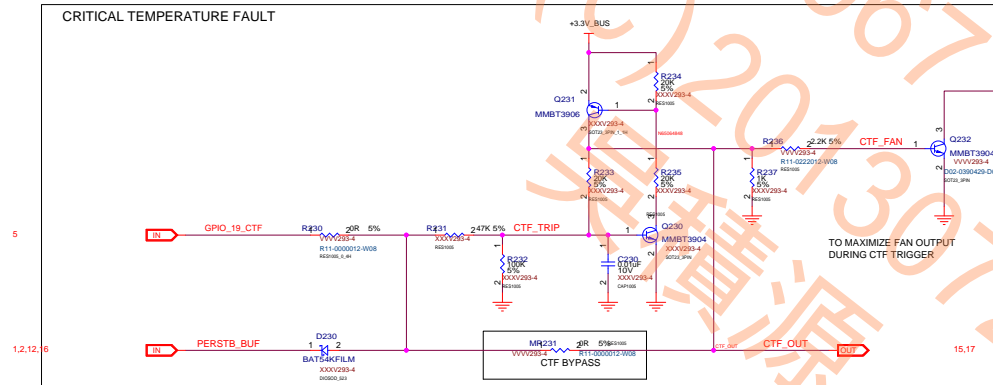
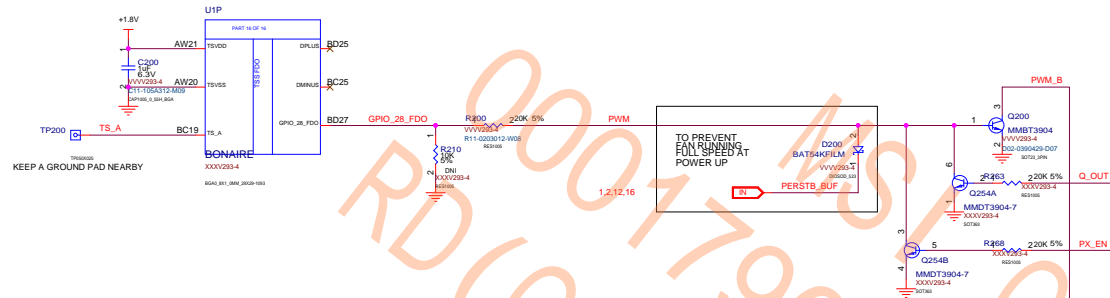
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15_POWER MANAGEMENT

Date: Friday, January 18, 2013

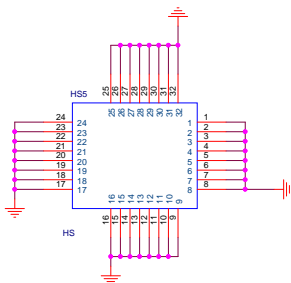
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(16) MECHANICAL AND THERMAL MANAGEMENT



ASIC XT HEATSINK WITHOUT SHROUD	7122500400G / 7121500400G
ASIC XT HEATSINK WITH SHROUD	7122E00400G / 7121E00400G
ASIC PRO HEATSINK WITHOUT SHROUD	7122A00400G
PASSIVE MEMORY HEATSINK FRONT	7122200400G / 7121700400G
PASSIVE REGULATOR HEATSINK	7122300400G / 7121300400G



ASIC SOCKET



BONAIRE M3 SOCKET
PN 6090041300G

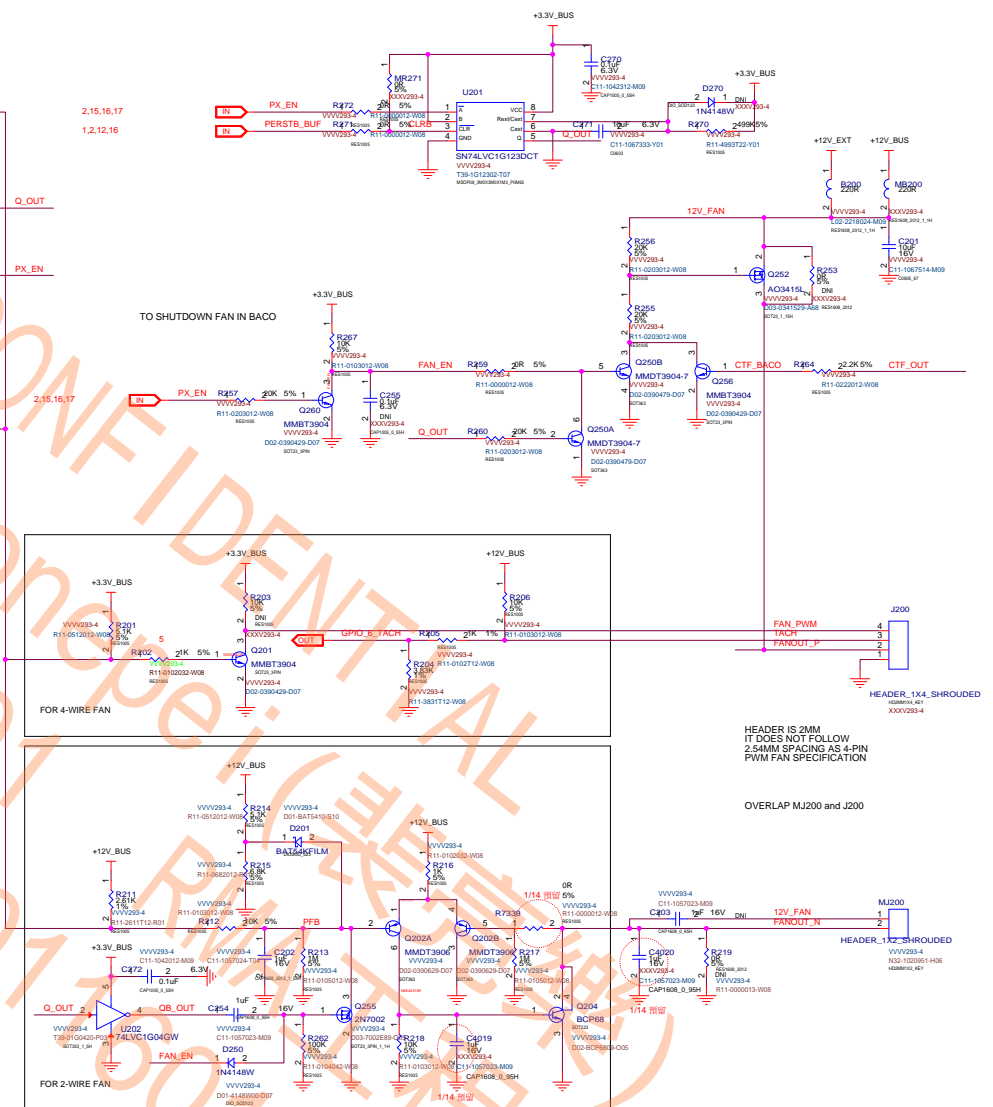
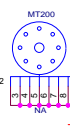
BRACKET



8020056100G
DP WO TAB, HDMI, STACKED DVI

8020056600G
DP W TAB, HDMI, STACKED DVI

BRACKET MT HOLE



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(17) DEBUG CIRCUIT

JTAG



LM96163 FOR BACKUP THERMAL CONTROL

1/10: remove U4003 circuit

SWITCHES

1/10: remove SW4002

VTMM - TEST CONNECTOR FOR VOLTAGE MEASUREMENTS

1/10: remove J4010 and J4011

LED LIGHTS

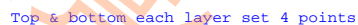
LED RED "ON" INDICATES CTF FAULT




LED GREEN "ON" INDICATES BACO MODE



optical cross point



AMD				TITLE: BONAIRE PRO G5 X32		DOCUMENT NUMBER: 105-CSE3xx-00C		DATE: Tue Dec 11 22:10:57 2012		SHEET NUMBER: 19 OF 19		REV: 1.0				
REVISION HISTORY				ENGINEER: <ENGINEER>		NOTES: NOTE		<div>CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. This AMD-based schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding the schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.</div>				AMD - GRAPHICS 1 COMMERCE VALLEY MARKHAM, ONTARIO, L3T 7X6				
SCH Rev	PCB Rev	Date	REVISION DESCRIPTION													
0	000	06/07/2012	INITIAL DESIGN													
<div>00017967 MSI CONFIDENTIAL RD(C)2013072301 jonepei (裴亮樂) 吳積源 RMA工程課 (00011601)</div>																
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Document Description 19_REVISION HISTORY

Date: Friday, January 18, 2013

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