PG150-C03

384b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

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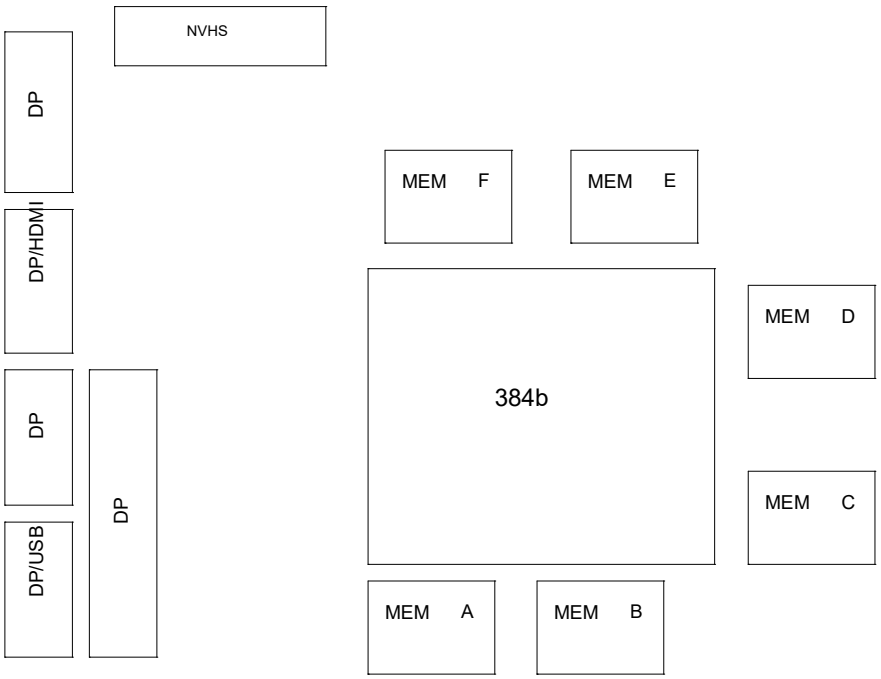
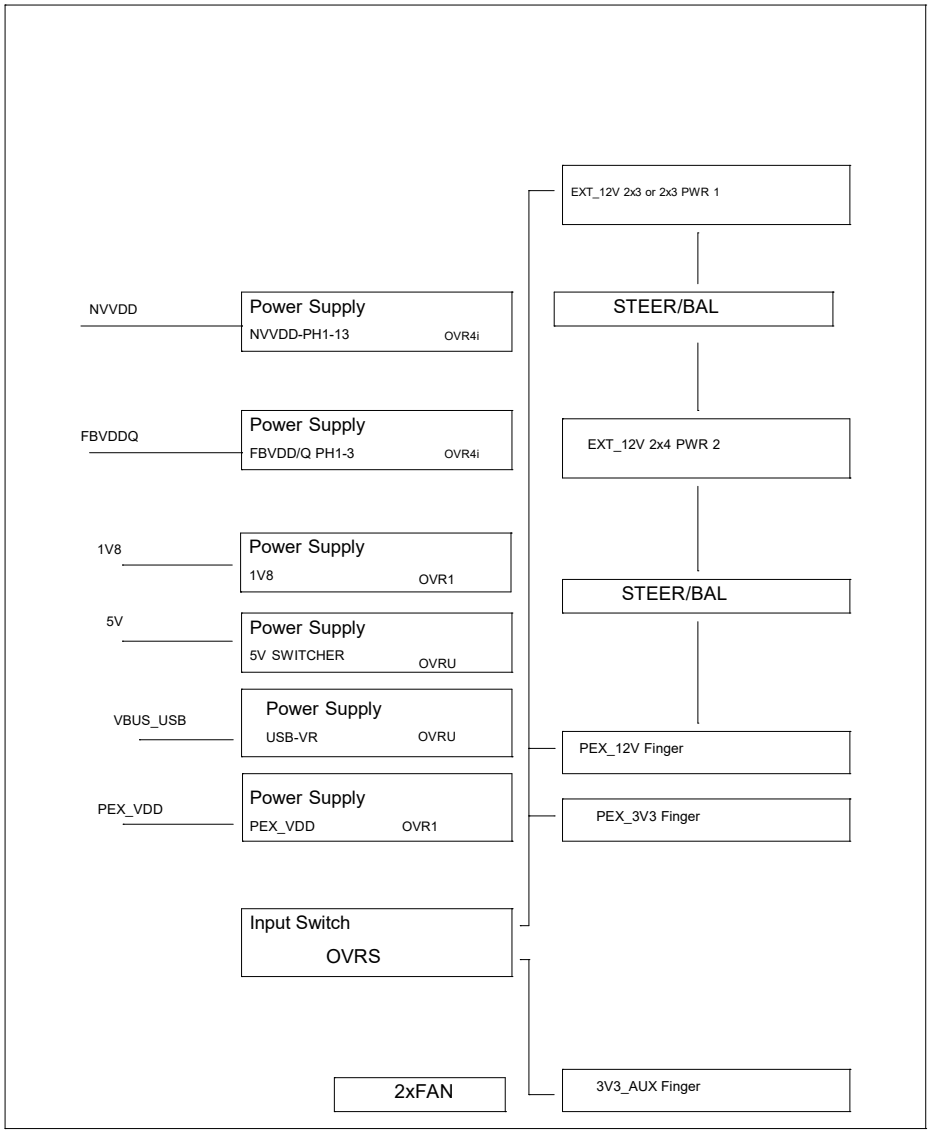
Block Diagram





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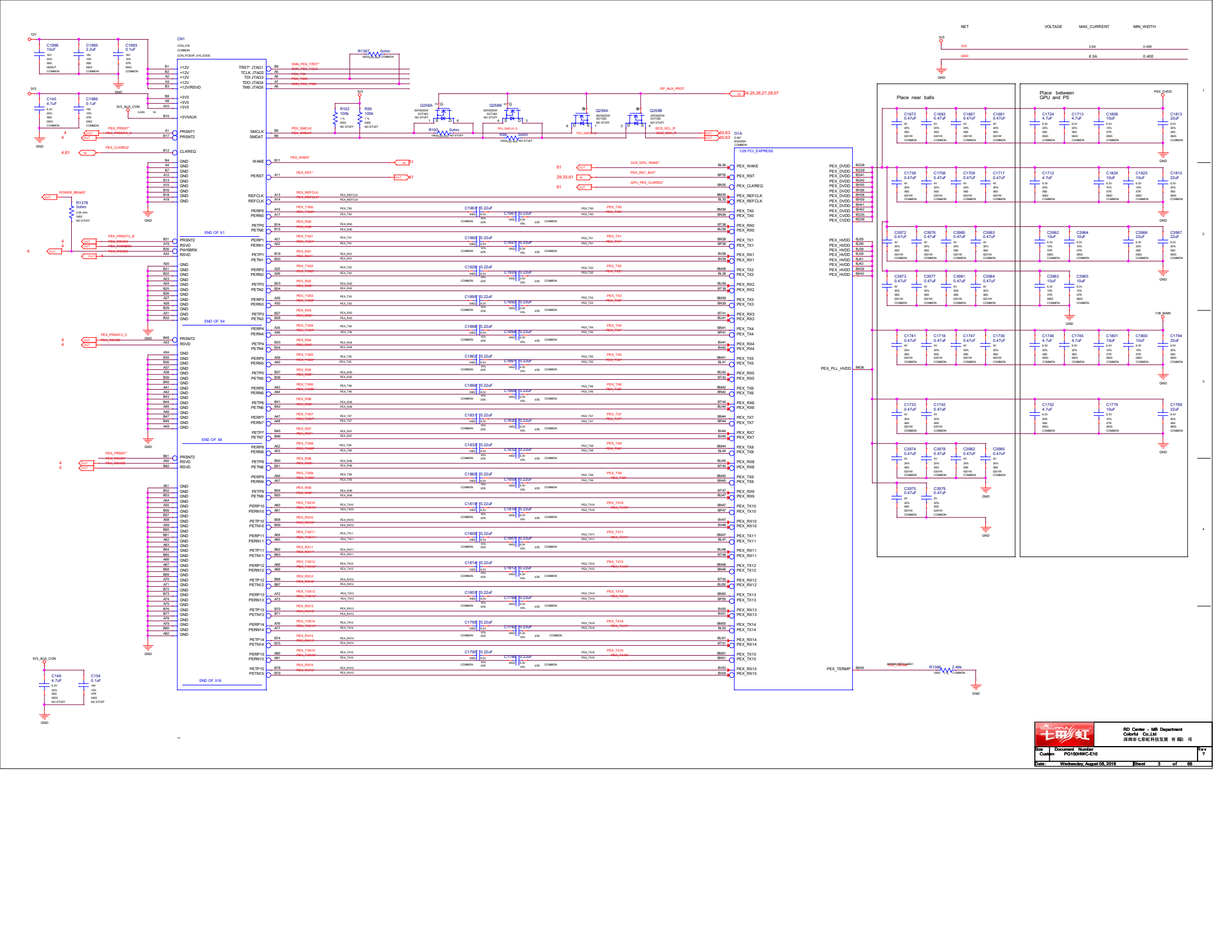
NET
VOLTAGE
MAX_CURRENT
MIN_WIDTH
3V3
3.0A
0.400
GND
8.5A
0.400
CN1
CON_X16
COMMON
CON_PCIEXP_X16_EDGE
1/28 PCI_EXPRESS
Place near balls
Place between GPU and PS
PEX_DVDD
PEX_HVDD
PEX_PLL_HVDD
PEX_TERMP
PEX_WAKE
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_REFCLK
PEX_TERMP
END OF X1
END OF X4
END OF X8
END OF X16
TVB_MAIN
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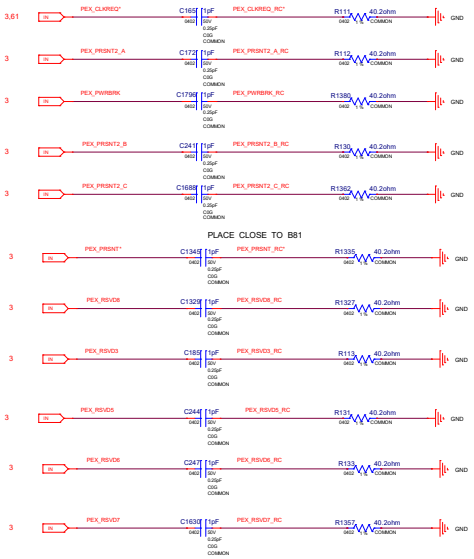
PCI TERM



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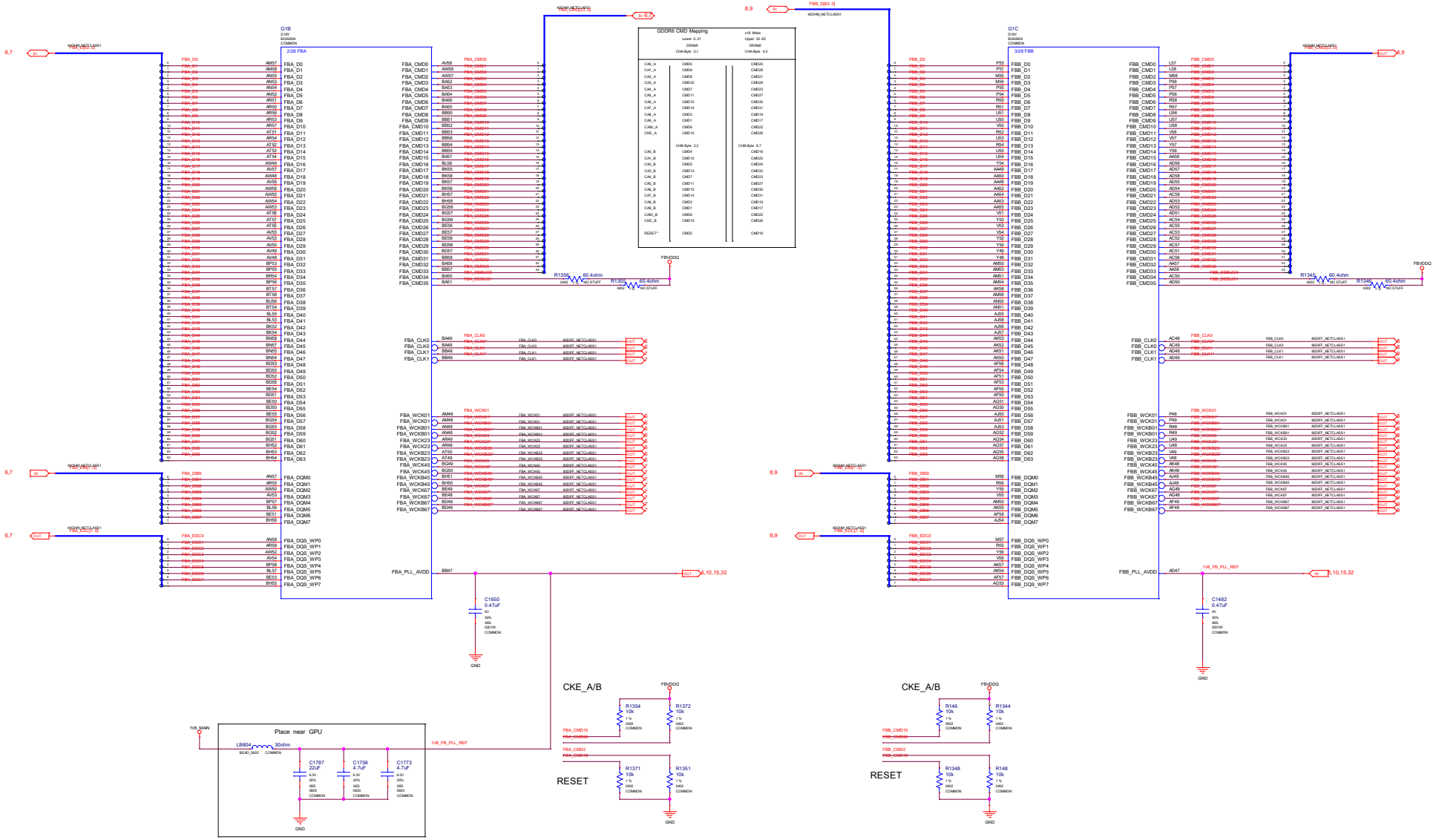
MEMORY: GPU Partition A/B



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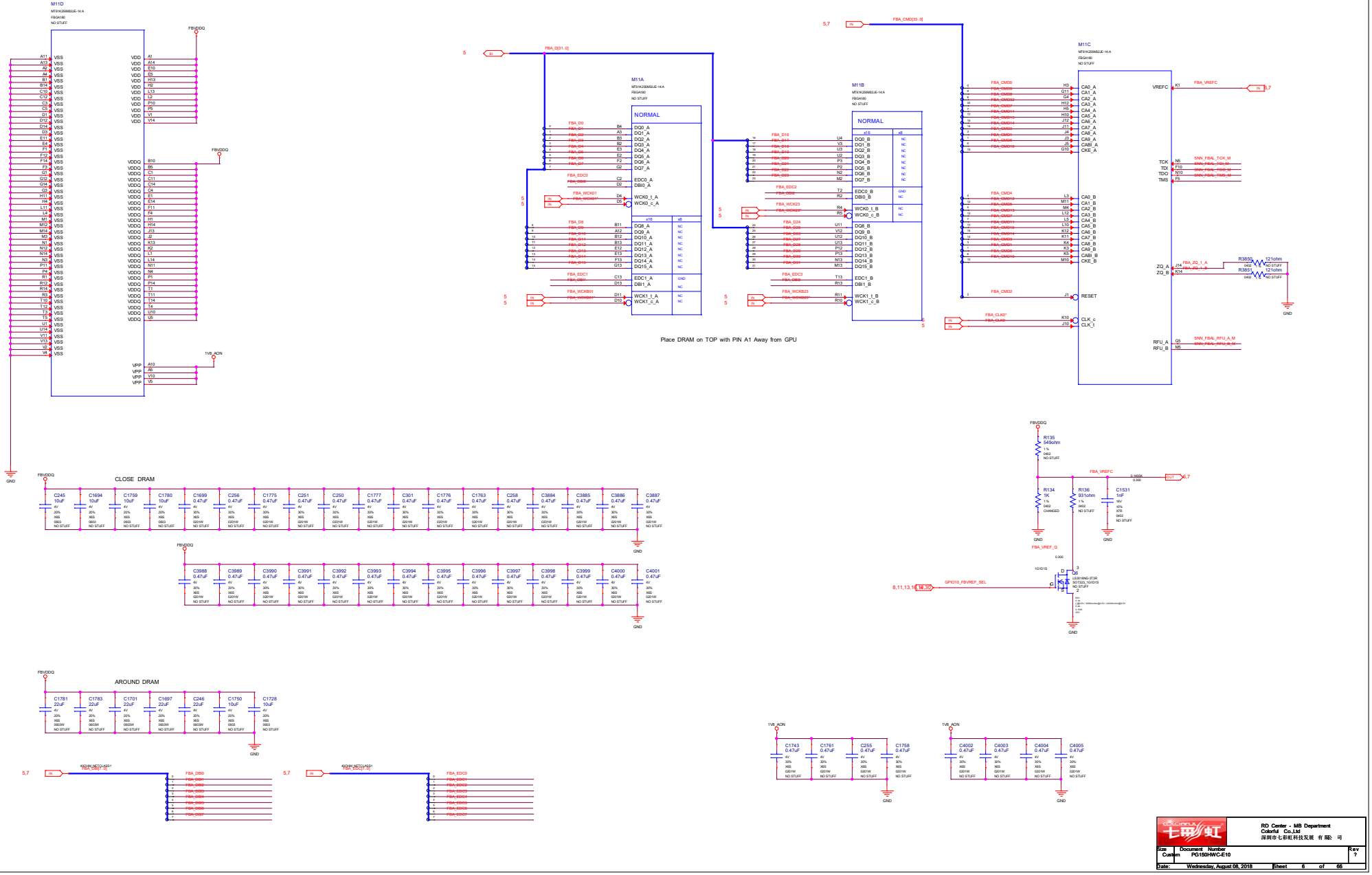
MEMORY: FBA Partition 31..0



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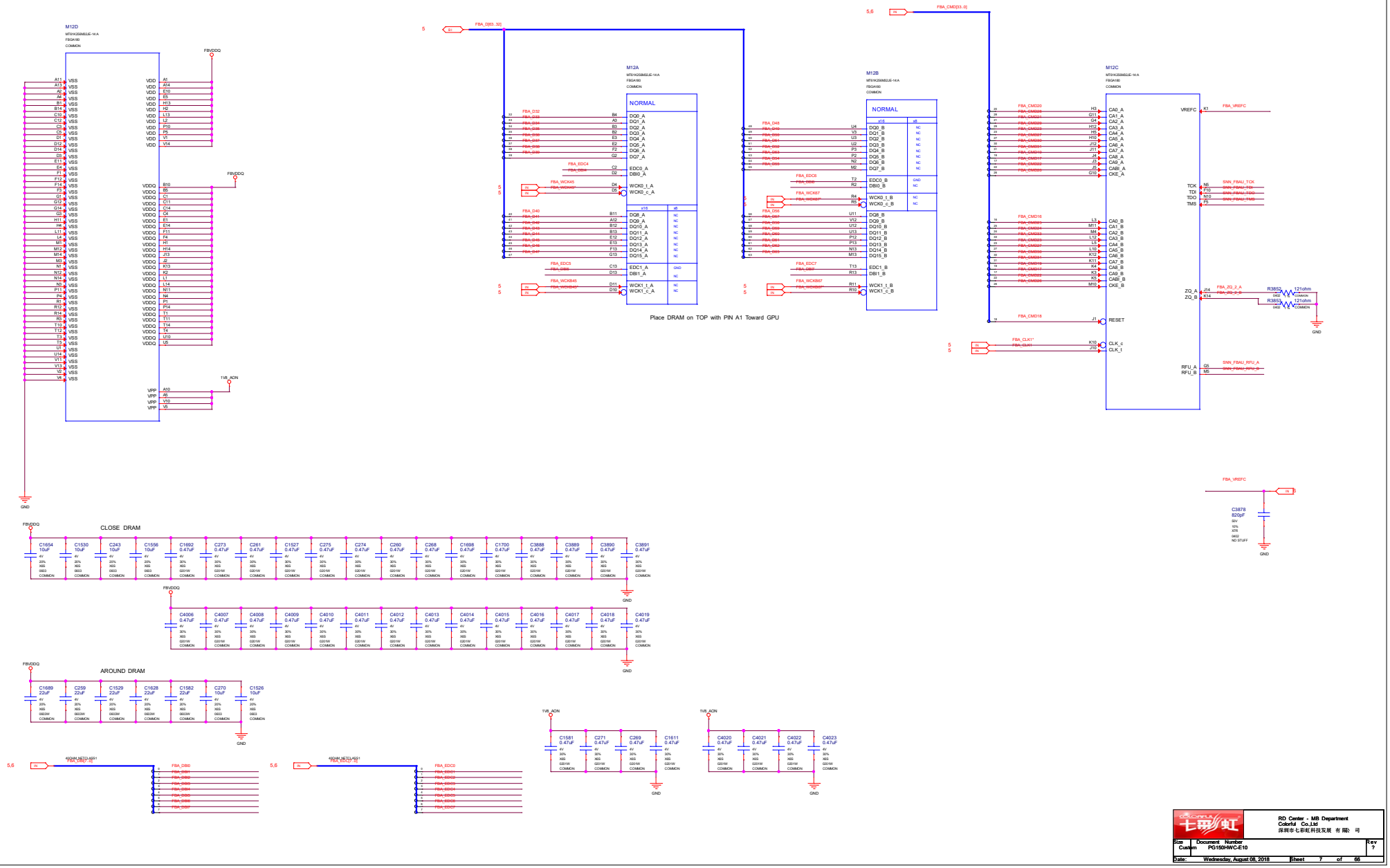
MEMORY: FBA Partition 63..32



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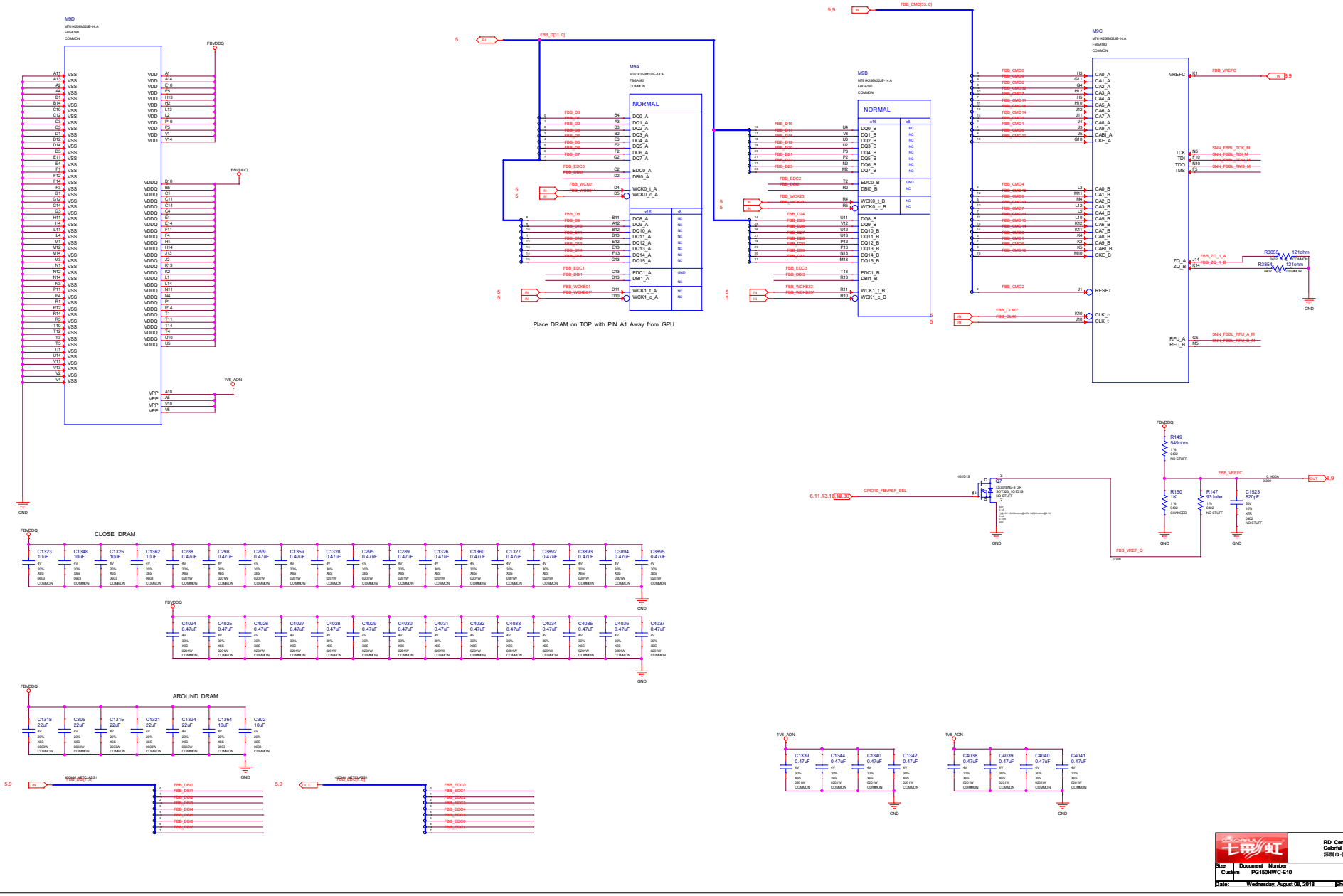

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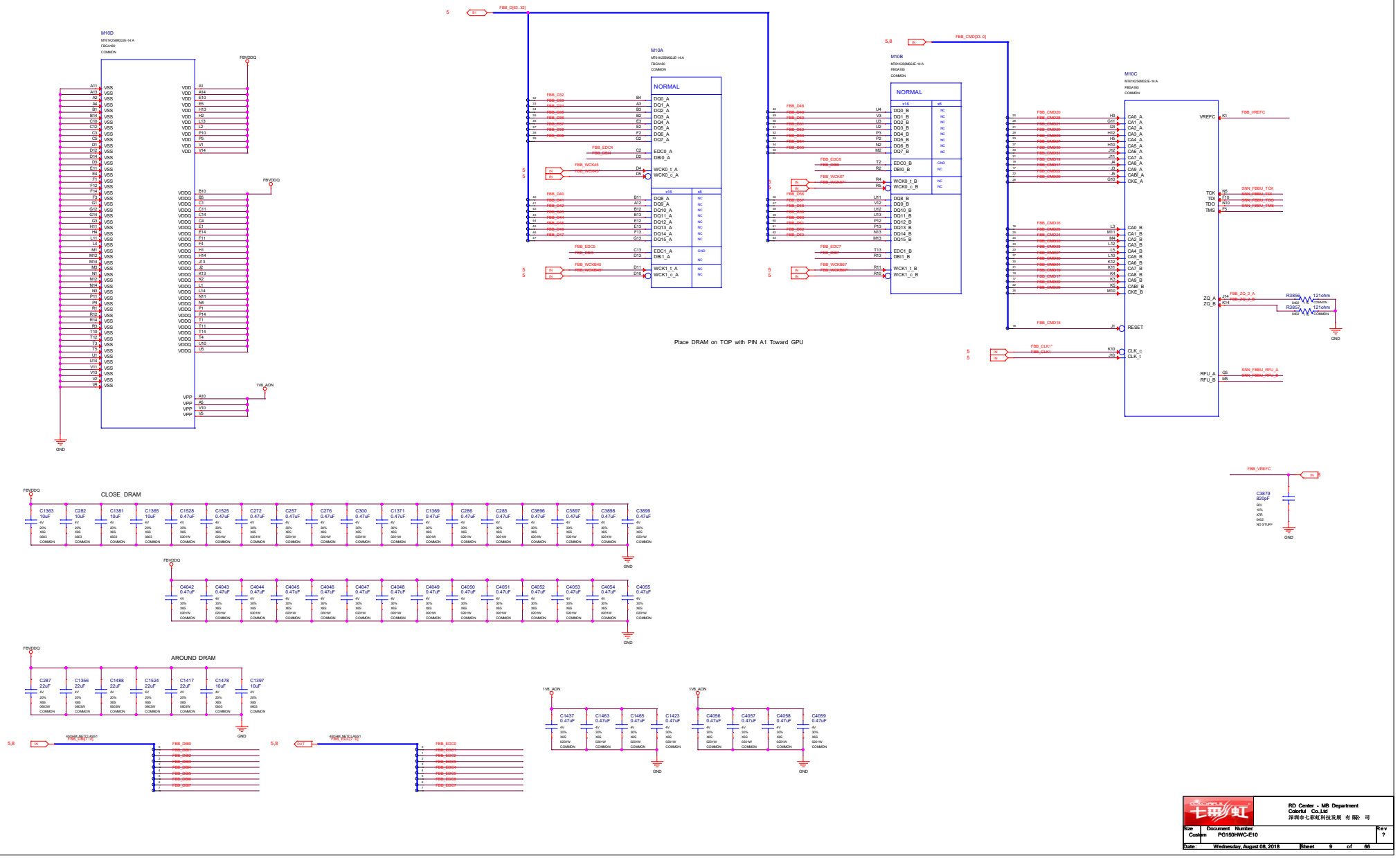
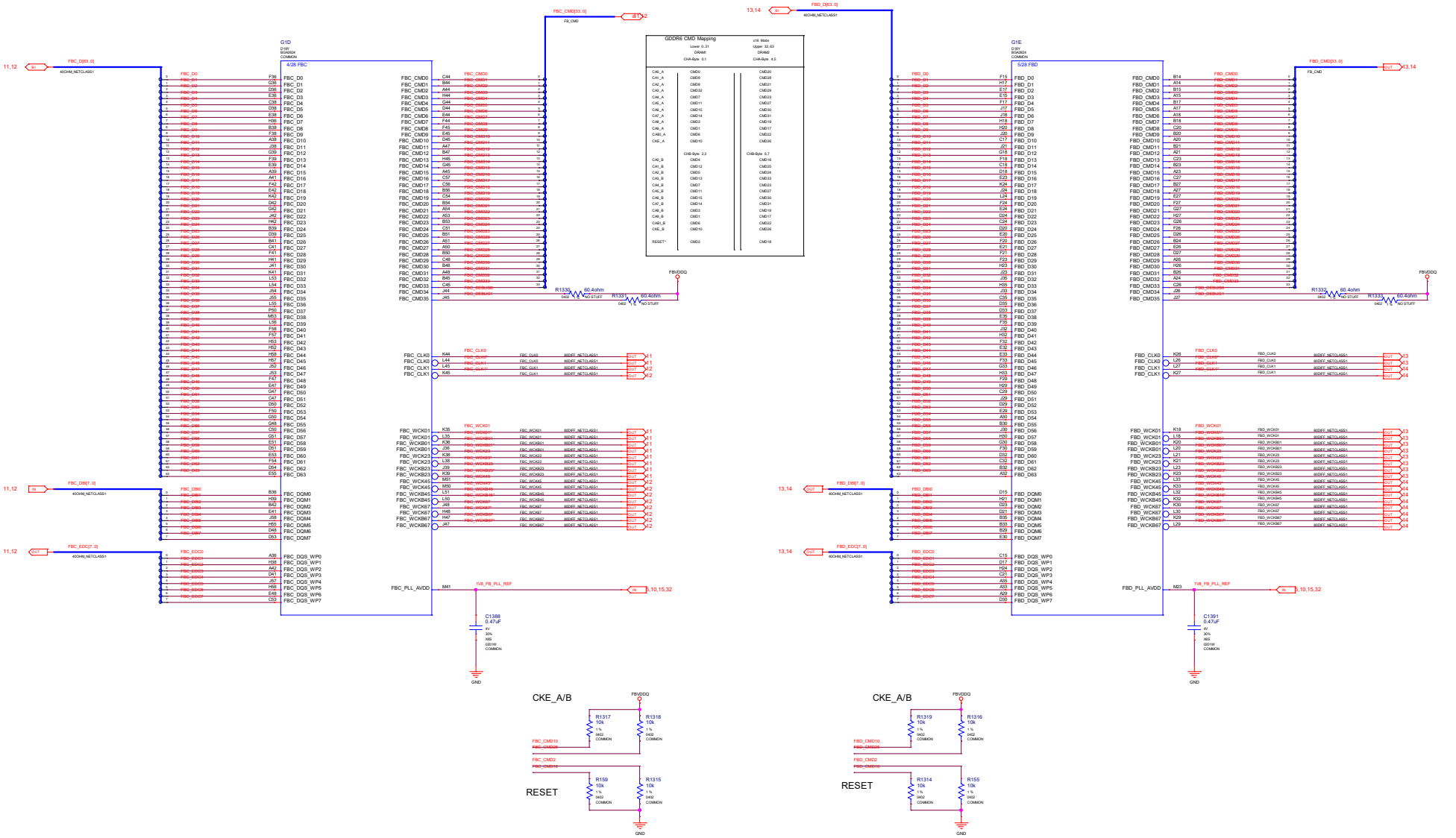
MEMORY: FBB Partition 63..32



MEMORY: GPU Partition C/D



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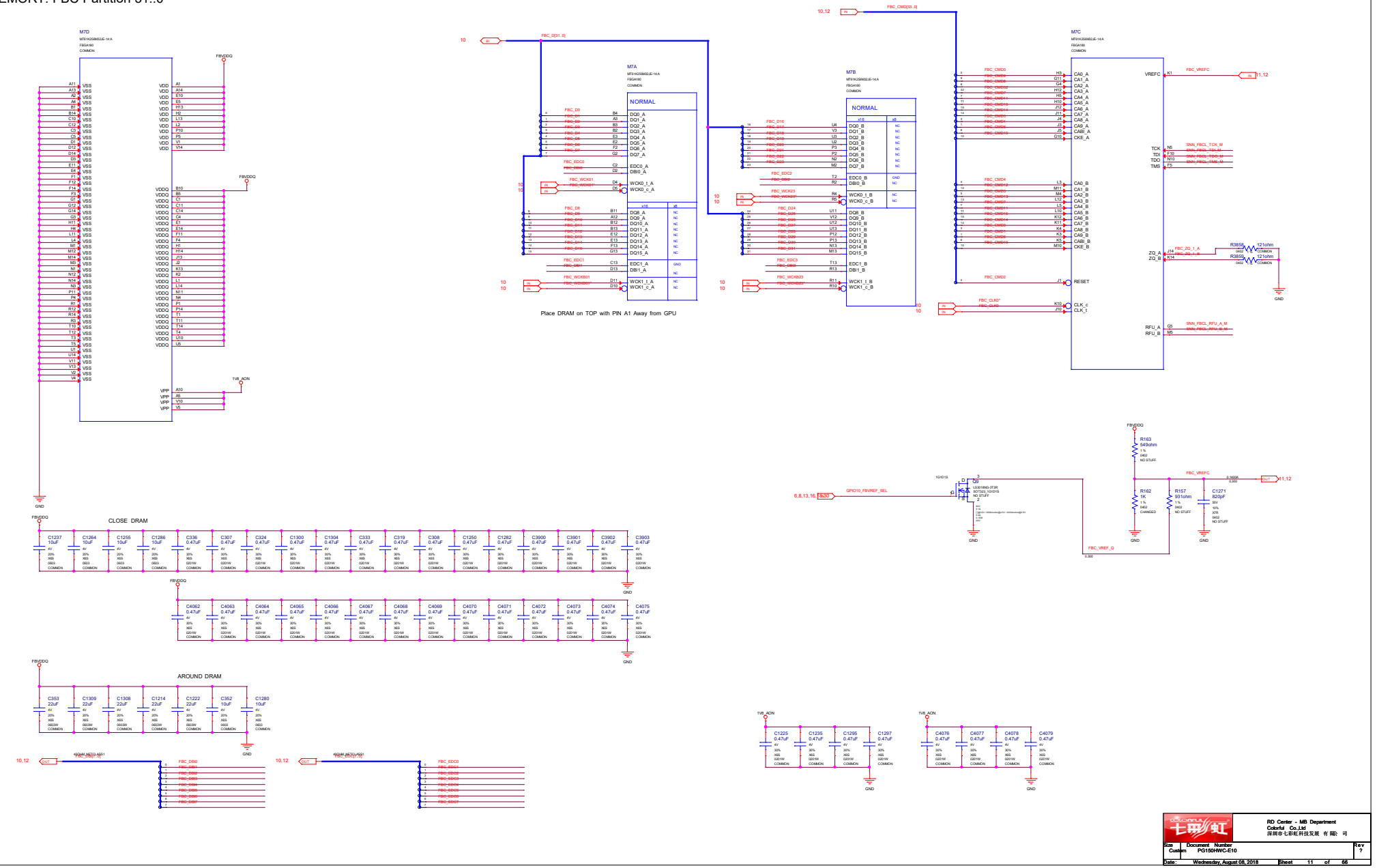
MEMORY: FBC Partition 31..0



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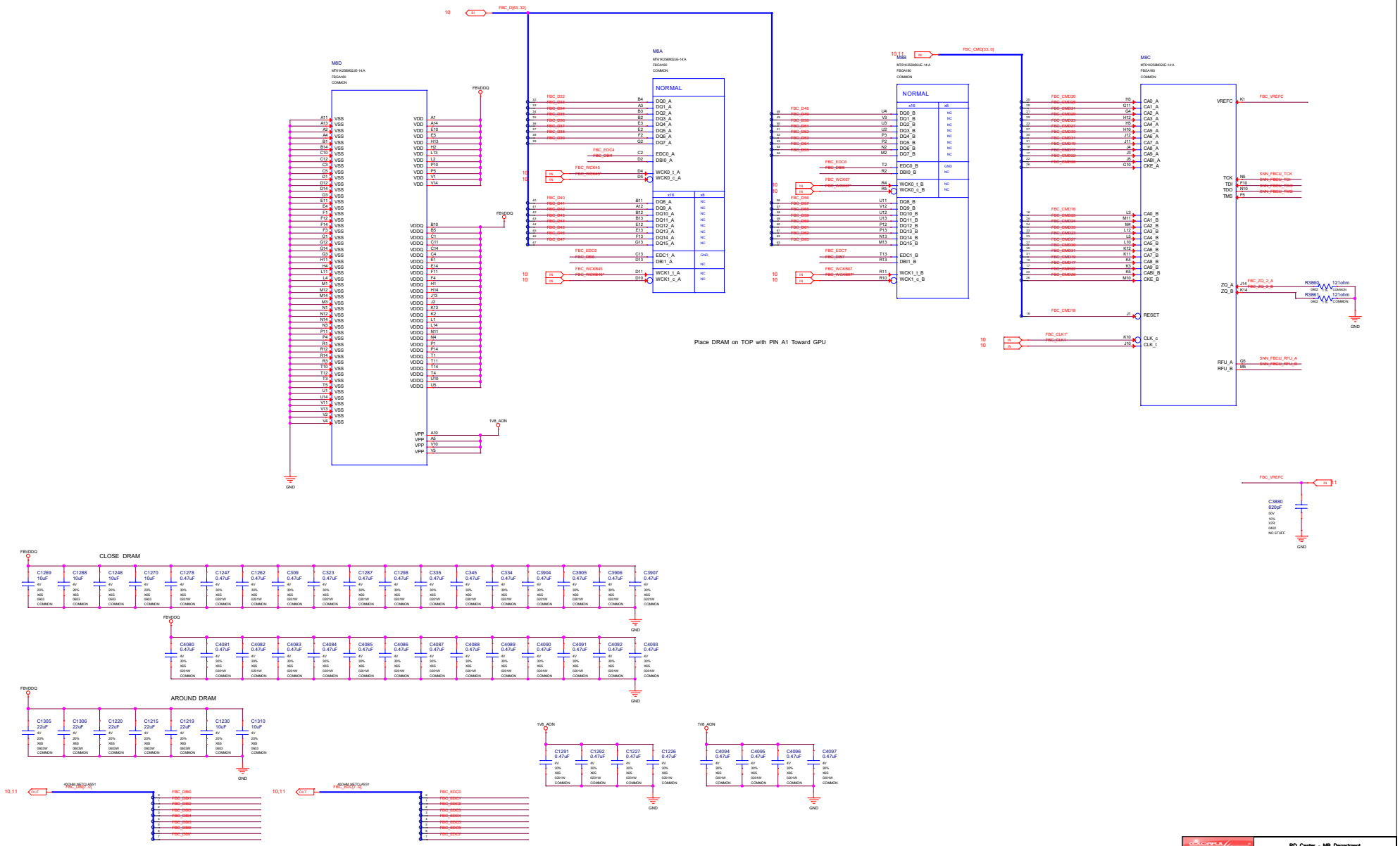

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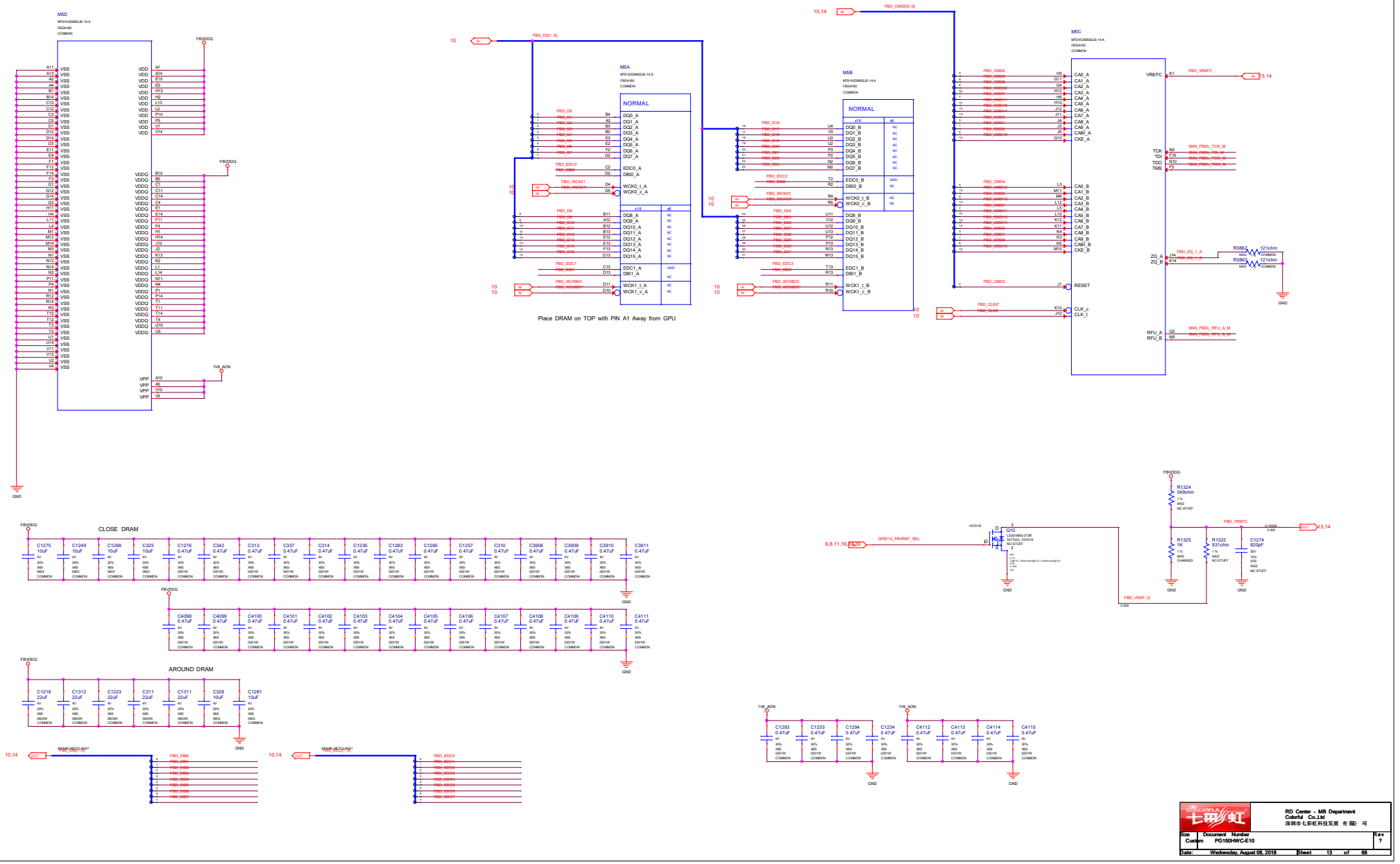
MEMORY: FBD Partition 31..0



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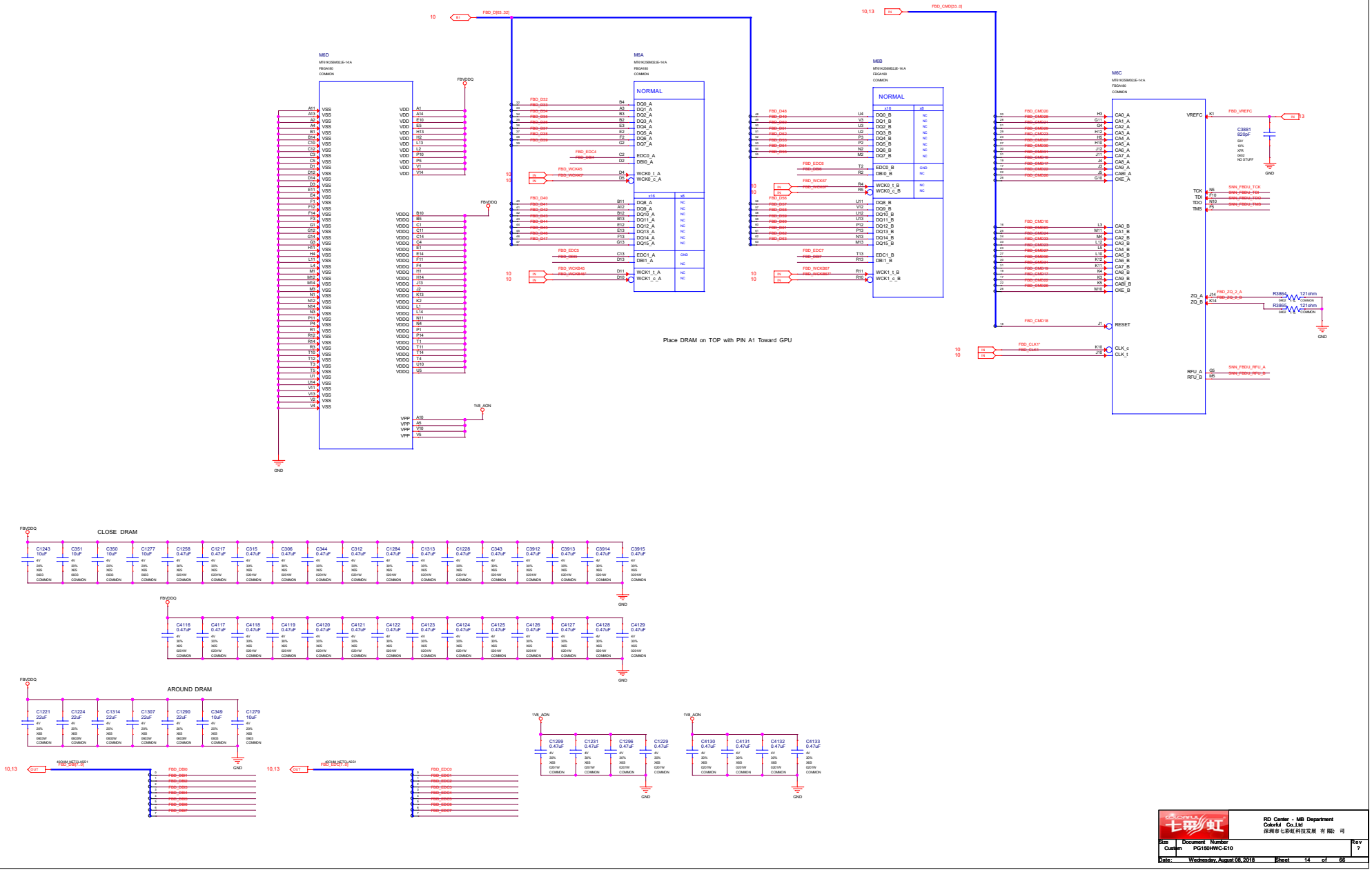
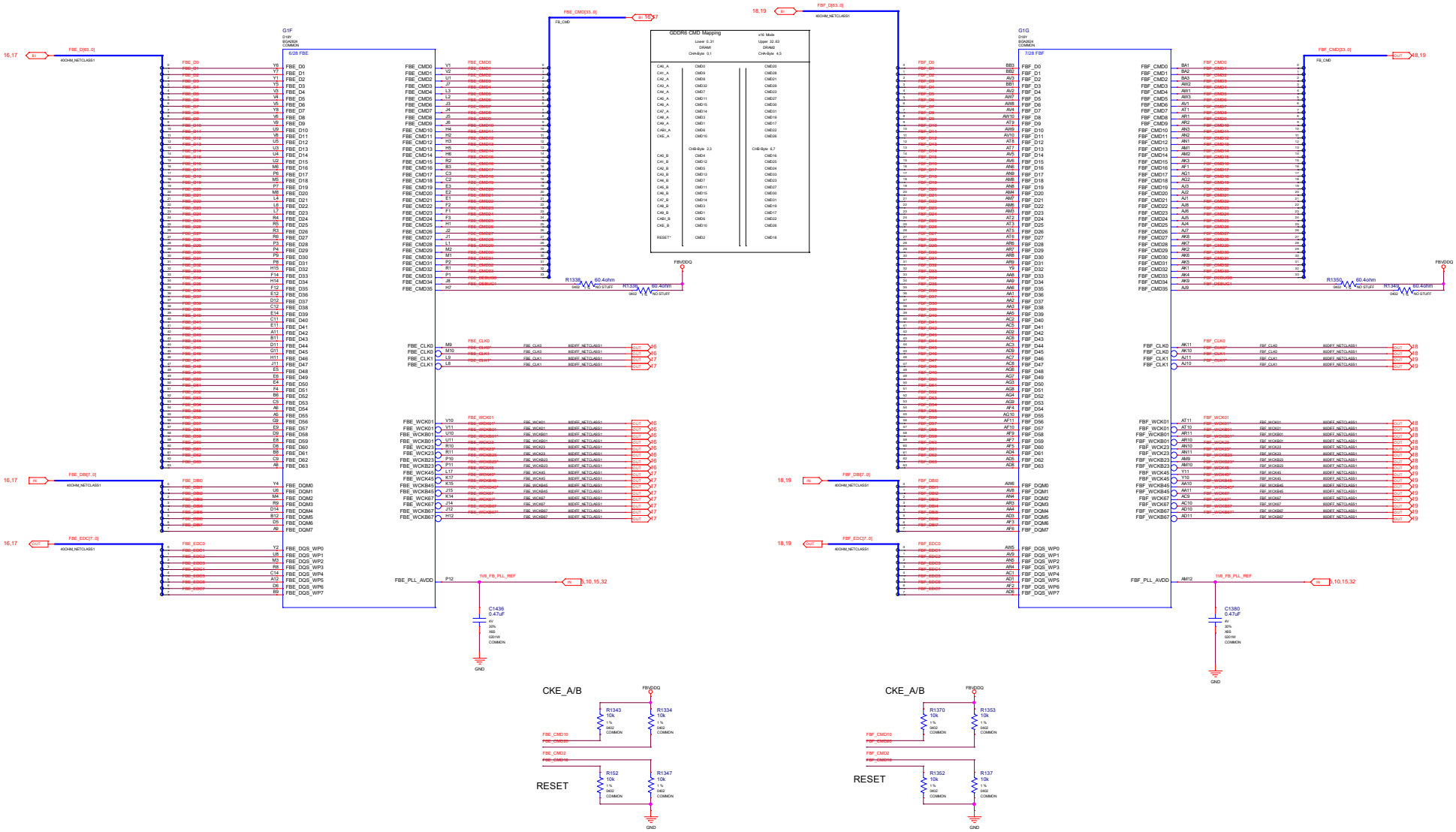
MEMORY: FBD Partition 63..32



MEMORY: GPU Partition E/F



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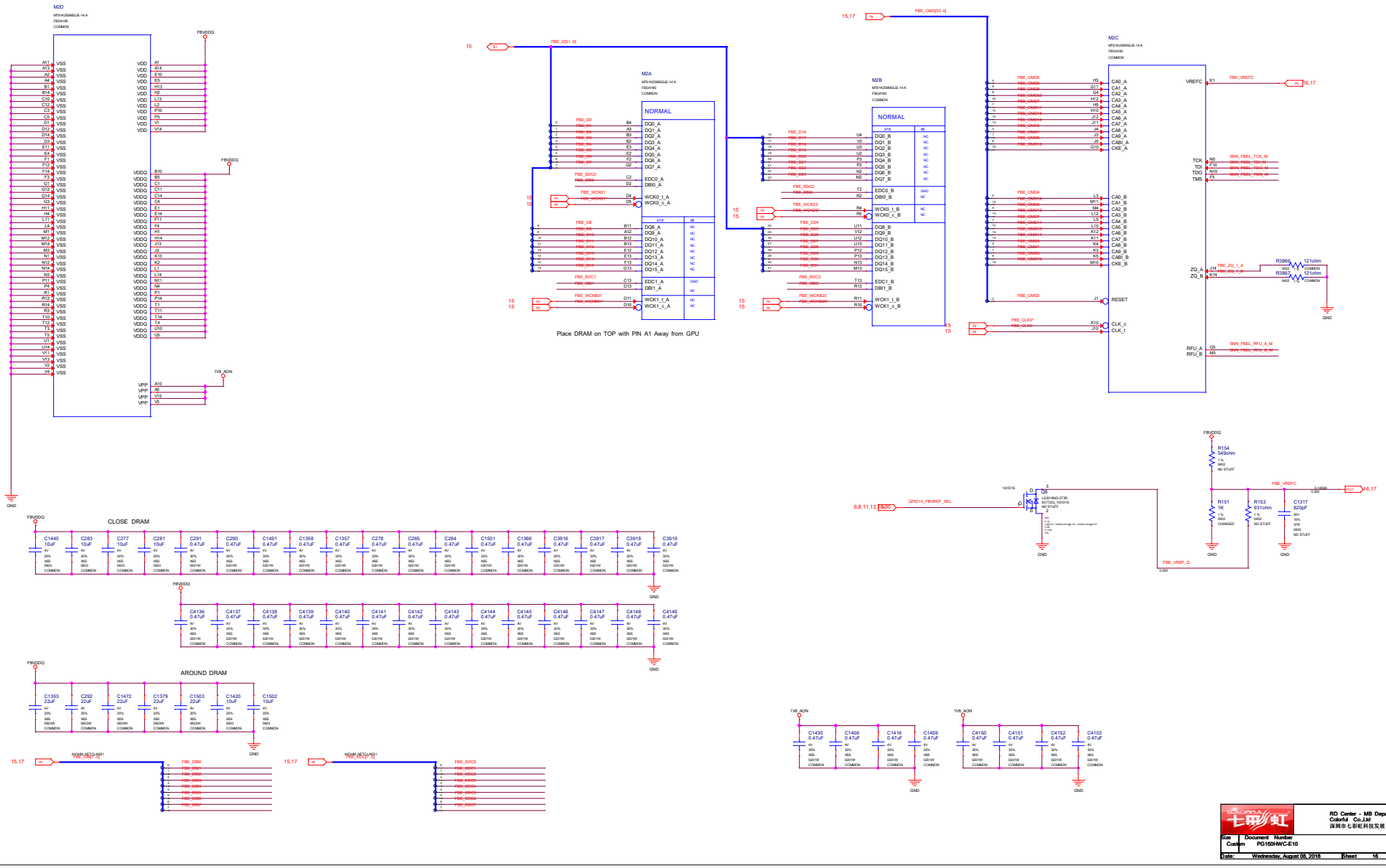
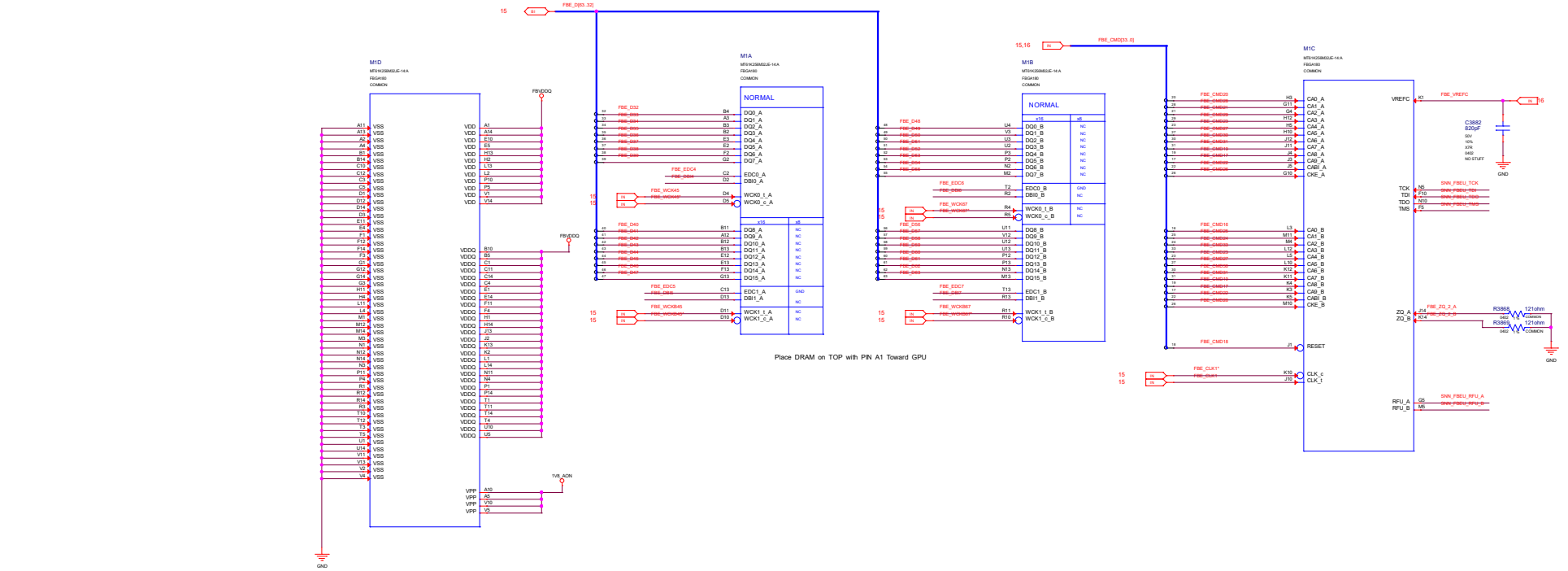
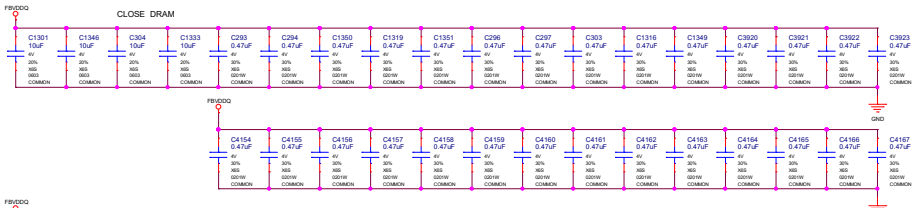
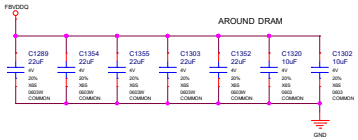
MEMORY: FBE Partition 31..0

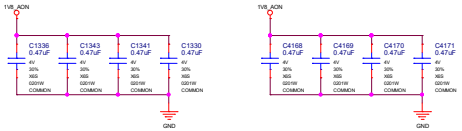


MEMORY: FBE Partition 63..32









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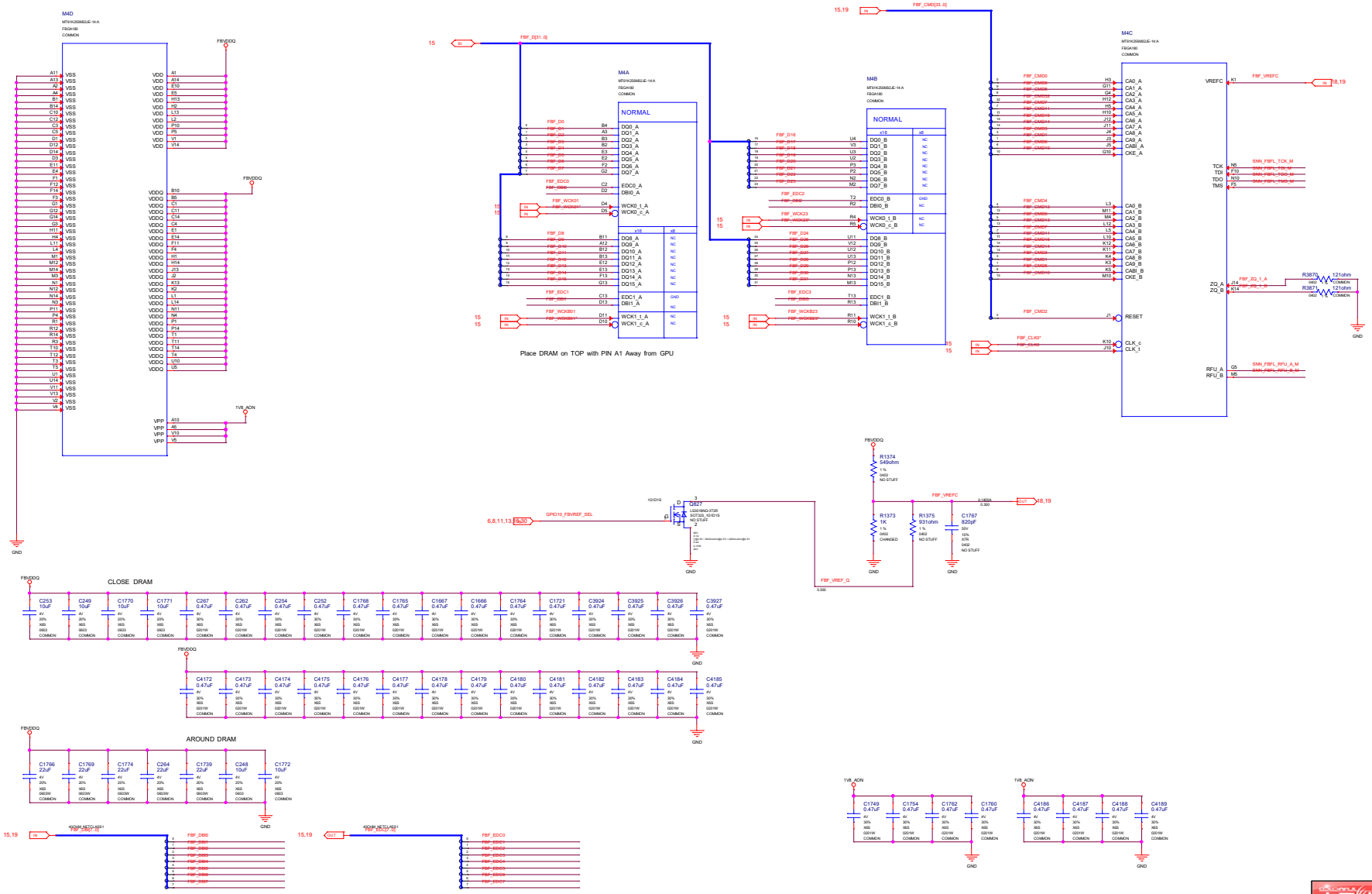
MEMORY: FBF Partition 31..0



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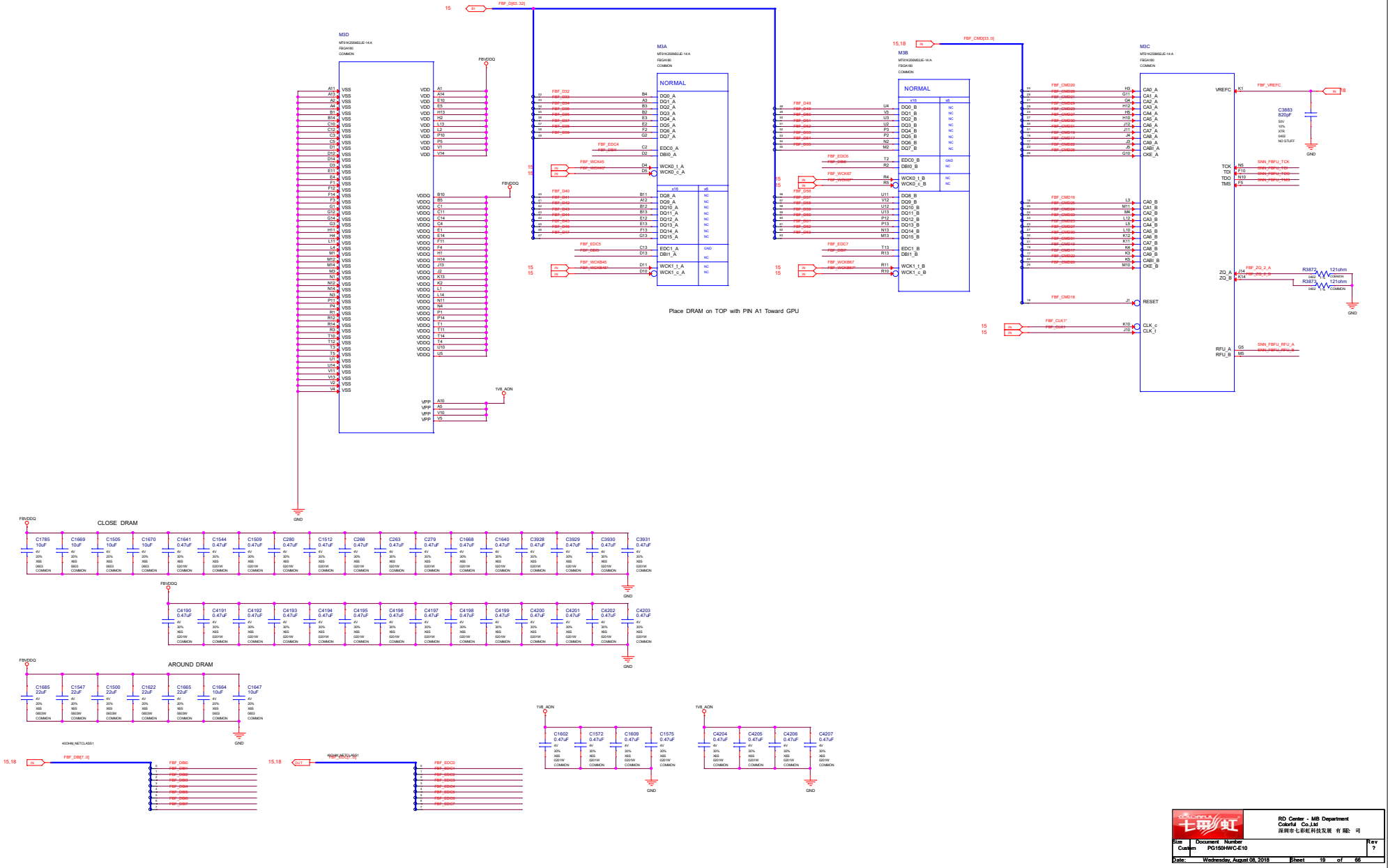
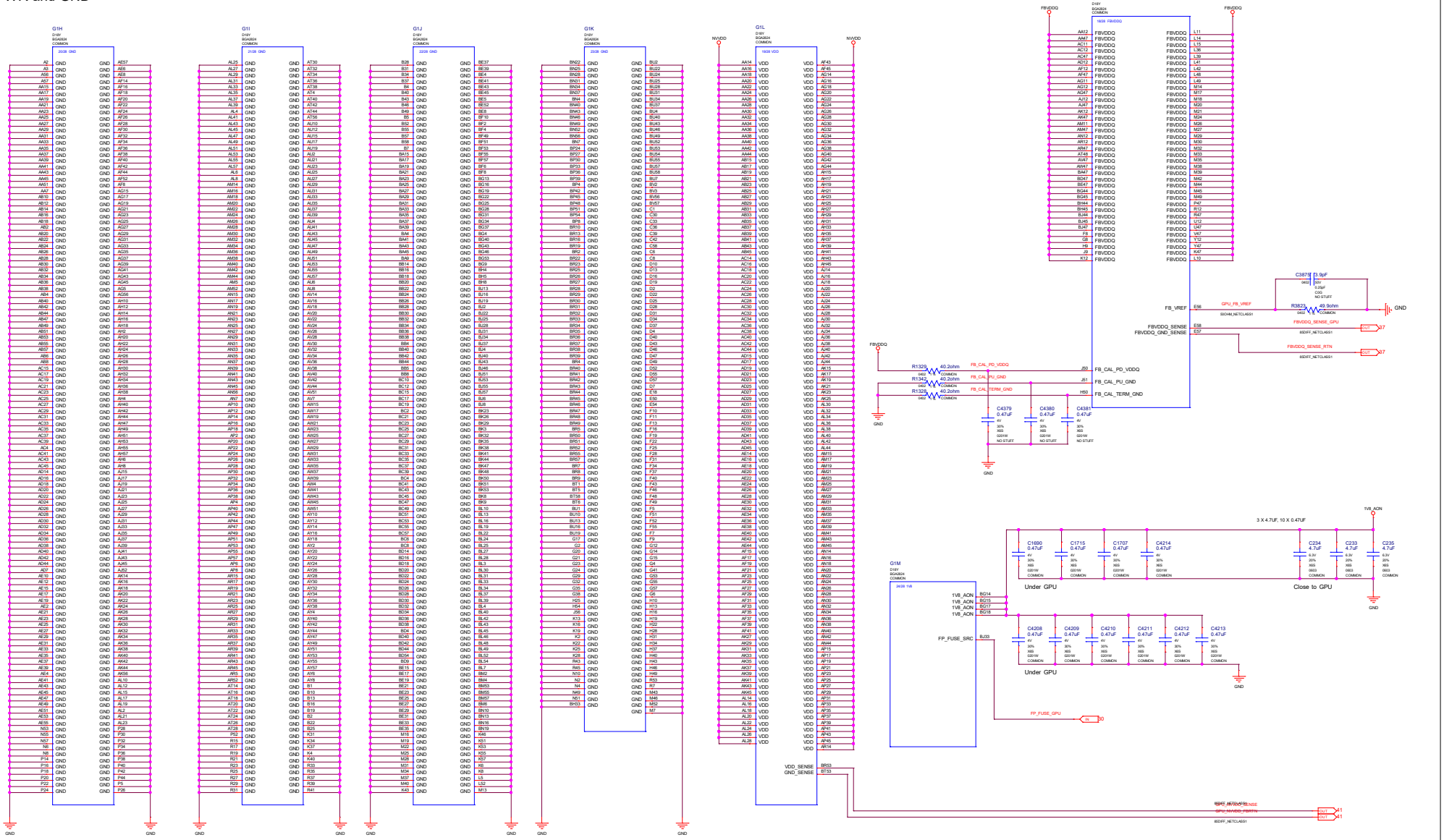
MEMORY: FBF Partition 63..32



GPU PWR and GND



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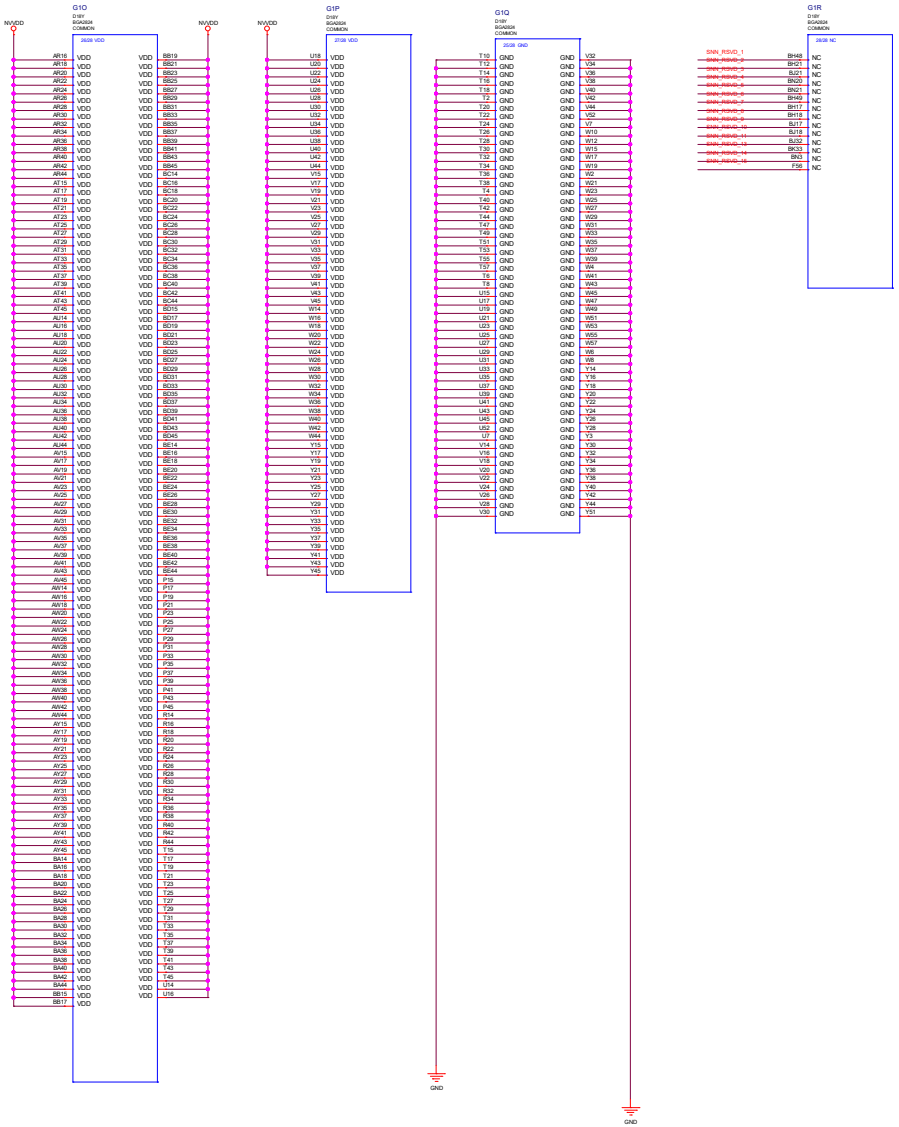
GPU PWR GND NCs



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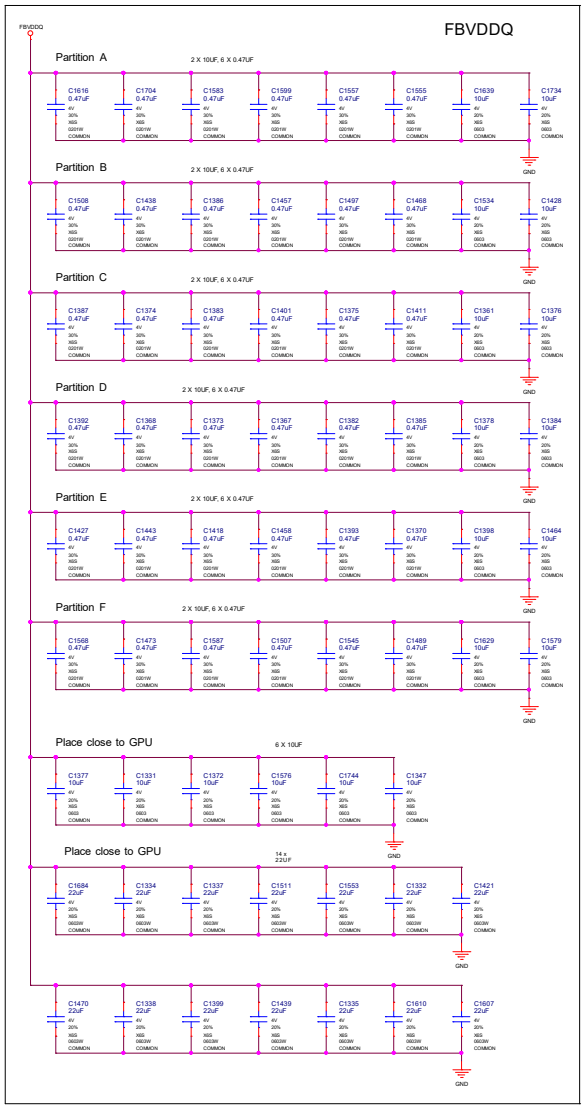
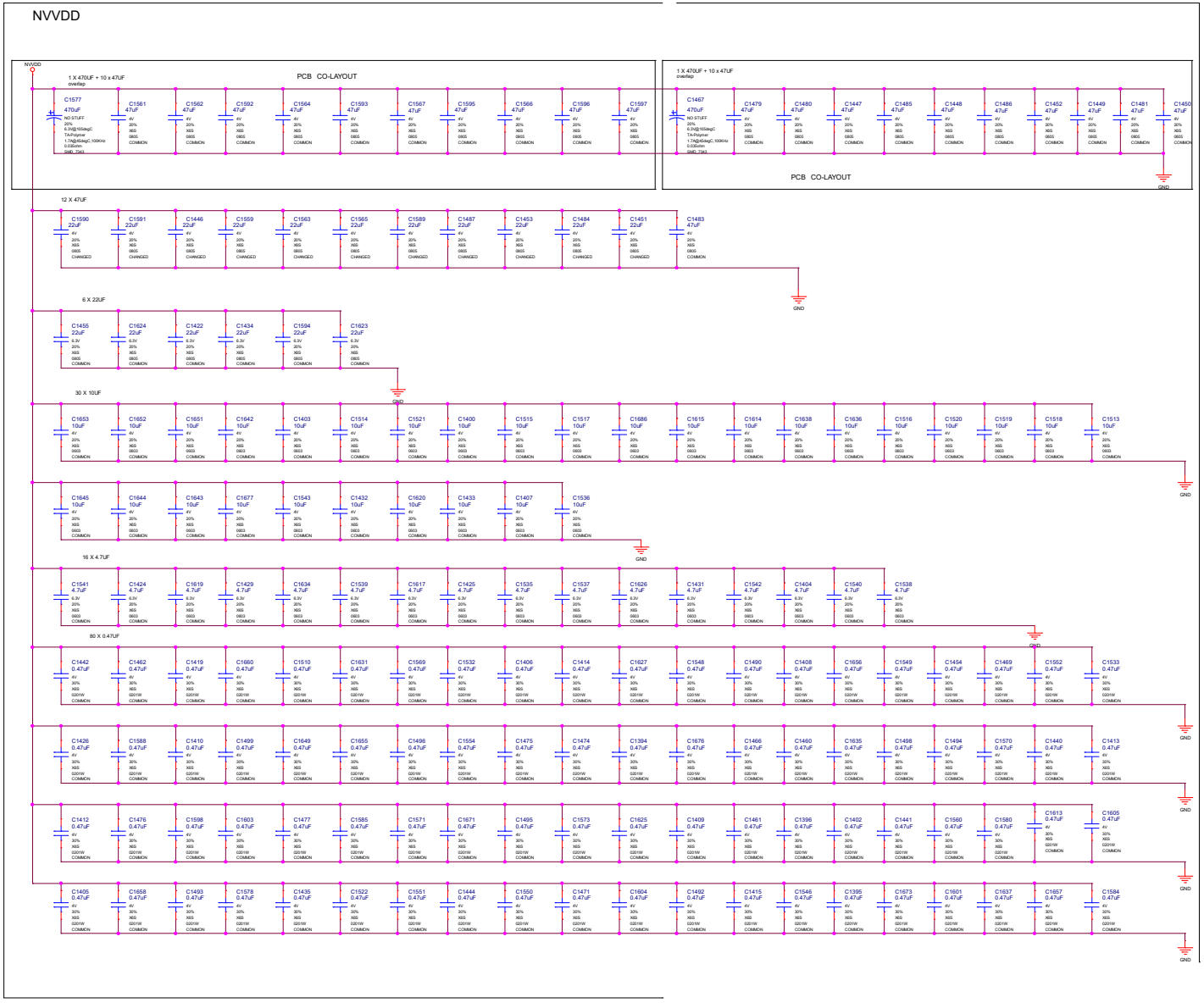
GPU Decoupling





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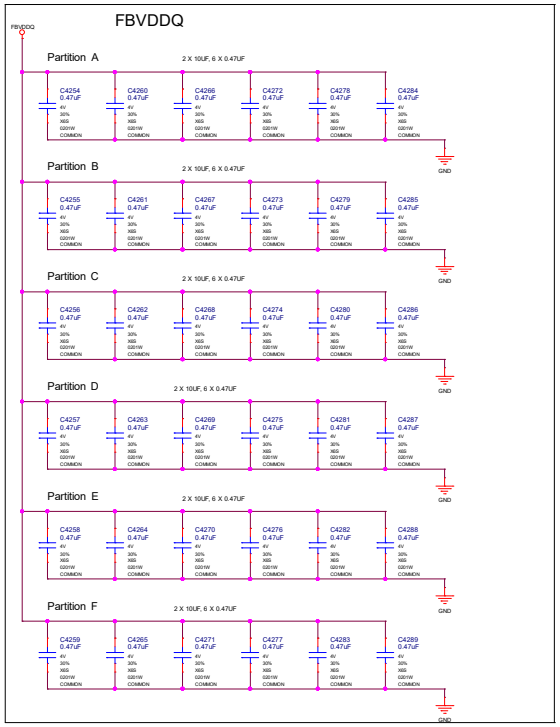
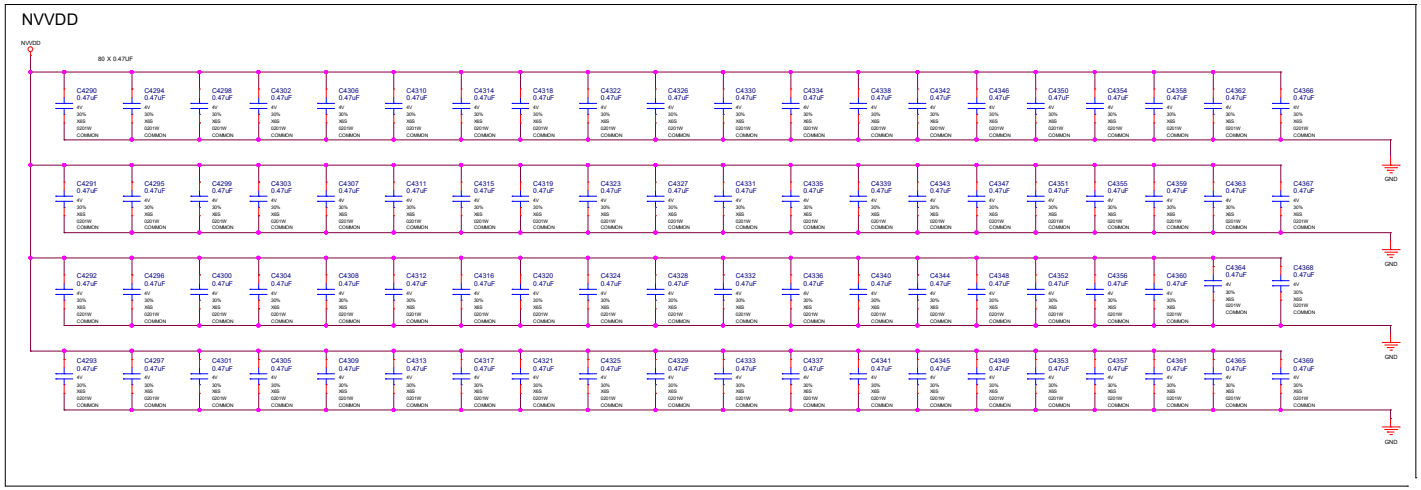
GPU Decoupling





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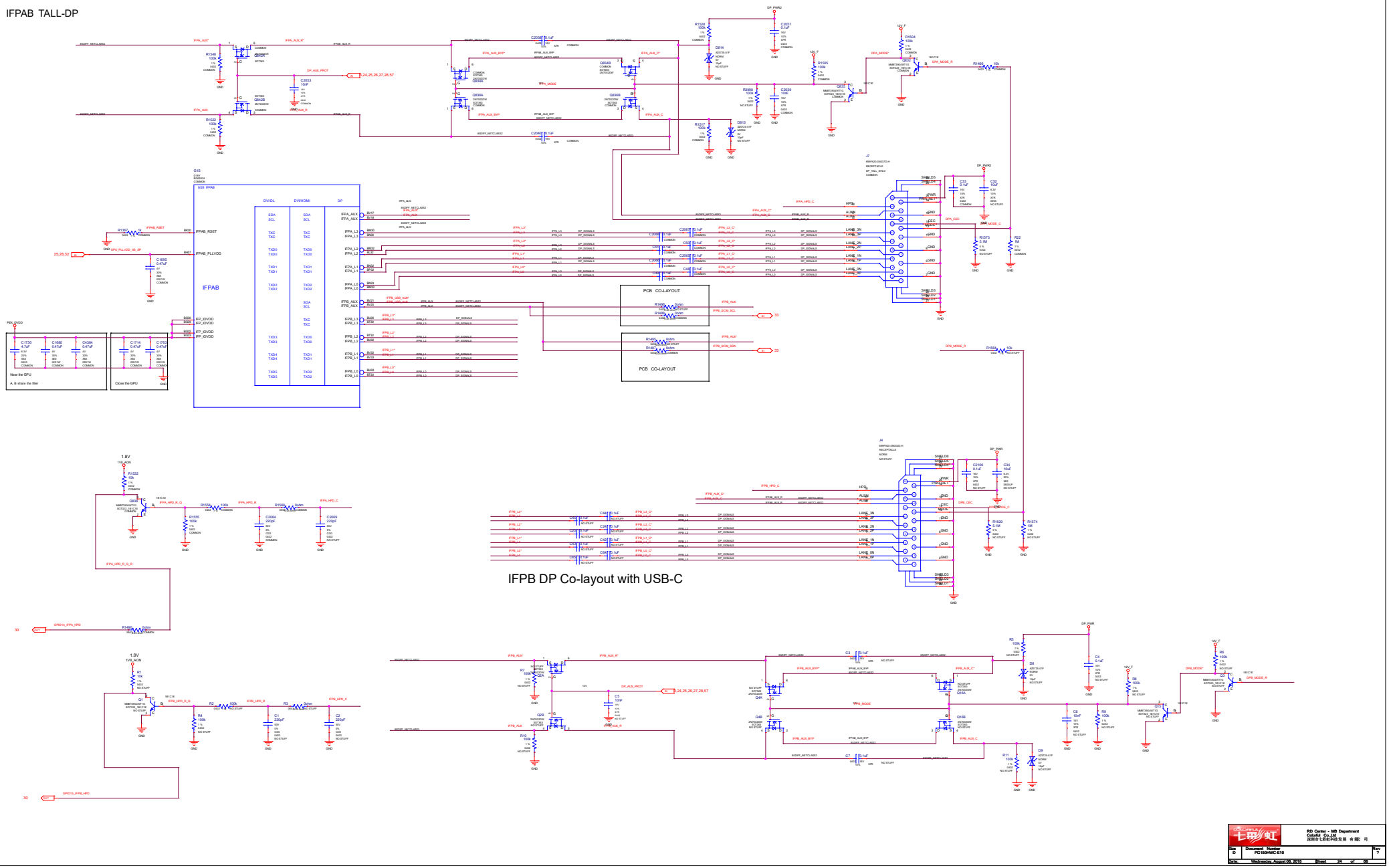
IFPAB TALL-DP



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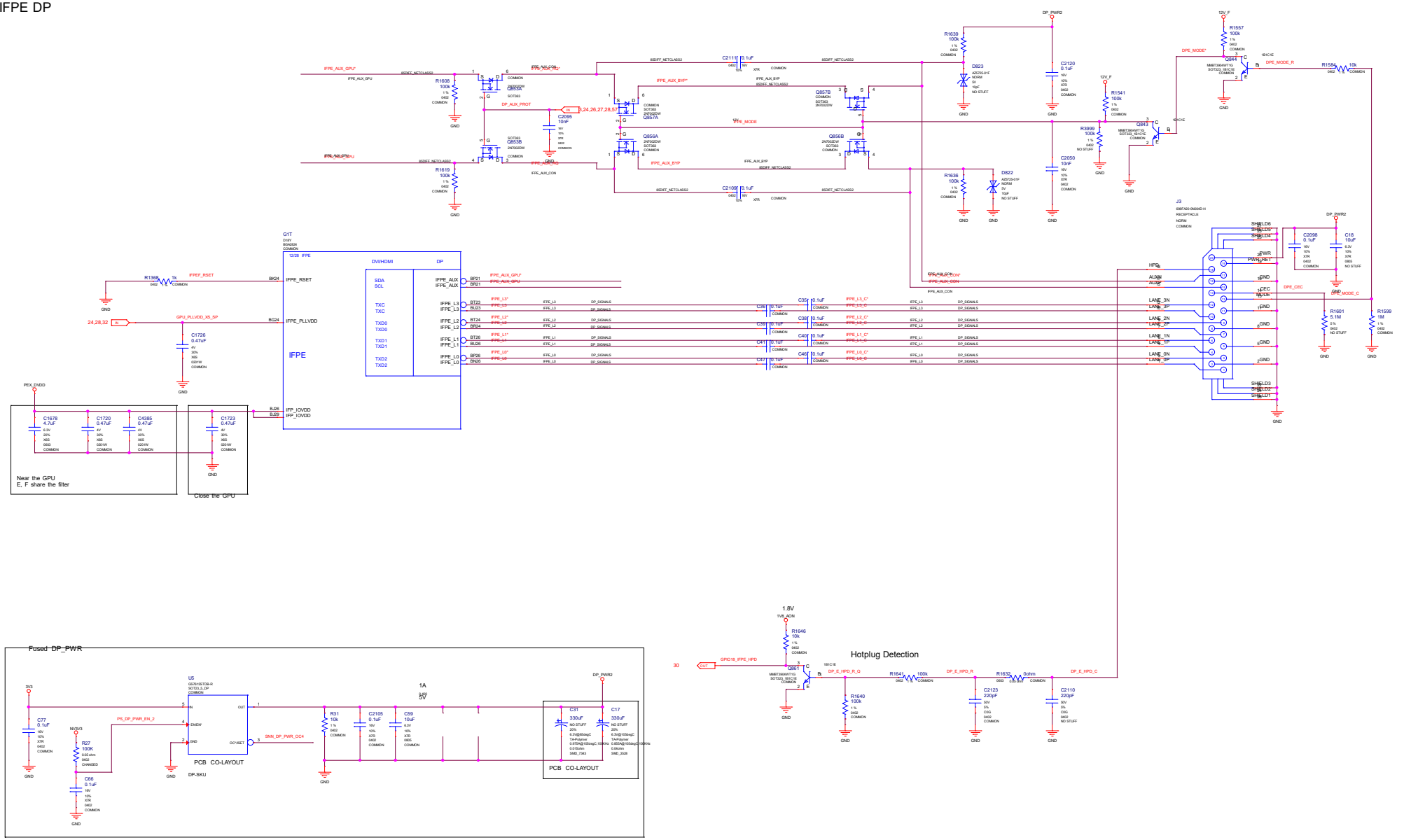
IFPE DP



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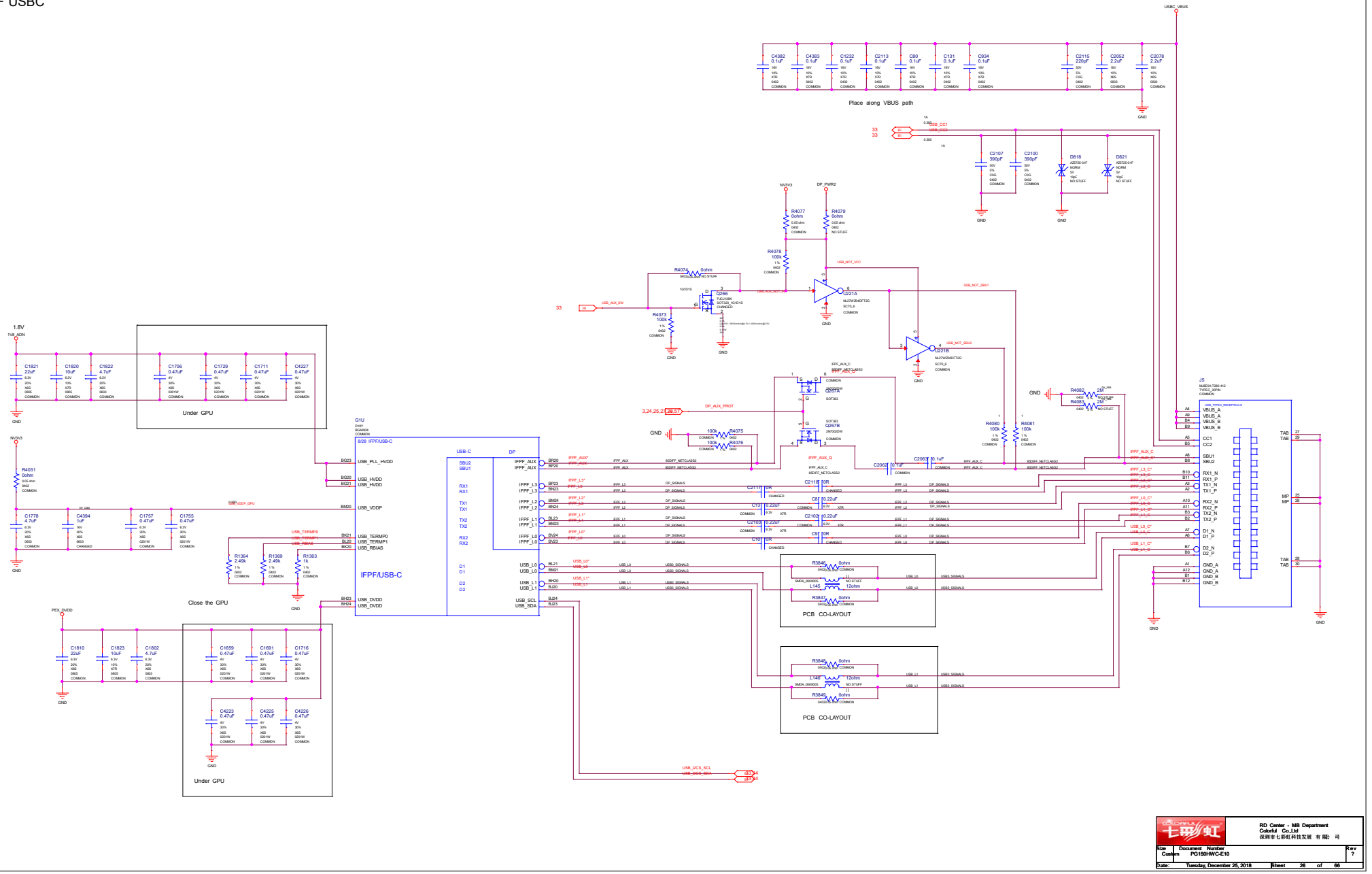
IFPF USBC


USBC_VBUS
Place along VBUS path
Under GPU
Close the GPU
Under GPU
IFPF/USB-C
PCB CO-LAYOUT
PCB CO-LAYOUT
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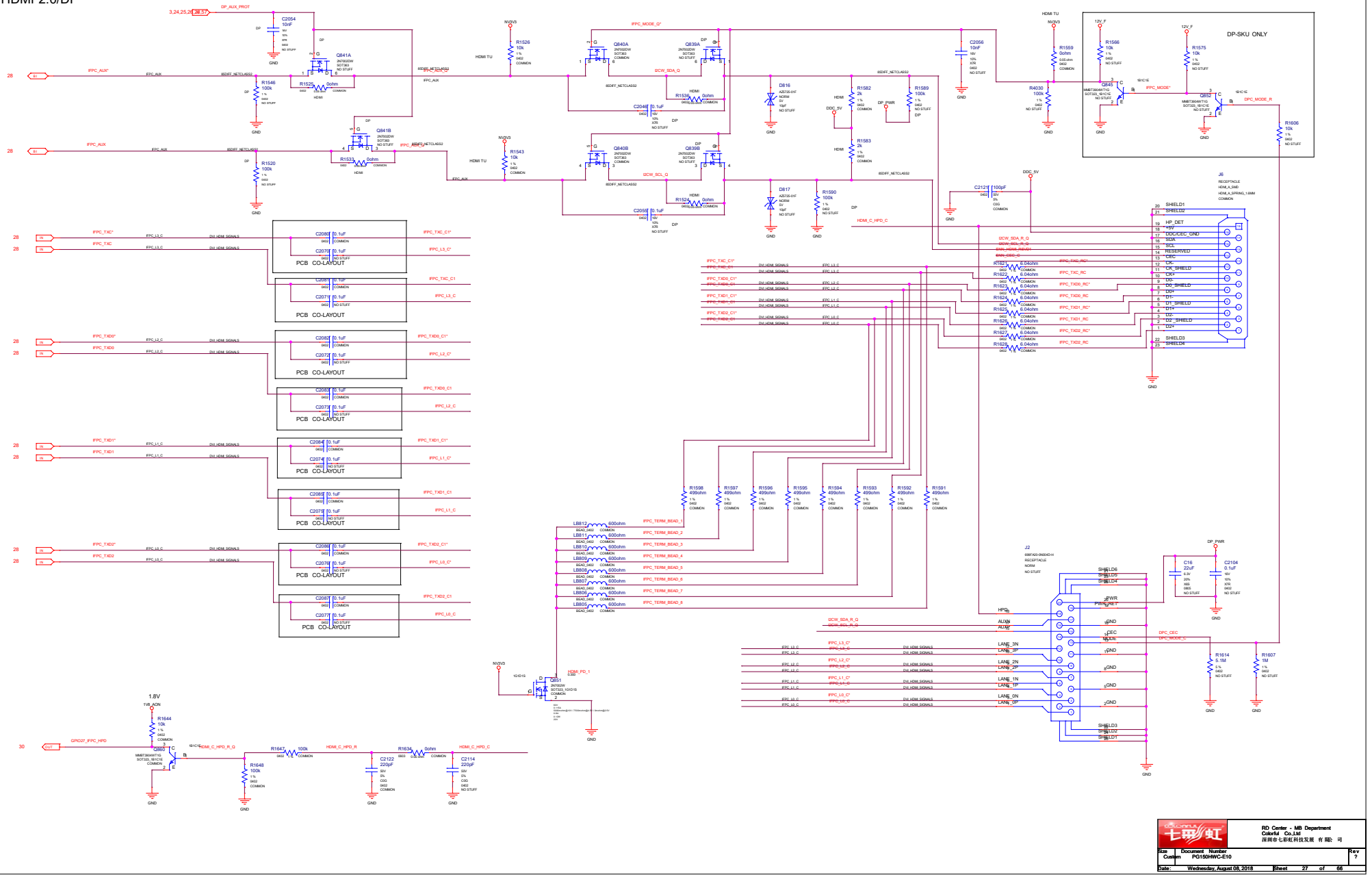
IFPC HDMI 2.0/DP



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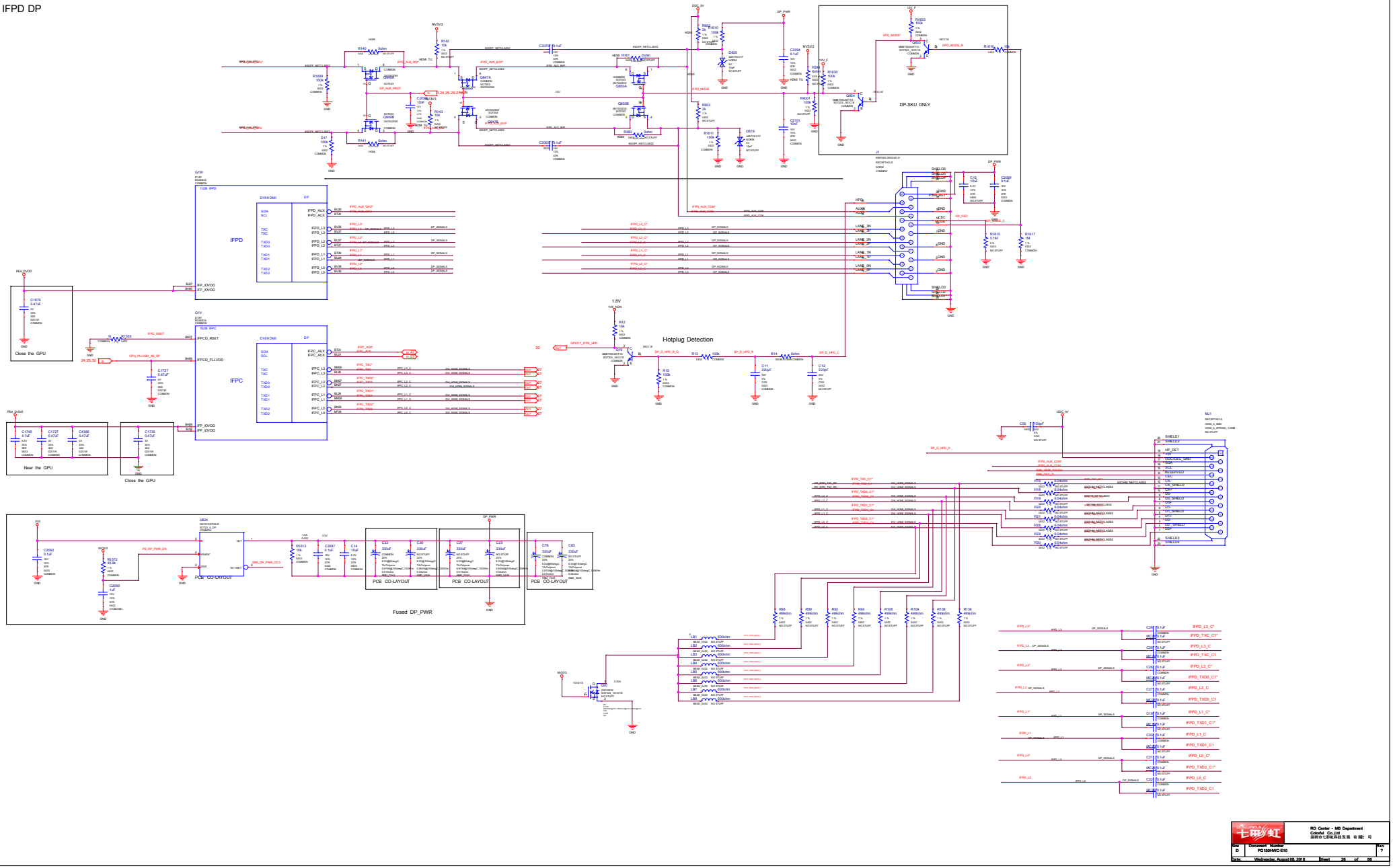
IFPD DP



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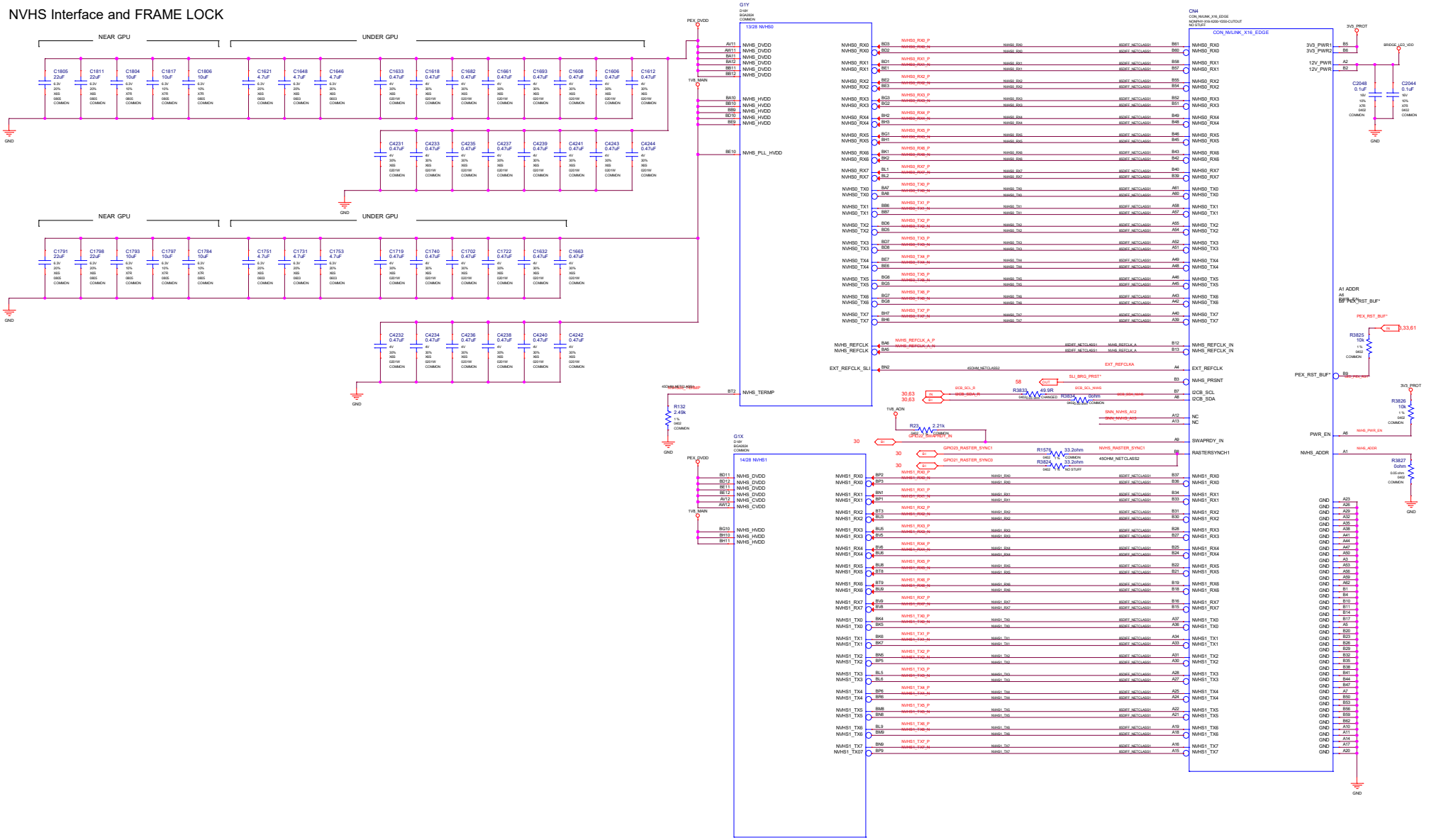
NVHS Interface and FRAME LOCK



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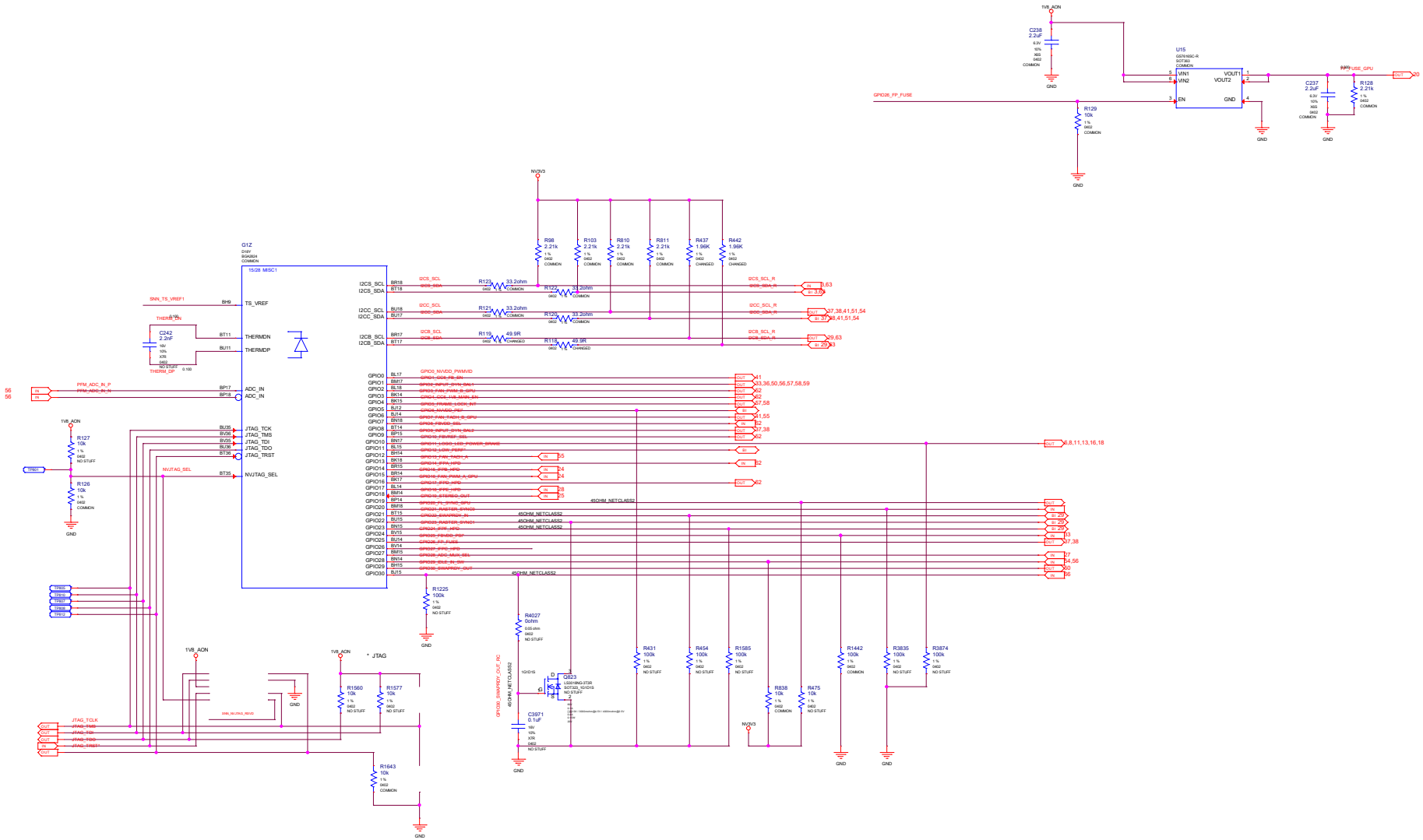
MISC1: Fan, Thermal, JTAG, GPIO, STEREO



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MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	
L	L	H	00001	DEFAULT
L	H	L	00010	
L	H	H	00011	
H	L	L	00100	
H	L	H	00101	
H	H	L	00110	
H	H	H	00111	
L	L	M	01000	
L	M	L	01001	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	H	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	SKU 200

H=High :Tied to 1.8V

M=Middle:Tied to 0.9V

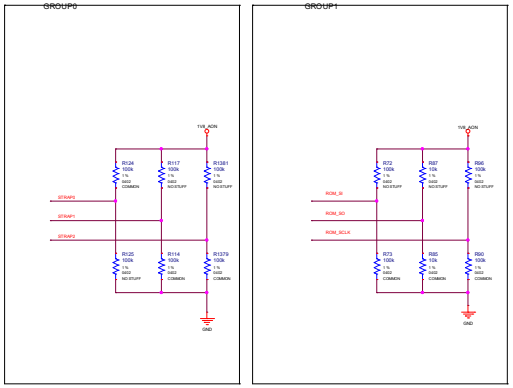
L=Low :Tied to 0V

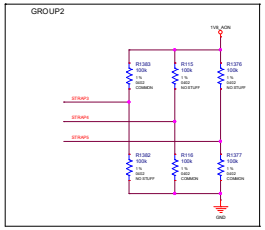
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

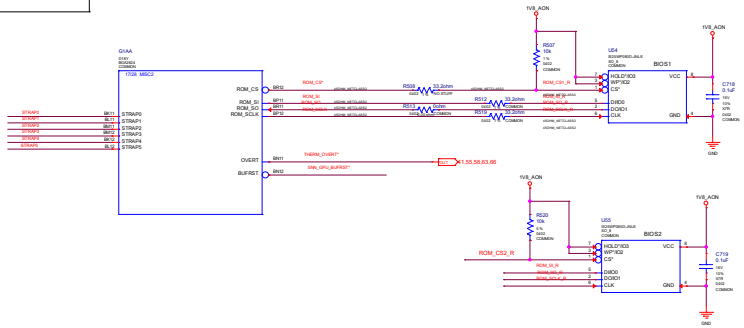
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

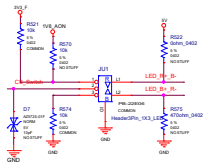
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

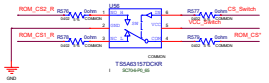




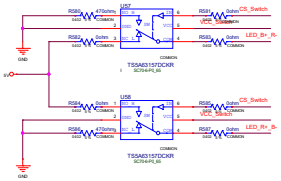




JU1复位 断 Pin(1 2) 到名 BI OS2 (选
JU1备份 断 Pin(2 3) 到名 BI OS1 (选



IN	NC TO COM,COM TO NC	NO TO COM,COM TO NO
L	ON	OFF
H	OFF	ON



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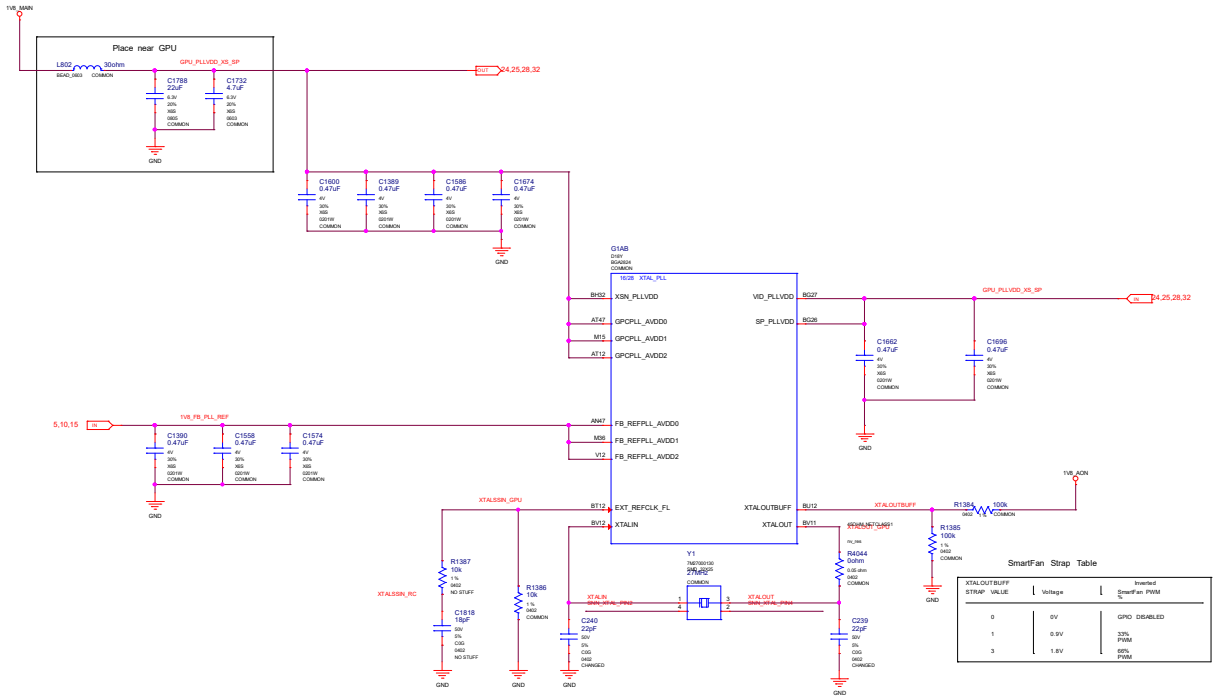

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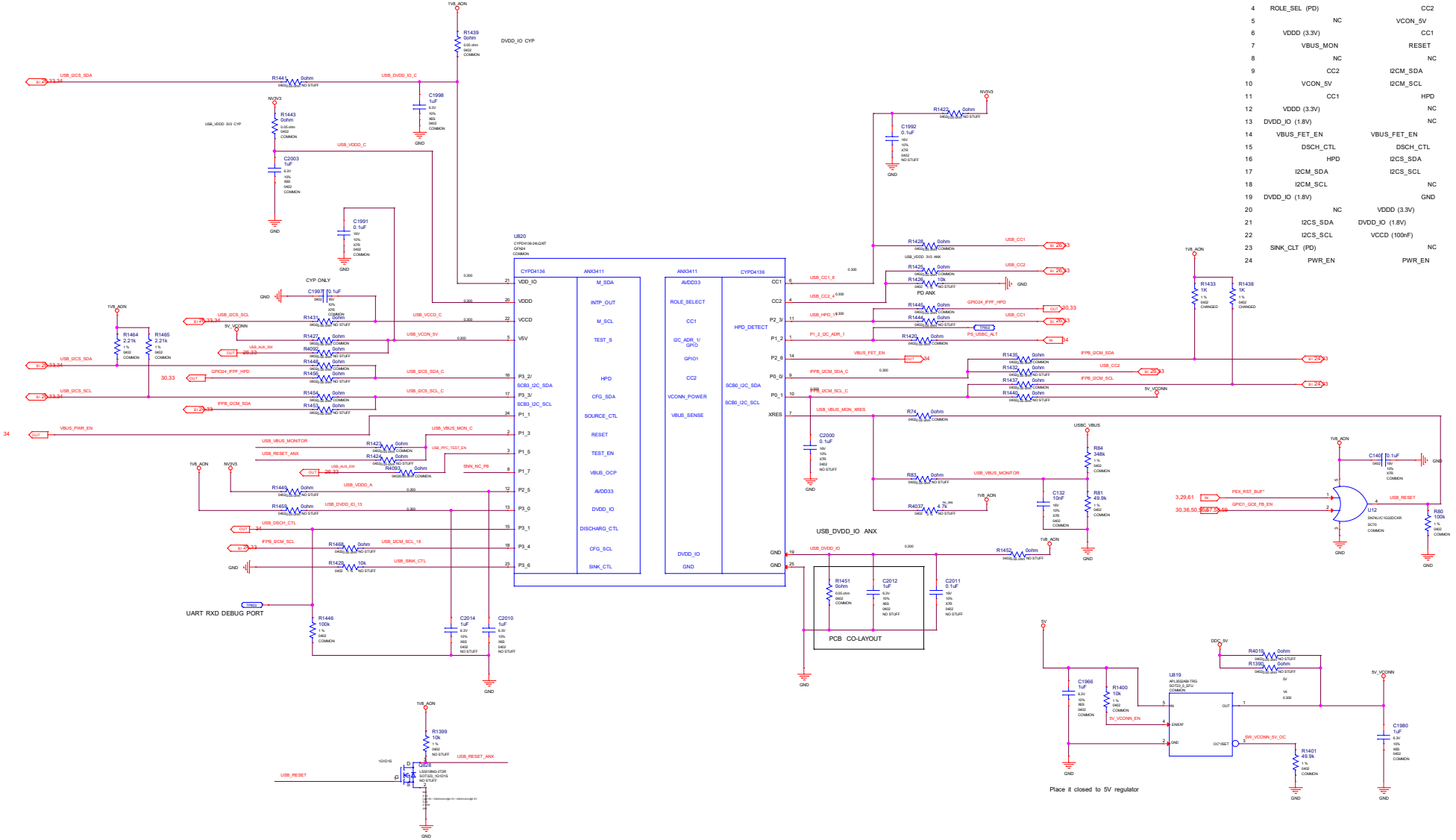
MISC: USB PPC


PIN ANX CYP
1 TP TP
2 RESET VBUS_MON
3 NC NC
4 ROLE_SEL (PD) CC2
5 NC VCON_5V
6 VDDD (3.3V) CC1
7 VBUS_MON RESET
8 NC NC
9 CC2 I2CM_SDA
10 VCON_5V I2CM_SCL
11 CC1 HPD
12 VDDD (3.3V) NC
13 DVDD_IO (1.8V) NC
14 VBUS_FET_EN VBUS_FET_EN
15 DSCH_CTL DSCH_CTL
16 HPD I2CS_SDA
17 I2CM_SDA I2CS_SCL
18 I2CM_SCL NC
19 DVDD_IO (1.8V) GND
20 NC VDDD (3.3V)
21 I2CS_SDA DVDD_IO (1.8V)
22 I2CS_SCL VCCD (100nF)
23 SINK_CLT (PD) NC
24 PWR_EN PWR_EN
U820
CYPD4136-24LQXIT
QFN24
COMMON
CYPD4136
ANX3411
CYPD4136
VDD_IO
VDDD
VCCD
V5V
P3_2/ SCB3_I2C_SDA
P3_3/ SCB3_I2C_SCL
P1_1
P1_3
P1_5
P1_7
P2_5
P3_0
P3_1
P3_4
P3_6
M_SDA
INTP_OUT
M_SCL
TEST_S
HPD
CFG_SDA
SOURCE_CTL
RESET
TEST_EN
VBUS_OCP
AVDD33
DVDD_IO
DISCHARG_CTL
CFG_SCL
SINK_CTL
AVDD33
ROLE_SELECT
CC1
I2C_ADR_1/ GPIO
GPIO1
CC2
VCONN_POWER
VBUS_SENSE
DVDD_IO
GND
SCB0_I2C_SDA
SCB0_I2C_SCL
CC1
CC2
P2_3/
HPD_DETECT
P1_2
P2_6
P0_0/
P0_1
XRES
GND
GND
USB_DVDD_IO ANX
PCB CO-LAYOUT
UART RXD DEBUG PORT
CYP ONLY
Place it closed to 5V regulator
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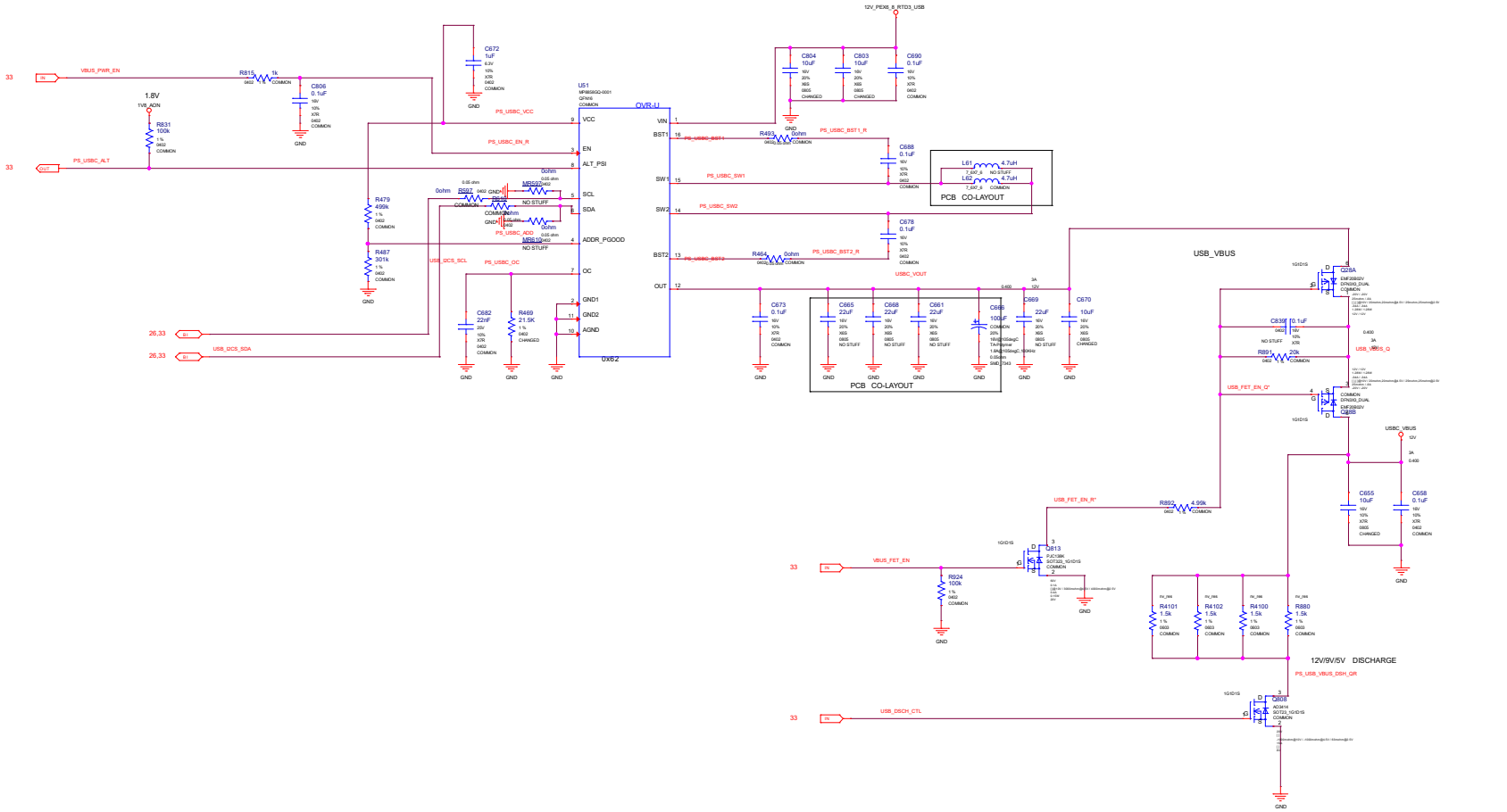
PS: USB VR

MP8858/uP9629 P2P



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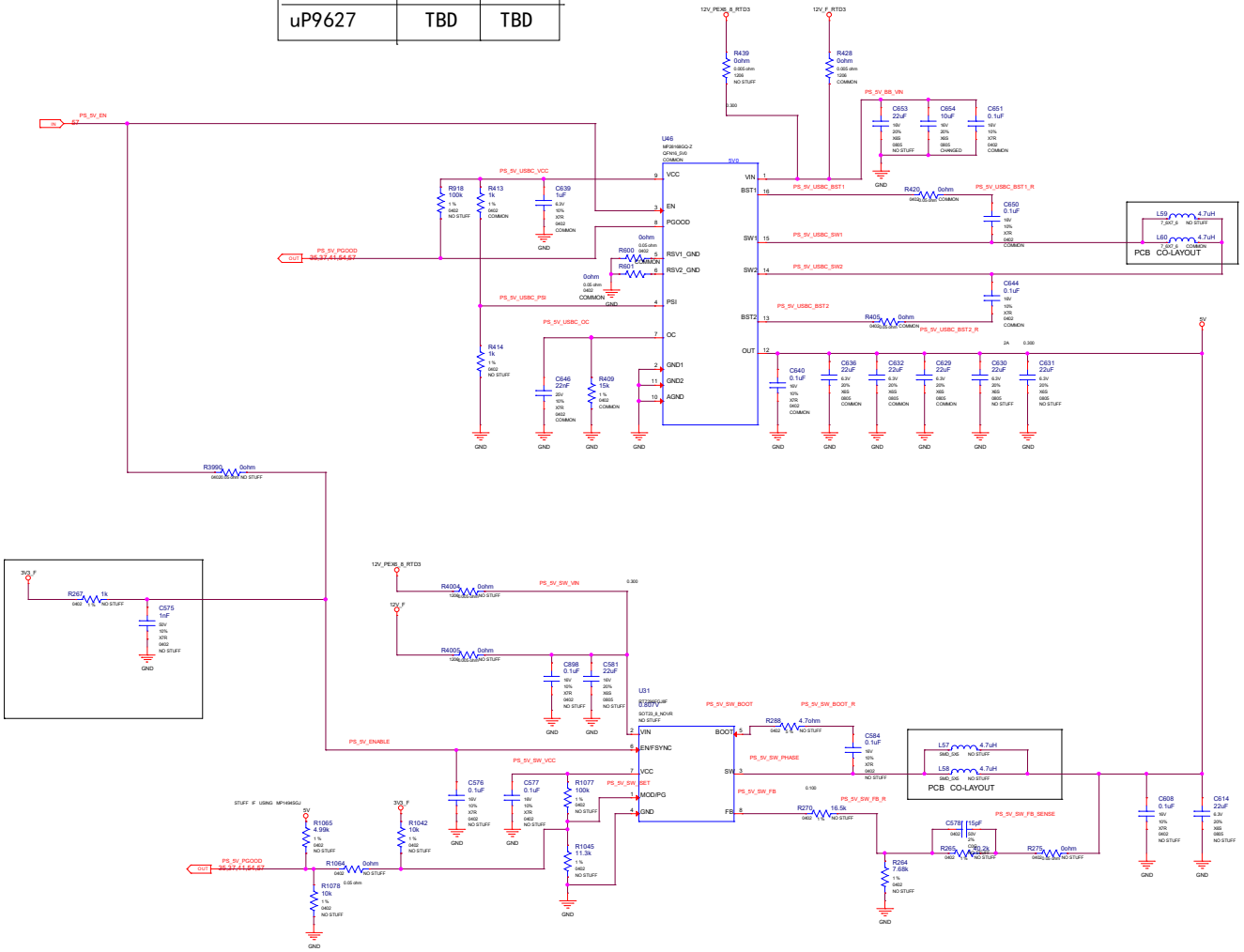
PS: 5V, 5V_BACKUP

	R600	R601
MPS28168	0R	0R
uP9627	TBD	TBD



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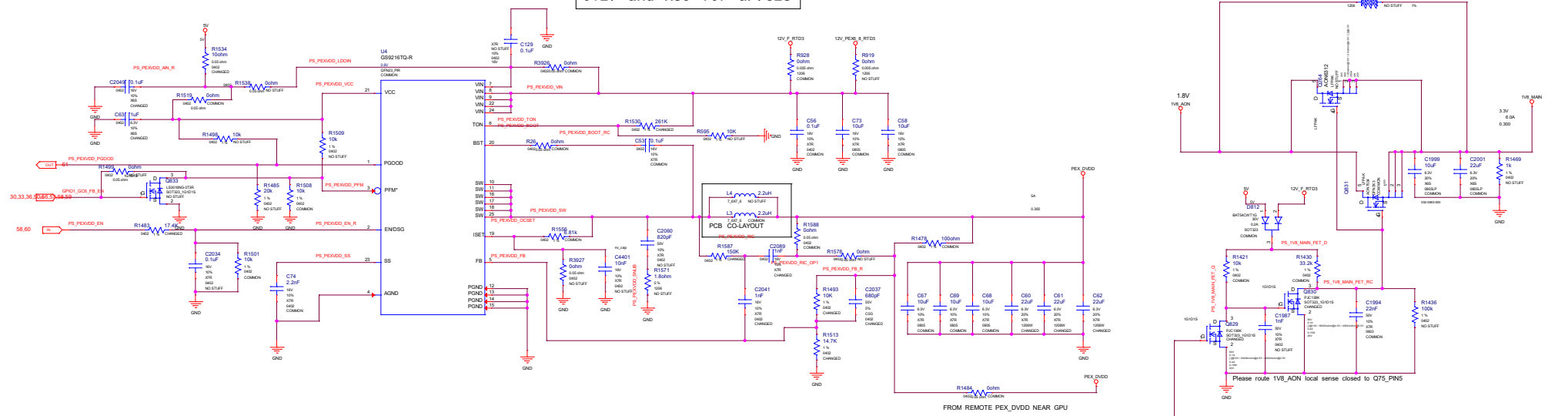
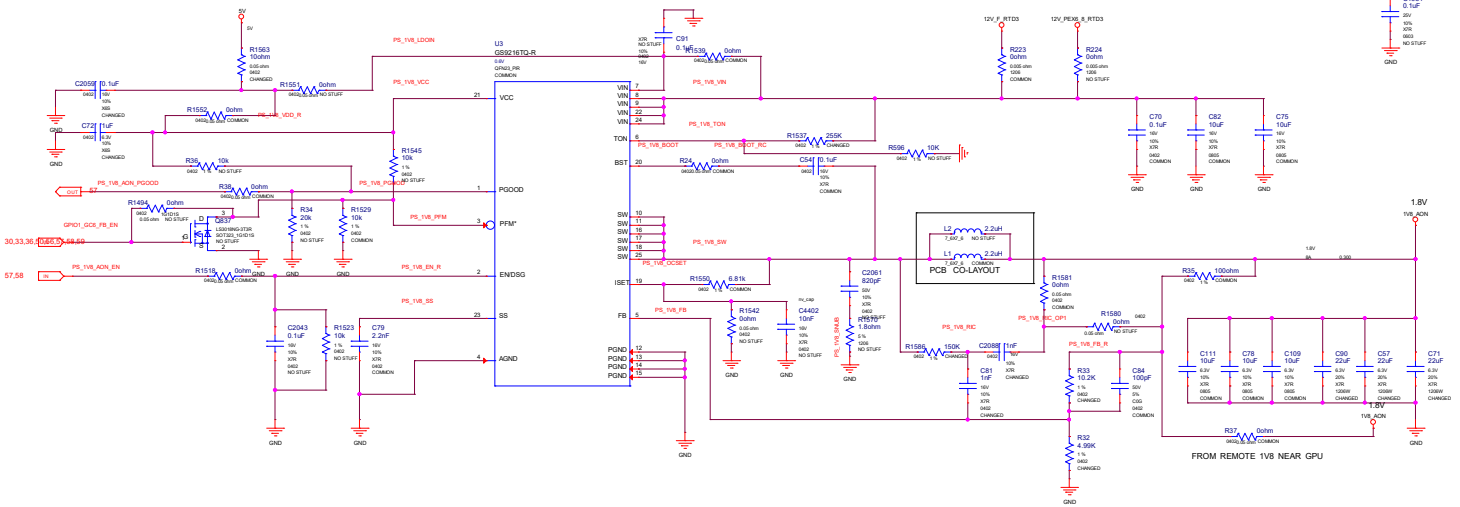
PS: PEXVDD 1V8 Rail

C129 and R85 for uP9628



C91 and R102 for uP9628



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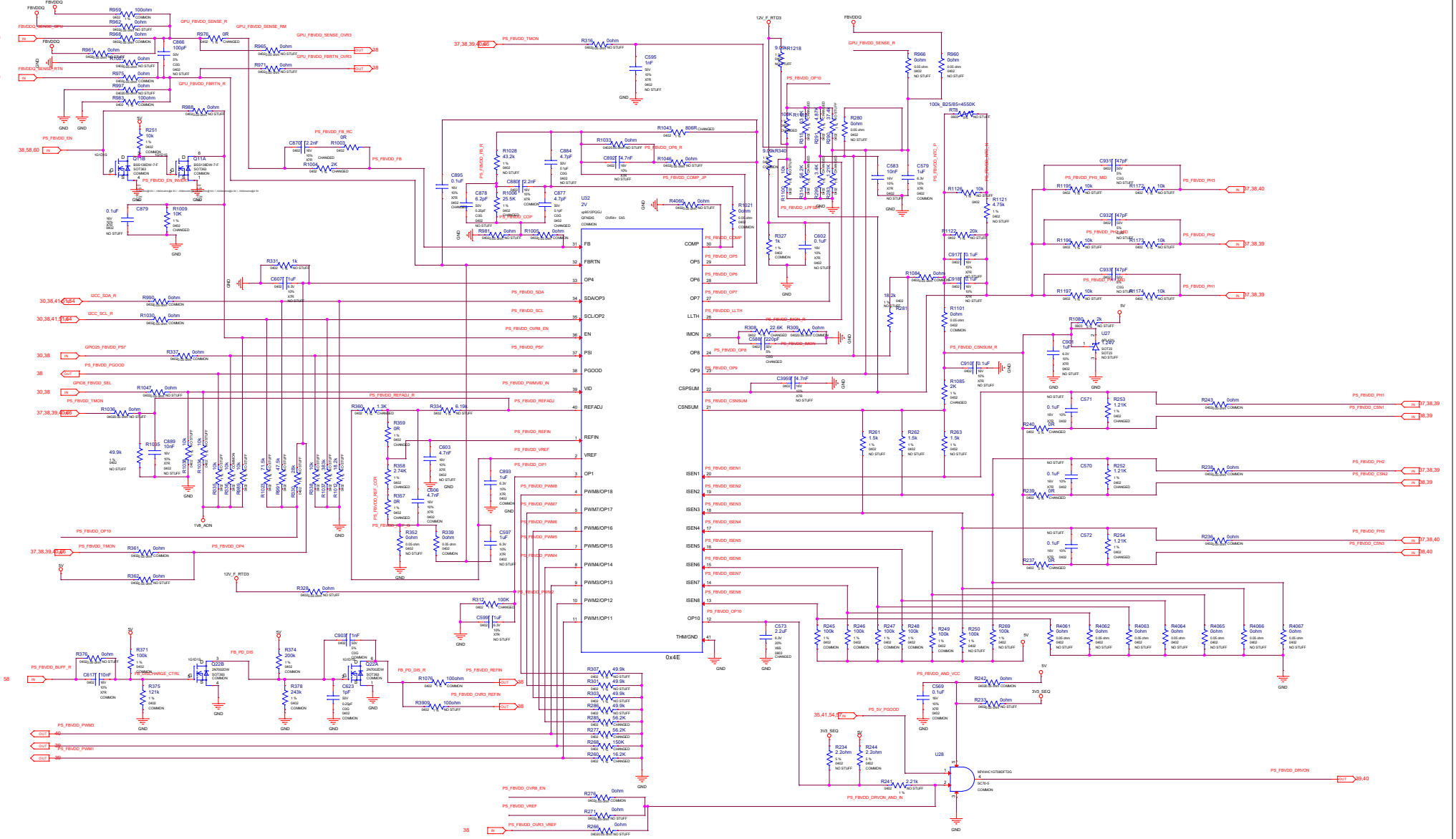
PS: FBVDD Controller



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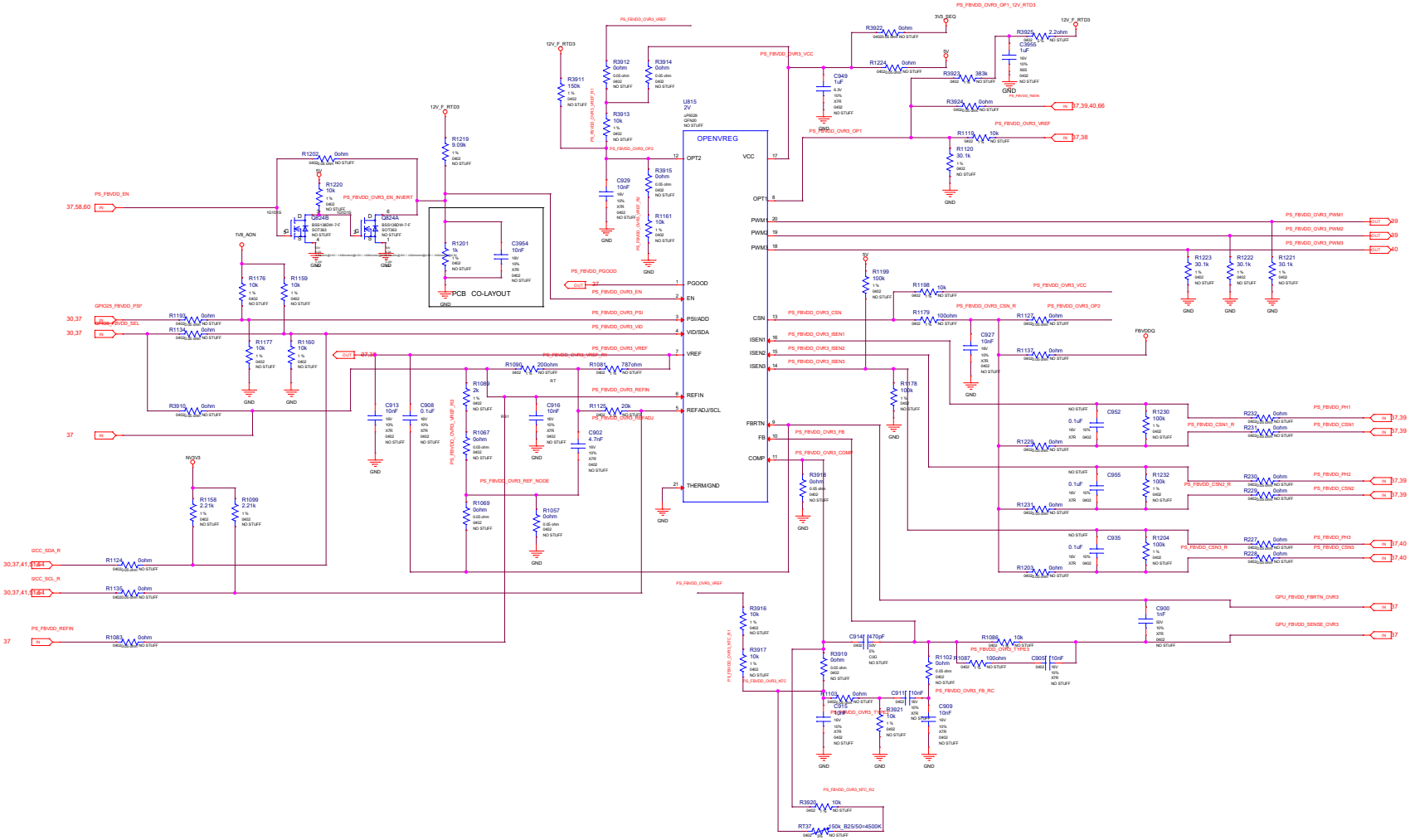
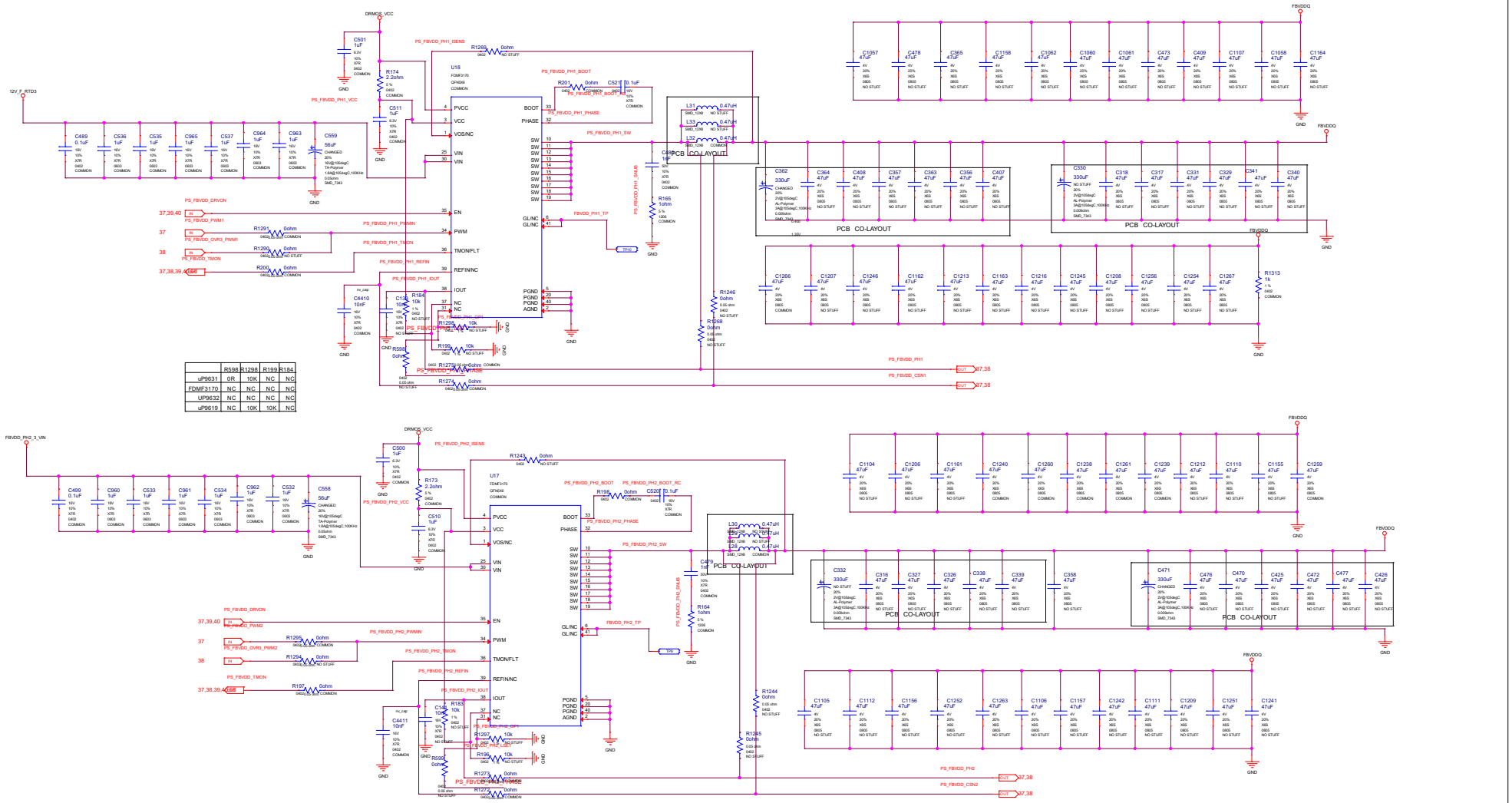
PS: FBVDD Controller OVR3


OPENVREG
PCB CO-LAYOUT
PS_FBVDD_EN
PS_FBVDD_REFIN
PS_FBVDD_PGOOD
PS_FBVDD_OVR3_EN
PS_FBVDD_OVR3_PSI
PS_FBVDD_OVR3_VID
PS_FBVDD_OVR3_VREF
PS_FBVDD_OVR3_REFIN
PS_FBVDD_OVR3_REF_NODE
PS_FBVDD_OVR3_FB
PS_FBVDD_OVR3_COMP
PS_FBVDD_OVR3_VCC
PS_FBVDD_OVR3_CSN
PS_FBVDD_OVR3_ISEN1
PS_FBVDD_OVR3_ISEN2
PS_FBVDD_OVR3_ISEN3
PS_FBVDD_OVR3_PWM1
PS_FBVDD_OVR3_PWM2
PS_FBVDD_OVR3_PWM3
PS_FBVDD_PH1
PS_FBVDD_PH2
PS_FBVDD_PH3
GPU_FBVDD_FBRTN_OVR3
GPU_FBVDD_SENSE_OVR3
PS_FBVDD_OVR3_FB_RC
PS_FBVDD_OVR3_NTC_R1
PS_FBVDD_OVR3_NTC_R2
PS_FBVDD_OVR3_VREF_R1
PS_FBVDD_OVR3_VREF_R2
PS_FBVDD_OVR3_REFADJ
PS_FBVDD_OVR3_OP1_12V_RTD3
PS_FBVDD_OVR3_OP1
PS_FBVDD_OVR3_OP2
PS_FBVDD_OVR3_VREF
PS_FBVDD_OVR3_CSN_R
PS_FBVDD_CSN1_R
PS_FBVDD_CSN2_R
PS_FBVDD_CSN3_R
PS_FBVDD_CSN1
PS_FBVDD_CSN2
PS_FBVDD_CSN3
PS_FBVDD_OVR3_TYPE3
PS_FBVDD_OVR3_TSEN
PS_FBVDD_OVR3_OP2_R
PS_FBVDD_OVR3_VREF_R
PS_FBVDD_OVR3_NTC_R1
PS_FBVDD_OVR3_REF_R1
PS_FBVDD_OVR3_REF_R2
PS_FBVDD_OVR3_REF_R3
PS_FBVDD_OVR3_REF_R4
PS_FBVDD_OVR3_REF_R5
PS_FBVDD_OVR3_REF_R6
PS_FBVDD_OVR3_REF_R7
PS_FBVDD_OVR3_REF_R8
PS_FBVDD_OVR3_REF_R9
PS_FBVDD_OVR3_REF_R10
PS_FBVDD_OVR3_REF_R11
PS_FBVDD_OVR3_REF_R12
PS_FBVDD_OVR3_REF_R13
PS_FBVDD_OVR3_REF_R14
PS_FBVDD_OVR3_REF_R15
PS_FBVDD_OVR3_REF_R16
PS_FBVDD_OVR3_REF_R17
PS_FBVDD_OVR3_REF_R18
PS_FBVDD_OVR3_REF_R19
PS_FBVDD_OVR3_REF_R20
PS_FBVDD_OVR3_REF_R21
PS_FBVDD_OVR3_REF_R22
PS_FBVDD_OVR3_REF_R23
PS_FBVDD_OVR3_REF_R24
PS_FBVDD_OVR3_REF_R25
PS_FBVDD_OVR3_REF_R26
PS_FBVDD_OVR3_REF_R27
PS_FBVDD_OVR3_REF_R28
PS_FBVDD_OVR3_REF_R29
PS_FBVDD_OVR3_REF_R30
PS_FBVDD_OVR3_REF_R31
PS_FBVDD_OVR3_REF_R32
PS_FBVDD_OVR3_REF_R33
PS_FBVDD_OVR3_REF_R34
PS_FBVDD_OVR3_REF_R35
PS_FBVDD_OVR3_REF_R36
PS_FBVDD_OVR3_REF_R37
PS_FBVDD_OVR3_REF_R38
PS_FBVDD_OVR3_REF_R39
PS_FBVDD_OVR3_REF_R40

PS: FBVDD PH1, 2



	R598	R1298	R199	R184
uP9631	0R	10K	NC	NC
FDMF3170	NC	NC	NC	NC
UP9632	NC	NC	NC	NC
uP9619	NC	10K	10K	NC

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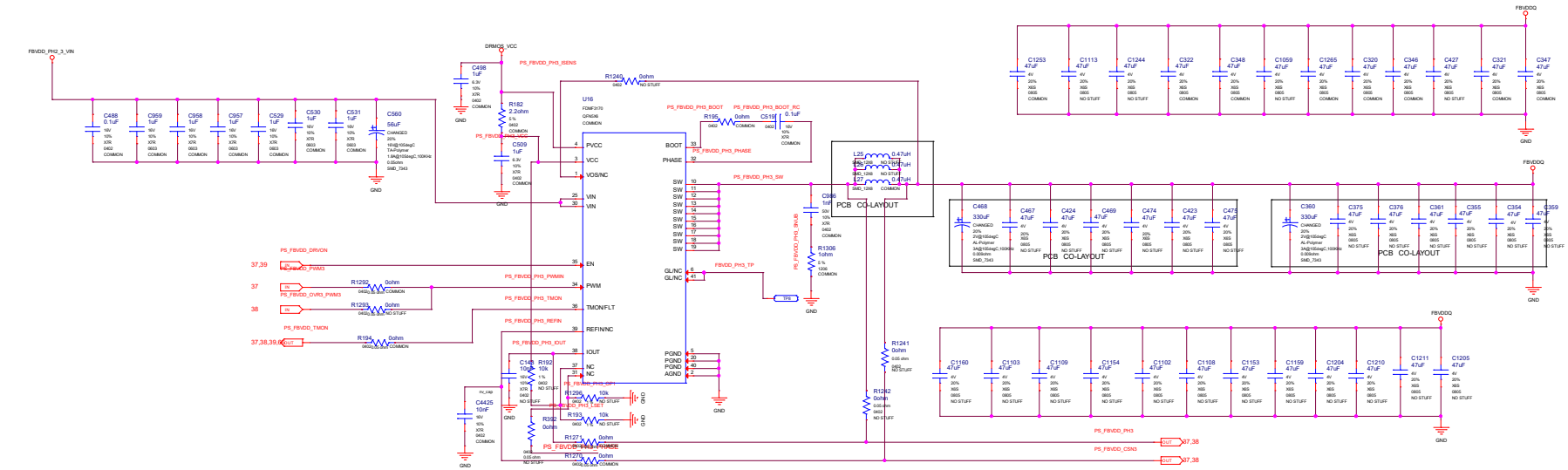
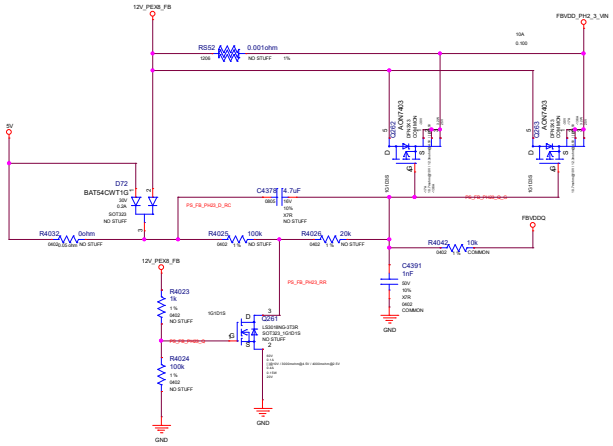
PS: FBVDD PH3





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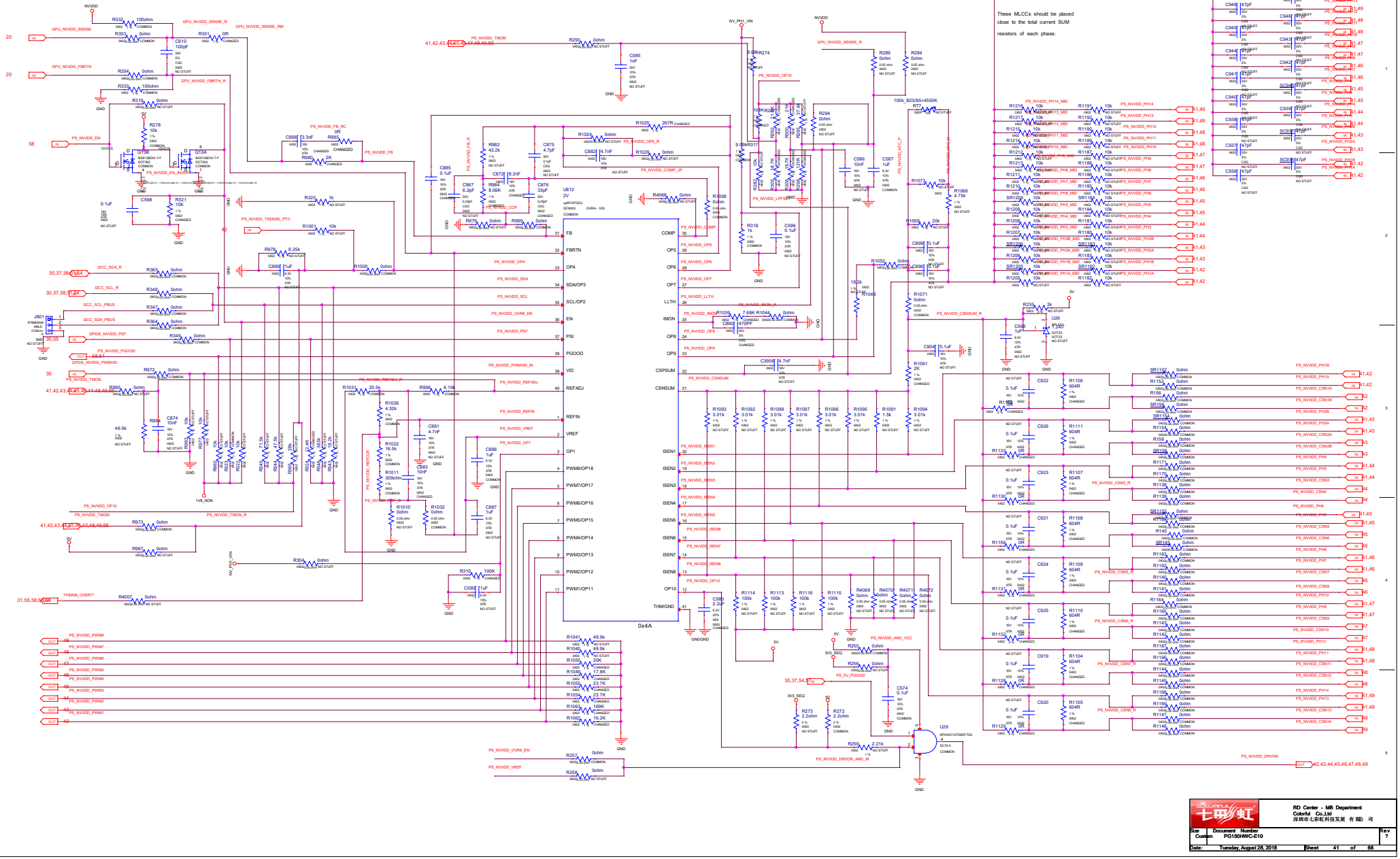
PS: NVVDD Controller_OVR8



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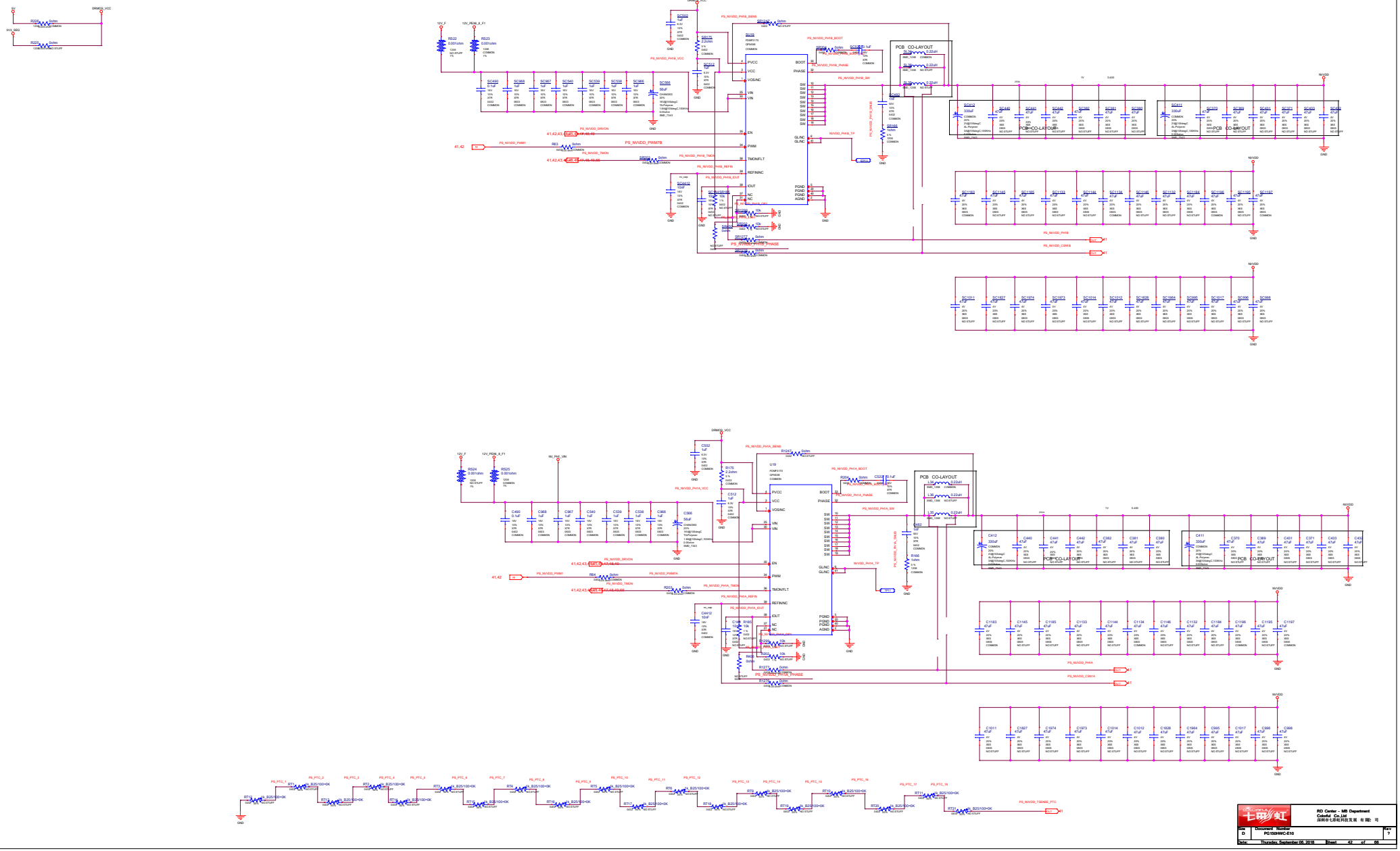
PS: NVVDD Phase 1



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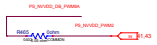
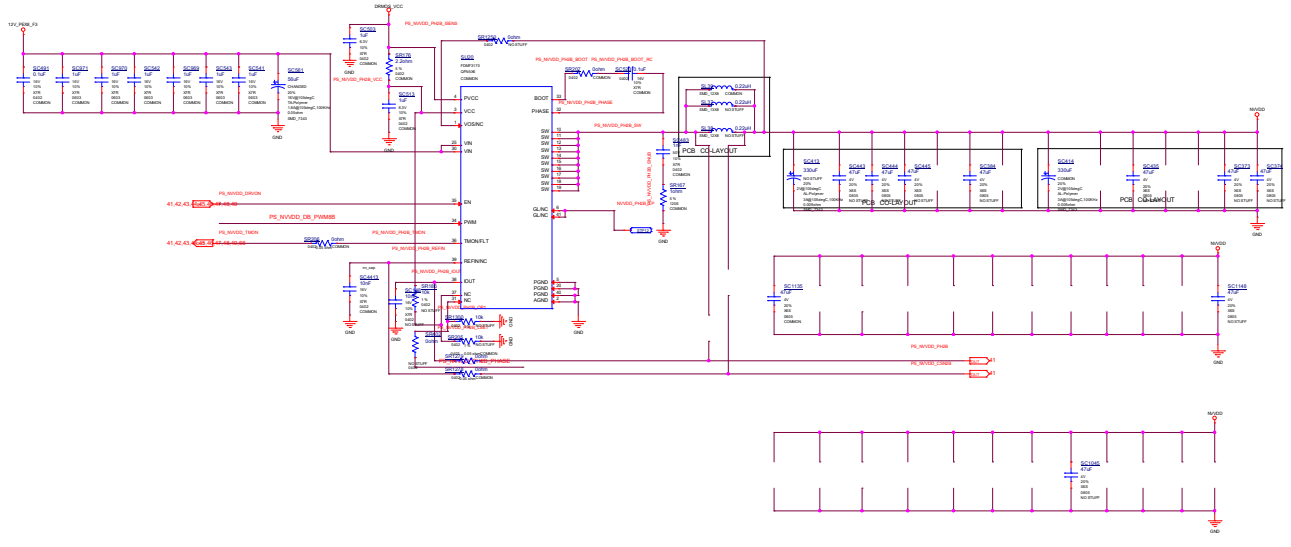
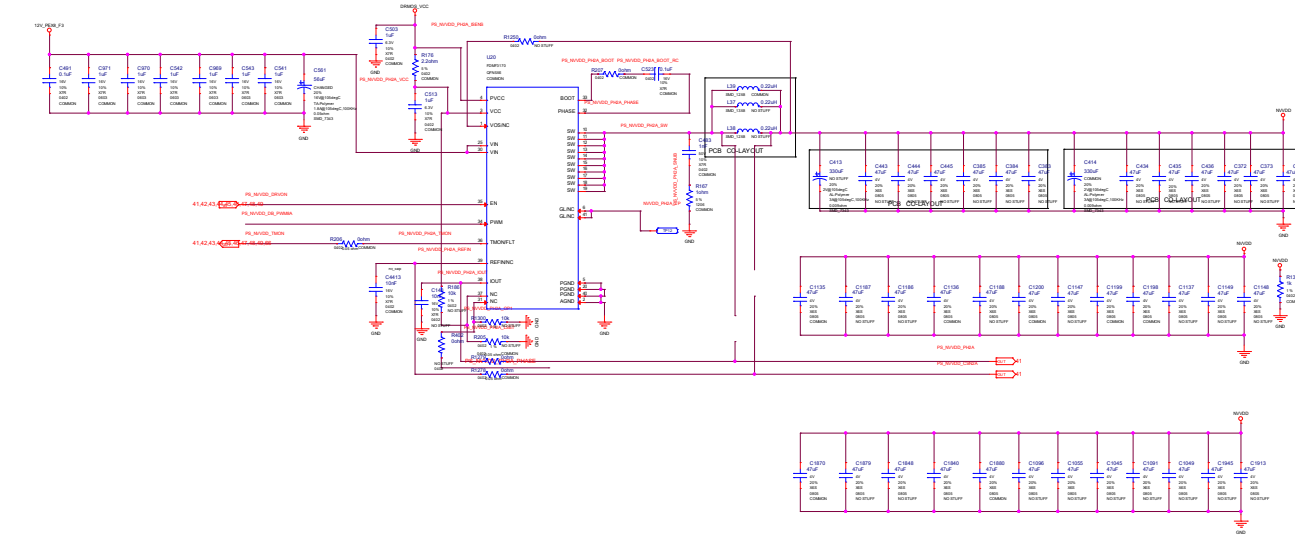
PS: NVVDD Phase 2







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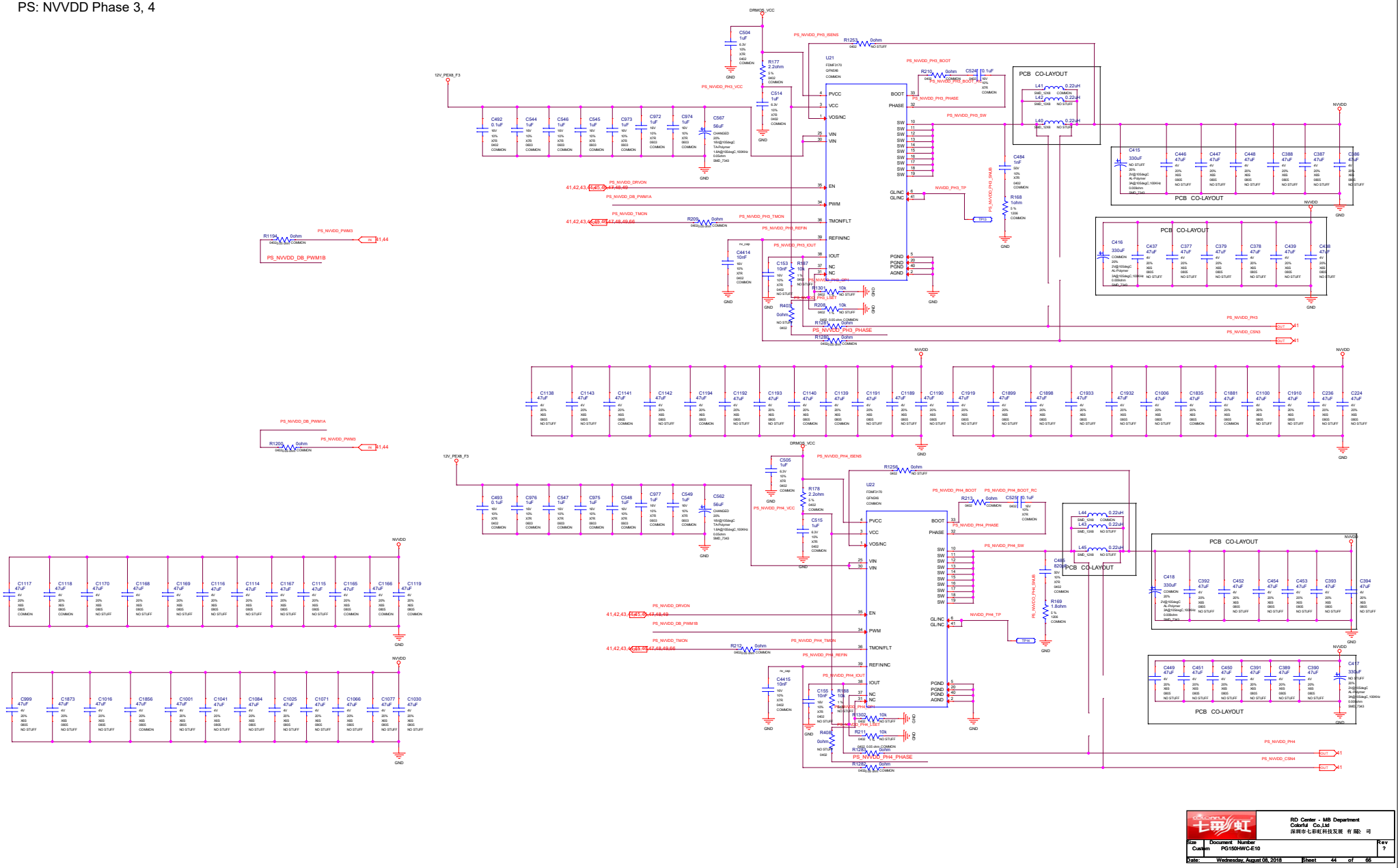
PS: NVVDD Phase 3, 4



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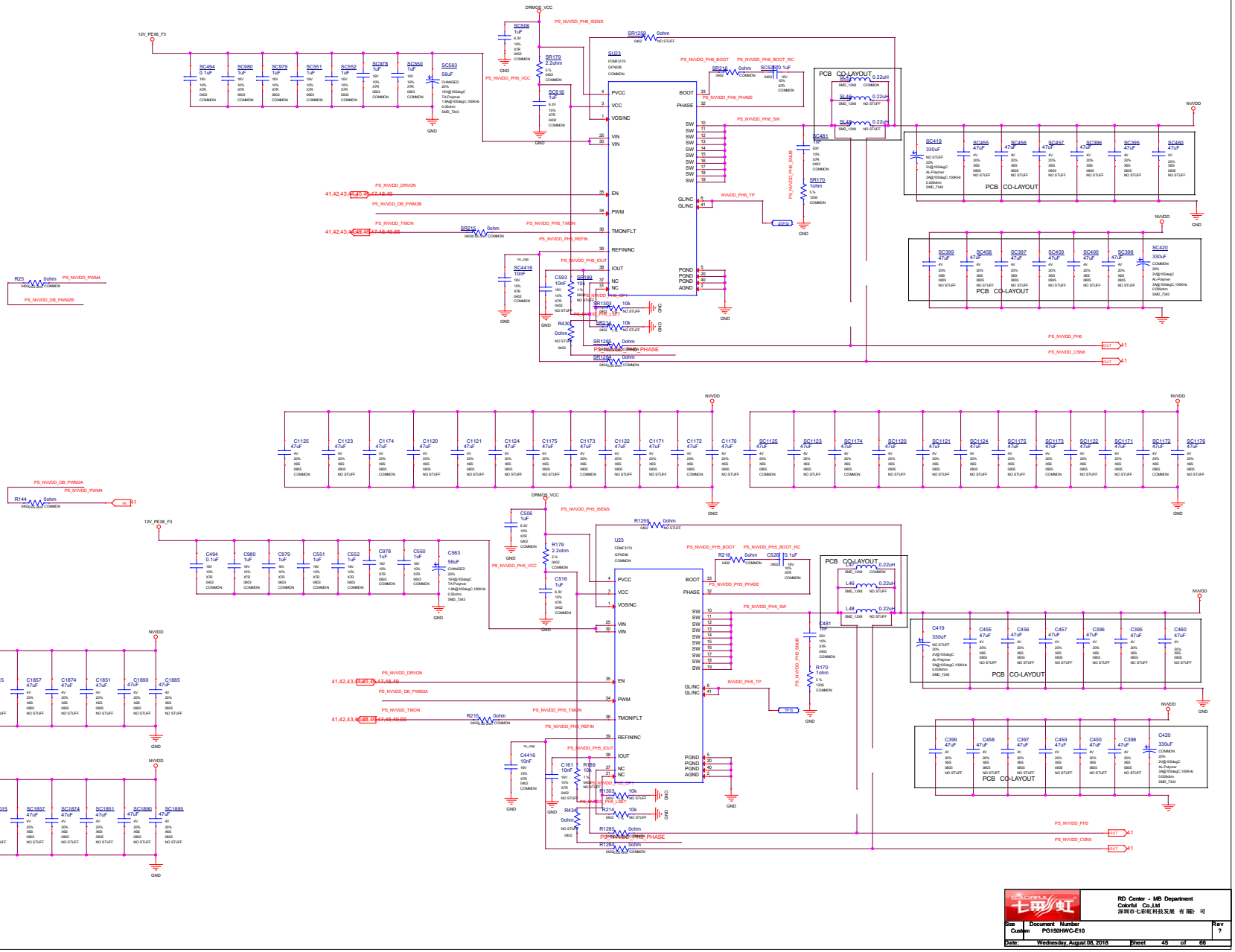
PS: NVVDD Phase 5



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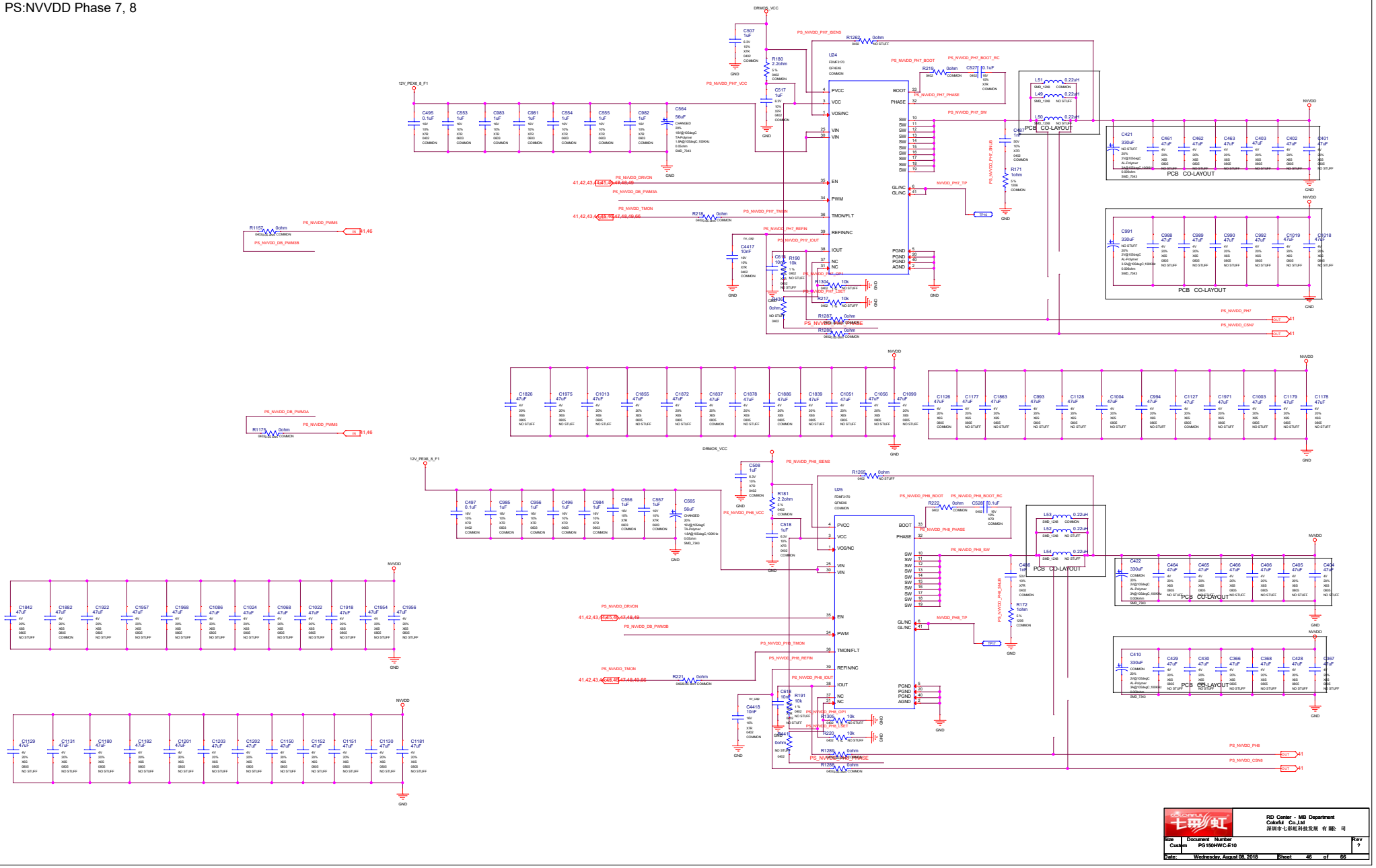
PS:NVVDD Phase 7, 8



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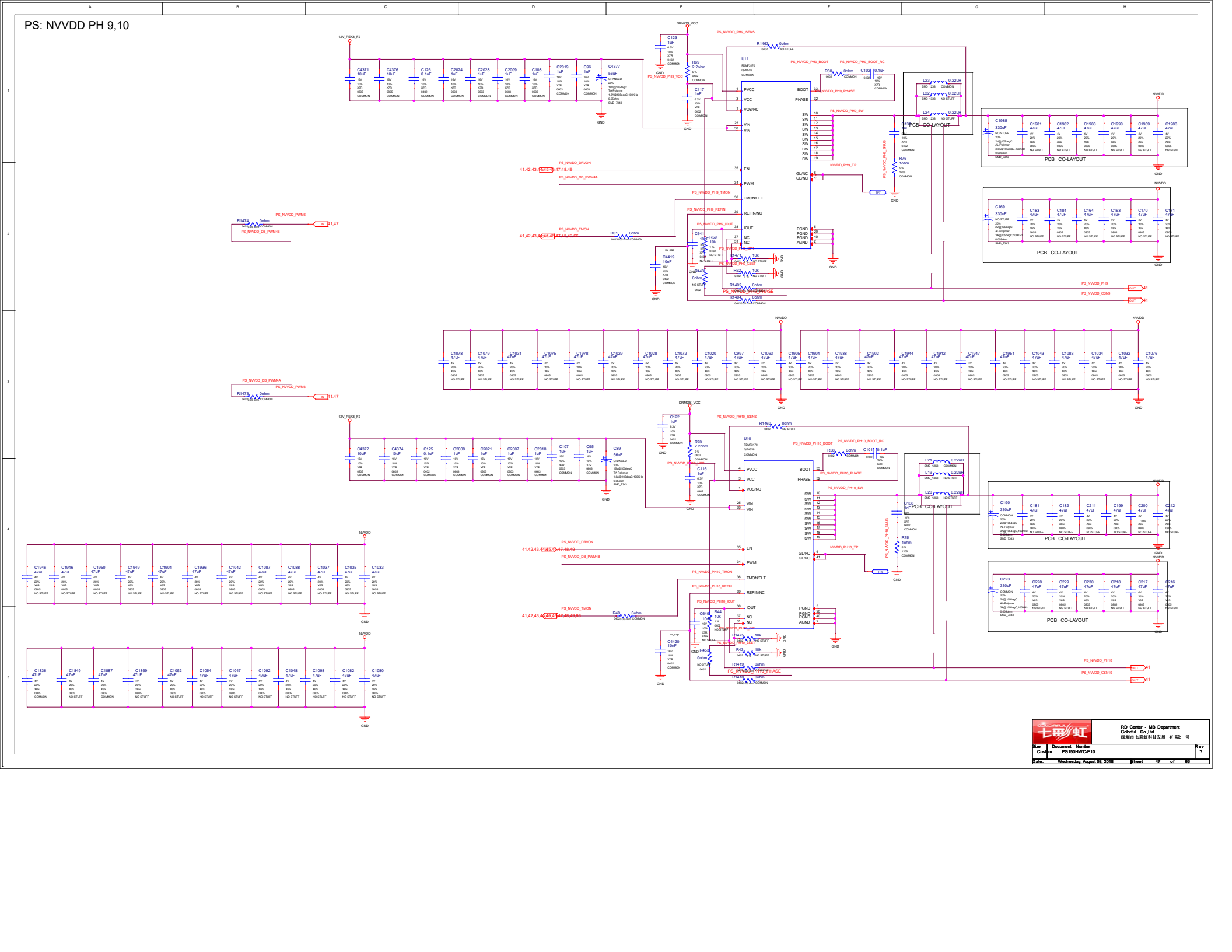
PS: NVVDD PH 9,10



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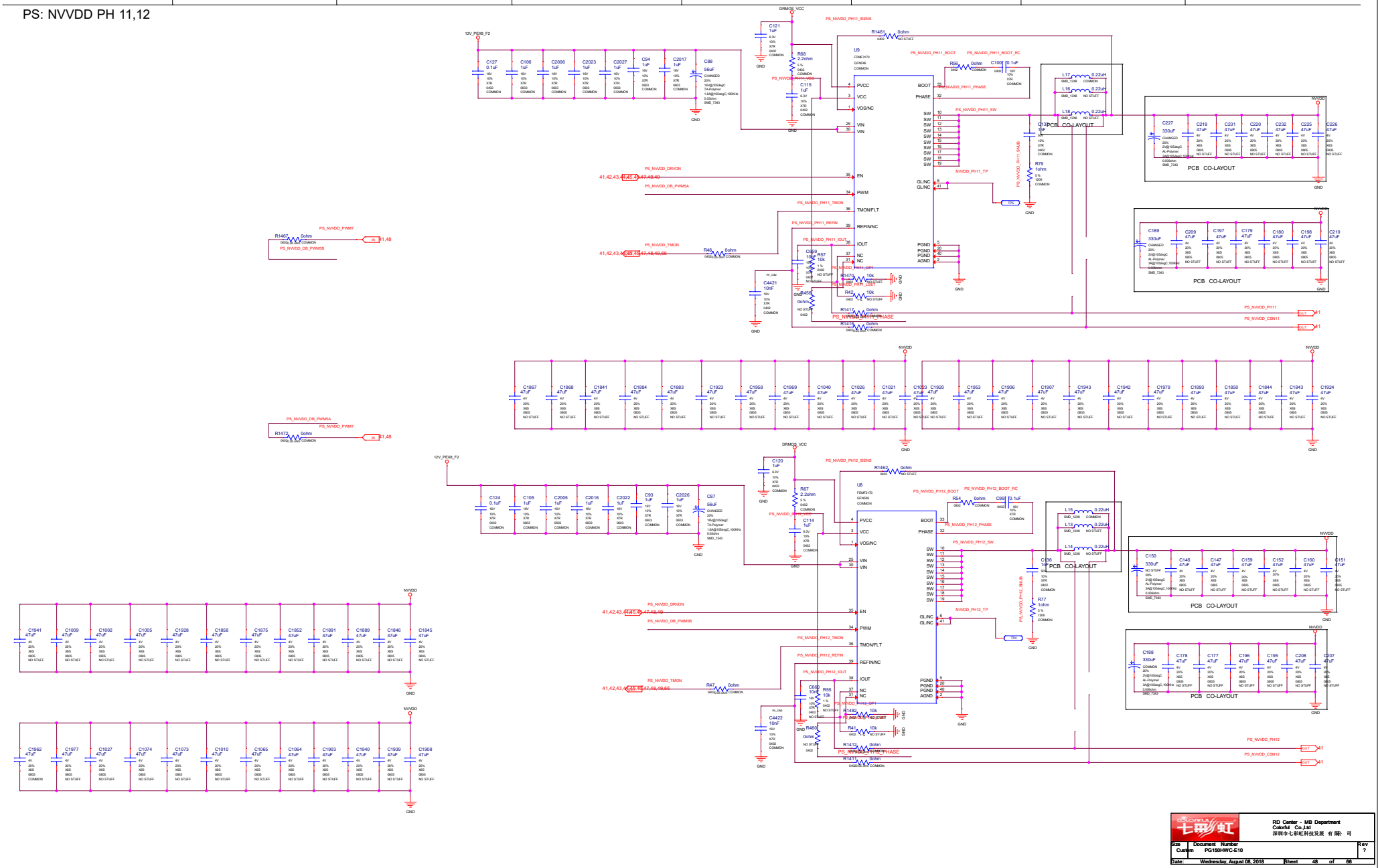
PS: NVVDD PH 11,12



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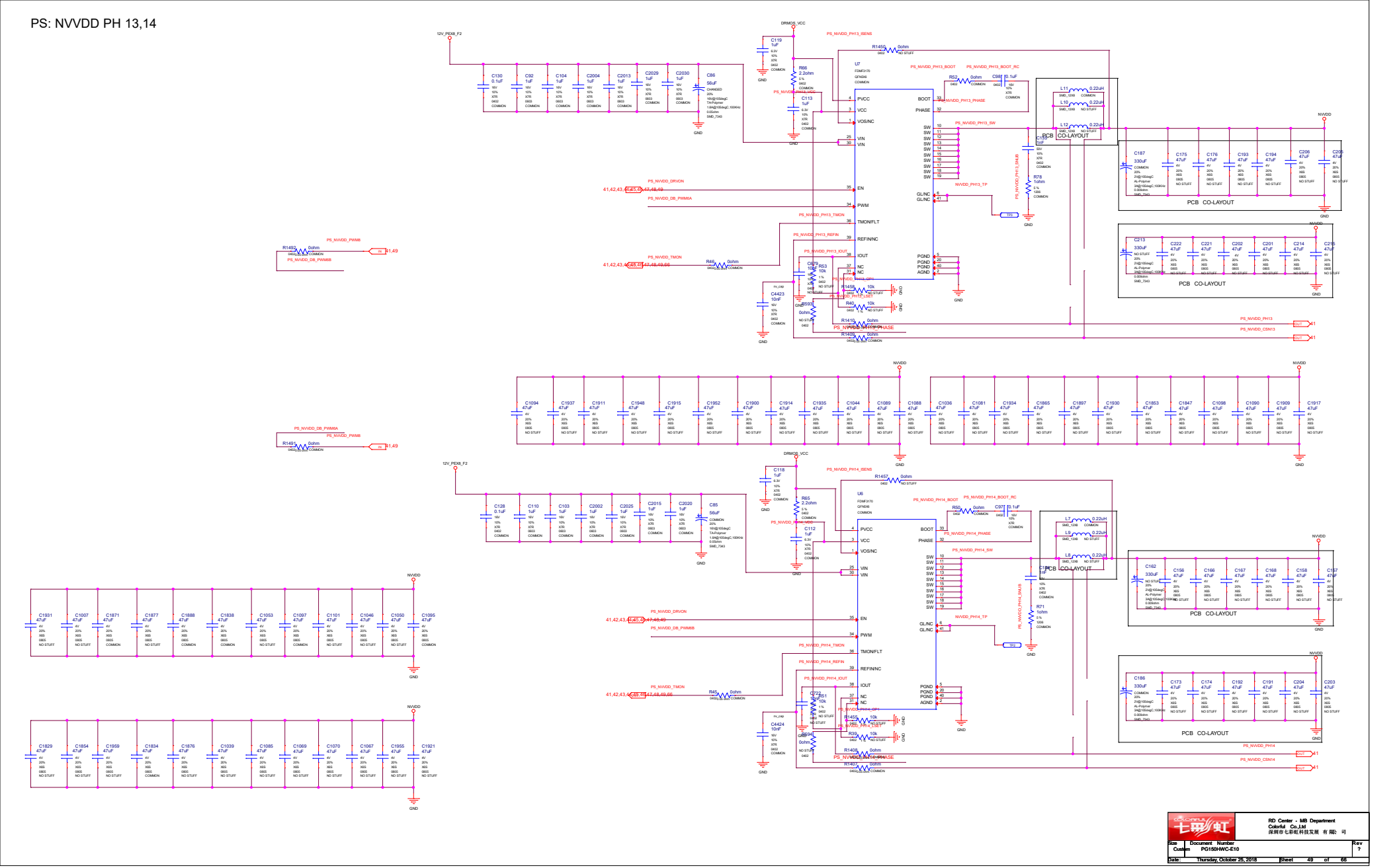
PS: NVVDD PH 13,14



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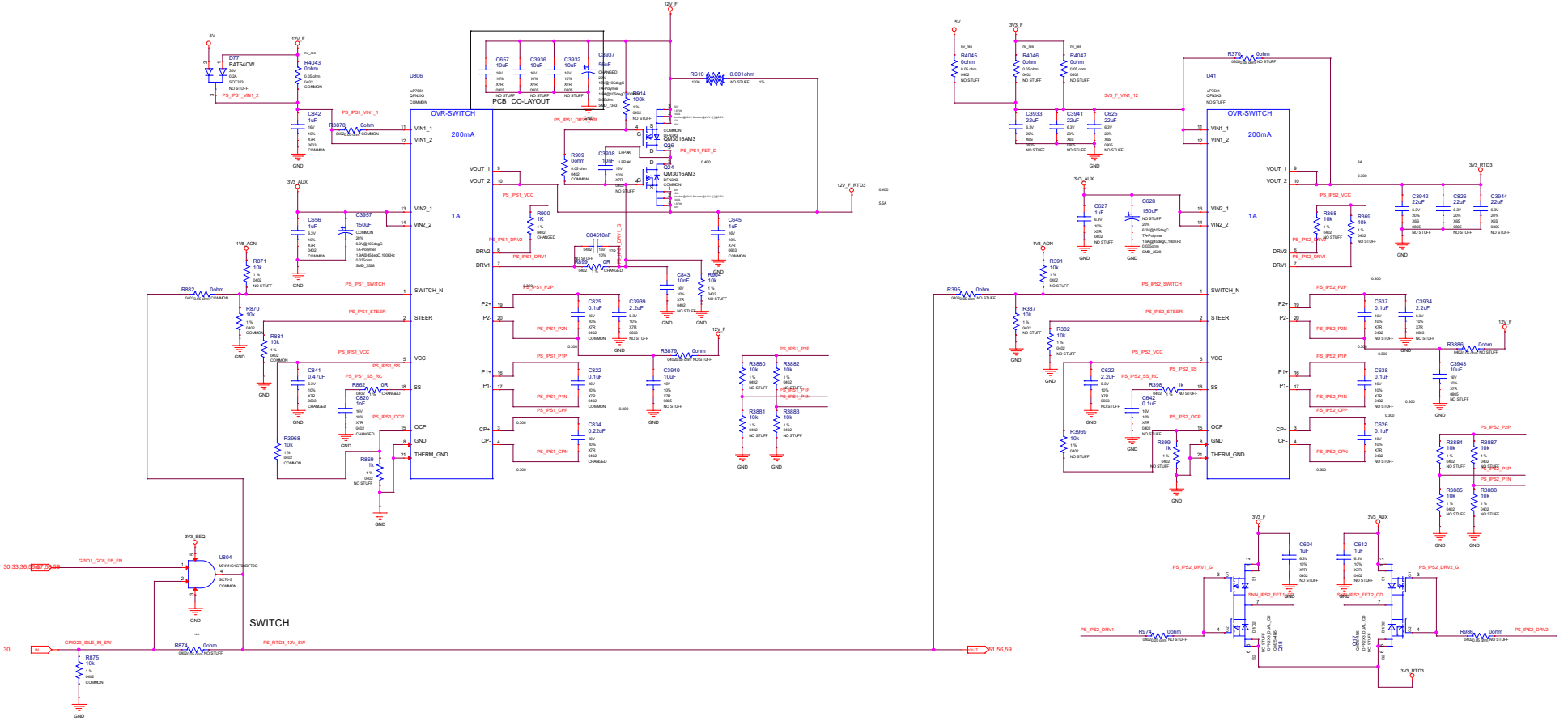
PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



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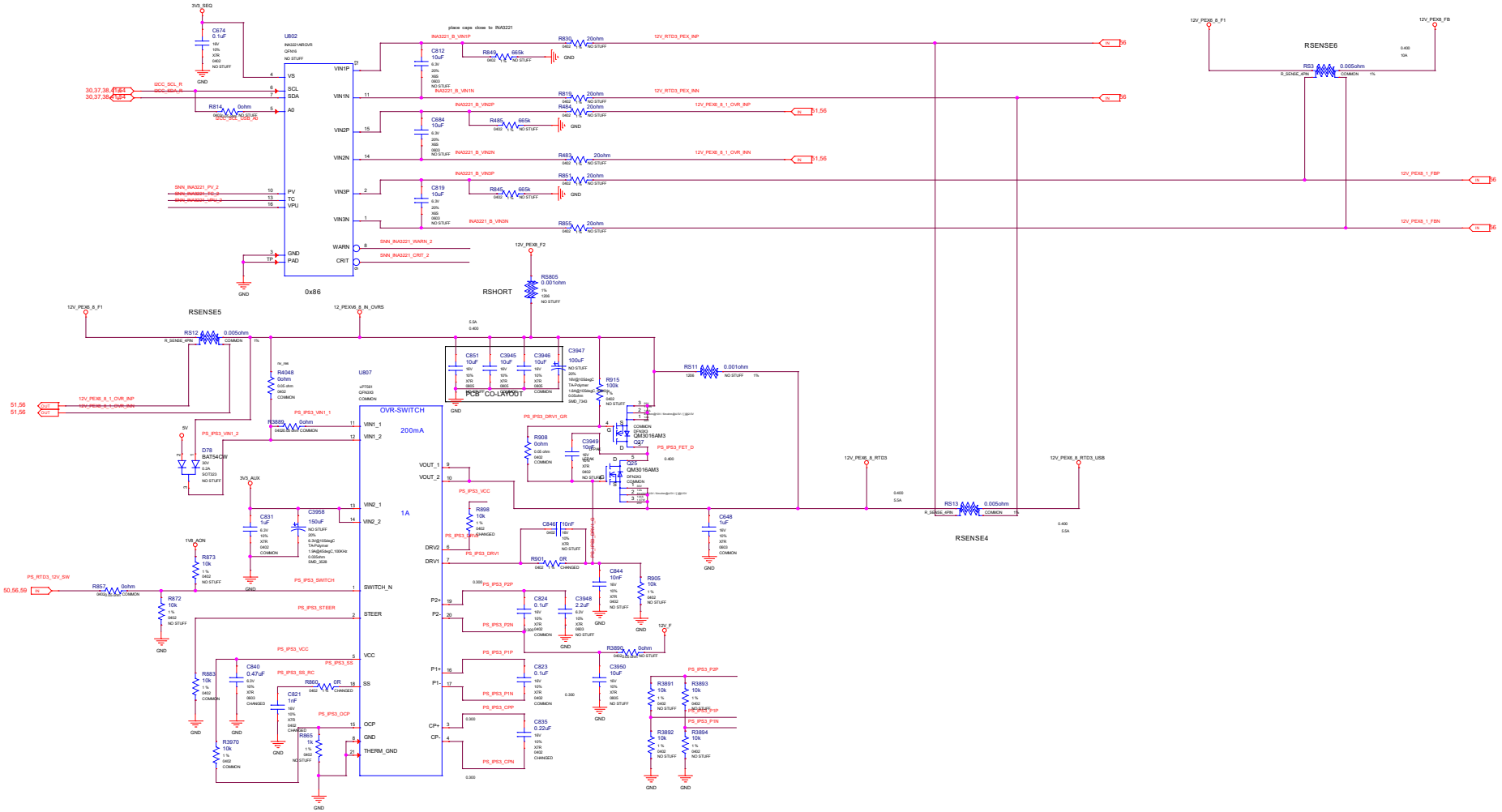

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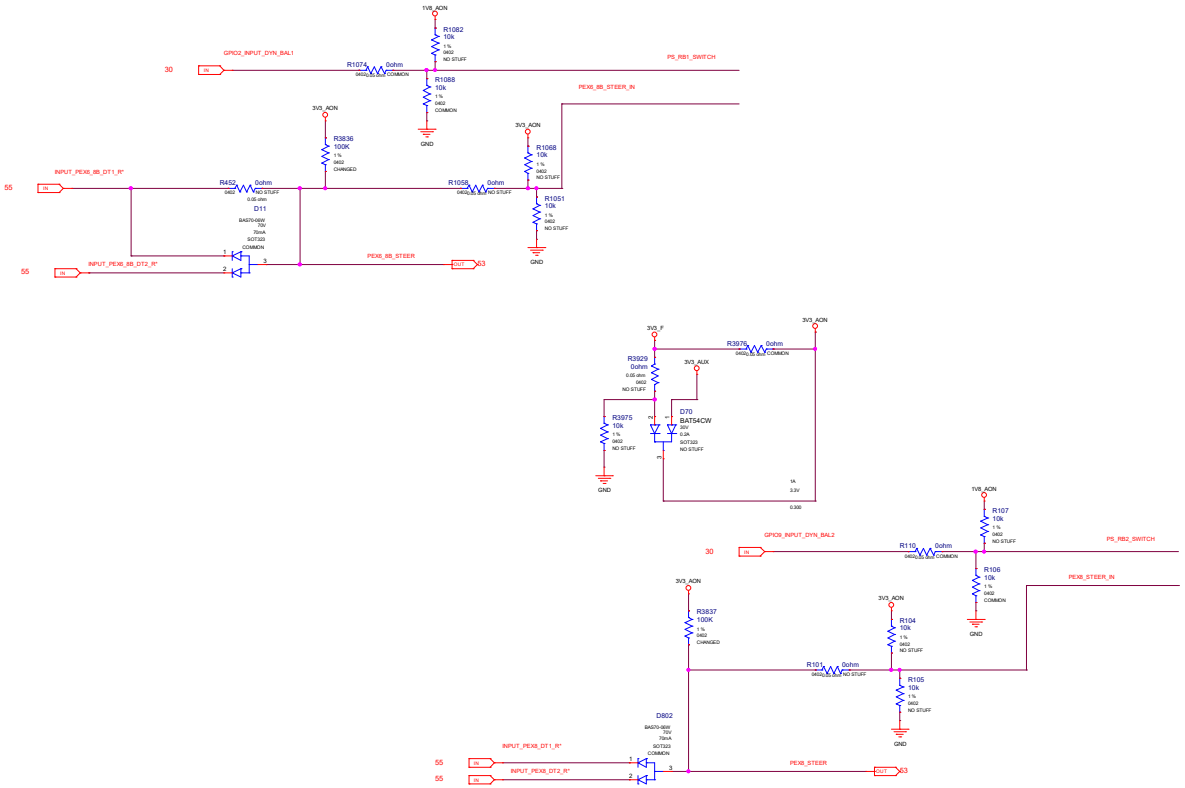
PS: Input Switch Rail Balance



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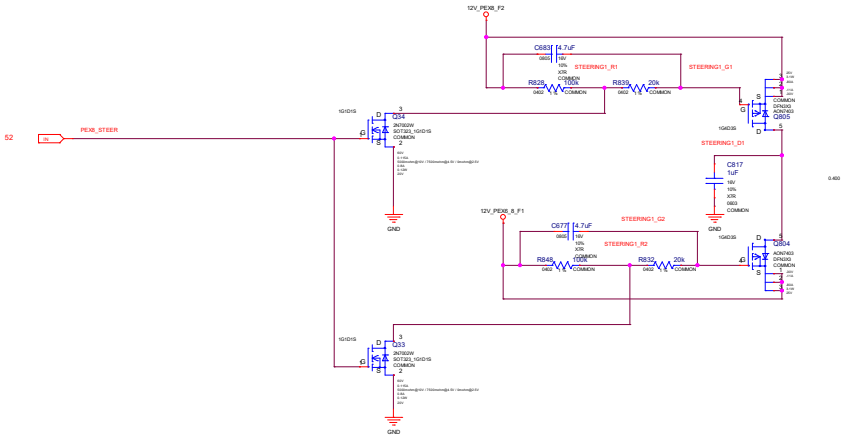
12V CURRENT STEERING (UNDER POWER BOOT):

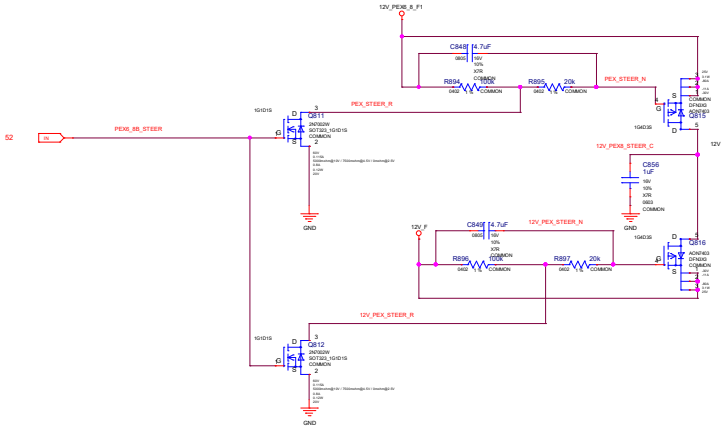
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



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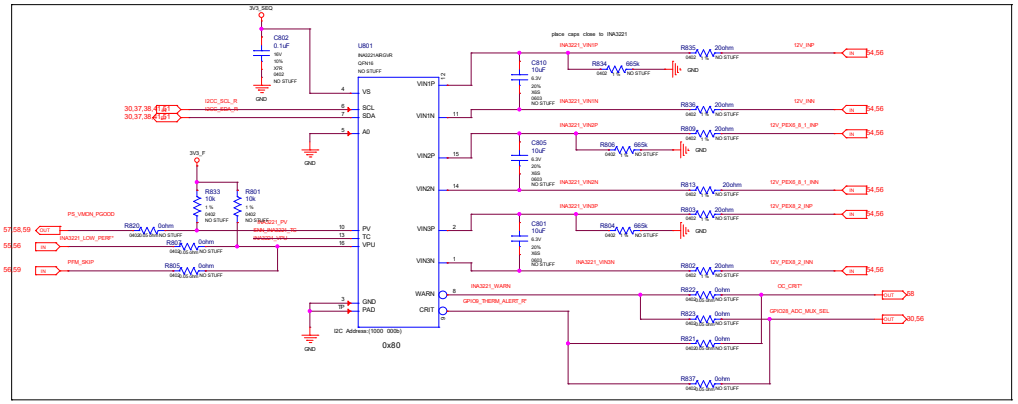
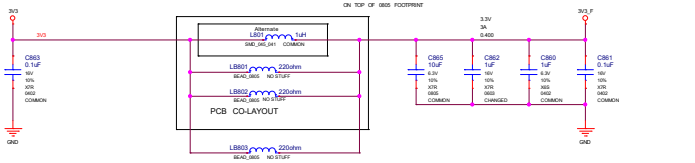
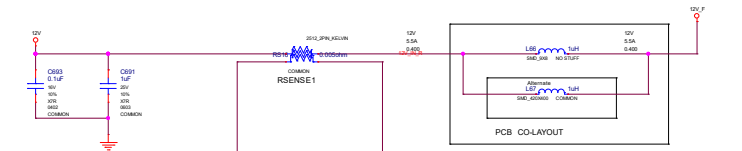
PS: Inputs, Filtering, and Monitoring



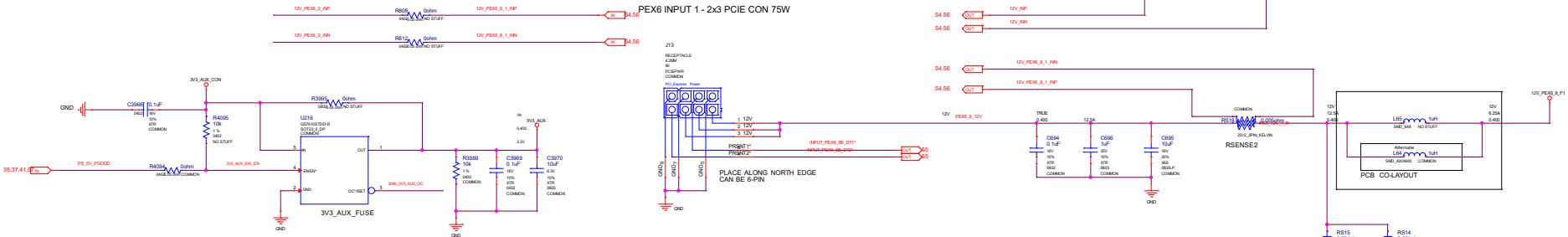
PEX 3V3 INPUT - 10W



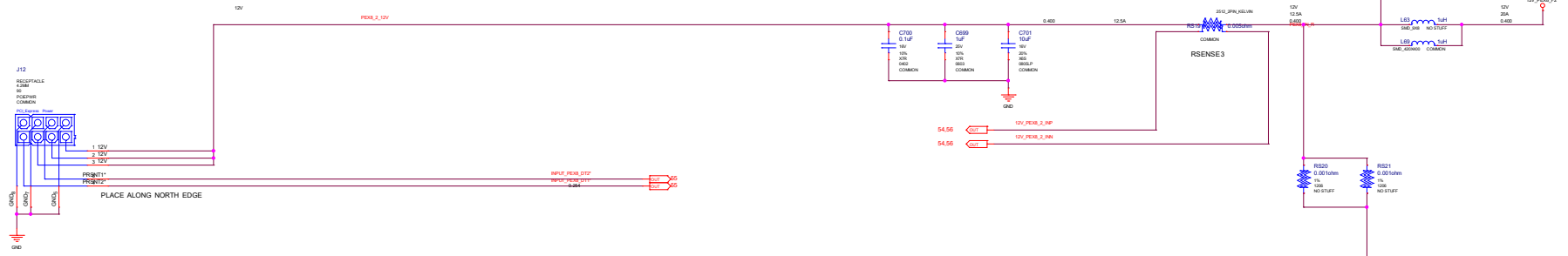
PEX_12V INPUT - 66W



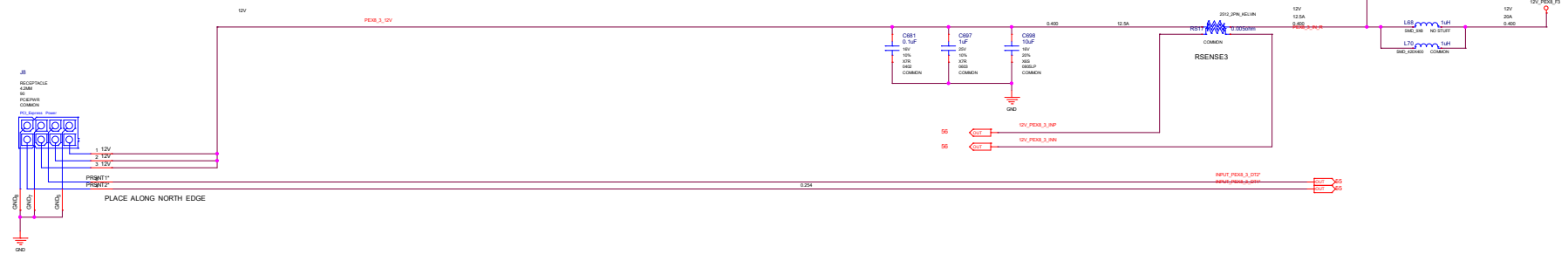
PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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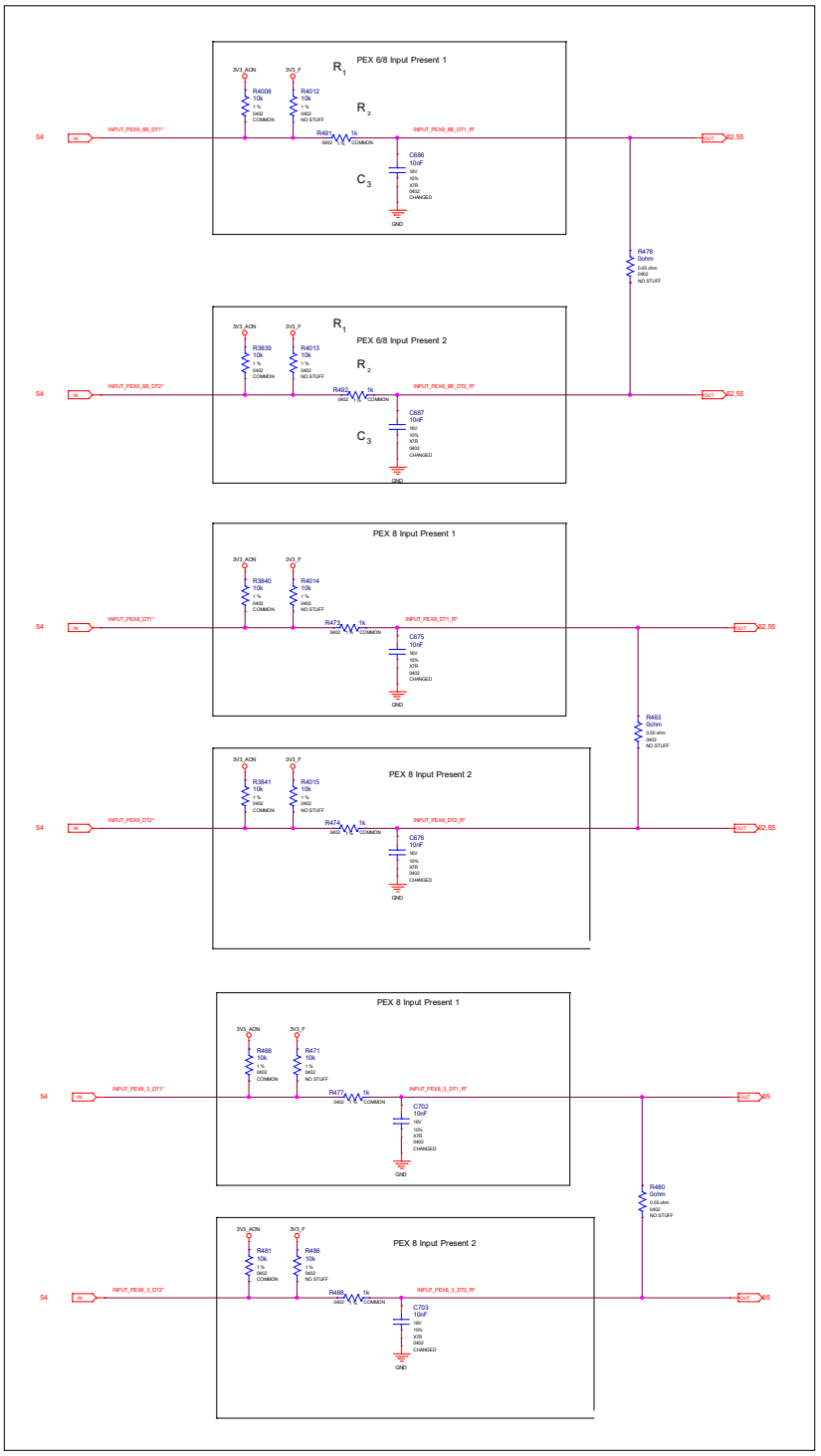
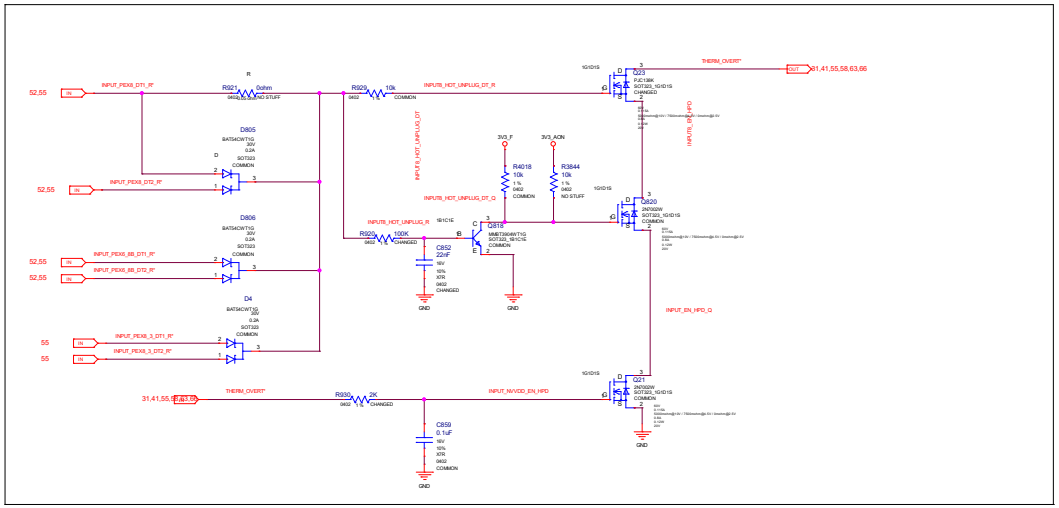
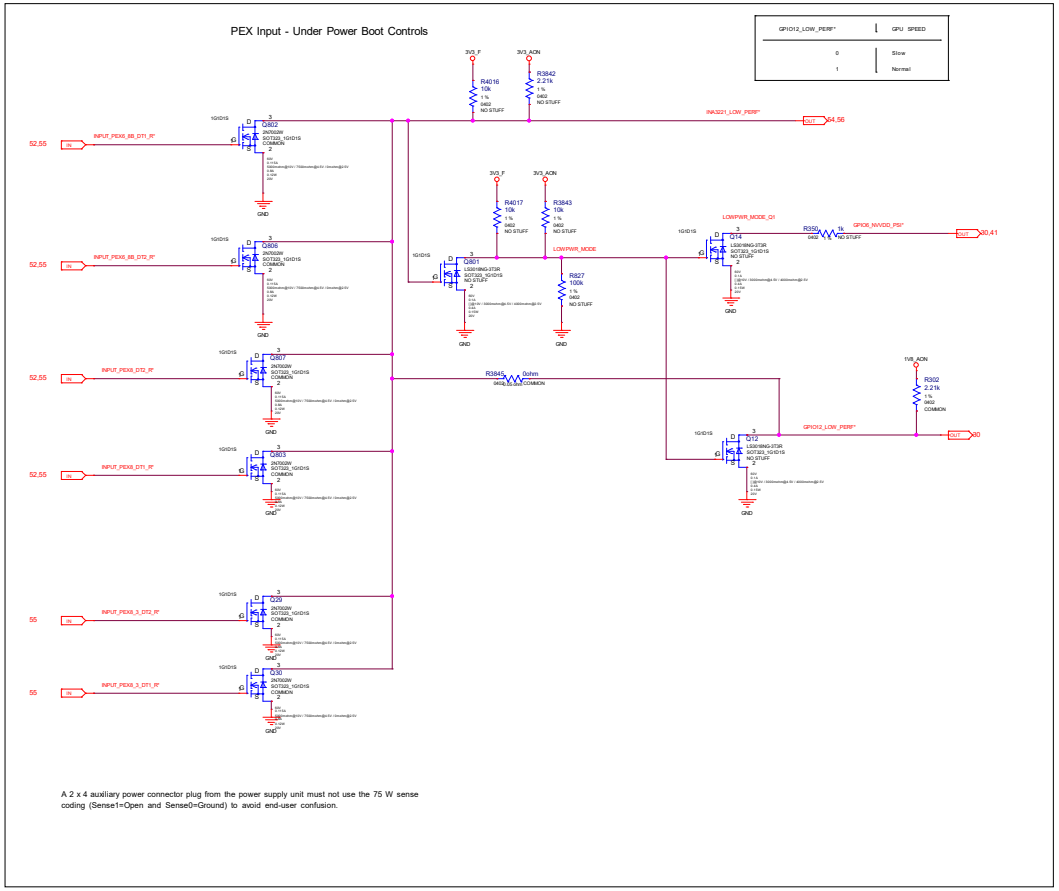
PS: 12V Current Steering & Hot Unplug Detect







A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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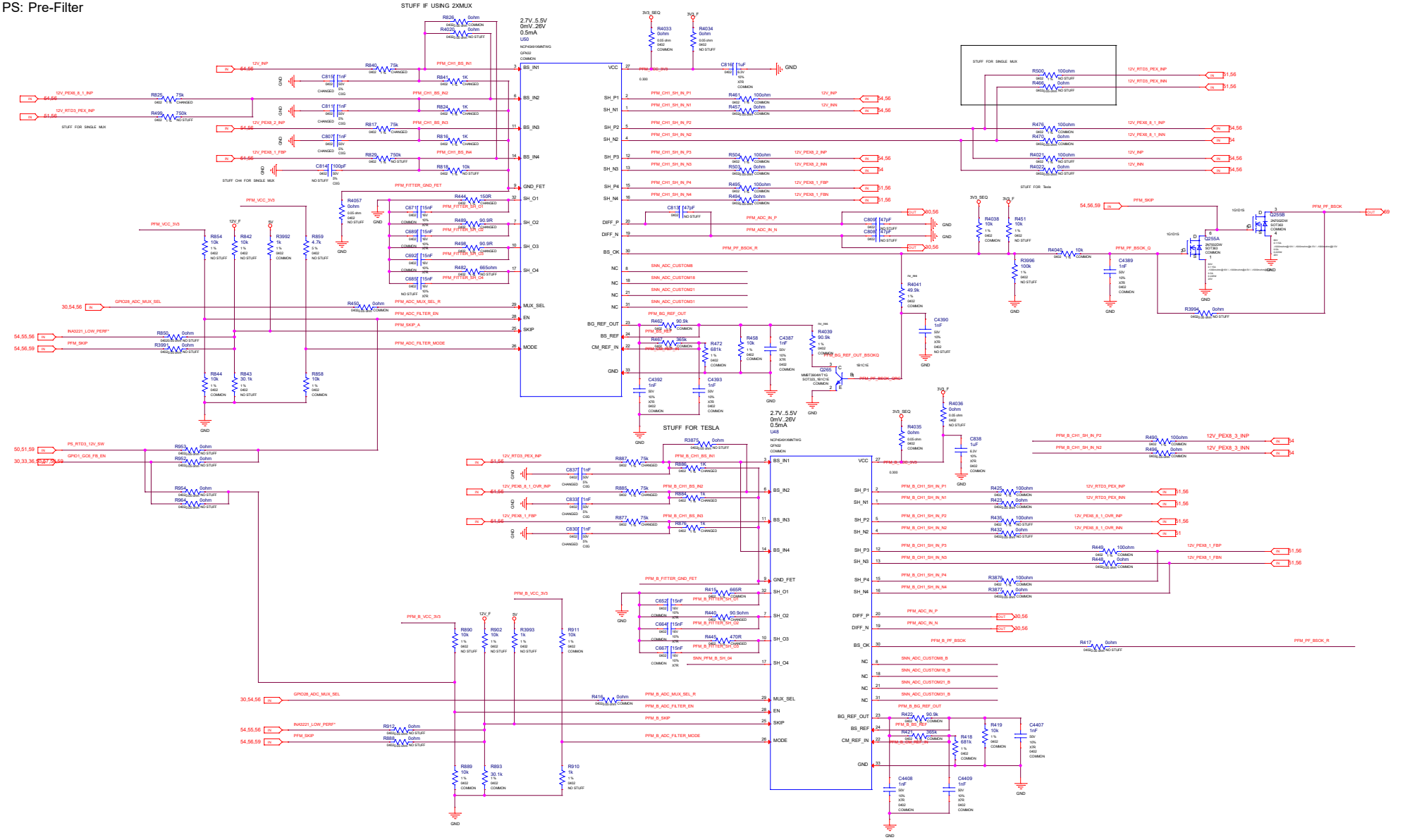
PS: Pre-Filter



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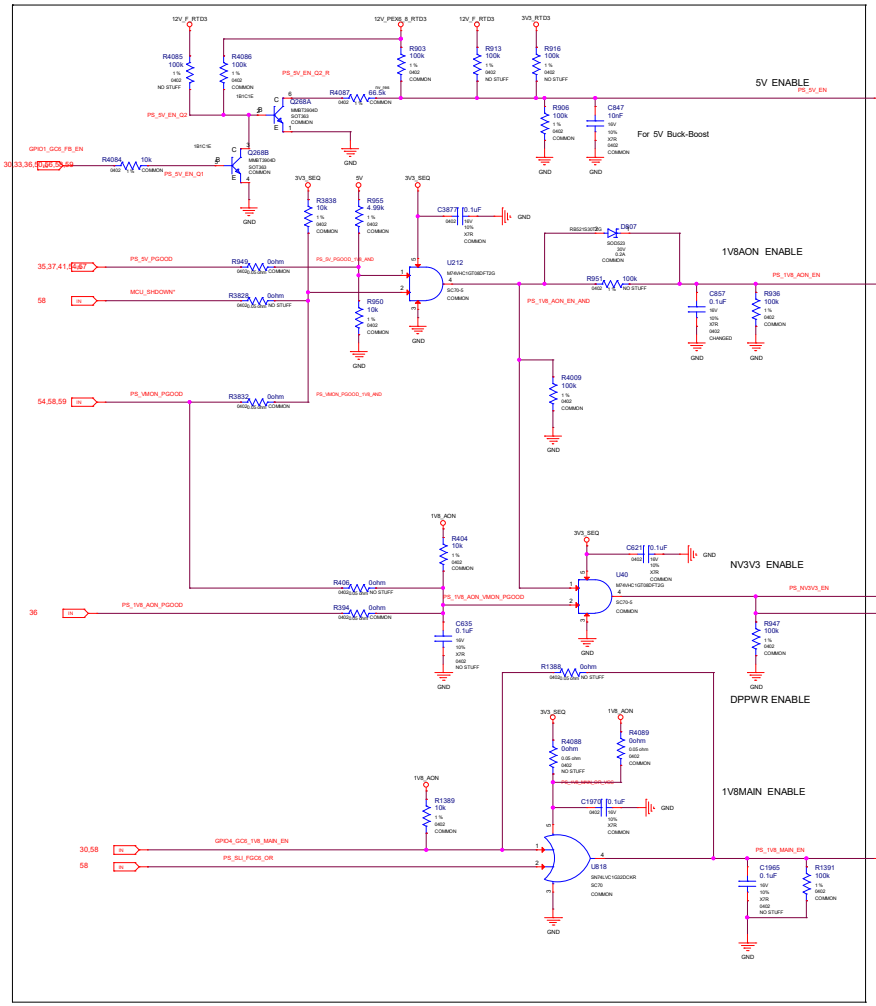
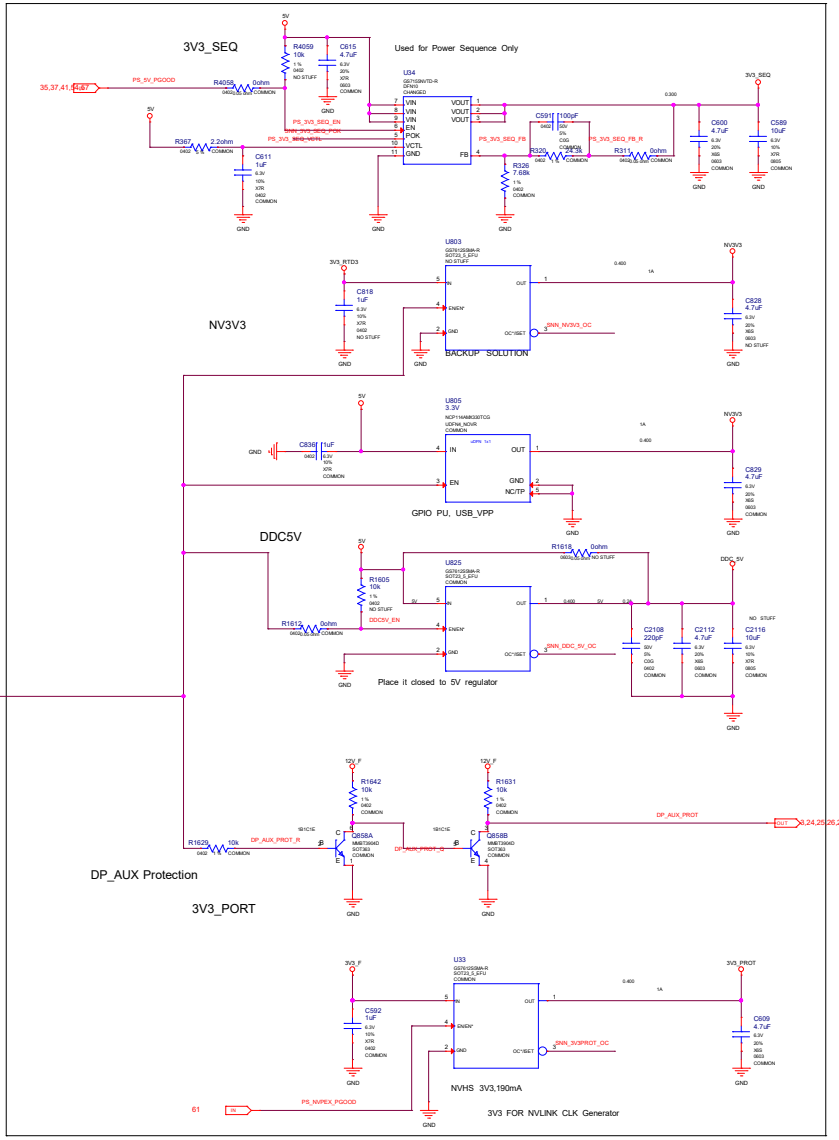
SEQUENCE:5V,1V8,NV3V3 ENABLE





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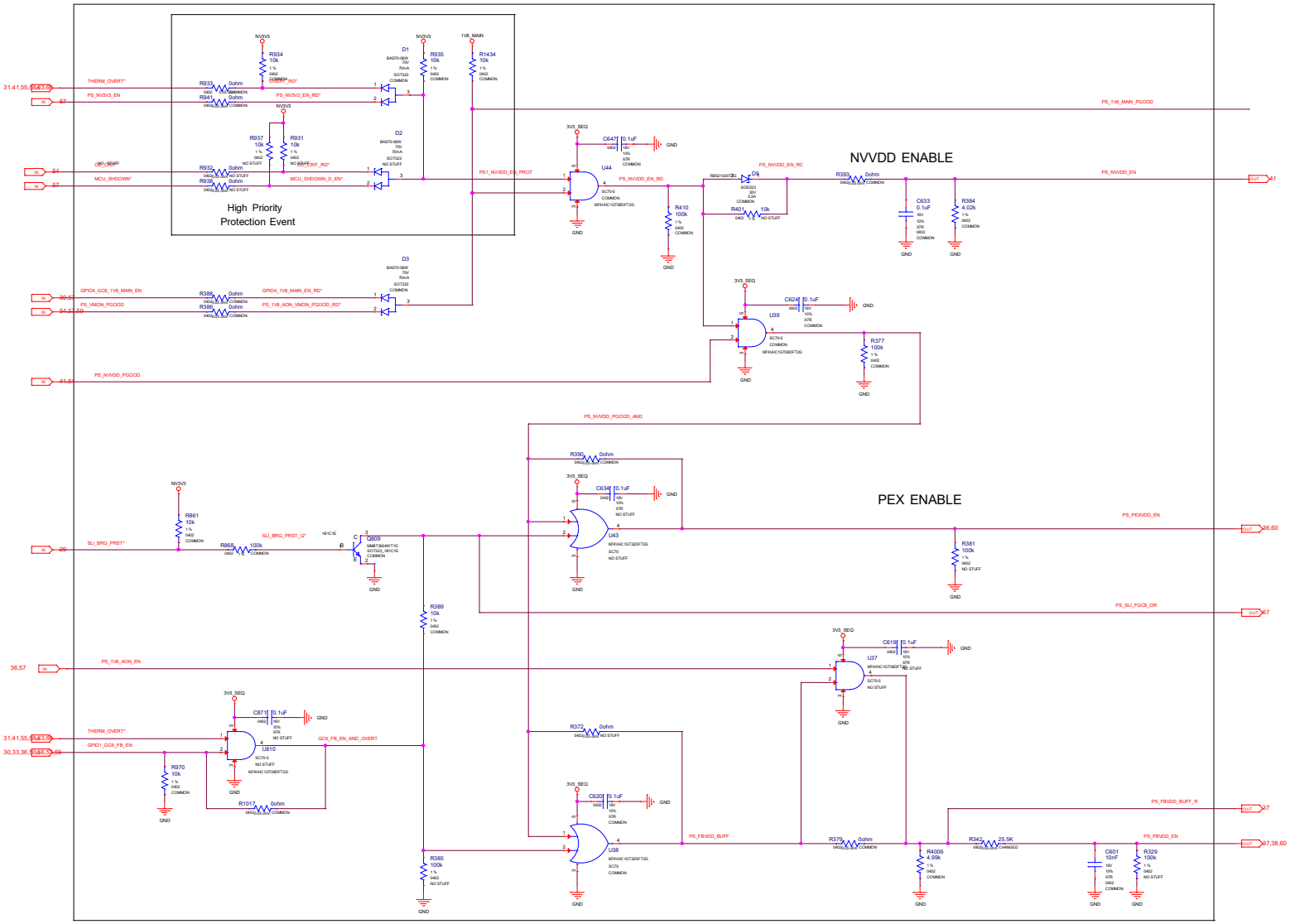
SEQUENCE:NV,PEX,FB ENABLE



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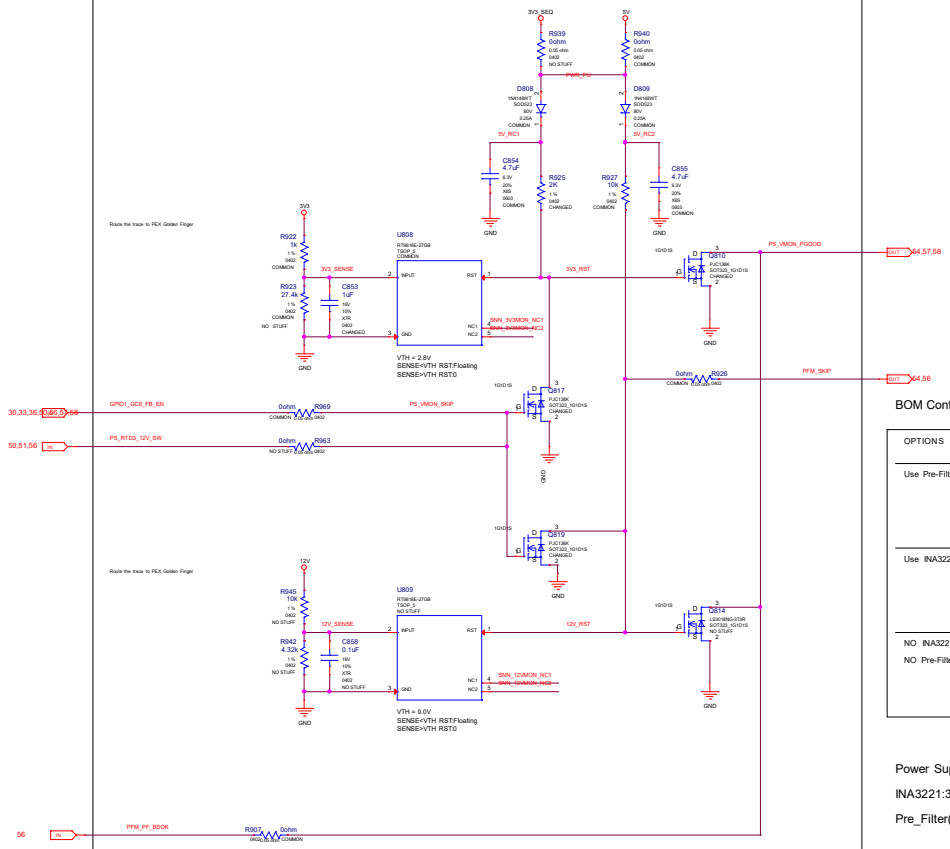
SEQUENCE:PCIE Voltage Monitor

PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL Sequence: PCIE Voltage Monitor

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

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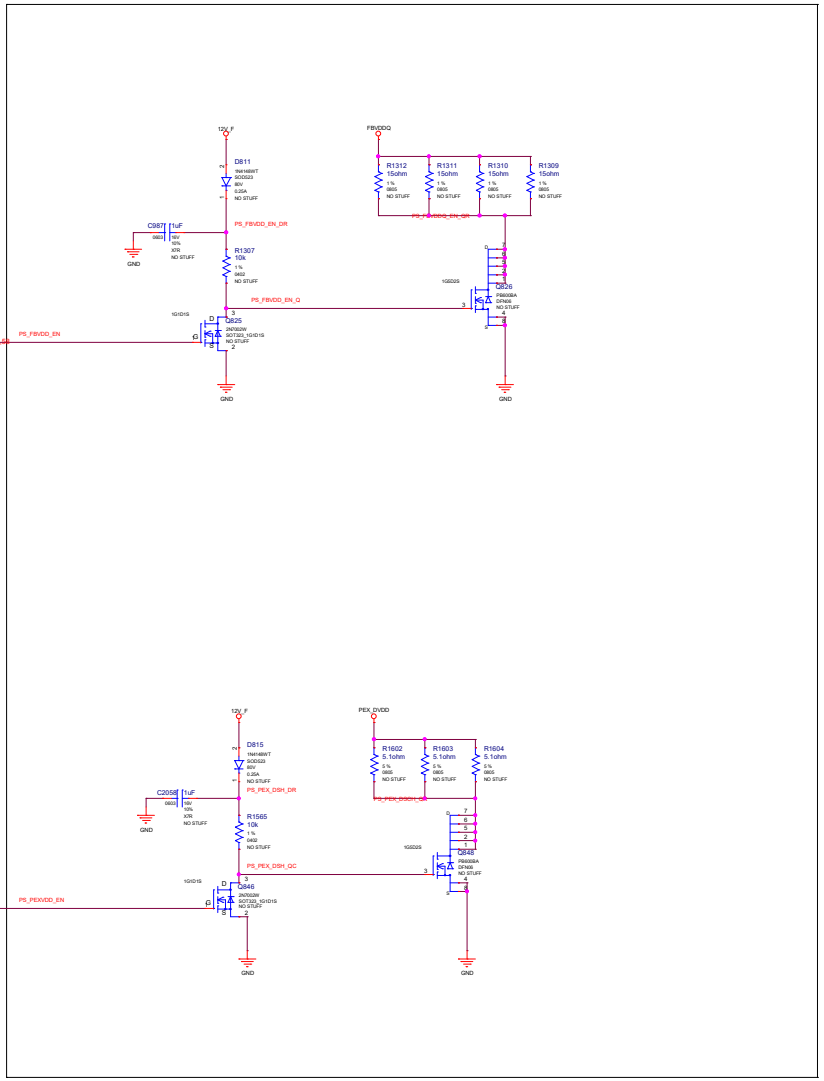
SEQUENCE:Discharge



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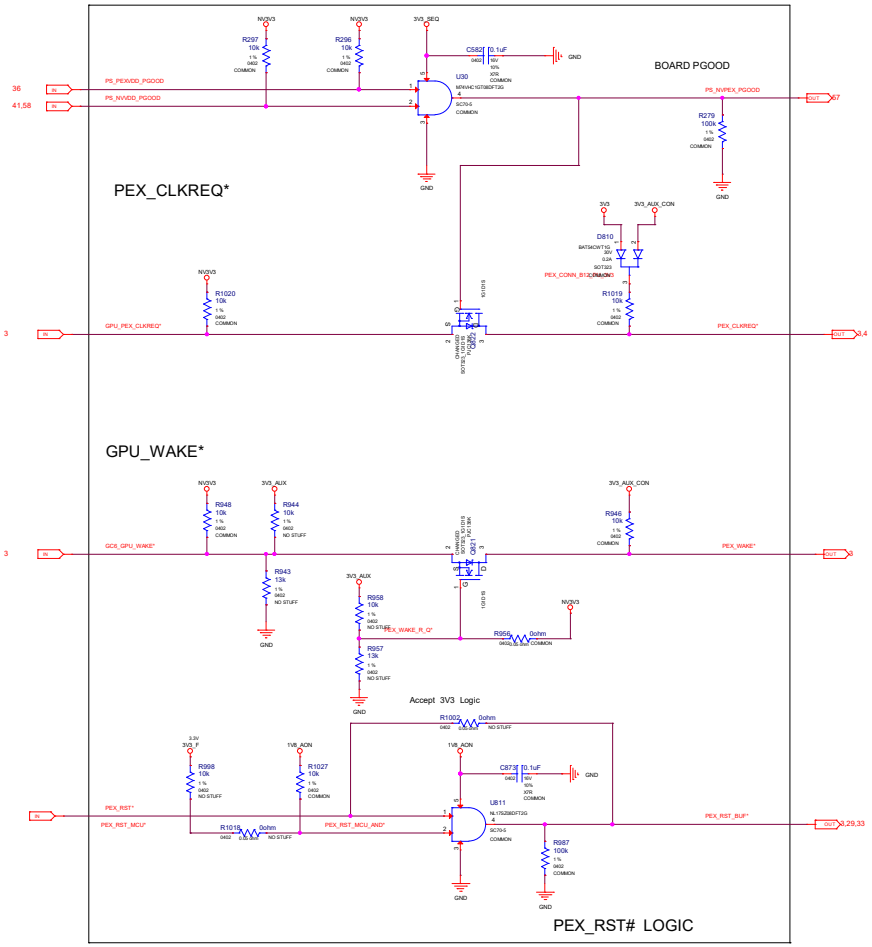
SEQUENCE:MISC



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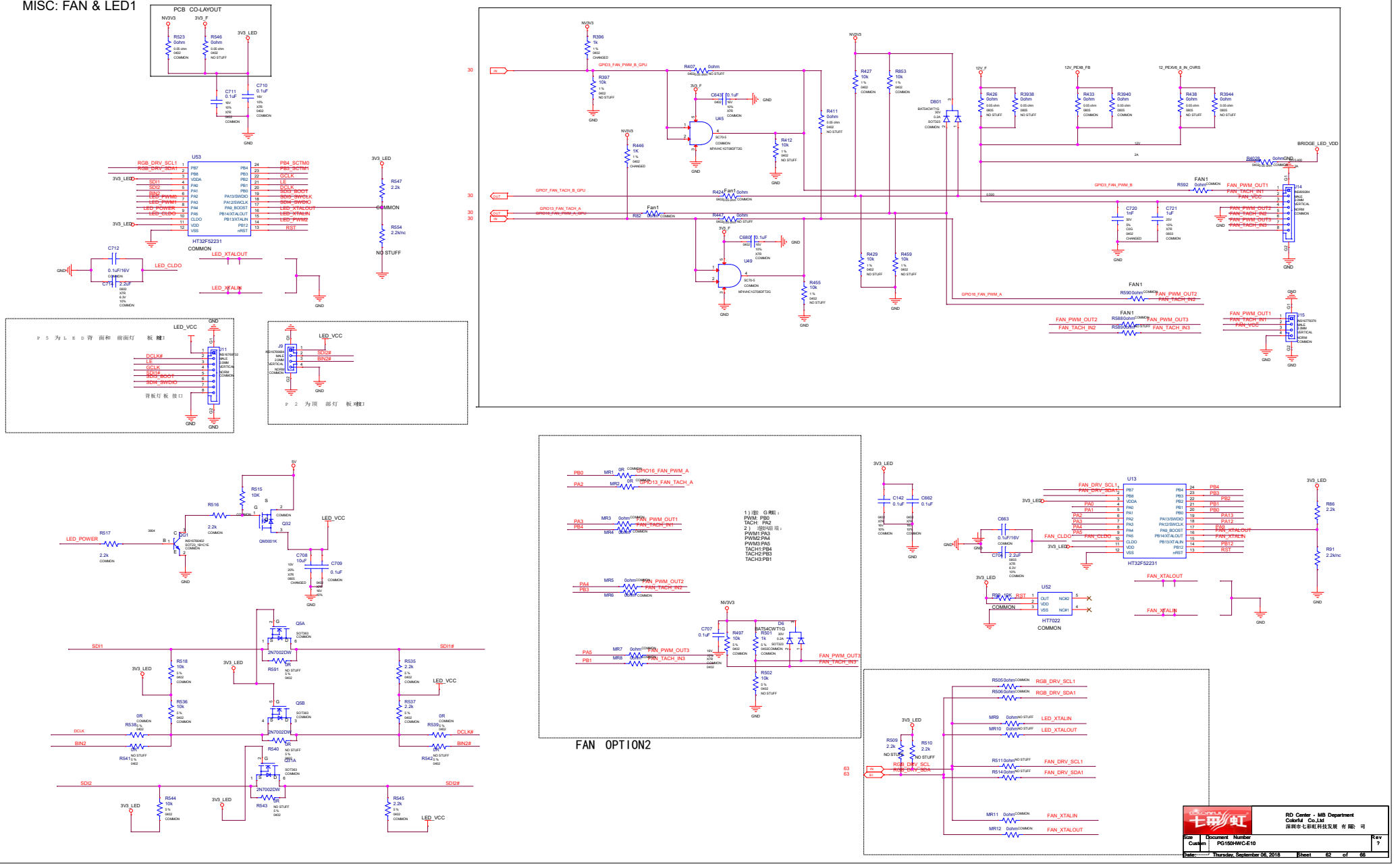
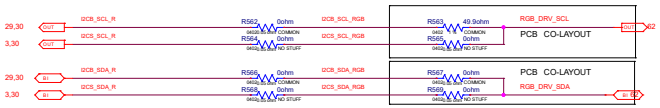
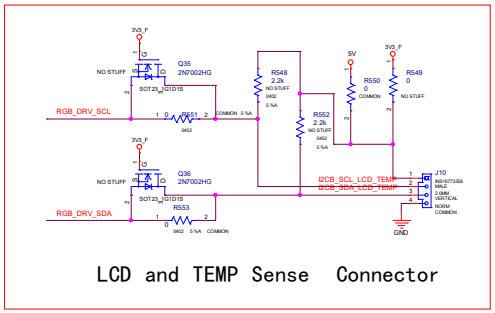
MISC: FAN & LED1

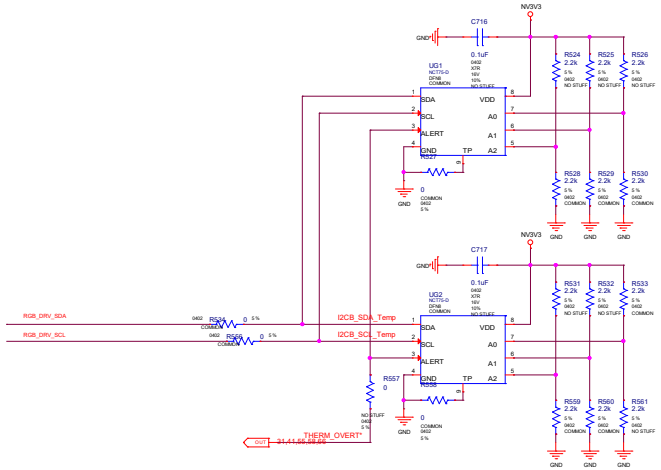




8-bit I2C Address of MCU on Daughter Board: TBD



LCD and TEMP Sense Connector



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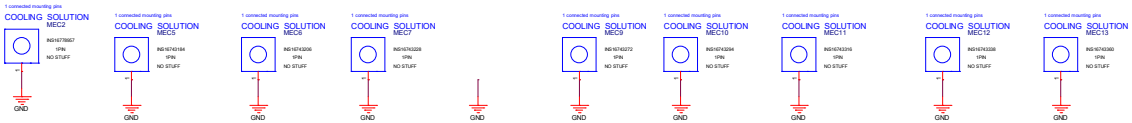
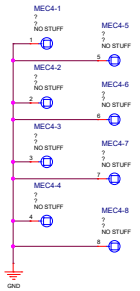
ZERO IDLE POWER MCU

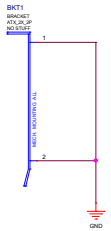
Mechanical: Bracket/Thermal Solution



GPU Mounting holes



Brackets:



Bracket Screw

Back Cover

GPU Stiffner back side

GPU Socket Symbol

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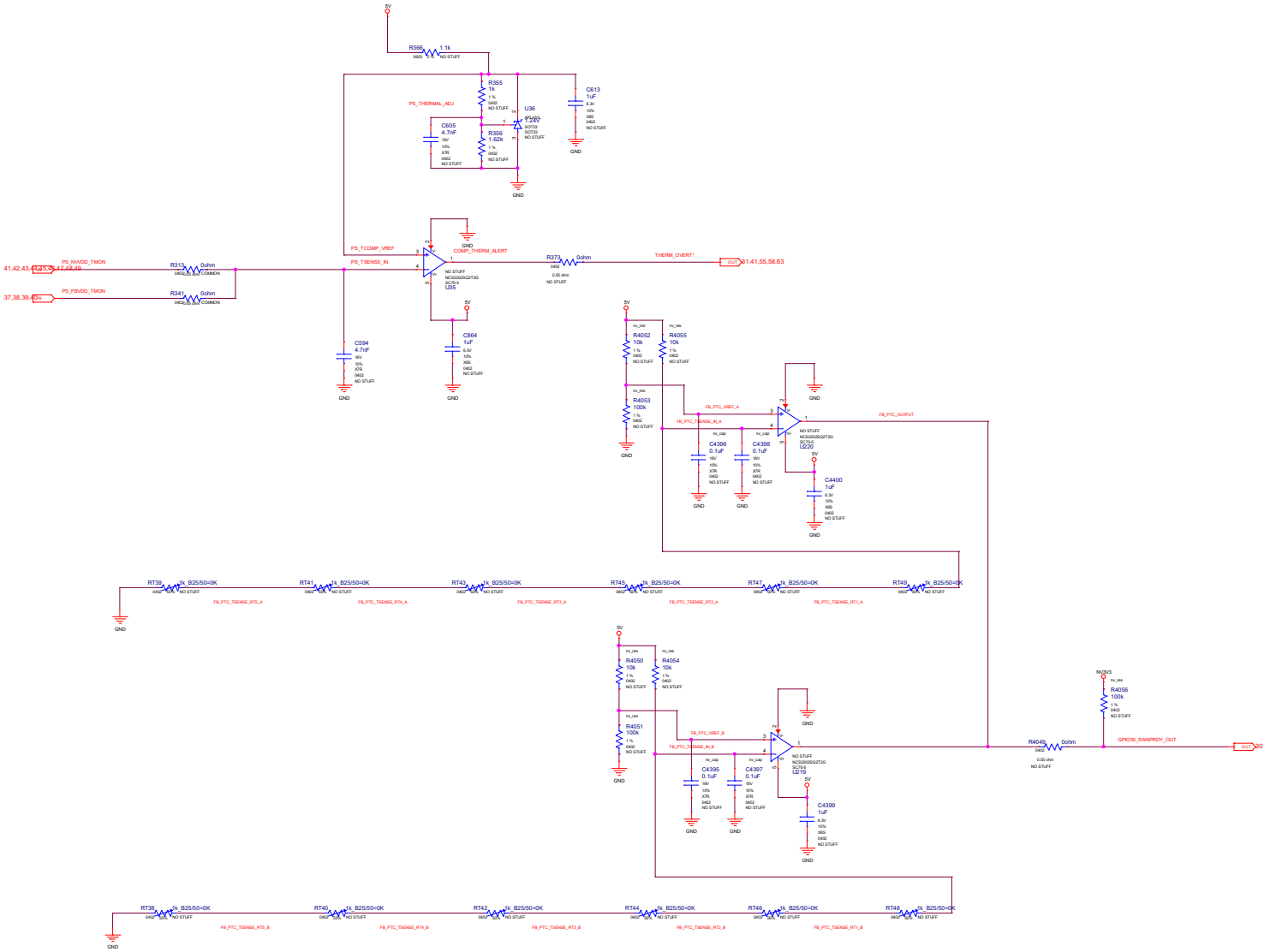
VR THERMAL PROTECTION



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