<Variant Name>

Title

PCI-E RV380/370 256M pterm TSOP V-VV-DI

Schematic No.

105-A334xx-00C

Date:

Tuesday, April 06, 2004

REVISION HISTORY

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	11-24-03	PRELIMINARY BASED ON 105-A297xx-00A 03-11-24 - (pg 02) Swap DVI DDC clock and data lines
1	00B	12-29-03	- (pg 07) Add R1043 for power dissipation - (Layout) Move C284, blocking Grantsdale PCIE connector latch
2	00C	03-09-04	- (Layout) Move fan connector to shorten fan power wire - (Layout) Correct C151 overlap - (pg02) Fix pull-up +VDD_DVO to +VDDR4 - (pg04) Remove CP2, 3, 4, 5, 6 and 8 for dual footprint manufacturing issues (Capacitor packs sharing with 402 footprints) - (pg05) Remove dual-package FET for VDDC - (pg06) Remove C986, C987, C988, C989, C990, C991, C992 and C993) - (pg06) Change R297 to 1206 footprint - (pg07) Add MC917 as multi-footprint for C917, remove L3 (redundant option) - (pg13, 15) +5V supply with current limiting for VESA DDC spec, remove F1, B21

PCI-EXPRESS EDGE CONNECTOR

+12V_BUS C5 100uF_16V DNI

+3.3V_BUS C8 100uF_16V >=6.3V

+3.3V_BUS C2 47uF_16V >=6.3V DNI

USE 47uF TANTALUM CAPACITOR OR HIGHER

GND_AVSSN GND_MPVSS GND_TPVSS GND_A2VSSN GND_AVSSQ GND_RSET
GND_PVSS GND_TXVSSR GND_A2VSSQ GND_R2SET

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

MPCI1

B1	+12V#B1	PRSNT1#A1	A1
B2	+12V#B2	+12V#A2	A2
B3	RSVD#B3	+12V#A3	A3
B4	GND#B4	GND#A4	A4
B5	SMCLK	JTAG2	A5
B6	SMDAT	JTAG3	A6
B7	GND#B7	JTAG4	A7
B8	+3.3V#B8	JTAG5	A8
B9	JTAG1	+3.3V#A9	A9
B10	3.3Vaux	+3.3V#A10	A10
B11	WAKE#	PERST#	A11
	Mechanical Key		
B12	RSVD#B12	GND#A12	A12
B13	GND#B13	REFCLK+	A13
B14	PETp0	REFCLK-	A14
B15	PETn0	GND#A15	A15
B16	GND#B16	PERp0	A16
B17	PRSNT2#B17	PERn0	A17
B18	GND#B18	GND#A18	A18
	End of the x1 Connector		
B19	PETp1	RSVD#A19	A19
B20	PETn1	GND#A20	A20
B21	GND#B21	PERp1	A21
B22	GND#B22	PERn1	A22
B23	PETp2	GND#A23	A23
B24	PETn2	GND#A24	A24
B25	GND#B25	PERp2	A25
B26	GND#B26	PERn2	A26
B27	PETp3	GND#A27	A27
B28	PETn3	GND#A28	A28
B29	GND#B27	PERp3	A29
B30	RSVD#B30	PERn3	A30
B31	PRSNT2#B31	GND#A31	A31
B32	GND#B32	RSVD#A32	A32
	End of the x4 Connector		
B33	PETp4	RSVD#A33	A33
B34	PETn4	GND#A34	A34
B35	GND#B35	PERp4	A35
B36	GND#B36	PERn4	A36
B37	PETp5	GND#A37	A37
B38	PETn5	GND#A38	A38
B39	GND#B39	PERp5	A39
B40	GND#B40	PERn5	A40
B41	PETp6	GND#A41	A41
B42	PETn6	GND#A42	A42
B43	GND#B43	PERp6	A43
B44	GND#B44	PERn6	A44
B45	PETp7	GND#A45	A45
B46	PETn7	GND#A46	A46
B47	GND#B47	PERp7	A47
B48	PRSNT2#B48	PERn7	A48
B49	GND#B49	GND#A49	A49
	End of the x8 Connector		
B50	PETp8	RSVD#A50	A50
B51	PETn8	GND#A51	A51
B52	GND#B52	PERp8	A52
B53	GND#B53	PERn8	A53
B54	PETp9	GND#A54	A54
B55	PETn9	GND#A55	A55
B56	GND#B56	PERp9	A56
B57	GND#B57	PERn9	A57
B58	PETp10	GND#A58	A58
B59	PETn10	GND#A59	A59
B60	GND#B60	PERp10	A60
B61	GND#B61	PERn10	A61
B62	PETp11	GND#A62	A62
B63	PETn11	GND#A63	A63
B64	GND#B64	PERp11	A64
B65	GND#B65	PERn11	A65
B66	PETp12	GND#A66	A66
B67	PETn12	GND#A67	A67
B68	GND#B68	PERp12	A68
B69	GND#B69	PERn12	A69
B70	PETp13	GND#A70	A70
B71	PETn13	GND#A71	A71
B72	GND#B72	PERp13	A72
B73	GND#B73	PERn13	A73
B74	PETp14	GND#A74	A74
B75	PETn14	GND#A75	A75
B76	GND#B76	PERp14	A76
B77	GND#B77	PERn14	A77
B78	PETp15	GND#A78	A78
B79	PETn15	GND#A79	A79
B80	GND#B80	PERp15	A80
B81	PRSNT2#B81	PERn15	A81
B82	RSVD#B82	GND#A82	A82

x16 PCIe EDGE CONNECTOR REV1.0a

+12V_BUS +3.3V_BUS

(2,13) A_HSYNC_DAC1 — R1008 0R 402 DNI — JTAG_TRST#

PRESENT_NULL

PRESENCE — 0R R1244

JTAG_TCK RP194A 8 1 0R DNI — A_VSYNC_DAC1 (2,13)
JTAG_TDI RP194B 7 2 0R DNI — CRT1DDCDATA (2,13)
JTAG_TDO RP194C 6 3 0R DNI — SCL (2,17)
JTAG_TMS RP194D 5 4 0R DNI — CRT1DDCCLK (2,13)

+5V — C972 100nF 402

PERST# — U2 TC7SZ08FU — R3 100R — PERST#_buf (2,16)

R4 180R 402

R64 402 0R

TP26 TP27 — PCIE_REFCLKP (2) / PCIE_REFCLKN (2)

(2) PETp0_GFXRp0 / (2) PETn0_GFXRn0	TP28 / TP29	PERp0 / PERn0	C607 / C608 100nF
(2) PETp1_GFXRp1 / (2) PETn1_GFXRn1	TP30 / TP31	PERp1 / PERn1	C617 / C618 100nF
(2) PETp2_GFXRp2 / (2) PETn2_GFXRn2	TP32 / TP33	PERp2 / PERn2	C626 / C627 100nF
(2) PETp3_GFXRp3 / (2) PETn3_GFXRn3	TP34 / TP35	PERp3 / PERn3	C631 / C632 100nF
(2) PETp4_GFXRp4 / (2) PETn4_GFXRn4	TP36 / TP37	PERp4 / PERn4	C611 / C612 100nF
(2) PETp5_GFXRp5 / (2) PETn5_GFXRn5	TP38 / TP39	PERp5 / PERn5	C622 / C623 100nF
(2) PETp6_GFXRp6 / (2) PETn6_GFXRn6	TP40 / TP41	PERp6 / PERn6	C621 / C630 100nF
(2) PETp7_GFXRp7 / (2) PETn7_GFXRn7	TP42 / TP43	PERp7 / PERn7	C605 / C606 100nF
(2) PETp8_GFXRp8 / (2) PETn8_GFXRn8	TP44 / TP45	PERp8 / PERn8	C615 / C616 100nF
(2) PETp9_GFXRp9 / (2) PETn9_GFXRn9	TP46 / TP47	PERp9 / PERn9	C624 / C625 100nF
(2) PETp10_GFXRp10 / (2) PETn10_GFXRn10	TP48 / TP49	PERp10 / PERn10	C633 / C634 100nF
(2) PETp11_GFXRp11 / (2) PETn11_GFXRn11	TP50 / TP51	PERp11 / PERn11	C609 / C610 100nF
(2) PETp12_GFXRp12 / (2) PETn12_GFXRn12	TP52 / TP53	PERp12 / PERn12	C619 / C620 100nF
(2) PETp13_GFXRp13 / (2) PETn13_GFXRn13	TP54 / TP55	PERp13 / PERn13	C628 / C629 100nF
(2) PETp14_GFXRp14 / (2) PETn14_GFXRn14	TP56 / TP57	PERp14 / PERn14	C603 / C604 100nF
(2) PETp15_GFXRp15 / (2) PETn15_GFXRn15	TP58 / TP59	PERp15 / PERn15	C613 / C614 100nF

GFXTp0_PERp0 (2) / GFXTn0_PERn0 (2)	GFXTp1_PERp1 (2) / GFXTn1_PERn1 (2)
GFXTp2_PERp2 (2) / GFXTn2_PERn2 (2)	GFXTp3_PERp3 (2) / GFXTn3_PERn3 (2)
GFXTp4_PERp4 (2) / GFXTn4_PERn4 (2)	GFXTp5_PERp5 (2) / GFXTn5_PERn5 (2)
GFXTp6_PERp6 (2) / GFXTn6_PERn6 (2)	GFXTp7_PERp7 (2) / GFXTn7_PERn7 (2)
GFXTp8_PERp8 (2) / GFXTn8_PERn8 (2)	GFXTp9_PERp9 (2) / GFXTn9_PERn9 (2)
GFXTp10_PERp10 (2) / GFXTn10_PERn10 (2)	GFXTp11_PERp11 (2) / GFXTn11_PERn11 (2)
GFXTp12_PERp12 (2) / GFXTn12_PERn12 (2)	GFXTp13_PERp13 (2) / GFXTn13_PERn13 (2)
GFXTp14_PERp14 (2) / GFXTn14_PERn14 (2)	GFXTp15_PERp15 (2) / GFXTn15_PERn15 (2)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

ATI Technologies Inc.
1 Commerce Valley Drive East
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Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI		
Size C	Document Number 105-A334xx-00C		Rev 2
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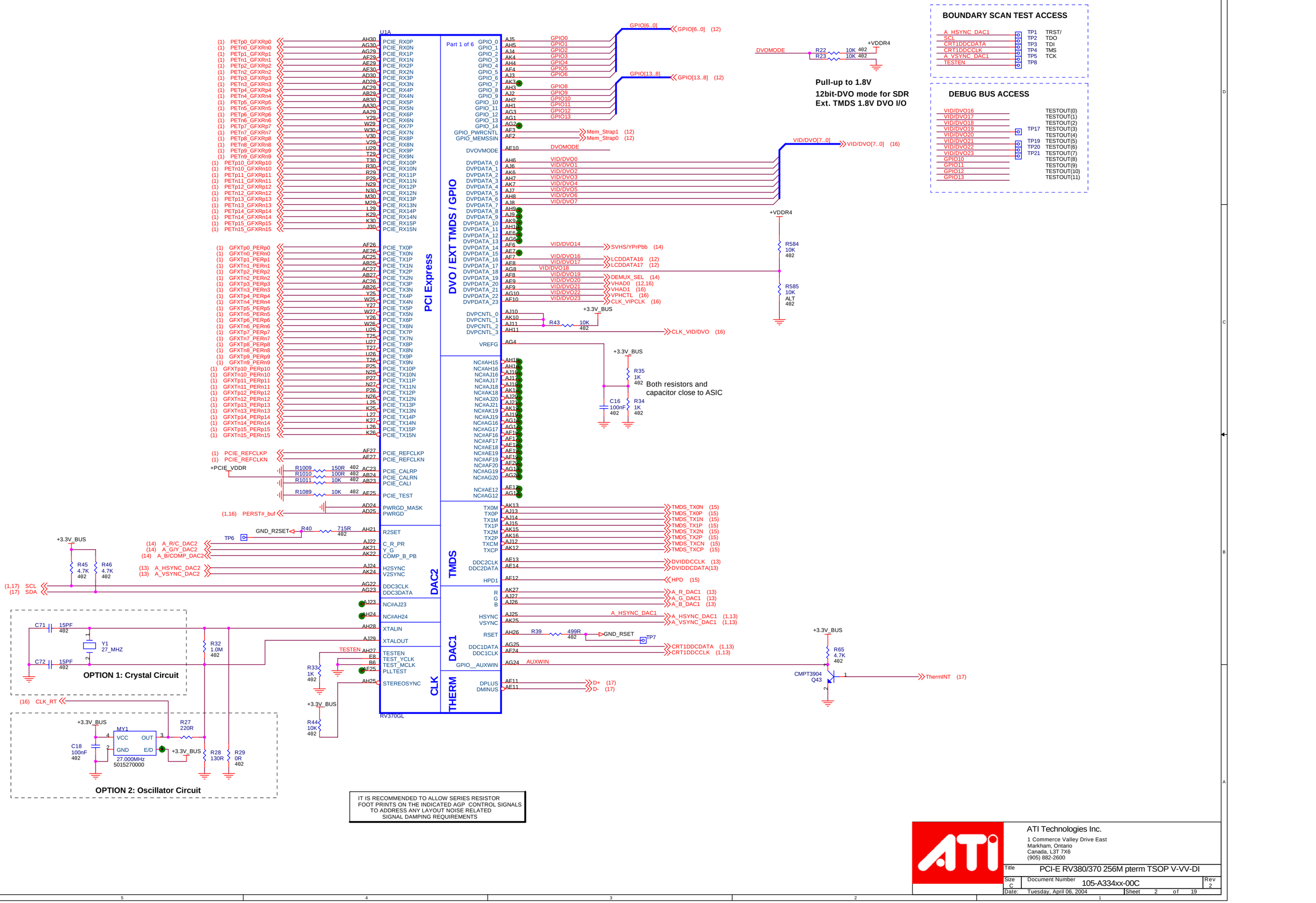
U1A
Part 1 of 6
PCI Express
DVO / EXT TMDS / GPIO
DAC2
TMDS
DAC1
CLK
THERM
RV370GL
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
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PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
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PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CALRP
PCIE_CALRN
PCIE_CALI
PCIE_TEST
PWRGD_MASK
PWRGD
R2SET
C_R_PR
Y_G
COMP_B_PB
H2SYNC
V2SYNC
DDC3CLK
DDC3DATA
NC#AJ23
NC#AH24
XTALIN
XTALOUT
TESTEN
TEST_YCLK
TEST_MCLK
PLLTEST
STEREOSYNC
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_PWRCNTL
GPIO_MEMSSIN
DVOVMODE
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_3
VREFG
NC#AH15
NC#AH16
NC#AJ16
NC#AJ17
NC#AJ18
NC#AK18
NC#AJ20
NC#AJ21
NC#AK19
NC#AJ19
NC#AG16
NC#AG17
NC#AF16
NC#AF17
NC#AE18
NC#AE19
NC#AF19
NC#AF20
NC#AG19
NC#AG20
NC#AE12
NC#AG12
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TXCM
TXCP
DDC2CLK
DDC2DATA
HPD1
R
G
B
HSYNC
VSYNC
RSET
DDC1DATA
DDC1CLK
GPIO_AUXWIN
DPLUS
DMINUS
GPIO[6..0]
GPIO[13..8]
Mem_Strap1
Mem_Strap0
VID/DVO0
VID/DVO1
VID/DVO2
VID/DVO3
VID/DVO4
VID/DVO5
VID/DVO6
VID/DVO7
VID/DVO14
VID/DVO16
VID/DVO17
VID/DVO18
VID/DVO19
VID/DVO20
VID/DVO21
VID/DVO22
VID/DVO23
VID/DVO[7..0]
SVHS/YPrPbb
LCDDATA16
LCDDATA17
DEMUX_SEL
VHAD0
VHAD1
VPHCTL
CLK_VIPCLK
CLK_VID/DVO
TMDS_TX0N
TMDS_TX0P
TMDS_TX1N
TMDS_TX1P
TMDS_TX2N
TMDS_TX2P
TMDS_TXCN
TMDS_TXCP
DVIDDCCLK
DVIDDCDATA
HPD
A_R_DAC1
A_G_DAC1
A_B_DAC1
A_HSYNC_DAC1
A_VSYNC_DAC1
CRT1DDCDATA
CRT1DDCCLK
AUXWIN
D+
D-
+3.3V_BUS
+VDDR4
R584 10K 402
R585 10K ALT 402
R43 10K 402
R35 1K 402
R34 1K 402
C16 100nF 402
Both resistors and capacitor close to ASIC
DVOMODE
R22 10K 402
R23 10K 402
Pull-up to 1.8V
12bit-DVO mode for SDR
Ext. TMDS 1.8V DVO I/O
BOUNDARY SCAN TEST ACCESS
A_HSYNC_DAC1
SCL
CRT1DDCDATA
CRT1DDCCLK
A_VSYNC_DAC1
TESTEN
TP1 TRST/
TP2 TDO
TP3 TDI
TP4 TMS
TP5 TCK
TP8
DEBUG BUS ACCESS
VID/DVO16
VID/DVO17
VID/DVO18
VID/DVO19
VID/DVO20
VID/DVO21
VID/DVO22
VID/DVO23
GPIO10
GPIO11
GPIO12
GPIO13
TP17
TP19
TP20
TP21
TESTOUT(0)
TESTOUT(1)
TESTOUT(2)
TESTOUT(3)
TESTOUT(4)
TESTOUT(5)
TESTOUT(6)
TESTOUT(7)
TESTOUT(8)
TESTOUT(9)
TESTOUT(10)
TESTOUT(11)
+PCIE_VDDR
R1009 150R 402
R1010 100R 402
R1011 10K 402
R1089 10K 402
PERST#_buf
GND_R2SET
R40 715R 402
TP6
A_R/C_DAC2
A_G/Y_DAC2
A_B/COMP_DAC2
A_HSYNC_DAC2
A_VSYNC_DAC2
SCL
SDA
R45 4.7K 402
R46 4.7K 402
C71 15PF 402
C72 15PF 402
Y1 27_MHZ
R32 1.0M 402
OPTION 1: Crystal Circuit
CLK_RT
MY1
VCC
OUT
GND
E/D
27.000MHz
5015270000
C18 100nF 402
R27 220R
R28 130R
R29 0R 402
OPTION 2: Oscillator Circuit
R33 1K 402
R44 10K 402
TP7
GND_RSET
R39 499R 402
R65 4.7K 402
CMPT3904
Q43
ThermINT
IT IS RECOMMENDED TO ALLOW SERIES RESISTOR FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS TO ADDRESS ANY LAYOUT NOISE RELATED SIGNAL DAMPING REQUIREMENTS
ATI Technologies Inc.
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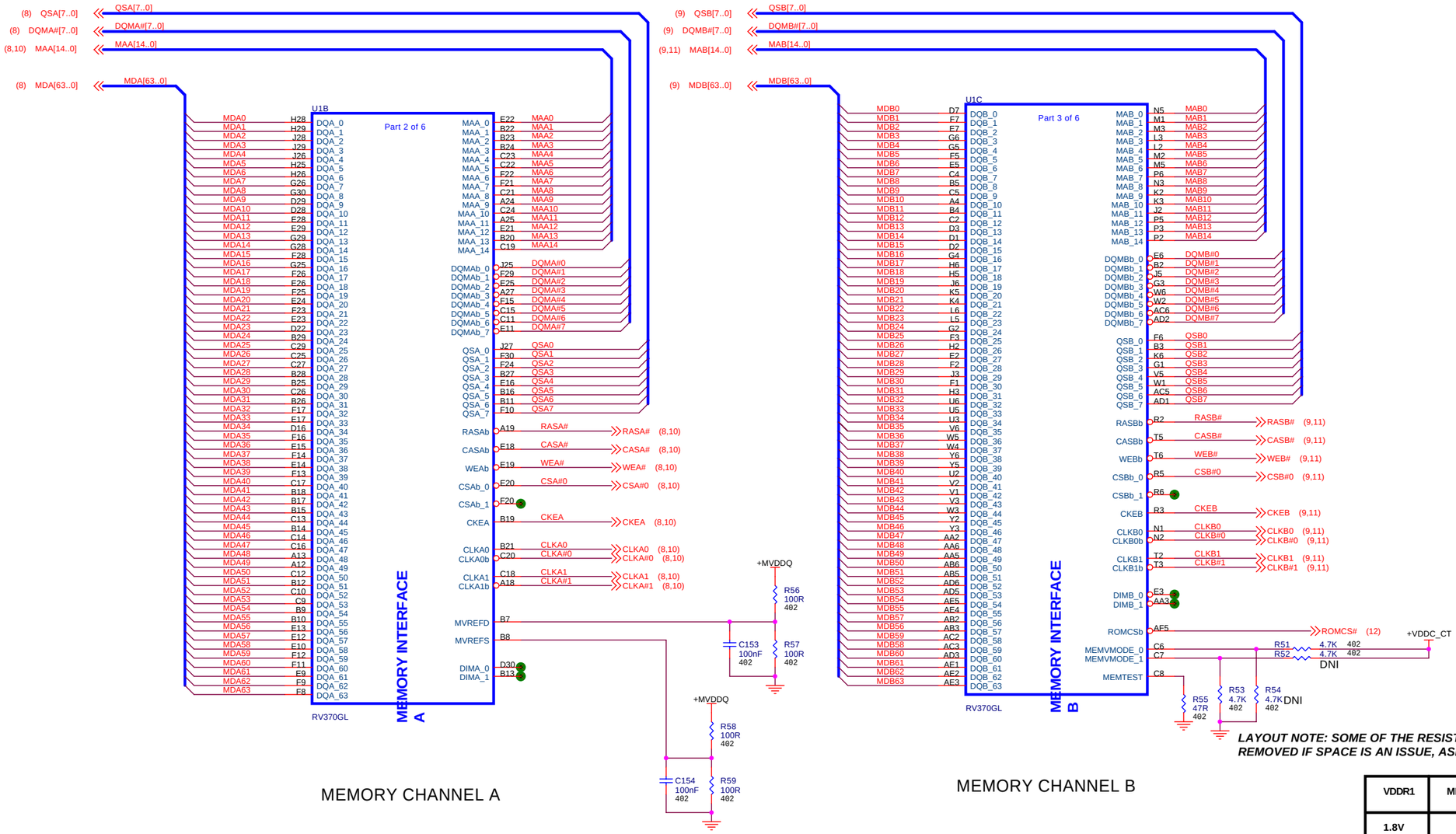

MEMORY CHANNEL A

MEMORY CHANNEL B

PLACE C351/152 VERY CLOSE TO ASIC

R56/57/58/59 CLOSE TO ASIC AS WELL

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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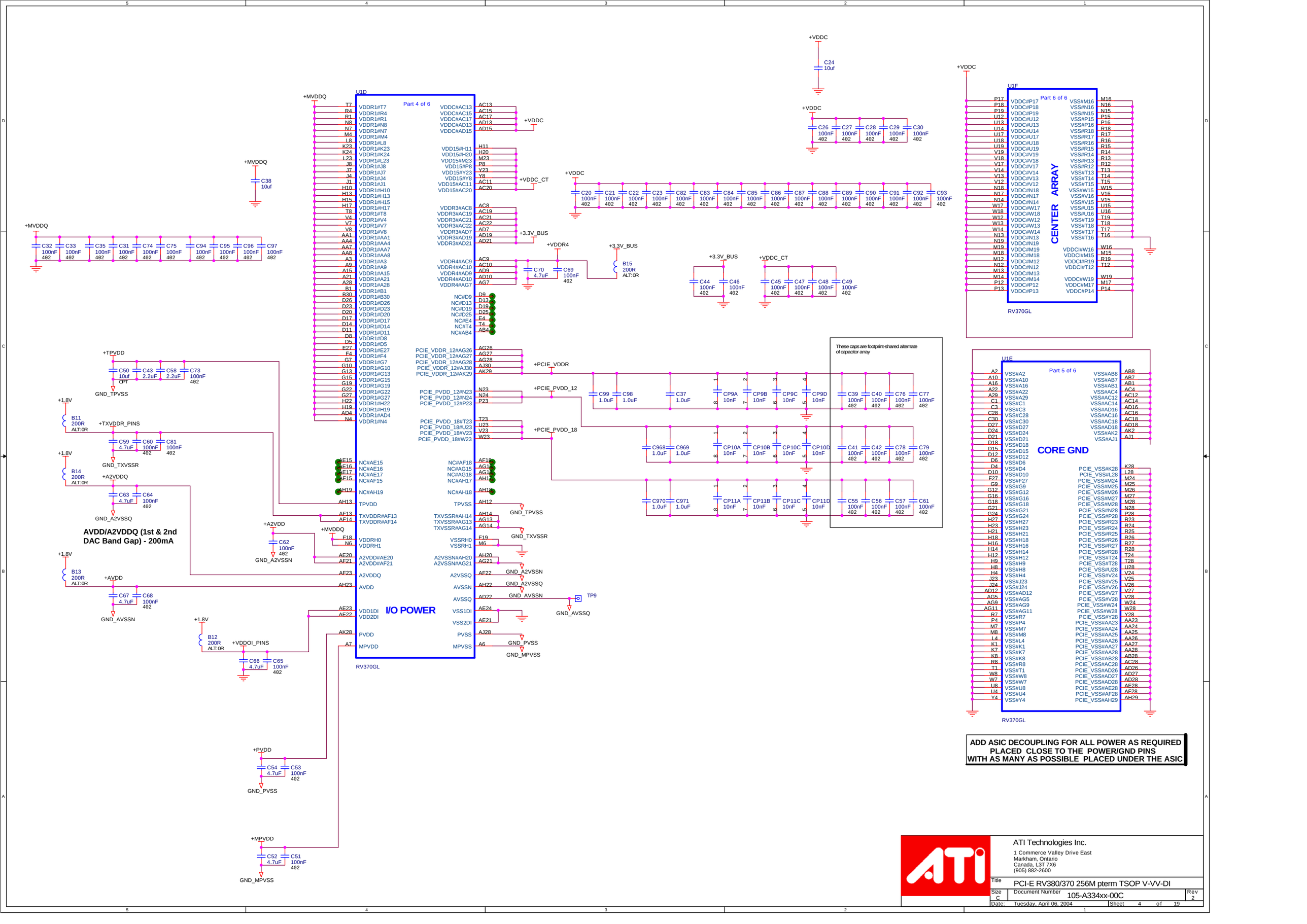
U1D
Part 4 of 6
RV370GL
I/O POWER
U1F
Part 6 of 6
CENTER ARRAY
RV370GL
U1E
Part 5 of 6
CORE GND
RV370GL
These caps are footprint-shared alternate of capacitor array
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
ATI Technologies Inc.
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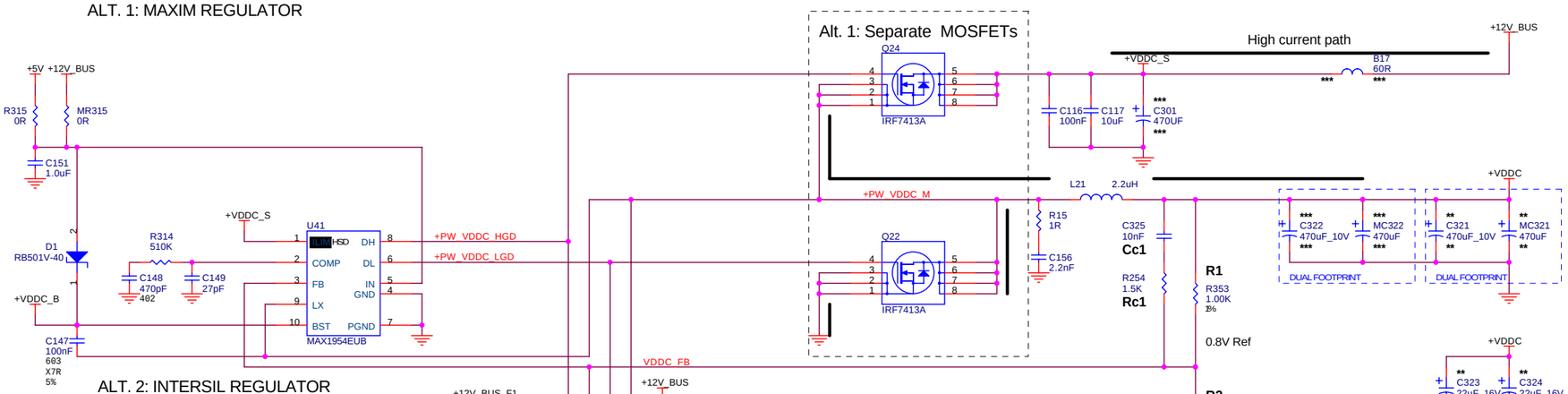
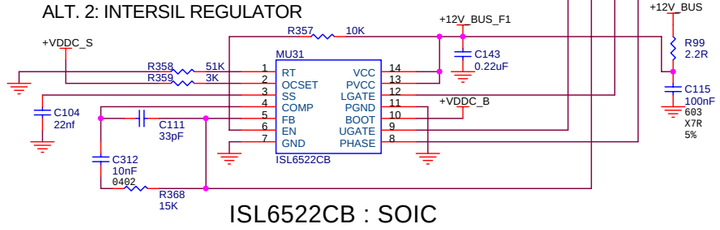
Regulator for VDDC (ASIC Core)

Vout = 1.2V ~ 1.3V

ALT. 1: MAXIM REGULATOR



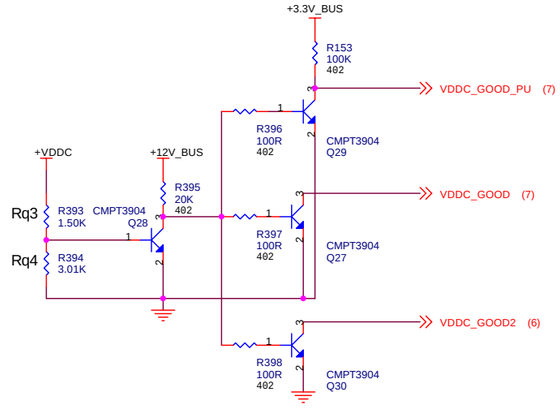
ALT. 2: INTERSIL REGULATOR



ISL6522CB : SOIC

+VDDC — L6 1.8uH ALT:0R — +PCIE_VDDR

+VDDC — L7 1.8uH ALT:0R — +PCIE_PVDD_12



*** Indicate number of power via required for the connection

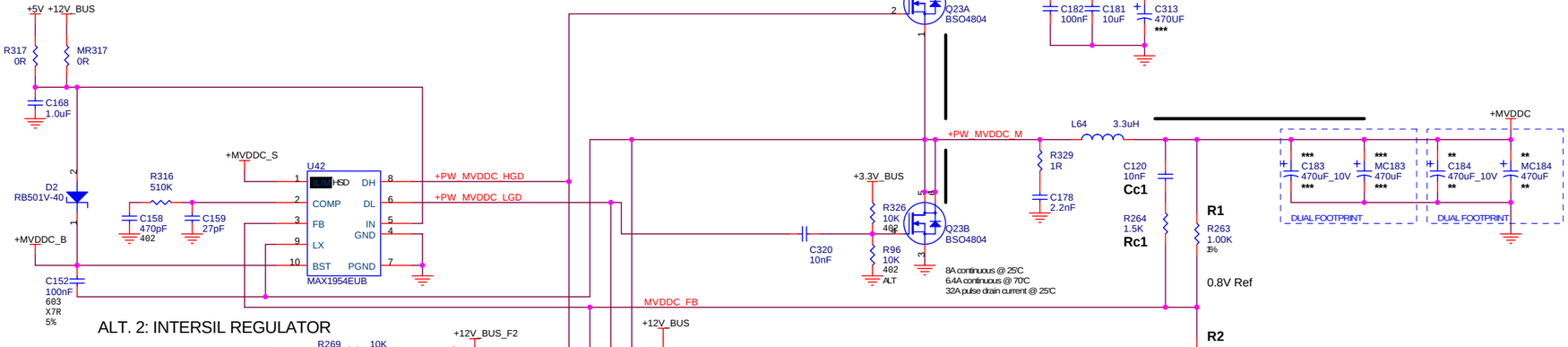
Part	NOTES
MAX1954	Do not install Cc1, Rc1
ISL6522	Install Cc1, Rc1

Part	Vout	R1	R2
MAX1954 ISL6522 0.8V Ref	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100

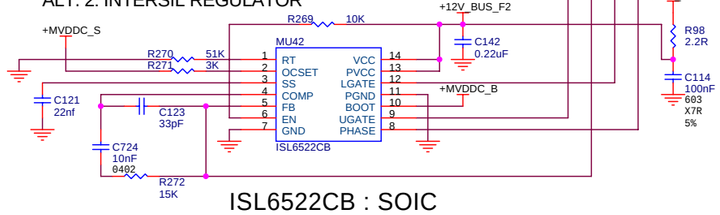
Regulator for MVDDC (Memory Core)

Vout = 2.5V ~ 3.3V

ALT. 1: MAXIM REGULATOR



ALT. 2: INTERSIL REGULATOR



ISL6522CB : SOIC

+VDDC	Rq3	Rq4
+1.3V	1.5K	2.4K
+1.2V	1.5K	3K

Circuit to hold PCI-E voltage low and wait for +VDDC for proper power sequence

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(905) 882-2600

Title	PCI-E RV380/370 256M pterm TSOP V-VV-DI	
Size C	Document Number 105-A334xx-00C	Rev 2
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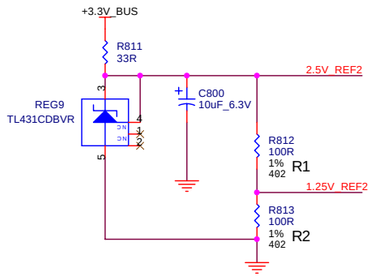
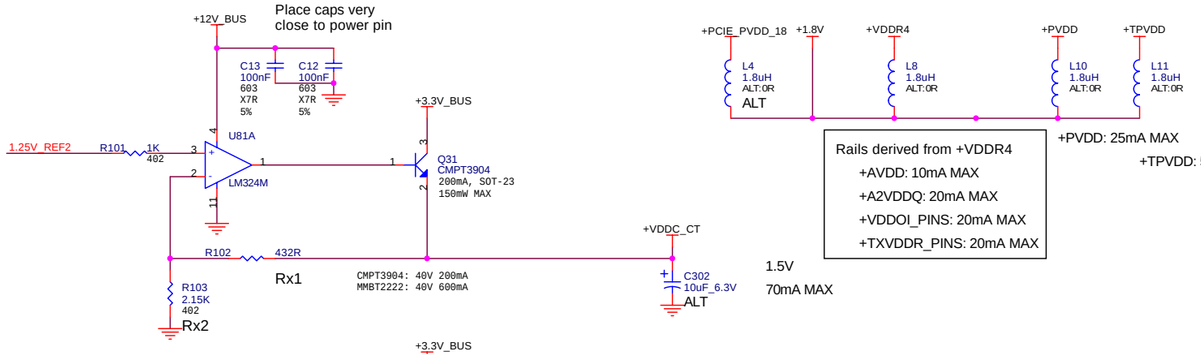


Voltage Req.	R1	R2
0.8V	150R P/N 3160150000 402	71.5R P/N 324075R500
1.25V	100R P/N 3160100000 402	100R P/N 3160100000 402
1.5V	100R P/N 3160100000 402	150R P/N 3160150000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

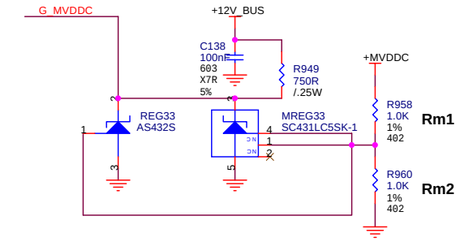
Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240015200

Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.5V	0R P/N 3230000000 603 P/N 3150000000 402	DNI



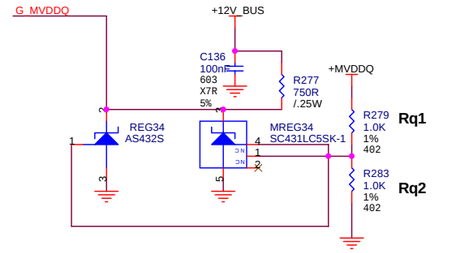
Alt. regulator for +MVDDC
Vout = 2.5V ~ 2.6V
Iout = 500mA MAX

Voltage Req.	Rm1	Rm2
3.34V [-0.04V/+0.04V]	4.32K	2.55K
3.45V [-0.04V/+0.04V]	4.32K	2.43K
2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100



Alt regulator for +MVDDQ
Vout = 2.5V ~ 2.6V
Iout = 200mA MAX

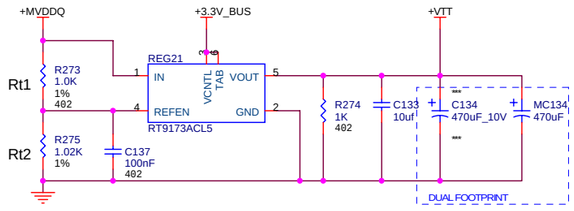
Voltage Req.	Rq1	Rq2
1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
2.5V	1K 3240100100	1K 3240100100
2.6V	4.75K 3240475100	4.32K 3240432100



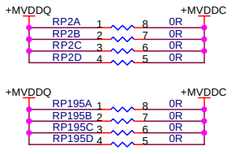
2.5V ~ 2.6V
1A MAX

Regulator for +VTT (Termination)
Vout = 1.25V ~ 1.3V with +2.5V +MVDDQ
Iout = 1000mA MAX

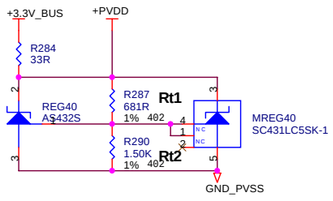
+MVDDQ = +2.5V	Rt1	Rt2
1.25V	1K 3240100100	1K 3240100100
1.3V	1.0K 3240100100 603 3160100100 402	1.02K 3240102100



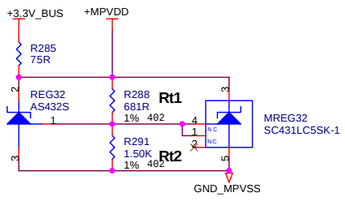
	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100



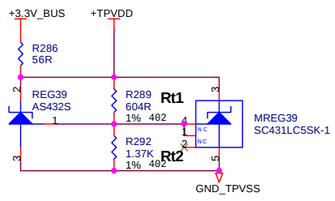
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



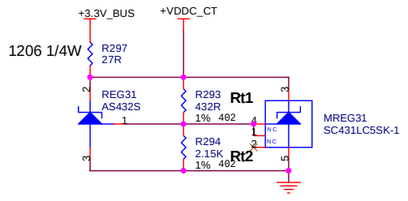
Alt regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX



Alt. regulator for +TPVDD
Vout = 1.65V ~ 1.85V
Iout = 20mA MAX



Alt regulator for +VDDC_CT
Vout = 1.5V
Iout = 70mA MAX



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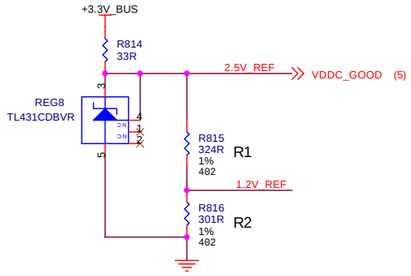
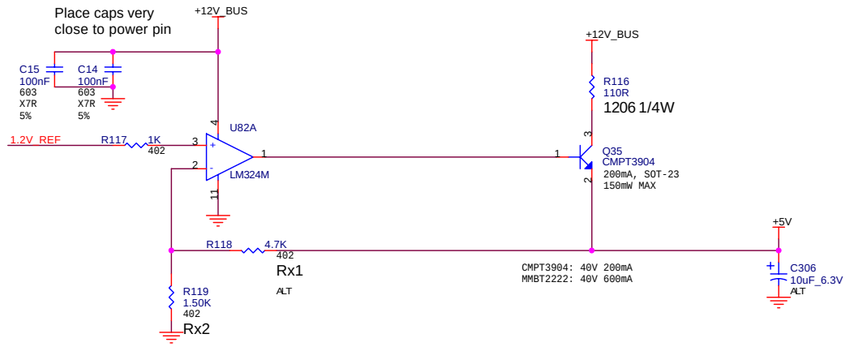
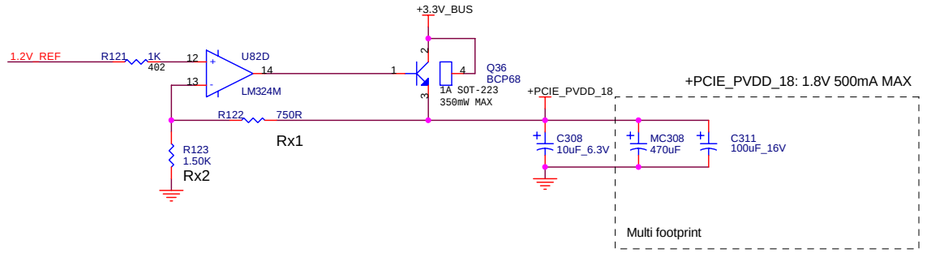
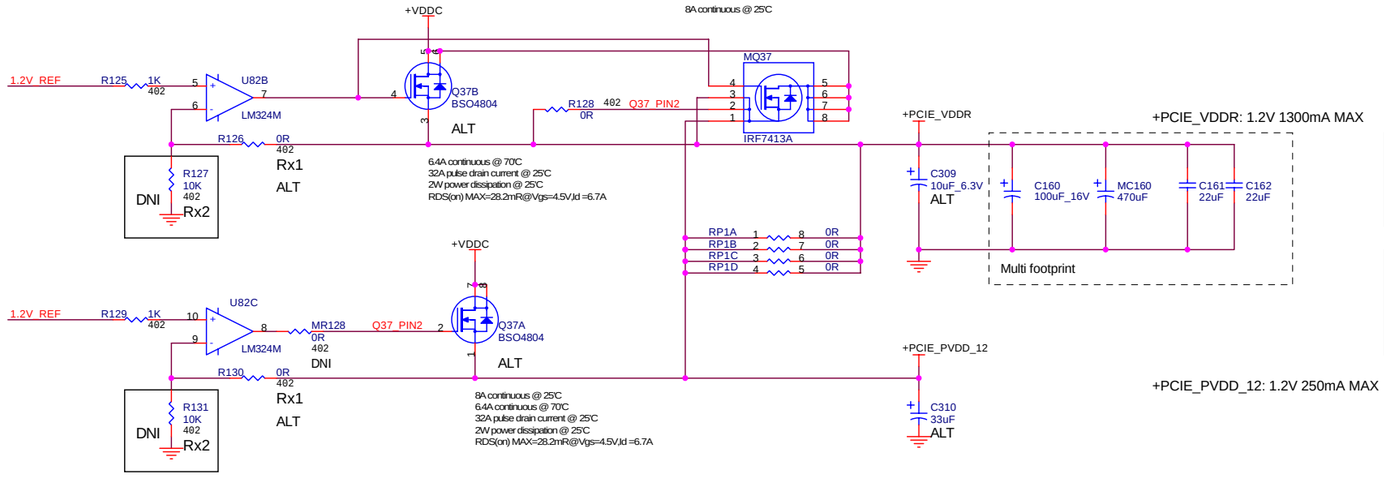
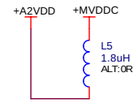




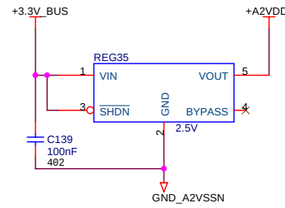




2.5V
120mA

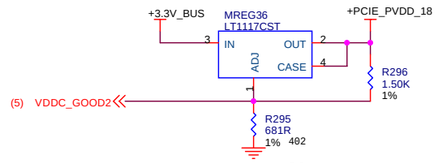


Alt. regulator for +A2VDD
Vout = 2.5V
Iout = 120mA MAX



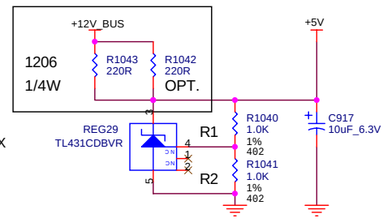
+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.

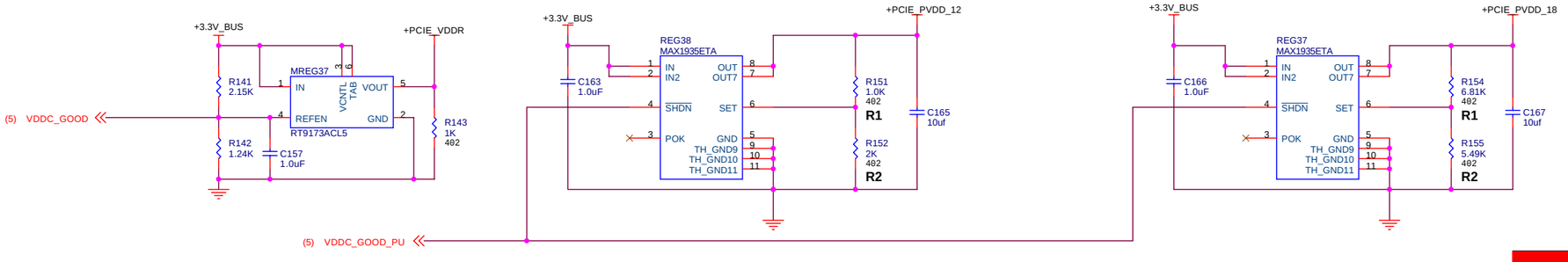
Alt. regulator for PCIE_PVDD_18
Vout = 1.85V
Iout = 500mA MAX



Need at least a 4.7uF output cap for stability

Regulator for +5V
Vout = 5V
Iout = 20mA MAX





Part	Vout	R1	R2
MAX1935 0.8V Ref	1.2V	1.00K 1% 402 ATI P/N 3160100100	2.00K 1% 402 ATI P/N 3160200100
	1.79V	6.81K 1% ATI P/N 3160681100	5.49K 1% 402 ATI P/N 3160549100

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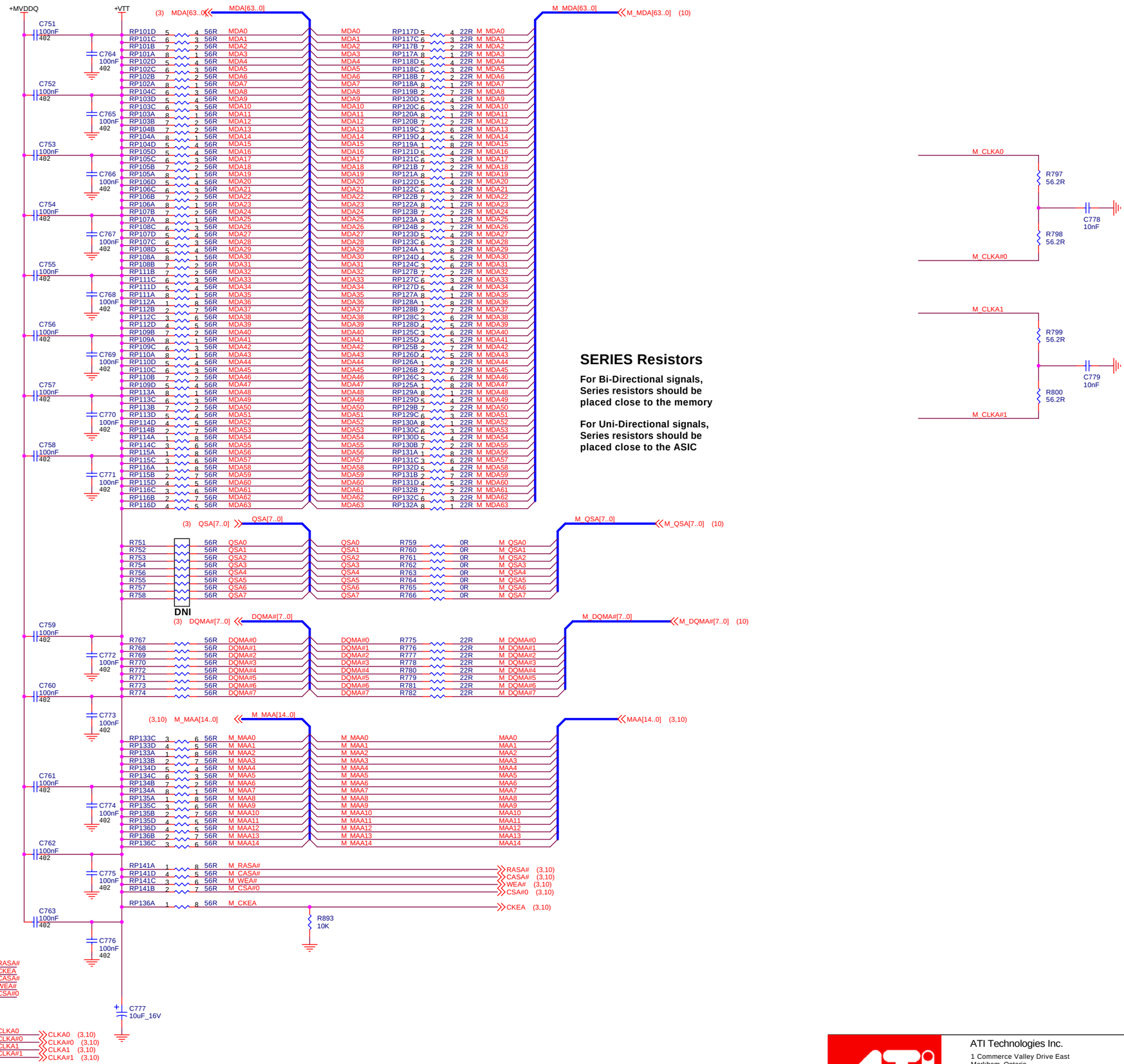

SERIES Resistors

For Bi-Directional signals, Series resistors should be placed close to the memory

For Uni-Directional signals, Series resistors should be placed close to the ASIC

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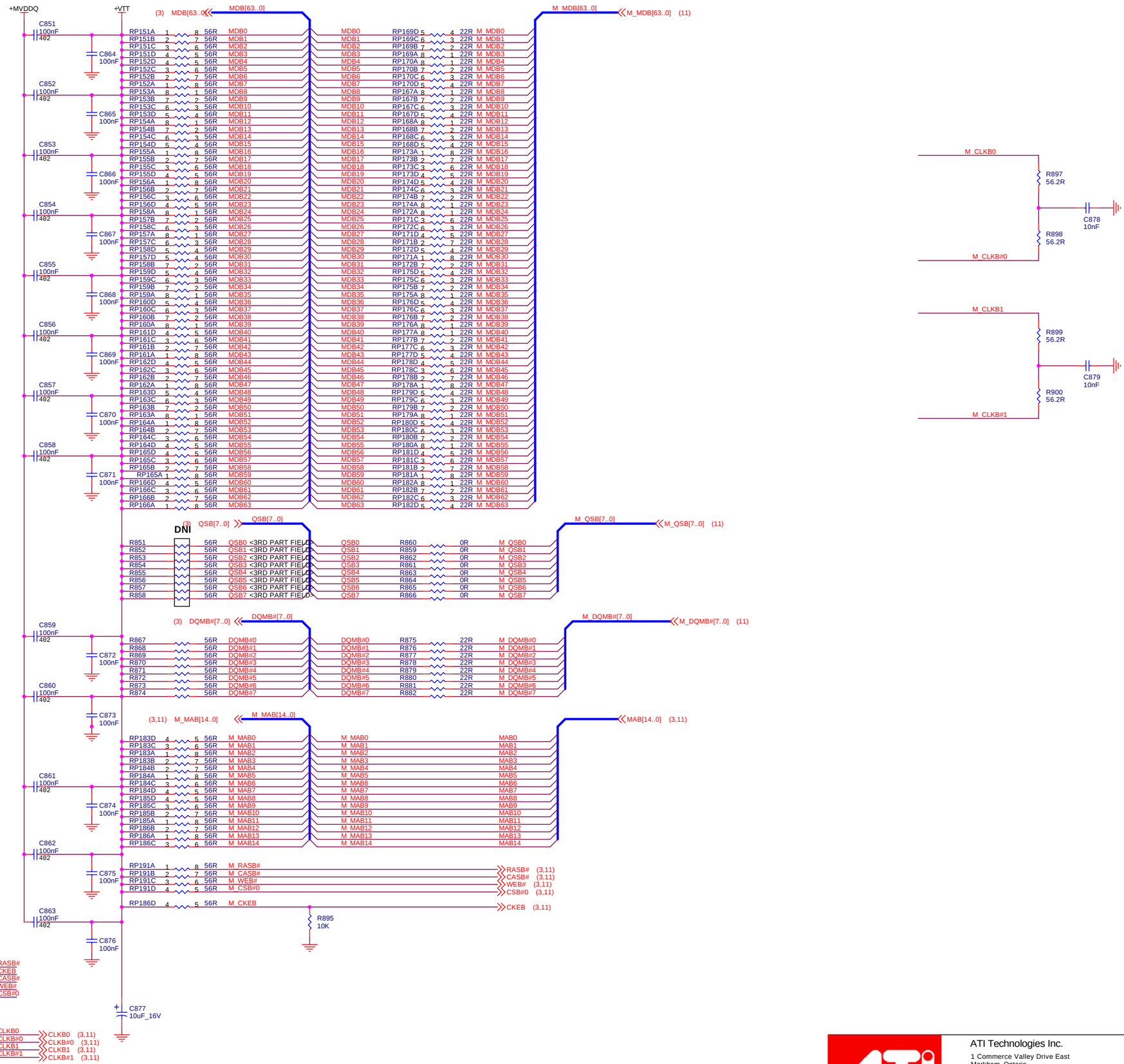

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Channel A Bottom Down

Channel A Bottom Up

Channel A Top Down

Channel A Top Up

Put 1 1uF cap per power pin of memory

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(9) M_DQMB#[7..0]

M_DQMB#[7..0]
M_DQMB#0
M_DQMB#1
M_DQMB#2
M_DQMB#3
M_DQMB#4
M_DQMB#5
M_DQMB#6
M_DQMB#7

(9) M_QSB[7..0]

M_QSB[7..0]
M_QSB0
M_QSB1
M_QSB2
M_QSB3
M_QSB4
M_QSB5
M_QSB6
M_QSB7

(3,9) M_CLKB#0
(3,9) M_CLKB#1

M_CLKB0#
M_CLKB1#

(3,9) M_CLKB0
(3,9) M_CLKB1

M_CLKB0
M_CLKB1

(3,9) M_CKEB
(3,9) M_WEB#
(3,9) M_CASB#
(3,9) M_RASB#
(3,9) M_CSB#0

M_CKEB
M_WEB#
M_CASB#0
M_RASB#0
M_CSB#0

(3,9) M_MAB[14..0]

M_MAB[14..0]
M_MAB0
M_MAB1
M_MAB2
M_MAB3
M_MAB4
M_MAB5
M_MAB6
M_MAB7
M_MAB8
M_MAB9
M_MAB10
M_MAB11
M_MAB12
M_MAB13
M_MAB14

(9) M_MDB[63..0]

Channel B Top Right

+MVDDQ
C246 100nF 402
C291 100nF 402
+VREF_U77
U31
VREF
M_MAB0 M_MAB1 M_MAB2 M_MAB3 M_MAB4 M_MAB5 M_MAB6 M_MAB7 M_MAB8 M_MAB9 M_MAB10 M_MAB11 → A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11
M_CLKB0 M_CLKB0# M_CKEB → CK CK CKE
M_CSB#0 M_RASB#0 M_CASB#0 M_WEB# → CS RAS CAS WE
M_QSB2 M_QSB0 → LDQS UDQS
M_DQMB#2 M_DQMB#0 → LDM UDM
M_MAB12 M_MAB13 → BA0 BA1
DQ0–DQ15 → M_MDB23 M_MDB22 M_MDB21 M_MDB20 M_MDB19 M_MDB18 M_MDB17 M_MDB16 M_MDB4 M_MDB5 M_MDB6 M_MDB7 M_MDB3 M_MDB2 M_MDB1 M_MDB0
NC NC#17 NC#19 NC#25 NC#42 NC#43 NC#50 NC#53 → M_MAB14
VDD VDD#18 VDD#33 VDDQ VDDQ#9 VDDQ#15 VDDQ#55 VDDQ#61 → +MVDDC
VSS VSS#48 VSS#66 VSSQ#6 VSSQ#12 VSSQ VSSQ#58 VSSQ#64 → +MVDDQ
1MX16X4

+MVDDQ
C266 100nF 402
C292 100nF 402
+VREF_U78
U35
VREF
M_MAB0 M_MAB1 M_MAB2 M_MAB3 M_MAB4 M_MAB5 M_MAB6 M_MAB7 M_MAB8 M_MAB9 M_MAB10 M_MAB11 → A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11
M_CLKB0 M_CLKB0# M_CKEB → CK CK CKE
M_CSB#0 M_RASB#0 M_CASB#0 M_WEB# → CS RAS CAS WE
M_QSB1 M_QSB3 → LDQS UDQS
M_DQMB#1 M_DQMB#3 → LDM UDM
M_MAB12 M_MAB13 → BA0 BA1
DQ0–DQ15 → M_MDB8 M_MDB9 M_MDB10 M_MDB11 M_MDB12 M_MDB13 M_MDB14 M_MDB15 M_MDB27 M_MDB25 M_MDB28 M_MDB30 M_MDB24 M_MDB31 M_MDB26 M_MDB29
NC NC#17 NC#19 NC#25 NC#42 NC#43 NC#50 NC#53 → M_MAB14
VDD VDD#18 VDD#33 VDDQ VDDQ#9 VDDQ#15 VDDQ#55 VDDQ#61 → +MVDDC
VSS VSS#48 VSS#66 VSSQ#6 VSSQ#12 VSSQ VSSQ#58 VSSQ#64 → +MVDDQ
1MX16X4

Channel B Bottom Left

+MVDDQ
C256 100nF 402
C293 100nF 402
+VREF_U76
U32
VREF
M_MAB0 M_MAB1 M_MAB2 M_MAB3 M_MAB4 M_MAB5 M_MAB6 M_MAB7 M_MAB8 M_MAB9 M_MAB10 M_MAB11 → A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11
M_CLKB1 M_CLKB1# M_CKEB → CK CK CKE
M_CSB#0 M_RASB#0 M_CASB#0 M_WEB# → CS RAS CAS WE
M_QSB5 M_QSB7 → LDQS UDQS
M_DQMB#5 M_DQMB#7 → LDM UDM
M_MAB12 M_MAB13 → BA0 BA1
DQ0–DQ15 → M_MDB40 M_MDB41 M_MDB42 M_MDB43 M_MDB44 M_MDB45 M_MDB46 M_MDB47 M_MDB56 M_MDB57 M_MDB58 M_MDB59 M_MDB60 M_MDB61 M_MDB62 M_MDB63
NC NC#17 NC#19 NC#25 NC#42 NC#43 NC#50 NC#53 → M_MAB14
VDD VDD#18 VDD#33 VDDQ VDDQ#9 VDDQ#15 VDDQ#55 VDDQ#61 → +MVDDC
VSS VSS#48 VSS#66 VSSQ#6 VSSQ#12 VSSQ VSSQ#58 VSSQ#64 → +MVDDQ
1MX16X4

+MVDDQ
C276 100nF 402
C294 100nF 402
+VREF_U76
U36
VREF
M_MAB0 M_MAB1 M_MAB2 M_MAB3 M_MAB4 M_MAB5 M_MAB6 M_MAB7 M_MAB8 M_MAB9 M_MAB10 M_MAB11 → A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11
M_CLKB1 M_CLKB1# M_CKEB → CK CK CKE
M_CSB#0 M_RASB#0 M_CASB#0 M_WEB# → CS RAS CAS WE
M_QSB6 M_QSB4 → LDQS UDQS
M_DQMB#6 M_DQMB#4 → LDM UDM
M_MAB12 M_MAB13 → BA0 BA1
DQ0–DQ15 → M_MDB55 M_MDB54 M_MDB53 M_MDB52 M_MDB51 M_MDB50 M_MDB49 M_MDB48 M_MDB39 M_MDB38 M_MDB37 M_MDB36 M_MDB35 M_MDB34 M_MDB33 M_MDB32
NC NC#17 NC#19 NC#25 NC#42 NC#43 NC#50 NC#53 → M_MAB14
VDD VDD#18 VDD#33 VDDQ VDDQ#9 VDDQ#15 VDDQ#55 VDDQ#61 → +MVDDC
VSS VSS#48 VSS#66 VSSQ#6 VSSQ#12 VSSQ VSSQ#58 VSSQ#64 → +MVDDQ
1MX16X4

Channel B Bottom Left

Channel B Top Left

+MVDDQ
R807 4.7K 402
+VREF_U77
R808 4.7K 402

+MVDDQ
R803 4.7K 402
+VREF_U78
R804 4.7K 402

+MVDDQ
R907 4.7K 402
+VREF_U79
R908 4.7K 402

+MVDDQ
R903 4.7K 402
+VREF_U76
R904 4.7K 402

+MVDDQ
C241 C242 C243 C244 C245 100nF 402

+MVDDQ
C251 C252 C253 C254 C255 100nF 402

+MVDDC
C247 C248 C249 100nF 402

+MVDDC
C257 C258 C259 100nF 402

+MVDDQ
C261 C262 C263 C264 C265 100nF 402

+MVDDQ
C271 C272 C273 C274 C275 100nF 402

+MVDDC
C267 C268 C269 100nF 402

+MVDDC
C277 C278 C279 100nF 402

+MVDDQ
C281 22uF_16V TANT

+MVDDC
C285 22uF_16V TANT

+MVDDQ
C282 22uF_16V TANT

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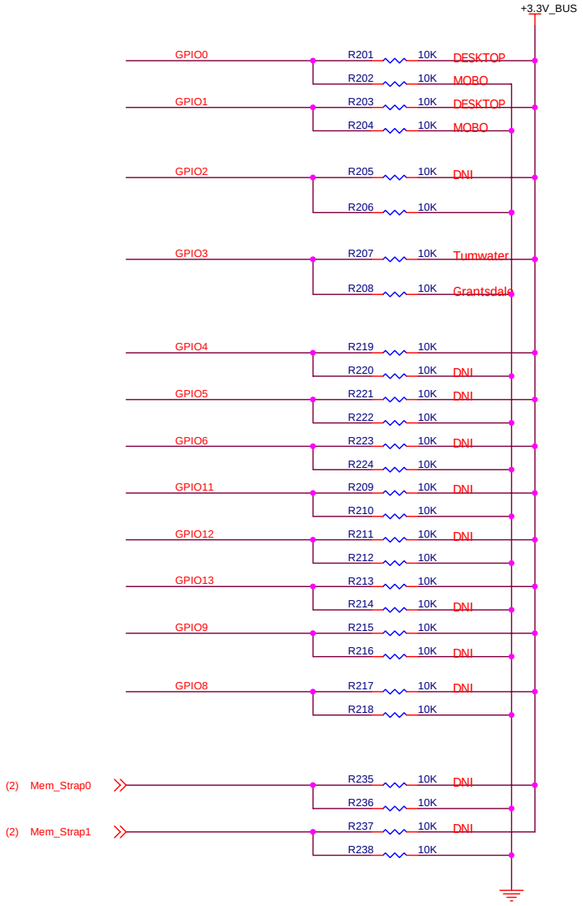
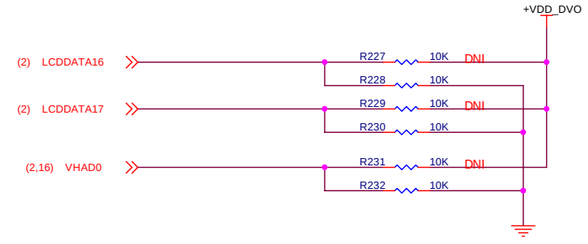
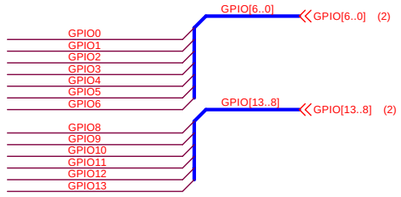
OPTION STRAPS





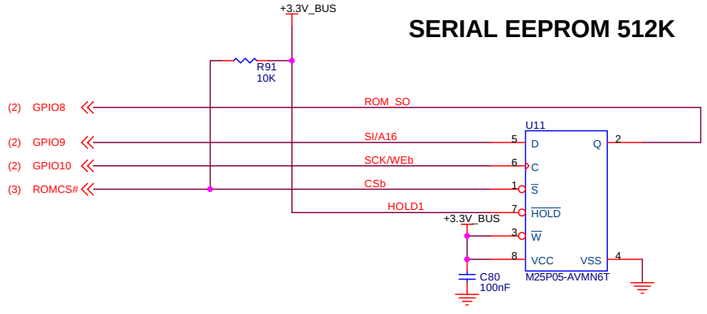


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K



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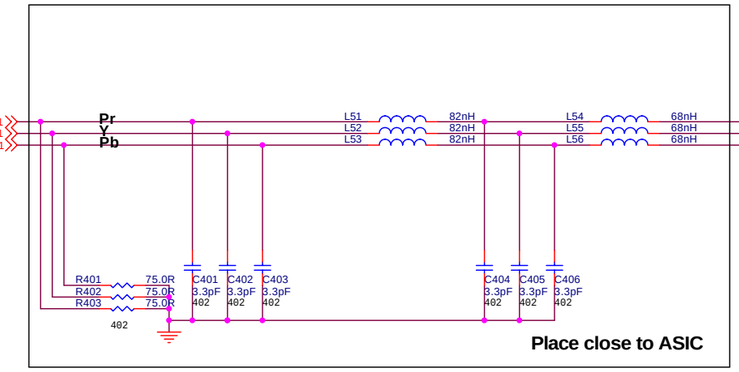
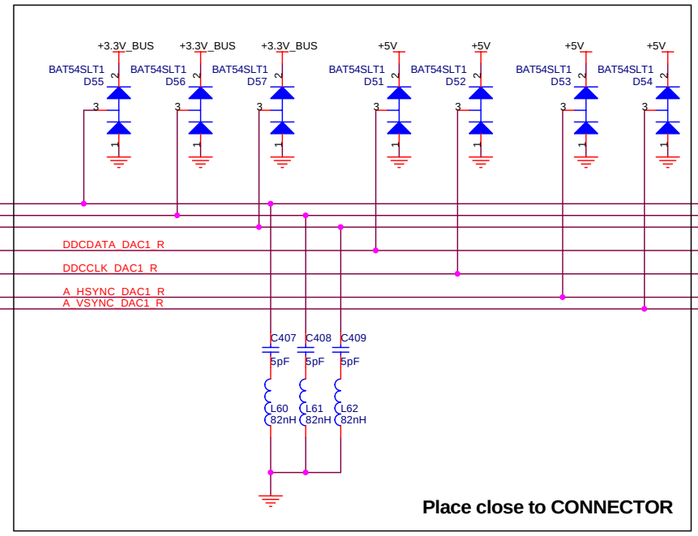
PRIMARY CRT

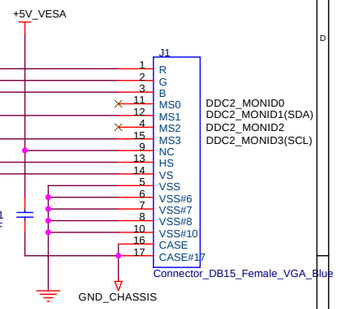


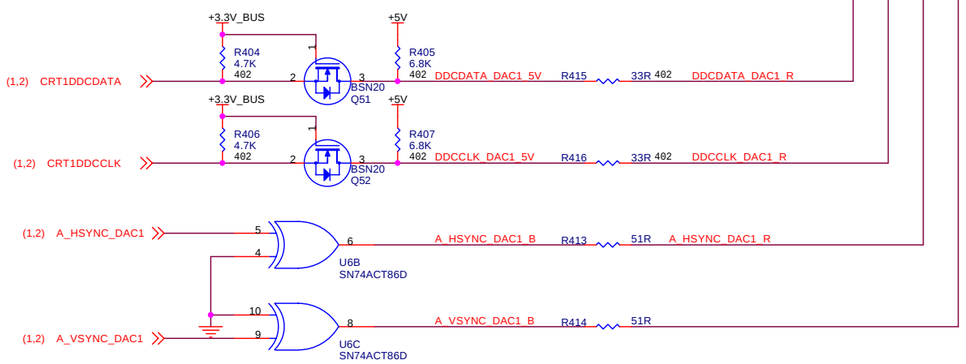
(2) A_R_DAC1
(2) A_G_DAC1
(2) A_B_DAC1

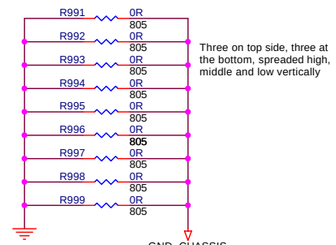
OPTIONAL ESD/HOTPLUG PROTECTION DIODES



A_R_DB15
A_G_DB15
A_B_DB16
DDCDATA_DAC1_R
DDCCLK_DAC1_R
A_HSYNC_DAC1_R
A_VSYNC_DAC1_R



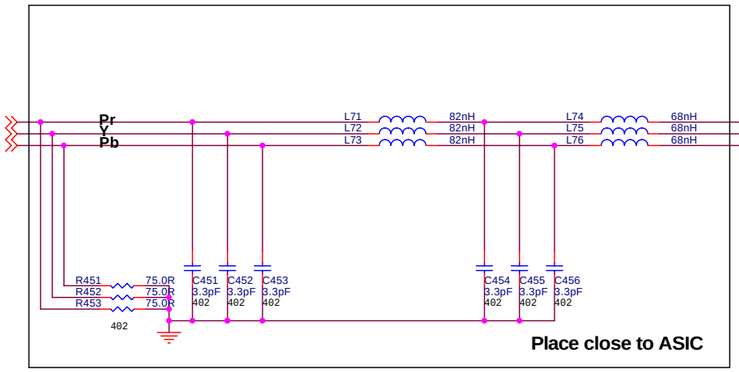




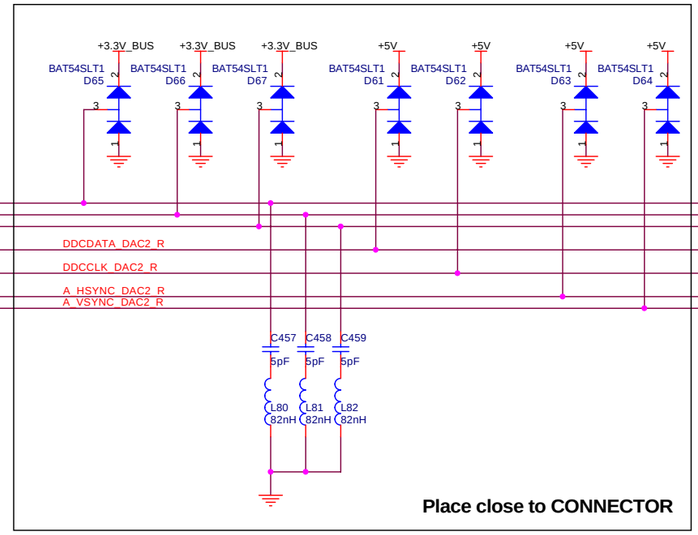
Three on top side, three at the bottom, spreaded high, middle and low vertically

OPTIONAL ESD/HOTPLUG PROTECTION DIODES

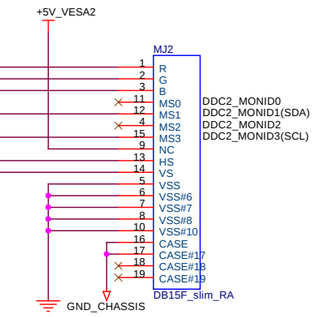
SECONDARY CRT



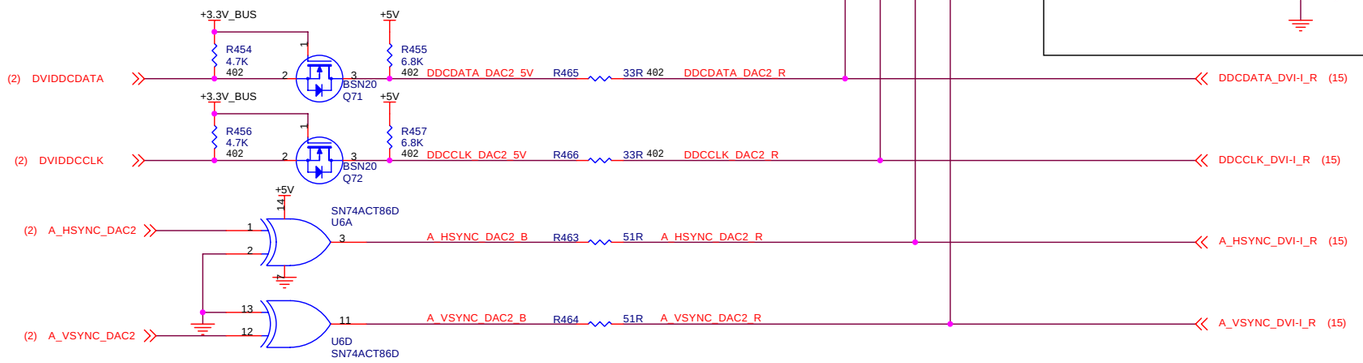
(14) A_R_DAC2
(14) A_G_DAC2
(14) A_B_DAC2



A_R_DVI-I (15)
A_G_DVI-I (15)
A_B_DVI-I (15)
DDCDATA_DAC2_R
DDCCLK_DAC2_R
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R



6052003000



DDCDATA_DVI-I_R (15)
DDCCLK_DVI-I_R (15)
A_HSYNC_DVI-I_R (15)
A_VSYNC_DVI-I_R (15)

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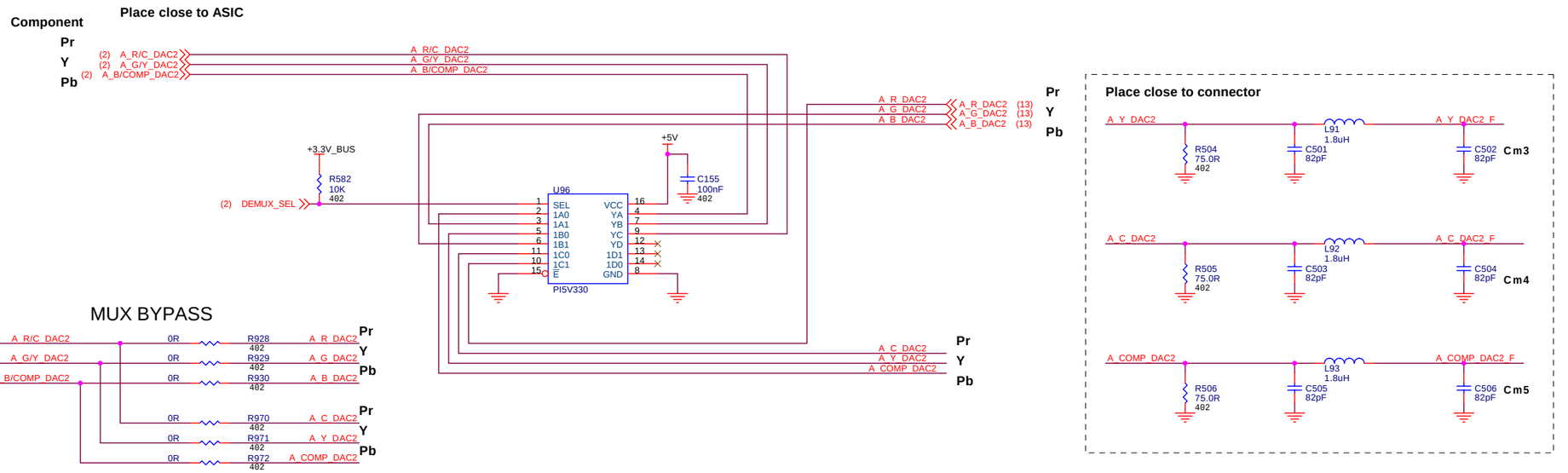

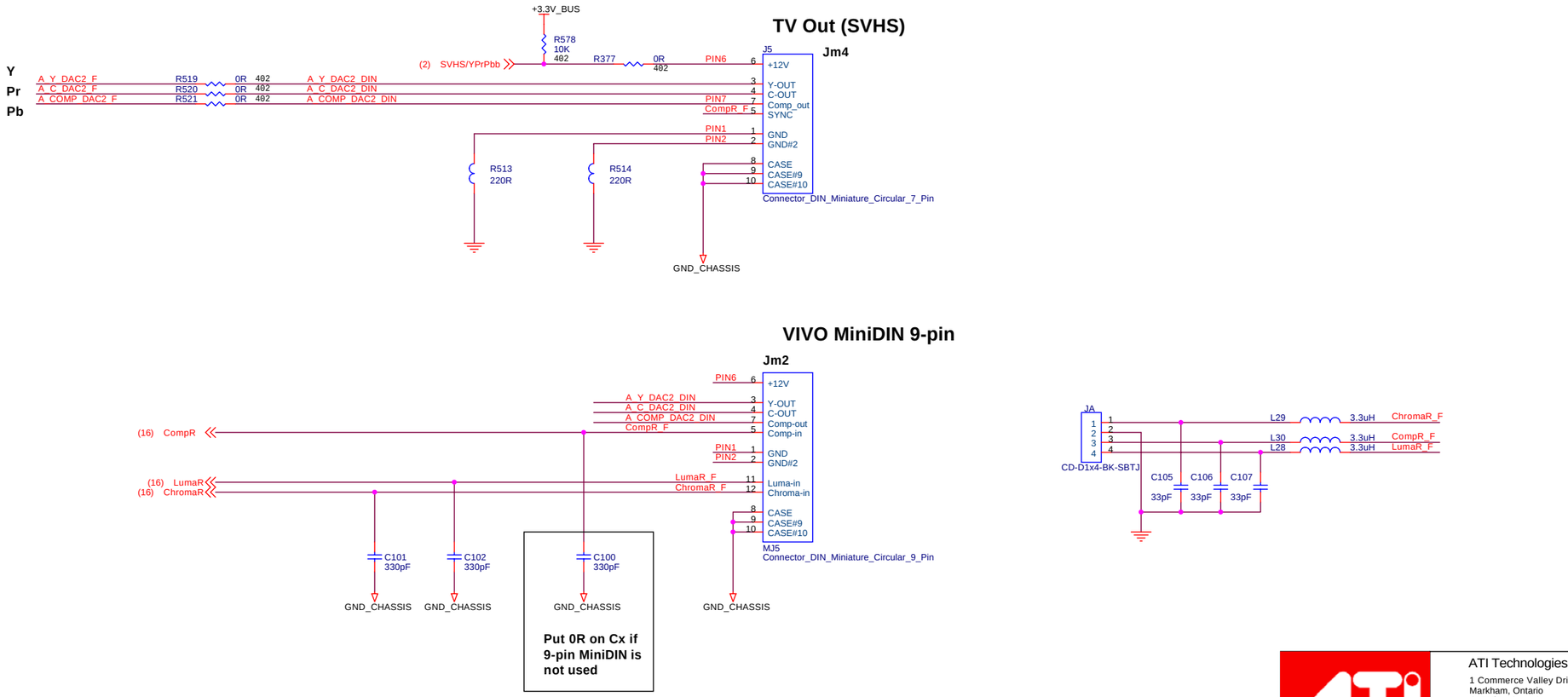

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PRIMARY DVI-I CONNECTOR

INSTALL TERMINATION RESISTORS CLOSE TO ASIC

R601 330R 402
R602 330R 402
R603 330R 402
R604 330R 402

(2) TMDS_TX2N
(2) TMDS_TX2P
(2) TMDS_TX1N
(2) TMDS_TX1P
(2) TMDS_TX0N
(2) TMDS_TX0P
(2) TMDS_TXCP
(2) TMDS_TXCN

(13) DDCCLK_DVI-I_R
(13) DDCDATA_DVI-I_R

DDCCLK_DVI-I
DDCDATA_DVI-I

(13) A_VSYNC_DVI-I_R
(13) A_R_DVI-I
(13) A_G_DVI-I
(13) A_B_DVI-I
(13) A_HSYNC_DVI-I_R

+5V_VESA2

+3.3V_BUS

R605 20K 402
R606 20K 402
R608 20K 402
R607 20K 402
R609 100K 402

(2) HPD

D121 2.5V DNI

Q25 CMPT3904
Q26 CMPT3904

C510 68pF DNI

GND_CHASSIS GND_CHASSIS

J2 — DVI_A/D

M1		CASE
M3		CASE#M3
1		TMDS Data2-
2		TMDS Data2+
3		TMDS Data2/4 Shield
4		TMDS Data4-
5		TMDS Data4+
6		DDC Clock
7		DDC Data
8		Analog VSYNC
9		TMDS Data1-
10		TMDS Data1+
11		TMDS Data1/3 Shield
12		TMDS Data3-
13		TMDS Data3+
14		+5V Power
15		GND (for +5V)
16		Hot Plug Detect
17		TMDS Data0-
18		TMDS Data0+
19		TMDS Data0/5 Shield
20		TMDS Data5-
21		TMDS Data5+
22		TMDS Clock Shield
23		TMDS Clock+
24		TMDS Clock-
C1	Pr	Analog Red
C2	Y	Analog Green
C3	Pb	Analog Blue
C4		Analog HYNC
C5		Analog GND
C6		Analog GND#C6
M4		CASE#M4
M2		CASE#M2

+12V_BUS
Req = 120.8R
Use 604R, 1206, 1/4W
R911 220R
R912 220R
R913 220R
R914 220R
R915 220R
REG19 TL431CDBVR
R916 1.0K 1% 402
R917 1.0K 1% 402
+5V_VESA
Multi-footprint
C911 10uF_6.3V
MC911 4.7uF

Normal +5V regulated operation
This circuit provide upto 58mA

If Iload > 58mA, +5V will drop

If Vout is shorted
Current across each Rx is 12V/604R = 20mA
Power dissipated by each Rx is 20mA x 12V = 238mW
Each Rx are rated 250mW (1/4W)

+12V_BUS
Req = 120.8R
Use 604R, 1206, 1/4W
R921 220R
R922 220R
R923 220R
R924 220R
R925 220R
REG20 TL431CDBVR
R918 1.0K 1% 402
R919 1.0K 1% 402
+5V_VESA2
Multi-footprint
C912 10uF_6.3V
MC912 4.7uF

Normal +5V regulated operation
This circuit provide upto 58mA

If Iload > 58mA, +5V will drop

If Vout is shorted
Current across each Rx is 12V/604R = 20mA
Power dissipated by each Rx is 20mA x 12V = 238mW
Each Rx are rated 250mW (1/4W)

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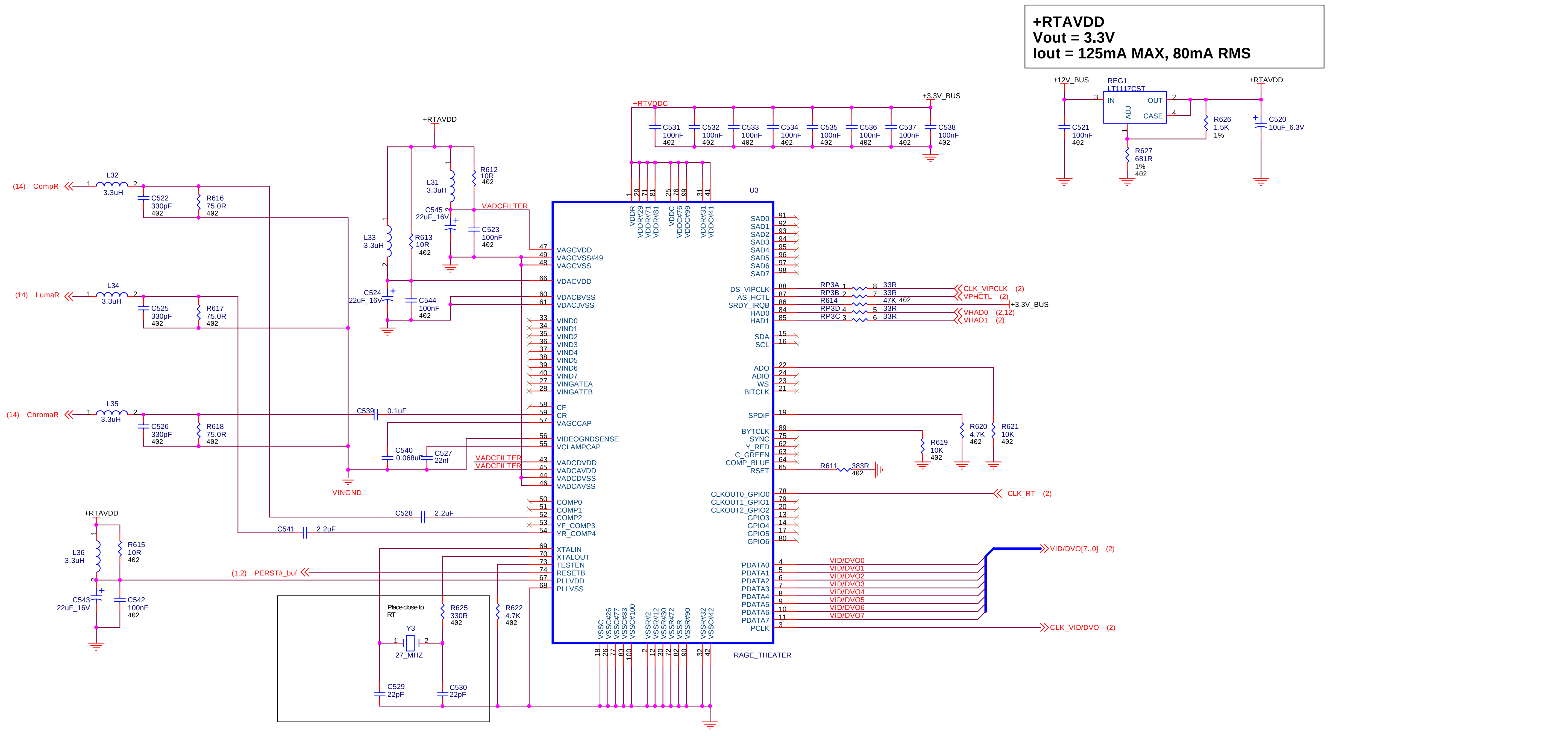

+RTAVDD
Vout = 3.3V
Iout = 125mA MAX, 80mA RMS
+12V_BUS
REG1
LT1117CST
IN
OUT
ADJ
CASE
C521 100nF 402
R626 1.5K 1%
R627 681R 1% 402
C520 10uF_6.3V
+3.3V_BUS
+RTVDDC
C531 100nF 402
C532 100nF 402
C533 100nF 402
C534 100nF 402
C535 100nF 402
C536 100nF 402
C537 100nF 402
C538 100nF 402
U3
RAGE_THEATER
(14) CompR
(14) LumaR
(14) ChromaR
L32 3.3uH
L34 3.3uH
L35 3.3uH
C522 330pF 402
C525 330pF 402
C526 330pF 402
R616 75.0R 402
R617 75.0R 402
R618 75.0R 402
L31 3.3uH
L33 3.3uH
R612 10R 402
R613 10R 402
C545 22uF_16V
C523 100nF 402
C524 22uF_16V
C544 100nF 402
VADCFILTER
C539 0.1uF
C540 0.068uF
C527 22nf
VINGND
C528 2.2uF
C541 2.2uF
L36 3.3uH
R615 10R 402
C543 22uF_16V
C542 100nF 402
(1,2) PERST#_buf
Place close to RT
Y3 27_MHZ
R625 330R 402
R622 4.7K 402
C529 22pF
C530 22pF
VAGCVDD
VAGCVSS#49
VAGCVSS
VDACVDD
VDACBVSS
VDACJVSS
VIND0
VIND1
VIND2
VIND3
VIND4
VIND5
VIND6
VIND7
VINGATEA
VINGATEB
CF
CR
VAGCCAP
VIDEOGNDSENSE
VCLAMPCAP
VADCDVDD
VADCAVDD
VADCDVSS
VADCAVSS
COMP0
COMP1
COMP2
YF_COMP3
YR_COMP4
XTALIN
XTALOUT
TESTEN
RESETB
PLLVDD
PLLVSS
SAD0
SAD1
SAD2
SAD3
SAD4
SAD5
SAD6
SAD7
DS_VIPCLK
AS_HCTL
SRDY_IRQB
HAD0
HAD1
SDA
SCL
ADO
ADIO
WS
BITCLK
SPDIF
BYTCLK
SYNC
Y_RED
C_GREEN
COMP_BLUE
RSET
CLKOUT0_GPIO0
CLKOUT1_GPIO1
CLKOUT2_GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
PDATA0
PDATA1
PDATA2
PDATA3
PDATA4
PDATA5
PDATA6
PDATA7
PCLK
RP3A 33R
RP3B 33R
R614 47K 402
RP3D 33R
RP3C 33R
CLK_VIPCLK (2)
VPHCTL (2)
VHAD0 (2,12)
VHAD1 (2)
R619 10K 402
R620 4.7K 402
R621 10K 402
R611 383R 402
CLK_RT (2)
VID/DVO[7..0] (2)
VID/DVO0
VID/DVO1
VID/DVO2
VID/DVO3
VID/DVO4
VID/DVO5
VID/DVO6
VID/DVO7
CLK_VID/DVO (2)

Footprint can be replaced with zero ohm or other.

B8 GND_CHASSIS VINGND

Layout Guide line of THEATER

#1 : C27 and C28 have to be placed as close as possible to the respective pins of Rage THEATER

#2 : VINGND should be seperated from Digital or Chassis Ground and have no loops

#3 : VINGND should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

IMPORTANT

Put 2D line as close as possible to pin 56 of Rage Theater

VINGND

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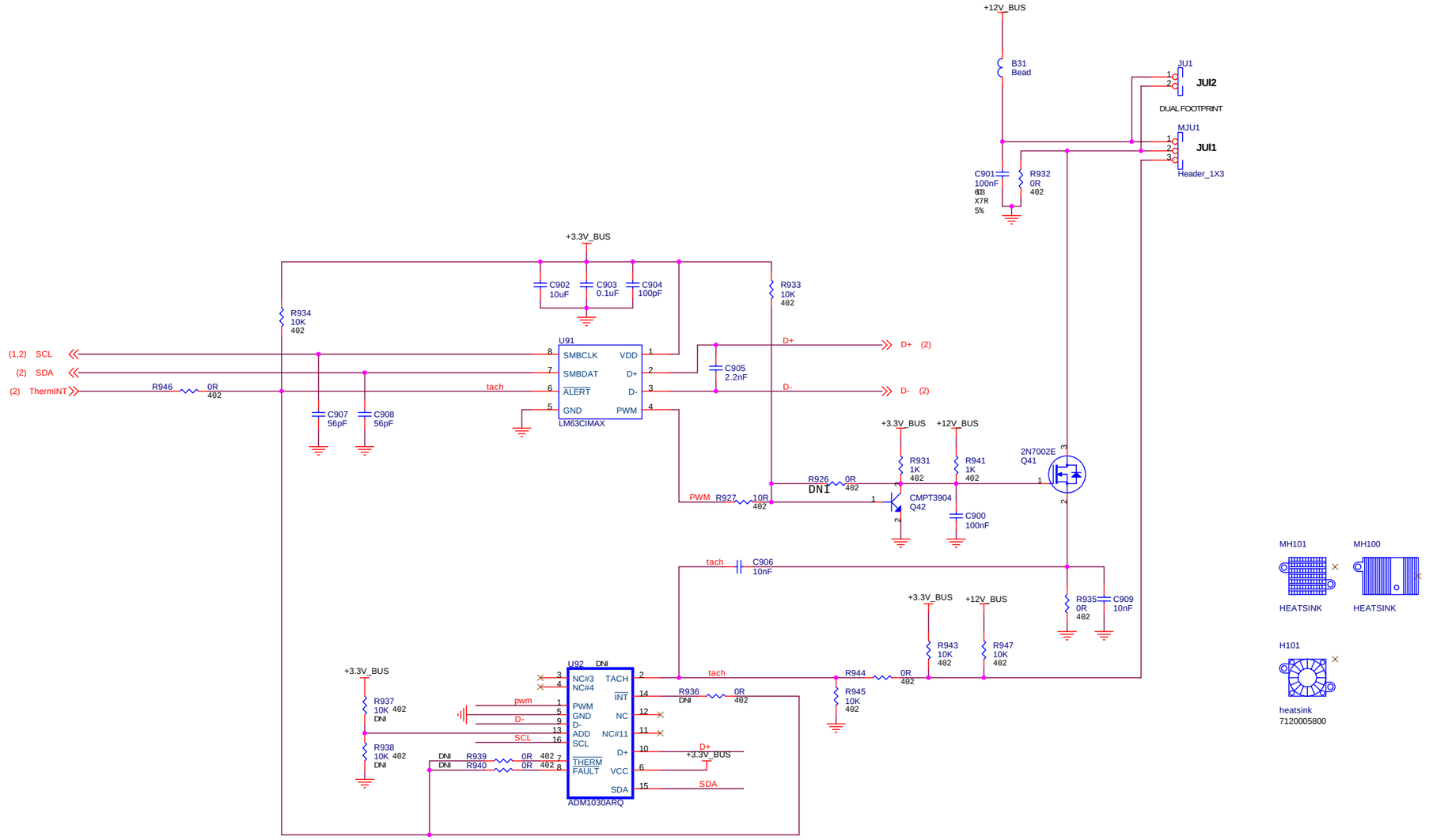
TEMPERATURE SENSE AND SPEED CONTROLLED FAN



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ASSY1
SCREW
JACKSCREW

ASSY2
SCREW
JACKSCREW

ASSY3
SCREW
JACKSCREW

ASSY4
SCREW
JACKSCREW

MISC. BOARD PARTS

ASSY7
ANTISTATIC BAG
6_X_11

REF5
ATI LOGO LABEL
ATI_LOGO_LABEL

ASSY8
BLANK LABEL

ASSY10
BRACKET
DVI, DIN, VGA

ASSY12
BRACKET
8020037100
SV-VO-V
Slim VGA, DIN, VGA, 347
8020034700

ASSY11
BRACKET
80200370A0
DI-V
DVI, DIN, VGA

ASSY13
BRACKET
80200371A0
SV-V
Slim VGA, DIN, VGA, 347

MT1
MT_Hole_0.136_in.
GND_CHASSIS

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MEMORY CHANNEL A

MEMORY CHANNEL B

TSOP 16Mx16 Memory

TSOP 16Mx16 Memory

MEMORY TERMINATIONS A

MEMORY TERMINATIONS B

PRIMARY CRT LOGIC

VGA DB15 CONN

CLOCK

MEM A

MEM B

DAC1

Int. TMDS

INTEGRATED TMDS LOGIC

DVI-I CONN and/or VGA Slim DB15 CONN

STRAPS

BIOS

ROM

VID

VIP

RageTheater 1

POWER REGULATION

RV370

DAC2

PCI-E

LCDDATA19

SEL

D E M U X

TVOUT Filters

VO or VIVO CONN

Secondary CRT LOGIC

PCI-Express

REFERENCE DESIGN

THESE SCHEMATICS ARE SUBJECT TO MODIFICATION AND DESIGN IMPROVEMENTS. PLEASE CONTACT ATI FIELD APPLICATION ENGINEERING BEFORE USING THE INFORMATION CONTAINED HEREIN.

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