

V191-33

P684-A01 GT216 DESKTOP Low Profile
PCI-EXPRESSx16 DL-DVI HDMI VGA DDR3

- Page 1: P684-A01 OVERVIEW
- Page 2: PCI-EXPRESS INTERFACE
- Page 3: PARTITION A FRAME BUFFER INTERFACE
- Page 4: PARTITION A MEMORIES
- Page 5: FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS
- Page 6: PARTITION C FRAME BUFFER INTERFACE
- Page 7: PARTITION C MEMORIES
- Page 8: FBC DECOUPLING CAPS
- Page 9: DACA (SOUTH DVI-I)
- Page 10: DACB (cable up VGA)
- Page 11: IFP AB (SOUTH DVI-I)
- Page 12: IFP C (NORTH HDMI)
- Page 13: IFP D (UNUSED)
- Page 14: IFP EF (UNUSED)
- Page 15: MIOA & MIOB
- Page 16: XTAL, MECHANICALS, THERMALS
- Page 17: FAN CONTROL, GPIO, JTAG
- Page 18: BIOS ROM, HDCP ROM, STRAPPING OPTIONS
- Page 19: LINEAR POWER SUPPLIES
- Page 20: FBVDDQ/PEXVDD POWER SUPPLY
- Page 21: NVVDD POWER SUPPLY

V191 31 pcb change list

- Page 5 : Add Capacitor C649 C684 for NVVDD
- Page 16 : Change EM1 EM2 EM3 footprint for EMI
- Page 17 : Since J5 footprint issue,Revise J5 pin define to same as P684
- Page 21 : Change EL21 footprint

V191 32 pcb change list

- Page 16 : Change Y1 footprint to NV reference type
- Reserve R72,R73 0ohm to GND for Y1

V191 33 pcb change list

- Page 19 : Change C52 footprint for 100uF OSCON
- Page 21 : Change NVVDD PWM power circuit to UP6137


| REV | VARIANT | NPVN | ASSEMBLY |
|-----|-------------|--------------------|--|
| B | BASE | 600-10684-base-100 | BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL |
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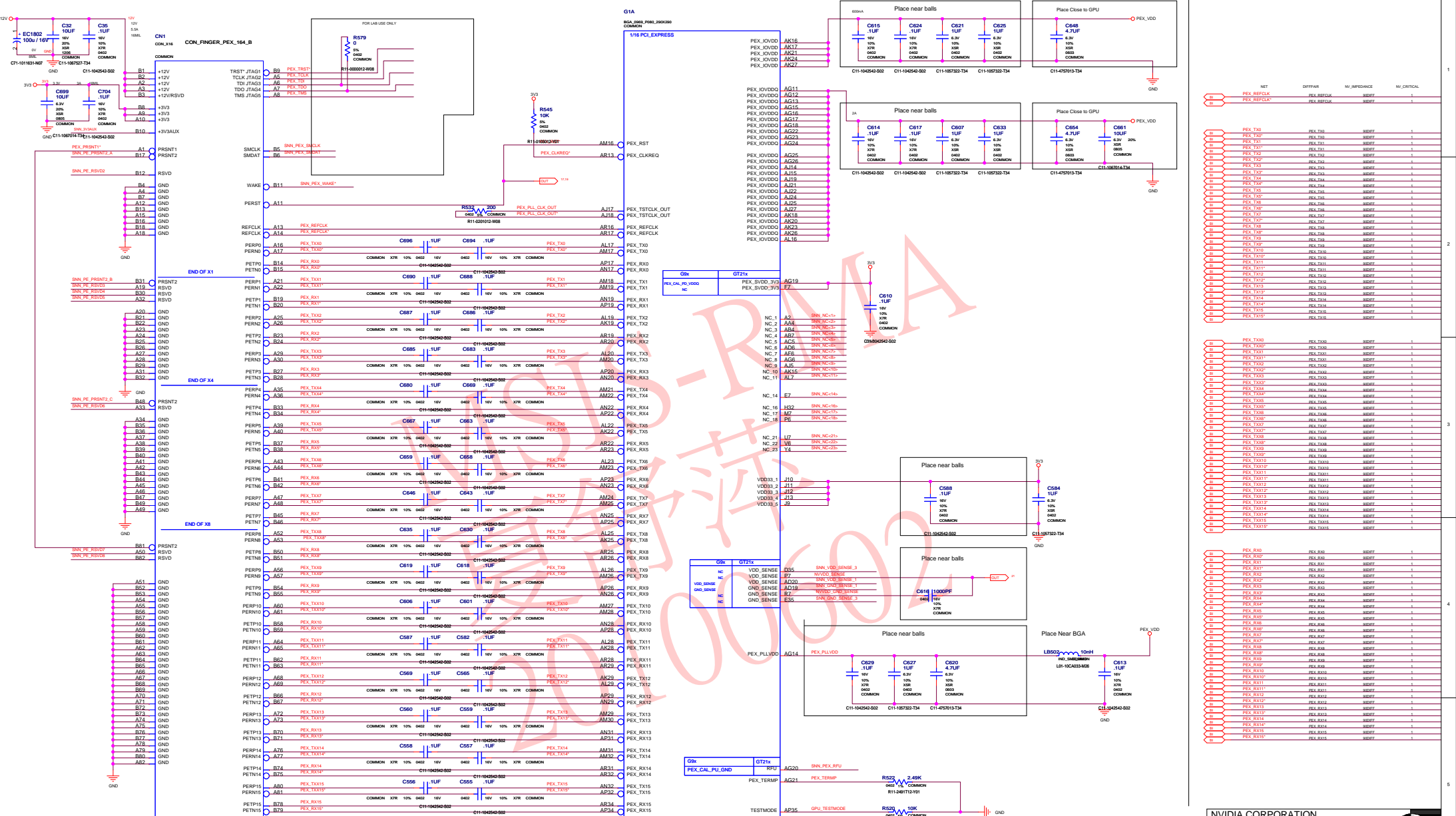
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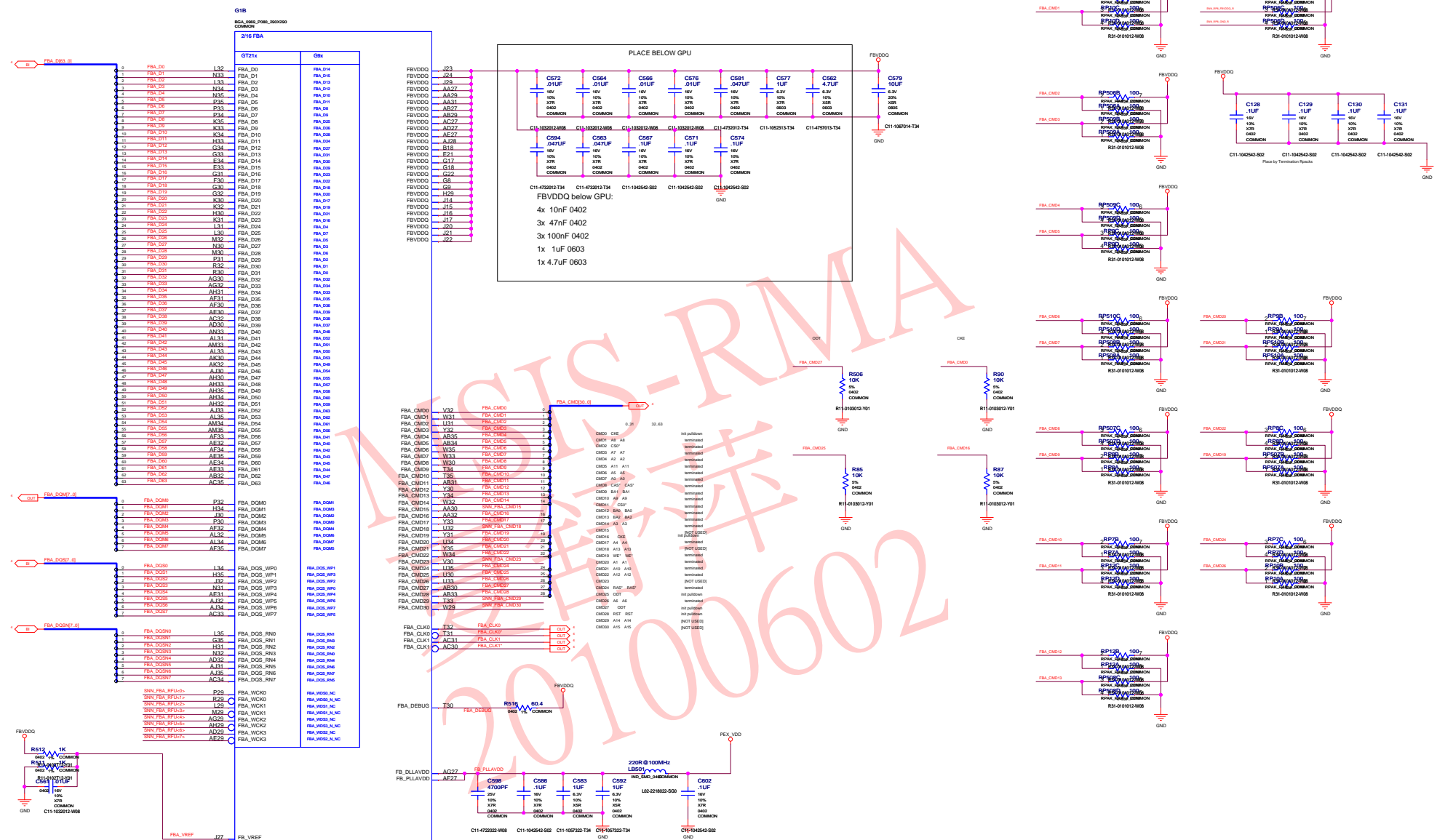
PCI-EXPRESS INTERFACE



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PARTITION A FRAME BUFFER INTERFACE



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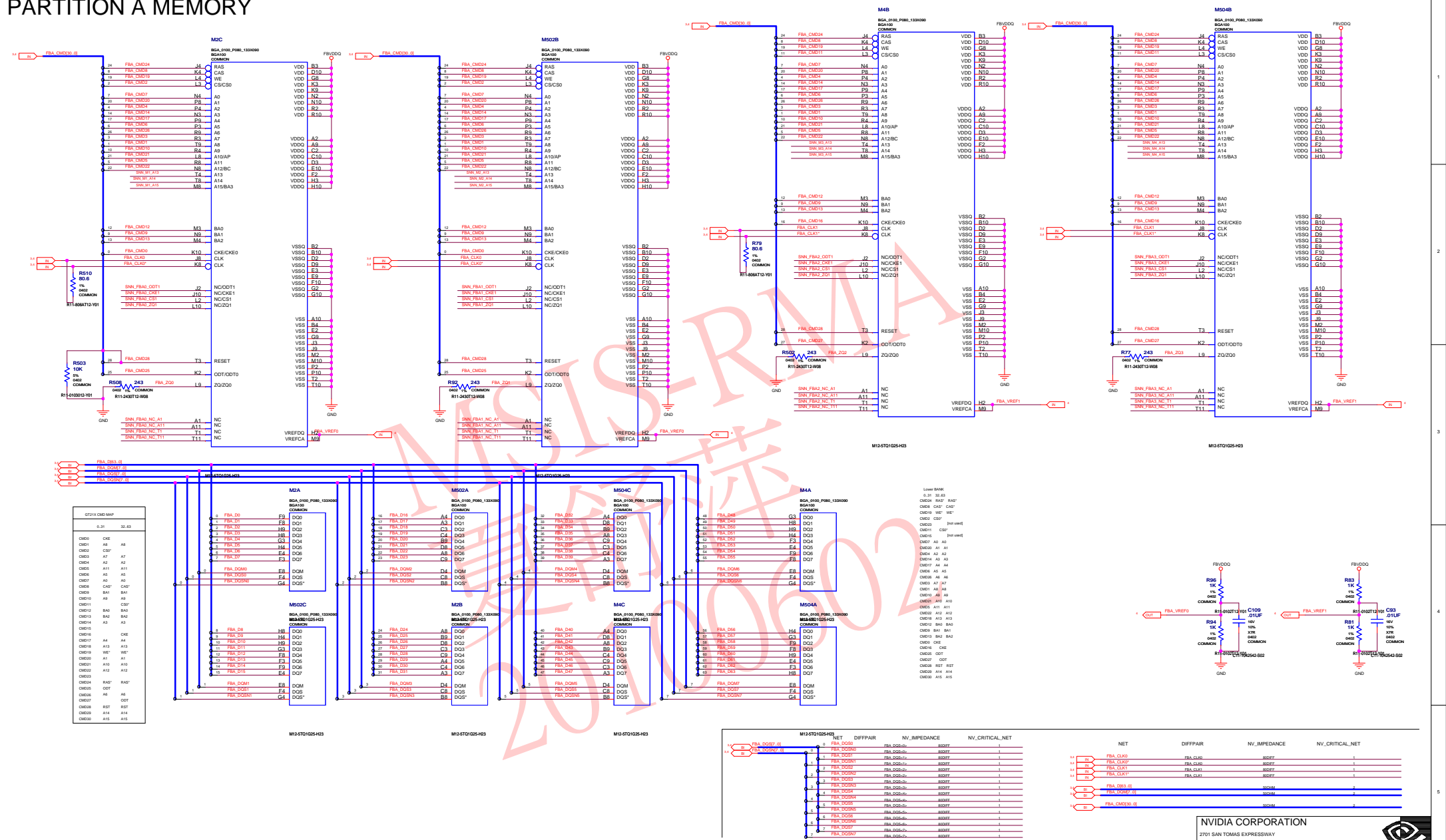
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| | |
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| ASSEMBLY | |
| PAGE DETAIL | PARTITION A FRAME BUFFER INTERFACE |

PARTITION A MEMORY



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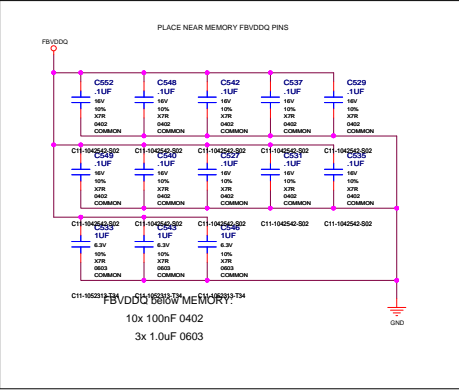
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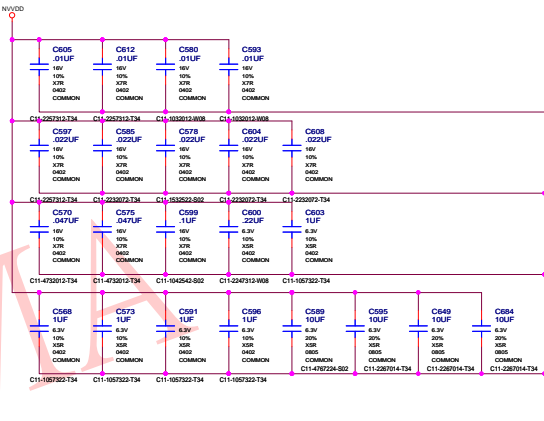
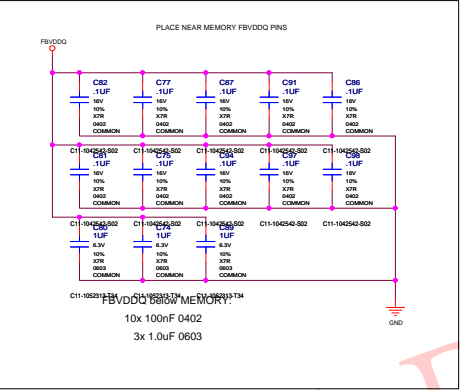
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| A | B | C | D | E | F | G | H |
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FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS

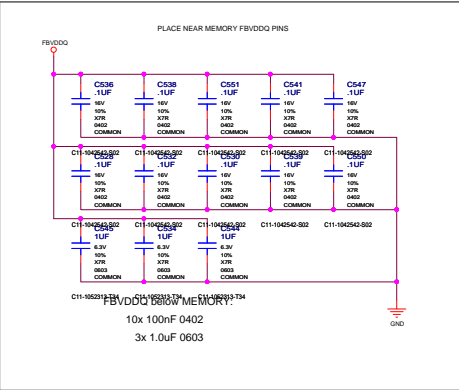
Decoupling for FBA 0..15



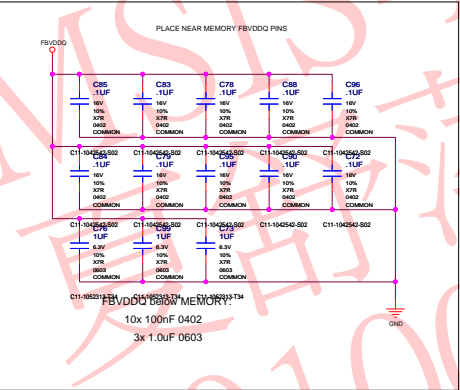
Decoupling for FBA 16..31



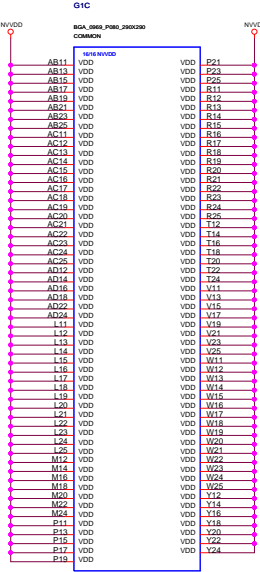
Decoupling for FBA 32..47



Decoupling for FBA 48..63



NVVDD under GPU:
4x 0.01uF 0402 X7R
5x 0.022uF 0402 X7R
2x 0.047uF 0402 X7R
1x 0.1uF 0402 X7R
1x 0.22uF 0402 X7R
4x 1.0uF 0402 X5R
1x 2.2uF 0402 X5R
2x 10uF 0805 X5R



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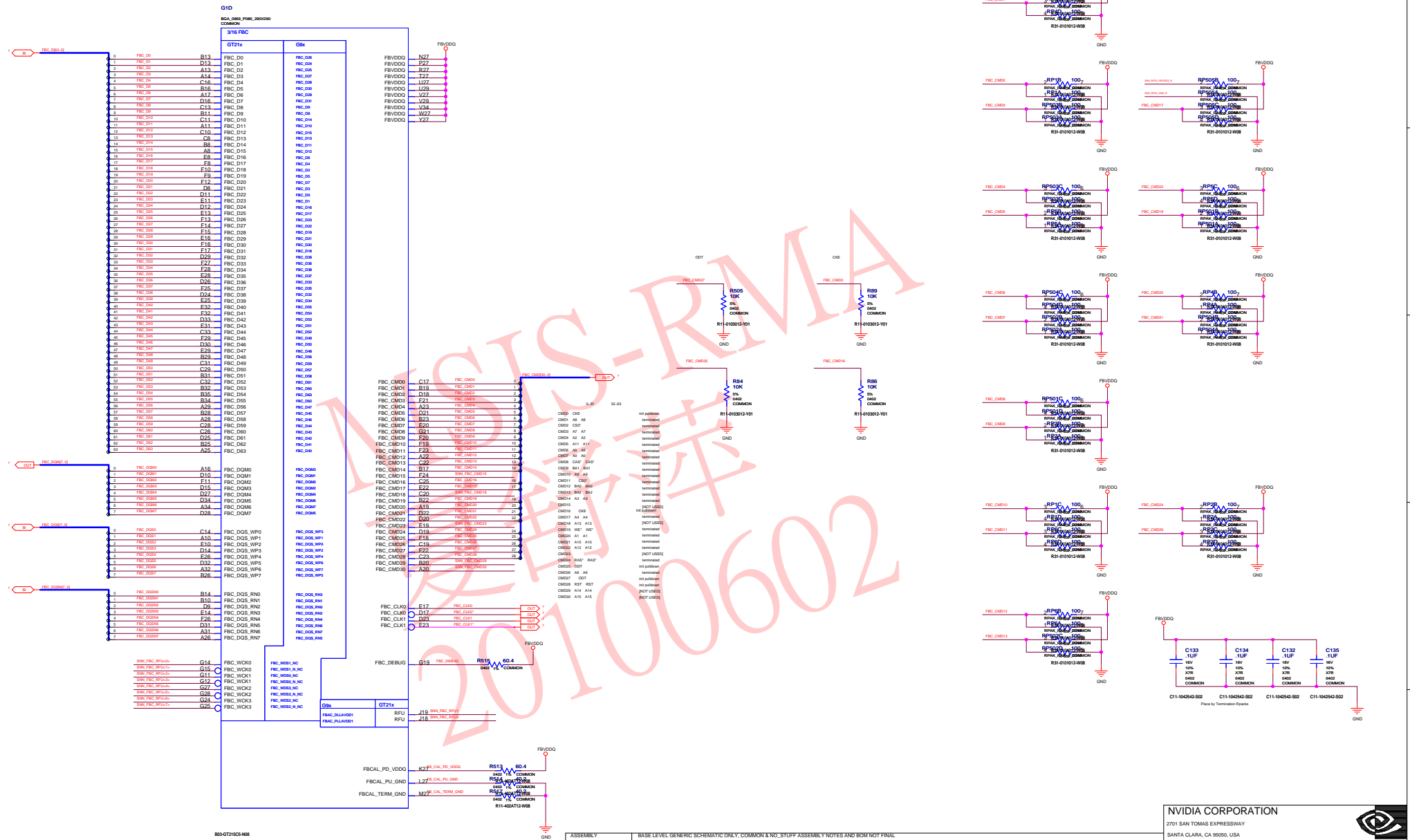


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PARTITION C FRAME BUFFER INTERFACE

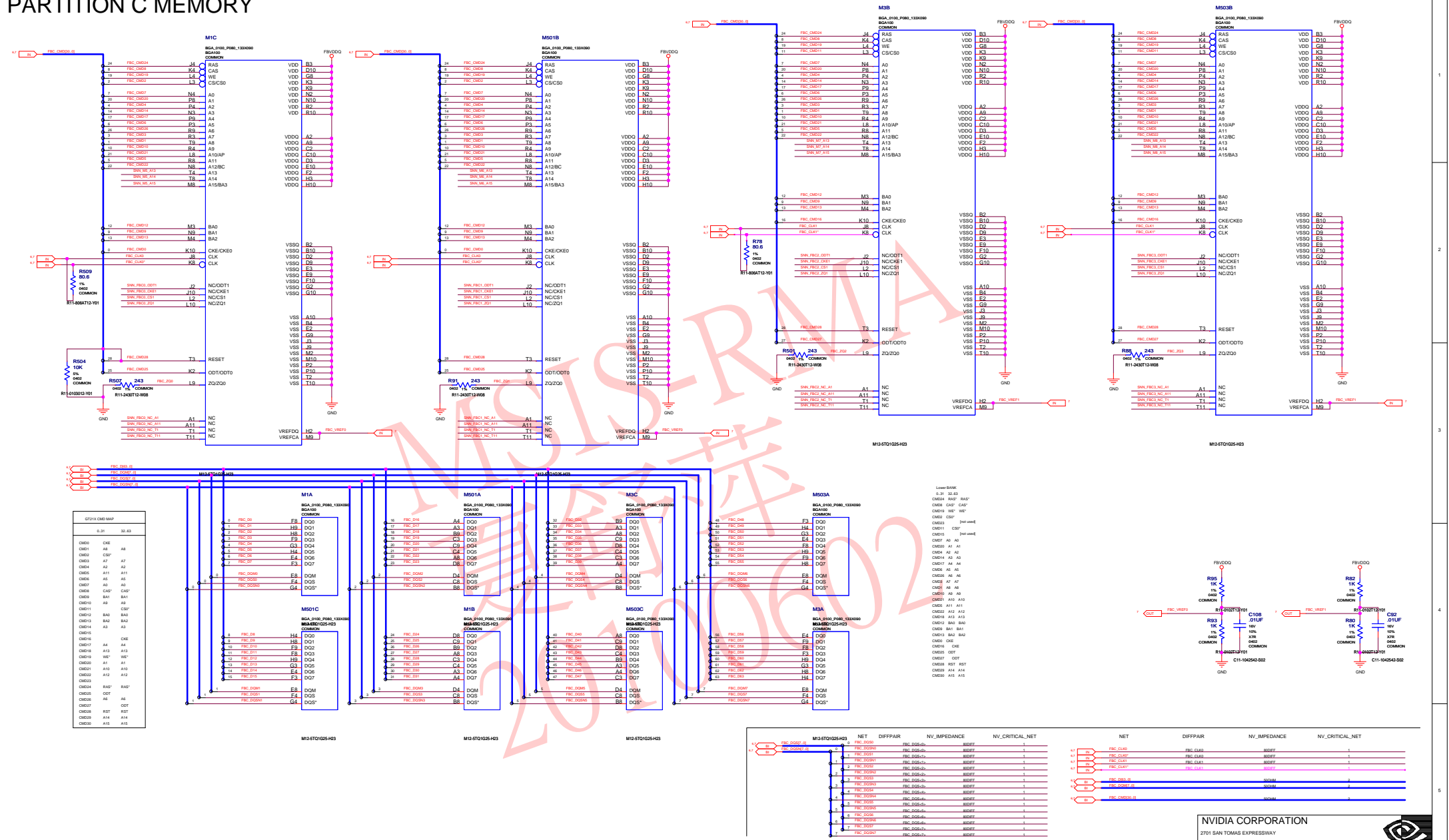


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PARTITION C MEMORY



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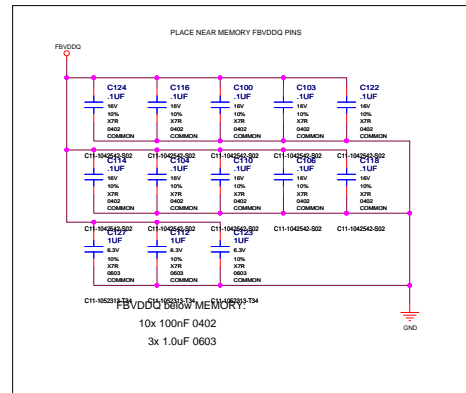
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| PAGE DETAIL | PARTITION C MEMORIES |

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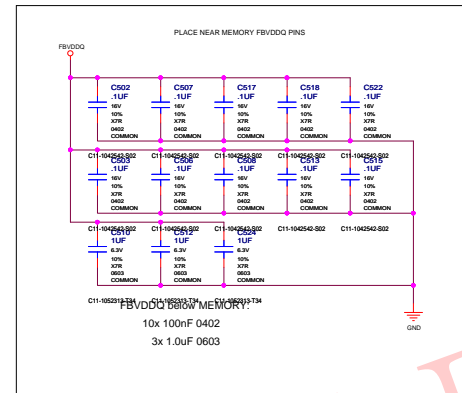


FBC DECOUPLING CAPS & NVVDD DECOUPLING CAPS

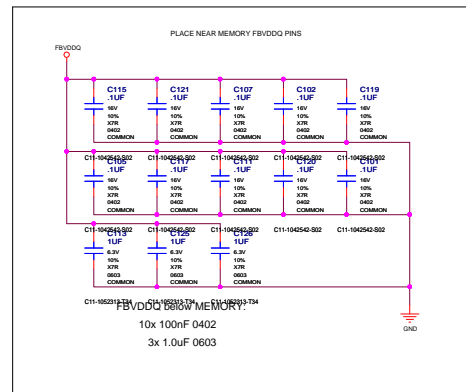
Decoupling for FBC 0..15



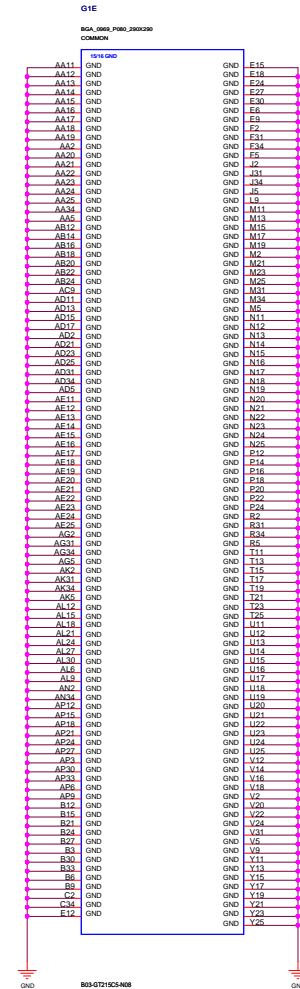
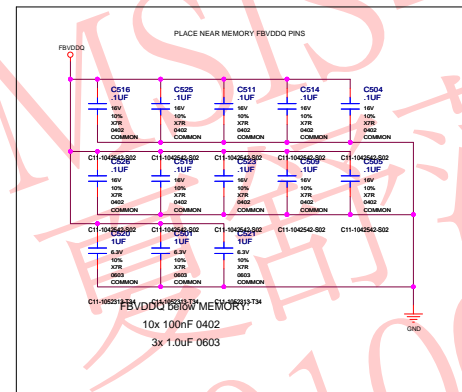
Decoupling for FBC 16..31



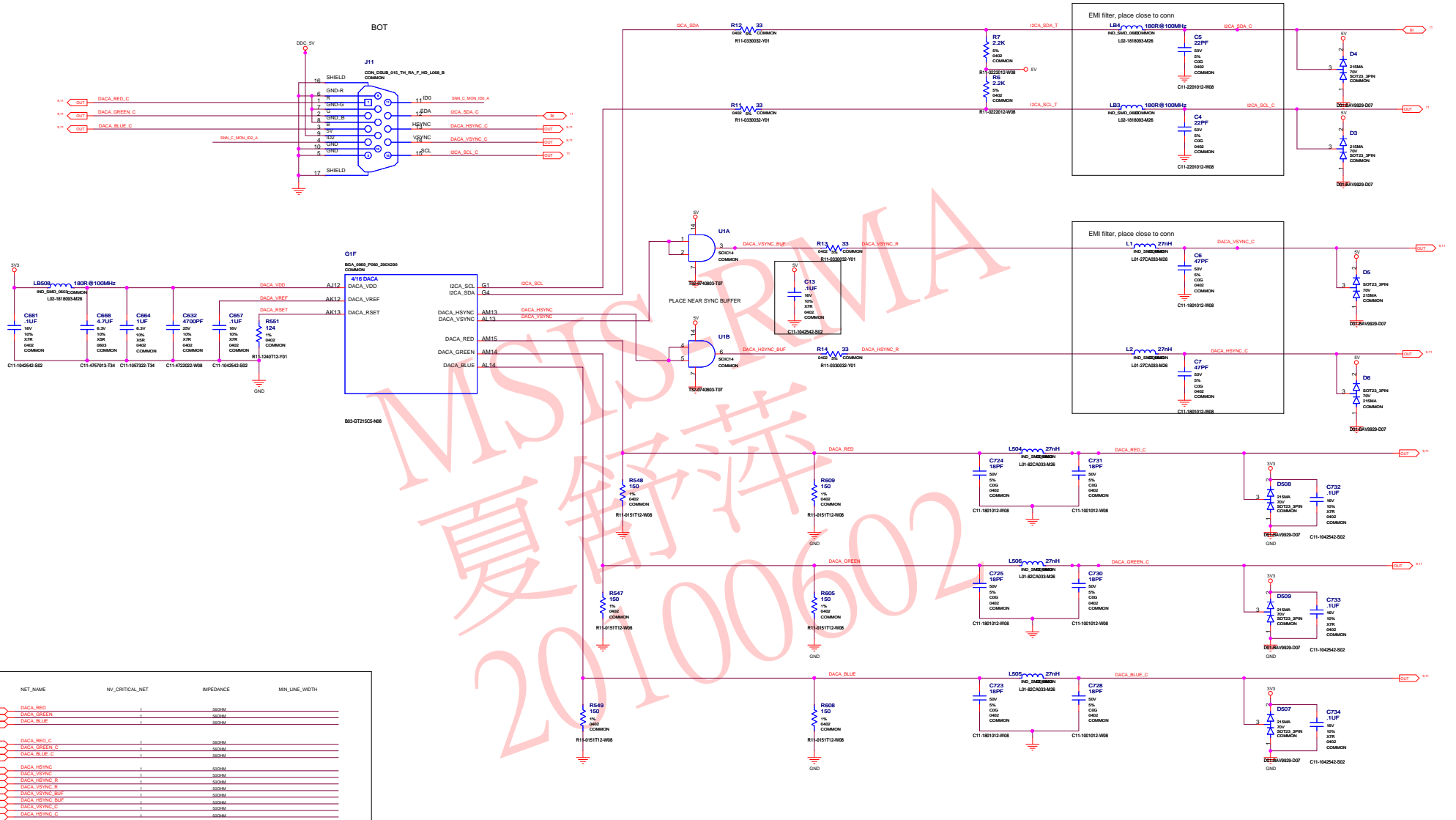
Decoupling for FBC 32..47



Decoupling for FBC 48..63



DACA (SOUTH DVI-I)



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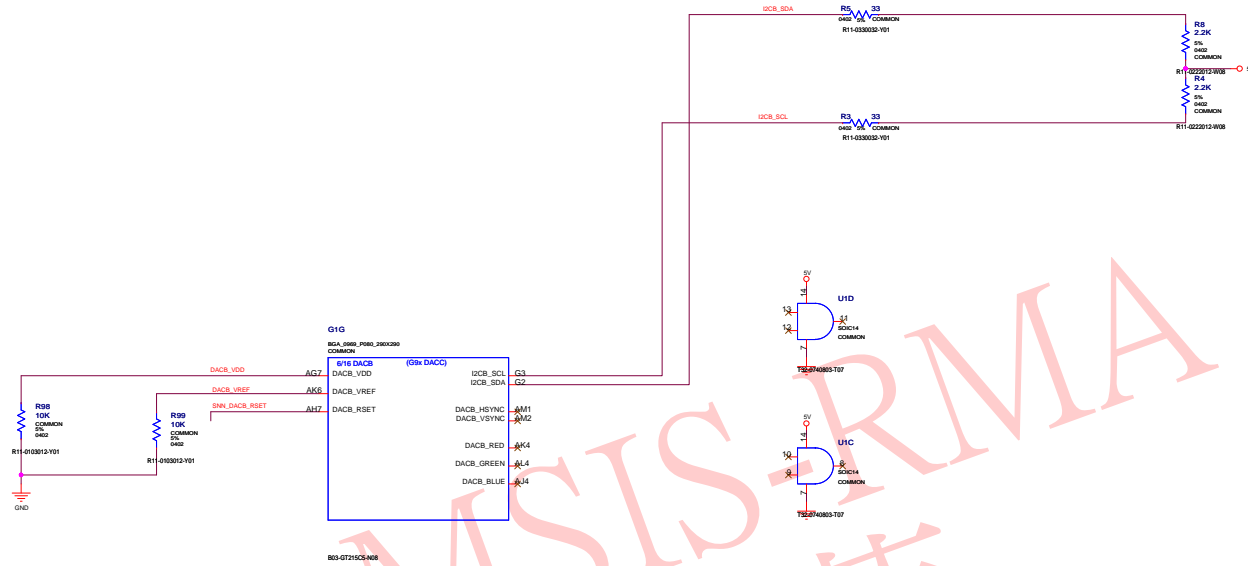
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DACB (cable-up VGA)

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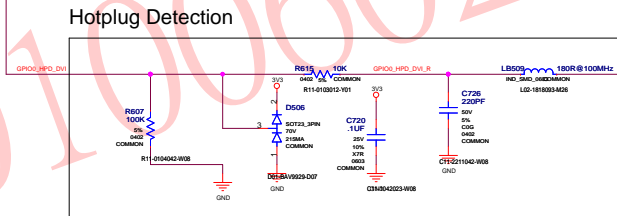
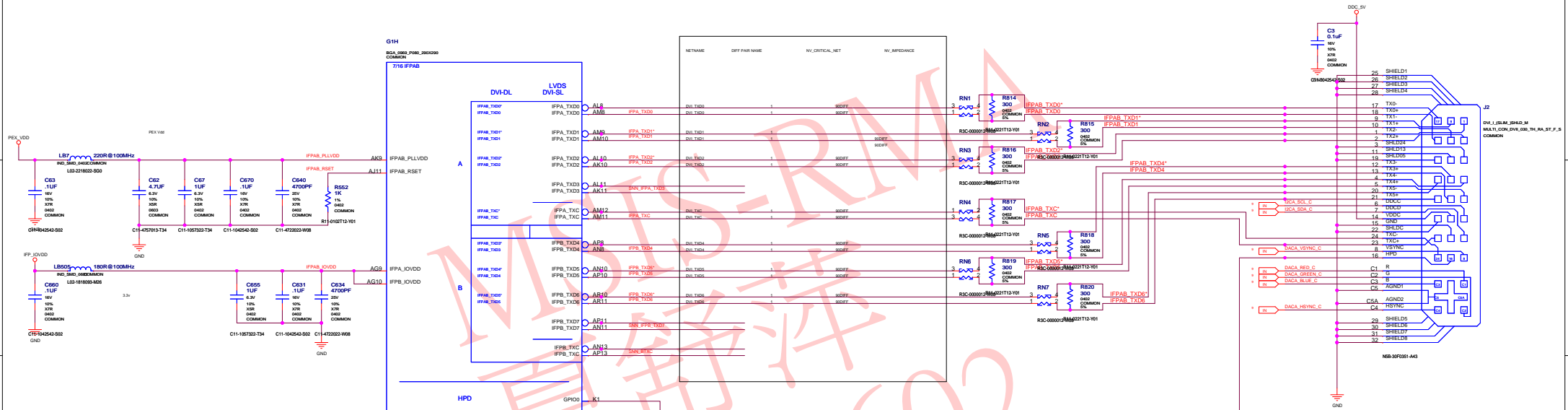
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IFP AB (SOUTH DVI-I)



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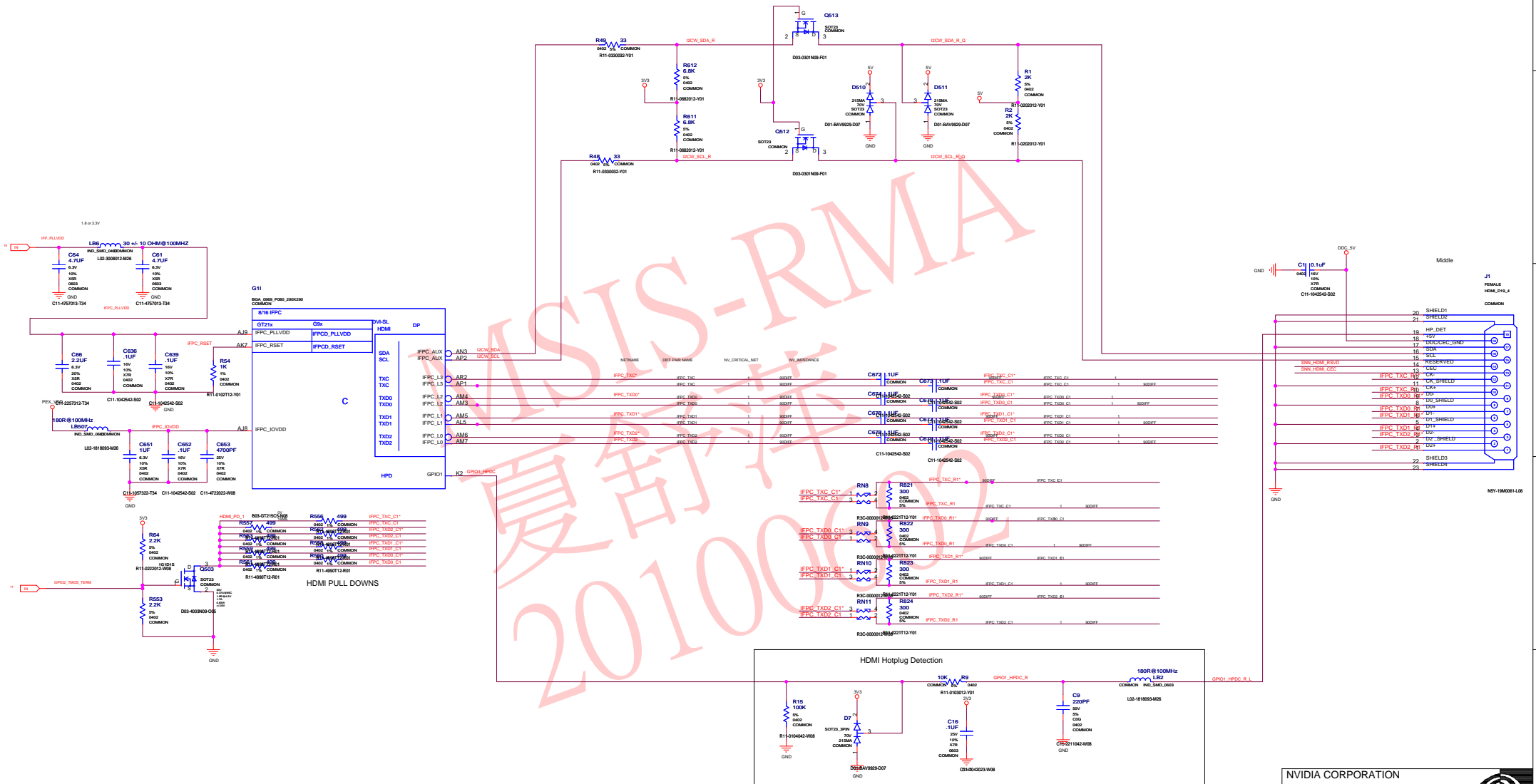
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IFP C (NORTH HDMI)



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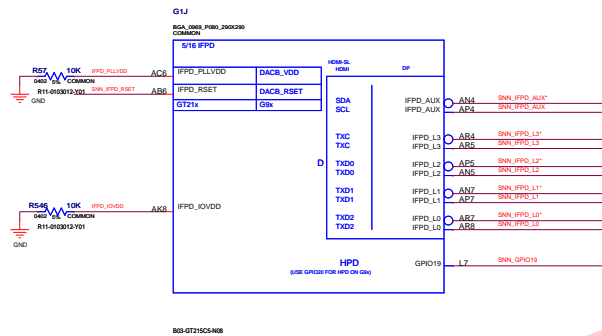


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IFP D (UNUSED)




| | |
|-----|---------------|
| AP4 | BNN_IPPO_AUX* |
| | BNN_IPPO_AUX |
| AP4 | BNN_IPPO_L3* |
| | BNN_IPPO_L3 |
| AP5 | BNN_IPPO_L3* |
| | BNN_IPPO_L3 |
| ANZ | BNN_IPPO_L3* |
| | BNN_IPPO_L3 |
| ANZ | BNN_IPPO_L3* |
| | BNN_IPPO_L3 |
| AP7 | BNN_IPPO_L3* |
| | BNN_IPPO_L3 |
| L7 | BNN_GPH019 |

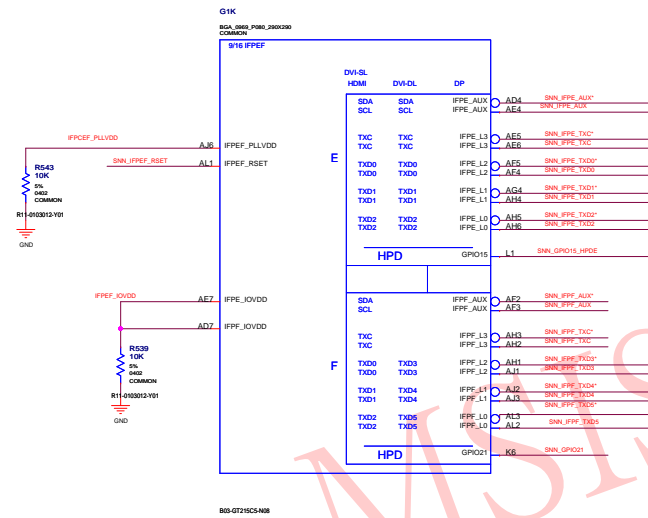
| | NET | PAIR | NV_CRITICAL | IMPEDANCE |
|-----|--------------|-------------|-------------|-----------|
| II | FPE_AUX_BYP | | 1 | |
| III | FPE_AUX_BYP* | FPE_AUX_BYP | 1 | SOJET |
| IV | | FPE_AUX_BYP | | SOJET |

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| ASSEMBLY | BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL |
| PAGE DETAIL | IFP D (UNUSED) & MID DISPLAYPORT |

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IFP EF (unused)

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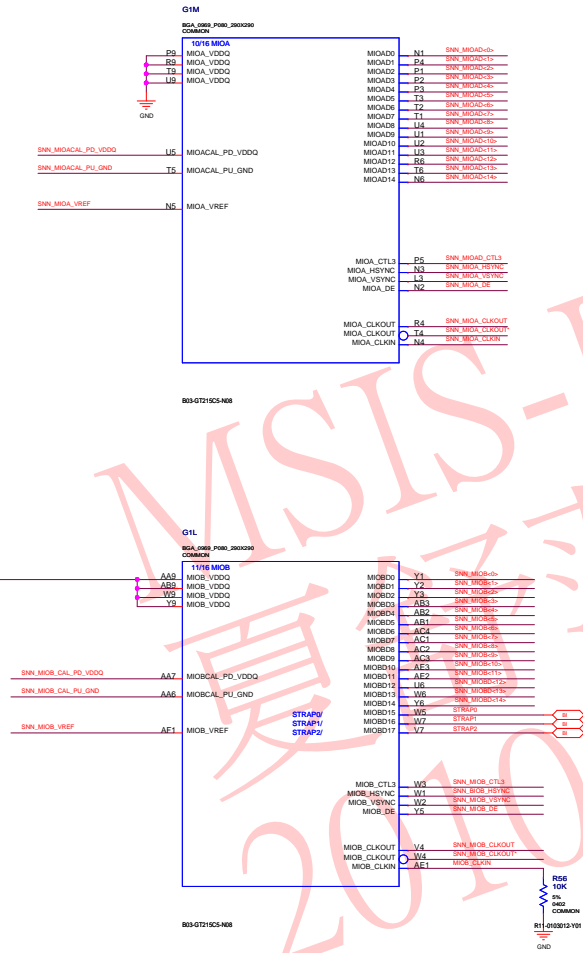
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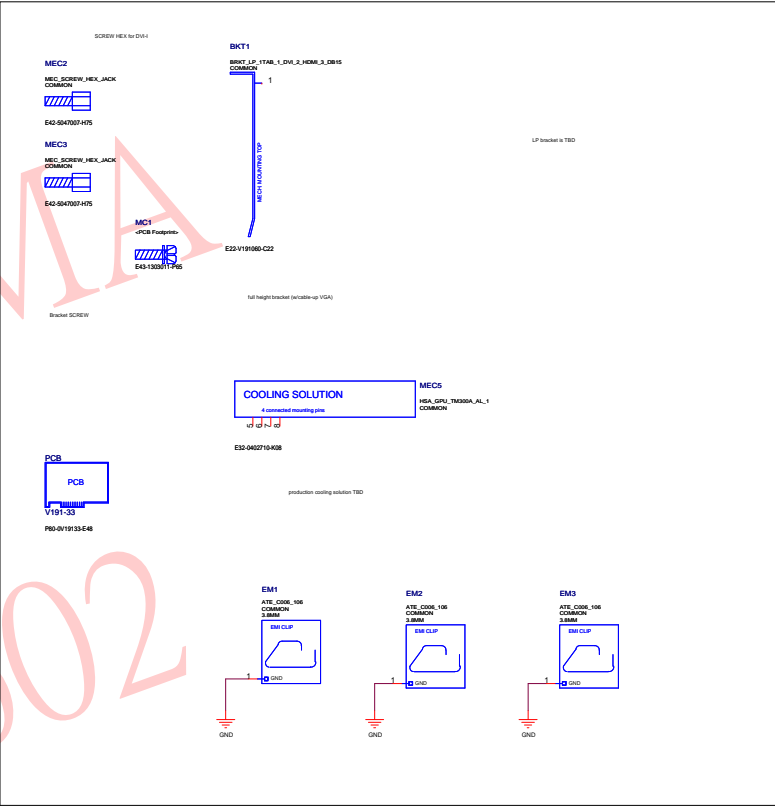
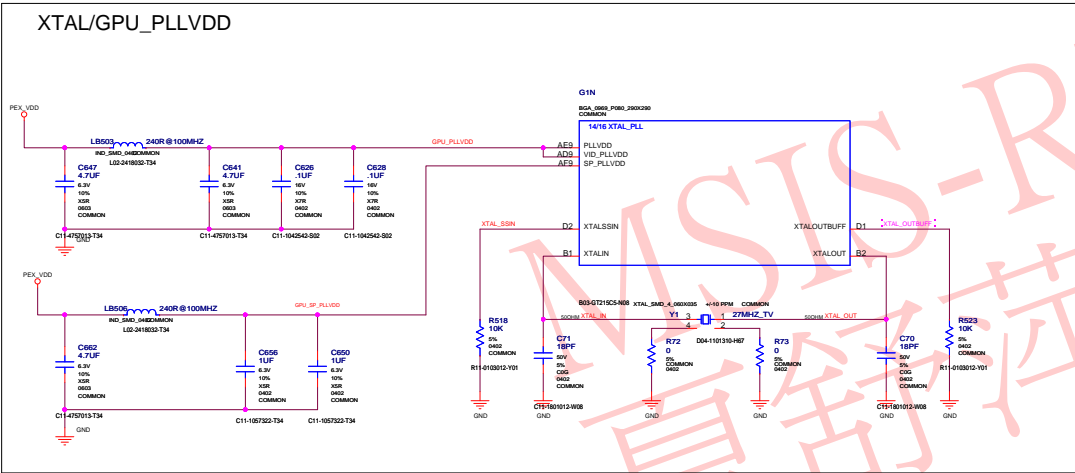


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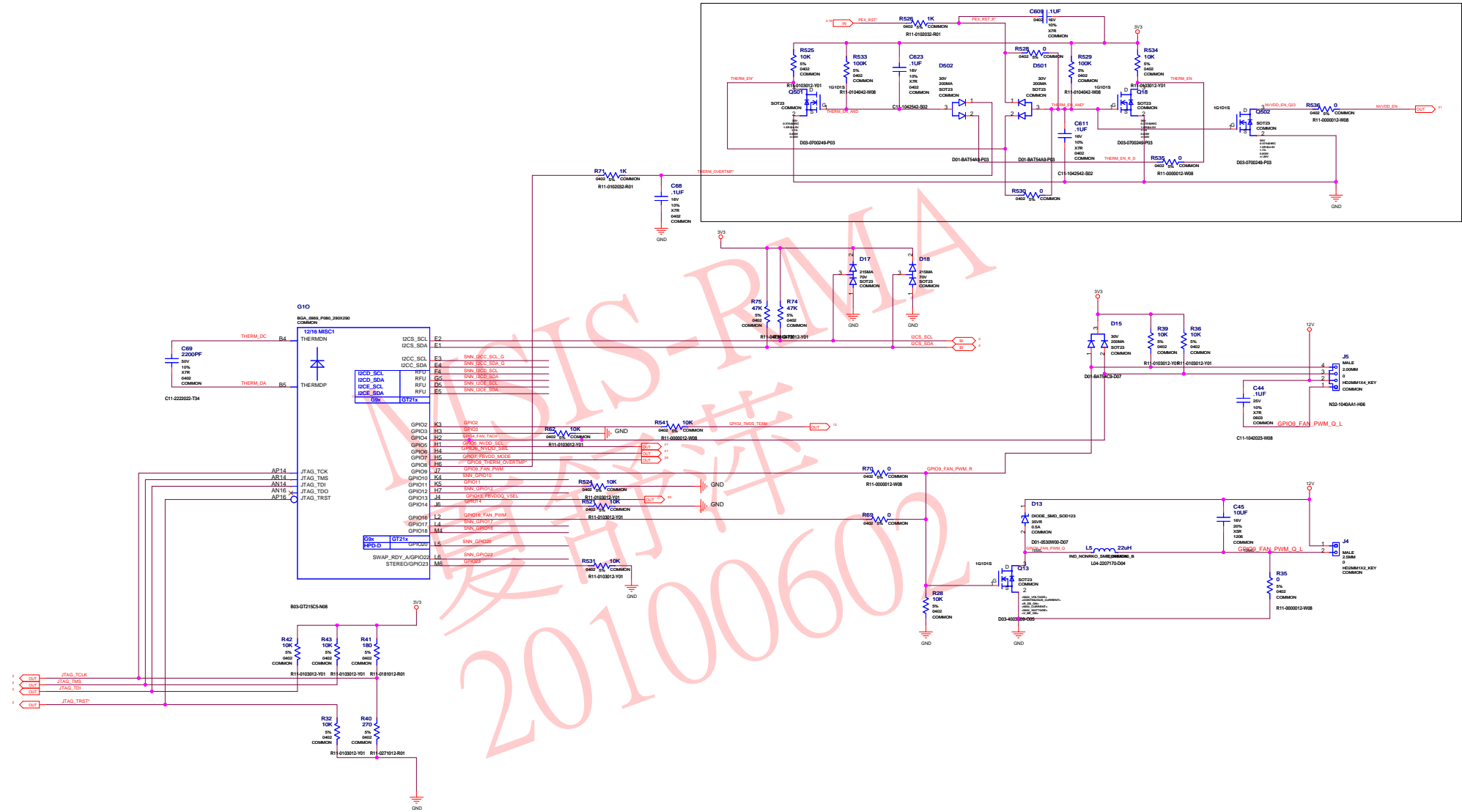
XTAL, MECHANICALS, THERMALS



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FAN CONTROL, GPIO, JTAG

OVERTEMP LATCH



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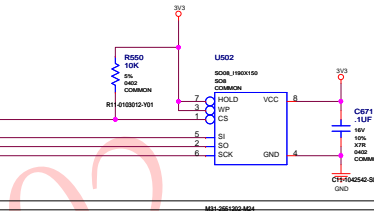
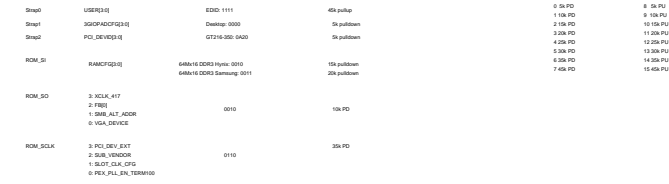


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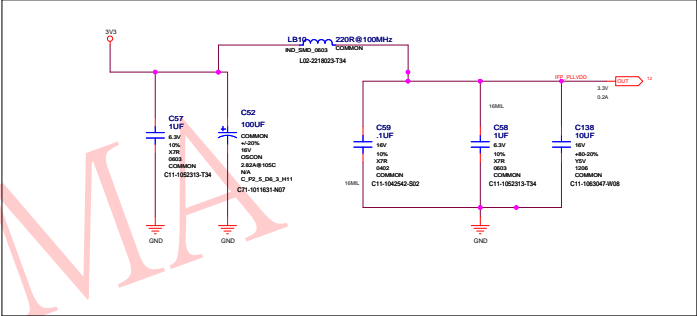
STRAPPING OPTIONS



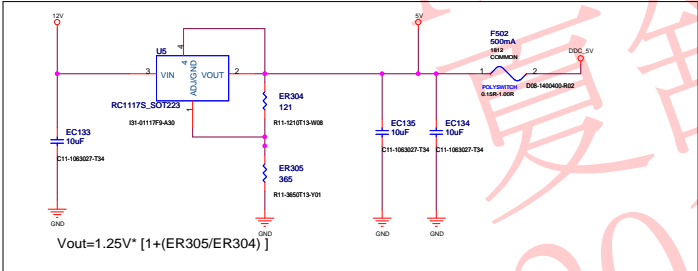
| | MULTI_STRAP_REF1_GND | MULTI_STRAP_REF0_GND |
|-------------------------------|----------------------|----------------------|
| BINARY PRODUCTION STRAP MODE: | 40.2K 1% TO GND | NC |
| BINARY BRINGUP STRAP MODE: | NC | NC |
| MULTI-LEVEL STRAP MODE: | 40.2K 1% TO GND | 40.2K 1% TO GND |

LINEAR POWER SUPPLIES

IFP_PLLVDD SUPPLY

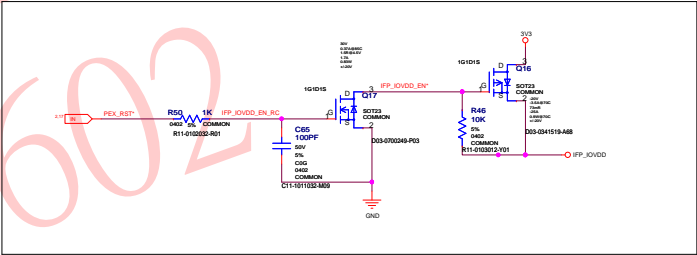


5V & DDC_5V REGULATOR



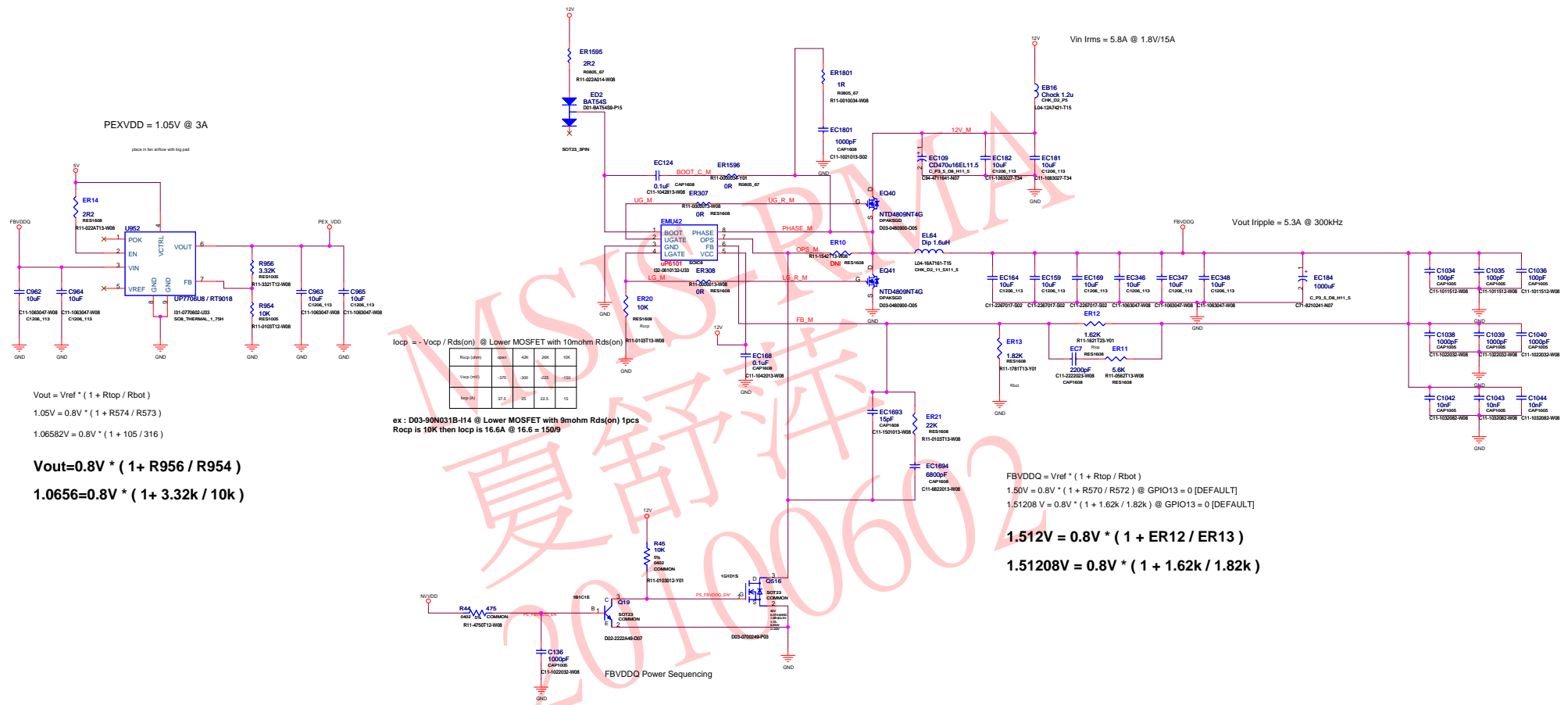
5.0206 = 1.25V * [1+(ER305/ER304)]

IFP_IOVDD BACKDRIVE PREVENTION



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FBVDDQ/PEXVDD POWER SUPPLY



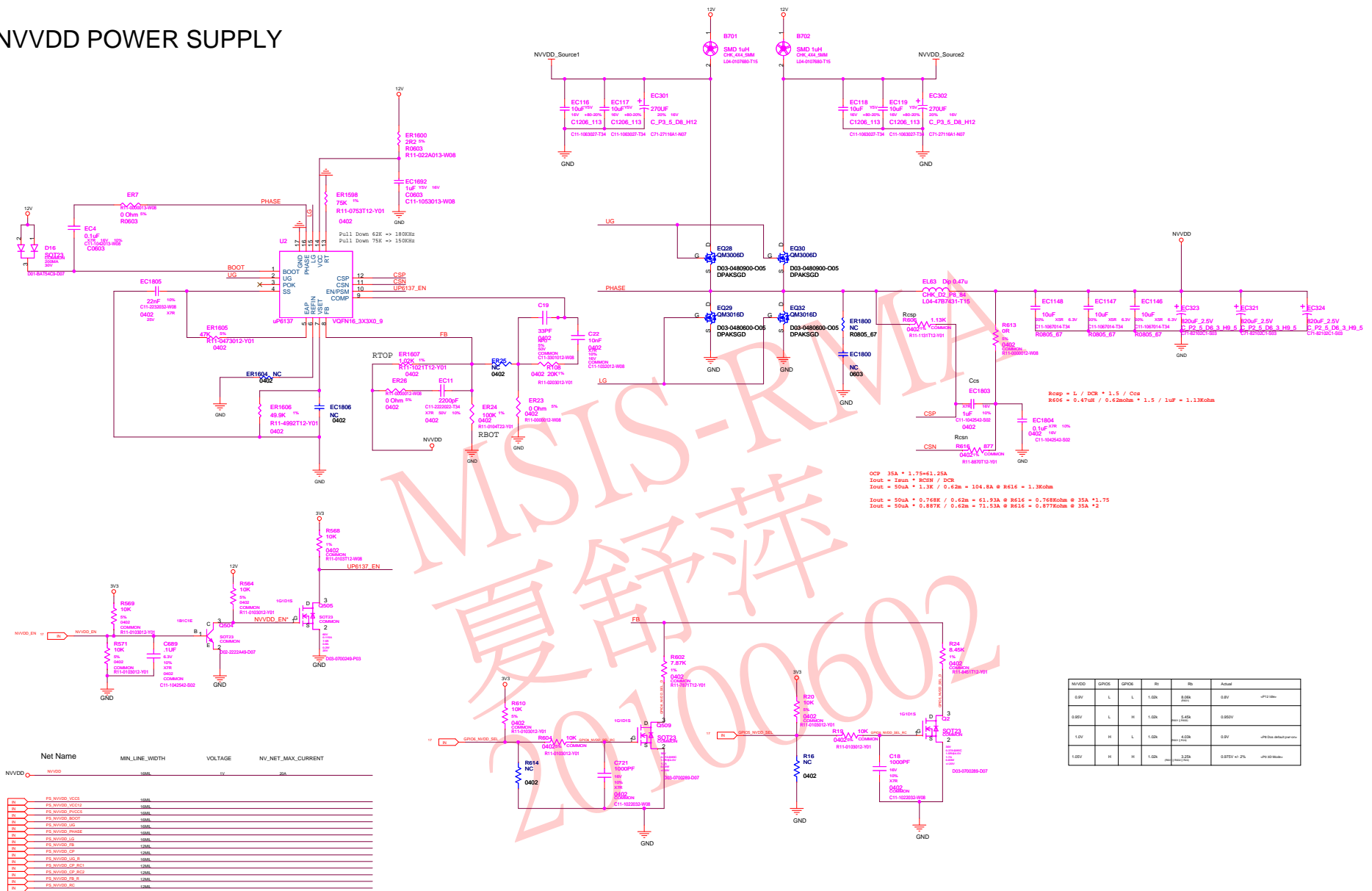
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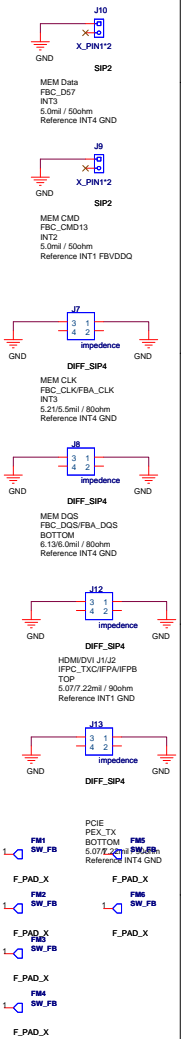
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NVVDD POWER SUPPLY



| INVID | GPIC | GPIC | R ₁ | R ₂ | Actual |
|-------|------|------|----------------|-----------------|--------------|
| 0.5V | L | L | 1.02k | 0.05k (50k) | 0.8V |
| 0.55V | L | H | 1.02k | 5.42k (5.4k) | 0.95V |
| 1.0V | H | L | 1.02k | 4.02k (4.0k) | 0.8V |
| 1.05V | H | H | 1.02k | 3.25k (3.2k) | 0.975V ±1-2% |



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| ASSEMBLY | BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL |
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