

# PG150-C03

384b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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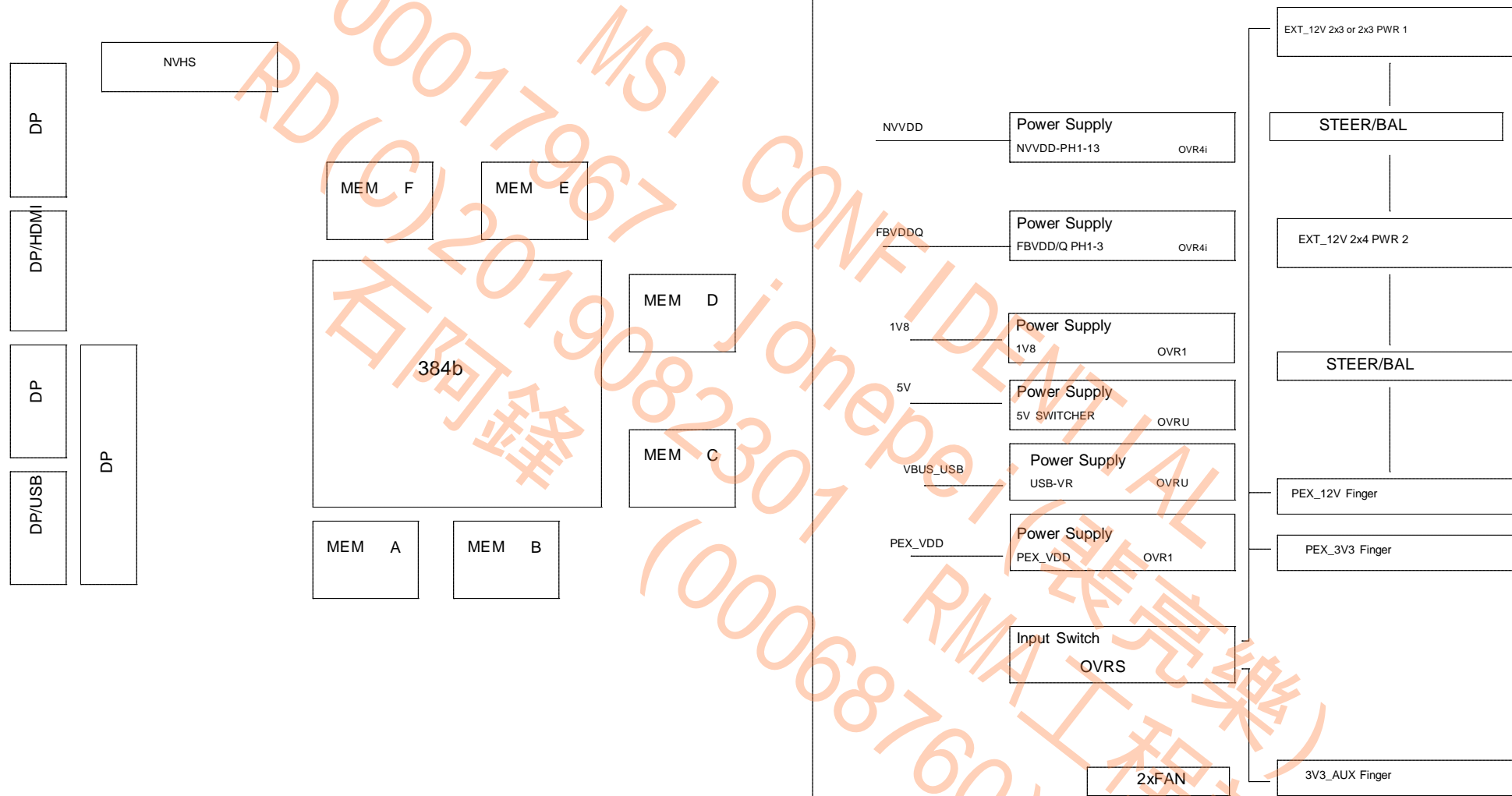
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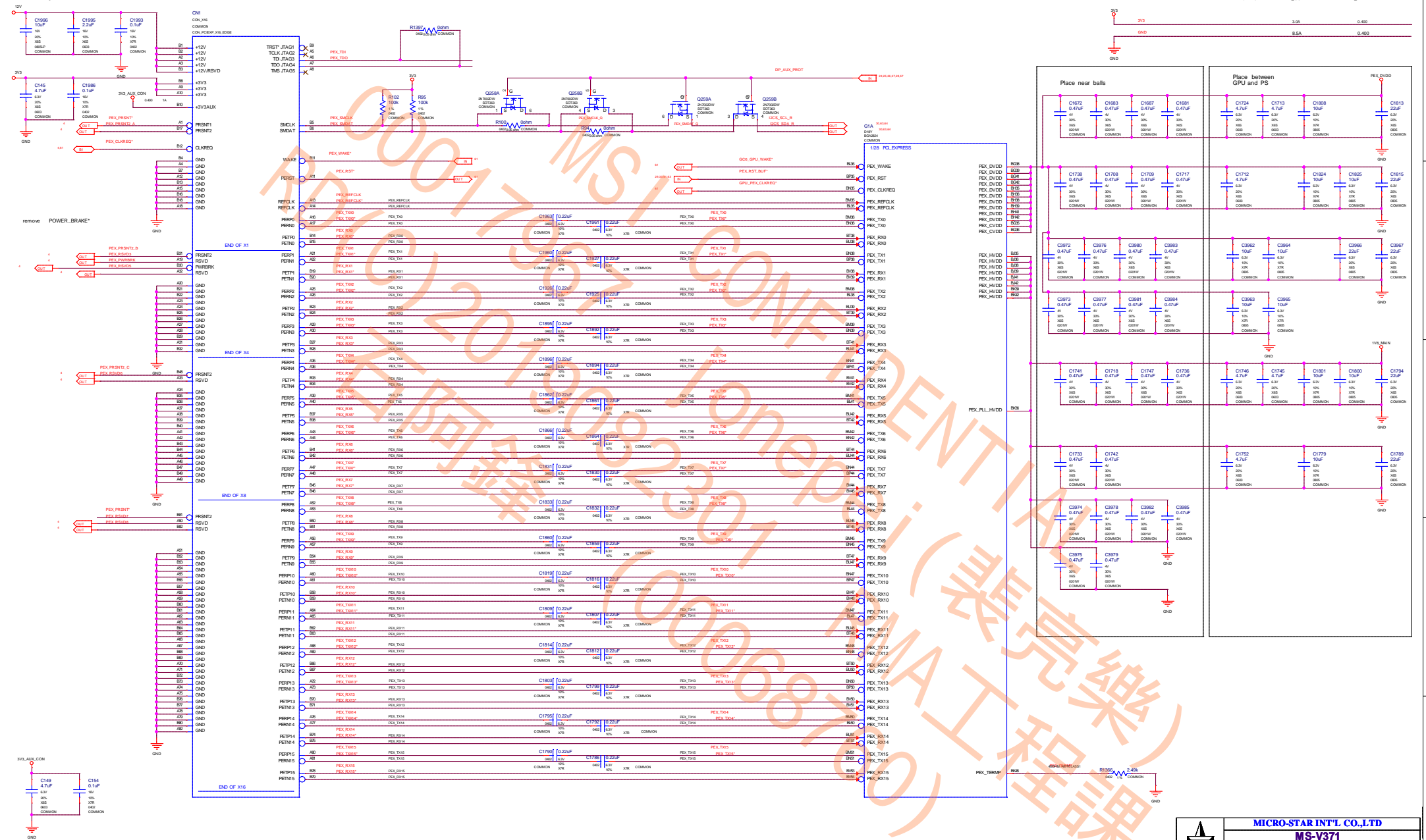
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Block Diagram



PCI Express



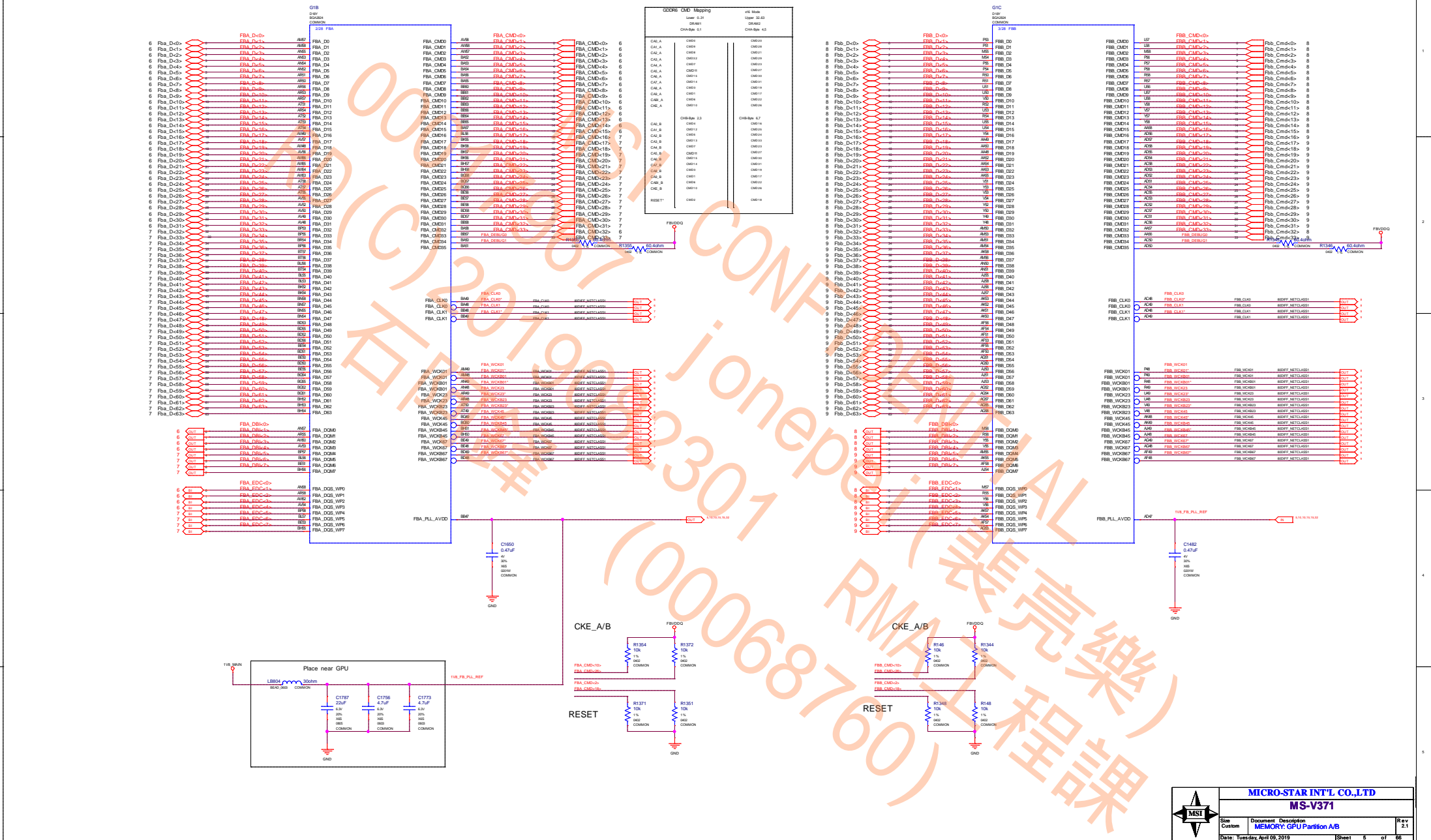
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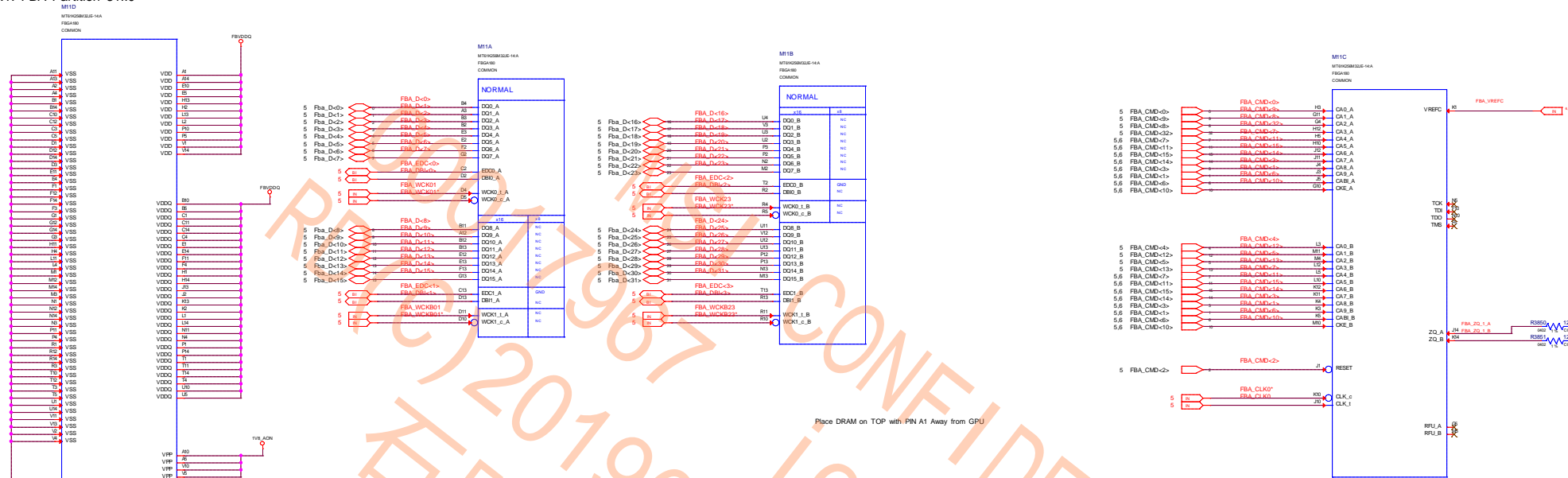
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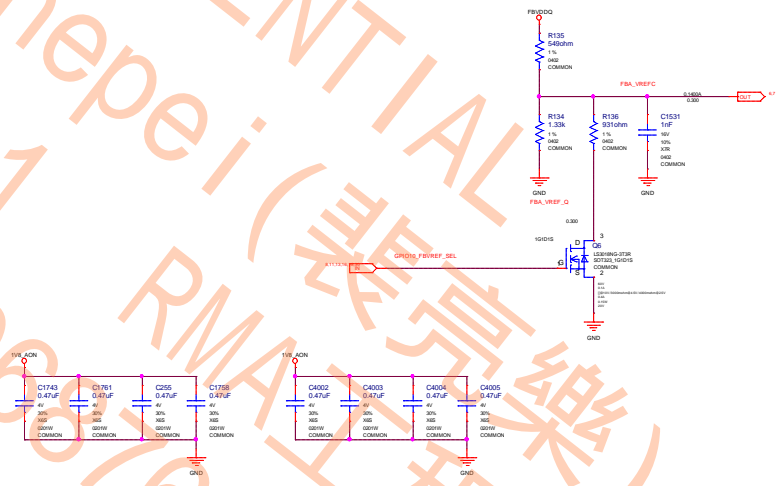
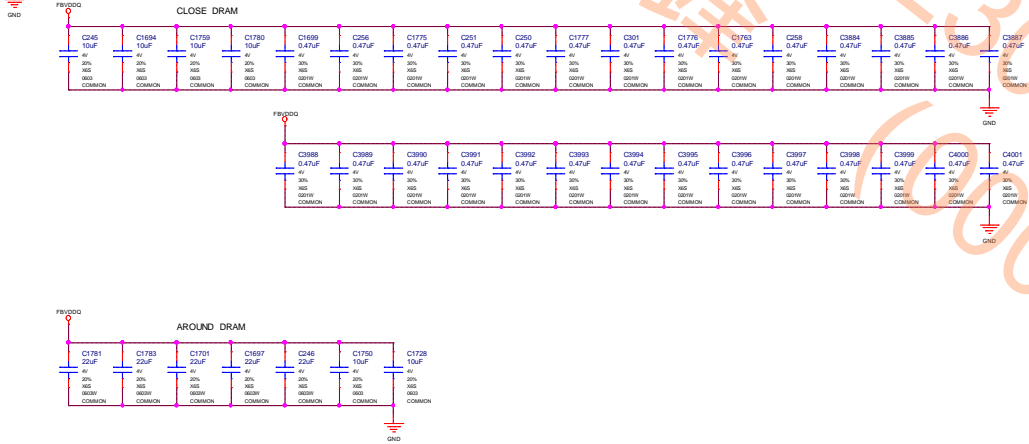
MEMORY: GPU Partition A/B



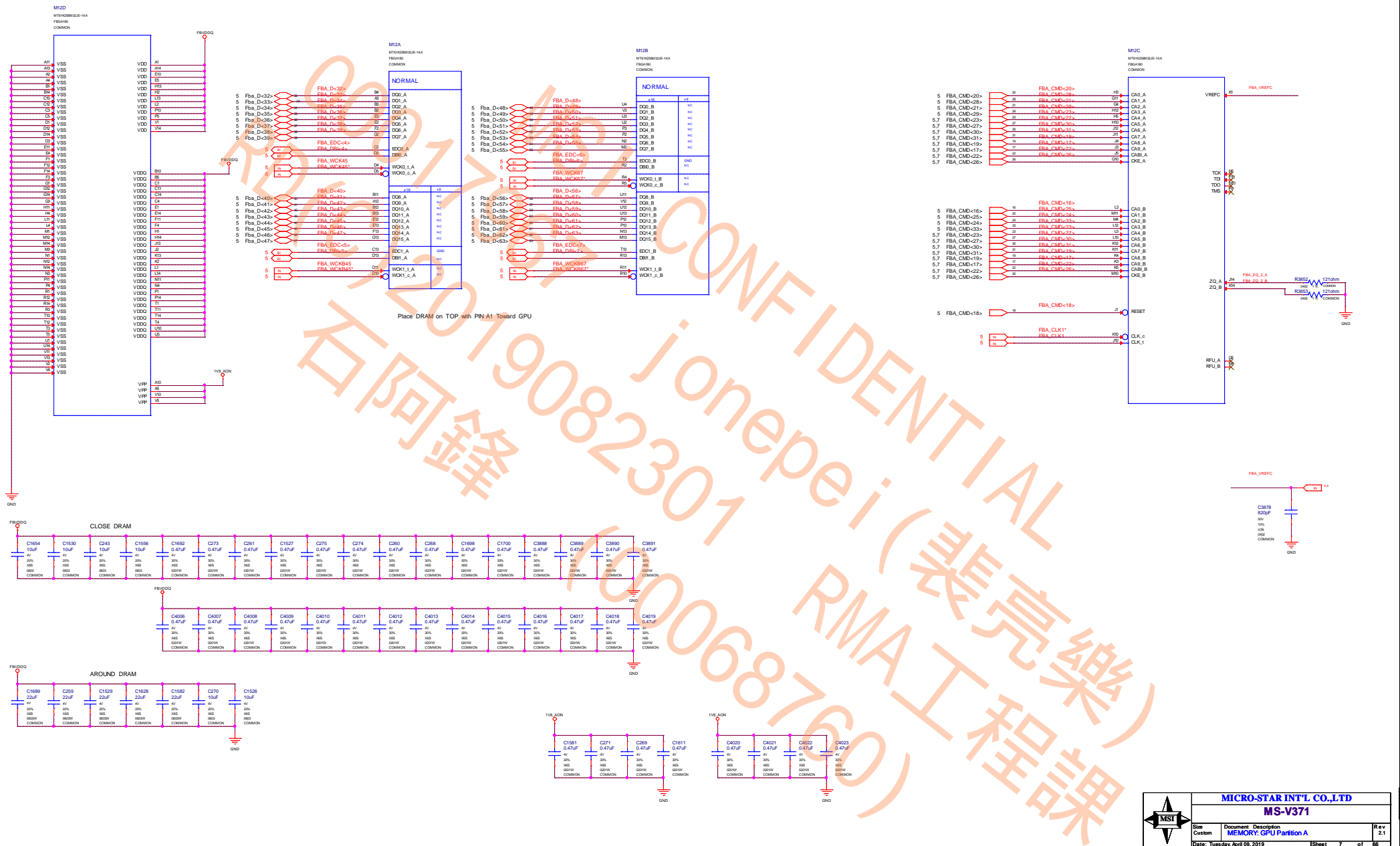
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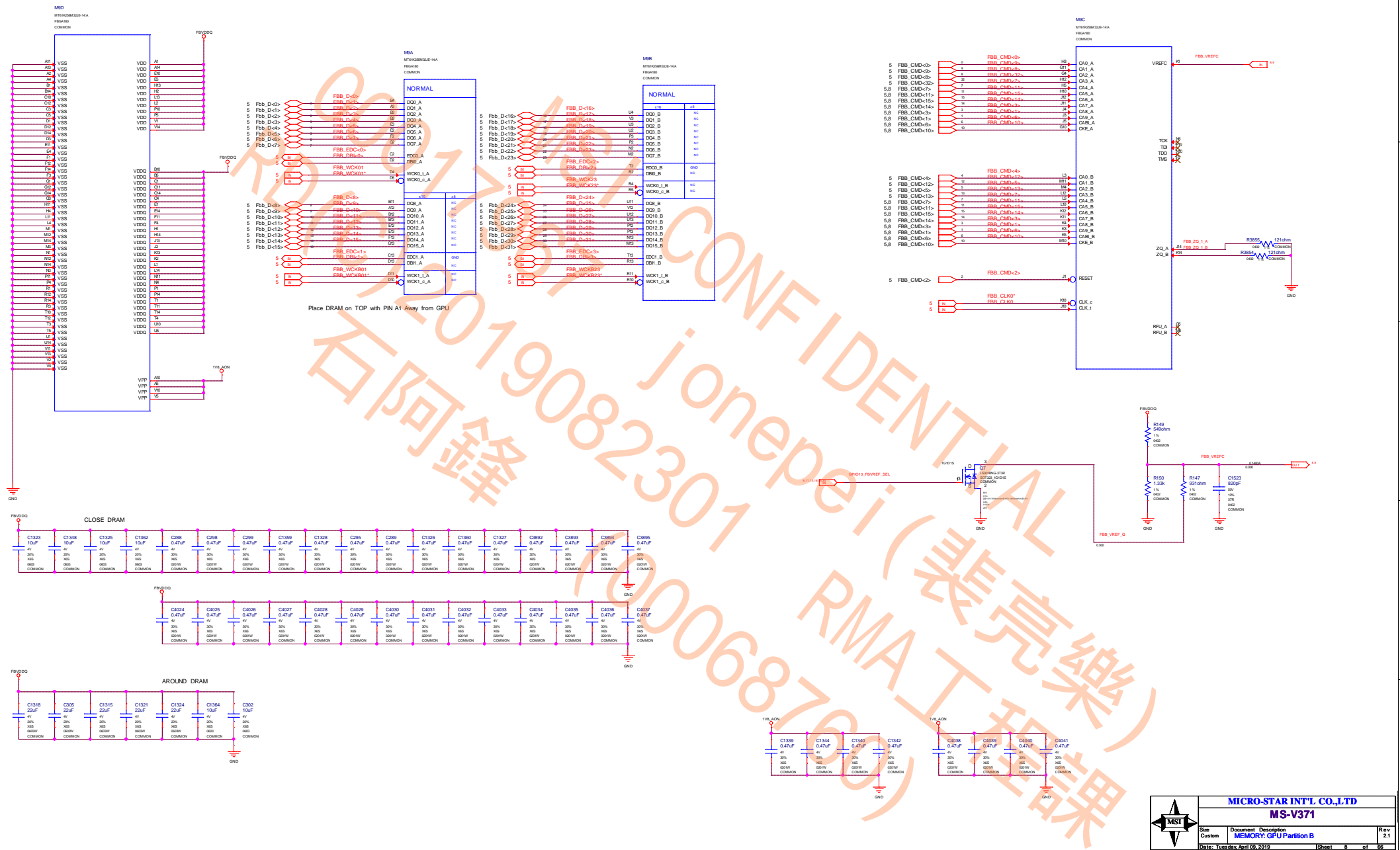


Place DRAM on TOP with PN A1 Away from GPU

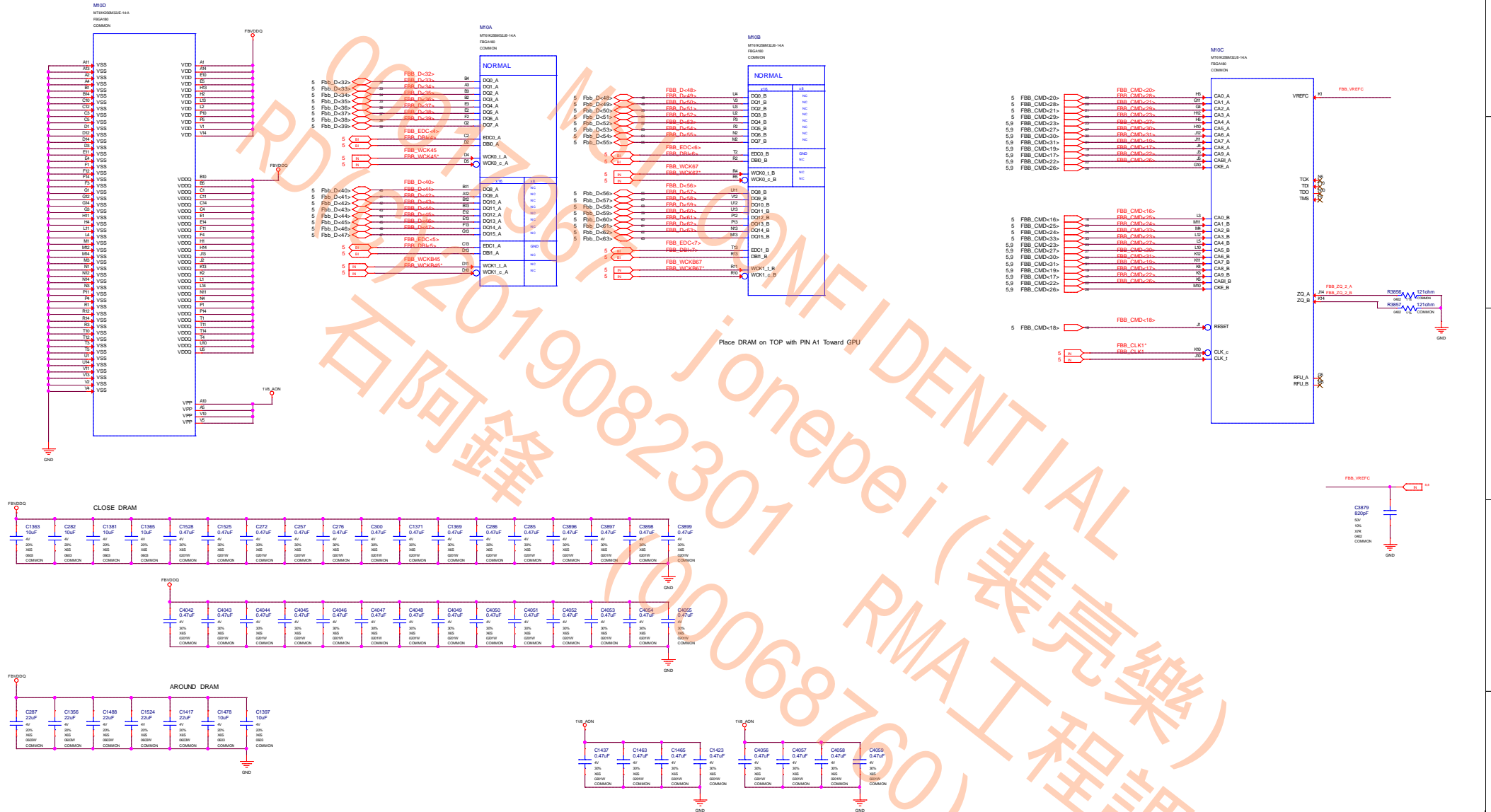




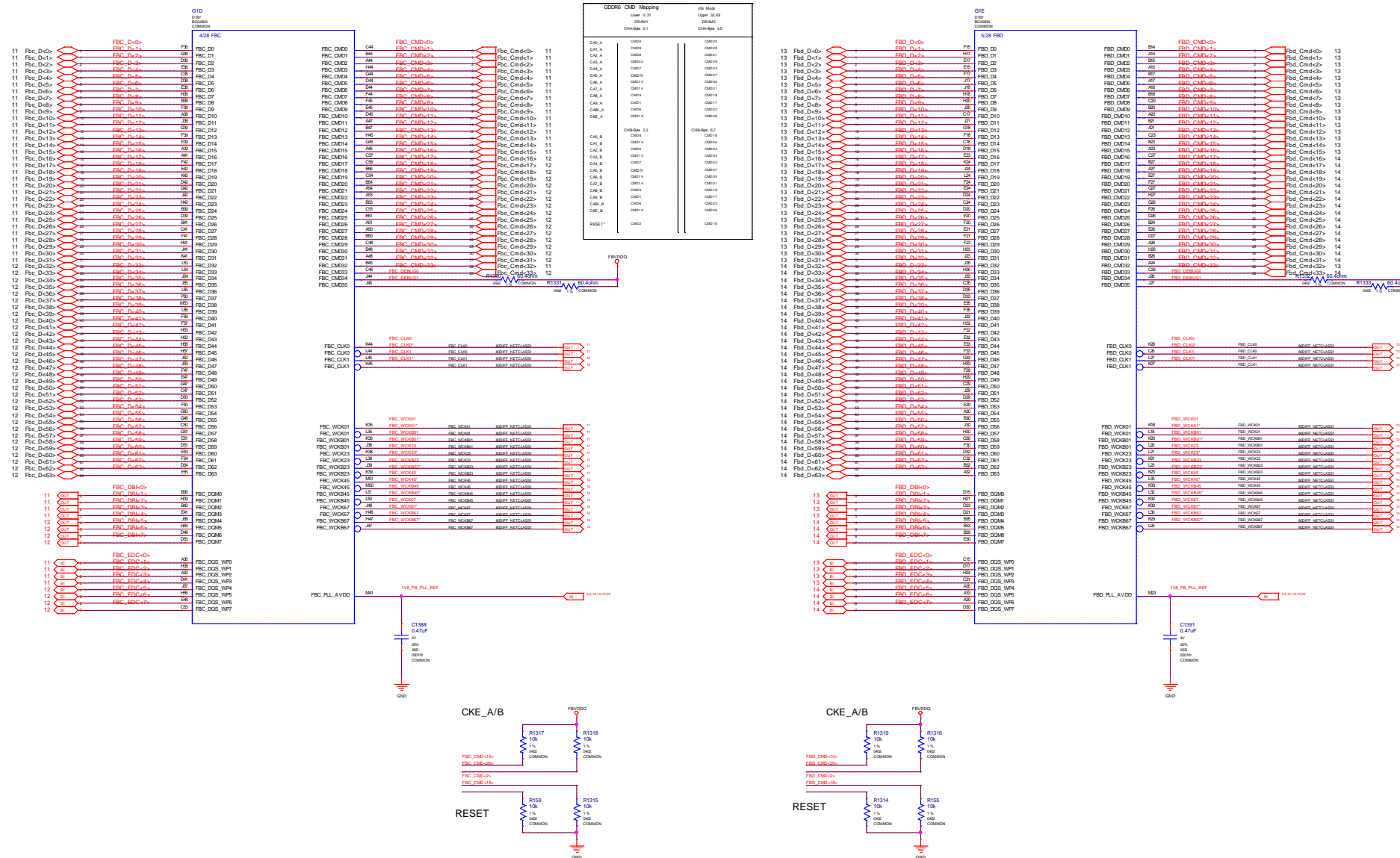




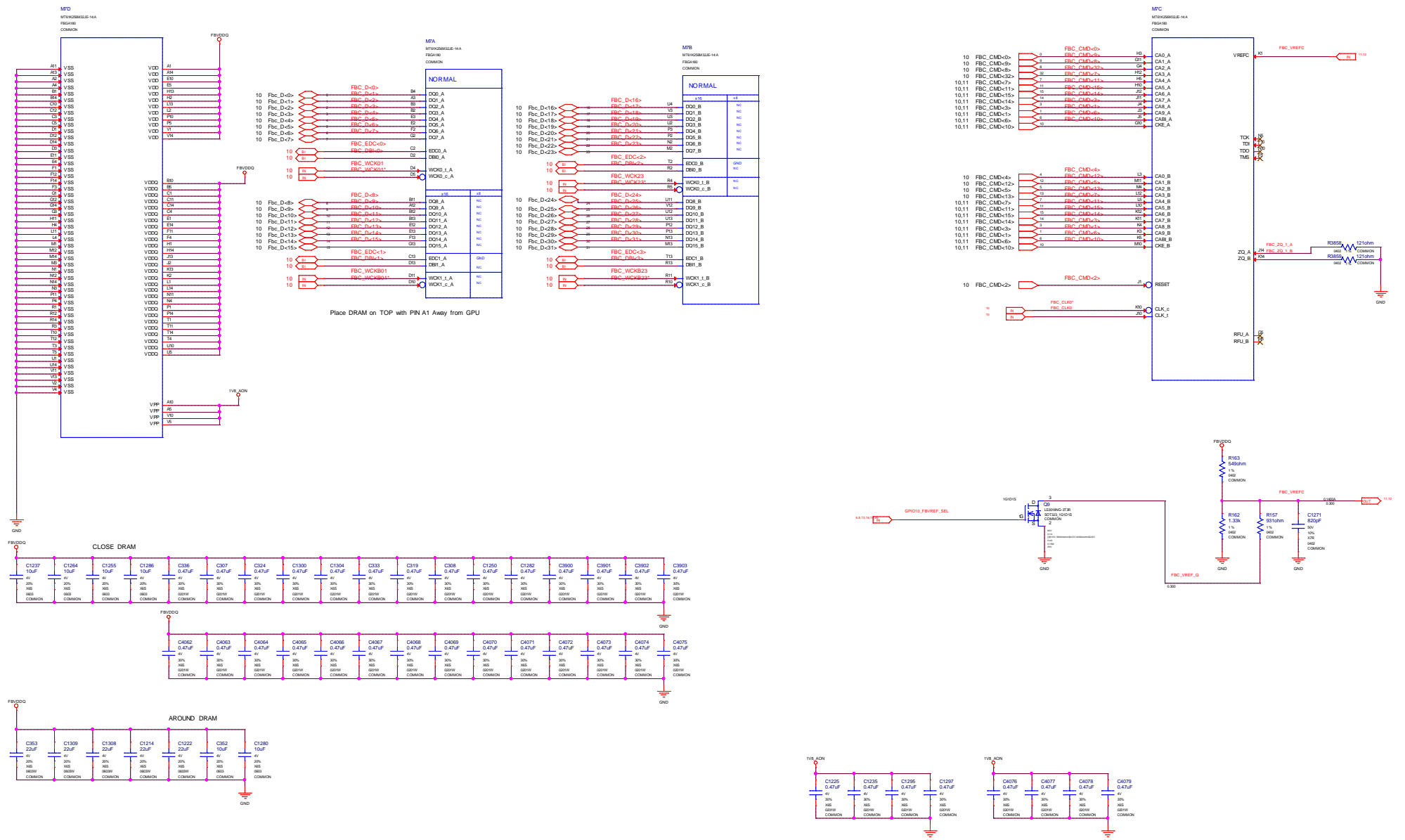


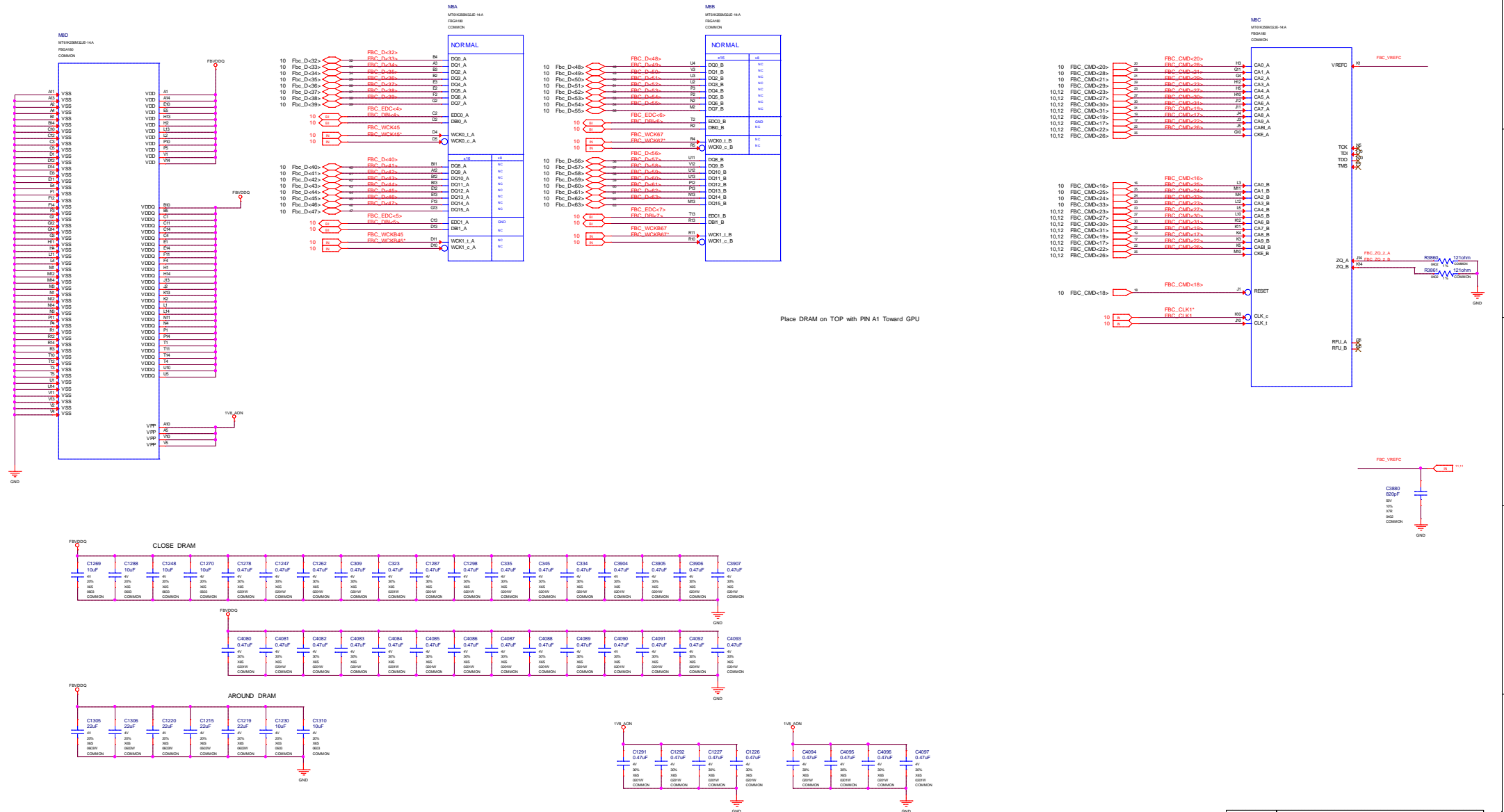


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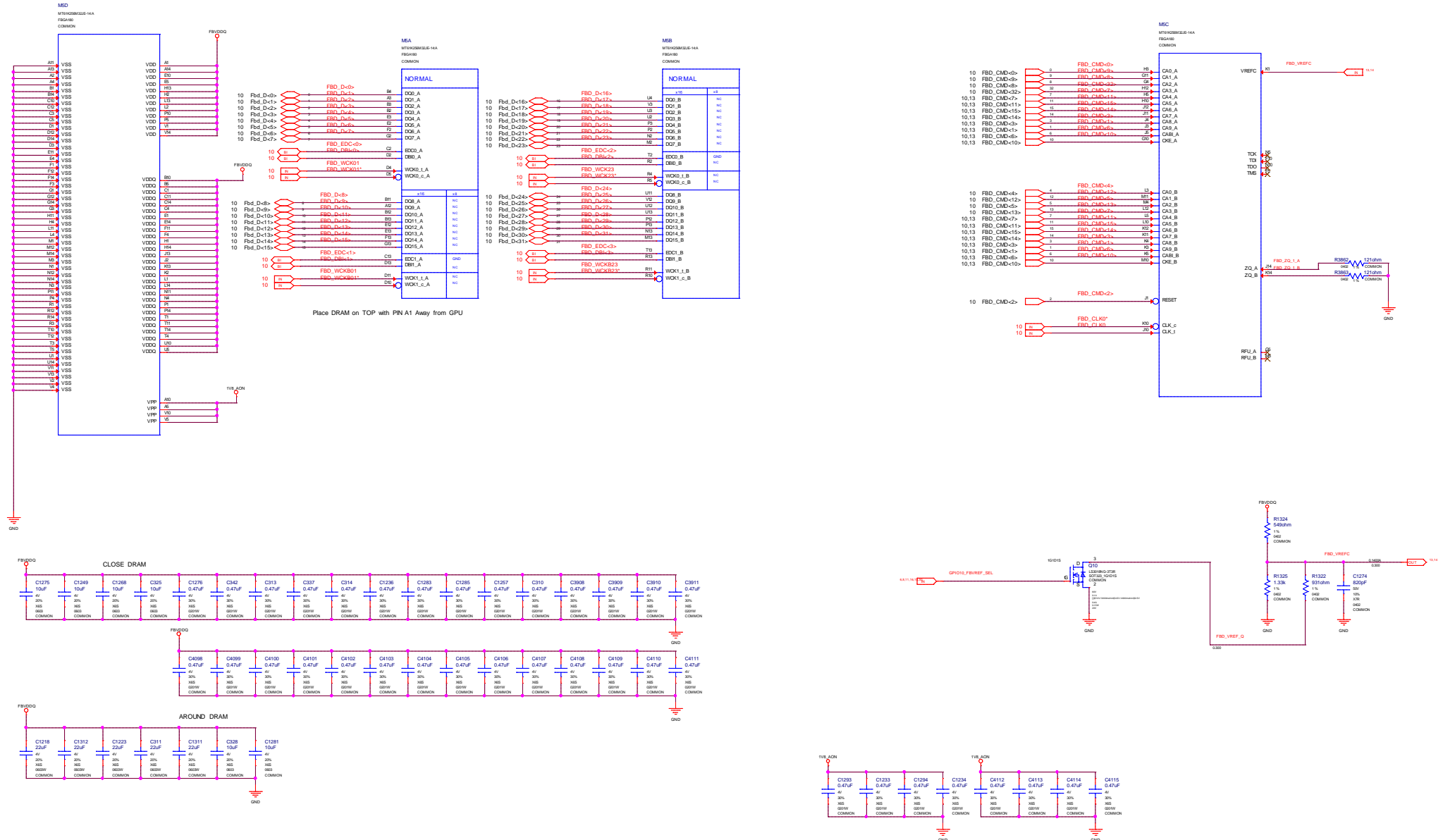


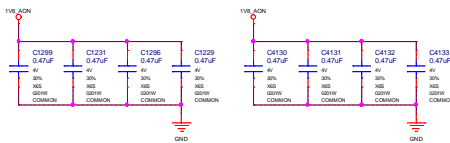
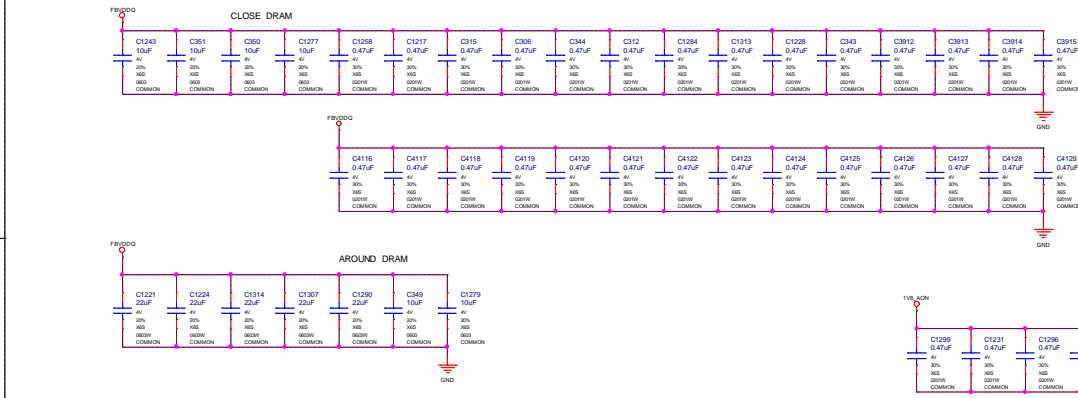
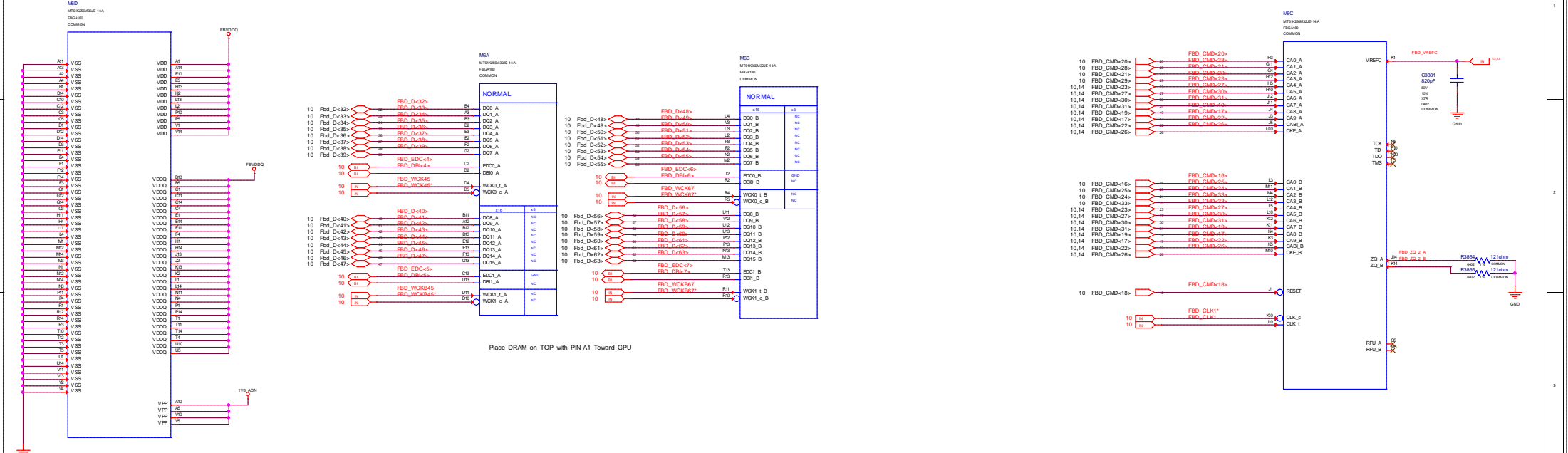
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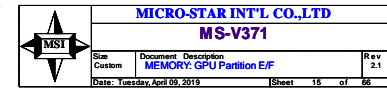


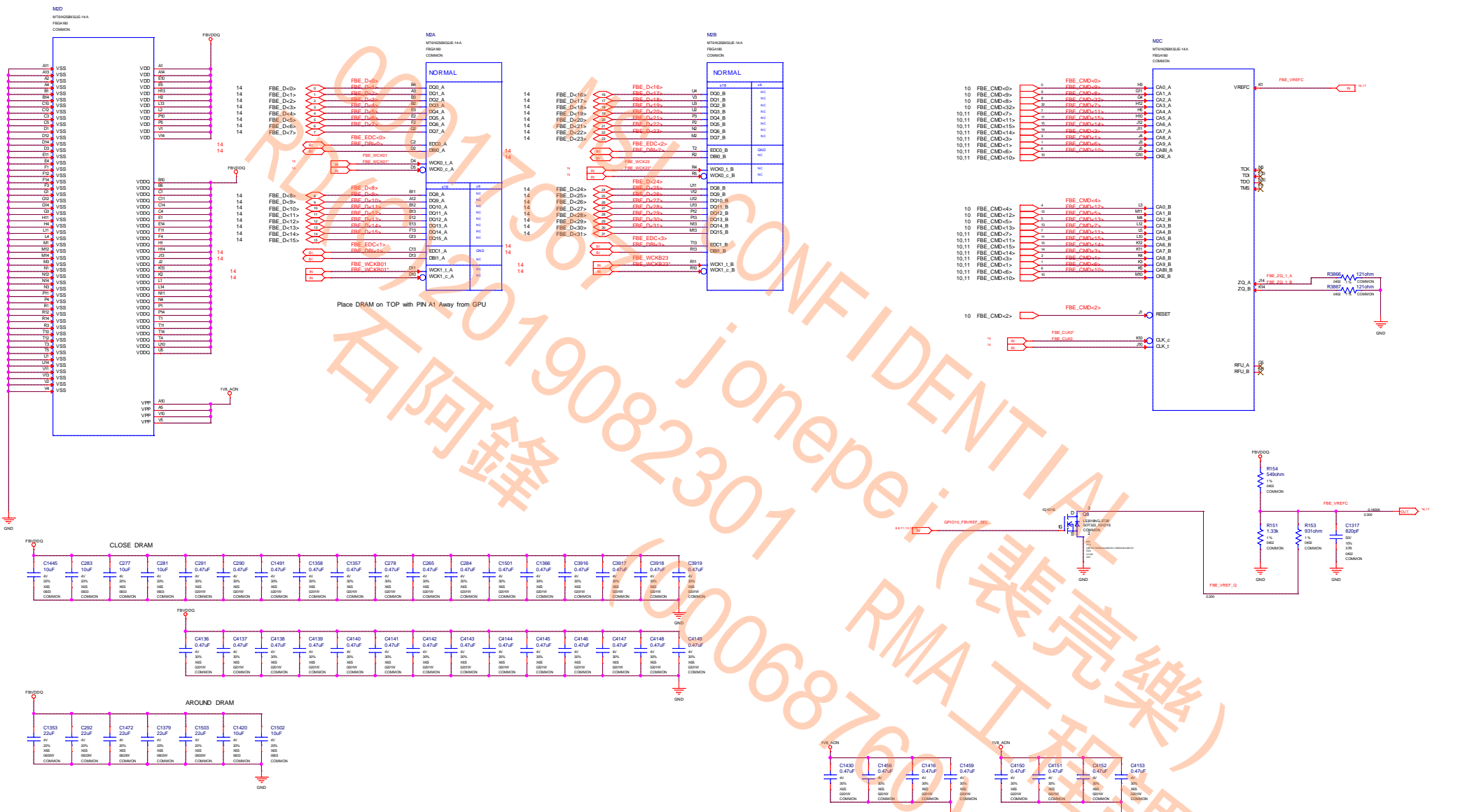
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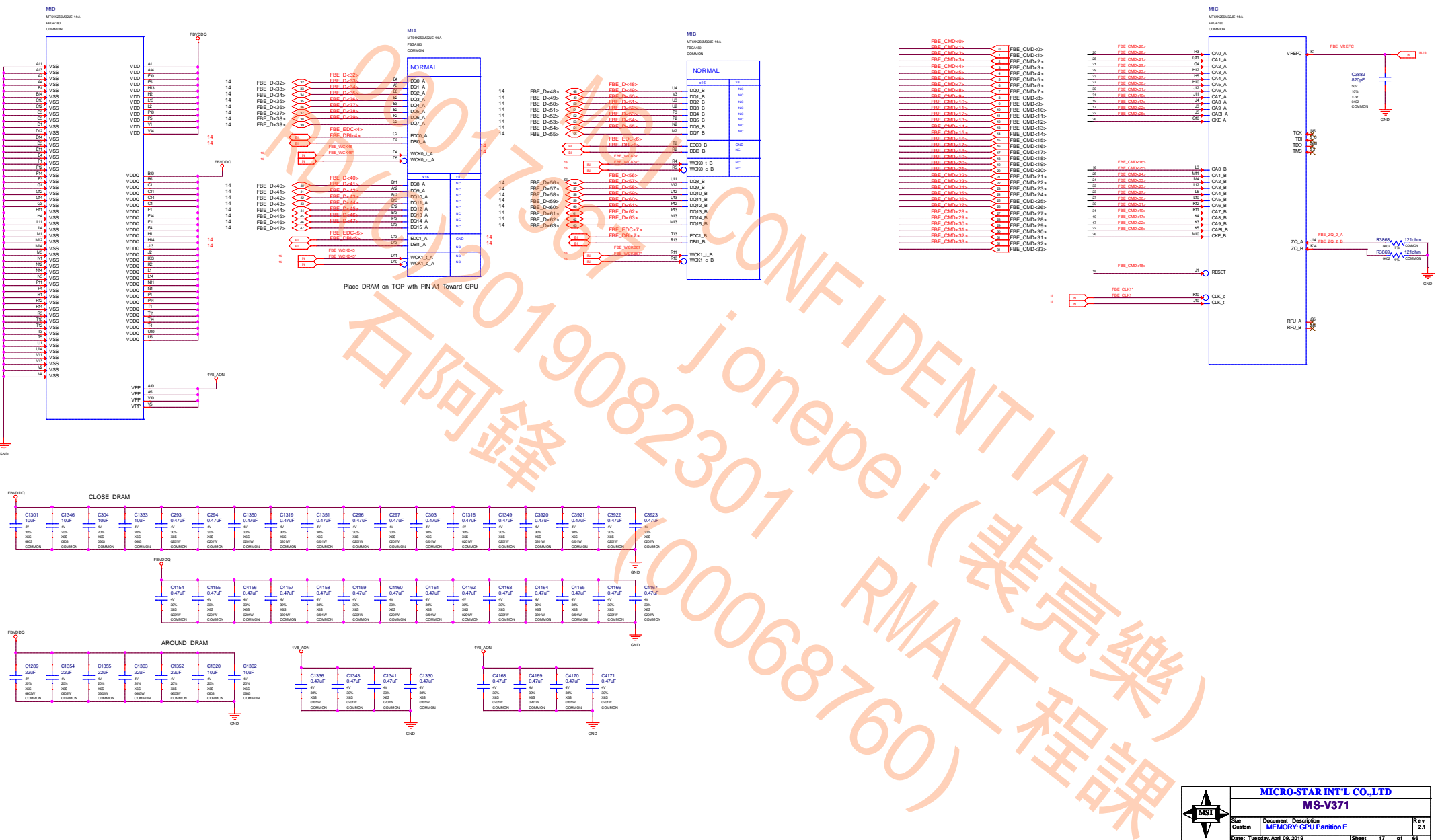


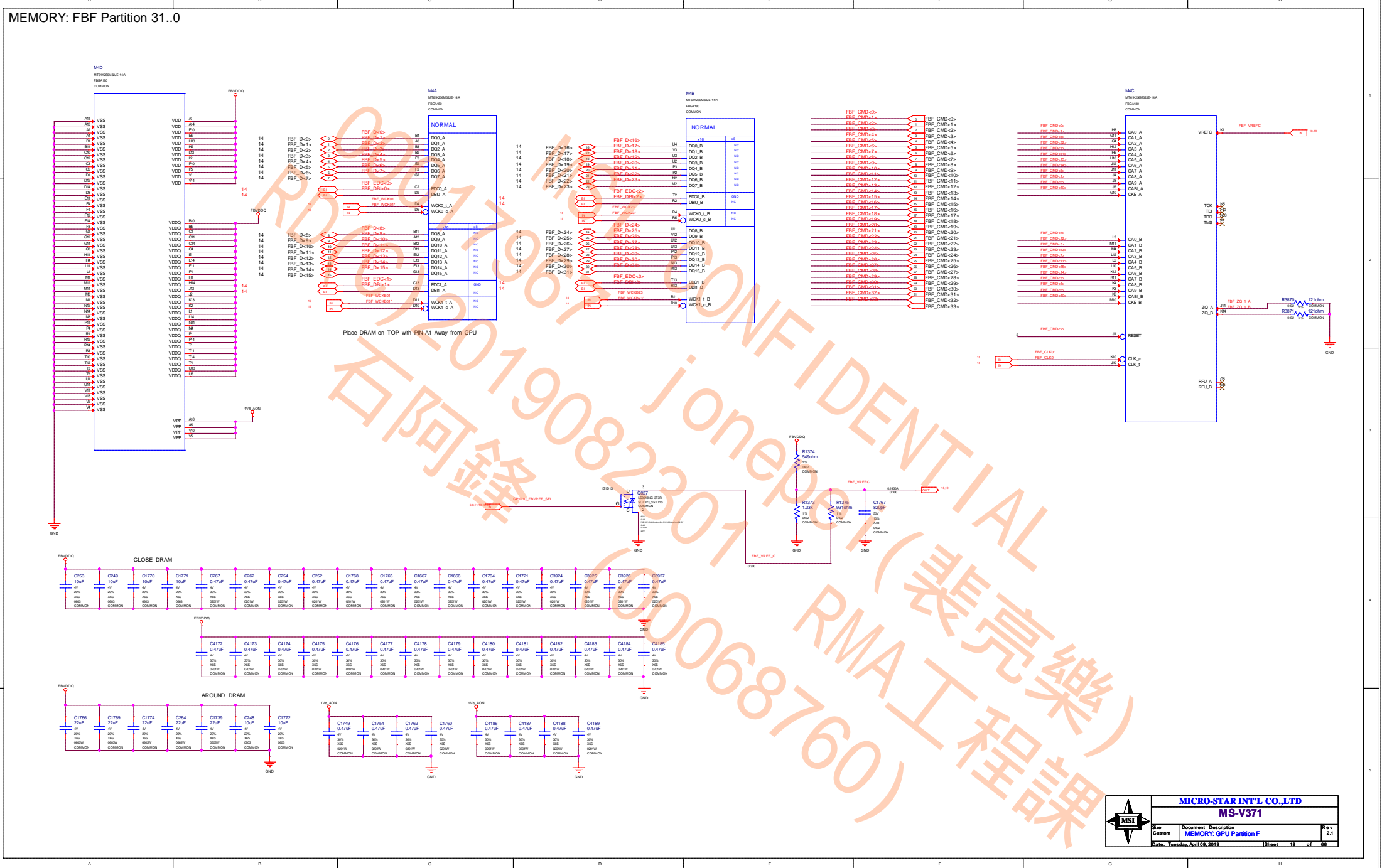


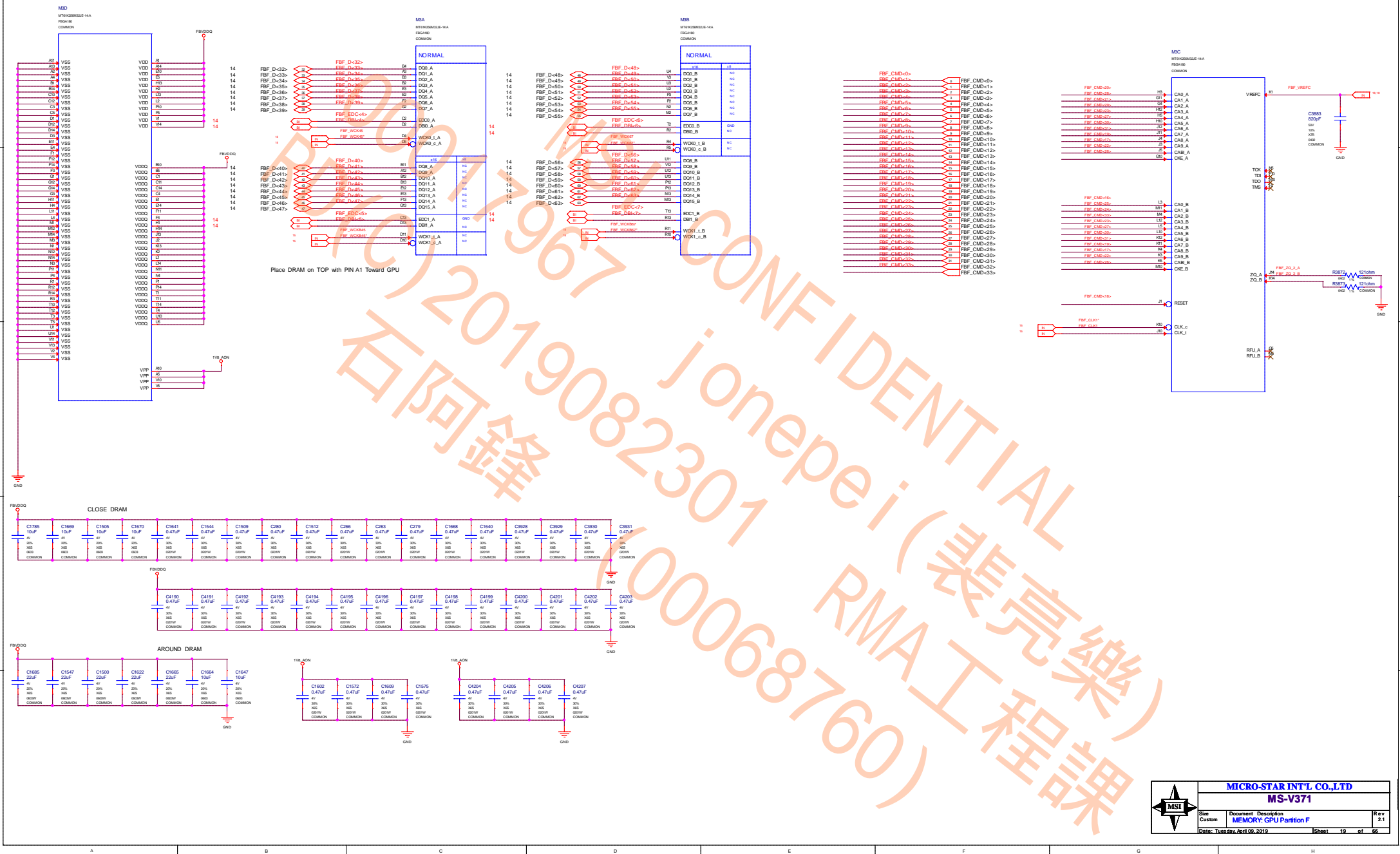






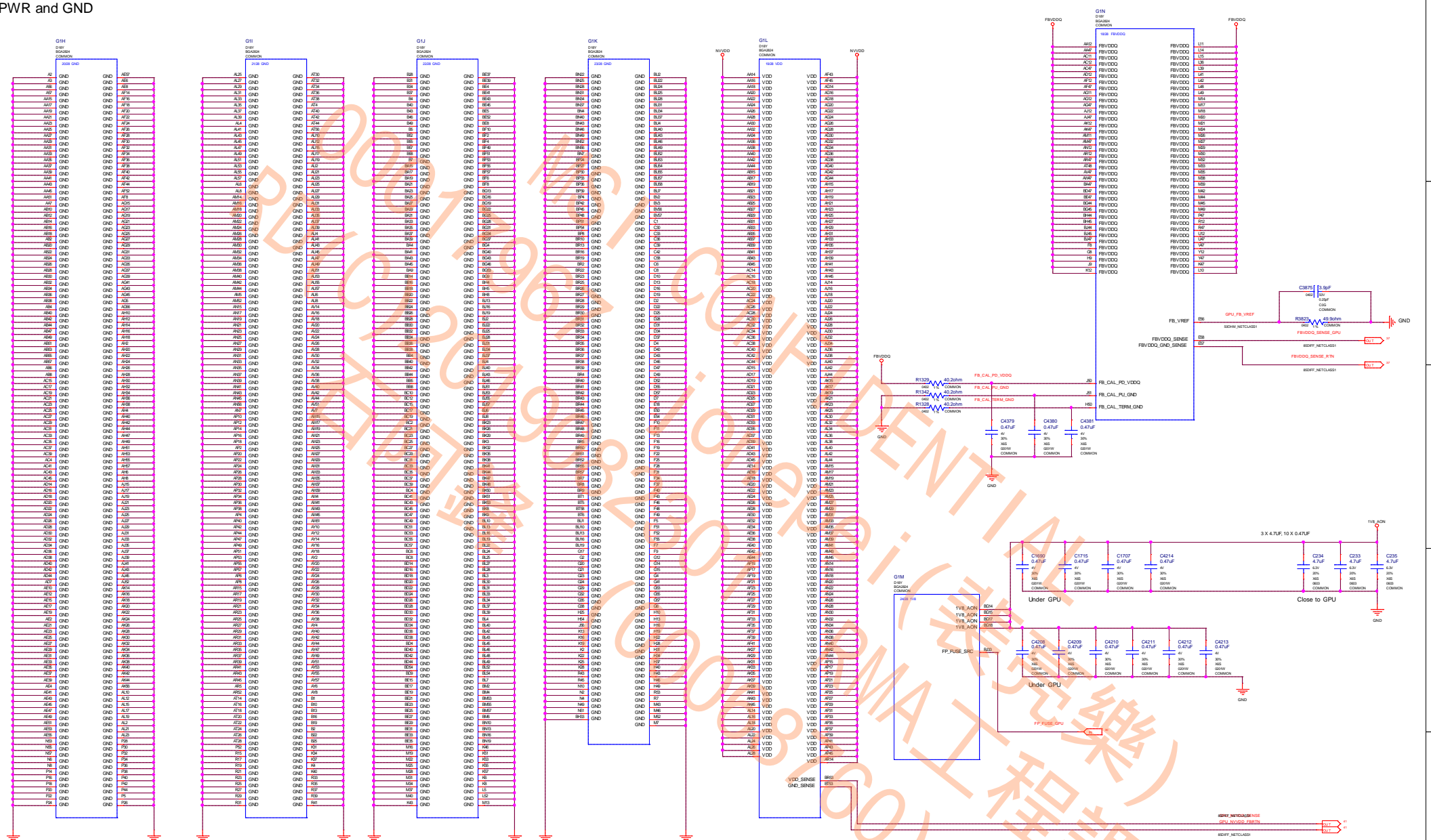






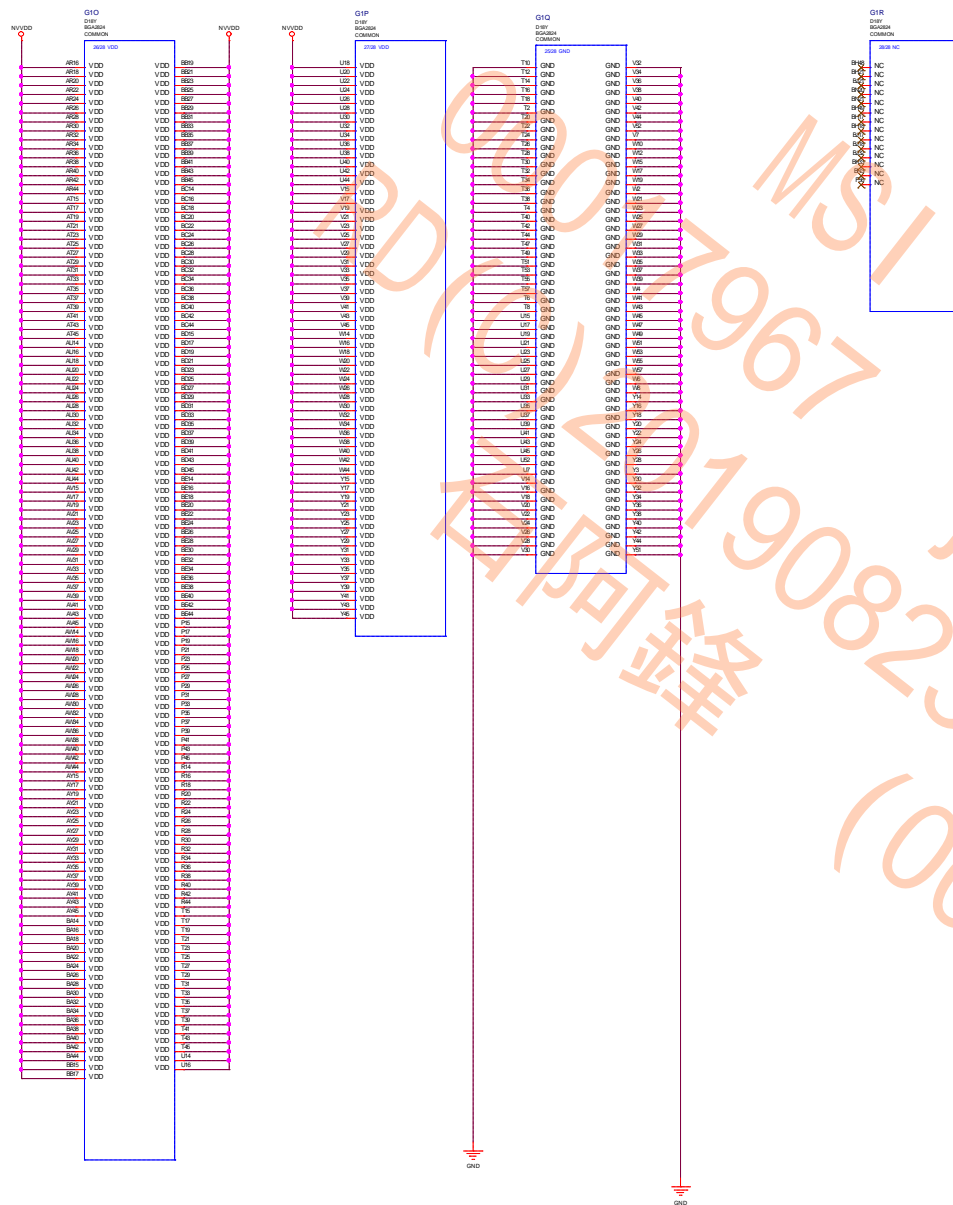


## GPU PWR and GND

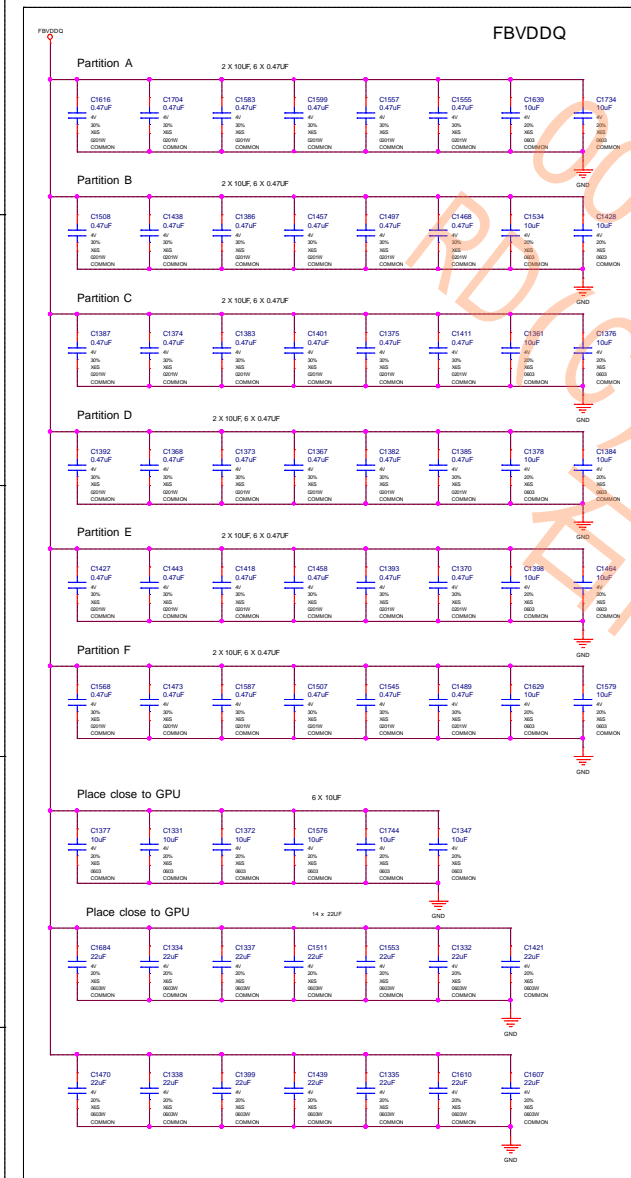




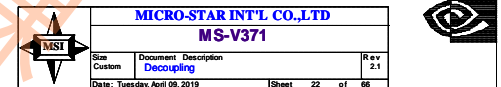
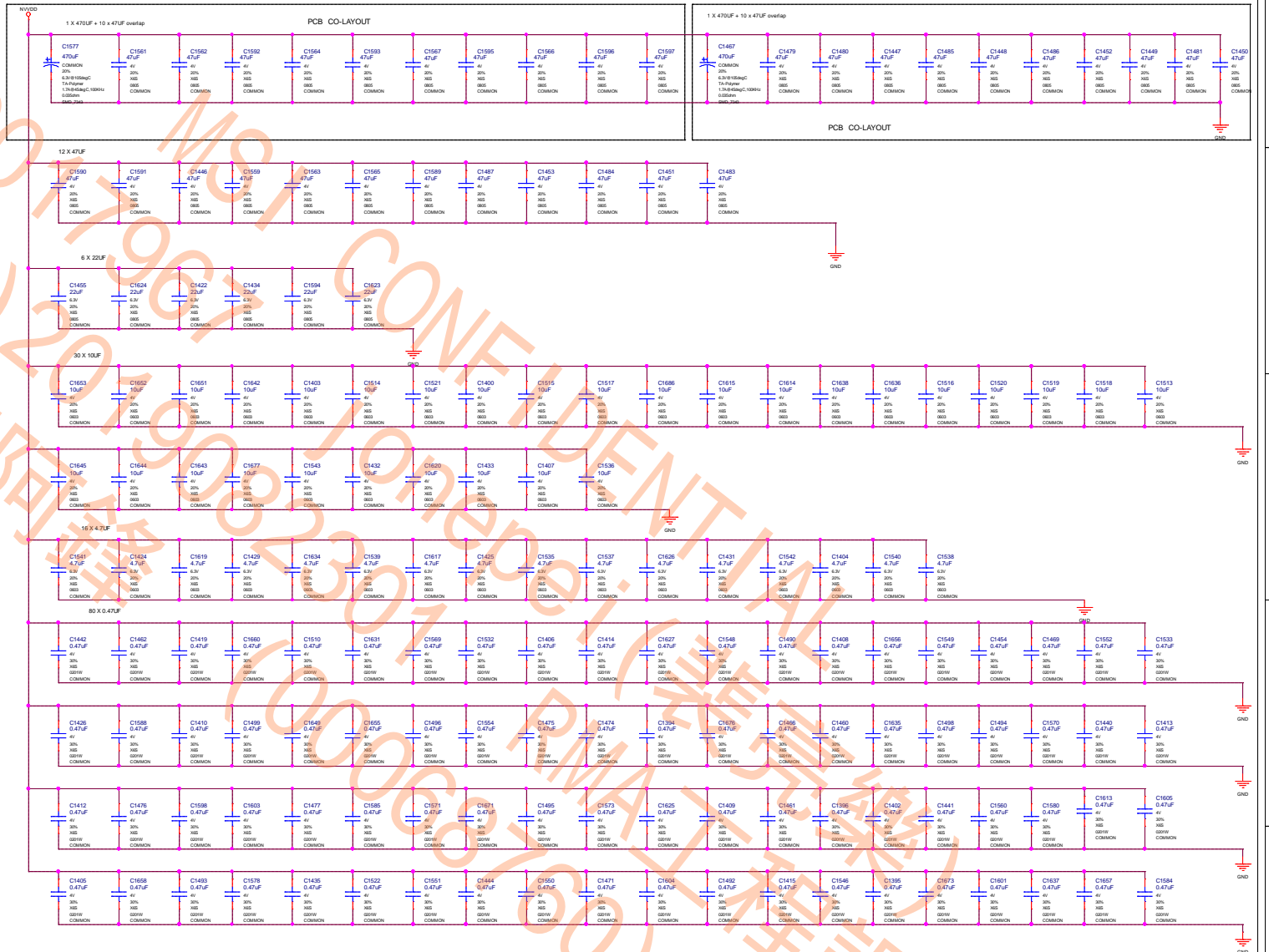
## GPU PWR GND NCs



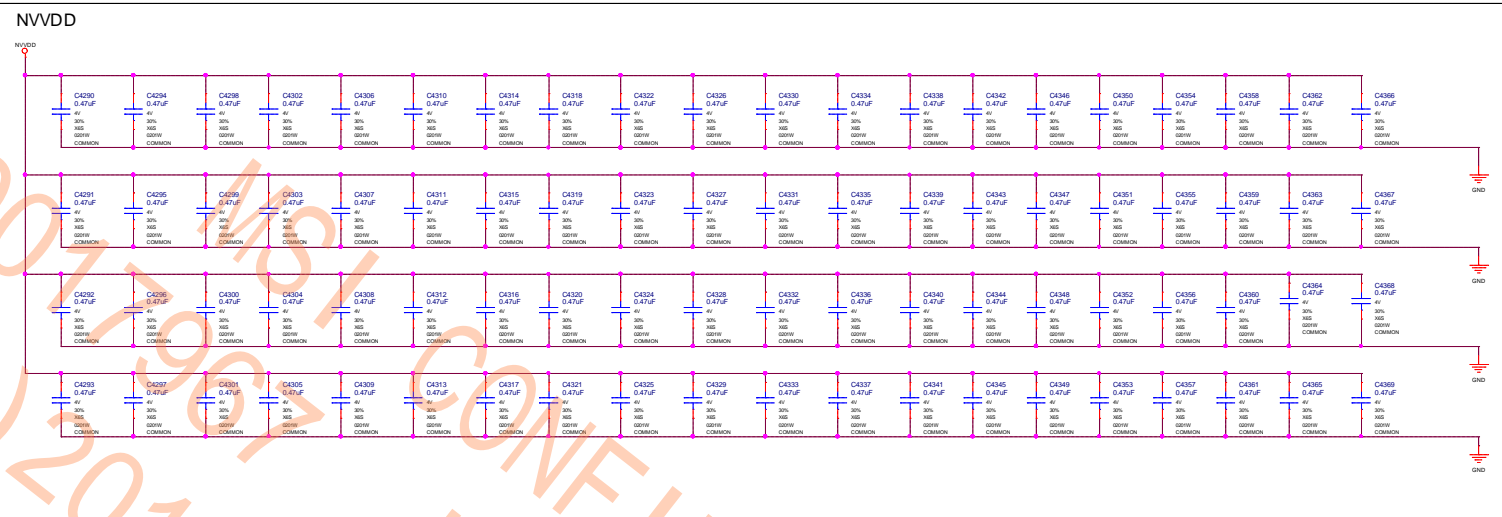
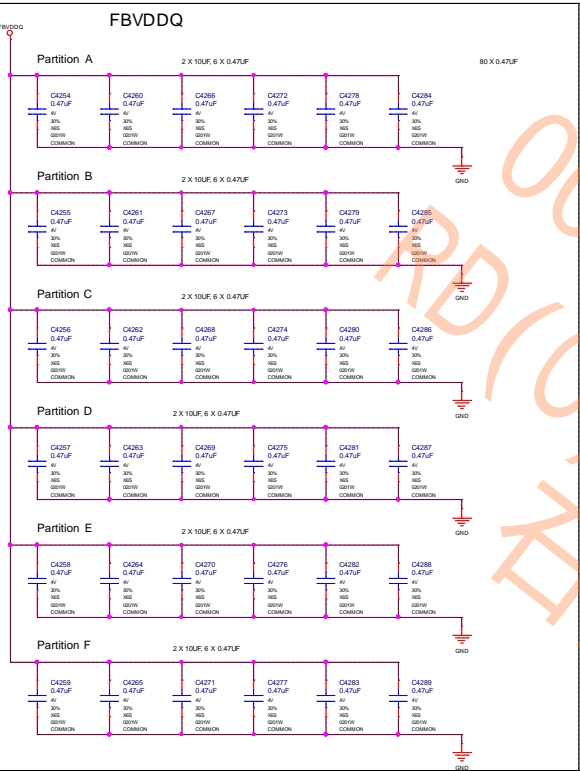
## GPU Decoupling



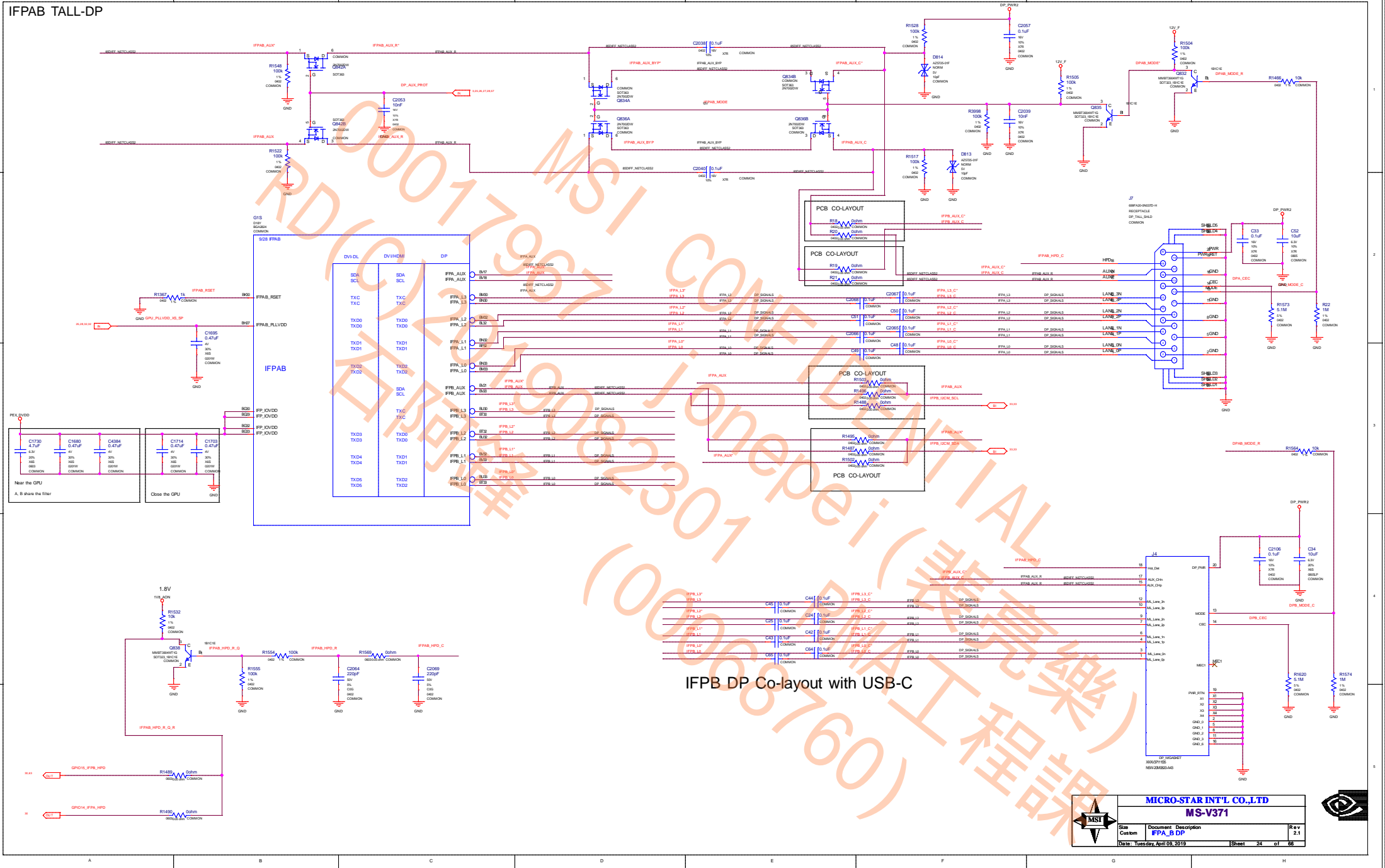
## NVVDD



GPU Decoupling



## IFPAB TALL-DP





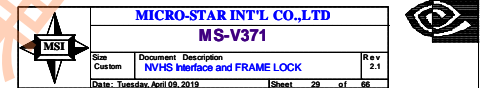
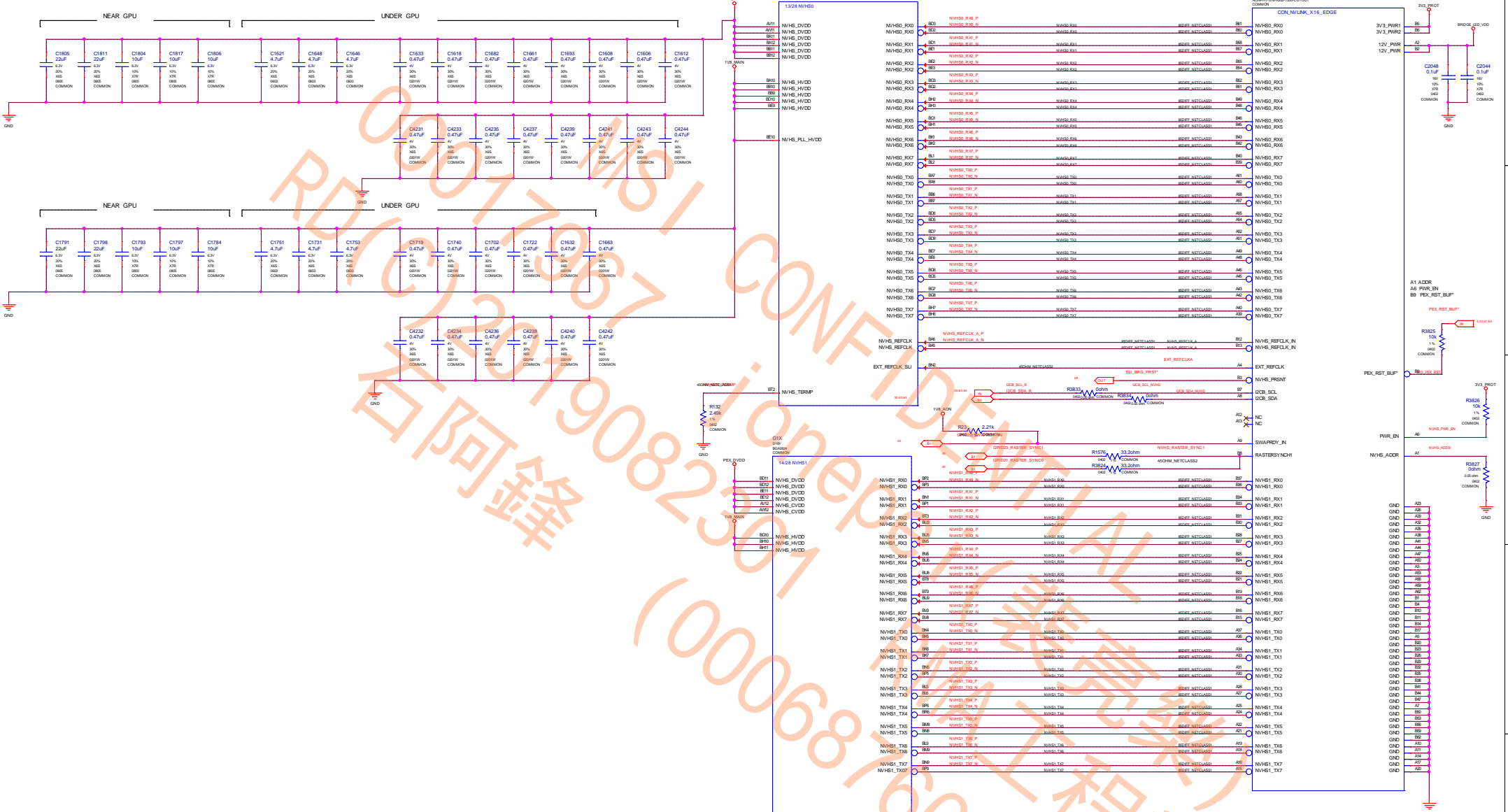




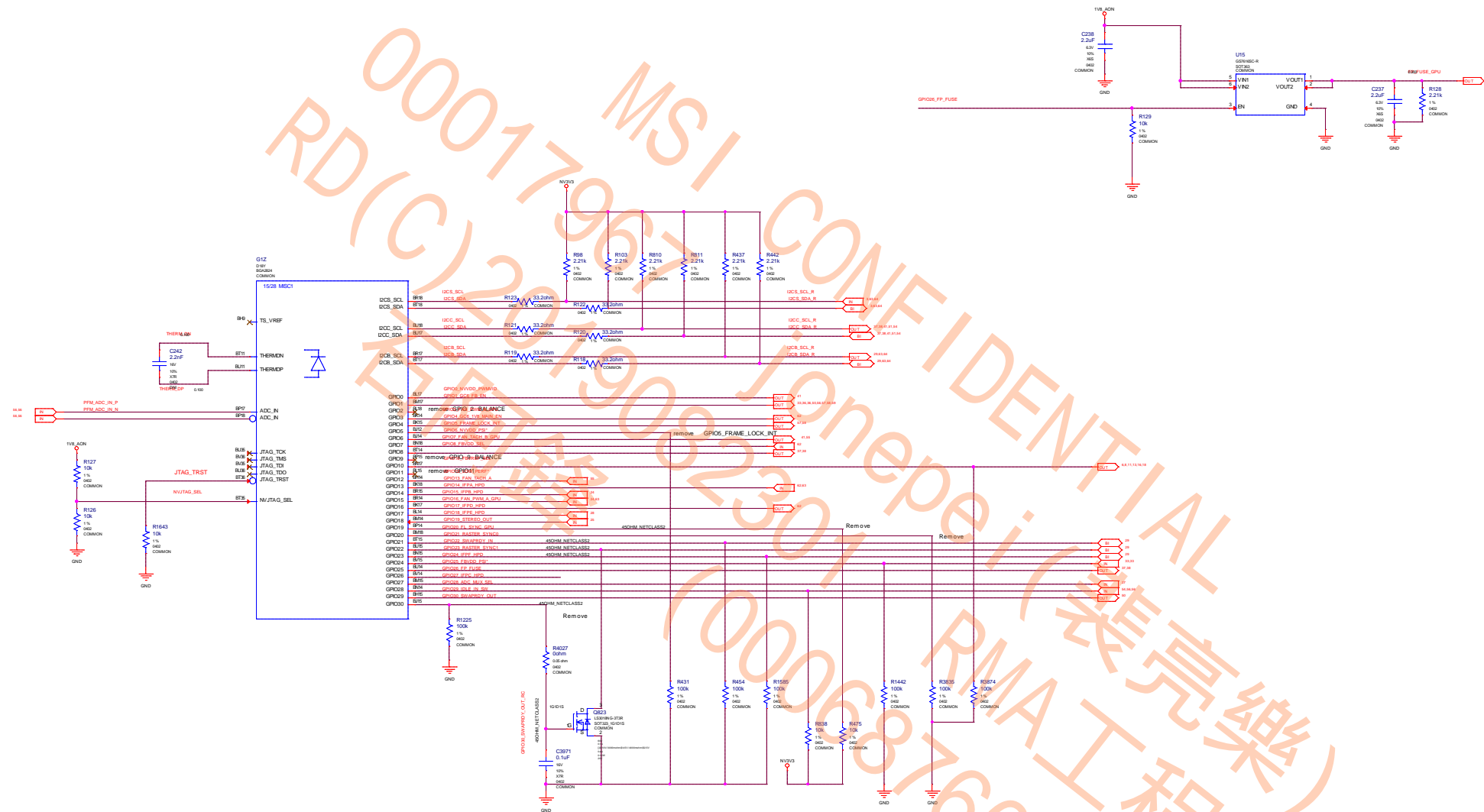




## NVHS Interface and FRAME LOCK



## MISC1: Fan, Thermal, JTAG, GPIO, STEREO



MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	DEFAULT
L	L	H	00001	
L	H	L	00010	
L	H	H	00011	
H	L	L	00100	
H	L	H	00101	
H	H	L	00110	
H	H	H	00111	
L	L	M	01000	
L	M	L	01001	

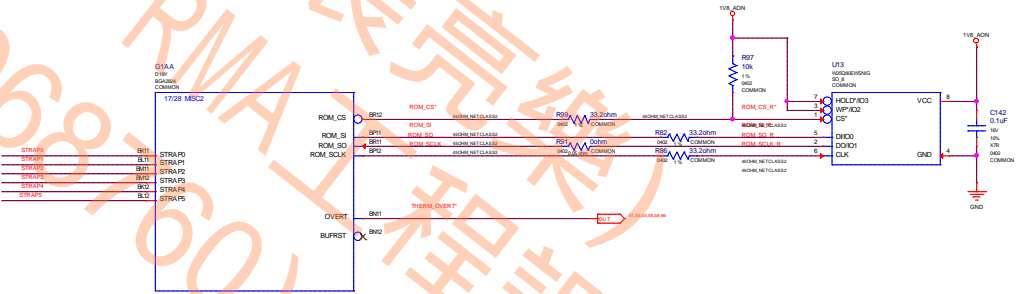
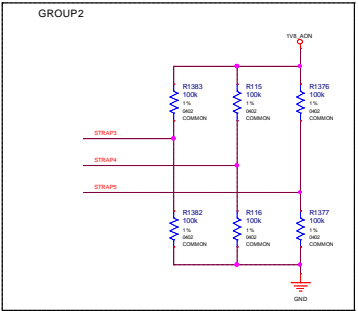
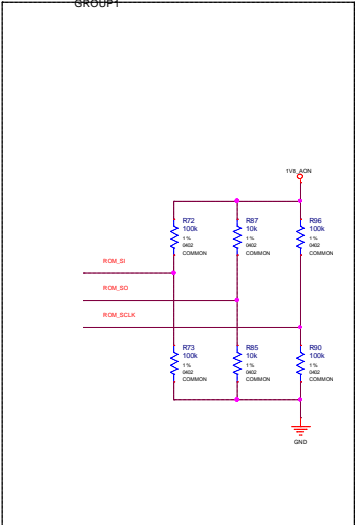
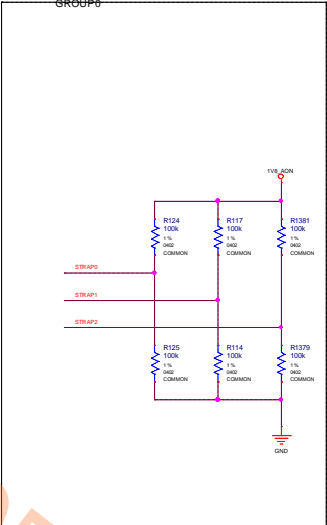
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	H	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	

Default:  
SKU 200

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

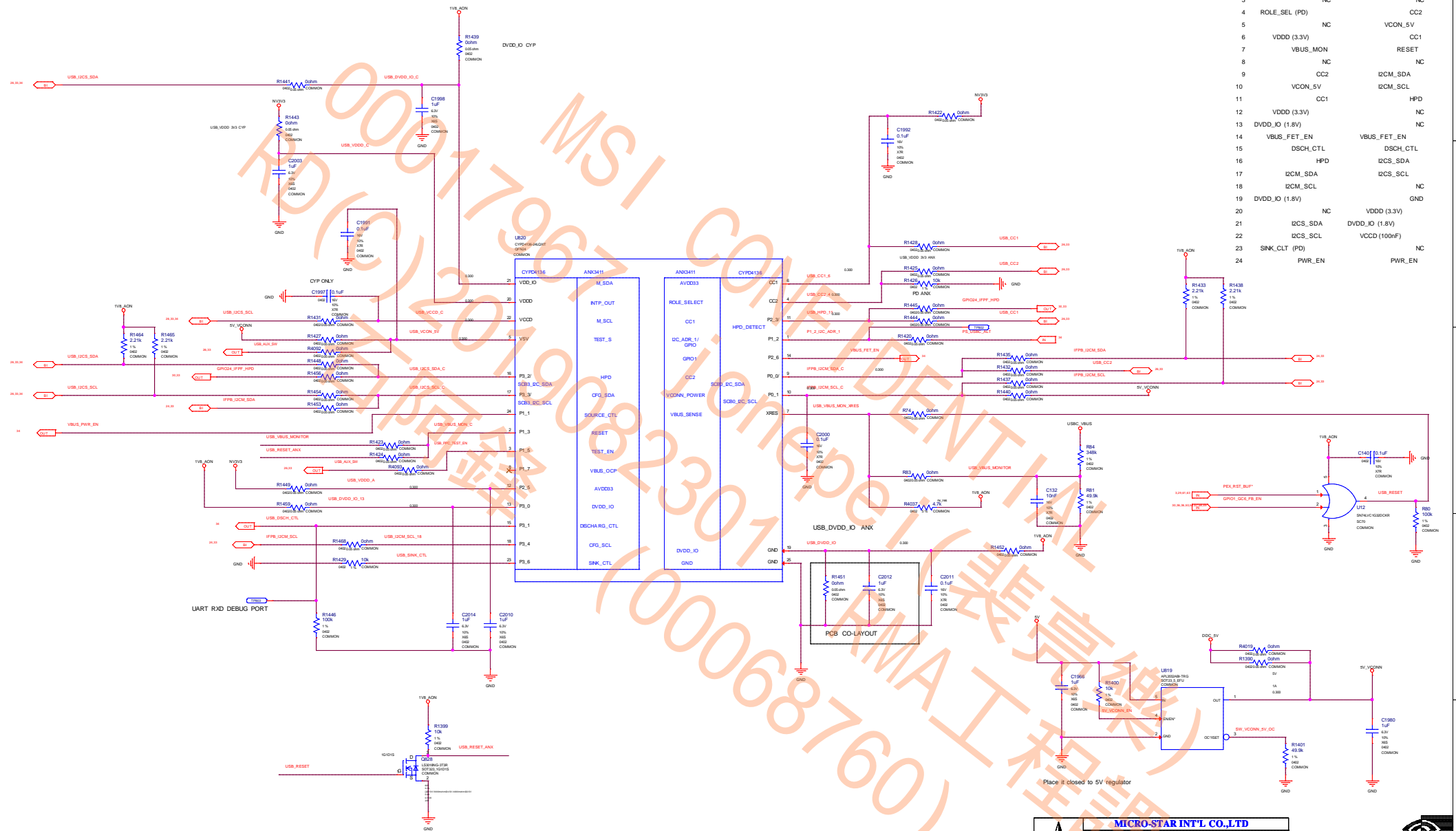
1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE







## MISC: USB PPC

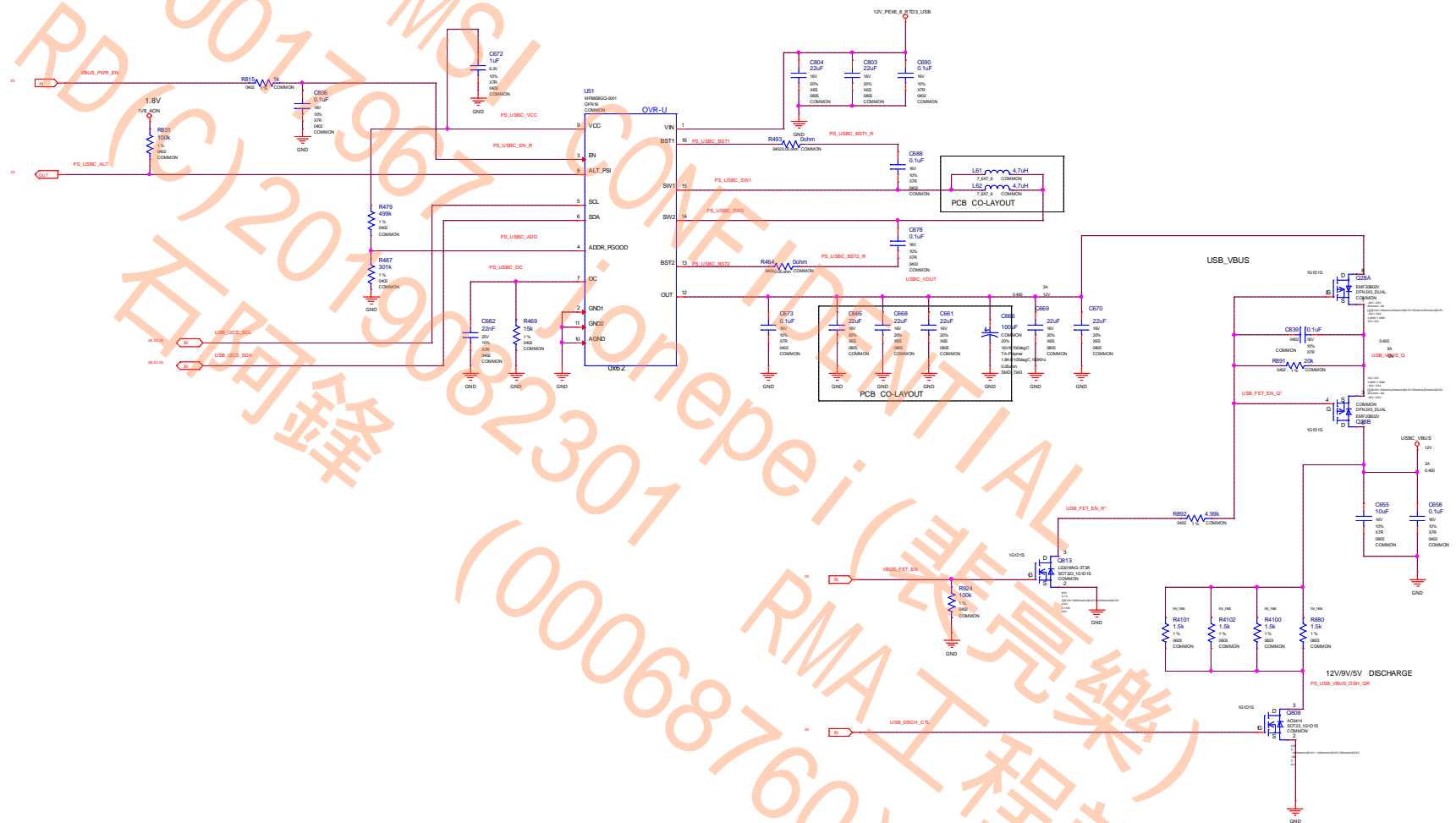


PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCDD (100mF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN

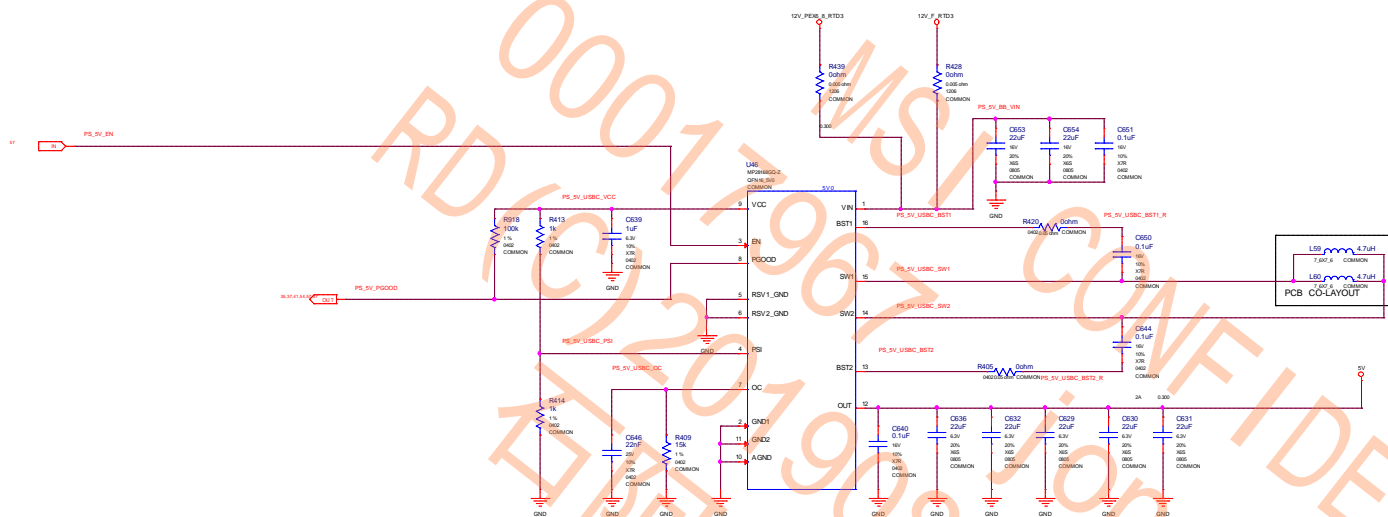


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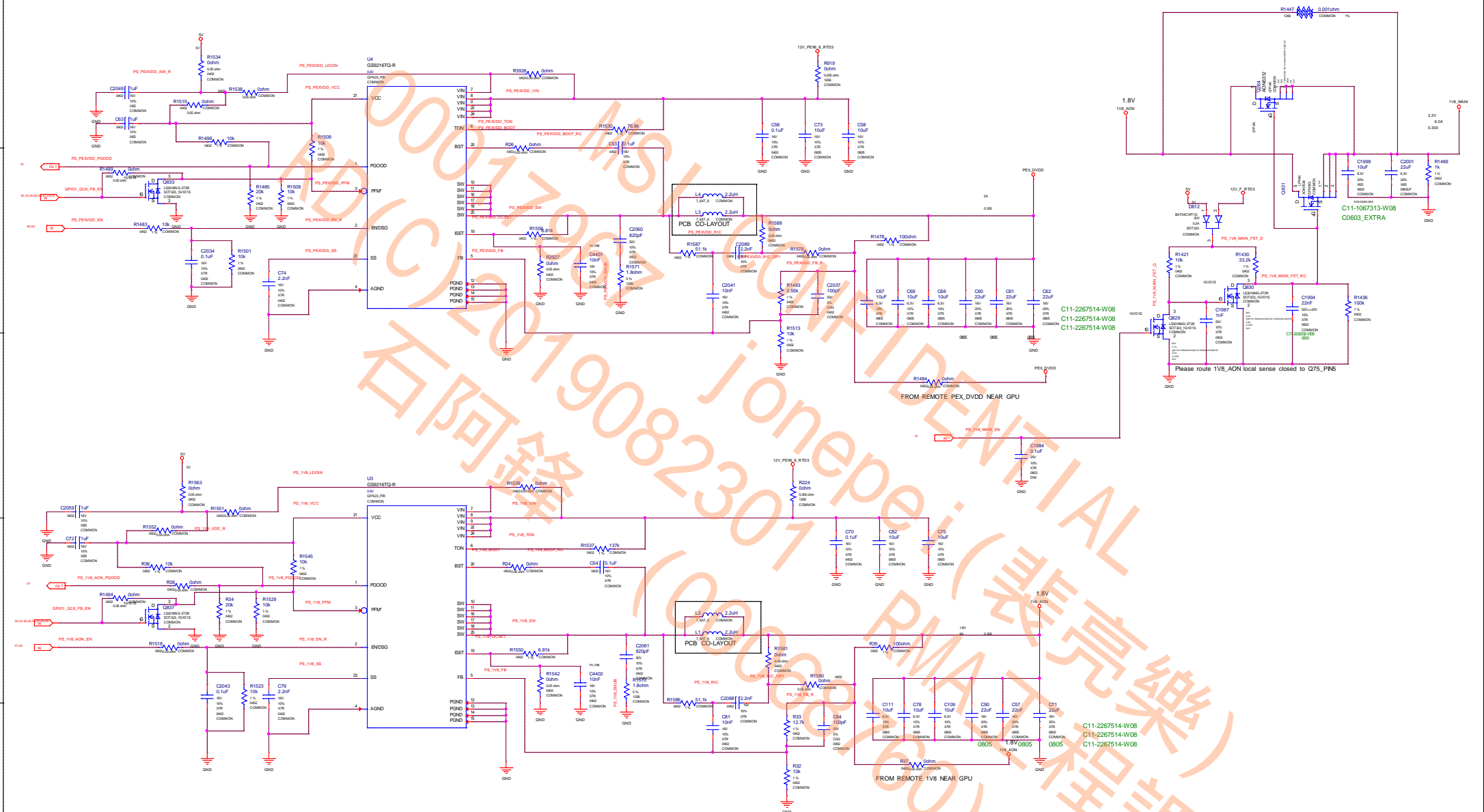
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PS: 5V, 5V\_BACKUP



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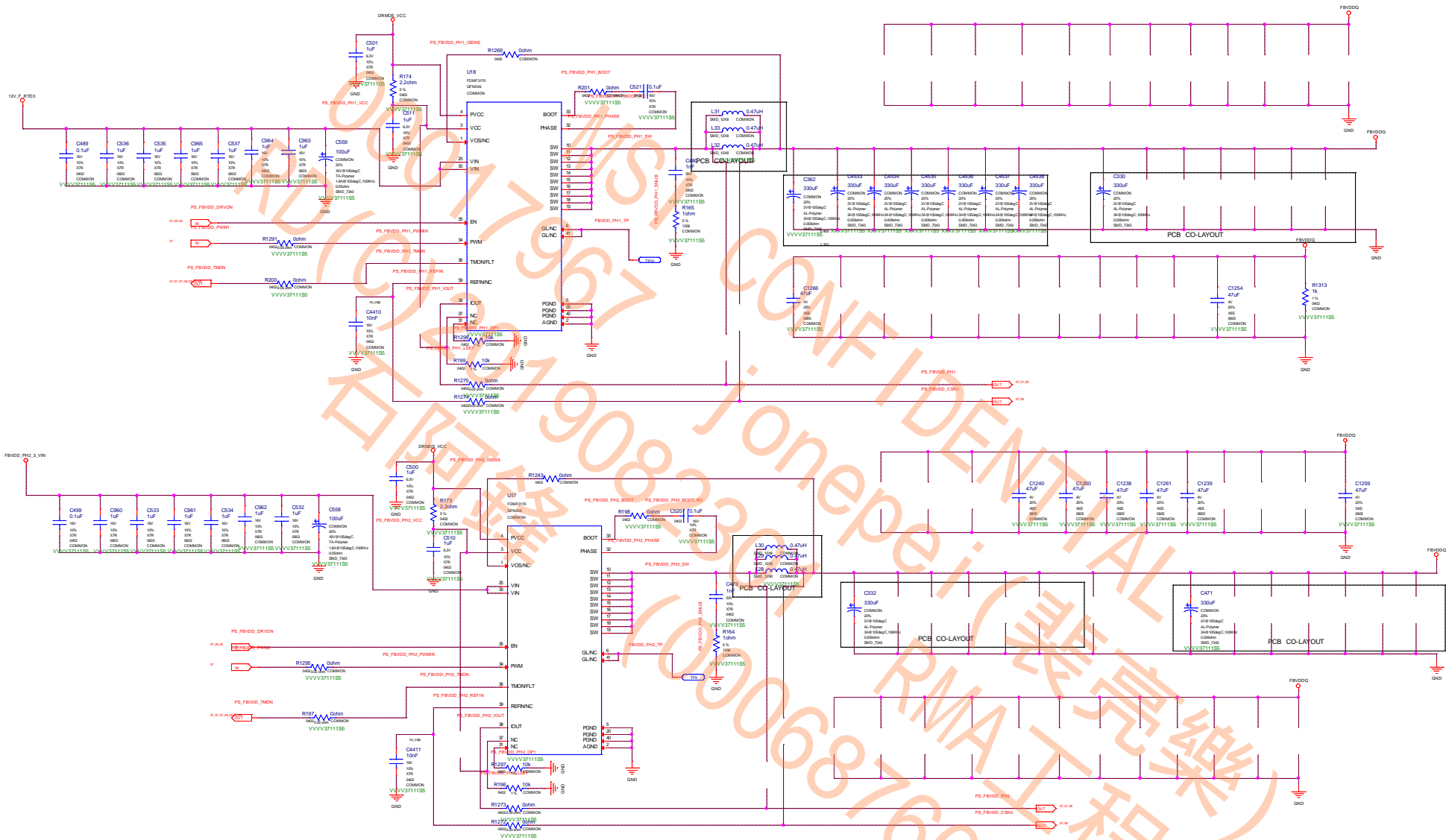
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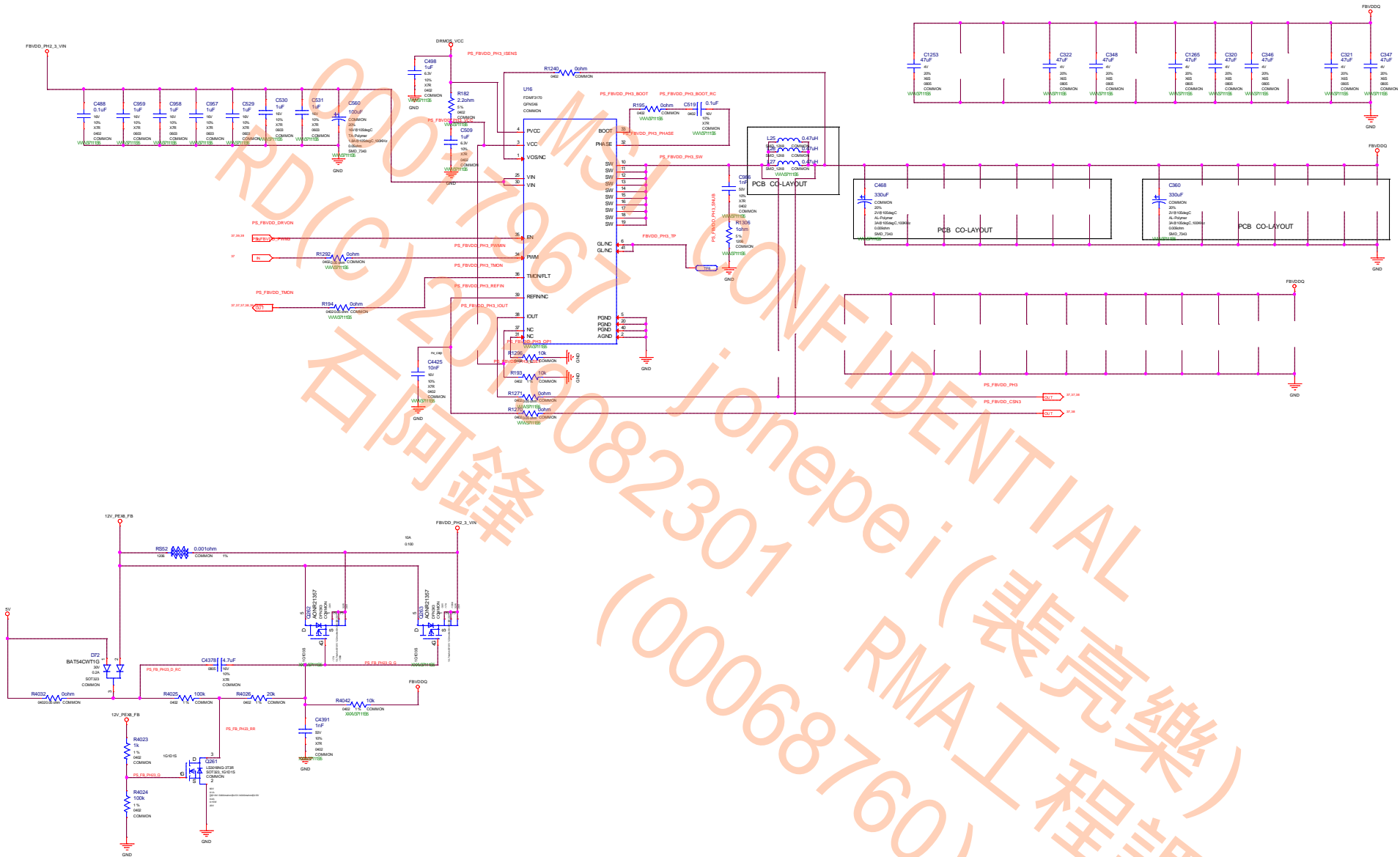
MSI CONFIDENTIAL  
00017967 jonepei (裴亮樂)  
RD(C)2019082301 RMA工程課  
石阿鋒 (00068760)

remove FBVDDQ

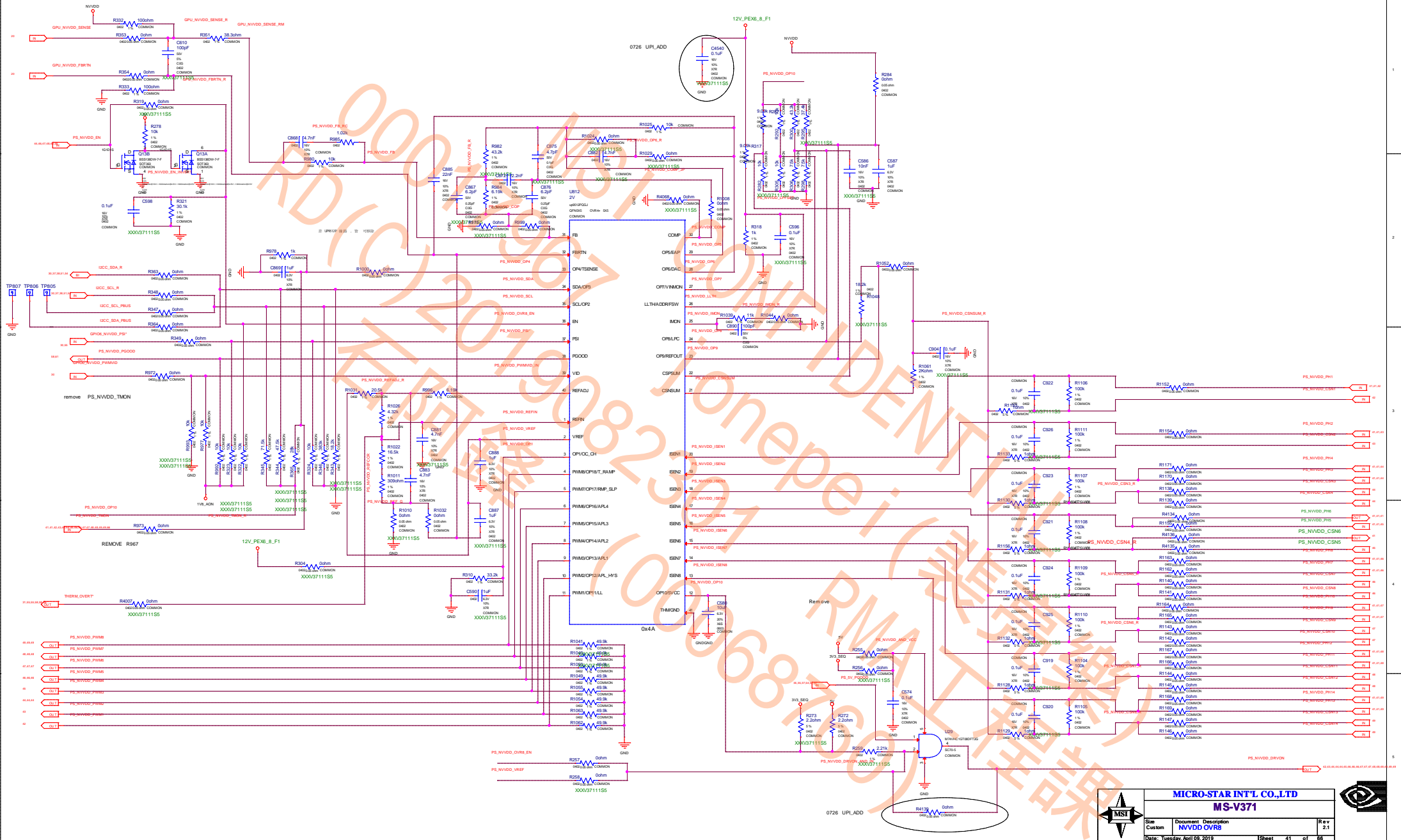
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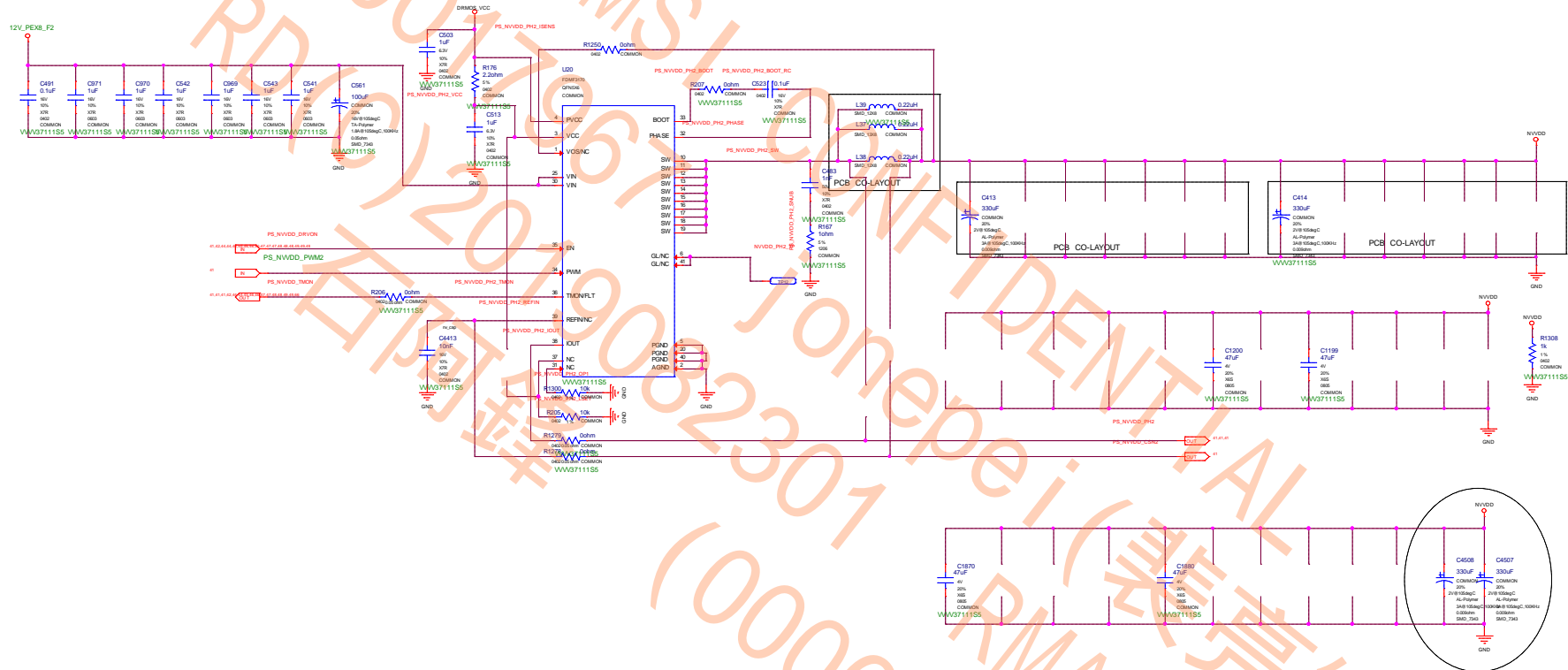


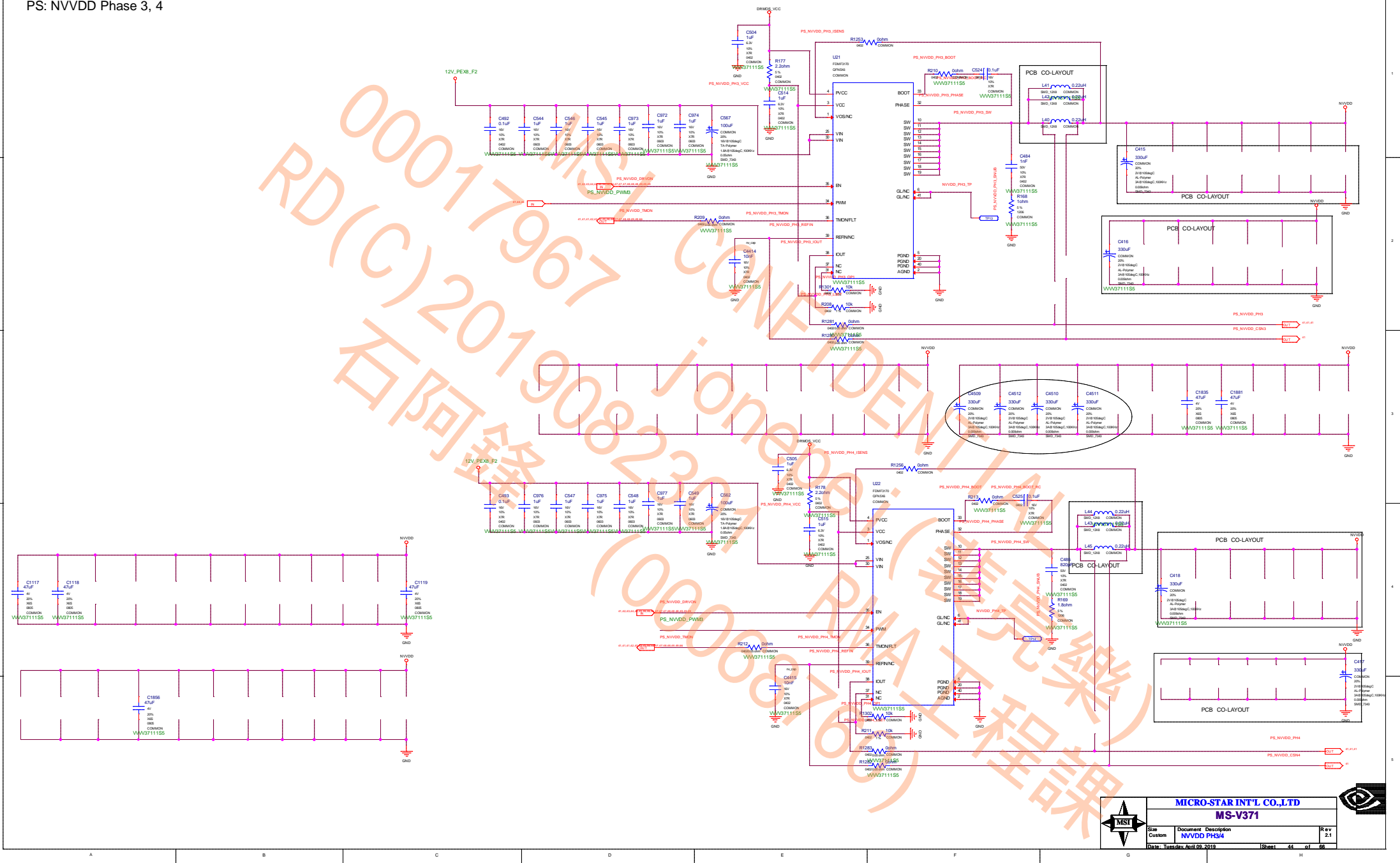


## PS: NVVDD Controller\_OVR8

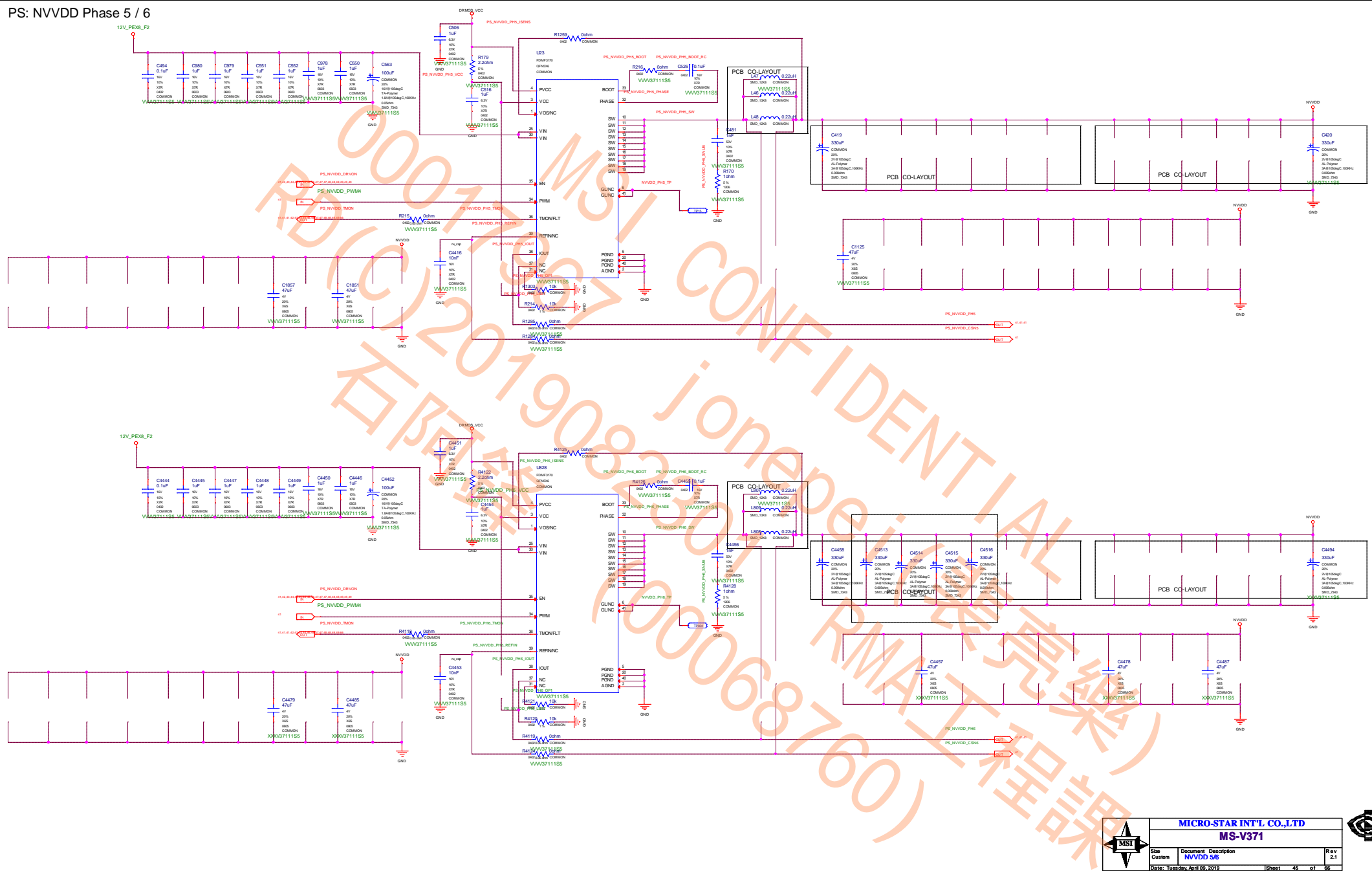


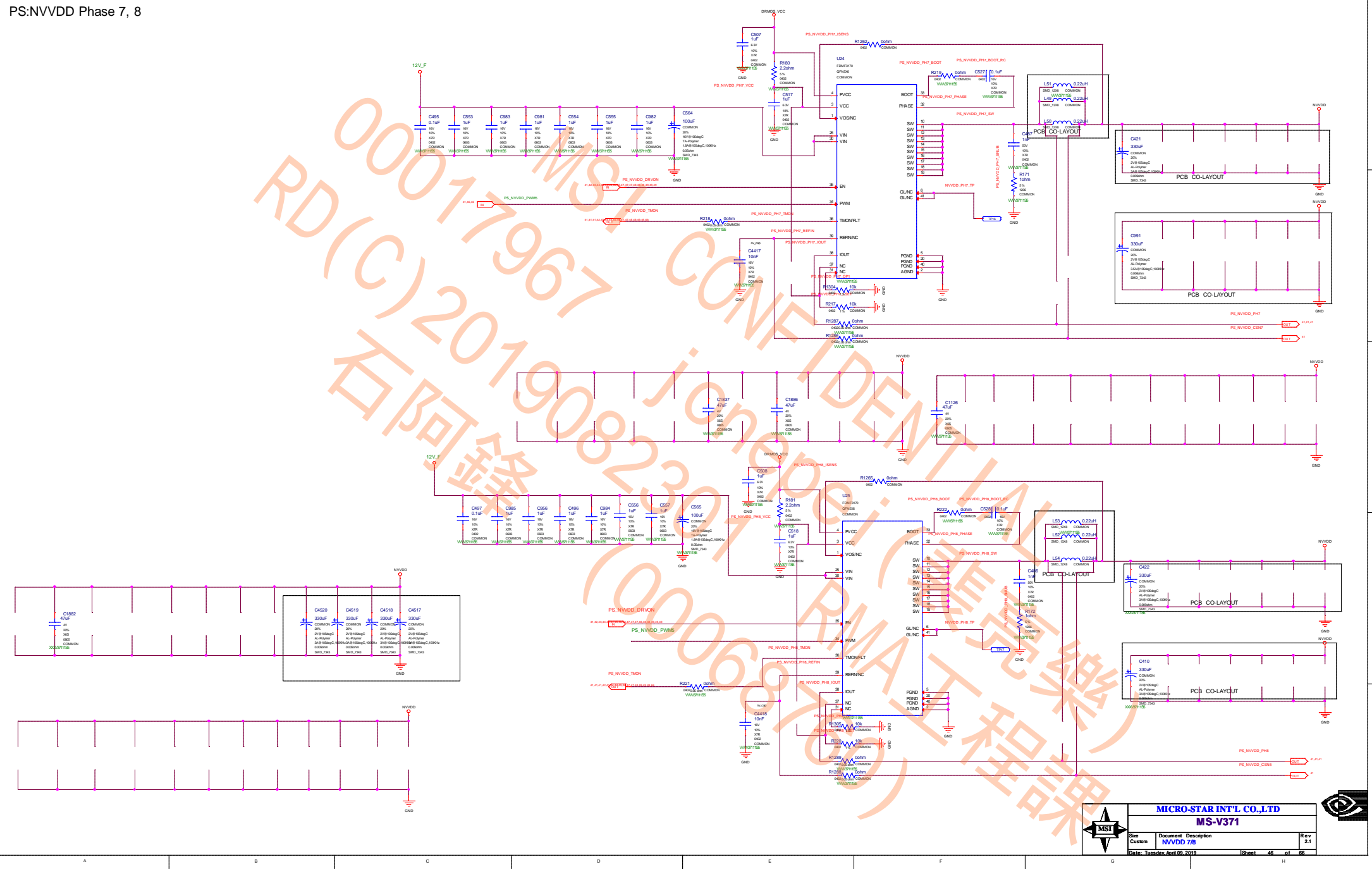






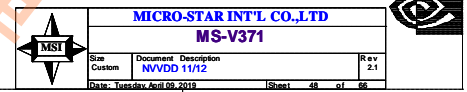


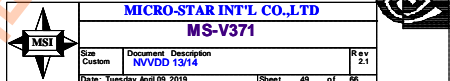






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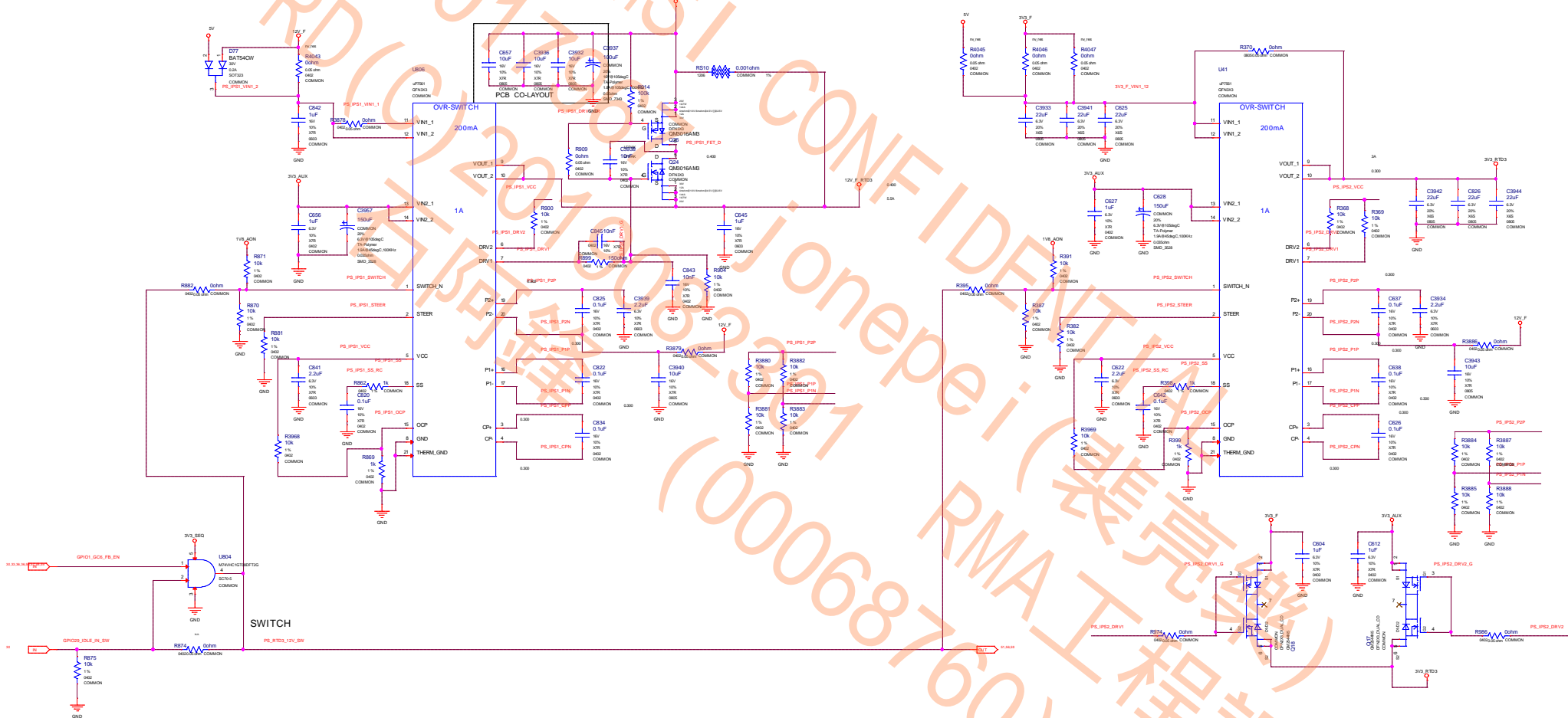
PS: INPUT SWITCH RTD3


AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A





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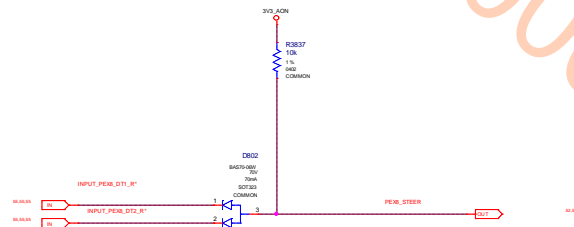
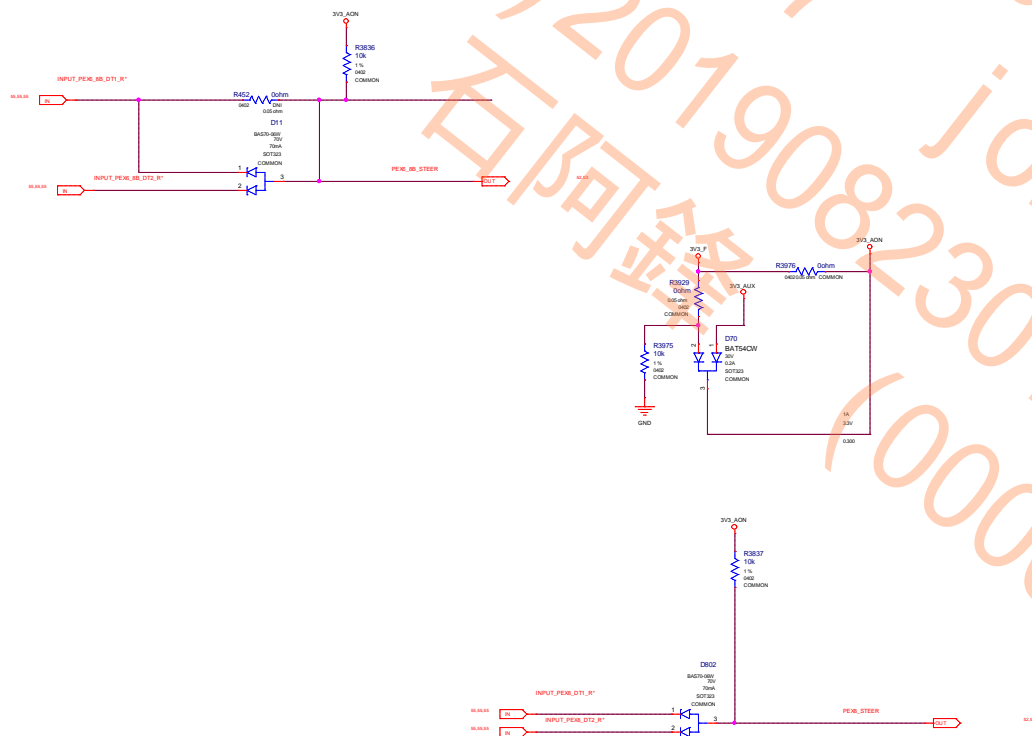
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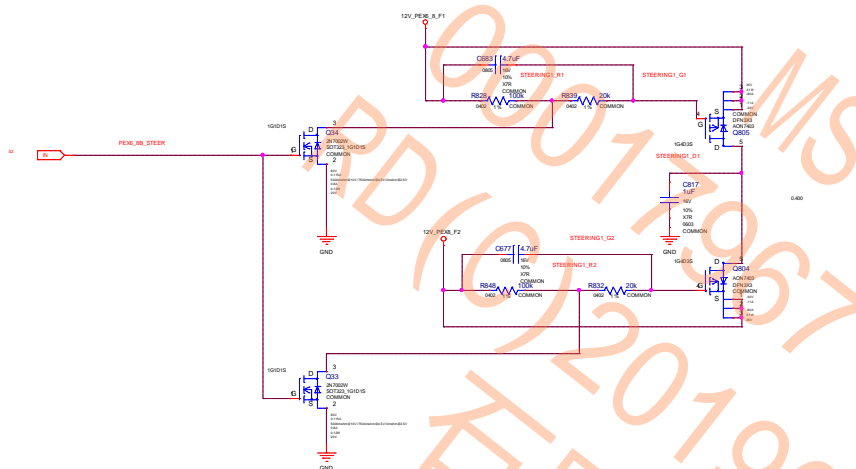






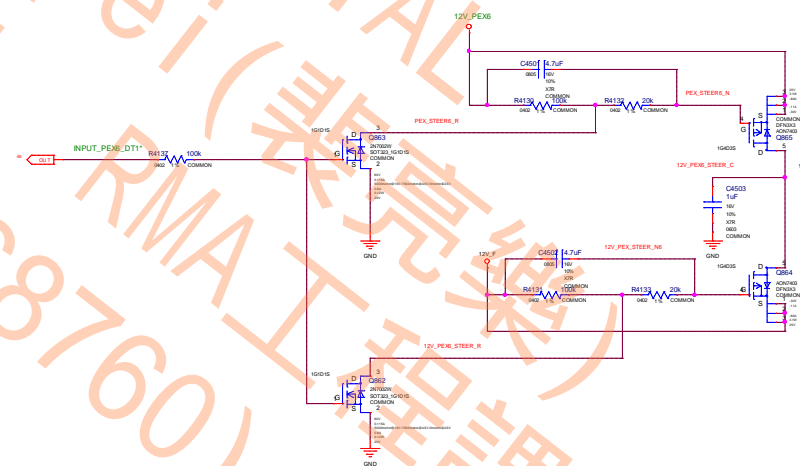
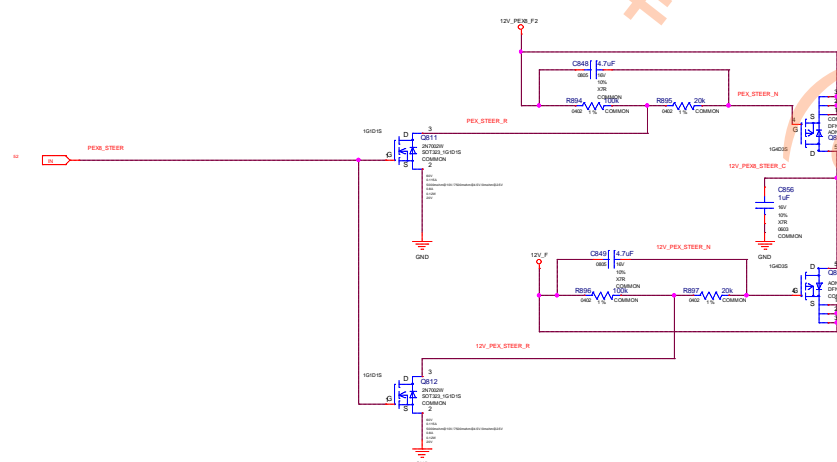


GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



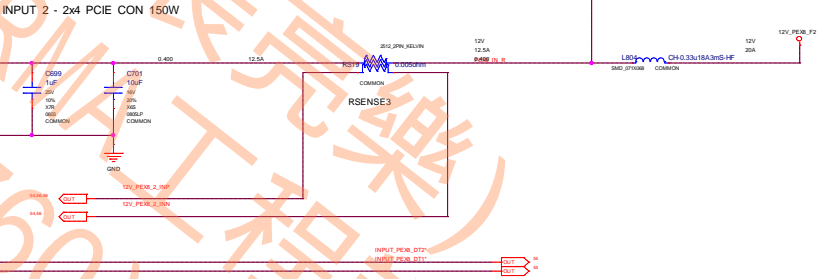
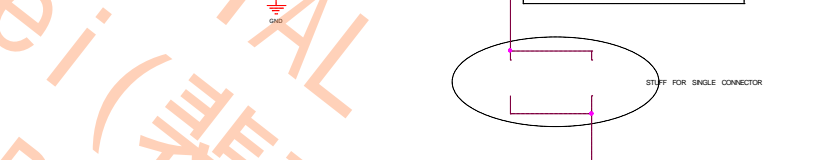
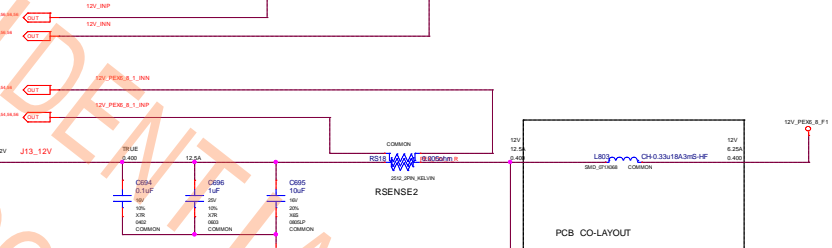
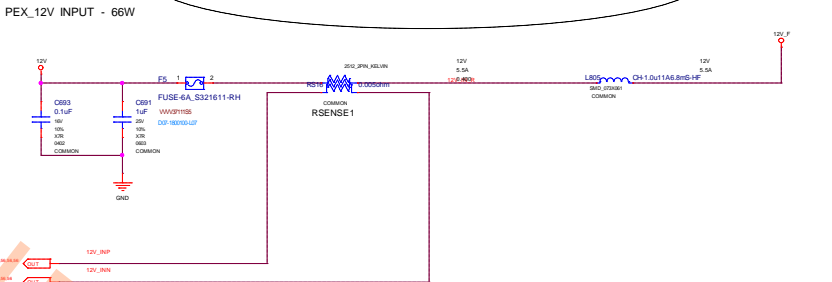
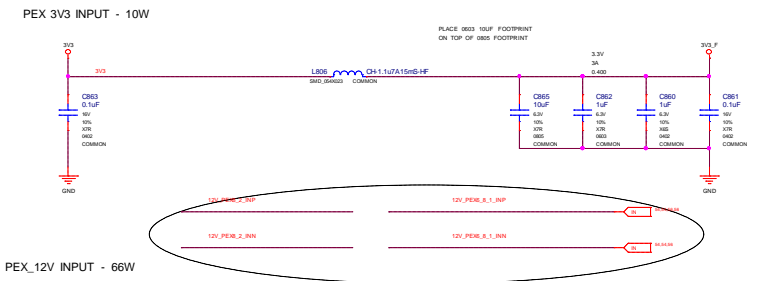
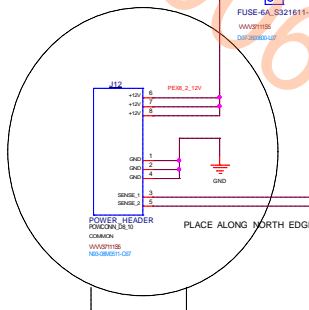
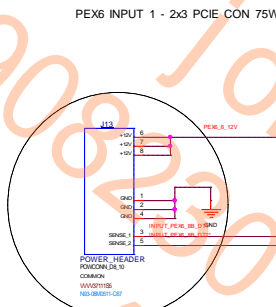
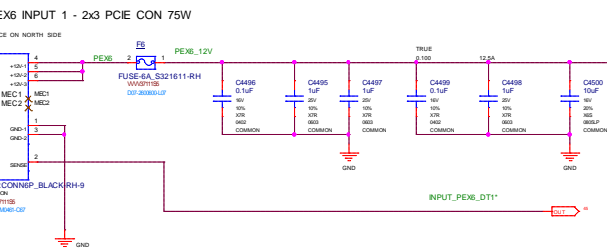
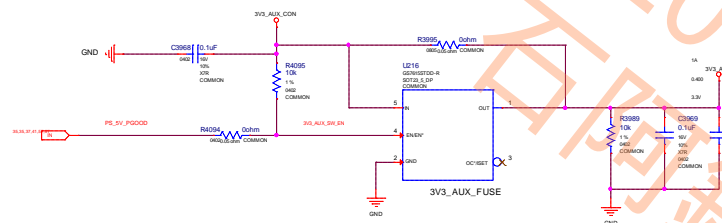
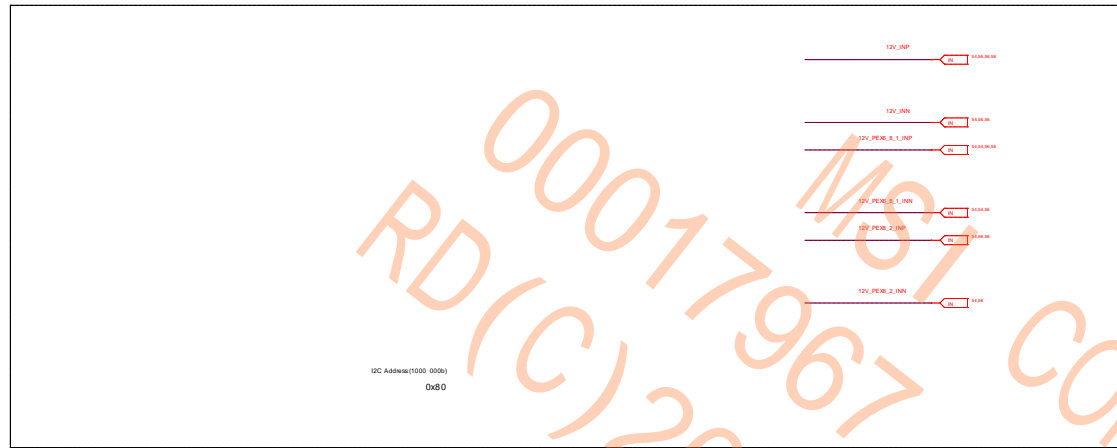
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode

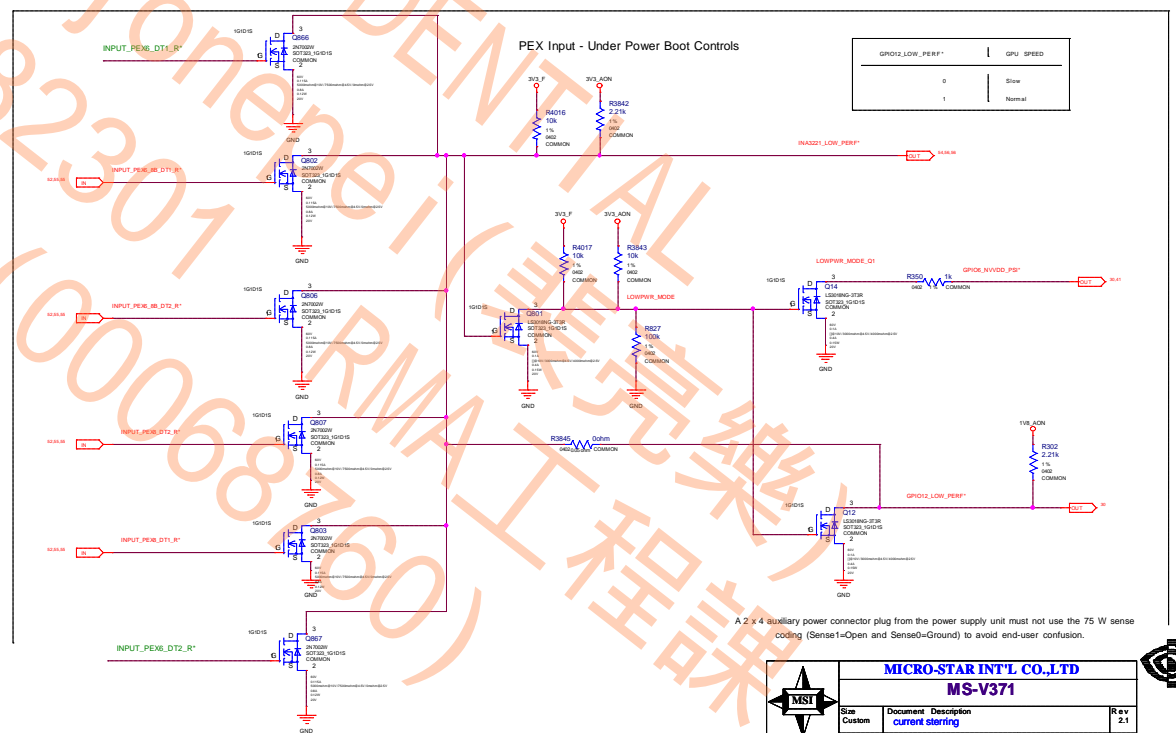
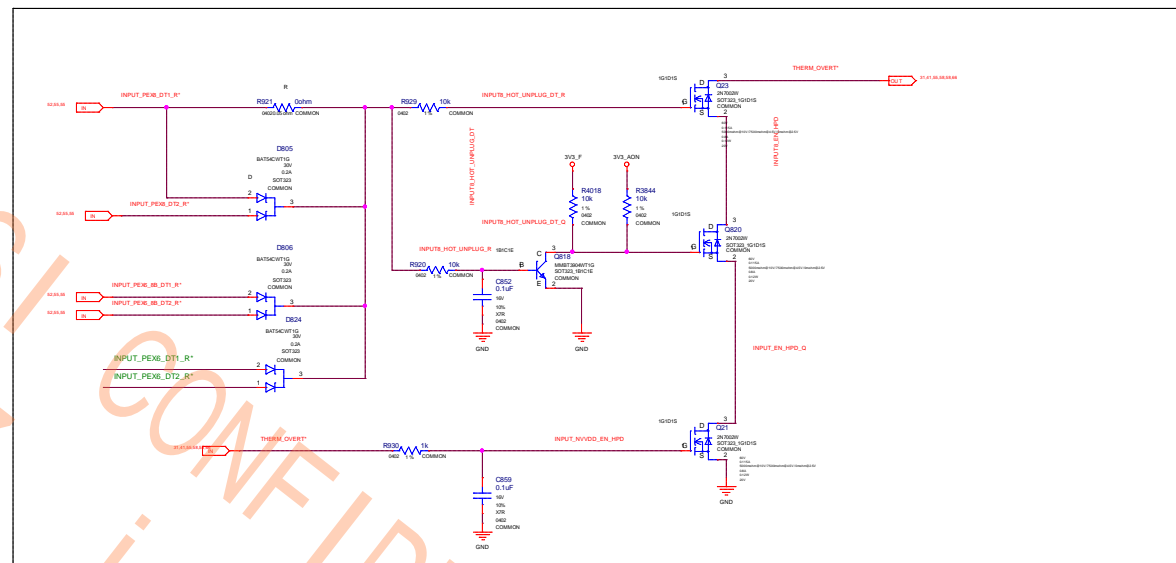
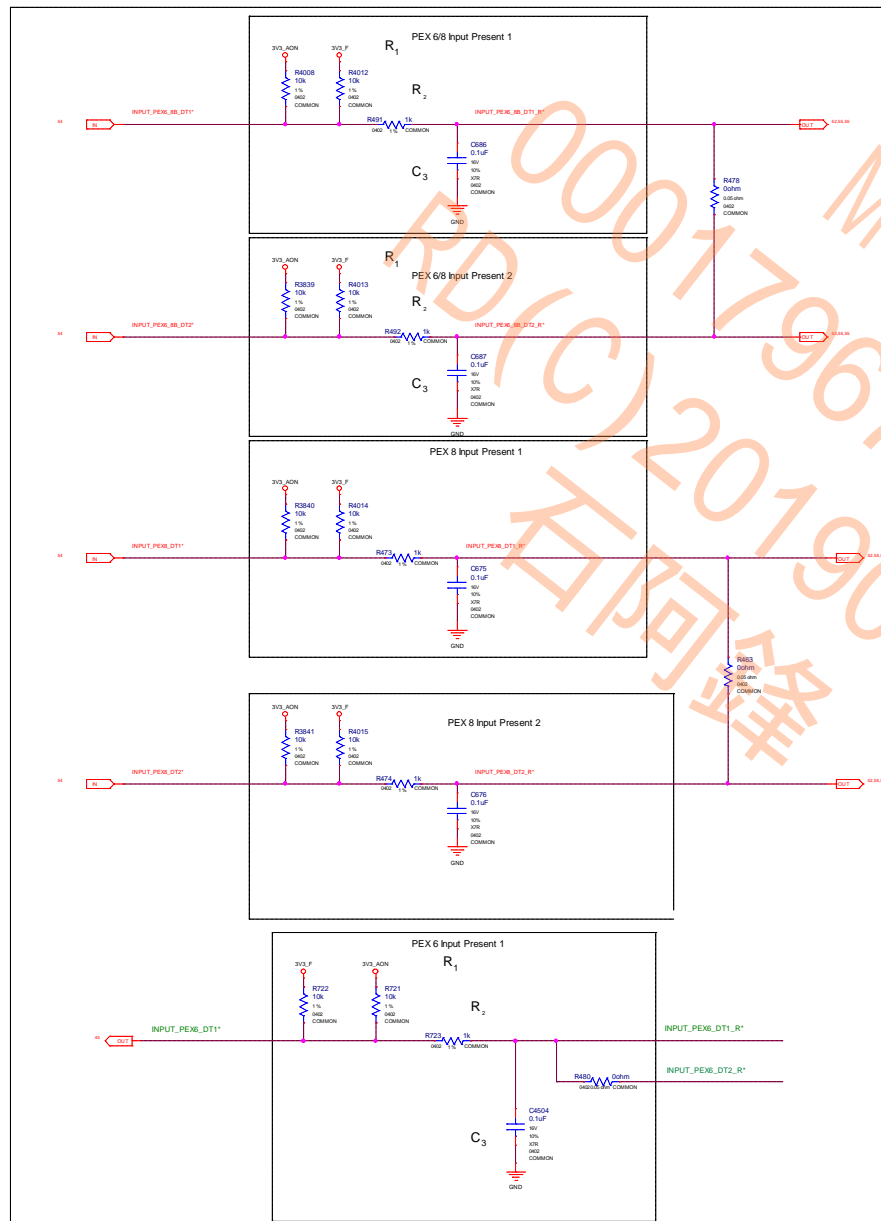


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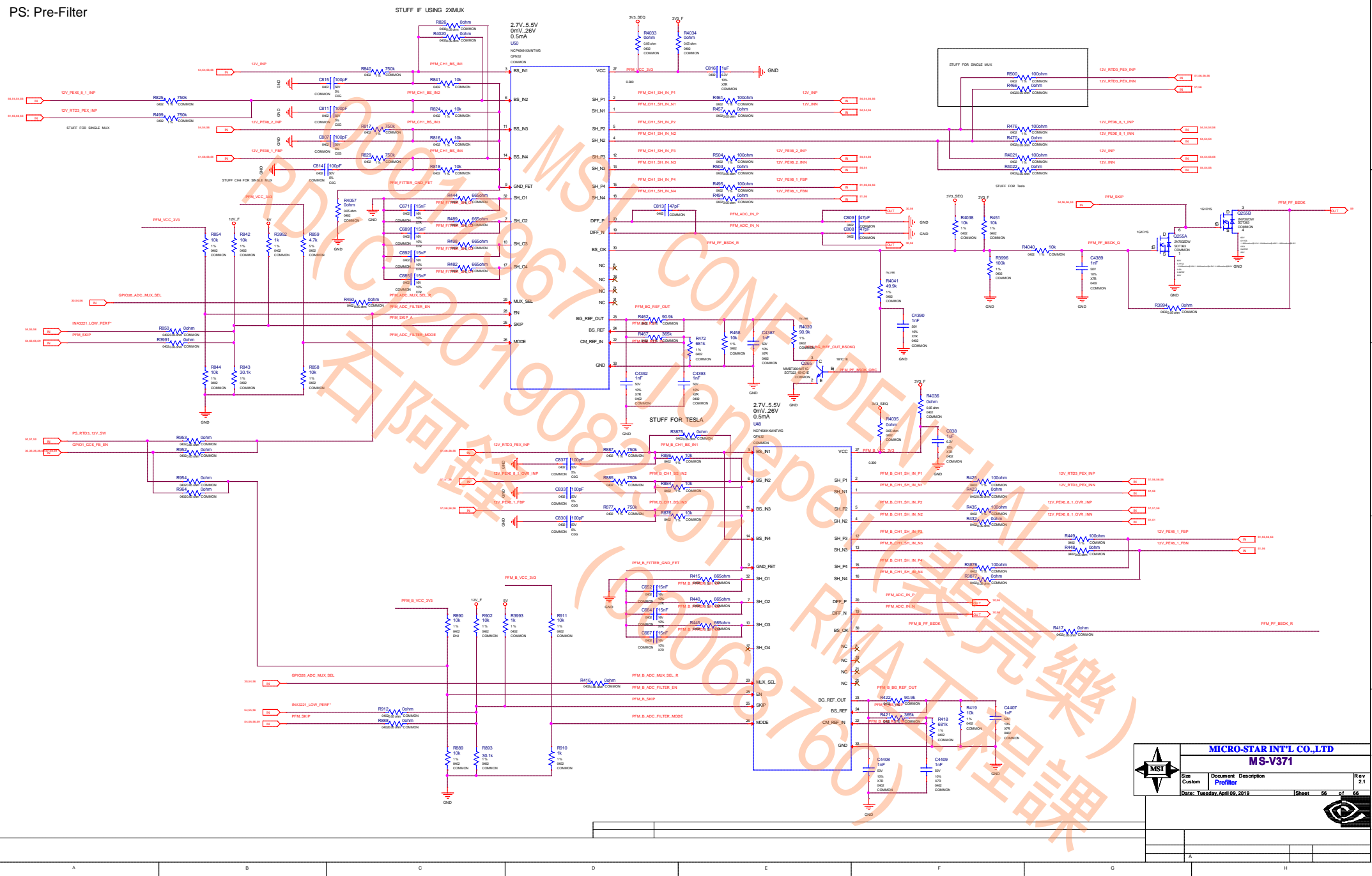
Size	Document Description	Re
Custom	steering	2



## PS: 12V Current Steering &amp; Hot Unplug Detect

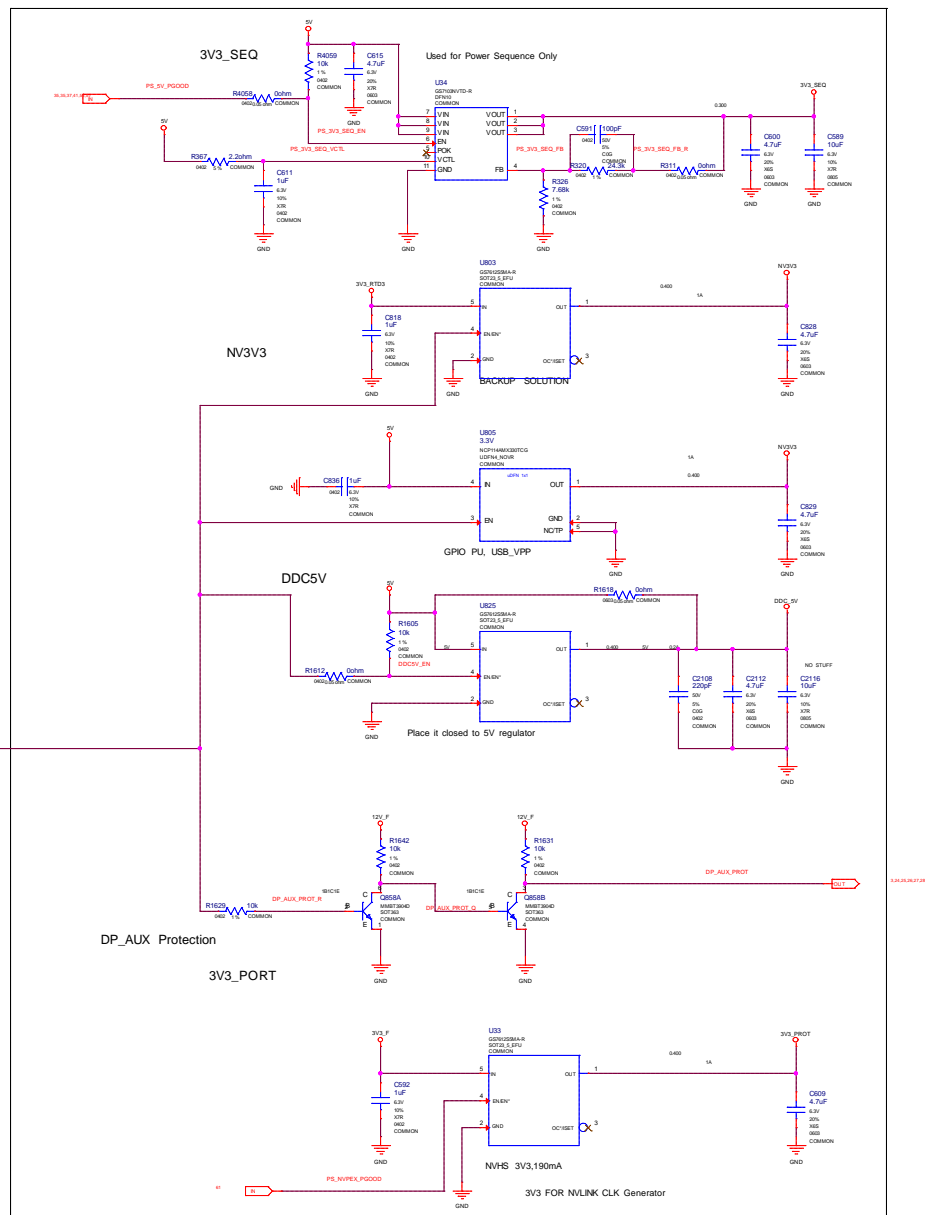
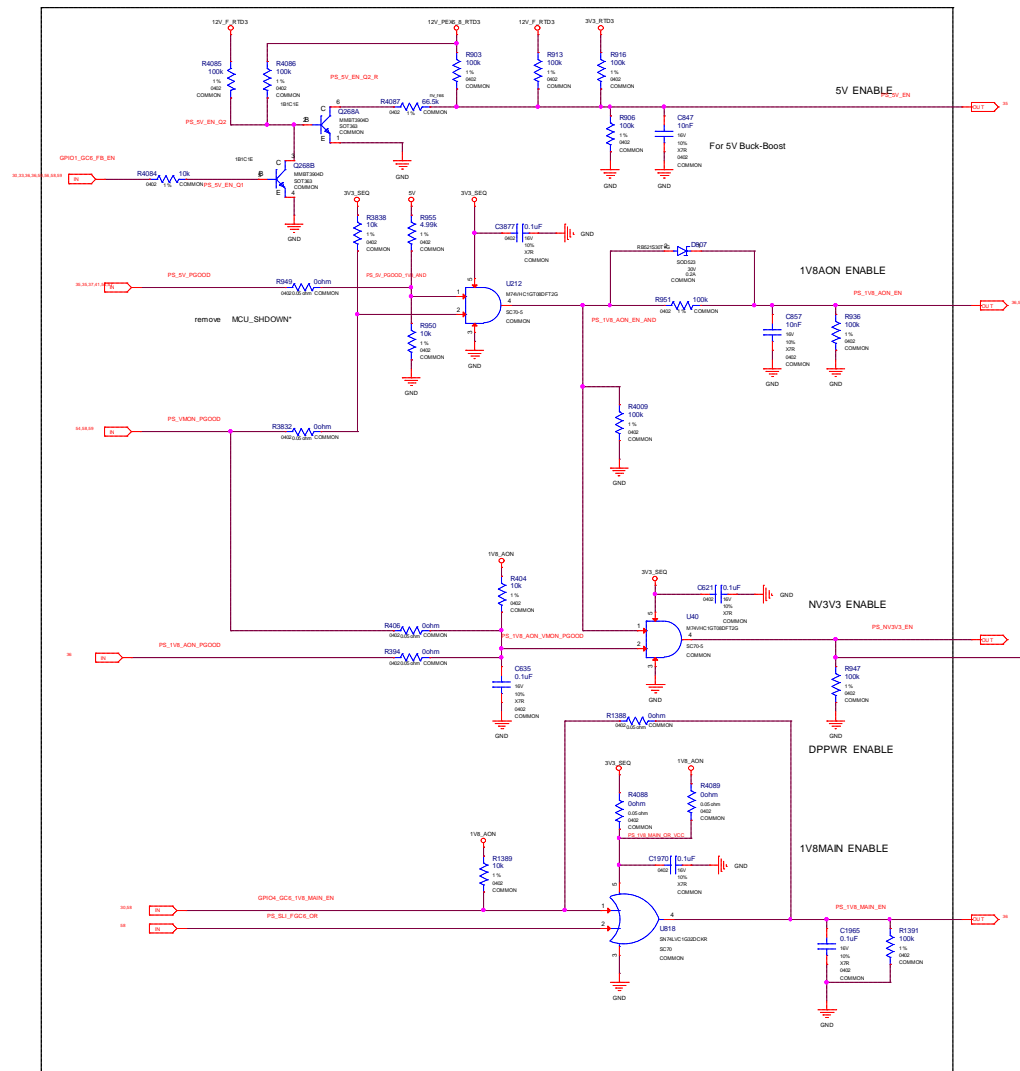


PS: Pre-Filter





SEQUENCE:5V,1V8,NV3V3 ENABLE



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ASSEMBLY  
PAGE DETAIL

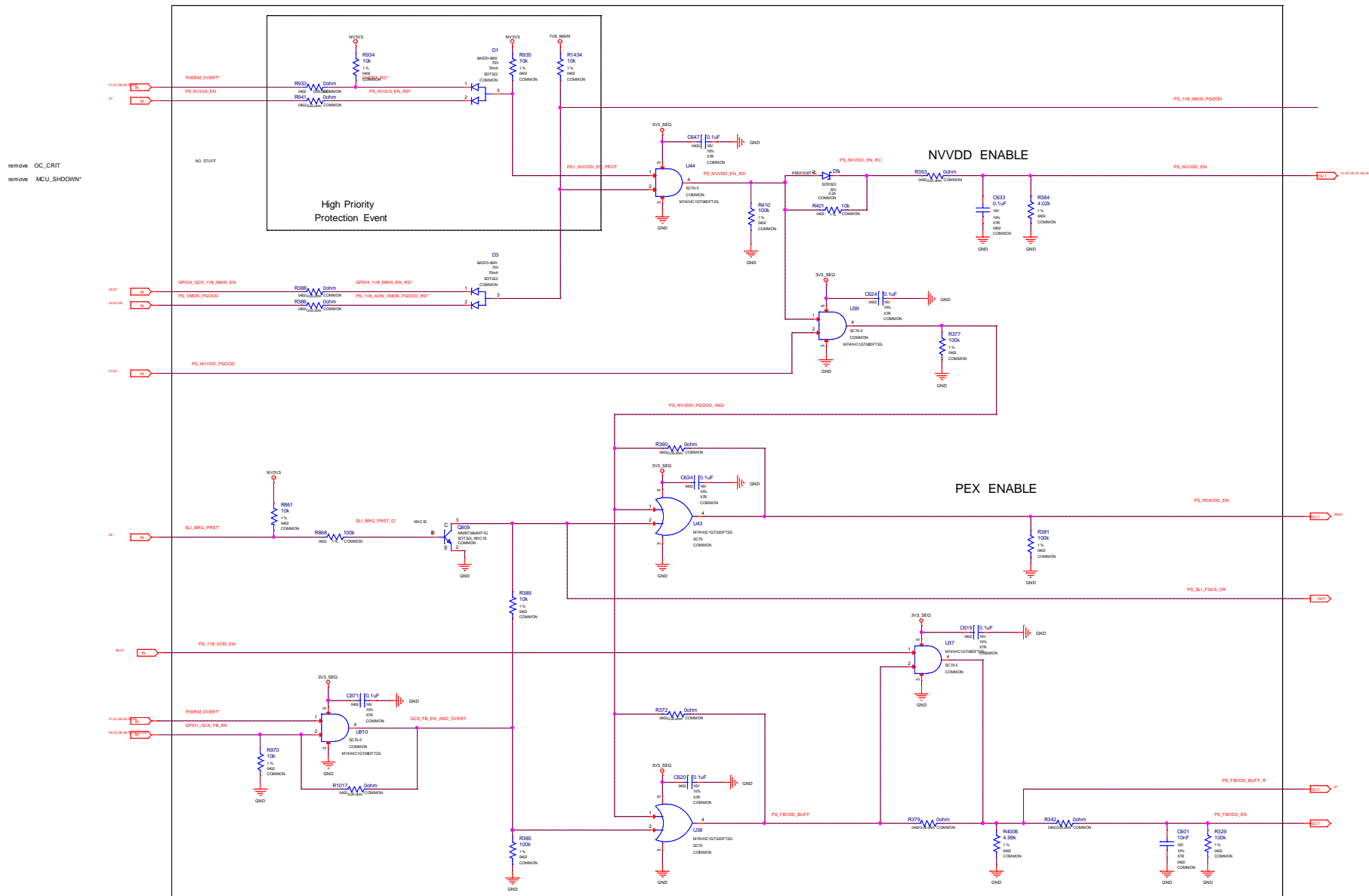
Sequence: 5V, 1V8, NV3V3 EN



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Size Custom	Document Description <b>5V/1V8/NV 3V3</b>	Rev 2.1
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SEQUENCE:NV,PEX,FB ENABLE

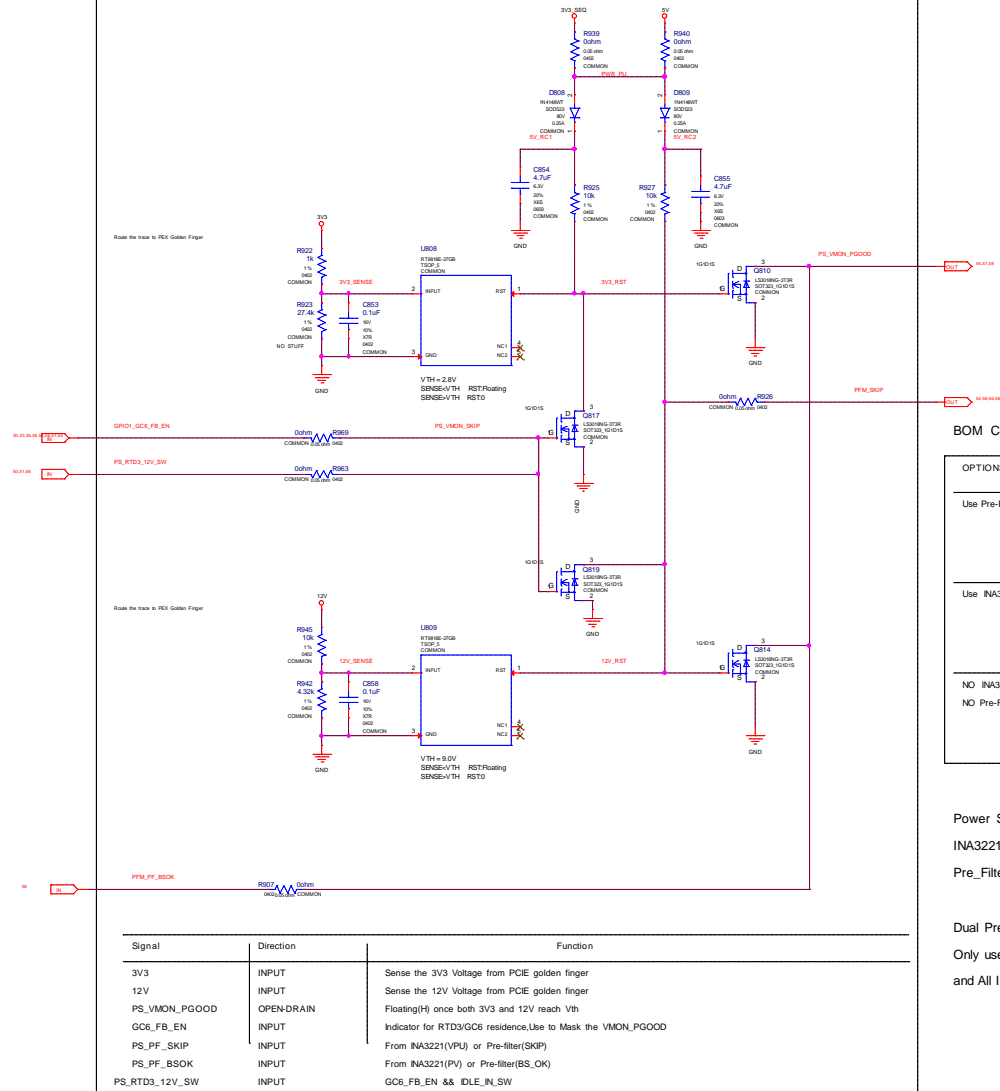


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**MS-V371**

Size Custom	Document Description <b>SEQUENCE:NV,PEX,FB ENABLE</b>	Rev 2.1
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## PCIE Voltage Monitor



## BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	NA

### Power Supply

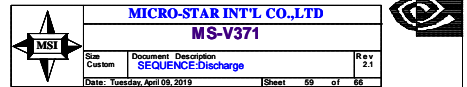
INA3221:3V3\_SEQ

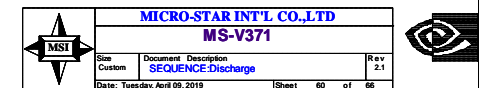
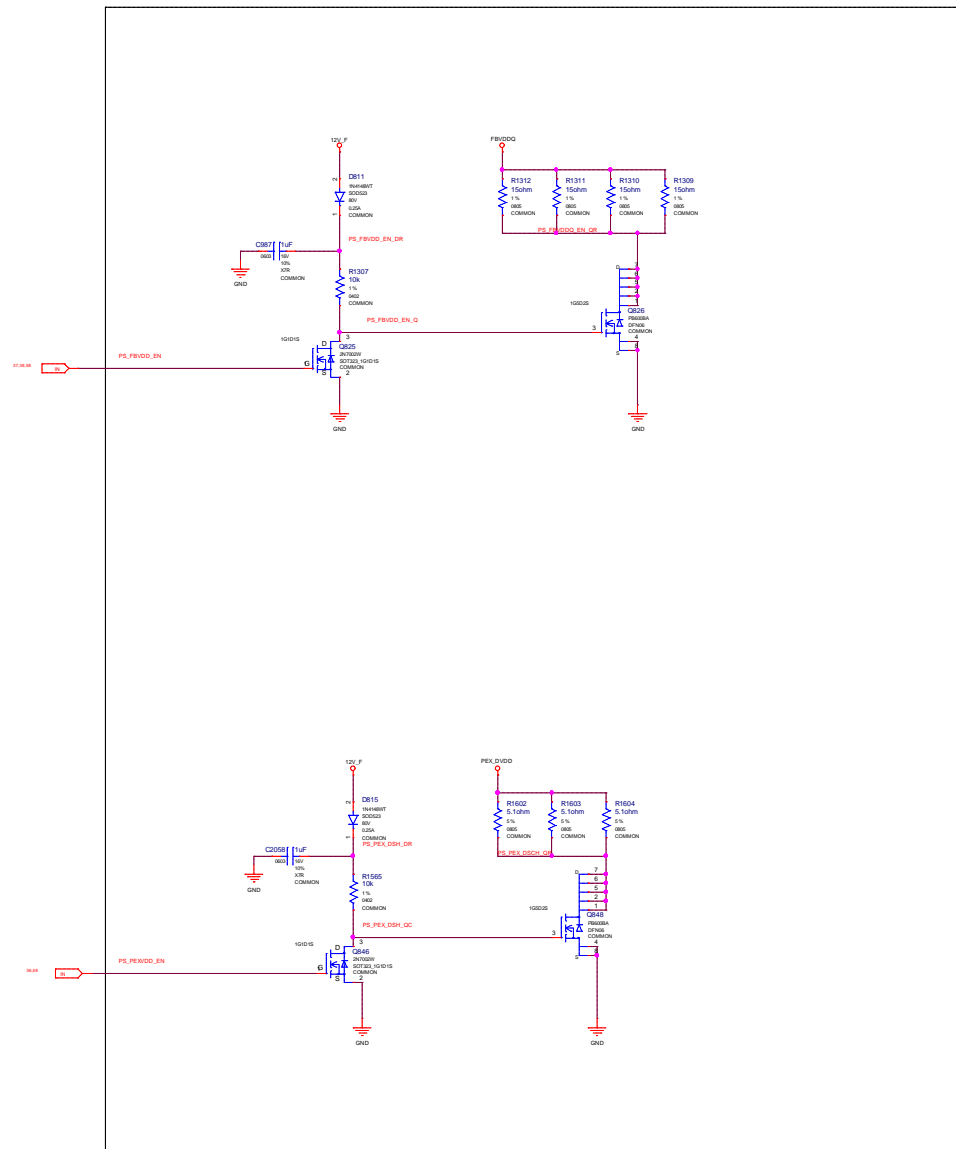
Pre\_Filter(ADC\_MUX):3V3(PEX)

Dual Pre-Filter case:

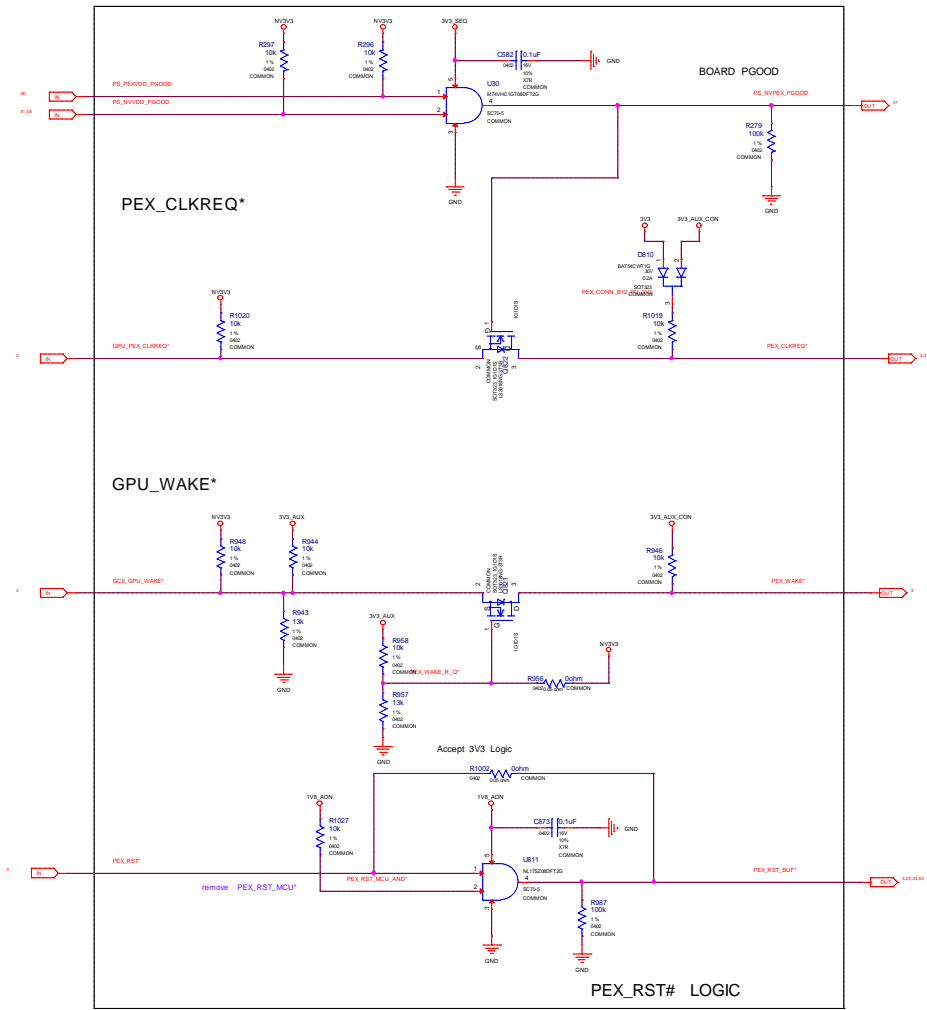
Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

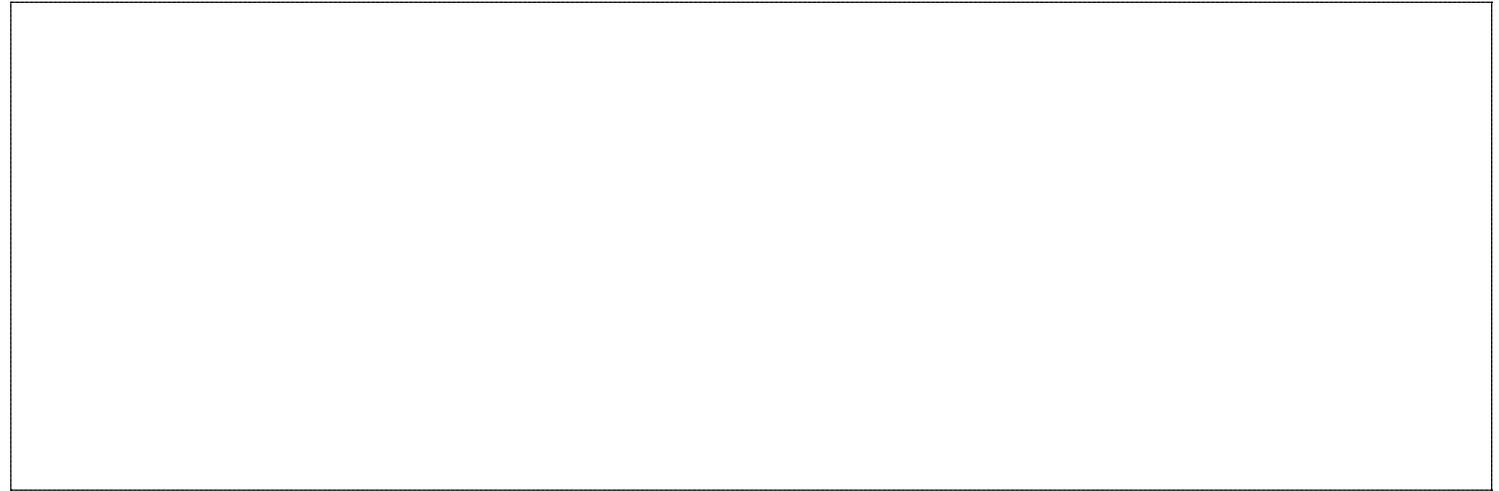
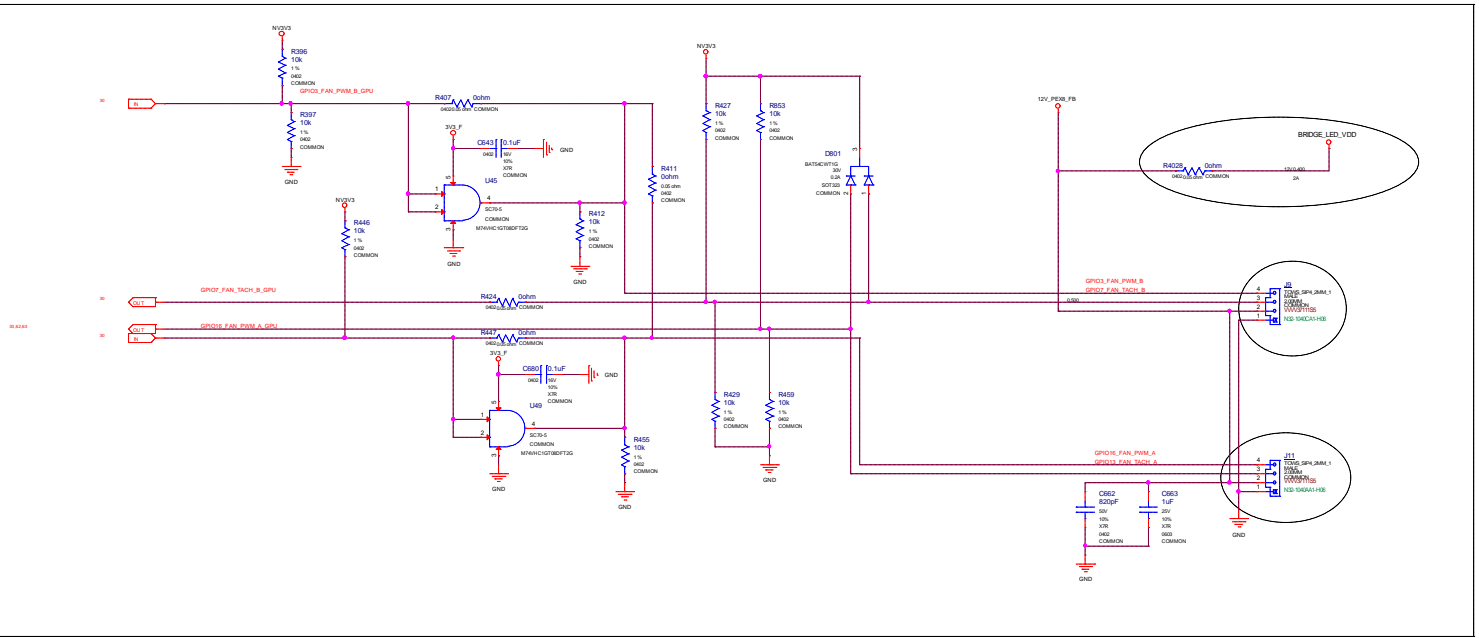




SEQUENCE:MISC



## MISC: FAN &amp; LED1





5V\_LED

GND

3V3\_F

J803

1

2

3

4

5

SMDAT3

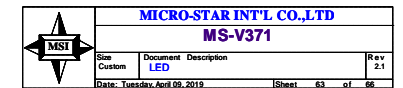
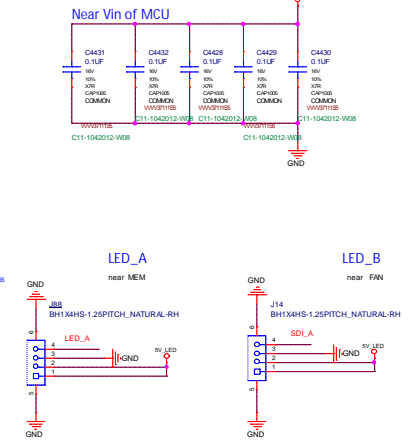
SMCLK3

H1X5

DNI

X000/SP1155

NSC-152065-H06



ZERO IDLE POWER MCU



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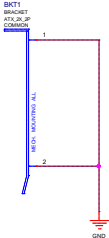
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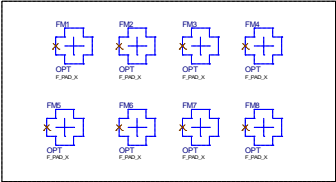
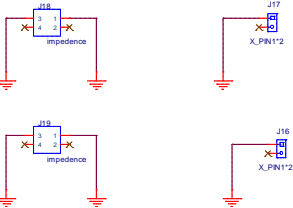
Mechanical: Bracket/Thermal Solution

Brackets:

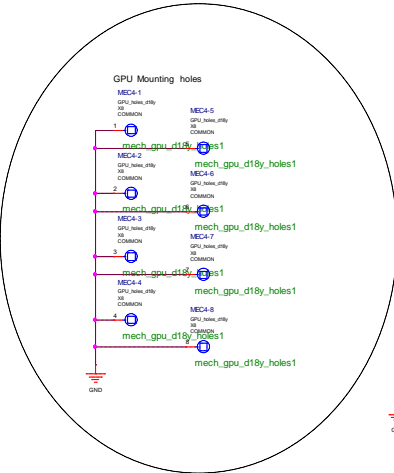


Bracket Screw

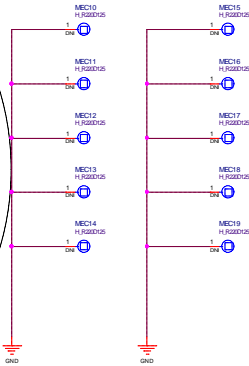
Screw



0726 通孔阵列板规格书 孔位




Mechanical Holes Symbol



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VR THERMAL PROTECTION



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