

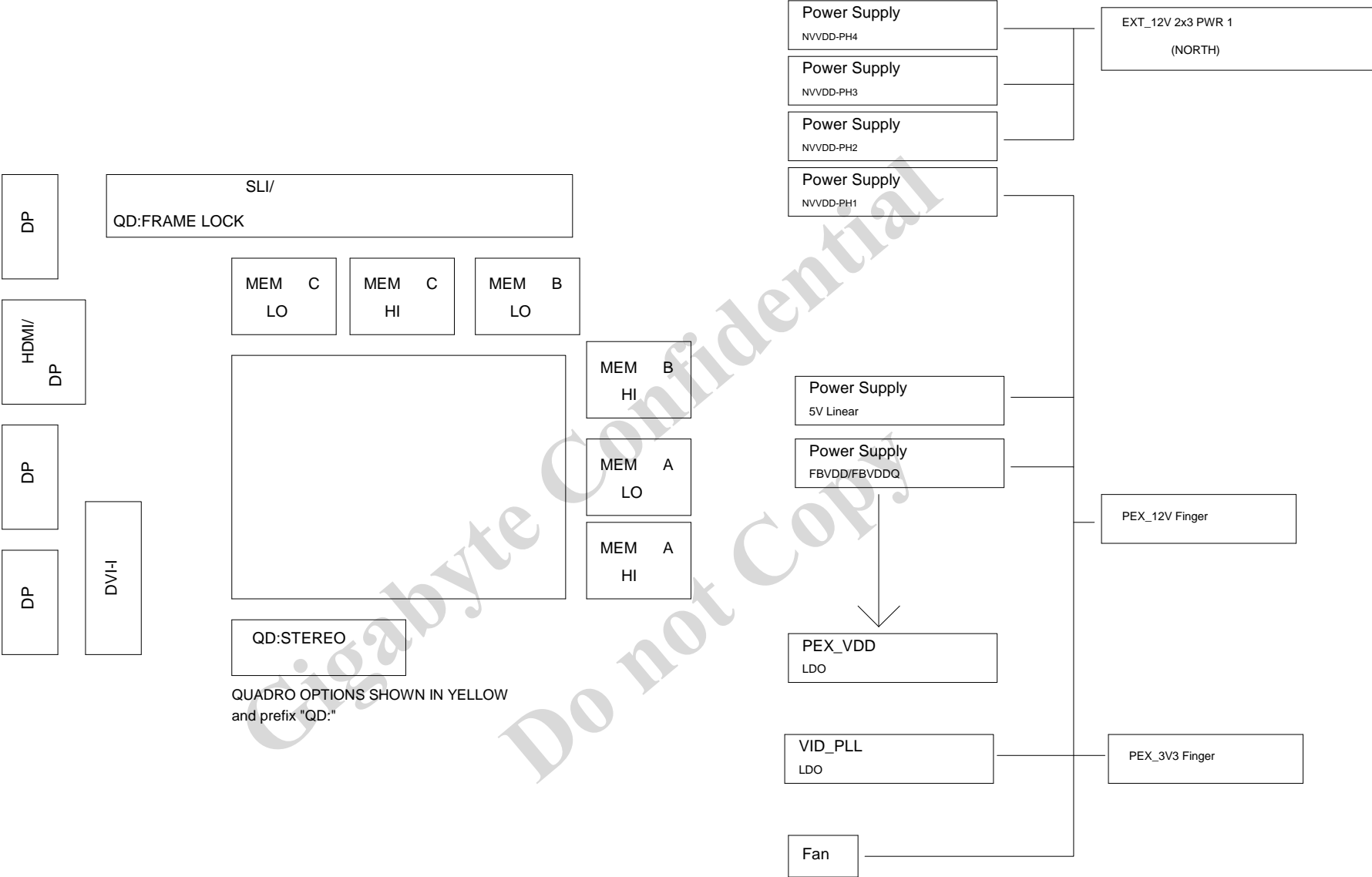
PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI
Tall DVI-I + DP + DP + DP/HDMI + DP

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Block Diagram



QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

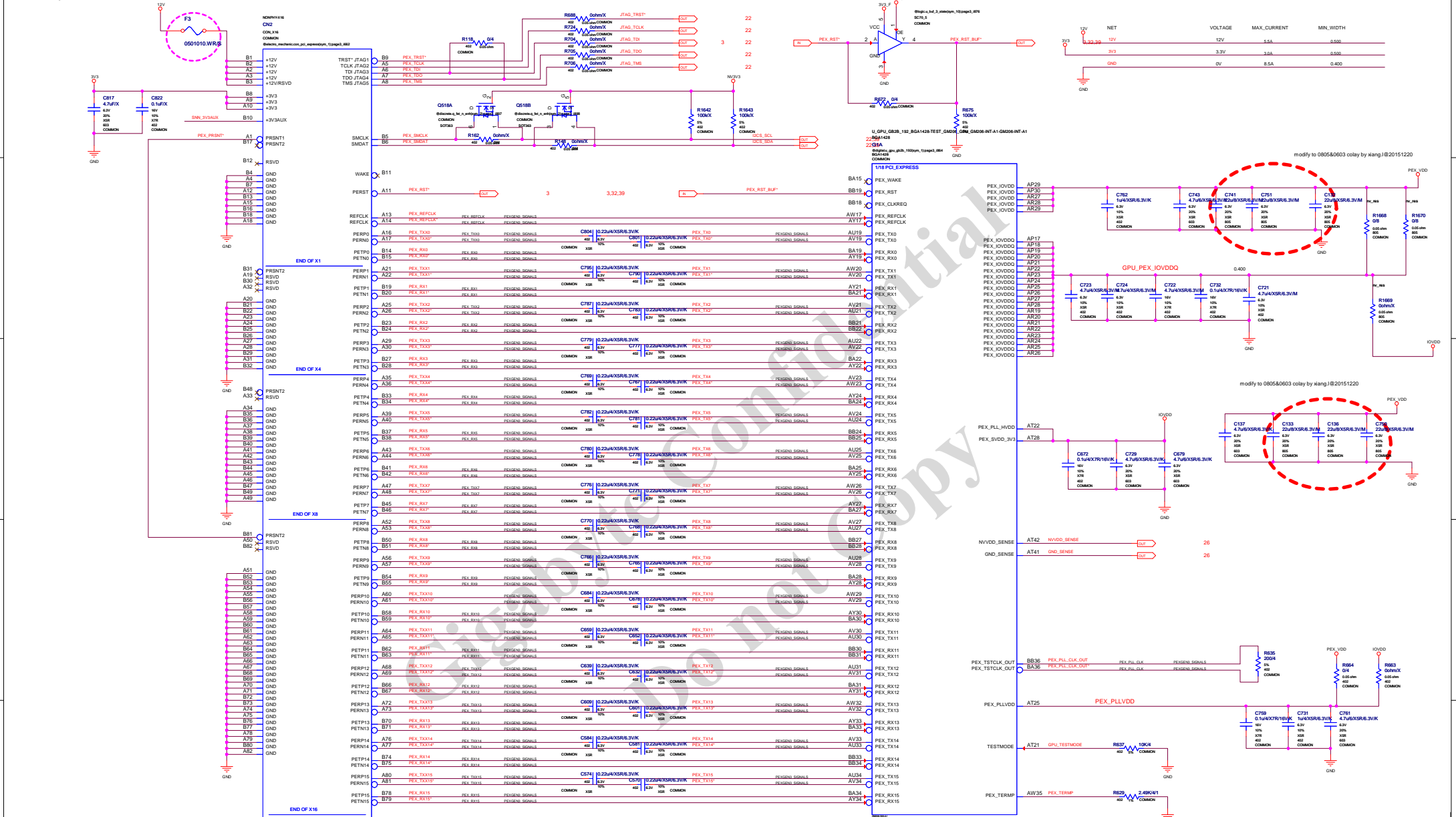
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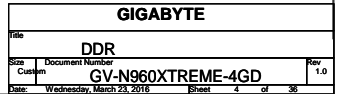
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Block Diagram

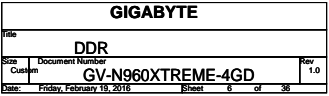
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PCI Express

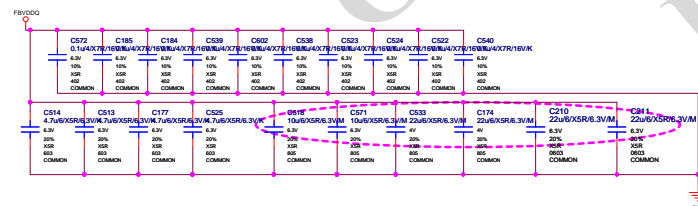
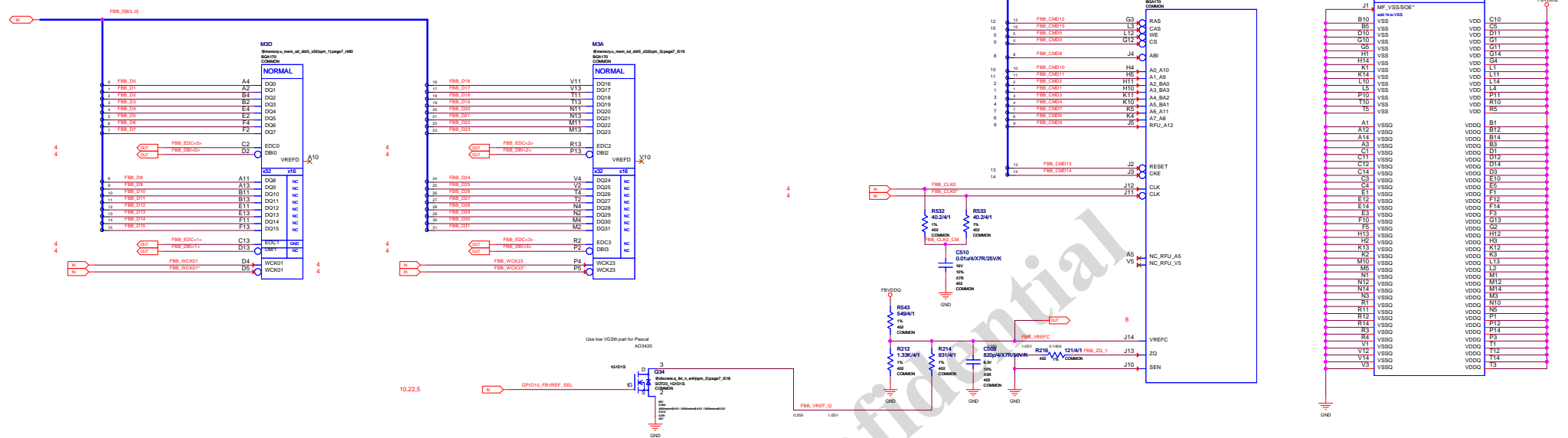


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MEMORY: FBB Partition 31..0



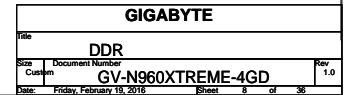
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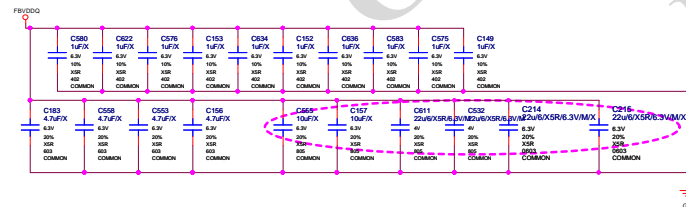
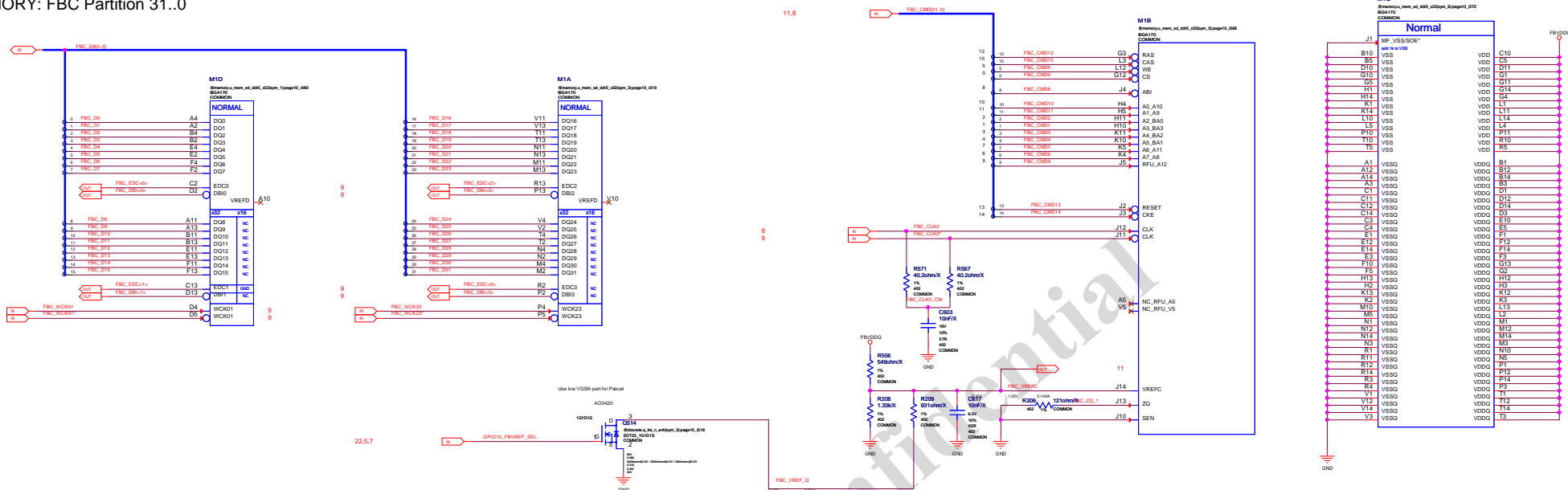
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CME0 C3¹ 32, 32.83
CME1 A2, BA3
CME2 A2, BA0
CME3 A4, BA2
CME4 A3, BA1
CME5 A3, BA0
CME6 A7, AB
CME7 A6, A11
CME8 AB⁰
CME9 A12, RFU
CME10 A4, A10
CME11 A1, AB
CME12 BA3⁰
CME13 AB¹
CME14 CME⁰
CME15 CA5⁰
CME20
CME21 D6G2⁰ D6G2
CME22 C2⁰
CME27 A3, BA3
CME18 A2, BA0
CME19 A4, BA2
CME20 A3, BA1
CME21 WB⁰
CME22 A7, AB
CME23 A6, A11
CME24 AB⁰
CME25 A12, RFU
CME26 A5, A10
CME27 A1, AB
CME28 A3, BA3
CME29 RS1⁰
CME30 CME⁰
CME31 CA5⁰
CME33
CME35 D6G1⁰ D6G1

MEMORY: FBC Partition 31..0



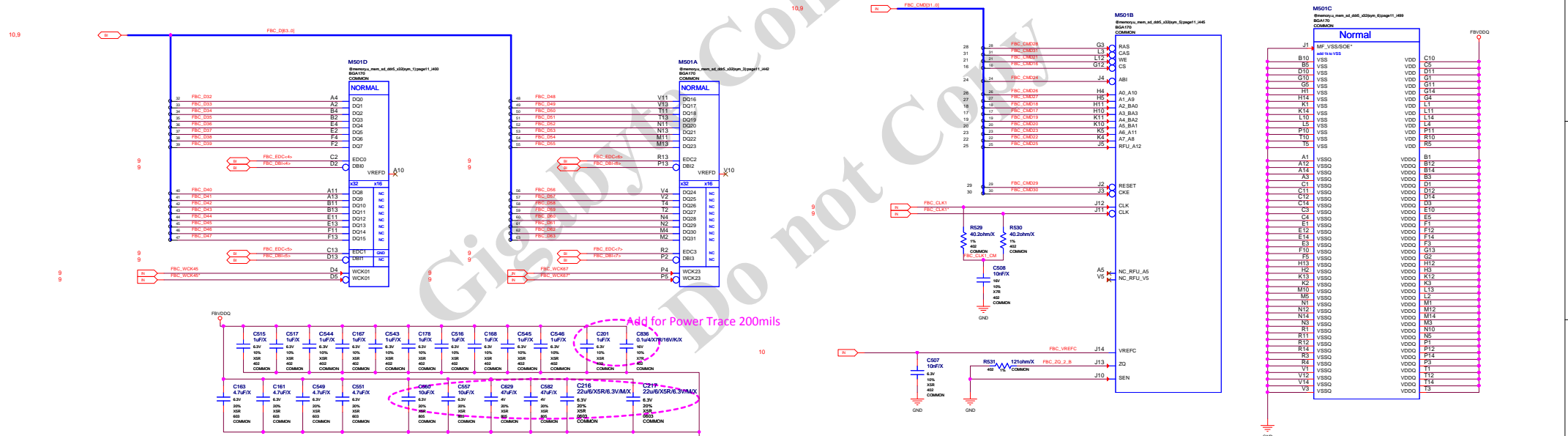
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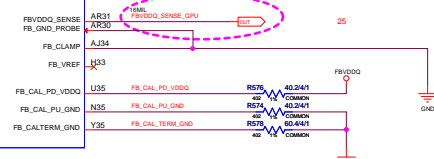
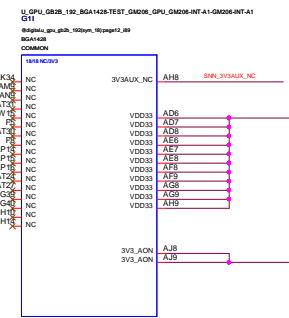
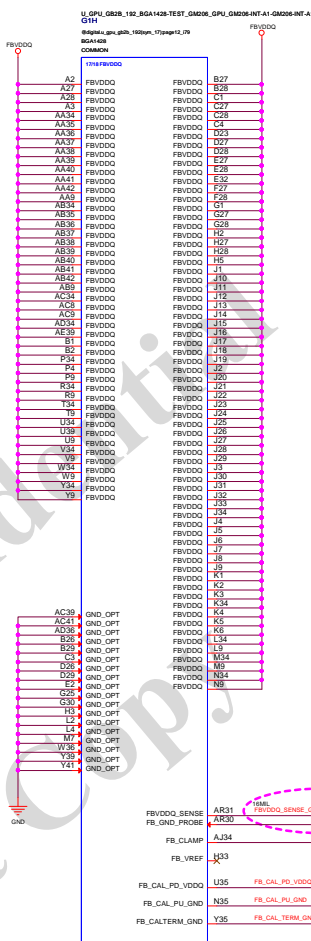
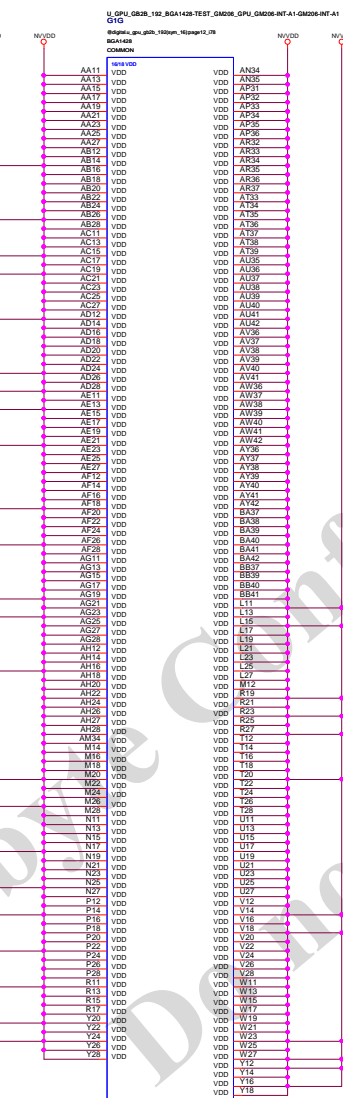
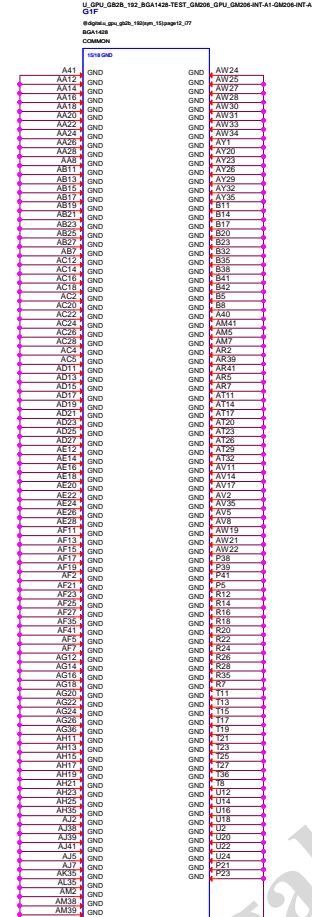
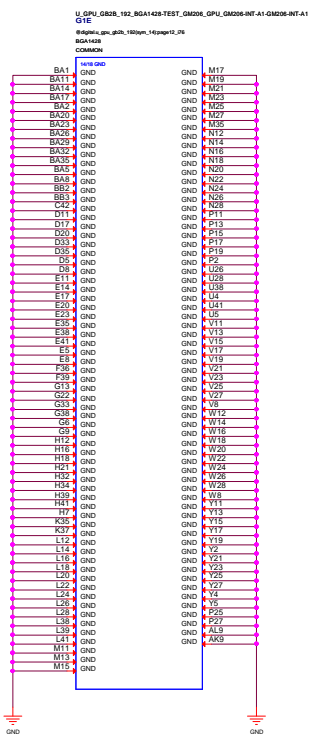
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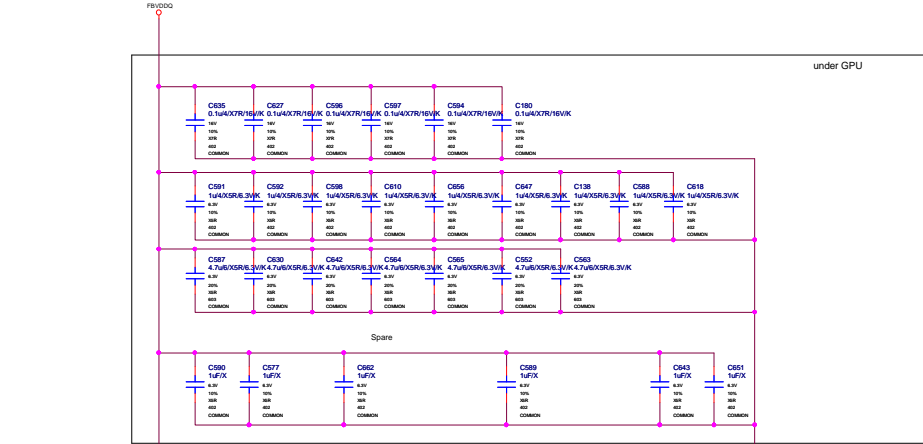


GPU PWR and GND



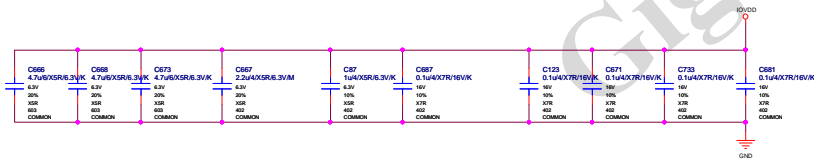
GPU Decoupling

FBVDDQ

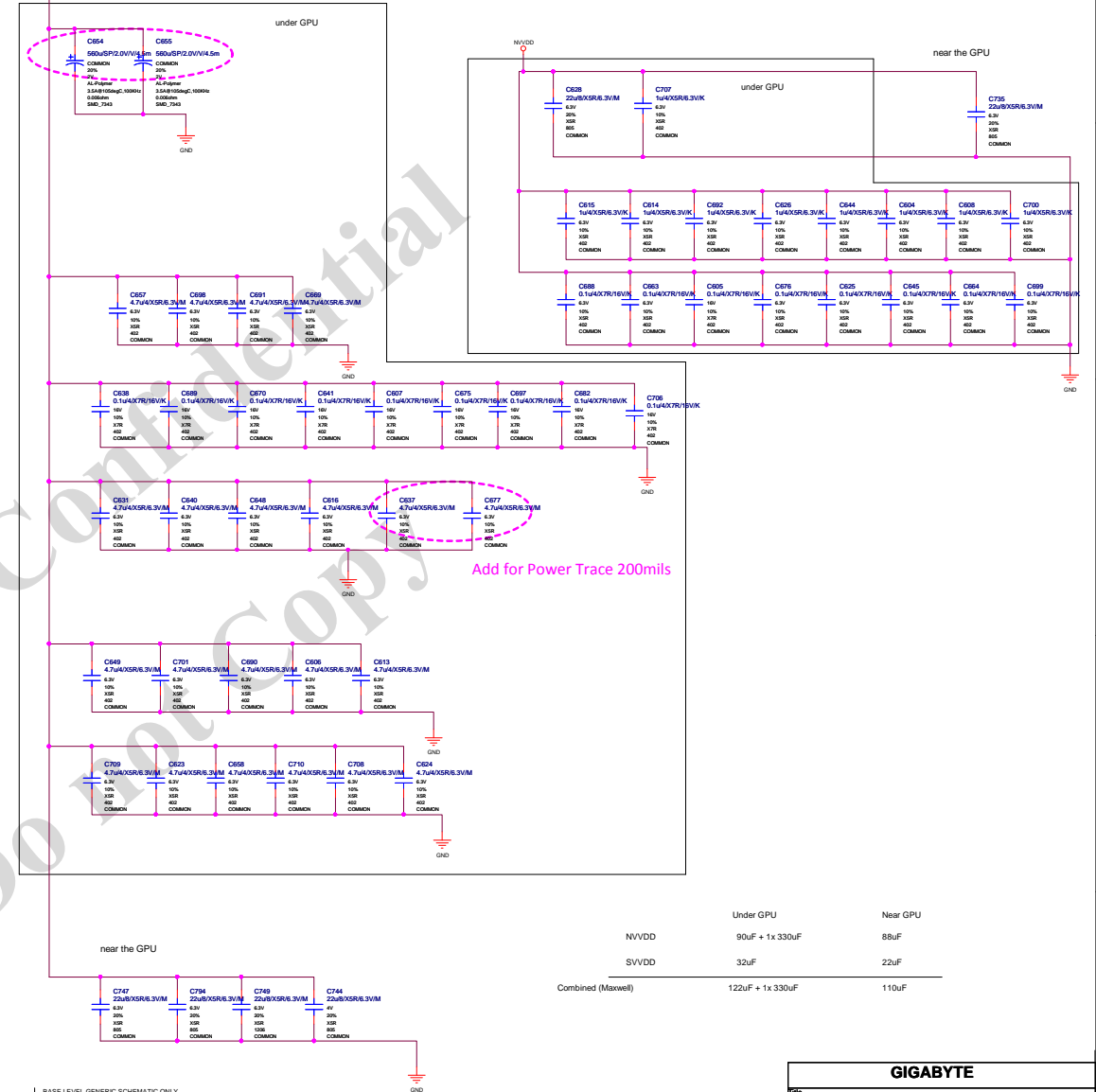


modify to 08050803 colby by xiang.18.2015.1220

Place under/near the GPU



NVVDD



Add for Power Trace 200mils

	Under GPU	Near GPU
NVVDD	90uF + 1x 330uF	88uF
SVVDD	32uF	22uF
Combined (Maxwell)	122uF + 1x 330uF	110uF

ASSEMBLY
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GPU Decoupling

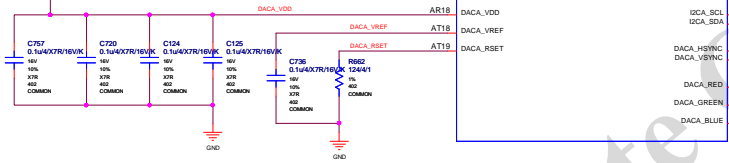
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DACA Interface

15,16,17,19

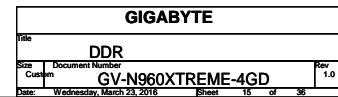


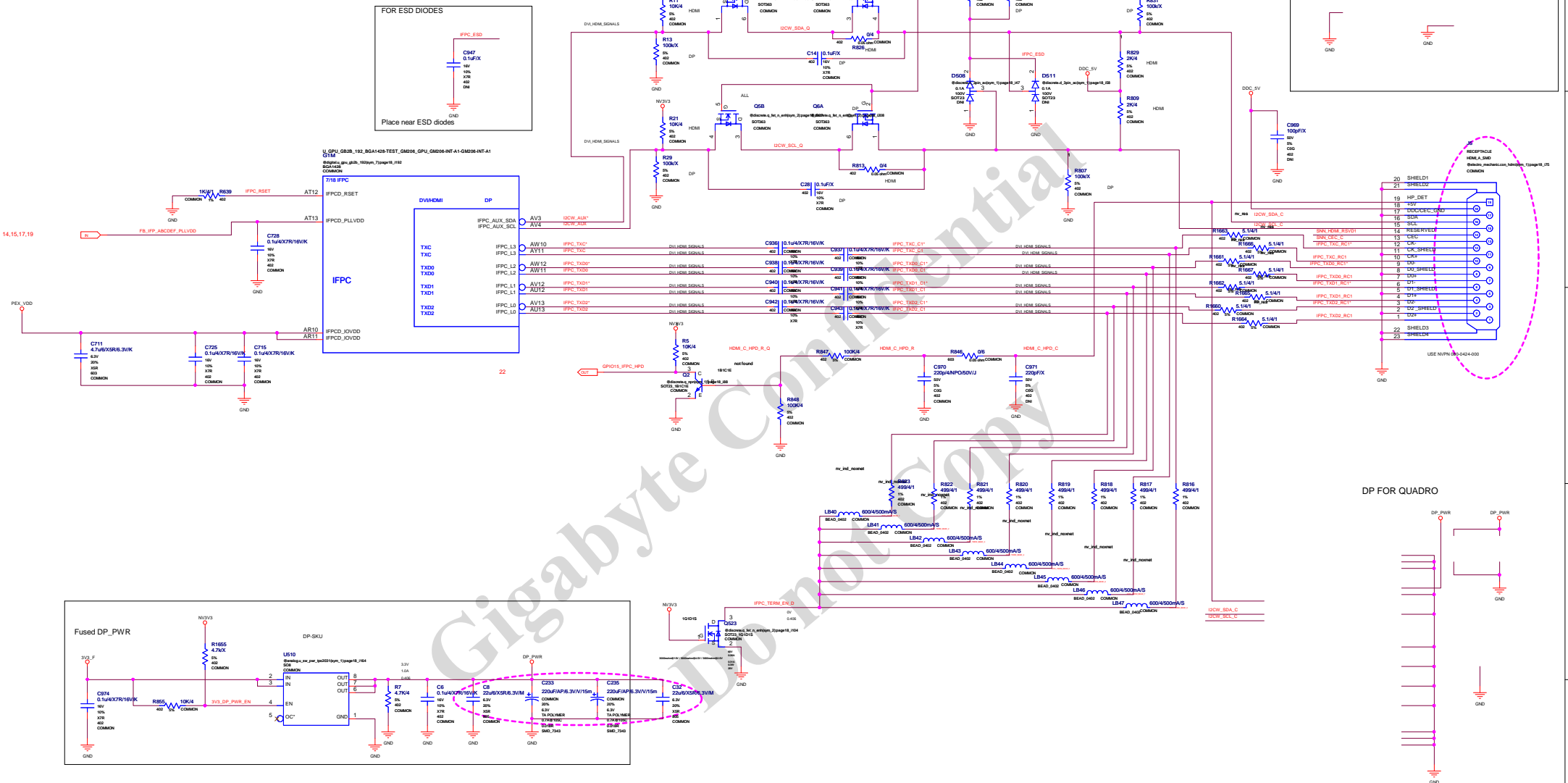
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DACA Interface

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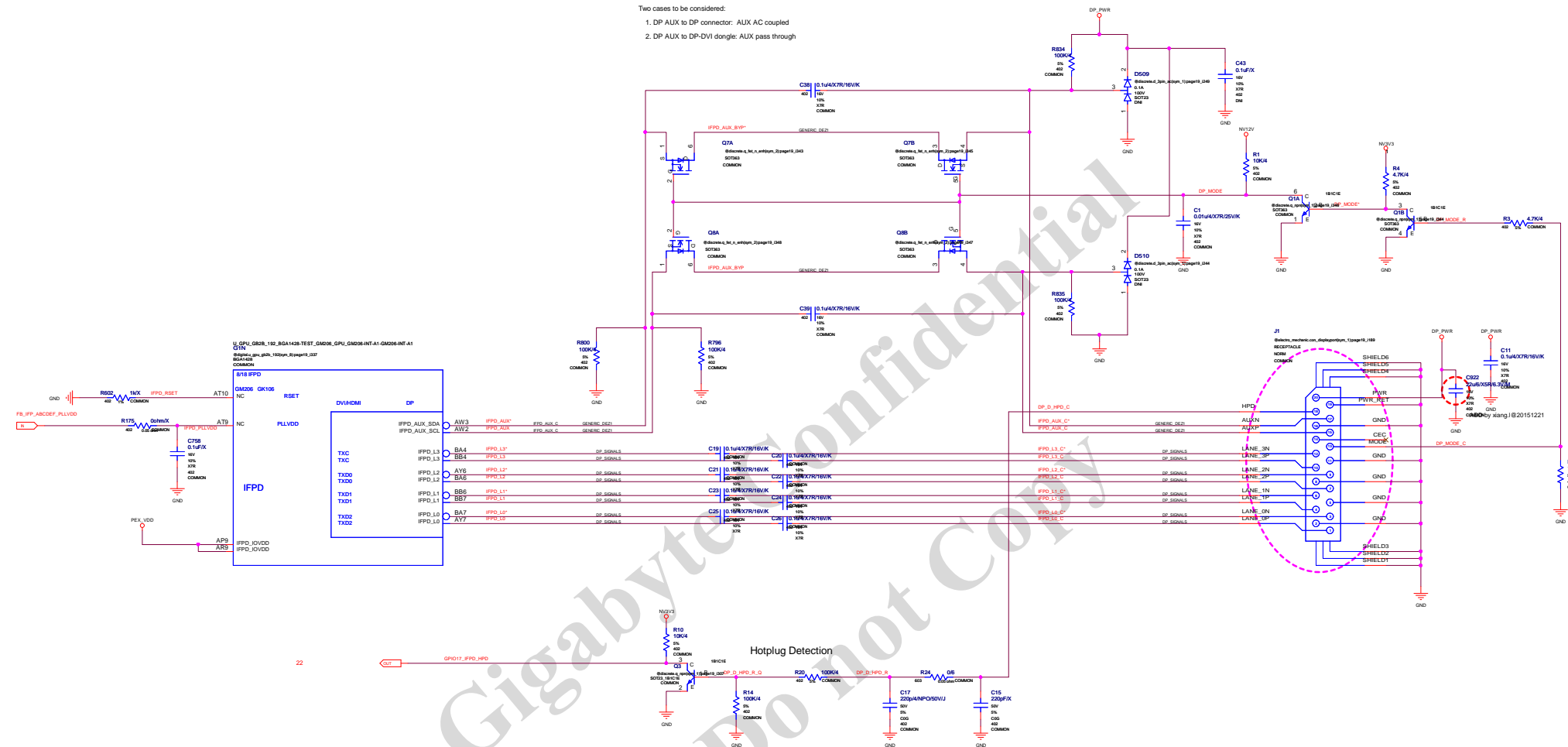
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IFPC HDMI/DP

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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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IFPD DP

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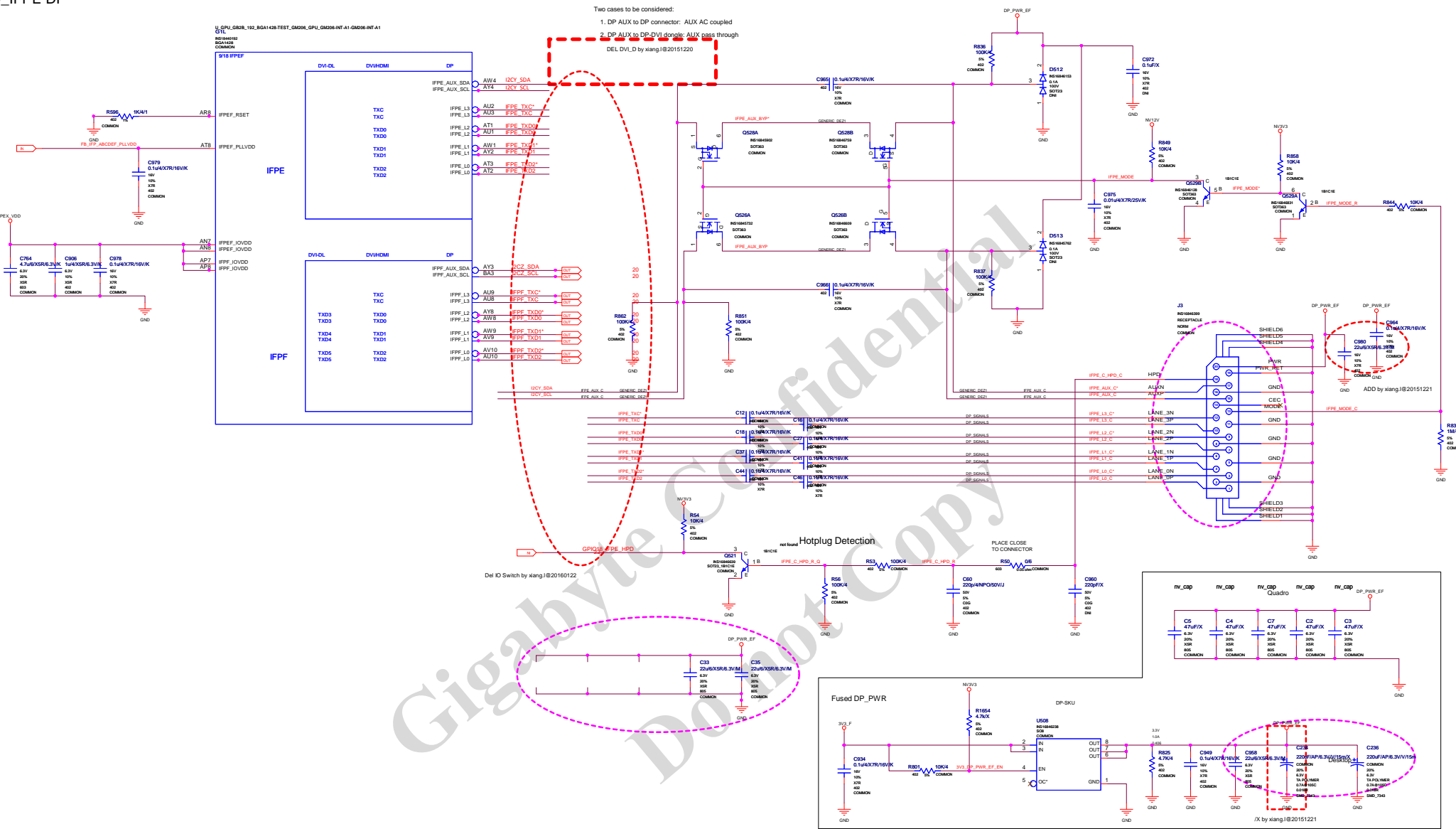
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2

3

4

5



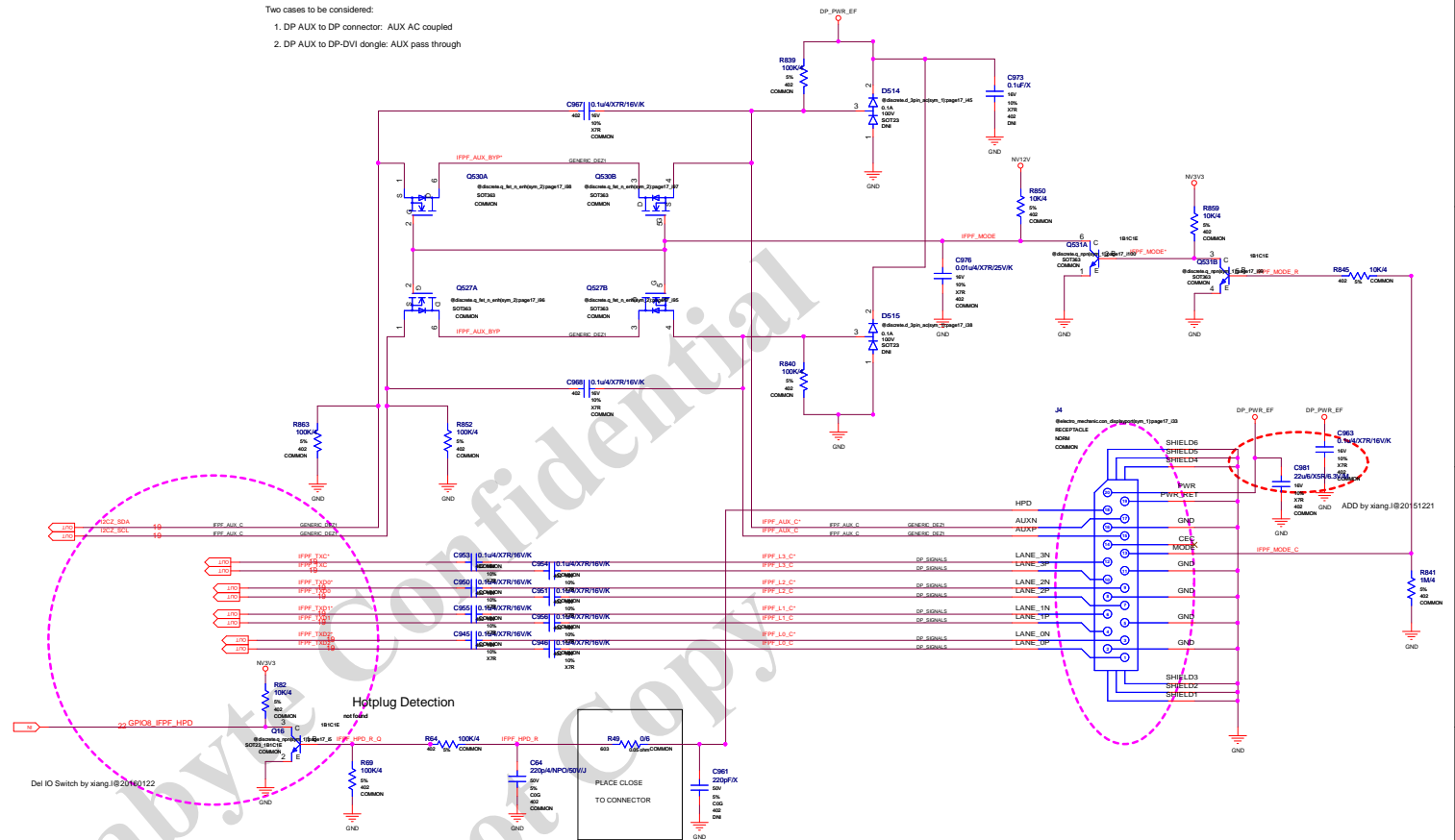
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IFPEF with IFPE DP

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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



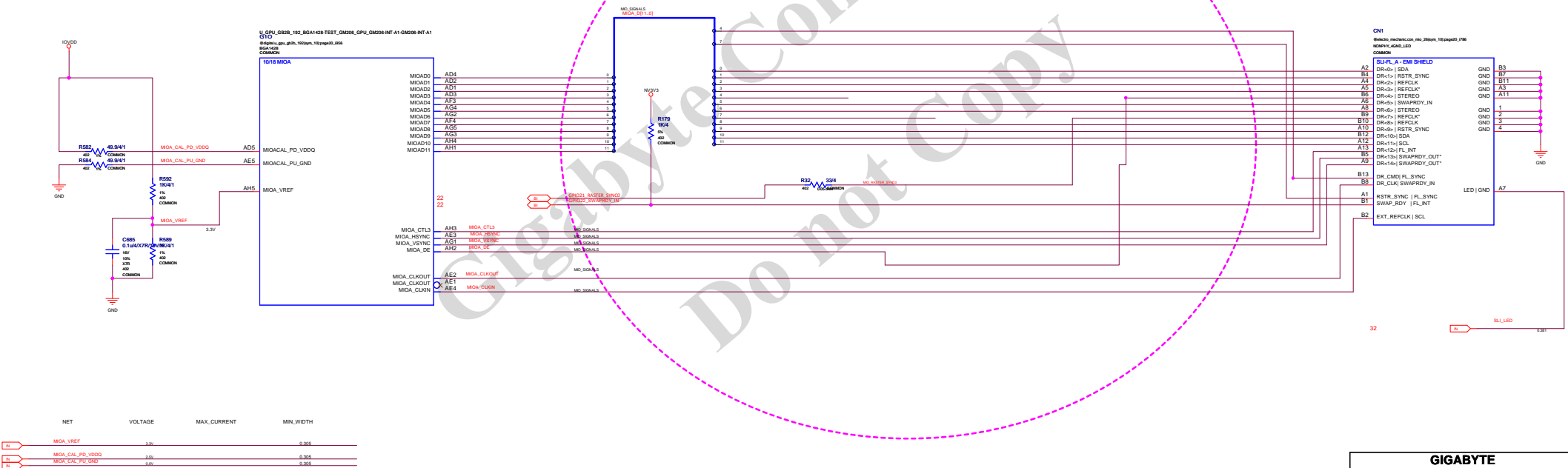
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IFPF DP

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MIOA/SLI Interface

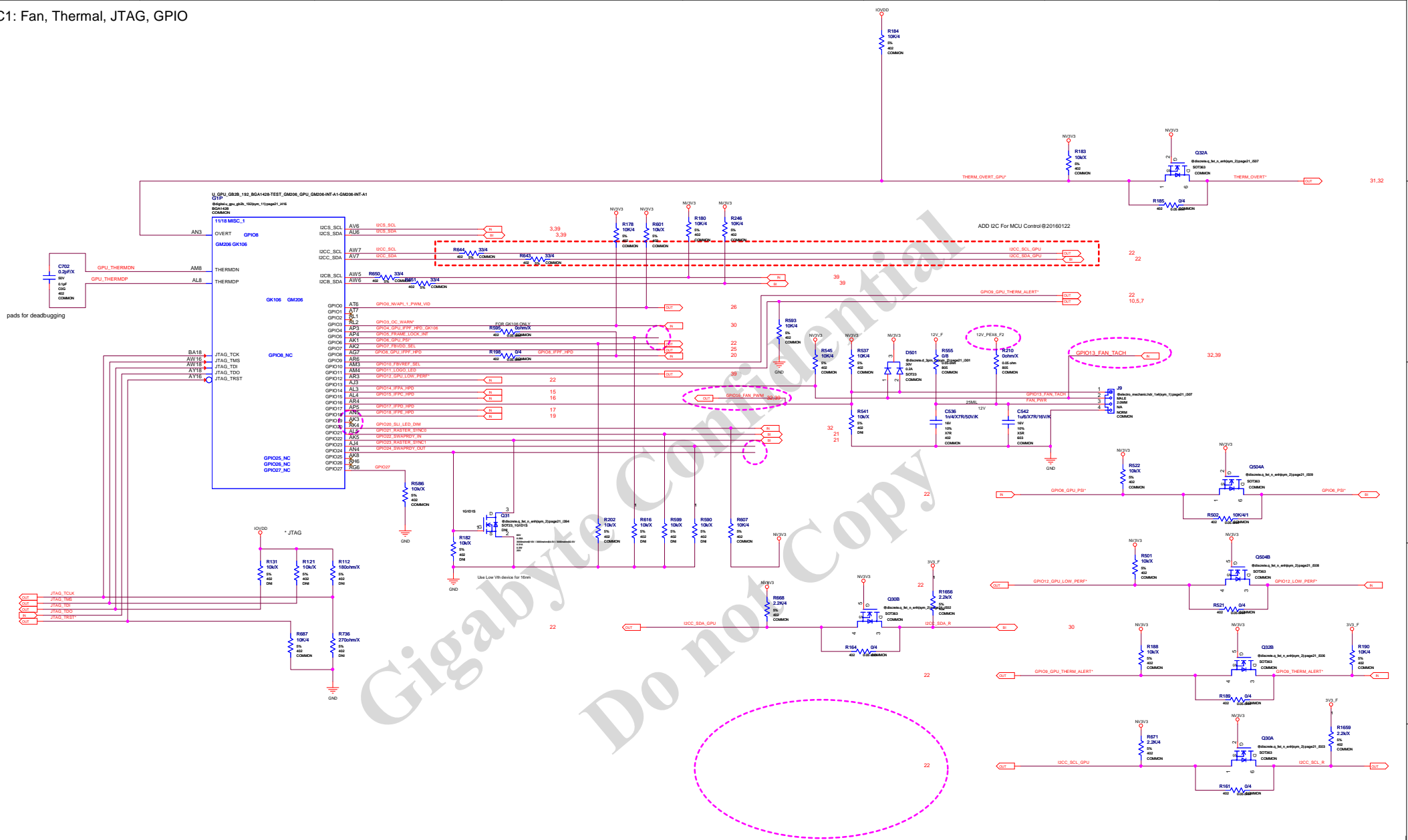


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MISC1: Fan, Thermal, JTAG, GPIO



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MISC1: Fan, Thermal, JTAG, GPIO

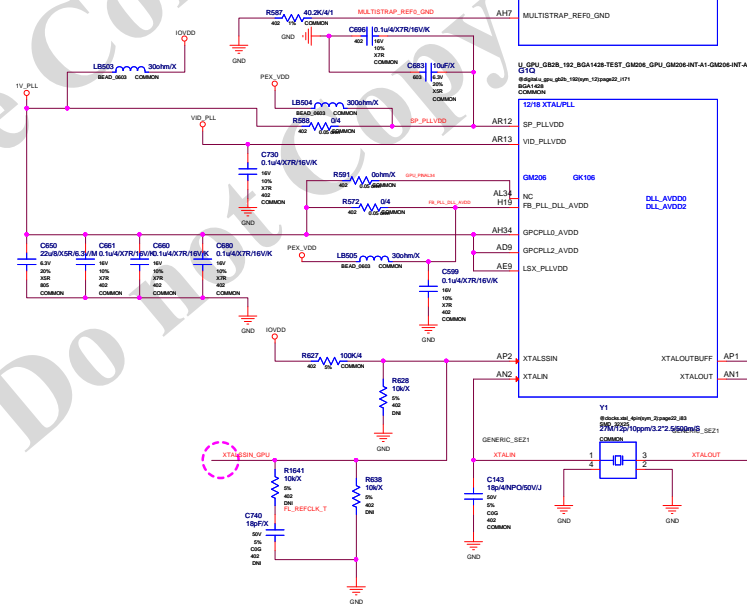
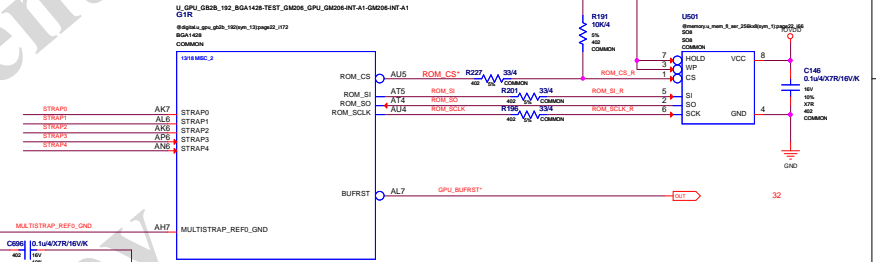
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MISC2: ROM, XTAL, Straps

KEPLER		MAXWELL
STRAP0	USER_BIT [3:0]*	
STRAP1	3GIO_PADCFG_LUT_ADR*	
STRAP2	PCI_DEVID [3:0]*	
STRAP3	SOR_EXPOSED [3:0]*	
STRAP4	DP_PLL_VDDO_33V*	
	PEX_MAX_SPEED*	
	PEX_SPD_CHANGE_GEN3*	
	*	
ROM_SI	RAMCFG[0]*	RAMCFG[0]*
	RAMCFG[1]*	RAMCFG[1]*
	RAMCFG[2]*	RAMCFG[2]*
	RAMCFG[3]*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	VGA_DEVICE*
	SMB_ALT_ADDR*	SMB_ALT_ADDR*
	FB[0]_APERTURE_SIZE*	PCIE_CFG*
	FB[1]_APERTURE_SIZE*	DEVID_SEL*
ROM_SCLK	PEX_PLL_EN_TERM100*	SOR0_EXPOSED*
	PCI_DEVID_EXT[5]*	SOR1_EXPOSED*
	SUB_VENDOR*	SOR2_EXPOSED*
	PCI_DEVID_EXT[4]*	SOR3_EXPOSED*

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111



The diagram illustrates the control logic for a Smart Fan. It consists of two main tables representing logic states.

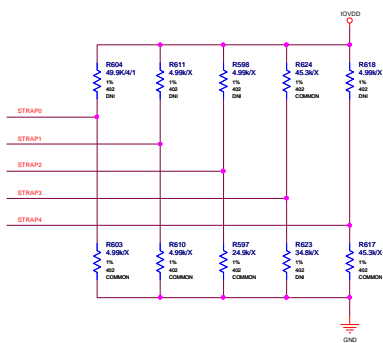
KEPLER

XTALIN	XTALOUTBUFF	Inverted PWM%
PU	PD	66 (20% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (80% HIGH)
PD	PD	0 (100% HIGH)

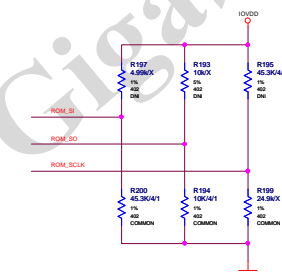
MAXWELL

XTALOUTBUFF
3.3V
1.65V
0V
66%
33%
DISABLED

MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTILEVEL	40.2K 1% TO GND



MAXWELL		
STRAP0		
3.3V	1.65V	0V
GC6+ ISLAND ENABLED	GC6+ DEBUG MODE	GC6+ ISLAND DISABLED



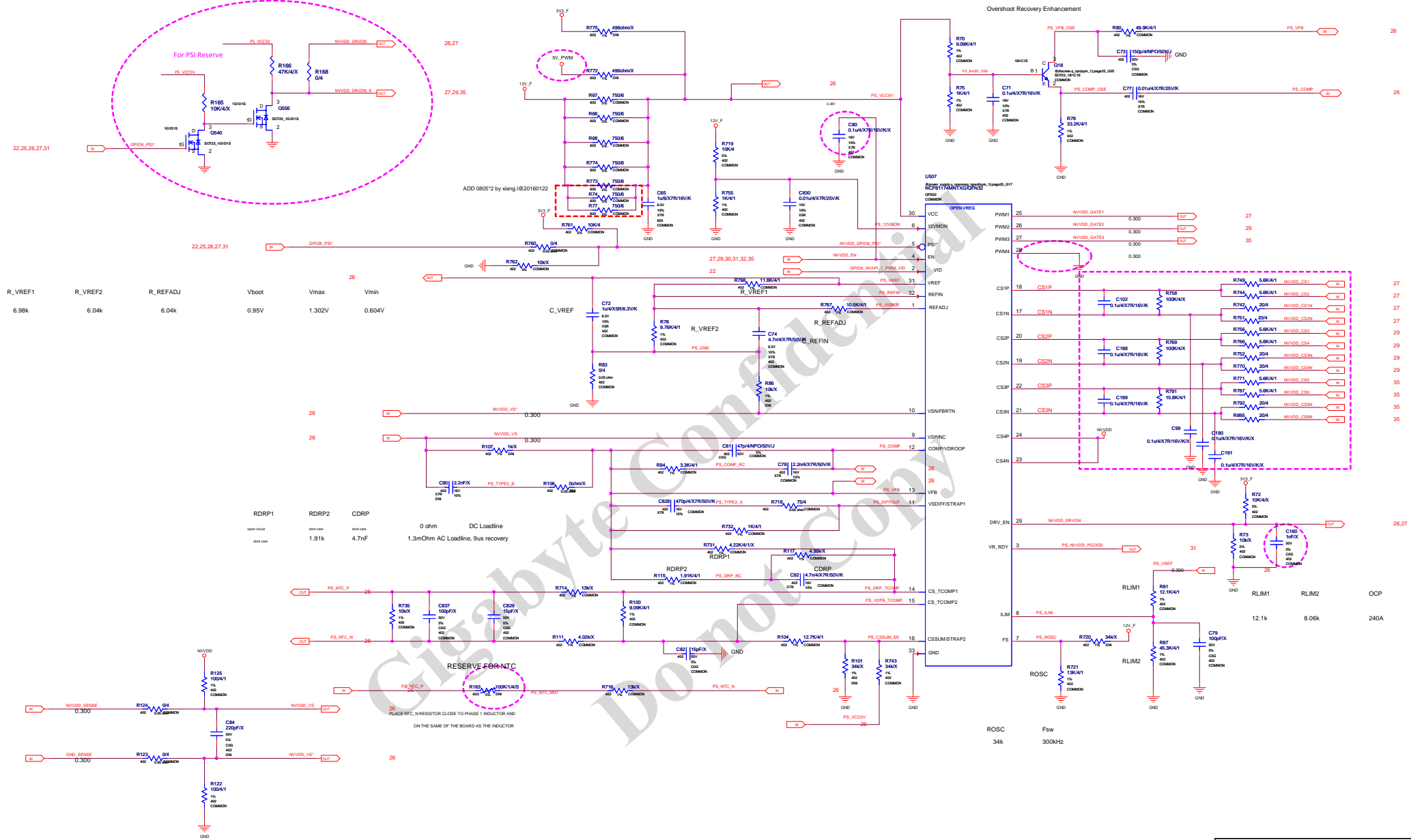
SAMSUNG		HYNIX	ELPIDA
45.3k	PD	34.8k PD	30.1k PD

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MISC2: ROM, XTAL, Straps

GIGABYTE			
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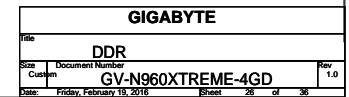
PS: NVVDD Controller



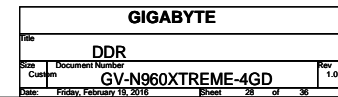
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BASE LEVEL GENERIC SCHEMATIC ONLY
PS: NVVDD Controller D9V4 option

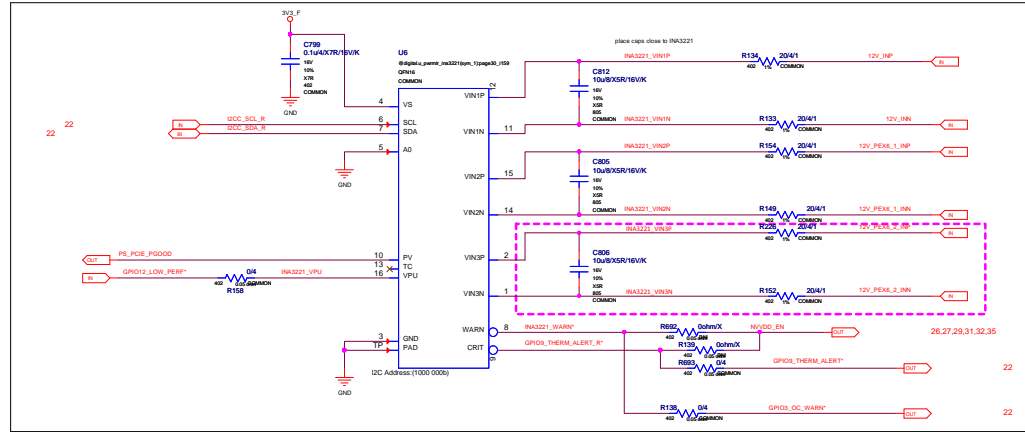
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File	DDR		
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Customer	GV-N960XTREME-4GD		
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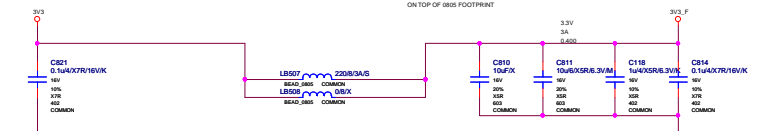
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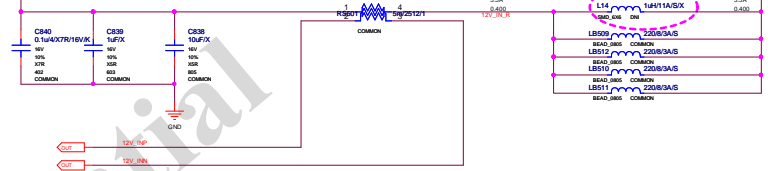
PS: Inputs, Filtering, and Monitoring



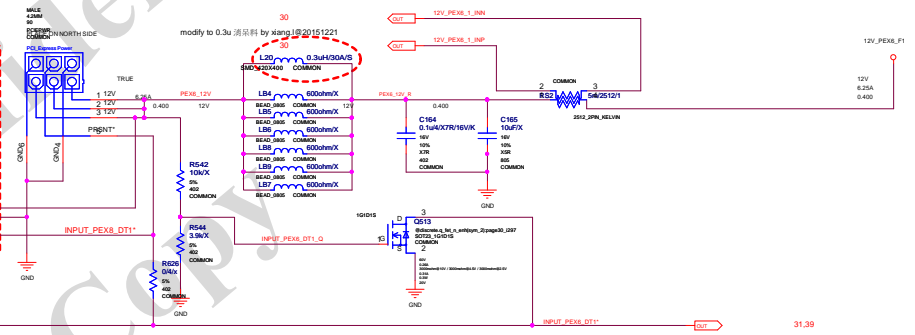
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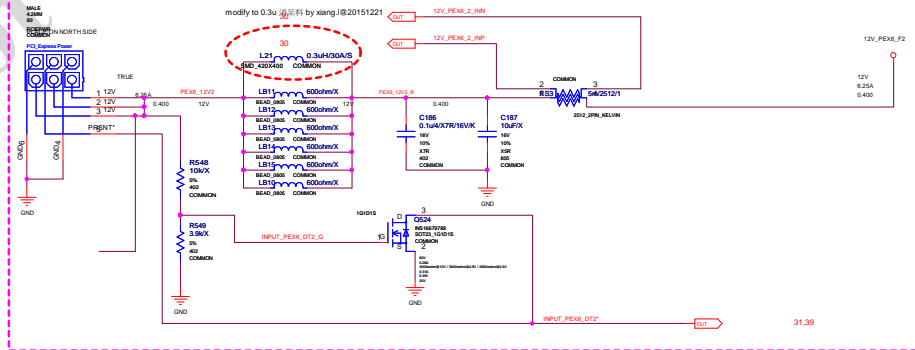
PEX 12V INPUT - 66W



PEX6 INPUT - 2x3 PCIe CON 75W



PEX6 INPUT - 2x3 PCIe CON 75W



LED1 放置在 J14 附近

LED3 放置在 J13/J16 附近

ADD 12V 前馈电路 by xiangj@20151220

GIGABYTE

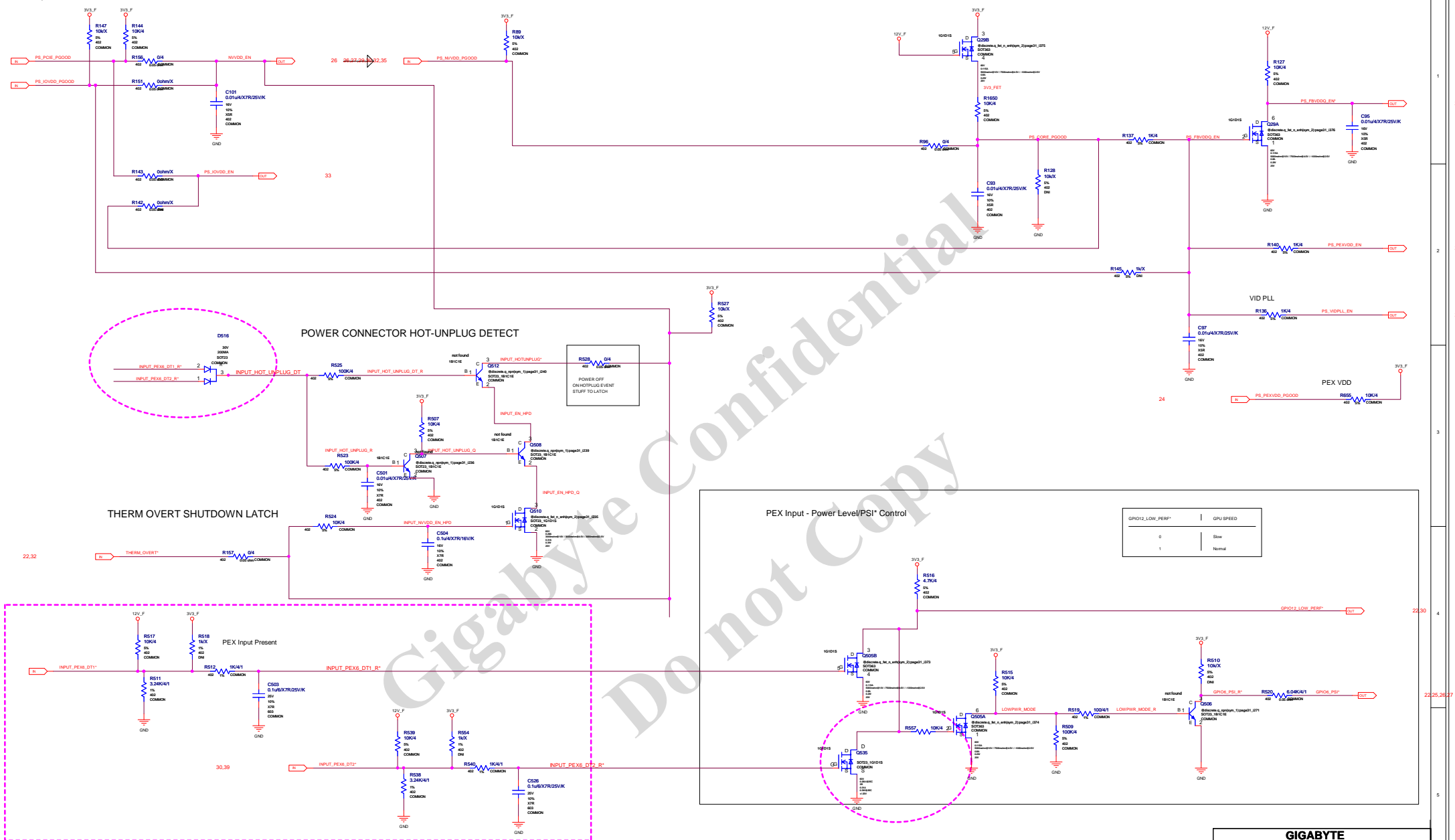
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PS: Inputs, Filtering, and Monitoring

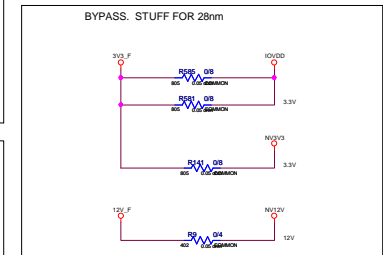
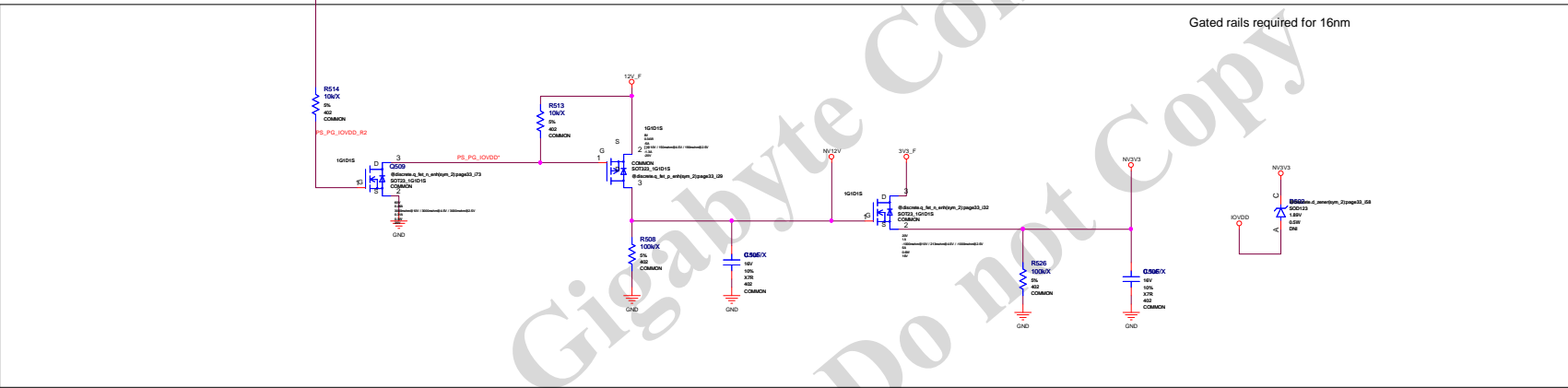
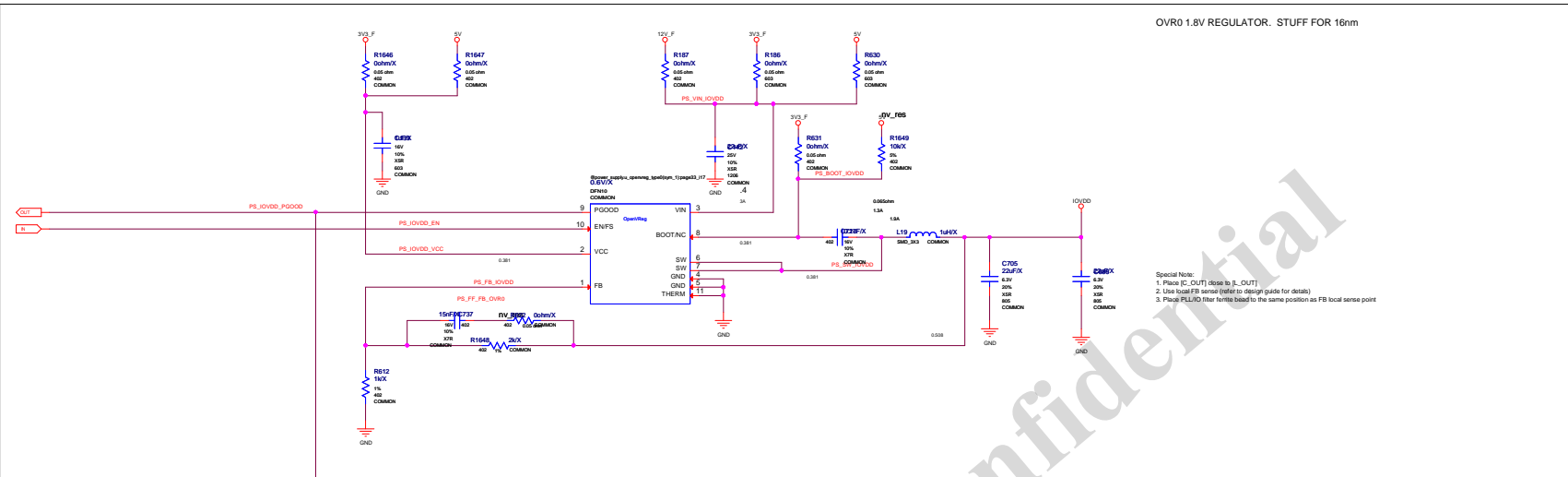
PS: Sequence and Shutdown



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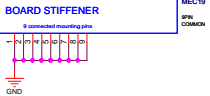
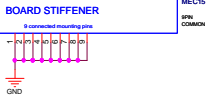
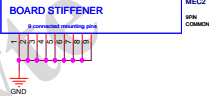
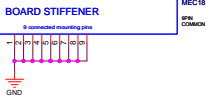
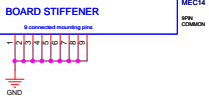
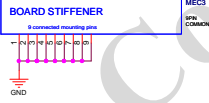
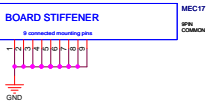
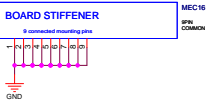
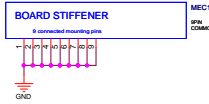
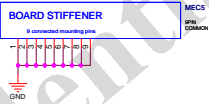
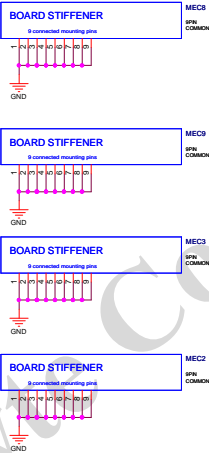
BASE LEVEL GENERIC SCHEMATIC ONLY
PS: Sequence and Shutdown

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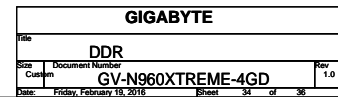
DEL Fan Top LED by xiang.1@20151221

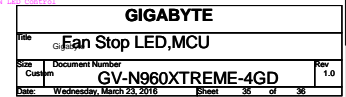
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MECH: Bracket/Thermal

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SCH REV	PCB REV	DATE	REVISION DESCRIPTION
01	01	2016/1/27	Modify From N960G1 GAMING-2GD 1.02-DEL DVI-D,ADD Page 35 MCU&RGB 光圖
1.0	1.0	2016/3/17	PVT 修改文字面，線路未改動

GIGABYTE			
Title History			
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