

PRIMARY ** VGA1 DAC A ** LFH1 TMD5 A I2C_A.
SECONDARY ** S-VIDEO/TV-OUT DAC B ** LFH2 VGA2 TMD5 B I2C_B
VIDCAP ** VIP 7113 I2C_C.
9pin DIN ** RGB2 I2C_C.

X01: P78-A00
New File Created P71-X39+memory of P75 and new Mem PS

X02: P78-A00
Memory Address bus termination removed

X03: P78-A00
Cleanup- Design Review updates

X04: P78-A00
Mem Data/DQM bus Swapped on 11/14/01

X05: P78-A00
IFP PLLVDD REGULATOR ADDED
FBBCLK0 and 1 interchanged

X06: P78-A00
U201/U203
Mem clock Pullups not required-R243 to R250 removed.
MVREF res package changed from 0603 to 0402 for
R219,R220 to R222, R239 to R242
U201- nets FBD19,20,21 swapped

X07: P78-A00
For I2C-2 Pull up/Protection
R1033 to 1036(4 pcs), 0603 added
L602, L603 (2pcs), 0805 added.
C883,C884 (2pcs), 0603 added
D505, D506 (2pcs), sot23 added.

X08: P78-A00
Changed the power for GPU Frame buffer decaps. Should be
FBVDDQ/FBVDD.
Deleted C868, C846 - TH part no space.
L602, L603- Package changed from 0805 to 0603.
GPU VDDDV0, C529, C530 AND DVOVREF TO 3.3V instead of
A3.3V

X09: P78-A00
ADDED ONE MORE REGULATOR FOR IFP PLLVDD
C885, C886 -0805 ADDED
R1038,R1039-0402 ADDED
U825 ADDED
R1028, R1029, R1031, R1032 PACKAGE
CHANGED TO 0402.

X10: P78-A00-Final Review
C419, C886 removed.-Not required

X11: P78-A00
R1040 Pull Down for Hotswap input added

X12: P78-A00
R616 added in series to Core switcher
12V input

X13: P78-A00
R201 AND C293 to be on FBVDD/Q instead of 3.3V

X14: P78-A00-PCB X-Released
Moved C618 CAP from 12V to 12V_IN

X15: P78-A00 -SCH X-Released
Memory Power R609 to 2.8V or 2.5V Sku.
R609 CHANGED TO 154R FROM 150R FOR 2.8V
Bracket component added to SCH

NVVD more comments added in PS sheet
Mem PScomments edited in PS sheet

- PAGE OVERVIEW
- 1 top (this) page
 - 2 1. AGP interface, core decoupling
 - 3 2.a NV17 Frame Buffer
 - 4 2.b Frame Buffer 0..63
 - 5 2.c Frame Buffer 64...127
 - 6 3.a Dual DAC, 1st VGA
 - 7 3.b Dual DAC, 2nd LFH
 - 8 4. LFH/Panel
 - 9 5. TV-out, video capture, stereo
 - 10 6. Power supply
 - 11 6a. Memory Linear Regulator
 - 12 7. BIOS, Strapping

P78, NV17, 4Mx32 DDR, 64MB, RGB, TV-out, video capture, AGP4X

PCI DEVICE ID = 0X171 FOR NV17-128D.



X17: P78-A00
Y300 Should be 18pF XTAL
C320,C321- New tuned values are 18pF
New Discrete VGA filter component values
changed to 10pF-68nH-No cap- 68nH-10pF.
NO_STUFF Integrated filter components.

U511 memory regulator o/p current spec lowerd to 2.0A
and Added new NVPN for 2.5V.
C145 No_stuff
U701-More substitute added
P300-DB15 and Bracket replaced with new PN.

X18: P78-A00
VGA Filter 10pF to be stuffed, missed in X17

X19: P78-A00
Add note in SCH that SAA7113 is not
supported in this design
Heat sink M2 changed from 45x45mm to 53x64mm

X20: P78-A00
PCI Device ID bit labels were reversed, Corrected.
FOR LFH we need 15pF caps for C335, C329, C332, C341,
C344, C338 in VGA Filter
R1031, R1032, R1038, R1039, resistor values corrected.

P78-A01-X01
Add D-FF buffer to PCIRST_ signal. Added U101.
Add R325, series termination res to XTALBUFF signal
Add R111, C146 smoothing ckt to PCIRST.
Add R112 to by pass D-FF ckt.
Replaced pkg IND_SMD0805_FLT with SMD0805 for L316-L318, L305, L307, L308
ADD SS Control circuit for 3.3V rail coming delayed
(No problem observed in P78 but in other Pxx)
Added Q2, Q3, D25, R618-R620
AGPSTOP pulled to 3.3V from AGPVDDQ

P78-A01-X02
Add R113 & R114 to D-FF ckt and Asynchronously Reset the o/p D-FF using PCIRST_

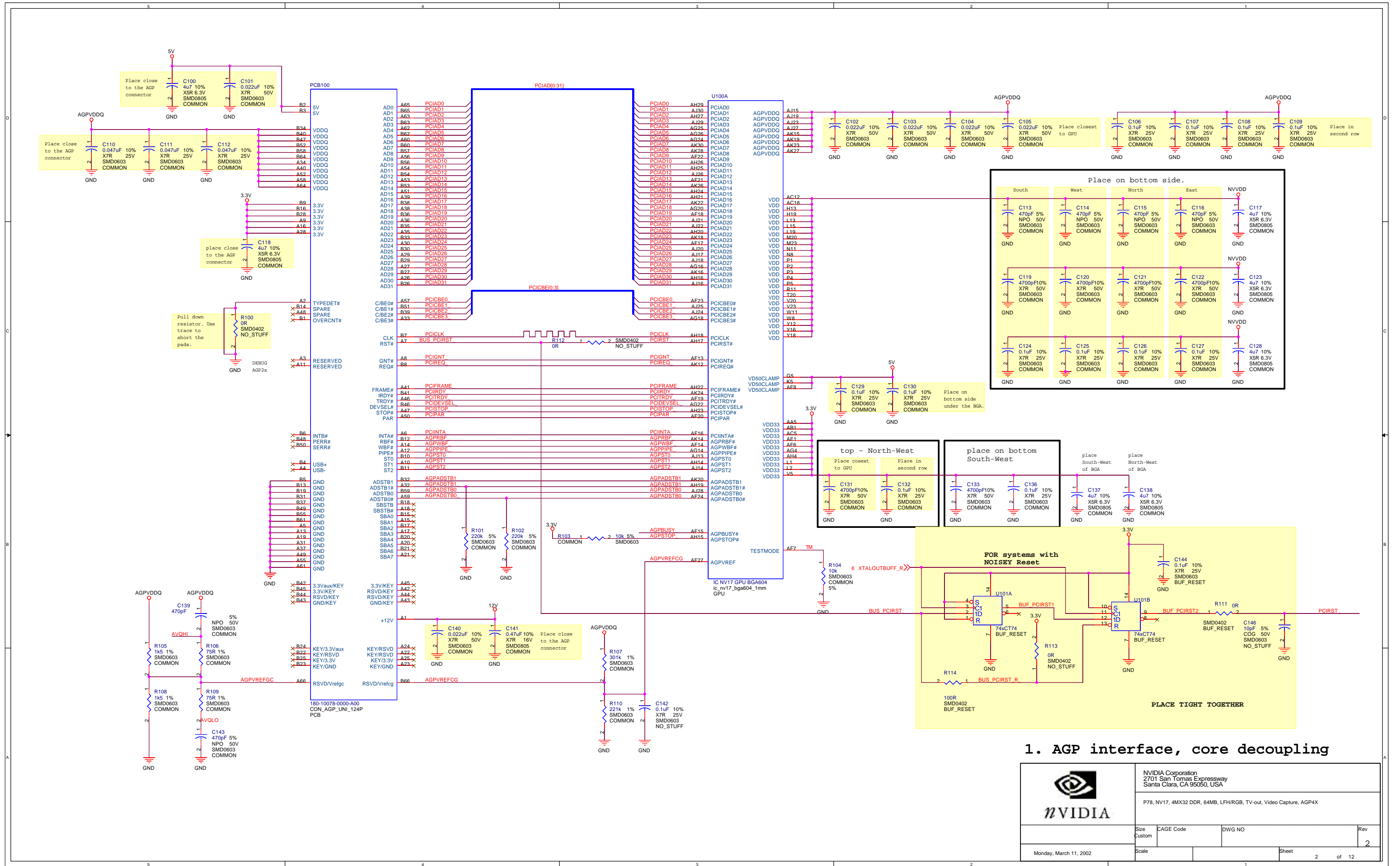
Stuff Option	Meaning
COMMON NO STUFF	Common to all assemblies Not present in any assembly
VIDCAP LFH TV TVO VGA1	Video In - Video Out, or Video Capture LFH BOTH CHANNELS, NO TV, NO VIDCAP Second DAC channel goes to Svideo connector as TV Out 4pin DIN for TV Only Filter cap for VGA SKU
1117 1117_ADJ NO_1117	Fixed 1117 linear regulator for A3.3V Adjustable 1117 linear regulator for A3.3V Connect A3.3V to 3.3V. No 1117 regulator.
IFPREG0 IFPREG1 IFPREG3V IFPREG5V ONE_IFPREG IFP03V IFP13V	2.8V FOR IFP0PLLVD FOR LFH 2.8V FOR IFP1PLLVD FOR LFH IFP PLLVDD REGULATORS INPUT 3.3V IFP PLLVDD REGULATORS INPUT 5V COMMON 2.8V REGULATOR FOR IFP0PLLVD AND IFP1PLLVD A3.3V FOR IFP0PLLVD, DON'T USE IFPREG0, FOR TV A3.3V FOR IFP1PLLVD, DON'T USE IFPREG1, FOR TV
NV17-128D	STRAP OPTION 0X171
CLAMP1 RGB_PROT CLAMP2 RGB2_PROT CLAMP3 TVCLAMP	VGA1 Sync/I2C Clamping diodes RGB Protection diodes on primary DAC outputs VGA2 Sync/I2C Clamping diodes RGB Protection diodes on secondary DAC outputs VIDCAP I2C/Video In Clamping diodes TV Red/Green Clamping diodes
GPU NV17-128D MEMORY M2-8V M2-5V BUF_RESET	GPU ONLY IDSTRAP OPTION-171H Memory only Memory & PS output 2.8V Memory & PS output 2.5V PCIRST through D-FF circuit

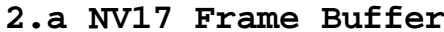
VIDEO CAPTURE USING SAA7113 IS NOT SUPPORTED IN P78

REFER BOM FOR CORRECT NVPNs

140-10078-0000-A01
602-10078-0000-A01

	NVIDIA Corporation 3535 Monroe St Santa Clara, CA 95051, USA			
	P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X			
	Size Custom	CAGE Code	DWG NO	Rev 17
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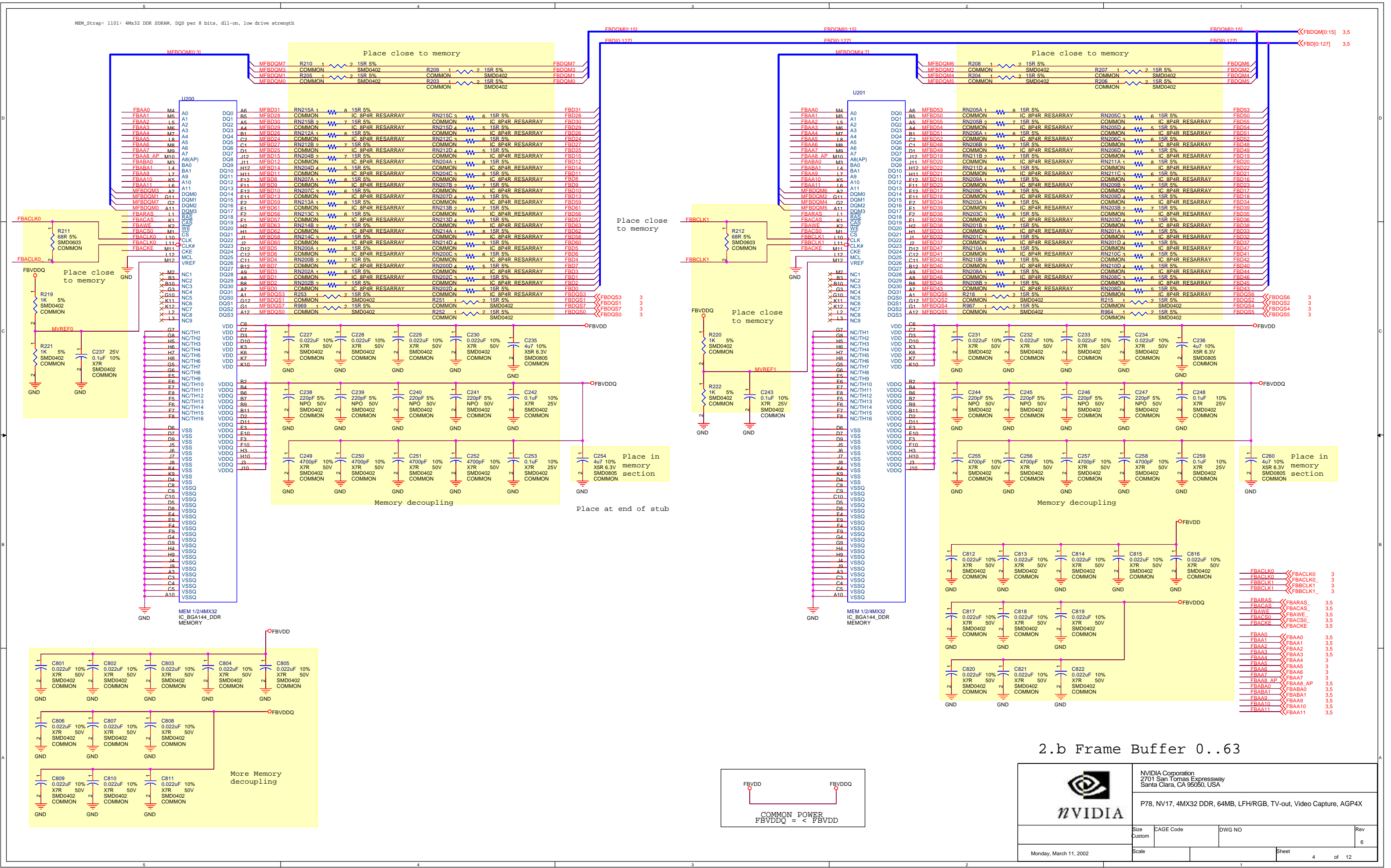


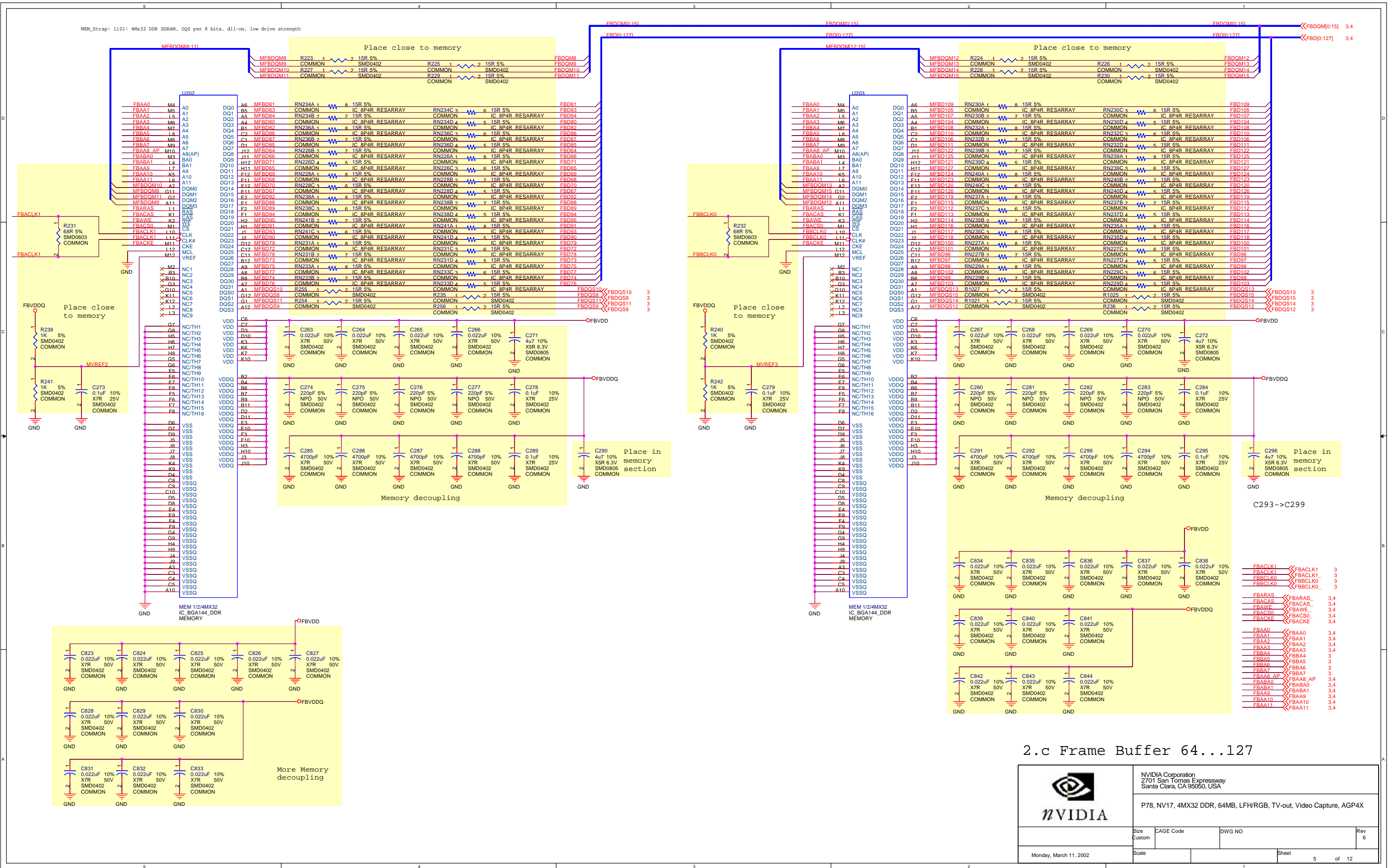


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P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X

	Size Custom	CAGE Code	DWG NO	Rev 01
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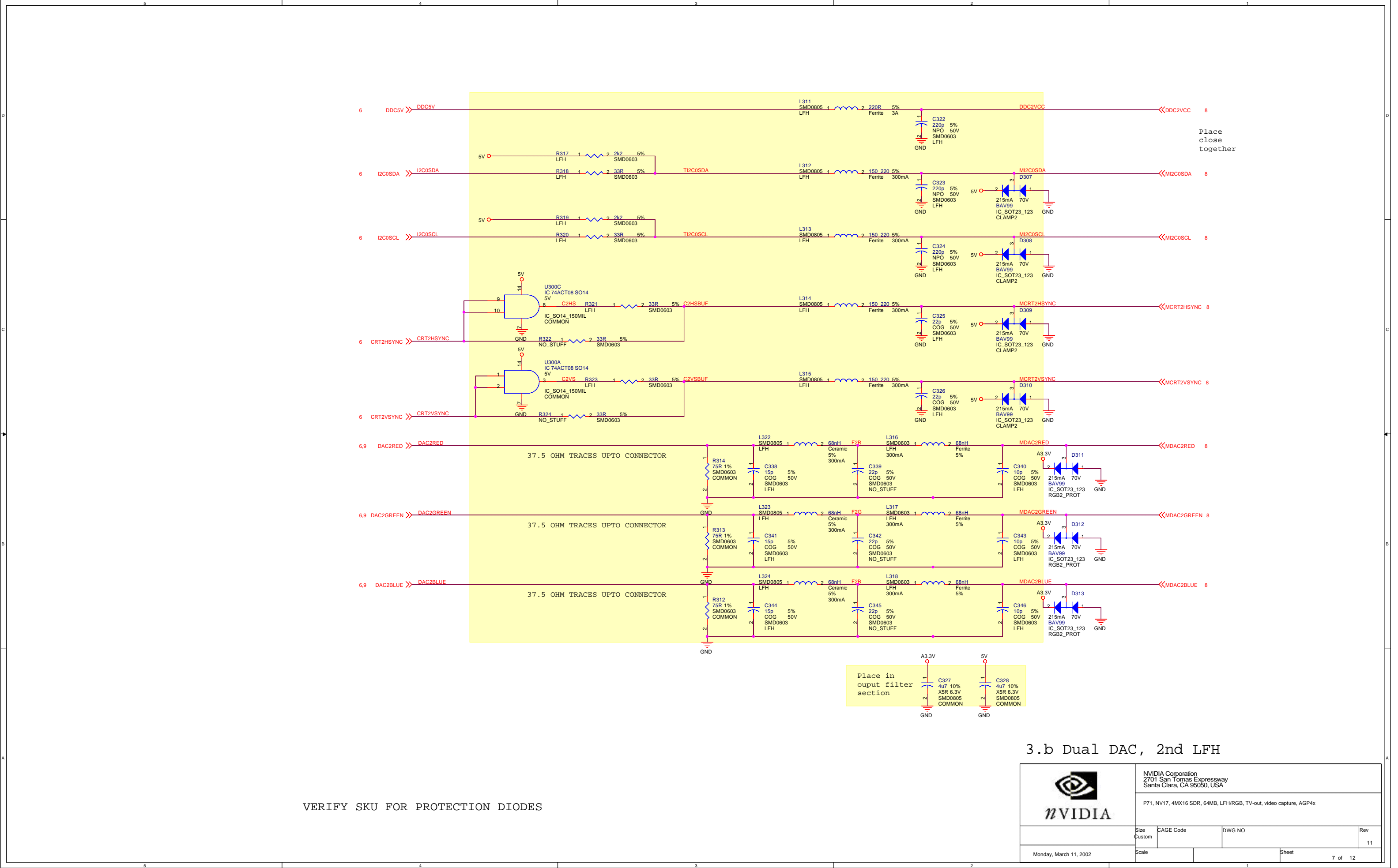


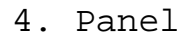




P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X

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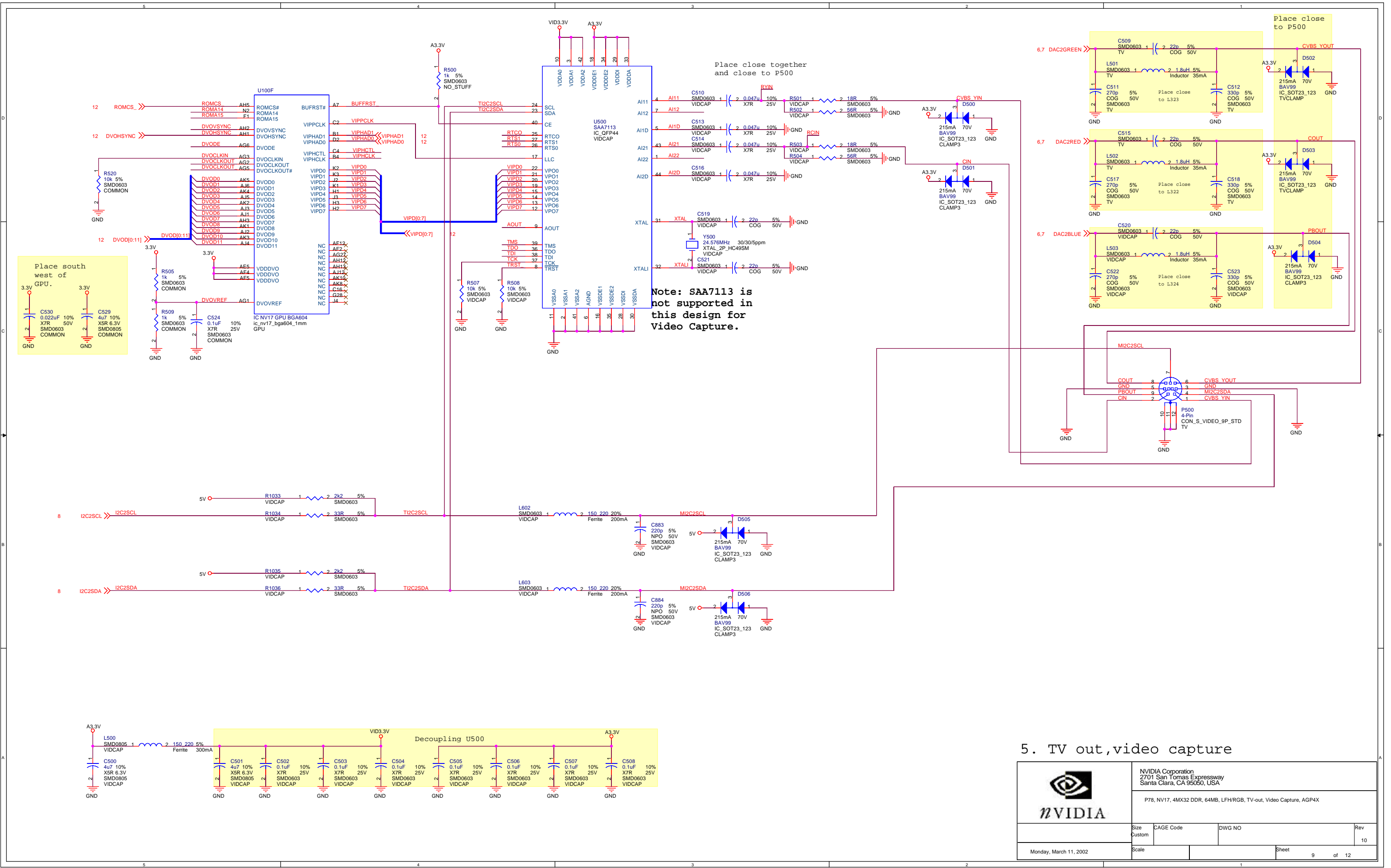




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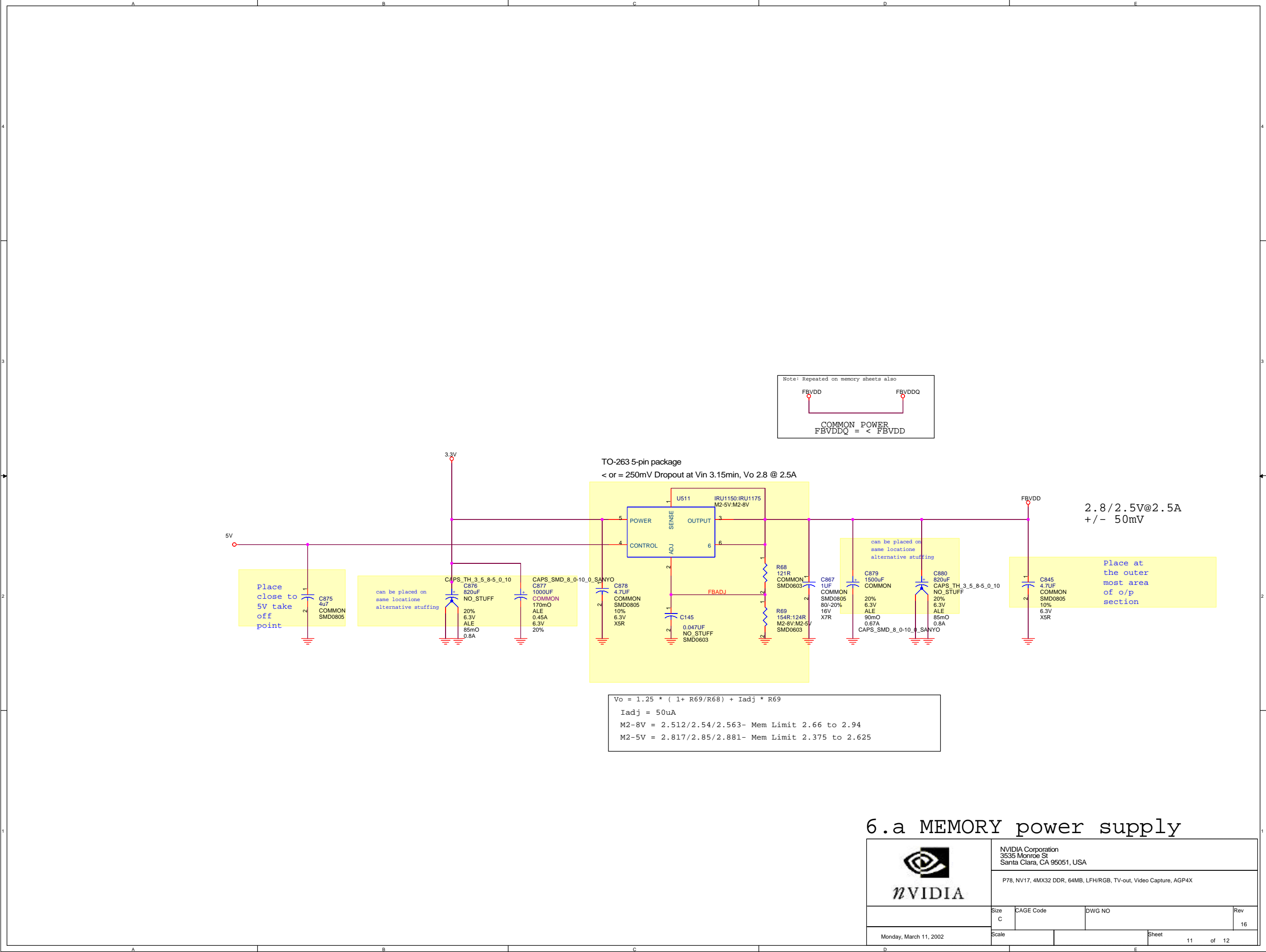
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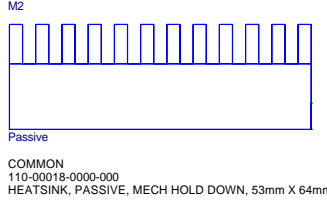
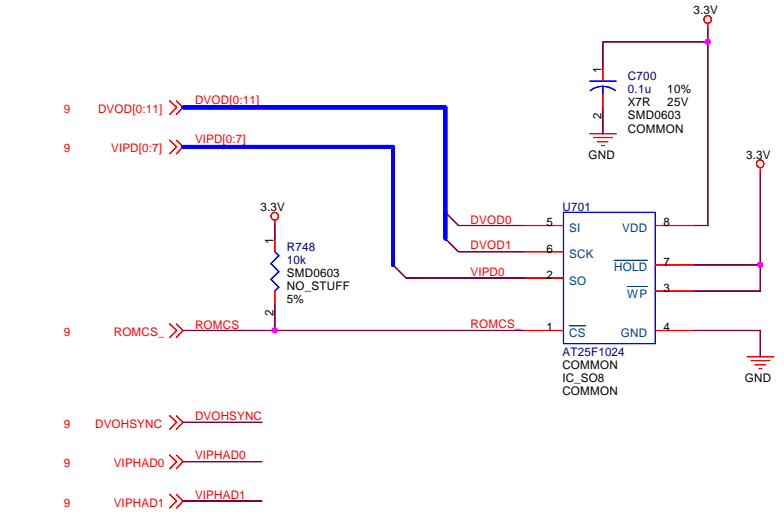
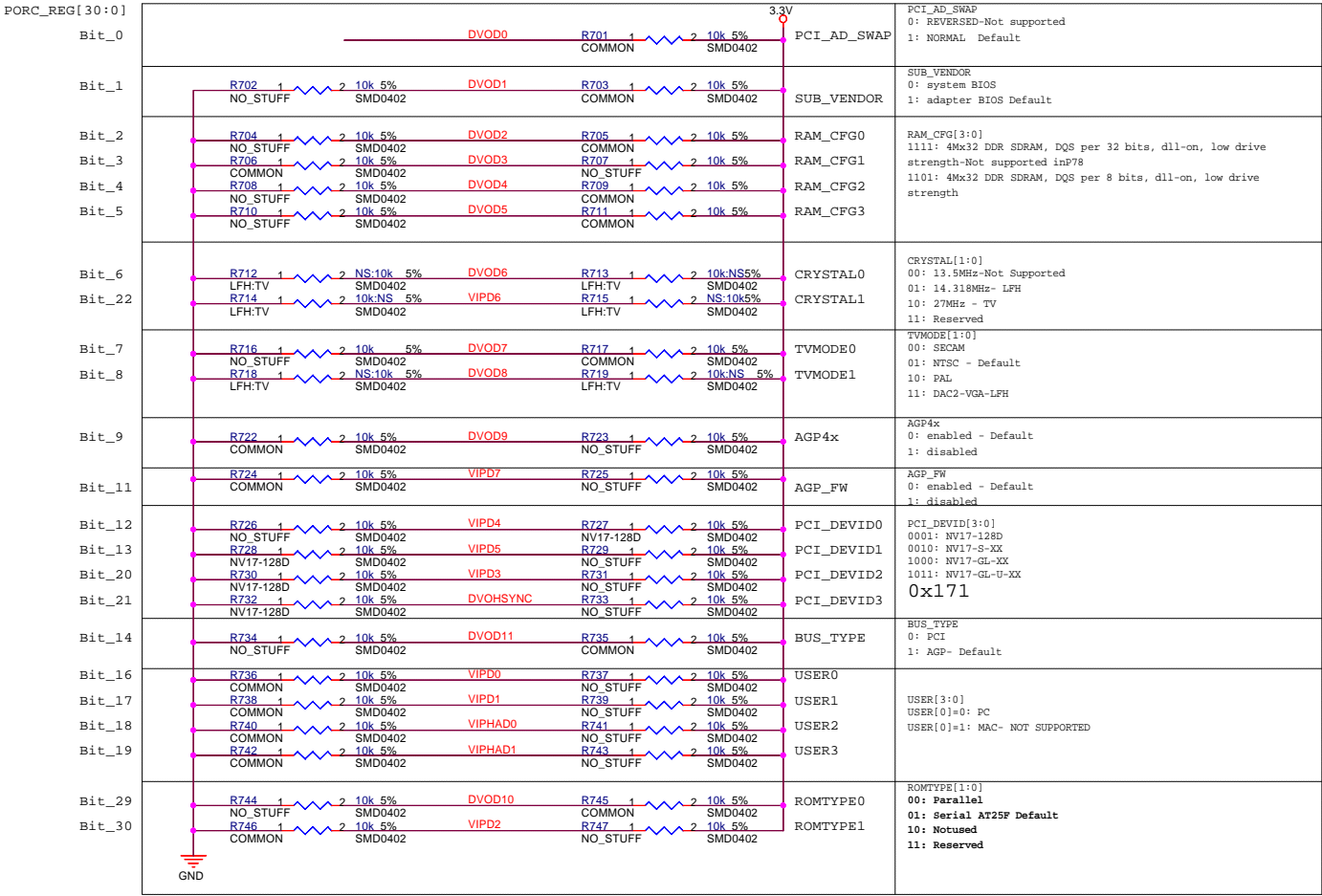
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5. TV out,video capture

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7. BIOS, Strapping

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	Scale		Rev 17
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