<Variant Name>

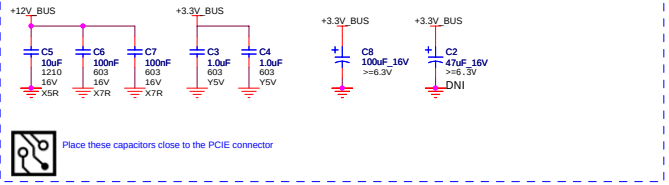
Title	Schematic No.	Date:
PCIE RV370 64-bit 32/64MB BGA DI-VO-V LS	105-A628XX-00A	**Friday, January 28, 2005**

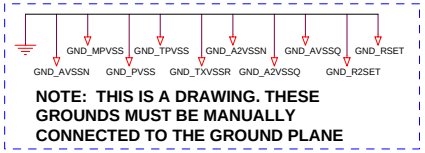
REVISION HISTORY

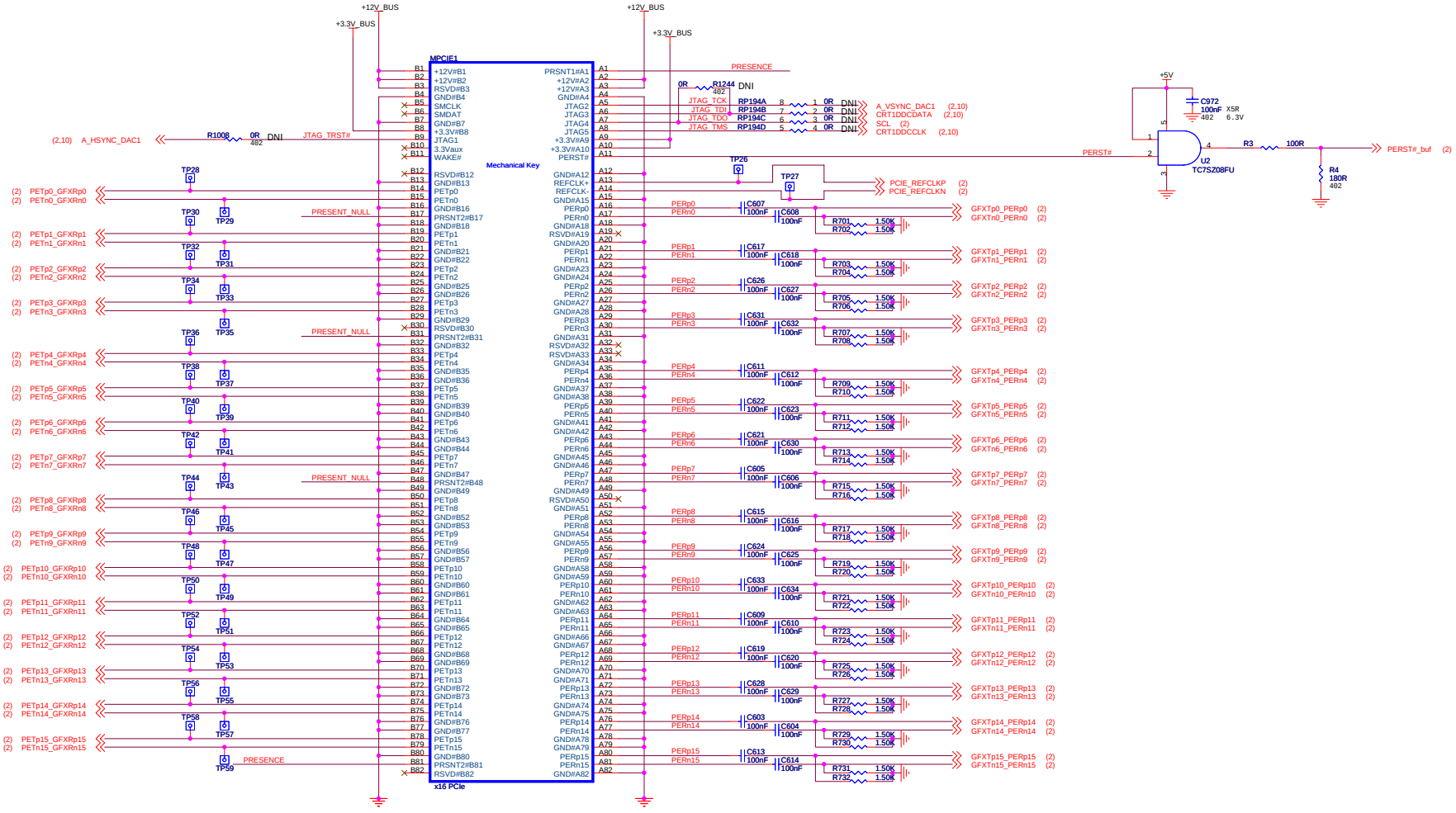
Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	2005-01-07	PRELIMINARY BASED ON 105-A53300-00A

PCI-EXPRESS EDGE CONNECTOR







SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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(905) 882-2600

Title	PCIE RV370 64-bit 32/64MB BGA DI-VO-V LS		
Size C	Document Number 105-A628XX-00A		Rev 0
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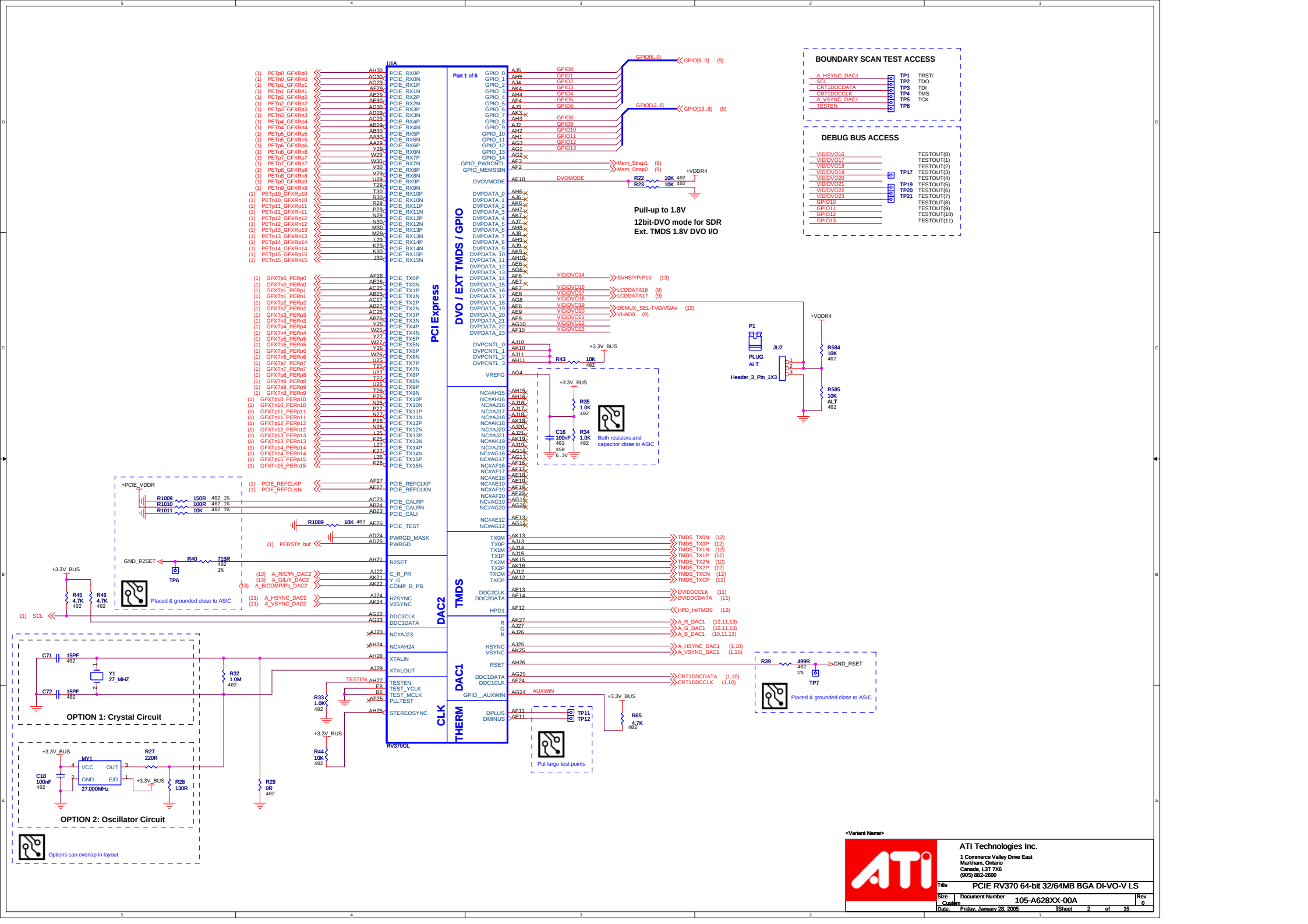
U1A
Part 1 of 6
PCI Express
DVO / EXT TMDS / GPIO
TMDS
DAC2
DAC1
CLK
THERM
RV370GL
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CALRP
PCIE_CALRN
PCIE_CALI
PCIE_TEST
PWRGD_MASK
PWRGD
R2SET
C_R_PR
Y_G
COMP_B_PB
H2SYNC
V2SYNC
DDC3CLK
DDC3DATA
NC#AJ23
NC#AH24
XTALIN
XTALOUT
TESTEN
TEST_YCLK
TEST_MCLK
PLLTEST
STEREOSYNC
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_PWRCNTL
GPIO_MEMSSIN
DVOVMODE
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_3
VREFG
NC#AH15
NC#AH16
NC#AJ16
NC#AJ17
NC#AJ18
NC#AK18
NC#AJ20
NC#AJ21
NC#AK19
NC#AJ19
NC#AG16
NC#AG17
NC#AF16
NC#AF17
NC#AE18
NC#AE19
NC#AF19
NC#AF20
NC#AG19
NC#AG20
NC#AE12
NC#AG12
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TXCM
TXCP
DDC2CLK
DDC2DATA
HPD1
R
G
B
HSYNC
VSYNC
RSET
DDC1DATA
DDC1CLK
GPIO__AUXWIN
DPLUS
DMINUS
GPIO[6..0]
GPIO[13..8]
Mem_Strap1 (9)
Mem_Strap0 (9)
DVOMODE
R22 10K 402
R23 10K 402
+VDDR4
Pull-up to 1.8V
12bit-DVO mode for SDR
Ext. TMDS 1.8V DVO I/O
VID/DVO14
VID/DVO16
VID/DVO17
VID/DVO18
VID/DVO19
VID/DVO20
VID/DVO21
VID/DVO22
VID/DVO23
SVHS/YPrPbb (13)
LCDDATA16 (9)
LCDDATA17 (9)
DEMUX_SEL-TVO/VGA# (13)
VHAD0 (9)
R43 10K 402
+3.3V_BUS
R35 1.0K 402
C16 100nF 402 X5R 6.3V
R34 1.0K 402
Both resistors and capacitor close to ASIC
P1
PLUG ALT
JU2
Header_3_Pin_1X3
R584 10K 402
R585 10K ALT 402
TMDS_TX0N (12)
TMDS_TX0P (12)
TMDS_TX1N (12)
TMDS_TX1P (12)
TMDS_TX2N (12)
TMDS_TX2P (12)
TMDS_TXCN (12)
TMDS_TXCP (12)
DVIDDCCLK (11)
DVIDDCDATA (11)
HPD_IntTMDS (12)
A_R_DAC1 (10,11,13)
A_G_DAC1 (10,11,13)
A_B_DAC1 (10,11,13)
A_HSYNC_DAC1 (1,10)
A_VSYNC_DAC1 (1,10)
CRT1DDCDATA (1,10)
CRT1DDCCLK (1,10)
AUXWIN
R65 4.7K 402
TP11
TP12
Put large test points
R39 499R 402 1%
GND_RSET
TP7
Placed & grounded close to ASIC
BOUNDARY SCAN TEST ACCESS
A_HSYNC_DAC1
SCL
CRT1DDCDATA
CRT1DDCCLK
A_VSYNC_DAC1
TESTEN
TP1 TRST/
TP2 TDO
TP3 TDI
TP4 TMS
TP5 TCK
TP8
DEBUG BUS ACCESS
VID/DVO16
VID/DVO17
VID/DVO18
VID/DVO19
VID/DVO20
VID/DVO21
VID/DVO22
VID/DVO23
GPIO10
GPIO11
GPIO12
GPIO13
TP17
TP19
TP20
TP21
TESTOUT(0)
TESTOUT(1)
TESTOUT(2)
TESTOUT(3)
TESTOUT(4)
TESTOUT(5)
TESTOUT(6)
TESTOUT(7)
TESTOUT(8)
TESTOUT(9)
TESTOUT(10)
TESTOUT(11)
+PCIE_VDDR
R1009 150R 402 1%
R1010 100R 402 1%
R1011 10K 402 1%
R1089 10K 402
PERST#_buf
GND_R2SET
R40 715R 402 1%
TP6
Placed & grounded close to ASIC
A_R/C/Pr_DAC2
A_G/L/Y_DAC2
A_B/COMP/Pb_DAC2
A_HSYNC_DAC2
A_VSYNC_DAC2
SCL
R45 4.7K 402
R46 4.7K 402
C71 15PF 402
C72 15PF 402
Y1 27_MHZ
R32 1.0M 402
OPTION 1: Crystal Circuit
MY1
VCC
OUT
GND
E/D
27.000MHz
C18 100nF 402
R27 220R
R28 130R
R29 0R 402
OPTION 2: Oscillator Circuit
Options can overlap in layout
TESTEN
R33 1.0K 402
R44 10K 402
<Variant Name>
ATI Technologies Inc.
1 Commerce Valley Drive East
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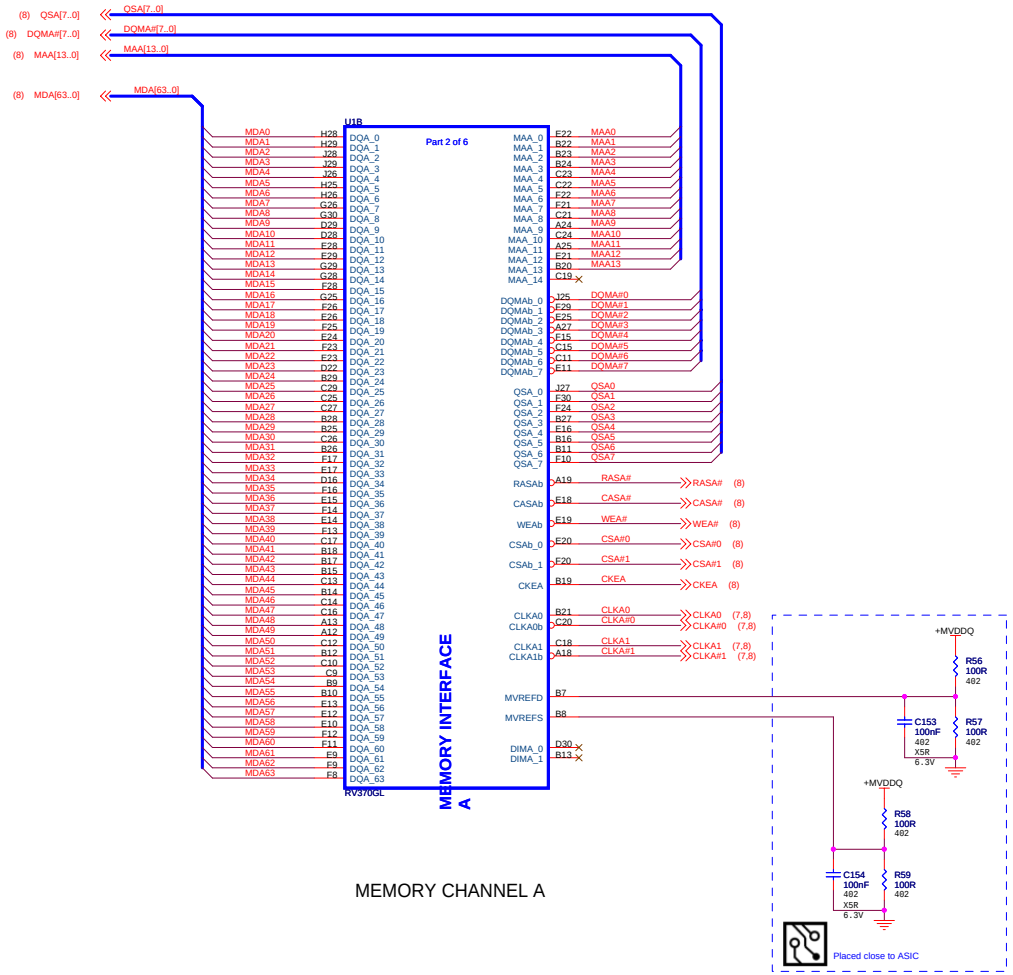
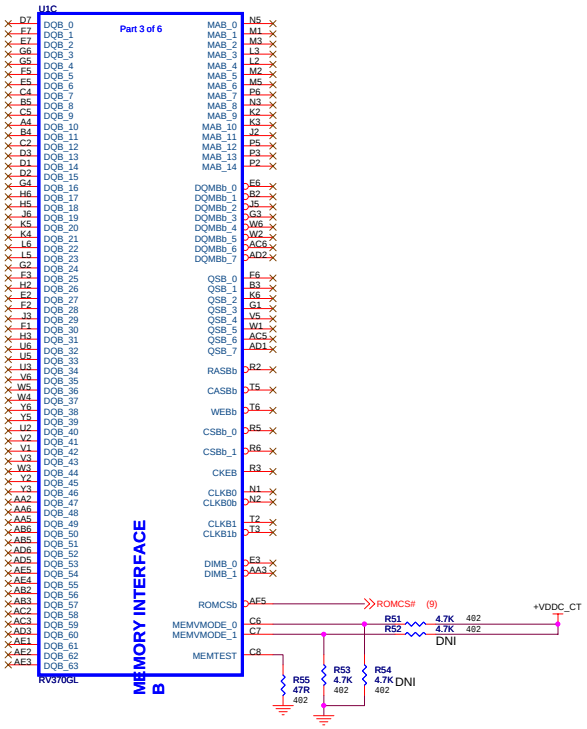
(905) 882-2600
Title
PCIE RV370 64-bit 32/64MB BGA DI-VO-V LS
Size Custom
Document Number 105-A628XX-00A
Rev 0
Date: Friday, January 28, 2005
Sheet 2 of 15



MEMORY CHANNEL A



MEMORY CHANNEL B

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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Size: Custom	Document Number: 105-A628XX-00A	Rev: 0
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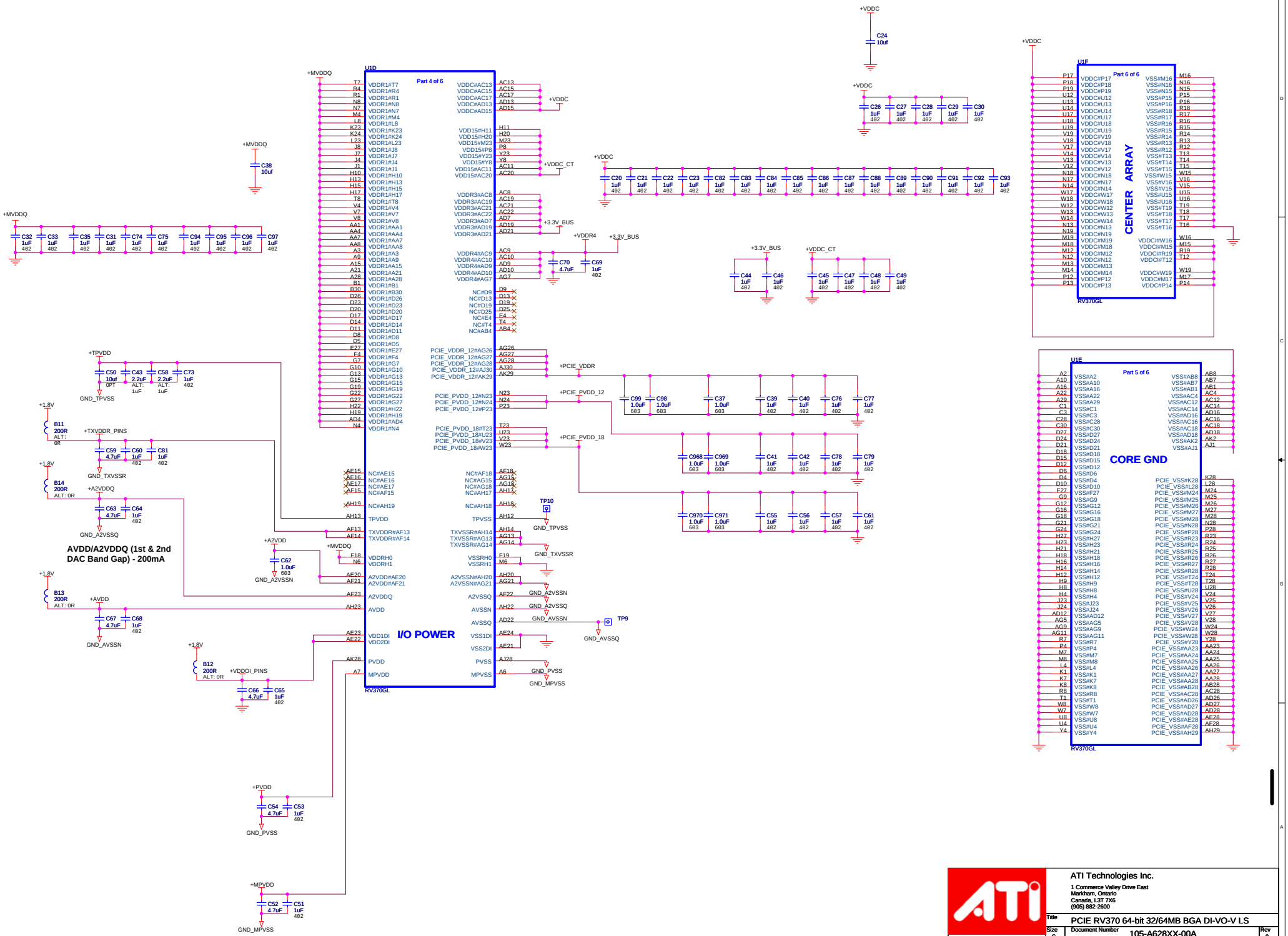
U1D
Part 4 of 6
I/O POWER
RV370GL
U1F
Part 6 of 6
CENTER ARRAY
RV370GL
U1E
Part 5 of 6
CORE GND
RV370GL
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
+MVDDQ
+VDDC
+VDDC_CT
+3.3V_BUS
+VDDR4
+PCIE_VDDR
+PCIE_PVDD_12
+PCIE_PVDD_18
+TPVDD
+TXVDDR_PINS
+A2VDDQ
+AVDD
+VDDOI_PINS
+PVDD
+MPVDD
GND_TPVSS
GND_TXVSSR
GND_A2VSSQ
GND_A2VSSN
GND_AVSSN
GND_AVSSQ
GND_PVSS
GND_MPVSS
TP10
TP9
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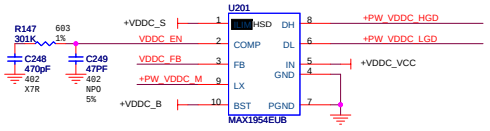
Regulator for VDDC (ASIC Core)

Vout = 1.2V ~ 1.3V

Part	Vout	R1	R2
0.8V Ref	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
	1.25V	1.00K 1% ATI P/N 3240100100	1.78K 1% ATI P/N 3240178100
	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100

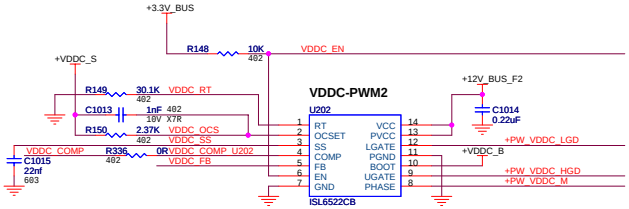
VDDC-PWM1



MAXIM MAX1954

MAXIM MAX1954A

VDDC-PWM2



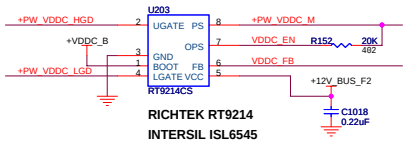
INTERSIL ISL6522

RICHTEK RT9232A

ANPEC APW7062A

ANPEC APW7062B

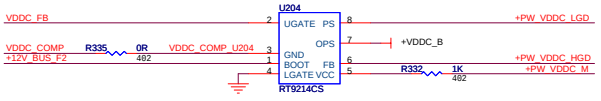
VDDC-PWM3



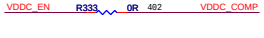
RICHTEK RT9214

INTERSIL ISL6545

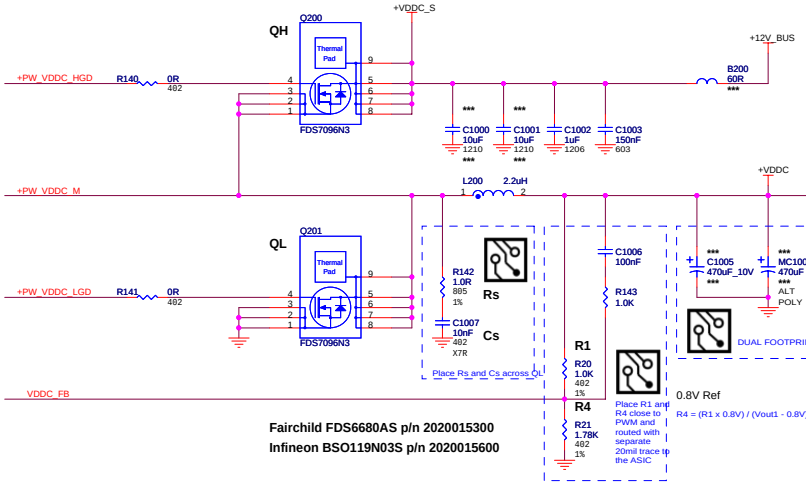
VDDC-PWM4



ANPEC APW7061



QH / QL



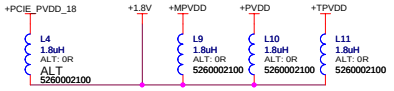
Fairchild FDS6680AS p/n 2020015300

Infineon BSO119N03S p/n 2020015600

+PCIE_VDDR: 1.2V 1300mA MAX

+PCIE_PVDD_12: 1.2V 100mA MAX

+MPVDD: 10mA MAX
+PVDD: 25mA MAX
+TPVDD: 50mA MAX



Rails derived from +1.8V

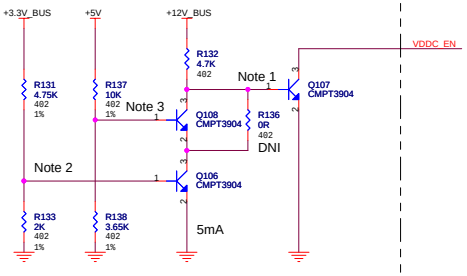
+AVDD: 10mA MAX

+A2VDDQ: 20mA MAX

+VDDOI_PINS: 20mA MAX

+TXVDDR_PINS: 20mA MAX

POWER SEQUENCING



Power Sequence Circuit to ensure SMPS_EN is released after +12V and +3.3V are both in regulation.

Note 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Note 2 When +3.3V gets closed to regulation, one of the two conditions of releasing SMPS_EN is active

Target for 920mV when +3.3 at min regulation (worse case)

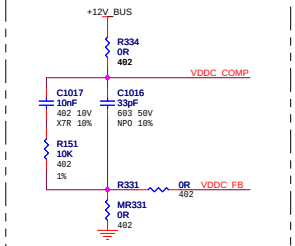
Typical trigger when +3.3V ramps above 2.2V (650mV)

Note 3 When +5V (derived from +12V) gets closed to regulation, one of the two conditions of releasing SMPS_EN is active

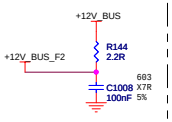
Target for 1.2V when +5 at min regulation (worse case)

Typical trigger when +5V ramps above 3.2V (850mV)

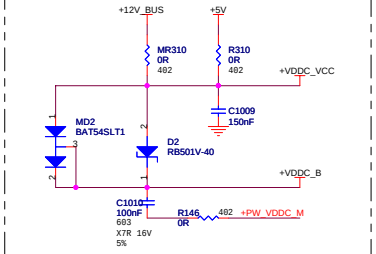
COMPENSATION CIRCUIT



FILTERED +12V_BUS



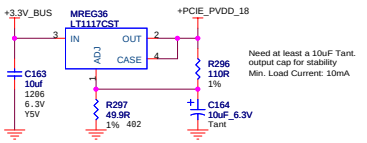
BOOT CIRCUIT



Alt. Regulator for PCIE_PVDD_18

Vout = 1.82V

Iout = 500mA MAX



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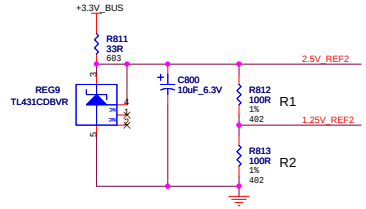
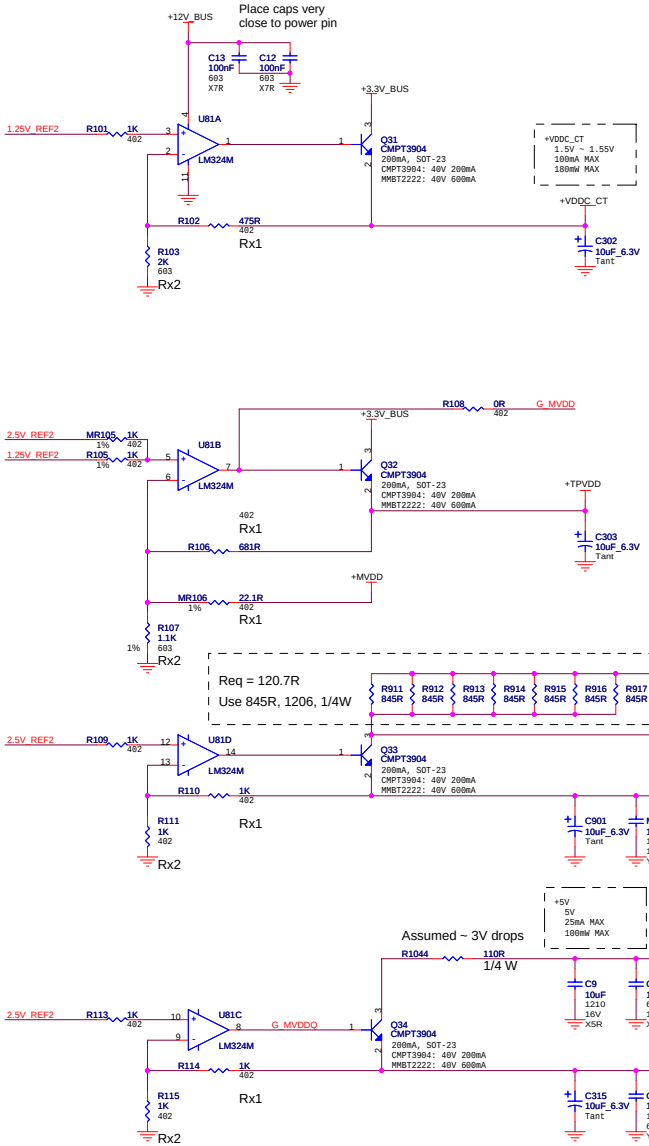
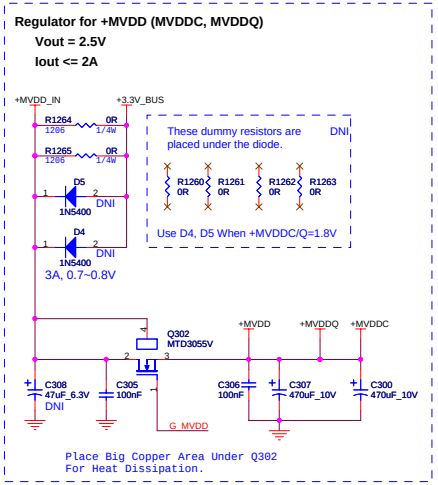


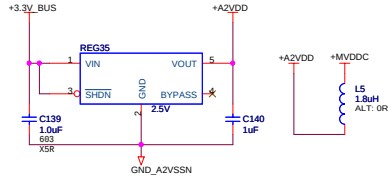
Voltage Req.	R1	R2
0.8V	150R P/N 3160150000 402	71.5R P/N 324075R500
1.25V	100R P/N 3160100000 402	100R P/N 3160100000 402
1.5V	100R P/N 3160100000 402	150R P/N 3160150000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

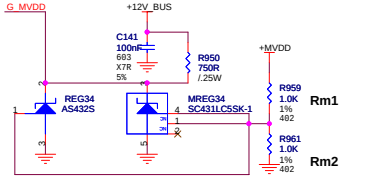
Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.55	475R (402, 1%) P/N 3160475000	2K (1%) P/N 3160200100 (402) P/N 3240200100 (603)
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240150100

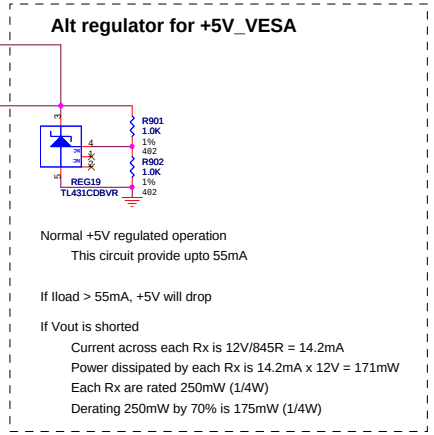
Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.61V	221R (402, 1%) P/N 3160221000	4.99K (402, 1%) P/N 3160499100
2.55V 2.5V Ref	22.1R 316022R100G 402	1,1K 3240110100G 603
2.5V	0R P/N 3230000000 603 P/N 3150000000 402	DNI



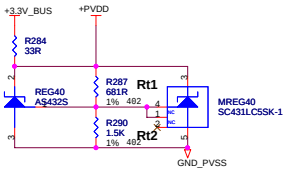


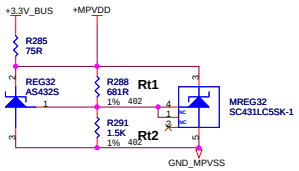


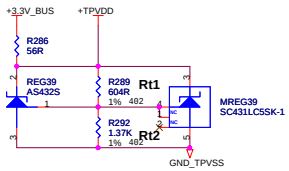


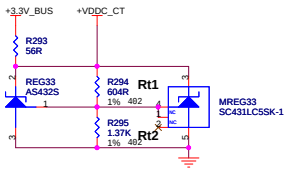


	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100









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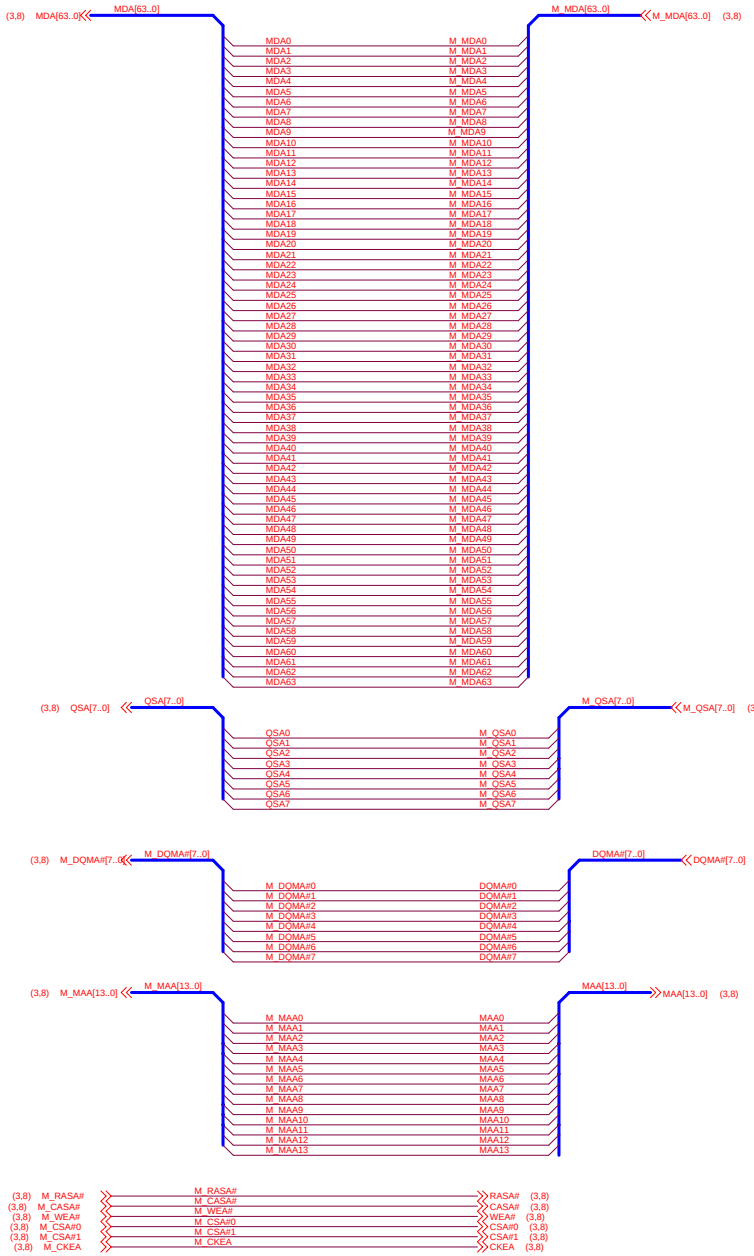
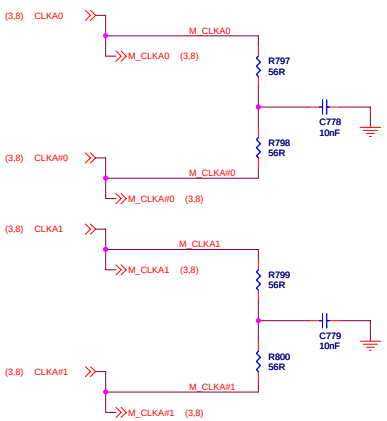


CLOCK terminations



<Variant Name>

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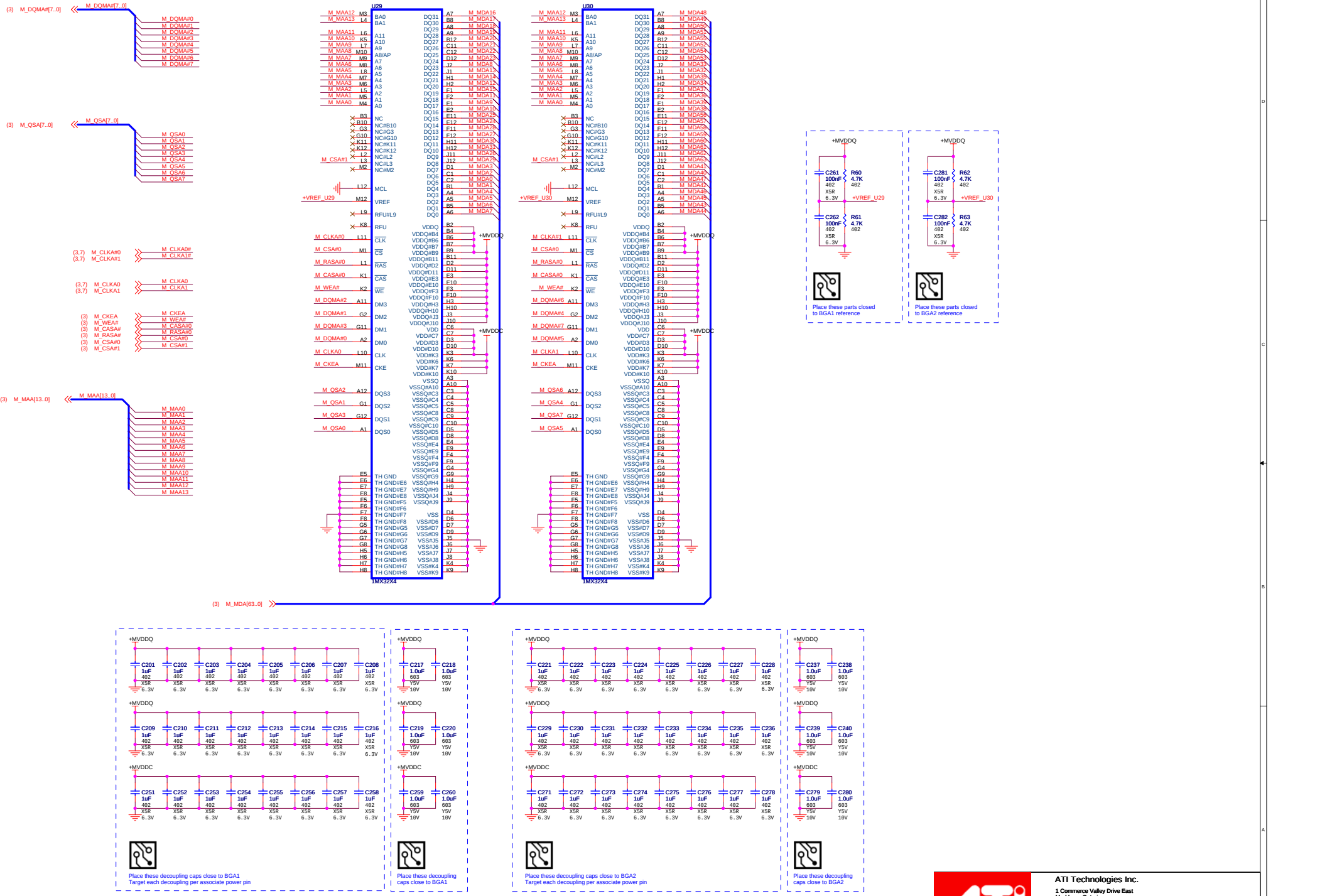

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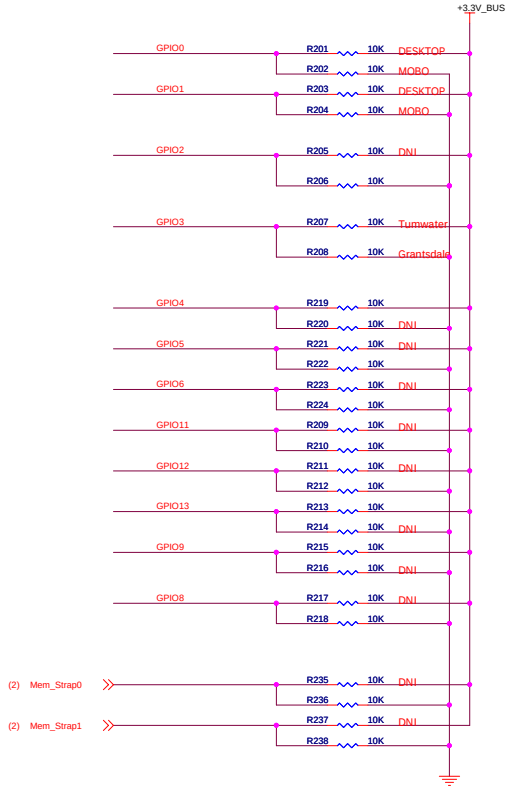
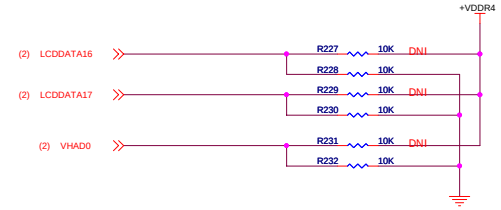
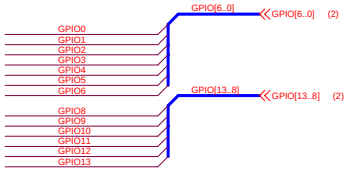
OPTION STRAPS





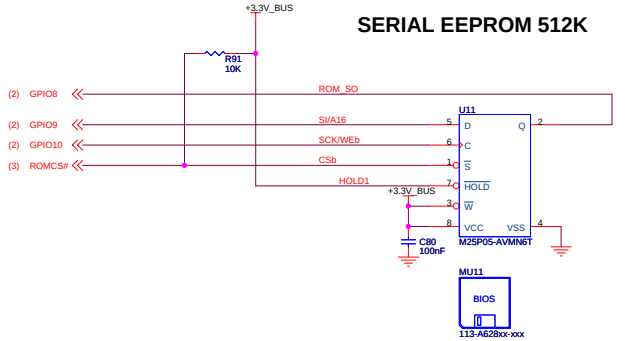


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K



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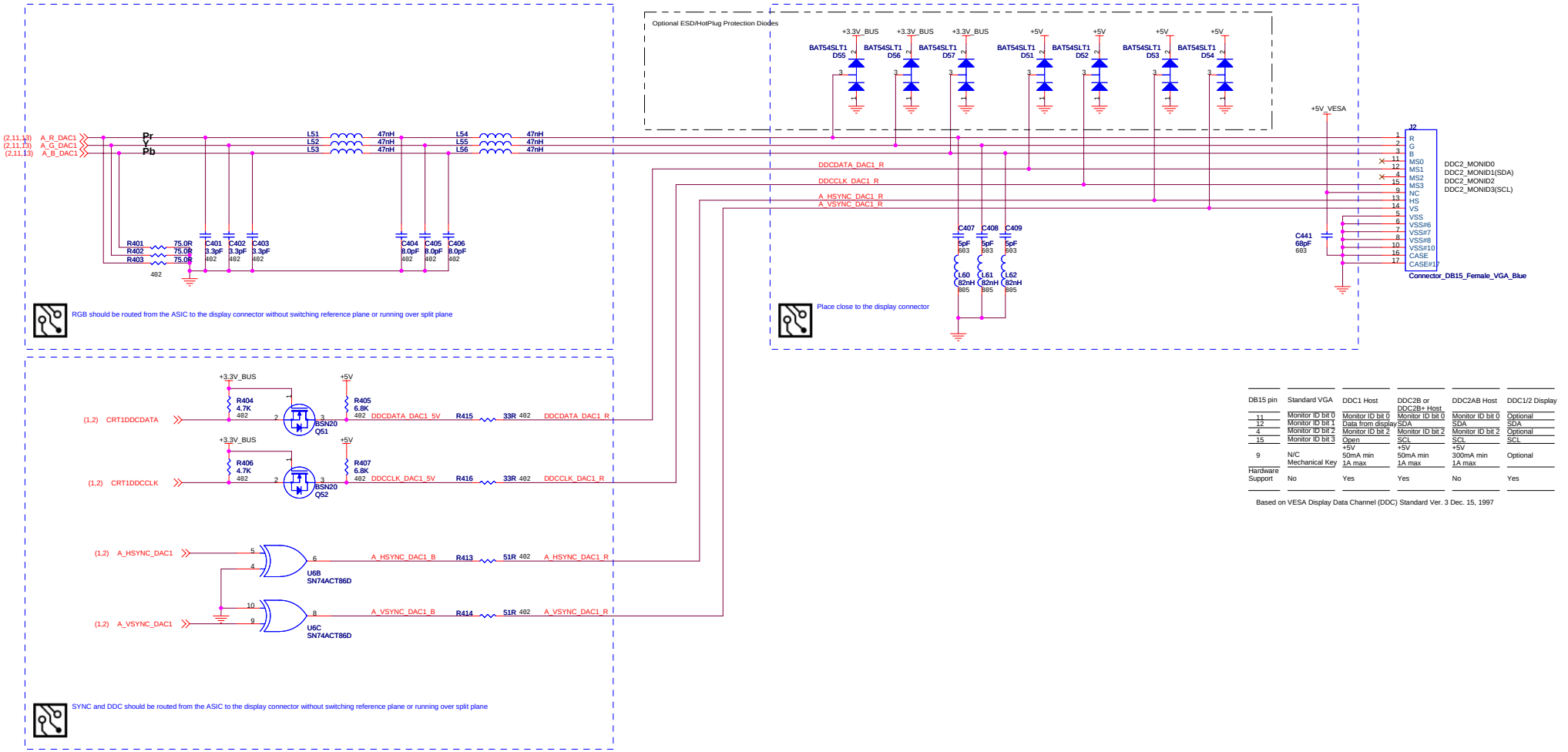

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C Mechanical Key	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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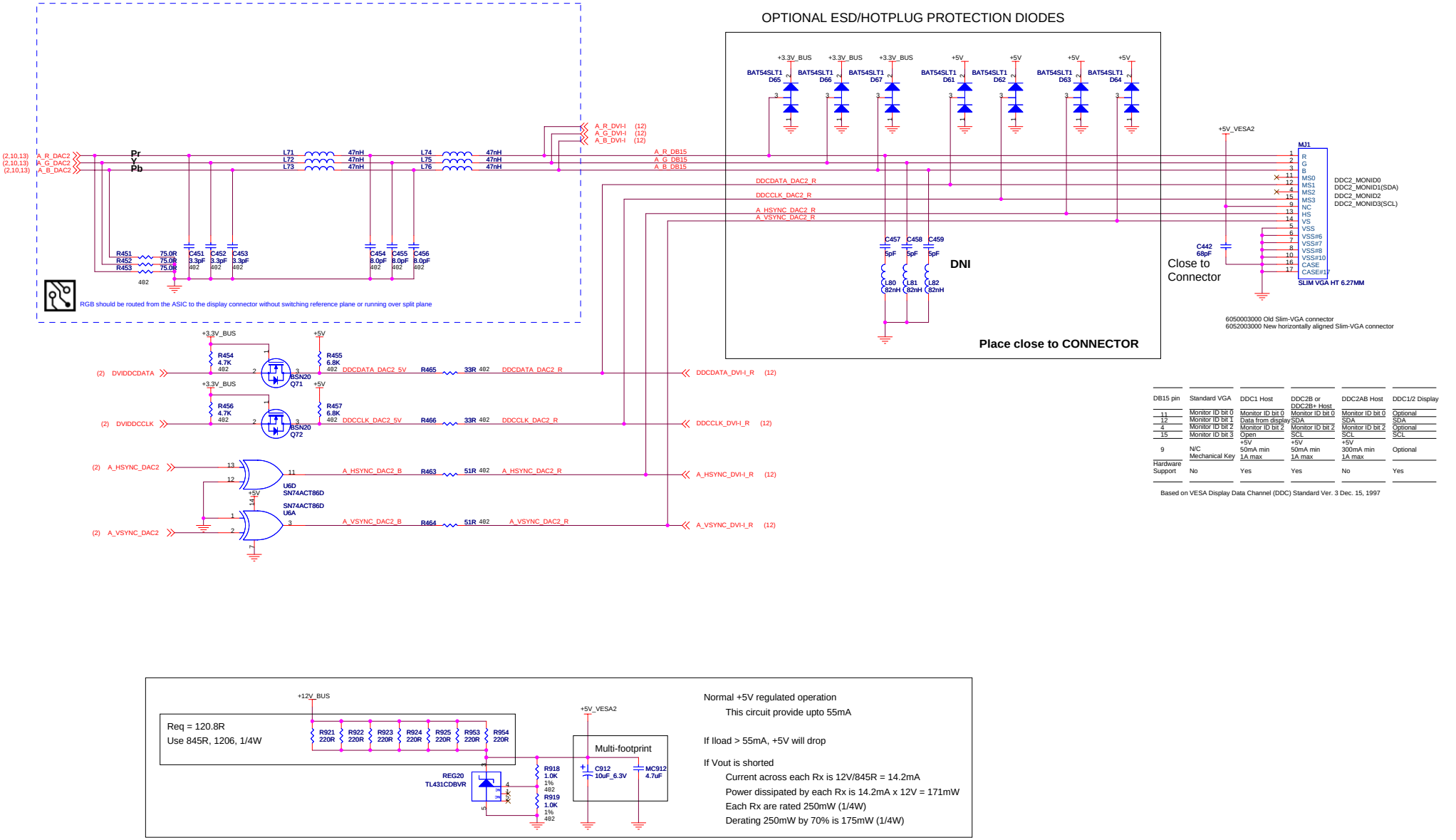

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C Mechanical Key	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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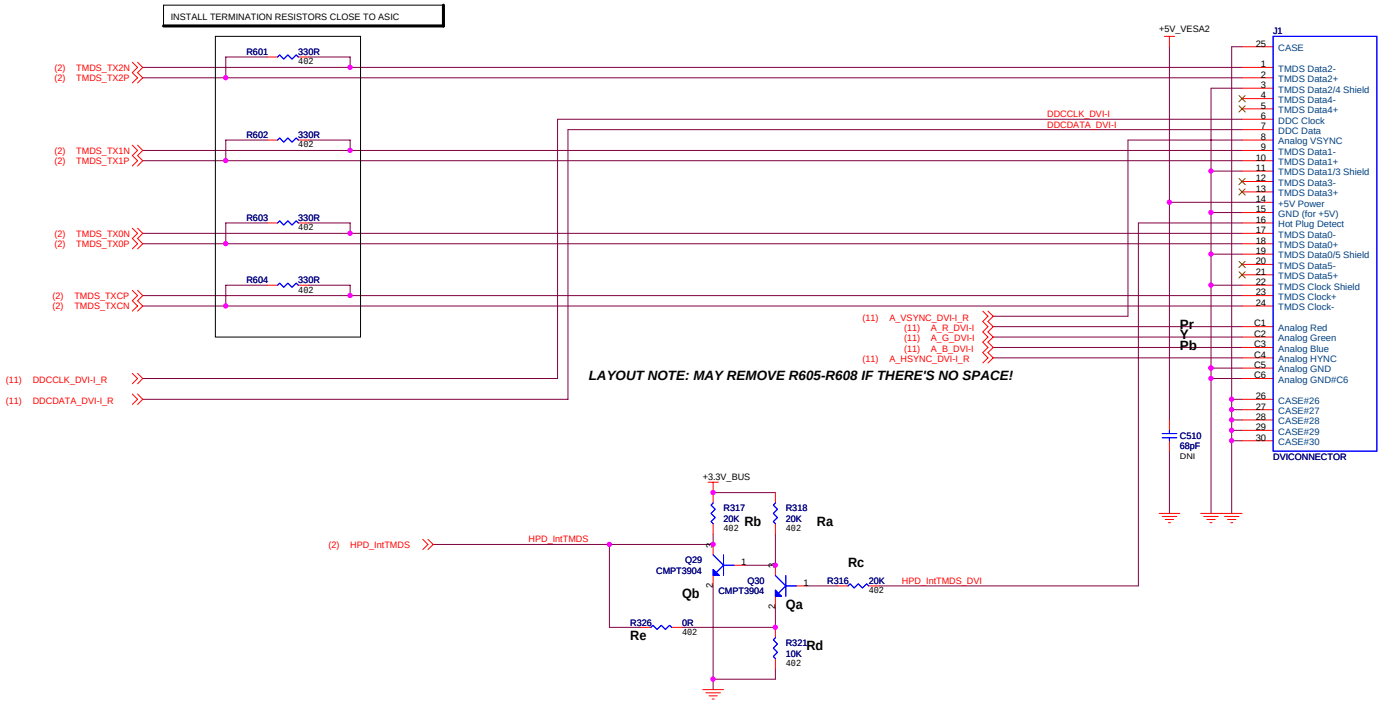
PRIMARY DVI-I CONNECTOR



LAYOUT NOTE: MAY REMOVE R605-R608 IF THERE'S NO SPACE!

STUFFING OPTIONS

Hot-Plug Detect Circuit	MUST INSTALL	MUST NOT INSTALL
Type A	Ra, Rb, Rc, Rd=0R, Qa, Qb	Re
Type B	Ra=0R, Rc, Rd=10K, Re, Qa	Rb, Qb

	HPD_ExtTMDS_DVI	HPD_ExtTMDS Type A	HPD_ExtTMDS Type B
NC	High Z	0 (0V)	0 (0V)
Connected	5V	1 (3.3V)	1 (3.3V)

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From DAC2

DAC2 DeMux

R / C / Pr
G / L / Y
B / COMP / Pb

(2) A_R/C/Pr_DAC2
(2) A_G/L/Y_DAC2
(2) A_B/COMP/Pb_DAC2

A_R/C/Pr_DAC2
A_G/L/Y_DAC2
A_B/COMP/Pb_DAC2

+3.3V_BUS
R582 10K 402
(2) DEMUX_SEL-TVO/VGA#

+5V
C168 1uF 402

U96
PI5V330
SEL, 1A0, 1A1, 1B0, 1B1, 1C0, 1C1, E, VCC, YA, YB, YC, YD, 1D1, 1D0, GND

To VGA Filters

A_R_DAC2
A_G_DAC2
A_B_DAC2
A_R_DAC2 (2,10,11)
A_G_DAC2 (2,10,11)
A_B_DAC2 (2,10,11)
R
G
B

To TVO filters

A_C/Pr_DAC2
A_L/Y_DAC2
A_COMP/Pb_DAC2
C / Pr
L / Y
COMP / Pb

DAC2 DeMux BYPASS

R / C / Pr — A_R/C/Pr_DAC2 — 0R R928 402 — A_R_DAC2 — R / Pr
G / L / Y — A_G/L/Y_DAC2 — 0R R929 402 — A_G_DAC2 — G / Y
B / COMP / Pb — A_B/COMP/Pb_DAC2 — 0R R930 402 — A_B_DAC2 — B / Pb

0R R970 402 — A_C/Pr_DAC2 — C / Pr
0R R971 402 — A_L/Y_DAC2 — L / Y
0R R972 402 — A_COMP/Pb_DAC2 — COMP / Pb

Place Resistors close to ASIC.

A_L/Y_DAC2 — L91 .47uH — R504 75.0R 402 — C501 47PF 402 — C502 47PF 402
A_C/Pr_DAC2 — L92 .47uH — R505 75.0R 402 — C503 47PF 402 — C504 47PF 402
A_COMP/Pb_DAC2 — L93 .47uH — R506 75.0R 402 — C505 47PF 402 — C506 47PF 402

Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI

A_L_DAC2_F — R519 0R 402 — A_L_DAC2_DIN
A_C_DAC2_F — R520 0R 402 — A_C_DAC2_DIN
A_COMP_DAC2_F — R521 0R 402 — A_COMP_DAC2_DIN

C507 82pF 402
C508 82pF 402
C509 82pF 402
R515 0R

TV Out (SVHS)

+3.3V_BUS
R578 10K 402
(2) SVHS/YPrPbb — R377 0R 402 — PIN6
PIN7
PIN5

J6
Connector_DIN_Miniature_Circular_7_Pin
+12V
Y-OUT
C-OUT
Comp_out
SYNC
GND
GND#2
CASE
CASE#9
CASE#10

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500
- 4-pin Svideo MiniDIN P/N 6070001000

PIN7 — MJ6 Jack_Phono_RCA

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DVI/VGA SCREWS

ASSY1
SCREW
JACKSCREW

ASSY2
SCREW
JACKSCREW

ASSY15
SCREW
JACKSCREW

ASSY16
SCREW
JACKSCREW

Bracket Screws

ASSY3
SCREW
PAN_HEAD

MISC. BOARD PARTS

ASSY7
ANTISTATIC BAG
6_X_11
9040000900

ASSY6
ANTISTATIC BAG
6_X_11
9040000900

ASSY8
BLANK LABEL
9050005900

ASSY9
LABEL
2" X 0.25"
9050004600

ASSY5
ATI LOGO LABEL
ATI_LOGO_LABEL
9110054500

ASSY10
ATI LOGO LABEL
ATI_LOGO_LABEL
9110054500

+12V_BUS

JU1

H101
heatsink
7120005800

H100
HEATSINK
7120005100

Spring push-pin

MH101
HEATSINK
7120002700

MH100
HEATSINK
7120008000

ITW push-pin

MT1
MT_Hole_0.136_in.

ATX Brackets

ASSY14
BRACKET
DVI, DIN, VGA
8020037000

ASSY12
BRACKET
VGA, DIN, VGA
8020037100

ASSY11
BRACKET
DVI, VGA
80200370A0

ASSY13
BRACKET
80200371A0

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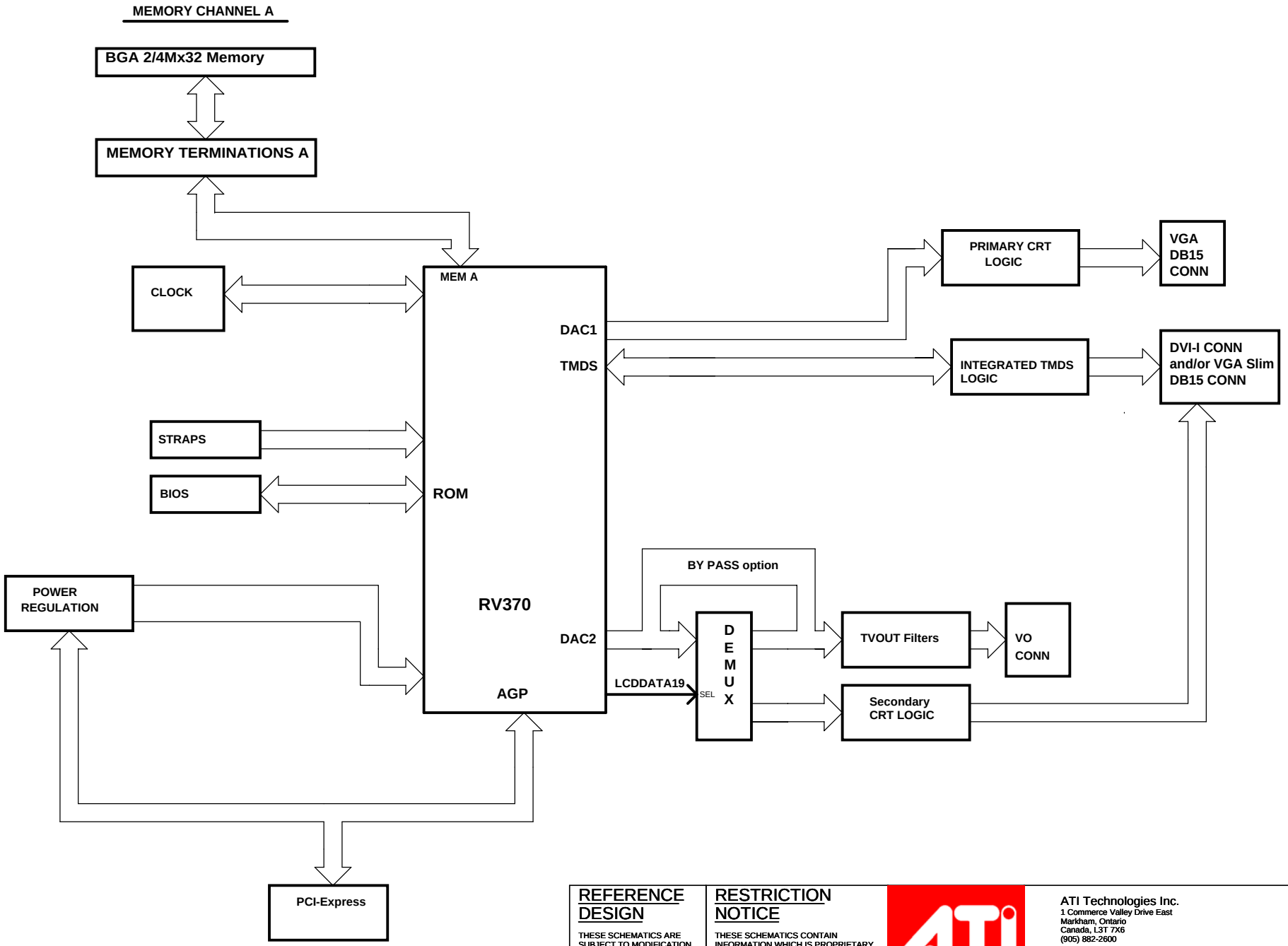

REFERENCE DESIGN

THESE SCHEMATICS ARE SUBJECT TO MODIFICATION AND DESIGN IMPROVEMENTS. PLEASE CONTACT ATI FIELD APPLICATION ENGINEERING BEFORE USING THE INFORMATION CONTAINED HEREIN.

RESTRICTION NOTICE

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