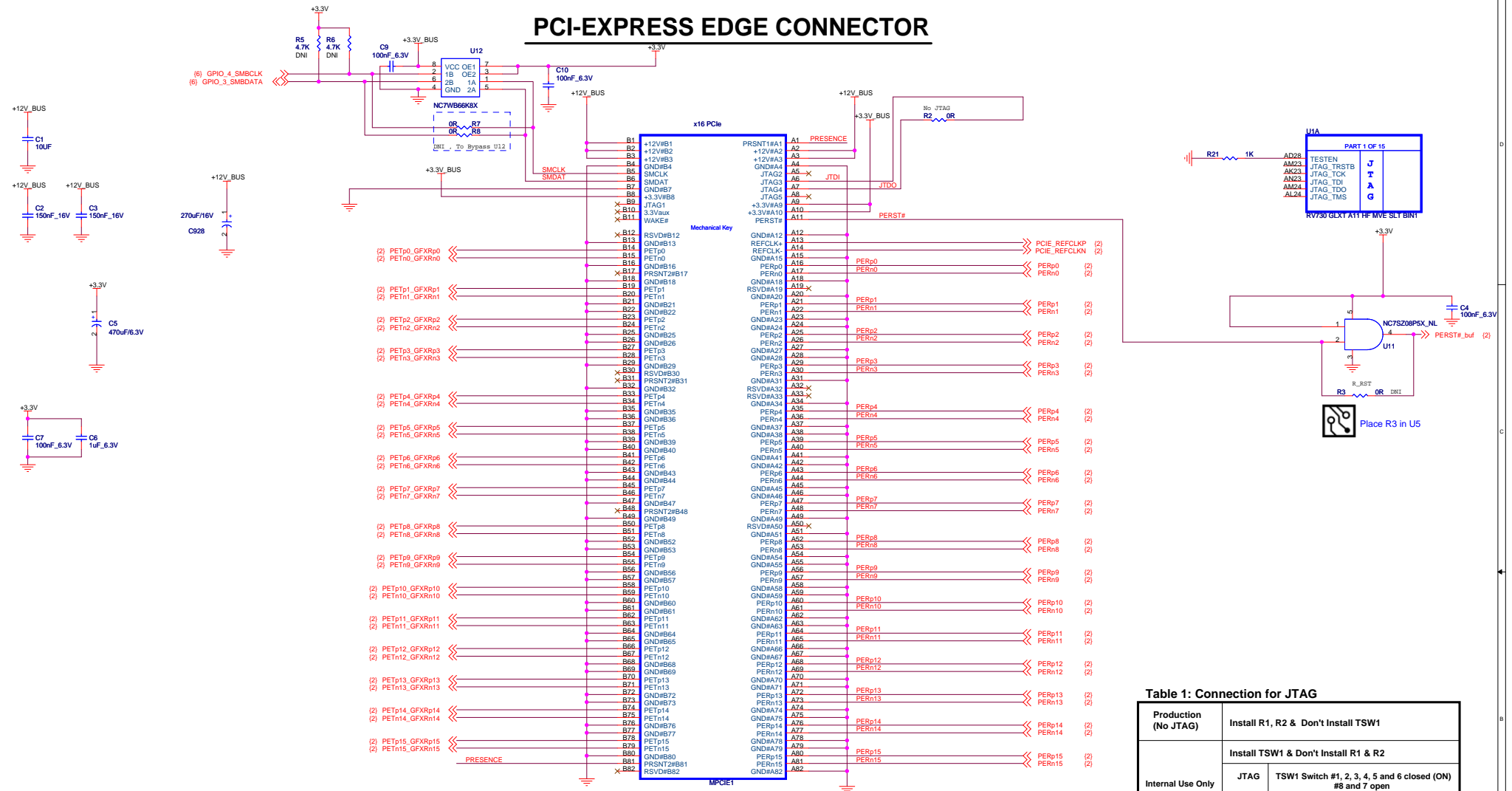


PCI-EXPRESS EDGE CONNECTOR



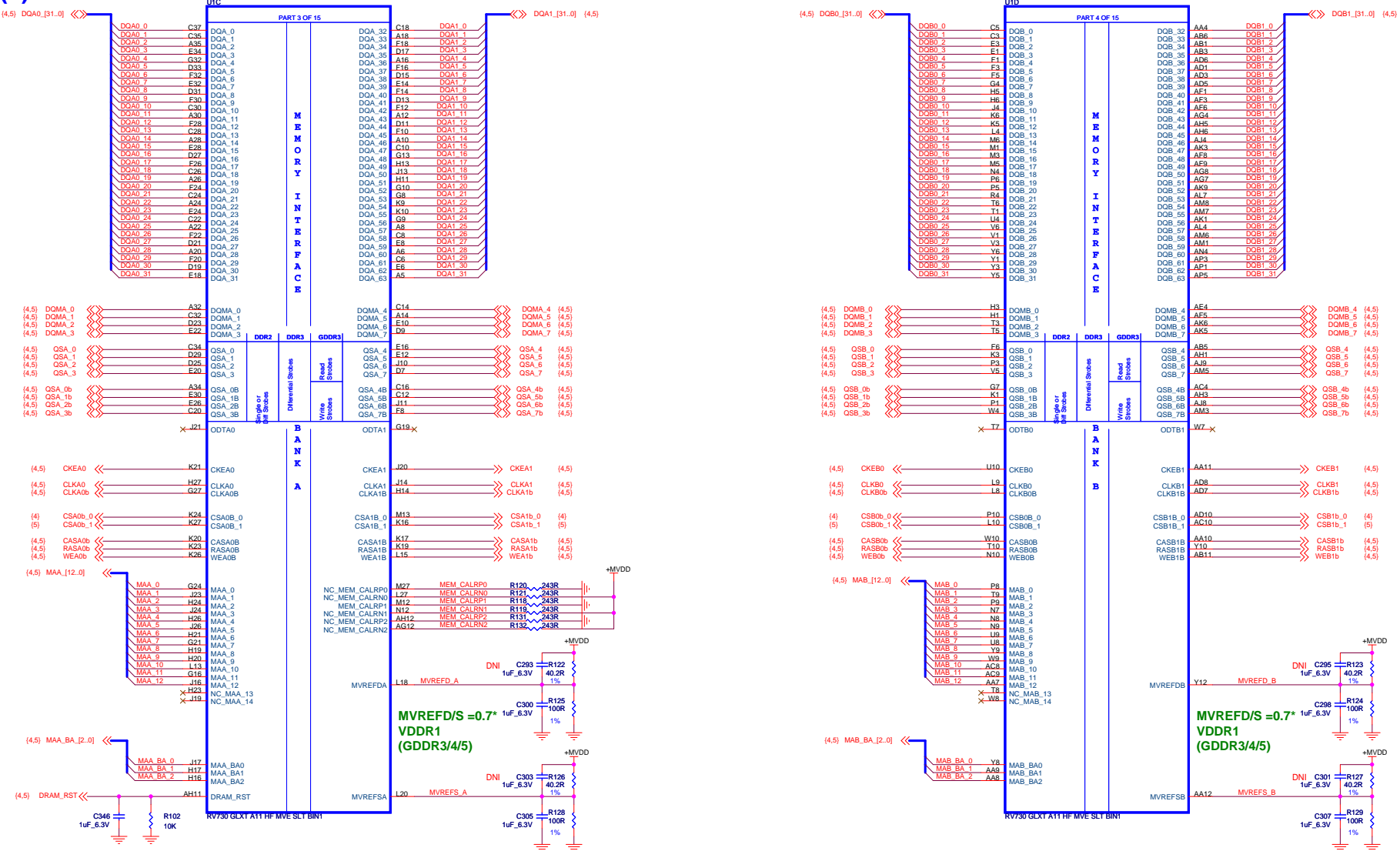
TSW1, R1 & R2 are located on the bottom side of the board close to PCIe connector.

| SYMBOL LEGEND | |
|---------------|----------------|
| DNI | DO NOT INSTALL |
| # | ACTIVE LOW |
| | DIGITAL GROUND |
| | ANALOG GROUND |
| BUO | BRING UP ONLY |

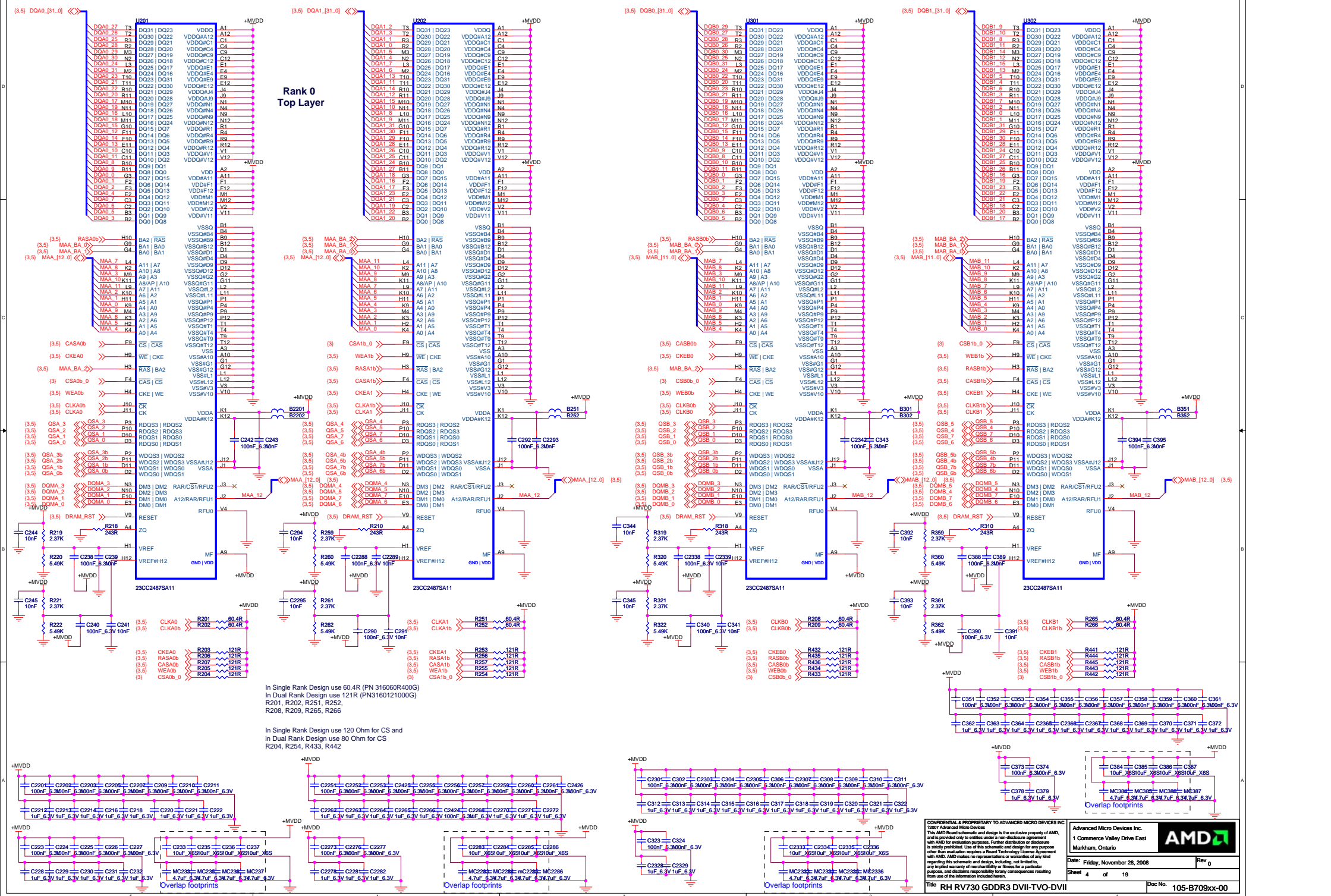


| | | | |
|-------|------------------------------|---------|---------------|
| Title | RH RV730 GDDR3 DVII-TVO-DVII | Doc No. | 105-B709xy-00 |
|-------|------------------------------|---------|---------------|

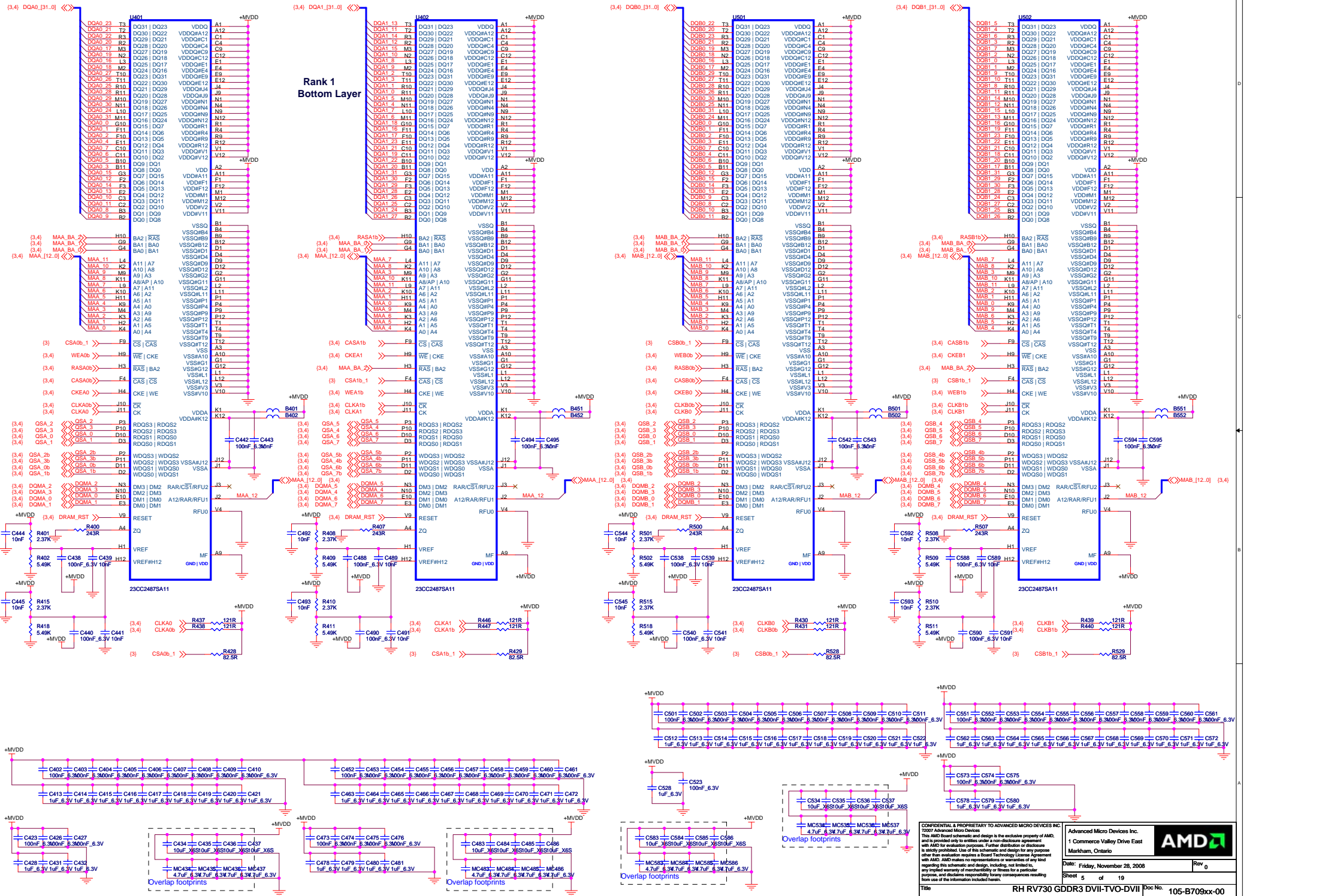
(3) RV730 MEM Interface Ch A&B



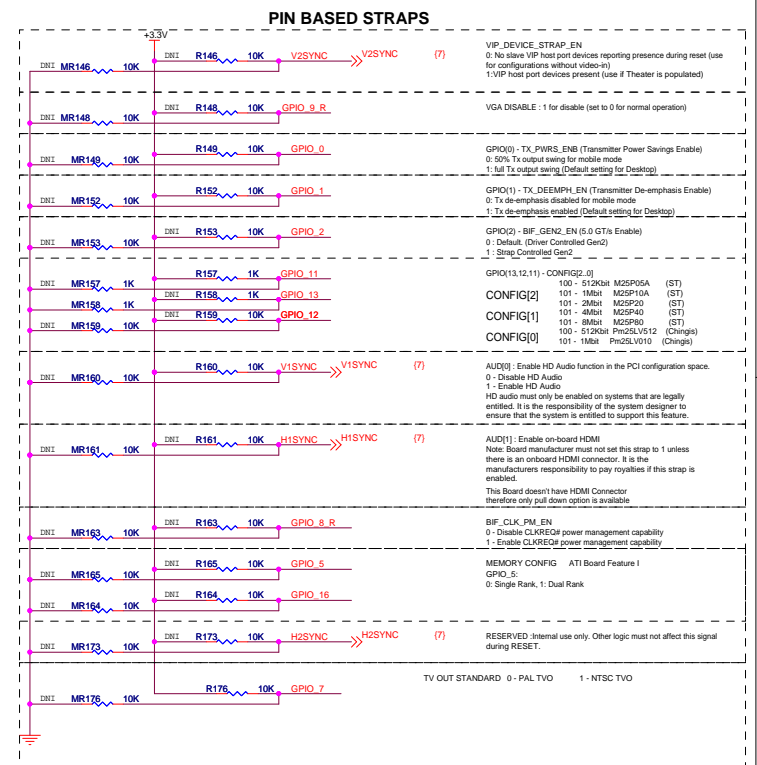
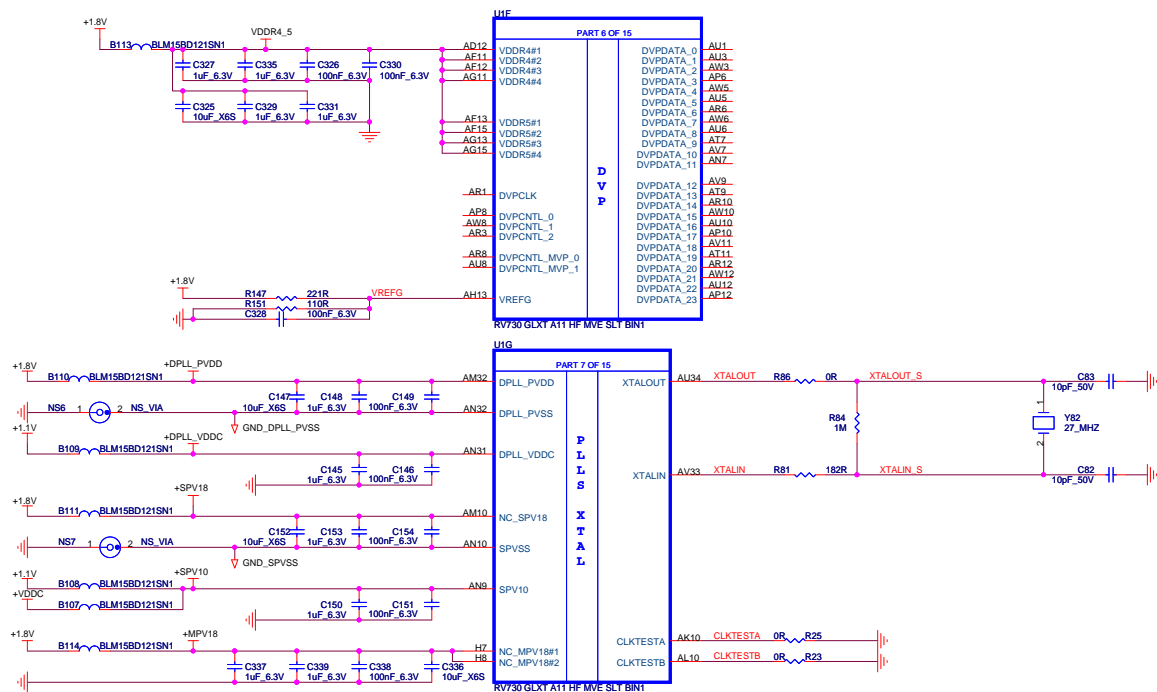
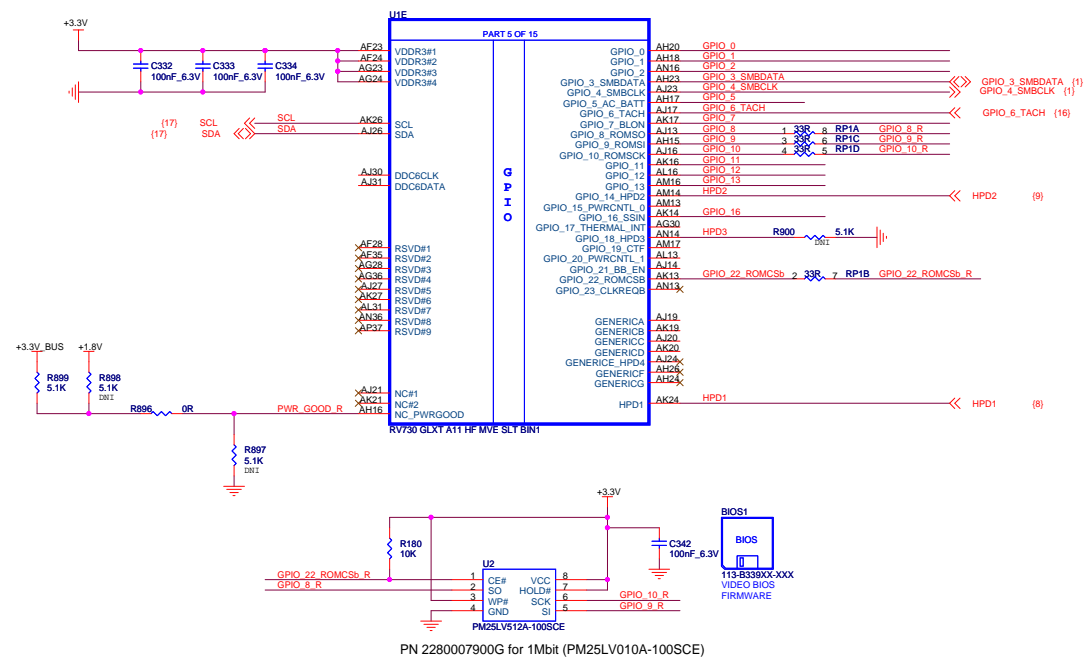
(4) GDDR3 Memory Channel A&B Bank 0



(5) GDDR3 Memory Channel A&B Bank 1




(06) RV730 GPIOs Strap CF XTAL

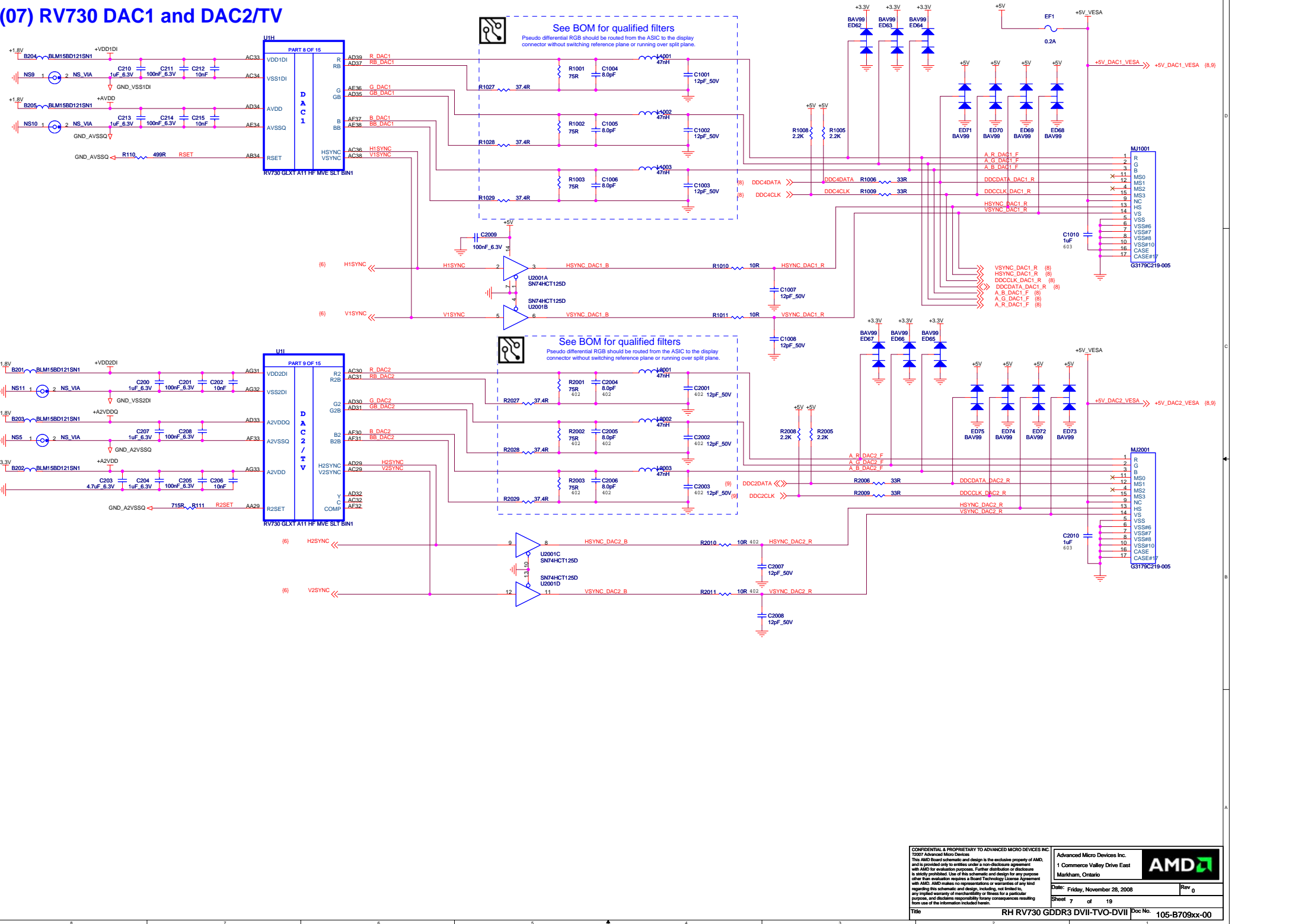


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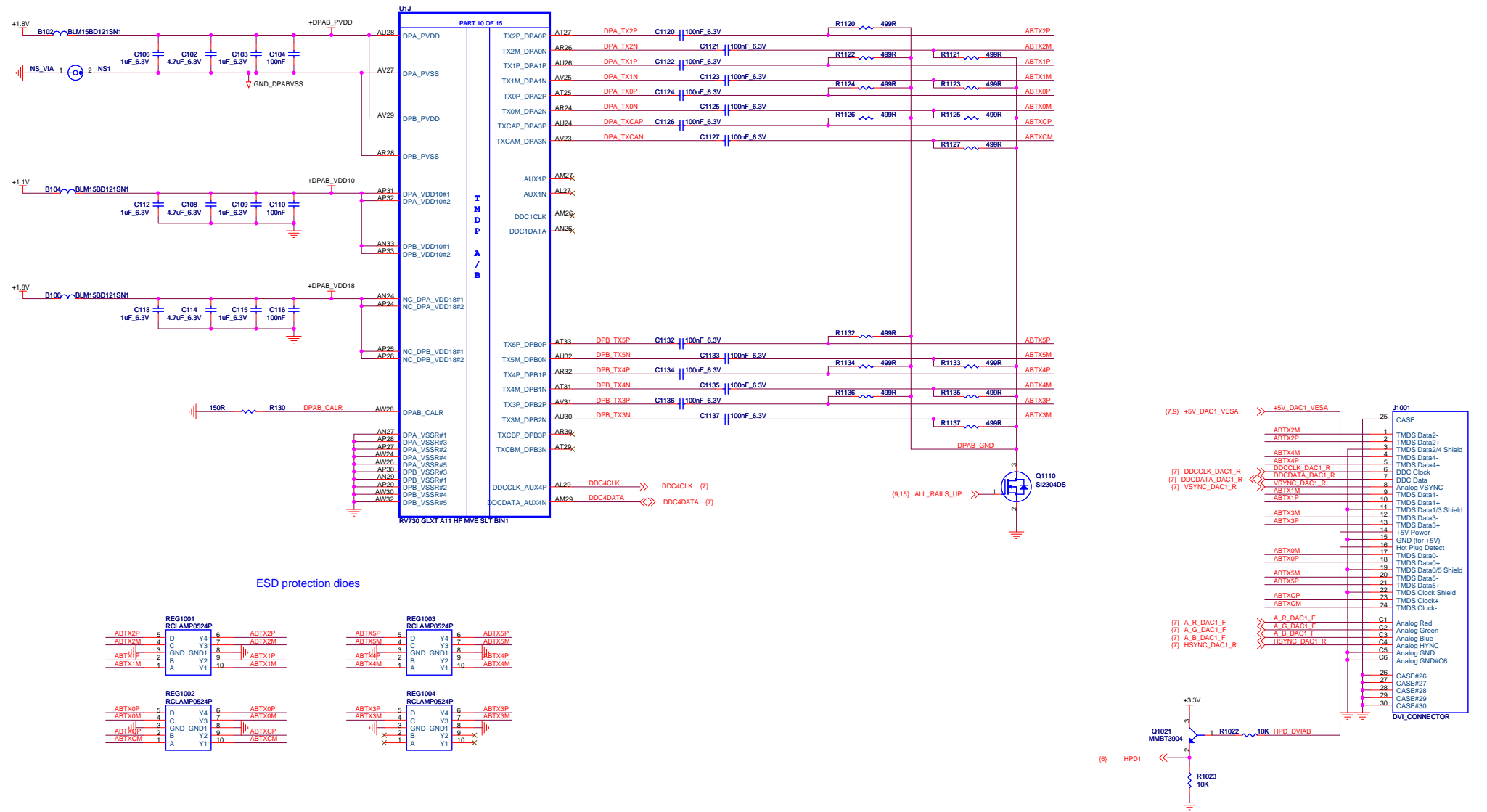
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| | | | |
|--|--|---|--|
| <p>Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario</p> | |  | |
| <p>Date: Friday, November 28, 2008</p> | | <p>Rev 0</p> | |
| <p>Sheet 6 of 19</p> | | | |

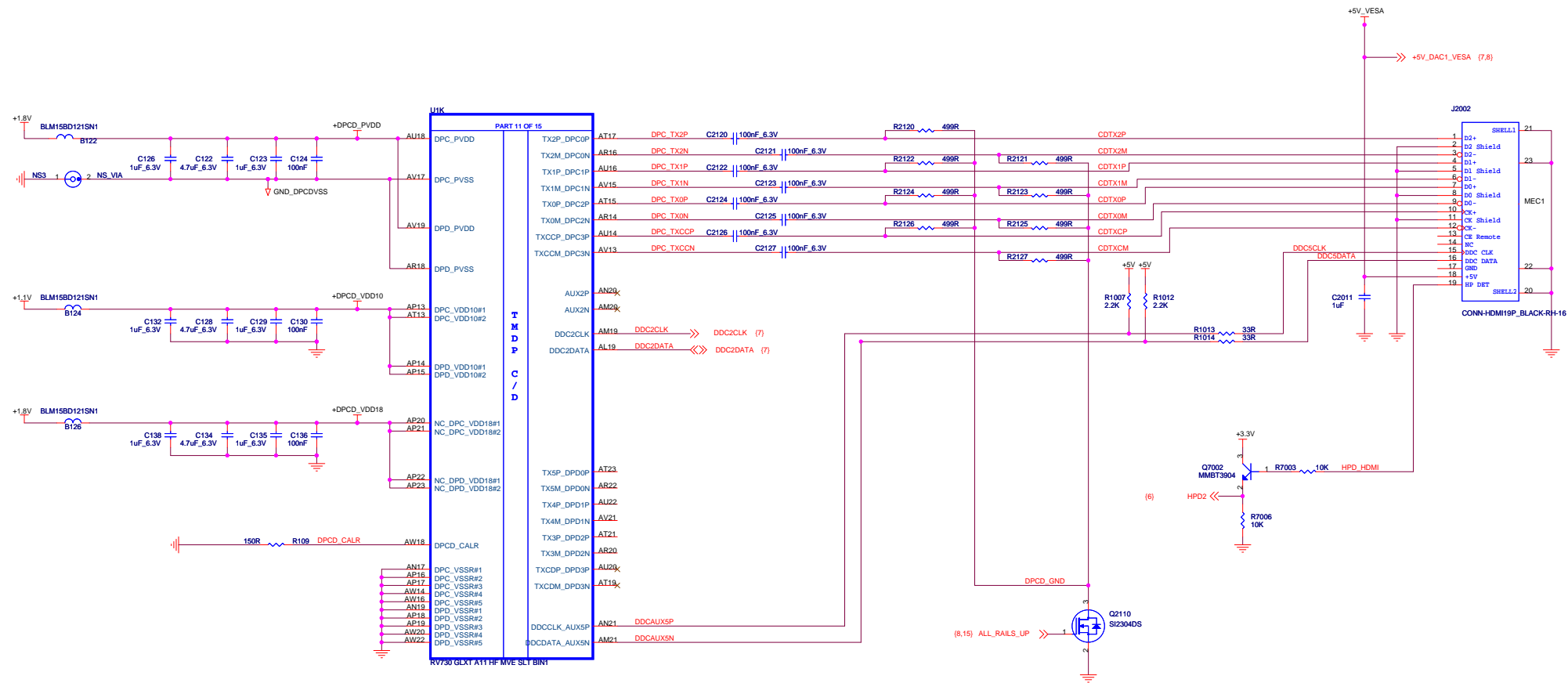
(07) RV730 DAC and DAC2/TV



(08) RV730 TMD5 A&B



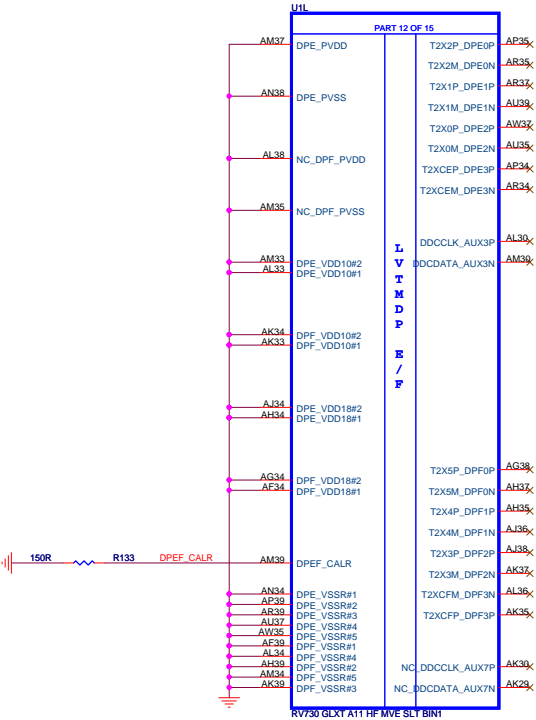
(09) RV730 Display Port C&D



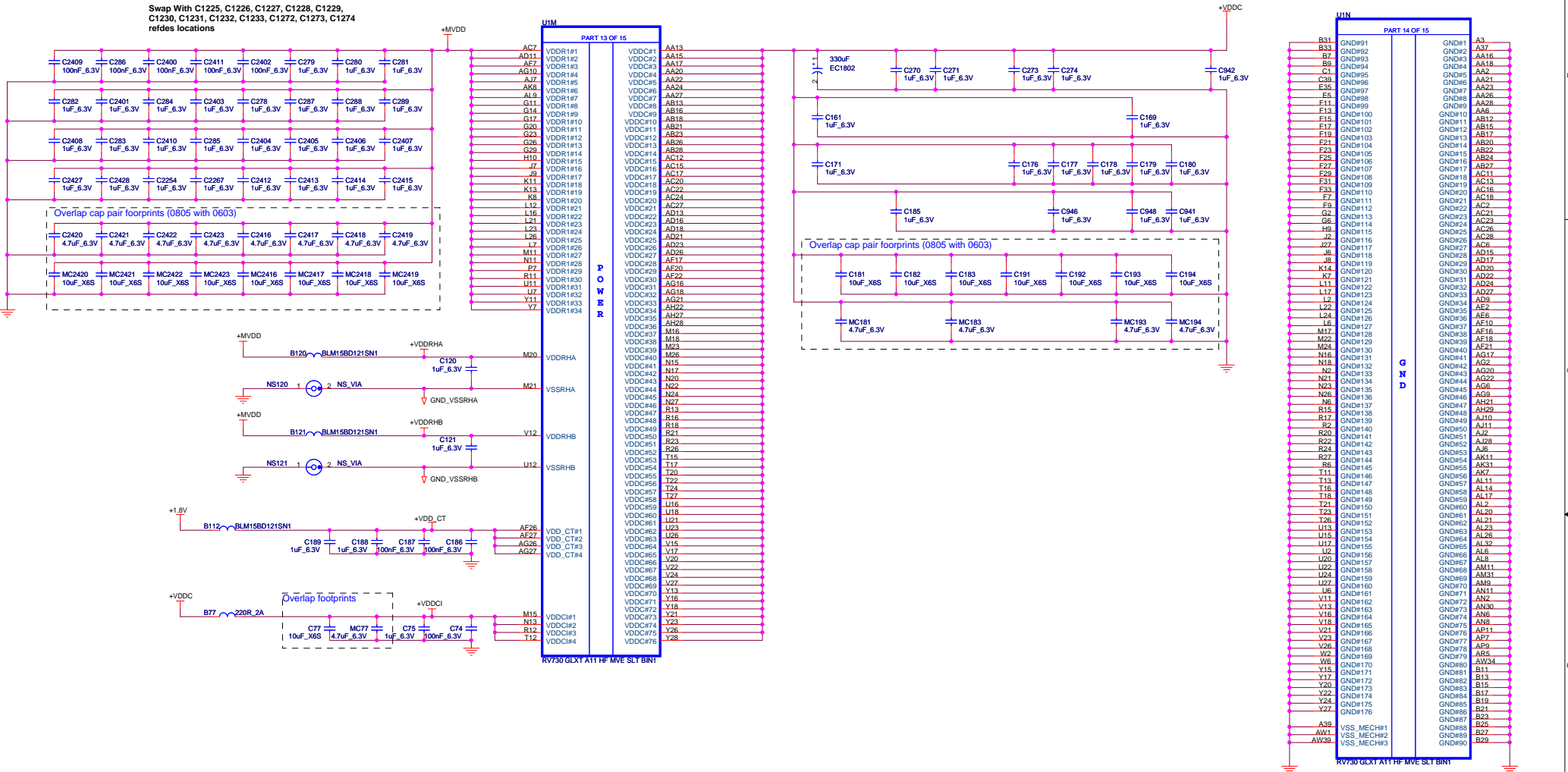
ESD protection diodes



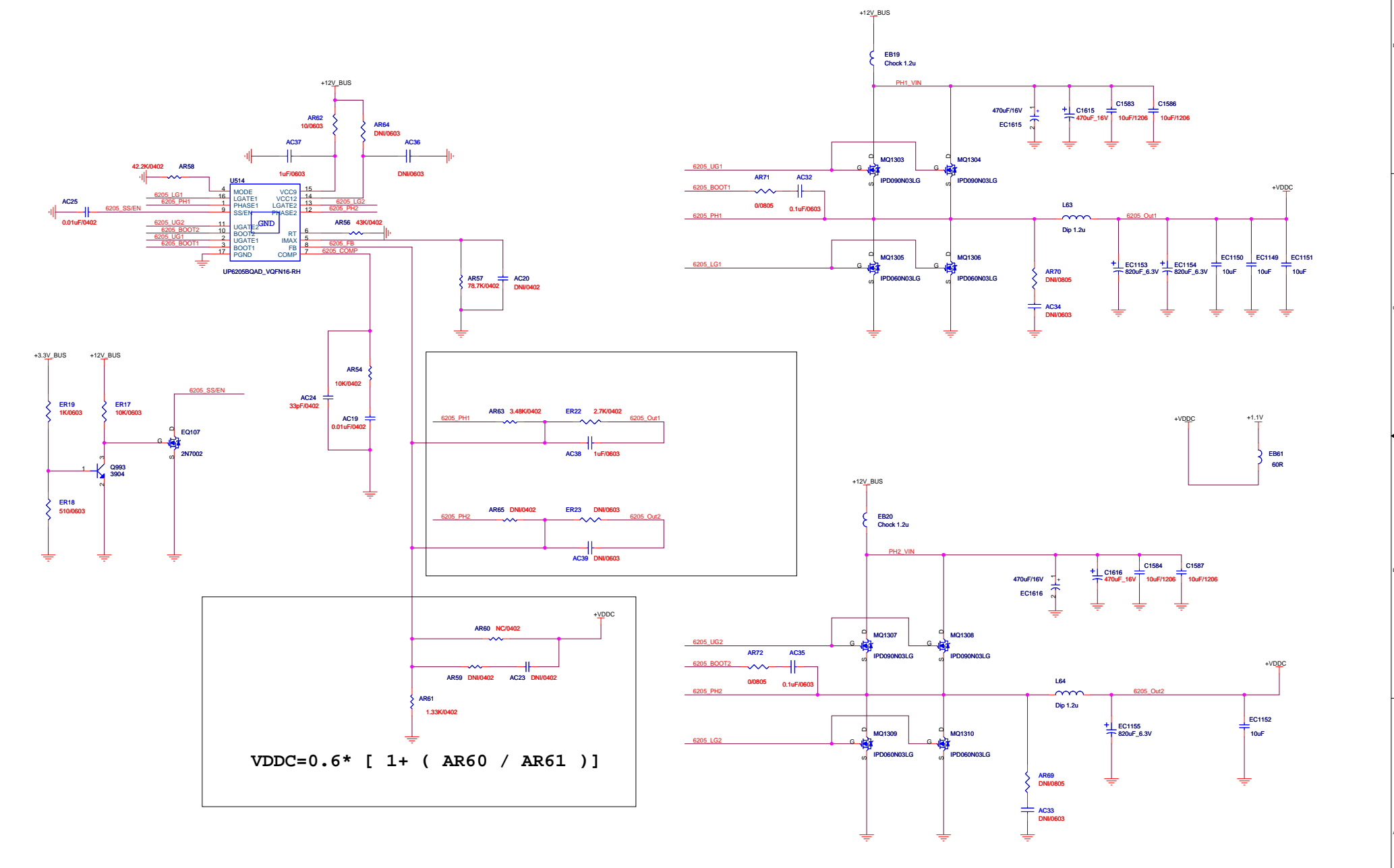
(10) No Connect E&F



(11) RV730 Power & GND

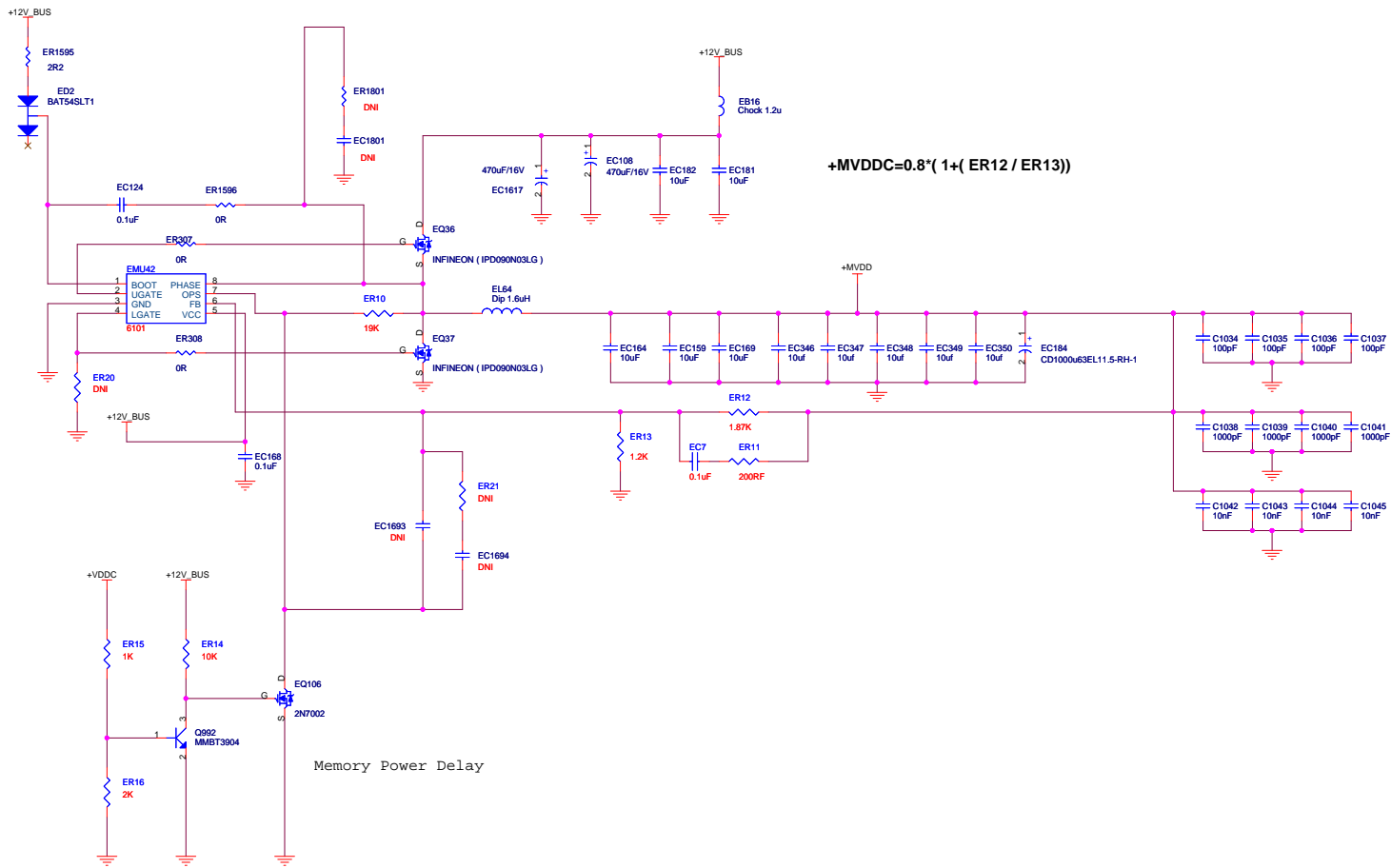


(12) VDDC



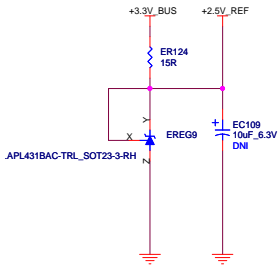
$$VDDC = 0.6 * [1 + (AR60 / AR61)]$$

(13) MVDD

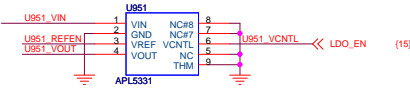
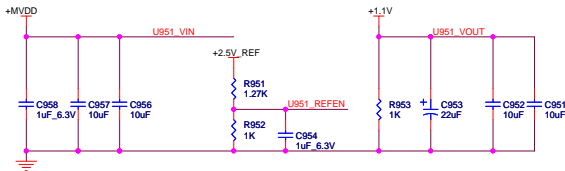


Memory Power Delay

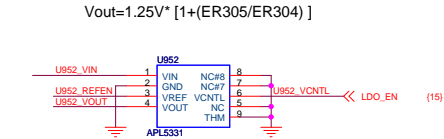
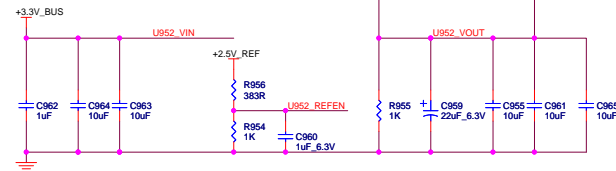
(14) Linear Regulators



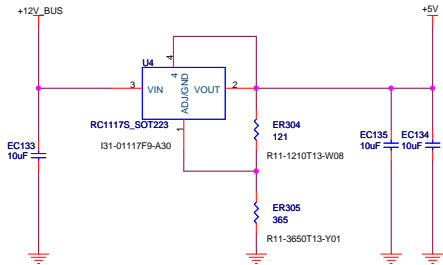
Optional regulator for +1.1V
Vout = 1.1V



Optional regulator for +1.8V
Vout = 1.8V

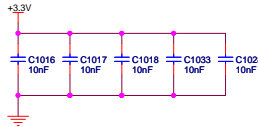
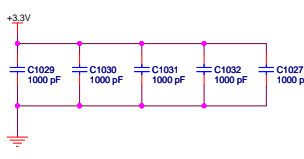
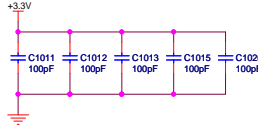
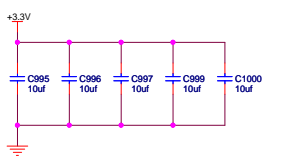
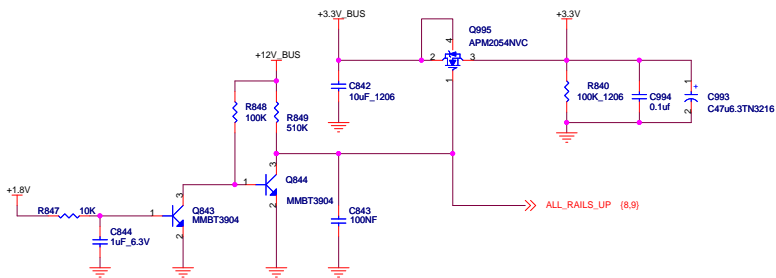
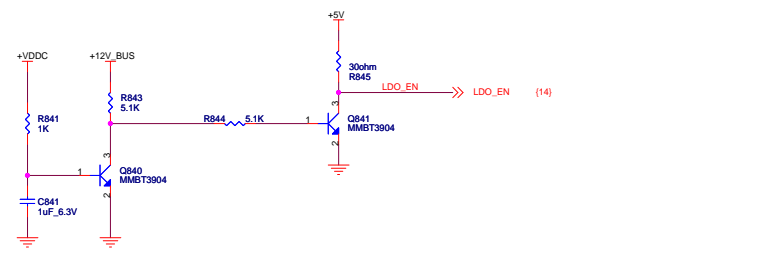


$V_{out}=1.25V \cdot [1+(ER305/ER304)]$

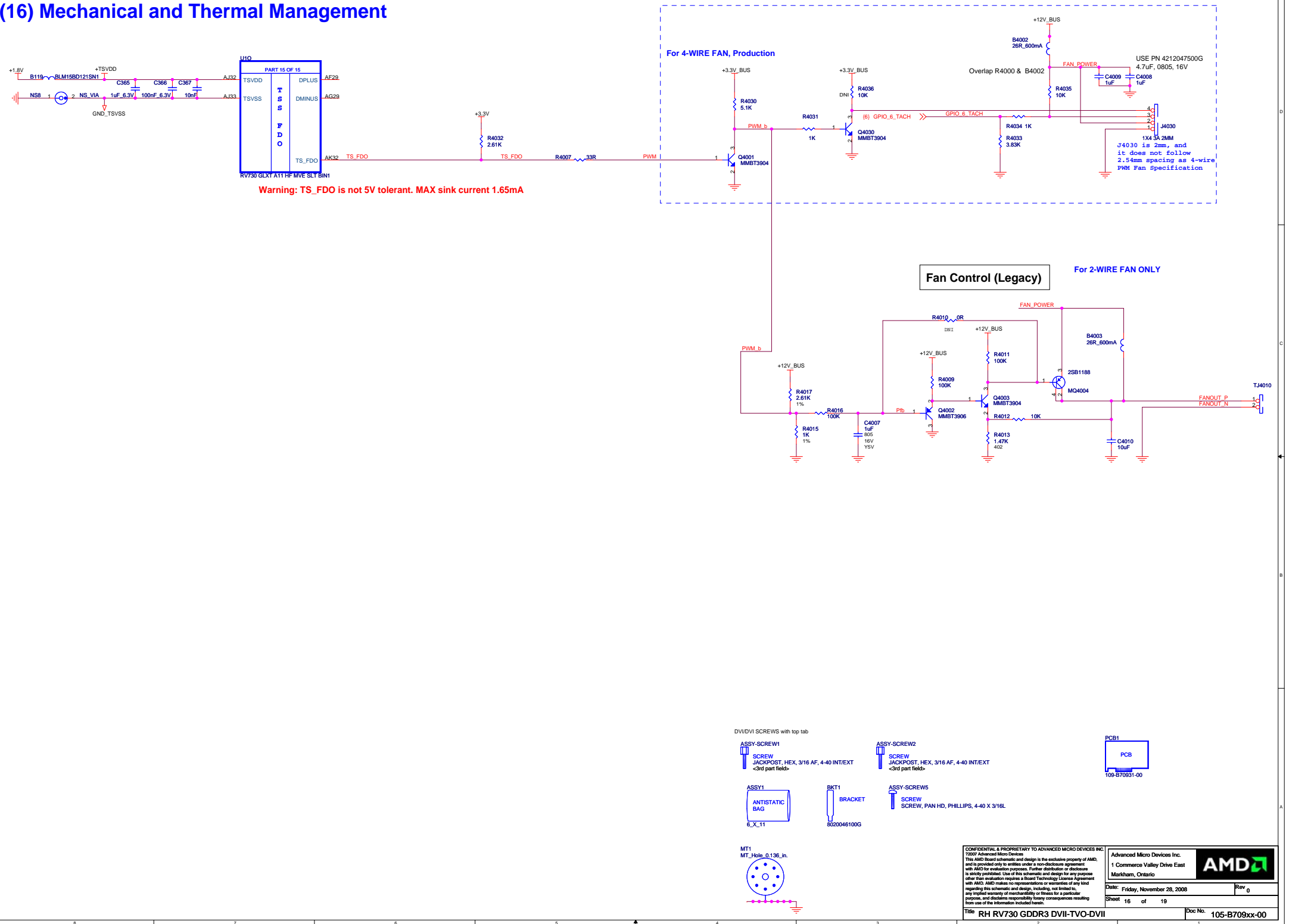


(15) Power Management

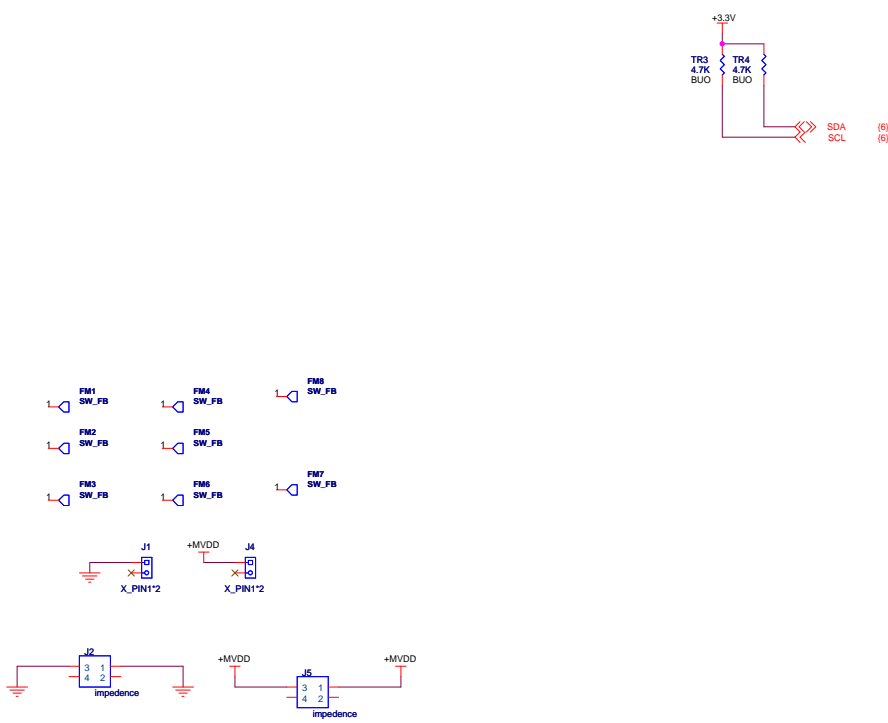
Power up Sequencing

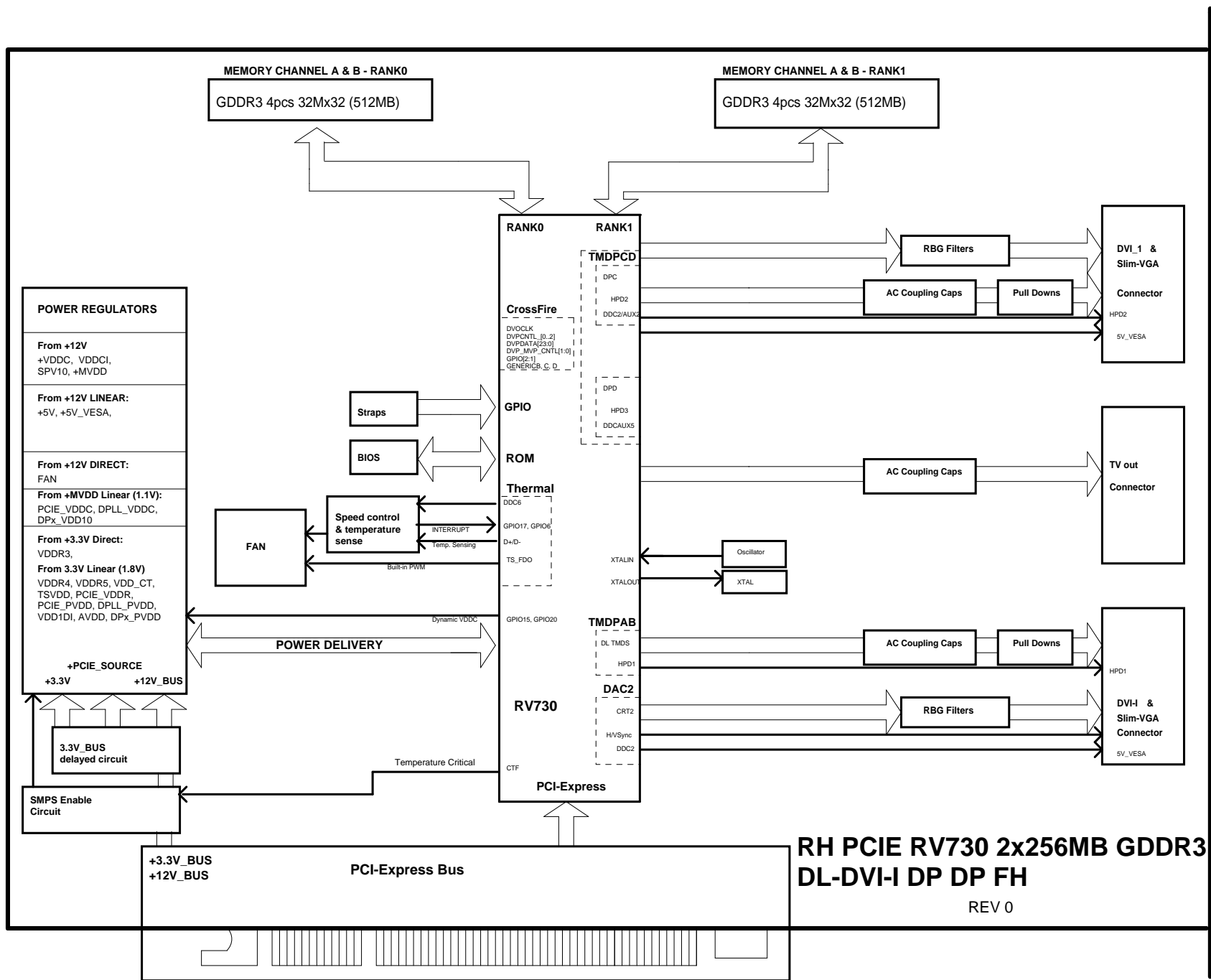


(16) Mechanical and Thermal Management



(17) Debug Circuits





| | | | | | | | | |
|------------------|---------|----------|--|--|---------------|--|---------------------------|-------|
| <div>AMD</div> | | | Title | | Schematic No. | | Date: | |
| | | | RH RV730 GDDR3 DVII-TVO-DVII | | 105-B709xx-00 | | Friday, November 28, 2008 | |
| REVISION HISTORY | | | NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired. | | | | | Rev 0 |
| | | | | | | | | |
| Sch Rev | PCB Rev | Date | REVISION DESCRIPTION | | | | | |
| A | A | 08/06/25 | Initial release; design for RV730 GDDR3 DVII TVO DVII | | | | | |
| 00 | 00 | 08/06/30 | Production release; based from B667 and B666 | | | | | |