G94-P545-A01 - GDDR3, DVI/VGA + DVI/VGA + Display port + HDMI

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10545-base-100	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU9100	600-10545-9100-100	G94-400 650MHz/1000MHz 512MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out (Bring Up SKU)
2	SKU0000	600-10545-0000-100	G94-400 650MHz/1000MHz 512MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
3	SKU0010	600-10545-0010-100	G94-300 500MHz/800MHz 512MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
4	SKU0020	600-10545-0020-100	G94-200 500MHz/800MHz 384MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
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V145-0A Base on V135-100 and P545

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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview

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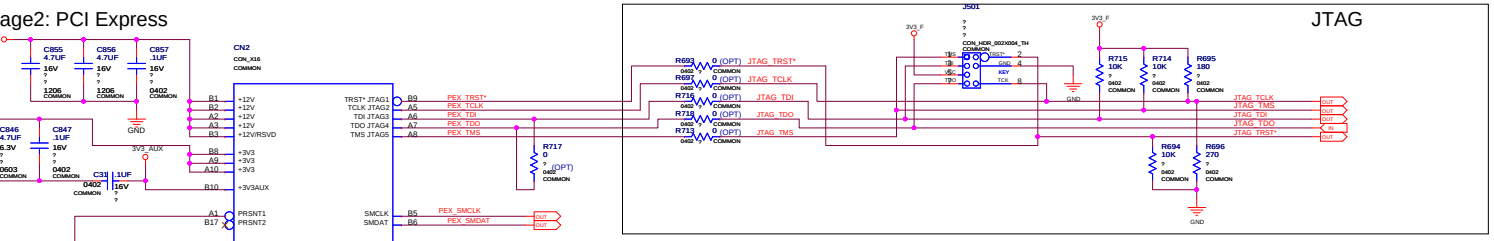

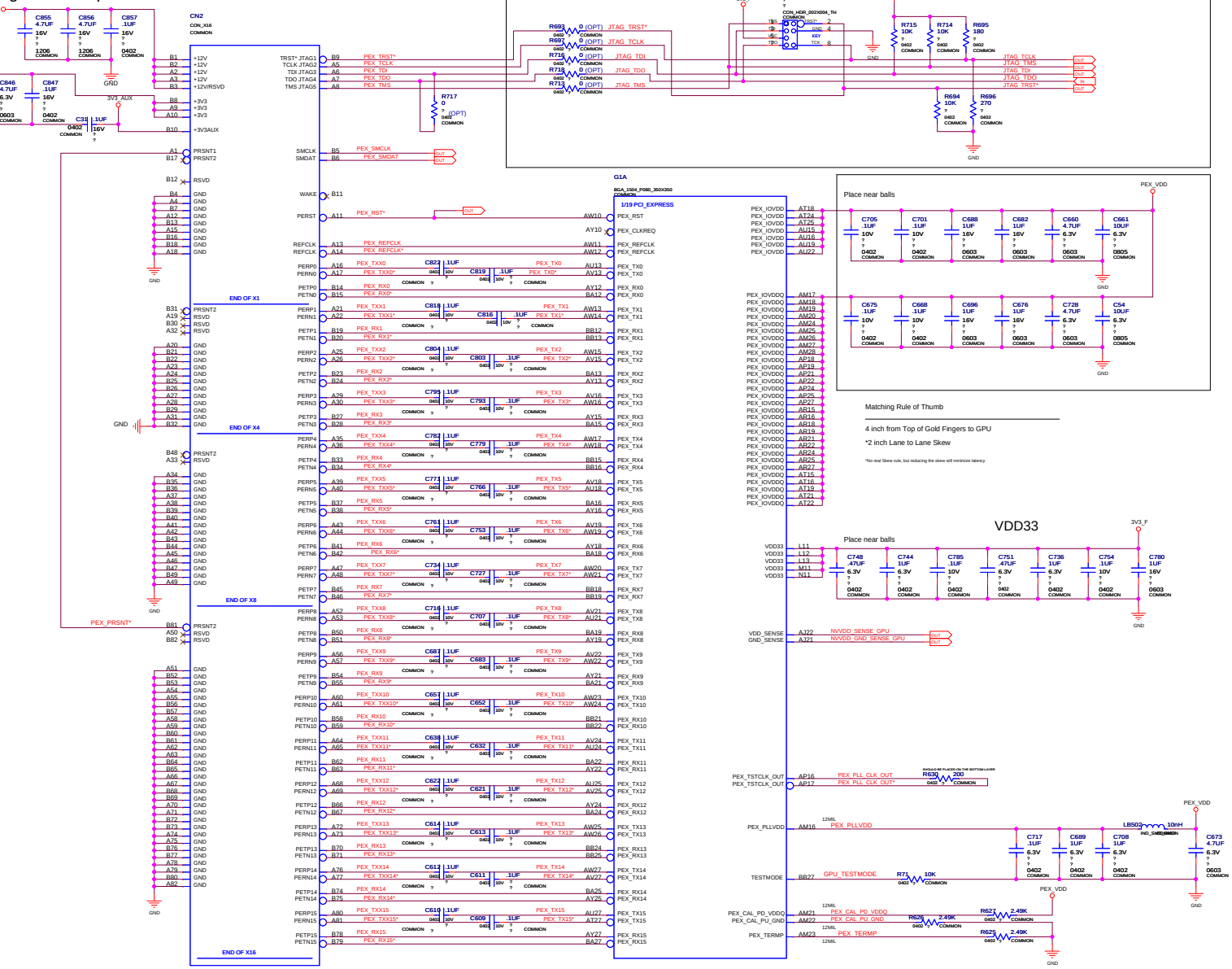

Matching Rule of Thumb

4 inch from Top of Gold Fingers to GPU

*2 inch Lane to Lane Skew

*No real Skew rule, but reducing the skew will minimize latency

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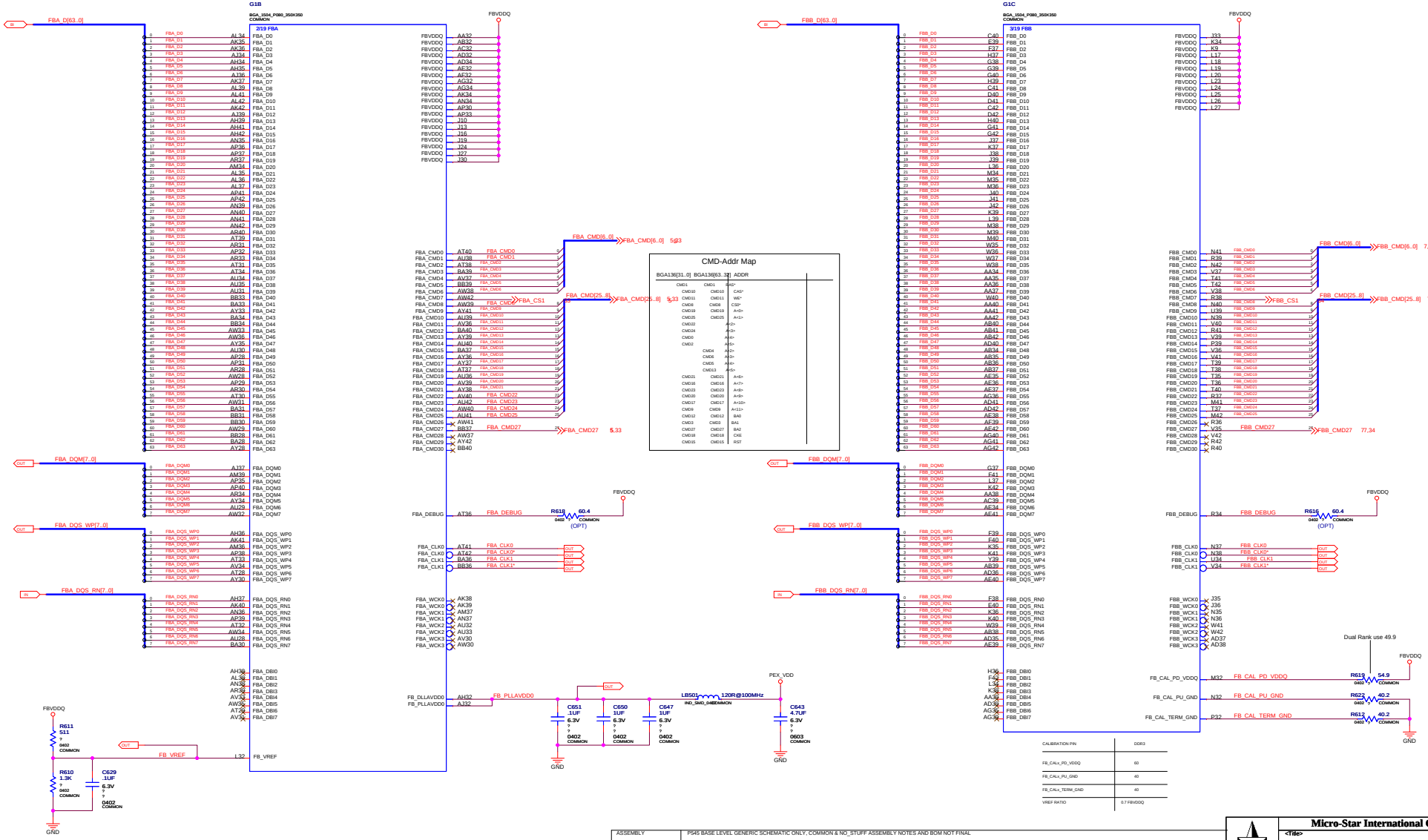

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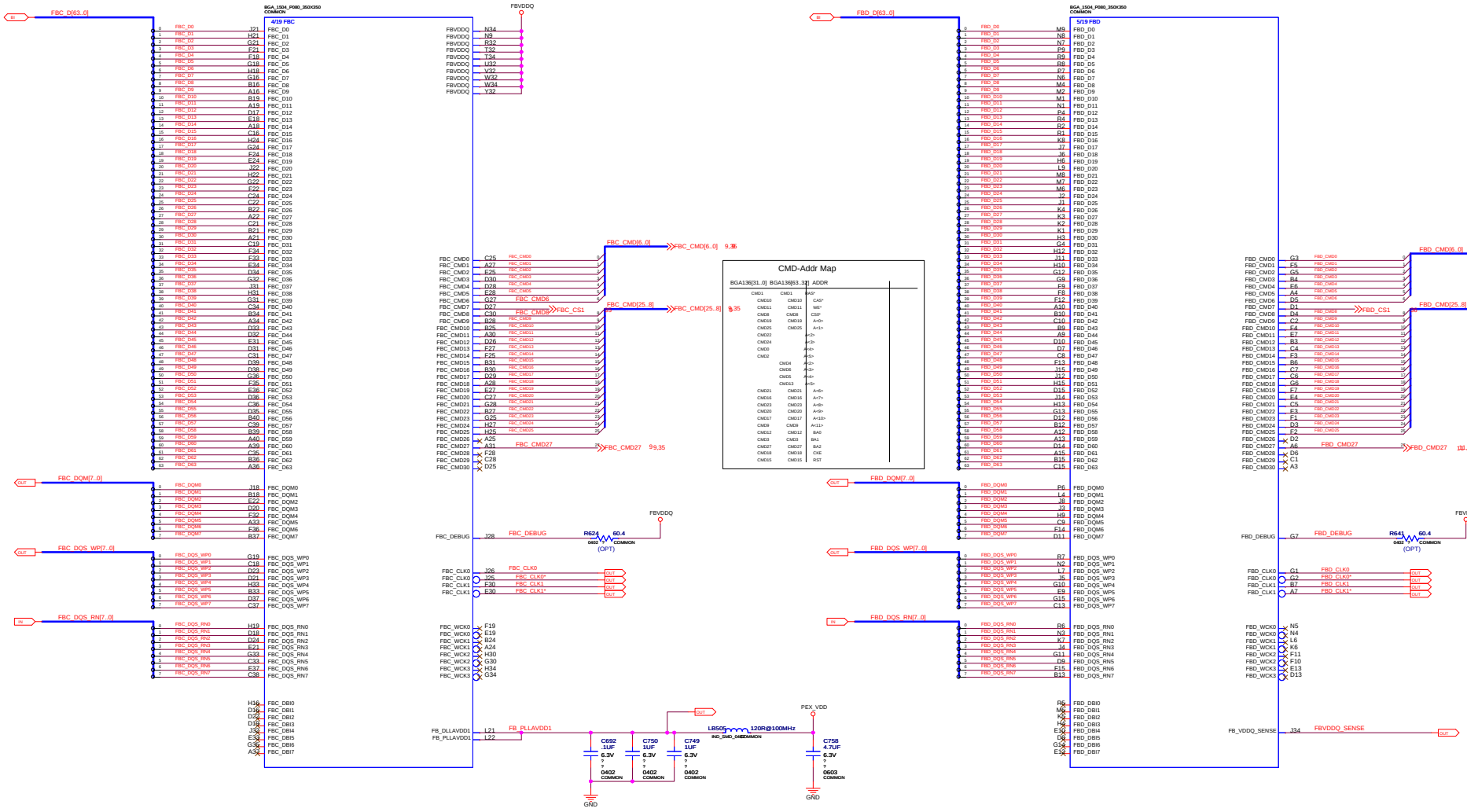

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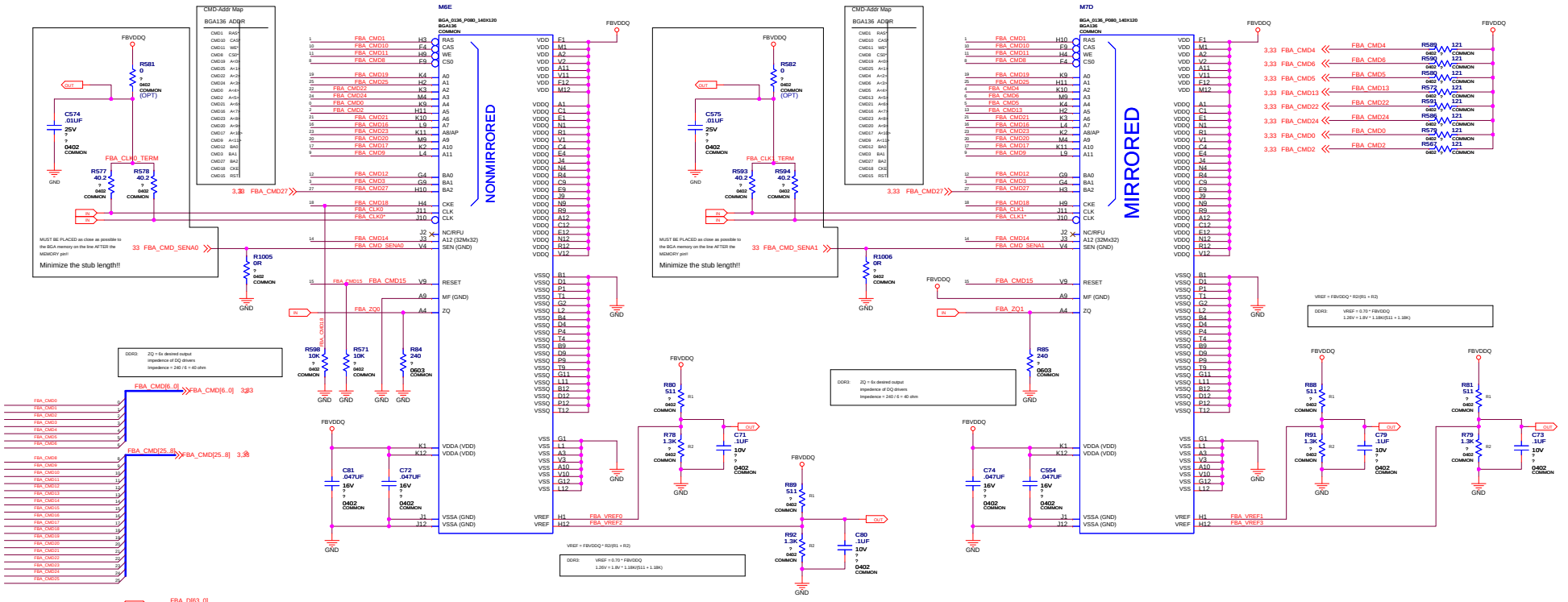
Page5: FBA Partition



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Page6: FBA Partition Decoupling

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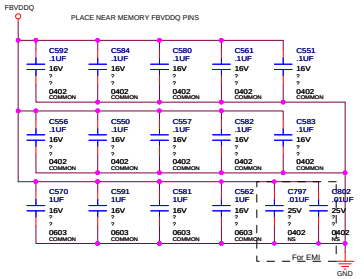

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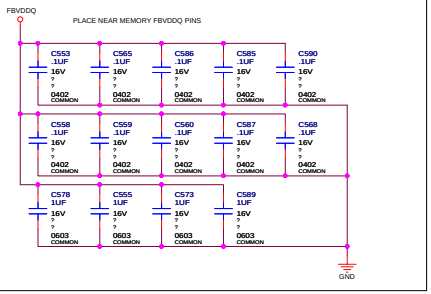

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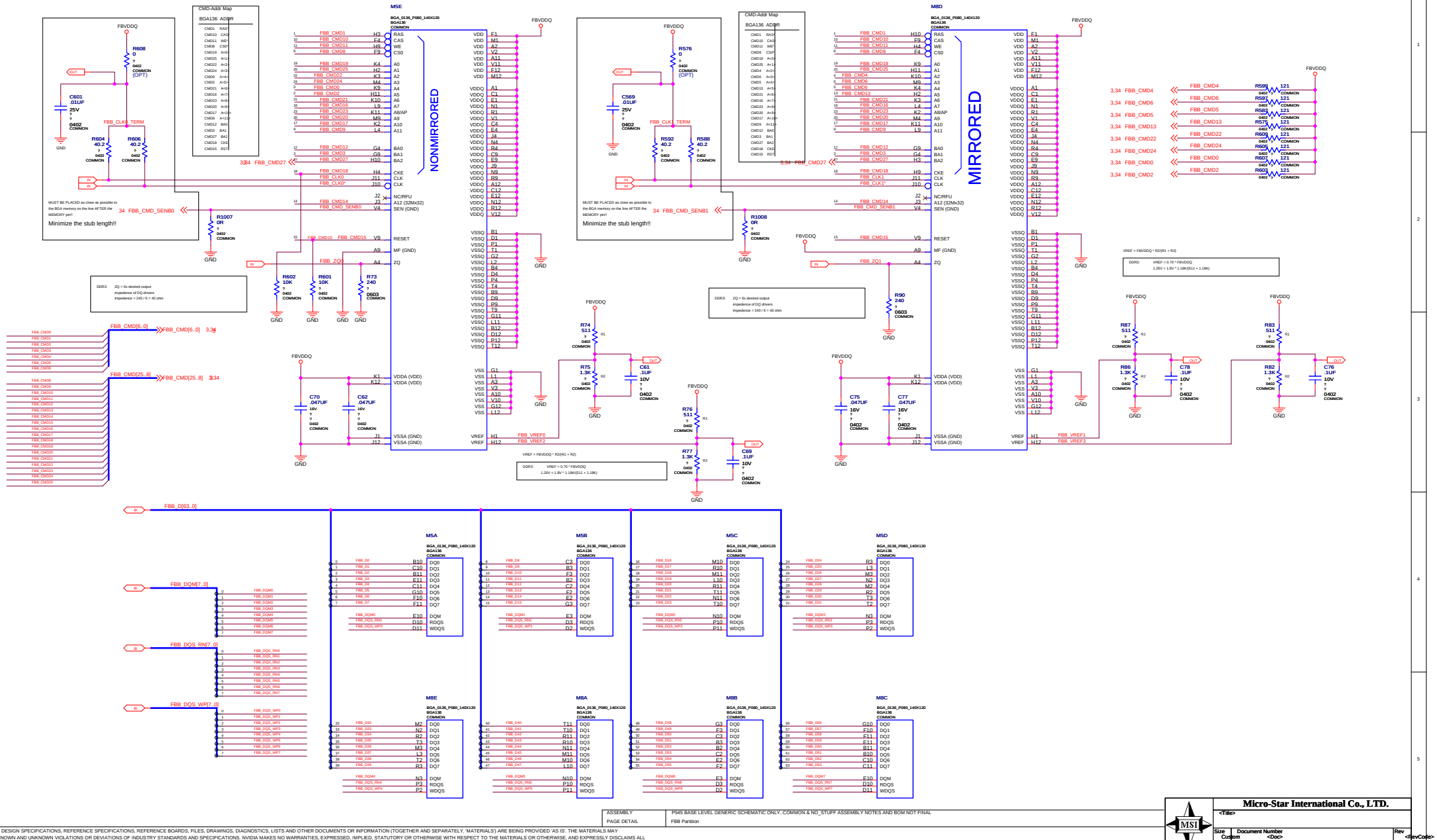

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PAGE DETAIL: FBB Partition

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Page8: FBB Partition Decoupling

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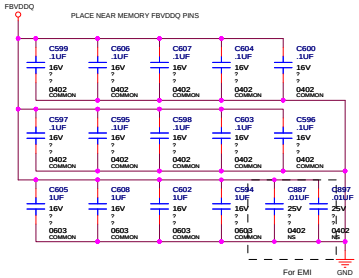

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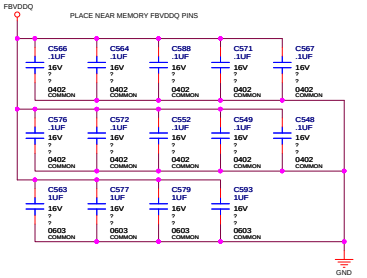

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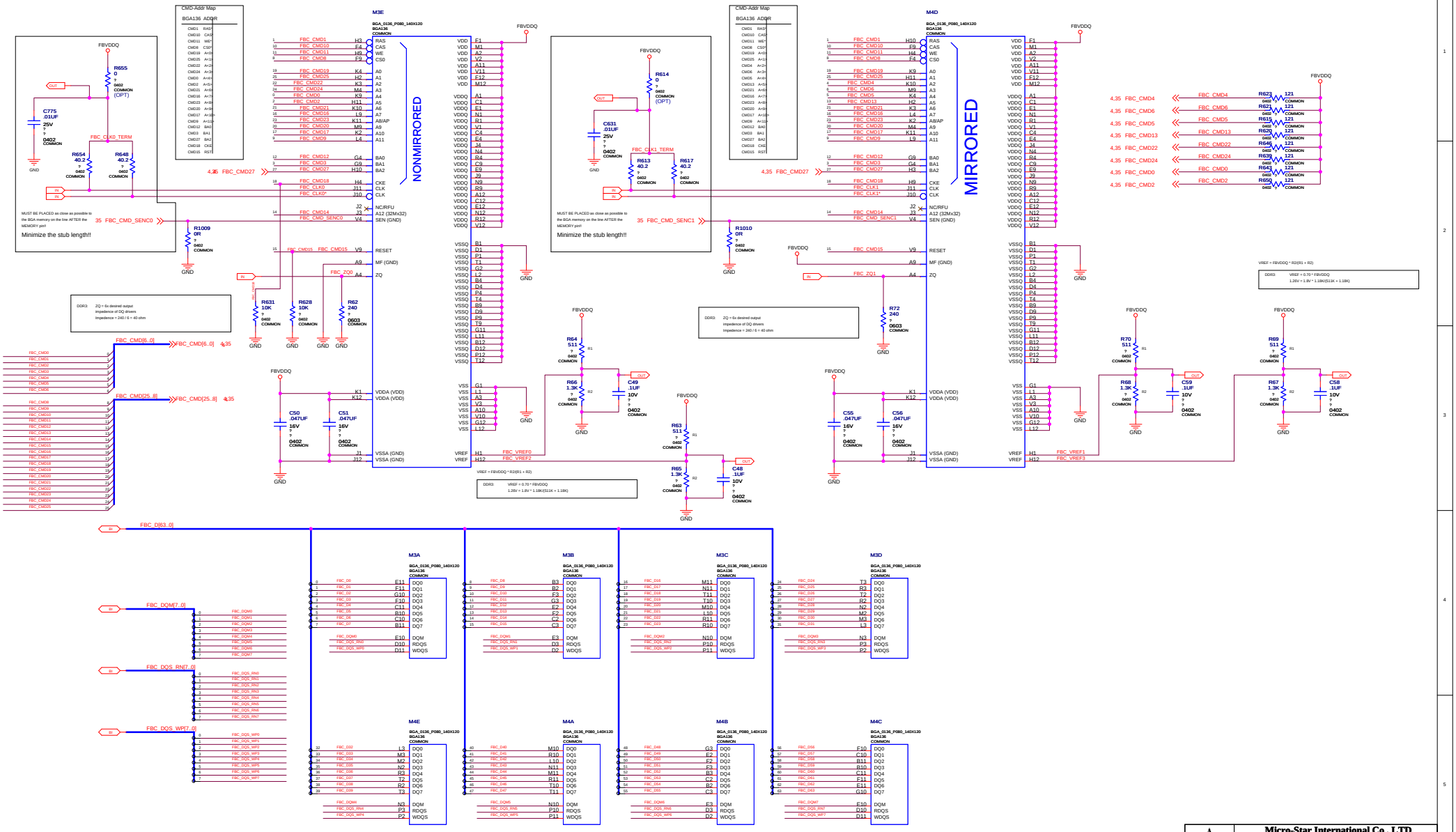

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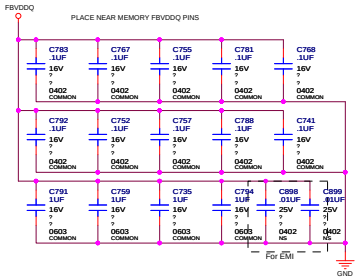

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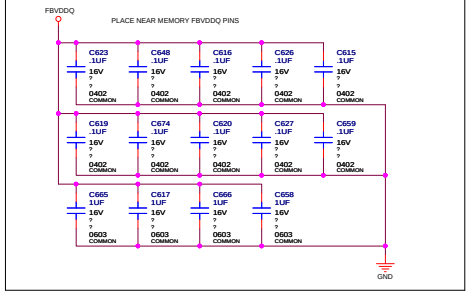

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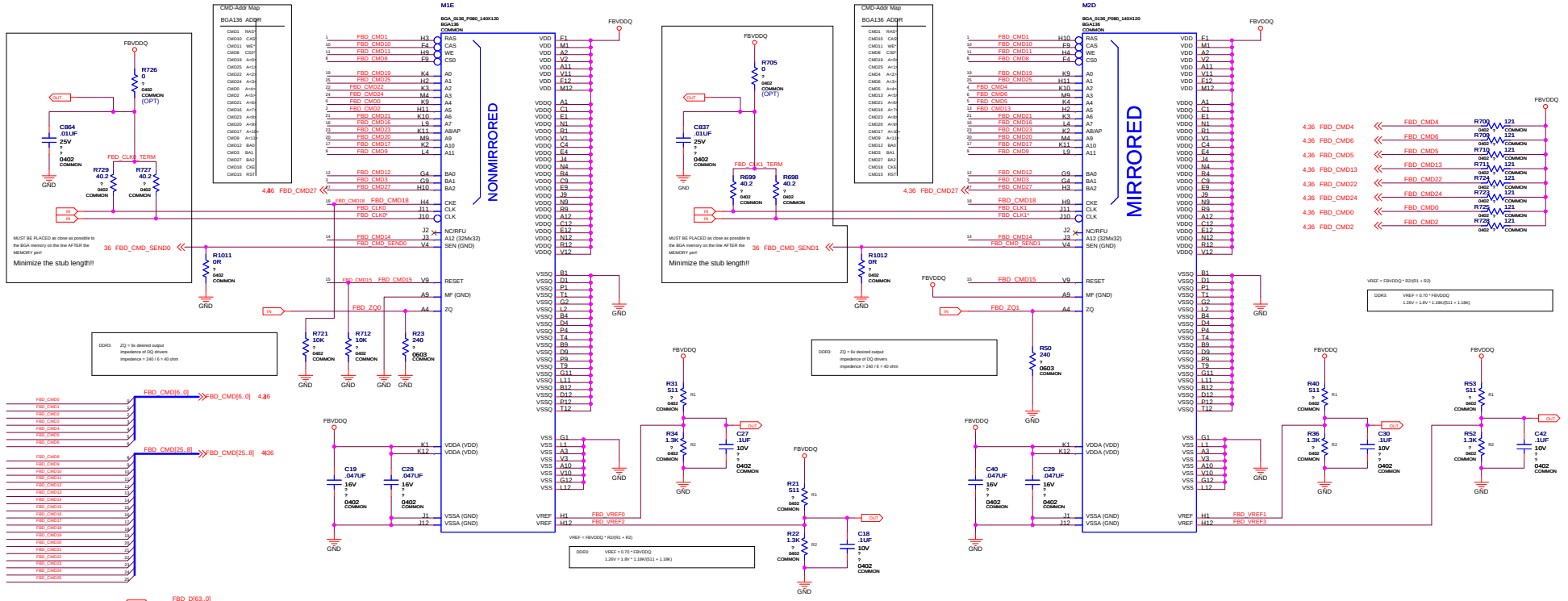
Page11: FBD Partition



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PAGE DETAIL	FBD Partition

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Page12: FBD Partition Decoupling

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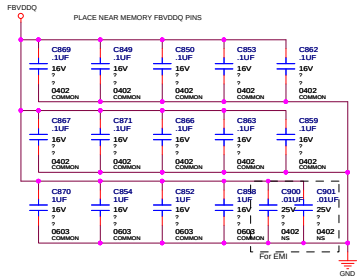

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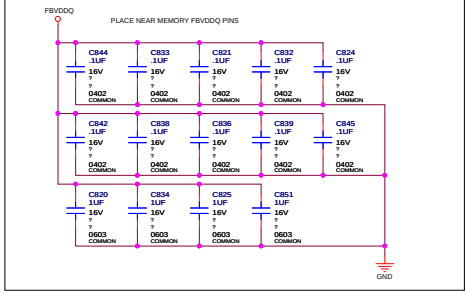

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PAGE DETAIL	FBD Partition Decoupling

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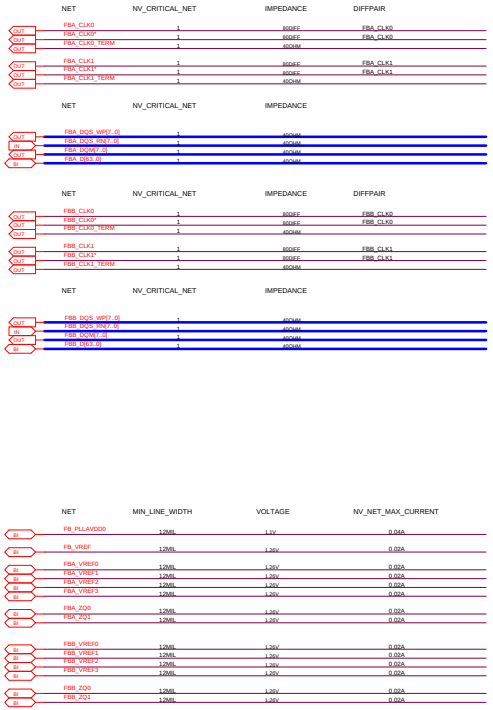
Page13: FB Net Properties

NET RULES for FBA and FBB



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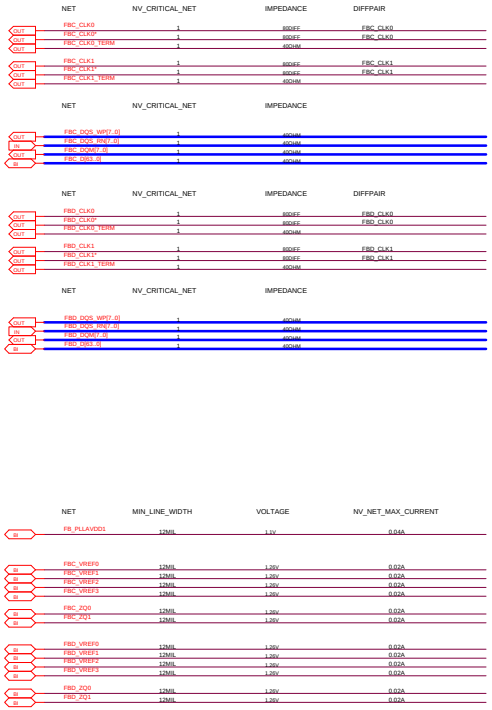

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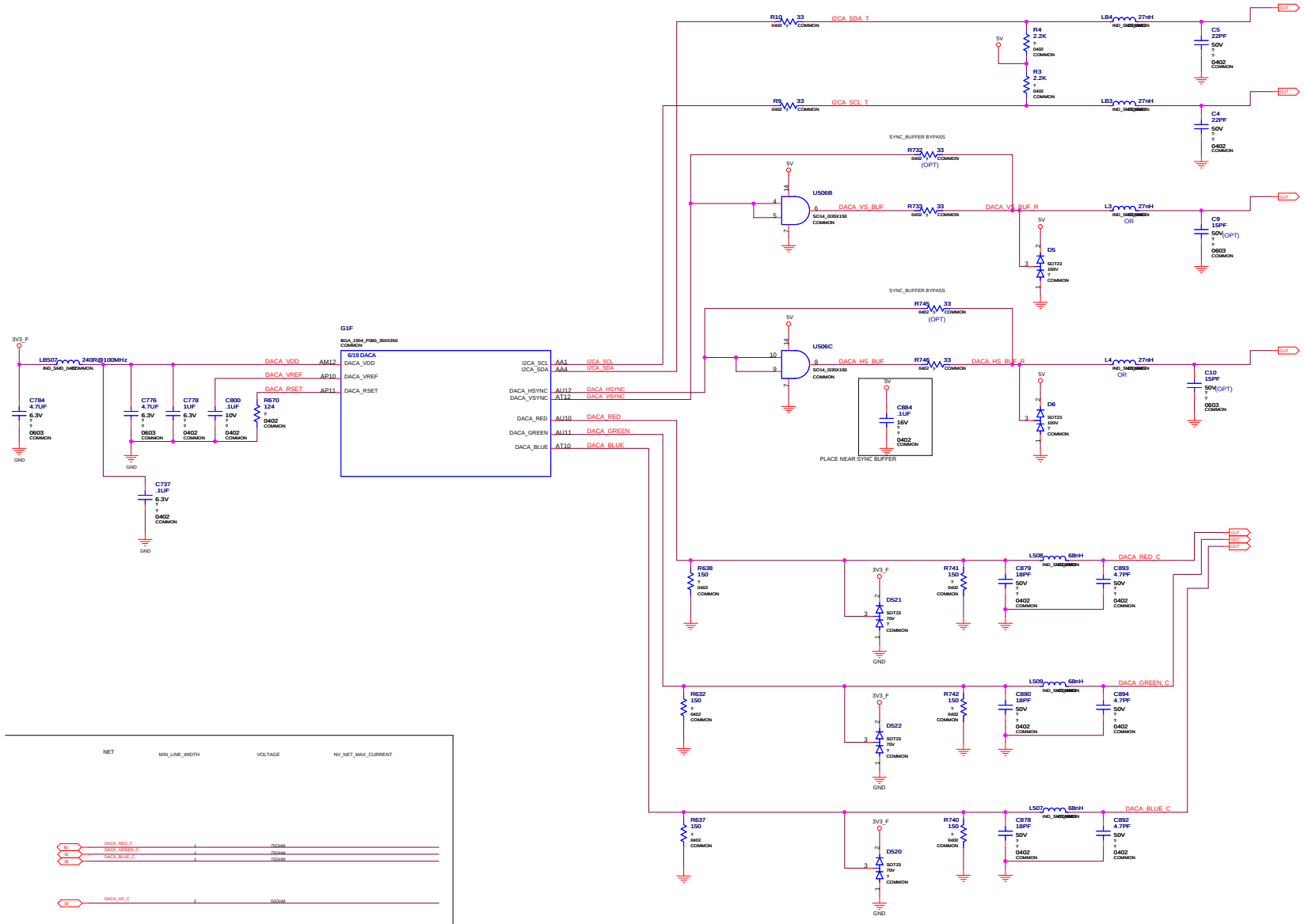
Page14: DACA Interface

DACA RGB-FILTER



NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
DACA_RED_C	1		75OHM
DACA_GREEN_C	1		75OHM
DACA_BLUE_C	1		75OHM
DACA_HS_C	2		50OHM
DACA_VS_C	2		50OHM

ASSEMBLY: PS4S BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: DACA Interface

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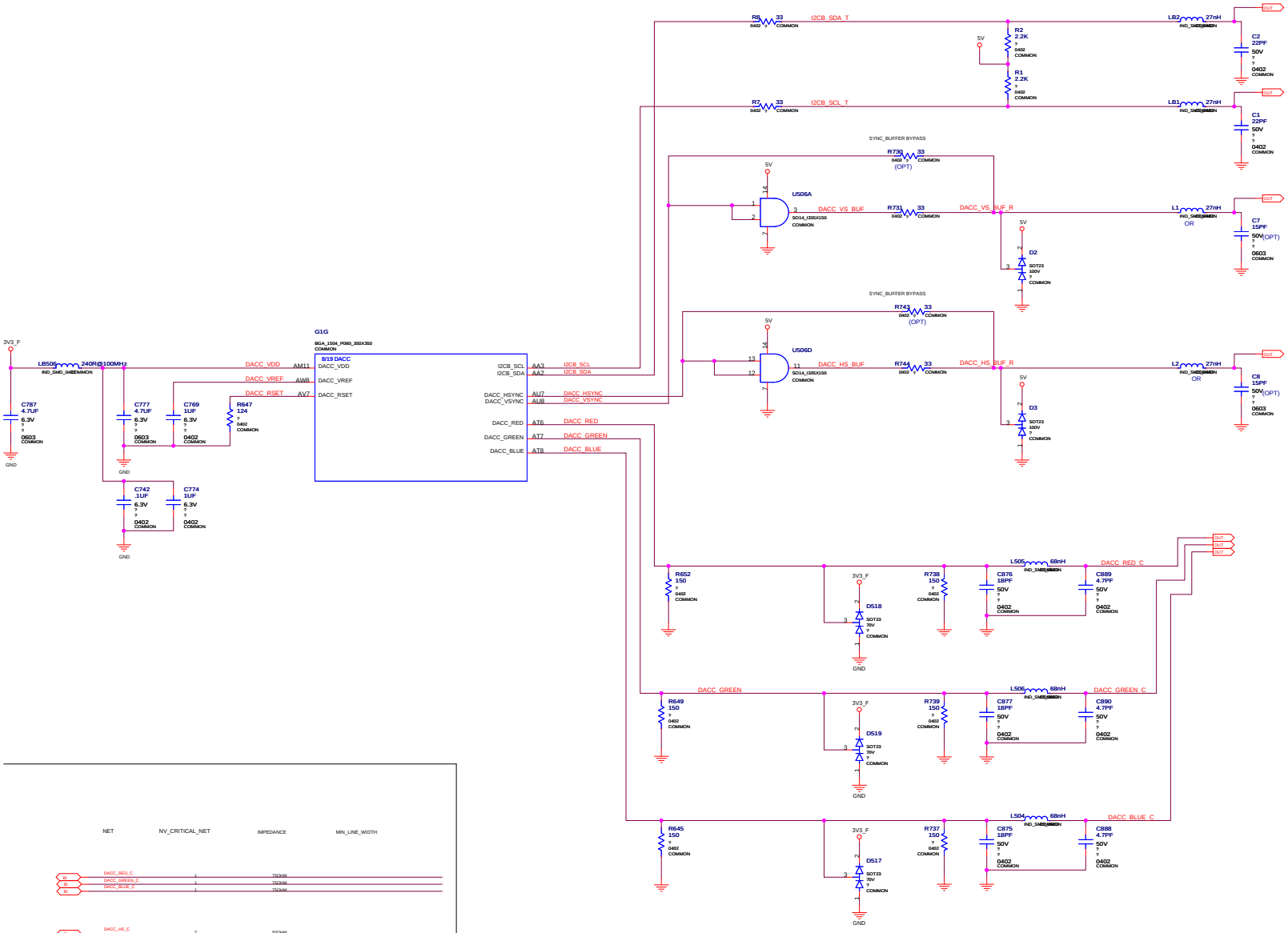
Page15: DACC Interface

DACC RGB-FILTER



ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC Interface

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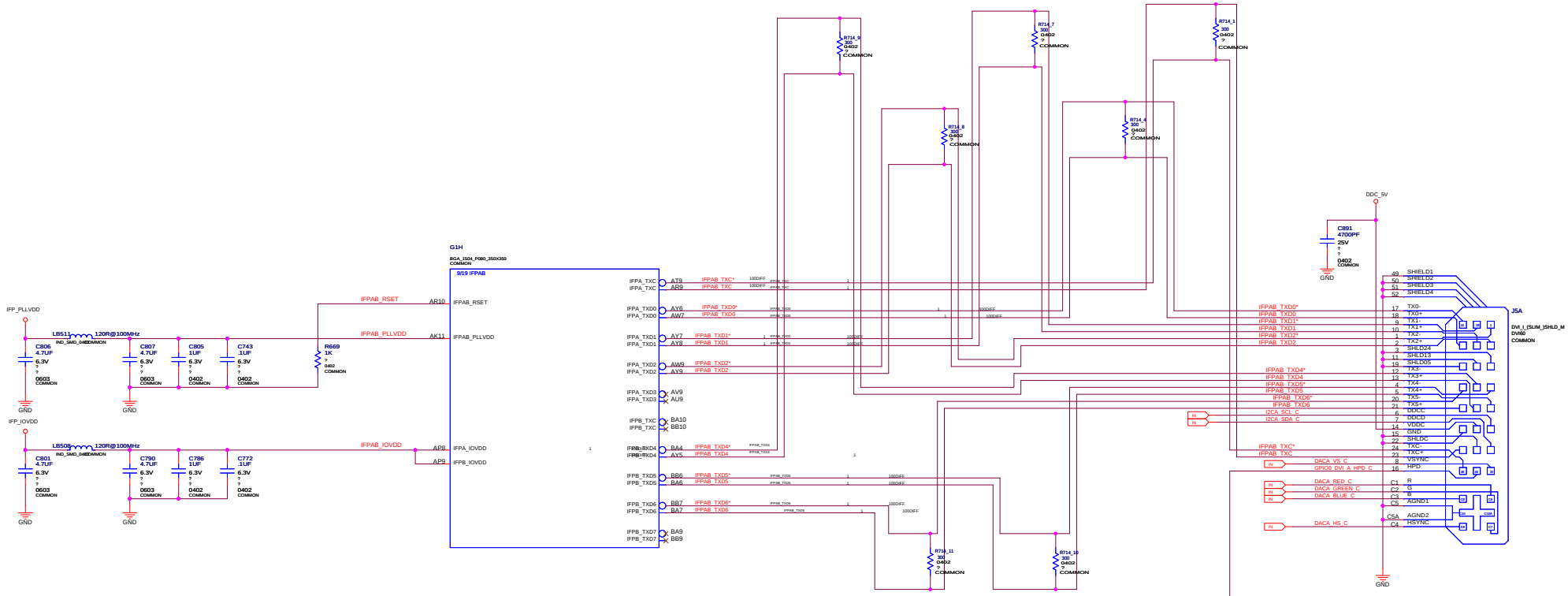
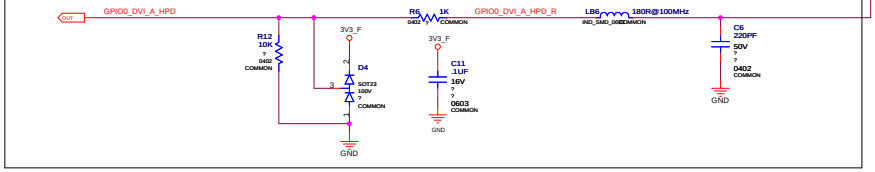
Date: Wednesday, June 18, 2008	Sheet 15 of 38		

Page16: IFP A/B Interface -- DVI Connector South



DVIAB Hotplug Detection



ASSEMBLY	PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP A/B Interface -- DVI Connector South

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Size: Custom	Document Number: <Doc>	Rev: <RevCode>	
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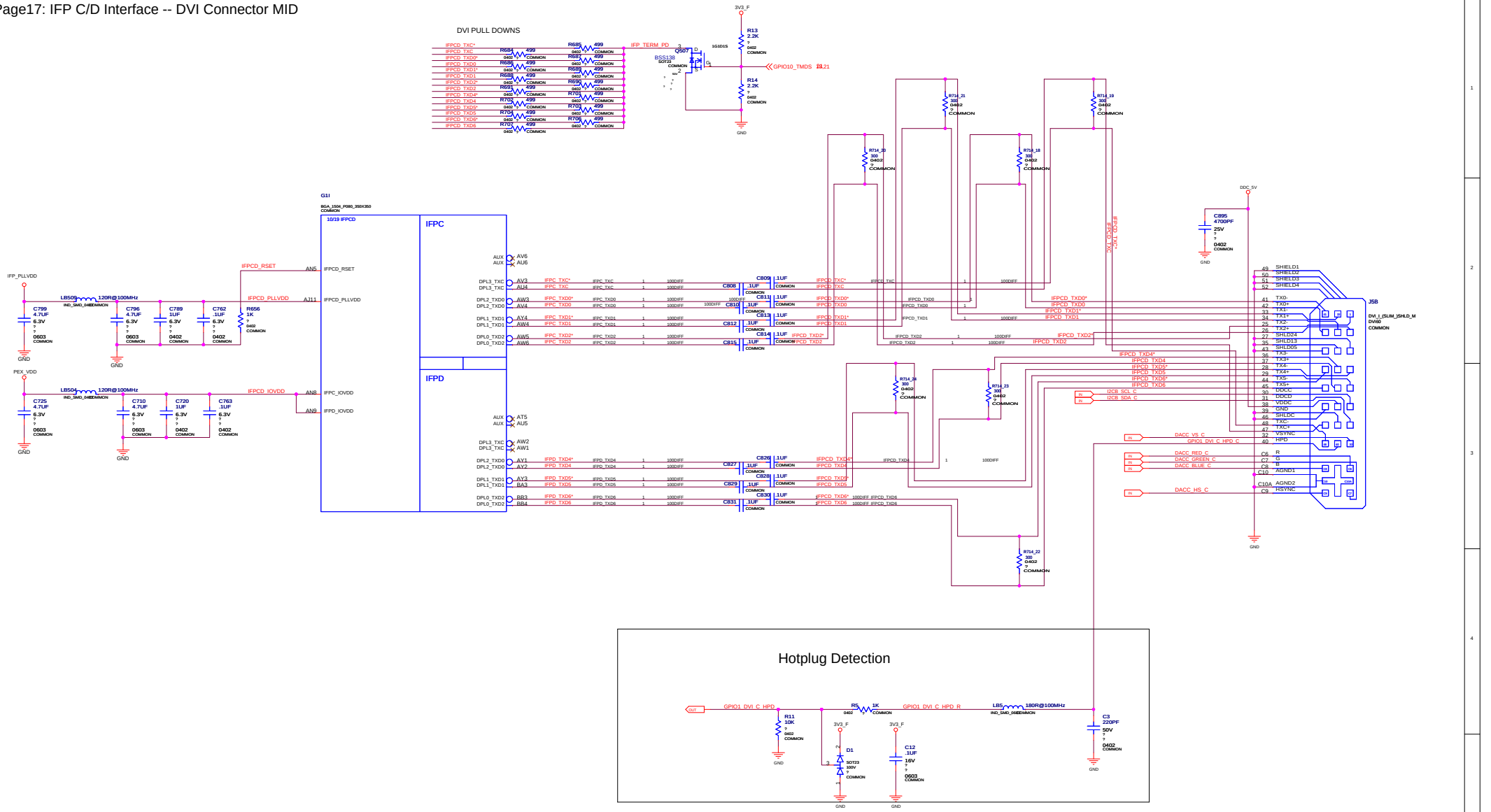
Page17: IFP C/D Interface -- DVI Connector MID



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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP C/D Interface -- DVI Connector MID

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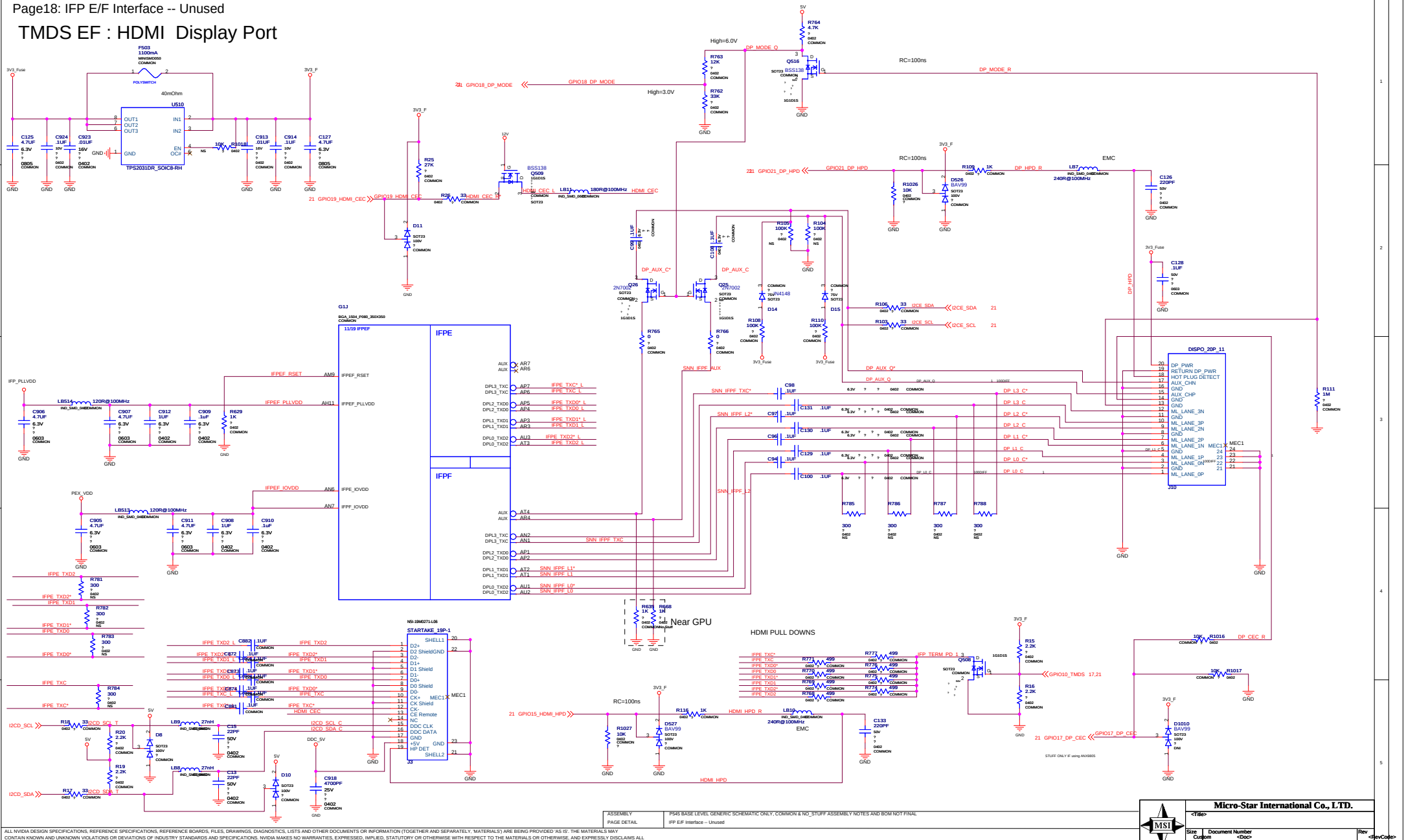
<Title>

Size	Document Number	Rev
Custom	<Doc>	<FevCode>

Date: Wednesday, June 18, 2008 Sheet 17 of 38

Page18: IFP E/F Interface -- Unused

TMDS EF : HDMI Display Port



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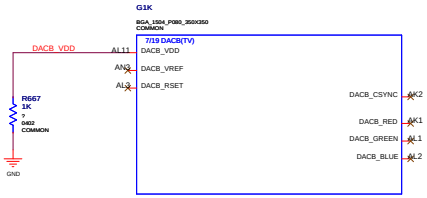
ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP E/F Interface -- Unused

Size: Custom	Document Number: <Doc>		Rev: <FevCode>
Date: Wednesday, June 18, 2008	Sheet 18 of 38		

Page19: DACB and HDTV/SDTV-Out

NET NET NV_CRITICAL_NET IMPEDANCE



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ASSEMBLY: PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL: DACB and HDTV/SDTV-Out

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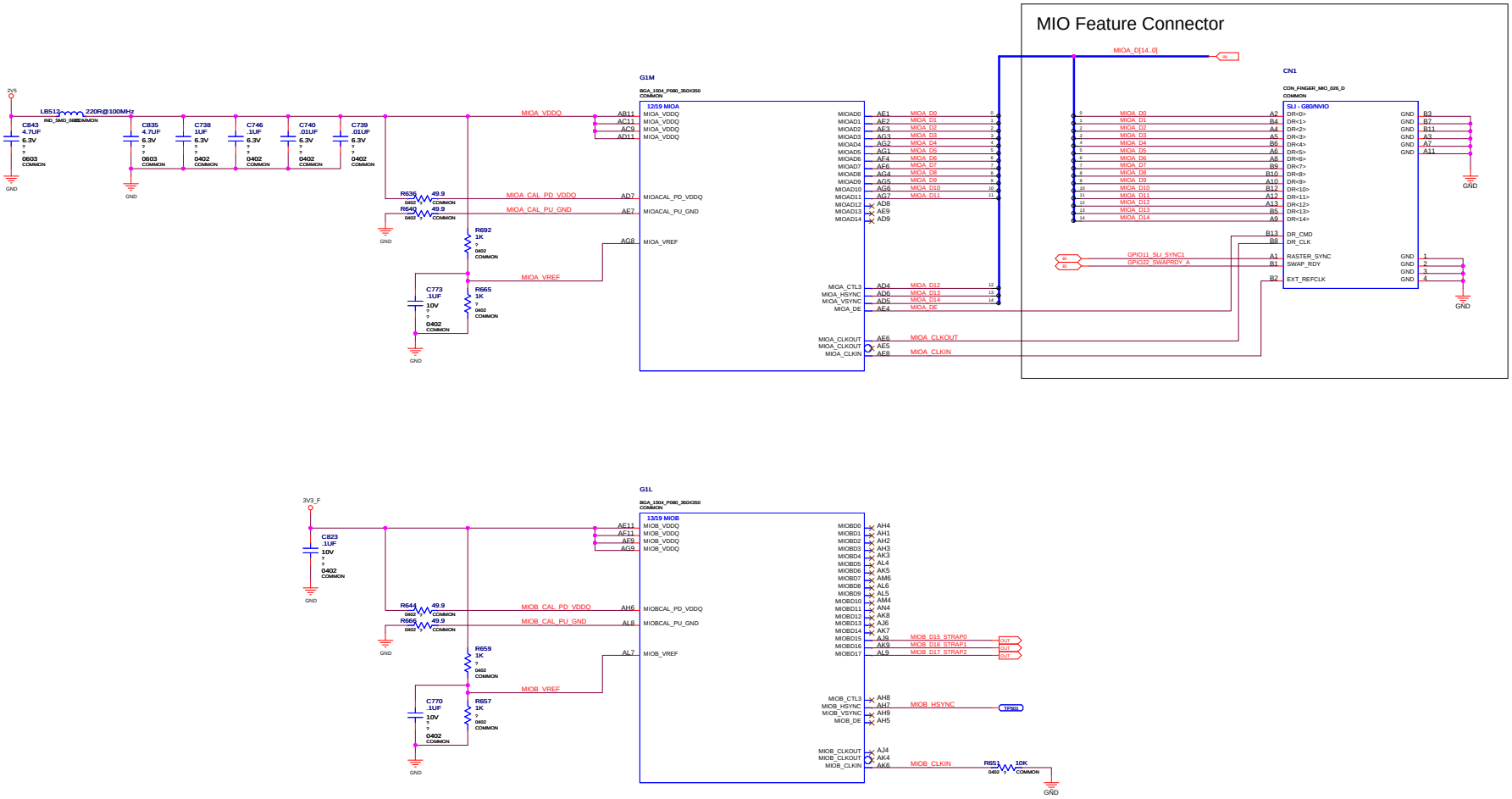
Date: Wednesday, June 18, 2008 | Sheet 19 of 36

Page20: MIO A/B Interface



NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
MIOA_D[14..0]	1	60ohm	

ASSEMBLY: PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: MIO A/B Interface

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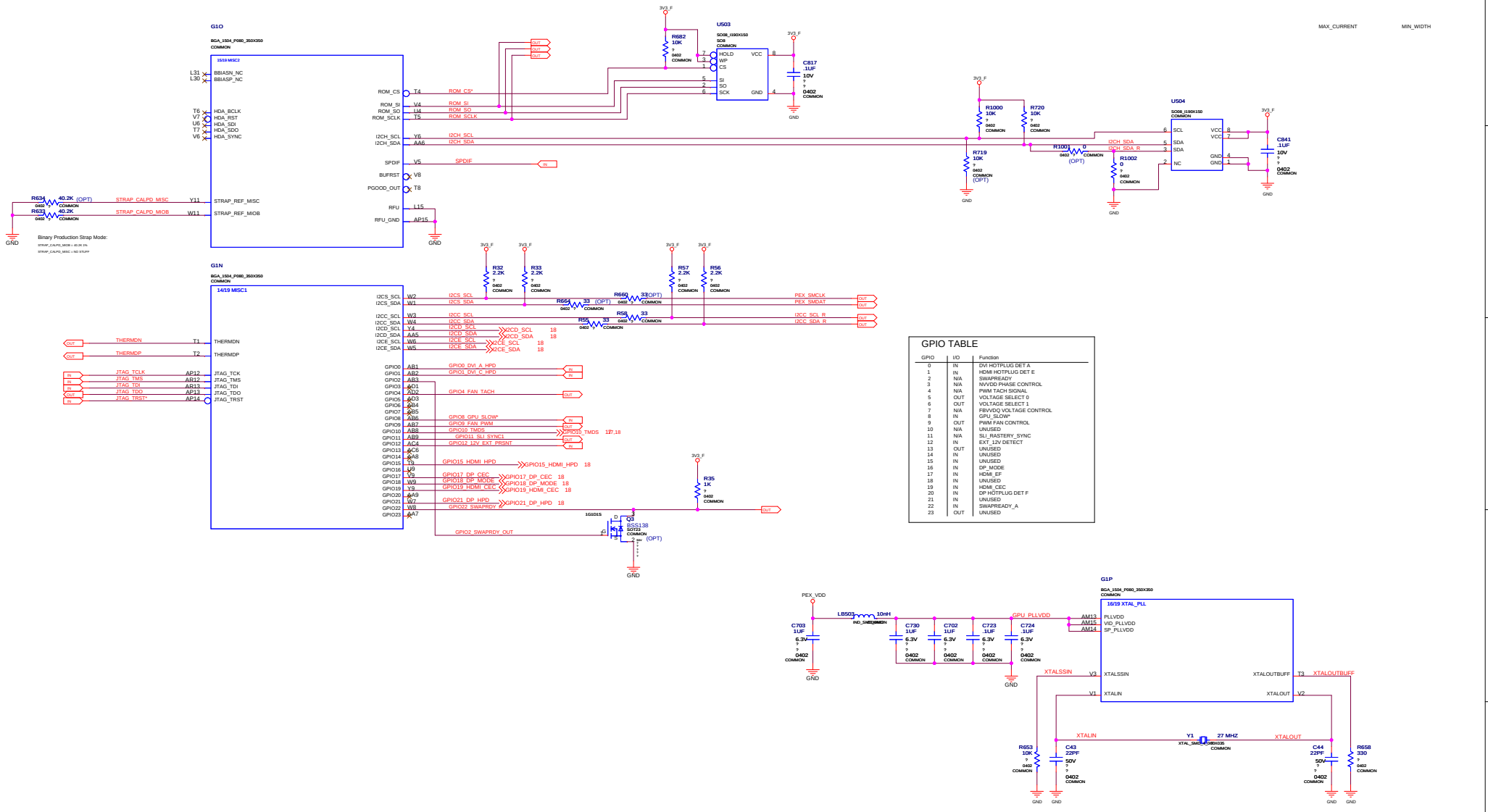
Date: Wednesday, June 18, 2008 | Sheet 20 of 38

Page21: MISC: GPIO, I2C, ROM, HDCP, and XTAL



GPIO TABLE

GPIO	I/O	Function
0	IN	DVI HOTPLUG DET A
1	IN	HDMI HOTPLUG DET E
2	N/A	SWAPREADY
3	N/A	NVVDD PHASE CONTROL
4	N/A	PWM TACH SIGNAL
5	OUT	VOLTAGE SELECT 0
6	OUT	VOLTAGE SELECT 1
7	N/A	FBVVDQ VOLTAGE CONTROL
8	IN	GPU_SLOW*
9	OUT	PWM FAN CONTROL
10	N/A	UNUSED
11	N/A	SLI_RASTERY_SYNC
12	IN	EXT_12V DETECT
13	OUT	UNUSED
14	IN	UNUSED
15	IN	UNUSED
16	IN	DP_MODE
17	IN	HDMI_EF
18	IN	UNUSED
19	IN	HDMI_CEC
20	IN	DP HOTPLUG DET F
21	IN	UNUSED
22	IN	SWAPREADY_A
23	OUT	UNUSED

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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO, I2C, ROM, HDCP, and XTAL

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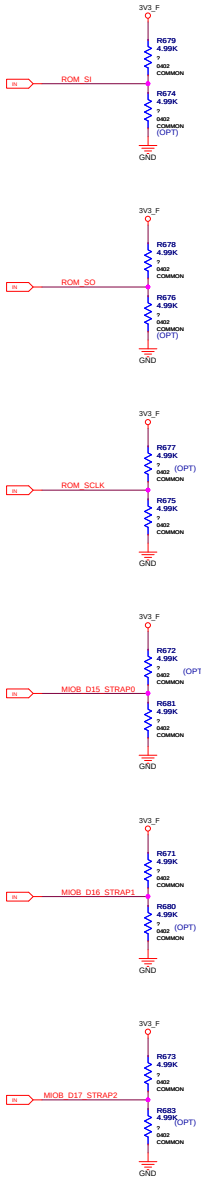
<Title>

Size: Custom | Document Number: <Doc> | Rev: <FevCode>

Date: Wednesday, June 18, 2008 | Sheet 21 of 38

Page22: Strap Configuration



STRAP PIN	STRAP NAME
ROM_SI	PCI_DEVID_EXT

STRAP PIN	STRAP NAME
ROM_SO	SLOT_CLK_CFG

STRAP PIN	STRAP NAME
ROM_SCLK	PCI_DEVID[3]

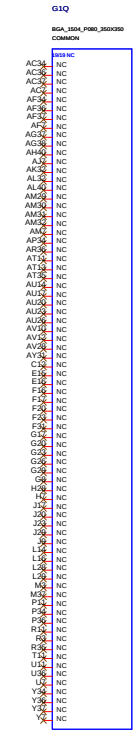
STRAP PIN	STRAP NAME
STRAP0	RAMCFG0
STRAP1	RAMCFG1
STRAP2	RAMCFG2

* RAMCFG[2:0]

256MB (8Mx32)	512MB (16Mx32)	1024MB (32Mx32)
101 --- 256-bit Qimonda 110 --- 256-bit Hynix 111 --- 256-bit Samsung	001 --- 256-bit Qimonda 010 --- 256-bit Hynix 011 --- 256-bit Samsung	101 --- 256-bit Qimonda 110 --- 256-bit Hynix 111 --- 256-bit Samsung

* VBIOS will be defined on a per SKU basis.

	3V3	GND
5K	1	0



ASSEMBLY: PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL: Strap Configuration

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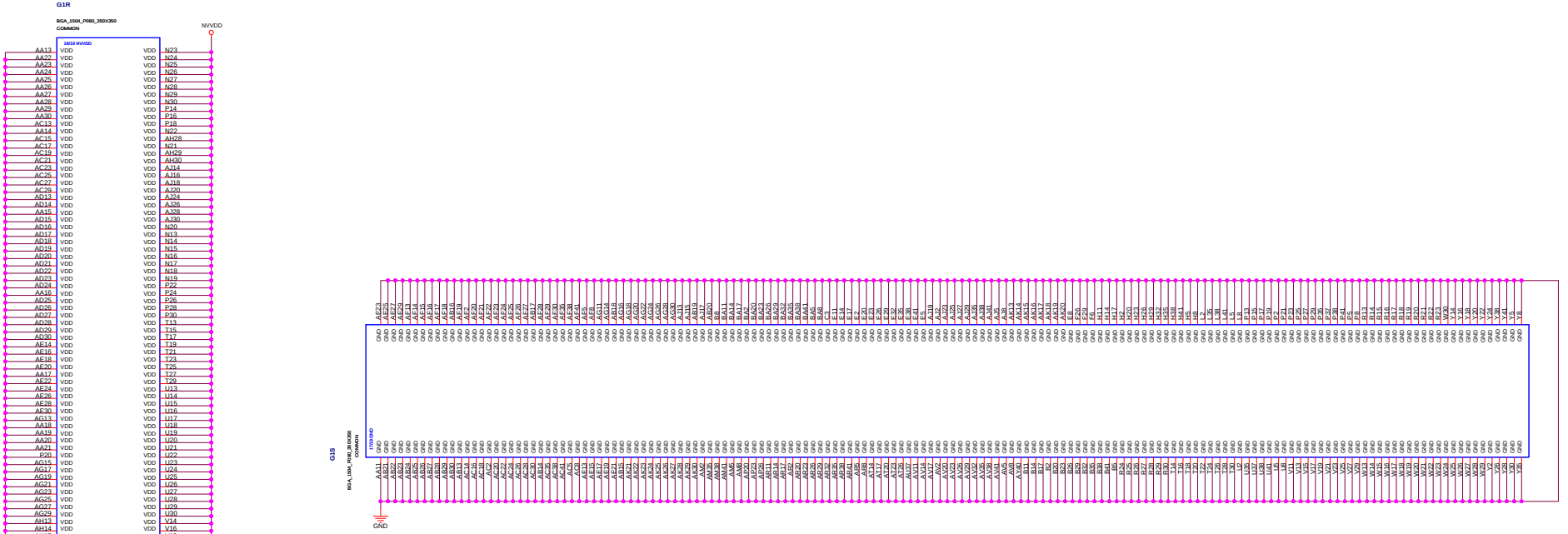
Page23: PWR and GND Signals



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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PWR and GND Signals

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Size	Document Number	Rev
Custom	<Doc>	<FevCode>

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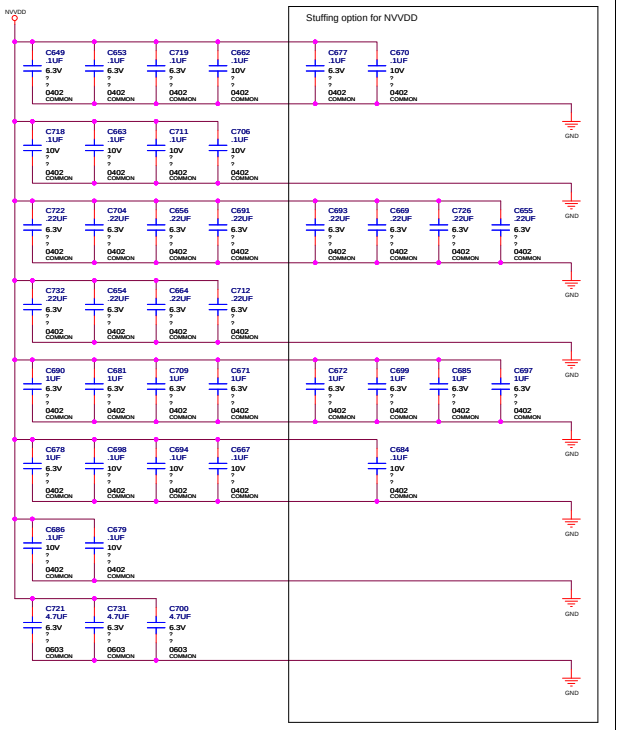
Page24: NVVDD and FBVDDQ Decoupling

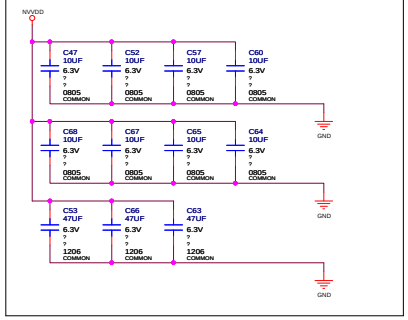
NVVDD

Place under GPU



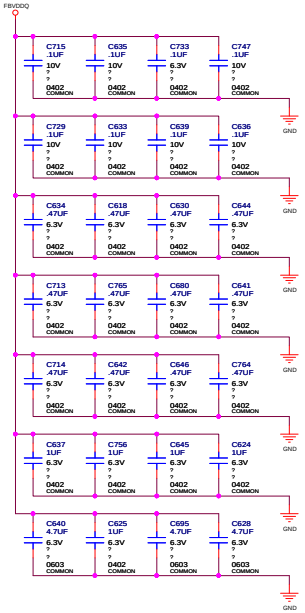
NVVDD

Place close to GPU



FBVDDQ

Place near BGA



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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	NVVDD and FBVDDQ Decoupling

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<Title>

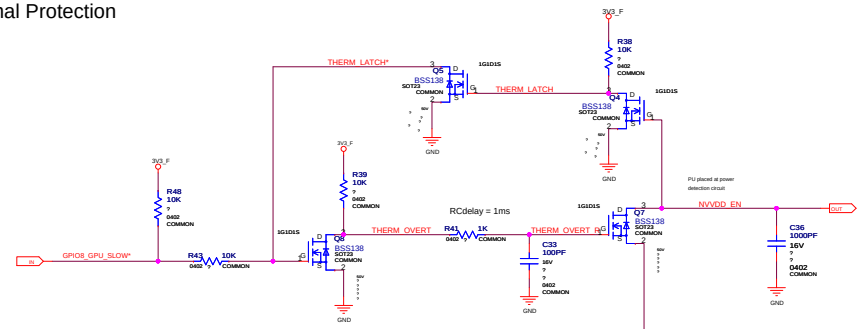
Size	Document Number	Rev
Custom	<Doc>	<FevCode>

Date: Wednesday, June 18, 2008 Sheet 24 of 36

Page25: SPDIF Input, Thermal Protection, and IFP_IOVDD Power Supply

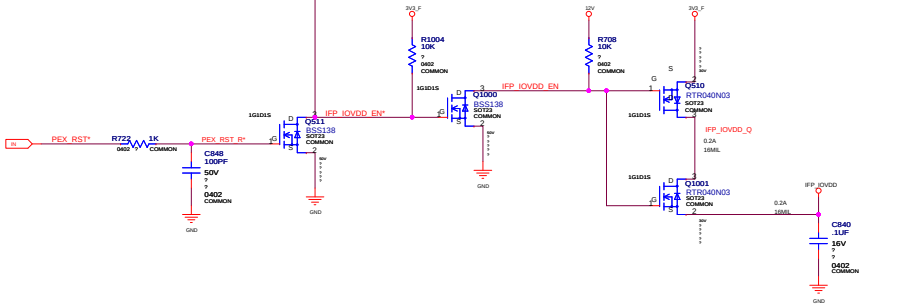
NET	IMPEDANCE	NV_CRITICAL_NET
SPDIF	100HM	1

Thermal Protection

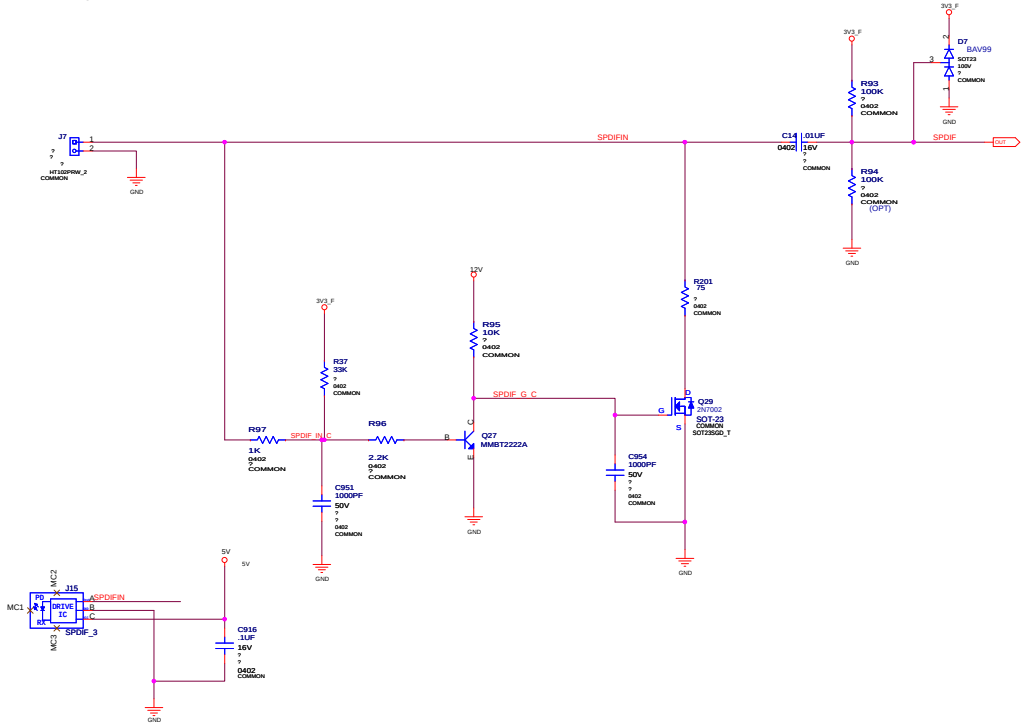


IFP_IOVDD Backdrive Prevention

Stuffing posibilities for thermal control and protection:



SPDIF Input



ASSEMBLY: PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: SPDIF Input, Backdrive Protection, and IFP_IOVDD Power Supply

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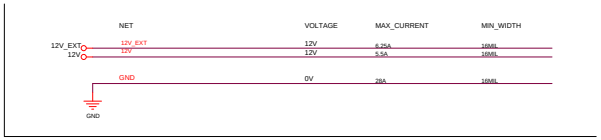
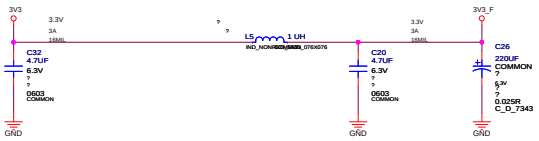
<Title>	
Size: Custom	Document Number: <Doc>
Rev: <FevCode>	
Date: Wednesday, June 18, 2008	Sheet 25 of 36

Page26: PS I: 3V3, 12V, and 12V_EXT Power Supply Filter



3V3 Power Supply Filter

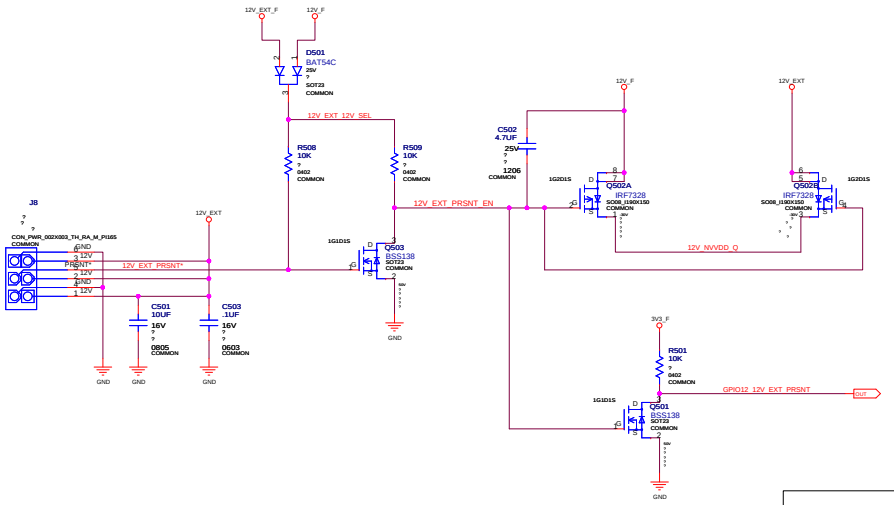
3V3_F = 3.3V @ 2.5A



12V Power Supply Filter

12V_F = 12V @ 5.5A

INPUT POWER SELECTION for NVVDD



	GPIO12
EMERENCY MODE (12V_EXT present)	0
150W POWER MODE (12V_EXT NOT present)	1

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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS I: 3V3, 12V, and 12V_EXT Power Supply Filter

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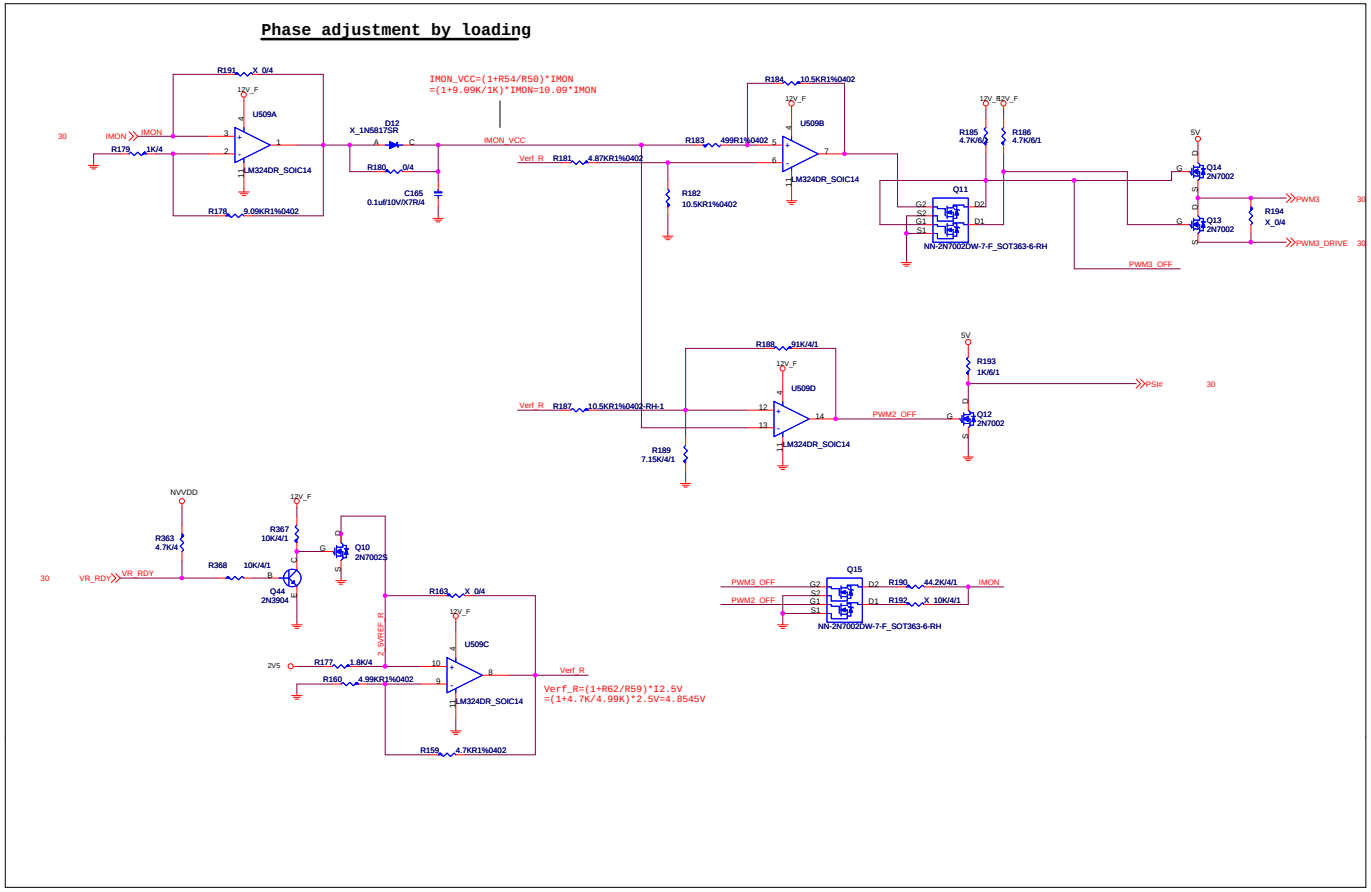
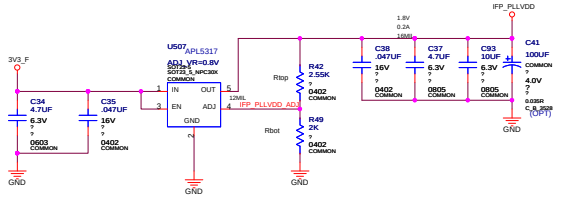
Page27: PS II: IFP_PLLVDD, 2V5, 5V, and DDC_5V Power Supply



IFP_PLLVDD Power Supply

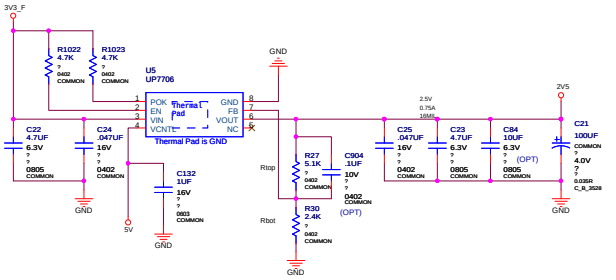
IFP_PLLVDD = 1.8V @ 200mA



IFP_PLLVDD = VREF * (1 + (Rtop / Rbot))
1.82V = 0.8V * (1 + (2.5K/2K))

2V5 Power Supply

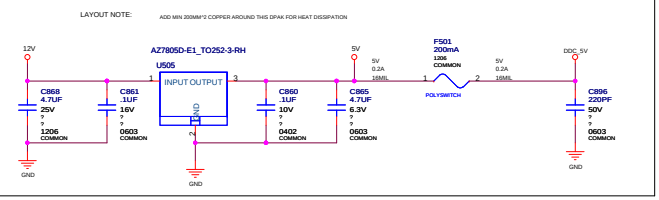
2V5 = 2.5V @ 750mA

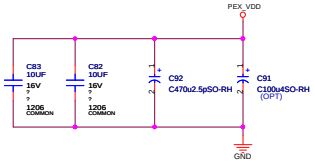


2V5 = VREF * (1 + (Rtop / Rbot))
2.5V = 0.8V * (1 + (5.1K/2.4K))

5V and DDC_5V Power Supply

DDC_5V = 5V @ 200mA





ASSEMBLY	PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS II PEX_VDD, IFP_PLLVDD, 2V5, 5V, and DDC_5V Power Supply

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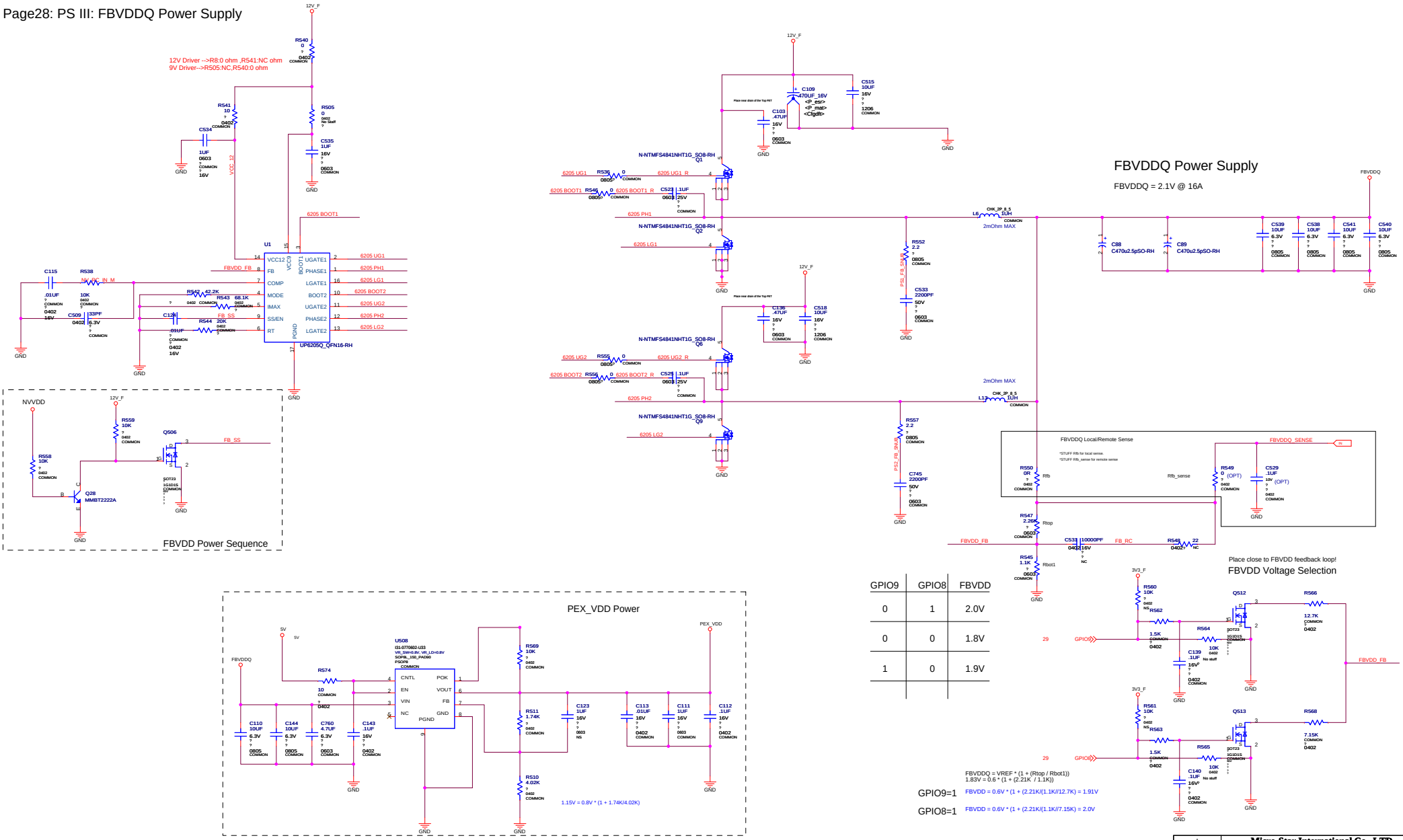
Page28: PS III: FBVDDQ Power Supply



GPIO9	GPIO8	FBVDD
0	1	2.0V
0	0	1.8V
1	0	1.9V

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ASSEMBLY	PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS III: FBVDDQ Power Supply

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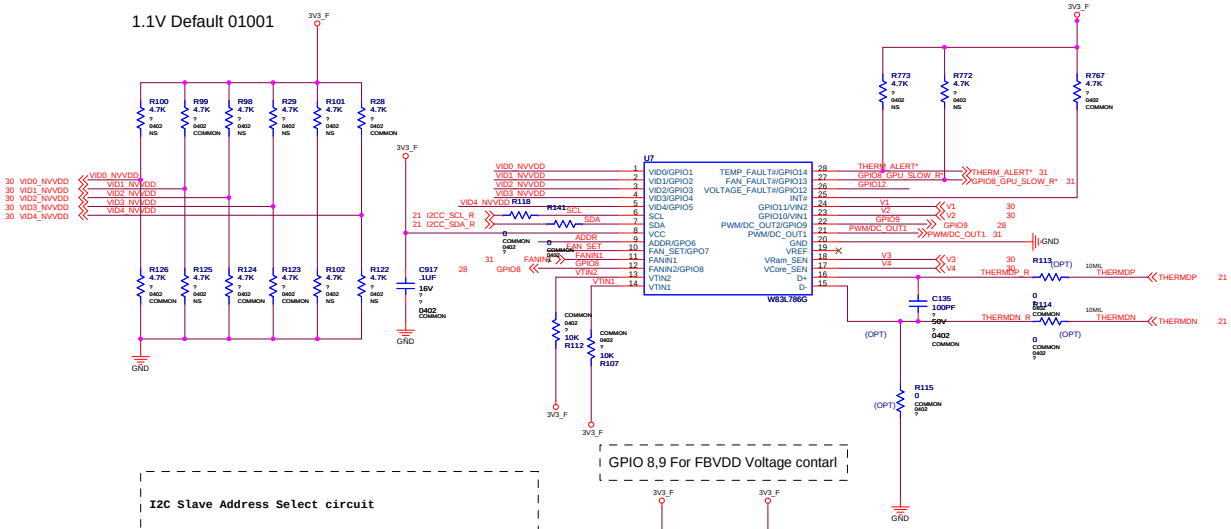
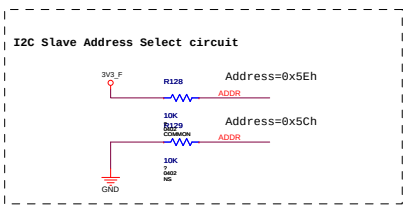
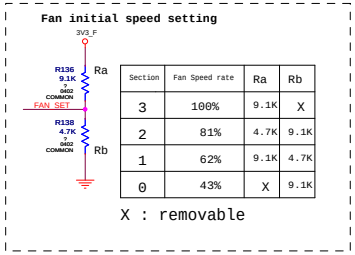
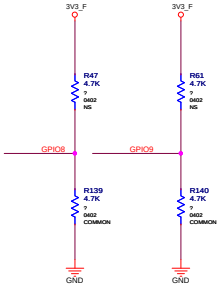
Page29: Winbond HW Monitor



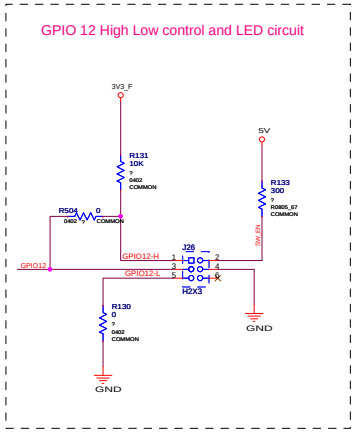




Section	Fan Speed rate	Ra	Rb
3	100%	9.1K	X
2	81%	4.7K	9.1K
1	62%	9.1K	4.7K
0	43%	X	9.1K



GPIO 8,9 For FBVDD Voltage contarl



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ASSEMBLY: PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: PS IV: NVVDD VID Control

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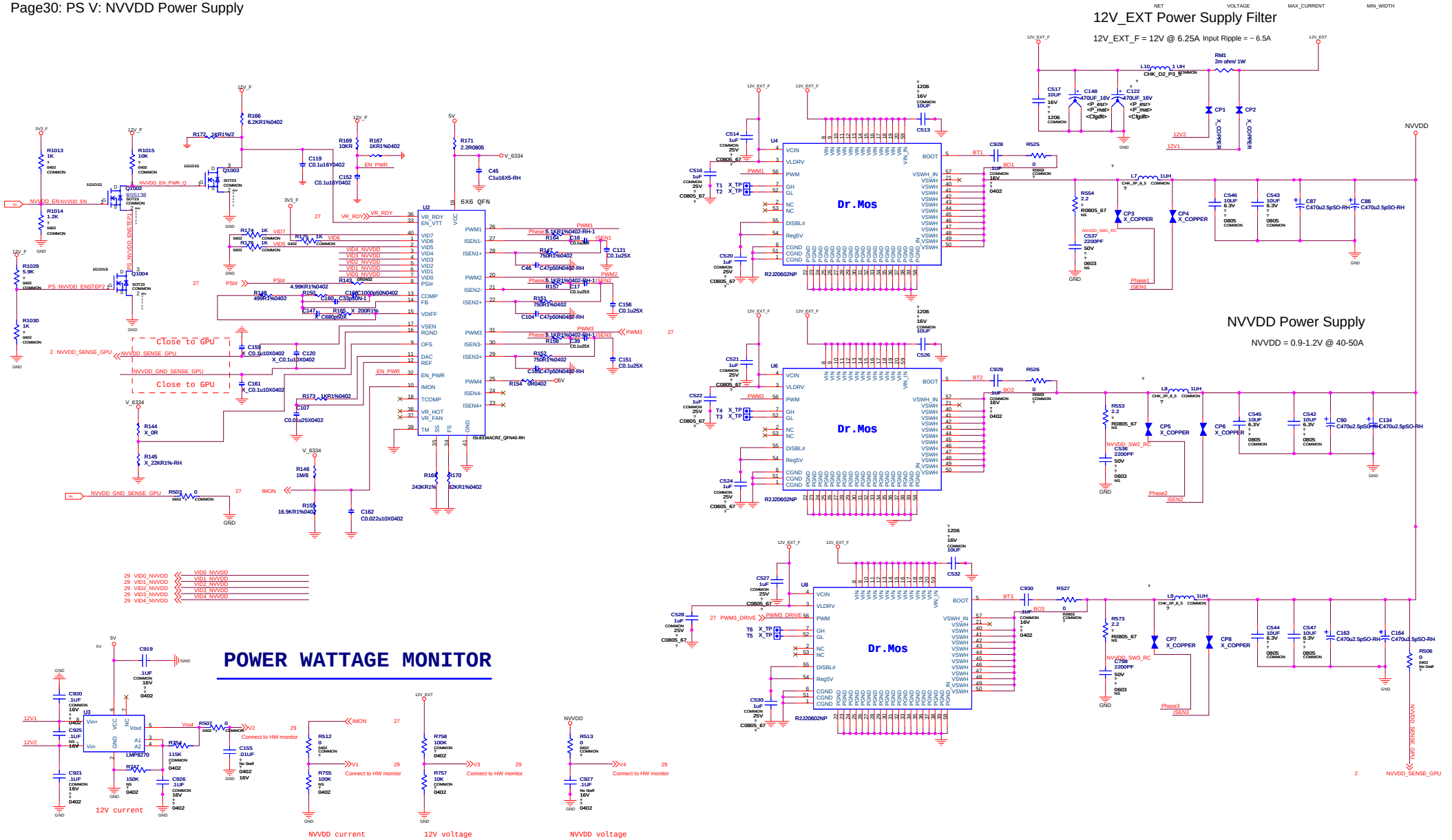
Page30: PS V: NVVDD Power Supply



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ASSEMBLY	PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS V: NVVDD Power Supply

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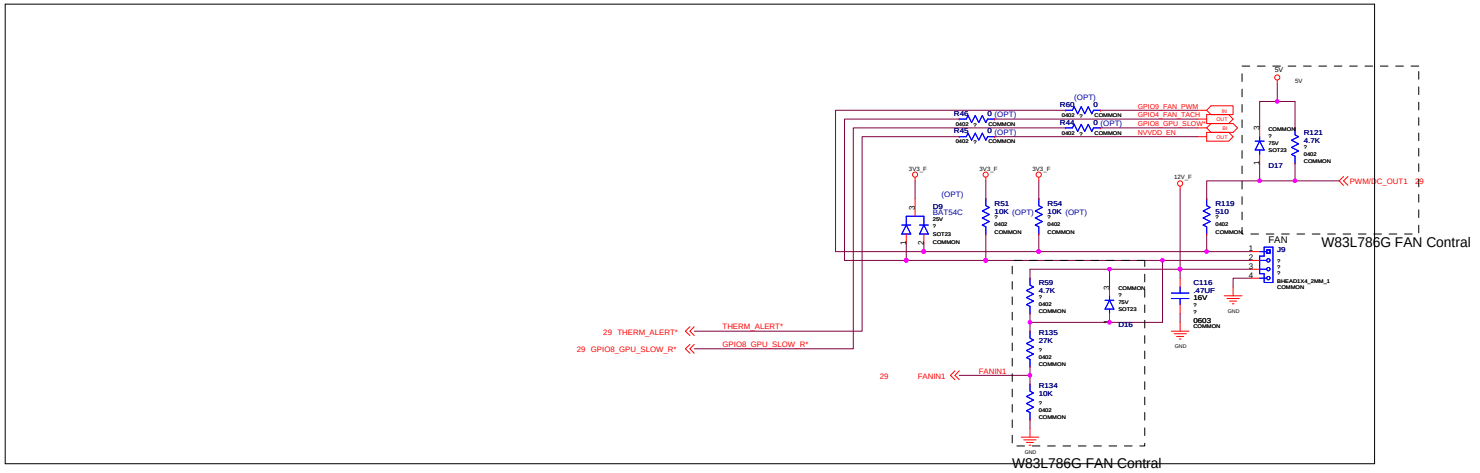
Page31: Thermal Diode and Fan Control



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PAGE DETAIL	Thermal Diode and Fan Control	

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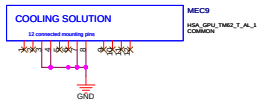
Page32: Thermal, Mechanical, and Bracket

Thermal



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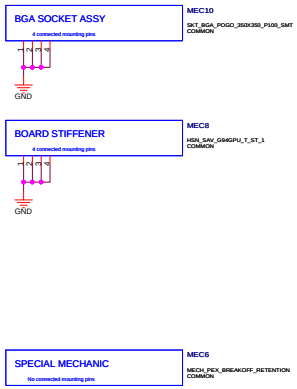
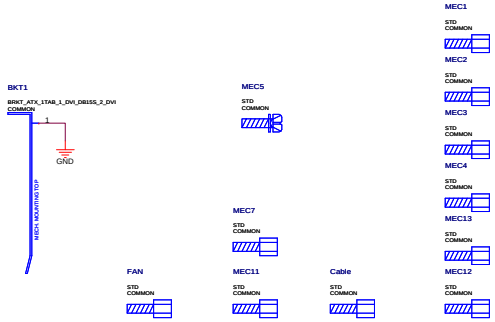
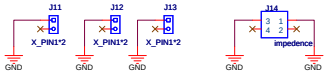
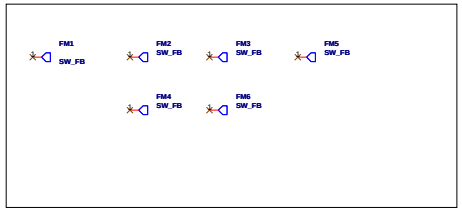


Bracket







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PAGE DETAIL	Thermal, Mechanical, and Bracket

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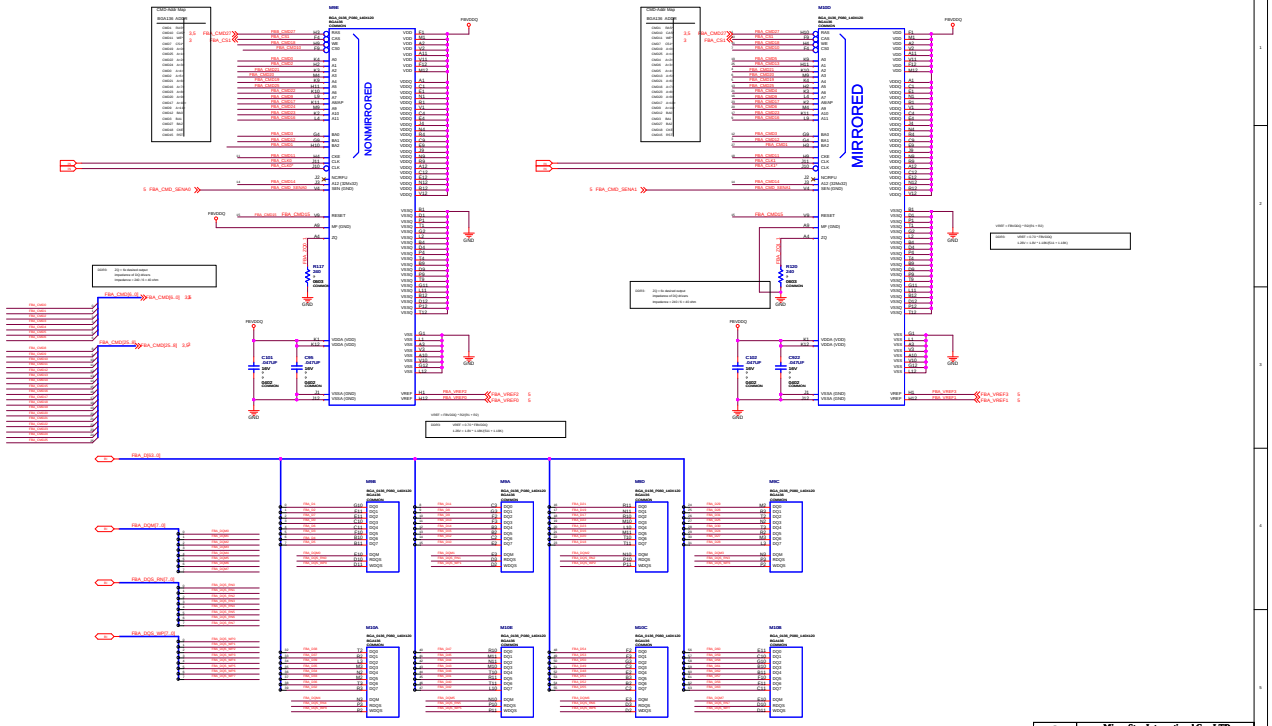
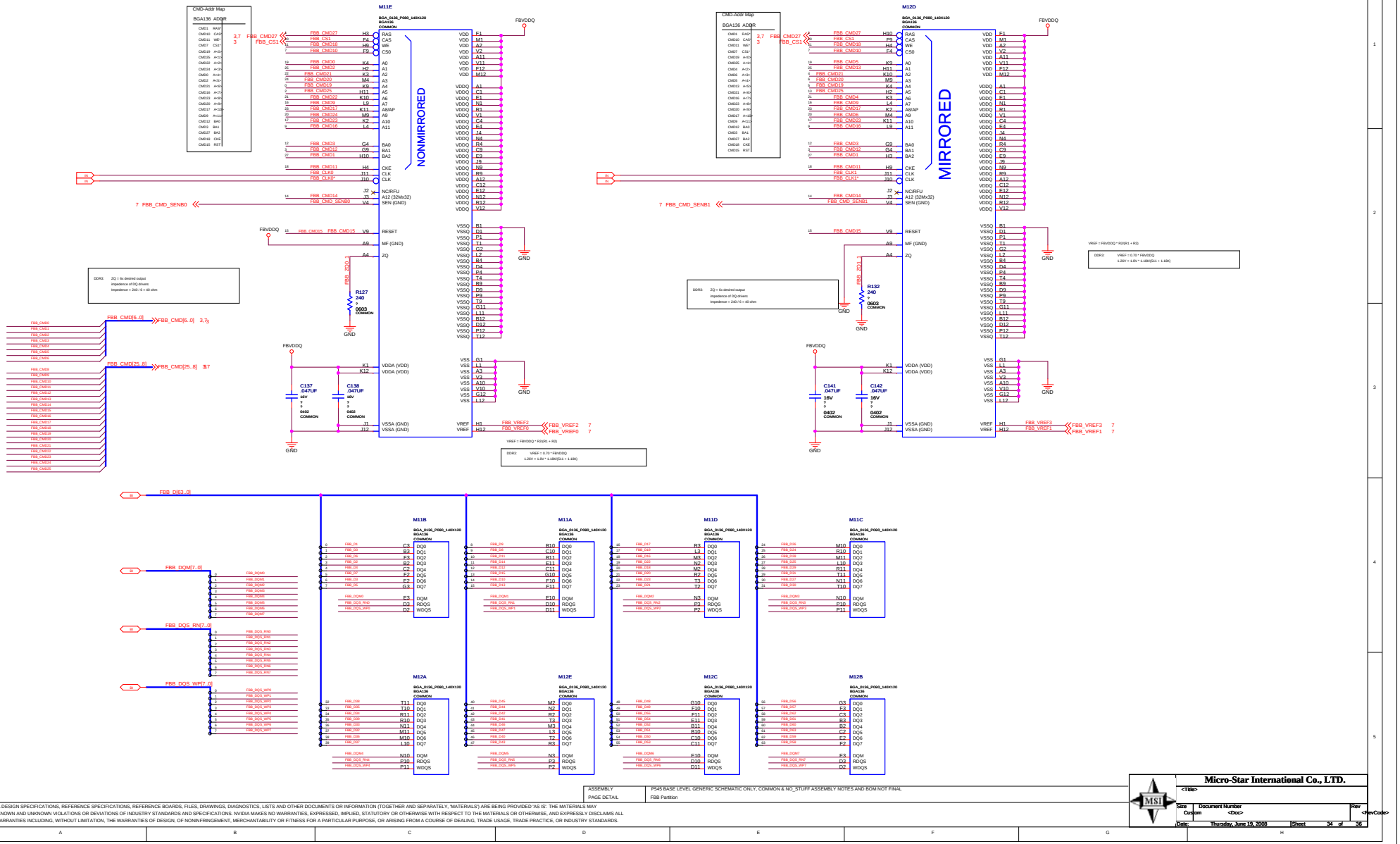
Page33: FBA-1 Partition



Page34: FBB-1 Partition



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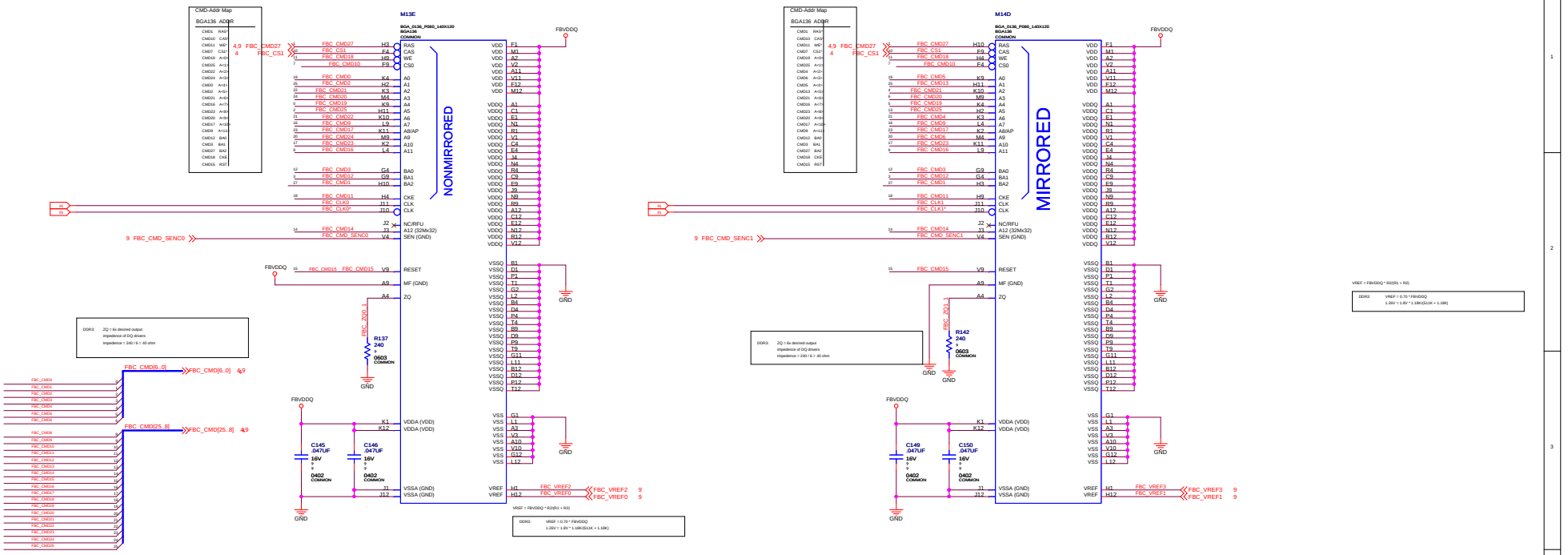
Page35 : FBC-1 Partition



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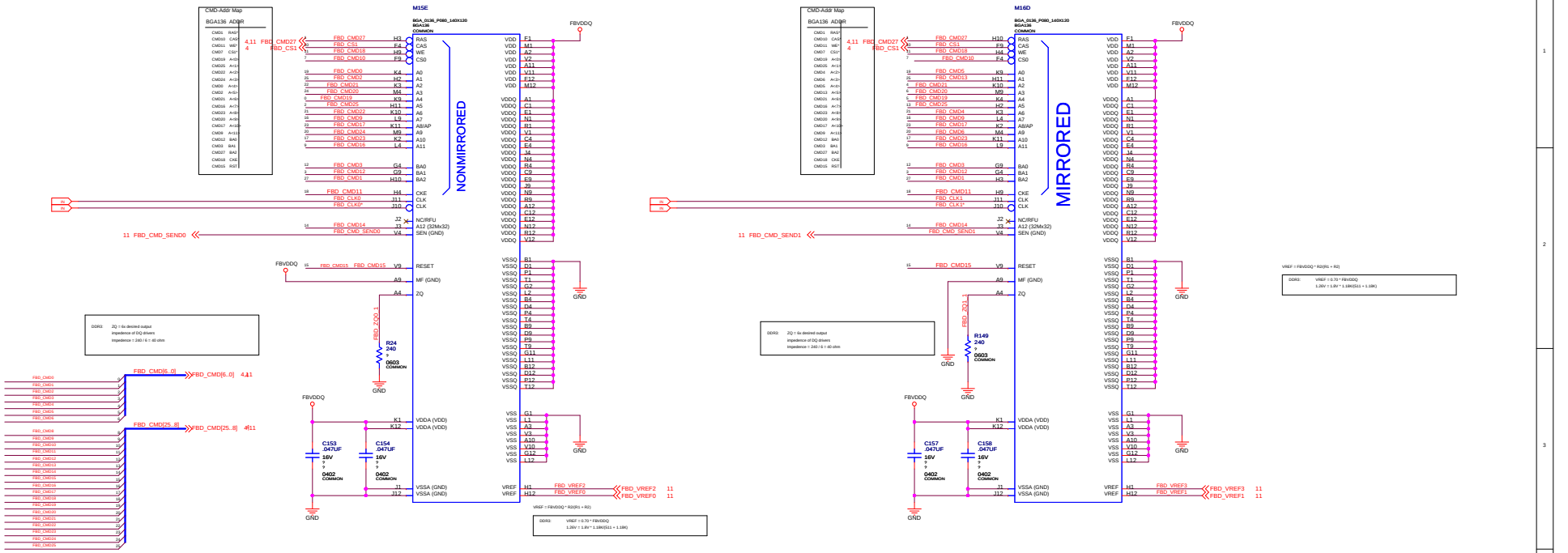
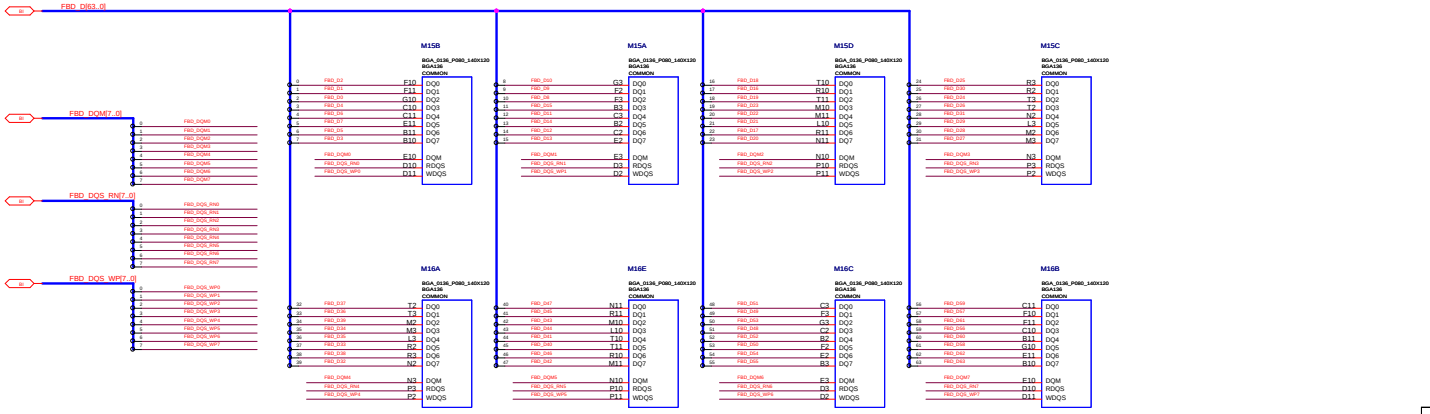
Page36: FBD-1 Partition





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