

MS-V041 VER 0A

NV43-PCIE NV43 128MB/64bit, BGA 16MX16 DDR2,VGA,DVI-I,TV-OUT(HT-10)

P295-A00 DESIGN NV43 300/267MHZ 128MB/256MB/512MB DDR2 84-FBGA

PAGE SUMMARY:

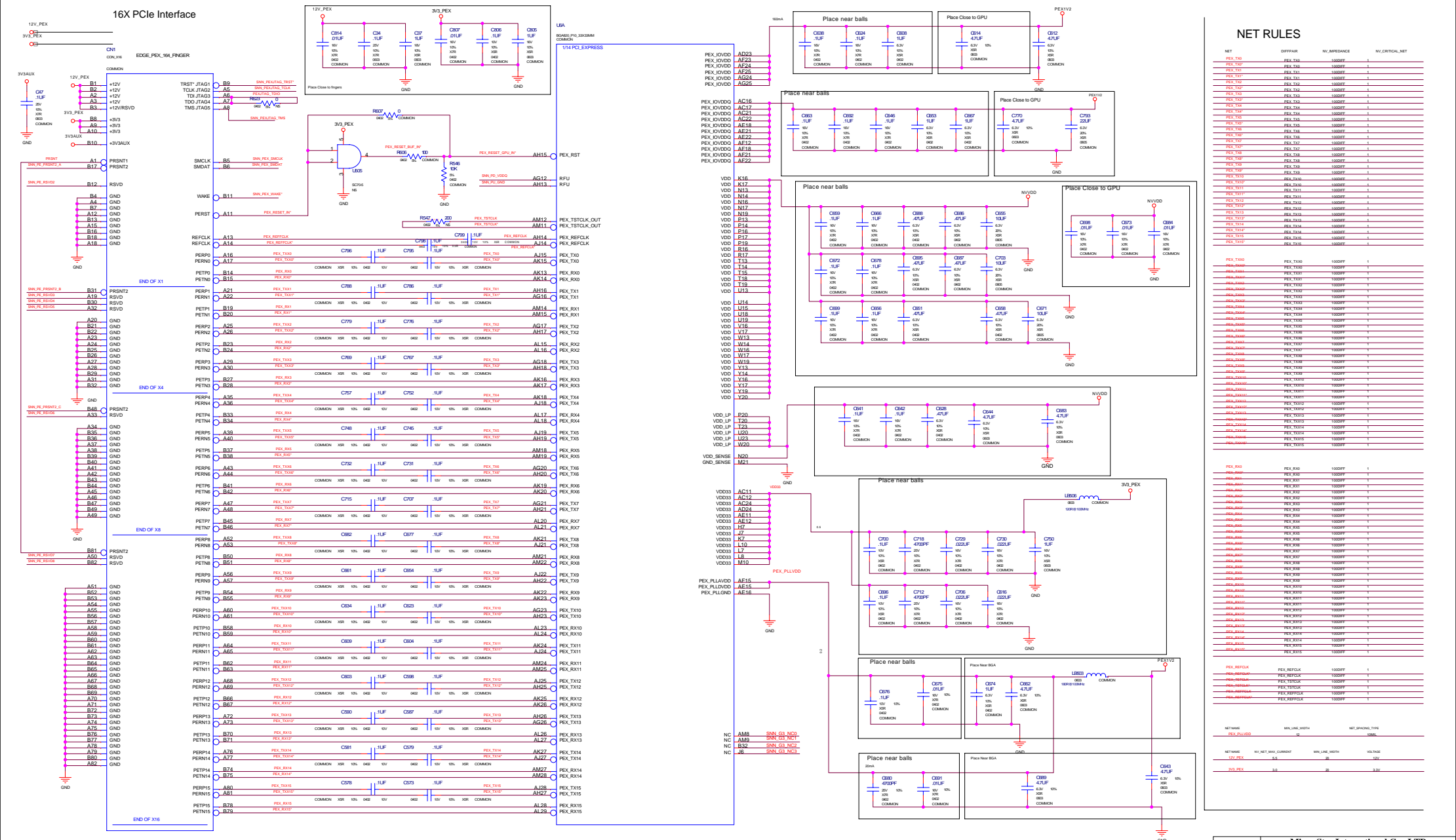
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REV HISTORY

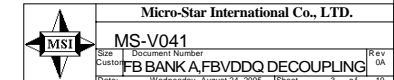
A00
-08/04/2005:

REV	VARIANT	NVPN	ASSEMBLY
0	BASE	80210295-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU00	80210295-0000-000	GF-6600-AD4 GEN 300267MHZ 256MB 84-FBGA DDR2 16MX16 VGA+DVI+HDTV
2	SKU01	80210295-0001-000	GF-6600-AD4 GEN 300267MHZ 128MB 84-FBGA DDR2 16MX16 VGA+DVI+HDTV
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02 PCI EXPRESS, NVVDD, VDD33

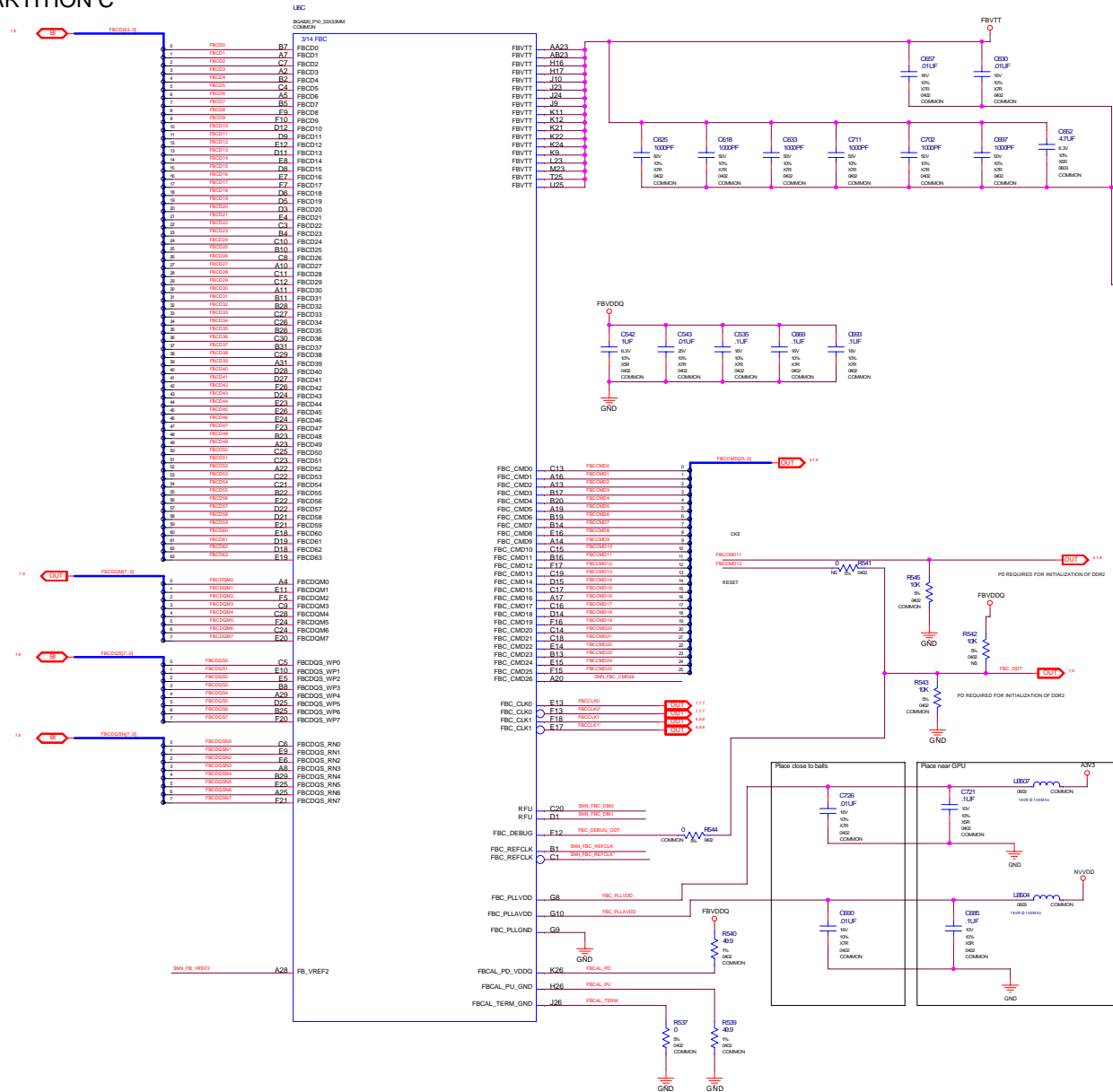


FB PARTITION A

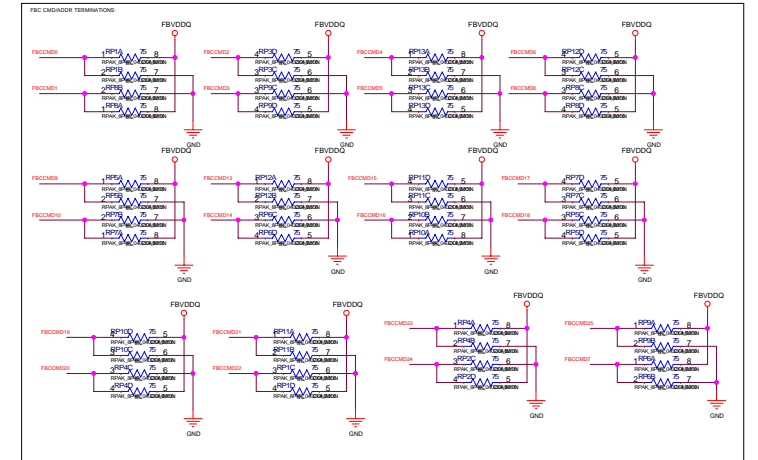


04 FB BANK C, FBVTT TERMINATIONS

FB PARTITION C



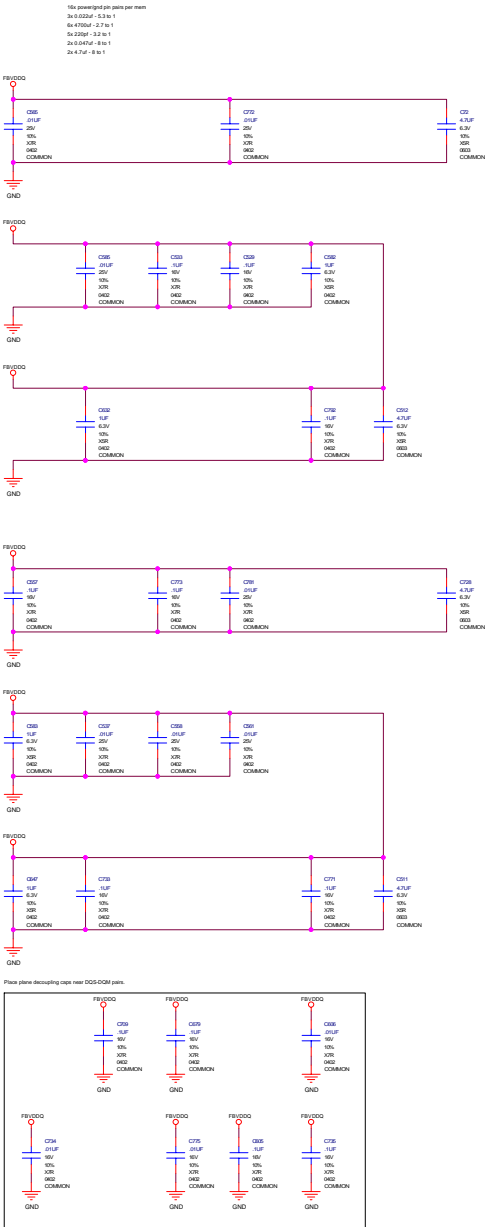
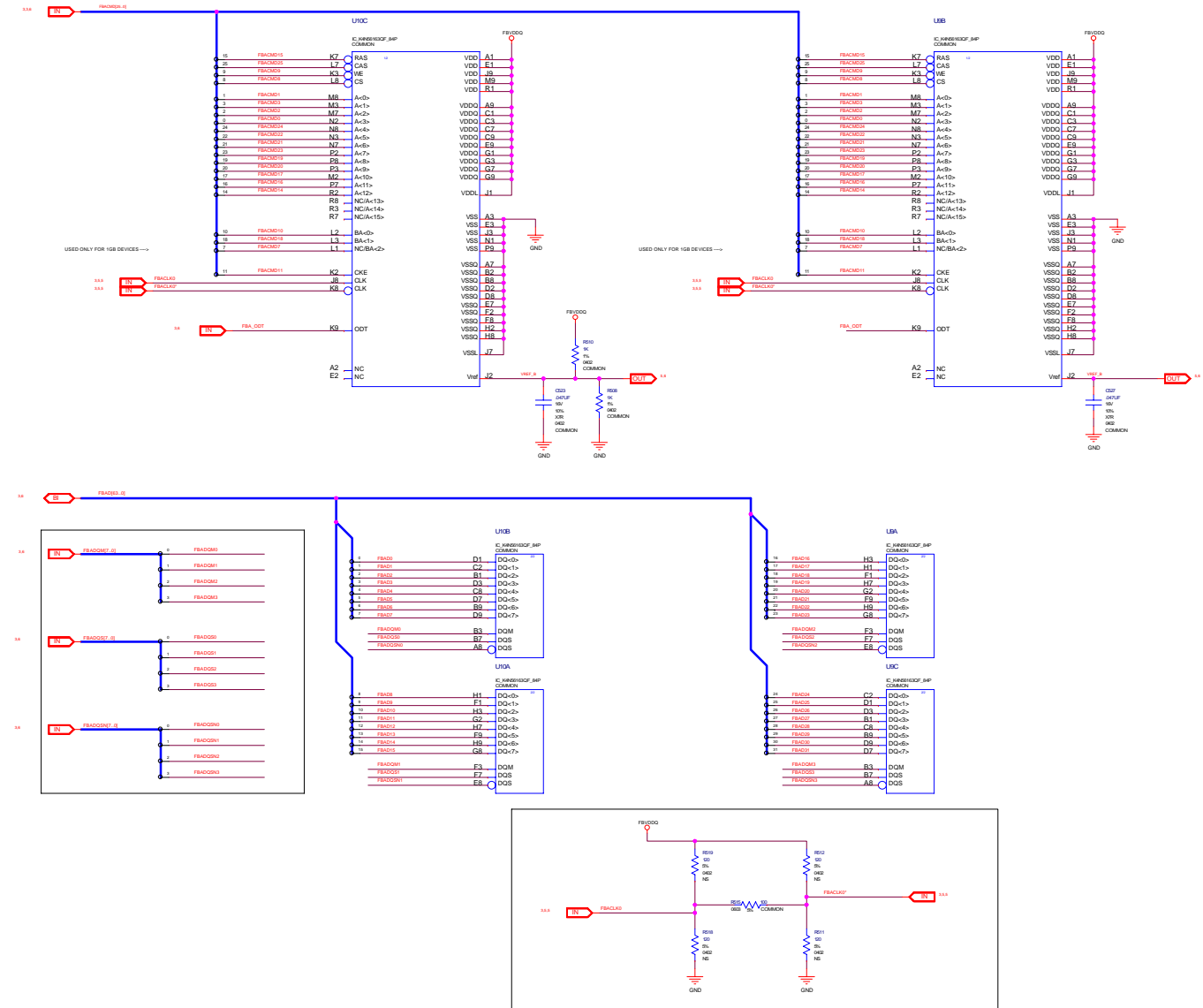
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FBVTT1	FBVTT1	1000FT	1	
FBVTT2	FBVTT2	1000FT	1	
FBVTT3	FBVTT3	1000FT	1	
FBVTT4	FBVTT4	1000FT	1	
FBVTT5	FBVTT5	1000FT	1	
FBVTT6	FBVTT6	1000FT	1	
FBVTT7	FBVTT7	1000FT	1	
FBVTT8	FBVTT8	1000FT	1	
FBVTT9	FBVTT9	1000FT	1	
FBVTT10	FBVTT10	1000FT	1	
FBVTT11	FBVTT11	1000FT	1	
FBVTT12	FBVTT12	1000FT	1	
FBVTT13	FBVTT13	1000FT	1	
FBVTT14	FBVTT14	1000FT	1	
FBVTT15	FBVTT15	1000FT	1	
FBVTT16	FBVTT16	1000FT	1	
FBVTT17	FBVTT17	1000FT	1	
FBVTT18	FBVTT18	1000FT	1	
FBVTT19	FBVTT19	1000FT	1	
FBVTT20	FBVTT20	1000FT	1	
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FBVTT25	FBVTT25	1000FT	1	
FBVTT26	FBVTT26	1000FT	1	
FBVTT27	FBVTT27	1000FT	1	
FBVTT28	FBVTT28	1000FT	1	
FBVTT29	FBVTT29	1000FT	1	
FBVTT30	FBVTT30	1000FT	1	
FBVTT31	FBVTT31	1000FT	1	
FBVTT32	FBVTT32	1000FT	1	
FBVTT33	FBVTT33	1000FT	1	
FBVTT34	FBVTT34	1000FT	1	
FBVTT35	FBVTT35	1000FT	1	
FBVTT36	FBVTT36	1000FT	1	
FBVTT37	FBVTT37	1000FT	1	
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FBVTT66	FBVTT66	1000FT	1	
FBVTT67	FBVTT67	1000FT	1	
FBVTT68	FBVTT68	1000FT	1	
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FBVTT73	FBVTT73	1000FT	1	
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FBVTT94	FBVTT94	1000FT	1	
FBVTT95	FBVTT95	1000FT	1	
FBVTT96	FBVTT96	1000FT	1	
FBVTT97	FBVTT97	1000FT	1	
FBVTT98	FBVTT98	1000FT	1	
FBVTT99	FBVTT99	1000FT	1	



05 MEMORY PARTITION A 0.31

FBA MEMORY 1st bank 0.31

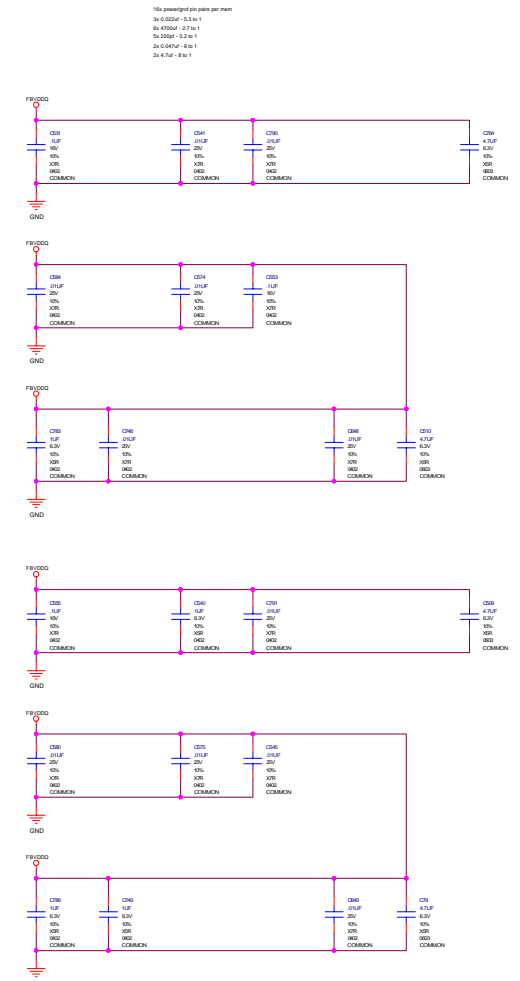
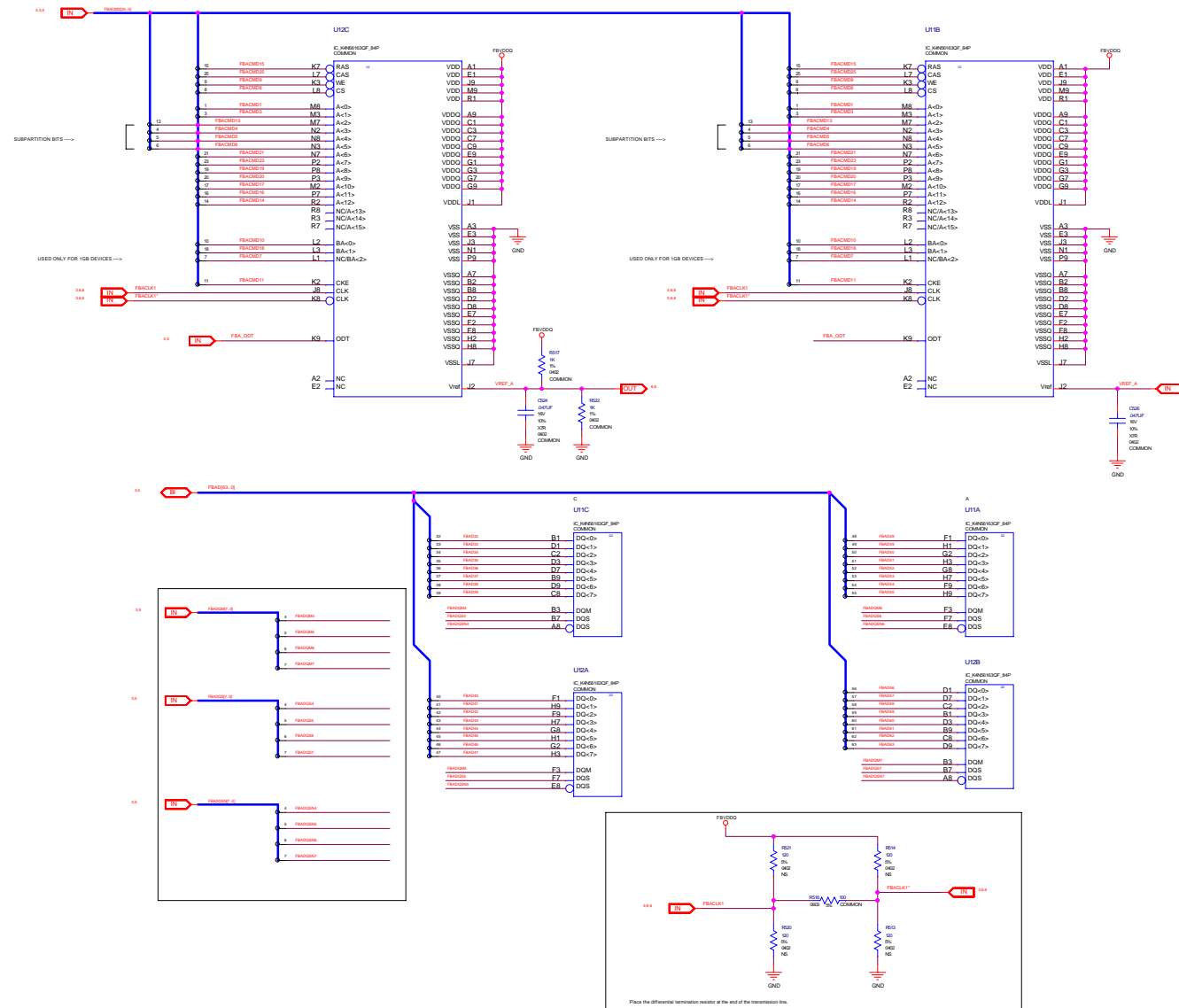
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



06 MEMORY PARTITION A 32..63

FBA MEMORY 1st bank 32..63

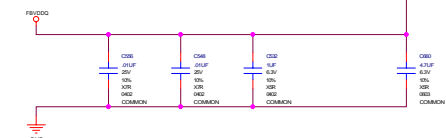
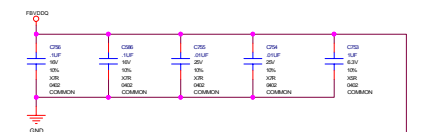
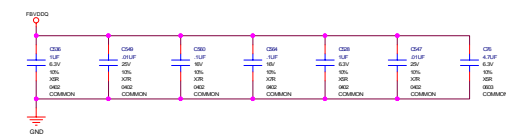
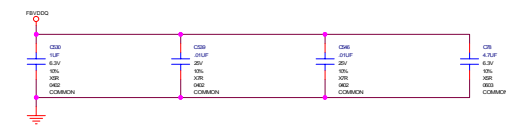
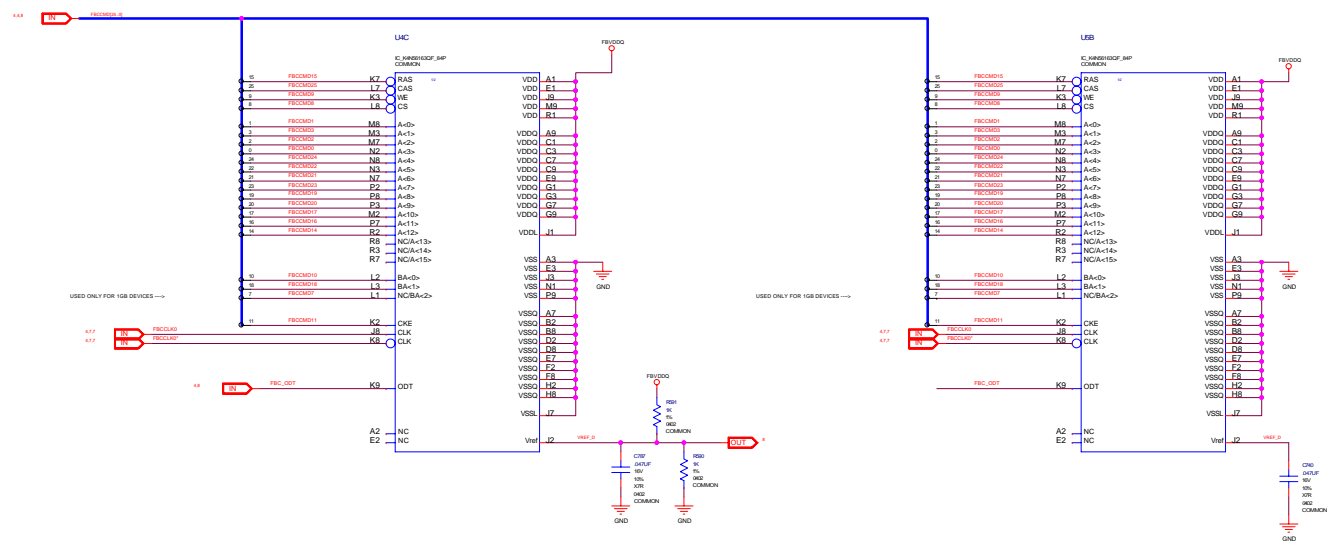
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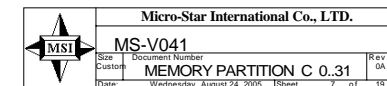
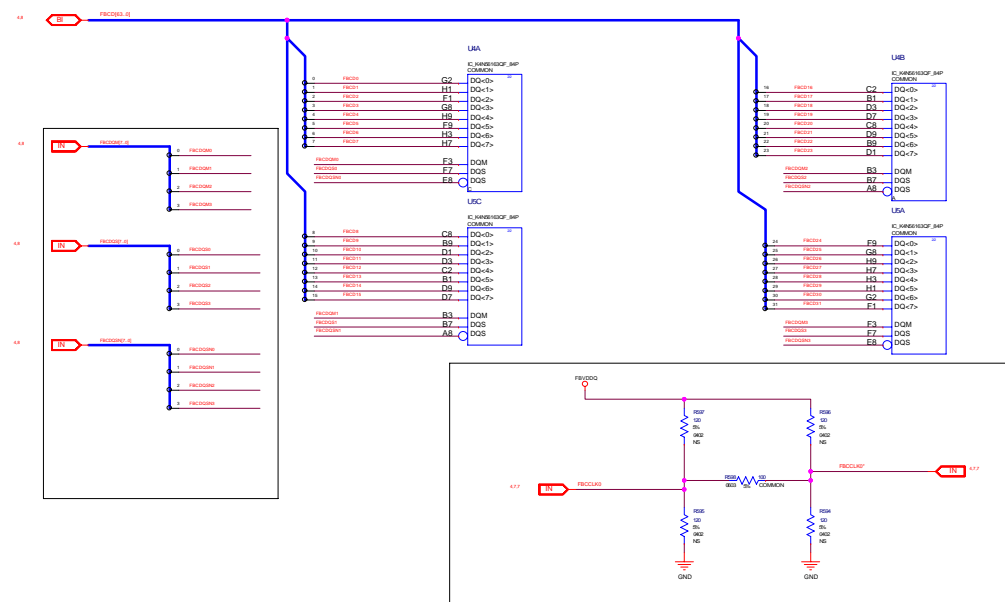
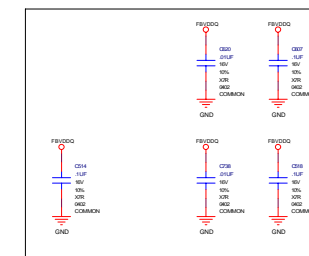
07 MEMORY PARTITION C 0..31

FBC MEMORY 2nd bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



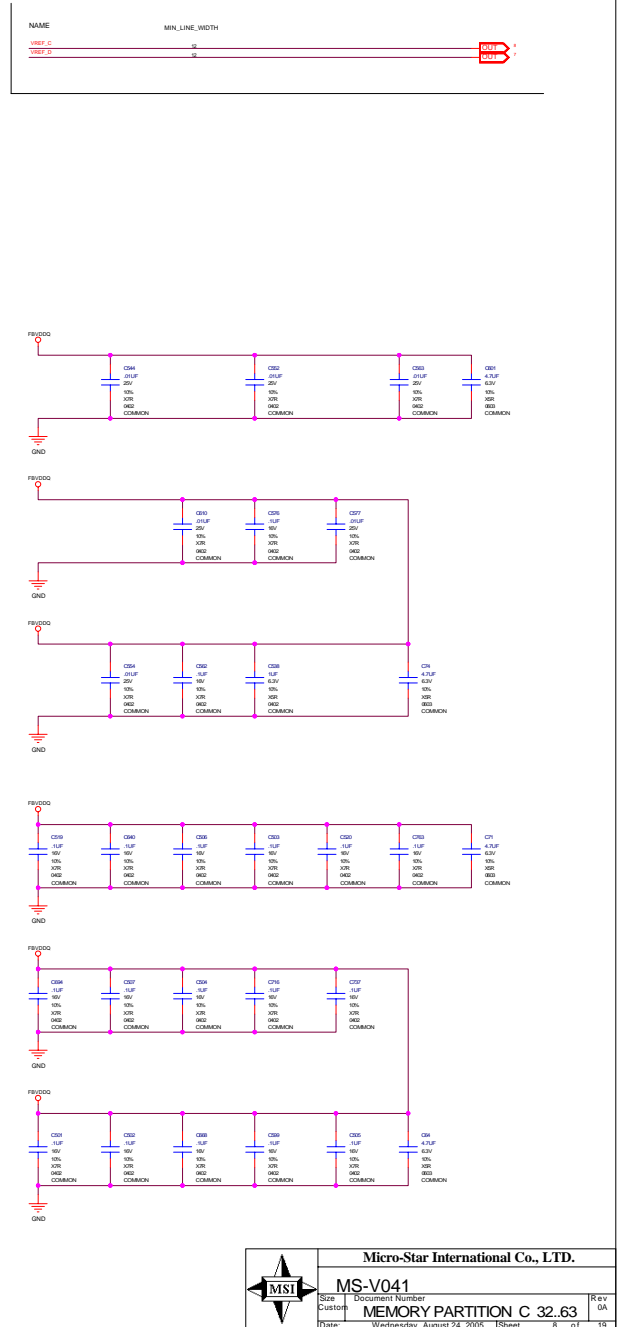
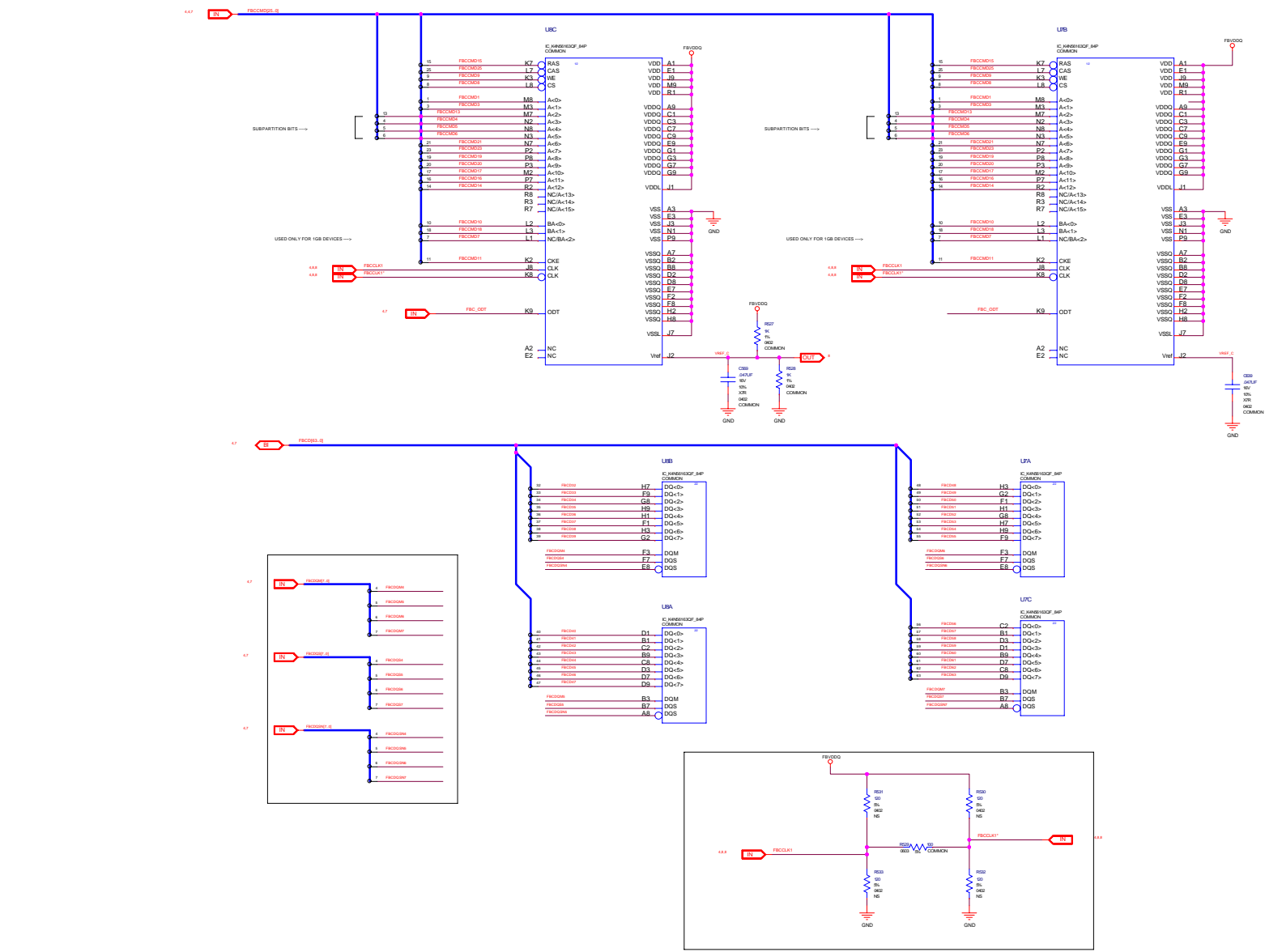
Place plane decoupling caps near DQS-QDM pairs



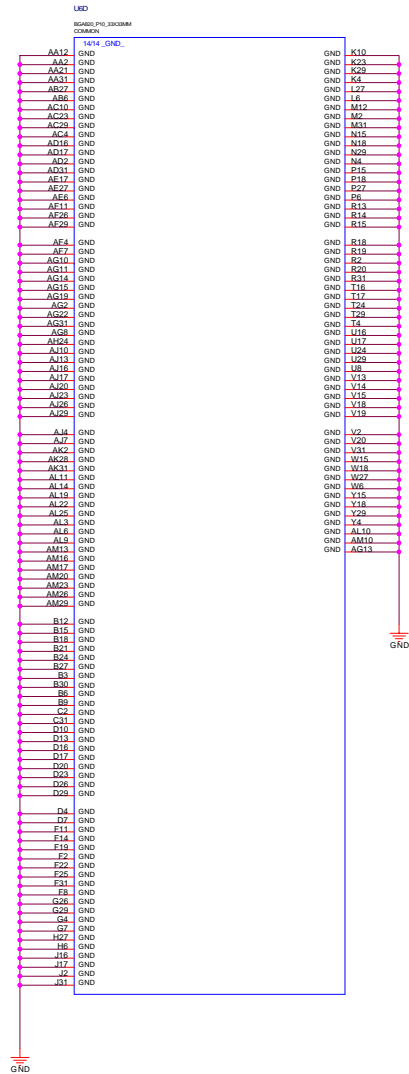
08 MEMORY PARTITION C 32..63

FBC MEMORY 2nd bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



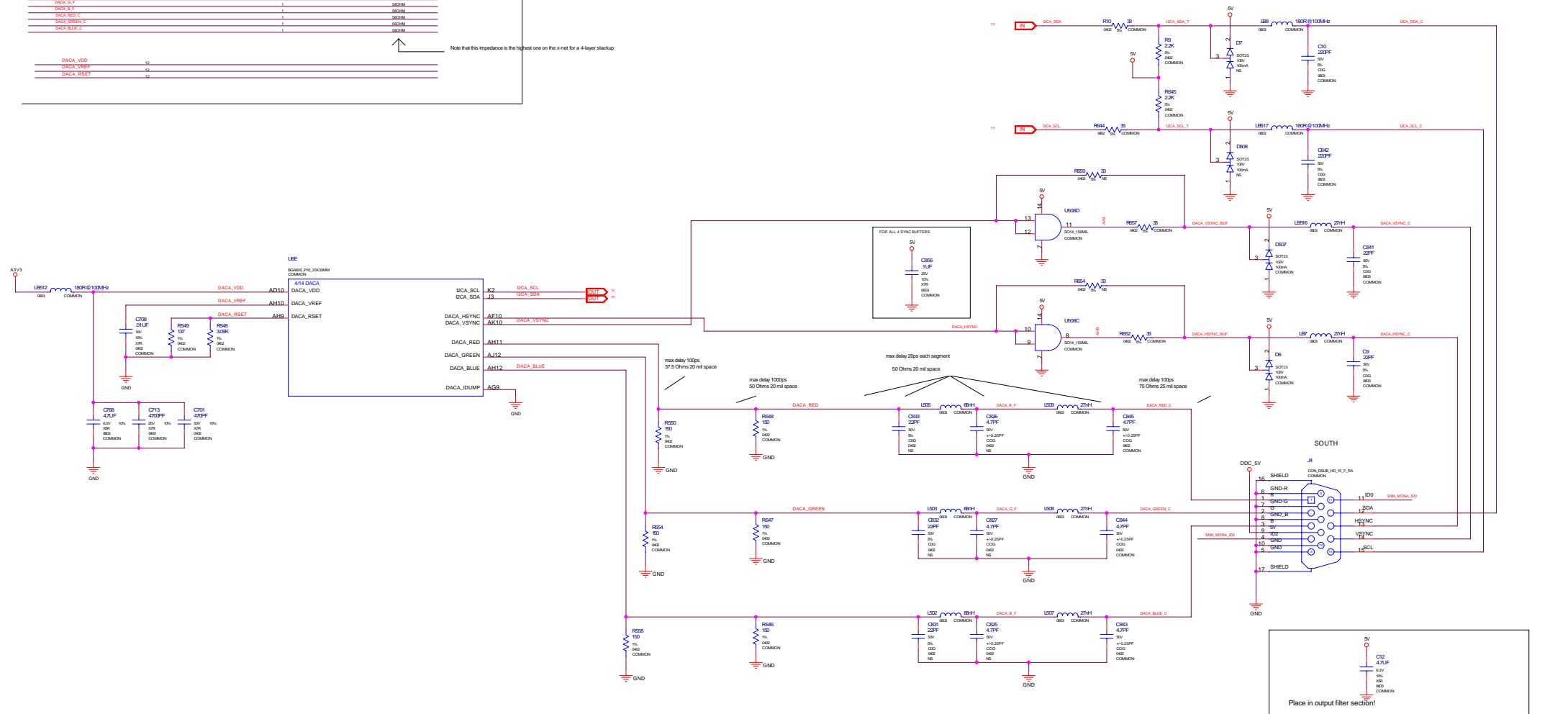
09 GPU GND



10 DACA - VGA

NET_NAME	MIN_LINE_WIDTH	NV_CRITICAL_NET	NV_IMPEDANCE
DACA_SCL			
DACA_SDA			
DACA_HSYNC			
DACA_VSYNC			
DACA_HSYNC_BUF			
DACA_VSYNC_BUF			
DACA_VSYNC_C			
DACA_HSYNC_C			
ATX5			
ATX6			
DACA_RED			
DACA_GREEN			
DACA_BLUE			
DACA_R_F			
DACA_R_C			
DACA_G_F			
DACA_G_C			
DACA_B_F			
DACA_B_C			
DACA_VREF			
DACA_VSET			
DACA_VDD	12		
DACA_VREF	12		
DACA_VSET	12		

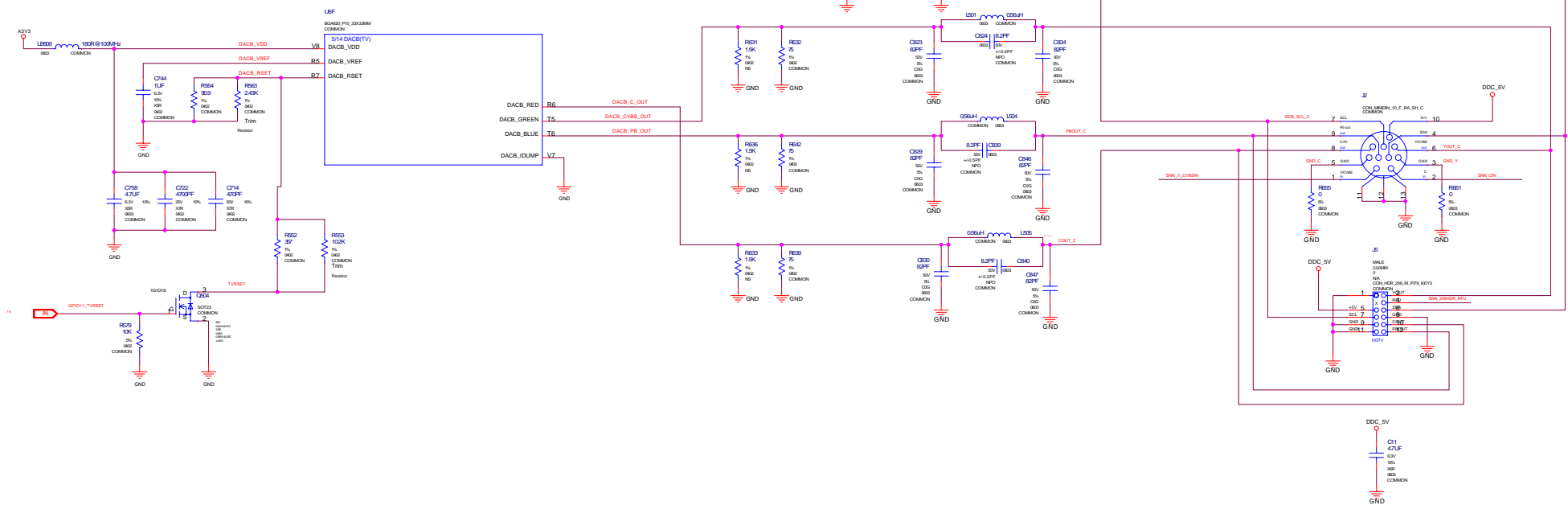
Note that this impedance is the highest one on the x-net for a 4-layer stackup



11 DACB - TVOUT, VIDEO IN

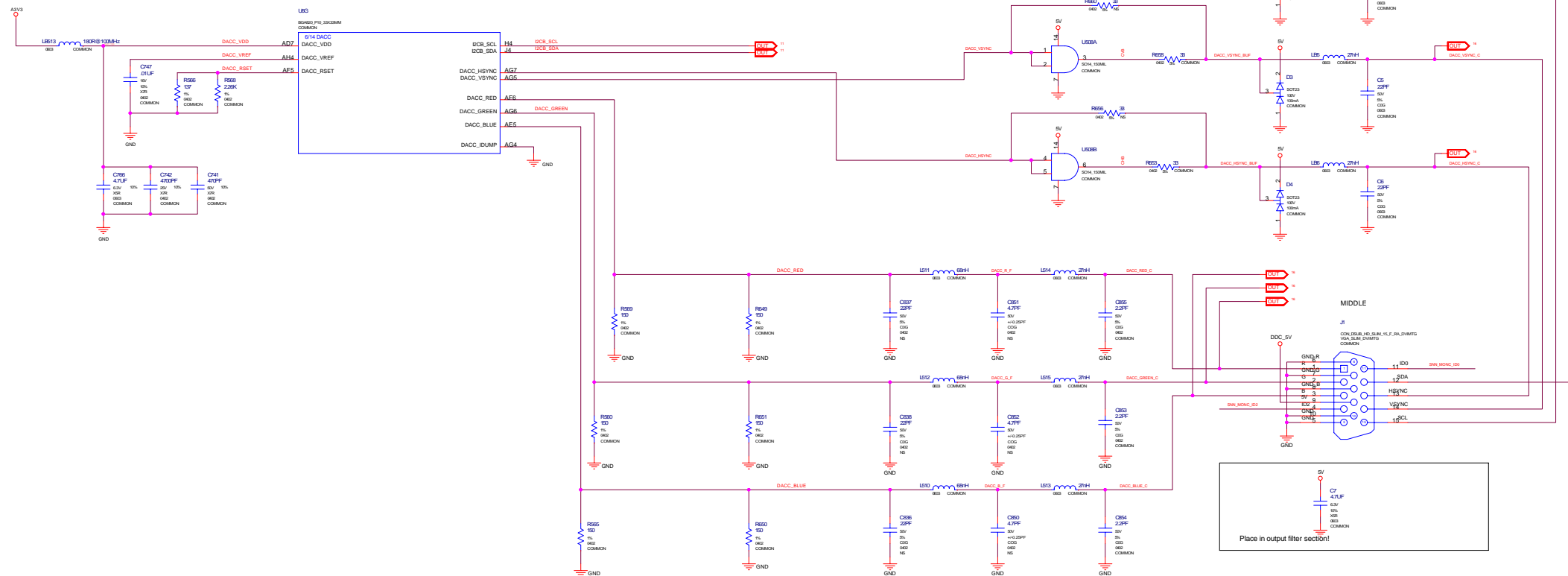
NET_NAME	MIN_LEN_WIDTH	SV_CRITICAL_NET	SV_REFERENCE
DACB_C_OUT		1	SDCBM
DACB_C_VREF_VOUT		1	SDCBM
DACB_PB_VOUT		1	SDCBM
COOUT_C		1	SDCBM
VOUT_C		1	SDCBM
PBOUT_G		1	SDCBM
DACS_VDD	12		
DACS_VREF	12		
DACS_RESET	12		
TVRESET	12		
GND_C	12		
GND_Y	12		

Note that this is the highest impedance on the xnet



2 DACC - VGA

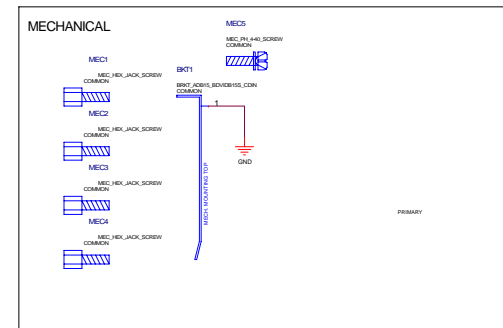
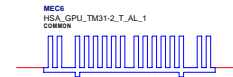
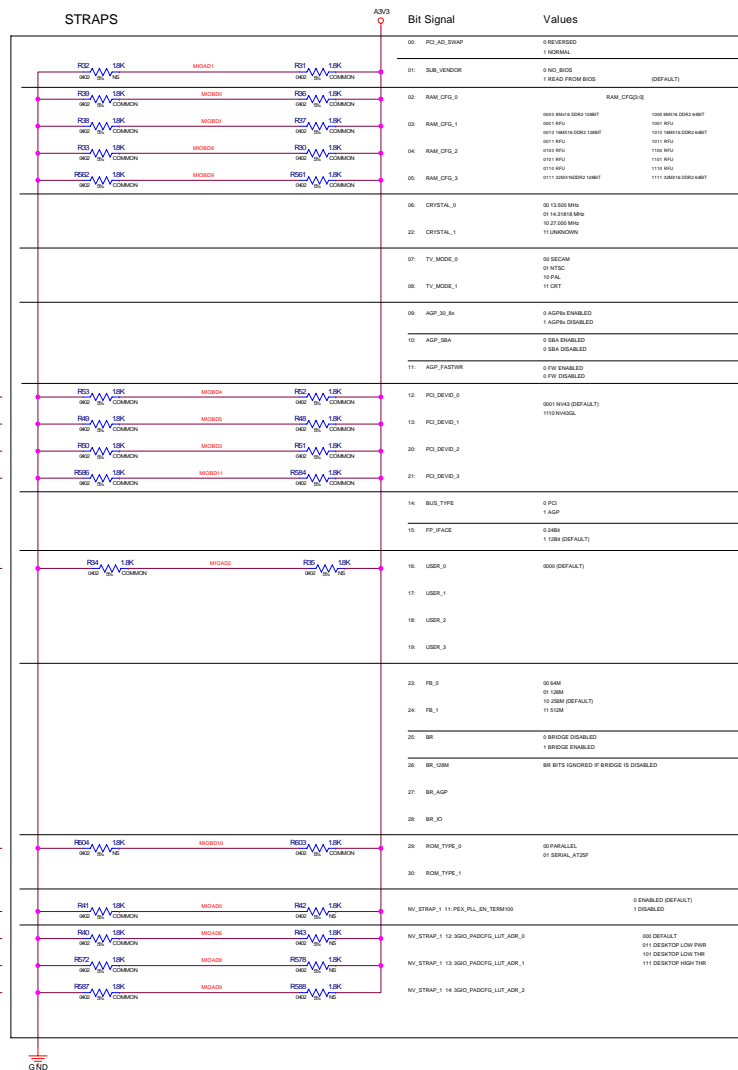
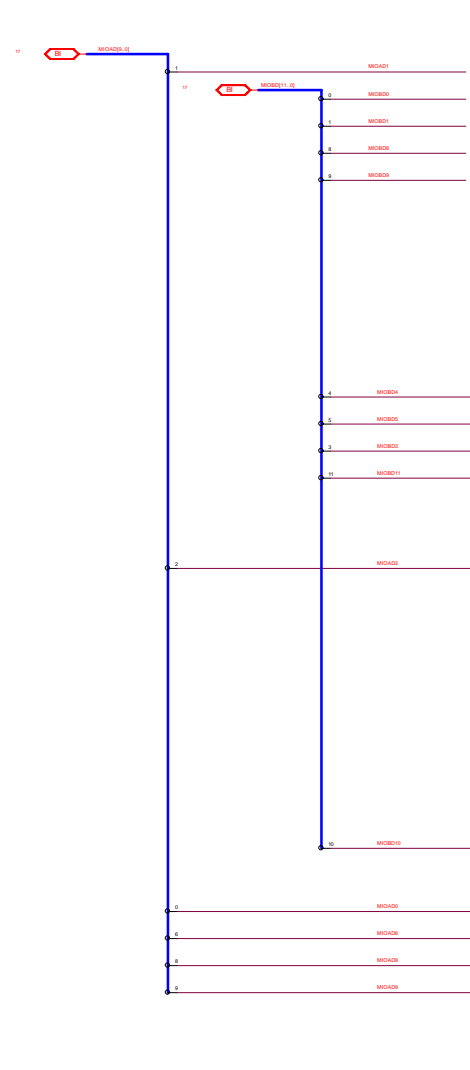
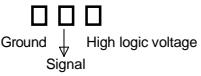
NET_NAME	MIN_WIDTH	NET_SPACING_RULE	NV_CRITICAL_NET	NV_IMPEDANCE
IOB_SCL				
IOB_SDA				
DACC_HSYNC		2	NOQDR	
DACC_VSYNC		2	NOQDR	
DACC_HSYNC_RUP		2	NOQDR	
DACC_VSYNC_RUP		2	NOQDR	
DACC_SERVING_C		2	NOQDR	
DACC_SERVING_E		2	NOQDR	
CHE		2	NOQDR	
LVIS		2	NOQDR	
DACC_RED		1	NOQDR	
DACC_GREEN		1	NOQDR	
DACC_BLUE		1	NOQDR	
DACC_X_F		1	NOQDR	
DACC_X_F		2	NOQDR	
DACC_SERVING_C		1	NOQDR	
DACC_GREEN_C		1	NOQDR	
DACC_BLUE_F		1	NOQDR	
DACC_VDD	18			
DMAC0_RESET	18			
DMAC0_RESET	18			



13 STRAPS, FANSINK, MECHANICALS

Overlap pads to save space
and to prevent assembly of
both resistors.

Layout



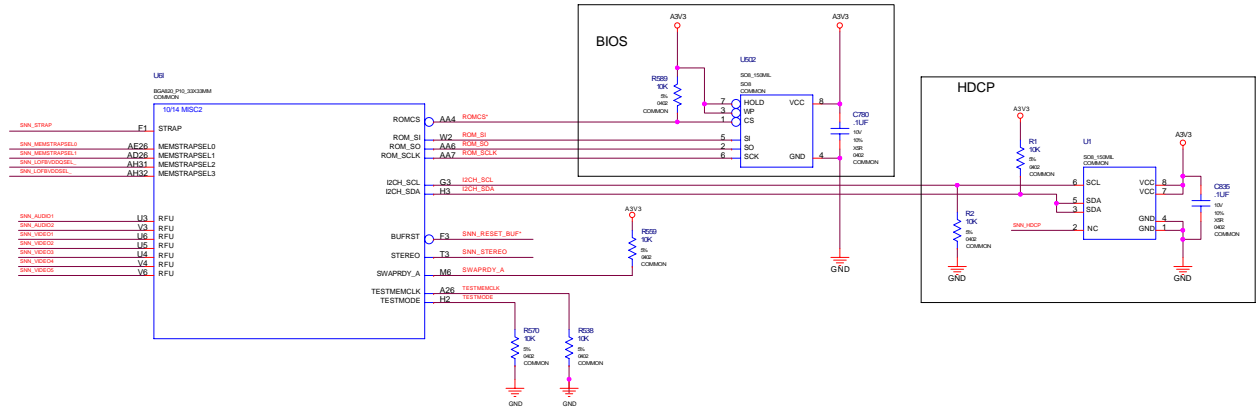
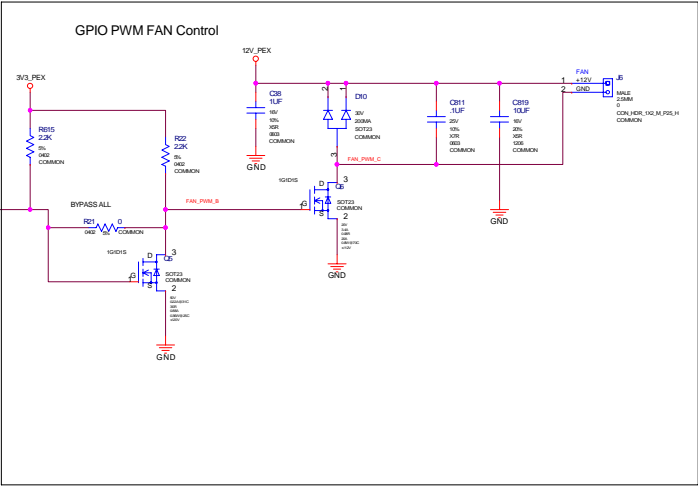
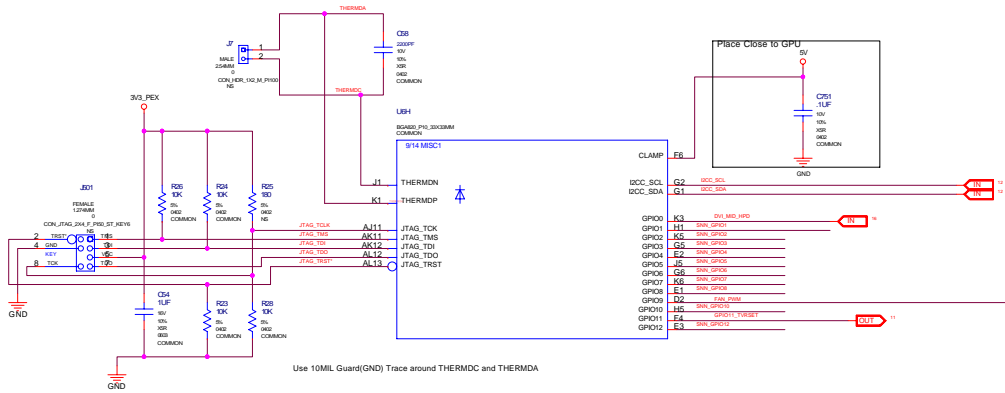
Micro-Star International Co., LTD.

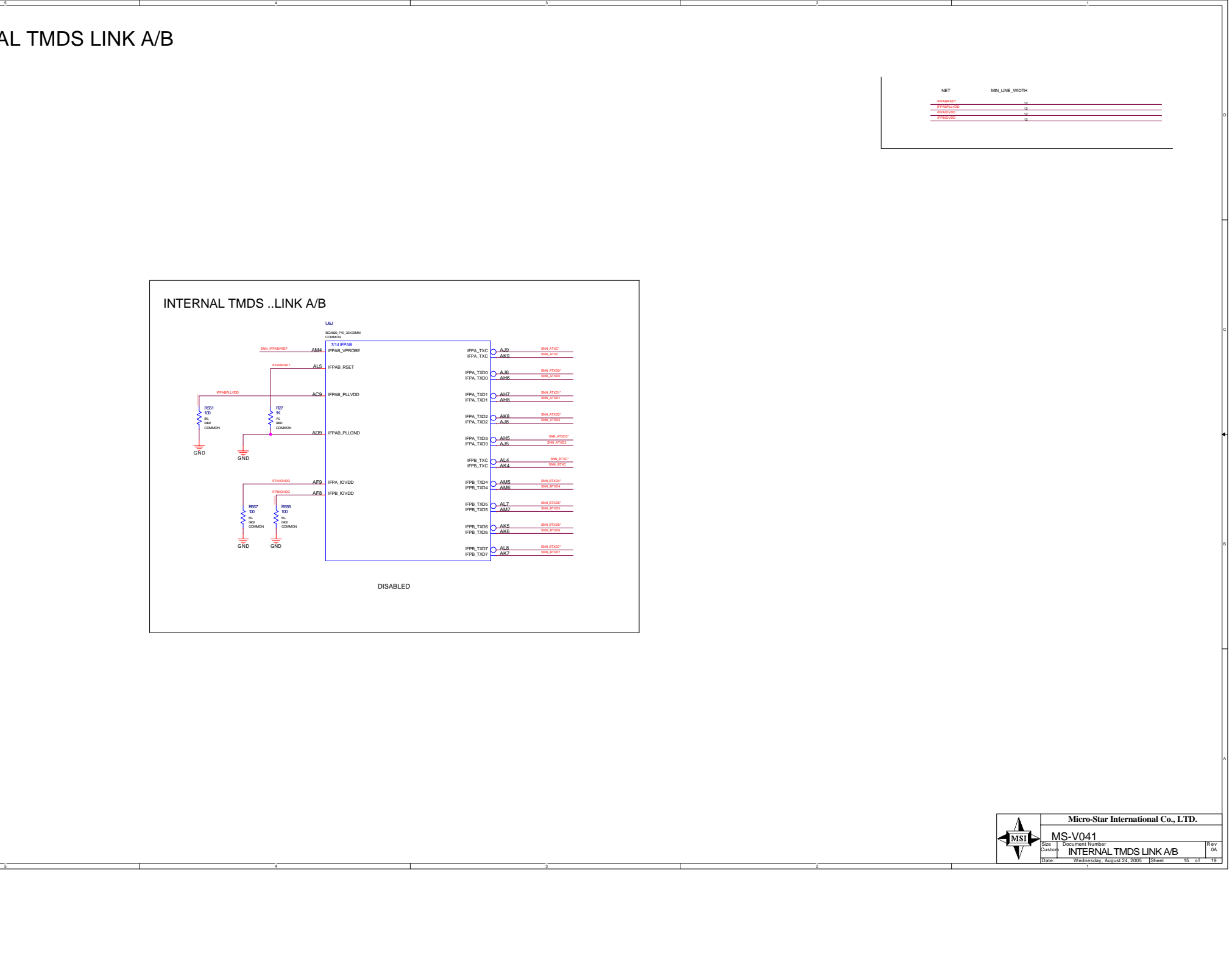
MS-V041			
Size	Document Number		Rev
Custom	STRAPS, FANSINK, MECHANICALS		0A
Date:	Wednesday, August 24, 2005	Sheet	13 of 19

JTAG, GPIO, BIOS ROM

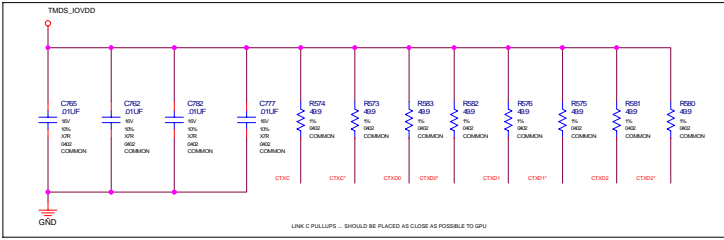
GPIO Assignment Table		
GPIO	IO	FUNCTION
0	IN	DVMID HOTPLUG DET
1	IN	RESERVED
2	IN	RESERVED
3	IN	RESERVED
4	IN	RESERVED
5	IN	RESERVED
6	IN	RESERVED
7	IN	RESERVED
8	IN	THERM ALERT SLOW
9	OUT	FAN CONTROL
10	IN	RESERVED
11	OUT	HDTV/SDTV SELECT
12	IN	RESERVED

NET	MIN_LINE_WIDTH
FAN_THERM_BYPASS	10
FAN_PWM	10
FAN_PWM_B	10
FAN_PWM_C	10
THERMDC	10
THERMDA	10



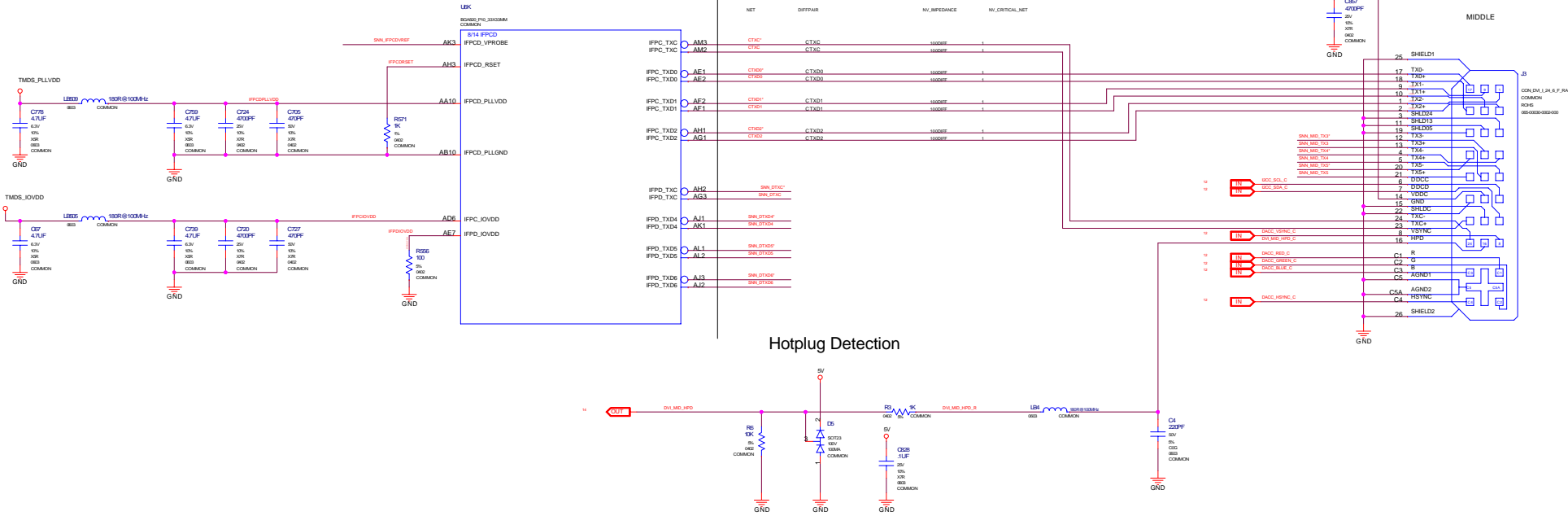
[illegible][illegible]

16 INTERNAL TMDS LINK C/D



NET	MIN_LINE_WIDTH	VOLTAGE
#PC0VREF	12	3.3V
#PC0FLVDD	12	3.3V
#PC0KVDD	12	3.3V
#PC0KVDD	12	3.3V
#PC0RSET	12	3.3V

INTERNAL TMDS ..LINK C

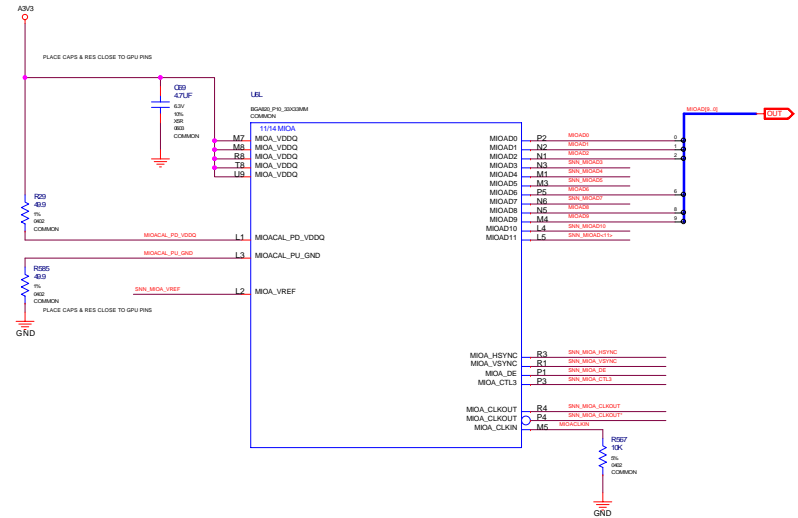


Micro-Star International Co., LTD.

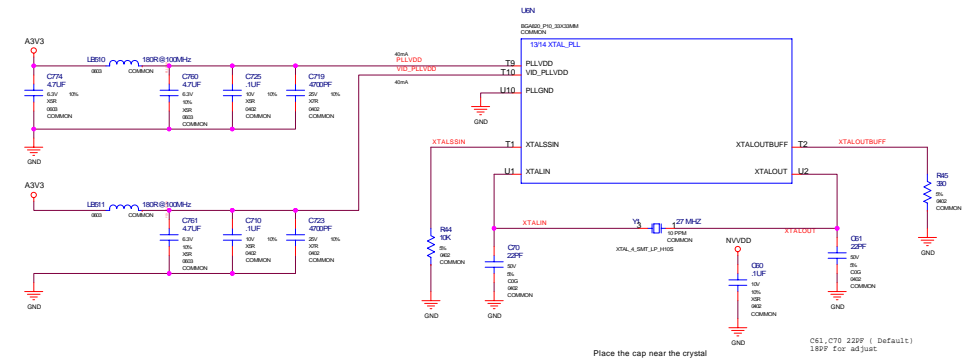
MS-V041	
Size Custom	Document Number INTERNAL TMD5 LINK C/D
Date: Wednesday, August 24, 2005	Sheet 16 of

17 MIOA, MIOB, NVPLL

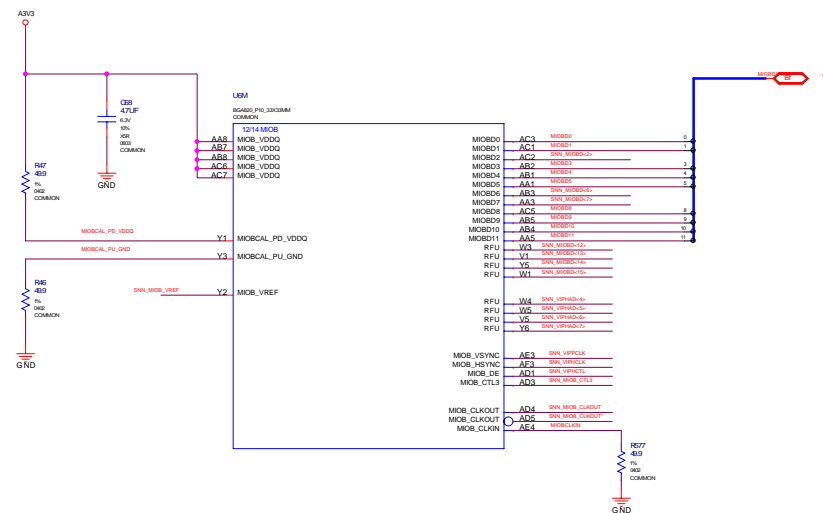
MIOA



XTAL/PLLVD



MIOB



NET	MIN_LINE_WIDTH
VIO_PLLVDD	12
XTALIN	
XTALOUT	
PLLVD	13



Micro-Star International Co., LTD.

MS-V041	
Size Custom	Document Number MIOA, MIOB, NVPLL
Date:	Wednesday, August 24, 2005

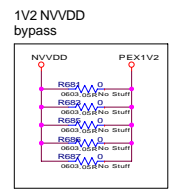
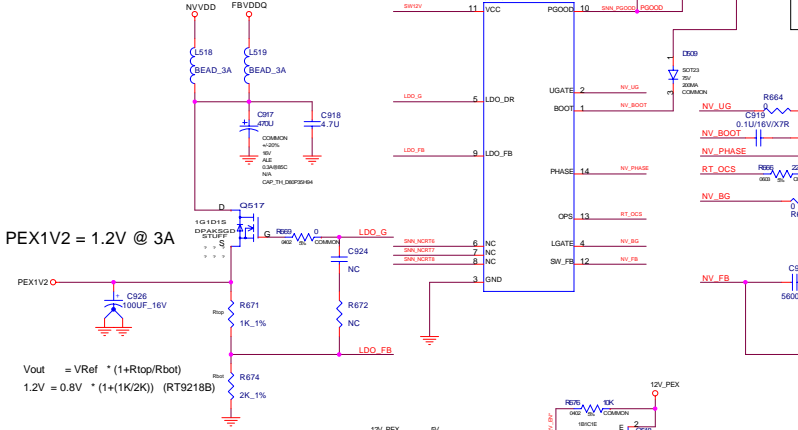
Rev	0A
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18 Power Supply (RT9218)

NVVD, PEX1V2, FBVDDQ

NV-Standard use FBVDDQ ,
Can't use RT9218 PGood power sequence

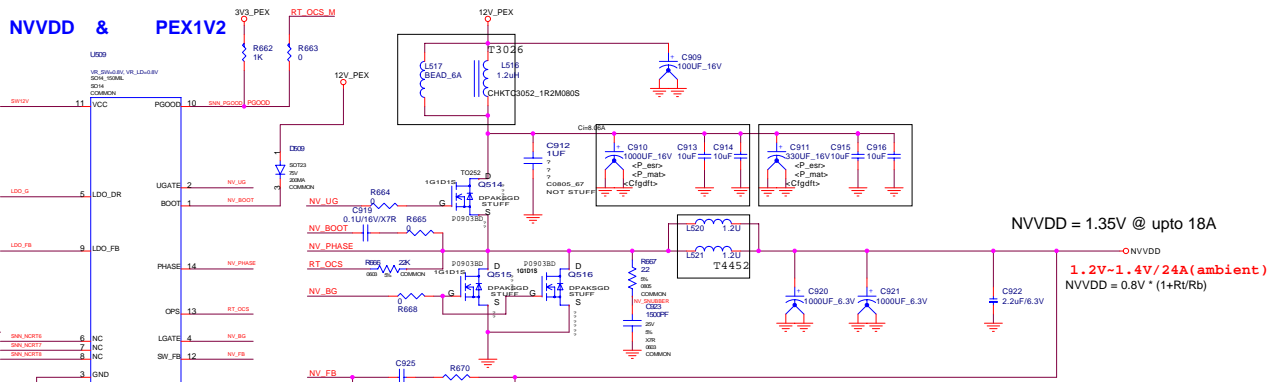
BOM added L821, C905
removed L819



Choose RT9218 PGood power sequence

Added BOM R883, R904

Removed R905



NVVD

$V_{out} = V_{ref} \cdot (1 + R_{top}/R_{bot})$

$1.262V = 0.8V \cdot (1 + (1.37k/2.37k))$ (RT9218)

$1.2V = 0.8V \cdot (1 + (1.54k/3.09k))$ (RT9218)

$1.359V = 0.8V \cdot (1 + (1k/1.43k))$ (RT9218)

$1.344V = 0.8V \cdot (1 + (1k/1.47k))$ (RT9218)

$1.344V = 0.8V \cdot (1 + (100/147))$ (RT9218)

$1.3V = 0.8V \cdot (1 + (100/160))$ (RT9218) default

FBVDDQ

$V_{out} = V_{ref} \cdot (1 + R_{top}/R_{bot})$

$1.8V = 0.8V \cdot (1 + (5k/4k))$ (RT9218)

$1.8V = 0.8V \cdot (1 + (200/160))$ (RT9218) Samsung MEM

$2.003V = 0.8V \cdot (1 + (200/133))$ (RT9218) Infineon MEM default

Net Name	MIN_LINE_WIDTH	VOLTAGE
5V	16	5V
NVVD	16	1.35V
12V_PEX	20	12V
PEX1V2	4	1.2V
12V_PEX_FILTER	20	12V
FBVTT	1.5	FBVTT2_V

DRIVE3_V2	20
UGATE_1	20
UGATE_2	20
UGATE_3	20
UGATE_4	20
UGATE_5	20
UGATE_6	20
UGATE_7	20
UGATE_8	20
UGATE_9	20
UGATE_10	20
UGATE_11	20
UGATE_12	20
UGATE_13	20
UGATE_14	20
UGATE_15	20
UGATE_16	20
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UGATE_96	20
UGATE_97	20
UGATE_98	20
UGATE_99	20
UGATE_100	20

DC/DC calculator Rev 1.1

Output current: 100mA

Output voltage: 1.2V

Input voltage: 12V

Load: 100mA

Switching frequency: 100kHz

Inductor: 1.2mH

Ripple current through the inductor: 1.2V

Maximum inductor current: 1.2V

Input: 12V

Input capacitor ripple current: 1.2V

Output: 1.2V

Output capacitor ripple current: 1.2V

Output capacitor ripple voltage: 1.2V

Output ripple voltage: 1.2V

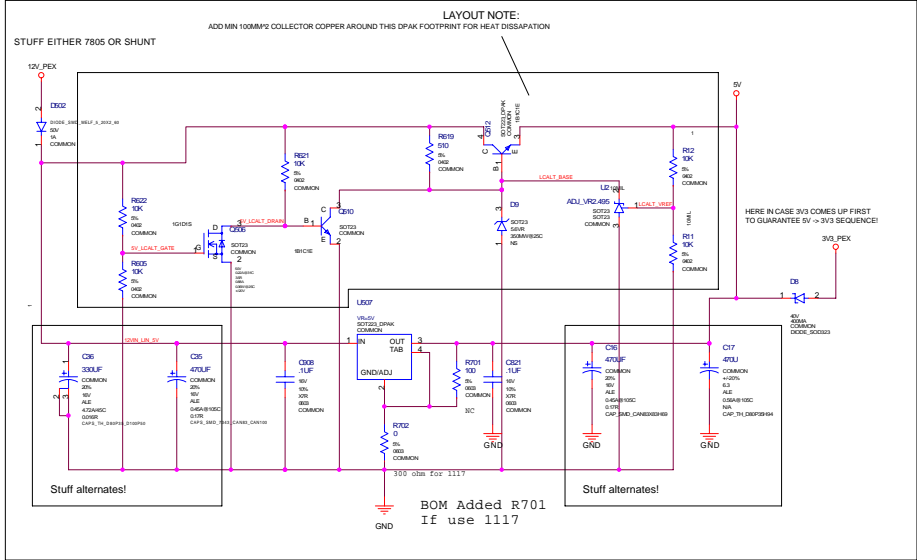
FBVDDQ = 1.8V @ upto 5A

1.8V / 5.0A

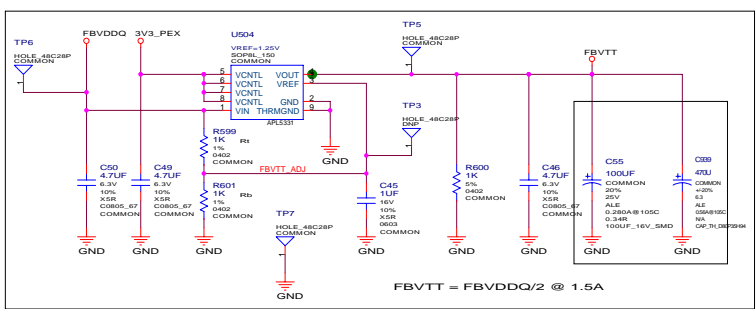
19 Others Power Supply (Linears)

5V,FBVDDQ,A3V3,3V3,TMDS_PLLVDD,TMDS_IOVDD,FBVTT

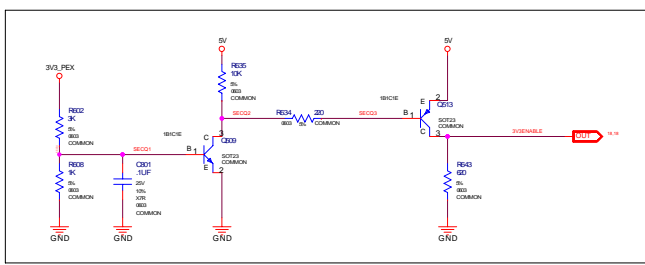
5V LOW COST REGULATOR



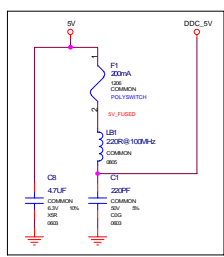
FBVTT TERMINATION



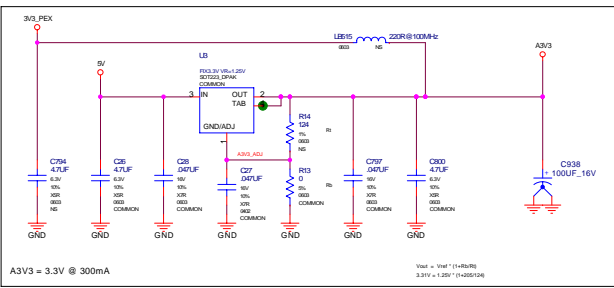
Power Sequencing



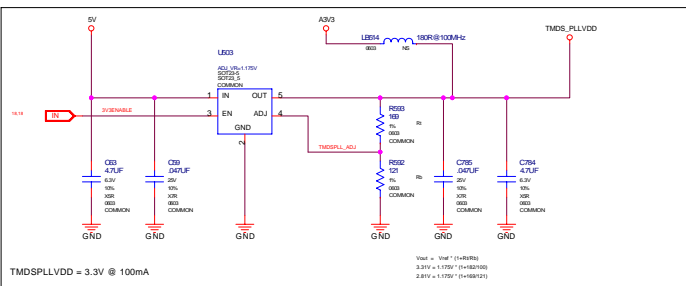
DDC 5V



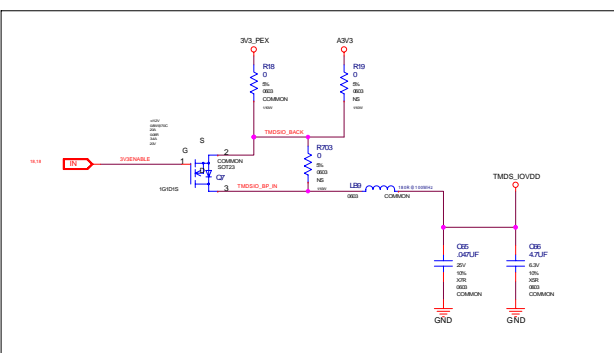
A3V3 Power Supply



TMDS PLL Supply



TMDS IO SUPPLY WITH BACKDRIVE PROTECTION



NET NAME	MIN_LINE_WIDTH	WV_NET_MAX_CURRENT	VOLTAGE
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V
FBVDDQ	FBVDDQ	FBVDDQ	1.8V
A3V3	A3V3	A3V3	3.3V
TMDS_PLLVDD	TMDS_PLLVDD	TMDS_PLLVDD	3.3V
TMDS_IOVDD	TMDS_IOVDD	TMDS_IOVDD	3.3V
3V3_PEX	3V3_PEX	3V3_PEX	3.3V