# "Polaris 20" Databook

Technical Reference Manual - AMD Confidential

Part Number: 55951_1.00

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# Revision History

**Note:** The release states are defined as:

**Preliminary Releases:**

Revision numbers 0.xx are rough works.

Revision numbers 1.xx are documents with substantial info

Revision numbers 2.xx are documents with complete information.

**Full Release**

Revision numbers 3.xx are for production.

## Revision History

### Rev 1.00 (February 17, 2017)

- Preliminary release.

# Contents

# Figures

## Chapter 1 Introduction



## Chapter 2 Functional Overview



## Chapter 3 Signal Descriptions



## Chapter 4 Timing Specifications



## Chapter 5 Electrical Characteristics



## Chapter 7 Mechanical Data



## Chapter 8 Boundary Scan Specification

# Tables

## Chapter 1 Introduction



## Chapter 2 Functional Overview



## Chapter 3 Signal Descriptions

## Chapter 4 Timing Specifications



## Chapter 5 Electrical Characteristics



## Chapter 6 Thermal Data



## Chapter 7 Mechanical Data



## Chapter 8 Boundary Scan Specification



## Appendix A Pin Listings

# 1

# Introduction

TBD.

**The features and functionalities identified in this databook are preliminary information and do not constitute specifications until they have been qualified by AMD.**
**The databook is updated as necessary following qualification to convert this document to a formal specification.**

**Please review any errata and advisories as they identify amendments to the specifications in this databook.**

**Contact your local AMD support person for the software support schedules of GPU features.**

## 1.1 Part Identification

### 1.1.1 Packaging Types and Device IDs

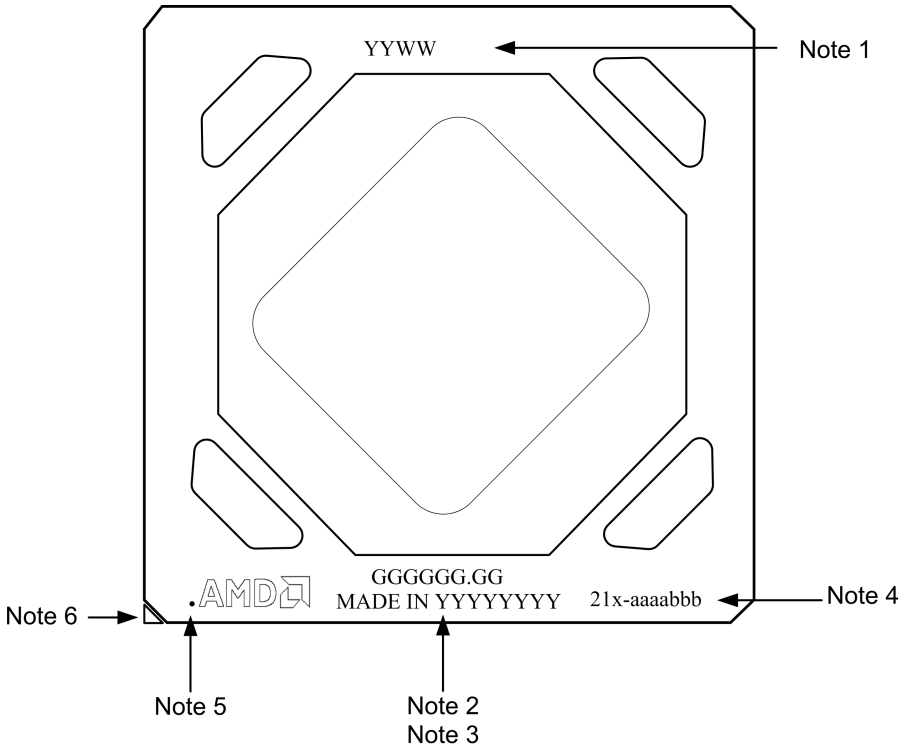
The vendor ID is 0×1002.

Table 1–1 Package Information

| Part | Device ID / Revision ID | Part Number | HD Audio Controller ID | HD Audio Codec ID | Package |
|---|---|---|---|---|---|
| "Polaris 20 XL" | 67DF/EF | 215-0910052 | AAF0 | AA01 | 1401 HFCBGA |
| "Polaris 20 XTX" | 67DF/E7 | 215-0910038 | | | |

### 1.1.2 Branding Format

Figure 1–1 "Polaris 20" Branding




**Note:**

1. The date code where YY is the assembly start year and WW is the assembly start week. Special markings that help differentiate the GPU from others may also appear on this line. For example, ES is found after the date code for engineering samples.
2. Country of origin YYYYYYYY (The assembly site; such as USA, SINGAPORE, TAIWAN, and CHINA).
3. The wafer foundry's lot number.
4. The part number. Refer to Table 1–1 (p. 1) for the appropriate part number.
5. Pin 1 dot.
6. GPU pin A1.

The branding format can be in laser, ink, or mixed laser and ink marking.

# 2

# Functional Overview

This section describes the major subsystems and interfaces of "Polaris 20". To go to a topic of interest, use the following list of linked cross-references:



## 2.1 Memory Interface

### 2.1.1 Memory Configurations Support

"Polaris 20" has eight (256-bit) DRAM sequencers. Each DRAM channel is 32-bit wide. All DRAM devices must be of the same type, have the same size on each channel and must run at the same voltage.

"Polaris 20" supports only GDDR5 DRAM.

**Supported DRAM Component Organizations:**

- 8 or 16 banks (3 or 4 bank bits). Single rank.
- Rows: 1024, 2048, 4096, 8192, 16384, 32768, or 65536 (10, 11, 12, 13, 14, 15, or 16 bits).
- Columns: 256, 512, 1024, 2048 (8, 9, 10 bits).
- CS (chip select): 1.

### 2.1.2 Memory Aperture Size

The memory-aperture size can be set up through either pin straps for designs that do not have dedicated ROM for the video BIOS, or ROM straps for designs that have dedicated ROM. Refer to the descriptions of the ROM_CONFIG[2:0] and MEM_AP_SIZE [2:0] straps in Configuration Straps (p. 35) for more information.

The memory aperture defines the address range that the CPU can access. The memory-aperture size assigned to the GPU by the system BIOS is different from the physical-memory size that the AMD display driver reports to the operating system and control panel. It does not limit the GPU's ability to use the entire frame-buffer memory at any time. Modern graphics and multimedia applications use drivers to alter the frame-buffer contents—direct manipulation of the frame buffer by the CPU is limited. Therefore, having a memory-aperture size that is smaller than the physical frame-buffer size does not limit performance. The AMD display driver reports the memory size based on the amount of physical VRAM installed on the card rather than the memory-aperture size.

Due to memory-management constraints, the memory-aperture size should be the same as the frame-buffer size for 64 MB, 128 MB, and 256 MB. For frame-buffer sizes larger than 256 MB, the memory-aperture size should be 256 MB. For designs requiring larger than 256 MB aperture size, consult with AMD.

### 2.1.3 Examples of Possible Memory Configurations

The following are examples of possible single-rank memory configurations using different memory types.

**Note:** Not all memories are qualified. Check with your local AMD support person for the latest qualified memory list.

#### 2.1.3.1 GDDR5 SGRAM (Graphics Double Data Rate Synchronous Graphics RAM)

Table 2–1 GDDR5 SGRAM

| Size per Part | Configuration | Row × Col × Bank Bits | Total Memory Size (256-bit Interface) |
|---|---|---|---|
| **512 Mbit** | 2 M × 32 × 8 | 12 × 6 × 3 | 512 MB |
| **1024 Mbit** | 2 M × 32 × 16 | 12 × 6 × 4 | 1024 MB |
| **2048 Mbit** | 4 M × 32 × 16 | 13 × 6 × 4 | 2048 MB |
| **4096 Mbit** | 8 M × 32 × 16 | 14 × 6 × 4 | 4096 MB |
| **8192 Mbit** | 16 M × 32 × 16 | 14 × 7 × 4 | 8192 MB |

## 2.2 Acceleration Features

- Support for DirectX® 12 (Feature Level 12_0) features, including the full-speed 32-bit floating point per component operation:
  - Shader Model 5.0 geometry and pixel support in a unified shader architecture:
    - Vertex, pixel, geometry, compute, domain, and hull shaders.
    - 32- and 64-bit floating-point processing per component.
    - New advanced shader instructions, including flexible flow control with CPU-level flexibility on branching.
    - A nearly unlimited shader-instruction store, using an advanced caching system.
    - An advanced shader design, with an ultra-threading sequencer for high-efficiency operations.
    - Graphics Core Next supporting native scalar instructions.
    - Advanced, high-performance branching support, including static and dynamic branching.
    - High dynamic-range rendering with floating-point blending, texture filtering, and anti-aliasing support.
    - 16- and 32-bit floating-point components for high dynamic-range computations.
    - Full anti-aliasing on renderable surfaces up to and including 128-bit floating-point formats.
    - A new read/write caching system, replacing texture cache with a unified read-write two-level cache.
- Support for OpenGL 4.5.
- Support for OpenCL™ 2.0.
- Support for Mantle
- Support for AMD LiquidVR™
- Anti-aliasing filtering:
  - 2×/4×/8× MSAA (multi-sample anti-aliasing) modes are supported.
  - A multi-sample algorithm with gamma correction, programmable sample patterns, and centroid sampling.
  - Custom filter anti-aliasing with up to 12-samples per pixel.
  - An adaptive anti-aliasing mode.
  - Lossless color compression (up to 16:1).

- Anisotropic filtering:
  - Continuous anisotropic with 1× through 16× taps.
  - Up to 128-tap texture filtering.
  - Anisotropic biasing to allow trading quality for performance.
  - Improved anisotropic filtering with unified non-power of two-tap distribution and higher precision filter computations.
  - Advanced texture compression (3Dc+™).
  - High quality 4:1 compression for normal and luminance maps.
  - Angle-invariant algorithm for improved quality.
  - Single- or two-channel data format compatibility.
- 3D resources virtualized to a 40-bit virtual addressing space, for support of large numbers of render targets and textures.
- Up to 16k × 16k textures, including 128-bit/pixel texture are supported.
- Programmable arbitration logic maximizes memory efficiency and is software upgradeable.
- Fully associative texture, color, and z-cache design.
- Hierarchical z- and stencil-buffers with early z-test.
- Lossless z-buffer compression for both z and stencil.
- Fast z-buffer clear.
- Fast color-buffer clear.
- Z-cache optimized for real-time shadow rendering.
- Z- and color-compression resources virtualized to a 32-bit addressing space, for support of multiple render targets and textures simultaneously.

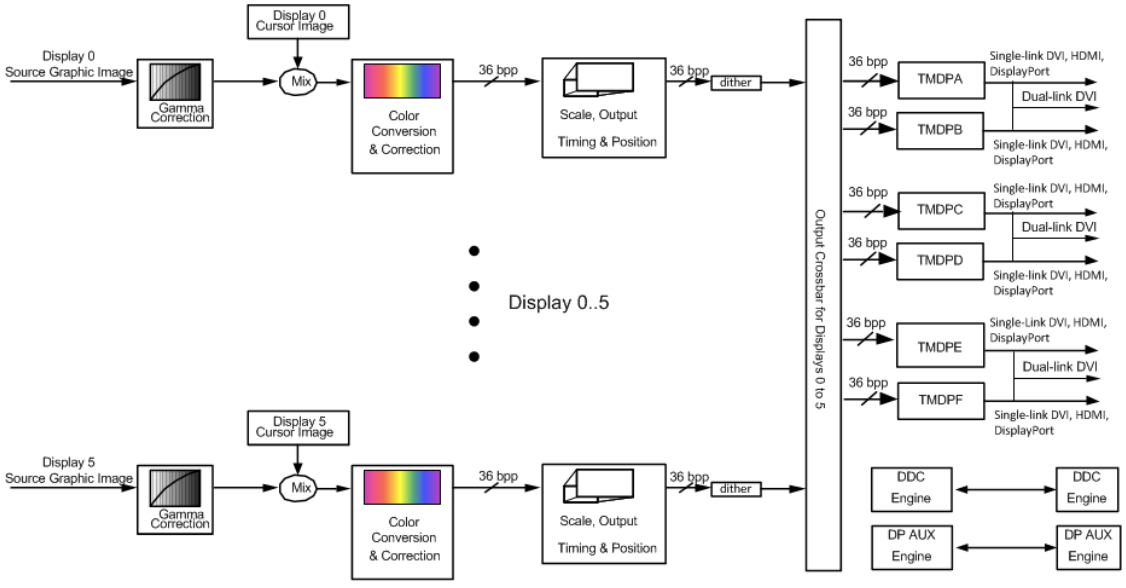
## 2.3 Display System

The display system supports accelerated display modes on up to six independent display controllers.

The full features of the display system are outlined in the following sections.

### 2.3.1 Display Features

Figure 2–1 "Polaris 20" Display Top-level Data-flow Diagram




- Up to six independent display controllers that support up to true 36-bpp (bits per pixel) throughout the display pipe.
- Support for each display output type up to the following display timings:
  - DisplayPort 1.4 (HBR3):
    - Up to three 5120 × 2880 pixel resolution displays @ 60 Hz refresh rates with dual-cable configuration, or
    - One 5120 × 2880 pixel resolution display @ 60 Hz refresh rates with single-cable configuration, or
    - Up to six 3840 × 2160 @ 60 Hz or six 4096 × 2160 @ 60 Hz displays.
  - HDMI™ 2.0b (6 Gbit/s) up to six 3840 × 2160 @ 60 Hz or six 4096 × 2160 @ 60 Hz outputs
  - Dual-link DVI up to three 2560 × 1600 @ 60 Hz or 1920 × 1200 @ 60 Hz
  - Single-link DVI up to six 1920 × 1200 @ 60 Hz
- Support for up to six independent display timings on DisplayPort, HDMI, or DVI interfaces
- Advanced video capabilities, including high-fidelity gamma, color correction, and scaling for High Dynamic Range (HDR) or Standard Dynamic Range (SDR)
- A high-precision color pipe with the support of sRGB, Rec. 709 and Rec. 2020 color spaces with up to 12 bits/component
- HDR 10 with HDMI 2.0b and DP 1.4 HDR protocol support

- Each display pipe includes a high quality scaler for upscaling lower resolution desktop modes to available display resolutions (RMX) or underscanning for the HDMI output (if needed)
  - All desktop sources up to 4096 pixels/line may be upscaled (RMX)
  - Desktops up to 1920 wide may be underscanned for HDMI
- Support for Virtual Super Resolution (VSR) modes with surface size up to 5120 × 2880 downscaled to 3840 × 2160 @ 60 Hz
- HDCP supported independently and simultaneously on all HDMI, DVI, and DisplayPort outputs

  **Note:** HDCP is available only to licensed HDCP licensees and can only be enabled when connected to an HDCP-capable receiver
  - Supports HDCP version 1.4/2.2 protection for the HDMI interface
  - Supports HDCP version 1.1/2.2 protection for the DisplayPort interface
  - Supports HDCP version 1.4 protection for the DVI interface
- Support for Stereo 3D displays through HDMI, DisplayPort, and DVI. Includes frame-sequential and frame-packed full Stereo 3D modes. Also 2D frame-compatible modes including side-by-side, top-and-bottom, line interleaved, and pixel interleaved
- Line or pixel interleave Stereo 3D mixing supported without the use of graphics shaders by using two display pipes for left and right and blending together immediately before the display output; this improves the Stereo 3D performance.

### 2.3.2 DVI/HDMI™/DisplayPort Features

- All TMDP links can be independently configured to any of single-link DVI, HDMI, or DisplayPort (DP)
- TMDPA and TMDPB (links A and B) may be combined to support dual-link DVI
- TMDPC and TMDPD (links C and D) may be combined to support dual-link DVI
- TMDPE and TMDPF (links E and F) may be combined to support dual-link DVI
- See Table 3–6 (p. 23) for more information on the supported display interface combinations
- Optional dithering or frame modulation from the 36-bpp internal display pipeline to 24-bit or 30-bit outputs on the DVI, HDMI, and DisplayPort if not using a 36-bpp output mode

#### 2.3.2.1 DVI/HDMI™ Features

- Supports industry-standard CEA-861 video modes including 480p, 720p, 1080i, 1080p, and 2160p. For a full list of currently supported modes, contact your local AMD support representative
- Supports AMD FreeSync™ technology on HDMI using AMD's vendor specific extension:
  - Fully HDMI compliant
  - Requires at least one display that is capable of AMD HDMI FreeSync™ technology
- Maximum pixel rates for 24-bpp outputs are:
  - DVI—165 MP/s (megapixels per second) for single-link DVI
  - DVI—330 MP/s for dual-link DVI
  - HDMI—594 MP/s

Table 2–2 HDMI™ Features

| HDMI Feature | Support |
|---|---|
| **Link Capabilities** | |
| **Maximum Signal Bandwidth (MHz)** | 594* |
| **Maximum HDMI Data Bandwidth (Gbit/s)** | 3 × 5.94 = 17.82 |
| **Video Capabilities** | |
| **Maximum 2D Resolution** | 1920 × 1080p @ 144 Hz, 36 bpp<br>2560 × 1440 @ 100 Hz, 30 bpp<br>2560 × 1440 @ 144 Hz, 24 bpp<br>3840 × 2160 @ 60 Hz, 24 bpp<br>4096 × 2160 @ 60 Hz, 24 bpp<br>3840 × 2160 @ 30 Hz, 36 bpp<br>4096 × 2160 @ 30 Hz, 36 bpp |
| **RGB** | Yes |
| **YCbCr 4:4:4 / YCbCr 4:2:2 / YCbCr 4:2:0** | Yes |
| **xvYCC** | Yes |
| **HDMI Deep Color** | Yes |
| **Maximum 4:4:4/4:2:2/4:2:0 Color Depth (bits per component)** | 12 |
| **PCM (Pulse-code Modulation) Audio Capabilities** | |
| **PCM Audio Rates Supported (kHz)** | 192, 96, 48, 176.4, 88.2, 44.1, 32 |
| **PCM Audio Bits per Sample** | 24, 20, 16 |
| **Maximum PCM Audio Channels** | 8 |
| **Maximum PCM Audio Bandwidth (rate × bits × channels) (Mbps)** | 36.864 |
| **Specific non-PCM Audio-format Support** | |
| **IEC 61937 Compressed-format support. For example, 5.1-channel Dolby DTS and 5.1-channel AC-3.** | Yes |
| **Dolby®-TrueHD Bitstream Capable** | Yes |

| HDMI Feature | Support |
|---|---|
| **DTS-HD Master-audio Bitstream Capable** | Yes |
| **DVD-A (DST) Support** | No |
| **SACD (DSD) Support** | No |
| **Stereo 3D Display Capabilities** | |
| **Packed Frame Stereo 3D Video Formats** | 2160p @ 30/25/24 Hz,<br>1080p @ 120/100/60/50/30/25/24 Hz,<br>720p @ 120/100/60/50/30/25/24 Hz |
| **Note:**<br>*** Applies to direct connections where GPU and HDMI connectors are on the same PCB with maximum trace lengths of 127 mm or 5 inches, otherwise re-driver is needed.** | |

#### 2.3.2.2 DisplayPort (DP) Features

- Supports all the mandatory features of the *DisplayPort Standard Version 1.4* and the following optional features on all links:
  - HBR3 (8.1 Gbps) support
  - HDR protocol support
  - ACM packet-type support
  - ISRC packet-type support
- DisplayPort Multi-streaming Transport (MST) allowing up to four display pipelines to drive a single DisplayPort interface (provided the DisplayPort link bandwidth is not exceeded)
- Supports AMD FreeSync™ technology, which dynamically synchronizes the refresh rate of a display with the frame rate of the GPU:
  - Based on DisplayPort™ Adaptive-Sync technology
  - Requires at least one display that is capable of DisplayPort Adaptive-Sync technology
- Each DisplayPort link can support three options for the number of lanes and four options for link-data rate as follows:
  - Four, two, or one lane(s)
  - 8.1-, 5.4-, 2.7-, or 1.62-Gbps link-data rate per lane

- Supports YCbCr formats in 4:4:4, 4:2:2, and 4:2:0 and 8, 10, and 12 bits/component using Rec. 709 and Rec. 2020
- Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth
  - Example of supported pixel rate/resolution support for four lanes at 8.1-Gbps link rate:
    - 5120 × 2880 @ 60 Hz, 24 bpp is supported using VESA timings @ 938.25 MP/sec
    - 3840 × 2160 @ 120 Hz, 24 bpp is supported using VESA timings @ 1075.804 MP/sec
  - Examples of supported pixel-rate/resolution for four lanes at 5.4-Gbps link rate:
    - 3840 × 2160 @ 60 Hz, 24 bpp or 30 bpp is supported using VESA timings @ 533.25 MP/sec
    - 3840 × 2160 @ 60 Hz, 24 bpp or 30 bpp is supported using CEA timings @ 594 MP/sec
    - 4096 × 2160 @ 60 Hz, 24 bpp or 30 bpp is supported using CEA timings @ 594 MP/sec
    - 2560 × 1440 @ 144 Hz, 24 bpp is supported using CEA timings @ 586.586 MP/sec
  - Examples of supported pixel-rate/resolution for two lanes at 5.4-Gbps link rate:
    - 2560 × 1600 @ 60 Hz, 24 bpp or 30 bpp is supported using VESA timings @ 268.5 MP/sec
  - The following table shows the maximum pixel rates for four, two, or one lane(s) at 8.1-GHz link rate.

Table 2–3 Maximum Pixel Rates for 4, 2, or 1 Lane(s) at 8.1-GHz Link Rate

| | **18 bpp** | **24 bpp** | **30 bpp** | **36 bpp** |
|---|---|---|---|---|
| **One Lane** | 360 MP/s | 270 MP/s | 216 MP/s | 180 MP/s |
| **Two Lanes** | 720 MP/s | 540 MP/s | 432 MP/s | 360 MP/s |
| **Four Lanes** | 1080 MP/s | 1080 MP/s | 864 MP/s | 720 MP/s |

### 2.3.3 Integrated HD-Audio Controller (Azalia) and Codec

- Each HDMI, DisplayPort, and wireless display output supports HD audio stream independently, up to a maximum of six output streams
- Maximum output bandwidth of 73.728 Mbit/s
- Low power ECN support
- Hardware silent stream for power optimization during no audio periods
- Function level reset
- Compatible Microsoft® UAA driver support for basic audio

- For advanced functionality (as follows), an AMD or a third party driver is required
- LPCM:
  - Speaker formats: 2.0, 2.1, 3.0, 4.0, 5.1, 6.1, and 7.1
  - Sample rates: 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz
  - Bits per sample: 16, 20, and 24
- Non-HBR compressed audio pass-through up to 6.144 Mbps:
  - Supports AC-3, MPEG1, MP3 (MPEG1 layer 3), MPEG2, AAC, DTS, ATRAC, Dolby Digital+, WMA Pro, and DTS-HD
- HBR compressed audio pass-through up to 24.576 Mbps:
  - Supports DTS-HD Master Audio and Dolby True HD
- Plug-and-Play:
  - Sink audio format capabilities declaration
  - Sink information
  - AV association
- Lip sync information
- HDCP content protection
- DisplayPort supports Global TimeCode using the regular AUX channel—GTC master mode only

## 2.4 Video Acceleration Features

- Video Decode Acceleration Technology:
  - Dedicated Unified Video Decoder hardware (UVD) for H.264, HEVC, VC-1, MPEG-4, MPEG-2, and MVC decode:
    - The H.264 implementation is based on the ISO/IEC 14496-10 specification. Up to HP@L5.1 decoding with a maximum bit rate of 160 Mbps. Support for constrained Baseline profile only (no FMO or ASO). Resolution support up to 4096 × 2160 (maximum 4K @ 60 fps).

      Multi View Coding (MVC) support for Blu-ray 3D content.
    - The HEVC implementation is based on the ISO/IEC 23008-2 specification. Up to Main/Main10 L5.1 decoding with a maximum bit rate of 160 Mbps. Resolution support up to 4096 × 2176 (maximum 4K @ 60 fps). Supports HDR-10 video playback.
    - The VC-1 implementation is based on the SMPTE 421M specification. Up to AP@L3 decoding with a maximum bit rate of 40 Mbit/sec. Resolution support up to 1920 × 1088 (maximum 1080p @ 60 fps).
    - MPEG-4 up to ASP@L5 decoding, supporting high-definition profiles. Sprite, GMC (global motion compensation), and RVLC (reversible variable length coding) are not supported. Resolution support up to 1920 × 1088 (maximum 1080p @ 60 fps).
    - The MPEG-2 implementation is based on the ISO 13818-2 specification. Up to MP@HL decoding. Resolution support up to 1920 × 1088 (maximum 1080p @ 60 fps).
    - MJPEG implementation is based on the ISO/IEC 10918-1 specification. Supports Baseline (DCT based, interleaved only). JFIF input format, 4:2:0 and 4:2:2 format support. Reference performance is 1080p @ 60 fps. MJPEG decoder can operate concurrently with other video decode or encode operations.
  - Microsoft DirectX Video Acceleration (DXVA) application interface (API) for Windows® operating systems.
- HEVC (H.265) Video Encoding acceleration technology:
  - HEVC encoder is frame interleaved with Video Decoder hardware (UVD) H.264, HEVC, VC-1, MPEG-4. and MPEG-2 decode:
    - HEVC encoding is based on the ISO/IEC 23008-2 specification.
    - Up to main profile @ level 5.0 High-Tier (4096 × 2160p @ 30fps) I and P frame (no B-frame) encode.
    - Multi-stream support with total throughput up to 1080p @ 120 fps.
    - Constant bit rate and variable bit rate rate controls.

- Video processing acceleration:
  - Video scaling and YCrCb to RGB color space conversion for video playback and fully adjustable color controls.
  - Motion Adaptive and Vector based deinterlacing filter eliminates video artifacts caused by displaying interlaced video on non-interlaced displays, and by analyzing image and using optimal deinterlacing function on a per-pixel basis.
  - HD HQV and SD HQV support: noise removal, detail enchantment, color enhancement, cadence detection, sharpness, and advanced deinterlacing.
  - Advanced upscaling of SD content to HD resolution.
  - Multi-planes compositing engine for Blu-ray player applications.
- Supports top-quality DVD and Blu-ray disc playback with the lowest CPU usage.

## 2.5 Video Codec Engine (VCE) Features

- Video encoding technology:
  - Video codec engine (VCE):
    - H.264 encoding is based on the ISO/IEC 14496-10 specification.
    - Up to Main Profile @ level 5.1 (3840 × 2160p @ 30 fps) I & P-frame (no B-frame) encode.
    - Multi-stream support with total throughput up to 1080p @ 120 fps.
    - Wi-Fi Display (WFD) compliant H.264 video encoding, and MPEG-2 transport stream generation, including audio muxing support for LPCM or non-LPCM (AC3/AAC) format audio with two channels up to 48 kHz.
    - HDCP2.0/2.1 encryption of protected content in WFD mode.
    - H.264 Scalable Video Coding (SVC) temporal video encoding.
    - Constant bit rate and variable bit rate rate controls.

## 2.6 PCI Express® Bus Support Features

- Compliant with the PCI Express® Base Specification Revision 3.0, up to 8.0 GT/s.
- Supports ×1, ×2, ×4, ×8, and ×16 lane widths.
- Supports 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s link-data rates.
- Supports ×16 lane reversal where the receivers on lanes 0 to 15 on the graphics endpoint are mapped to the transmitters on lanes 15 down to 0 on the root complex.
- Supports ×16 lane reversal where the transmitters on lanes 0 to 15 on the graphics endpoint are mapped to the receivers on lanes 15 down to 0 on the root complex (requires corresponding support on the root complex).
- Supports full-swing and low-swing transmitter output levels.

## 2.7 Power Management Features

- Single-chip solution in 14 nm.
- Full ACPI 1.0b, OnNow, and IAPC (instantly available PC) power management.
- Intelligent power control through AMD PowerTune technology.
- Clocks to every major functional block are controlled by a unique dynamic clock-switching technique which is completely transparent to the software. By turning off the clock to a block that is idle or not in use, power consumption is significantly reduced during normal operation.
- Dynamic Power Management (DPM) defines multiple power levels (up to eight) to achieve best overall performance and idle power.

## 2.8 Spread-spectrum Support

### 2.8.1 Engine and Memory Spread-spectrum Support

- Internal engine and memory spread-spectrum support:
  - Internal engine spread-spectrum support programmable from 0% to 2% down spread with modulation frequencies from 30 kHz to 33 kHz.
  - Internal memory spread-spectrum support programmable from 0% to 1.25% down spread with modulation frequencies from 30 kHz to 33 kHz.
- External memory spread-spectrum support:
  - For GDDR5 memory, the external spread-spectrum clock is not supported. Only internal spread spectrum is supported for GDDR5 memory.

### 2.8.2 DisplayPort Internal Spread-spectrum Support

- From 0.25% to 0.5% down spread.
- Modulation frequency between 30 kHz and 33 kHz.

## 2.9 Internal Thermal Sensor

"Polaris 20" has an integrated thermal sensor that offers the following advantages:

- Provides GPU die temperature (accuracy ± 3°C) without the need for an external chip.
- High- and low-notification limits can be defined to generate interrupts and to change power states.
- Can be used to control a fan through PWM (see Table 3–17 (p. 32)).
- A critical temperature limit can be defined to allow the system to protect the GPU from damage (see GPIO_19_CTF).
- Temperature information can be provided through software (ACPI control methods) or directly through the SMBus hardware interface.

## 2.10 Thermal Diode

The thermal diode in "Polaris 20" is a grounded collector PNP BJT and is compatible with most temperature monitor chips from ADI, such as ADM 1020 and ADM 1030, TI, Maxim, and National Semiconductor. The thermal diode has two pins for its interface—DPLUS and DMINUS (see Table 3–17 (p. 32)). DPLUS connects to the emitter of the BJT while DMINUS connects to its base. The collector is tied to substrate ground.

**Note:** The thermal diode can only be used when the GPU is powered; for example, it cannot be used when in D3 cold. The 3.3-V supply has to be active for temperature sensing to work because of the ESD protection diodes.

## 2.11 Logo Compliance

This product complies with the Windows Logo Program requirements for all target operating systems. This includes both the current logo and future (draft) requirements that will be enforced during the lifespan of the product.

## 2.12 Test Capability Features

"Polaris 20" has a variety of test modes and capabilities that provide a high-fault coverage and low-DPM (defect per million) ratio:

- Full-scan implementation on the digital core logic which provides high-fault coverage through ATPG (automatic test-pattern generation) vectors.
- Dedicated test logic for the on-chip custom memory macros to provide complete coverage on these modules.
- JTAG (Joint Test Action Group) test mode, largely compliant with the IEEE 1149.1 standard, with internal scan chain for access to chip-level test functions and some board-level connectivity testing.
- Integrated hardware-diagnostic tests performed automatically upon initialization.
- Improved access to analog modules and PLLs to allow full evaluation and characterization of these modules.

## 2.13 Other Features

- Support for serial-ROM video BIOS.
- Support for 32- and 64-bit operating systems based on Intel, AMD, and PowerPC CPUs.

## 2.14 Export Control Classification

For information on the export control classification of this product, please contact dl.exportcontrol@amd.com.

# 3

# Signal Descriptions

This section describes the signals of "Polaris 20".

**The following conventions are used:**

- All active low signals are shown with the suffix “B”, such as CASA0B.
- “PD” denotes a permanent internal pull down. “PD-register” denotes an internal pull down which is register controlled, and by default is turned off. “PD-reset” denotes an internal pull down which is register controlled, and by default is turned on. “PD-reset” also denotes that the internal pull down is active during reset. “PD” or “PD-reset” is not relevant when the pins are in output modes.
- To designate a group of pins that have the same pin name but are distinguished by a trailing number only, such as QSA_0, QSA_1, or QSA_2, the abbreviation “Pin name[y:x]” is used. For example, QSA_[7:0] means pins QSA_7 to QSA_0.
- In the "Polaris 20" pin assignment:
  - NC or NC_*: Pins marked as NC are free pins that have no electrical connection on the GPU package.
  - RSVD: These pins should float (i.e., no electrical connection) on the PCB.

To go to a topic of interest, use the following list of linked cross-references:

## 3.1 Pin Assignments

Table 3–1 Pin Assignment - Left Half

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | VSS | DQB1_31 | | DDBIB1_3 | VSS | | WCKB1_1 | DQB1_23 | | VSS | EDCB1_2 | | DQB1_18 | VSS | | DQB0_21 | EDCB0_2 | VSS | DQB0_17 | WCKB0_1 | |
| B | VSS | VSS | | DQB1_30 | EDCB1_3 | DQB1_27 | | VSS | WCKB1B_1 | | DQB1_21 | VSS | | DQB1_19 | DQB1_16 | | VSS | DQB0_20 | DQB0_19 | VSS | WCKB0B_1 | |
| C | DQC0_0 | | | DQB1_29 | VSS | DQB1_26 | | DQB1_24 | VSS | | DQB1_22 | DDBIB1_2 | | VSS | DQB1_17 | | DQB0_22 | VSS | DDBIB0_2 | DQB0_16 | VSS | |
| D | | DQC0_1 | DQC0_2 | | DQB1_28 | VSS | | DQB1_25 | EDCB1_1 | | VSS | DQB1_20 | | DQB1_6 | VSS | | DQB0_23 | DQB0_15 | VSS | DQB0_18 | DQB0_31 | |
| E | DDBIC0_0 | EDCC0_0 | VSS | DQC0_3 | VSS | VMEMIO | | VSS | DQB1_12 | | DQB1_9 | VMEMIO | | DQB1_7 | EDCB1_0 | | VMEMIO | DQB0_14 | DQB0_12 | VMEMIO | DQB0_8 | |
| F | VSS | DQC0_4 | DQC0_5 | VSS | VMEMIO | VSS | | DQB1_15 | VSS | | DQB1_10 | WCKB1_0 | | VSS | DQB1_4 | | DQB1_2 | VSS | DQB0_13 | DQB0_11 | VSS | |
| G | | | | | | | | | DQB1_13 | | VMEMIO | WCKB1B_0 | | CLKB1B | VMEMIO | | DQB1_3 | DQB1_0 | VMEMIO | DQB0_10 | WCKB0_0 | |
| H | WCKC0_0 | VSS | DQC0_7 | DQC0_6 | VSS | DQC0_16 | | VSS | DQB1_14 | | DQB1_11 | VSS | | CLKB1 | DQB1_5 | | VSS | DQB1_1 | DDBIB0_1 | VSS | WCKB0B_0 | |
| J | DQC0_8 | WCKC0B_0 | VSS | EDCC0_2 | DQC0_19 | VSS | DQC0_18 | DQC0_17 | VSS | | DDBIB1_1 | DQB1_8 | | VMEMIO | MAB1_5 | | DDBIB1_0 | VMEMIO | EDCB0_1 | DQB0_9 | VSS | |
| K | | | | | | | | | | | | CSB1B_0 | | MAB1_9 | VSS | | MAB1_1 | MAB1_7 | VSS | RASB0B | CASB0B | |
| L | VSS | DQC0_10 | DQC0_9 | VSS | DQC0_22 | DQC0_21 | VSS | DQC0_20 | DDBIC0_2 | | VSS | VSS | | VSS | MAB1_4 | | VMEMIO | MAB1_8 | ADBIB1 | VMEMIO | ADBIB0 | |
| M | EDCC0_1 | VSS | DDBIC0_1 | DQC0_11 | VMEMIO | WCKC0_1 | WCKC0B_1 | VSS | DQC0_23 | CSC0B_0 | VSS | VMEMIO | | DRAM_RSTB | WEB1B | | MAB1_3 | VSS | CASB1B | RASB1B | VSS | |
| N | | | | | | | | | | | | | | | VMEMIO | | MAB1_2 | MAB1_0 | VMEMIO | CKEB1 | CKEB0 | |
| P | DQC0_13 | DQC0_12 | VSS | DQC0_25 | DQC0_24 | VSS | CLKC0B | CLKC0 | VSS | MAC0_9 | VSS | DRAM_RSTC | | VMEMIO | MEM_CALRB | | VSS | VSS | MAB1_6 | MVREFDB | VDDCI | |
| R | VSS | DQC0_15 | DQC0_14 | VSS | EDCC0_3 | DQC0_27 | VMEMIO | DQC0_26 | MAC0_5 | VSS | MAC0_4 | WEC0B | VMEMIO | MEM_CALRC | VSS | VDDCI | VSS | VDDCI | VDDCI | VDDCI | VSS | VSS |
| T | | | | | | | | | | | | | | | VDDCI | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| U | DQC1_10 | VSS | DQC1_9 | DQC1_8 | VMEMIO | DQC0_29 | DQC0_28 | VSS | DDBIC0_3 | MAC0_1 | VMEMIO | MAC0_3 | MAC0_2 | VSS | VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| V | EDCC1_1 | DQC1_11 | VSS | DQC1_16 | DQC1_17 | VSS | DQC0_31 | DQC0_30 | VMEMIO | MAC0_7 | MAC0_8 | VSS | MAC0_0 | TEST6 | VDDCI | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| W | VSS | DQC1_12 | DDBIC1_1 | VSS | DQC1_19 | DQC1_18 | VMEMIO | DDBIC1_2 | EDCC1_2 | VSS | ADBIC0 | CASC0B | VMEMIO | MAC0_6 | VDDCI | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| Y | DQC1_14 | VSS | DQC1_15 | DQC1_13 | VSS | DQC1_20 | DQC1_21 | VSS | DQC1_22 | RASC1B | VMEMIO | RASC0B | CKEC0 | MVREFDC | VDDCI | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| AA | WCKC1_0 | WCKC1B_0 | VSS | DQC1_0 | DQC1_23 | VSS | WCKC1_1 | WCKC1B_1 | VSS | CASC1B | ADBIC1 | VSS | CKEC1 | VDDCI | VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| AB | | | | | | | | | | | | | | | VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| AC | DQC1_2 | DQC1_1 | VSS | DQC1_26 | DQC1_25 | VSS | DQC1_24 | MAC1_0 | VMEMIO | MAC1_8 | MAC1_7 | VSS | MAC1_6 | VDDCI | VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| AD | DQC1_3 | VSS | DDBIC1_0 | EDCC1_0 | VSS | EDCC1_3 | DDBIC1_3 | VSS | DQC1_27 | MAC1_2 | VMEMIO | MAC1_3 | MAC1_1 | VSS | VDDCI | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| AE | VSS | DQC1_5 | DQC1_4 | VSS | DQC1_30 | DQC1_29 | VMEMIO | DQC1_28 | WEC1B | VSS | MAC1_4 | MAC1_5 | VMEMIO | MVREFDD | VDDCI | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| AF | DQC1_7 | DQC1_6 | VSS | DQD0_2 | DQD0_1 | VSS | DQD0_0 | VSS | VMEMIO | DQC1_31 | CSC1B_0 | VSS | CLKC1B | CLKC1 | VDDCI | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| AG | DQD0_16 | VSS | DQD0_17 | DQD0_18 | VMEMIO | DQD0_3 | EDCD0_0 | VSS | MAC1_9 | VSS | VMEMIO | CSD0B_0 | MAD0_9 | VSS | VSS | VDDCI | VDDC | VSS | VSS | VDDC | VDDC | VSS |
| AH | | | | | | | | | | | | | | | VDDCI | VSS | VDDCI | VDDC | VDDC | VDDC | VDDC | VDDC |
| AJ | VSS | DQD0_19 | EDCD0_2 | VSS | DQD0_5 | DQD0_4 | VMEMIO | DDBID0_0 | DQD0_6 | VSS | CLKD0B | CLKD0 | VMEMIO | VSS | VSS | VDDCI | VSS | VDDCI | VDDC | VDDC | VDDC | VDDC |
| AK | DDBID0_2 | DQD0_20 | VSS | WCKD0_0 | WCKD0B_0 | VSS | DQD0_7 | WED0B | VMEMIO | MAD0_4 | MAD0_5 | VSS | | VMEMIO | VSS | | VSS | VSS | DRAM_RSTD | VSS | FB_VSS | |
| AL | | | | | | | | | | | | | | | VMEMIO | | MAD1_8 | MAD1_2 | VMEMIO | MEM_CALRD | FB_VDDC | |
| AM | DQD0_23 | VSS | DQD0_22 | DQD0_21 | VMEMIO | DQD0_9 | DQD0_8 | VSS | MAD0_2 | MAD0_3 | VSS | MAD0_1 | | VSS | CASD1B | | MAD1_0 | VSS | CLKD1 | DRAIN | GATE | |
| AN | VSS | WCKD0_1 | WCKD0B_1 | VSS | DQD0_11 | DQD0_10 | VMEMIO | MAD0_0 | MAD0_8 | | MAD0_7 | VSS | | RASD1B | MAD1_6 | | VMEMIO | MAD1_5 | CLKD1B | VMEMIO | DBGDATA_10 | |
| AP | | | | | | | | | | | | CKED0 | | CKED1 | VSS | | MAD1_1 | WED1B | VSS | CSD1B_0 | DBGDATA_11 | |
| AR | DQD0_24 | DQD0_25 | VSS | EDCD0_1 | DDBID0_1 | VSS | DQD0_12 | MAD0_6 | VSS | | CASD0B | RASD0B | | VMEMIO | MAD1_7 | | MAD1_3 | VMEMIO | MAD1_9 | DBGDATA_5 | DBGDATA_15 | |
| AT | DQD0_26 | VSS | DQD0_27 | DDBID0_3 | VSS | DQD0_13 | | DQD0_14 | ADBID0 | | DQD1_7 | VSS | | ADBID1 | DQD1_12 | | VSS | MAD1_4 | DBGDATA_2 | DBGDATA_6 | VSS | |
| AU | | | | | | | | | DQD1_4 | | VMEMIO | DQD1_8 | | DQD1_10 | VMEMIO | | DQD1_14 | VSS | VSS | DBGDATA_9 | DBGDATA_14 | |
| AV | VSS | EDCD0_3 | DQD0_28 | VSS | DQD0_15 | VSS | | EDCD1_0 | VSS | | WCKD1B_0 | DQD1_9 | | VSS | DQD1_13 | | DQD1_15 | DBGDATA_0 | DBGDATA_3 | VSS | DBGDATA_13 | |
| AW | DQD0_29 | VSS | DQD1_0 | DQD1_1 | VSS | DDBID1_0 | | VSS | DQD1_5 | | WCKD1_0 | VMEMIO | | DQD1_11 | EDCD1_1 | | VMEMIO | DBGDATA_1 | DBGDATA_4 | DBGDATA_8 | DBGDATA_12 | |
| AY | | DQD0_30 | VSS | | DQD1_3 | VSS | | DDBID1_2 | DQD1_6 | | VSS | DQD1_24 | | DDBID1_1 | VSS | | DQD1_29 | VSS | VSS | DBGDATA_7 | TXCEM_DPE3N | |
| BA | DQD0_31 | | | VSS | DQD1_2 | DQD1_19 | | DQD1_20 | VSS | | WCKD1B_1 | DQD1_25 | | VSS | EDCD1_3 | | DQD1_30 | VSS | TX0M_DPF2N | TX0P_DPF2P | VSS | |
| BB | VSS | VSS | | DQD1_16 | VSS | EDCD1_2 | | VSS | DQD1_22 | | WCKD1_1 | VSS | | DQD1_27 | DQD1_28 | | VSS | VSS | TXCFM_DPF3N | TX1P_DPF1P | TX2M_DPF0N | |
| BC | | VSS | DQD1_17 | | DQD1_18 | VSS | | DQD1_21 | DQD1_23 | | VSS | DQD1_26 | | DDBID1_3 | VSS | | DQD1_31 | VSS | TXCFP_DPF3P | TX1M_DPF1N | TX2P_DPF0P | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |

Table 3–2 Pin Assignment - Right Half

| 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DQB0_29 | DQB0_28 | VSS | DQB0_24 | DQA1_15 | | VSS | DDBIA1_1 | | DQA1_8 | VSS | | DQA1_7 | DQA1_5 | | VSS | DQA1_2 | | DQA1_0 | VSS | | A |
| DQB0_30 | VSS | DQB0_27 | DQB0_25 | VSS | | DQA1_12 | DQA1_11 | | VSS | WCKA1_0 | | DQA1_6 | VSS | | EDCA1_0 | VSS | DQA1_1 | | VSS | VSS | B |
| VSS | DDBIB0_3 | DQB0_26 | VSS | DQA1_14 | | EDCA1_1 | VSS | | DQA1_9 | WCKA1B_0 | | VSS | DQA1_4 | | DQA1_3 | DQA0_31 | VSS | | | DQA0_14 | C |
| DQB0_5 | EDCB0_3 | VSS | DQA1_29 | DQA1_13 | | VSS | WCKA1_1 | | DQA1_10 | VSS | | EDCA1_2 | DDBIA1_0 | | VSS | DQA0_30 | | VSS | DQA0_15 | | D |
| DQB0_6 | VSS | DQB0_1 | DQA1_30 | VMEMIO | | DQA1_26 | WCKA1B_1 | | VMEMIO | DQA1_20 | | DDBIA1_2 | VSS | | DQA1_16 | VSS | DQA0_28 | DQA0_29 | VSS | DQA0_13 | E |
| VSS | EDCB0_0 | DQB0_2 | VSS | DQA1_28 | | DQA1_27 | VSS | | DQA1_22 | DQA1_21 | | VSS | DQA1_18 | | VSS | DDBIA0_3 | VSS | DQA0_12 | EDCA0_1 | VSS | F |
| DQB0_7 | DDBIB0_0 | VMEMIO | DQA1_31 | EDCA1_3 | | VMEMIO | DQA1_24 | | DQA1_23 | VMEMIO | | DQA1_19 | | | | | | | | | G |
| MAB0_0 | VSS | DQB0_3 | VSS | VSS | | DDBIA1_3 | WEA1B | | VSS | MAA1_0 | | MAA1_6 | DQA1_17 | | EDCA0_3 | VSS | DDBIA0_1 | DQA0_11 | VSS | DQA0_10 | H |
| VMEMIO | DQB0_4 | WEB0B | VMEMIO | MAB0_9 | | DQA1_25 | VMEMIO | | MAA1_2 | MAA1_8 | | VSS | ADBIA1 | DQA0_27 | VSS | DQA0_26 | DQA0_25 | VSS | DQA0_9 | DQA0_8 | J |
| MAB0_8 | MAB0_2 | VSS | DQB0_0 | VSS | | VSS | MAA1_4 | | MAA1_3 | | | | | | | | | | | | K |
| MAB0_7 | VMEMIO | MAB0_4 | CSB0B_0 | VMEMIO | | CLKA1B | MAA1_5 | | VSS | MAA1_7 | | CASA1B | DQA0_24 | VMEMIO | WCKA0B_1 | WCKA0_1 | VSS | WCKA0B_0 | WCKA0_0 | VSS | L |
| VSS | MAB0_3 | MAB0_5 | VSS | CSA1B_0 | | CLKA1 | VSS | | MAA1_1 | VSS | CKEA1 | RASA1B | VSS | DQA0_23 | DQA0_22 | VMEMIO | DQA0_7 | DQA0_6 | VSS | DQA0_5 | M |
| MAB0_6 | MAB0_1 | VMEMIO | CLKB0B | MAA1_9 | | VMEMIO | | | | | | | | | | | | | | | N |
| VDDCI | VSS | MVREFDA | CLKB0 | VSS | | VSS | VMEMIO | | VSS | RASA0B | CKEA0 | VMEMIO | ADBIA0 | DQA0_21 | VSS | DQA0_20 | DDBIA0_2 | VSS | DQA0_4 | DDBIA0_0 | P |
| VSS | VDDCI | VDDCI | VDDCI | VSS | VDDCI | VSS | VSS | VMEMIO | CASA0B | MAA0_6 | VSS | MAA0_7 | DQA0_19 | VMEMIO | DQA0_18 | EDCA0_2 | VSS | EDCA0_0 | DQA0_3 | VSS | R |
| VSS | VDDC | VDDC | VSS | VDDCI | VSS | VDDCI | | | | | | | | | | | | | | | T |
| VSS | VDDC | VDDC | VSS | VSS | VDDCI | VSS | VSS | MAA0_8 | MAA0_0 | VMEMIO | MAA0_1 | MAA0_3 | VSS | DQA0_17 | DQA0_16 | VMEMIO | DQA0_2 | DQA0_1 | VSS | DQA0_0 | U |
| VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDCI | VSS | MAA0_2 | VSS | MAA0_5 | WEA0B | VMEMIO | MAA0_4 | VSS | GPIO_1 | GPIO_0 | PX_EN | GPIO_13 | GPIO_12 | GPIO_11 | V |
| VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | DRAM_RSTA | VMEMIO | CLKA0 | CLKA0B | VSS | MAA0_9 | VSS | GPIO_2 | VSS | VSS | VSS | VSS | PCIE_RX15P | PCIE_RX15N | W |
| VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | VSS | MEM_CALRA | TEST_PG_BACO | VMEMIO | CSA0B_0 | VSS | VSS | VSS | PCIE_TX15P | PCIE_TX15N | VSS | PCIE_RX13N | PCIE_RX14N | PCIE_RX14P | Y |
| VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | TS_A | TEST_PG | VSS | VSS | VDD_08 | VDD_08 | VSS | PCIE_TX13N | PCIE_TX14N | PCIE_TX14P | VSS | PCIE_RX13P | PCIE_RX12P | PCIE_RX12N | AA |
| VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | | | | | | | | | | | | | | | AB |
| VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | JTAG_TRSTB | GPIO_19_CTF | VSS | VSS | DMINUS | DPLUS | VSS | PCIE_TX13P | PCIE_TX12P | PCIE_TX12N | VSS | VSS | PCIE_RX11N | PCIE_RX11P | AC |
| VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | JTAG_TDI | JTAG_TDO | VSS | DDCVGADATA | DDCVGACLK | VSS | VDD_08 | VSS | PCIE_TX11N | PCIE_TX11P | VSS | PCIE_RX9N | PCIE_RX10N | PCIE_RX10P | AD |
| VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | TESTEN | JTAG_TMS | VSS | GPIO_17_THERMAL_INT | GPIO_6_TACH | VDD_08 | VSS | PCIE_TX9N | PCIE_TX10N | PCIE_TX10P | VSS | PCIE_RX9P | PCIE_RX8P | PCIE_RX8N | AE |
| VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | JTAG_TCK | GPIO_28_FDO | VSS | SDA | SCL | VDD_08 | VSS | PCIE_TX9P | PCIE_TX8P | PCIE_TX8N | VSS | VSS | PCIE_RX7N | PCIE_RX7P | AF |
| VSS | VDDC | VDDC | VSS | VSS | VDDC | VDDC | GPIO_30 | GPIO_29 | VSS | TEMPIN0 | TEMPINRETURN | VSS | VDD_08 | VSS | PCIE_TX7N | PCIE_TX7P | VSS | PCIE_RX5N | PCIE_RX6N | PCIE_RX6P | AG |
| VDDC | VDDC | VDDC | VDDC | VDDC | VDDC | VDDC | | | | | | | | | | | | | | | AH |
| VDDC | VDDC | VDDC | VDDC | VDDC | VDDC | VSS | VDD_08 | GPIO_15 | VSS | GPIO_16_8P_DETECT | GPIO_5_REG_HOT_AC_BATT | VDD_08 | VSS | PCIE_TX5N | PCIE_TX6N | PCIE_TX6P | VSS | PCIE_RX5P | PCIE_RX4P | PCIE_RX4N | AJ |
| FB_VDDCI | VSS | DIGON | BL_ENABLE | VSS | | VSS | PCIE_ZVSS | | VSS | GPIO_20 | GPIO_21 | VDD_08 | VSS | PCIE_TX5P | PCIE_TX4P | PCIE_TX4N | VSS | VSS | PCIE_RX3N | PCIE_RX3P | AK |
| VSS | VDD_33 | VSS | BL_PWM_DIM | GENLK_VSYNC | | VSS | | | | | | | | | | | | | | | AL |
| GPIO_SVC | VDD_33 | VDD_18 | VSS | GENLK_CLK | | PLLCHARZ_H | GPIO_10_ROMSCK | | VSS | SMBDAT | SMBCLK | VSS | VDD_08 | VSS | PCIE_TX3N | PCIE_TX3P | VSS | PCIE_RX1N | PCIE_RX2N | PCIE_RX2P | AM |
| GPIO_SVT | VSS | VDD_18 | VDD_18 | VSS | | PLLCHARZ_L | GPIO_8_ROMSO | | GPIO_22_ROMCSB | VSS | | VDD_08 | VSS | PCIE_TX1N | PCIE_TX2N | PCIE_TX2P | VSS | PCIE_RX1P | PCIE_RX0P | PCIE_RX0N | AN |
| GPIO_SVD | HSYNC | VSS | VDD_18 | VDD_18 | | VSS | VSS | | GPIO_9_ROMSI | | | | | | | | | | | | AP |
| DDC1DATA | VSYNC | SWAPLOCKB | TSVDD | VDD_18 | | GPIO_14_HPD2 | GENERICD | | VSS | VSS | | VSS | VSS | PCIE_TX1P | PCIE_TX0P | PCIE_TX0N | VSS | VSS | PCIE_REFCLKP | PCIE_REFCLKN | AR |
| DDC1CLK | GENERICB | SWAPLOCKA | VSS | VSS | | GPIO_18_HPD3 | GENERICC | | HPD1 | DDCAUX4N | | VSS | DP_ZVDD_08 | | VSS | VSS | VSS | VSS | VSS | VSS | AT |
| VSS | VSS | VSS | DDC2CLK | DDCAUX3P | | GENERICE_HPD4 | GENERICF_HPD5 | | GENERICG_HPD6 | DDCAUX4P | | DDCAUX5P | | | | | | | | | AU |
| AUX1P | BP_1 | AUX2P | DDC2DATA | DDCAUX3N | | VSS | VSS | | VSS | VSS | | DDCAUX5N | DP_ZVSS | | VSS | VSS | VSS | CLKREQB | PERSTB | WAKEB | AV |
| AUX1N | BP_0 | AUX2N | VSS | VSS | | VSS | VSS | | VSS | VSS | | VSS | VSS | | VSS | VSS | GENERICA | VSS | ANALOGIO | VSS | AW |
| TXCEP_DPE3P | AUX_ZVSS | VSS | TX1M_DPD1N | TX1P_DPD1P | | TX3M_DPC2N | TX3P_DPC2P | | TXCBM_DPB3N | TXCBP_DPB3P | | TX2M_DPB0N | TX2P_DPB0P | | TX4M_DPA1N | TX4P_DPA1P | | VSS | XTALOUT | | AY |
| VSS | TX5M_DPE0N | TX5P_DPE0P | VSS | VSS | | VSS | VSS | | VSS | VSS | | VSS | VSS | | VSS | VSS | VSS | | | XTALIN | BA |
| TX3P_DPE2P | TX4M_DPE1N | TXCDP_DPD3P | TX0M_DPD2N | TX2P_DPD0P | | TXCCM_DPC3N | TX4P_DPC1P | | TX5M_DPC0N | TX0P_DPB2P | | TX1M_DPB1N | TXCAP_DPA3P | | TX3M_DPA2N | TX5P_DPA0P | DDCAUX6N | | VSS | VSS | BB |
| TX3M_DPE2N | TX4P_DPE1P | TXCDM_DPD3N | TX0P_DPD2P | TX2M_DPD0N | | TXCCP_DPC3P | TX4M_DPC1N | | TX5P_DPC0P | TX0M_DPB2N | | TX1P_DPB1P | TXCAM_DPA3N | | TX3P_DPA2P | TX5M_DPA0N | | DDCAUX6P | VSS | | BC |
| 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | |

## 3.2 PCI Express® Bus Interface

For more information on signal definitions and electrical requirements, refer to the *PCI Express® Card Electromechanical 3.0 Specification* and *PCI Express Base 3.0 Specification*.

**Note:**

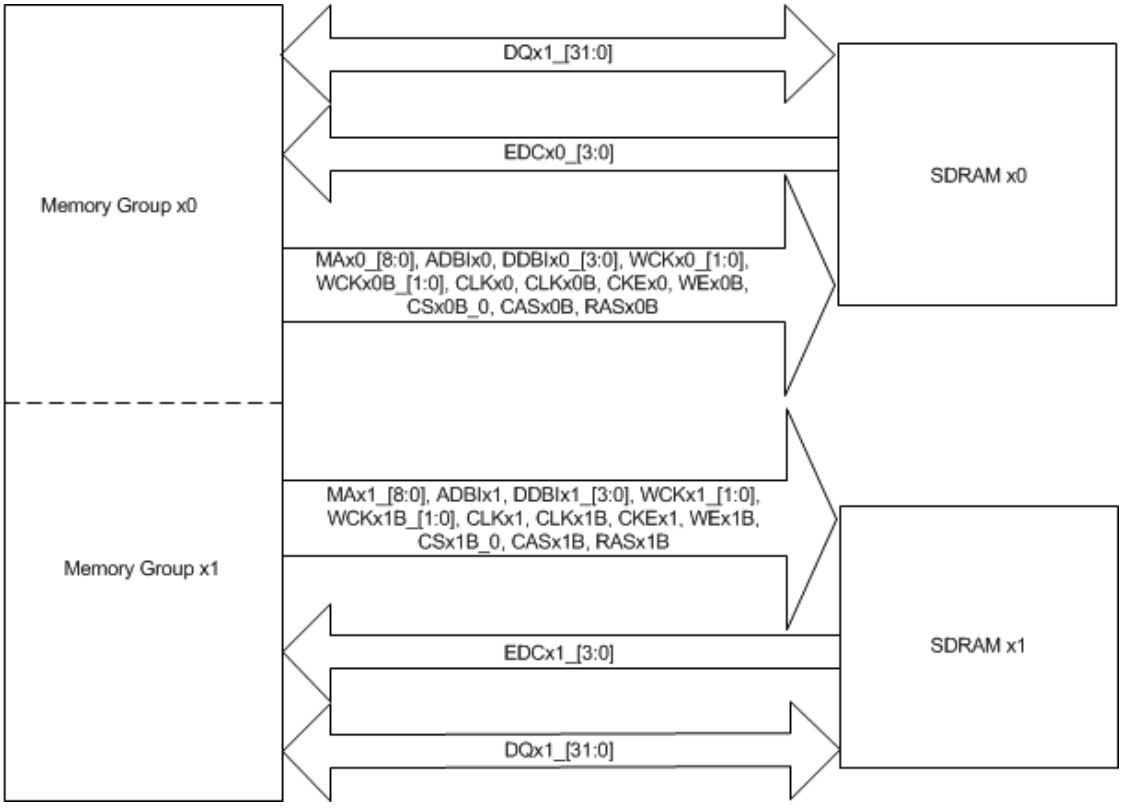
- "Polaris 20" supports ×16 lane reversal, where the receivers on lanes 0 to 15 of the graphics endpoint are mapped to the transmitter on lanes 15 down to 0 of the root complex. If ×16 lane reversal is employed, both the receive and transmit lanes must be reversed. In addition, polarity inversion is supported, such as when the + of the differential pair is connected to the - at the root complex.
- 220-nF AC-coupling capacitors are required.

Table 3–3 PCI Express® Bus Interface

| Pin Name | I/O | Description |
|---|---|---|
| PERSTB | I | Fundamental reset.<br>3.3-V tolerant pad.<br>This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.<br>A buffered reset signal dedicated to the GPU is required. |
| PCIE_REFCLKP/N | I | PCI Express PLL differential reference clock (+/-).<br>100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing. |
| PCIE_TX[15:0]P/N | O | PCI Express transmitter output data channel TX[15:0] (+/-).<br>Differential serial data transmitted up to 8.0-GT/s bit rate. |
| PCIE_RX[15:0]P/N | I | PCI Express receiver input data channel RX[15:0] (+/-).<br>Differential serial data received up to 8.0-GT/s bit rate. |
| PCIE_ZVSS | I | Connect to VSS through a 180Ω (1% tolerance) resistor. |
| CLKREQB | I/O | CLKREQB only: CLKREQB is an open drain output on the GPU and an input on the platform which can be used to request the PCIe® reference clock to GPU on or off.<br>L1 PM Substates: CLKREQB is a bi-directional open drain that can be asserted by either the GPU or the platform to initiate an L1 exit. |
| WAKEB | I | WAKEB is used as an input for the PCIe Optimized Buffer Flush/Fill (OBFF) feature.<br>OBFF serves as a mechanism for the platform to tune power management (PM), and to align device activities.<br>The signaling on WAKEB helps to tell the system status (CPU active or idle). The PCIe device will respond to this information to control its upstream traffic.<br>Support from the platform is required. |

## 3.3 Memory Interface (SGRAM, SDRAM)

Figure 3–1 Memory Interface




**Note:**

- A lower-case "x" is used to represent any of the available primary 64-bit-wide memory channels. "Polaris 20" uses memory groups A, B, C, and D.
- A "0" or "1" after "x" is used to separate the 64-bit-wide memory channel into two 32-bit wide sub-channels.
- "Polaris 20" supports GDDR5 memory with the mapping shown in Table 3–5 (p. 22).

Table 3–4 Memory Interface

| Pin Name | Type | Description |
|---|---|---|
| **MEM_CALRx** | I | Connect to VSS through a 120-Ω (± 0.5%) resistor. Preferred resistor tolerance is 0.5%, but 1% is acceptable. |
| **DQx0_[31:0]** | I/O | Memory data bus for channel x0. |
| **DQx1_[31:0]** | I/O | Memory data bus for channel x1. |
| **MAx0_[9:0]** | O | Memory address bus for channel x0.<br>Supplies bank addresses and row/column addresses for one 32-bit interface. |
| **MAx1_[9:0]** | O | Memory address bus for channel x1.<br>Supplies bank addresses and row/column addresses for one 32-bit interface. |
| **EDCx0_[3:0]** | I | Error detection pins. |
| **EDCx1_[3:0]** | I | Error detection pins. |
| **ADBIx0** | O | Address dynamic bus inversion for channel x0. |

| Pin Name | Type | Description |
|---|---|---|
| **ADBIx1** | O | Address dynamic bus inversion for channel x1. |
| **DDBIx0_[3:0]** | I/O | Data dynamic bus inversion. |
| **DDBIx1_[3:0]** | I/O | Data dynamic bus inversion. |
| **WCKx0_[1:0]**<br>**WCKx0B_[1:0]** | O | Forwarded clock. |
| **WCKx1_[1:0]**<br>**WCKx1B_[1:0]** | O | Forwarded clock. |
| **CLKx0**<br>**CLKx0B** | O | Differential memory clock for channel x0. |
| **CLKx1**<br>**CLKx1B** | O | Differential memory clock for channel x1. |
| **CKEx0** | O | Clock enable control for channel x0. |
| **CKEx1** | O | Clock enable control for channel x1. |
| **WEx0B** | O | Write enable for channel x0. |
| **WEx1B** | O | Write enable for channel x1. |
| **CSx0B_0** | O | Chip select for channel x0. |
| **CSx1B_0** | O | Chip select for channel x1. |
| **CASx0B** | O | Column address strobe for channel x0. |
| **CASx1B** | O | Column address strobe for channel x1. |
| **RASx0B** | O | Row address strobe for channel x0. |
| **RASx1B** | O | Row address strobe for channel x1. |
| **MVREFDx** | A-I | Reference voltage per channel (memory data).<br>0.7 × VMEMIO. |
| **DRAM_RSTx** | O | Reset for all populated DRAMs (active low). |

Table 3–5 GDDR5 Memory Mapping

| **GPU Signal** | MAA0_9 | MAA0_8 | MAA0_7 | MAA0_6 | MAA0_5 | MAA0_4 | MAA0_3 | MAA0_2 | MAA0_1 | MAA0_0 |
|---|---|---|---|---|---|---|---|---|---|---|
| **Memory Signal Mapping when**<br>**MF = 0** | RSVD | A13/A12 | A7/A8 | A6/A11 | A5/BA1 | A4/BA2 | A3/BA3 | A2/BA0 | A1/A9 | A0/A10 |

## 3.4 Display Configuration Overview

"Polaris 20" has six display links, A to F.

Table 3–6 Display Configuration Overview for Links A, B, C, D, E, and F (DisplayPort Version 1.4)

| Pin Name | Possible Display Configurations | | |
|---|---|---|---|
| **TX[5:3]P/M_DPA[0:2]P/N**<br>**TXCAP/M_DPA3P/N** | Single-link DisplayPort/ TMDS | Dual-link DVI | A DisplayPort can be connected to any of links A, B, C, D, E, or F. The six links are independent and can be active simultaneously.<br>HDMI™ can be connected to any of links A, B, C, D, E, or F.<br>Dual-link DVI is available on links A and B, C and D, or E and F, respectively.<br>B, D, or F must be the master link for the respective dual-link pair. |
| **TX[2:0]P/M_DPB[0:2]P/N**<br>**TXCBP/M_DPB3P/N** | Single-link DisplayPort/ TMDS | | |
| **TX[5:3]P/M_DPC[0:2]P/N**<br>**TXCCP/M_DPC3P/N** | Single-link DisplayPort/ TMDS | Dual-link DVI | |
| **TX[2:0]P/M_DPD[0:2]P/N**<br>**TXCDP/M_DPD3P/N** | Single-link DisplayPort/ TMDS | | |
| **TX[5:3]P/M_DPE[0:2]P/N**<br>**TXCEP/M_DPE3P/N** | Single-link DisplayPort/ TMDS | Dual-link DVI | |
| **TX[2:0]P/M_DPF[0:2]P/N**<br>**TXCFP/M_DPF3P/N** | Single-link DisplayPort/ TMDS | | |

## 3.5 Integrated HDMI™/TMDS Interface

"Polaris 20" has six display links, A to F.

**Note:**

- The maximum pixel clock rate is 594 MHz on direct connectors. The GPU and HDMI connector are on the same PCB with a maximum trace length of 127 mm or 5 inches, and may be affected by TMDS signals layout and trace lengths.
- For unused interfaces, all signal outputs can be unconnected. AUX_ZVSS, DP_ZVDD_08, and DP_ZVSS should always be connected.

Please refer to the *Digital Visual Interface (DVI) 1.0 Specification* and the *High-Definition Multimedia Interface (HDMI) Specification* for additional details.

Table 3–7 Integrated HDMI™/TMDS Interface

| Pin Name | Type | Description |
|---|---|---|
| **TX[5:3]P/M_DPA[0:2]P/N**<br>**TX[2:0]P/M_DPB[0:2]P/N**<br>**TX[5:3]P/M_DPC[0:2]P/N**<br>**TX[2:0]P/M_DPD[0:2]P/N**<br>**TX[5:3]P/M_DPE[0:2]P/N**<br>**TX[2:0]P/M_DPF[0:2]P/N** | O | TMDS data pairs (+/-).<br>For single- and dual-link configurations.<br>Transmitting at a bit rate of 10× pixel clock, up to 594-MHz pixel clock.<br>A 100-nF capacitor is required on each differential signal placed near the connector.<br>A 500-Ω resistor to ground is required on each differential-signal line. One FET is needed to disconnect the path from the 500-Ω resistors to ground when the system is off and the panel is on. |
| **TXCAP/M_DPA3P/N**<br>**TXCBP/M_DPB3P/N**<br>**TXCCP/M_DPC3P/N**<br>**TXCDP/M_DPD3P/N**<br>**TXCEP/M_DPE3P/N**<br>**TXCFP/M_DPF3P/N** | O | TMDS clock channels (+/-).<br>For single- and dual-link configurations.<br>A 100-nF capacitor is required on each differential signal placed near the connector.<br>A 500-Ω resistor to ground is required on each differential-signal line. One FET is needed to disconnect the path from the 500-Ω resistors to ground when the system is off and the panel is on.<br>**Note:** TXCBP/M_DPB3P/N, TXCDP/M_DPD3P/N, or TXCFP/M_DPF3P/N should be used as the clock pairs for dual-link configurations. |
| **DDC[2:1]CLK**<br>**DDC[2:1]DATA**<br>**DDCAUX[6:3]N**<br>**DDCAUX[6:3]P** | I/O | Differential signals for HDMI/TMDS DDC. For more details, see Table 3–14 (p. 30).<br>NOT 5-V tolerant. |
| **AUX_ZVSS** | A | Analog calibration.<br>Connect to VSS through a 150-Ω (1%) resistor. |
| **DP_ZVDD_08** | A | Analog calibration.<br>Connect to VDD_08 through a 200-Ω (1%) resistor. |
| **DP_ZVSS** | A | Analog calibration.<br>Connect to GND through a 200-Ω (1%) resistor. |

## 3.6 DisplayPort

**Note:** If this interface is not used, all signal outputs can be unconnected. AUX_ZVSS, DP_ZVDD_08, and DP_ZVSS should always be connected.

"Polaris 20" supports six DisplayPort links.

The GPU and DisplayPort connector are on the same PCB with a maximum trace length of 127 mm or 5 inches.

Please refer to the *DisplayPort Standard Version 1.3* for additional details.

Table 3–8 DisplayPort Interface

| Pin Name | Type | Description |
|---|---|---|
| **TX[5:3]P/M_DPA[0:2]P/N**<br>**TXCAP/M_DPA3P/N** | O | DisplayPort (DPA) differential signals.<br>DPA can be configured as a DisplayPort link.<br>A 100-nF capacitor is required on each differential signal placed near the connector. |
| **TX[2:0]P/M_DPB[0:2]P/N**<br>**TXCBP/M_DPB3P/N** | O | DisplayPort (DPB) differential signals.<br>DPB can be configured as a DisplayPort link.<br>A 100-nF capacitor is required on each differential signal placed near the connector. |
| **TX[5:3]P/M_DPC[0:2]P/N**<br>**TXCCP/M_DPC3P/N** | O | DisplayPort (DPC) differential signals.<br>DPC can be configured as a DisplayPort link.<br>A 100-nF capacitor is required on each differential signal placed near the connector. |
| **TX[2:0]P/M_DPD[0:2]P/N**<br>**TXCDP/M_DPD3P/N** | O | DisplayPort (DPD) differential signals.<br>DPD can be configured as a DisplayPort link.<br>A 100-nF capacitor is required on each differential signal placed near the connector. |
| **TX[5:3]P/M_DPE[0:2]P/N**<br>**TXCEP/M_DPE3P/N** | O | DisplayPort (DPE) differential signals.<br>DPE can be configured as a DisplayPort link.<br>A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector. |
| **TX[2:0]P/M_DPF[0:2]P/N**<br>**TXCFP/M_DPF3P/N** | O | DisplayPort (DPF) differential signals.<br>DPF can be configured as a DisplayPort link.<br>A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector. |
| **AUX[2:1]P/N**<br>**DDCAUX[6:3]N**<br>**DDCAUX[6:3]P** | I/O | DisplayPort auxiliary differential signals.<br>See Table 3–14 (p. 30) |
| **AUX_ZVSS** | A | Analog calibration.<br>Connect to VSS through a 150-Ω (1%) resistor. |
| **DP_ZVDD_08** | A | Analog calibration.<br>Connect to VDD_08 through a 200-Ω (1%) resistor. |
| **DP_ZVSS** | A | Analog calibration.<br>Connect to GND through a 200-Ω (1%) resistor. |

## 3.7 Hardware I²C Interface

Table 3–9 Hardware IC Interface

| Pin Name | Type | Description |
|---|---|---|
| **SCL** | I/O<br>3.3 V<br>(VDD_33) | I²C clock.<br>**Note:** Can be left unconnected if not used. |
| **SDA** | I/O<br>3.3 V<br>(VDD_33) | I²C data/address.<br>**Note:** Can be left unconnected if not used. |

## 3.8 Serial Flash Interface

Configuration straps must be set to identify the appropriate ROM type. See ROM Configurations (p. 38).

Table 3–10 Serial Flash Interface

| Pin Name | Type | PD/PU | Description |
|---|---|---|---|
| **GPIO_8_ROMSO** | I<br>3.3 V<br>(VDD_33) | PD-reset | Serial-ROM output from ROM.<br>General purpose I/O or open-drain output. |
| **GPIO_9_ROMSI** | O<br>3.3 V<br>(VDD_33) | PD-reset | Serial-ROM input to ROM.<br>General purpose I/O or open-drain output. |
| **GPIO_10_ROMSCK** | O<br>3.3 V<br>(VDD_33) | PD-reset | Serial-ROM clock to ROM.<br>General purpose I/O or open-drain output. |
| **GPIO_22_ROMCSB** | O<br>3.3 V<br>(VDD_33) | PU-reset | BIOS-ROM chip select.<br>Used to enable the ROM for ROM read and program operations. |

## 3.9 General Purpose I/O Interface

Table 3–11 General Purpose I/O Interface

| Pin Name | Type | PD/PU | Description |
|---|---|---|---|
| 3.3-V GPIOs | | | |
| The following signals, if not used for their primary purposes, may be used as GPIO pins. | | | |
| GPIO_0 | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O and pin strap.<br>See Table 3–24 (p. 36) for pin strap definition. |

| Pin Name | Type | PD/PU | Description |
|---|---|---|---|
| GPIO_1 | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O and pin strap.<br>See Table 3–24 (p. 36) for pin strap definition. |
| GPIO_5_REG_HOT_AC_BATT | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O |
| GPIO_6_TACH | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O or fan tachometer feedback.<br>See Table 3–17 (p. 32) for the latter usage. |
| GPIO_8_ROMSO | I/O<br>3.3 V<br>(VDD_33) | PD-reset | Pin strap, general purpose I/O, or serial-ROM output.<br>See Table 3–24 (p. 36) for pin strap definition.<br>See Table 3–10 (p. 26) for serial ROM usage. |
| GPIO_9_ROMSI | I/O<br>3.3 V<br>(VDD_33) | PD-reset | Pin strap, general purpose I/O, or serial-ROM input.<br>See Table 3–24 (p. 36) for pin strap definition.<br>See Table 3–10 (p. 26) for serial ROM usage. |
| GPIO_10_ROMSCK | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O or serial-ROM clock.<br>See Table 3–10 (p. 26) for serial ROM usage. |
| GPIO_12 | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O and pin strap.<br>See Table 3–24 (p. 36) for pin strap definition. |
| GPIO_14_HPD2 | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O or hot-plug detect signal from the display device.<br>See Table 3–14 (p. 30) for the latter usage. |
| GPIO_15 | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O and pin strap.<br>See Table 3–24 (p. 36) for pin strap definition. |
| GPIO_16_8P_DETECT | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O on mobile. |
| GPIO_17_THERMAL_INT | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O or thermal interrupt.<br>See Table 3–17 (p. 32) for the latter usage. |
| GPIO_18_HPD3 | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O or hot-plug detect signal from the display device.<br>See Table 3–14 (p. 30) for the latter usage. |

| Pin Name | Type | PD/PU | Description |
|---|---|---|---|
| GPIO_20 | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O and pin strap.<br>See Table 3–24 (p. 36) for pin strap definition. |
| GPIO_21 | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O. |
| GPIO_28_FDO | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O or fan drive.<br>See Table 3–17 (p. 32) for the latter usage. |
| GPIO_29 | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O and pin strap.<br>See Table 3–24 (p. 36) for pin strap definition. |
| GPIO_30 | I/O<br>3.3 V<br>(VDD_33) | PD-reset | General purpose I/O. |
| GPIO_2 | I/O<br>3.3 V<br>(VDD_33) | PU-reset | General purpose I/O and pin strap.<br>See Table 3–24 (p. 36) for pin strap definition. |
| GPIO_11 | I/O<br>3.3 V<br>(VDD_33) | PU-reset | General purpose I/O and pin strap.<br>See Table 3–24 (p. 36) for pin strap definition. |
| GPIO_13 | I/O<br>3.3 V<br>(VDD_33) | PU-reset | General purpose I/O and pin strap.<br>See Table 3–24 (p. 36) for pin strap definition. |
| GPIO_22_ROMCSB | I/O<br>3.3 V<br>(VDD_33) | PU-reset | Pin strap, general purpose I/O, or ROM chip-select.<br>See Table 3–24 (p. 36) for pin strap definition.<br>See Table 3–10 (p. 26) for serial ROM usage. |

**Note:**

1. During the ramp-up of the VDD_33 power rail, all GPIOs are undefined and a voltage bump may appear momentarily (up to 800 mV). GPIOs should be gated/filtered using an appropriate qualifier if they are connected to external circuits that are sensitive or responsive to the voltage bump.
2. Internal PU or PD is effective after VDDC is at ready state. Before VDDC is ready, the GPIOs are of Hi-Z state.
3. All GPIOs are configured as input by default after VDDC is at ready state. GPIOs can be programmed as output by the video BIOS. For any GPIOs that are default to PD internally, but used as output and expected to drive high level at power-up, if the external circuit is sensitive and responsive to the voltage level present on the GPIO during the period before the vBIOS is loaded, a strong pull-up of 1K Ω (5%) is recommended.
4. For GPIOs that serve as pin straps, any external circuits using them must not conflict with the logic level required by the strap after power up until PCIe reset gets de-asserted.
5. See Configuration Straps (p. 35) for more information on pin strap configurations.

## 3.10 AMD SVI2 Master Interface

Table 3–12 AMD SVI2 Master Interface

| Pin Name | Type | Description |
|---|---|---|
| **GPIO_SVC** | O<br>1.8 V<br>(VDD_18) | Serial VID clock.<br>Push-pull clock output for the SVI2 data bus; driven by the GPU. Point-to-point connection to the SVI2 voltage regulator controller. |
| **GPIO_SVD** | I/O<br>1.8 V<br>(VDD_18) | Serial VID data.<br>Push-pull data output for the SVI2 data bus; driven by the GPU. Sets the voltage, power-state indicator, load-line slope, and voltage offsets for two voltage rails. Point-to-point connection to the SVI2 voltage regulator controller. |
| **GPIO_SVT** | I<br>1.8 V<br>(VDD_18) | Serial VID telemetry.<br>Push-pull data input driven by the SVI2 voltage regulator controller. Continuously streams the voltage and current telemetry information to the GPU. Also provides an indication when positive voltage transitions are complete (VOTFC). |

## 3.11 Global Swap Lock on Multiple GPUs

Global swap lock is used to synchronize the timing and surface flip for multiple display pipes on multiple GPUs.

If this feature is not required, the following signals can be used as 3.3-V GPIOs or left unconnected on the PCB.

Table 3–13 Global Swap Lock on Multiple GPUs

| Pin Name | Type | PD/ PU | Description |
|---|---|---|---|
| **GENLK_CLK** | I/O<br>3.3 V<br>(VDD_33) | PD-reset | Reference-clock input for the display PLLs (including the DCPLL and pixel PLLs) received from the framelock/genlock interface.<br>**Note:** Can be unconnected if not used. |
| **GENLK_VSYNC** | I/O<br>3.3 V<br>(VDD_33) | PD-reset | Frame-timing indicator.<br>Output to the framelock/genlock interface. |
| **SWAPLOCKA** | Open drain<br>3.3 V | - | (Optional) Used in a multiple GPU design with multiple display outputs to allow all displays in group A to update at the same time and have synchronous left/right stereo timing.<br>In a multiple GPU design where displays are connected to more than one GPU, connect SWAPLOCKA from all GPUs together with an external 10-kΩ pull-up resistor.<br>GPU genlock is needed, either via a genlock system or by feeding all GPUs with the same reference clock.<br>Connecting SWAPLOCKB is preferred but not required. |
| **SWAPLOCKB** | Open drain<br>3.3 V | - | (Optional) Used in a multiple GPU design with multiple display outputs to allow all displays in group B to update at the same time and have synchronous left/right stereo timing.<br>In a multiple GPU design where displays are connected to more than one GPU, connect SWAPLOCKB from all GPUs together with an external 10-kΩ pull-up resistor.<br>GPU genlock is needed, either via a genlock system or by feeding all GPUs with the same reference clock. |

## 3.12 Display Identification Interface

Table 3–14 Display Identification Interface

| Pin Name | Type | Description |
|---|---|---|
| **DDC1CLK/ DDC1DATA or AUX1P/N** | I/O 3.3 V (VDD_33) | DDC1CLK/DDC1DATA and AUX1P/N signal pairs are mutually exclusive.<br>A design can use either the DDC1 or AUX1 pair on one display connector. Alternatively, DDC1DATA can be connected to AUX1N, and DDC1CLK can be connected to AUX1P on one DisplayPort connector (see reference schematics).<br>**Note:** Can be unconnected if not used.<br>For the DDC functionality (DDC data and clock signals ($I^2C$ master)):<br>• These pins can be used to support internal high-bandwidth digital content protection (HDCP).<br>• Outputs are open drain and NOT 5-V tolerant. External pull-up resistors to 3.3 V are required.<br>For the AUX functionality (auxiliary differential signals for DisplayPort):<br>• A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector, and<br>• A source detection pull-down resistor (100-kΩ 5% tolerance) is required on the AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on the AUXN signal. |
| **DDC2CLK/ DDC2DATA or AUX2P/N** | I/O 3.3 V (VDD_33) | DDC2CLK/DDC2DATA and AUX2P/N signal pairs are mutually exclusive.<br>A design can use either the DDC2 or AUX2 pair on one display connector.<br>Alternatively, DDC2DATA can be connected to AUX2N, and DDC2CLK can be connected to AUX2P on one DisplayPort connector (see reference schematics).<br>**Note:** Can be unconnected if not used.<br>For the DDC functionality (DDC data and clock signals ($I^2C$ master)):<br>• These pins can be used to support internal HDCP.<br>• Outputs are open drain and NOT 5-V tolerant. External pull-up resistors to 3.3 V are required.<br>For the AUX functionality (auxiliary differential signals for DisplayPort):<br>• A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector, and<br>• A source detection pull-down resistor (100-kΩ 5% tolerance) is required on the AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on the AUXN signal. |
| **DDCAUX[6:3]N DDCAUX[6:3]P** | I/O 3.3 V (VDD_33) | DDC data/clock for DVI/HDMI or auxiliary differential signals for DisplayPort.<br>These pins can be used to support internal HDCP.<br>**Note:** Can be unconnected if not used.<br>For the AUX functionality:<br>• A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector, and<br>• A source detection pull-down resistor (100-kΩ 5% tolerance) is required on each AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on each AUXN signal.<br>For the $I^2C$ functionality: |

| Pin Name | Type | Description |
|---|---|---|
| | | Outputs are open drain and NOT 5-V tolerant. External pull-up resistors to 3.3 V are required. |
| **HPD1**<br>**GPIO_14_HPD2**<br>**GPIO_18_HPD3**<br>**GENERICE_HPD4**<br>**GENERICF_HPD5**<br>**GENERICG_HPD6** | I<br>3.3 V<br>(VDD_33) | Hot-plug detect signal from the display device to the GPU. |

## 3.13 JTAG Interface

In order to debug issues, AMD requires access to the JTAG interface.

Test points can be used on the JTAG signals to minimize the PCB space needed.

Table 3–15 JTAG Interface

| Pin Name | Type | PD/ PU | Description |
|---|---|---|---|
| **TESTEN** | I<br>3.3 V<br>(VDD_33) | - | Reserved signal.<br>This pin must be tied to ground through a 1-kΩ to 10-kΩ resistor for normal GPU operation. |
| **JTAG_TRSTB** | I/O<br>3.3 V<br>(VDD_33) | PU-reset | TRSTB (test reset).<br>This pin can be left floating, or tied to 3.3 V through a 10-kΩ resistor for normal GPU operation.<br>Must be accessible on all PCBs through a test point or resistor pad. |
| **JTAG_TDI** | I/O<br>3.3 V<br>(VDD_33) | PU-reset | TDI (test data input).<br>This pin can be left floating, or tied to 3.3 V through a 10-kΩ resistor for normal GPU operation.<br>Must be accessible on all PCBs through a test point or resistor pad. |
| **JTAG_TCK** | I/O<br>3.3 V<br>(VDD_33) | PD-reset | TCK (test clock).<br>This pin can be left floating, or tied to ground through a 10-kΩ resistor for normal GPU operation.<br>Must be accessible on all PCBs through a test point or resistor pad. |
| **JTAG_TMS** | I/O<br>3.3 V<br>(VDD_33) | PU-reset | TMS (test mode select).<br>This pin can be left floating, or tied to 3.3 V through a 10-kΩ resistor for normal GPU operation.<br>Must be accessible on all PCBs through a test point or resistor pad. |
| **JTAG_TDO** | I/O<br>3.3 V<br>(VDD_33) | - | TDO (test data output).<br>This pin can be left floating, or unconnected if not used.<br>Must be accessible on all PCBs through a test point or resistor pad. |

## 3.14 Debug Port

Table 3–16 Debug Port

| Pin Name | Functional Name |
|---|---|
| **SMBDAT** | Serial debug port data |
| **SMBCLK** | Serial debug port clock |
| **DBGDATA[15:0]** | Debug bus output data |
| **TEST6** | Connect to GND through a zero-Ω resistor |
| **BP_0** | Provide a pull-up resistor to 1.8 V on the PCB |
| **BP_1** | Provide a pull-up resistor to 1.8 V on the PCB |
| **ANALOGIO** | Provide access on the PCB through a test pad |
| **GATE** | Provide access on the PCB through a test pad |
| **DRAIN** | Provide access on the PCB through a test pad |
| **PLLCHARZ_H** | Provide access on the PCB through a test pad |
| **PLLCHARZ_L** | Provide access on the PCB through a test pad |

## 3.15 Thermal Information and Management Interface

Table 3–17 Thermal Interface Signals

| Pin Name | Type | PU/PD | Description |
|---|---|---|---|
| **DPLUS** | Anode | - | Thermal diode plus side (anode), used by the external temperature controller to obtain GPU die temperature.<br>**Note:** Can be unconnected if not used. |
| **DMINUS** | Cathode | - | Thermal diode minus side (cathode), used by the external temperature controller to obtain the GPU die temperature.<br>**Note:** Can be unconnected if not used. |
| **GPIO_6_TACH** | I<br>3.3 V<br>(VDD_33) | PD-reset | Fan tachometer feedback. |
| **GPIO_17_THERMAL_INT** | Bi-dir<br>3.3 V<br>(VDD_33) | PD-reset | Thermal monitor interrupt.<br>An input from an external temperature sensor (ALERTb). |

| Pin Name | Type | PU/PD | Description |
|---|---|---|---|
| **GPIO_19_CTF**[1] | O<br>3.3 V<br>(VDD_33) | PD-reset | Critical temperature fault (CTF) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the GPU from damage by removing power.<br>If GPIO_19_CTF is expected to be latched at "high" level upon occurrence of the CTF event, 1.8 V and 3.3 V to the GPU must remain.<br>The CTF setpoint is 96℃ by default, and is programmed during GPU initialization. |
| **GPIO_28_FDO** | O | PD-reset | Fan drive output (output to control fan).<br>In PWM mode, the PWM frequency is 15 kHz to 50 kHz. |
| **TEMPIN0** | I | - | A provision to connect to the anode of an external thermal diode for the GPU to read the temperature from a spot of interest on the board or platform.<br>For experimental purposes and should be left unconnected. |
| **TEMPINRETURN** | I | - | A provision to connect to the cathode of an external thermal diode for the GPU to read the temperature from a spot of interest on the board or platform.<br>For experimental purposes and should be left unconnected. |

**Note:**
1. **Like other GPIOs, during the ramp-up of the VDD_33 power rail, GPIO_19_CTF is undefined and a voltage bump may appear momentarily (up to 800 mV). It should be gated/filtered using an appropriate qualifier if it is connected to a external circuit that is sensitive or responsive to the voltage bump.**

## 3.16 SMBus Interface

Table 3–18 SMBus Interface

| Pin Name | Type | Description |
|---|---|---|
| **SMBDAT** | Bi-dir<br>3.3 V<br>(VDD_33) | SMBus data.<br>Connected to the SMBDAT line of the SMBus master with an external pull-up resistor to 3.3 V.<br>Supports the SMBus 2.0 protocol.<br>The SMBus slave address can be set to either 0×40 or 0×41 through pin strap on GPIO_1. For more details, see Table 3–24 (p. 36). The GPU also supports ARP. |
| **SMBCLK** | Bi-dir<br>3.3 V<br>(VDD_33) | SMBus clock.<br>Connected to the line of the SMBus master with an external pull-up resistor to 3.3 V.<br>Supports the SMBus 2.0 protocol.<br>The SMBus slave address can be set to either 0×40 or 0×41 through pin strap on GPIO_1. For more details, see Table 3–24 (p. 36). The GPU also supports ARP. |

## 3.17 PLL Interface

Table 3–19 PLL Interface

| Pin Name | Type | Description |
|---|---|---|
| **XTALIN** | A-I<br>1.8 V | An external 100-MHz non-spread 1.8-V oscillator is required to connect to XTALIN to provide the reference clock.<br>Oscillator characteristics:<br>• Frequency: 100 MHz.<br>• Voltage swing: 1.8 V.<br>• $V_{IH}$ = 1.45 V (min)<br>• $V_{IL}$ = 0.45 V (max)<br>• Accuracy: ± 10 ppm at room temperature, (± 30 ppm overall (including temperature drift)).<br>• Duty cycle (worst case): 45-55 (max).<br>• Jitter:<br>200 ps (max) cycle-to-cycle jitter.<br>300 ps (max) long-term jitter (10,000 cycles after the triggered edge). |
| **XTALOUT** | A-O<br>1.8 V | PLL Reference Clock<br>Provides a provision to have a parallel-resonant crystal connected between XTALIN and XTALOUT as a reference clock to the GPU. Backup plan.<br>Crystal characteristics:<br>• ESR: <80Ω.<br>• Combined frequency tolerance and stability: ±30 ppm max.<br>A 1-MΩ resistor must be connected between XTALIN and XTALOUT when a crystal is used.<br>Capacitive loading from the package and PCB trace should be subtracted from the C1 and C2 capacitor values.<br>**Note:** External oscillator must connect to XTALIN only. (An oscillator cannot be connected to XTALOUT.) |

Table 3–20 Recommended Clock-input Configurations

| Memory Type | Description |
|---|---|
| **GDDR5** | 100-MHz non-spread (1.8 V) oscillator connected to XTALIN. |

## 3.18 AMD PowerXpress™ Interface

Table 3–21 AMD PowerXpress™ Interface

| Pin Name | Type | PD/ PU | Description |
|---|---|---|---|
| **PX_EN** | O | PD | On/off regulator control signal for AMD ZeroCore Power feature (BACO mode).<br>High (3.3 V) switches the regulators off (enter BACO mode).<br>Low (0 V) switches the regulators on. (Default)<br>PX_EN is tri-state before internal TEST_PG is asserted and PERSTb is de-asserted.<br>Can be left unconnected if not used. |

## 3.19 Power and Ground Descriptions and Operating Conditions

**Note:**

- All power and ground pins must always be connected.

Table 3–22 Power and Ground Descriptions and Operating Conditions

| Pin Name | Value | Description |
|---|---|---|
| **Main Power and Ground Pins** | | |
| **VDDC** | XTX: 0.750 V to 1.200 V<br>XL: 0.750 V to 1.150 V | Dedicated core power, provides power to the internal logic.<br>Refer to Electrical Design Power (p. 51) for the SVI2 and other requirements on VDDC.<br>The voltage quoted is the set voltage through SVI2. |
| **VDDCI** | XTX: 0.800 V / 0.850 V / 0.950 V<br>XL: 0.800 V / 0.850 V / 0.900 V | Isolated (clean) core power for the l/O logic.<br>Particular attention should be paid to minimize AC ripple on VDDCI. |
| **FB_VDDC** | — | Provides VDDC feedback path to the regulator.<br>If unused, connect to a test point or leave not connected. |
| **FB_VDDCI** | — | Provides VDDCI feedback path to the regulator.<br>If unused, connect to a test point or leave not connected. |
| **FB_VSS** | — | Provides ground feedback path to the regulator.<br>If unused, connect to a test point or leave not connected. |
| **VDD_08** | 0.9 V | Digital power supply for PLL, PCIe, and display PHYs. |
| **VDD_18** | 1.8 V | 1.8-V I/O power for PLL, PCIe, and display PHYs. |
| **TSVDD** | 1.8 V | On-die thermal sensor power. |
| **VMEMIO (memory)** | 1.5 V or 1.55 V<br>See memory specifications. | I/O power for the memory interface. |
| **VDD_33** | 3.3 V | I/O power for 3.3-V pins, such as GPIOs. |
| **VSS** | Gnd | Ground. |

Table 3–23 Other Signals

| Pin Name | Type | Description |
|---|---|---|
| **TEST_PG**<br>**TEST_PG_BACO** | I | TEST_PG and TEST_PG_BACO should be accessible for test purposes and must be pulled up to the 1.8-V power rail for normal operation. |
| **TS_A** | I | Reserved. Do not connect on the PCB. |

## 3.20 Configuration Straps

### 3.20.1 GPIO Pin Straps

"Polaris 20" uses GPIO pin straps (i.e., one GPIO for one strap).

Some of the straps are on 3.3-V GPIOs while others are on 1.8-V GPIOs.

Each strap pin has either an internal pull-down resistor which provides a default value of 0, or an internal pull-up resistor which provides a default value of 1, at power up. For each strap that defaults to 0 by the GPU, provide a pull-up resistor option (to 3.3-V or 1.8-V depending on the GPIO type) on the PCB. For each strap that defaults to 1 by the GPU, provide a pull-down resistor option to GND on the PCB.

To change the straps from the default values, use pull-up or pull-down resistors of **5.1K Ω (5%)** on the PCB.

Any external circuit using these pins must not conflict with the logic level required by the strap after power up until PCIe reset gets de-asserted.

Table 3–24 Pin Straps

| Strap Name | Pin Name | Description | GPU Default | Recommended Settings[1] |
|---|---|---|---|---|
| BIF_VGA_DIS | GPIO_29 | Determine whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space).<br>0: VGA Controller capacity enabled.<br>1: The device will not be recognized as the system's VGA controller (for headless designs). | 0<br>(Internal pull-down) | Design dependent<br>Provide a pull-up resistor option to VDD_33. |
| TX_DEEMPH_EN | GPIO_20 | PCI Express transmitter de-emphasis enable<br>0: Tx de-emphasis disabled.<br>1: Tx de-emphasis enabled. | 0<br>(Internal pull-down) | 1<br>Through pull-up resistor to VDD_33. |
| TX_HALF_SWING | GPIO_0 | Controls the transmitter full/half swing mode.<br>0: The transmitter full-swing is enabled.<br>1: The transmitter half-swing is enabled. | 0<br>(Internal pull-down) | 0<br>Provide a pull-up resistor option to VDD_33. |
| ROM_CONFIG[2:0] | GPIO_13<br>GPIO_12<br>GPIO_11 | a) If BIOS_ROM_EN = 1, then ROM_CONFIG[2:0] defines the ROM type. See ROM Configurations (p. 38) for details.<br>b) If BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size. See ROM Configurations (p. 38) for details. | 101<br>(Internal pull-up/ pull-down) | Design dependent.<br>Provide a pull-down resistor option to GND on the PCB for GPIO_13.<br>Provide a pull-up resistor option to VDD_33 on the PCB for GPIO_12.<br>Provide a pull-down resistor option to GND on the PCB for GPIO_11. |

| Strap Name | Pin Name | Description | GPU Default | Recommended Settings[1] |
|---|---|---|---|---|
| BIOS_ROM_EN | GPIO_22_ROMCSB | Enable external BIOS ROM device.<br>0: Disable external BIOS ROM device.<br>1: Enable external BIOS ROM device.<br>**Note:** When an external BIOS ROM device is used, GPIO_22_ROMCSB also connects to the ROM device's chip select (active low). | 1<br>(Internal pull-up) | Design dependent.<br>Provide a pull-down resistor option to GND on the PCB. |
| Special Usage [1]<br>Special Usage [0] | HSYNC<br>VSYNC | Special usage | 0<br>(Internal pull-down) | Design dependent.<br>Refer to application note order #55739 on the special usage.<br>Provide a pull-up resistor option to VDD_33 on the PCB for each pin. |
| AUD_PORT_CONN [2:0] | DBGDATA_2<br>DBGDATA_1<br>DBGDATA_0 | Determine the maximum number of digital display audio endpoints that will be presented to the OS and user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the GPU itself, the number and type of connectors on the board (DP/HDMI), and the number of sinks for each DP connector (the DP MST link policy of the video driver). Unused endpoints should be disabled.<br>111: No usable endpoints<br>110: One usable endpoint<br>101: Two usable endpoints<br>100: Three usable endpoints<br>011: Four usable endpoints<br>010: Five usable endpoints<br>001: Six usable endpoints<br>000: All endpoints are usable | 0<br>(Internal pull-down) | Design dependent, see description.<br>Provide a pull-up resistor option **to VDD_18** on the PCB for each pin. |
| BOARD_CONFIG [2:0] | DBGDATA_5<br>DBGDATA_4<br>DBGDATA_3 | Provides an option to specify certain board-level specifics to the VBIOS or driver. | 0<br>(Internal pull-down) | Design dependent.<br>Provide a pull-up resistor option **to VDD_18** on the PCB for each pin. |

| Strap Name | Pin Name | Description | GPU Default | Recommended Settings[1] |
|---|---|---|---|---|
| SMBUS_ADDR | GPIO_1 | Provide a strap option to change the SMBUS slave address of the GPU.<br>0: 0×40<br>1: 0×41 | 0<br>(Internal pull-down) | Design dependent.<br>Provide a pull-up resistor option to VDD_33 on the PCB for the pin.<br>Strap on the PCB the address **to 0×41** if it does not cause address conflict on the platform. |
| BIF_GEN3_EN_A | GPIO_2 | PCIe Gen3 capability.<br>1: PCIe Gen3 is supported.<br>0: PCIe Gen3 is not supported. | 1<br>(Internal pull-up) | Design dependent.<br>Provide a pull-down resistor option to GND on the PCB. |
| BIF_CLK_PM_EN | GPIO_8_ROMSO | Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB).<br>0: The CLKREQB power management capability is disabled.<br>1: The CLKREQB power management capability is enabled. | 0<br>(Internal pull-down) | Design dependent.<br>Provide a pull-up resistor option to VDD_33 on the PCB. |
| Reserved | GPIO_15 | Reserved | 0<br>(Internal pull-down) | Must default to 0 for production.<br>Provide a pull-up resistor option to VDD_33 on the PCB. |
| Reserved | GPIO_9_ROMSI | Reserved | 0<br>(Internal pull-down) | Must default to 0 for production.<br>Provide a pull-up resistor option to VDD_33 on the PCB. |

**Note:**
1. To change the straps from the default values, use pull-up or pull-down resistors of 5.1K Ω (5%) on the PCB.

### 3.20.2 ROM Configurations

For designs that have a dedicated ROM device for the GPU video BIOS:

- Use the GPU default strap on GPIO_22_ROMCSB (i.e., 1).
- Use the GPU default straps on GPIO_13, GPIO_12, and GPIO_11 (i.e., 101).

### 3.20.3 Primary Memory Aperture Size

The following table shows the primary memory aperture sizes requested at PCI configuration.

Table 3–25 Primary Memory Aperture Sizes Requested at PCI Configuration

| Size of the Primary Memory Apertures | ROM_CONFIG[2:0] |
|---|---|
| **128 MB** | 000 |
| **256 MB** | 001 |
| **64 MB** | 010 |
| **8 GB** | 011 |
| **16 GB** | 100 |
| **1 GB** | 101 |
| **2 GB** | 110 |
| **4 GB** | 111 |

**Note:** The memory aperture size should be the same as the frame buffer size for 64 MB, 128 MB, and 256 MB. For a frame buffer size larger than 256 MB, memory aperture size should be set to 256 MB.
For designs requiring larger than 256 MB aperture size, consult with AMD.

### 3.20.4 ROM Straps for Add-in Card Design

If a dedicated ROM is used for the video BIOS (see ROM_CONFIG[2:0] and BIOS_ROM_EN in GPIO Pin Straps (p. 35)), then after PERSTB goes inactive (high), the ROM is read at the BIOS addresses and default BIOS settings in the following table.

The ROM straps are ORed with the corresponding pin straps.

Table 3–26 ROM Straps

| Strap Name | Description | Default BIOS Setting |
|---|---|---|
| **F0_64BAR_DIS_A** | Enable 64-bit BAR for function 0.<br>Affects bit 2 of BLOCK_MEM_TYPE for each BAR register in the PCI configuration space. | 1 |
| **SUBSYS_VEN_ID** | Subsystem vendor ID (SSVID) in the PCI configuration space.<br>If a VBIOS ROM is not used, then the SBIOS is permitted to overwrite this register for each PCI function on the device before the enumeration cycle is initiated, otherwise the default value is used. | 0x1002 |
| **F0_SUBSYS_ID** | Subsystem ID (SSID) for the PCI configuration space for function 0.<br>If enabled, SSID for the secondary display function (F1) is set to the same value as the primary display function (F0) with bit 0 inverted. | |
| **F0_BAR_EN** | 0 = Disable resizable BAR feature.<br>1 = Enable resizable BAR feature. | 1 |

| Strap Name | Description | Default BIOS Setting |
|---|---|---|
| **MEM_AP_SIZE[2:0]** | Size of the primary memory apertures claimed in the PCI configuration space:<br>If F0_BAR_EN = 1 (i.e., resizable BAR enabled):<br>• 000: 256 MB to 1 GB<br>• 001: 256 MB to 4 GB<br>• 010: 256 MB to 8 GB<br>• 011: 256 MB to 16 GB<br>• 100: 128 MB to 1 GB<br>• 101: 128 MB to 2 GB<br>• 110: 128 MB to 8 GB<br>• 111: 128 MB to 16 GB<br>If F0_BAR_EN = 0 (i.e., resizable BAR disabled):<br>• 000: 128 MB<br>• 001: 256 MB<br>• 010: 64 MB<br>• 011: 8 GB<br>• 100: 16 GB<br>• 101: 1 GB<br>• 110: 2 GB<br>• 111: 4 GB<br>When F0_BAR_EN = 0, the aperture size should be set to the same size as the frame buffer size for 64 MB, 128 MB, and 256 MB. For a frame bugger size larger than 256 MB, the aperture size should be set to 256 MB. For designs requiring larger than 256 MB aperture size, contact AMD. | Depends on the board configuration, see the description. |
| **AUDIO_EN** | Multi-function device select.<br>Affects bit seven of the header register in the PCI configuration space.<br>PCI configuration setting:<br>0 = Audio function not present.<br>1 = Audio function present.<br>Boards with a ROM will require both the ROM and the specific pin straps to be set in order to enable the audio function. Boards without a ROM will only require the pin straps to be set in order to enable the audio function. | Depends on the board configuration, see the description. |
| **VGA_DIS** | VGA disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in PCI configuration space):<br>0 = VGA controller capacity enabled.<br>1 = The device will not be recognized as the system’s VGA controller. | 0 |
| **DEBUG_ACCESS** | The debug access sets the debug MUX settings from the ROM in order to bring out internal signals for observation when registers are inaccessible through the host interface. | 0 |

# 4

# Timing Specifications

This chapter describes bus and memory timing specifications of "Polaris 20".

To link to a topic of interest, use the following list of linked cross-references:



## 4.1 DRAM Timing

### 4.1.1 Programming Timing Values

The following tables show the memory-timing parameters that can be programmed through the registers MC_SEQ_RAS_TIMING, MC_SEQ_CAS_TIMING, MC_SEQ_MISC_TIMING, and MC_SEQ_MISC_TIMING2.

The MC_SEQ_RAS_TIMING register allows the programming of the row operation timing parameters.

Table 4–1 MC_SEQ_RAS_TIMING Parameters

| Field | Bits | Description |
|---|---|---|
| **TRCDW** | 4:0 | ACTIVE to WRITE (in hclk) - 1. |
| **TRCDWA** | 9:5 | ACTIVE to WRITE with AUTO PRECHARGE (in hclk) - 1. |
| **TRCDR** | 14:10 | ACTIVE to READ (in hclk) - 1. |
| **TRCDRA** | 19:15 | ACTIVE to READ with AUTO PRECHARGE (in hclk) - 1. |
| **TRRD** | 23:20 | ACTIVE bank a to ACTIVE bank b (in hclk) - 1. |
| **TRC** | 30:24 | ACTIVE to ACTIVE (same bank)/AUTO REFRESH period (in hclk). |
| **TRCDW** | 31 | Most significant bit of TRCDW. |

The MC_SEQ_CAS_TIMING register allows the programming of the column operation timing parameters.

Table 4–2 MC_SEQ_CAS_TIMING Parameters

| Field | Bits | Description |
|---|---|---|
| **TNOPW** | 1:0 | Extra write pitch between bursts for debug purposes (in hclk). |
| **TNOPR** | 3:2 | Extra read pitch between bursts for debug purposes (in hclk). |
| **TR2W** | 8:4 | READ to WRITE turnaround time (in hclk) - 1. |

| Field | Bits | Description |
|---|---|---|
| **TCCDL** | 11:9 | Col to Col access delay – 1 (within the same bank group). GDDR5 only. |
| **TR2R** | 15:12 | READ to READ different rank (in hclk) - 1. |
| **TW2R** | 20:16 | WRITE to READ turn around time (in hclk) - 1. |
| **TCL** | 28:24 | CAS to read data return latency - 2 (0 to 20). |

The MC_SEQ_MISC_TIMING and MC_SEQ_MISC_TIMING2 registers allow programming of miscellaneous timing parameters.

Table 4–3 MC_SEQ_MISC_TIMING Parameters

| Field | Bits | Description |
|---|---|---|
| **TRP_WRA** | 5:0 | AUTO PRECHARGE to ACTIVE for WRITE (in hclk) - 1. |
| **TRP_RDA** | 13:8 | AUTO PRECHARGE to ACTIVE for READ (in hclk) - 1. |
| **TRP** | 19:16 | PRECHARGE command period (in hclk) - 1. |
| **TRFC** | 28:20 | AUTO REFRESH command period (in hclk) -1. |
| **TRCDWA** | 29 | Most significant bit of TRCDWA described in Table 4–1 (p. 41). |
| **TRCDR** | 30 | Most significant bit of TRCDR described in Table 4–1 (p. 41). |
| **TRCDRA** | 31 | Most significant bit of TRCDRA described in Table 4–1 (p. 41). |

Table 4–4 MC_SEQ_MISC_TIMING2 Parameters

| Field | Bits | Description |
|---|---|---|
| **PA2RDATA** | 2:0 | READ PREAMBLE (for GDDR4 only) (in hclk). |
| **PA2WDATA** | 6:4 | WRITE PREAMBLE (for GDDR4 only) (in hclk). |
| **FAW** | 12:8 | FOUR ACTIVE WINDOW (in mclk) - 5. |
| **TREDC** | 15:13 | READ EDC LATENCY in addition to READ DATA LATENCY (in hclk). |
| **TWEDC** | 20:16 | WRITE EDC LATENCY (in hclk)– 8. |
| **T32AW** | 24:21 | 32 ACTIVE TIMING WINDOW (in mclk). |
| **TWDATATR** | 24:21 | DQ→WCMD timing for write training. |

Table 4–5 Mapping DRAM Parameters to Programmed Values (GDDR5)

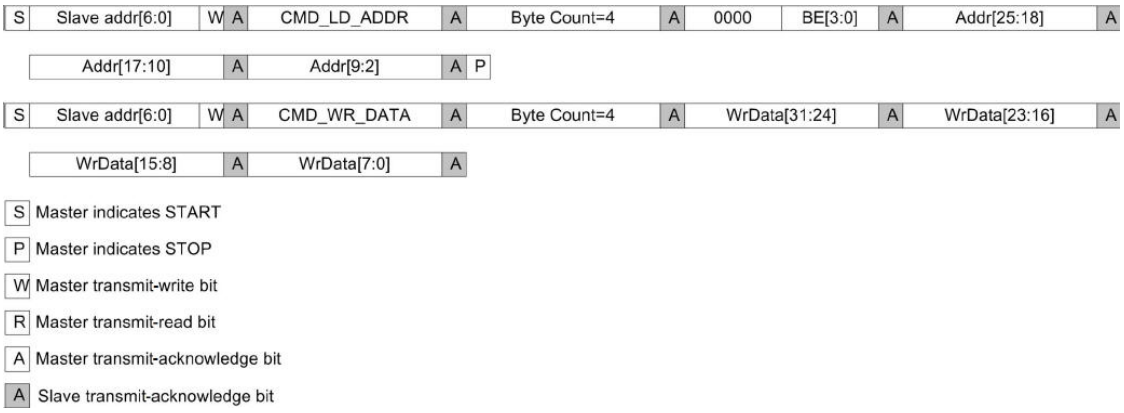
| Parameter | Programmed Value | Unit |
|---|---|---|
| **Burst Length** | 8 | edge |
| **YCLK** | 4000 | MHz |
| **HCLK (memory clock)** | 1000 | MHz |
| **MCLK** | 500 | MHz |
| **HCLK Period** | 1.0 | ns |

## 4.2 SMBus Timing

### 4.2.1 SMBus Write Cycle

The following figure shows an SRBM (system register bus manager) write cycle on the SMBus interface.

Figure 4–1 SMBus Write Cycle




A typical SMBus write cycle consists of the following steps:

1. Issuing a Load Address Command to the SMB_ADDR register:
   - **a.** The SMBus master issues a START bit to the slave.
   - **b.** The SMBus master issues 7-bit slave address to the slave.
   - **c.** The SMBus master issues a write bit to the slave.
   - **d.** The SMBus slave acknowledges the master.
   - **e.** The SMBus master issues an 8-bit CMD_LD_ADDR command to the slave.
   - **f.** The SMBus slave acknowledges the master.
   - **g.** The SMBus master sends a byte count (always 4).
   - **h.** The SMBus slave acknowledges the master.
   - **i.** The SMBus master issues a 4-bit byte enable with a 4-bit zero padding.
   - **j.** The SMBus slave acknowledges the master.
   - **k.** The SMBus master sends SMB_ADDR[25:18] to the slave.
   - **l.** The SMBus slave acknowledges the master.
   - **m.** The SMBus master sends SMB_ADDR[17:10] to the slave.
   - **n.** The SMBus slave acknowledges the master.
   - **o.** The SMBus master sends SMB_ADDR[9:2] to the slave.
   - **p.** The SMBus slave acknowledges the master.
   - **q.** The SMBus master sends a STOP bit to the slave.
2. Issuing a Write Data Command to the SMB_WR_DATA register:
   - **a.** The SMBus master issues a START bit to the slave.

**b.** The SMBus master issues a 7-bit slave address to the slave.

**c.** The SMBus master issues a write bit to the slave.

**d.** The SMBus slave acknowledges the master.

**e.** The SMBus master issues an 8-bit CMD_WR_DATA command to the slave.

**f.** The SMBus slave acknowledges the master.

**g.** The SMBus master sends a byte count (always 4).

**h.** The SMBus slave acknowledges the master.

**i.** The SMBus master sends SMB_WR_DATA[31:24] to the slave.

**j.** The SMBus slave acknowledges the master.

**k.** The SMBus master sends SMB_WR_DATA[23:16] to the slave.

**l.** The SMBus slave acknowledges the master.

**m.** The SMBus master sends SMB_WR_DATA[15:8] to the slave.

**n.** The SMBus slave acknowledges the master.

**o.** The SMBus master sends SMB_WR_DATA[7:0] to the slave.

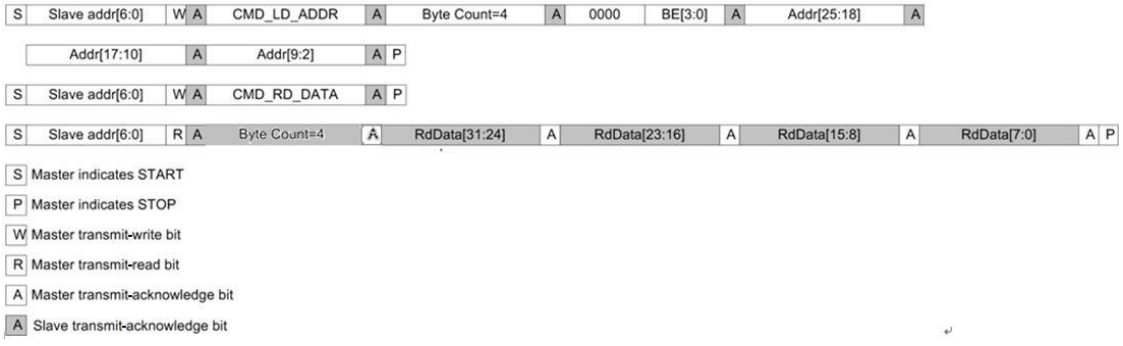
**p.** The SMBus slave acknowledges the master.

**q.** The SMBus master sends a STOP bit to the slave.

### 4.2.2 SMBus Read Cycle

The following figure shows an SRBM read cycle on the SMBus interface.

Figure 4–2 SMBus Read Cycle




A typical SMBus read cycle consists of the following steps:

**1.** Issuing a Load Address Command to the SMB_ADDR register:

**a.** The SMBus master issues a START bit to the slave.

**b.** The SMBus master issues a 7-bit slave address to the slave.

**c.** The SMBus master issues a write bit to the slave.

**d.** The SMBus slave acknowledges the master.

**e.** The SMBus master issues an 8-bit CMD_LD_ADDR command to the slave.

**f.** The SMBus slave acknowledges the master.

**g.** The SMBus master sends a byte count (always 4).

**h.** The SMBus slave acknowledges the master.

**i.** The SMBus master issues a 4-bit byte enable with a 4-bit zero padding. These bits should have no effect on the reads.

**j.** The SMBus slave acknowledges the master.

**k.** The SMBus master sends SMB_ADDR[25:18] to the slave.

**l.** The SMBus slave acknowledges the master.

**m.** The SMBus master sends SMB_ADDR[17:10] to the slave.

**n.** The SMBus slave acknowledges the master.

**o.** The SMBus master sends SMB_ADDR[9:2] to the slave.

**p.** The SMBus slave acknowledges the master.

**q.** The SMBus master sends a STOP bit to the slave.

**2.** Issuing a Read Data Command to the slave.

**a.** The SMBus master issues a START bit to the slave.

**b.** The SMBus master issues a 7-bit slave address to the slave.

**c.** The SMBus master issues a write bit to the slave.

**d.** The SMBus slave acknowledges the master.

**e.** The SMBus master issues an 8-bit CMD_RD_DATA command to the slave.

**f.** The SMBus slave acknowledges the master.

**g.** The SMBus master terminates the transaction with a STOP.

**3.** Issuing an SMBus read to the slave:

**a.** The SMBus master issues a START bit to the slave.

**b.** The SMBus master issues an 7-bit slave address to the slave.

**c.** The SMBus master issues a read bit to the slave.

**d.** The SMBus slave acknowledges the master.

**e.** The SMBus slave sends a byte count (always 4).

**f.** The SMBus master acknowledges the slave.

**g.** The SMBus slave sends SMB_RD_DATA[31:24] to the master.

**h.** The SMBus master acknowledges the slave.

**i.** The SMBus slave sends SMB_RD_DATA[23:16] to the master.

**j.** The SMBus master acknowledges the slave.

**k.** The SMBus slave sends SMB_RD_DATA[15:8] to the master.

**l.** The SMBus master acknowledges the slave.

**m.** The SMBus slave sends SMB_RD_DATA[7:0] to the master.

**n.** The SMBus master acknowledges the slave.

**o.** The SMBus master terminates the transaction with a STOP.

### 4.2.3 SMBus Read Thermal Sensor

Since SMU has moved thermal value register into indirect space, so if we want to access it, we need 2 indirect steps.

Programming sequence is shown below:

1. SMB Issue a Load Address Command(cmd1) to the SMC_IND_INDEX_7 address. (Tell SMBus slave the index address.)

   82 01 04 0f 00 00 8E

2. SMB Issue a Write Data Command(cmd2) to the thermal register real address. (Tell SMBus slave to write the real address to #1's index.)

   82 02 04 c0 30 00 14

3. SMB Issue a Load Address Command(cmd1) to the SMC_IND_DATA_7 (Tell SMBus slave the index pair's data address.)

   82 01 04 0f 00 00 8F

4. SMB Issue a Read Data Command(cmd3) (Tell SMBus slave to read out thermal value.)

   82 03 83 <value read back>

5. Repeat step 4.

## 4.3 Initialization Sequence and Timing

### 4.3.1 Initialization Sequence and Timing

1. Chip reset (PERSTB) is asserted, and PCIE_REFCLK starts running.
2. All GPIOs go to a tristate (input) mode at RESETB. Some GPIOs have internal pull-down (PD) or pull-up (PU) resistors—see descriptions of pin-based straps.
3. External pin straps are driving their values onto the GPU pins.
4. Chip reset (PERSTB) is deasserted.
5. External pin-strap values are latched internally.
6. In parallel:
   a. eFuse state machine begins to read "eFuse straps."
   b. If a ROM exists (and is programmed), a request is sent to the ROM controller to read the "ROM straps."

7. eFuse and ROM straps are "forwarded" to PHY.
8. In parallel:
    a. If GPU memory repair is required, then memory repair starts.
    b. eFuse and ROM straps are "forwarded" to other blocks in the GPU.
9. Wait for memory repair to complete. De-assert a hard reset to all the blocks including BIF. Enable PCIe® PHY impedance calibration. After polling for the PHY impedance calibration, distribute the remaining fuses and poll for BIF to complete its reset sequence.
10. The GPU begins link training according to the PCIe specification.

    After link training and the reset sequence are complete, the system is ready for the first transaction, such as a configuration space request.

The following figure and table provide an outline of the "Polaris 20" reset sequence.

Figure 4–3 Reset Sequence

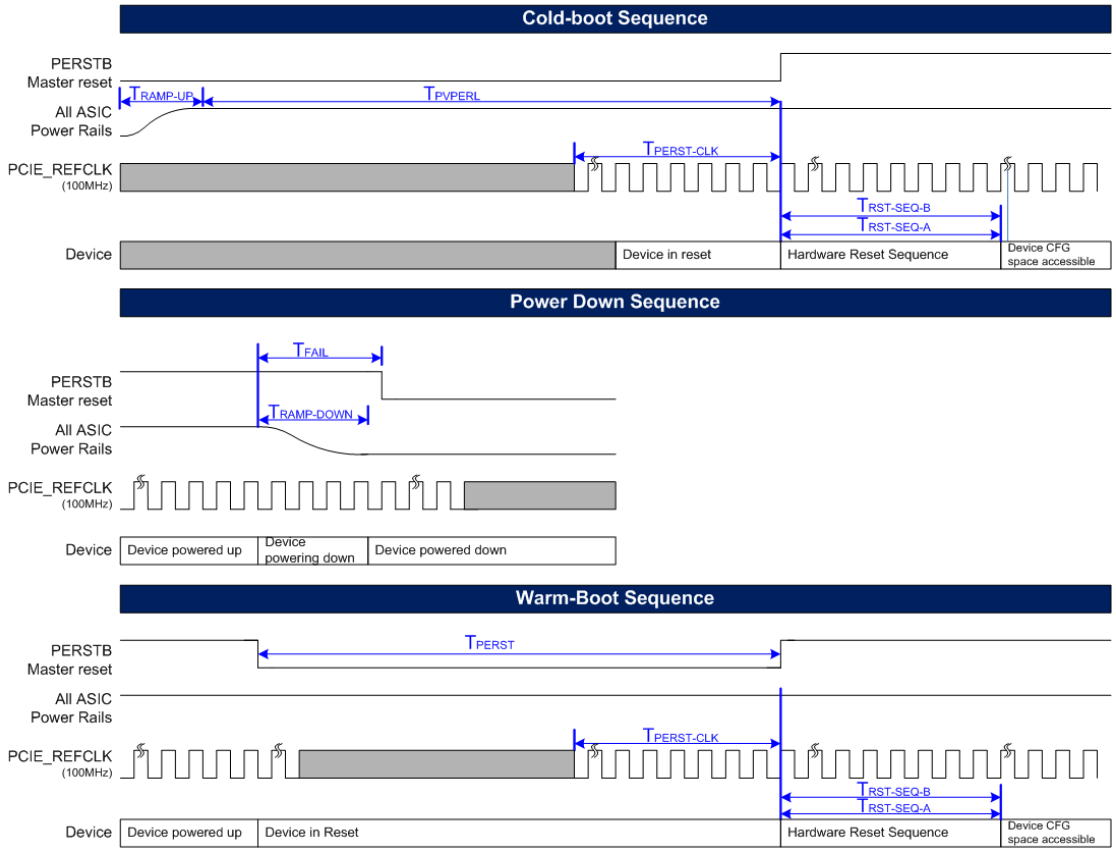



Table 4–6 Power-on Reset Sequence Timing Parameters

| Parameter | Description | Minimum Time | Maximum Time |
|---|---|---|---|
| $T_{RAMP-UP}$ | Power rail ramp-up time | 0 ms | 20 ms |
| $T_{PVPERL}$ | All GPU power rails stable to PERSTB inactive | 100 ms | Not limited |
| $T_{PERST-CLK}$ | PCIE_REFCLK stable before PERSTB inactive | 100 µs | Not limited |
| $T_{RST-SEQ-A}$ | The time required by the GPU to complete its internal reset sequence, and become ready for PCI configuration space access | N/A | 100 ms |

| Parameter | Description | Minimum Time | Maximum Time |
|---|---|---|---|
| $T_{RST-SEQ-B}$ | The time the system software must wait after de-assertion of PERSTB before accessing the GPU's PCI configuration space | 100 ms | Not limited |
| $T_{RAMP-DOWN}$ | Power rail ramp-down time | 0 ms | 20 ms |
| $T_{FAIL}$ | Power level invalid to PERSTB active | No requirements | No requirements |
| $T_{PERST}$ | PERSTB active time | 100 µs | Not limited |

### 4.3.2 Standard Boot-up Sequence

1. PERSTB (fundamental reset) is asserted to the device.
2. Select internal-strap values are determined by the configuration of pin straps on a subset of GPIOs on the board.
3. PERSTB is deasserted, and pin-strap settings are latched permanently into the device (until PERSTB is asserted again, or the power is removed).
4. In parallel:
   a. The device begins to read "eFuse straps."
   b. If a ROM exists (and is programmed), the device begins to read "ROM straps" from its external ROM.

   **Note:** The system may not issue a configuration transaction to the device until the device internal reset sequence is complete.
5. For an add-in card implementation, the device completes reading the "ROM straps."
6. Device internal reset is complete. The system begins enumerating the devices attached to it by issuing configuration transactions.
7. The chip responds to any pending transaction requests, and the system continues PCI Express® enumeration, which sets up the configuration registers of the device.
8. The system copies the contents of the ROM into system memory, and executes the video BIOS, completing the device initialization. This occurs before POST begins in the system BIOS, based on the *PC 98 System Design Guide*.

   The device is ready for normal operation.

There are three configurations for strap/BIOS implementation:

**Configuration 1.** The controller is located on an add-in card, and there is access to a local video BIOS serial flash memory.

The ROM state machine of "Polaris 20" will read in all the "ROM-based straps" right after PERSTB reset is deasserted. There are a total of 33 DWORDs of "ROM-based straps" which are stored at byte locations 0x70 through 0xF4 in the serial flash memory. See Table 3–26 (p. 39) for details.

For "Polaris 20", security features have been implemented to block access to the ROM when a fuse is set. After this, when the ROM needs to be accessed, external software will have to message the SMU firmware which will authenticate the new ROM contents and write it out.

**Configuration 2.** The controller is located on the system motherboard and the video BIOS is stored in the system BIOS serial-flash memory (i.e., no dedicated ROM for the video BIOS).

The system BIOS will be responsible for loading the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID through an aliased address in the controller chip's configuration space. The reason for writing through an aliased address (16#4c) is that the configuration location 16#2c is read only. Any writes to this location (16#4c) will also change the content of the SUBSYSTEM_VENDOR_ID at 16#2c.

**Configuration 3.** A combination of configurations 1 and 2 (add-in card and device on the motherboard)

The system BIOS will take care of the graphics device on the motherboard as in case 2, while the chip on the add-in board will be taken care of as in case 1. This should cover the situation where the OS does not read the add-in card’s video BIOS because the ROM state machine from the graphics chip reads the "ROM-based straps" independently from the video BIOS.

**Note:** If neither the system BIOS nor the add-in card video BIOS supply the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID, their values default to the DEVICE_ID and VENDOR_ID respectively inside the chip.

## 4.4 Serial Flash Read/Write Timing

Figure 4–4 Serial Flash Write/Read Timing

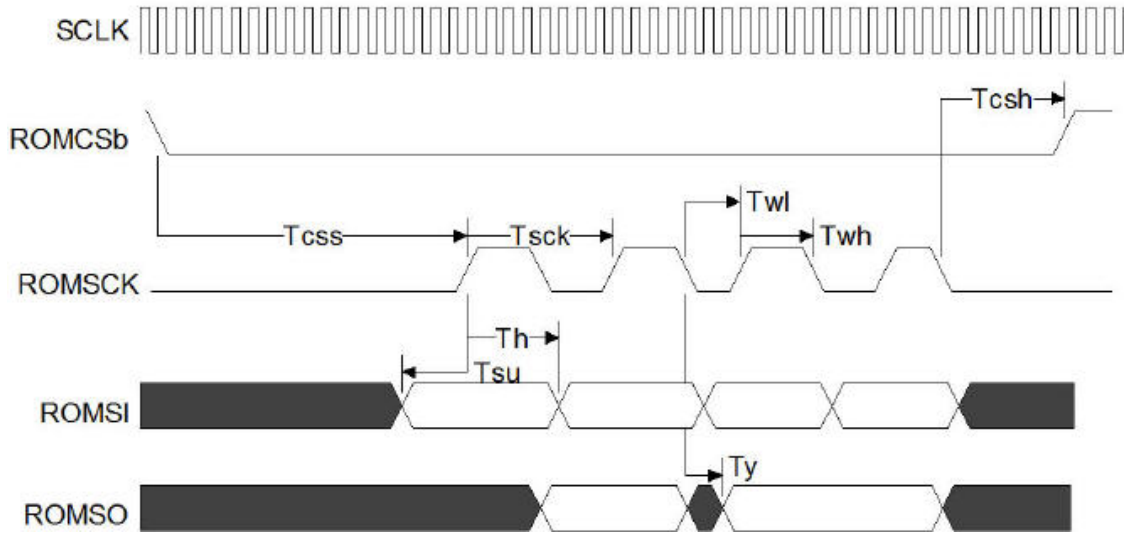



Table 4–7 Serial Flash Write/Read Timing Parameters for the Bootup Case

| Symbol | Description | Min (ns) | Max (ns) |
|---|---|---|---|
| **Tcss** | ROMCSb falling edge to first clock sent to the device. | 110 | |
| **Tsck** | ROMSCK period. | 70 | |
| **Twl** | ROMSCK low time. | 30 | |
| **Twh** | ROMSCK high time. | 30 | |
| **Tsu** | ROMSI data setup. | 20 | |

| Symbol | Description | Min (ns) | Max (ns) |
|---|---|---|---|
| **Th** | ROMSI data hold. | 40 | |
| **Ty** | ROMSO data valid. | 0 | 20 |
| **Tcsh** | Last clock sent to the ROMCSb rising edge. | 70 | |
| **SCLK = 100 MHz, XTALIN = 27 MHz, ROM_CNTL.SCK_PRESCALE_CRYSTAL_CLK=0x1** | | | |

# 5

# Electrical Characteristics

This chapter describes the electrical characteristics of "Polaris 20".

All voltages are with respect to VSS unless specified otherwise.

To link to a topic of interest, use the following list of linked cross-references:



## 5.1 Maximum Voltage Ranges

**Note:** The maximum voltage ranges are stress voltage ranges only, and the operation of the device at these conditions is not implied. Voltage ranges refer to the delta between FB_VDDC and FB_VSS, FB_VDDCI and FB_VSS, or power balls and VSS for rails that do not have voltage sensing feedback. Any stress voltage greater than the *absolute maximum range* may cause permanent damage to the device, or adversely affect the device reliability.

Table 5–1 Maximum Voltage Ranges

| Supply | Maximum Voltage Range |
|---|---|
| **VDDC, VDDCI** | 0 V to 1.075 V |
| **VDD_33** | 0 V to 3.630 V |
| **VMEMIO** | 0 V to 1.600 V |
| **VDD_18, TSVDD** | 0 V to 1.980 V |
| **VDD_08** | 0 V to 0.945 V |

## 5.2 Electrical Design Power

The following table lists the estimated Thermal Design Current (TDC) numbers for all GPU power rails. Designers must ensure that their regulator circuits are capable of supplying continuous TDC safely. The regulator circuits must also meet AMD's

Electrical Design Current (EDC) requirement that is defined as the minimum current for which the voltage regulator must be capable of safely supplying for a minimum of 1 ms. This means that if a voltage regulator design can safely supply this amount of current for more than 1 ms, it meets AMD's EDC criterion. EDC can be estimated to be 1.5 times of TDC unless otherwise specified.

It is required that AMD's SVI2-compliant voltage controllers be used on all "Polaris 20" designs for VDDC. A SVI2-compliant voltage controller has two independent voltage domains built in such that one controller can deliver two power rails to the GPU (the main domain powers VDDC, and the 2nd domain powers VDDCI), saving both cost and space compared to two-regulator solutions. Both voltage outputs are controlled through the high-speed SVI2 bus from dedicated GPU pins.

All voltage regulators that are compliant with AMD's SVI2 specification use the SVT pin to serially stream real-time voltage and current telemetry to the GPU. "Polaris 20" uses the telemetry information to enable power management features. In order to maintain the accuracy of the current measurement, it is required that the passive current-sensing components have a tolerance less than or equal to ±5%. For example, if an inductor DCR (direct current resistance) is being used as the current-sensing element, the tolerance of the DCR must be less than or equal to ±5%. Full-scale current calibration is also required. Please refer to AMD's application note, order# 54265, for details on the calibration procedure.

For the power-up sequence requirements affected by the adoption of SVI2-compliant voltage regulators, refer to Power-up/down Sequence (p. 53).

To allow for driver optimizations, faster CPUs, and new applications, designers need to provide adequate electrical margins.

The numbers are preliminary estimates and subject to change.

Table 5–2 Regulator Guidelines

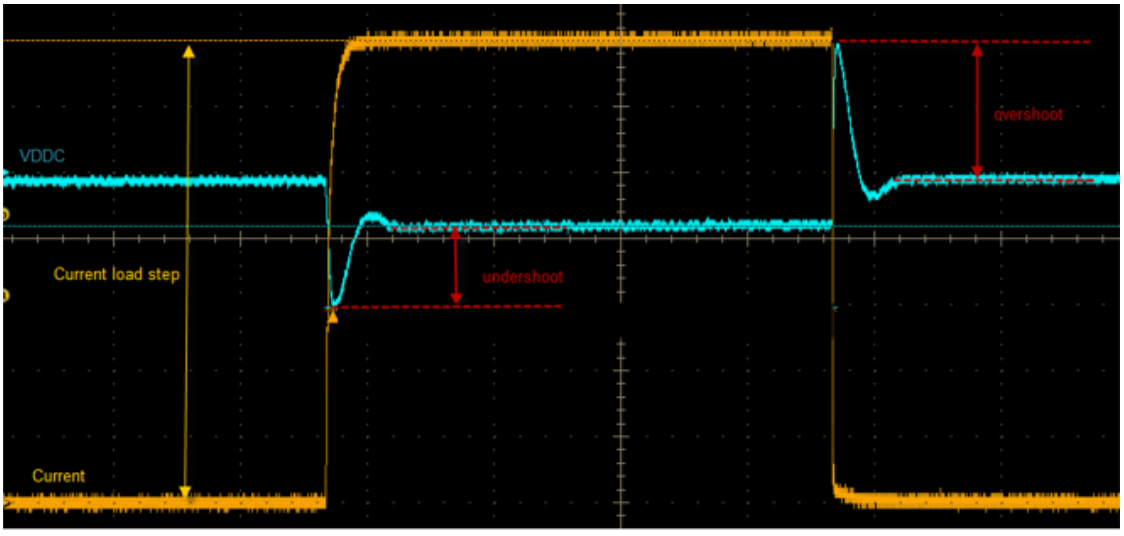
| Rail Name | | Nominal Voltage | DC Tolerance | AC Tolerance | Maximum Current | Notes |
|---|---|---|---|---|---|---|
| VDDC | "Polaris 20 XL" | 0.750 V to 1.150 V | VID_VDDC - I_VDDC × 0.3 mΩ ± 20 mV | Overshoot: TBD<br>Undershoot: TBD | 107 A (TDC)<br>TBD (EDC) | 1, 2, 4, 7 |
| | "Polaris 20 XTX" | 0.750 V to 1.200 V | | Overshoot: TBD<br>Undershoot: TBD | 132 A (TDC)<br>TBD (EDC) | |
| VDDCI | "Polaris 20 XL" | 0.80 V to 0.90 V | ±3% | ±3% | 19 A (TDC) | |
| | "Polaris 20 XTX" | 0.80 V to 0.95 V | | | | |
| VDD_08 | | 0.9 V | ±3% | ±3% | 4 A (TDC) | |
| VMEMIO | | 1.5 V or 1.55 V | ±3% | ±3% | 5 A (TDC)<br>10 A (EDC) | 3 |

| Rail Name | Nominal Voltage | DC Tolerance | AC Tolerance | Maximum Current | Notes |
|---|---|---|---|---|---|
| VDD_18 | 1.8 V | ±3% | ±3% | 1 A (TDC) | 5, 6 |
| VDD_33 | 3.3 V | ±3% | ±3% | 10 mA (TDC) | |
| TSVDD | 1.8 V | ±3% | ±3% | 13 mA (TDC) | |

**Note:**

1. The SVI2 regulator can provide any voltage required on VDDC.
2. EDC can be optimized based on the platform specifics. Contact AMD for more details.
3. GPU consumption only and does not include memory parts. Consult with your memory vendor for additional current requirements to size the regulator. Voltage requirements are vendor- and speed-dependent.
4. AMD requires an effective load line of 0.3 mΩ on the VDDC rail. Some AMD reference designs set initial load line to 0.5 mΩ on the PCB and rely on the VBIOS to trim it down to 0.3 mΩ.
5. If a switching regulator is used to power VDD_18, a filter inductor should be placed between the output of the regulator circuit and the GPU decoupling capacitors, and outside the feedback loop of the switching regulator. The filter inductor should be of 0.24 µH, and its DCR should be of 15 mΩ or less. The LDO solution does not need the filter inductor.
6. For the switching regulator, tolerance is defined at the 1.8-V regulator output before the filter inductor.
7. Undershoot and overshoot are conceptually illustrated in the following figure (Figure 5–1 (p. 53)). The set voltage is TBD. The current load step is TBD.

Figure 5–1 Sample Undershoot and Overshoot




## 5.3 Power-up/down Sequence

**"Polaris 20" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:**

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 µs before VDDC, VDDCI, and VDD_08 start to ramp up.

## 5.4 TTL Interface Electrical Characteristics

The following table provides the electrical characteristics of the TTL Interface (GPIOs).

Table 5–3 DC Characteristics for 3.3-V GPIO Pads

| Parameter | Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| **$V_{IL}$—input voltage low level.** | Maximum DC voltage at the PAD pin that will produce a logic low. | — | 0.7 | V | — |
| **$V_{IH}$—input voltage high level.** | Minimum DC voltage at the PAD pin that will produce logic high. | 1.7 | — | V | — |
| **$V_{OL}$—output voltage low level.** | Maximum output low voltage @ I = 8 mA. | — | 0.42 | V | 1, 2 |
| **$V_{OH}$—output voltage high level.** | Minimum output high voltage @ I = 8 mA. | 2.5 | — | V | 1, 2 |
| **$I_{OL}$—output current low level.** | Minimum output low current @ V = 0.1 V. | 1.9 | — | mA | 1, 2 |
| **$I_{OH}$—output current high level.** | Minimum output high current @ V = VDDR - 0.1 V. | 1.9 | — | mA | 1, 2 |

## 5.5 Memory Interface Electrical Characteristics

The following table provides the electrical characteristics of the memory interface.

Table 5–4 Memory Interface Electrical Characteristics

| Parameters | Min | Typical | Max |
|---|---|---|---|
| **DDR3/GDDR5:**<br>**MVREFx, MVREFDx—input reference voltages.** | 0.69 × VMEMIO | 0.7 × VMEMIO | 0.71 × VMEMIO |
| **$V_{IH-DC}$—DC input logic high level.** | MVREFDx + 100 mV | — | VMEMIO |
| **$V_{IL-DC}$—DC input logic low level.** | 0 | — | MVREFDx - 100 mV |
| **$V_{IH-AC}$—AC input logic high level.** | MVREFDx + 150 mV | — | — |
| **$V_{IL-AC}$—AC input logic low level.** | — | — | MVREFDx - 150 mV |
| **$VOL(DC)_{VMEMIO = 1.5 V}$—output logic low-level voltage.** | — | — | 0.62 V |

**Note:**

- **Peak-to-peak AC noise on MVREFDx/MVREFx may not exceed ±25 mV.**
- **VTT of the transmitting device must track VREF of the receiving device.**
- **A 1-V/ns input-signal minimum slew rate is to be maintained for DDR3.**
- **A 3-V/ns input-signal minimum slew rate is to be maintained for GDDR5.**
- **The VI-xx voltage levels exceed the DRAM specification for GDDR5, leading to higher performance.**

## 5.6 DDC $I^2C$ Mode Electrical Characteristics

The following tables provide the electrical characteristics for the DDC pins in $I^2C$ mode.

Table 5–5 Transmitter Electrical Specification for DDC I²C

| Symbol | Description | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| **I2C_Tx$_{Freq}$** | Supported transmittable data rate. | — | 400 | kHz | - |
| **I2C_V$_{OL}$** | Maximum output low voltage @ I = 8 mA. | — | 300 | mV | 1, 2, 3 |
| **I2C_V$_{OH}$** | Minimum output high voltage. | VDD5 - 0.25 | — | mV | 1, 2, 3, 4 |

**Note:**
1. **For detailed current/voltage characteristics, refer to the IBIS model.**
2. **Measurement taken with NMOS strength set to default values, PVT = Noml case.**
3. **The I²C interface is an open-drain circuit and pull high is determined by external power.**
4. **VDD5 refers to a 5-V external pull up.**

Table 5–6 Receiver Electrical Specification for DDC I²C Pins

| Symbol | Description | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| **I2C_Y_V$_{IH-AC}$** | Minimum AC voltage at the PAD pin that will produce a stable high at the I2C_Y pin of the macro. | 2.3 | | V | 3 |
| **I2C_Y_V$_{IL-AC}$** | Maximum AC voltage at the PAD pin that will produce a stable low at the I2C_Y pin of the macro. | | 1.5 | V | 3 |
| **I2C_Y_V$_{IH-DC}$** | Minimum DC voltage at the PAD pin that will produce a stable high at the I2C_Y pin of the macro. | 2.3 | | V | 1 |
| **I2C_Y_V$_{IL-DC}$** | Maximum DC voltage at the PAD pin that will produce a stable low at the I2C_Y pin of the macro. | | 1.5 | V | 1 |
| **I2C_Y_Rx$_{Freq}$** | Supported received frequency. | | 400 | kHz | - |
| **I2C_Y$_{dc}$** | I2C_Y output duty cycle. | 40 | 60 | % | 2 |

**Note:**
1. **Measured with an edge rate of 1 µs at the PAD pin.**
2. **Assuming perfect duty cycle on input.**
3. **Measured at the maximum operating frequency.**

## 5.7 DisplayPort AUX Electrical Specification

This table provides the electrical characteristics of the DisplayPort AUX.

Table 5–7 DisplayPort AUX Electrical Specification

| Symbol | Description | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| **AUX_V$_{cm}$** | Input/output common-mode voltage. | 550 | 620 | mV | - |
| **AUX_V$_{diff}$** | Pad differential-output swing. | 525 | 622 | mV | - |
| **AUX_Tx$_{Freq}$** | Supported transmit-data rate. | — | 5 | MHz | - |
| **AUX_Rx$_{Freq}$** | Supported received frequency. | — | 5 | MHz | - |
| **AUX_Pad$_{dc}$** | PADP/N output duty cycle. | 40 | 60 | % | 1 |

**Note:**
1. **Assuming perfect duty cycle on input.**

## 5.8 DisplayPort Main Link Electrical Characteristics

This table provides the electrical characteristics of the DisplayPort main link.

Table 5–8 DisplayPort Main Link Electrical Specification

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $UI_{HIGH\_RATE}$ | Unit interval for the DP high bit rate (2.7 Gbps/lane). | — | 370 | — | ps | High limit = +300 ppm<br>Low limit = -5300 ppm |
| $UI_{LOW\_RATE}$ | Unit interval for the DP reduced bit rate (1.62 Gbps/ lane). | — | 617 | — | ps | High limit = +300 ppm<br>Low limit = -5300 ppm |
| $UI_{HIGH\_RATE2}$ | Unit interval for DP high-bit rate 2 (5.4 Gbps/lane). | — | 185 | — | ps | High limit = +300 ppm<br>Low limit = -5300 ppm |
| $V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$ | Ratio of output voltage level 1/ level 0. | 0.8 | | 6.0 | dB | - |
| | Ratio of output voltage level 2/ level 1. | 0.1 | | 5.1 | dB | - |
| $V_{TX\text{-}OUTPUT\text{-}RATIO\_HBR2}$ | Ratio of output voltage level 2/ level 0. | 5.2 | | 6.9 | dB | - |
| | Ratio of output voltage level 2/ level 1. | 1.6 | | 3.5 | dB | - |
| $V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$ | Delta of pre-emphasis level 1 versus level 0. | 2.0 | | | dB | - |
| | Delta of pre-emphasis level 2 versus level 1. | 1.6 | | | dB | - |
| $V_{TX\text{-}PREEMP\text{-}OFF}$ | Maximum pre-emphasis when disabled. | | | 0.25 | dB | - |

## 5.9 SMBus Electrical Characteristics

The following tables provide the electrical characteristics for the SMBus DATA, CLOCK, and CLK_REQB pads.

Table 5–9 Transmitter Electrical Specification

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $F_{TX}$ | Supported transmit data rate. | — | 100 | kHz |
| $V_{OL}$ | Maximum output low voltage @ I = 4 mA. | — | 200 | mV |
| $V_{OH}$ | Minimum output high voltage. | VDD33 - 0.4 | — | mV |

Table 5–10 Receiver Electrical Specification

| Symbol | Description | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $VIH_{AC}$ | Minimum AC voltage at the PAD pin that will produce a stable high at the Y pin of the macro at FRX. | 2.0 | — | V | 3 |
| $VIL_{AC}$ | Maximum AC voltage at the PAD pin that will produce a stable low at the Y pin of the macro. | — | 0.8 | V | 3 |
| $VIH_{DC}$ | Minimum DC voltage at the PAD pin that will produce a stable high at the Y pin of the macro. | 2.0 | — | V | 1 |

| Symbol | Description | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $VIL_{DC}$ | Maximum DC voltage at the PAD pin that will produce a stable low at the Y pin of the macro. | — | 0.8 | V | 1 |
| $F_{RX}$ | Supported received frequency. | — | 100 | kHz | - |
| $Y_{dc}$ | Y output duty cycle. | 40 | 60 | % | 2 |
| $Y_{tiPDr}$ | Receiver propagation delay rise. | — | 400 | ns | 1, 2, 4 |
| $Y_{tiPDf}$ | Receiver propagation delay fall. | — | 20 | ns | 1, 2, 4 |

1. **Measured with an edge rate of 1 µs at the PAD pin.**
2. **Assuming perfect duty cycle on input.**
3. **Measured at the maximum operating frequency.**
4. **Typical simulation corner only.**

# 6

# Thermal Data

To link to a topic of interest, use the following list of linked cross-references:



## 6.1 Thermal Equations

For the thermal equations, the Delphi model is recommended.

**Note:** Thermal simulation models are available. Please refer to the AMD OEM Resource Center for more information.

## 6.2 Thermal Characteristics

For engineering design purposes, the thermal characteristics, $T_C$max and $T_J$max, found in the thermal simulation models are not practical as they are not easily determined. Instead, it is more convenient to define a new parameter, maximum recommended operating temperature ($T_{j,op}$), and re-define $T_{j,\ max}$ as shown in the following table:

Table 6–1 Thermal Characteristics

| Variable | Value |
|---|---|
| **$T_{j,op}$: Maximum recommended operating temperature.**<br>**This is the maximum temperature at which the functionality is qualified and tested. Operation above this temperature will negatively impact product reliability.**<br>**This temperature is measured using an on-die temperature sensor near the integrated thermal diode (see Thermal Diode Characteristics (p. 60)).** | 90°C |
| **$T_{j,max}$: Absolute maximum rated junction temperature.**<br>**This is the maximum allowable instantaneous GPU temperature, above which damage to the GPU is likely.**<br>**This temperature is measured using an on-die temperature sensor near the integrated thermal diode (see Thermal Diode Characteristics (p. 60)).** | 96°C |
| **Minimum ambient operating temperature.** | 0°C |
| **$\theta_{JC}$: Junction to case thermal resistance (based on the two-resistor model).**<br>**Note: Case here means the center of the top of the GPU package.** | 0.05°C/W |
| **$\theta_{JB}$: Junction to board thermal resistance (based on the two-resistor model).** | 6.49°C/W |

## 6.3 Thermal Design Power (TDP)

The thermal design power is defined as the power dissipated by the GPU while running a selected application at up to the maximum recommended operating temperature, and is measured as the maximum average power in a five-second moving window.

The TDP is intended as a recommended thermal design point; it is not an absolute maximum power under all conditions.

"Polaris 20" has up to eight defined Dynamic Power Management (DPM) states, from DPM_0 to DPM_7, in ascending order of performance and power. When a graphics demanding application (such as a game) is running, AMD's PowerTune constantly switches GPU among the states based on run-time analysis of GPU activities, power and thermal conditions. The effective power/performance depends on the percentage of time spent in each state.

The data are targets only, and are subject to change.

Table 6–2 TDP for Discrete Variants

| **Variant** | | **"Polaris 20 XL"** | **"Polaris 20 XTX"** |
|---|---|---|---|
| **VDDC (V)** | | 0.750 to 1.150 | 0.750 to 1.200 |
| **VDDCI (V)** | | 0.800 to 0.900 | 0.800 to 0.950 |
| **Engine (MHz)** | DPM_7 | 1244 | 1340 |
| | DPM_6 | 1209 | 1300 |
| | DPM_5 | 1168 | 1257 |
| | DPM_4 | 1106 | 1215 |
| | DPM_3 | 1041 | 1145 |
| | DPM_2 | 952 | 900 |
| | DPM_1 | 588 | 600 |
| | DPM_0 | 300 | 300 |
| **Memory (MHz)** | | 300 / 1000 / 1750 | 300 / 1000 / 2000 |
| **Memory Voltage (V)** | | 1.5 or 1.55 | |
| **Memory Interface (bits)** | | 256 | |
| **GPU Leakage** | | Variable | |
| **GPU Die Temperature (°C)** | | 90 | |
| **Driver** | | 17.10 | |
| **Test Platform** | | Intel Core™ i7-4790X Extreme Edition 3.6-GHz CPU, 16-GB RAM | |
| **PCIe® Configuration** | | PCIe revision 3.0, up to 8.0 GT/s | |
| **TDP Targets (W)** | | 110 | 135 |

## 6.4 Thermal Diode Characteristics

For "Polaris 20", the ideality factor of the on-die thermal diode varies significantly with temperature and sourcing current. If a design chooses to use the GPU's on-die thermal diode coupled with an external thermal sensor chip to read the GPU temperature, the external thermal sensor chip must support and enable beta compensation.

## 6.5 Storage Requirements

Ambient temperature < 40°C

Relative humidity < 90%

# 7

# Mechanical Data

This chapter contains information on the mechanical data for "Polaris 20". To go to a topic of interest, use the following list of linked cross-references:



## 7.1 Physical Dimensions

### 7.1.1 "Polaris 20"-L4 Physical Dimensions

HFCBGA 40 mm × 40 mm—1401 pins

Figure 7–1 "Polaris 20"-L4 Package Outline (Preliminary—MOD-00280 REV 03)

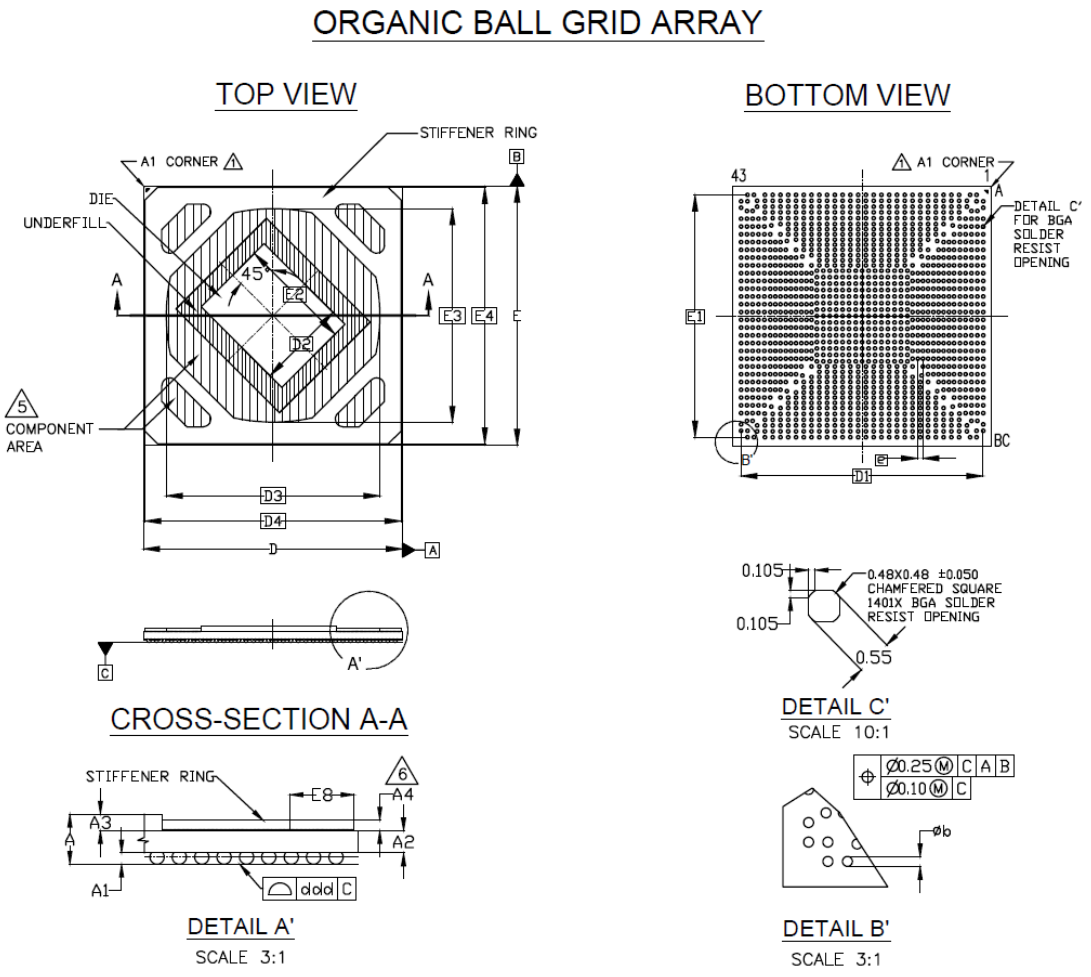


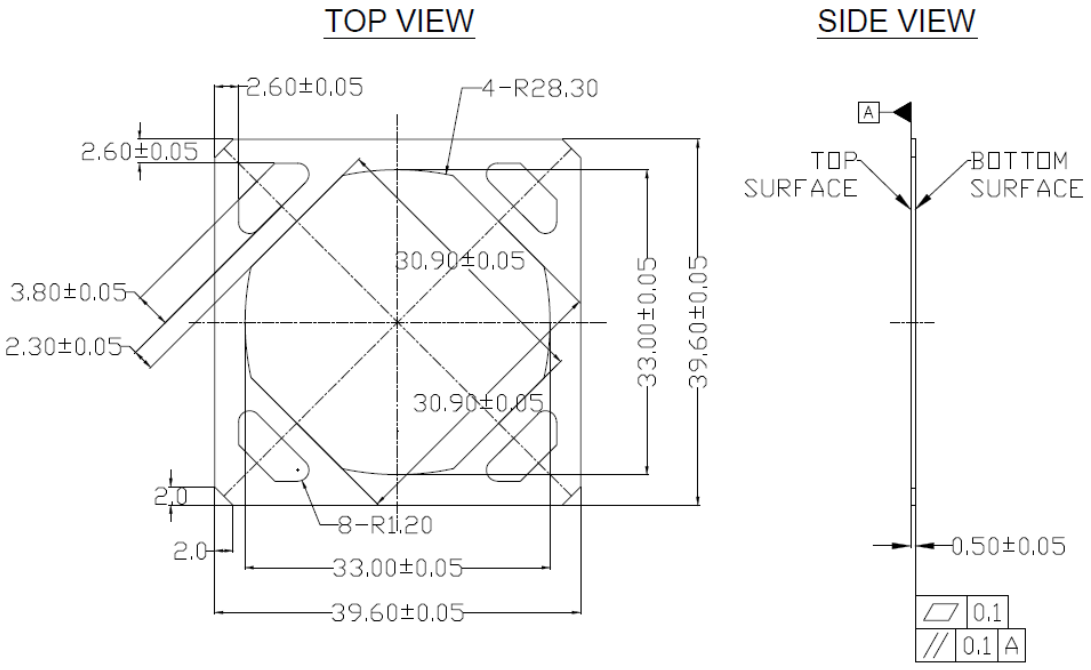

Table 7–1 -L4 Physical Dimensions (mm)

| Symbol | Minimum | Normal | Maximum | Note |
|---|---|---|---|---|
| **A** | 2.21 | 2.40 | 2.59 | See side view. |
| **A1** | 0.25 | 0.35 | 0.45 | See side view. |
| **A2** | 1.05 | 1.15 | 1.25 | See side view. |
| **A3** | 0.80 | 0.85 | 0.90 | See side view. |
| **A4** | 0.50 | 0.55 | 0.60 | See side view. |
| **øb** | — | — | — | See note 3 below and bottom view. |
| **D** | 39.90 | 40.00 | 40.10 | See top view. |
| **D1** | — | 37.40 | — | See bottom view. |
| **D2** | — | 13.80 | — | See top view. |
| **D3** | — | 33.00 | — | See top view. |
| **D4** | — | 39.60 | — | See top view. |
| **E** | 39.90 | 40.00 | 40.10 | See top view. |
| **E1** | — | 37.40 | — | See bottom view. |
| **E2** | — | 17.63 | — | See top view. |
| **E3** | — | 33.00 | — | See top view. |

| Symbol | Minimum | Normal | Maximum | Note |
|---|---|---|---|---|
| **E4** | — | 39.60 | — | See top view. |
| **E8** | | 3.30 | | See side view. |
| **e** | | 0.80 BSC (basic) | | See bottom view. |
| **ddd** | — | — | 0.23 | See side view. |
| **N** | | 1401 | | Number of pins. |

**Note:**
1. **This is a multi-pitch (more than one pitch or distance on the substrate between the balls) package.**
2. **The SMT (surface mount technology) component height from the substrate top surface is 0.65 mm maximum.**
3. **Before solder ball attach reflow, the solder ball diameter øb is 0.50 nominal. After solder ball attach reflow, the solder ball diameter øb is 0.55 ± 0.10.**

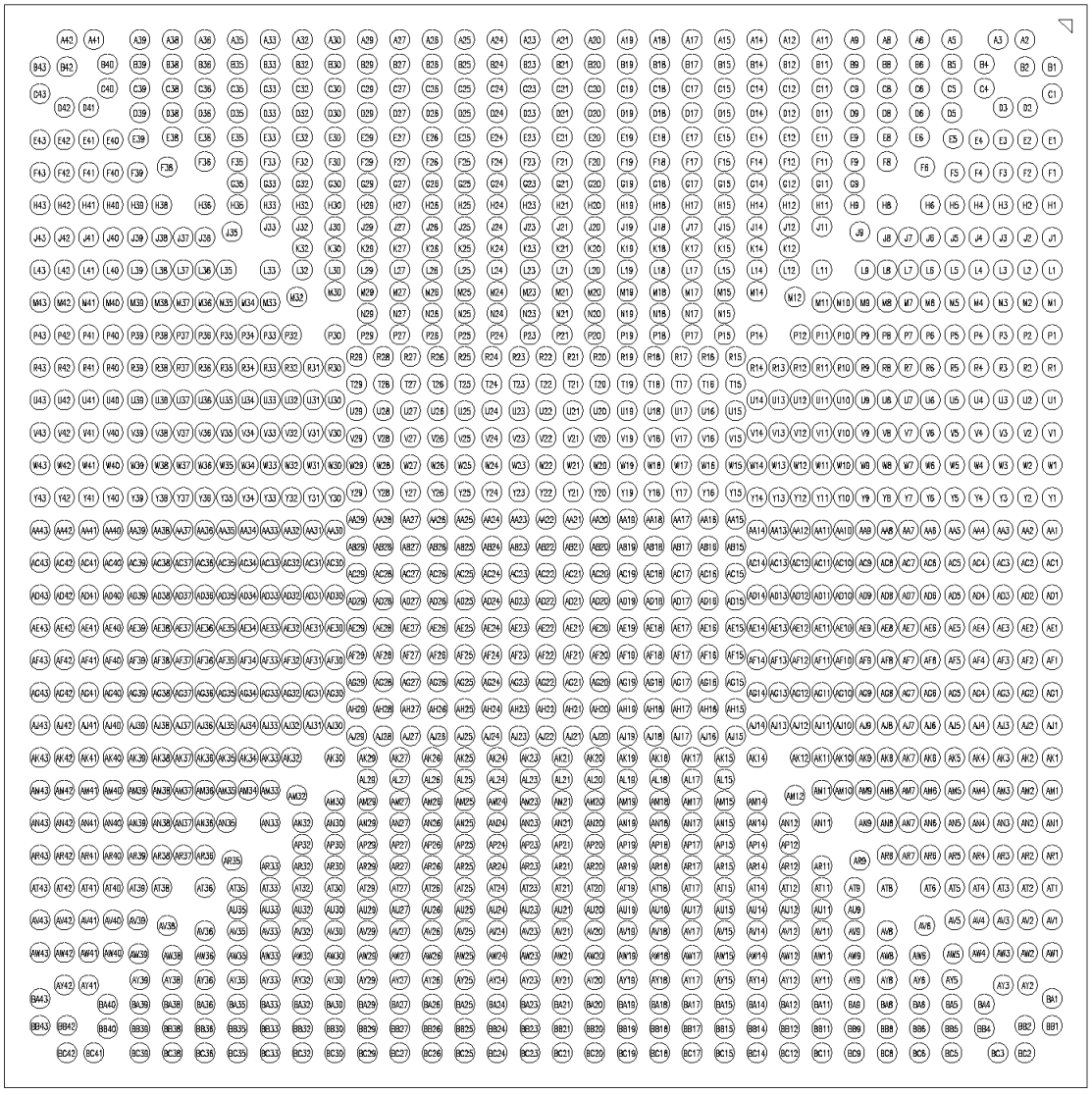
Figure 7–2 "Polaris 20"-L4 Ring Stiffener




**Note:** The following notes are for the "Polaris 20"-L4 stiffener ring with 0.50 mm thickness:

- The maximum standard radius is 0.20 mm.
- The maximum burr size is 0.05 mm.
- The material is copper (C1100).
- The surface finish is Ni plating at 5 µM to 15 µM.

Figure 7–3 "Polaris 20"-L4 Ball Arrangement



## 7.2 Pressure Specification

To avoid damage to the GPU (die or solder-ball joint cracks) caused by improper mechanical assembly of the cooling device, follow the following recommendations:

- It is recommended that the maximum pressure that is evenly applied across the contact area between the thermal management device and the die does not exceed 75 PSI. A contact pressure of 30-40 PSI is adequate to secure the thermal management device and to achieve the lowest thermal contact resistance with a temperature drop across the thermal interface material of no more than 3°C. Also, the surface flatness of the metal spreader should be 0.001 inch/1 inch.
- Pre-test the assembly fixture with a strain gauge to ensure that the flexing of the final assembled board and the pressure applying around the GPU package will not exceed 600-micron strain under any circumstance.
- Ensure that any distortion (bow or twist) of the board after SMT and cooling device assembly is within industry guidelines (IPC/EIA J-STD-001). For the measurement method, refer to the industry approved technique described in the manual, *IPC-TM-650*, section 2.4.22.

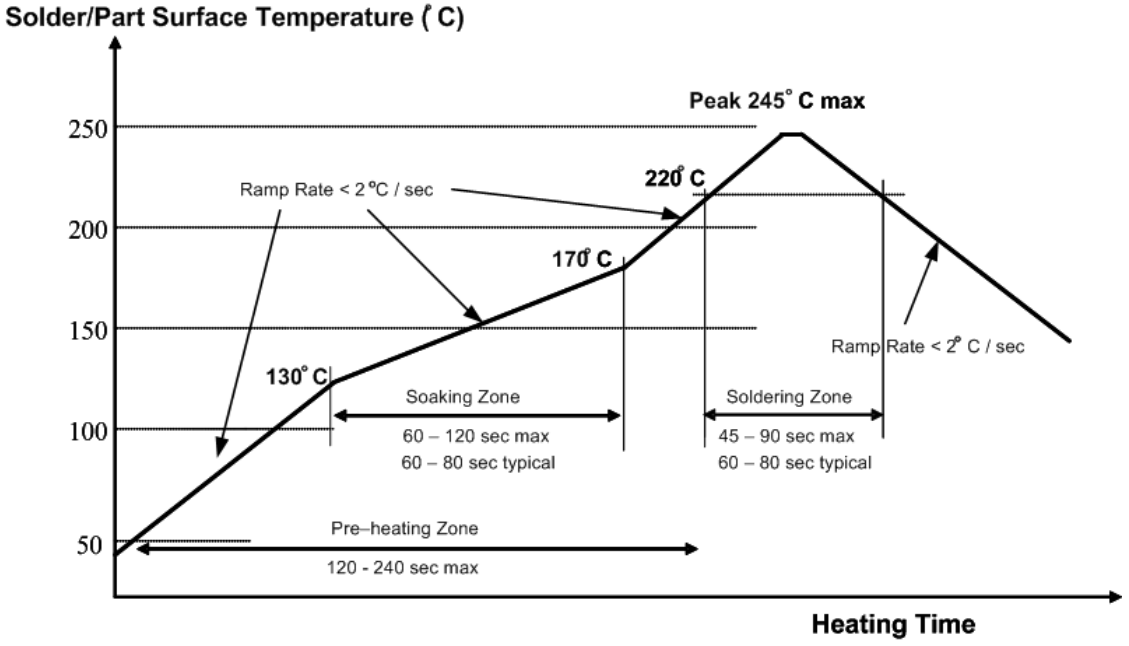
## 7.3 Board Solder Reflow Process Recommendations

### 7.3.1 Stencil Opening Size for Solderball Pads on PCB

Warpage of the PCB and the BGA package may cause solder-joint quality issues at the surface mount. Therefore, it is recommended that the stencil opening sizes be adjusted to compensate for the warpage. The recommendation is for the stencil aperture of BGA balls to be kept as the same size as the PWB BGA pad design.

### 7.3.2 FCBGA Reference Reflow Profile for RoHS/Lead-free Solder

Figure 7–4 FCBGA Reference Reflow Profile for RoHS/Lead-Free SMT




Notes when using RoHS/lead-free solder (SAC305 Tin-Silver-Cu):

- The final reflow temperature profile will depend on the type of solder paste and chemistry of flux used in the SMT process or BGA rework process. Modifications to this reference reflow profile may also be required in order to accommodate to other critical components.
- The use of a reflow oven with 10 heating zones or above is highly recommended.
- To ensure that the reflow profile meets the target specification on both sides of SMT components, a different reflow profile for the first and second reflow may be required.
- A mechanical stiffening carrier boat can be used to minimize PWB warpage during the reflow process.
- It is suggested to decrease the temperature cooling rate to minimize BGA component and PWB warpage.
- This recommended reflow profile applies only to the RoHS/lead-free (high temperature) soldering process, and it should not be applied to Eutectic solder packages without any reliability validation.
- Maximum three reflows are allowed on the same part.

Table 7–2 Recommended Profiling — RoHS/Lead-Free Solder

| Profiling Stage | Temperature | Process Range |
|---|---|---|
| **Overall Preheat** | Room temperature to 220℃ | Two to four minutes |
| **Soaking Time** | 130℃ to 170℃ | Typically 60 to 80 seconds |
| **Liquidus** | 220℃ | Typically 60 to 80 seconds |
| **Ramp Rate** | Ramp up and cooling | < 2℃ / second |
| **Peak** | Maximum 245℃ | 235℃ ± 5℃ |
| **Temperature at Peak Within 5℃** | 240℃ to 245℃ | 10 to 30 seconds |

# 8

# Boundary Scan Specification

This chapter contains information on boundary scan specifications as they apply to "Polaris 20". To go to a topic of interest, use the following list of linked cross-references:



## 8.1 Introduction

"Polaris 20" has a JTAG 1149.1 compliant TAP controller. The boundary scan implementation is IEEE compliant. The implementation supports BYPASS, EXTEST, and PRELOAD instructions. A BSDL file for each of the modes can be obtained from the AMD OEM Resource Center.

## 8.2 Boundary Scan

The "Polaris 20" boundary scan can perform board-level capture and drive out on all pins mentioned in the BSDL file.

## 8.3 JTAG Interface Signals

Table 8–1 JTAG Interface

| Pin-name | I/O | Description |
|---|---|---|
| **JTAG_TCK** | I | TCK: Test clock. |
| **JTAG_TMS** | I | TMS: Test mode select. |
| **JTAG_TDI** | I | TDI: Test data in. |
| **JTAG_TDO** | O | TDO: Test data out. |
| **JTAG_TRSTB** | I | TRST#: Test asynchronous reset. |
| **TESTEN** | I | Compliance pin: Pull up to 3.3 V to enable JTAG access. |

## 8.4 JTAG Timing Characteristics

Table 8–2 JTAG Timing Characteristics

| Symbol | Description | Min | Max |
|---|---|---|---|
| $f_{cyc}$ | Frequency of operation. | 0.001 MHz | 10 MHz |
| $t_{cyc}$ | TCK cycle period. | 0.10 µs | 1000 µs |
| $t_{bsst}$ | Input data setup time to TCK rise. | 15 ns | |
| $t_{bsht}$ | Input data hold time to TCK rise. | 20 ns | |
| $t_{bsdv}$ | TCK low to output data valid. | 0.00 µs | 0.05 µs |
| $t_{tcst}$ | TDI, TMS setup time to TCK rise. | 2.5 ns | |
| $t_{tcht}$ | TDI, TMS hold time to TCK rise. | 3.0 ns | |
| $t_{tcdv}$ | TCK low to TDO data valid. | 0.0 µs | 0.05 µs |

Figure 8–1 Timing of the Boundary Scan Signals with Respect to TCK

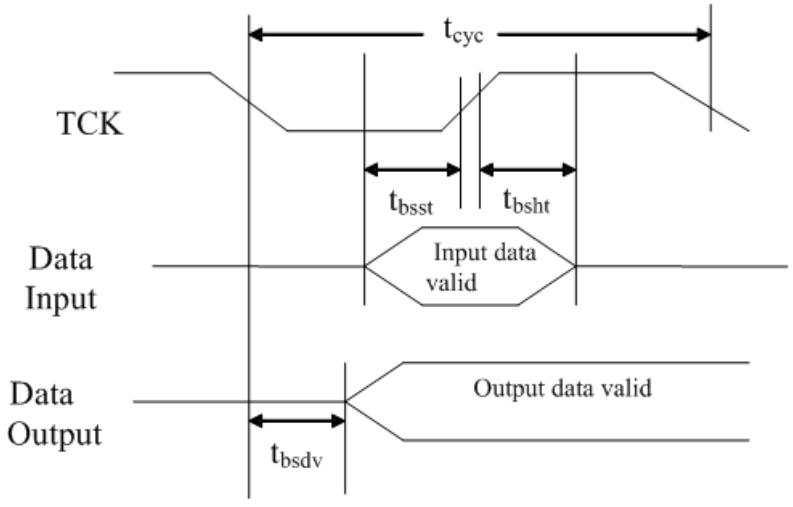
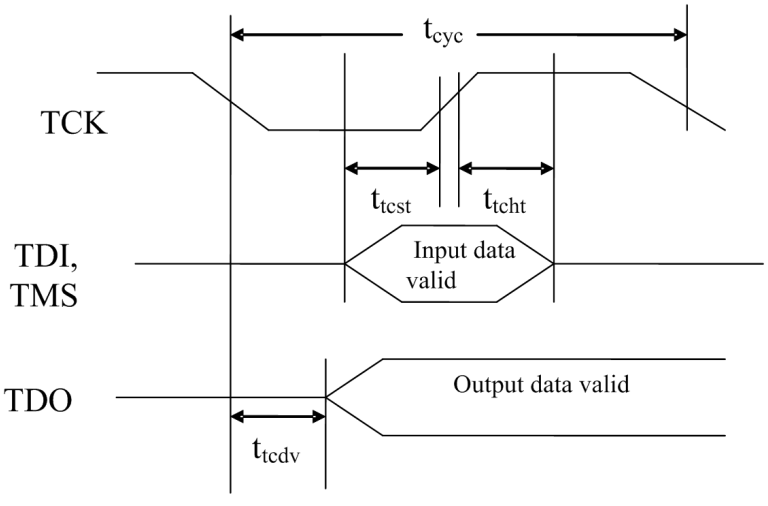



Figure 8–2 Timing of the TAP Ports (TDI, TMS, and TDO) with Respect to TCK



# Appendix A

# Pin Listings

This appendix contains pin listings for "Polaris 20" sorted in two ways. To go to the listing of interest, use the following list of linked cross-references:



## A.1 Pins Sorted by Ball Reference

Table A–1 "Polaris 20" Pins Sorted by Ball Reference

| Ball Reference | Signal Name |
|---|---|
| A2 | VSS |
| A3 | DQB1_31 |
| A5 | DDBIB1_3 |
| A6 | VSS |
| A8 | WCKB1_1 |
| A9 | DQB1_23 |
| A11 | VSS |
| A12 | EDCB1_2 |
| A14 | DQB1_18 |
| A15 | VSS |
| A17 | DQB0_21 |
| A18 | EDCB0_2 |
| A19 | VSS |
| A20 | DQB0_17 |
| A21 | WCKB0_1 |
| A23 | DQB0_29 |
| A24 | DQB0_28 |
| A25 | VSS |
| A26 | DQB0_24 |
| A27 | DQA1_15 |
| A29 | VSS |
| A30 | DDBIA1_1 |
| A32 | DQA1_8 |
| A33 | VSS |
| A35 | DQA1_7 |
| A36 | DQA1_5 |

| Ball Reference | Signal Name |
|---|---|
| A38 | VSS |
| A39 | DQA1_2 |
| A41 | DQA1_0 |
| A42 | VSS |
| B1 | VSS |
| B2 | VSS |
| B4 | DQB1_30 |
| B5 | EDCB1_3 |
| B6 | DQB1_27 |
| B8 | VSS |
| B9 | WCKB1B_1 |
| B11 | DQB1_21 |
| B12 | VSS |
| B14 | DQB1_19 |
| B15 | DQB1_16 |
| B17 | VSS |
| B18 | DQB0_20 |
| B19 | DQB0_19 |
| B20 | VSS |
| B21 | WCKB0B_1 |
| B23 | DQB0_30 |
| B24 | VSS |
| B25 | DQB0_27 |
| B26 | DQB0_25 |
| B27 | VSS |
| B29 | DQA1_12 |
| B30 | DQA1_11 |
| B32 | VSS |
| B33 | WCKA1_0 |
| B35 | DQA1_6 |
| B36 | VSS |
| B38 | EDCA1_0 |
| B39 | VSS |
| B40 | DQA1_1 |
| B42 | VSS |
| B43 | VSS |
| C1 | DQC0_0 |
| C4 | DQB1_29 |
| C5 | VSS |
| C6 | DQB1_26 |
| C8 | DQB1_24 |
| C9 | VSS |

| Ball Reference | Signal Name |
|---|---|
| C11 | DQB1_22 |
| C12 | DDBIB1_2 |
| C14 | VSS |
| C15 | DQB1_17 |
| C17 | DQB0_22 |
| C18 | VSS |
| C19 | DDBIB0_2 |
| C20 | DQB0_16 |
| C21 | VSS |
| C23 | VSS |
| C24 | DDBIB0_3 |
| C25 | DQB0_26 |
| C26 | VSS |
| C27 | DQA1_14 |
| C29 | EDCA1_1 |
| C30 | VSS |
| C32 | DQA1_9 |
| C33 | WCKA1B_0 |
| C35 | VSS |
| C36 | DQA1_4 |
| C38 | DQA1_3 |
| C39 | DQA0_31 |
| C40 | VSS |
| C43 | DQA0_14 |
| D2 | DQC0_1 |
| D3 | DQC0_2 |
| D5 | DQB1_28 |
| D6 | VSS |
| D8 | DQB1_25 |
| D9 | EDCB1_1 |
| D11 | VSS |
| D12 | DQB1_20 |
| D14 | DQB1_6 |
| D15 | VSS |
| D17 | DQB0_23 |
| D18 | DQB0_15 |
| D19 | VSS |
| D20 | DQB0_18 |
| D21 | DQB0_31 |
| D23 | DQB0_5 |
| D24 | EDCB0_3 |
| D25 | VSS |

| Ball Reference | Signal Name |
|---|---|
| D26 | DQA1_29 |
| D27 | DQA1_13 |
| D29 | VSS |
| D30 | WCKA1_1 |
| D32 | DQA1_10 |
| D33 | VSS |
| D35 | EDCA1_2 |
| D36 | DDBIA1_0 |
| D38 | VSS |
| D39 | DQA0_30 |
| D41 | VSS |
| D42 | DQA0_15 |
| E1 | DDBIC0_0 |
| E2 | EDCC0_0 |
| E3 | VSS |
| E4 | DQC0_3 |
| E5 | VSS |
| E6 | VMEMIO |
| E8 | VSS |
| E9 | DQB1_12 |
| E11 | DQB1_9 |
| E12 | VMEMIO |
| E14 | DQB1_7 |
| E15 | EDCB1_0 |
| E17 | VMEMIO |
| E18 | DQB0_14 |
| E19 | DQB0_12 |
| E20 | VMEMIO |
| E21 | DQB0_8 |
| E23 | DQB0_6 |
| E24 | VSS |
| E25 | DQB0_1 |
| E26 | DQA1_30 |
| E27 | VMEMIO |
| E29 | DQA1_26 |
| E30 | WCKA1B_1 |
| E32 | VMEMIO |
| E33 | DQA1_20 |
| E35 | DDBIA1_2 |
| E36 | VSS |
| E38 | DQA1_16 |
| E39 | VSS |

| Ball Reference | Signal Name |
|---|---|
| E40 | DQA0_28 |
| E41 | DQA0_29 |
| E42 | VSS |
| E43 | DQA0_13 |
| F1 | VSS |
| F2 | DQC0_4 |
| F3 | DQC0_5 |
| F4 | VSS |
| F5 | VMEMIO |
| F6 | VSS |
| F8 | DQB1_15 |
| F9 | VSS |
| F11 | DQB1_10 |
| F12 | WCKB1_0 |
| F14 | VSS |
| F15 | DQB1_4 |
| F17 | DQB1_2 |
| F18 | VSS |
| F19 | DQB0_13 |
| F20 | DQB0_11 |
| F21 | VSS |
| F23 | VSS |
| F24 | EDCB0_0 |
| F25 | DQB0_2 |
| F26 | VSS |
| F27 | DQA1_28 |
| F29 | DQA1_27 |
| F30 | VSS |
| F32 | DQA1_22 |
| F33 | DQA1_21 |
| F35 | VSS |
| F36 | DQA1_18 |
| F38 | VSS |
| F39 | DDBIA0_3 |
| F40 | VSS |
| F41 | DQA0_12 |
| F42 | EDCA0_1 |
| F43 | VSS |
| G9 | DQB1_13 |
| G11 | VMEMIO |
| G12 | WCKB1B_0 |
| G14 | CLKB1B |

| Ball Reference | Signal Name |
|---|---|
| G15 | VMEMIO |
| G17 | DQB1_3 |
| G18 | DQB1_0 |
| G19 | VMEMIO |
| G20 | DQB0_10 |
| G21 | WCKB0_0 |
| G23 | DQB0_7 |
| G24 | DDBIB0_0 |
| G25 | VMEMIO |
| G26 | DQA1_31 |
| G27 | EDCA1_3 |
| G29 | VMEMIO |
| G30 | DQA1_24 |
| G32 | DQA1_23 |
| G33 | VMEMIO |
| G35 | DQA1_19 |
| H1 | WCKC0_0 |
| H2 | VSS |
| H3 | DQC0_7 |
| H4 | DQC0_6 |
| H5 | VSS |
| H6 | DQC0_16 |
| H8 | VSS |
| H9 | DQB1_14 |
| H11 | DQB1_11 |
| H12 | VSS |
| H14 | CLKB1 |
| H15 | DQB1_5 |
| H17 | VSS |
| H18 | DQB1_1 |
| H19 | DDBIB0_1 |
| H20 | VSS |
| H21 | WCKB0B_0 |
| H23 | MAB0_0 |
| H24 | VSS |
| H25 | DQB0_3 |
| H26 | VSS |
| H27 | VSS |
| H29 | DDBIA1_3 |
| H30 | WEA1B |
| H32 | VSS |
| H33 | MAA1_0 |

| Ball Reference | Signal Name |
|---|---|
| H35 | MAA1_6 |
| H36 | DQA1_17 |
| H38 | EDCA0_3 |
| H39 | VSS |
| H40 | DDBIA0_1 |
| H41 | DQA0_11 |
| H42 | VSS |
| H43 | DQA0_10 |
| J1 | DQC0_8 |
| J2 | WCKC0B_0 |
| J3 | VSS |
| J4 | EDCC0_2 |
| J5 | DQC0_19 |
| J6 | VSS |
| J7 | DQC0_18 |
| J8 | DQC0_17 |
| J9 | VSS |
| J11 | DDBIB1_1 |
| J12 | DQB1_8 |
| J14 | VMEMIO |
| J15 | MAB1_5 |
| J17 | DDBIB1_0 |
| J18 | VMEMIO |
| J19 | EDCB0_1 |
| J20 | DQB0_9 |
| J21 | VSS |
| J23 | VMEMIO |
| J24 | DQB0_4 |
| J25 | WEB0B |
| J26 | VMEMIO |
| J27 | MAB0_9 |
| J29 | DQA1_25 |
| J30 | VMEMIO |
| J32 | MAA1_2 |
| J33 | MAA1_8 |
| J35 | VSS |
| J36 | ADBIA1 |
| J37 | DQA0_27 |
| J38 | VSS |
| J39 | DQA0_26 |
| J40 | DQA0_25 |
| J41 | VSS |

| Ball Reference | Signal Name |
|---|---|
| J42 | DQA0_9 |
| J43 | DQA0_8 |
| K12 | CSB1B_0 |
| K14 | MAB1_9 |
| K15 | VSS |
| K17 | MAB1_1 |
| K18 | MAB1_7 |
| K19 | VSS |
| K20 | RASB0B |
| K21 | CASB0B |
| K23 | MAB0_8 |
| K24 | MAB0_2 |
| K25 | VSS |
| K26 | DQB0_0 |
| K27 | VSS |
| K29 | VSS |
| K30 | MAA1_4 |
| K32 | MAA1_3 |
| L1 | VSS |
| L2 | DQC0_10 |
| L3 | DQC0_9 |
| L4 | VSS |
| L5 | DQC0_22 |
| L6 | DQC0_21 |
| L7 | VSS |
| L8 | DQC0_20 |
| L9 | DDBIC0_2 |
| L11 | VSS |
| L12 | VSS |
| L14 | VSS |
| L15 | MAB1_4 |
| L17 | VMEMIO |
| L18 | MAB1_8 |
| L19 | ADBIB1 |
| L20 | VMEMIO |
| L21 | ADBIB0 |
| L23 | MAB0_7 |
| L24 | VMEMIO |
| L25 | MAB0_4 |
| L26 | CSB0B_0 |
| L27 | VMEMIO |
| L29 | CLKA1B |

| Ball Reference | Signal Name |
|---|---|
| L30 | MAA1_5 |
| L32 | VSS |
| L33 | MAA1_7 |
| L35 | CASA1B |
| L36 | DQA0_24 |
| L37 | VMEMIO |
| L38 | WCKA0B_1 |
| L39 | WCKA0_1 |
| L40 | VSS |
| L41 | WCKA0B_0 |
| L42 | WCKA0_0 |
| L43 | VSS |
| M1 | EDCC0_1 |
| M2 | VSS |
| M3 | DDBIC0_1 |
| M4 | DQC0_11 |
| M5 | VMEMIO |
| M6 | WCKC0_1 |
| M7 | WCKC0B_1 |
| M8 | VSS |
| M9 | DQC0_23 |
| M10 | CSC0B_0 |
| M11 | VSS |
| M12 | VMEMIO |
| M14 | DRAM_RSTB |
| M15 | WEB1B |
| M17 | MAB1_3 |
| M18 | VSS |
| M19 | CASB1B |
| M20 | RASB1B |
| M21 | VSS |
| M23 | VSS |
| M24 | MAB0_3 |
| M25 | MAB0_5 |
| M26 | VSS |
| M27 | CSA1B_0 |
| M29 | CLKA1 |
| M30 | VSS |
| M32 | MAA1_1 |
| M33 | VSS |
| M34 | CKEA1 |
| M35 | RASA1B |

| Ball Reference | Signal Name |
|---|---|
| M36 | VSS |
| M37 | DQA0_23 |
| M38 | DQA0_22 |
| M39 | VMEMIO |
| M40 | DQA0_7 |
| M41 | DQA0_6 |
| M42 | VSS |
| M43 | DQA0_5 |
| N15 | VMEMIO |
| N17 | MAB1_2 |
| N18 | MAB1_0 |
| N19 | VMEMIO |
| N20 | CKEB1 |
| N21 | CKEB0 |
| N23 | MAB0_6 |
| N24 | MAB0_1 |
| N25 | VMEMIO |
| N26 | CLKB0B |
| N27 | MAA1_9 |
| N29 | VMEMIO |
| P1 | DQC0_13 |
| P2 | DQC0_12 |
| P3 | VSS |
| P4 | DQC0_25 |
| P5 | DQC0_24 |
| P6 | VSS |
| P7 | CLKC0B |
| P8 | CLKC0 |
| P9 | VSS |
| P10 | MAC0_9 |
| P11 | VSS |
| P12 | DRAM_RSTC |
| P14 | VMEMIO |
| P15 | MEM_CALRB |
| P17 | VSS |
| P18 | VSS |
| P19 | MAB1_6 |
| P20 | MVREFDB |
| P21 | VDDCI |
| P23 | VDDCI |
| P24 | VSS |
| P25 | MVREFDA |

| Ball Reference | Signal Name |
|---|---|
| P26 | CLKB0 |
| P27 | VSS |
| P29 | VSS |
| P30 | VMEMIO |
| P32 | VSS |
| P33 | RASA0B |
| P34 | CKEA0 |
| P35 | VMEMIO |
| P36 | ADBIA0 |
| P37 | DQA0_21 |
| P38 | VSS |
| P39 | DQA0_20 |
| P40 | DDBIA0_2 |
| P41 | VSS |
| P42 | DQA0_4 |
| P43 | DDBIA0_0 |
| R1 | VSS |
| R2 | DQC0_15 |
| R3 | DQC0_14 |
| R4 | VSS |
| R5 | EDCC0_3 |
| R6 | DQC0_27 |
| R7 | VMEMIO |
| R8 | DQC0_26 |
| R9 | MAC0_5 |
| R10 | VSS |
| R11 | MAC0_4 |
| R12 | WEC0B |
| R13 | VMEMIO |
| R14 | MEM_CALRC |
| R15 | VSS |
| R16 | VDDCI |
| R17 | VSS |
| R18 | VDDCI |
| R19 | VDDCI |
| R20 | VDDCI |
| R21 | VSS |
| R22 | VSS |
| R23 | VSS |
| R24 | VDDCI |
| R25 | VDDCI |
| R26 | VDDCI |

| Ball Reference | Signal Name |
|---|---|
| R27 | VSS |
| R28 | VDDCI |
| R29 | VSS |
| R30 | VSS |
| R31 | VMEMIO |
| R32 | CASA0B |
| R33 | MAA0_6 |
| R34 | VSS |
| R35 | MAA0_7 |
| R36 | DQA0_19 |
| R37 | VMEMIO |
| R38 | DQA0_18 |
| R39 | EDCA0_2 |
| R40 | VSS |
| R41 | EDCA0_0 |
| R42 | DQA0_3 |
| R43 | VSS |
| T15 | VDDCI |
| T16 | VDDC |
| T17 | VDDC |
| T18 | VSS |
| T19 | VSS |
| T20 | VDDC |
| T21 | VDDC |
| T22 | VSS |
| T23 | VSS |
| T24 | VDDC |
| T25 | VDDC |
| T26 | VSS |
| T27 | VDDCI |
| T28 | VSS |
| T29 | VDDCI |
| U1 | DQC1_10 |
| U2 | VSS |
| U3 | DQC1_9 |
| U4 | DQC1_8 |
| U5 | VMEMIO |
| U6 | DQC0_29 |
| U7 | DQC0_28 |
| U8 | VSS |
| U9 | DDBIC0_3 |
| U10 | MAC0_1 |

| Ball Reference | Signal Name |
|---|---|
| U11 | VMEMIO |
| U12 | MAC0_3 |
| U13 | MAC0_2 |
| U14 | VSS |
| U15 | VSS |
| U16 | VDDC |
| U17 | VDDC |
| U18 | VSS |
| U19 | VSS |
| U20 | VDDC |
| U21 | VDDC |
| U22 | VSS |
| U23 | VSS |
| U24 | VDDC |
| U25 | VDDC |
| U26 | VSS |
| U27 | VSS |
| U28 | VDDCI |
| U29 | VSS |
| U30 | VSS |
| U31 | MAA0_8 |
| U32 | MAA0_0 |
| U33 | VMEMIO |
| U34 | MAA0_1 |
| U35 | MAA0_3 |
| U36 | VSS |
| U37 | DQA0_17 |
| U38 | DQA0_16 |
| U39 | VMEMIO |
| U40 | DQA0_2 |
| U41 | DQA0_1 |
| U42 | VSS |
| U43 | DQA0_0 |
| V1 | EDCC1_1 |
| V2 | DQC1_11 |
| V3 | VSS |
| V4 | DQC1_16 |
| V5 | DQC1_17 |
| V6 | VSS |
| V7 | DQC0_31 |
| V8 | DQC0_30 |
| V9 | VMEMIO |

| Ball Reference | Signal Name |
|---|---|
| V10 | MAC0_7 |
| V11 | MAC0_8 |
| V12 | VSS |
| V13 | MAC0_0 |
| V14 | TEST6 |
| V15 | VDDCI |
| V16 | VDDC |
| V17 | VDDC |
| V18 | VSS |
| V19 | VSS |
| V20 | VDDC |
| V21 | VDDC |
| V22 | VSS |
| V23 | VSS |
| V24 | VDDC |
| V25 | VDDC |
| V26 | VSS |
| V27 | VSS |
| V28 | VDDC |
| V29 | VDDCI |
| V30 | VSS |
| V31 | MAA0_2 |
| V32 | VSS |
| V33 | MAA0_5 |
| V34 | WEA0B |
| V35 | VMEMIO |
| V36 | MAA0_4 |
| V37 | VSS |
| V38 | GPIO_1 |
| V39 | GPIO_0 |
| V40 | PX_EN |
| V41 | GPIO_13 |
| V42 | GPIO_12 |
| V43 | GPIO_11 |
| W1 | VSS |
| W2 | DQC1_12 |
| W3 | DDBIC1_1 |
| W4 | VSS |
| W5 | DQC1_19 |
| W6 | DQC1_18 |
| W7 | VMEMIO |
| W8 | DDBIC1_2 |

| Ball Reference | Signal Name |
|---|---|
| W9 | EDCC1_2 |
| W10 | VSS |
| W11 | ADBIC0 |
| W12 | CASC0B |
| W13 | VMEMIO |
| W14 | MAC0_6 |
| W15 | VDDCI |
| W16 | VDDC |
| W17 | VDDC |
| W18 | VSS |
| W19 | VSS |
| W20 | VDDC |
| W21 | VDDC |
| W22 | VSS |
| W23 | VSS |
| W24 | VDDC |
| W25 | VDDC |
| W26 | VSS |
| W27 | VSS |
| W28 | VDDC |
| W29 | VDDC |
| W30 | DRAM_RSTA |
| W31 | VMEMIO |
| W32 | CLKA0 |
| W33 | CLKA0B |
| W34 | VSS |
| W35 | MAA0_9 |
| W36 | VSS |
| W37 | GPIO_2 |
| W38 | VSS |
| W39 | VSS |
| W40 | VSS |
| W41 | VSS |
| W42 | PCIE_RX15P |
| W43 | PCIE_RX15N |
| Y1 | DQC1_14 |
| Y2 | VSS |
| Y3 | DQC1_15 |
| Y4 | DQC1_13 |
| Y5 | VSS |
| Y6 | DQC1_20 |
| Y7 | DQC1_21 |

| Ball Reference | Signal Name |
|---|---|
| Y8 | VSS |
| Y9 | DQC1_22 |
| Y10 | RASC1B |
| Y11 | VMEMIO |
| Y12 | RASC0B |
| Y13 | CKEC0 |
| Y14 | MVREFDC |
| Y15 | VDDCI |
| Y16 | VDDC |
| Y17 | VDDC |
| Y18 | VSS |
| Y19 | VSS |
| Y20 | VDDC |
| Y21 | VDDC |
| Y22 | VSS |
| Y23 | VSS |
| Y24 | VDDC |
| Y25 | VDDC |
| Y26 | VSS |
| Y27 | VSS |
| Y28 | VDDC |
| Y29 | VDDC |
| Y30 | VSS |
| Y31 | MEM_CALRA |
| Y32 | TEST_PG_BACO |
| Y33 | VMEMIO |
| Y34 | CSA0B_0 |
| Y35 | VSS |
| Y36 | VSS |
| Y37 | VSS |
| Y38 | PCIE_TX15P |
| Y39 | PCIE_TX15N |
| Y40 | VSS |
| Y41 | PCIE_RX13N |
| Y42 | PCIE_RX14N |
| Y43 | PCIE_RX14P |
| AA1 | WCKC1_0 |
| AA2 | WCKC1B_0 |
| AA3 | VSS |
| AA4 | DQC1_0 |
| AA5 | DQC1_23 |
| AA6 | VSS |

| Ball Reference | Signal Name |
|---|---|
| AA7 | WCKC1_1 |
| AA8 | WCKC1B_1 |
| AA9 | VSS |
| AA10 | CASC1B |
| AA11 | ADBIC1 |
| AA12 | VSS |
| AA13 | CKEC1 |
| AA14 | VDDCI |
| AA15 | VSS |
| AA16 | VDDC |
| AA17 | VDDC |
| AA18 | VSS |
| AA19 | VSS |
| AA20 | VDDC |
| AA21 | VDDC |
| AA22 | VSS |
| AA23 | VSS |
| AA24 | VDDC |
| AA25 | VDDC |
| AA26 | VSS |
| AA27 | VSS |
| AA28 | VDDC |
| AA29 | VDDC |
| AA30 | TS_A |
| AA31 | TEST_PG |
| AA32 | VSS |
| AA33 | VSS |
| AA34 | VDD_08 |
| AA35 | VDD_08 |
| AA36 | VSS |
| AA37 | PCIE_TX13N |
| AA38 | PCIE_TX14N |
| AA39 | PCIE_TX14P |
| AA40 | VSS |
| AA41 | PCIE_RX13P |
| AA42 | PCIE_RX12P |
| AA43 | PCIE_RX12N |
| AB15 | VSS |
| AB16 | VDDC |
| AB17 | VDDC |
| AB18 | VSS |
| AB19 | VSS |

| Ball Reference | Signal Name |
|---|---|
| AB20 | VDDC |
| AB21 | VDDC |
| AB22 | VSS |
| AB23 | VSS |
| AB24 | VDDC |
| AB25 | VDDC |
| AB26 | VSS |
| AB27 | VSS |
| AB28 | VDDC |
| AB29 | VDDC |
| AC1 | DQC1_2 |
| AC2 | DQC1_1 |
| AC3 | VSS |
| AC4 | DQC1_26 |
| AC5 | DQC1_25 |
| AC6 | VSS |
| AC7 | DQC1_24 |
| AC8 | MAC1_0 |
| AC9 | VMEMIO |
| AC10 | MAC1_8 |
| AC11 | MAC1_7 |
| AC12 | VSS |
| AC13 | MAC1_6 |
| AC14 | VDDCI |
| AC15 | VSS |
| AC16 | VDDC |
| AC17 | VDDC |
| AC18 | VSS |
| AC19 | VSS |
| AC20 | VDDC |
| AC21 | VDDC |
| AC22 | VSS |
| AC23 | VSS |
| AC24 | VDDC |
| AC25 | VDDC |
| AC26 | VSS |
| AC27 | VSS |
| AC28 | VDDC |
| AC29 | VDDC |
| AC30 | JTAG_TRSTB |
| AC31 | GPIO_19_CTF |
| AC32 | VSS |

| Ball Reference | Signal Name |
|---|---|
| AC33 | VSS |
| AC34 | DMINUS |
| AC35 | DPLUS |
| AC36 | VSS |
| AC37 | PCIE_TX13P |
| AC38 | PCIE_TX12P |
| AC39 | PCIE_TX12N |
| AC40 | VSS |
| AC41 | VSS |
| AC42 | PCIE_RX11N |
| AC43 | PCIE_RX11P |
| AD1 | DQC1_3 |
| AD2 | VSS |
| AD3 | DDBIC1_0 |
| AD4 | EDCC1_0 |
| AD5 | VSS |
| AD6 | EDCC1_3 |
| AD7 | DDBIC1_3 |
| AD8 | VSS |
| AD9 | DQC1_27 |
| AD10 | MAC1_2 |
| AD11 | VMEMIO |
| AD12 | MAC1_3 |
| AD13 | MAC1_1 |
| AD14 | VSS |
| AD15 | VDDCI |
| AD16 | VDDC |
| AD17 | VDDC |
| AD18 | VSS |
| AD19 | VSS |
| AD20 | VDDC |
| AD21 | VDDC |
| AD22 | VSS |
| AD23 | VSS |
| AD24 | VDDC |
| AD25 | VDDC |
| AD26 | VSS |
| AD27 | VSS |
| AD28 | VDDC |
| AD29 | VDDC |
| AD30 | JTAG_TDI |
| AD31 | JTAG_TDO |

| Ball Reference | Signal Name |
|---|---|
| AD32 | VSS |
| AD33 | DDCVGADATA |
| AD34 | DDCVGACLK |
| AD35 | VSS |
| AD36 | VDD_08 |
| AD37 | VSS |
| AD38 | PCIE_TX11N |
| AD39 | PCIE_TX11P |
| AD40 | VSS |
| AD41 | PCIE_RX9N |
| AD42 | PCIE_RX10N |
| AD43 | PCIE_RX10P |
| AE1 | VSS |
| AE2 | DQC1_5 |
| AE3 | DQC1_4 |
| AE4 | VSS |
| AE5 | DQC1_30 |
| AE6 | DQC1_29 |
| AE7 | VMEMIO |
| AE8 | DQC1_28 |
| AE9 | WEC1B |
| AE10 | VSS |
| AE11 | MAC1_4 |
| AE12 | MAC1_5 |
| AE13 | VMEMIO |
| AE14 | MVREFDD |
| AE15 | VDDCI |
| AE16 | VDDC |
| AE17 | VDDC |
| AE18 | VSS |
| AE19 | VSS |
| AE20 | VDDC |
| AE21 | VDDC |
| AE22 | VSS |
| AE23 | VSS |
| AE24 | VDDC |
| AE25 | VDDC |
| AE26 | VSS |
| AE27 | VSS |
| AE28 | VDDC |
| AE29 | VDDC |
| AE30 | TESTEN |

| Ball Reference | Signal Name |
|---|---|
| AE31 | JTAG_TMS |
| AE32 | VSS |
| AE33 | GPIO_17_THERMAL_INT |
| AE34 | GPIO_6_TACH |
| AE35 | VDD_08 |
| AE36 | VSS |
| AE37 | PCIE_TX9N |
| AE38 | PCIE_TX10N |
| AE39 | PCIE_TX10P |
| AE40 | VSS |
| AE41 | PCIE_RX9P |
| AE42 | PCIE_RX8P |
| AE43 | PCIE_RX8N |
| AF1 | DQC1_7 |
| AF2 | DQC1_6 |
| AF3 | VSS |
| AF4 | DQD0_2 |
| AF5 | DQD0_1 |
| AF6 | VSS |
| AF7 | DQD0_0 |
| AF8 | VSS |
| AF9 | VMEMIO |
| AF10 | DQC1_31 |
| AF11 | CSC1B_0 |
| AF12 | VSS |
| AF13 | CLKC1B |
| AF14 | CLKC1 |
| AF15 | VDDCI |
| AF16 | VDDC |
| AF17 | VDDC |
| AF18 | VSS |
| AF19 | VSS |
| AF20 | VDDC |
| AF21 | VDDC |
| AF22 | VSS |
| AF23 | VSS |
| AF24 | VDDC |
| AF25 | VDDC |
| AF26 | VSS |
| AF27 | VSS |
| AF28 | VDDC |
| AF29 | VDDC |

| Ball Reference | Signal Name |
|---|---|
| AF30 | JTAG_TCK |
| AF31 | GPIO_28_FDO |
| AF32 | VSS |
| AF33 | SDA |
| AF34 | SCL |
| AF35 | VDD_08 |
| AF36 | VSS |
| AF37 | PCIE_TX9P |
| AF38 | PCIE_TX8P |
| AF39 | PCIE_TX8N |
| AF40 | VSS |
| AF41 | VSS |
| AF42 | PCIE_RX7N |
| AF43 | PCIE_RX7P |
| AG1 | DQD0_16 |
| AG2 | VSS |
| AG3 | DQD0_17 |
| AG4 | DQD0_18 |
| AG5 | VMEMIO |
| AG6 | DQD0_3 |
| AG7 | EDCD0_0 |
| AG8 | VSS |
| AG9 | MAC1_9 |
| AG10 | VSS |
| AG11 | VMEMIO |
| AG12 | CSD0B_0 |
| AG13 | MAD0_9 |
| AG14 | VSS |
| AG15 | VSS |
| AG16 | VDDCI |
| AG17 | VDDC |
| AG18 | VSS |
| AG19 | VSS |
| AG20 | VDDC |
| AG21 | VDDC |
| AG22 | VSS |
| AG23 | VSS |
| AG24 | VDDC |
| AG25 | VDDC |
| AG26 | VSS |
| AG27 | VSS |
| AG28 | VDDC |

| Ball Reference | Signal Name |
|---|---|
| AG29 | VDDC |
| AG30 | GPIO_30 |
| AG31 | GPIO_29 |
| AG32 | VSS |
| AG33 | TEMPIN0 |
| AG34 | TEMPINRETURN |
| AG35 | VSS |
| AG36 | VDD_08 |
| AG37 | VSS |
| AG38 | PCIE_TX7N |
| AG39 | PCIE_TX7P |
| AG40 | VSS |
| AG41 | PCIE_RX5N |
| AG42 | PCIE_RX6N |
| AG43 | PCIE_RX6P |
| AH15 | VDDCI |
| AH16 | VSS |
| AH17 | VDDCI |
| AH18 | VDDC |
| AH19 | VDDC |
| AH20 | VDDC |
| AH21 | VDDC |
| AH22 | VDDC |
| AH23 | VDDC |
| AH24 | VDDC |
| AH25 | VDDC |
| AH26 | VDDC |
| AH27 | VDDC |
| AH28 | VDDC |
| AH29 | VDDC |
| AJ1 | VSS |
| AJ2 | DQD0_19 |
| AJ3 | EDCD0_2 |
| AJ4 | VSS |
| AJ5 | DQD0_5 |
| AJ6 | DQD0_4 |
| AJ7 | VMEMIO |
| AJ8 | DDBID0_0 |
| AJ9 | DQD0_6 |
| AJ10 | VSS |
| AJ11 | CLKD0B |
| AJ12 | CLKD0 |

| Ball Reference | Signal Name |
|---|---|
| AJ13 | VMEMIO |
| AJ14 | VSS |
| AJ15 | VSS |
| AJ16 | VDDCI |
| AJ17 | VSS |
| AJ18 | VDDCI |
| AJ19 | VDDC |
| AJ20 | VDDC |
| AJ21 | VDDC |
| AJ22 | VDDC |
| AJ23 | VDDC |
| AJ24 | VDDC |
| AJ25 | VDDC |
| AJ26 | VDDC |
| AJ27 | VDDC |
| AJ28 | VDDC |
| AJ29 | VSS |
| AJ30 | VDD_08 |
| AJ31 | GPIO_15 |
| AJ32 | VSS |
| AJ33 | GPIO_16_8P_DETECT |
| AJ34 | GPIO_5_REG_HOT_AC_BATT |
| AJ35 | VDD_08 |
| AJ36 | VSS |
| AJ37 | PCIE_TX5N |
| AJ38 | PCIE_TX6N |
| AJ39 | PCIE_TX6P |
| AJ40 | VSS |
| AJ41 | PCIE_RX5P |
| AJ42 | PCIE_RX4P |
| AJ43 | PCIE_RX4N |
| AK1 | DDBID0_2 |
| AK2 | DQD0_20 |
| AK3 | VSS |
| AK4 | WCKD0_0 |
| AK5 | WCKD0B_0 |
| AK6 | VSS |
| AK7 | DQD0_7 |
| AK8 | WED0B |
| AK9 | VMEMIO |
| AK10 | MAD0_4 |
| AK11 | MAD0_5 |

| Ball Reference | Signal Name |
|---|---|
| AK12 | VSS |
| AK14 | VMEMIO |
| AK15 | VSS |
| AK17 | VSS |
| AK18 | VSS |
| AK19 | DRAM_RSTD |
| AK20 | VSS |
| AK21 | FB_VSS |
| AK23 | FB_VDDCI |
| AK24 | VSS |
| AK25 | DIGON |
| AK26 | BL_ENABLE |
| AK27 | VSS |
| AK29 | VSS |
| AK30 | PCIE_ZVSS |
| AK32 | VSS |
| AK33 | GPIO_20 |
| AK34 | GPIO_21 |
| AK35 | VDD_08 |
| AK36 | VSS |
| AK37 | PCIE_TX5P |
| AK38 | PCIE_TX4P |
| AK39 | PCIE_TX4N |
| AK40 | VSS |
| AK41 | VSS |
| AK42 | PCIE_RX3N |
| AK43 | PCIE_RX3P |
| AL15 | VMEMIO |
| AL17 | MAD1_8 |
| AL18 | MAD1_2 |
| AL19 | VMEMIO |
| AL20 | MEM_CALRD |
| AL21 | FB_VDDC |
| AL23 | VSS |
| AL24 | VDD_33 |
| AL25 | VSS |
| AL26 | BL_PWM_DIM |
| AL27 | GENLK_VSYNC |
| AL29 | VSS |
| AM1 | DQD0_23 |
| AM2 | VSS |
| AM3 | DQD0_22 |

| Ball Reference | Signal Name |
|---|---|
| AM4 | DQD0_21 |
| AM5 | VMEMIO |
| AM6 | DQD0_9 |
| AM7 | DQD0_8 |
| AM8 | VSS |
| AM9 | MAD0_2 |
| AM10 | MAD0_3 |
| AM11 | VSS |
| AM12 | MAD0_1 |
| AM14 | VSS |
| AM15 | CASD1B |
| AM17 | MAD1_0 |
| AM18 | VSS |
| AM19 | CLKD1 |
| AM20 | DRAIN |
| AM21 | GATE |
| AM23 | GPIO_SVC |
| AM24 | VDD_33 |
| AM25 | VDD_18 |
| AM26 | VSS |
| AM27 | GENLK_CLK |
| AM29 | PLLCHARZ_H |
| AM30 | GPIO_10_ROMSCK |
| AM32 | VSS |
| AM33 | SMBDAT |
| AM34 | SMBCLK |
| AM35 | VSS |
| AM36 | VDD_08 |
| AM37 | VSS |
| AM38 | PCIE_TX3N |
| AM39 | PCIE_TX3P |
| AM40 | VSS |
| AM41 | PCIE_RX1N |
| AM42 | PCIE_RX2N |
| AM43 | PCIE_RX2P |
| AN1 | VSS |
| AN2 | WCKD0_1 |
| AN3 | WCKD0B_1 |
| AN4 | VSS |
| AN5 | DQD0_11 |
| AN6 | DQD0_10 |
| AN7 | VMEMIO |

| Ball Reference | Signal Name |
|---|---|
| AN8 | MAD0_0 |
| AN9 | MAD0_8 |
| AN11 | MAD0_7 |
| AN12 | VSS |
| AN14 | RASD1B |
| AN15 | MAD1_6 |
| AN17 | VMEMIO |
| AN18 | MAD1_5 |
| AN19 | CLKD1B |
| AN20 | VMEMIO |
| AN21 | DBGDATA_10 |
| AN23 | GPIO_SVT |
| AN24 | VSS |
| AN25 | VDD_18 |
| AN26 | VDD_18 |
| AN27 | VSS |
| AN29 | PLLCHARZ_L |
| AN30 | GPIO_8_ROMSO |
| AN32 | GPIO_22_ROMCSB |
| AN33 | VSS |
| AN35 | VDD_08 |
| AN36 | VSS |
| AN37 | PCIE_TX1N |
| AN38 | PCIE_TX2N |
| AN39 | PCIE_TX2P |
| AN40 | VSS |
| AN41 | PCIE_RX1P |
| AN42 | PCIE_RX0P |
| AN43 | PCIE_RX0N |
| AP12 | CKED0 |
| AP14 | CKED1 |
| AP15 | VSS |
| AP17 | MAD1_1 |
| AP18 | WED1B |
| AP19 | VSS |
| AP20 | CSD1B_0 |
| AP21 | DBGDATA_11 |
| AP23 | GPIO_SVD |
| AP24 | HSYNC |
| AP25 | VSS |
| AP26 | VDD_18 |
| AP27 | VDD_18 |

| Ball Reference | Signal Name |
|---|---|
| AP29 | VSS |
| AP30 | VSS |
| AP32 | GPIO_9_ROMSI |
| AR1 | DQD0_24 |
| AR2 | DQD0_25 |
| AR3 | VSS |
| AR4 | EDCD0_1 |
| AR5 | DDBID0_1 |
| AR6 | VSS |
| AR7 | DQD0_12 |
| AR8 | MAD0_6 |
| AR9 | VSS |
| AR11 | CASD0B |
| AR12 | RASD0B |
| AR14 | VMEMIO |
| AR15 | MAD1_7 |
| AR17 | MAD1_3 |
| AR18 | VMEMIO |
| AR19 | MAD1_9 |
| AR20 | DBGDATA_5 |
| AR21 | DBGDATA_15 |
| AR23 | DDC1DATA |
| AR24 | VSYNC |
| AR25 | SWAPLOCKB |
| AR26 | TSVDD |
| AR27 | VDD_18 |
| AR29 | GPIO_14_HPD2 |
| AR30 | GENERICD |
| AR32 | VSS |
| AR33 | VSS |
| AR35 | VSS |
| AR36 | VSS |
| AR37 | PCIE_TX1P |
| AR38 | PCIE_TX0P |
| AR39 | PCIE_TX0N |
| AR40 | VSS |
| AR41 | VSS |
| AR42 | PCIE_REFCLKP |
| AR43 | PCIE_REFCLKN |
| AT1 | DQD0_26 |
| AT2 | VSS |
| AT3 | DQD0_27 |

| Ball Reference | Signal Name |
|---|---|
| AT4 | DDBID0_3 |
| AT5 | VSS |
| AT6 | DQD0_13 |
| AT8 | DQD0_14 |
| AT9 | ADBID0 |
| AT11 | DQD1_7 |
| AT12 | VSS |
| AT14 | ADBID1 |
| AT15 | DQD1_12 |
| AT17 | VSS |
| AT18 | MAD1_4 |
| AT19 | DBGDATA_2 |
| AT20 | DBGDATA_6 |
| AT21 | VSS |
| AT23 | DDC1CLK |
| AT24 | GENERICB |
| AT25 | SWAPLOCKA |
| AT26 | VSS |
| AT27 | VSS |
| AT29 | GPIO_18_HPD3 |
| AT30 | GENERICC |
| AT32 | HPD1 |
| AT33 | DDCAUX4N |
| AT35 | VSS |
| AT36 | DP_ZVDD_08 |
| AT38 | VSS |
| AT39 | VSS |
| AT40 | VSS |
| AT41 | VSS |
| AT42 | VSS |
| AT43 | VSS |
| AU9 | DQD1_4 |
| AU11 | VMEMIO |
| AU12 | DQD1_8 |
| AU14 | DQD1_10 |
| AU15 | VMEMIO |
| AU17 | DQD1_14 |
| AU18 | VSS |
| AU19 | VSS |
| AU20 | DBGDATA_9 |
| AU21 | DBGDATA_14 |
| AU23 | VSS |

| Ball Reference | Signal Name |
|---|---|
| AU24 | VSS |
| AU25 | VSS |
| AU26 | DDC2CLK |
| AU27 | DDCAUX3P |
| AU29 | GENERICE_HPD4 |
| AU30 | GENERICF_HPD5 |
| AU32 | GENERICG_HPD6 |
| AU33 | DDCAUX4P |
| AU35 | DDCAUX5P |
| AV1 | VSS |
| AV2 | EDCD0_3 |
| AV3 | DQD0_28 |
| AV4 | VSS |
| AV5 | DQD0_15 |
| AV6 | VSS |
| AV8 | EDCD1_0 |
| AV9 | VSS |
| AV11 | WCKD1B_0 |
| AV12 | DQD1_9 |
| AV14 | VSS |
| AV15 | DQD1_13 |
| AV17 | DQD1_15 |
| AV18 | DBGDATA_0 |
| AV19 | DBGDATA_3 |
| AV20 | VSS |
| AV21 | DBGDATA_13 |
| AV23 | AUX1P |
| AV24 | BP_1 |
| AV25 | AUX2P |
| AV26 | DDC2DATA |
| AV27 | DDCAUX3N |
| AV29 | VSS |
| AV30 | VSS |
| AV32 | VSS |
| AV33 | VSS |
| AV35 | DDCAUX5N |
| AV36 | DP_ZVSS |
| AV38 | VSS |
| AV39 | VSS |
| AV40 | VSS |
| AV41 | CLKREQB |
| AV42 | PERSTB |

| Ball Reference | Signal Name |
|---|---|
| AV43 | WAKEB |
| AW1 | DQD0_29 |
| AW2 | VSS |
| AW3 | DQD1_0 |
| AW4 | DQD1_1 |
| AW5 | VSS |
| AW6 | DDBID1_0 |
| AW8 | VSS |
| AW9 | DQD1_5 |
| AW11 | WCKD1_0 |
| AW12 | VMEMIO |
| AW14 | DQD1_11 |
| AW15 | EDCD1_1 |
| AW17 | VMEMIO |
| AW18 | DBGDATA_1 |
| AW19 | DBGDATA_4 |
| AW20 | DBGDATA_8 |
| AW21 | DBGDATA_12 |
| AW23 | AUX1N |
| AW24 | BP_0 |
| AW25 | AUX2N |
| AW26 | VSS |
| AW27 | VSS |
| AW29 | VSS |
| AW30 | VSS |
| AW32 | VSS |
| AW33 | VSS |
| AW35 | VSS |
| AW36 | VSS |
| AW38 | VSS |
| AW39 | VSS |
| AW40 | GENERICA |
| AW41 | VSS |
| AW42 | ANALOGIO |
| AW43 | VSS |
| AY2 | DQD0_30 |
| AY3 | VSS |
| AY5 | DQD1_3 |
| AY6 | VSS |
| AY8 | DDBID1_2 |
| AY9 | DQD1_6 |
| AY11 | VSS |

| Ball Reference | Signal Name |
|---|---|
| AY12 | DQD1_24 |
| AY14 | DDBID1_1 |
| AY15 | VSS |
| AY17 | DQD1_29 |
| AY18 | VSS |
| AY19 | VSS |
| AY20 | DBGDATA_7 |
| AY21 | TXCEM_DPE3N |
| AY23 | TXCEP_DPE3P |
| AY24 | AUX_ZVSS |
| AY25 | VSS |
| AY26 | TX1M_DPD1N |
| AY27 | TX1P_DPD1P |
| AY29 | TX3M_DPC2N |
| AY30 | TX3P_DPC2P |
| AY32 | TXCBM_DPB3N |
| AY33 | TXCBP_DPB3P |
| AY35 | TX2M_DPB0N |
| AY36 | TX2P_DPB0P |
| AY38 | TX4M_DPA1N |
| AY39 | TX4P_DPA1P |
| AY41 | VSS |
| AY42 | XTALOUT |
| BA1 | DQD0_31 |
| BA4 | VSS |
| BA5 | DQD1_2 |
| BA6 | DQD1_19 |
| BA8 | DQD1_20 |
| BA9 | VSS |
| BA11 | WCKD1B_1 |
| BA12 | DQD1_25 |
| BA14 | VSS |
| BA15 | EDCD1_3 |
| BA17 | DQD1_30 |
| BA18 | VSS |
| BA19 | TX0M_DPF2N |
| BA20 | TX0P_DPF2P |
| BA21 | VSS |
| BA23 | VSS |
| BA24 | TX5M_DPE0N |
| BA25 | TX5P_DPE0P |
| BA26 | VSS |

| Ball Reference | Signal Name |
|---|---|
| BA27 | VSS |
| BA29 | VSS |
| BA30 | VSS |
| BA32 | VSS |
| BA33 | VSS |
| BA35 | VSS |
| BA36 | VSS |
| BA38 | VSS |
| BA39 | VSS |
| BA40 | VSS |
| BA43 | XTALIN |
| BB1 | VSS |
| BB2 | VSS |
| BB4 | DQD1_16 |
| BB5 | VSS |
| BB6 | EDCD1_2 |
| BB8 | VSS |
| BB9 | DQD1_22 |
| BB11 | WCKD1_1 |
| BB12 | VSS |
| BB14 | DQD1_27 |
| BB15 | DQD1_28 |
| BB17 | VSS |
| BB18 | VSS |
| BB19 | TXCFM_DPF3N |
| BB20 | TX1P_DPF1P |
| BB21 | TX2M_DPF0N |
| BB23 | TX3P_DPE2P |
| BB24 | TX4M_DPE1N |
| BB25 | TXCDP_DPD3P |
| BB26 | TX0M_DPD2N |
| BB27 | TX2P_DPD0P |
| BB29 | TXCCM_DPC3N |
| BB30 | TX4P_DPC1P |
| BB32 | TX5M_DPC0N |
| BB33 | TX0P_DPB2P |
| BB35 | TX1M_DPB1N |
| BB36 | TXCAP_DPA3P |
| BB38 | TX3M_DPA2N |
| BB39 | TX5P_DPA0P |
| BB40 | DDCAUX6N |
| BB42 | VSS |

| Ball Reference | Signal Name |
|---|---|
| BB43 | VSS |
| BC2 | VSS |
| BC3 | DQD1_17 |
| BC5 | DQD1_18 |
| BC6 | VSS |
| BC8 | DQD1_21 |
| BC9 | DQD1_23 |
| BC11 | VSS |
| BC12 | DQD1_26 |
| BC14 | DDBID1_3 |
| BC15 | VSS |
| BC17 | DQD1_31 |
| BC18 | VSS |
| BC19 | TXCFP_DPF3P |
| BC20 | TX1M_DPF1N |
| BC21 | TX2P_DPF0P |
| BC23 | TX3M_DPE2N |
| BC24 | TX4P_DPE1P |
| BC25 | TXCDM_DPD3N |
| BC26 | TX0P_DPD2P |
| BC27 | TX2M_DPD0N |
| BC29 | TXCCP_DPC3P |
| BC30 | TX4M_DPC1N |
| BC32 | TX5P_DPC0P |
| BC33 | TX0M_DPB2N |
| BC35 | TX1P_DPB1P |
| BC36 | TXCAM_DPA3N |
| BC38 | TX3P_DPA2P |
| BC39 | TX5M_DPA0N |
| BC41 | DDCAUX6P |
| BC42 | VSS |

## A.2 Pins Sorted by Signal Name

Table A–2 "Polaris 20" Pins Sorted by Signal Name

| Signal Name | Ball Reference |
|---|---|
| ADBIA0 | P36 |
| ADBIA1 | J36 |
| ADBIB0 | L21 |
| ADBIB1 | L19 |
| ADBIC0 | W11 |

| Signal Name | Ball Reference |
|---|---|
| ADBIC1 | AA11 |
| ADBID0 | AT9 |
| ADBID1 | AT14 |
| ANALOGIO | AW42 |
| AUX1N | AW23 |
| AUX1P | AV23 |
| AUX2N | AW25 |
| AUX2P | AV25 |
| AUX_ZVSS | AY24 |
| BL_ENABLE | AK26 |
| BL_PWM_DIM | AL26 |
| BP_0 | AW24 |
| BP_1 | AV24 |
| CASA0B | R32 |
| CASA1B | L35 |
| CASB0B | K21 |
| CASB1B | M19 |
| CASC0B | W12 |
| CASC1B | AA10 |
| CASD0B | AR11 |
| CASD1B | AM15 |
| CKEA0 | P34 |
| CKEA1 | M34 |
| CKEB0 | N21 |
| CKEB1 | N20 |
| CKEC0 | Y13 |
| CKEC1 | AA13 |
| CKED0 | AP12 |
| CKED1 | AP14 |
| CLKA0 | W32 |
| CLKA0B | W33 |
| CLKA1 | M29 |
| CLKA1B | L29 |
| CLKB0 | P26 |
| CLKB0B | N26 |
| CLKB1 | H14 |
| CLKB1B | G14 |
| CLKC0 | P8 |
| CLKC0B | P7 |
| CLKC1 | AF14 |
| CLKC1B | AF13 |
| CLKD0 | AJ12 |

| Signal Name | Ball Reference |
|---|---|
| CLKD0B | AJ11 |
| CLKD1 | AM19 |
| CLKD1B | AN19 |
| CLKREQB | AV41 |
| CSA0B_0 | Y34 |
| CSA1B_0 | M27 |
| CSB0B_0 | L26 |
| CSB1B_0 | K12 |
| CSC0B_0 | M10 |
| CSC1B_0 | AF11 |
| CSD0B_0 | AG12 |
| CSD1B_0 | AP20 |
| DBGDATA_0 | AV18 |
| DBGDATA_1 | AW18 |
| DBGDATA_2 | AT19 |
| DBGDATA_3 | AV19 |
| DBGDATA_4 | AW19 |
| DBGDATA_5 | AR20 |
| DBGDATA_6 | AT20 |
| DBGDATA_7 | AY20 |
| DBGDATA_8 | AW20 |
| DBGDATA_9 | AU20 |
| DBGDATA_10 | AN21 |
| DBGDATA_11 | AP21 |
| DBGDATA_12 | AW21 |
| DBGDATA_13 | AV21 |
| DBGDATA_14 | AU21 |
| DBGDATA_15 | AR21 |
| DDBIA0_0 | P43 |
| DDBIA0_1 | H40 |
| DDBIA0_2 | P40 |
| DDBIA0_3 | F39 |
| DDBIA1_0 | D36 |
| DDBIA1_1 | A30 |
| DDBIA1_2 | E35 |
| DDBIA1_3 | H29 |
| DDBIB0_0 | G24 |
| DDBIB0_1 | H19 |
| DDBIB0_2 | C19 |
| DDBIB0_3 | C24 |
| DDBIB1_0 | J17 |
| DDBIB1_1 | J11 |

| Signal Name | Ball Reference |
|---|---|
| DDBIB1_2 | C12 |
| DDBIB1_3 | A5 |
| DDBIC0_0 | E1 |
| DDBIC0_1 | M3 |
| DDBIC0_2 | L9 |
| DDBIC0_3 | U9 |
| DDBIC1_0 | AD3 |
| DDBIC1_1 | W3 |
| DDBIC1_2 | W8 |
| DDBIC1_3 | AD7 |
| DDBID0_0 | AJ8 |
| DDBID0_1 | AR5 |
| DDBID0_2 | AK1 |
| DDBID0_3 | AT4 |
| DDBID1_0 | AW6 |
| DDBID1_1 | AY14 |
| DDBID1_2 | AY8 |
| DDBID1_3 | BC14 |
| DDC1CLK | AT23 |
| DDC1DATA | AR23 |
| DDC2CLK | AU26 |
| DDC2DATA | AV26 |
| DDCAUX3N | AV27 |
| DDCAUX3P | AU27 |
| DDCAUX4N | AT33 |
| DDCAUX4P | AU33 |
| DDCAUX5N | AV35 |
| DDCAUX5P | AU35 |
| DDCAUX6N | BB40 |
| DDCAUX6P | BC41 |
| DDCVGACLK | AD34 |
| DDCVGADATA | AD33 |
| DIGON | AK25 |
| DMINUS | AC34 |
| DPLUS | AC35 |
| DP_ZVDD_08 | AT36 |
| DP_ZVSS | AV36 |
| DQA0_0 | U43 |
| DQA0_1 | U41 |
| DQA0_2 | U40 |
| DQA0_3 | R42 |
| DQA0_4 | P42 |

| Signal Name | Ball Reference |
|---|---|
| DQA0_5 | M43 |
| DQA0_6 | M41 |
| DQA0_7 | M40 |
| DQA0_8 | J43 |
| DQA0_9 | J42 |
| DQA0_10 | H43 |
| DQA0_11 | H41 |
| DQA0_12 | F41 |
| DQA0_13 | E43 |
| DQA0_14 | C43 |
| DQA0_15 | D42 |
| DQA0_16 | U38 |
| DQA0_17 | U37 |
| DQA0_18 | R38 |
| DQA0_19 | R36 |
| DQA0_20 | P39 |
| DQA0_21 | P37 |
| DQA0_22 | M38 |
| DQA0_23 | M37 |
| DQA0_24 | L36 |
| DQA0_25 | J40 |
| DQA0_26 | J39 |
| DQA0_27 | J37 |
| DQA0_28 | E40 |
| DQA0_29 | E41 |
| DQA0_30 | D39 |
| DQA0_31 | C39 |
| DQA1_0 | A41 |
| DQA1_1 | B40 |
| DQA1_2 | A39 |
| DQA1_3 | C38 |
| DQA1_4 | C36 |
| DQA1_5 | A36 |
| DQA1_6 | B35 |
| DQA1_7 | A35 |
| DQA1_8 | A32 |
| DQA1_9 | C32 |
| DQA1_10 | D32 |
| DQA1_11 | B30 |
| DQA1_12 | B29 |
| DQA1_13 | D27 |
| DQA1_14 | C27 |

| Signal Name | Ball Reference |
|---|---|
| DQA1_15 | A27 |
| DQA1_16 | E38 |
| DQA1_17 | H36 |
| DQA1_18 | F36 |
| DQA1_19 | G35 |
| DQA1_20 | E33 |
| DQA1_21 | F33 |
| DQA1_22 | F32 |
| DQA1_23 | G32 |
| DQA1_24 | G30 |
| DQA1_25 | J29 |
| DQA1_26 | E29 |
| DQA1_27 | F29 |
| DQA1_28 | F27 |
| DQA1_29 | D26 |
| DQA1_30 | E26 |
| DQA1_31 | G26 |
| DQB0_0 | K26 |
| DQB0_1 | E25 |
| DQB0_2 | F25 |
| DQB0_3 | H25 |
| DQB0_4 | J24 |
| DQB0_5 | D23 |
| DQB0_6 | E23 |
| DQB0_7 | G23 |
| DQB0_8 | E21 |
| DQB0_9 | J20 |
| DQB0_10 | G20 |
| DQB0_11 | F20 |
| DQB0_12 | E19 |
| DQB0_13 | F19 |
| DQB0_14 | E18 |
| DQB0_15 | D18 |
| DQB0_16 | C20 |
| DQB0_17 | A20 |
| DQB0_18 | D20 |
| DQB0_19 | B19 |
| DQB0_20 | B18 |
| DQB0_21 | A17 |
| DQB0_22 | C17 |
| DQB0_23 | D17 |
| DQB0_24 | A26 |

| Signal Name | Ball Reference |
|---|---|
| DQB0_25 | B26 |
| DQB0_26 | C25 |
| DQB0_27 | B25 |
| DQB0_28 | A24 |
| DQB0_29 | A23 |
| DQB0_30 | B23 |
| DQB0_31 | D21 |
| DQB1_0 | G18 |
| DQB1_1 | H18 |
| DQB1_2 | F17 |
| DQB1_3 | G17 |
| DQB1_4 | F15 |
| DQB1_5 | H15 |
| DQB1_6 | D14 |
| DQB1_7 | E14 |
| DQB1_8 | J12 |
| DQB1_9 | E11 |
| DQB1_10 | F11 |
| DQB1_11 | H11 |
| DQB1_12 | E9 |
| DQB1_13 | G9 |
| DQB1_14 | H9 |
| DQB1_15 | F8 |
| DQB1_16 | B15 |
| DQB1_17 | C15 |
| DQB1_18 | A14 |
| DQB1_19 | B14 |
| DQB1_20 | D12 |
| DQB1_21 | B11 |
| DQB1_22 | C11 |
| DQB1_23 | A9 |
| DQB1_24 | C8 |
| DQB1_25 | D8 |
| DQB1_26 | C6 |
| DQB1_27 | B6 |
| DQB1_28 | D5 |
| DQB1_29 | C4 |
| DQB1_30 | B4 |
| DQB1_31 | A3 |
| DQC0_0 | C1 |
| DQC0_1 | D2 |
| DQC0_2 | D3 |

| Signal Name | Ball Reference |
|---|---|
| DQC0_3 | E4 |
| DQC0_4 | F2 |
| DQC0_5 | F3 |
| DQC0_6 | H4 |
| DQC0_7 | H3 |
| DQC0_8 | J1 |
| DQC0_9 | L3 |
| DQC0_10 | L2 |
| DQC0_11 | M4 |
| DQC0_12 | P2 |
| DQC0_13 | P1 |
| DQC0_14 | R3 |
| DQC0_15 | R2 |
| DQC0_16 | H6 |
| DQC0_17 | J8 |
| DQC0_18 | J7 |
| DQC0_19 | J5 |
| DQC0_20 | L8 |
| DQC0_21 | L6 |
| DQC0_22 | L5 |
| DQC0_23 | M9 |
| DQC0_24 | P5 |
| DQC0_25 | P4 |
| DQC0_26 | R8 |
| DQC0_27 | R6 |
| DQC0_28 | U7 |
| DQC0_29 | U6 |
| DQC0_30 | V8 |
| DQC0_31 | V7 |
| DQC1_0 | AA4 |
| DQC1_1 | AC2 |
| DQC1_2 | AC1 |
| DQC1_3 | AD1 |
| DQC1_4 | AE3 |
| DQC1_5 | AE2 |
| DQC1_6 | AF2 |
| DQC1_7 | AF1 |
| DQC1_8 | U4 |
| DQC1_9 | U3 |
| DQC1_10 | U1 |
| DQC1_11 | V2 |
| DQC1_12 | W2 |

| Signal Name | Ball Reference |
|---|---|
| DQC1_13 | Y4 |
| DQC1_14 | Y1 |
| DQC1_15 | Y3 |
| DQC1_16 | V4 |
| DQC1_17 | V5 |
| DQC1_18 | W6 |
| DQC1_19 | W5 |
| DQC1_20 | Y6 |
| DQC1_21 | Y7 |
| DQC1_22 | Y9 |
| DQC1_23 | AA5 |
| DQC1_24 | AC7 |
| DQC1_25 | AC5 |
| DQC1_26 | AC4 |
| DQC1_27 | AD9 |
| DQC1_28 | AE8 |
| DQC1_29 | AE6 |
| DQC1_30 | AE5 |
| DQC1_31 | AF10 |
| DQD0_0 | AF7 |
| DQD0_1 | AF5 |
| DQD0_2 | AF4 |
| DQD0_3 | AG6 |
| DQD0_4 | AJ6 |
| DQD0_5 | AJ5 |
| DQD0_6 | AJ9 |
| DQD0_7 | AK7 |
| DQD0_8 | AM7 |
| DQD0_9 | AM6 |
| DQD0_10 | AN6 |
| DQD0_11 | AN5 |
| DQD0_12 | AR7 |
| DQD0_13 | AT6 |
| DQD0_14 | AT8 |
| DQD0_15 | AV5 |
| DQD0_16 | AG1 |
| DQD0_17 | AG3 |
| DQD0_18 | AG4 |
| DQD0_19 | AJ2 |
| DQD0_20 | AK2 |
| DQD0_21 | AM4 |
| DQD0_22 | AM3 |

| Signal Name | Ball Reference |
|---|---|
| DQD0_23 | AM1 |
| DQD0_24 | AR1 |
| DQD0_25 | AR2 |
| DQD0_26 | AT1 |
| DQD0_27 | AT3 |
| DQD0_28 | AV3 |
| DQD0_29 | AW1 |
| DQD0_30 | AY2 |
| DQD0_31 | BA1 |
| DQD1_0 | AW3 |
| DQD1_1 | AW4 |
| DQD1_2 | BA5 |
| DQD1_3 | AY5 |
| DQD1_4 | AU9 |
| DQD1_5 | AW9 |
| DQD1_6 | AY9 |
| DQD1_7 | AT11 |
| DQD1_8 | AU12 |
| DQD1_9 | AV12 |
| DQD1_10 | AU14 |
| DQD1_11 | AW14 |
| DQD1_12 | AT15 |
| DQD1_13 | AV15 |
| DQD1_14 | AU17 |
| DQD1_15 | AV17 |
| DQD1_16 | BB4 |
| DQD1_17 | BC3 |
| DQD1_18 | BC5 |
| DQD1_19 | BA6 |
| DQD1_20 | BA8 |
| DQD1_21 | BC8 |
| DQD1_22 | BB9 |
| DQD1_23 | BC9 |
| DQD1_24 | AY12 |
| DQD1_25 | BA12 |
| DQD1_26 | BC12 |
| DQD1_27 | BB14 |
| DQD1_28 | BB15 |
| DQD1_29 | AY17 |
| DQD1_30 | BA17 |
| DQD1_31 | BC17 |
| DRAIN | AM20 |

| Signal Name | Ball Reference |
|---|---|
| DRAM_RSTA | W30 |
| DRAM_RSTB | M14 |
| DRAM_RSTC | P12 |
| DRAM_RSTD | AK19 |
| EDCA0_0 | R41 |
| EDCA0_1 | F42 |
| EDCA0_2 | R39 |
| EDCA0_3 | H38 |
| EDCA1_0 | B38 |
| EDCA1_1 | C29 |
| EDCA1_2 | D35 |
| EDCA1_3 | G27 |
| EDCB0_0 | F24 |
| EDCB0_1 | J19 |
| EDCB0_2 | A18 |
| EDCB0_3 | D24 |
| EDCB1_0 | E15 |
| EDCB1_1 | D9 |
| EDCB1_2 | A12 |
| EDCB1_3 | B5 |
| EDCC0_0 | E2 |
| EDCC0_1 | M1 |
| EDCC0_2 | J4 |
| EDCC0_3 | R5 |
| EDCC1_0 | AD4 |
| EDCC1_1 | V1 |
| EDCC1_2 | W9 |
| EDCC1_3 | AD6 |
| EDCD0_0 | AG7 |
| EDCD0_1 | AR4 |
| EDCD0_2 | AJ3 |
| EDCD0_3 | AV2 |
| EDCD1_0 | AV8 |
| EDCD1_1 | AW15 |
| EDCD1_2 | BB6 |
| EDCD1_3 | BA15 |
| FB_VDDC | AL21 |
| FB_VDDCI | AK23 |
| FB_VSS | AK21 |
| GATE | AM21 |
| GENERICA | AW40 |
| GENERICB | AT24 |

| Signal Name | Ball Reference |
|---|---|
| GENERICC | AT30 |
| GENERICD | AR30 |
| GENERICE_HPD4 | AU29 |
| GENERICF_HPD5 | AU30 |
| GENERICG_HPD6 | AU32 |
| GENLK_CLK | AM27 |
| GENLK_VSYNC | AL27 |
| GPIO_0 | V39 |
| GPIO_1 | V38 |
| GPIO_2 | W37 |
| GPIO_5_REG_HOT_AC_BATT | AJ34 |
| GPIO_6_TACH | AE34 |
| GPIO_8_ROMSO | AN30 |
| GPIO_9_ROMSI | AP32 |
| GPIO_10_ROMSCK | AM30 |
| GPIO_11 | V43 |
| GPIO_12 | V42 |
| GPIO_13 | V41 |
| GPIO_14_HPD2 | AR29 |
| GPIO_15 | AJ31 |
| GPIO_16_8P_DETECT | AJ33 |
| GPIO_17_THERMAL_INT | AE33 |
| GPIO_18_HPD3 | AT29 |
| GPIO_19_CTF | AC31 |
| GPIO_20 | AK33 |
| GPIO_21 | AK34 |
| GPIO_22_ROMCSB | AN32 |
| GPIO_28_FDO | AF31 |
| GPIO_29 | AG31 |
| GPIO_30 | AG30 |
| GPIO_SVC | AM23 |
| GPIO_SVD | AP23 |
| GPIO_SVT | AN23 |
| HPD1 | AT32 |
| HSYNC | AP24 |
| JTAG_TCK | AF30 |
| JTAG_TDI | AD30 |
| JTAG_TDO | AD31 |
| JTAG_TMS | AE31 |
| JTAG_TRSTB | AC30 |
| MAA0_0 | U32 |
| MAA0_1 | U34 |

| Signal Name | Ball Reference |
|---|---|
| MAA0_2 | V31 |
| MAA0_3 | U35 |
| MAA0_4 | V36 |
| MAA0_5 | V33 |
| MAA0_6 | R33 |
| MAA0_7 | R35 |
| MAA0_8 | U31 |
| MAA0_9 | W35 |
| MAA1_0 | H33 |
| MAA1_1 | M32 |
| MAA1_2 | J32 |
| MAA1_3 | K32 |
| MAA1_4 | K30 |
| MAA1_5 | L30 |
| MAA1_6 | H35 |
| MAA1_7 | L33 |
| MAA1_8 | J33 |
| MAA1_9 | N27 |
| MAB0_0 | H23 |
| MAB0_1 | N24 |
| MAB0_2 | K24 |
| MAB0_3 | M24 |
| MAB0_4 | L25 |
| MAB0_5 | M25 |
| MAB0_6 | N23 |
| MAB0_7 | L23 |
| MAB0_8 | K23 |
| MAB0_9 | J27 |
| MAB1_0 | N18 |
| MAB1_1 | K17 |
| MAB1_2 | N17 |
| MAB1_3 | M17 |
| MAB1_4 | L15 |
| MAB1_5 | J15 |
| MAB1_6 | P19 |
| MAB1_7 | K18 |
| MAB1_8 | L18 |
| MAB1_9 | K14 |
| MAC0_0 | V13 |
| MAC0_1 | U10 |
| MAC0_2 | U13 |
| MAC0_3 | U12 |

| Signal Name | Ball Reference |
|---|---|
| MAC0_4 | R11 |
| MAC0_5 | R9 |
| MAC0_6 | W14 |
| MAC0_7 | V10 |
| MAC0_8 | V11 |
| MAC0_9 | P10 |
| MAC1_0 | AC8 |
| MAC1_1 | AD13 |
| MAC1_2 | AD10 |
| MAC1_3 | AD12 |
| MAC1_4 | AE11 |
| MAC1_5 | AE12 |
| MAC1_6 | AC13 |
| MAC1_7 | AC11 |
| MAC1_8 | AC10 |
| MAC1_9 | AG9 |
| MAD0_0 | AN8 |
| MAD0_1 | AM12 |
| MAD0_2 | AM9 |
| MAD0_3 | AM10 |
| MAD0_4 | AK10 |
| MAD0_5 | AK11 |
| MAD0_6 | AR8 |
| MAD0_7 | AN11 |
| MAD0_8 | AN9 |
| MAD0_9 | AG13 |
| MAD1_0 | AM17 |
| MAD1_1 | AP17 |
| MAD1_2 | AL18 |
| MAD1_3 | AR17 |
| MAD1_4 | AT18 |
| MAD1_5 | AN18 |
| MAD1_6 | AN15 |
| MAD1_7 | AR15 |
| MAD1_8 | AL17 |
| MAD1_9 | AR19 |
| MEM_CALRA | Y31 |
| MEM_CALRB | P15 |
| MEM_CALRC | R14 |
| MEM_CALRD | AL20 |
| MVREFDA | P25 |
| MVREFDB | P20 |

| Signal Name | Ball Reference |
|---|---|
| MVREFDC | Y14 |
| MVREFDD | AE14 |
| PCIE_REFCLKN | AR43 |
| PCIE_REFCLKP | AR42 |
| PCIE_RX0N | AN43 |
| PCIE_RX0P | AN42 |
| PCIE_RX1N | AM41 |
| PCIE_RX1P | AN41 |
| PCIE_RX2N | AM42 |
| PCIE_RX2P | AM43 |
| PCIE_RX3N | AK42 |
| PCIE_RX3P | AK43 |
| PCIE_RX4N | AJ43 |
| PCIE_RX4P | AJ42 |
| PCIE_RX5N | AG41 |
| PCIE_RX5P | AJ41 |
| PCIE_RX6N | AG42 |
| PCIE_RX6P | AG43 |
| PCIE_RX7N | AF42 |
| PCIE_RX7P | AF43 |
| PCIE_RX8N | AE43 |
| PCIE_RX8P | AE42 |
| PCIE_RX9N | AD41 |
| PCIE_RX9P | AE41 |
| PCIE_RX10N | AD42 |
| PCIE_RX10P | AD43 |
| PCIE_RX11N | AC42 |
| PCIE_RX11P | AC43 |
| PCIE_RX12N | AA43 |
| PCIE_RX12P | AA42 |
| PCIE_RX13N | Y41 |
| PCIE_RX13P | AA41 |
| PCIE_RX14N | Y42 |
| PCIE_RX14P | Y43 |
| PCIE_RX15N | W43 |
| PCIE_RX15P | W42 |
| PCIE_TX0N | AR39 |
| PCIE_TX0P | AR38 |
| PCIE_TX1N | AN37 |
| PCIE_TX1P | AR37 |
| PCIE_TX2N | AN38 |
| PCIE_TX2P | AN39 |

| Signal Name | Ball Reference |
|---|---|
| PCIE_TX3N | AM38 |
| PCIE_TX3P | AM39 |
| PCIE_TX4N | AK39 |
| PCIE_TX4P | AK38 |
| PCIE_TX5N | AJ37 |
| PCIE_TX5P | AK37 |
| PCIE_TX6N | AJ38 |
| PCIE_TX6P | AJ39 |
| PCIE_TX7N | AG38 |
| PCIE_TX7P | AG39 |
| PCIE_TX8N | AF39 |
| PCIE_TX8P | AF38 |
| PCIE_TX9N | AE37 |
| PCIE_TX9P | AF37 |
| PCIE_TX10N | AE38 |
| PCIE_TX10P | AE39 |
| PCIE_TX11N | AD38 |
| PCIE_TX11P | AD39 |
| PCIE_TX12N | AC39 |
| PCIE_TX12P | AC38 |
| PCIE_TX13N | AA37 |
| PCIE_TX13P | AC37 |
| PCIE_TX14N | AA38 |
| PCIE_TX14P | AA39 |
| PCIE_TX15N | Y39 |
| PCIE_TX15P | Y38 |
| PCIE_ZVSS | AK30 |
| PERSTB | AV42 |
| PLLCHARZ_H | AM29 |
| PLLCHARZ_L | AN29 |
| PX_EN | V40 |
| RASA0B | P33 |
| RASA1B | M35 |
| RASB0B | K20 |
| RASB1B | M20 |
| RASC0B | Y12 |
| RASC1B | Y10 |
| RASD0B | AR12 |
| RASD1B | AN14 |
| SCL | AF34 |
| SDA | AF33 |
| SMBCLK | AM34 |

| Signal Name | Ball Reference |
|---|---|
| SMBDAT | AM33 |
| SWAPLOCKA | AT25 |
| SWAPLOCKB | AR25 |
| TEMPIN0 | AG33 |
| TEMPINRETURN | AG34 |
| TEST6 | V14 |
| TESTEN | AE30 |
| TEST_PG | AA31 |
| TEST_PG_BACO | Y32 |
| TSVDD | AR26 |
| TS_A | AA30 |
| TX0M_DPB2N | BC33 |
| TX0M_DPD2N | BB26 |
| TX0M_DPF2N | BA19 |
| TX0P_DPB2P | BB33 |
| TX0P_DPD2P | BC26 |
| TX0P_DPF2P | BA20 |
| TX1M_DPB1N | BB35 |
| TX1M_DPD1N | AY26 |
| TX1M_DPF1N | BC20 |
| TX1P_DPB1P | BC35 |
| TX1P_DPD1P | AY27 |
| TX1P_DPF1P | BB20 |
| TX2M_DPB0N | AY35 |
| TX2M_DPD0N | BC27 |
| TX2M_DPF0N | BB21 |
| TX2P_DPB0P | AY36 |
| TX2P_DPD0P | BB27 |
| TX2P_DPF0P | BC21 |
| TX3M_DPA2N | BB38 |
| TX3M_DPC2N | AY29 |
| TX3M_DPE2N | BC23 |
| TX3P_DPA2P | BC38 |
| TX3P_DPC2P | AY30 |
| TX3P_DPE2P | BB23 |
| TX4M_DPA1N | AY38 |
| TX4M_DPC1N | BC30 |
| TX4M_DPE1N | BB24 |
| TX4P_DPA1P | AY39 |
| TX4P_DPC1P | BB30 |
| TX4P_DPE1P | BC24 |
| TX5M_DPA0N | BC39 |

| Signal Name | Ball Reference |
|---|---|
| TX5M_DPC0N | BB32 |
| TX5M_DPE0N | BA24 |
| TX5P_DPA0P | BB39 |
| TX5P_DPC0P | BC32 |
| TX5P_DPE0P | BA25 |
| TXCAM_DPA3N | BC36 |
| TXCAP_DPA3P | BB36 |
| TXCBM_DPB3N | AY32 |
| TXCBP_DPB3P | AY33 |
| TXCCM_DPC3N | BB29 |
| TXCCP_DPC3P | BC29 |
| TXCDM_DPD3N | BC25 |
| TXCDP_DPD3P | BB25 |
| TXCEM_DPE3N | AY21 |
| TXCEP_DPE3P | AY23 |
| TXCFM_DPF3N | BB19 |
| TXCFP_DPF3P | BC19 |
| VDDC | T16 |
| VDDC | T17 |
| VDDC | T20 |
| VDDC | T21 |
| VDDC | T24 |
| VDDC | T25 |
| VDDC | U16 |
| VDDC | U17 |
| VDDC | U20 |
| VDDC | U21 |
| VDDC | U24 |
| VDDC | U25 |
| VDDC | V16 |
| VDDC | V17 |
| VDDC | V20 |
| VDDC | V21 |
| VDDC | V24 |
| VDDC | V25 |
| VDDC | V28 |
| VDDC | W16 |
| VDDC | W17 |
| VDDC | W20 |
| VDDC | W21 |
| VDDC | W24 |
| VDDC | W25 |

| Signal Name | Ball Reference |
|---|---|
| VDDC | W28 |
| VDDC | W29 |
| VDDC | Y16 |
| VDDC | Y17 |
| VDDC | Y20 |
| VDDC | Y21 |
| VDDC | Y24 |
| VDDC | Y25 |
| VDDC | Y28 |
| VDDC | Y29 |
| VDDC | AA16 |
| VDDC | AA17 |
| VDDC | AA20 |
| VDDC | AA21 |
| VDDC | AA24 |
| VDDC | AA25 |
| VDDC | AA28 |
| VDDC | AA29 |
| VDDC | AB16 |
| VDDC | AB17 |
| VDDC | AB20 |
| VDDC | AB21 |
| VDDC | AB24 |
| VDDC | AB25 |
| VDDC | AB28 |
| VDDC | AB29 |
| VDDC | AC16 |
| VDDC | AC17 |
| VDDC | AC20 |
| VDDC | AC21 |
| VDDC | AC24 |
| VDDC | AC25 |
| VDDC | AC28 |
| VDDC | AC29 |
| VDDC | AD16 |
| VDDC | AD17 |
| VDDC | AD20 |
| VDDC | AD21 |
| VDDC | AD24 |
| VDDC | AD25 |
| VDDC | AD28 |
| VDDC | AD29 |

| Signal Name | Ball Reference |
|---|---|
| VDDC | AE16 |
| VDDC | AE17 |
| VDDC | AE20 |
| VDDC | AE21 |
| VDDC | AE24 |
| VDDC | AE25 |
| VDDC | AE28 |
| VDDC | AE29 |
| VDDC | AF16 |
| VDDC | AF17 |
| VDDC | AF20 |
| VDDC | AF21 |
| VDDC | AF24 |
| VDDC | AF25 |
| VDDC | AF28 |
| VDDC | AF29 |
| VDDC | AG17 |
| VDDC | AG20 |
| VDDC | AG21 |
| VDDC | AG24 |
| VDDC | AG25 |
| VDDC | AG28 |
| VDDC | AG29 |
| VDDC | AH18 |
| VDDC | AH19 |
| VDDC | AH20 |
| VDDC | AH21 |
| VDDC | AH22 |
| VDDC | AH23 |
| VDDC | AH24 |
| VDDC | AH25 |
| VDDC | AH26 |
| VDDC | AH27 |
| VDDC | AH28 |
| VDDC | AH29 |
| VDDC | AJ19 |
| VDDC | AJ20 |
| VDDC | AJ21 |
| VDDC | AJ22 |
| VDDC | AJ23 |
| VDDC | AJ24 |
| VDDC | AJ25 |

| Signal Name | Ball Reference |
|---|---|
| VDDC | AJ26 |
| VDDC | AJ27 |
| VDDC | AJ28 |
| VDDCI | P21 |
| VDDCI | P23 |
| VDDCI | R16 |
| VDDCI | R18 |
| VDDCI | R19 |
| VDDCI | R20 |
| VDDCI | R24 |
| VDDCI | R25 |
| VDDCI | R26 |
| VDDCI | R28 |
| VDDCI | T15 |
| VDDCI | T27 |
| VDDCI | T29 |
| VDDCI | U28 |
| VDDCI | V15 |
| VDDCI | V29 |
| VDDCI | W15 |
| VDDCI | Y15 |
| VDDCI | AA14 |
| VDDCI | AC14 |
| VDDCI | AD15 |
| VDDCI | AE15 |
| VDDCI | AF15 |
| VDDCI | AG16 |
| VDDCI | AH15 |
| VDDCI | AH17 |
| VDDCI | AJ16 |
| VDDCI | AJ18 |
| VDD_08 | AA34 |
| VDD_08 | AA35 |
| VDD_08 | AD36 |
| VDD_08 | AE35 |
| VDD_08 | AF35 |
| VDD_08 | AG36 |
| VDD_08 | AJ30 |
| VDD_08 | AJ35 |
| VDD_08 | AK35 |
| VDD_08 | AM36 |
| VDD_08 | AN35 |

| Signal Name | Ball Reference |
|---|---|
| VDD_18 | AM25 |
| VDD_18 | AN25 |
| VDD_18 | AN26 |
| VDD_18 | AP26 |
| VDD_18 | AP27 |
| VDD_18 | AR27 |
| VDD_33 | AL24 |
| VDD_33 | AM24 |
| VMEMIO | E6 |
| VMEMIO | E12 |
| VMEMIO | E17 |
| VMEMIO | E20 |
| VMEMIO | E27 |
| VMEMIO | E32 |
| VMEMIO | F5 |
| VMEMIO | G11 |
| VMEMIO | G15 |
| VMEMIO | G19 |
| VMEMIO | G25 |
| VMEMIO | G29 |
| VMEMIO | G33 |
| VMEMIO | J14 |
| VMEMIO | J18 |
| VMEMIO | J23 |
| VMEMIO | J26 |
| VMEMIO | J30 |
| VMEMIO | L17 |
| VMEMIO | L20 |
| VMEMIO | L24 |
| VMEMIO | L27 |
| VMEMIO | L37 |
| VMEMIO | M5 |
| VMEMIO | M12 |
| VMEMIO | M39 |
| VMEMIO | N15 |
| VMEMIO | N19 |
| VMEMIO | N25 |
| VMEMIO | N29 |
| VMEMIO | P14 |
| VMEMIO | P30 |
| VMEMIO | P35 |
| VMEMIO | R7 |

| Signal Name | Ball Reference |
|---|---|
| VMEMIO | R13 |
| VMEMIO | R31 |
| VMEMIO | R37 |
| VMEMIO | U5 |
| VMEMIO | U11 |
| VMEMIO | U33 |
| VMEMIO | U39 |
| VMEMIO | V9 |
| VMEMIO | V35 |
| VMEMIO | W7 |
| VMEMIO | W13 |
| VMEMIO | W31 |
| VMEMIO | Y11 |
| VMEMIO | Y33 |
| VMEMIO | AC9 |
| VMEMIO | AD11 |
| VMEMIO | AE7 |
| VMEMIO | AE13 |
| VMEMIO | AF9 |
| VMEMIO | AG5 |
| VMEMIO | AG11 |
| VMEMIO | AJ7 |
| VMEMIO | AJ13 |
| VMEMIO | AK9 |
| VMEMIO | AK14 |
| VMEMIO | AL15 |
| VMEMIO | AL19 |
| VMEMIO | AM5 |
| VMEMIO | AN7 |
| VMEMIO | AN17 |
| VMEMIO | AN20 |
| VMEMIO | AR14 |
| VMEMIO | AR18 |
| VMEMIO | AU11 |
| VMEMIO | AU15 |
| VMEMIO | AW12 |
| VMEMIO | AW17 |
| VSS | A2 |
| VSS | A6 |
| VSS | A11 |
| VSS | A15 |
| VSS | A19 |

| Signal Name | Ball Reference |
|---|---|
| VSS | A25 |
| VSS | A29 |
| VSS | A33 |
| VSS | A38 |
| VSS | A42 |
| VSS | B1 |
| VSS | B2 |
| VSS | B8 |
| VSS | B12 |
| VSS | B17 |
| VSS | B20 |
| VSS | B24 |
| VSS | B27 |
| VSS | B32 |
| VSS | B36 |
| VSS | B39 |
| VSS | B42 |
| VSS | B43 |
| VSS | C5 |
| VSS | C9 |
| VSS | C14 |
| VSS | C18 |
| VSS | C21 |
| VSS | C23 |
| VSS | C26 |
| VSS | C30 |
| VSS | C35 |
| VSS | C40 |
| VSS | D6 |
| VSS | D11 |
| VSS | D15 |
| VSS | D19 |
| VSS | D25 |
| VSS | D29 |
| VSS | D33 |
| VSS | D38 |
| VSS | D41 |
| VSS | E3 |
| VSS | E5 |
| VSS | E8 |
| VSS | E24 |
| VSS | E36 |

| Signal Name | Ball Reference |
|---|---|
| VSS | E39 |
| VSS | E42 |
| VSS | F1 |
| VSS | F4 |
| VSS | F6 |
| VSS | F9 |
| VSS | F14 |
| VSS | F18 |
| VSS | F21 |
| VSS | F23 |
| VSS | F26 |
| VSS | F30 |
| VSS | F35 |
| VSS | F38 |
| VSS | F40 |
| VSS | F43 |
| VSS | H2 |
| VSS | H5 |
| VSS | H8 |
| VSS | H12 |
| VSS | H17 |
| VSS | H20 |
| VSS | H24 |
| VSS | H26 |
| VSS | H27 |
| VSS | H32 |
| VSS | H39 |
| VSS | H42 |
| VSS | J3 |
| VSS | J6 |
| VSS | J9 |
| VSS | J21 |
| VSS | J35 |
| VSS | J38 |
| VSS | J41 |
| VSS | K15 |
| VSS | K19 |
| VSS | K25 |
| VSS | K27 |
| VSS | K29 |
| VSS | L1 |
| VSS | L4 |

| Signal Name | Ball Reference |
|---|---|
| VSS | L7 |
| VSS | L11 |
| VSS | L12 |
| VSS | L14 |
| VSS | L32 |
| VSS | L40 |
| VSS | L43 |
| VSS | M2 |
| VSS | M8 |
| VSS | M11 |
| VSS | M18 |
| VSS | M21 |
| VSS | M23 |
| VSS | M26 |
| VSS | M30 |
| VSS | M33 |
| VSS | M36 |
| VSS | M42 |
| VSS | P3 |
| VSS | P6 |
| VSS | P9 |
| VSS | P11 |
| VSS | P17 |
| VSS | P18 |
| VSS | P24 |
| VSS | P27 |
| VSS | P29 |
| VSS | P32 |
| VSS | P38 |
| VSS | P41 |
| VSS | R1 |
| VSS | R4 |
| VSS | R10 |
| VSS | R15 |
| VSS | R17 |
| VSS | R21 |
| VSS | R22 |
| VSS | R23 |
| VSS | R27 |
| VSS | R29 |
| VSS | R30 |
| VSS | R34 |

| Signal Name | Ball Reference |
|---|---|
| VSS | R40 |
| VSS | R43 |
| VSS | T18 |
| VSS | T19 |
| VSS | T22 |
| VSS | T23 |
| VSS | T26 |
| VSS | T28 |
| VSS | U2 |
| VSS | U8 |
| VSS | U14 |
| VSS | U15 |
| VSS | U18 |
| VSS | U19 |
| VSS | U22 |
| VSS | U23 |
| VSS | U26 |
| VSS | U27 |
| VSS | U29 |
| VSS | U30 |
| VSS | U36 |
| VSS | U42 |
| VSS | V3 |
| VSS | V6 |
| VSS | V12 |
| VSS | V18 |
| VSS | V19 |
| VSS | V22 |
| VSS | V23 |
| VSS | V26 |
| VSS | V27 |
| VSS | V30 |
| VSS | V32 |
| VSS | V37 |
| VSS | W1 |
| VSS | W4 |
| VSS | W10 |
| VSS | W18 |
| VSS | W19 |
| VSS | W22 |
| VSS | W23 |
| VSS | W26 |

| Signal Name | Ball Reference |
|---|---|
| VSS | W27 |
| VSS | W34 |
| VSS | W36 |
| VSS | W38 |
| VSS | W39 |
| VSS | W40 |
| VSS | W41 |
| VSS | Y2 |
| VSS | Y5 |
| VSS | Y8 |
| VSS | Y18 |
| VSS | Y19 |
| VSS | Y22 |
| VSS | Y23 |
| VSS | Y26 |
| VSS | Y27 |
| VSS | Y30 |
| VSS | Y35 |
| VSS | Y36 |
| VSS | Y37 |
| VSS | Y40 |
| VSS | AA3 |
| VSS | AA6 |
| VSS | AA9 |
| VSS | AA12 |
| VSS | AA15 |
| VSS | AA18 |
| VSS | AA19 |
| VSS | AA22 |
| VSS | AA23 |
| VSS | AA26 |
| VSS | AA27 |
| VSS | AA32 |
| VSS | AA33 |
| VSS | AA36 |
| VSS | AA40 |
| VSS | AB15 |
| VSS | AB18 |
| VSS | AB19 |
| VSS | AB22 |
| VSS | AB23 |
| VSS | AB26 |

| Signal Name | Ball Reference |
|---|---|
| VSS | AB27 |
| VSS | AC3 |
| VSS | AC6 |
| VSS | AC12 |
| VSS | AC15 |
| VSS | AC18 |
| VSS | AC19 |
| VSS | AC22 |
| VSS | AC23 |
| VSS | AC26 |
| VSS | AC27 |
| VSS | AC32 |
| VSS | AC33 |
| VSS | AC36 |
| VSS | AC40 |
| VSS | AC41 |
| VSS | AD2 |
| VSS | AD5 |
| VSS | AD8 |
| VSS | AD14 |
| VSS | AD18 |
| VSS | AD19 |
| VSS | AD22 |
| VSS | AD23 |
| VSS | AD26 |
| VSS | AD27 |
| VSS | AD32 |
| VSS | AD35 |
| VSS | AD37 |
| VSS | AD40 |
| VSS | AE1 |
| VSS | AE4 |
| VSS | AE10 |
| VSS | AE18 |
| VSS | AE19 |
| VSS | AE22 |
| VSS | AE23 |
| VSS | AE26 |
| VSS | AE27 |
| VSS | AE32 |
| VSS | AE36 |
| VSS | AE40 |

| Signal Name | Ball Reference |
|---|---|
| VSS | AF3 |
| VSS | AF6 |
| VSS | AF8 |
| VSS | AF12 |
| VSS | AF18 |
| VSS | AF19 |
| VSS | AF22 |
| VSS | AF23 |
| VSS | AF26 |
| VSS | AF27 |
| VSS | AF32 |
| VSS | AF36 |
| VSS | AF40 |
| VSS | AF41 |
| VSS | AG2 |
| VSS | AG8 |
| VSS | AG10 |
| VSS | AG14 |
| VSS | AG15 |
| VSS | AG18 |
| VSS | AG19 |
| VSS | AG22 |
| VSS | AG23 |
| VSS | AG26 |
| VSS | AG27 |
| VSS | AG32 |
| VSS | AG35 |
| VSS | AG37 |
| VSS | AG40 |
| VSS | AH16 |
| VSS | AJ1 |
| VSS | AJ4 |
| VSS | AJ10 |
| VSS | AJ14 |
| VSS | AJ15 |
| VSS | AJ17 |
| VSS | AJ29 |
| VSS | AJ32 |
| VSS | AJ36 |
| VSS | AJ40 |
| VSS | AK3 |
| VSS | AK6 |

| Signal Name | Ball Reference |
|---|---|
| VSS | AK12 |
| VSS | AK15 |
| VSS | AK17 |
| VSS | AK18 |
| VSS | AK20 |
| VSS | AK24 |
| VSS | AK27 |
| VSS | AK29 |
| VSS | AK32 |
| VSS | AK36 |
| VSS | AK40 |
| VSS | AK41 |
| VSS | AL23 |
| VSS | AL25 |
| VSS | AL29 |
| VSS | AM2 |
| VSS | AM8 |
| VSS | AM11 |
| VSS | AM14 |
| VSS | AM18 |
| VSS | AM26 |
| VSS | AM32 |
| VSS | AM35 |
| VSS | AM37 |
| VSS | AM40 |
| VSS | AN1 |
| VSS | AN4 |
| VSS | AN12 |
| VSS | AN24 |
| VSS | AN27 |
| VSS | AN33 |
| VSS | AN36 |
| VSS | AN40 |
| VSS | AP15 |
| VSS | AP19 |
| VSS | AP25 |
| VSS | AP29 |
| VSS | AP30 |
| VSS | AR3 |
| VSS | AR6 |
| VSS | AR9 |
| VSS | AR32 |

| Signal Name | Ball Reference |
|---|---|
| VSS | AR33 |
| VSS | AR35 |
| VSS | AR36 |
| VSS | AR40 |
| VSS | AR41 |
| VSS | AT2 |
| VSS | AT5 |
| VSS | AT12 |
| VSS | AT17 |
| VSS | AT21 |
| VSS | AT26 |
| VSS | AT27 |
| VSS | AT35 |
| VSS | AT38 |
| VSS | AT39 |
| VSS | AT40 |
| VSS | AT41 |
| VSS | AT42 |
| VSS | AT43 |
| VSS | AU18 |
| VSS | AU19 |
| VSS | AU23 |
| VSS | AU24 |
| VSS | AU25 |
| VSS | AV1 |
| VSS | AV4 |
| VSS | AV6 |
| VSS | AV9 |
| VSS | AV14 |
| VSS | AV20 |
| VSS | AV29 |
| VSS | AV30 |
| VSS | AV32 |
| VSS | AV33 |
| VSS | AV38 |
| VSS | AV39 |
| VSS | AV40 |
| VSS | AW2 |
| VSS | AW5 |
| VSS | AW8 |
| VSS | AW26 |
| VSS | AW27 |

| Signal Name | Ball Reference |
|---|---|
| VSS | AW29 |
| VSS | AW30 |
| VSS | AW32 |
| VSS | AW33 |
| VSS | AW35 |
| VSS | AW36 |
| VSS | AW38 |
| VSS | AW39 |
| VSS | AW41 |
| VSS | AW43 |
| VSS | AY3 |
| VSS | AY6 |
| VSS | AY11 |
| VSS | AY15 |
| VSS | AY18 |
| VSS | AY19 |
| VSS | AY25 |
| VSS | AY41 |
| VSS | BA4 |
| VSS | BA9 |
| VSS | BA14 |
| VSS | BA18 |
| VSS | BA21 |
| VSS | BA23 |
| VSS | BA26 |
| VSS | BA27 |
| VSS | BA29 |
| VSS | BA30 |
| VSS | BA32 |
| VSS | BA33 |
| VSS | BA35 |
| VSS | BA36 |
| VSS | BA38 |
| VSS | BA39 |
| VSS | BA40 |
| VSS | BB1 |
| VSS | BB2 |
| VSS | BB5 |
| VSS | BB8 |
| VSS | BB12 |
| VSS | BB17 |
| VSS | BB18 |

| Signal Name | Ball Reference |
|---|---|
| VSS | BB42 |
| VSS | BB43 |
| VSS | BC2 |
| VSS | BC6 |
| VSS | BC11 |
| VSS | BC15 |
| VSS | BC18 |
| VSS | BC42 |
| VSYNC | AR24 |
| WAKEB | AV43 |
| WCKA0B_0 | L41 |
| WCKA0B_1 | L38 |
| WCKA0_0 | L42 |
| WCKA0_1 | L39 |
| WCKA1B_0 | C33 |
| WCKA1B_1 | E30 |
| WCKA1_0 | B33 |
| WCKA1_1 | D30 |
| WCKB0B_0 | H21 |
| WCKB0B_1 | B21 |
| WCKB0_0 | G21 |
| WCKB0_1 | A21 |
| WCKB1B_0 | G12 |
| WCKB1B_1 | B9 |
| WCKB1_0 | F12 |
| WCKB1_1 | A8 |
| WCKC0B_0 | J2 |
| WCKC0B_1 | M7 |
| WCKC0_0 | H1 |
| WCKC0_1 | M6 |
| WCKC1B_0 | AA2 |
| WCKC1B_1 | AA8 |
| WCKC1_0 | AA1 |
| WCKC1_1 | AA7 |
| WCKD0B_0 | AK5 |
| WCKD0B_1 | AN3 |
| WCKD0_0 | AK4 |
| WCKD0_1 | AN2 |
| WCKD1B_0 | AV11 |
| WCKD1B_1 | BA11 |
| WCKD1_0 | AW11 |
| WCKD1_1 | BB11 |

| Signal Name | Ball Reference |
|---|---|
| WEA0B | V34 |
| WEA1B | H30 |
| WEB0B | J25 |
| WEB1B | M15 |
| WEC0B | R12 |
| WEC1B | AE9 |
| WED0B | AK8 |
| WED1B | AP18 |
| XTALIN | BA43 |
| XTALOUT | AY42 |