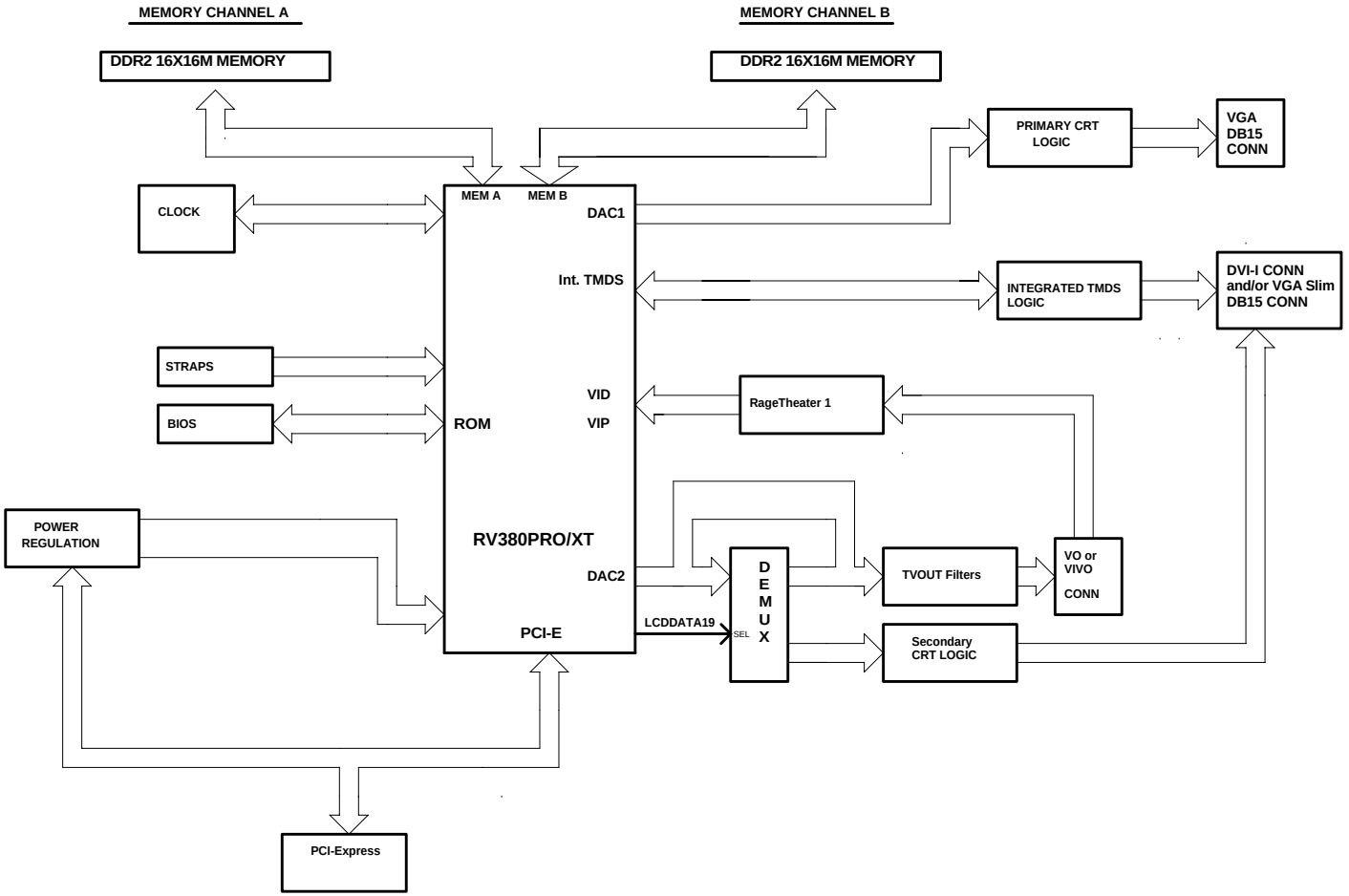
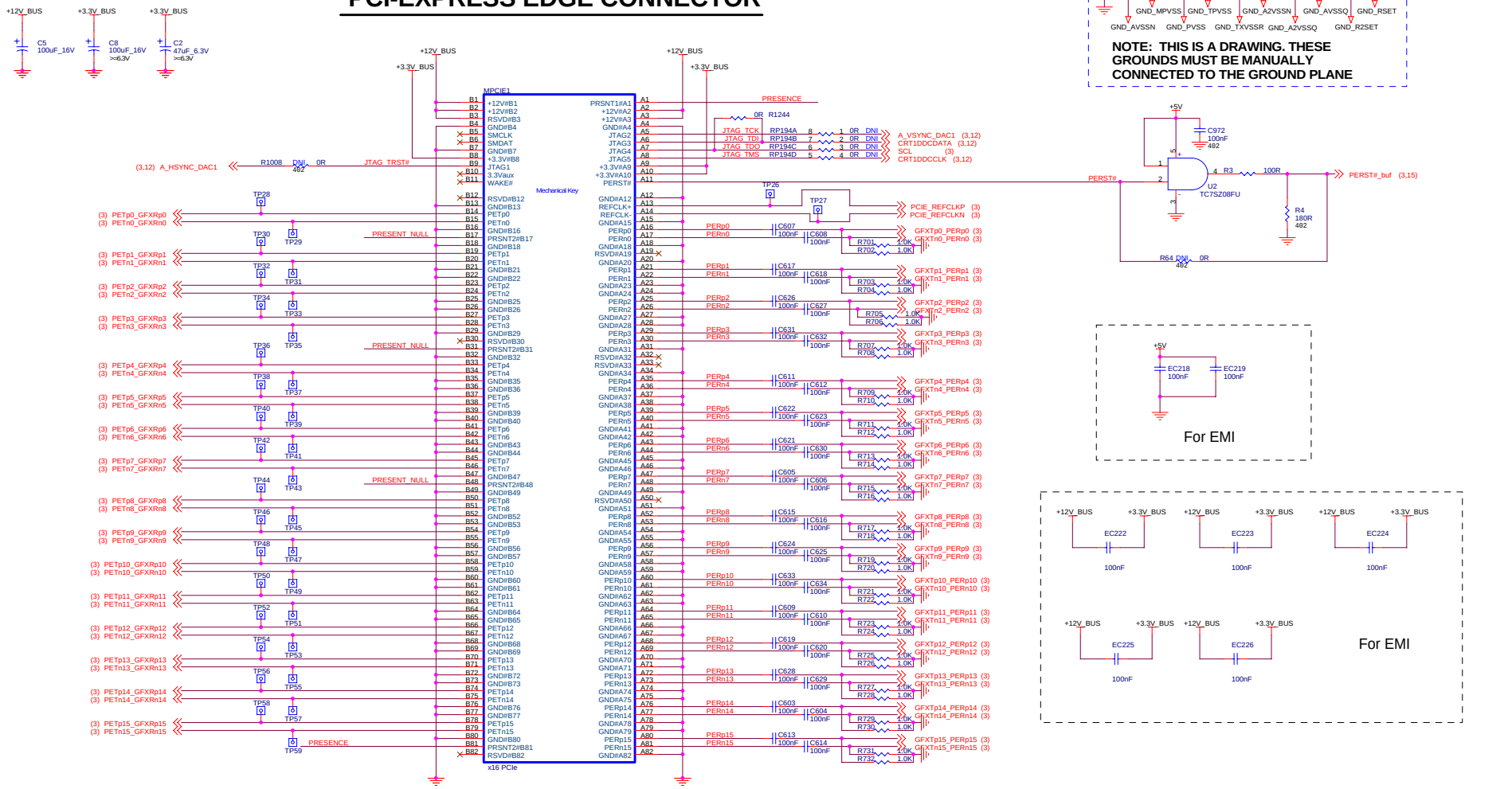


MS-V031 / ATI X550 / DDRII		
Size C	Document Number	Rev 0A
Date: Monday, June 27, 2005	Sheet 1 of 17	

PCI-EXPRESS EDGE CONNECTOR



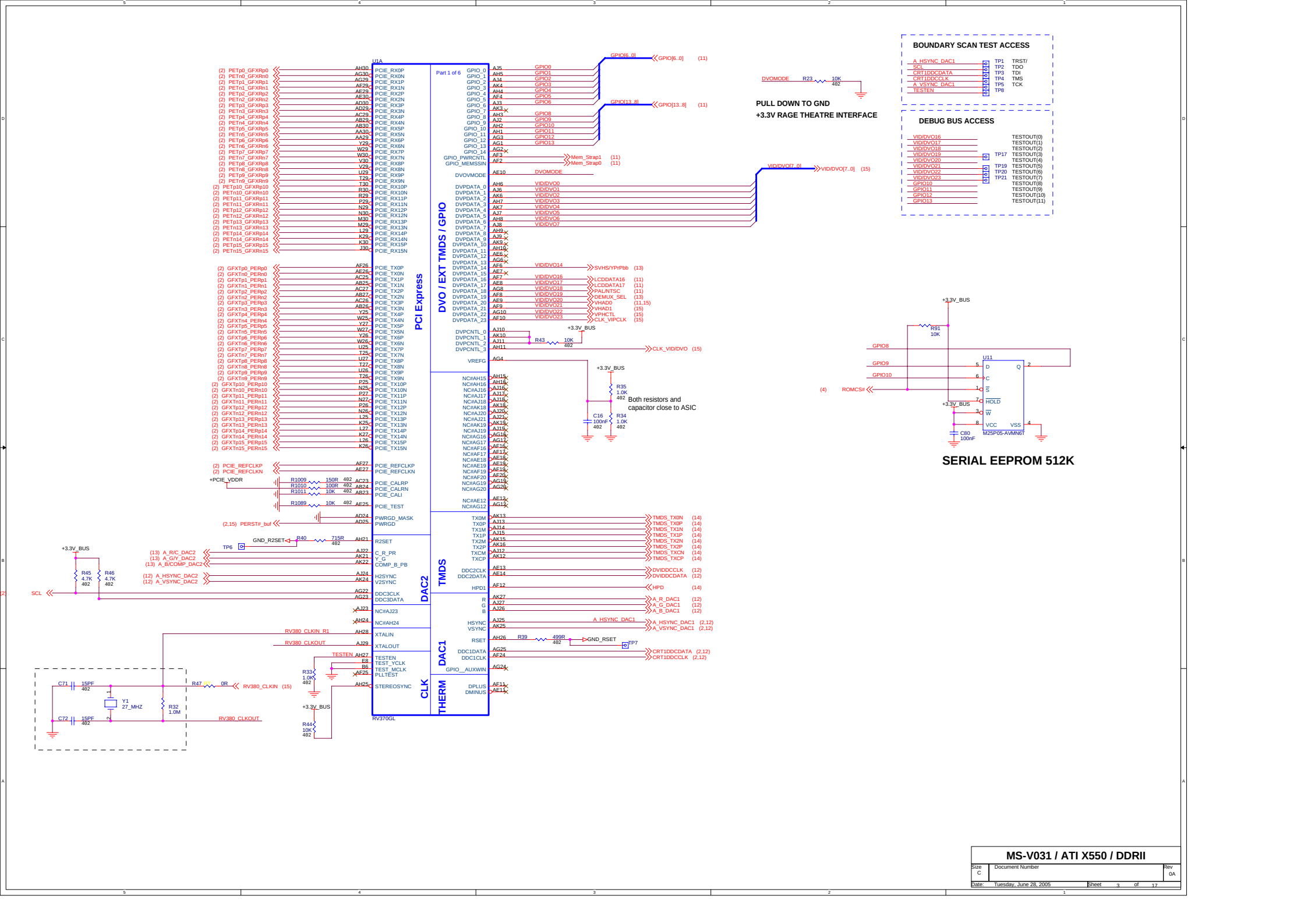
SYMBOL LEGEND

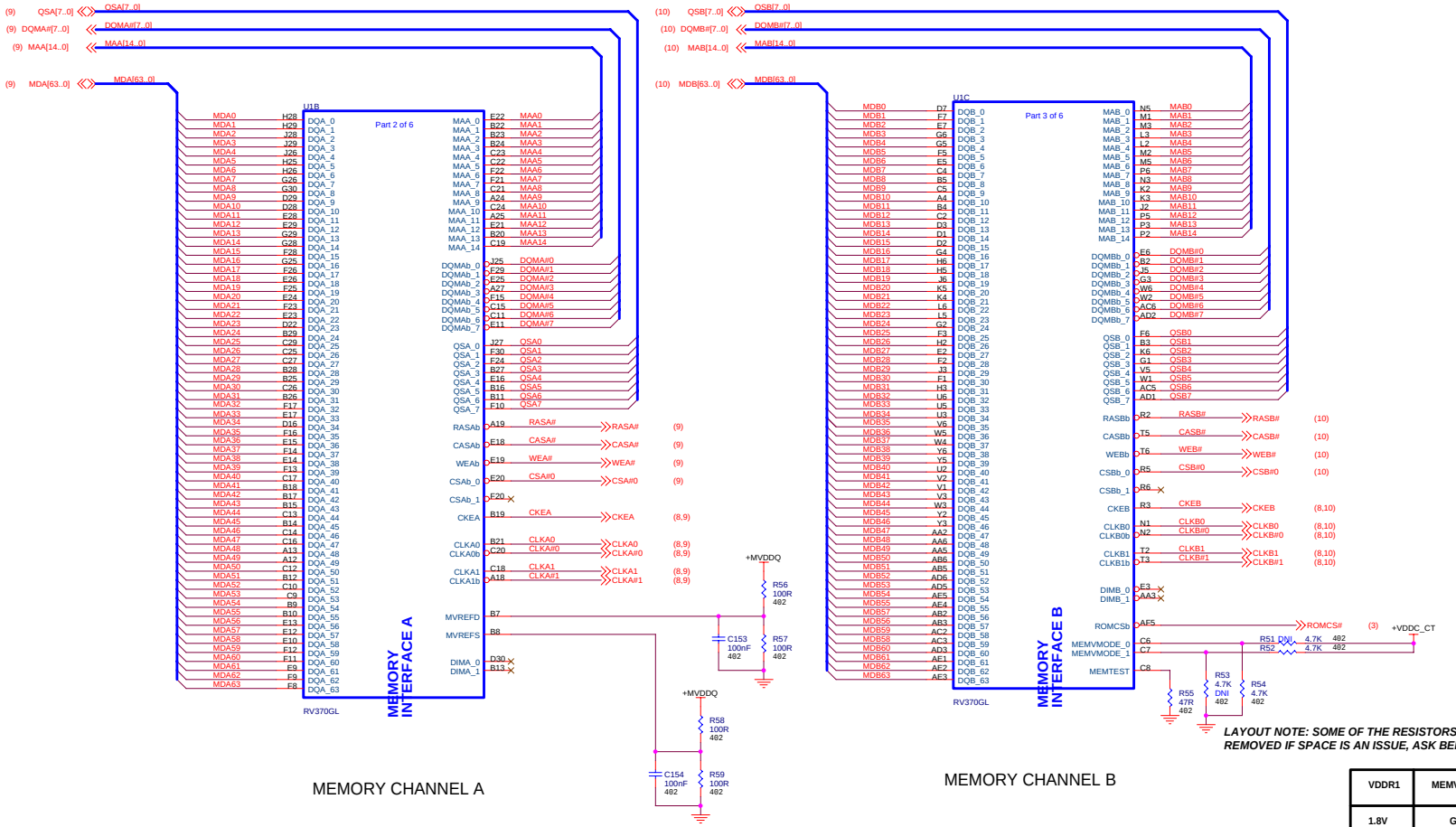
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

MS-V031 / ATI X550 / DDRII

Size	Document Number	Rev
C		0A

Date: Tuesday, June 28, 2005 Sheet 2 of 17


U1A
Part 1 of 6
PCI Express
DVO / EXT TMDS / GPIO
TMDS
DAC2
DAC1
CLK
THERM
RV370GL
PULL DOWN TO GND
+3.3V RAGE THEATRE INTERFACE
BOUNDARY SCAN TEST ACCESS
DEBUG BUS ACCESS
SERIAL EEPROM 512K
M25P05-AVMN6T
Both resistors and capacitor close to ASIC
MS-V031 / ATI X550 / DDRII
Size C
Document Number
Rev 0A
Date: Tuesday, June 28, 2005
Sheet 3 of 17



MEMORY CHANNEL A

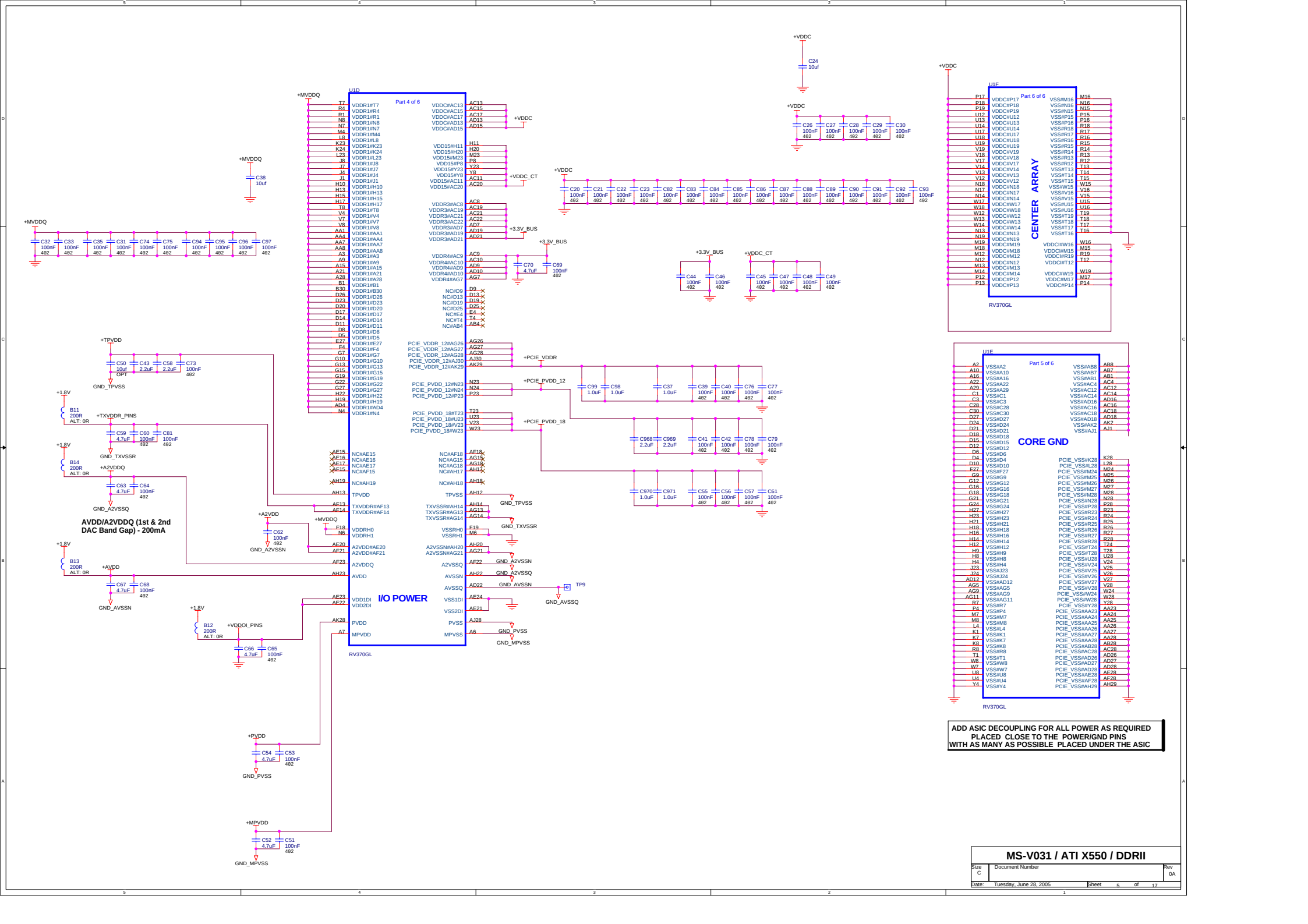
PLACE C351/152 VERY CLOSE TO ASIC
R56/57/58/59 CLOSE TO ASIC AS WELL

MEMORY CHANNEL B

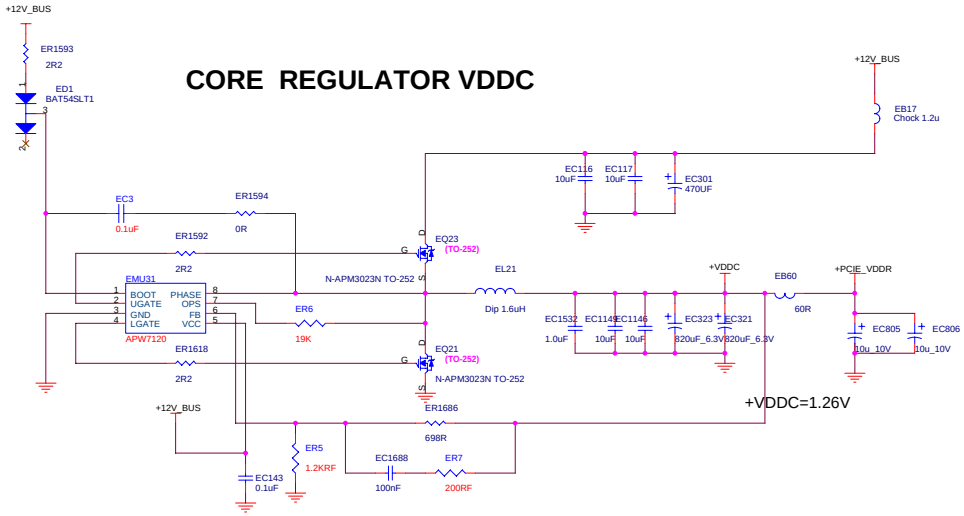
LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

VDDR1	MEMVMODE_0	MEMVMODE_1	
1.8V	GND	+VDDC_CT	**DEFAULT**
2.5V	+VDDC_CT	GND	
2.8V	+VDDC_CT	+VDDC_CT	

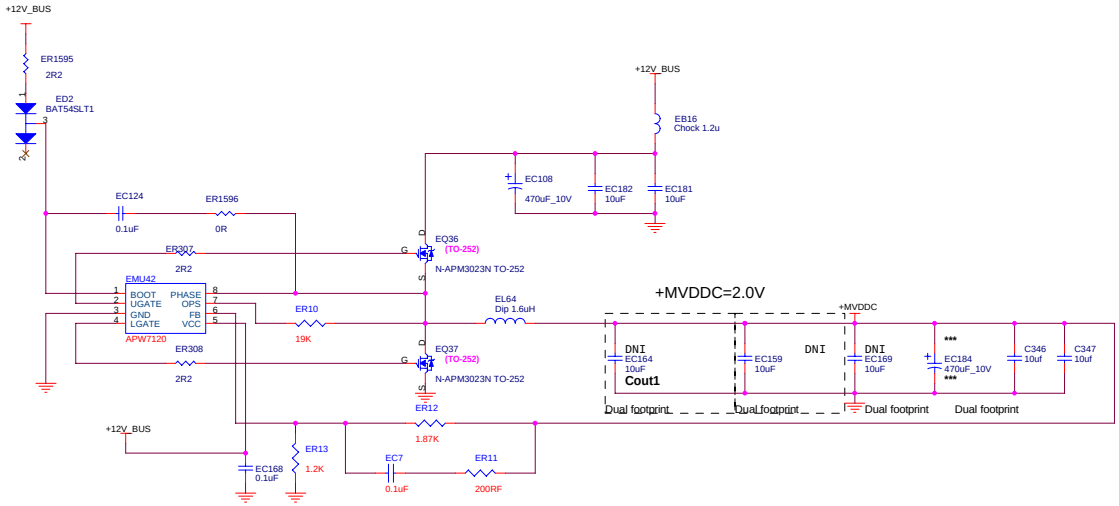
MS-V031 / ATI X550 / DDRII		
Size C	Document Number	Rev 0A
Date: Tuesday, June 28, 2005	Sheet 4 of 17	


U1D
Part 4 of 6
RV370GL
I/O POWER
U1F
Part 6 of 6
CENTER ARRAY
RV370GL
U1E
Part 5 of 6
CORE GND
RV370GL
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
MS-V031 / ATI X550 / DDRII
Size C
Document Number
Rev 0A
Date: Tuesday, June 28, 2005
Sheet 5 of 17

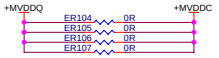
CORE REGULATOR VDDC

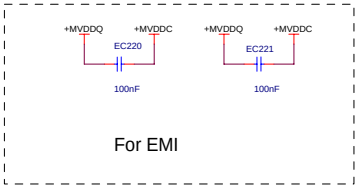


APW7120 Application Circuit

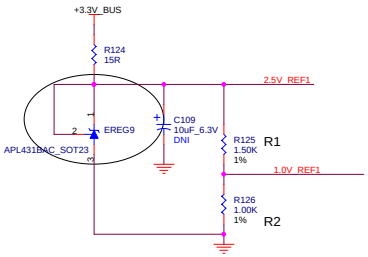


APW7120 Application Circuit

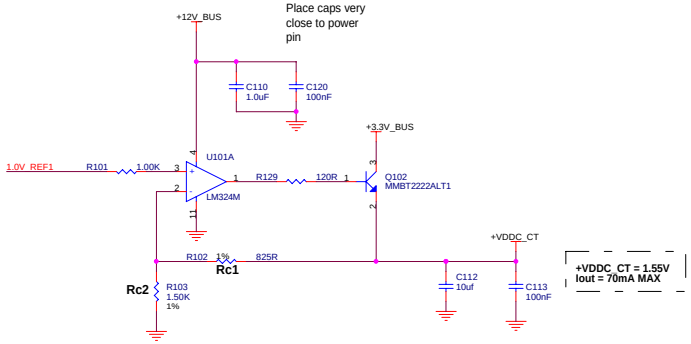


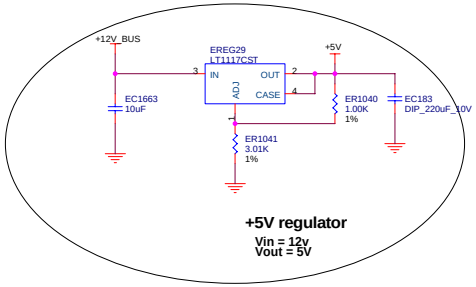


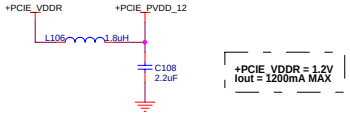
MS-V031 / ATI X550 / DDRII		
Size C	Document Number	Rev 0A
Date: Tuesday, June 28, 2005	Sheet 6 of 17	

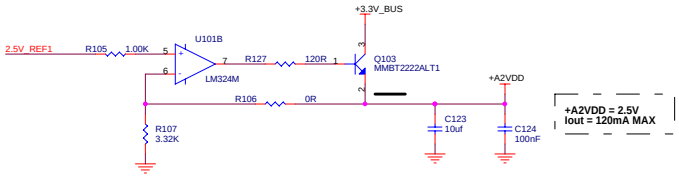


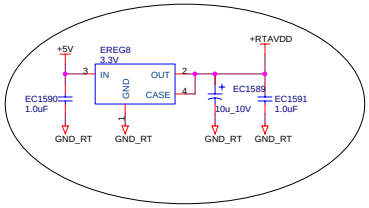
Change to SOT-23

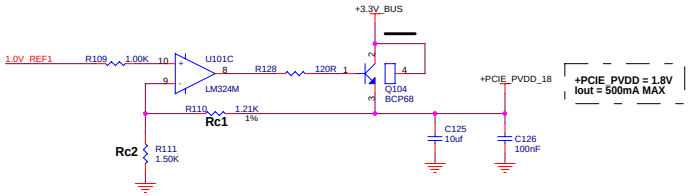


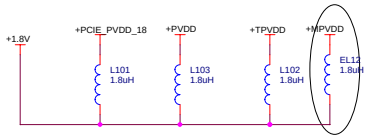




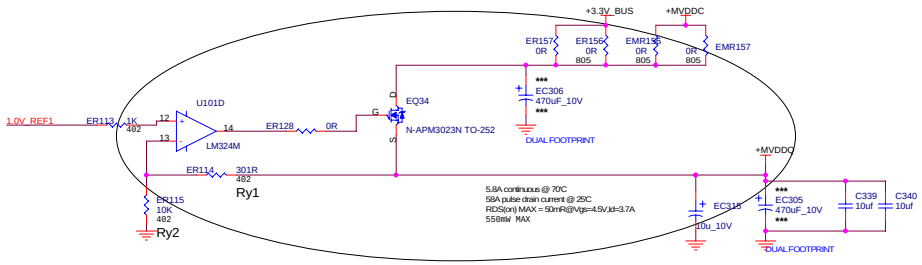








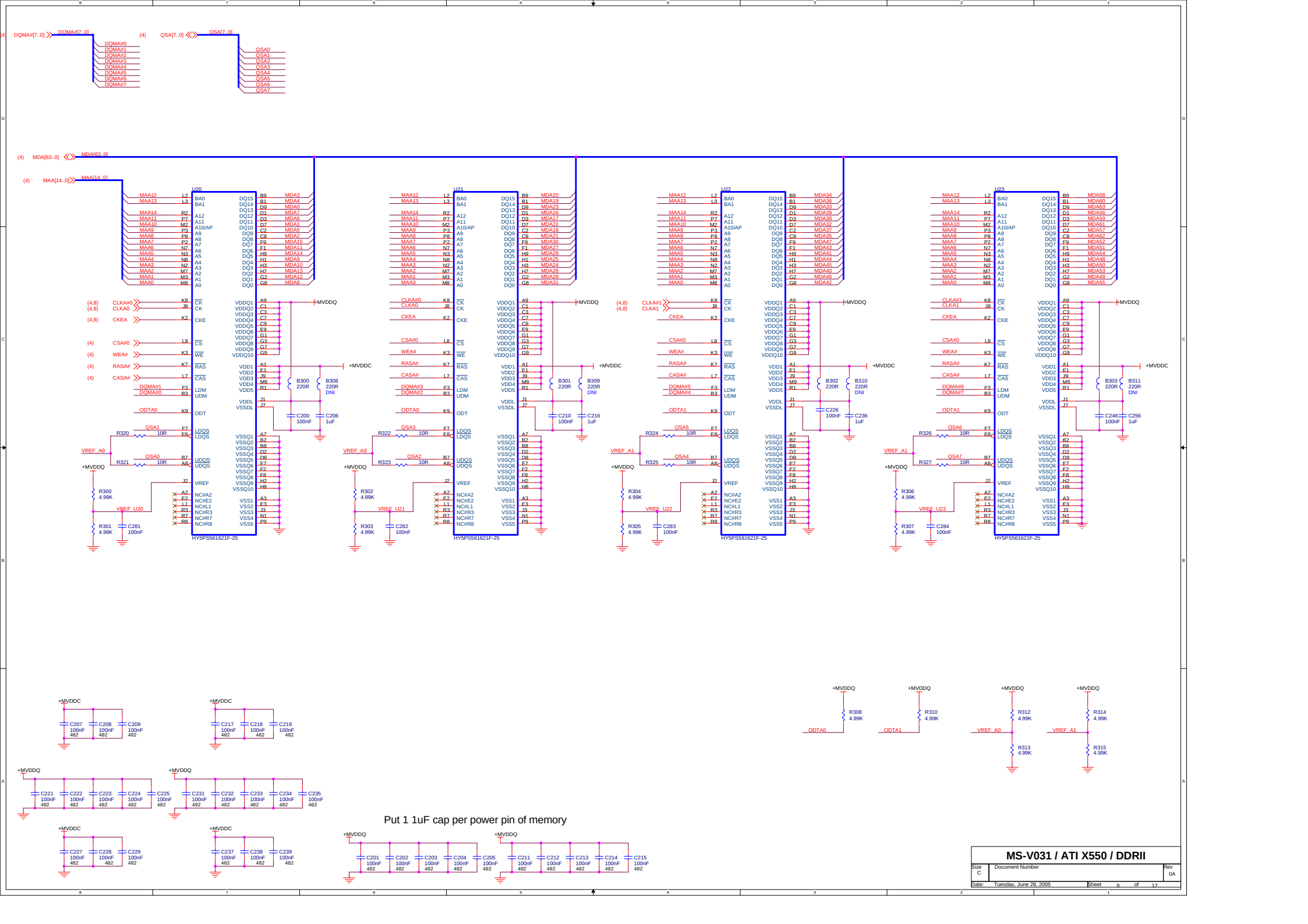
Rails derived from +1.8V
- +AVDD: 10mA MAX
- +A2VDDQ: 20mA MAX
- +VDDOI_PINS: 20mA MAX
- +TXVDDR_PINS: 20mA MAX

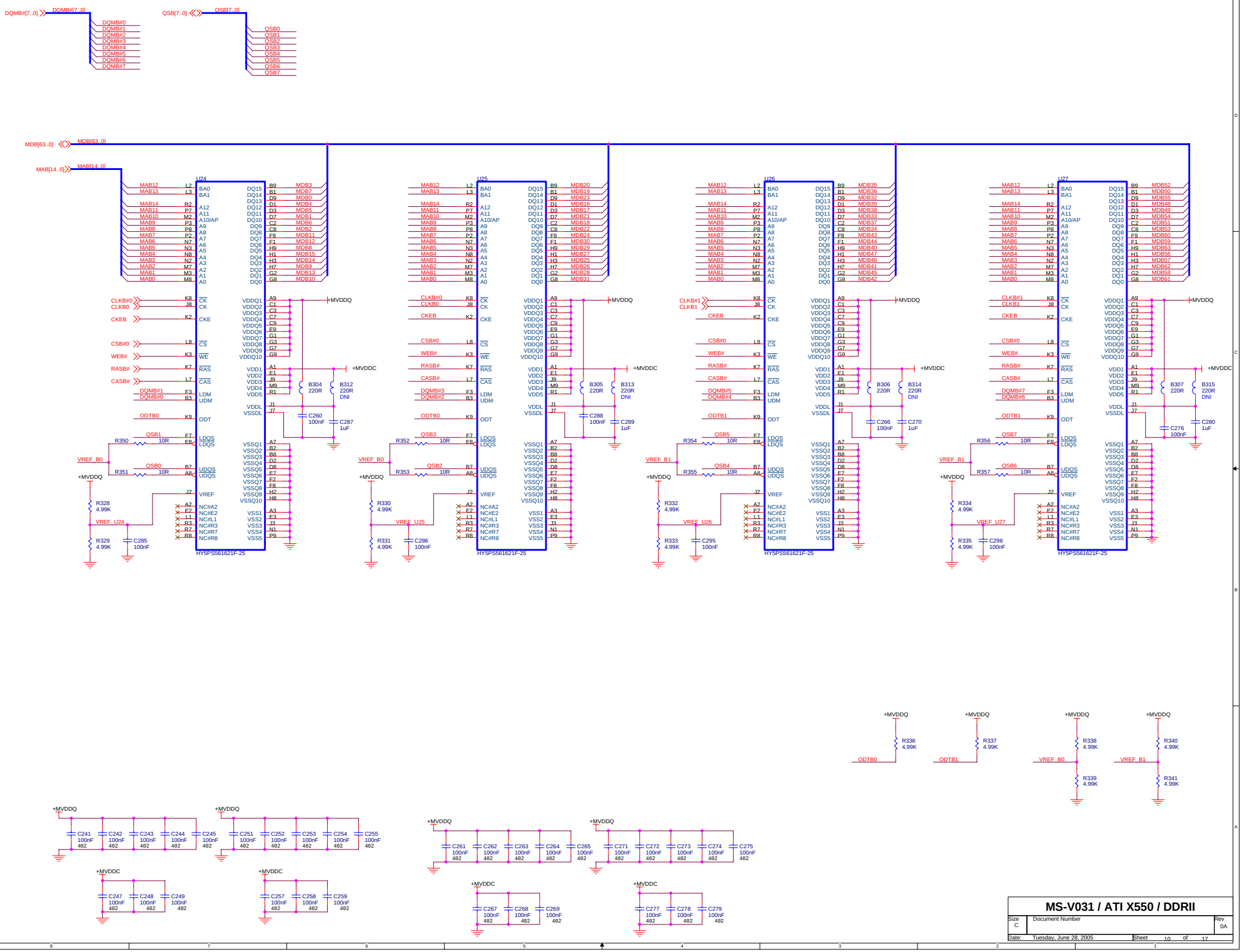


MS-V031 / ATI X550 / DDRII		
Size C	Document Number	Rev 0A
Date: Tuesday, June 28, 2005	Sheet 7 of 17	

TAKE OUT THE PARALLEL TERMINATION ON ADDRESS AND CONTROL

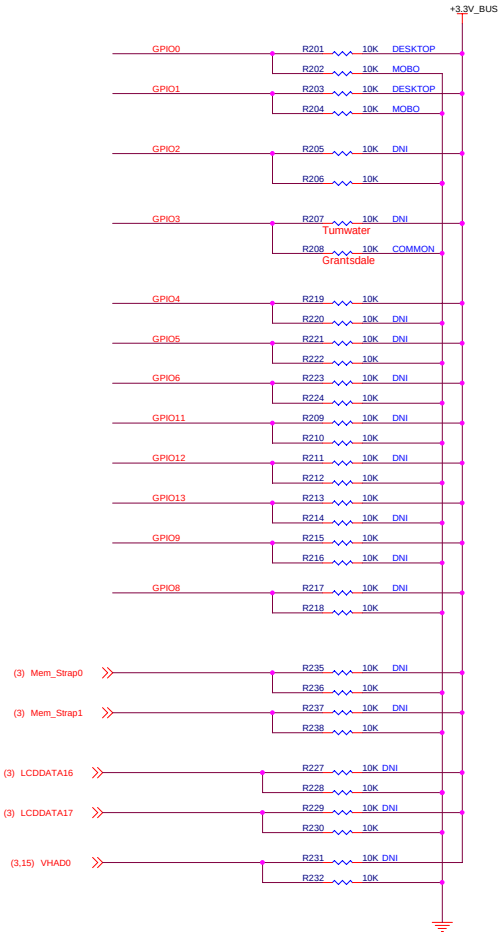
MS-V031 / ATI X550 / DDRII		
Size C	Document Number	Rev 0A
Date: Tuesday, June 28, 2005	Sheet 8 of 17	

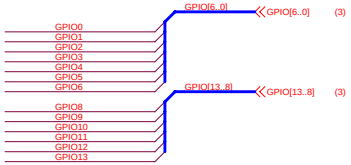

(4) DQMA#[7..0]
DQMA#[7..0]
DQMA#0
DQMA#1
DQMA#2
DQMA#3
DQMA#4
DQMA#5
DQMA#6
DQMA#7
(4) QSA[7..0]
QSA[7..0]
QSA0
QSA1
QSA2
QSA3
QSA4
QSA5
QSA6
QSA7
(4) MDA[63..0]
MDA[63..0]
(4) MAA[14..0]
MAA[14..0]
U20
U21
U22
U23
HY5PS561621F-25
+MVDDQ
+MVDDC
VREF_A0
VREF_A1
VREF_U20
VREF_U21
VREF_U22
VREF_U23
ODTA0
ODTA1
Put 1 1uF cap per power pin of memory
MS-V031 / ATI X550 / DDRII
Size C
Document Number
Rev 0A
Date: Tuesday, June 28, 2005
Sheet 9 of 17



MS-V031 / ATI X550 / DDRII		
Size C	Document Number	Rev 0A
Date: Tuesday, June 28, 2005	Sheet 10 of 17	

OPTION STRAPS

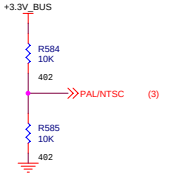




STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

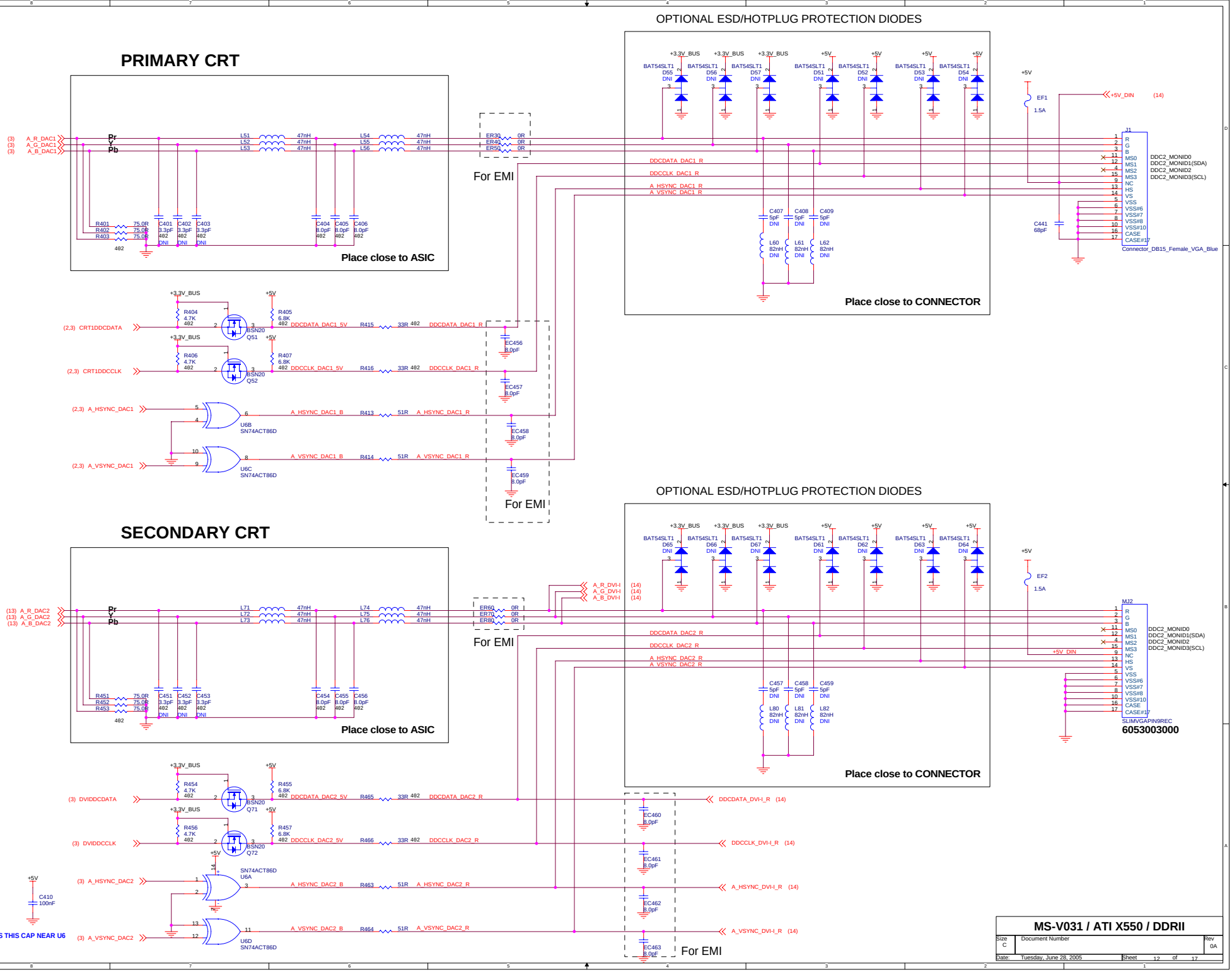


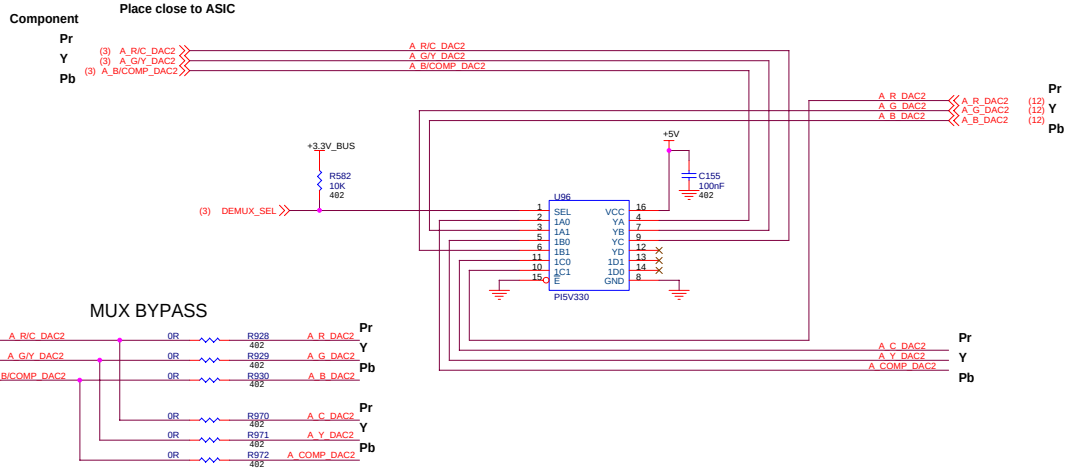
STRAPS	PIN	DESCRIPTION
NTSC/PAL	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 -NTSC (on board resistor pull-up)

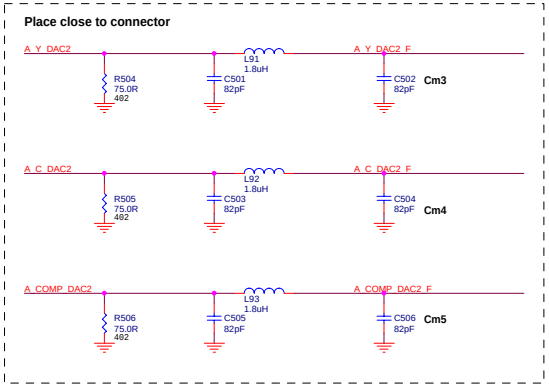
MS-V031 / ATI X550 / DDRII

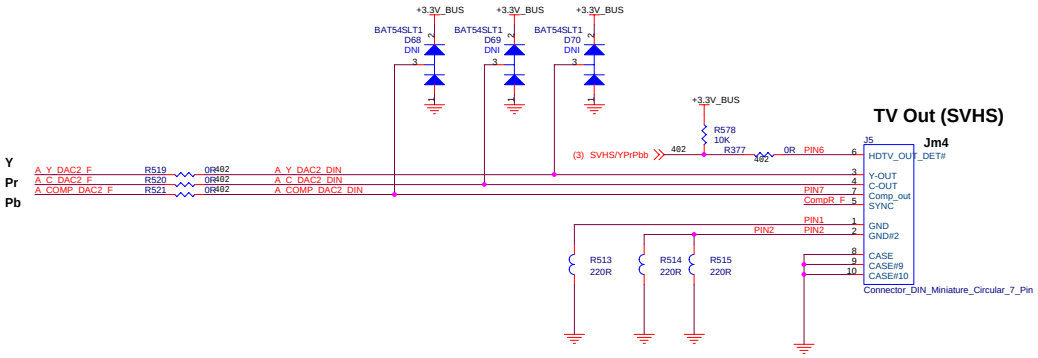
Size	Document Number	Rev
C		0A

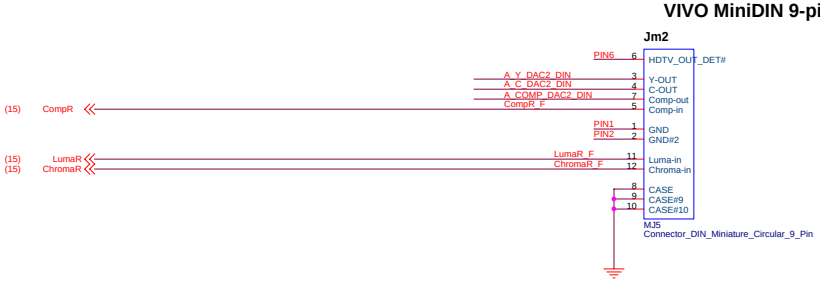
Date: Tuesday, June 28, 2005 Sheet 11 of 17


PRIMARY CRT
OPTIONAL ESD/HOTPLUG PROTECTION DIODES
Place close to ASIC
Place close to CONNECTOR
For EMI
SECONDARY CRT
OPTIONAL ESD/HOTPLUG PROTECTION DIODES
Place close to ASIC
Place close to CONNECTOR
For EMI
PLACES THIS CAP NEAR U6
MS-V031 / ATI X550 / DDRII
Document Number
Tuesday, June 28, 2005
Sheet 12 of 17



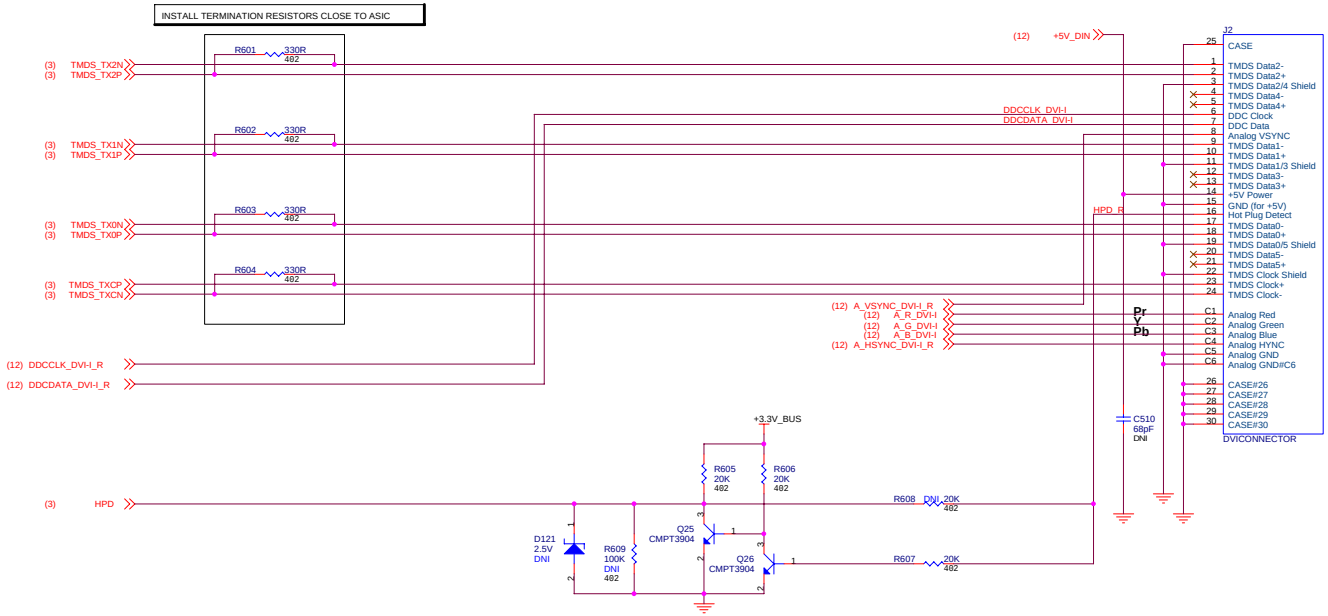




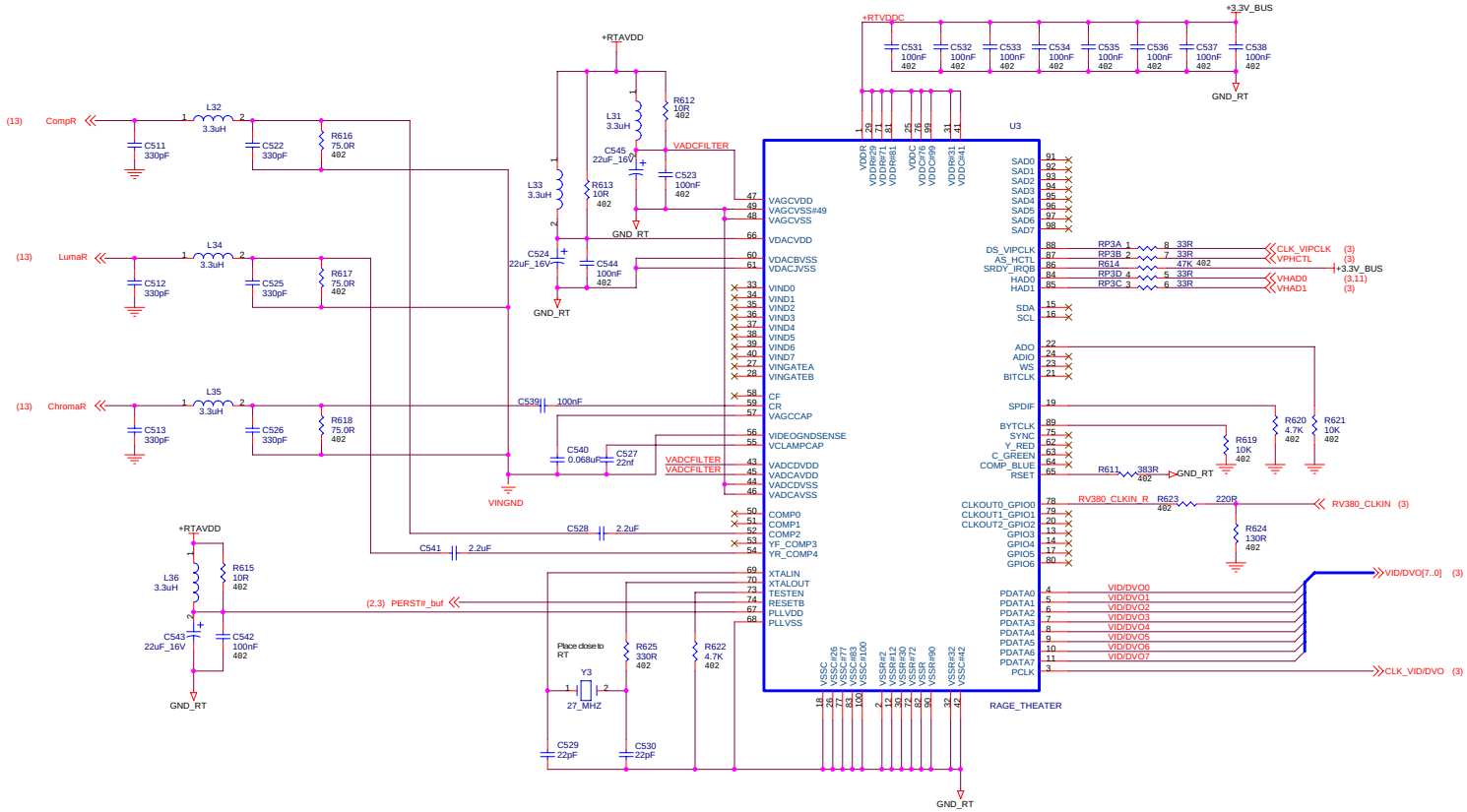


MS-V031 / ATI X550 / DDRII		
Size C	Document Number	Rev 0A
Date: Tuesday, June 28, 2005	Sheet 13 of 17	

PRIMARY DVI-I CONNECTOR



MS-V031 / ATI X550 / DDRII			
Size C	Document Number		Rev 0A
Date: Tuesday, June 28, 2005		Sheet 14 of 17	

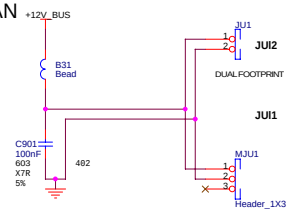


MS-V031 / ATI X550 / DDRII

Size	Document Number	Rev
C		0A

Date: Tuesday, June 28, 2005 Sheet 15 of 17

TEMPERATURE SENSE AND SPEED CONTROLLED FAN



Spring push-pin

ITW push-pin

MS-V031 / ATI X550 / DDRII		
Size C	Document Number	Rev 0A
Date: Tuesday, June 28, 2005	Sheet 16 of 17	

ASSY1

SCREW
JACKSCREW

ASSY2

SCREW
JACKSCREW

ASSY3

SCREW
JACKSCREW

ASSY4

SCREW
JACKSCREW

MISC. BOARD PARTS

ASSY5

ANTISTATIC BAG

6_X_11

REF1

ATI LOGO LABEL

ATI_LOGO_LABEL

PCB

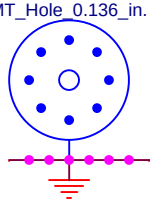
PCB

109-A51600-00B

Brack

BKT
JACKSCREW

MT1
MT_Hole_0.136_in.



FM1
SW_FB

FM2
SW_FB

FM3
SW_FB

FM4
SW_FB

FM5
SW_FB

FM6
SW_FB

MS-V031 / ATI X550 / DDRII

Size	Document Number	Rev
A		0A

Date: Monday, June 27, 2005 Sheet 17 of 17