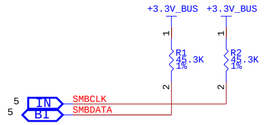
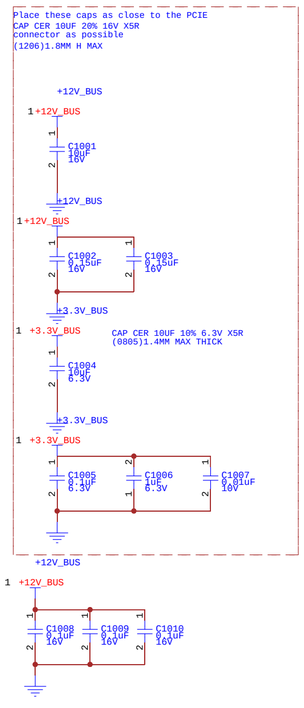
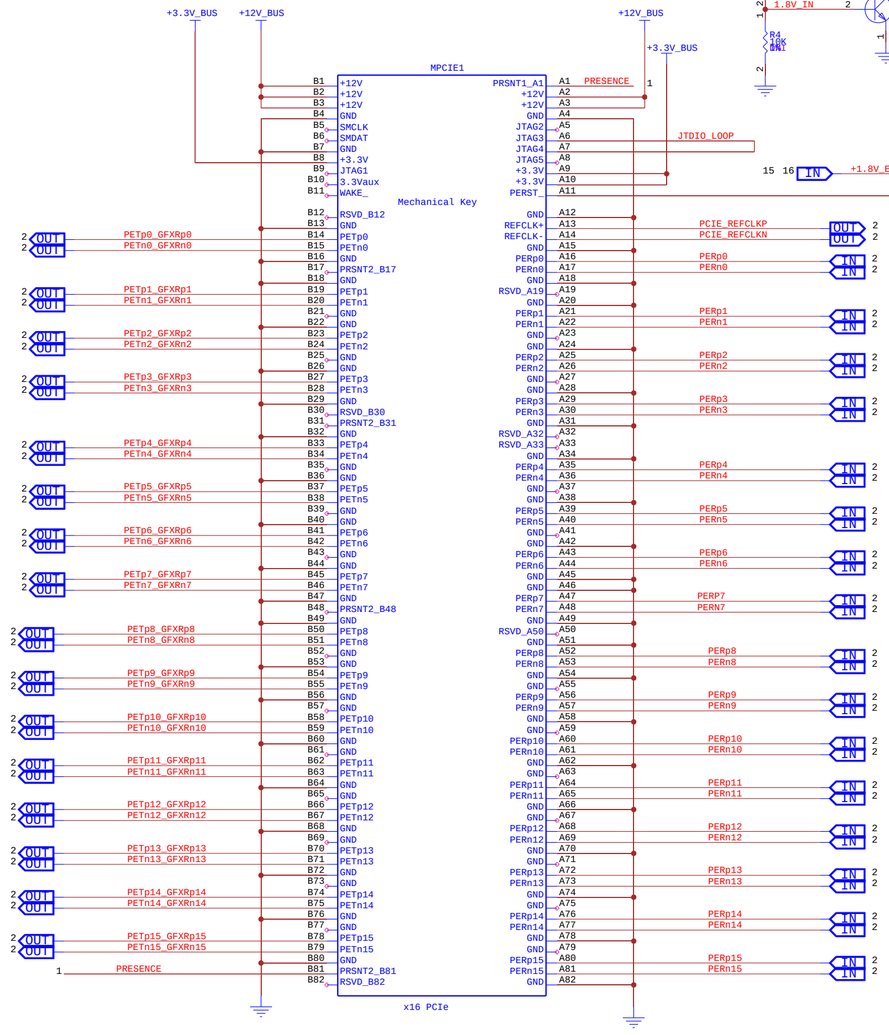
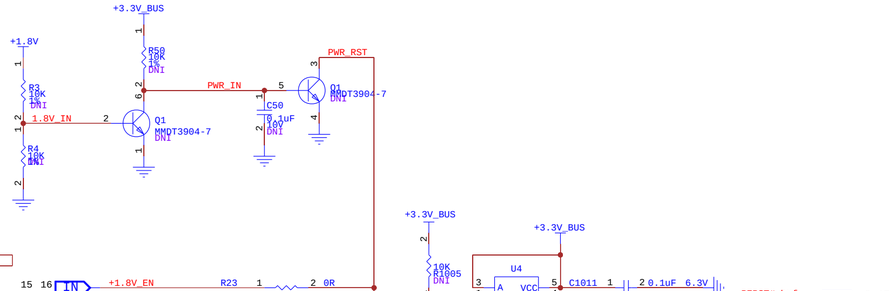
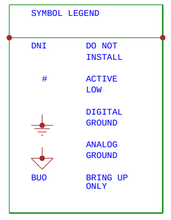
PCI-EXPRESS EDGE CONNECTOR









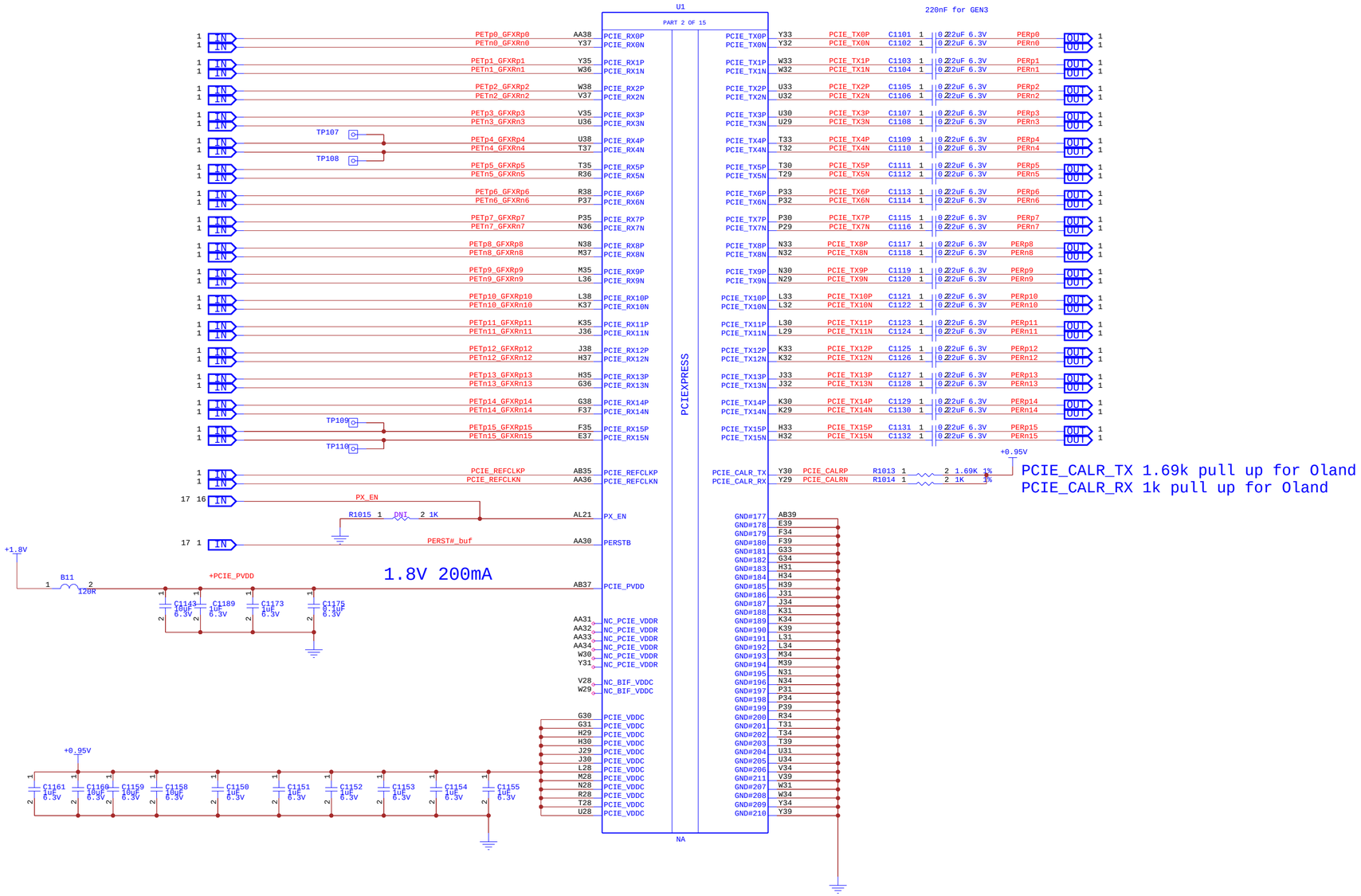


AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: PCI-E Edge Connector	
DATE: Wed Apr 27 16:35:17 2016	REV: 1.0
SHEET NUMBER: 1 OF 21	
DOCUMENT NUMBER: 105_D039xx_00A	
	TITLE: TITLE

Verde PCIe Interface

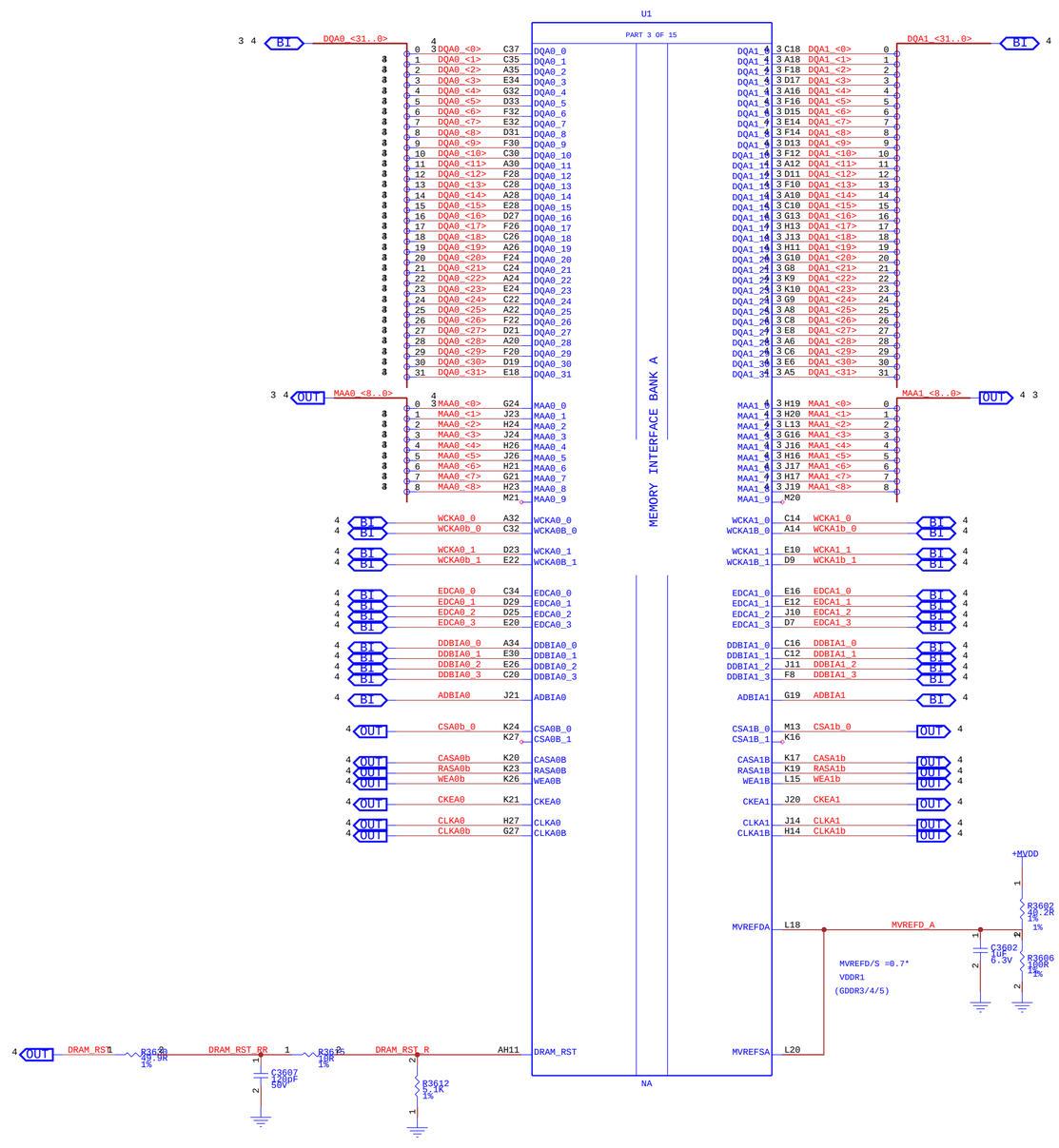
NOTE: Some of the PCIE testpoints will

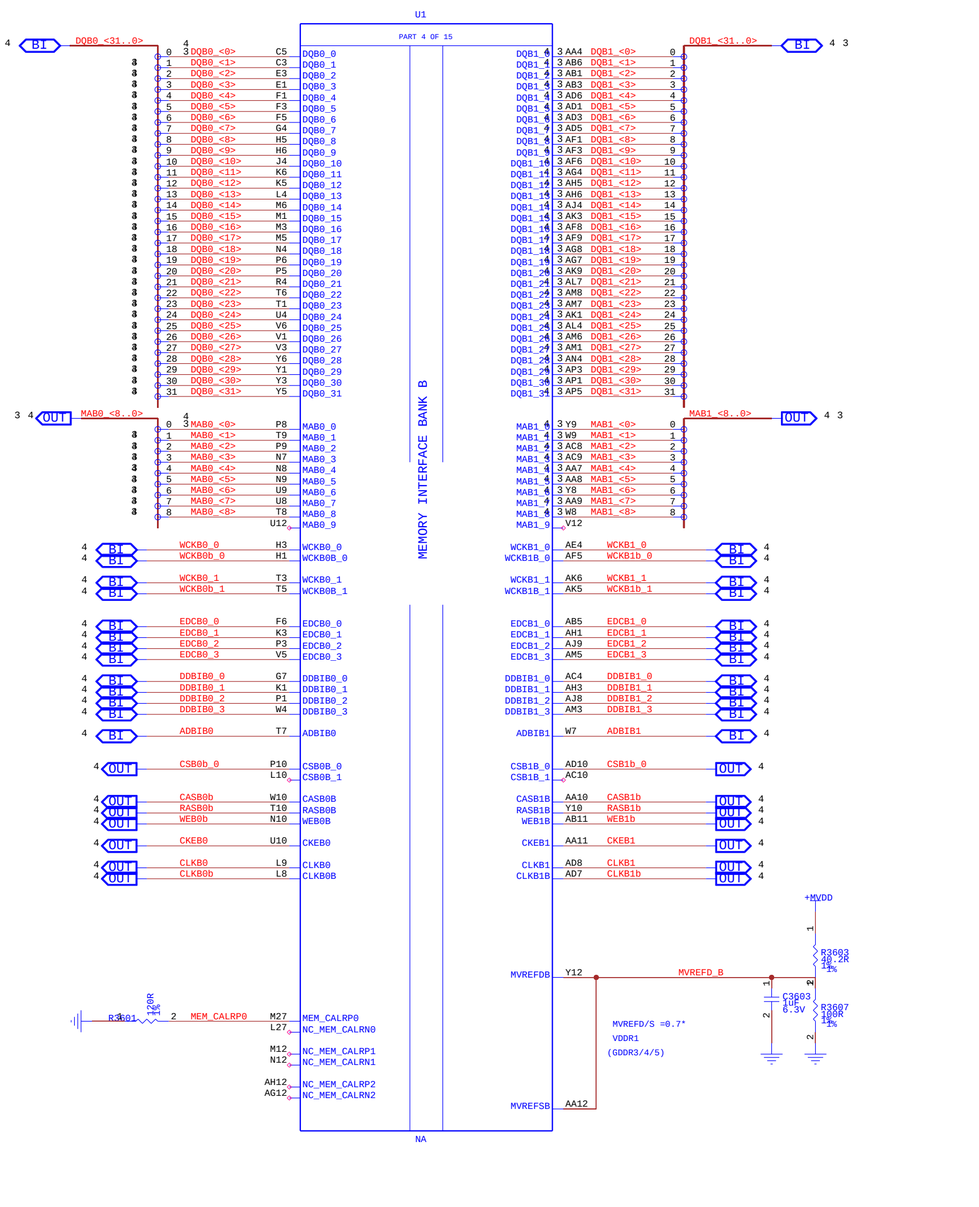
be available through vias on traces.



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: Cape Verde PCIE Interface	
DATE: Wed Apr 27 16:35:27 2016	REV: 1.0
SHEET NUMBER: 2 OF 21	
DOCUMENT NUMBER: 105_D039xx_00A	TITLE: TITLE

(3) Verde MEM Interface Ch A&B





AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Cape Verde MEMORY INTERFACE

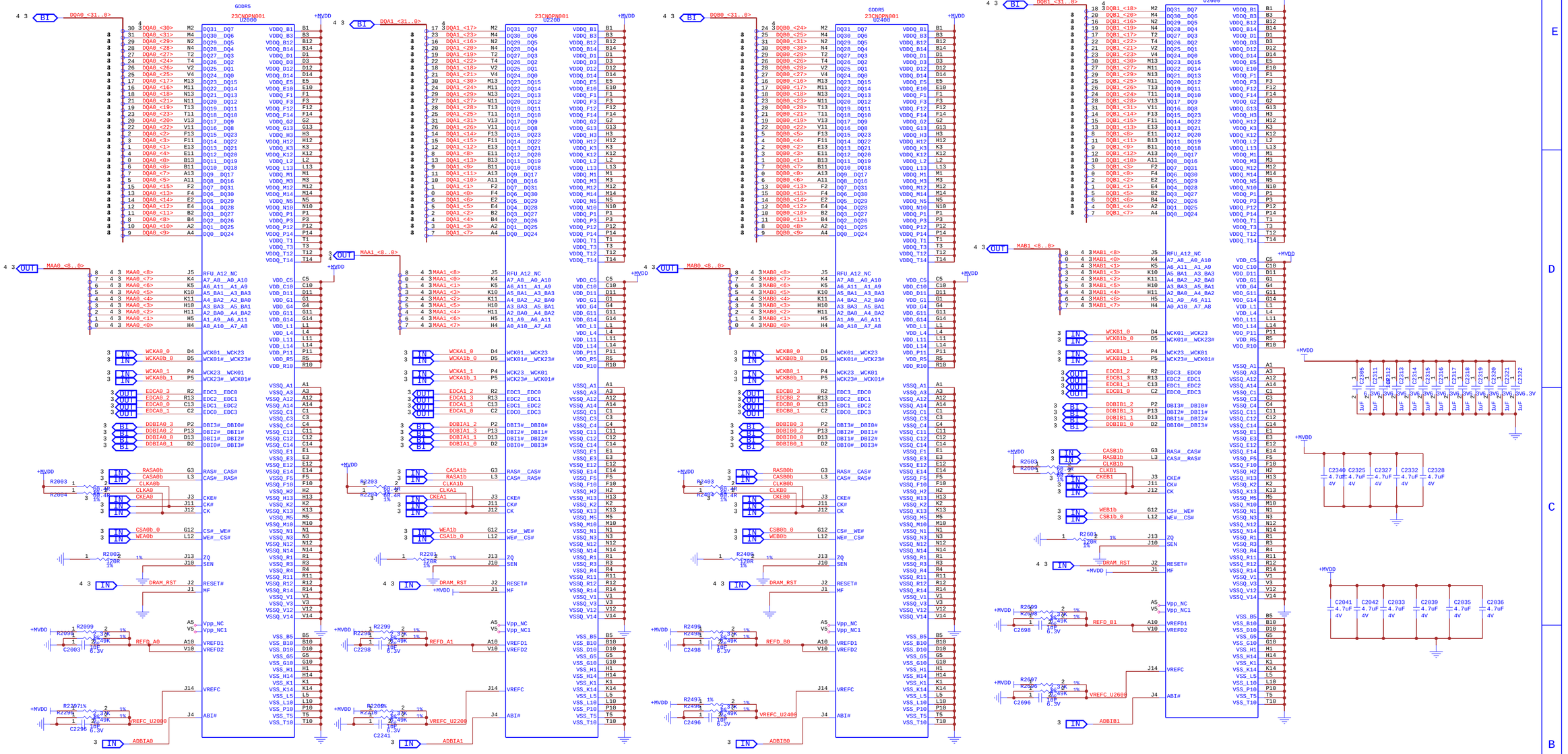
DATE: Wed Apr 27 16:35:28 2016 REV: 1.0

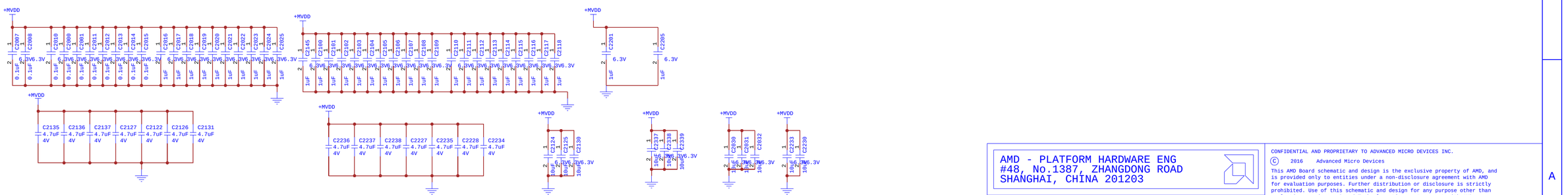
SHEET NUMBER: 3 OF 21

DOCUMENT NUMBER: 105_D039xx_00A

TITLE:
TITLE

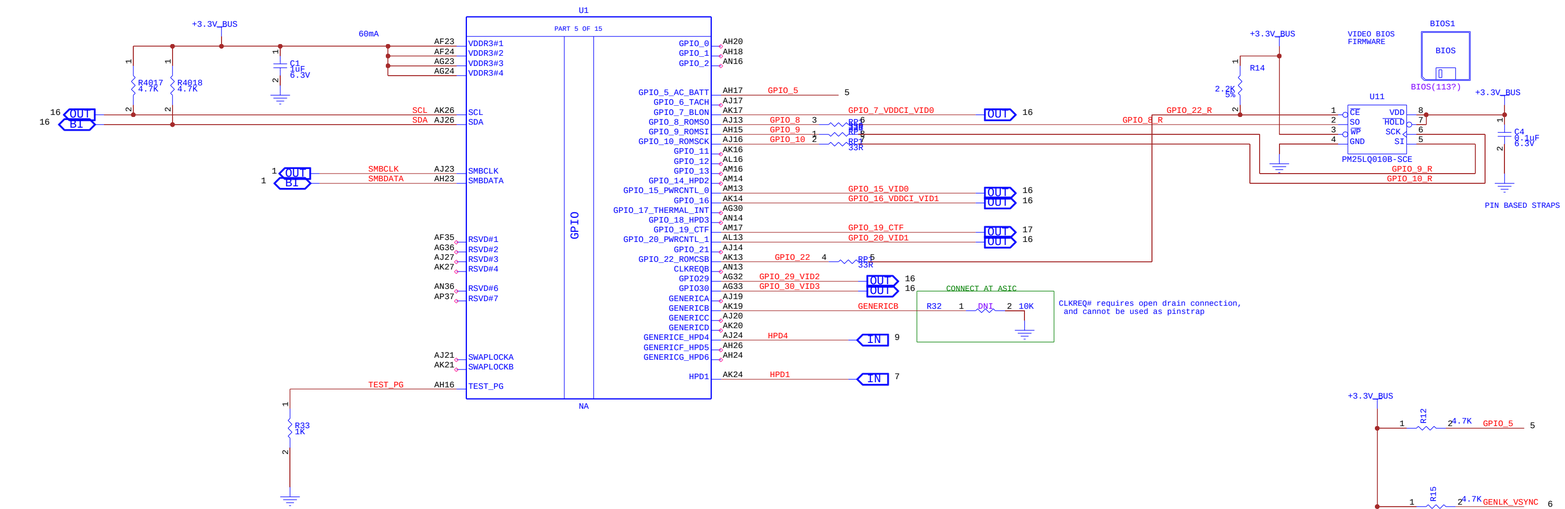
(4) GDDR5 Memory Channel A&B



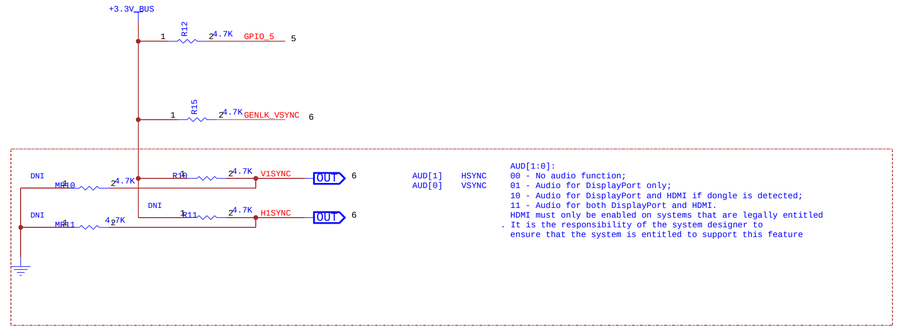


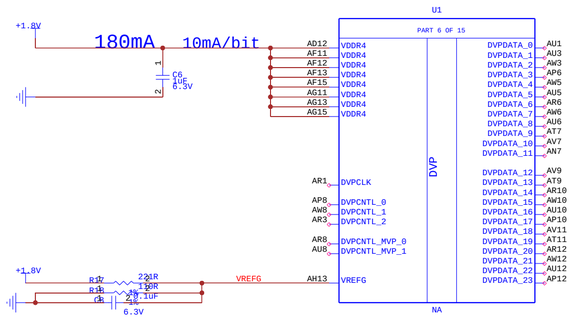
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. © 2016 Advanced Micro Devices This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.
SHEET: GDDR5 CHA&B	
DATE: Wed Apr 27 16:35:20 2016 REV: 1.0	
SHEET NUMBER: 4 OF 21	
DOCUMENT NUMBER: 105_D039xx_00A	
NOTES: NOTE	TITLE: TITLE

Verde GPIOs Strap CF XTAL OSC



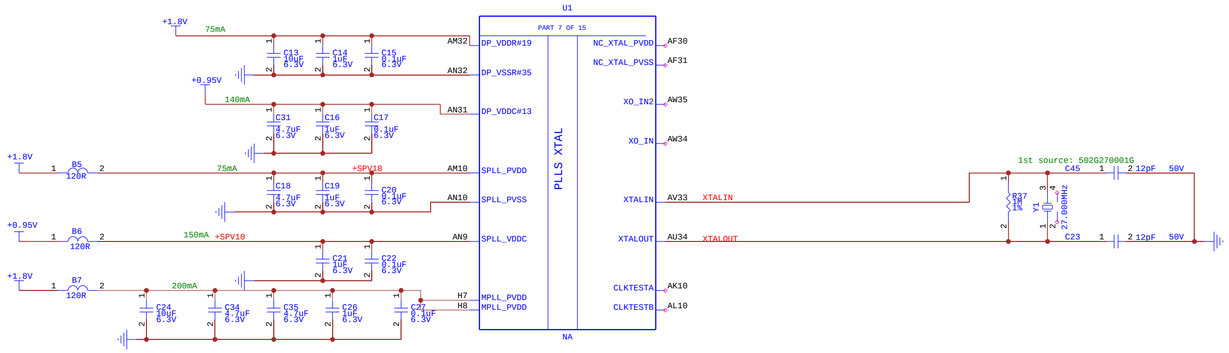
PN 2280007000G for 1Mbit (PM25LV010A-100SCE)





Place the crossfire testpoints near the ASIC and not the connector

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.



AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Cape Verde GPIO STRAP PLL

DATE: Wed Apr 27 16:35:23 2016 REV: 1.0

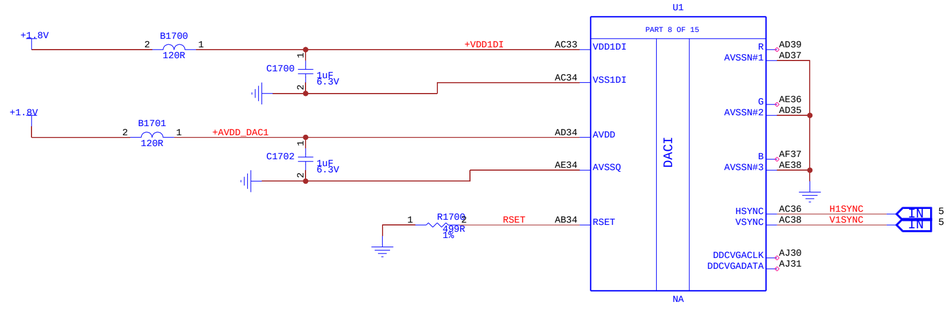
SHEET NUMBER: 5 OF 21

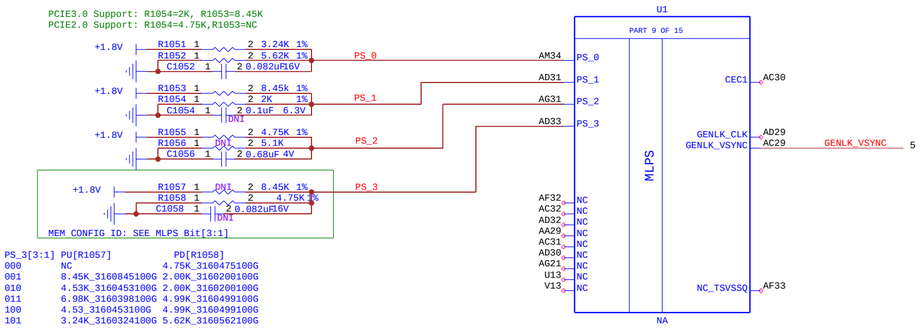
DOCUMENT NUMBER: 105_D039xx_00A

NOTES: NOTE

TITLE:

TITLE





PS_3[3:1]	PU[R1057]	PD[R1058]
000	NC	4.75K_3160475100G
001	8.45K_31608451006	2.00K_3160200100G
010	4.53K_3160453100G	2.00K_3160200100G
011	6.98K_3160398100G	4.99K_3160499100G
100	4.53_3160453100G	4.99K_3160499100G
101	3.24K_31603241006	5.62K_3160562100G
110	3.40K_3160340100G	10.0K_3160100200G
111	4.75K_3160475100G	NC

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Cape Verde DAC and MLPS

DATE: Wed Apr 27 16:35:29 2016 REV: 1.0

SHEET NUMBER: 6 OF 21

DOCUMENT NUMBER: 105_D039xx_00A

NOTES: NOTE

TITLE:

TITLE

CAPE VERDE TMDP A HDMI

U1
PART 10 OF 15
TMDP A/B
NA

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

+0.95V
C2515 4.7uF 6.3V
C2516 1uF 6.3V
C2517 0.1uF 10V

AU28 NC_DP_VDDR#10
AV27 DP_VSSR
AV29 NC_DP_VDDR#12
AR28 DP_VSSR
AP31 DP_VDDC
AP32 DP_VDDC
AN33 DP_VDDC
AP33 DP_VDDC
AN24 NC_DP_VDDR#1
AP24 NC_DP_VDDR#6
AP25 NC_DP_VDDR#7
AP26 NC_DP_VDDR#8
R2540 10K 1%
DPAB_CALR AW28 DPAB_CALR
AN27 DP_VSSR
AP27 DP_VSSR
AP28 DP_VSSR
AW24 DP_VSSR
AW26 DP_VSSR
AN29 DP_VSSR
AP29 DP_VSSR
AP30 DP_VSSR
AW30 DP_VSSR
AW32 DP_VSSR

TX2P_DPA0P AT27
TX2M_DPA0N AR26
TX1P_DPA1P AU26
TX1M_DPA1N AV25
TX0P_DPA2P AT25
TX0M_DPA2N AR24
TXCAP_DPA3P AU24
TXCAM_DPA3N AV23
AUX1P AM27
AUX1N AL27
DDC1CLK AM26
DDC1DATA AN26
TX5P_DPB0P AT33 DPB_B0P 7
TX5M_DPB0N AU32 DPB_B0N 7
TX4P_DPB1P AR32 DPB_B1P 7
TX4M_DPB1N AT31 DPB_B1N 7
TX3P_DPB2P AV31 DPB_B2P 7
TX3M_DPB2N AU30 DPB_B2N 7
TXCBP_DPB3P AR30 DPB_B3P 7
TXCBM_DPB3N AT29 DPB_B3N 7
DDCCLK_AUX4P AL29
DDCDATA_AUX4N AM29

D1550
RCLAMP0524P
7 DPB_3N 1 A Y1 10 DPB_3N 7
7 DPB_3P 2 B Y2 9 DPB_3P 7
3 GND GND1 8
7 DPB_2N 4 C Y3 7 DPB_2N 7
7 DPB_2P 5 D Y4 6 DPB_2P 7

D1551
RCLAMP0524P
7 DPB_1N 1 A Y1 10 DPB_1N 7
7 DPB_1P 2 B Y2 9 DPB_1P 7
3 GND GND1 8
7 DPB_0N 4 C Y3 7 DPB_0N 7
7 DPB_0P 5 D Y4 6 DPB_0P 7

OPTIONAL ESD protection diodes
D2500 2 1 ESD5V3U1U-02LRH DPB_AUXP 7
D2501 2 1 ESD5V3U1U-02LRH DPB_AUXN 7
D2502 2 1 ESD5V3U1U-02LRH HPD_DPB 7
D2503 2 1 ESD5V3U1U-02LRH DPB_DONGLE_DET 7

7 IN DPB_B0P — C3530 0.1uF 6.3V DP;HDMI — 7 DPB_0P
7 IN DPB_B0N — C3531 0.1uF 6.3V DP;HDMI — 7 DPB_0N
7 IN DPB_B1P — C3532 0.1uF 6.3V DP;HDMI — 7 DPB_1P
7 IN DPB_B1N — C3533 0.1uF 6.3V DP;HDMI — 7 DPB_1N
7 IN DPB_B2P — C3534 0.1uF 6.3V DP;HDMI — 7 DPB_2P
7 IN DPB_B2N — C3536 0.1uF 6.3V DP;HDMI — 7 DPB_2N
7 IN DPB_B3P — C3537 0.1uF 6.3V DP;HDMI — 7 DPB_3P
7 IN DPB_B3N — C3538 0.1uF 6.3V DP;HDMI — 7 DPB_3N

+5V_VESA
R2701 2.2K HDMI
R2703 2.2K HDMI
7 8 BI DDCCLK_AUX5P — C3535 0.1uF 6.3V DP
8 7 BI DDCDATA_AUX5N — C3541 0.1uF 6.3V DP
8 7 IN DDCCLK_AUX5P — R2528 DNI 0R
8 7 BI DDCDATA_AUX5N — R2529 DNI 0R

Q4 2N7002DW DP;HDMI
+12V_BUS
R1804 10K DP;HDMI
R1805 10K DP
AUX4_BYPSS_EN
Q2513 MMDT3904-7
Q1804 2N7002E DP

7 DPB_DONGLE_DET
+3.3V_BUS
Q2513 MMDT3904-7
R2527 10K DP;HDMI
7 HPD_DPB
5 OUT HPD1
R2530 10K DP;HDMI

R2524 1 DP 2 1M
R2522 1 DP 2 100K
R2523 2 DP 1 100K
7 DPB_AUXP
7 DPB_AUXN
+3.3V_BUS
DPB_1M
9 +3.3V_DP
C2540 22uF 6.3V DP
R2526 1M DP

DP J2501
1 ML_Lane_0p
2 GND_0
3 ML_Lane_0n
4 ML_Lane_1p
5 GND_1
6 ML_Lane_1n
7 ML_Lane_2p
8 GND_2
9 ML_Lane_2n
10 ML_Lane_3p
11 GND_3
12 ML_Lane_3n
13 CONFIG 1
14 CONFIG 2
15 AUX_CHp
16 GND_6
17 AUX_CHn
18 Hot_Det G4 G4
20 DP_PWR G2 G2
19 PWR_RTN G1 G1
DP W/GASKET DISPLAYPORT

+5V_VESA
HDMI MJ2501
DPB_0P 1 P1 CASE 20
DPB_0N 3 P3 CASE 21
DPB_1P 4 P4 CASE 22
DPB_1N 6 P6 CASE 23
DPB_2P 7 P7
DPB_2N 9 P9
DPB_3P 10 P10
DPB_3N 12 P12
DPB_AUXP 15 P15
DPB_AUXN 16 P16
HPD_DPB 19 P19
P2 P5 P8 P11 P13 P14 P17 P18
LONG_TYPE-2_HDMI_W/TAB LONG_TYPE-2_HDMI
C2722 1UF 6.3V HDMI

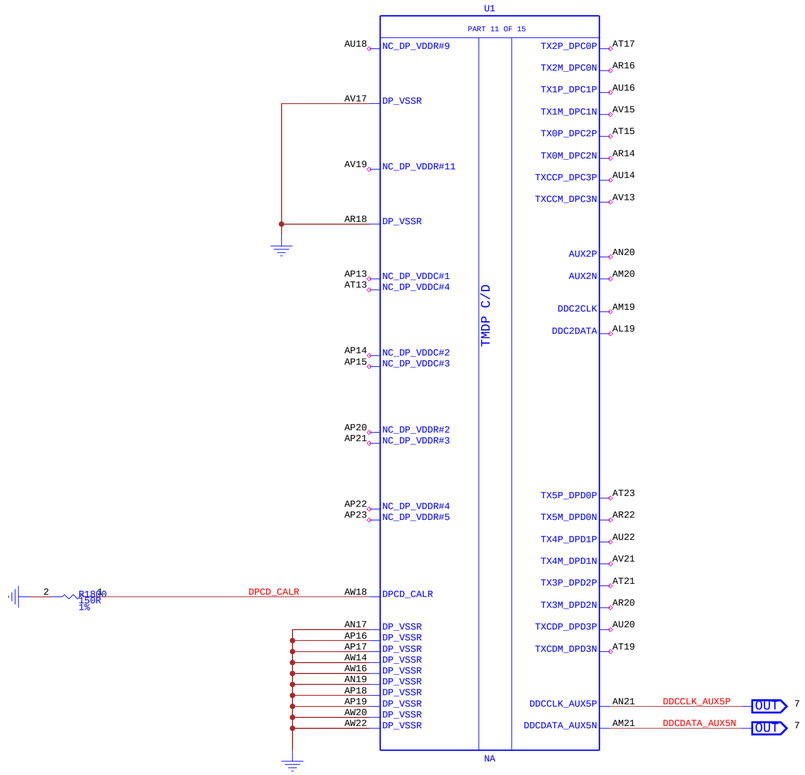
+12V_BUS
R2344 10K
TMDP_EN 1
C2344 0.1UF 16V
DPB_GND
Q2701 2N7002E HDMI

R2713 499R 1% HDMI
R2714 499R 1% HDMI
R2715 499R 1% HDMI
R2716 499R 1% HDMI
R2717 499R 1% HDMI
R2718 499R 1% HDMI
R2719 499R 1% HDMI
R2720 499R 1% HDMI

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203
OVERLAP HDMI WITH DP_D

SHEET: Cape Verde TMDP AB HDMI
DATE: Wed Apr 27 16:35:26 2016
REV: 1.0
SHEET NUMBER: 7 OF 21
DOCUMENT NUMBER: 105_D039xx_00A

TITLE:
TITLE



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: Cape Verde TMDP CD	
DATE: Wed Apr 27 16:35:30 2016	REV: 1.0
SHEET NUMBER: 8 OF 21	
DOCUMENT NUMBER: 105_D039xx_00A	

TITLE:
TITLE

CAPE VERDE LVTMDP E&F dDVI-I

PATH=I103
PART NAME=CAPE_VERDE_DDR5
PART_NUMBER=215NDNMCAPEVERDEDDR5
$LOCATION=U1

PART 12 OF 15

LVTMDP E/F

DEVICE_NAME=NA

+1.8V

+0.95V

C1520 4.7uF 6.3V
C1521 1uF 6.3V
C1522 10V 0.1uF
C1523 4.7uF 6.3V
C1524 1uF 6.3V
C1525 10V 0.1uF

AM37 DP_VDDR
AN38 DP_VSSR
AL38 DP_VDDR
AM35 DP_VSSR
AL33 DP_VDDC
AM33 DP_VDDC
AK33 DP_VDDC
AK34 DP_VDDC
AH34 DP_VDDR
AJ34 DP_VDDR
AF34 DP_VDDR
AG34 DP_VDDR

R1510 150R 1%
DPEF_CALR AM39 DPEF_CALR

AN34 DP_VSSR
AP39 DP_VSSR
AR39 DP_VSSR
AU37 DP_VSSR
AF39 DP_VSSR
AH39 DP_VSSR
AK39 DP_VSSR
AL34 DP_VSSR

T2X2P_DPE0P AP35
T2X2M_DPE0N AR35
T2X1P_DPE1P AR37
T2X1M_DPE1N AU39
T2X0P_DPE2P AW37
T2X0M_DPE2N AU35
T2XCEP_DPE3P AP34
T2XCEM_DPE3N AR34

DDCCLK_AUX3P AL30
DDCDATA_AUX3N AM30

T2X5P_DPF0P AG38 DPF_F0P
T2X5M_DPF0N AH37 DPF_F0N
T2X4P_DPF1P AH35 DPF_F1P
T2X4M_DPF1N AJ36 DPF_F1N
T2X3P_DPF2P AJ38 DPF_F2P
T2X3M_DPF2N AK37 DPF_F2N
T2XCFP_DPF3P AK35 DPF_F3P
T2XCFM_DPF3N AL36 DPF_F3N

C1822 0.1uF 6.3V
C1823 0.1uF 6.3V
C1824 0.1uF 6.3V
C1825 0.1uF 6.3V
C1826 0.1uF 6.3V
C1827 0.1uF 6.3V
C1828 0.1uF 6.3V
C1829 0.1uF 6.3V

DDCCLK_AUX6P AK30 DDCCLK_AUX6P
DDCDATA_AUX6N AK29 DDCDATA_AUX6N

C1830 0.1uF 6.3V
C1831 0.1uF 6.3V

Q1800 2N7002DW
Q1801 2N7002DW

AUX6_BYPASS_EN

+12V_BUS
R1857 10K
Q1808 MMDT3904-7
R1855 10K
Q1803 2N7002

+3.3V_BUS
Q1809 MMDT3904-7
R1824 10K
R1815 10K
HPD_DPF
HPD4
OUT

To use Mini DP: 6141073900G
Watch out for spacing and Bracket
due to connectors' spring

J1801
DP_RECEPTACLE_W/TAB

1	ML_Lane_0p	9	DPF_0P
2	GND_0		
3	ML_Lane_0n	9	DPF_0N
4	ML_Lane_1p	9	DPF_1P
5	GND_1		
6	ML_Lane_1n	9	DPF_1N
7	ML_Lane_2p	9	DPF_2P
8	GND_2		
9	ML_Lane_2n	9	DPF_2N
10	ML_Lane_3p	9	DPF_3P
11	GND_3		
12	ML_Lane_3n	9	DPF_3N
13	CONFIG 1	9	DPF_DONGLE_DET
14	CONFIG 2		
15	AUX_CHp	9	DPF_AUXP
16	GND_6		
17	AUX_CHn	9	DPF_AUXN
18	Hot_Det		
19	PWR_RTN		
20	DP_PWR	+3.3V_DP	
G4	G3	G2	G1

R1820 1M
R1821 100K
R1822 100K
+3.3V_BUS
+3.3V_BUS
F1800 1.5A
C1833 22uF 6.3V
R1813 5.1M

OPTIONAL ESD PROTECTION DIODES

D1801 RCLAMP0524P

9 DPF_0P	5	D	Y4	6	DPF_0P 9
9 DPF_0N	4	C	Y3	8	DPF_0N 9
	3	GND	GND1	9	
9 DPF_1P	2	B	Y2	10	DPF_1P 9
9 DPF_1N	1	A	Y1		DPF_1N 9

D1803 RCLAMP0524P

9 DPF_2P	5	D	Y4	6	DPF_2P 9
9 DPF_2N	4	C	Y3	8	DPF_2N 9
	3	GND	GND1	9	
9 DPF_3P	2	B	Y2	10	DPF_3P 9
9 DPF_3N	1	A	Y1		DPF_3N 9

D1807 ESD5V3U1U-02LRH DPF_AUXN 9
D1806 ESD5V3U1U-02LRH DPF_AUXP 9
D1804 ESD5V3U1U-02LRH DPF_DONGLE_DET 9
D1812 ESD5V3U1U-02LRH HPD_DPF 9

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Cape Verde TMDP EF DP

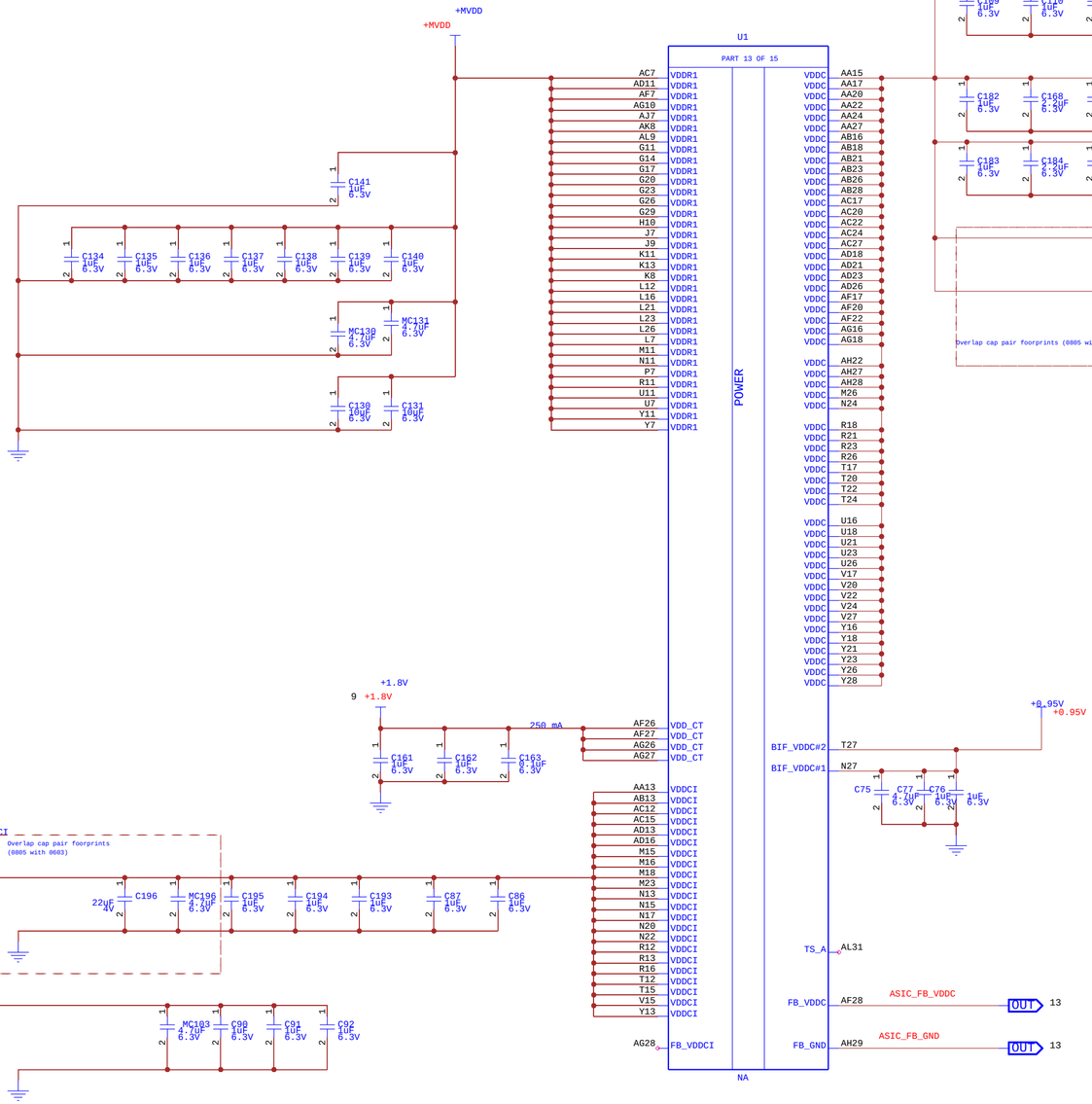
DATE: Wed Apr 27 16:35:25 2016 REV: 1.0

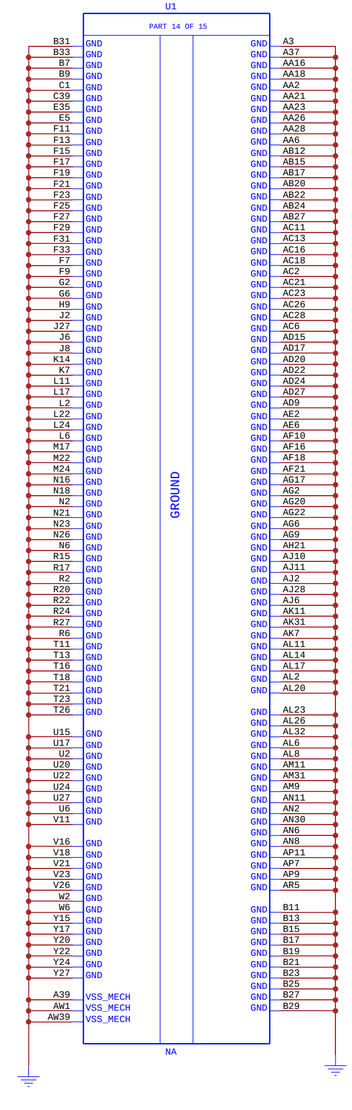
SHEET NUMBER: 9 OF 21

DOCUMENT NUMBER: 105_D039xx_00A

TITLE:
TITLE

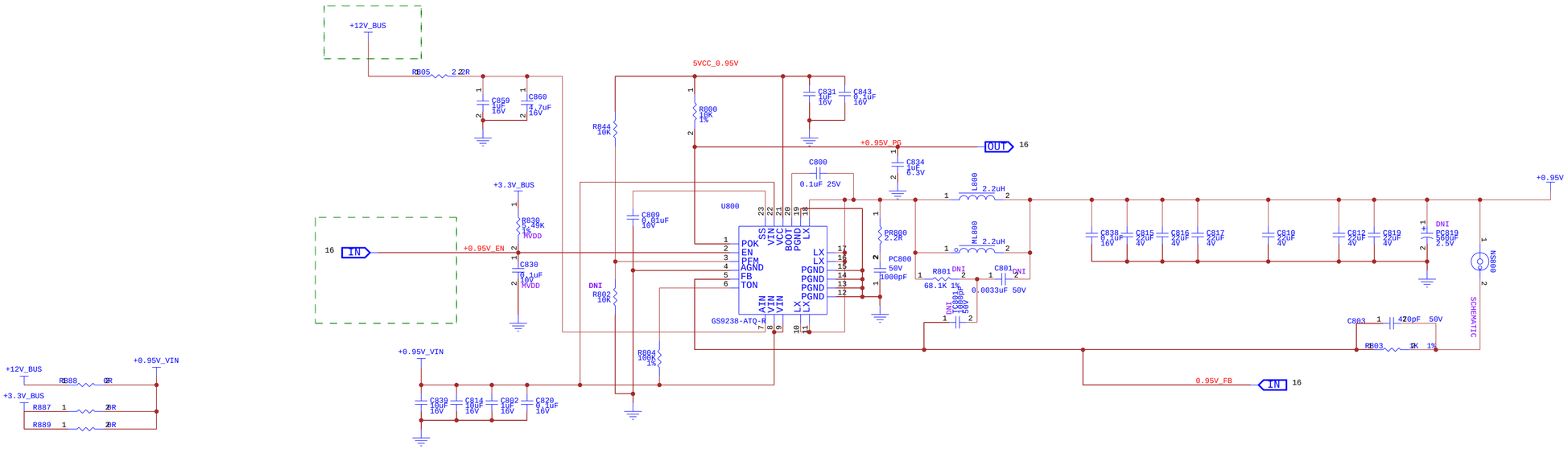
Verde Power & GND





AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: Cape Verde Power&GND	
DATE: Wed Apr 27 16:35:29 2016	REV: 1.0
SHEET NUMBER: 10 OF 21	
DOCUMENT NUMBER: 105_D039xx_00A	TITLE: TITLE

(17) 0.95V

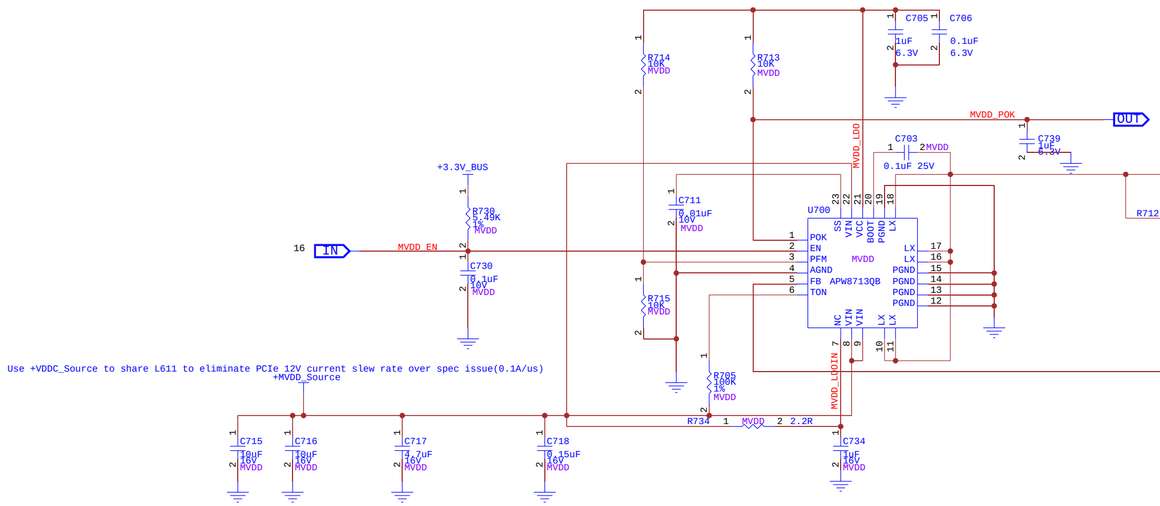


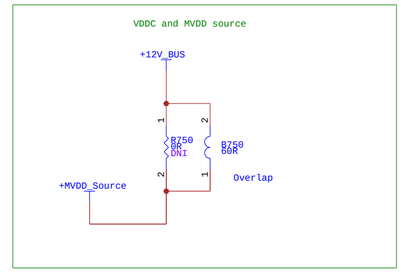
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: 0.95V	
DATE: Wed Apr 27 16:35:24 2016	REV: 1.0
SHEET NUMBER: 11 OF 21	
DOCUMENT NUMBER: 105_D039xx_00A	
NOTES: NOTE	

TITLE:

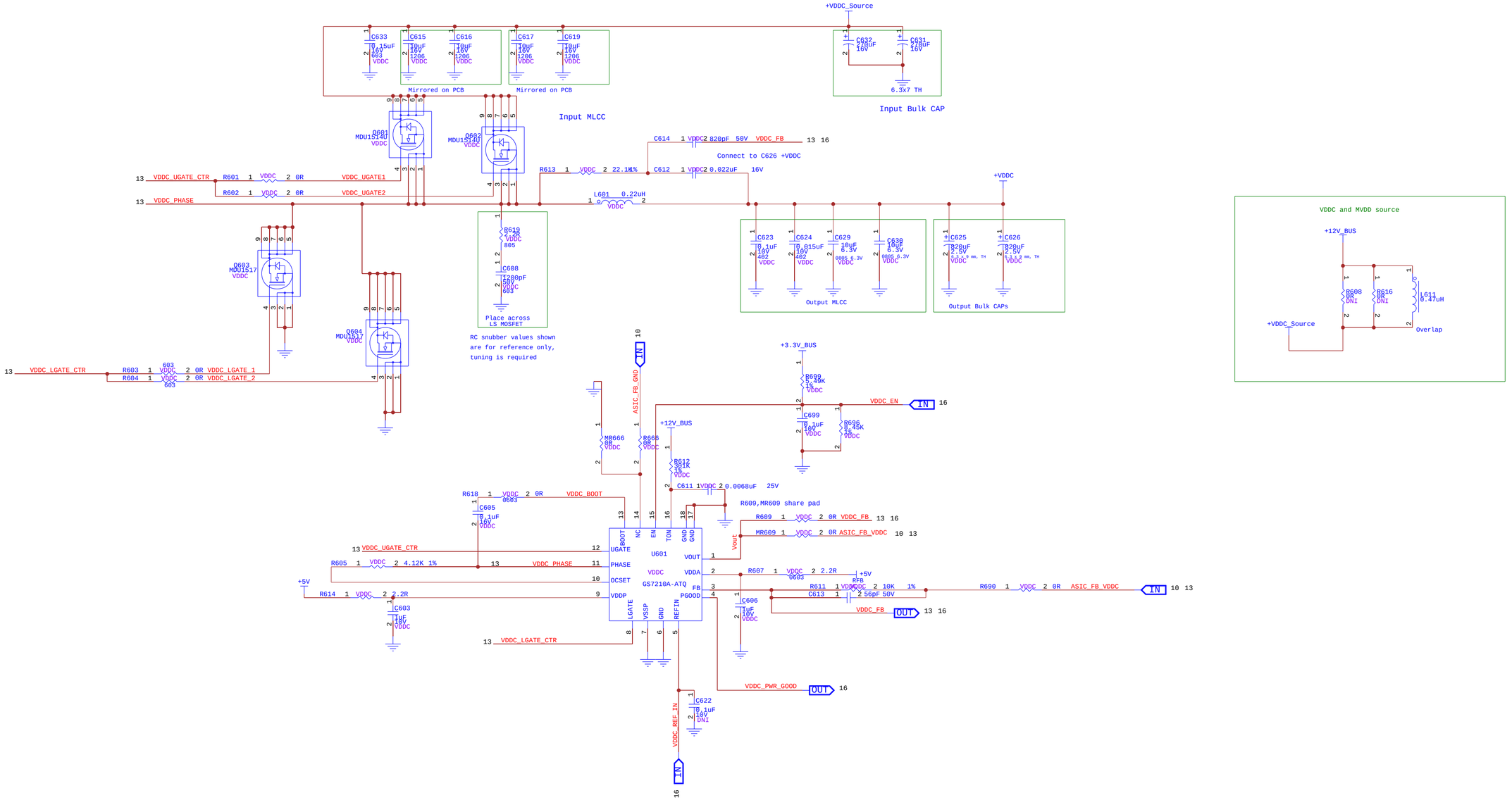
TITLE

Regulator for MVDD





AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: MVDD	
DATE: Wed Apr 27 16:35:23 2016	REV: 1.0
SHEET NUMBER: 12 OF 21	
DOCUMENT NUMBER: 105_D039xx_00A	TITLE: TITLE



AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: VDDC

DATE: Wed Apr 27 16:35:26 2016 REV: 1.0

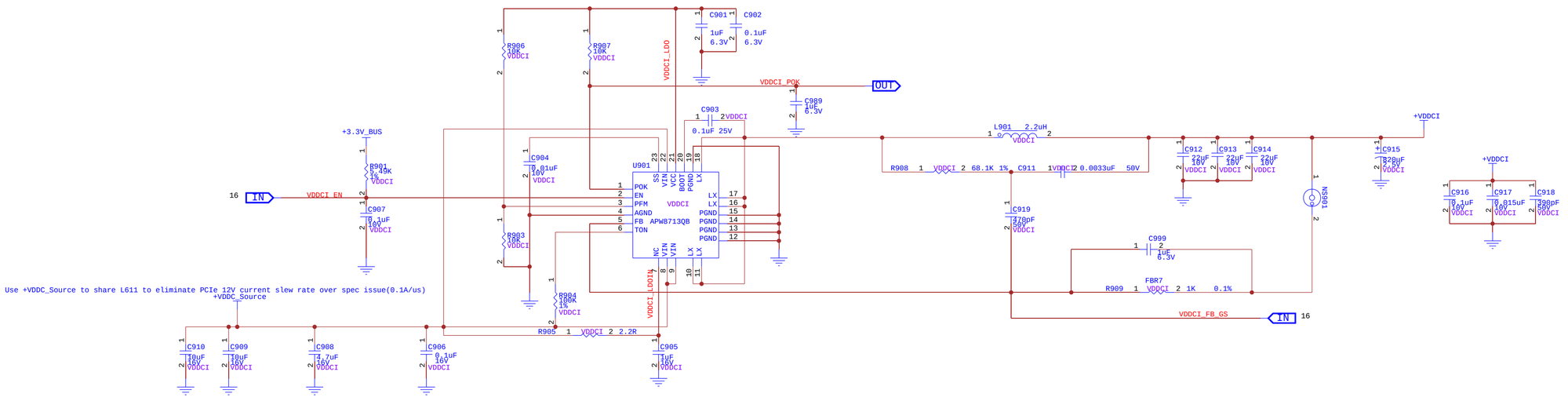
SHEET NUMBER: 13 OF 21

DOCUMENT NUMBER: 105_D039xx_00A

TITLE:

TITLE

Regulator for MVDD



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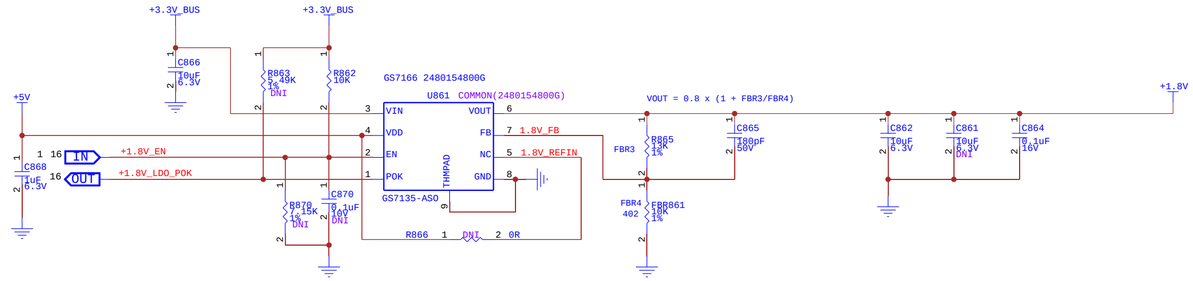
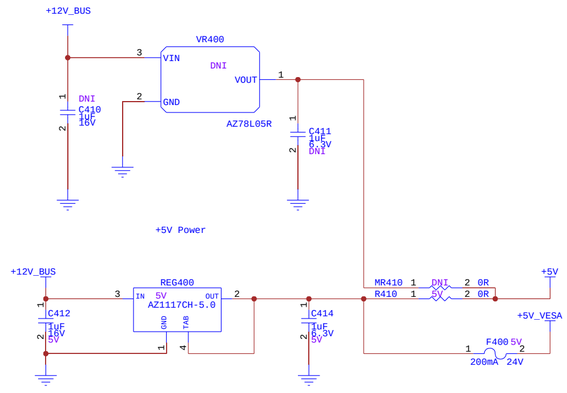
SHEET: VDDCI	
DATE: Wed Apr 27 16:35:24 2016 / REV: 1.0	
SHEET NUMBER: 14 OF 21	TITLE: TITLE
DOCUMENT NUMBER: 105_D039xx_00A	
NOTES: NOTE	

Linear Regulators

LDO #2: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling





AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Linear Regulators

DATE: Wed Apr 27 16:35:24 2016 REV: 1.0

SHEET NUMBER: 15 OF 21

DOCUMENT NUMBER: 105_D039xx_00A

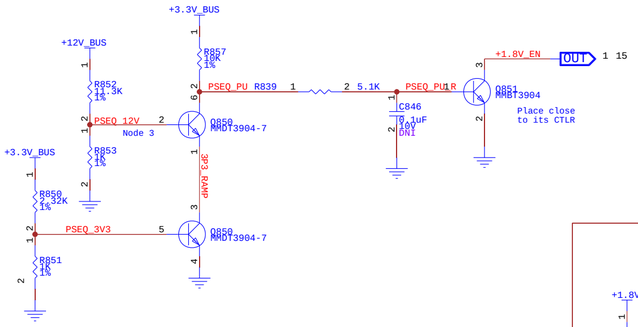
TITLE:

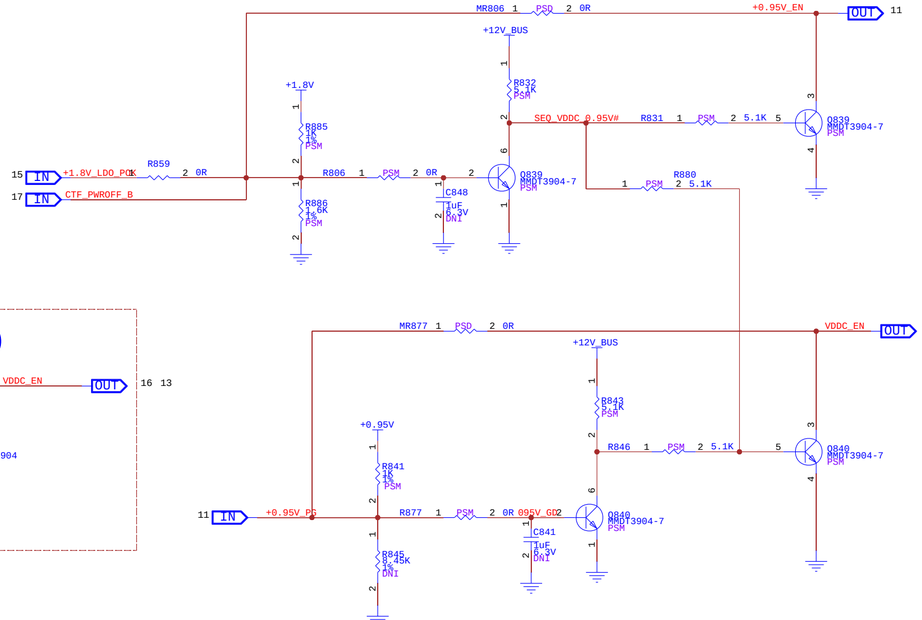
TITLE

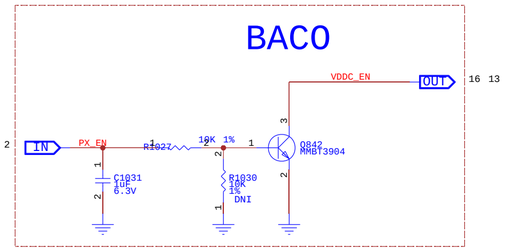
Power Management - Power Gating and Dynamic Voltage Control

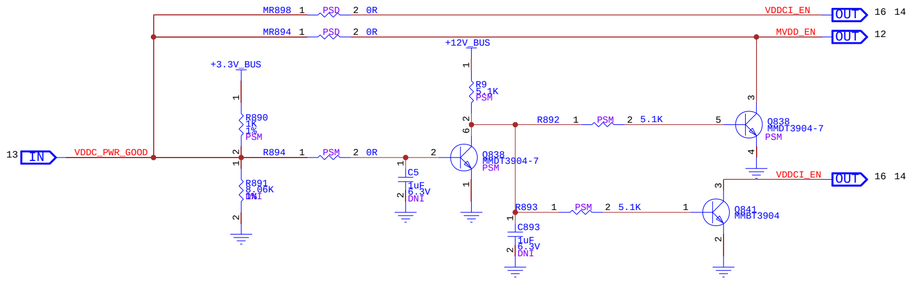
POWER SEQUENCE
+1.8V-2.8ms->MVDD-3.4ms->0.95V-4.3ms->VDDC

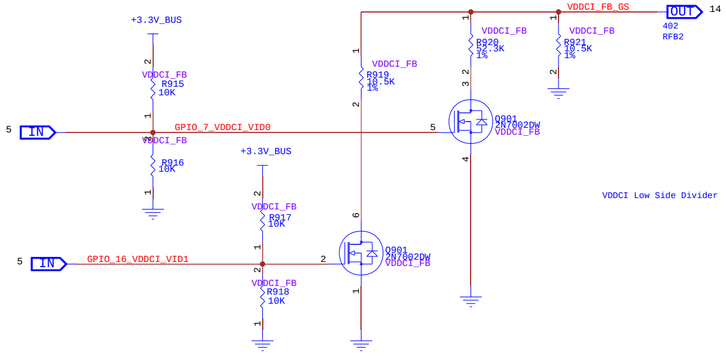
0.95V must ramp up before VDDC



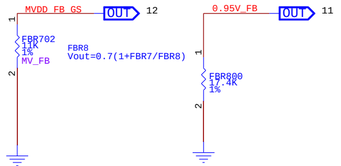




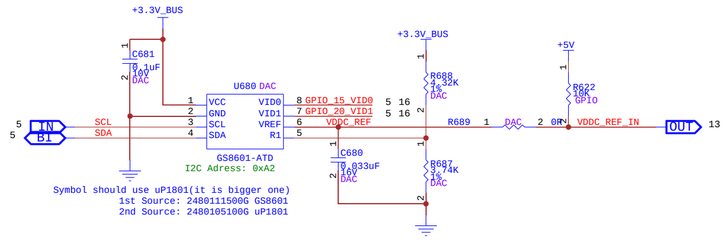




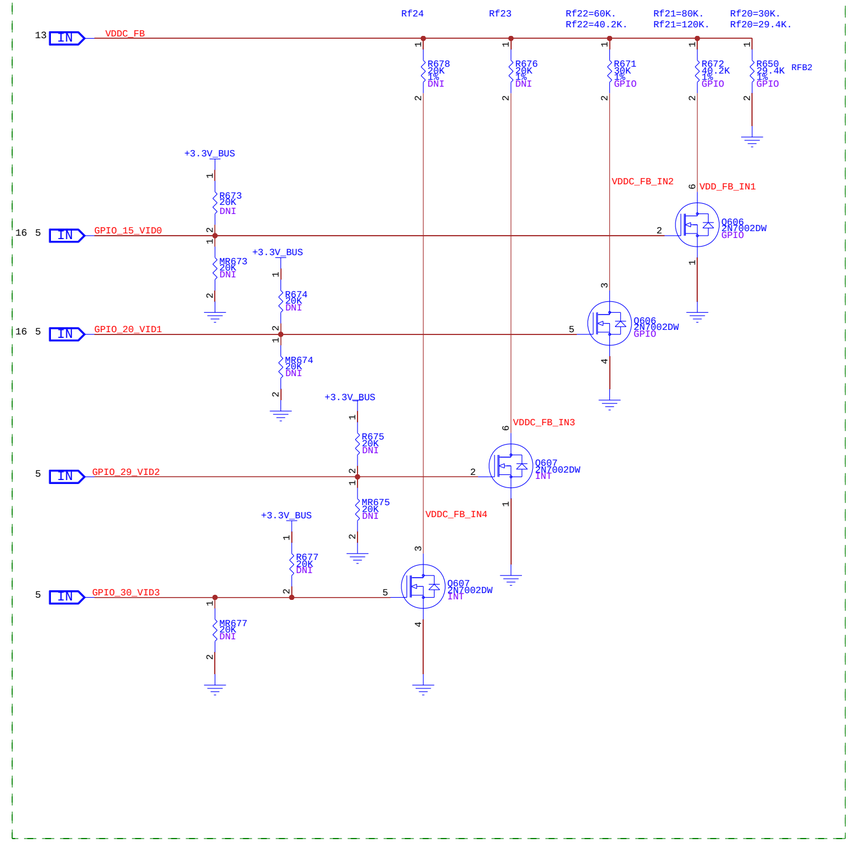
VDDCI Low Side Divider



VDDC Low Side Divider



Symbol should use uP1801(it is bigger one)
1st Source: 24801115006 GS8601
2nd Source: 24801051006 uP1801

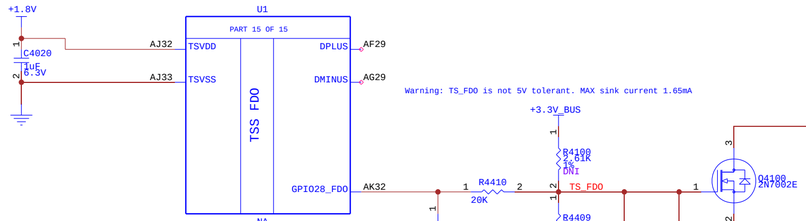


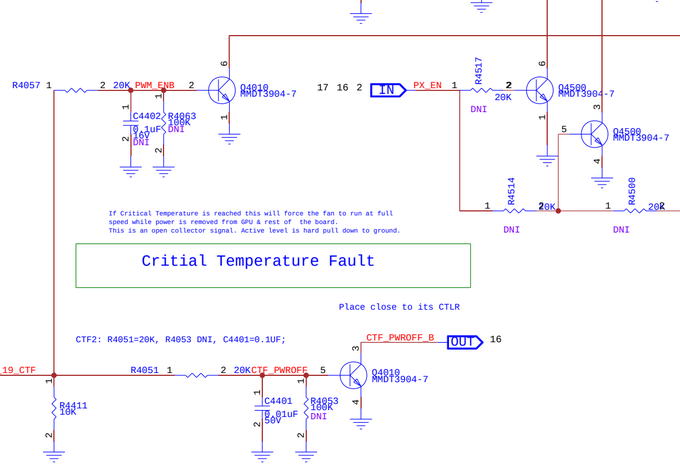
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203		
SHEET: PWR MGMT & SEQ		
DATE: Wed Apr 27 16:35:21 2016	REV: 1.0	
SHEET NUMBER: 16 OF 21		
DOCUMENT NUMBER: 105_D039xx_00A		

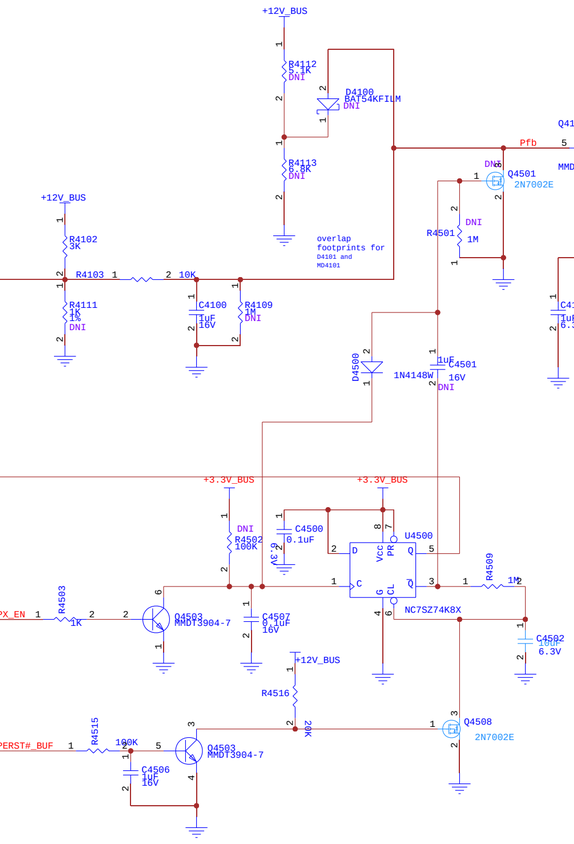
TITLE:
TITLE

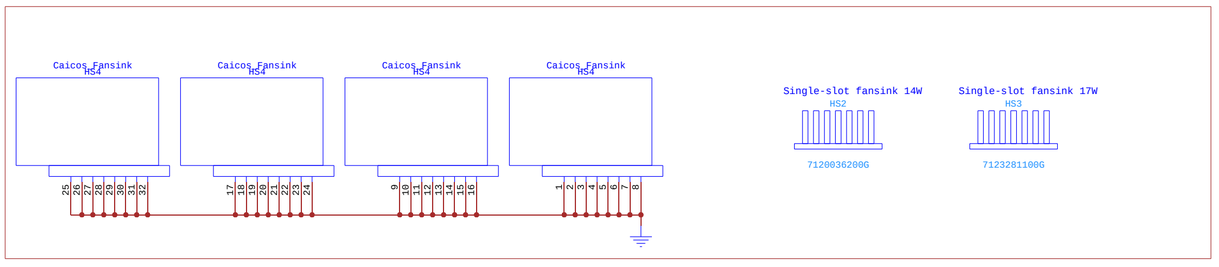
Mechanical and Thermal Management

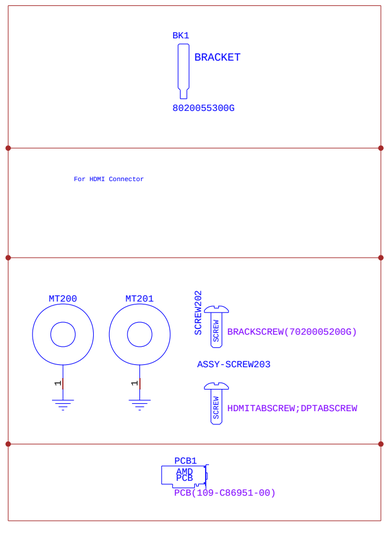
Install R4520	GPIO6 is 0: Fan stop GPIO6 is PWM: Fan running
Install R4516 Q4511,R4519	GPIO6 is 1: Fan stop GPIO6 is PWM: Fan running



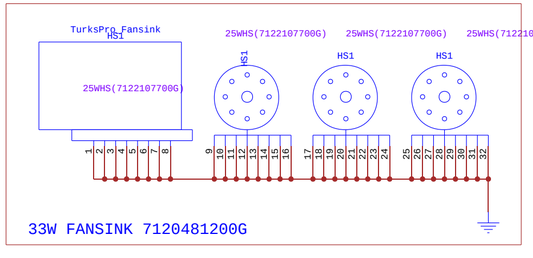








Bracket, HDMI, DP	80200055200G
Bracket, DP, DP	80200552A0G



Rectangular Heatsink 8W

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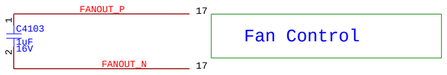
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

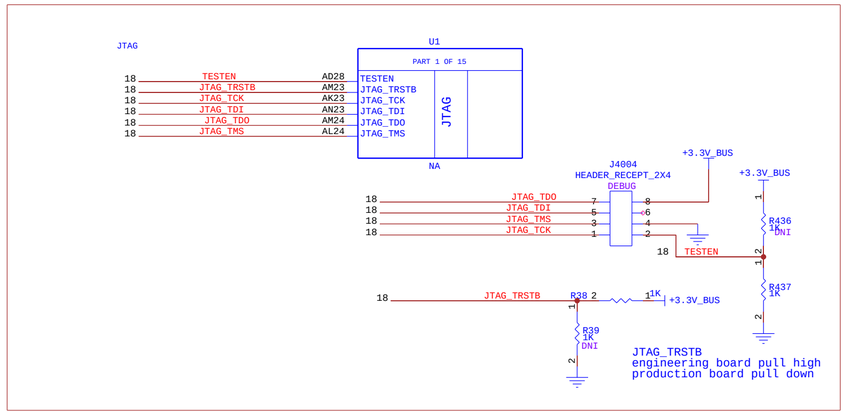
SHEET:	Mech/Thermal Management	
DATE:	Wed Apr 27 16:35:22 2016	REV: 1.0
SHEET NUMBER:	17 OF 21	
DOCUMENT NUMBER:	105_D039xx_00A	
TITLE:	TITLE	

Fan Control



This circuit provides a minimum voltage for the fan, independent of PWM input -> check if needed for RV710

(19) Debug Circuits



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#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Debug Circuit

DATE: Wed Apr 27 16:35:29 2016 REV: 1.0

SHEET NUMBER: 18 OF 21

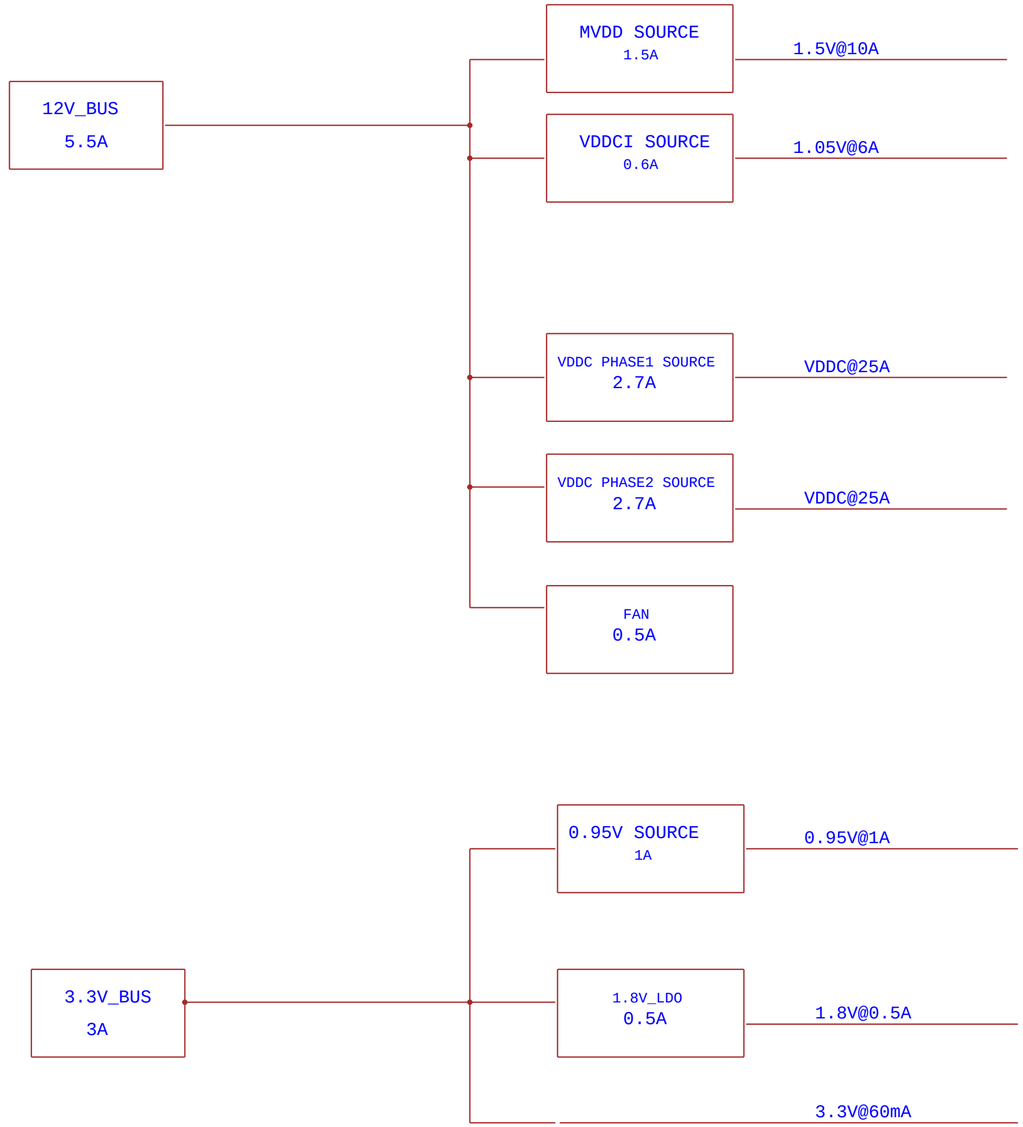
DOCUMENT NUMBER: 105_D039xx_00A

TITLE:

TITLE

DVI-I	HPD4	DDC/AUX4
HDMI	HPD1	DDC/AUX1
DP	HPD3	DDC/AUX5

GPIO15	VDDC_VID0	
GPIO20	VDDC_VID1	
GPIO7	VDDCI_VID	DEFAULT 1
GPIO5	VR_HOT	



AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: GPIO DDC HPD map

DATE: Tue Dec 04 11:46:00 2012 REV: 1.0

SHEET NUMBER: 19 OF 21

DOCUMENT NUMBER: 105_D039xx_00A

NOTES: NOTE

TITLE:

TITLE

Debug

MEMORY CHANNEL A & B

GDDR5 4pcs 128Mx32 (2GB)

CH A&B

JTAG/I2C

GPIO

POWER REGULATORS

From +12V

+VDDC
+MVDD
FAN

From +12V LINEAR:

+5V_VESA, +5V_VESA2

From +12V_BUS

+5V

From +3.3V_BUS converter(+0.95V):

PCIE_VDDC, DPLL_VDDC,
DPx_VDD10, SPV10, MEM_VREF

From +3.3V Direct:

VDDR3, AVDD

From 3.3V Linear (1.8V)

PCIE_PVDD, PCIE_VDDR, VDDR4,
DPLL_PVDD, SPV18, MPV18,
VDD1DI, VDD2DI, AVDD, AVDDQ,
DPx_PVDD, DPx_VDD18, VDD_CT,
TSVDD

Straps

ROM

BIOS

Thermal

Speed control
& temperature
sense

FAN

DDC
GPIO17
D+/D-
TS_FDO

INTERRUPT
Temp. Sensing
Built-in PWM

Dynamic Power Management

POWER DELIVERY

Verde

TMDP-A

SL TMDS

AC Coupling Caps

HDMI
Connector

5V_VESA

AUXDDC2

HPD1

DisplayPort
Connector

Overlap

TMDPB

DL TMDS

AC Coupling Caps

sDVI-I

Connector

5V_VESA

DACVGA

RGB Filters

AUXDDC1

HPD2

XO_IN2

XO_IN

XTALIN

VGA CONN

Temperature Critical

CTF

PCI-Expressx8

27MHz

Xtal

Power Sequencing
Circuit

+3.3V_BUS
+12V_BUS

PCI-Express Bus

Verde GDDR5 2GB
HDMI/DP SL-DVI-I

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#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: BLOCK DIAGRAM

DATE: Wed Apr 27 14:19:15 2016

REV: 1.0

SHEET NUMBER: 20 OF 21

DOCUMENT NUMBER: 105_D039xx_00A

TITLE:

TITLE

AMD

TITLE: TITLE

DOCUMENT NUMBER: 105_D039xx_00A

DATE: Wed Apr 27 14:08:27 2016

SHEET NUMBER: 21 OF 21

REV: 1.0

REVISION HISTORY

ENGINEER: XXX

NOTES: NOTE

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#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
1.00	00A	04/27/16	1. Initial release