

©

REV: 2.0

TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP

DOCUMENT NUMBER: 105-C869:xx-00B

11

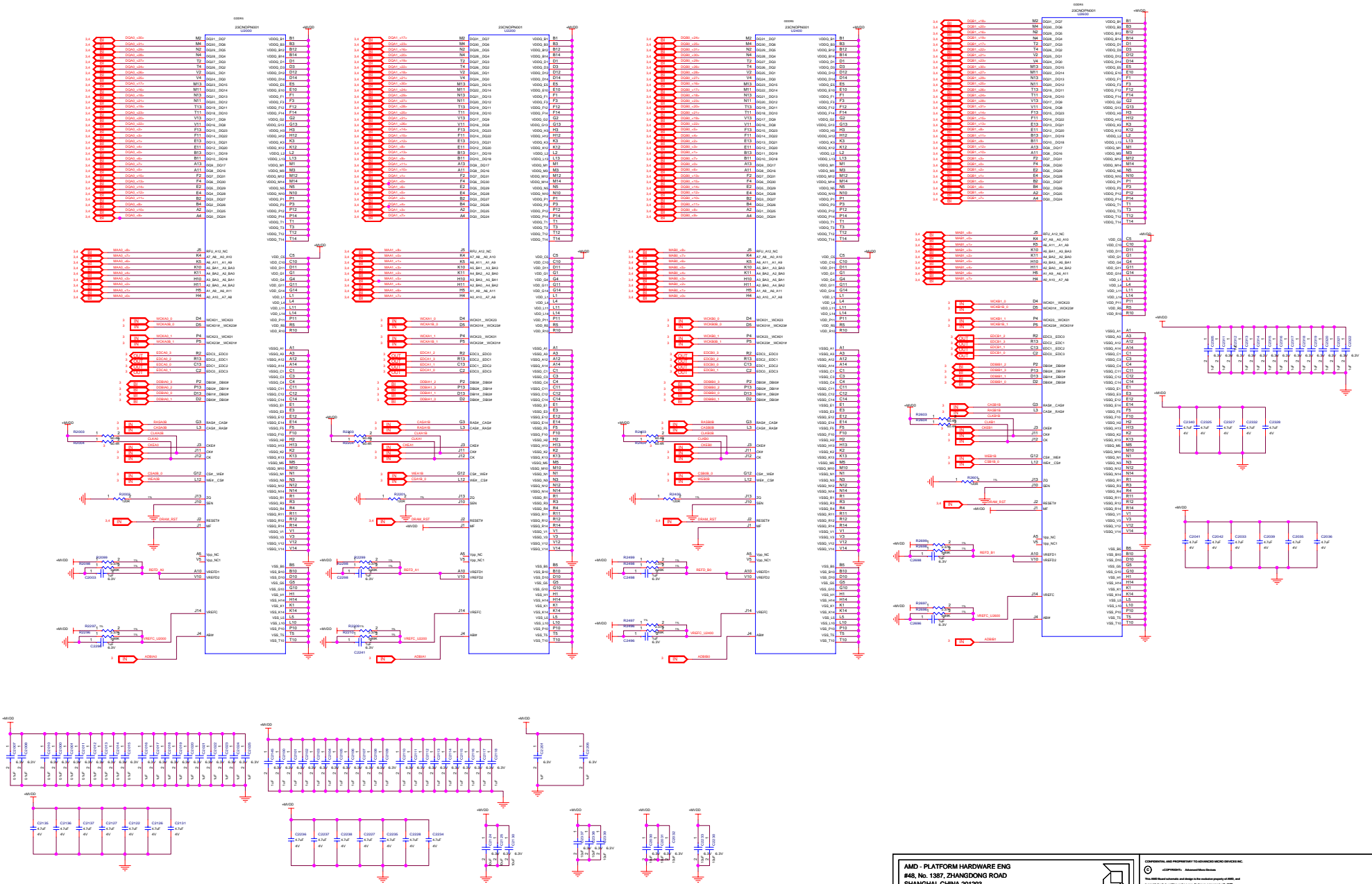
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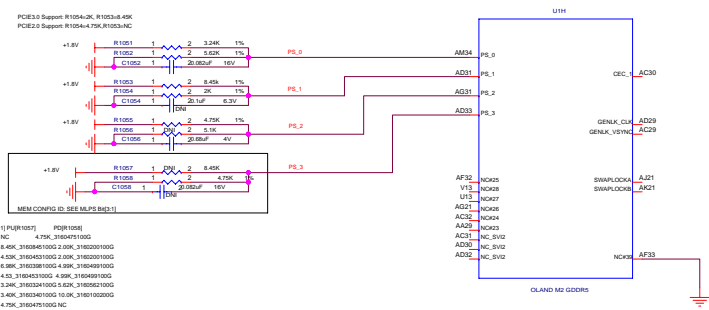
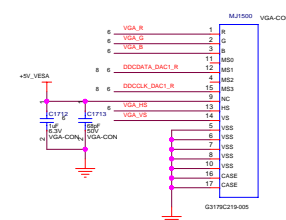
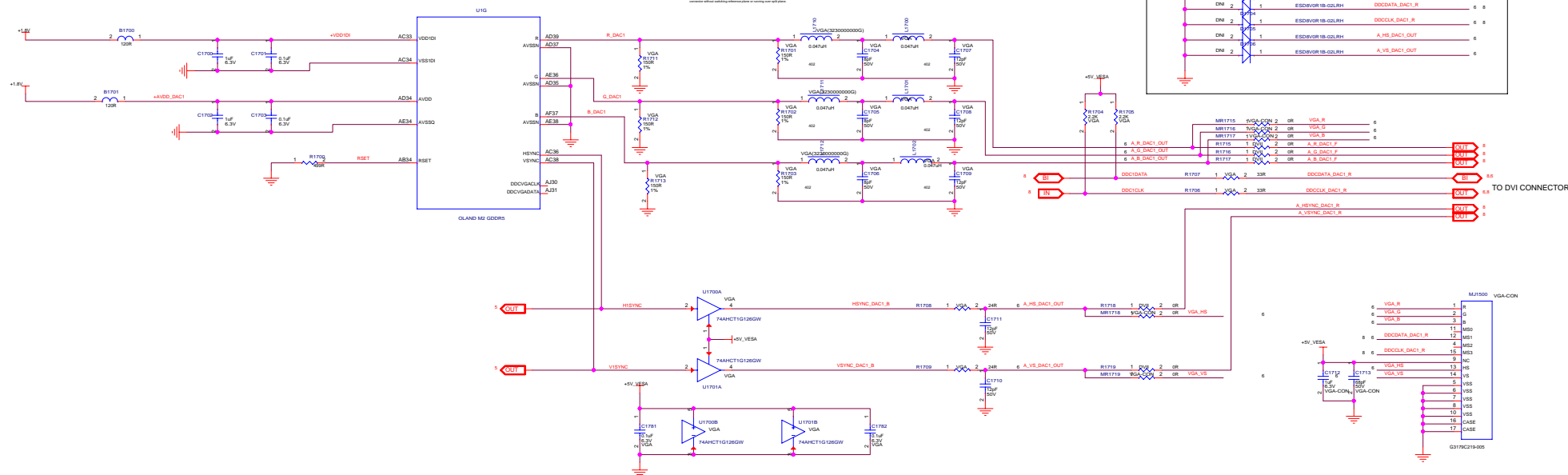
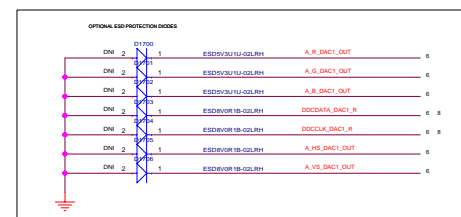


11

8	7	6	5	4	3	2	1
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AMD - PLATFORM HARDWARE ENG
#48, No. 1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203



SHEET: Oland DAC and MLPS

DATE: Tue Sep 22 06:32:58 2015

SHEET NUMBER: 6 OF 20

DOCUMENT NUMBER: 105-C869xx-0

NOTES:	NOTE
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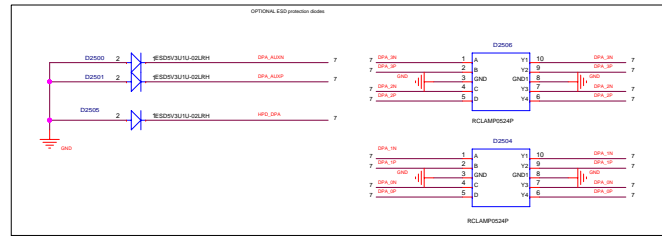
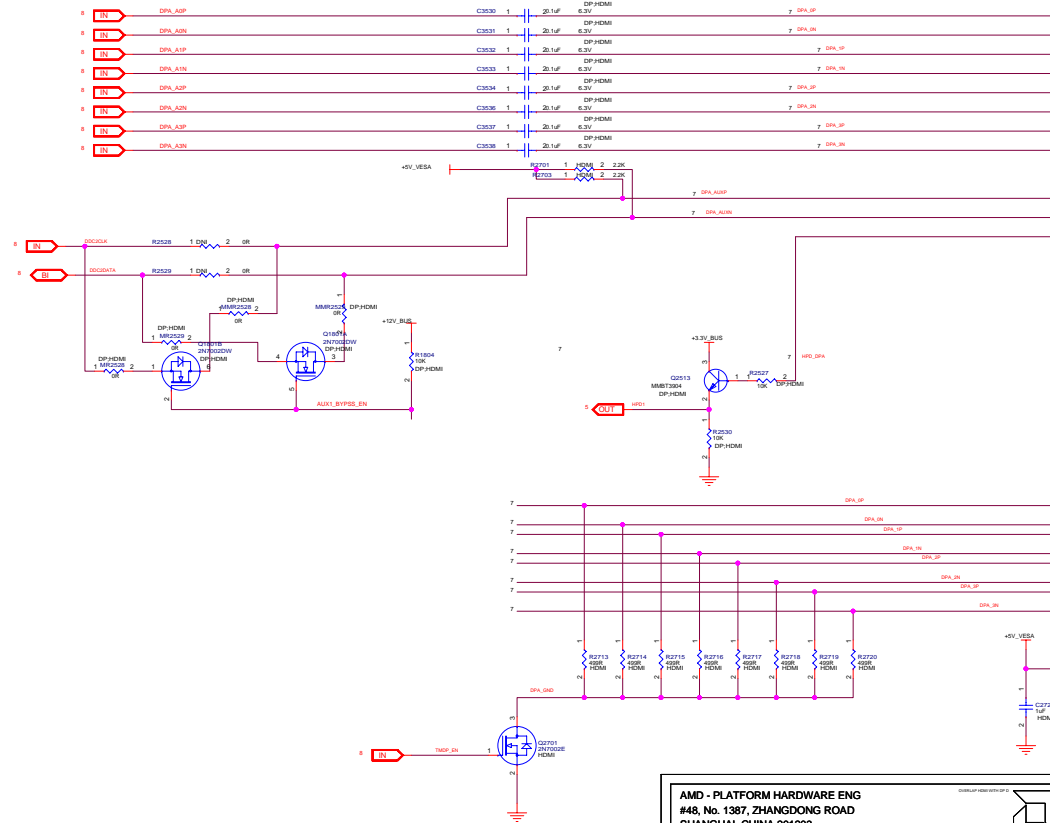
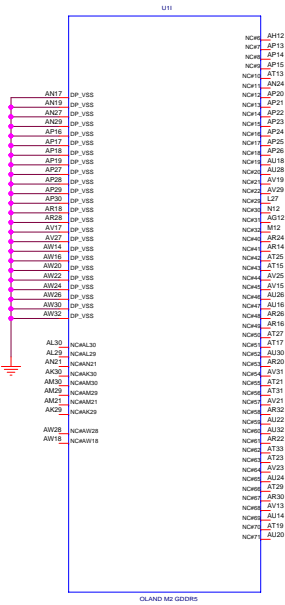
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TITLE:

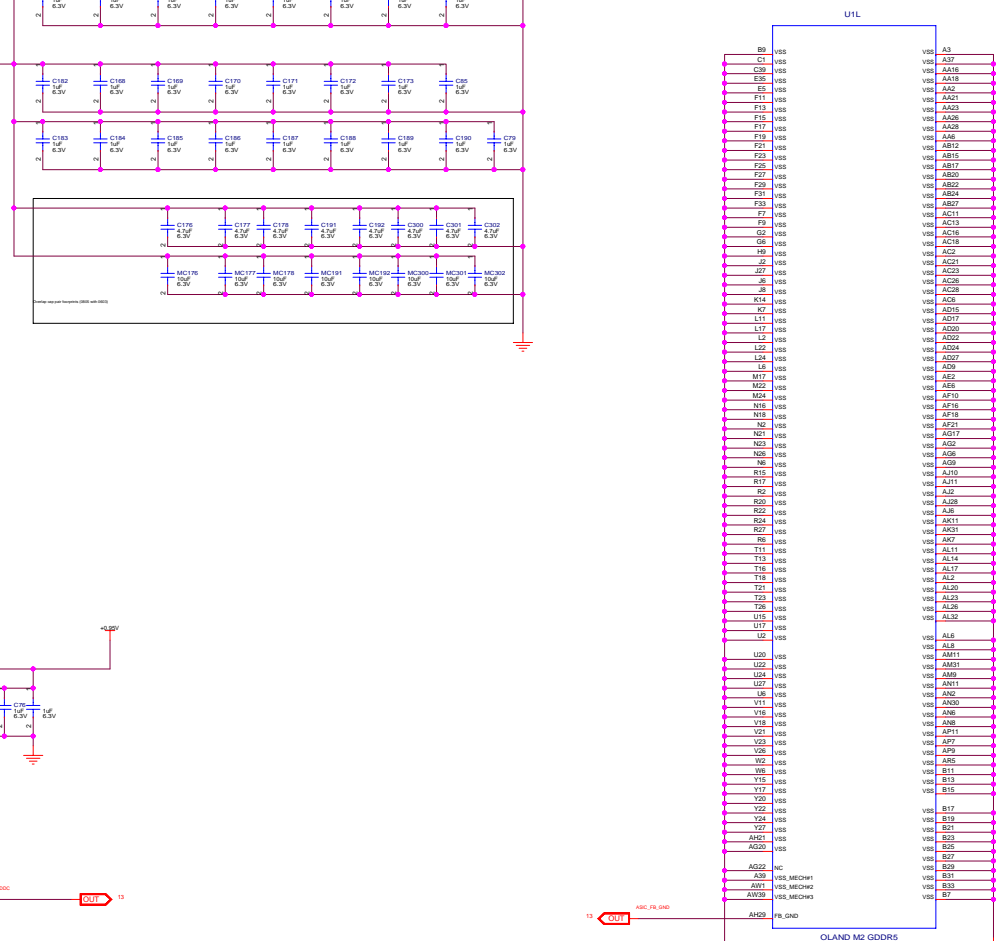
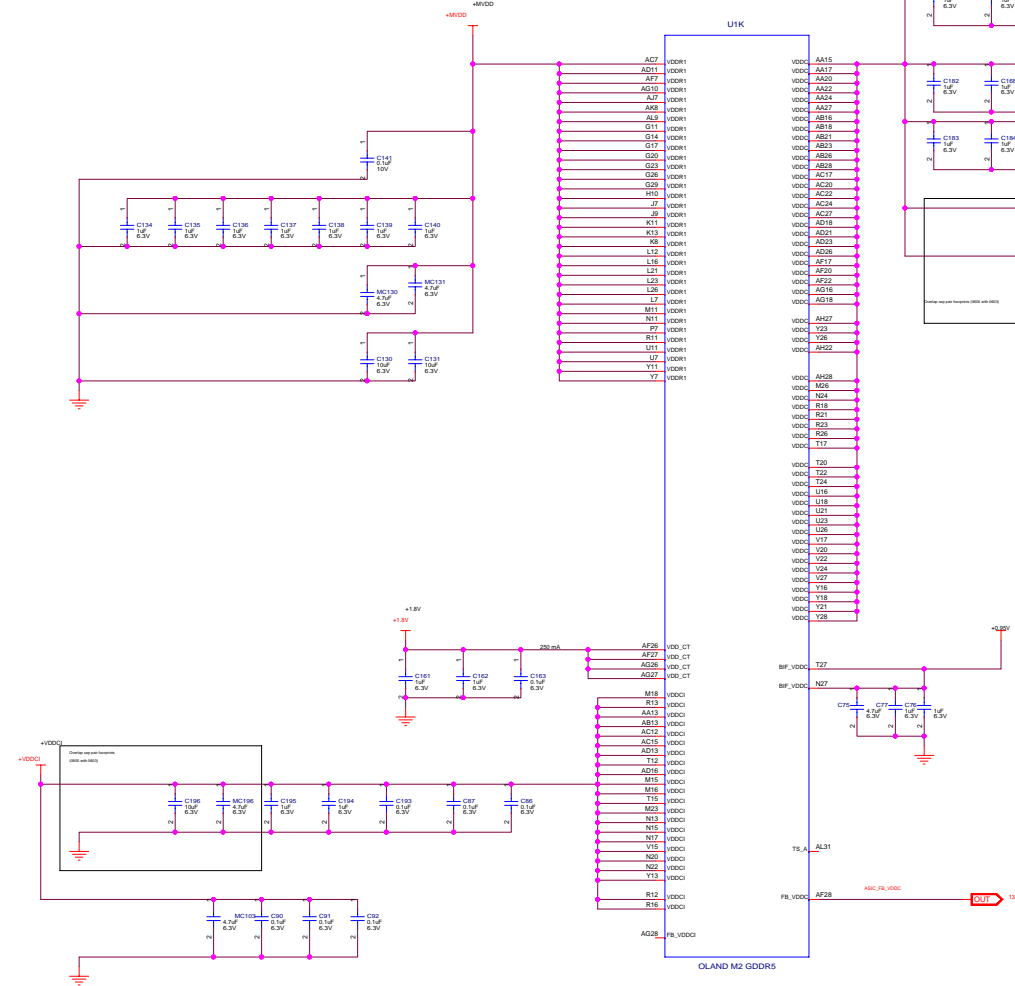
Oland G5 2GB VGA/sDVI-I+HDMI/DP



AMD - PLATFORM HARDWARE ENG #48, No. 1367, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: HDMI	
DATE: Tue Sep 22 06:32:59 2015	REV: 2.0
SHEET NUMBER: 7 OF 20	
DOCUMENT NUMBER: 105-CM6900-008	
NOTES: NOTE	

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TITLE: Oland G5 2GB VGA+DVI-I+HDMI/DP	

OLAND Power & GND



AMD - PLATFORM HARDWARE ENG
#48, No. 1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Oland Power&GND

DATE: Mon Sep 21 10:05:46 2015

SHEET NUMBER:

DOCUMENT NUMBER: 105-C869xx-008

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TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP

Linear Regulators

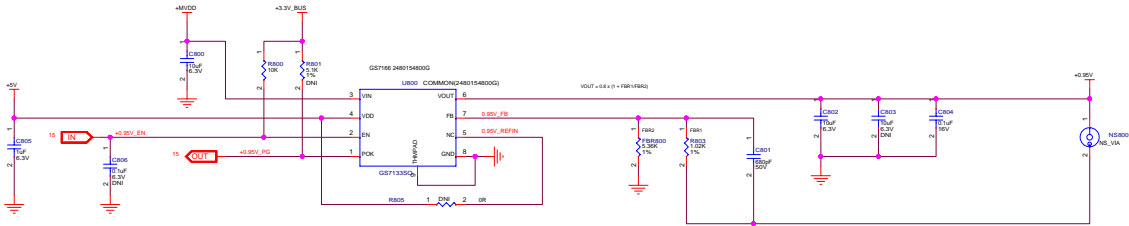
LDO #1:

$V_{in} = +1.5V \pm 2\%$

$V_{out} = +0.95V \pm 2\%$

$I_{out} = 1.44A (T_{BV}) RMS MAX$

PCB: 50 to 70mm sq. copper area for cooling



AMD - PLATFORM HARDWARE ENG
#48, No. 1367, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: 0.95V

DATE: Mon Sep 21 10:06:44 2015

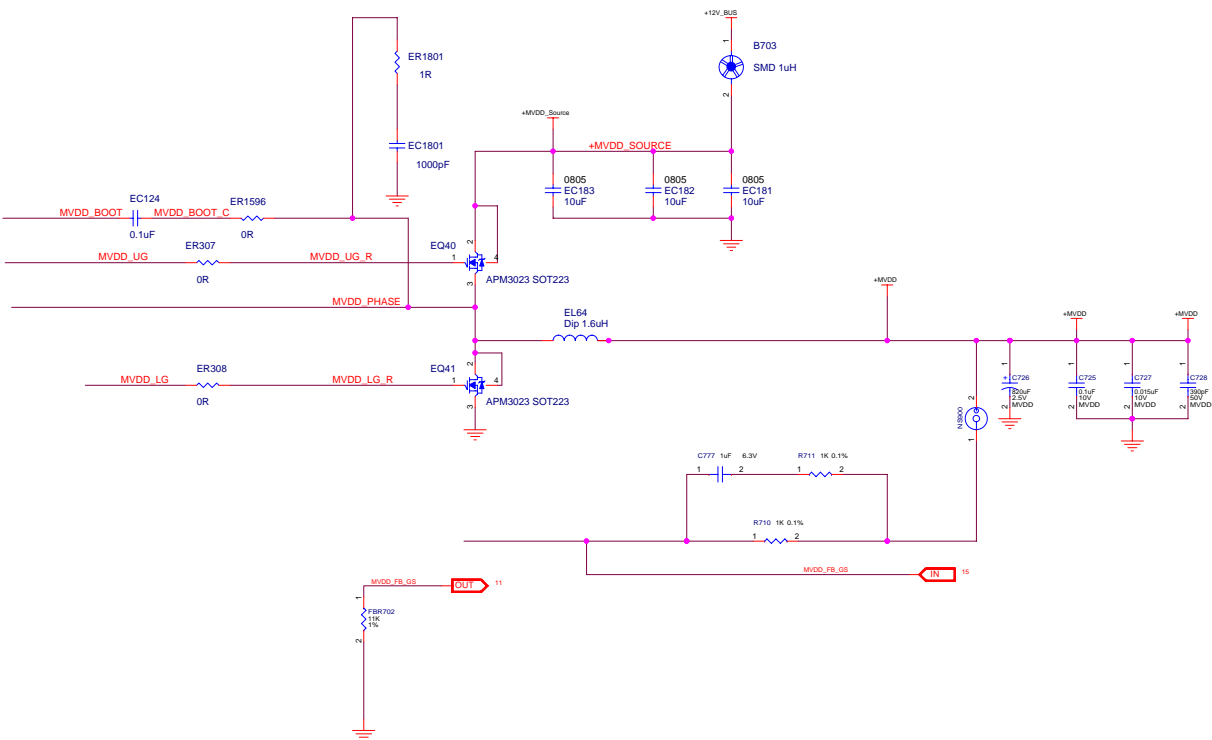
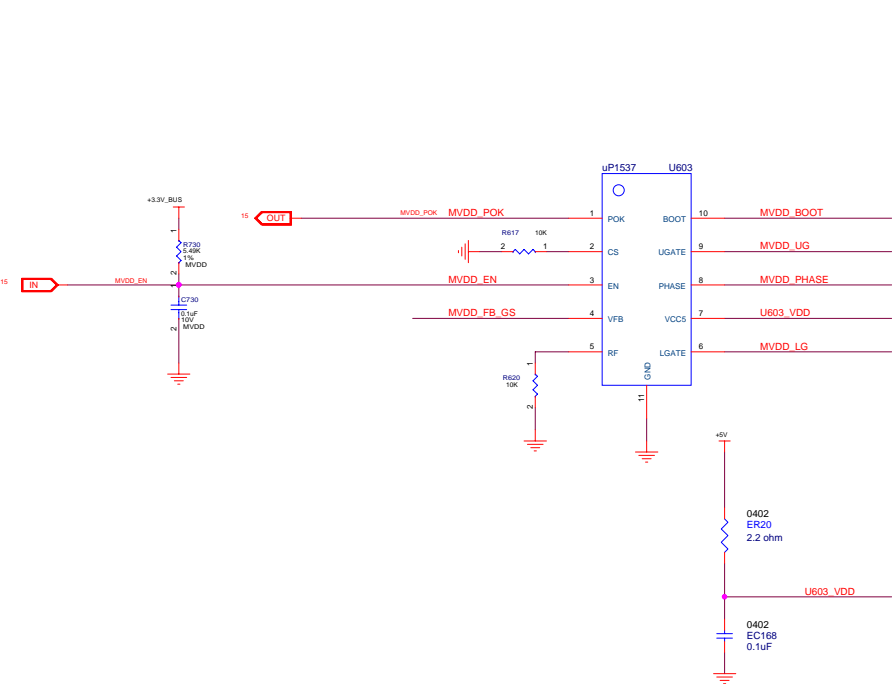
REV: 2.0

SHEET NUMBER: 10 OF 20

DOCUMENT NUMBER: 105-CM68xx-008

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TITLE: Oland G5 2GB VGA/sDV/H+HDMI/DP



AMD - PLATFORM HARDWARE ENG
#48, No. 1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203



SHEET: MVDD

DATE: Tue Sep 22 06:32:59 2015

REV: 2.0

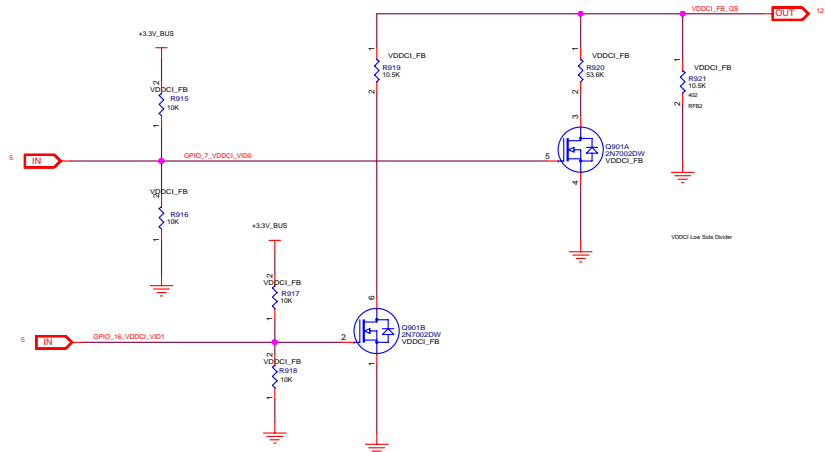
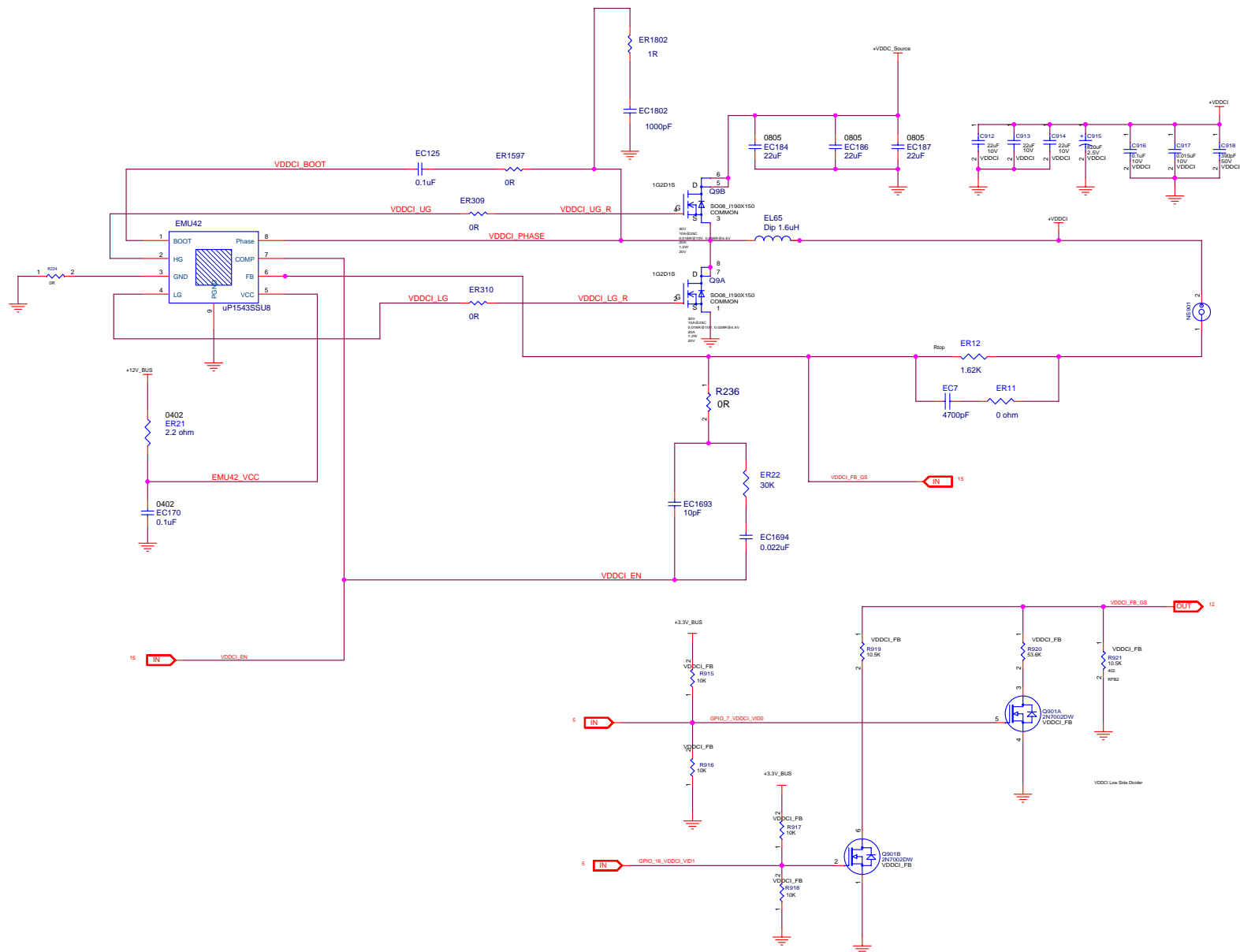
SHEET NUMBER: 11 OF 20

DOCUMENT NUMBER: 105-C860xx-008

NOTES: NOTE

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TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP



AMD - PLATFORM HARDWARE ENG
#48, No. 1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203



SHEET: VDDCI

DATE: Tue Sep 22 06:32:59 2015

REV: 2.0

SHEET NUMBER: 12 OF 20

DOCUMENT NUMBER: 105-C869xx-00B

NOTES: NOTE

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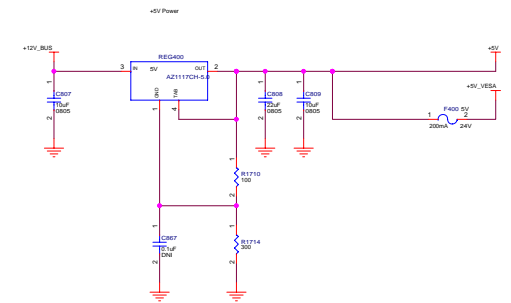
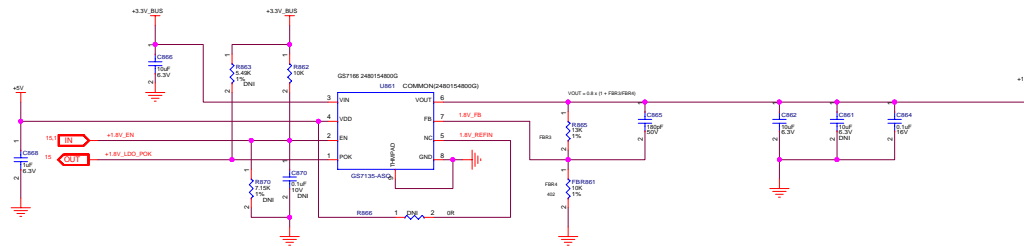
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TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP

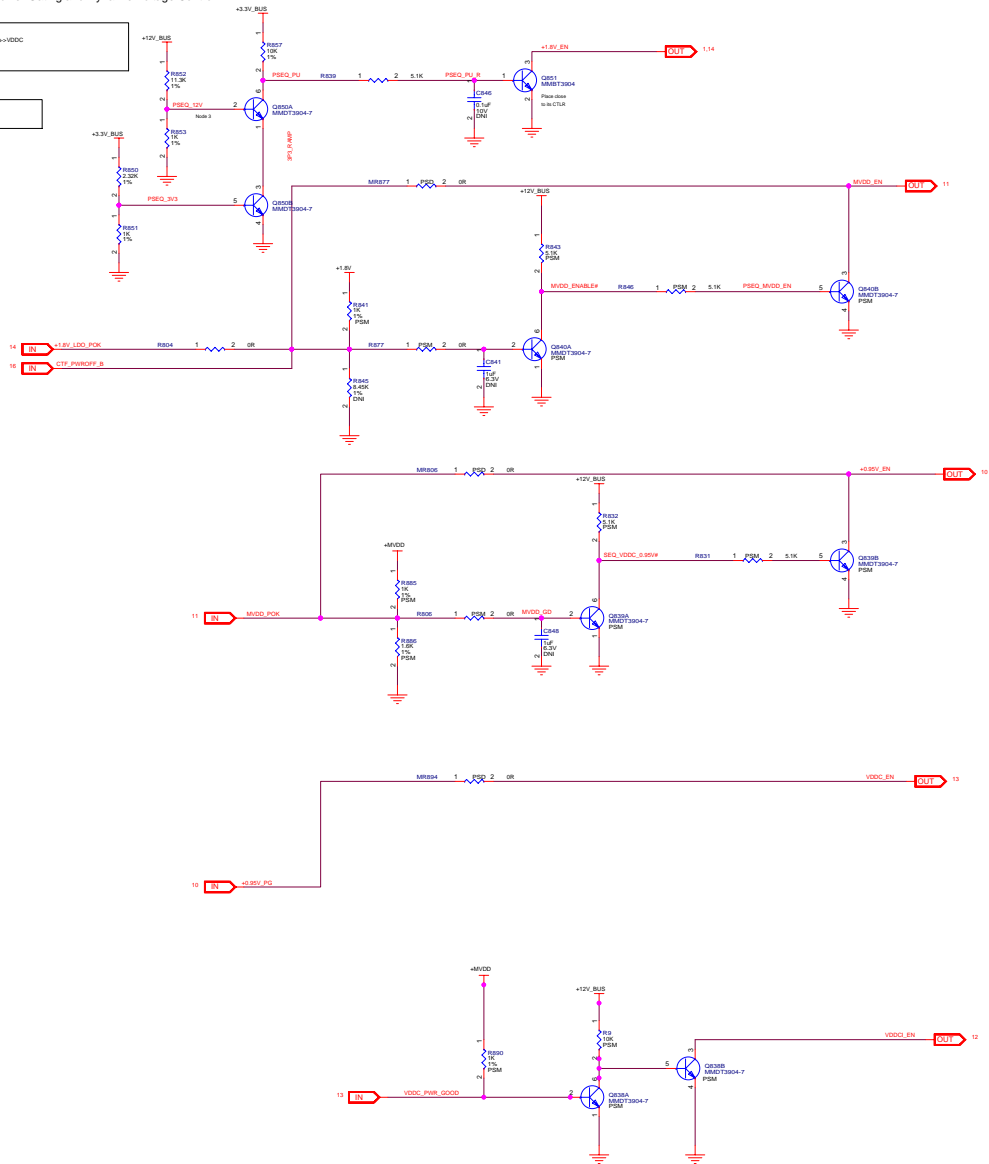
Linear Regulators

LDO #2:	$V_{in} = 3.00V \text{ to } 3.60V \text{ (3.3V } \pm 5\%)$	$V_{out} = +1.8V \text{ } \pm 2\%$	Iout = 1.6A (TBR) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling			

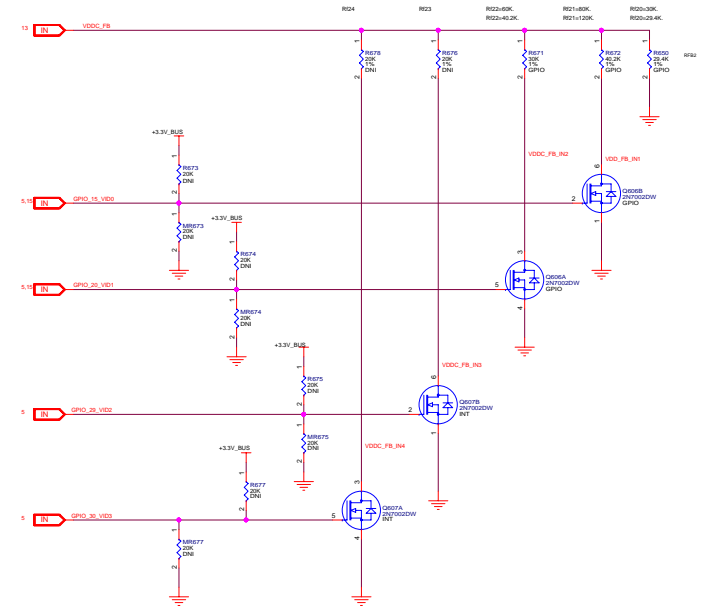



<p>AMD - PLATFORM HARDWARE ENG #48, No. 1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203</p>		<p>CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.</p> <p>COPYRIGHT © Advanced Micro Devices, Inc.</p> <p>This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.</p>
<p>SHEET: VDDCI</p>	<p>REV: 2.0</p>	
<p>DATE: Tue Sep 22 06:32:59 2015</p>	<p>SHEET NUMBER: 14 OF 20</p>	
<p>DOCUMENT NUMBER: 105-C8869-us-008</p>	<p>TITLE:</p> <p style="text-align: center; font-weight: bold;">Oland G5 2GB VGA/sdVI-I+HDMI/DP</p>	
<p>NOTES: NOTE</p>		

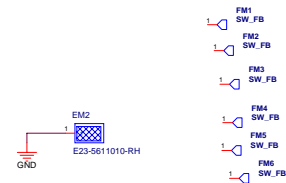
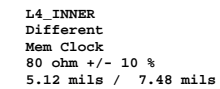
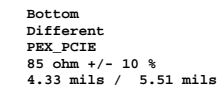
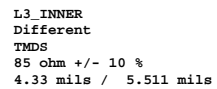
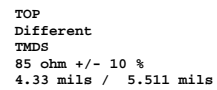
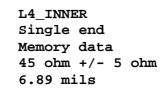
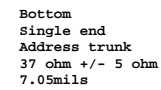
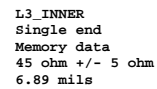
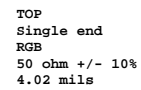
Don't support BACO Support CTF(internal)

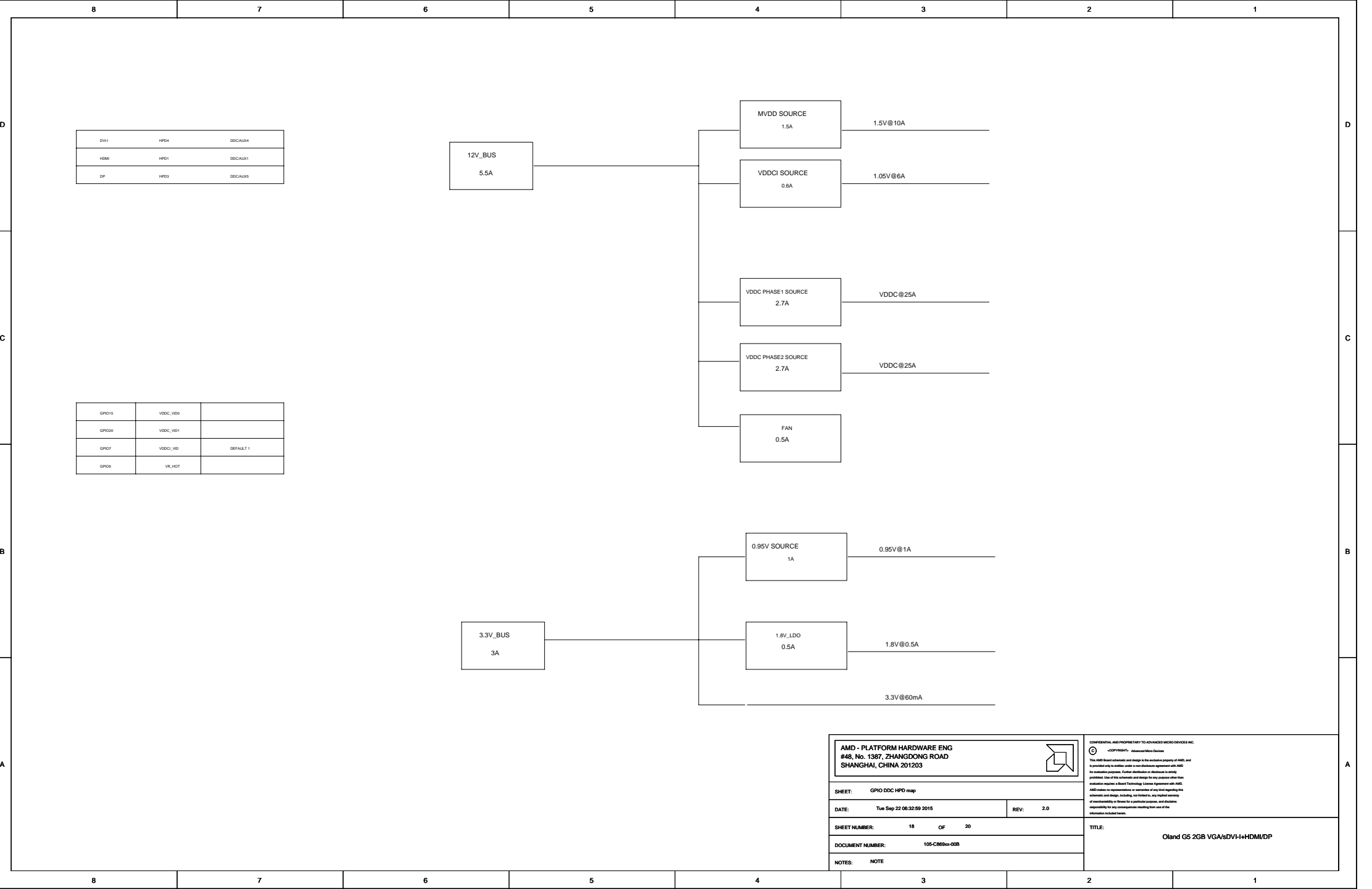


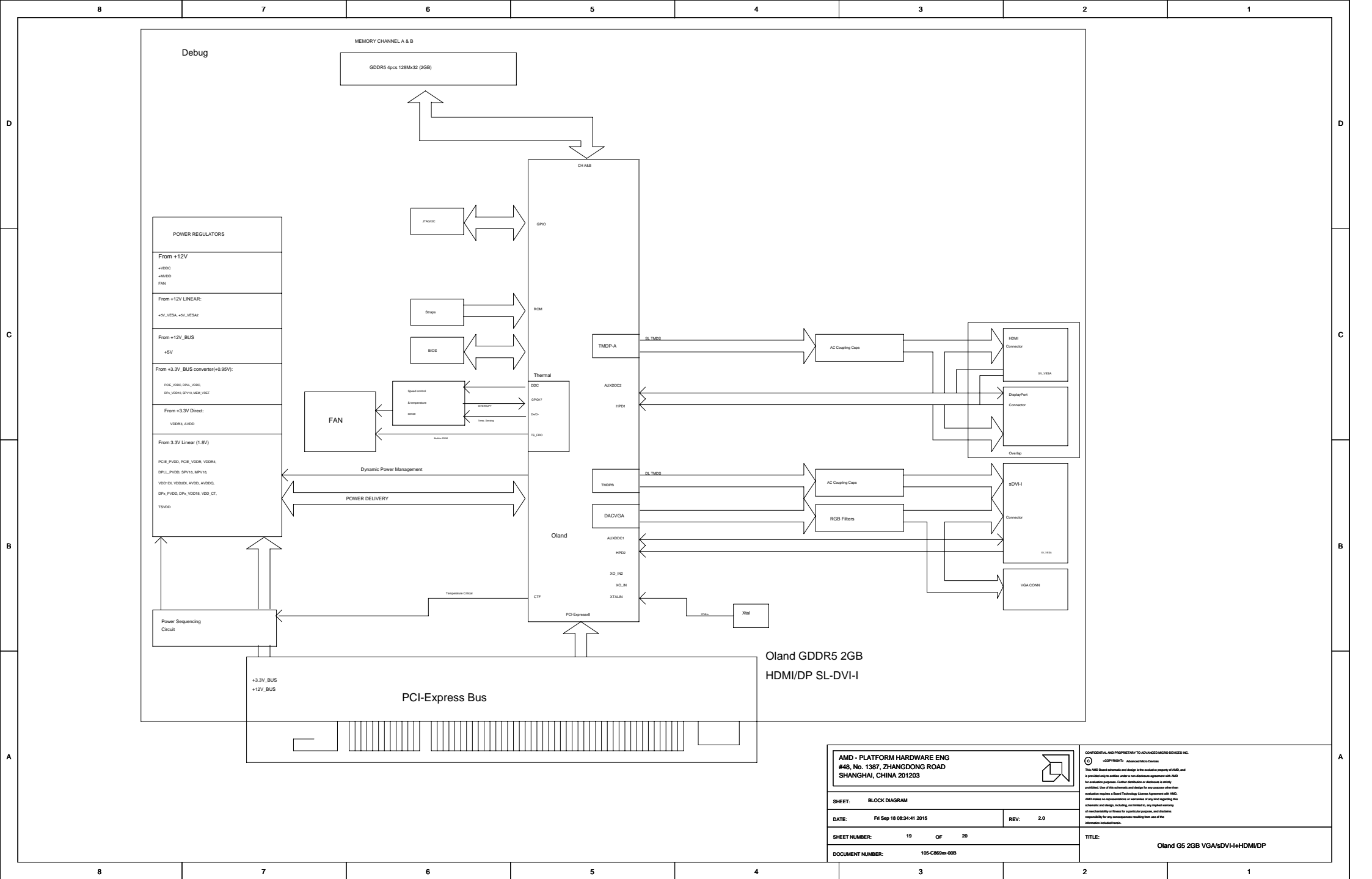
Symbol should use uP180116 is bigger one)
 For Baudrate: 240Kbit/115000: 058801
 2nd Source: 24801051000: uP1801



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SHEET: VDDC		REV: 2.0			
DATE: Tue Sep 22 06:32:59 2015					
SHEET NUMBER: 15 OF 20				TITLE: Oland G5 2GB VGA+sDVI+HDMI/DP	
DOCUMENT NUMBER: 105-C869xx-00B					
NOTES: NOTE					







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AMD



TITLE:

Oland G5 2GB VGA/sDVI-++HDMI/DP

DOCUMENT NUMBER:

105-C869xx-008

DATE:

Tue Sep 22 02:20:17 2015

SHEET NUMBER:

20 OF 20

REV:

2.0

REVISION HISTORY

ENGINEER:

Tony Yang

NOTES:

NOTE

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SCH Rev	PCB Rev	Date	REVISION DESCRIPTION
1.00	000	04/19/14	1 Initial release
2.00	000	09/22/15	2. AMD VGA, etc

8

7

6

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B

A