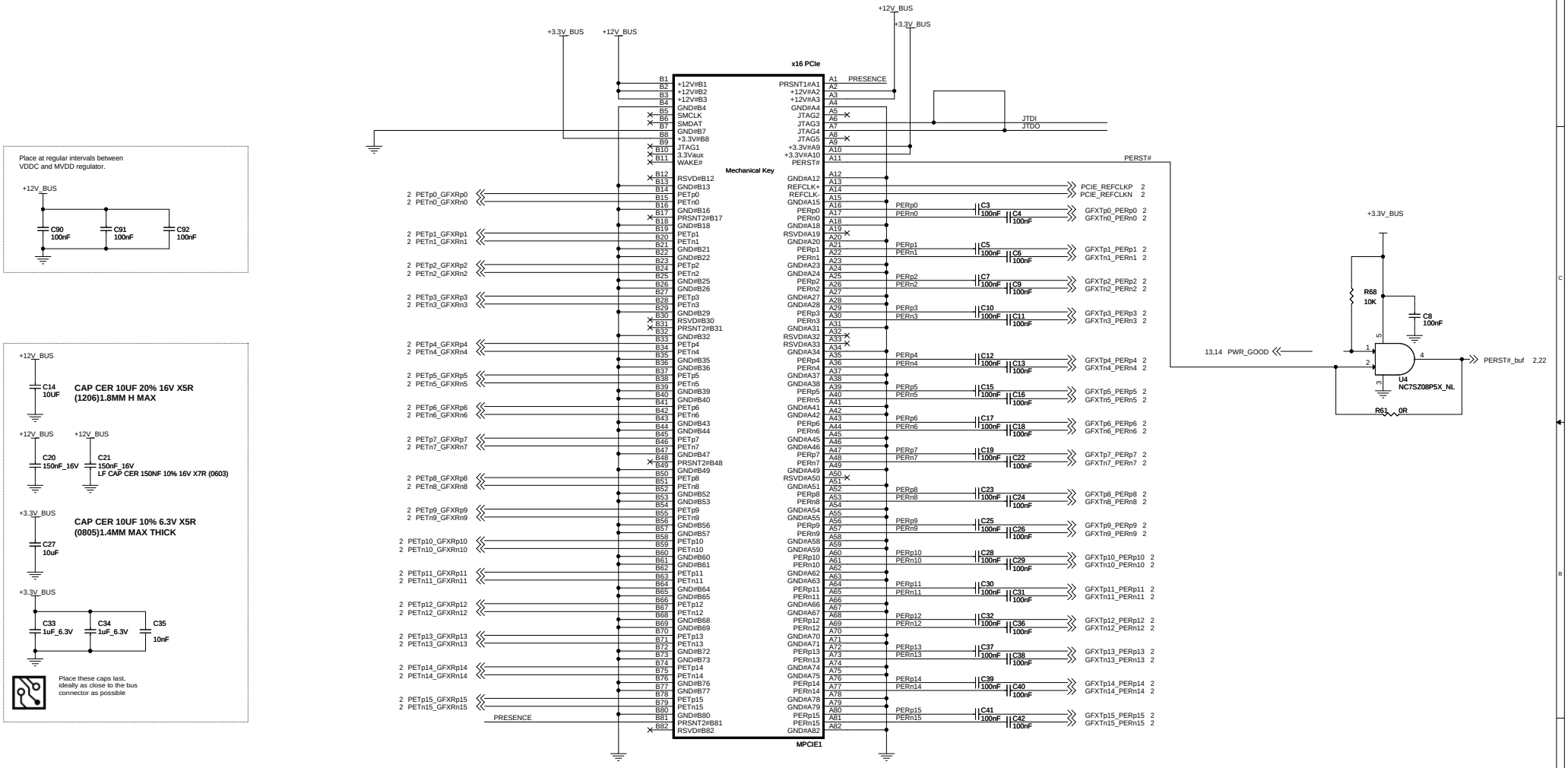
Cedar

VGA(header) +HDMI + DVI

PCI-EXPRESS EDGE CONNECTOR



Place at regular intervals between VDDC and MVDD regulator.

Place these caps last, ideally as close to the bus connector as possible

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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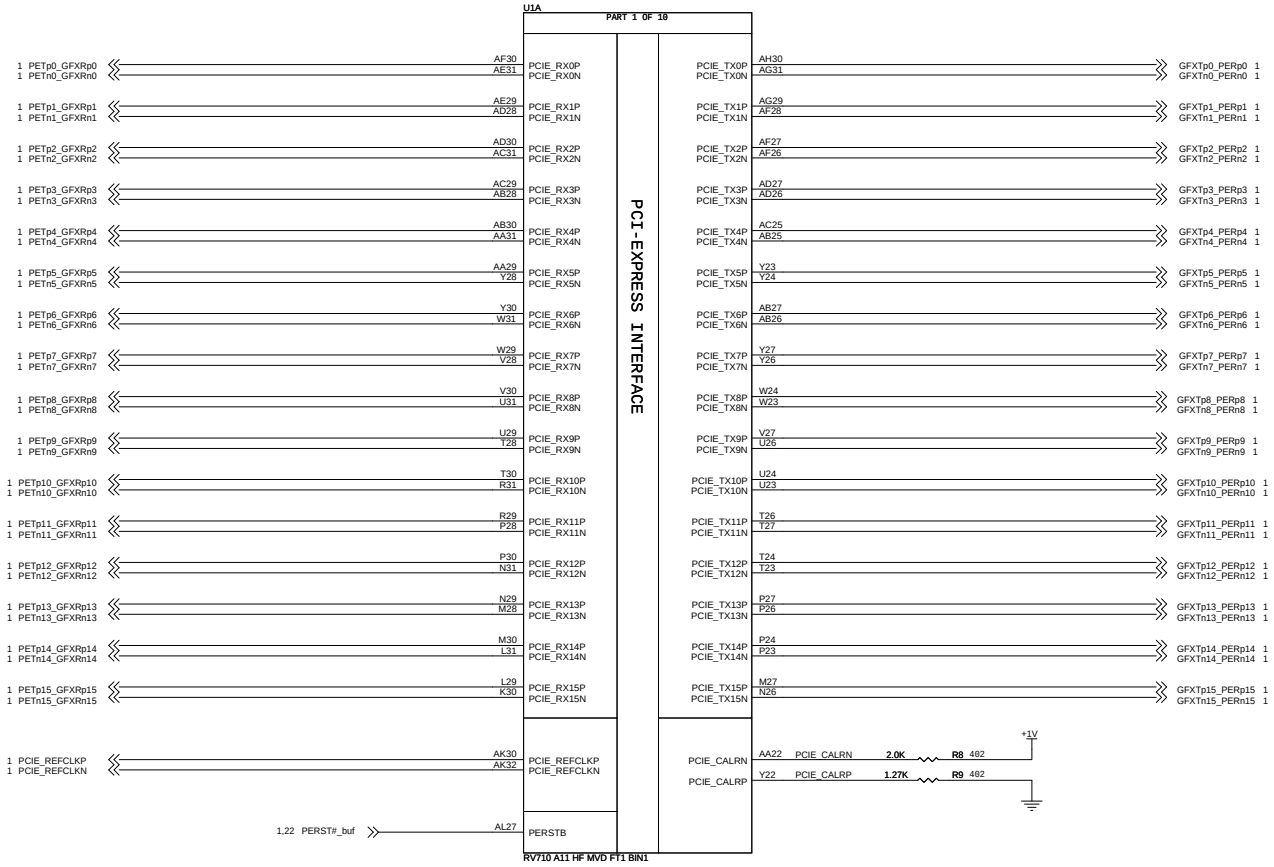
(2) Cedar PCIE Interface

NOTE: some of the PCIE testpoints will
be available through via on traces.



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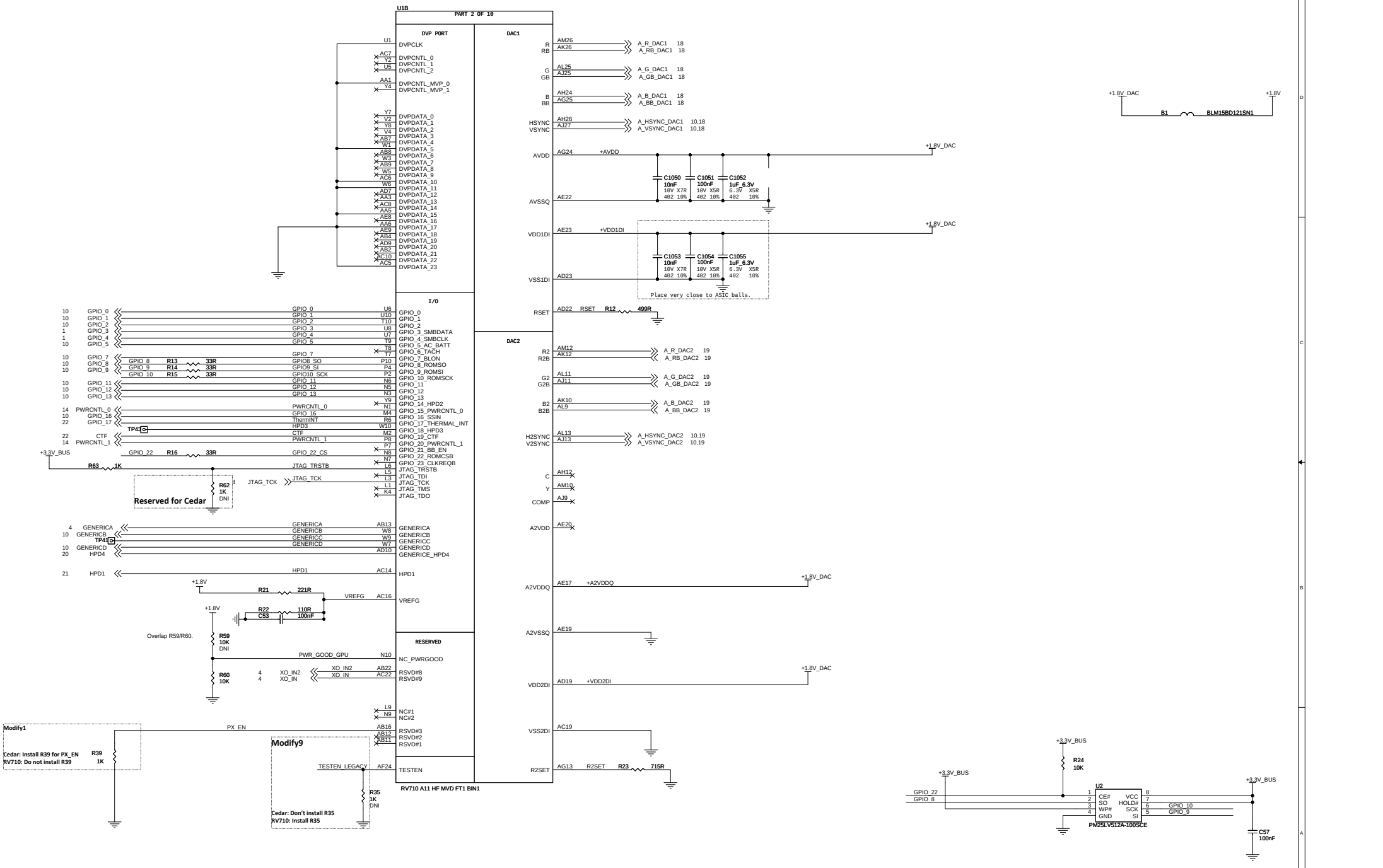
(3) Cedar Main



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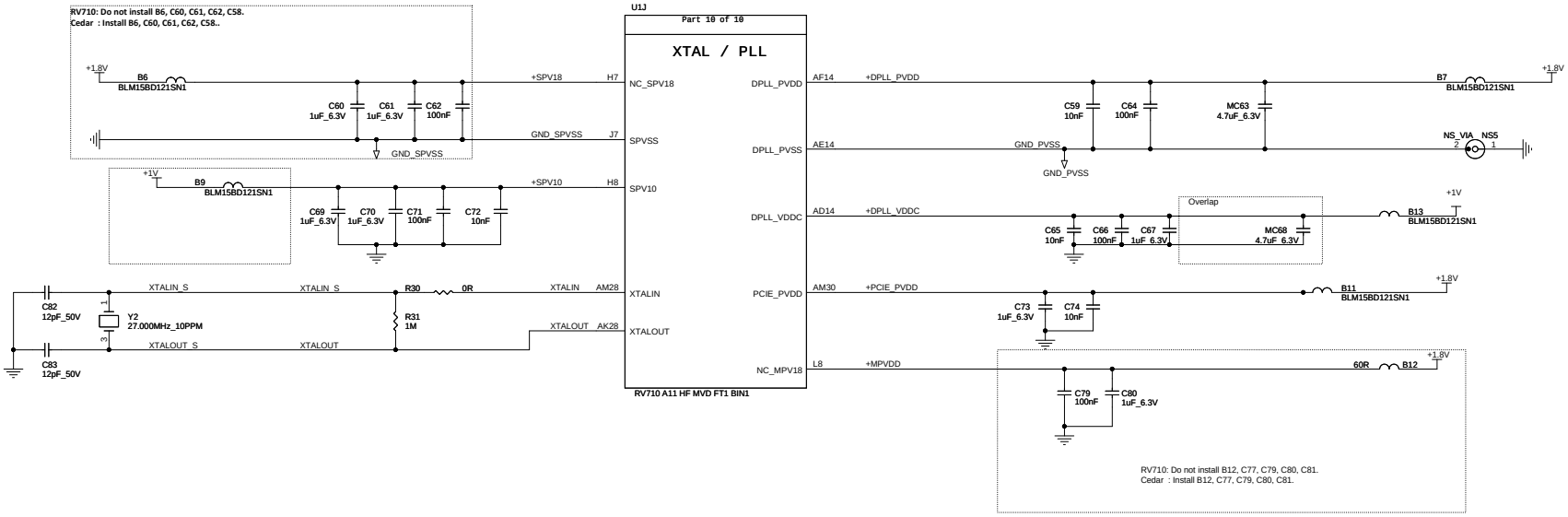
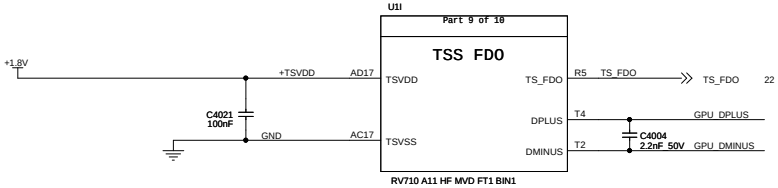
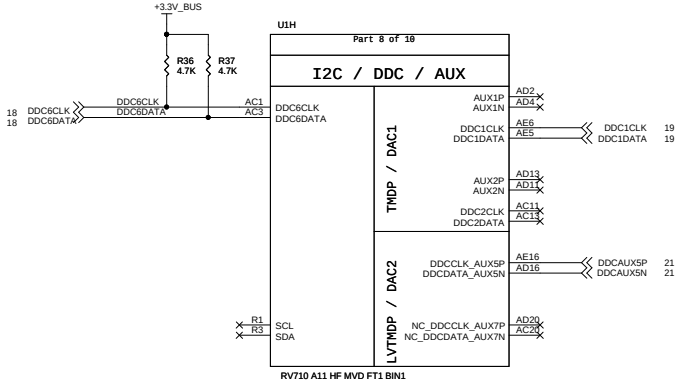
(04) Cedar GPIOs CF XTAL





DDC1	Top VGA
AUX1	NC
DDC2	NC
AUX2	NC
DDC/AUX3	Middle HDMI/DP
DDC/AUX5	Bottom DVI/VGA
DDC6	NA
I2C	Debug Access Port



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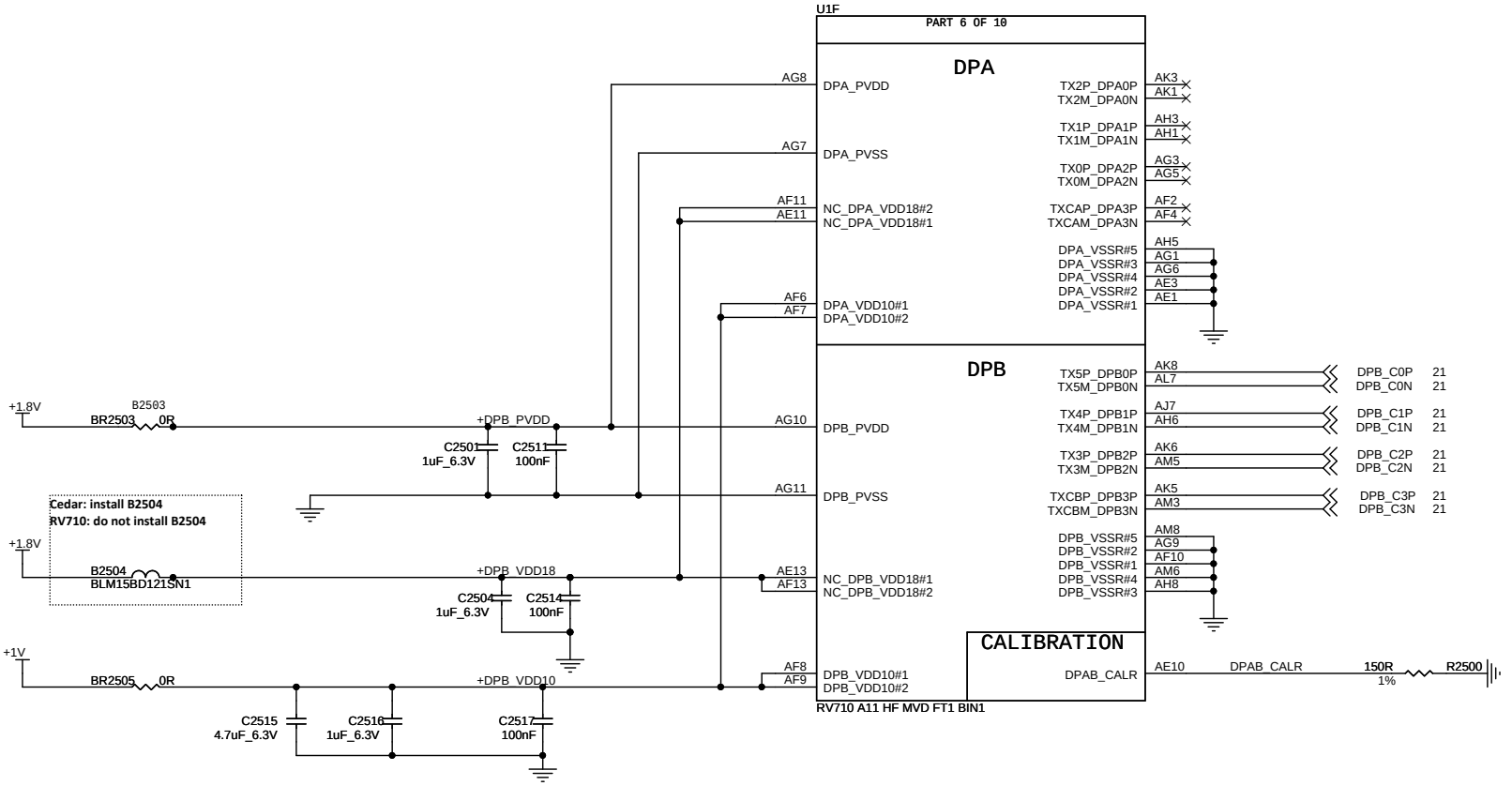
(05) Cedar TMDP A&B

TMDP INTERFACE



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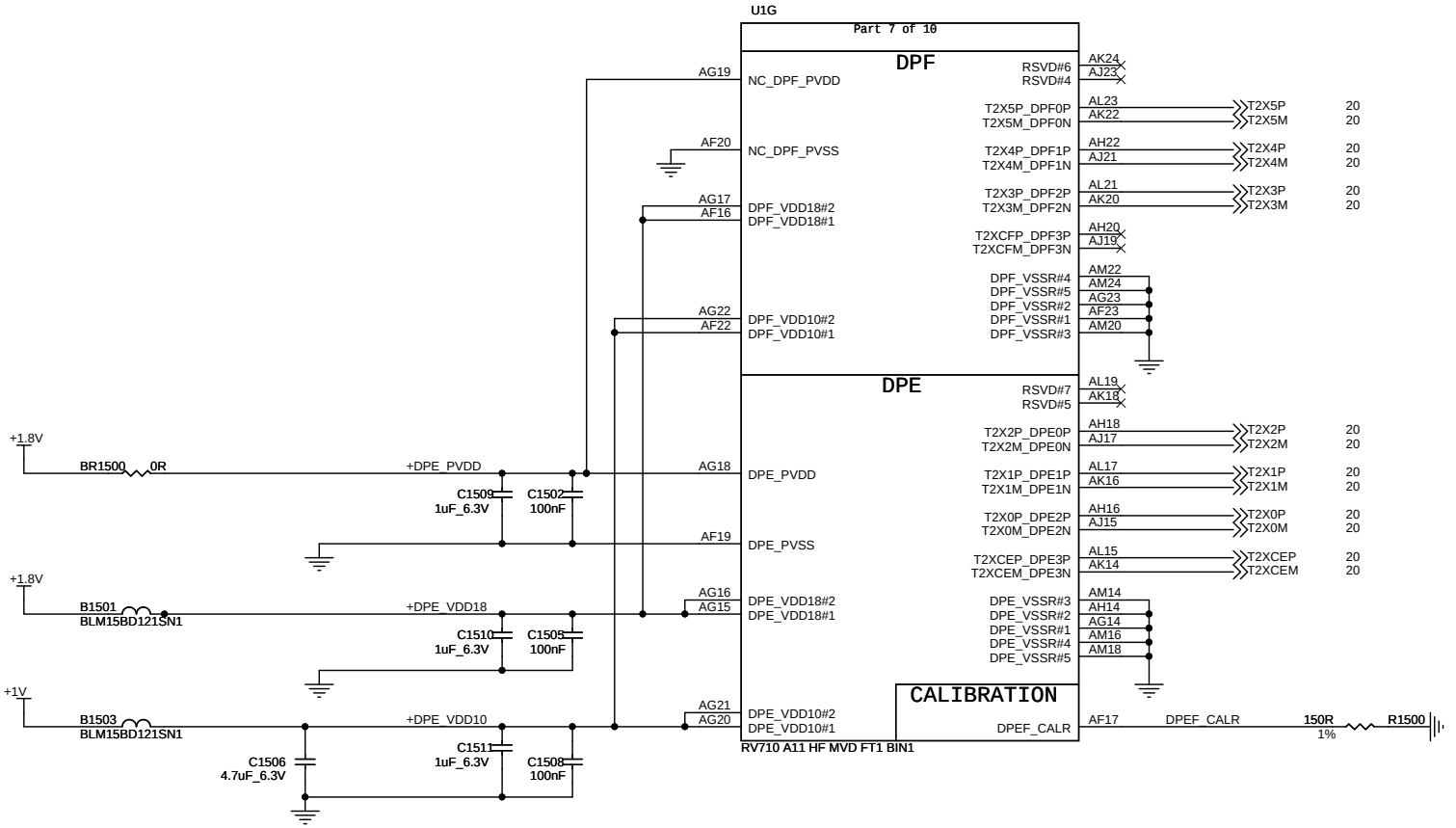
(06) Cedar TMDP E&F

LVTMDP INTERFACE



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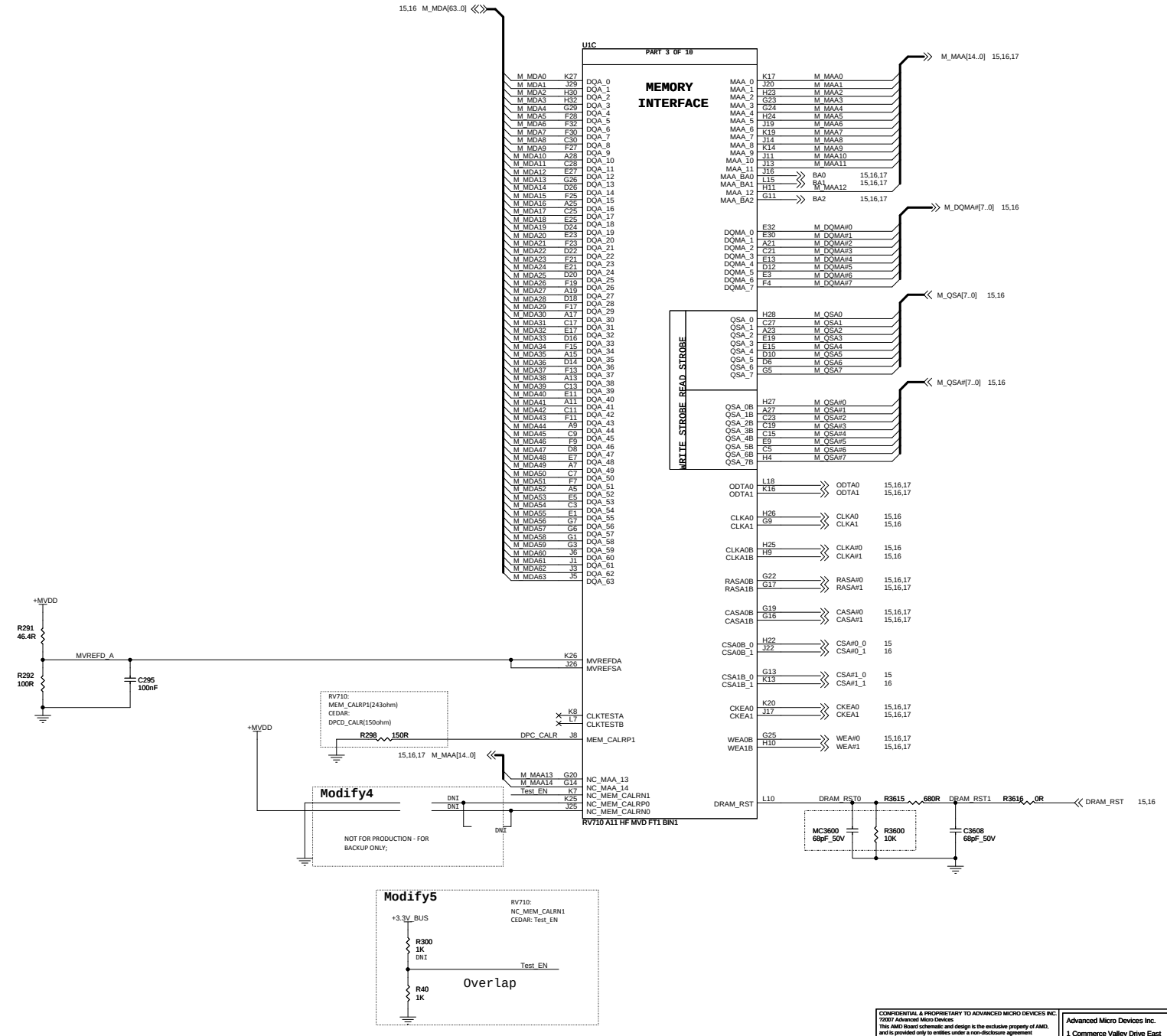
(07) Cedar MEM Interface Ch A

MEMORY INTERFACE



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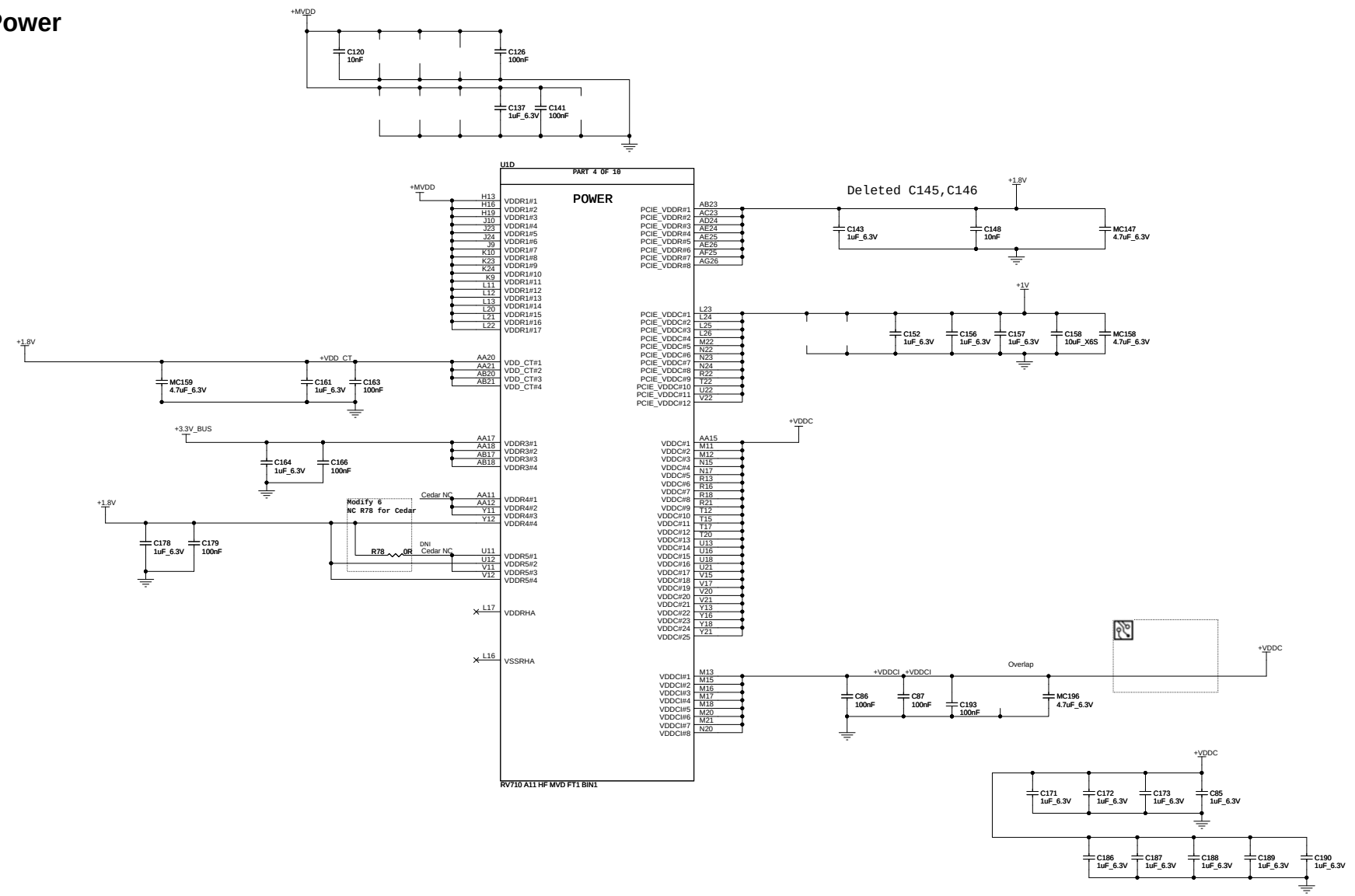
(08) Cedar Power



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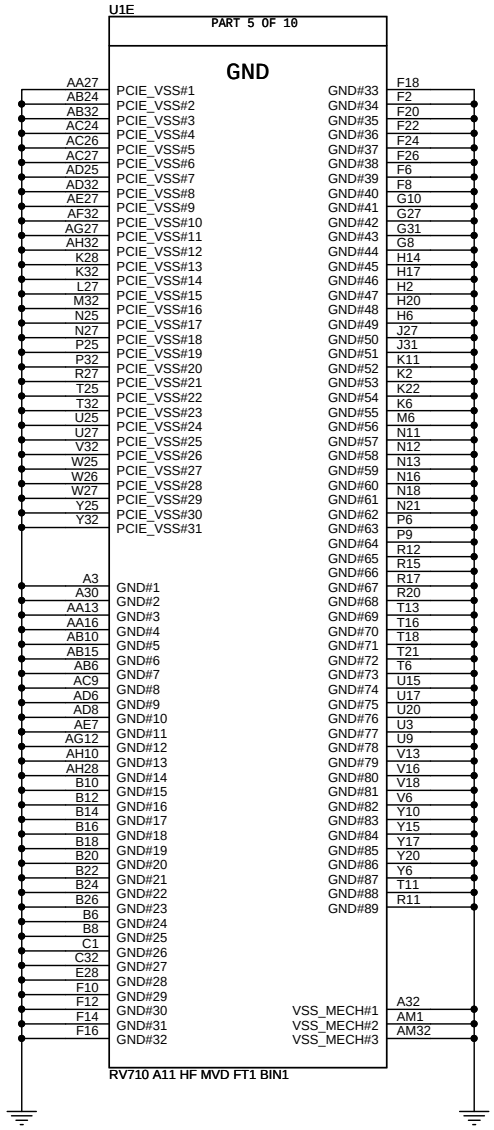
(09) Cedar GND



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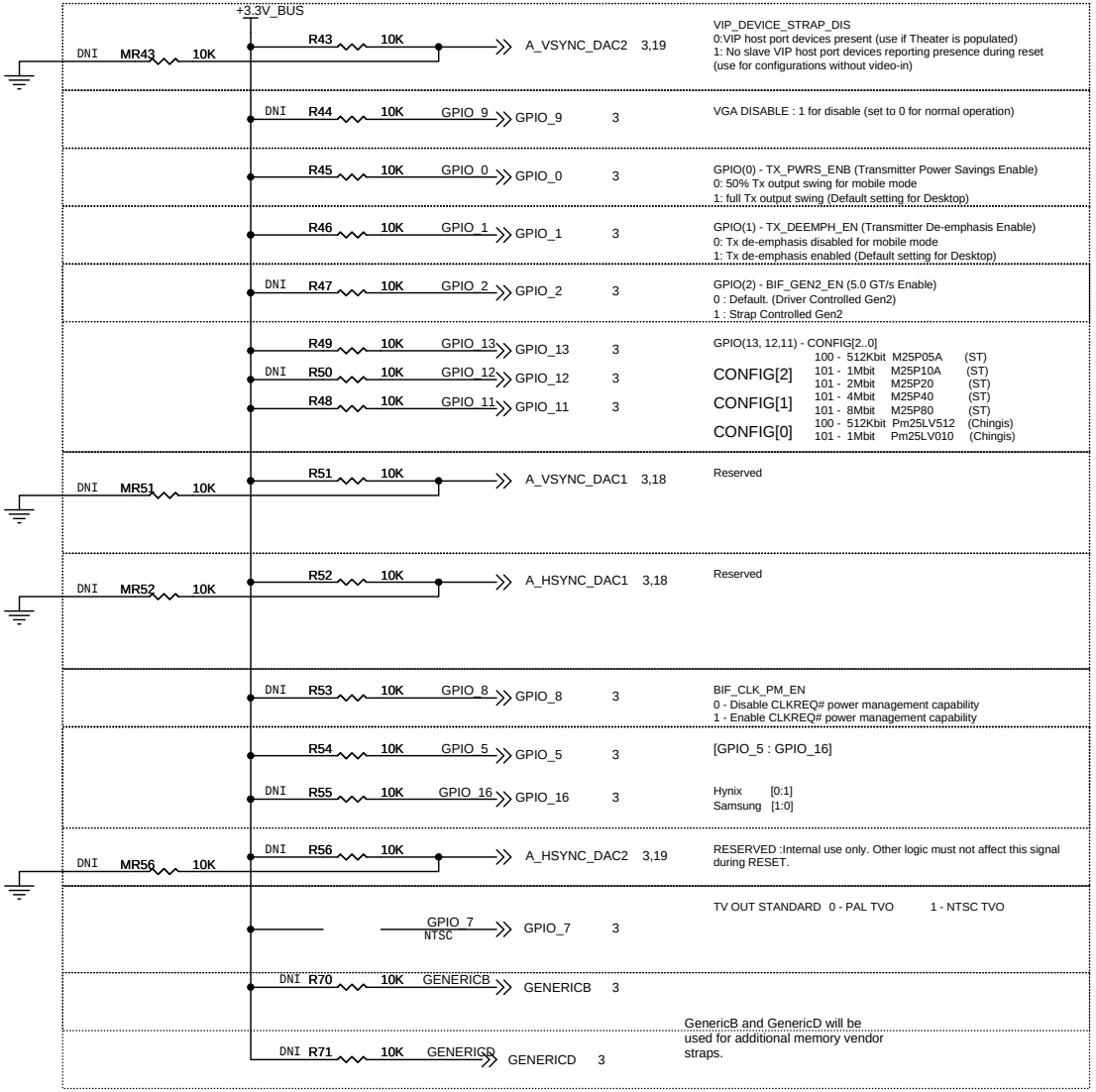
(10) Cedar STRAPS

PIN BASED STRAPS



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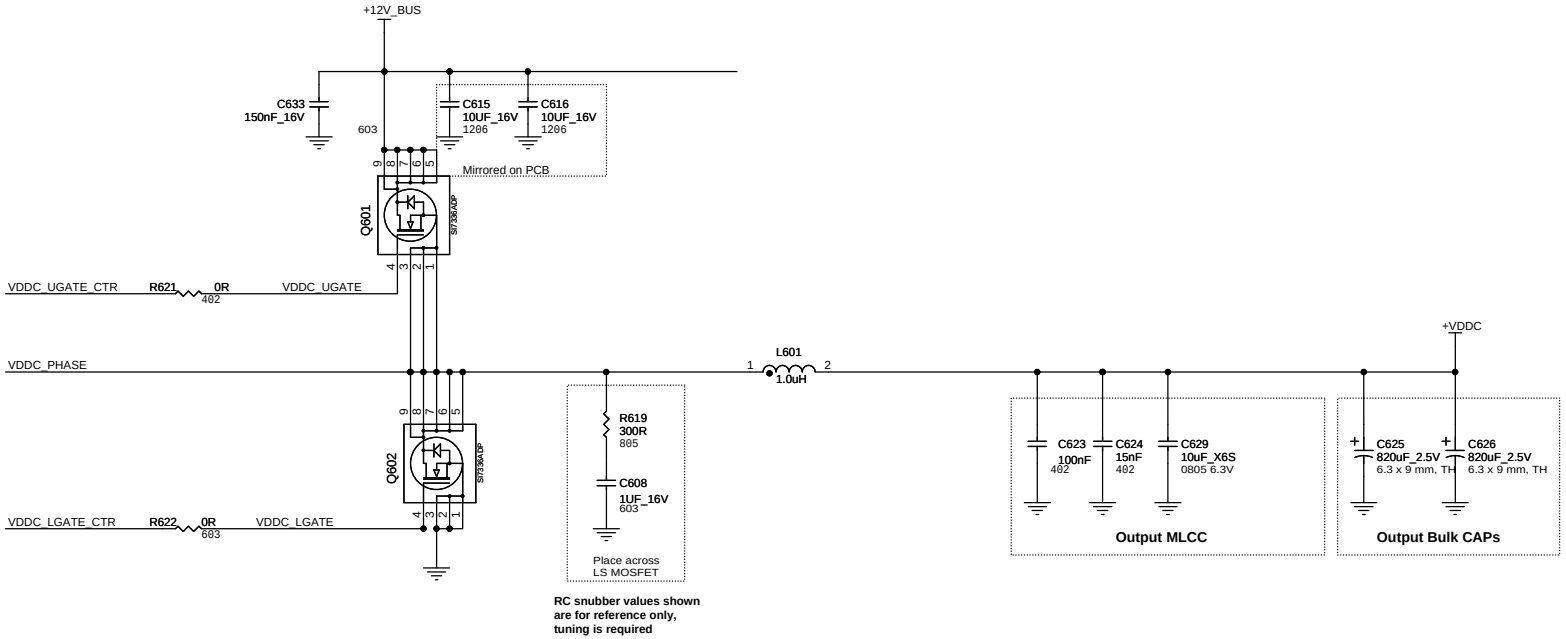
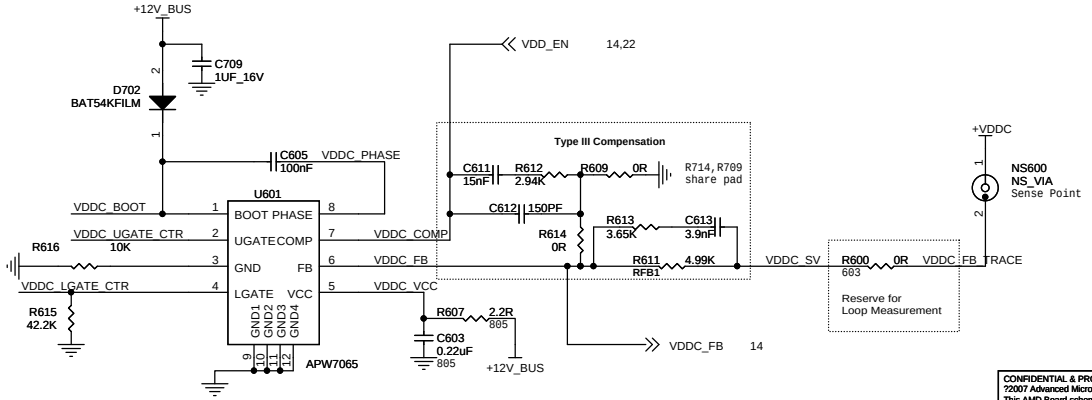


RC snubber values shown are for reference only, tuning is required



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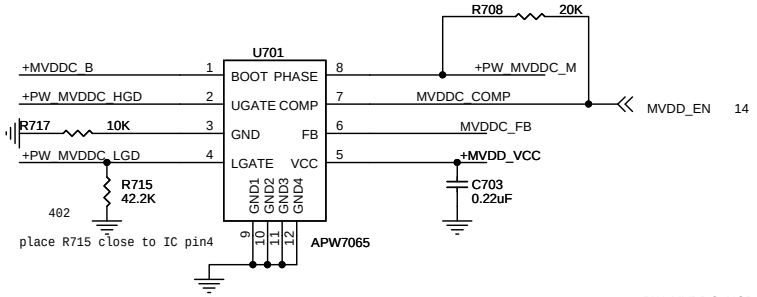
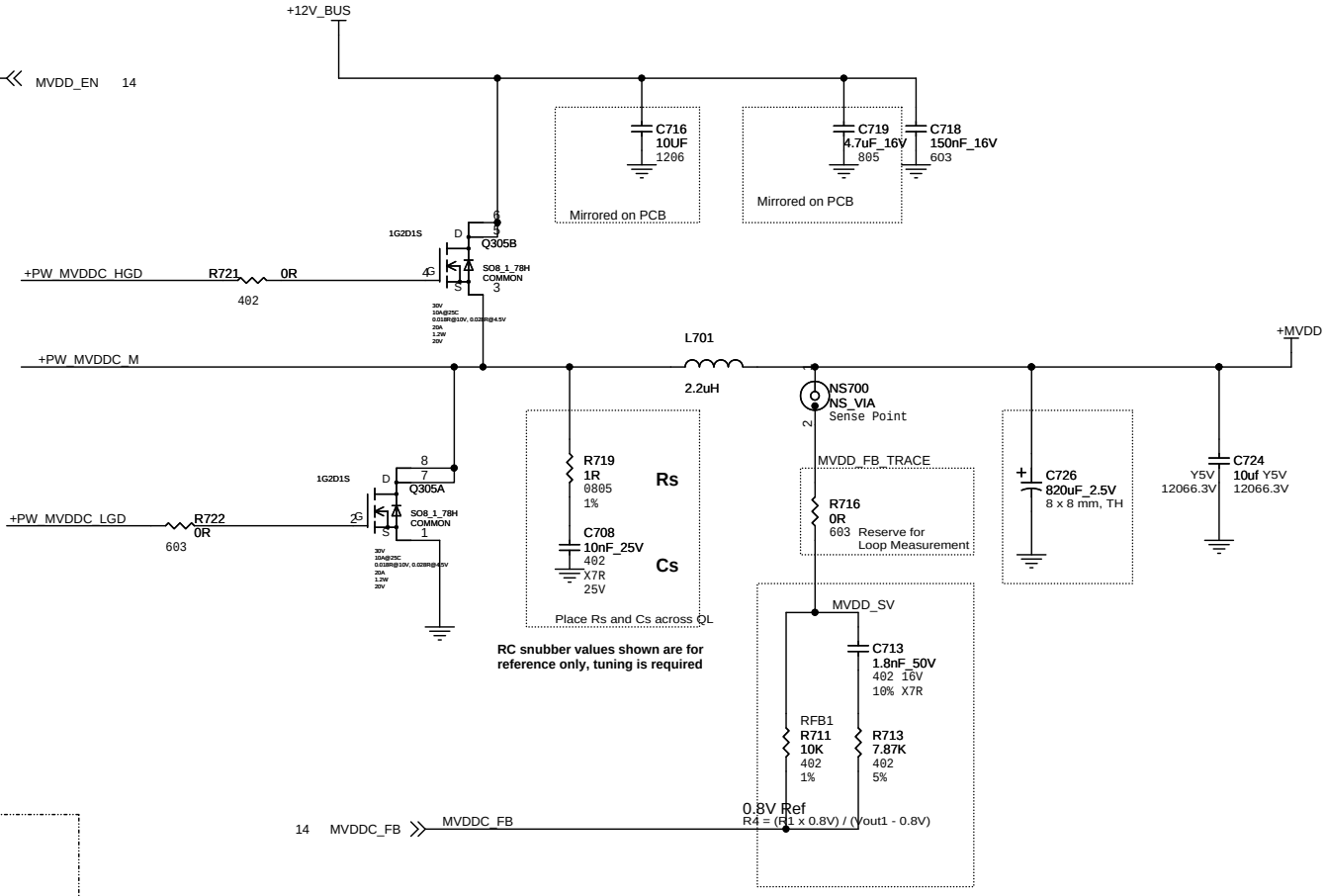
(12) MVDD

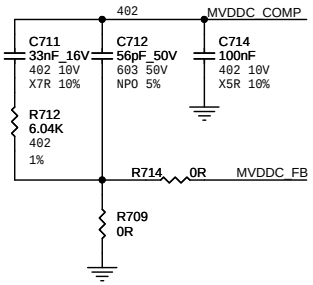


Layout guideline

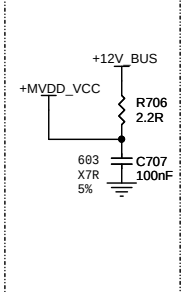
1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



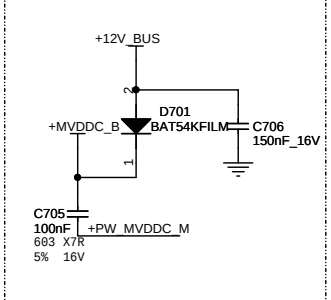
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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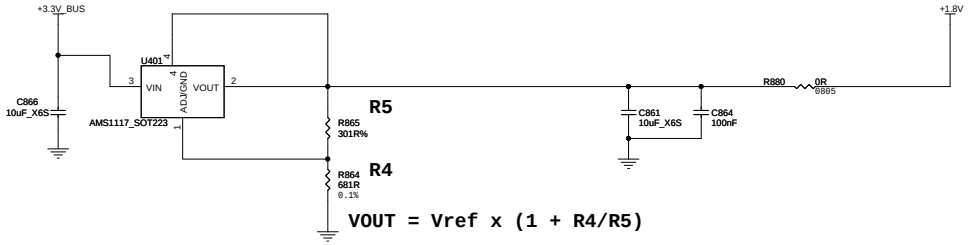
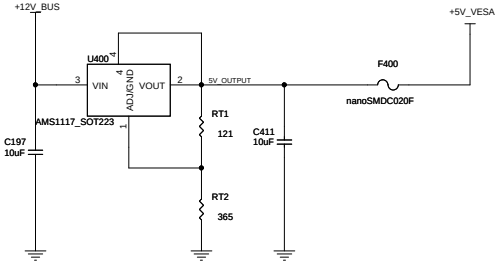
(13) Linear Regulators

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



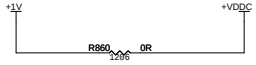
Regulators for +5V_VESA



Vout=1.25V* [1+(RT2/RT1)]

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA



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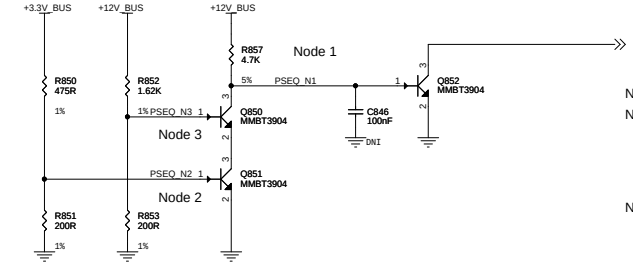
(14) Power Management

Power up/down Sequencing



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.

Node 1

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

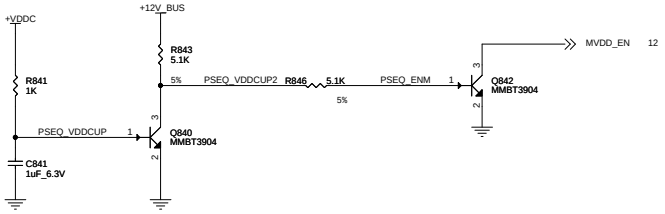
Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

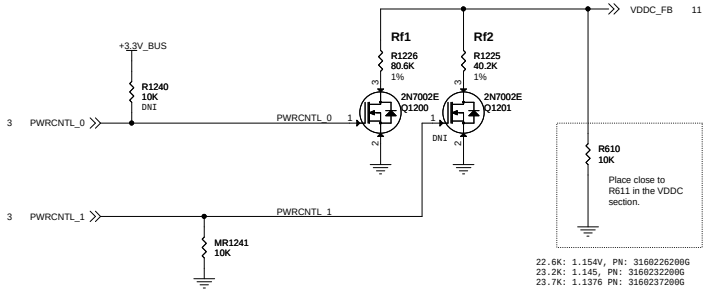
When +12V_BUS ramps above min Vbe, SMPS_EN will be held low



Power Play

VDDC Voltage Settings Using GPIOs

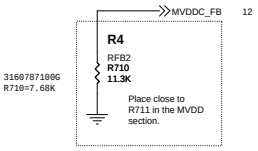
PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=		Rf1= Rf2=	Rf1= Rf2=	
0	0					
0	1					
1	0					
1	1	1	0	1		**Power-up Default**



MVDD Voltage Settings Using GPIOs

PWRCNTL_2 GPIO_6	Output Voltage (V) Rf1= Rf2=		Rf1= Rf2=	Rf1= Rf2=	
0					
1	1	0	1		**Power-up Default**

11.32k-ohm (3160113200G), Vout = 1.507V



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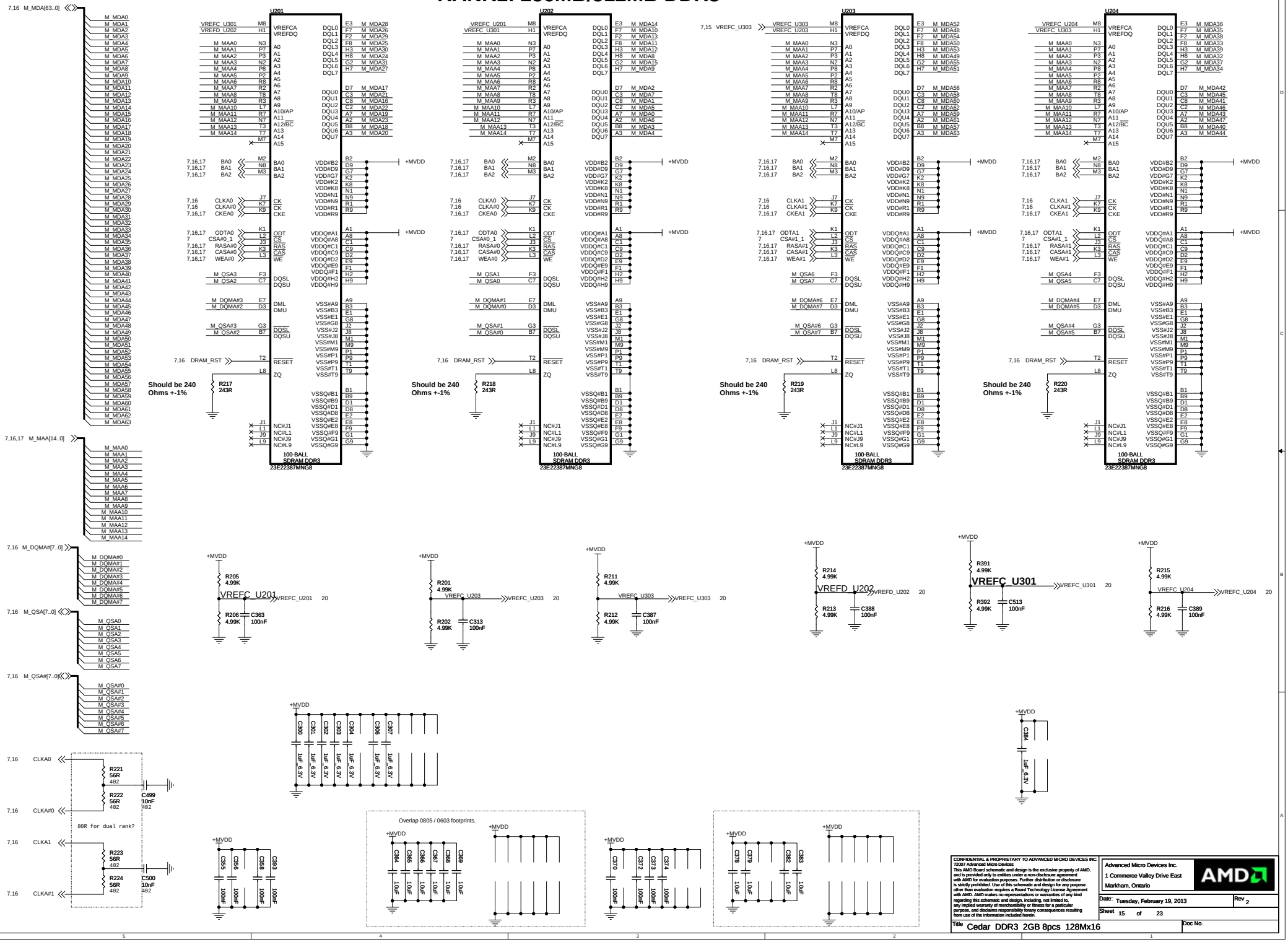
(15) DDR3 RANK1

RANK1: 256MB/512MB DDR3



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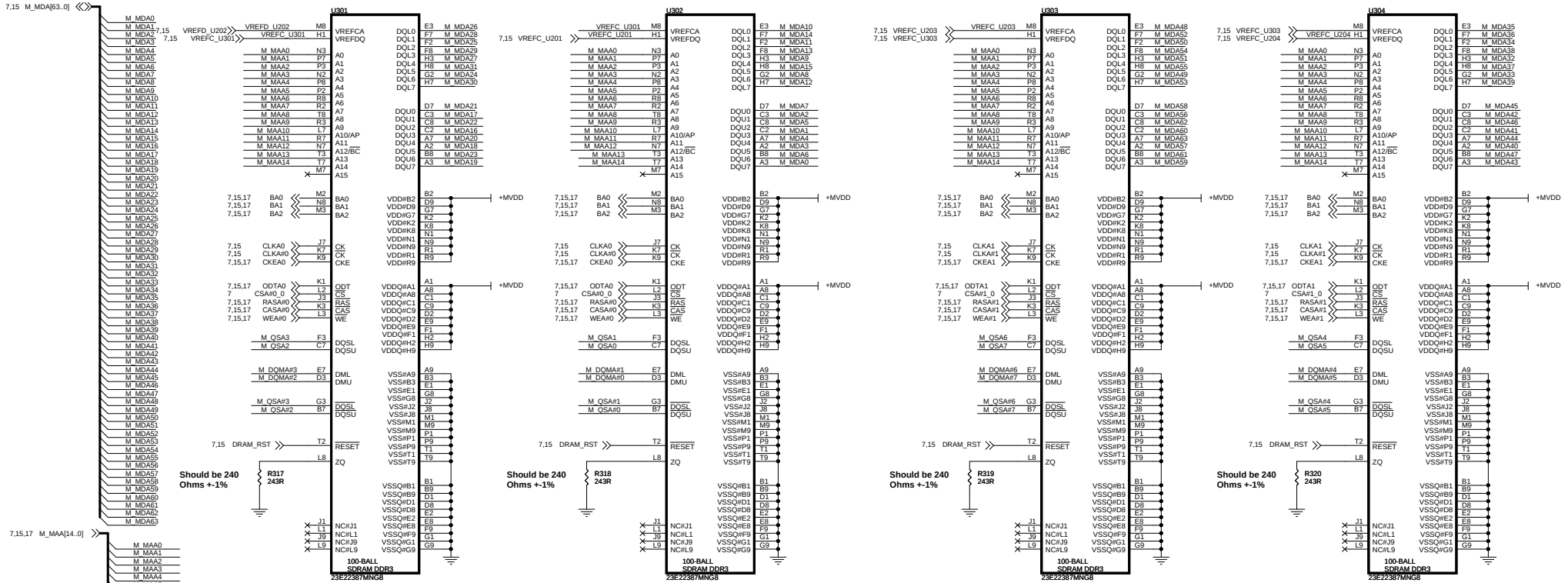
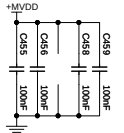
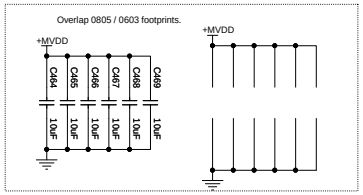
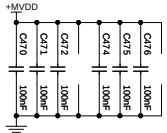
(16) DDR3 RANK2

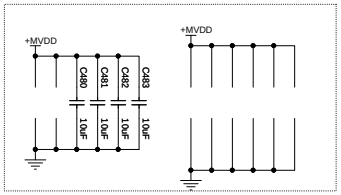
RANK2: 256MB/512MB DDR3

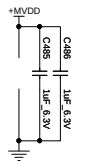












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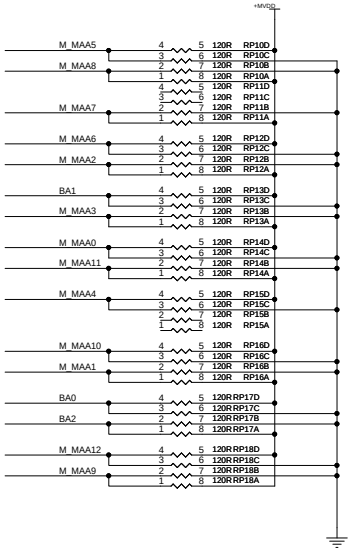
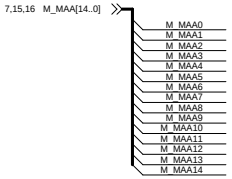
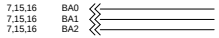
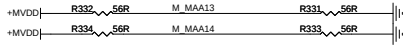
(17) DDR3 Termination









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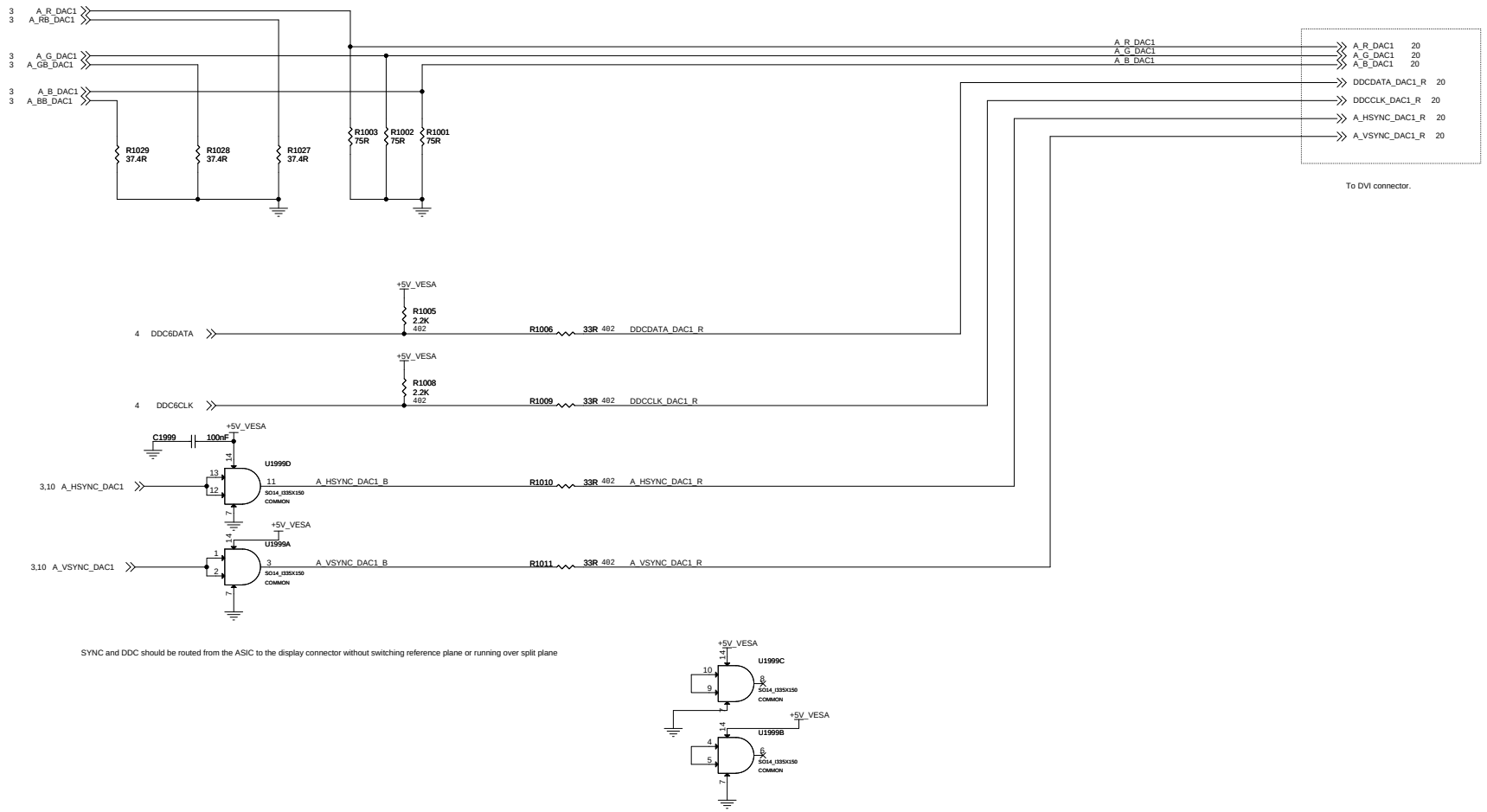
(18) DAC1 OUTPUT

DAC 1 OUTPUT

Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)



SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

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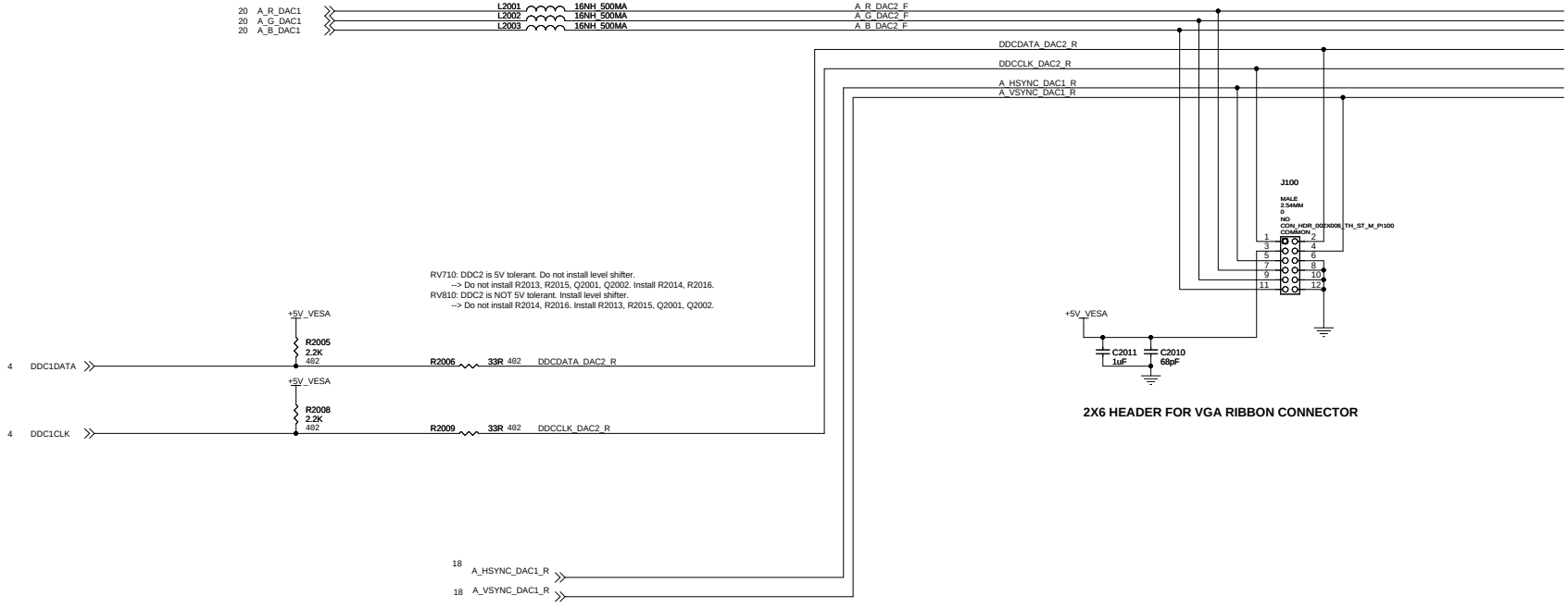
(19) DAC2 OUTPUT

DAC 2 OUTPUT

Place close to Connector

Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane



SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

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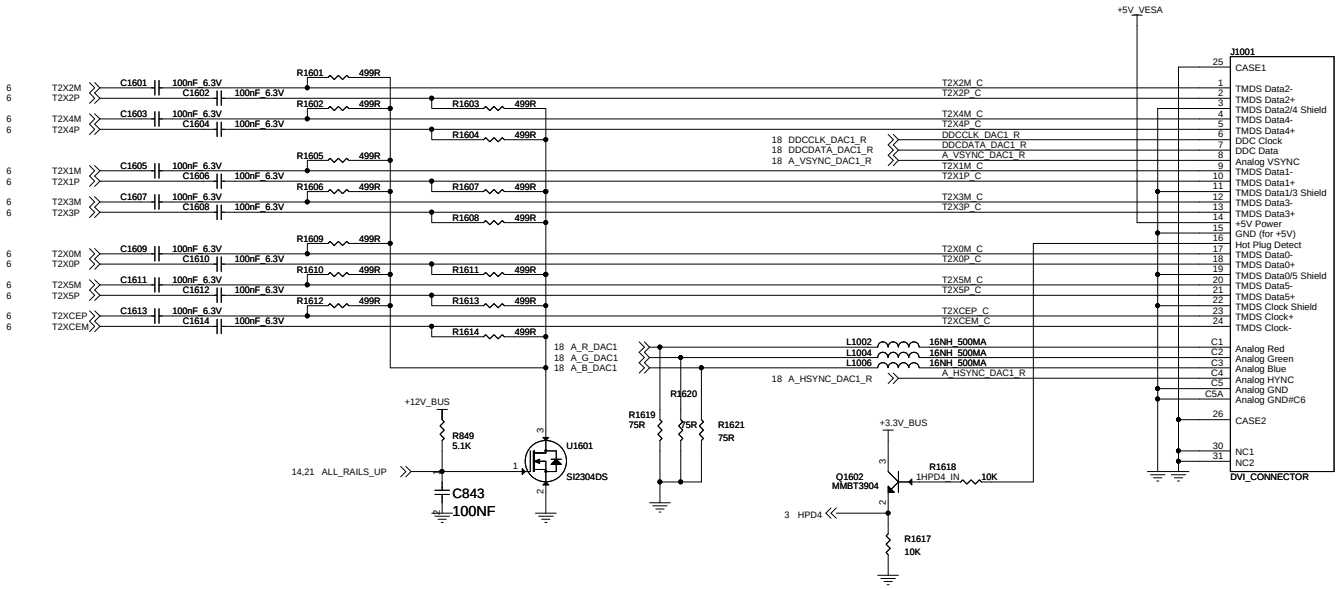
(20) DVI OUTPUT

DPE / DPF OUTPUT



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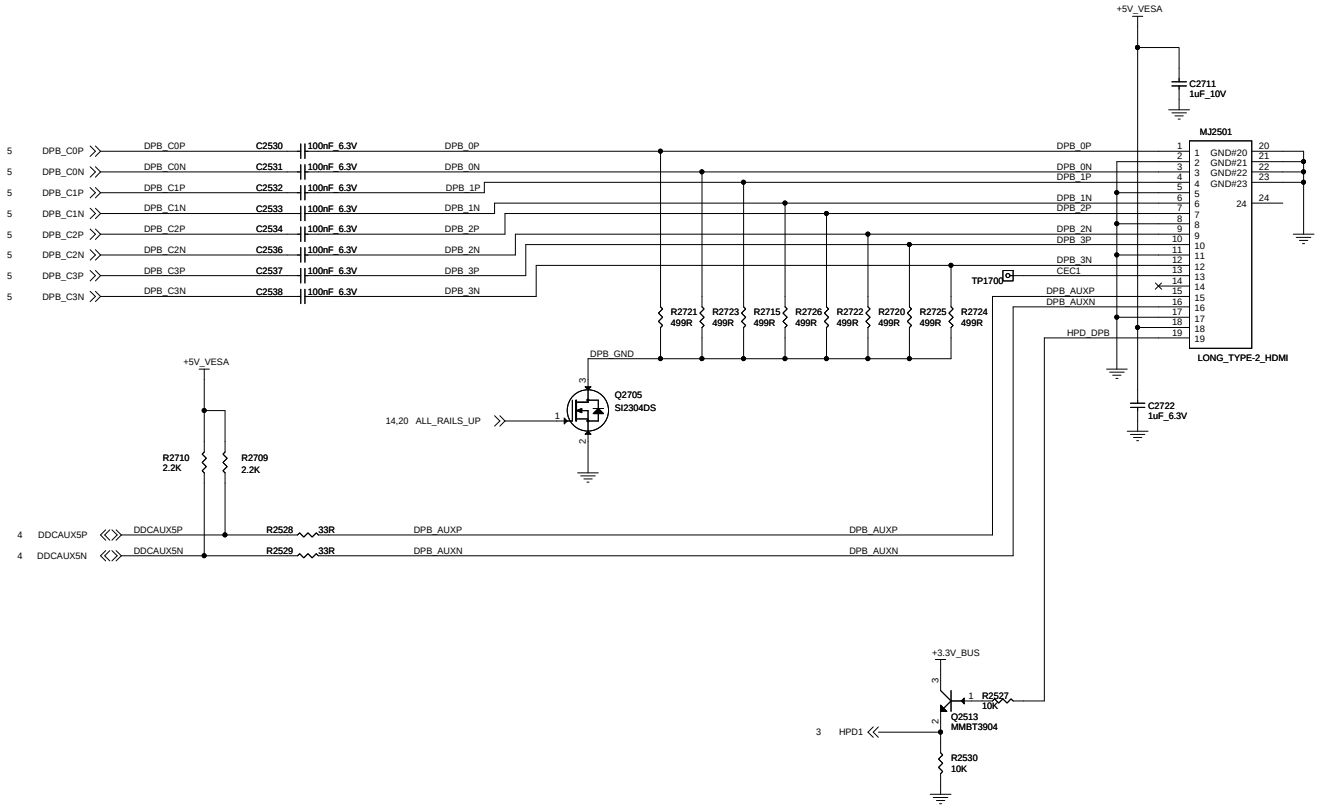
HDMI



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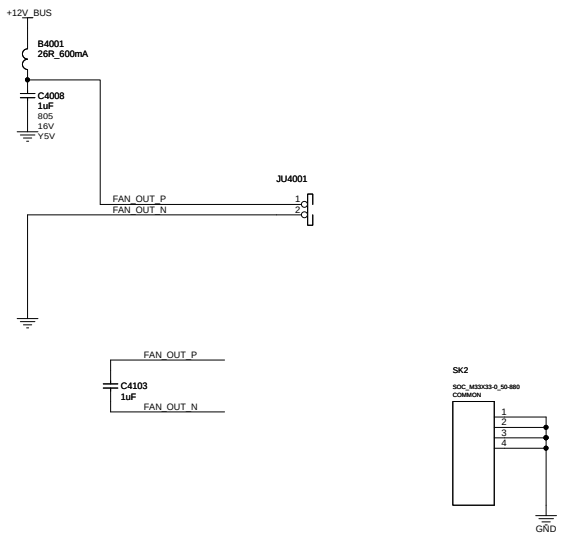
(22) Thermal Management



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For DVI Connector

ASSY-SCREW200
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW201
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

Bracket Components

ASSY-SCREW202
SCREW
SCREW

7020005200G

H3
HEATSINK

Square Fansink 12W

7120036200G BLACK
7120336200G RED

Rectangular Fansink 22W

7120035100G

SKU	P/N	CONFIGURATION	Form Factor
WALLEYE	8020051300G	DVI + DP + VGA	FH / SS
	8020051400G	DVI +HDMI+ VGA	FH / SS
	8020051700G	DVI + DP + VGA	FH / DS
	80200517A0G	DVI +HDMI+ VGA	FH / DS

Dual-slot Heatsink 14W

7120181000G

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