GDDR6X SGRAM

MT61K256M32

2 Channels x 256 Meg x 16 I/O, 2 Channels x 512 Meg x 8 I/O

Features

- V_{DD}, V_{DDQ} = 1.35V ±3% and 1.25V ±3%
- V_{PP} = 1.8V -3%/+6%
- 2 separate independent channels (x16)
- x16/x8 mode configurations set at reset
- Single ended interfaces per channel for command/ address (CA) and data
- Differential clock input CK_t/CK_c for CA per 2 channels
- One differential clock input WCK_t/WCK_c per channel for data (DQ, DQX, EDC)
- Double data rate (DDR) command/address (CK)
- Double data or symbol rate-data (WCK)
- $16n$ prefetch architecture
- 16 internal banks
- 4 bank groups
- Programmable read latency
- Programmable write latency
- Write data mask function via CA bus with single and double byte mask granularity
- CA bus inversion (CABI)
- CA bus training via DQ/ DQX/EDC signals
- WCK2CK clock training via EDC signals
- Data read and write training via FIFO (depth = 16)
- Read/write data transmission integrity secured by cyclic redundancy check CRC
- Programmable CRC read latency
- Programmable CRC write latency
- Programmable EDC hold pattern for CDR
- RDQS mode on EDC pins
- Programmable data encoding (MTA)
- Low power modes
- On-chip temperature sensor with read-out
- Auto precharge option for each burst access
- Auto refresh modes (32ms, 16k cycles)
- Temperature sensor controlled self refresh rate
- Hibernate self refresh mode with V_{DDQ} off option
- Digital t_{RAS} lockout
- On-die termination (ODT) for all high-speed inputs

- Pseudo open drain (POD135 and POD125) compatible CA, CK and WCK inputs
- ODT and output driver strength auto-calibration with external resistor ZQ pin (360Ω)
- Internal V_{REF} for data inputs
- Selectable external or internal V_{REF} for CA inputs
- Vendor ID for device identification
- IEEE 1149.1 compliant boundary scan
- 180-ball BGA package
- Lead-free (RoHS-compliant) and halogen-free packaging
- T_C = 0°C to +95°C

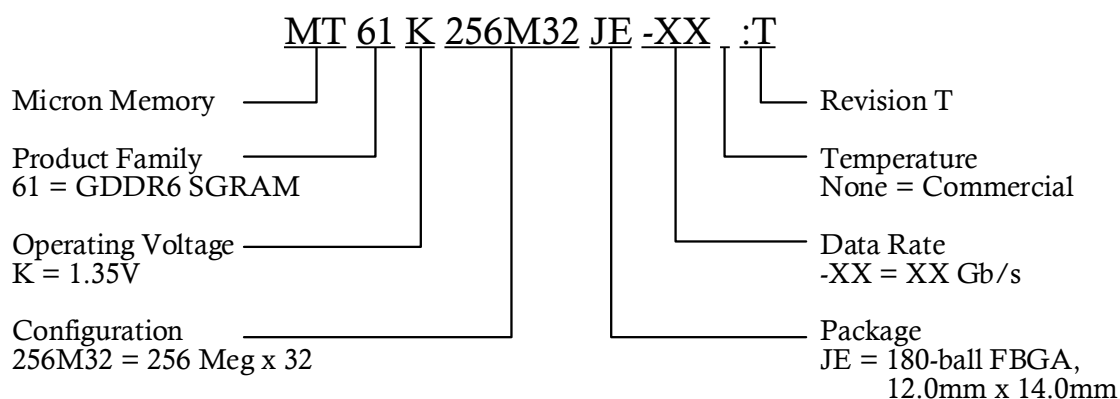## Options[1]   Marking

- Organization
  – 256 Meg x 32 (words x bits)   256M32
- FBGA package
  –180-ball (12mm x 14mm)   JE
- Timing – maximum data rate
  –XX Gb/s   -XX
- Operating temperature
  – Commercial (0°C ≤ T_C ≤ +95°C)   None
- Revision   :T

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Products and specifications discussed herein are subject to change by Micron without notice.

Figure 1: Part Numbering

MT 61 K 256M32 JE -XX :T

Micron Memory

Product Family
61 = GDDR6 SGRAM

Operating Voltage
K = 1.35V

Configuration
256M32 = 256 Meg x 32

Revision T

Temperature
None = Commercial

Data Rate
-XX = XX Gb/s

Package
JE = 180-ball FBGA,
    12.0mm x 14.0mm

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking
that is different from the part number. For a quick conversion of an FBGA code, see the
FBGA Part Marking Decoder on Micron's web site: http://www.micron.com.

Important Notes And Warnings

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Package Dimensions

Figure 2: 180-Ball FBGA
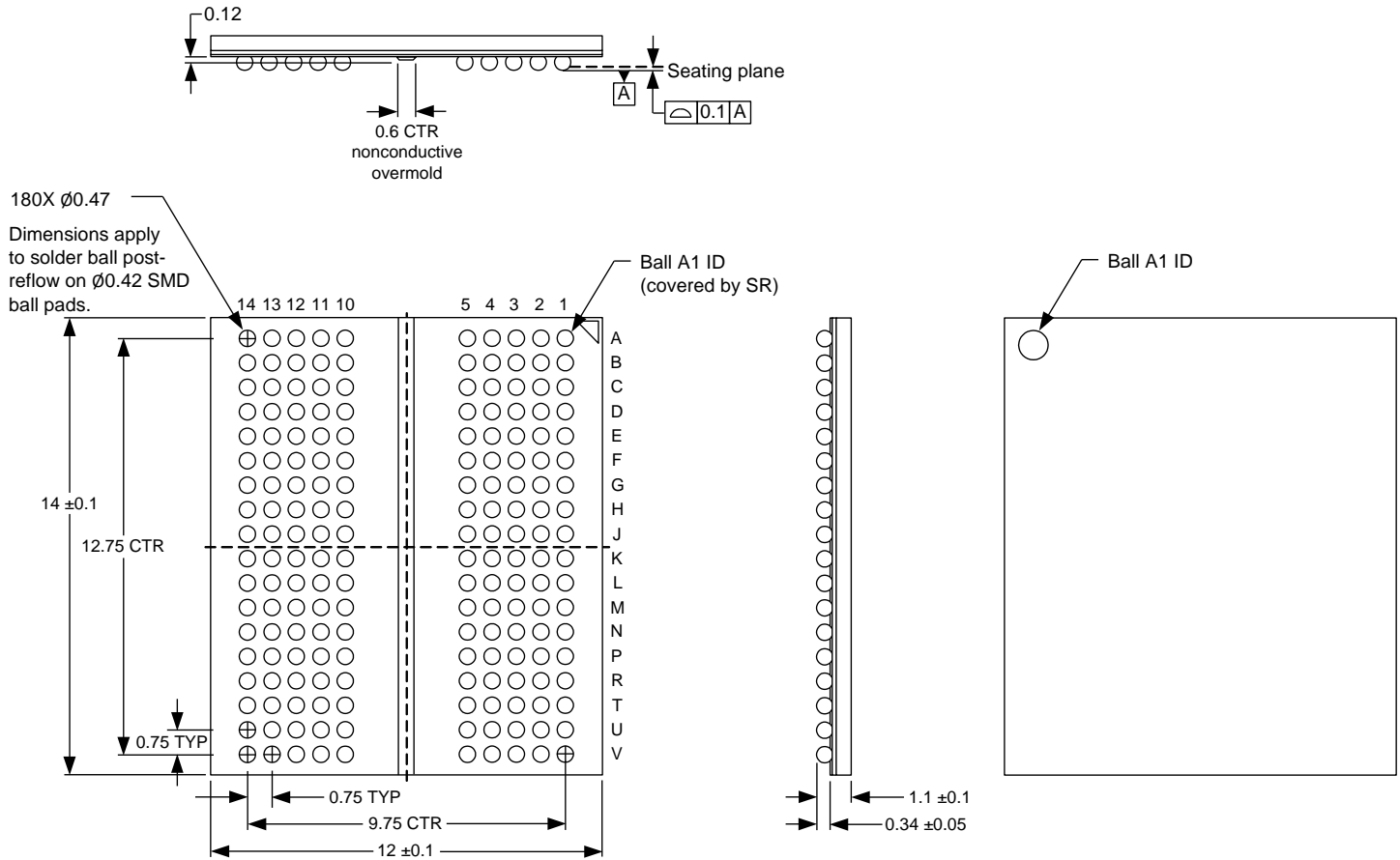
Notes:
1. Package dimension specification is compliant to JC11 MO328 Variation PBGA-B180[252]_I0p75-R12p0x14p0Z#-C0p525Z0p22.
2. All dimensions are in millimeters.
3. Solder ball material: SAC-Q (92.5% Sn, 4% Ag, 3% Bi, 0.5% Cu)