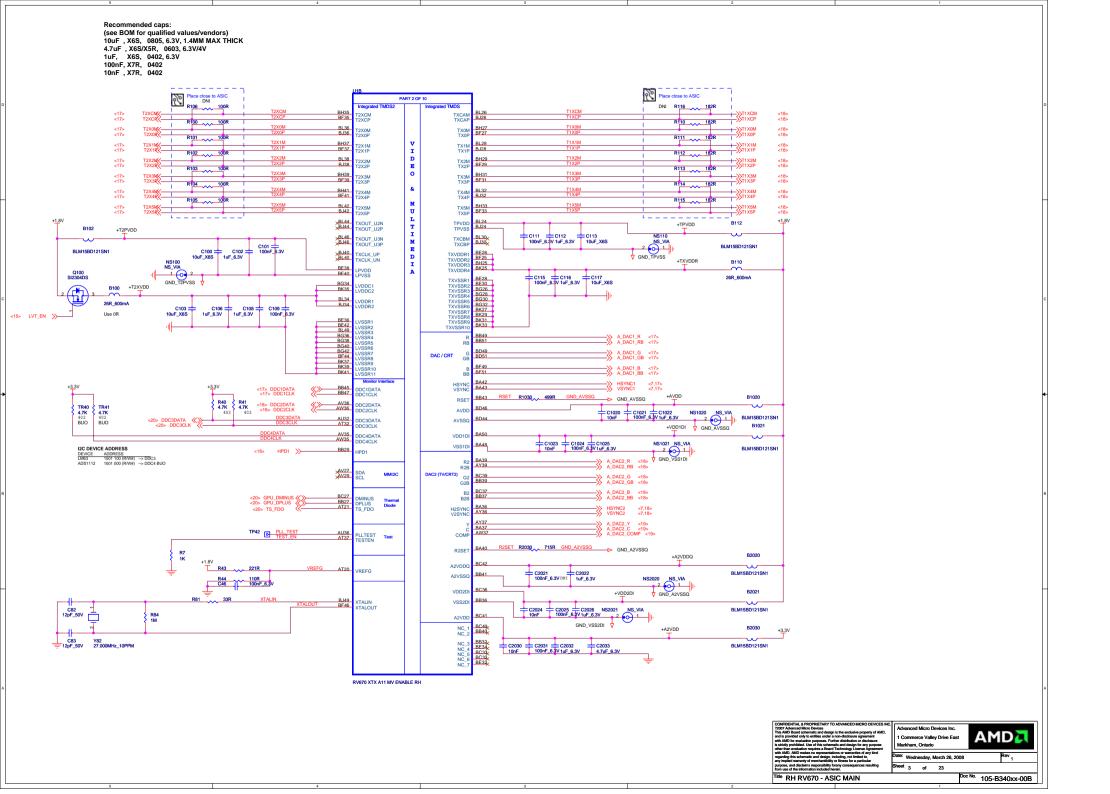
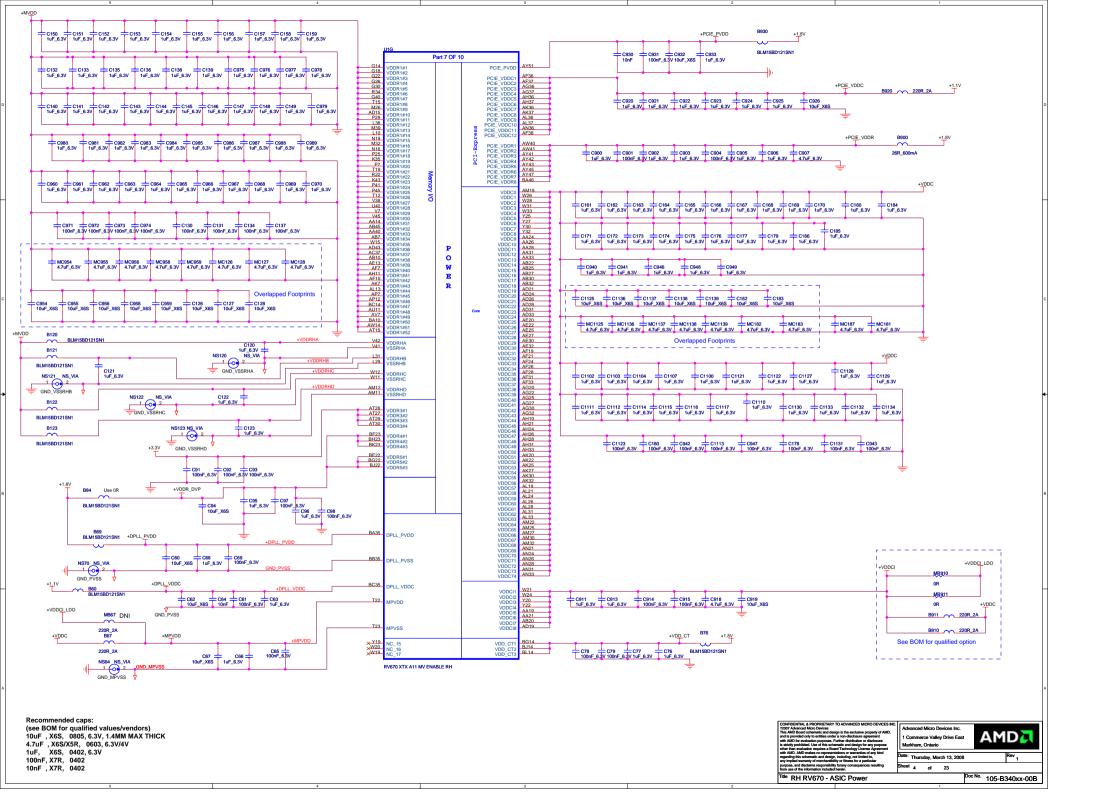
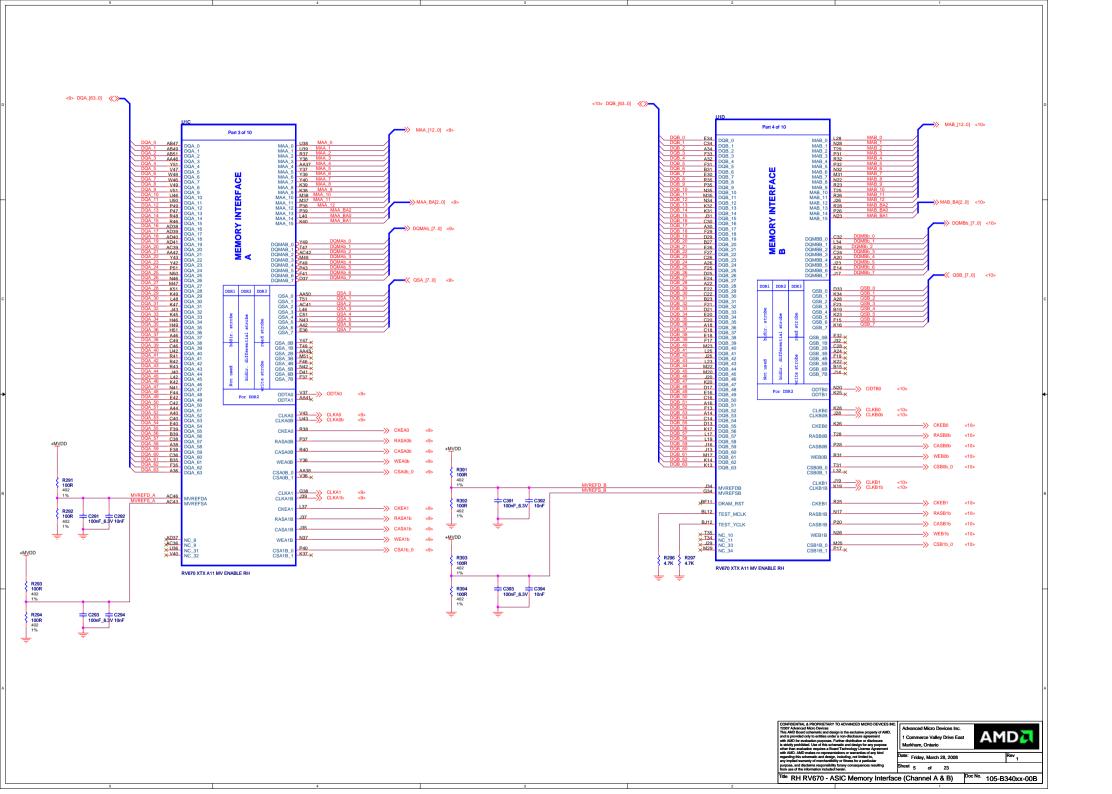
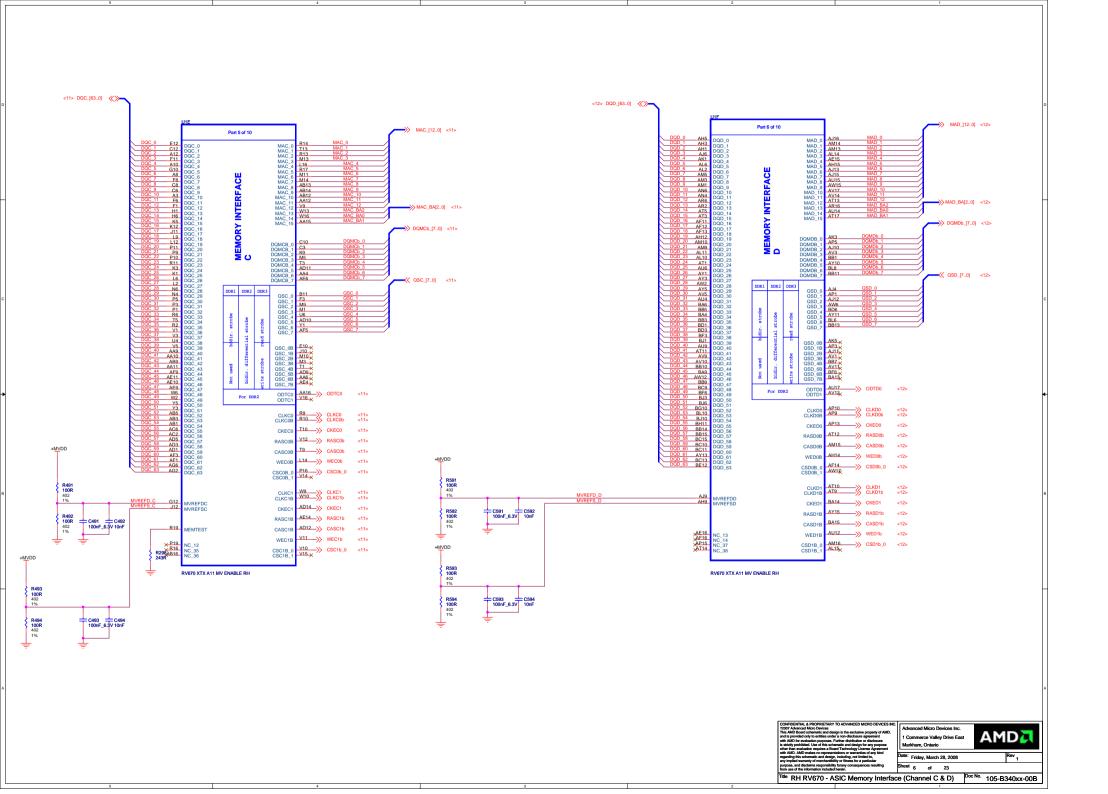


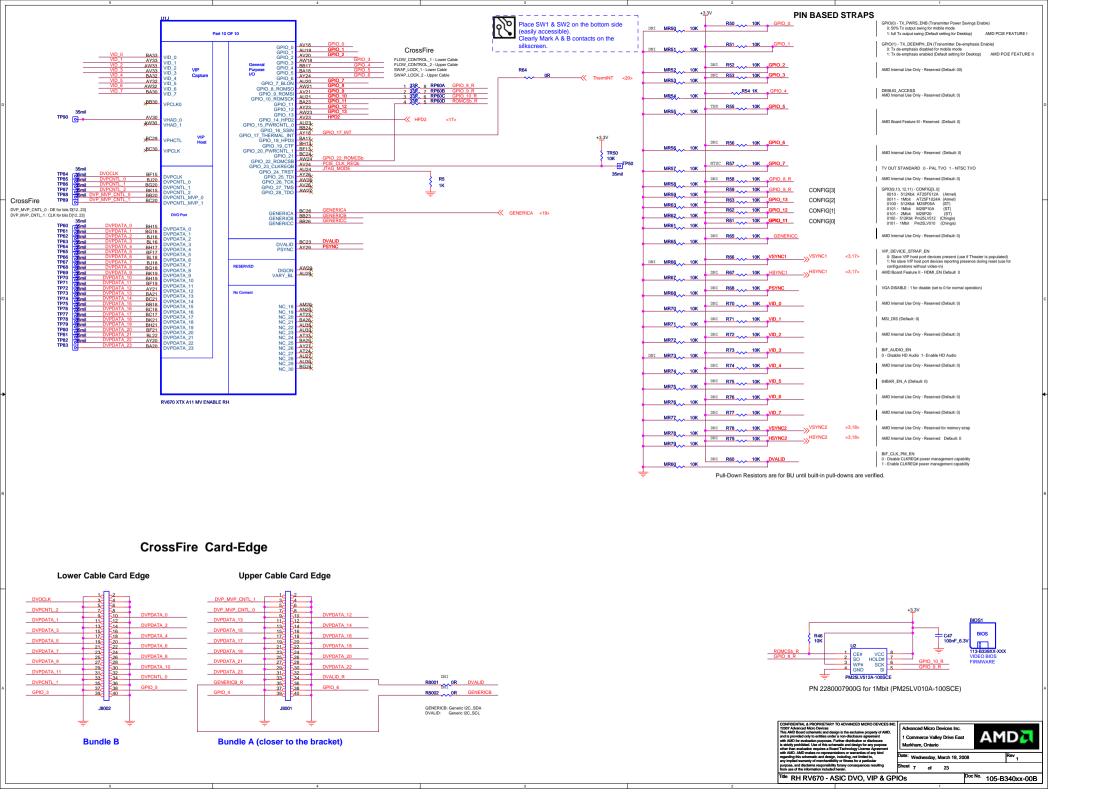
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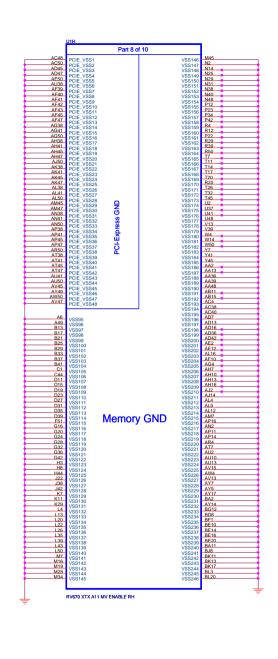


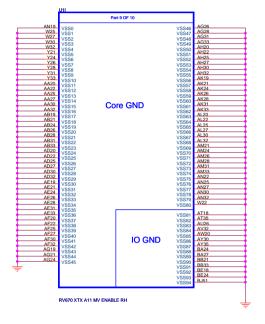












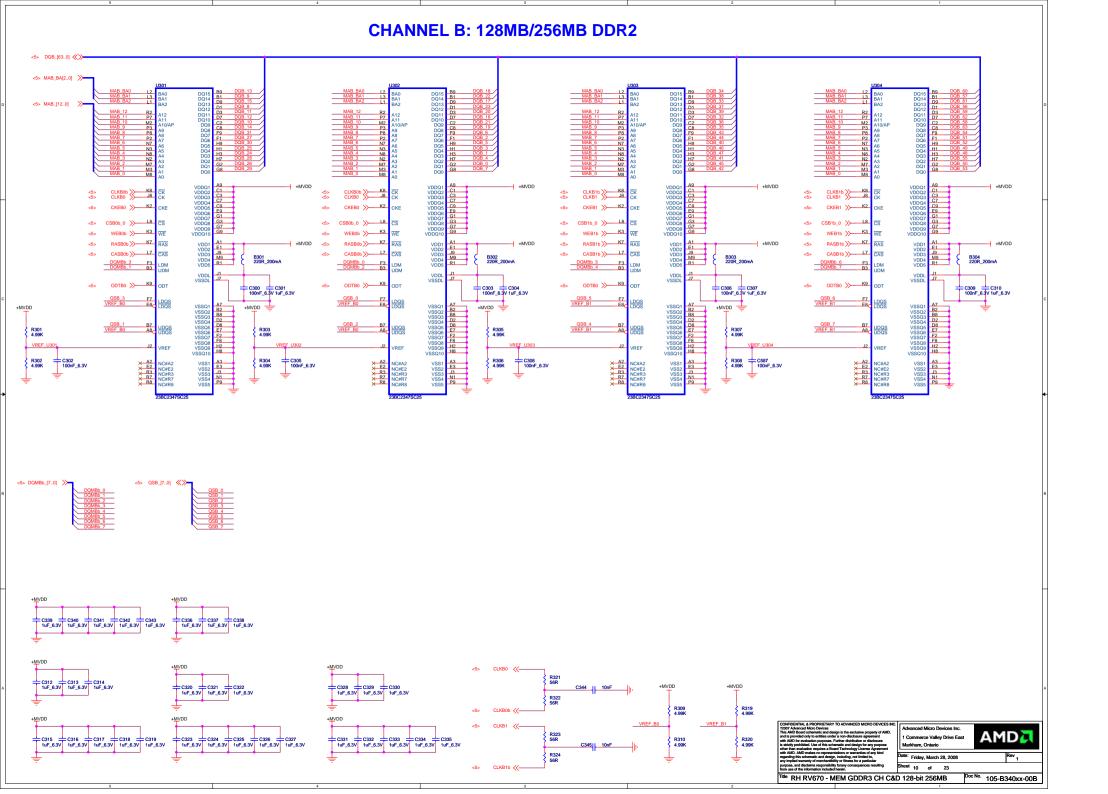
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ADVANCED MOTO Devices Inc.
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Date: Thursday, March 13, 2008
Rev 1

Table: Thursday, March 13, 2008
Shed 8 of 23

Table: RH RV670 - ASIC Grounds

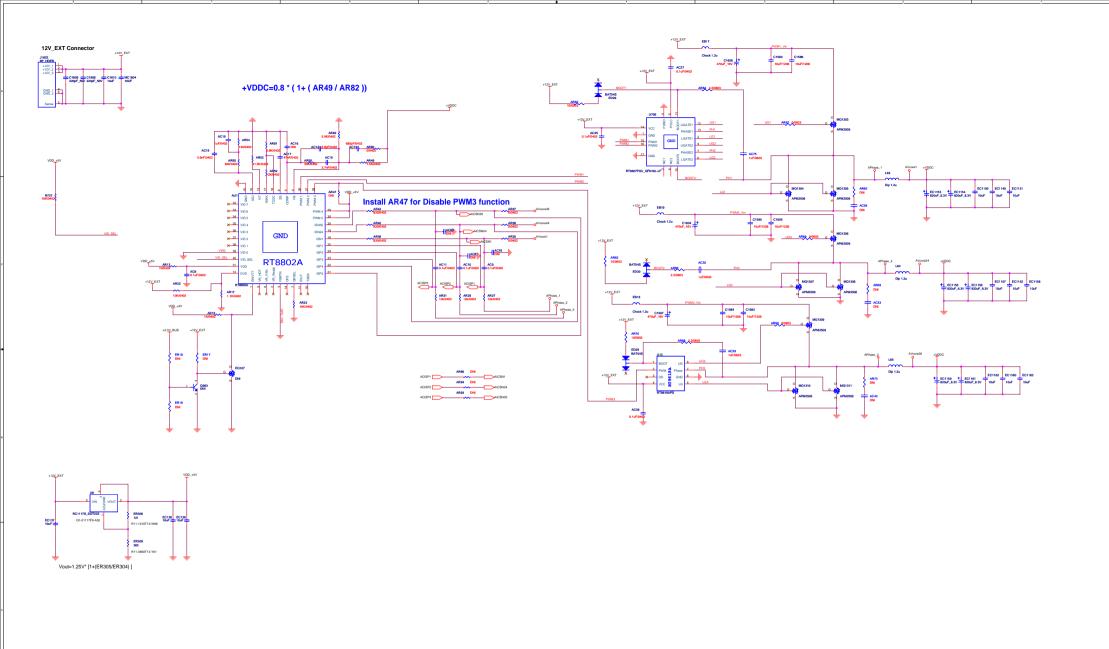
Table: Thursday, March 13, 2008
Doc No. 105-B340xx-00B

## CHANNEL A: 128MB/256MB DDR2 <5> DOA 163 01 (()) VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 B201 220R\_200mA B203 220R\_200mA C200 = C201 100nF\_6.3V 1uF\_6.3V C203 C204 100nF 6.3V 1uF 6.3V C206 C207 100nF\_6.3V 1uF\_6.3V C209 C210 +MVDD +MVDD VSSQ1 +MVDD = R203 4.99K └ +MVDD R208 4.99K <5> DQMAb [7..0] >> <5> QSA\_[7..0] >> C239 C240 C241 C242 C243 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V C236 C237 C238 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V <5> CLKA0 (<-C212 C213 C214 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V R222 56R R209 4.99K R219 4.99K CLKA0b //-+MVDD Commerce Valley Drive East C215 C216 C217 C218 C219 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V R220 4.99K Markham, Ontario C245 10nF Title RH RV670 - MEM GDDR3 CH A&B 128-bit 256MB Doc No. 105-B340xx-00B

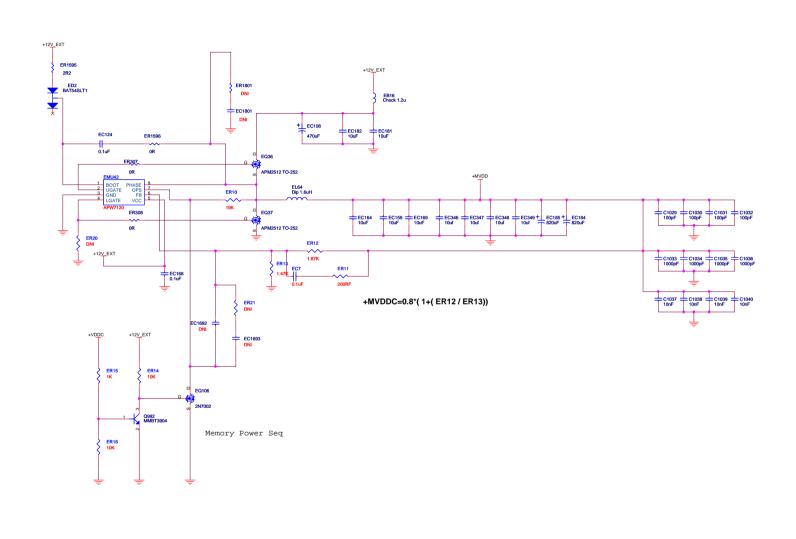


## CHANNEL C: 128MB/256MB DDR2 <6> DOC 163 01 (()) VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ7 VDDQ8 VDDQ9 VDDQ10 CLKC0b K8 CLKC0 J8 CLKC1b K8. CLKC1 J8 CLKC1b K8 CK RASC1b X RAS +MVDD CAS CAS CAS CASC1b >> L7 CAS B402 220R\_200mA B404 220R\_200mA VDDL VSSDL C403 C404 100nF\_6.3V 1uF\_6.3V C409 C410 100nF\_6.3V 1uF\_6.3V C400 = C401 100nF\_6.3V 1uF\_6.3V + C406 + C407 100nF 6.3V 1uF 6.3V VSSQ1 A7 VSSQ2 B2 VSSQ3 B8 VSSQ4 D2 VSSQ5 D8 VSSQ6 F7 VSSQ6 F2 VSSQ7 F8 VSSQ8 H2 VSSQ9 H2 VSSQ10 VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 +MVDD = +MVDD UDQS UDQS UDQS R401 4.99K R405 4.99K VSSQ7 VSSQ8 VSSQ9 R402 4.99K R406 4.99K VSS1 VSS2 VSS3 VSS4 VSS5 NC#A2 NC#E2 NC#R3 NC#R7 NC#R8 <6> DQMCb\_[7..0] >> C439 C440 C441 C442 C443 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V C436 C437 C438 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V CLKC0 ((-C420 C421 C422 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V C412 C413 C414 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V R409 4.99K R419 4.99K CLKC0b //-+MVDD +MVDD C431 C432 C433 C434 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V C423 C424 C425 C426 C427 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V C415 C416 C417 C418 C419 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V R410 4.99K R420 4.99K C445 10nF

## CHANNEL D: 128MB/256MB DDR2 DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9 DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9 DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ1 <6> MAD\_[12..0] >> VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ1( VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ10 VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 RAS VDD1 VDD2 VDD3 VDD4 VDD5 VDD1 VDD2 VDD3 VDD4 VDD5 VDD1 VDD2 VDD3 VDD4 VDD5 CAS CAS VDDL VSSDL C500 C501 100nF\_6.3V 1uF\_6.3V C503 C504 100nF\_6.3V 1uF\_6.3V VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 VSSQ10 VSSQ1 B8 VSSQ3 VSSQ4 VSSQ5 P5 VSSQ6 F7 VSSQ6 VSSQ7 VSSQ9 VSSQ10 H8 VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 +MVDD R501 4,99K R507 4.99K R503 4,99K R505 4.99K R502 4.99K C502 100nF\_6.3V R504 4.99K R506 4.99K R508 4.99K VSS: VSS: VSS: VSS: VSS: VSS1 VSS2 VSS3 VSS4 VSS5 VSS1 VSS2 VSS3 VSS4 VSS5 VSS1 VSS2 VSS3 VSS4 VSS5 <6> DQMDb\_[7..0] >> <6> QSD\_[7..0] 《》 C536 C537 C538 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V CLKD0 <<-C520 C521 C522 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V C528 C529 C530 1uF\_6.3V 1uF\_6.3V 1uF\_6.3V R317 4.99K R326 4.99K CLKD0b //-+MVDD R330 4.99K R329 56R



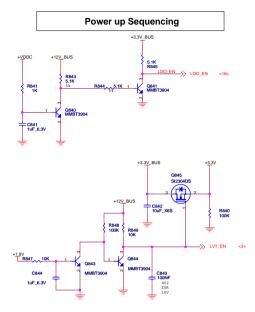




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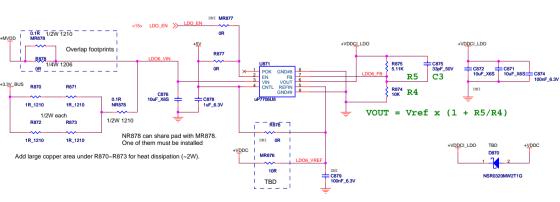
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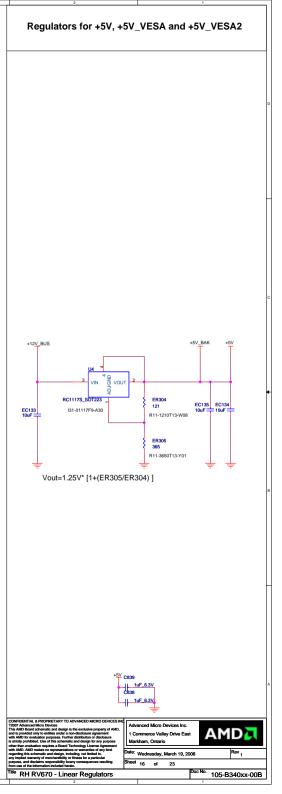


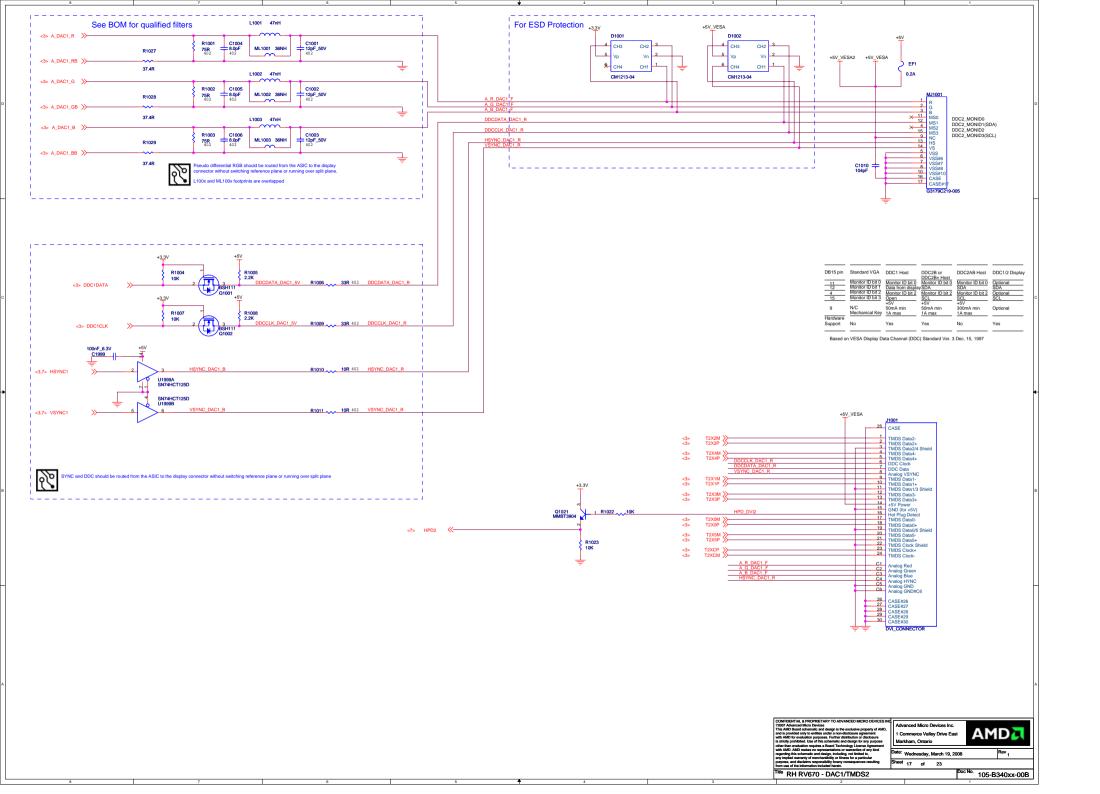
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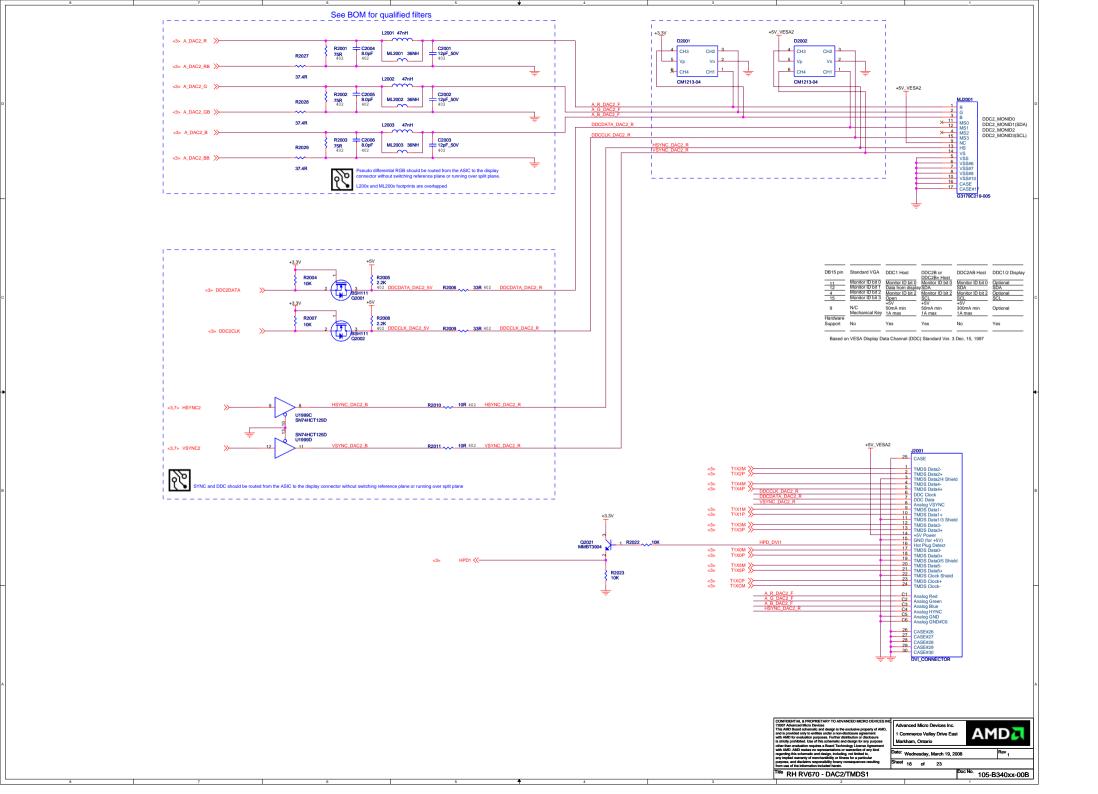
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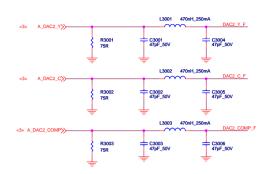
LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% lout = 0.8A (TBV) RMS MAX PCB: 50 to 70mm sq. copper area for cooling Overlap footprints C865 33pF\_50V R5 VOUT = Vref x (1 + R5/R4)LDO #3: Vin = +1.70V to 2.1VMAX Vout = +1.1V +/- 3% lout = Up to 1.3A (TBV) RMS MAX PCB: 50 to 70mm sq. copper area for cooling Overlap footprints R858 R855 C855 33pF\_50V R5 R854 R4 VOUT = Vref x (1 + R5/R4)LDO #6: For fixed output voltage: Vin = +1.70V to 2.1V MAX Vout = +1.20V +/- 3% lout = 1.3A (TBV) RMS MAX PCB: 50 to 70mm sq. copper area for cooling LDO #6: For tracking VDDC: Vin = TBD Vout = TBD Iout = 1.3A (TBV) RMS MAX PCB: 50 to 70mm sq. copper area for cooling Overlap footprints R5 C3 R874 R4 1R\_1210

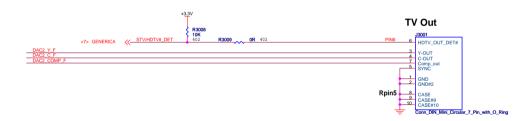












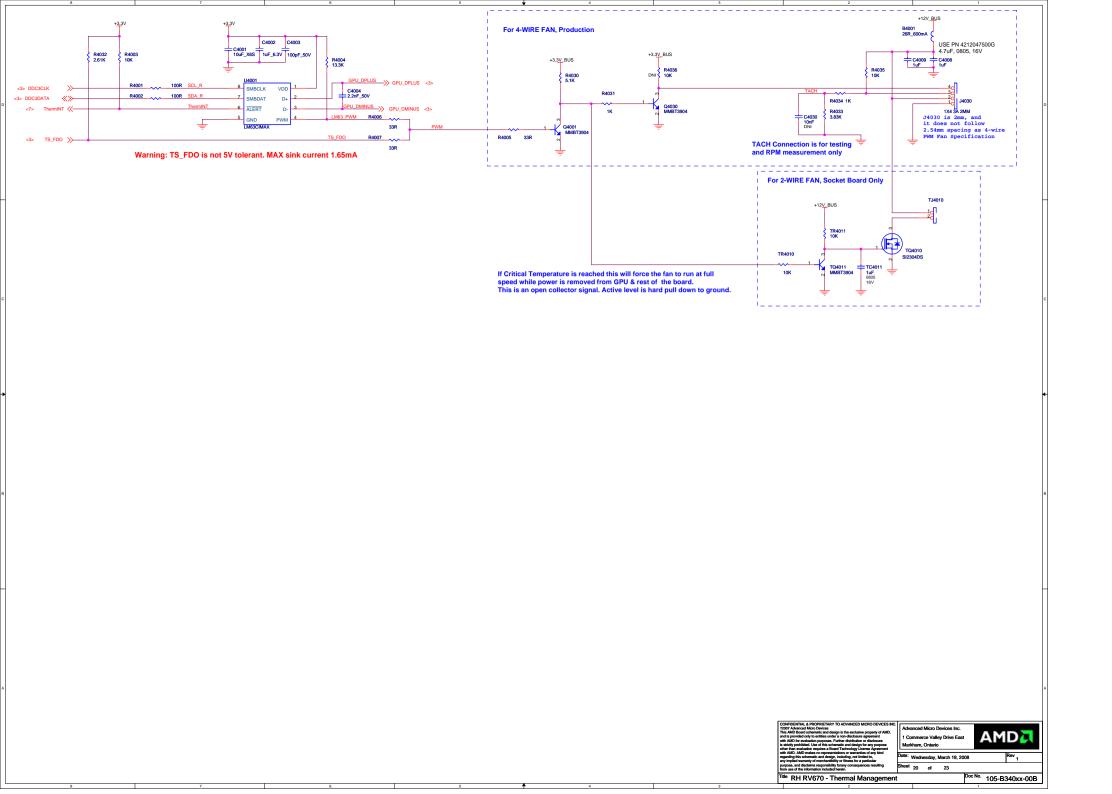
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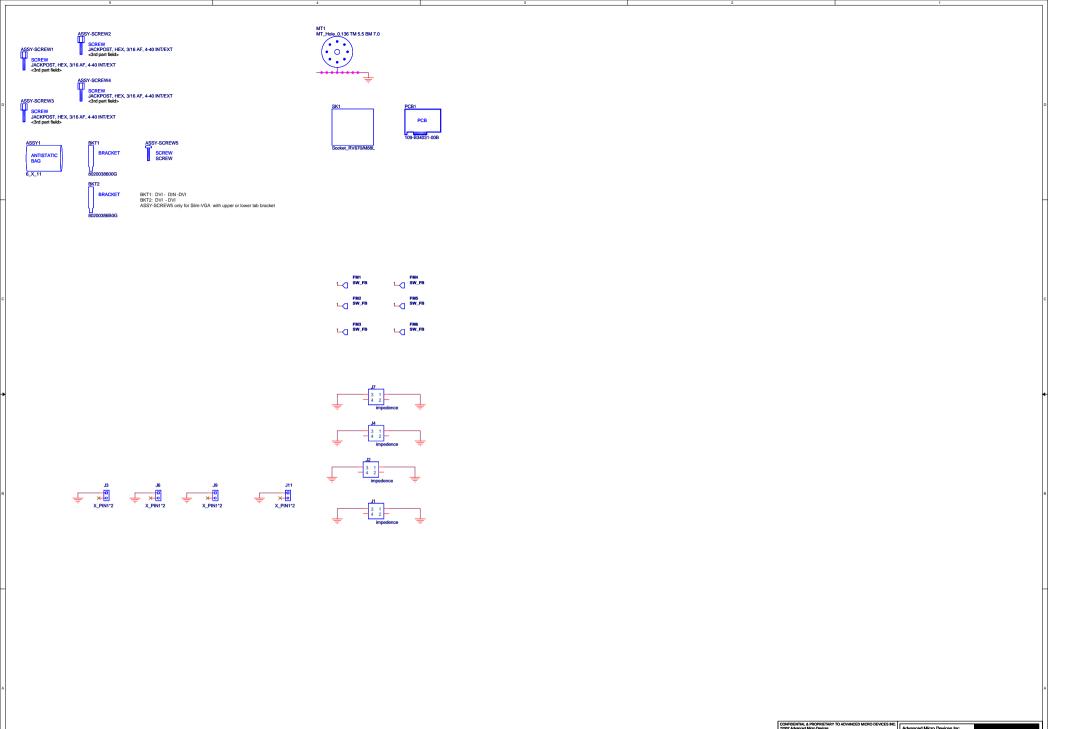
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	Δ	МГ	5	Title RH PCIE RV670 512MB GDDR3 DUAL DL-DVI-I VO F	1	Schematic No. 105-B340xx-00B	Date: Thursday, March 1	3, 2008	
AMD			REVISION HISTORY	For Stuffing options (con	hts the PCB, it does not represent any specific SKU.  In ponent values, DNI , ? please consult the product specific BOM.  In prosentative to obtain latest BOM closest to the application desired.				
	Sch Rev	PCB Rev	Date	RE	REVISION DESCRIPTION				
	0	A00	07/05/11	Initial design for RV670 GDDR3 (Revival) based on B339					
	1	00B	07/08/1	(pg 1) Adding R1 and connecting switch #7 of TSW1. Some mother boards require B7 to be grounded. Table-1 updated accordingly (pg 7) Adding R64 and MR64 to select HOT_PLUG_DET or ThermINT as the interrupt source. (pg 13) Adding R1617, MR1617, R1616, Q1613, R1615, R1618, and R1619 as option to support hot plug detection of external cable. (pg 13) Adding R1282, MR1282, R1283, MR1283, R1284, R1281, R1285, Q1280, and C1280 as option for thermal protection for VDDC SMPS MOSFETs (pg 13) Adding MC1603 (overlapped with C1603) (pg 14) Adding D870 as option for power up sequencing (pg 18) Adding heatsink symbol/footprint (Layout) Increasing spacing between DDC4DATA & DDC4CLK going to U1270 to reduce the crosstalk					
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