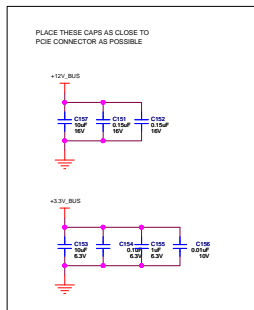
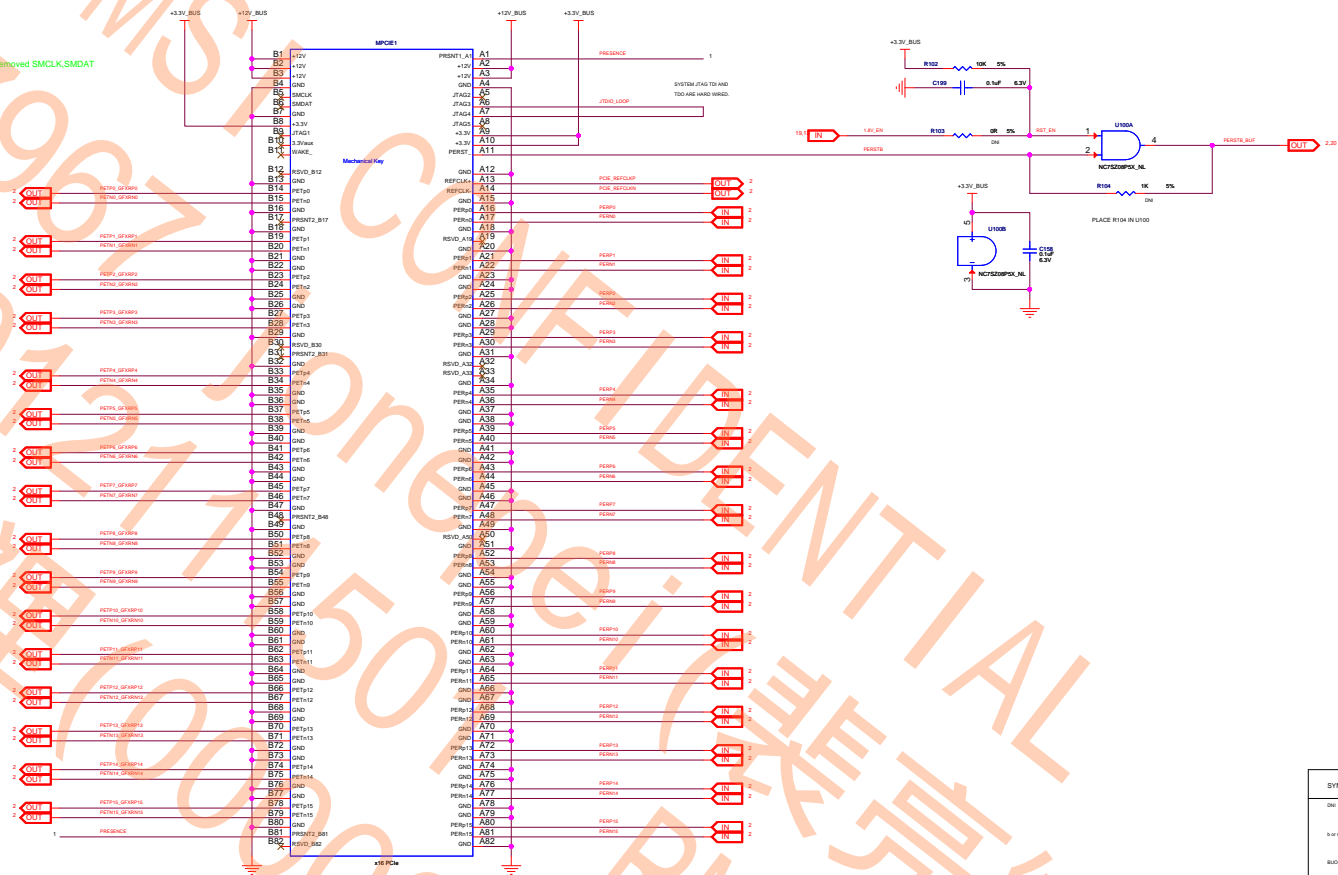




(1) PCI-EXPRESS EDGE CONNECTOR



FOR BILL, ONE BOTH TRANSISTOR
AND SERIES RESISTORS
(Q100, R107, R108)



SYMBOL LEGEND	
DN:	DO NOT INSTALL
o or #	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND



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<TID

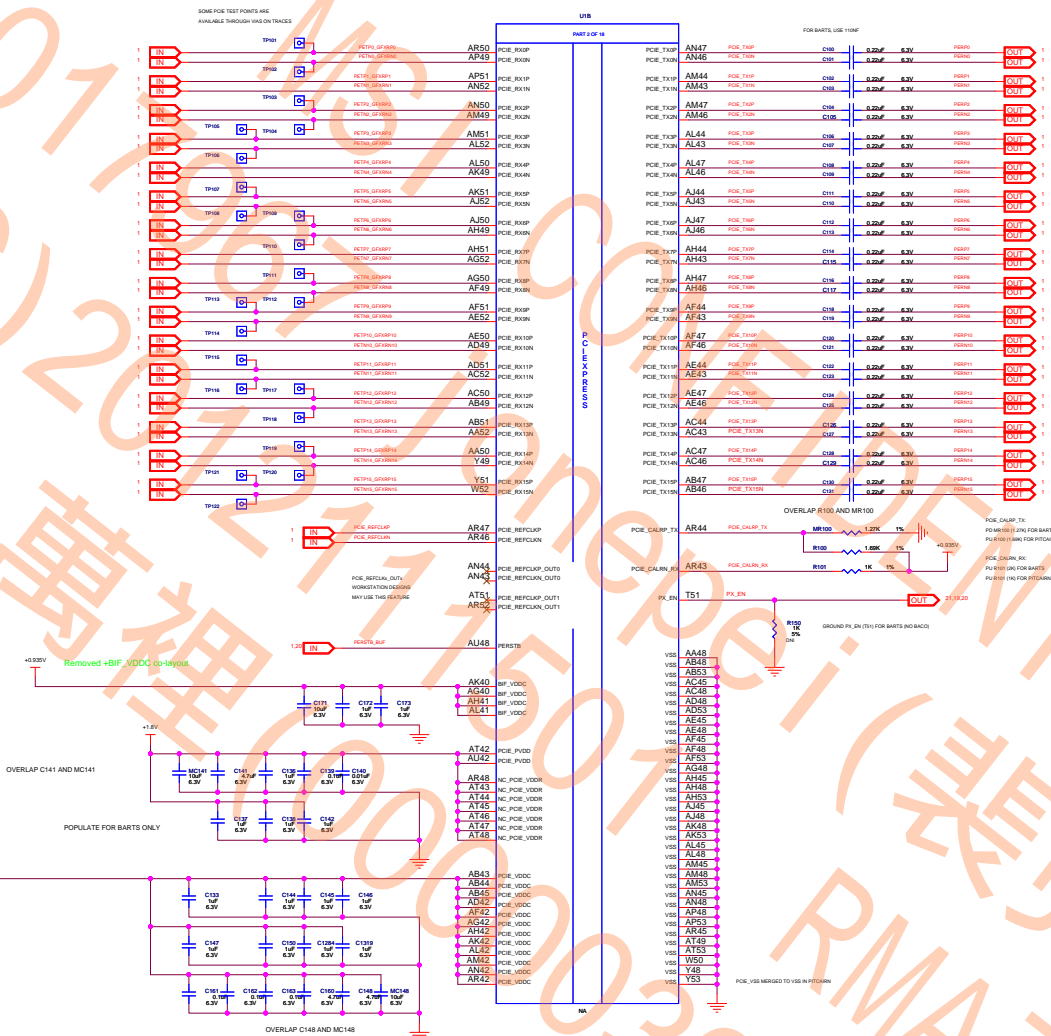
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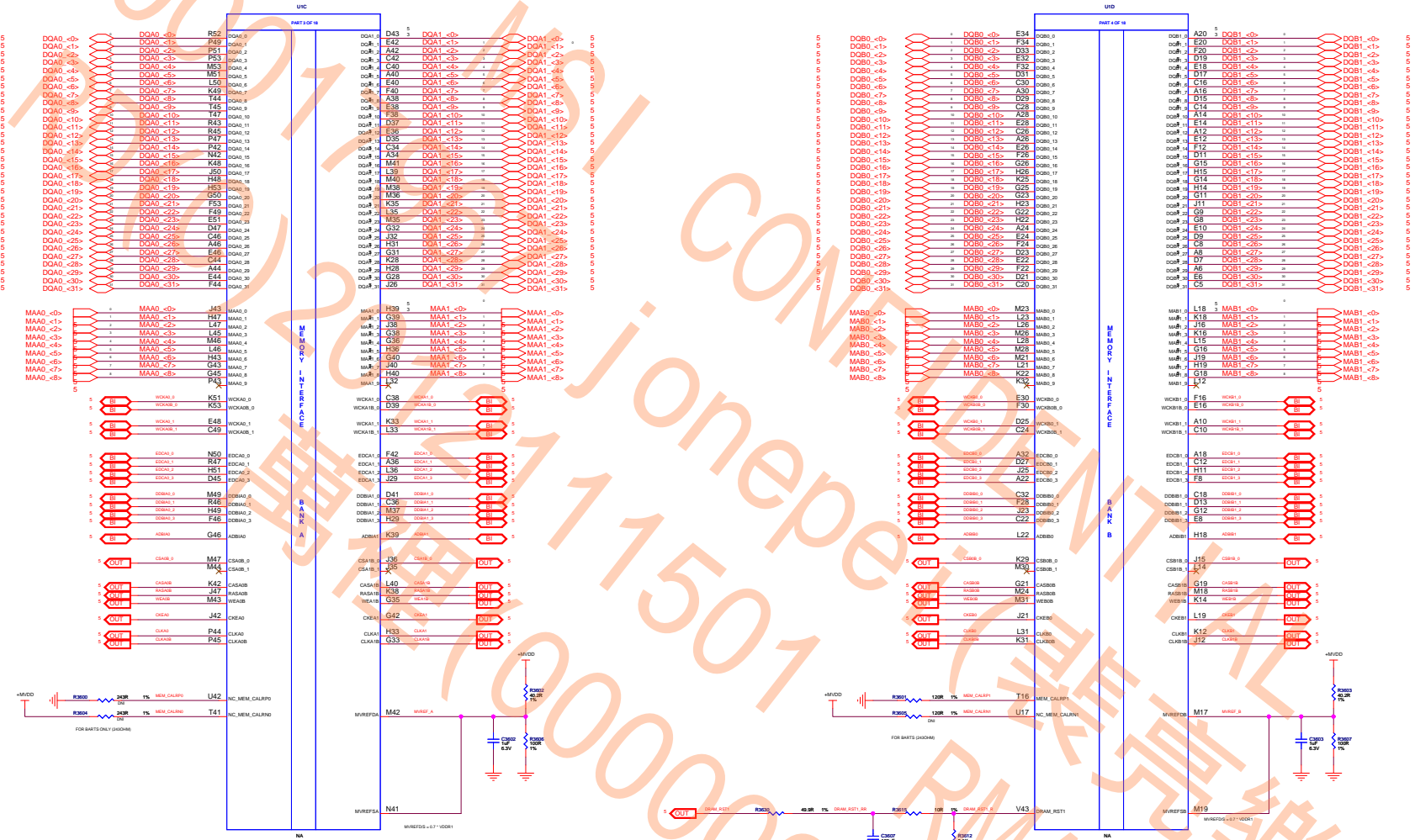
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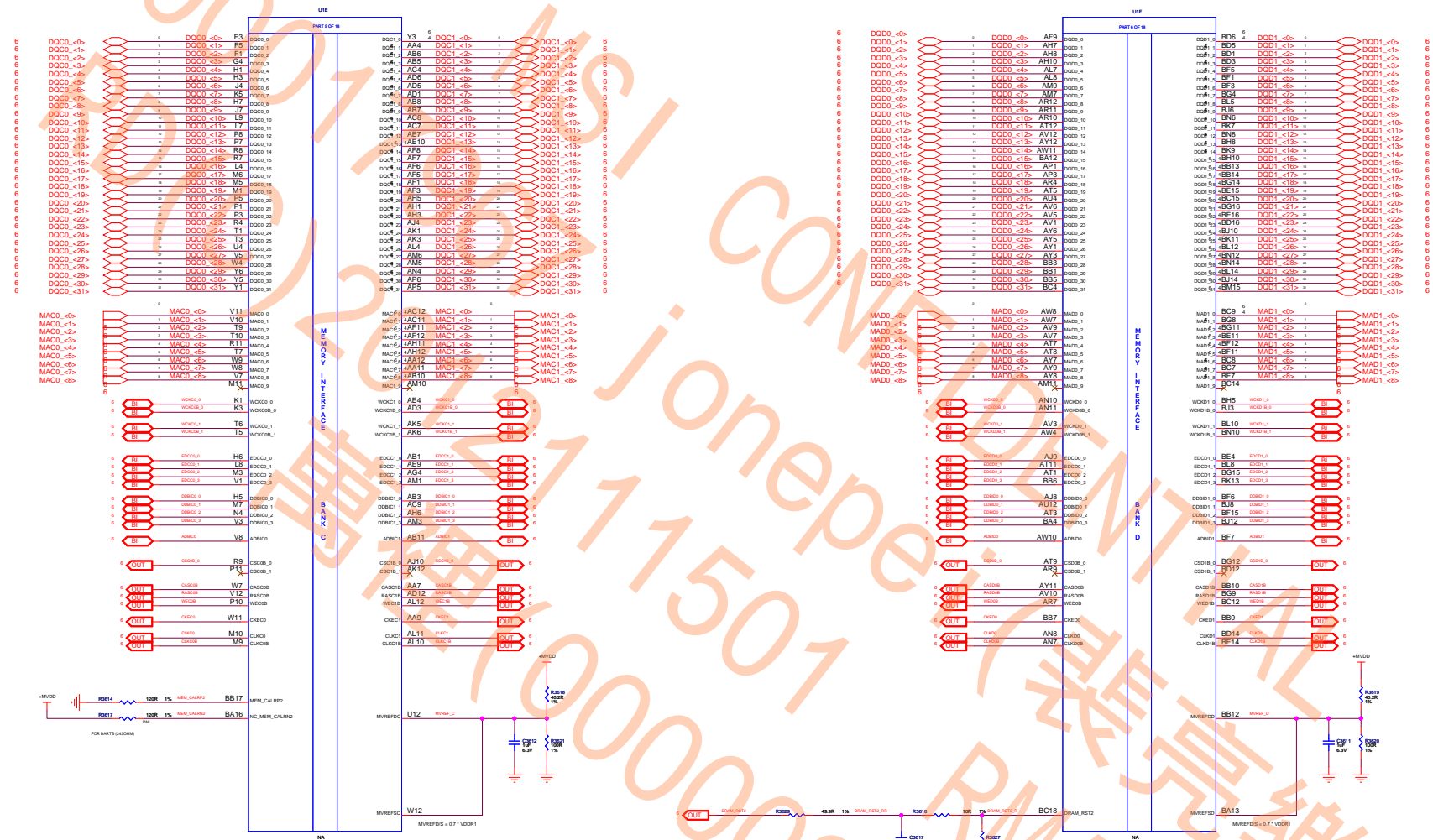
(2) PITCAIRN PCIE INTERFACE



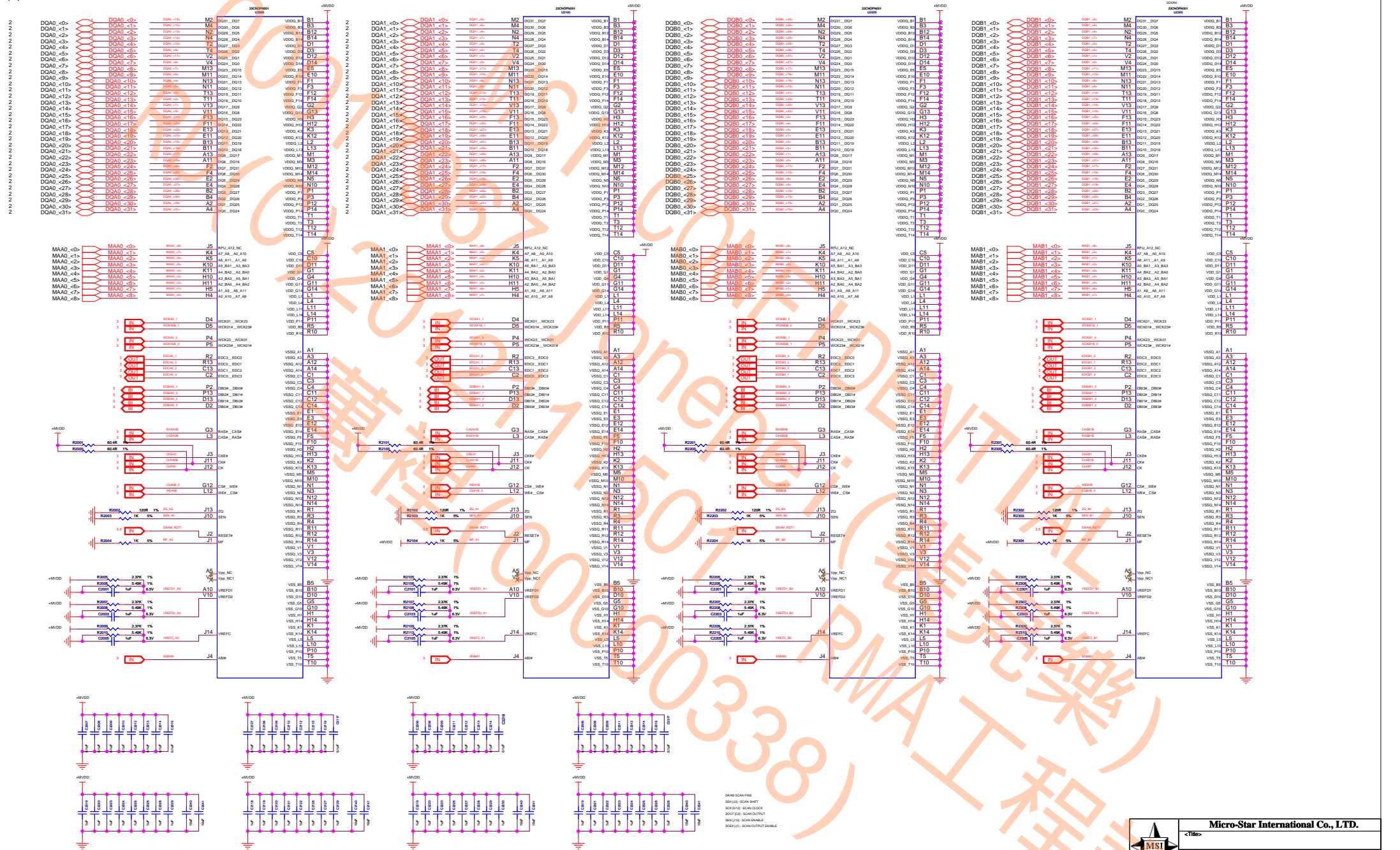
(3) PITCAIRN MEM INTERFACE CH A/B



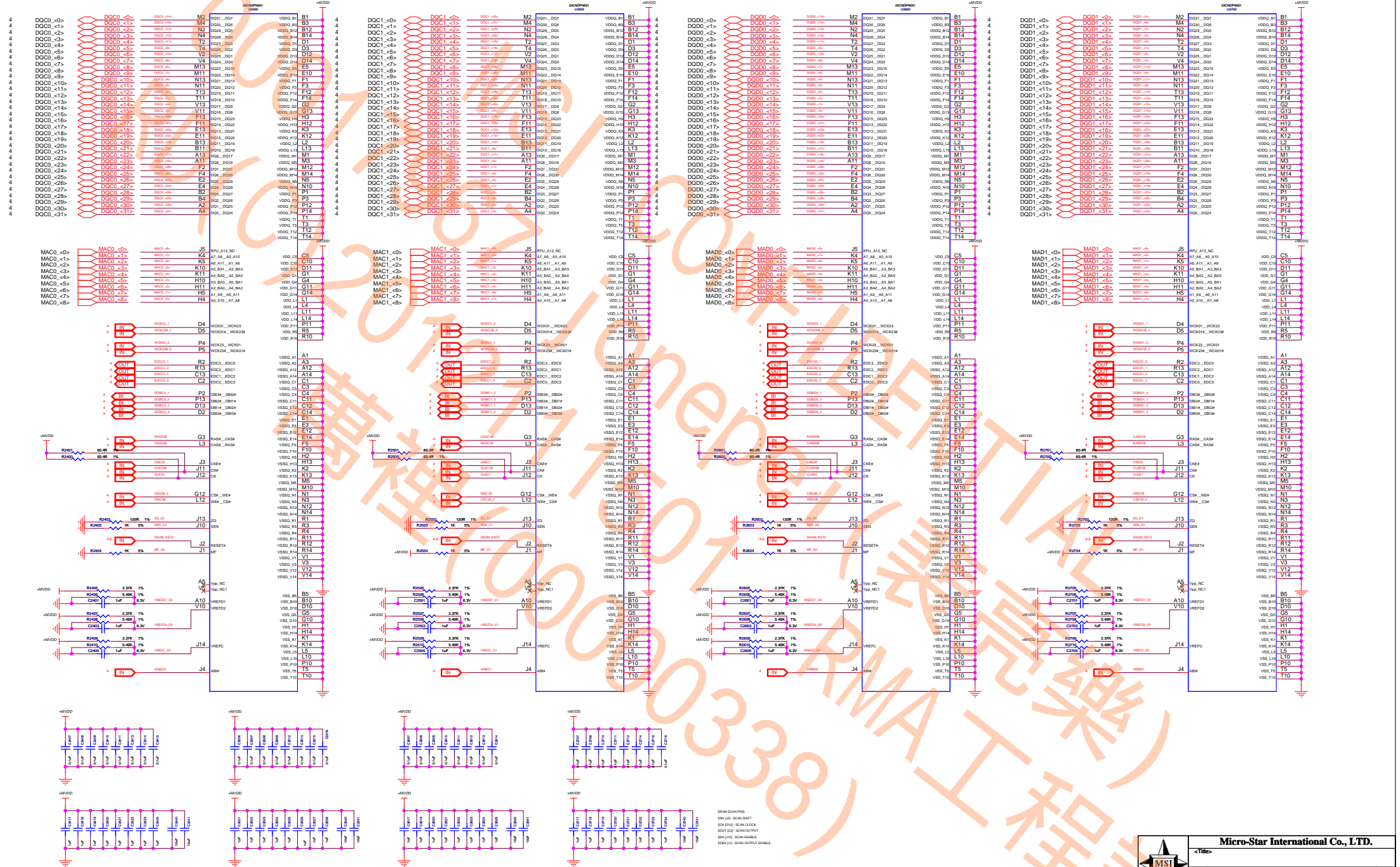
(4) PITCAIRN MEM INTERFACE CH C/D



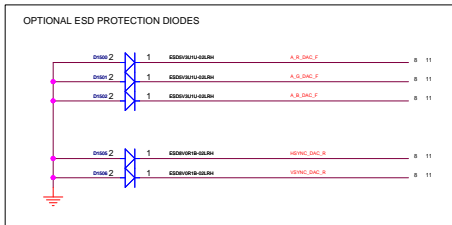
(5) GDDR5 MEMORY CH A/B



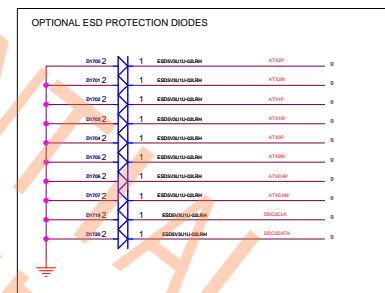
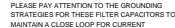
(6) GDDR5 MEMORY CH C/D

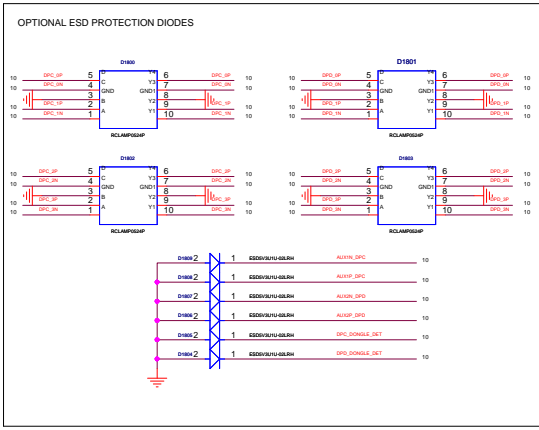
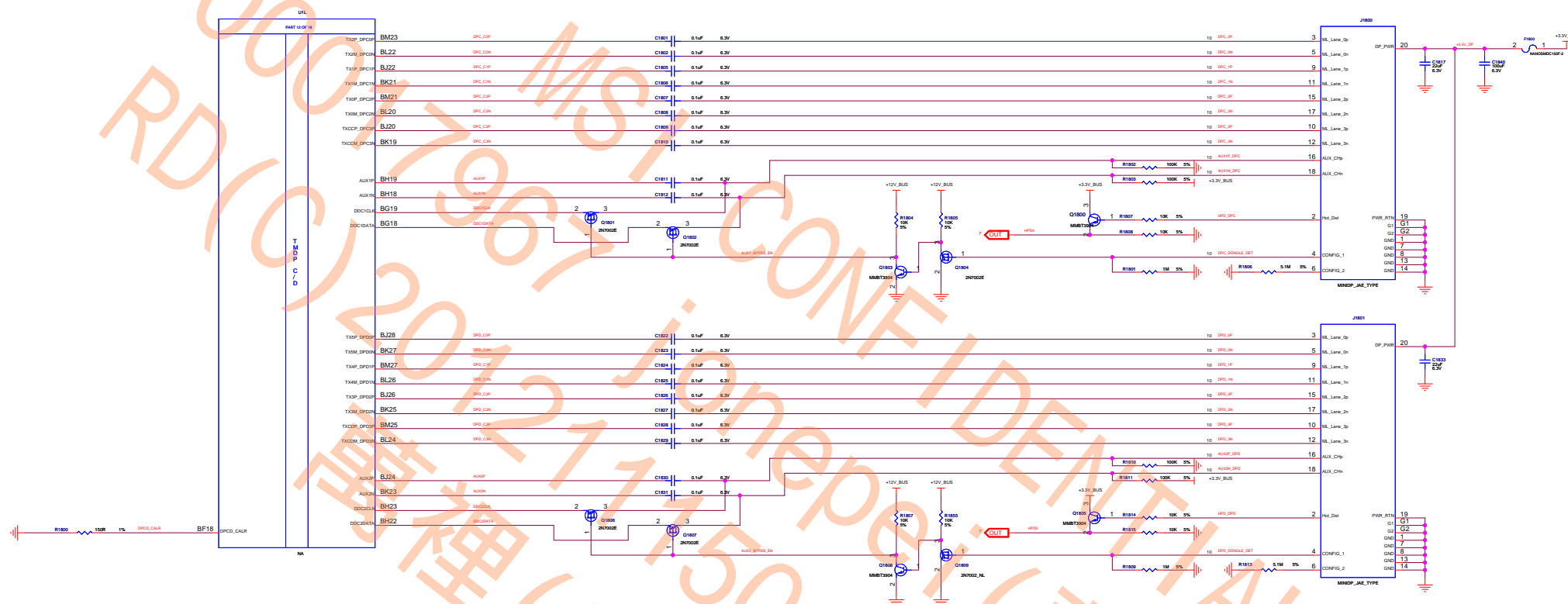


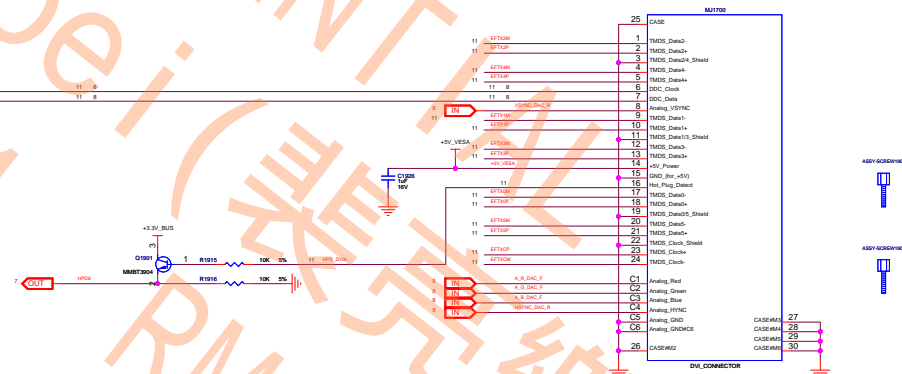
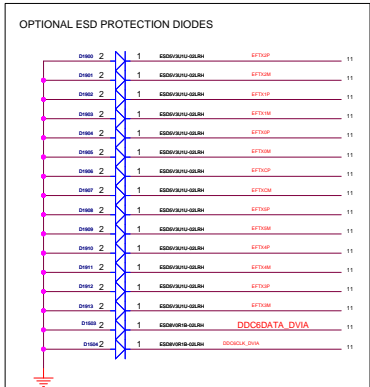
(8) PITCAIRN DAC1 LOCK



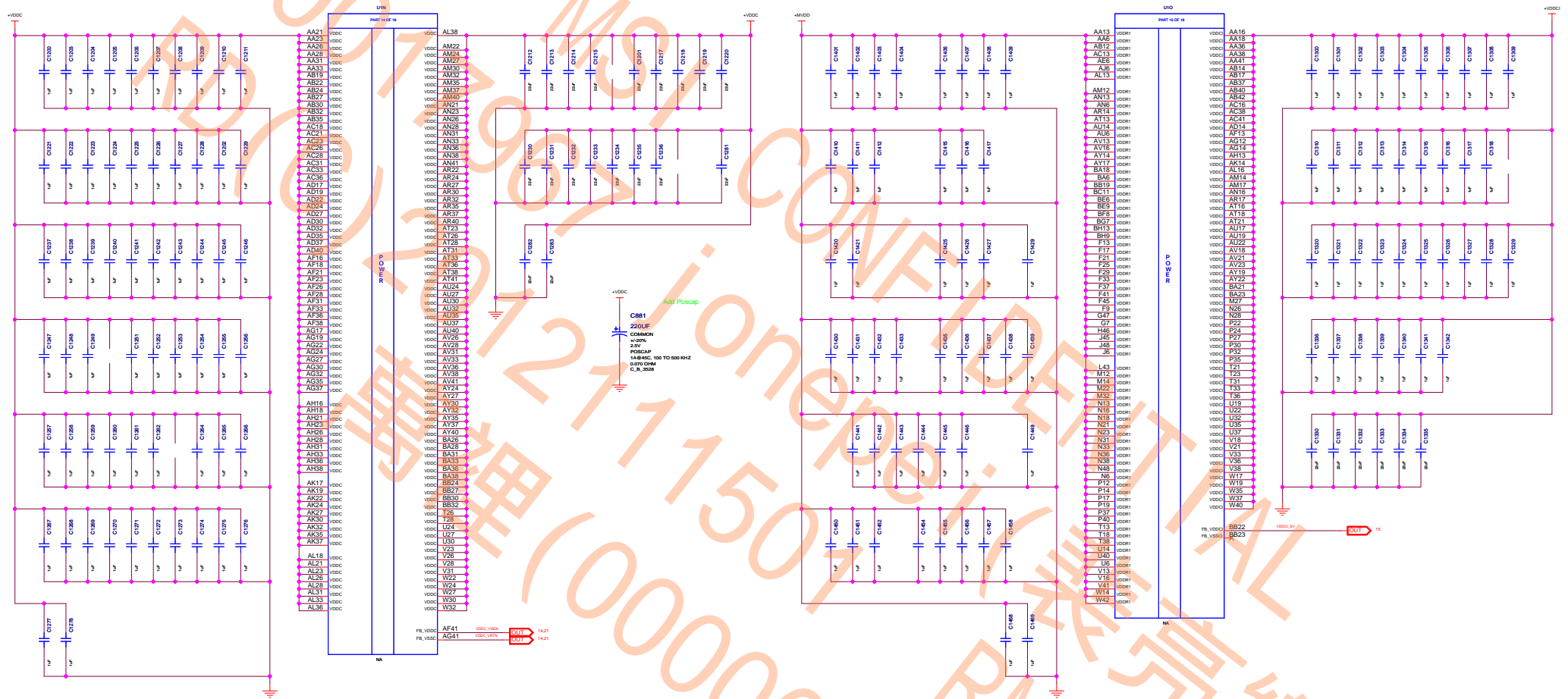
(9) PITCAIRN TMDP A/B

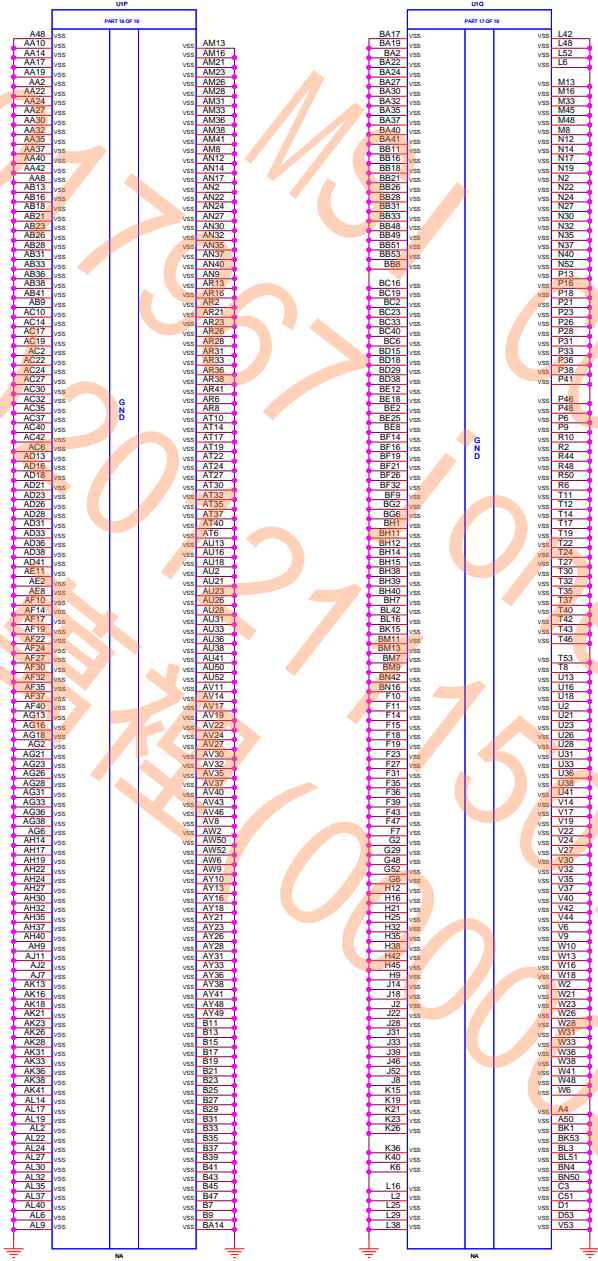




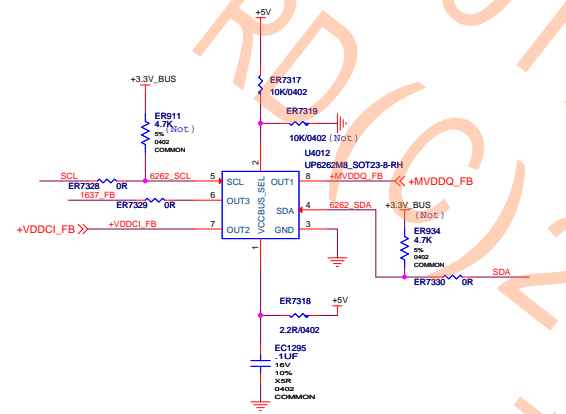


(12) PITCAIRN POWER

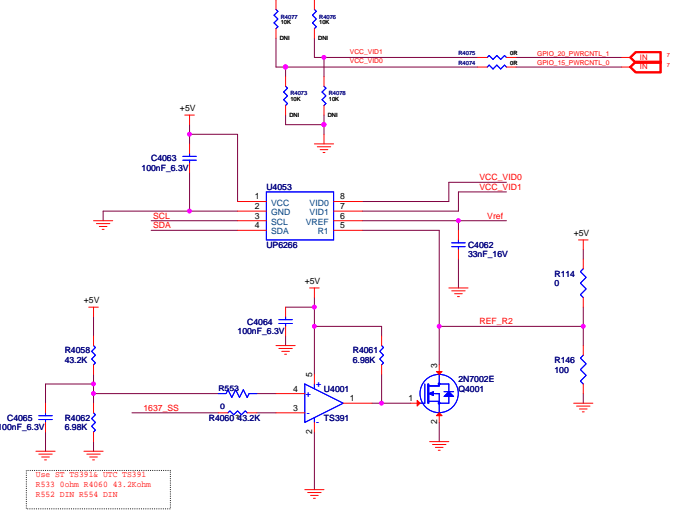




I2C VOLTAGE REFERENCE FOR VDDCI,MVDD

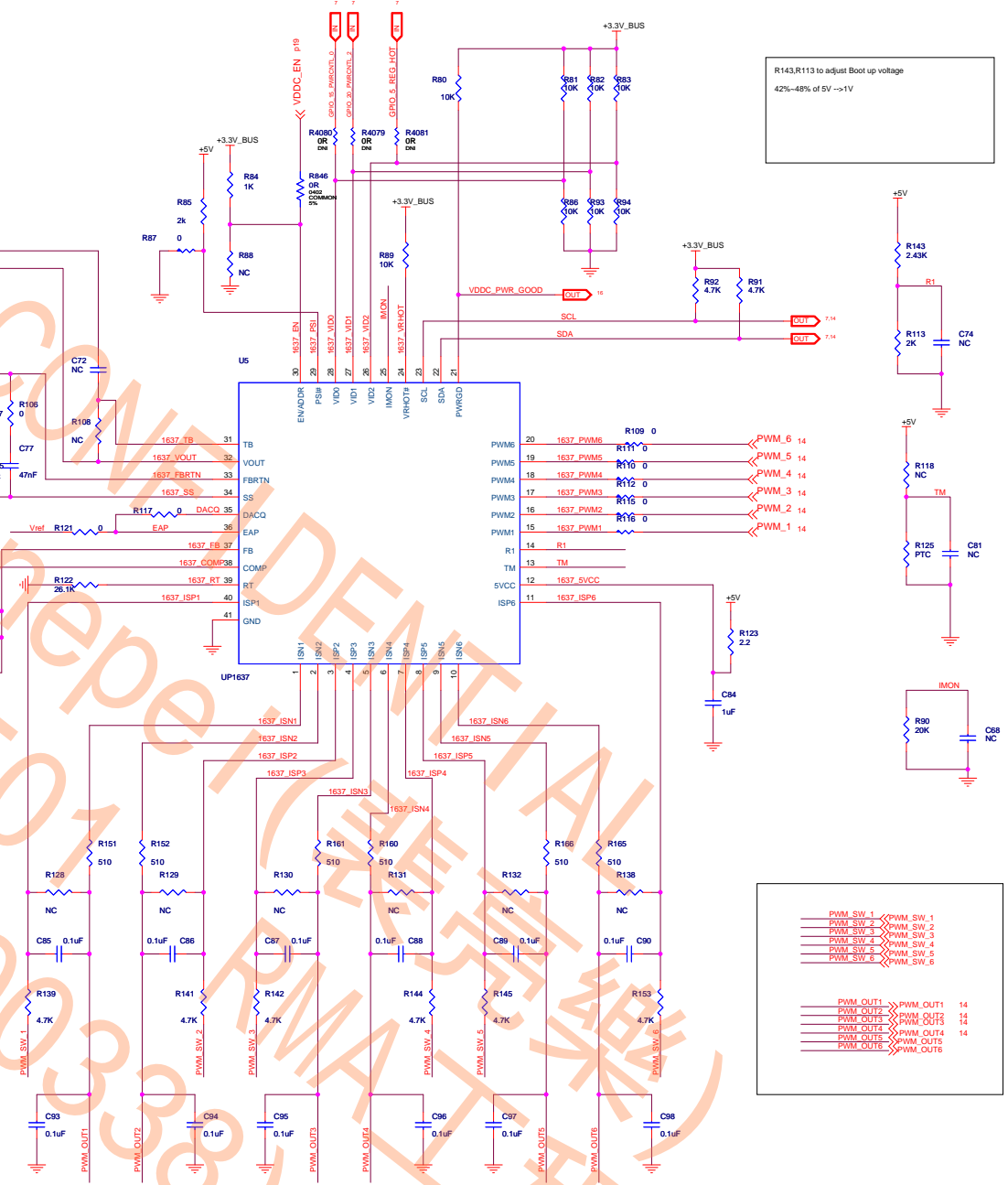


I2C VOLTAGE REFERENCE FOR VDDC



Use R1 R13914 00C 70391
R533 0ohm R4060 43.2Kohm
R552 02M R554 02M

R117 is for loadline setting



R143,R113 to adjust Boot up voltage
42%-48% of 5V ->1V

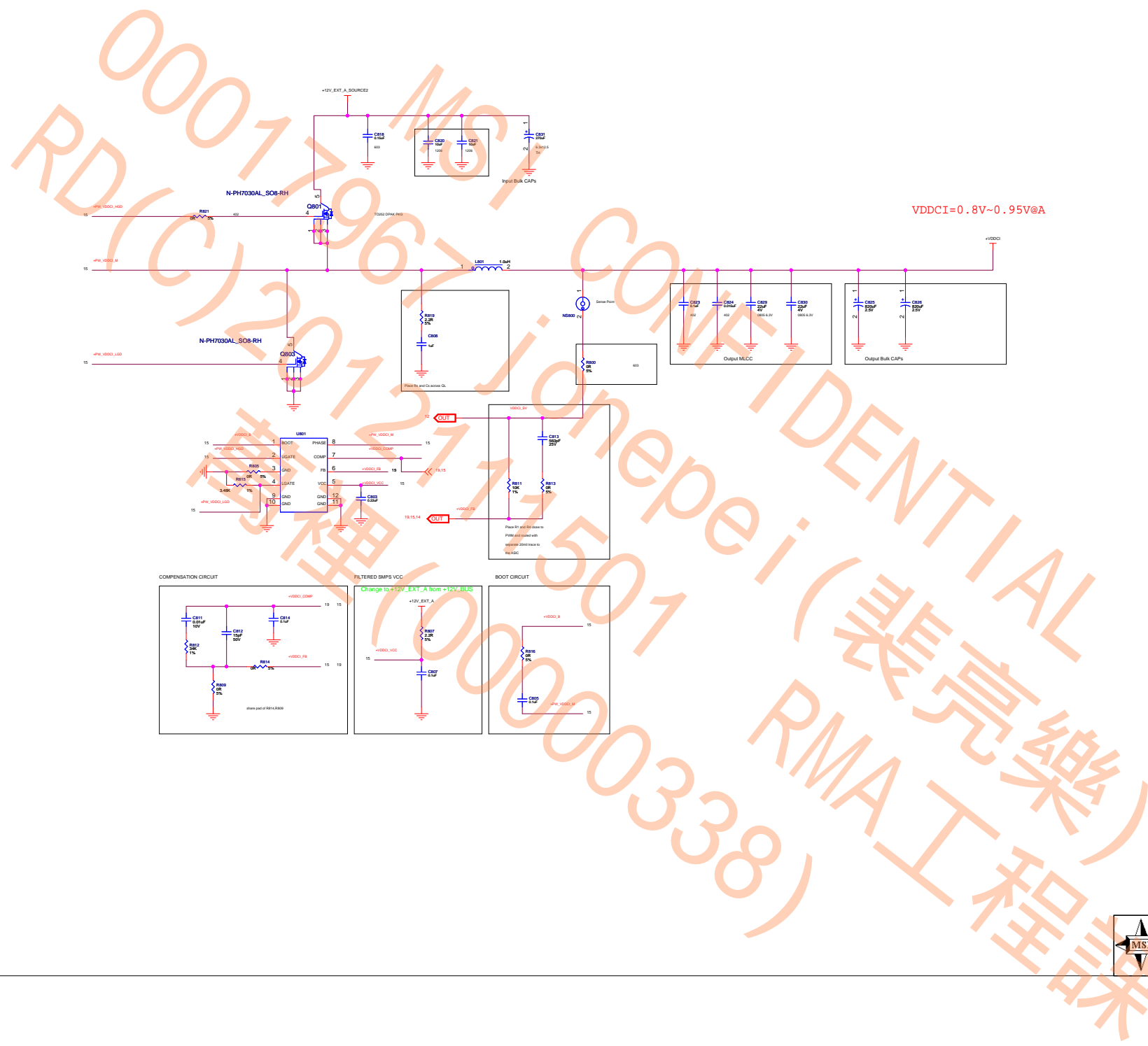
PWM_SW_1 <-> PWM_SW_1
PWM_SW_2 <-> PWM_SW_2
PWM_SW_3 <-> PWM_SW_3
PWM_SW_4 <-> PWM_SW_4
PWM_SW_5 <-> PWM_SW_5
PWM_SW_6 <-> PWM_SW_6

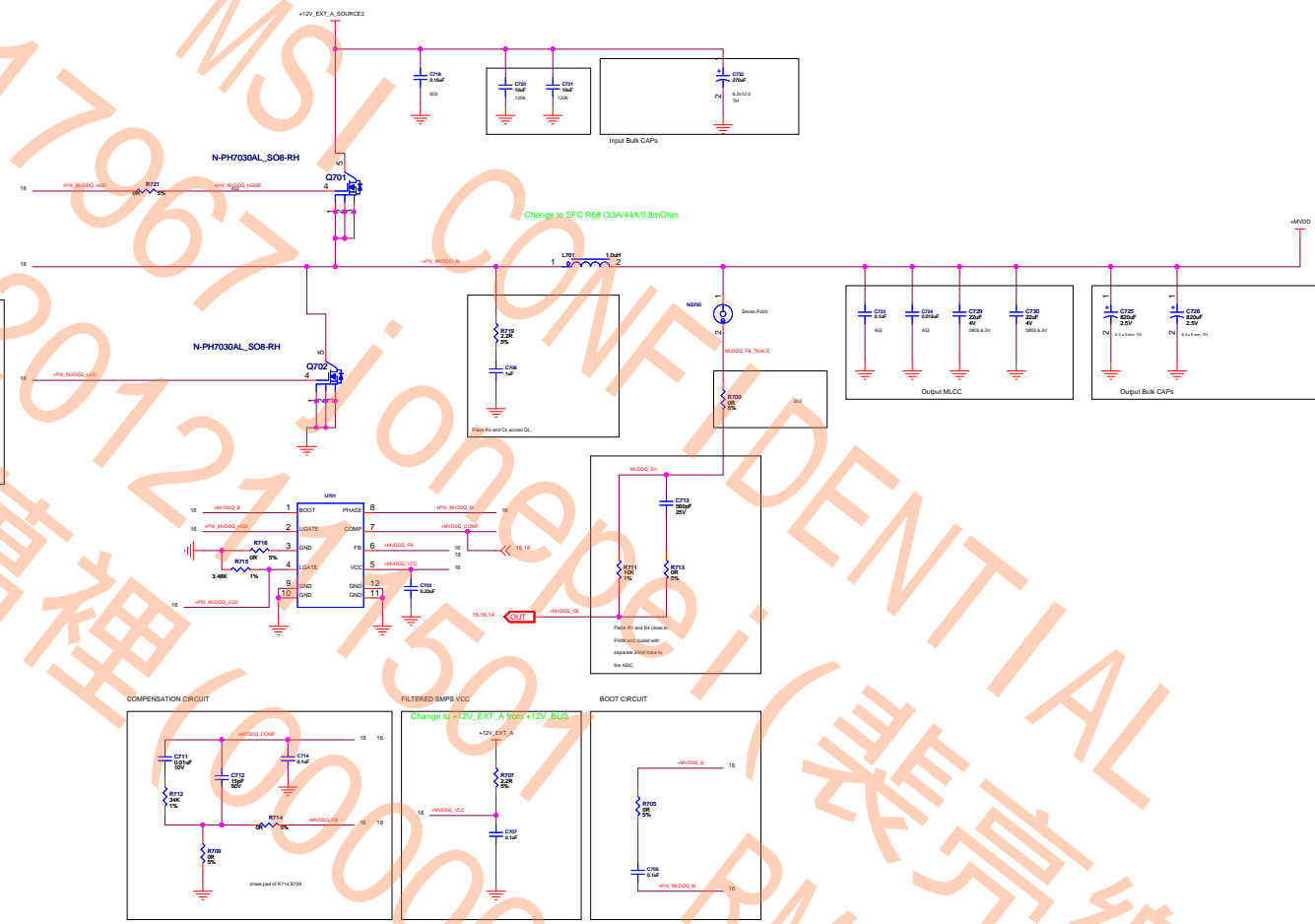
PWM_OUT1 <-> PWM_OUT1 14
PWM_OUT2 <-> PWM_OUT2 14
PWM_OUT3 <-> PWM_OUT3 14
PWM_OUT4 <-> PWM_OUT4 14
PWM_OUT5 <-> PWM_OUT5 14
PWM_OUT6 <-> PWM_OUT6 14



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Date:	Monday, March 05, 2012	Sheet 14 of 26

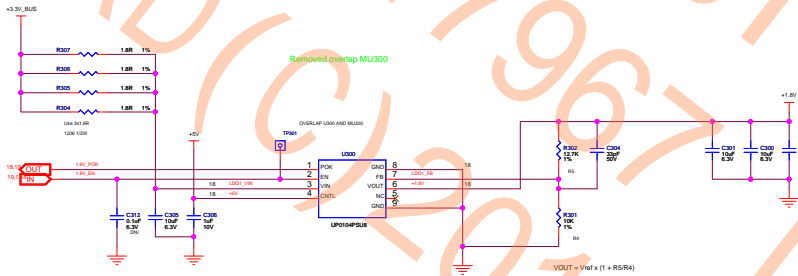






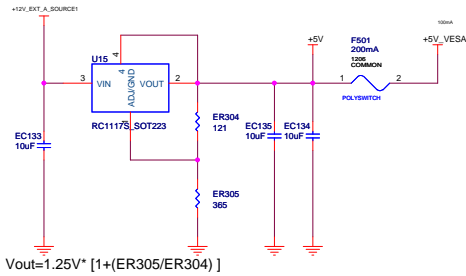
(18) SMALL RAIL REGULATORS

LDO #1: VIN = 3.0V TO 3.6V MAX VOUT = +1.8V +/- 2% IOUT = 1.3A RMS MAX
PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING

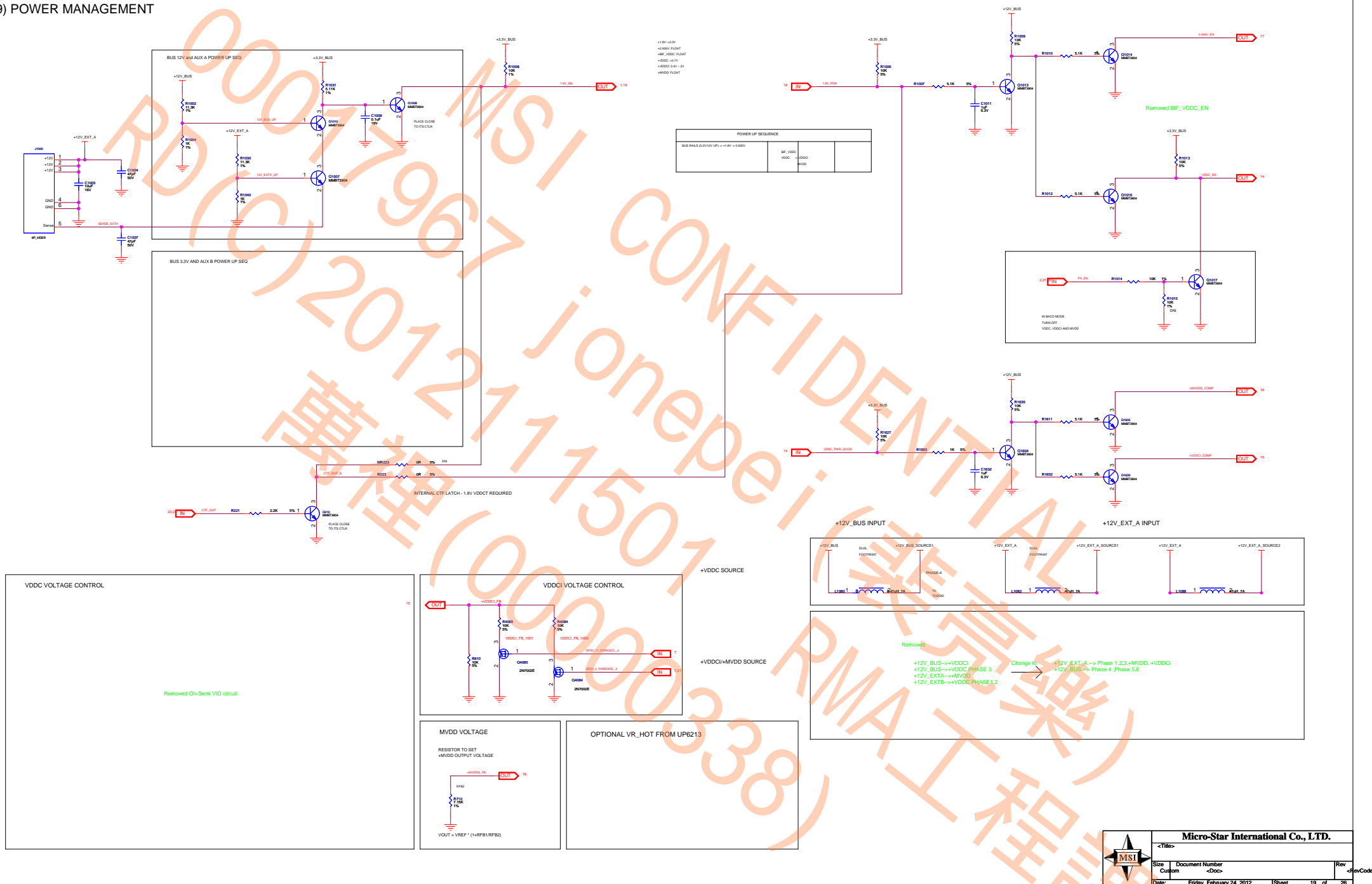


BIF_VDDC VOUT = TBD +/- 2% IOUT = TBD

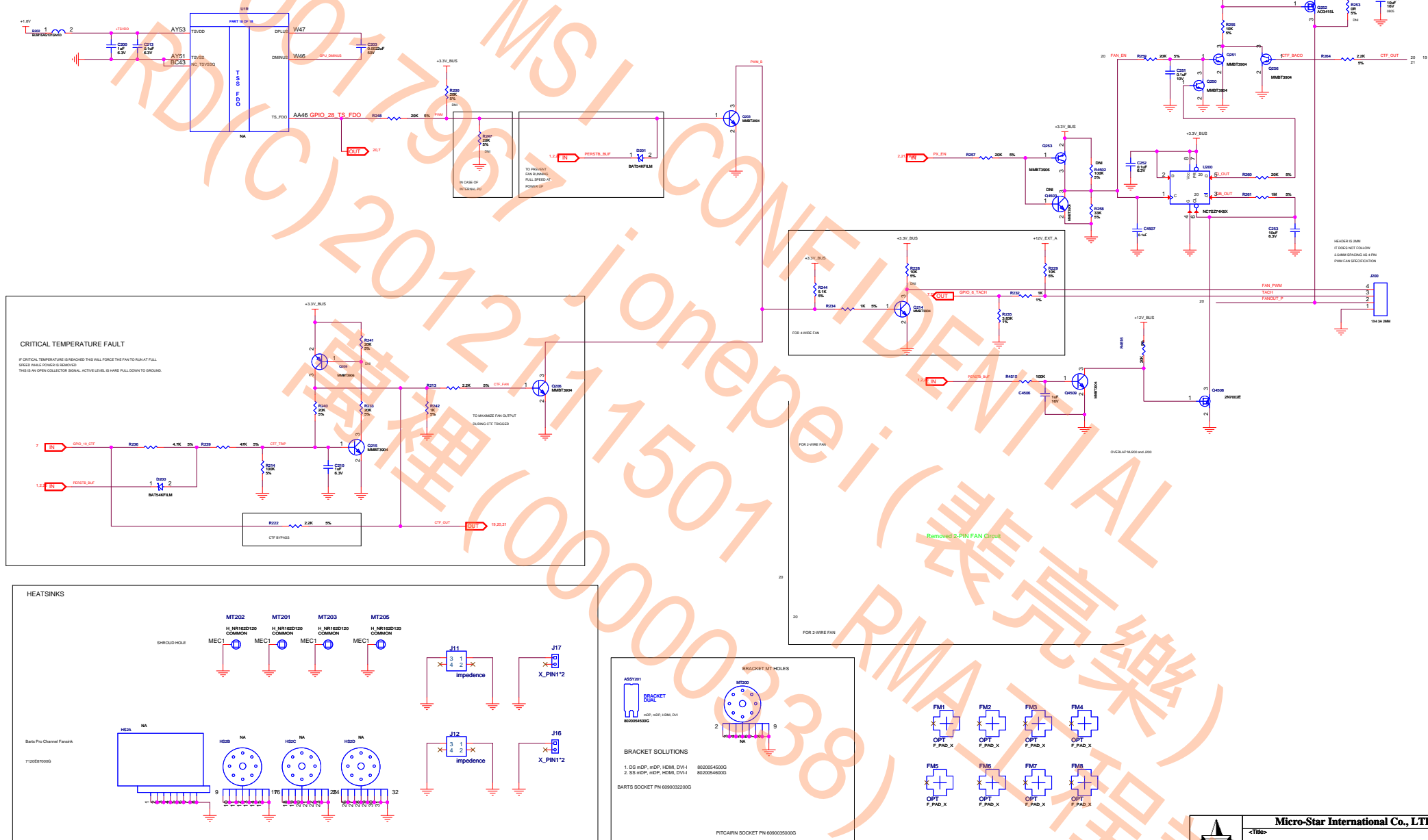
REGULATOR FOR +5V RAILS
IOUT MAX = 150mA

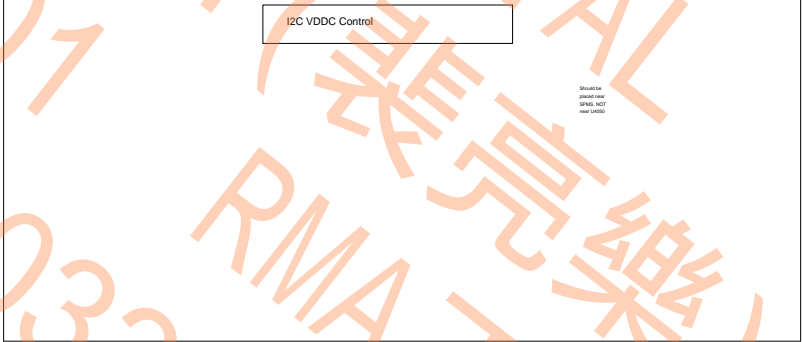
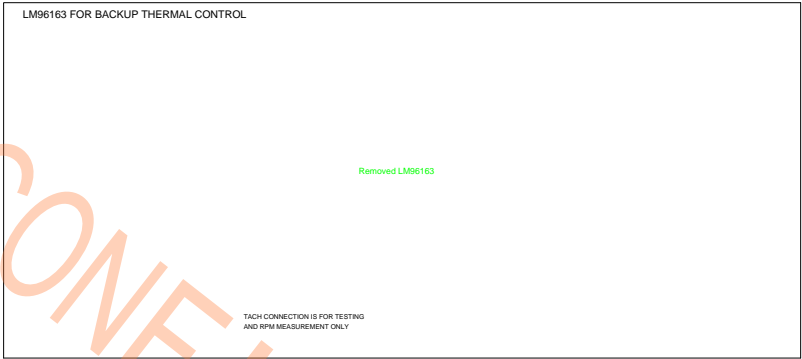
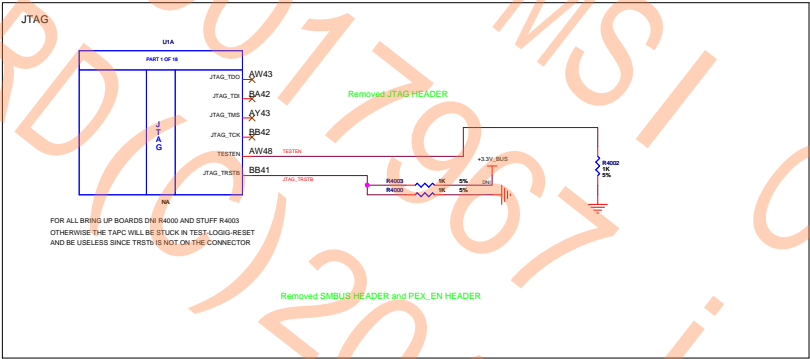


(19) POWER MANAGEMENT

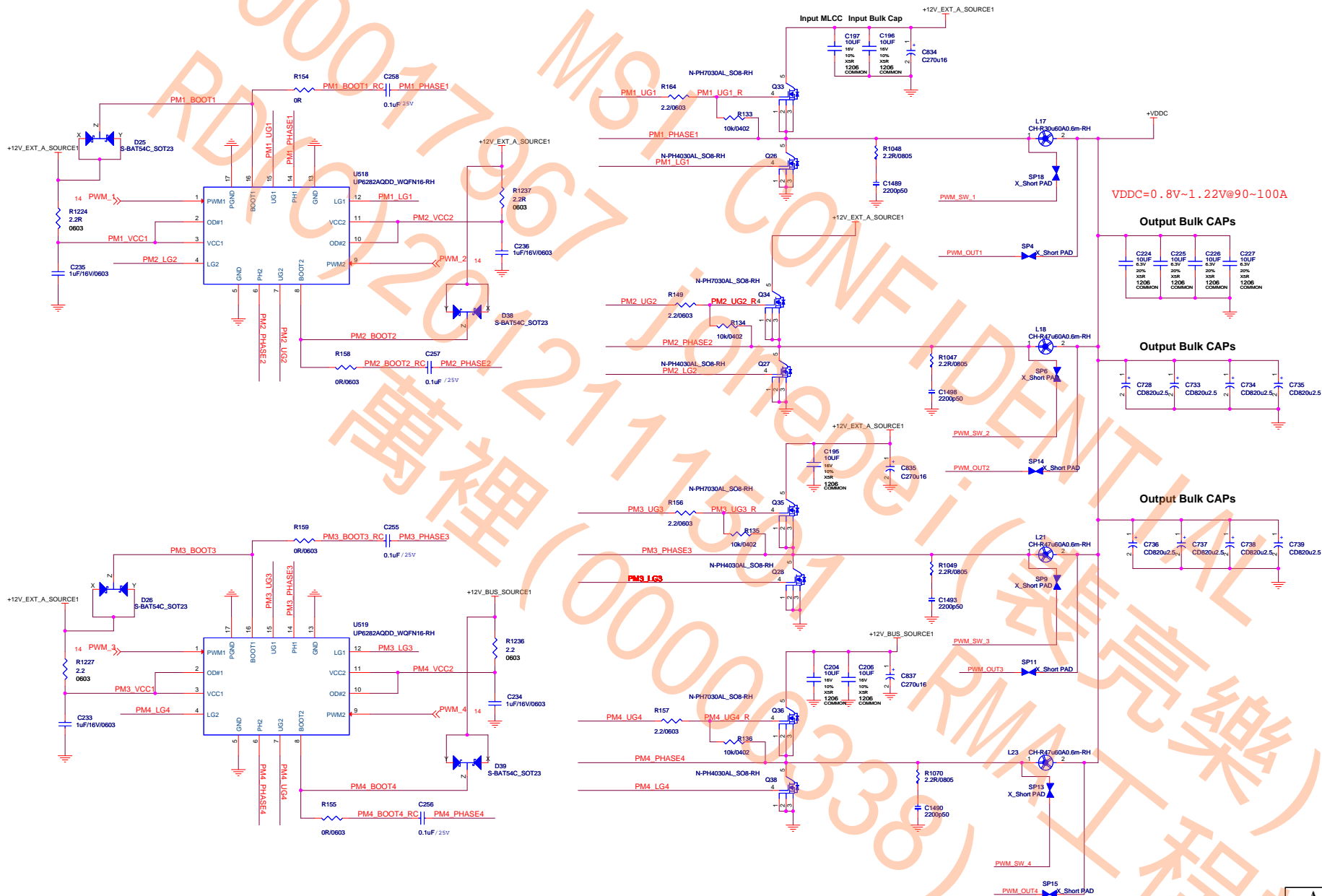


(20) MECHANICAL AND THERMAL MANAGEMENT





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AMD				TITLE:		TITLE		DOCUMENT NUMBER: 105-CXX000-00A		DATE: Tue Dec 13 20:26:17 2011		SHEET NUMBER: 23 OF 23		REV: 1.0	
REVISION HISTORY						ENGINEER: XXXX		NOTES: NOTE		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding this schematic and design, including, not limited to, any implied warranty of non-infringement or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of this information included herein.		C 3916 Advanced Micro Devices		AMD - GRAPHICS 1 COMMERCE VALLEY MARKHAM, ONTARIO, L3T 7X6	
SCH Rev		PCB Rev		Date		REVISION DESCRIPTION									
0		00A		20110104		POTCAREN PRO CA DESIGN									
1		00B		20110105		Update Board delay circuitry for 3 pin fan									



PWM_SW_1 < PWM_SW_1
 PWM_SW_2 < PWM_SW_2
 PWM_SW_3 < PWM_SW_3
 PWM_SW_4 < PWM_SW_4
 PWM_OUT1 < PWM_OUT1
 PWM_OUT2 < PWM_OUT2
 PWM_OUT3 < PWM_OUT3
 PWM_OUT4 < PWM_OUT4

