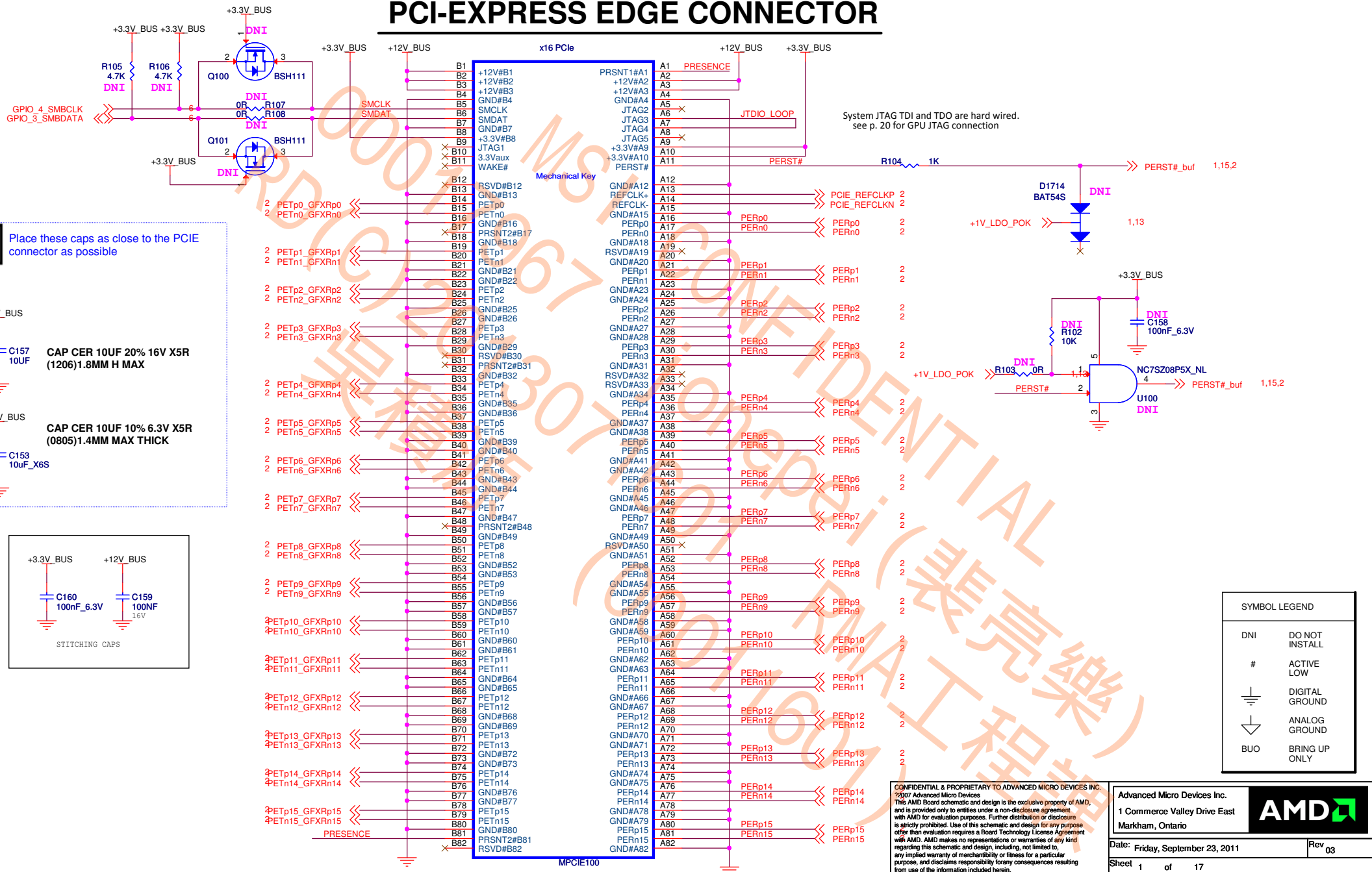
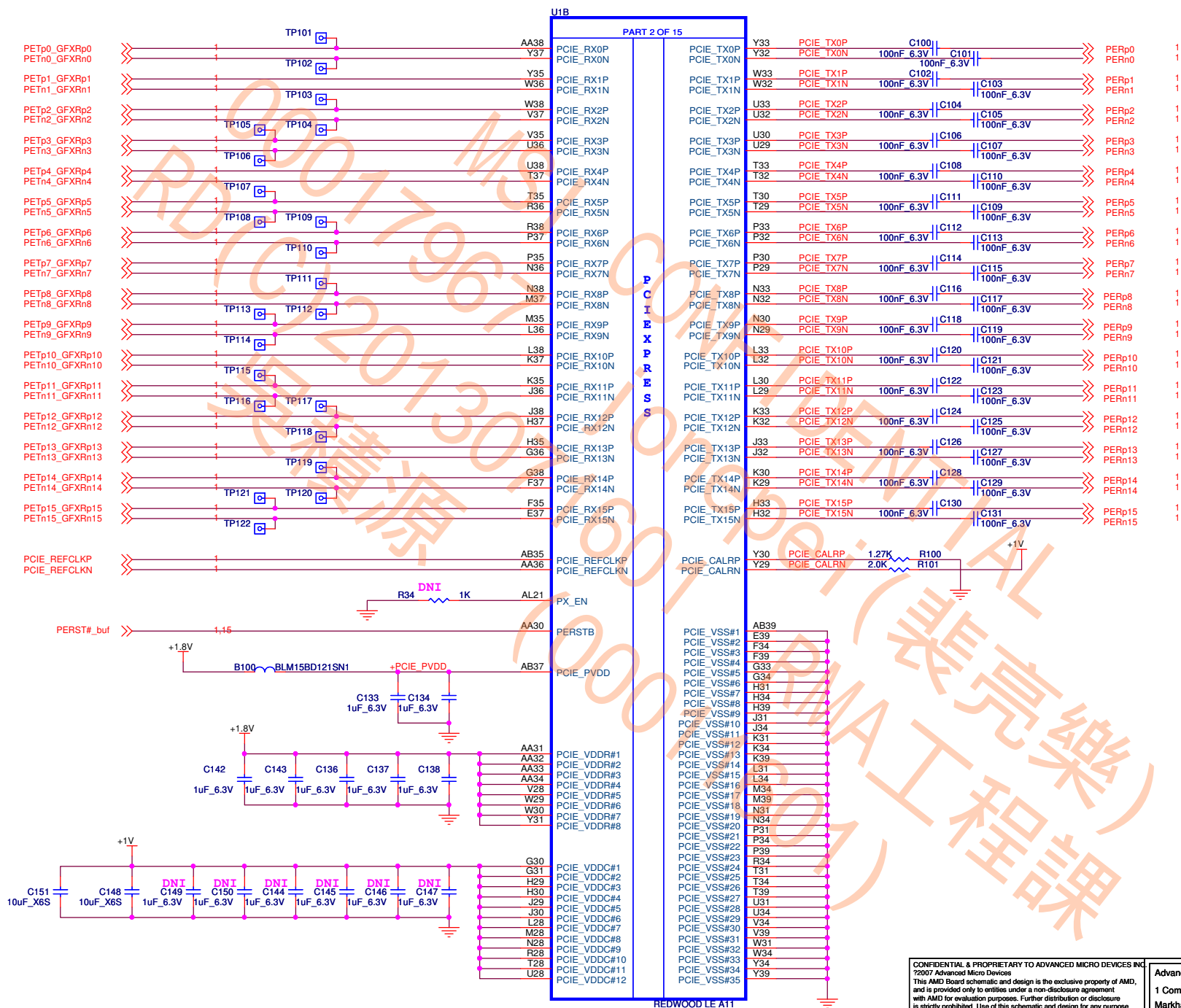
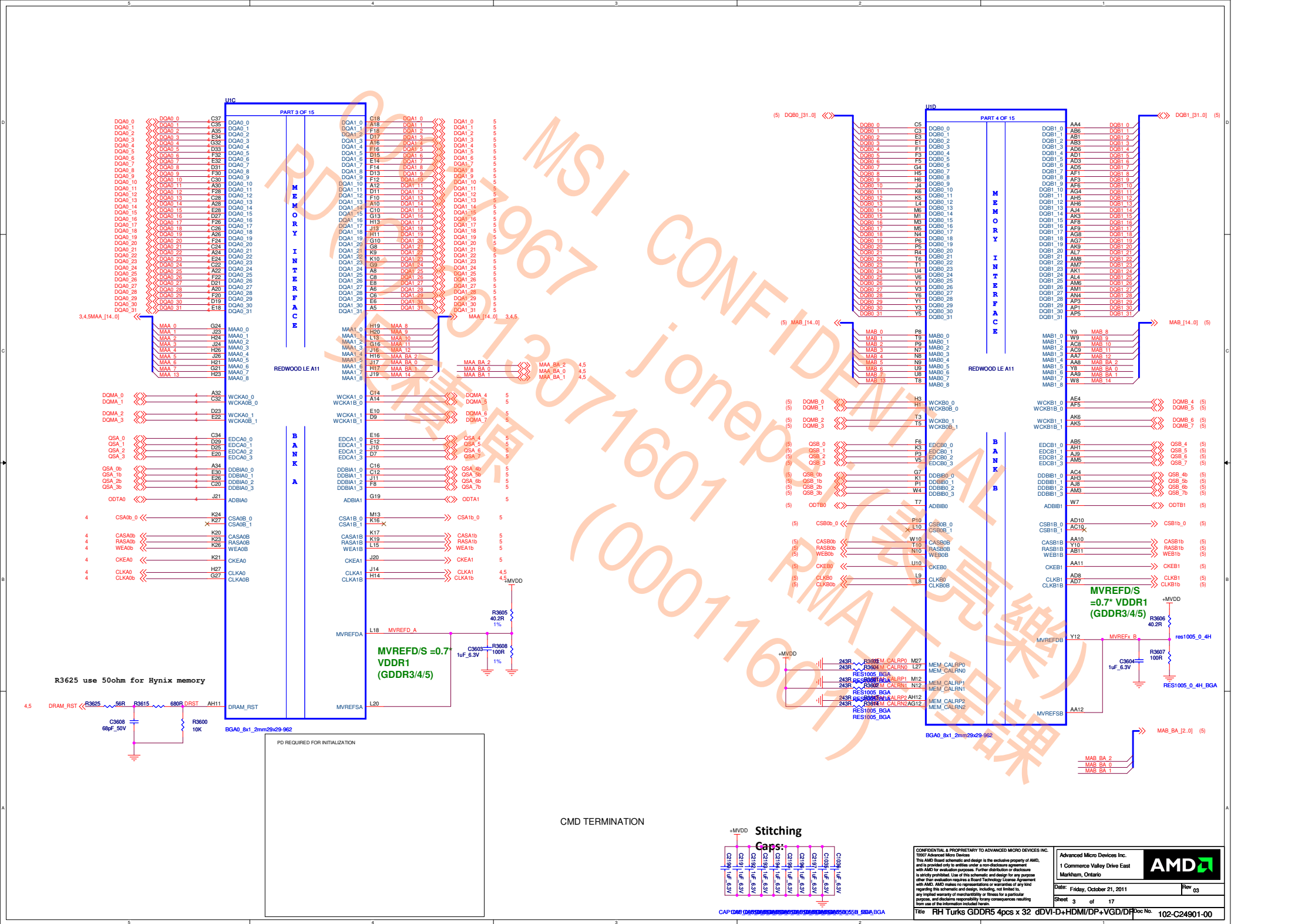


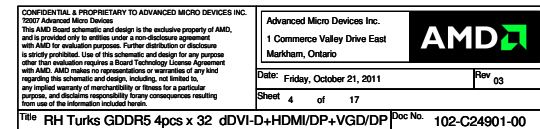
PCI-EXPRESS EDGE CONNECTOR



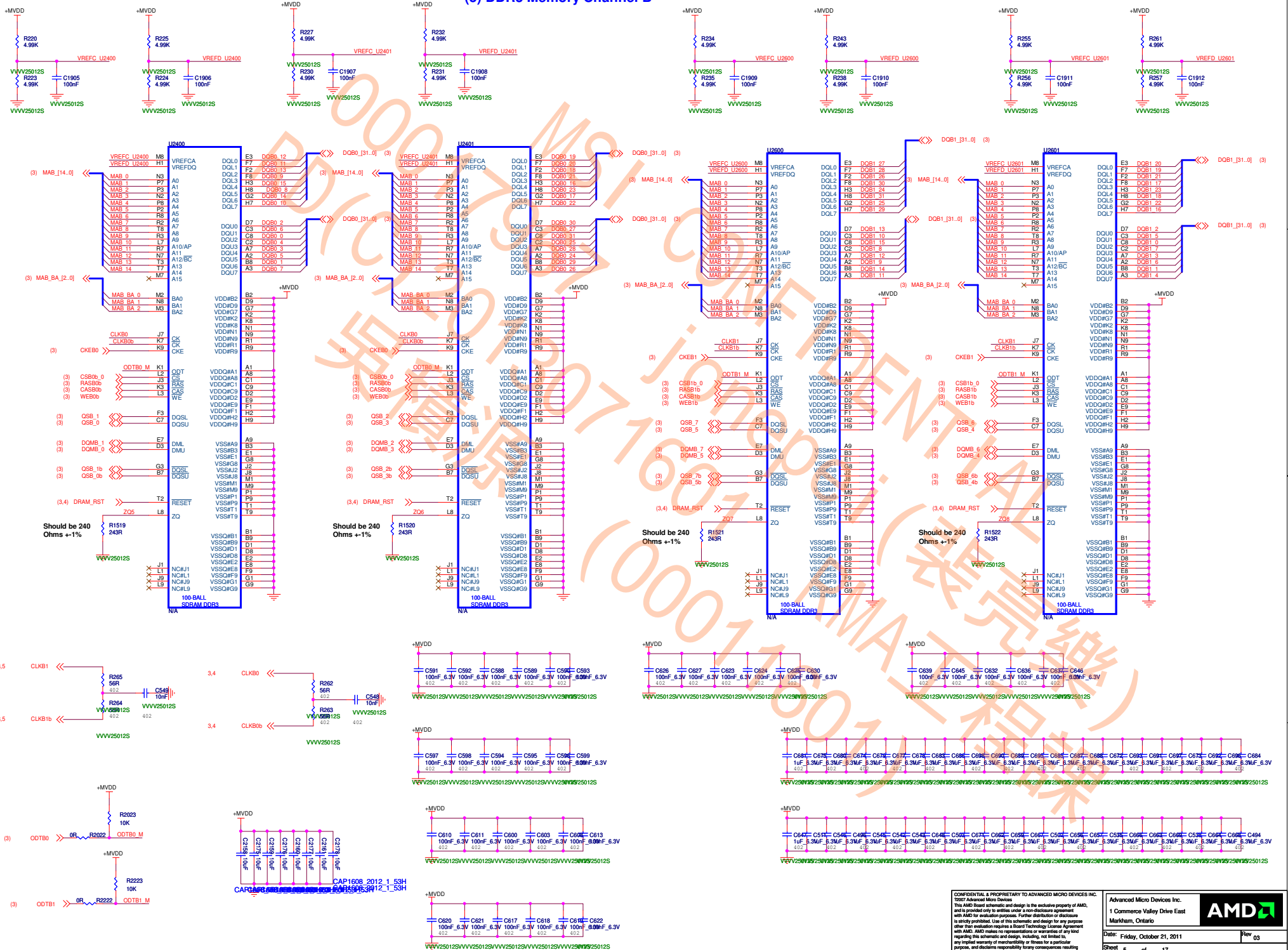


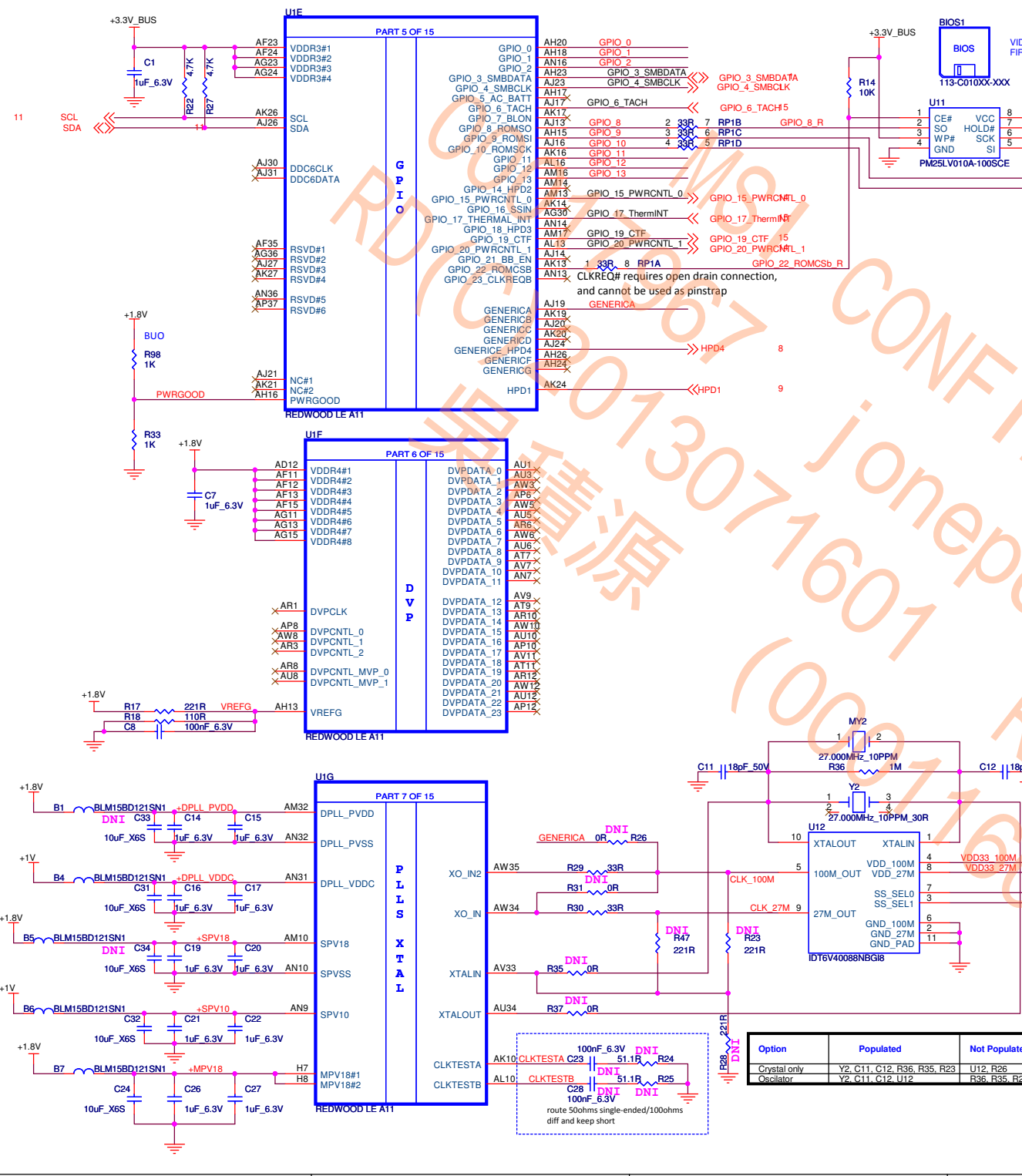


MAX DENSITY: 128Mx16



(5) DDR3 Memory Channel B





PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0: Default. (Driver Controlled Gen2)
1: Strap Controlled Gen2

GPIO(13,12,11) - CONFIG[2:0]
100 - 512Kbit M25P05A (ST)
101 - 1Mbit M25P10A (ST)
101 - 2Mbit M25P40 (ST)
101 - 8Mbit M25P80 (ST)
100 - 512Kbit Pm25LV512 (Chingis)
101 - 1Mbit Pm25LV010 (Chingis)

VIP_DEVICE_STRAP_DIS
0: VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

RESERVED:
Internal use only. Other logic must not affect these signals during RESET.

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

Don't set GENERICC high at reset

Option	Populated	Not Populated
Crystal only	Y2, C11, C12, R36, R35, R23	U12, R26
Oscillator	Y2, C11, C12, U12	R36, R35, R23, R26

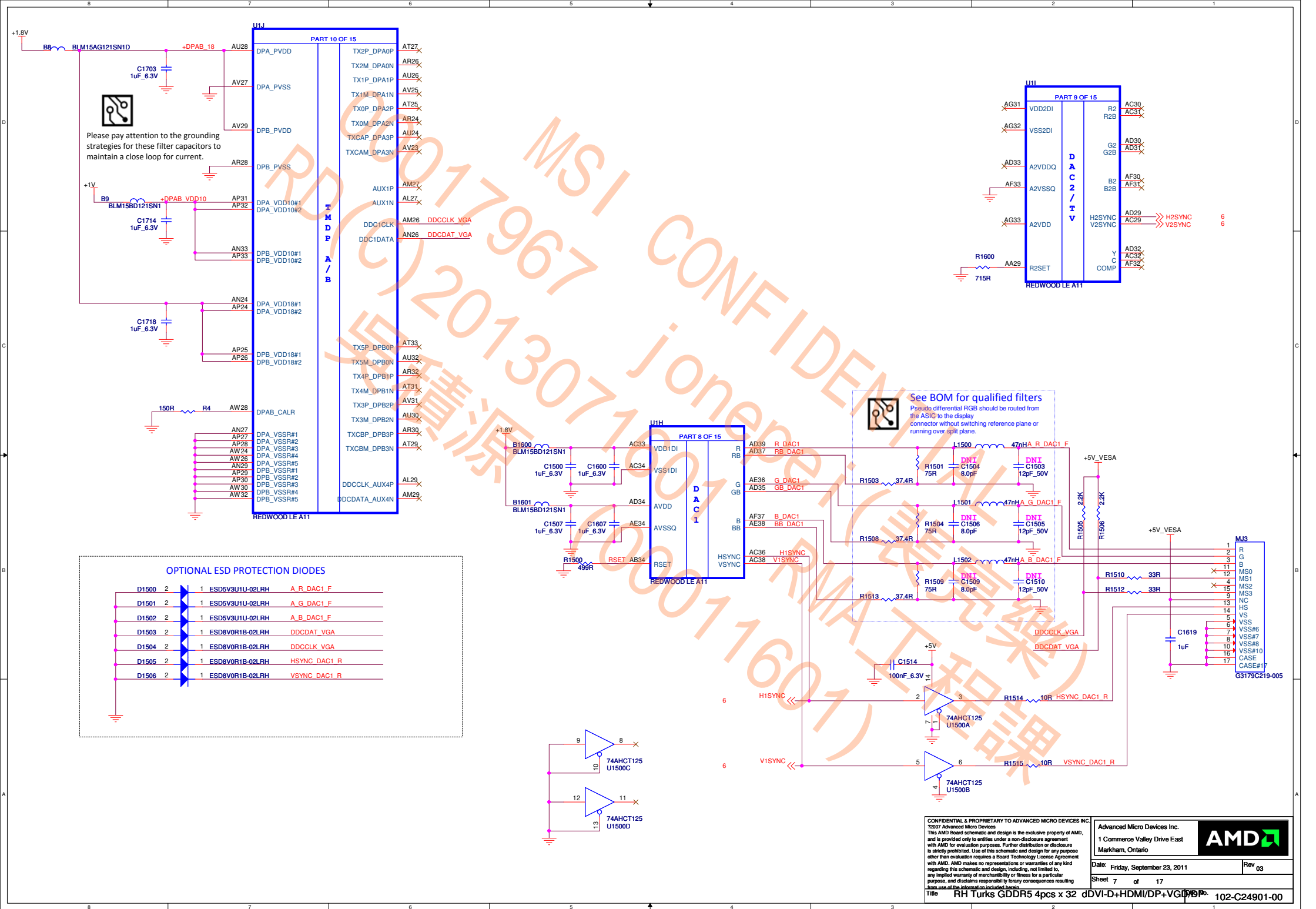
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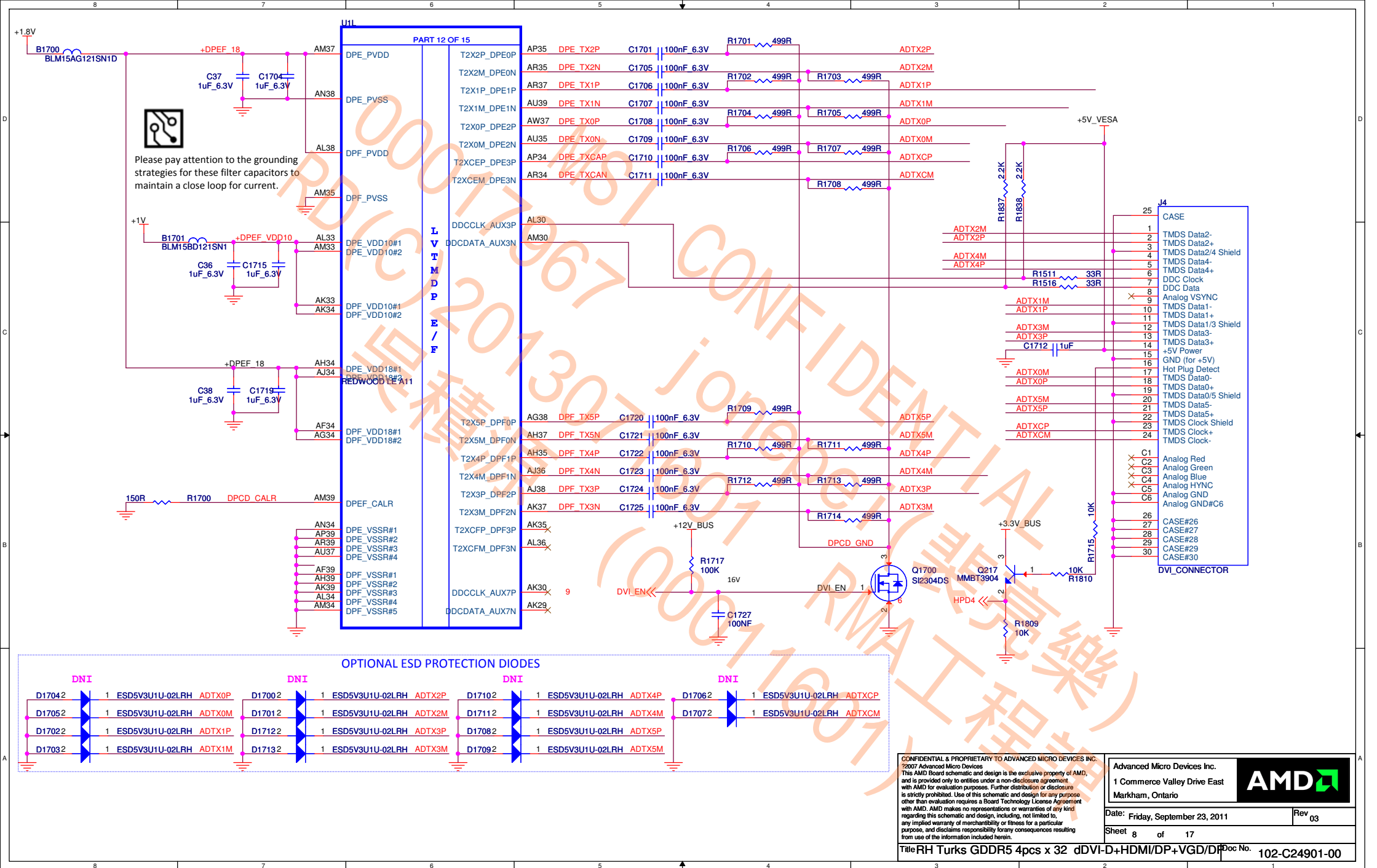
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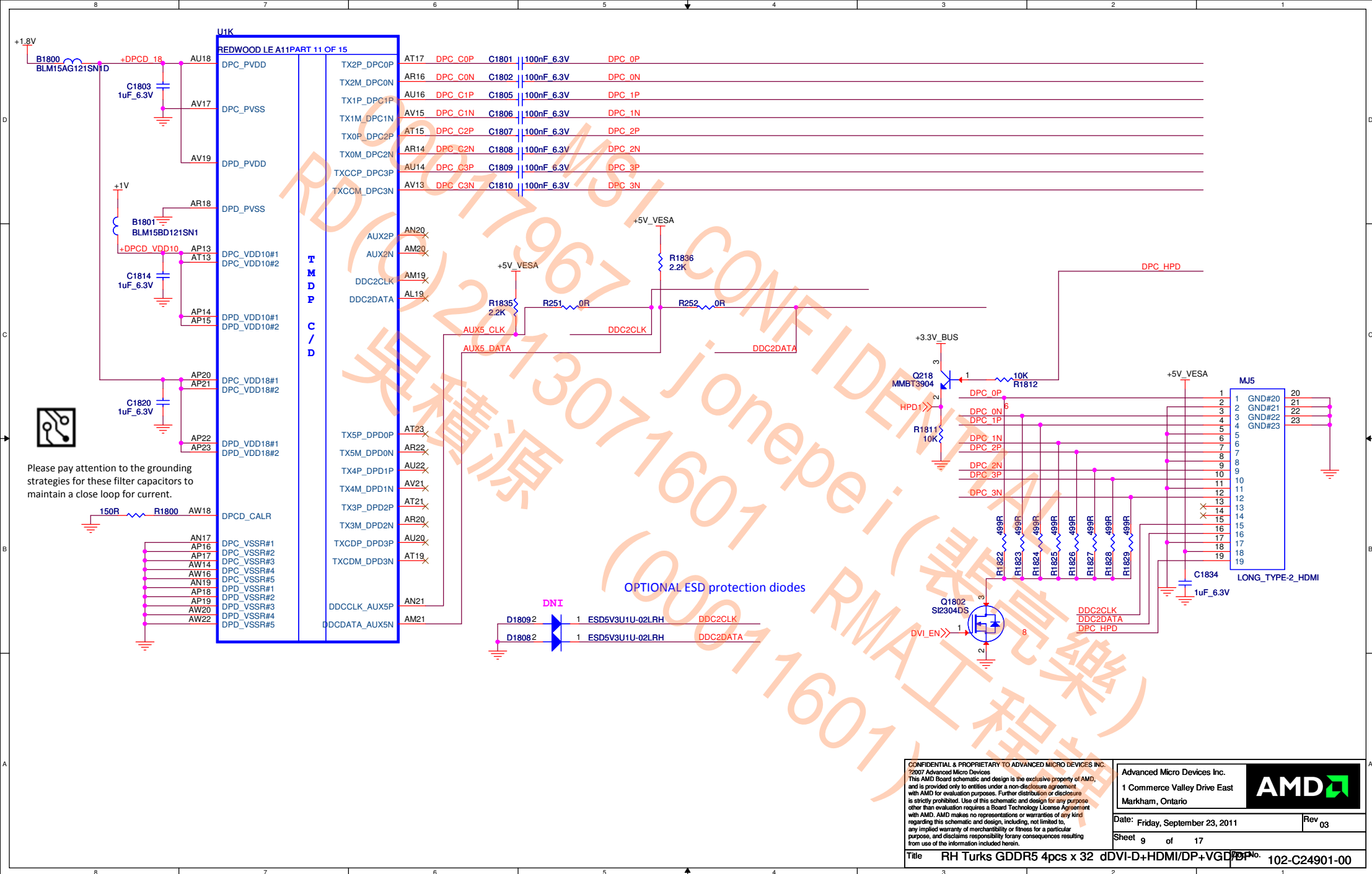
Date: Friday, September 23, 2011
Rev 03

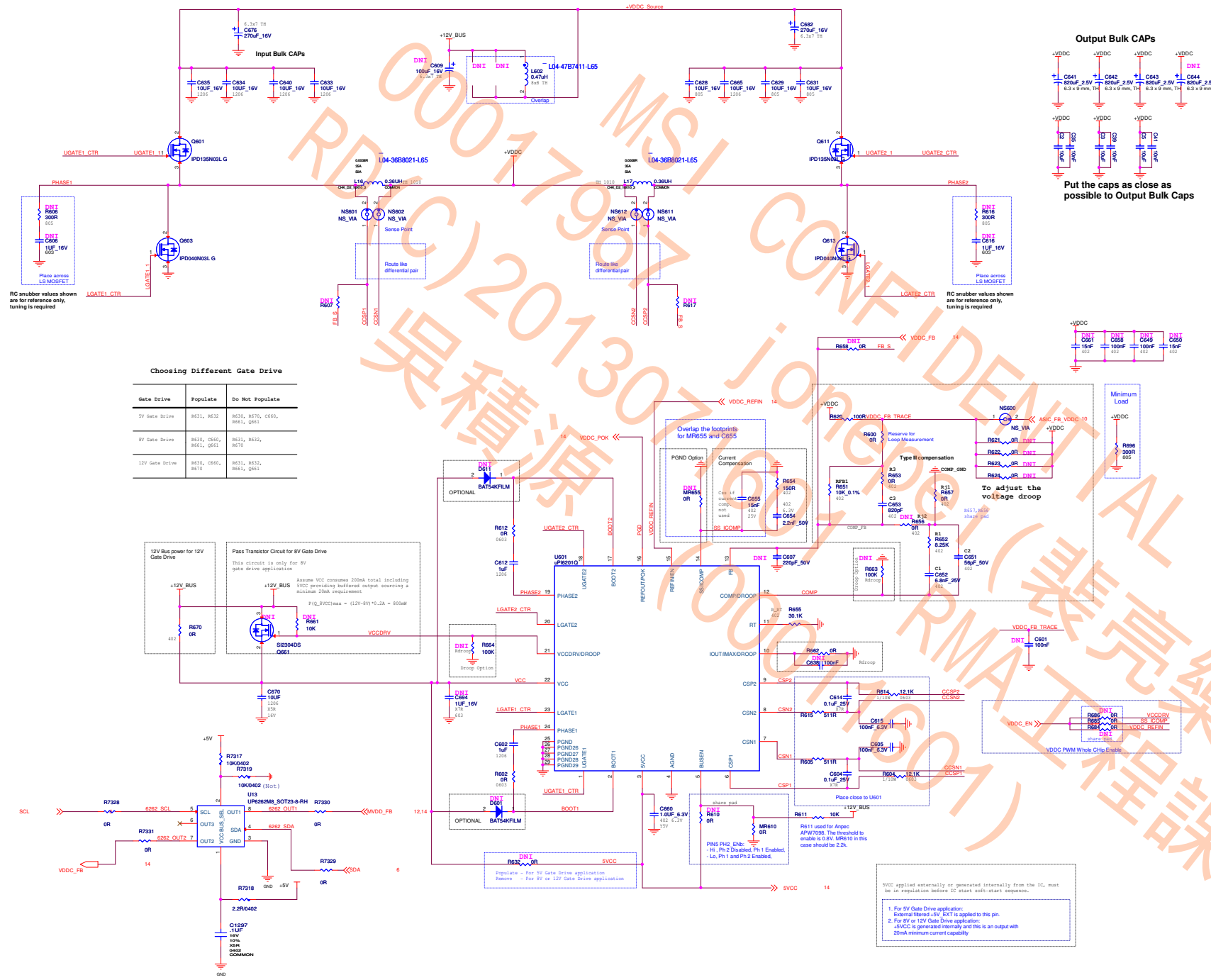
Sheet 6 of 17

Title RH Turks GDDR5 4pcs x 32 dDVI-D+HDMI/DP+VGD/DP Doc No 102-G24901-00



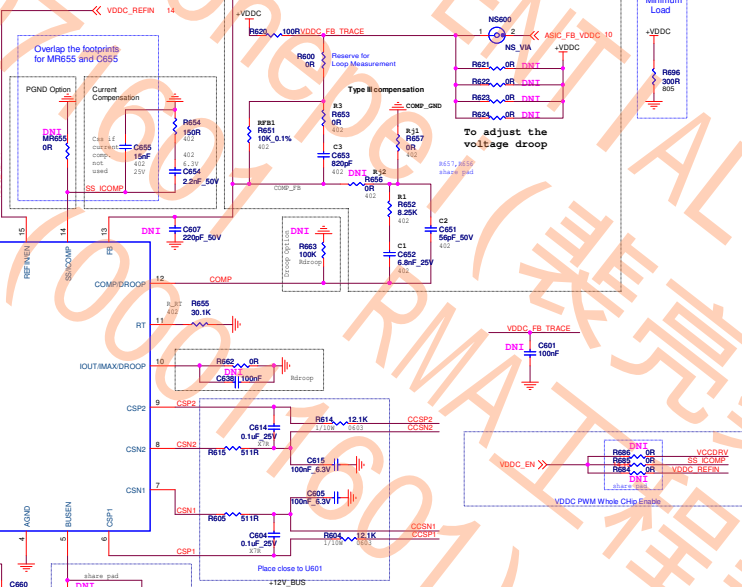
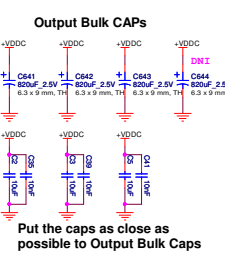
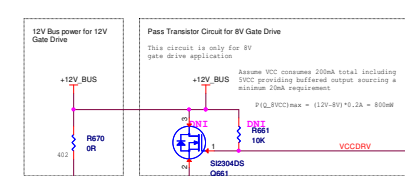






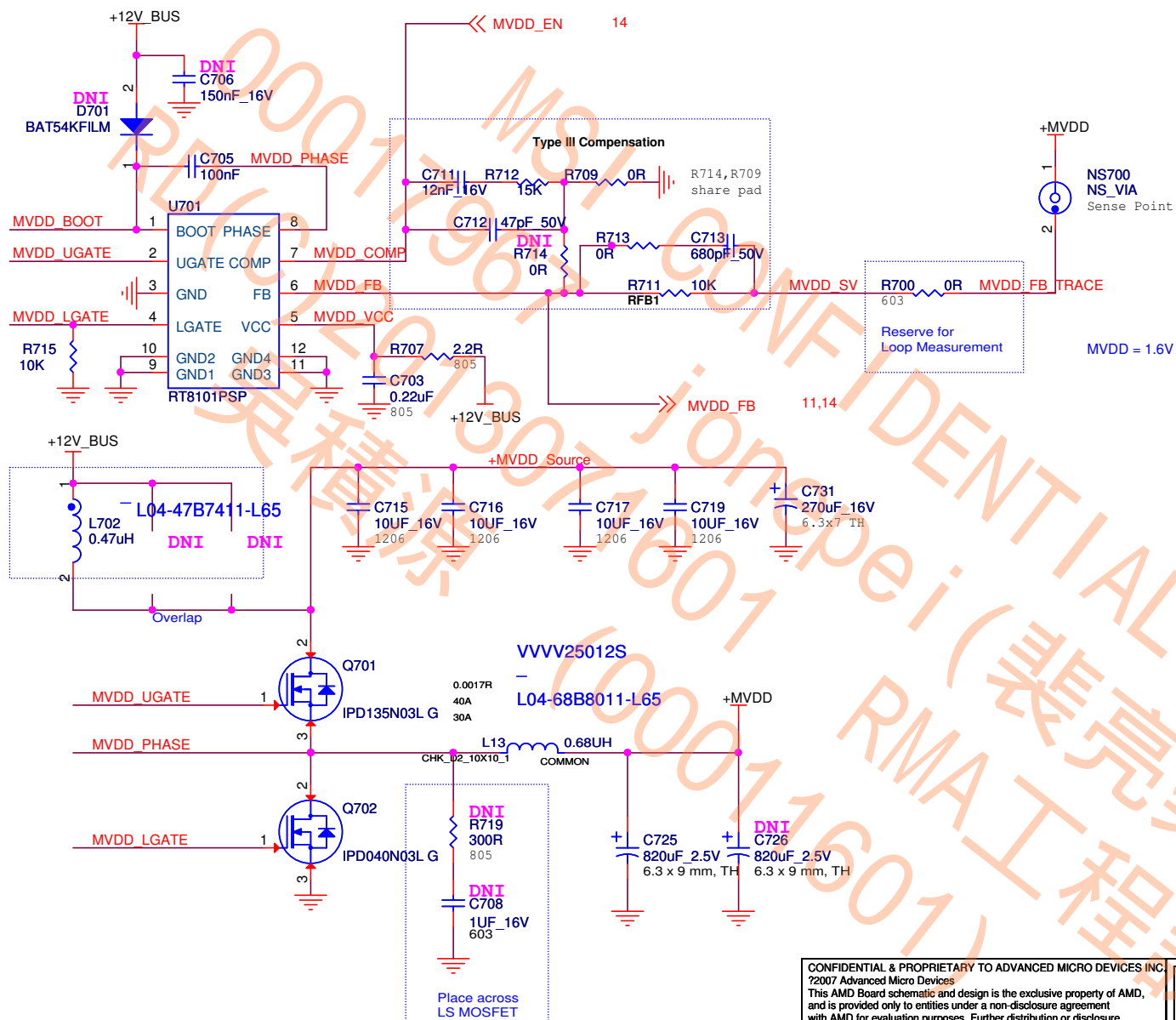
Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661



VDDC applied externally or generated internally from the IC, must be in regulation before IC start soft-start sequence.

1. For 5V Gate Drive application:
External 5V, EXT is applied to this pin.
2. For 8V or 12V Gate Drive application:
+VDDC is generated internally and this is an output with 20mA minimum current capacity.



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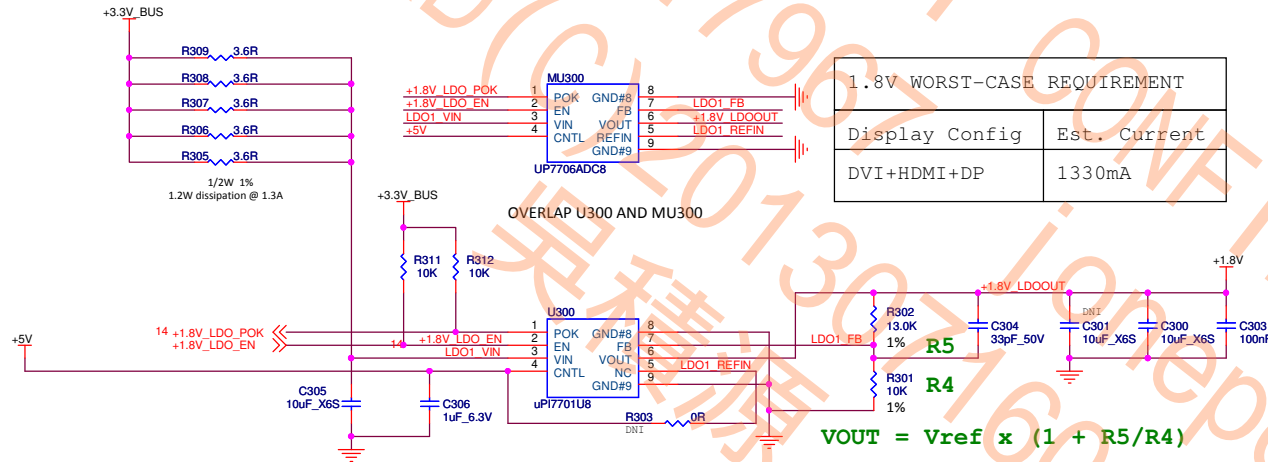
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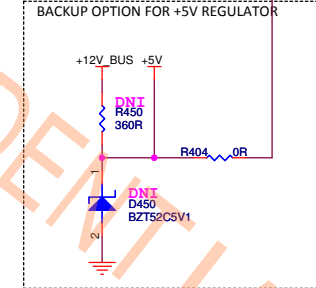
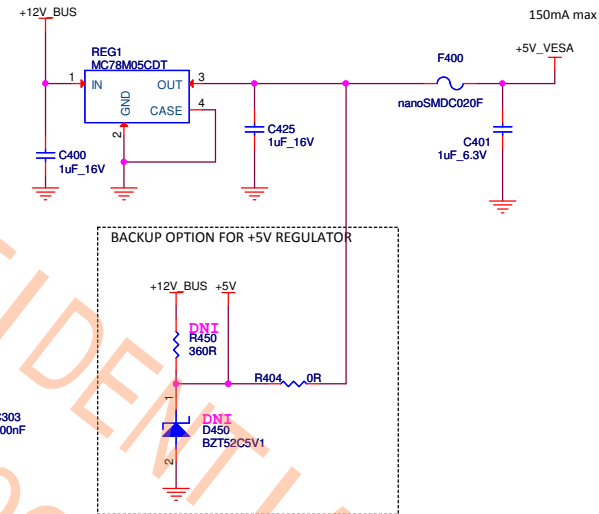
Title RH Turks GDDR5 4pcs x 32 dDVI-D+HDMI/DP+VGD/DP Doc No. 102-C24901-00

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

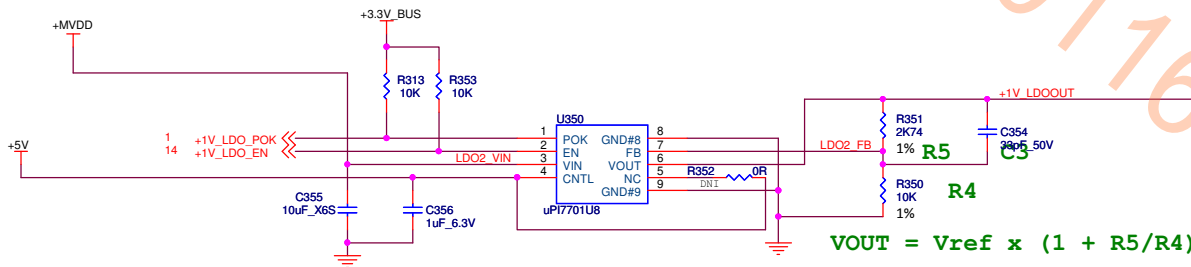


1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

Regulator for +5V and +5V_VESA
Iout max = 150mA (VGA+DVI+HDMI)

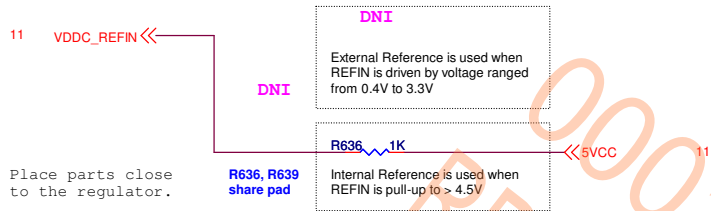


LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA

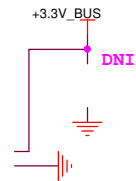
VDDC Reference Voltage Selection



VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

I2C VOLTAGE REFERENCE FOR VDDC (not for production)

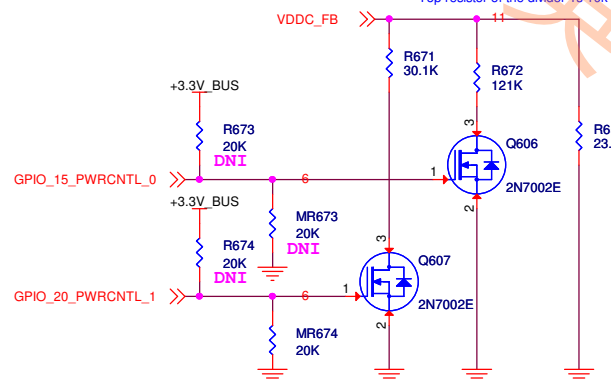


I2C ADDRESS:
A6

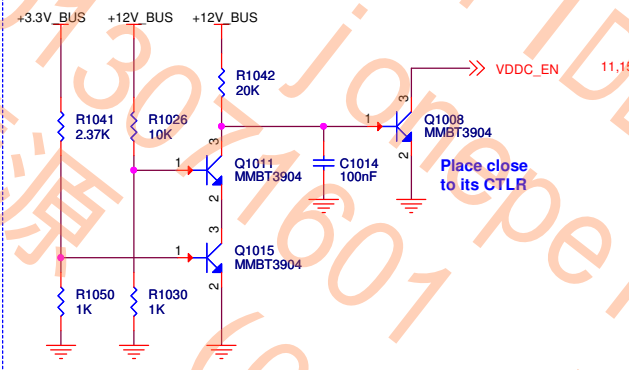
VDDC Low Side Divider

R650 must be populated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.

Low state 0.9V
Middle state 1.0V
High state 1.1V
Vref=0.6V
Top resistor of the divider 1s 10k



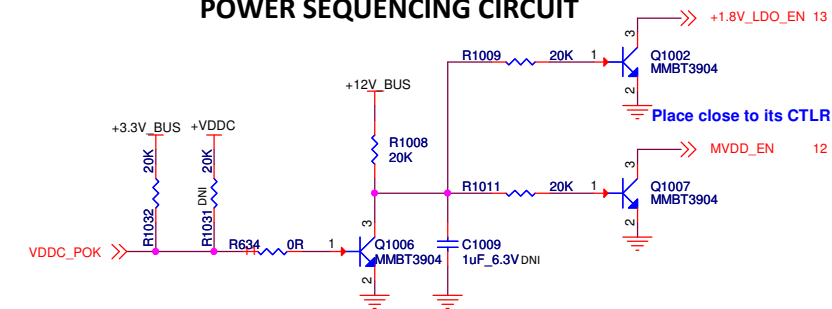
12V_BUS & 3V3_BUS POWER SEQUENCING



Install R1010 to gate 1V LDO with 1.8V LDO.

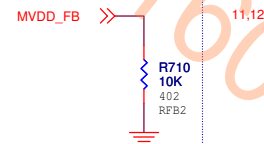


POWER SEQUENCING CIRCUIT



MVDD Low Side Divider

MVDD = 1.6V
Vref = 0.8V



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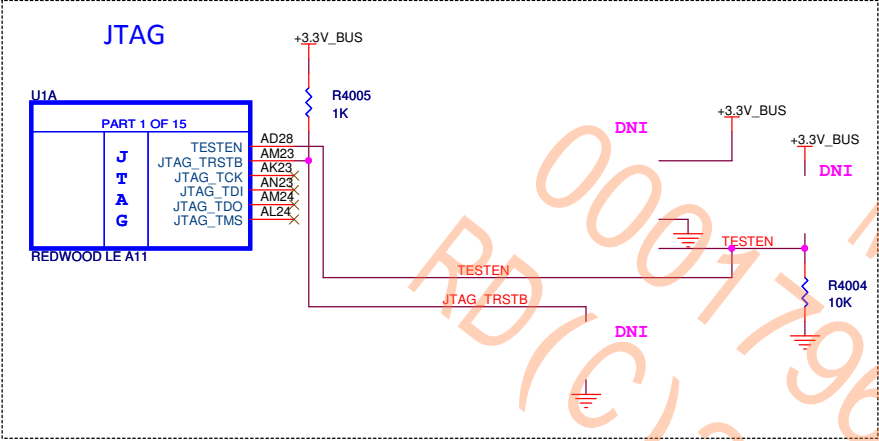


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SWITCH CONNECTIONS TO PINSTRAPS

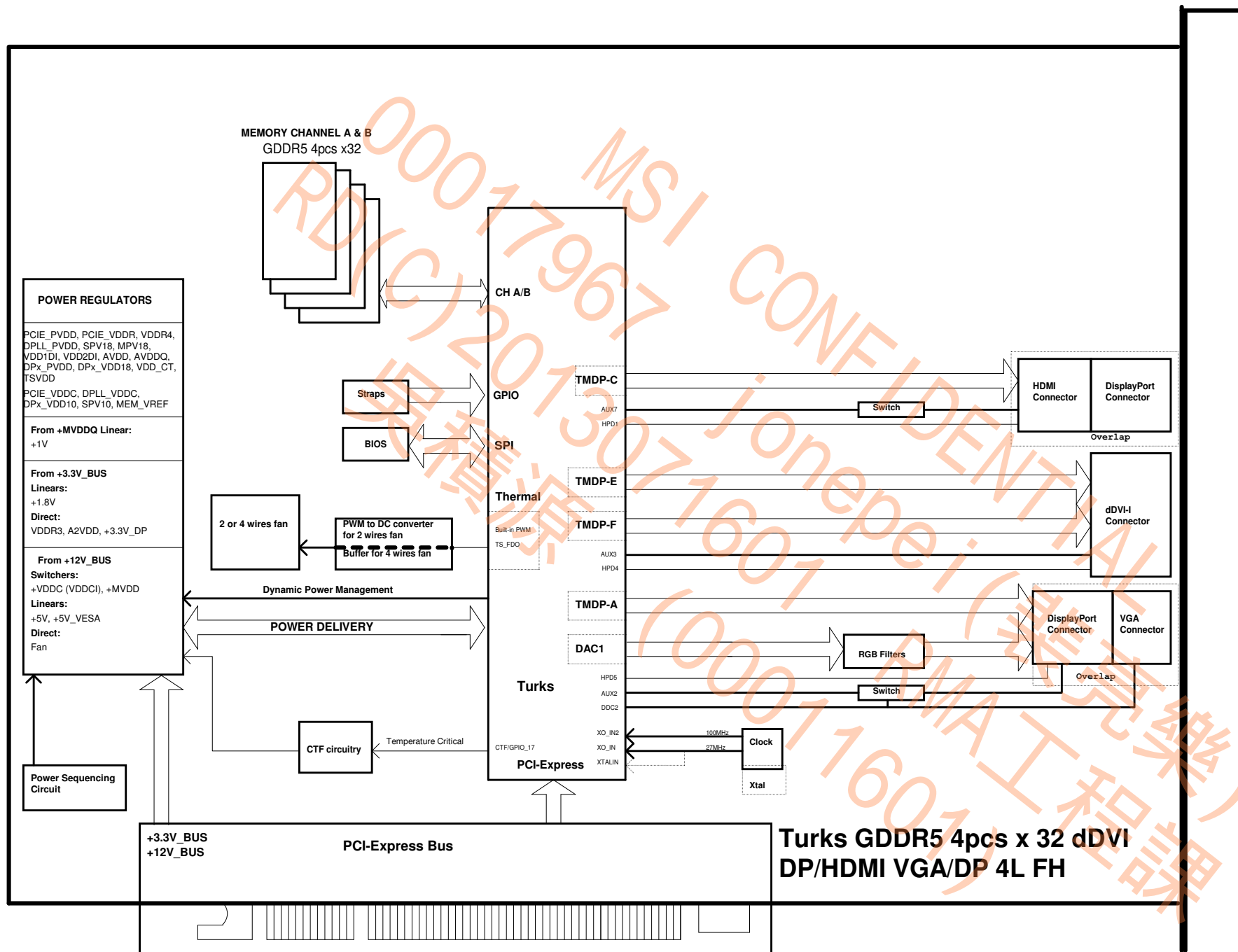
LM96163 FOR BACKUP THERMAL CONTROL




SCL/SDA PORT DEBUG ACCESS

Place connector on the back side
(easily accessible and not blocked by the heatsink).

TACH Connection is for testing
and RPM measurement only



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Sheet of 102-C24901-00		
Title RH Turks GDDR3 4pcSut02 dDVI-D+HDMI/DP+VGD/DP		Doc No. 18 17

00A	00A	Nov 11, 2010	1)Based on: V250-4.0
		10.18.2011	1. Change 128X16 to 128bit P.04 referene C245