P393-A01 DT SKU 4

G92-270, 16Mx32 GDDR3 900 MHz, DVI-I-DL, DVI-I-DL, HDTVout

Table of Contents:

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10393-base-100	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU_DT_0000	600-10393-0000-100	P393 G92-300 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
2	SKU_DT_0002	600-10393-0002-100	P393 G92-200 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
3	SKU_WS_0500	600-50393-0500-100	P393 G92-875 512MB GDDR3 16Mx32 DVI-I+DP+STEREO
4	SKU_WS_0501	600-50393-0501-100	P393 G92-850 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
5	SKU_DT_0004	600-10393-0004-100	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
6	SKU_DT_0006	600-10393-0006-100	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I, Apple
7	SKU_WS_0503	600-50393-0503-100	P393 G92-875 512Mb GDDR4 16Mx32 DVI-I+DVI-I+STEREO
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Overview

NVIDIA CORPORATION
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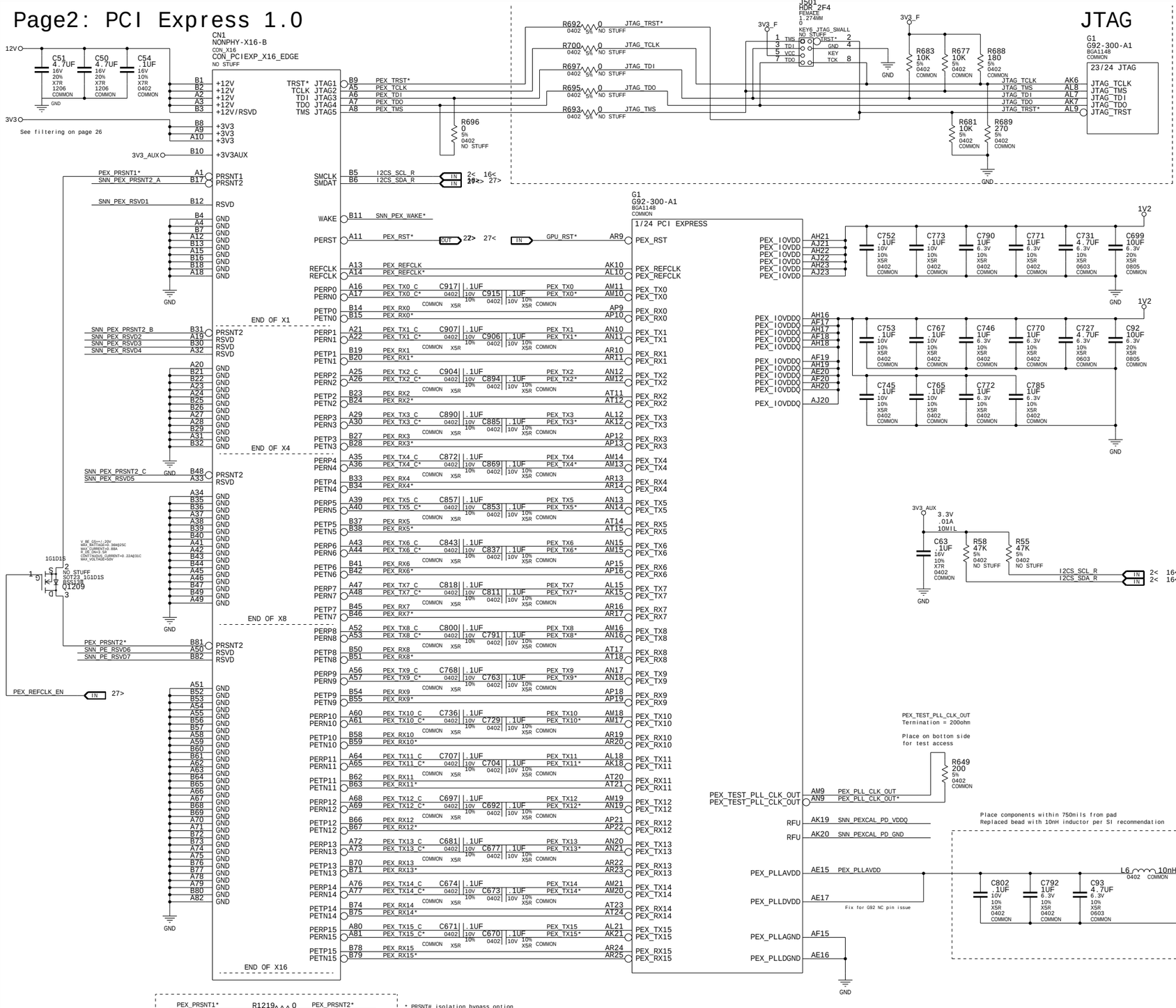
Page2: PCI Express 1.0



PEX NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
PEX_REFCLK	1	100DIFF	PEX_REFCLK
PEX_REFCLK*	1	100DIFF	PEX_REFCLK
PEX_TX0_C	1	90DIFF	PEX_TX0_C
PEX_TX0_C*	1	90DIFF	PEX_TX0_C
PEX_TX1_C	1	90DIFF	PEX_TX1_C
PEX_TX1_C*	1	90DIFF	PEX_TX1_C
PEX_TX2_C	1	90DIFF	PEX_TX2_C
PEX_TX2_C*	1	90DIFF	PEX_TX2_C
PEX_TX3_C	1	90DIFF	PEX_TX3_C
PEX_TX3_C*	1	90DIFF	PEX_TX3_C
PEX_TX4_C	1	90DIFF	PEX_TX4_C
PEX_TX4_C*	1	90DIFF	PEX_TX4_C
PEX_TX5_C	1	90DIFF	PEX_TX5_C
PEX_TX5_C*	1	90DIFF	PEX_TX5_C
PEX_TX6_C	1	90DIFF	PEX_TX6_C
PEX_TX6_C*	1	90DIFF	PEX_TX6_C
PEX_TX7_C	1	90DIFF	PEX_TX7_C
PEX_TX7_C*	1	90DIFF	PEX_TX7_C
PEX_TX8_C	1	90DIFF	PEX_TX8_C
PEX_TX8_C*	1	90DIFF	PEX_TX8_C
PEX_TX9_C	1	90DIFF	PEX_TX9_C
PEX_TX9_C*	1	90DIFF	PEX_TX9_C
PEX_TX10_C	1	90DIFF	PEX_TX10_C
PEX_TX10_C*	1	90DIFF	PEX_TX10_C
PEX_TX11_C	1	90DIFF	PEX_TX11_C
PEX_TX11_C*	1	90DIFF	PEX_TX11_C
PEX_TX12_C	1	90DIFF	PEX_TX12_C
PEX_TX12_C*	1	90DIFF	PEX_TX12_C
PEX_TX13_C	1	90DIFF	PEX_TX13_C
PEX_TX13_C*	1	90DIFF	PEX_TX13_C
PEX_TX14_C	1	90DIFF	PEX_TX14_C
PEX_TX14_C*	1	90DIFF	PEX_TX14_C
PEX_TX15_C	1	90DIFF	PEX_TX15_C
PEX_TX15_C*	1	90DIFF	PEX_TX15_C
PEX_RX0	1	90DIFF	PEX_RX0
PEX_RX0*	1	90DIFF	PEX_RX0
PEX_RX1	1	90DIFF	PEX_RX1
PEX_RX1*	1	90DIFF	PEX_RX1
PEX_RX2	1	90DIFF	PEX_RX2
PEX_RX2*	1	90DIFF	PEX_RX2
PEX_RX3	1	90DIFF	PEX_RX3
PEX_RX3*	1	90DIFF	PEX_RX3
PEX_RX4	1	90DIFF	PEX_RX4
PEX_RX4*	1	90DIFF	PEX_RX4
PEX_RX5	1	90DIFF	PEX_RX5
PEX_RX5*	1	90DIFF	PEX_RX5
PEX_RX6	1	90DIFF	PEX_RX6
PEX_RX6*	1	90DIFF	PEX_RX6
PEX_RX7	1	90DIFF	PEX_RX7
PEX_RX7*	1	90DIFF	PEX_RX7
PEX_RX8	1	90DIFF	PEX_RX8
PEX_RX8*	1	90DIFF	PEX_RX8
PEX_RX9	1	90DIFF	PEX_RX9
PEX_RX9*	1	90DIFF	PEX_RX9
PEX_RX10	1	90DIFF	PEX_RX10
PEX_RX10*	1	90DIFF	PEX_RX10
PEX_RX11	1	90DIFF	PEX_RX11
PEX_RX11*	1	90DIFF	PEX_RX11
PEX_RX12	1	90DIFF	PEX_RX12
PEX_RX12*	1	90DIFF	PEX_RX12
PEX_RX13	1	90DIFF	PEX_RX13
PEX_RX13*	1	90DIFF	PEX_RX13
PEX_RX14	1	90DIFF	PEX_RX14
PEX_RX14*	1	90DIFF	PEX_RX14
PEX_RX15	1	90DIFF	PEX_RX15
PEX_RX15*	1	90DIFF	PEX_RX15
PEX_TX0	1	90DIFF	PEX_TX0
PEX_TX0*	1	90DIFF	PEX_TX0
PEX_TX1	1	90DIFF	PEX_TX1
PEX_TX1*	1	90DIFF	PEX_TX1
PEX_TX2	1	90DIFF	PEX_TX2
PEX_TX2*	1	90DIFF	PEX_TX2
PEX_TX3	1	90DIFF	PEX_TX3
PEX_TX3*	1	90DIFF	PEX_TX3
PEX_TX4	1	90DIFF	PEX_TX4
PEX_TX4*	1	90DIFF	PEX_TX4
PEX_TX5	1	90DIFF	PEX_TX5
PEX_TX5*	1	90DIFF	PEX_TX5
PEX_TX6	1	90DIFF	PEX_TX6
PEX_TX6*	1	90DIFF	PEX_TX6
PEX_TX7	1	90DIFF	PEX_TX7
PEX_TX7*	1	90DIFF	PEX_TX7
PEX_TX8	1	90DIFF	PEX_TX8
PEX_TX8*	1	90DIFF	PEX_TX8
PEX_TX9	1	90DIFF	PEX_TX9
PEX_TX9*	1	90DIFF	PEX_TX9
PEX_TX10	1	90DIFF	PEX_TX10
PEX_TX10*	1	90DIFF	PEX_TX10
PEX_TX11	1	90DIFF	PEX_TX11
PEX_TX11*	1	90DIFF	PEX_TX11
PEX_TX12	1	90DIFF	PEX_TX12
PEX_TX12*	1	90DIFF	PEX_TX12
PEX_TX13	1	90DIFF	PEX_TX13
PEX_TX13*	1	90DIFF	PEX_TX13
PEX_TX14	1	90DIFF	PEX_TX14
PEX_TX14*	1	90DIFF	PEX_TX14
PEX_TX15	1	90DIFF	PEX_TX15
PEX_TX15*	1	90DIFF	PEX_TX15
PEX_PLL_CLK_OUT	1	90DIFF	PEX_PLL_CLK_OUT
PEX_PLL_CLK_OUT*	1	90DIFF	PEX_PLL_CLK_OUT
PEX_RST*	3	50OHM	
PEX_TRST*	3	50OHM	
PEX_TCLK	3	50OHM	
PEX_TDI	3	50OHM	
PEX_TDO	3	50OHM	
PEX_TMS	3	50OHM	
JTAG_TCLK	3	50OHM	
JTAG_TMS	3	50OHM	
JTAG_TDI	3	50OHM	
JTAG_TDO	3	50OHM	
JTAG_TRST*	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
PEX_PLLAVDD	1.2V	0.25A	12MIL
PEX_PLLDVDD	1.2V	0.10A	12MIL

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	PCI Express 1.0

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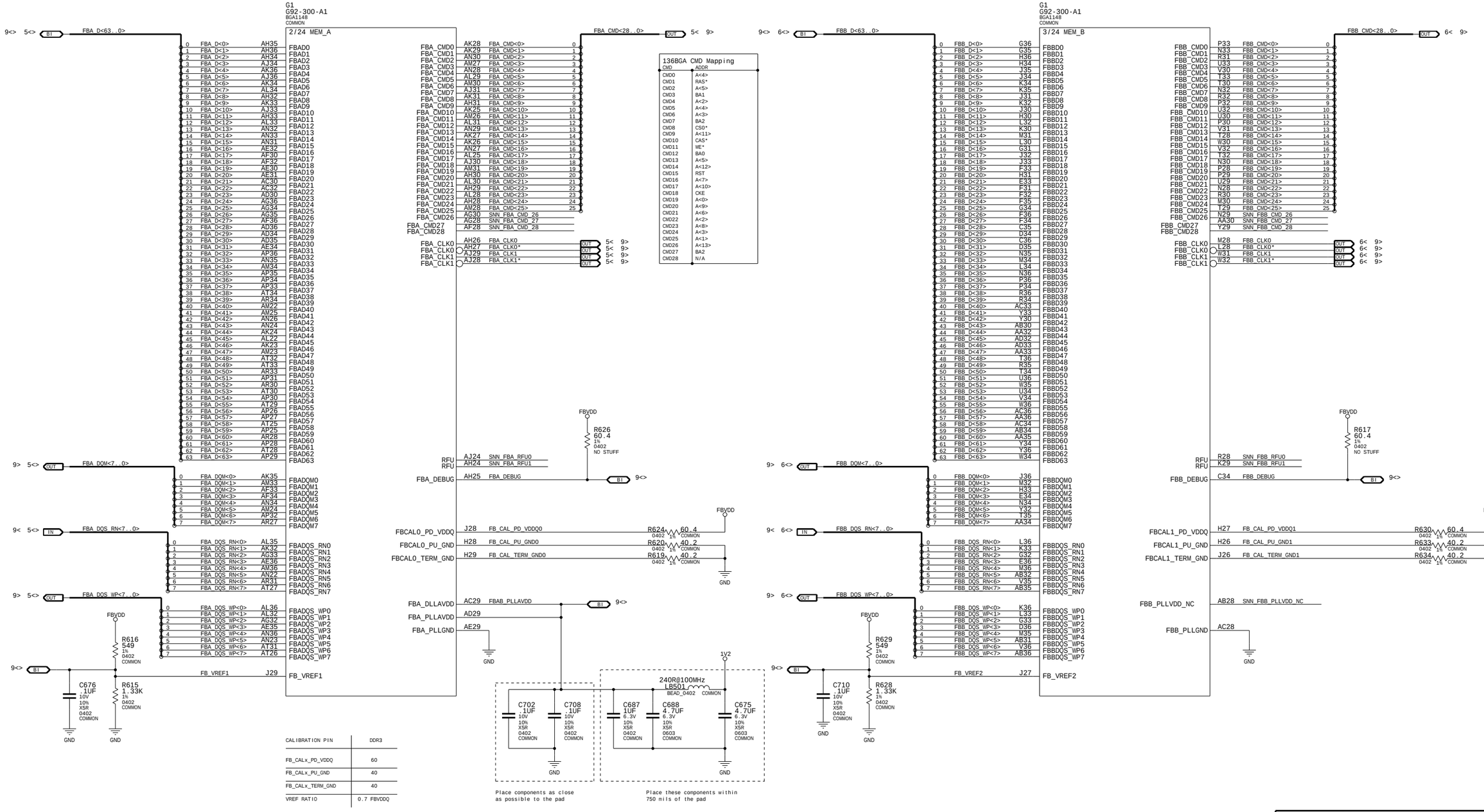
Page3: MEMORY: GPU Partition A/B



ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	MEMORY: GPU Partition A/B

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Page4: MEMORY: GPU Partition C/D

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	MEMORY: GPU Partition C/D

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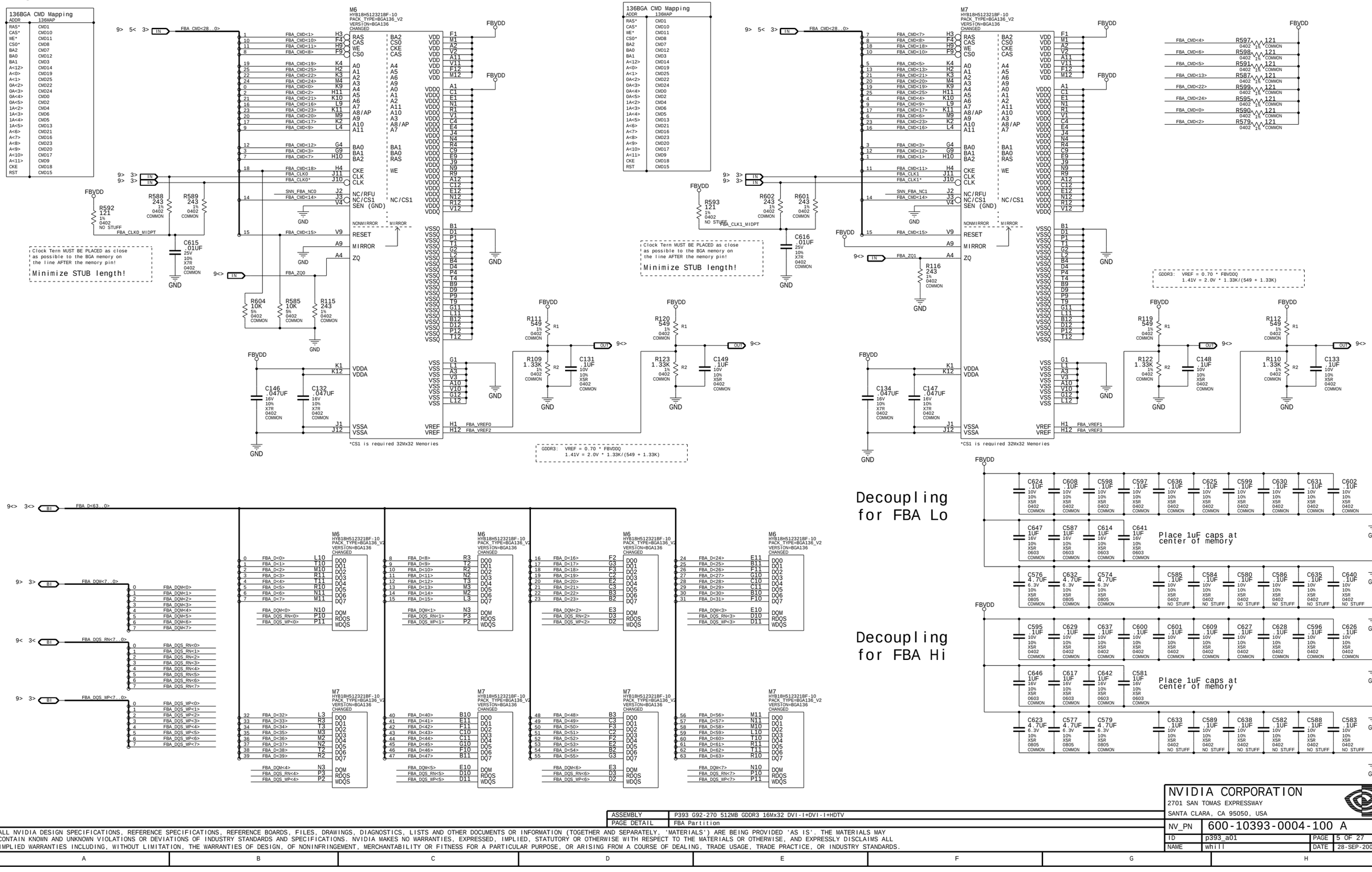
Page5: FBA Partition



ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	FBA Partition

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Page6: FBB Partition

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

M5 / M8: HYB18H512321BF-10, PACK_TYPE=BGA136_V2, VERSION=BGA136 CHANGED

FBB_CMD<28..0>

FBB_CLK0_MIDPT — R613 121 1% 0402 NO STUFF

FBB_CLK1_MIDPT — R586 121 1% 0402 NO_STUFF

Clock Term MUST BE PLACED as close as possible to the BGA memory on the line AFTER the memory pin!

Minimize STUB length!

R609 243 1% 0402 COMMON — R611 243 1% 0402 COMMON — C659 .01UF 25V 10% X7R 0402 COMMON

R596 243 1% 0402 COMMON — R600 243 1% 0402 COMMON — C610 .01UF 25V 10% X7R 0402 COMMON

FBB_ZQ0 — R608 10K 5% 0402 COMMON — R606 10K 5% 0402 COMMON — R104 243 1% 0402 COMMON

FBB_ZQ1 — R121 243 1% 0402 COMMON

C109 .047UF 16V 10% X7R 0402 COMMON — C129 .047UF 16V 10% X7R 0402 COMMON

C130 .047UF 16V 10% X7R 0402 COMMON — C141 .047UF 16V 10% X7R 0402 COMMON

R105 549 1% 0402 COMMON — R106 1.33K 1% 0402 COMMON — C108 .1UF 10V 10% X5R 0402 COMMON

R107 549 1% 0402 COMMON — R108 1.33K 1% 0402 COMMON — C128 .1UF 10V 10% X5R 0402 COMMON

R118 549 1% 0402 COMMON — R117 1.33K 1% 0402 COMMON — C144 .1UF 10V 10% X5R 0402 COMMON

R114 549 1% 0402 COMMON — R113 1.33K 1% 0402 COMMON — C136 .1UF 10V 10% X5R 0402 COMMON

*CS1 is required 32Mx32 Memories

GDDR3: VREF = 0.70 * FBVDDQ
1.41V = 2.0V * 1.33K/(549 + 1.33K)

R605 121 1% 0402 COMMON — FBB_CMD<4>
R603 121 1% 0402 COMMON — FBB_CMD<6>
R594 121 1% 0402 COMMON — FBB_CMD<5>
R584 121 1% 0402 COMMON — FBB_CMD<13>
R614 121 1% 0402 COMMON — FBB_CMD<22>
R610 121 1% 0402 COMMON — FBB_CMD<24>
R612 121 1% 0402 COMMON — FBB_CMD<0>
R607 121 1% 0402 COMMON — FBB_CMD<2>

FBB_D<63..0>

FBB_DQM<7..0>

FBB_DQS_RN<7..0>

FBB_DQS_WP<7..0>

Decoupling for FBB Lo

Decoupling for FBB Hi

C666 .1UF 10V 10% X5R 0402 COMMON — C656 .1UF 10V 10% X5R 0402 COMMON — C661 .1UF 10V 10% X5R 0402 COMMON — C652 .1UF 10V 10% X5R 0402 COMMON — C660 .1UF 10V 10% X5R 0402 COMMON — C667 .1UF 10V 10% X5R 0402 COMMON — C655 .1UF 10V 10% X5R 0402 COMMON — C657 .1UF 10V 10% X5R 0402 COMMON — C653 .1UF 10V 10% X5R 0402 COMMON — C650 .1UF 10V 10% X5R 0402 COMMON

C645 1UF 10V 10% X5R 0603 COMMON — C665 1UF 16V 10% X5R 0603 COMMON — C663 1UF 16V 10% X5R 0603 COMMON — C669 1UF 16V 10% X5R 0603 COMMON

Place 1uF caps at center of memory

C672 4.7UF 6.3V 10% X5R 0805 COMMON — C644 4.7UF 6.3V 10% X5R 0805 COMMON — C664 4.7UF 6.3V 10% X5R 0805 COMMON — C654 .1UF 10V 10% X5R 0402 NO STUFF — C651 .1UF 10V 10% X5R 0402 NO STUFF — C668 .1UF 10V 10% X5R 0402 NO STUFF — C658 .1UF 10V 10% X5R 0402 NO STUFF — C648 .1UF 10V 10% X5R 0402 NO STUFF — C662 .1UF 10V 10% X5R 0402 NO STUFF

C590 .1UF 10V 10% X5R 0402 COMMON — C618 .1UF 10V 10% X5R 0402 COMMON — C613 .1UF 10V 10% X5R 0402 COMMON — C634 .1UF 10V 10% X5R 0402 COMMON — C607 .1UF 10V 10% X5R 0402 COMMON — C639 .1UF 10V 10% X5R 0402 COMMON — C606 .1UF 10V 10% X5R 0402 COMMON — C643 .1UF 10V 10% X5R 0402 COMMON — C622 .1UF 10V 10% X5R 0402 COMMON — C575 .1UF 10V 10% X5R 0402 COMMON

C591 1UF 10V 10% X5R 0603 COMMON — C649 1UF 16V 10% X5R 0603 COMMON — C620 1UF 16V 10% X5R 0603 COMMON — C621 1UF 16V 10% X5R 0603 COMMON

Place 1uF caps at center of memory

C572 4.7UF 6.3V 10% X5R 0805 COMMON — C605 4.7UF 6.3V 10% X5R 0805 COMMON — C603 4.7UF 6.3V 10% X5R 0805 COMMON — C612 .1UF 10V 10% X5R 0402 NO STUFF — C611 .1UF 10V 10% X5R 0402 NO STUFF — C619 .1UF 10V 10% X5R 0402 NO STUFF — C604 .1UF 10V 10% X5R 0402 NO STUFF — C573 .1UF 10V 10% X5R 0402 NO STUFF — C578 .1UF 10V 10% X5R 0402 NO STUFF

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	FBB Partition

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Page7: FBC Partition

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

M3 / M4: HYB18H512321BF-10, PACK_TYPE=BGA136_V2, VERSION=BGA136, CHANGED

Clock Term MUST BE PLACED as close as possible to the BGA memory on the line AFTER the memory pin!

Minimize STUB length!

*CS1 is required 32Mx32 Memories

GDDR3: VREF = 0.70 * FBVDDQ
1.41V = 2.0V * 1.33K/(549 + 1.33K)

Decoupling for FBC Lo

Decoupling for FBC Hi

Place 1uF caps at center of memory

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	FBC Partition

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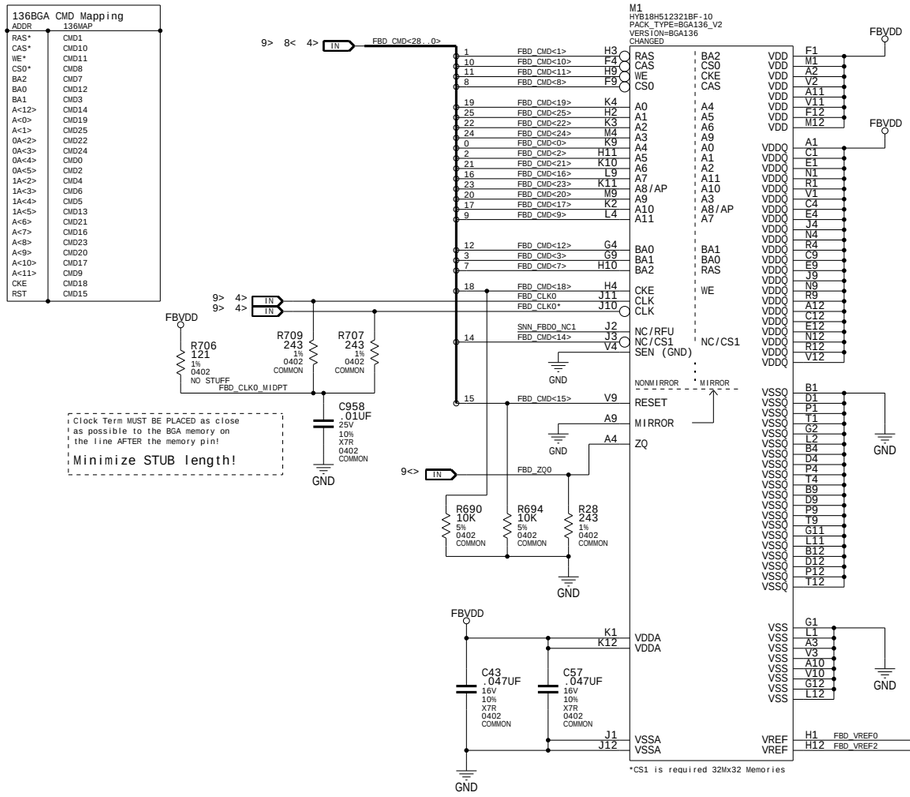
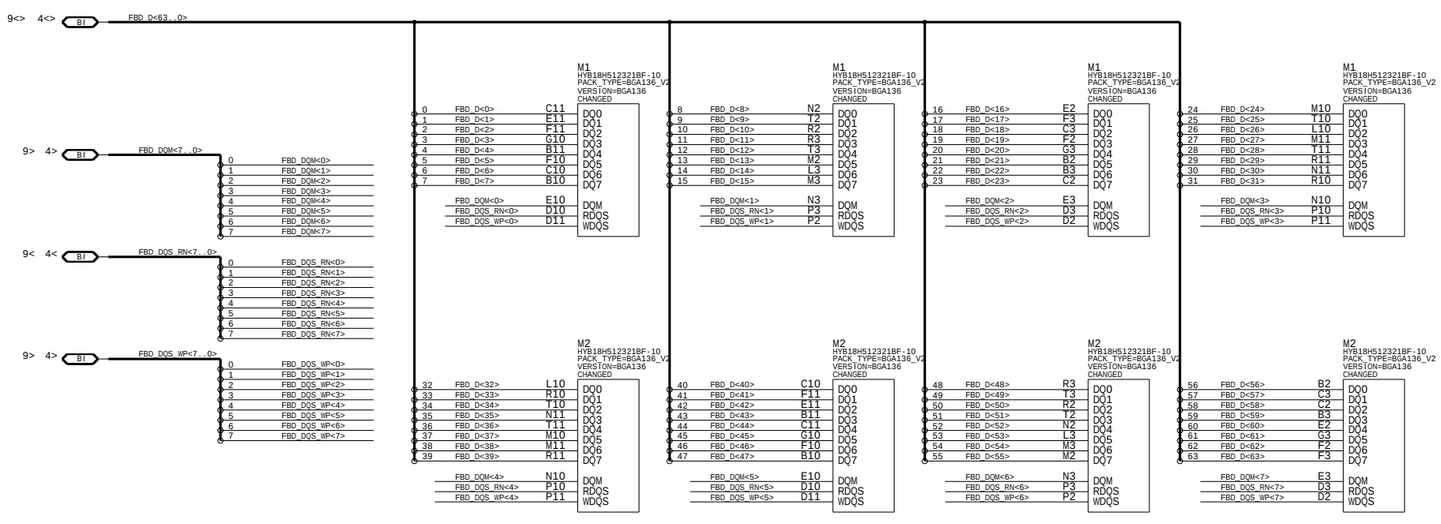
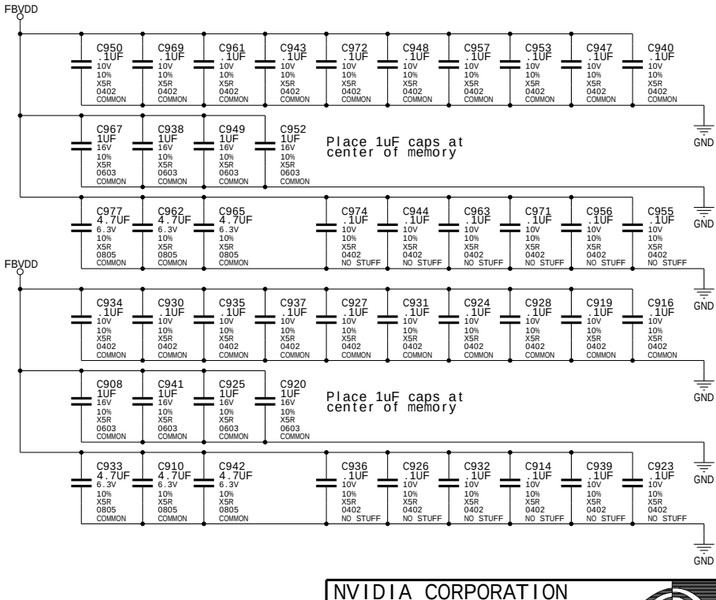
Page8: FBD Partition





Decoupling for FBD Lo

Decoupling for FBD Hi



ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	FBD Partition

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Page9: FrameBuffer Net Rules

NET RULES for FrameBuffer A/B

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
5< 3>	OUT	FBA_CLK0	1	80DIFF	FBA_CLK0
5< 3>	OUT	FBA_CLK0*	1	80DIFF	FBA_CLK0
5< 3>	OUT	FBA_CLK1	1	80DIFF	FBA_CLK1
5< 3>	OUT	FBA_CLK1*	1	80DIFF	FBA_CLK1
5< 3>	OUT	FBA_CMD<28..0>	1	40OHM	
5<> 3>	OUT	FBA_DQS_WP<7..0>	1	40OHM	
5<> 3<	IN	FBA_DQS_RN<7..0>	1	40OHM	
5<> 3>	OUT	FBA_DQ#<7..0>	1	40OHM	
5<> 3<>	BI	FBA_D<63..0>	1	40OHM	

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
6< 3>	OUT	FBB_CLK0	1	80DIFF	FBB_CLK0
6< 3>	OUT	FBB_CLK0*	1	80DIFF	FBB_CLK0
6< 3>	OUT	FBB_CLK1	1	80DIFF	FBB_CLK1
6< 3>	OUT	FBB_CLK1*	1	80DIFF	FBB_CLK1
6< 3>	OUT	FBB_CMD<28..0>	1	40OHM	
6<> 3>	OUT	FBB_DQS_WP<7..0>	1	40OHM	
6<> 3<	IN	FBB_DQS_RN<7..0>	1	40OHM	
6<> 3>	OUT	FBB_DQ#<7..0>	1	40OHM	
6<> 3<>	BI	FBB_D<63..0>	1	40OHM	
3<>	BI	FBA_DEBUG	1	40OHM	
3<>	BI	FBB_DEBUG	1	40OHM	

		NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
3<>	BI	FBAB_PLLAVDD	1.2V	0.02A	12MIL
5>	BI	FBA_VREF0	1.40V	0.02A	12MIL
5>	BI	FBA_VREF1	1.40V	0.02A	12MIL
5>	BI	FBA_VREF2	1.40V	0.02A	12MIL
5>	BI	FBA_VREF3	1.40V	0.02A	12MIL
5<	BI	FBA_ZQ0	2.0V	0.02A	12MIL
5<	BI	FBA_ZQ1	2.0V	0.02A	12MIL
6>	BI	FBB_VREF0	1.40V	0.02A	12MIL
6>	BI	FBB_VREF1	1.40V	0.02A	12MIL
6>	BI	FBB_VREF2	1.40V	0.02A	12MIL
6>	BI	FBB_VREF3	1.40V	0.02A	12MIL
6<	BI	FBB_ZQ0	2.0V	0.02A	12MIL
6<	BI	FBB_ZQ1	2.0V	0.02A	12MIL
3<>	BI	FB_VREF1	1.40V	0.02A	12MIL
3<>	BI	FB_VREF2	1.40V	0.02A	12MIL

NET RULES for FrameBuffer C/D

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
7< 4>	OUT	FBC_CLK0	1	80DIFF	FBC_CLK0
7< 4>	OUT	FBC_CLK0*	1	80DIFF	FBC_CLK0
7< 4>	OUT	FBC_CLK1	1	80DIFF	FBC_CLK1
7< 4>	OUT	FBC_CLK1*	1	80DIFF	FBC_CLK1
7< 4>	OUT	FBC_CMD<28..0>	1	40OHM	
7<> 4>	OUT	FBC_DQS_WP<7..0>	1	40OHM	
7<> 4<	IN	FBC_DQS_RN<7..0>	1	40OHM	
7<> 4>	OUT	FBC_DQ#<7..0>	1	40OHM	
7<> 4<>	BI	FBC_D<63..0>	1	40OHM	

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
8< 4>	OUT	FBD_CLK0	1	80DIFF	FBD_CLK0
8< 4>	OUT	FBD_CLK0*	1	80DIFF	FBD_CLK0
8< 4>	OUT	FBD_CLK1	1	80DIFF	FBD_CLK1
8< 4>	OUT	FBD_CLK1*	1	80DIFF	FBD_CLK1
8< 4>	OUT	FBD_CMD<28..0>	1	40OHM	
8<> 4>	OUT	FBD_DQS_WP<7..0>	1	40OHM	
8<> 4<	IN	FBD_DQS_RN<7..0>	1	40OHM	
8<> 4>	OUT	FBD_DQ#<7..0>	1	40OHM	
8<> 4<>	BI	FBD_D<63..0>	1	40OHM	
4<>	BI	FBC_DEBUG	1	40OHM	
4<>	BI	FBD_DEBUG	1	40OHM	

		NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
4<>	BI	FBCD_PLLAVDD	1.2V	0.02A	12MIL
7>	BI	FBC_VREF0	1.40V	0.02A	12MIL
7>	BI	FBC_VREF1	1.40V	0.02A	12MIL
7>	BI	FBC_VREF2	1.40V	0.02A	12MIL
7>	BI	FBC_VREF3	1.40V	0.02A	12MIL
7<	BI	FBC_ZQ0	2.0V	0.02A	12MIL
7<	BI	FBC_ZQ1	2.0V	0.02A	12MIL
8>	BI	FBD_VREF0	1.40V	0.02A	12MIL
8>	BI	FBD_VREF1	1.40V	0.02A	12MIL
8>	BI	FBD_VREF2	1.40V	0.02A	12MIL
8>	BI	FBD_VREF3	1.40V	0.02A	12MIL
8<	BI	FBD_ZQ0	2.0V	0.02A	12MIL
8<	BI	FBD_ZQ1	2.0V	0.02A	12MIL

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	FrameBuffer Net Rules

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Page10: DACA Interface

DACA NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	DACA_RED	1	75OHM	
IN	DACA_GREEN	1	75OHM	
IN	DACA_BLUE	1	75OHM	
IN	DACA_RED_F	1	75OHM	
IN	DACA_GREEN_F	1	75OHM	
IN	DACA_BLUE_F	1	75OHM	
12< 10> IN	DACA_RED_DVI	1	75OHM	
12< 10> IN	DACA_GREEN_DVI	1	75OHM	
12< 10> IN	DACA_BLUE_DVI	1	75OHM	
IN	DACA_HS	2	50OHM	
IN	DACA_VS	2	50OHM	
IN	DACA_HS_BUF	2	50OHM	
IN	DACA_VS_BUF	2	50OHM	
IN	DACA_HS_BUF_R	2	50OHM	
IN	DACA_VS_BUF_R	2	50OHM	
12< 10> IN	DACA_HS_DVI	2	50OHM	
12< 10> IN	DACA_VS_DVI	2	50OHM	
IN	I2CA_SCL	3	50OHM	
IN	I2CA_SDA	3	50OHM	
27> 10< IN	I2CA_SCL_R	3	50OHM	
27<> 10< IN	I2CA_SDA_R	3	50OHM	
12< 10> IN	I2CA_SCL_DVI	3	50OHM	
12< 10> IN	I2CA_SDA_DVI	3	50OHM	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	DACA_VREF			12MIL
IN	DACA_RSET			12MIL
BI	DACA_VDD	3.3V	0.100A	16MIL
12< 10> IN	DACA_GND	0.0V		16MIL

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	DACA Interface

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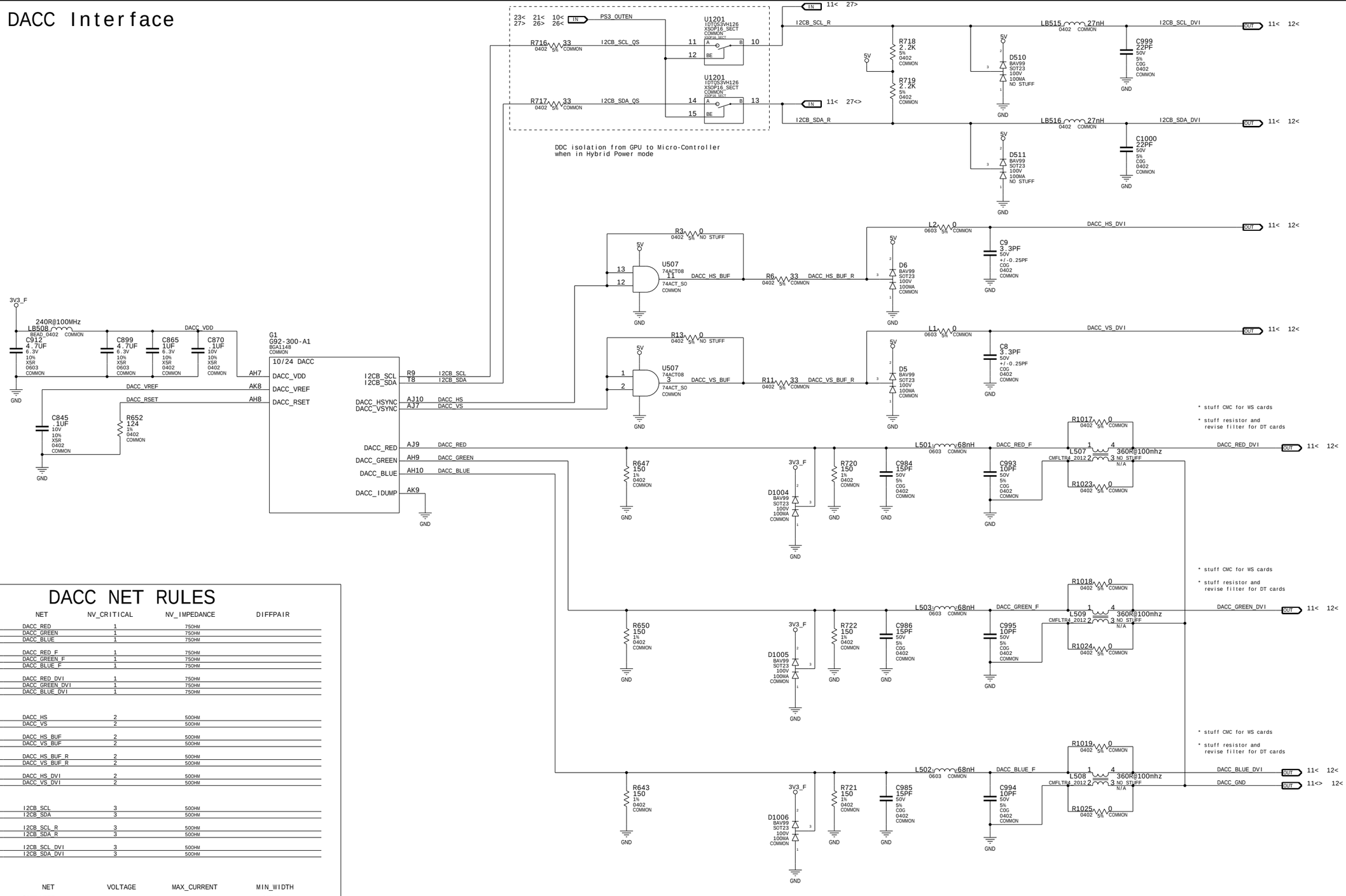
Page11: DACC Interface



DACC NET RULES

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
	IN	DACC_RED	1	75OHM	
	IN	DACC_GREEN	1	75OHM	
	IN	DACC_BLUE	1	75OHM	
	IN	DACC_RED_F	1	75OHM	
	IN	DACC_GREEN_F	1	75OHM	
	IN	DACC_BLUE_F	1	75OHM	
12< 11>	IN	DACC_RED_DVI	1	75OHM	
12< 11>	IN	DACC_GREEN_DVI	1	75OHM	
12< 11>	IN	DACC_BLUE_DVI	1	75OHM	
	IN	DACC_HS	2	50OHM	
	IN	DACC_VS	2	50OHM	
	IN	DACC_HS_BUF	2	50OHM	
	IN	DACC_VS_BUF	2	50OHM	
	IN	DACC_HS_BUF_R	2	50OHM	
	IN	DACC_VS_BUF_R	2	50OHM	
12< 11>	IN	DACC_HS_DVI	2	50OHM	
12< 11>	IN	DACC_VS_DVI	2	50OHM	
	IN	I2CB_SCL	3	50OHM	
	IN	I2CB_SDA	3	50OHM	
27> 11<	IN	I2CB_SCL_R	3	50OHM	
27<> 11<	IN	I2CB_SDA_R	3	50OHM	
12< 11>	IN	I2CB_SCL_DVI	3	50OHM	
12< 11>	IN	I2CB_SDA_DVI	3	50OHM	

		NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
	IN	DACC_VREF			12MIL
	IN	DACC_RSET			12MIL
	BI	DACC_VDD	3.3V	0.100A	16MIL
12< 11>	BI	DACC_GND	0.0V		16MIL

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	DACC Interface

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Page12: IFP A/B and C/D Interface

IFPABCD NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RSET			12MIL
IFPCD_RSET			12MIL
GPIO0_DVIAB_HPD_F	3	50OHM	
GPIO0_DVIAB_HPD_R	3	50OHM	
GPIO1_DVICD_HPD_F	3	50OHM	
GPIO1_DVICD_HPD_R	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLLVDD	1.8V	0.03A	16MIL
IFPAB_IOVDD	3.3V	0.09A	16MIL
IFPCD_PLLVDD	1.8V	0.03A	16MIL
IFPCD_IOVDD	3.3V	0.09A	16MIL

NET RULES

NET	DIFFPAIR	NV_CRITICAL	NV_IMPEDANCE
IFPA_TXC*	IFPAB_TXC	1	100DIFF
IFPA_TXC	IFPAB_TXC	1	100DIFF
IFPA_TXD0*	IFPAB_TXD0	1	100DIFF
IFPA_TXD0	IFPAB_TXD0	1	100DIFF
IFPA_TXD1*	IFPAB_TXD1	1	100DIFF
IFPA_TXD1	IFPAB_TXD1	1	100DIFF
IFPA_TXD2*	IFPAB_TXD2	1	100DIFF
IFPA_TXD2	IFPAB_TXD2	1	100DIFF
IFPB_TXD4*	IFPAB_TXD4	1	100DIFF
IFPB_TXD4	IFPAB_TXD4	1	100DIFF
IFPB_TXD5*	IFPAB_TXD5	1	100DIFF
IFPB_TXD5	IFPAB_TXD5	1	100DIFF
IFPB_TXD6*	IFPAB_TXD6	1	100DIFF
IFPB_TXD6	IFPAB_TXD6	1	100DIFF

NET RULES

NET	DIFFPAIR	NV_CRITICAL	NV_IMPEDANCE
IFPC_TXC*	IFPCD_TXC	1	100DIFF
IFPC_TXC	IFPCD_TXC	1	100DIFF
IFPC_TXD0*	IFPCD_TXD0	1	100DIFF
IFPC_TXD0	IFPCD_TXD0	1	100DIFF
IFPC_TXD1*	IFPCD_TXD1	1	100DIFF
IFPC_TXD1	IFPCD_TXD1	1	100DIFF
IFPC_TXD2*	IFPCD_TXD2	1	100DIFF
IFPC_TXD2	IFPCD_TXD2	1	100DIFF
IFPD_TXD4*	IFPCD_TXD4	1	100DIFF
IFPD_TXD4	IFPCD_TXD4	1	100DIFF
IFPD_TXD5*	IFPCD_TXD5	1	100DIFF
IFPD_TXD5	IFPCD_TXD5	1	100DIFF
IFPD_TXD6*	IFPCD_TXD6	1	100DIFF
IFPD_TXD6	IFPCD_TXD6	1	100DIFF

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	IFP A/B and C/D Interface

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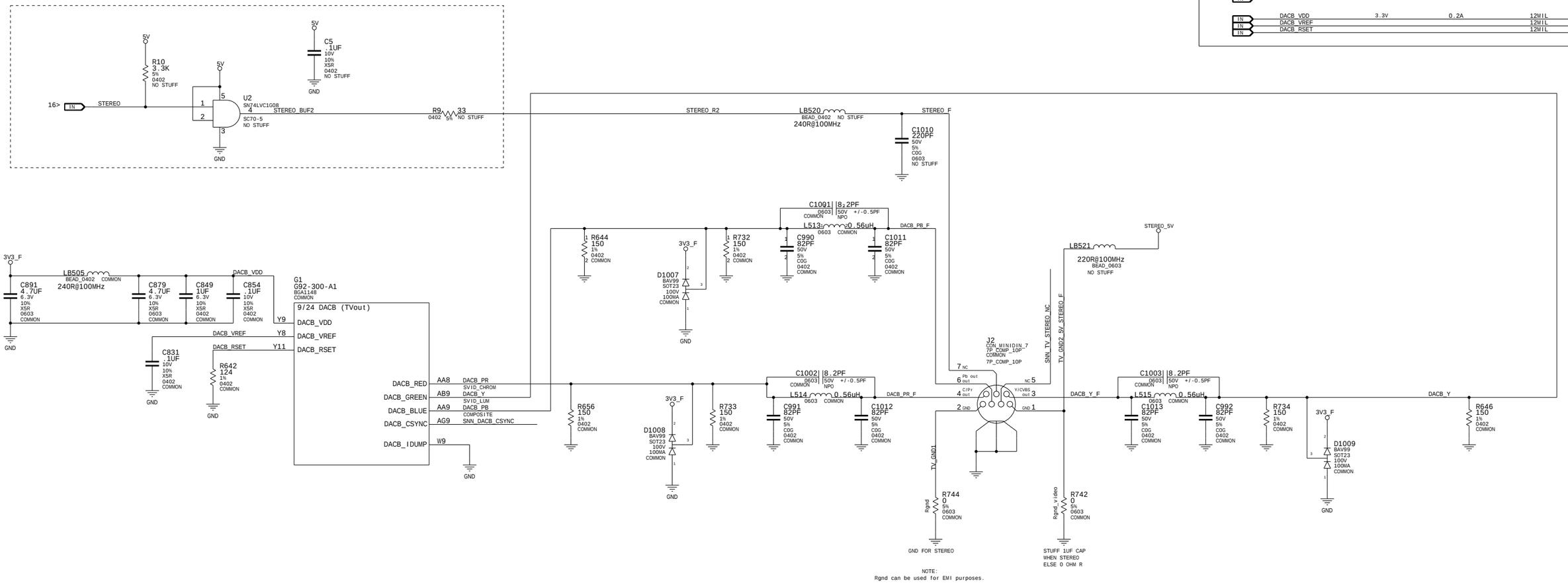
Page13: DACB and Stereo Interface

DACB,STEREO, FL NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	DACB_PR	1	75OHM	
IN	DACB_Y	1	75OHM	
IN	DACB_PB	1	75OHM	
IN	DACB_PR_F	1	75OHM	
IN	DACB_Y_F	1	75OHM	
IN	DACB_PB_F	1	75OHM	
IN	GPU_STEREO_BUF1	3	50OHM	
IN	GPU_STEREO_R1	3	50OHM	
IN	GPIO14_FL_SYNC_R	3	50OHM	
IN	GPU_STEREO_BUF2	3	50OHM	
IN	GPU_STEREO_R2	3	50OHM	
IN	GPU_STEREO_F	3	50OHM	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	TV_GND1	0.0V		12MIL
IN	TV_GND2_5V_STEREO_F	5V	0.5A	20MIL
IN	DACB_VDD	3.3V	0.2A	12MIL
IN	DACB_VREF			12MIL
IN	DACB_RSET			12MIL

Stereo



NOTE:
Rgnd can be used for EMI purposes.

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	DACB and Stereo Interface

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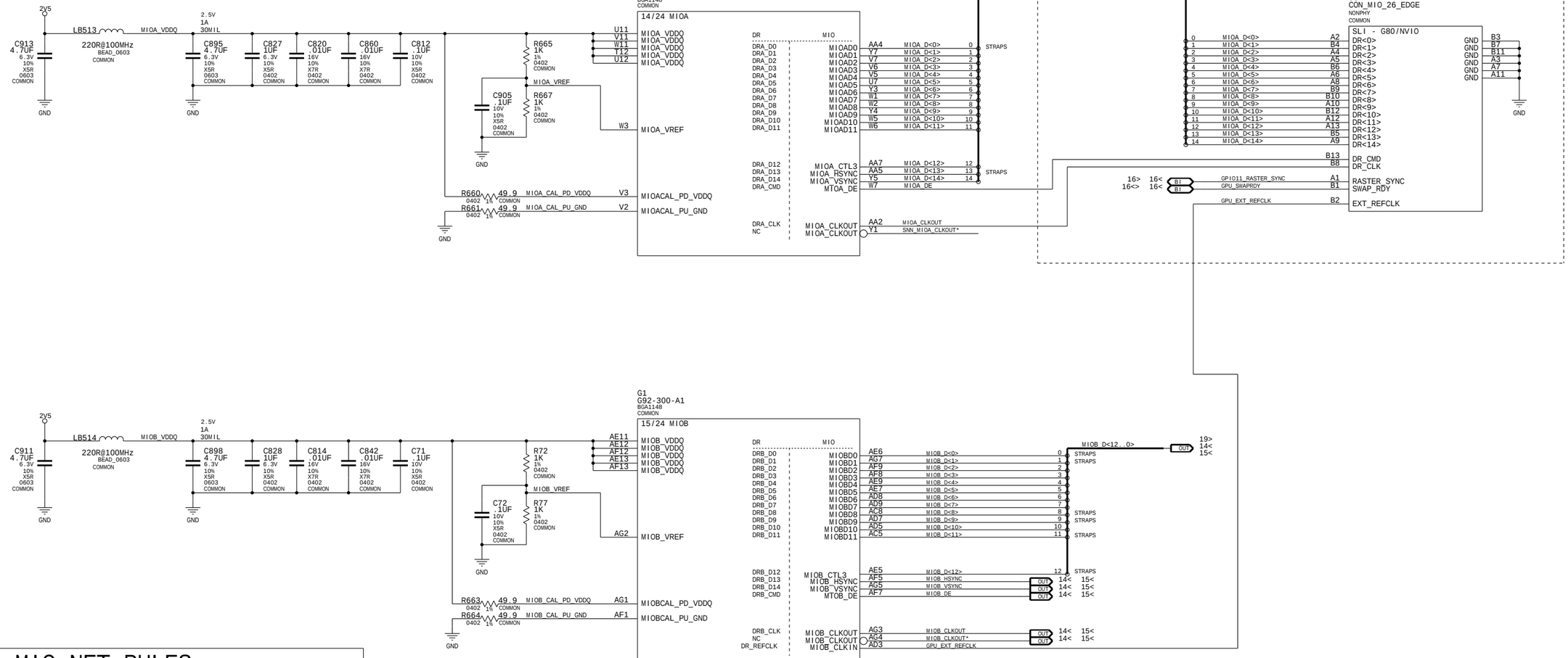
Page14: Multi-use IO(MIO) Interface

MIO Feature Connector



MIO NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
19> 14<	MIOA_D<14..0>	1	50OHM	
	MIOA_CLKOUT	1	50OHM	
	MIOA_DE	1	50OHM	
19> 15< 14>	MIOB_D<12..0>	1	50OHM	
15< 14>	MIOB_HSYNC	1	50OHM	
15< 14>	MIOB_VSYNC	1	50OHM	
15< 14>	MIOB_DE	1	50OHM	
15< 14>	MIOB_CLKOUT	1	100DIFF	MIOB_CLK
15< 14>	MIOB_CLKOUT*	1	100DIFF	MIOB_CLK
	GPU_EXT_REFCLK	1	50OHM	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
	MIOA_VREF	1.25V		12MIL
	MIOACAL_PD_VDDQ			12MIL
	MIOACAL_PU_GND			12MIL
	MIOB_VREF	1.25V		12MIL
	MIOBCAL_PD_VDDQ			12MIL
	MIOBCAL_PU_GND			12MIL

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Multi-use IO(MIO) Interface

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Page15: Display Port (Analogix ANX9802/ANX9805)

* I2C keeper circuit removed

* ANX9805 support

pin 76 - GPIO3 to DP mode, from pin 13, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 74 - GPIO2, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 73 - CEC support via FET and pull-up, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 71 - SPDIF1 - tie to GND, input select 0/1 through internal register

pin 70 - SPDIF0 - support for Audio input, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 68 - NC - tie to GND

100 R1000 NO STUFF 5% 0402 DP_GPIO3
100 R1001 NO STUFF 5% 0402 DP_GPIO2
100 R1002 NO STUFF 5% 0402 DP_CEC
100 R1003 NO STUFF 5% 0402 DP_SPDIF_0
STUFF if ANX9802 is used
DNI ONLY IF using ANX9805

0 R1004 NO STUFF 5% 0402 GPIO3_DP_PIN13
STUFF ONLY IF using ANX9805

16< OUT GPIO3_DP_PIN13 R712 0 0402 5% NO STUFF DP_MODE_R*
High=3.0V
R714 10K 1% 0402 NO STUFF
R713 10K 1% 0402 NO STUFF
High=6.0V
12V_PEX6_F
R715 20K 1% 0402 NO STUFF
DP_MODE*
Q513 BSS138 SOT23_1G1D1S NO STUFF DP_MODE_RC
RC=100ns
R18 10K 5% 0402 NO STUFF
C982 100PF 50V 5% C0G 0402 NO STUFF
R16 1K 1% 0402 NO STUFF DP_MODE_R
EMC
LB3 BEAD_0402 240R@100MHz NO STUFF
C16 220PF 50V 5% C0G 0402 NO STUFF
DP_MODE

27< 16< 12< OUT GPIO1_DVICD_DP_HPD
R702 0 5% 0402 NO STUFF
R704 604K 1% 0402 NO STUFF

3V3_F
R33 100K 5% 0402 NO STUFF
R31 100K 5% 0402 NO STUFF
DP_HPD_F
R32 100K 5% 0402 NO STUFF
R30 100K 5% 0402 NO STUFF
RC=100ns
R19 47K 5% 0402 NO STUFF
C26 100PF 50V 5% C0G 0402 NO STUFF
R17 1K 1% 0402 NO STUFF DP_HPD_R
EMC
LB4 BEAD_0402 240R@100MHz NO STUFF
C17 220PF 50V 5% C0G 0402 NO STUFF

U3
ANX9802
TQFP_80
NO STUFF

100 R821 NO STUFF 5% 0402 DP_XTAL_OUT
16< IN DP_XTAL_IN 1 50OHM
19> 14< 14< IN MIOB_D<12..0>
100 R711 NO STUFF 5% 0402 DP_D_PD
DP_GPIO3
DP_GPIO2
DP_CEC
17> 17< IN DP_SPDIF_0
14< 14> IN MIOB_HSYNC
14< 14> IN MIOB_VSYNC
14< 14> IN MIOB_DE
14< 14> IN MIOB_CLKOUT
14< 14> IN MIOB_CLKOUT*
27<> 23< 17<> 16< 16<> IN I2CC_SDA_R
27> 23<> 17< 16< 16> BI I2CC_SCL_R
16< OUT GPIO10_DP_INT*
16> 16< IN GPU_BUFRST*

1/2
62 XTAL_OUT
63 XTAL_IN
22 21 20 19 17 15 14 13 9 8 7 6 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11
5 3 2 80 78 77 76 74 73 71 70 68 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23
25 HSYNC
24 VSYNC
23 DE
10 CLKP
11 CLKN*
32 CSDA
33 CSCL
28 INTP
37 RESETN*
ANX9802
HPD 29
DSDA 38
DSCL 39
AUXN* 58
AUXP 59
TX3N* 42
TX3P 43
TX2N* 46
TX2P 47
TX1N* 50
TX1P 51
TX0N* 54
TX0P 55
DEV_ADR_SEL_GPIO 34
R_BIAS 64
NC 65
RSVL 40
SNN_DP_NC
DP_RSVD
R29 4.99K 0402 1% NO STUFF
DP_GPIO
R36 1K 0402 5% NO STUFF
DP_RBIAS 12MIL
R22 4.99K 0402 1% NO STUFF
R38 1K 0402 5% NO STUFF
I2CC Address:
H=0x78,0x79,0x7C,0x7D
L=0x70,0x71,0x74,0x75

C48 .1UF 6.3V 10% X5R 0402 NO STUFF
C46 .1UF 6.3V 10% X5R 0402 NO STUFF
Q3 BSS138 SOT23_1G1D1S NO STUFF
Q2 BSS138 SOT23_1G1D1S NO STUFF
DP_AUX_C*
DP_AUX_C
DP_AUX*
DP_AUX

C41 .1UF 6.3V 10% X7R 0402 NO STUFF DP_L3*
C40 .1UF 6.3V 10% X7R 0402 NO STUFF DP_L3
C39 .1UF 6.3V 10% X7R 0402 NO STUFF DP_L2*
C36 .1UF 6.3V 10% X7R 0402 NO STUFF DP_L2
C35 .1UF 6.3V 10% X7R 0402 NO STUFF DP_L1*
C33 .1UF 6.3V 10% X7R 0402 NO STUFF DP_L1
C31 .1UF 6.3V 10% X7R 0402 NO STUFF DP_L0*
C30 .1UF 6.3V 10% X7R 0402 NO STUFF DP_L0

DP_AUX_Q* DP_AUX_Q 100DIFF 1
DP_AUX_Q DP_AUX_Q 100DIFF 1
DP_L3_C* DP_L3_C 100DIFF 1
DP_L3_C DP_L3_C 100DIFF 1
DP_L2_C* DP_L2_C 100DIFF 1
DP_L2_C DP_L2_C 100DIFF 1
DP_L1_C* DP_L1_C 100DIFF 1
DP_L1_C DP_L1_C 100DIFF 1
DP_L0_C* DP_L0_C 100DIFF 1
DP_L0_C DP_L0_C 100DIFF 1

J1
DISPLAYPORT RECEPTACLE NORM NO STUFF
DP_PWR
C12 .1UF 50V 10% X7R 0603 NO STUFF
21 SHIELD5 23 SHIELD4 25
PWR 20 PWR_RET 19
18 HPD
17 AUXN 15 AUXP
GND 16 GND 14 MODE 13
GND 11 GND 8 GND 5 GND 2
12 LANE 3N 10 LANE 3P 9 LANE 2N 7 LANE 2P 6 LANE 1N 4 LANE 1P 3 LANE 0N 1 LANE 0P
SHIELD3 22 SHIELD2 24 SHIELD1 26
R15 100K 1% 0402 NO STUFF DP_MODE
0 R1006 NO STUFF 5% 0402

1\2 2\2 DP_MODE DP_HPD
D3 RCLAMP0524 15KV/8KV DUAL NO STUFF
D3 RCLAMP0524 15KV/8KV DUAL NO STUFF
D2 RCLAMP0524 15KV/8KV DUAL NO STUFF
D2 RCLAMP0524 15KV/8KV DUAL NO STUFF
D1 RCLAMP0524 15KV/8KV DUAL NO STUFF
D1 RCLAMP0524 15KV/8KV DUAL NO STUFF
ESD
Place near DP Connector's Pins.

3V3_F LB5 BEAD_0603 NO STUFF DP_AVDD33 12MIL
C21 4.7UF 6.3V 10% X5R 0603 NO STUFF
C28 4.7UF 6.3V 10% X5R 0603 NO STUFF
C973 .1UF 16V 10% X5R 0402 NO STUFF
C980 .01UF 16V 10% X5R 0402 NO STUFF
C979 .01UF 16V 10% X5R 0402 NO STUFF
C978 .01UF 16V 10% X5R 0402 NO STUFF
C975 1000PF 16V 10% X7R 0402 NO STUFF
C981 1000PF 16V 10% X7R 0402 NO STUFF
GND

U3
ANX9802
TQFP_80
NO STUFF
2/2
41 45 49 53 57 61 AVDD33
31 VPP
12 30 75 DVDD33
1 16 26 35 72 DVDD18
PWRPAD
VREF 67
DP_VREF
C32 1UF 16V 10% X5R 0402 NO STUFF
R23 1K 1% 0402 NO STUFF
R24 1K 1% 0402 NO STUFF
2V5
AVSS 44 48 52 56 60 66
DVSS 4 18 27 36 69 79
ANX9802

3V3_F
C951 4.7UF 6.3V 10% X5R 0603 NO STUFF
C38 4.7UF 6.3V 10% X5R 0603 NO STUFF
C959 .1UF 16V 10% X5R 0402 NO STUFF
C976 .1UF 16V 10% X5R 0402 NO STUFF
C960 .01UF 16V 10% X5R 0402 NO STUFF
C964 .01UF 16V 10% X5R 0402 NO STUFF
GND

1V8 LB6 BEAD_0603 NO STUFF DP_DVDD18 12MIL
C56 4.7UF 6.3V 10% X5R 0603 NO STUFF
C44 4.7UF 6.3V 10% X5R 0603 NO STUFF
C37 1UF 6.3V 10% X5R 0402 NO STUFF
C954 .1UF 16V 10% X5R 0402 NO STUFF
C49 .1UF 16V 10% X5R 0402 NO STUFF
C53 .01UF 16V 10% X5R 0402 NO STUFF
C45 .01UF 16V 10% X5R 0402 NO STUFF
GND

12V_PEX6_F
Q1000 BSS138 SOT23_1G1D1S NO STUFF DP_CABLE_CEC_L
LB1000 BEAD_0402 240R@100MHz DP_CABLE_CEC NO STUFF
3V3_F
R1005 27K 5% 0402 NO STUFF DP_CEC
D1010 BAV99 SOT23 100V 100MA NO STUFF
STUFF ONLY IF using ANX9805

NETNAME	DIFF_PAIR	NV_IMPEDANCE	NV_CRIT_NET
BI DP_AUX*	DP_AUX	100DIFF	1
BI DP_AUX	DP_AUX	100DIFF	1
BI DP_AUX_C*	DP_AUX_C	100DIFF	1
BI DP_AUX_C	DP_AUX_C	100DIFF	1
BI DP_AUX_Q*	DP_AUX_Q	100DIFF	1
BI DP_AUX_Q	DP_AUX_Q	100DIFF	1
BI DP_L3*	DP_L3	100DIFF	1
BI DP_L3	DP_L3	100DIFF	1
BI DP_L2*	DP_L2	100DIFF	1
BI DP_L2	DP_L2	100DIFF	1
BI DP_L1*	DP_L1	100DIFF	1
BI DP_L1	DP_L1	100DIFF	1
BI DP_L0*	DP_L0	100DIFF	1
BI DP_L0	DP_L0	100DIFF	1

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Display Port

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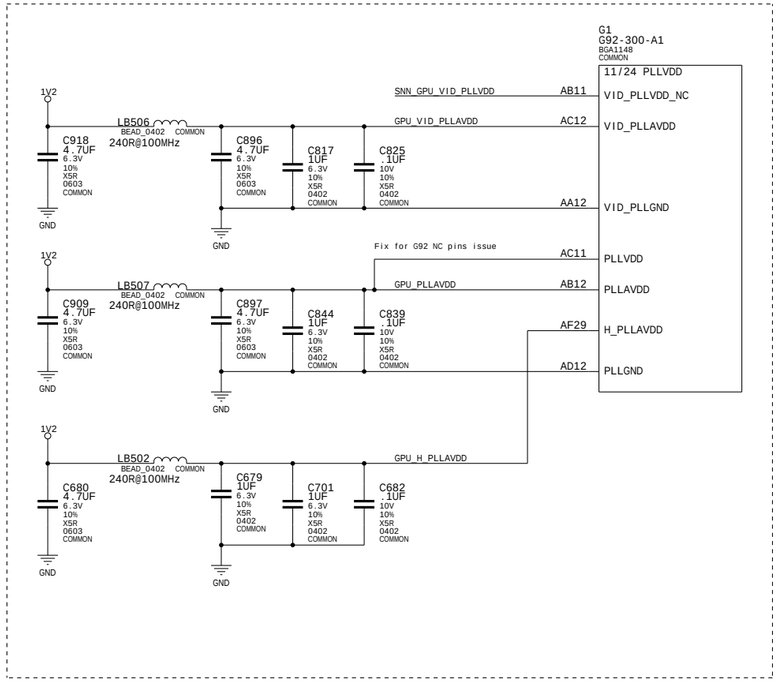
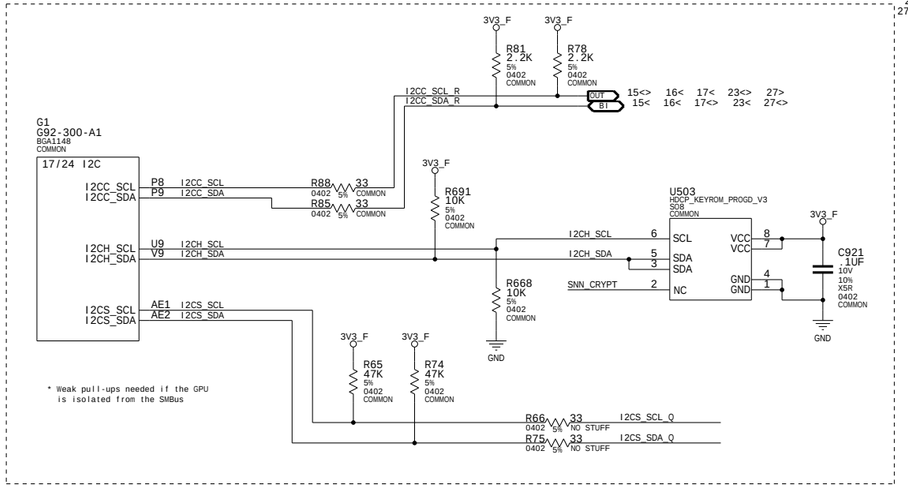
Page16: MISC: GPIO, I2C, BIOS, PLL, and XTAL

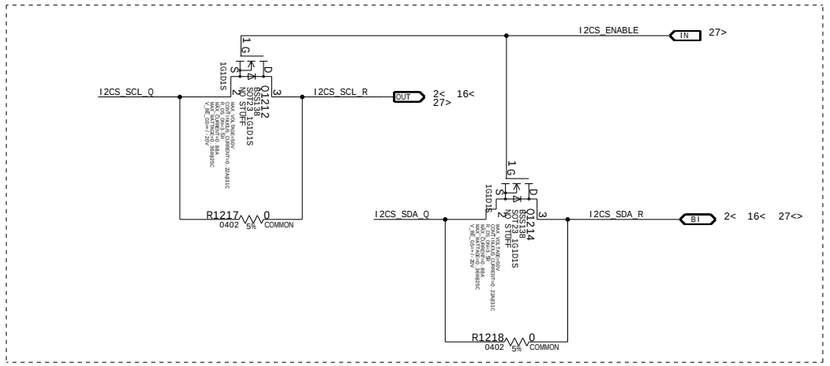
PLLVDD/VID_PLLVDD



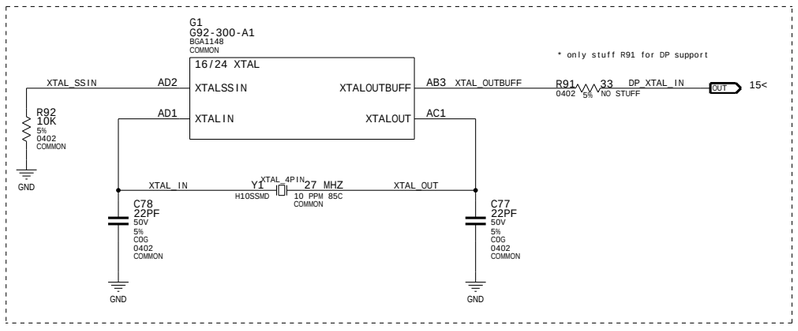
I2CC / I2CH(+ HDCP ROM) / I2CS



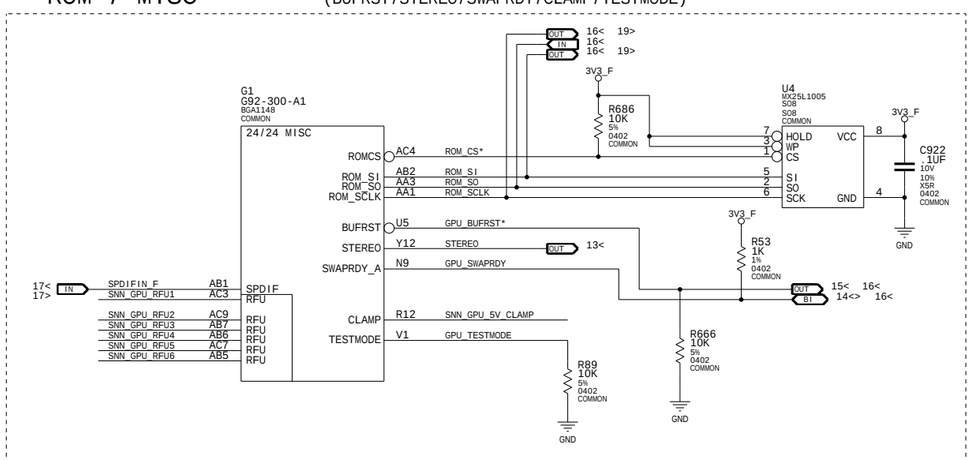
I2CS isolation for Hybrid Power



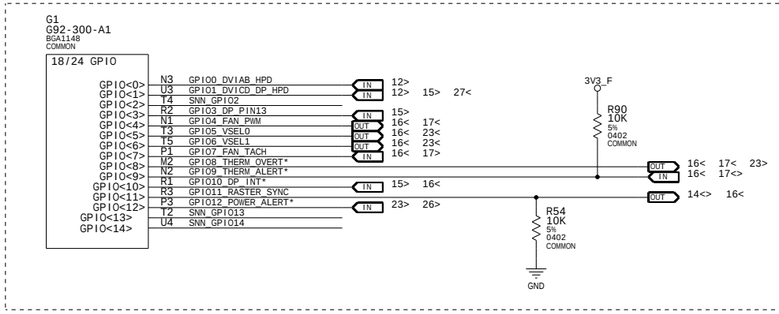
XTAL



ROM / MISC (BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)



GPIO



GPIO Assignment Table

GPIO	I/O	Function
0	IN	DVI Hotplug Detect South
1	IN	DVI or DP Hotplug Detect Mid
2	IN	Framelock Interrupt
3	BI	Framelock GPIO/DP Dongle Detect
4	OUT	Fan PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fan Tach Input
8	OUT	THERM_OVERT*
9	IN	THERM_ALERT*
10	IN	DisplayPort Interrupt
11	OUT	RASTER (SLI) SYNC
12	IN	POWER_ALERT*
13	OUT	DP I2C Keeper
14	IN	Framelock Sync

MISC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
I2CC_SCL	3	50OHM	
I2CC_SDA	3	50OHM	
I2CC_SCL_R	3	50OHM	
I2CC_SDA_R	3	50OHM	
I2CH_SCL	3	50OHM	
I2CH_SDA	3	50OHM	
I2CS_SCL	3	50OHM	
I2CS_SDA	3	50OHM	
I2CS_SCL_R	3	50OHM	
I2CS_SDA_R	3	50OHM	
ROM_CS*	3	50OHM	
ROM_SI	3	50OHM	
ROM_SO	3	50OHM	
ROM_SCLK	3	50OHM	
GPU_BUFRST*	3	50OHM	
GPU_STEREO	3	50OHM	
GPU_SWAPRDY	3	50OHM	
GPU_TESTMODE	3	50OHM	
GPIO0_DVI_A_HPD	3	50OHM	
GPIO1_DVI_C_HPD	3	50OHM	
GPIO4_FAN_PWM	3	50OHM	
GPIO5_VSEL0	3	50OHM	
GPIO6_VSEL1	3	50OHM	
GPIO7_FAN_TACH	3	50OHM	
GPIO8_THERM_OVERT*	3	50OHM	
GPIO9_THERM_ALERT*	3	50OHM	
GPIO10_DP_INT*	3	50OHM	
GPIO11_RASTER_SYNC	3	50OHM	
GPIO12_POWER_ALERT	3	50OHM	
GPIO13_DP_KEEP	3	50OHM	
XTAL_SSIN	1	50OHM	
XTAL_IN	1	50OHM	
XTAL_OUT	1	50OHM	
XTAL_OUTBUFF	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
GPU_VID_PLLVDD	1.2V	0.05A	12MIL
GPU_VID_PLLAVDD	1.2V	0.05A	12MIL
GPU_PLLVDD	1.2V	0.05A	12MIL
GPU_PLLAVDD	1.2V	0.05A	12MIL
GPU_H_PLLAVDD	1.2V	0.05A	12MIL

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	MISC: GPIO, I2C, BIOS, PLL, and XTAL

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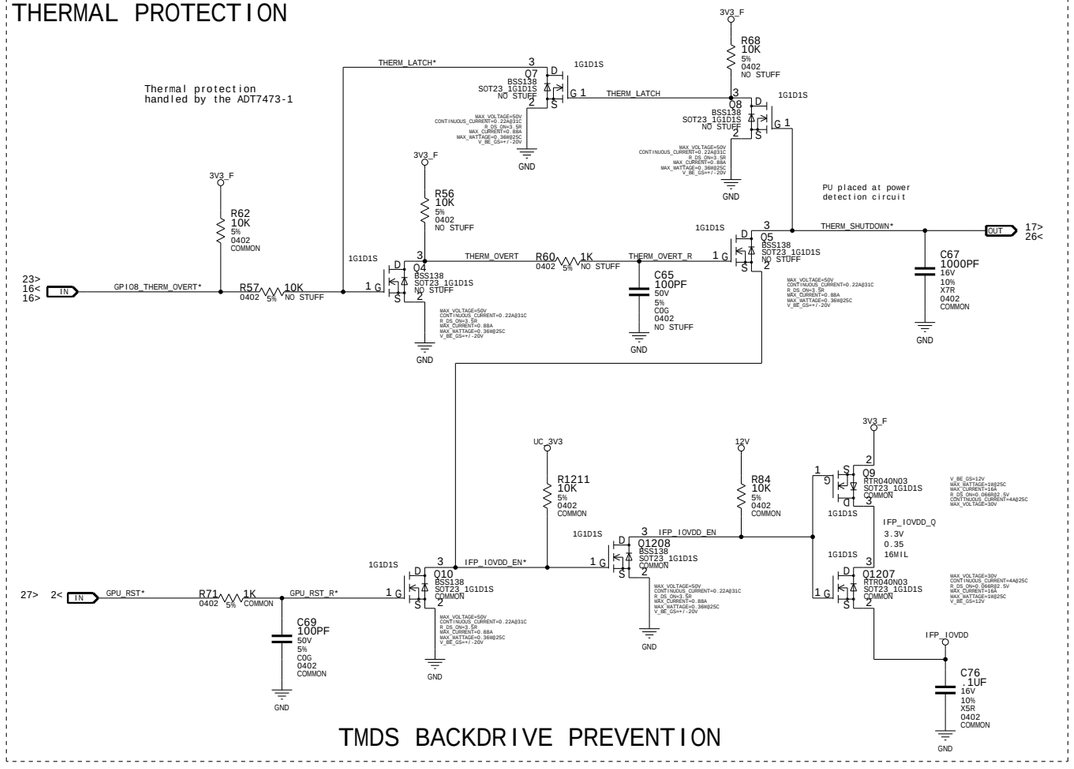
Page17: Thermal Control/Protection and SPDIF Input

THERMAL PROTECTION



TMDS BACKDRIVE PREVENTION

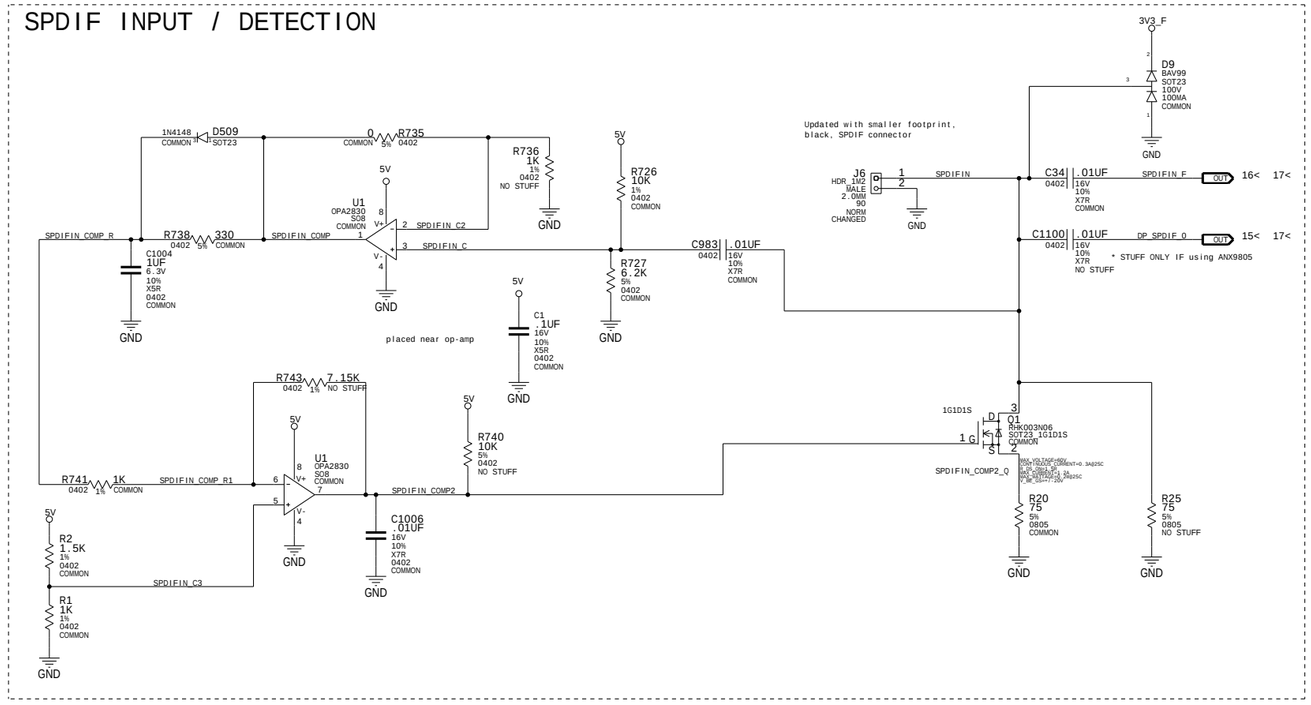
Stuffing posibilities for thermal control and protection:

2) ADT7473 is COMMON
GPIO4 is not used.
GPIO7 is the tach input from the fan
GPIO9 is the thermal alert for GPU slowdown.
With a newer version of the ADT chip, PWM2 can optionally be used for shutdown

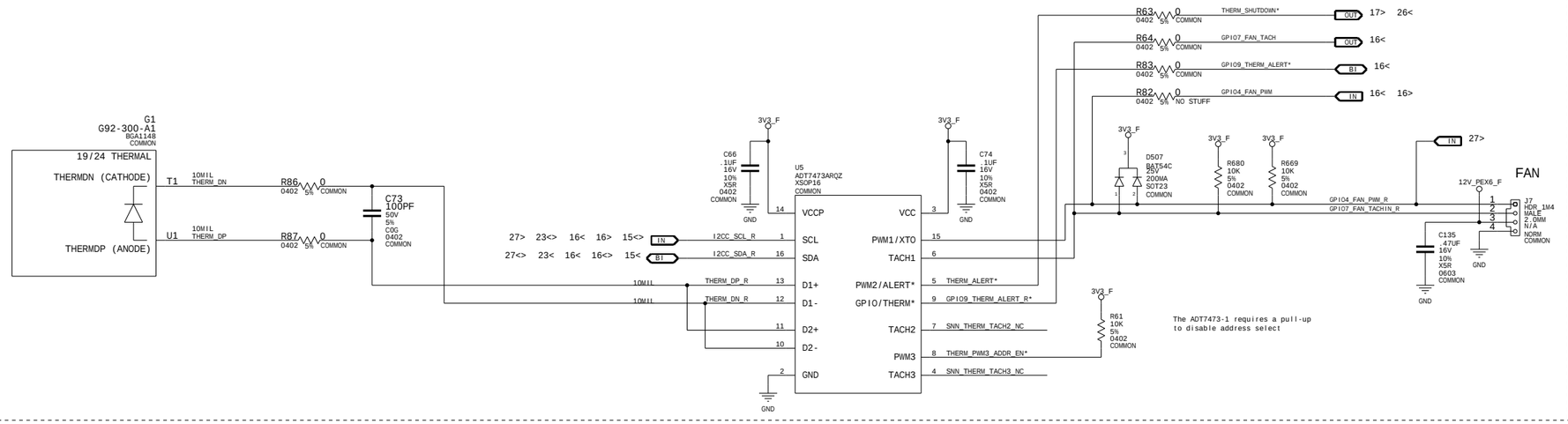
NET	IMPEDANCE	NV_CRITICAL_NET	MIN_LINE_WIDTH
SPDIFIN	50OHM	1	
SPDIFIN_C	50OHM	1	
SPDIFIN_C2	50OHM	1	
SPDIFIN_COMP	50OHM	1	
SPDIFIN_COMP_R	50OHM	1	
SPDIFIN_COMP_R1	50OHM	1	
SPDIFIN_C3	50OHM	1	
SPDIFIN_COMP2	50OHM	1	
SPDIFIN_COMP2_Q	50OHM	1	
SPDIFIN_F	50OHM	1	
DP_SPDIF_0	50OHM	1	

17> 16<
17> 15<

SPDIF INPUT / DETECTION



THERMAL CONTROL



The FAN connector needs to move
as follows for mechanical / ID support:
* move -43mils in Y
* move +33mils in X

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Thermal Control/Protection and SPDIF Input

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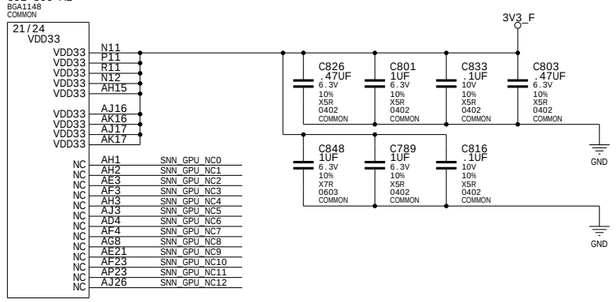
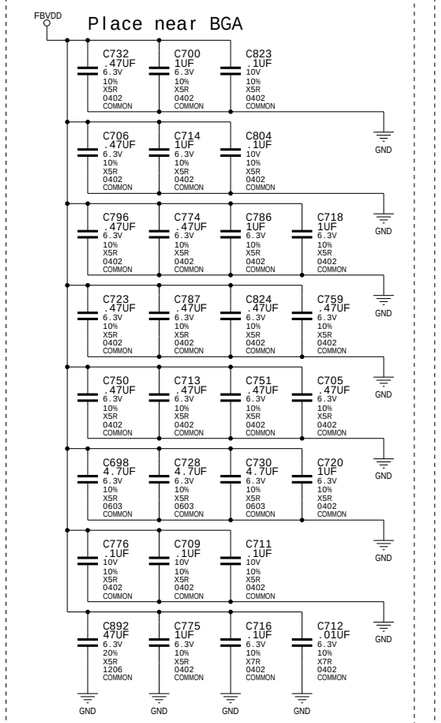
Page18: Power/GND and Decoupling

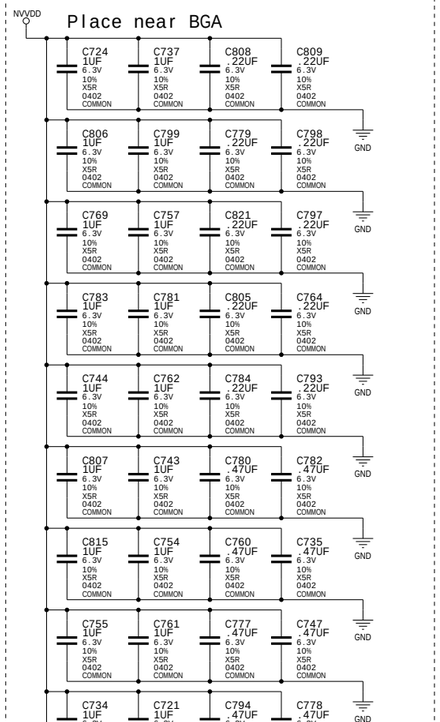
VDD33



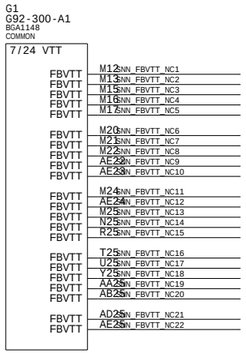
FBVDDQ

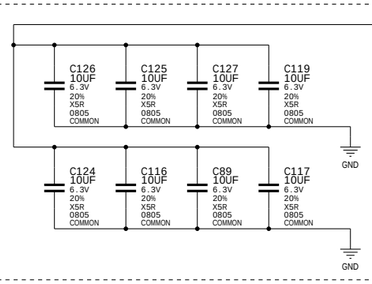


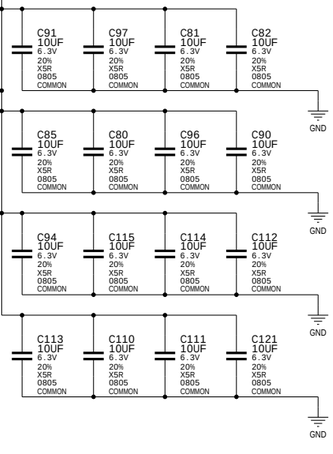
NVVDD

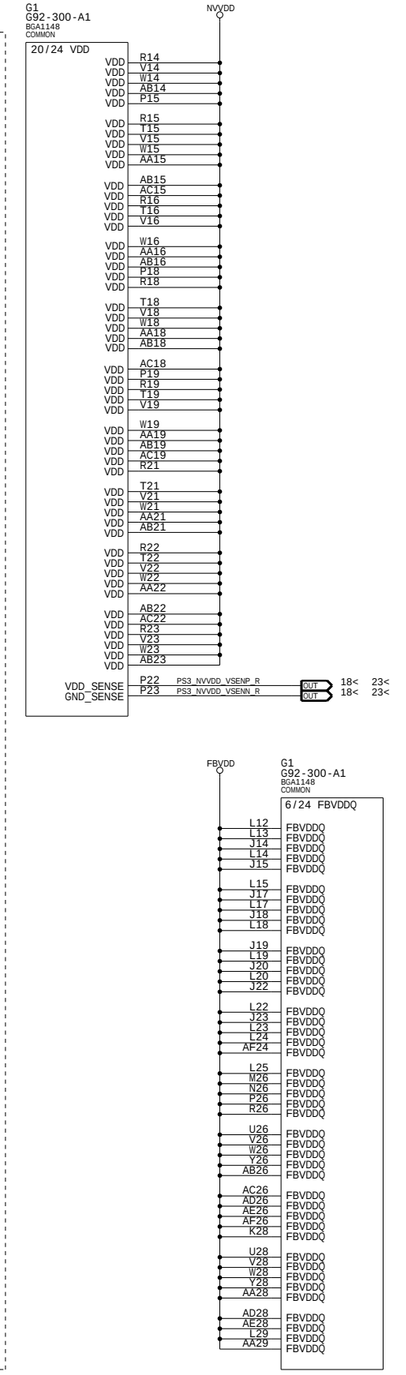


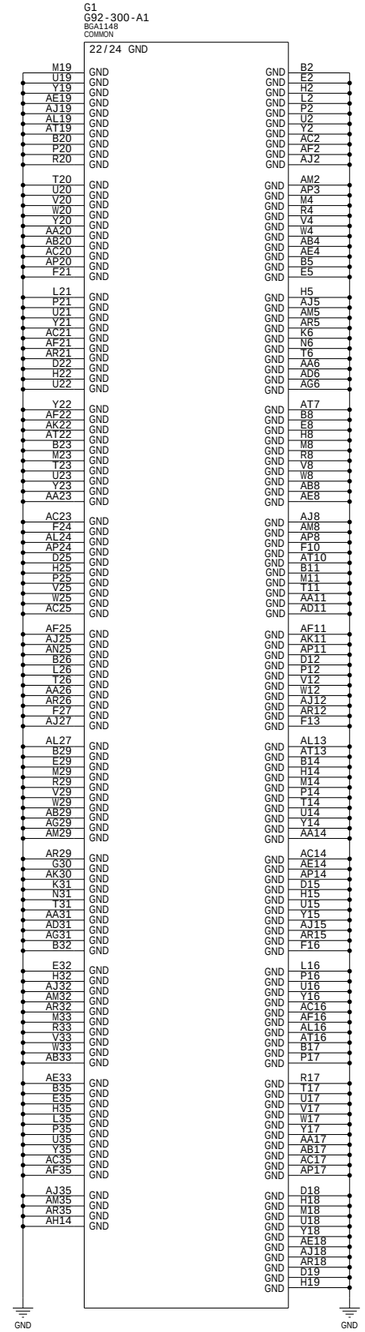
FBVTT











NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
23< 18> IN PS3_NVVDD_VSENP_R	1	80DIFF	NVVDD_SENSE
23< 18> IN PS3_NVVDD_VSENN_R	1	80DIFF	NVVDD_SENSE

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Power/GND and Decoupling

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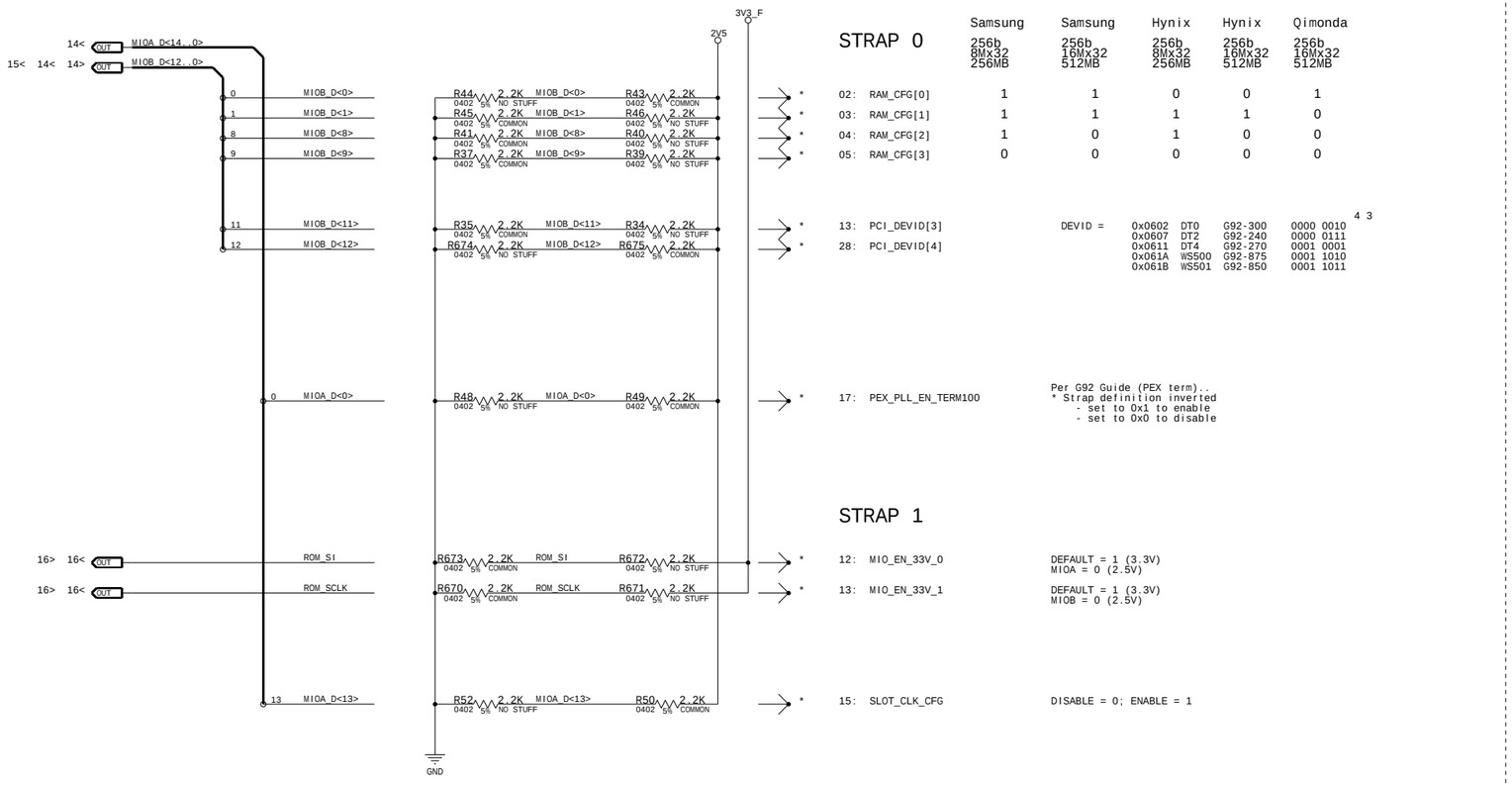
Page19: Configuration Straps and Mechanical

STRAPS



STRAP 0

		Samsung	Samsung	Hynix	Hynix	Qimonda
		256b 8Mx32 256MB	256b 16Mx32 512MB	256b 8Mx32 256MB	256b 16Mx32 512MB	256b 16Mx32 512MB
02:	RAM_CFG[0]	1	1	0	0	1
03:	RAM_CFG[1]	1	1	1	1	0
04:	RAM_CFG[2]	1	0	1	0	0
05:	RAM_CFG[3]	0	0	0	0	0

13:	PCI_DEVID[3]	DEVID =	0x0602	DT0	G92-300	0000 0010
28:	PCI_DEVID[4]		0x0607	DT2	G92-240	0000 0111
			0x0611	DT4	G92-270	0001 0001
			0x061A	WS500	G92-875	0001 1010
			0x061B	WS501	G92-850	0001 1011

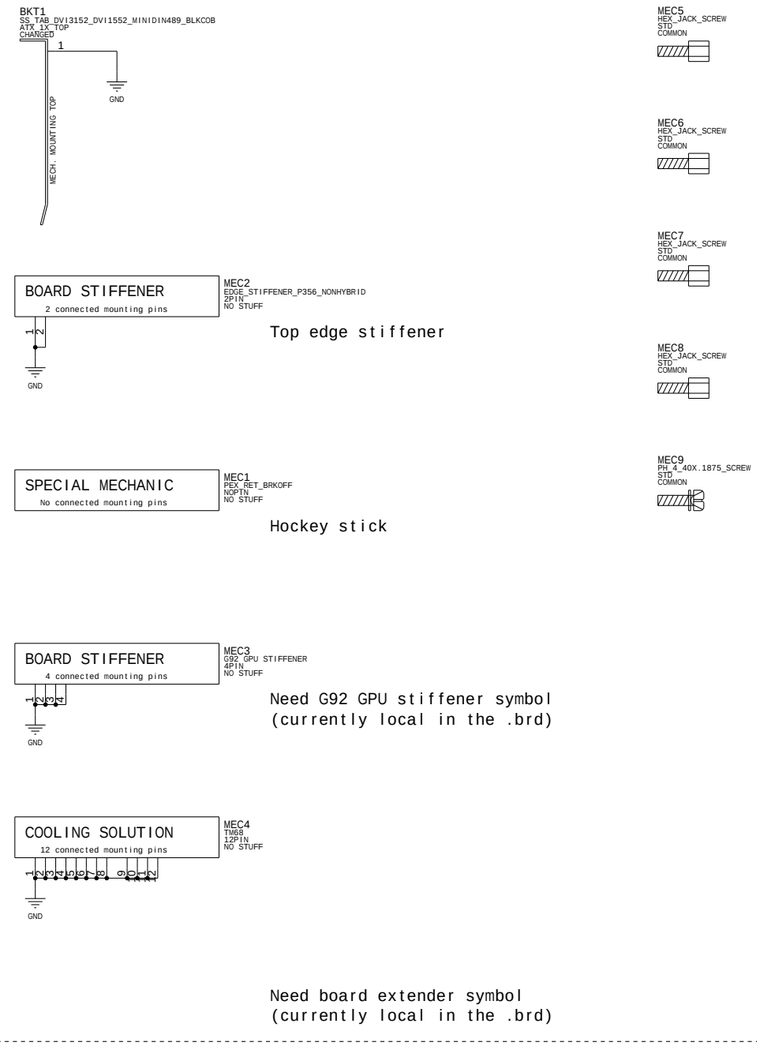
4 3

17: PEX_PLL_EN_TERM100 — Per G92 Guide (PEX term).. * Strap definition inverted - set to 0x1 to enable - set to 0x0 to disable

STRAP 1

12:	MIO_EN_33V_0	DEFAULT = 1 (3.3V) MIOA = 0 (2.5V)
13:	MIO_EN_33V_1	DEFAULT = 1 (3.3V) MIOB = 0 (2.5V)
15:	SLOT_CLK_CFG	DISABLE = 0; ENABLE = 1

MECHANICAL



ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Configuration Straps and Mechanical

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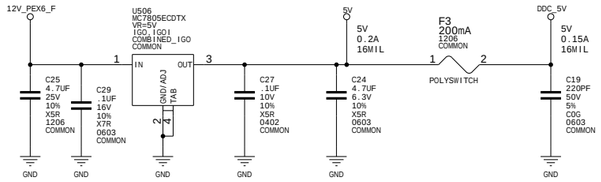
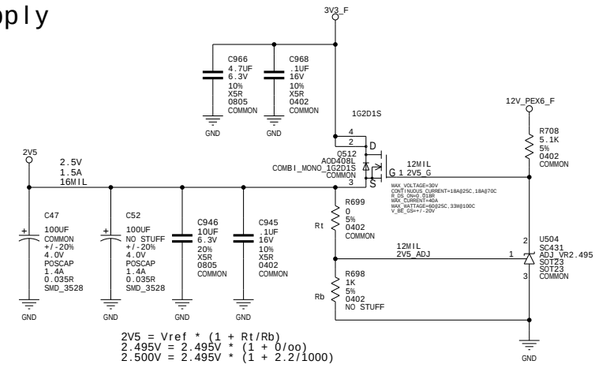
Page20: Power Supply: 5V, STEREO_5V, 2V5, DP_PWR

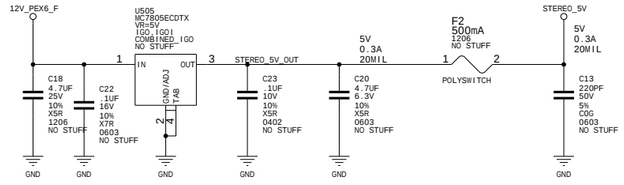
5V and DDC5V Supply



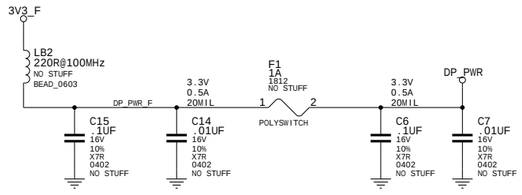
2V5 Supply



5V STEREO Supply



DP_PWR



Power for DP dongle support.

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Power Supply: 5V, STEREO_5V, 2V5, DP_PWR

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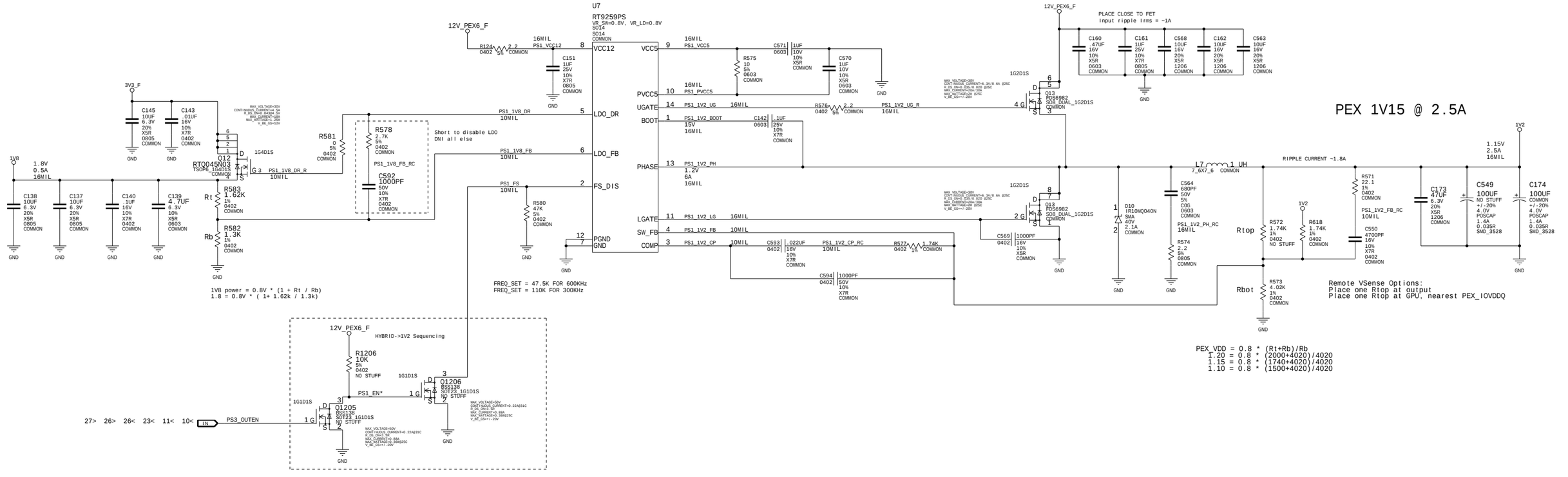
Page21: Power Supply: 1V2, 1V8



ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Power Supply: 1V2, 1V8

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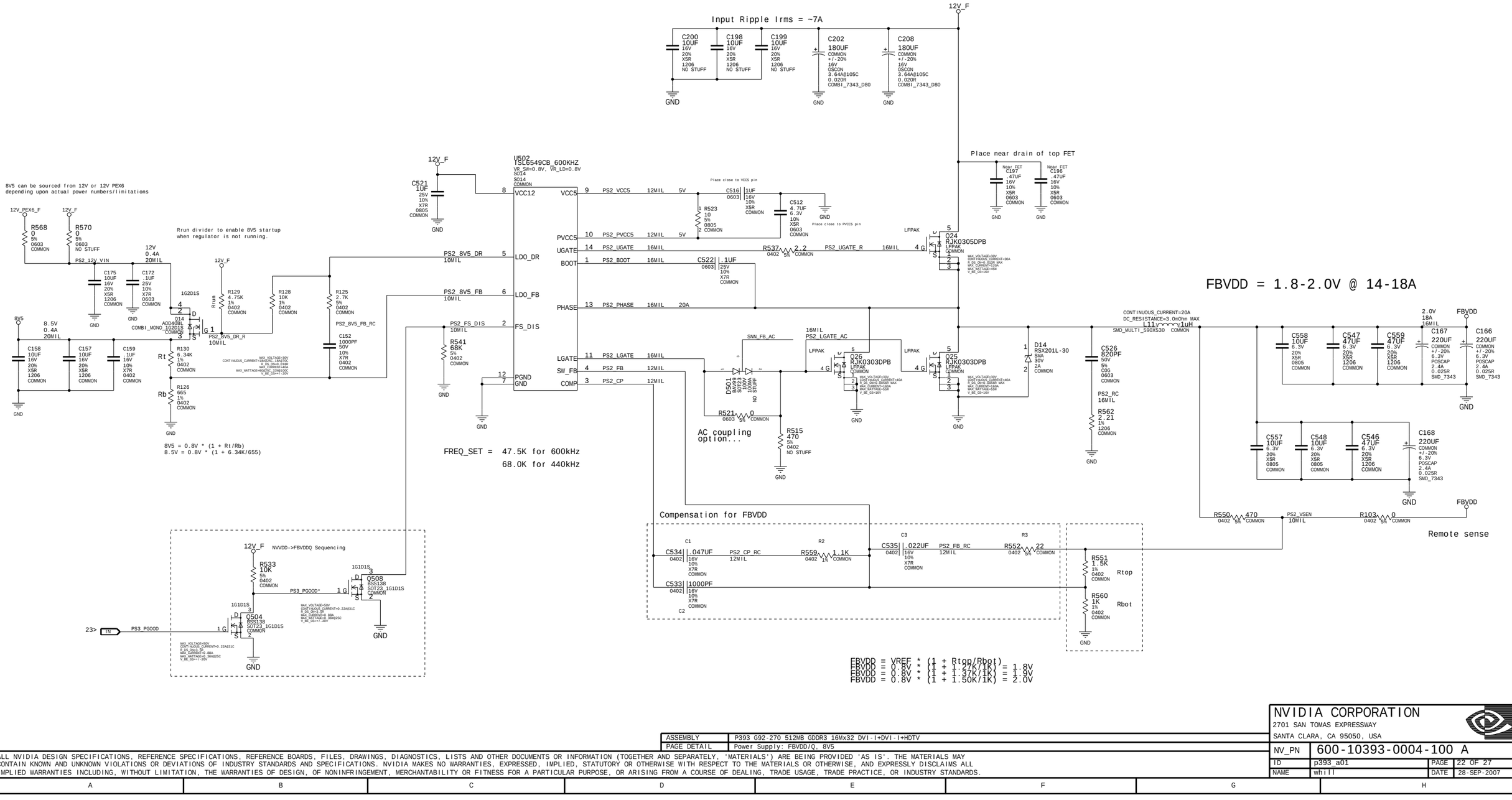
Page22: Combined FBVDD/VDDQ, 8V5



ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Power Supply: FBVDD/Q, 8V5

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Page23: Power Supply: NVVDD Regulator

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Power Supply: NVVDD Regulator

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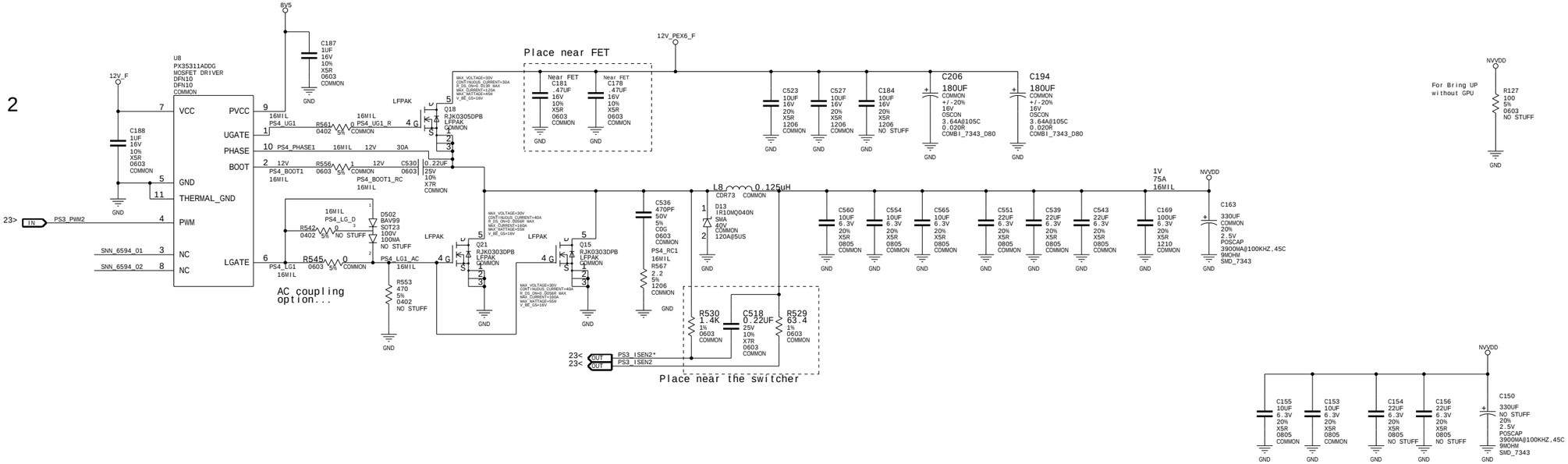
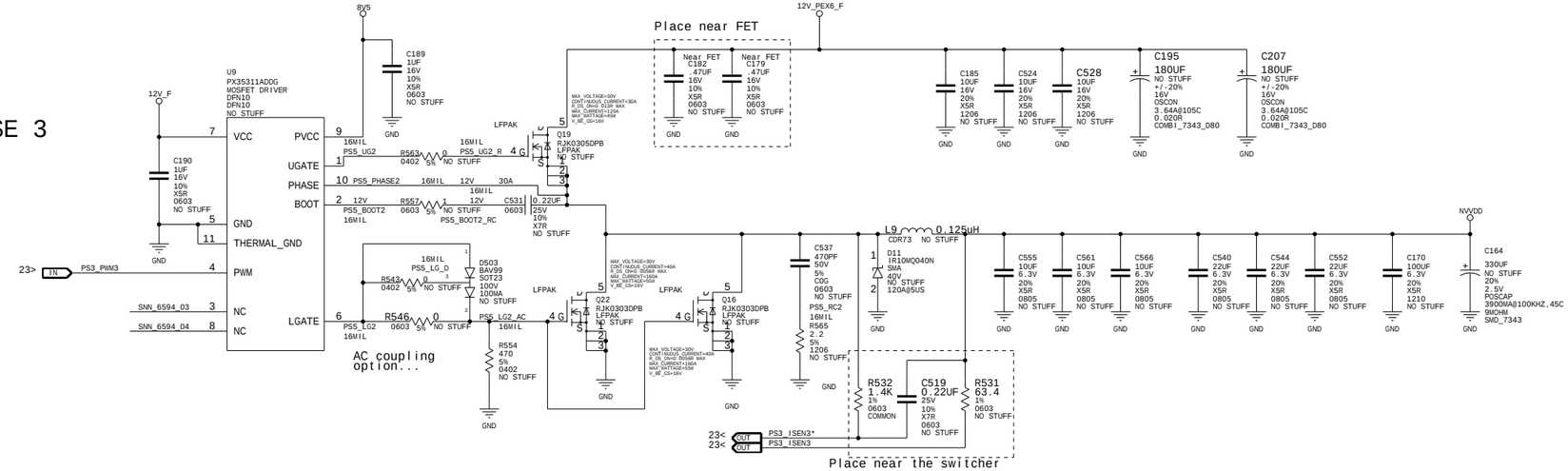
Page24: Power Supply: NVVDD Phase 2, 3

PHASE 2



PHASE 3



ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Power Supply: NVVDD Phase 1 & 2

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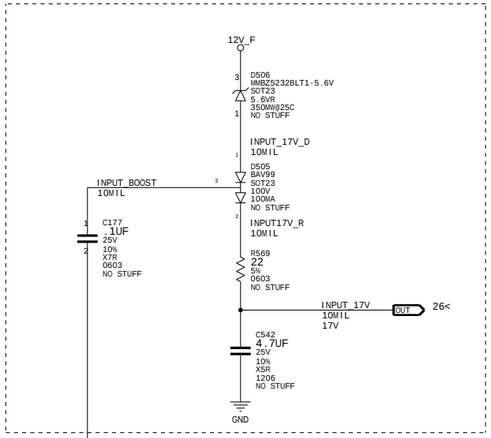
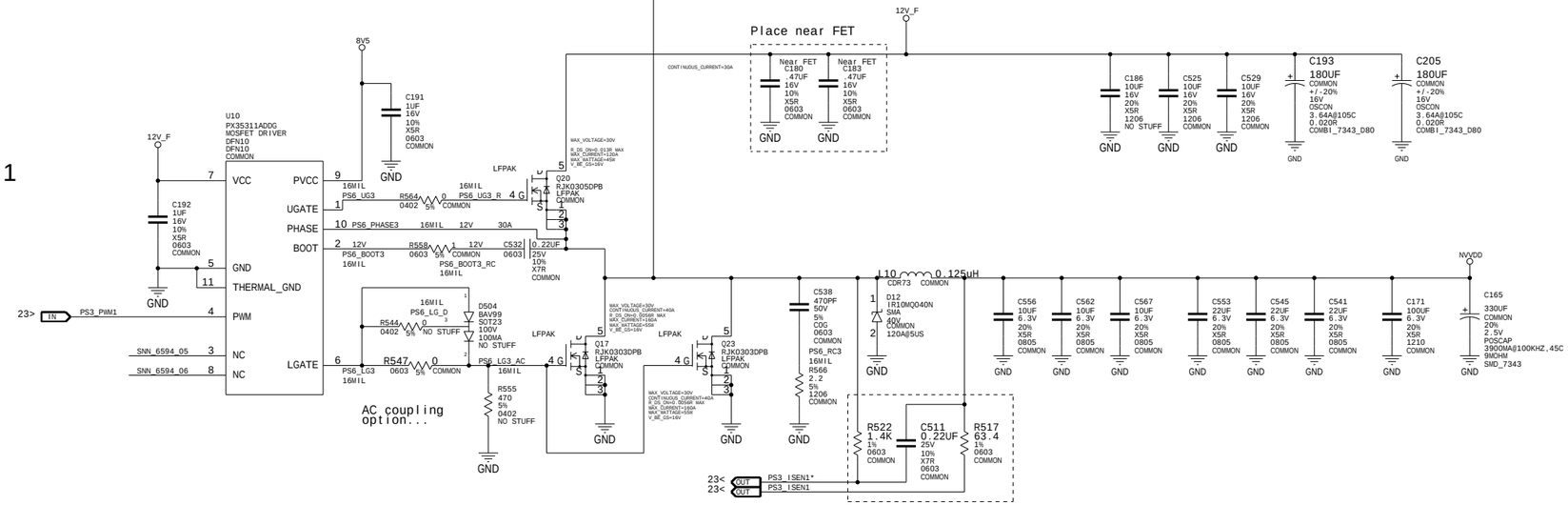
Page25: Power Supply: NVVDD Phase 1

PHASE 1

Boost from 12V pex to create 17V





ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Power Supply: NVVDD Phase 3

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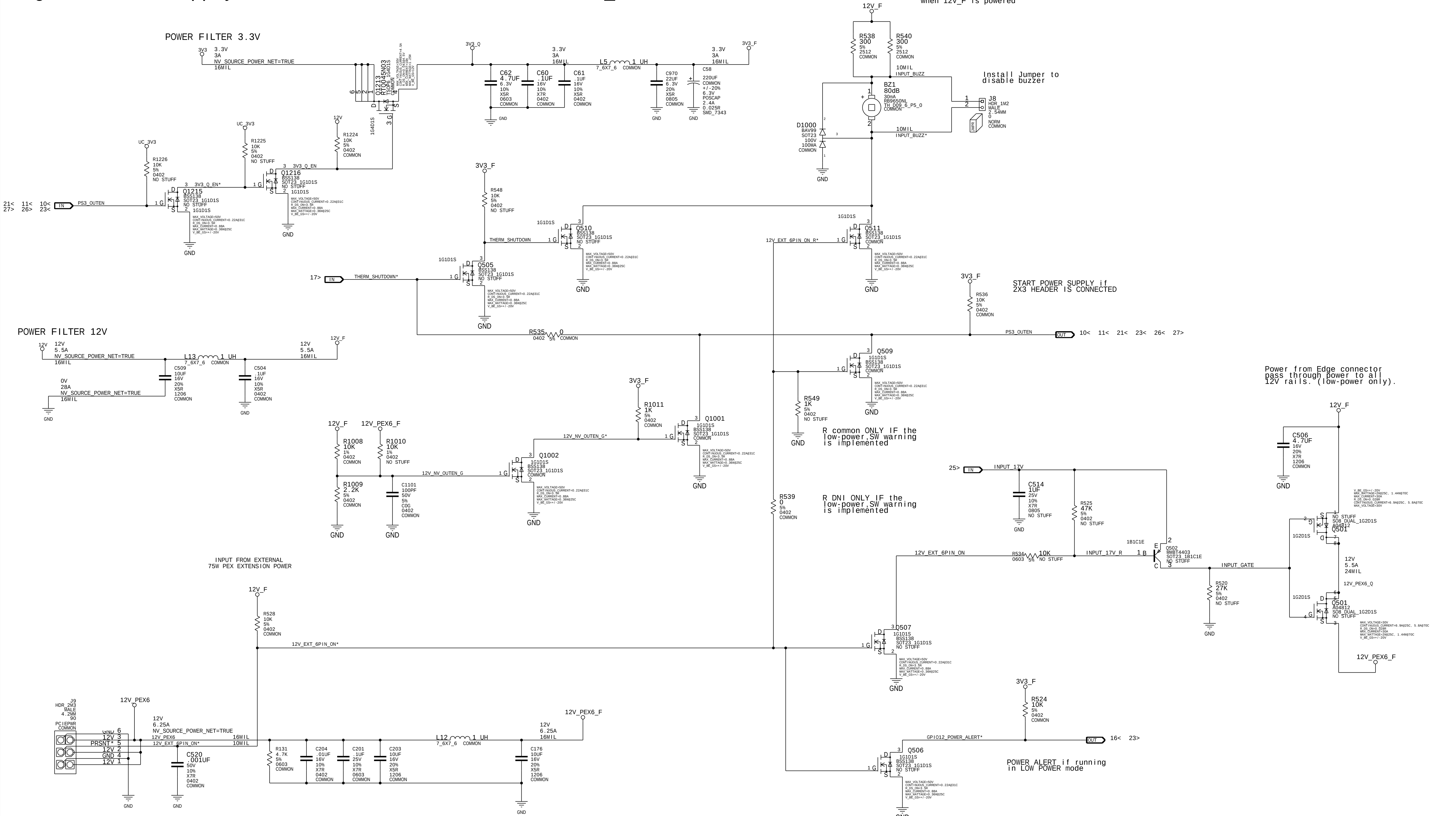
Page26: Power Supply: Filter/Detection of 3V3,12V,12V_PEX



ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Power Supply: Filter/Detection of 3V3, 12V, 12V_PEX6

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Page27: Power Supply: Hybrid Power

Per Datasheet:

Vf = 400mV at 10mA
Vf = 500mV at 30mA
* expected current < 2mA

3V3_AUX
3V3_F
D1200 BAT54C 25V 200MA SOT23 NO STUFF
R1221 0 5% 0402 COMMON
C1200 1UF 6.3V 10% X5R 0402 COMMON
C1201 .1UF 16V 10% X7R 0402 COMMON
UC_3V3
3.0V 0.01A 10MIL
GND

U1200
HYBRID_PIC16F690
XSOP20
NO STUFF
PIC16F690

1	VDD		
2	PEX_REFCLK_ENABLE		
3	IICC_SCL	I2CC_SCL_R	
17	IICC_SDA	I2CC_SDA_R	
11	SMB_SCL	I2CS_SCL_R	
13	SMB_SDA	I2CS_SDA_R	
16	PCI_E_RESET*	PEX_RST*	
4	VPP	HYBRID_PRG_TP	
20	GND		
15	I2CA_SCL_UC	I2CA_SCL	I2CA_SCL_R OUT 10<
14	I2CA_SDA_UC	I2CA_SDA	I2CA_SDA_R BI 10<
8	I2CB_SCL_UC	I2CB_SCL	I2CB_SCL_R OUT 11<
9	I2CB_SDA_UC	I2CB_SDA	I2CB_SDA_R BI 11<
12	HYBRID_DP_HPD	HOTPLUG_DETECT_C	
10	HPLG_DET_D	HOTPLUG_DETECT_D	
19	HPLG_DET_E	HOTPLUG_DETECT_E	
18	HPLG_DET_F	HOTPLUG_DETECT_F	
6	GPU_RST*	GPU_RESET*	OUT 2< 17<
7	PS3_OUTEN	POWER_ENABLE	OUT 10< 11< 21< 23< 26< 26>
5	GPIO4_FAN_PWM_R	FAN_ENABLE	OUT 17<

R1201 68K 5% 0402 NO STUFF — 2< OUT PEX_REFCLK_EN
R1213 68K 5% 0402 NO STUFF — 23<> 17< 16< 16> 15<> OUT I2CC_SCL_R
R1214 68K 5% 0402 NO STUFF — 16< 16<> 23< 17<> 15< BI I2CC_SDA_R
16> 16< 2< OUT I2CS_SCL_R
16<> 16< 2< BI I2CS_SDA_R
R1220 68K 5% 0402 NO STUFF — 2> IN PEX_RST*
HYBRID_PRG_TP
PEX_RST* R1205 0 5% 0402 COMMON GPU_RST*

Weak pull-ups needed for I2CS:
* if SMBus is isolated from the GPU
* if MB does not support SMBus
* if MB does not support 3V3AUX

Stuff only to bypass the micro-controller

R1207 68K 5% 0402 NO STUFF
R1208 68K 5% 0402 NO STUFF
R1209 68K 5% 0402 NO STUFF
R1210 68K 5% 0402 NO STUFF
R1212 10K 5% 0402 NO STUFF — GND
Stuff 10K pull-down for DP skus

R1222 68K 5% 0402 NO STUFF
R1223 68K 5% 0402 NO STUFF
R1202 68K 5% 0402 NO STUFF
R1200 10K 5% 0402 NO STUFF — GND

Q01201 BSS138 SOT23_1G1D1S NO STUFF
Q01200 BSS138 SOT23_1G1D1S NO STUFF
Q01203 BSS138 SOT23_1G1D1S NO STUFF
Q01202 BSS138 SOT23_1G1D1S NO STUFF
1G1D1S
MAX_VOLTAGE=50V MAX_CONTINUOUS_CURRENT=0.22A@31C R_DS_ON=3.5Ω MAX_CURRENT=0.88A MAX_WATTAGE=0.36W@25C V_BE_GS=+/-20V

Inverts DP HPD signal polarity

R1203 68K 5% 0402 NO STUFF
Q01204 BSS138 SOT23_1G1D1S NO STUFF
GPIO1_DVICD_DP_HPD — IN 12> 15> 16<

Vcc section of I2C bus switch
See sheets 10-11 for switch sections

U1201 XSOP16_SECT IDTQS3VH126 COMMON
SNN_QS_NC1 1 NC
SNN_QS_NC2 9 NC
VCC 16
GND 8
C1202 1UF 16V 10% X7R 0402 COMMON

R1215 68K 5% 0402 NO STUFF
R1216 10K 5% 0402 NO STUFF
12V
I2CS_ENABLE OUT 16<
I2CS_ENABLE*
Q01210 BSS138 SOT23_1G1D1S NO STUFF
Q01211 BSS138 SOT23_1G1D1S NO STUFF
PS3_OUTEN

isolates SMBus to the GPU when in Hybrid mode

ASSEMBLY	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
PAGE DETAIL	Power Supply: Hybrid Power

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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