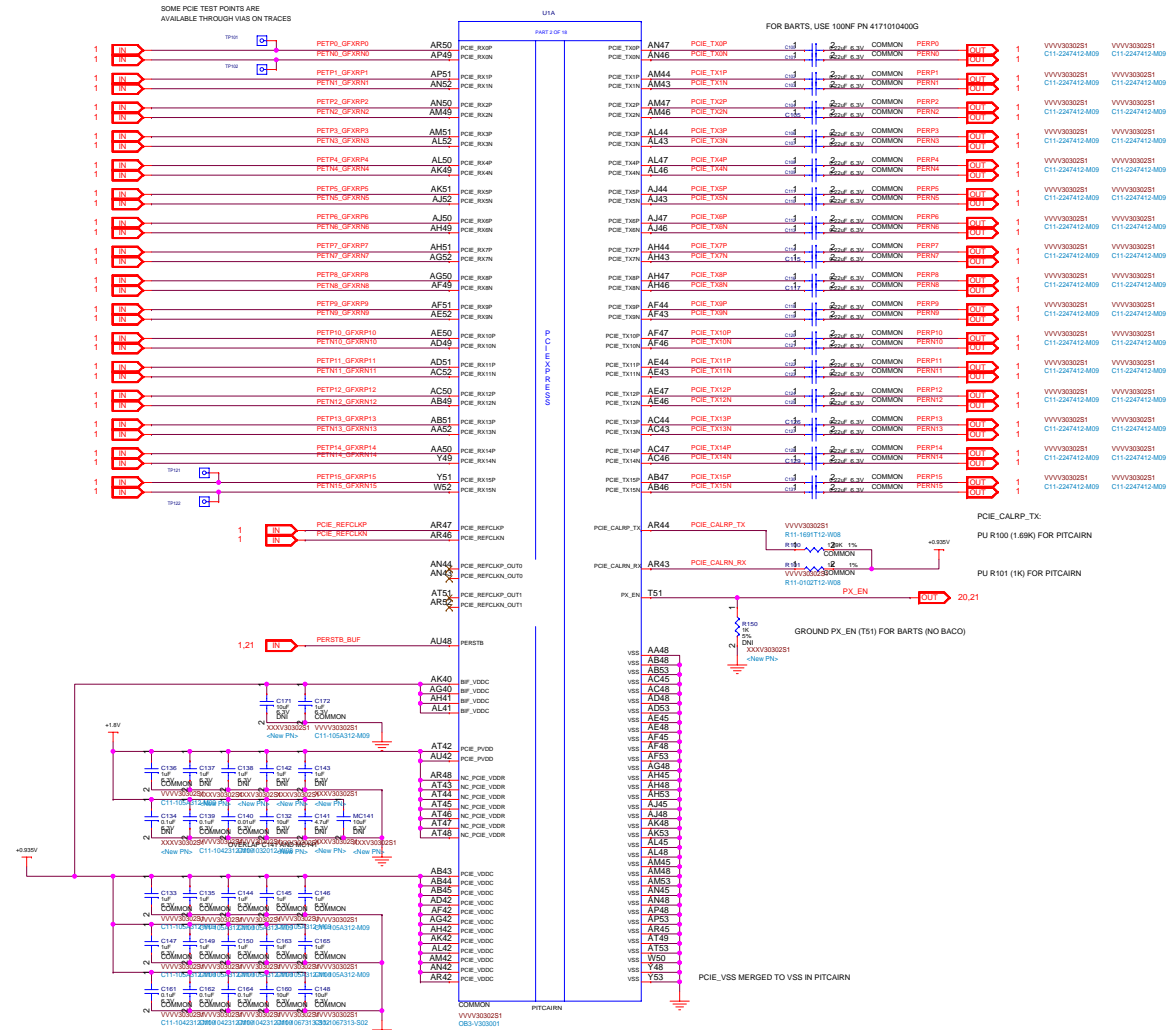
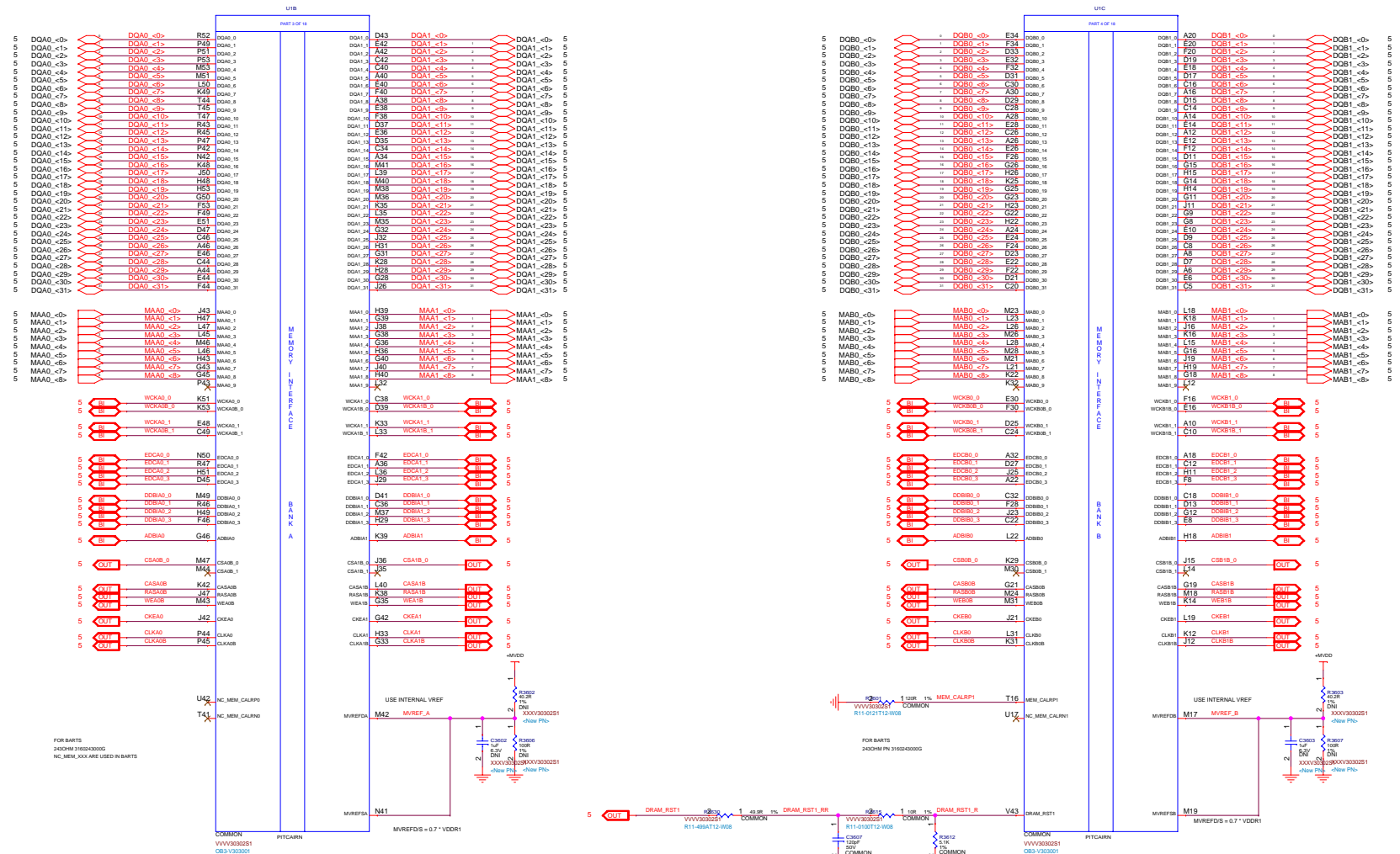


(2) CURACAO PCIE INTERFACE



(3) CURACAO MEM INTERFACE CH AB

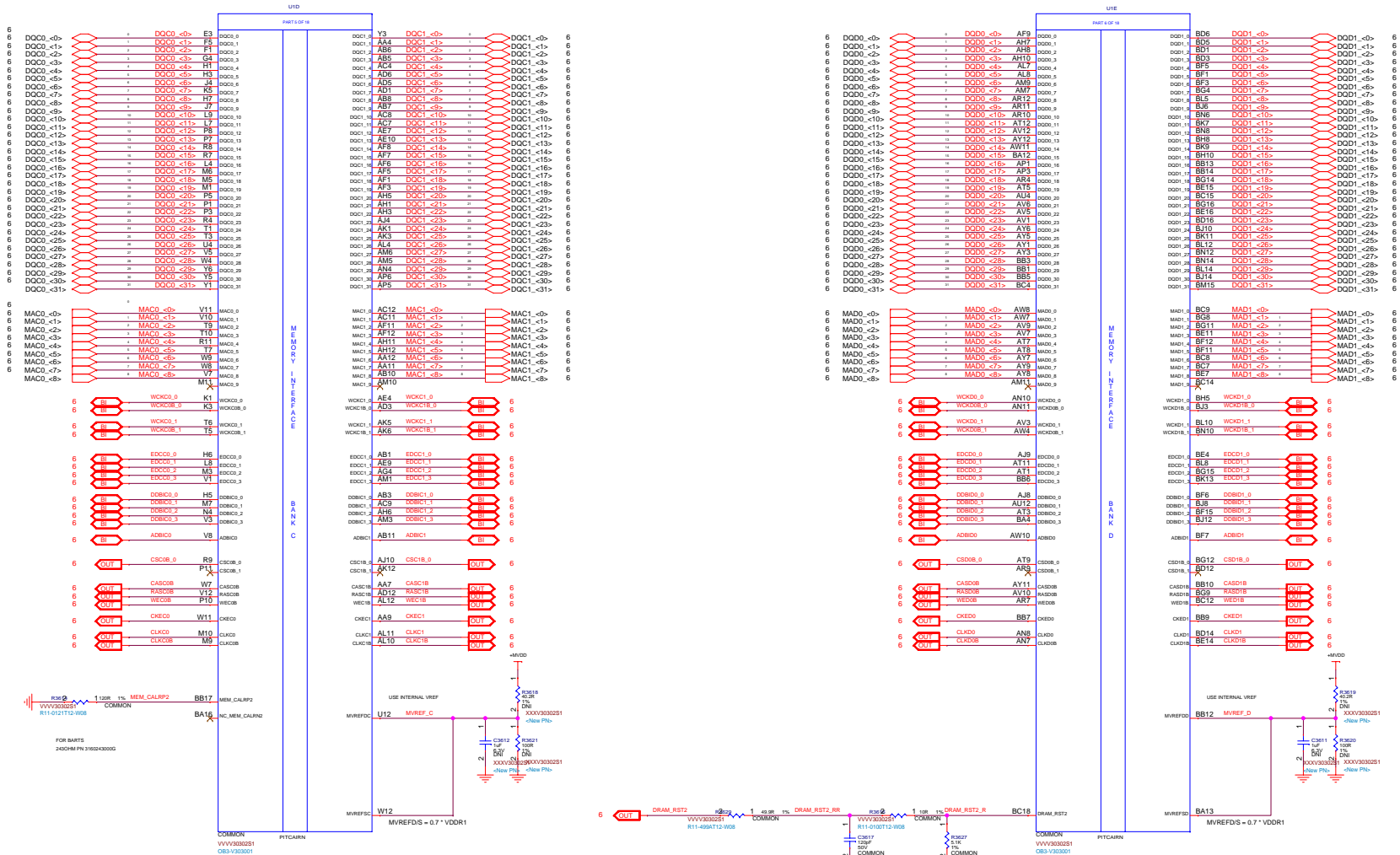


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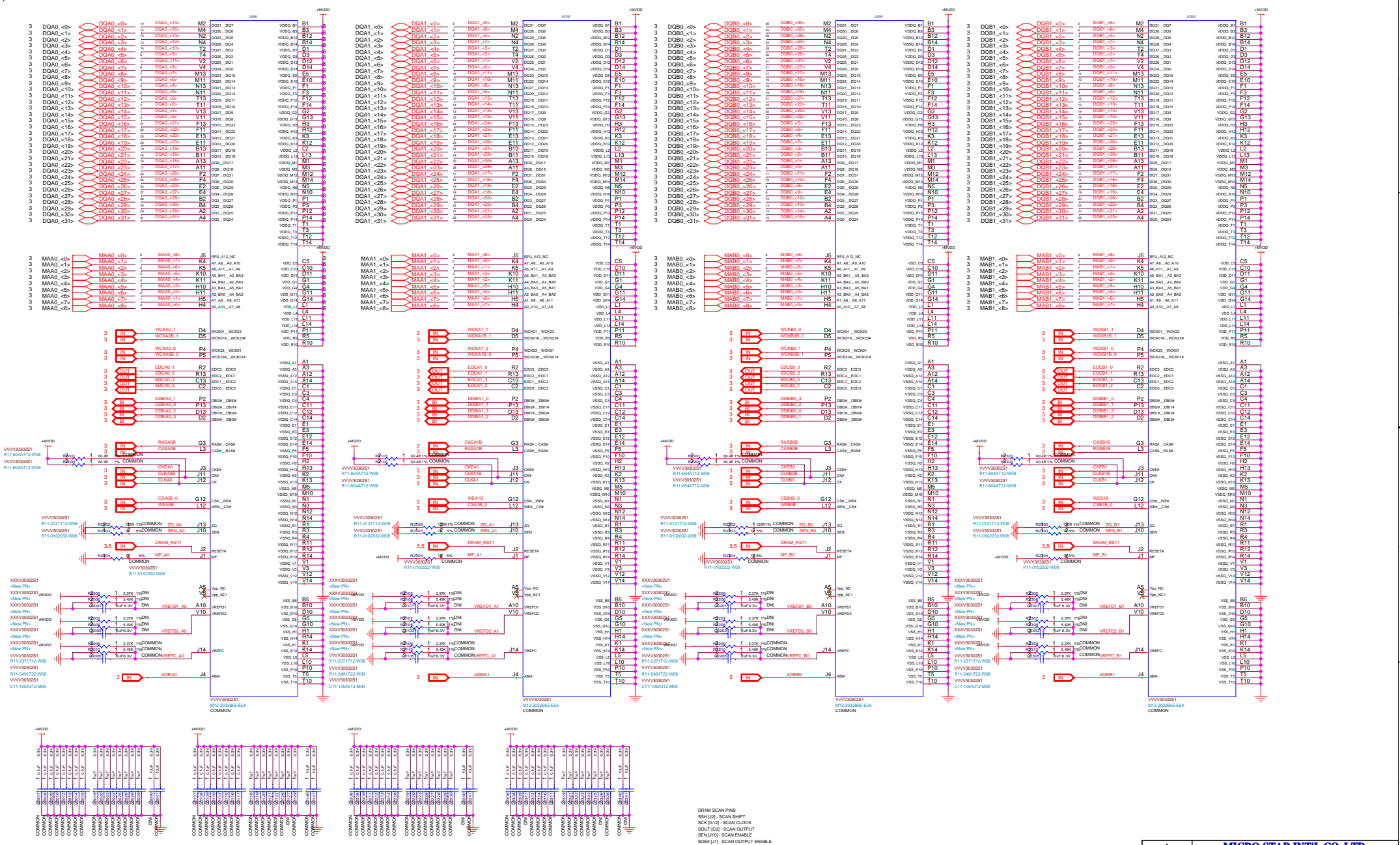
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Size Custom	Document Description 03 CURACAO PITCAIRN MEM CH AB	Rev 1.1
Date: Thursday, August 08, 2013		Sheet 3 of 24

(4) CURACAO MEM INTERFACE CH CD



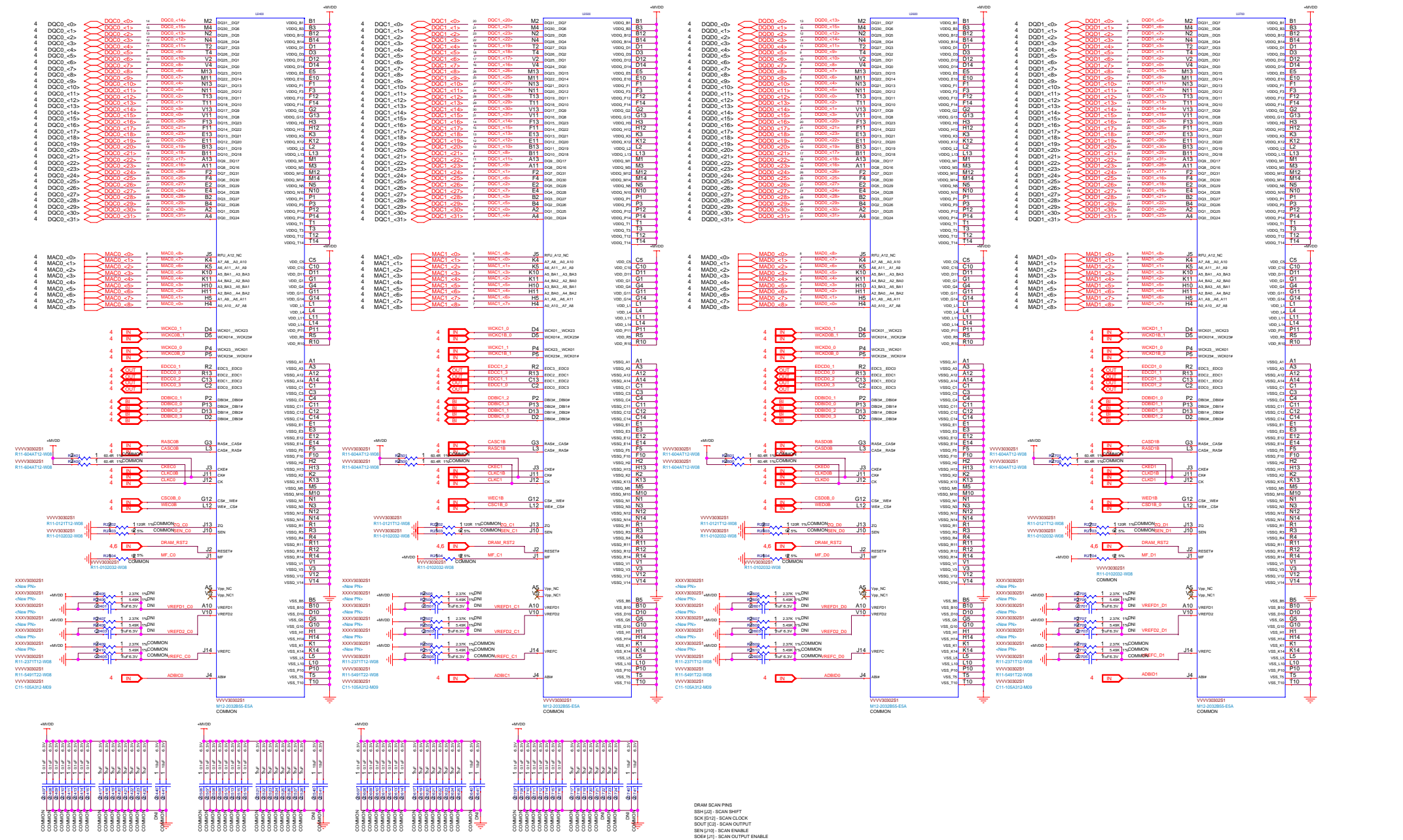
(5) GDDR5 MEM CH AB



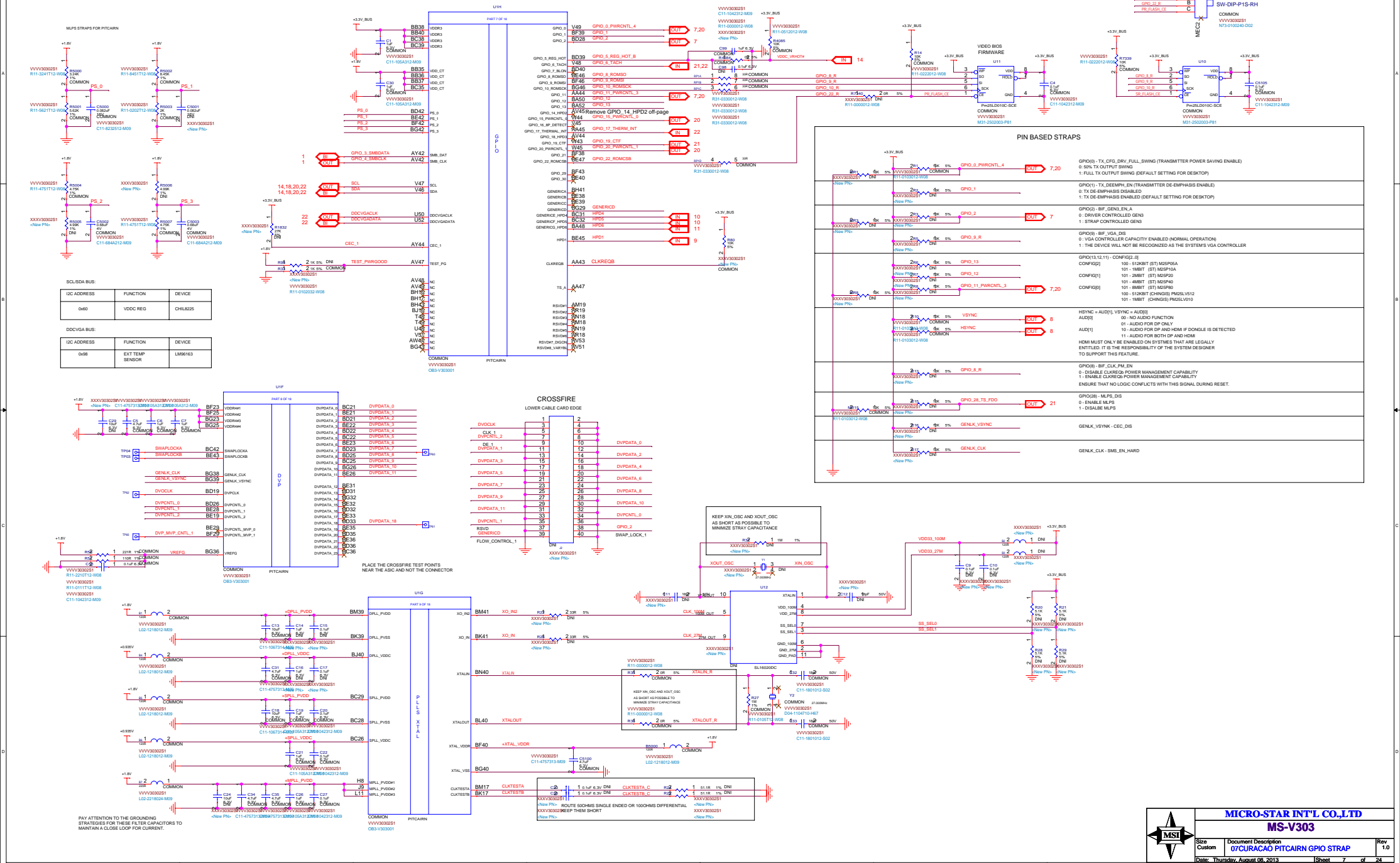
MICRO-STAR INT'L CO.,LTD
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Size Custom	Document Description 05 GDDR5 MEM CH AB	R
Date: Thursday, August 08, 2013	Sheet 5 of 24	

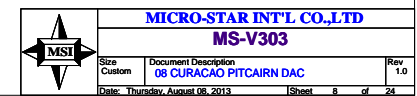
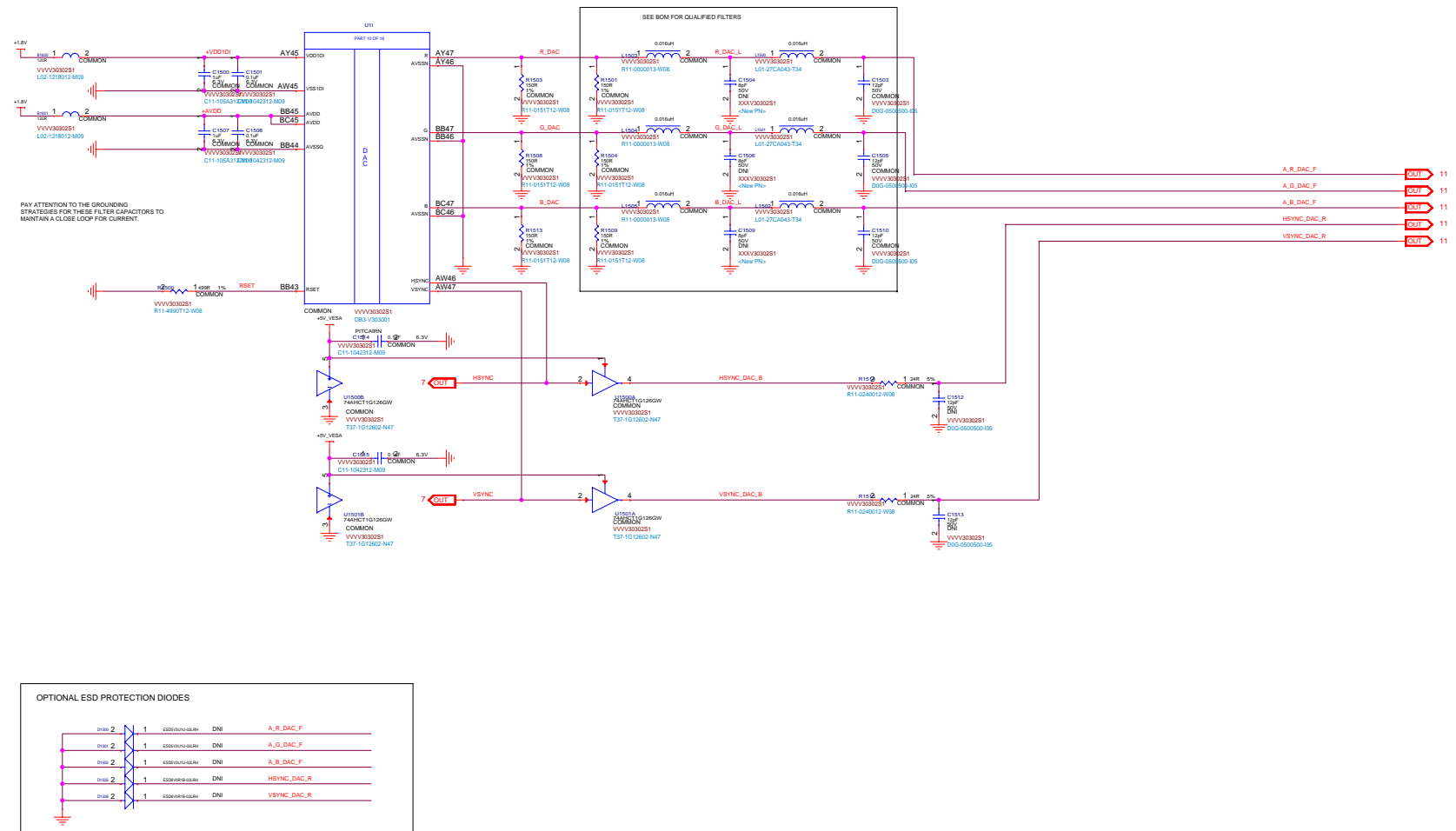
(6) GDDR5 MEM CH CD



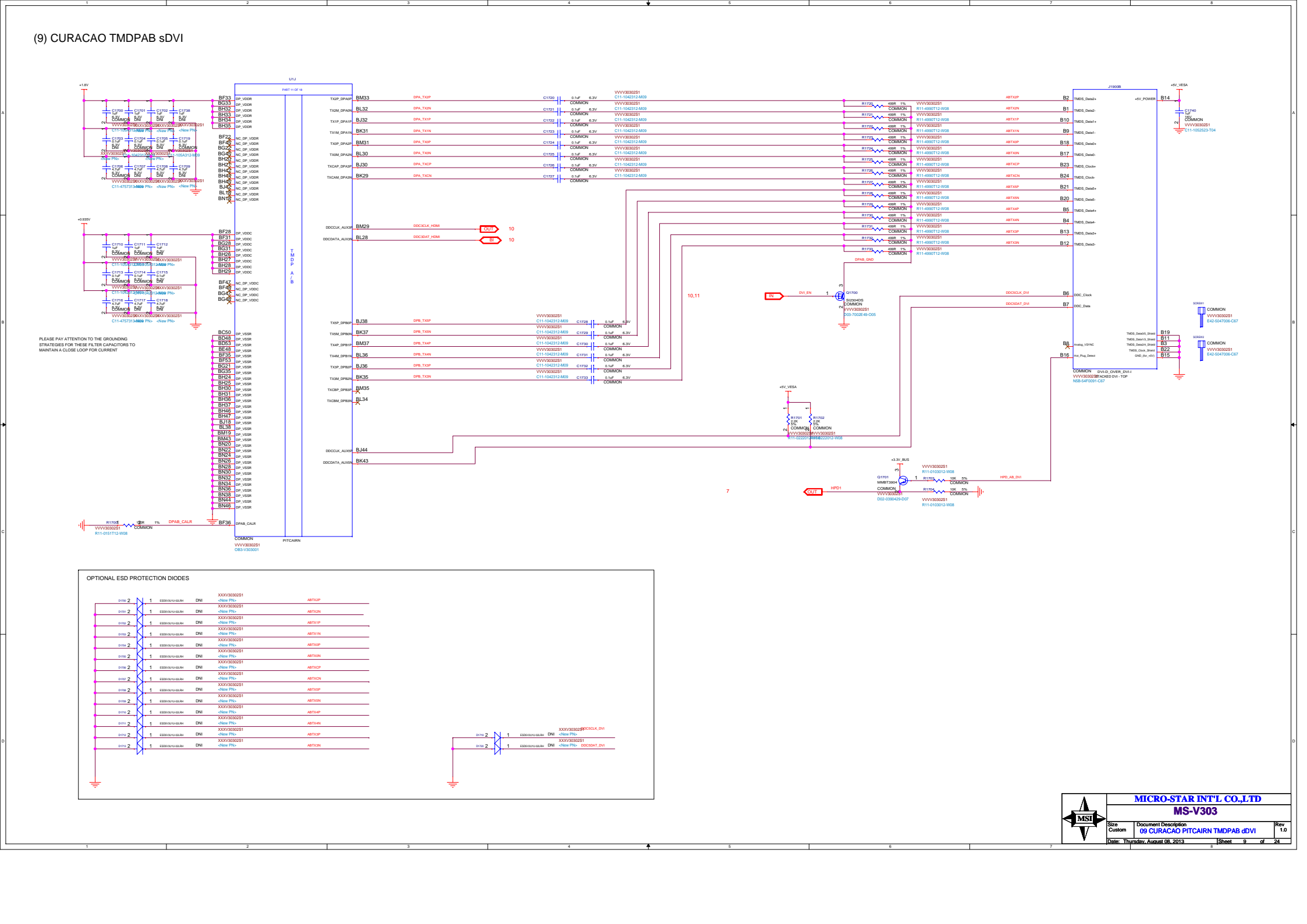
(7) CURACAO GPIO STRAP CF PLL XTAL



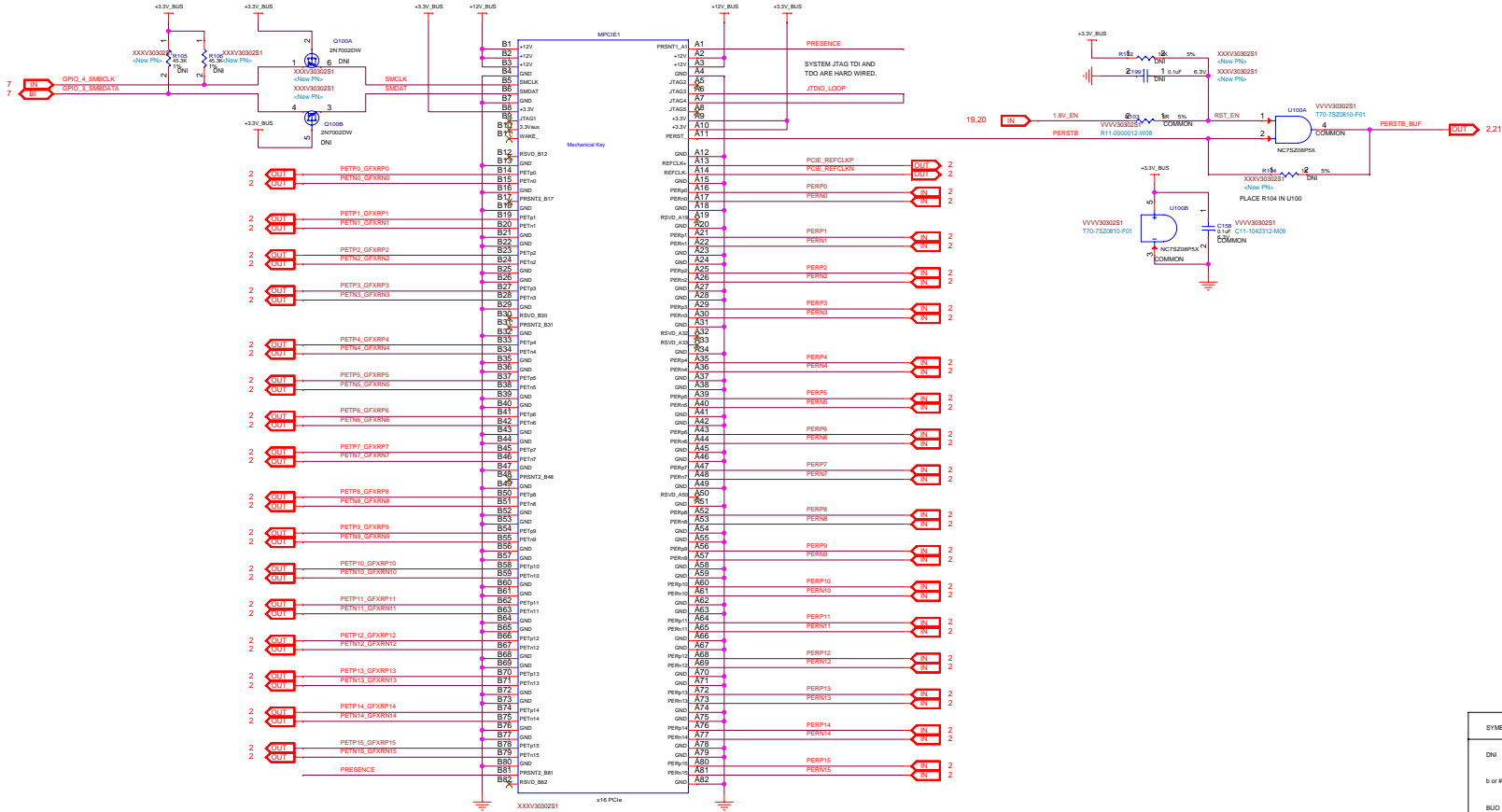
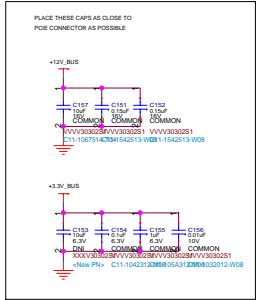
(8) CURACAO DAC



(9) CURACAO TMDPAB sDVI

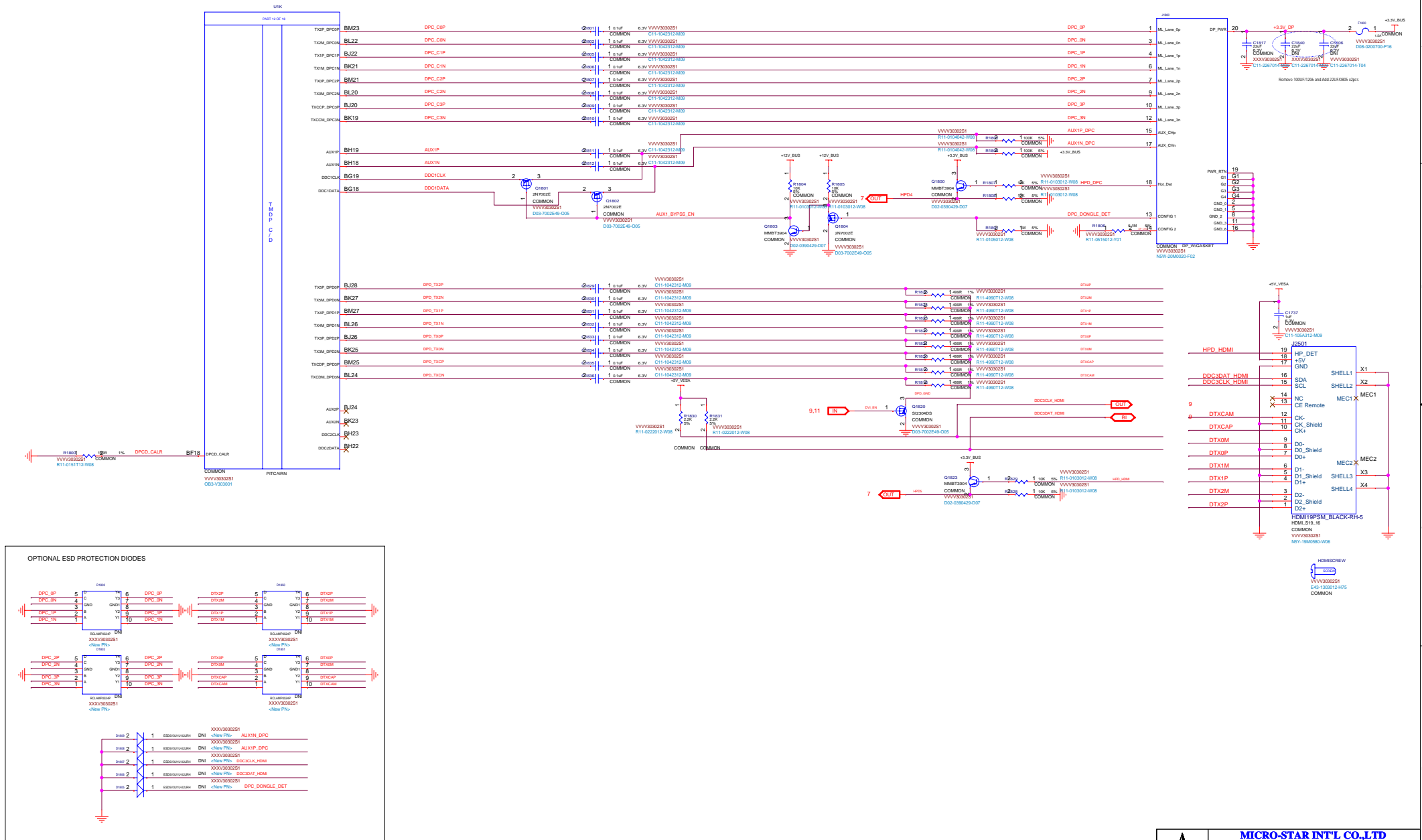


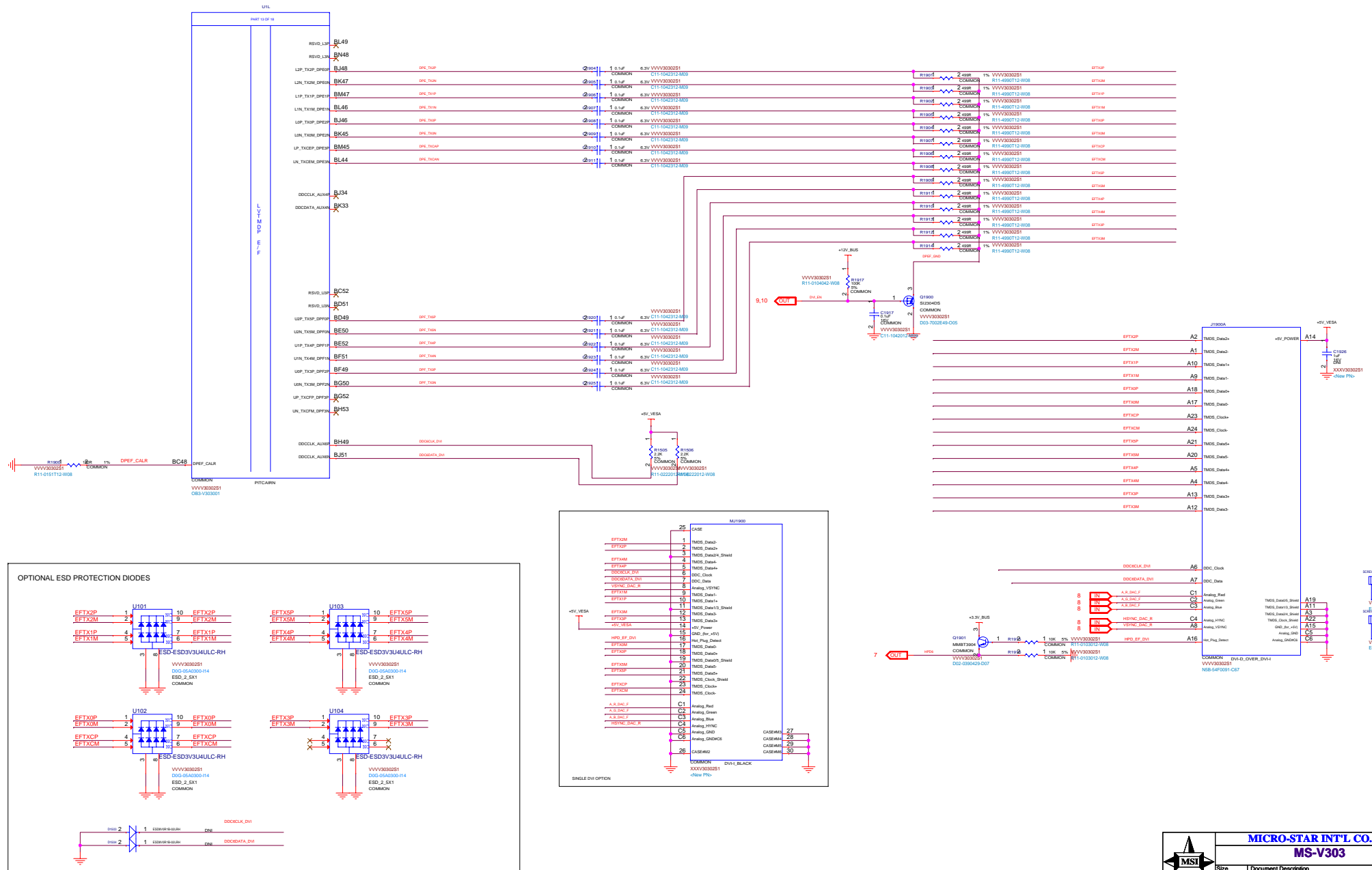
(1) PCI-EXPRESS EDGE CONNECTOR



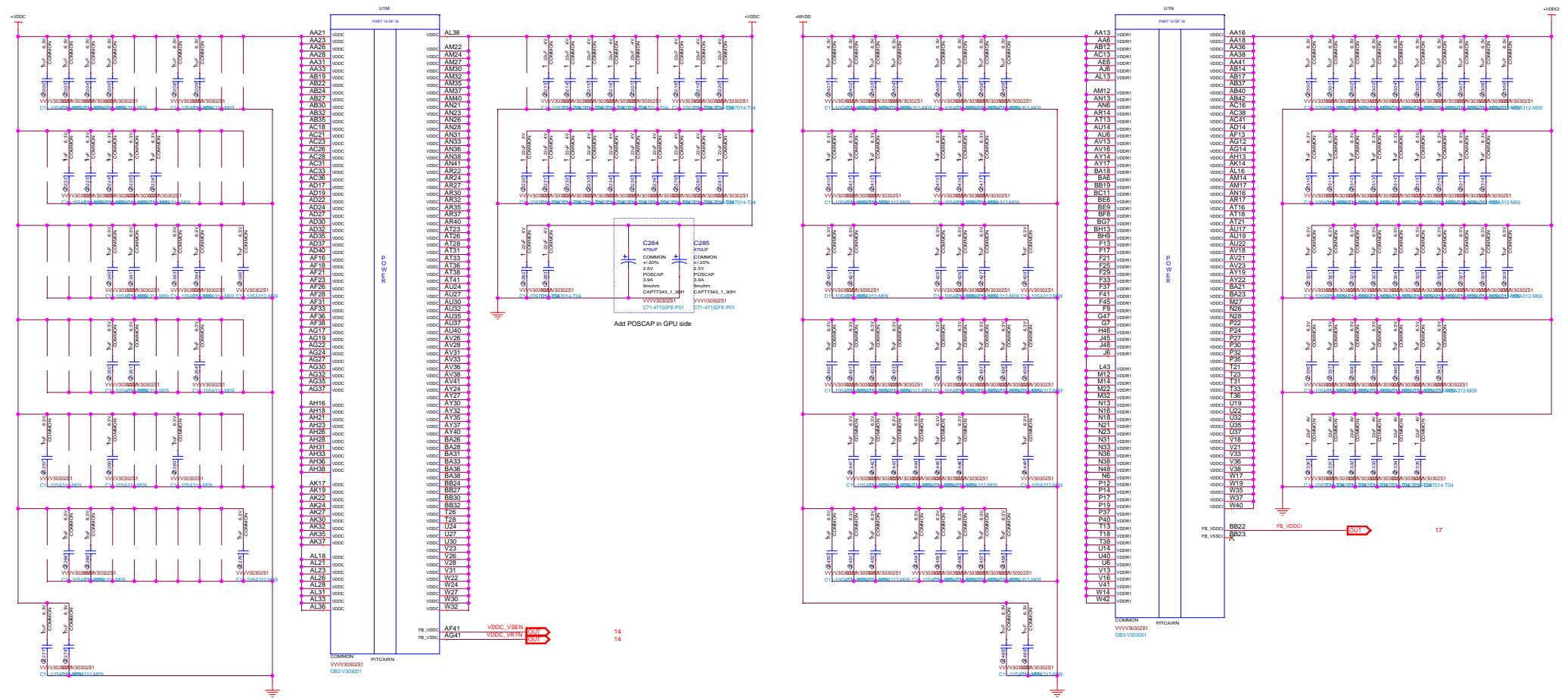
SYMBOL LEGEND	
DN	DO NOT INSTALL
b or #	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

(10) CURACAO TMDPCD DP HDMI





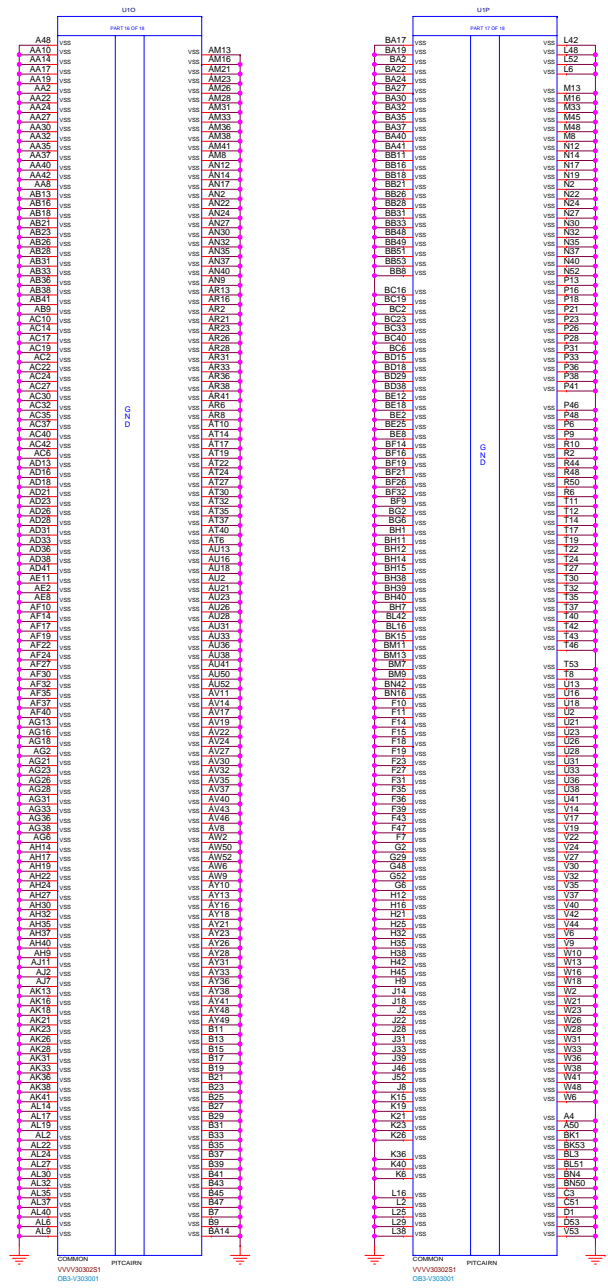
(12) CURACAO POWER



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Date: Thursday, August 08, 2013		Sheet 12 of 24

(13) CURACAO GND





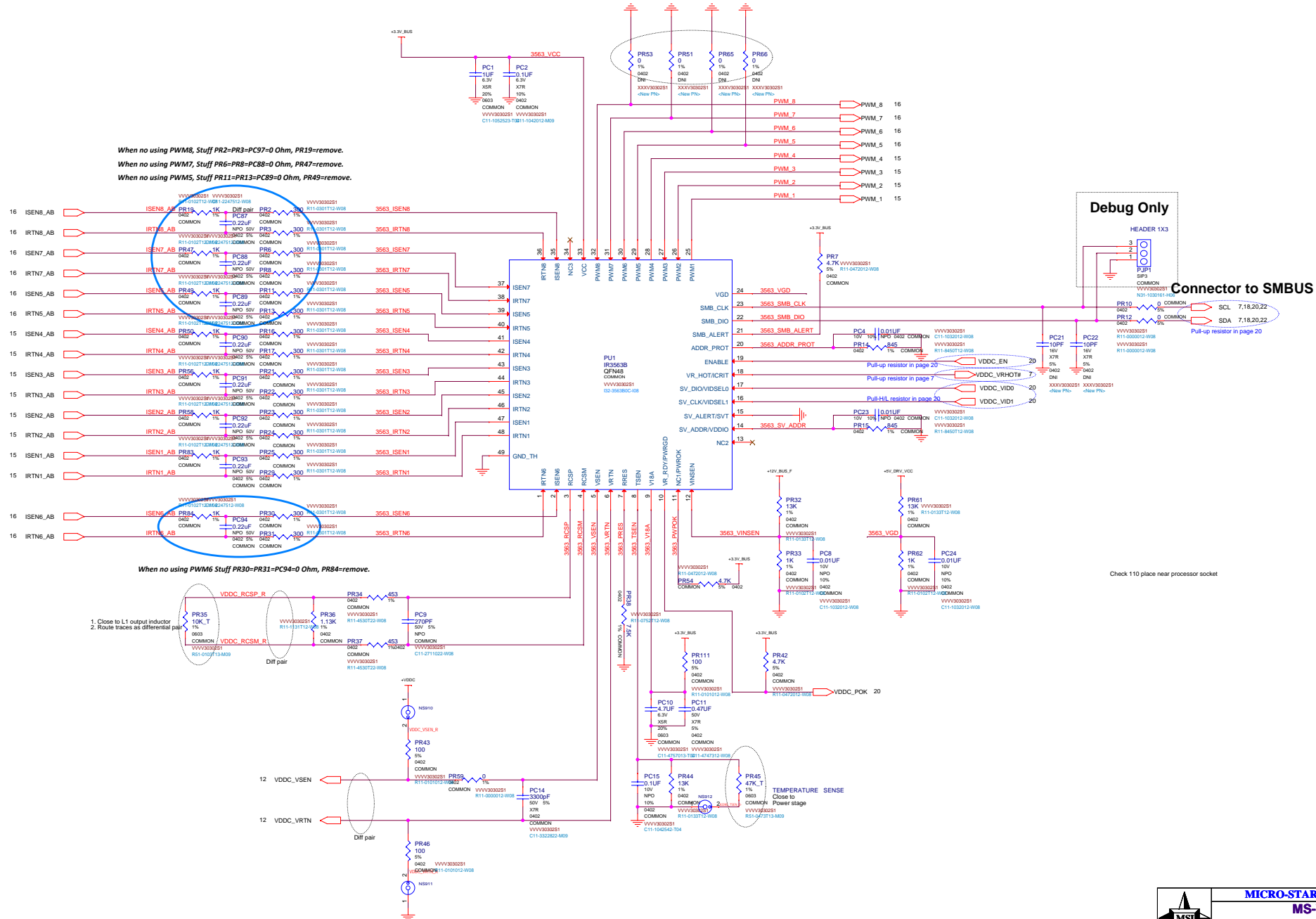
MICRO-STAR INT'L CO.,LTD

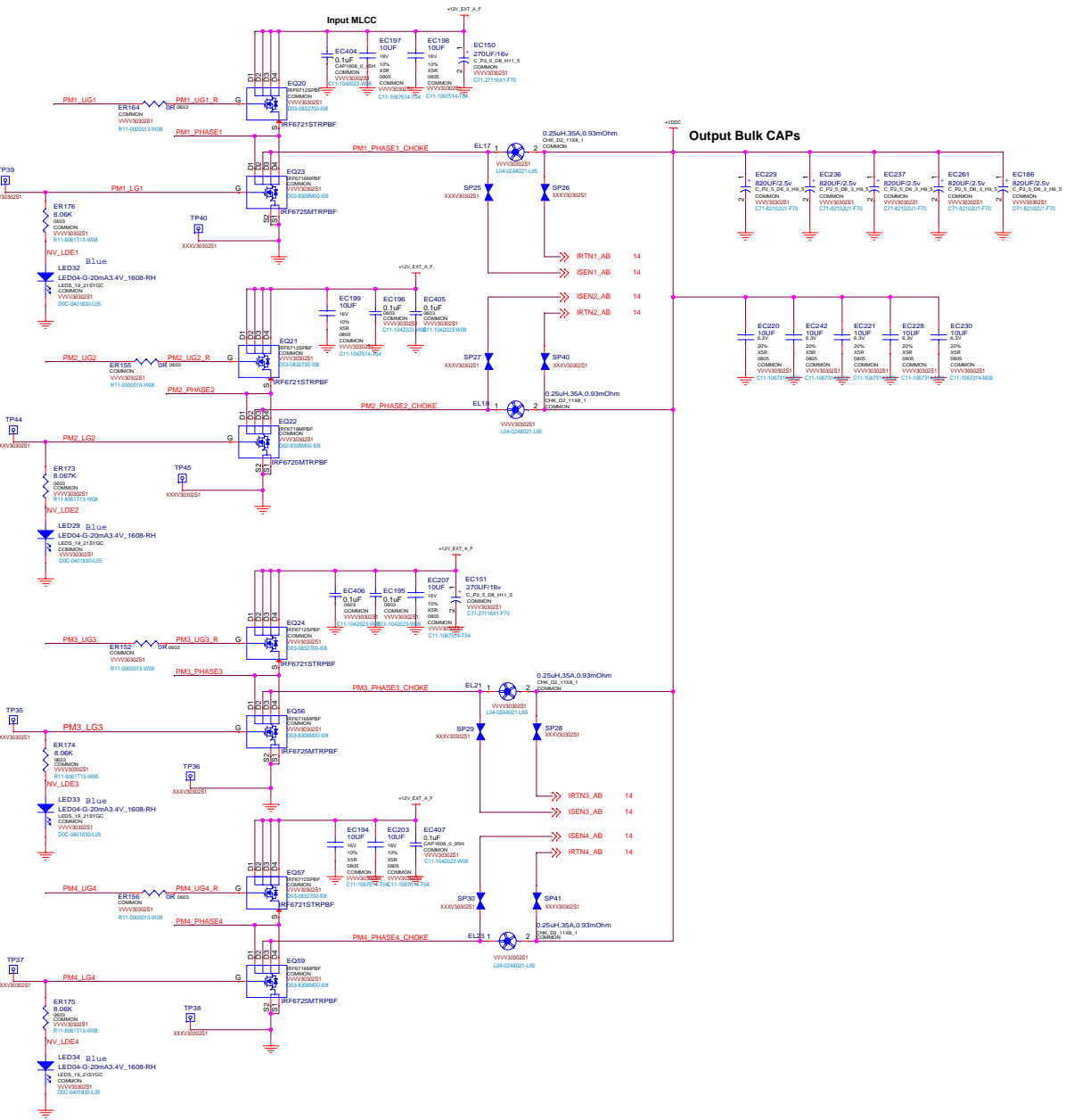
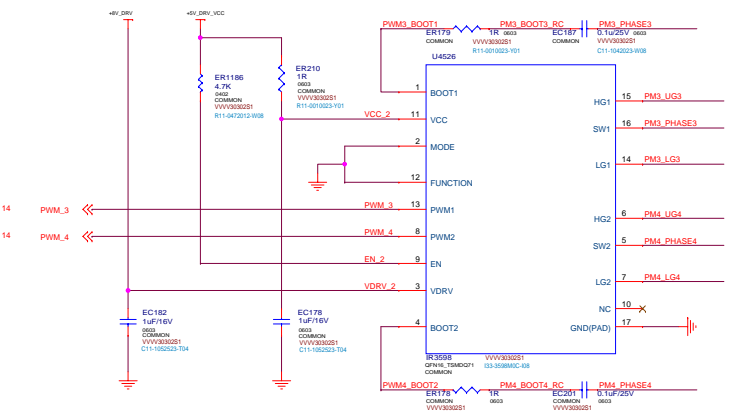
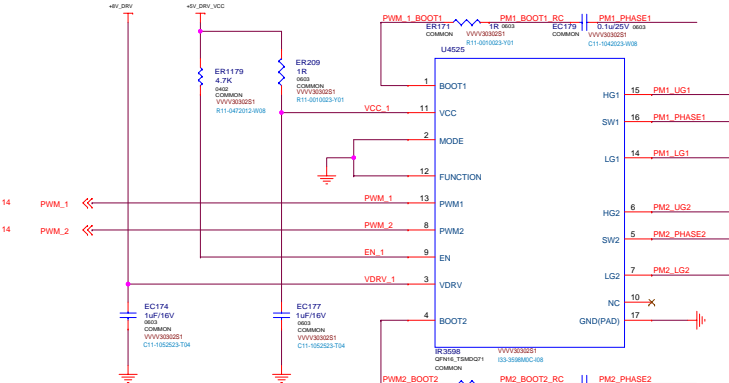
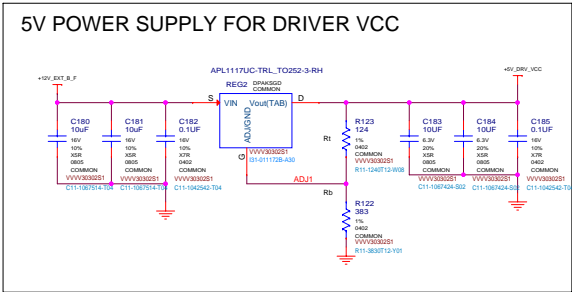
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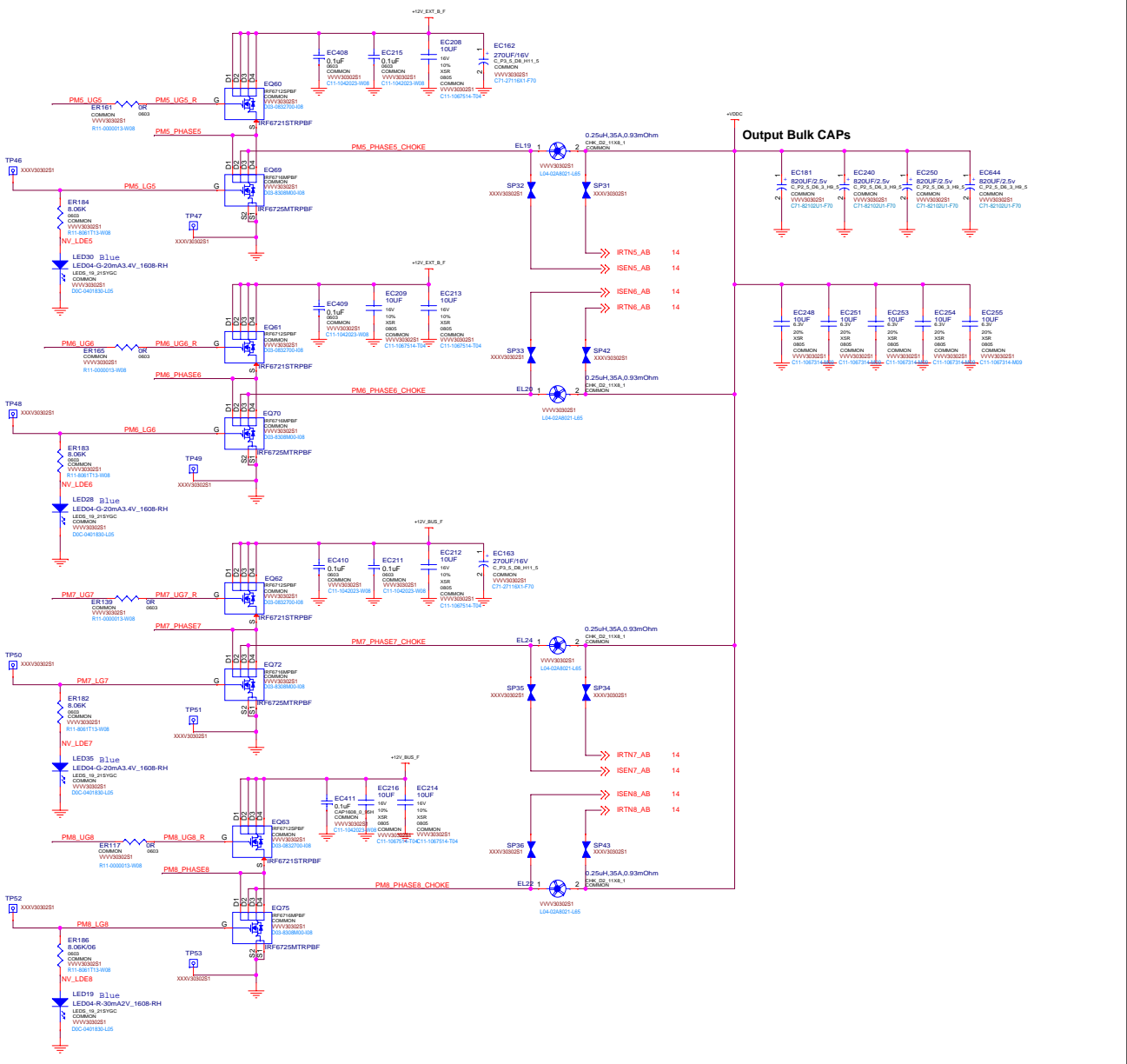
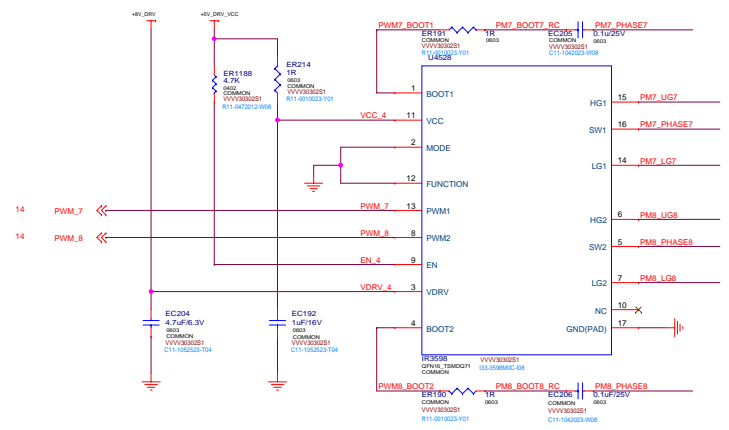
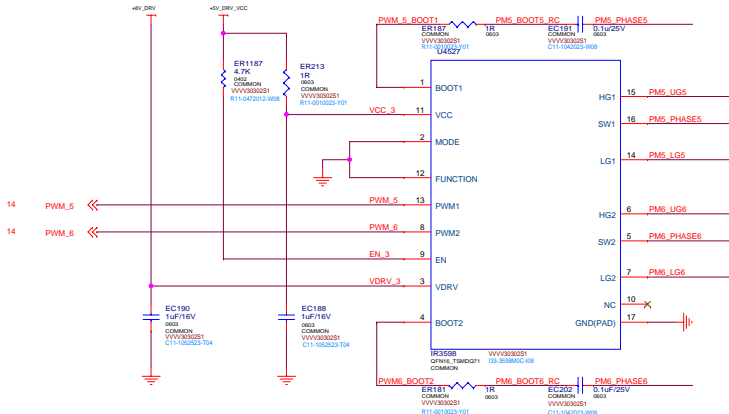
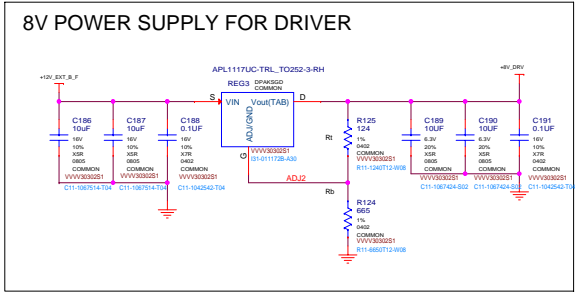
Size Custom Document Description 13 CURACAO PITCAIRN GND Rev 1.0

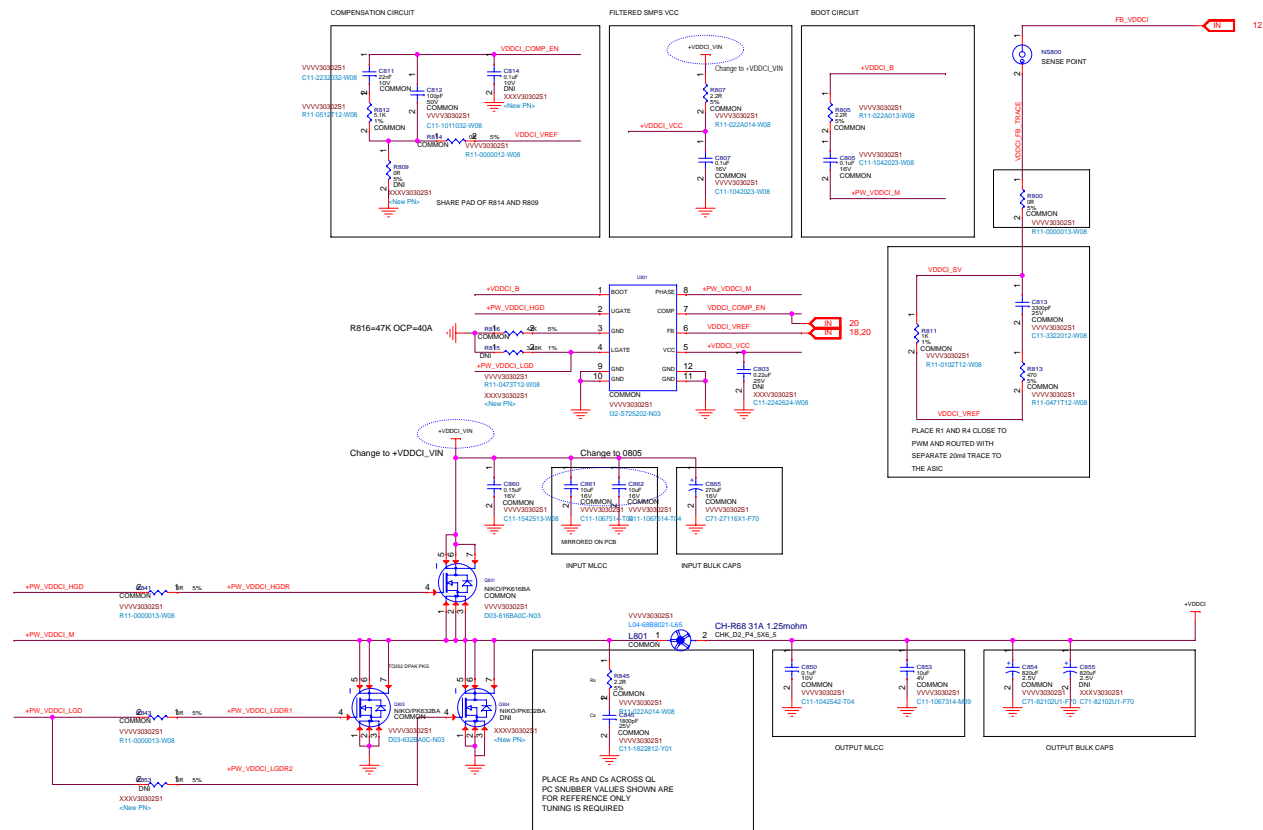
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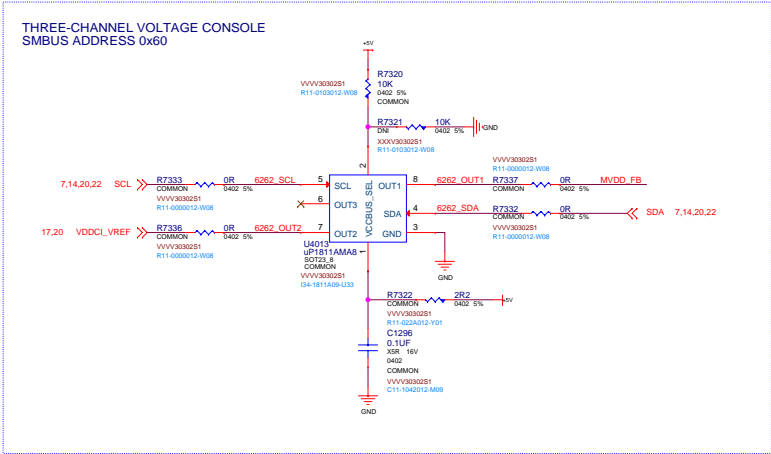
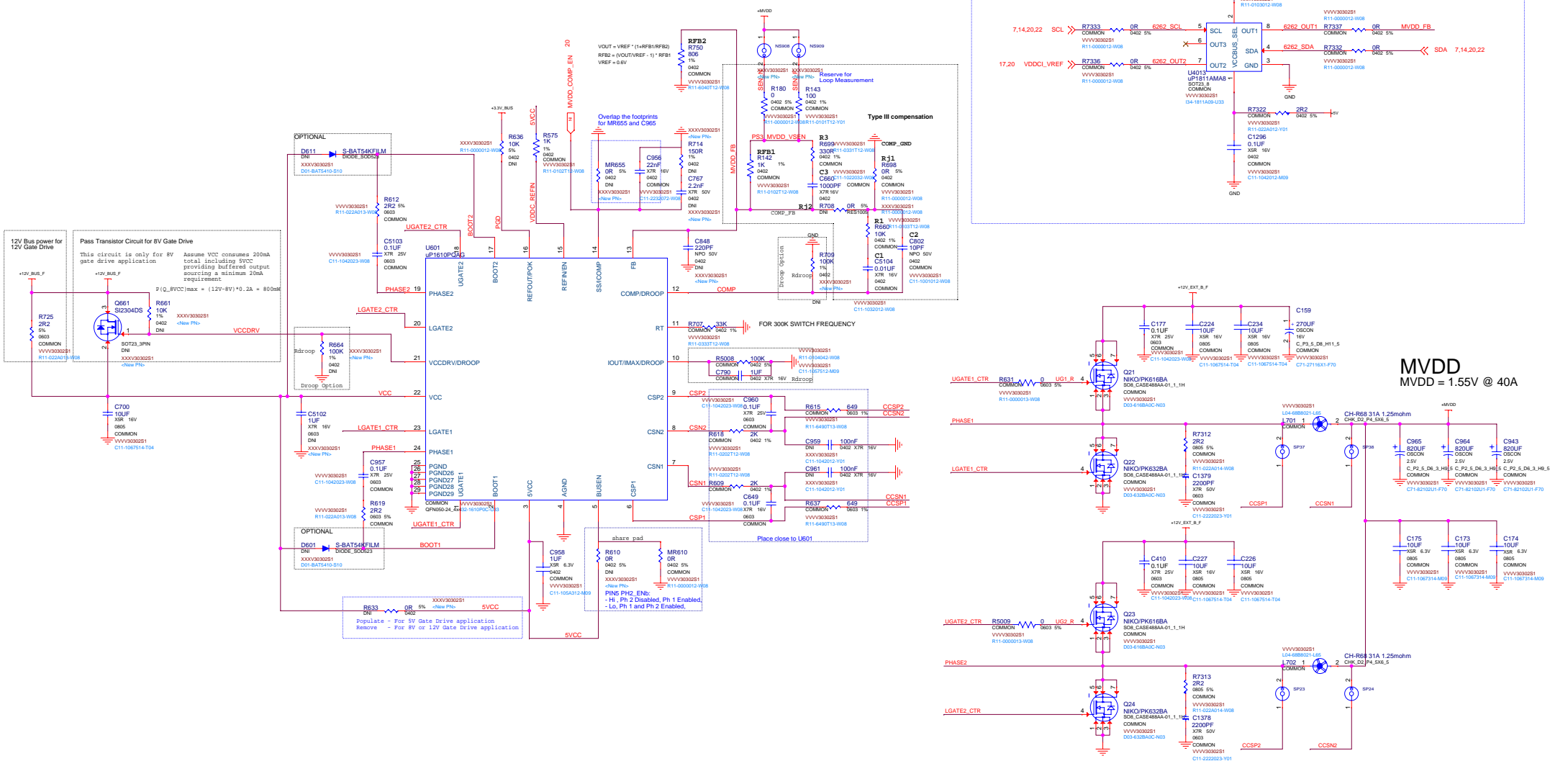
When no using PWM5~8, Stuff PR51/PR53/PR65/PR66 = 0 Ohm.









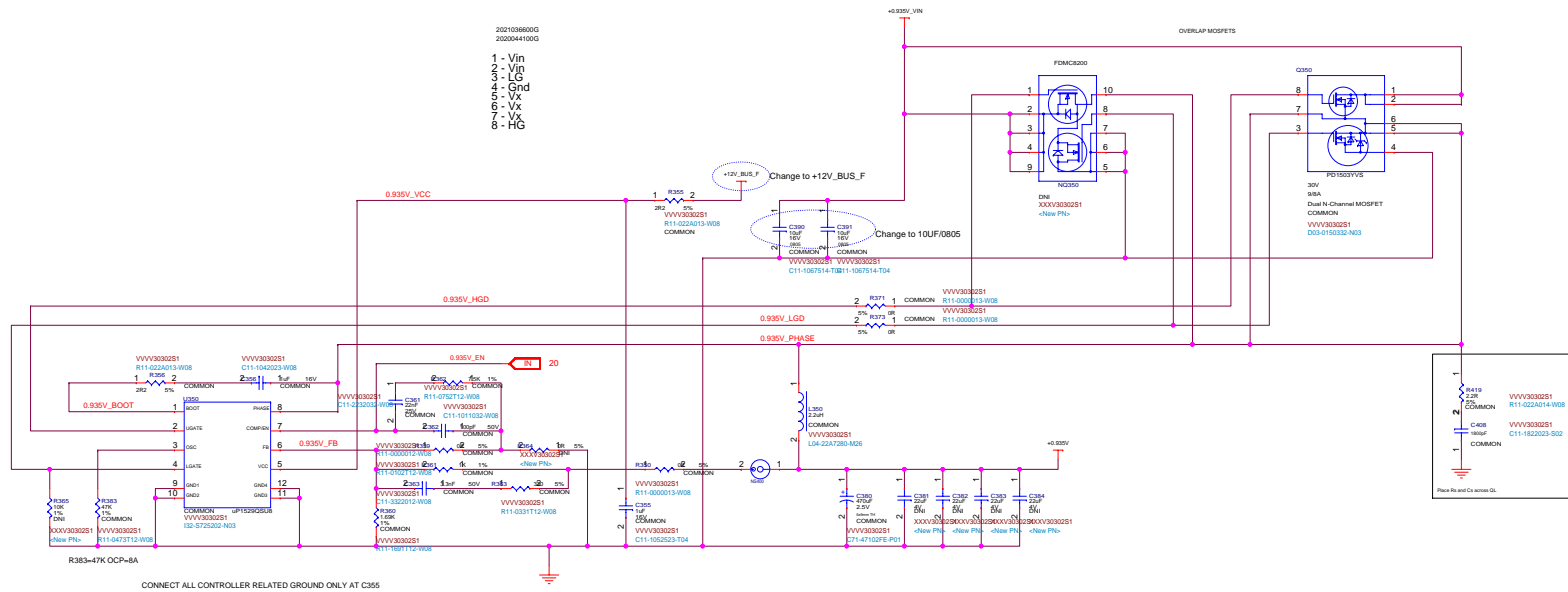
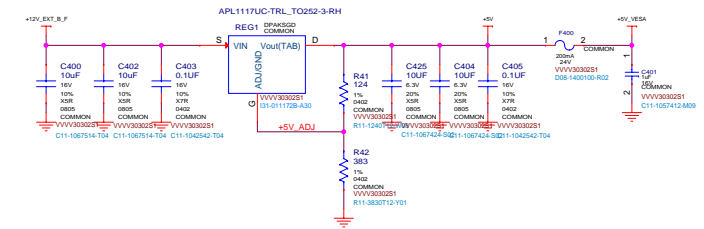
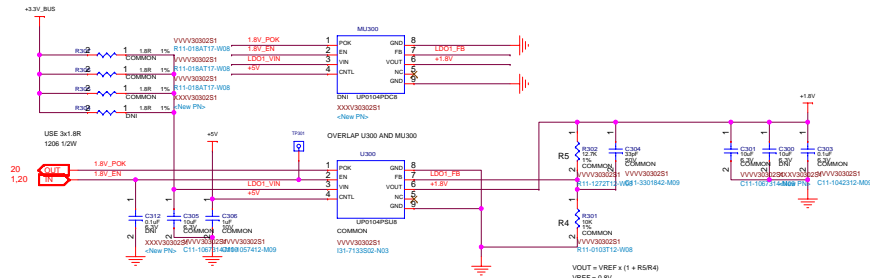


MVDD
MVDD = 1.55V @ 40A

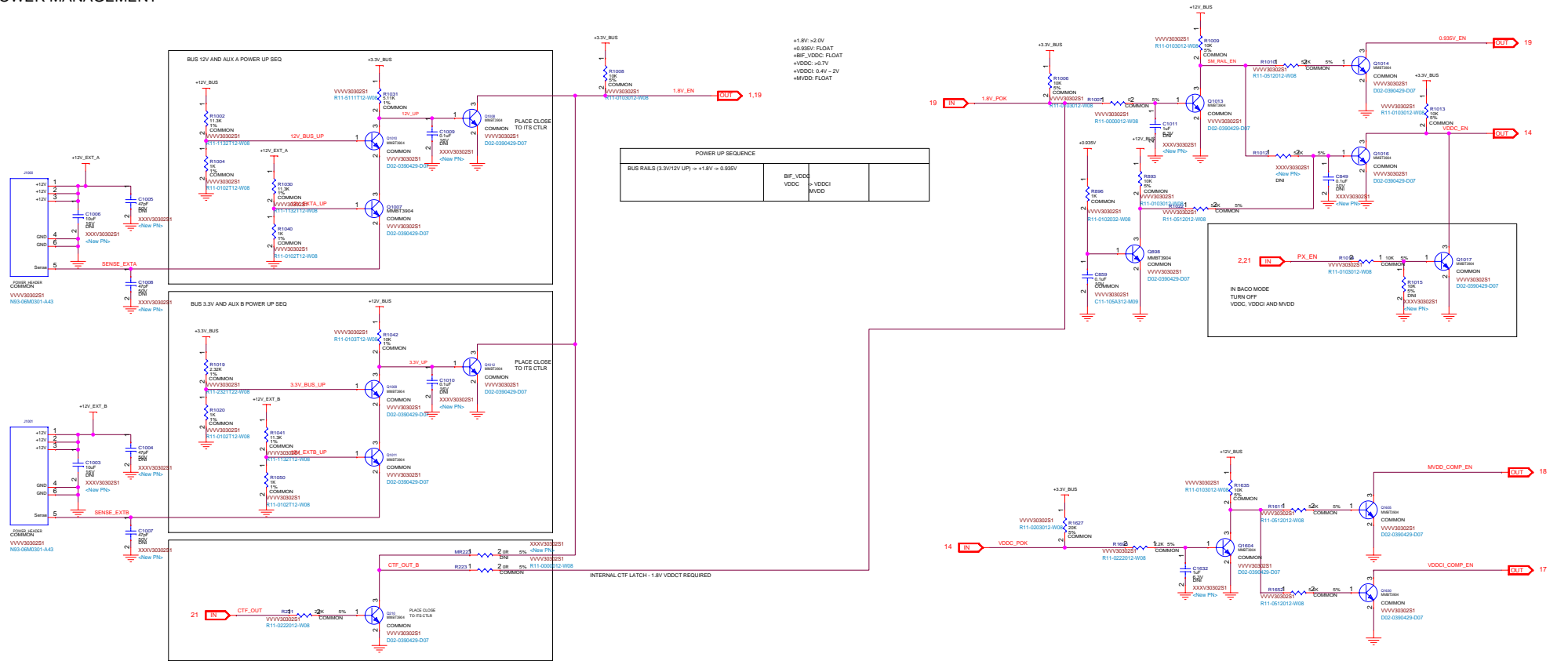
(18) SMALL RAIL REGULATOR

LDO #1: VIN = 3.0V TO 3.6V MAX VOUT = +1.8V +/- 2% IOUT = 1.3A RMS MAX
PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING

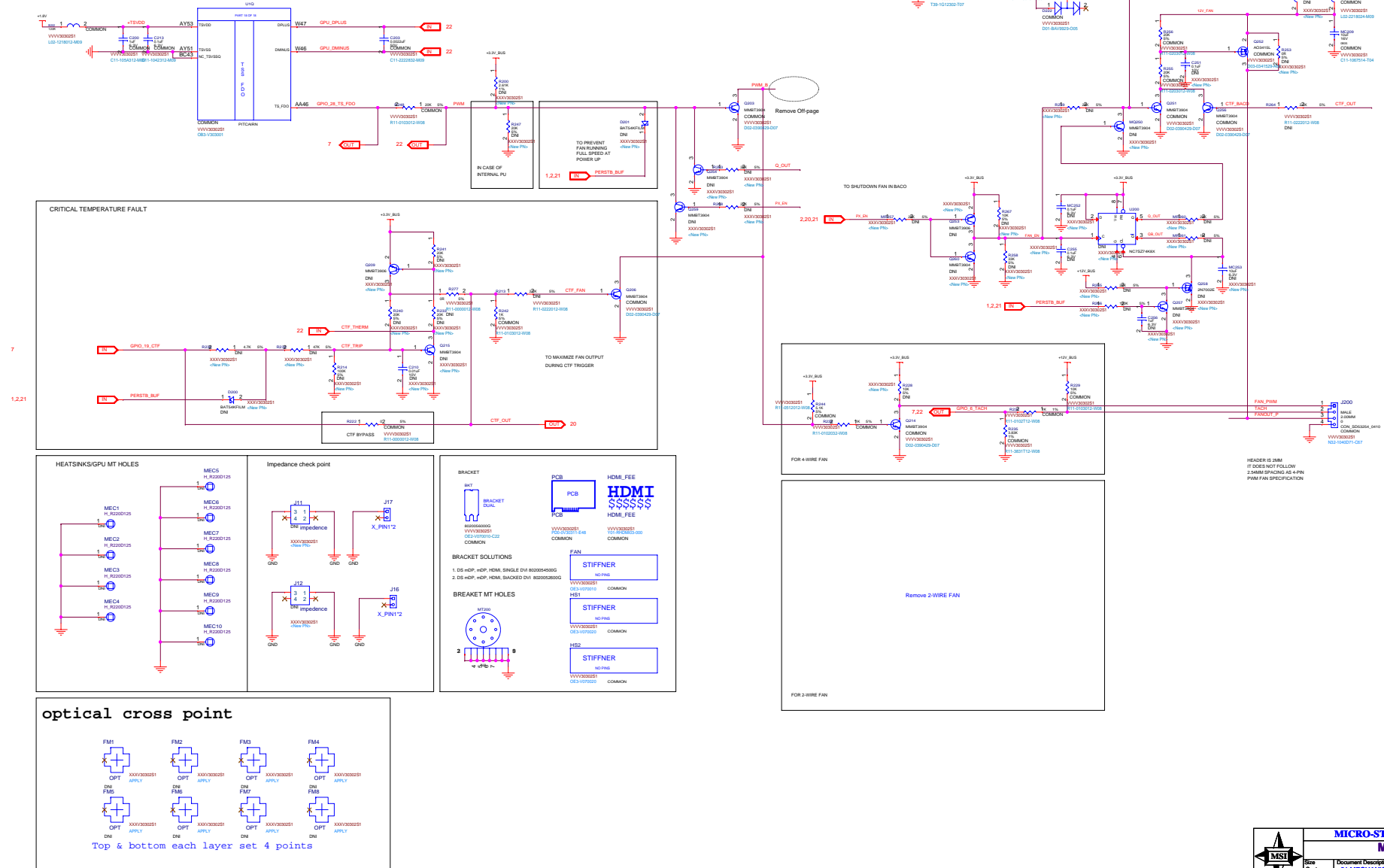
REGULATOR FOR +5V RAILS
IOUT MAX = 150mA

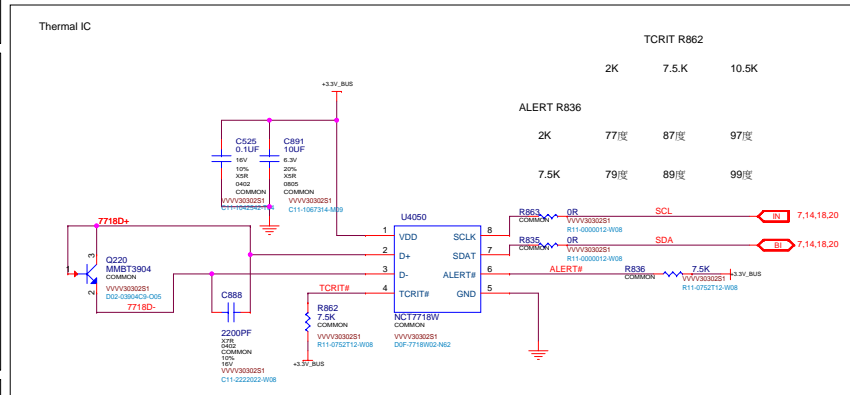
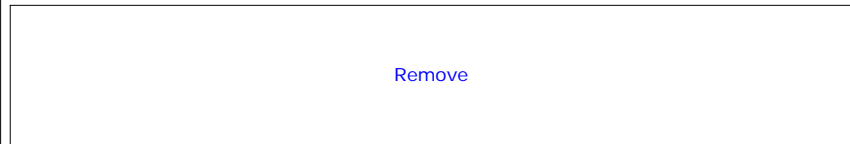
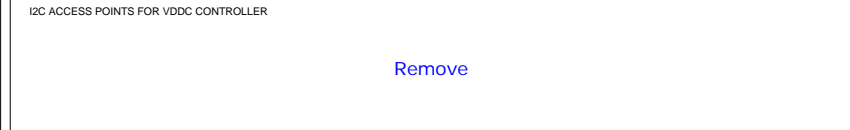
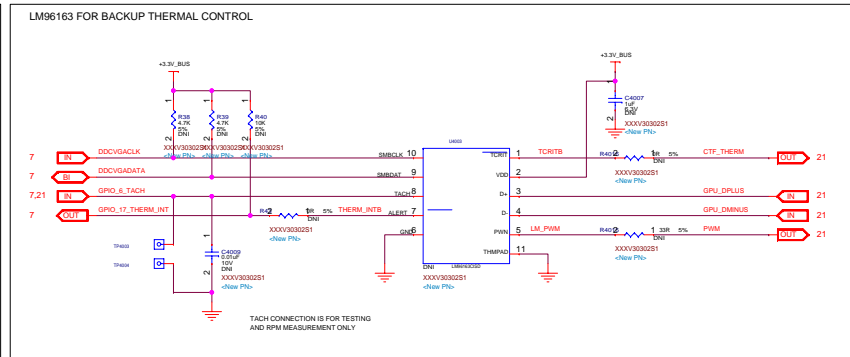
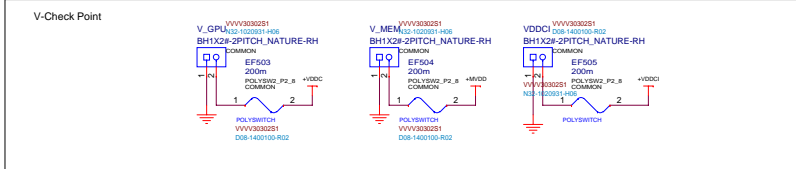
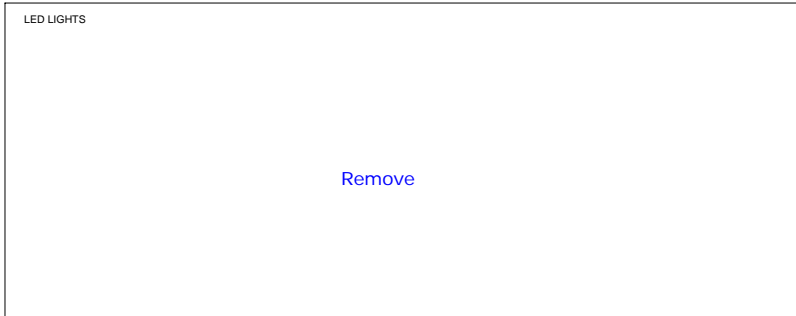
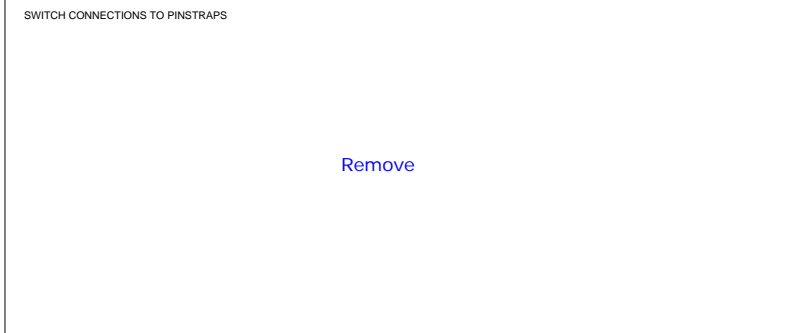
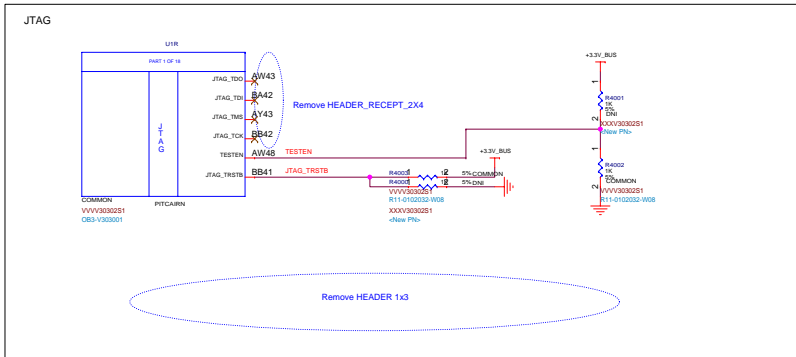


(19) POWER MANAGEMENT



(20) MECH AND THERM MANAGEMENT





0	00A	12/07/2012	INITIAL SCHEMATIC BASED ON C400
1	00B	30/10/2012	add R688,C98,C99
1	00C	25/12/2012	remove L1720 ~ L1733 remove NC pin for DP_VDDR/DP_VDDC
	00D	19/06/2013	update power sequence to make 0.95V power up before vddc
V303-1.0	01/08/2013	Page07 : Remove GPIO_14_HPDI off-page Add Dual-BIOS & Switch Page10 : Change J2501 footprint and Library Page11 : Add optional ESD Protection DIODES Page12 : Add C284/C285 (POSCAP) Remove some 1UF/0402 of VDDC Page14 : Change VDDC controller to 8228G Page15 : Add Driver IR3598 circuit Page16 : Add Driver IR3598 circuit Page17 : Change L801 footprint Change VDDCI_VIN Page18 : Page14 : Change MVDD controller to uP1610PQAG Page19 : Change +5V circuit Change 0.935V_VCC to +12V_BUS_F Page20 : Add R7341/R7342/L1506 Del R1090~R1095 Page21 : Remove 2-wire FAN circuit Page22 : Remove JTAG pin header Remove SWITCH CONNECTIONS TO PINSTRAPS Remove LED LIGHTS Remove I2C ACCESS POINTS FOR VDDC CONTROLLER Add V-Check Point and Thermal IC	
V303-1.1	06/08/2013	Page14 : Controller change to IR3563B	