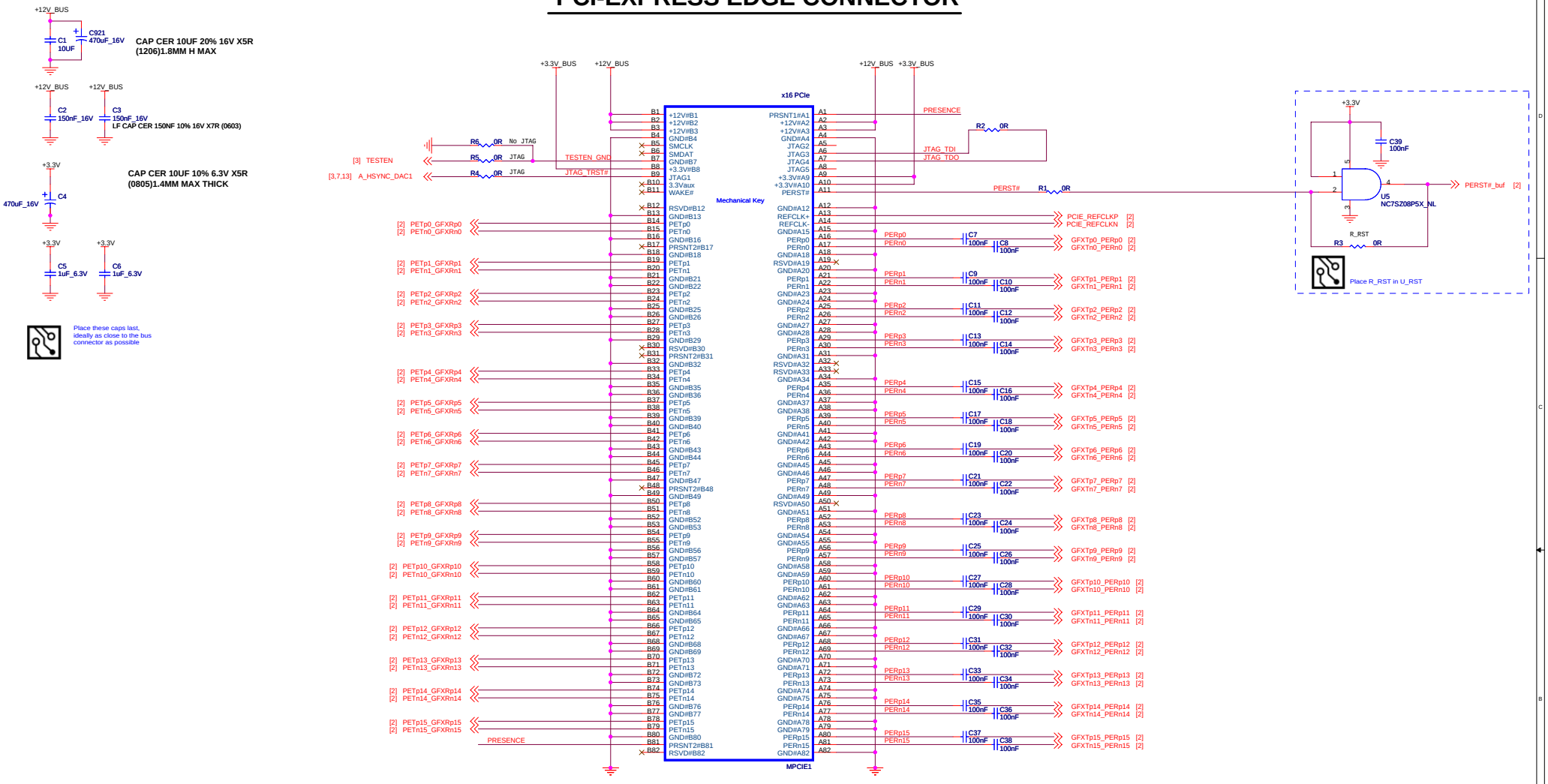
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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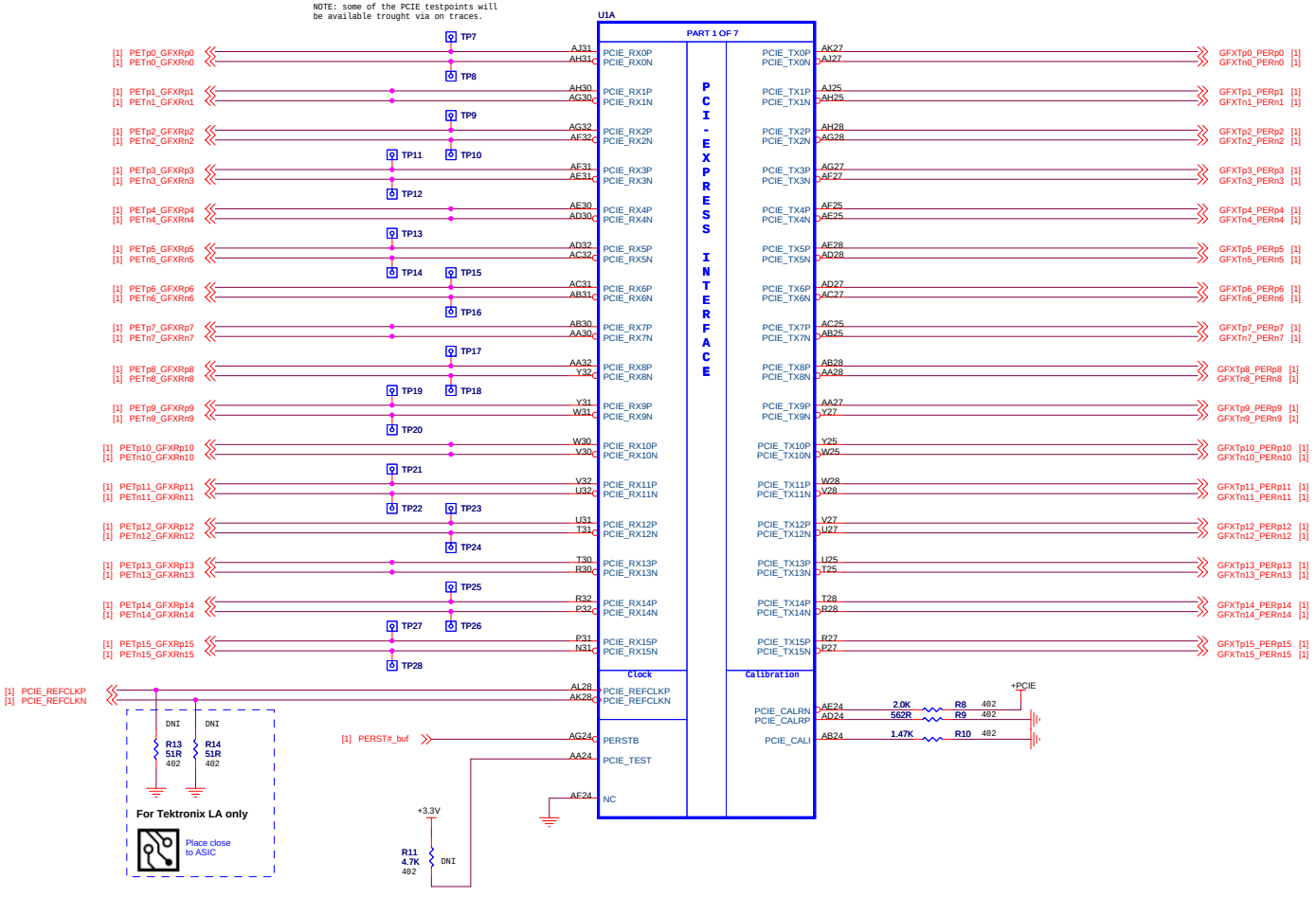
Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH		
Size C	Document Number 105-A880xx-00C		Rev 2
Date: Tuesday, July 18, 2006		Sheet 1 of 20	



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PCB RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH

Size	Document Number	Rev
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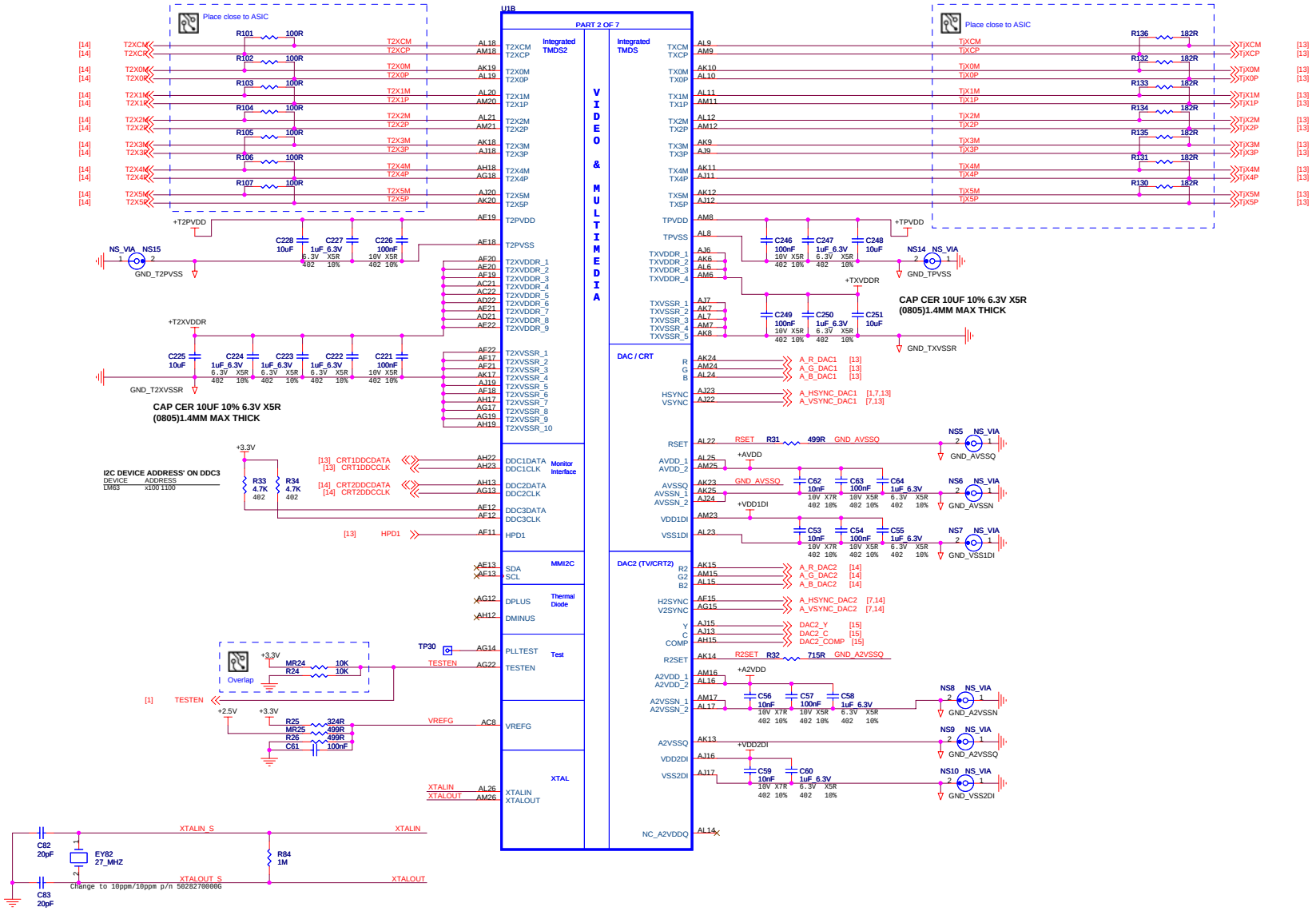

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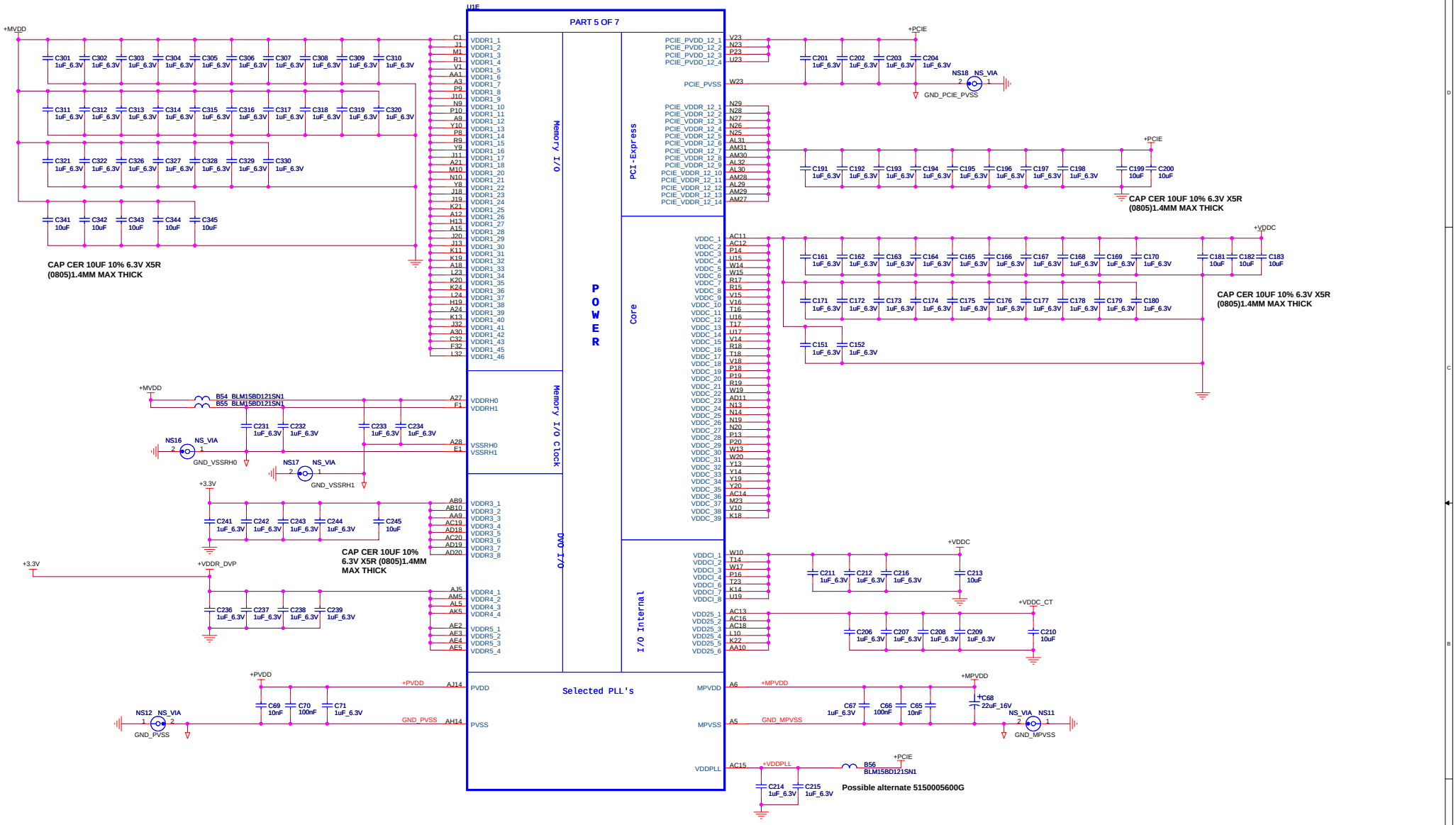
Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH	
Size: Custom	Document Number: 105-A880xx-00C	Rev: 2
Date: Tuesday, July 18, 2006	Sheet 3 of 20	



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Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH		
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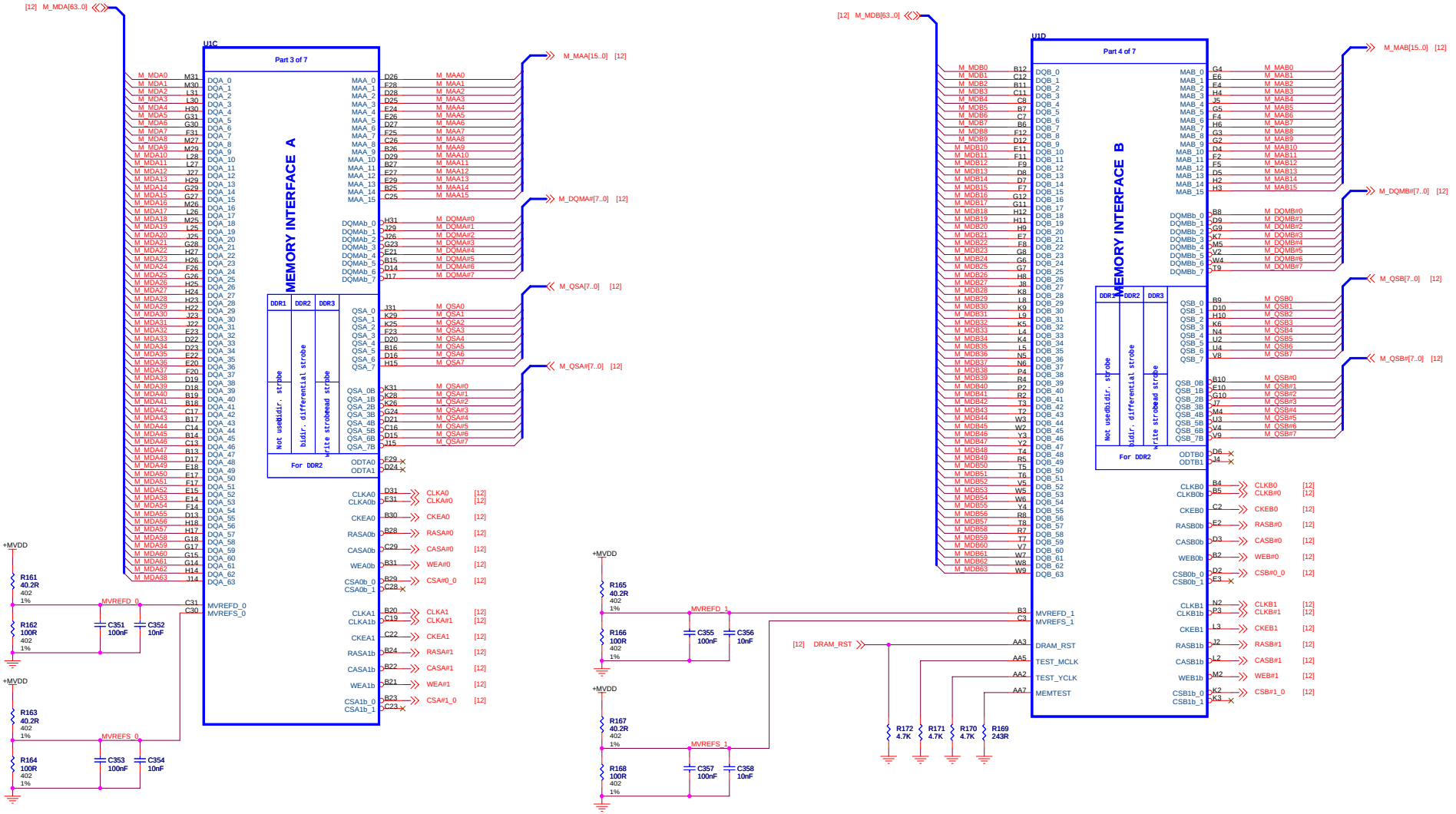

Company	ATI Technologies Inc.
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Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH
Size	C
Document Number	105-A880xx-00C
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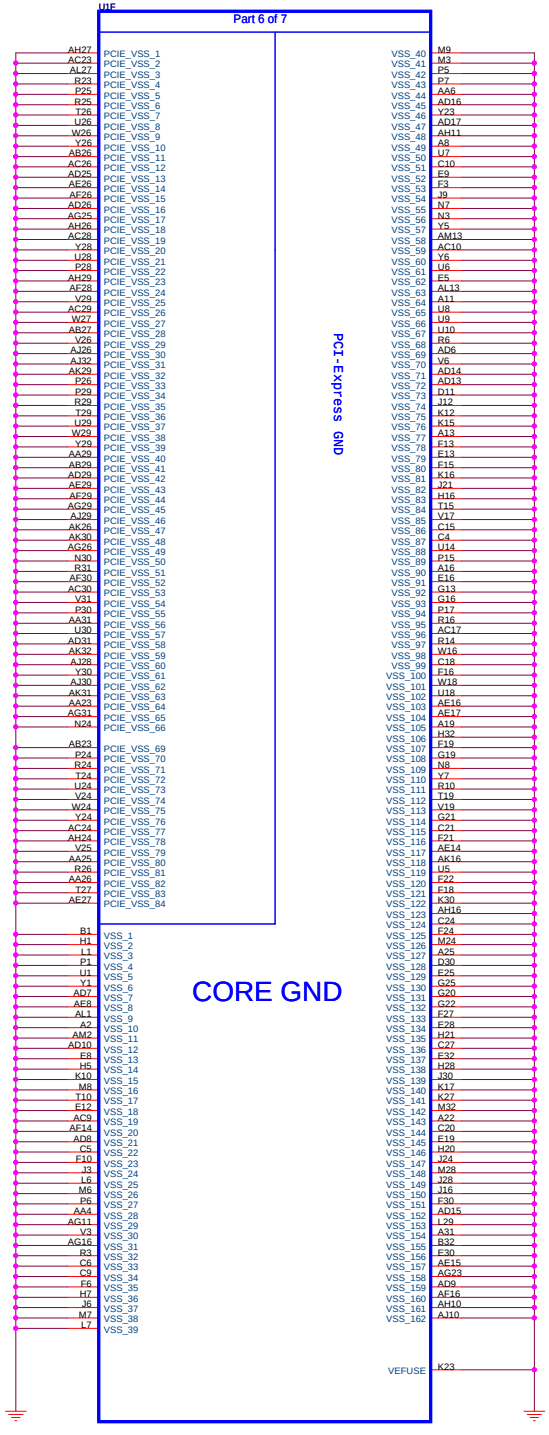

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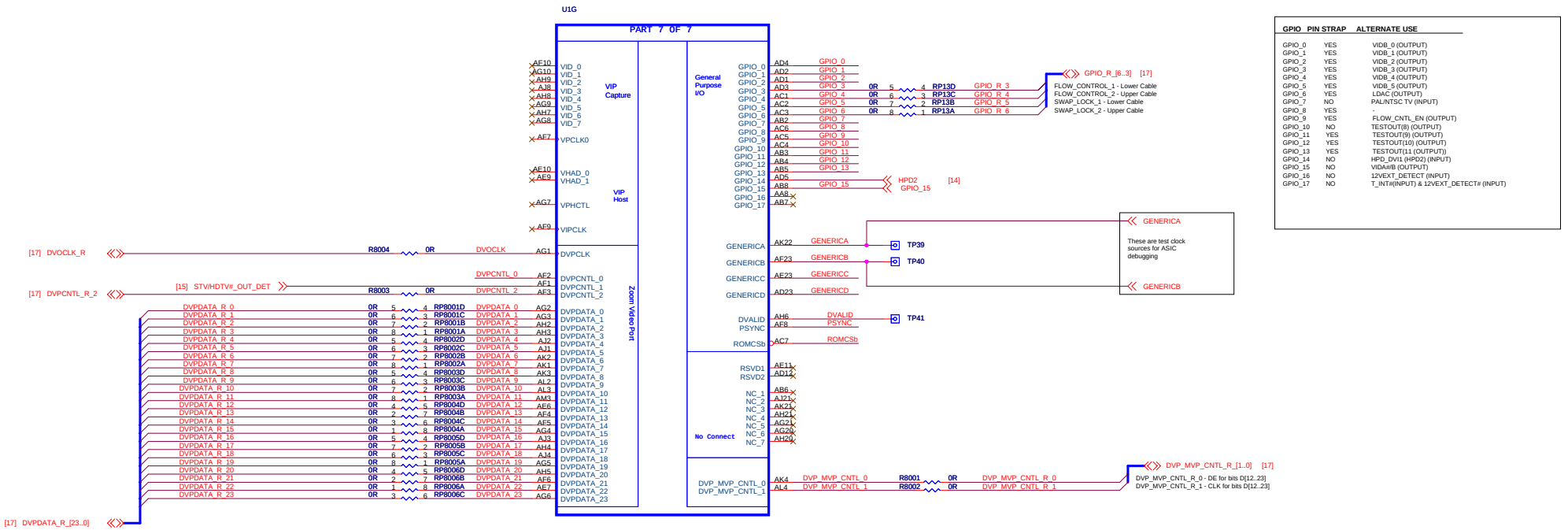
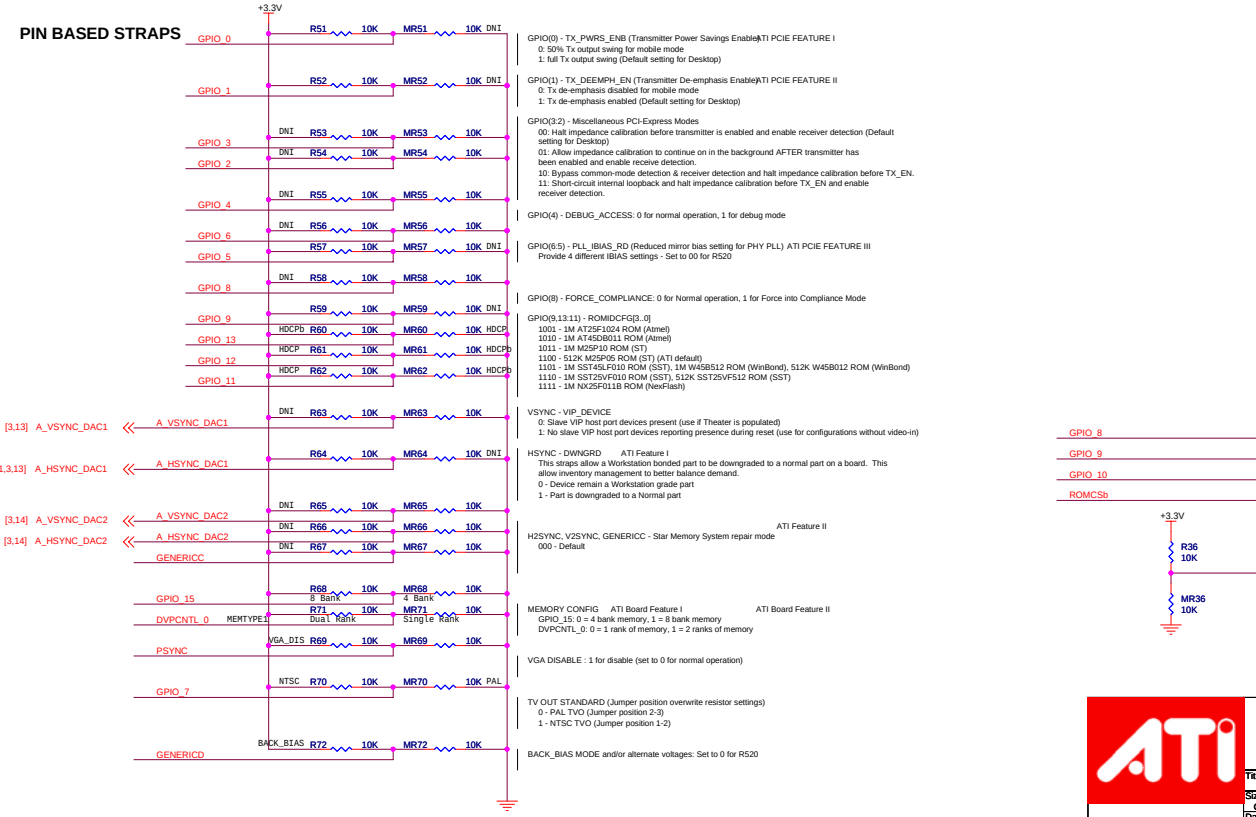
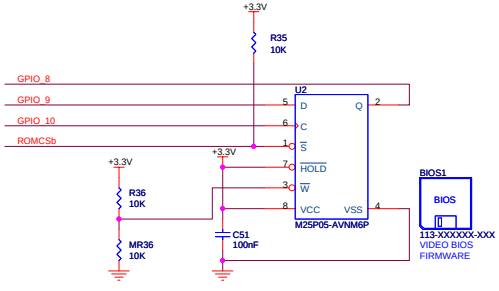


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDAst/B (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)





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Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH	
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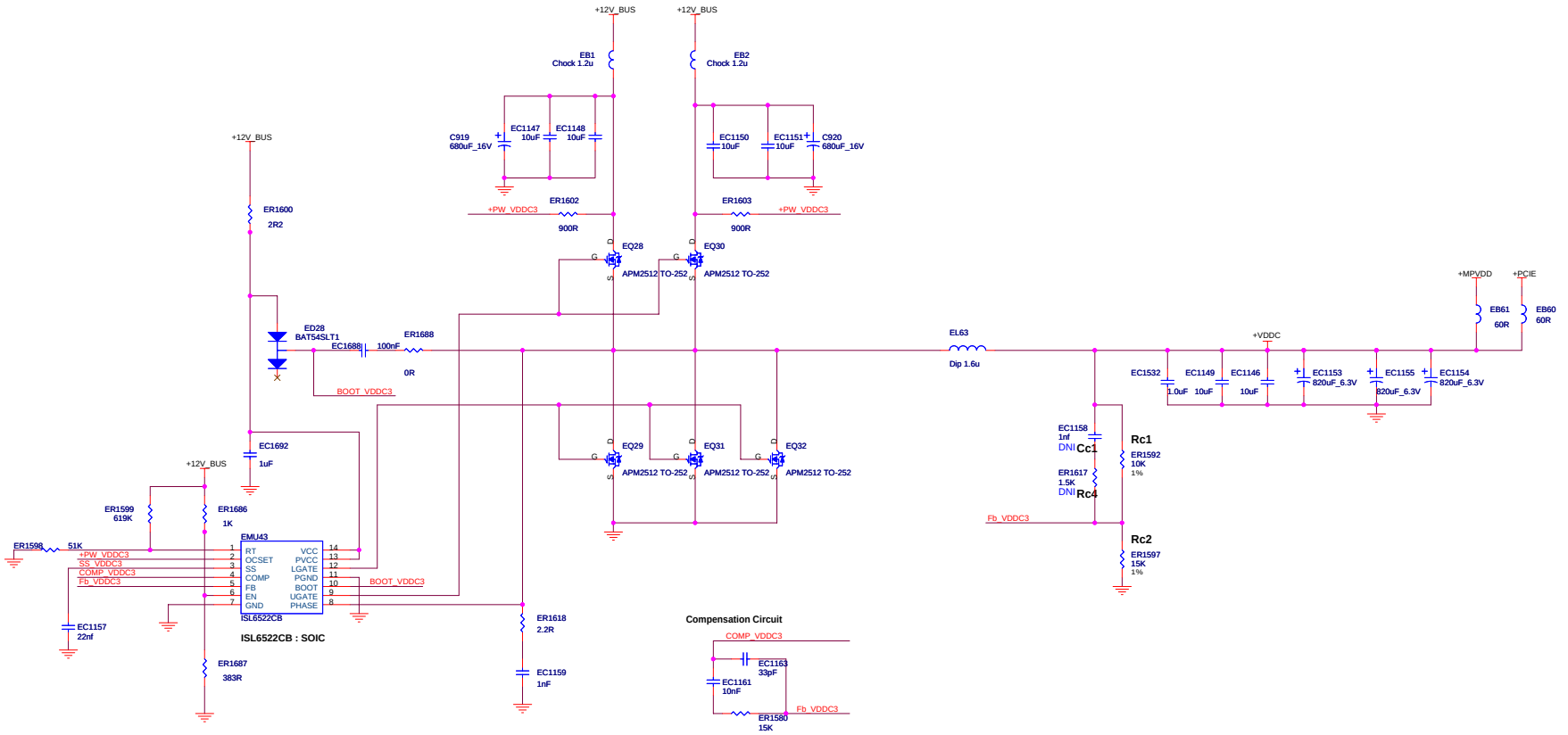
CORE REGULATOR VDDC



+VDDC=0.8*(1+(ER1592 / ER1597))

RV560XT 1.33V

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Size: Custom	Document Number: 105-A880xx-00C	Rev: 2
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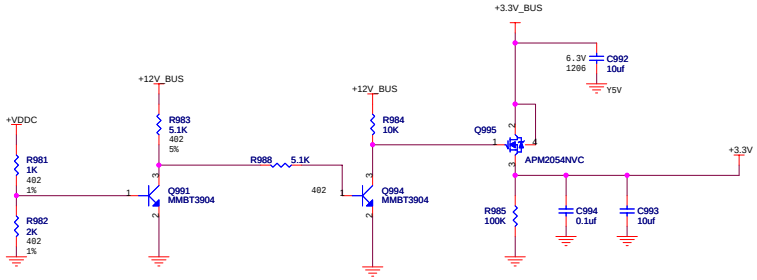

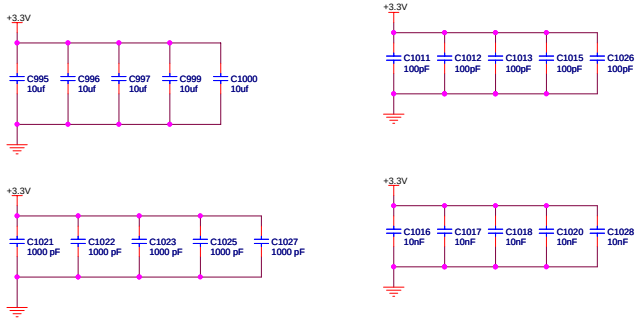

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Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH	
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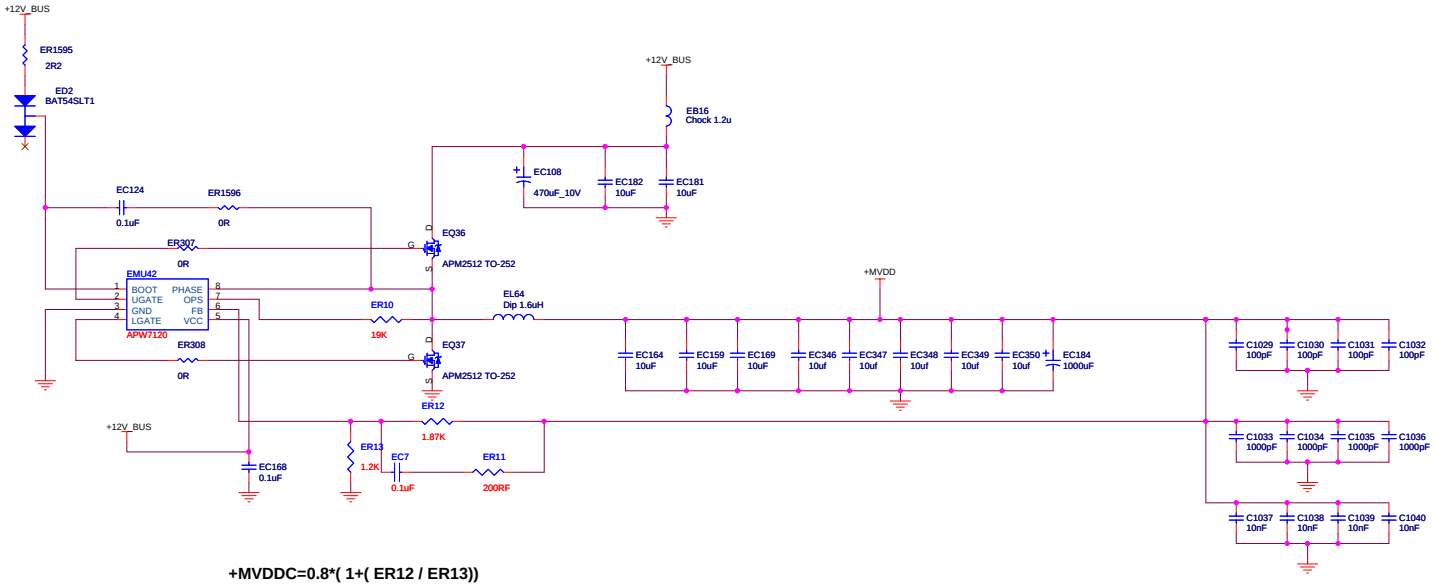

+MVDDC=0.8*(1+(ER12 / ER13))

Regulator for MVDD

Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G

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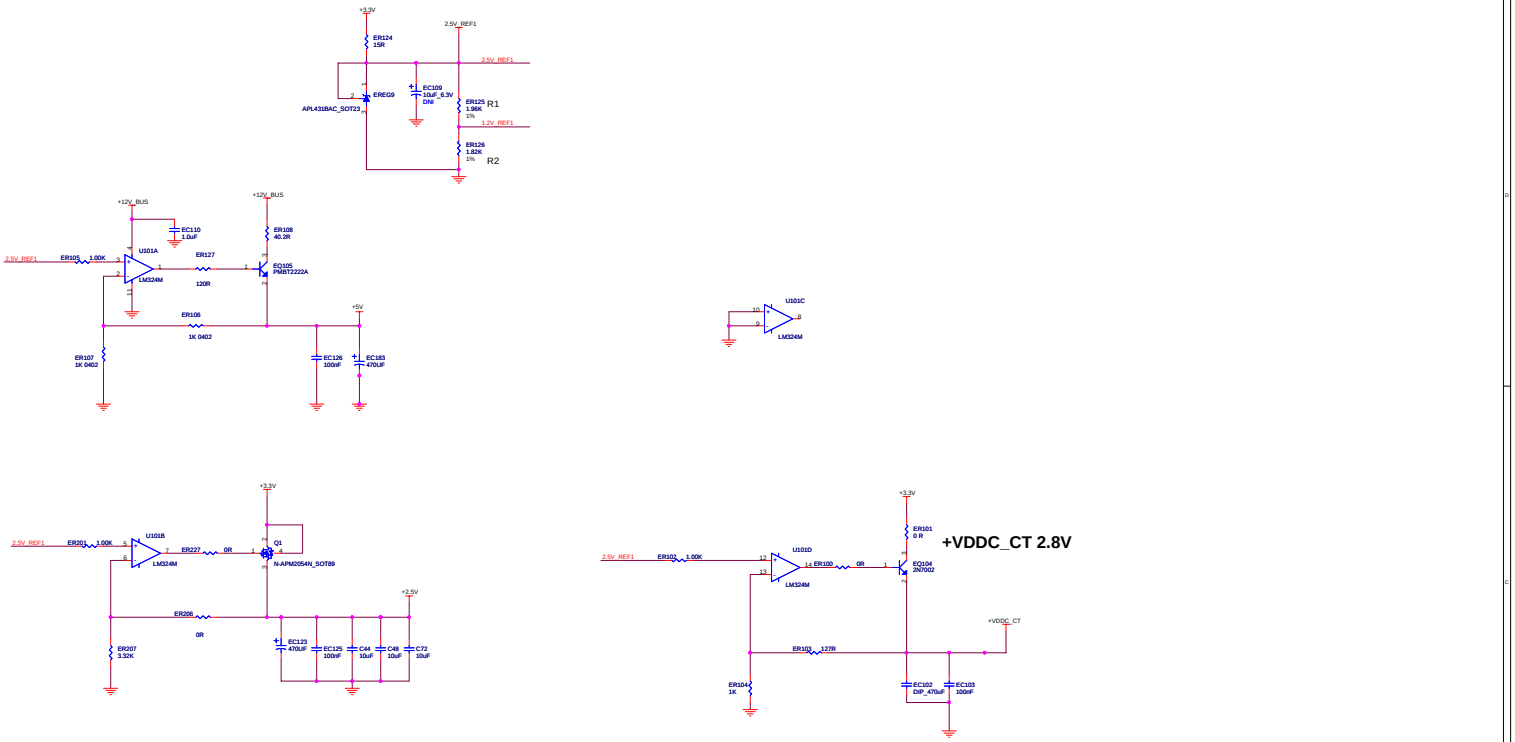

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Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO PH	
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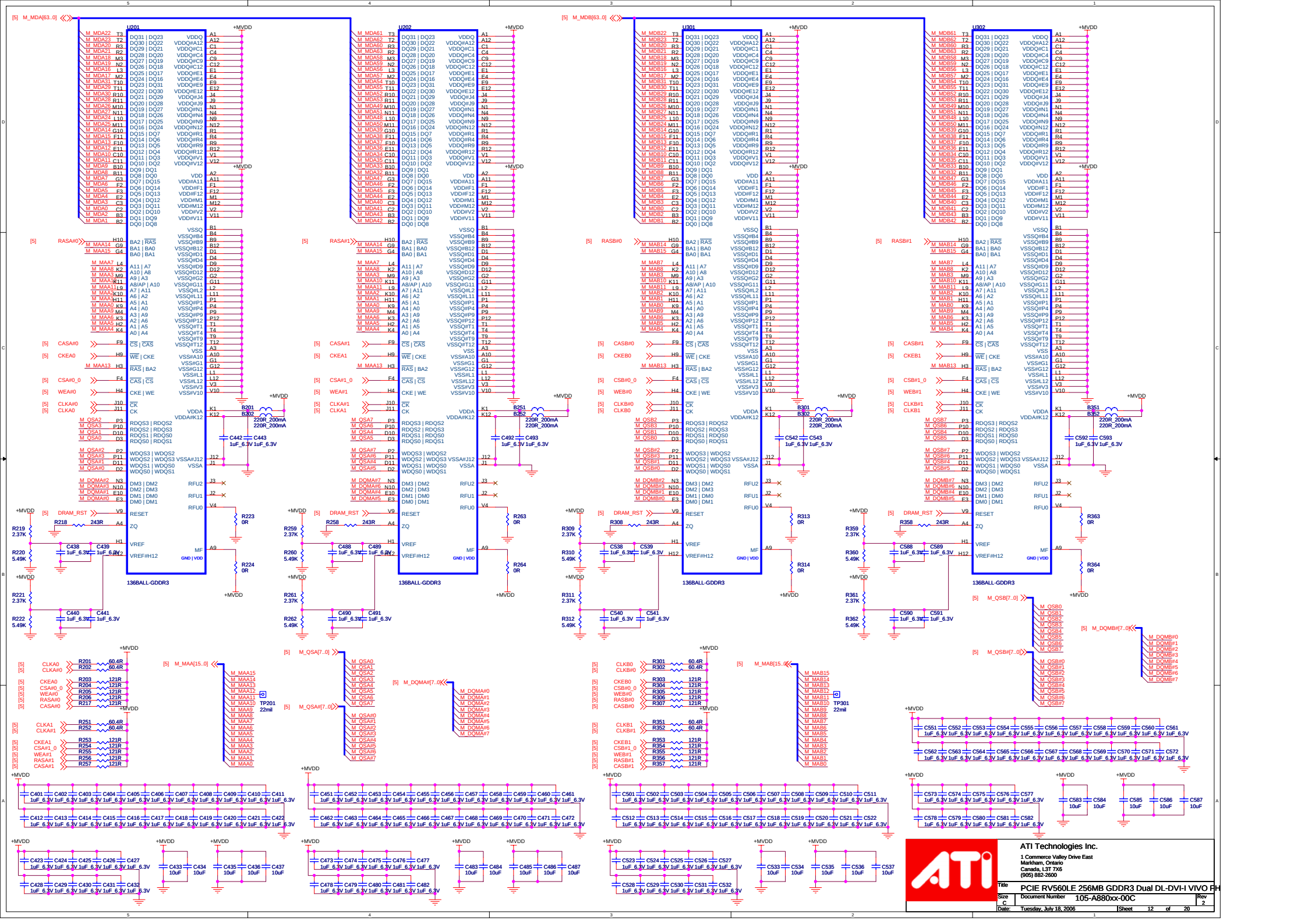
U201
U202
U301
U302
136BALL-GDDR3
M_MDA[63..0]
M_MDB[63..0]
RASA#0
RASA#1
RASB#0
RASB#1
CASA#0
CASA#1
CASB#0
CASB#1
CKEA0
CKEA1
CKEB0
CKEB1
WEA#0
WEA#1
WEB#0
WEB#1
CSA#0_0
CSA#1_0
CSB#0_0
CSB#1_0
CLKA0
CLKA#0
CLKA1
CLKA#1
CLKB0
CLKB#0
CLKB1
CLKB#1
DRAM_RST
M_MAA[15..0]
M_MAB[15..0]
M_QSA[7..0]
M_QSB[7..0]
M_DQMA#[7..0]
M_DQMB#[7..0]
TP201
TP301
22mil
+MVDD
220R_200mA
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Title
PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH
Size
C
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12
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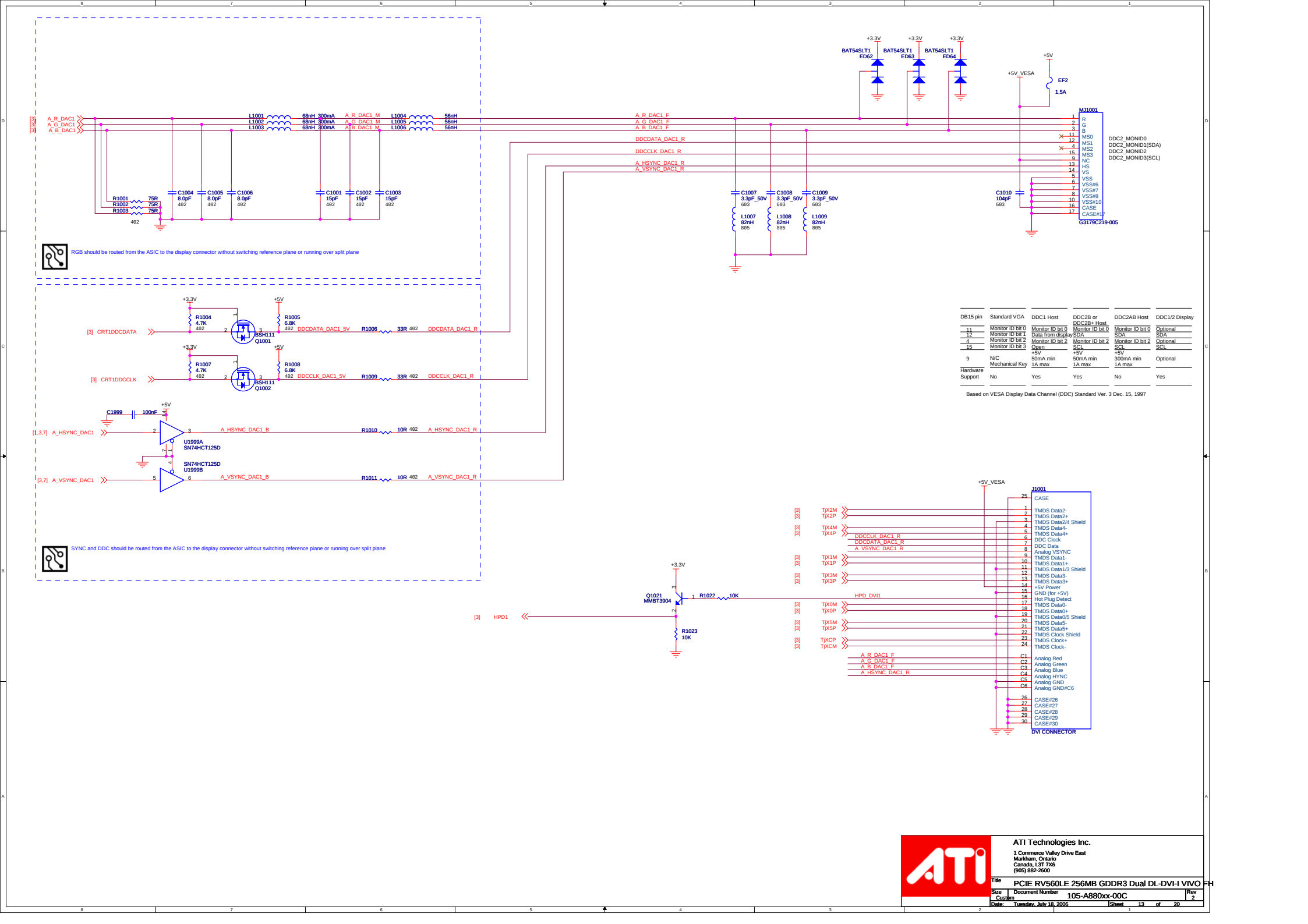
20



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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Size: Custom	Document Number: 105-A880xx-00C	Rev: 2
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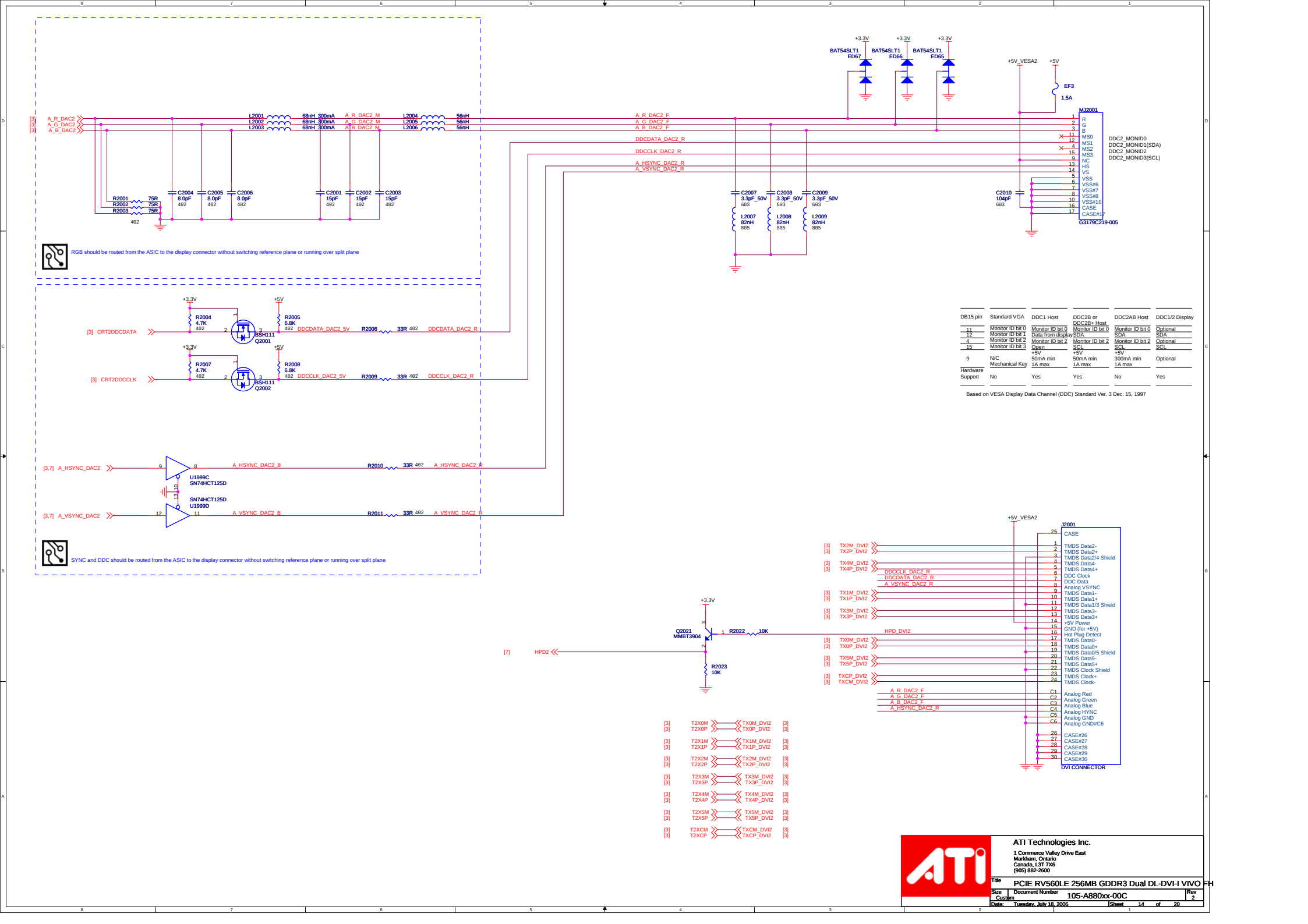

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH	
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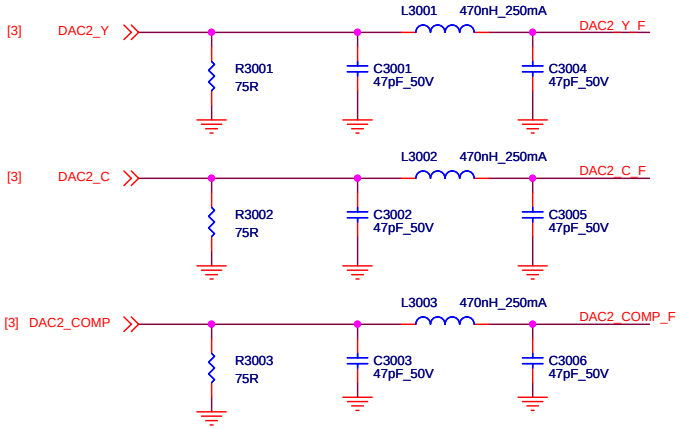
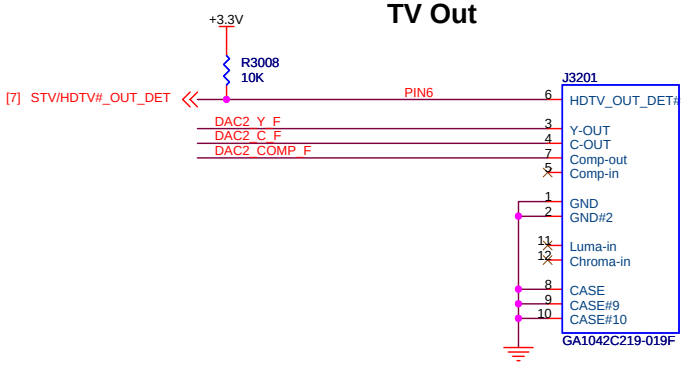


TV Out



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Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH	
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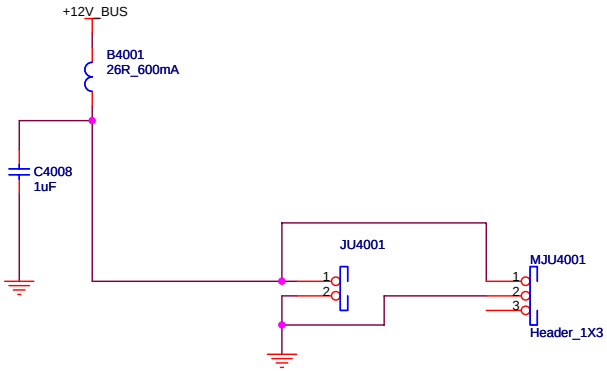

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Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH	
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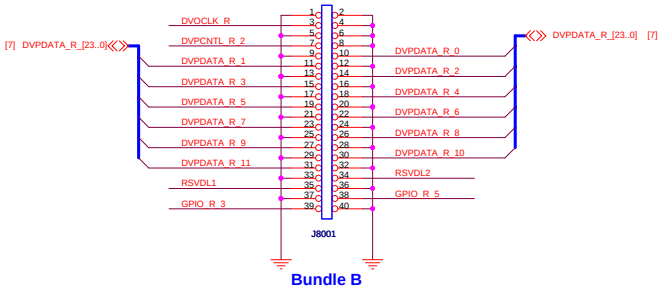
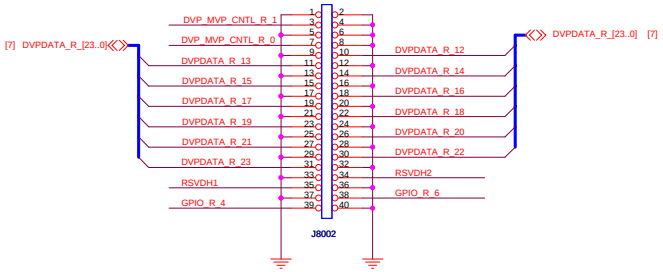
CrossFire Card-Edge

Lower Cable Card Edge

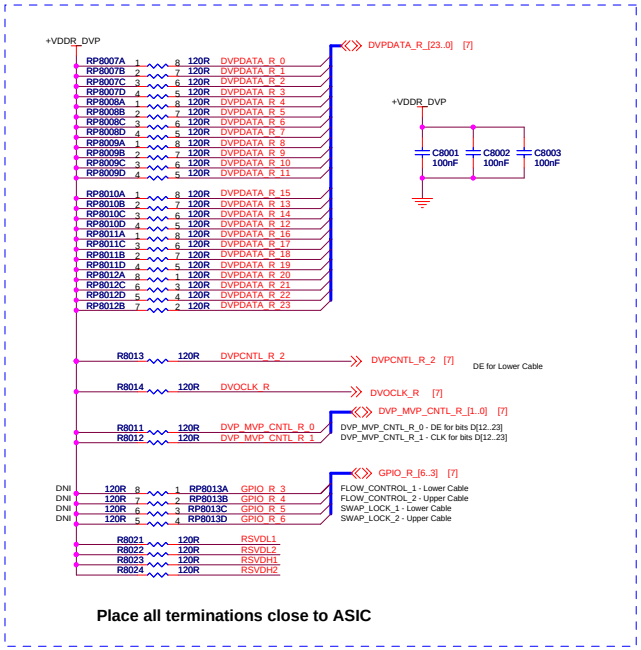


Bundle B

Upper Cable Card Edge



Bundle A



Place all terminations close to ASIC

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DVI/VGA SCREWS

ASSY-SCREW1
SCREW
JACKSCREW
<3rd part field>
7020000800

ASSY-SCREW2
SCREW
JACKSCREW
<3rd part field>
7020000800

ASSY-SCREW5
SCREW
PAN_HEAD
7020001700

ASSY-SCREW3
SCREW
JACKSCREW
<3rd part field>
7020000800

ASSY-SCREW4
SCREW
JACKSCREW
<3rd part field>
7020000800

MT1
MT_Hole_0.136_in.

MT2
MT_Hole_0.136_in_6VIA

DNI

SK1
RV410SOCKET

PCB1
RV410SOCKET

FM1
SW_FB

FM5
SW_FB

FM2
SW_FB

FM6
SW_FB

FM3
SW_FB

FM4
SW_FB

J1
X_PIN1*2

J4
X_PIN1*2

J7
X_PIN1*2

J2
X_PIN1*2

J5
X_PIN1*2

J8
X_PIN1*2

J3
X_PIN1*2

J6
X_PIN1*2

J9
X_PIN1*2

<Variant Name>

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Title: PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH

Size: C | Document Number: 105-A880xx-00C | Rev: 2

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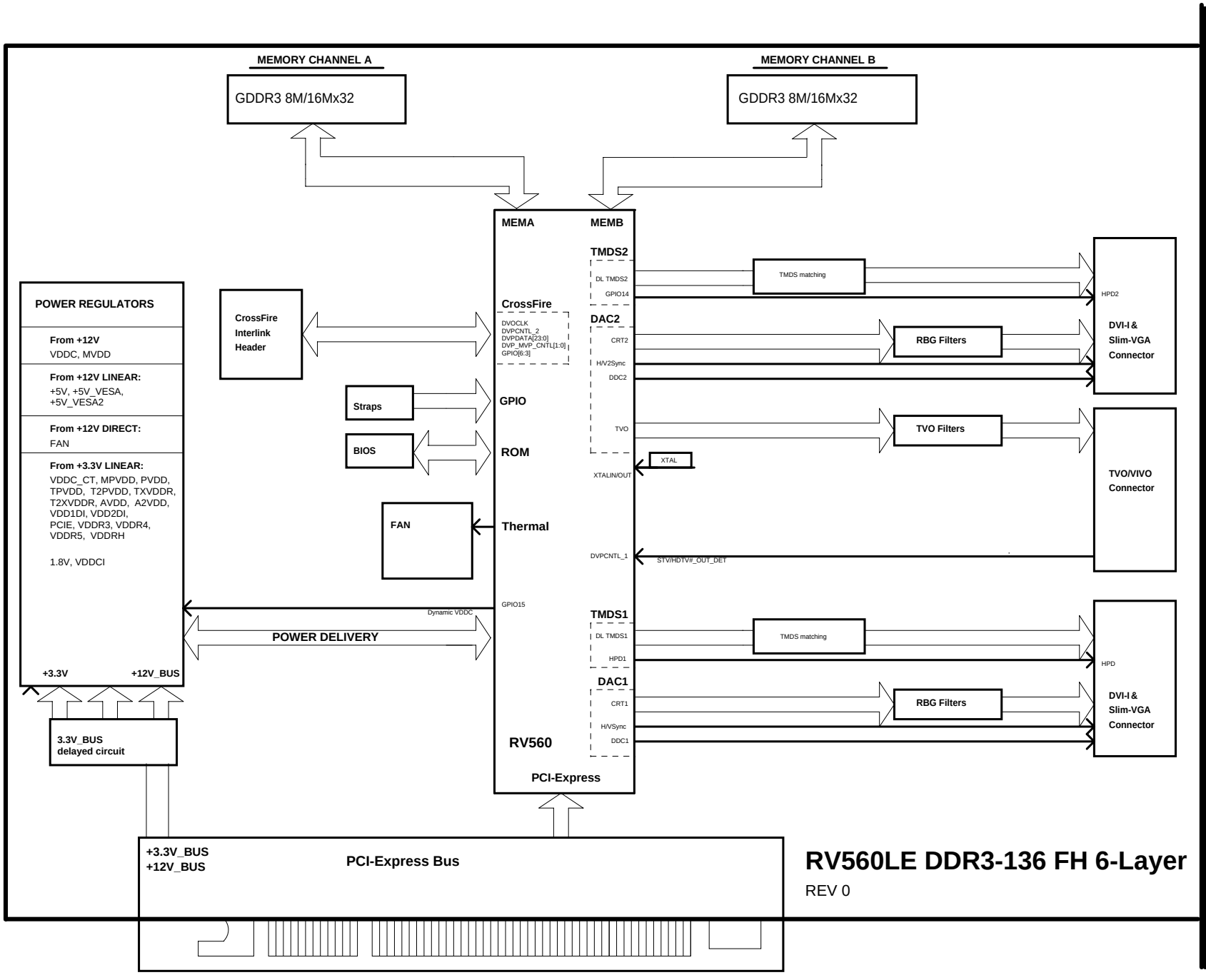

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<variant Name>

Title	Schematic No.	Date:
PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO FH	105-A880xx-00C	Thursday, July 13, 2006

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.**

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/02/27	Design based on 105/109-A671xx-20 (pg 03) Change TMDS power decouplings, change crystal/oscillator sharing circuit (pg 04) Change VDDR4/VDDR5 to have 1.8V/3.3V option , Separate VDDCI from VDDC option, add decoupling for VDDC and VDDCI (pg 07) Connect DVO to CrossFire Edge Connector, change pin straps matching RV570, remove PAL/NTSC header, H/W FPGA Crossfire (pg 08) New SMPS Tile (A800-00A-46) for RV560 VDDC 46A solution (pg 09) New SMPS Tile (A800-00A-30_VT) for RV560 VDDC 30A solution (pg 10) New SMPS Tile (A800-00A-8) for RV560 MVDD 8A solution (pg 11) Remove 1.8V regulator, LED for Dyn. VDDC, add VDDCI regulator (pg 12) Improve power sequencing and +5V sequencing from +5V_SMPS, add LDO new footprints, remove MVDD to 2.5V short (pg 13) Remove +5V_EN, change +5V to +5V_SMPS with current up to 115mA, add VDDC output current monitoring for debugging (pg 15) Remove H/W FPGA CrossFile options, change ESD protection to +5V_VESA (pg 16) Remove H/W FPGA CrossFile options and chnage ESD protetion to +5V_VESA2 (pg 17) Change RTAVDD regulator for power sequencing, add Dell specific TVO mapping (pg 18) Update fan control for other thermal monitoring IC options (pg 19) Add CrossFire Edge Connectors and 1.8V regulator
1	00B	06/03/06	Fix DFM issues on layout (pg 03/07) Add clock source to GenericA/B for ASIC debugging (pg 13) Add J601 for ease of bring up for VDDC current monitoring
2	00C	06/05/08	(pg 03) Add MR25 and C61 for VREFG (pg 03) Change GND_TXVSSR and GND_T2XVSSR directly to GND (pg 08) Remove VR650, VR663, MR676, MR677, MR673, MU678 and U678, modify BUSEN and share it to MU601 (pg 08) Remove redundant external detection circuits (pg 11) Replace RP801 with B801~B803 (pg 11) Add resistors to dissipate Q_MVDD, sourced from 3.3V_BUS (pg 12) Add RP952 for PCIE VDDC share, add 5V_EN, remove Q998 for RTAVDD_ENb (pg 13) Add Q922 for improved power dissipation, use series R926~R928 dissipation and add 5V_EN option (pg 17) Replace RTAVDD regulator with AP1118 (pg 19) Crossfire pin mapping change, 50R impedance matched (Layout) Power distribution layout change (Layout) TMDS1 and TMDS2 termination resistor changes

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Title	RV560LE 256MB GDDR3 VGA VIVO DVI-I (DL-TMDS1+DAC2) FH	
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