<variant Name>

Title

RH RV610 128MB DDR2-BGA84 16MX16 VO dDVI

Schematic No.

105-B170xx-00

Date:

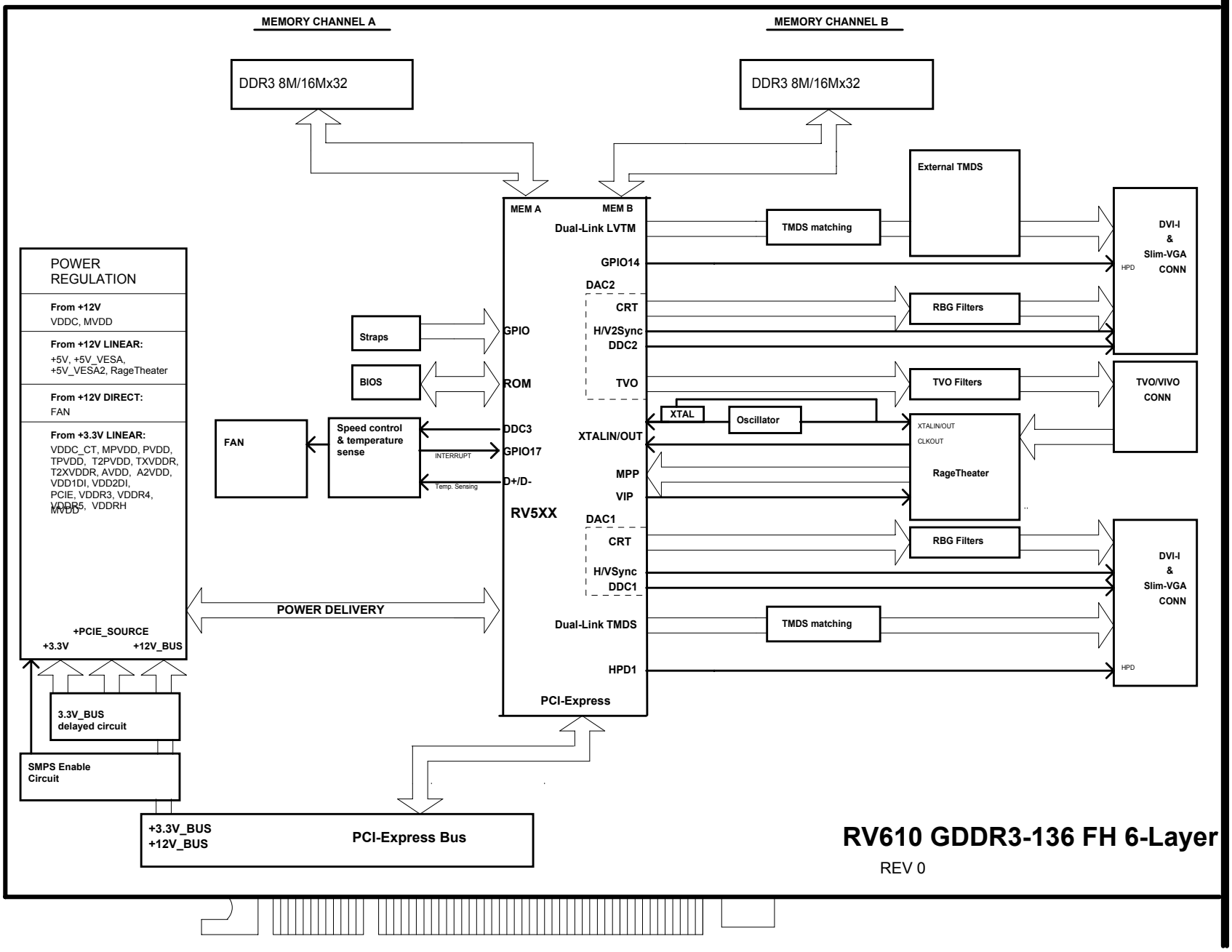
Friday, April 27, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.

Rev 21

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
014	00B	2007.02.22	RM C890/MC890, RM B801/L801/ML801
015	00B	2007.02.27	ADD R4010 FOR FAN CIRCUIT. ADD STITCHING CAPS C300, C301, C302, C303
016	00B	2007.02.28	CORRECT "300" TO C300; ADD C304, CHNG C301;
017	00B	2007.03.06	POWER SUPPLY CHANGES: ADD MC627, R615, R609, R715, R709, R714, R614; REMOVE MC630, MC624;
018	00B	2007.03.06	DUE TO LAYOUT CONSTRAINTS: RM ML601. CHANGE C627, MC627.
019	00C	2007.04.17	REMOVE R90, Q90 (A12+ ASIC REMOVES NEED FOR THESE PARTS); REMOVE C850 (IS NOT POPULATED ON ANY BOM - WILL CAUSE VDDC TO BE UNSTABLE); ADD C4010 (FOR FAN SPIN UP);
020	00C	2007.04.19	ADD C490, C491, C492 FOR POSSIBLE MEMORY SIGNAL INTEGRITY/EMI IMPROVEMENTS (PER EMI TEAM);
021	00	2007.04.25	NO NETLIST/LAYOUT CHANGES. SCHEMATIC UPDATE NOTES p.12 (V2SYNC/GPIO_18 CLARIFICATION)



RV610 GDDR3-136 FH 6-Layer

REV 0

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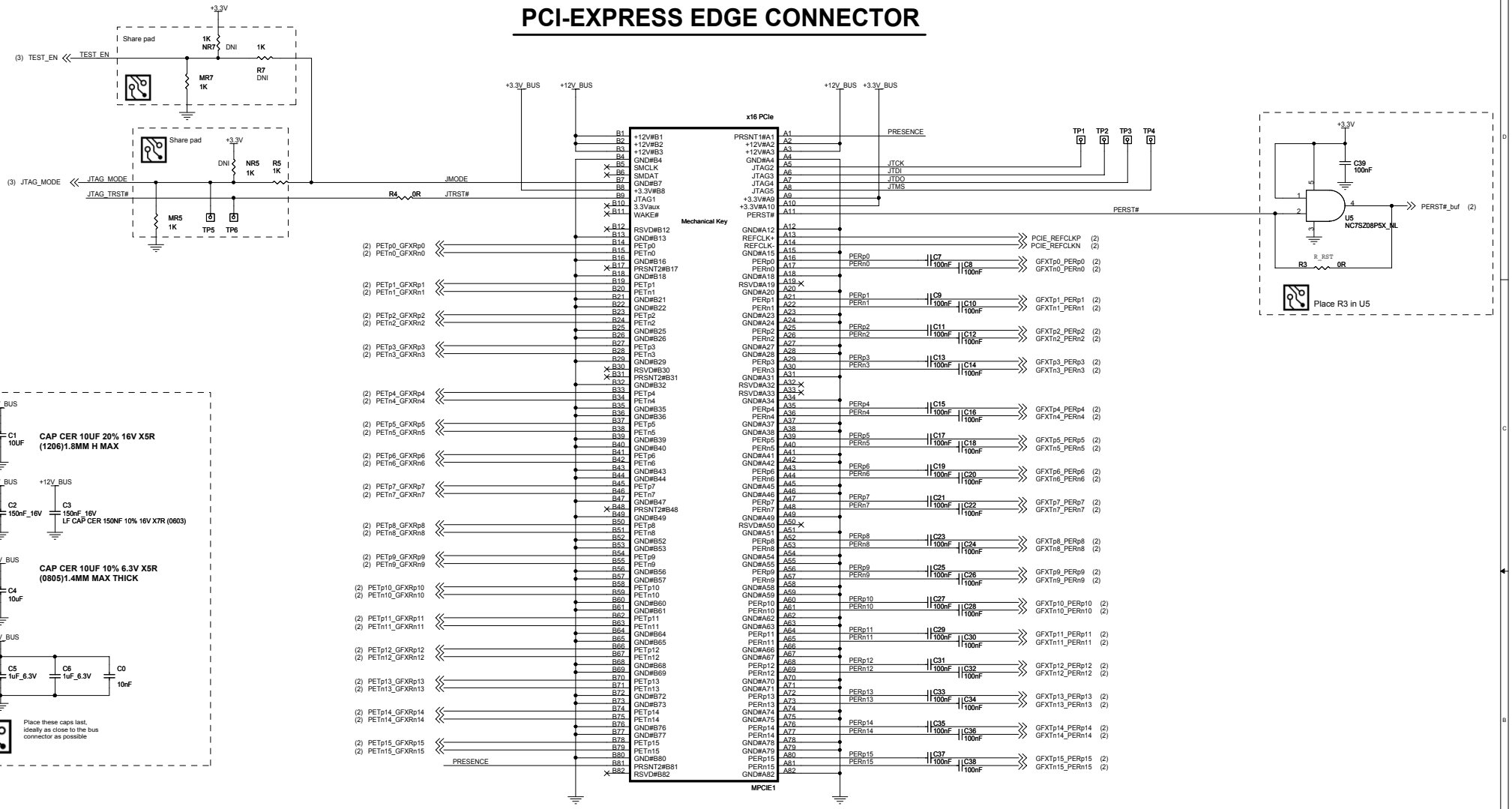
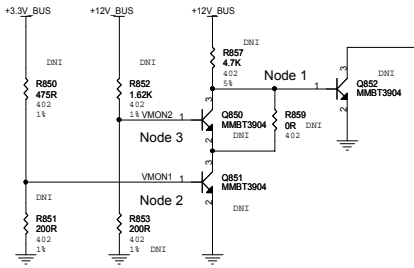
PCI-EXPRESS EDGE CONNECTOR





Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.

Node 1 When +12V_BUS ramps above min Vbe, SMPS_EN will be held low

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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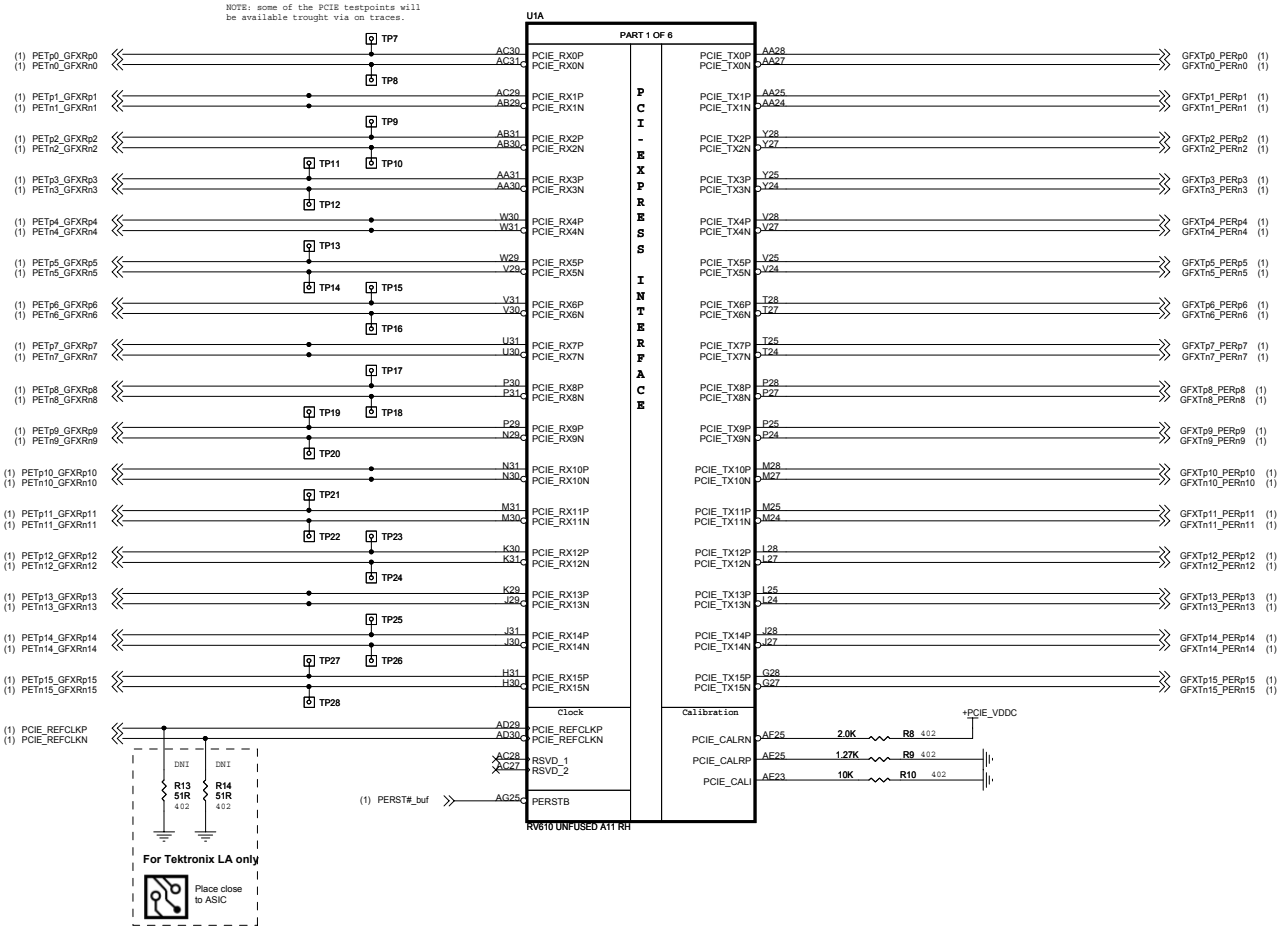

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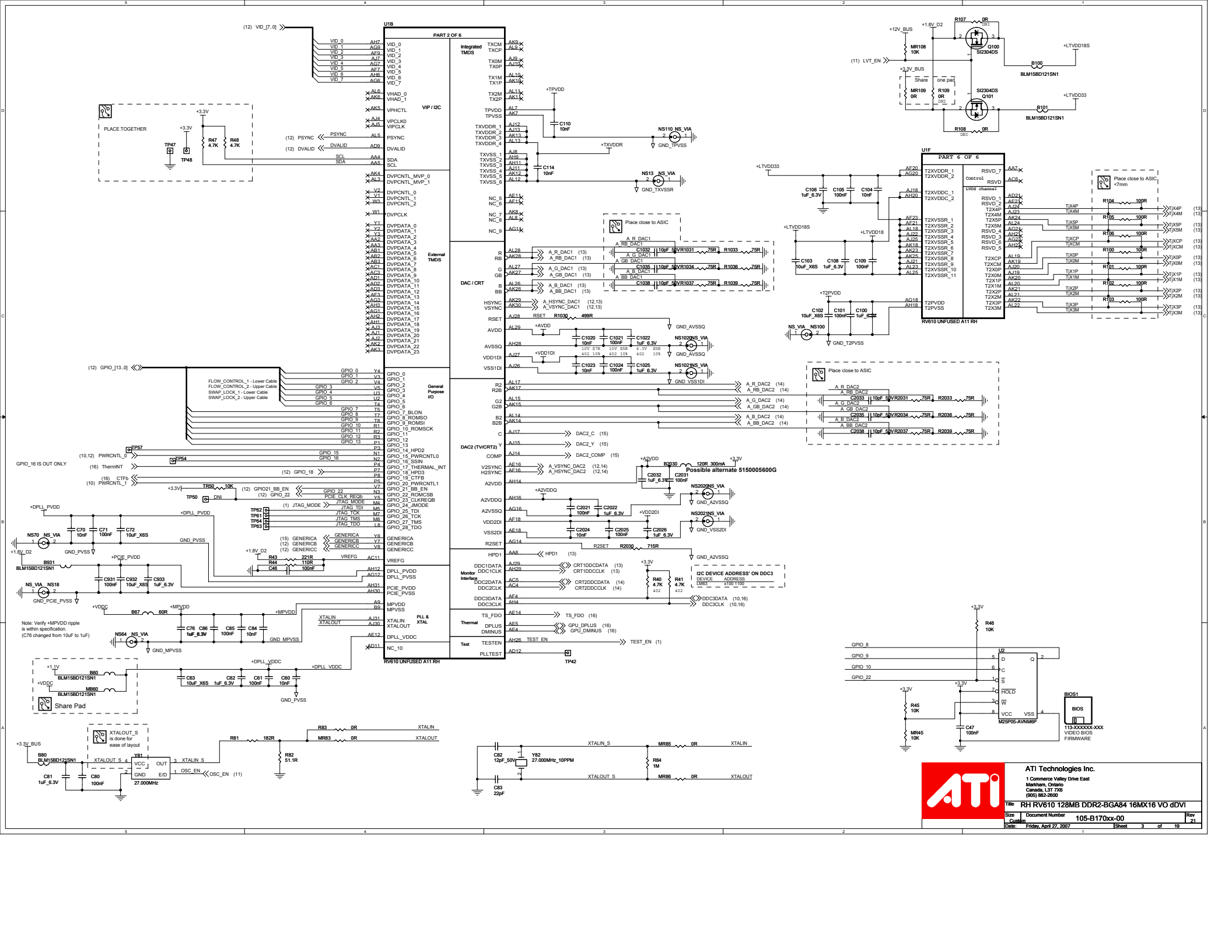
U1B
PART 2 OF 6
RV610 UNFUSED A11 RH
U1F
PART 6 OF 6
RV610 UNFUSED A11 RH
VID / I2C
External TMDS
DAC / CRT
General Purpose I/O
DAC2 (TV/CRT2)
Monitor Interface
PLL & XTAL
Thermal
Test
Integrated TMDS
LVDS channel
Control
PLACE TOGETHER
Share Pad
Possible alternate 5150005600G
I2C DEVICE ADDRESS' ON DDC3
BIOS
M25P05-AVNM6P
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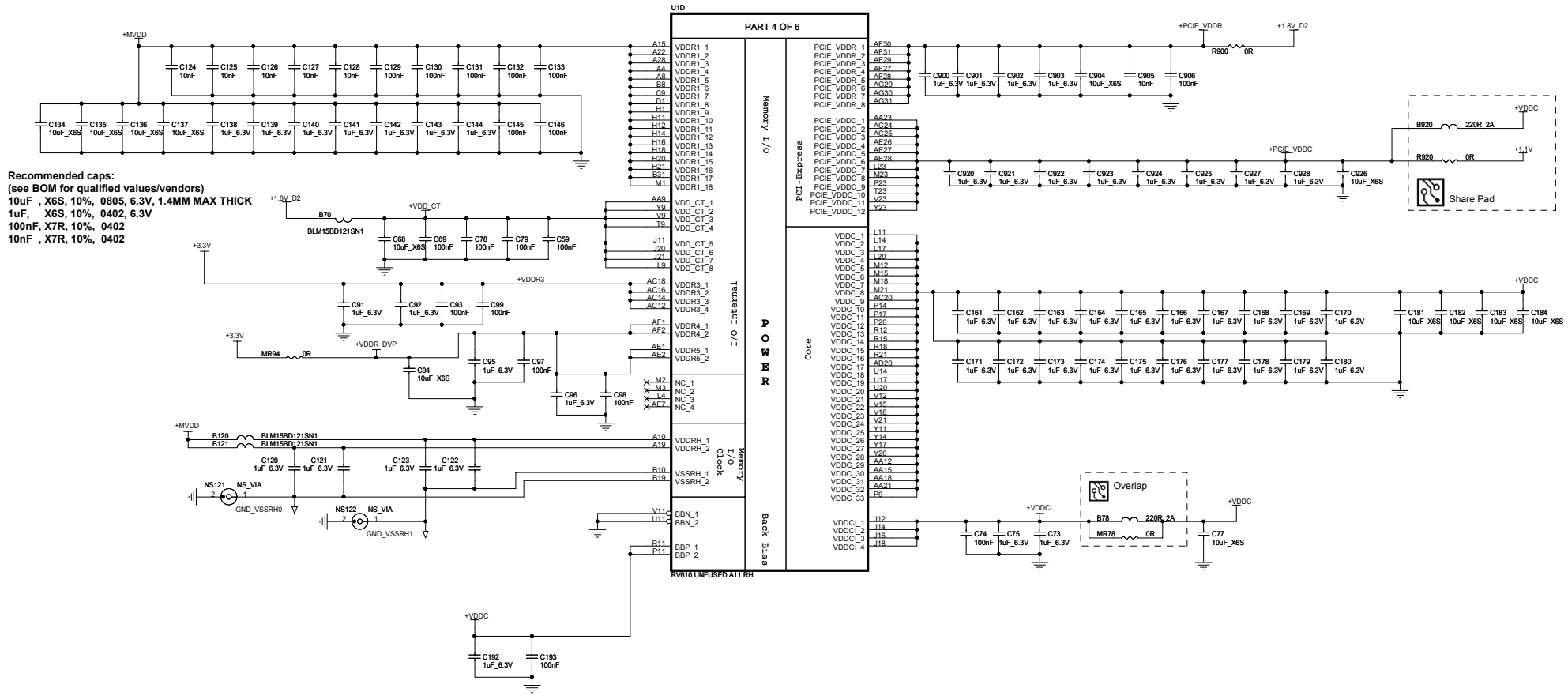

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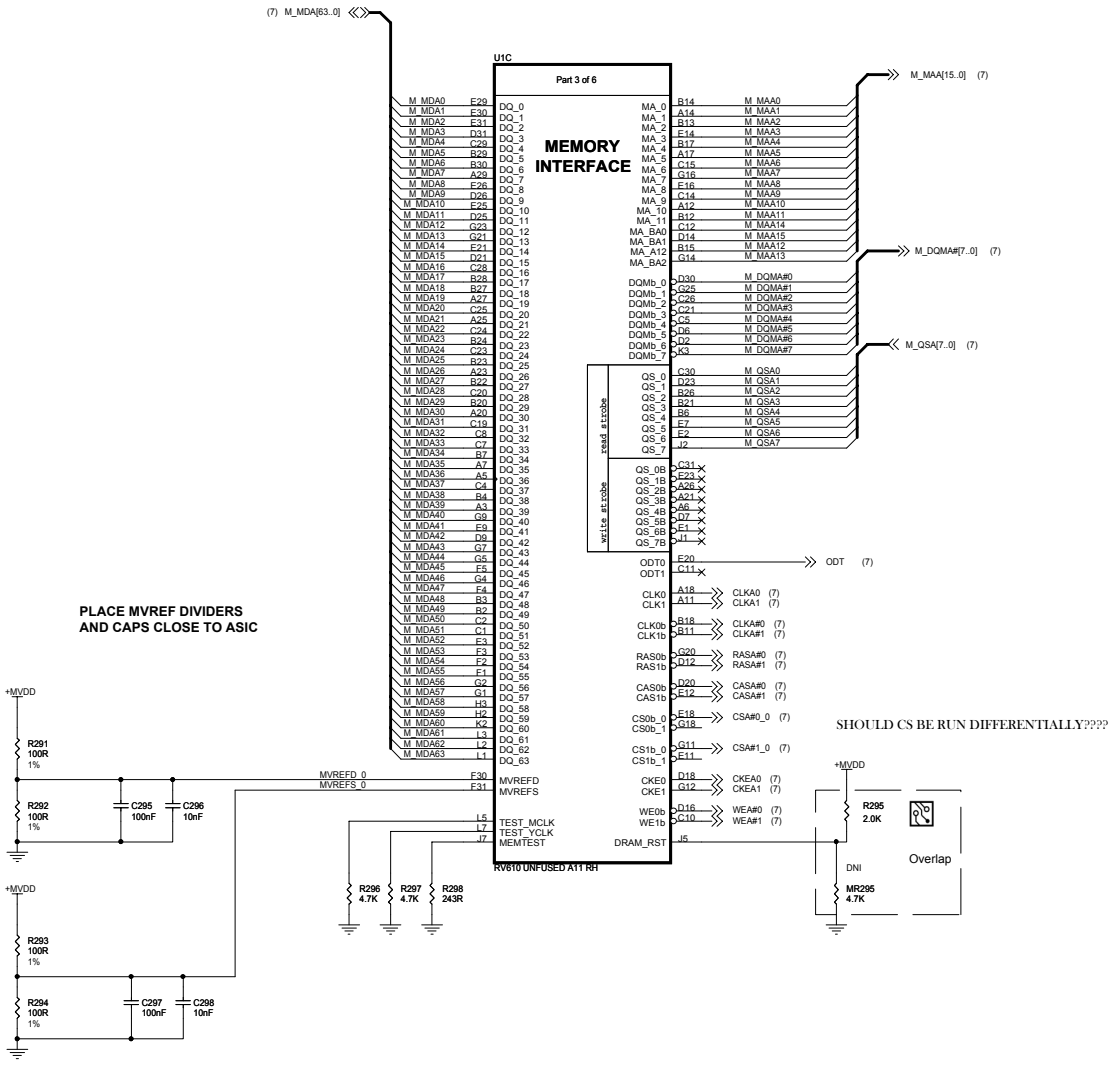

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

SHOULD CS BE RUN DIFFERENTIALLY????

DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

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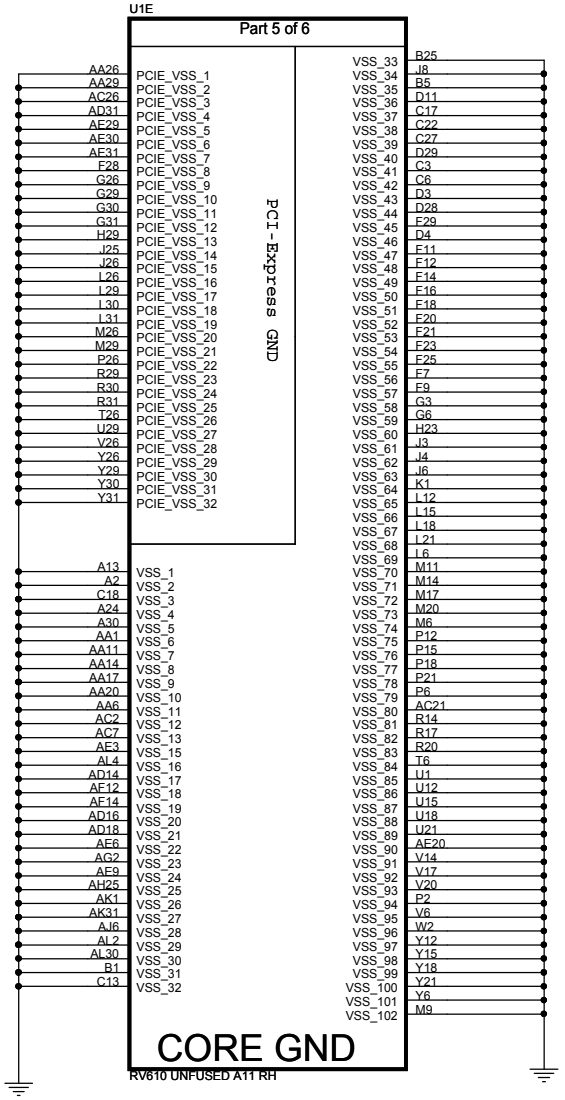

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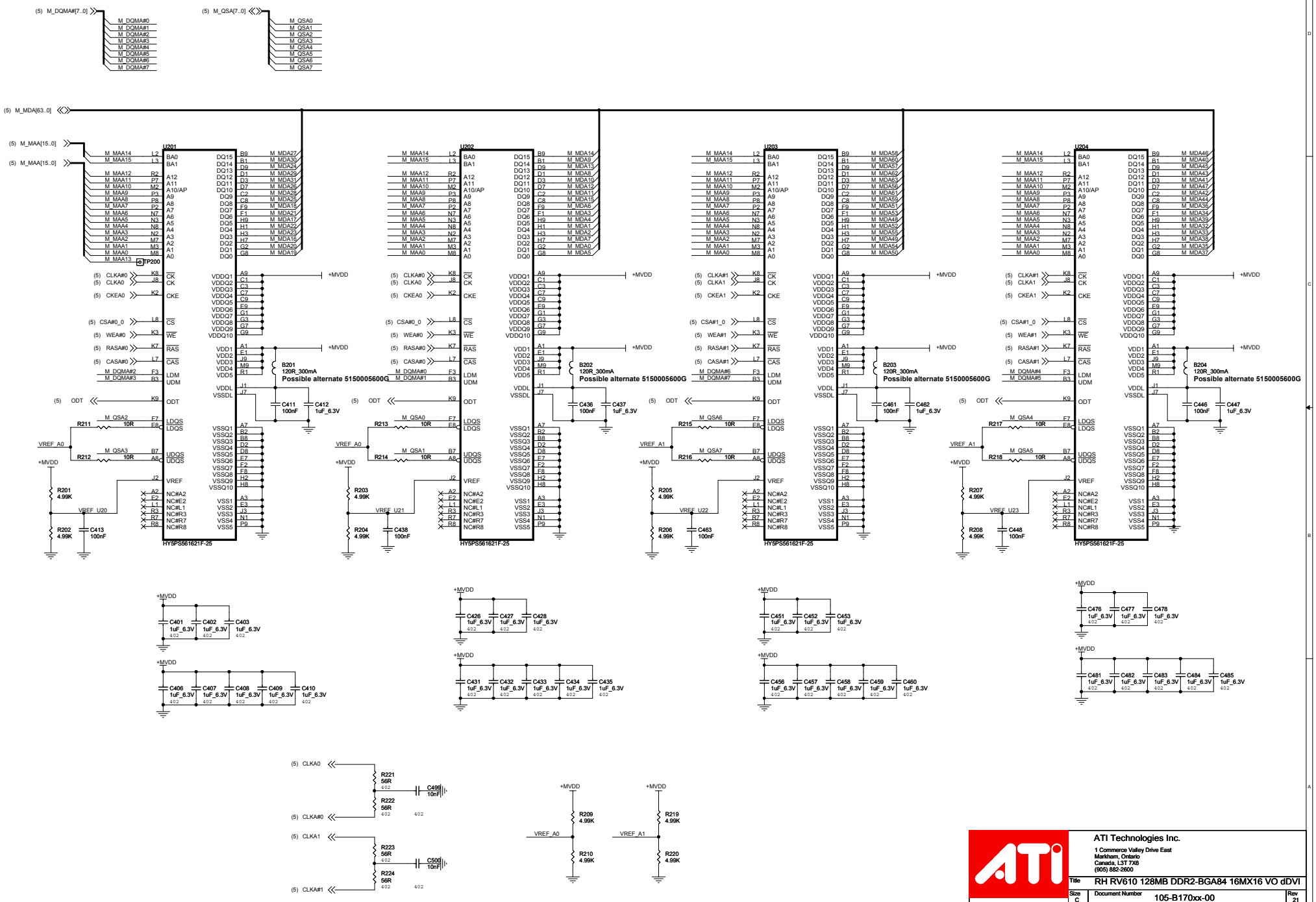
CHANNEL A: RANK 0 128MB DDR2



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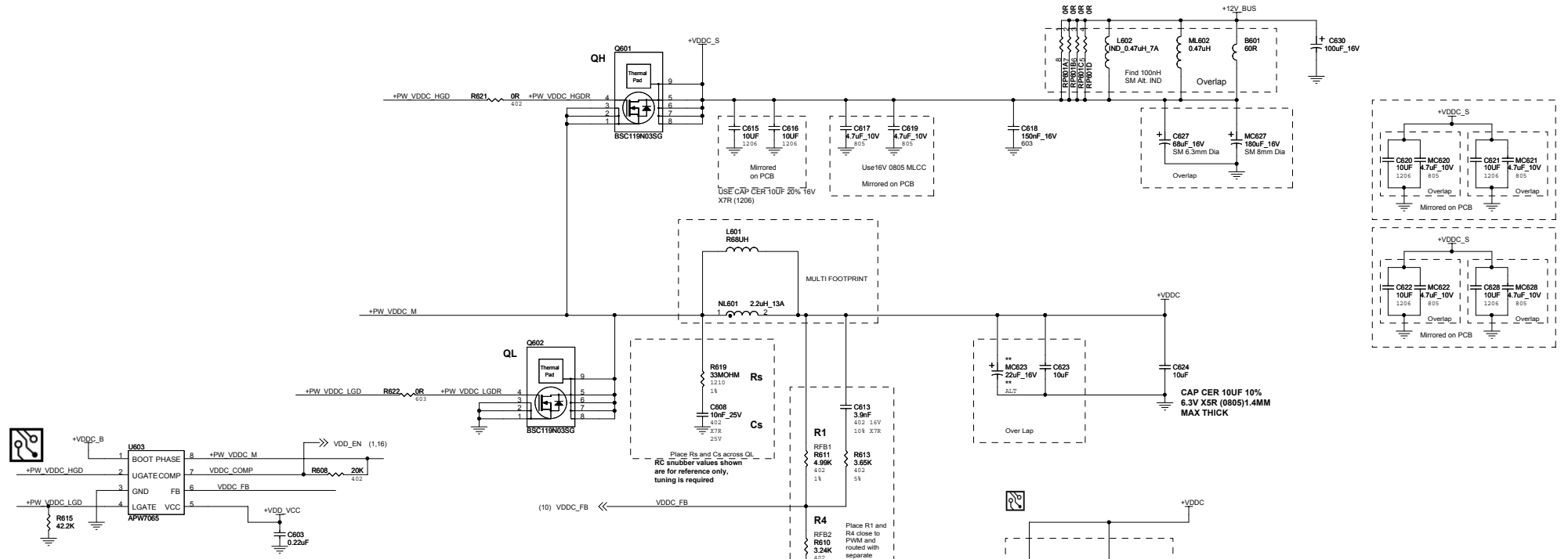


List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7120/APW7065 (12V)
CAT CAT7583 (12V)
INTERSIL ISL6545
NEXSEM NX2114/2307
RICHTEK RT9214/RT8101
OnSemi ON1582
uPI UP6101 (No Ext_Vref in)

Layout guideline for Nexsem NX2114/2307

1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW_MVDDC_LGD and PW_MVDDC_HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

SMPS02- Regulator for VDDC

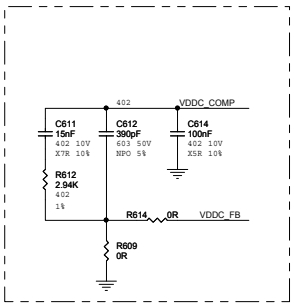
Vout = 0.9V ~ 1.1V

Part	Vout	RFB1	RFB2
0.8V Ref	1.1V (1.98V~2.08V)	200R p/n 3160200000G	511R p/n 3160511000G
	1.1V (1.10V~1.14V)	10K p/n 3160100200G	24.9K p/n 3160249200G

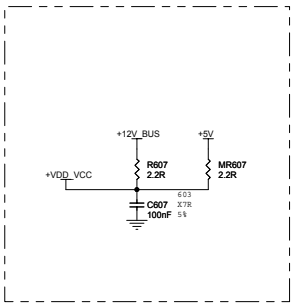
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

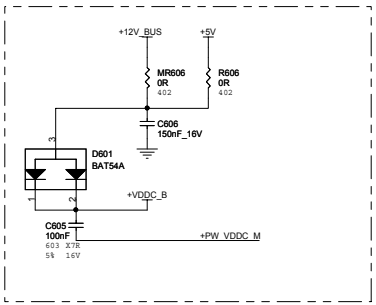
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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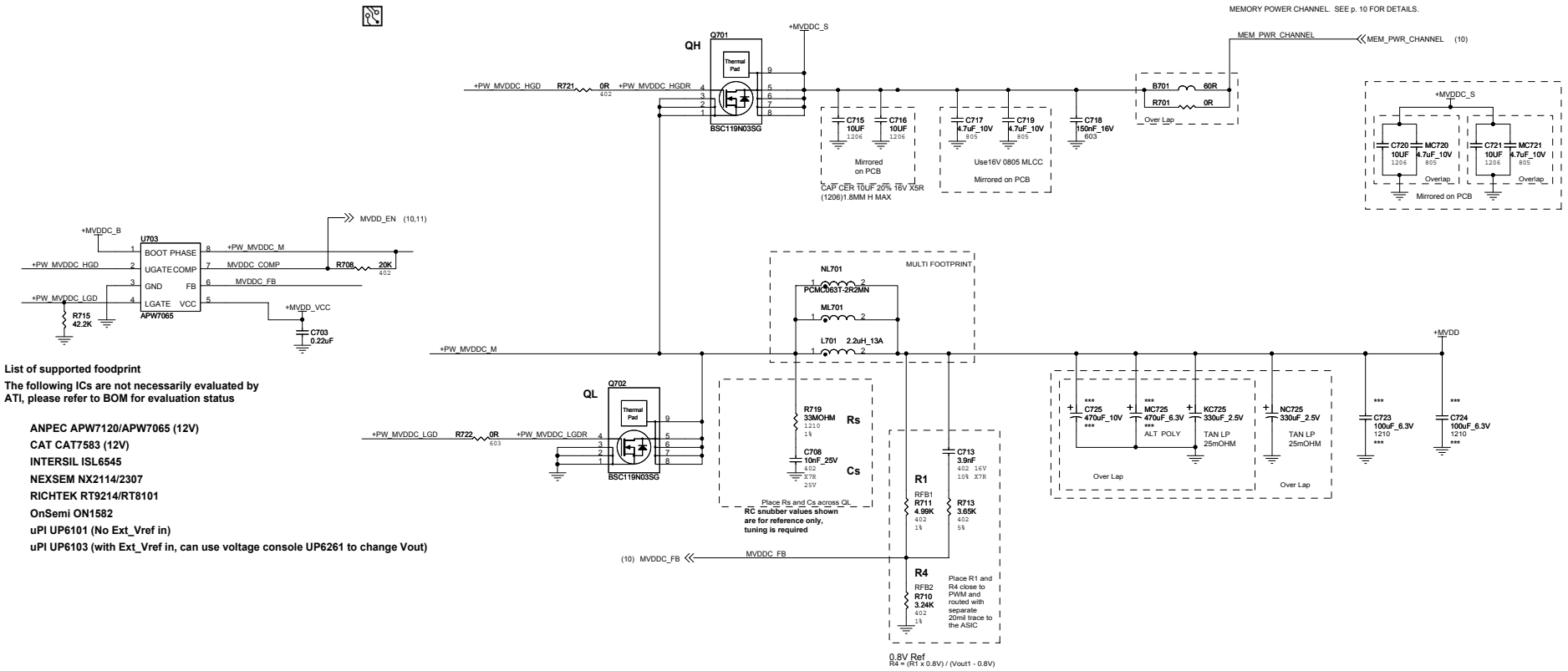

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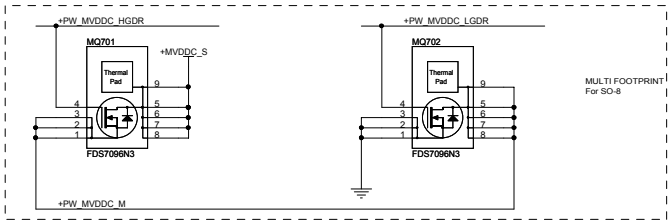
- **RICHTEK RT9214/RT8101**
- **OnSemi ON1582**
- **uPI UP6101 (No Ext_Vref in)**
- **uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**



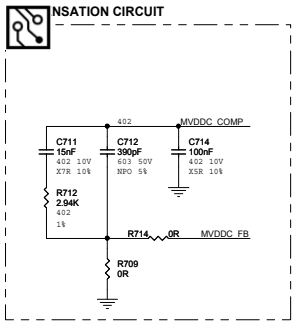
SMPS02- Regulator for MVDD

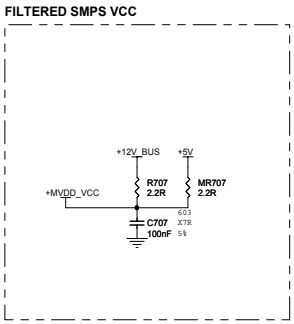
Vout = 1.8V ~ 2.85V

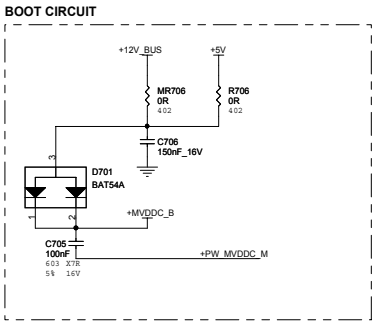
Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G
	1.8V (1.78V~1.86V)	4.99K p/n 3160499100G	3.92K p/n 3160392100G

SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		







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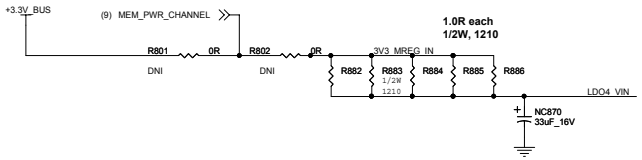
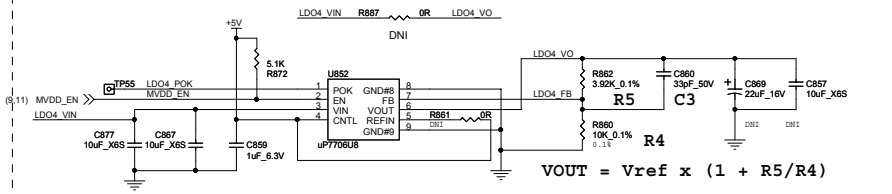
Linear Regulator for +MVDD
Vout = 1.8V ~ 2.1V
Iout = 2.75A MAX
P_REG = 1.35W
Tj(rise)max = 1.35Wx50C/W(50~70mm sq. Cu) = 67.5C

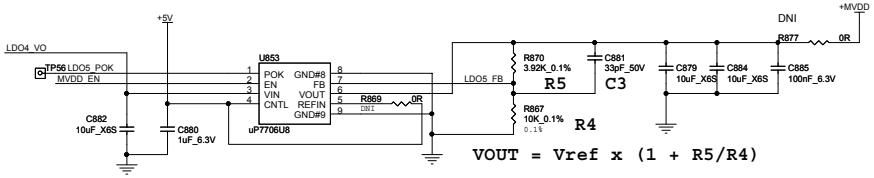
MEM PWR INPUT	INSTALL	DO NOT INSTALL
3.3V BUS (3V3_BUS_F)	R801 R802	R602 R701 or B701
12V (+VDDC_S)	R602 R701 or B701	R801 R802

Req = 1R/5 = 0.2R
P_Req = 0.2R * 2.75^2 = 1.5W
P_Reach = 1.5W/5 = 300mW < 500mW * 70%

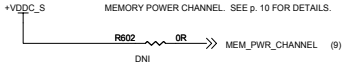
MEMORY POWER CHANNEL TO EASE LAYOUT CONGESTION OF LP BOARD. MEMORY POWER CHANNEL CAN BE USED TO DELIVER SOURCE VOLTAGE TO MVDD SMPS OR LINEAR REGULATORS (12V IN OR 3.3V IN)

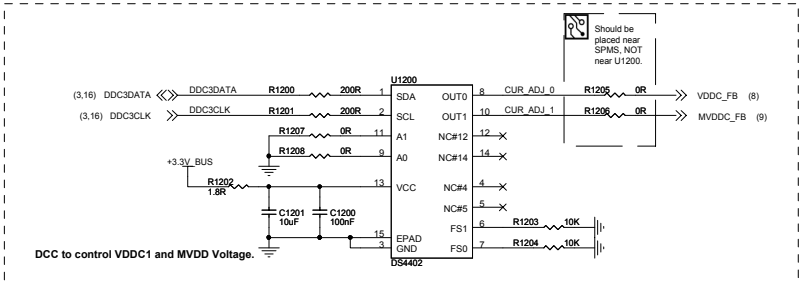






Memory Power Channel
Source Selection



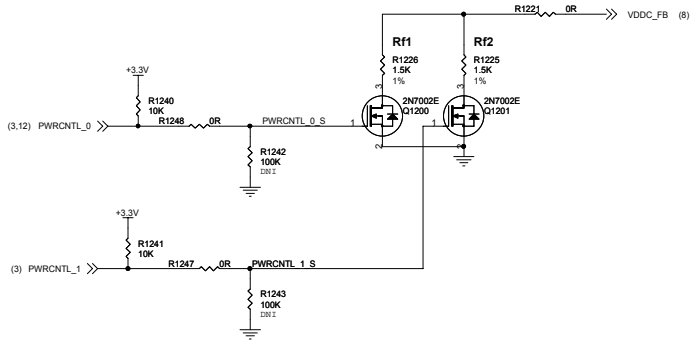


DCC to control VDDC1 and MVDD Voltage.

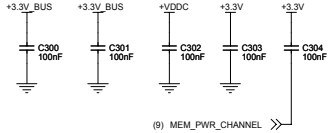
ASIC GPIO(x2) to control VDDC Voltage.

VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0	0				
0	1				
1	0				
1	1	1 0	1		Power-up Default



THESE ARE STITCHING CAPACITORS. THEIR PLACEMENT IS LAYOUT DEPENDANT.



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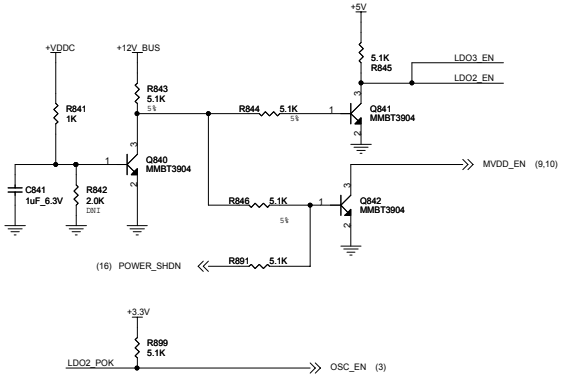
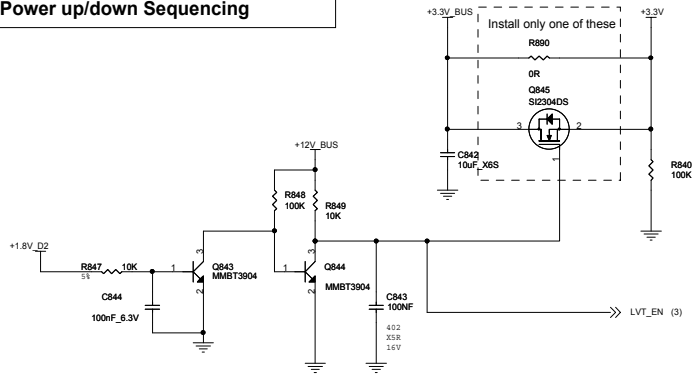
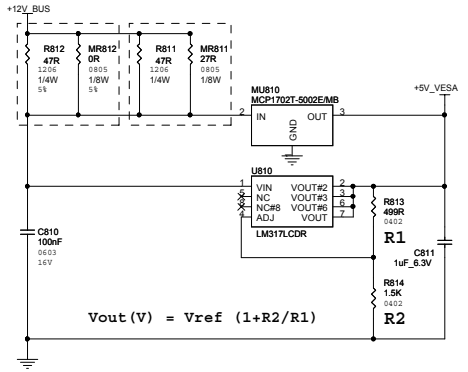
Power up/down Sequencing



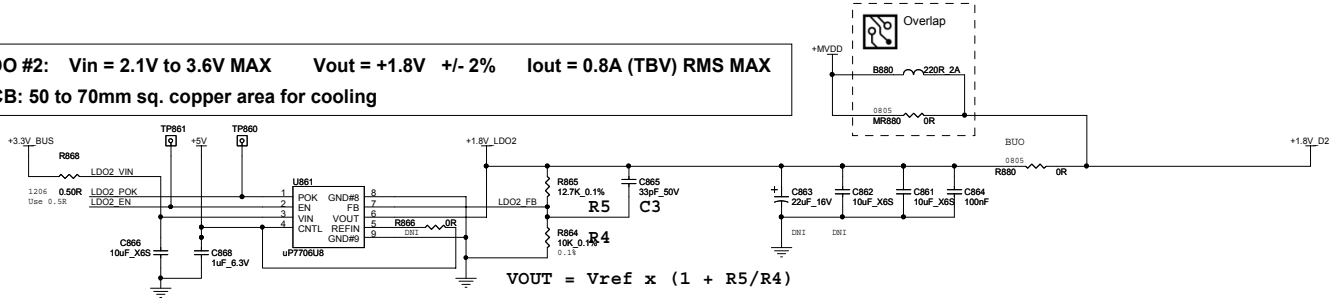


Regulators for +5V, +5V_VESA and +5V_VESA2



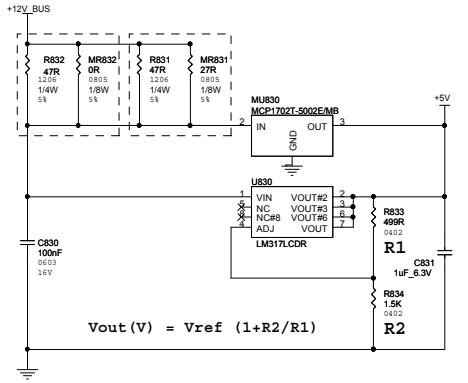
LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



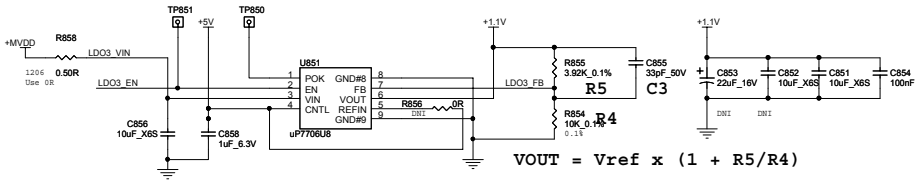
VOUT = Vref x (1 + R5/R4)

R868 (0.5R 1/2W or 0R 1206), R864, R865 & C865: To Be Verified



LDO #3: Vin = +1.45V to 2.1VMAX Vout = +1.1V +/- 2% Iout = 1.1A (TBV) RMS MAX

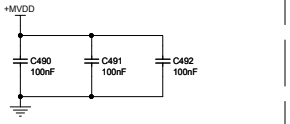
PCB: 50 to 70mm sq. copper area for cooling



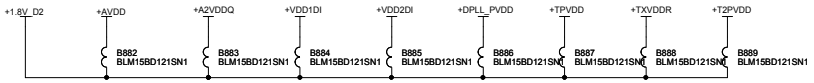
VOUT = Vref x (1 + R5/R4)

R854, R855 (3.92K) & C855: To Be Verified

Place C490-492 near layer transitions (top/bottom).
THIS IS LAYOUT DEPENDENT.



Shared Power Rails



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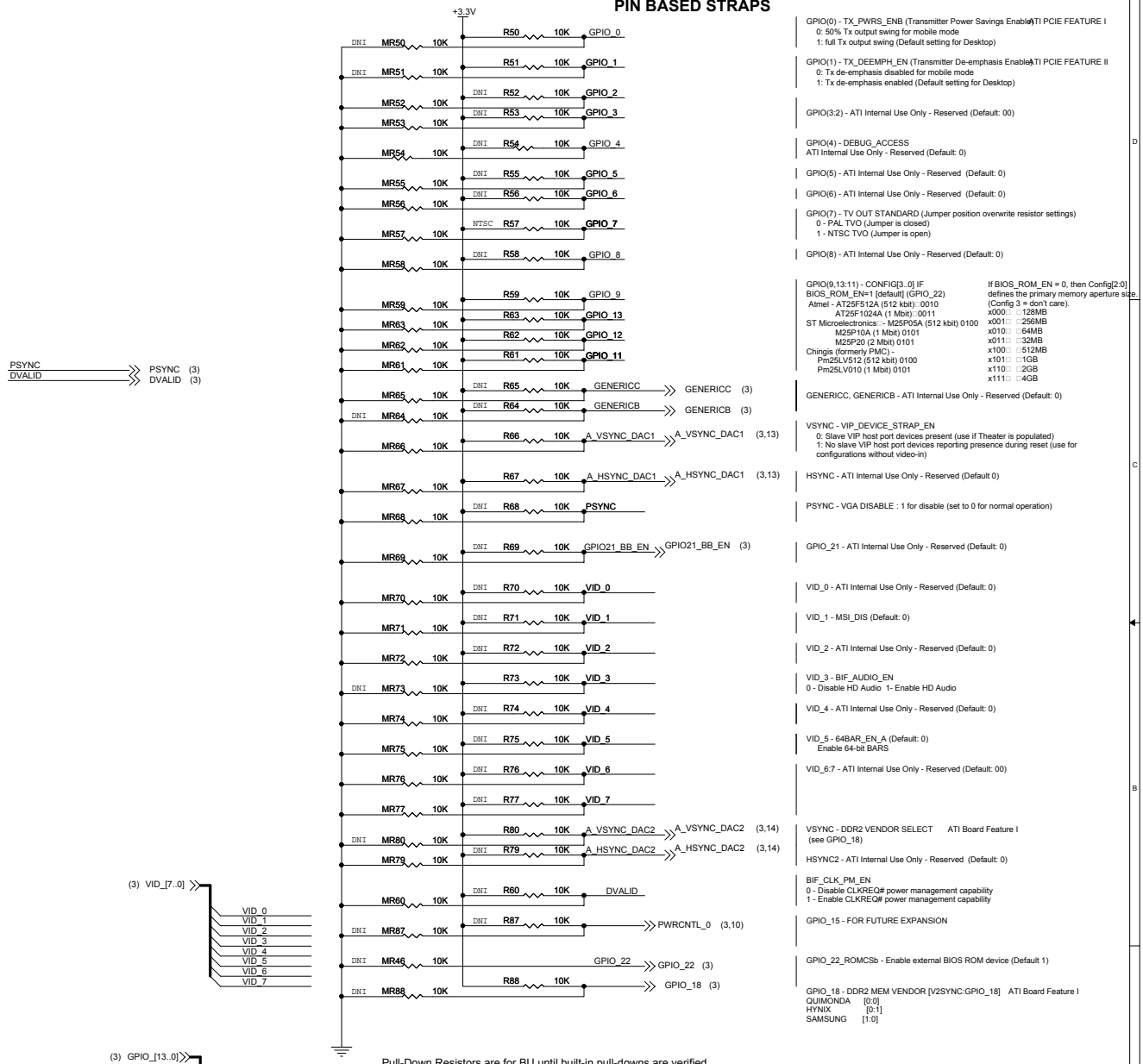
PIN BASED STRAPS



GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - ATI Internal Use Only - Reserved (Default: 00)

GPIO(4) - DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(7) - TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

GPIO(8) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0] IF BIOS_ROM_EN=1 [default] (GPIO_22)
Atmel - AT25F512A (512 kbit): 0010
AT25F1024A (1 Mbit): 0011
ST Microelectronics: M25P05A (512 kbit) 0100
M25P10A (1 Mbit) 0101
M25P20 (2 Mbit) 0101
Chingis (formerly PMC) -
Pm25LV512 (512 kbit) 0100
Pm25LV010 (1 Mbit) 0101

If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.
(Config 3 = don't care).
x000: 128MB
x001: 256MB
x010: 64MB
x011: 32MB
x100: 512MB
x101: 1GB
x110: 2GB
x111: 4GB

GENERICC, GENERICB - ATI Internal Use Only - Reserved (Default: 0)

VSYNC - VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - ATI Internal Use Only - Reserved (Default 0)

PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO_21 - ATI Internal Use Only - Reserved (Default: 0)

VID_0 - ATI Internal Use Only - Reserved (Default: 0)

VID_1 - MSI_DIS (Default: 0)

VID_2 - ATI Internal Use Only - Reserved (Default: 0)

VID_3 - BIF_AUDIO_EN
0 - Disable HD Audio 1- Enable HD Audio

VID_4 - ATI Internal Use Only - Reserved (Default: 0)

VID_5 - 64BAR_EN_A (Default: 0)
Enable 64-bit BARS

VID_6:7 - ATI Internal Use Only - Reserved (Default: 00)

VSYNC - DDR2 VENDOR SELECT ATI Board Feature I
(see GPIO_18)

HSYNC2 - ATI Internal Use Only - Reserved (Default: 0)

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

GPIO_15 - FOR FUTURE EXPANSION

GPIO_22_ROMCSb - Enable external BIOS ROM device (Default 1)

GPIO_18 - DDR2 MEM VENDOR [V2SYNC:GPIO_18] ATI Board Feature I
QUIMONDA [0:0]
HYNIX [0:1]
SAMSUNG [1:0]

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground High logic voltage

Signal

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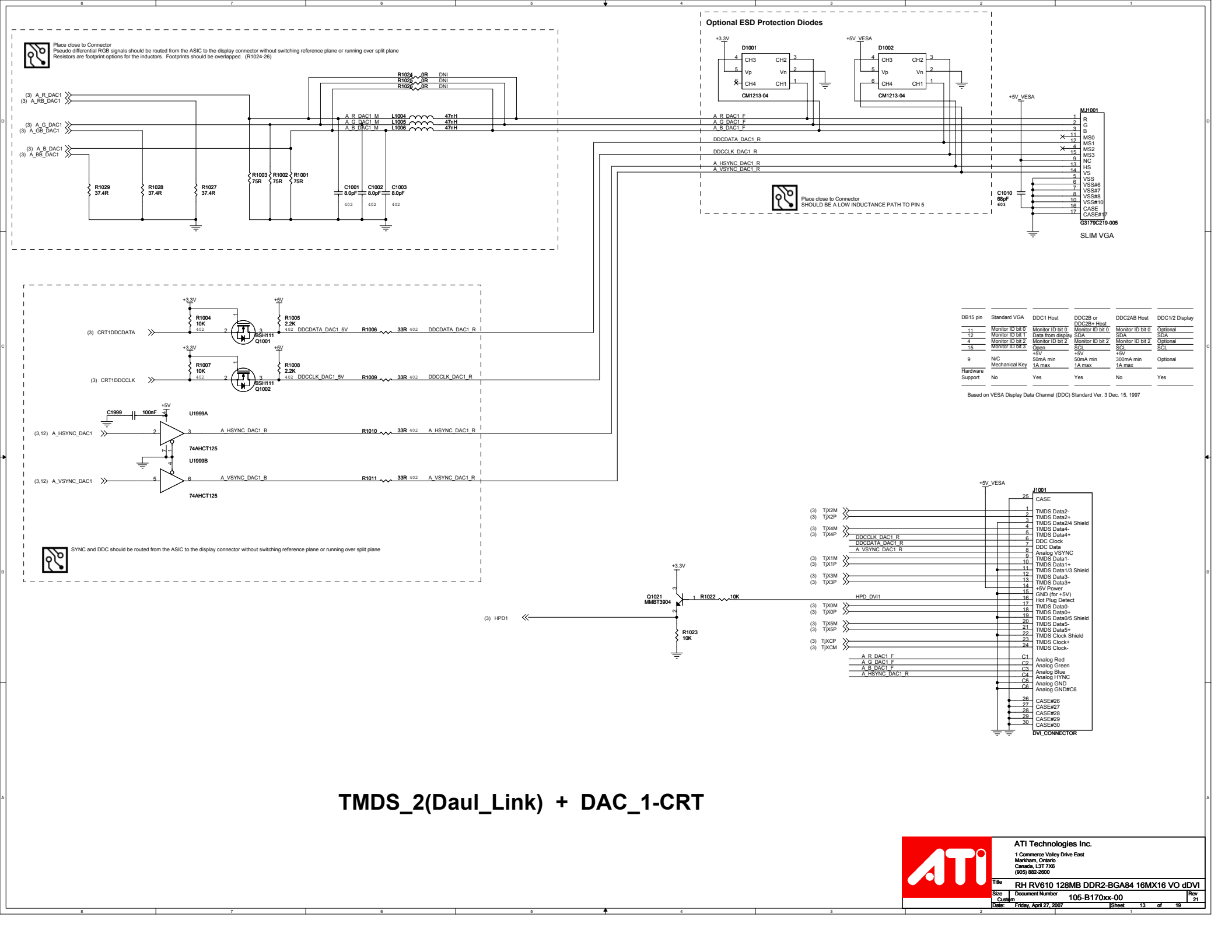

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

TMDS_2(Daul_Link) + DAC_1-CRT

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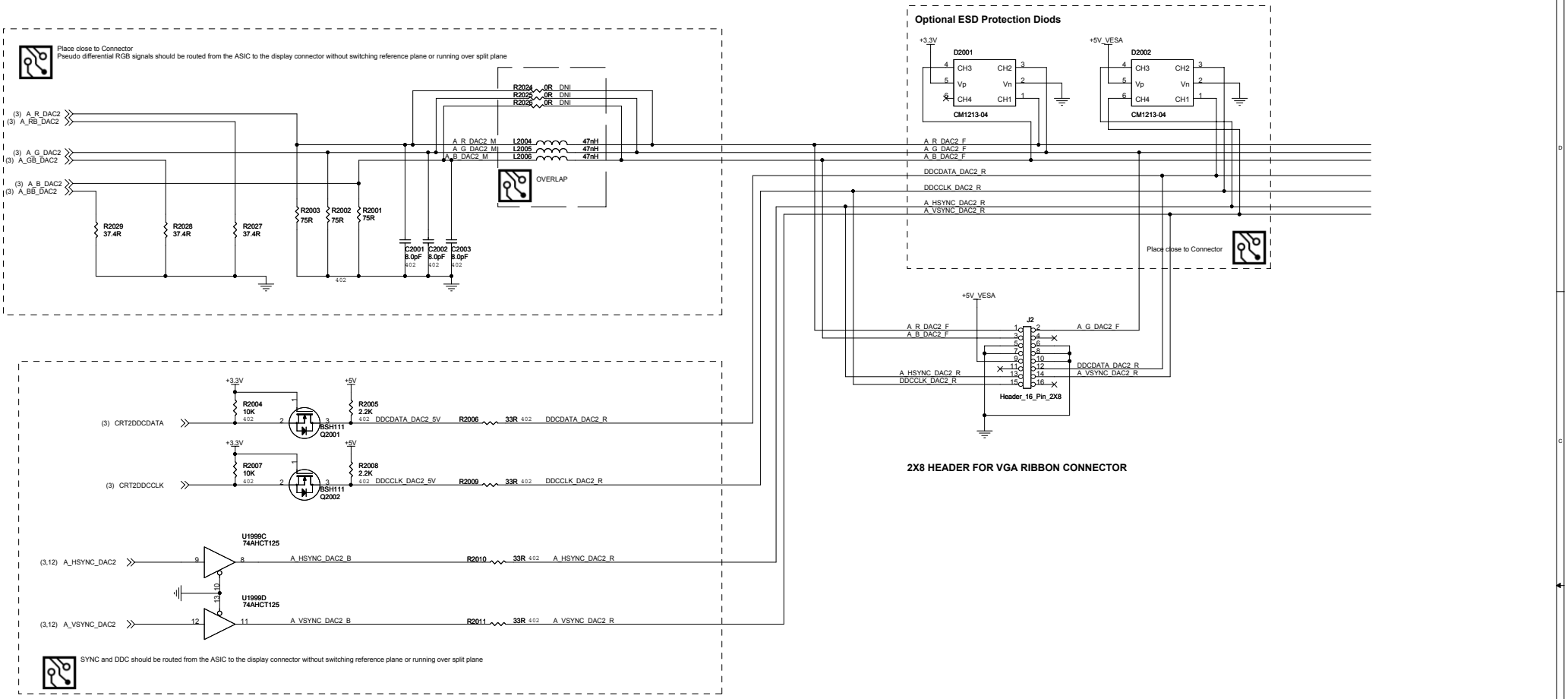

TMDS_1(Single_Link) + DAC_2-CRT

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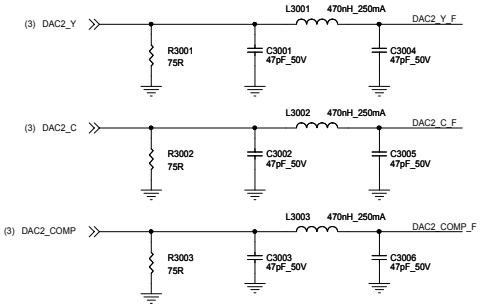

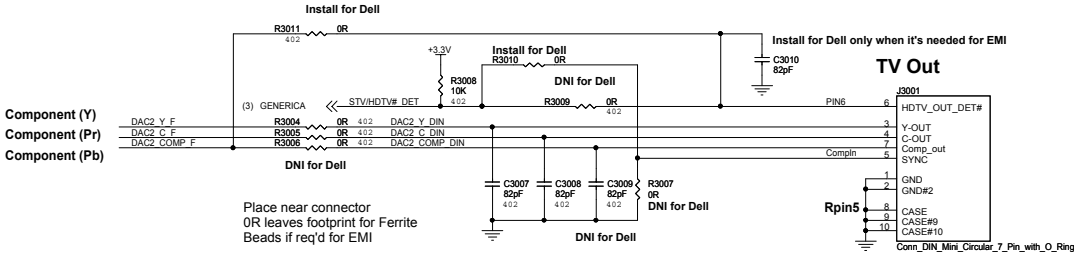

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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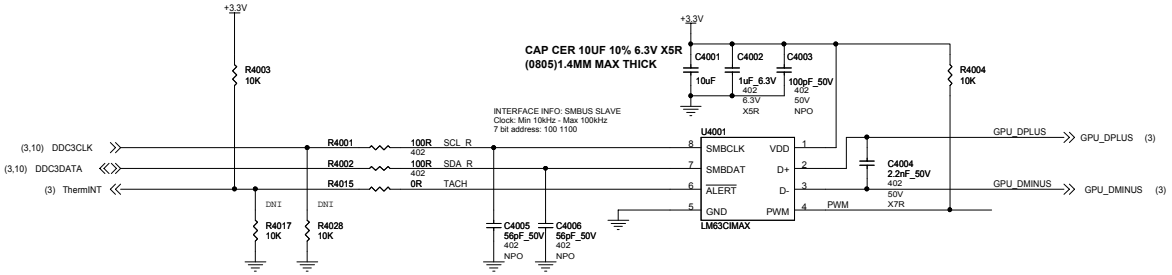
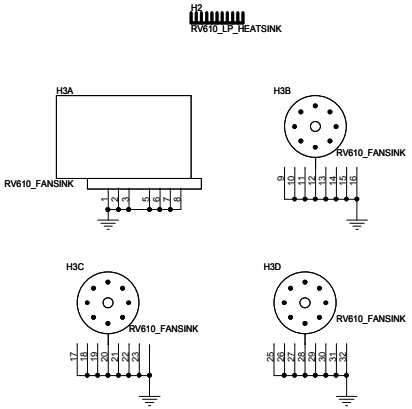
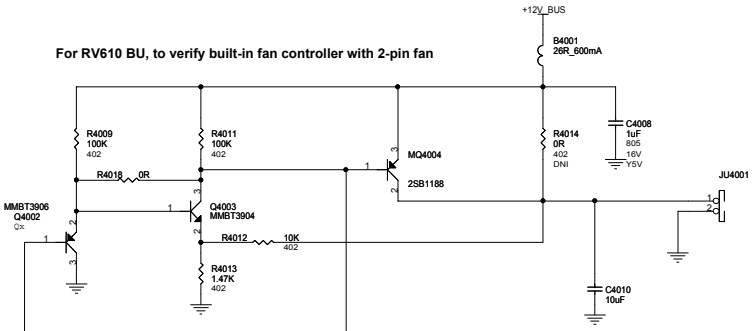
LM63 is for RV610 BU, until built-in fan controller is verified.

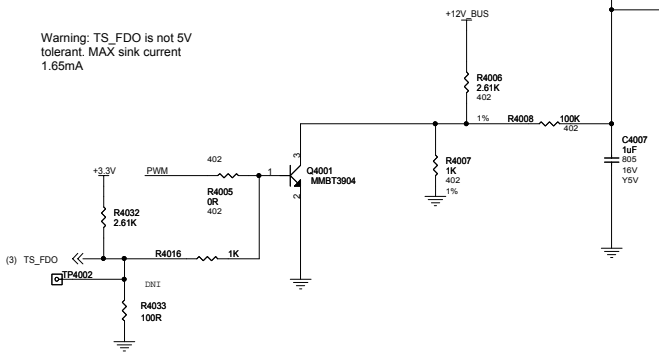




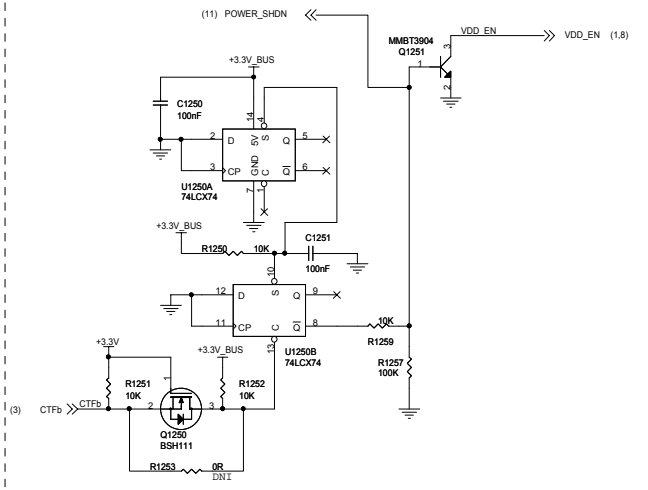
For RV610 BU, to verify built-in fan controller with 2-pin fan



Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA



CRITICAL TEMPERATURE FAULT



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DVI/VGA SCREWS

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

MT1
MT_Hole_0.136_in.
DNI

MT2
MT_Hole_0.136_in_6VIA
DNI

ASSY1
BRACKET
8020040100G

ASSY2
BRACKET
LP
8020040400G

<Variant Name>

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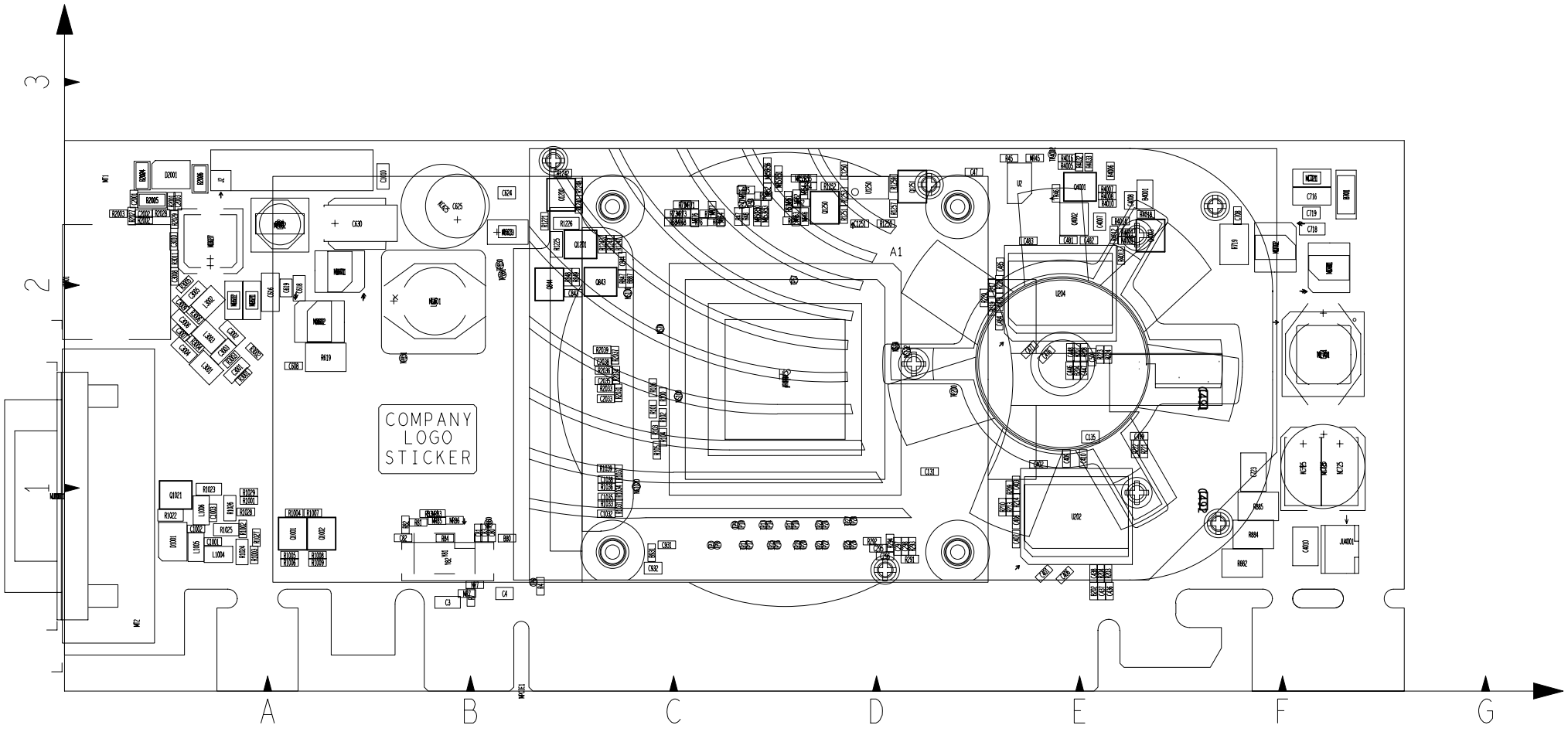

AMD ADVANCED MICRO DEVICES PCBCAD GROUP	RH RV610 256MB/128MB DDR2-BGA84 32/16Mx16 VO dDVI PN 109-B17031-00 APRIL 26, 2007 DESIGNER DORINA A.\SVETLANA O. ASSEMBLY TOP SHEET 1 OF 2

ADVANCED MICRO DEVICES PCBCAD GROUP	RH RV610 256MB\128MB DDR2-BGA84 32\16Mx16 VO dDVI PN 109-B17031-00 APRIL 26, 2007 DESIGNER DORINA A./SVETLANA O.