

NV28M-P138, DAC, TMDS, LVDS, TVout, 32/64MB 4MX32 BGA DDR, AGP4X, Dell
Mobile

X00

1. Schematics taken from E153-A00.

X17

1. Use RUNPWRGD for all PS enabling.

A01:

X40

1. Corrected serial ROM hookup.

A02:

X42

1. Corrected I2C2 hookup at U9 (CH7009).
2. Changed R254 to 1.5K 1%. This raises NVVDD to 1.25V.
3. Connect GPIO1 to 90C387 PD, and disconnect SUS_STAT- from motherboard.
4. Change Q2 to FDS6982.

X44

5. Change R287 to 2.67K and R254 to 1.1K when NVVDDSW stuff option is employed, with R254 = 1.5K when no NVVDDSW is used (NOSW stuff option).
6. Removed TP606 to allow better guard trace on thermal sensor D+ and D- lines.
7. Connected CH_GPIO0 to NSM_DUAL to select single or dual link panels.

A03:

X00

1. Add r989, r990, r991, r992 to pull up I2C bus.
2. Change c82 and c84 into small package to fit into new mechanical requirement.
3. Change r44 from pull-up to pull-up to ground.
4. Chang c60 and c61 to 47pF fot TVout issue.

X01

1. Change r287 to 4.02k; r254 to 1.21k.

A04:

X00


1. Change Mem vendor strapping option

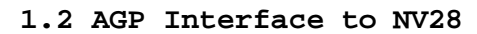
X01

1. In P.13, rework to prevent LCDVCC backdrive. Connect L12.2 directly to C32.1 instead of 3.3NSM.
2. In P.14, rework to prevent LCDVCC glich. Use resistive load n-fet as an inverter driven by 3VRUN instead of 5VRUN.
3. Change CH7009 to CH7009B and connect U9.9 (HPDET) to J10.36 (DVI_DET)

1.1 TOP PAGE 140-10138-0000-004
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	P138 L/K Module		
Size Custom	CAGE Code	DWG NO	Rev 100
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FBD_DATA0_C19	FBD_DATA0	FBC_DATA0	D32_FBC_DATA0
FBD_DATA1_B19	FBD_DATA1	FBC_DATA1	C33_FBC_DATA1
FBD_DATA2_E18	FBD_DATA2	FBC_DATA2	E30_FBC_DATA2
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FBD_DATA4_B17	FBD_DATA4	FBC_DATA4	C32_FBC_DATA4
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FBD_DATA6_D17	FBD_DATA6	FBC_DATA6	E30_FBC_DATA6
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FBD_DATA8_F17	FBD_DATA8	FBC_DATA8	E32_FBC_DATA8
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FBD_ADR4_F13	FBD_ADR4	FBC_ADR4	E27_FBC_ADR4
FBD_ADR5_B12	FBD_ADR5	FBC_ADR5	D26_FBC_ADR5
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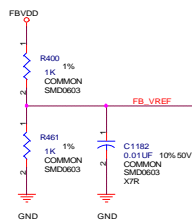
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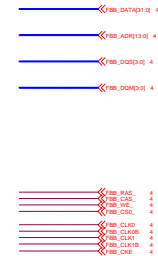
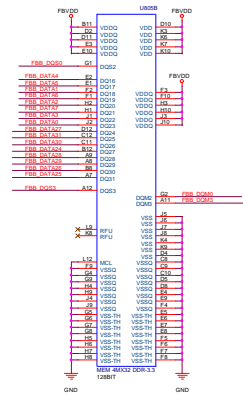
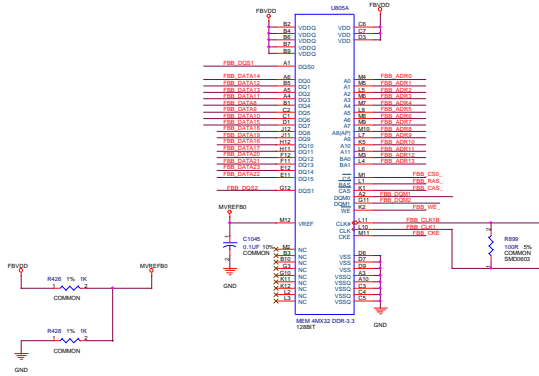
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2.1 NV FBA/B/C/D

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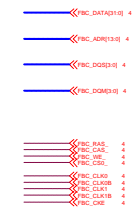
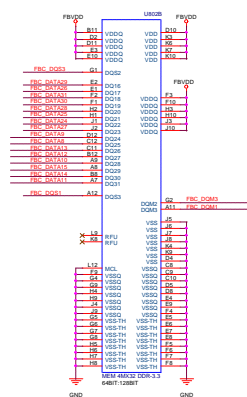
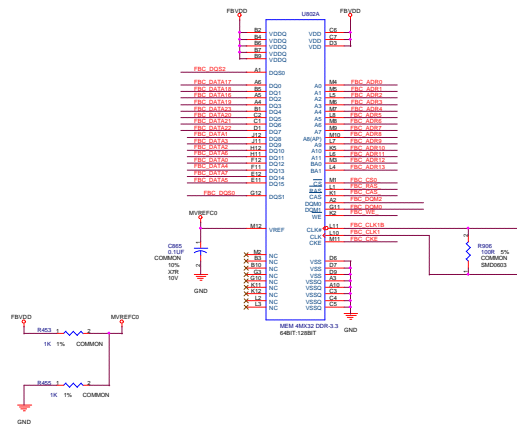
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2.3 FBB DDR 4MX32 SDRAM

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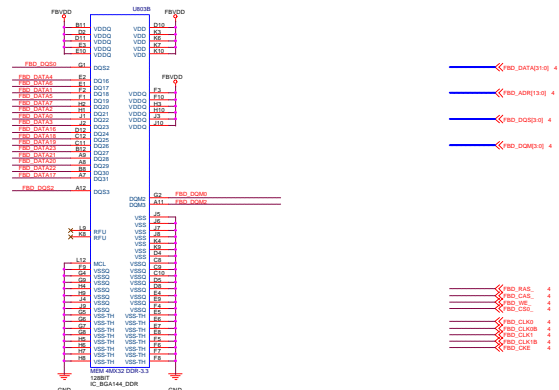
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2.4 FBC DDR 4MX32 SDRAM

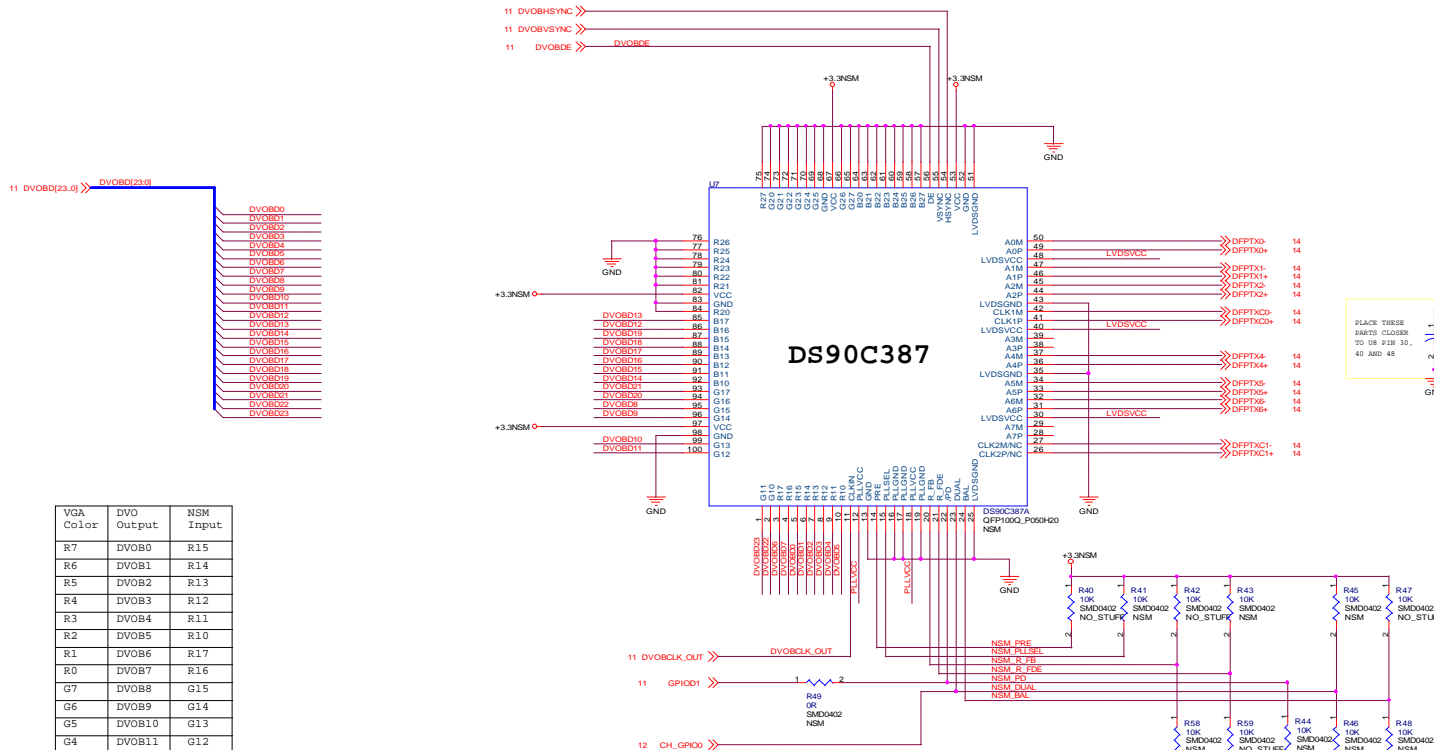
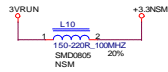
	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA		
	P138 L/K Module		
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Rev	1	DATE Code	0000 NO
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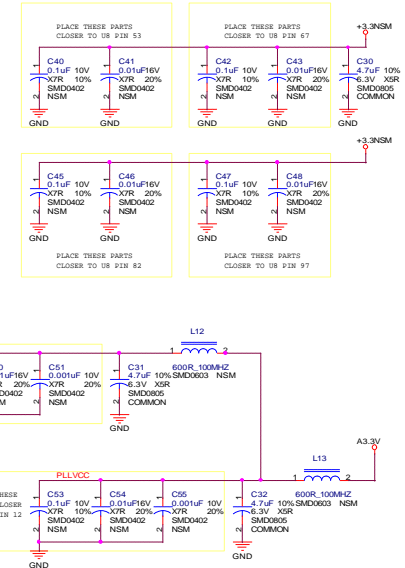


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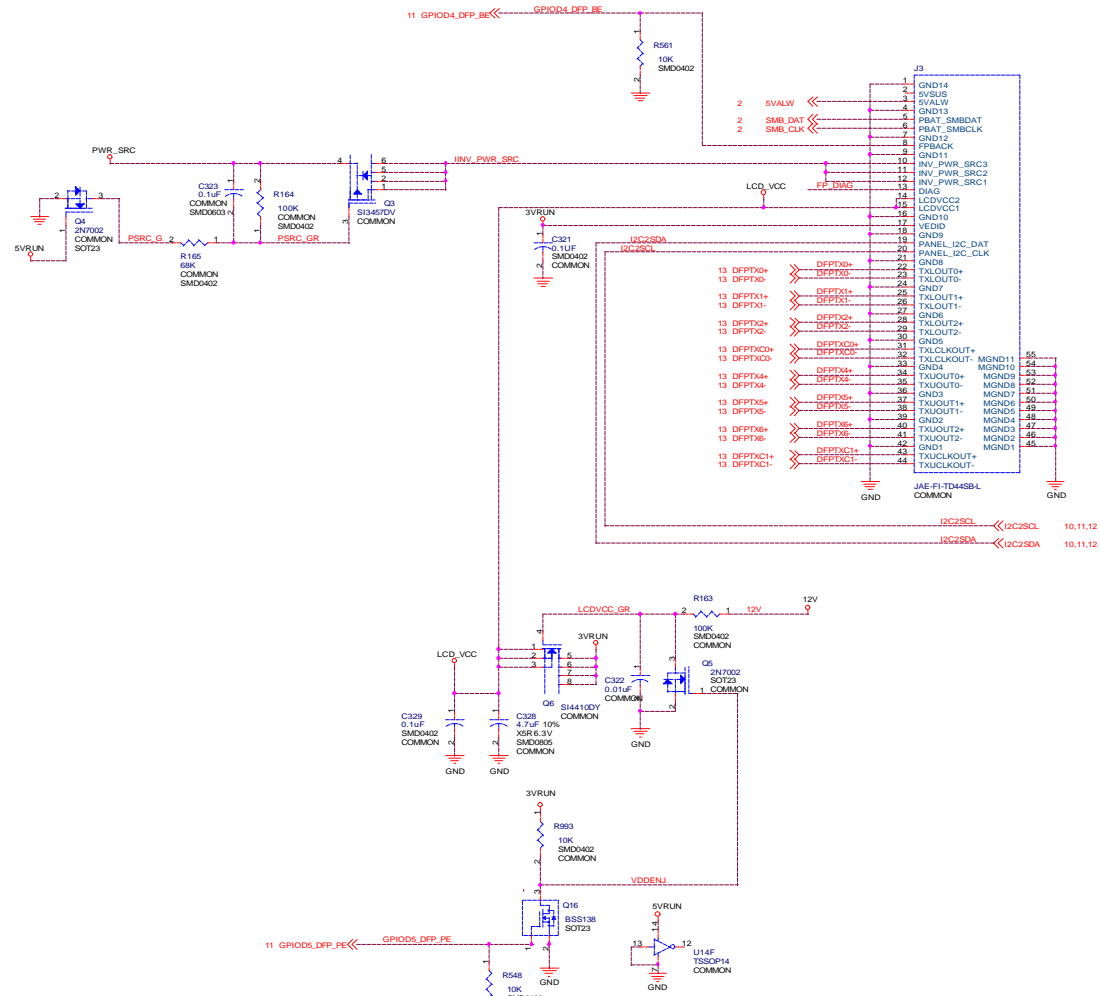
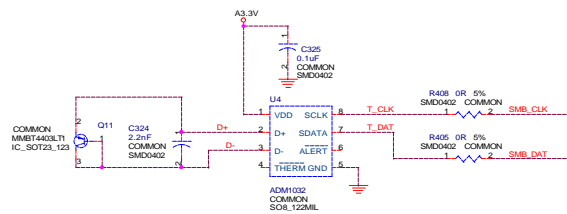


NOTE:
This is for single pixel per clock input mapping ONLY.



4.2 DS90C387 - LVDS


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	P138 L/K MODULE		
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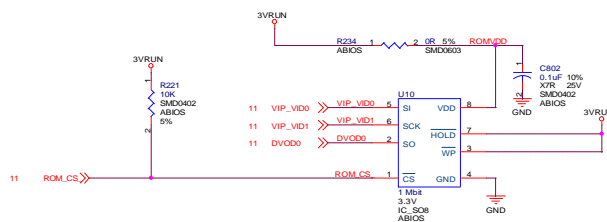
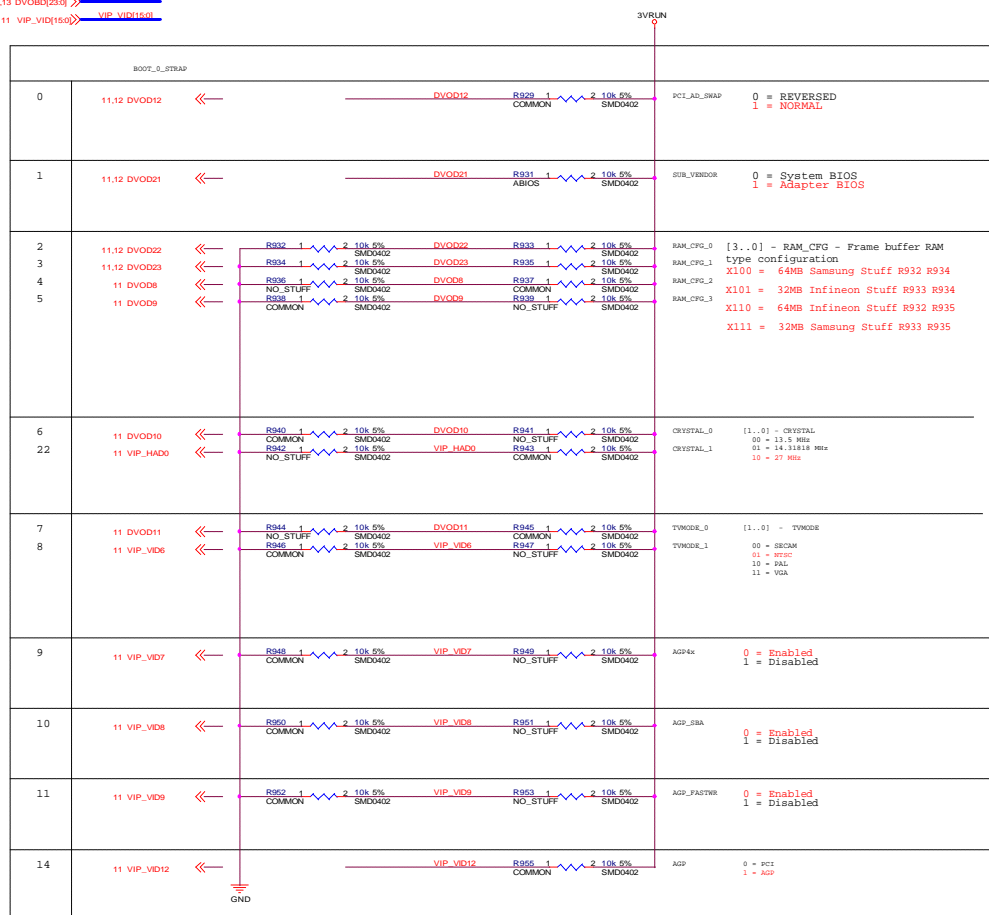


4. Panel

5.2 Panel, Thermal Sensor

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P138 L/K MODULE			
Size	EAGE Code	DWG NO	Rev
Custom			100
Scale		Sheet	14 of 16
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6.1 NV STRAP, S-ROM



P138 L/K MODULE

Size	CAGE Code	DWG NO	Rev
Custom			100
Scale		Sheet	15 of 16



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