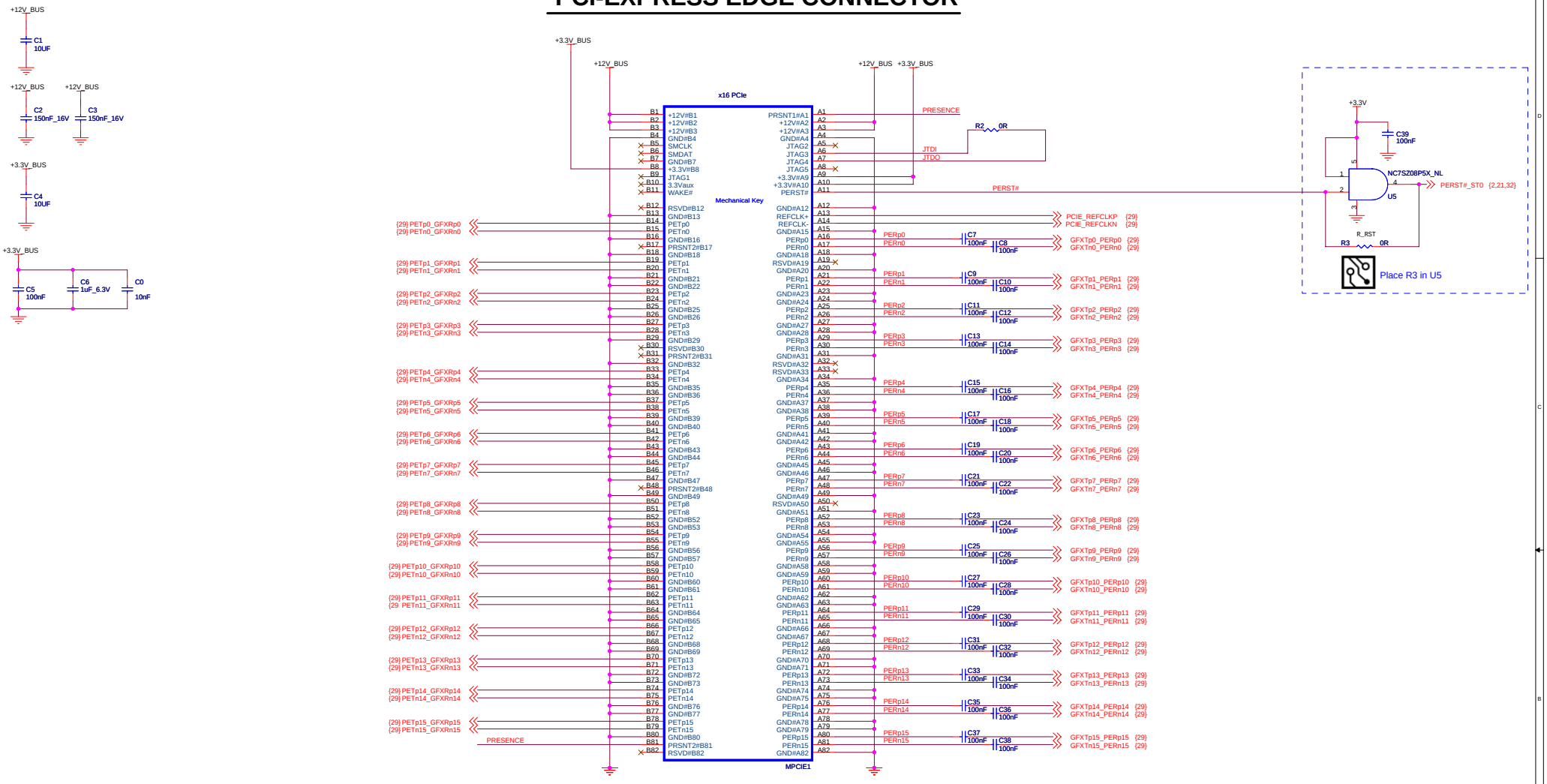
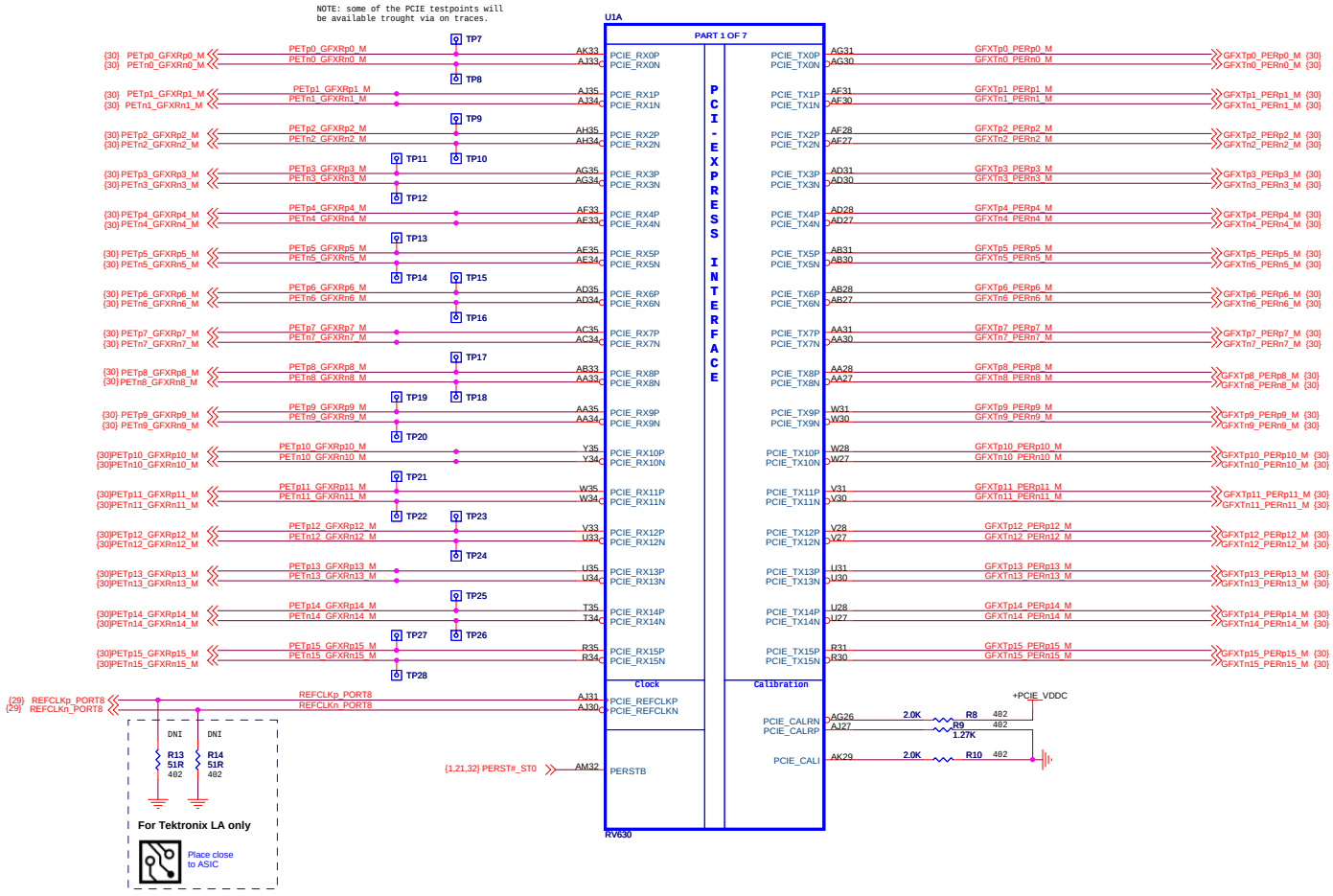
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	PEX8547+RV630 GDDR3 VGA CARD		
Size C	Document Number DUAL GPU		Rev A
Date: Tuesday, May 15, 2007		Sheet 1 of 36	



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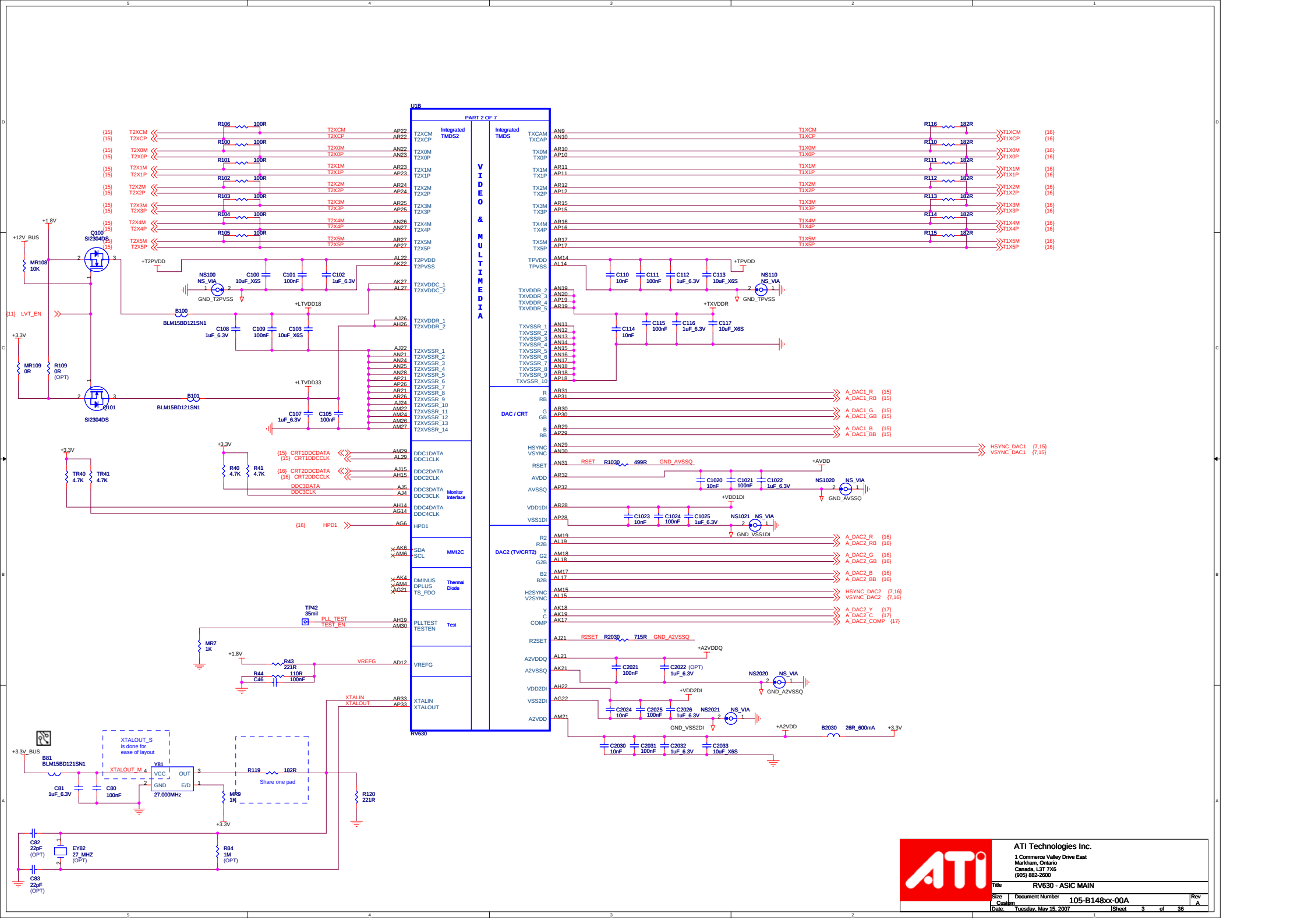
(905) 882-2600

Title	PEX8547+RV630 GDDR3 VGA CARD	
Size: C	Document Number: DUAL GPU	Rev: A
Date: Tuesday, May 15, 2007	Sheet 2 of 36	


U1B
PART 2 OF 7
VIDEO & MULTIMEDIA
RV630
Integrated TMDS2
Integrated TMDS
DAC / CRT
DAC2 (TV/CRT2)
Monitor Interface
MMI2C
Thermal Diode
Test
T2XCM T2XCP T2X0M T2X0P T2X1M T2X1P T2X2M T2X2P T2X3M T2X3P T2X4M T2X4P T2X5M T2X5P
T1XCM T1XCP T1X0M T1X0P T1X1M T1X1P T1X2M T1X2P T1X3M T1X3P T1X4M T1X4P T1X5M T1X5P
TXCAM TXCAP TX0M TX0P TX1M TX1P TX2M TX2P TX3M TX3P TX4M TX4P TX5M TX5P
R106 R100 R101 R102 R103 R104 R105 100R
R116 R110 R111 R112 R113 R114 R115 182R
+1.8V +12V_BUS +3.3V +TPVDD +TXVDDR +AVDD +VDD1DI +A2VDDQ +A2VDD +LTVDD18 +LTVDD33
Q100 Q101 SI2304DS
MR108 10K MR109 0R R109 0R (OPT)
B100 B101 BLM15BD121SN1
{11} LVT_EN
NS100 NS110 NS1020 NS1021 NS2020 NS_VIA
GND_T2PVSS GND_TPVSS GND_AVSSQ GND_VSS1DI GND_A2VSSQ GND_VSS2DI
C100 10uF_X6S C101 100nF C102 1uF_6.3V C103 10uF_X6S C105 100nF C107 1uF_6.3V C108 1uF_6.3V C109 100nF
C110 10nF C111 100nF C112 1uF_6.3V C113 10uF_X6S C114 10nF C115 100nF C116 1uF_6.3V C117 10uF_X6S
C1020 10nF C1021 100nF C1022 1uF_6.3V C1023 10nF C1024 100nF C1025 1uF_6.3V
C2021 100nF C2022 (OPT) 1uF_6.3V C2024 10nF C2025 100nF C2026 1uF_6.3V
C2030 10nF C2031 100nF C2032 1uF_6.3V C2033 10uF_X6S
B2030 26R_600mA
TR40 4.7K TR41 4.7K R40 4.7K R41 4.7K
{15} CRT1DDCDATA CRT1DDCCLK {16} CRT2DDCDATA CRT2DDCCLK
DDC3DATA DDC3CLK
{16} HPD1
AK6 AM6 SDA SCL
AK4 AM4 AG21 DMINUS DPLUS TS_FDO
TP42 35mil PLL_TEST TEST_EN
MR7 1K R43 221R R44 110R C46 100nF VREFG
R1030 499R GND_AVSSQ
R2030 715R GND_A2VSSQ
RSET AJ21
A_DAC1_R A_DAC1_RB A_DAC1_G A_DAC1_GB A_DAC1_B A_DAC1_BB
A_DAC2_R A_DAC2_RB A_DAC2_G A_DAC2_GB A_DAC2_B A_DAC2_BB
A_DAC2_Y A_DAC2_C A_DAC2_COMP
HSYNC_DAC1 VSYNC_DAC1 HSYNC_DAC2 VSYNC_DAC2
XTALIN XTALOUT AR33 AP33
XTALOUT_S is done for ease of layout
XTALOUT_M
Y81 27.000MHz
B81 BLM15BD121SN1
C81 1uF_6.3V C80 100nF
R119 182R Share one pad
MR9 1K R120 221R
C82 22pF (OPT) C83 22pF (OPT) EY82 27_MHZ (OPT) R84 1M (OPT)
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600
Title RV630 - ASIC MAIN
Size Custom
Document Number 105-B148xx-00A
Rev A
Date: Tuesday, May 15, 2007
Sheet 3 of 36

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402

U1E

PART 5 OF 7

POWER

Memory I/O

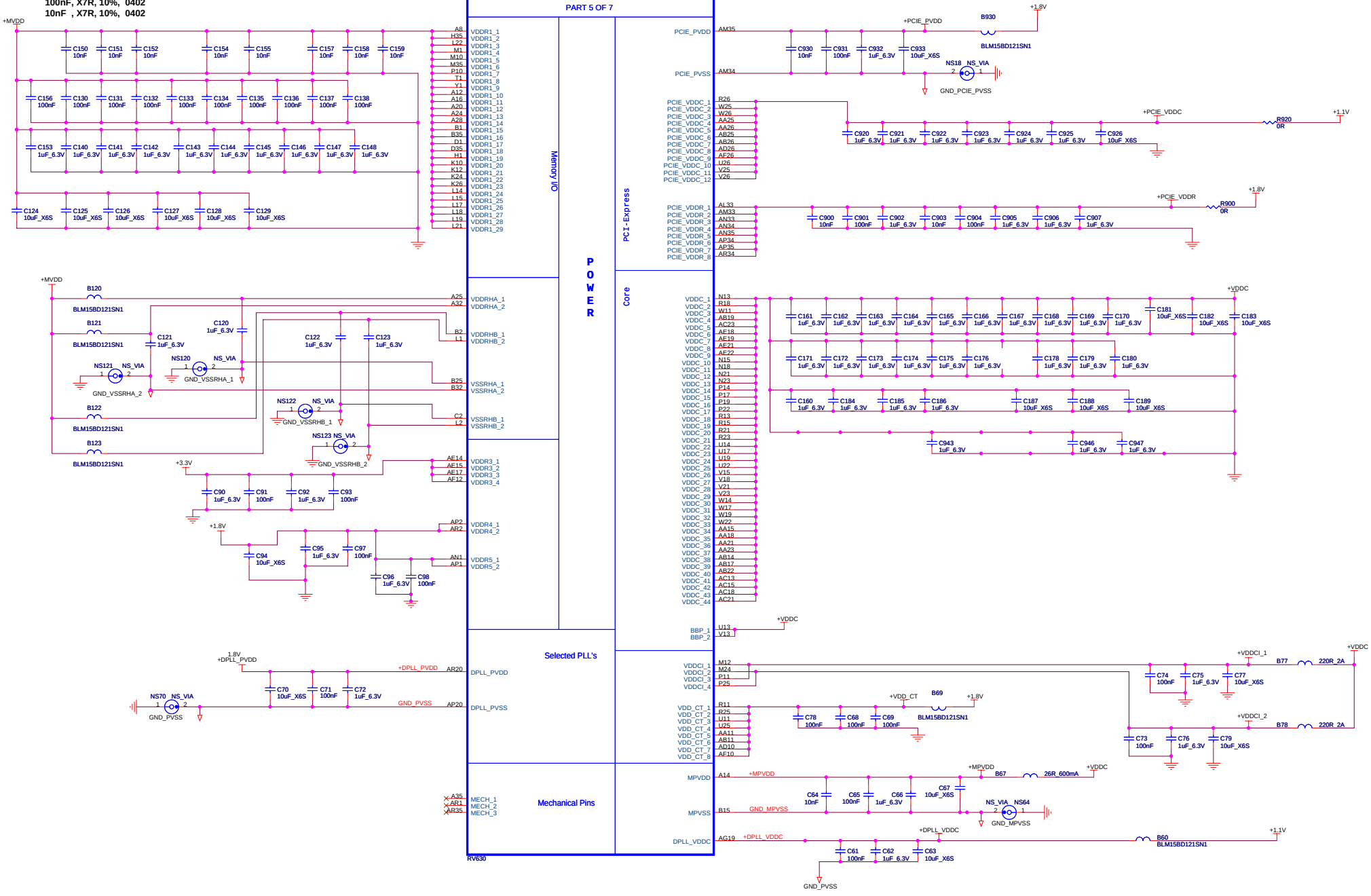
PCI-Express

Core

Selected PLL's

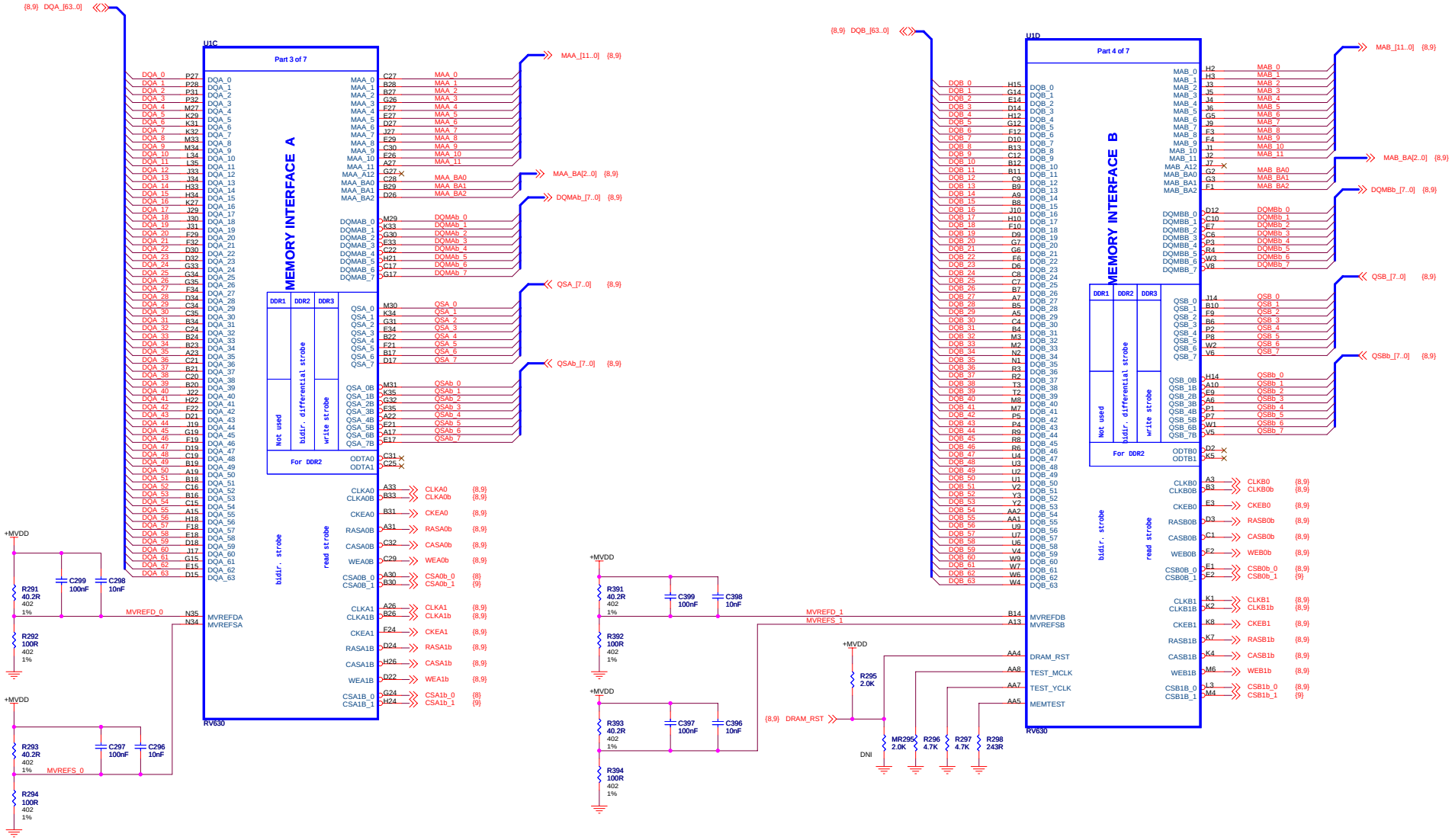
Mechanical Pins

RV630



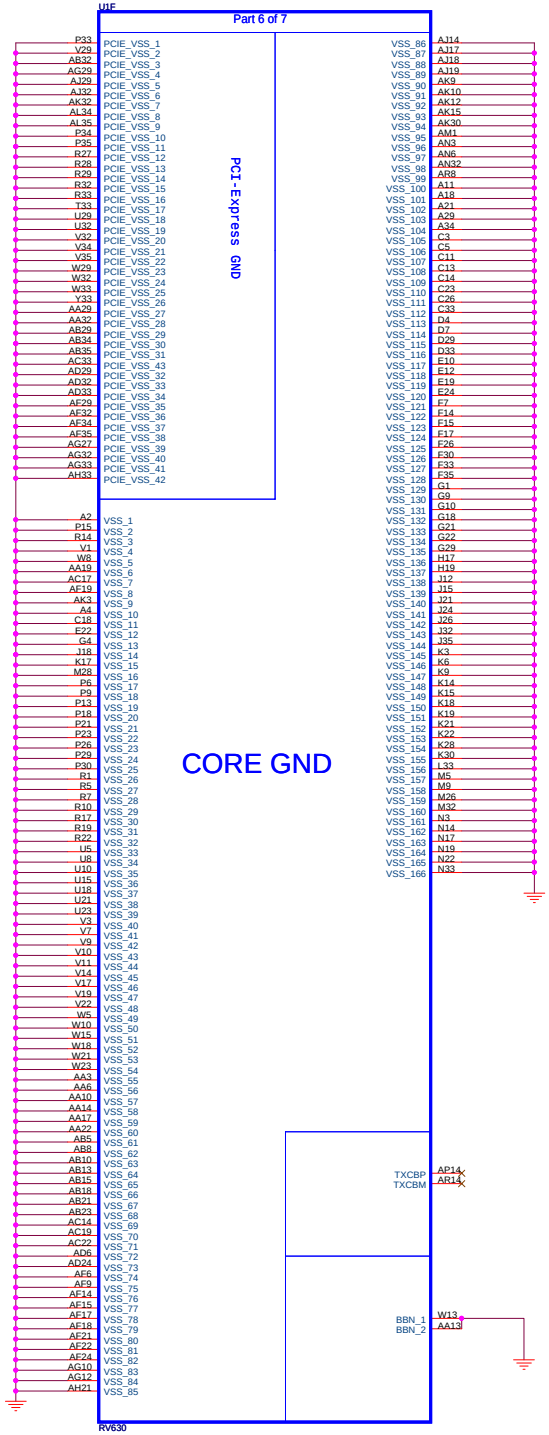
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV630 GDDR3 - ASIC Power		
Size: C	Document Number: 105-B148xx-00A		Rev: A
Date: Tuesday, May 15, 2007	Sheet 4 of 36		



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV630 GDDR3 - ASIC Memory Interface (Channel A & B)		
Size: C	Document Number: 105-B148xx-00A		Rev: A
Date: Tuesday, May 15, 2007		Sheet 5 of 36	



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
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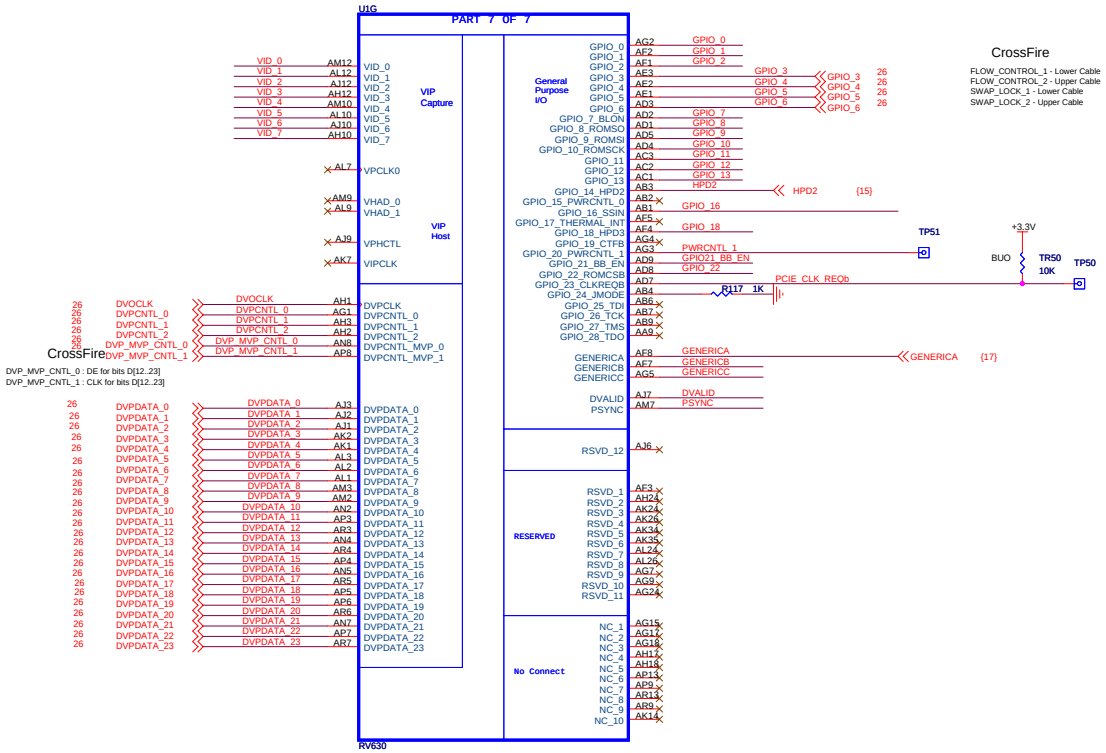
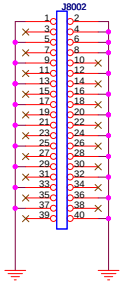
(905) 882-2600

Title	RV630 GDDR3 - ASIC Grounds	
Size: C	Document Number: 105-B148xx-00A	Rev: A
Date: Tuesday, May 15, 2007	Sheet 6 of 36	



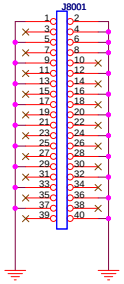
CrossFire Card-Edge

Lower Cable Card Edge

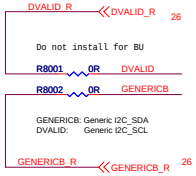


Bundle A

Upper Cable Card Edge

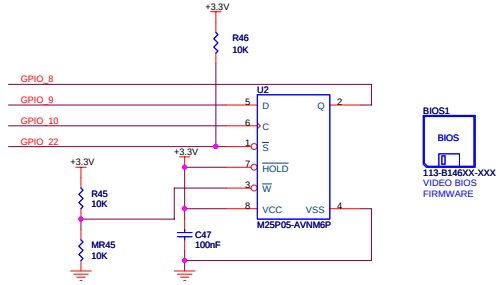


Bundle B (closer to the bracket)



CrossFire

FLOW_CONTROL_1 - Lower Cable
FLOW_CONTROL_2 - Upper Cable
SWAP_LOCK_1 - Lower Cable
SWAP_LOCK_2 - Upper Cable



ATI Technologies Inc.
1 Commerce Valley Drive East
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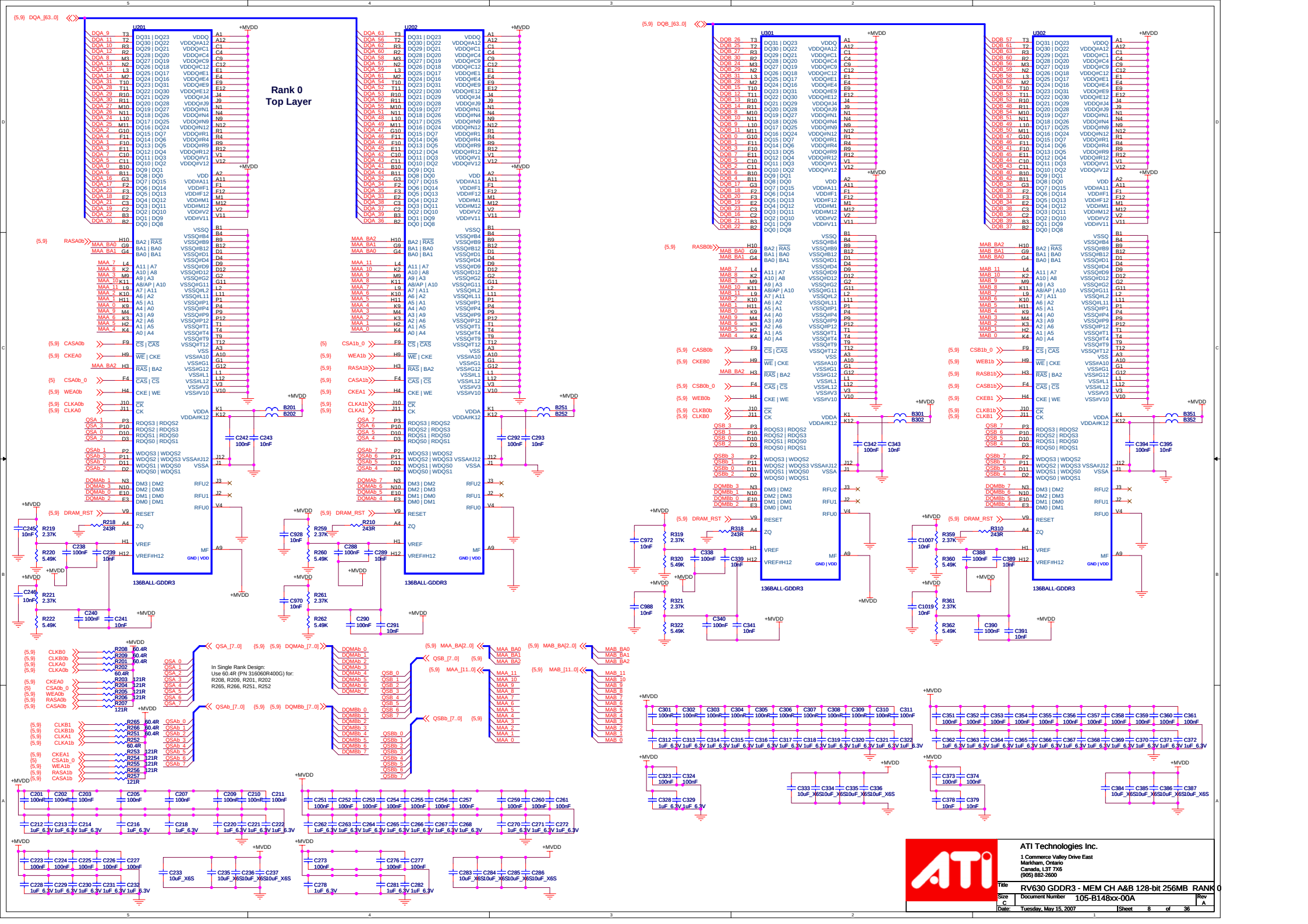
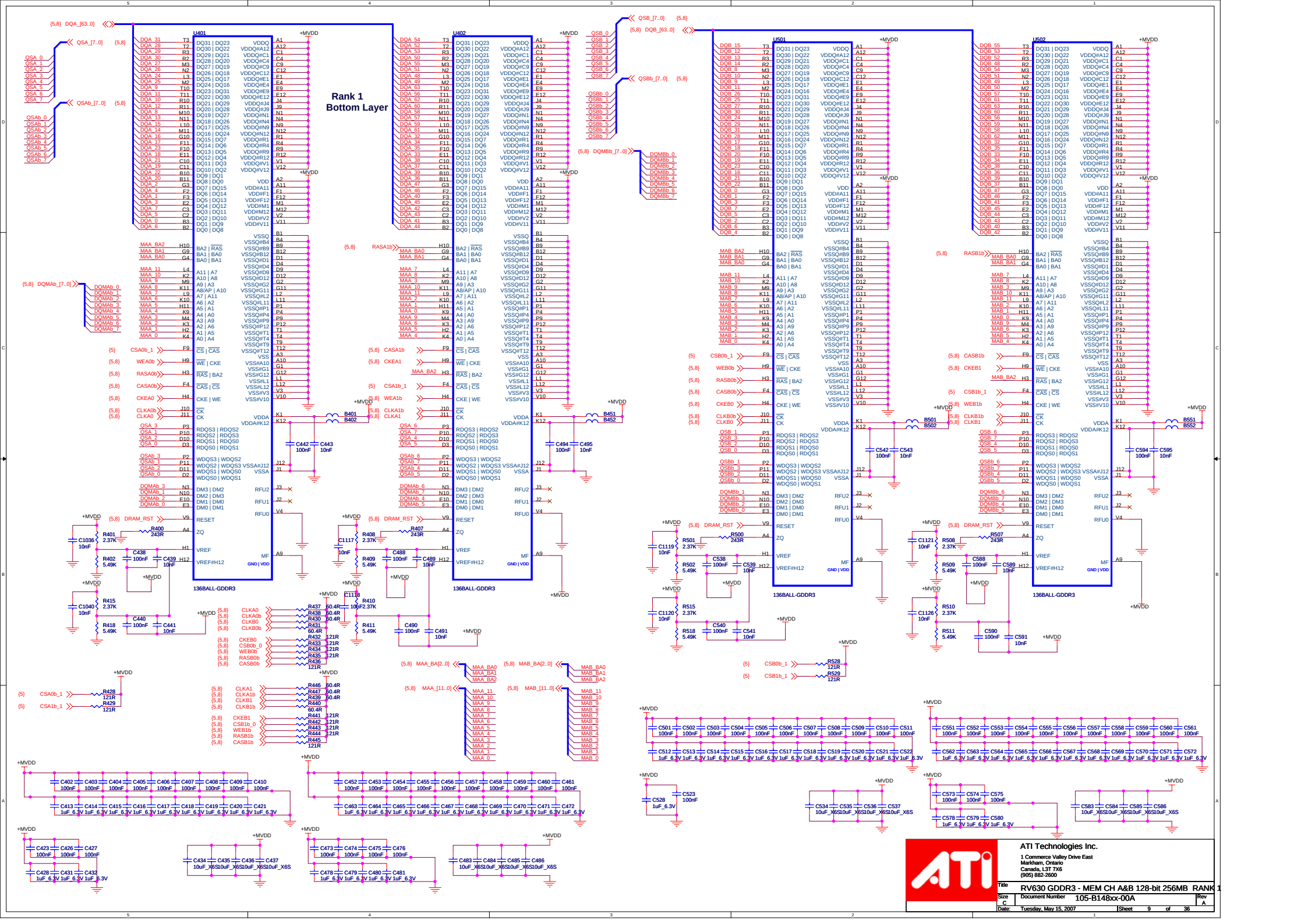
(905) 882-2600

Title	RV630 GDDR3 - ASIC DVO & GPIOs	
Size C	Document Number 105-B148xx-00A	Rev A
Date: Tuesday, May 15, 2007	Sheet 7 of 36	


Rank 0
Top Layer
U201
U202
U301
U302
136BALL-GDDR3
In Single Rank Design:
Use 60.4R (PN 316060R400G) for:
R208, R209, R201, R202
R265, R266, R251, R252
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600
Title
RV630 GDDR3 - MEM CH A&B 128-bit 256MB RANK 0
Size
C
Document Number
105-B148xx-00A
Rev
A
Date:
Tuesday, May 15, 2007
Sheet
8
of
36



ATI Technologies Inc.
1 Commerce Valley Drive East
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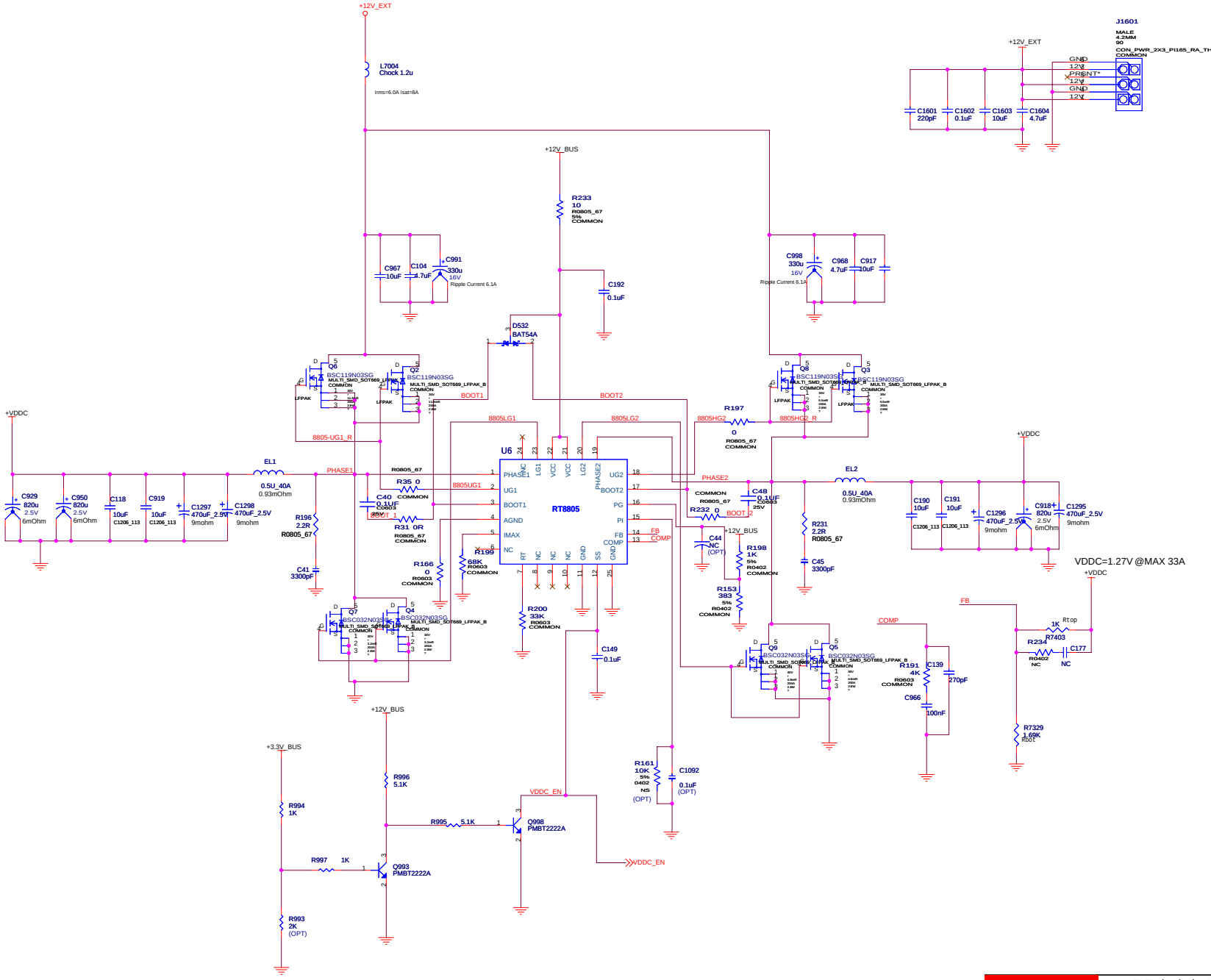
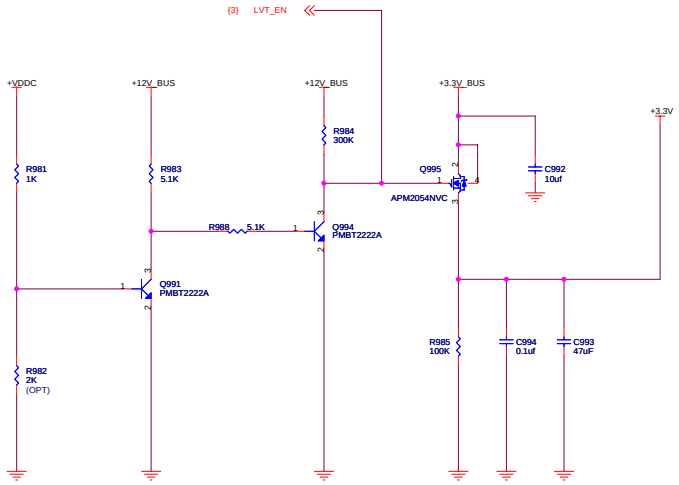
(905) 882-2600

Title	RV630 GDDR3 - MEM CH A&B 128-bit 256MB RANK 1		
Size C	Document Number 105-B148xx-00A		Rev A
Date: Tuesday, May 15, 2007		Sheet 9 of 36	

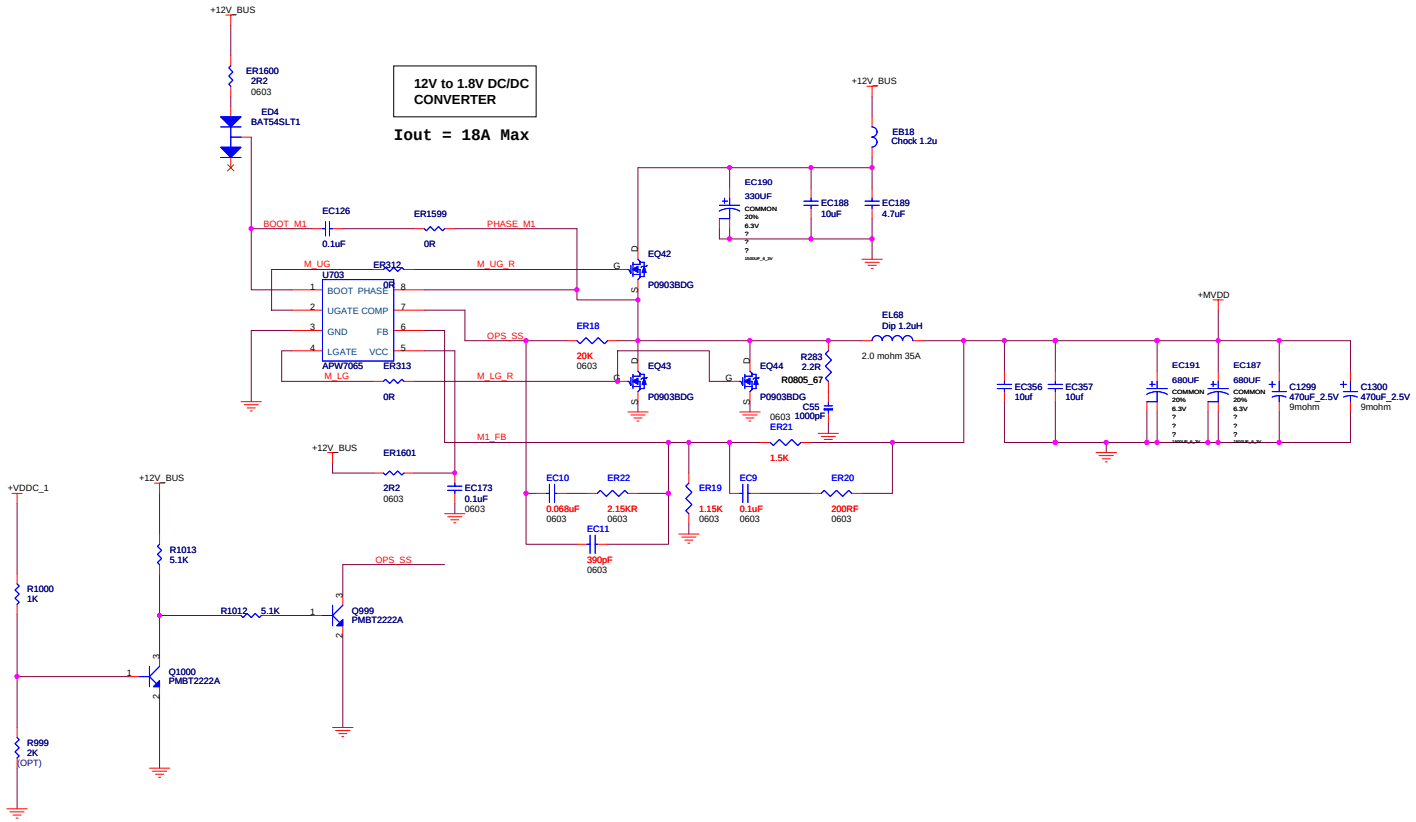


ATI Technologies Inc.			
1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600			
Title: RV630 GDDR3 - VDDC SMPS 01			
Size: Custom	Document Number: 105-B148xx-00A		Rev: A
Date: Tuesday, May 15, 2007		Sheet 10 of 36	



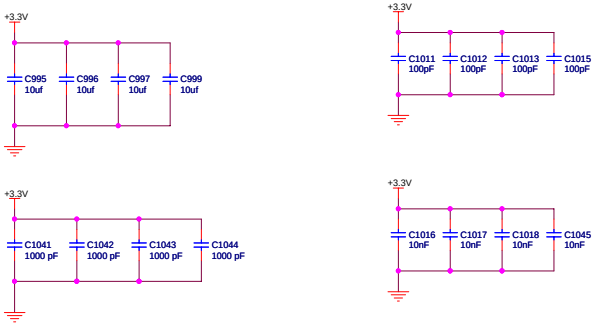
ATI Technologies Inc.		
1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600		
Title	RV630 GDDR3 - VDDC SMPS 02	
Size: Custom	Document Number: 105-B148xx-00A	Rev: A
Date: Tuesday, May 15, 2007	Sheet 11 of 36	

CORE REGULATOR VDDC



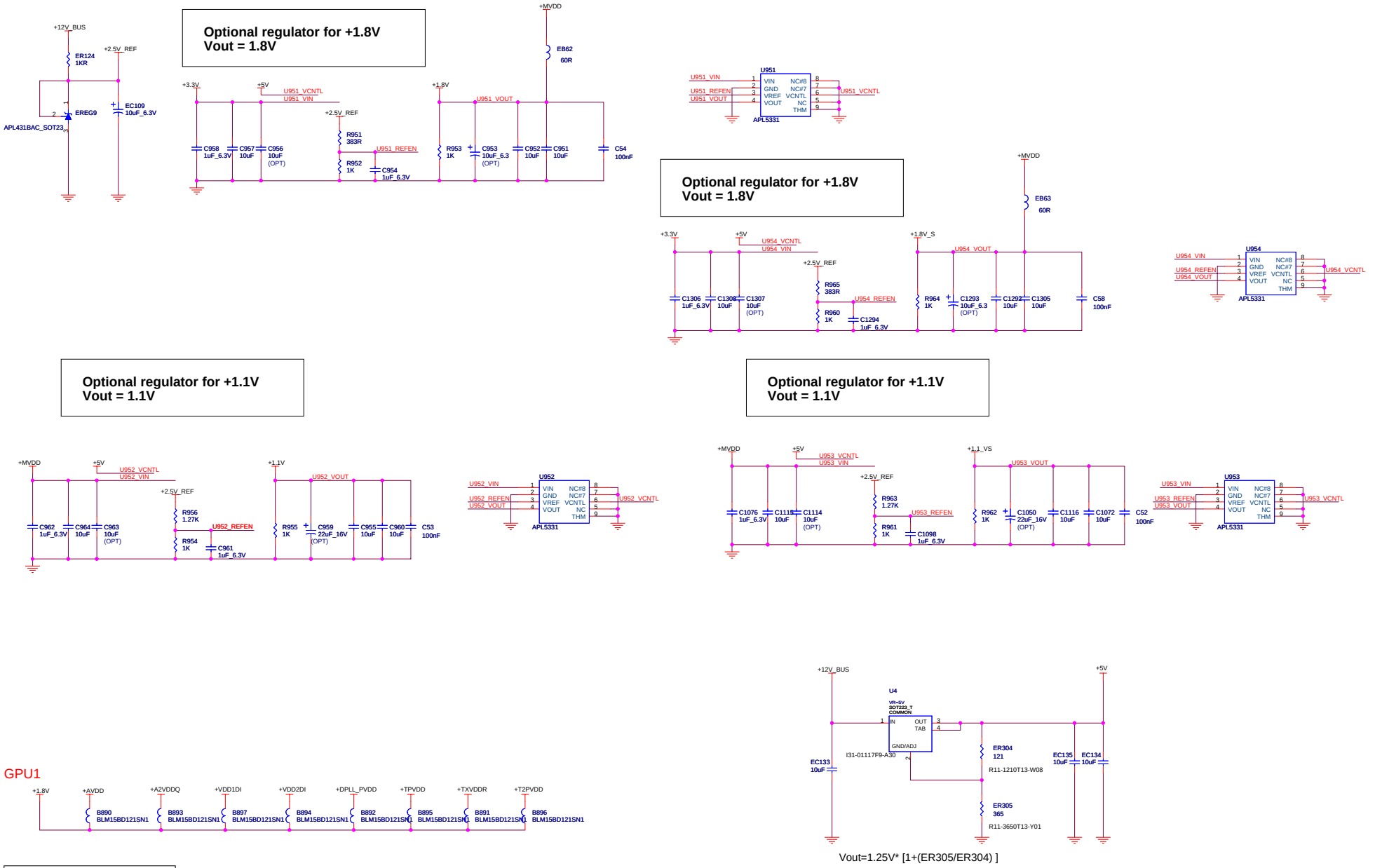
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV630 GDDR3 - MVDD SMPS 01		
Size: Custom	Document Number: 105-B148xx-00A		Rev: A
Date: Tuesday, May 15, 2007		Sheet 12 of 36	



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV630 GDDR3 - Power Management	
Size: C	Document Number: 105-B148xx-00A	Rev: A
Date: Tuesday, May 15, 2007	Sheet 13 of 36	



ATI Technologies Inc.
1 Commerce Valley Drive East
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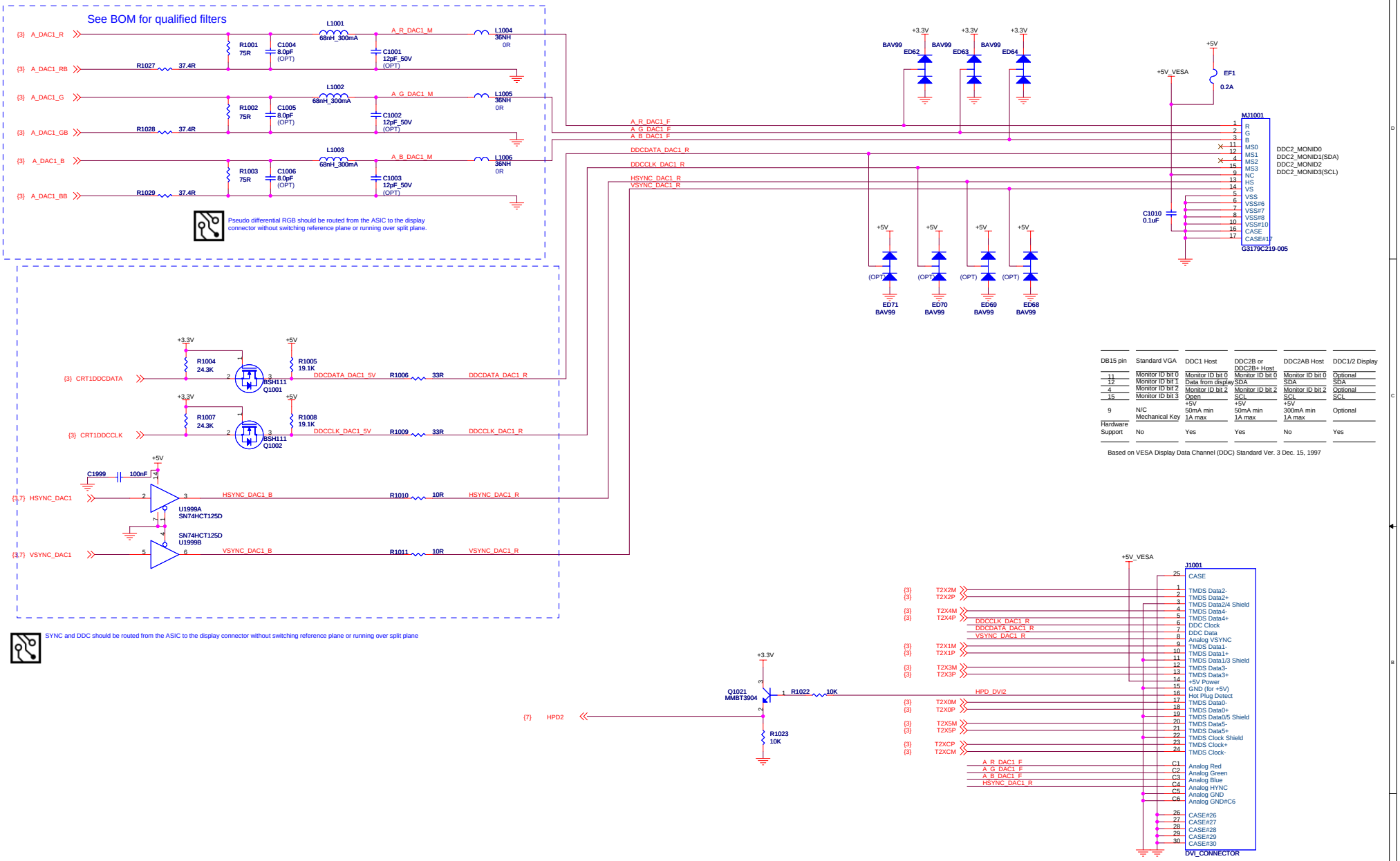
Canada, L3T 7X6
(905) 882-2600

Title	RV630 GDDR3 - Linear Regulators	
Size C	Document Number 105-B148xx-00A	Rev A
Date: Tuesday, May 15, 2007	Sheet 14 of 36	



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV630 GDDR3- DAC1&TMDS2	
Size: Custom	Document Number: 105-B148xx-00A	Rev: A
Date: Tuesday, May 15, 2007	Sheet 15 of 36	

See BOM for qualified filters

{3} A_DAC2_R
{3} A_DAC2_RB
{3} A_DAC2_G
{3} A_DAC2_GB
{3} A_DAC2_B
{3} A_DAC2_BB

R2001 75R 402
R2027 37.4R
R2002 75R 402
R2028 37.4R
R2003 75R 402
R2029 37.4R

C2004 8.0pF 402 (OPT)
C2001 12pF_50V 402 (OPT)
C2005 8.0pF 402 (OPT)
C2002 12pF_50V 402 (OPT)
C2006 8.0pF 402 (OPT)
C2003 12pF_50V 402 (OPT)

L2001 68nH_300mA
L2002 68nH_300mA
L2003 68nH_300mA

A_R_DAC2_M
A_G_DAC2_M
A_B_DAC2_M

L2004 36NH 0R
L2005 36NH 0R
L2006 36NH 0R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R

+3.3V
BAV99 ED67
BAV99 ED66
BAV99 ED65

+5V_VESA

MJ2001
R
G
B
MS0
MS1
MS2
MS3
NC
HS
VS
VSS
VSS#6
VSS#7
VSS#8
VSS#10
CASE
CASE#17
G3179C219-005

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

+5V
(OPT) ED75 BAV99
(OPT) ED74 BAV99
(OPT) ED73 BAV99
(OPT) ED72 BAV99

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

+3.3V
+5V

{3} CRT2DDCDATA
R2004 24.3K
R2005 19.1K 402
Q2001 BSH111
DDCDATA_DAC2_5V
R2006 33R 402
DDCDATA_DAC2_R

{3} CRT2DDCCLK
R2007 24.3K
R2008 19.1K 402
Q2002 BSH111
DDCCLK_DAC2_5V
R2009 33R 402
DDCCLK_DAC2_R

{3,7} HSYNC_DAC2
U1999C SN74HCT125D
HSYNC_DAC2_B
R2010 10R 402
HSYNC_DAC2_R

U1999D SN74HCT125D

{3,7} VSYNC_DAC2
VSYNC_DAC2_B
R2011 10R 402
VSYNC_DAC2_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

+3.3V
Q2021 MMBT3904
R2022 10K
HPD_DVI1
{3} HPD1
R2023 10K

{3} T1X2M
{3} T1X2P
{3} T1X4M
{3} T1X4P
DDCCLK_DAC2_R
DDCDATA_DAC2_R
VSYNC_DAC2_R
{3} T1X1M
{3} T1X1P
{3} T1X3M
{3} T1X3P
{3} T1X0M
{3} T1X0P
{3} T1X5M
{3} T1X5P
{3} T1XCP
{3} T1XCM
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
HSYNC_DAC2_R

+5V_VESA

J2001
CASE
TMDS Data2-
TMDS Data2+
TMDS Data2/4 Shield
TMDS Data4-
TMDS Data4+
DDC Clock
DDC Data
Analog VSYNC
TMDS Data1-
TMDS Data1+
TMDS Data1/3 Shield
TMDS Data3-
TMDS Data3+
+5V Power
GND (for +5V)
Hot Plug Detect
TMDS Data0-
TMDS Data0+
TMDS Data0/5 Shield
TMDS Data5-
TMDS Data5+
TMDS Clock Shield
TMDS Clock+
TMDS Clock-
Analog Red
Analog Green
Analog Blue
Analog HYNC
Analog GND
Analog GND#C6
CASE#26
CASE#27
CASE#28
CASE#29
CASE#30
DVI_CONNECTOR

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title: RV630 GDDR3-DAC2/TMDS1
Size: Custom
Document Number: 105-B148xx-00A
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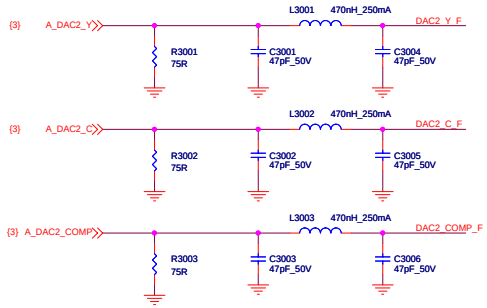
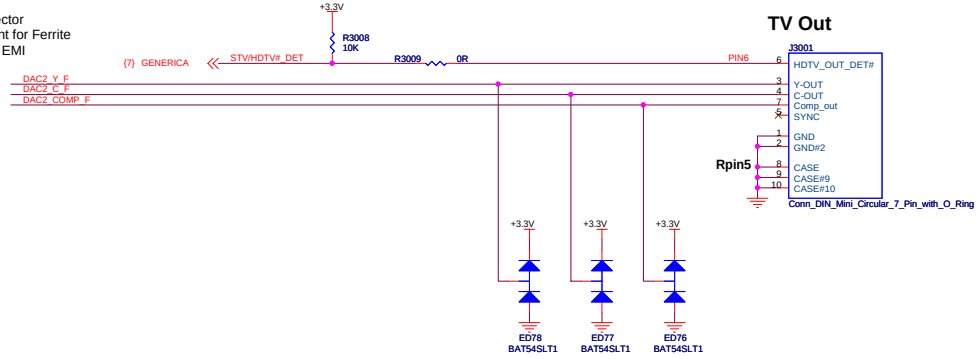
Date: Tuesday, May 15, 2007
Sheet 16 of 36

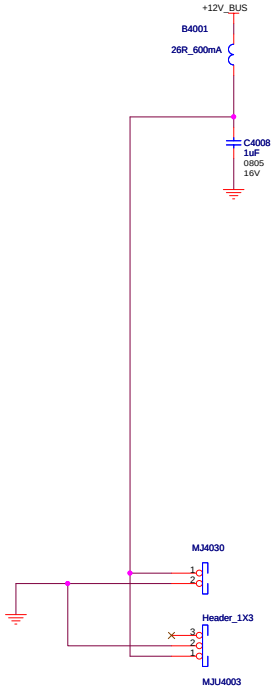


Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV630 GDDR3 - TVO	
Size C	Document Number 105-B148xx-00A	Rev A
Date: Tuesday, May 15, 2007	Sheet 17 of 36	



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RV630 GDDR3- Thermal Management	
Size: C	Document Number: 105-B148xx-00A	Rev: A
Date: Tuesday, May 15, 2007	Sheet 18 of 36	

DVI/DVI SCREWS with top tab

MEC4
MEC_HEX_JACK_SCREW
COMMON

MEC3
MEC_HEX_JACK_SCREW
COMMON

MEC2
MEC_HEX_JACK_SCREW
COMMON

MEC1
MEC_HEX_JACK_SCREW
COMMON

BKT1
BRACKET
8020042500G

MT2
MT_Hole_0.136_in_6VIA

DNI
SK1
RV410SOCKET

PCB1
PCB
109-GN982-00A

<Variant Name>

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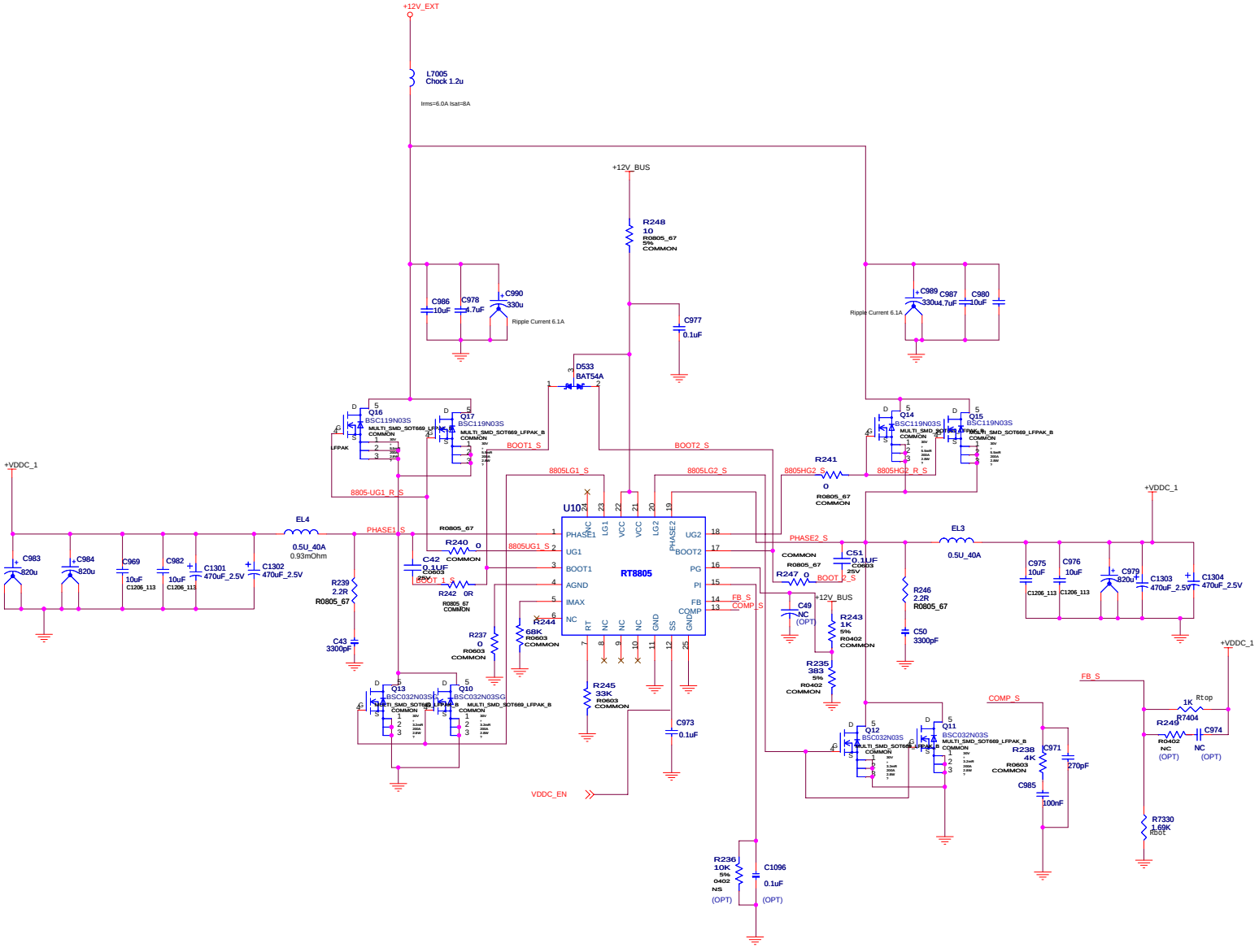
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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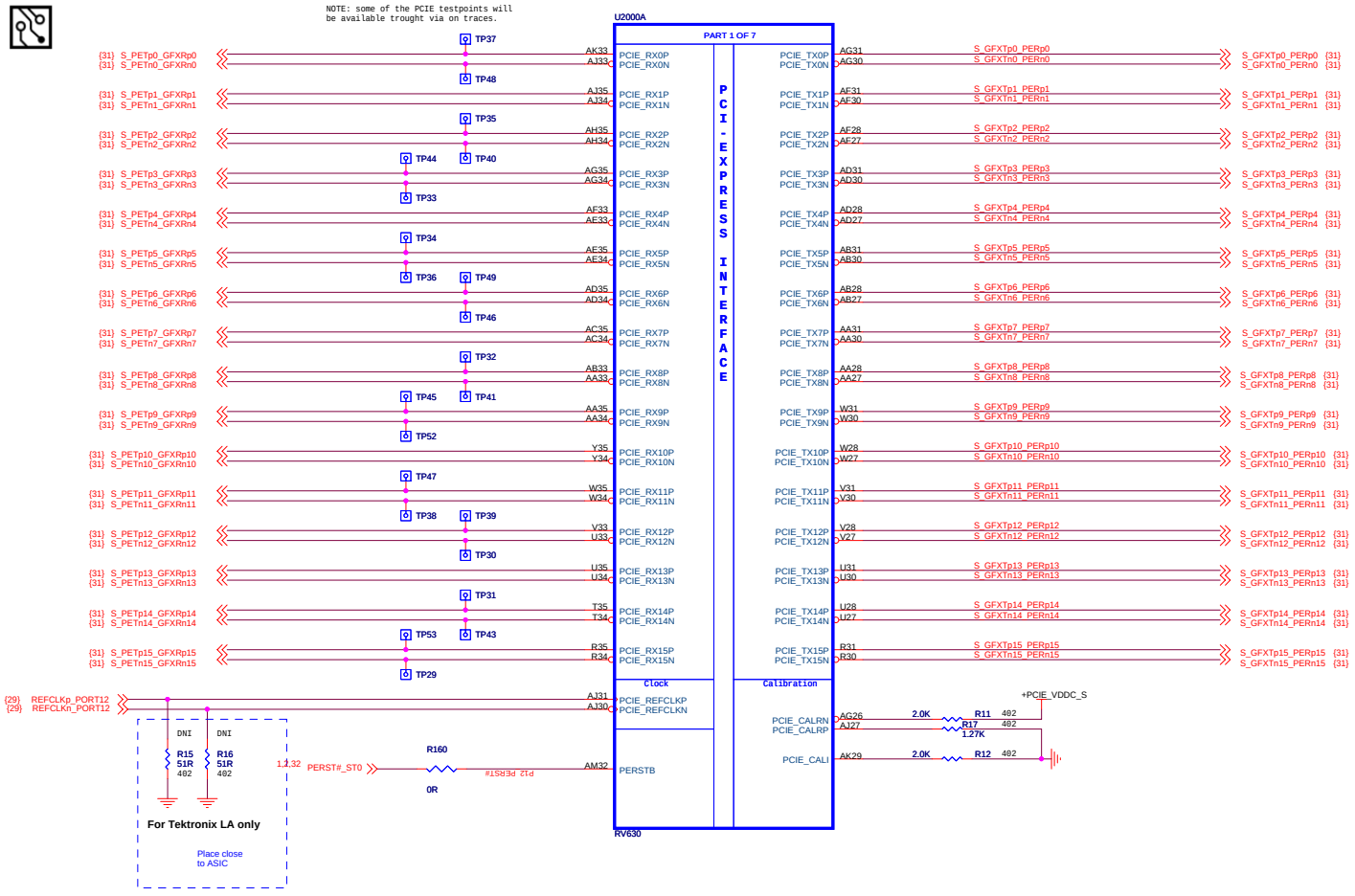

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Title	PEX8547+RV630 GDDR3 VGA CARD		
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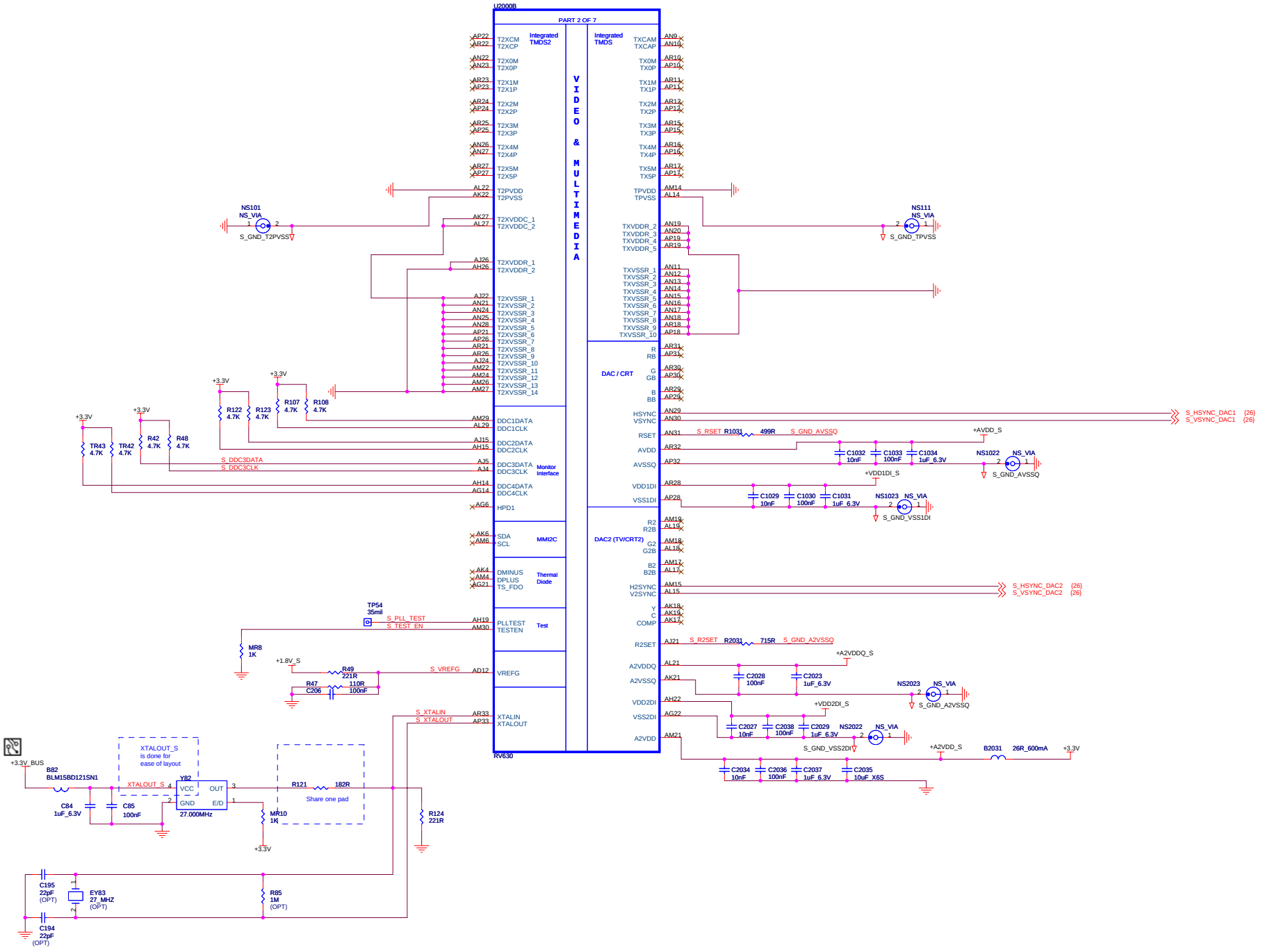

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Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402

U2000E

PART 5 OF 7

RV630

Memory I/O

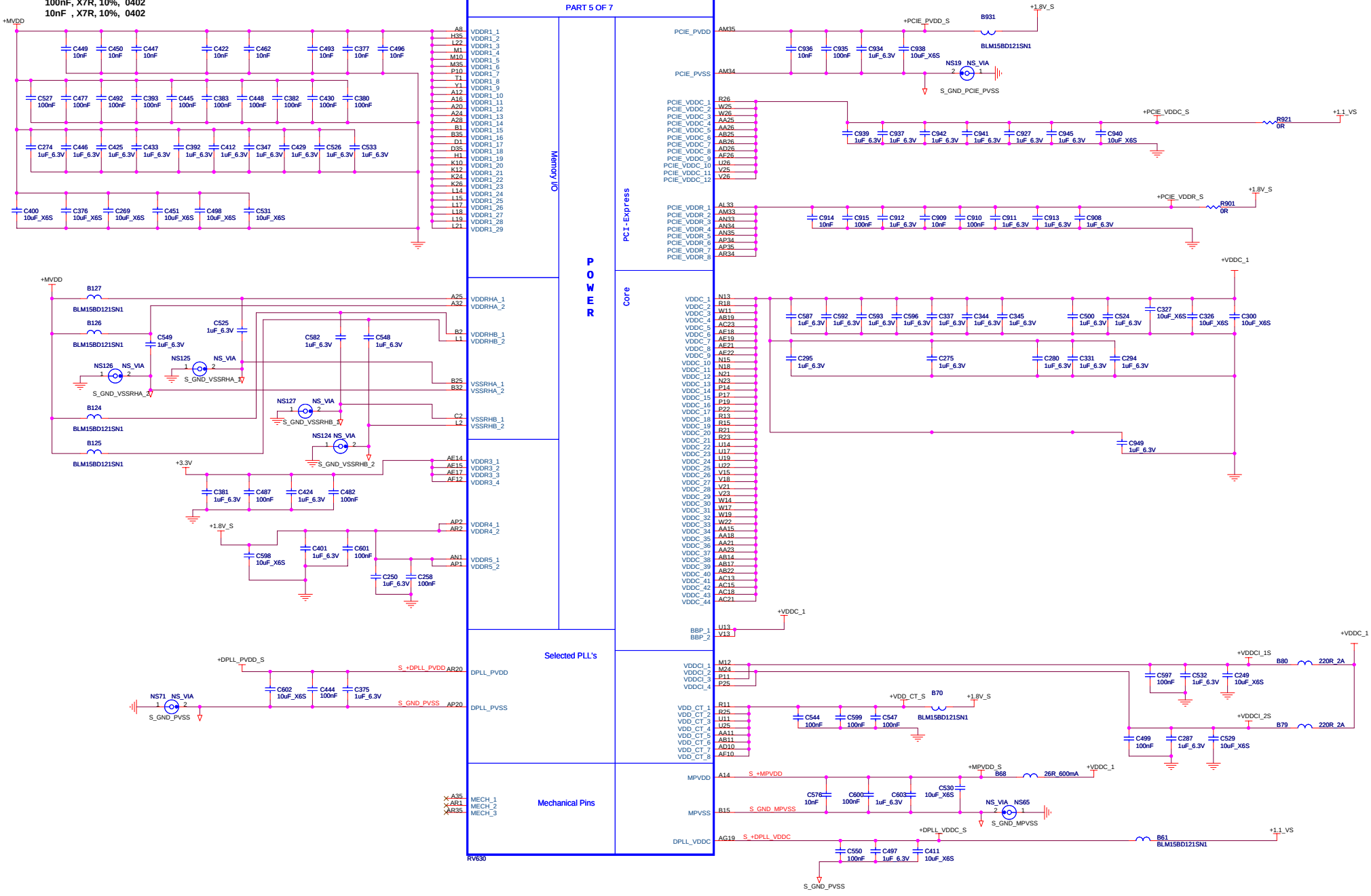
PCI-Express

Core

Selected PLL's

Mechanical Pins

POWER



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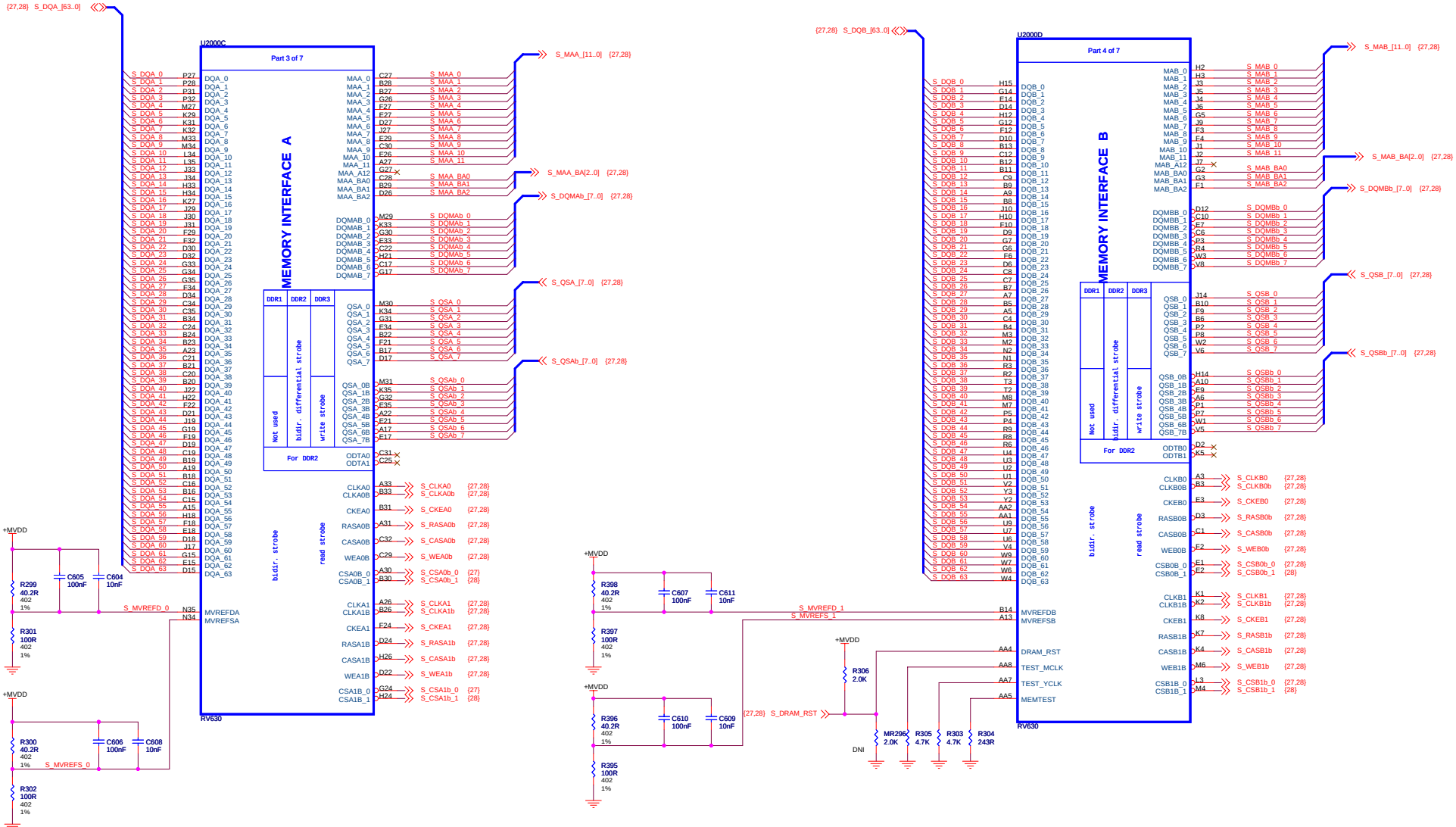

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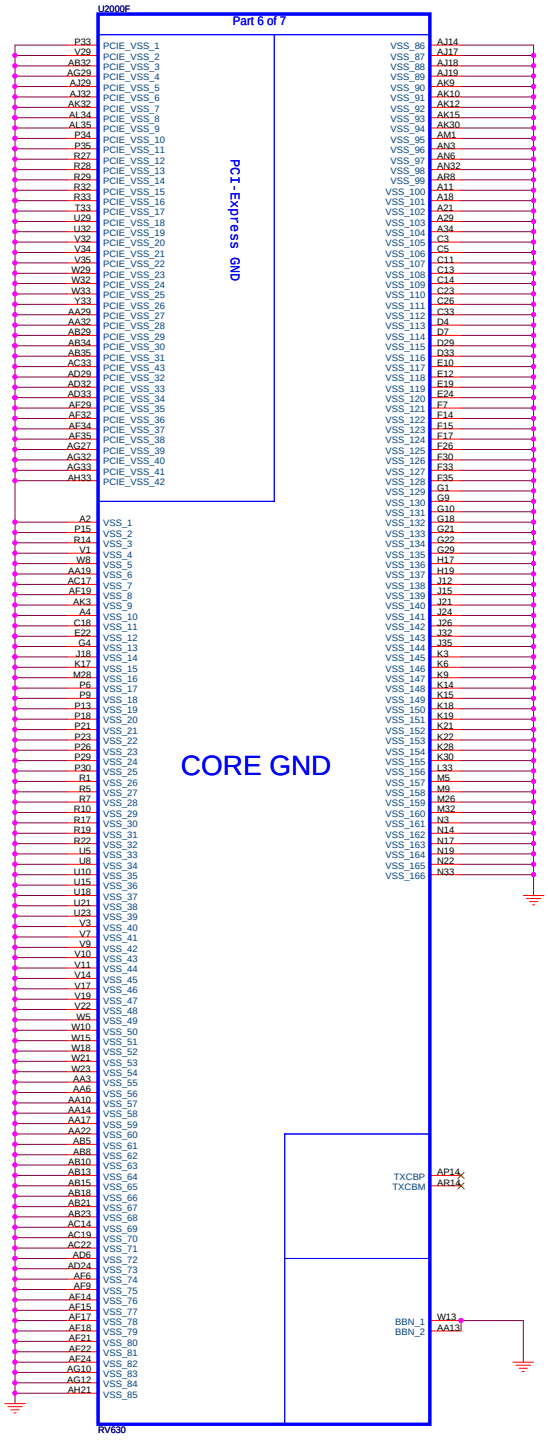

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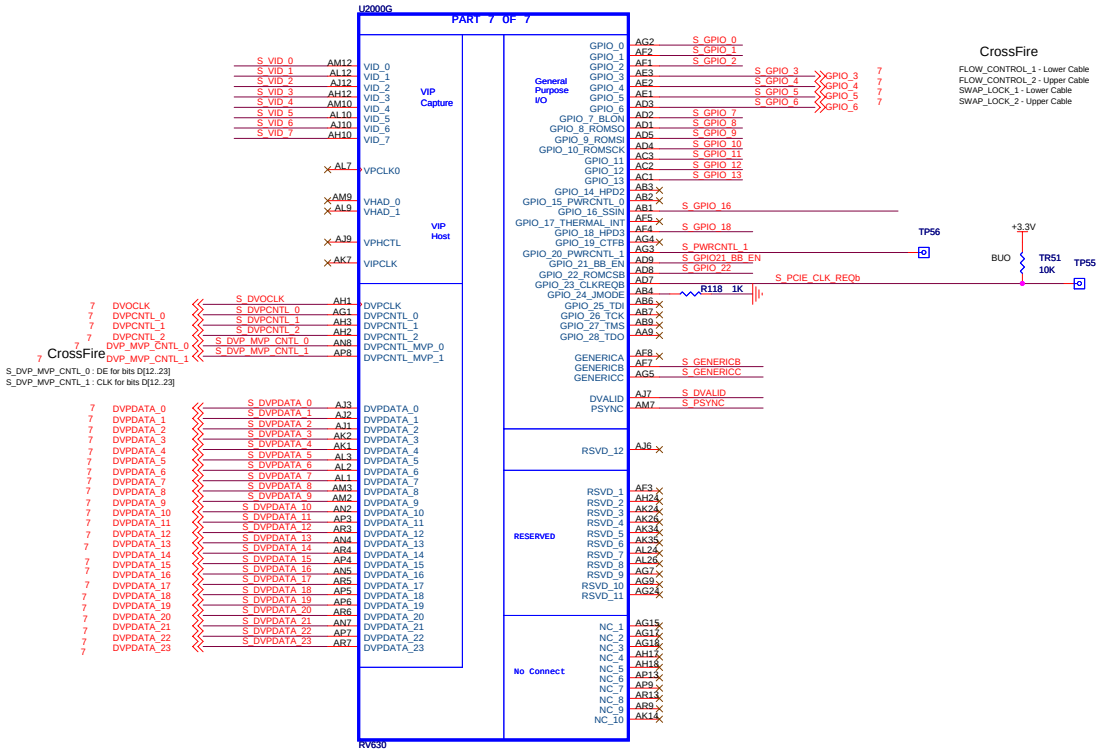
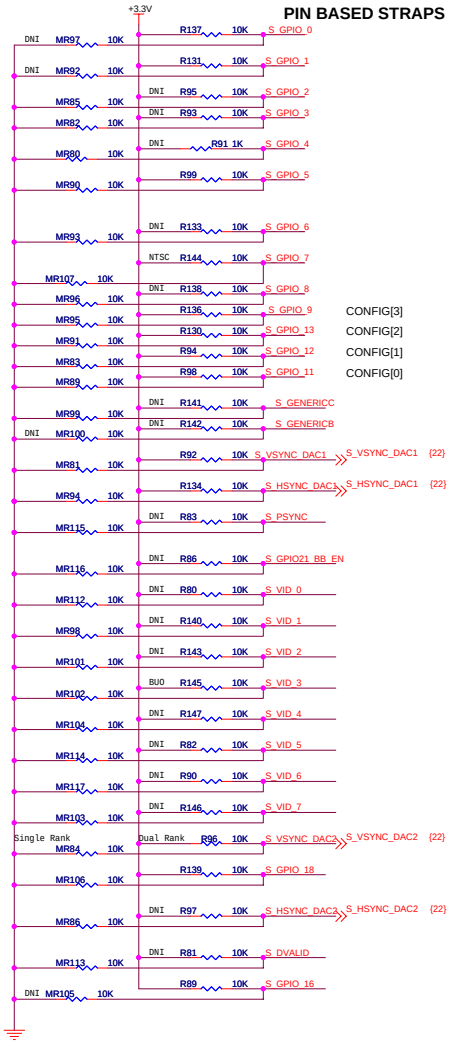




GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

AMD Internal Use Only - Reserved (Default: 00)

DEBUG_ACCESS
AMD Internal Use Only - Reserved (Default: 0)

AMD Internal Use Only - Reserved (Default: G1=0, G2=1)

AMD Internal Use Only - Reserved (Default: 0)

TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

AMD Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0]
0010 - 512Kbit AT25F512A (Atmel)
0011 - 1Mbit AT25F1024A (Atmel)
0100 - 512Kbit M25P05A (ST)
0101 - 1Mbit M25P10A (ST)
0101 - 2Mbit M25P20 (ST)
0100 - 512Kbit Pm25LV512 (Chingis)
0101 - 1Mbit Pm25LV010 (Chingis)

AMD Internal Use Only - Reserved (Default: 0)

VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

AMD Internal Use Only - Reserved (HDMI_EN =1)

VGA DISABLE : 1 for disable (set to 0 for normal operation)

AMD Internal Use Only - Reserved (Default: 0)

AMD Internal Use Only - Reserved (Default: 0)

MSI_DIS (Default: 0)

AMD Internal Use Only - Reserved (Default: 0)

BIF_AUDIO_EN
0 - Disable HD Audio 1- Enable HD Audio

AMD Internal Use Only - Reserved (Default: 0)

64BAR_EN_A (Default: 0)

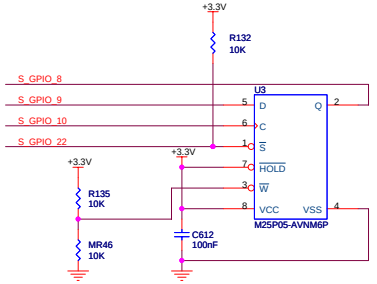
AMD Internal Use Only - Reserved (Default: 0)

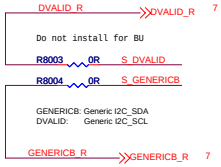
AMD Internal Use Only - Reserved (Default: 0)

MEMORY CONFIG ATI Board Feature I
V2SYNC: 0 = 1 rank of memory, 1 = 2 ranks of memory

AMD Internal Use Only - Reserved Default: 0

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability





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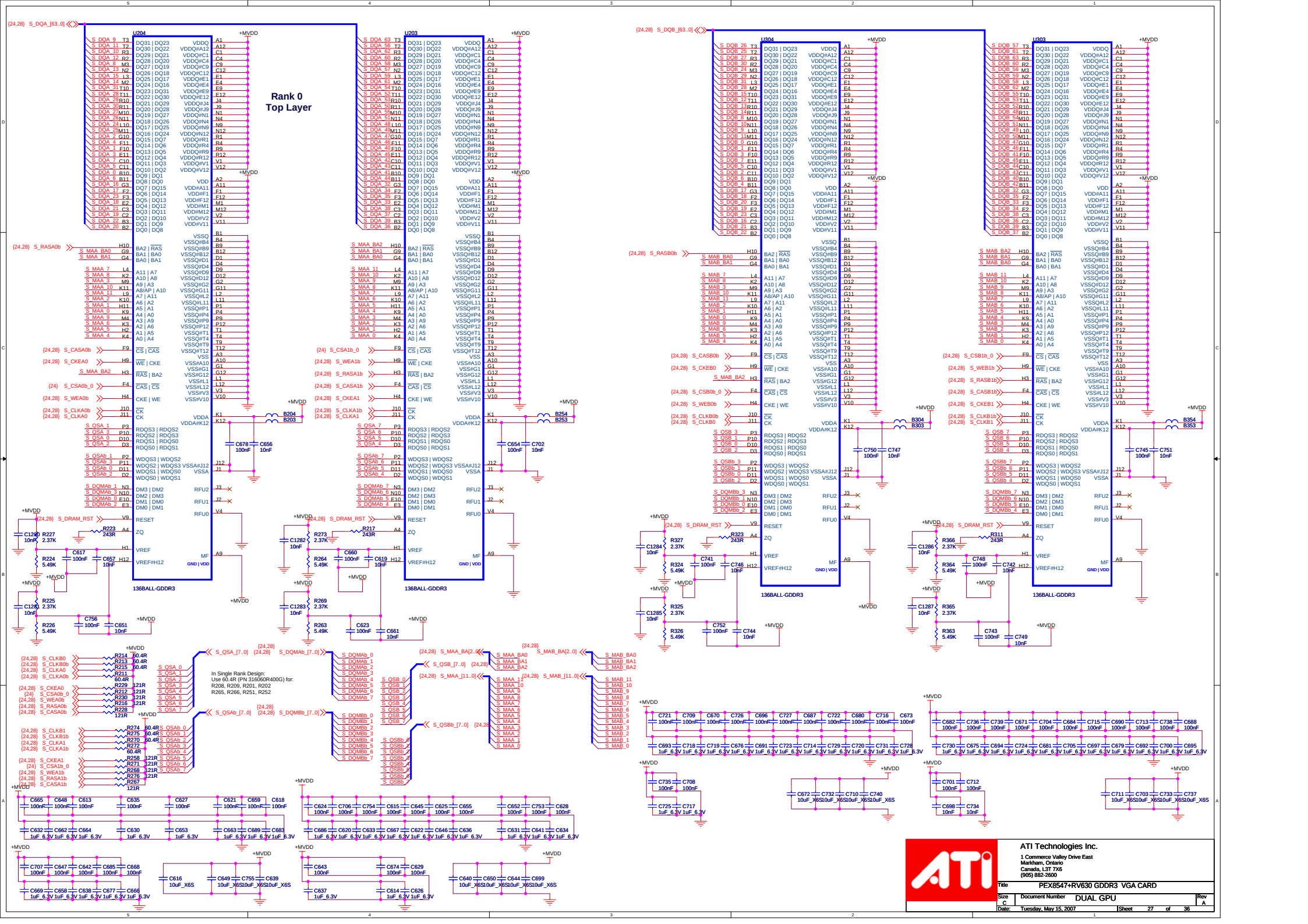
Rank 0
Top Layer
U204
U203
U304
U303
136BALL-GDDR3
In Single Rank Design:
Use 60.4R (PN 316060R400G) for:
R208, R209, R201, R202
R265, R266, R251, R252
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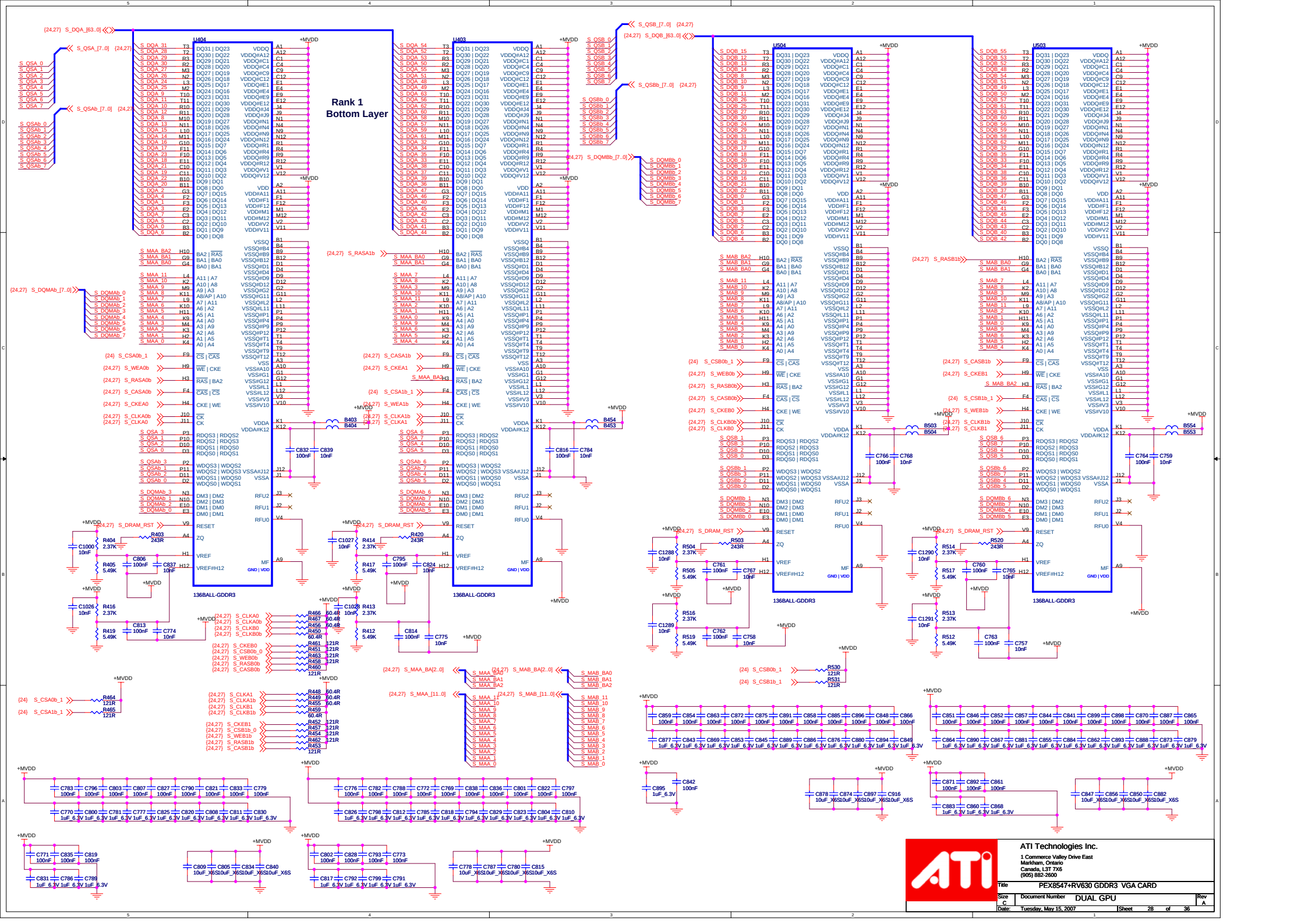
Rank 1
Bottom Layer
U404
U403
U504
U503
136BALL-GDDR3
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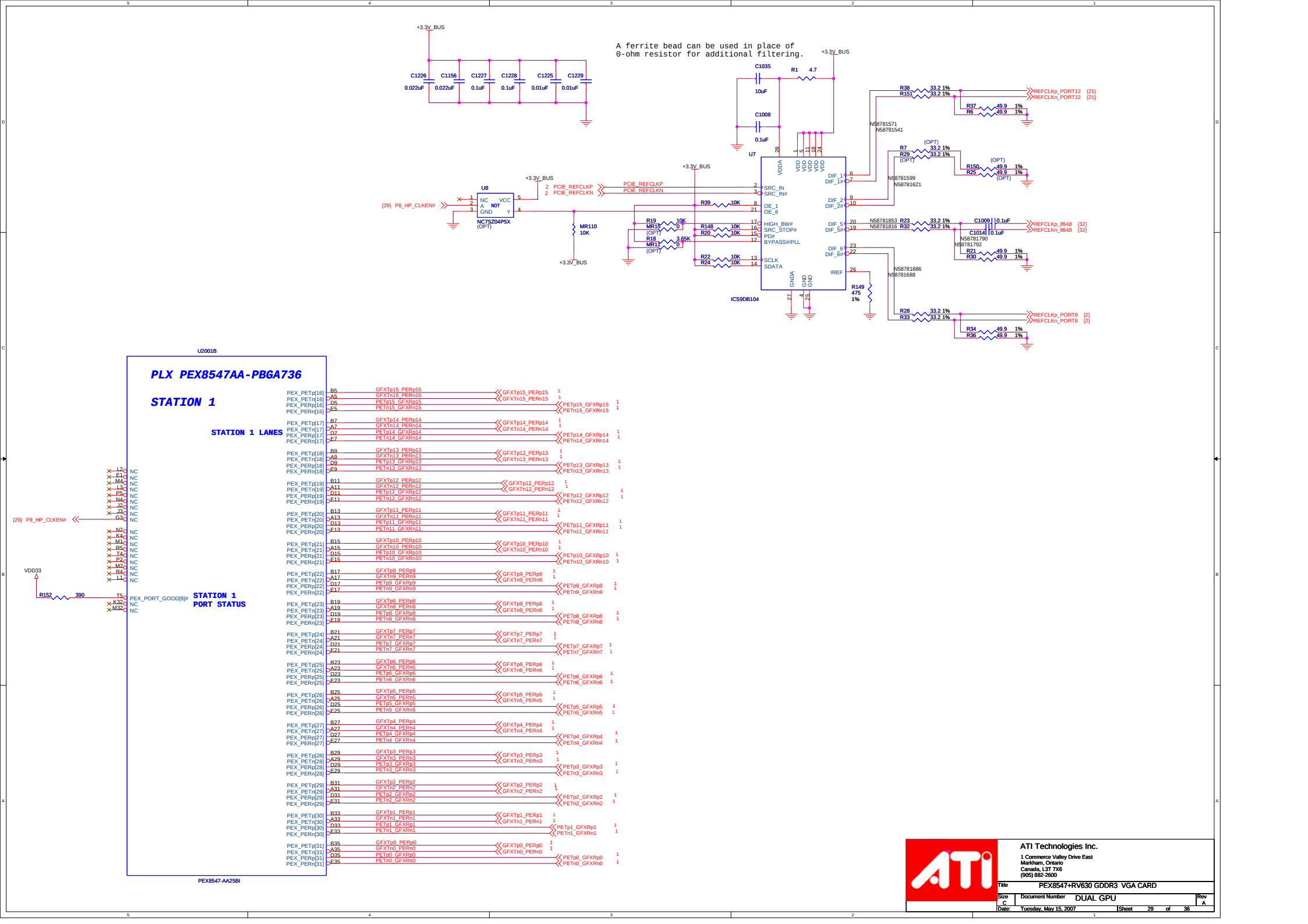

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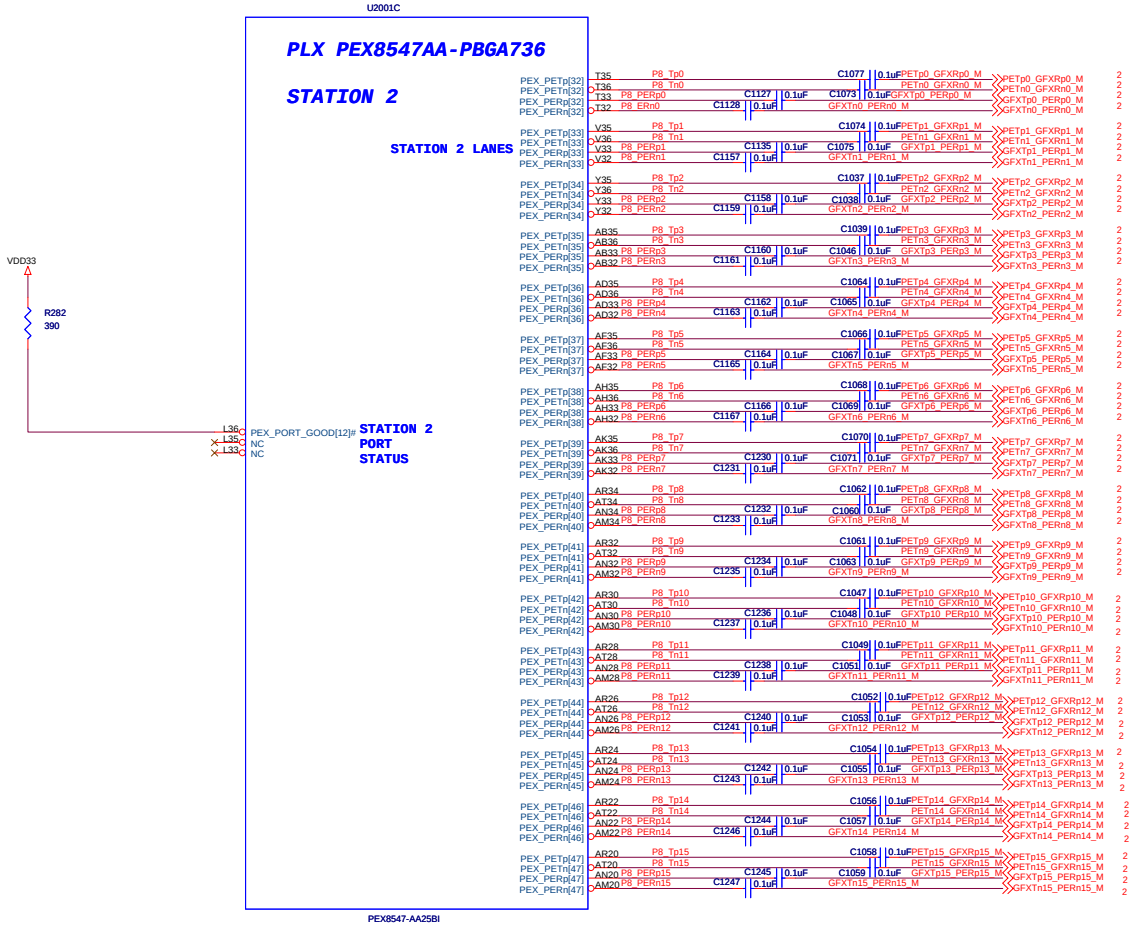

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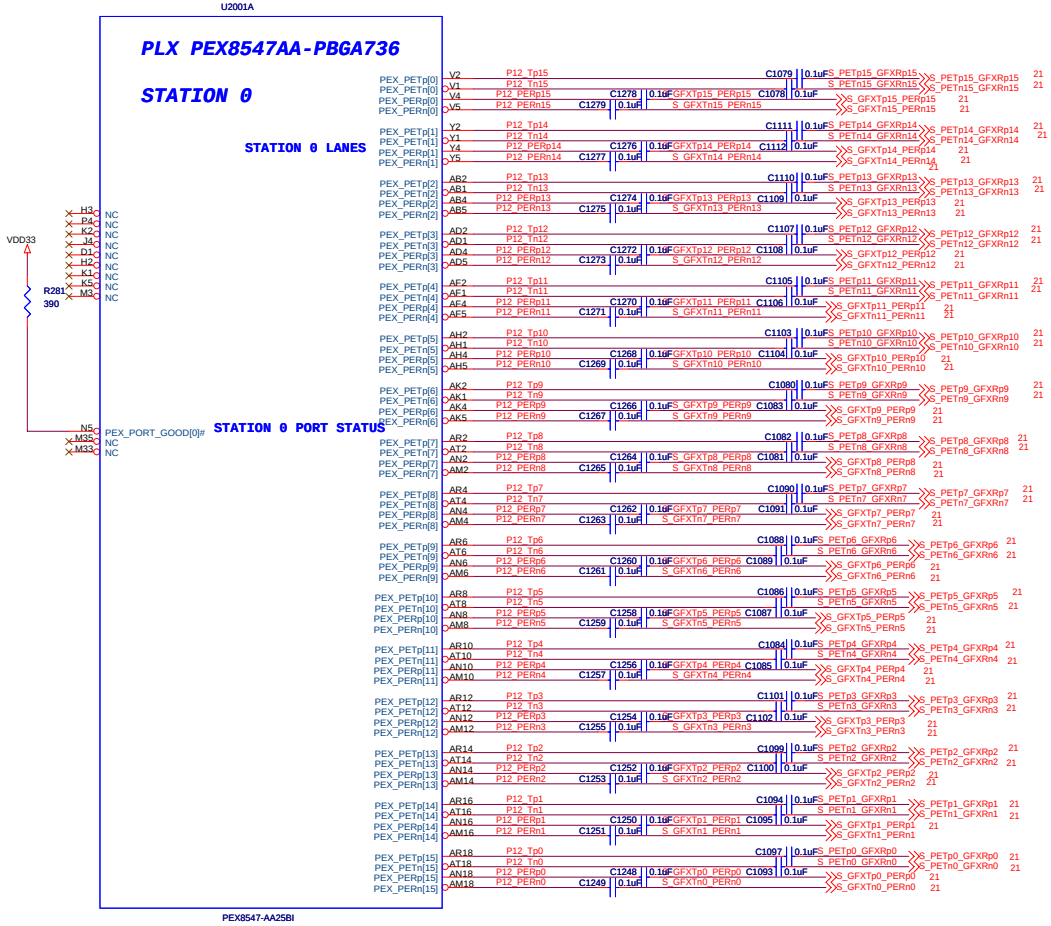

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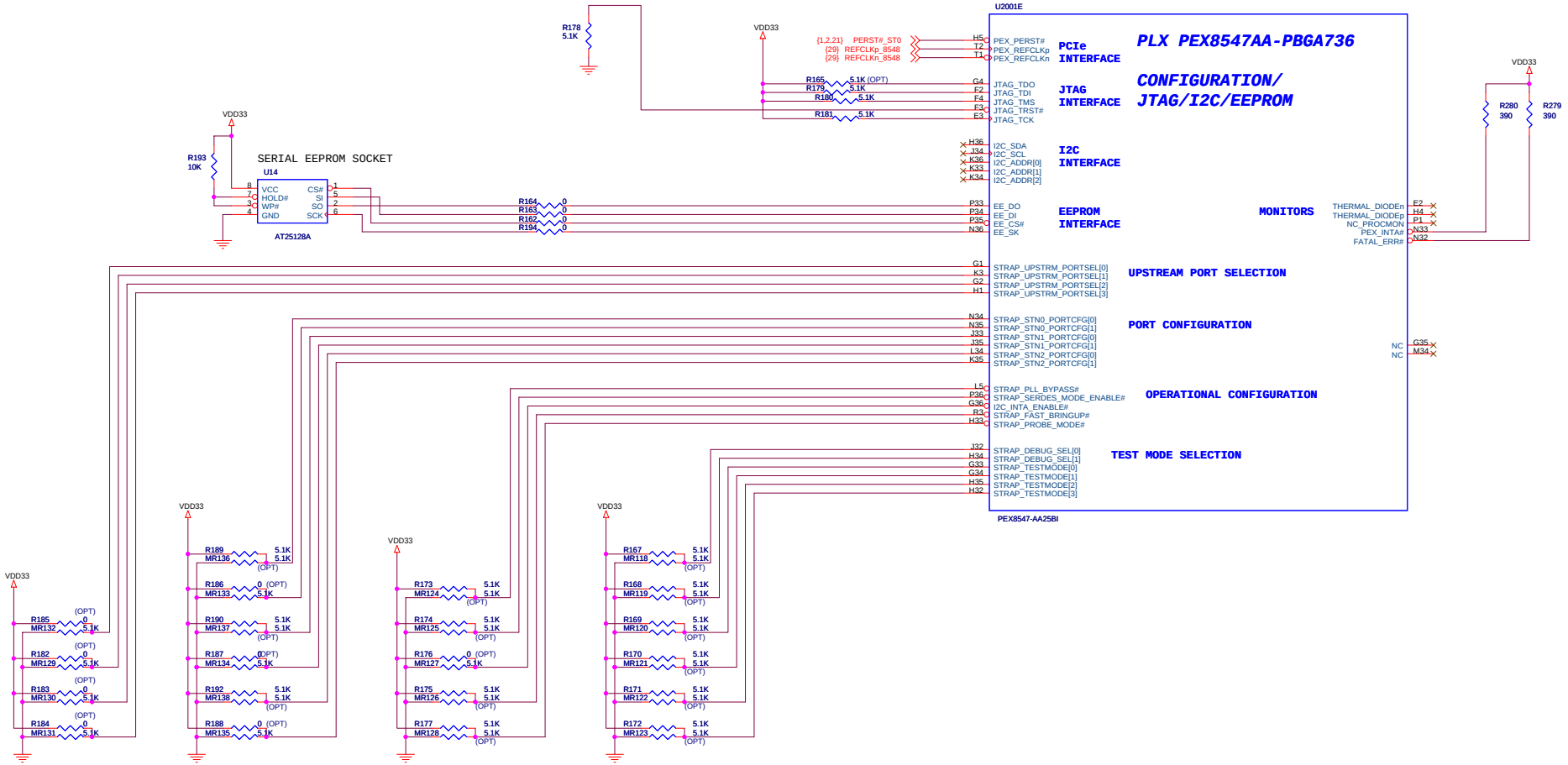

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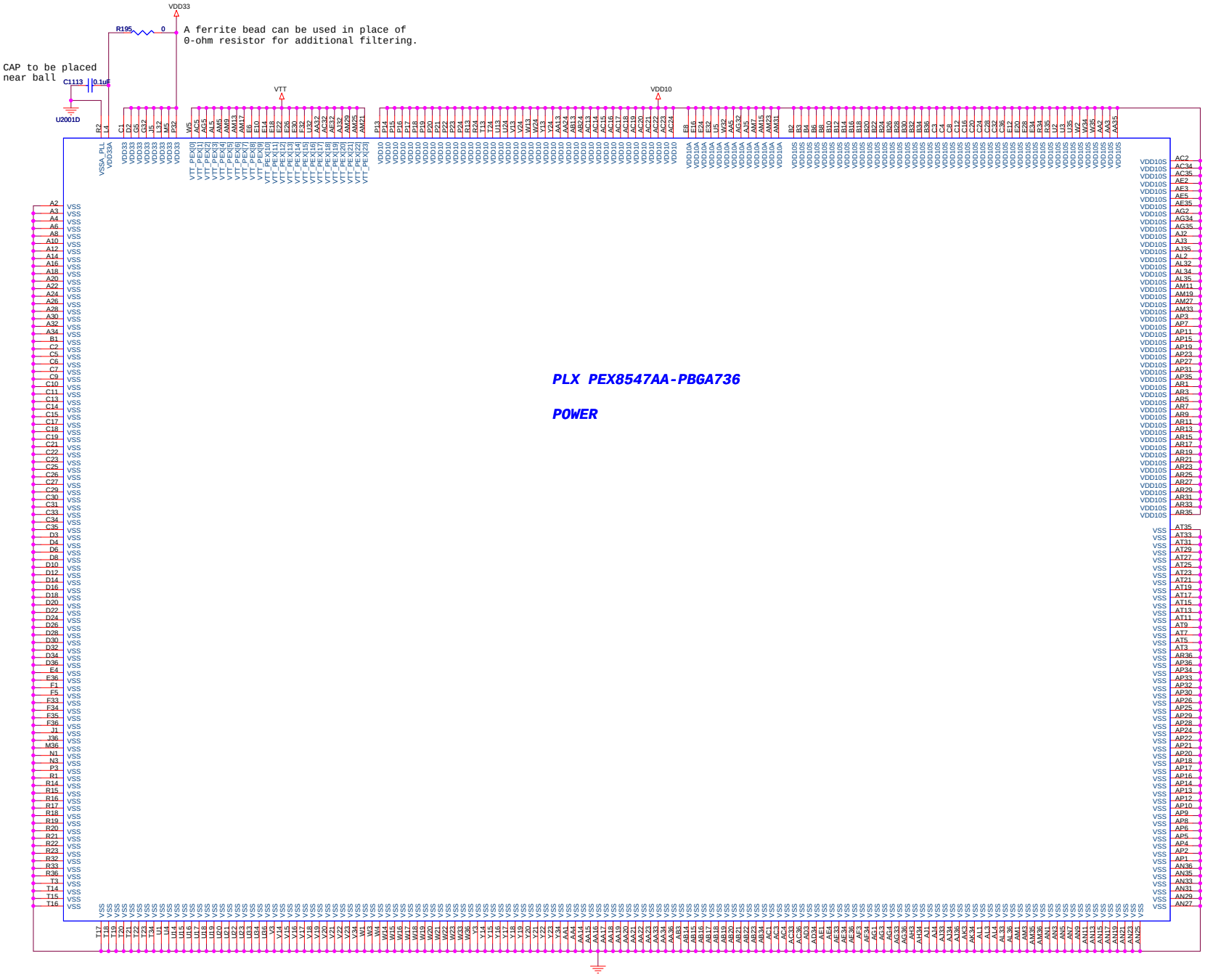

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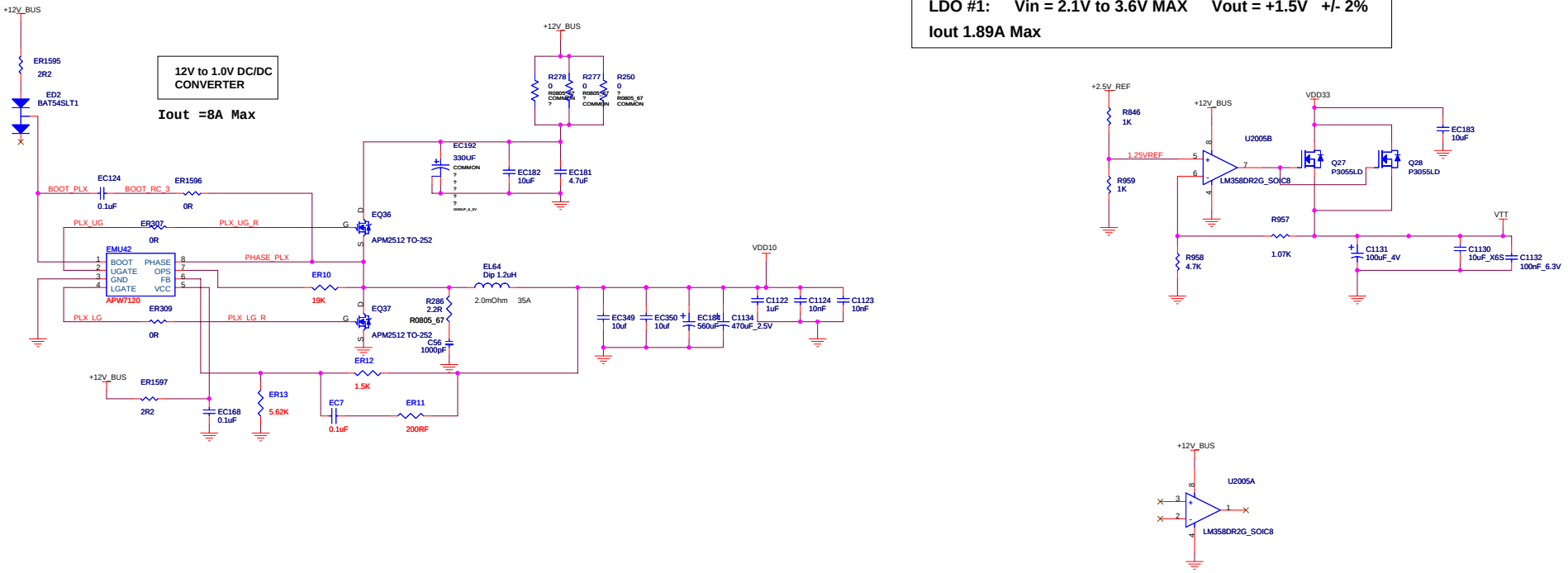
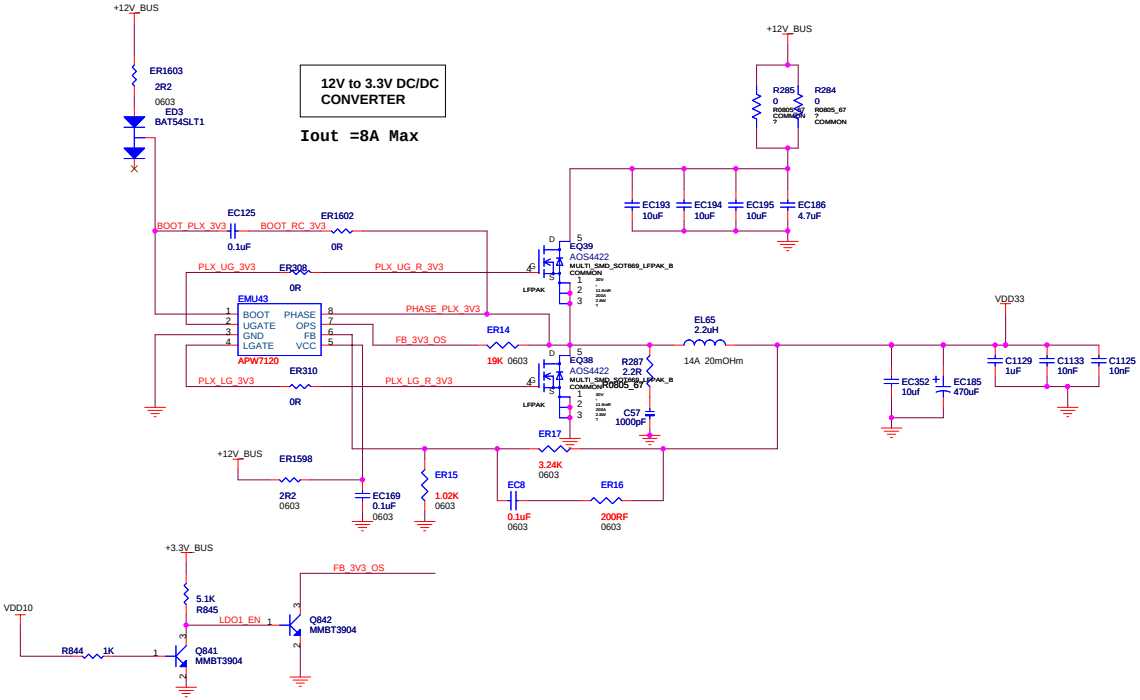
LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.5V +/- 2%
Iout 1.89A Max





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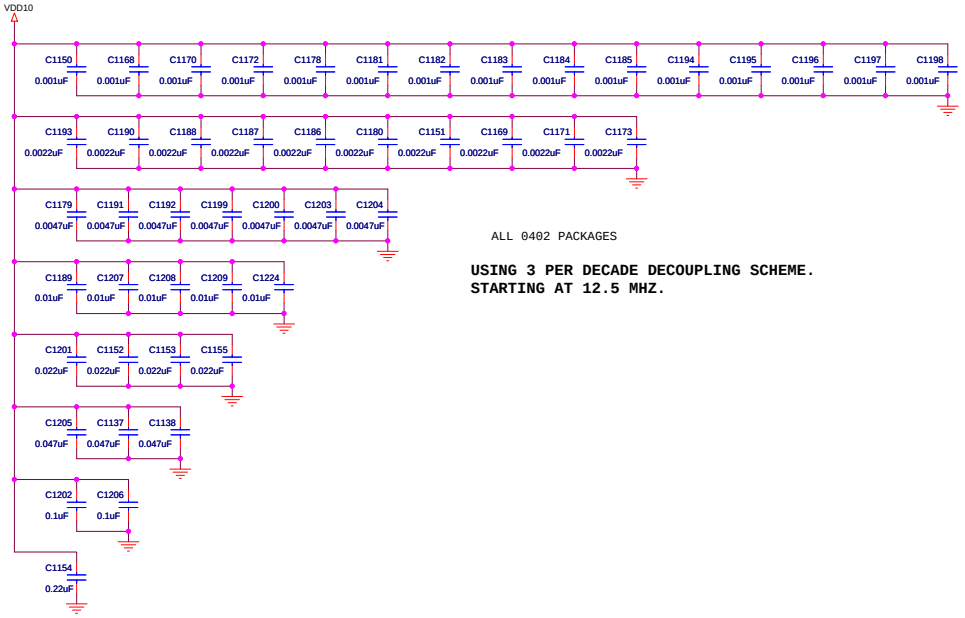
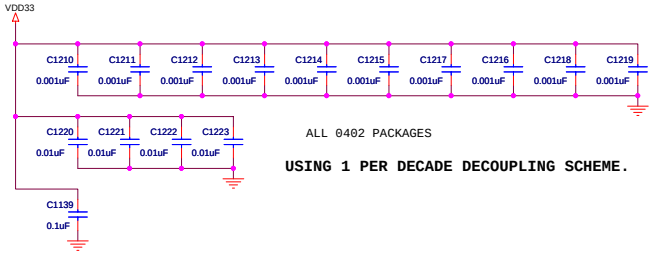


ALL 0402 PACKAGES

USING 3 PER DECADE DECOUPLING SCHEME.
STARTING AT 12.5 MHZ.



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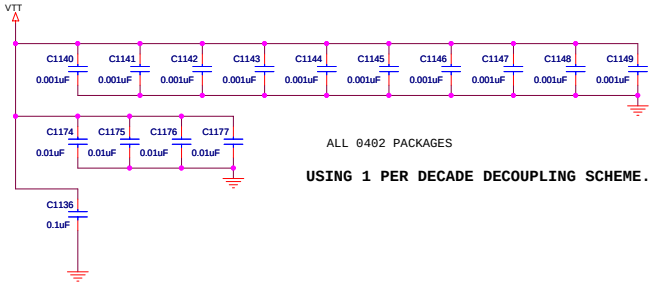
USING 1 PER DECADE DECOUPLING SCHEME.



ALL 0402 PACKAGES

USING 1 PER DECADE DECOUPLING SCHEME.

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