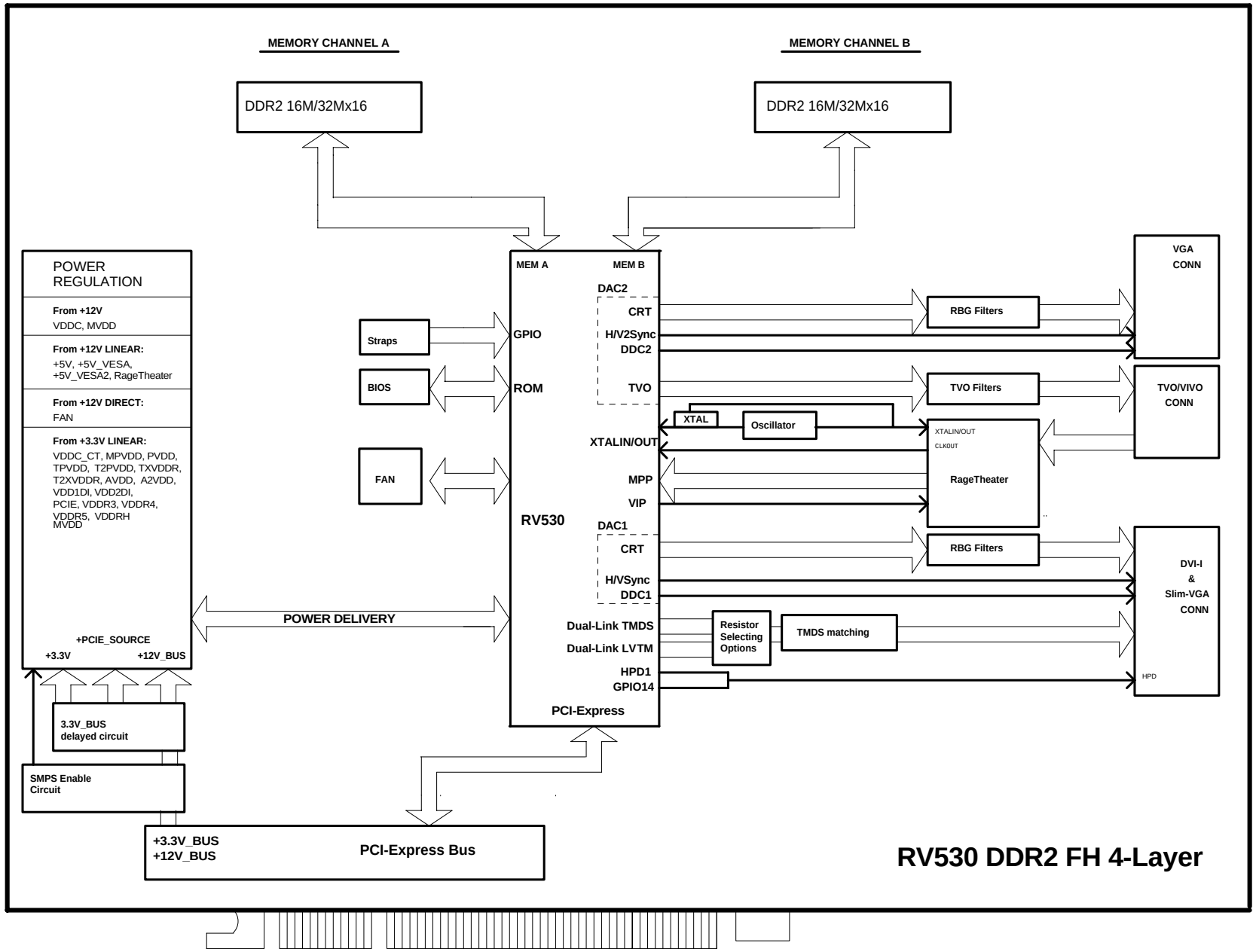

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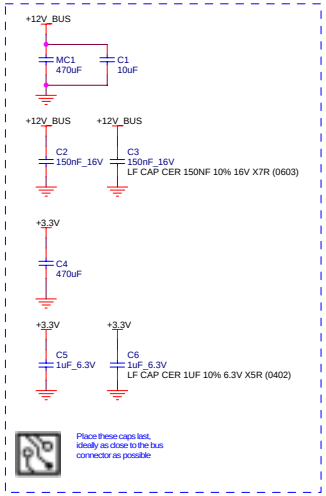
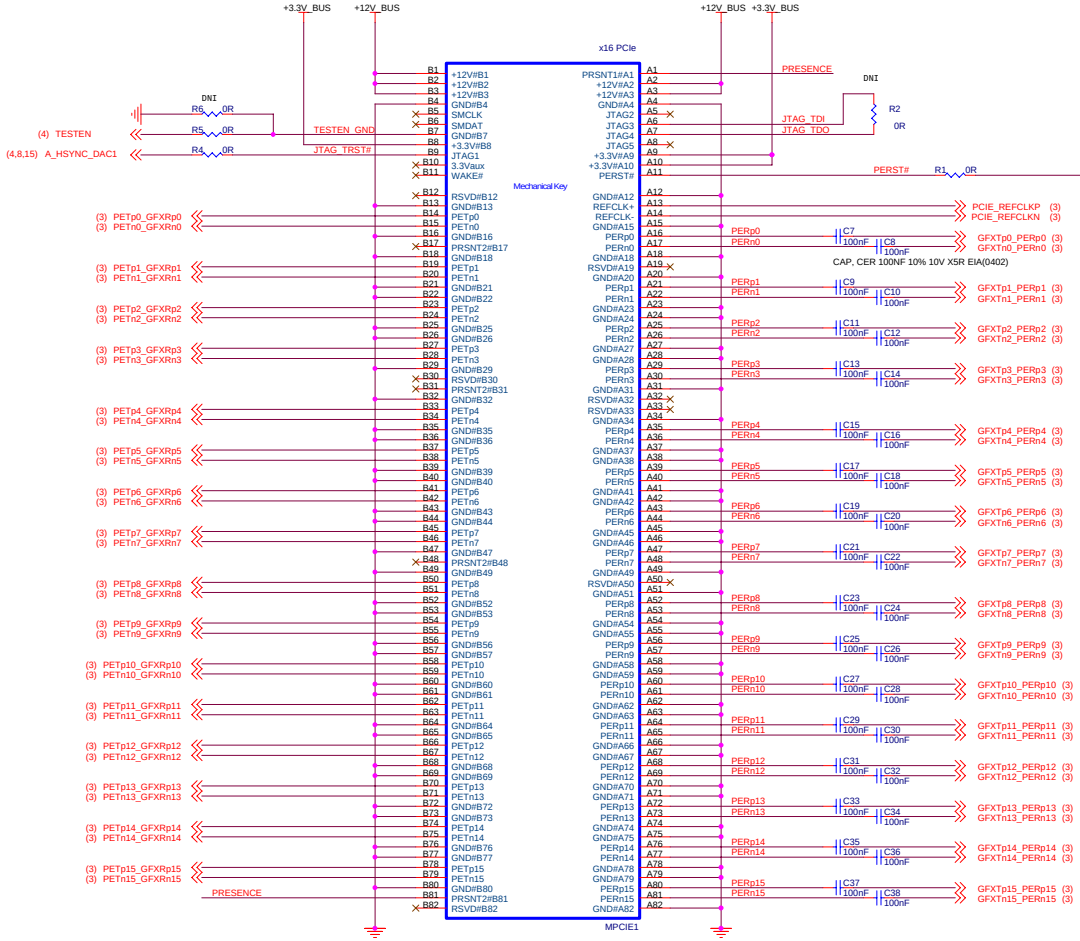
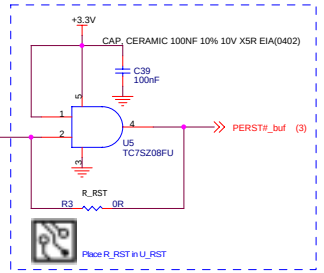
PCI-EXPRESS EDGE CONNECTOR







Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

Micro-Star International Co., LTD.

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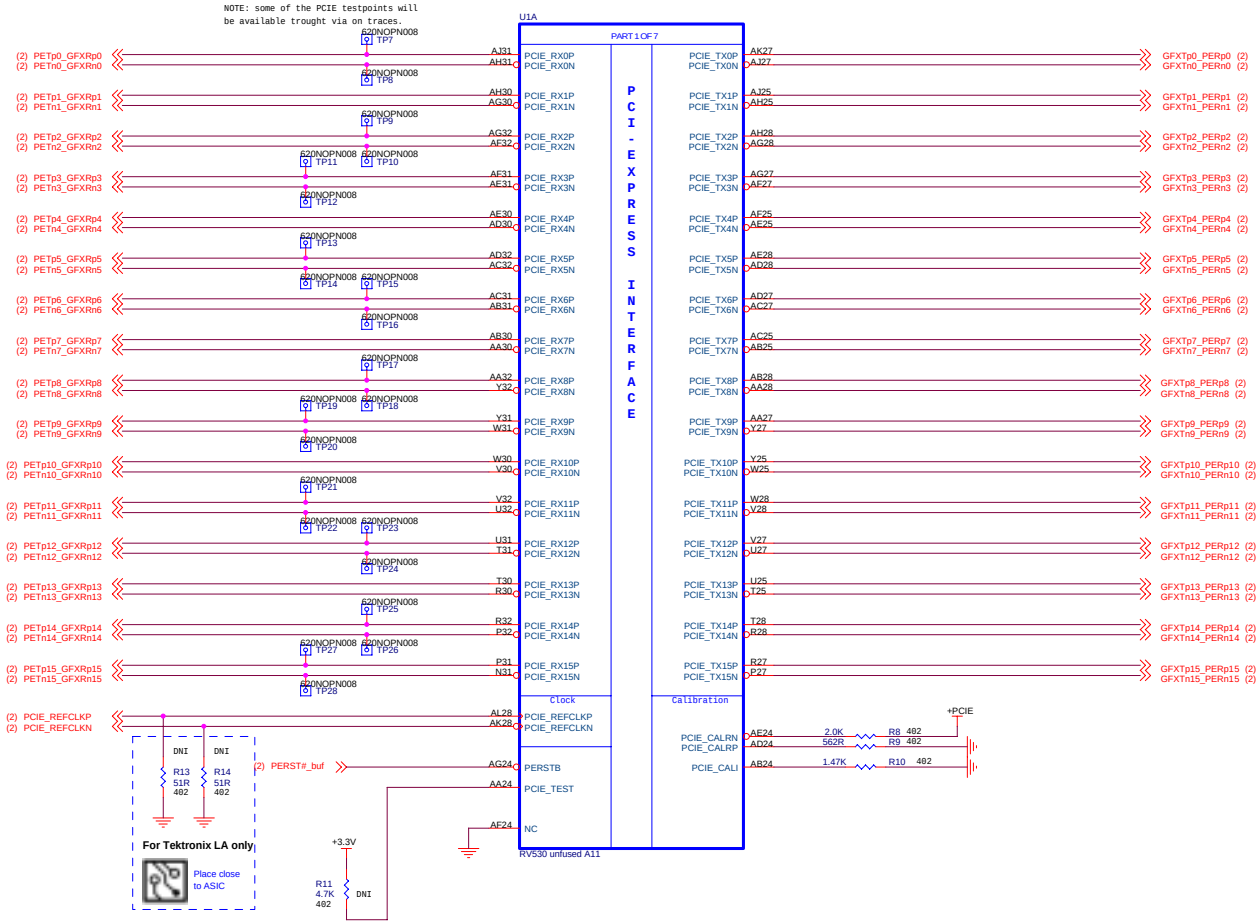

Micro-Star International Co., LTD.			
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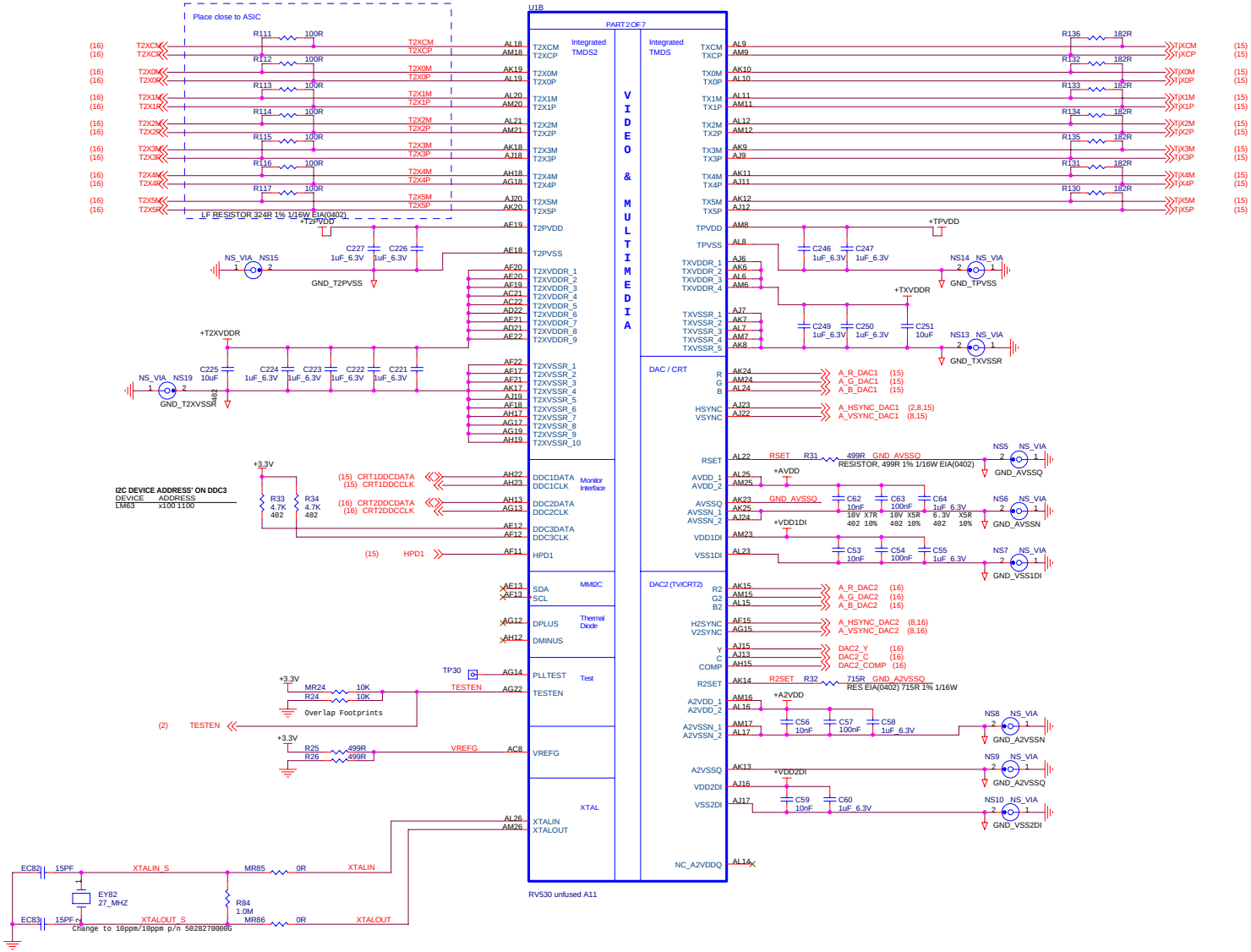

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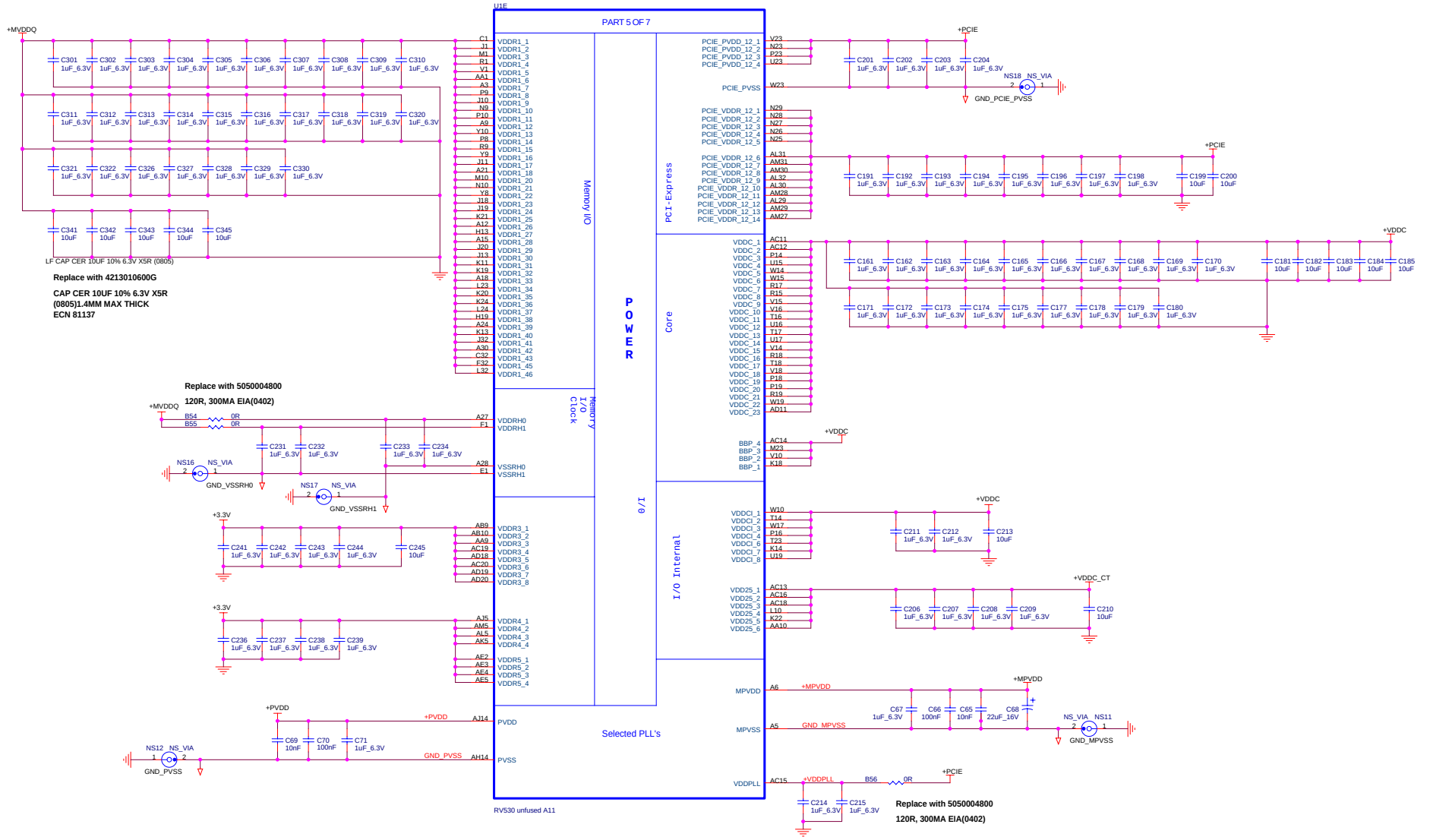

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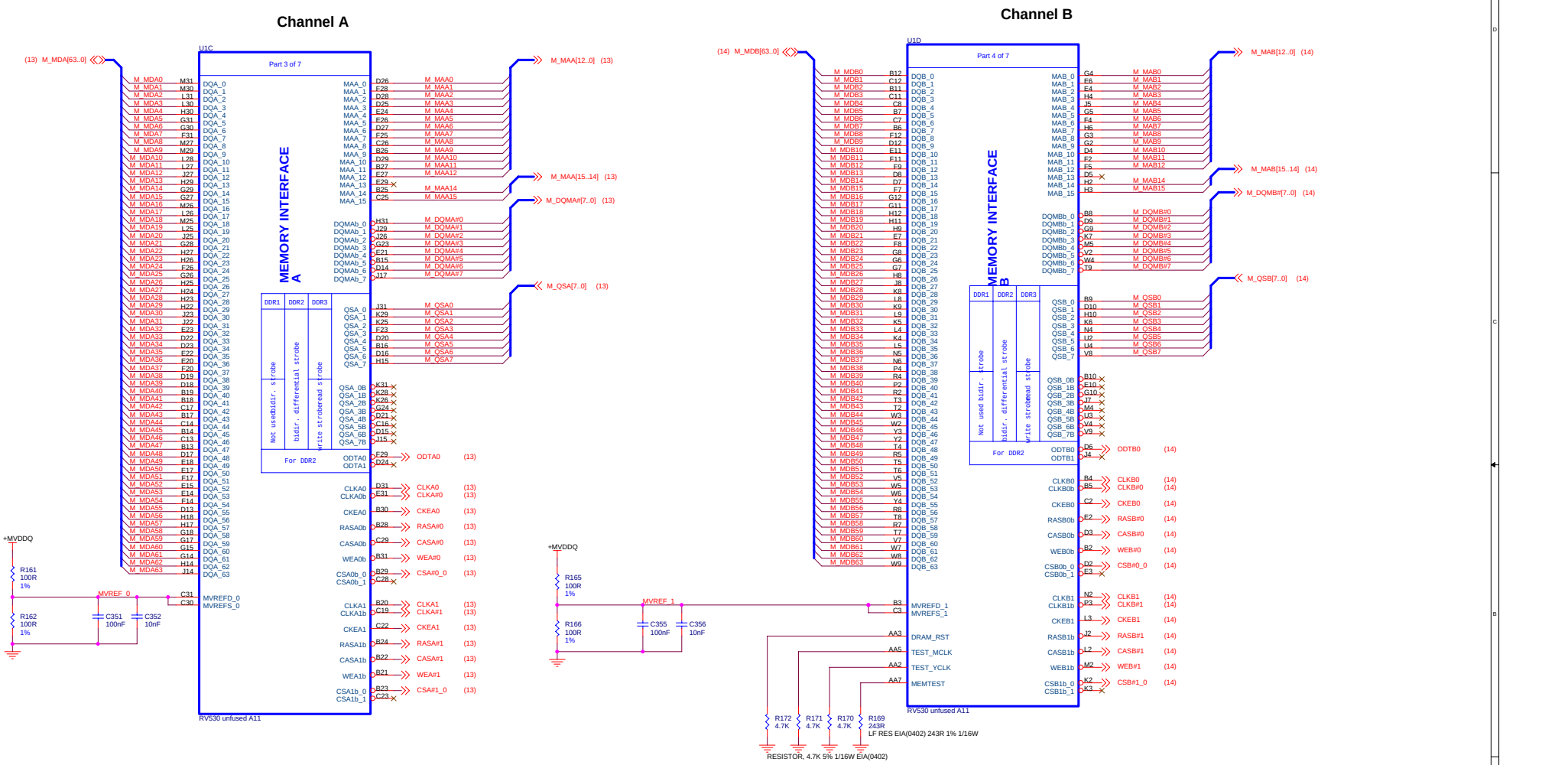
RV530 MEMORY CHANNELS A and B



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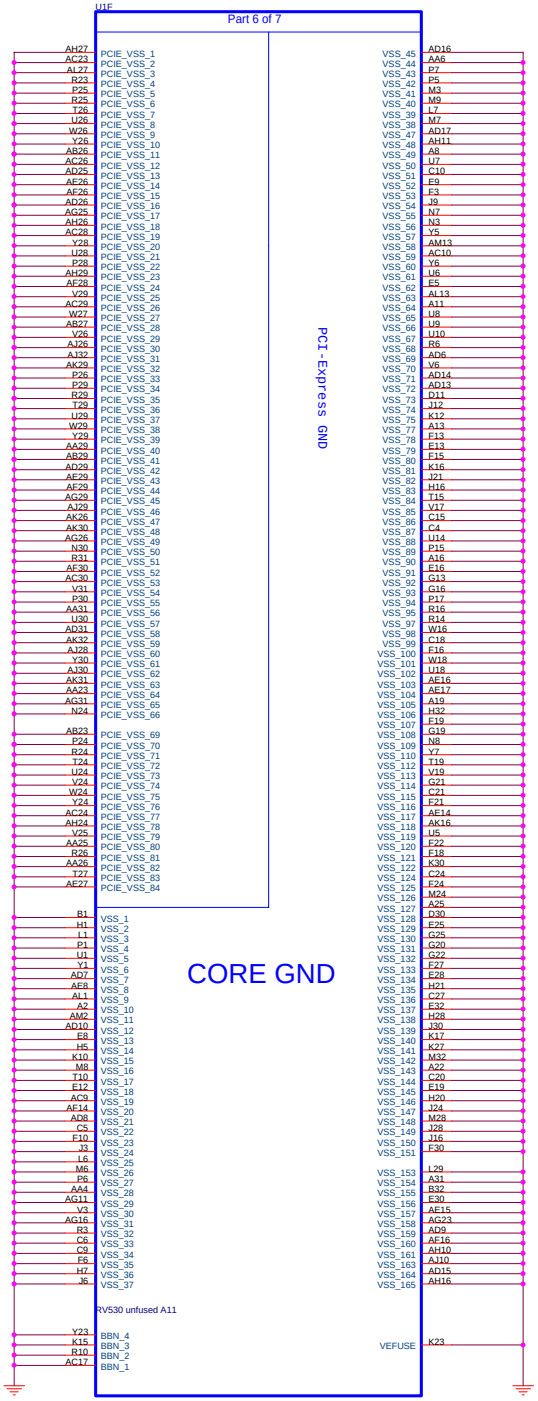

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MS-V040 RV530/DDRII			
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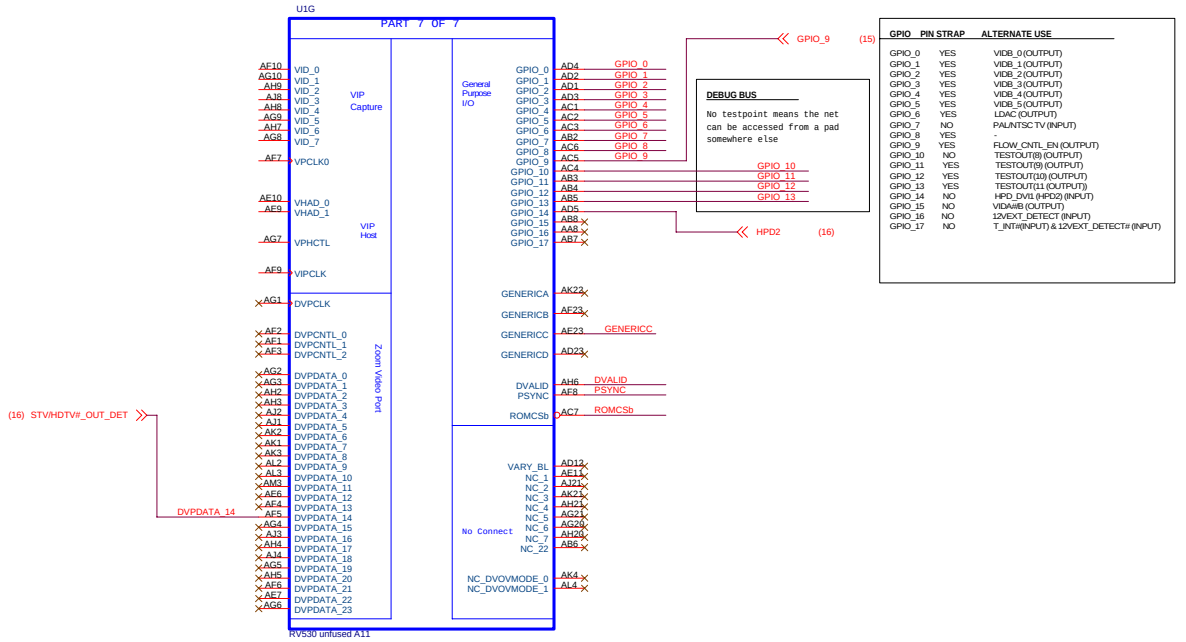
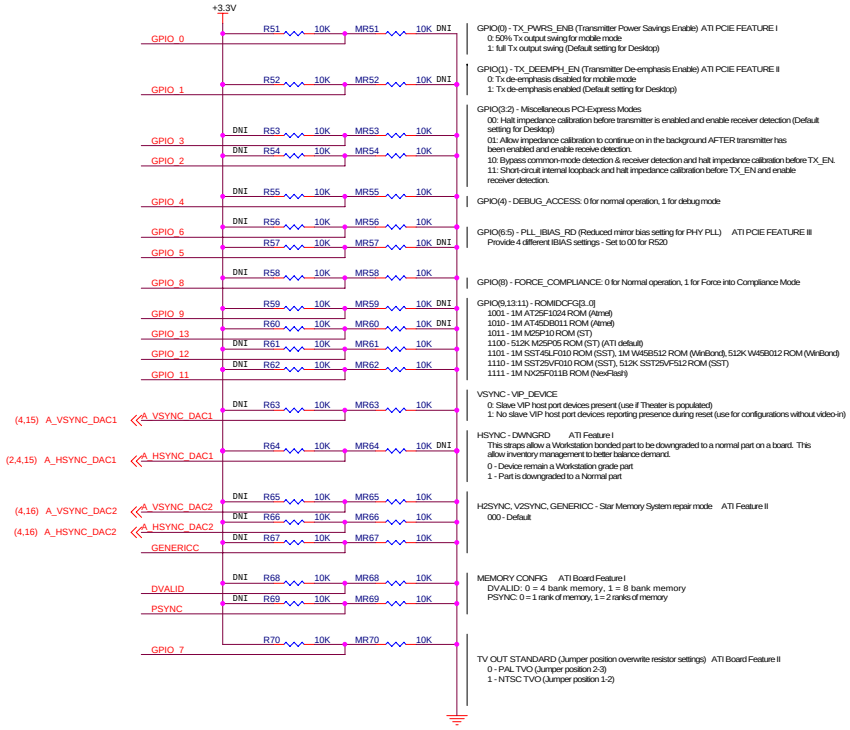
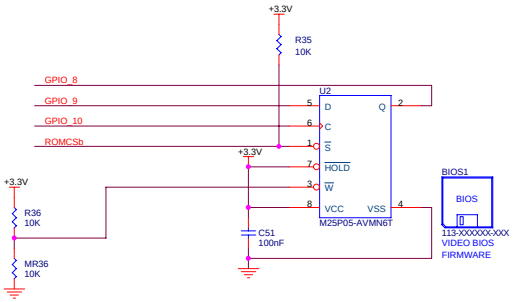


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDAal/B (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

PIN BASED STRAPS





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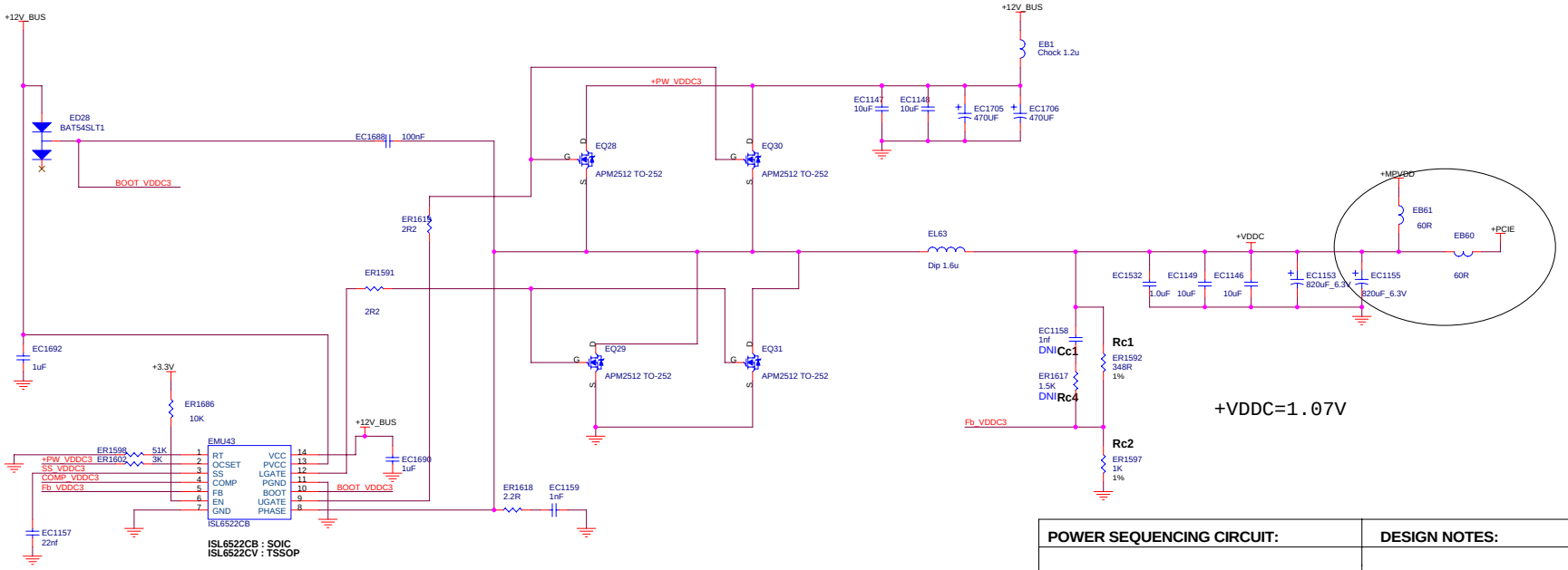
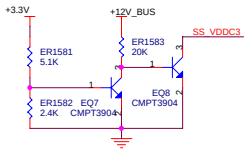
CORE REGULATOR VDDC



+VDDC=1.07V

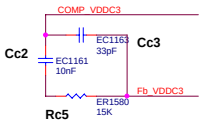
Lower MOSFET should be surrounded by a lot of copper for heat dissipation

POWER SEQUENCING CIRCUIT:



DESIGN NOTES:

Compensation Circuit



FOR ALTERNATE #1

Remove R374, R375, R371, C168 and U32

Install R370, R112, R954, R305-R308, C166, C159 and MU32

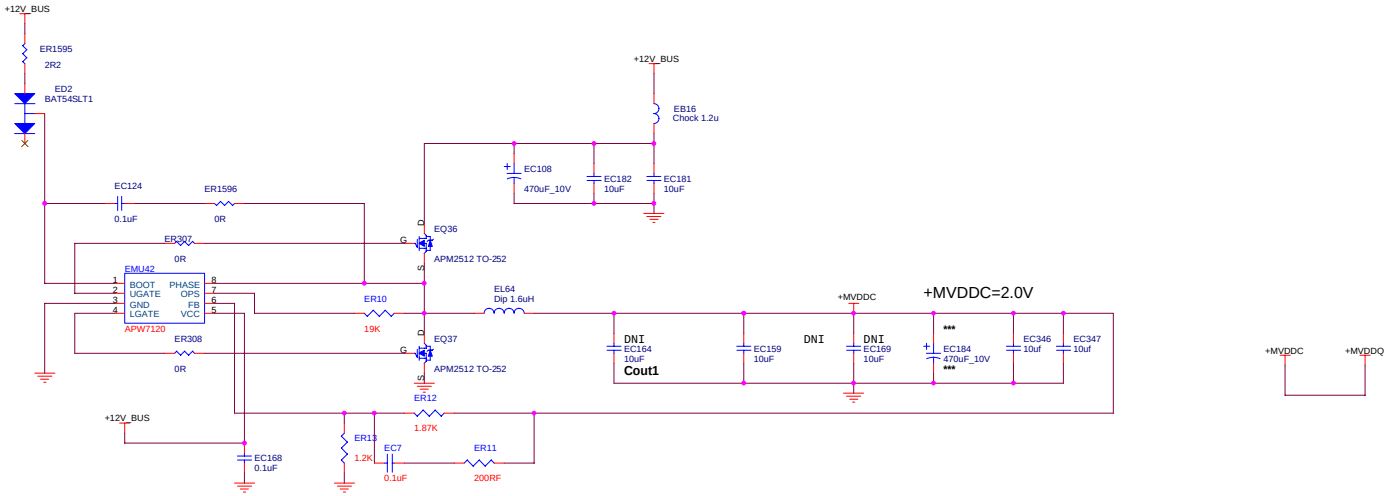
FOR ALTERNATE #2

Change C157 for 10 uF and C121 for 1 uF
Replace C764 by 0 Ohm resistor
Replace R314 with a bead
Remove R954, R370, R305-R308, C159, R112, C160 and MU32

Install R374, R375, R371, C168 and U32

Compensation circuit

Rc1 = 10K, Rc2 = 8.06K
R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF



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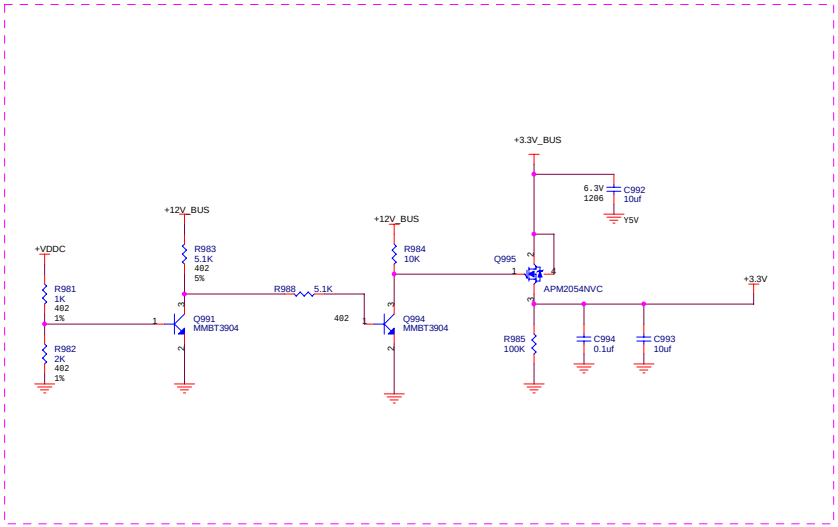

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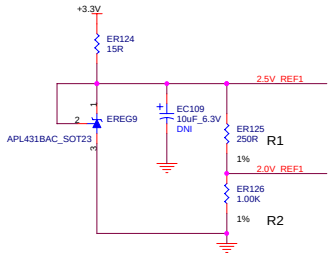

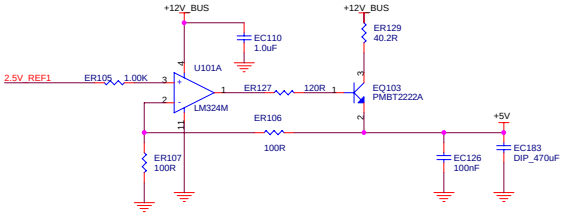

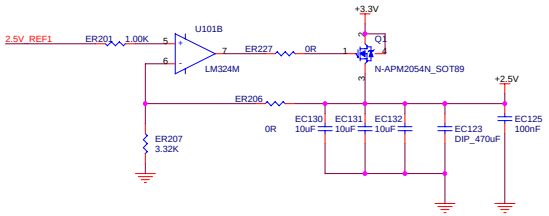

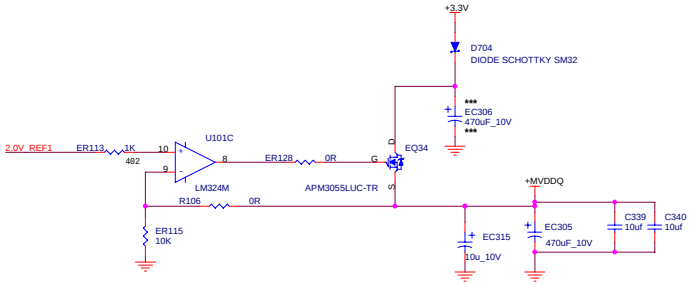

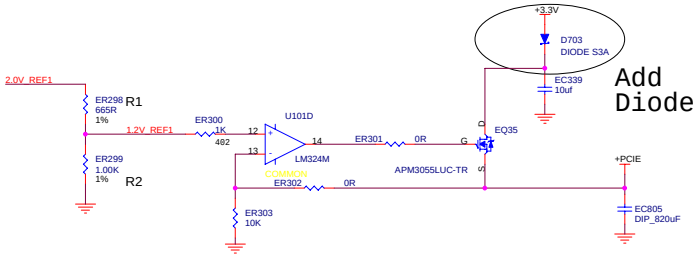

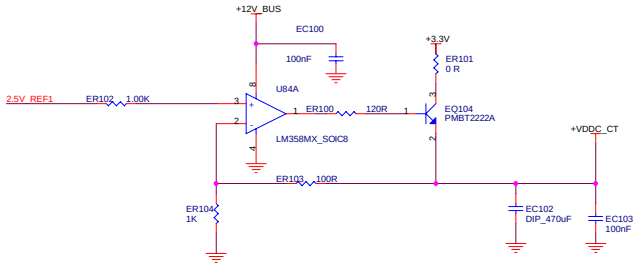

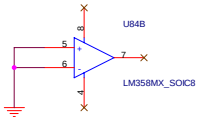

Replace with 5050004800
120R, 300MA EIA(0402)

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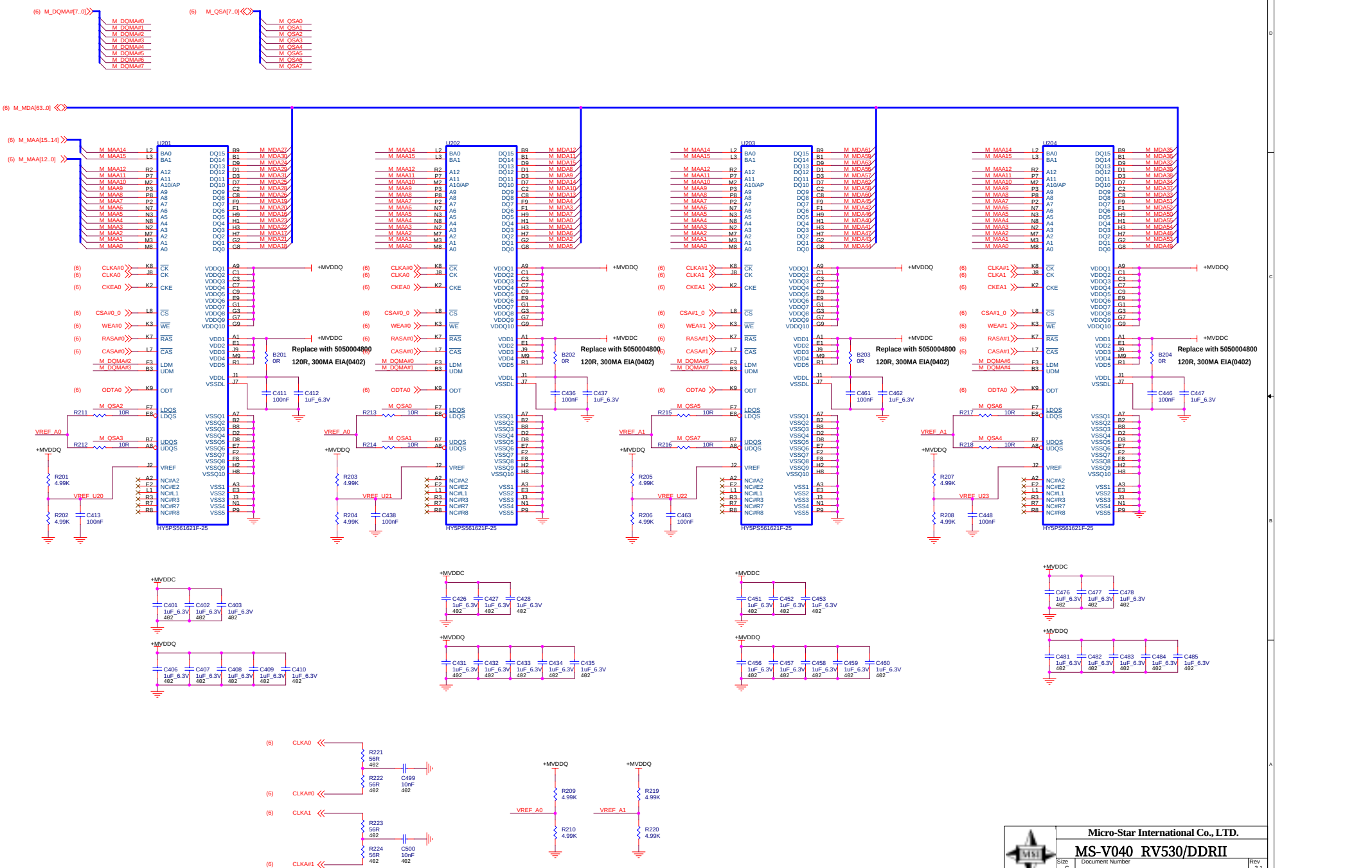
CHANNEL A: RANK 0 128MB DDR2



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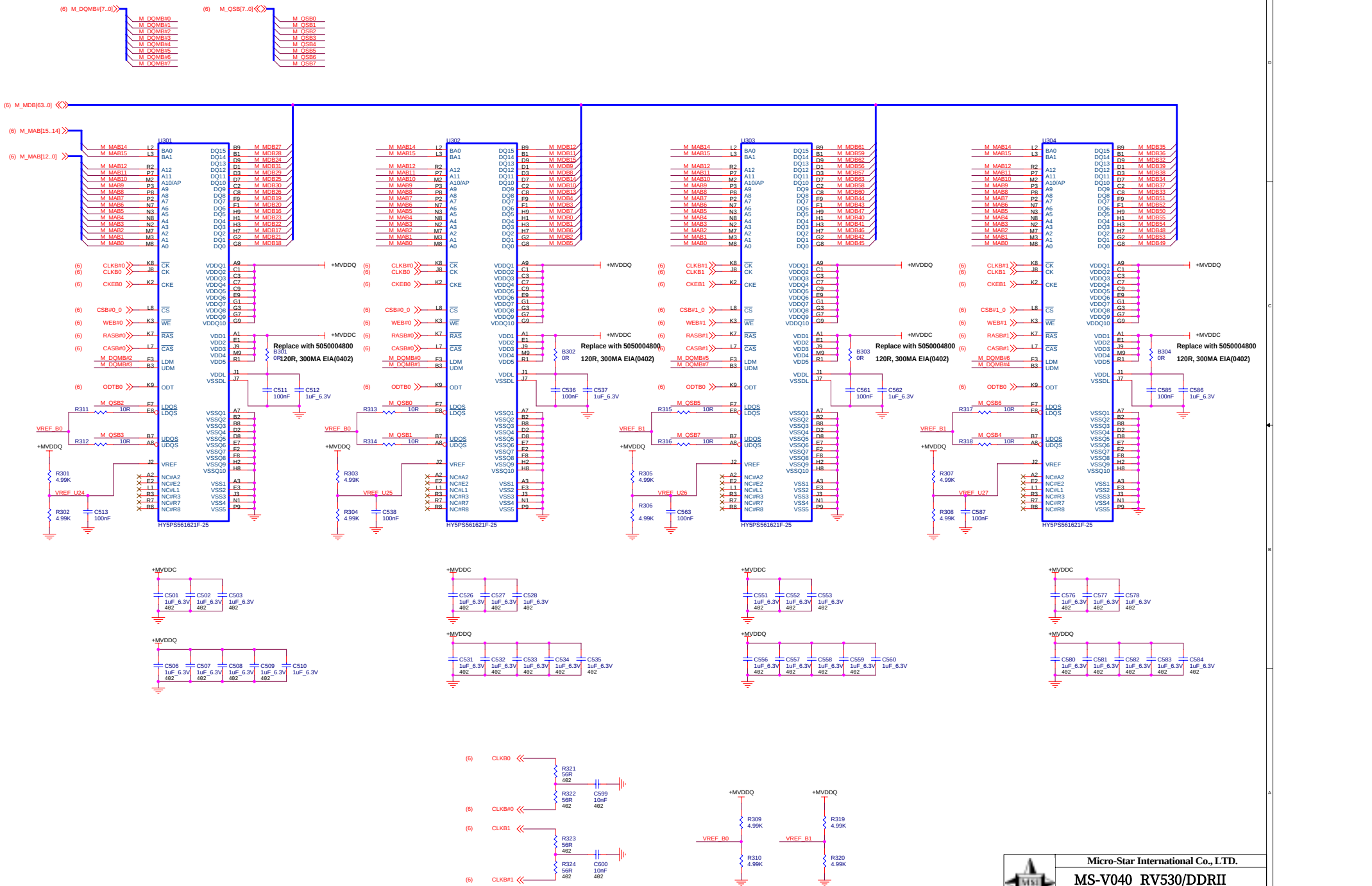
CHANNEL B: RANK 0 128MB DDR2



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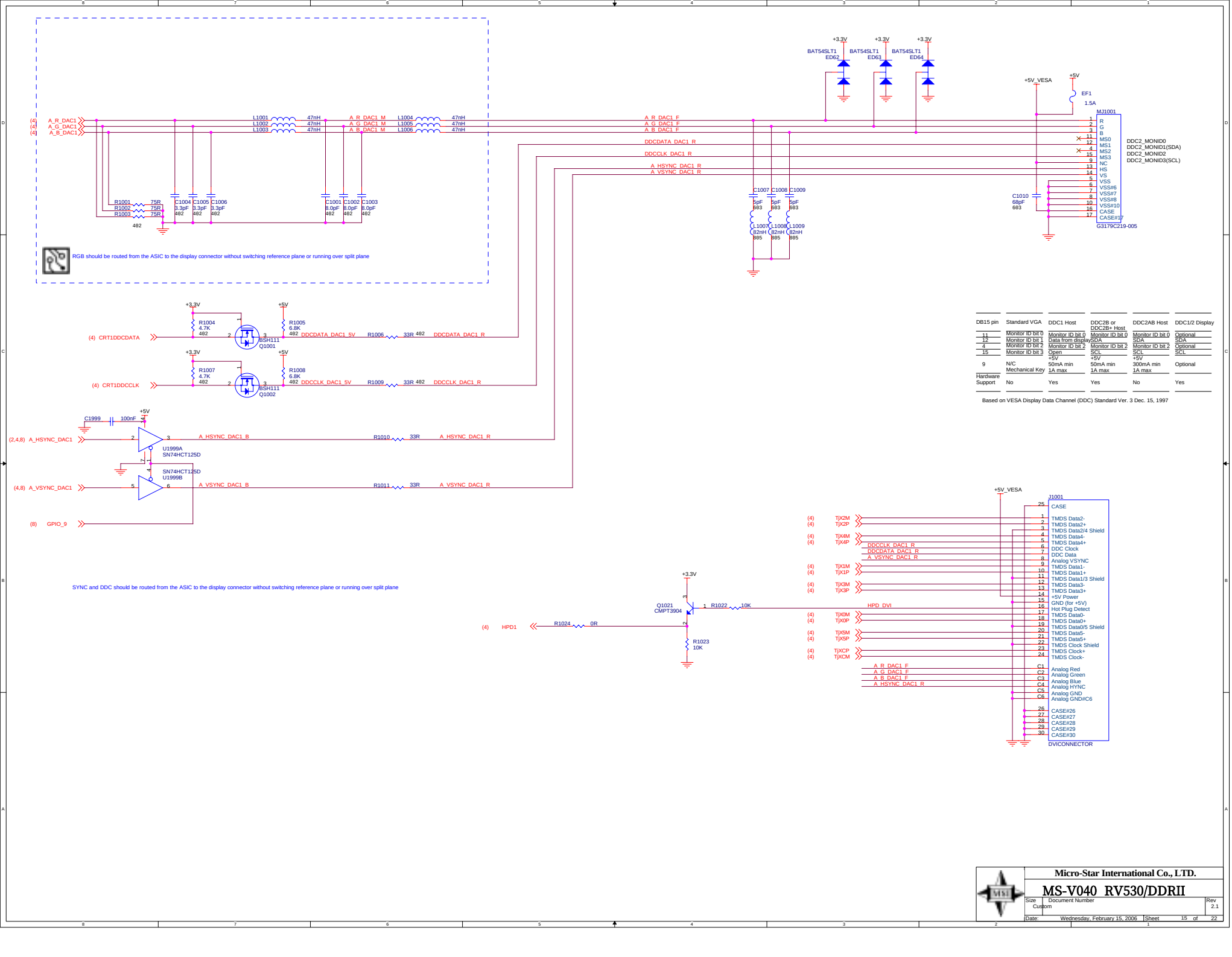

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C Mechanical Key	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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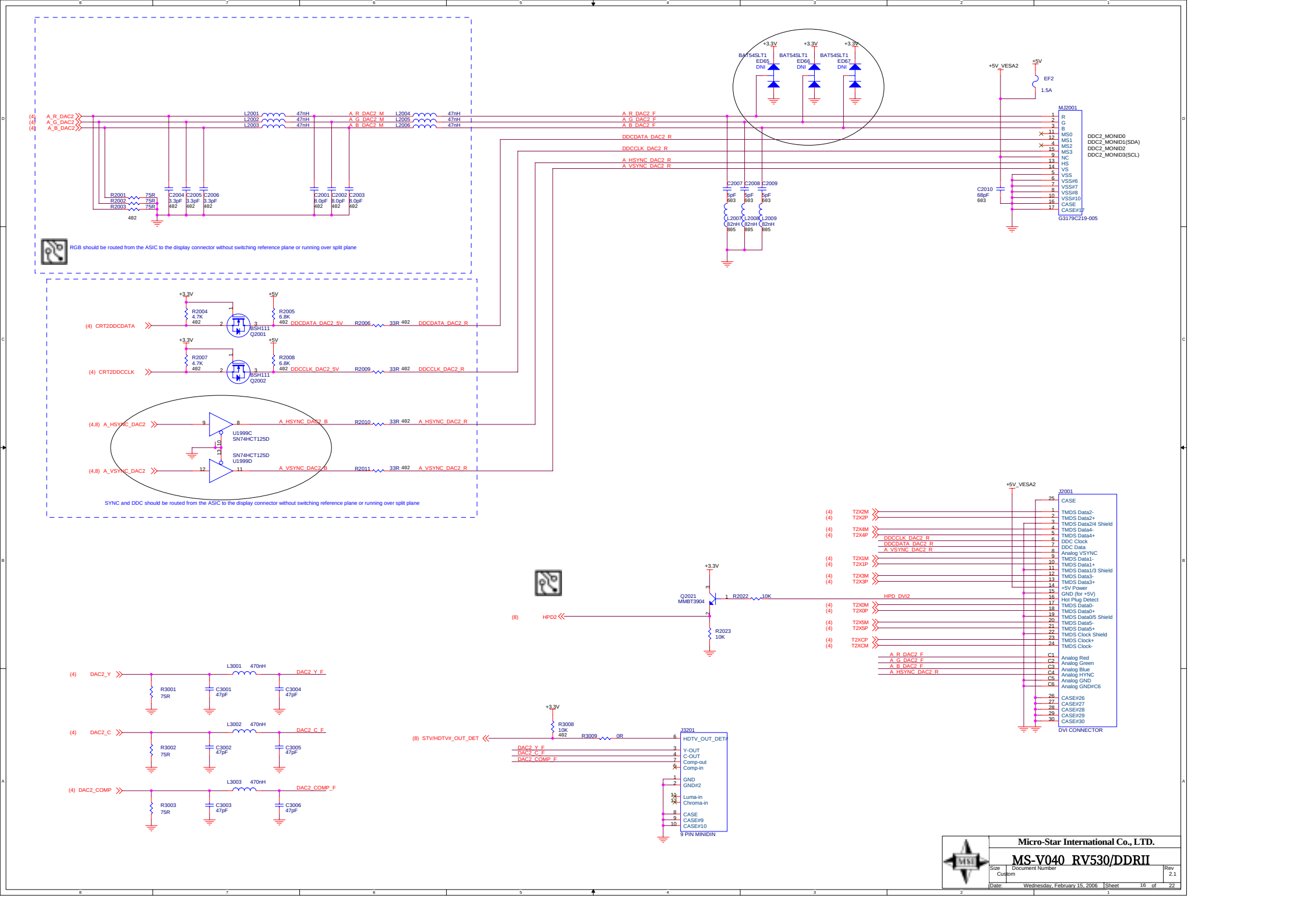
A_R_DAC2
A_G_DAC2
A_B_DAC2
L2001 47nH
L2002 47nH
L2003 47nH
A_R_DAC2_M
A_G_DAC2_M
A_B_DAC2_M
L2004 47nH
L2005 47nH
L2006 47nH
R2001 75R
R2002 75R
R2003 75R
C2004 3.3pF
C2005 3.3pF
C2006 3.3pF
C2001 8.0pF
C2002 8.0pF
C2003 8.0pF
RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane
BAT54SLT1 ED65 DNI
BAT54SLT1 ED66 DNI
BAT54SLT1 ED67 DNI
+3.3V
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R
C2007 5pF
C2008 5pF
C2009 5pF
L2007 82nH
L2008 82nH
L2009 82nH
+5V_VESA2
+5V
EF2
1.5A
C2010 68pF
MJ2001
R
G
B
MS0
MS1
MS2
MS3
NC
HS
VS
VSS
VSS#6
VSS#7
VSS#8
VSS#10
CASE
CASE#17
G3179C219-005
DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)
(4) CRT2DDCDATA
R2004 4.7K
R2005 6.8K
BSH111 Q2001
DDCDATA_DAC2_5V
R2006 33R
DDCDATA_DAC2_R
(4) CRT2DDCCLK
R2007 4.7K
R2008 6.8K
BSH111 Q2002
DDCCLK_DAC2_5V
R2009 33R
DDCCLK_DAC2_R
(4,8) A_HSYNC_DAC2
U1999C SN74HCT125D
A_HSYNC_DAC2_B
R2010 33R
A_HSYNC_DAC2_R
(4,8) A_VSYNC_DAC2
U1999D SN74HCT125D
A_VSYNC_DAC2_B
R2011 33R
A_VSYNC_DAC2_R
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane
(8) HPD2
Q2021 MMBT3904
R2022 10K
R2023 10K
HPD_DVI2
J2001
CASE
T2X2M
T2X2P
T2X4M
T2X4P
T2X1M
T2X1P
T2X3M
T2X3P
T2X0M
T2X0P
T2X5M
T2X5P
T2XCP
T2XCM
TMDS Data2-
TMDS Data2+
TMDS Data2/4 Shield
TMDS Data4-
TMDS Data4+
DDC Clock
DDC Data
Analog VSYNC
TMDS Data1-
TMDS Data1+
TMDS Data1/3 Shield
TMDS Data3-
TMDS Data3+
+5V Power
GND (for +5V)
Hot Plug Detect
TMDS Data0-
TMDS Data0+
TMDS Data0/5 Shield
TMDS Data5-
TMDS Data5+
TMDS Clock Shield
TMDS Clock+
TMDS Clock-
Analog Red
Analog Green
Analog Blue
Analog HYNC
Analog GND
Analog GND#C6
CASE#26
CASE#27
CASE#28
CASE#29
CASE#30
DVI CONNECTOR
DAC2_Y
L3001 470nH
DAC2_Y_F
R3001 75R
C3001 47pF
C3004 47pF
DAC2_C
L3002 470nH
DAC2_C_F
R3002 75R
C3002 47pF
C3005 47pF
DAC2_COMP
L3003 470nH
DAC2_COMP_F
R3003 75R
C3003 47pF
C3006 47pF
(8) STV/HDTV#_OUT_DET
R3008 10K
R3009 0R
J3201
HDTV_OUT_DET#
Y-OUT
C-OUT
Comp-out
Comp-in
GND
GND#2
Luma-in
Chroma-in
CASE
CASE#9
CASE#10
9 PIN MINIDIN
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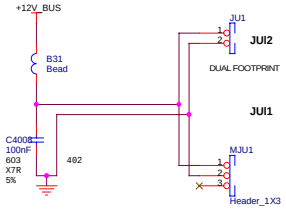

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DVI/VGA SCREWS

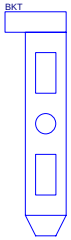
SCREW1
SCREW
JACKSCREW ASSY
7020000800

SCREW2
SCREW
JACKSCREW ASSY
7020000800

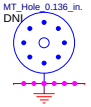
SCREW3
SCREW
JACKSCREW ASSY
7020000800

SCREW4
SCREW
JACKSCREW ASSY
7020000800

BKT



MT1
MT_Hole_0.136_in.
DNI



PCB

H2

LOW PROFILE HS

FM1
SW_FB

FM5
SW_FB

FM2
SW_FB

FM6
SW_FB

FM3
SW_FB

FM4
SW_FB

+MVDDQ

J1
X_PIN1*2

J3
X_PIN1*2

J2
X_PIN1*2

J4
X_PIN1*2

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