MS-V060 -- G73, 128/256 Mb DDR3-136pin, VGA, DVI-I, SD/HDTV, VIVO

SUMMARY:

1. Base on V045-10 to Modify
2. BGA-136 DDRIII
3. Dual MS-11 for NVVDD and FBVDD

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10216-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
1	000	602-10216-0000-200	NV43 P-0 [65nm] FBVA 128MB DDR3 8MX32
2	001	602-10216-0001-200	NV43 V-Port [65nm] FBVA 128MB DDR3 8MX32
3	002	602-10216-0002-200	NV43 V-Port [65nm] FBVA 128MB DDR3 8MX32
4	003	602-10216-0003-200	NV43 V-Port [65nm] FBVA 128MB DDR3 8MX32
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

X01

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE	TABLE OF CONTENTS & REVISION
DETAIL	AND BOM NOT FINAL
HISTORY	

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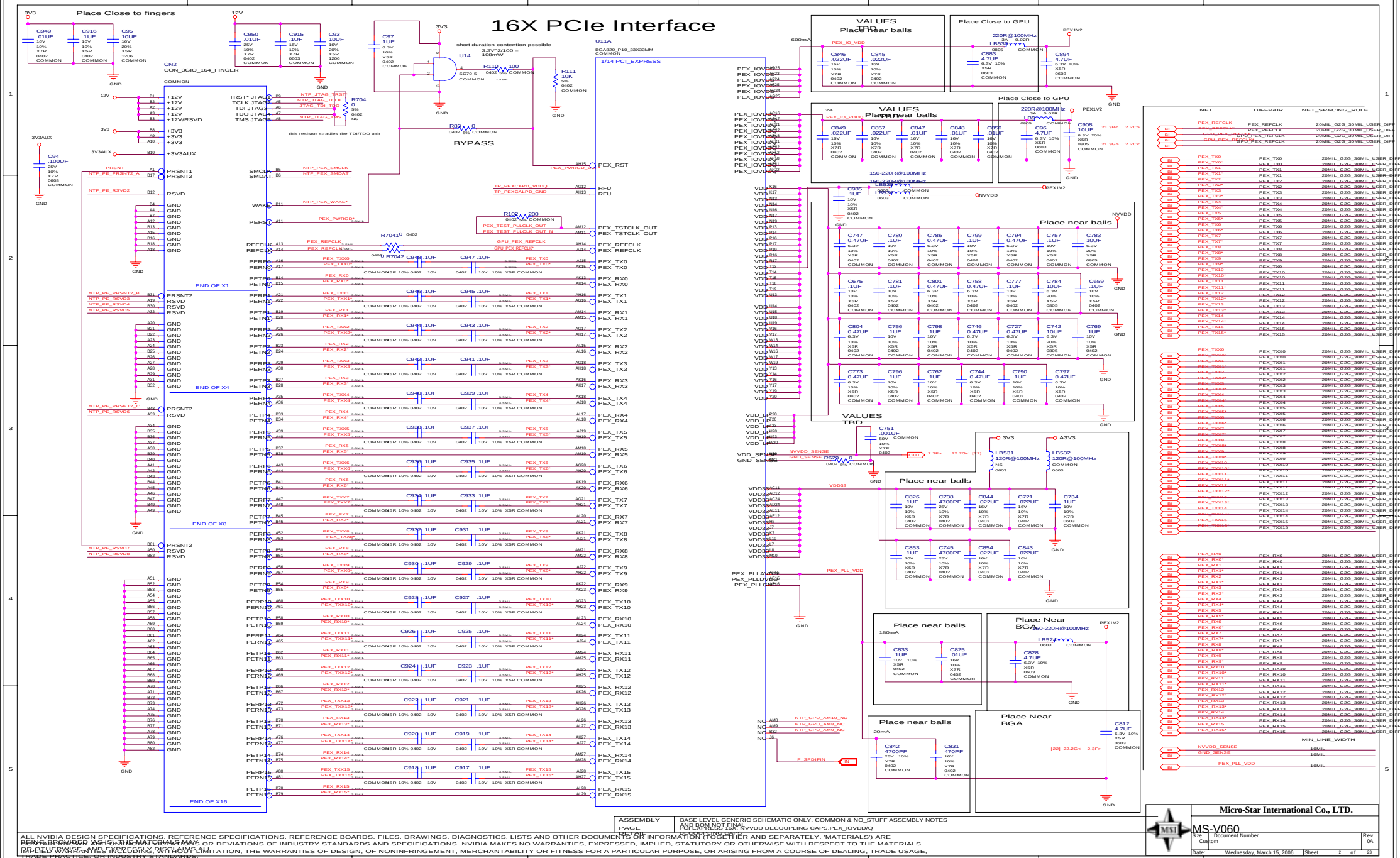

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	PCI EXPRESS 16X, NVVDD DECOUPLING CAPS,PEX_IOVDD/Q
TITLE	DECOUPLING CAPS

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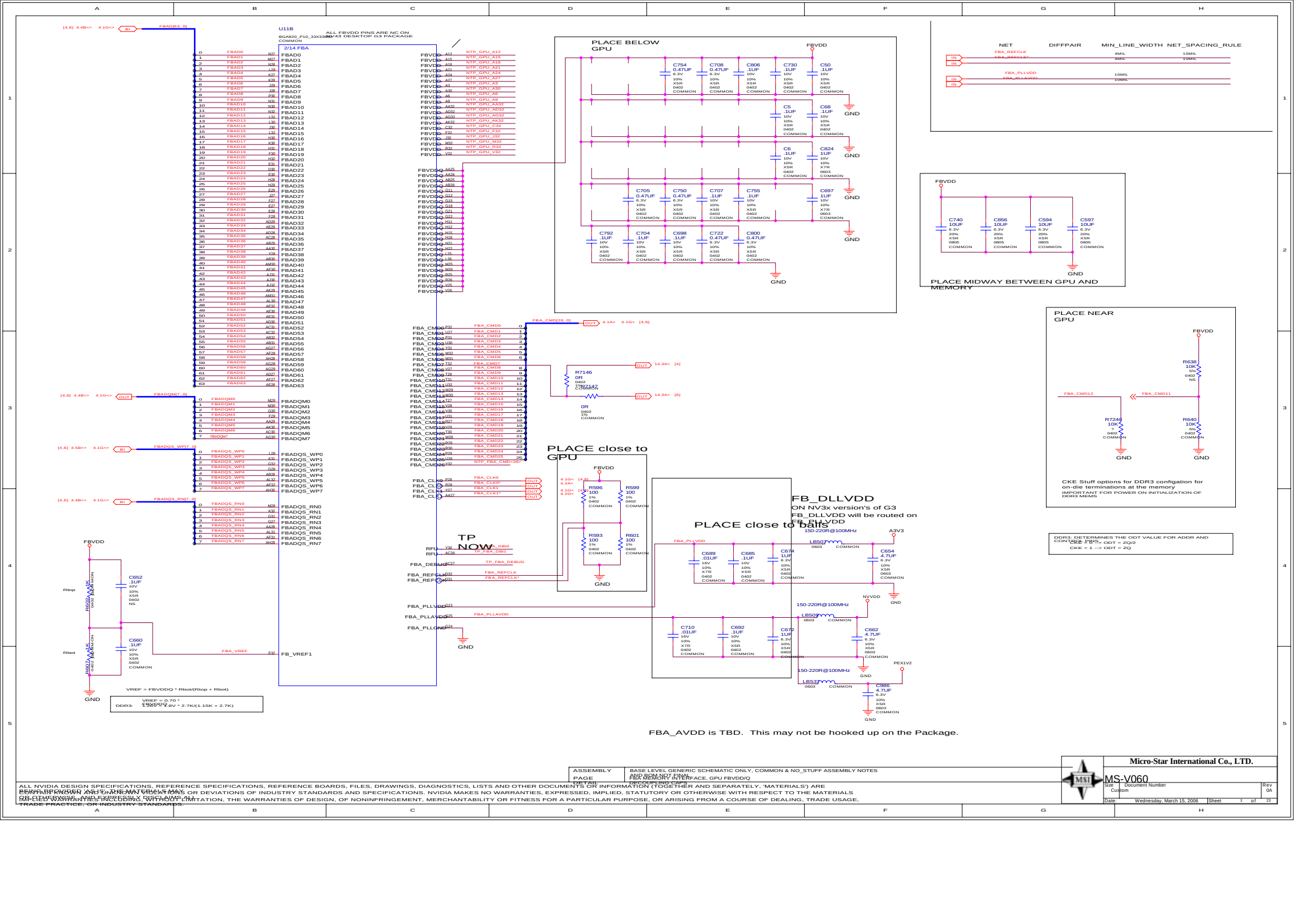

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE	AND BOM NOT FINAL
TITLE	FBA MEMORY INTERFACE, GPU FBVDD/Q
	DECOUPLING CAPS

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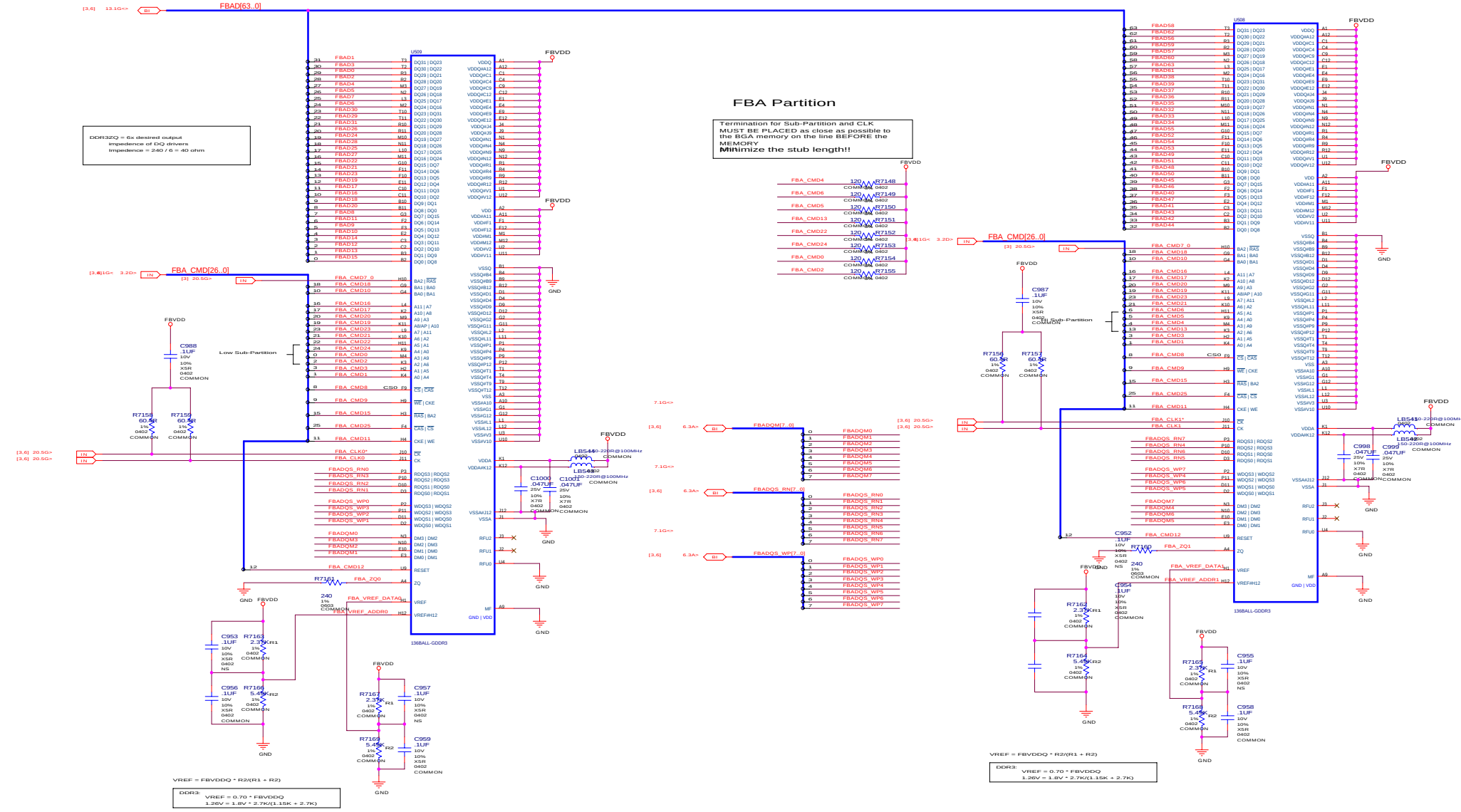
5 FrameBuffer: Partition A
8Mx32 BGA136 DDR3



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE DETAIL	AND BOM NOT FINAL FBA 8MX32 DDR3 MEMORIES, FBA COMMAND BUS PU'S, FBA CLK PU'S

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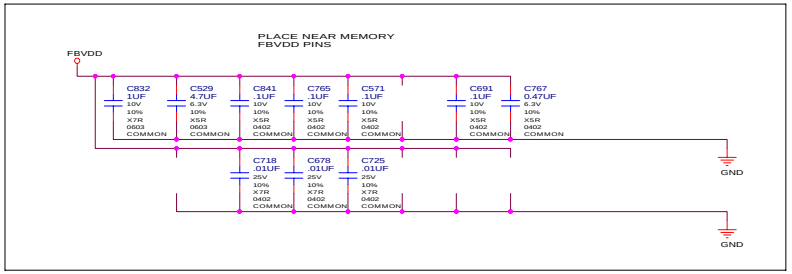
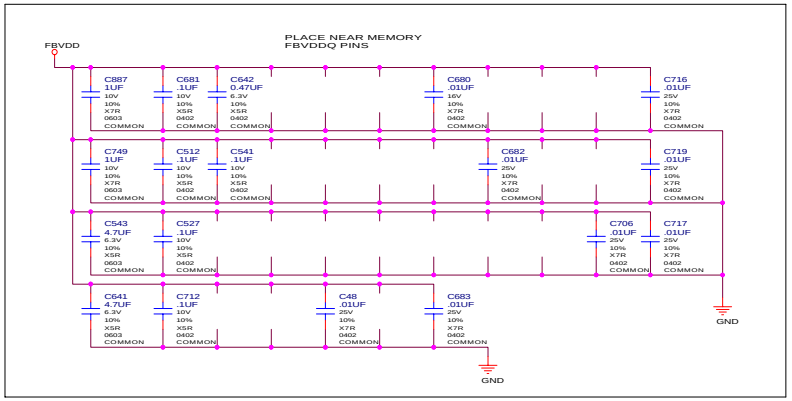
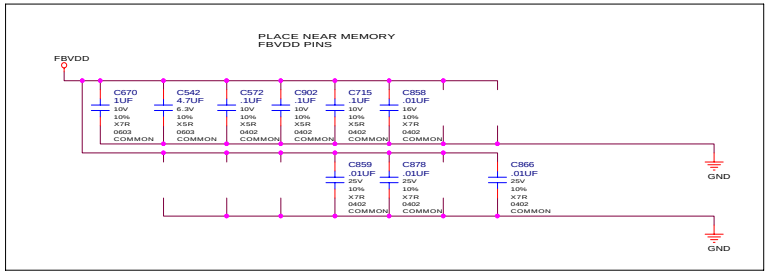
FRAME BUFFER: PARTITION A DECOUPLING

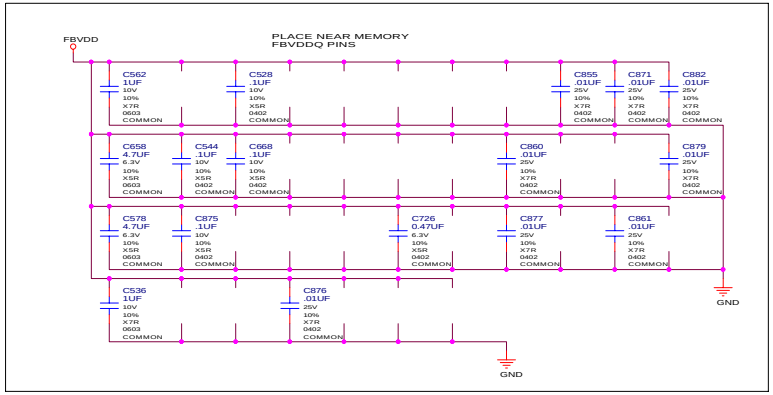
Decoupling for FBA 0..31





Decoupling for FBA 32..63





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE	AND BOM NOT FINAL
TITLE	FBA MEMORY FBVDD/Q DECOUPLING CAPS

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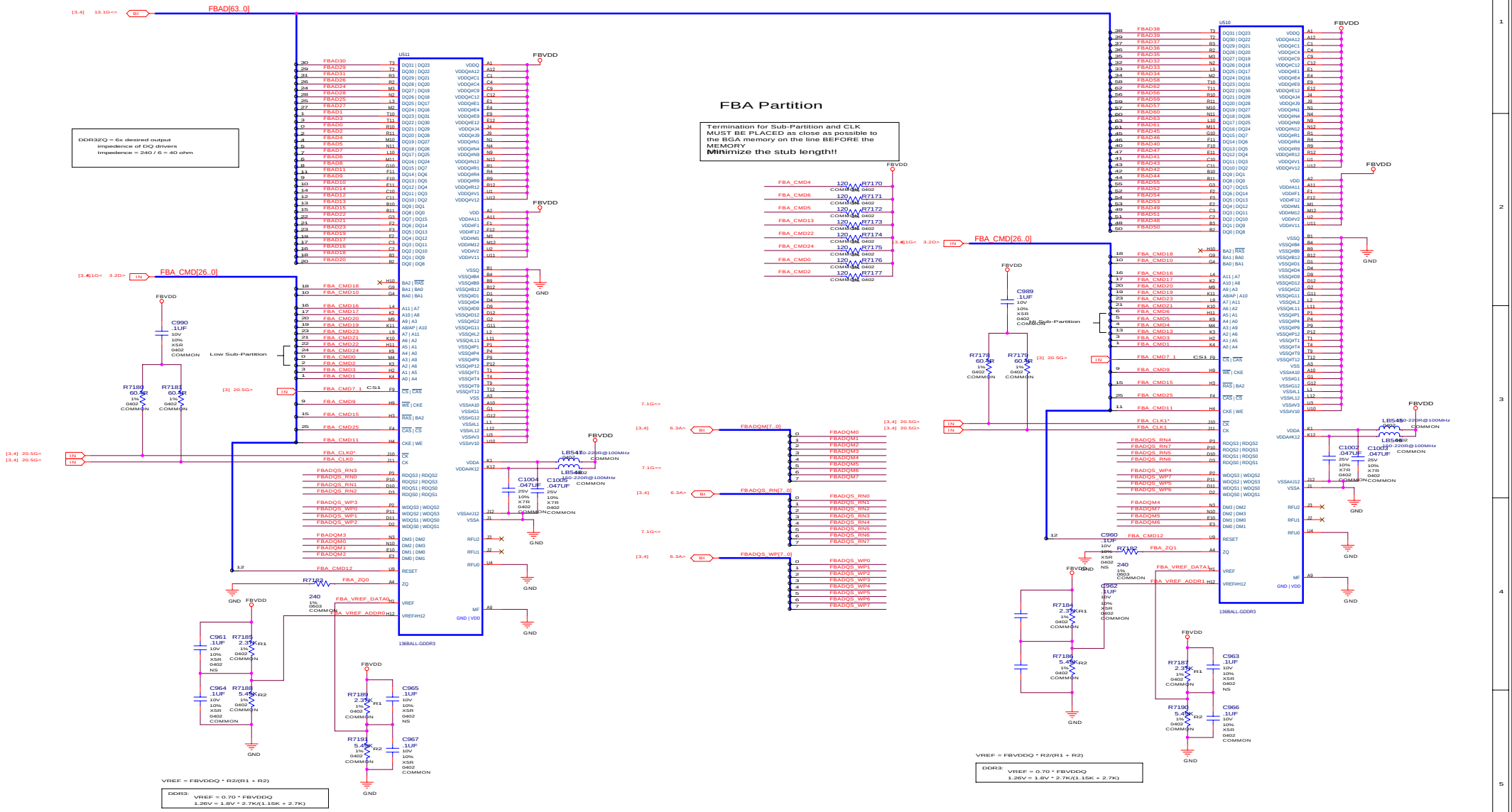
5 FrameBuffer: Partition A
8Mx32 BGA136 DDR3



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DESC.	FBA 8Mx32 DDR3 MEMORIES, FBA COMMAND BUS PU'S, FBA

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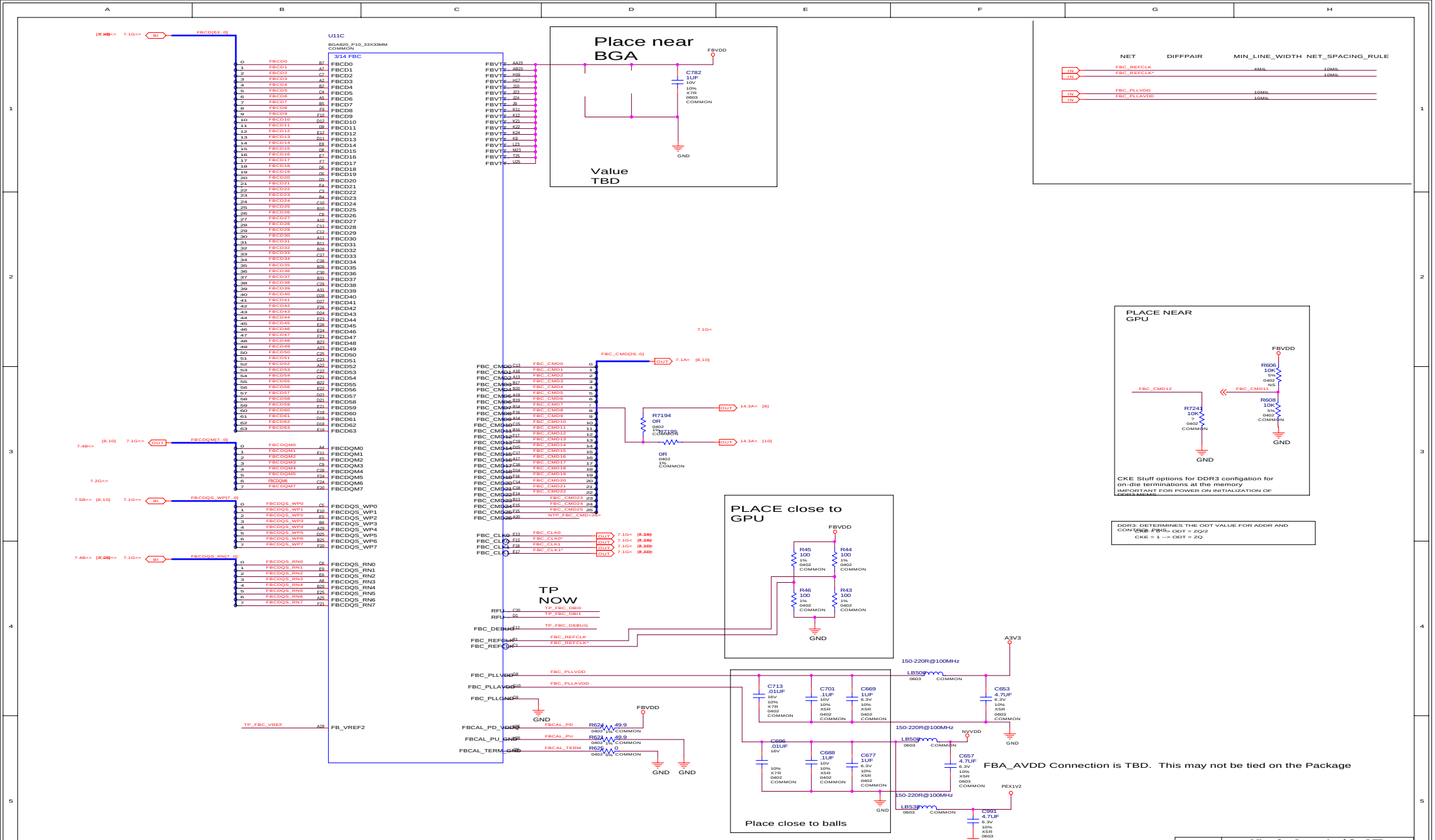

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	FBC MEMORY INTERFACE,
DETAIL	GPU FBVDD

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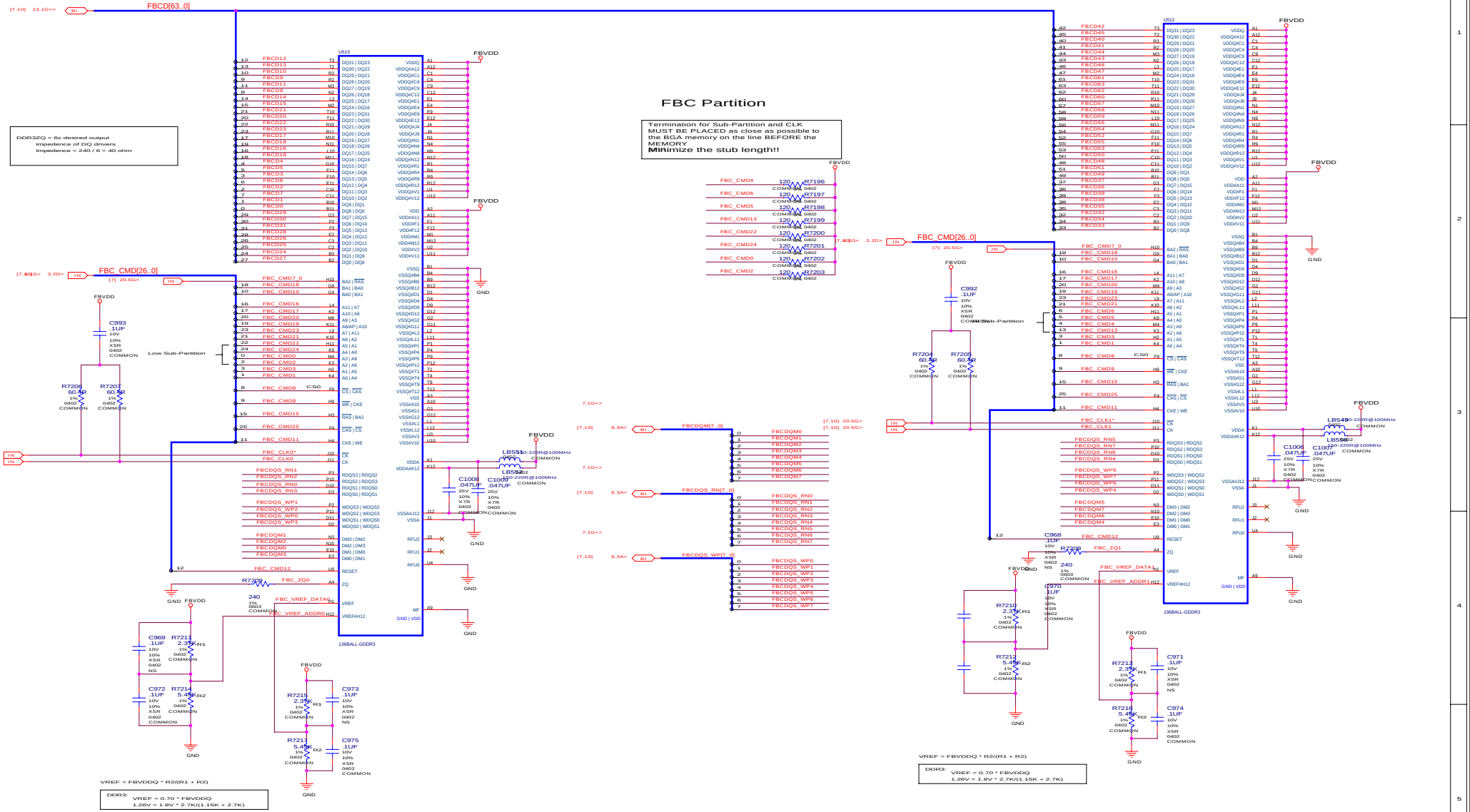
FRAMEBUFFER: PARTITION
C 8Mx32 BGA136 DDR3



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	FBC 8MX32 DDR3 MEMORIES, FBC CMD BUS PU'S, FBC
PAGE	CONTENTS

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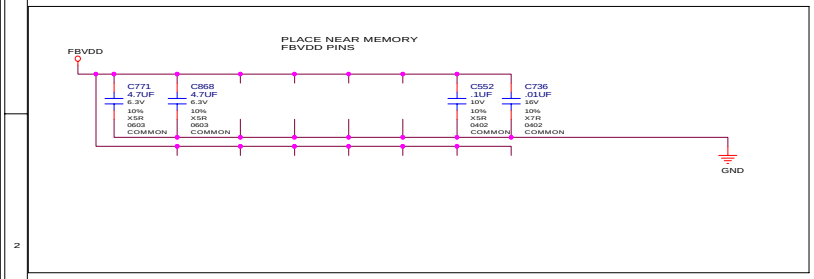
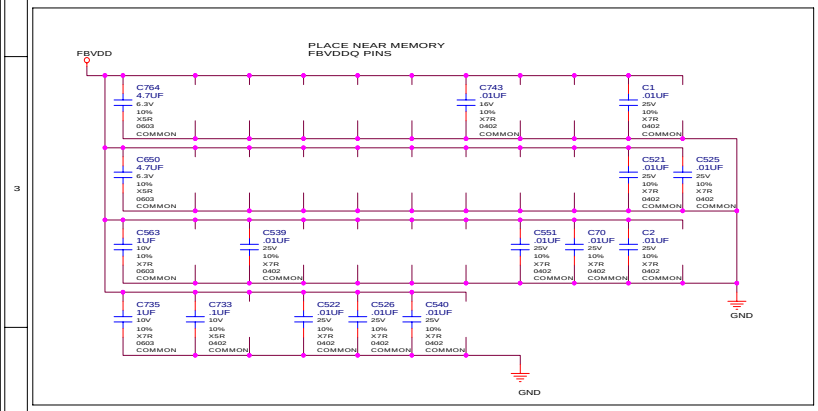
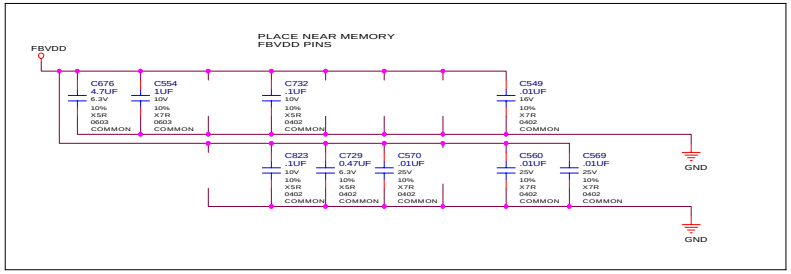
FRAMEBUFFER: PARTITION C DECOUPLING

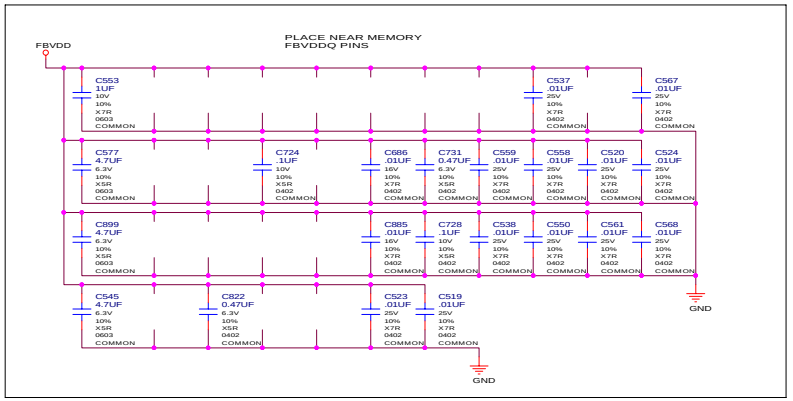
Decoupling for FBC 0..31

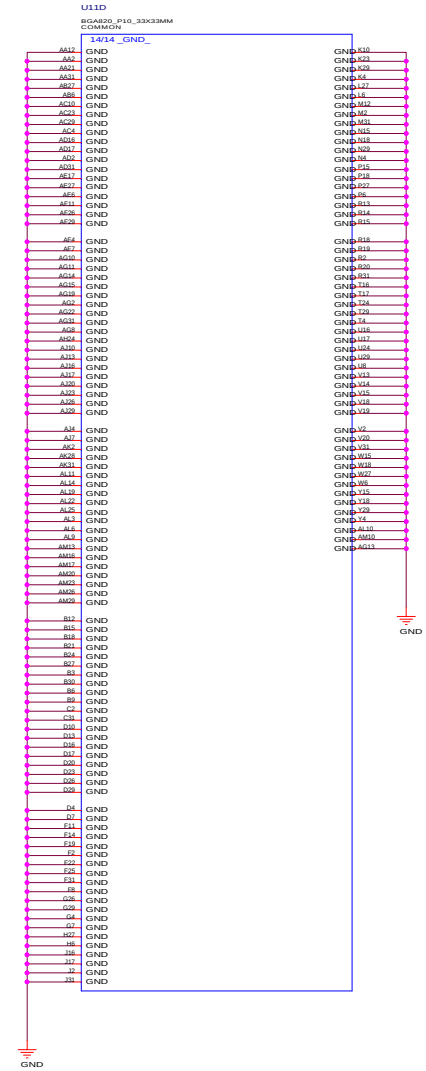




Decoupling for FBC 32..63







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE	AND BOM NOT FINAL FBC MEMORY FBVDD/Q DECOUPLING CAPS, GPU GND
PAGE TITLE	CONNECTIONS

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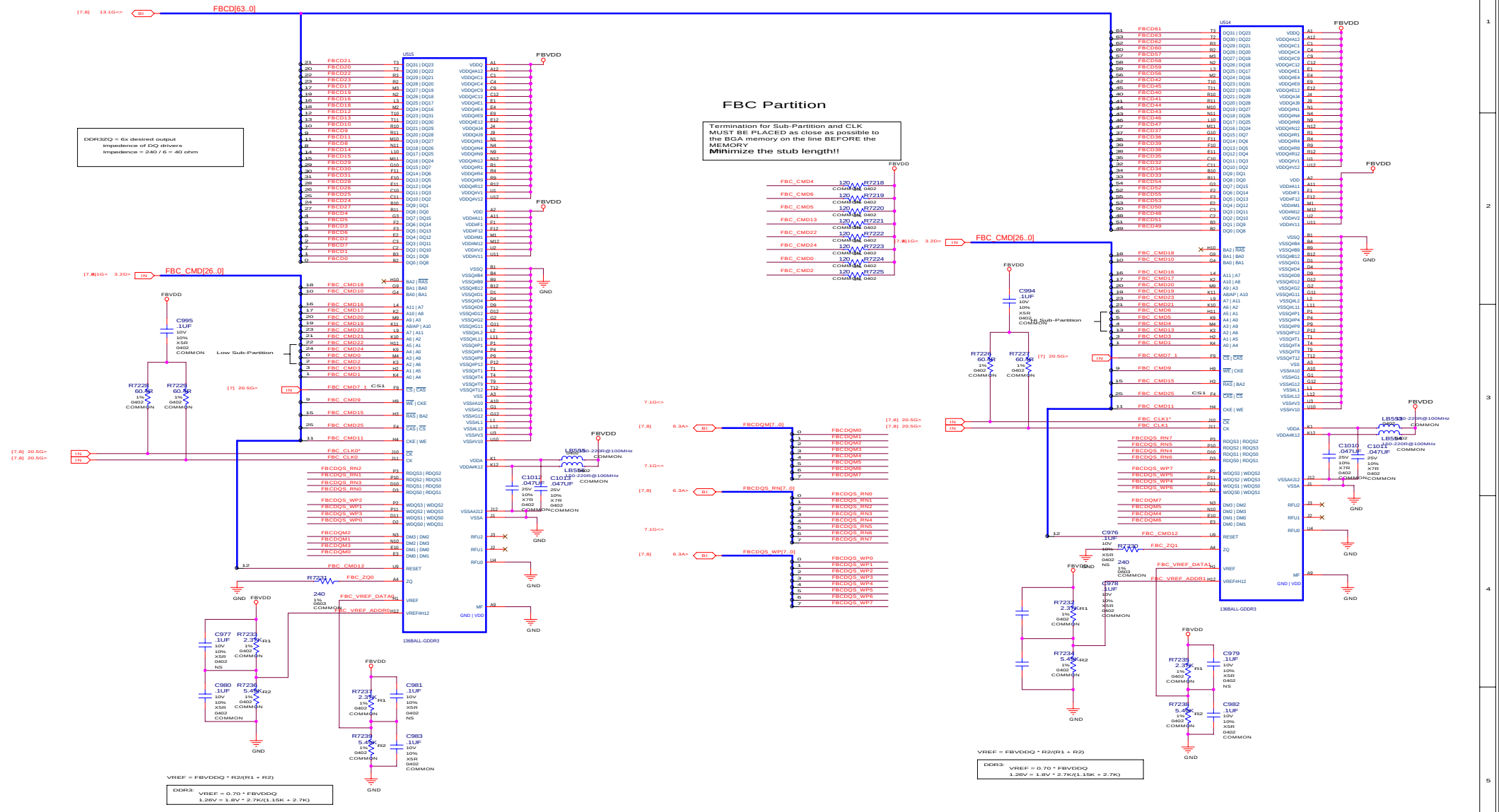
FRAMEBUFFER: PARTITION
C 8Mx32 BGA136 DDR3



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	FBC 8MX32 DDR3 MEMORIES, FBC CMD BUS PU'S, FBC
DETAIL	CLK PU'S

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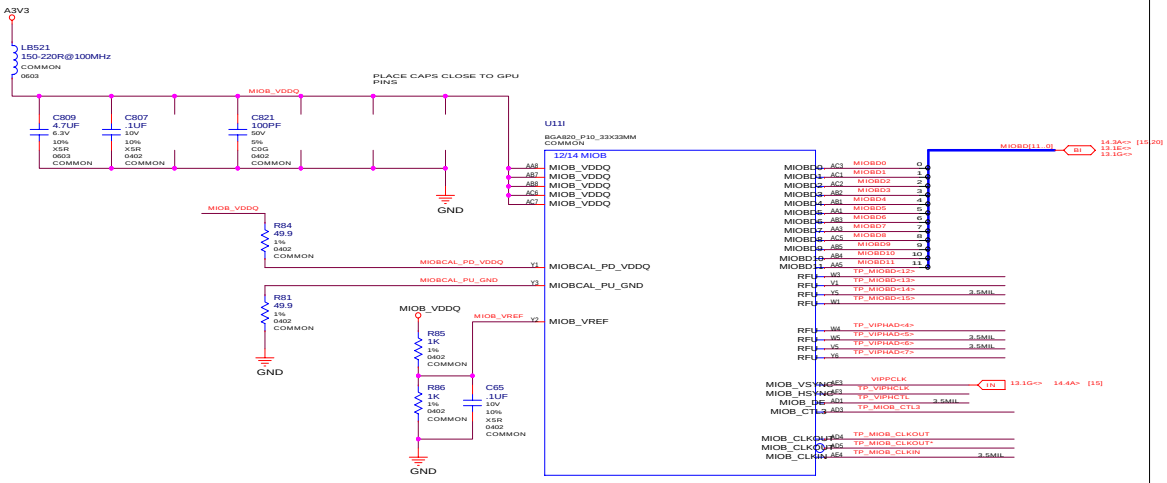
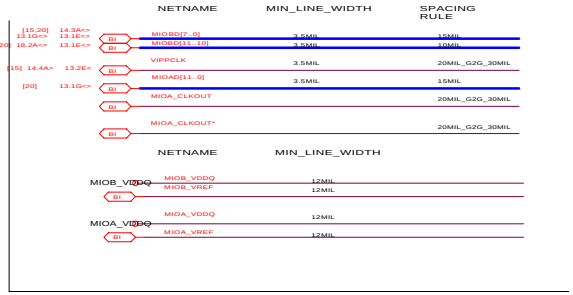
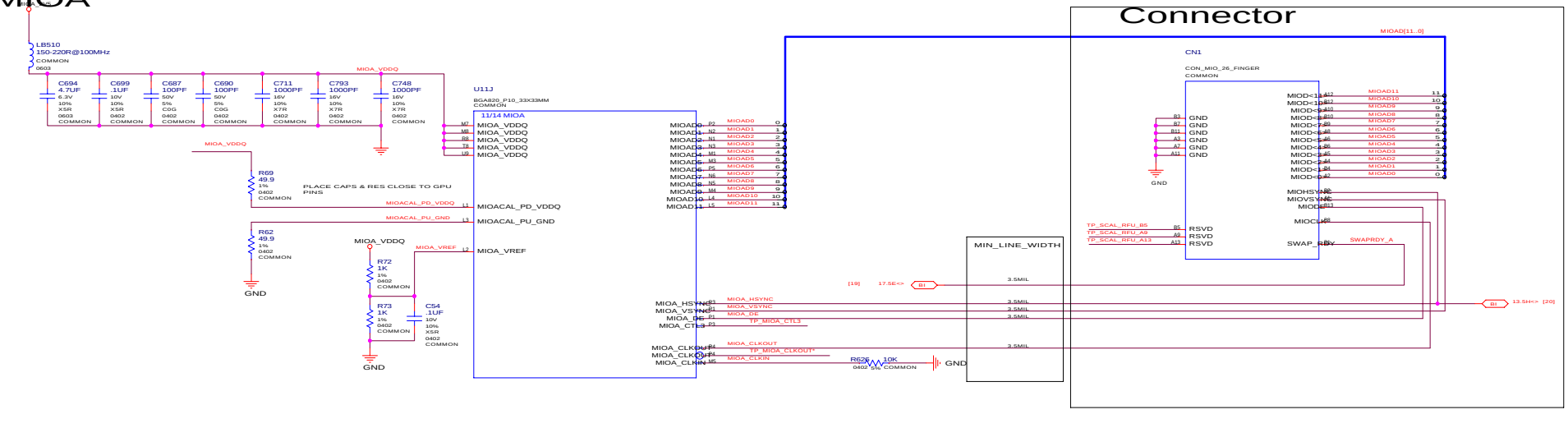
G3 VIP/MIOB





G3 MIOA



Feature Connector

ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE: AND BOM NOT FINAL
DETAIL: MIOA & MIOB_FEATURE CONNECTOR

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Secondary Display (DACC), Slim DB15

DACC RGB-FILTER

NET_NAME	NET_SPACING_RULE	IMPEDANCE	MIN_LINE_WIDTH
DACC_VDD			12MIL
DACC_VREF			12MIL
DACC_RSET			12MIL
DACC_RED	20MIL	U11.AF6:R59.1:37.50 ohm:2 %	
DACC_GREEN	20MIL	U11.AG6:R70.1:37.50 ohm:2 %	
DACC_BLUE	20MIL	U11.AE5:R50.1:37.50 ohm:2 %	
DACBC_R_F	20MIL	L10.2:L9.1:75.00 ohm:2 %	
DACBC_G_F	20MIL	L12.2:L11.1:75.00 ohm:2 %	
DACBC_B_F	20MIL	L8.2:L7.1:75.00 ohm:2 %	
DACC_RED_C	20MIL	L9.2:J6.1:75.00 ohm:2 %	
DACC_GREEN_C	20MIL	L11.2:J6.2:75.00 ohm:2 %	
DACC_BLUE_C	20MIL	L7.2:J6.3:75.00 ohm:2 %	

Place 0ohm Resistor Incident with Common Mode Choke

MIDDLE

FOR ESD DIODES

Place in output filter section!

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID

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Primary Display (DACA), Slim DB15

DACA RGB-FILTER

NET_NAME	NET_SPACING_RULE	IMPEDANCE	MIN_LINE_WIDTH
DACA_VDD			12MIL
DACA_VREF			12MIL
DACA_RSET			12MIL
DACA_RED	20MIL	U11.AH11-R101.1-37.50 ohm:2 %	
DACA_GREEN	20MIL	U11.AJ12-R104.1-37.50 ohm:2 %	
DACA_BLUE	20MIL	U11.AH12-R98.1-37.50 ohm:2 %	
DACA_R_F	20MIL	L15.2-L16.1-75.00 ohm:2 %	
DACA_G_F	20MIL	L17.2-L18.1-75.00 ohm:2 %	
DACA_B_F	20MIL	L13.2-L14.1-75.00 ohm:2 %	
DACA_RED_C	20MIL	L16.2-J8.1-75.00 ohm:2 %	
DACA_GREEN_C	20MIL	L18.2-J8.2-75.00 ohm:2 %	
DACA_BLUE_C	20MIL	L14.2-J8.3-75.00 ohm:2 %	
DDC_5V			12MIL

Route DAC RGB with ~37.5ohm impedence

NO STUFF 2.2K ON RGB FOR BRINGUP

PLACE NEAR SYNC BUFFER

SOUTH

FOR ESD DIODES

Place in output filter section!

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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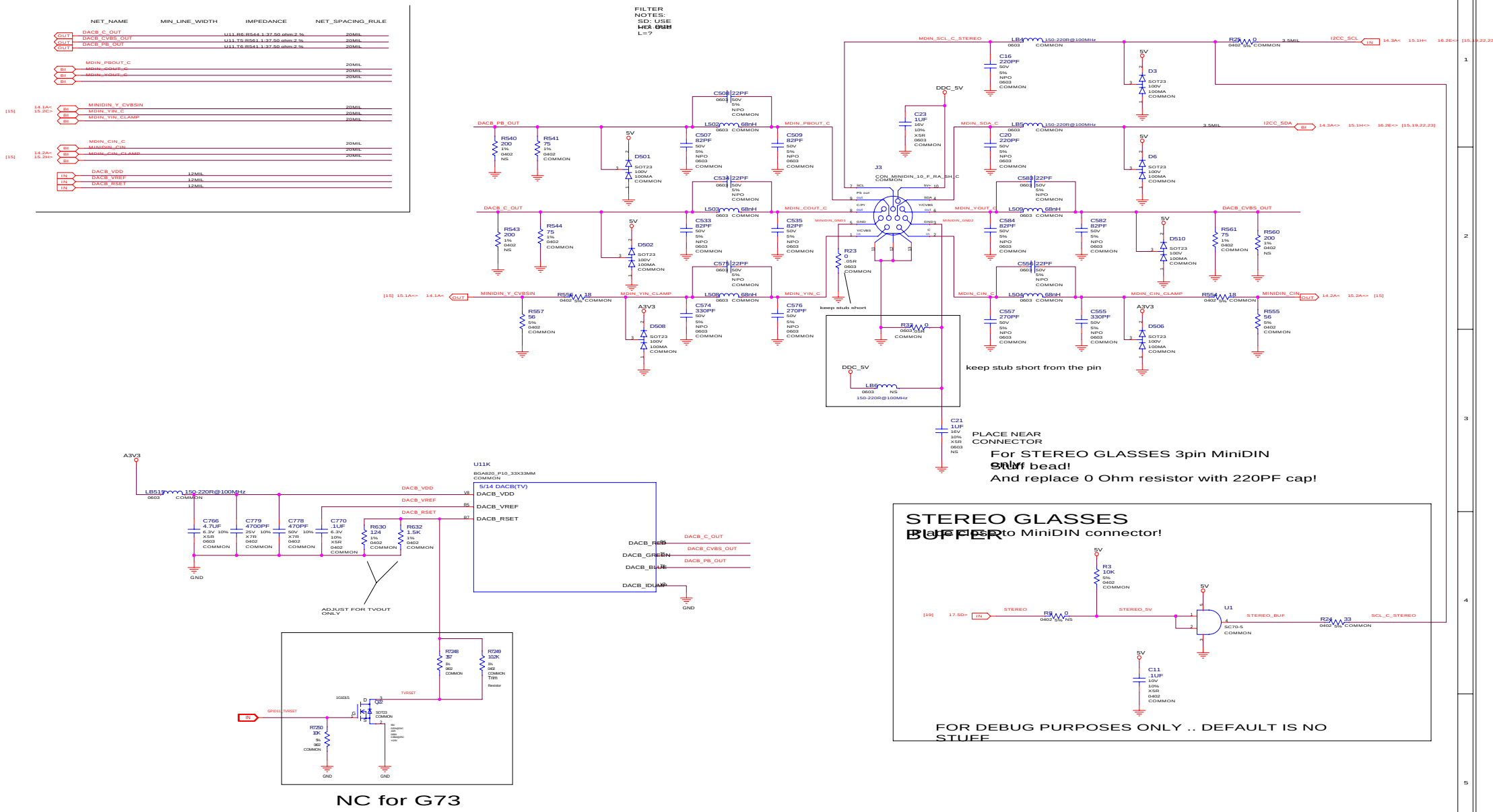
DACB .. MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE	AND ROM NOT FINAL
DETAIL	DACB FILTERS, MINIDIN CONNECTOR NORTH

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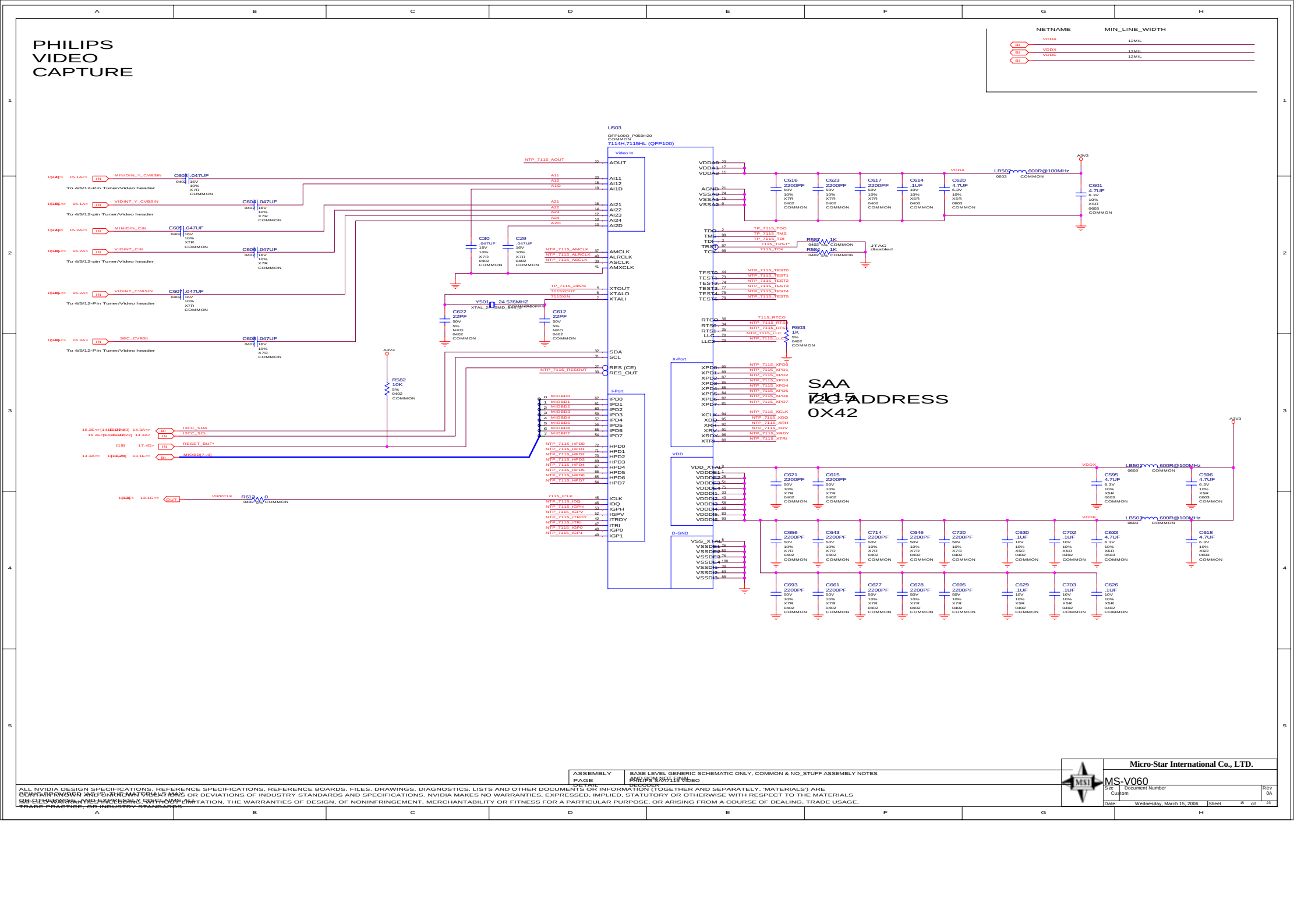
PHILIPS VIDEO CAPTURE



ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL: PHILIPS SAA7115 VIDEO DECODER

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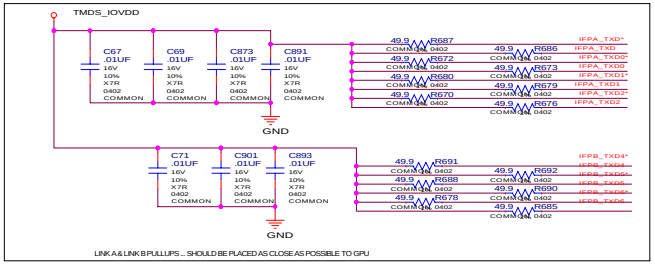
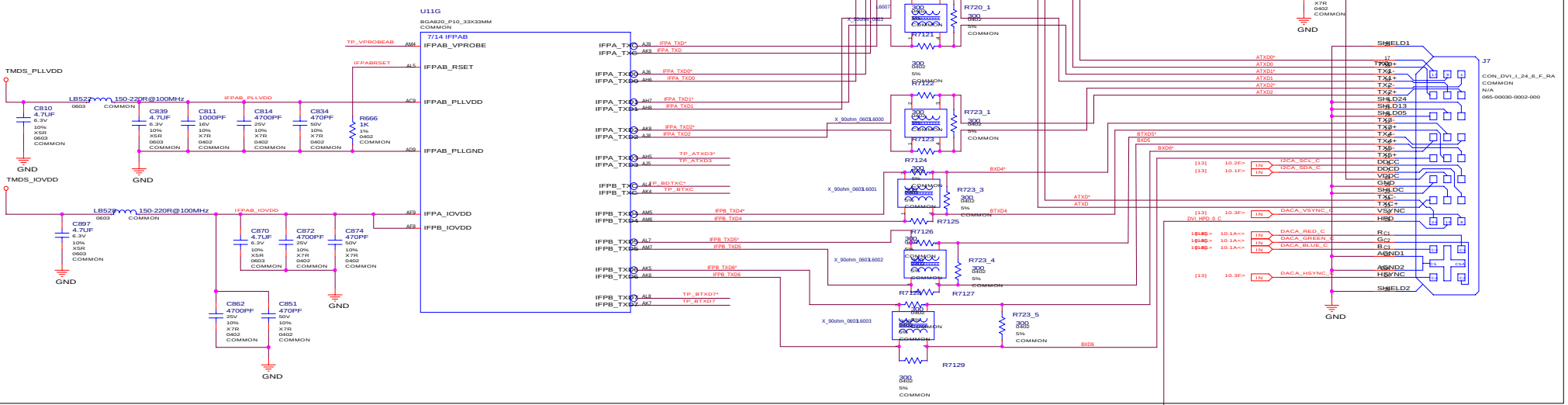
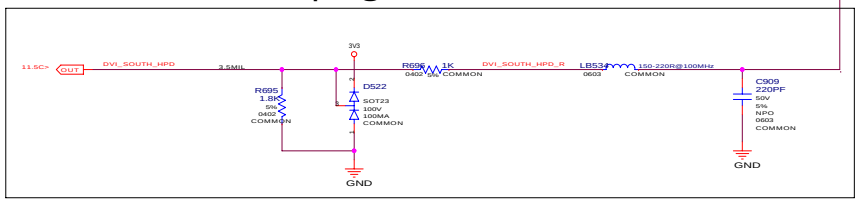
INTERNAL TMDS .. LINK A & B



NOTE: GPU HAS ON DIE PULL UPS ON TMDS LINES .. EXTERNAL PULLUPS ADDED (FOR CYA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE



Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
TMDS_PLLVDD	12MIL	3.3V
IFPAB_PLLVDD	12MIL	3.3V
TMDS_IOVDD	12MIL	3.3V
IFPAB_IOVDD	12MIL	3.3V
IFPABRSET	12MIL	
TMDS_IOBACK	12MIL	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE DETAIL	AND BOM NOTES FINAL TMDS LINK A/B & PU's, TMDS IO BACKDRIVE PREVENTION,DVI CONNECTOR SOUTH

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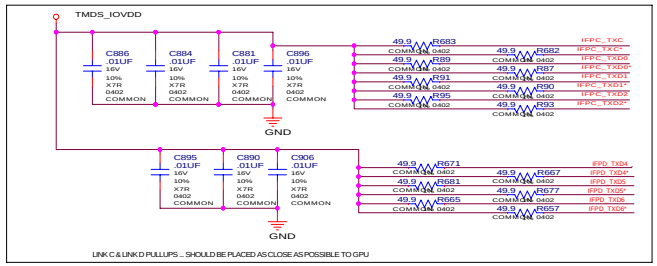
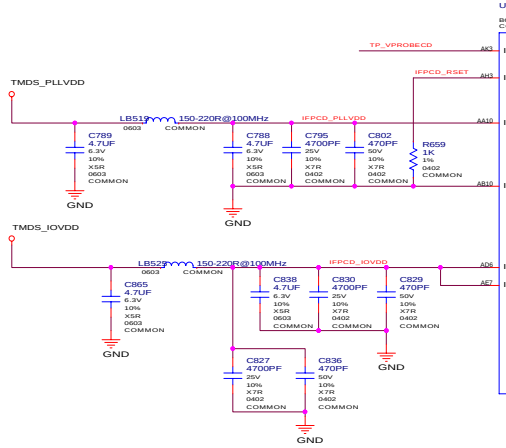
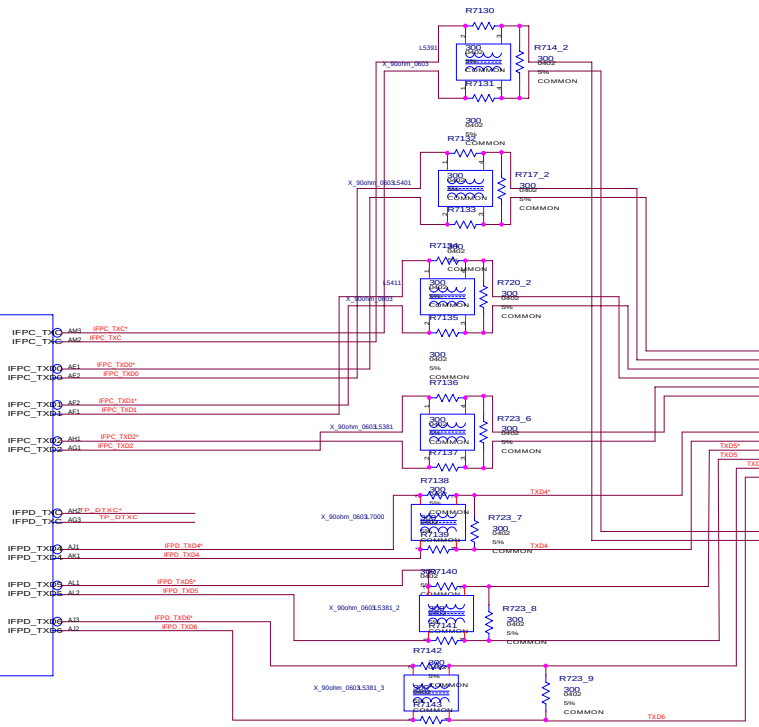
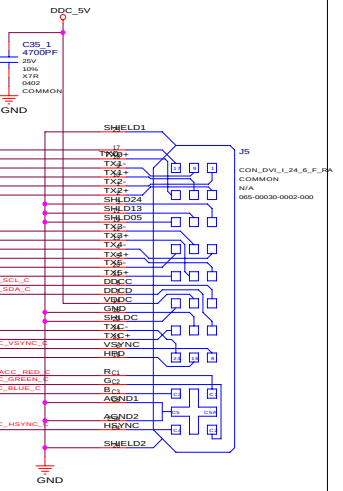
INTERNAL TMDS
.. LINK C & D

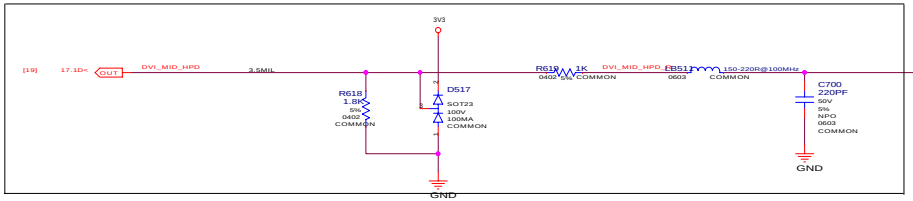








Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
IFPCD_RSET	12MIL	
IFPCD_PLLVDD	12MIL	3.3V
IFPCD_IOVDD	12MIL	3.3V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK C/D & POS,DVI CONNECTOR
MID	

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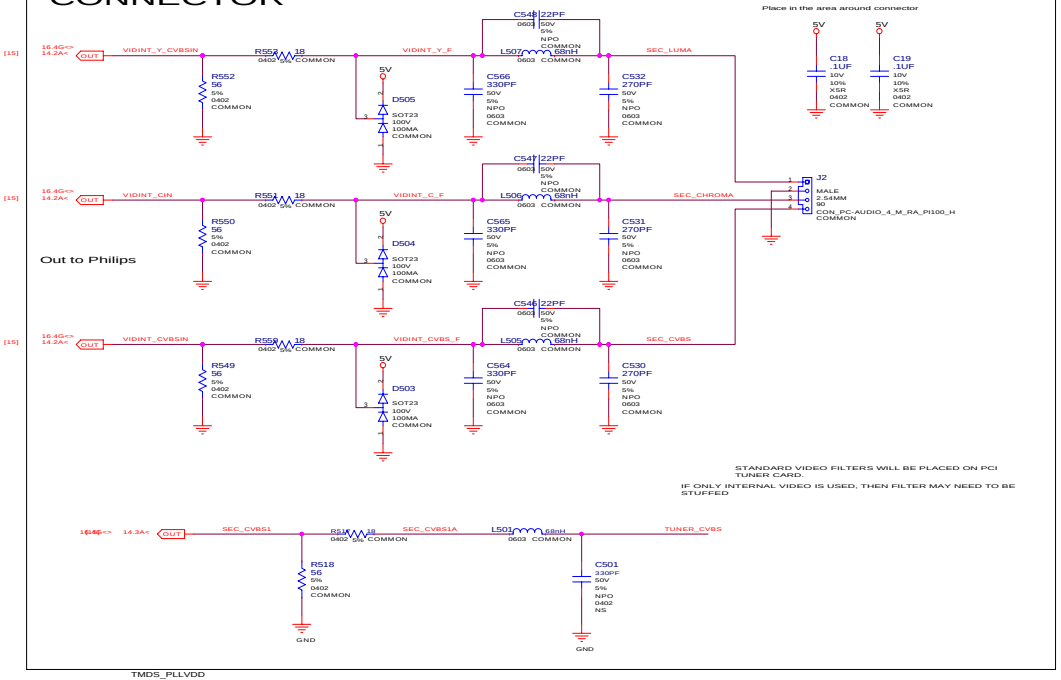
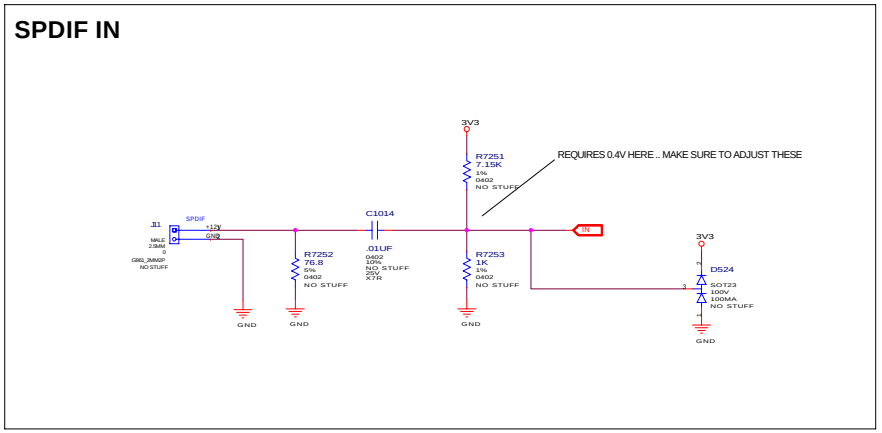
4-Pin Video In, 12-pin Video In connectors

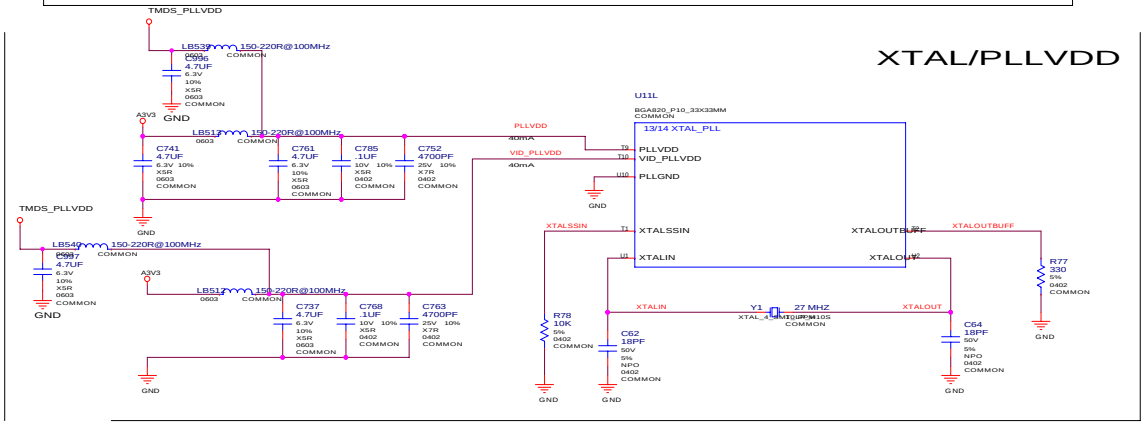
EXTERNAL 4-PIN VIDEO IN CONNECTOR

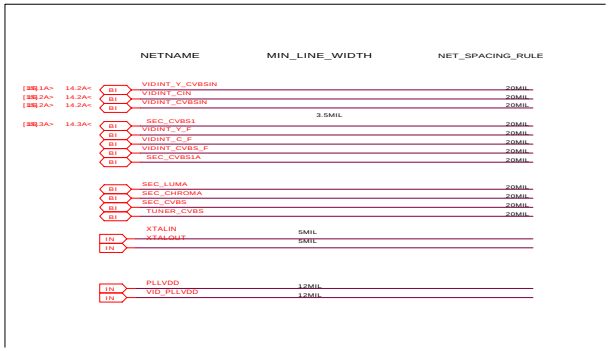


SPDIF IN



XTAL/PLLVDD





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE DETAIL	4-PIN & 12-PIN VIDEO HEADERS, XTAL

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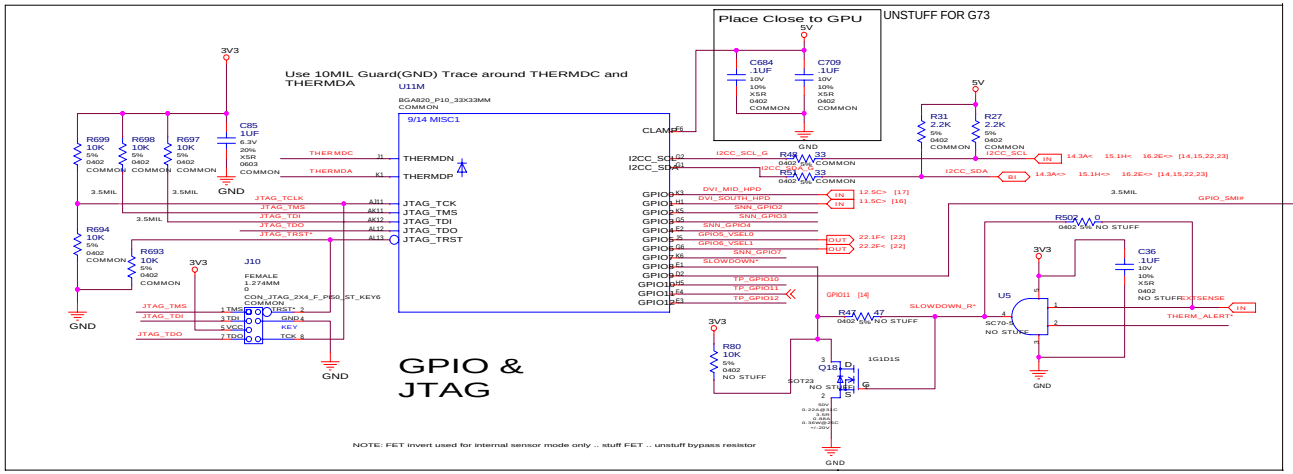
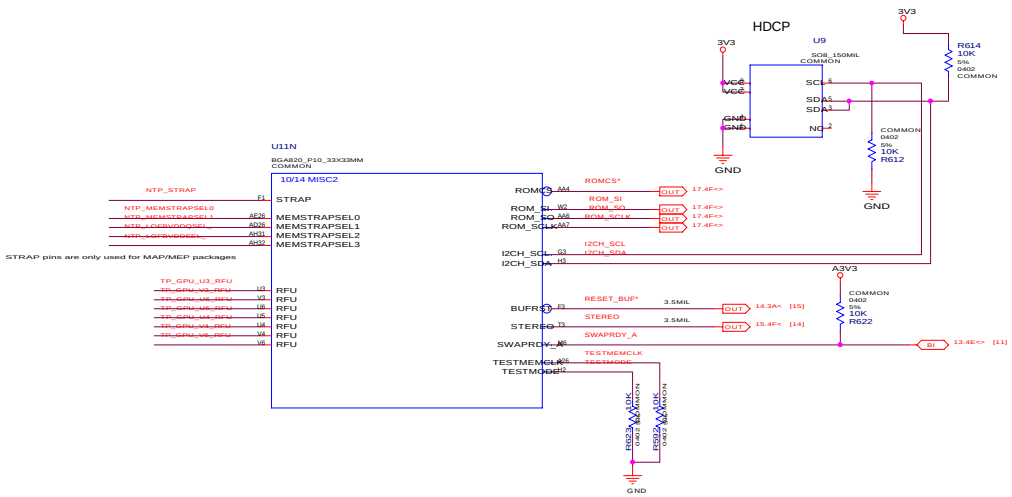
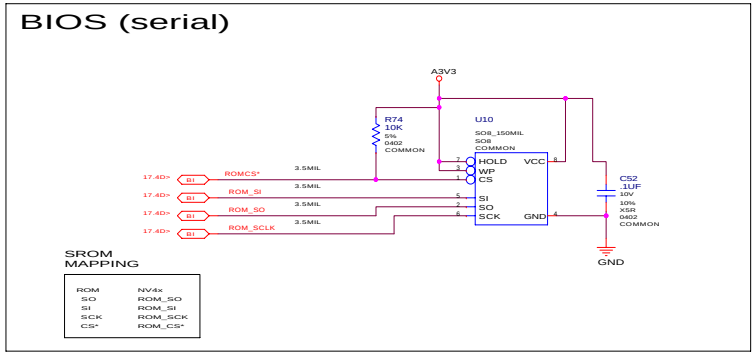


GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	DVI SOUTH HOTPLUG DET
2	IN	RESERVED
3	IN	RESERVED
4	IN	TUNER IRQ
5	OUT	NVVDD VOLTAGE SELECT 0
6	OUT	NVVDD VOLTAGE SELECT 1
7	IN	RESERVED
8	IN	RESERVED
9	OUT	PWM FAN
10	IN	RESERVED
11	IN	TVRSET
12	IN	RESERVED





NETNAME	MIN_LINE_WIDTH	VOLTAGE
THERMDC	10MIL	
THERMDA	10MIL	
FAN_PWM_B	12MIL	
FAN_PWM_C	12MIL	
FAN_PWM_D	12MIL	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE	AND BOM NOT FINAL
DETAIL	JTAG, BIOS ROM, HDCP ROM, FAN CONTROL, TEMP SENSOR & GPIO's

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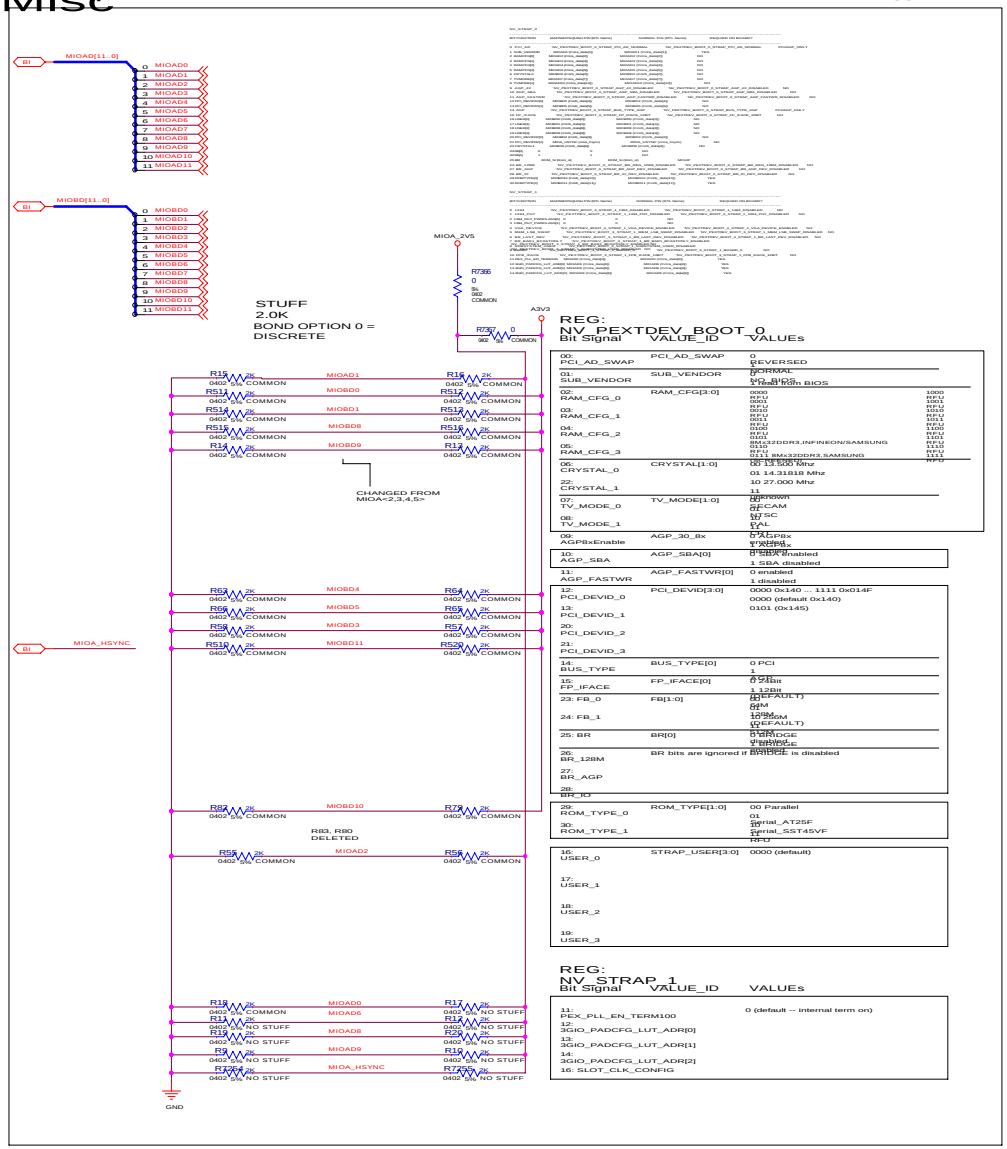
BIOS, Straps, Misc

Straps

Assembly: BIOS



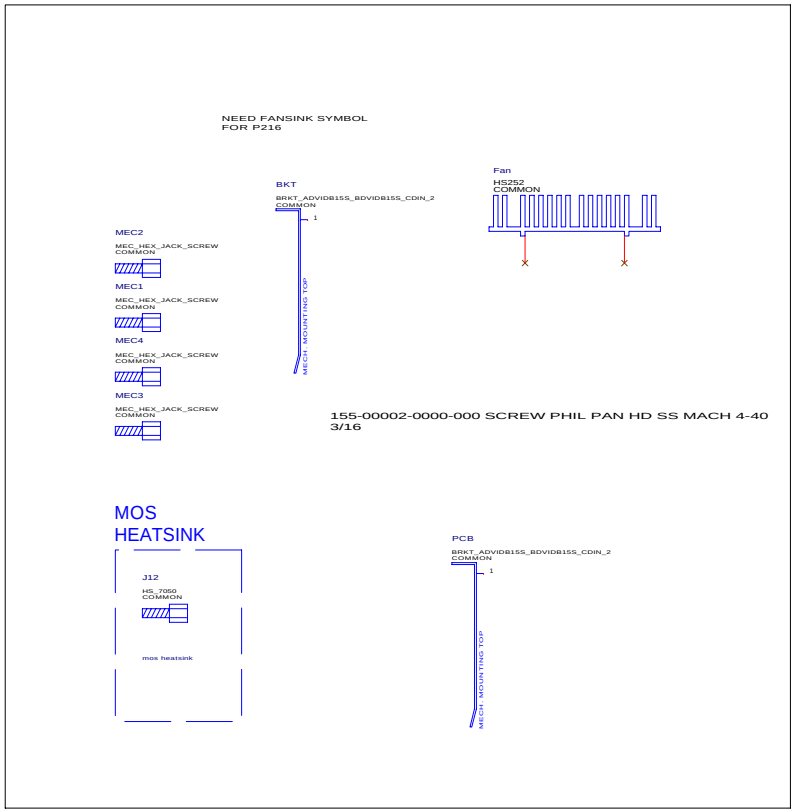
REG: NV_PEXTDEV_BOOT_0

Bit Signal	VALUE_ID	VALUES
00: PCI_AD_SWAP	PCI_AD_SWAP	0 NORMAL 1 REVERSED
01: SUB_VENDOR	SUB_VENDOR	0 NORMAL 1 Nvidia's BIOS
02: RAM_CFG_0	RAM_CFG[3:0]	0000 RFU 0001 RFU 0010 RFU 0011 RFU 0100 RFU 0101 RFU 0110 RFU 0111 8Mx32DDR3,INFINEON/SAMSUNG 1000 RFU 1001 RFU 1010 RFU 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 RFU
03: RAM_CFG_1		
04: RAM_CFG_2		
05: RAM_CFG_3		
06: CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz 01 14.31818 Mhz 10 27.000 Mhz 11
22: CRYSTAL_1		
07: TV_MODE_0	TV_MODE[1:0]	00 NTSC 01 PAL 10 SECAM 11 NTSC
08: TV_MODE_1		
09: AGP8xEnable	AGP_30_8x	0 AGP8x enabled 1 AGP8x disabled
10: AGP_SBA	AGP_SBA[0]	0 SBA enabled 1 SBA disabled
11: AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled
12: PCI_DEVID_0	PCI_DEVID[3:0]	0000 0x140 .. 1111 0x014F 0000 (default 0x140) 0101 (0x145)
13: PCI_DEVID_1		
20: PCI_DEVID_2		
21: PCI_DEVID_3		
14: BUS_TYPE	BUS_TYPE[0]	0 PCI 1 AGP
15: FP_IFACE	FP_IFACE[0]	0 24bit 1 12Bit
23: FB_0	FB[1:0]	00 (DEFAULT) 01 64M 10 128M 11 256M (DEFAULT)
24: FB_1		
25: BR	BR[0]	0 BR BRIDGE disabled 1 BR BRIDGE enabled (DEFAULT)
26: BR_128M	BR bits are ignored if BRIDGE is disabled	
27: BR_AGP		
28: BR_IO		
29: ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Spiral_AT25F 10 Spiral_SST45VF 11 RFU
30: ROM_TYPE_1		
16: USER_0	STRAP_USER[3:0]	0000 (default)
17: USER_1		
18: USER_2		
19: USER_3		

REG: NV_STRAP_1

Bit Signal	VALUE_ID	VALUES
11: PEX_PLL_EN_TERM100		0 (default -- internal term on)
12: 3GIO_PADCFG_LUT_ADR[0]		
13: 3GIO_PADCFG_LUT_ADR[1]		
14: 3GIO_PADCFG_LUT_ADR[2]		
16: SLOT_CLK_CONFIG		

Mechanical parts



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE DETAIL	BIOS STRAPS & MECHANICALS

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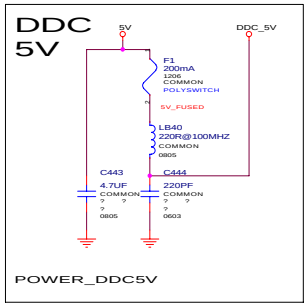
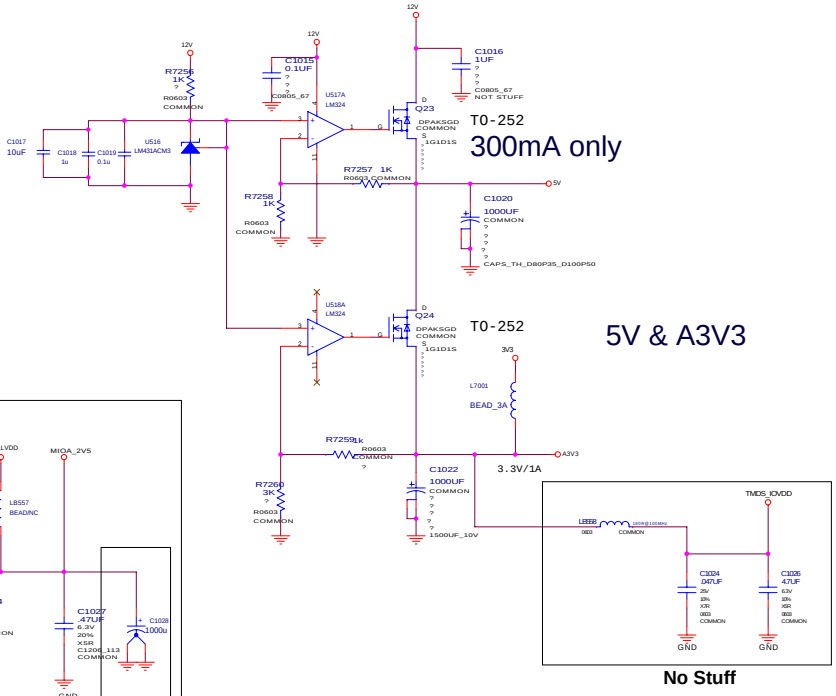
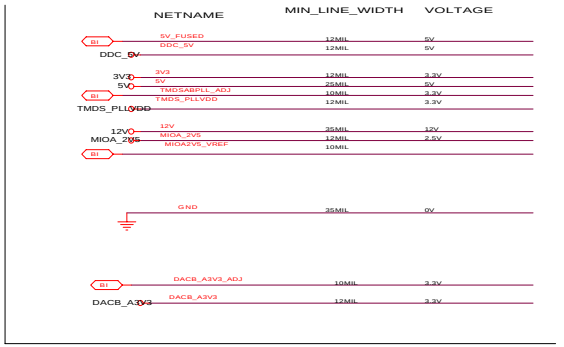
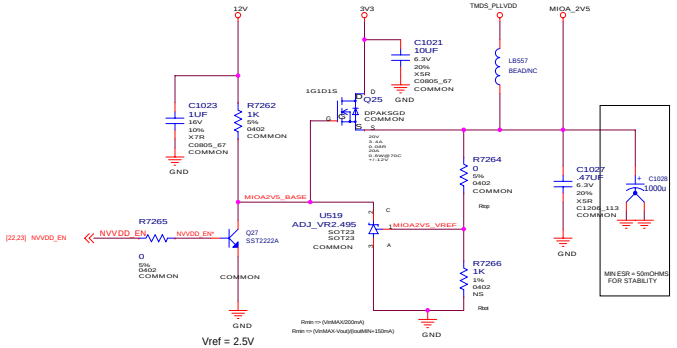
Power Supply TMDS/A3V3



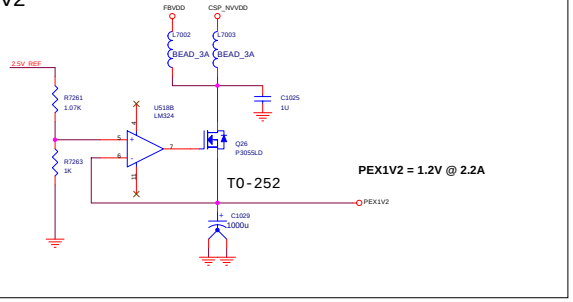


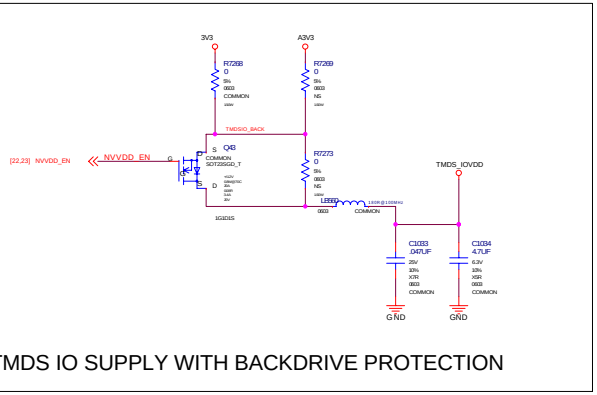


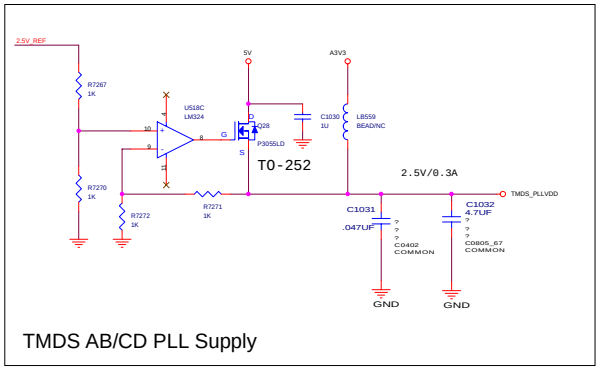
MIOA_VDDQ



PEX1V2







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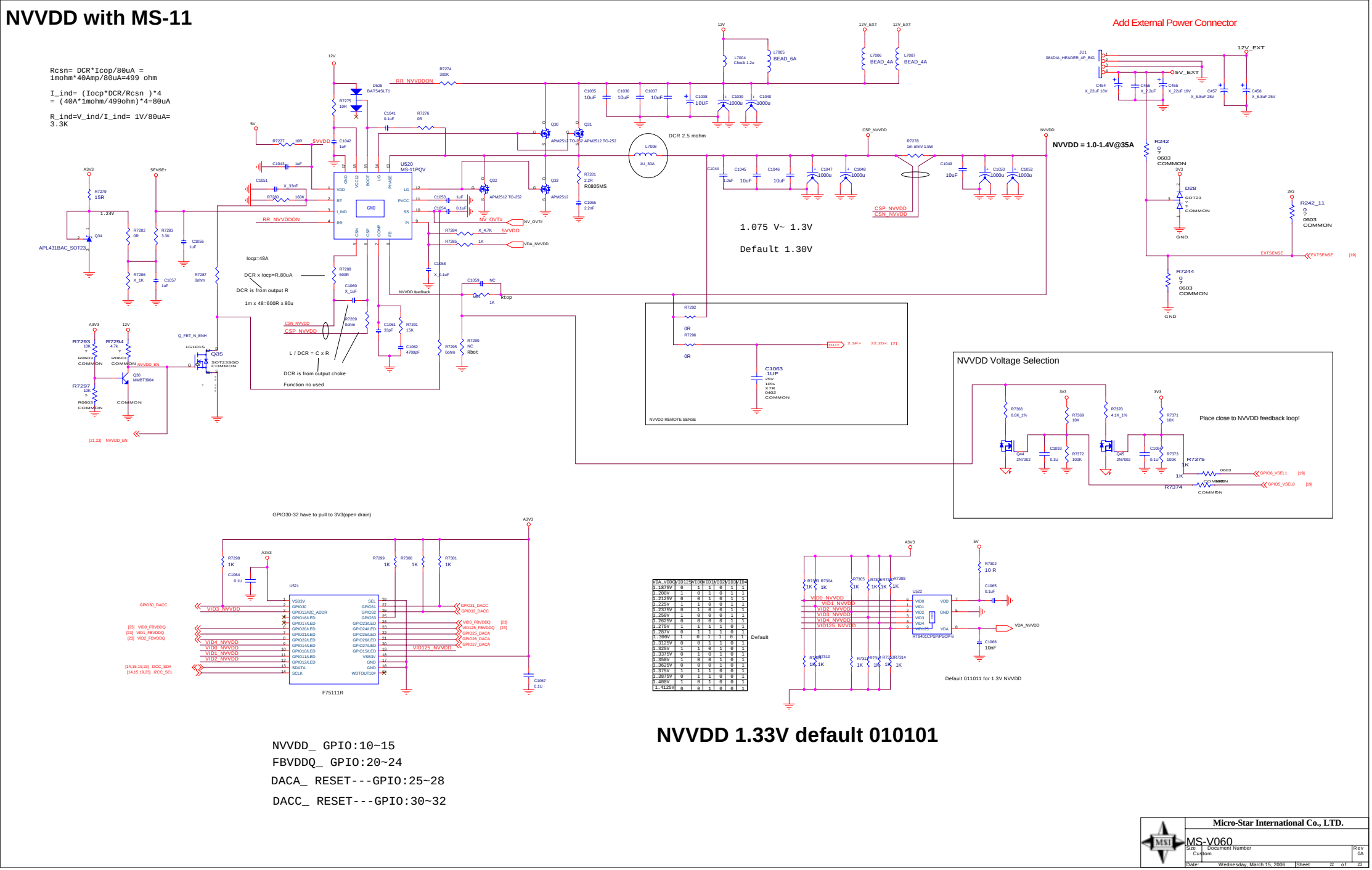
NVDD with MS-11



VDA_VDDQ	VID125	VID4	VID3	VID2	VID1	VID0
1.1875V	0	1	1	0	1	1
1.200V	1	0	1	0	1	1
1.2125V	0	0	1	0	1	1
1.225V	1	1	0	0	1	1
1.2375V	0	1	0	0	1	1
1.250V	1	0	0	0	1	1
1.2625V	0	0	0	0	1	1
1.275V	1	1	1	1	0	1
1.287V	0	1	1	1	0	1
1.300V	1	0	1	1	0	1
1.3125V	0	0	1	1	0	1
1.325V	1	1	0	1	0	1
1.3375V	0	1	0	1	0	1
1.350V	1	0	0	1	0	1
1.3625V	0	0	0	1	0	1
1.375V	1	1	1	0	0	1
1.3875V	0	1	1	0	0	1
1.400V	1	0	1	0	0	1
1.4125V	0	0	1	0	0	1

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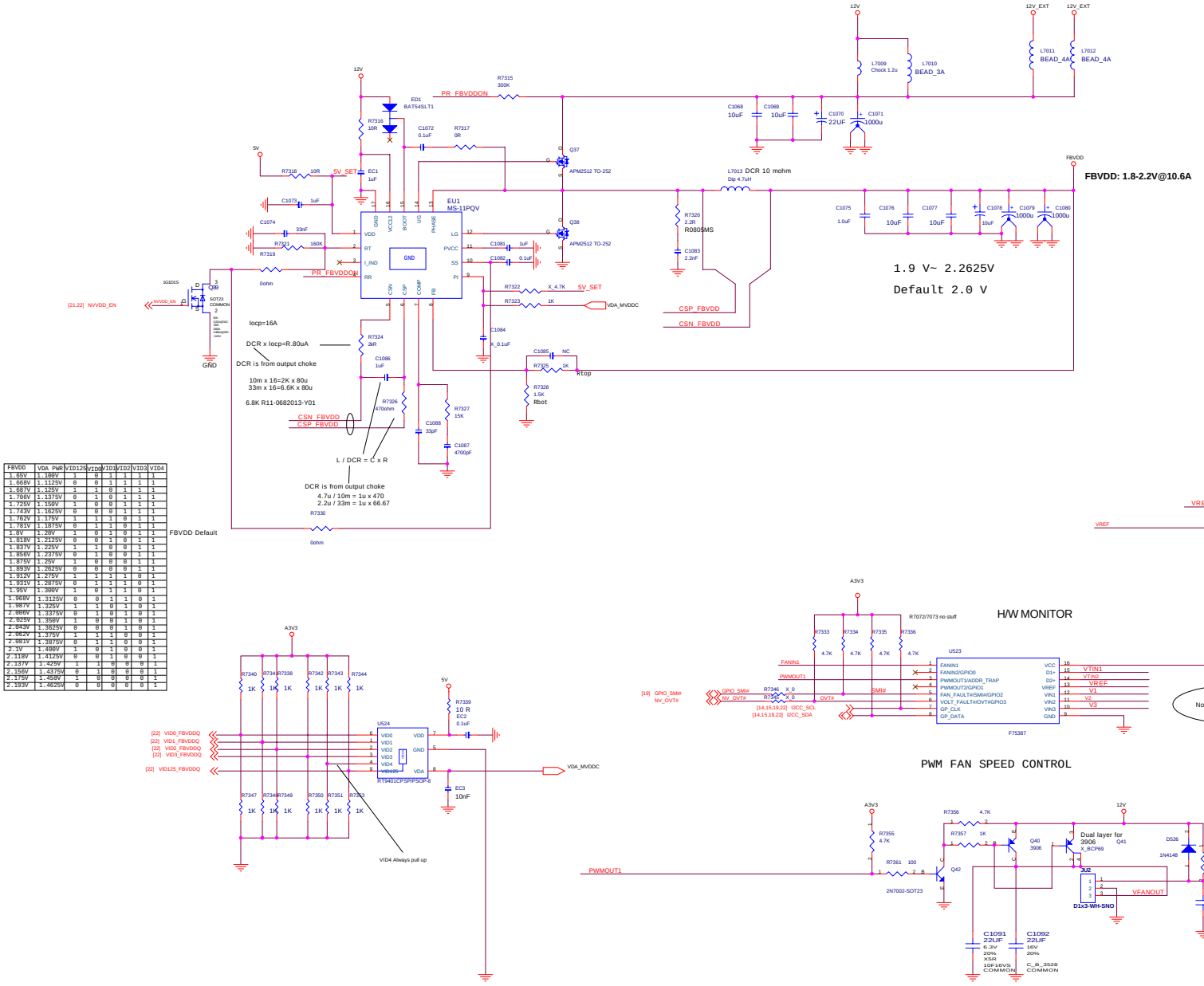
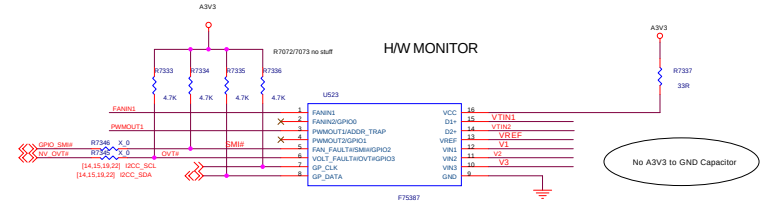
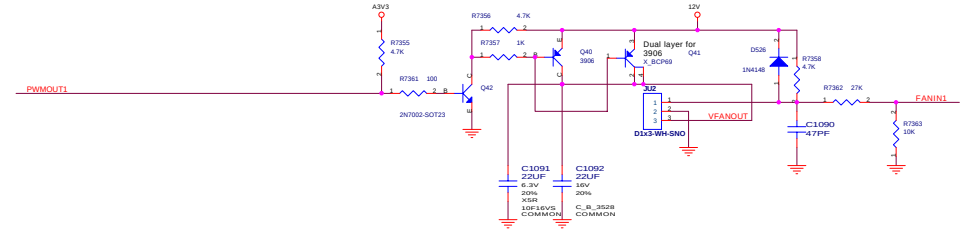
FBVDD with MS-11

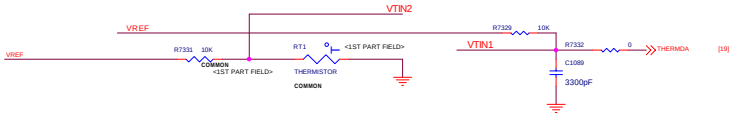


FBVDD	VDA_PWR	VID12S	VID6	VID1	VID2	VID3	VID4
1.65V	1.100V	1	0	1	1	1	1
1.668V	1.1125V	0	0	1	1	1	1
1.687V	1.125V	1	0	1	1	1	1
1.706V	1.1375V	0	1	0	1	1	1
1.725V	1.150V	1	0	0	1	1	1
1.743V	1.1625V	0	0	0	1	1	1
1.762V	1.175V	1	1	1	0	1	1
1.781V	1.1875V	0	1	1	0	1	1
1.8V	1.20V	1	0	1	0	1	1
1.818V	1.2125V	0	0	1	0	1	1
1.837V	1.225V	1	1	0	0	1	1
1.856V	1.2375V	0	1	0	0	1	1
1.875V	1.25V	1	0	0	0	1	1
1.893V	1.2625V	0	0	0	0	1	1
1.912V	1.275V	1	1	1	1	0	1
1.931V	1.2875V	0	1	1	1	0	1
1.95V	1.300V	1	0	1	1	0	1
1.968V	1.3125V	0	0	1	1	0	1
1.987V	1.325V	1	1	0	1	0	1
2.006V	1.3375V	0	1	0	1	0	1
2.025V	1.350V	1	0	0	1	0	1
2.043V	1.3625V	0	0	0	1	0	1
2.062V	1.375V	1	1	1	0	0	1
2.081V	1.3875V	0	1	1	0	0	1
2.1V	1.400V	1	0	1	0	0	1
2.118V	1.4125V	0	0	1	0	0	1
2.137V	1.425V	1	1	0	0	0	1
2.156V	1.4375V	0	1	0	0	0	1
2.175V	1.450V	1	0	0	0	0	1
2.193V	1.4625V	0	0	0	0	0	1





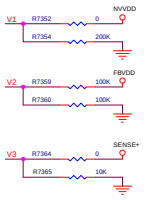
TEMPERATURE MONITOR



H/W MONITOR

PWM FAN SPEED CONTROL

VOLTAGE SENSORING CIRCUIT



VOLTAGE SENSORING CIRCUIT

Micro-Star International Co., LTD.			
MS-V060			
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