MS-V089 -- G73GT/G84, 128/256 MB 16x32 DDR3-136pin, DVI-I,SD/HDTV,VIVO,HDMI

SUMMARY:

1. Base on V069-100 to Modify HDMI change to internal support
2. BGA-136 DDRIII
3. RT-8805 Two Phase PWM for NVVDD
4. MS-11 for FBVDD

Table of Contents:

Rev History

OA

Page 3 Enable G23pin H_PLLVDD 1V2 for G84 only
Page 11 reserve G84 SLI circuit
Page 12,13,14 reserve DAC_Vref power for G84 DACA,B,C
Page 16 reserve 1V8 for G84 IFPAB_PLLVDD
Page 17 reserve 1V8 for G84 IFPCD_PLLVDD
Page 18 reserve 1V2 for G84 PLLVDD and VID_PLLVDD
Page 20 reserve MIOB_CTL3 new strap for G84 PCI_DEVID_4
Page 20 reserve ROM_SI pull-down resister required if MIOA VDDQ=2.5V for G84
Page 21add 1V8 power for G84
Page 22,23 Reserve MS-V1co-lay circuit

100

Page 3 H_PLLVDD 1V2 use 0ohm connect to PEX1V2
Page 3 Reserve G84 Dual Rank(Stacked Die) circuit FBA_CMD7----CS1 FBA_CMD27---BA2
Page 7 Reserve G84 Dual Rank(Stacked Die) circuit FBC_CMD7----CS1 FBC_CMD27---BA2
Page 7 Reserve I2CS citcuit for G84
Page 6,10 Enable FBAA2 and FBCC2 BA2 Pin this is for Stacked Die Function
Page 13 Modify RGB circuit
Page 15 Modify SAA7115 RESET circuit
Page 18 Modify Spidf circuit
Page 21 Modify Linear Power circuit
Page 22 NVVDD PWM Change to RT-8805 Two Phase
Page 22,23 Remove MS-V1co-lay circuit

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	SUMMARY		
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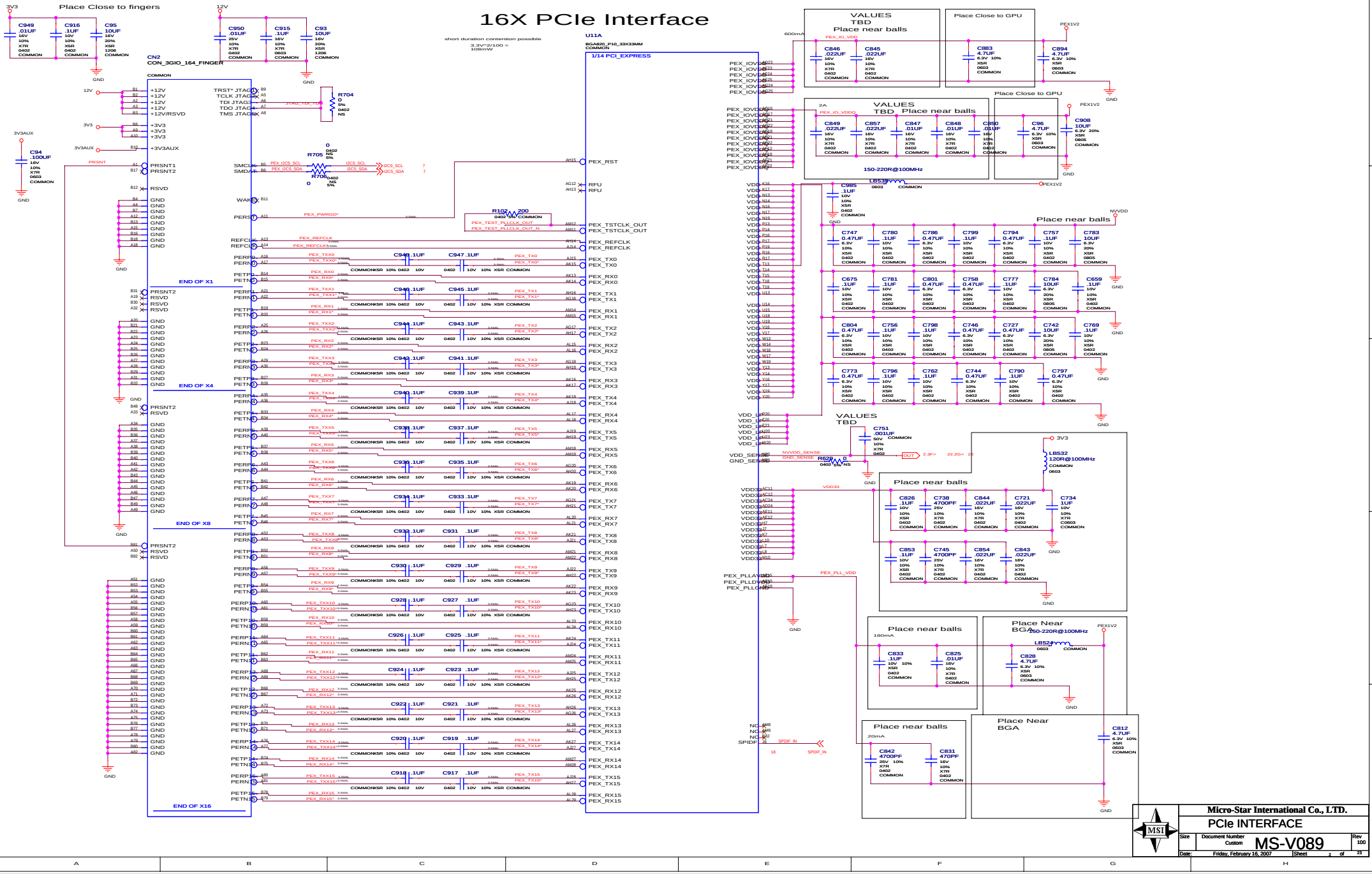
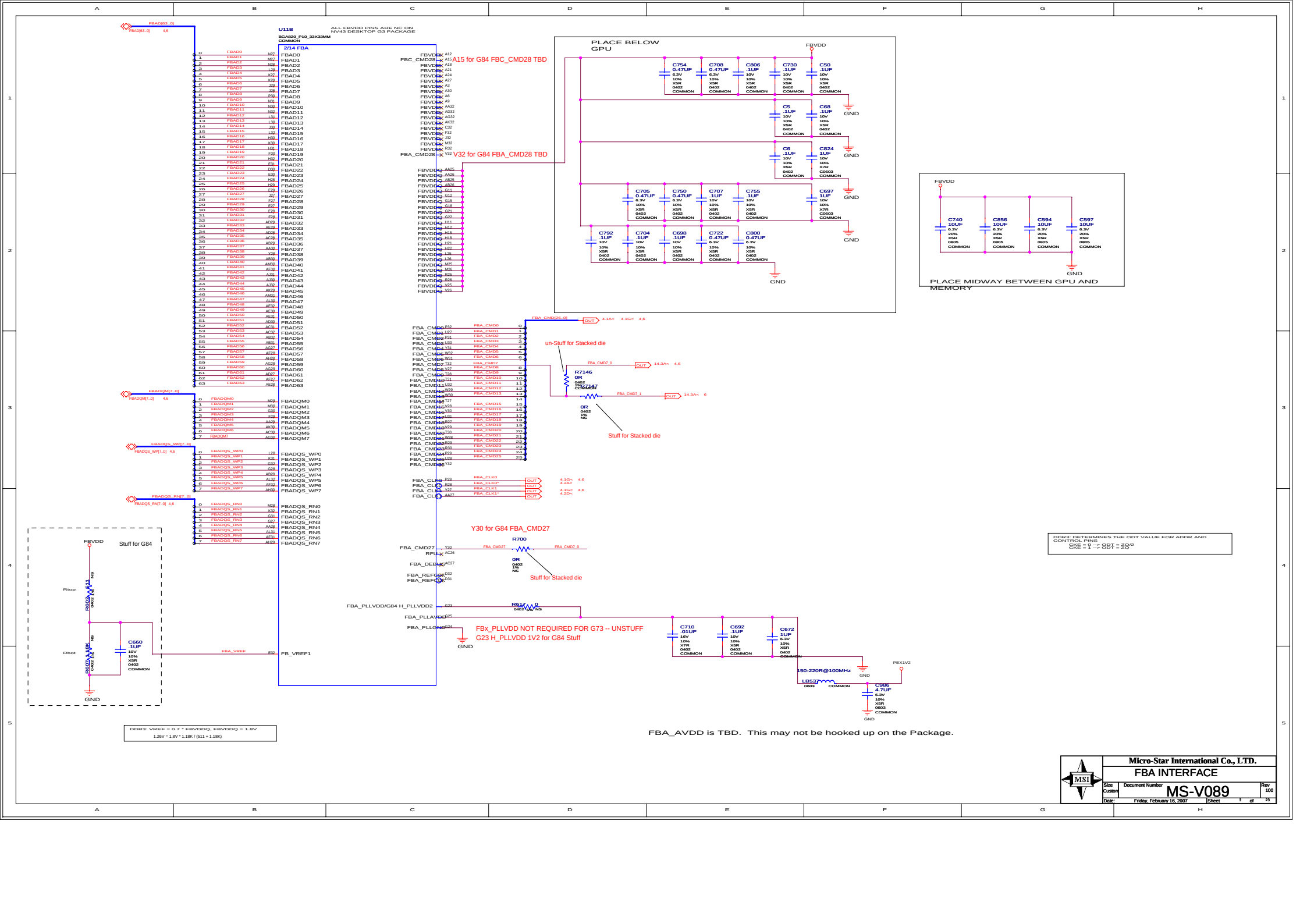
16X PCIe Interface




U11B
BGA820_P10_33X33MM
COMMON
ALL FBVDD PINS ARE NC ON NV43 DESKTOP G3 PACKAGE
2/14 FBA
A15 for G84 FBC_CMD28 TBD
V32 for G84 FBA_CMD28 TBD
PLACE BELOW GPU
FBVDD
GND
PLACE MIDWAY BETWEEN GPU AND MEMORY
un-Stuff for Stacked die
Stuff for Stacked die
R7146 0R 0402 1% NS
Y30 for G84 FBA_CMD27
R700 0R 0402 1% NS
FBx_PLLVDD NOT REQUIRED FOR G73 -- UNSTUFF
G23 H_PLLVDD 1V2 for G84 Stuff
R617 0 0402 1% NS
150-220R@100MHz
LB537 0603 COMMON
PEX1V2
Stuff for G84
Rtop
Rbot
C660 .1UF 10V 10% XSR 0402 COMMON
DDR3: VREF = 0.7 * FBVDDQ, FBVDDQ = 1.8V
1.26V = 1.8V * 1.18K / (511 + 1.18K)
DDR3: DETERMINES THE ODT VALUE FOR ADDR AND CONTROL PINS
CKE = 0 --> ODT = 2G/2
CKE = 1 --> ODT = 2G
FBA_AVDD is TBD. This may not be hooked up on the Package.
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FBA INTERFACE
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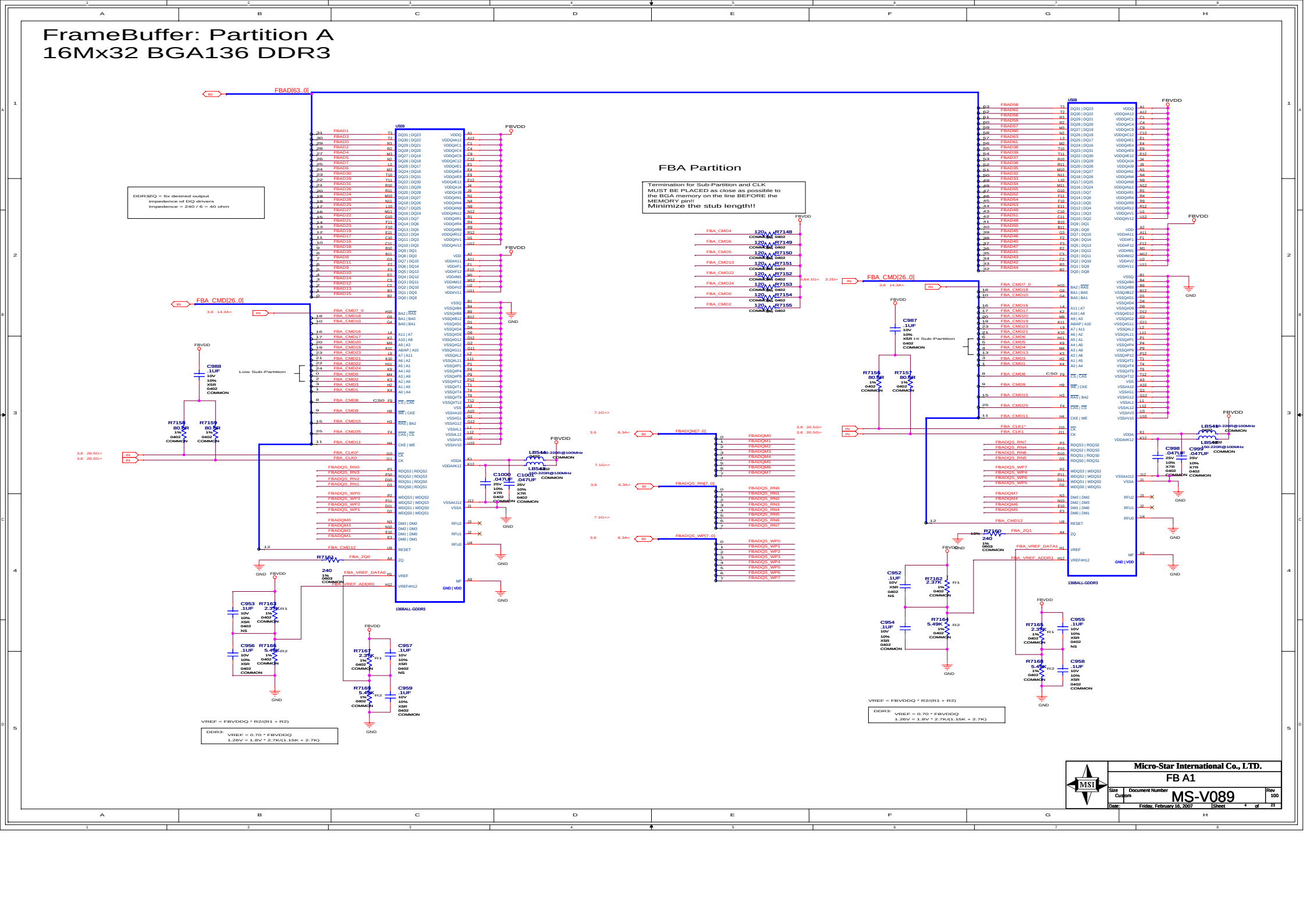
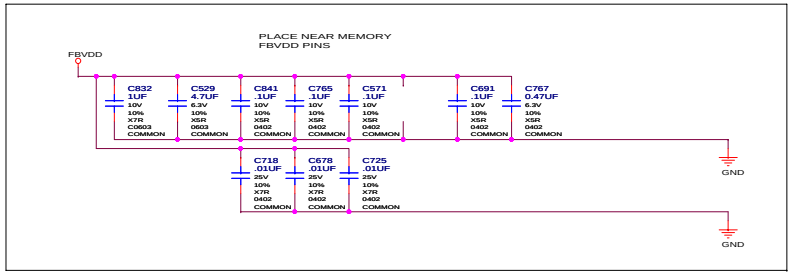
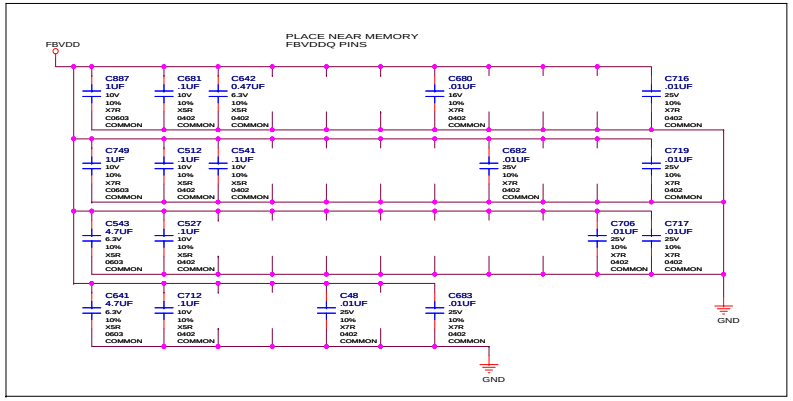
FrameBuffer: Partition A
16Mx32 BGA136 DDR3



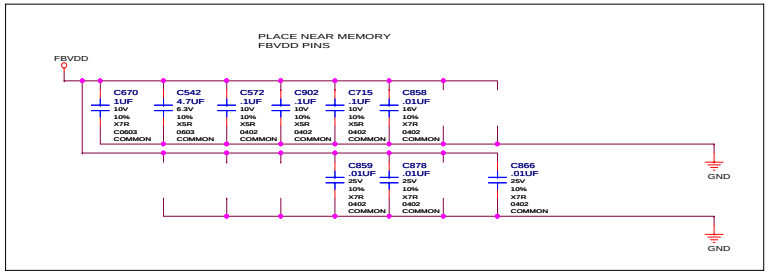
FRAME BUFFER: PARTITION A DECOUPLING

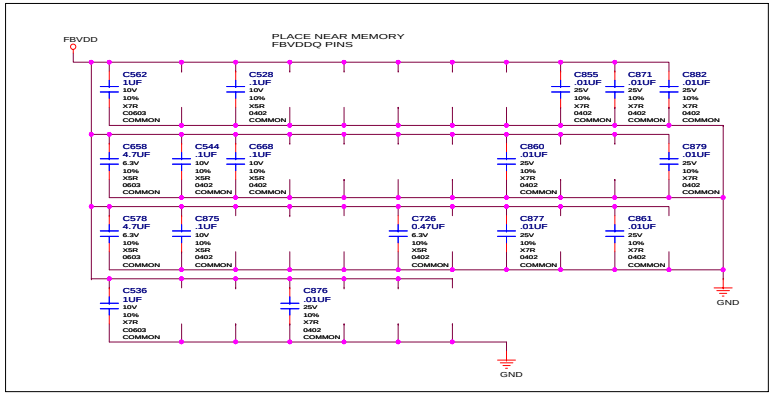
Decoupling for FBA 0..31





Decoupling for FBA 32..63





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FBA DECOUPLING	
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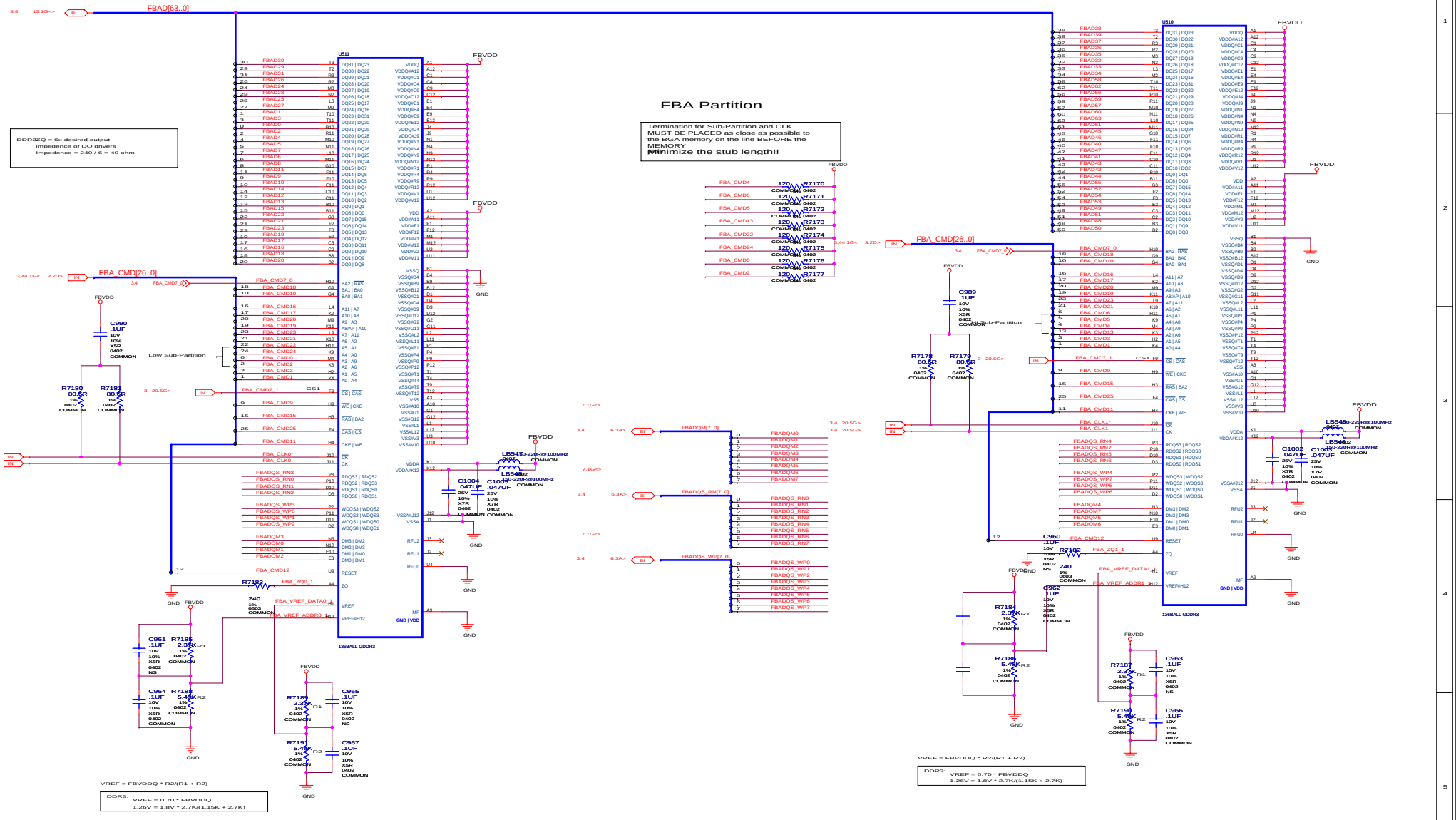
FrameBuffer: Partition A
16Mx32 BGA136 DDR3



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FB A2			
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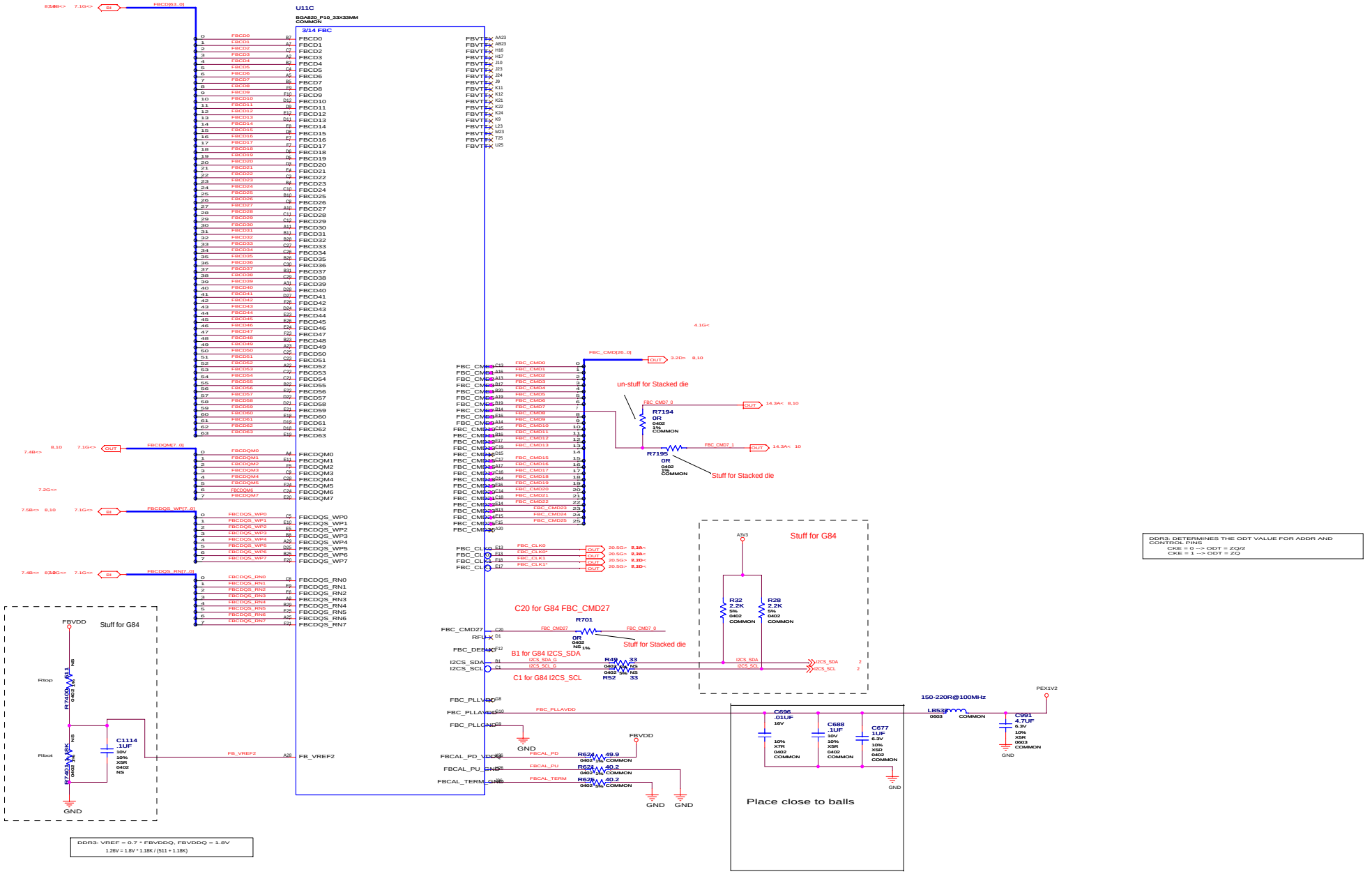
U11C
BGA820_P10_33X33MM
COMMON
3/14 FBC
FBCD(63..0)
FBCDQM(7..0)
FBCDQS_WP(7..0)
FBCDQS_RN(7..0)
FBVDD
Stuff for G84
Rtop
Rbot
R7400 .61
R7401 1.18K
C1114 .1UF 10V 10% X5R 0402 NS
GND
FB_VREF2
DDR3: VREF = 0.7 * FBVDDQ, FBVDDQ = 1.8V
1.26V = 1.8V * 1.18K / (511 + 1.18K)
FBC_CMD[26..0]
un-stuff for Stacked die
R7194 0R 0402 1% COMMON
R7195 0R 0402 1% COMMON
Stuff for Stacked die
C20 for G84 FBC_CMD27
R701 0R 0402 NS 1%
B1 for G84 I2CS_SDA
C1 for G84 I2CS_SCL
R49 33 0402 NS
R52 33
Stuff for G84
R32 2.2K 5% 0402 COMMON
R28 2.2K 5% 0402 COMMON
DDR3: DETERMINES THE ODT VALUE FOR ADDR AND CONTROL PINS
CKE = 0 --> ODT = ZQ/2
CKE = 1 --> ODT = ZQ
FBVTT
FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_TERM_GND
R624 49.9 1% COMMON
R624 40.2 1% COMMON
R626 40.2 1% COMMON
C696 .01UF 16V 10% X7R 0402 COMMON
C688 1UF 10V 10% X5R 0402 COMMON
C677 1UF 6.3V 10% X5R 0402 COMMON
Place close to balls
150-220R@100MHz
LB538 0603 COMMON
C951 4.7UF 6.3V 10% X5R 0603 COMMON
PEX1V2
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FBC INTERFACE
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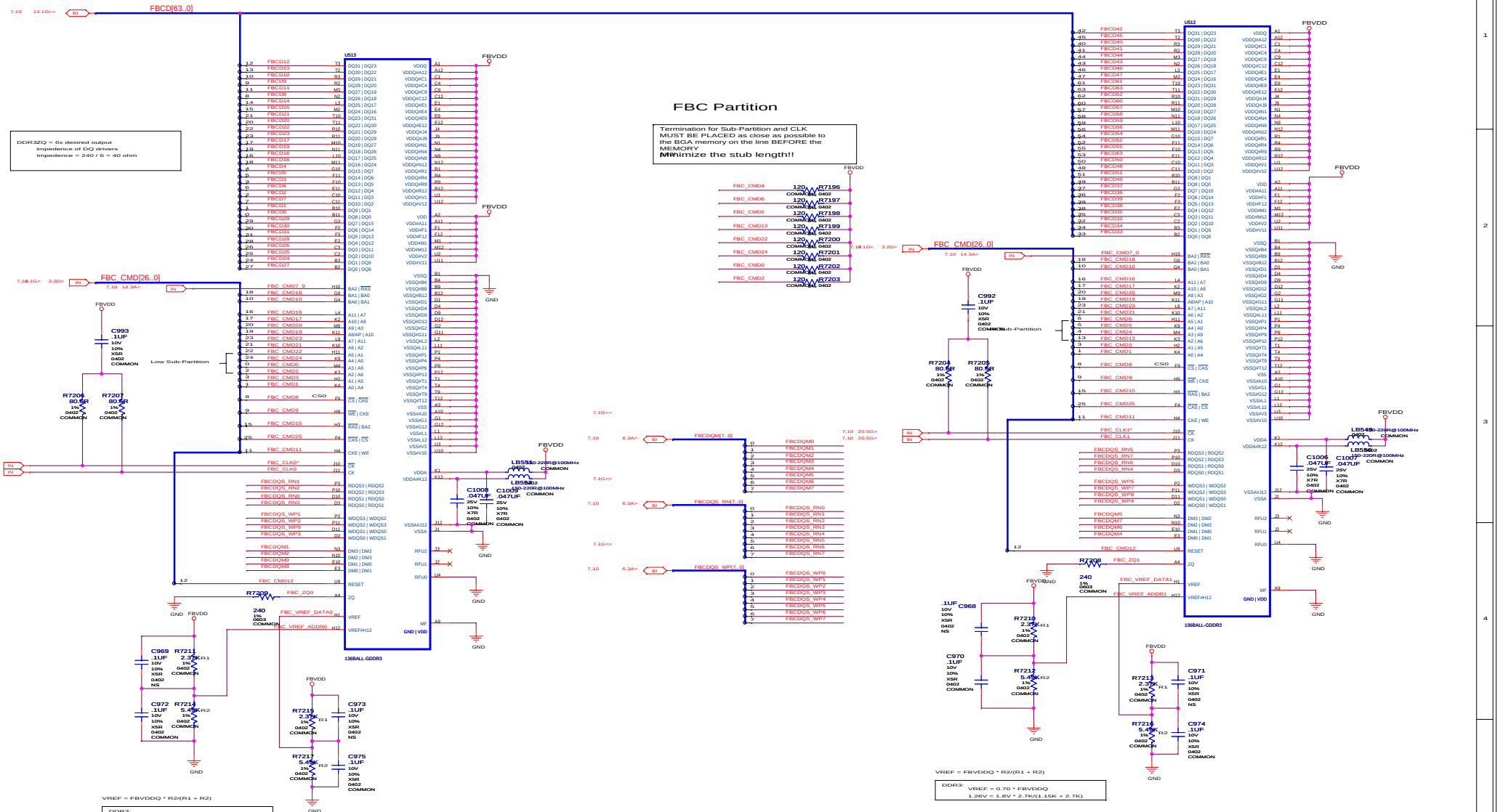
FRAMEBUFFER: PARTITION
C 16Mx32 BGA136 DDR3



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FB C1			
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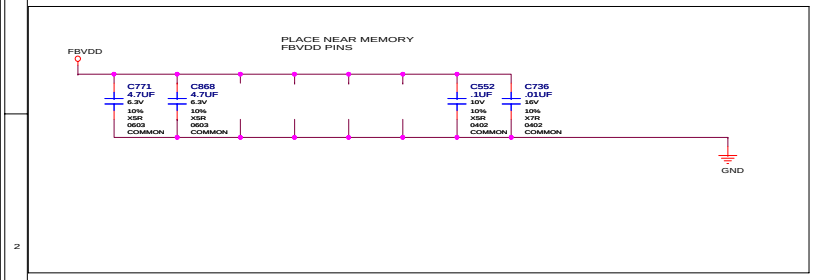
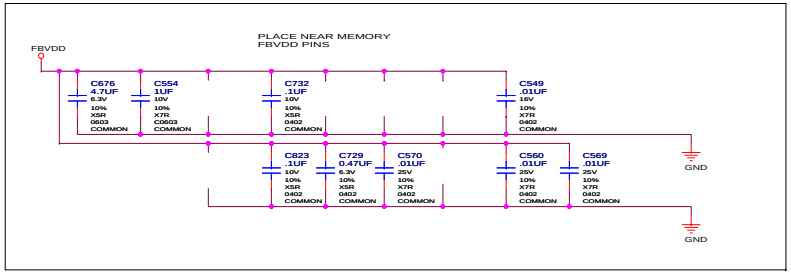
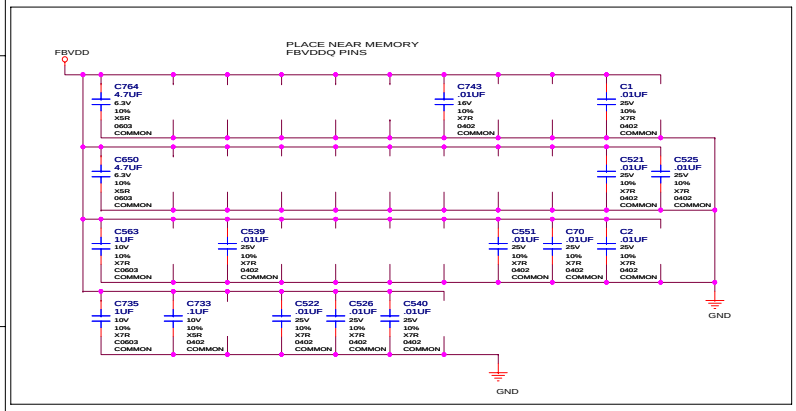
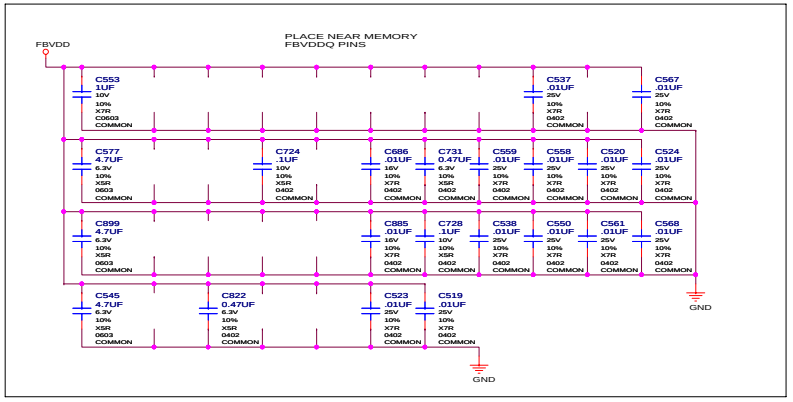
FRAMEBUFFER: PARTITION C DECOUPLING

Decoupling for FBC 0..31

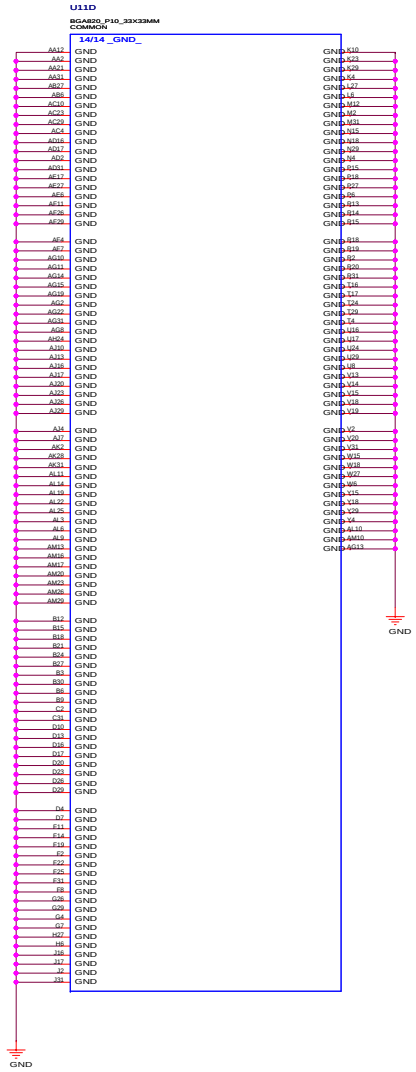








Decoupling for FBC 32..63



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FBC DECOUPLING	
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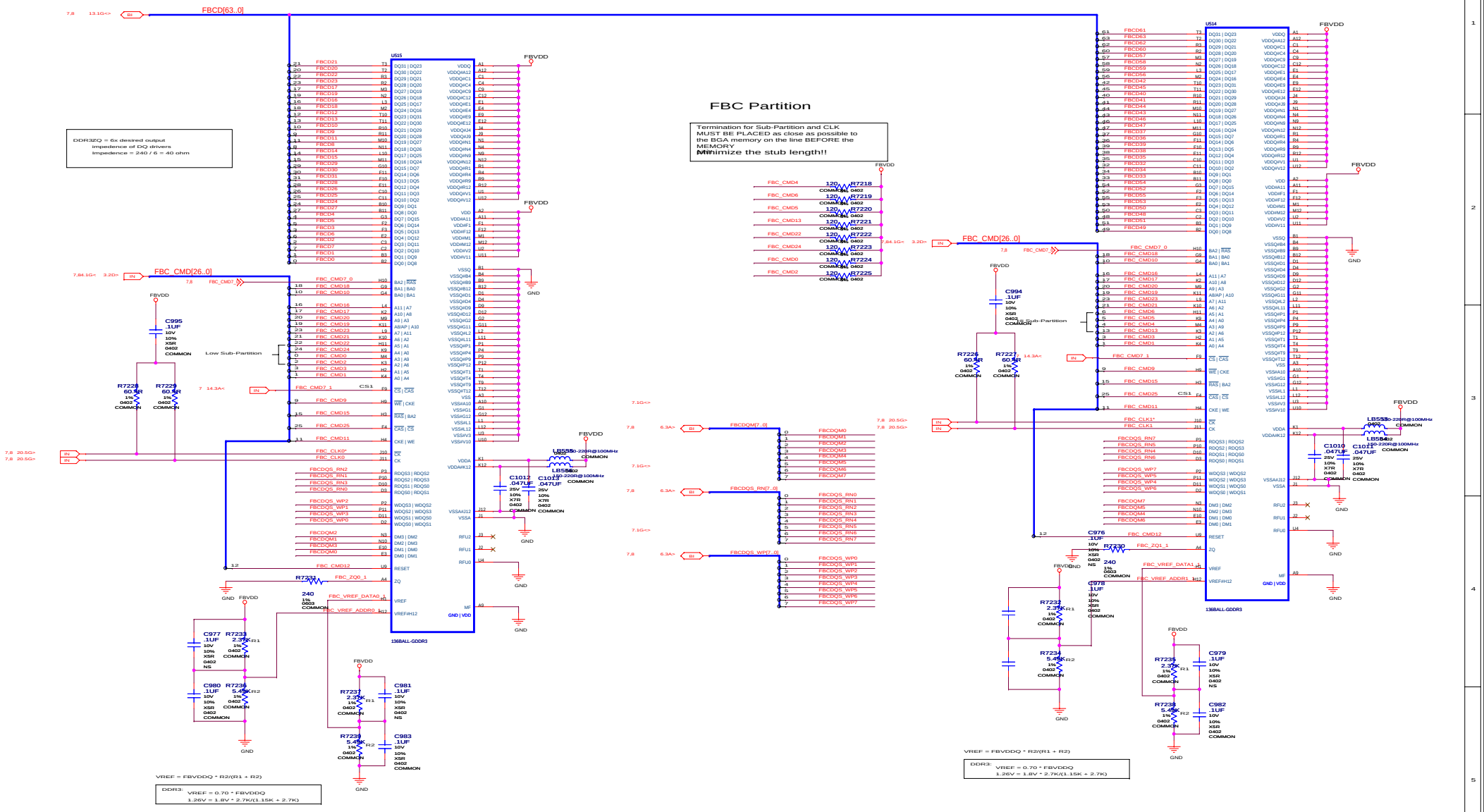
FRAMEBUFFER: PARTITION
C 8Mx32 BGA136 DDR3



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FB C2	
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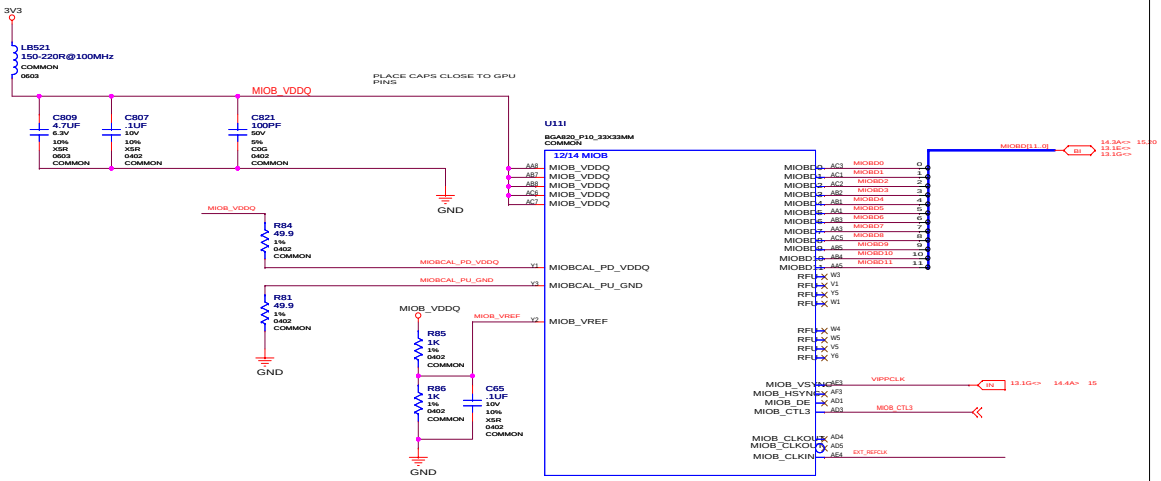
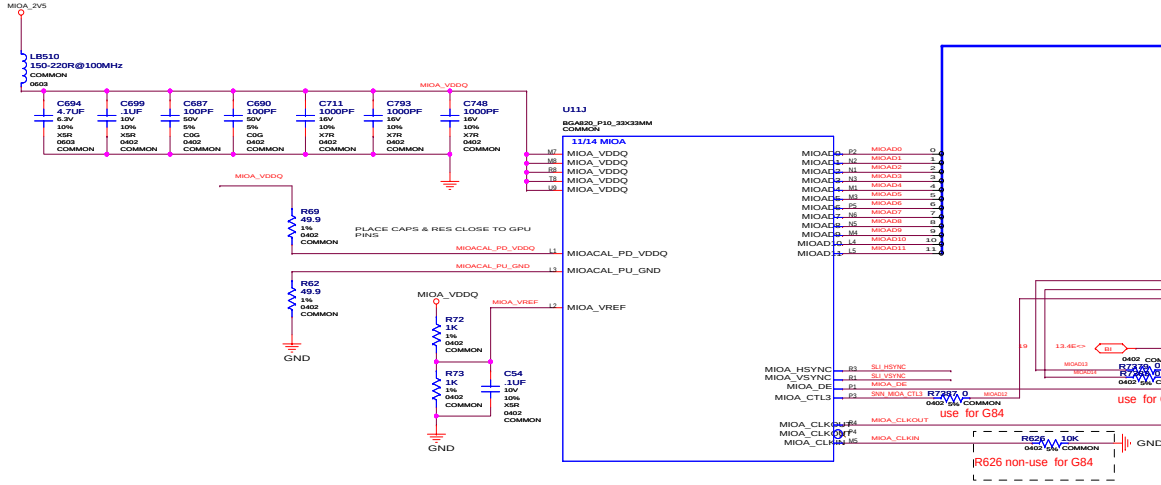
G3 VIP/MIOB

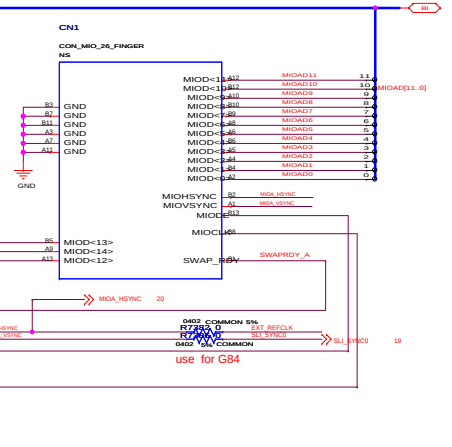


NETNAME	MIN_LINE_WIDTH	SPACING RULE
MIOBD[7..0]	3.5MIL	15MIL

G3 MIOA



Feature Connector



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MIOA/MIOB			
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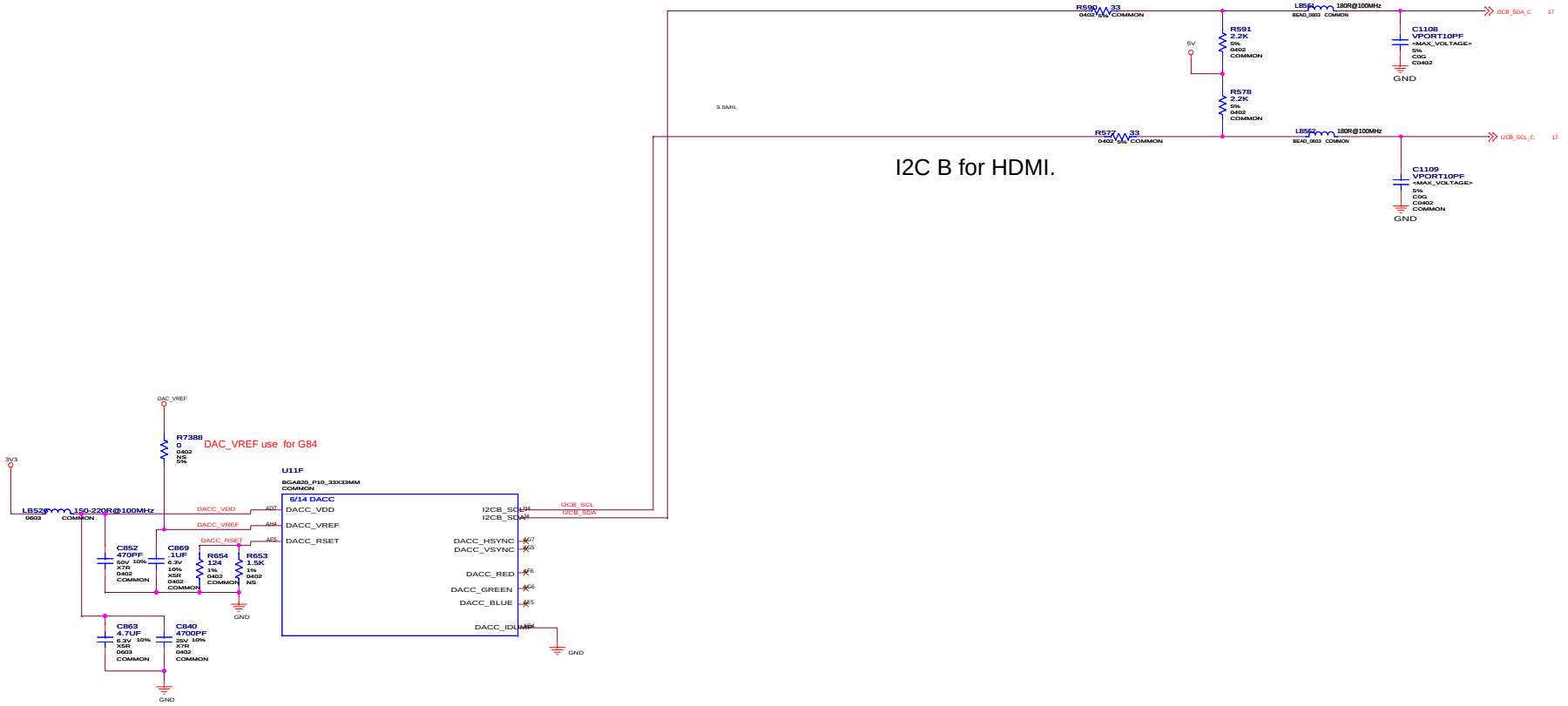
Secondary Display (DACC), HDMI



Micro-Star International Co., LTD.		
DACC		
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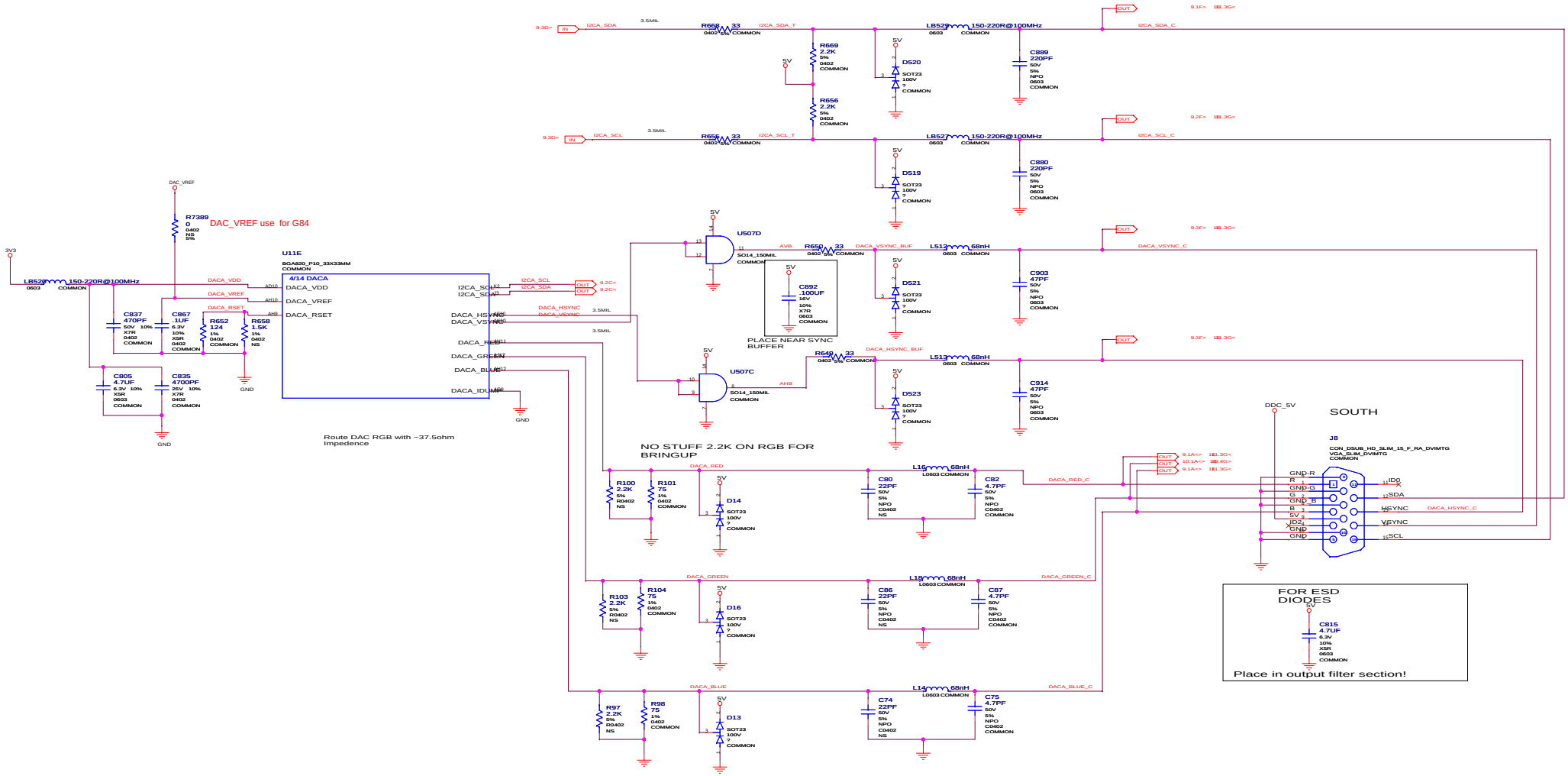
Primary Display (DACA), Slim DB15

DACA
RGB-FILTER



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DACA	
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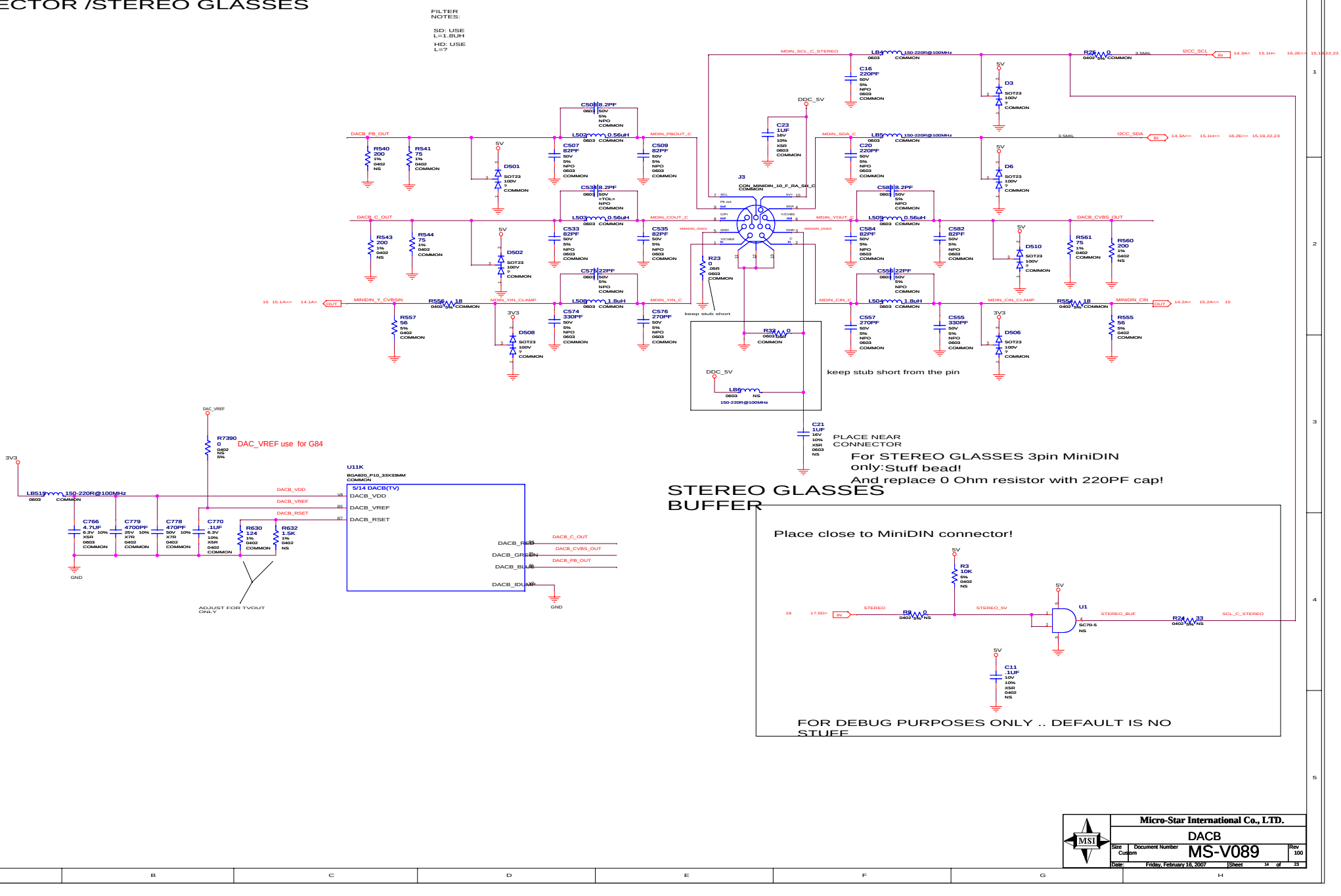
DACB .. MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES



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DACB	
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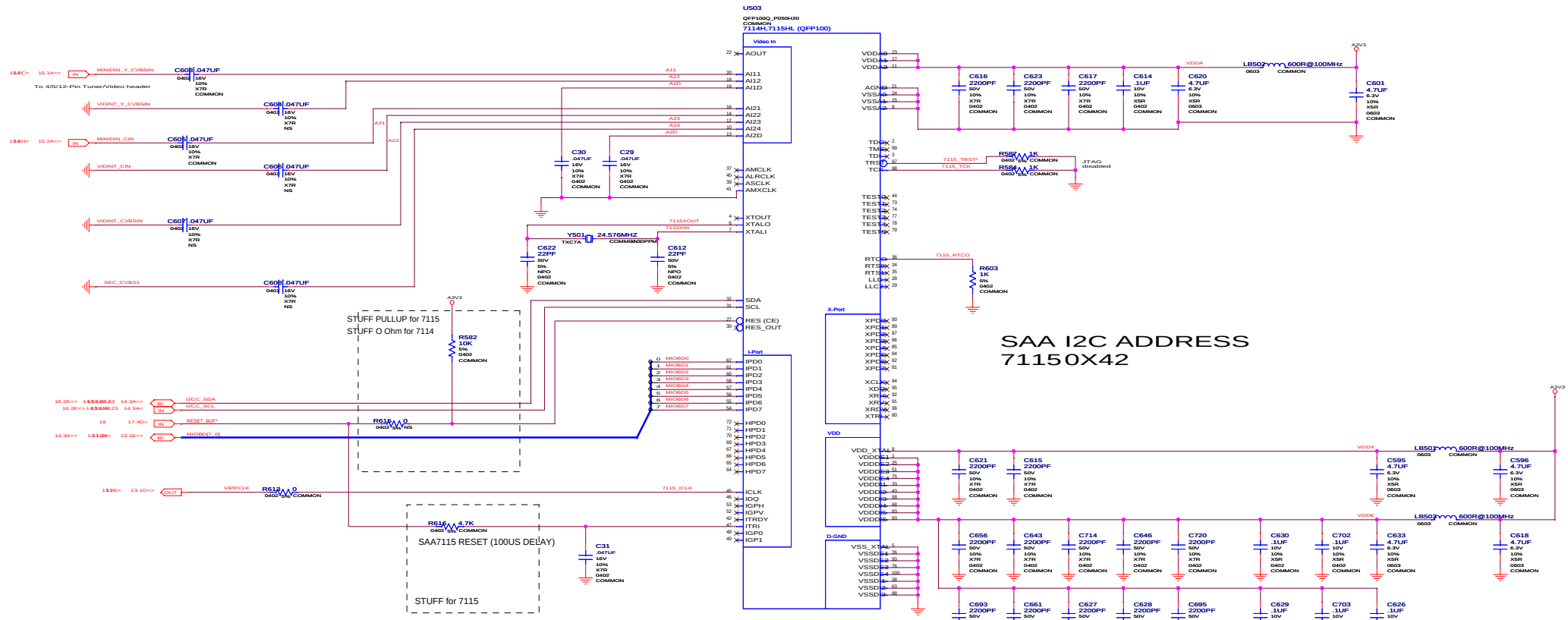
PHILIPS
VIDEO
CAPTURE



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VIDEO CAPTURE	
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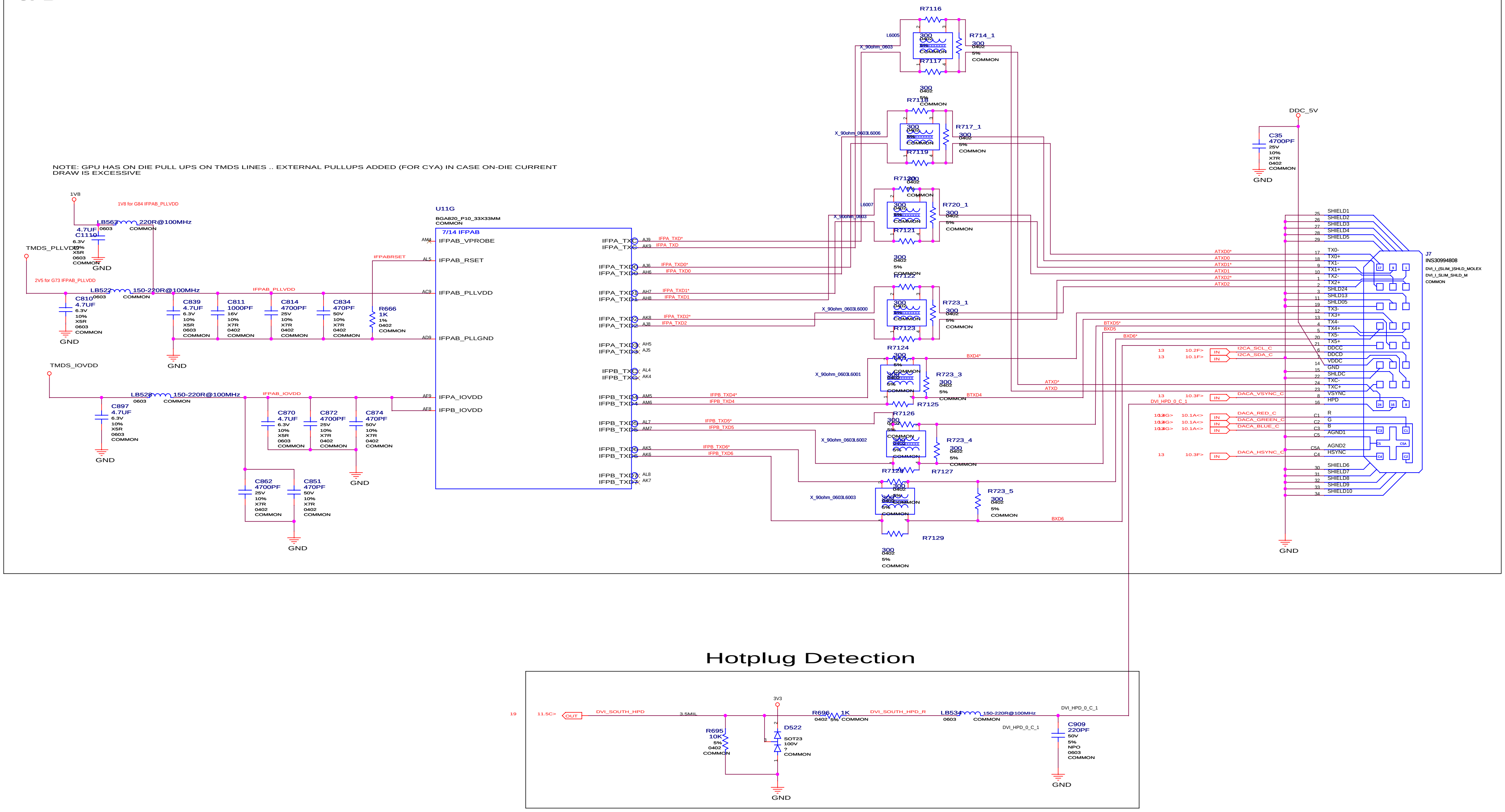
INTERNAL TMDS .. LINK A & B

NOTE: GPU HAS ON DIE PULL UPS ON TMDS LINES .. EXTERNAL PULLUPS ADDED (FOR CYA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE



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TMDS LINK A & B		
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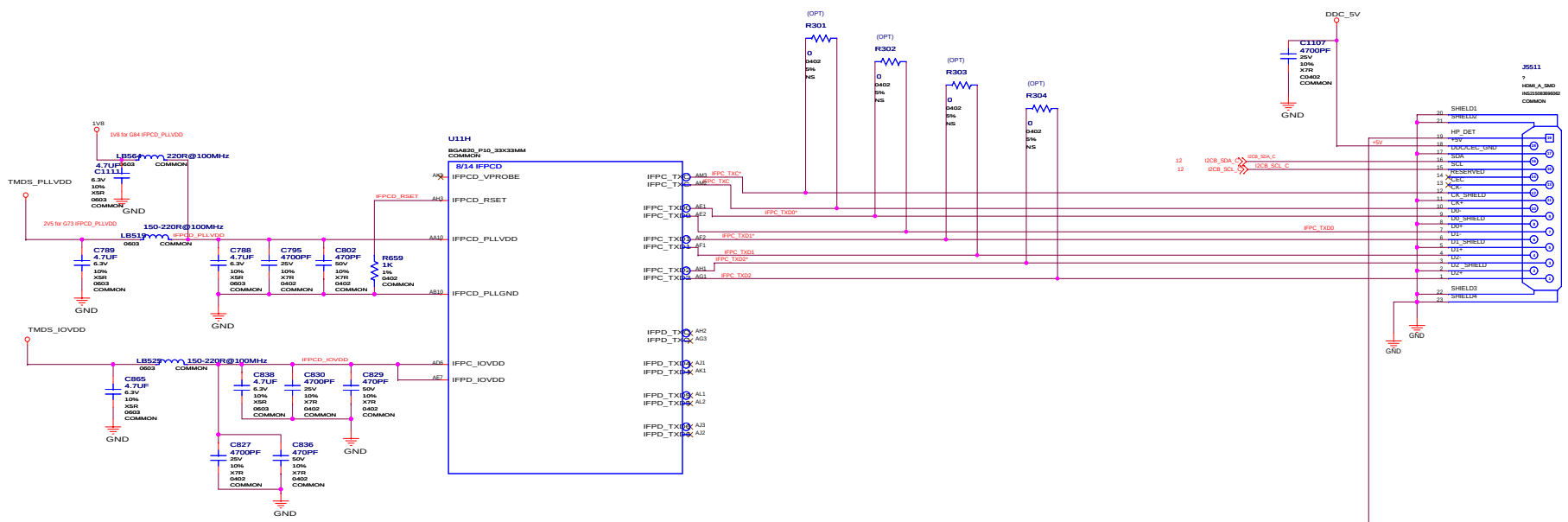
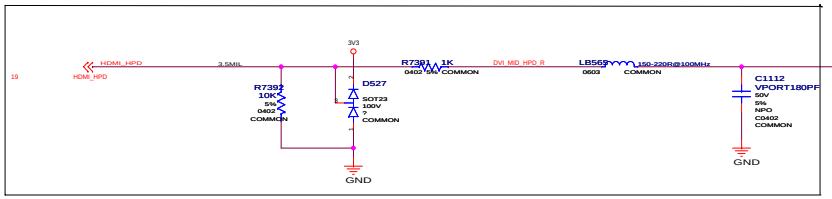
INTERNAL TMDS
.. LINK C & D



Hotplug Detection



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TMDS LINK C & D	
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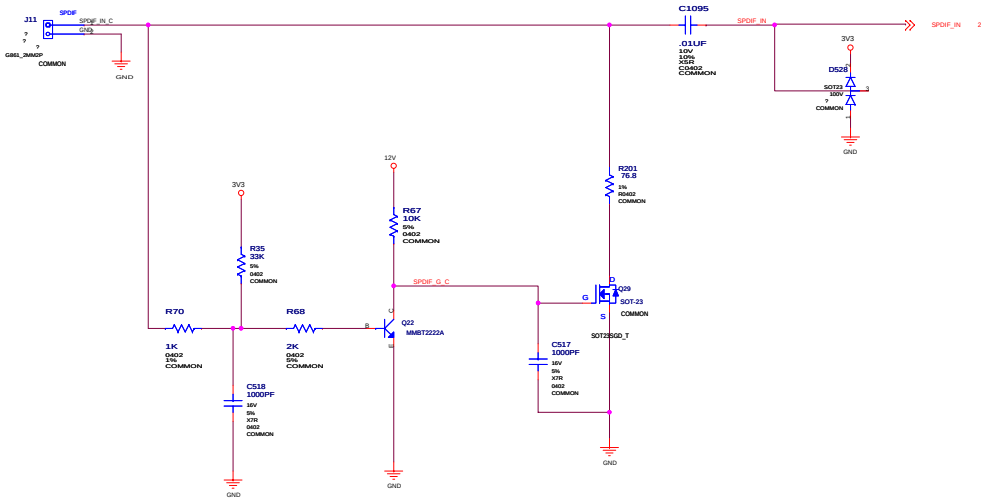
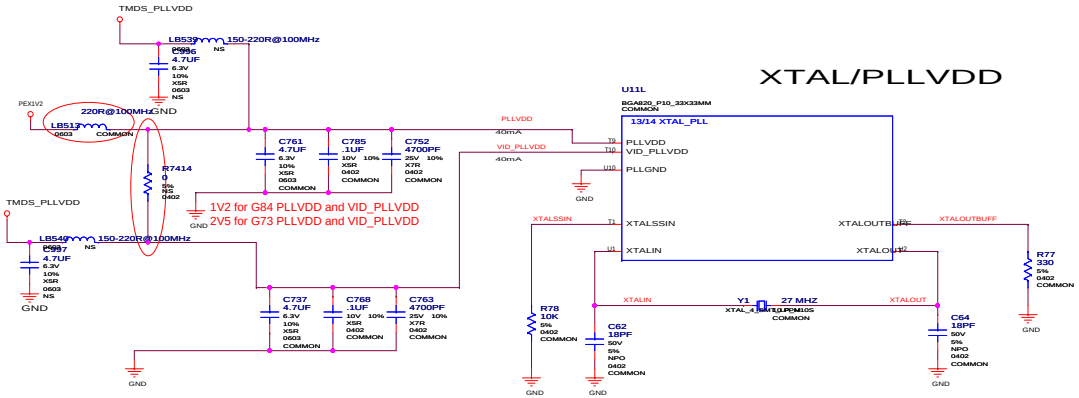
SPDIF IN





MSI	Micro-Star International Co., LTD.	
	4-Pin Video-In/SPDIF IN	
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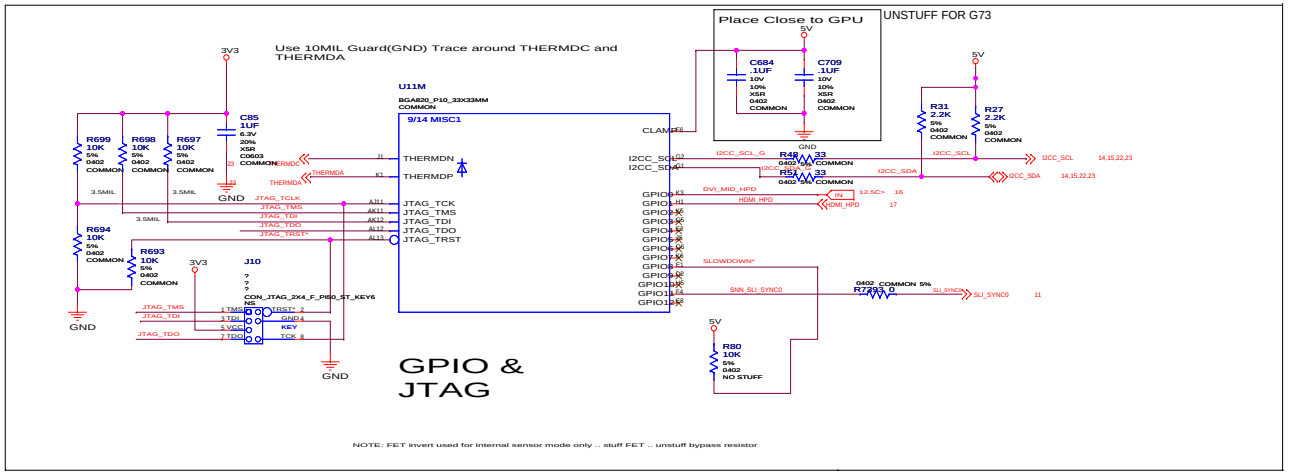
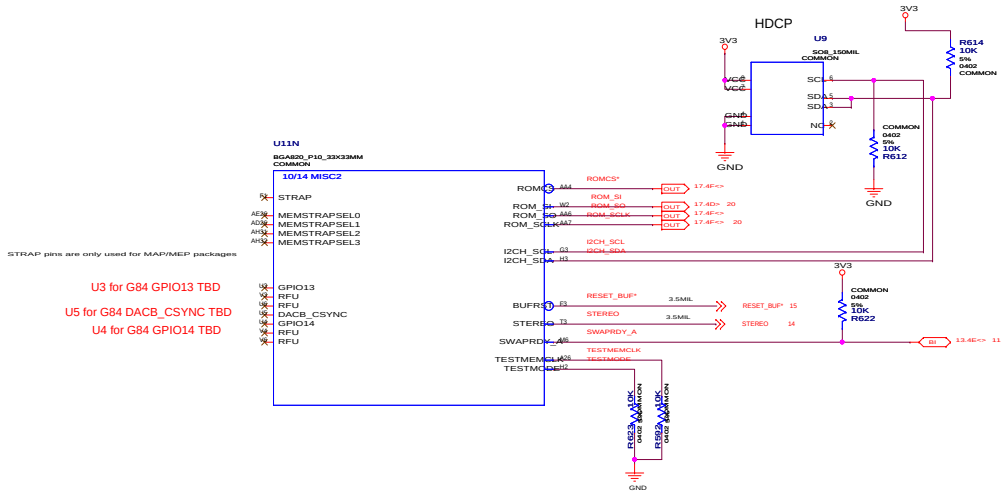
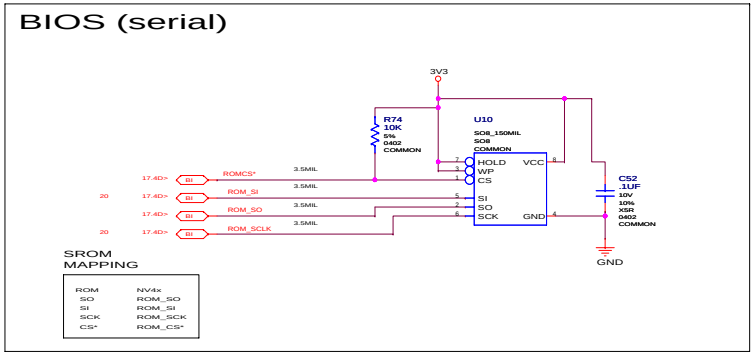


GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	HDMI hotplug
2	IN	RESERVED
3	IN	RESERVED
4	IN	TUNER IRQ
5	OUT	NVVDD VOLTAGE SELECT 0
6	OUT	NVVDD VOLTAGE SELECT 1
7	Out	TPI INTERRUPT ENABLE
8	IN	RESERVED
9	OUT	PWM FAN
10	IN	INT from Sii1930
11	IN	TVRSET
12	IN	uC PROGRAMMING CONTROL





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GPIO/ROM/HDCP ROM	
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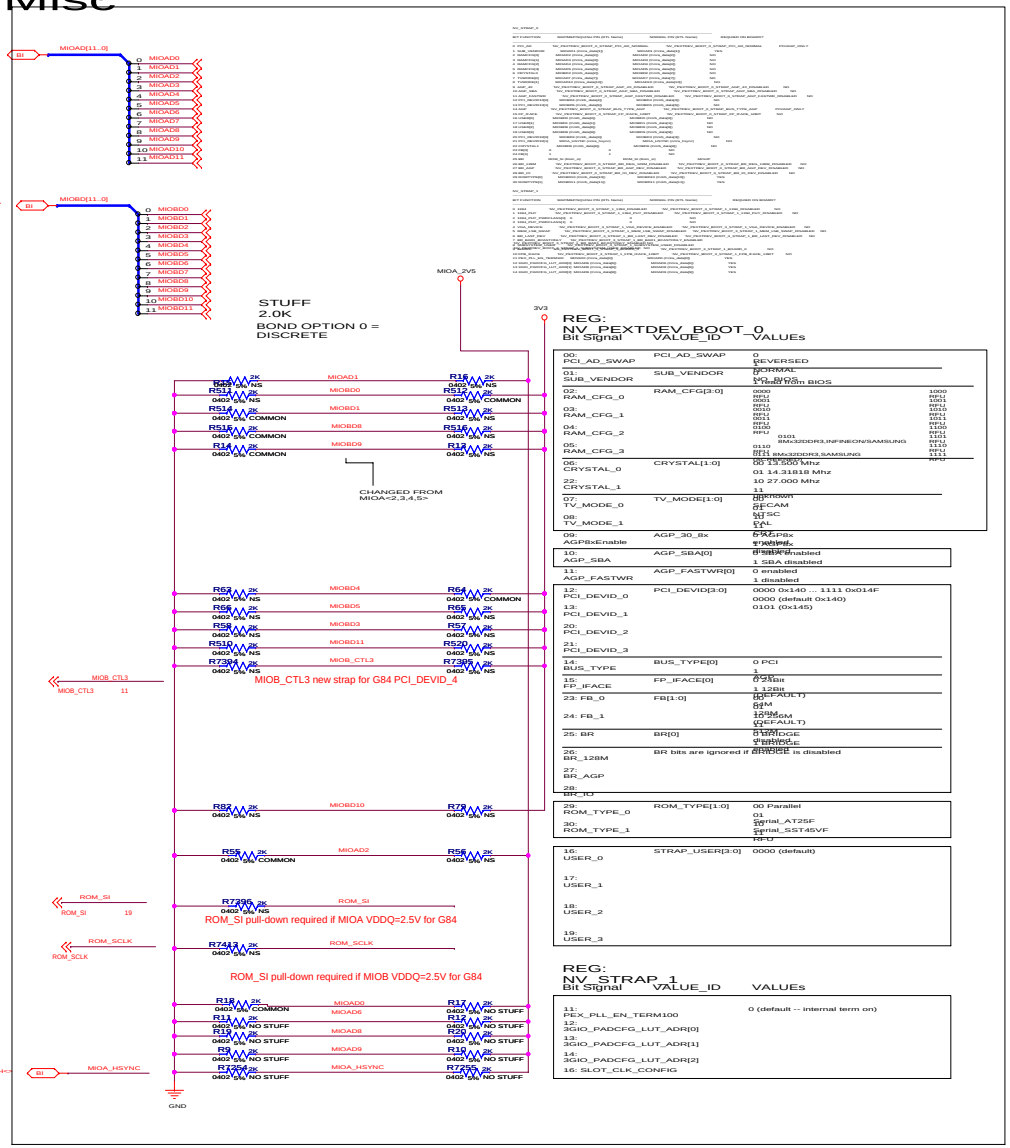
BIOS, Straps, Misc

Straps

Assembly: BIOS



REG: NV_PEXTDEV_BOOT_0

Bit	Signal	VALUE_ID	VALUEs
00:	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED 1 NORMAL
01:	SUB_VENDOR	SUB_VENDOR	0 NO_BIOS 1 Defined from BIOS
02:	RAM_CFG_0	RAM_CFG[3:0]	0000 RFU 0001 RFU 0010 RFU 0011 RFU 0100 RFU 0101 RFU 0110 RFU 0111 RFU 1000 RFU 1001 RFU 1010 RFU 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 RFU
03:	RAM_CFG_1		
04:	RAM_CFG_2		
05:	RAM_CFG_3		0101 8Mx32DDR3,INFINEON/SAMSUNG 0110 RFU 0111 8Mx32DDR3,SAMSUNG
06:	CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz 01 14.31818 Mhz 10 27.000 Mhz 11
22:	CRYSTAL_1		
07:	TV_MODE_0	TV_MODE[1:0]	00 NTSC 01 SECAM 10 NTSC 11 PAL
08:	TV_MODE_1		
09:	AGP_30_8x	AGP_30_8x	0 AGP8x enabled 1 AGP30 enabled
10:	AGP_SBA	AGP_SBA[0]	0 SBA enabled 1 SBA disabled
11:	AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled
12:	PCI_DEVID_0	PCI_DEVID[3:0]	0000 0x140 .. 1111 0x014F 0000 (default 0x140) 0101 (0x145)
13:	PCI_DEVID_1		
20:	PCI_DEVID_2		
21:	PCI_DEVID_3		
14:	BUS_TYPE	BUS_TYPE[0]	0 PCI 1 PCIe
15:	FP_IFACE	FP_IFACE[0]	0 24bit 1 12Bit
23:	FB_0	FB[1:0]	00 (DEFAULT) 01 64M 10 128M 11 256M (DEFAULT)
24:	FB_1		
25:	BR	BR[0]	0 BR/DDGE disabled 1 BR/DDGE enabled
26:	BR_128M	BR bits are ignored if BR/DDGE is disabled	
27:	BR_AGP		
28:	BR_IO		
29:	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F 10 Serial_SST45VF 11 RFU
30:	ROM_TYPE_1		
16:	USER_0	STRAP_USER[3:0]	0000 (default)
17:	USER_1		
18:	USER_2		
19:	USER_3		

REG: NV_STRAP_1

Bit	Signal	VALUE_ID	VALUEs
11:	PEX_PLL_EN_TERM100		0 (default -- internal term on)
12:	3GIO_PADCFG_LUT_ADR[0]		
13:	3GIO_PADCFG_LUT_ADR[1]		
14:	3GIO_PADCFG_LUT_ADR[2]		
16:	SLOT_CLK_CONFIG		

Mechanical parts

NEED FANSINK SYMBOL FOR P216

MEC2 — MEC_HEX_JACK_SCREW COMMON
MEC1 — MEC_HEX_JACK_SCREW COMMON
MEC4 — MEC_HEX_JACK_SCREW COMMON
MEC3 — MEC_HEX_JACK_SCREW COMMON

155-00002-0000-000 SCREW PHIL PAN HD SS MACH 4-40 3/16

BKT — BRKT_ADVIDB15S_BDVIDB15S_CDIN_2 COMMON

FAN — HSA_GPU_TM31-2_T_AL_1 COMMON

MECH MOUNTING TOP

PCB — PCB V089-100

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM5 SW_FB
FM4 SW_FB
FM6 SW_FB

Fiducial Point

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Straps/Mechanical			
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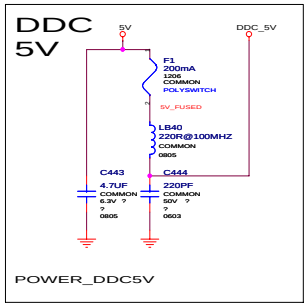
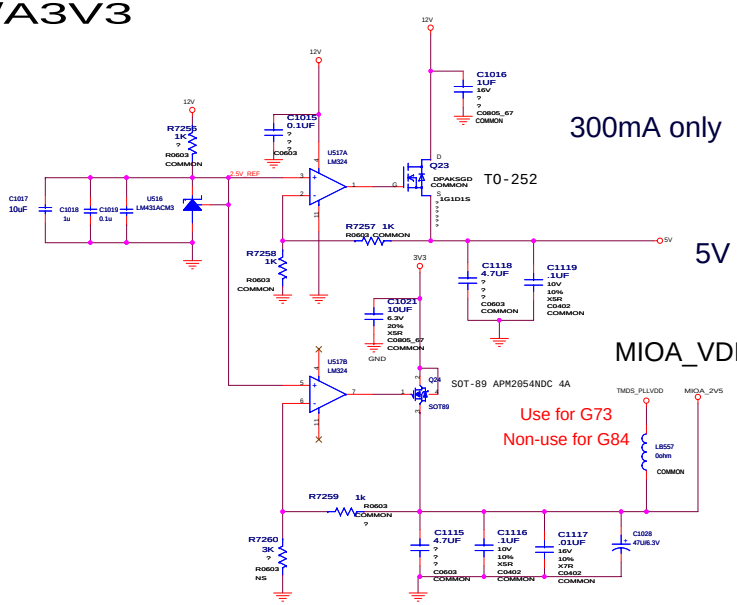
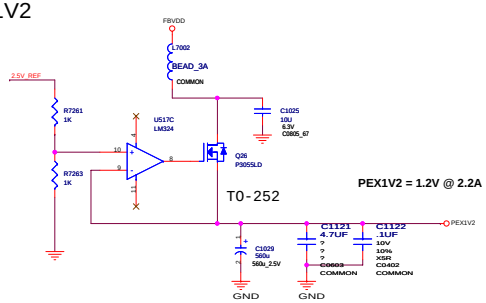
Power Supply TMDS/A3V3

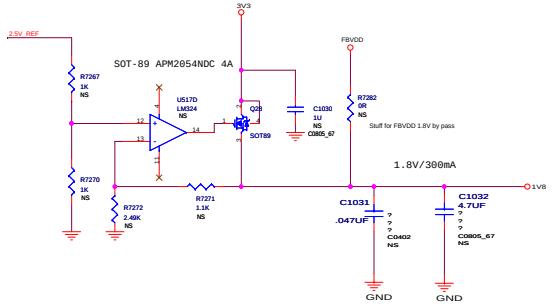




Vout=2.5V

PEX1V2

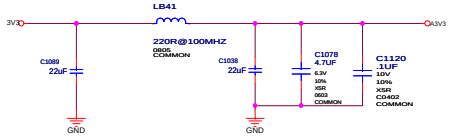


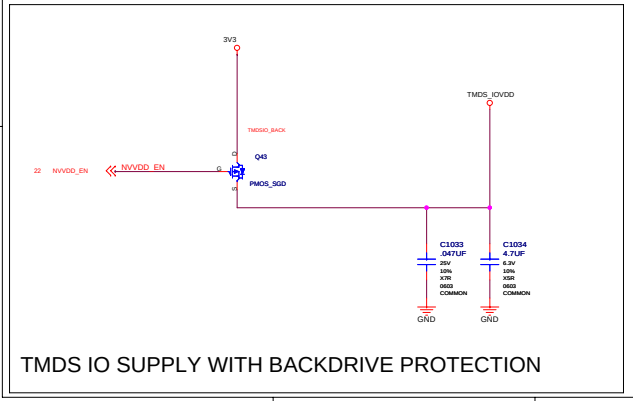


1V8 Supply use for G84 Non-use for G73

Vout=Vref(1+Rtopt/Rbot)

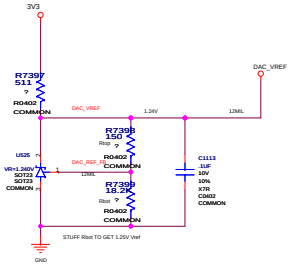
Vout=1.25(1+1.1K/2.49K)=1.8V





TMDS IO SUPPLY WITH BACKDRIVE PROTECTION

DAC V_REFERENCE SUPPLY for G84



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Linear Power		
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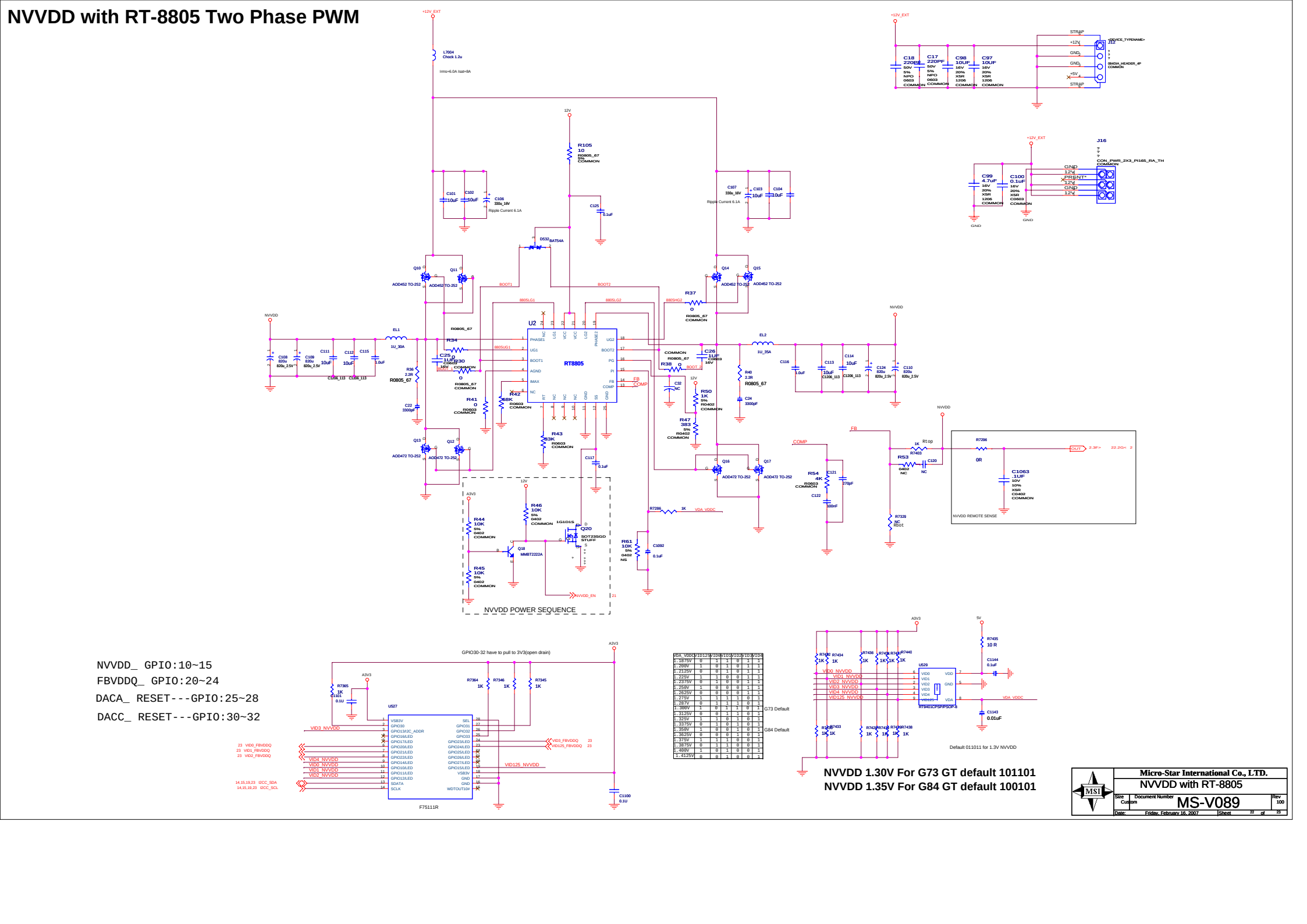
NVVDD with RT-8805 Two Phase PWM



NVDD_ GPIO:10~15

FBVDDQ_ GPIO:20~24

DACA_ RESET---GPIO:25~28

DACC_ RESET---GPIO:30~32

VDA_VDDC	VID125	VID4	VID3	VID2	VID1	VID0
1.1875V	0	1	1	0	1	1
1.2000V	1	0	1	0	1	1
1.2125V	0	0	1	0	1	1
1.225V	1	1	0	0	1	1
1.2375V	0	1	0	0	1	1
1.250V	1	0	0	0	1	1
1.2625V	0	0	0	0	1	1
1.275V	1	1	1	1	0	1
1.287V	0	1	1	1	0	1
1.300V	1	0	1	1	0	1
1.3125V	0	0	1	1	0	1
1.325V	1	1	0	1	0	1
1.3375V	0	1	0	1	0	1
1.350V	1	0	0	1	0	1
1.3625V	0	0	0	1	0	1
1.375V	1	1	1	0	0	1
1.3875V	0	1	1	0	0	1
1.400V	1	0	1	0	0	1
1.4125V	0	0	1	0	0	1

NVVDD 1.30V For G73 GT default 101101

NVVDD 1.35V For G84 GT default 100101

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NVVDD with RT-8805			
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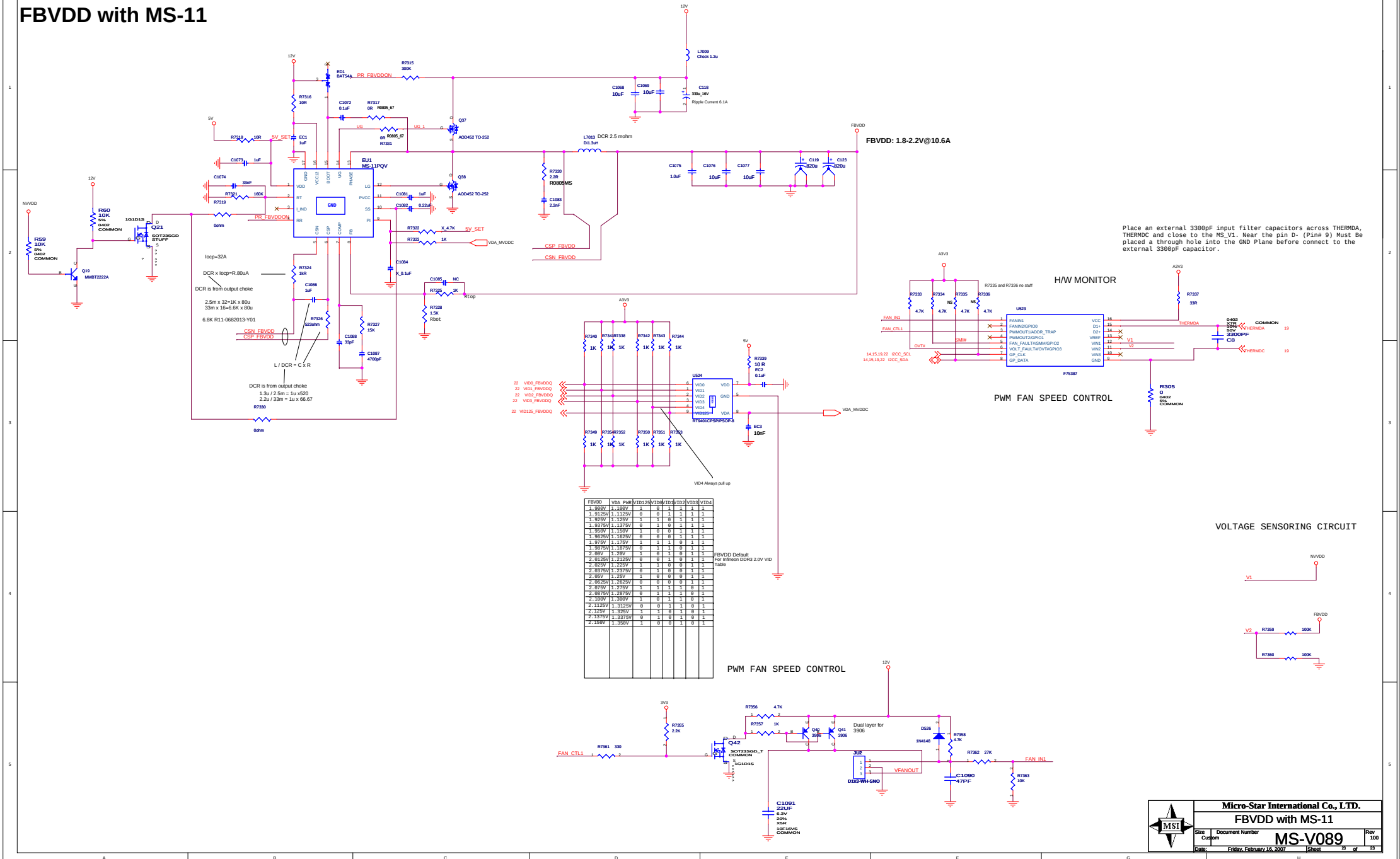
FBVDD with MS-11



FBVDD	VDA_PWR	VID125	VID6	VID1	VID2	VID3	VID4
1.900V	1.100V	1	0	1	1	1	1
1.9125V	1.1125V	0	0	1	1	1	1
1.925V	1.125V	1	1	0	1	1	1
1.9375V	1.1375V	0	1	0	1	1	1
1.950V	1.150V	1	0	0	1	1	1
1.9625V	1.1625V	0	0	0	1	1	1
1.975V	1.175V	1	1	1	0	1	1
1.9875V	1.1875V	0	1	1	0	1	1
2.00V	1.20V	1	0	1	0	1	1
2.0125V	1.2125V	0	0	1	0	1	1
2.025V	1.225V	1	1	0	0	1	1
2.0375V	1.2375V	0	1	0	0	1	1
2.05V	1.25V	1	0	0	0	1	1
2.0625V	1.2625V	0	0	0	0	1	1
2.075V	1.275V	1	1	1	1	0	1
2.0875V	1.2875V	0	1	1	1	0	1
2.100V	1.300V	1	0	1	1	0	1
2.1125V	1.3125V	0	0	1	1	0	1
2.125V	1.325V	1	1	0	1	0	1
2.1375V	1.3375V	0	1	0	1	0	1
2.150V	1.350V	1	0	0	1	0	1

FBVDD Default For Infineon DDR3 2.0V VID Table

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FBVDD with MS-11	
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