

C116, NV18, 8MX16DDR, 128MB, Video IN/OUT, DVI-I, VGA

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HISTORY:

- X00: INITIAL VERSION
- X01 Remove R117, C87, C131, C143 for CKE
- Change C736, C743 to 18pf capacitors.
- Remove C1099 - additional Capacitor for AGPVREFcg
- Changed AGPVREFcg circuit.

C116 Base on P112 to Modify.


1. Change page 4~7 & page 18 Reference.
2. Change J1 foot print from slim type to stand D-SUB.
3. Remove I1394 function.
- ~~4. Page 2, change voltage C75.1 & Q2.E from 3V3 to A3V3.~~
5. Page 8, Add Twin Bios for MSI function.
6. Page 16 ,replace INTERNAL VIDEO CAPTURE CONNECTOR.
7. Page 17 ,ADD C874 & C1098 ALE CAP. (DUAL-LAY)
8. Page 18 , Add H/W Monitor founction for MSI .
9. Page 2 change Q508, Q509 footprint from SOT23 to SOT-6 U200 package.

00A change to version 100.

1. DACA and DACB signal swap.

600-10116-000X-A00

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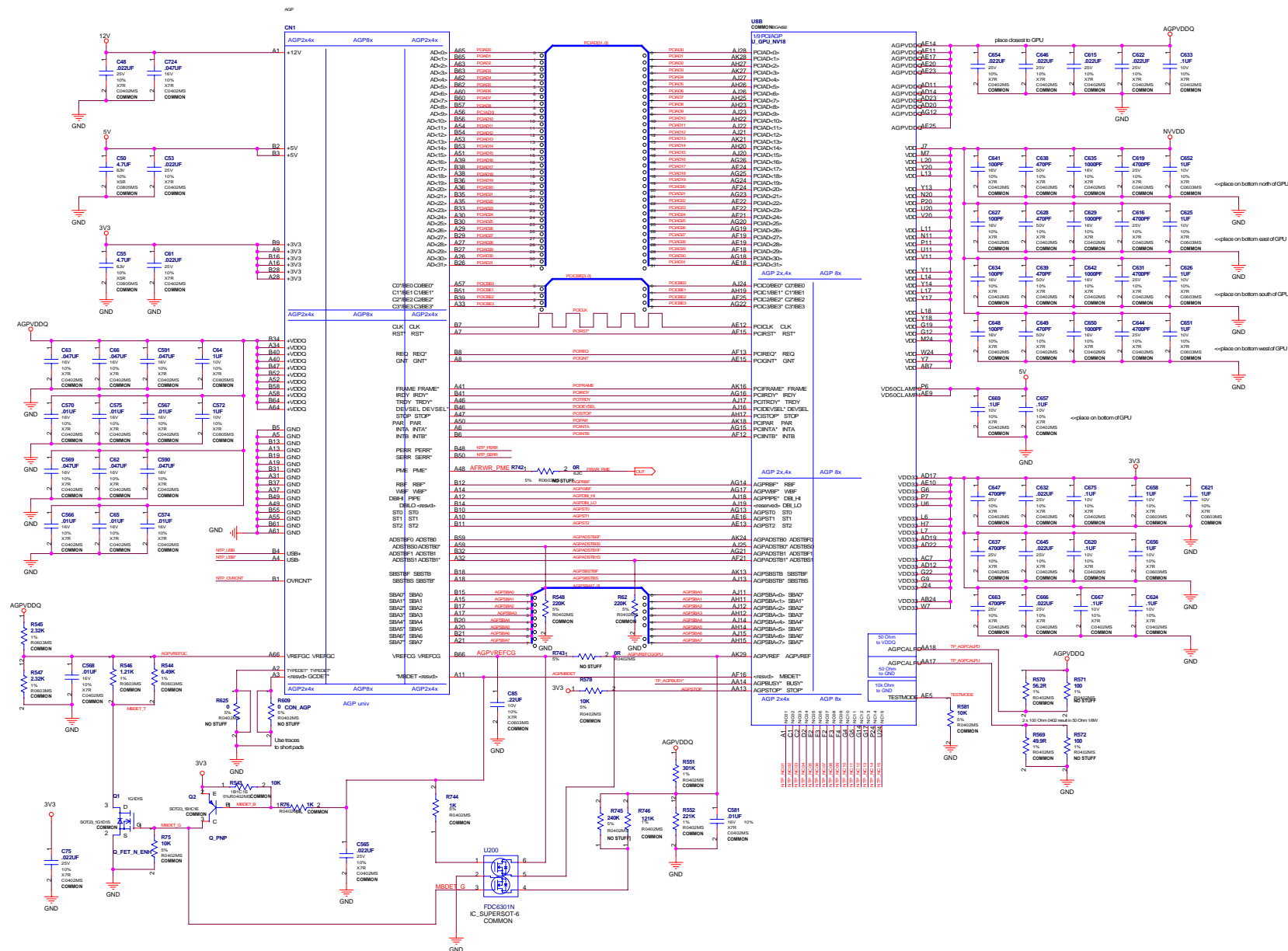
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MS-8891 base on C116 Modify

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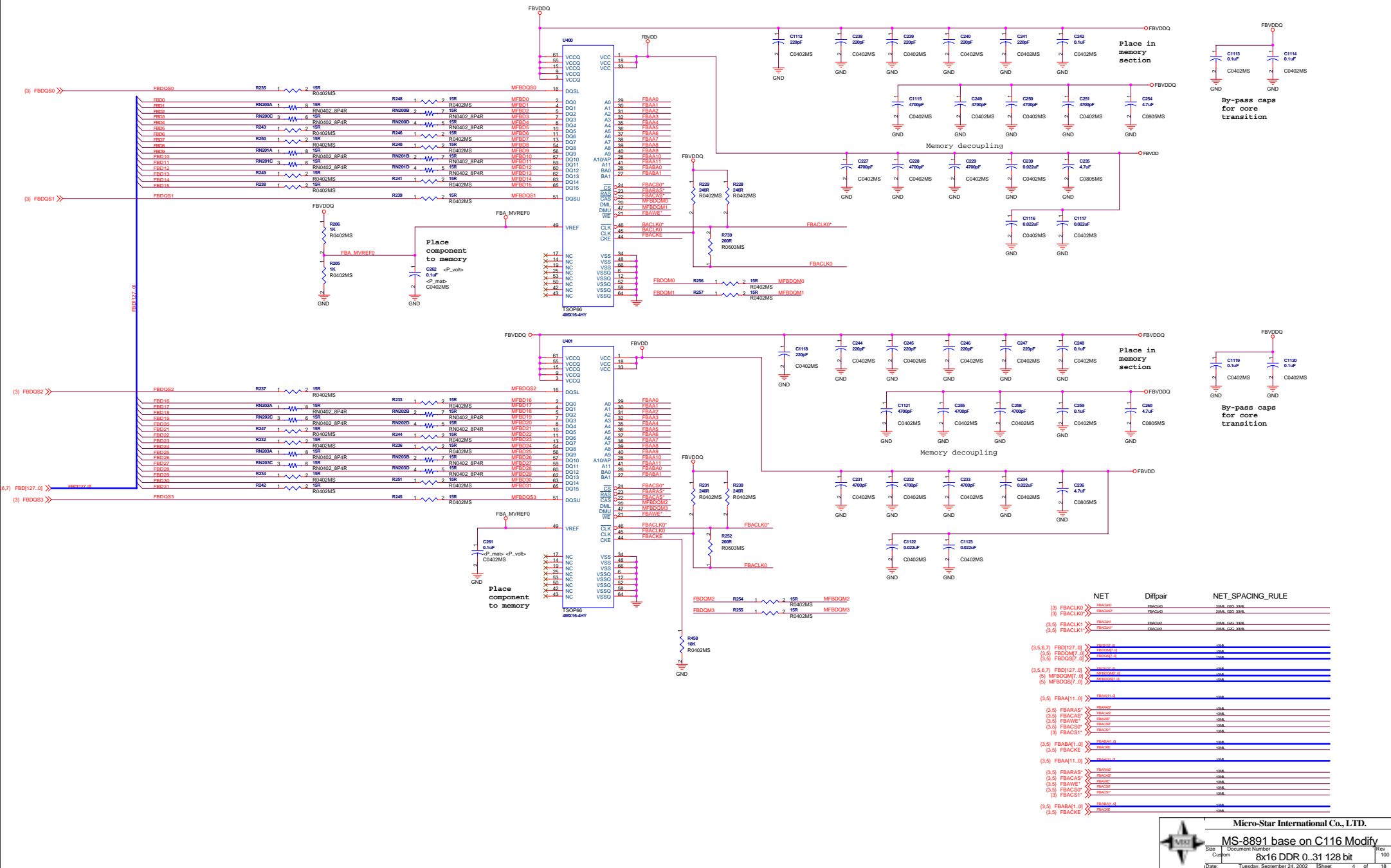
## NV18 AGP SECTION AND AGP CONNECTOR



## AGP spacing rules

PCICB31_0	PCICB31_0	100%
PCICB32_0	PCICB32_0	100%
POICK	POICK	100%
POICKT	POICKT	100%
POICR	POICR	100%
POICGT	POICGT	100%
PCIFRAME	PCIFRAME	100%
PCIRDY	PCIRDY	100%
PCITRDY	PCITRDY	100%
PCISTOP	PCISTOP	100%
PCIDEBSEL	PCIDEBSEL	100%
PCIPAR	PCIPAR	100%
PCINTA	PCINTA	100%
PCINTB	PCINTB	100%
AGPBRB	AGPBRB	100%
AGPBRF	AGPBRF	100%
AGPDBI_HI	AGPDBI_HI	100%
AGPDBI_LO	AGPDBI_LO	100%
AGPDS0	AGPDS0	100%
AGPDS1	AGPDS1	100%
AGPDS2	AGPDS2	100%
AGPDS3	AGPDS3	100%
AGPDS4	AGPDS4	100%
AGPDS5	AGPDS5	100%
AGPDS6	AGPDS6	100%
AGPDS7	AGPDS7	100%
AGPDS8	AGPDS8	100%
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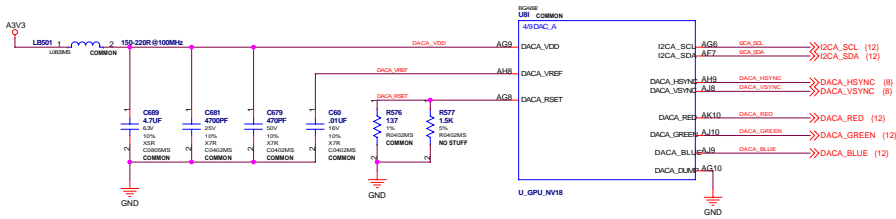




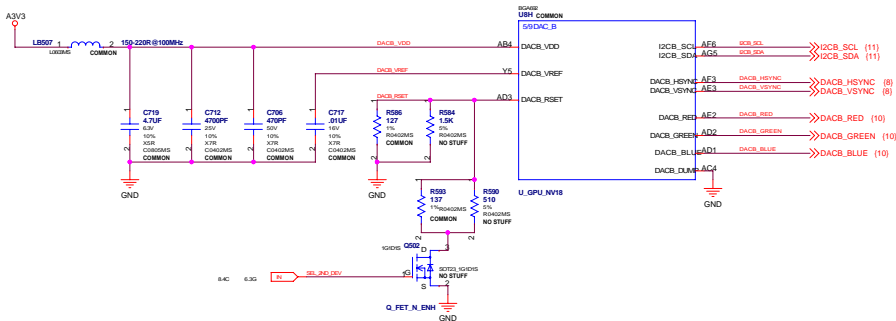


NV18 DAC\_A, DAC\_B, PLL, SYNC AMPL

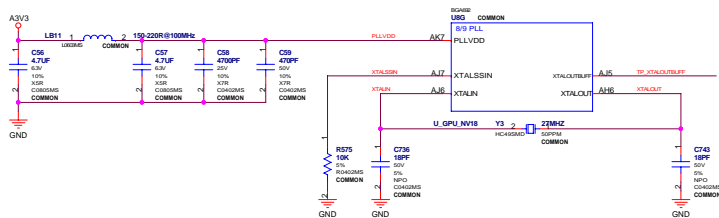
NV18 DAC\_A



NV18 DAC\_B with RSet select



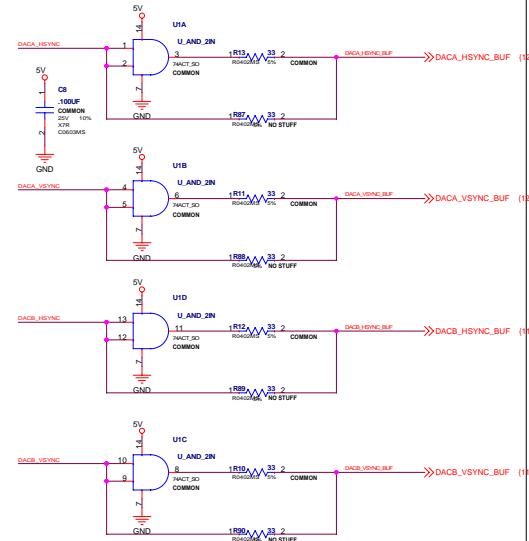
NV18 PLL



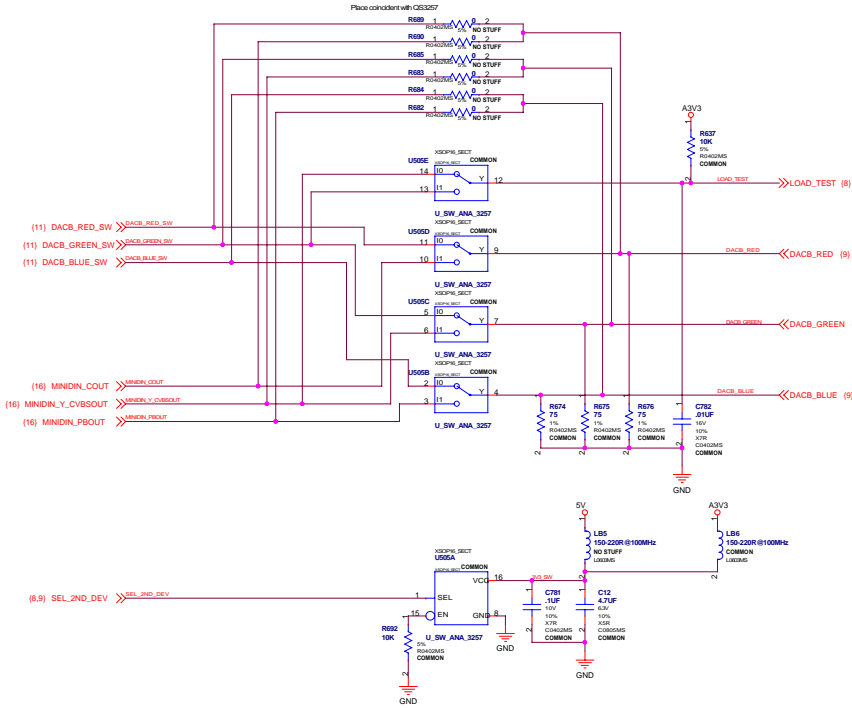
NET	NET_PHYSICAL_TYPE	VOLTAGE
DACA_VDD	DACA_VDD	1.8V
DACA_VREF	DACA_VREF	1.8V
DACA_RSET	DACA_RSET	1.8V
DACB_VDD	DACB_VDD	1.8V
DACB_VREF	DACB_VREF	1.8V
DACB_RSET	DACB_RSET	1.8V
PLLVDD	PLLVDD	1.8V

NET	Diffpair	NET_SPACING_RULE
(12) DACA_RED	DACA_RED	20MIL_20MIL
(12) DACA_GREEN	DACA_GREEN	20MIL_20MIL
(12) DACA_BLUE	DACA_BLUE	20MIL_20MIL
(10) DACB_RED	DACB_RED	20MIL_20MIL
(10) DACB_GREEN	DACB_GREEN	20MIL_20MIL
(10) DACB_BLUE	DACB_BLUE	20MIL_20MIL

SYNC Amplifier

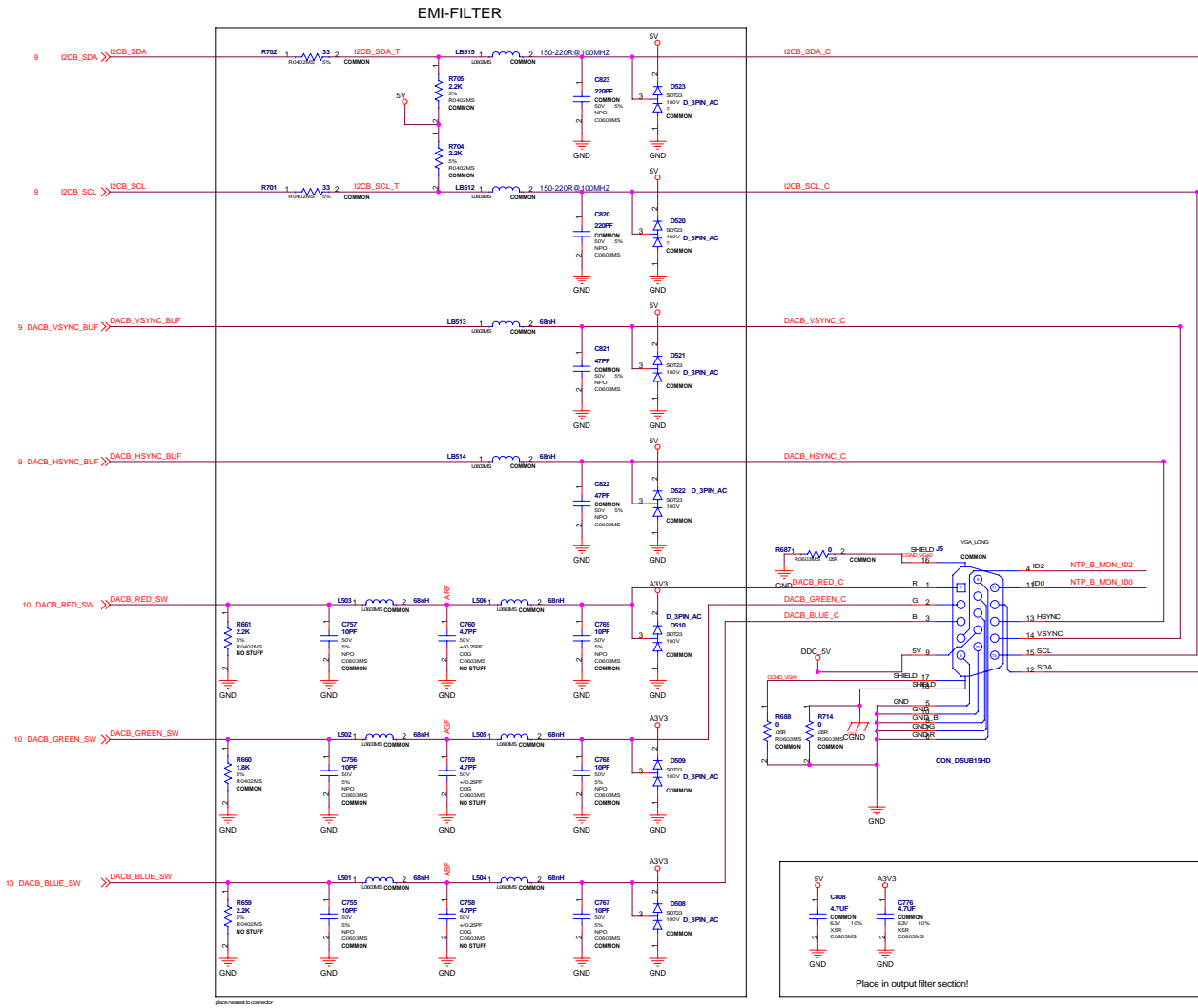


DACB SWITCH BETWEEN VGA OUT AND TV OUT



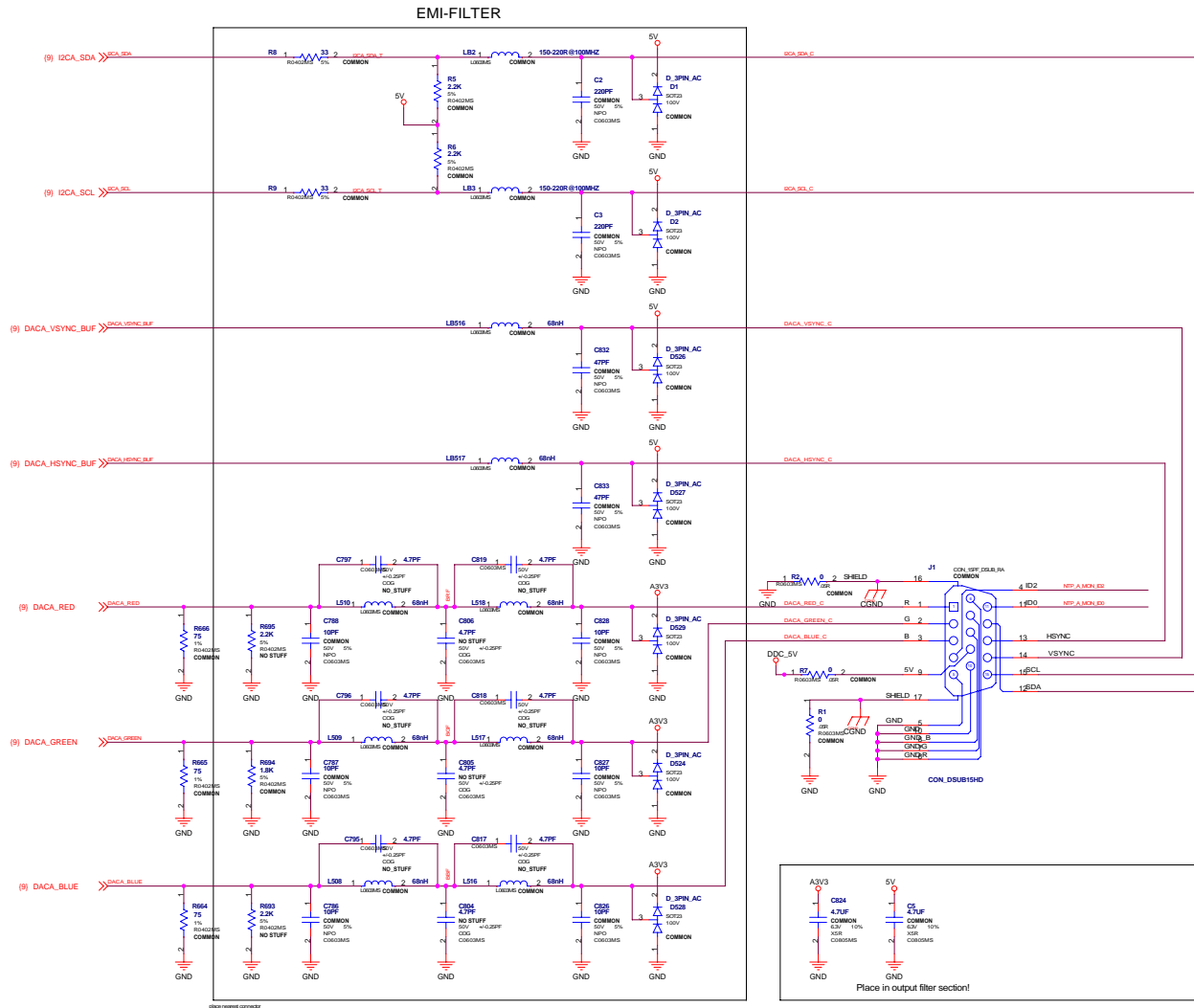
NET	Diffpair	NET_SPACING_RULE
(11) DACB_RED_SW	>>> DACB_RED_SW	20MIL_GST_20MIL
(11) DACB_GREEN_SW	>>> DACB_GREEN_SW	20MIL_GST_20MIL
(11) DACB_BLUE_SW	>>> DACB_BLUE_SW	20MIL_GST_20MIL
(16) MINIDIN_COUT	>>> MINIDIN_COUT	20MIL_GST_20MIL
(16) MINIDIN_Y_CVBSOUT	>>> MINIDIN_Y_CVBSOUT	20MIL_GST_20MIL
(16) MINIDIN_PBOUT	>>> MINIDIN_PBOUT	20MIL_GST_20MIL

DACA output



NET	Diffpair	NET_SPACING_RULE
BRF	BRF	2XLS, 2XLS, 2XLS
BGF	BGF	2XLS, 2XLS, 2XLS
BBF	BBF	2XLS, 2XLS, 2XLS
DACB_RED_C	DACB_RED_C	2XLS, 2XLS, 2XLS
DACB_GREEN_C	DACB_GREEN_C	2XLS, 2XLS, 2XLS
DACB_BLUE_C	DACB_BLUE_C	2XLS, 2XLS, 2XLS

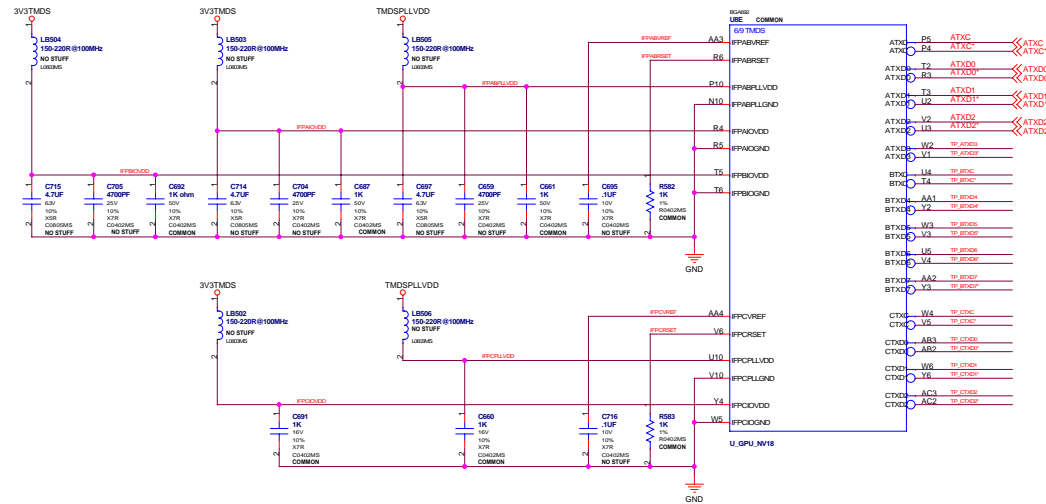
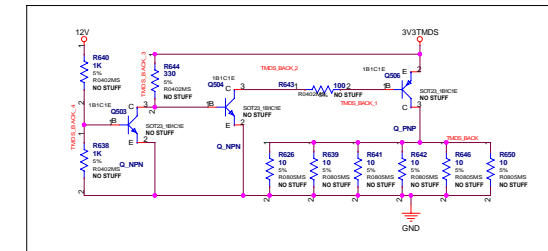
DACB output



	NET	Diffpair	NET_SPACING_RULE
ARF	ARF	2008_C001_2008	
AGF	AGF	2008_C002_2008	
ABF	ABF	2008_C003_2008	
DACA_RED_C	DACA_RED_C	2008_C004_2008	
DACA_GREEN_C	DACA_GREEN_C	2008_C005_2008	
DACA_BLUE_C	DACA_BLUE_C	2008_C006_2008	

## INTERNAL TMDS POWER AND DECOUPLING

NET	NET_PHYSICAL_TYPE	VOLTAGE
IFPABVREF	IFPABVREF	1.00k_1000V
IFPAPMLVDD	IFPAPMLVDD	3.3V
IFPAQVDD	IFPAQVDD	1.00k_1000V
IFPBIOVDD	IFPBIOVDD	3.3V
IFPCVREF	IFPCVREF	1.00k_1000V
IFPCLVDD	IFPCLVDD	3.3V
IFPCVDD	IFPCVDD	1.00k_1000V
IFPCVDD	IFPCVDD	1.00k_1000V
FAN_RETURN	FAN_RETURN	3.3V
TMS0_BACK	TMS0_BACK	3.3V



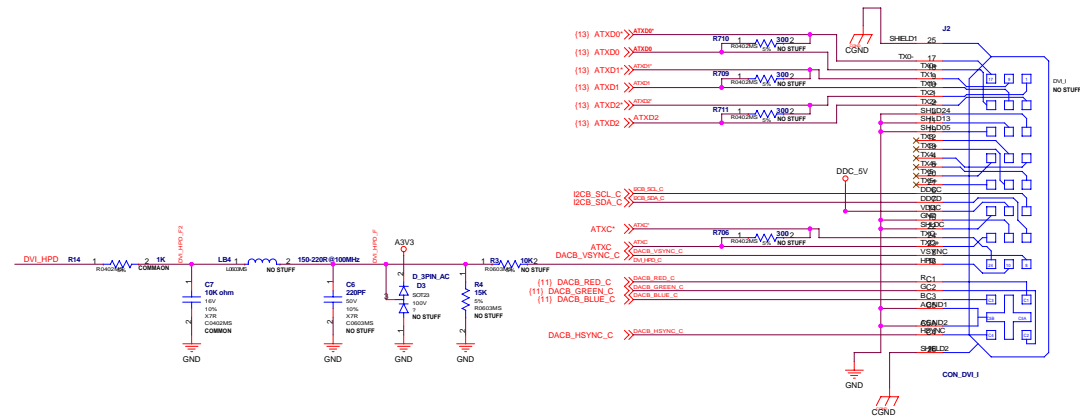
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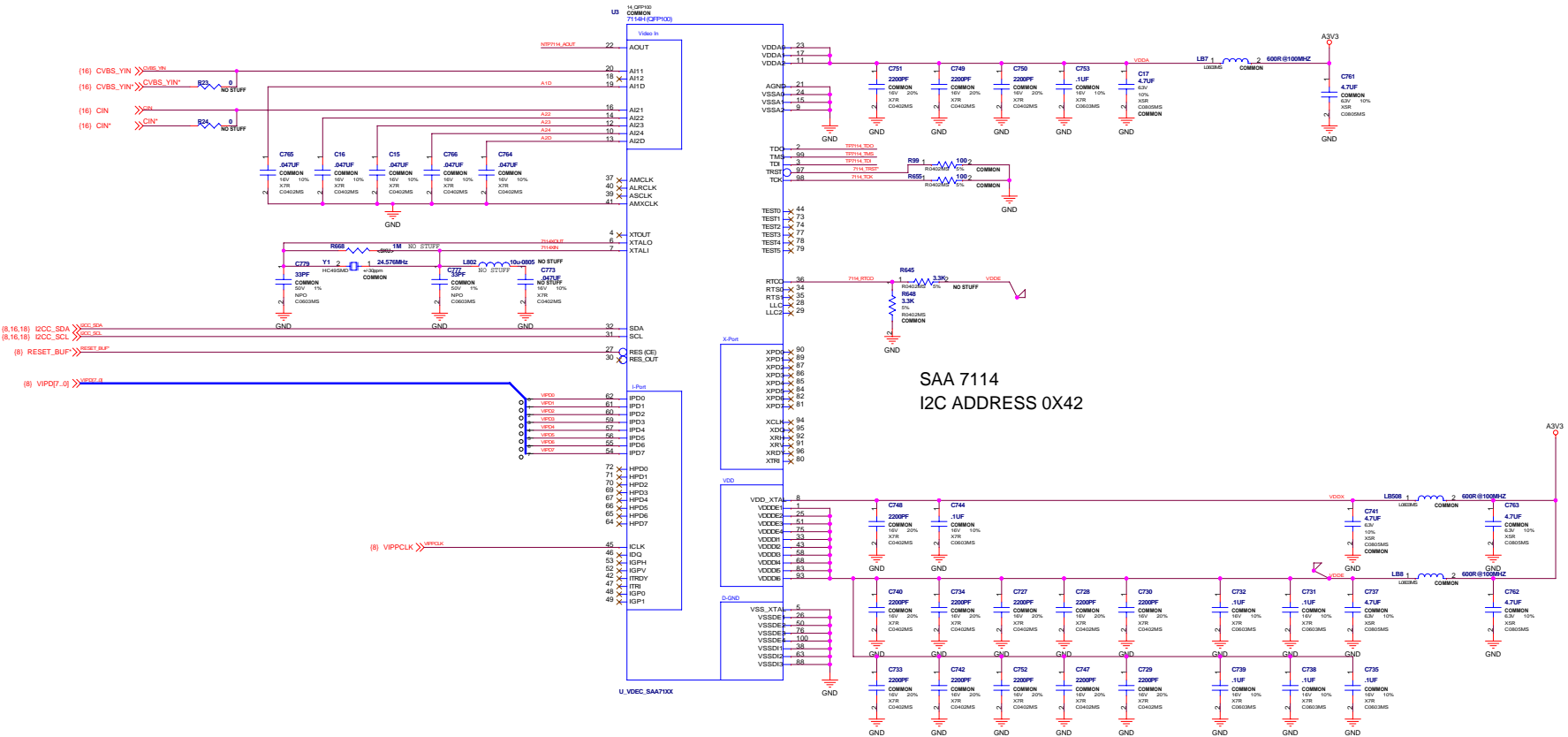
MS-8891 base on C116 Modify			
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Customer	TMDS POWER AND DECOUPLING	100	
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## DVI\_I OUTPUT



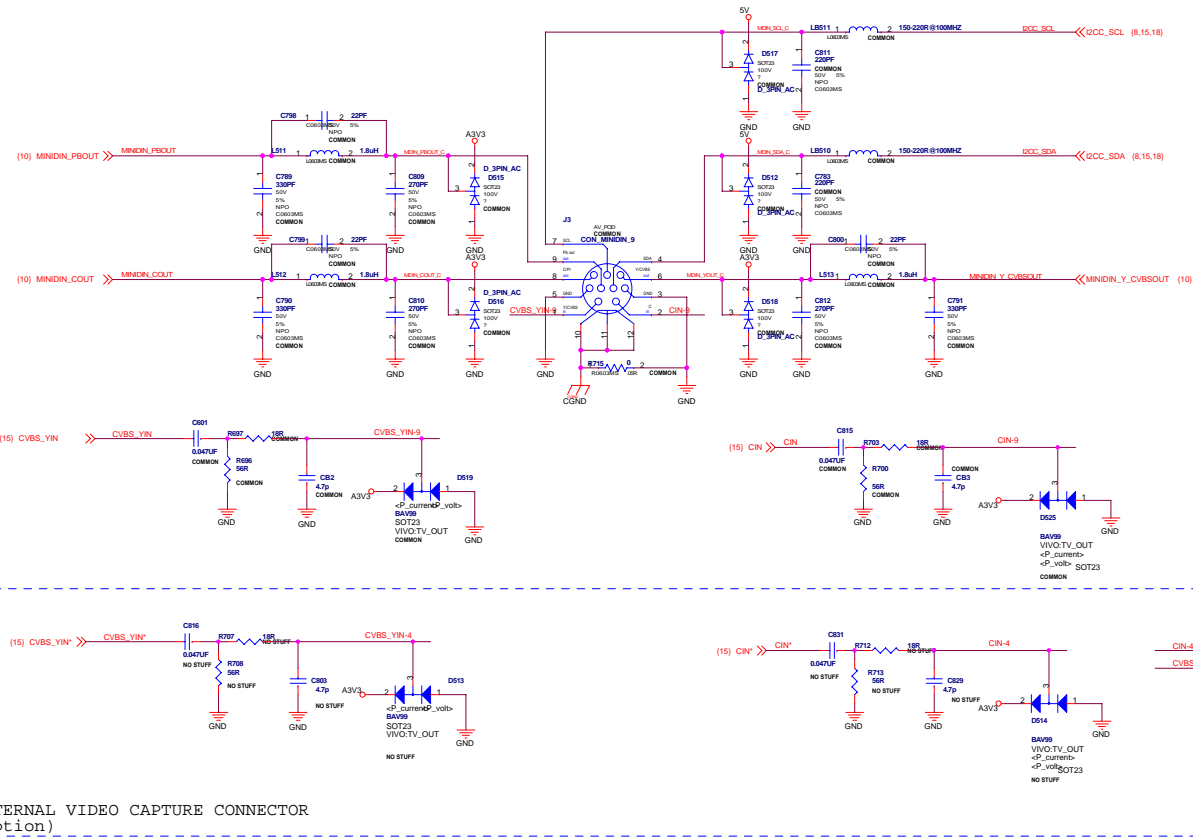
NET	Diffpair	NET_SPACING_RULE
ATX0D	ATX0D	200ML GIG 300L
ATX0D	ATX0Z	200ML GIG 300L
ATX0I	ATX0I	200ML GIG 300L
ATX0I	ATX0I	200ML GIG 300L
ATX0Z	ATX0Z	200ML GIG 300L
ATX0Z	ATX0Z	200ML GIG 300L
ATXC	ATXC	200ML GIG 300L
ATXC	ATXC	200ML GIG 300L

VIDEO CAPTURE



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## VIDEO IN/OUT CONNECTOR

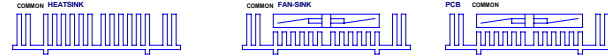


INTERNAL VIDEO CAPTURE CONNECTOR  
(option)

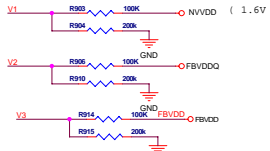




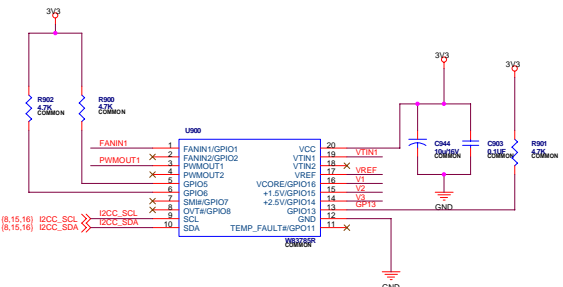
MECHANICS



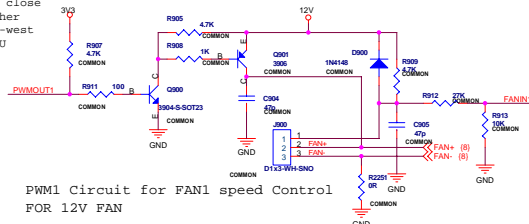
H/W Monitor Funtion



VOLTAGE SENSING CIRCUIT

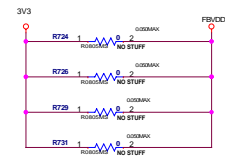


Place close together south-west of GPU

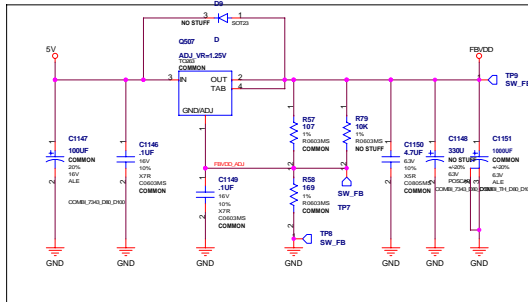


PWM1 Circuit for FAN1 speed Control FOR 12V FAN

NET	NET_PHYSICAL_TYPE	VOLTAGE
3V3	3V3	3.3V
FBVDD	FBVDD	3.3V
5V	5V	5.0V
FBVDD_ADJ	FBVDD_ADJ	3.3V



FBVDD Supply



$$\begin{aligned} \text{FBVDD} &= V_{\text{Ref}} * (1 + R_{\text{bot}} / R_{\text{top}}) \\ 3.315\text{V} &= 1.250\text{V} * (1 + 165 / 100) \\ 3.300\text{V} &= 1.250\text{V} * (1 + 187 / 115) \end{aligned}$$

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Size: Custom

Document Number: MECHANICS

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