

NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF, AGP4X

PCI DEVICE ID 0X0=0X200 FOR NV20.

NVDD SET TO 1.60 FOR -VP CHIP  
FBVDD SET TO: 3.47V  
FBVDDQ SET TO: 2.59V

HISTORY REVISION:

X00: Based on P50-A06  
- See change list in 149- file.  
- Set FBVDDQ=2.59V

P50-A07-X01:  
- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

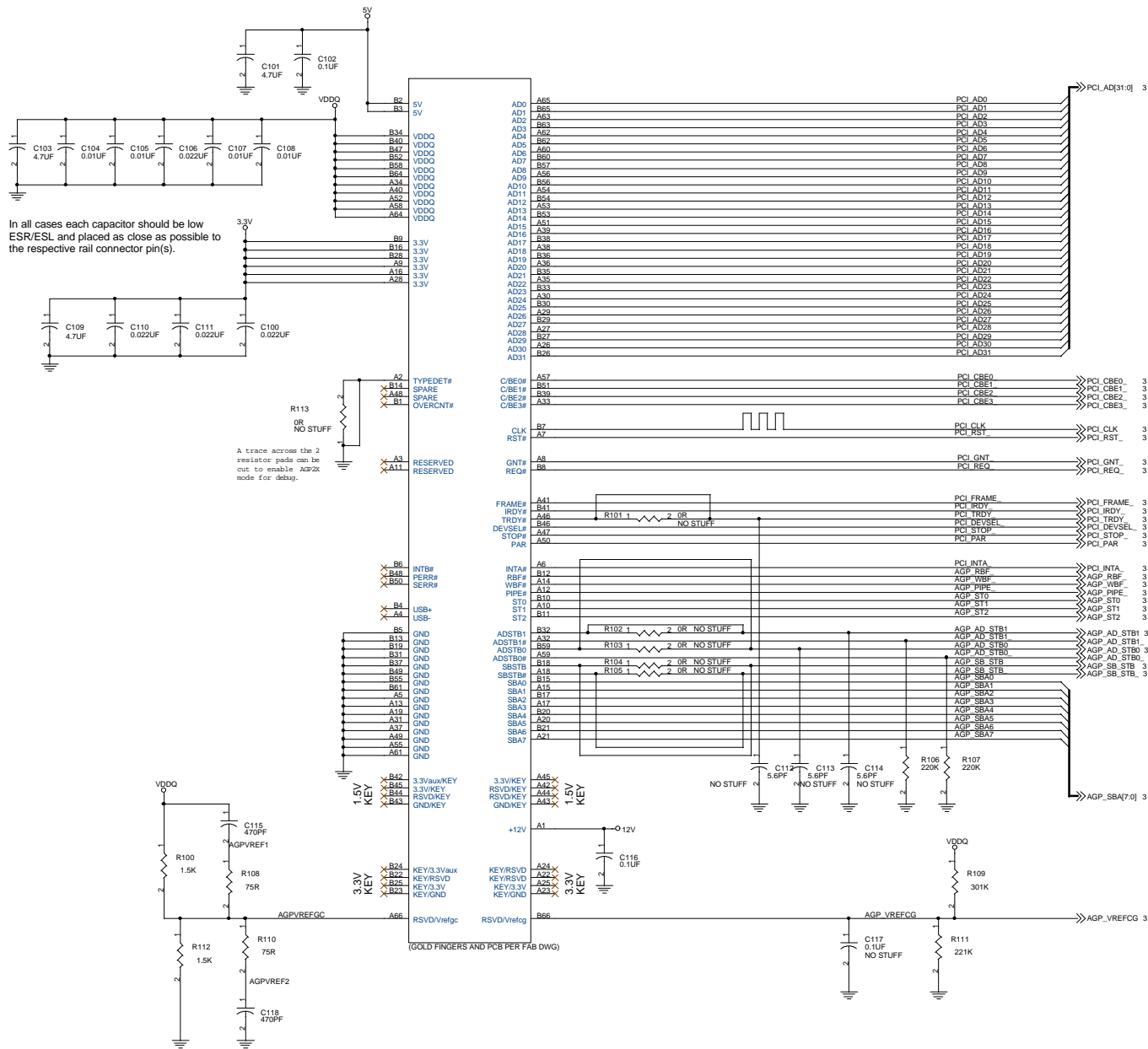
P50-A08:  
X04: - Delay PLL\_VDD to come up after NVVDD.  
X05: - Added 1UF accross R257.  
X06: - Removed X04-5 above, added a switcher generated PLL delay option.  
- SSEN A cap for 2nd SW changed to 1UF.  
- A05 Si, NVVDD=1.52V

P50-A09:  
X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.  
X03: - Added option to pull up power good to 12V

EC01235: - Changed R841 PU to 10K (from 4.7K)

EC01373: - Moved 75 ohm termination closer to filter for noise level reduction.  
Replaced C303,306,309 with 75ohm and no stuffed R208-210.

- 1. GOLD FINGER
- 2. HOST
- 3. DAC/TV/TMDS
- 4. DECOUPING
- 5. STRAPS
- 6. CRT
- 7. FBA/FBB
- 8. DECOUPING
- 9. 2\*32 DDR
- 10. 2\*32 DDR
- 11. 1M FLASH ROM 3.3V
- 12. TV PH/7108
- 13. POWER
- 14. HARDWARE MONITOR



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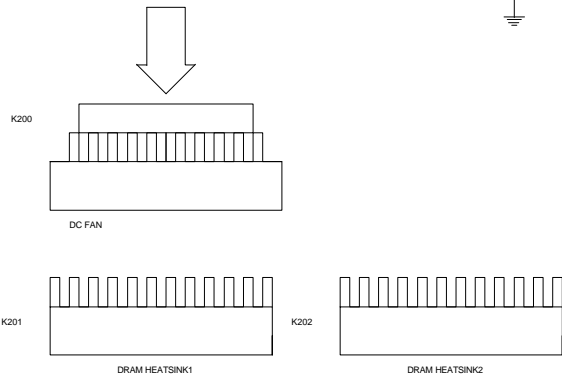
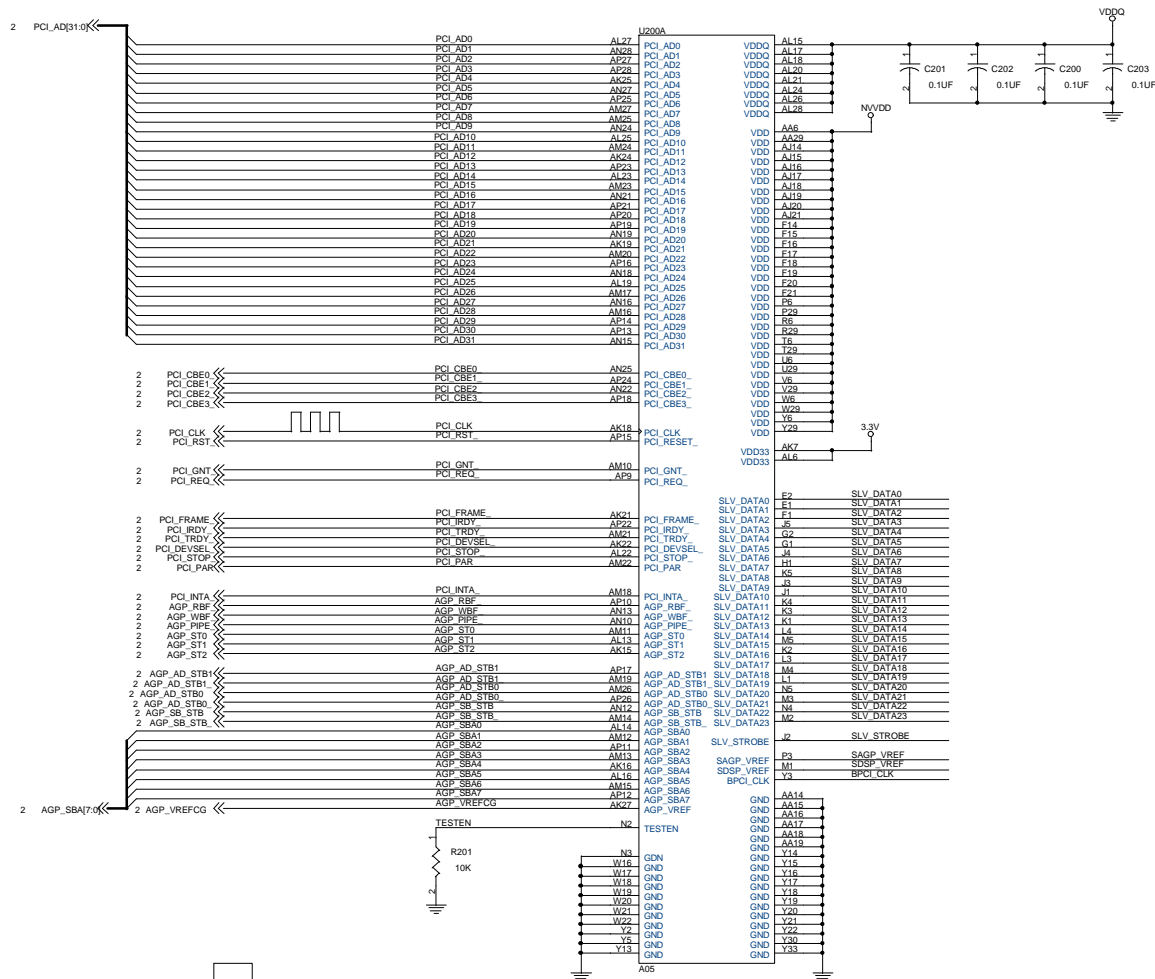
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BUS I/O

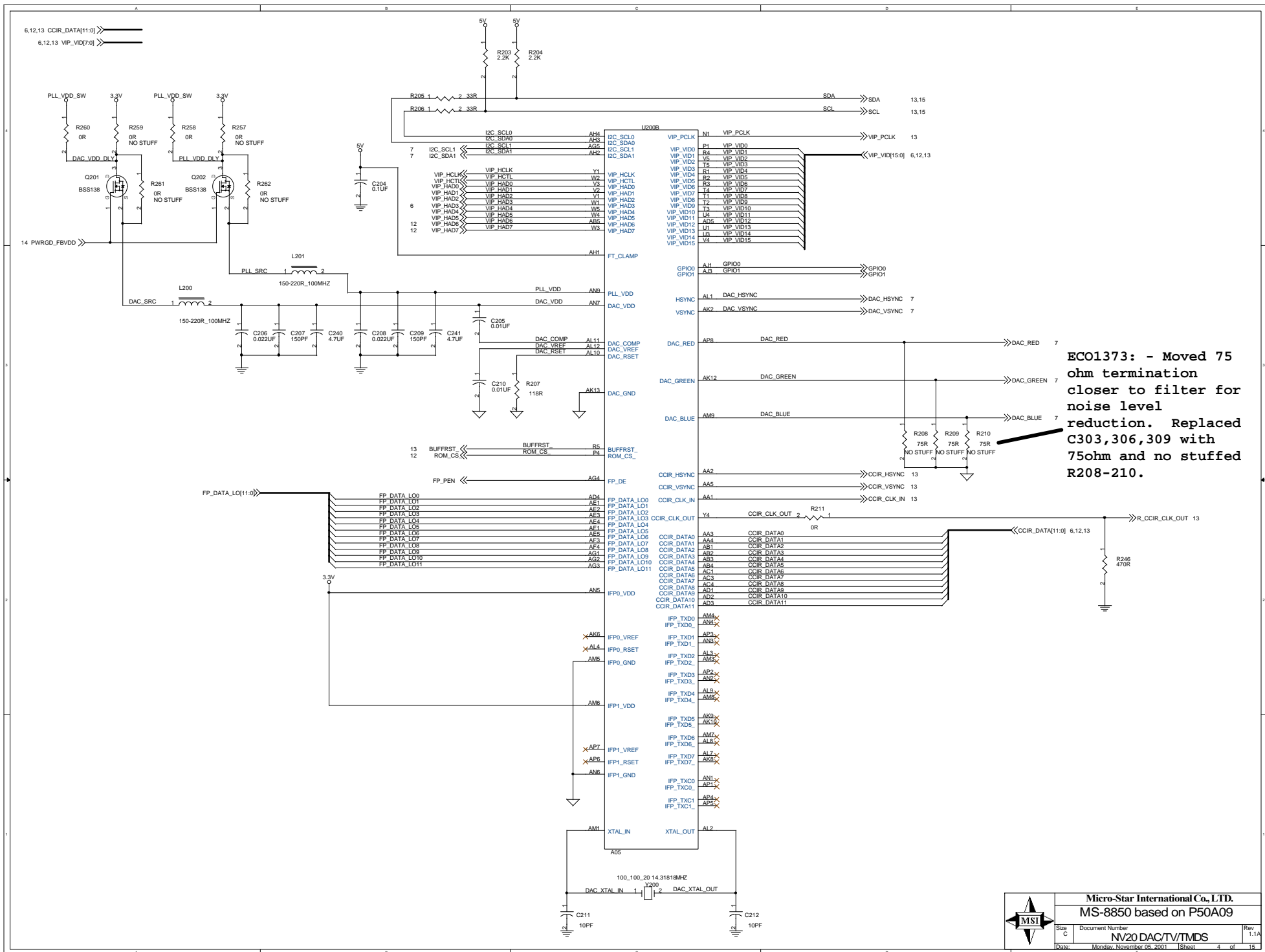
Rev 1.1A

Date: Monday, November 05, 2001 [Sheet 2 of 15]



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Size C Document Number NV20-HOST Rev 1.1A  
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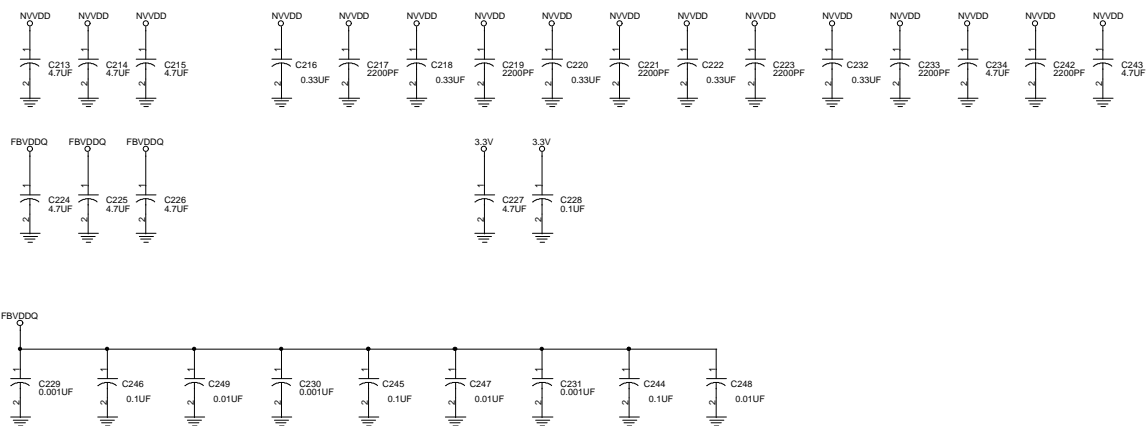


Use thick (non-impedance controlled) traces on XTALIN/OUT

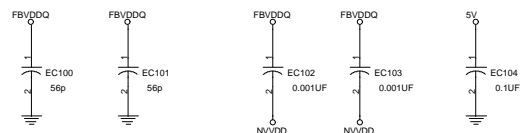


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Size C Document Number NV20 DAC/TV/TMDS Rev 1.1A  
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#### For EMI Solution



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4,12,13 CCIR\_DATA[11:0] >>  
4,12,13 VIP\_VID[15:0] >>  
4 FP\_DATA\_LO[11:0] >>

4 VIP\_HAD0 >>  
4 VIP\_HAD1 >>  
4 VIP\_HAD2 >>  
4 VIP\_HAD3 >>  
4 VIP\_HAD4 >>  
4 VIP\_HAD5 >>  
4,12 VIP\_HAD6 >>  
4,12 VIP\_HAD7 >>



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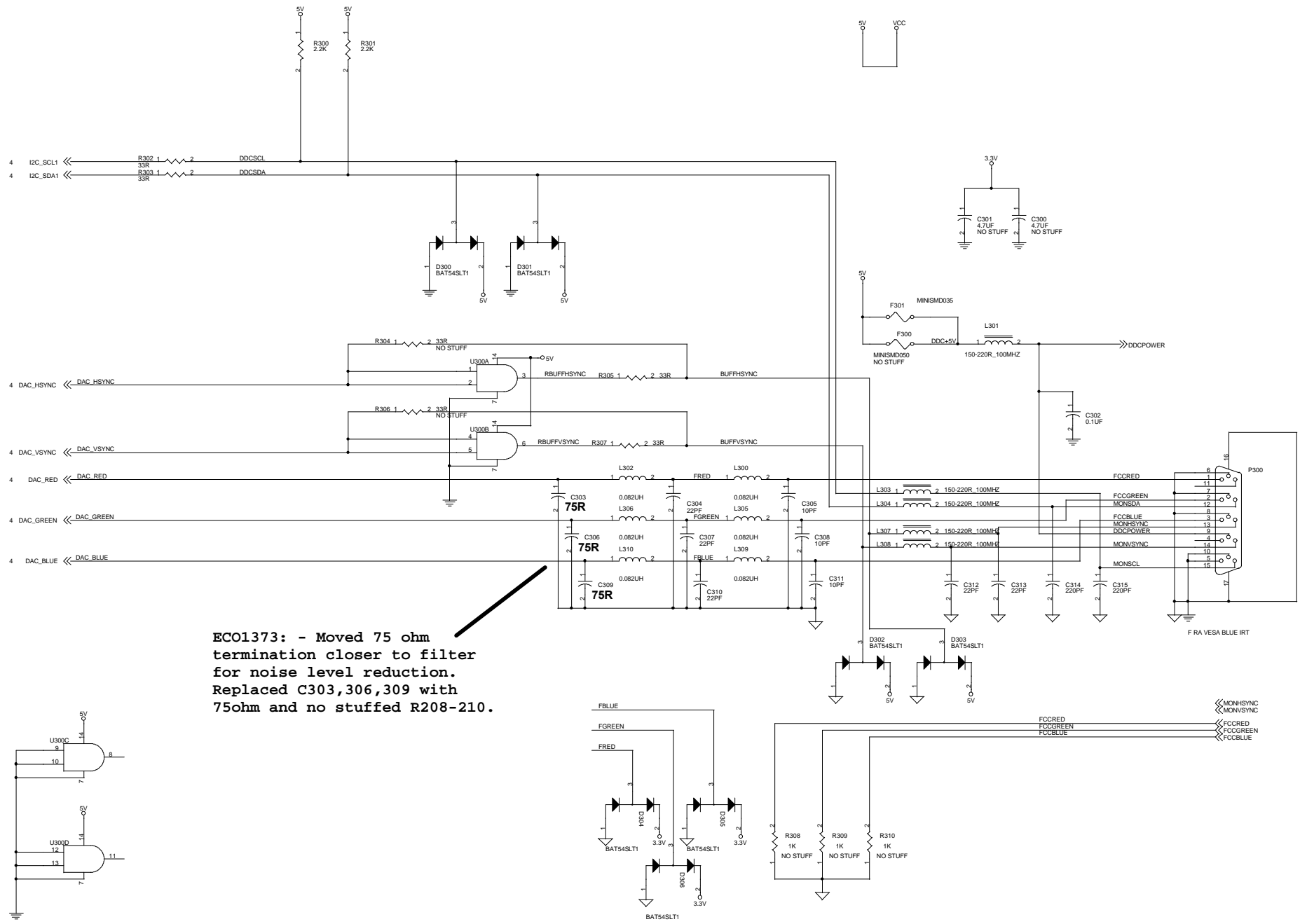
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Document Number

NV20 HOST STRAPS

Rev  
1.1A

Date: Monday, November 05, 2001 1 Sheet 6 of 15

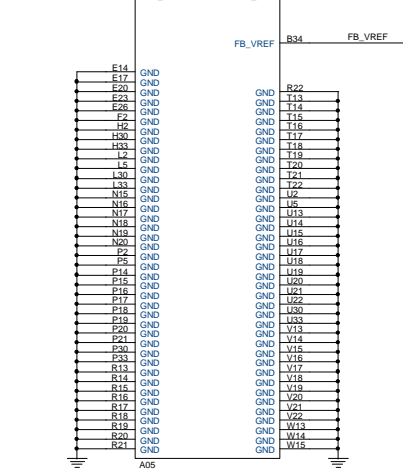


EC01373: - Moved 75 ohm termination closer to filter for noise level reduction. Replaced C303,306,309 with 75ohm and no stuffed R208-210.

FBD_DATA0_R16	FBD_DATA0	FBC_DATA0	A34	FBC_DATA0
FBD_DATA1_A16	FBD_DATA1	FBC_DATA1	B33	FBC_DATA1
FBD_DATA2_E15	FBD_DATA2	FBC_DATA2	A33	FBC_DATA2
FBD_DATA3_C15	FBD_DATA3	FBC_DATA3	A32	FBC_DATA3
FBD_DATA4_D14	FBD_DATA4	FBC_DATA4	B31	FBC_DATA4
FBD_DATA5_C12	FBD_DATA5	FBC_DATA5	A32	FBC_DATA5
FBD_DATA6_D12	FBD_DATA6	FBC_DATA6	B30	FBC_DATA6
FBD_DATA7_A14	FBD_DATA7	FBC_DATA7	A29	FBC_DATA7
FBD_DATA8_C13	FBD_DATA8	FBC_DATA8	C29	FBC_DATA8
FBD_DATA9_B13	FBD_DATA9	FBC_DATA9	D28	FBC_DATA9
FBD_DATA10_A13	FBD_DATA10	FBC_DATA10	B28	FBC_DATA10
FBD_DATA11_A11	FBD_DATA11	FBC_DATA11	D27	FBC_DATA11
FBD_DATA12_A12	FBD_DATA12	FBC_DATA12	B27	FBC_DATA12
FBD_DATA13_A11	FBD_DATA13	FBC_DATA13	D27	FBC_DATA13
FBD_DATA14_C11	FBD_DATA14	FBC_DATA14	B27	FBC_DATA14
FBD_DATA15_D11	FBD_DATA15	FBC_DATA15	D26	FBC_DATA15
FBD_DATA16_B11	FBD_DATA16	FBC_DATA16	A27	FBC_DATA16
FBD_DATA17_A4	FBD_DATA17	FBC_DATA17	A21	FBC_DATA17
FBD_DATA18_C4	FBD_DATA18	FBC_DATA18	B20	FBC_DATA18
FBD_DATA19_A2	FBD_DATA19	FBC_DATA19	C20	FBC_DATA19
FBD_DATA20_D3	FBD_DATA20	FBC_DATA20	D19	FBC_DATA20
FBD_DATA21_C3	FBD_DATA21	FBC_DATA21	C19	FBC_DATA21
FBD_DATA22_D3	FBD_DATA22	FBC_DATA22	B19	FBC_DATA22
FBD_DATA23_C2	FBD_DATA23	FBC_DATA23	D18	FBC_DATA23
FBD_DATA24_D2	FBD_DATA24	FBC_DATA24	C18	FBC_DATA24
FBD_DATA25_E3	FBD_DATA25	FBC_DATA25	A18	FBC_DATA25
FBD_DATA26_G4	FBD_DATA26	FBC_DATA26	D18	FBC_DATA26
FBD_DATA27_G4	FBD_DATA27	FBC_DATA27	C18	FBC_DATA27
FBD_DATA28_G3	FBD_DATA28	FBC_DATA28	C17	FBC_DATA28
FBD_DATA29_H6	FBD_DATA29	FBC_DATA29	A17	FBC_DATA29
FBD_DATA30_H3	FBD_DATA30	FBC_DATA30	C16	FBC_DATA30
FBD_DATA31_H4	FBD_DATA31	FBC_DATA31	C16	FBC_DATA31

FBD_ADR0_D13	FBD_ADR0	FBC_ADR0	D26	FBC_ADR0
FBD_ADR1_B10	FBD_ADR1	FBC_ADR1	C26	FBC_ADR1
FBD_ADR2_C10	FBD_ADR2	FBC_ADR2	A26	FBC_ADR2
FBD_ADR3_D10	FBD_ADR3	FBC_ADR3	D25	FBC_ADR3
FBD_ADR4_A10	FBD_ADR4	FBC_ADR4	D23	FBC_ADR4
FBD_ADR5_D8	FBD_ADR5	FBC_ADR5	C23	FBC_ADR5
FBD_ADR6_C8	FBD_ADR6	FBC_ADR6	A23	FBC_ADR6
FBD_ADR7_A8	FBD_ADR7	FBC_ADR7	D22	FBC_ADR7
FBD_ADR8_D7	FBD_ADR8	FBC_ADR8	E24	FBC_ADR8
FBD_ADR9_C7	FBD_ADR9	FBC_ADR9	E21	FBC_ADR9
FBD_ADR10_B6	FBD_ADR10	FBC_ADR10	D21	FBC_ADR10
FBD_ADR11_A6	FBD_ADR11	FBC_ADR11	B19	FBC_ADR11
FBD_ADR12_H4	FBD_ADR12	FBC_ADR12	C21	FBC_ADR12
FBD_ADR13_A5	FBD_ADR13	FBC_ADR13	C21	FBC_ADR13

FBD_DQM0_B15	FBD_DQM0	FBC_DQM0	C31	FBC_DQM0
FBD_DQM1_E13	FBD_DQM1	FBC_DQM1	A28	FBC_DQM1
FBD_DQM2_A13	FBD_DQM2	FBC_DQM2	E19	FBC_DQM2
FBD_DQM3_C1	FBD_DQM3	FBC_DQM3	B18	FBC_DQM3
FBD_DQ00_A15	FBD_DQ00	FBC_DQ00	A31	FBC_DQ00
FBD_DQ01_B17	FBD_DQ01	FBC_DQ01	E27	FBC_DQ01
FBD_DQ02_D17	FBD_DQ02	FBC_DQ02	A20	FBC_DQ02
FBD_DQ03_D1	FBD_DQ03	FBC_DQ03	D17	FBC_DQ03
FBD_RAS_B9	FBD_RAS	FBC_RAS	C24	FBC_RAS
FBD_CAS_E10	FBD_CAS	FBC_CAS	D24	FBC_CAS
FBD_WE_E9	FBD_WE	FBC_WE	B24	FBC_WE
FBD_CS0_A9	FBD_CS0	FBC_CS0	E22	FBC_CS0
FBD_CS1_D17	FBD_CS1	FBC_CS1	A24	FBC_CS1
FBD_CLK0_A7	FBD_CLK0	FBC_CLK0	B22	FBC_CLK0
FBD_CLK0B_A7	FBD_CLK0B	FBC_CLK0B	C22	FBC_CLK0B
FBD_CLK1_D9	FBD_CLK1	FBC_CLK1	A25	FBC_CLK1
FBD_CLK1B_C8	FBD_CLK1B	FBC_CLK1B	B25	FBC_CLK1B
FBD_CKE_C8	FBD_CKE	FBC_CKE	A22	FBC_CKE



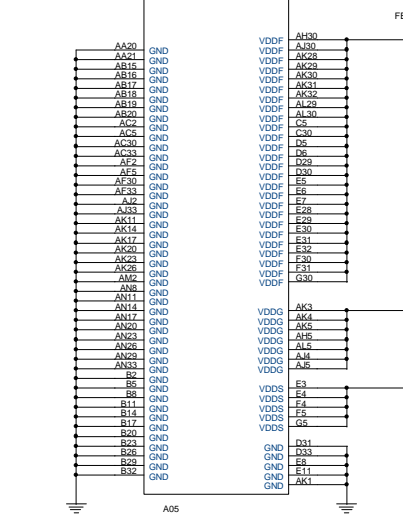
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FBB_DATA1_W33	FBB_DATA1	FBA_DATA1	AF29	FBA_DATA1
FBB_DATA2_W34	FBB_DATA2	FBA_DATA2	AM29	FBA_DATA2
FBB_DATA3_W30	FBB_DATA3	FBA_DATA3	AF30	FBA_DATA3
FBB_DATA4_W30	FBB_DATA4	FBA_DATA4	AF31	FBA_DATA4
FBB_DATA5_W34	FBB_DATA5	FBA_DATA5	AM31	FBA_DATA5
FBB_DATA6_W34	FBB_DATA6	FBA_DATA6	AF32	FBA_DATA6
FBB_DATA7_W31	FBB_DATA7	FBA_DATA7	AM32	FBA_DATA7
FBB_DATA8_W32	FBB_DATA8	FBA_DATA8	AF33	FBA_DATA8
FBB_DATA9_W34	FBB_DATA9	FBA_DATA9	AM33	FBA_DATA9
FBB_DATA10_W31	FBB_DATA10	FBA_DATA10	AF34	FBA_DATA10
FBB_DATA11_W31	FBB_DATA11	FBA_DATA11	AM34	FBA_DATA11
FBB_DATA12_W34	FBB_DATA12	FBA_DATA12	AF35	FBA_DATA12
FBB_DATA13_W33	FBB_DATA13	FBA_DATA13	AM35	FBA_DATA13
FBB_DATA14_W32	FBB_DATA14	FBA_DATA14	AF36	FBA_DATA14
FBB_DATA15_W30	FBB_DATA15	FBA_DATA15	AM36	FBA_DATA15
FBB_DATA16_W30	FBB_DATA16	FBA_DATA16	AF37	FBA_DATA16
FBB_DATA17_W31	FBB_DATA17	FBA_DATA17	AM37	FBA_DATA17
FBB_DATA18_W31	FBB_DATA18	FBA_DATA18	AF38	FBA_DATA18
FBB_DATA19_W32	FBB_DATA19	FBA_DATA19	AM38	FBA_DATA19
FBB_DATA20_W34	FBB_DATA20	FBA_DATA20	AF39	FBA_DATA20
FBB_DATA21_W32	FBB_DATA21	FBA_DATA21	AM39	FBA_DATA21
FBB_DATA22_W33	FBB_DATA22	FBA_DATA22	AF40	FBA_DATA22
FBB_DATA23_W31	FBB_DATA23	FBA_DATA23	AM40	FBA_DATA23
FBB_DATA24_W32	FBB_DATA24	FBA_DATA24	AF41	FBA_DATA24
FBB_DATA25_W33	FBB_DATA25	FBA_DATA25	AM41	FBA_DATA25
FBB_DATA26_W34	FBB_DATA26	FBA_DATA26	AF42	FBA_DATA26
FBB_DATA27_W33	FBB_DATA27	FBA_DATA27	AM42	FBA_DATA27
FBB_DATA28_W34	FBB_DATA28	FBA_DATA28	AF43	FBA_DATA28
FBB_DATA29_W32	FBB_DATA29	FBA_DATA29	AM43	FBA_DATA29
FBB_DATA30_W33	FBB_DATA30	FBA_DATA30	AF44	FBA_DATA30
FBB_DATA31_W34	FBB_DATA31	FBA_DATA31	AM44	FBA_DATA31

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FBB_ADR2_P31	FBB_ADR2	FBA_ADR2	AL33	FBA_ADR2
FBB_ADR3_P32	FBB_ADR3	FBA_ADR3	AJ31	FBA_ADR3
FBB_ADR4_L34	FBB_ADR4	FBA_ADR4	AK33	FBA_ADR4
FBB_ADR5_L34	FBB_ADR5	FBA_ADR5	AG33	FBA_ADR5
FBB_ADR6_L32	FBB_ADR6	FBA_ADR6	AG32	FBA_ADR6
FBB_ADR7_R31	FBB_ADR7	FBA_ADR7	AK31	FBA_ADR7
FBB_ADR8_K34	FBB_ADR8	FBA_ADR8	AE31	FBA_ADR8
FBB_ADR9_N30	FBB_ADR9	FBA_ADR9	AE32	FBA_ADR9
FBB_ADR10_P34	FBB_ADR10	FBA_ADR10	AE33	FBA_ADR10
FBB_ADR11_J33	FBB_ADR11	FBA_ADR11	AE32	FBA_ADR11
FBB_ADR12_J32	FBB_ADR12	FBA_ADR12	AE33	FBA_ADR12
FBB_ADR13_M30	FBB_ADR13	FBA_ADR13	AD32	FBA_ADR13

FBB_DQM0_V31	FBB_DQM0	FBA_DQM0	AN30	FBA_DQM0
FBB_DQM1_V33	FBB_DQM1	FBA_DQM1	AM32	FBA_DQM1
FBB_DQM2_J30	FBB_DQM2	FBA_DQM2	AC31	FBA_DQM2
FBB_DQM3_E34	FBB_DQM3	FBA_DQM3	AS33	FBA_DQM3

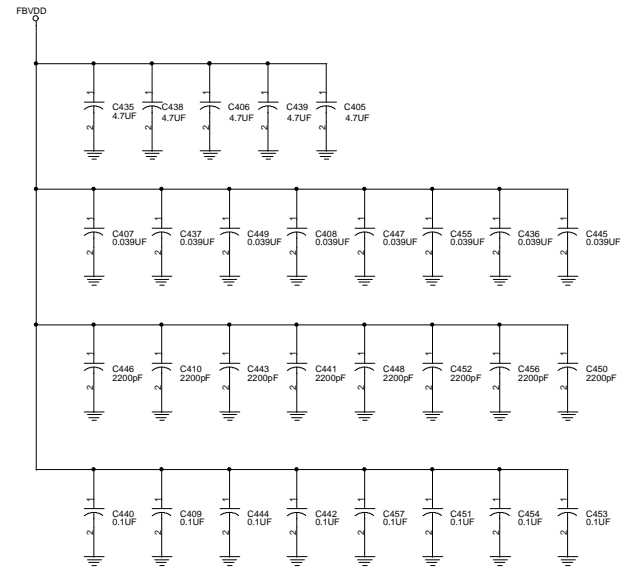
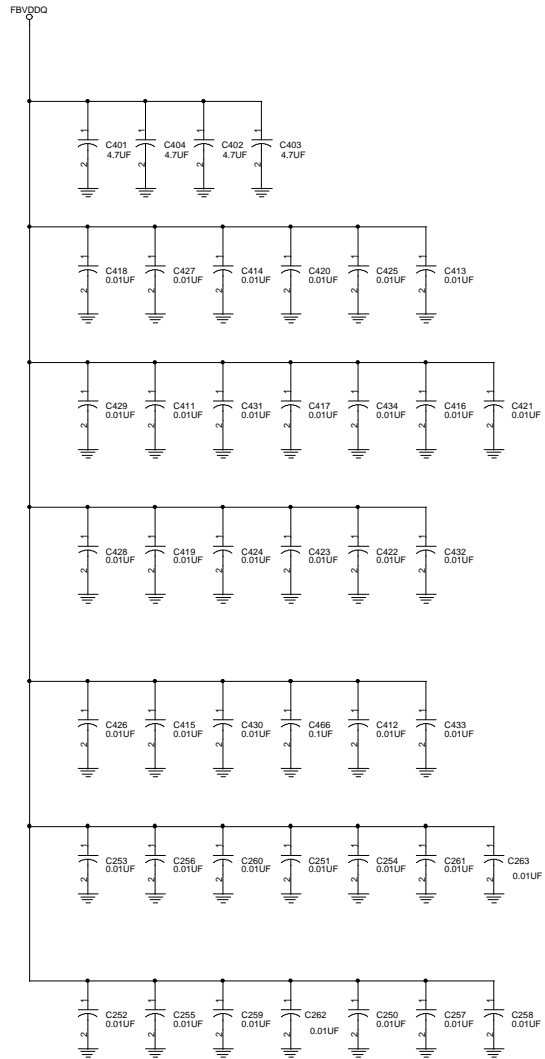
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FBB_DQ01_T32	FBB_DQ01	FBA_DQ01	AL32	FBA_DQ01
FBB_DQ02_H31	FBB_DQ02	FBA_DQ02	AE30	FBA_DQ02
FBB_DQ03_D32	FBB_DQ03	FBA_DQ03	AA34	FBA_DQ03
FBB_RAS_M33	FBB_RAS	FBA_RAS	AH31	FBA_RAS
FBB_CAS_M34	FBB_CAS	FBA_CAS	AG30	FBA_CAS
FBB_WE_A32	FBB_WE	FBA_WE	AE32	FBA_WE
FBB_CS0_M31	FBB_CS0	FBA_CS0	AG34	FBA_CS0
FBB_CS1_N31	FBB_CS1	FBA_CS1	AG31	FBA_CS1

FBB_CLK0_K32	FBB_CLK0	FBA_CLK0	AE34	FBA_CLK0
FBB_CLK0B_K33	FBB_CLK0B	FBA_CLK0B	AE34	FBA_CLK0B
FBB_CLK1_N32	FBB_CLK1	FBA_CLK1	AH33	FBA_CLK1
FBB_CLK1B_N33	FBB_CLK1B	FBA_CLK1B	AH34	FBA_CLK1B
FBB_CKE_K31	FBB_CKE	FBA_CKE	AD31	FBA_CKE



- <<FBA\_DATA[31:0] 10
- <<FBB\_DATA[31:0] 11
- <<FBD\_DATA[31:0] 11
- <<FBA\_ADR[13:0] 10
- <<FBB\_ADR[13:0] 10
- <<FBC\_ADR[13:0] 11
- <<FBD\_ADR[13:0] 11
- <<FBA\_DQS[3:0] 10
- <<FBB\_DQS[3:0] 11
- <<FBC\_DQS[3:0] 11
- <<FBD\_DQS[3:0] 11
- <<FBA\_DOM[3:0] 10
- <<FBB\_DOM[3:0] 11
- <<FBC\_DOM[3:0] 11
- <<FBD\_DOM[3:0] 11
- <<FBA\_RAS\_ 10
- <<FBA\_CAS\_ 10
- <<FBA\_WE\_ 10
- <<FBA\_CS0\_ 10
- <<FBA\_CLK0 10
- <<FBA\_CLK0B 10
- <<FBA\_CLK1 10
- <<FBA\_CLK1B 10
- <<FBA\_CKE 10
- <<FBB\_RAS\_ 10
- <<FBB\_CAS\_ 10
- <<FBB\_WE\_ 10
- <<FBB\_CS0\_ 10
- <<FBB\_CLK0 10
- <<FBB\_CLK0B 10
- <<FBB\_CLK1 10
- <<FBB\_CLK1B 10
- <<FBB\_CKE 10
- <<FBC\_RAS\_ 11
- <<FBC\_CAS\_ 11
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- <<FBC\_CLK0 11
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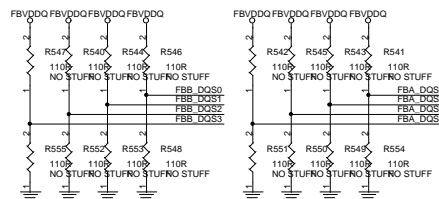
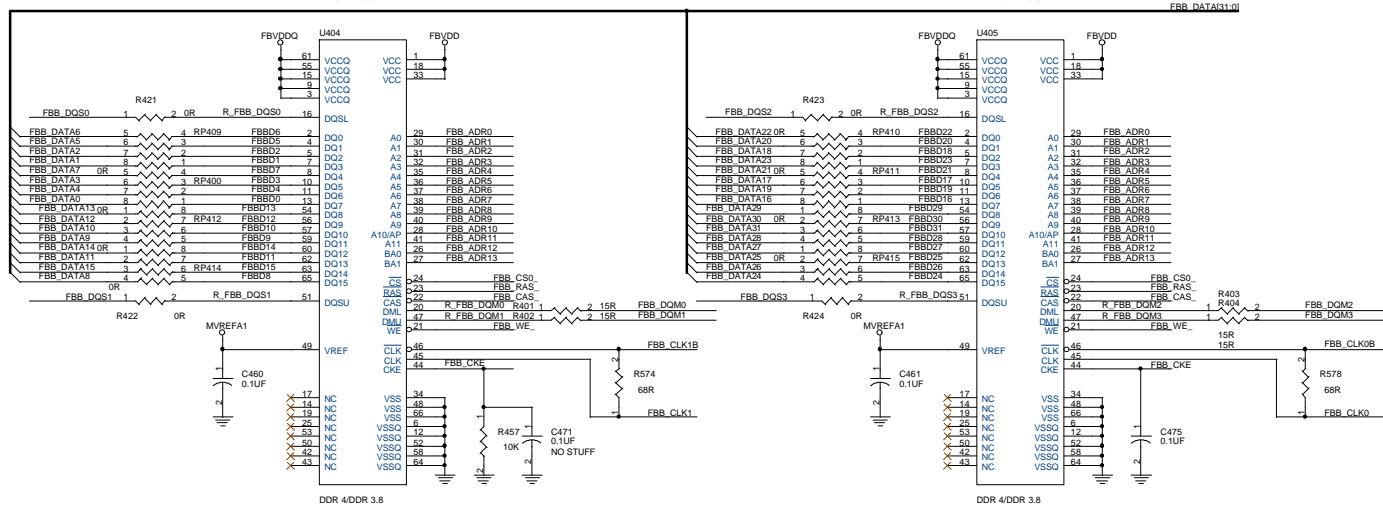
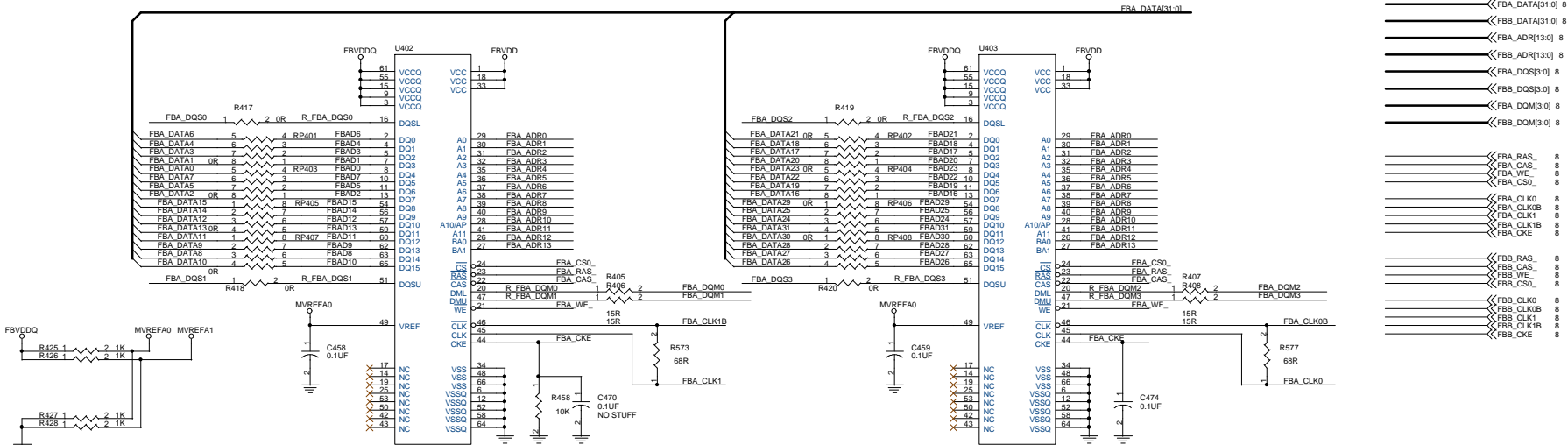


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Size C Document Number  
FB DECOUPLING 4MX16 SDRAM

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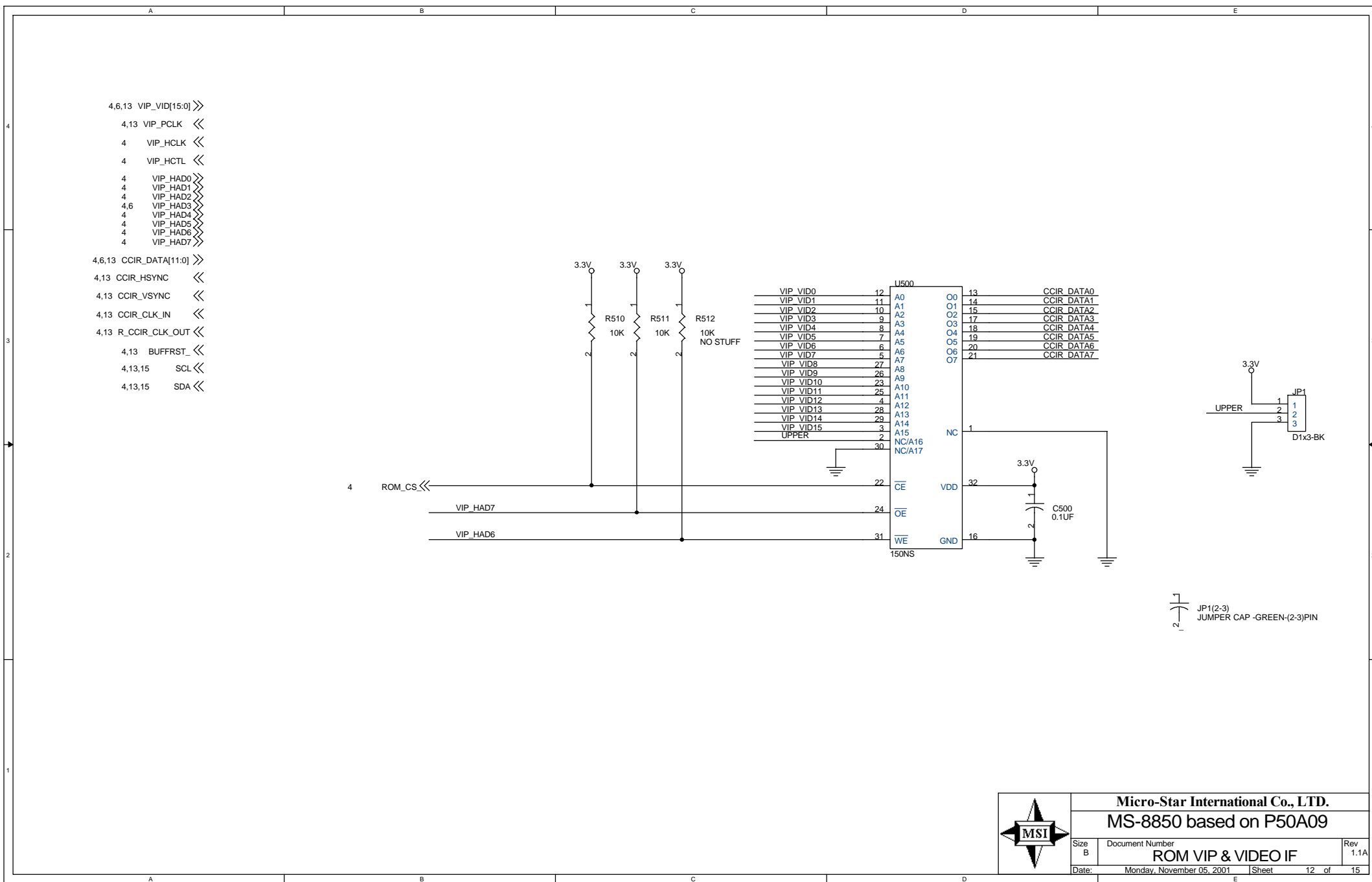
Rev 1.1A

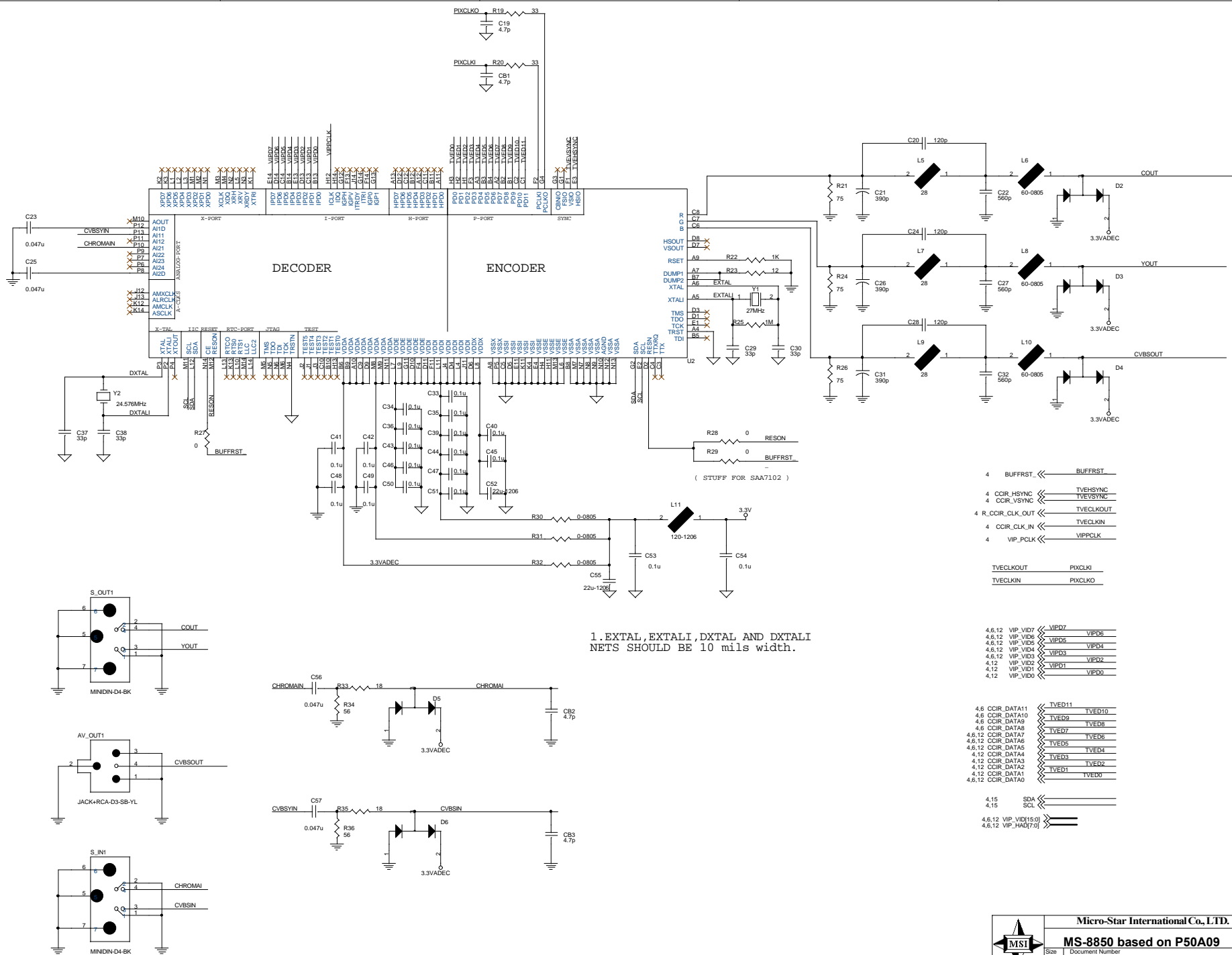


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MS-8850 based on P50A09

Size C Document Number  
FBA/B DDR 4MX16 SDRAM  
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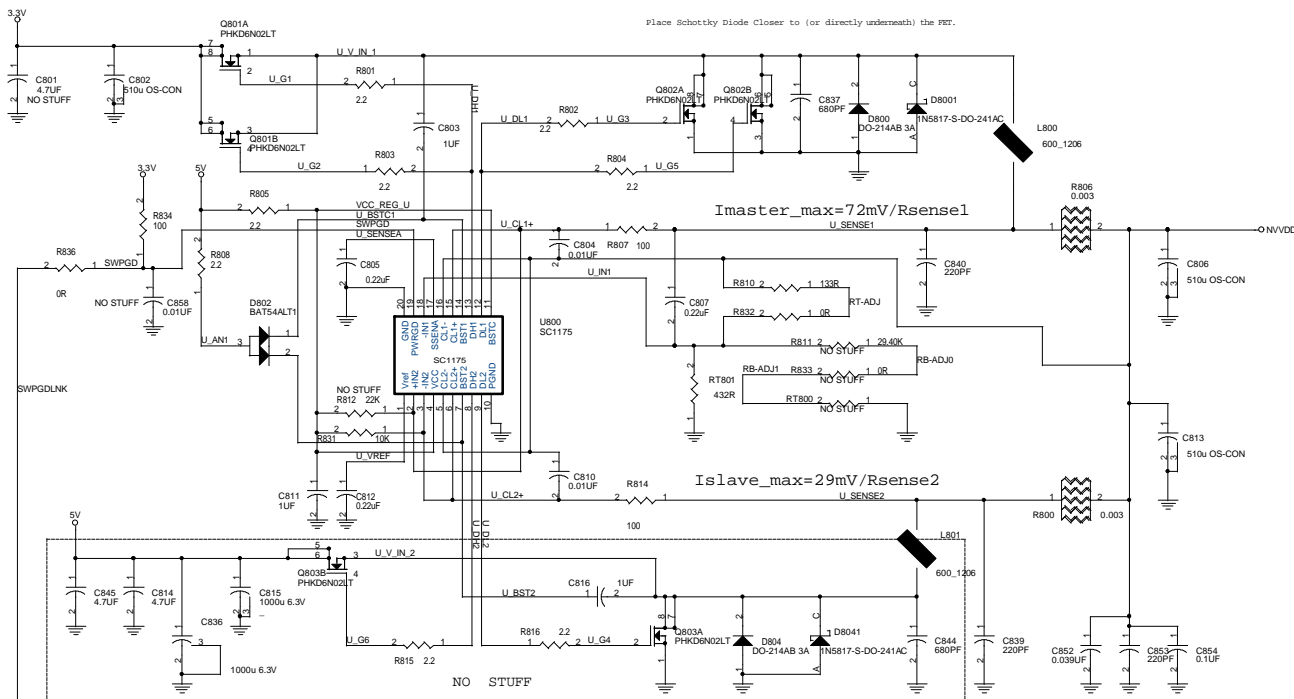
4 BUFFRST << BUFFRST  
 4 CCIR\_HSYNC << TVEHSYNC  
 4 CCIR\_VSYNC << TVEVSYNC  
 4 R\_CCIR\_CLK\_OUT << TVECLKOUT  
 4 CCIR\_CLK\_IN << TVECLKIN  
 4 VIP\_PCLK << VIPPCLK

TVECLKOUT PIXCLKI  
 TVECLKIN PIXCLKO

4.6,12 VIP\_VID7 << VIPD7  
 4.6,12 VIP\_VID6 << VIPD6  
 4.6,12 VIP\_VID5 << VIPD5  
 4.6,12 VIP\_VID4 << VIPD4  
 4.6,12 VIP\_VID3 << VIPD3  
 4.6,12 VIP\_VID2 << VIPD2  
 4.6,12 VIP\_VID1 << VIPD1  
 4.6,12 VIP\_VID0 << VIPD0

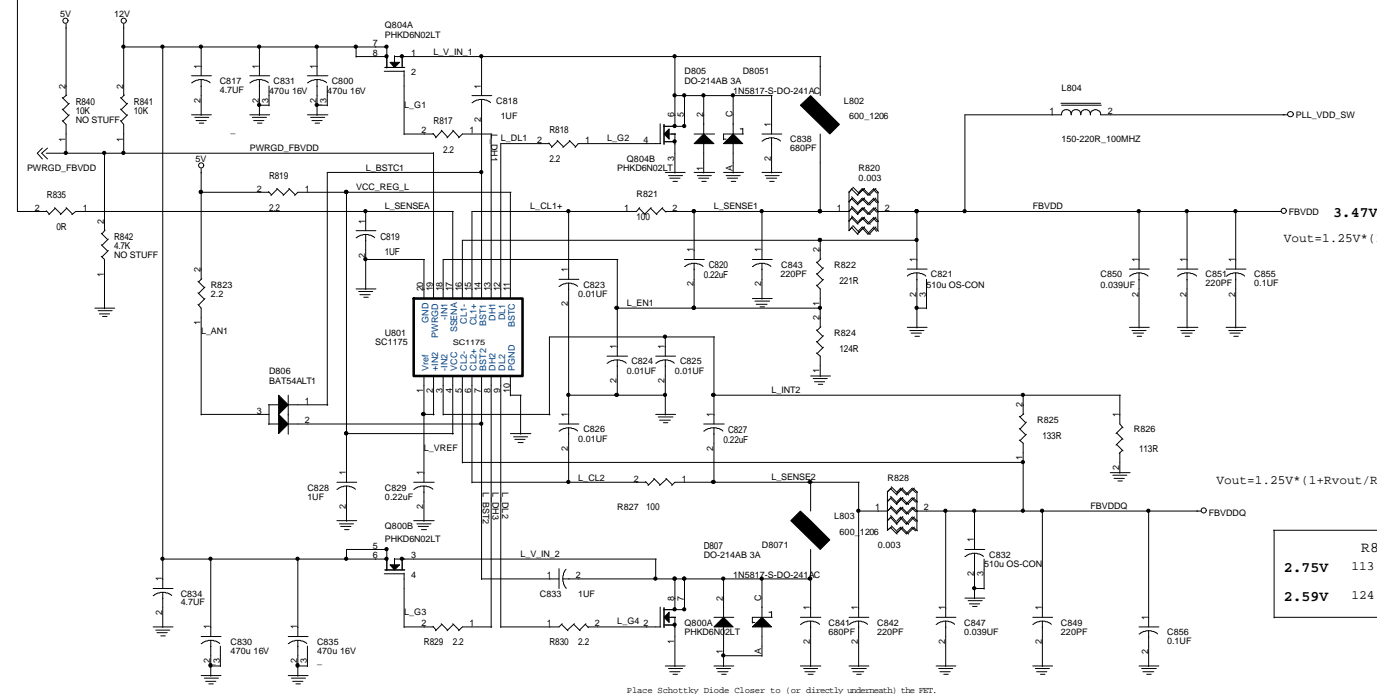
4.6 CCIR\_DATA11 << TVED11  
 4.6 CCIR\_DATA10 << TVED10  
 4.6 CCIR\_DATA9 << TVED9  
 4.6 CCIR\_DATA8 << TVED8  
 4.6,12 CCIR\_DATA7 << TVED7  
 4.6,12 CCIR\_DATA6 << TVED6  
 4.6,12 CCIR\_DATA5 << TVED5  
 4.6,12 CCIR\_DATA4 << TVED4  
 4.6,12 CCIR\_DATA3 << TVED3  
 4.6,12 CCIR\_DATA2 << TVED2  
 4.6,12 CCIR\_DATA1 << TVED1  
 4.6,12 CCIR\_DATA0 << TVED0

4.15 SDA << SDA  
 4.15 SCL << SCL  
 4.6,12 VIP\_VID[15:0] << VIP\_VID[15:0]  
 4.6,12 VIP\_HD[7:0] << VIP\_HD[7:0]



$$V_{out} = 1.25V * (1 + R_{vout}/R_{gnd}) + R_{gnd} * (I_{fb} = 2\mu A / 10^6)$$

	R810	RT801
<b>1.52V</b>	133 Ohm	619 Ohm
<b>1.67V</b>	133 Ohm	392 Ohm
1.67V is for GF3-H chip		
<b>1.60V</b>	133 Ohm	432 Ohm

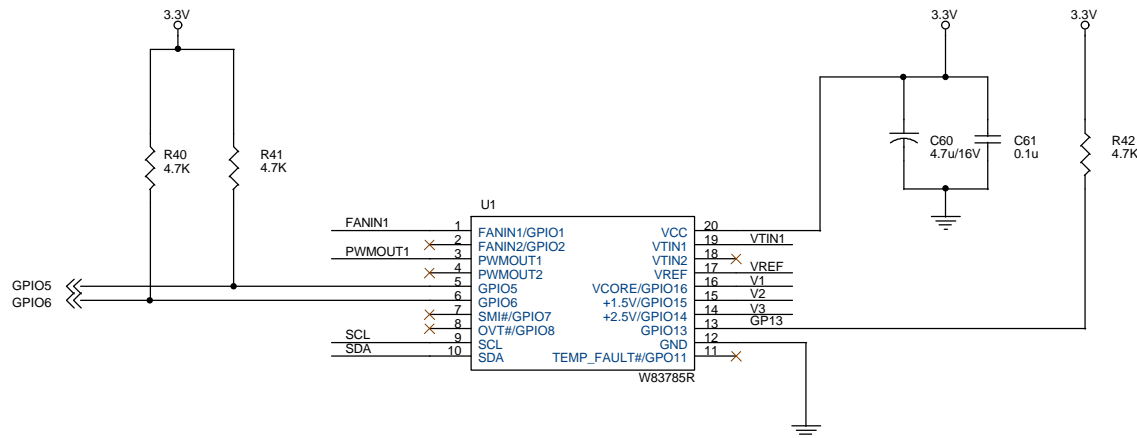


	R826
<b>2.75V</b>	113 Ohm
<b>2.59V</b>	124 Ohm



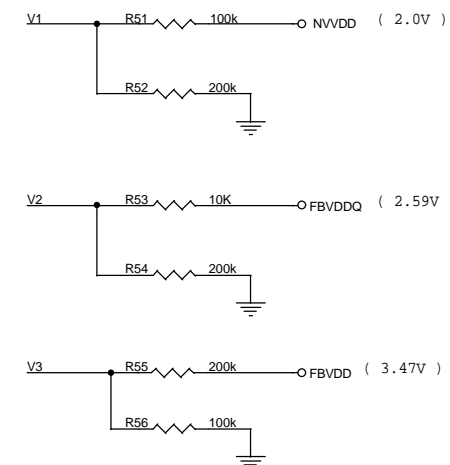
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NV20 POWER  
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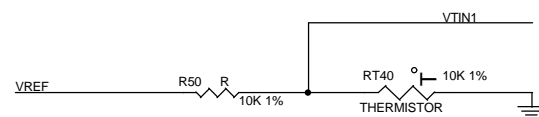


PWM1 Circuit for FAN1 speed Control  
FOR 12V FAN

SDA << SDA 4,13  
SCL << SCL 4,13



VOLTAGE SENSING CIRCUIT



TEMPERATURE SENSING CIRCUIT



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