

G94-P545-A01 - GDDR3, DVI/VGA + DVI/VGA + HDTV/SDTV-Out

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10545-0000-100	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	600-10545-0100-100	G94-400 6500MHz/1000MHz 512MB 16MA32 BGA136 GDDR3, DVI-I+DL+DVI-I+DL+HDTV-Out (Bring Up SKU)
2	SKU0000	600-10545-0000-100	G94-400 6500MHz/1000MHz 512MB 16MA32 BGA136 GDDR3, DVI-I+DL+DVI-I+DL+HDTV-Out
3	SKU0010	600-10545-0010-100	G94-300 6500MHz/8000MHz 512MB 16MA32 BGA136 GDDR3, DVI-I+DL+DVI-I+DL+HDTV-Out
4	SKU020	600-10545-0020-100	G94-300 6500MHz/1000MHz 384MB 16MA32 BGA136 GDDR3, DVI-I+DL+DVI-I+DL+HDTV-Out
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

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V127-0A Base on P545

- 1.PAGE18: ADD Display port circuit
- 2.PAGE21: ADD GPIO circuit
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- 8.PAGE 30: change NNVDD POWER APW7088 circuit
- 9.PAGE 16/17 : ADD EMI bridge R
- 10.PAGE 17 CO-LAYOUT HDIM CONNECT
- 11.PAGE 15 remove J2 D_SUB SLIM CONNECT
- 12.PAGE 29 ADD CH7322 circuit

V127-20 Base on V127-0A


- 1.PAGE30 .CO-LAYOUT RT9258 circuit

V127-40 Base on V127-20

- 1.PAGE34 .Add Hybrid Power circuit modify form P393 and Hybrid APP note
- 2.PAGE20 .Remove SLi circuit
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- 4.PAGE17 .TMDS C/D Revise to HDMI short connector and remove DVI connector, And Change HDMI to I2CD bus
- 5.PAGE32 .Add FAN seat for Heatsink solution
- 6.PAGE25&2 .Reserve MB support SPDIF IN circuit
- 7.PAGE29 .Remove U508 CEC circuit
- 8.PAGE16 .Add EMI diff sultion
- 9.PAGE17 .Add EMI diff sultion
- 10.PAGE17 .Add EMI suggestion C16 for 3V3_F to GND
- 11.PAGE32 .Add EMI suggestion EM1~EM6 Spring part

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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview



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<Title>

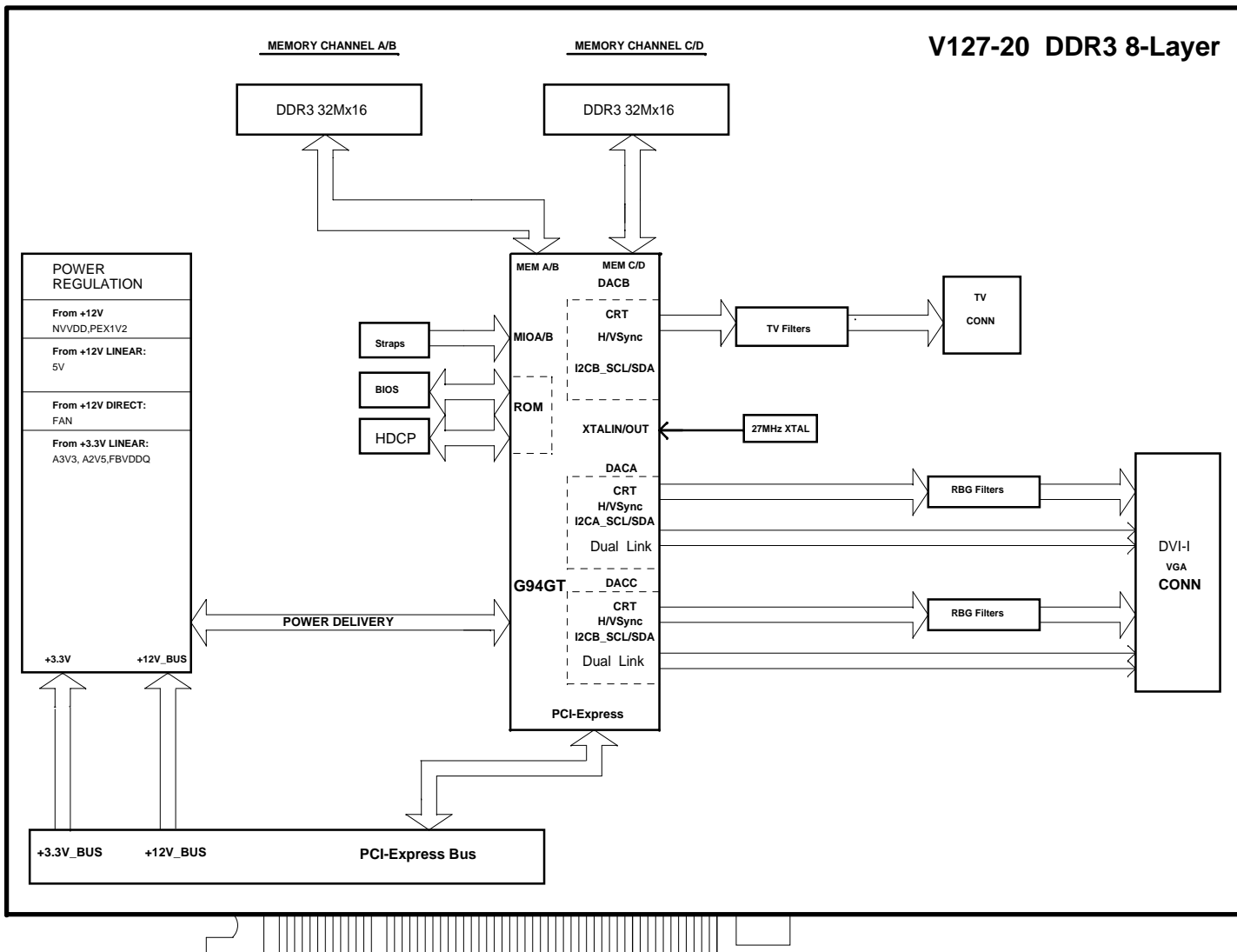
Size: 11
Custom

Document Number: MS-V127

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ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

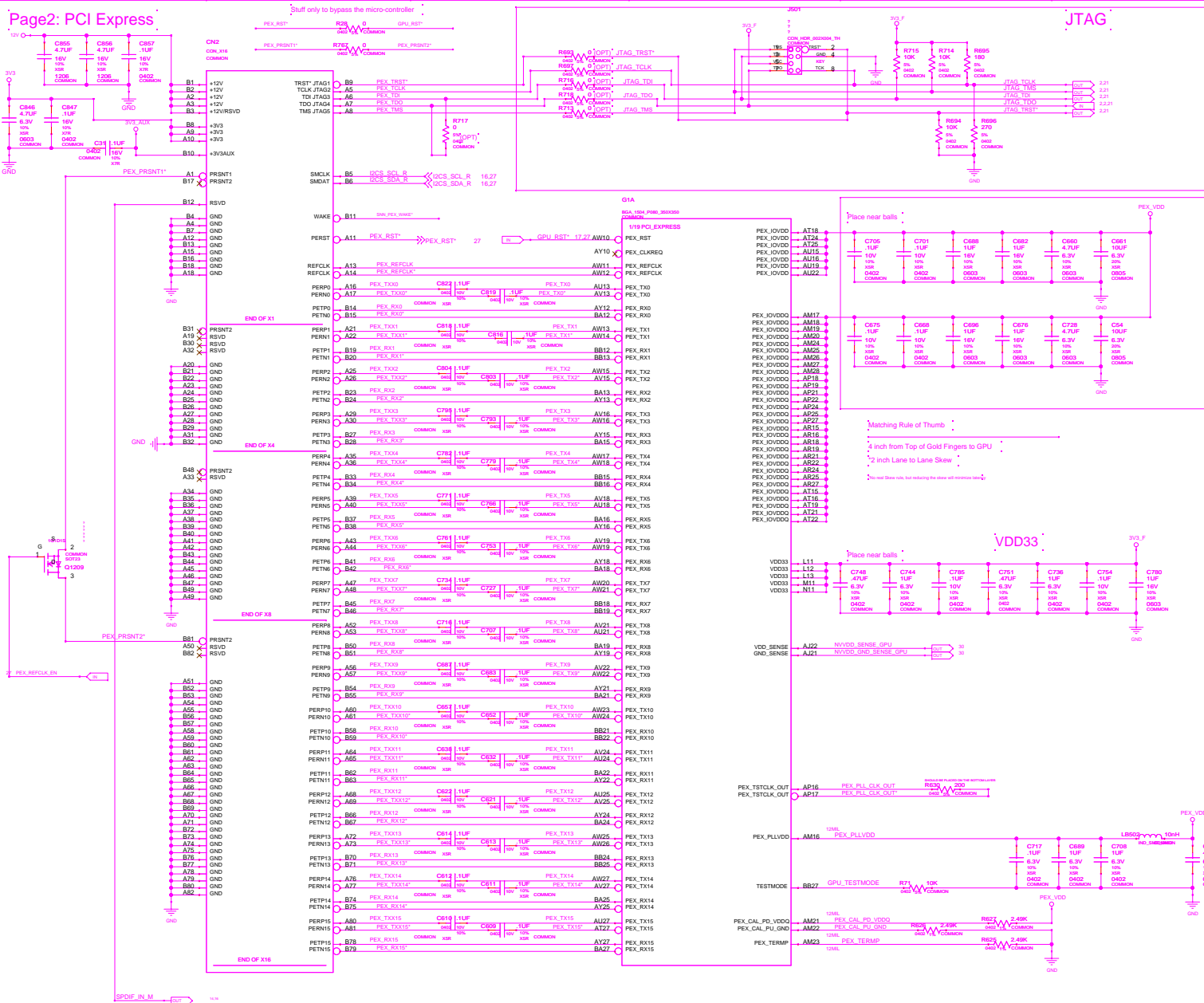
ASSEMBLY PAGE DETAIL	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL P381 Overview
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ASSEMBLY	M545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express



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	<Title>
--	---------

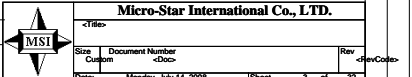
Size	Document Number
------	-----------------

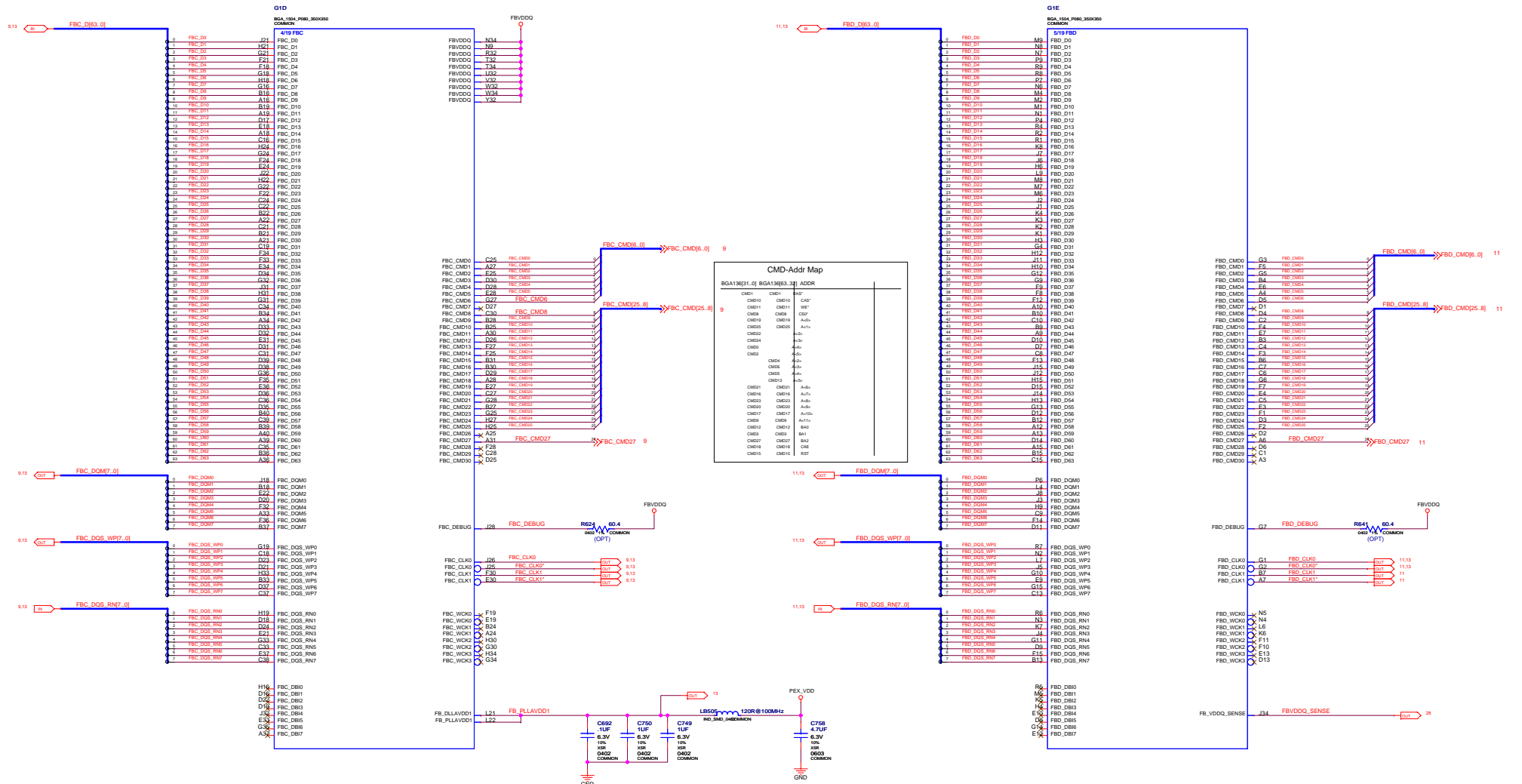
Custom <Doc>

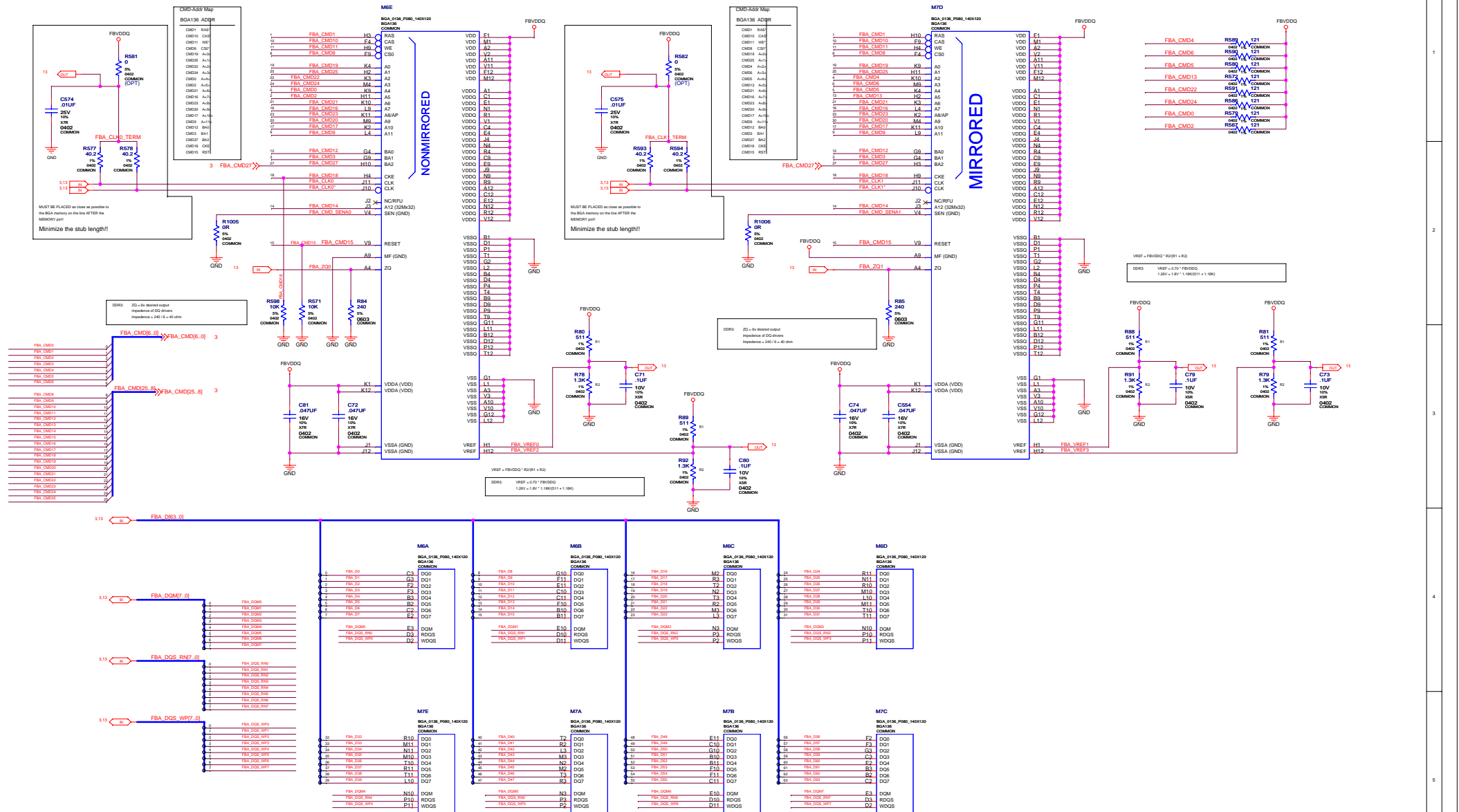
Date: Monday, July 14

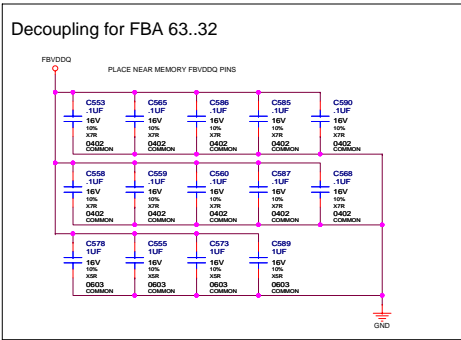
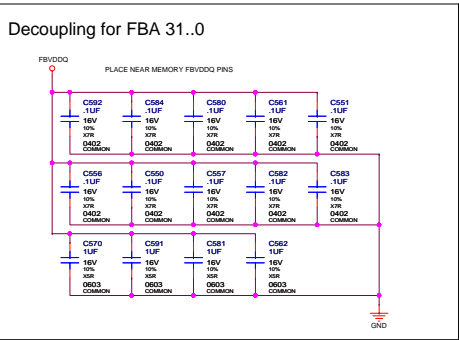
29

<RevCode>









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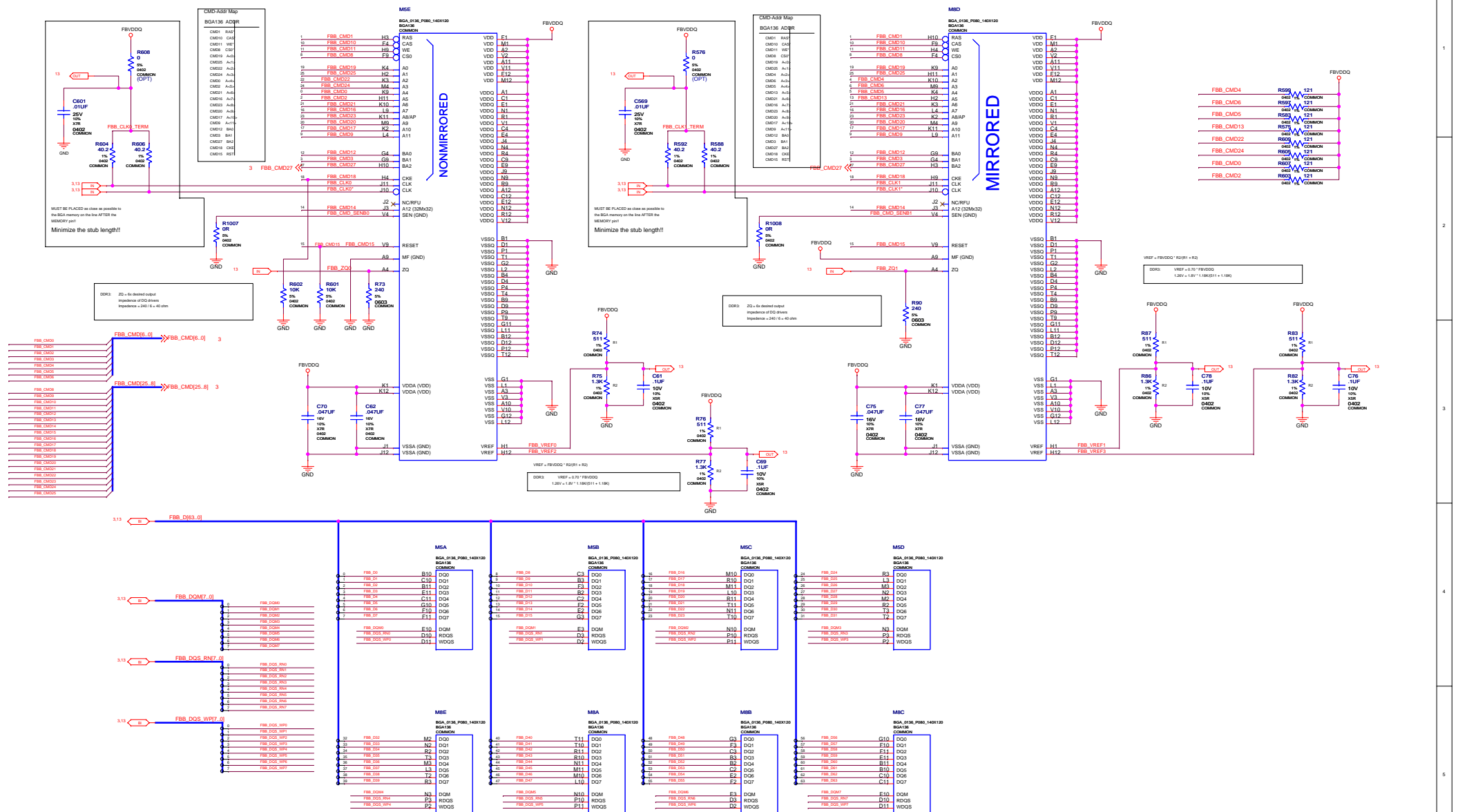
ASSEMBLY PAGE DETAIL FBA Partition Decoupling



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<Title>
Size Custom Document Number <Doc>
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Rev <RevCode>

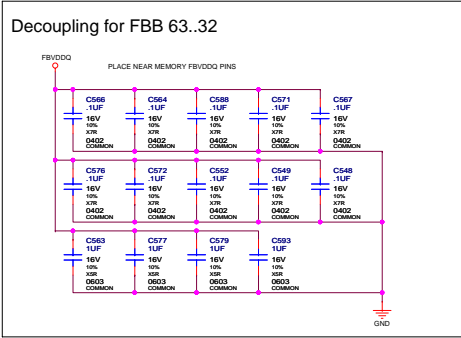
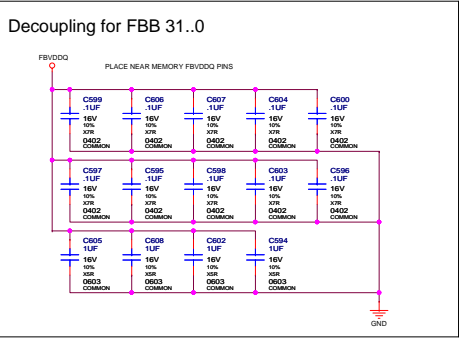


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ASSEMBLY PAGE DETAIL
FBB Partition

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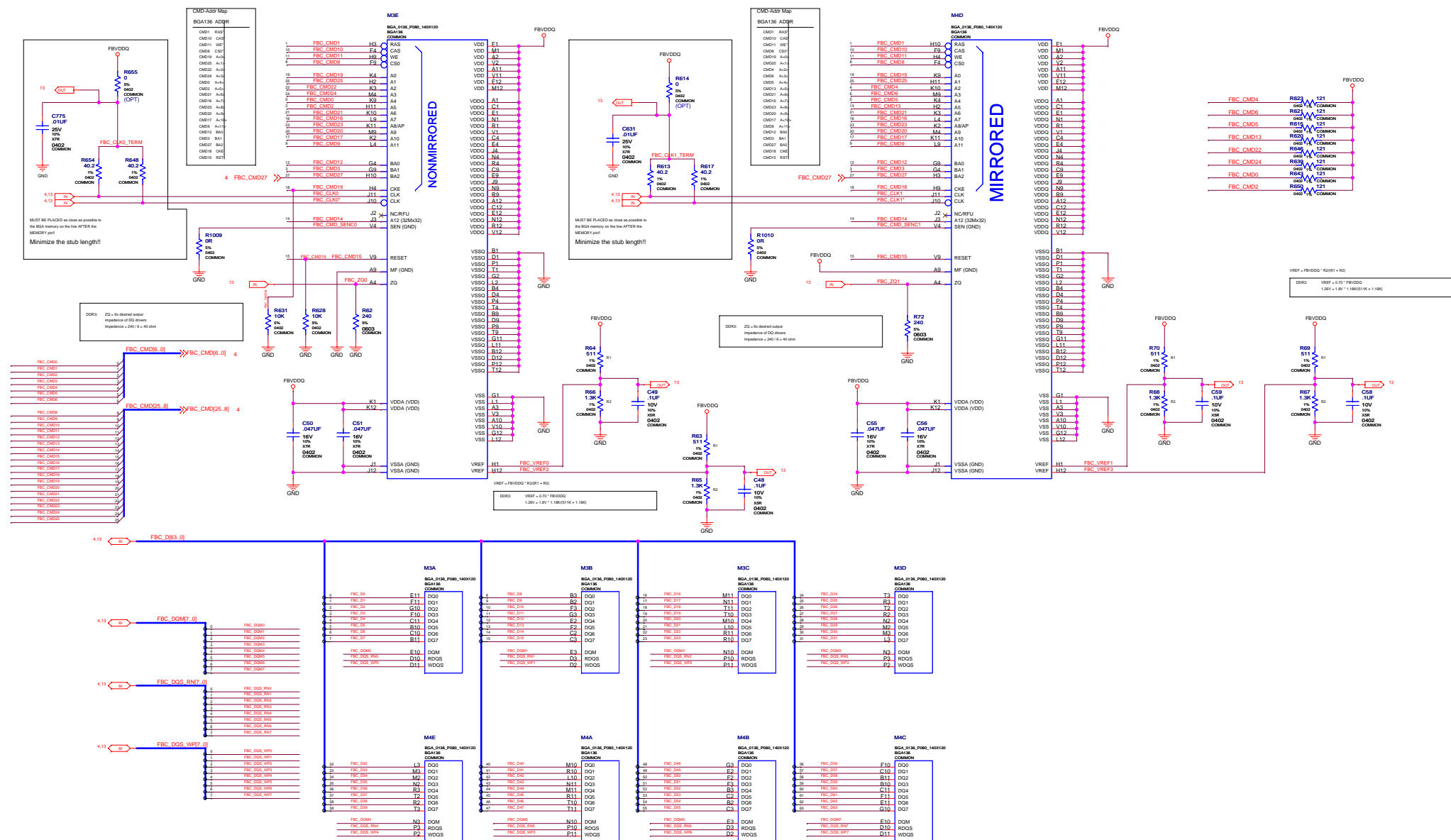
ASSEMBLY
PAGE DETAIL
PS/2 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. 3, 1U/2U ASSEMBLY NOTES AND BOM NOT FINAL
FBB Partition Decoupling



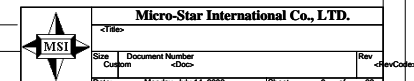
Micro-Star International Co., LTD.

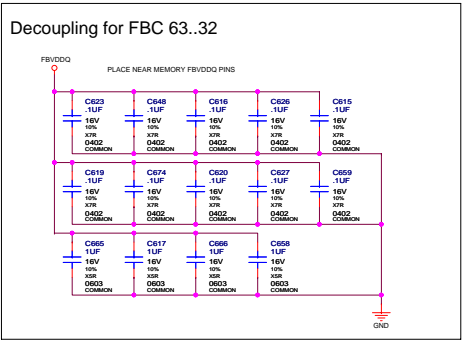
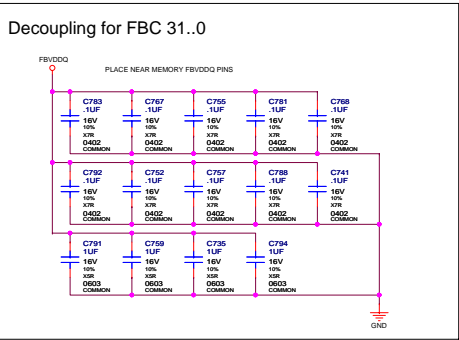
<Title>
Size Custom Document Number <Doc>
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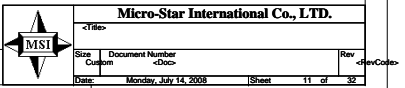
ASSEMBLY
PAGE DETAIL
PSIE BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO 3YUFF ASSEMBLY NOTES AND BOM NOT FINAL
FBC Partition Decoupling



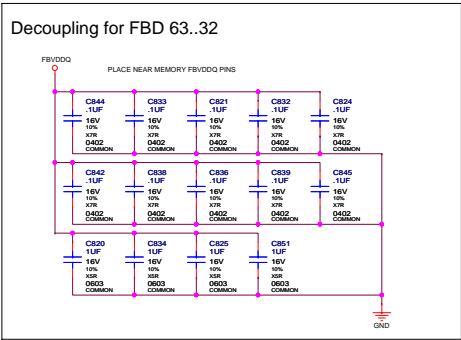
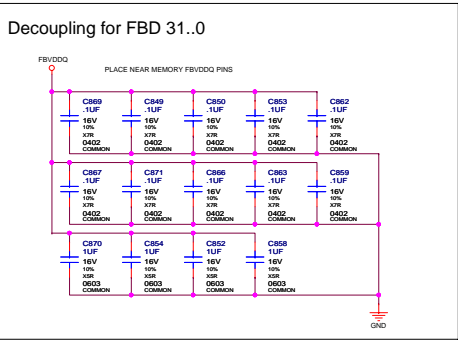
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<Title>
Size Custom
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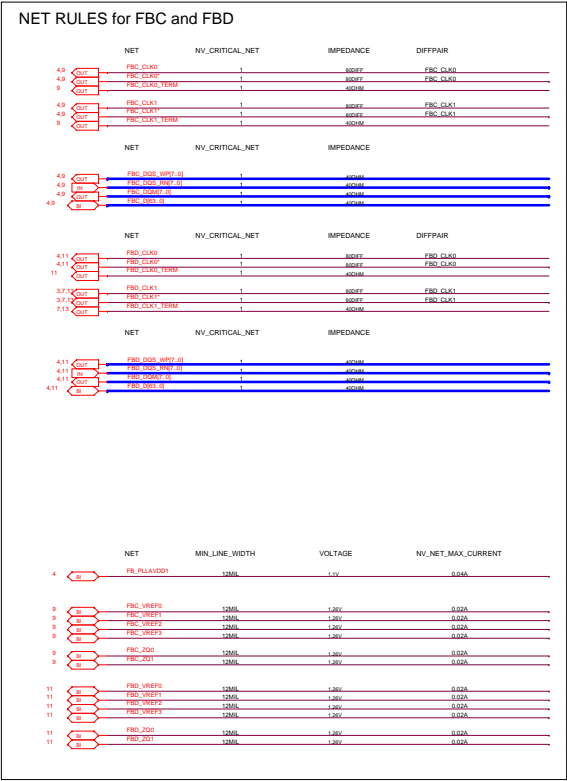
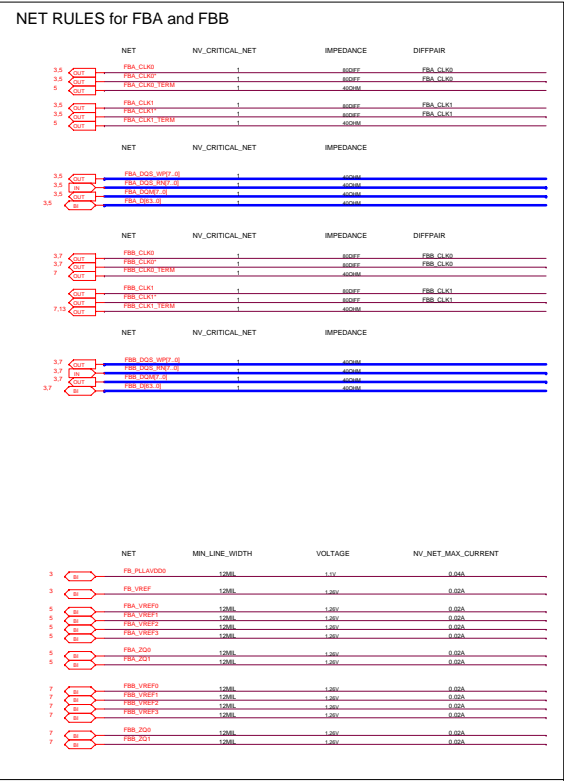
ASSEMBLY PAGE DETAIL
PS4 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO 3V3UFF ASSEMBLY NOTES AND BOM NOT FINAL
FBD Partition Decoupling



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<Title>
Size Custom Document Number <Doc>
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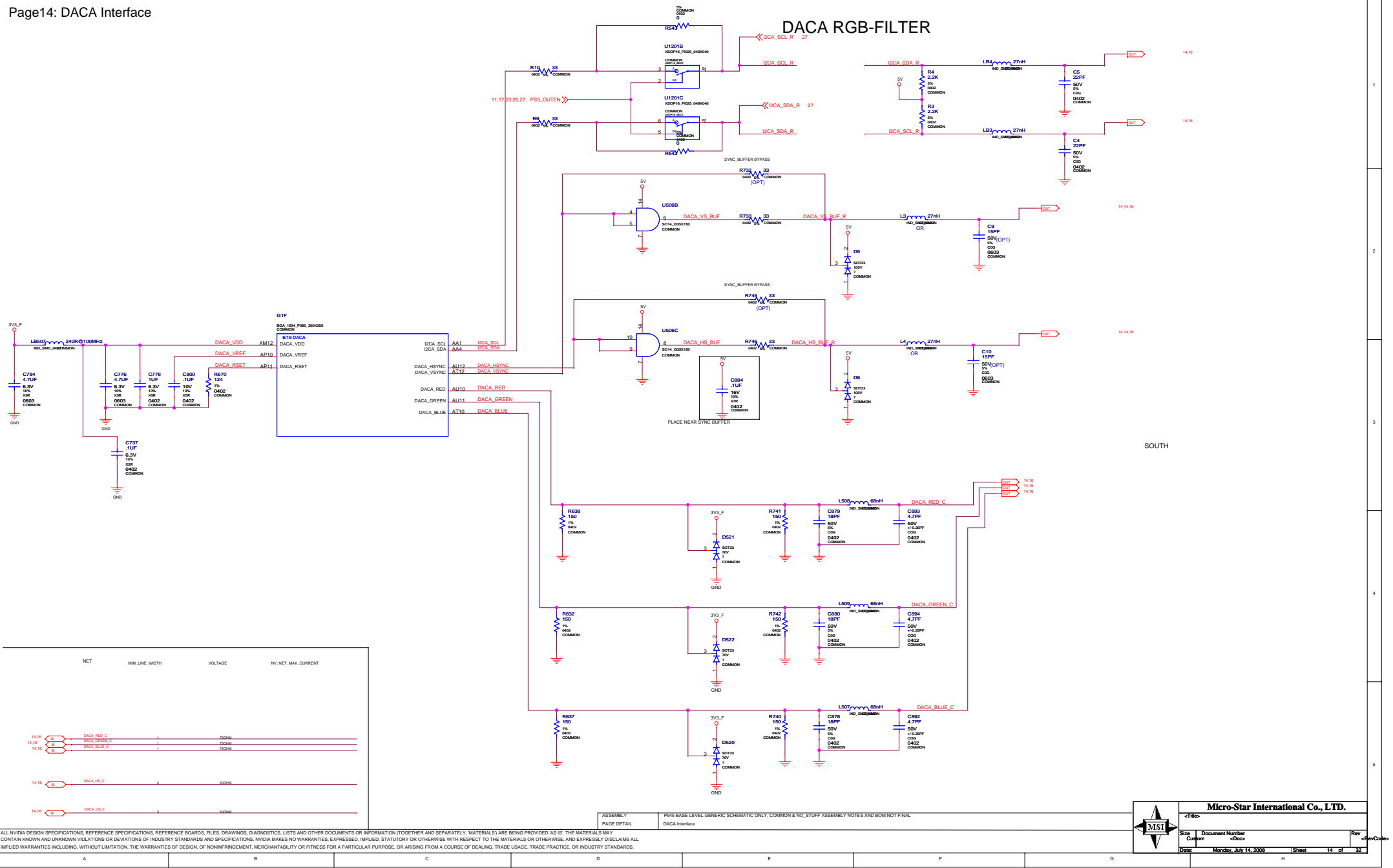
ASSEMBLY PAGE DETAIL P/S47 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. 3/UFF ASSEMBLY NOTES AND BOM NOT FINAL FB Net Properties

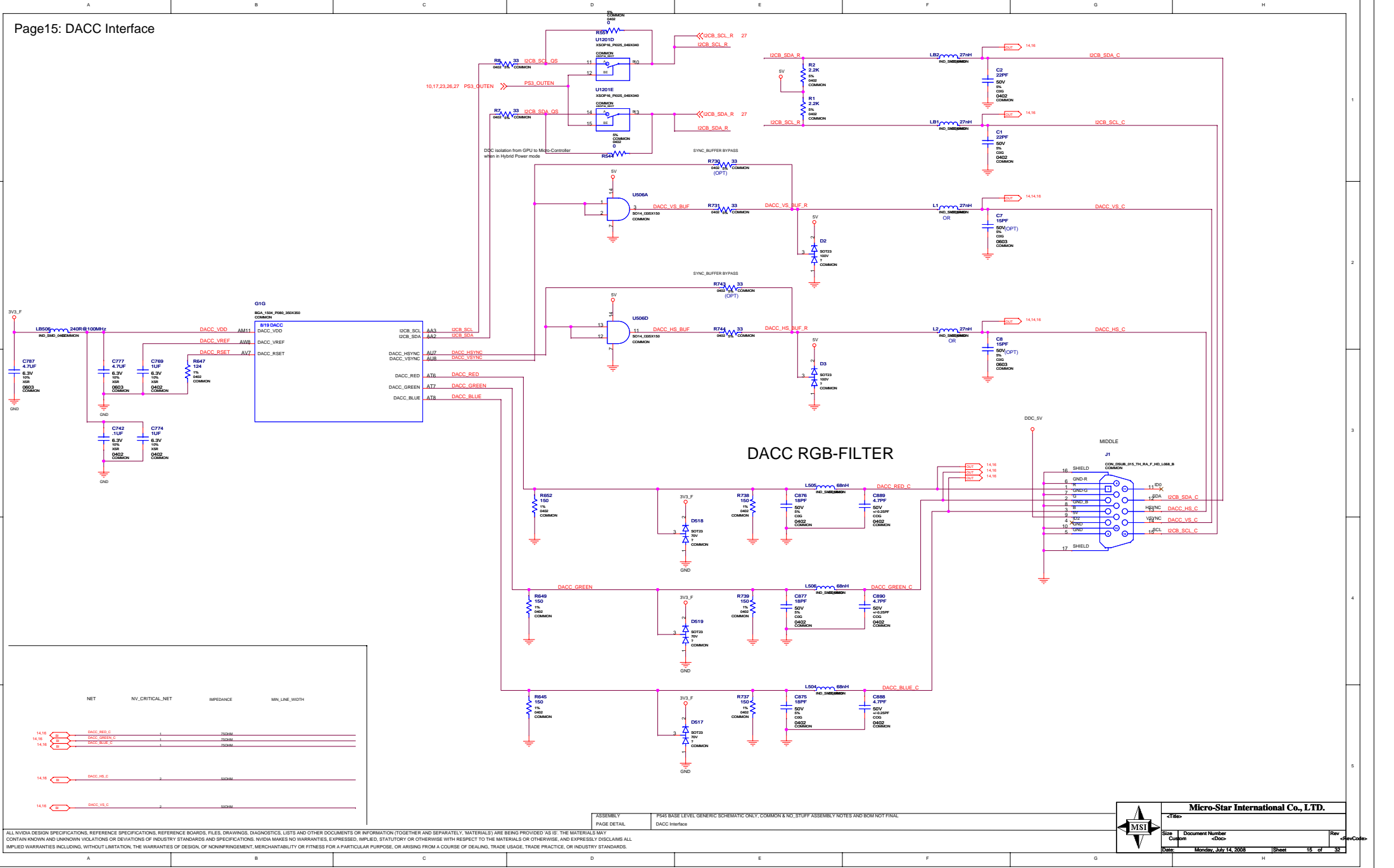


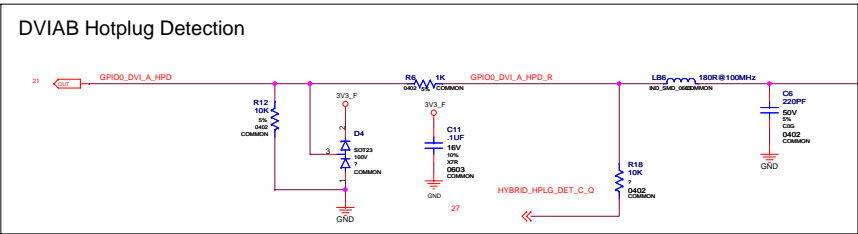
Micro-Star International Co., Ltd.


<Title> Size Custom Document Number <Doc> Date: Tuesday, July 01, 2008 Sheet 13 of 32


Rev <Rev Code>

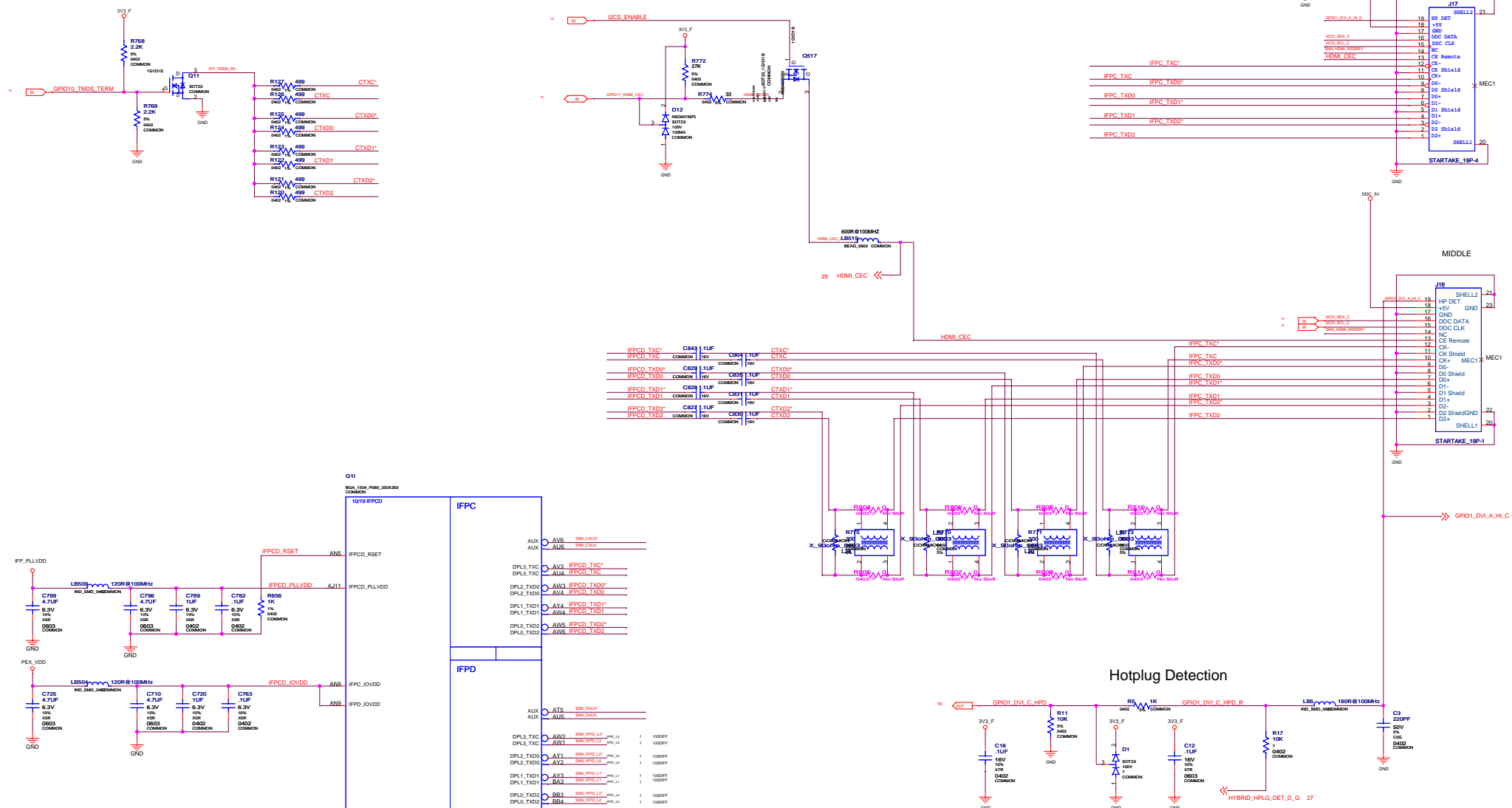




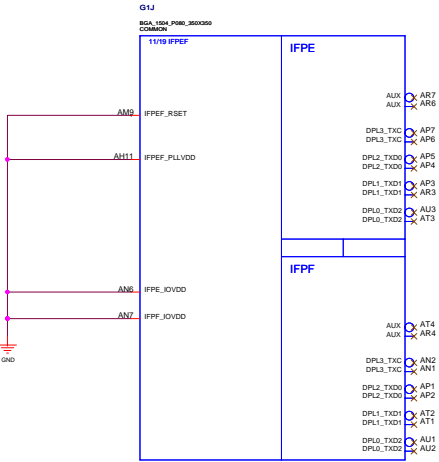
[illegible]

	Micro-Star International Co., LTD.		
	<Title>		
	Size Custom	Document Number <Doc>	Rev <Rev/Code>
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	Micro-Star International Co., LTD.		
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	Size Custom	Document Number <Doc>	Rev <Rev/Code>
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Page18: IFP E/F Interface -- Unused
TMDS E : Display Port



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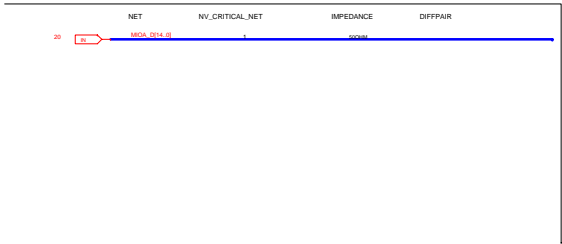
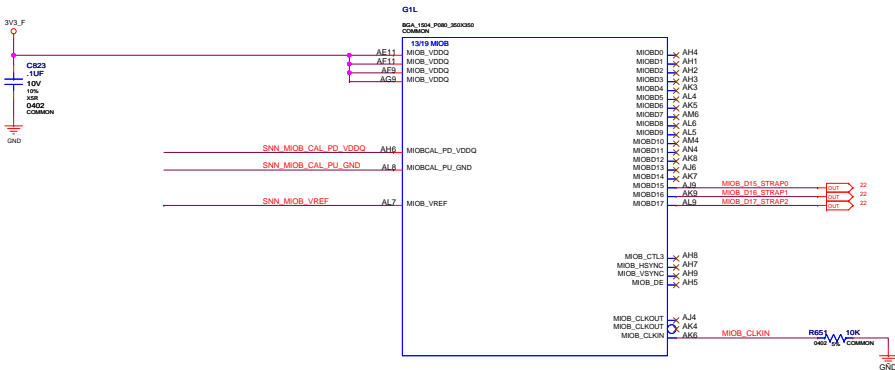
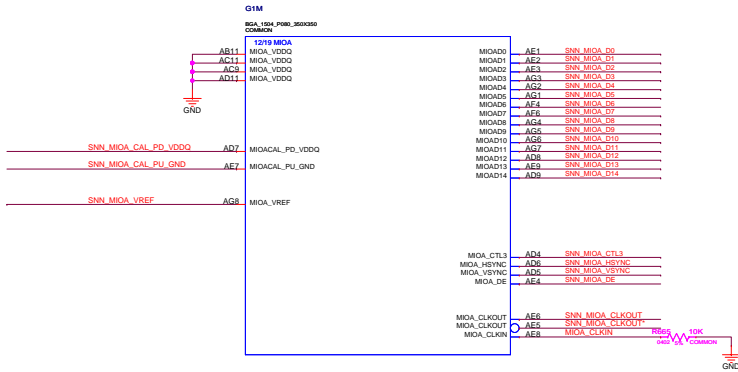
ASSEMBLY PAGE DETAIL P&ID BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO 31/0FF ASSEMBLY NOTES AND BOM NOT FINAL IFP E/F Interface -- Unused



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Size Custom Document Number <Doc>
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ASSEMBLY	PG# BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO 3V3/FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIO A/B Interface

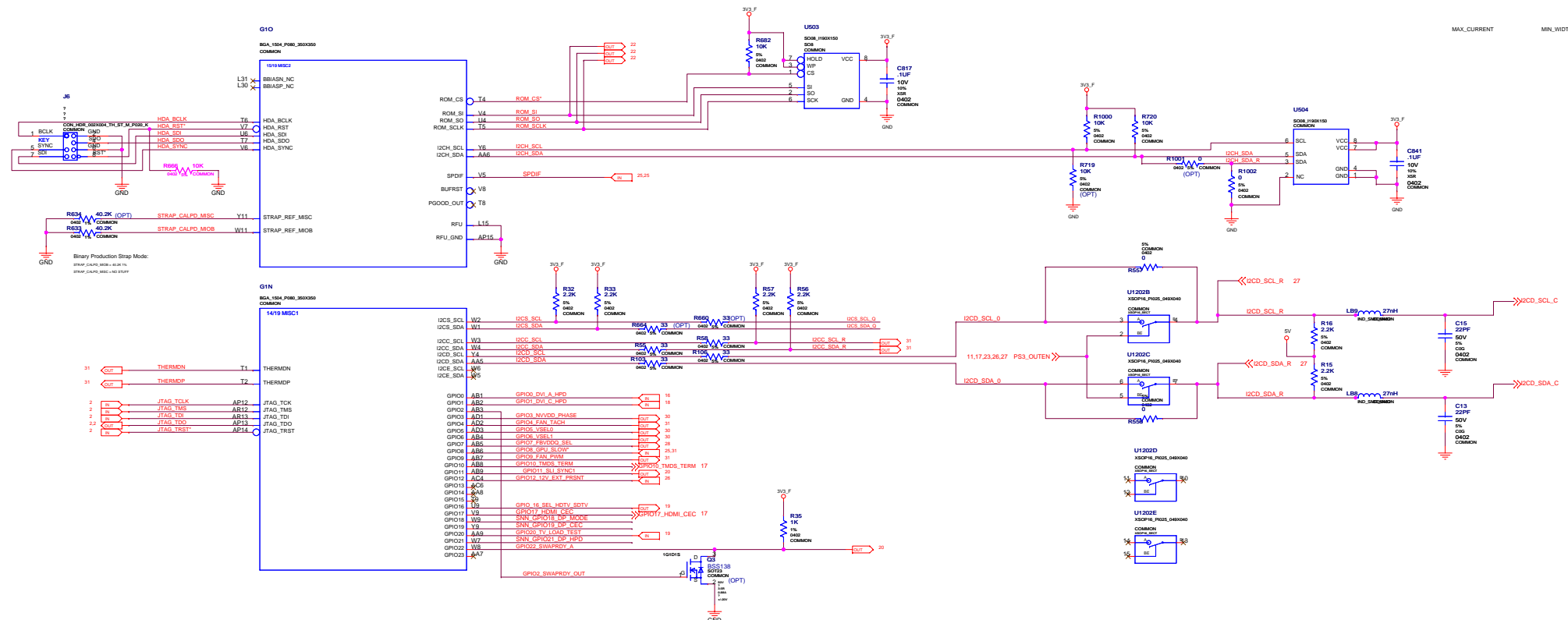


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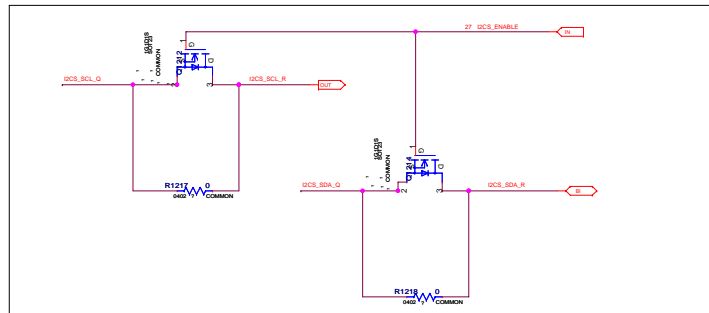
<Title>	
Size	Document Number
Custom	<Doc>
Date	Monday, July 14, 2008
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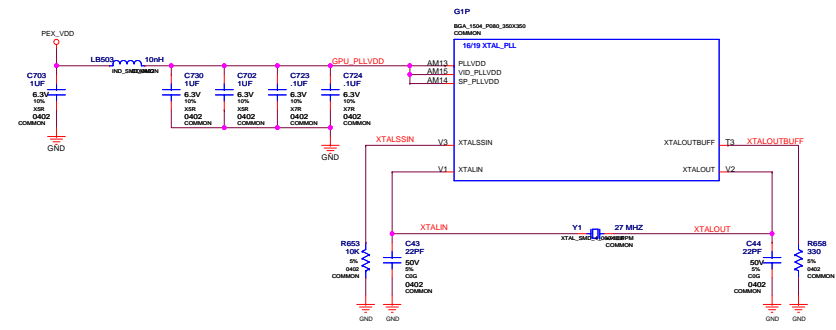
<Rev Code>

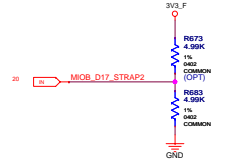


I2CS isolation for Hybrid Power



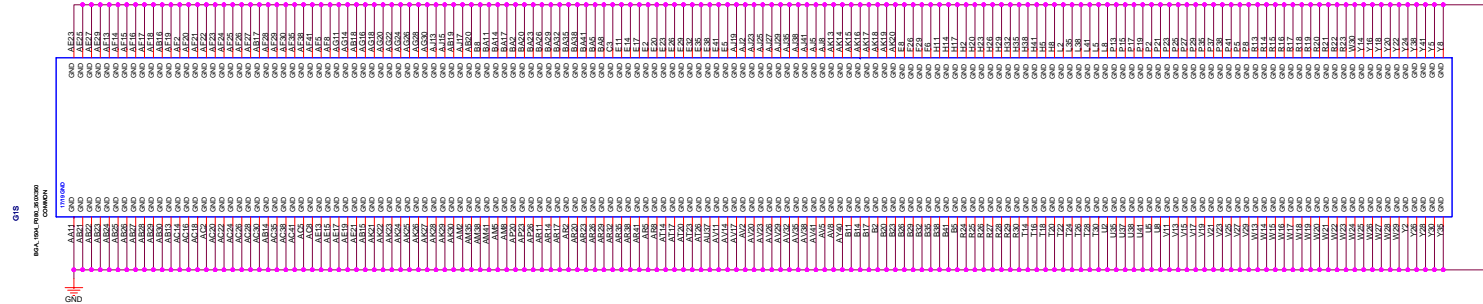
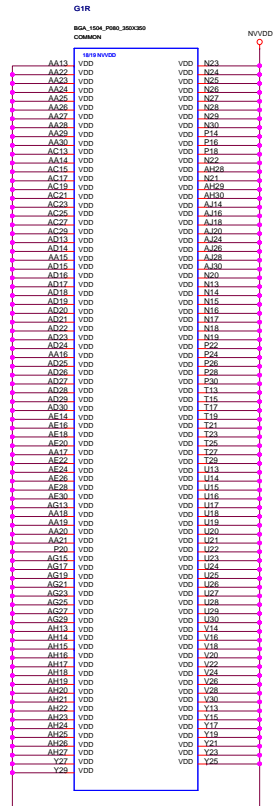
GPIO Table		
GPIO	IO	Function
0	IN	DI0 HPIOL2 SELECT A
1	IN	DI0 HPIOL2 SELECT E
2	IN	SWAPREADY
3	N/A	NVDDO POWER CONTROL
4	N/A	PWM7X SIGNAL
5	OUT	VOLTAGE SELECT 0
6	OUT	VOLTAGE SELECT 1
7	N/A	PERFID VOLTAGE CONTROL
8	IO	DP15, 16
9	OUT	PWM FAN CONTROL
10	N/A	UNUSED
11	IN	SLI MASTER/SLY SYNC
12	IN	EXT. INT. DETECT
13	OUT	UNUSED
14	IN	UNUSED
15	IN	UNUSED
16	IN	DP_MODE
17	IN	HDMI_CEC
18	IN	UNUSED
19	IN	DP HPIOL2 SELECT F
21	IN	SWAPREADY_A
22	IN	UNUSED
23	OUT	UNUSED

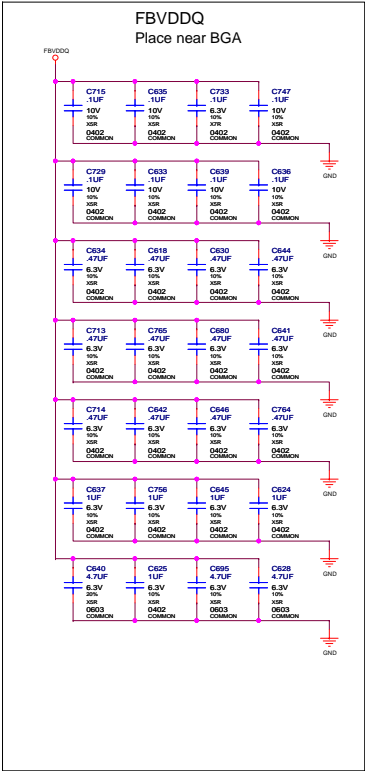
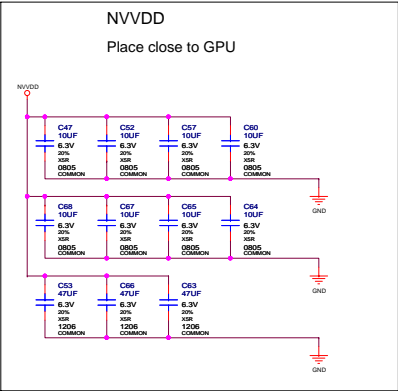
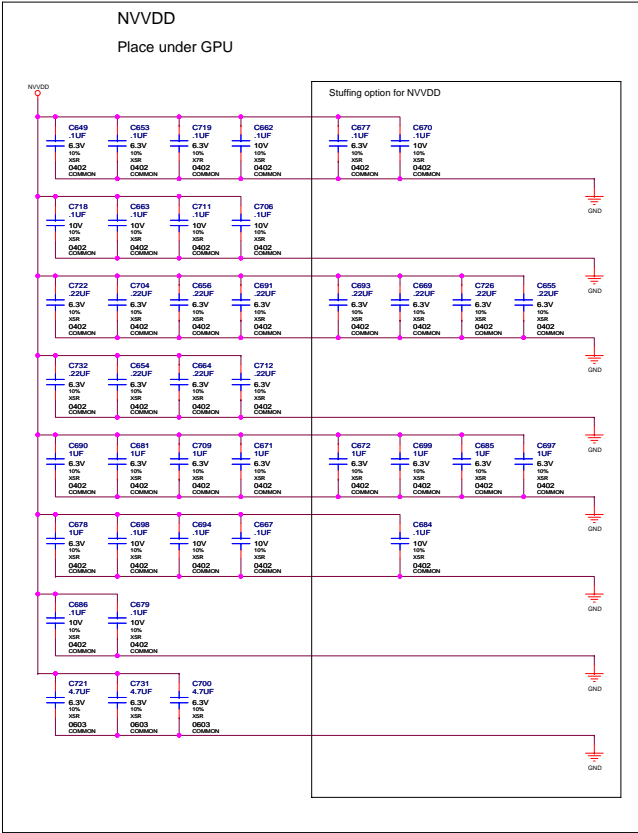




STRAP PIN	STRAP NAME			
STRAP0	RAMCFG0			

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ASSEMBLY PAGE DETAIL P507 BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 3/UFF ASSEMBLY NOTES AND BOM NOT FINAL NVVDD and FBVDDQ Decoupling



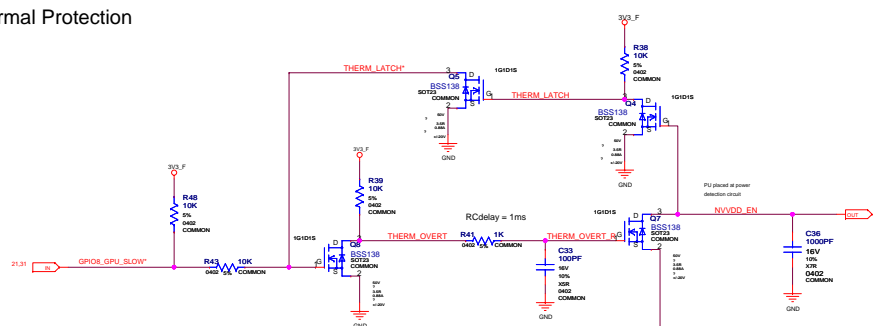
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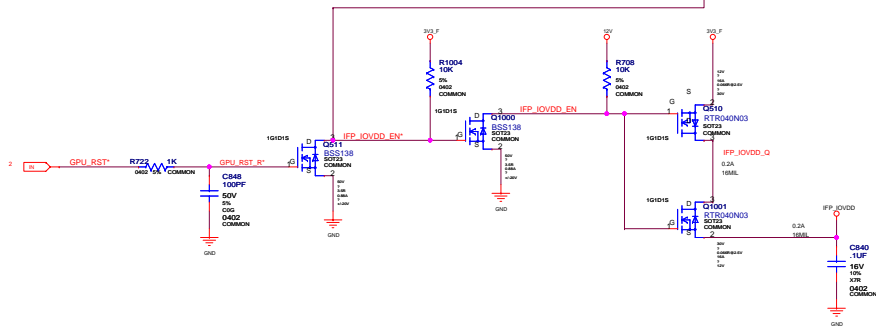


Thermal Protection

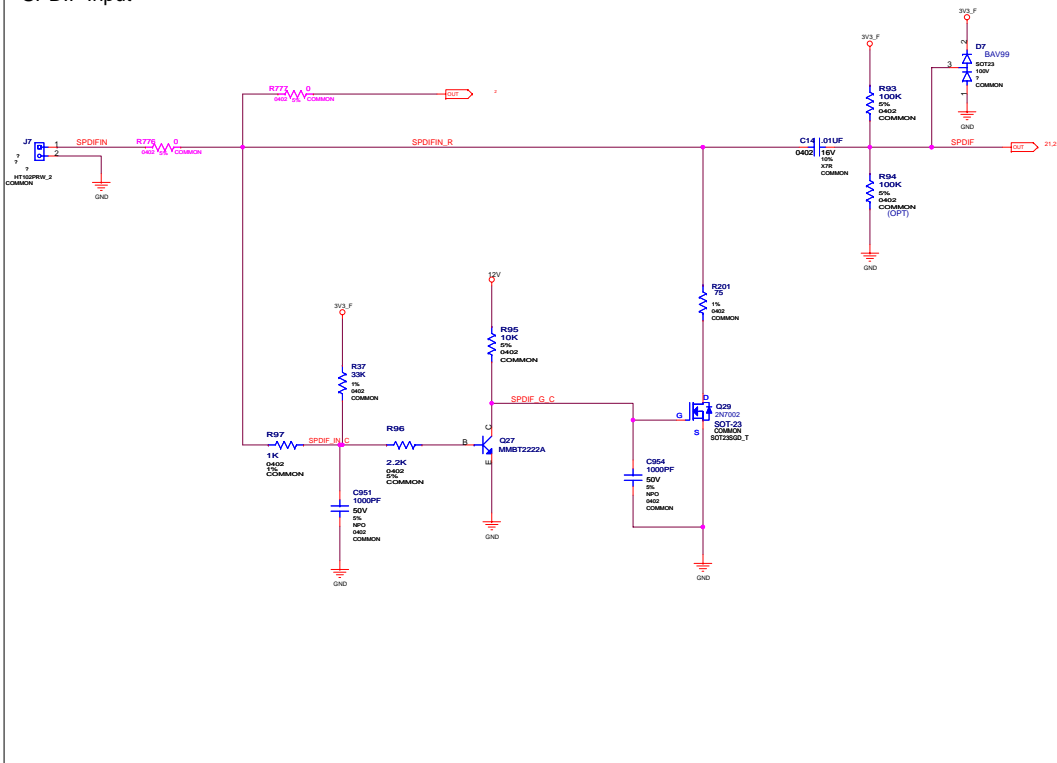


IFP_IOVDD Backdrive Prevention

Stuffing possibilities for thermal control and protection:



SPDIF Input



ASSEMBLY	P645 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPI0IF Input, Backdrive Protection, and IFF_I0VDD Power Supply

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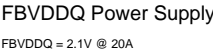
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	GPIO7
FBVDDQ = 1.792V	0
FBVDDQ = 1.999V	1

$$\begin{aligned} \text{FBVDDQ} &= \text{VREF} * (1 + (\text{Rtop} / \text{Rbot1})) \\ 1.82\text{V} &= 0.8 * (1 + (2.55\text{K} / 2\text{K})) \end{aligned}$$

$$\begin{aligned} \text{FBVDDQ} &= \text{VREF} * (1 + (\text{Rtop} / (\text{Rbot1} // \text{Rbot2}))) \\ 2.02\text{V} &= 0.8 * (1 + (2.55\text{K} / (2\text{K} // 10\text{K}))) \end{aligned}$$
$$2.02V = 0.8 * (1 + (2.55K / (2K // 10K)))$$
$$\| \text{vec}(\hat{\Sigma}_n) - \text{vec}(\Sigma_0) \| = \left(\sum_{j=1}^m \left\{ \|\text{vec}(\hat{\Sigma}_{nj}) - \text{vec}(\Sigma_{0j})\|^2 + \|\text{vec}(\hat{\Sigma}_{n,j+1}) - \text{vec}(\Sigma_{0,j+1})\|^2 \right\} \right)^{1/2}$$

ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTE'S AND BOM NOT FINAL
PAGE DETAIL	PS III: FBVDDQ Power Supply



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NVVDD Voltage Select			
NVVDD range 0.80V-1.40V			
Register: A2F3208			
Control via NV_GPU0s NV_VSEL[1..0]			
VID		NVVDD	
E 5#32	10 Vout	G94	
0 1 1 0 0 0	0.80V		
0 1 1 0 1 0	0.80V		
0 1 1 0 0 0	0.90V		
0 1 0 1 1 0	0.90V		
0 1 0 1 0 0	1.00V		
0 1 0 0 1 0	1.00V		
0 1 0 0 0 0	1.10V		
0 0 1 1 1 0	1.15V		
0 0 1 1 0 0	1.20V		
0 0 1 0 1 0	1.25V		
0 0 1 0 0 0	1.30V		
0 0 1 1 1 0	1.35V		
0 0 1 1 0 0	1.40V		
		==> Default	
		==> Voltage1	
		==> Voltage2	

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ASSEMBLY	PSIV BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO SHUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS IV: NVVDD VID Control



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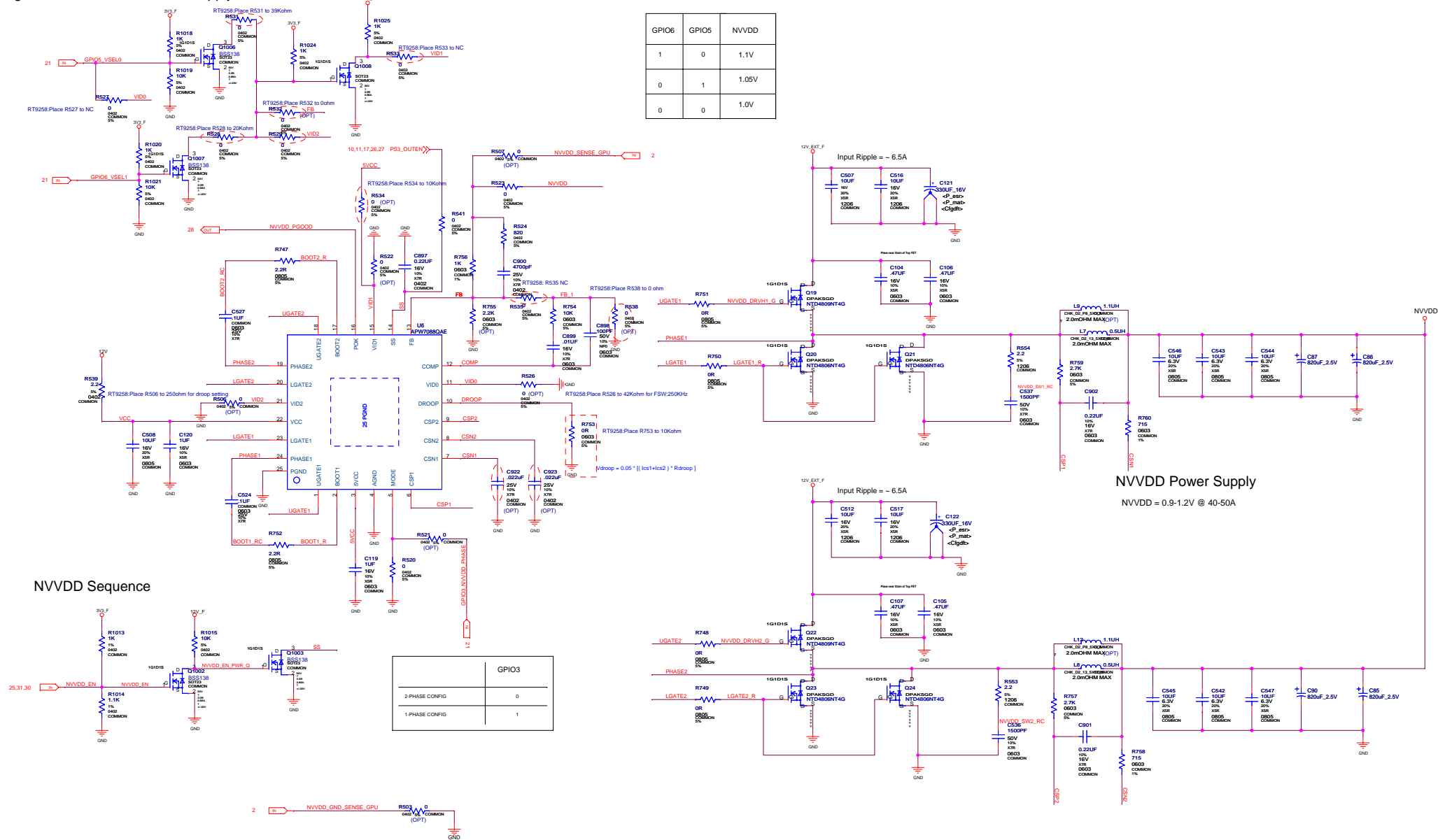
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GPI06	GPI05	NVDD
1	0	1.1V
0	1	1.05V
0	0	1.0V



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PAGE DETAIL	PS V: NVVDD Power Supply



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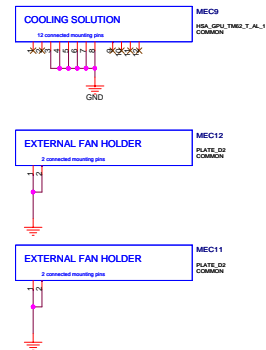
25	ENCLOSURE
----	-----------

AD7473 External Fan/Thermal Control

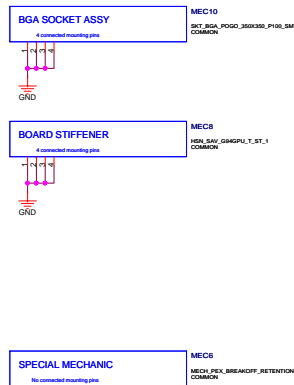
The diagram illustrates the AD7473 External Fan/Thermal Control circuit. It shows the internal components of the AD7473, including the XSPC16, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, and the external components like the fan, temperature sensor, and various resistors and capacitors. The circuit is powered by a 3.3V supply and ground. The output of the IC is connected to a fan. The

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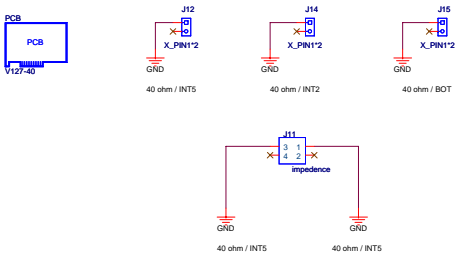
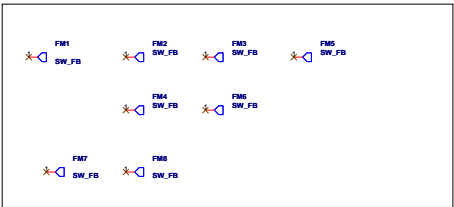
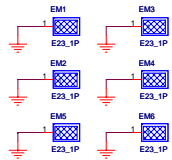
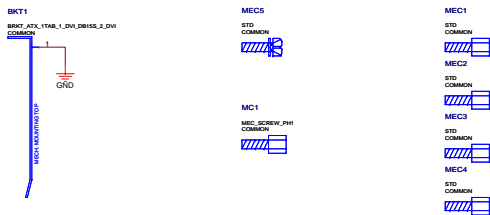
Thermal



Mechanical



Bracket



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Thermal, Mechanical, and Bracket

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