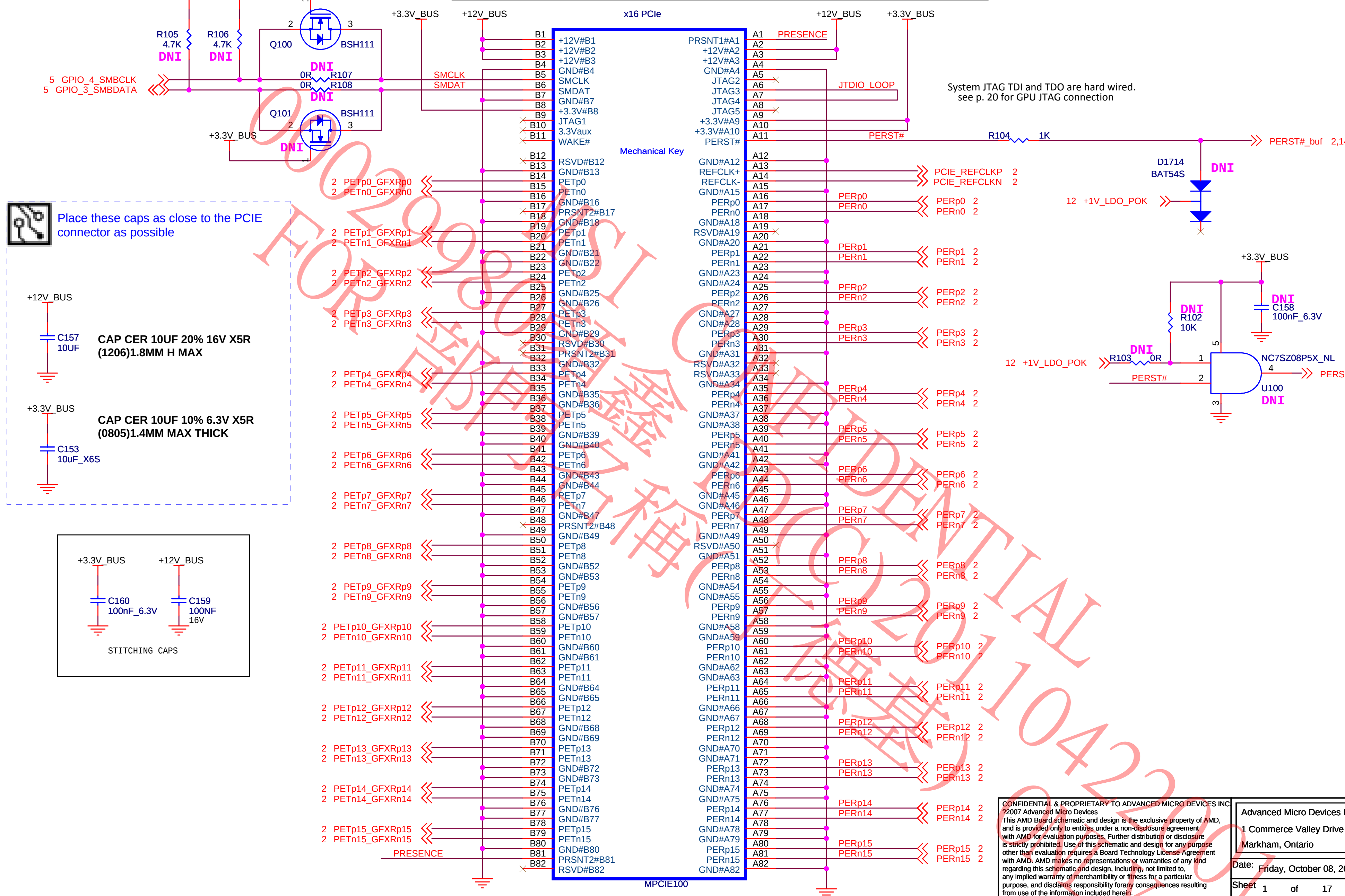
PCI-EXPRESS EDGE CONNECTOR



System JTAG TDI and TDO are hard wired.
see p. 20 for GPU JTAG connection

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
⏚	DIGITAL GROUND
▽	ANALOG GROUND
BUO	BRING UP ONLY

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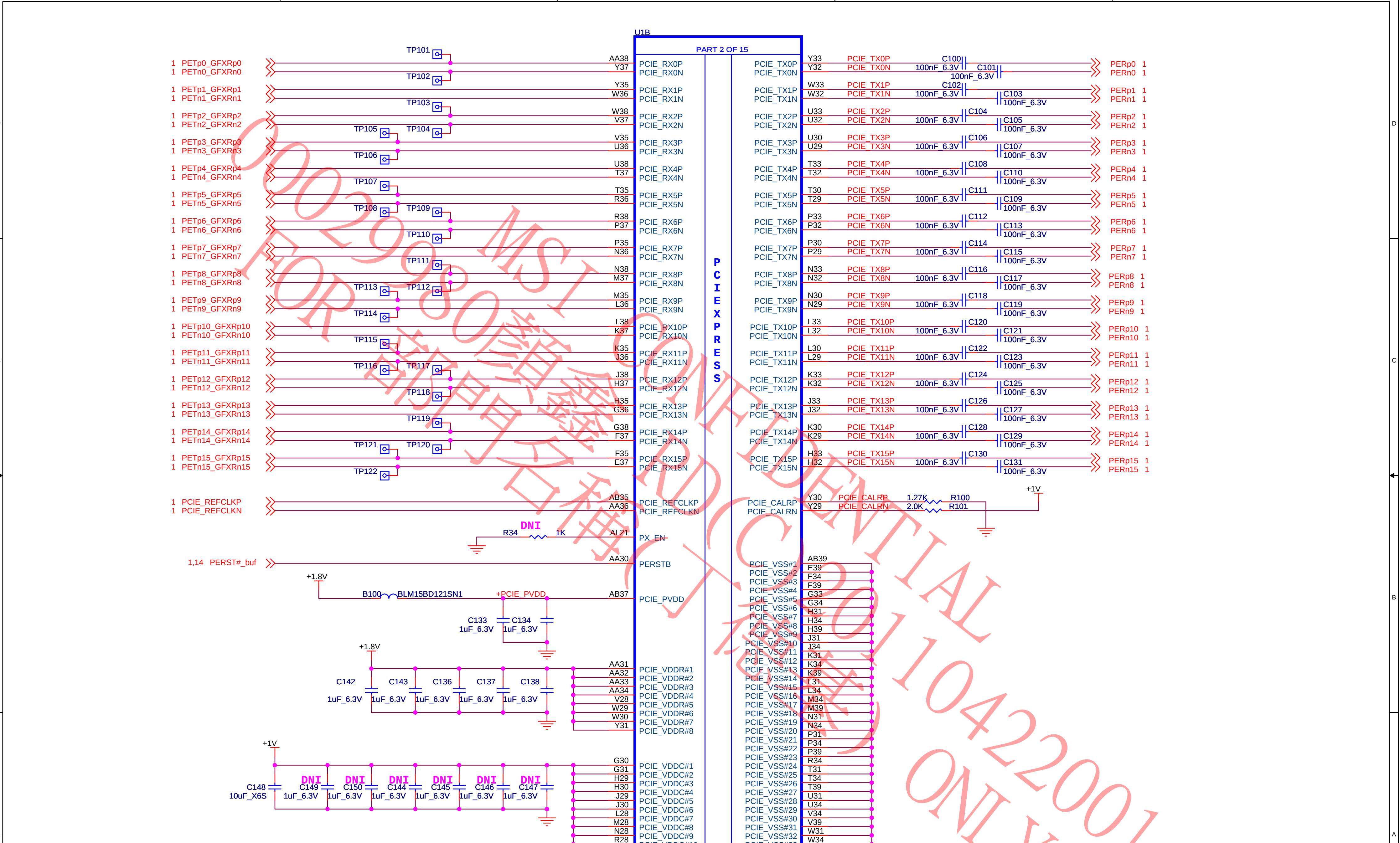

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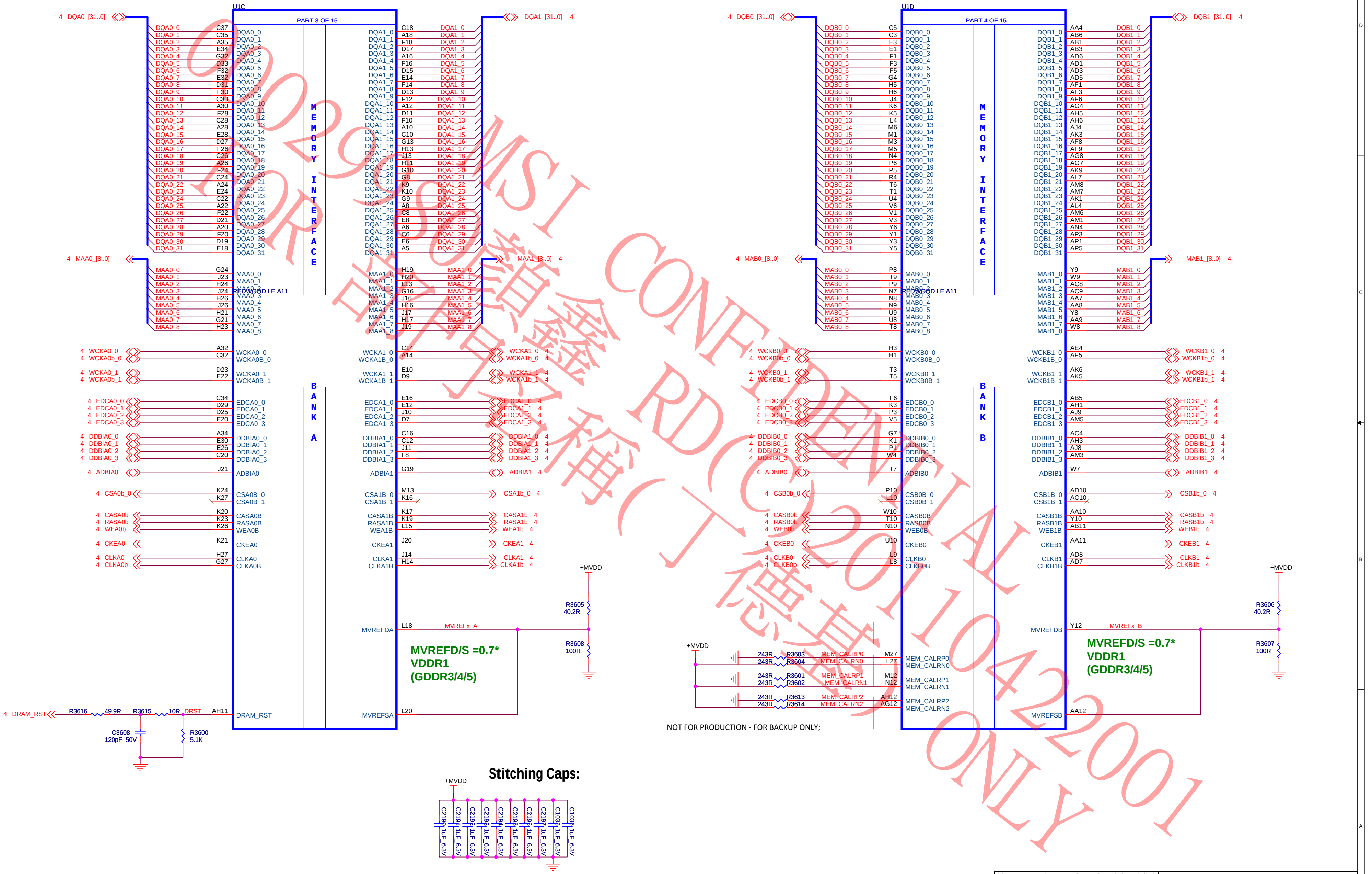
Title: RH Turks GDDR5 4pcs x 32 HDMI/DP+dDVI-D+VGD/DP

Doc No. 105-C24300-00B



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Title: RH Turks GDDR5 4pcs x 32 HDMI/DP+dDVI-D+VGD/DP

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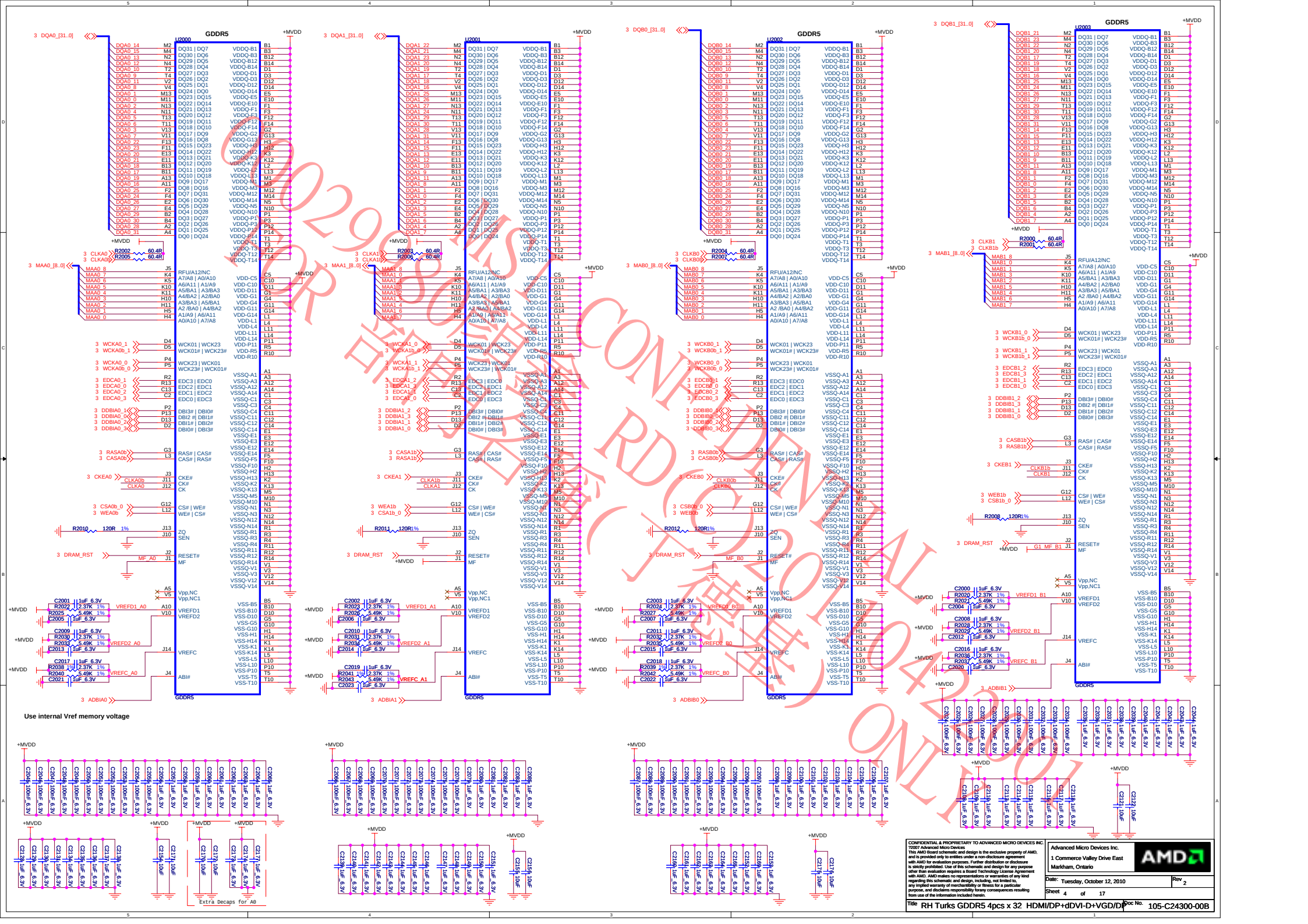

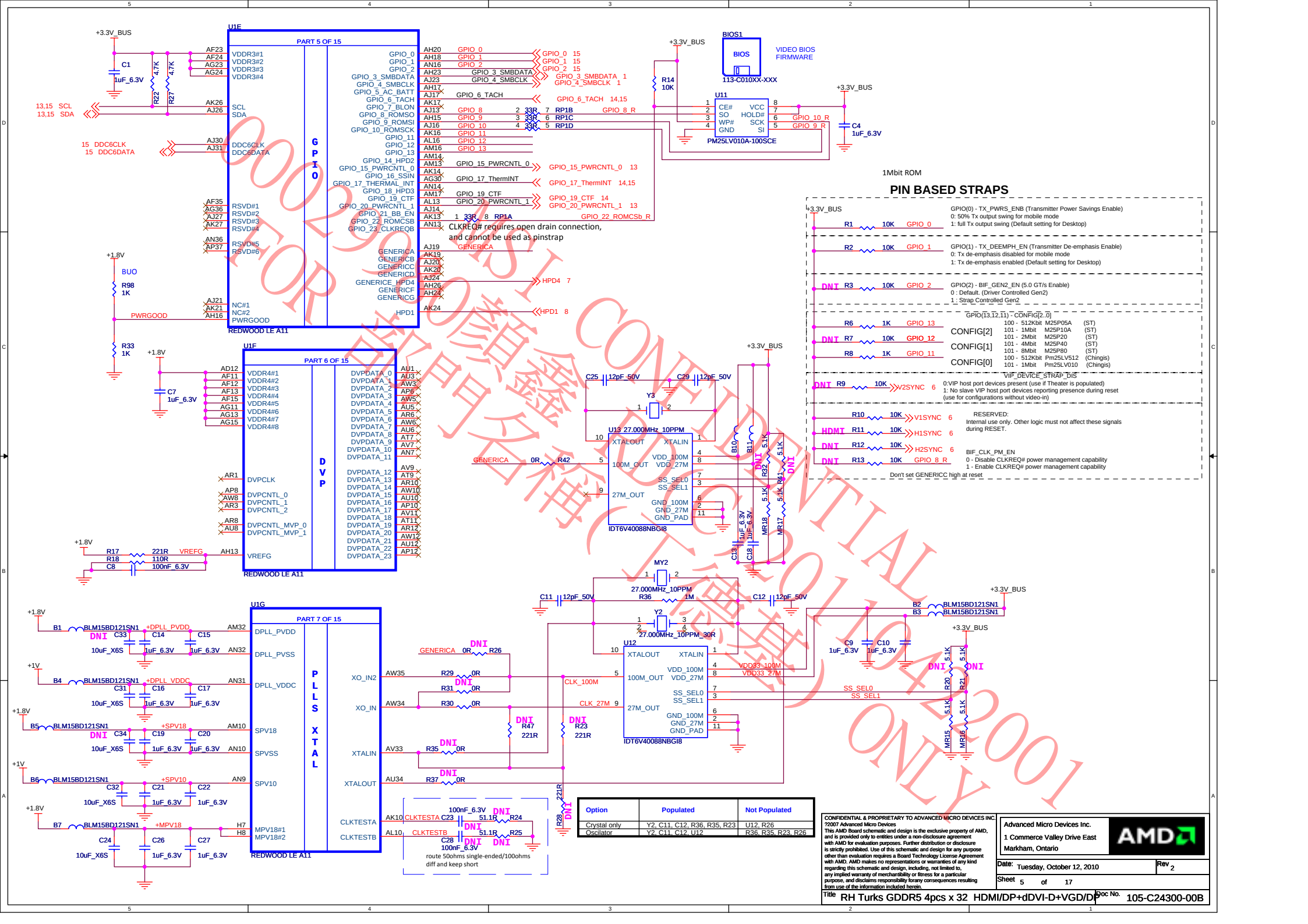
U1E
PART 5 OF 15
GPIO
REDWOOD LE A11
U1F
PART 6 OF 15
DVP
REDWOOD LE A11
U1G
PART 7 OF 15
PLS XTAL
REDWOOD LE A11
BIOS1
BIOS
VIDEO BIOS FIRMWARE
113-C010XX-XXX
U11
PM25LV010A-100SCE
U13 27.000MHz_10PPM
U12
IDT6V40088NBGI8
MY2
Y2
Y3
27.000MHz_10PPM_30R
CLKREQ# requires open drain connection, and cannot be used as pinstrap
route 50ohms single-ended/100ohms diff and keep short
1Mbit ROM
PIN BASED STRAPS
GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)
GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)
GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2
GPIO(13,12,11) - CONFIG[2..0]
CONFIG[2]
CONFIG[1]
CONFIG[0]
100 - 512Kbit M25P05A (ST)
101 - 1Mbit M25P10A (ST)
101 - 2Mbit M25P20 (ST)
101 - 4Mbit M25P40 (ST)
101 - 8Mbit M25P80 (ST)
100 - 512Kbit Pm25LV512 (Chingis)
101 - 1Mbit Pm25LV010 (Chingis)
VIP_DEVICE_STRAP_DIS
0:VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)
RESERVED:
Internal use only. Other logic must not affect these signals during RESET.
BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability
Don't set GENERICC high at reset
Option
Populated
Not Populated
Crystal only
Y2, C11, C12, R36, R35, R23
U12, R26
Oscillator
Y2, C11, C12, U12
R36, R35, R23, R26
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Title RH Turks GDDR5 4pcs x 32 HDMI/DP+dDVI-D+VGD/DP
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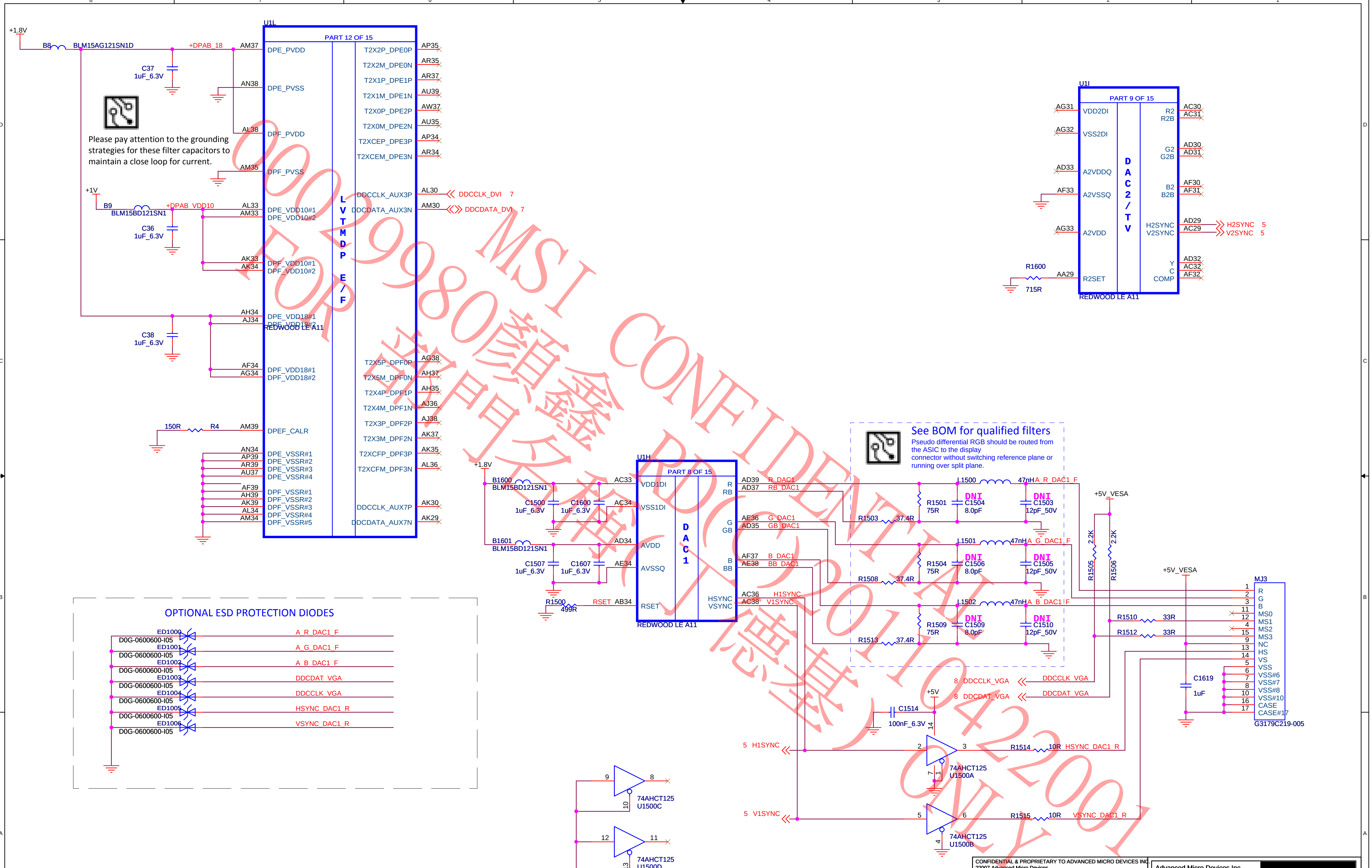

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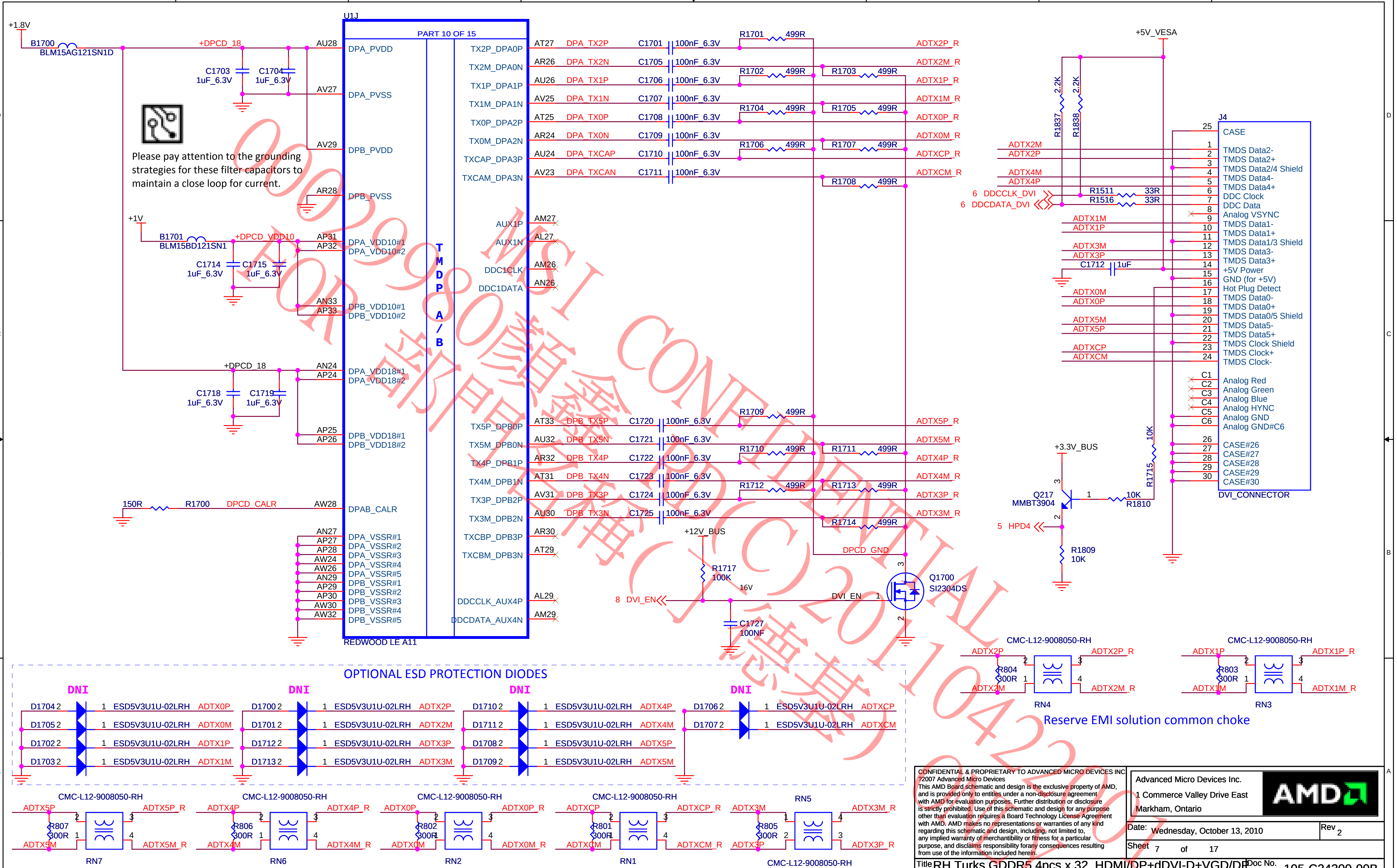
Title: RH Turks GDDR5 4pcs x 32 HDMI/DP+dDVI-D+VGA/DP

Doc No. 105-C24300-00B



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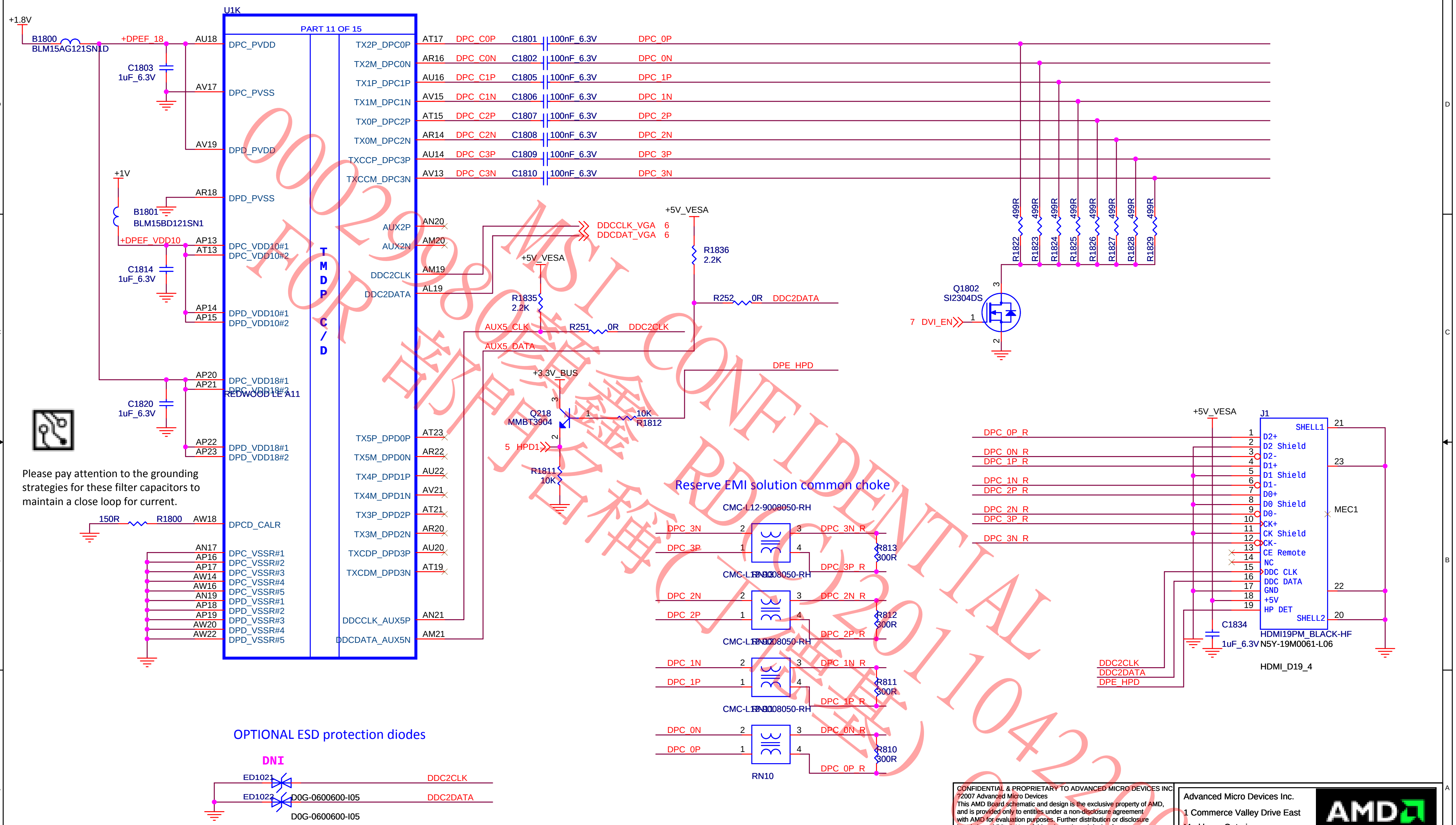
Title RH Turks GDDR5 4pcs x 32 HDMI/DP+dDVI-D+VGD/DP	Doc No. 105-C24300-00B



Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

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Title: RH Turks GDDR5 4pcs x 32 HDMI/DP+dDVI-D+VGD/DP

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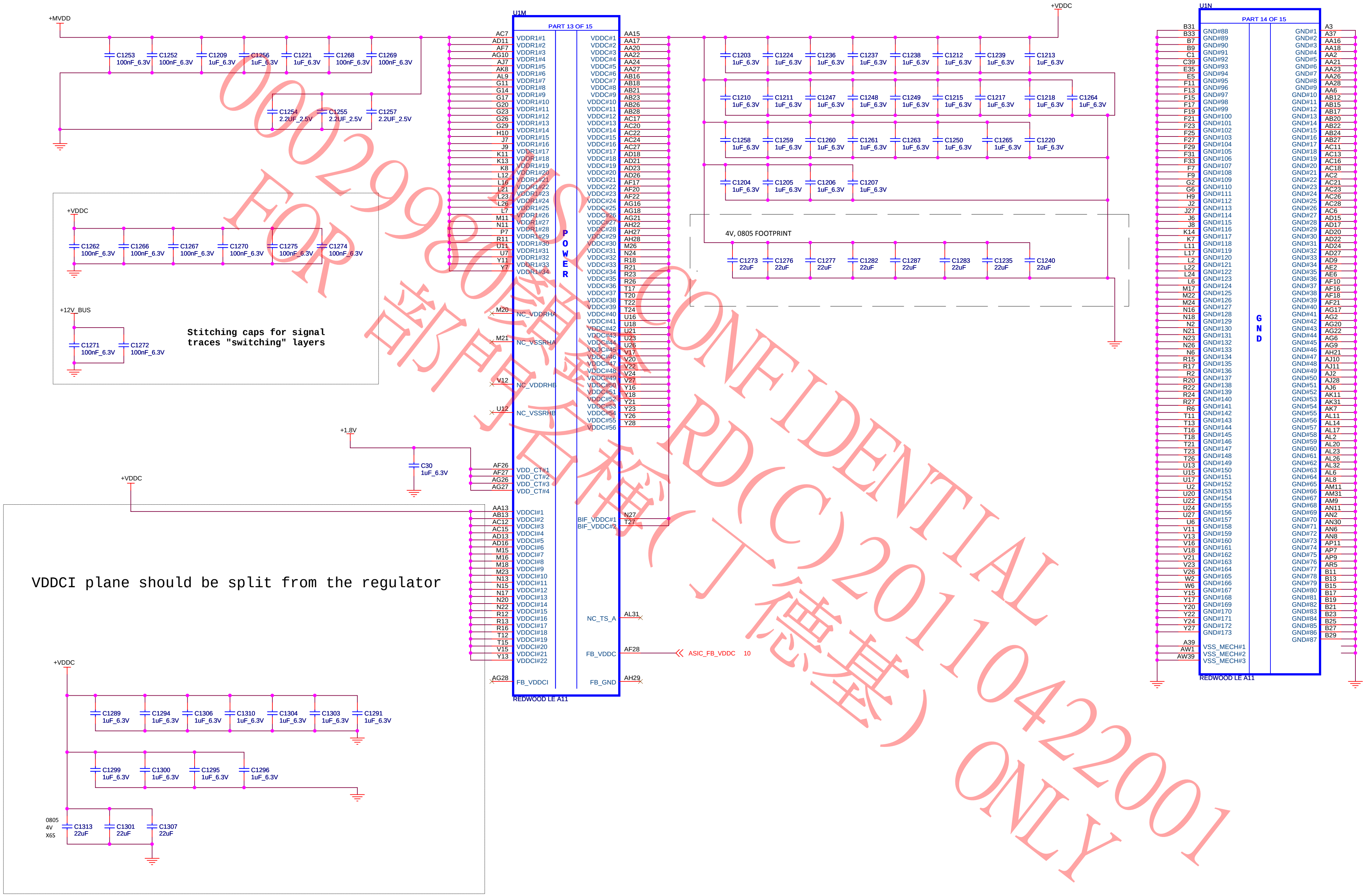

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Title: RH Turks GDDR5 4pcs x 32 HDMI/DP+dDVI-D+VGD/DP
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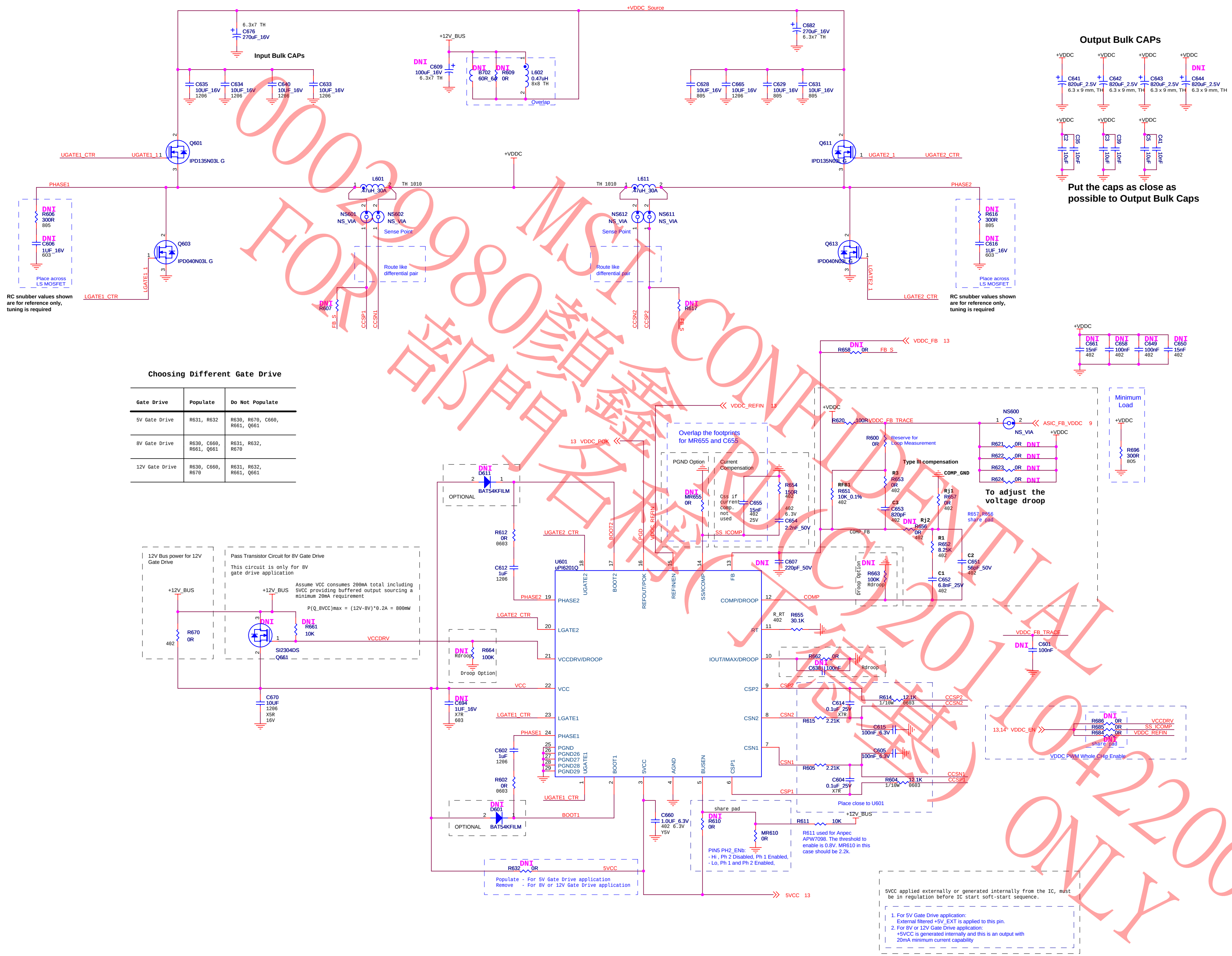

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661

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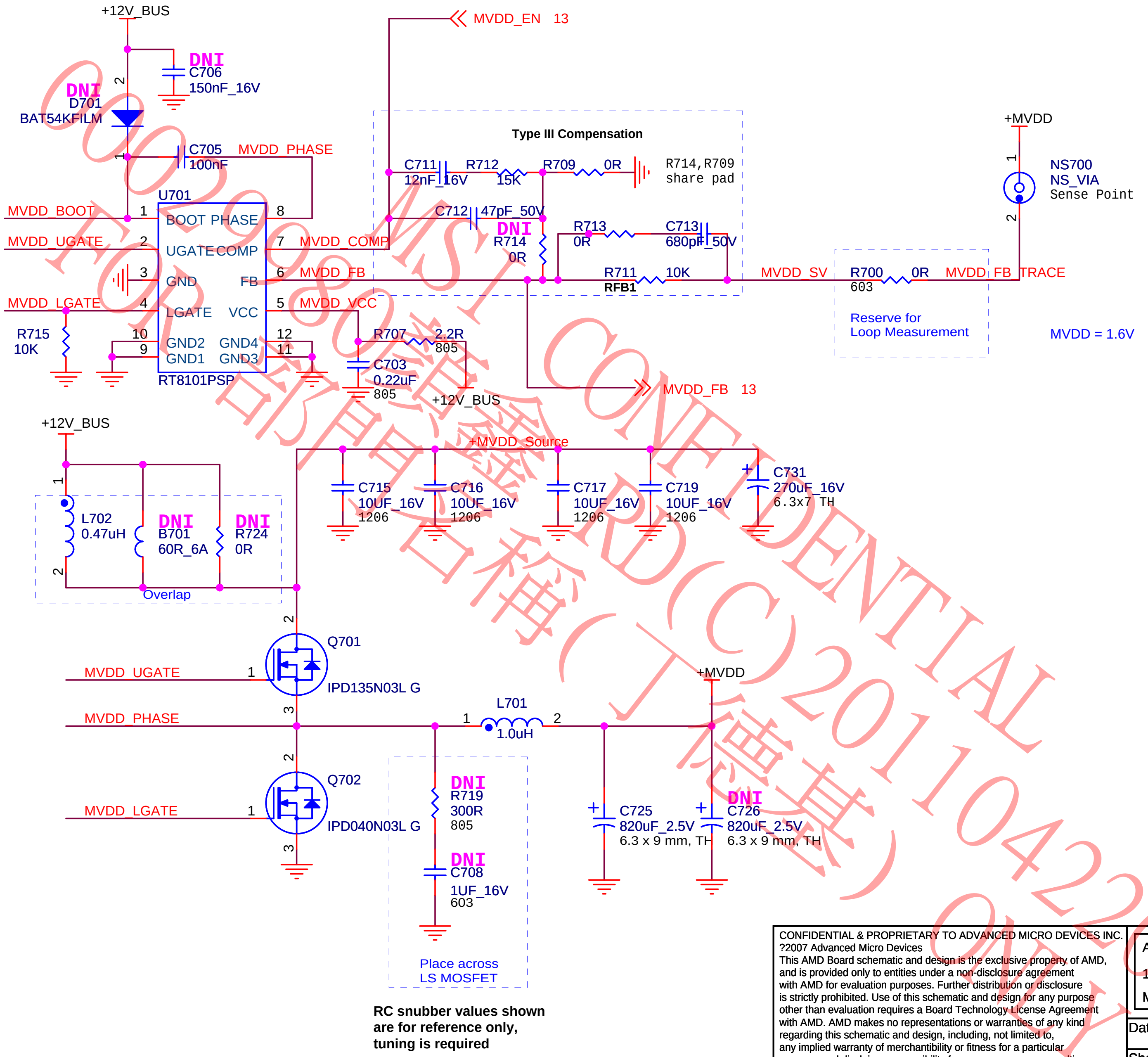

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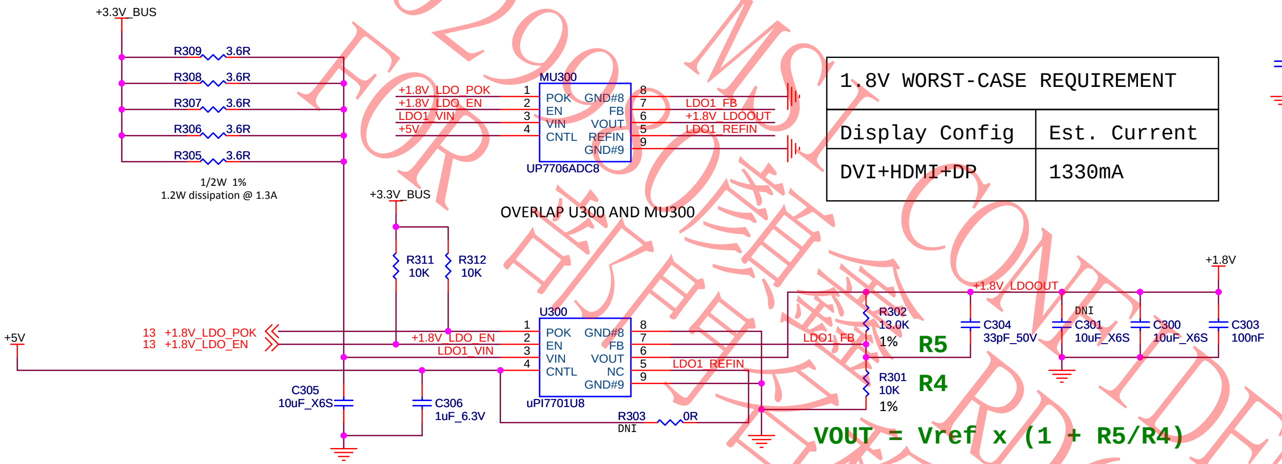
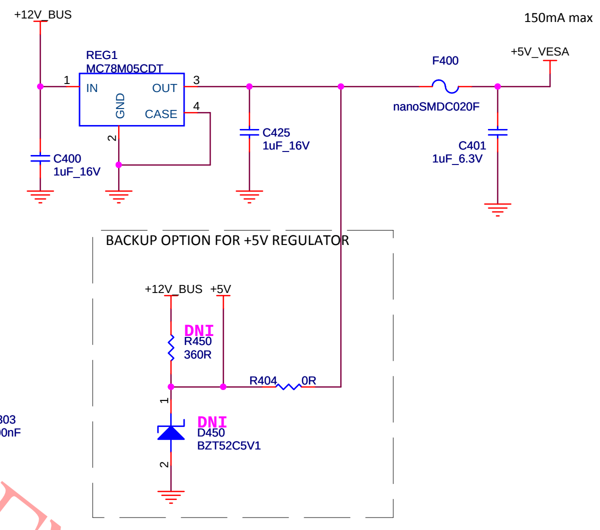
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

Regulator for +5V and +5V_VESA
Iout max = 150mA (VGA+DVI+HDMI)

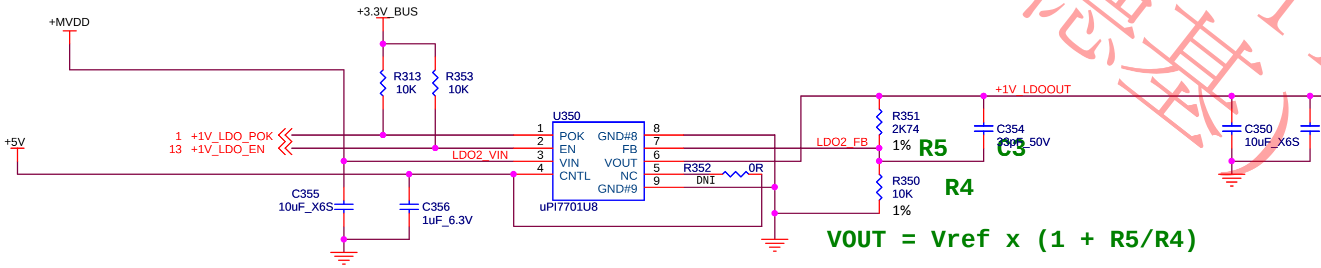
1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA





LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA



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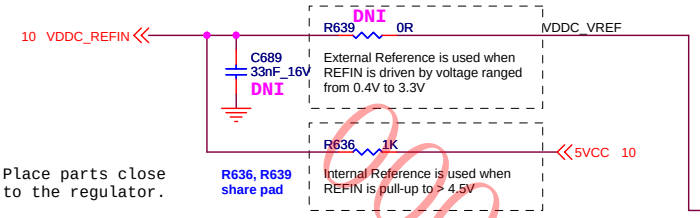
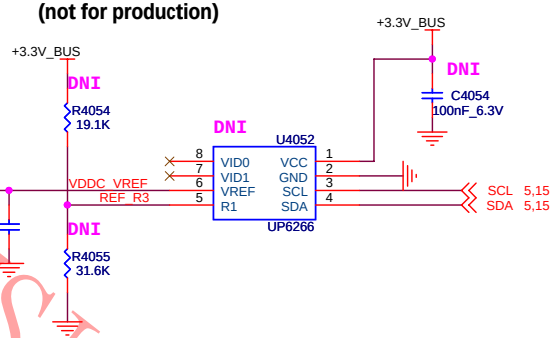
VDDC Reference Voltage Selection



VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

I2C VOLTAGE REFERENCE FOR VDDC (not for production)



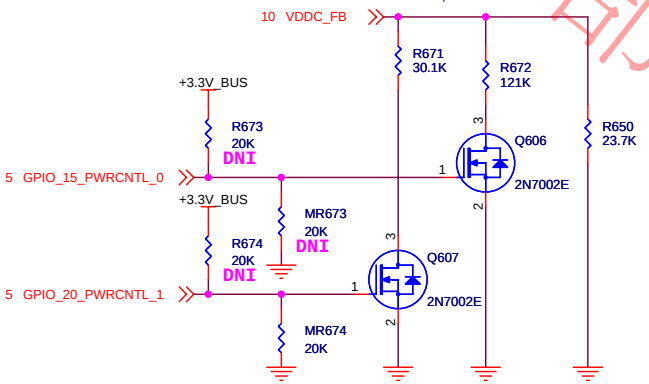
I2C ADDRESS: A6

VDDC Low Side Divider

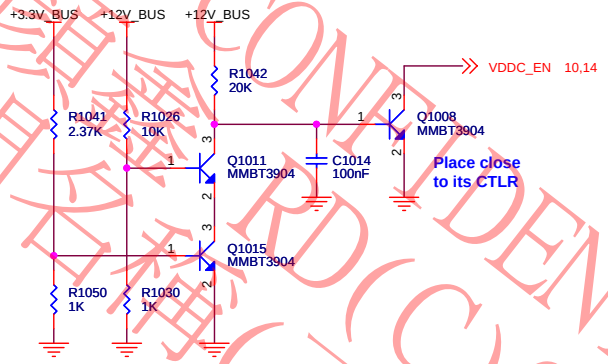
R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V.
Then this will set VDDC to a fixed value.

Low state 0.9V
Middle state 1.0V
High state 1.1V

Vref=0.6V
Top resistor of the divider is 10k

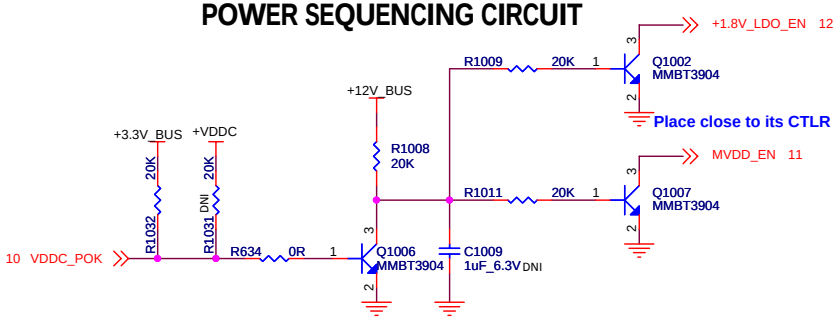


12V_BUS & 3V3_BUS POWER SEQUENCING



Install R1010 to gate 1V LDO with 1.8V LDO.

POWER SEQUENCING CIRCUIT



MVDD Low Side Divider

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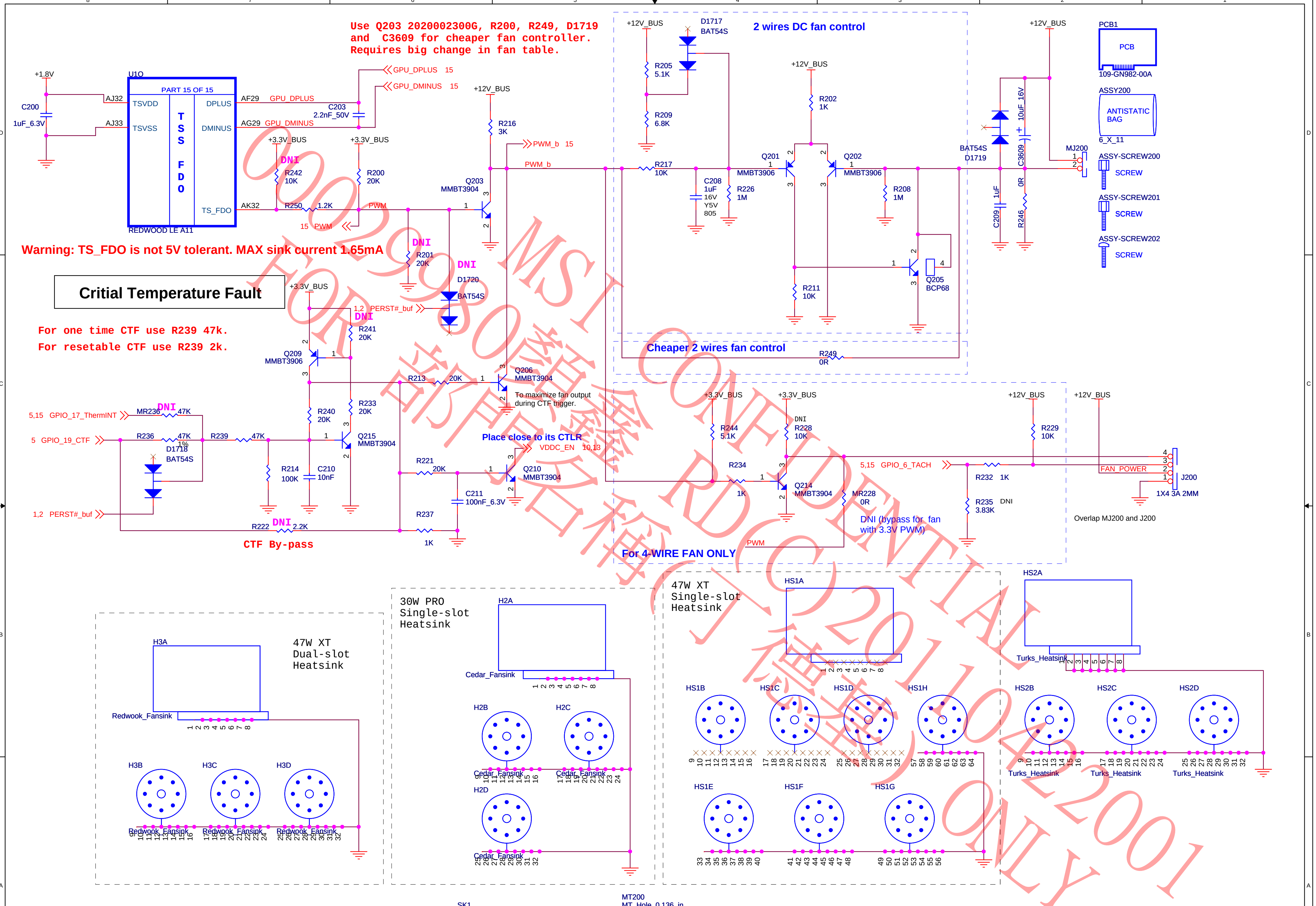

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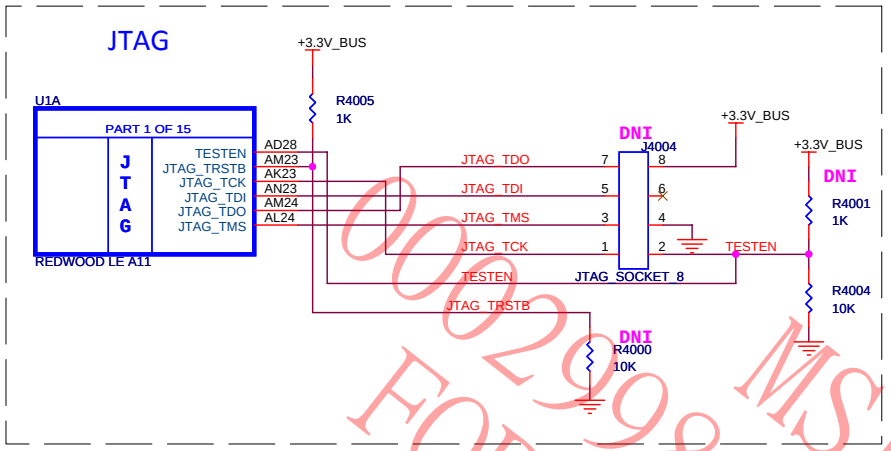

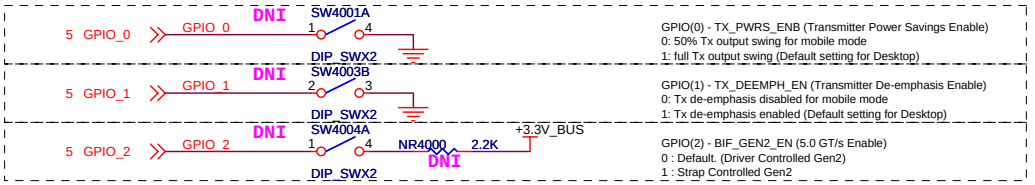

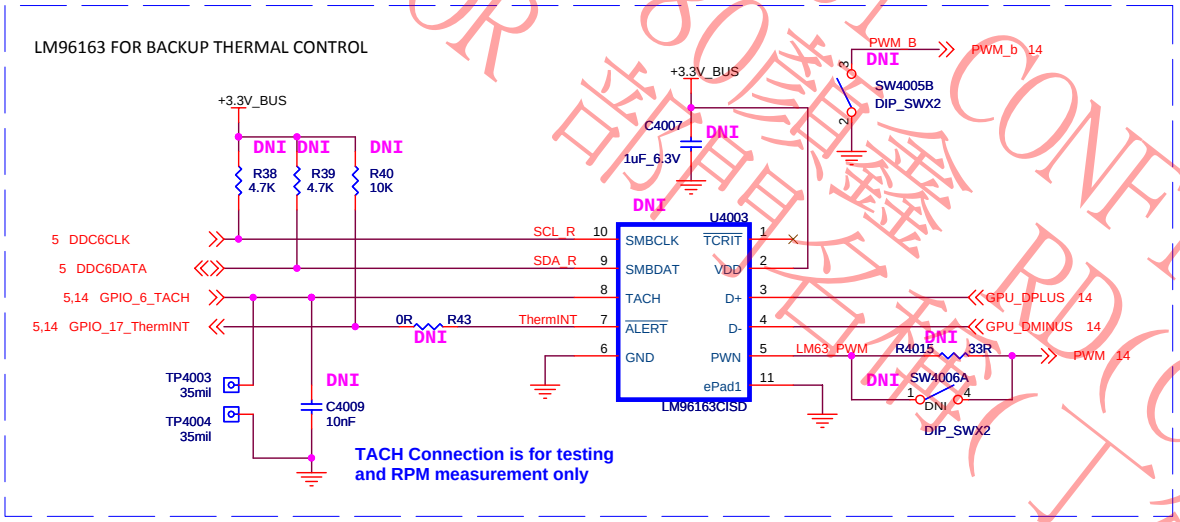

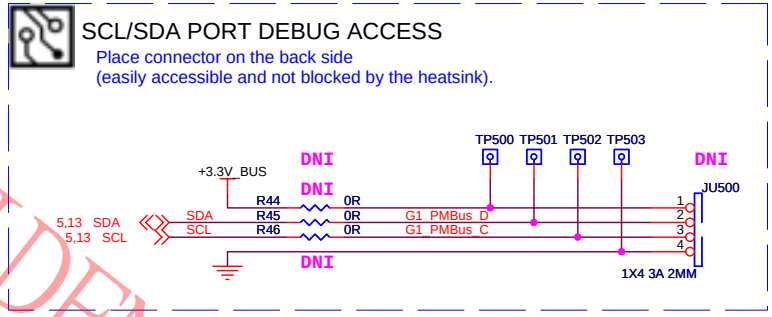

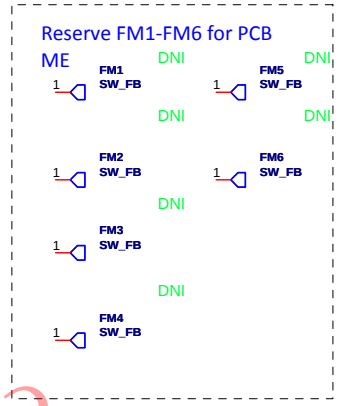

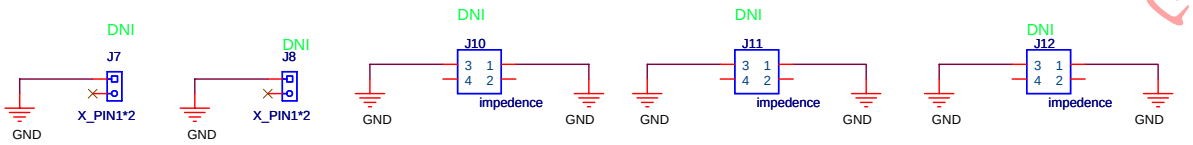

MEM Data
DQB0_20
BOTTOM
0.13MM / 45ohm +/- 10%
Reference L3 +MVDD

MEM Data
DQA1_31
TOP
0.13MM / 45ohm +/- 10%
Reference L2 GND

MEM CLK
WCKB0_0/WCKB0b_0
TOP
0.13MM/0.18MM / 80ohm +/- 10%
Reference L2 GND

HDMI/DVI J1 TMDS signals
DPC_C2N/DPC_C2P
Top
0.1016MM/0.14MM / 85ohm +/- 10%
Reference L2 GND

PEX_PCEI
PCIE_TX6P/PCIE_TX6N
BOTTOM
0.1016MM/0.14MM / 85ohm +/- 10%
Reference L2 GND

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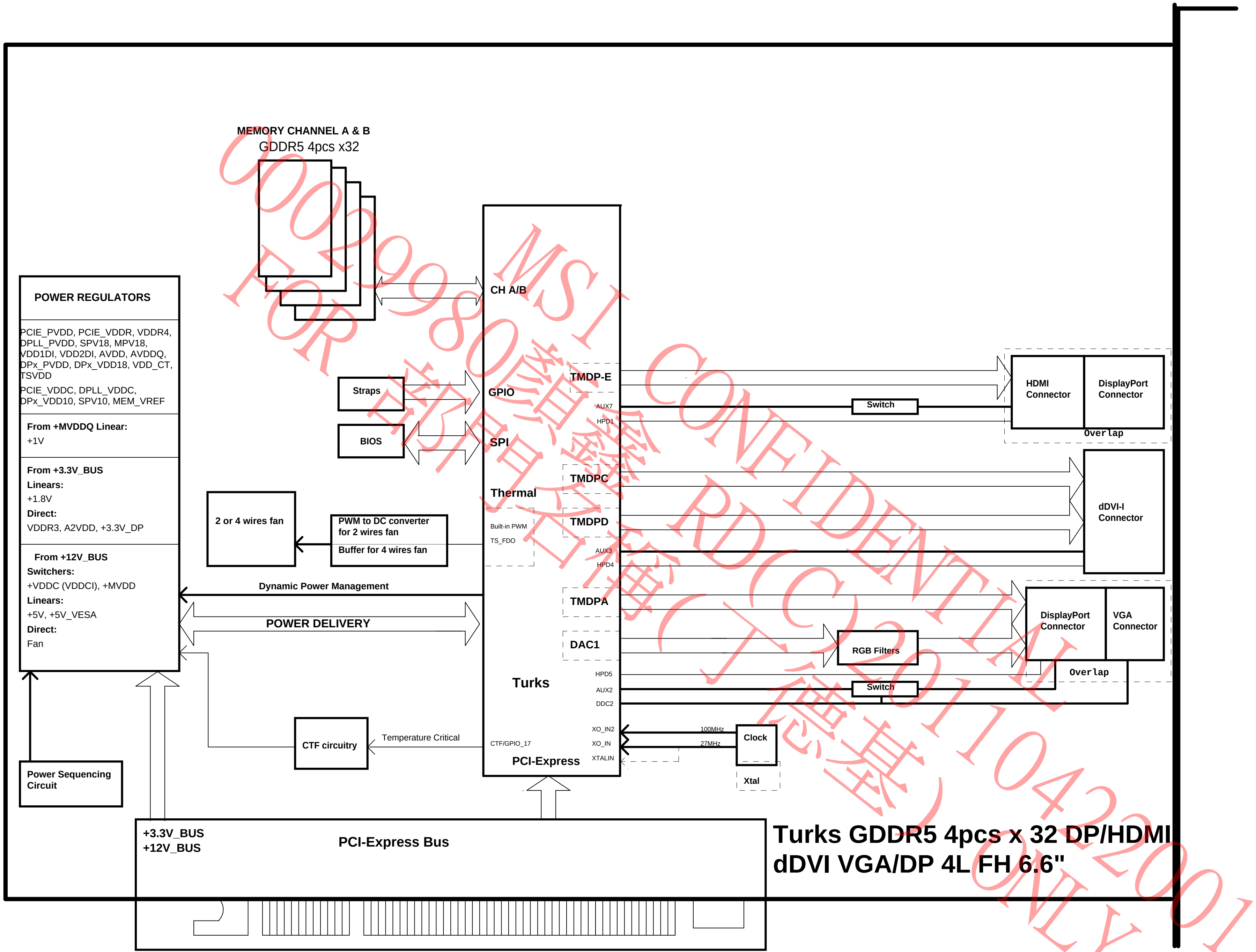

Turks GDDR5 4pcs x 32 DP/HDMI dDVI VGA/DP 4L FH 6.6"

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5	4	3	2	1

AMD

Title

RH Turks GDDR5 4pcs x 32 HDMI/DP+dDVI-D+VGD/DP

Schematic No.

105-C24300-00B

Date:

Friday, October 08, 2010

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00A	00A	14/05/2010	1)Based on: C240-00B 2) Changed placement of VDDC and MVDD regulators to accomodate cheapper fansink
00B	00B	11/06/2010	1) Changed layout of VDDC to add GND vias 2) moved cap on SPV10 3) added resistor R241 to CTF circuitry 4) added capacitors C644 (VDDC) and C31..C34 5) added R47 to feed 27 MHz into XTALIN
00C	00C	27/07/2010	1) added extra pull-up R242 on TS_FD0 output; 2) added C211 to delay VDDC shutdown of VTF; 3) added R611- provision for Anpec APW7098 VDDC regulator; 4) added ceramic caps to output bulk caps to reduce the OCP

5	4	3	2	1