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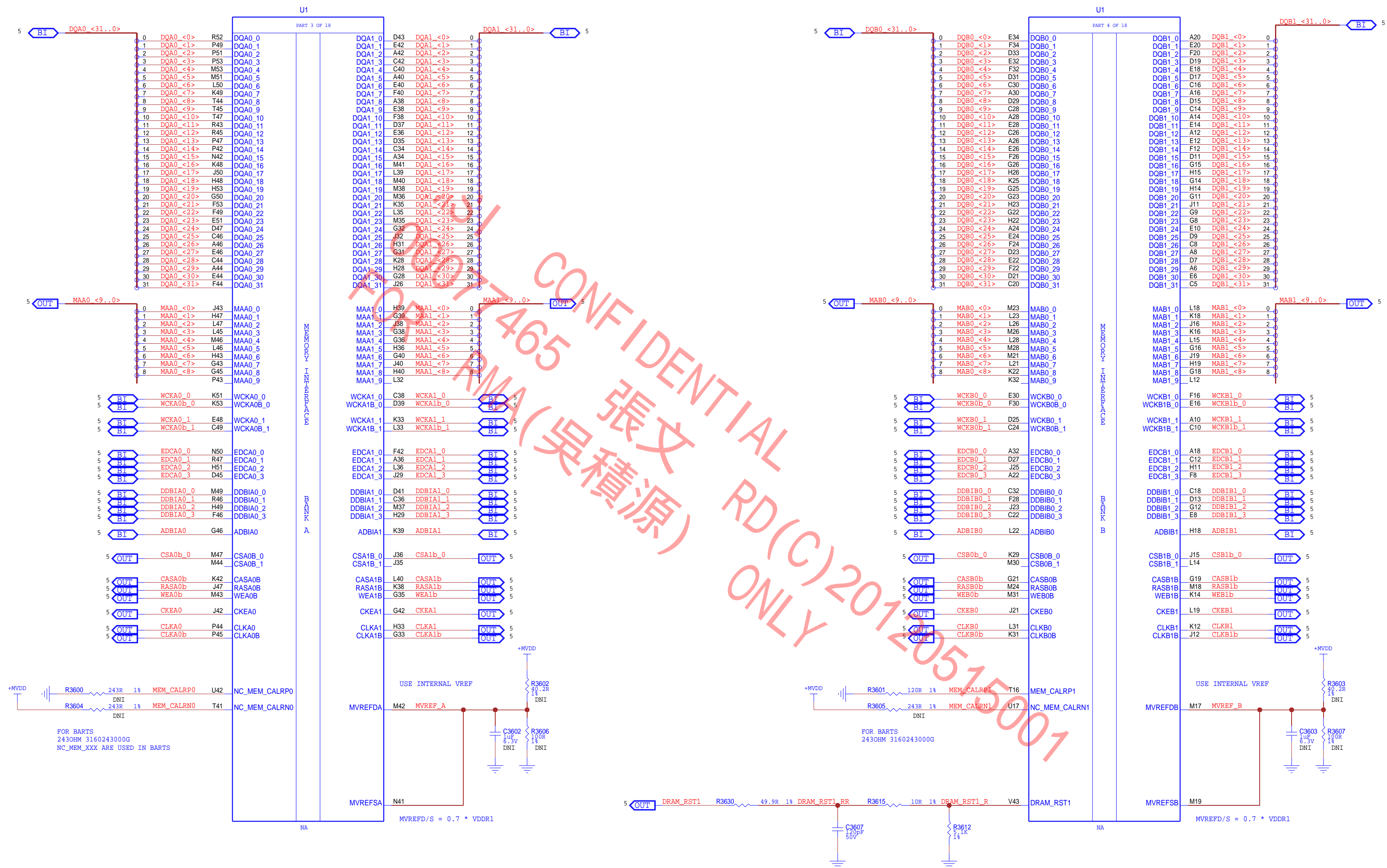
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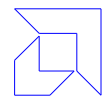
TITLE: Pitcairn GDDR5 x32

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(3) PITCAIRN MEM INTERFACE CH AB



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SHEET: PITCAIRN MEM CH AB

DATE: Thu Dec 01 18:38:22 2011

REV: 1.0

SHEET NUMBER: 3 OF 22

DOCUMENT NUMBER: 105-C401xx-00

TITLE:

Pitcairn GDDR5 x32

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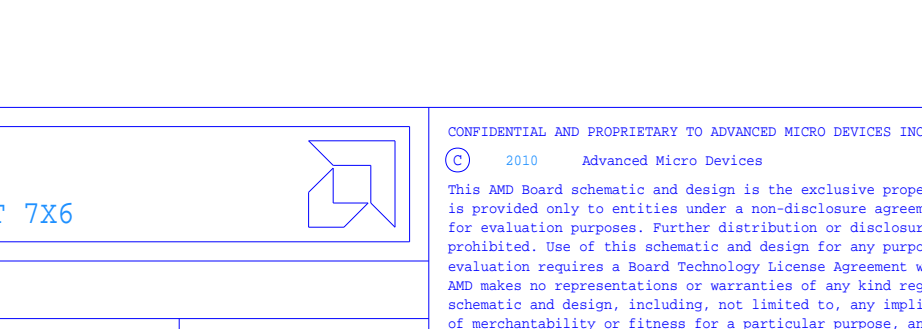
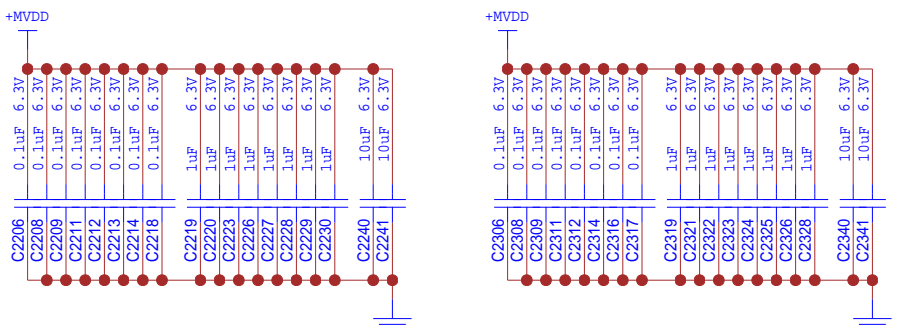
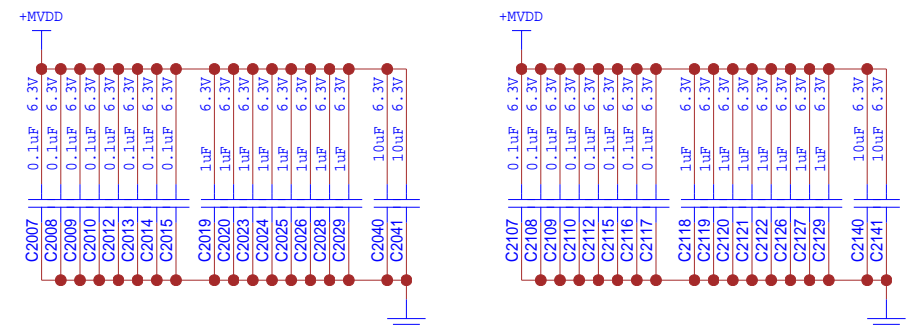
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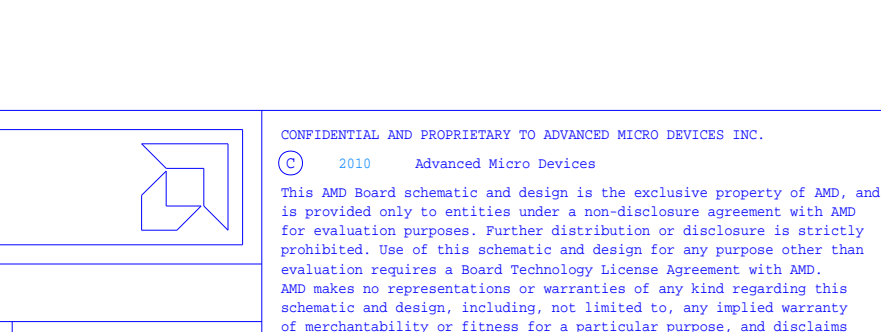
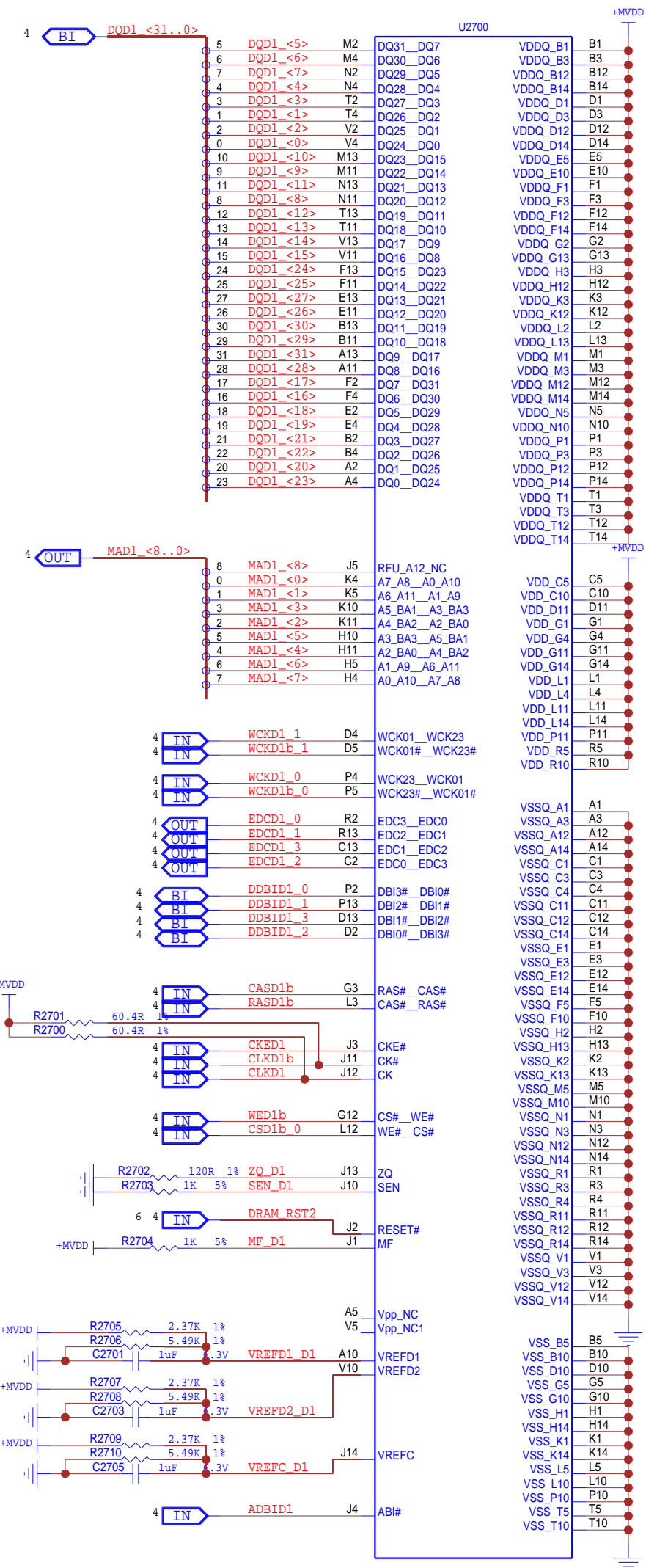
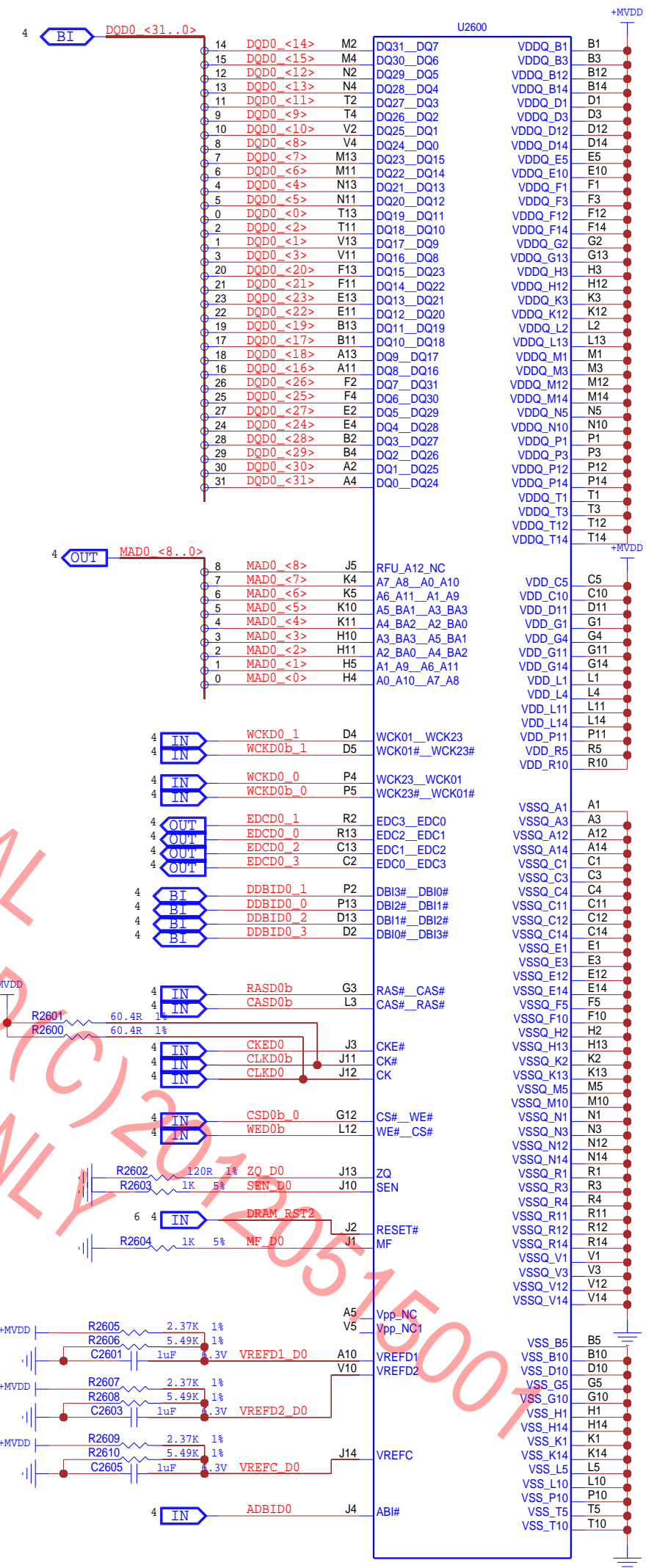
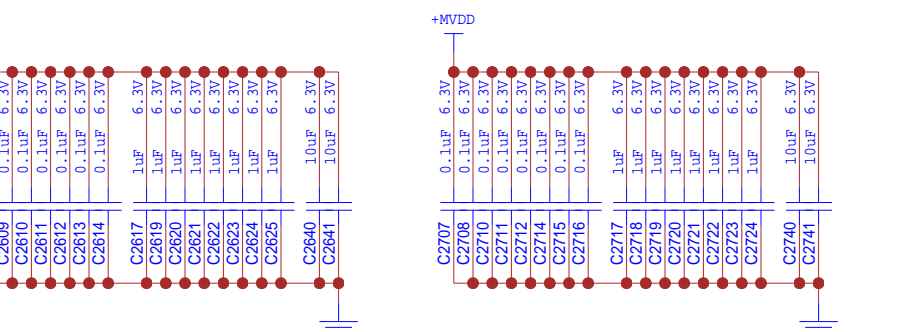
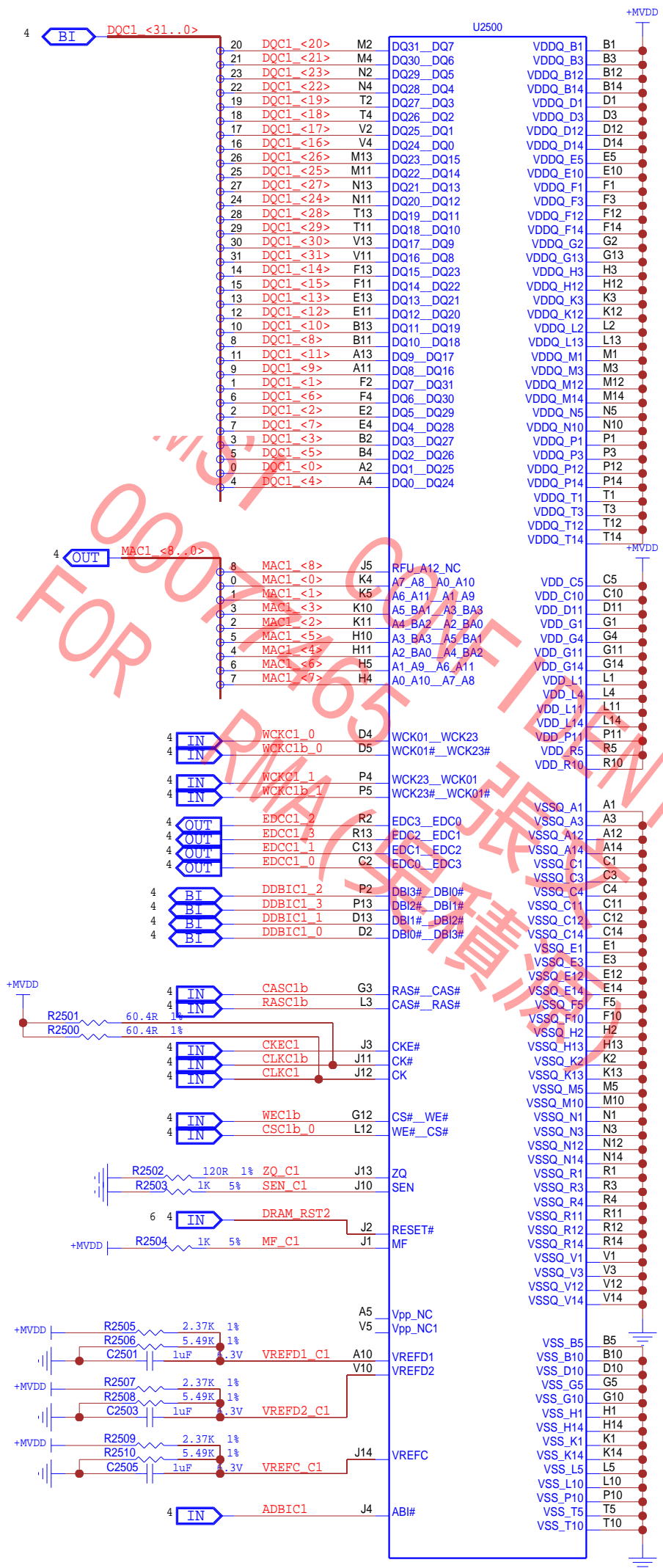
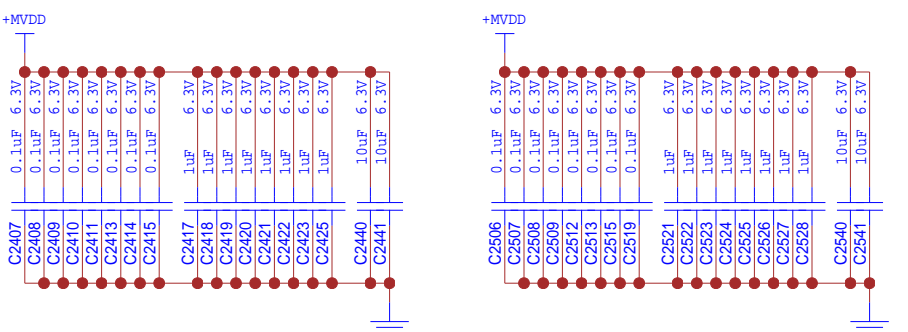
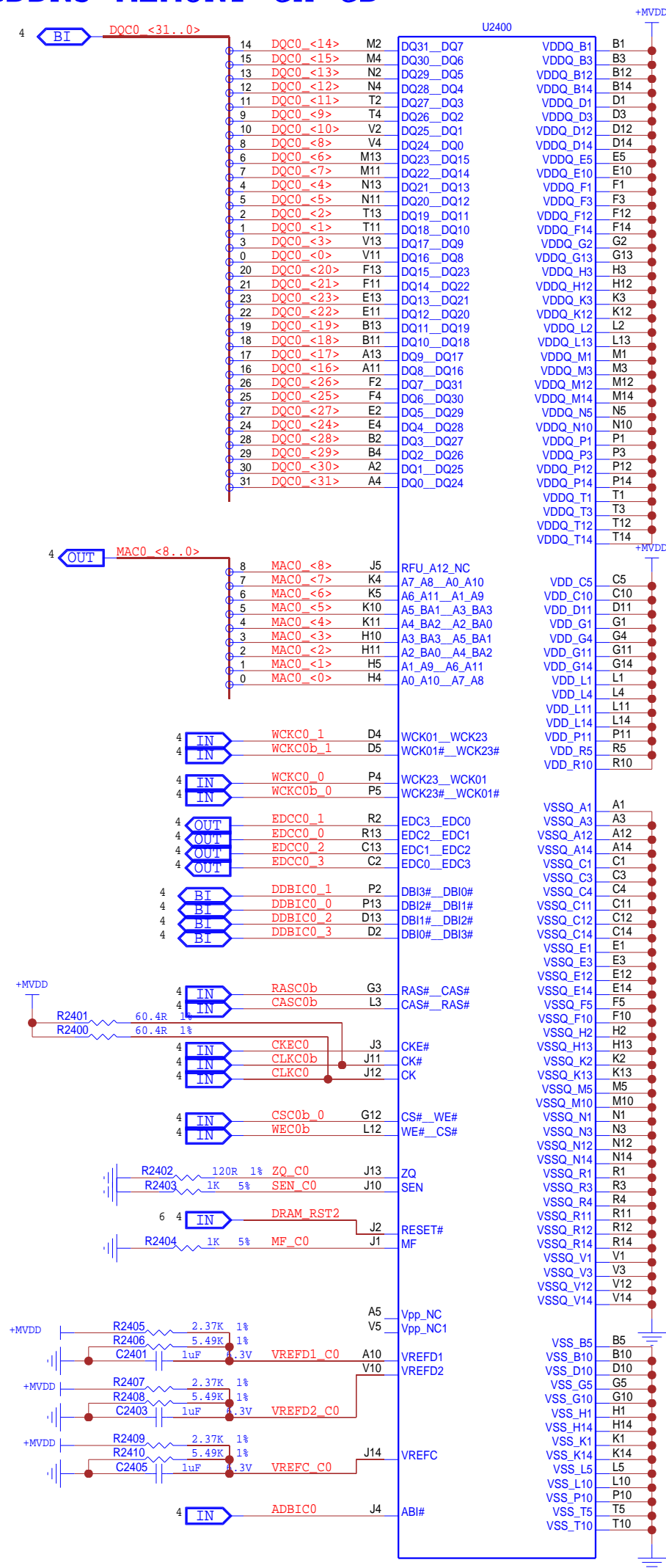
DOCUMENT NUMBER: 105-C401xx-00

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Pitcairn GDDR5 x32

(6) GDDR5 MEMORY CH CD



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SHEET: GDDR5 MEM CH CD

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DOCUMENT NUMBER: 105-C401xx-00

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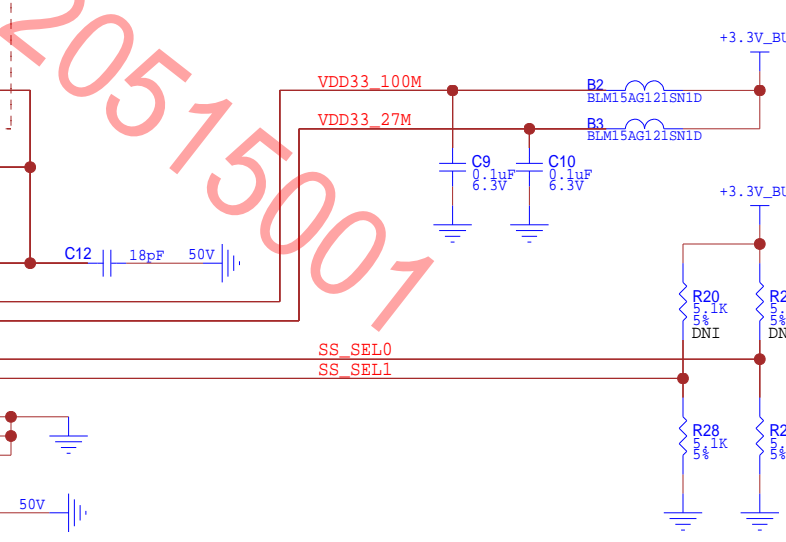
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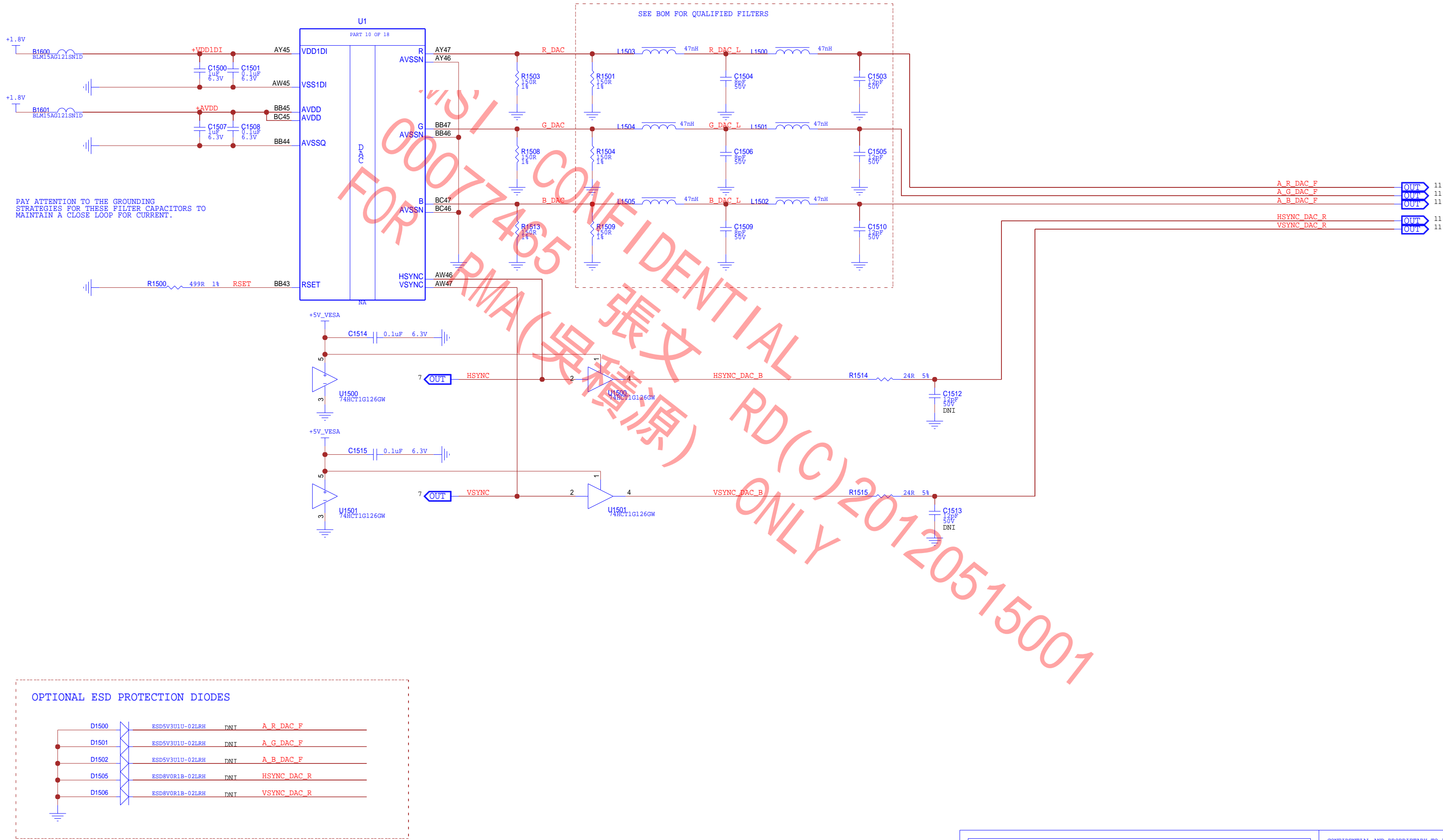
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DATE: Thu Dec 01 18:38:26 2011

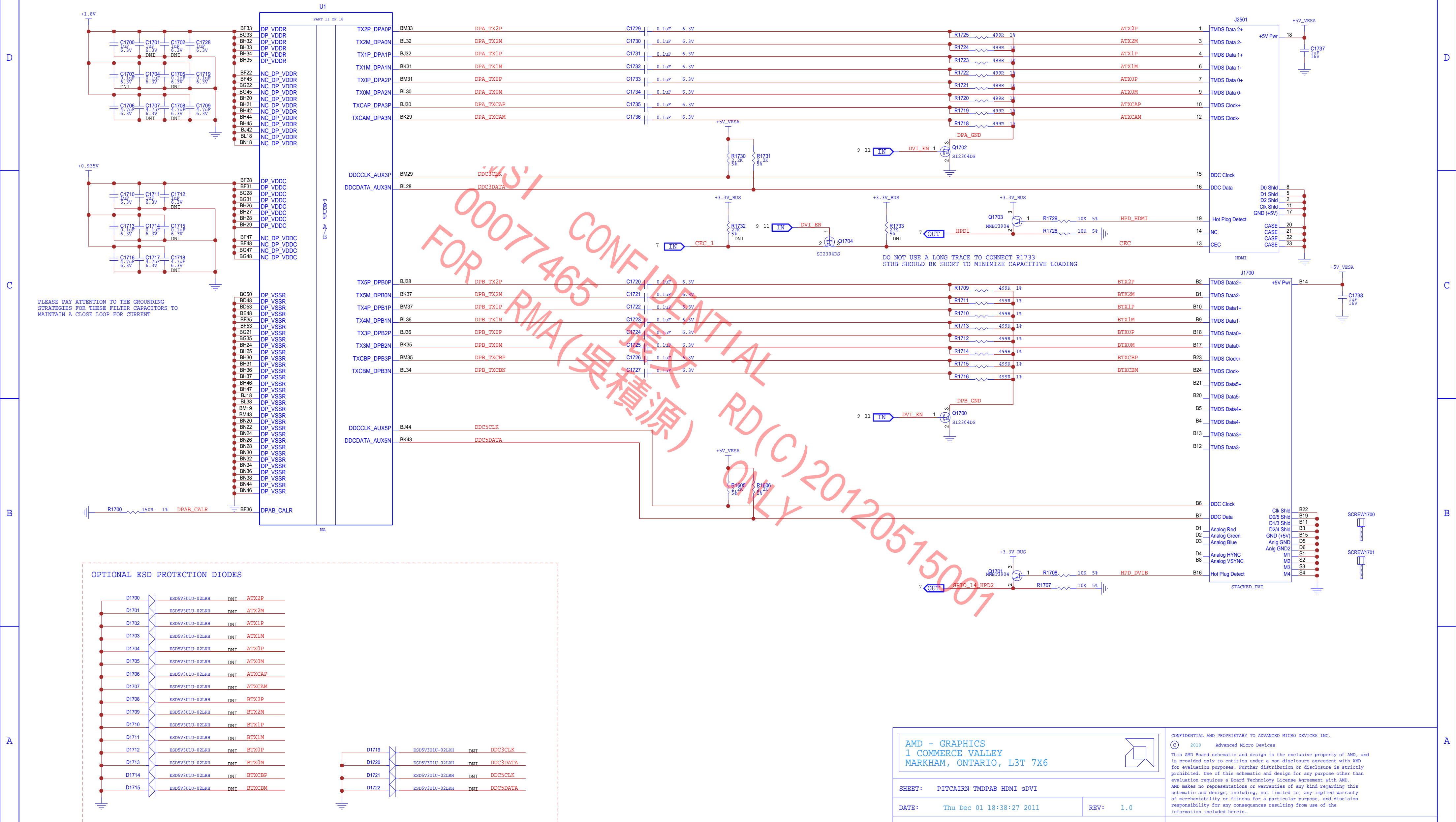
DOCUMENT NUMBER: 105-C401xx-00

TITLE: Pitcairn GDDR5 x32

(8) PITCAIRN DAC



(9) PITCAIRN TMDP AB HDMI sDVI



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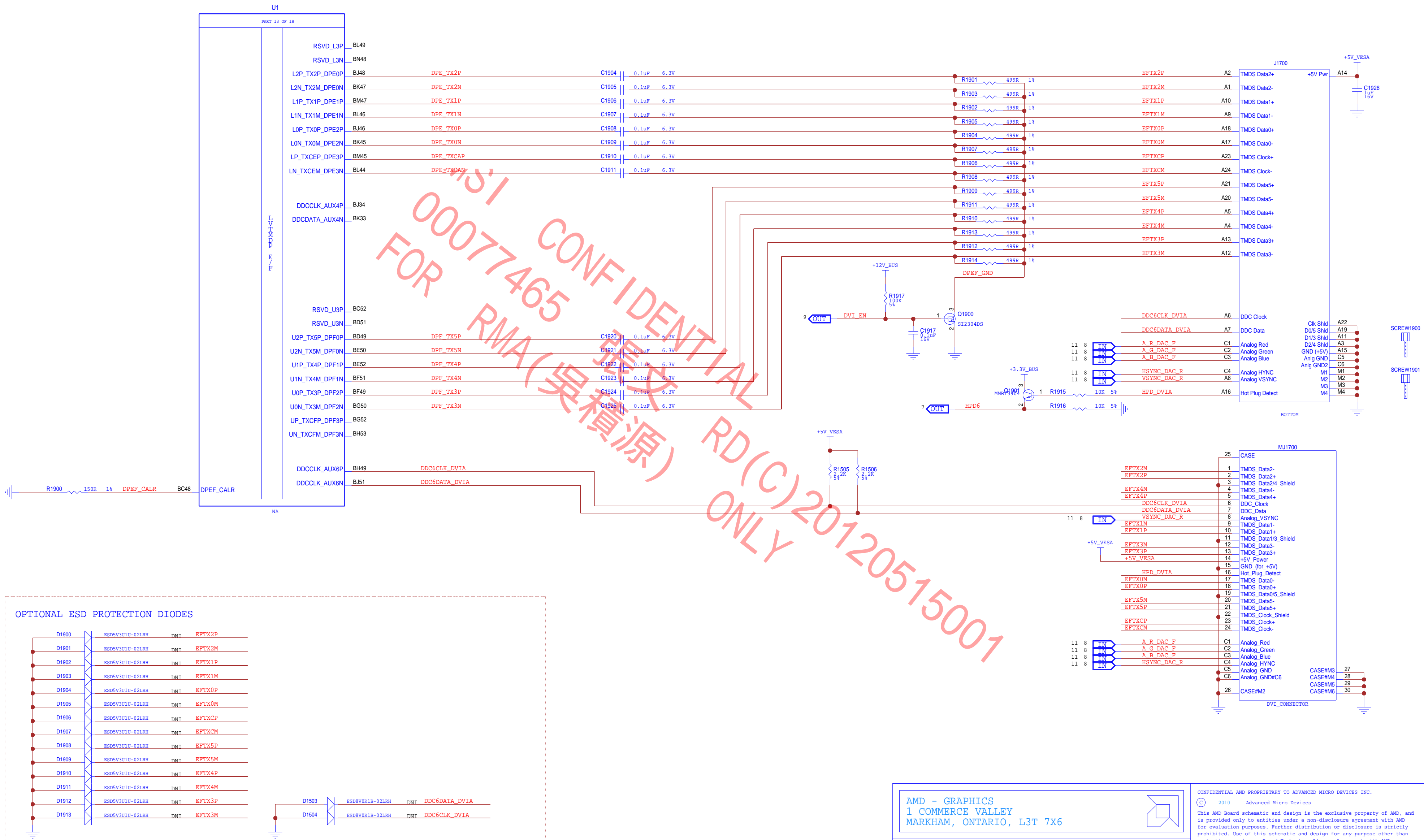


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TITLE: Pitcairn GDDR5 x32

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(11) PITCAIRN LVTMDP EF dDVI



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SHEET: PITCAIRN LVTMDP EF dDVI

DATE: Thu Dec 01 18:38:27 2011

SHEET NUMBER: 11 OF 22

DOCUMENT NUMBER: 105-C401xx-00

REV: 1.0

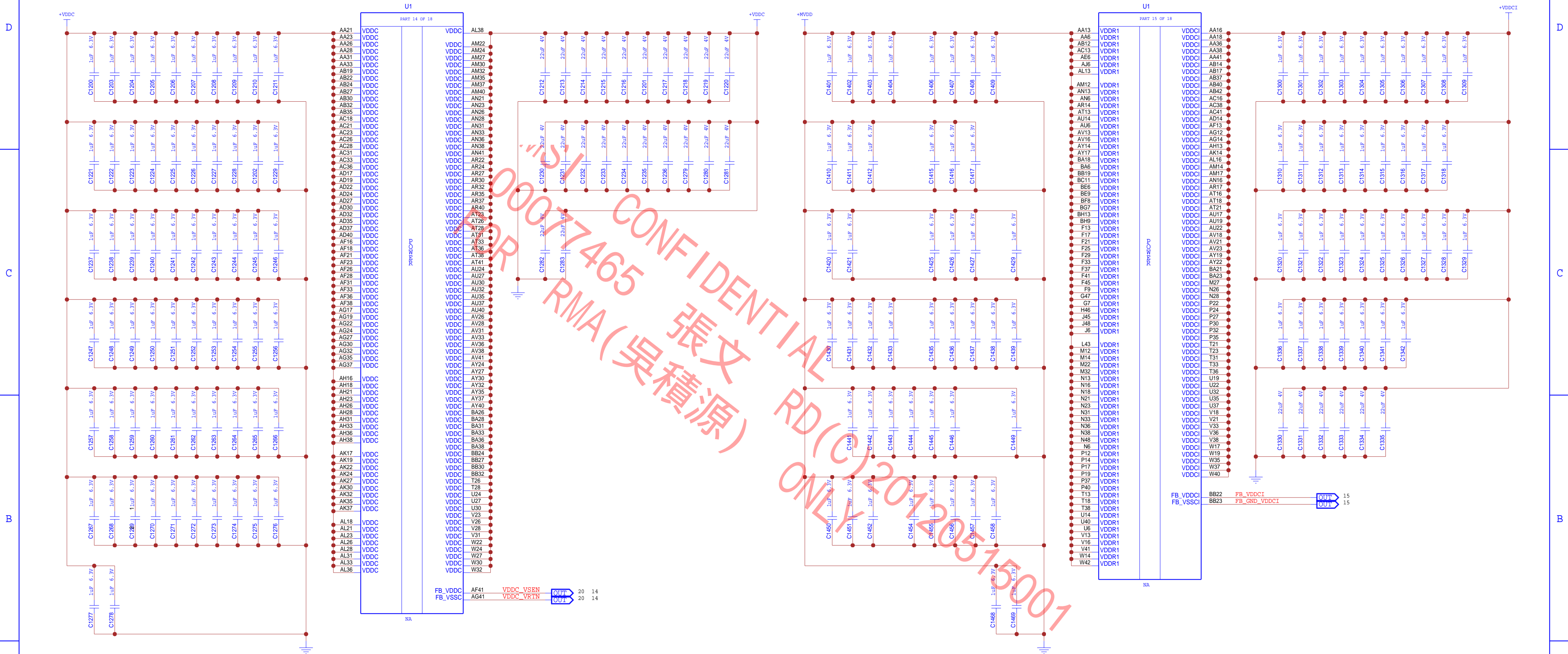
TITLE: Pitcairn GDDR5 x32

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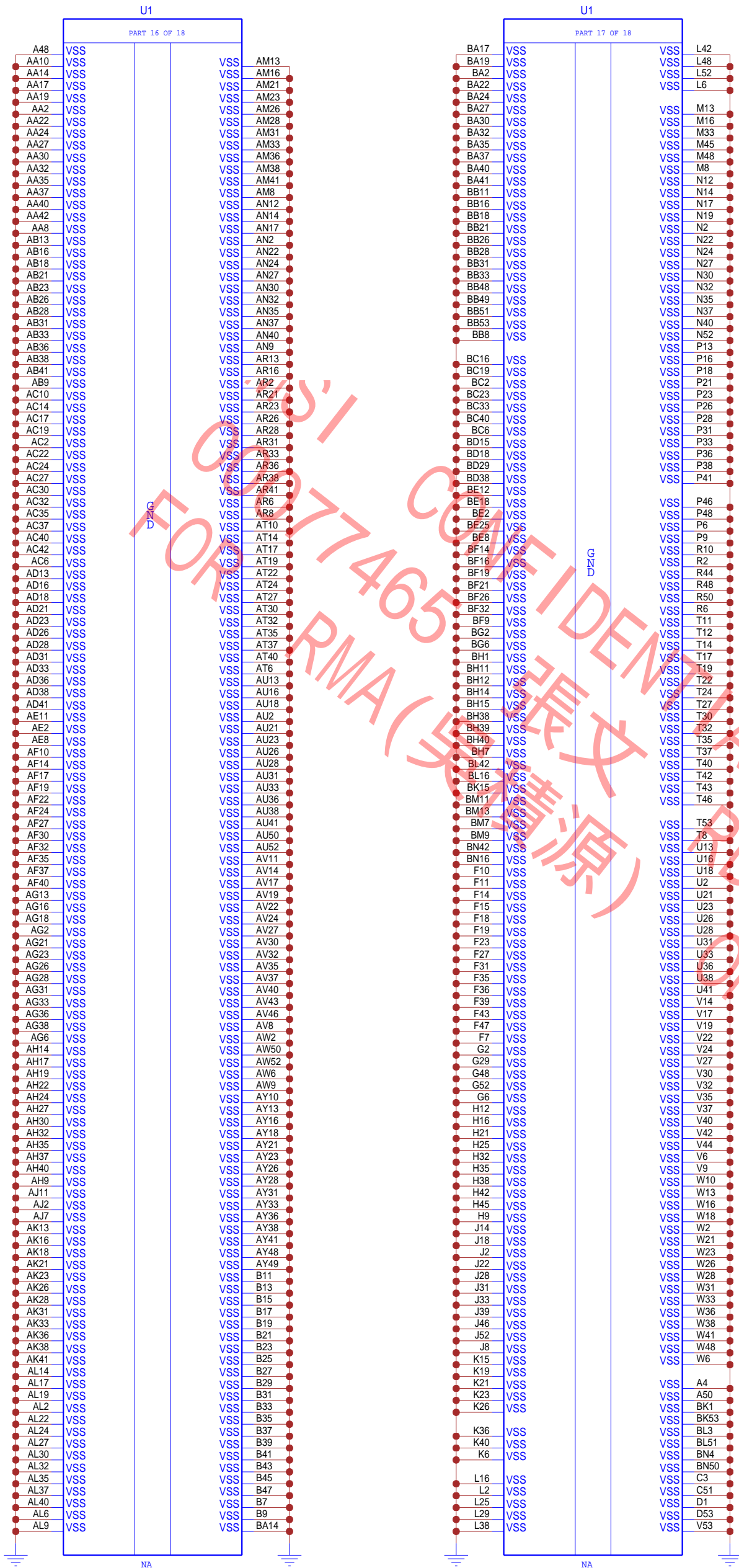
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(12) PITCAIRN POWER



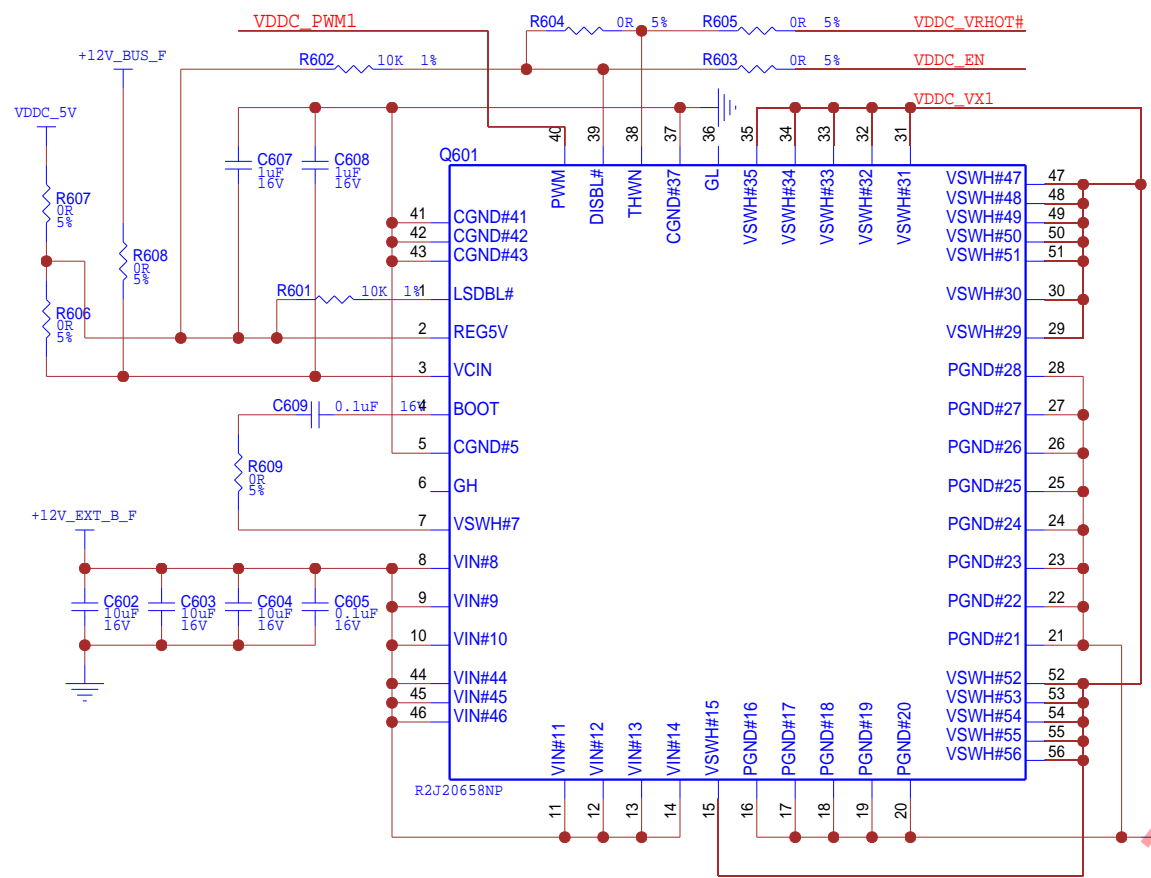
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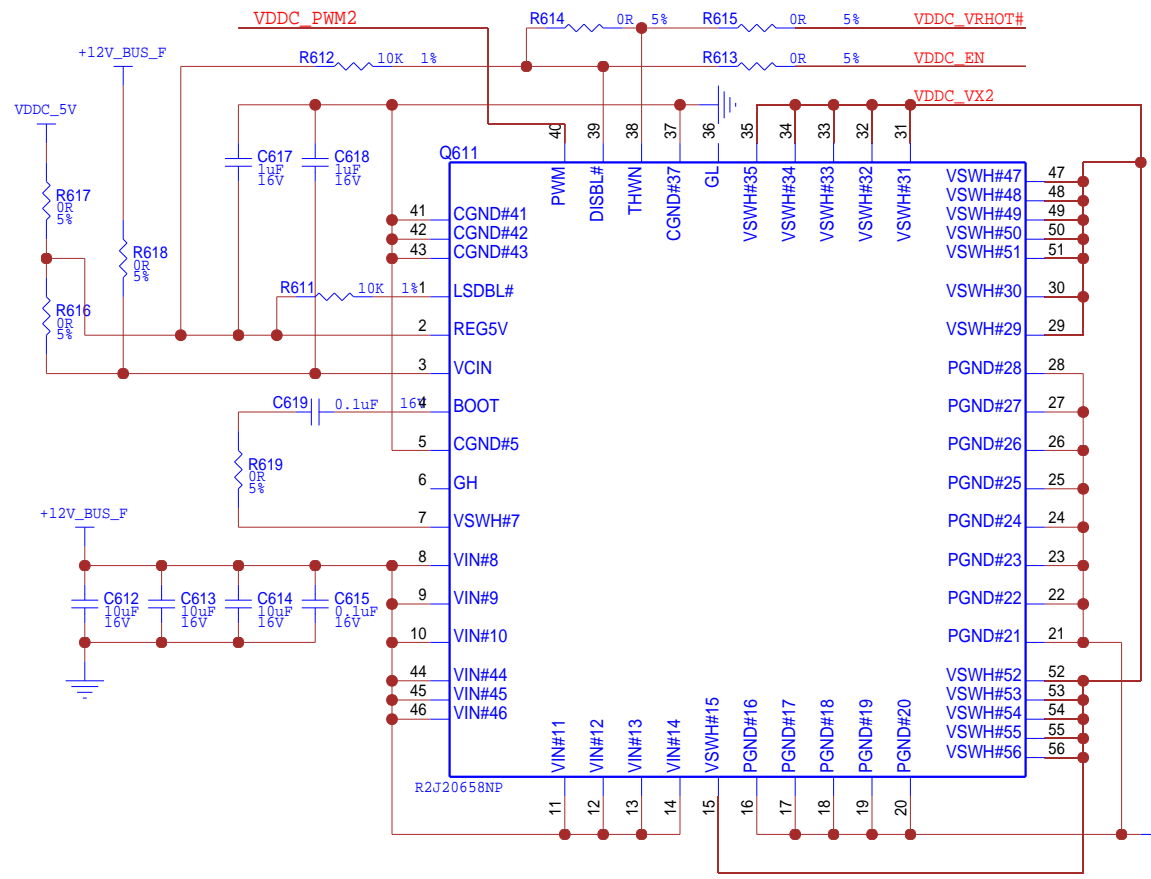
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| SHEET: PITCAIRN GND | | TITLE: Pitcairn GDDR5 x32 | |
| DATE: Thu Dec 01 18:38:28 2011 | | REV: 1.0 | |
| SHEET NUMBER: 13 OF 22 | | DOCUMENT NUMBER: 105-C401xx-00 | |

(14) VDDC

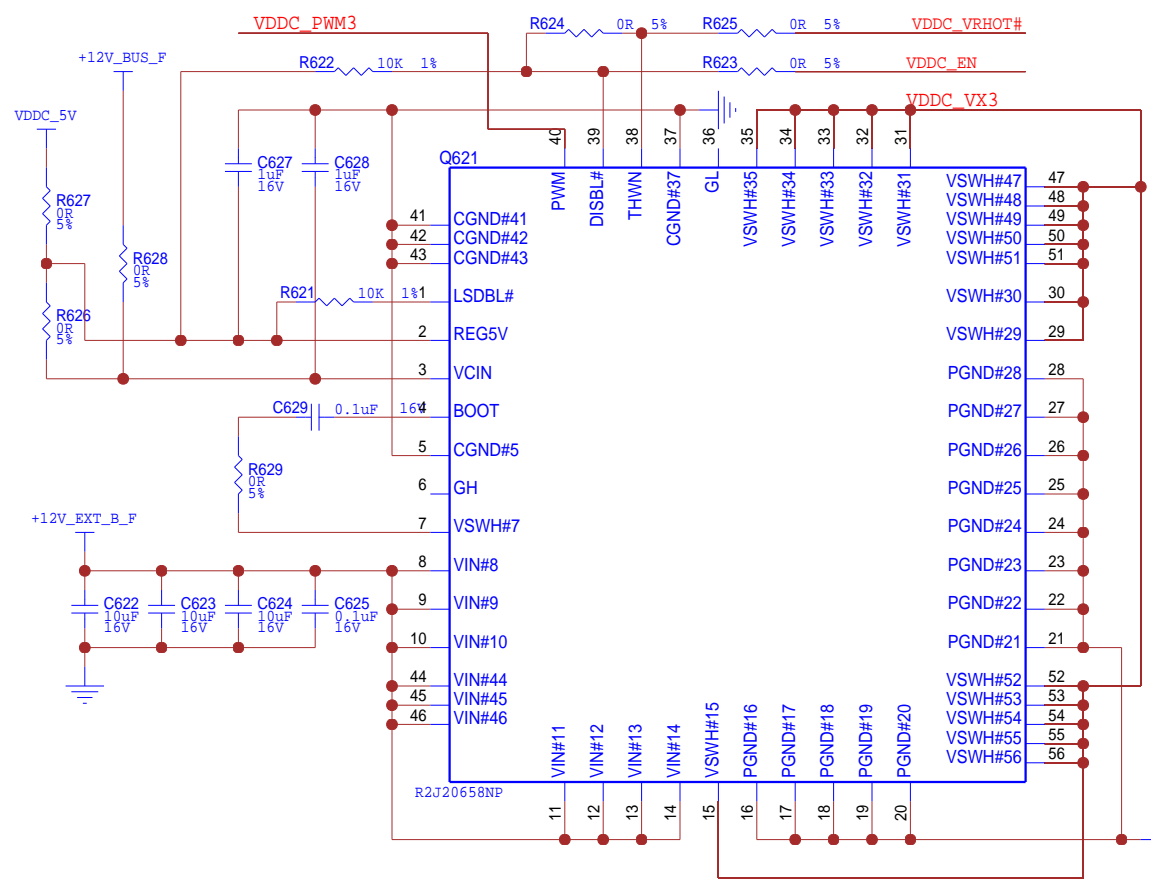
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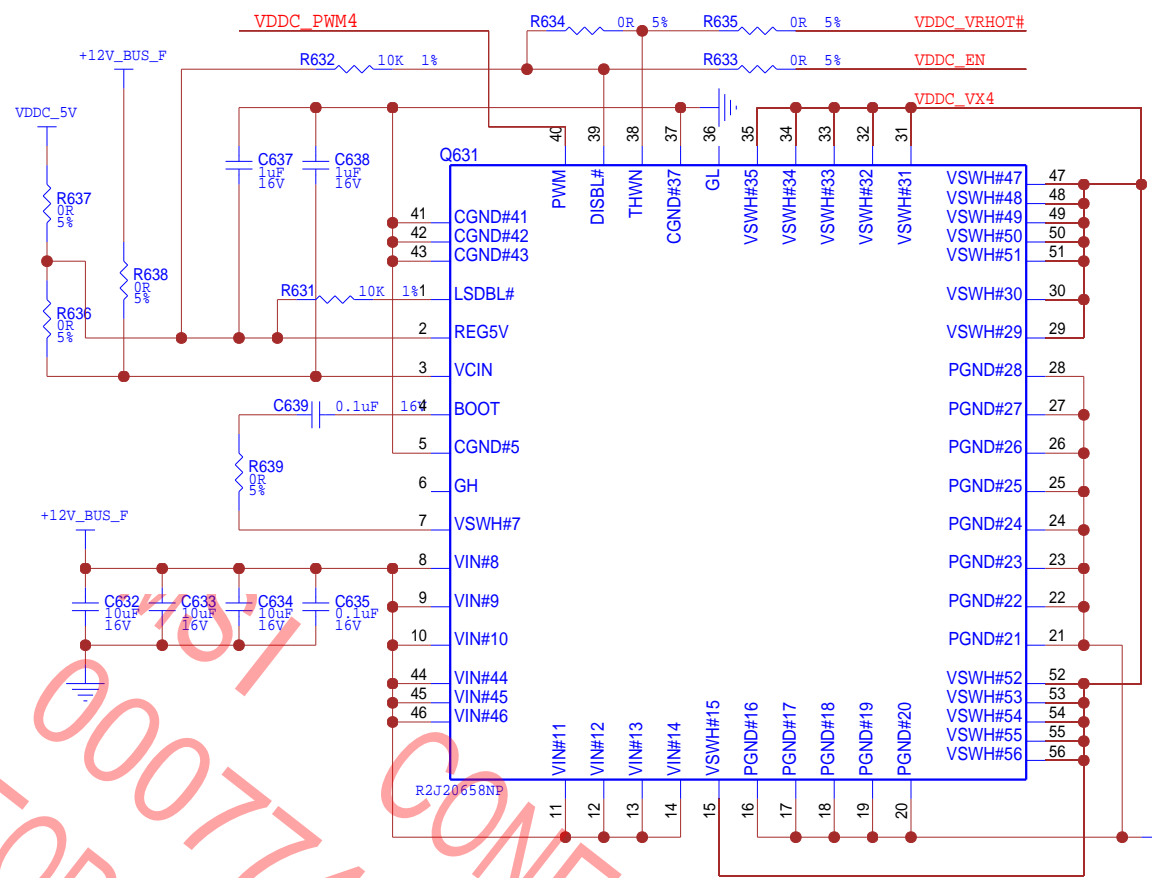


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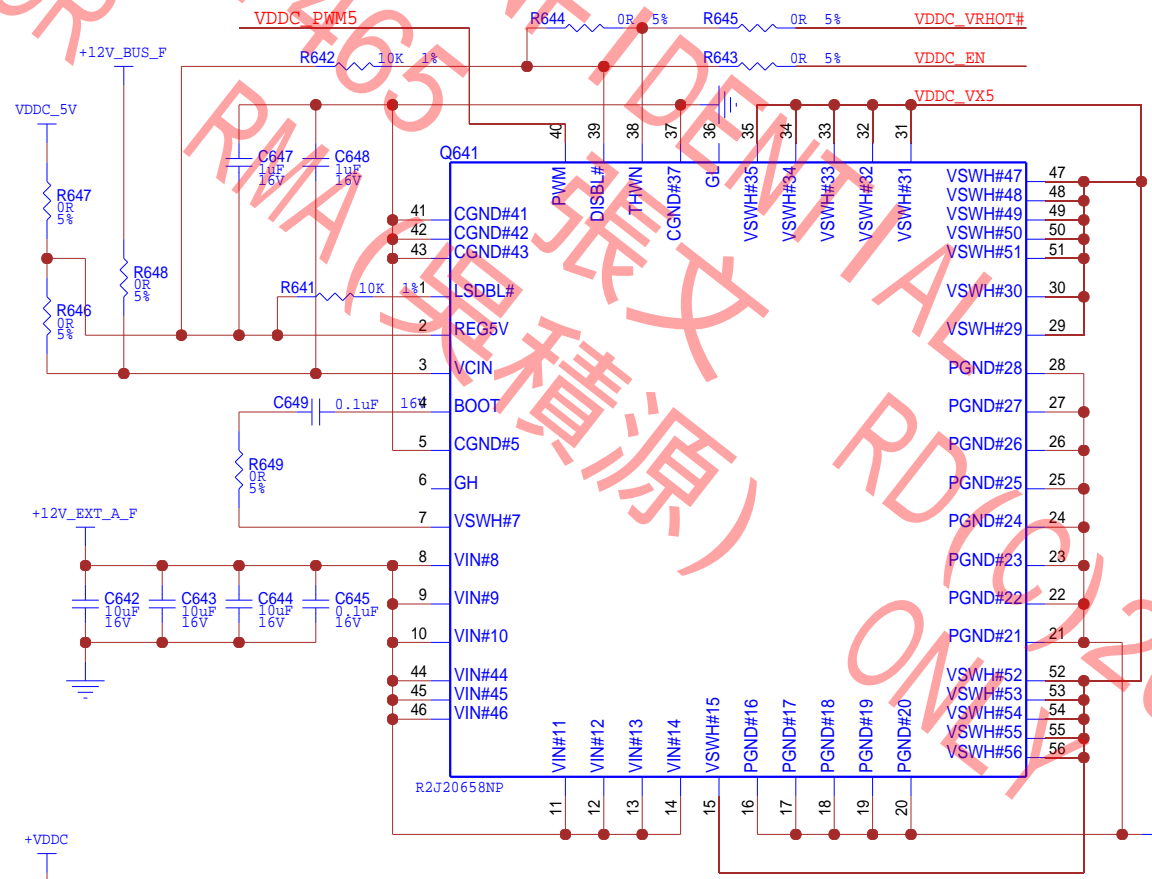


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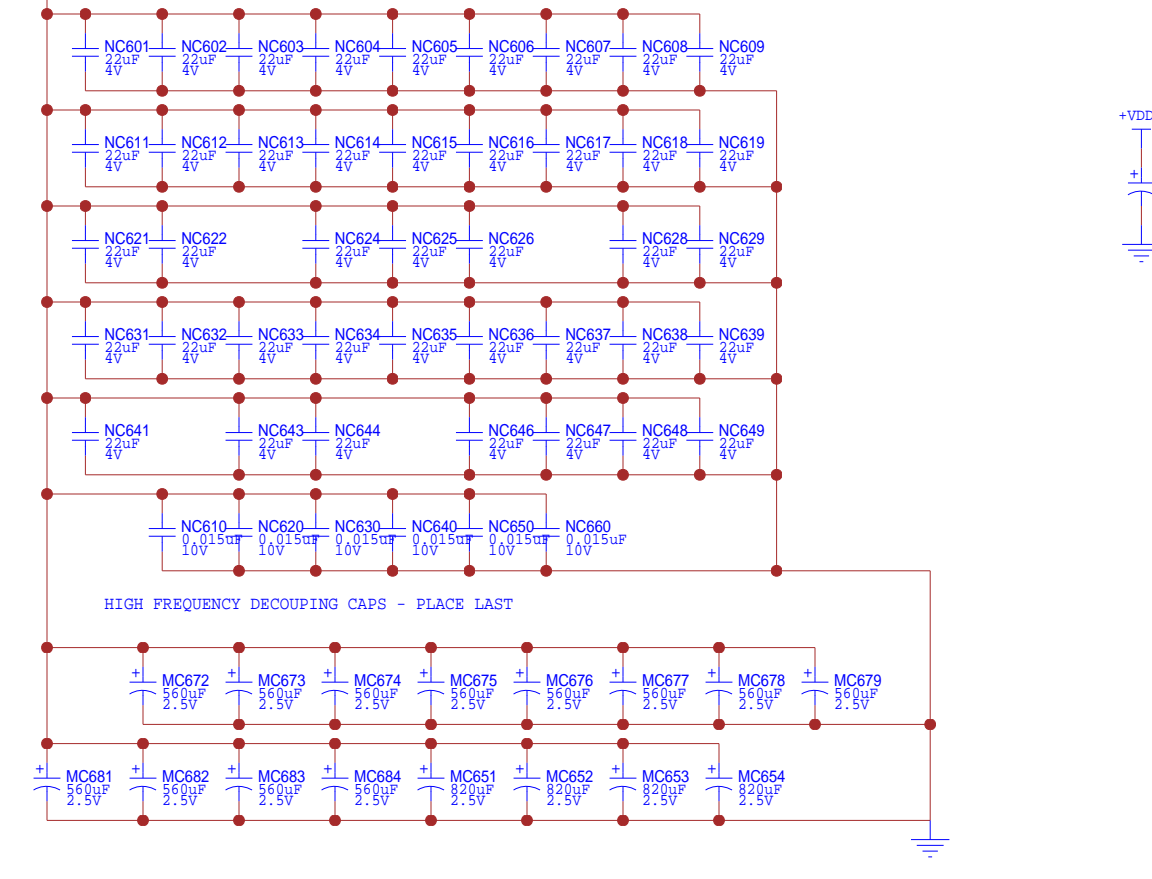
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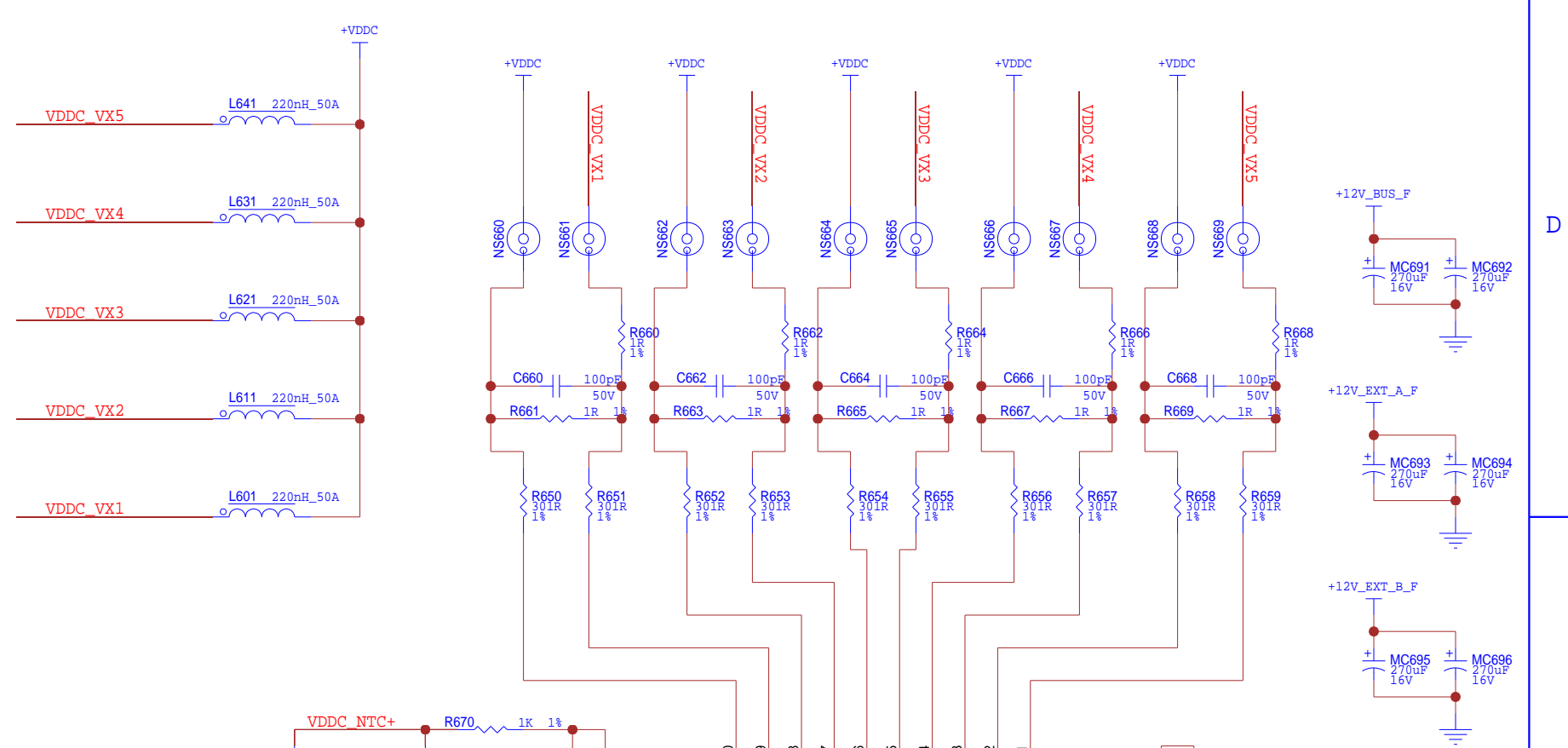


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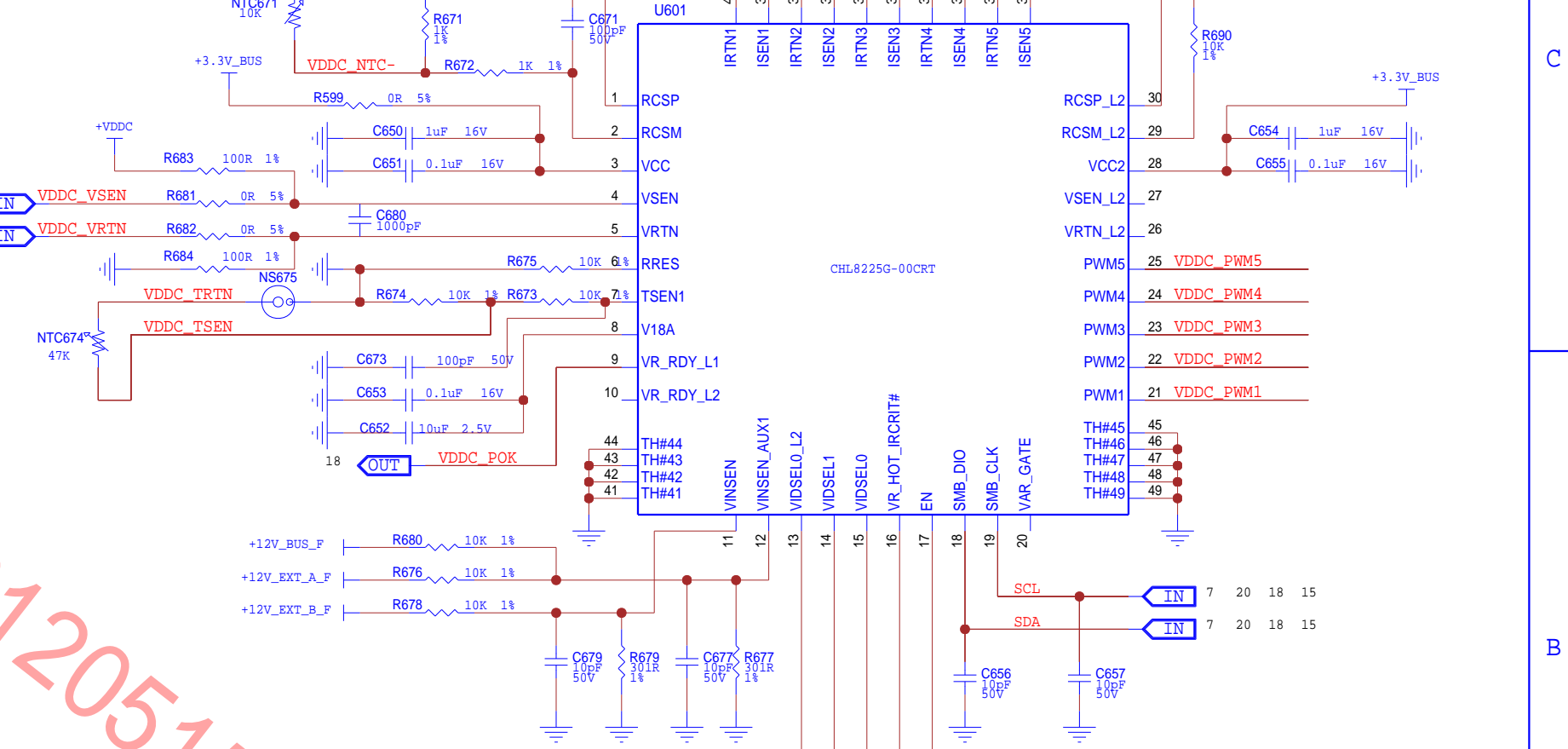


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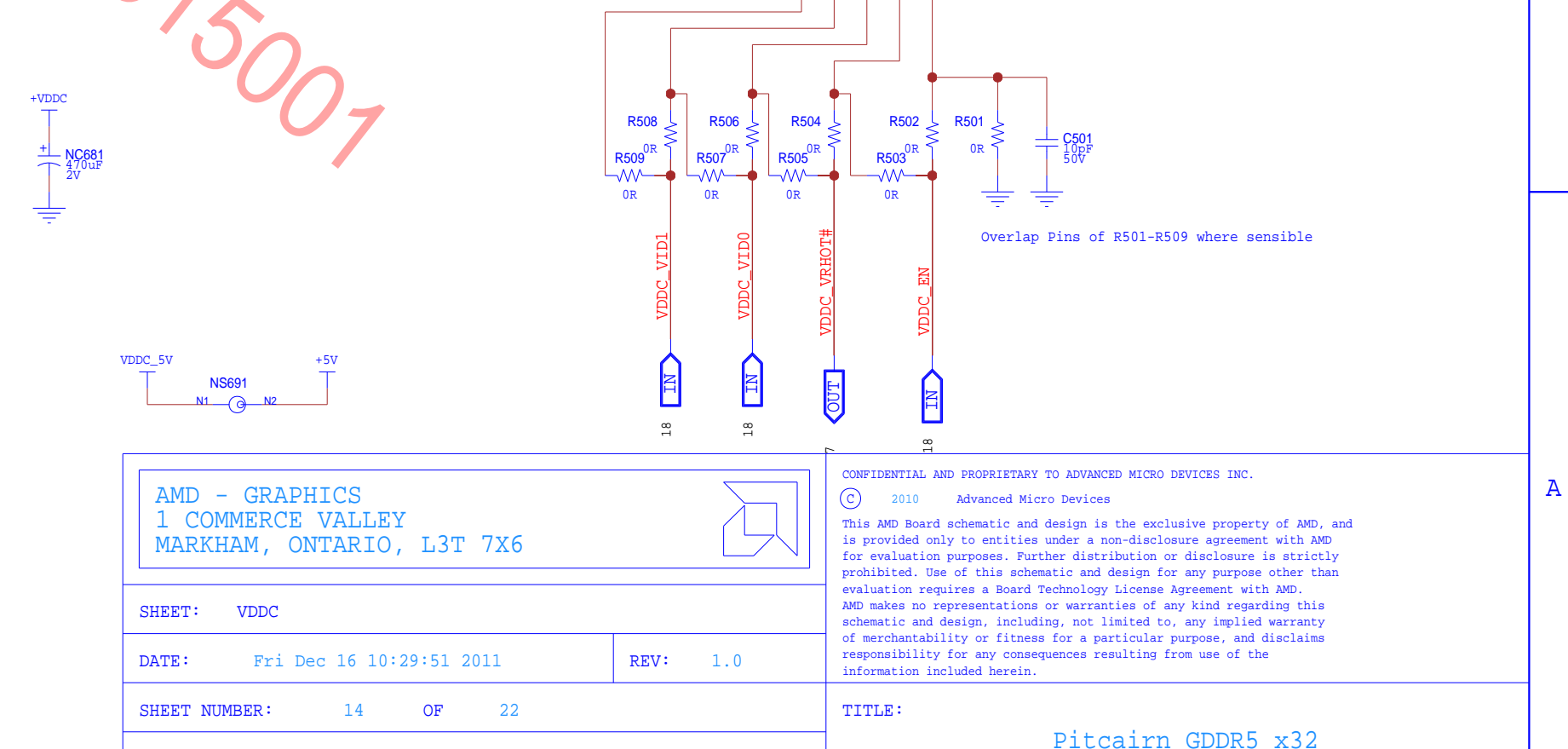
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SHEET: VDDC

DATE: Fri Dec 16 10:29:51 2011

SHEET NUMBER: 14 OF 22

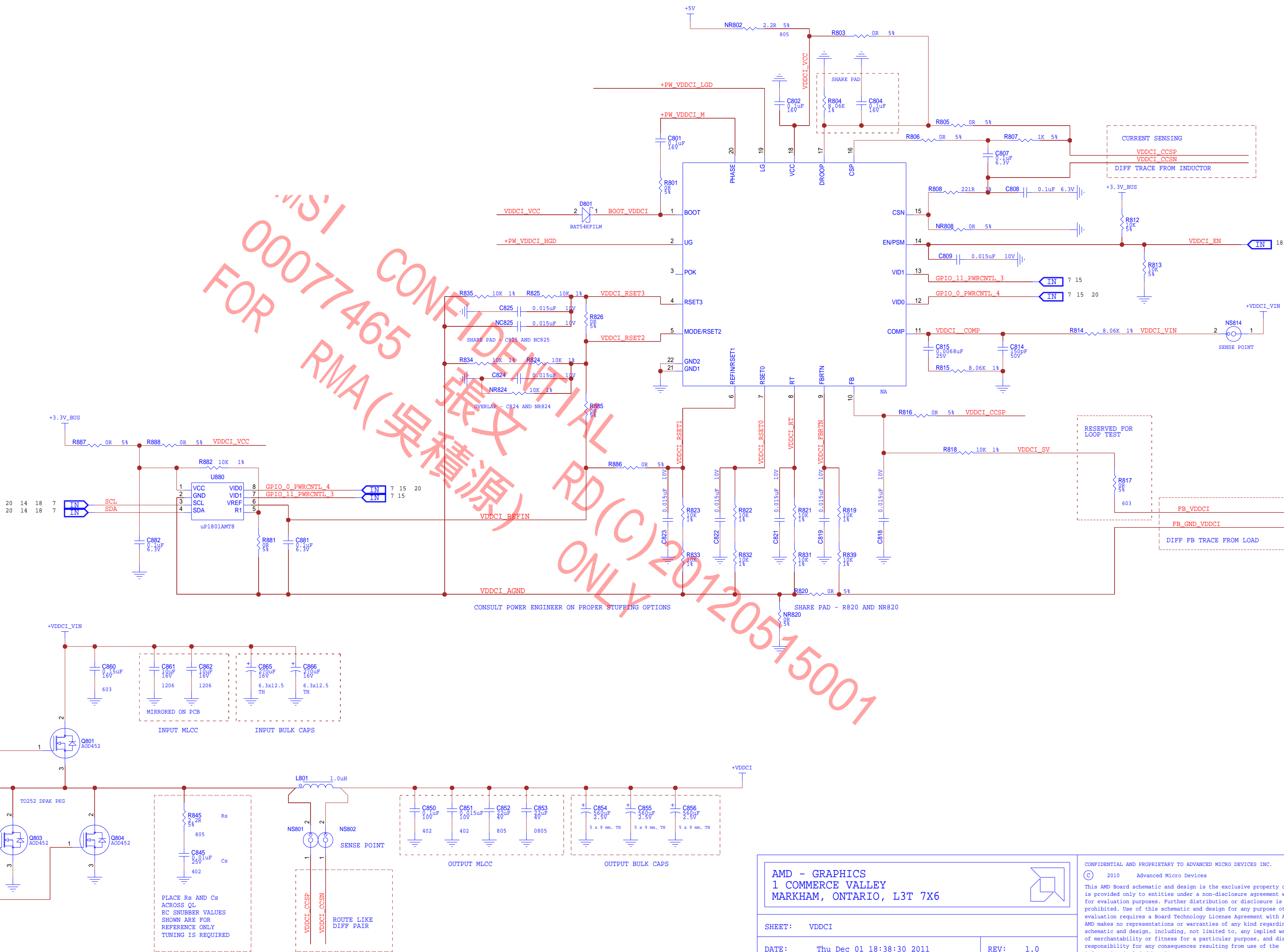
DOCUMENT NUMBER: 105-C401xx-00

REV: 1.0

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(15) VDDCI



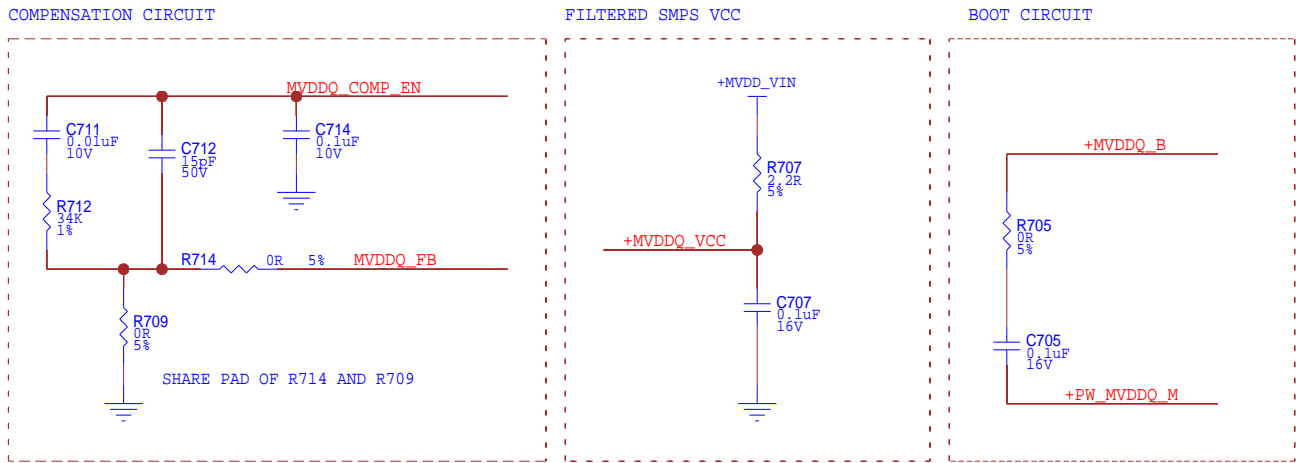
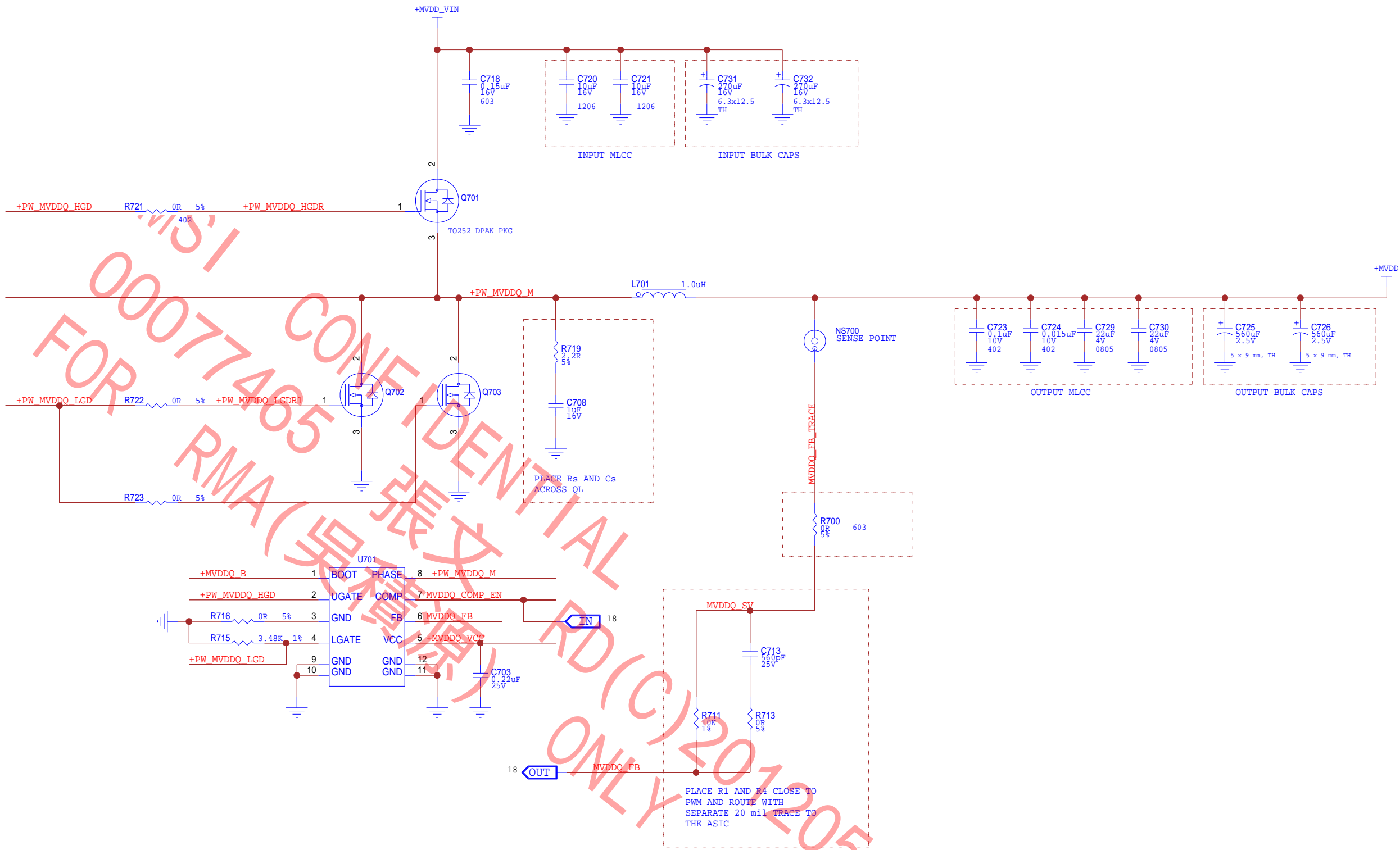
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| DOCUMENT NUMBER: 105-C401xx-00 | | | |

LAYOUT GUIDELINE

1. POSITION THE CONTROLLER (U703) SUCH THAT LGATE (PIN4) IS THE CLOSEST TO THE GATE OF THE MOSFETS. YOU CAN PLACE THE GATE RESISTORS R721 AND R722 NEXT TO THE GATE OF THE MOSFETS. MAKE THE GATE DRIVE TRACES (PW_MVDDQ_LGD/HGD) AS SHORT AS POSSIBLE TO REDUCE THE TRACE INDUCTANCE.

2. PLACE THE BYPASS CAPACITORS FOR VCC (C703) AS WELL AS BOOST CAPS (C705) AS CLOSE TO THE CONTROLLER AS POSSIBLE.

3. VOLTAGE AMPLIFIER COMPENSATION NETWORK: PLACE R714 CLOSE TO THE PIN 7. PLACE THE REST OF THE COMPENSATION NETWORK (R710, R711, R712, R713, C711, C712 AND C713) CLOSE TO THE PINS 7 AND 6.



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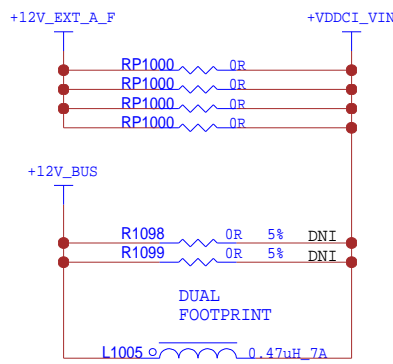
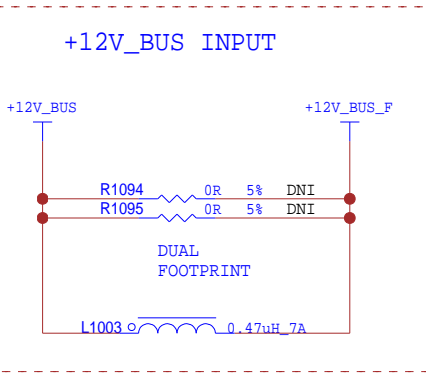
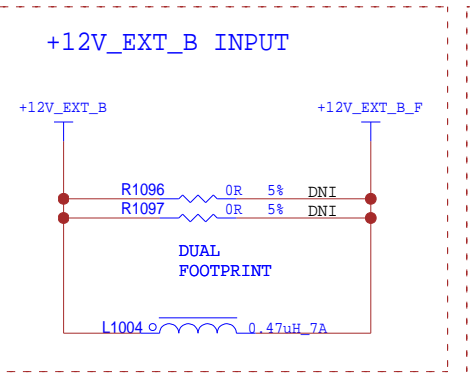
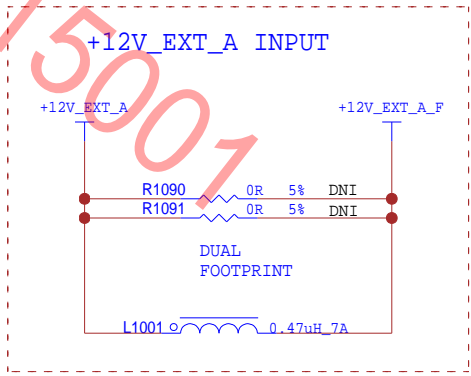
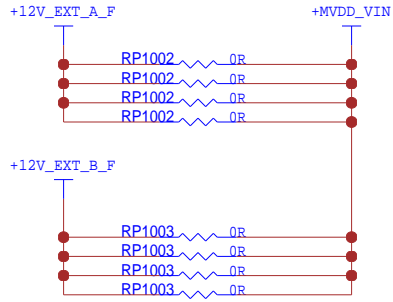
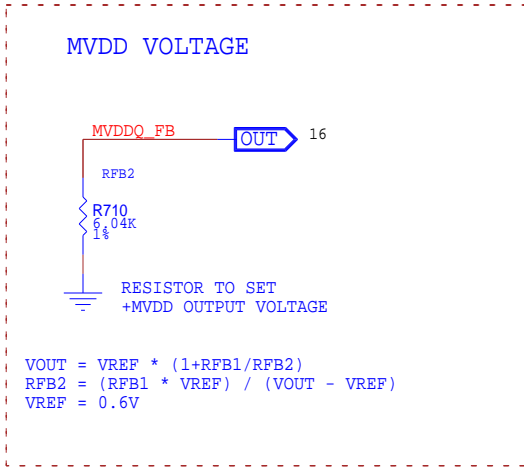
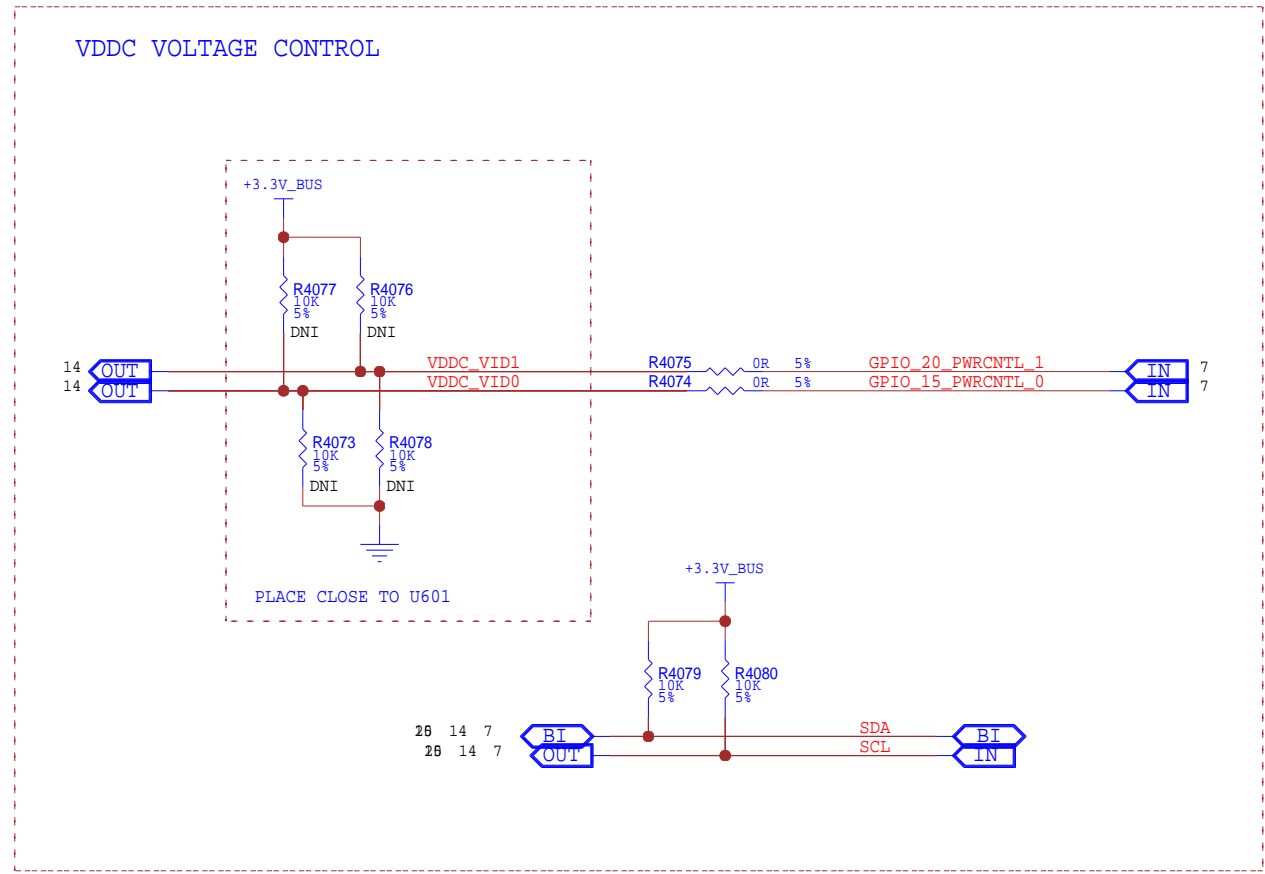
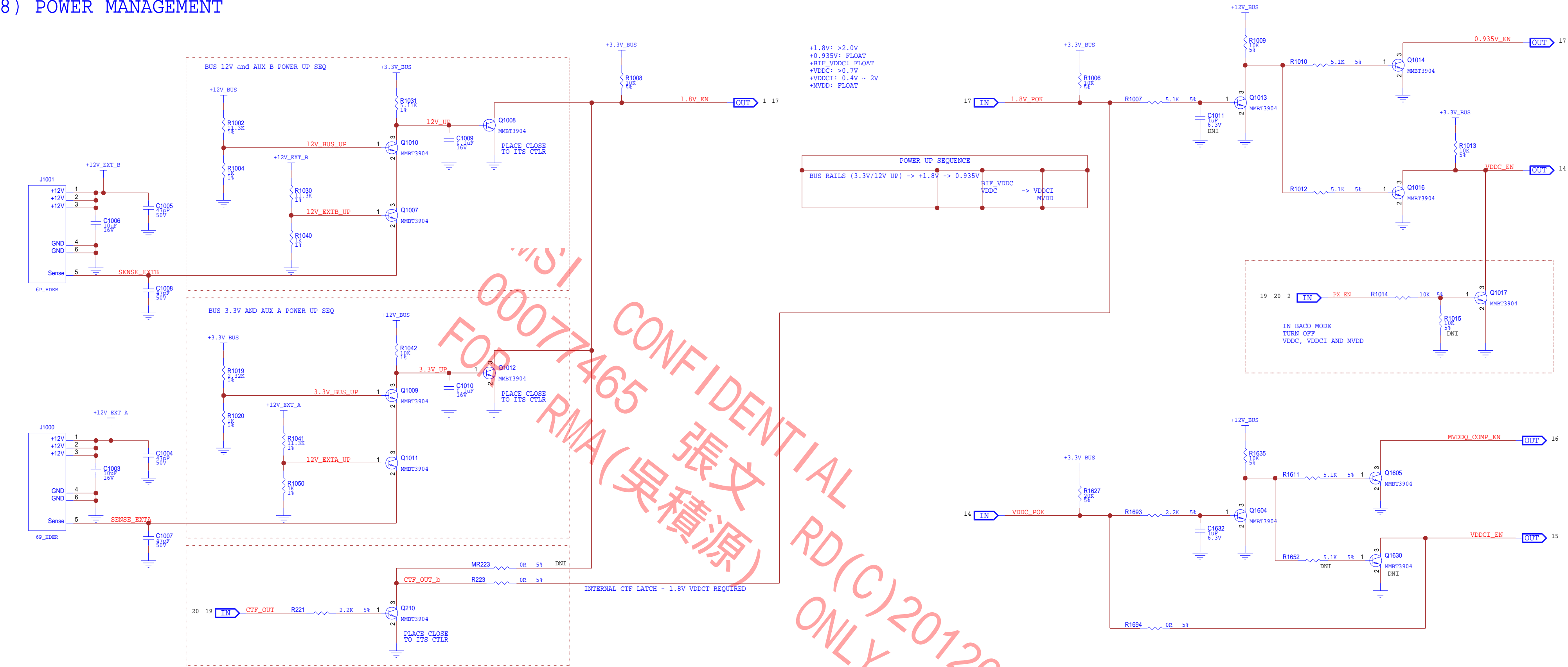
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(18) POWER MANAGEMENT



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| SHEET: POWER MANAGEMENT | |
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DATE: Fri Dec 16 12:16:19 2011

SHEET NUMBER: 19 OF 22

DOCUMENT NUMBER: 105-C401xx-00

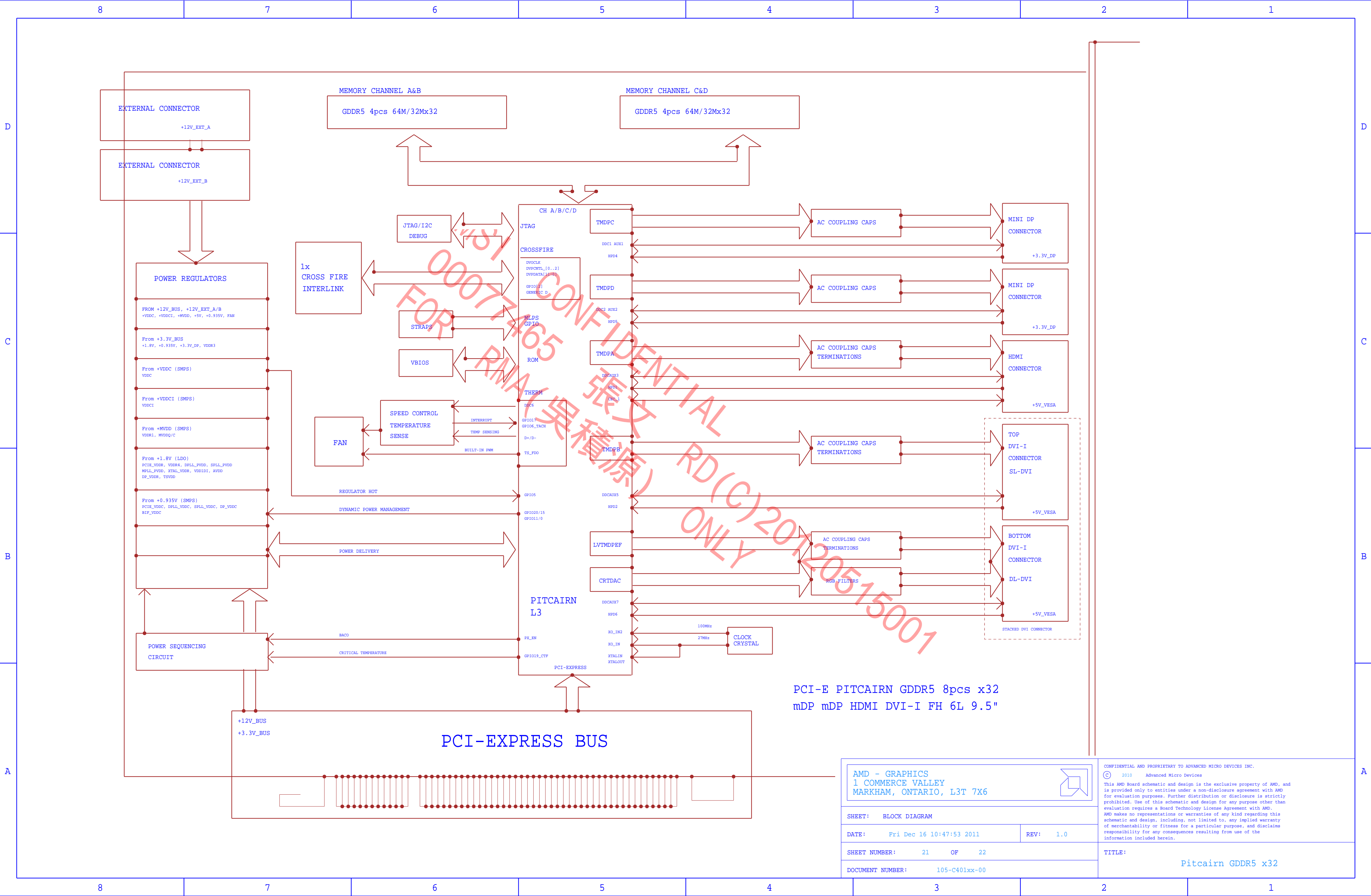
TITLE: Pitcairn GDDR5 x32

Pitcairn GDDR5 x32

(20) DEBUG CIRCUIT



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| DATE: Thu Dec 01 18:38:32 2011 | | REV: 1.0 | |
| SHEET NUMBER: 20 OF 22 | | | |
| DOCUMENT NUMBER: 105-C401xx-00 | | | |



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| SHEET: BLOCK DIAGRAM | | | TITLE: Pitcairn GDDR5 x32 | |
| DATE: Fri Dec 16 10:47:53 2011 | | | REV: 1.0 | |
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