

P682: GT216, GB1-128, DDR2 1024MB 64Mx16, DL-DVI,VGA, HDMI

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Page 21: POWER SUPPLY: NVVDD DUAL PHASE SWITCHER

0A

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Page 2 Remove JTAG resistor; Disconnecter SMCLK to I2CS_SCL, SMDAT to I2CS_SDA

Page 3 Add FBA_CMD18 for A13

Page 4 Add FBA_CMD18 for A13

Page 6 Add FBC_CMD18 for A13

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Page 11 Add R1101~R1107 for EMI

Page 12 Add R1201~R1204 for EMI, Change J2 footprint

Page 13 Remove J1 slim VGA

Page 16 Change Crystal Footprint to 2-PIN SMD; Remove Info ROM function

Page 17 Remove JTAG (J3) Connector

Page 19 Cahnge PEXVDD solution to UP7706

Page 20 Change FBVDDQ PWM solution to UP6101

Page 21 Change NVVDD PWM solution to UP6161

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Page 17 Modify PIN4 for co-lay connector (4PIN and 2PIN)

Page 18 Remove HDCP

Page 19 change IFPPLLVD to 3V3

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Page 19 add PEX_PLLVDD

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Page 16 Add R1601,R1602

Page 19 Remove 1V8

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Page 5 Add FBA_CMD18's Terminations

Page 6 Add FBC_CMD18's Terminations

Page 21 Remove C926,C931

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Only change PCB ver:

REV	VARIANT	NPVN	ASSEMBLY
B	BASE	600-10682-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	600-10682-0000-100	GT216-200, 600/1500MHz
2	SKU001	600-10682-0001-100	GT216-200, 600/1500MHz 512MB 32Mx16 BGA84 500MHz DCR2 DVI-I(DP)HDMI
3	SKU002	600-10682-0002-100	GT216-300, 600/1500MHz 512MB 32Mx16 BGA84 500MHz DCR2 DVI-I(DP)HDMI
4	SKU003	600-10682-0003-100	GT216-100, 600/1500MHz 256MB 32Mx16 BGA84 500MHz DCR2 DVI-I(DP)HDMI
5	SKU011	600-10682-0011-100	GT216-300, 600/1500MHz 512MB 32Mx16 BGA84 500MHz DCR2 DVI-I(DV)I(H)HDMI
6	SKU012	600-10682-0012-100	GT216-200, 600/1500MHz 512MB 32Mx16 BGA84 500MHz DCR2 DVI-I(DV)I(H)HDMI
7	SKU013	600-10682-0013-100	GT216-100, 600/1500MHz 512MB 32Mx16 BGA84 500MHz DCR2 DVI-I(DV)I(H)HDMI
8	SKU004	600-10682-0004-100	GT216-200, 600/1500MHz 1024MB 64Mx16 BGA84 500MHz DCR2 DVI-I(DP)HDMI
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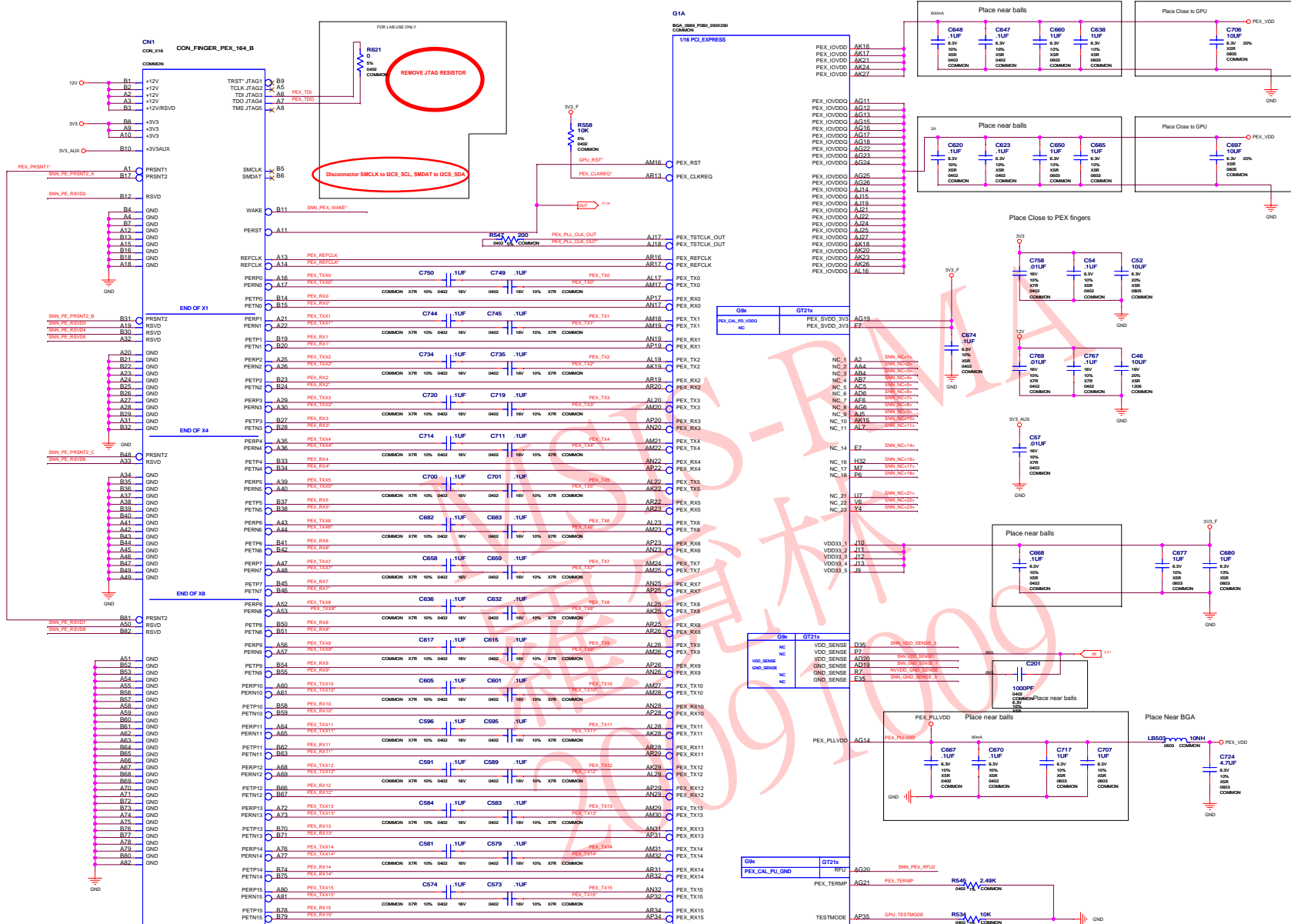
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SANTA CLARA, CA 95050, USA



NV_PN 600-10682-base-100 A

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NAME		DATE	15 MAY 2009

16X PEX INTERFACE



	NET	DIFFER	N/APPEANCE	N/CITICAL
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PEX REF01	PEX REF01	REF01	00001	0
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Pin	Signal	Level	Value
21	NVDD_SENSE	1.2V	
22	NVDD_GND_SENSE	0V	
23	PEX_PL1VDD	1.2V	
3V3	3V3	3.3V	3A
12V	12V	12V	5.5A
3V3_PEX_SVDD	3V3_PEX_SVDD	3.3V	0.05A

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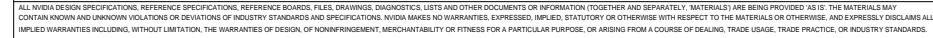
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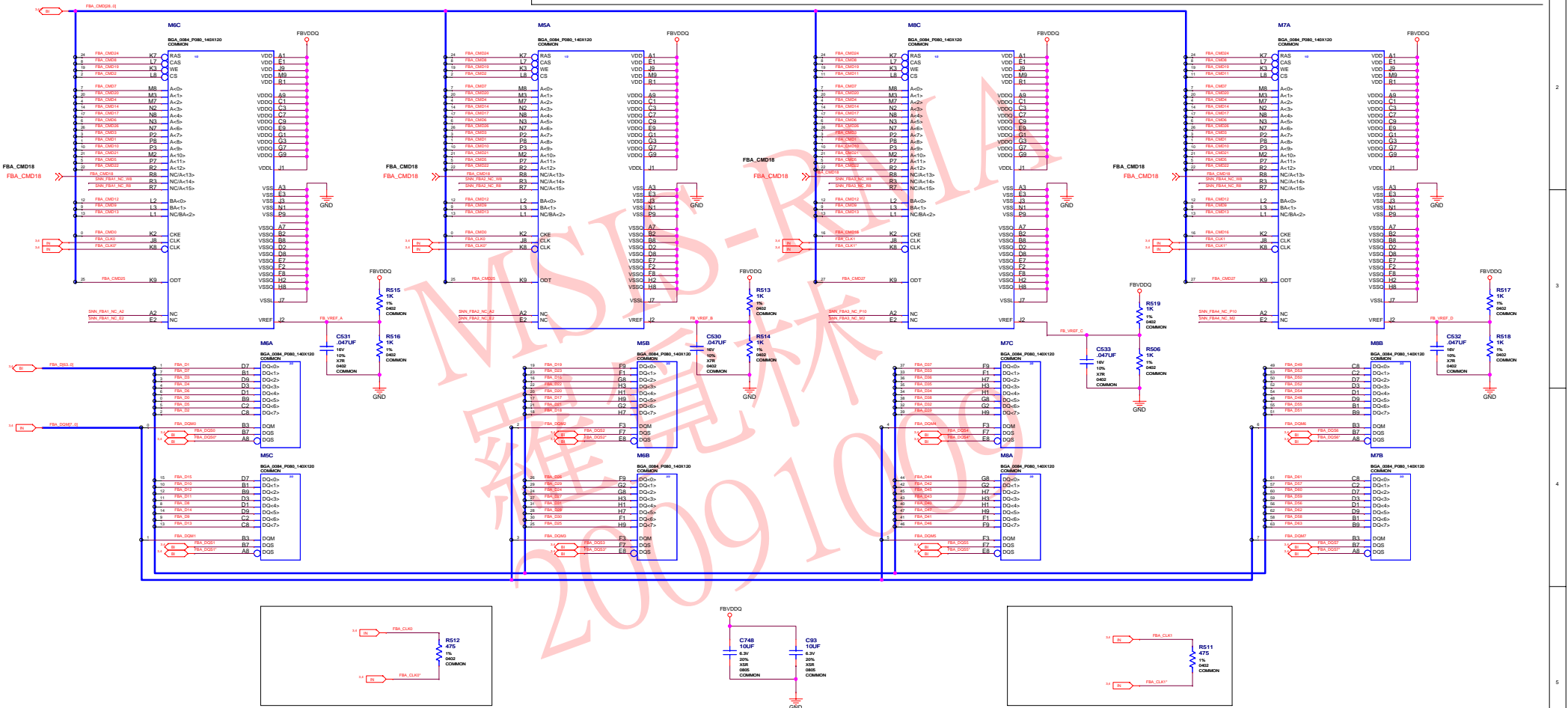
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Partition A Memories

GT21x CMD MAP



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ASSEMBLY: BASE LEVEL: GENERIC SCHEMATIC ONLY. COMMON & NC: BY OFF-ASSEMBLY NOTES AND BOM NOT FINAL.
PAGE: DETAIL: FBA 10252023 (2023) MEMORIES, FBA COMMAND BUS PINS, FBA CLK TERMS

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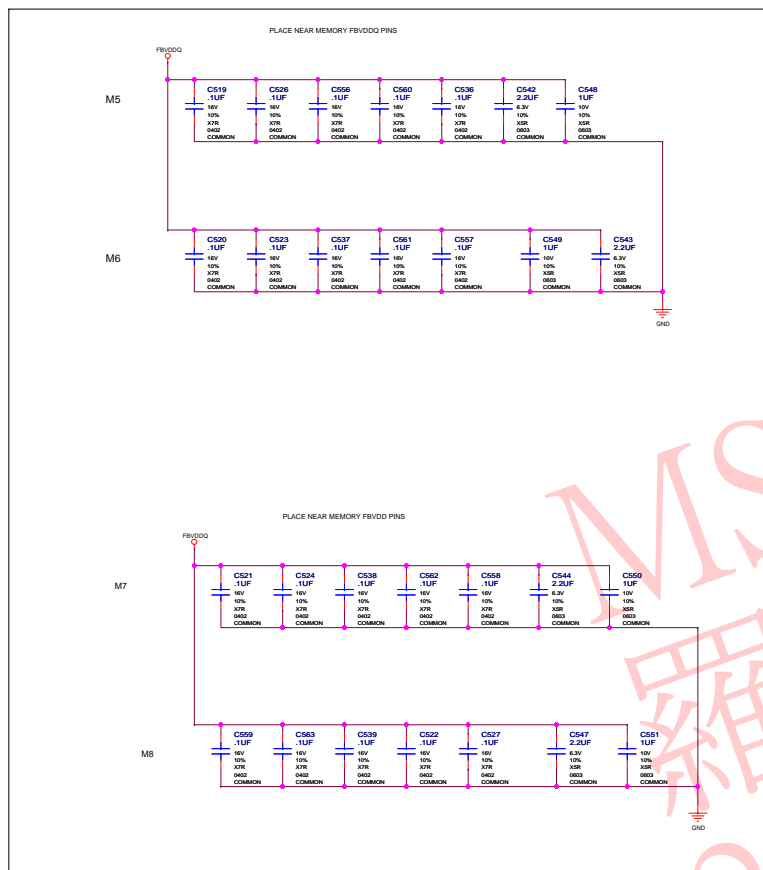


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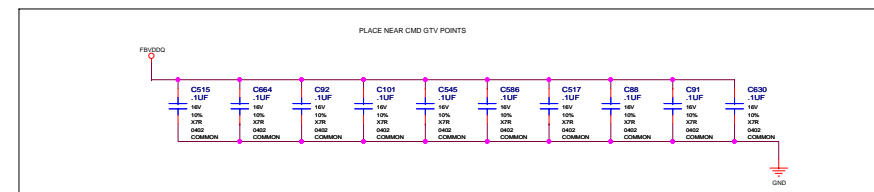
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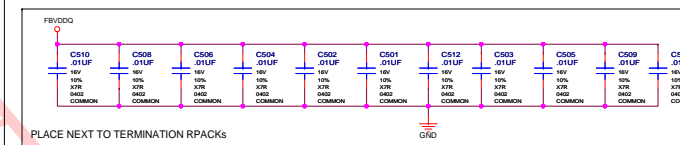
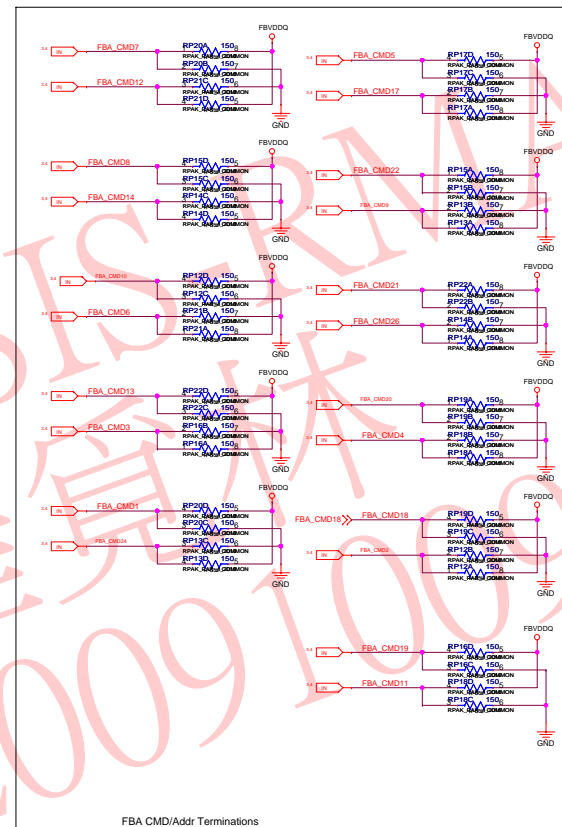
Decoupling for FBA



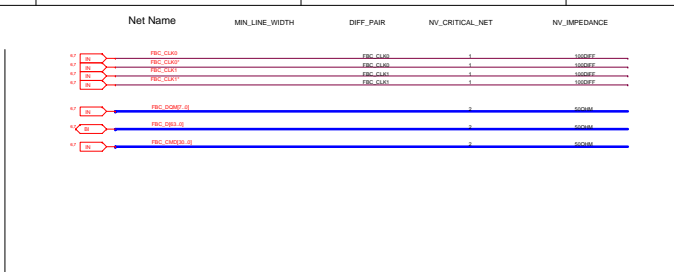
Return path coupling GND/FBVDDQ



FB A Addr/CMD termination



GT21x CMD MAP



	Net Name	MIN_LINE_WIDTH	DIFF_PAIR	NV_CRITICAL_NET	NV_IMPEDANCE
1	FRC_D050		FRC_D050	1	100DPT
2	FRC_D050		FRC_D050	1	100DPT
3	FRC_D051		FRC_D051	1	100DPT
4	FRC_D051		FRC_D051	1	100DPT
5	FRC_D052		FRC_D052	1	100DPT
6	FRC_D052		FRC_D052	1	100DPT
7	FRC_D053		FRC_D053	1	100DPT
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9	FRC_D054		FRC_D054	1	100DPT
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11	FRC_D055		FRC_D055	1	100DPT
12	FRC_D055		FRC_D055	1	100DPT
13	FRC_D056		FRC_D056	1	100DPT
14	FRC_D056		FRC_D056	1	100DPT
15	FRC_D057		FRC_D057	1	100DPT
16	FRC_D057		FRC_D057	1	100DPT
17	FRC_D058		FRC_D058	1	100DPT
18	FRC_D058		FRC_D058	1	100DPT
19	FRC_D059		FRC_D059	1	100DPT
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21	FRC_D060		FRC_D060	1	100DPT
22	FRC_D060		FRC_D060	1	100DPT
23	FRC_D061		FRC_D061	1	100DPT
24	FRC_D061		FRC_D061	1	100DPT
25	FRC_D062		FRC_D062	1	100DPT
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32	FRC_D065		FRC_D065	1	100DPT
33	FRC_D066		FRC_D066	1	100DPT
34	FRC_D066		FRC_D066	1	100DPT
35	FRC_D067		FRC_D067	1	100DPT
36	FRC_D067		FRC_D067	1	100DPT
37	FRC_D068		FRC_D068	1	100DPT
38	FRC_D068		FRC_D068	1	100DPT
39	FRC_D069		FRC_D069	1	100DPT
40	FRC_D069		FRC_D069	1	100DPT
41	FRC_D070		FRC_D070	1	100DPT
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43	FRC_D071		FRC_D071	1	100DPT
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45	FRC_D072		FRC_D072	1	100DPT
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53	FRC_D076		FRC_D076	1	100DPT
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65					
66	PL_VREF_2	UNSL			
67	PL_VREF_P	UNSL			
68	PL_VREF_N	UNSL			
69	PL_VREF_2P	UNSL			
70					

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS PUS, FBC CLK TERMS

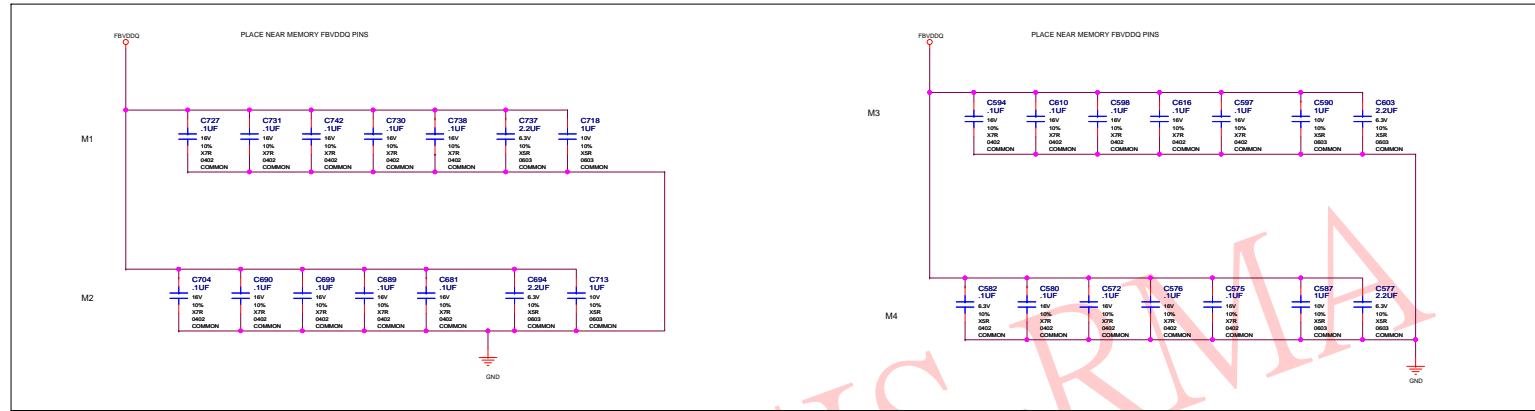
2701 SAN TOMAS EXPRESSWAY



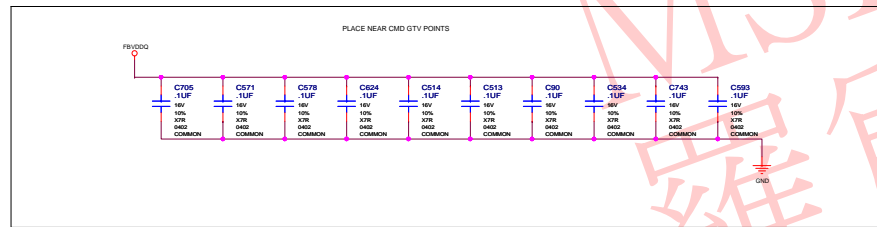
NV_PN	600-10682-base-100 A		
ID		PAGE	
NAME		DATE	15-MAY-2009

FRAMEBUFFER: PARTITION C DECOUPLING

Decoupling for FBC

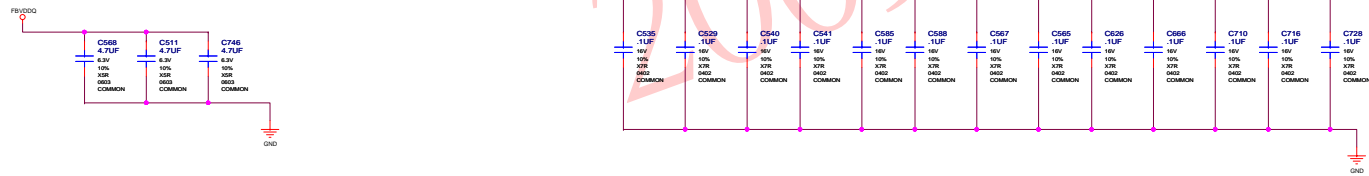


Return path coupling GND/FBVDDQ

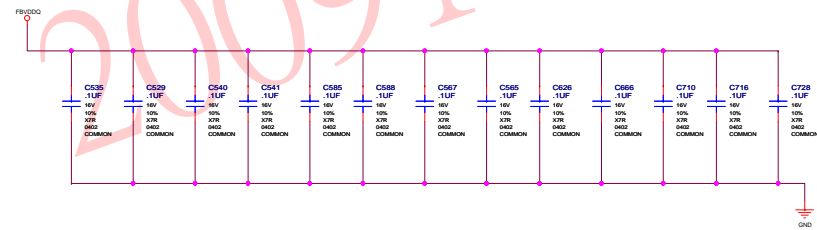


Capacitors bounding the FB area

on each side and in middle



Return path coupling GND/FBVDDQ for FBA/FBC




G1E

NW-DBD		
A411	GND	GND
A412	GND	E18
A413	GND	E24
A414	GND	E27
A415	GND	E30
A416	GND	E8
A417	GND	E9
A418	GND	E22
A419	GND	E31
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A425	GND	E11
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A565	GND	E19
A5		

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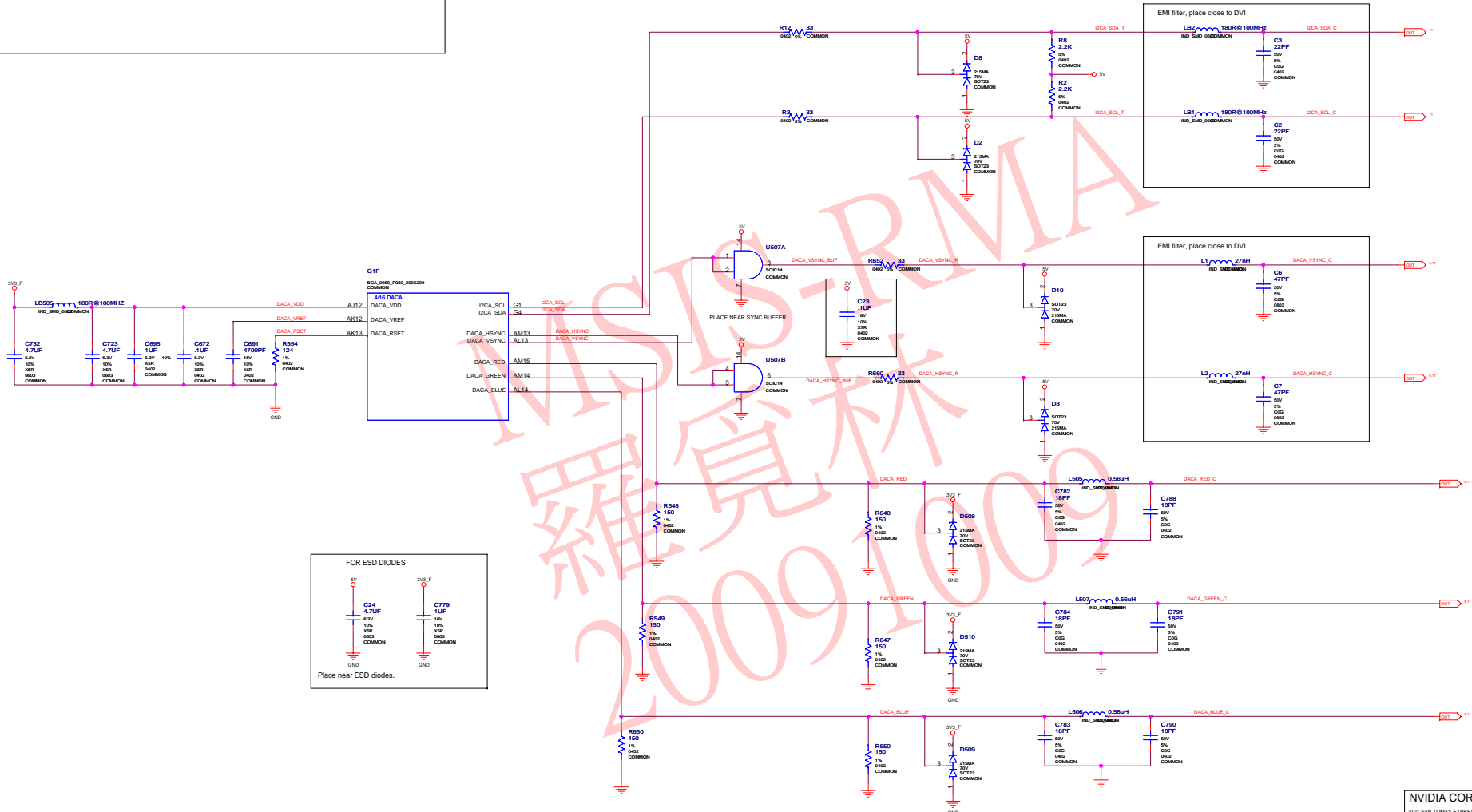
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS, GPU GND CONNECTIONS

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NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACA_VDD		3.3V 120M	
DACA_VREF		120M	
DACA_VREF_F		120M	
DACA_RED	1	500M	
DACA_GREEN	1	500M	
DACA_BLUE	1	500M	
DACA_RED_C	1	500M	
DACA_GREEN_C	1	500M	
DACA_BLUE_C	1	500M	
DACA_HSYNC	2	500M	
DACA_VSYNC	2	500M	
DACA_HSYNC_F	2	500M	
DACA_VSYNC_F	2	500M	
DACA_HSYNC_F_F	2	500M	
DACA_VSYNC_F_F	2	500M	
DACA_HSYNC_C	2	500M	
DACA_VSYNC_C	2	500M	

Primary Display (DACA), DVI-I

DACA RGB-FILTER




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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. 10000 ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA (PRIMARY DVI-I)

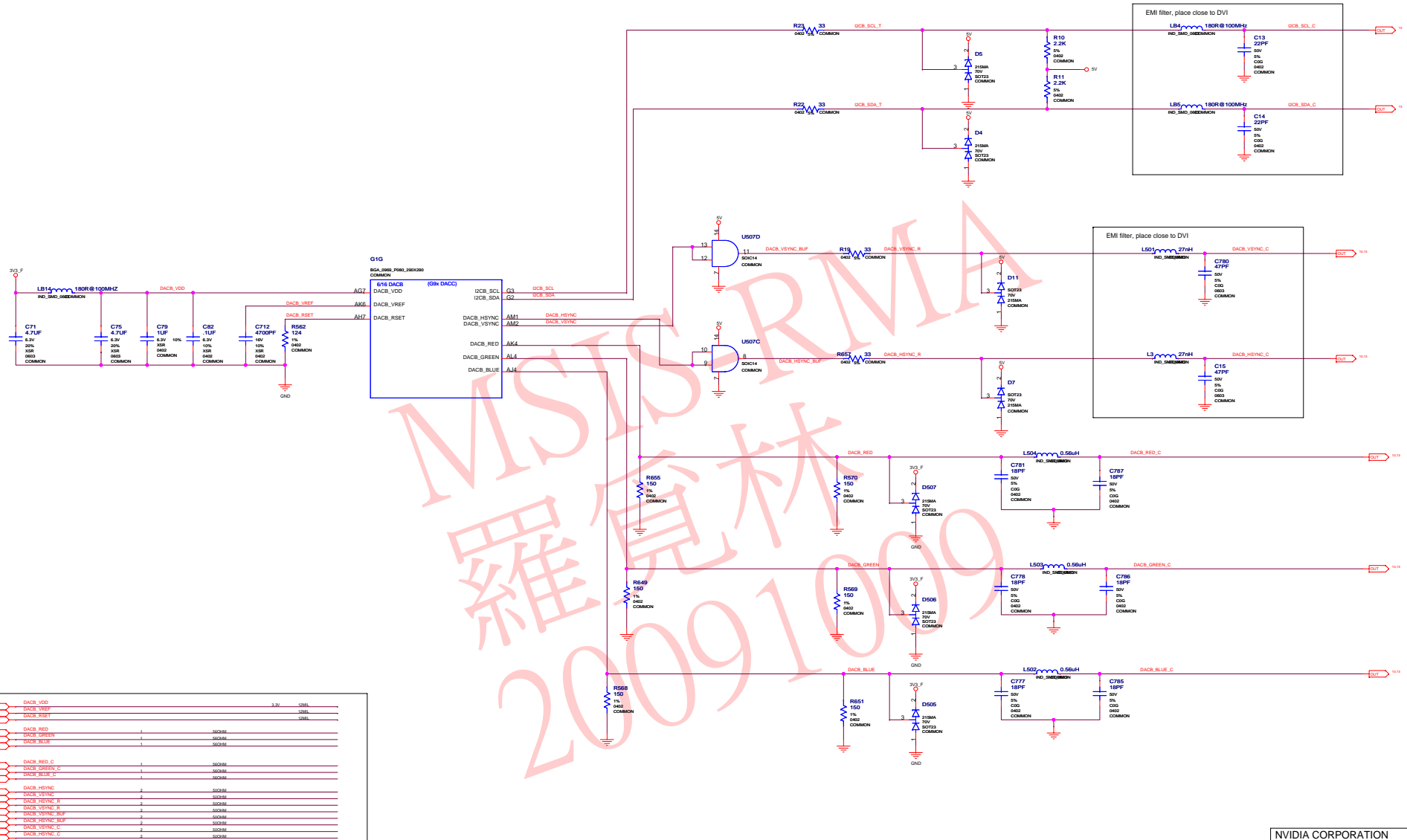
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NAME		DATE	15-MAY-2009


DACB, SECONDARY VGA



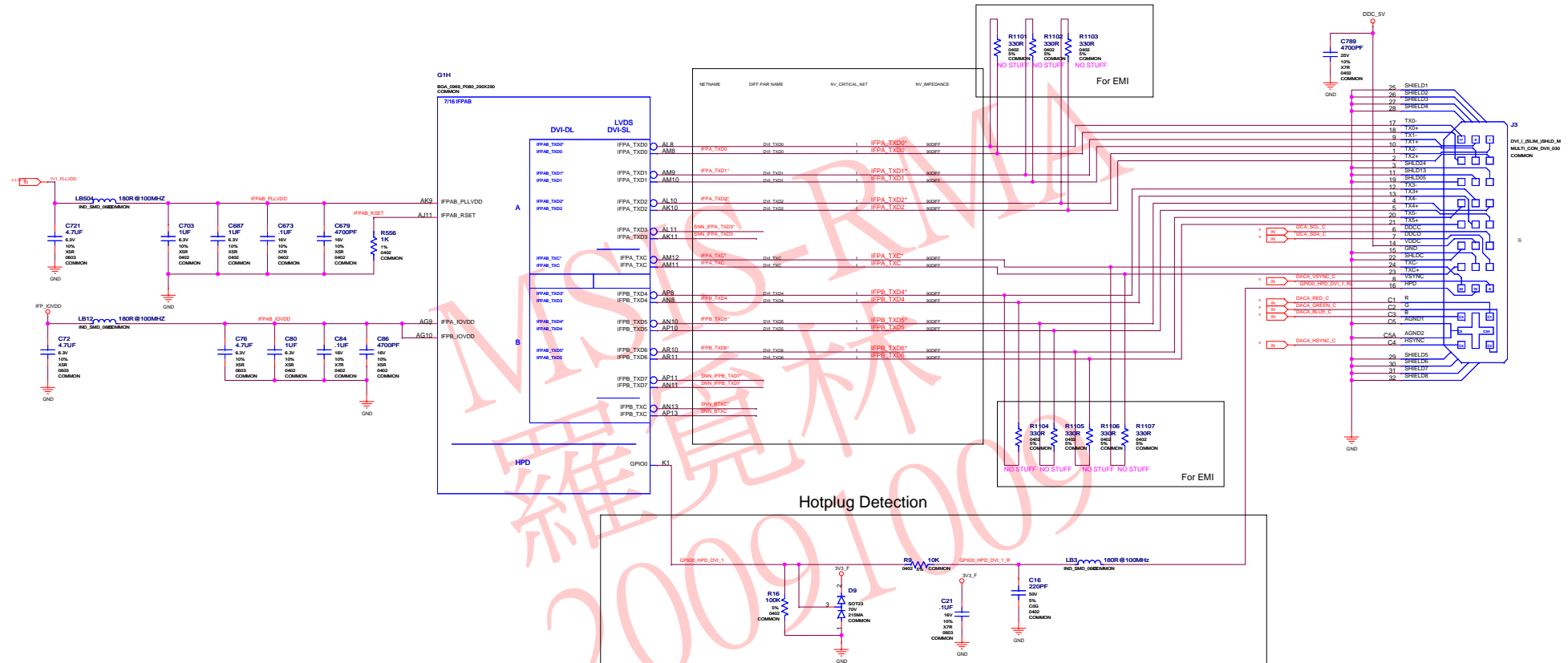
Symbol	Value	Unit
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$\alpha_{\text{DACK_VREF}}$		VDD
$\alpha_{\text{DACK_VREF}}$		VDD
$\alpha_{\text{DACK_RED}}$	1	SDIO
$\alpha_{\text{DACK_GREEN}}$	1	SDIO
$\alpha_{\text{DACK_BLUE}}$	1	SDIO
$\alpha_{\text{DACK_RED_C}}$	1	SDIO
$\alpha_{\text{DACK_GREEN_C}}$	1	SDIO
$\alpha_{\text{DACK_BLUE_C}}$	1	SDIO
$\alpha_{\text{DACK_HYSTC}}$	2	SDIO
$\alpha_{\text{DACK_HYSTC_H}}$	2	SDIO
$\alpha_{\text{DACK_HYSTC_M}}$	2	SDIO
$\alpha_{\text{DACK_HYSTC_B}}$	2	SDIO
$\alpha_{\text{DACK_HYSTC_BLP}}$	2	SDIO
$\alpha_{\text{DACK_HYSTC_BLP}}$	2	SDIO
$\alpha_{\text{DACK_HYSTC_V}}$	2	SDIO

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB, SECONDARY DVI-I

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TMD5 LINK A/B: DVI-I DUALLINK, SOUTH



	NETNAME	MIN_LENGTH	VOLTAGE
IS	PPAS_PLLVDD	120MIL	1.00V
IS	PPAS_IOVDD	120MIL	3.3V
IS	PPAS_ISET	120MIL	

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMD5 LINK A/B: DVI-I (SOUTH)

NVIDIA CORPORATION

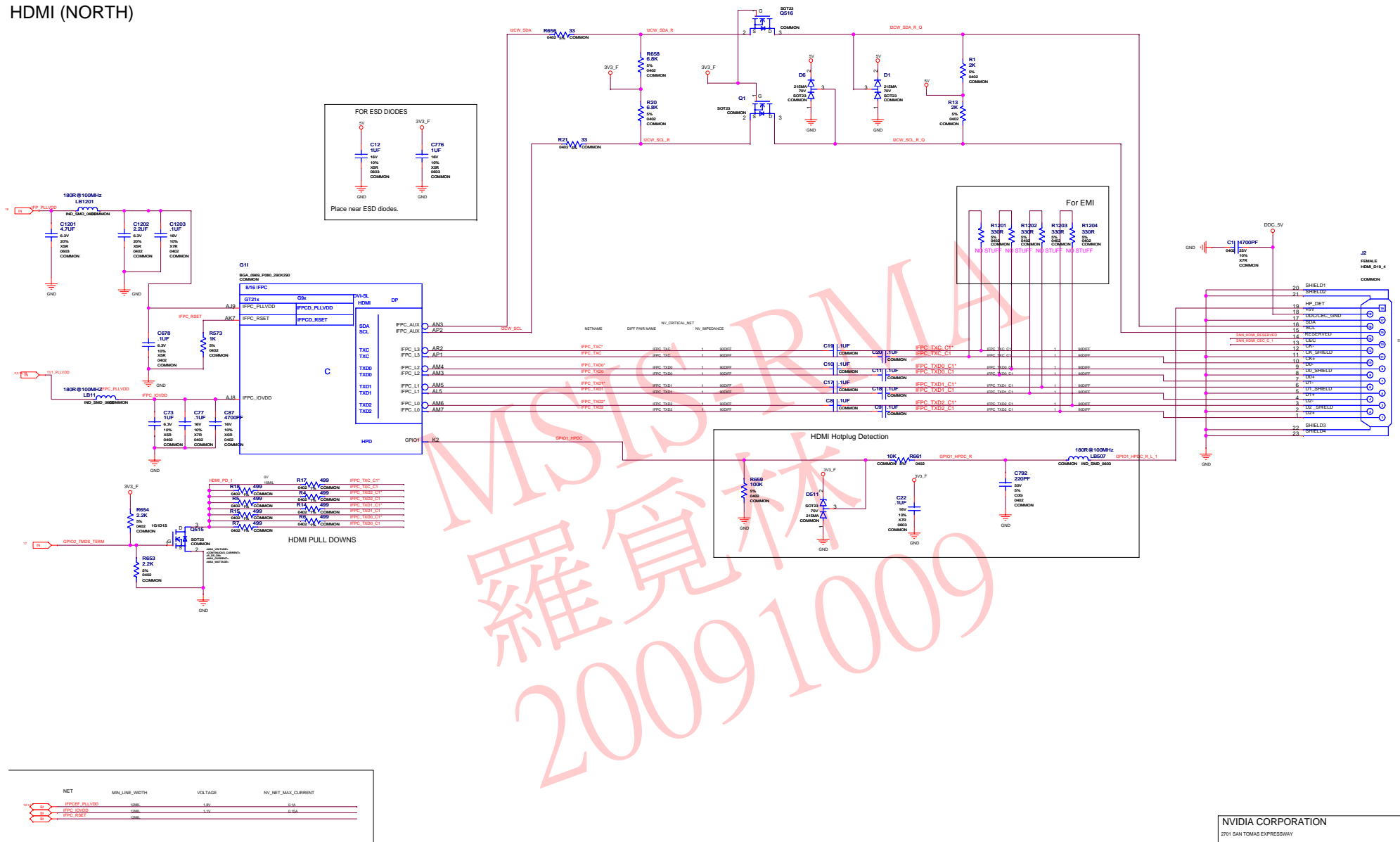
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NAME		DATE	15-MAY-2009

LINK C: HDMI
HDMI (NORTH)

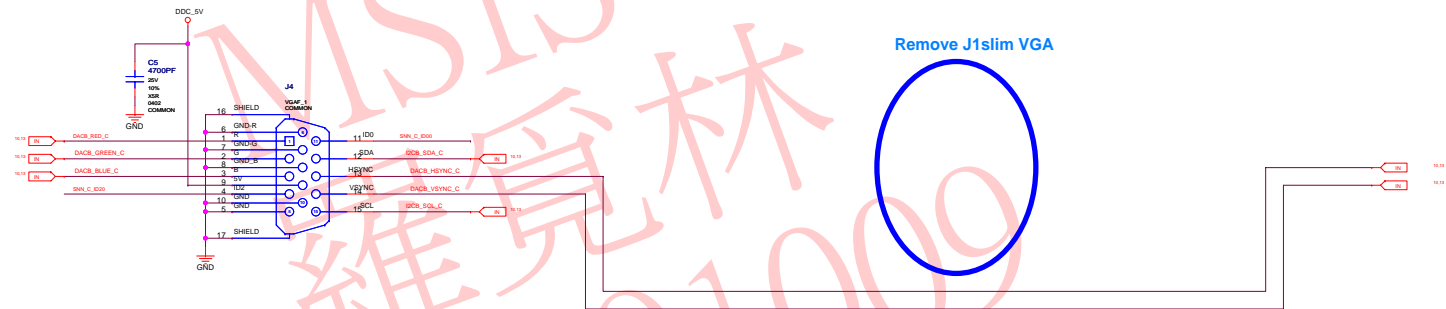
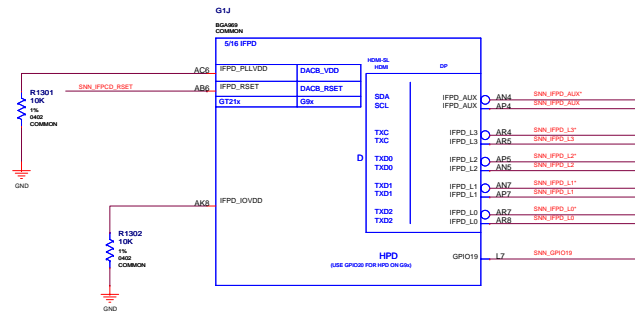


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK C: HDMI (NORTH)

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NAME		DATE	15-MAY-2009

LINK D (UNUSED) DISPLAYPORT, MID



Remove J1slim VGA

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK D: DISPLAYPORT (MID)

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK E/F: DVI-4 (MID)

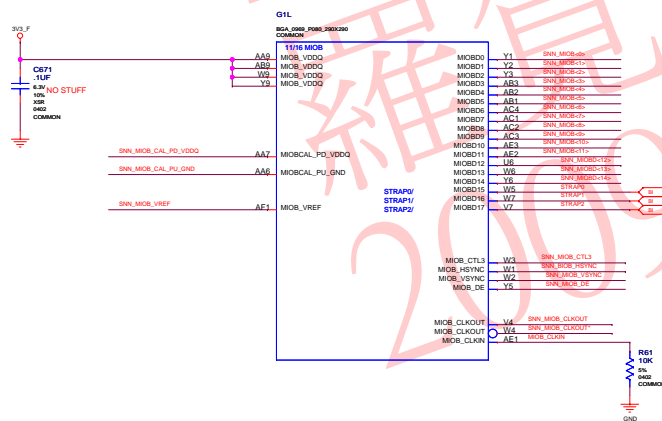
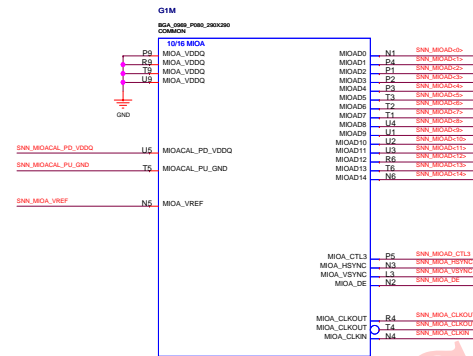
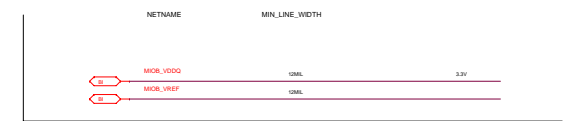
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MIOA/B SLI

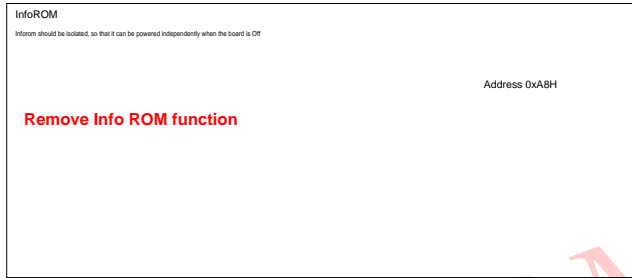


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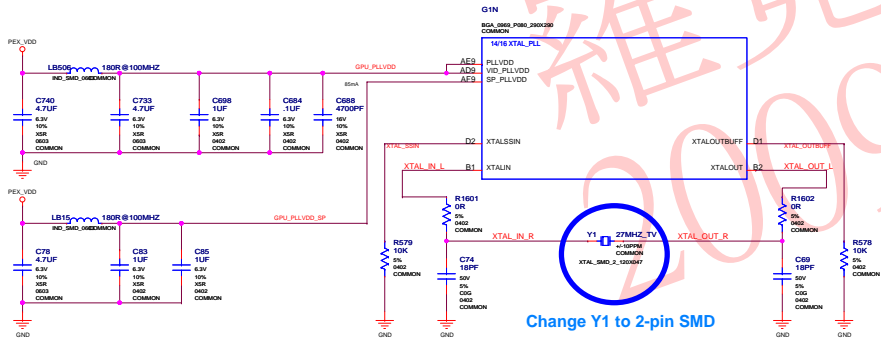
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB, SLI CONNECTOR

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NV_PN 600-10682-base-100 A			
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NAME		DATE	15-MAY-2009

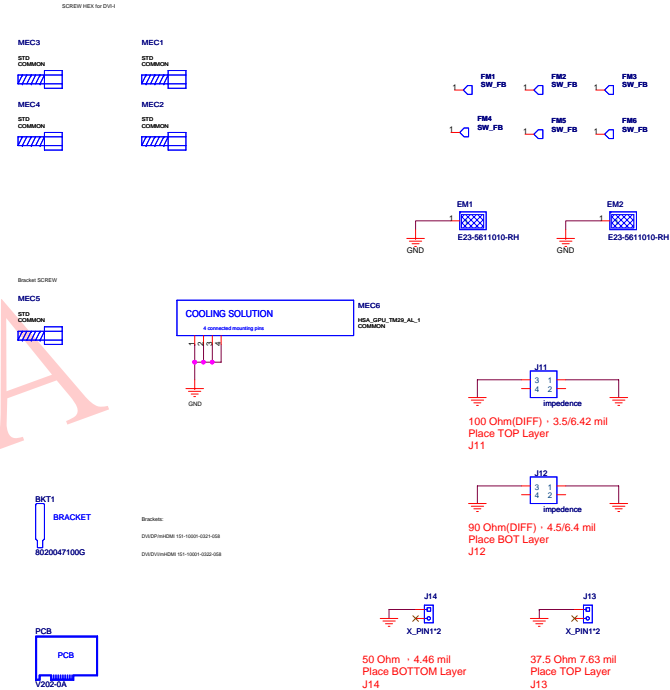
INFO_ROM/XTAL/PLLVDD



XTAL/GPU_PLLVDD



MECHANICALS & THERMALS



NETNAME	MIN_LINE_WIDTH
GPU_PLLVDD	120mil
GPU_PLLVDD_SP	120mil
XTAL_IN	100mil
XTAL_OUT	100mil
XTAL_SSIN	100mil
XTAL_OUTBUFF	100mil

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ASSEMBLY	BASE LEVEL: GENERIC BOARD; ONLY COMMON & NO. 31000 ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, MECHANICALS, THERMALS

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GPIO & JTAG

THERMAL SENSOR

I2C: 0x98H

OVERTEMP LATCH

NETNAME	MIN_LINE_WIDTH	VOLTAGE
THERM_DC	10MIL	
THERM_DC_B	10MIL	
THERM_DA_B	10MIL	
THERM_DC_R	10MIL	
GPIO_FAN_PWM_ALERT	8MIL	
GPIO_FAN_PWM_B	8MIL	
GPIO_FAN_PWM_G_L	8MIL	
GPIO_FAN_PWM_G	8MIL	
GPIO_FAN_PWM_R	8MIL	
GPIO_FAN_PWM_ALERT_B	8MIL	

Remove JTAG Connector

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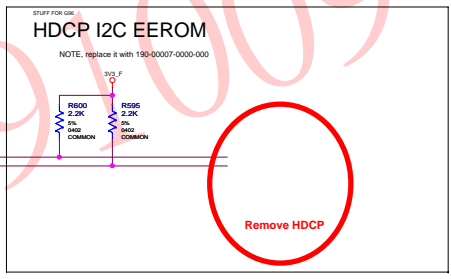
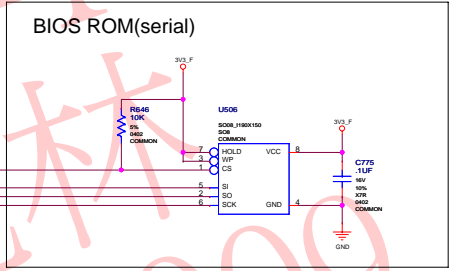
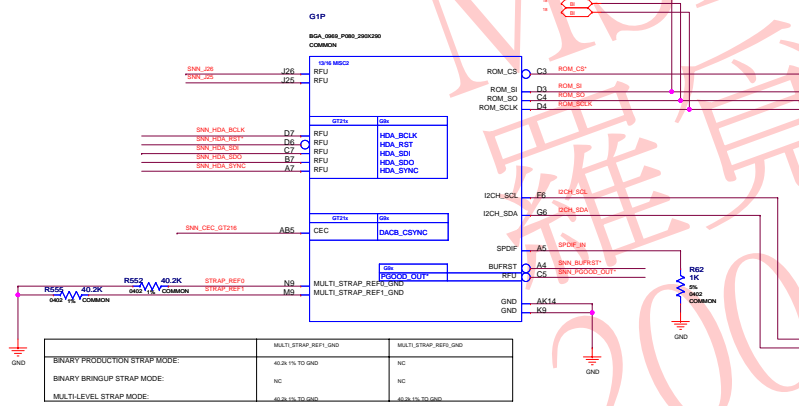
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ASSEMBLY	BASE LEVEL GENERIC BOARD ONLY, COMMON & NO 3V3/5V ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	EXTERNAL THERMAL SENSOR, FAN CONTROL, GPIO, JTAG

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Stream	USERID [E]	END. 1111	64 PU
Stream1	3500_PACQ020 [E]	DESKTOP 0000	56 PU
Stream2	PC1_DEV000 [E]	GT210-000 (GAT 0001)	104 PU
		0001 1000 640x16 D002 Samsung	1001 640x 640x16 D002 Samsung
		0001 1000 640x16 D002 Samsung	1001 640x 640x16 D002 Samsung
		0011 1000 640x16 D002 Hyun	1011 640x 640x16 D002 Hyun
RCM_S1	RAMC020 [E]	0101 1000 320x16 D002 Samsung	1101 640x 320x16 D002 Samsung
		0101 1000 320x16 D002 Samsung	1101 640x 320x16 D002 Samsung
		0111 1000 320x16 D002 Hyun	1111 640x 320x16 D002 Hyun
RCM_SCLX	3. PC1_DEV00_EXT 2. SDR_VID000 (1 - BIOS not present) 1. SLOT_CLK, CP12 (1 - common for MCH0GPU) 0. PEK_PUL_IN_TERR (0 - disable pin term)	0110	320 PU
RCM_SO	3. CLK_47.15 (1 - J008 27MHz) 2. PU_0_VDD_3.0V (0 - J008 3.000V) 1. SDR_A11_A00 (0 - J008) 0. VDD_0V000 (0 - J008)	0001	56 PU
		0 PU 1A	8 PU 1A
		1 PU 1A	9 PU 1A
		2 PU 1A	10 PU 1A
		3 PU 1A	11 PU 1A
		4 PU 1A	12 PU 1A
		5 PU 1A	13 PU 1A
		6 PU 1A	14 PU 1A
		7 PU 1A	15 PU 1A



	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION STRAP MODE:	40.2k 1% TO GND	NC
BINARY BRINGUP STRAP MODE:	NC	NC
MULTI-LEVEL STRAP MODE:	40.2k 1% TO GND	40.2k 1% TO GND

Remove HDCP

A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

NO STUFF

MODE: SMD, MELF

D1804 1

R1804 100k

D1805 10k

COMMON

V

EC133 47uF

10V

10%

10%

10%

COMMON

U5

VIN

Vout(TAB)

D

APL1117

ICL_T0252-3-RH

ER304 200R

ER305 619R

EC134 10uF

10V

10%

10%

10%

COMMON

5V

VOUT = (14RvalReg)*VREF + (1+14R200)/1.25 + 5.12V

F: POLYSW, 120670A075A2C8B

F502

7500mA

1206

COMMON

1

2

POLYSWITCH

5V

DCD 5V

[illegible]

3.3V

U3
ADJ_VREG=0V
3.3V
COMMON

IN OUT
EN ADJ
GND

C1901 1µF
0.33V
10%
XGR
COMMON

GND

R1901 3.57K
0402
COMMON

R1902 11.5K
0402
COMMON

R1903 10K
0402
COMMON

PEX_PL1VDD

C1902 1µF
0.33V
10%
XGR
COMMON

C1903 4.7µF
0402
COMMON

PEX_PL1VDD

Total = 1.05V (1.05V@170mA)
1.05V = 3.3V / (1 + 1901/1902)

Bypass inductor with OR

LB15 600R @ 100MHz

IND_SMD_0805040001H

LB15 600R @ 100MHz

IND_SMD_0805040001H

3V3_O 3V3_F

	NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
	SV_FUSED	0.1A	120MIL	5V
	SV_300V1	0.0A	120MIL	5V
	SV_300C	0.1A	120MIL	5V
	SV_500C	0.1A	120MIL	5V
	SV	0.0A	120MIL	5V
	PS_1V8_A0J1		120MIL	1.8V
	1V8	0.12A	120MIL	1.8V
	GND		100MIL	0V
	3V3_F	6A	20MIL	3.3V
	3V3_VF		20MIL	3.3V
	3V3_V0V0	0.3A	20MIL	3.3V
	12V_F	6A	20MIL	12V

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY LINEARS: 5V, DDC5V, IFP PLLVDD, IFP IOVDD, 3V3 FILTER, 12V FILTER, 12V EXT



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FBVDDQ: 1.8-2.0V @ 12.7A



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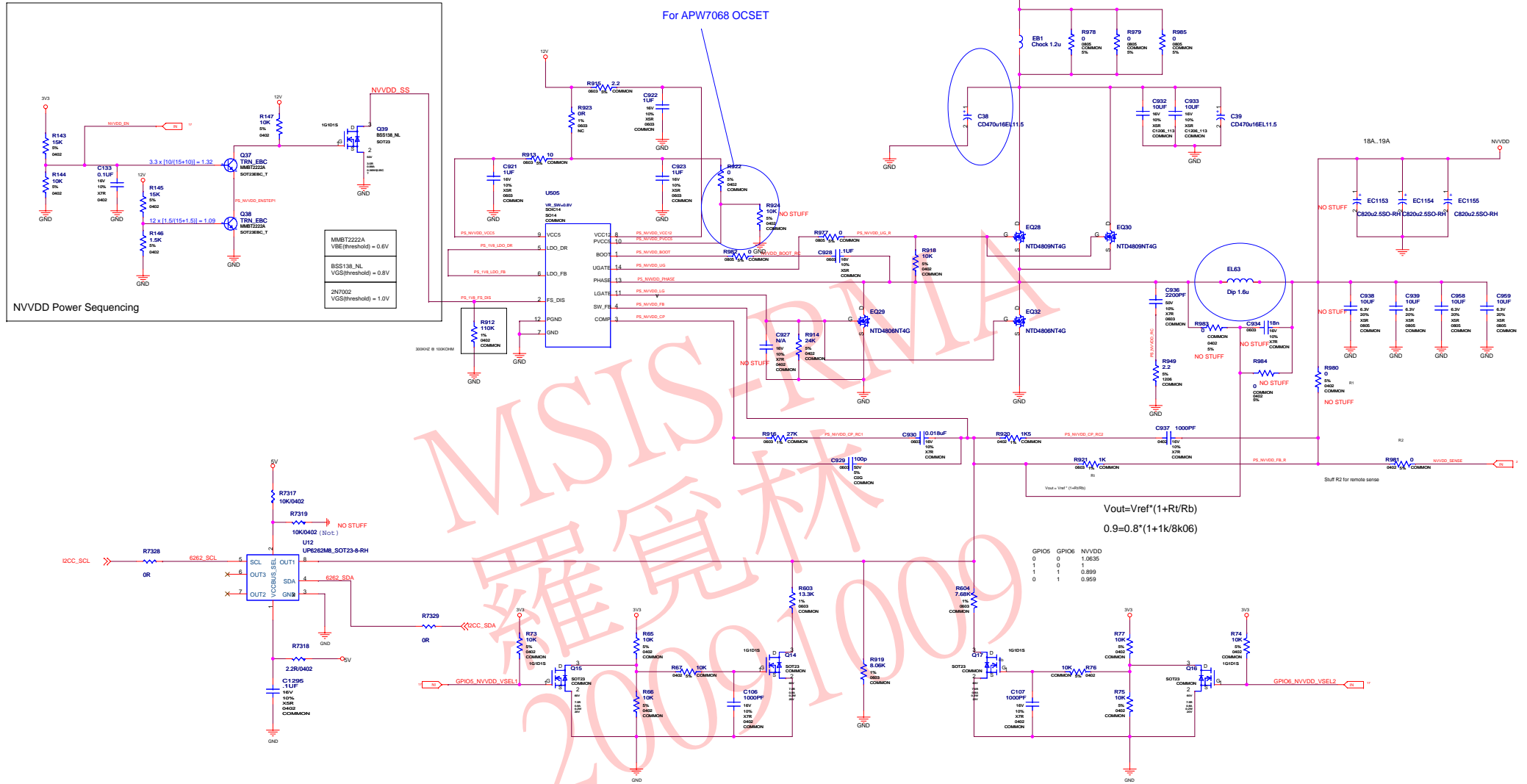
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: FBVDDQ SINGLE PHASE SWITCHER, PEX_VDD LINEAR

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POWER SUPPLY: NVVDD



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: NVDD DUAL PHASE SWITCHER

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