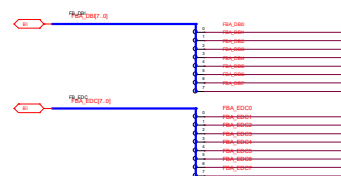
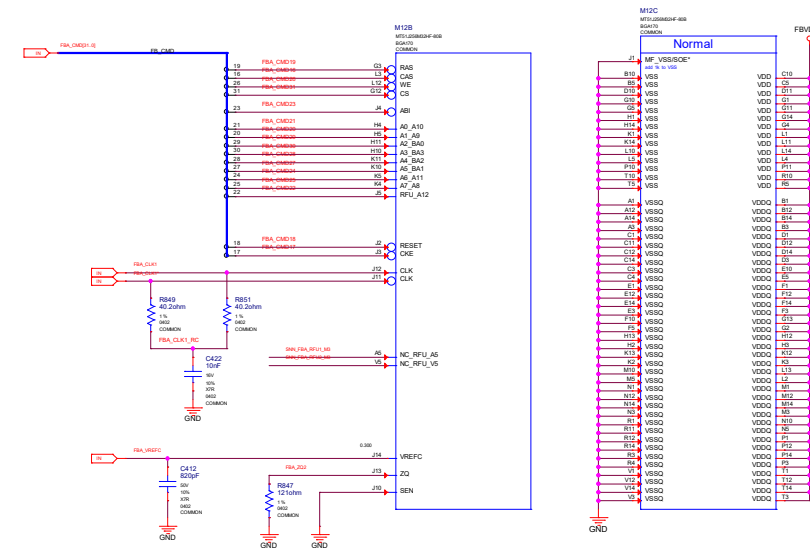
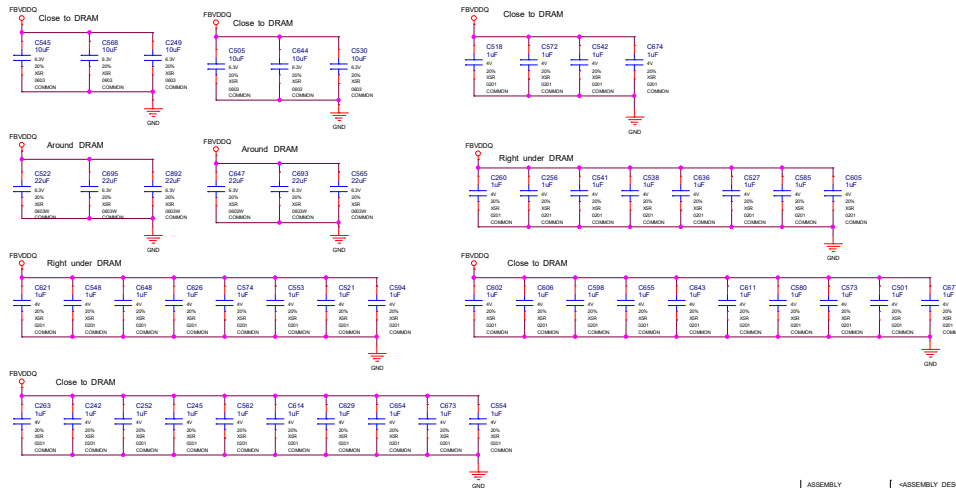
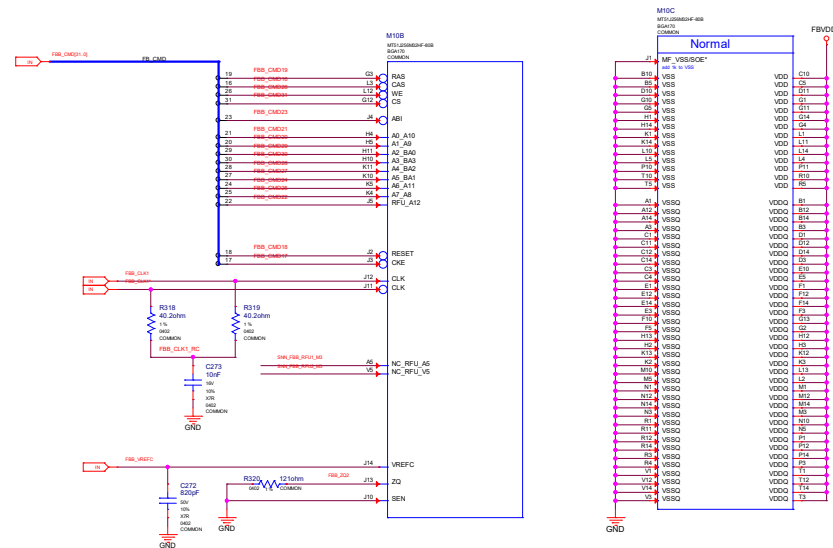
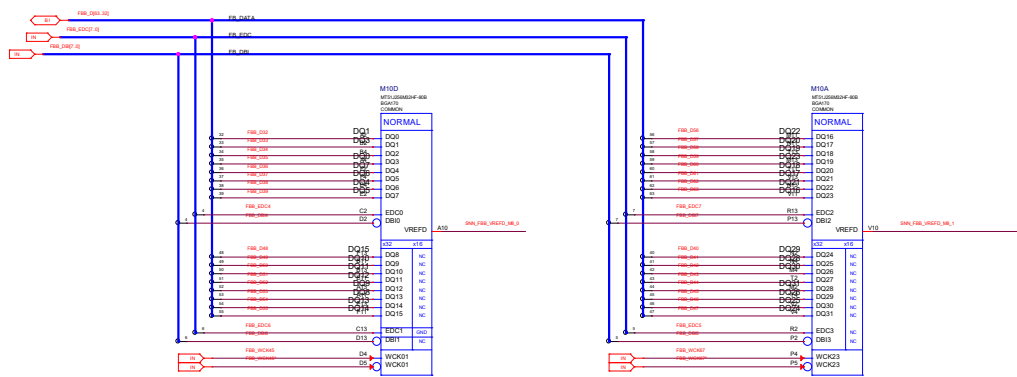


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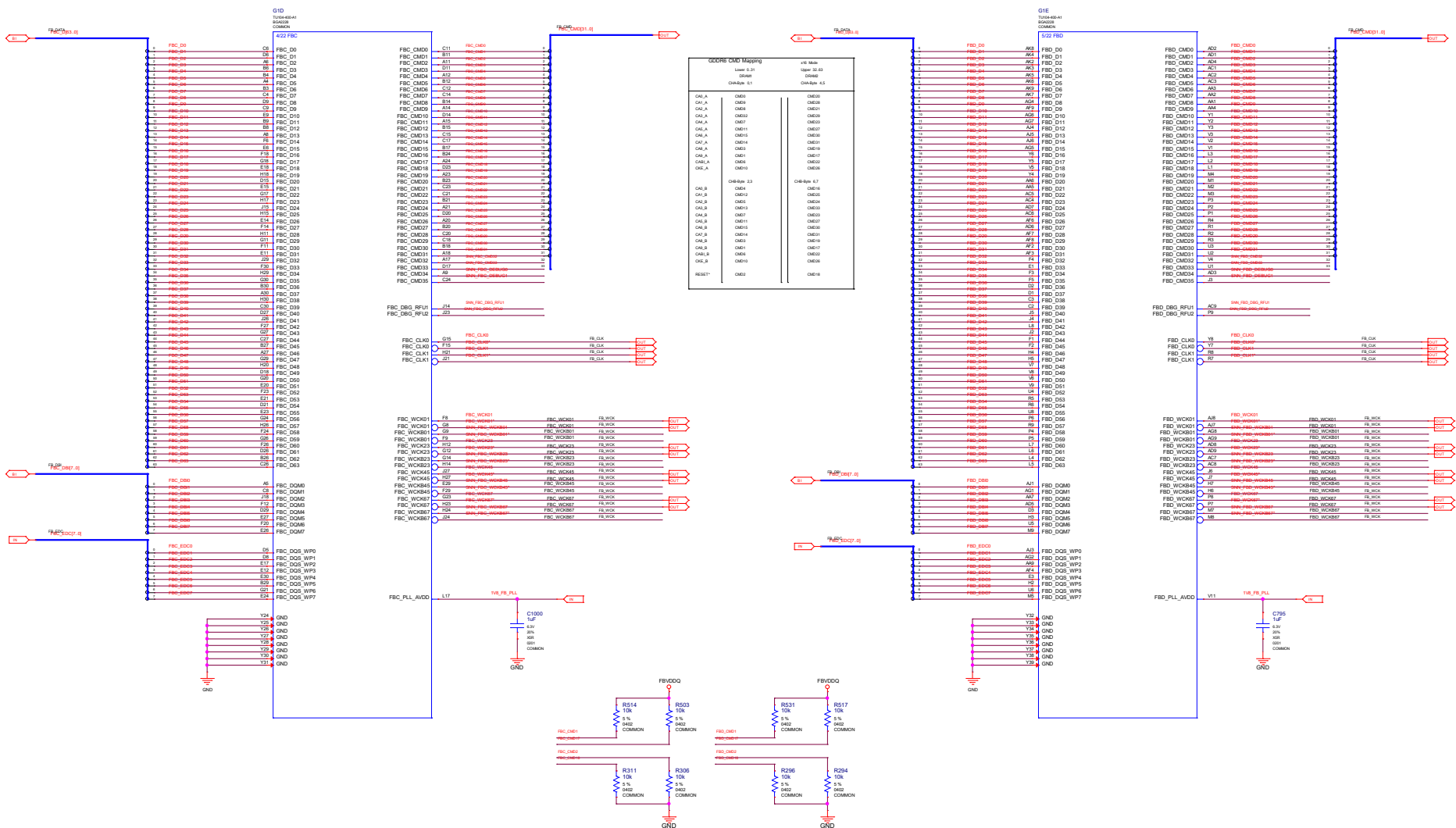






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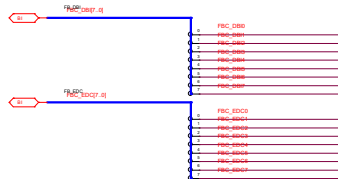
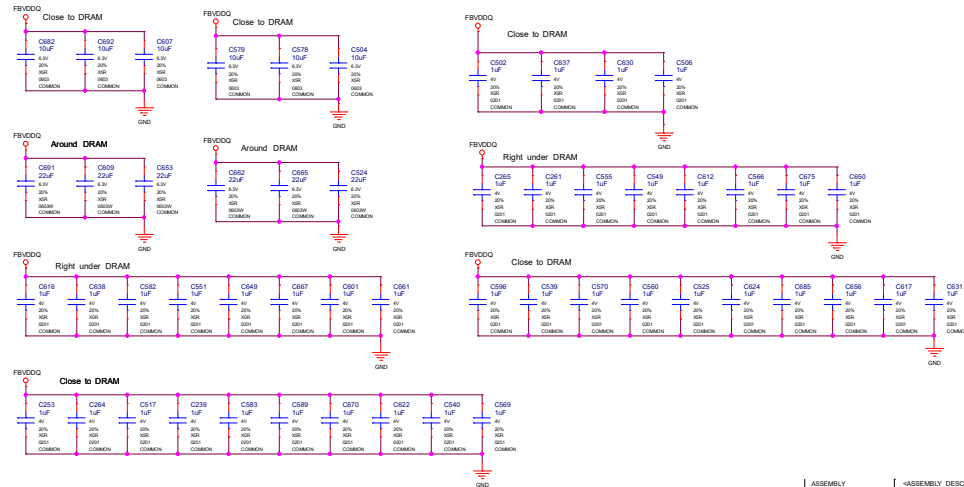
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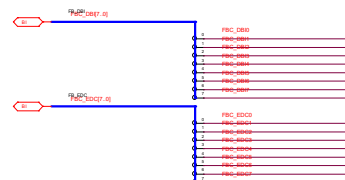
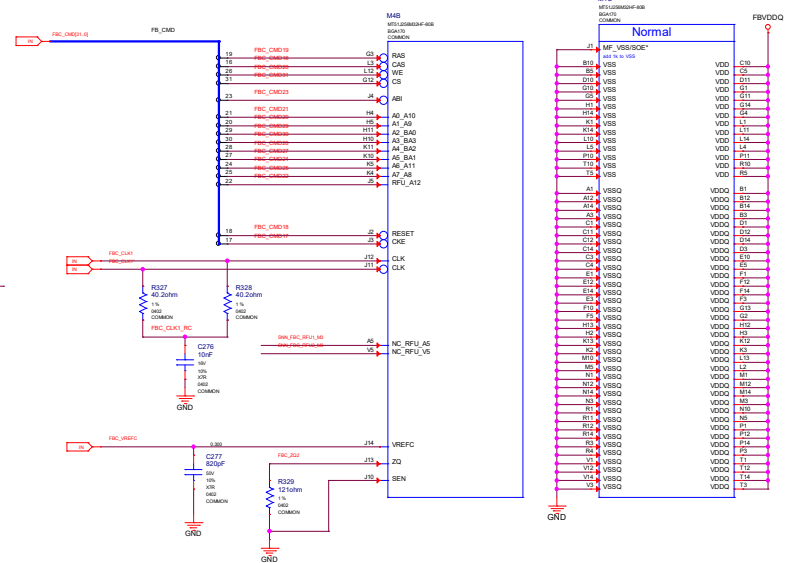
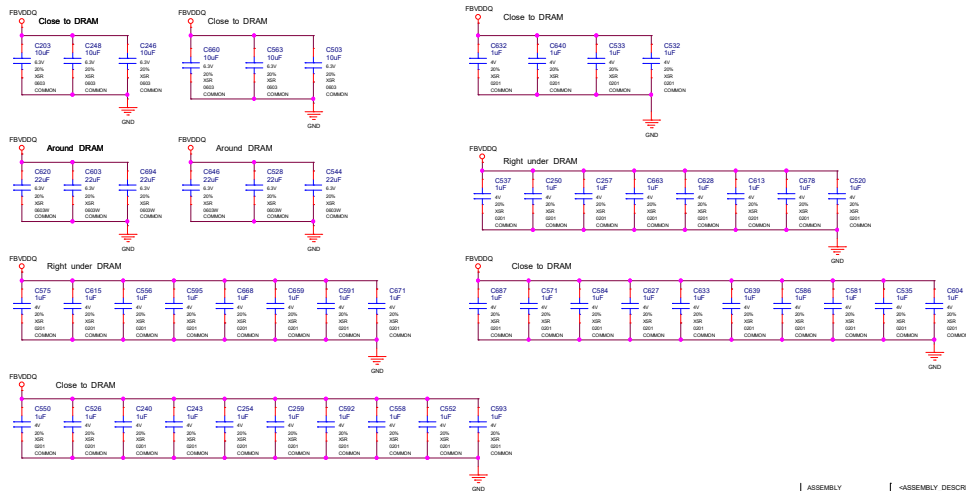
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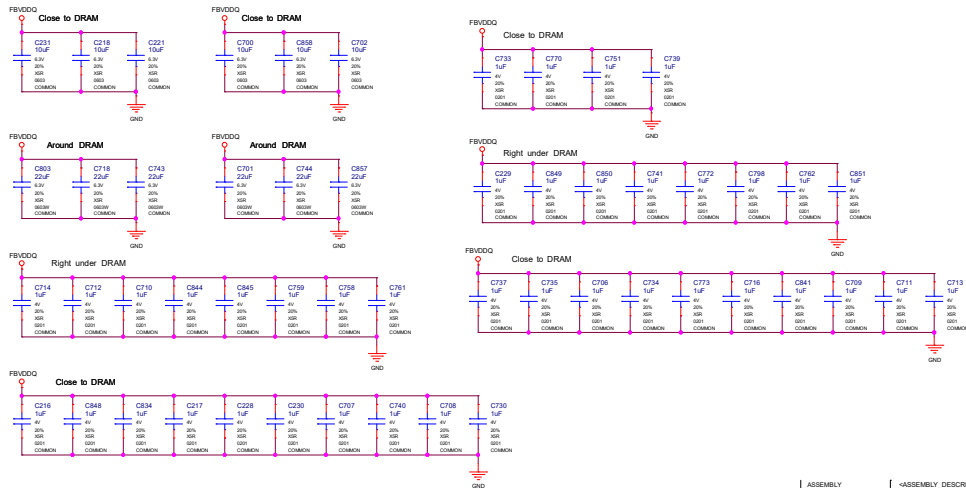
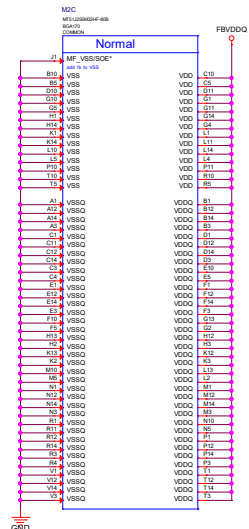
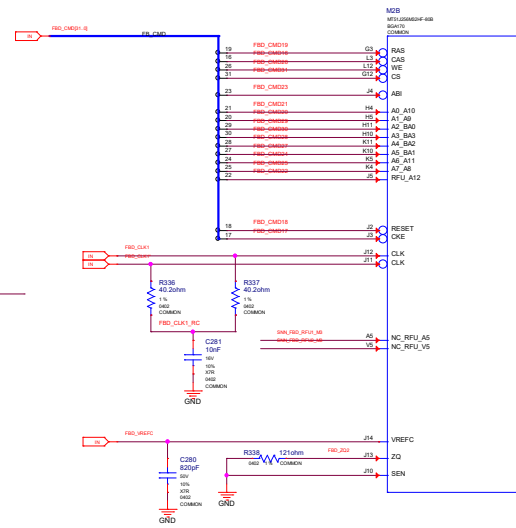
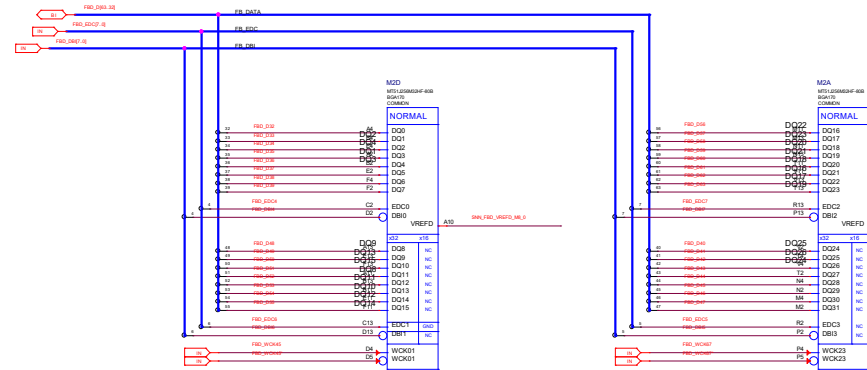
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ASSEMBLY  
PAGE DETAIL  
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MEMORY: FB003.32




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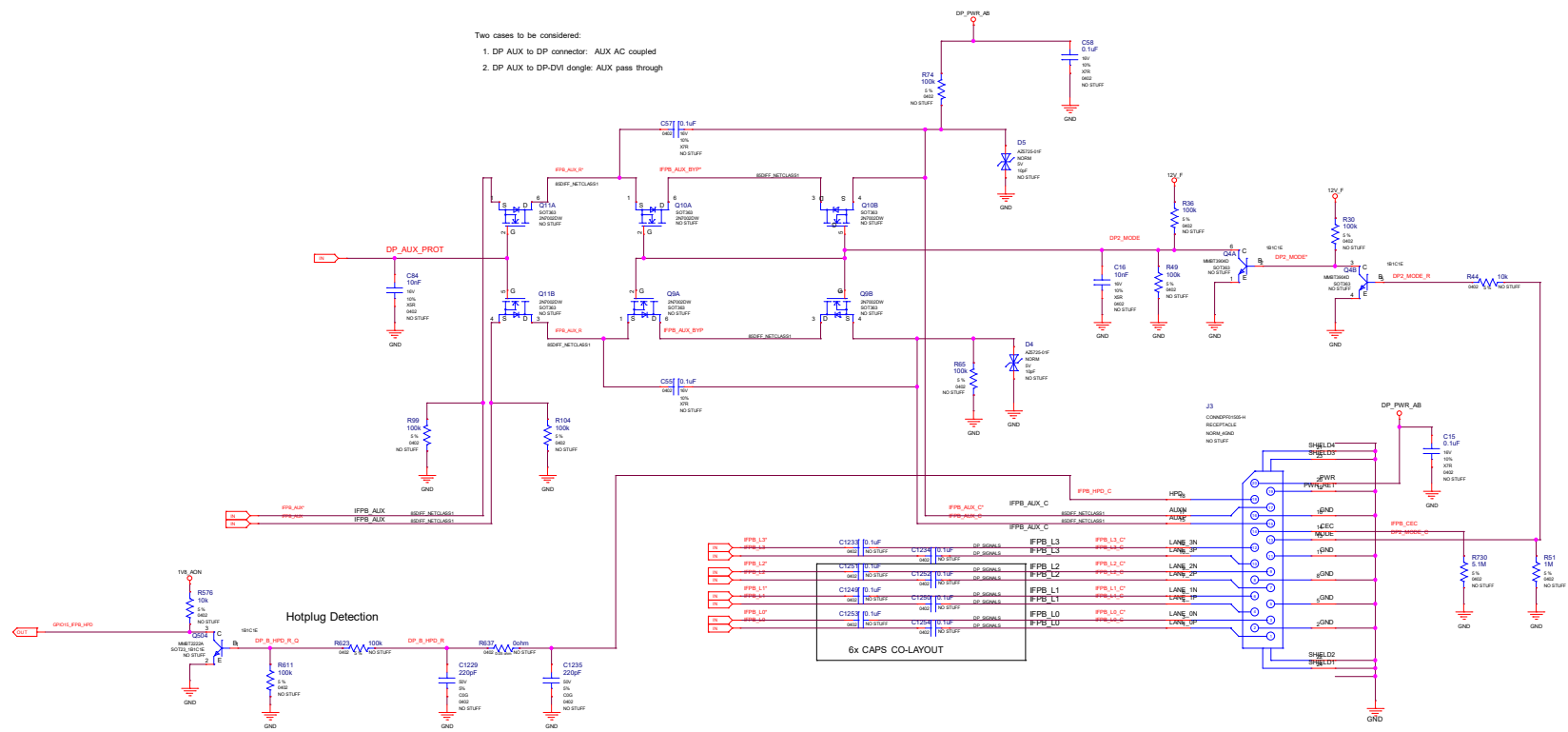


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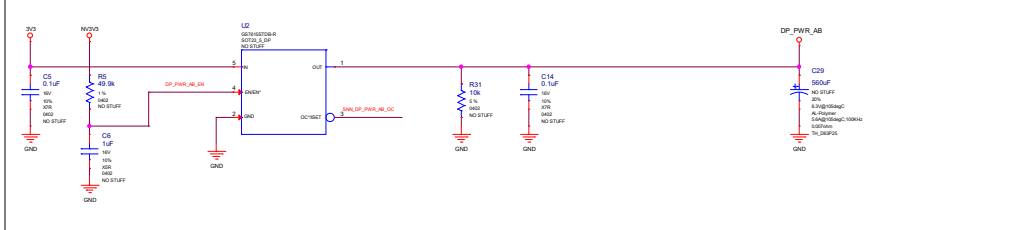
# IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



## Fused DP\_PWR



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IQ: IFPB DP

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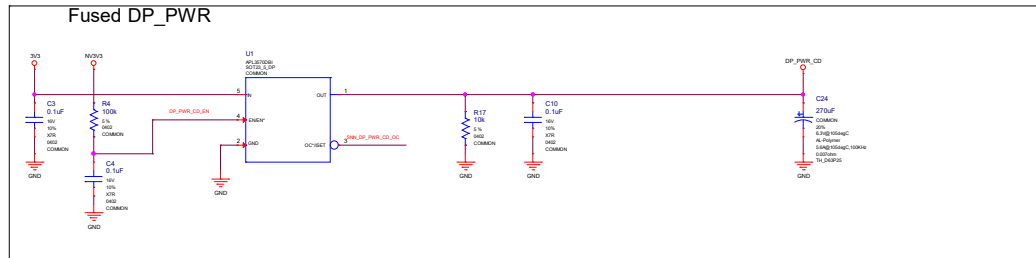
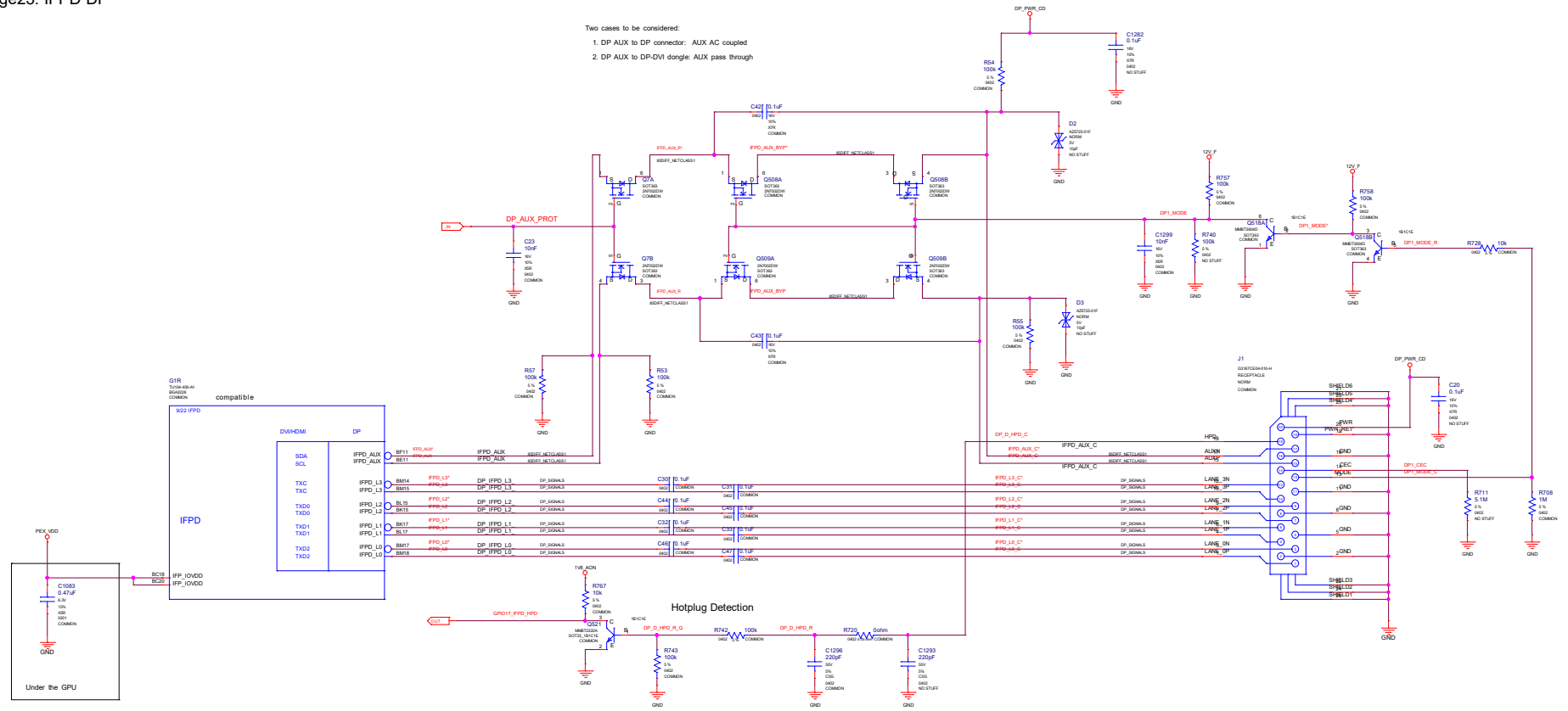


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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFFD DP

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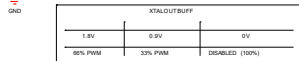



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00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

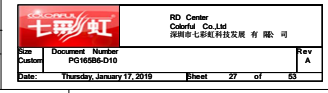
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M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

```
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```



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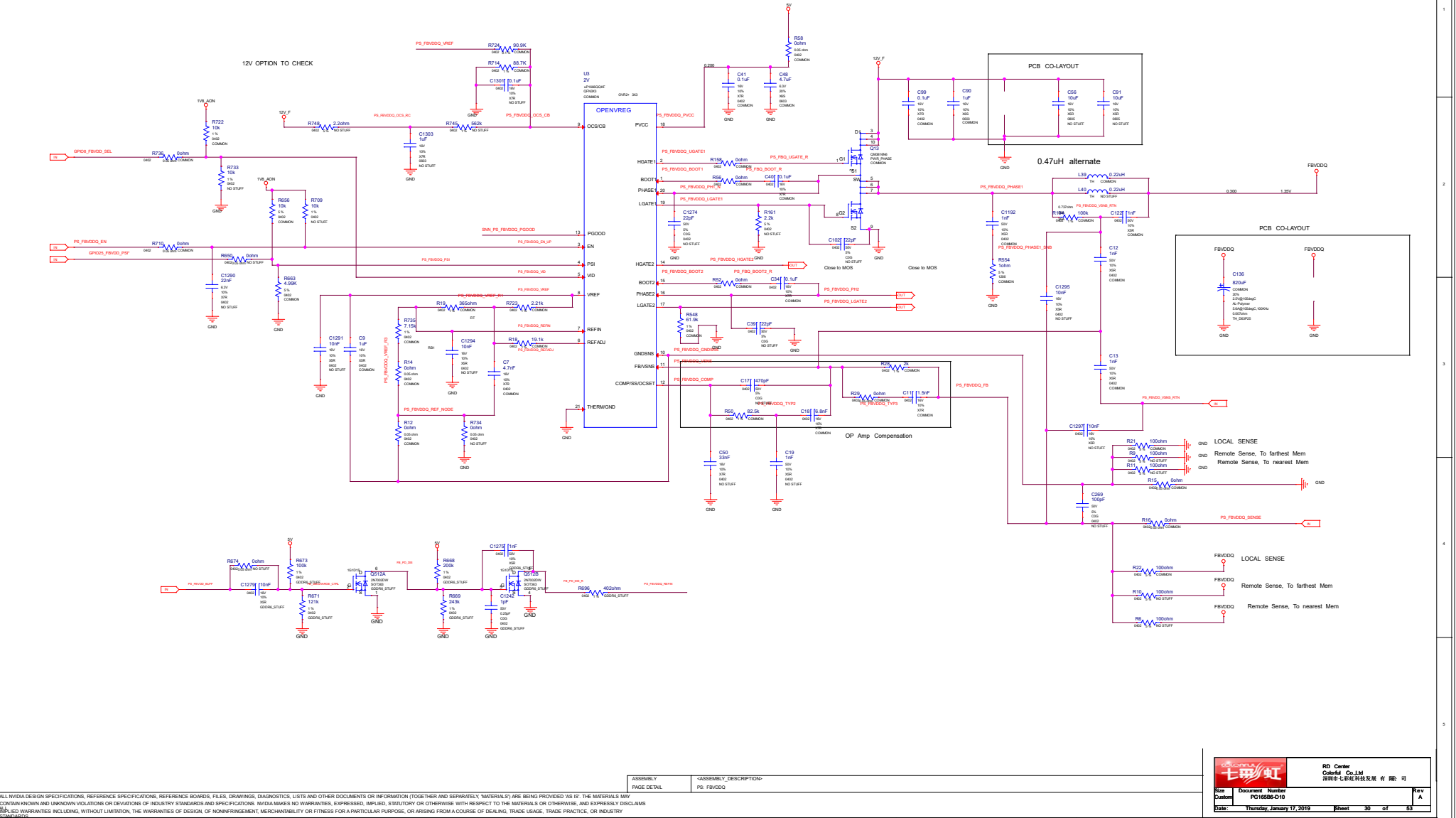




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DROP OVR3i SOLUTION

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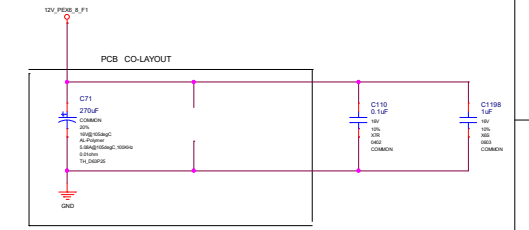
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PAGE DETAIL	PS: NVVDD Controller OVR3i




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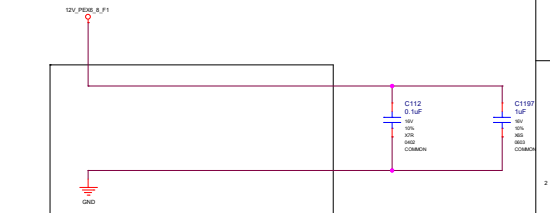
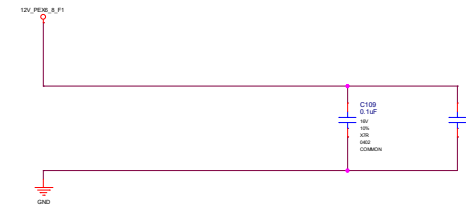
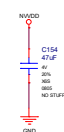


Figure 1 shows two schematic diagrams of test boards. The left board, labeled C144, features a network analyzer port connected to a 50 ohm load, a 100 pF capacitor, and a 50 ohm load, with a 100 pF capacitor and a 50 ohm load in parallel. The right board, labeled C154, features a network analyzer port connected to a 50 ohm load, a 100 pF capacitor, and a 50 ohm load, with a 100 pF capacitor and a 50 ohm load in parallel.




ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVDD Phase 2,1

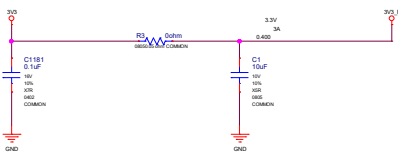
DELETE RAIL BALANCE CIRCUIT

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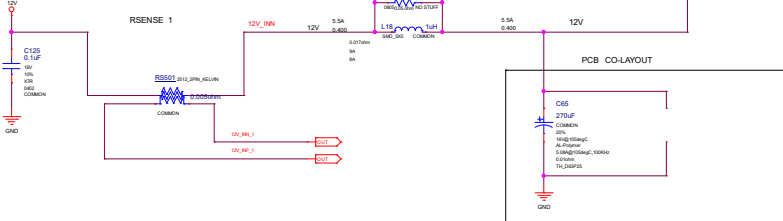
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PAGE DETAIL	PS: Input Power Balancing Switcher

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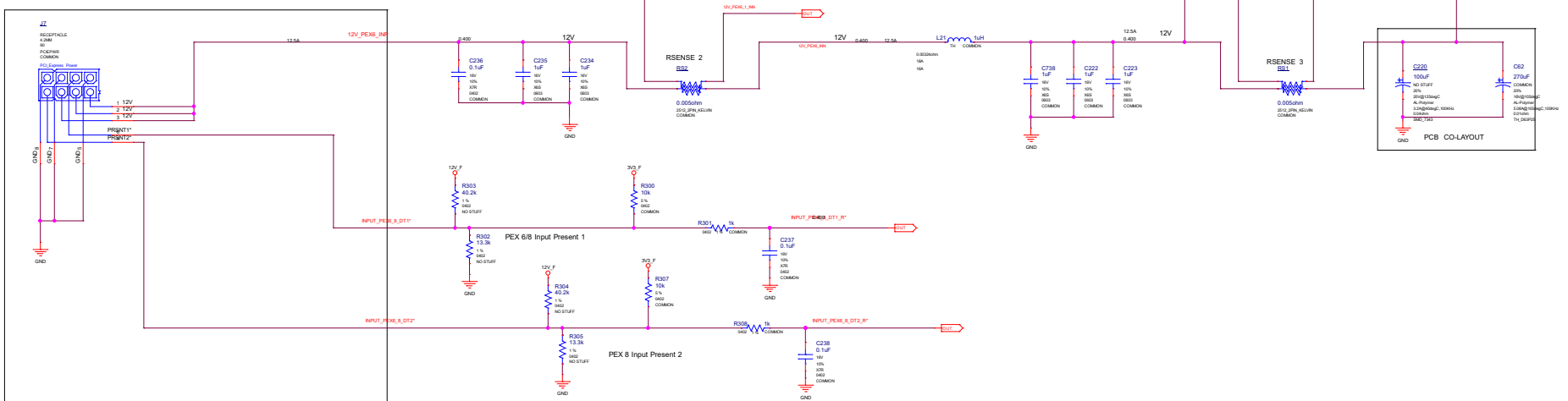
### PEX 3V3 INPUT - 10W



### PEX\_12V INPUT - 66W




### PEX8 INPUT 1 - 2x4 PCIE CON 150W




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ASSEMBLY PAGE DETAIL  
"ASSEMBLY" DESCRIPTION:  
PS Input, Filtering, and Monitoring

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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	PB_Type-C BuckBoost




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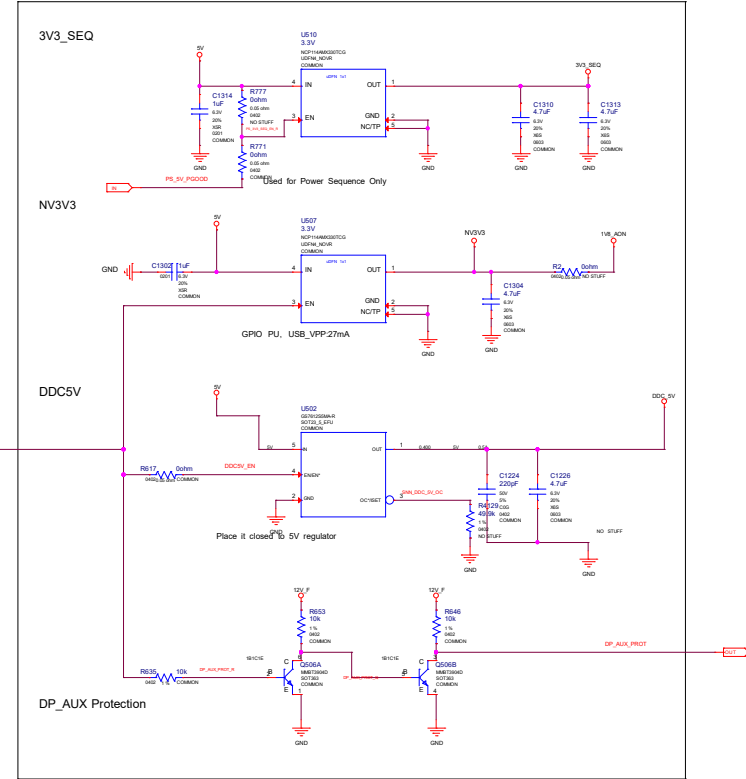
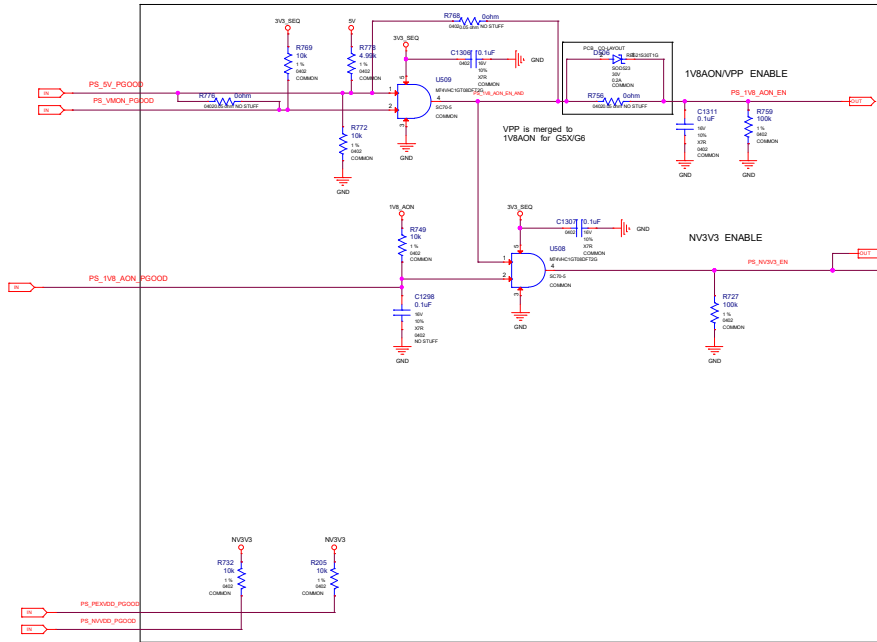
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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PD-PPC



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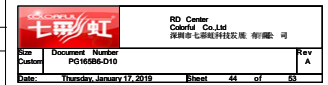


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ASSEMBLY	ASSEMBLY DESCRIPTION
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PAGE DETAIL	SEQ. VOLTAGE MONITOR



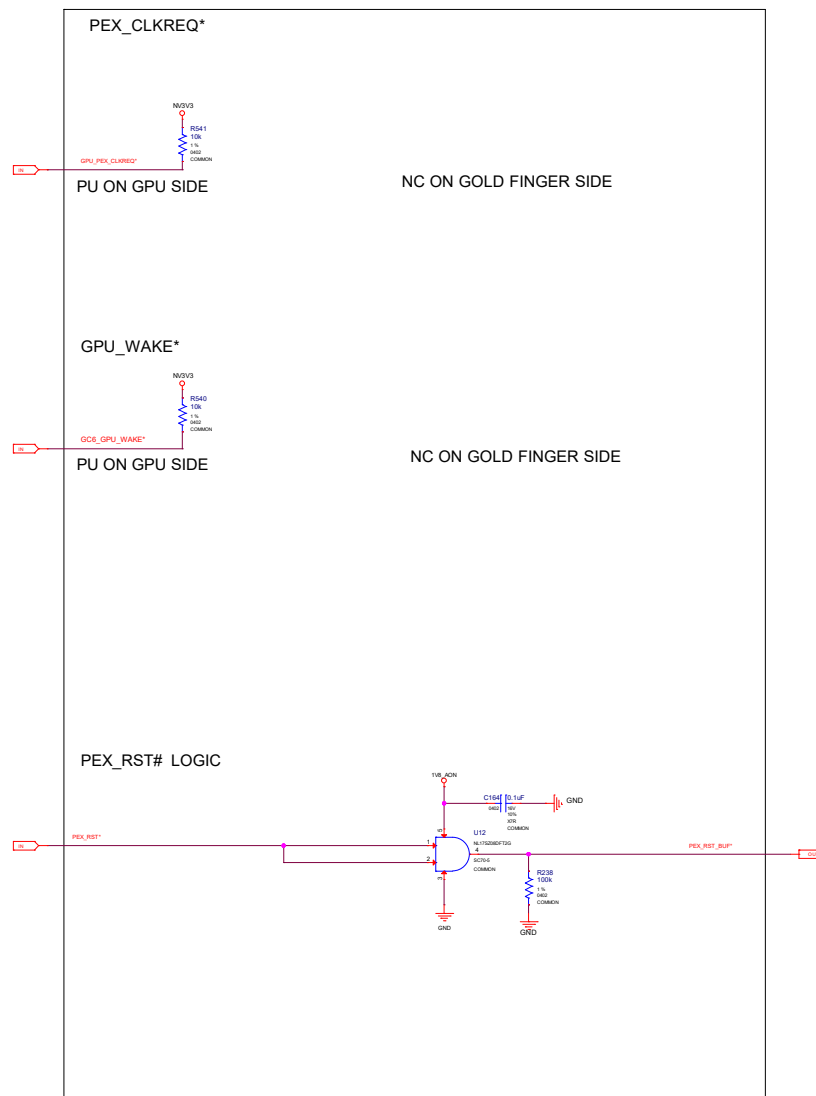
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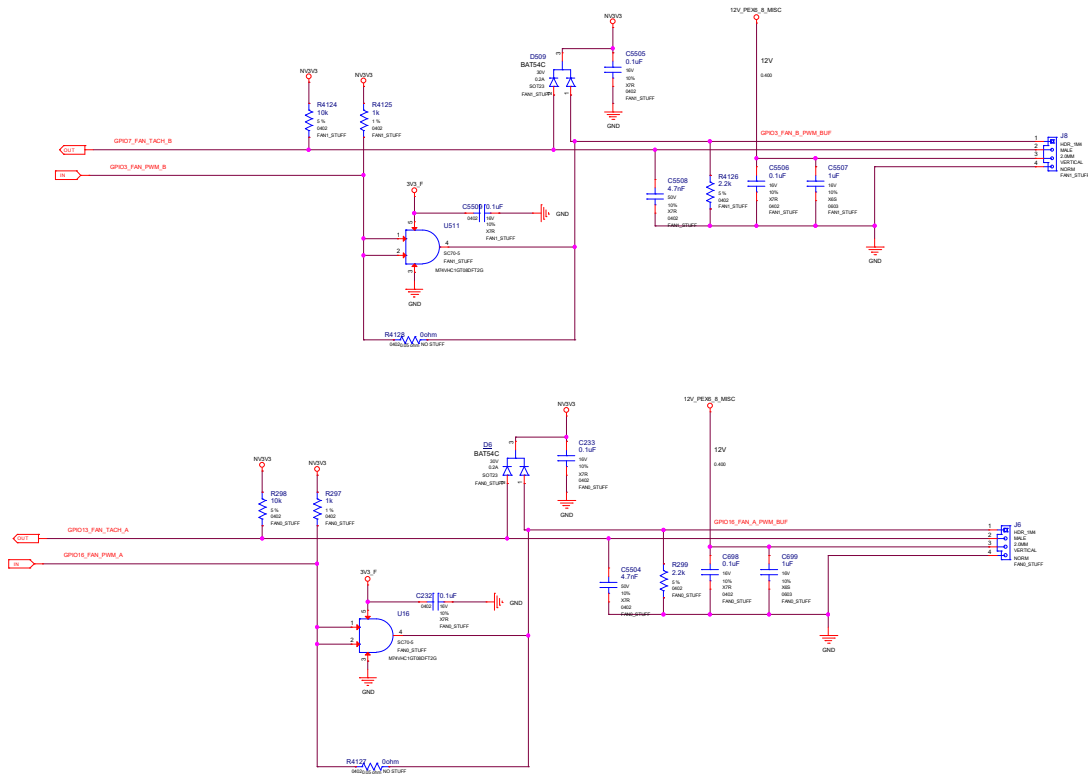
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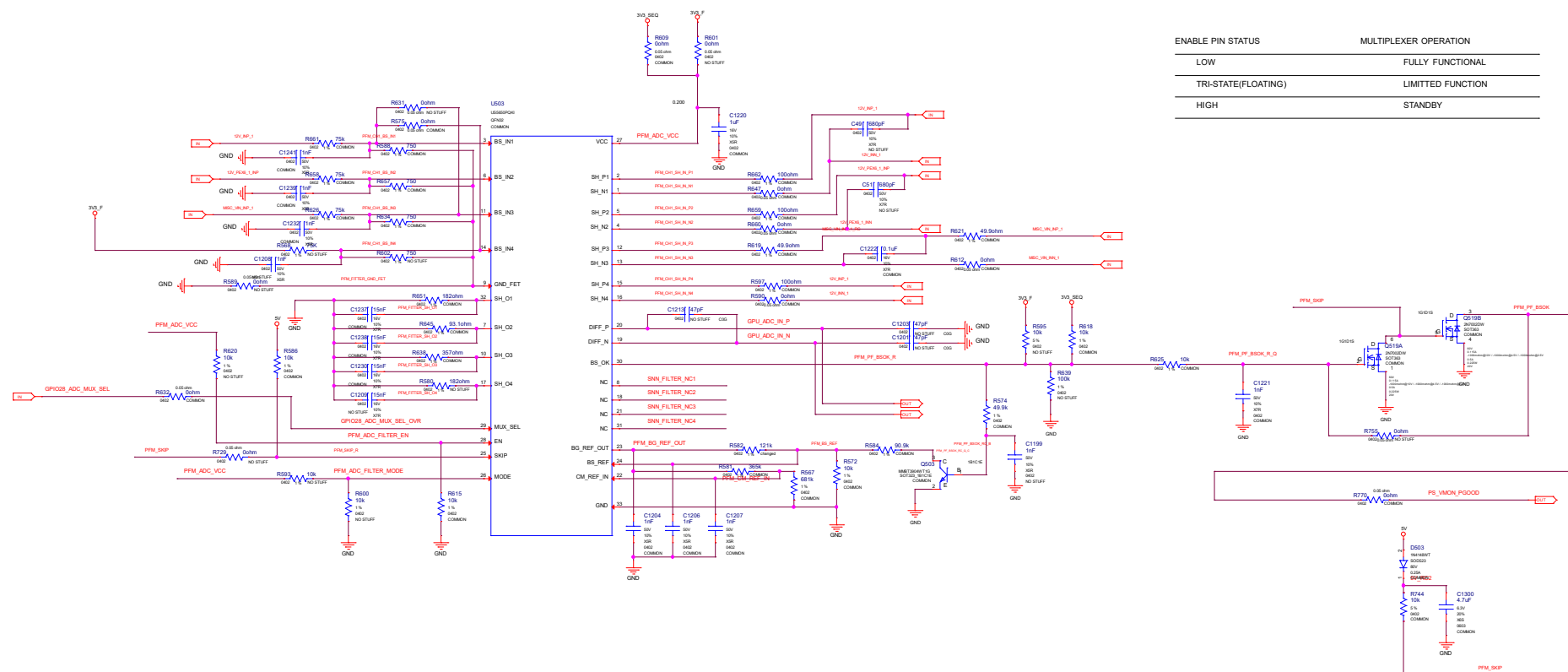
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MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

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