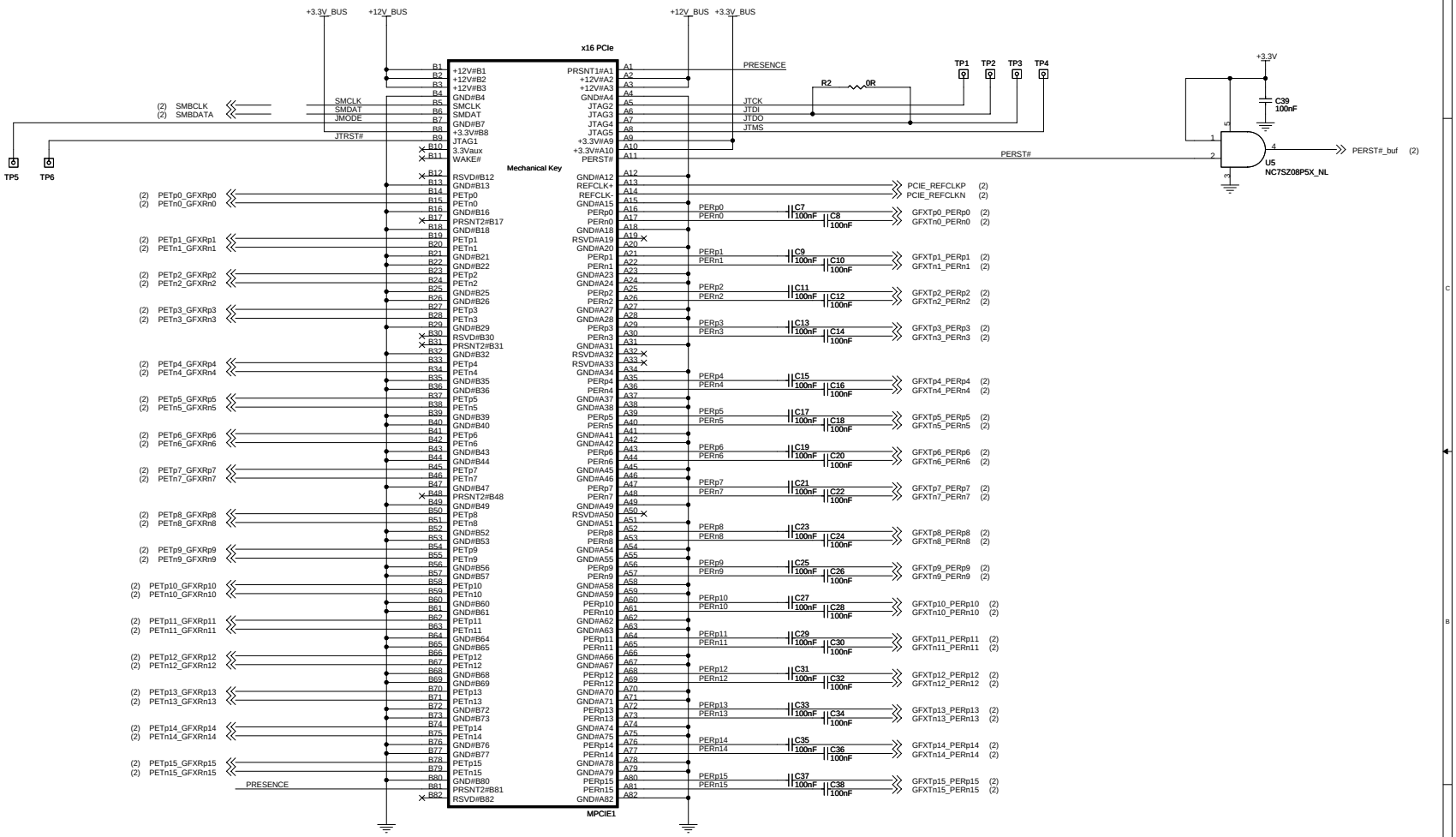
PCI-EXPRESS EDGE CONNECTOR



+12V_BUS

CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX

+12V_BUS +12V_BUS

C2 150nF_16V

C3 150nF_16V

LF CAP CER 150NF 10% 16V X7R (0603)

+3.3V_BUS

CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

+3.3V_BUS

C5 1uF_6.3V C6 1uF_6.3V C0 10nF

Place these caps last, ideally as close to the bus connector as possible

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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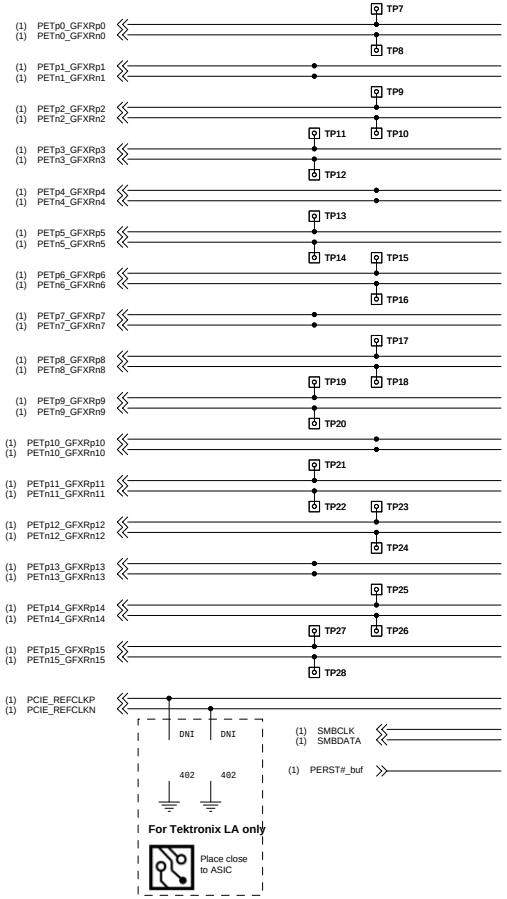
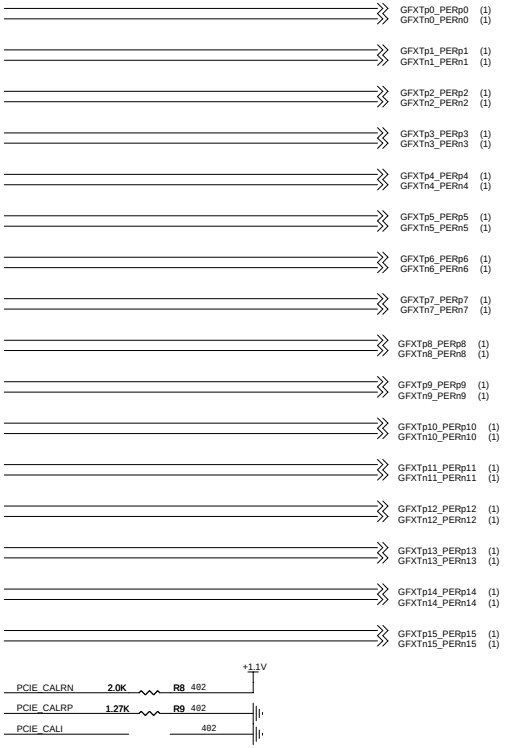
NOTE: some of the PCIE testpoints will
be available through via on traces.





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Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI

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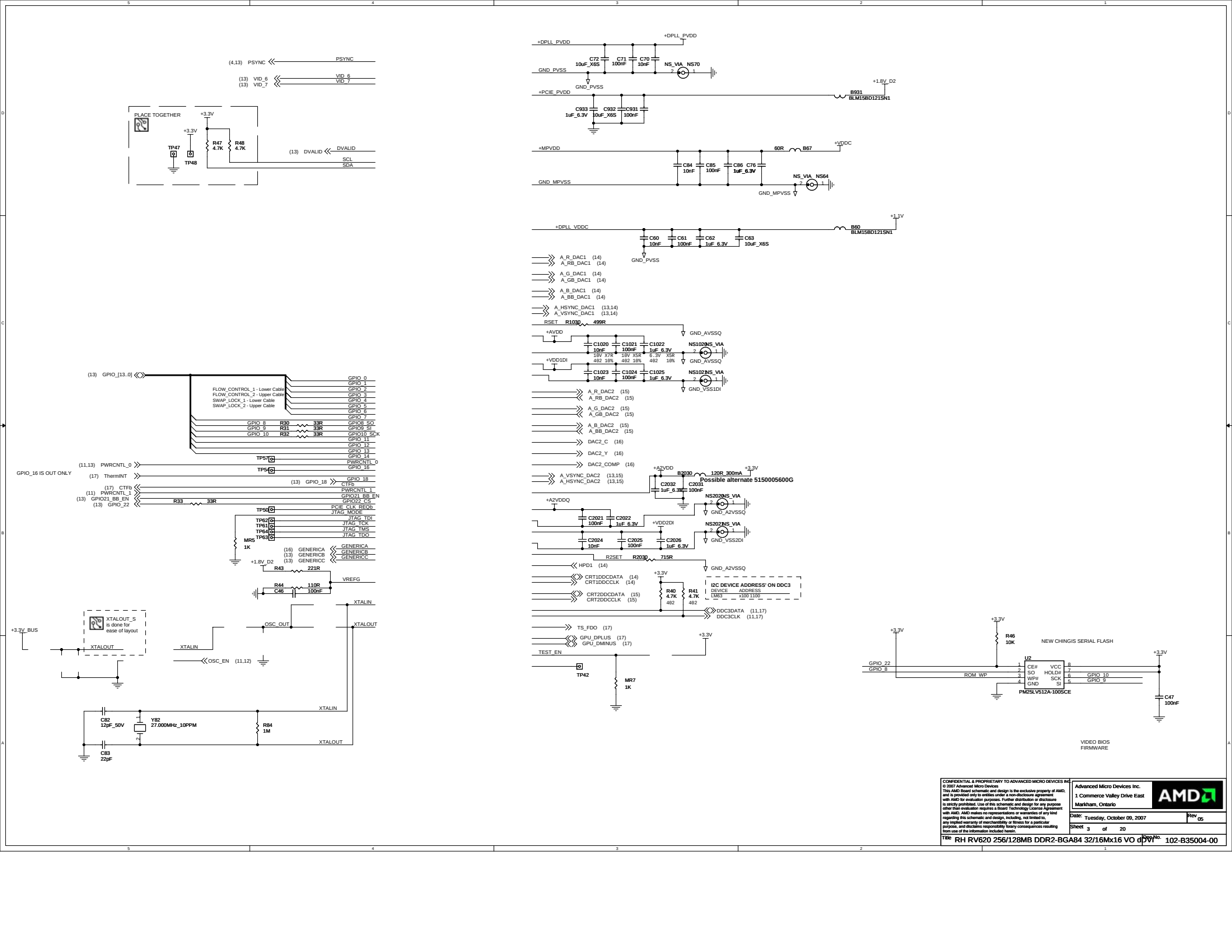

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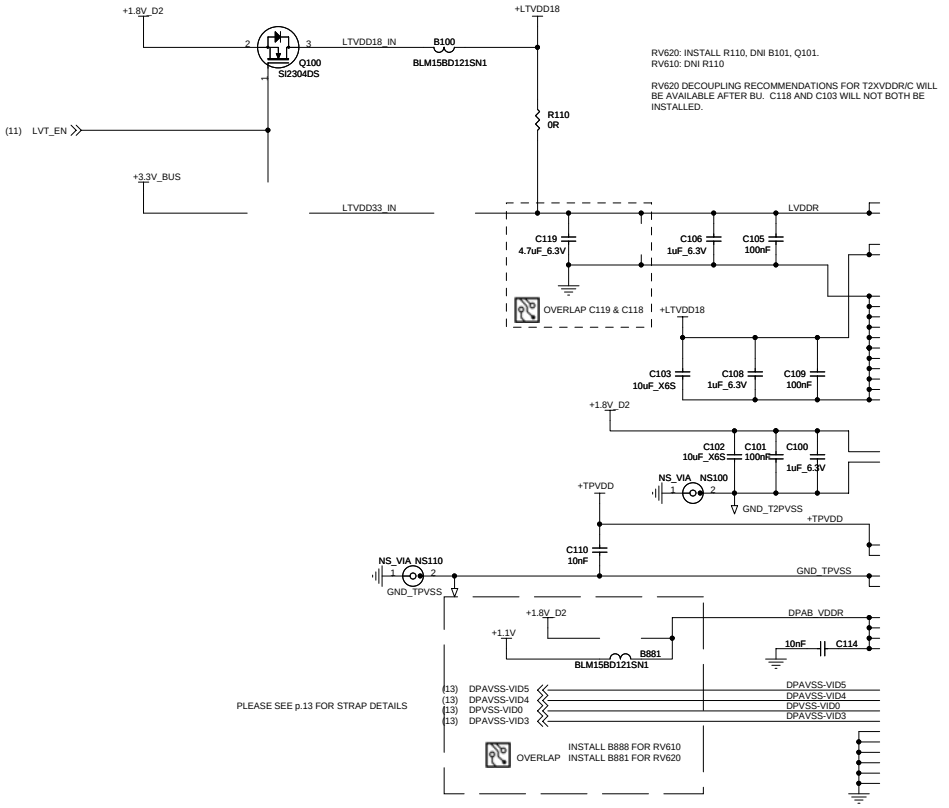
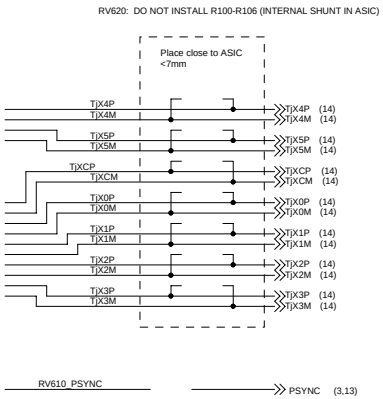
Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No. 102-B35004-00





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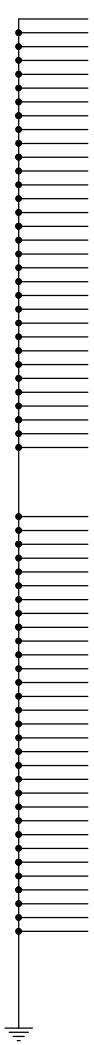

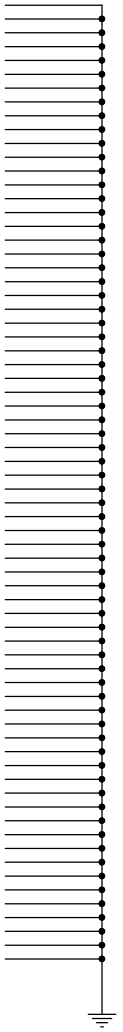

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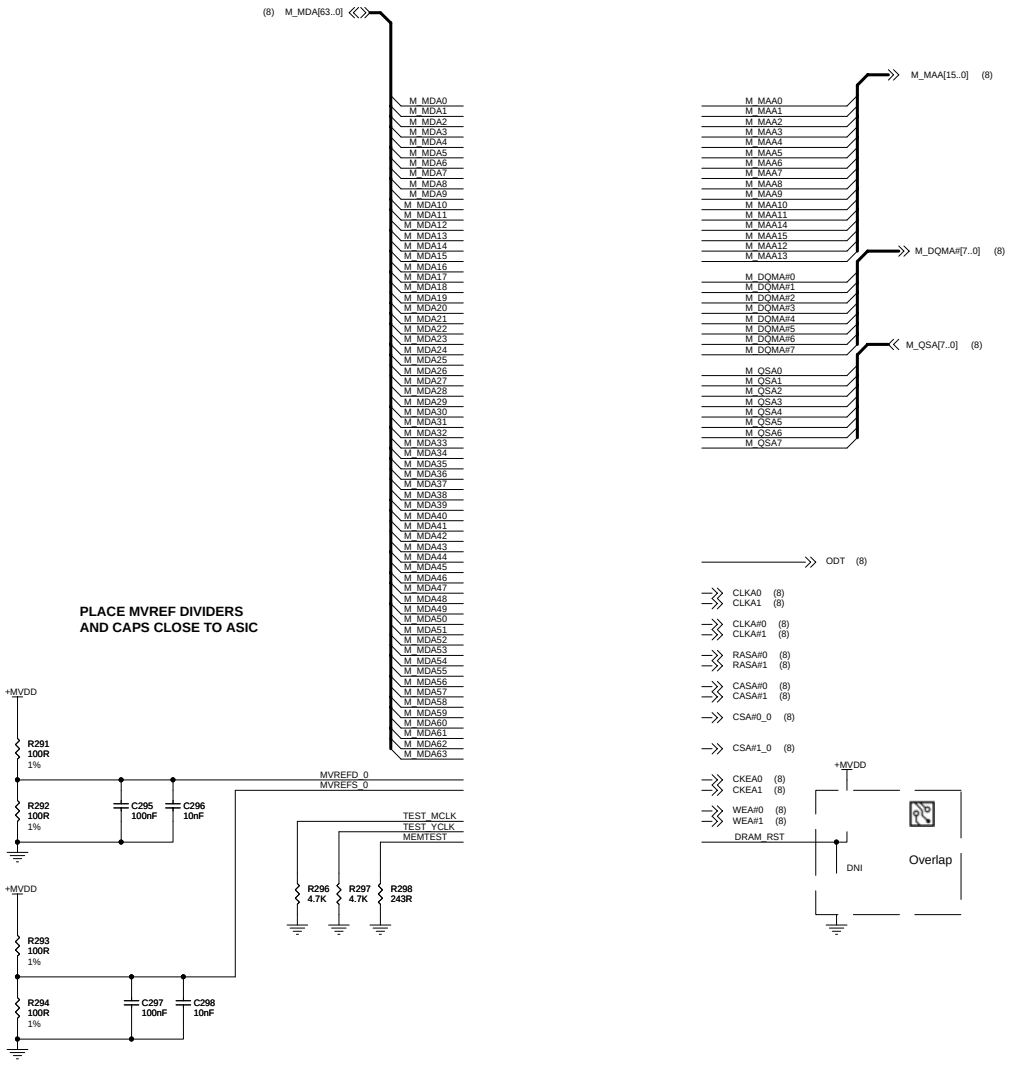

DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

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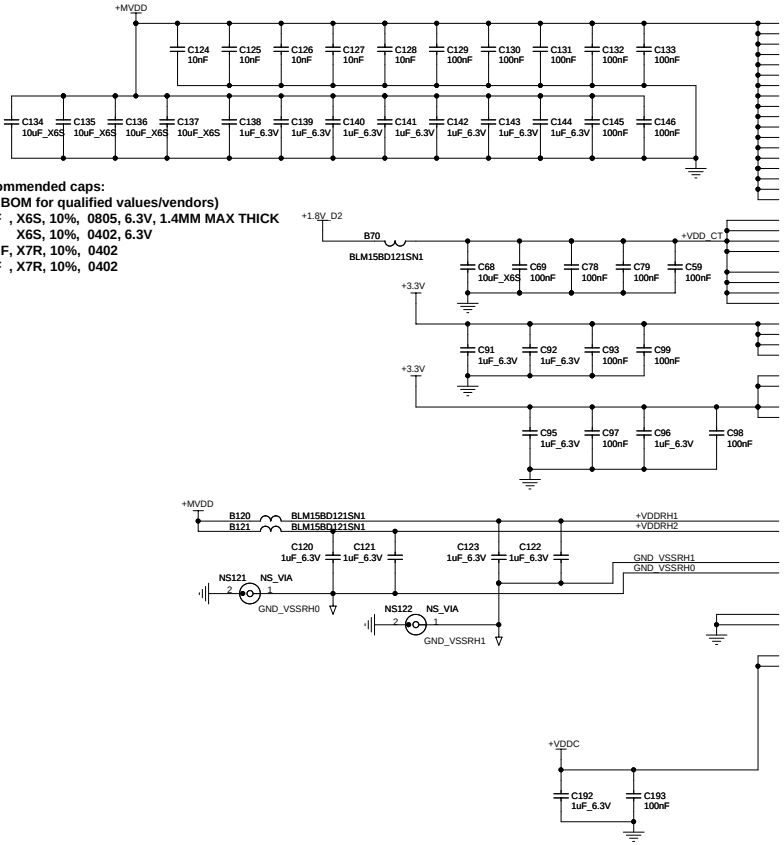

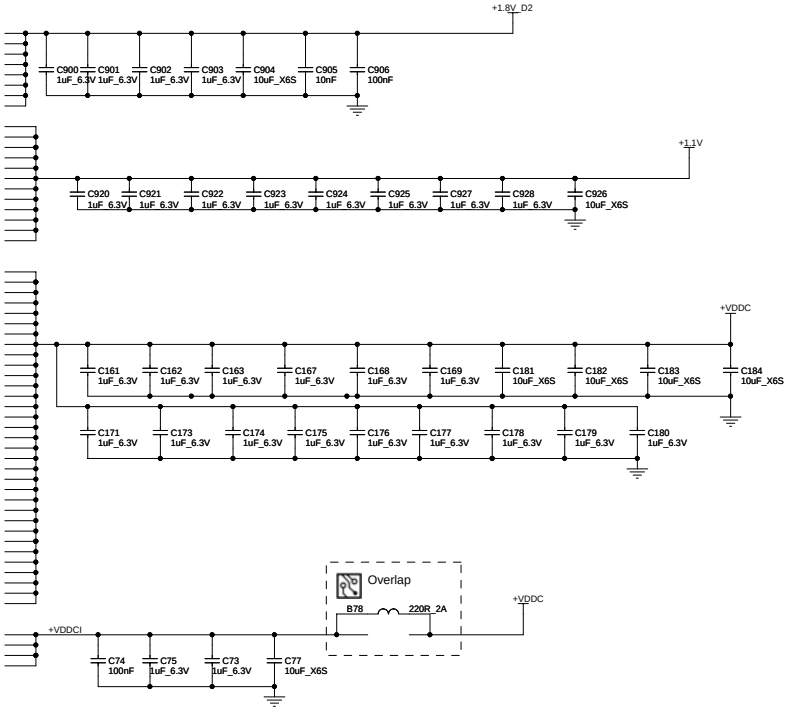

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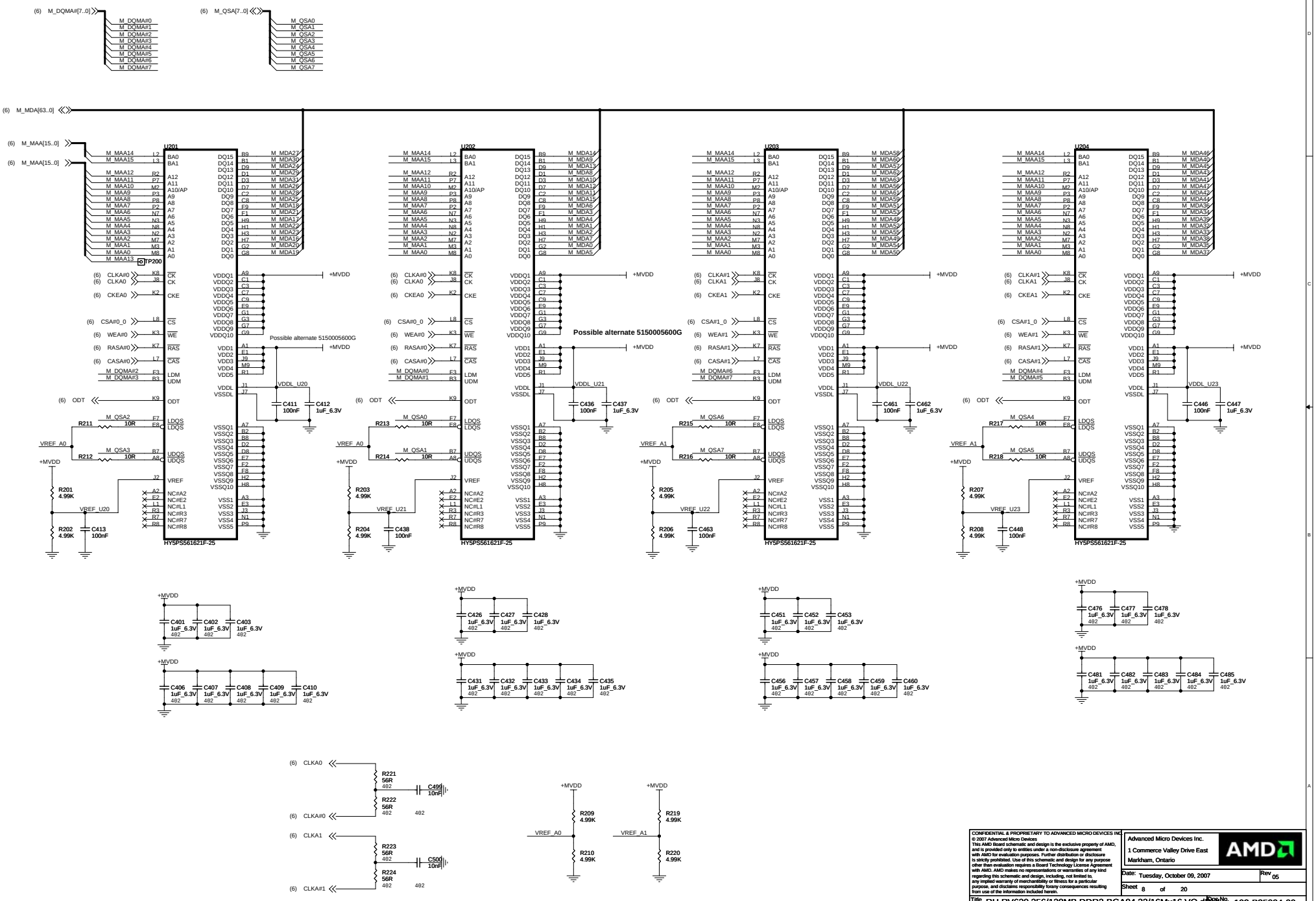
CHANNEL A: RANK 0 128MB DDR2



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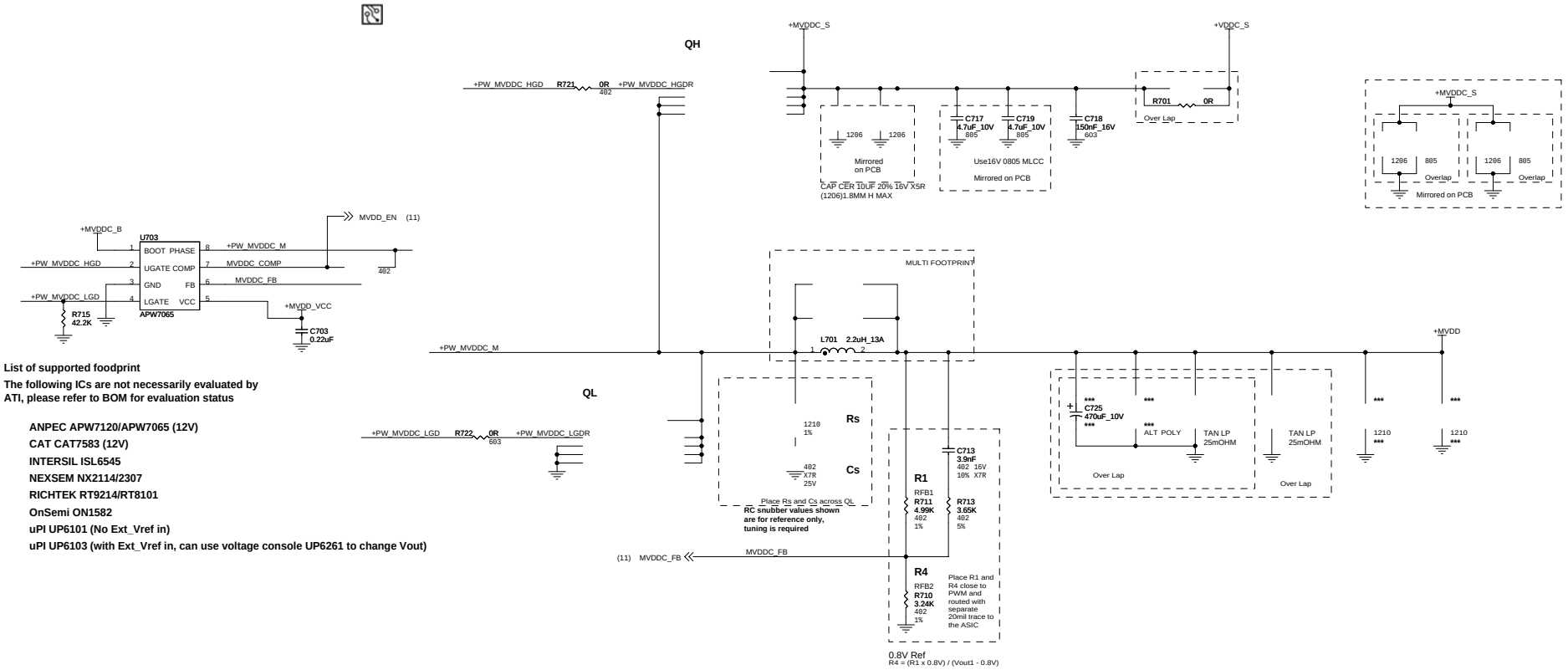
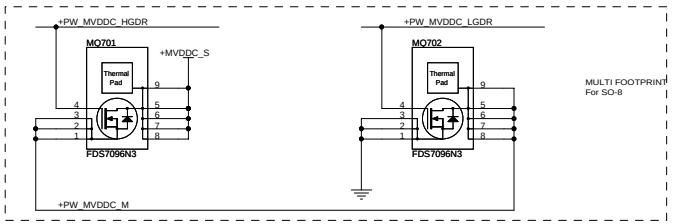


List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

- **ANPEC APW7120/APW7065 (12V)**
- **CAT CAT7583 (12V)**
- **INTERSIL ISL6545**
- **NEXSEM NX2114/2307**
- **RICHTEK RT9214/RT8101**
- **OnSemi ON1582**
- **uPI UP6101 (No Ext_Vref in)**
- **uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**



SMPS02- Regulator for MVDD

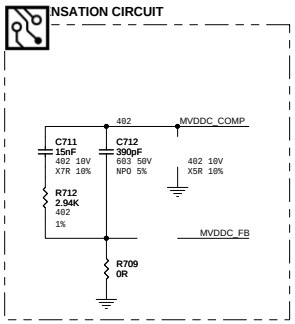
Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G
	1.8V (1.78V~1.86V)	4.99K p/n 3160499100G	3.92K p/n 3160392100G

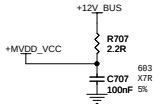
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

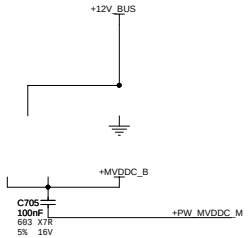
NSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



Layout guideline for Nexsem NX2114/2307

1- Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2- Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3- Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

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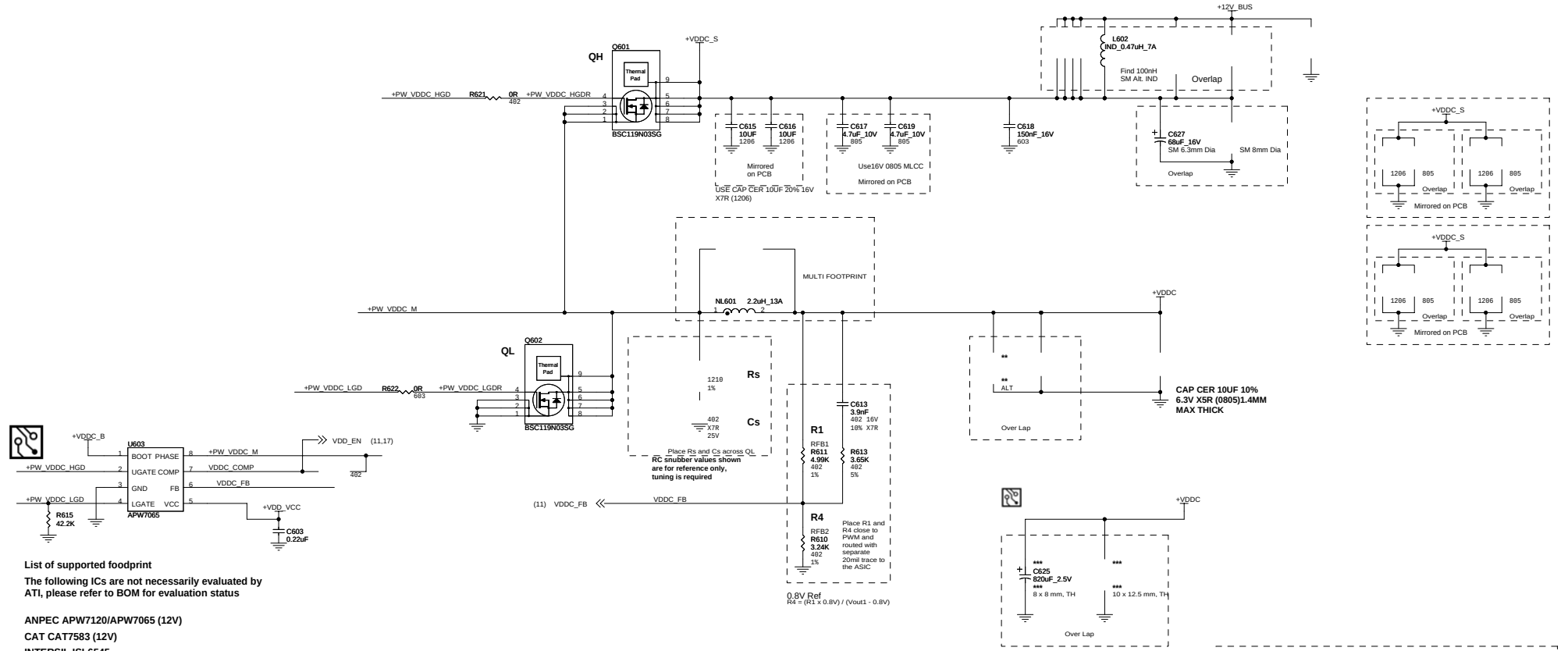

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ANPEC APW7120/APW7065 (12V)
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SMPS02- Regulator for VDDC

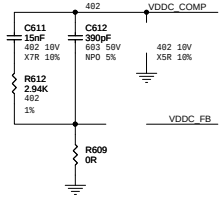
Vout = 0.9V ~ 1.1V

Part	Vout	RFB1	RFB2
0.8V Ref	1.1V (1.98V~2.08V)	200R p/n 3160200000G	511R p/n 3160511000G
	1.1V (1.10V~1.14V)	10K p/n 3160100200G	24.9K p/n 3160249200G

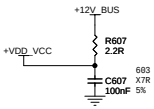
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

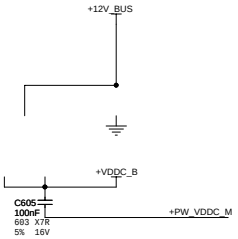
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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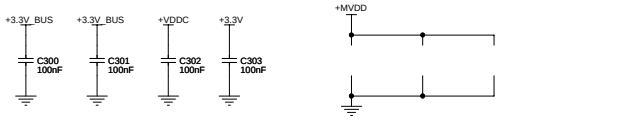
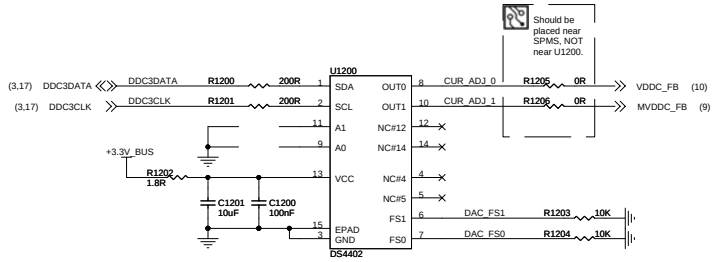
Stitching Capacitors

THESE ARE STITCHING CAPACITORS. THEIR PLACEMENT IS LAYOUT DEPENDANT.

Place C490-492 near layer transitions (top/bottom). THIS IS LAYOUT DEPENDENT.

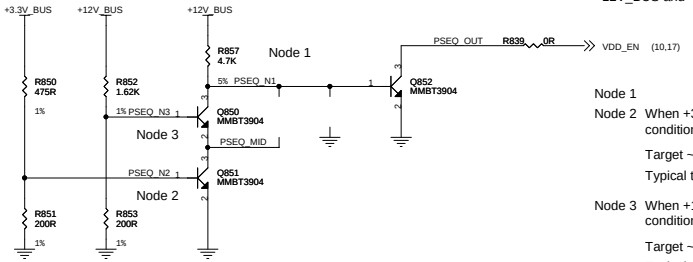


I2C control of VDDC/MVDD



Power up/down Sequencing

Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.



Node 1

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

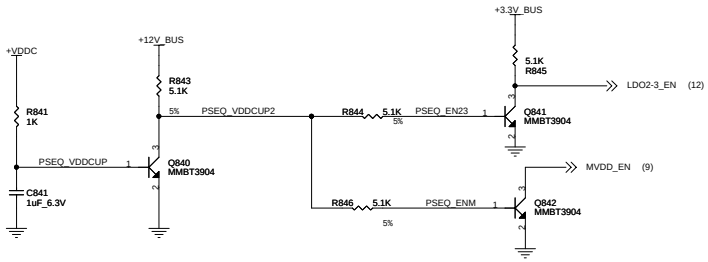
Typical trigger when +3.3V ramps above 2.2V (650mV)

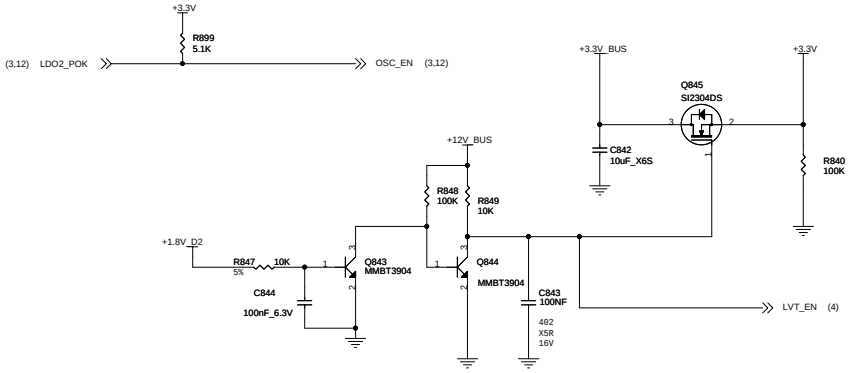
Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

When +12V_BUS ramps above min Vbe, SMPS_EN will be held low

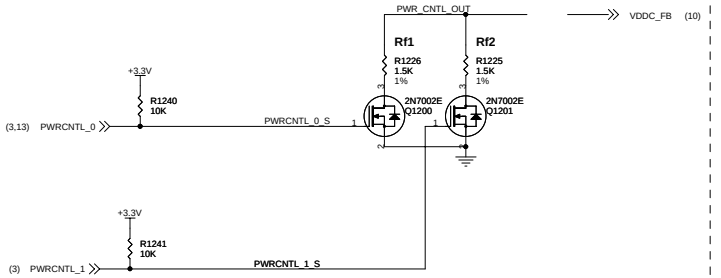




Power Play

VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0	0				
0	1				
1	0				
1	1	1 0	1		**Power-up Default**



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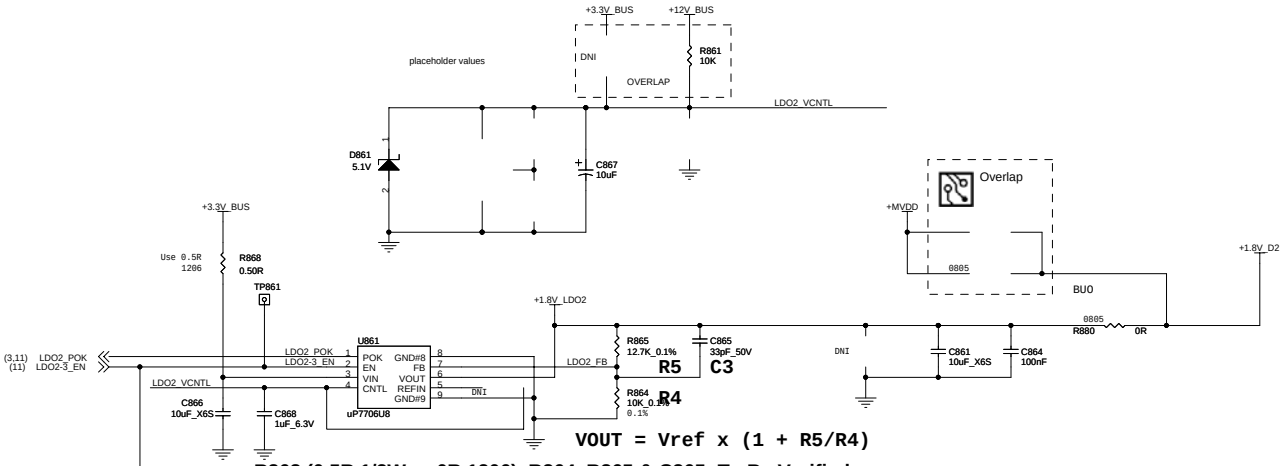
Doc No. 102-B35004-00

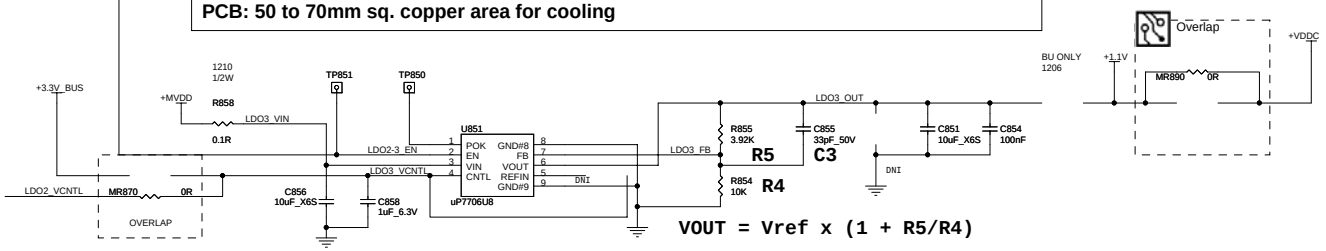
LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



VOUT = Vref x (1 + R5/R4)

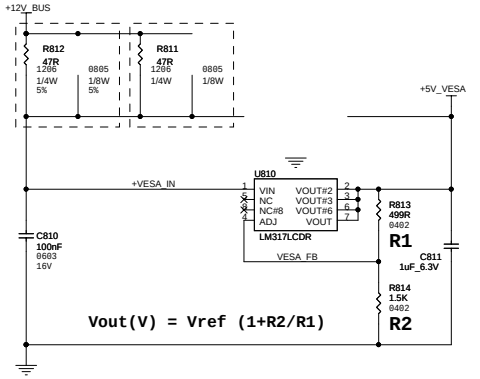
R868 (0.5R 1/2W or 0R 1206), R864, R865 & C865: To Be Verified

LDO #3: Vin = +1.4V to 2.087VMAX Vout = +1.1V +/- 2.5% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

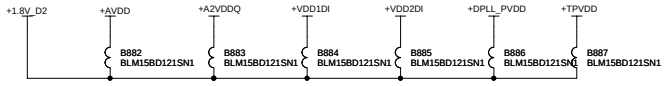


VOUT = Vref x (1 + R5/R4)

Regulators for +5V, +5V_VESA



Shared Power Rails



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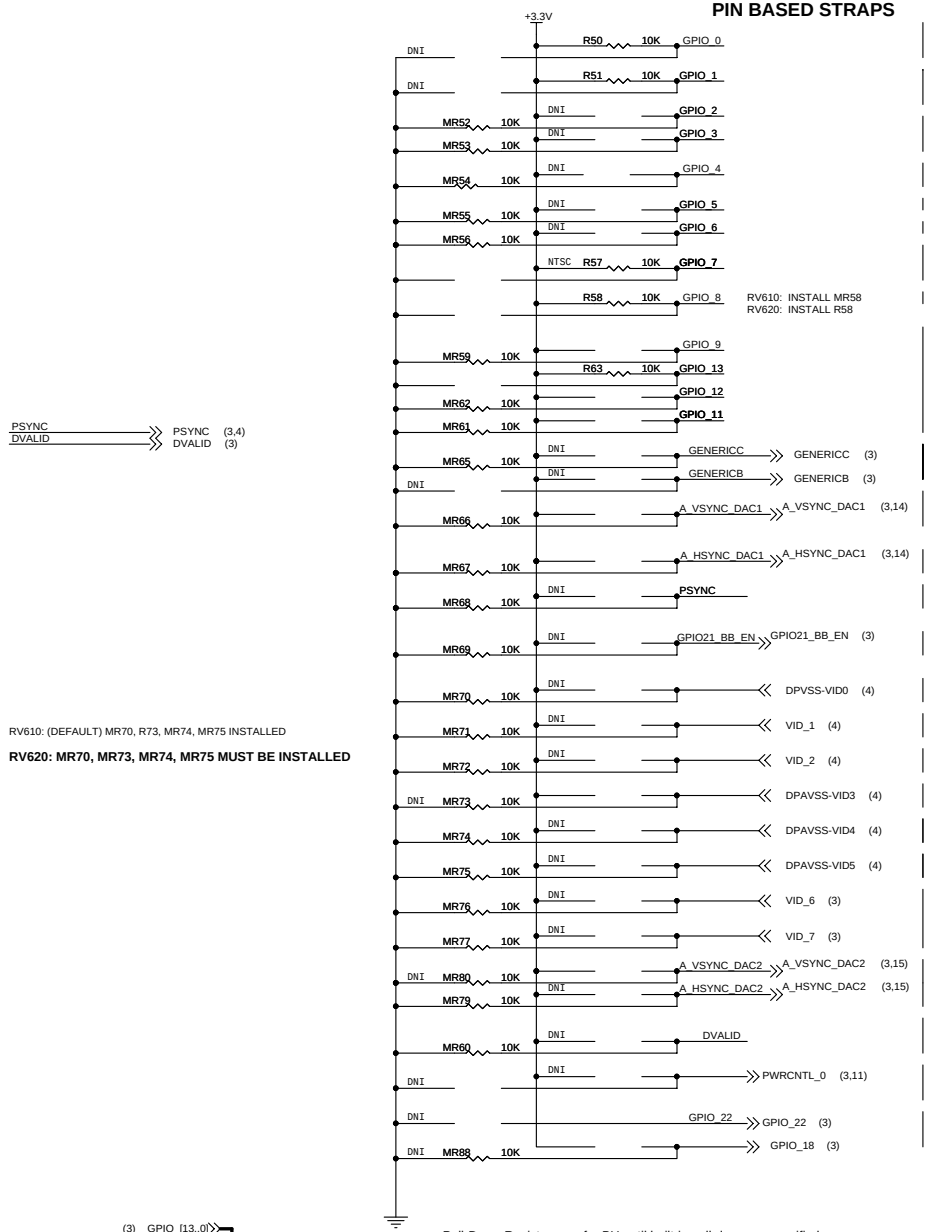
PIN BASED STRAPS



GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - ATI Internal Use Only - Reserved (Default: 00)

GPIO(4) - DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(7) - TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

RV610: INSTALL MR58
RV620: INSTALL R58

GPIO(8) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0] IF BIOS_ROM_EN=1 [default] (GPIO_22)

Atmel - AT25F512A (512 kbit) 0010
AT25F1024A (1 Mbit) 0011
ST Microelectronics - M25P05A (512 kbit) 0100
M25P10A (1 Mbit) 0101
M25P20 (2 Mbit) 0101
Chingis (formerly PMC) -
Pm25LV512 (512 kbit) 0100
Pm25LV010 (1 Mbit) 0101

If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. (Config 3 = don't care).

x000	128MB
x001	256MB
x010	64MB
x011	32MB
x100	512MB
x101	1GB
x110	2GB
x111	4GB

GENERICC, GENERICB - ATI Internal Use Only - Reserved (Default: 0)

VSYNC - VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - ATI Internal Use Only - Reserved (Default 0)

PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO_21 - ATI Internal Use Only - Reserved (Default: 0)

VID_0 - ATI Internal Use Only - Reserved (Default: 0)

VID_1 - MSI_DIS (Default: 0)

VID_2 - ATI Internal Use Only - Reserved (Default: 0)

VID_3 - ATI Internal Use Only - Reserved (Default: 0)

VID_4 - ATI Internal Use Only - Reserved (Default: 0)

VID_5 - 64BAR_EN_A (Default: 0)
Enable 64-bit BARS

VID_6:7 - ATI Internal Use Only - Reserved (Default: 00)

VSYNC - DDR2 VENDOR SELECT ATI Board Feature I
(see GPIO_18)

HSYNC2 - ATI Internal Use Only - Reserved (Default: 0)

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

GPIO_15 - FOR FUTURE EXPANSION

GPIO_22_ROMCSb - Enable external BIOS ROM device (Default 1)

GPIO_18 - DDR2 MEM VENDOR [V2SYNC:GPIO_18] ATI Board Feature I
QUIMONDA [0:0]
HYNIX [0:1]
SAMSUNG [1:0]

PSYNC (3,4)
DVALID (3)

RV610: (DEFAULT) MR70, R73, MR74, MR75 INSTALLED

RV620: MR70, MR73, MR74, MR75 MUST BE INSTALLED

(3) GPIO_[13..0]

GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground High logic voltage

Signal

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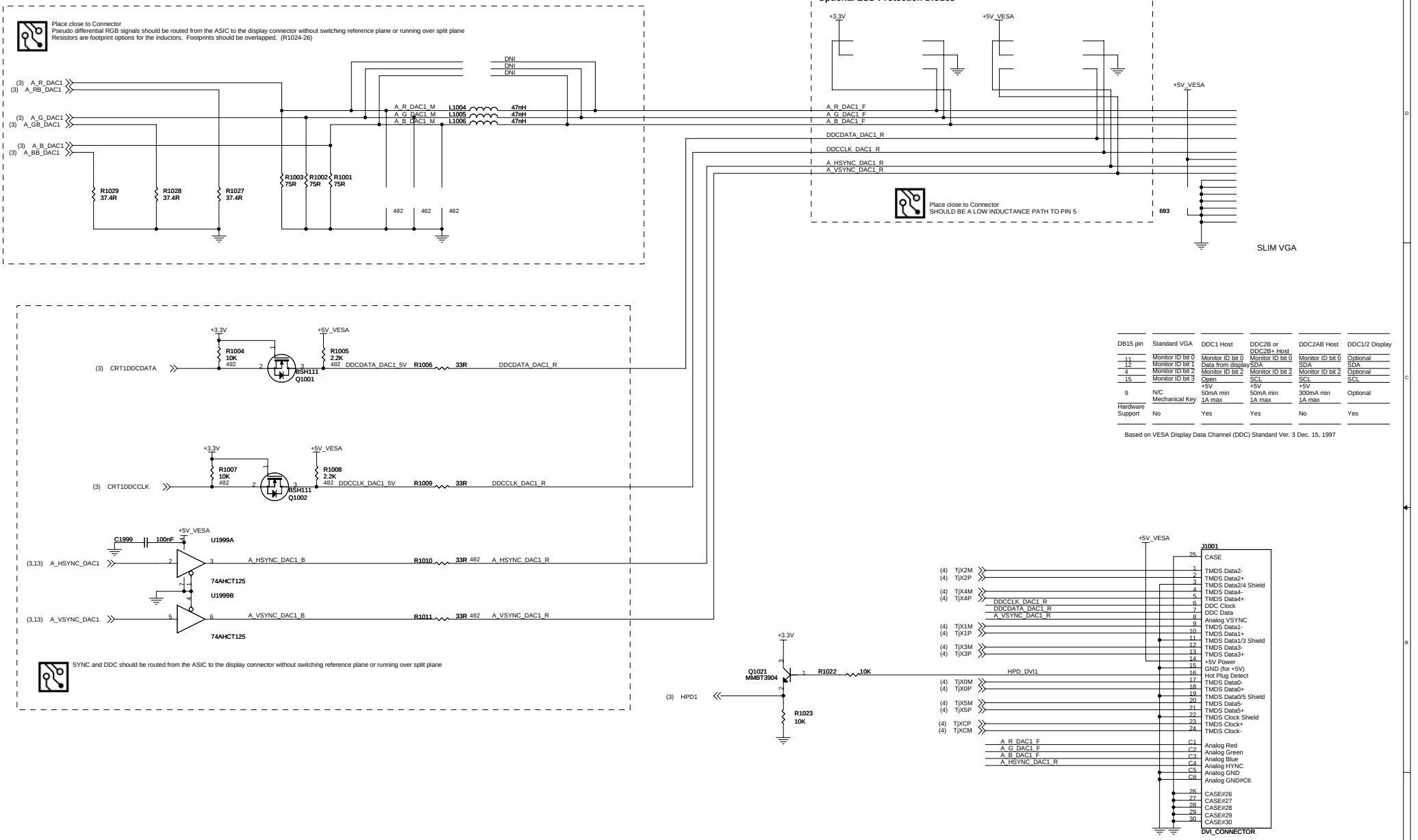

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

TMDS_2(Daul_Link) + DAC_1-CRT

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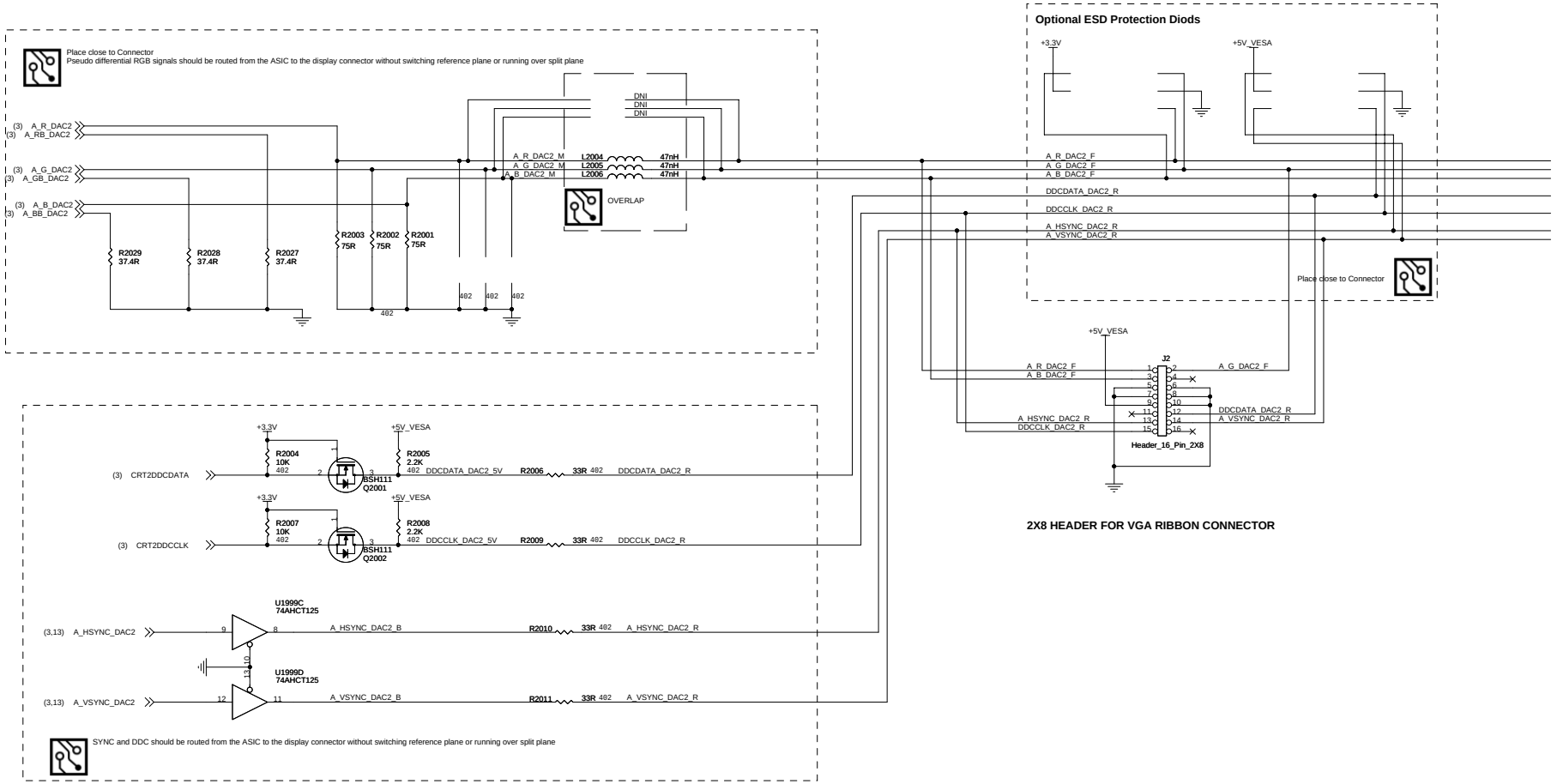

TMDS_1(Single_Link) + DAC_2-CRT

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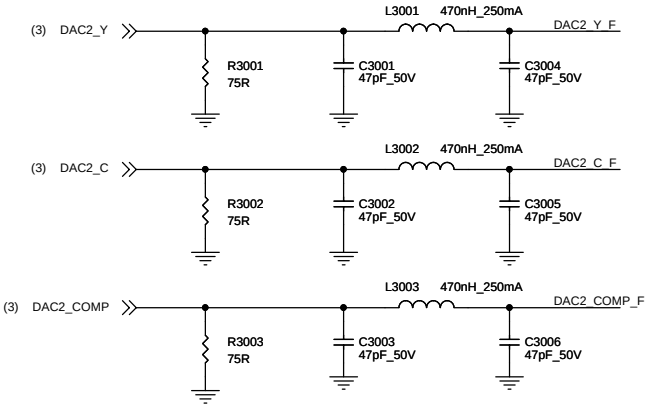

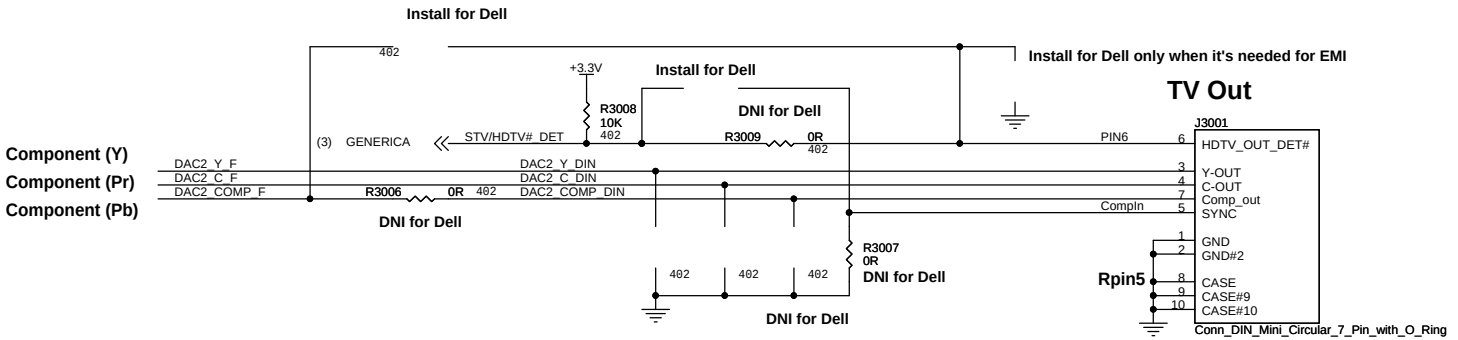

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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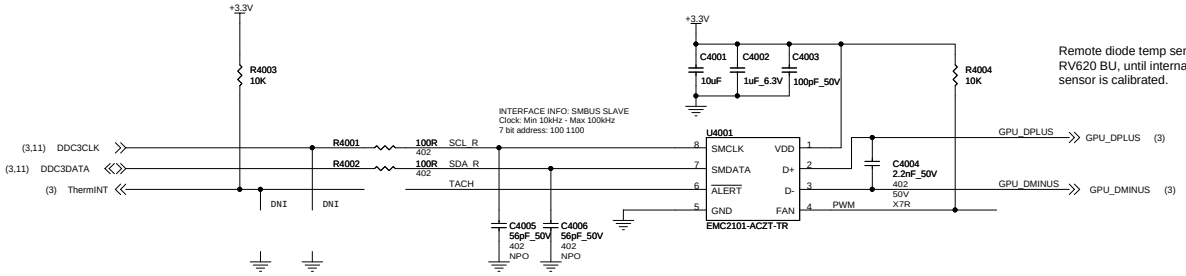
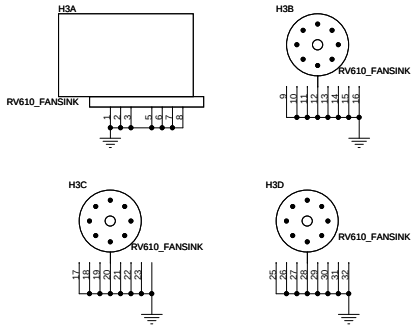
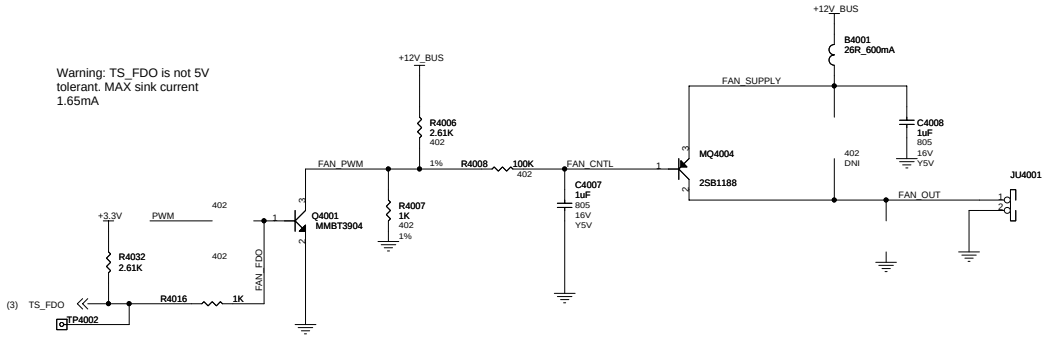


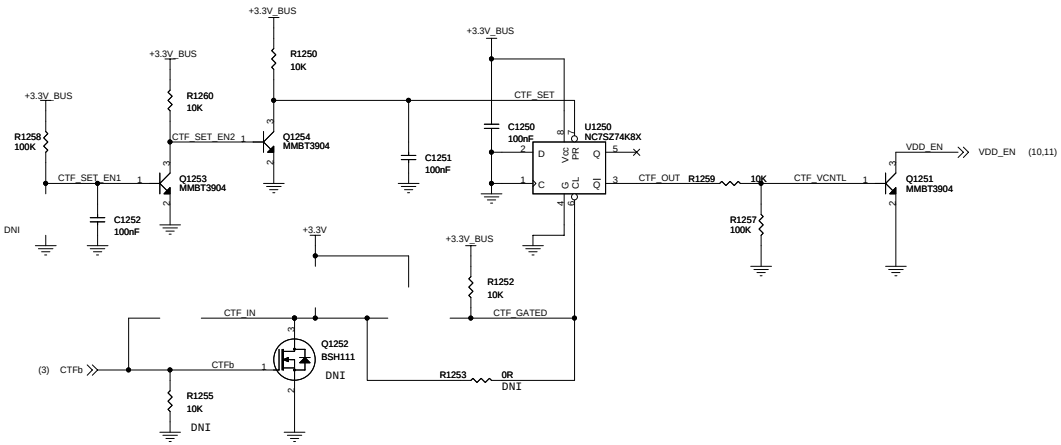
Remote diode temp sensor is for RV620 BU, until internal thermal sensor is calibrated.



Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA



Critial Temperature Fault



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DVI/VGA SCREWS

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

MT1
MT_Hole_0.136_in.
DNI

MT2
MT_Hole_0.136_in_6VIA
DNI

ASSY1
BRACKET
8020040100G

ASSY2
BRACKET
LP
8020040400G

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<variant Name>

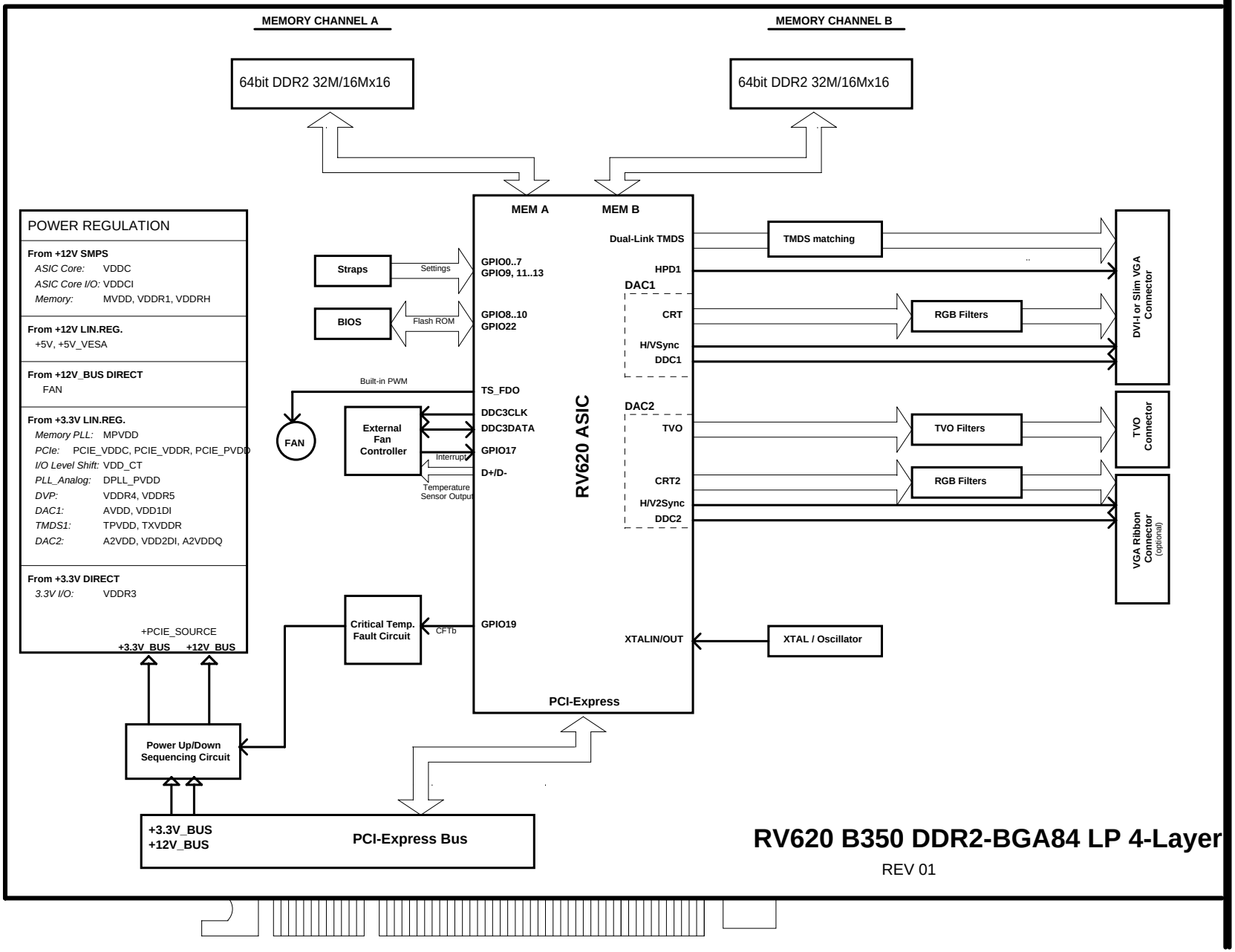
Title	Schematic No.	Date:
RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI	102-B35004-00	**Tuesday, October 09, 2007**

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 05

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
01	00A	2007.05.07	START NEW SCHEMATIC. DERIVED FROM B170 (RV610) SCHEMATIC.
02	00A	2007.05.17	p. 4 MR155/R155 FIX SHORT
03	00A	2007.05.17	RM R7, NR7, R5, MB60, MR45, R45, R890, R1248, R1247, R1242, R1243, C853, C863; ADD R2, B890, MR890, C846; CHANGE R1022, R1023;
04	00A	2007.05.22	REMOVE GND_TXVSSR, GND_PVSS; AG23 NOW NC - WAS SCHEM MISTAKE; ADD R858 FOR BUO; R858 CHANGE TO 1210;
05	00A	2007.05.24	CTF: ADD Q1252, R1254, R1255, R1256, R1258, Q1253, Q1254, CHANGE U1250 TO SINGLE FF; UPDATE BLOCK DIAGRAM.
06	00A	2007.05.25	LVTM: ADD R110, RM R109, MR109, R108, R107;
07	00A	2007.05.28	LVTM: ADD C118, RM C104; REMOVE MR85, MR86 FOR SIMPLIFICATION;
08	00A	2007.05.28	XTALIN/OUT: LAYOUT EASEMENT; REMOVE MR108 (R849 ALREADY THERE); LVTM: ADD C119 (LOWER COST OPTION); POWER SUPPLY: REMOVE R706, MR707, R606 & MR607;
09	00A	2007.05.29	REMOVAL OF +5V: ADD R861, MR861, R862, REG861, R869, R863, R867; REMOVE MU830, U830, C830. R833, R834, C831, R832, MR832, R831, MR831; CONNECT DDC TO 5V_VESA;
010	00A	2007.05.30	CHNG C858 TO 3.3VBUS; CONNECTION TO R845 CHNG; ADD R870, MR870, C867;
011	00A	2007.05.30	REMOVE R4033; REMOVE B201-204; ADD R30-33 [PLACE NEAR ASIC]; REMOVE R3004, R3005;
012	00A	2007.05.31	REMOVE C164-C166, C170, C172 PER SIMULATION RESULTS - THESE CAPS DO NOT IMPROVE DECOUPLING. RM TP860 (LAYOUT CONSTRAINTS. ALREADY ICT TP ON THAT NET);
013	00A	2007.05.31	RM R154-R157, MR154-157 -> FUNCTIONALITY TAKEN BY EXISTING STRAPS. LAYOUT USE PLACE OF M/R154-7; ADD R7; RM MR706, MR606, B889, R863; ADD D861;
014	00A	2007.05.32	ADD SOCKET SK1
015	00A	2007.06.1	SK? CORRECTED TO SK1.
016	00B	2007.06.25	NO NETLIST CHANGES; - MOUNTING HOLES CHANGED TO 3.175mm;



RV620 B350 DDR2-BGA84 LP 4-Layer

REV 01

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