電子類元件 零件承認書文件 **CHECK LIST**

零件廠商：AOS　　**品名規格：**DR MOS AOZ5066QI 60A AOS SMD QFN-40L

技嘉料號：10IFD-605066-01R

項次	文件項目
Data Sheet 檢核項目	
1	DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2**
8	零件樣品 20PCS(Chipset 等高單價，至少 1PCS)
9	**主動電子零件承認基本調查表。註 3**
10	以上資料電子檔為 PDF 檔，且是同 1 個 File
GPMS 綠色產品管理系統-物料管制文件檢核清單	
物料管制文件 1	GPMS 綠色產品管理系統：零件照片
物料管制文件 2	GPMS 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4**
物料管制文件 3	GPMS 綠色產品管理系統：Data Sheet
GPMS 綠色產品管理系統-MCD 表格	
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
其他文件 (僅適用電阻、電容類之系列元件)	
附件 1	危害物質測試報告 Test Report of Hazardous Substances。**註 5**
附件 2	元件調查表 Component Composition Table

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等
※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)
※ **3. 主動電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G***
※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”
※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

主動電子零件承認基本調查表

一、原物料規格/來源

項次	部位名稱/規格	材質	原物料來源產地
1	BONDING WIRE	Au	SINGAPORE
2	CHIP	Silicon	CHINA
3	DIE ATTACH	ADHESIVE	USA
4	LEAD-FINISHED	Sn	CHINA
5	LEADFRAME	Cu Alloy	TAIWAN
6	MOLD COMPOUND	Plastic	CHINA

二、晶圓廠

項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	Intersil	Japan	8		外包
2	J-fab	USA	8		自有

三、封裝廠

項次	工廠名稱	生產產地	投產比率(%)	自有/外包
1	APM	Shanghai		自有
2				
3				

四、產能

總產能(月/PCS)	可供技嘉產能(月/PCS)
1440K	

※ 1. 晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動) 時，請主動通知技嘉研發管理與 CE 單位，並更新文件

※ 2. 以上資訊欄位若有不足，可自行增加行數

AOZ5066

60A DrMOS Power Module

General Description

The AOZ5066 is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The high side MOSFET has low capacitance and gate charge for fast switching with low duty cycle operation. The low side MOSFET has ultra low $R_{DS(ON)}$ to minimize conduction losses.

The AOZ5066 is available with two PWM options. AOZ5066QI is intended for use with TTL compatible PWM inputs. AOZ5066QI-01 has lower thresholds on the PWM signal and can operate with 3V inputs. All other parameters are identical for the two versions. Both versions are tri-state compatible that allows both power MOSFETs to be turned off.

A number of features are provided making the AOZ5066 a highly versatile power module. The boot supply diode is integrated in the driver. The low side MOSFET can be driven into diode emulation mode to provide asynchronous operation when required. The pinout is optimized for low inductance routing of the converter keeping the parasitics and their effects to the minimum.

Features

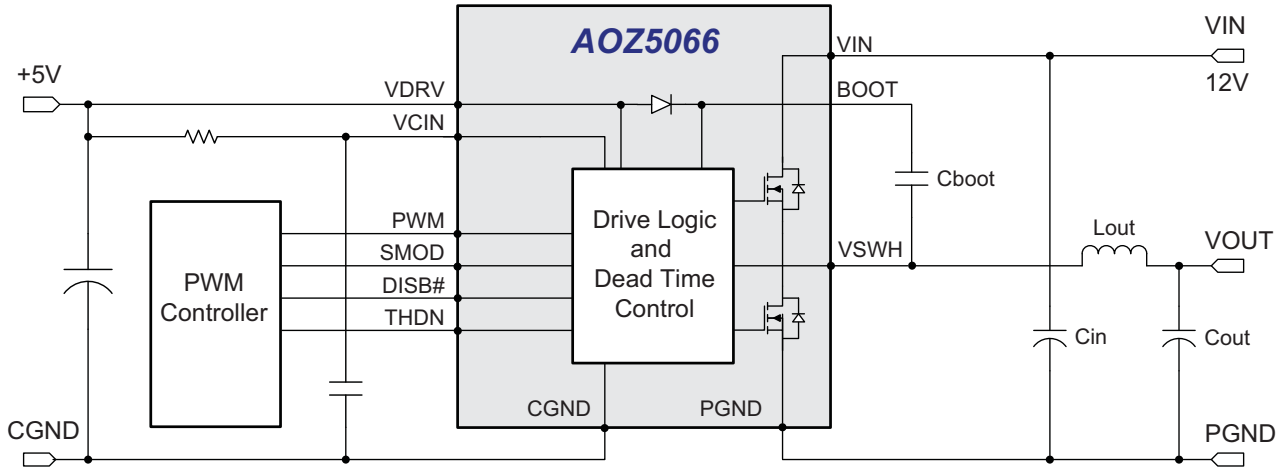
- Fully complies with Intel DrMOS Rev 4.0 specifications
- 4.5V to 25V input voltage range
- 4.5V to 5.5V driver supply range
- Up to 60A output current
- Up to 1MHz PWM operation
- Tri state PWM input
- Undervoltage protection
- Integrated boot supply diode
- Diode Emulation mode of operation
- Thermal shutdown alarm with flag
- Small 6x6 QFN-40L package

Applications

- Servers
- VRMs for motherboards
- Point of load DC/DC converters
- Memory and graphic cards
- Video gaming consoles

Green Product

Typical Application Circuit

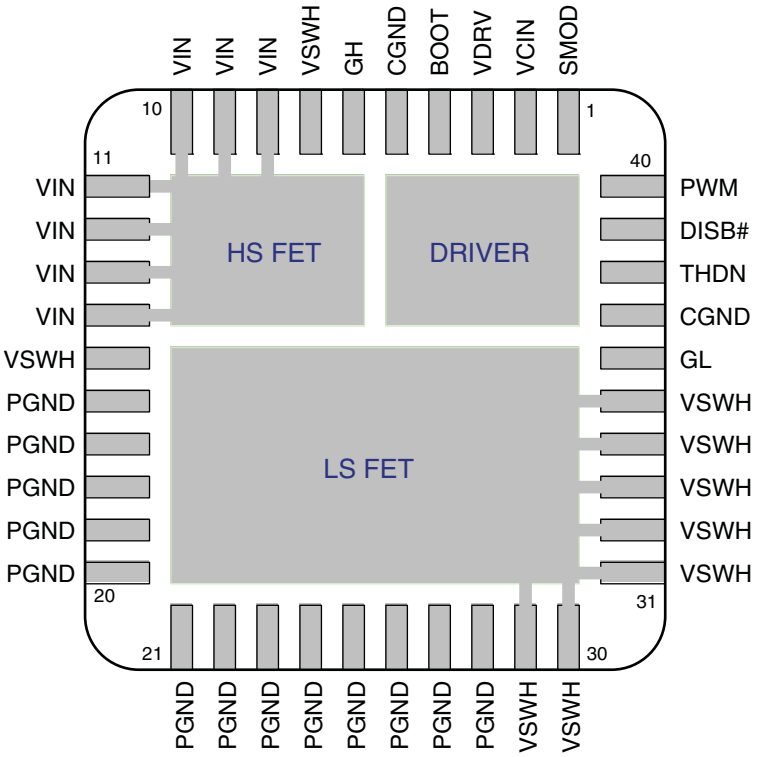


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5066QI	-40°C to +85°C	6x6 QFN-40L	Green Product
AOZ5066QI-01			

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

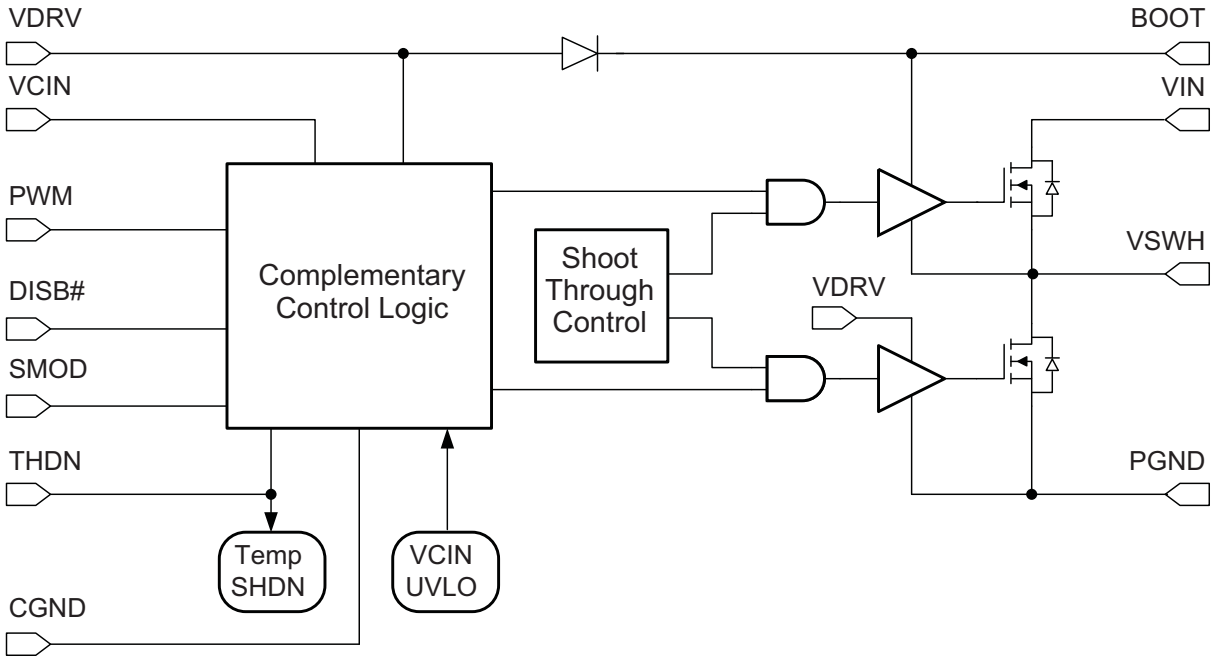


6x6 QFN-40
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	SMOD	Skip Mode input. When the pin is held active low, Diode Emulation or Skip Mode is enabled for the LS FET.
2	VCIN	Control supply input. Nominal 5V. Can be derived from the gate drive supply VDRV with an RC filter for noise bypass.
3	VDRV	Gate drive supply input. Nominal 5V.
4	BOOT	Gate drive supply for the HS FET. Nominal 5V. The bootstrap diode is internal to the module. Connect a 0.1µF or higher ceramic capacitor between VSWH node at pin 7.
5, 37	CGND	Control or analog ground for return of control signals and bypass capacitors. Attached to exposed pad in the driver section.
6	GH	Gate of the HS FET. Used for module testing during production. No user connections.
7	VSWH	Switching or the phase node for bootstrap capacitor connection.
8 to 14	VIN	Power input to the switching MOSFETs. Attached to the HS FET drain tab.
15	VSWH	Switching or the phase node pin. Not for power connections.
16 to 28	PGND	Power ground. Internally connected to control GND of pin 37.
29 to 35	VSWH	Switching or phase node connected to source of high side MOSFET and drain of the low side MOSFET. Electrically attached to the LS FET drain tab.
36	GL	Gate of the LS FET. Used for module testing during production. No user connections.
38	THDN	Open drain output of the thermal shutdown circuit. Active low.
39	DISB#	Disable pin for the controller. Both gates are held active low when DISB# is grounded.
40	PWM	Pulse Width Modulated Tri State input from external controller.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (VIN)	-0.3V to 30V
Switch Node Voltage (VSWH) (1)	-8V to 30V
Bootstrap Voltage (VBOOT)	-0.3V to 30V
VBOOT Voltage Transient (1)	36V
Supply and Gate Drive Voltages {VCIN, VDRV, (VBOOT – VSWH)}	-0.3V to 7V
Control Inputs (PWM, SMOD, DISB#)	-0.3V to VCIN+0.3 V
Storage Temperature (T_S)	-65°C to +150°C
Junction Temperature (T_J)	+150°C
ESD Rating(2)	2kV

Notes:

1. Peak voltages can be applied for 100nS per switching cycle.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (VIN)	4.5V to 25V
Supply and Gate Drive Voltages {VCIN, VDRV, (VBOOT – VSWH)}	4.5V to 5.5V
Control Inputs (PWM, SMOD, DISB#)	0V to VCIN – 0.3V
Operating Frequency	200kHz to 1MHz

Electrical Characteristics(3)

T_A = 25°C, V_{IN} = 12V, VDRV = VCIN = 5V unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIN	Operating Voltage		4.5		25	V
VCIN		VDRV Tied to VCIN	4.5		5.5	V
$R_{\theta JC}$(4)	Thermal Resistance	PCB Temp = 100°C		5.0		°C / W
$R_{\theta JA}$ (4)				50		°C / W
INPUT SUPPLY AND UVLO						
V_{CINON}	Undervoltage Lockout	V_{CIN} Rising		3.5	3.9	V
$V_{CINHYST}$		V_{CIN} Falling		550		mV
I_{VCIN}	Control Circuit Bias Current	DISB# = 0, VCIN = 5V		50	75	µA
		DISB# = High, V_{PWM} = Open		350	500	µA
		DISB# = High, V_{PWM} = 0V		650		µA
I_{VDRV}	Drive Circuit Operating Current	DISB# = High, V_{PWM} = 300kHz @ 50%		46		mA
		DISB# = High, V_{PWM} = 1MHz @ 50%		152		mA
PWM INPUT (AOZ5066QI)						
V_{PWMH}	PWM Input High Threshold	V_{PWM} Rising, VCIN = 5V	3.6	3.9	4.1	V
V_{PWML}	PWM Input Low Threshold	V_{PWM} Falling, VCIN = 5V	0.8	1.0	1.2	V
I_{PWM}	PWM Pin Input Current	Source or Sink, V_{PWM} = 0V to 5V		±250		µA
V_{TRIH}	PWM Input Tri State Threshold	V_{PWM} Rising, VCIN = 5V	1.0	1.3	1.6	V
V_{TRIL}		V_{PWM} Falling, VCIN = 5V	3.4	3.7	4.0	V
V_{TRRH}	Tri State Threshold Hysteresis	V_{PWM} Rising, VCIN = 5V		280		mV
V_{TRFH}		V_{PWM} Falling, VCIN = 5V		170		mV

Electrical Characteristics[3] (Continued)

T_A = 25°C, V_{IN} = 12V, VDRV = VCIN = 5V unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PWM INPUT (AOZ5066QI-01)						
V_{PWMH}	PWM Input High Threshold	V_{PWM} Rising, VCIN = 5V	1.8	2.0	2.2	V
V_{PWML}	PWM Input Low Threshold	V_{PWM} Falling, VCIN = 5V	0.8	1.0	1.2	V
I_{PWM}	PWM Pin Input Current	Source or Sink, V_{PWM} = 0V to 3V		±10		µA
V_{TRIH}	PWM Input Tri State Threshold	V_{PWM} Rising, VCIN = 5V	1.15	1.3	1.45	V
V_{TRIL}		V_{PWM} Falling, VCIN = 5V	1.65	1.75	1.9	V
V_{TRRH}	Tri State Threshold Hysteresis	V_{PWM} Rising, VCIN = 5V		300		mV
V_{TRFH}		V_{PWM} Falling, VCIN = 5V		300		mV
DISB# INPUT						
V_{DISBON}	Outputs Enable Threshold	VCIN = 5V	2.0			V
$V_{DISBOFF}$	Outputs Disable Threshold	VCIN = 5V			0.8	V
I_{DISB}	DISB# pin input current	Source or Sink		±10		µA
SMOD INPUT						
V_{SMODH}	SMOD Enable Threshold	VCIN = 5V	2.0			V
V_{SMODL}	SMOD Disable Threshold	VCIN = 5V			0.8	V
I_{SMOD}	SMOD Pin Input Current	Source or Sink		±10		µA
GATE DRIVER TIMINGS						
t_{PDLU}	PWM to HS Gate	PWM H → L, GH H → L		20		ns
t_{PDLL}	PWM to LS Gate	PWM L → H, GL H → L		35		ns
t_{PDHU}	LS to HS Gate Deadtime	GL H → L, GH L → H		16		ns
t_{PDHL}	HS to LS Gate Deadtime	GH H → L, GL L → H		17		ns
t_{TSSHD}	Tri State Shutdown Delay			170		ns
t_{PTS}	Tri State Propagation Delay			35		ns
THERMAL SHUTDOWN[5]						
T_{JTHDN}	Shutdown Threshold			150		°C
T_{JHYST}	Hysteresis			15		°C
V_{THDNL}	THDN Pin Output Low	5kΩ pull up resistor to VCIN		0.06		V
R_{THDNL}	THDN Pull Down Resistance			60		Ω

Notes:

3. All voltages are specified with respect to the corresponding GND pin
4. Characterisation value. Not tested in production.
5. Temperature sensed on the driver pad

Typical Performance Characteristics

Unless otherwise noted, VIN = 12V, VDRV = VCIN = 5V, F_{sw} = 670kHz, L_{out} = 470nH, V_{out} = 1.2V.
Loss and efficiency measured on AOS evaluation board at T_A = 25°C. No forced air for module loss < 7W.
Module loss includes power MOSFET loss plus drive circuit loss.
Power train consists of AOZ5066 power module plus output inductor IHLP6767GZERR47M01.
Power train efficiency does not include other losses in the test board.

Fig 1. Module Loss vs. Load Current

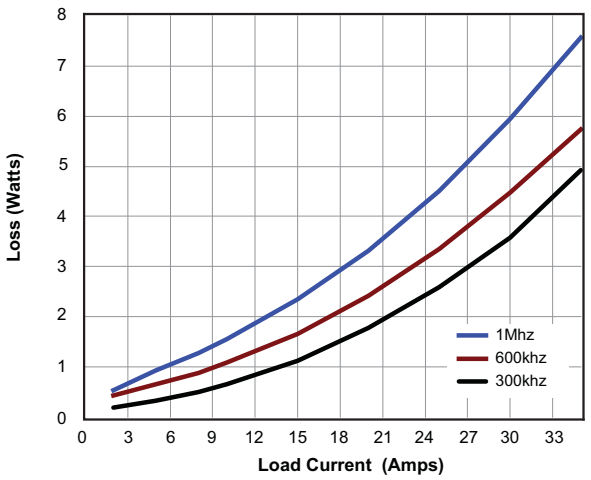


Fig 2. Power Train Efficiency vs. Load Current

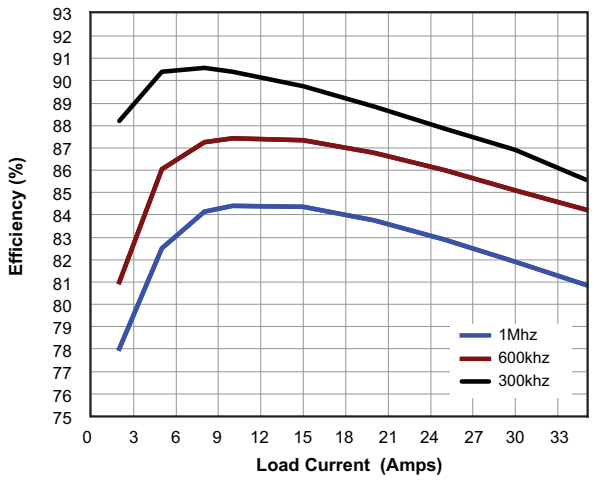


Fig 3. Normalised Module Loss and Power Train Efficiency vs. Drive Voltage

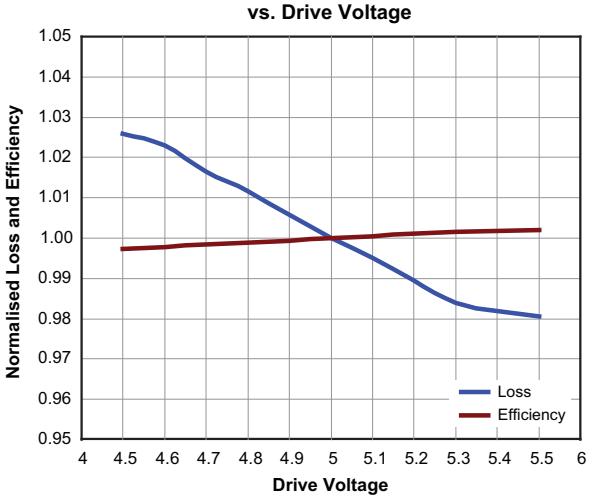
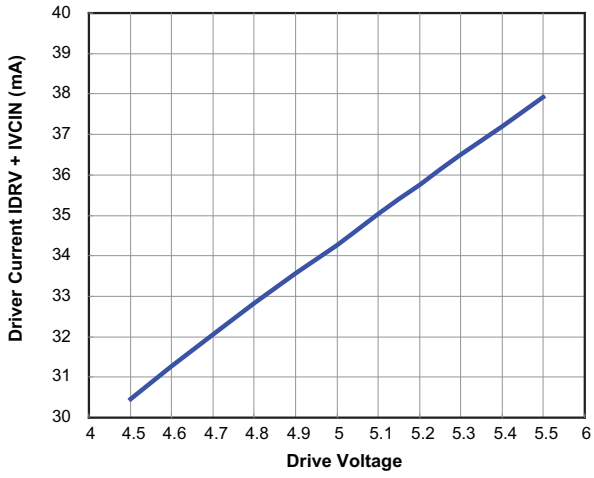


Fig 4. I_{DRV} + I_{VCIN} vs. Drive Voltage



Typical Performance Characteristics (Continued)

Fig 3. Normalised Module Loss and Power Train Efficiency vs. Drive Voltage

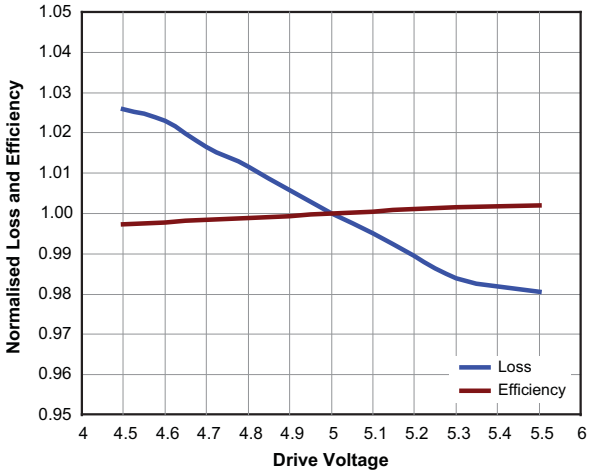


Fig 4. I_{DRV} + I_{VCIN} vs. Drive Voltage

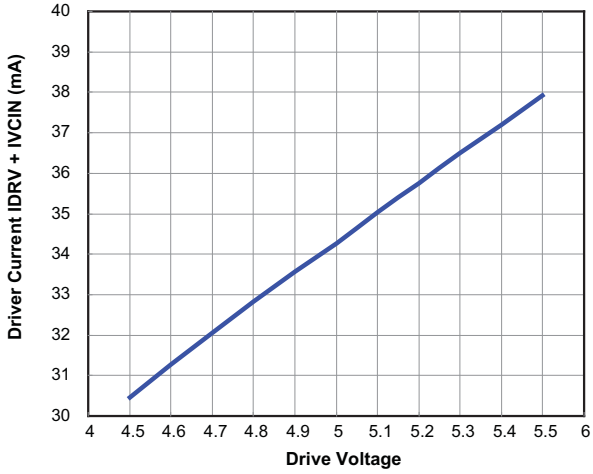


Fig 5. Normalised I_{DRV} + I_{VCIN} vs. Operating Frequency

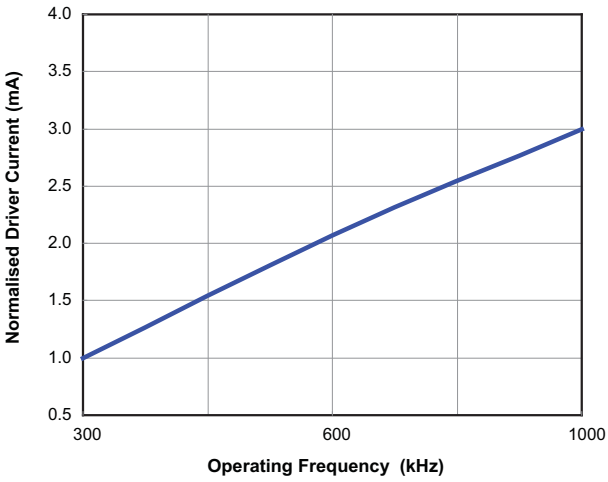


Fig 6. I_{DRV} + I_{VCIN} vs. Temperature

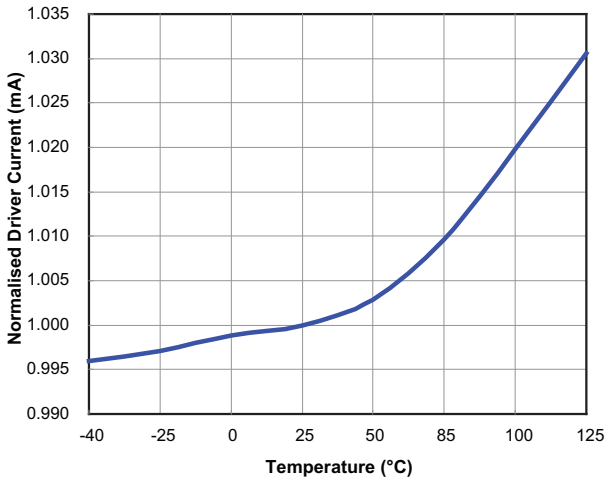


Fig 7. VDRV UVLO Threshold vs. Temperature

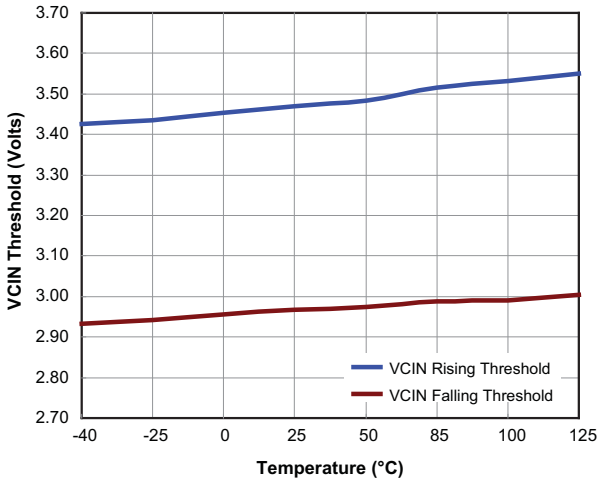
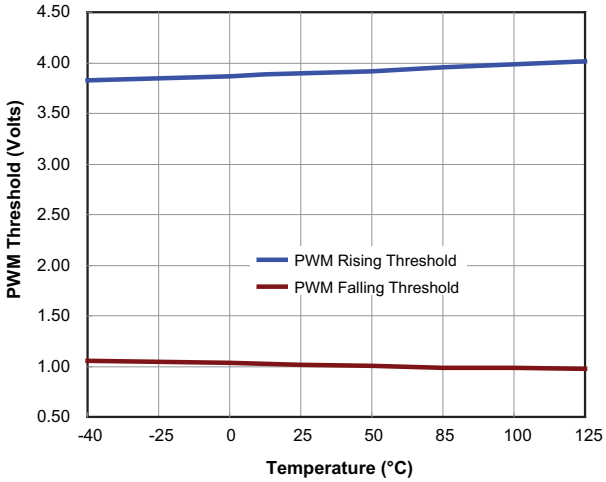


Fig 8. PWM Input Threshold vs. Temperature



Typical Performance Characteristics (Continued)

Fig 11. DISB# Input Threshold vs. Temperature

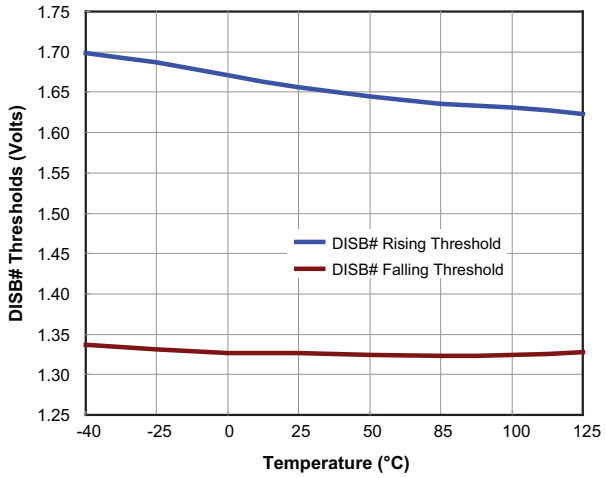
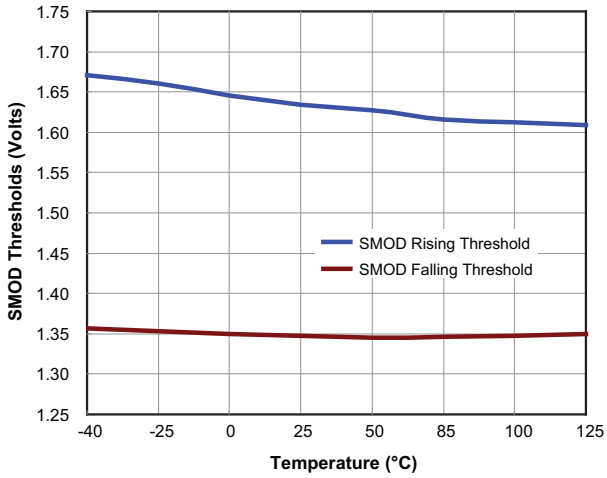


Fig 12. SMOD Input Threshold vs. Temperature



Timing Diagram

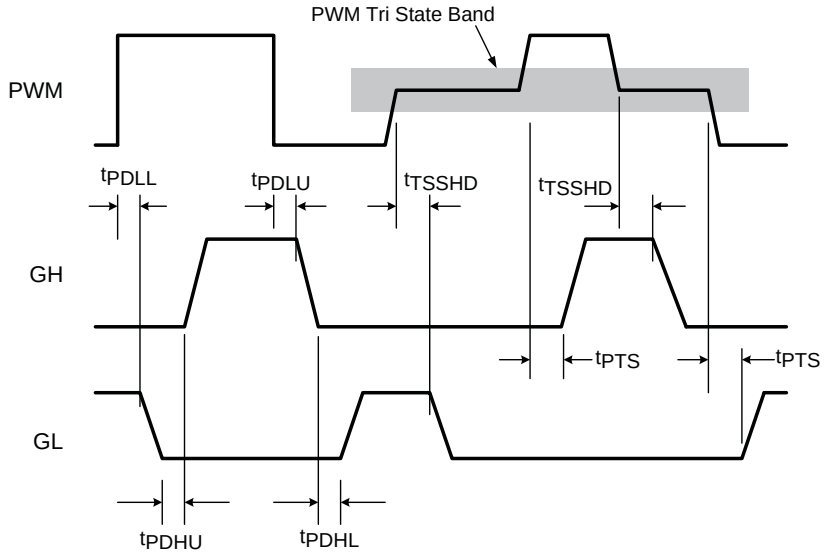


Figure 13. Timing Diagram

Application Information

AOZ5066QI and AOZ5066QI-01 are fully integrated power modules designed to work over an input voltage range of 4.5V to 25V with 5V supplies for gate drive and internal control circuits. A number of features are provided making the AOZ5066QI a highly versatile power module. High side and low side power MOSFETs are combined in one package with the pin outs optimized for power routing with minimum parasitic inductances. The MOSFETs are individually tailored for efficient operation as either high side or low side switches in a low duty cycle synchronous buck converter. A high current driver is also included in the package which minimizes the gate drive loop and results in extremely fast switching. The modules are fully compatible with Intel DrMOS specification Rev 4.0 in form fit and function.

Powering the Module and the Gate Drives

An external supply VDRV of 5V is required for driving the MOSFETs. The MOSFETs are designed with low gate thresholds so that lower drive voltage can be used to reduce the switching and drive losses without compromising the conduction losses. The control logic supply VCIN can be derived from the gate drive supply VDRV through an RC filter to bypass the switching noise. See Figure 14 for recommended gate drive supply connections. The gate driver is capable of supplying several amperes of peak current into the LS FET to achieve extremely fast switching. A ceramic bypass capacitor of 1μF or higher is recommended from VDRV to CGND.

The boost supply for driving the high side MOSFET is generated by connecting a small capacitor between BOOT pin and the switching node VSWH. It is recommended that this capacitor Cboot be connected as close as possible to the device across pins 4 and 7. Boost diode is integrated into the package. Rboot is an optional resistor used by designers to slow down the turn on speed of the high side MOSFET. The value is a compromise between the need to keep both the switching time and VSWH node spikes as low as possible and is typically 1Ω to 5Ω.

Undervoltage Lockout and Enable

VCIN is monitored for UVLO conditions and both outputs are actively held low unless adequate gate supply is available. The undervoltage lockout is set at 3.5V with a 550mV hysteresis. Since the PWM control signals are provided typically from an external controller or a digital processor extra care must be taken during start up. The AOZ5066QI must be powered up and enabled before the PWM input is applied. It should be ensured that PWM signal goes through a proper soft start sequence to minimise inrush current in the converter during start up. Powering the module with a full duty cycle PWM signal already applied may lead to a number of undesirable consequences as explained below.

Outputs can also be turned off through the DISB# pin. When this input is grounded the drivers are disabled and held active low. The module is in standby mode with low quiescent current of less than 75μA.

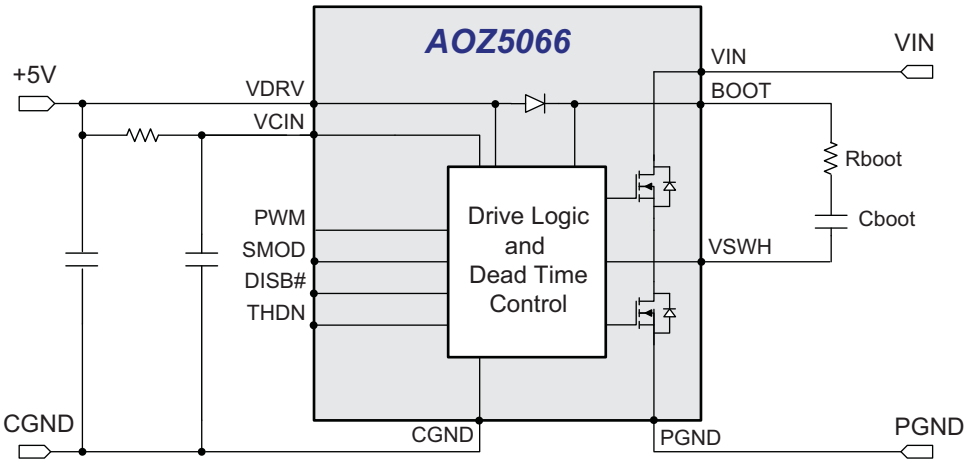


Figure 14. Applying VDRV and Generating BOOT Supply

IMPORTANT: If the DISB# is used it is necessary to ensure proper coordination with soft start and enable features of the external PWM controller in the system. Every time AOZ5066QI is disabled through DISB# there will be no output and the external controller may enter into open loop and put out a PWM signal with maximum duty ratio possible. If the AOZ5066QI is re-enabled by taking DSBL# high, there will be extremely large inrush currents while the output voltage builds up again which may drive the system into current limit. There might be undesirable consequences such as inductor saturation, overloading of the input or even a catastrophic failure of the device. It is recommended that the PWM controller be disabled when AOZ5066QI is disabled or non operational because of UVLO. The PWM controller should always be enabled with a soft start to minimise stresses on the converter.

In general it should be noted that AOZ5066QI is a combination of two MOSFETs with an unintelligent driver, all of which are optimized for switching at the highest efficiency. Other than UVLO and thermal protection, it does not have any monitoring or protection functions built in. The PWM controller should be designed in to perform these functions under all possible operating and transient conditions.

Input Voltage VIN

AOZ5066QI is rated to operate over a wide input range of 4.5V to 25V. As with any other synchronous buck converter, large pulse currents at high frequency and extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to bypass the input supply very close to package leads with X7R or X5R quality ceramic capacitors.

The high side MOSFET in AOZ5066QI is optimized for fast switching with low duty ratios. It has ultra low gate charges which have been achieved as a trade off with higher $R_{DS(ON)}$ value. When the module is operated at low VIN the duty ratio will be higher and conduction losses in the HS FET will also be correspondingly higher. This will be compensated to some extent by reduced switching losses. The total power loss in the module may appear to be low even though in reality the HS MOSFET losses may be disproportionately high. Since the two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation, the HS FET may be much hotter than the LS FET. It is recommended that worst case junction temperature be measured and ensured to be within safe limits when the module is operated with high duty ratios.

PWM Input

AOZ5066QI is offered in two versions which can be interfaced with PWM logic compatible with either 5V (TTL) or 3V (CMOS). Refer to Figure 13 for the timing and propagation delays between the PWM input and the gate drives. The PWM is also a tri state compatible input. When the input is high impedance or unconnected both the gate drives will be off and the gates are held active low. The PWM Threshold Table (Table 1) lists the thresholds for high and low level transitions as well as tri state operation. As shown in Figure 13, there is a hold off delay between the time PWM signal enters the tri state window and the corresponding gate drive is pulled low. This delay is typically 170ns and intended to prevent spurious triggering of the tri state mode which may be caused either by noise induced glitches in the PWM waveform or slow rise and fall times.

Table 1. PWM Input and Tri State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5066QI	3.9V	1.0V	1.3V	3.7V
AOZ5066QI-01	2V	1V	1.3V	1.75V

Note: See Figure 13 for propagation delays and tri state window.

Diode Mode Emulation of Low Side MOSFET (SMOD)

AOZ5066QI can be operated in the diode emulation or skip mode using the SMOD pin. This is useful if the converter has to operate in asynchronous mode during start up, light load or under pre bias conditions. If SMOD is taken high, the controller will use the PWM signal as reference and generate both the high and low side complementary gate drive outputs with the minimal delays necessary to avoid cross conduction. When the pin is taken low the HS FET drive is not affected but diode emulation mode is activated for the LS FET. See Table 2 for a comprehensive view of all logic inputs and corresponding drive conditions.

Table 2. Control Logic Truth Table

DISB#	SMOD	PWM	GH	GL
L	X	X	L	L
H	L	H	H	L
H	L	L	L	See Note
H	H	Tri State	L	L
H	H	H	H	L
H	H	L	L	H

Note: Diode emulation mode is activated when SMOD pin is held low.

Gate Drives

AOZ5066QI has an internal high current high speed driver that generates the floating gate drive for the HS FET and a complementary drive for the LS FET. Propagation delays between transitions of the PWM waveform and corresponding gate drives are kept to the minimum. An internal shoot through protection scheme ensures that neither MOSFET turns on while the other one is still conducting, thereby preventing shoot through condition of the input current. When the PWM signal makes a transition from H → L or L → H, the corresponding gate drive GH or GL begins to turn off. The adaptive timing circuit monitors the falling edge of the gate voltage and when the level goes below 1V, the complementary gate driver is turned on. The dead time between the two switches is minimized, at the same time preventing cross conduction across the input bus. The adaptive circuit also monitors the switching node VSWH and ensures that transition from one MOSFET to another always takes place without cross conduction, even under transient and abnormal conditions of operation.

The gate pins GH and GL are brought out on pins 6 and 36 respectively. However these connections are not made directly to MOSFET gate pads and their voltage measurement may not reflect the actual gate voltage applied inside the package. The gate connections are primarily for functional tests during manufacturing and no connections should be made to them in the application.

Thermal Shutdown

The module temperature is internally sensed and an alarm is asserted if it exceeds 150°C. The alarm is reset when the temperature cools down to 135°C. The THDN is an open drain pin that is pulled to CGND to indicate an overtemperature condition. It may be pulled up to VCIN through a resistor for monitoring purposes.

PCB Layout Guidelines

AOZ5066 is a high current module rated for operation up to 1MHz. This requires extremely fast switching speeds to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package helps to minimise the driver-to-MOSFET gate pad connections without involving the parasitics of the package or PCB traces. While excellent switching speeds are achieved, correspondingly high levels of dv/dt and di/dt will be observed throughout the power train which requires careful attention to PCB layout to minimise voltage spikes and other transients. As with any synchronous buck converter layout the critical requirement is to minimise the area of the primary switching current loop, formed by the HS FET, LS FET and the input bypass capacitor C_{in}. The PCB design is somewhat simplified because of the optimized pin out in AOZ5066QI. The bulk of VIN and PGND pins are located adjacent to each other and the input bypass capacitors should be placed as close as possible to these pins. The area of the secondary switching loop, formed by LS FET, output inductor and output capacitor C_{out} is the next critical parameter. The ground plane should be extended and the negative pins of C_{out} should be returned to it, again as close as possible to the device pins.

While AOZ5066QI is extremely efficient it can still dissipate up to 6W of heat which requires attention to thermal design. MOSFETs in the package are directly attached to individual exposed pads to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal reliefs should be avoided to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the 12V system input, is desirable and vias should be provided near the device to connect the VIN

copper pour to the power plane. Though ground does not form a part of any device tabs, significant amount of heat is dissipated though multiple PGND pins. A large copper pour connected to PGND pins and further to the system ground plane through vias will further improve thermal management of the system.

Figure 15 illustrates the various copper pours and bypass capacitor locations.

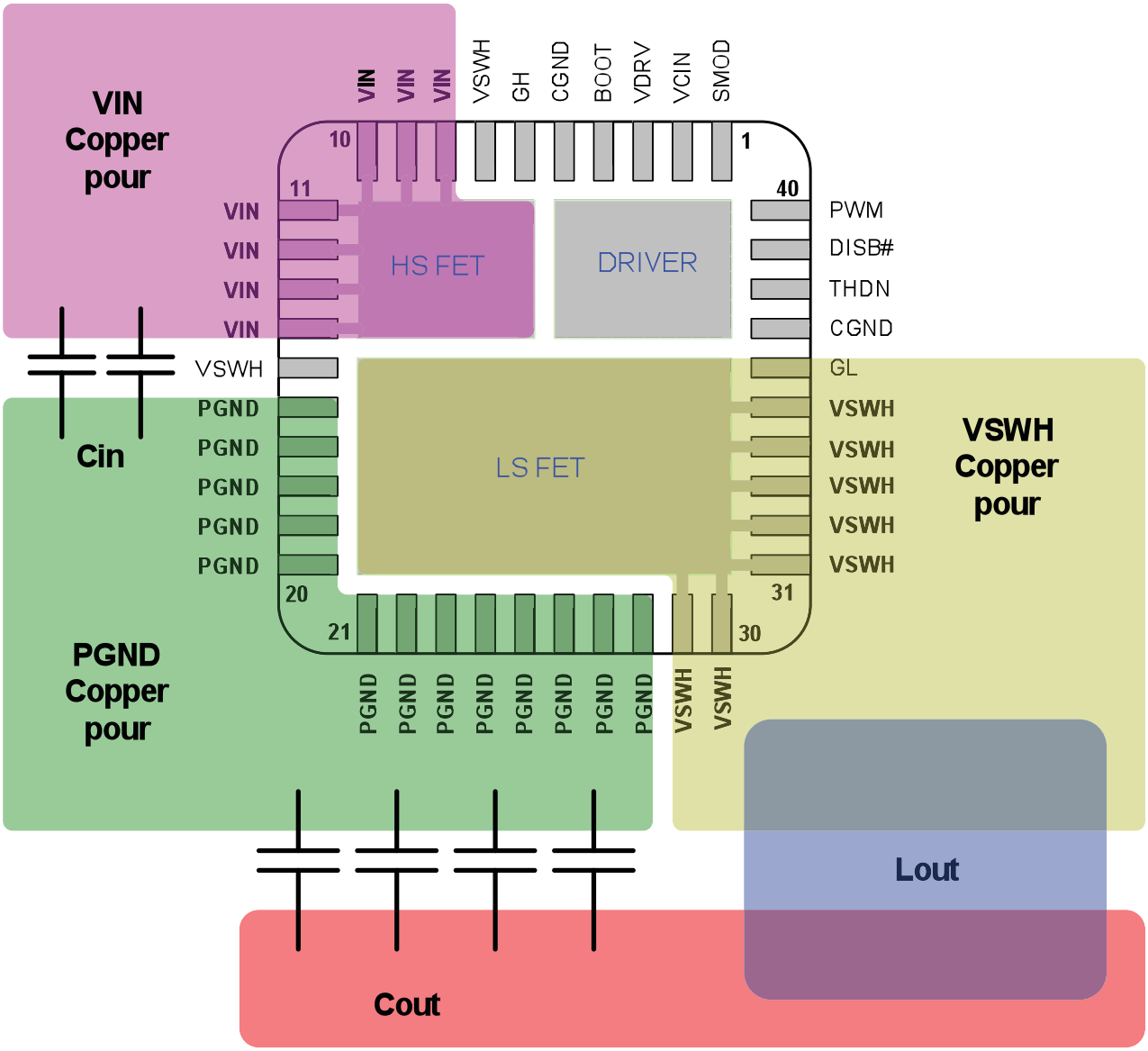
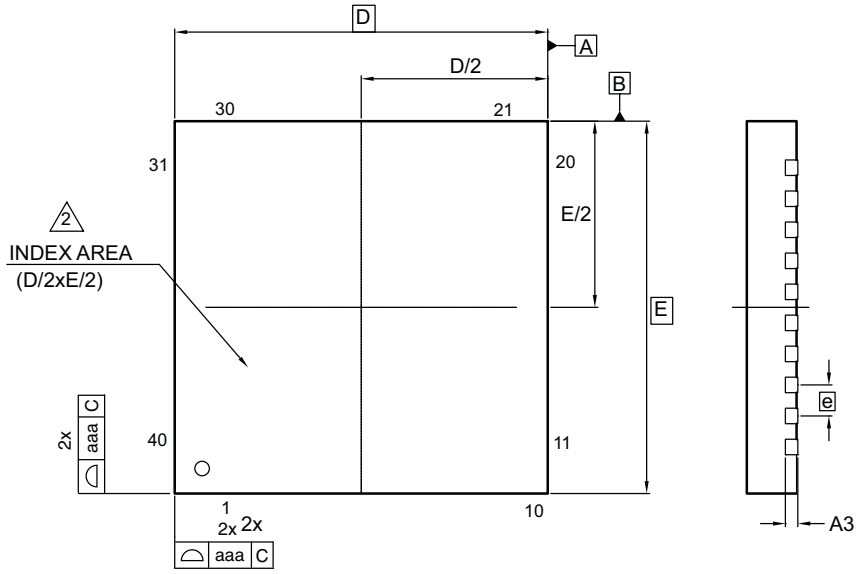
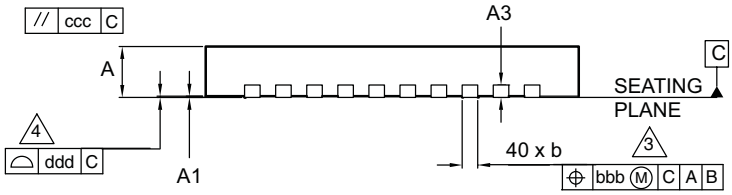


Figure 15. PCB Layout Illustration for Minimizing Current Loops

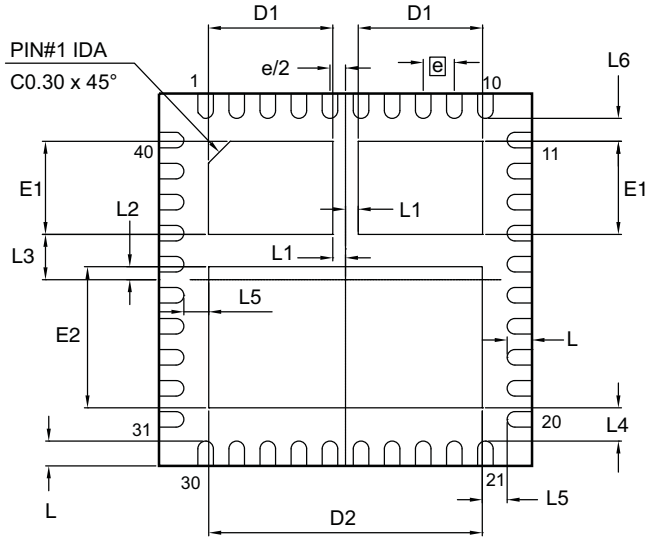
Package Dimensions, 6x6 QFN-40 EP3_S



TOP VIEW



SIDE VIEW

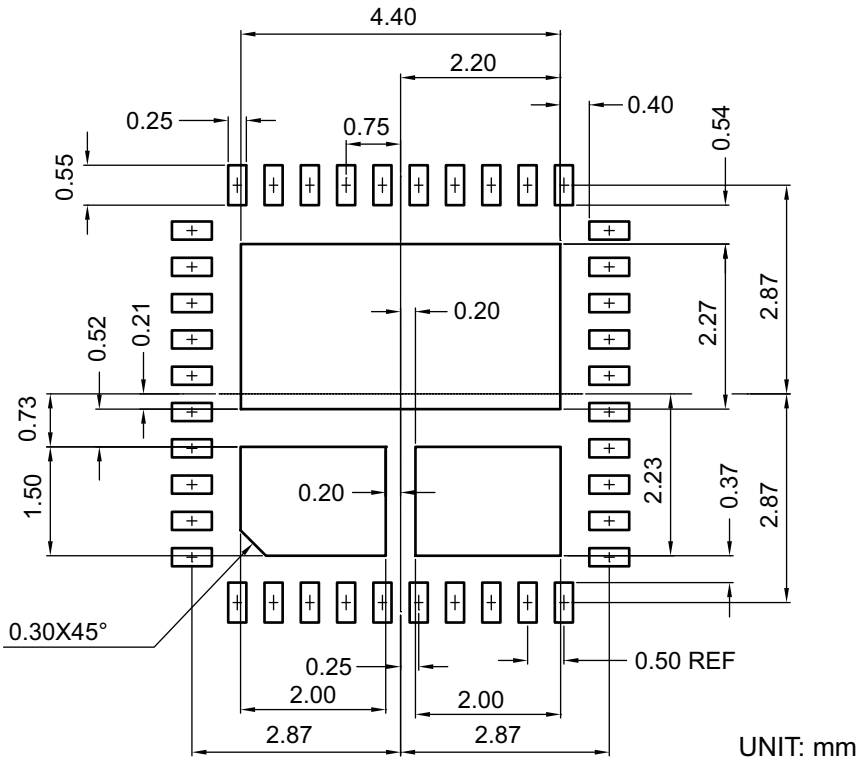


BOTTOM VIEW

Notes:

1. All dimensions are in millimeters.
2. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.
3. Dimension b applies to metallized terminal and is measured between 0.20mm and 0.35mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
4. Coplanarity applies to the terminals and all other bottom surface metalization.

Package Dimensions, 6x6 QFN-40 EP3_S (Continued)



RECOMMENDED LAND PATTERN

Dimensions in millimeters

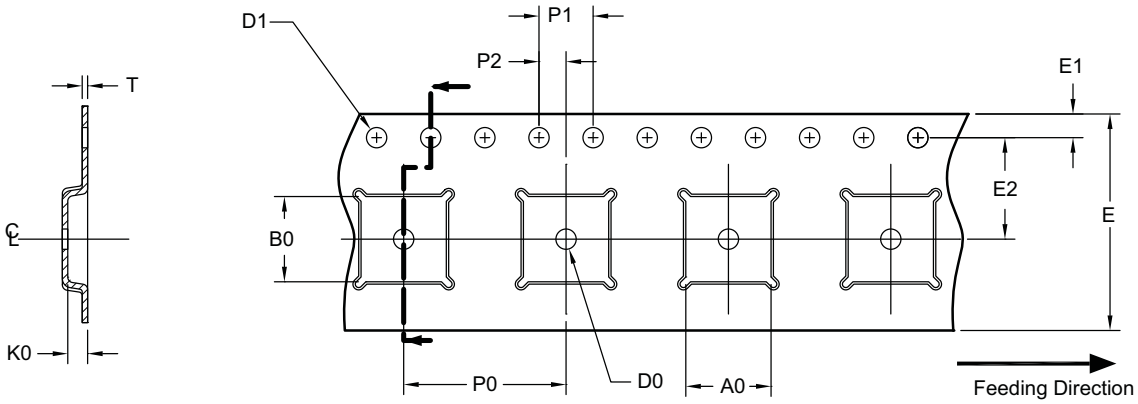
Symbols	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.35
D		6.00 BSC	
D1	1.90	2.00	2.10
D2	4.30	4.40	4.50
E		6.00 BSC	
E1	1.40	1.50	1.60
E2	2.17	2.27	2.37
e		0.50 BSC	
L	0.30	0.40	0.50
L1	0.15	0.20	0.25
L2	0.15	0.21	0.26
L3	0.63	0.73	0.83
L4	0.44	0.54	0.64
L5	0.30	0.40	0.50
L6	0.27	0.37	0.47
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.08	

Dimensions in inches

Symbols	Min.	Typ.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.008	0.010	0.014
D		0.236 BSC	
D1	0.075	0.079	0.083
D2	0.169	0.173	0.177
E		0.236 BSC	
E1	0.055	0.059	0.063
E2	0.085	0.089	0.093
e		0.020 BSC	
L	0.012	0.016	0.020
L1	0.006	0.008	0.010
L2	0.006	0.008	0.010
L3	0.024	0.028	0.032
L4	0.017	0.021	0.025
L5	0.012	0.016	0.020
L6	0.011	0.015	0.019
aaa		0.006	
bbb		0.004	
ccc		0.004	
ddd		0.003	

Tape and Reel Dimensions, 6x6 QFN

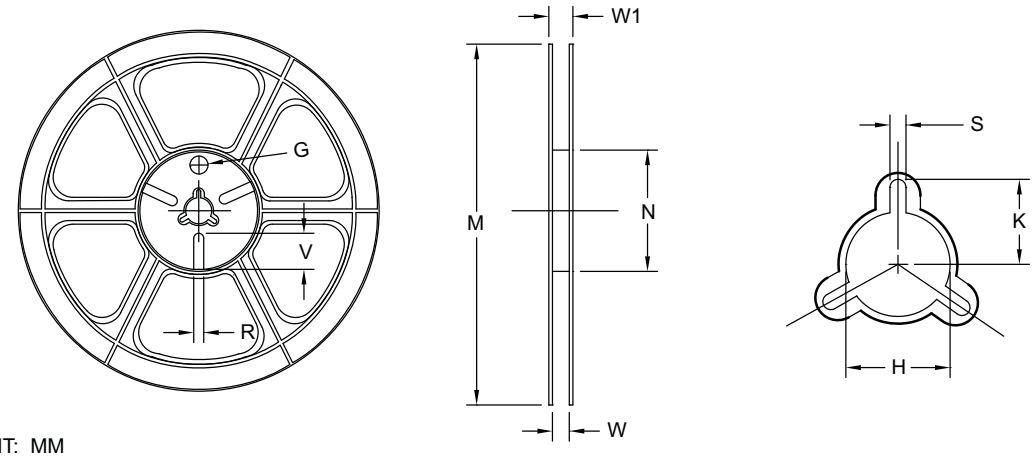
Carrier Tape



UNIT: MM

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN6x6 (16mm)	6.30 ±0.20	6.30 ±0.20	1.10 ±0.20	1.50 MIN.	1.50 +0.1 -0.0	16.0 ±0.3	1.75 ±0.10	7.5 ±0.1	12.00 ±0.20	4.00 ±0.20	2.00 ±0.10	0.30 ±0.05

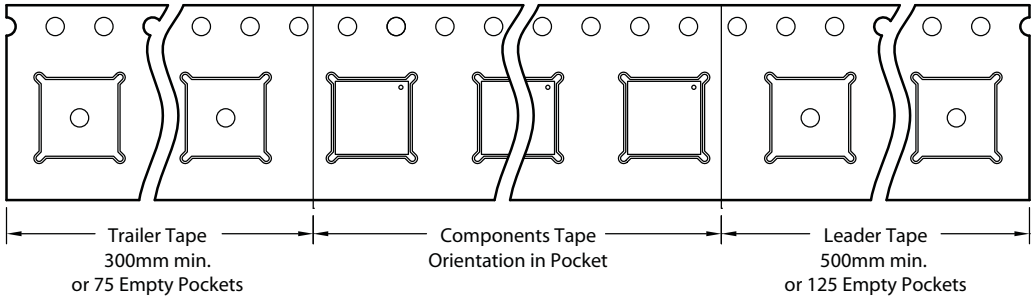
Reel



UNIT: MM

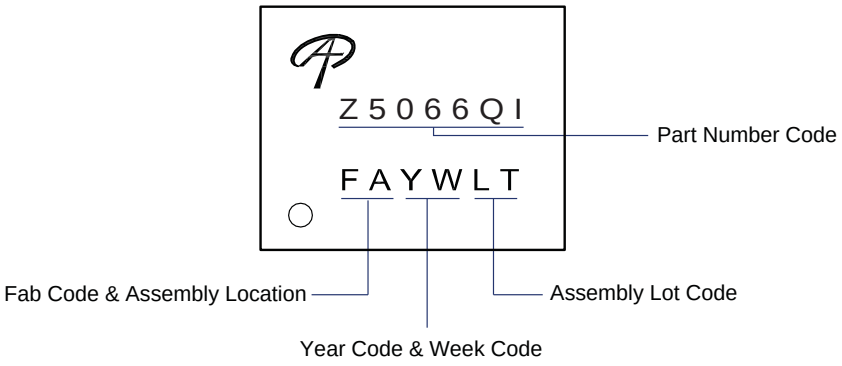
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
16mm	Ø330	Ø330 Max.	Ø100 Min.	16.4 +2.0 -0.0	22.4 Max.	Ø13.0 +0.5 -0.2	10.1 Min.	1.5 Min.	---	---	---

Leader/Trailer and Orientation

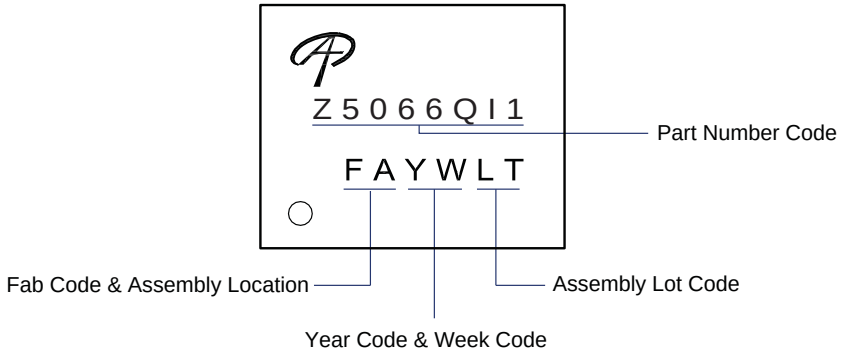


Part Marking

AOZ5066QI
(6.0 x 6.0 QFN)



AOZ5066QI-01
(6.0 x 6.0 QFN)



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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TITLE: AOS General Packing Spec

RELEASE DATE: 2012-07-09 | **OWNER DEPARTMENT: Product & Test**

REVISION HISTORY

(The original approval sheet is kept in DCC)

REVISION	RELEASE DATE	AUTHOR	DESCRIPTION OF CHANGES
A	2003-12-25	Limin Wang	Original
B	2003-12-25	Limin Wang	
C	2004-07-29	Emory Zhang	(1)Revise 6.3.2, 6.3.4, Appendix II, IV, and V(2)Add packing procedure 6.4
D	2004-08-23	Emory Zhang	Totally update (Removed detail package definition).
E	2004-10-31	Vicky Wang	1.Add 6.1.6 2.Update appendix II 3.Add appendix IV
F	2004-12-05	Emory Zhang	1.Add 6.1.6; Update Appendix II; Add Appendix IV.2.Add Pb free label (6.1.7/7.5); Add the rule for merge lots (6.1.8); Add the packing label printing requirement for special AOS part number and update €ship data€ print format. (Appendix II and Appendix III); Update 6.2.1.5.
G	2005-04-04	Emory Zhang	Specify the QC stamp for inner label and outer label. Appendix II and Appendix III;Added a note about green product does not need print €Pb free€ on inner/outer label. Appendix II and Appendix III. And updated 6.1.7.
H	2005-12-27	Hui Fang	H.New packing label layout.(Appendix III and IV)Add new special part which need add character at the right side of €Remark blank of label€. Add QC stamp instruction, Seal strip format on Appendix II, III and IV. Use a special €Pb Free€ label for all products with Normal Molding Compound + Pb FreePlating and Green products (6.1.7).
I	2006-09-08	Yunchao Shu	Rev.I.Add additional external label.
J	2006-11-15	Yunchao Shu	J.€Origin€ blank shall fill abbreviation country and district.Add standard PKG name in additional external label. Update inner label, if combine lot, the €Qty€ blank shall showdetail qty for two lots and €Remark€ blank shall shows combine lot NO. & barcode.Update the date code in all labels to 4 digital.
K	2006-12-06	Yunchao Shu	Rev.K Update inner label, if combine lot, the €Qty€ blank still show total quantity of the production in the inner box. Update the date code to 3 digital in all label.

L	2007-02-20	Yunchao Shu	Rev.L Adding Chinese. Introduce IMC (Internal Manufacturing Code) from this version pacing spec. Update label, add IMC information in inner and outer label. Update PKG name in additional label.
M	2007-05-28	Yunchao Shu	Rev.M Update related information of FAB location code in Appendix III and IV. Update package name reference in Appendix V.
N	2008-01-22	Yunchao Shu	Rev N:Remove "Ltd. from inner label
O	2008-07-01	Yunchao Shu	O.Modify the 6.2.1.6 description of static shielding packing. Copper wire product neednt show "Cu character in Remark blank. RG tested product need to show "RG in Remark blank. Modify FAB location code in Appendix III and IV. Modify the description of additional external label, the label shall be listed assembly lot No, date code and quantity information of every reel in the outer box.
P	2009-02-25	Yunchao Shu	P.Modify the 6.2.1.6 description of tape and reel. Add some package special date code definition in label description.
Q	2009-07-14	Yunchao Shu	Q:Define HF label and position.
R	2009-11-26	Yunchao Shu	R.Modify 6.1.9, date code combine limitation from 3 months to 6 months. Change the merged reel information of inner label Remark. Only the combined lot number should be printed in the REMARK area.
S	2010-08-23	Yunchao Shu	S.Update year, origin and FAB code of inner and outer label.
T	2010-11-01	Yunchao Shu	T.Update FAB code of inner and outer label.
U	2010-12-23	Yunchao Shu	U.Update FAB code of inner and outer label.
V	2011-04-13	Yunchao Shu	V.Update FAB code of inner and outer label. FAB Code 'G' denote 'Jxxx' wafer.
W	2011-08-10	Yunchao Shu	W.Define week code list in the spec. Unify date code definition in the packing label.
X	2011-12-18	Yunchao Shu	X.Update FAB code of inner and outer label.
Y	2012-07-09	Yunchao Shu	Y.Update inner label format and add marking code in the inner label.

TITLE: AOS PACKING SPEC
万代半导体包装规范

1 PURPOSE 目的

This specification shall serve as the basic spec for packing and labeling of the assembled AOS parts at all subcontractors.

此份规范目的是定义万代半导体所有代工厂生产的产品包装和标签的基本规范。

2 SCOPE 范围

This outline covers all packing and labeling of AOS assembled parts at all subcontractors.

此份规范应用于万代半导体所有代工厂生产的产品包装和标签。

3 REFERENCE DOCUMENT 参考文件

AOS Marking SPEC: MK type documents.

万代半导体打印规范：MK 类型的文件。

4 DEFINITION 定义

IMC: Internal Manufacturing Code 内部制造代码

5 GENERAL 概要

It's the responsibility of pacing engineer to update this document if necessary.

如有必要，由包装工程师负责更新该文件。

It's the responsibility of packing engineer to implement the requirement defined in this document.

由包装工程师负责执行该文件所定义的要求。

6 CONTENT 内容

6.1 General packing requirement 基本包装要求

6.1.1 One IMC product per carton box, no empty is allowed except the last box. Use empty inner box to fill up the rest of the carton box for damage prevention.

每种 IMC 产品一个外箱，除了最后一个外箱，其余的每个外箱都必须是满箱。如果最后一箱不是满箱，为了防止产品损坏，必须用空的内盒填满外箱。

6.1.2 QC stamp instruction for AOS product: No detail definition on outline, size, font, font size. But must contain below three instruction: Pls refer Appendix II for example.

应用于万代半导体 QC 图章的要求：不具体定义 QC 印章的外形，尺寸，字体和字号，但是必须满足以下 4 点要求：（可参考附件 II）

6.1.2.1 Have "QC ACCEPTED" or content in the stamp equivalent.

要有"QC ACCEPTED"或相近意思的字样。

6.1.2.2 All word shall be in English or digit.

在图章上的字词必须是英文或数字。

6.1.2.3 Staff number (digit) of QC shall be included in the mark.

必须要有 QC 检查人员的工号。

6.1.2.4 QC stamp should be on all labels. (Including label on tape reel, inner box, outer box)

所有的标签上必须有 QC 印章。（包括卷盘上的标签，内盒标签和外箱标签）

6.1.3 Inner label & QA Seal strip for AOS product: Refer Appendix III.

万代半导体内盒标签和 QA 封条，请参考附件 III。

6.1.4 Outer label for AOS product: Refer Appendix IV.

万代半导体外箱标签，请参考附件 IV。

6.1.5 Additional external label for AOS product: Refer Appendix V

万代半导体附加标签，请参考附件 V。

6.1.6 Use plastic wrap in carton to prevent moisture.

为防止内盒受潮，内盒要放进塑胶袋后再装入外箱。

6.1.7 Use AOS special adhesive tape (with AOS Logo) to seal the packing boxes (except Pizza box), refer Appendix VI.

在封外箱的时，使用带有万代半导体公司标识的封箱带（内箱不需使用），请参考附件 VI。

6.1.8 Use a special “Pb Free” label for the products with Normal Molding Compound + Pb Free Plating. Use a special “HF” label for the Green products. The special label should be affixed on Pizza box and outer Box, under the packing labels. (Refer Appendix VII).

普通塑封料加上无铅电镀的产品要使用指定的“Pb Free”标签。绿色产品要使用指定的“HF”标签。此标签粘贴于内盒标签和外箱标签的下方。

6.1.9 The date codes of merge lots can not over 6 months.

合并批的日期代码不能超过 6 个月。

6.2 Special packing requirement 特殊包装要求

6.2.1 Tape/Reel 编带/卷盘

6..2.1.1 There shall be min. 500 mm empty pockets sealed tape contained in the leader and min. 300 mm empty pockets sealed tape in the trailer. (Refer to Appendix I)

编带引带部分至少须留有 500mm 的封闭的空的编带，带尾部分至少须保留 300mm 封闭的空的编带。请参考附件 I。

6.2.1.2 Full reel quantity: no empty cavity is allowed, except in the leader & trailer.

满卷数量，在卷盘中，除了编带引带和带尾，中间不允许有空穴存在。

6.2.1.3 No tape repair is allowed. Once defective units are found in the tape, the whole reel must be de-taped and re-taped.

编带不允许有修补。一旦在编带中发现有缺陷产品，整卷产品都必须重新编带。

6.2.1.4 For products packed in tape/reel, maximum 2 assembly (Date Code) lots per reel except QA replacement units (QA replacement units quantity not over 10pcs). Lot A must be at the beginning of the

reel and Lot B at the other end. Units from both lots cannot be mixed together randomly. However, QA replacement can be mixed anywhere inside.

卷盘包装的产品，除了 QA 补料的产品（QA 补料产品最多不允许超过 10 颗），只允许有 2 个组装（日期代码）批在一卷产品中。两批产品不允许被随机的混合在一起。但是，QA 补料的产品可以被混合。

6.2.1.5 Use conductive adhesive tape to fix the carrier after Tape&Reel. No need other protective materials.

在编带卷盘后，使用导电粘合胶带来固定编带。不需要其他保护材料。

6.2.1.6 The reel shall be packed with static shielding bag (Transparent). The static shielding bag shall be air bleed and sealed by sealing machine. Ensure that no product is damaged and no tape / reel deformation happens. One reel was packed in one pizza box.

卷盘产品需用防静电袋包装后,经封口机排出空气并封口后再放入在内盒中，并保证产品,编带及卷盘不被损坏。每个内盒只能放一个卷盘。

6.2.1.7 Sealing the Ammo box (Pizza box) with a QA seal label, and QC stamp on sealing area after post pack inspection.

使用 QA 封条将内盒封住内盒，并在检查包装后加盖 QC 印章。

6.2.2 Tube packing requirement 管条包装要求

6.2.2.1 Full tube quantity, No empty is allowed in the tube.

要求满管数量，在管条中不允许有空。

6.2.2.2 For products packed in Tube, maximum 2 assembly (Date Code) lots per inner box.

使用管条包装时，一个内盒至多只允许 2 个组装（日期代码）批。

7 APPENDIX LIST 附件目录

7.1 Appendix I: Leader and Trailer of Tape & Reel Packing
附件 I：卷盘包装的引带和带尾示意图

7.2 Appendix II: QC stamp Format (Example)
附件 II：QC 印章示意图

7.3 Appendix III: Inner Label & QA Seal Strip Content
附件 III：内盒标签和 QA 封条

7.4 Appendix IV: Outer Label Content
附件 IV：外箱标签

7.5 Appendix V: Additional external label.
附件 V：附加外箱标签

7.6 Appendix VI: Sealing Tape
附件 VI：封箱带

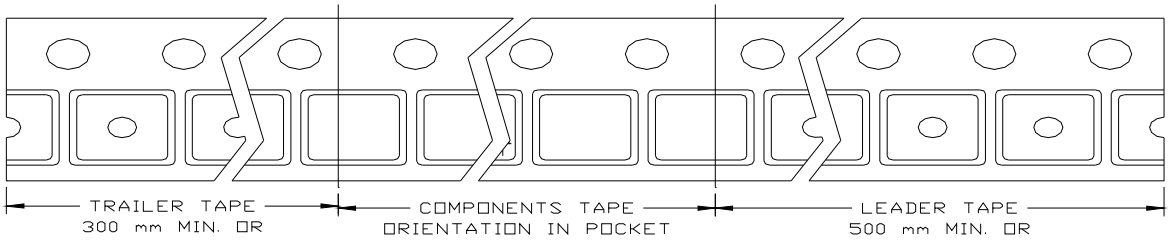
7.7 Appendix VII: Pb Free and HF special label & Position
附件 VII：无铅和无卤素标签及标签位置示意图

Appendix I

附件 I

Leader and Trailer of Tape & Reel Packing

卷盘包装的引带和带尾示意图



Feeding Direction

运行方向

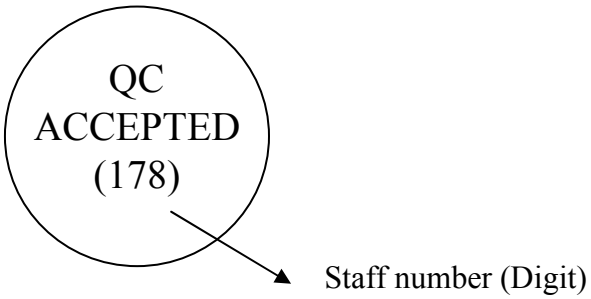
Appendix II

附件 II

QC stamp

QC 印章

Below is the just the example of the QC stamp

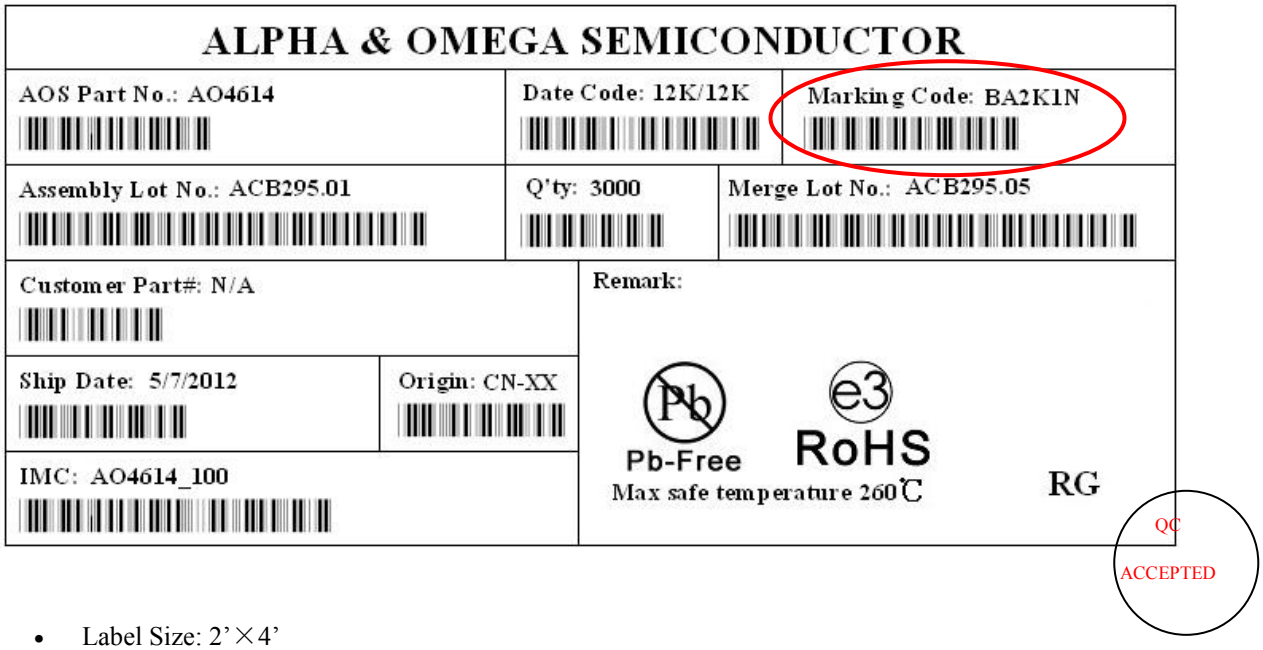


Appendix III

附件 III

Inner Label Content

内盒标签内容



- Label Size: 2'×4'
  标签尺寸：2 英寸×4 英寸
- Barcode: Use code 39. If using code 39 exceeds print space available, code 128 is preferred.
  条形码：使用 39 码。如果空间不够容纳 39 码，可以选用 128 码。
- If pass QC buy-off, QC should stamp at the place of QC stamp. The QC stamp shall not cover the barcode. Refer the above drawing, the content of QC Stamp should same as the above drawing, (XXX) is the number of QC operator.
  加盖 QC 印章时，QC 印章请不要遮盖到条形码。请参考以上示意图。
- Print format:
  打印格式：
  Company name: Times New Roman/12/Bold; Center-Center Alignment
  公司名称：Times New Roman/12/粗体；居中对齐。
  Other characters: Times New Toman/6/Normal; Left-Top Alignment
  其他字体：Times New Roman/6/正常；左对齐。
  Line: 0.75 pound
  线：0.75 磅。
- Print Color: Black
  文字颜色：黑色。

Label content: 标签内容

- Company name: **ALPHA & OMEGA SEMICONDUCTOR, LTD.**
  公司名称：**ALPHA & OMEGA SEMICONDUCTOR, LTD.**
- **IMC:**
  内部制造代码：
  - All AOS product shall have corresponding Internal Manufacturing Code.
    所有万代半导体的产品都有相应的内部制造代码。
  - For standard AOS product, the IMC is the same as its external product name officially published to all customers. Example: The IMC for AO4614 is AO4614. The IMC for AO4614L is AO4614L.
    对于万代半导体标准的产品，内部制造代码和万代半导体对外正式公布的名称相同。如：AO4614 的内部制造代码就还是 AO4614。AO4614L 的内部制造代码就还是 AO4614L。
  - The naming convention of Internal Manufacturing Code is defined as:
    内部制造代码的命名规则定义如下：

    [Standard AOS product name] _ [XXX]

    e.g. AO4614_100.
  - When AOS logistic issue PO, the IMC shall be filled in "**AOS PART NO.**" blank of the PO.
    当万代半导体下订单时，在订单"**AOS PART NO.**"这一栏中，会使用内部制造代码。

- **AOS Part Number:** Use Standard AOS product name. e.g. AO4614. (The letters before "_" of IMC).
  万代半导体产品名称：使用标准万代半导体产品名。例如：内部制造代码是 AO4614_100，在标签上的"AOS Part Number"则使用"_"前的字母，即 AO4614。
- **Date Code:** e.g. 06A ("06" stands for year code, "A" stands for work week code)
  日期代码：如 06A（"06"代表年代码，"A"代表工作周代码）
  For year code:
  年代码

Year Code	Year
08	2008
09	2009
10	2010
11	2011
12	2012
13	2013
14	2014
15	2015

For Work week code:

工作周代码

Week	WK Code	Week	WK Code	Week	WK Code	Week	WK Code
1 to 2	A	15 to 16	H	29 to 30	T	43 to 44	2
3 to 4	B	17 to 18	K	31 to 32	U	45 to 46	3
5 to 6	C	19 to 20	L	33 to 34	V	47 to 48	4
7 to 8	D	21 to 22	N	35 to 36	X	49 to 50	5
9 to 10	E	23 to 24	P	37 to 38	Y	51 to 52	6
11 to 12	F	25 to 26	R	39 to 40	Z	53	7
13 to 14	G	27 to 28	S	41 to 42	1		

In the merged lot, should show 2 date code. e.g. 06A/06B.

在合并批中，需显示 2 个日期代码。例如：06A/06B。

* Note: SOD523, SOD923, DFN1.0X0.6 and DFN0.6X0.3 four package products have special date code. To unify date code definition in the packing label, these four PKG products will follow general date code rule to print date code in the packing label (Year Code + Work Week Code)

* 注意：SOD523, SOD923，DFN1.0X0.6 和 DFN0.6X0.3 这四种封装形式的产品有特别的日期代码。为了统一在包装标签上日期代码的定义，这四种封装形式的产品将会按照一般日期代码的规则来打印包装标签上的日期代码（年代码+工作周代码）。

- **Marking Code:** Shows the marking code with lot information on product package. Below table summarize the major package which marking code shows on inner label.

  打印代码：显示在封装体上的带有组装批信息的打印代码。以下表格总结了主要的封装体需要在内盒标签上显示哪种打印代码。

Marking Type	Typical PKG	Typical Marking	Show In Label
One Line Marking	SOT23, SC70, SC89, SOD, D(Q)FN Small PKG, WLCSP	A0KA 11	A0KA11
Two Line Marking	SO8, TSSOP8, TO Serial, DFN, PDIP, Ultra-SO8	4614 BA2K1N	BA2K1N

- **Assembly Lot No. :** e.g. 123456 (If merged lot, show largest qty lot as mother lot A)

  封装批号：如 123456。如果是合并批，列出数量较大的那批为母批。

- **Quantity:** Actual quantity of product, e.g. 3000

数量：产品实际的数量。如 3000。

- **Customer Part #:** e.g. 1234567,If there is no information of customer part, it should be “NA”.

  客户产品代码：如 1234567。如果没有客户产品代码信息，需显示“N/A”。

- **Ship Date:** Estimate ship date , the format should be: MM/DD/YYYY(e.g. 07/31/2006)

  运送日期：预估的运送日期，格式为月/日/年（如 07/31/2006）

- **Origin:** e.g. CN-XX.

  产地：如 CN-XX

  “CN” position shall fill abbreviation of supplier country or district. Below is some country and district abbreviation.

  “CN”的位置应该填入供应商国家或地区的字母缩写。以下下是一些国家或地区的缩写。

Country And District	Shortened Form
CHINA	CN
HONGKONG	HK
JAPAN	JP
MALAYSIA	MY
PHILIPPINES	PH
REPUBLIC OF KOREA	KR
TAIWAN	TW
THAILAND	TH
UNITED STATES	US

The 1st “X” is for FAB subcontractor code. It can be distinguished from wafer ID. The FAB code please refers to below list. If dual or triple die in one package, the FAB code please according to the wafer ID of chip1.

第一个“X”代表FAB厂的代码。可通过芯片名称进行辨识。请参考以下表格。如果是双芯片或三芯片的产品，请按照配线图第一个芯片名称来打印FAB厂代码。

FAB Code	Wafer ID
B	AOSNxxx or AOSPxxx or Bxxxxx or Fxxxxx or Hxxxxx or Sxxxxx (except B286)
C	ANxxx or APxxx or AYxxx or AQxxx
D	Dxxx
E	Xxxx or Yxxx or Zxxx
F	Gxxx
T	ISLxxx
U	9B002-1
V	AXxxx
X	Rxxx
Y	S-xxx
Z	Uxxx
G	Jxxx or J2904 or B286

Note: "xxx" denote any digital number and letter.

注释："xxx"代表任意位数的任意位数的数字和字母。

The 2nd "X" is for assembly subcontractor code. Please refer to "BOM SPEC".

第二个"X"是封装厂的代码。具体请参考"BOM SPEC"。

- **Remark:**
- **备注：**

If merged lot, only the combined lot (child lot) number should be printed in the REMARK area. If not, it needn't be shown.)

如果是合并批，则在 REMARK 区域只打印被合并批(子批)的批号及它的条形码。如果不是合并批，则不需显示。

If the product was done 100% RG testing, the "RG" character shall be shown in the Remark blank. RG tested product can't be combined with none RG tested product.

如果经过 100% RG 测试过的产品，必须在 Remark 栏里显示"RG"字样。测过 RG 的产品不能和未测过 RG 的产品混在一起。

For Pb free products (normal compound + Pb free plating) and Green product: Add "PB FREE" characters and logo. Add "RoHS" characters. Add "Max safe temperature: 260℃". Add terminal finish/material category number. Details please see below table.

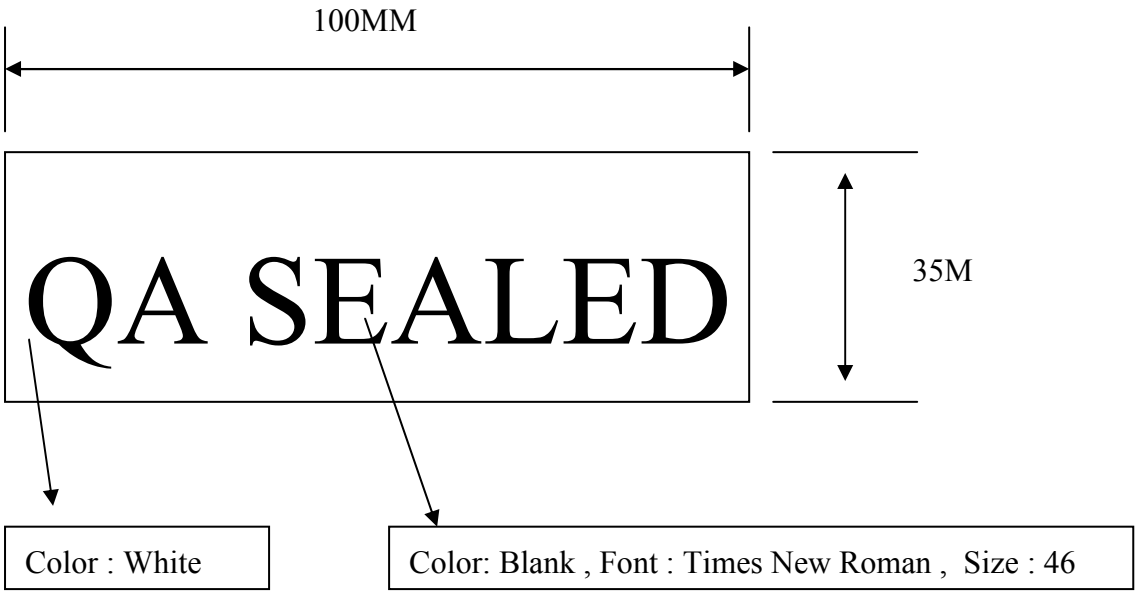
对于无铅的产品（普通塑封料+无铅电镀）和绿色产品：需打印“PB FREE”的字样和标识。需打印“RoHS”字样。需打印“Max safe temperature: 260℃”。需打印材料类别号。具体请见下表。

Mark	Material Type
(e1)	SnAgCu (shall not be included in category e2)
(e2)	Sn alloys with no Bi or Zn (excluding SnAgCu)
(e3)	Sn
(e4)	Precious metal (e.g., Ag, Au, NiPd, NiPdAu) (no Sn)
(e5)	SnZn, SnZnx (no Bi)
(e6)	Contains Bi
(e7)	Low temperature solder (≤ 150 °C) containing Indium (no Bi)

For Normal product: Keep it blank.

普通的产品，则不需打印材料有关信息。

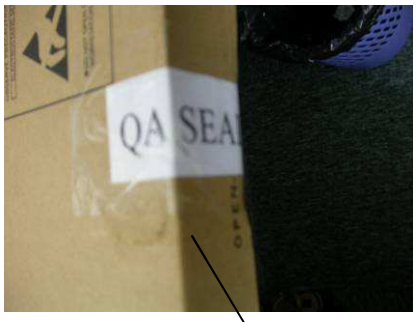
QA Seal Strip
QA 封条



***Note: If subcon need to use own format QA seal strip for special issue, subcon shall send out formal report for AOS approval. If AOS didn't approve it, subcon shall follow AOS standard format QA seal strip.**

***注：如果封装厂由于特殊原因要使用自己格式的 QA 封条，封装厂需要发出正式的报告给 AOS 审批。如果 AOS 不能接受，封装厂则必须使用 AOS 标准格式的 QA 封条。**

Strip seal position:



Pizza Box

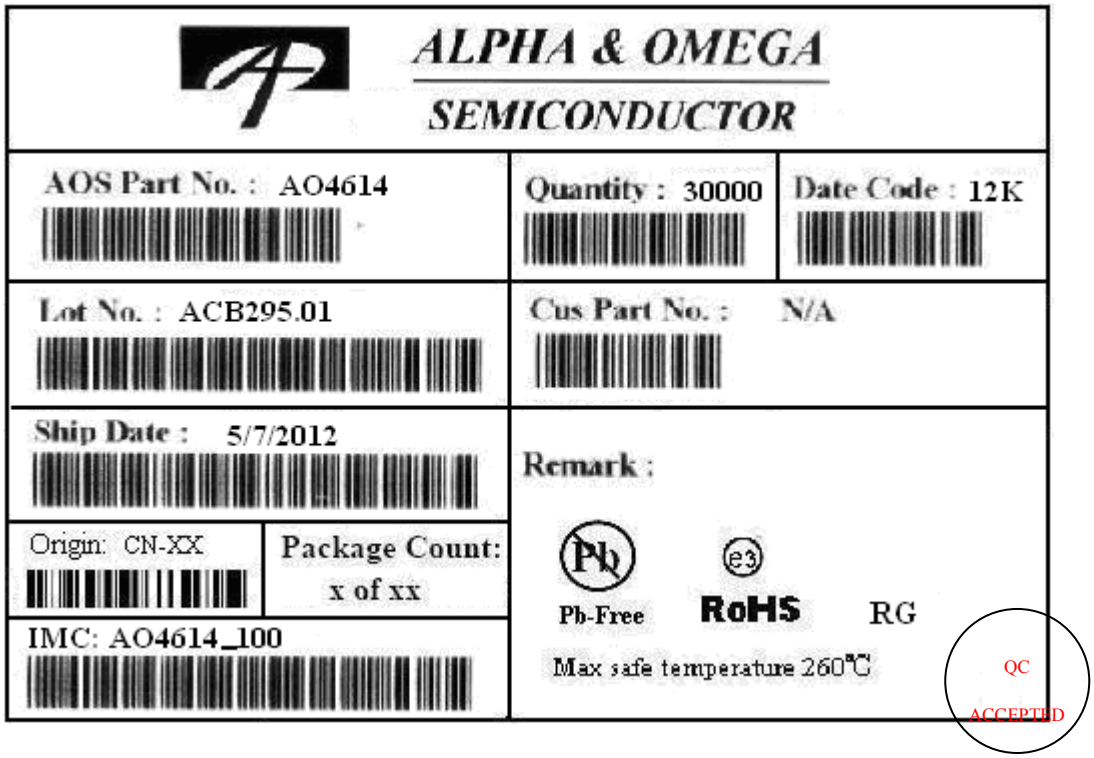
Seal strip position: Aside "Open "

Appendix IV

附件 IV

Outer Label Content

外箱标签内容



- Label Size: 4”×6”
  标签尺寸：4 英寸×6 英寸
- Barcode: Use code 39. If using code 39 exceeds print space available, code 128 is preferred.
  条形码：使用 39 码。如果空间不够容纳 39 码，可以选用 128 码。
- If pass QC buy-off, QC should stamp at the place of QC stamp. The QC stamp shall not cover the barcode. Refer the above drawing, the content of QC Stamp should same as the above drawing, (XXX) is the number of QC operator.
  加盖 QC 印章时，QC 印章请不要遮盖到条形码。请参考以上示意图。
- Print format:
  打印格式：
  AOS Logo: Width: 10 mm; Length: 100mm. Center-Center alignment.
  公司标识：宽：10 毫米；长 100 毫米。居中对齐。
  Other characters: Times New Toman/10/Bold; Left-Top Alignment
  其他字体：Times New Roman/10/粗体；左对齐。
  Line: 1.5 pound
  线：1.5 磅。

- Print Color: Black
  文字颜色：黑色。

Label content:

- **AOS Logo** AOS Logo 万代公司标识
- **IMC:**

  内部制造代码：

  - All AOS product shall have corresponding Internal Manufacturing Code.
    所有万代半导体的产品都有相应的内部制造代码。
  - For standard AOS product, the IMC is the same as its external product name officially published to all customers. Example: The IMC for AO4614 is AO4614. The IMC for AO4614L is AO4614L.
    对于万代半导体标准的产品，内部制造代码和万代半导体对外正式公布的名称相同。如：AO4614 的内部制造代码就还是 AO4614。AO4614L 的内部制造代码就还是 AO4614L。
  - The naming convention of Internal Manufacturing Code is defined as:
    内部制造代码的命名规则定义如下：

    [Standard AOS product name] _ [XXX]

    e.g. AO4614_100.
  - When AOS logistic issue PO, the IMC shall be filled in "**AOS PART NO.**" blank of the PO.
    当万代半导体下订单时，在订单"**AOS PART NO.**"这一栏中，会使用内部制造代码。

- **AOS Part Number:** Use Standard AOS product name. e.g. AO4614. (The letters before "_" of IMC).

  万代半导体产品名称：使用标准万代半导体产品名。例如：内部制造代码是 AO4614_100，在标签上的"AOS Part Number"则使用"_"前的字母，即 AO4614。

- **Customer Part #:** e.g. 1234567,If there is no information of customer part, it should be "NA".

  客户产品代码：如 1234567。如果没有客户产品代码信息，需显示"N/A"。

- **Lot No.**: Assembly Lot No. (e.g.123456). Only the lot no with largest qty is shown.

  封装批号：如 123456。只列出在外箱中数量最大的那批产品的批号。

- **Q'ty**： Actual quantity in carton, e.g. 36000

  数量：产品实际的数量。如 36000。

- **Ship Date**: Print format should be: MM/DD/YYYY, (e.g. 7/31/2006)

运送日期：格式为月/日/年（如 07/31/2006）

- **Date Code:** e.g. 06A ("06" stands for year code, "A" stands for work week code)

  日期代码：如 06A（"06"代表年代码，"A"代表工作周代码）

For year code:

年代码

Year Code	Year
08	2008
09	2009
10	2010
11	2011
12	2012
13	2013
14	2014
15	2015

For Work week code:

工作周代码

Week	WK Code	Week	WK Code	Week	WK Code	Week	WK Code
1 to 2	A	15 to 16	H	29 to 30	T	43 to 44	2
3 to 4	B	17 to 18	K	31 to 32	U	45 to 46	3
5 to 6	C	19 to 20	L	33 to 34	V	47 to 48	4
7 to 8	D	21 to 22	N	35 to 36	X	49 to 50	5
9 to 10	E	23 to 24	P	37 to 38	Y	51 to 52	6
11 to 12	F	25 to 26	R	39 to 40	Z	53	7
13 to 14	G	27 to 28	S	41 to 42	1		

* Note: SOD523, SOD923, DFN1.0X0.6 and DFN0.6X0.3 four package products have special date code. To unify date code definition in the packing label, these four PKG products will follow general date code rule to print date code in the packing label (Year Code + Work Week Code)

* 注意：SOD523, SOD923，DFN1.0X0.6 和 DFN0.6X0.3 这四种封装形式的产品有特别的日期代码。为了统一在包装标签上日期代码的定义，这四种封装形式的产品将会按照一般日期代码的规则来打印包装标签上的日期代码（年代码+工作周代码）。

- **Origin:** e.g. CN-XX.

  产地：如 CN-XX

  "CN" position shall fill abbreviation of supplier country or district. Below is some country and district abbreviation.

“CN”的位置应该填入供应商国家或地区的字母缩写。一下是一些国家或地区的缩写。

Country And District	Shortened Form
CHINA	CN
HONGKONG	HK
JAPAN	JP
MALAYSIA	MY
PHILIPPINES	PH
REPUBLIC OF KOREA	KR
TAIWAN	TW
THAILAND	TH
UNITED STATES	US

The 1st “X” is for FAB subcontractor code. It can be distinguished from wafer ID. The FAB code please refers to below list. If dual or triple die in one package, the FAB code please according to the wafer ID of chip1.

第一个“X”代表FAB厂的代码。可通过芯片名称进行辨识。请参考以下表格。如果是双芯片或三芯片的产品，请按照配线图第一个芯片名称来打印FAB厂代码。

FAB Code	Wafer ID
B	AOSNxxx or AOSPxxx or Bxxxxx or Fxxxxx or Hxxxxx or Sxxxxx (except B286)
C	ANxxx or APxxx or AYxxx or AQxxx
D	Dxxx
E	Xxxx or Yxxx or Zxxx
F	Gxxx
T	ISLxxx
U	9B002-1
V	AXxxx
X	Rxxx
Y	S-xxx
Z	Uxxx
G	Jxxx or J2904 or B286

Note: "xxx" denote any digital number and letter.

注释："xxx"代表任意位数的任意位数的数字和字母。

The 2nd “X” is for assembly subcontractor code. Please refer to "BOM SPEC".

第二个“X”是封装厂的代码。具体请参考“BOM SPEC”。

- **Remark:**

- **备注：**

If the product was done 100% RG testing, the “RG” character shall be shown in the Remark blank. RG tested product can’t be combined with none RG tested product.

如果经过 100% RG 测试过的产品，必须在 Remark 栏里显示“RG”字样。测过 RG 的产品不能和未测过 RG 的产品混在一起。

For Pb free products (normal compound + Pb free plating) and Green product: Add “PB FREE” characters and logo. Add “RoHS” characters. Add “Max safe temperature: 260℃”. Add terminal finish/material category number. Details please see below table.

对于无铅的产品（普通塑封料+无铅电镀）和绿色产品：需打印“PB FREE”的字样和标识。需打印“RoHS”字样。需打印“Max safe temperature: 260℃”。需打印材料类别号。具体请见下表。

Mark	Material Type
e1	SnAgCu (shall not be included in category e2)
e2	Sn alloys with no Bi or Zn (excluding SnAgCu)
e3	Sn
e4	Precious metal (e.g., Ag, Au, NiPd, NiPdAu) (no Sn)
e5	SnZn, SnZnx (no Bi)
e6	Contains Bi
e7	Low temperature solder (≤ 150 °C) containing Indium (no Bi)

For Normal product: Keep it blank.

普通的产品，则不需打印材料有关信息。

- **Package count**: e.g. 1 of 11.

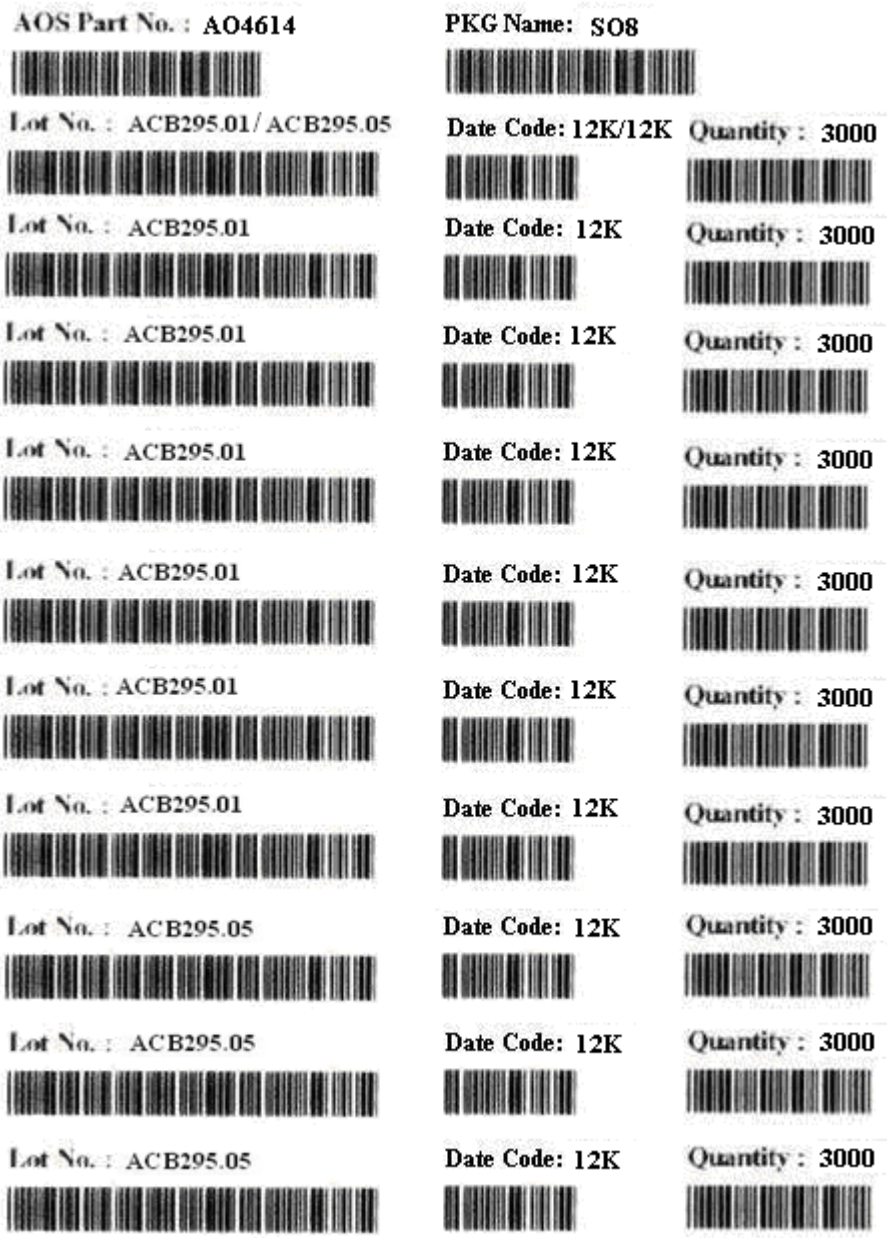
包装箱计数：如 1 of 11

Appendix V

附件 V

Additional external label

附加外箱标签



- **Description: 描述**

  The label paste on the outer box and list assembly lot No, date code and quantity information of every reel in outer box.

这张标签贴于外箱。主要列出了外箱内每一个卷盘的批号，日期代码和数量信息。

- **Label Size:** 4“×6”

  标签尺寸：4 英寸×6 英寸

- **Barcode:** Use code 39. If using code 39 exceeds print space available, code 128 is preferred.

  条形码：使用 39 码。如果空间不够容纳 39 码，可以选用 128 码。

- **Font:**

  字体：

  Other characters: Times New Toman/10/Bold; Left-Top Alignment

  其他字体：Times New Roman/10/粗体；左对齐。

  Line: 1.5 pound

  线：1.5 磅。

  Print Color: Black

  文字颜色：黑色。

- **Label Content:**

  标签内容：

  The first line: AOS Part No. and AOS specify standard PKG Name. AOS Part No. use AOS standard product name. AOS standard PKG Name please use “Package Type” of relevant AOS PO.

  第一行列出万代半导体的产品名称和封装名称。产品名称使用万代半导体标准产品名。封装名称请使用万代半导体订单上“封装类型”中的名称。

  Other lines: Every line shall show every reel Assembly Lot No., Date Code and Quantity. If merged reel, it shall be shown two lots Assembly Lot No and Date Code. e. g. Lot No.: 123456/134528 Date Code: 06A/06B

  其他行，每行必须列出每个卷盘的封装批次号，日期代码和每批的具体数量。如果是合并卷，则必须列出两个合并的封装批号和日期代码。如： Lot No.: 123456/134528 Date Code: 06A/06B

- **Label Position:** Stick beside outer box packing label. Details please refer Appendix VII.

标签位置：贴在外箱标签旁边。具体请参见附件 VII。

- **Others:** Every content need barcode. If one label can't include all assembly lots, please add one label. And stick below first label.

  其他：每一项内容都需要条形码。如果一张标签不能列出所有的批次的信息，可在第一张附加标签下加贴另一张标签。

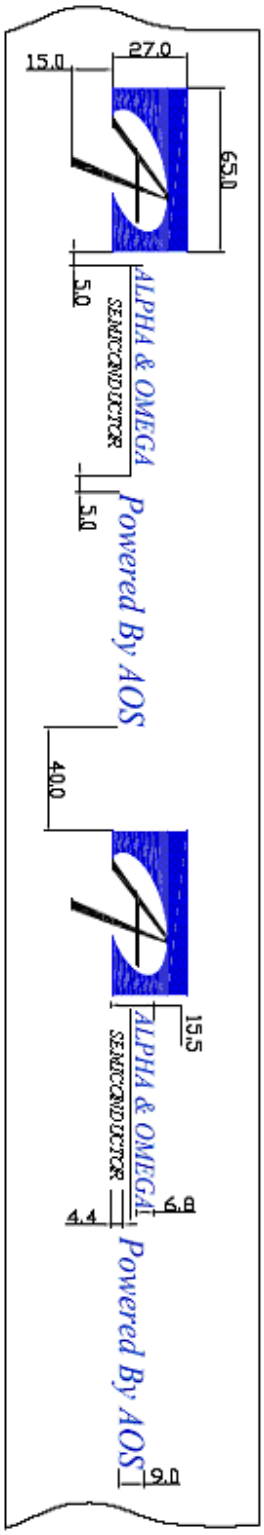
Appendix VI

附件 VI

Sealing tape

封箱带

Character Font: Times New Roman

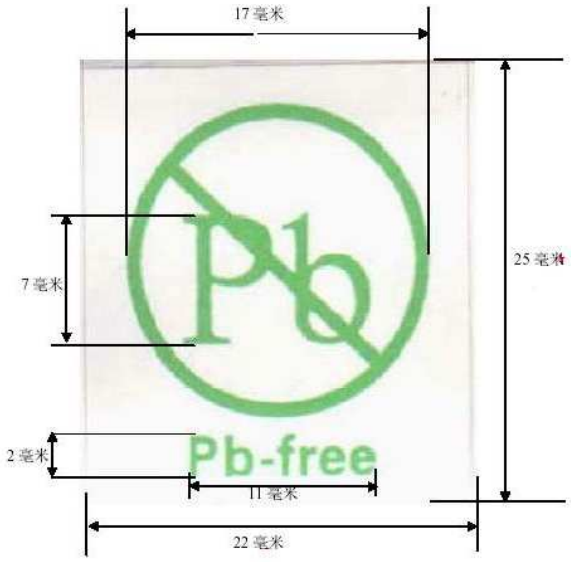


Appendix VII

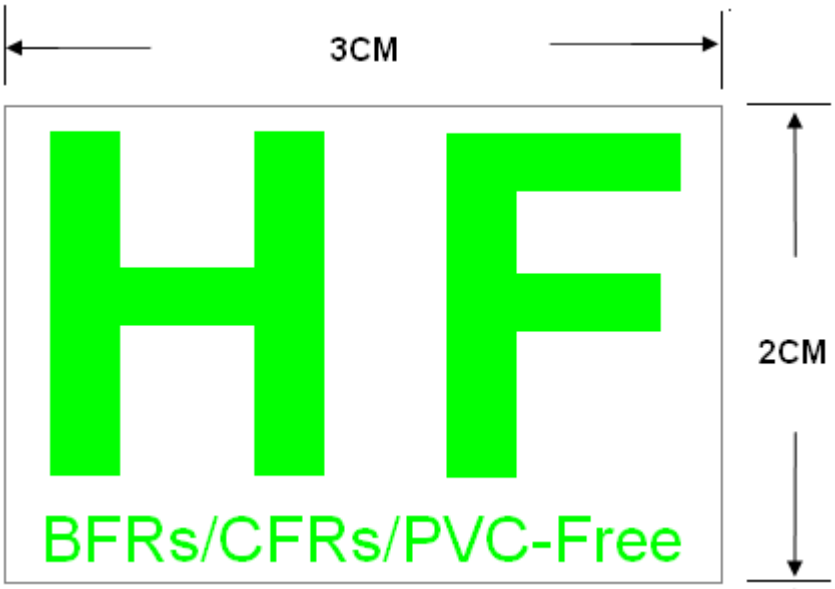
附件 VII

Pb Free and HF special label & Position

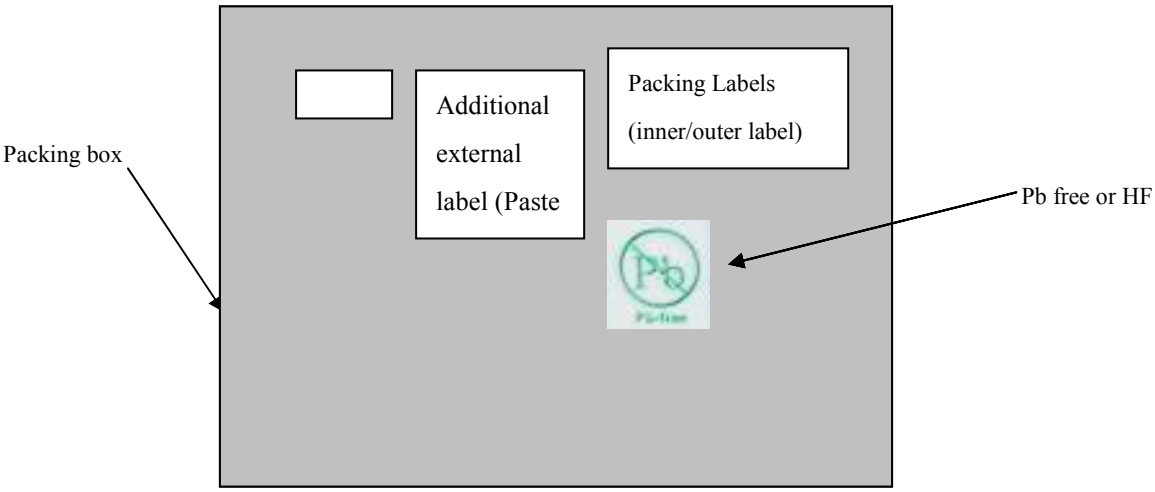
无铅和无卤素标签及标签位置示意图



Pb Free Label



HF Label



Label Position

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Recommended Temperature Profile For Soldering AOS Product with Lead Free Solder

For AOS internal reliability precondition profile see Appendix A

TITLE: Soldering Temperature Profile of AOS Product with Lead free solder

1 PURPOSE

This document defines the recommendation of soldering temperature profiles for all the Alpha & Omega Semiconductor (AOS) products. Using temperature and time duration not to exceed these conditions will prevent damage to the parts during the mounting processes, and also help to ensure the quality and reliability of AOS parts.

2 SCOPE

This procedure is applicable to all of AOS product/packages that are required to perform soldering on to PCB (Printed circuit board)

3 REFERENCE DOCUMENTS

JESD22-A113，Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

IPC/JEDEC J-STD-020D，Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

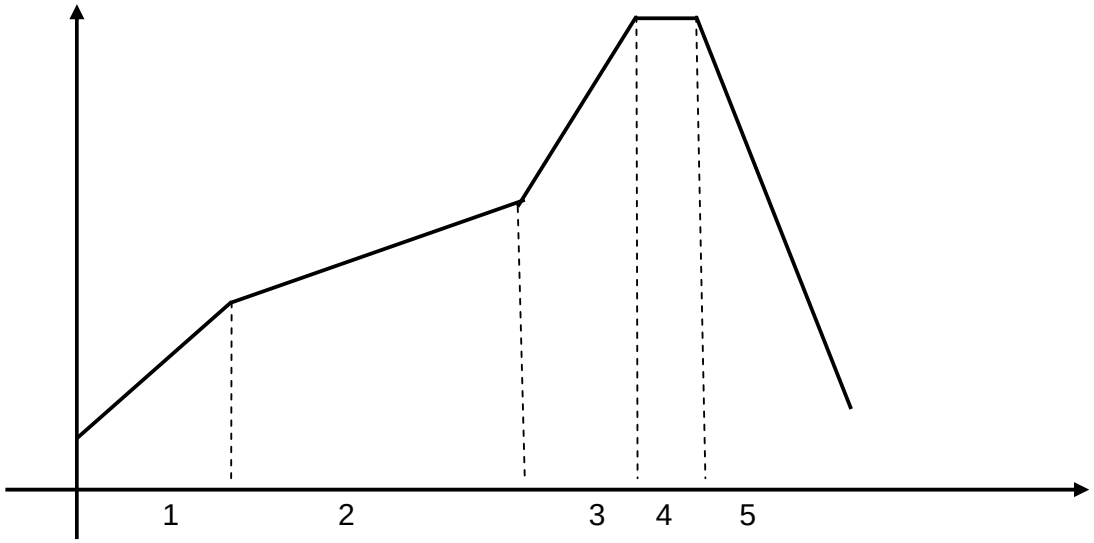
4 GENERAL

Soldering profile is used in PCB assembly. Since different system, different components and different solder are used by different customer, the optimum soldering condition to insure the solder integrity and reliability can only be determined by user (customer). AOS does not assume any responsibilities for the recommendation outlined in this document.

However during the reliability qualification, AOS parts are subject to very severe condition in accordance with the IPC/JEDEC J-STD-20D document (see profile in Appendix A), which involves one week moisture absorption in 85 ºC and 85% relative humidity follow by three solder reflows simulation for 30 sec at peak temperature between 255 ºC and 260 ºC. By using temperature and time duration not to exceed these recommended conditions will be obviously not damage AOS parts.

5 Recommended Soldering Profile

5.1 Reflow Soldering Profile:



Profile Feature	**Requirement**
1. Ramp up	1-4 ºC/second
2. Soak	150 ºC~200 ºC 60-180 seconds
3. Ramp up	1-4ºC/second
4. Peak soak *	245~260 ºC 10 seconds max
5. Ramp-down Rate	1~6 ºC/second max.

* Maximum thermal excursion allowed during the reflow assembly is as follow:

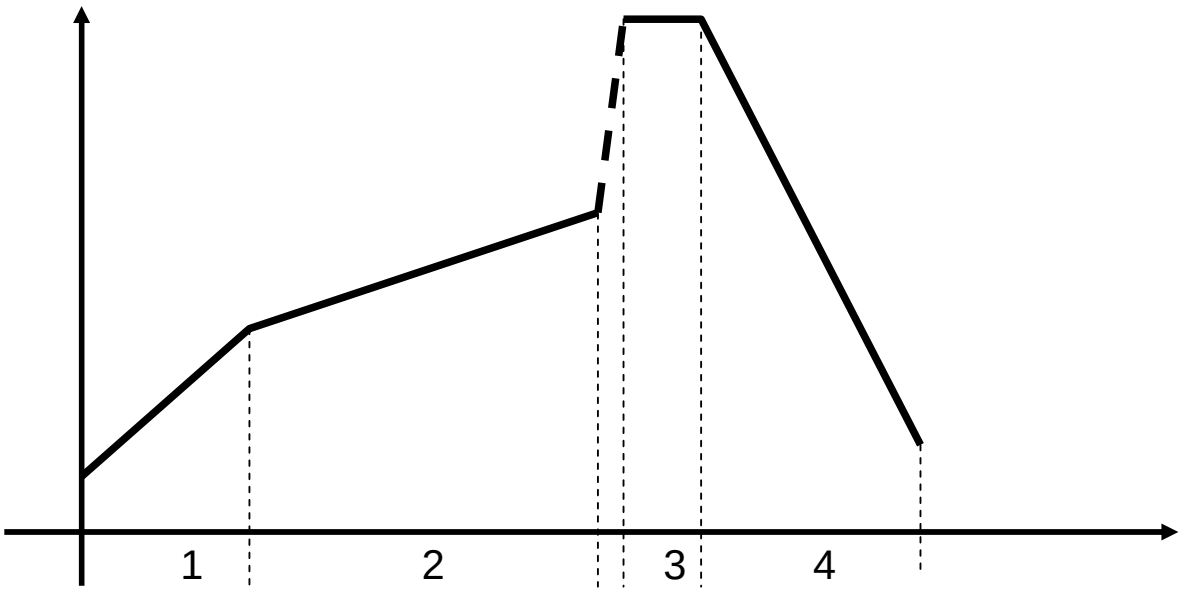
Temperature: 255 ºC ~ 260 ºC

Duration at peak soak: 30 sec

Number of reflow: 3

5.2 Wave Soldering Profile:

Not recommended for leadless package



Profile Feature	**Recommended Condition**
1. Preheat - Ramp up rate	1-7 ºC/second
2. Soak - Temprature: - Time:	80ºC ramp to 140ºC 60-120 seconds
3. Peak - Peak package body temperature - Time	245 ºC to 260 ºC 10 seconds max.
4. Ramp down: - Ramp down rate:	1-7 ºC/second

5.3 Hand Soldering:

Not recommended for mass production. For engineering project or re-work should be used with cautious

Parameters	**Recommended Condition**
Tip Temperature	350 ±10 ºC
Time*	3 seconds

*Maximum duration is 5 seconds

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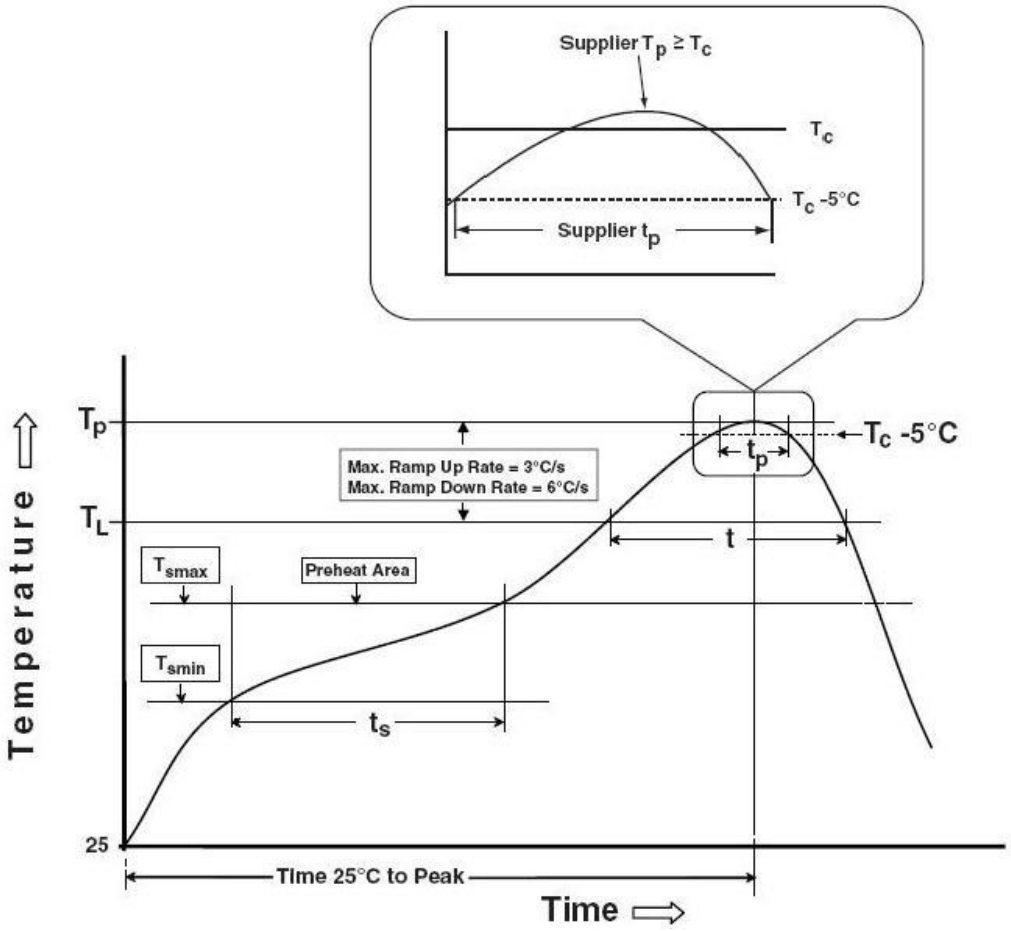
Appendix A

AOS internal reflow profile for reliability test precondition is as follow:



Profile Feature	**Condition**
Preheat & Soak - Temperature Min ($T_{S(min)}$): - Temperature Max ($T_{S(min)}$): - Time (min to max)(ts):	 150 ºC 200 ºC 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 ºC/second max
Liquidous Temperature (T_L): Time (t_L):	217 ºC 60-150 seconds
Peak Package body Temperature(T_p)*: See IPC/JEDEC J-STD-020 for detail	Tp must equal to or exceed the Classification Temperature. Typically Tp = 260 ºC
Time t_p within 5ºC of specified classification temperature (T_C):	30 seconds min.
Ramp-down Rate (T_p to $T_{smax)}$:	6 ºC/second max.
Time 25 ºC to Peak Temp. :	8 minutes max

AOS Semiconductor
Product Reliability Report

AOZ5036QI, AOZ5036QI-01, AOZ5066QI, AOZ5066QI-01

rev 1.0

Plastic Encapsulated Device

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ALPHA & OMEGA SEMICONDUCTOR

August 7, 2013

This AOS product reliability report summarizes the qualification result for AOZ5036QI-01. The Qualification results would apply to AOZ5036QI, AOZ5066QI and AOZ5066QI-01 as well. AOZ5066QI/AOZ5066QI-01 is the marking version of AOZ5036QI/AOZ5036QI-01 respectively.

Review of the electrical test results confirmed that AOZ5036QI-01 passes AOS quality and reliability requirements for final product and package release.

Table of Contents:

I. Product Description:

The AOZ5036QI-01 is a high-efficiency Driver plus MOSFET output stage. The AOZ5036QI-01 is available in a tiny 6mm x 6mm 40-pin QFN package and is rated over a -40°C to +85°C operating temperature range.

Absolute Maximum Ratings	
Parameter	**Rating**
Supply Voltage (VIN)	-0.3V to 25V
Switch Node Voltage (VSWH)	-0.8V to 25V
Bootstrap Voltage (VBOOT)	-0.3V to 25V
VBOOT Voltage Transient	36V
Supply and Gate Drive Voltages { VCIN, VDRV, (VBOOT – VSWH)}	-0.3V to 7V
Control Inputs (PWM, SMOD, DISB#)	-0.3V to VCIN+0.3 V
Storage Temperature (Ts)	-40°C to +150°C
Junction Temperature (Tj)	-40°C to +150°C
Thermal Characteristics	
Package Thermal Resistance ($R_{\Theta JA}$)	50°C/W
Package Thermal Resistance ($R_{\Theta JC}$)	5°C/W

II. Package and Die Information:

Product ID	AOZ5036QI-01
Package Type	6x6QFN_40L_EP3_S
Die Size	Chip1 1040x940 $um^{2,}$ Chip2 2200x1180 $um^{2,}$ Chip3 4430x1700 $um^{2,}$
L/F material	Triple 4.65x2.62/2.3x1.77/2.62x1.72 Etch Ag 63.5 With Photo Mask Plating For Clip Without Tape
Clip Type	Plate-20 3.6 Etch Bare 18.2 For 4mil Wafer
Die attach material	84-3J epoxy and solder paste clip bond
Bond wire	Au, 1-mil
Mold Material	G770

III. Qualification Tests Requirements

- 1 lot of AOZ5036QI-01 168 hrs of HTOL. Extension from AOZ5006QI.
- 3 lots of PCT, TC and Unbiased HAST for 6X6QFN-40 package release.

IV. Qualification Tests Result

Test Item	Test Condition	Sample Size	Result	Comment
HTOL	**Per JESD 22-A108-B V_{IN}=12V . VCIN=5.5V Tj = 125 ^{0}C**	**1 lot (80 /lot)**	**pass**	**1 AOZ5036QI-01 lot (BA007), 80 units passed HTOL 168 hrs test.**
ESD (HBM, MM, CDM)	**Per JESD 22-A114E, JESD 22-A115A**	**3 units each mode**	**pass**	**3 units (BA006) AOZ5036QI-01 passed 2KV HBM, 3 units (BA006) AOZ5036QI-01 passed 200V MM, 3 units (BA006) AOZ5036QI-01 passed 1KV CDM.**
Latch-up	**Per JESD 78A**	**3 units**	**pass**	**3 units (BA006) AOZ5036QI-01 passed latch-up test.**
Power Cycling	**25C, Vin=15V, Output=1.0V, Load=35A(resistor),EN cycle 0-4.7V, 48hours, cycle times>100K**	**24 units**	**pass**	**8 units (BA005) AOZ5036QI-01, 8 units (BA006) AOZ5036QI-01 and 8 units (BA007) AOZ5036QI-01 passed on bench and post ATE testing.**
6x6QFN_40L_EP3_S package qual data				
Pre-Conditioning	**Per JESD 22-A113 85C ^{0}/85%RH, 3-cycle reflow@260 ^{0}C**	**3 lots (82 /lot)**	**pass**	**3 AOZ5036QI-01 lots (BA005,BA006, BA007), 246 units passed preconditioning.**

HAST	**130 +/- 2 ^{0}C, 85%RH, 33.3 psi, at VCC min power dissipation**	**3 lots (80 /lot)**	**pass**	**3 AOZ5036QI-01 lots (BA005,BA006, BA007), 240 units passed 100 hrs HAST.**
Temperature Cycle	**-65 ^{0}C to +150 ^{0}C, air to air (2cyc/hr)**	**3 lots (82 /lot)**	**pass**	**3 AOZ5036QI-01 lots (BA005,BA006, BA007), 246 units passed 500 temperature cycles.**
Pressure Pot	**121 ^{0}C, 15+/-1 PSIG, RH= 100%**	**3 lots (82 /lot)**	**pass**	**3 AOZ5036QI-01 lots (BA005,BA006, BA007), 246 units passed 96 hrs PCT.**

V. Reliability Evaluation

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size of the product. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

FIT rate (per billion): 23
MTTF = 4884 years

The failure rate (λ) is calculated as follows:

$\lambda = (\chi^2[CL,(2f+2)]/2) \times (1/SS \times t \times AF)$ ……..[eqn 1] where CL = % of confidence level
f = number of failure
SS = sample size
t = stress time

Looking up the $\chi^2/2$ table for zero failure (in HTOL) with 60% confidence, the value of $(\chi^2[CL,(2f+2)]/2)$ is 0.92.

The Acceleration Factor (AF) is calculated from the following formula:

$AF = \exp\{(E_a/k) \times [1/T_0 - 1/T_s]\}$ where E_a = activation energy
k = Boltzman constant
T_0 = operating T_J
T_s = stress T_J

Taking the result of HTOL with SS (Total of 2 lots AOZ1950DI) = 120 and t = 500hr. and assuming under typical operating environment, T_0 = 55°C; E_a = 0.7eV and T_s = 140°C

$AF = \exp\{(0.7/8.617 \times 10^{-5}) \times [1/(273+55) - 1/(273+140)]\} = 164$

Substituting the values in equation 1, we have

$\lambda = 0.92 \times \{1/((240 \times 1000) \times 164)\} = 2.337E\text{-}8\ hr^{-1}$ or 23 FIT [MTTF = (1/ λ) million hrs.]

The calculation shows that under typical operating environment, the device failure rate is less than 23 FIT or an MTTF of over 42.8e06 hours.

The qualification test results confirm that AOZ5036QI-01 passed AOS quality and reliability requirements for product manufacturing release.