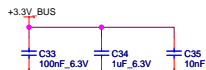


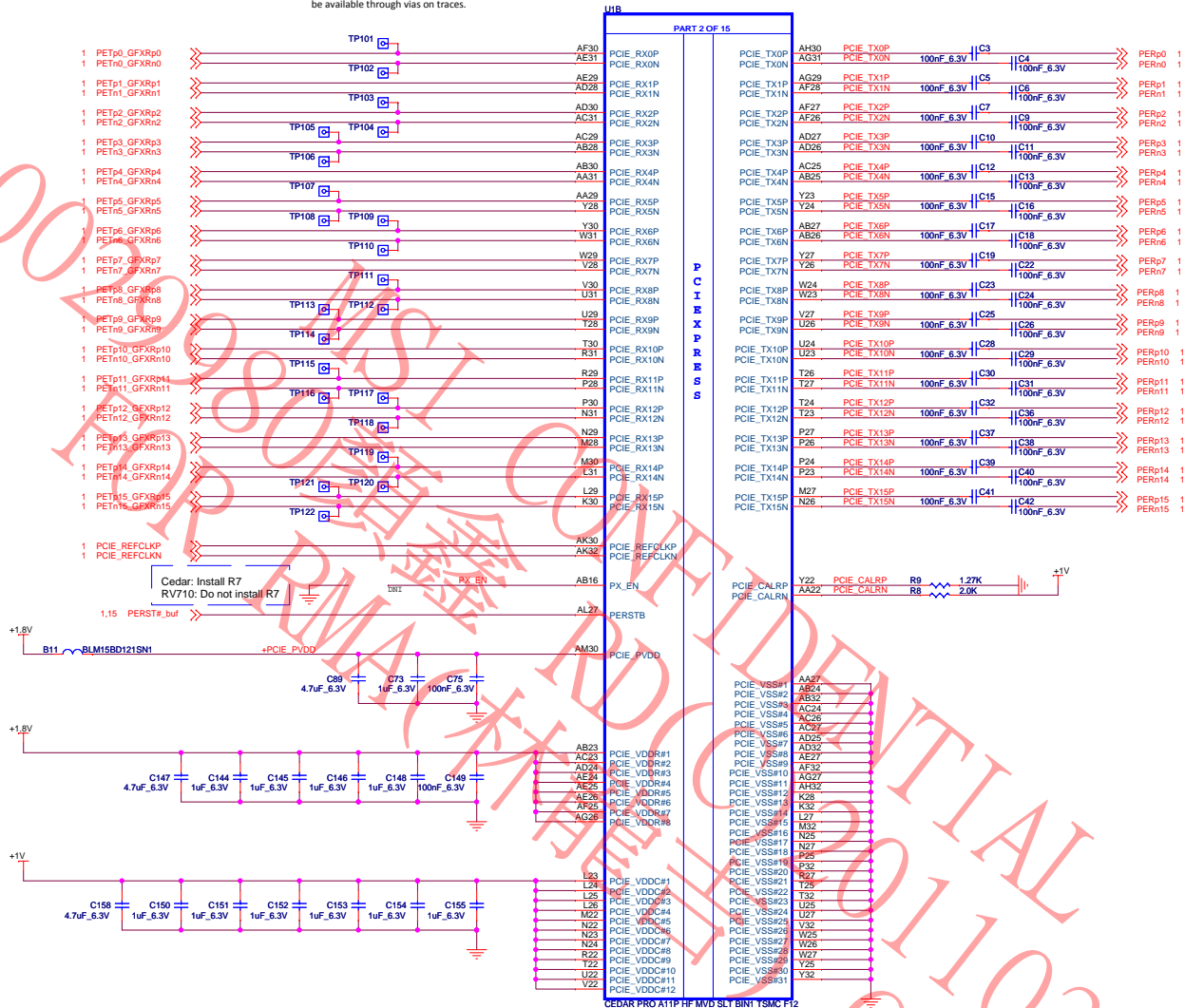
CEDAR SS



| | | | | |
|----------------------------------------------|--------------------------------------------|--------|----|---------------|
| from use of the information included herein. | | 1 | or | 15 |
| Title | Cedar DDR3 1GB 1pcs 128Mx16 VGAH HDMI dVId | Pc No. | | 102-C26701-00 |


CEDAR PCIe Interface

NOTE: Some of the PCIE testpoints will be available through vias on traces.



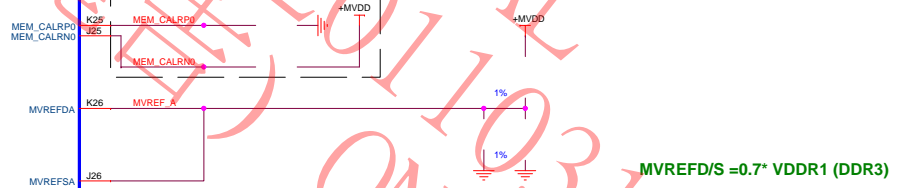
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| Sheet 2 of 18 | | | |

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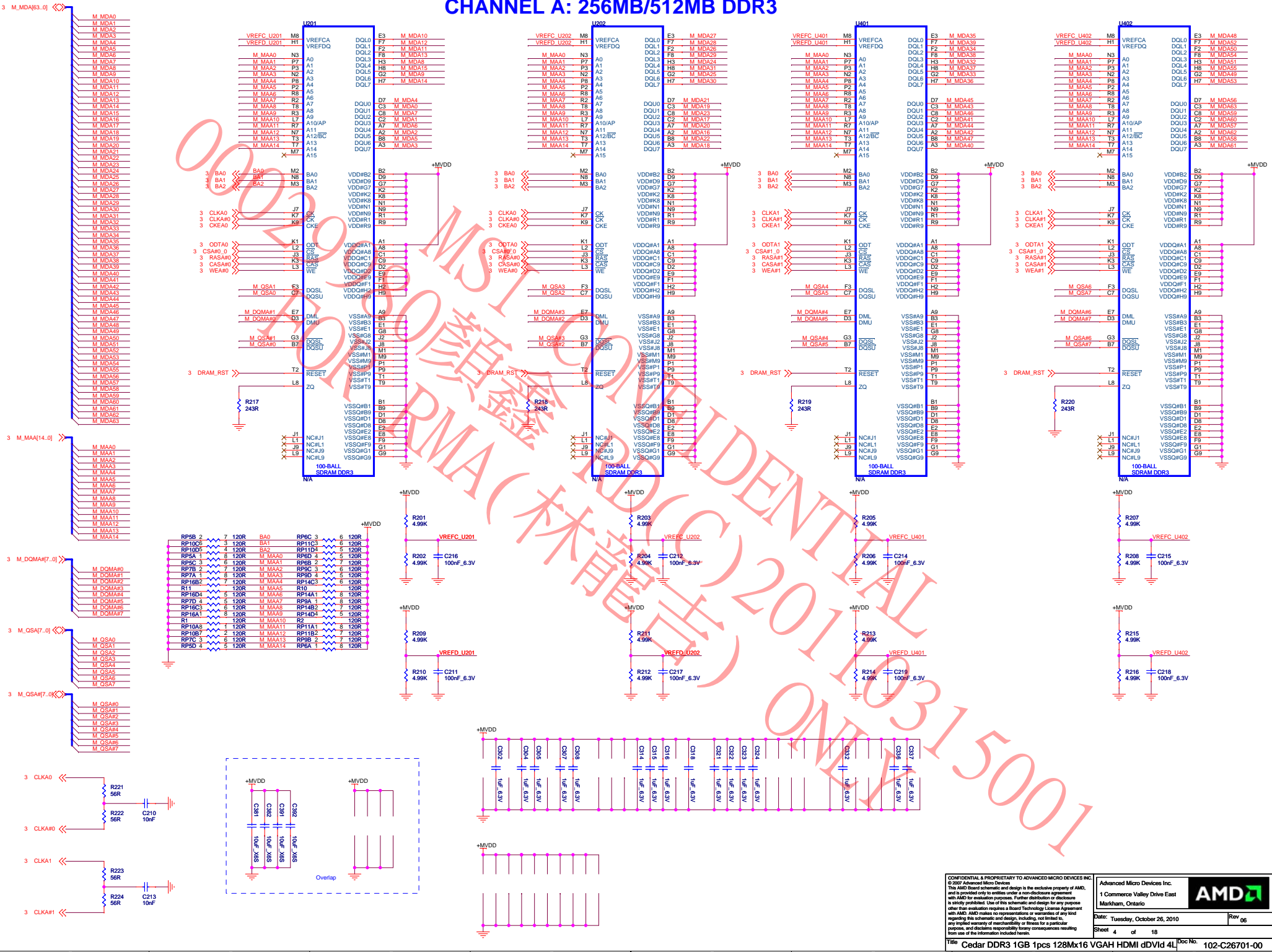
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| Sheet 3 of 18 | |

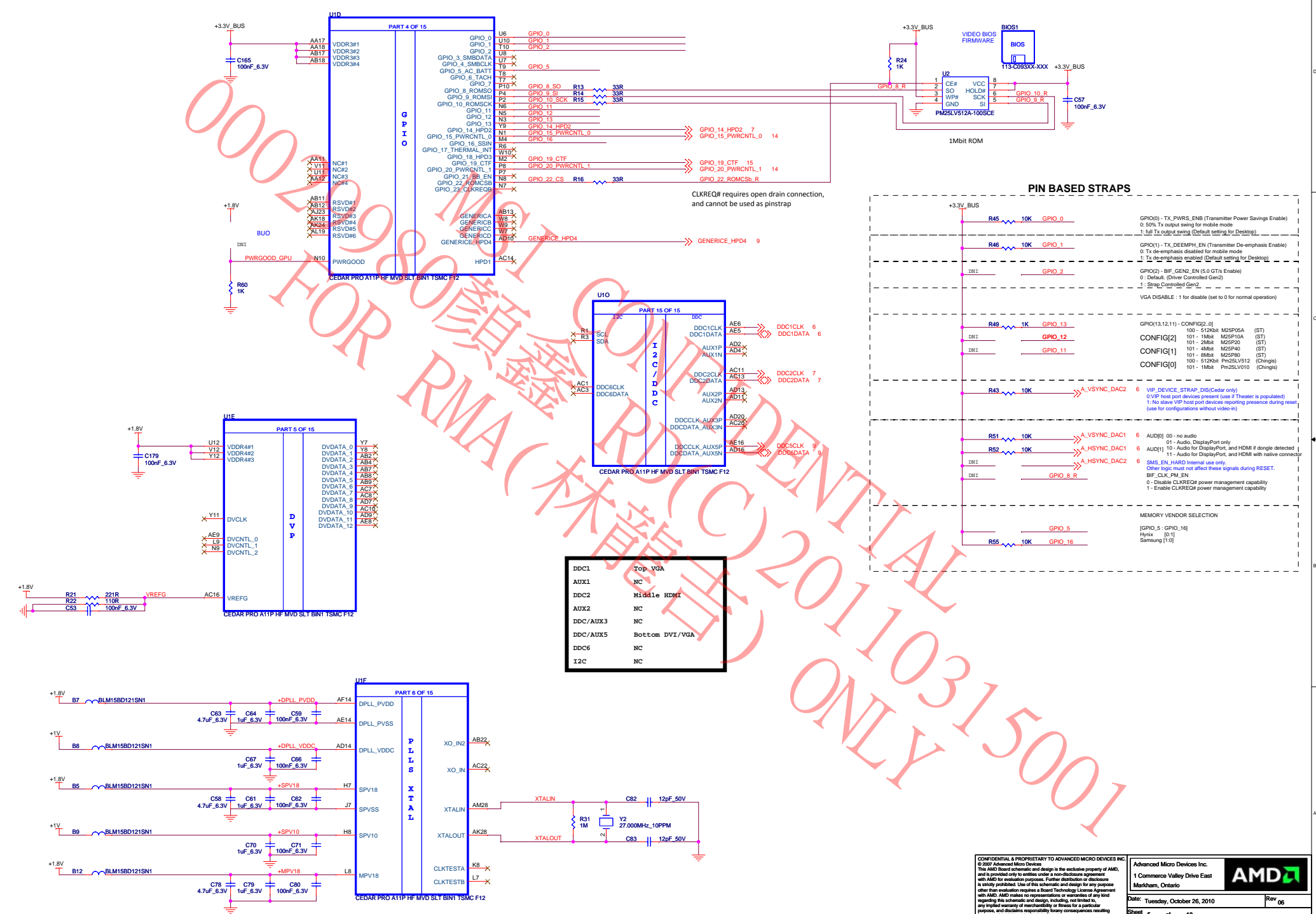
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|-------|-------------------------------------------------|---------|---------------|
| Title | Cedar DDR3 1GB 1pcs 128Mx16 VGAH HDMI dDVI d 4L | Doc No. | 102-C26701-00 |
|-------|-------------------------------------------------|---------|---------------|

CHANNEL A: 256MB/512MB DDR3

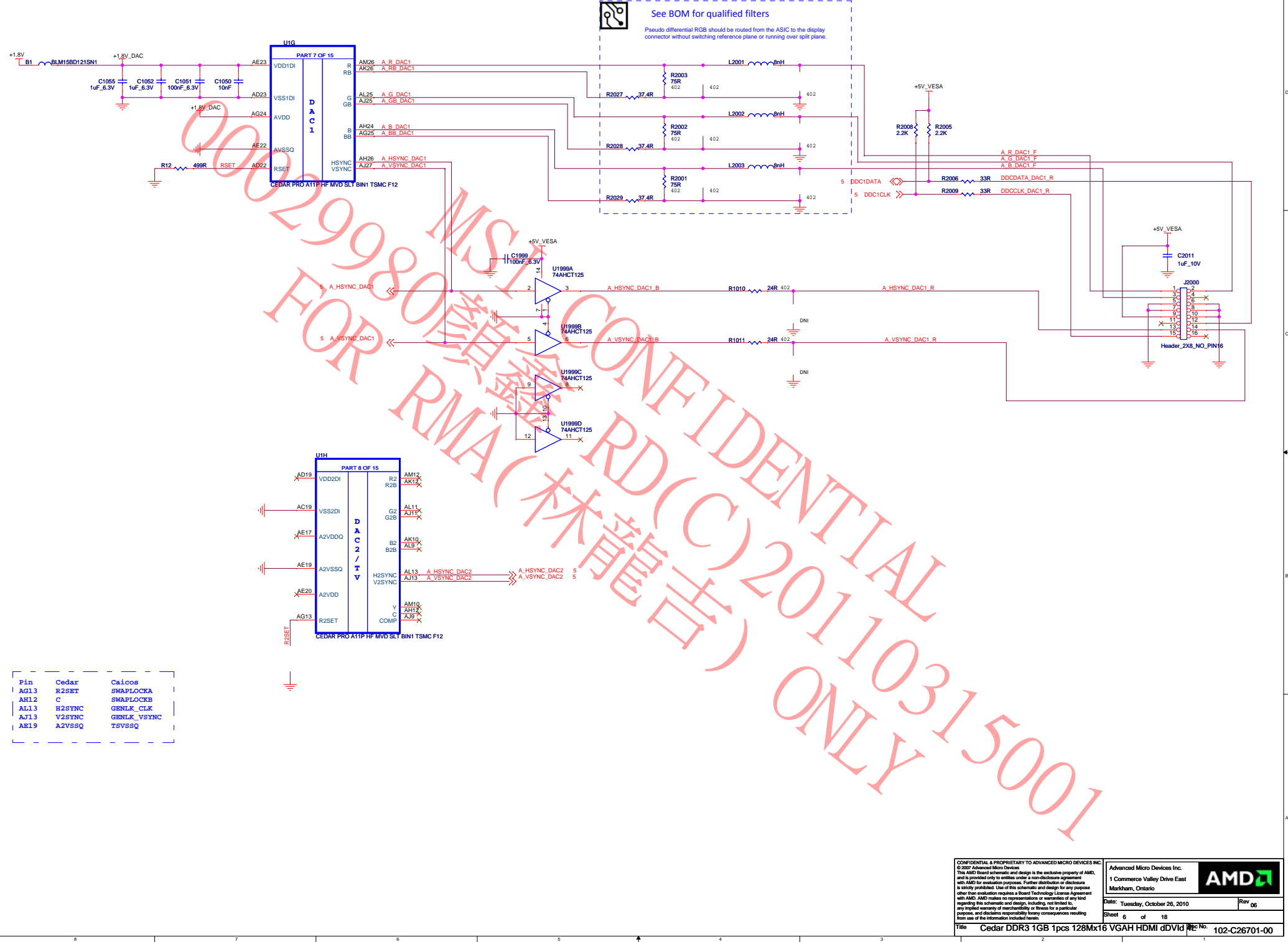


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| <p>Title Cedar D383 1GB 1ops 128MBx16 VGAH HDMI dVdV4.1</p> | | <p>Doc No. 102-C26701-00</p> | | | |

CEDAR GPIOs Strap CF XTAL OSC

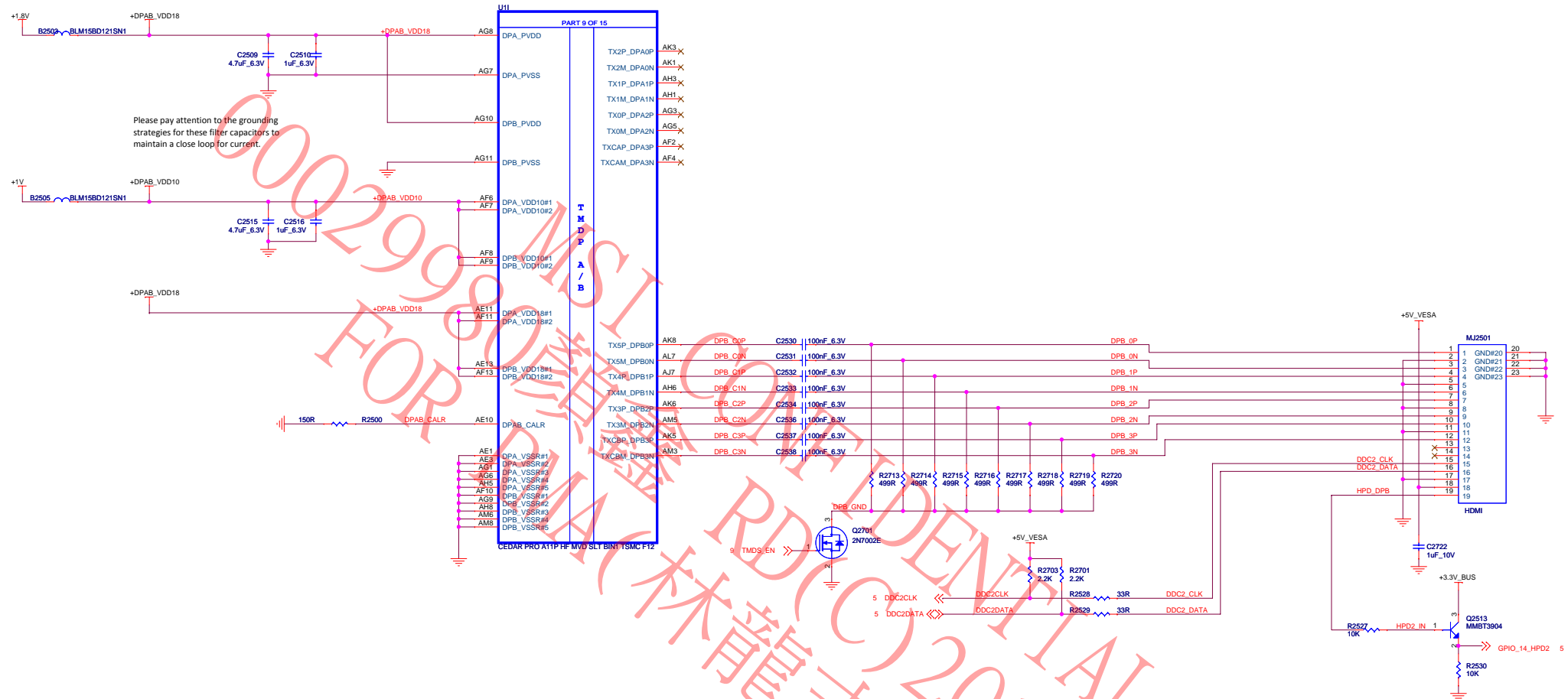



CEDAR DAC1 and DAC2



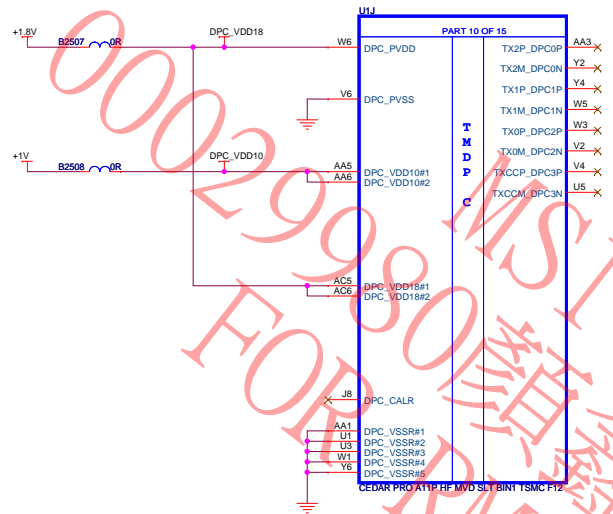
| | | |
|------|--------|-------------|
| Pin | Cedar | Caicos |
| AG13 | R2SET | SWAPLOCKA |
| AE12 | C | SWAPLOCKB |
| AL13 | H2SYNC | GENLK_CLK |
| AJ13 | V2SYNC | GENLK_VSYNC |
| AE19 | A2VSSQ | TSVSSQ |

CEDAR TMDP A&B HDMI

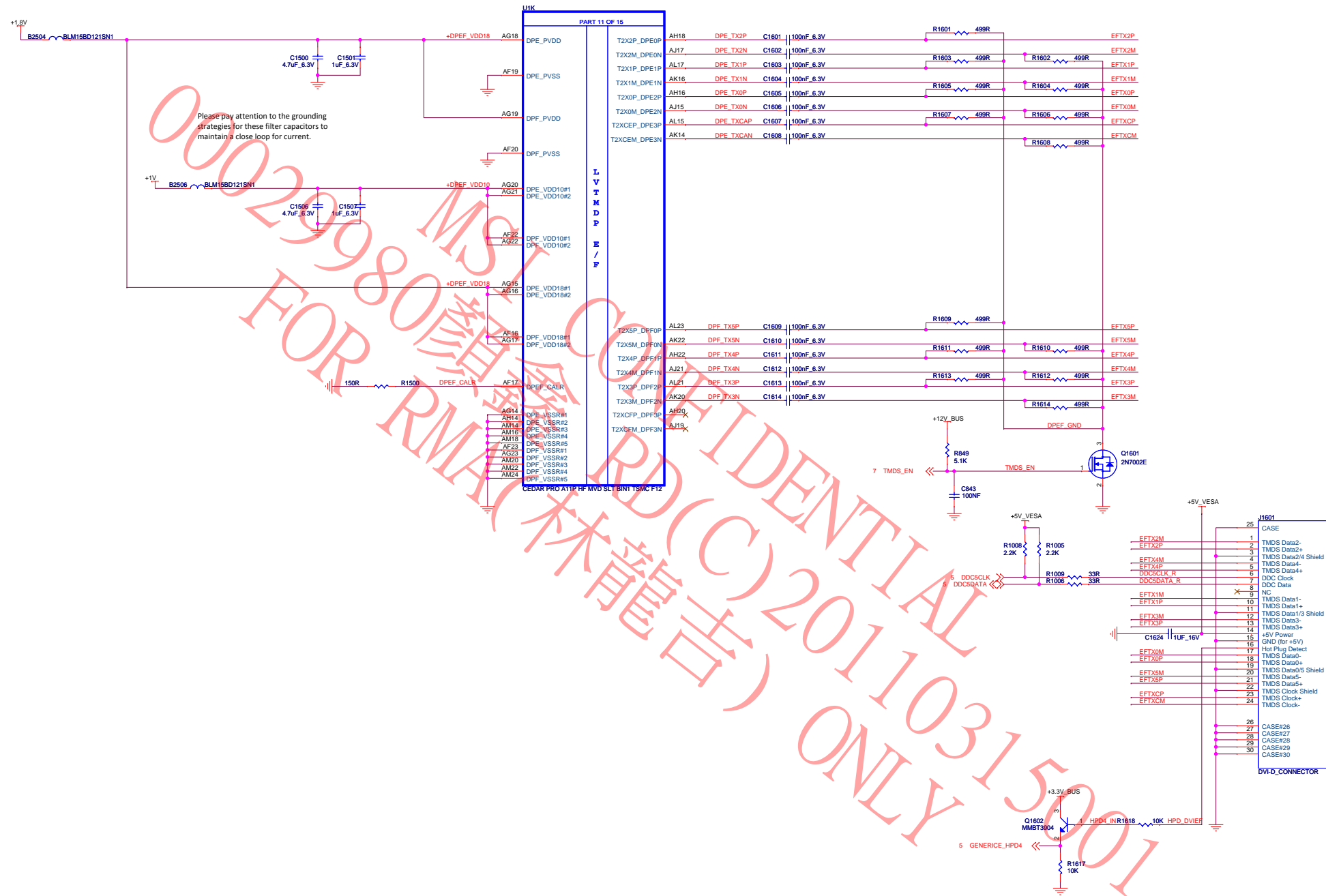


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| <p>Title Cedar DDR3 1GB 1pcs 128Mx16 VGH4 HDMI d18</p> | <p>Date: Tuesday, October 26, 2010 Sheet 7 of 18</p> |
| <p>102-C26701-00</p> | <p>Rev 06</p> |

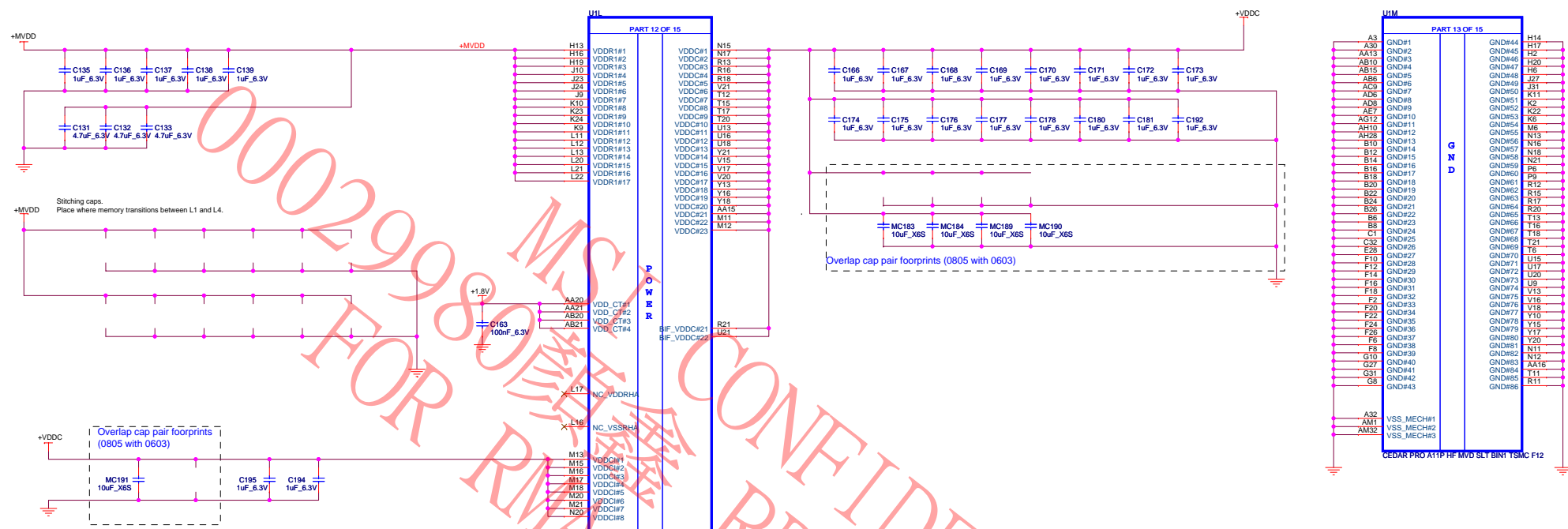
CEDAR Display Port C (Unused)

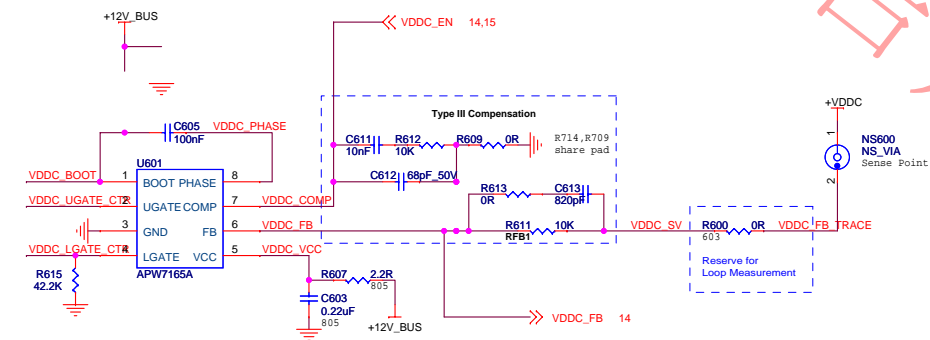
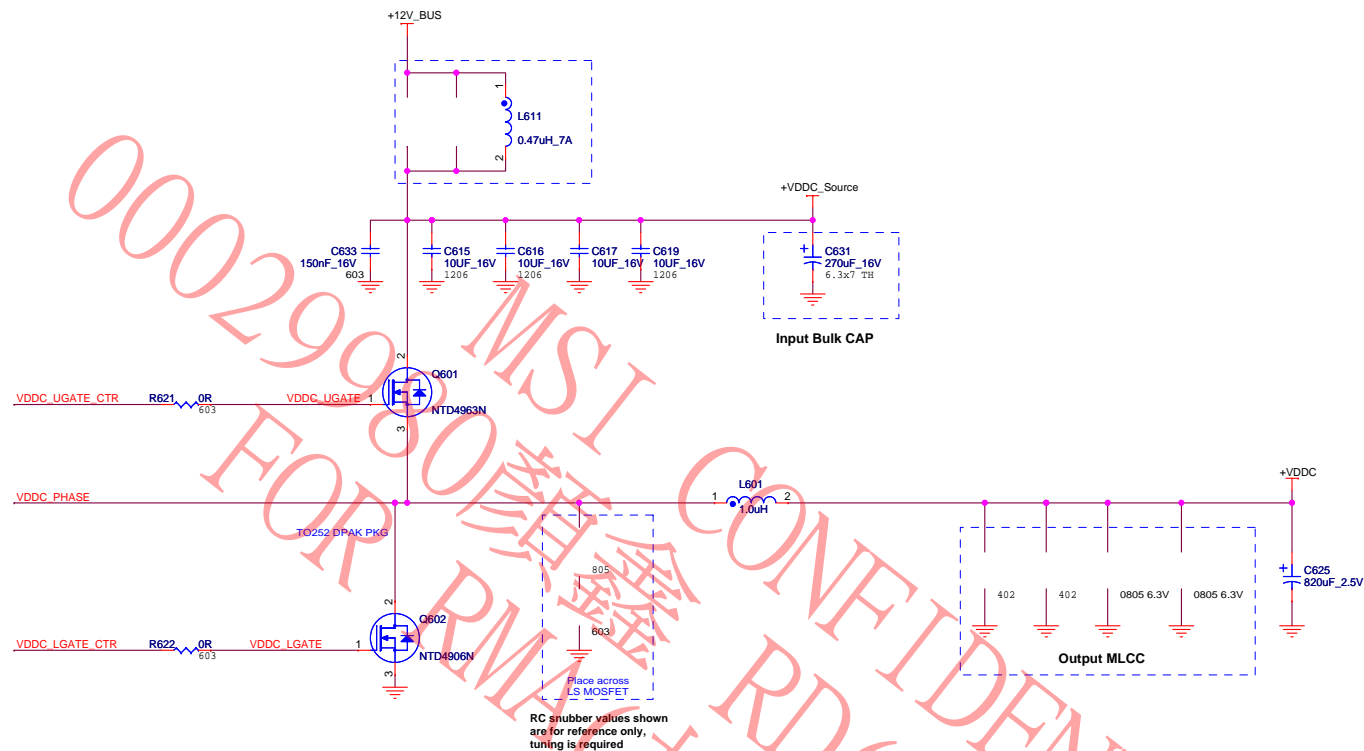


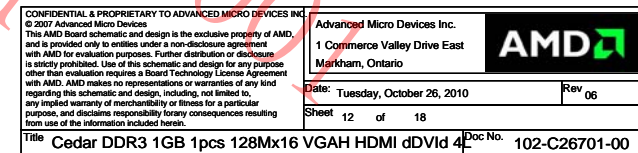
CEDAR LVTMDP E&F dDVI-I



CEDAR Power & GND



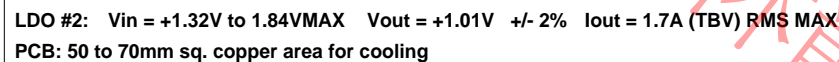




Regulators for +5V, +5V_VESA

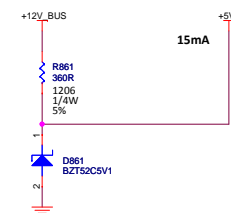
1.8V WORST-CASE REQUIREMENT

| | |
|----------------|--------------|
| Display Config | Est. Current |
| DVI+HDMI+DP | |



1.0V WORST-CASE REQUIREMENT

| | |
|----------------|--------------|
| Display Config | Est. Current |
| DVI+HDMI+DP | |



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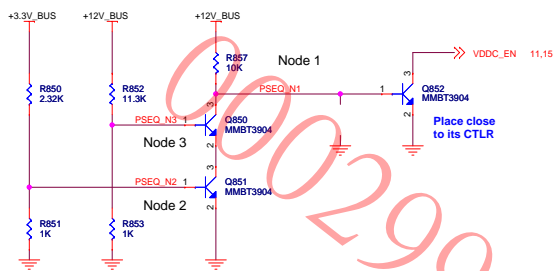
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18

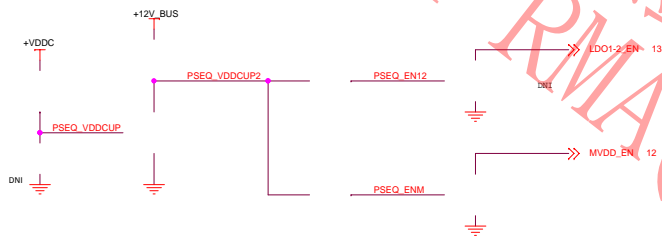
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|-------|-------------------------------------------------|---------|---------------|
| Title | Cedar DDR3 1GB 1pcs 128Mx16 VGAH HDMI dDVI d 4L | Doc No. | 102-C26701-00 |
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Power Management - Power Gating and Dynamic Voltage Control

12V_BUS & 3V3_BUS POWER SEQUENCING



POWER SEQUENCING CIRCUIT



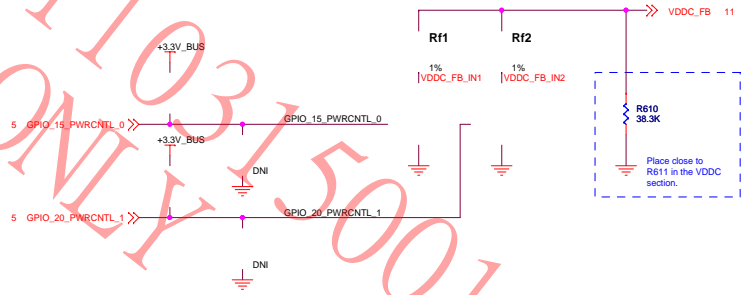
MVDD Low Side Divider

- Hi-Side Divider RFB1 is Fixed to 10K
- $V_o = V_{ref} * (1 + RFB1 / RFB2)$
- $V_{ref} = 0.8V$

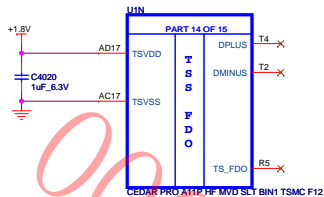


VDDC Low Side Divider

Cedar VDDC=1.0V R610=39.2K (3160392200G)
RV710 VDDC=1.1V R610=23.7K (3160237200G)



Mechanical and Thermal Management

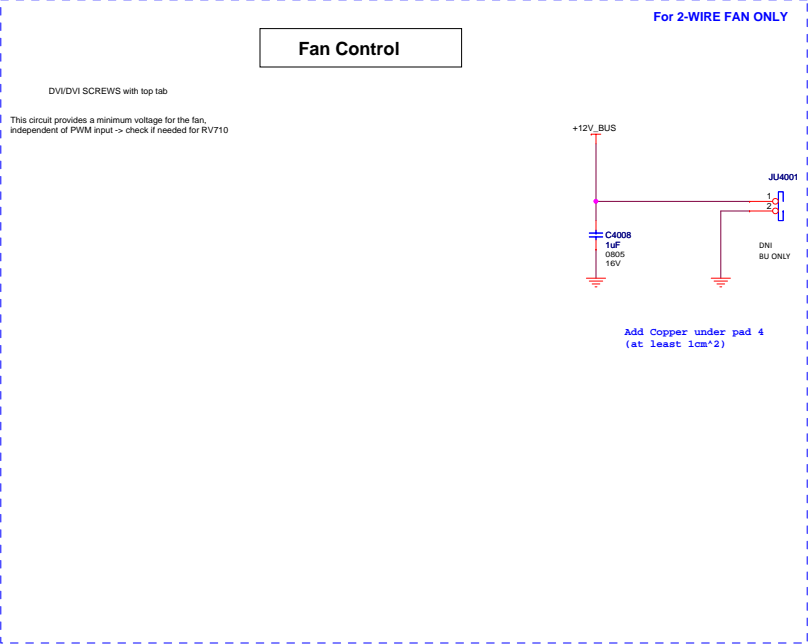
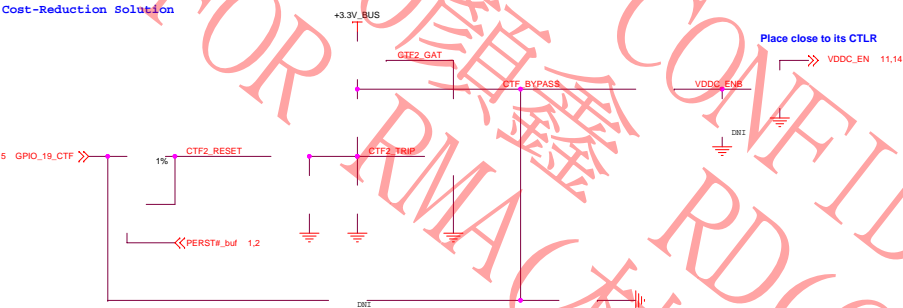


Warning: TS_FDO is not 5V tolerant, MAX sink current 1.65mA


If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.

Critical Temperature Fault

Cost-Reduction Solution



Square Fansink 12W

7120336200G

For DVI Connector

ASSY-SCREW200

SCREW JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT <3rd part field>

ASSY-SCREW201

SCREW JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT <3rd part field>

702000800G

Bracket Components

ASSY-SCREW202

SCREW SCREW

7020005200G

| SKU | P/N | CONFIGURATION | Form Factor |
|------|-------|---------------|----------------|
| | PERCH | 8020051300G | DVI + DP + VGA |
| | | | FH / SS |
| BASS | | 8020051400G | DVI +HDMI+ VGA |
| | | | FH / SS |
| | PERCH | 8020051600G | DVI + DP |
| | | | LP / SS |
| BASS | | 80200516A0G | DVI +HDMI |
| | | | LP / SS |
| | PERCH | 8020051700G | DVI + DP + VGA |
| | | | FH / DS |
| BASS | | 80200517A0G | DVI +HDMI+ VGA |
| | | | FH / DS |

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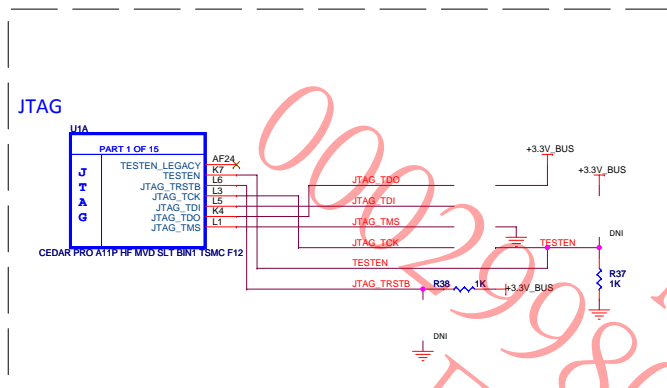
Date: Tuesday, October 26, 2010

Rev: 06

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Doc No: 102-C26701-00

(19) Debug Circuits



LM96163 FOR BACKUP THERMAL CONTROL

LED RED "ON" shows Fault



SCL/SDA PORT DEBUG ACCESS

Place connector on the back side
(easily accessible and not blocked by the heatsink).

SWITCH CONNECTIONS TO PINSTRAPS

```
GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0: Default. (Driver Controlled Gen2)
1: Default Controlled Gen2
```

I2C VDDDC Control

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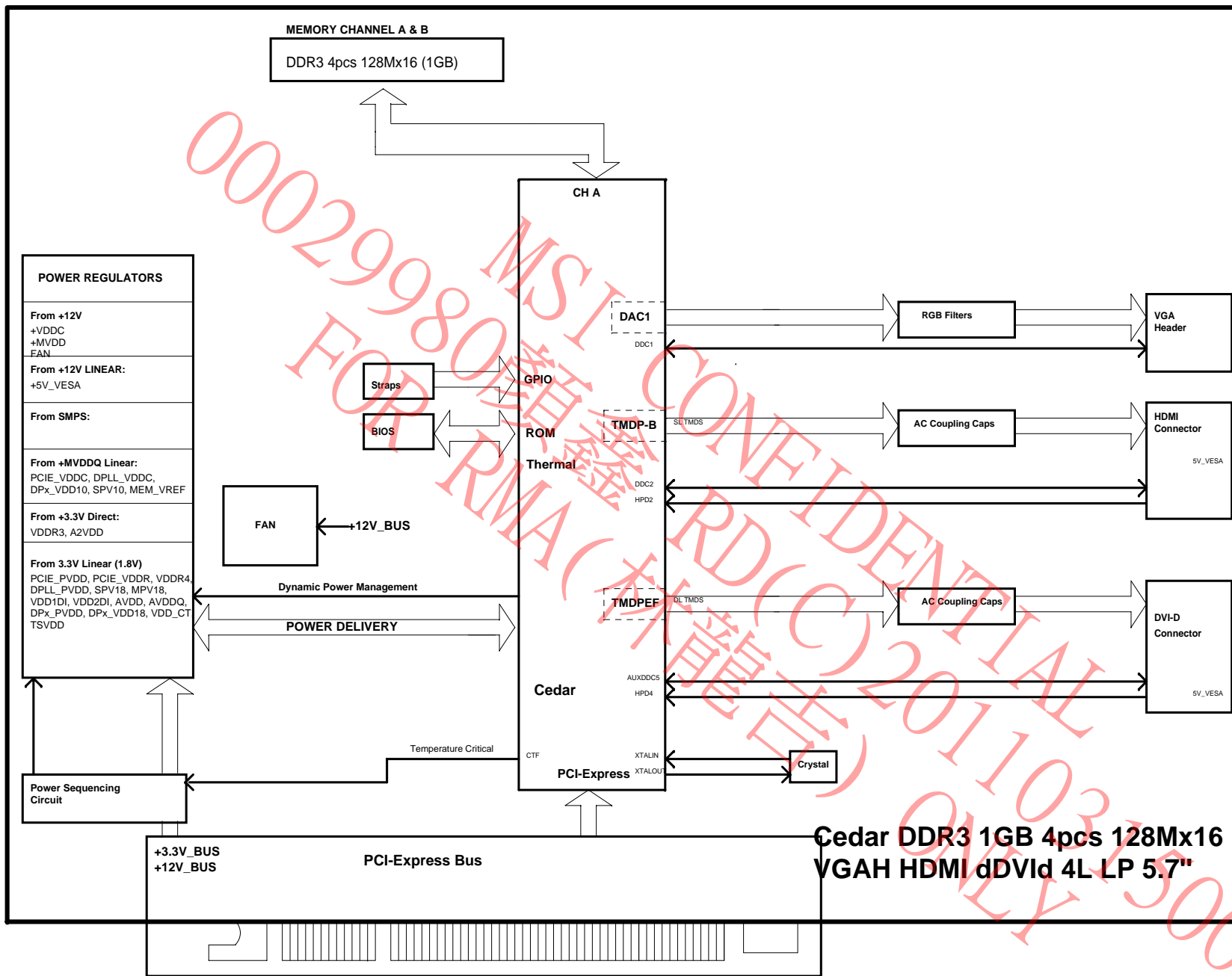
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| 4L | Doc No. | 102-C26701-00 |
|----|---------|---------------|

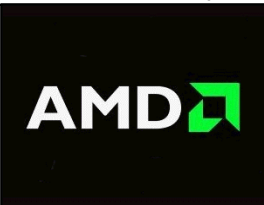
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| Title | Cedar DDR3 1GB 1pcs 128Mx16 VGAH HDMI dDVI d 4L | Doc No. | 102-C26701-00 |
|-------|-------------------------------------------------|---------|---------------|

| | | | |
|-------|-------------------------------------------------|---------|---------------|
| Title | Cedar DDR3 1GB 1pcs 128Mx16 VGAH HDMI dDVI d 4L | Doc No. | 102-C26701-00 |
|-------|-------------------------------------------------|---------|---------------|



Cedar DDR3 1GB 4pcs 128Mx16
VGAH HDMI dDVI d 4L LP 5.7"





Title
Cedar DDR3 1GB 1pcs 128Mx16 VGAH HDMI dDVI d 4L

Schematic No.
102-C26701-00

Date:
Tuesday, October 26, 2010

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
 For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
 Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 06

| Sch Rev | PCB Rev | Date | REVISION DESCRIPTION |
|---------|---------|------------|----------------------------------------|
| 00 | 00A | 2009/11/23 | Initial Cedar schematic, based on C093 |
| | | | |
| | | | |
| | | | |
| | | | |

A large, diagonal, semi-transparent red watermark is overlaid across the entire page. The watermark text is arranged in a line following the diagonal and includes the following elements: the number '00029980', the company name 'MSI', the name '盧金鑫' (Lu Jinxin), the word 'CONFIDENTIAL', the phrase 'FOR RMA (林龍吉)' (for RMA (Lin Longji)), the initials 'RD (C)', the date '20110315', and the number '0001'. The watermark is oriented from the bottom-left towards the top-right.