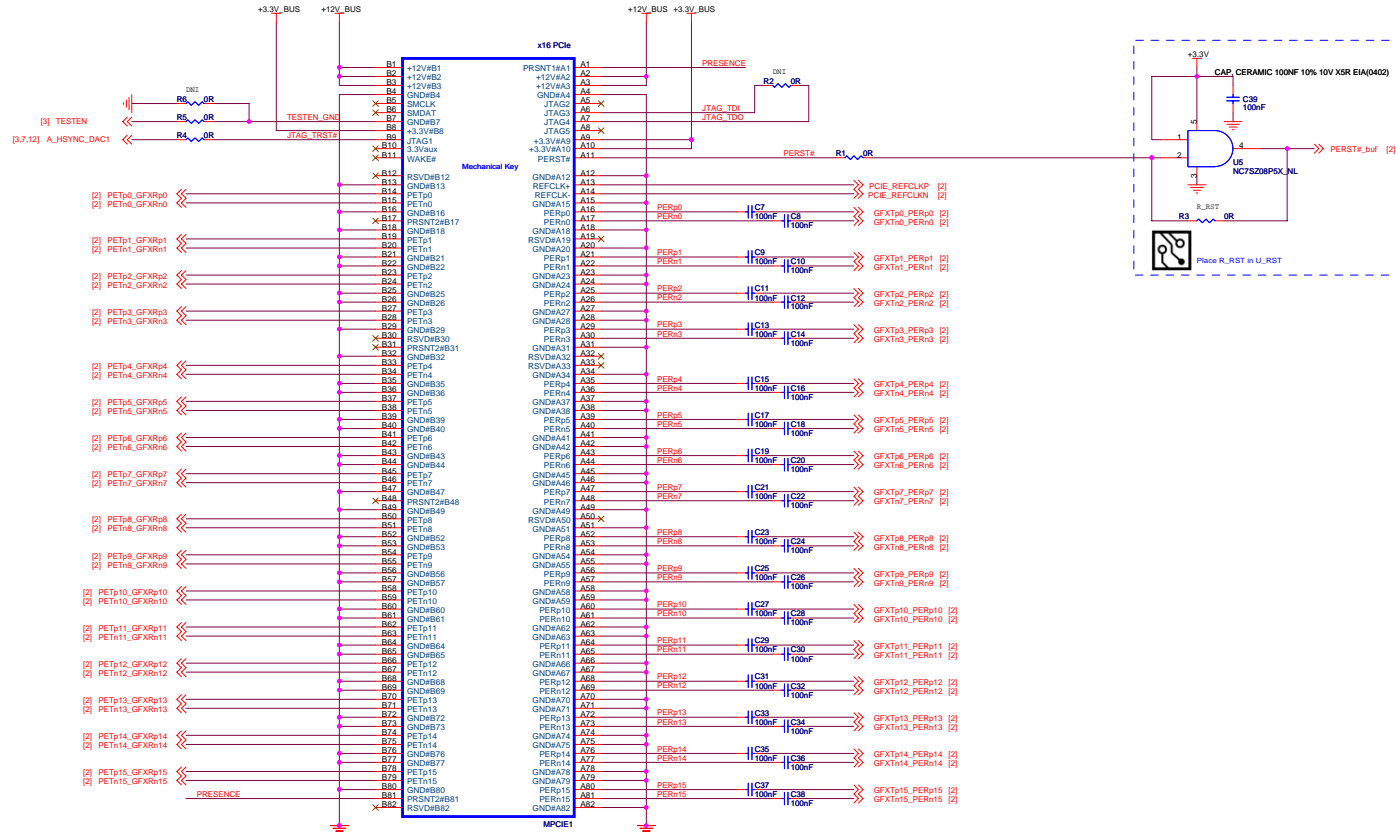
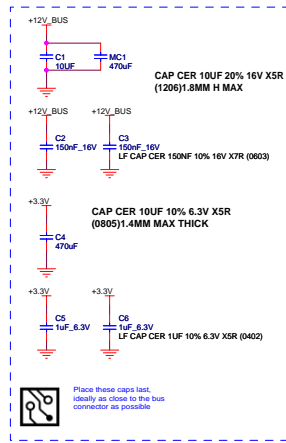


# PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND



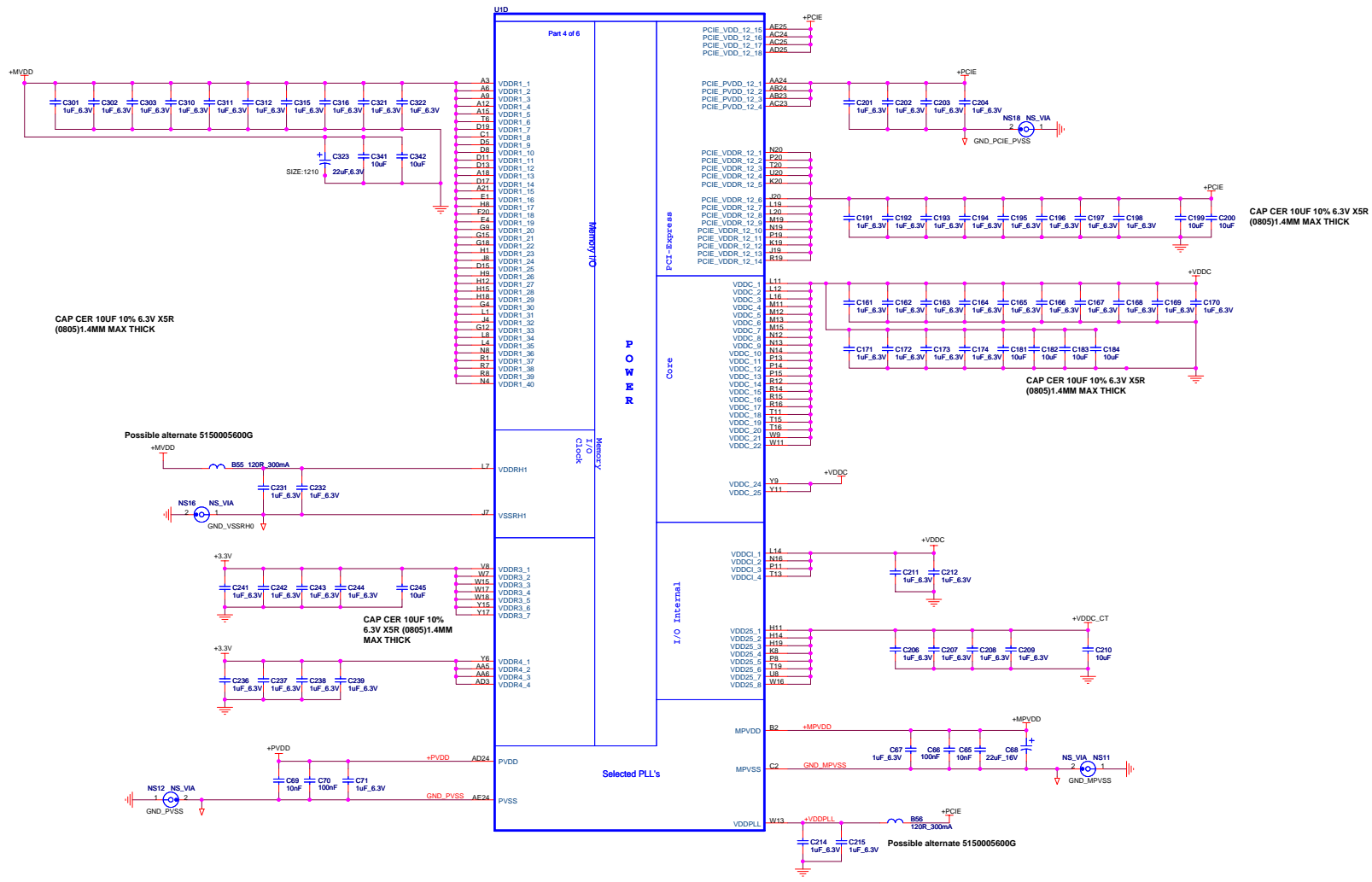
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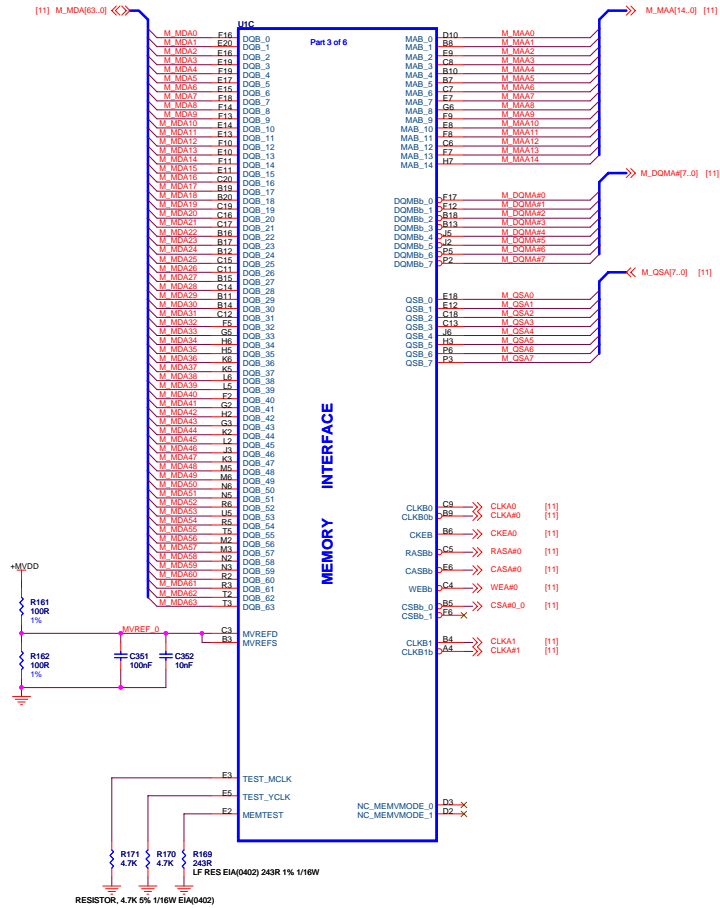
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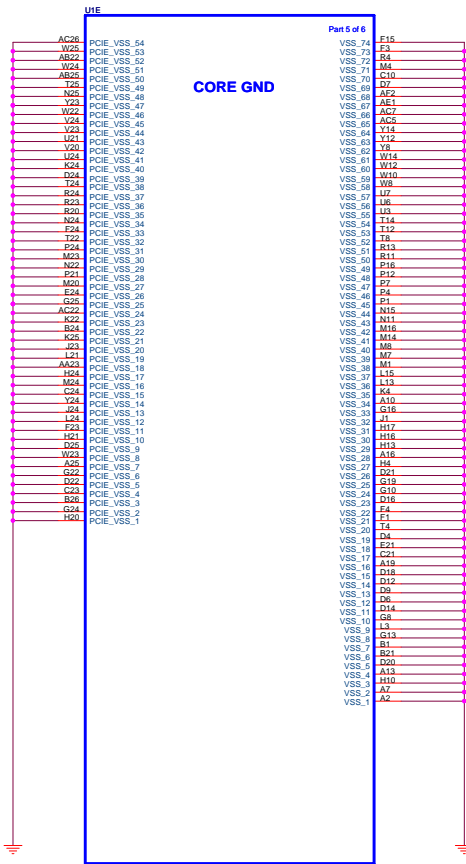
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## Channel A

Register control is from Registers named CHANNEL B although this ASIC package only has 1 channel





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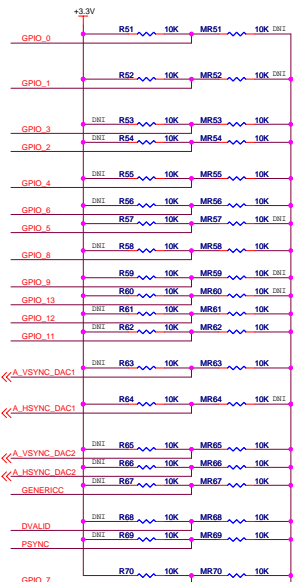
Title RH RV505CE 256MB DDR2 LP 4L

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# PIN BASED STRAPS

[1,12] A\_VSYNC\_DAC1  
[1,12] A\_HSYNC\_DAC1  
[3] A\_VSYNC\_DAC2  
[3] A\_HSYNC\_DAC2  
DVALID  
PSYNC  
GPIO\_7



GPIO(0) - TX\_PWRS\_ENB (Transmitter Power Savings Enable) PCI FEATURE I  
0: 50% Tx output swing for mobile mode  
1: Full Tx output swing (Default setting for Desktop)

GPIO(1) - TX\_DEEMPH\_EN (Transmitter De-emphasis Enable) PCI FEATURE II  
0: Tx de-emphasis disabled for mobile mode  
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - Miscellaneous PCI-Express Modes  
00: Halt impedance calibration before transmitter is enabled and enable receiver detection (Default setting for Desktop)  
01: Allow impedance calibration to continue on in the background AFTER transmitter has been enabled and enable receive detection.  
10: Bypass common-mode detection & receiver detection and halt impedance calibration before TX\_EN.  
11: Short-circuit internal loopback and halt impedance calibration before TX\_EN and enable receiver detection.

GPIO(4) - DEBUG\_ACCESS: 0 for normal operation, 1 for debug mode

GPIO(5) - PLL\_BIAS\_RD (Reduced mirror bias setting for PHY PLL) PCI FEATURE III  
Provide 4 different BIAS settings - Set to 00 for R520

GPIO(8) - FORCE\_COMPLIANCE: 0 for Normal operation, 1 for Force into Compliance Mode

GPIO(9,13,11) - ROMIDCFQ3\_0  
1001 - 1M AT25P1024 ROM (Atmel)  
1010 - 1M AT45DB01 ROM (Atmel)  
1011 - 1M M25P10 ROM (ST)  
1100 - 512K M25P10 ROM (ST) (ATI default)  
1101 - 1M S5745F010 ROM (SST), 1M W45B512 ROM (Winbond), 512K W45B012 ROM (Winbond)  
1110 - 1M S5745F010 ROM (SST), 512K S5720P512 ROM (SST)  
1111 - 1M NQ25F01B ROM (NexFlash)

VSYNC - VIP\_DEVICE  
0: Slave VIP host port devices present (use if Theater is populated)  
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - DINGRD ATI Feature I  
This straps allow a Workstation bonded part to be downgraded to a normal part on a board. This allow inventory management to better balance demand.  
0: Device remains a Workstation grade part  
1: Part is downgraded to a Normal part

HSYNCR V2SYNCR GENERICC - Star Memory System repair mod ATI Feature II  
000 - Default

MEMORY CONFIG ATI Board Feature I  
DVALID: 0 = 4 bank memory, 1 = 8 bank memory  
PSYNC: 0 = 1 rank of memory, 1 = 2 ranks of memory

TV OUT STANDARD (Jumper position overwrite resistor settings) ATI Board Feature II  
0: PAL TVO (Jumper position 2-3)  
1: NTSC TVO (Jumper position 1-2)

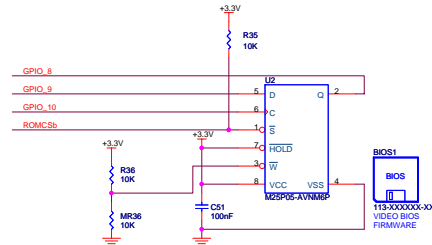


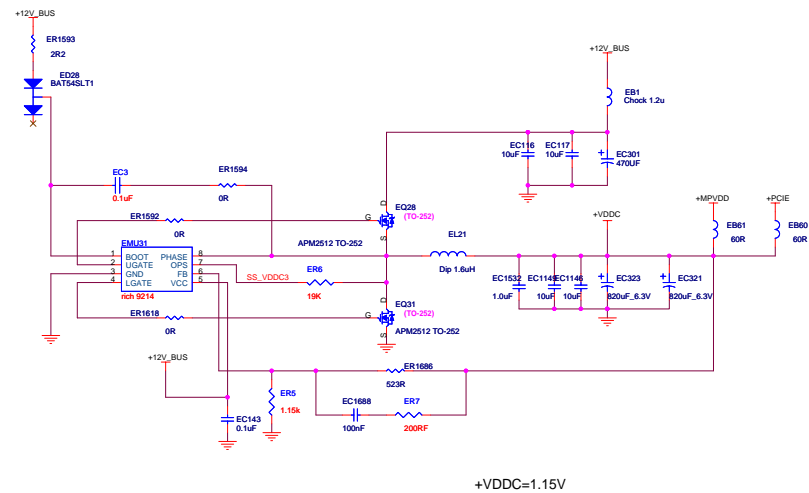
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GPIO	PN STRAP	ALTERNATE USE
GPIO_0	YES	VIOB_0 (OUTPUT)
GPIO_1	YES	VIOB_1 (OUTPUT)
GPIO_2	YES	VIOB_2 (OUTPUT)
GPIO_3	YES	VIOB_3 (OUTPUT)
GPIO_4	YES	VIOB_4 (OUTPUT)
GPIO_5	YES	VIOB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAINTSTRV (INPUT)
GPIO_8	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_9	YES	TESTOUT(8) (OUTPUT)
GPIO_10	NO	TESTOUT(9) (OUTPUT)
GPIO_11	YES	TESTOUT(10) (OUTPUT)
GPIO_12	YES	TESTOUT(11) (OUTPUT)
GPIO_13	YES	WPO_DVIT (INPUT)
GPIO_14	NO	VIDA8B (OUTPUT)
GPIO_15	NO	12VEXT_DETECT (INPUT)
GPIO_16	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)
GPIO_17	NO	

DEBUG BUS  
No testpoint means the net can be accessed from a pad somewhere else





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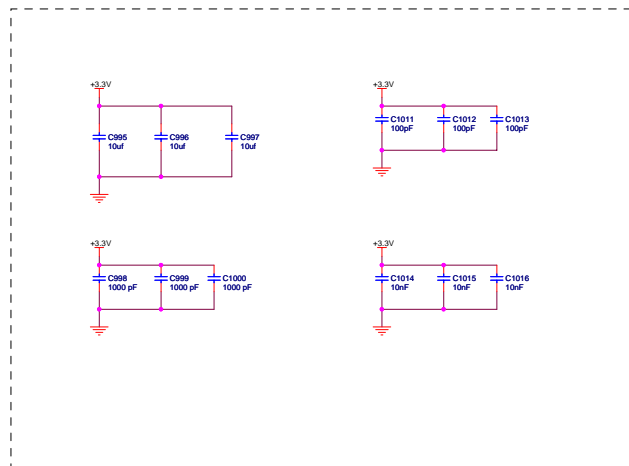
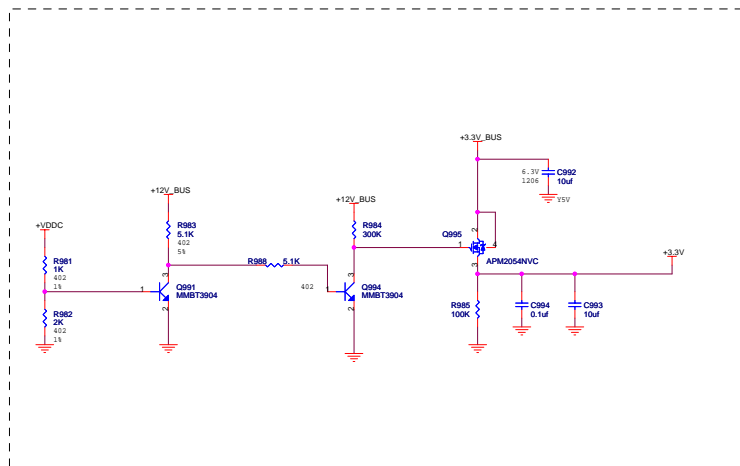
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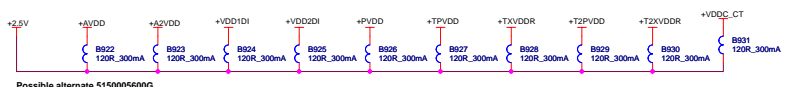
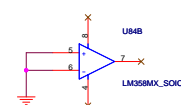
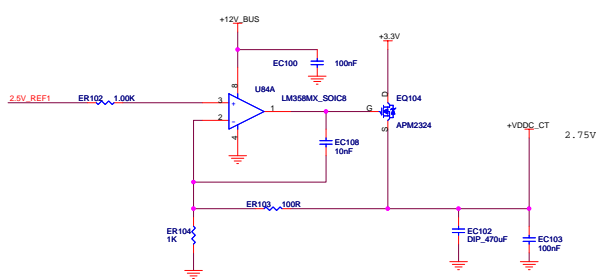
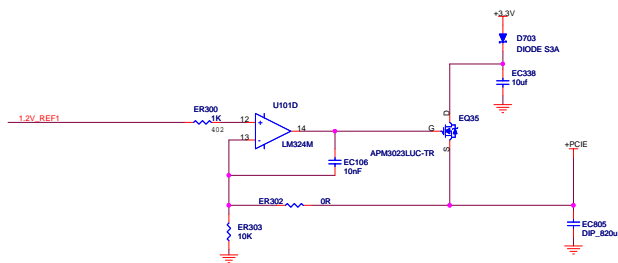
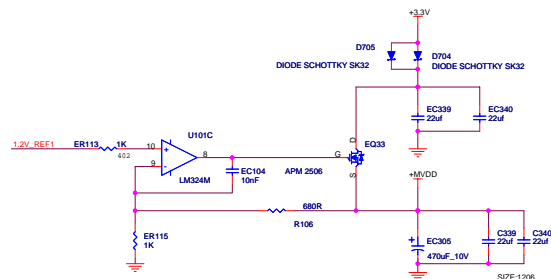
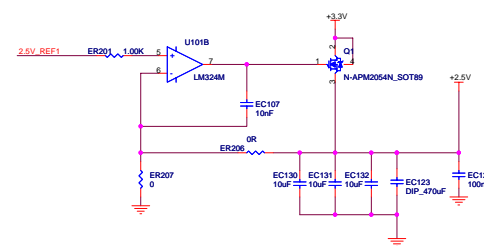
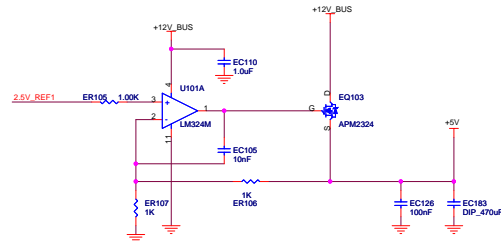
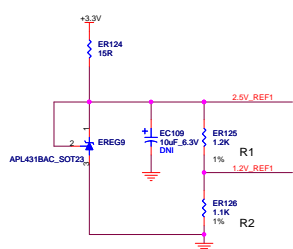


sequence



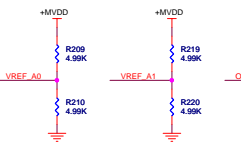
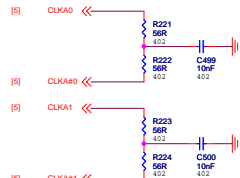
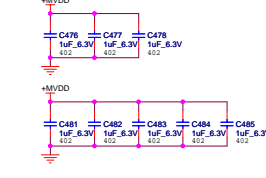
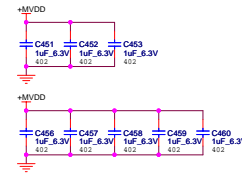
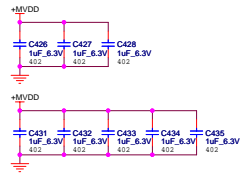
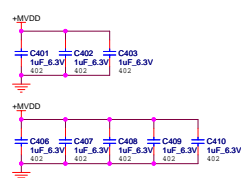
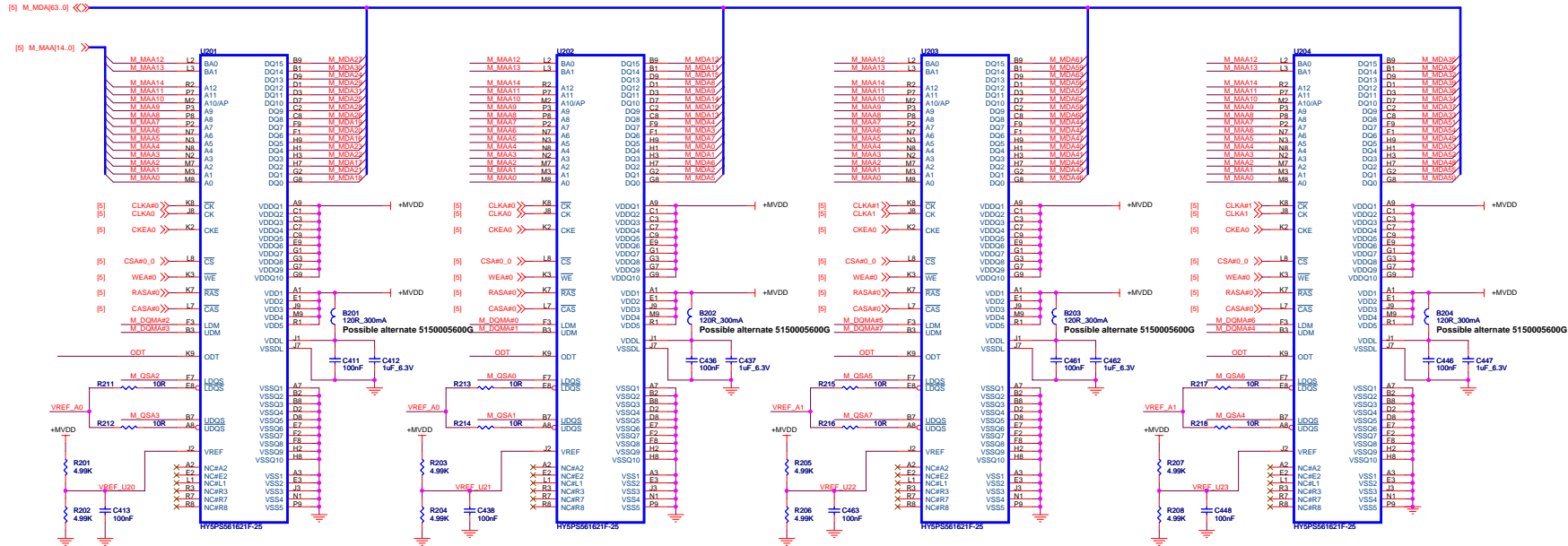
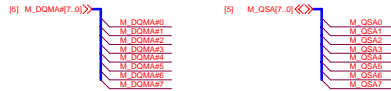
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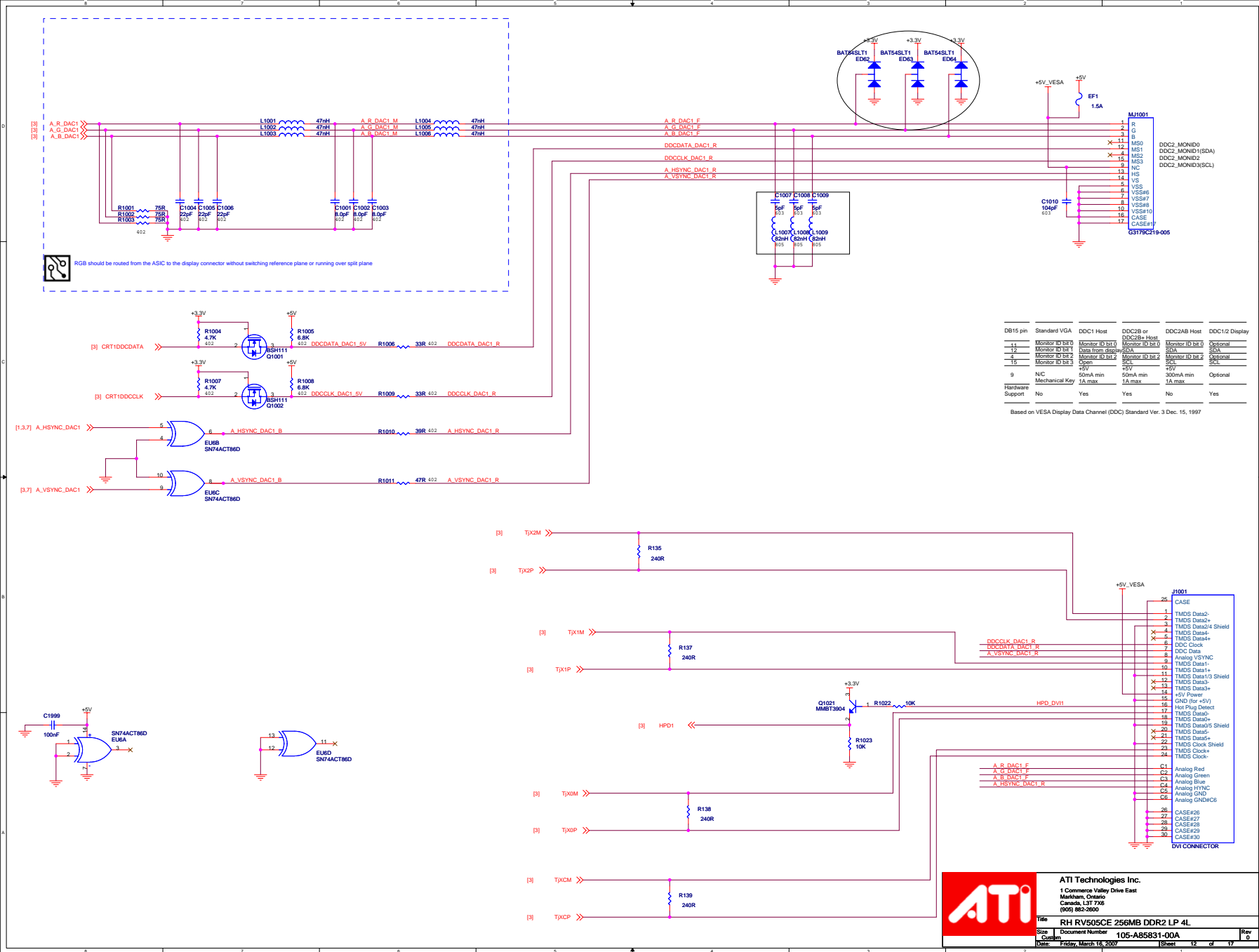
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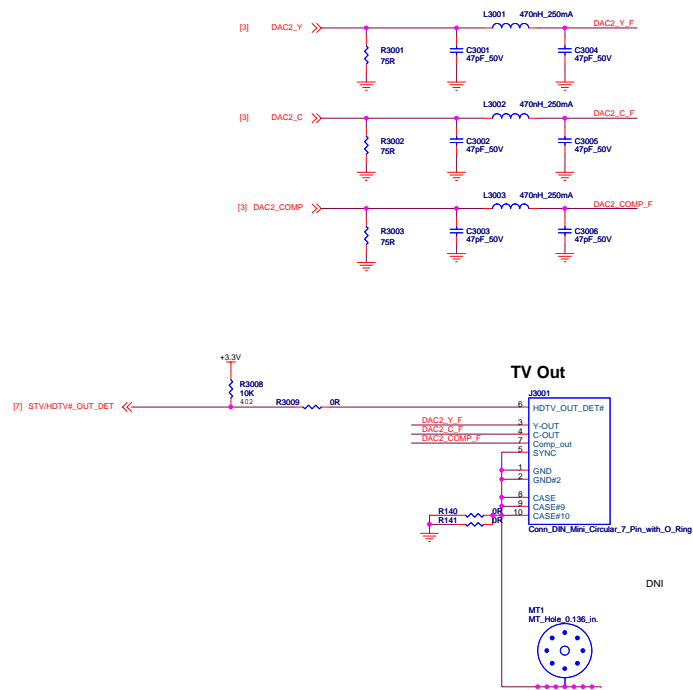
# CHANNEL A: RANK 0 128MB DDR2



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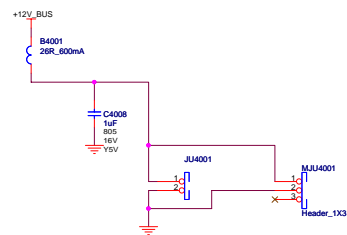
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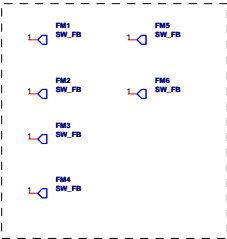
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DIVVGA SCREWS

ASSY-SCREW1  
SCREW  
JACKSCREW  
ASSY  
7000000800

ASSY-SCREW2  
SCREW  
JACKSCREW  
ASSY  
7000000800



DNI



PCB DESIGN NOTE:

- ASIC REQUIREMENTS  
FOR THIS SOCKET:
1. USE ALTERNATE ASIC DECAL  
WITH SQUARE VIA PADS.
  2. SOCKET & ASIC PADS  
REQUIRED GOLD PLATING.  
SEE SPEC. FOR DETAILS.



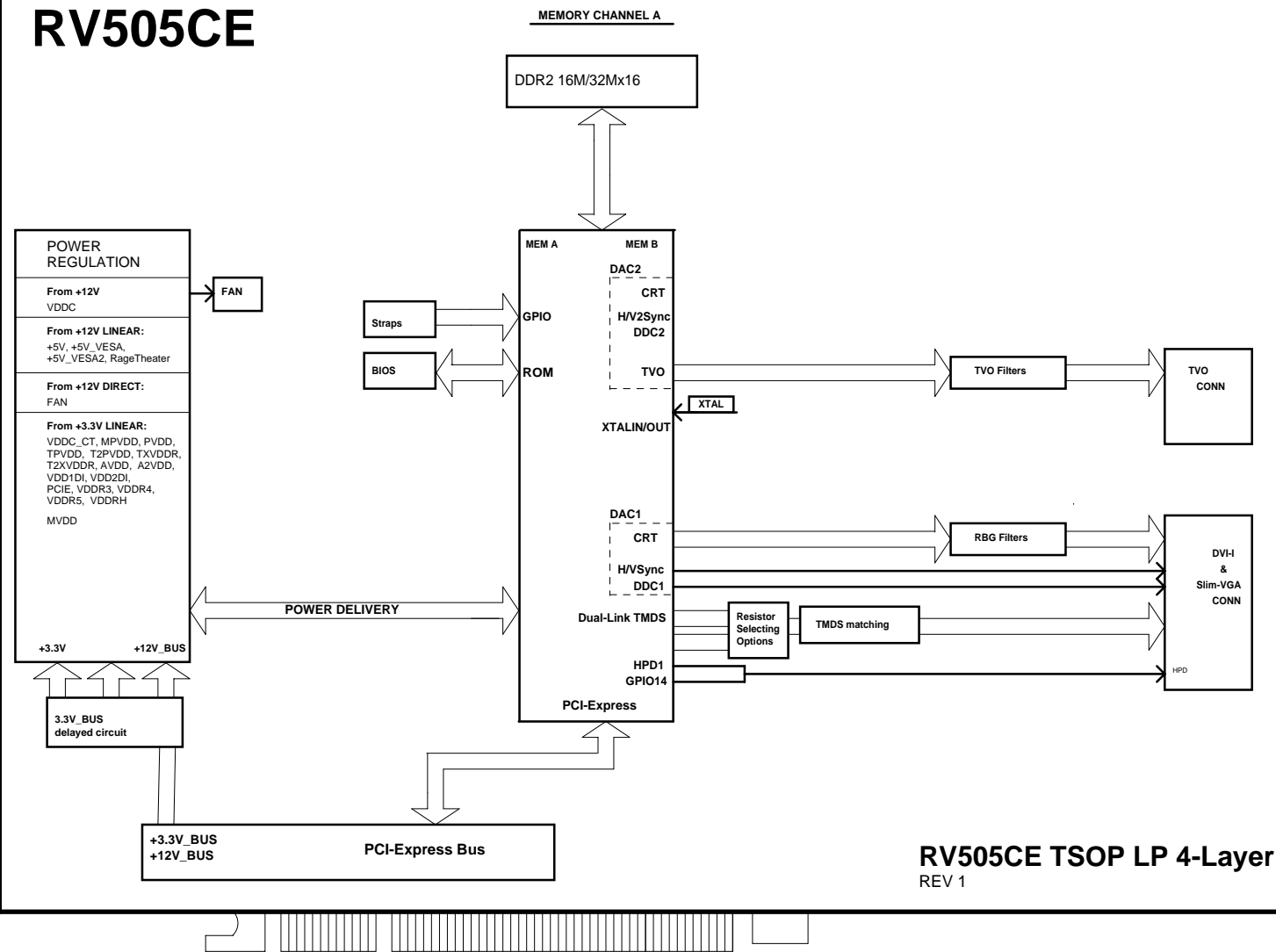
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# RV505CE



RV505CE TSOP LP 4-Layer  
REV 1



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