V133-0A

P729: G96, DDR2 MEMORY 32MX16/16MX16

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10729-xxxx-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU00000	600-10729-0000-000	G96-300-A1, 550/500MHz, 512MB 32Mx16 DDR2 BGA84 DVIDL+VGA+HDTV
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3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

REV HISTORY

Modify Power Sequencing

01/21 : PAGE 19.Add R100 R102 R103 R104 R105 Q100

PAGE 20.Add R101 R106 R107

PAGE 15.Add U100 U101 U102 U103 for EMI solution

PAGE 19.Add C100 C101 C102 C103 C104 to 12V_F power reserve

01/22 : PAGE 10.Add R111 R112 R113 R114 R115 R116 R117 for EMI bridge

PAGE 11.Add R121 R122 R123 R124 R125 R126 R127 for EMI bridge

PAGE 19.Add FBCDDQ to GND CAP C105 C106 C107 C108 C109 C110 C111 C112 for EMI solution

PAGE 19.Add 12V_F to GND CAP C113 C114 C115 C116 C117 for EMI solution

PAGE 18.Add 3V3_PEX to GND CAP C118 C119 for EMI solution

Nvidia updata Circuit

01/22 : PAGE 18 : remove PEX_RST

PAGE 11 : Add bias voltage resistor R130 R131 Link GPIO10_IFPCD_PD

PAGE 13 : Change new SLI connector for better EMI. (please refer to the symbol/part on P545)

PAGE 14 : revise fan circuit . Add C120 J9

PAGE 16 : change strape power to 2.5V

Nvidia modify Power circuit

01/22 : PAGE 19 : remove R100 R101 R102 R103 R628 R633 C85 Q13 L12

PAGE 19 : Add C121 C122

PAGE 19 : change P.20 LDO to P.19

Nvidia updata Circuit

01/29 : PAGE 15 : Change R602 to 2.2k ohm, C727 to 10k ohm, R598 to 75 ohm

PAGE 16 : Straps ROM_SI, ROM_SO,ROM_SCLK should still pull high to 3V3_PEX

PAGE 14 : Please use correct BJT for Q23, Q24,Q25,Q31,Q32

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P729 Overview

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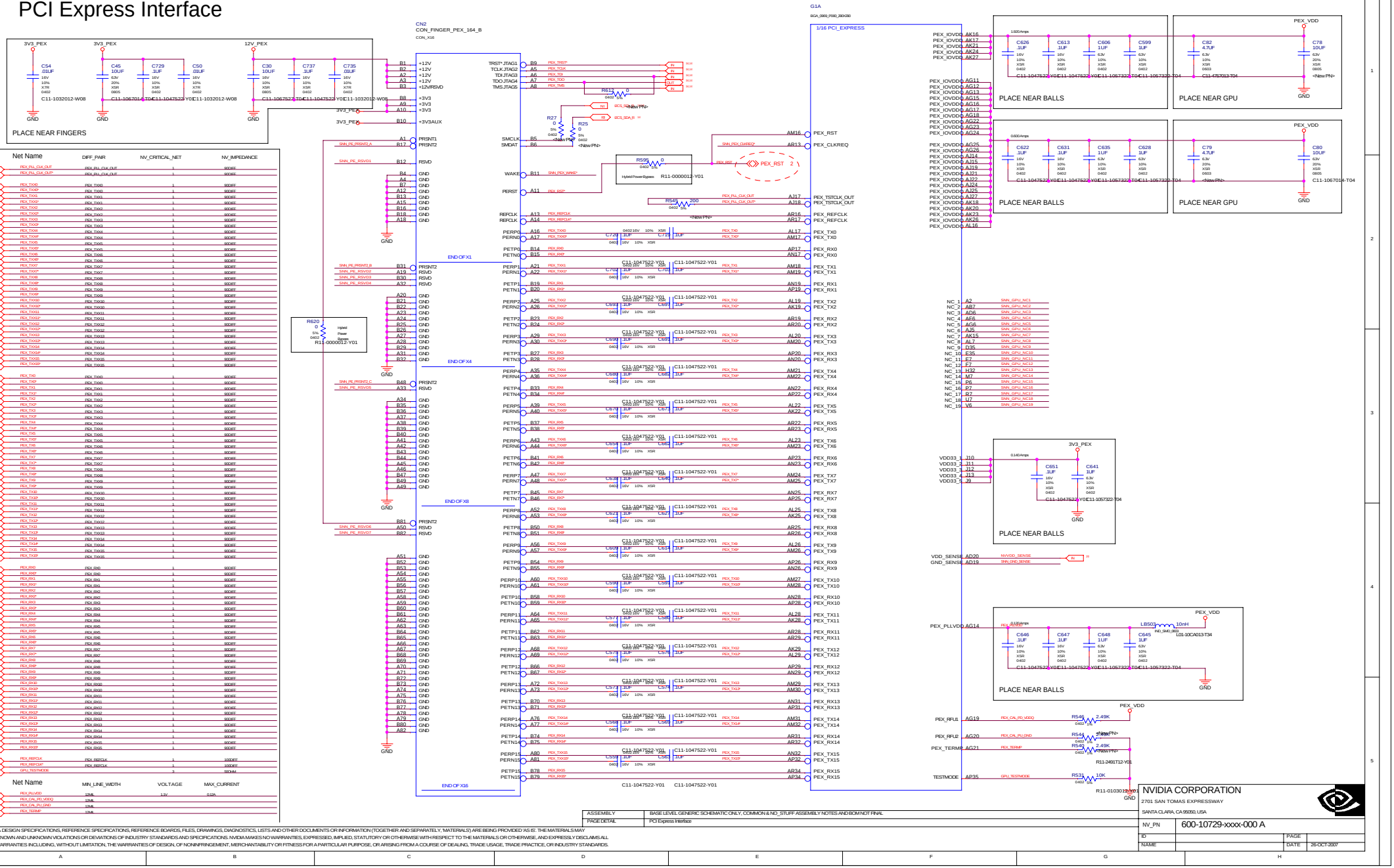
PCI Express Interface



Net Name

Net Name	DIFF_PAIR	NV_CRITICAL_NET	NV_IMPEDANCE
PEX_PLL_CLK_OUT	PEX_PLL_CLK_OUT	1	90DIFF
PEX_PLL_CLK_OUT*	PEX_PLL_CLK_OUT*	1	90DIFF
PEX_TX0D	PEX_TX0D	1	90DIFF
PEX_TX0D*	PEX_TX0D*	1	90DIFF
PEX_TX0C	PEX_TX0C	1	90DIFF
PEX_TX0C*	PEX_TX0C*	1	90DIFF
PEX_TX0B	PEX_TX0B	1	90DIFF
PEX_TX0B*	PEX_TX0B*	1	90DIFF
PEX_TX0A	PEX_TX0A	1	90DIFF
PEX_TX0A*	PEX_TX0A*	1	90DIFF
PEX_TX04	PEX_TX04	1	90DIFF
PEX_TX04*	PEX_TX04*	1	90DIFF
PEX_TX05	PEX_TX05	1	90DIFF
PEX_TX05*	PEX_TX05	1	90DIFF
PEX_TX06	PEX_TX06	1	90DIFF
PEX_TX06*	PEX_TX06	1	90DIFF
PEX_TX07	PEX_TX07	1	90DIFF
PEX_TX07*	PEX_TX07	1	90DIFF
PEX_TX08	PEX_TX08	1	90DIFF
PEX_TX08*	PEX_TX08	1	90DIFF
PEX_TX09	PEX_TX09	1	90DIFF
PEX_TX09*	PEX_TX09	1	90DIFF
PEX_TX0D	PEX_TX10	1	90DIFF
PEX_TX0D*	PEX_TX10	1	90DIFF
PEX_TX0E	PEX_TX11	1	90DIFF
PEX_TX0E*	PEX_TX11	1	90DIFF
PEX_TX0F	PEX_TX12	1	90DIFF
PEX_TX0F*	PEX_TX12	1	90DIFF
PEX_TX10	PEX_TX13	1	90DIFF
PEX_TX10*	PEX_TX13	1	90DIFF
PEX_TX11	PEX_TX14	1	90DIFF
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PEX_TX12	PEX_TX15	1	90DIFF
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PEX_TX16	PEX_TX19	1	90DIFF
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PEX_TX17	PEX_TX20	1	90DIFF
PEX_TX17*	PEX_TX20	1	90DIFF
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PEX_TX18*	PEX_TX21	1	90DIFF
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PEX_TX23	PEX_TX32	1	90DIFF
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PEX_TX29*	PEX_TX38	1	90DIFF
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PEX_TX2A*	PEX_TX39	1	90DIFF
PEX_TX2B	PEX_TX40	1	90DIFF
PEX_TX2B*	PEX_TX40	1	90DIFF
PEX_TX2C	PEX_TX41	1	90DIFF
PEX_TX2C*	PEX_TX41	1	90DIFF
PEX_TX2D	PEX_TX42	1	90DIFF
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PEX_TX3B*	PEX_TX56	1	90DIFF
PEX_TX3C	PEX_TX57	1	90DIFF
PEX_TX3C*	PEX_TX57	1	90DIFF
PEX_TX3D	PEX_TX58	1	90DIFF
PEX_TX3D*	PEX_TX58	1	90DIFF
PEX_TX3E	PEX_TX59	1	90DIFF
PEX_TX3E*	PEX_TX59	1	90DIFF
PEX_TX3F	PEX_TX60	1	90DIFF
PEX_TX3F*	PEX_TX60	1	90DIFF
PEX_REFCLK	PEX_REFCLK	1	100DIFF
PEX_REFCLK*	PEX_REFCLK	1	100DIFF
GPU_TESTMODE		1	50OHM

Net Name

Net Name	MIN_LINE_WIDTH	VOLTAGE	MAX_CURRENT
PEX_PLLVDD	20MIL	1.0V	0.12A
PEX_CAL_PD_VDDQ	10MIL		
PEX_CAL_PU_GND	10MIL		
PEX_TERMP	10MIL		

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express Interface

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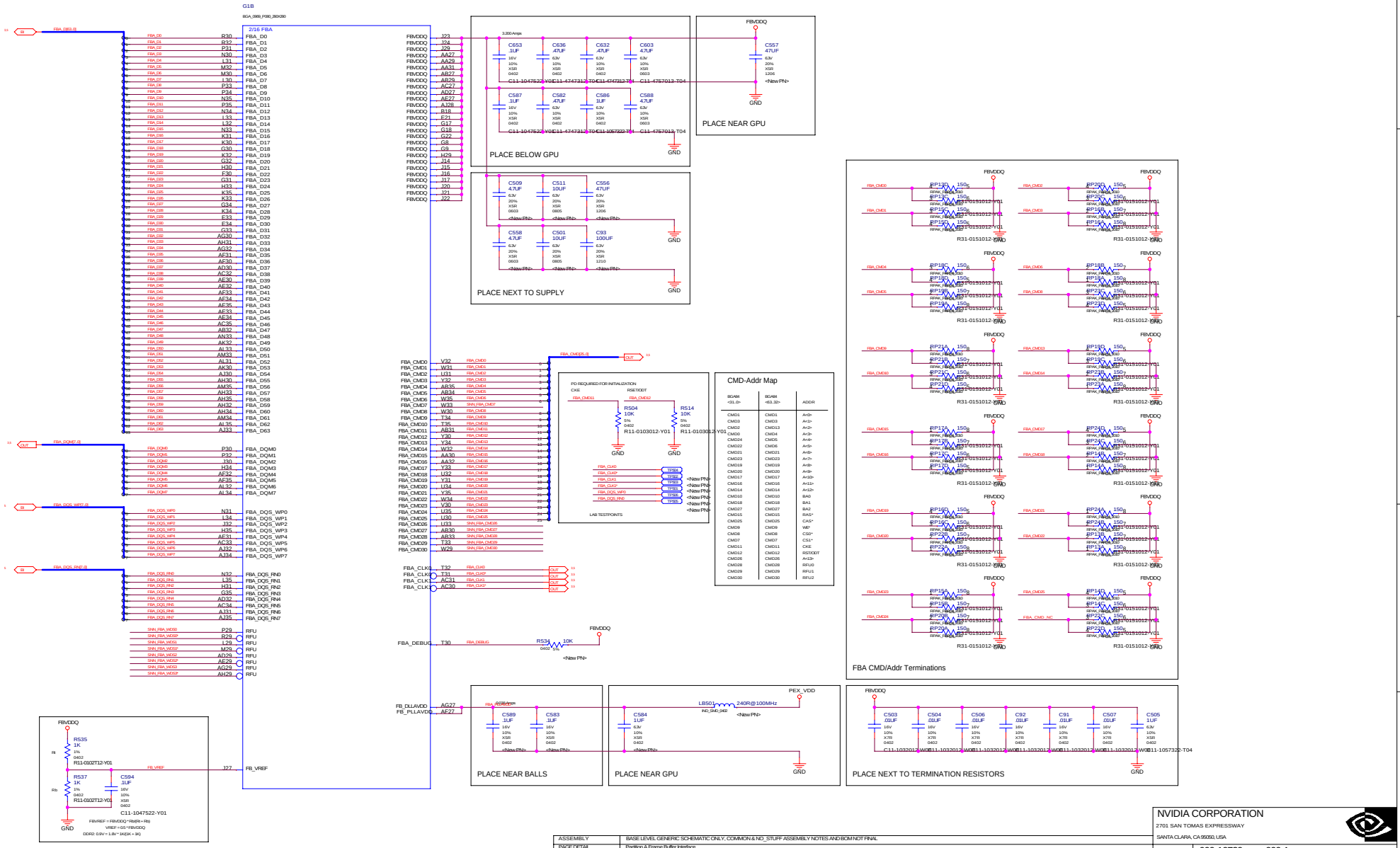
Partition A Frame Buffer Interface



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PAGE DETAIL	Partition A Frame Buffer Interface

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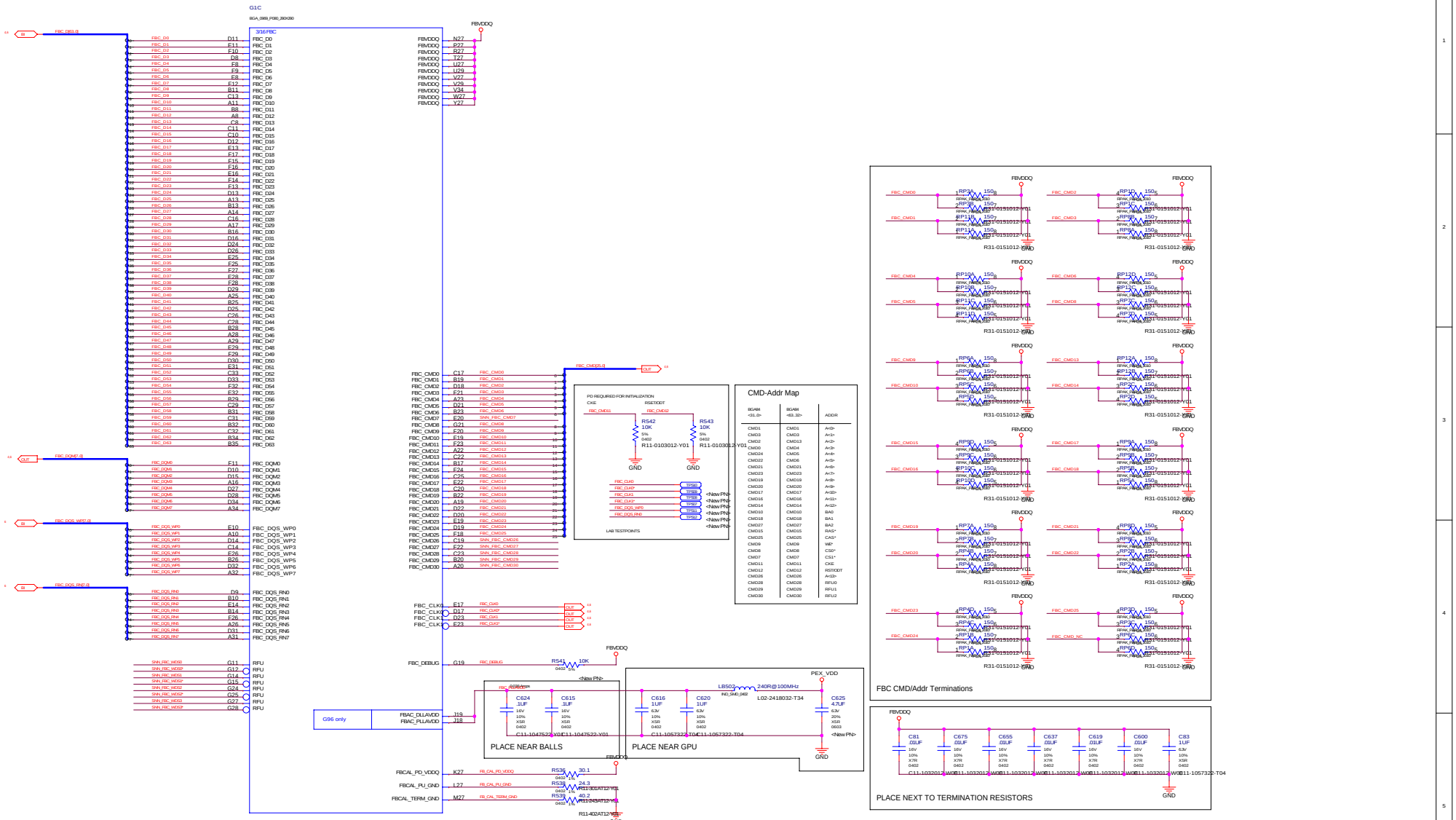
Partition C Frame Buffer Interface



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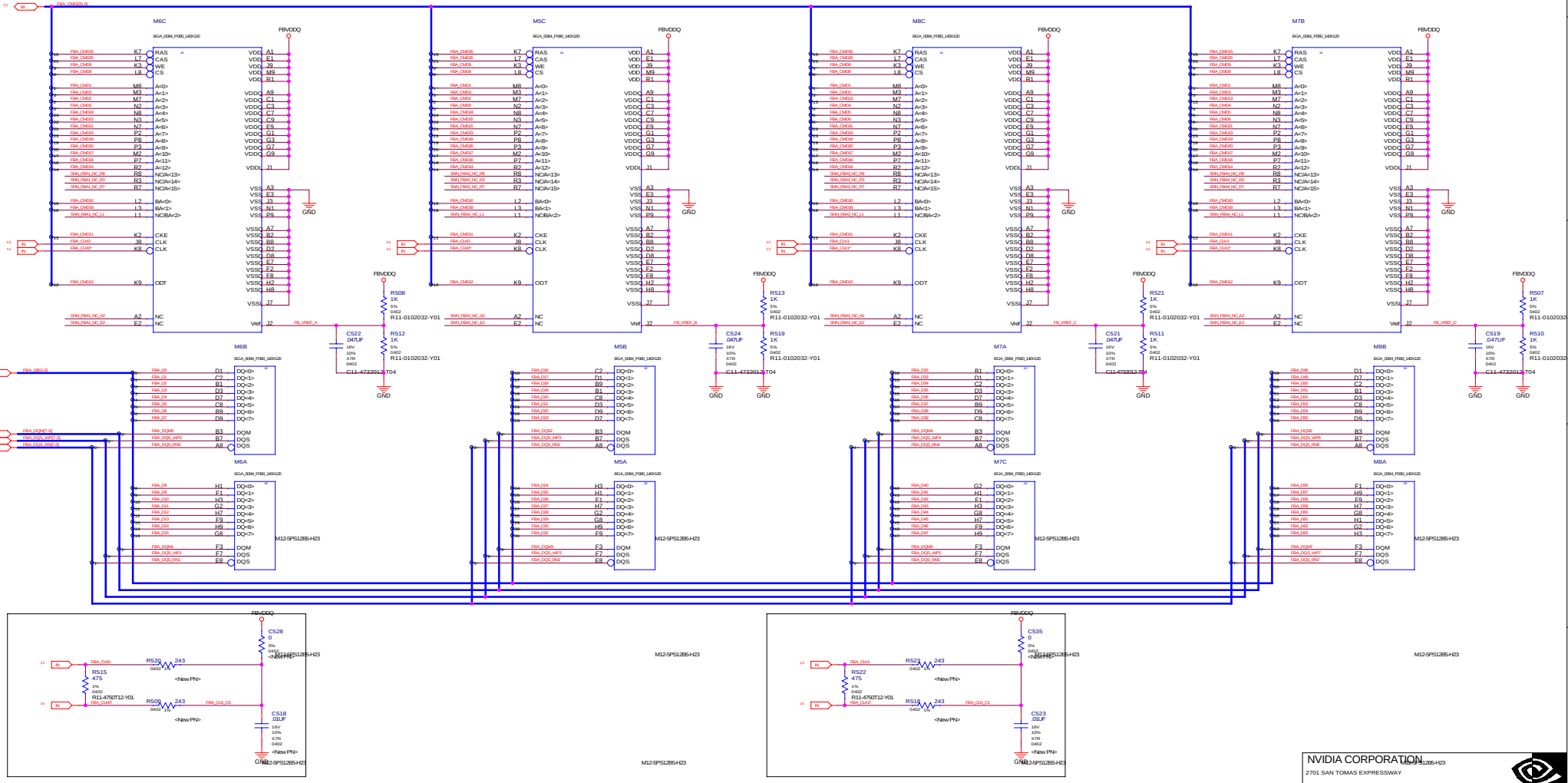
Partition A Memories



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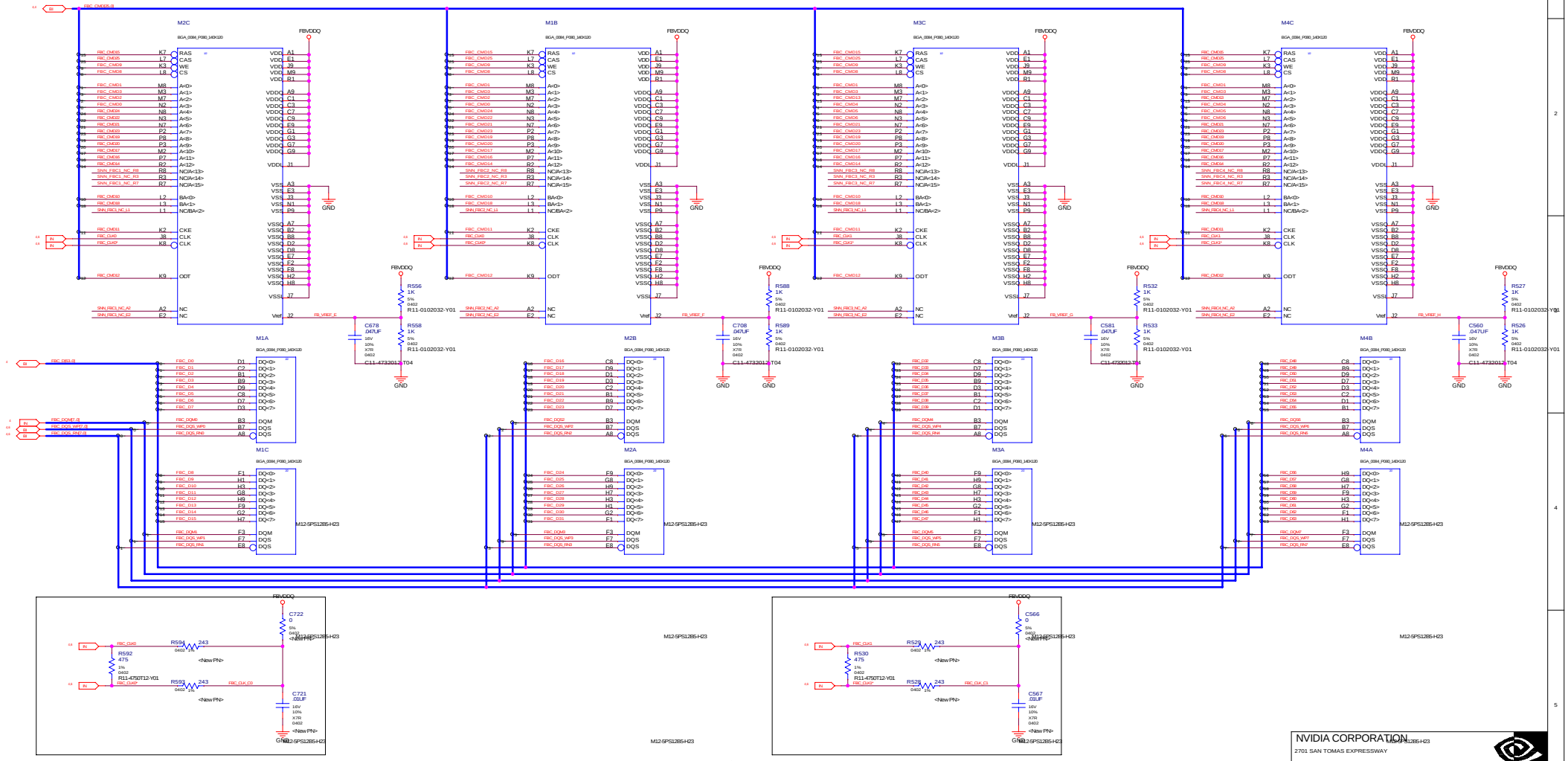
Partition C Memories



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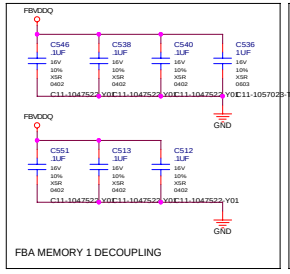
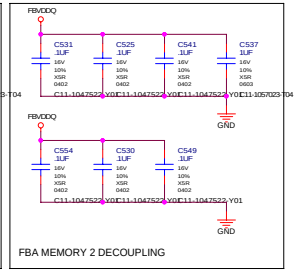
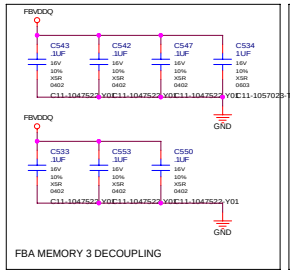
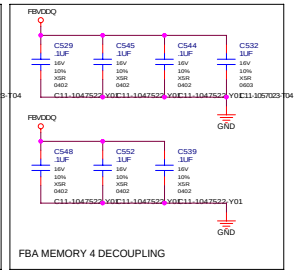
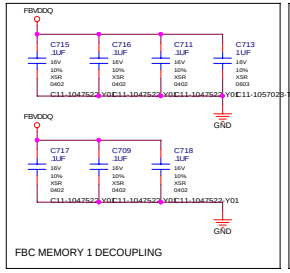
Decoupling Caps

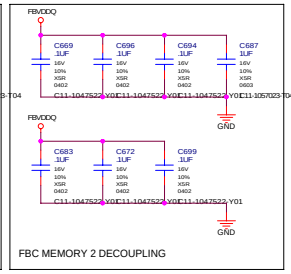


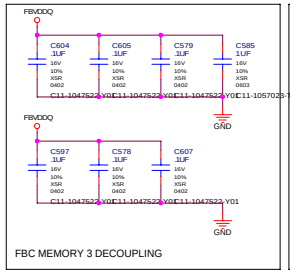


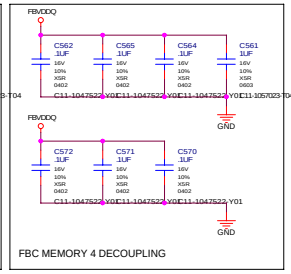


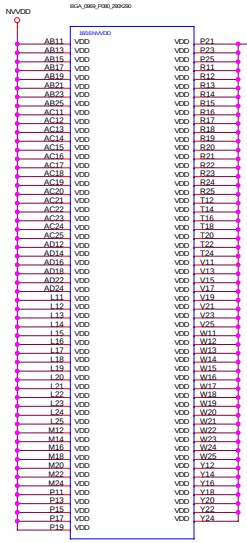


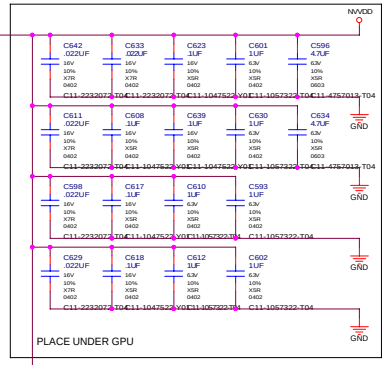


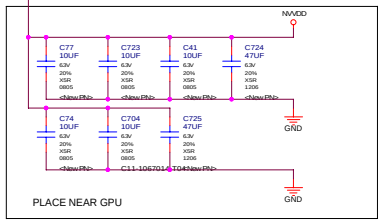


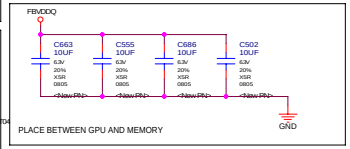


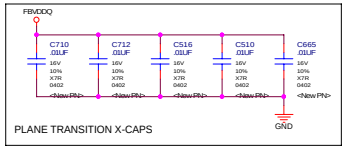


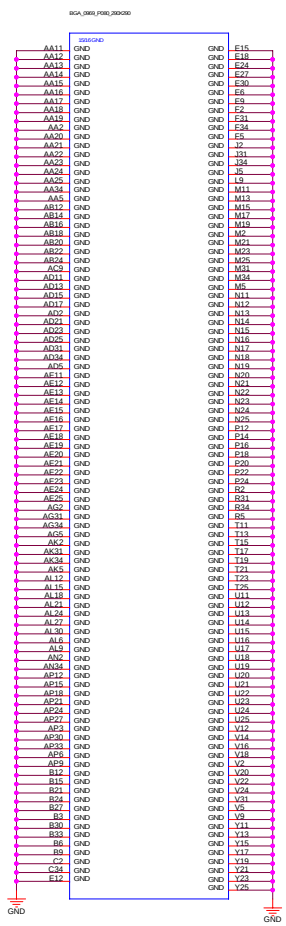












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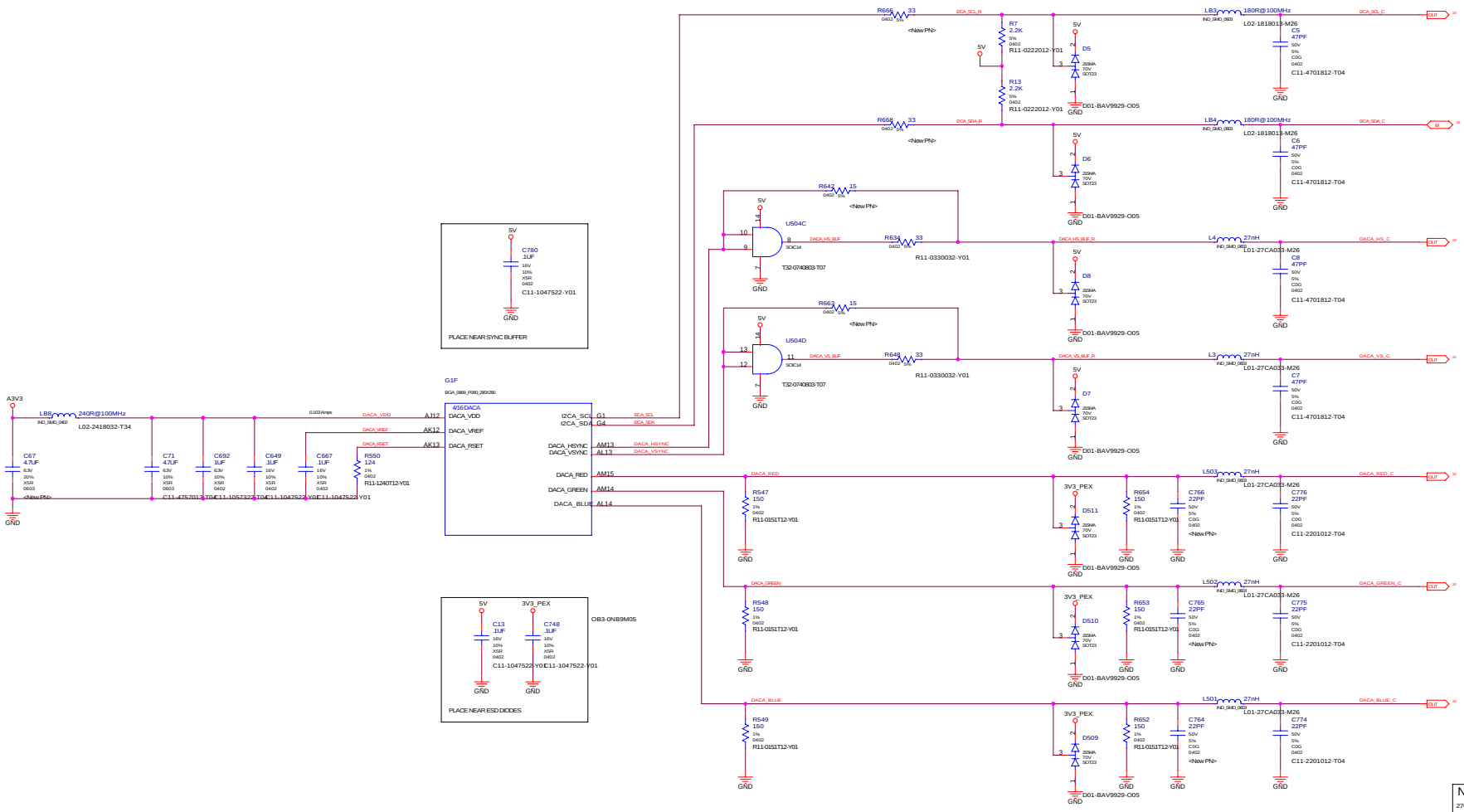
PAGE DETAIL	Decoupling Caps

DACA



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA

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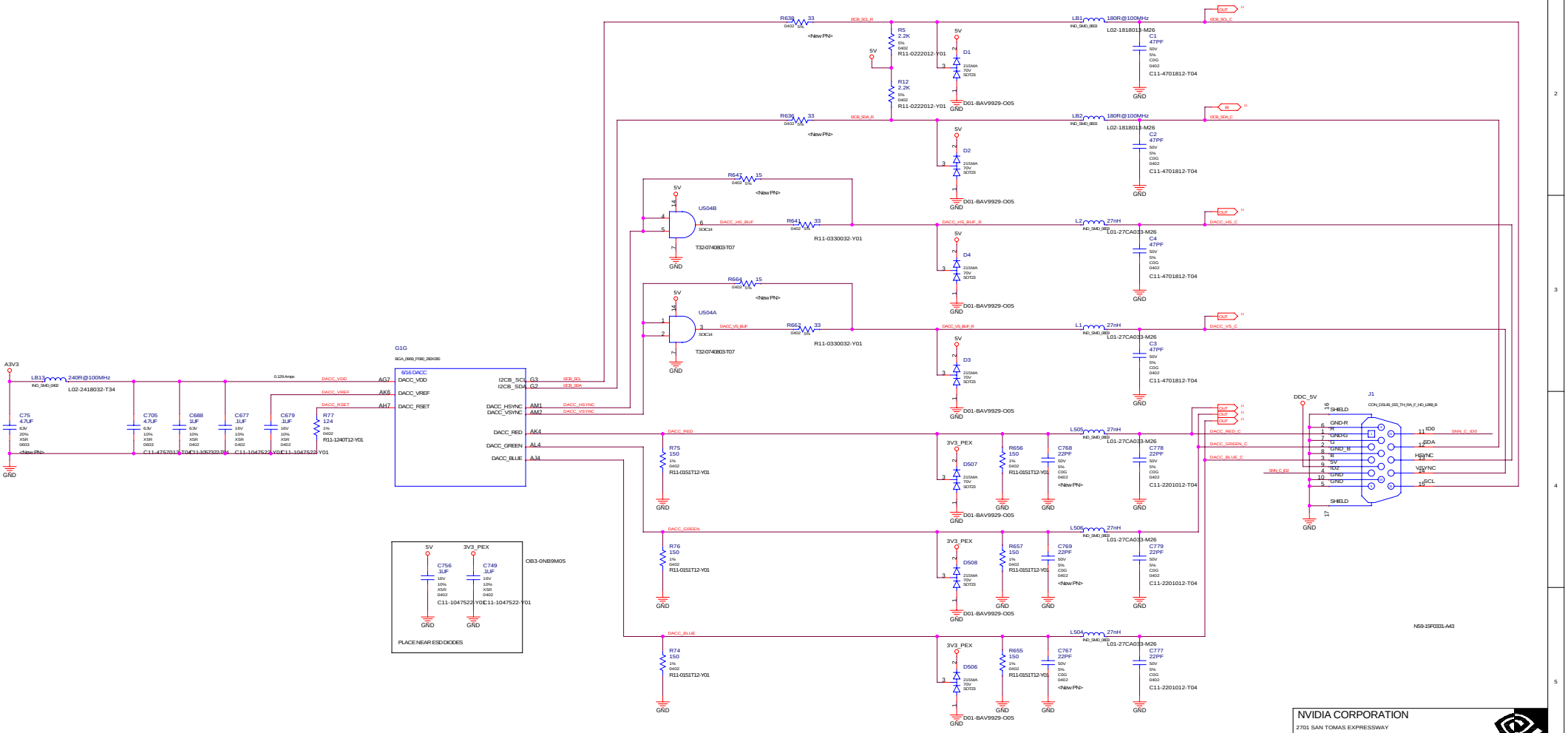
DACC, Slim DB15 Connector



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC, Slim DB15 Connector

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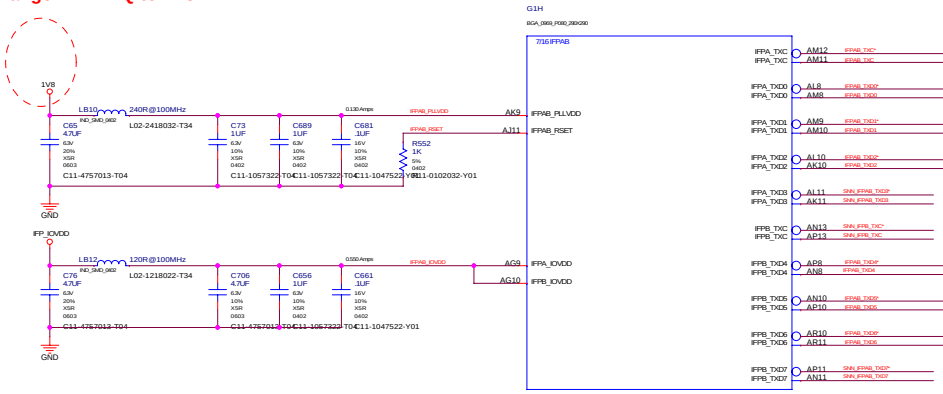
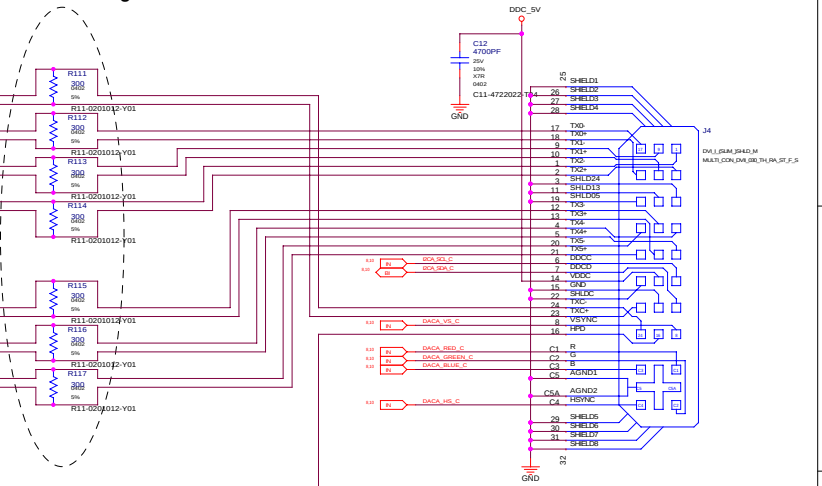
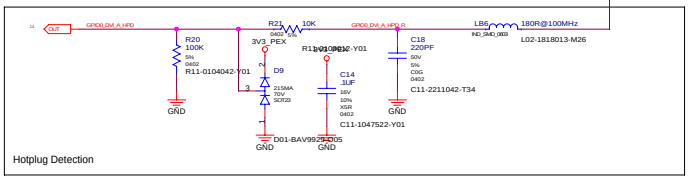
Internal TMDS .. Link A & B

change FBVDDQ to 1V8



add EMI bridge





NSB-30F0281-A43

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Internal TMDS .. Link A & B

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Internal TMDS .. Link C & D

change FBVDDQ to 1V8

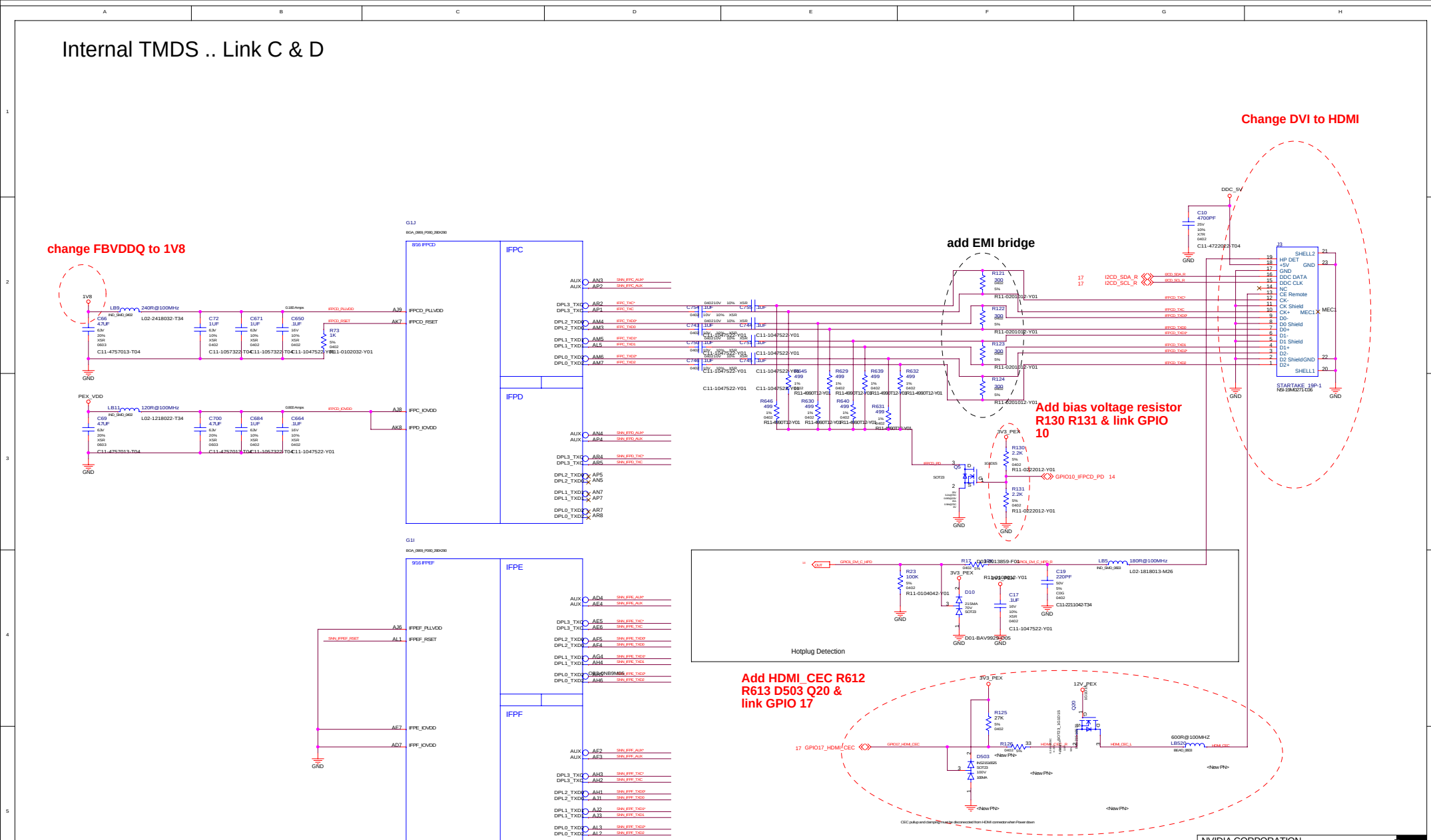
add EMI bridge

Change DVI to HDMI

Add bias voltage resistor R130 R131 & link GPIO 10

Add HDMI_CEC R612 R613 D503 Q20 & link GPIO 17

Hotplug Detection



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Internal TMDS .. Link C & D

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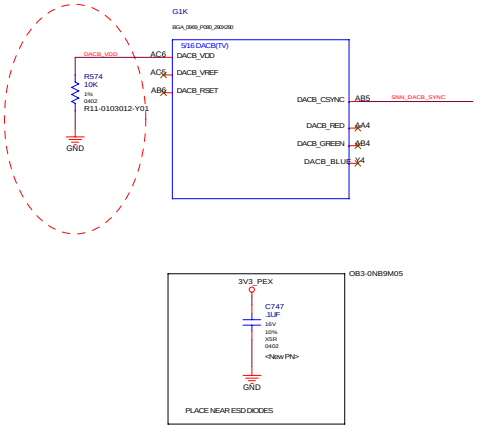
DACB, MINIDIN Connector

Change R574 to 10K



Remove TV-OUT

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB, MINIDIN Connector

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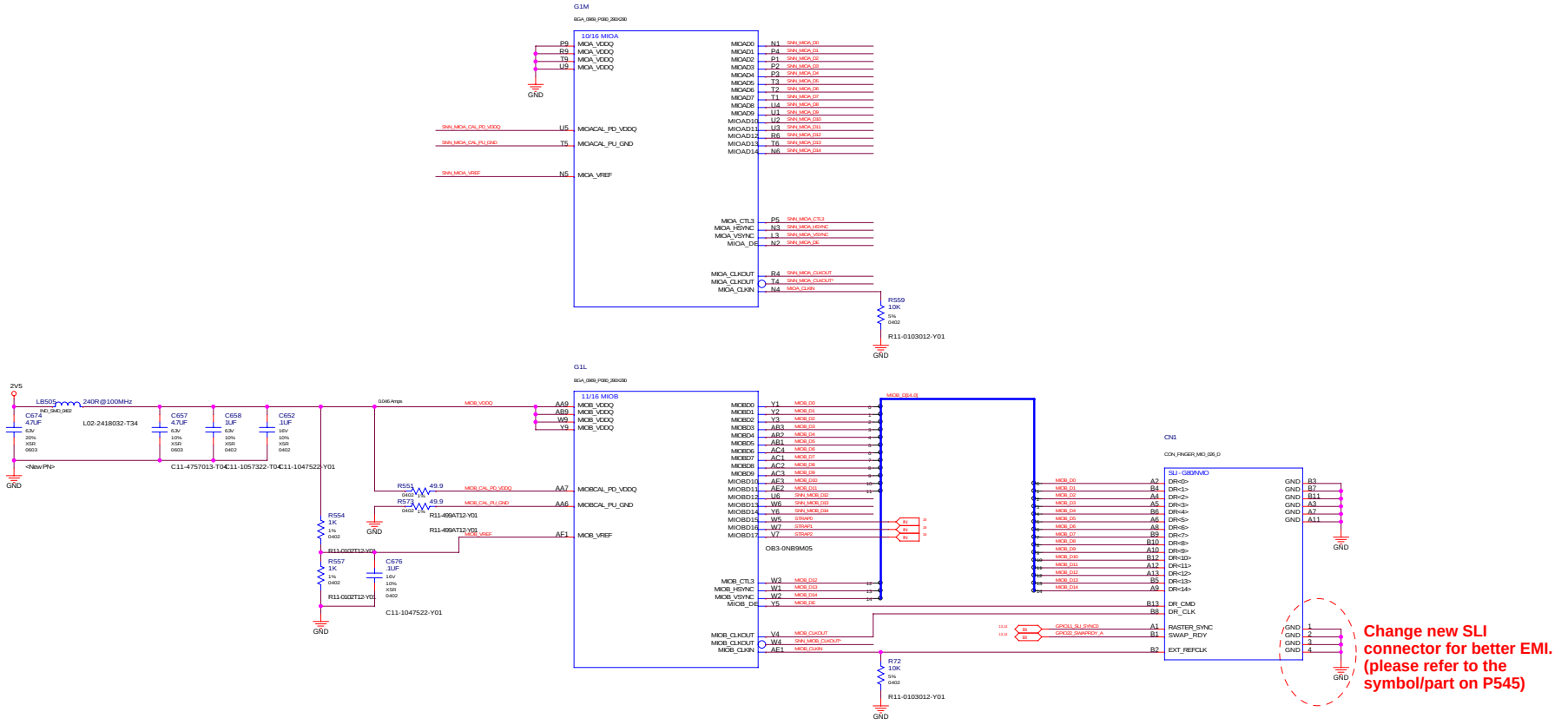
MIOA, MIOB Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA, MIOB Interface

OB3-0NB9M05

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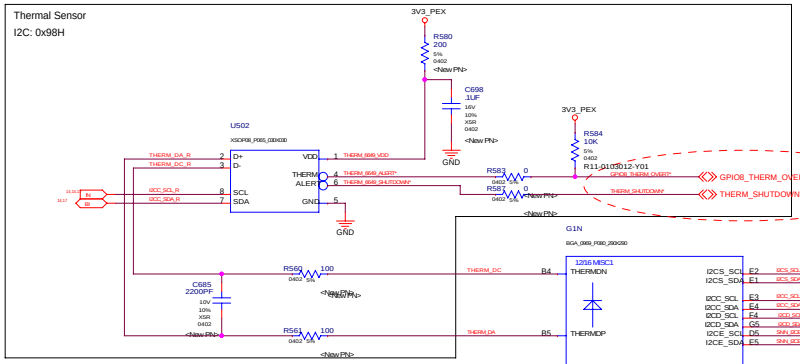
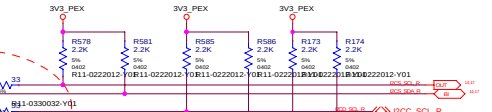
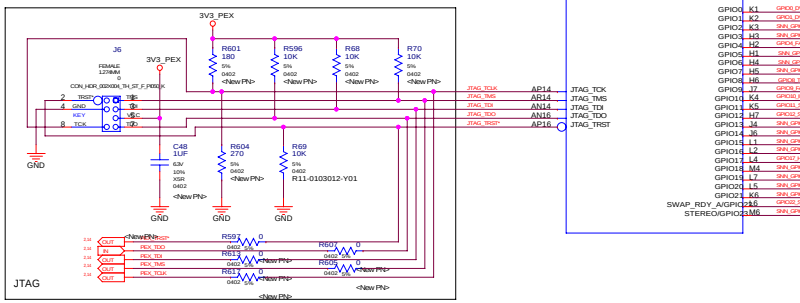
Thermal Sensors, GPIOs, XTAL, JTAG, Fan

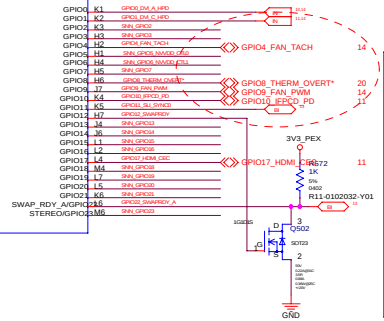




change Thermal protection

Add R171 R172 R173 R174
I2CD_SCL & I2CD_SDA



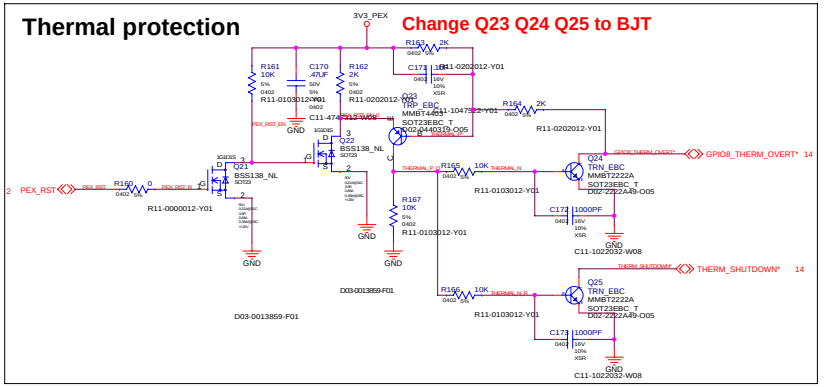


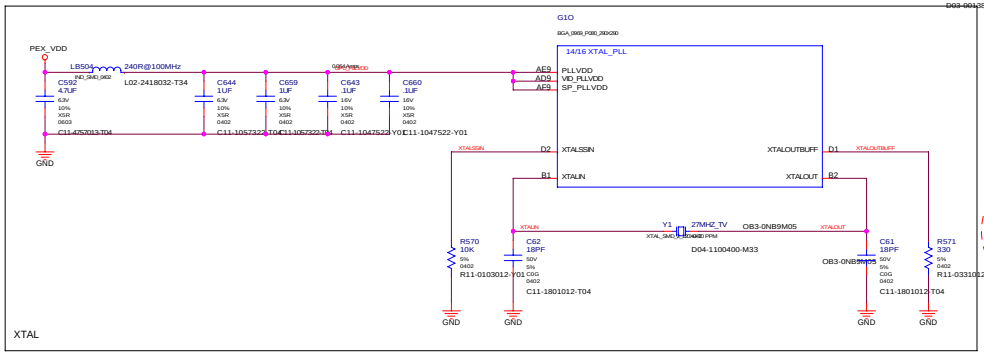
GPIO Table

GPIO	I/O	Function
0	IN	DVI SOUTH HOTPLUG DETECT
1	IN	DVI MID HOTPLUG DETECT
2		
3		
4	OUT	PWMFAN
5	OUT	NVVDD VOLTAGE SELECT 0
6	OUT	NVVDD VOLTAGE SELECT 1
7		
8	IN	THERMAL SLOWDOWN
9	IN	FAN TACH
10		
11	IN/OUT	RASTER SYNC 0
12	OUT	SWAP READY OUT
13		
14		
15		
16		
17		
18		
19		
20		
21		
22	IN	SWAP READY IN
23		

Thermal protection

Change Q23 Q24 Q25 to BJT





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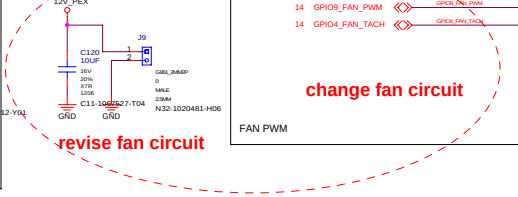
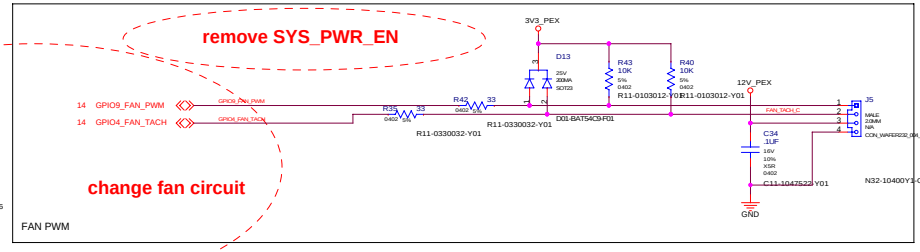


revise fan circuit

remove SYS_PWR_EN



change fan circuit

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Sensors, GPIOs, XTAL, JTAG, Fan

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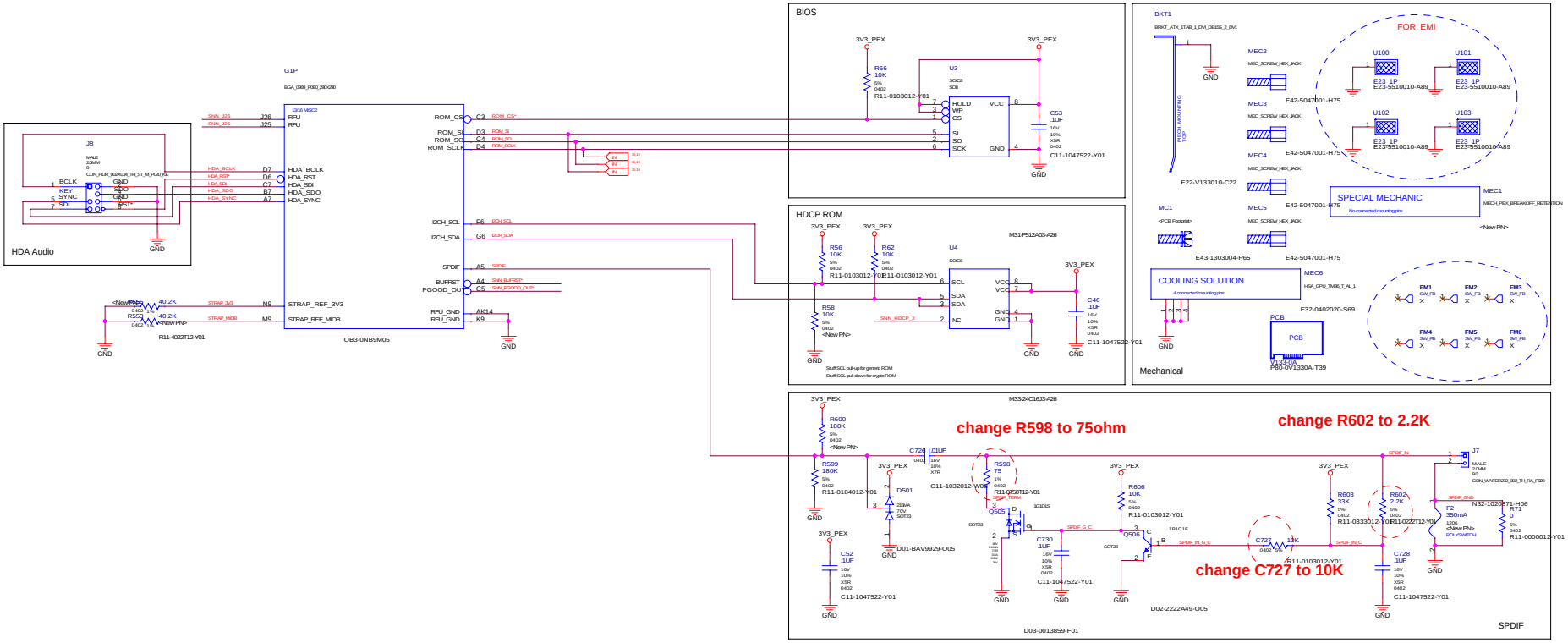
BIOS, HDCP, SPDIF, HDA, Mechanical



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS, HDCP, SPDIF, HDA, Mechanical

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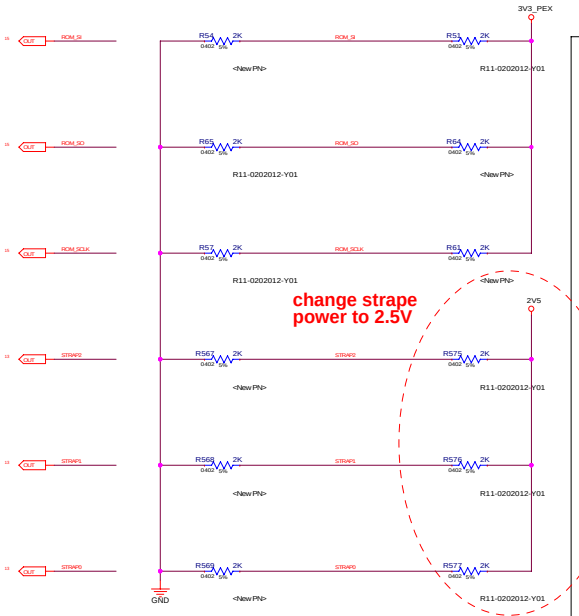
Straps



G94 Straps
Multilevel Mode

Bit	Signal	Values
03	XCLK_277	0:DISABLED 1:ENABLED
02	TVMODE[2]	000:NTSC_M 001:NTSC_J 010:PAL_M 011:PAL_N 100:PAL_CN 101:PAL_BDGHI 110:RESERVED0 111:RESERVED1
01	TVMODE[1]	
00	TVMODE[0]	
03	PCI_DEVID_EXT	1:G96-300-A1
02	SUB_VENDOR	0:NO BIOS 1:BIOS
01	SLOT_CLK_CFG	0:DISABLE 1:ENABLE
00	PEX_PLL_EN_TERM000	0:DIS 1:EN
03	RAMCFG[3]	0000:32Mx16/16Mx16:DDR2:128-bit:Elpida 0001:16Mx16:DDR2:128-bit:Samsung, Micron 0010:16Mx16:DDR2:128-bit:Qimonda 0011:16Mx16:DDR2:128-bit:Hynix 0100:32Mx16/16Mx16:DDR2:128-bit:Nanya 0101:32Mx16:DDR2:128-bit:Samsung 0110:32Mx16:DDR2:128-bit:Qimonda 0111 32Mx16 DDR2 128-bit Hynix 1000:32Mx16/16Mx16:DDR2:64-bit:Elpida 1001:16Mx16:DDR2:64-bit:Samsung, Micron 1010:16Mx16:DDR2:64-bit:Qimonda 1011:16Mx16:DDR2:64-bit:Hynix 1100:32Mx16/16Mx16:DDR2:64-bit:Nanya 1101:32Mx16:DDR2:64-bit:Samsung 1110:32Mx16:DDR2:64-bit:Qimonda 1111:32Mx16:DDR2:64-bit:Hynix
02	RAMCFG[2]	
01	RAMCFG[1]	
00	RAMCFG[0]	
03	PCI_DEVID[3]	0001:G96-300-A1
02	PCI_DEVID[2]	
01	PCI_DEVID[1]	
00	PCI_DEVID[0]	
03	3GIO_PADCFG_LUG_ADR[3]	0000:DSKTOP_DEFAULT 0001:MOBILE_DEFAULT 0010:MOBILE_NTHRS_LLAMP 0011:MOBILE_NTHRS_LAMP 0100:MOBILE_NTHRS_HAMP 0101:MOBILE_NTHRS_HHAMP 0110:MOBILE_NTHRS_HHHAMP 0111:MOBILE_NTHRS_HHHHAMP 1000:DSKTOP_HTHRS 1001:MOBILE_HTHRS_NAMP 1010:MOBILE_HTHRS_LLAMP 1011:MOBILE_HTHRS_LAMP 1100:MOBILE_HTHRS_HAMP 1101:MOBILE_HTHRS_HHAMP 1110:MOBILE_HTHRS_HHHAMP 1111:MOBILE_HTHRS_HHHHAMP
02	3GIO_PADCFG_LUG_ADR[2]	
01	3GIO_PADCFG_LUG_ADR[1]	
00	3GIO_PADCFG_LUG_ADR[0]	
03	USER[3]	0000:DEFAULT
02	USER[2]	
01	USER[1]	
00	USER[0]	

Multilevel Straps

5K to GND	0000
10K to GND	0001
15K to GND	0010
20K to GND	0011
25K to GND	0100
30K to GND	0101
35K to GND	0110
45K to GND	0111
5K to VCC	1000
10K to VCC	1001
15K to VCC	1010
20K to VCC	1011
25K to VCC	1100
30K to VCC	1101
35K to VCC	1110
45K to VCC	1111

G94 Straps
Binary-Bringup Mode

Bit	Signal	Values
	SUB_VENDOR	0:NO BIOS 1:BIOS
	SLOT_CLK_CFG	0:DISABLE 1:ENABLE
	3GIO_PADCFG_LUT_ADR[3]	0000:DSKTOP_DEFAULT 0001:MOBILE_DEFAULT 0010:MOBILE_NTHRS_LLAMP 0011:MOBILE_NTHRS_LAMP 0100:MOBILE_NTHRS_HAMP 0101:MOBILE_NTHRS_HHAMP 0110:MOBILE_NTHRS_HHHAMP 0111:MOBILE_NTHRS_HHHHAMP 1000:DSKTOP_HTHRS 1001:MOBILE_HTHRS_NAMP 1010:MOBILE_HTHRS_LLAMP 1011:MOBILE_HTHRS_LAMP 1100:MOBILE_HTHRS_HAMP 1101:MOBILE_HTHRS_HHAMP 1110:MOBILE_HTHRS_HHHAMP 1111:MOBILE_HTHRS_HHHHAMP
	3GIO_PADCFG_LUT_ADR[2]	
	3GIO_PADCFG_LUT_ADR[1]	
	3GIO_PADCFG_LUT_ADR[0]	

G94 Straps
Binary-Production Mode

Bit	Signal	Values
	SLOT_CLK_CFG	0:DISABLE 1:ENABLE
	PCI_DEVID_EXT	10:G96-300-A1
	PCI_DEVID[3]	
	RAMCFG[3]	000:32Mx16/16Mx16:DDR2:Elpida 001:16Mx16:DDR2:Samsung,Micron 010:16Mx16:DDR2:Qimonda 011:16Mx16:DDR2:Hynix 100:32Mx16/16Mx16:DDR2:Nanya 101:32Mx16:DDR2:Samsung 110:32Mx16:DDR2:Qimonda 111:32Mx16:DDR2:Hynix
	RAMCFG[1]	
	RAMCFG[0]	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Straps

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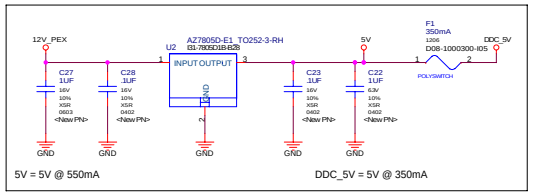
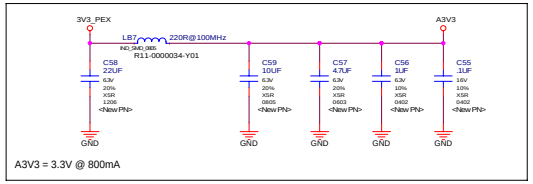
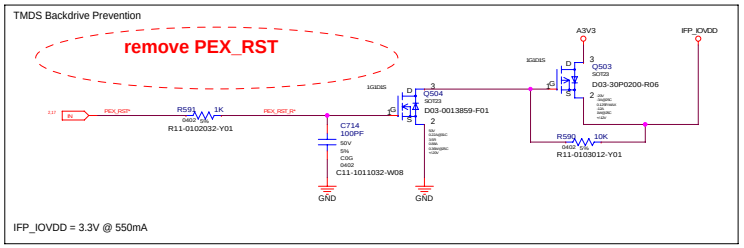
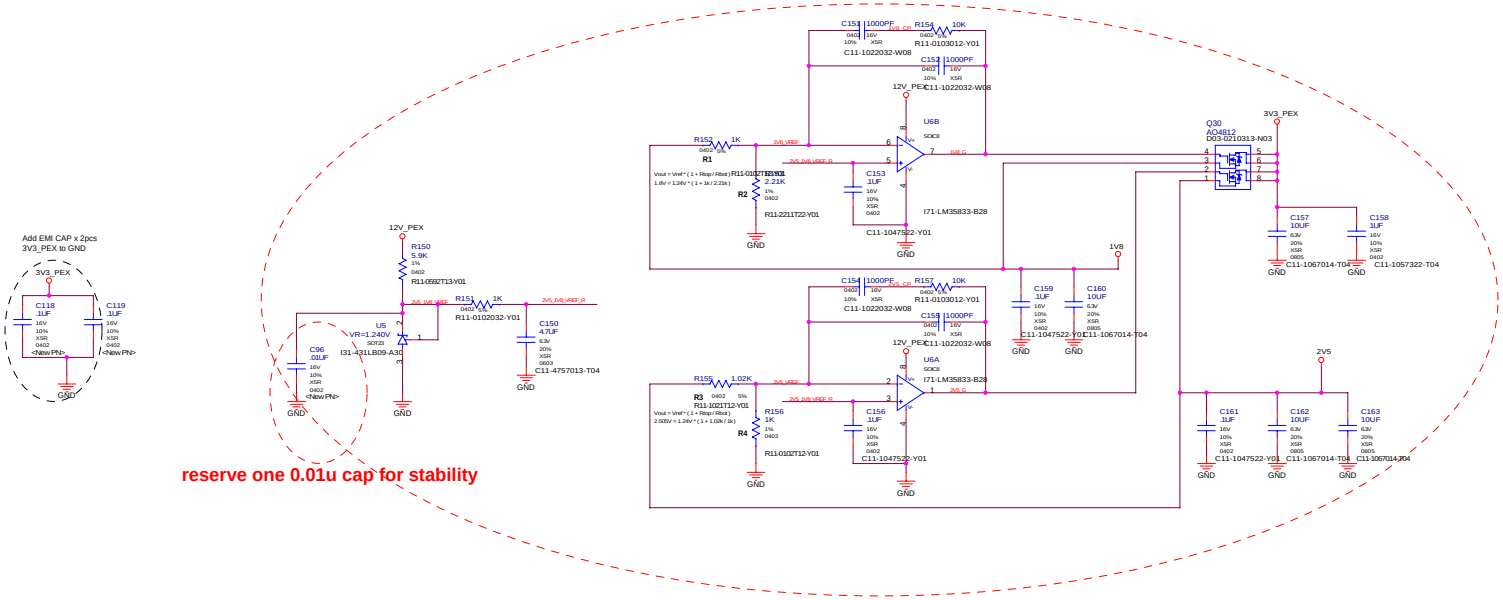
Power Supply I: 2V5, 3V3, 5V, IFP_IOVDD







Change 1V8 & 2V5 circuit



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply I: 2V5, 3V3, 5V, IFP_IOVDD

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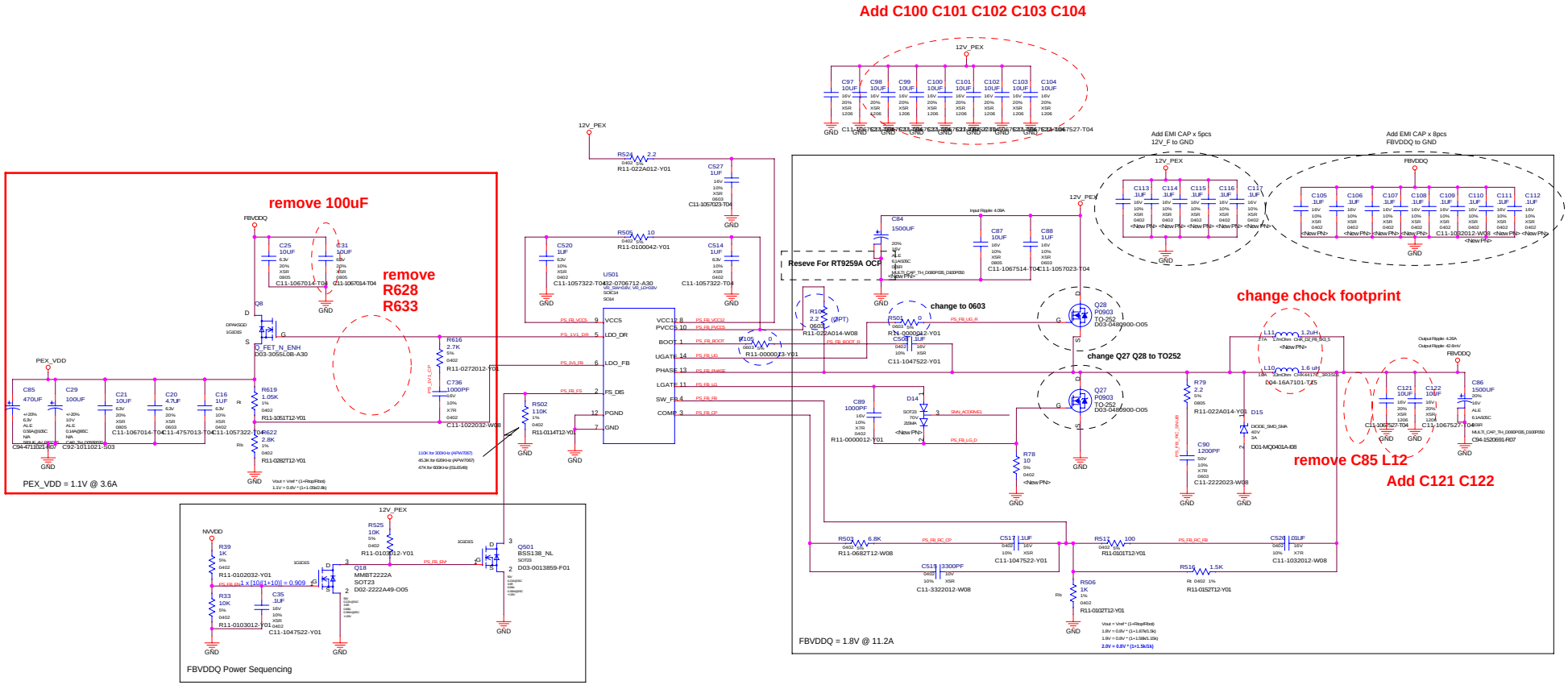
Power Supply II: FBVDDQ



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply II: FBVDDQ

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Power Supply III: NVVDD, PEX_VDD