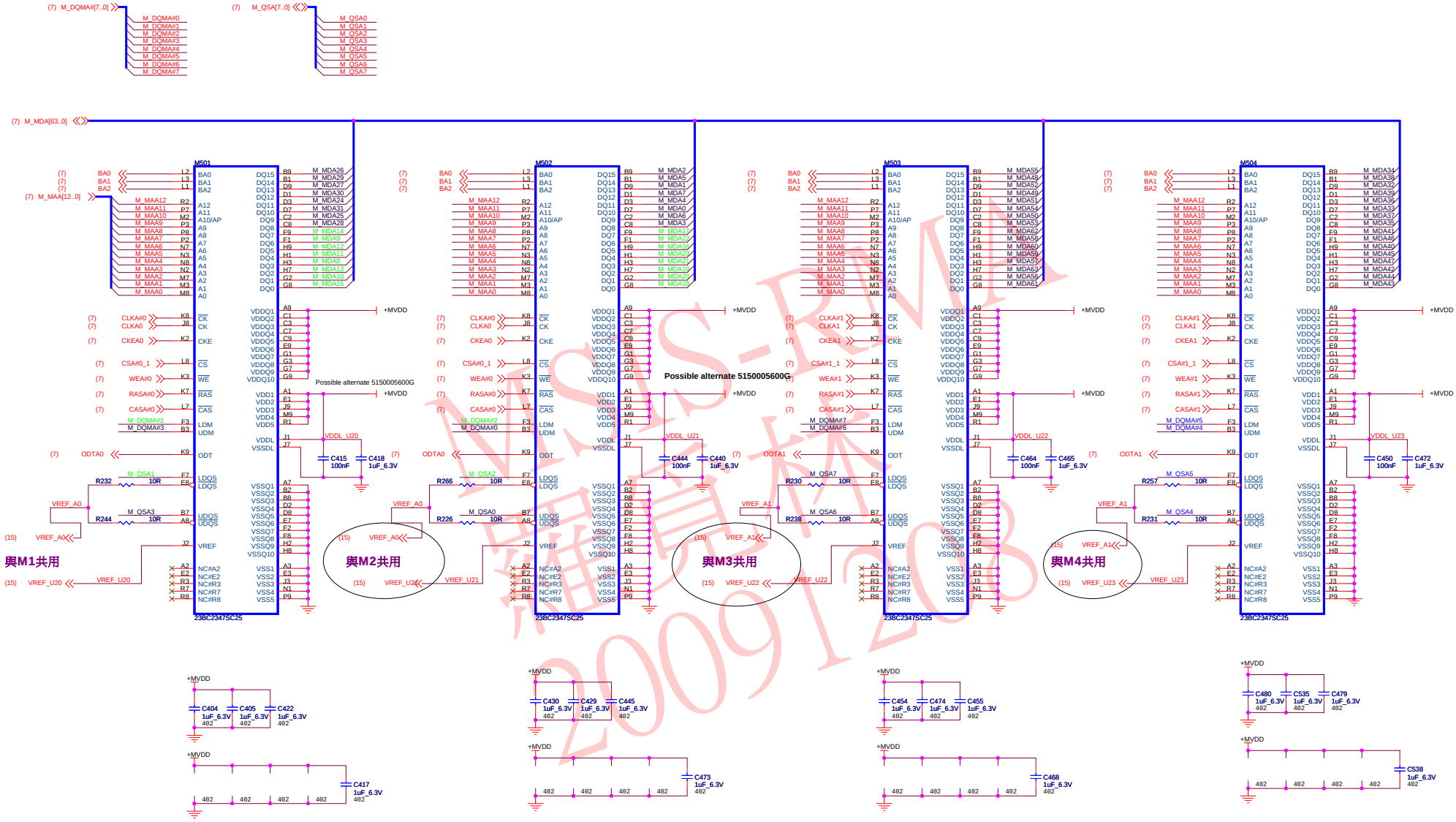
CHANNEL A: RANK 1 512MB DDR2

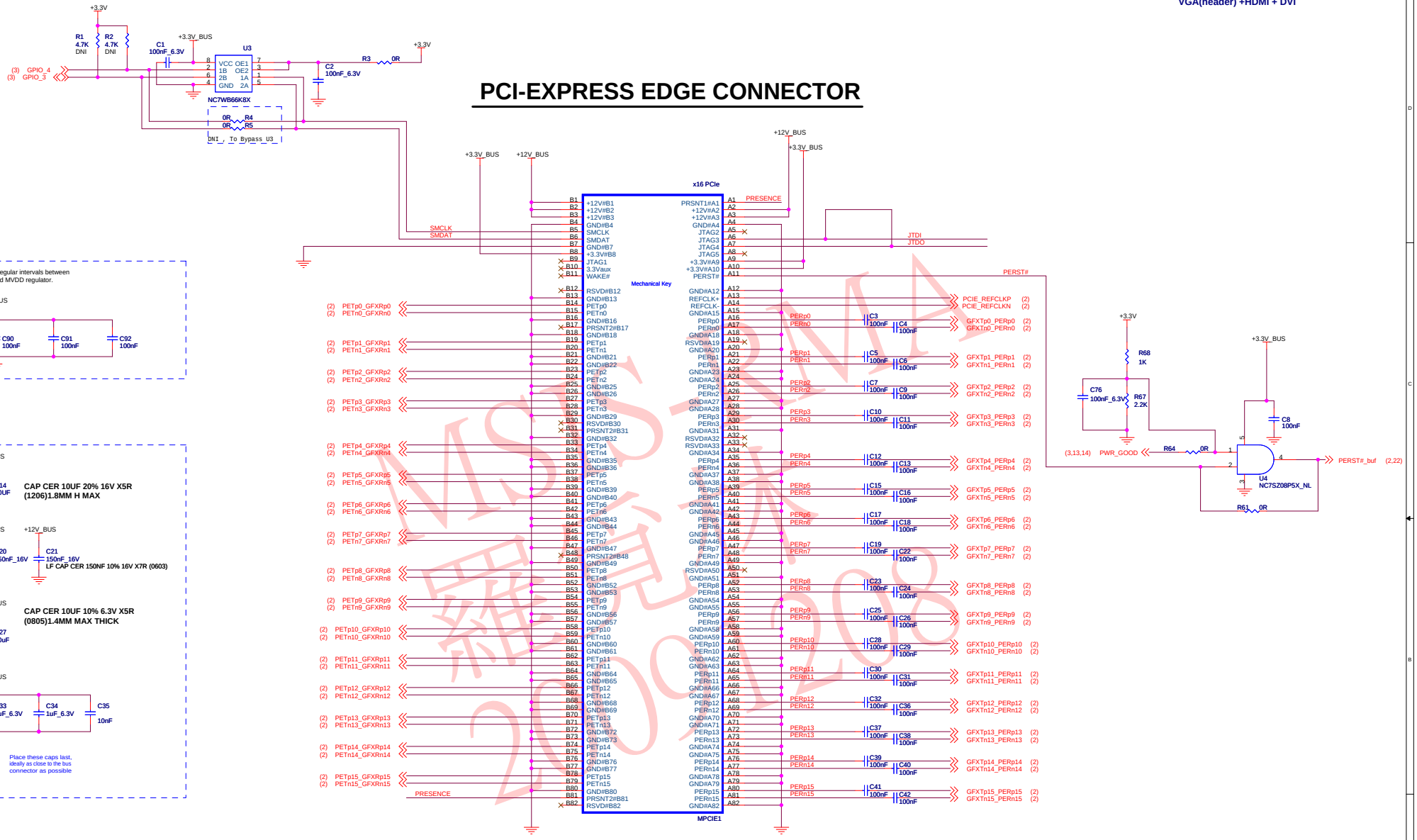
MAX DENSITY: 64Mx16



RV710 CLASH

VGA(header) +HDMI + DVI

PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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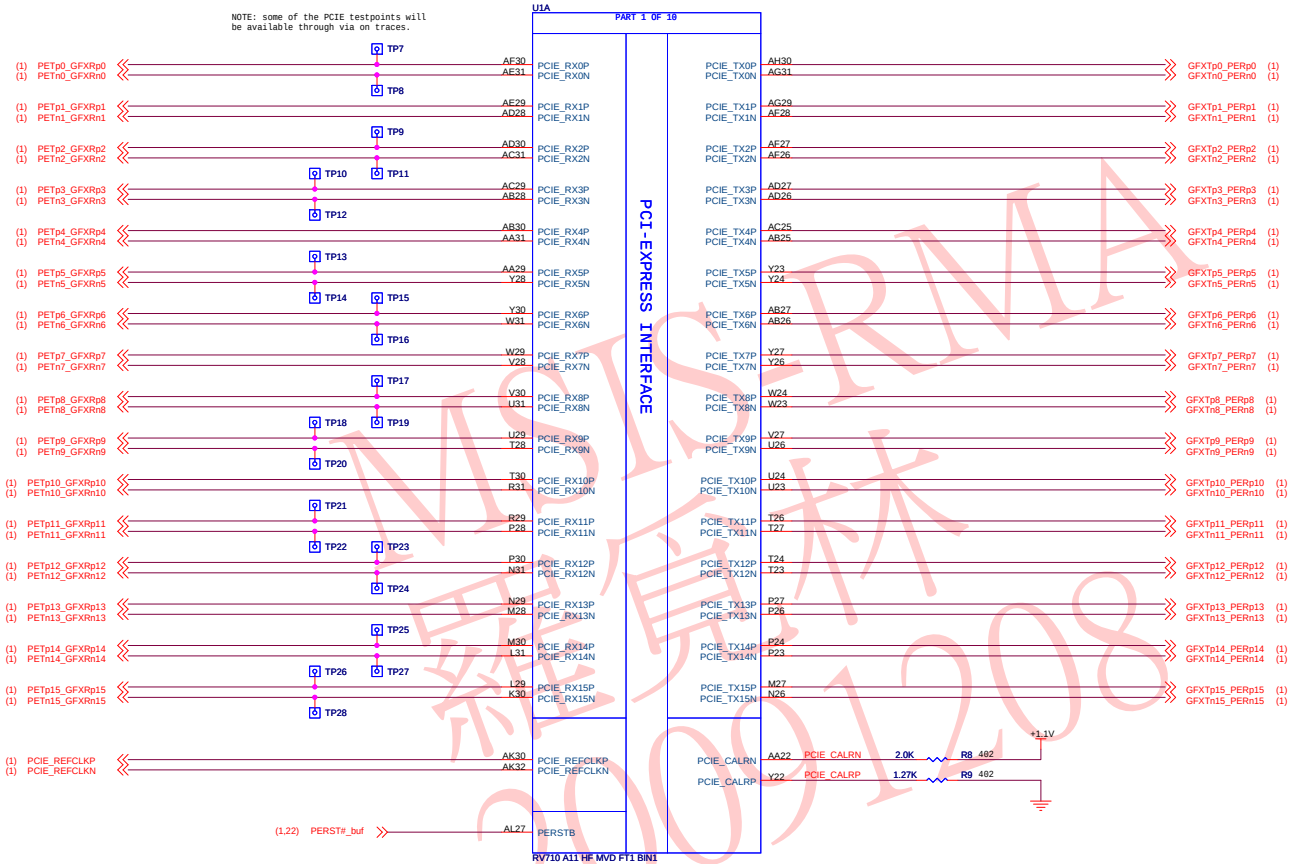
(2) RV710 PCIE Interface



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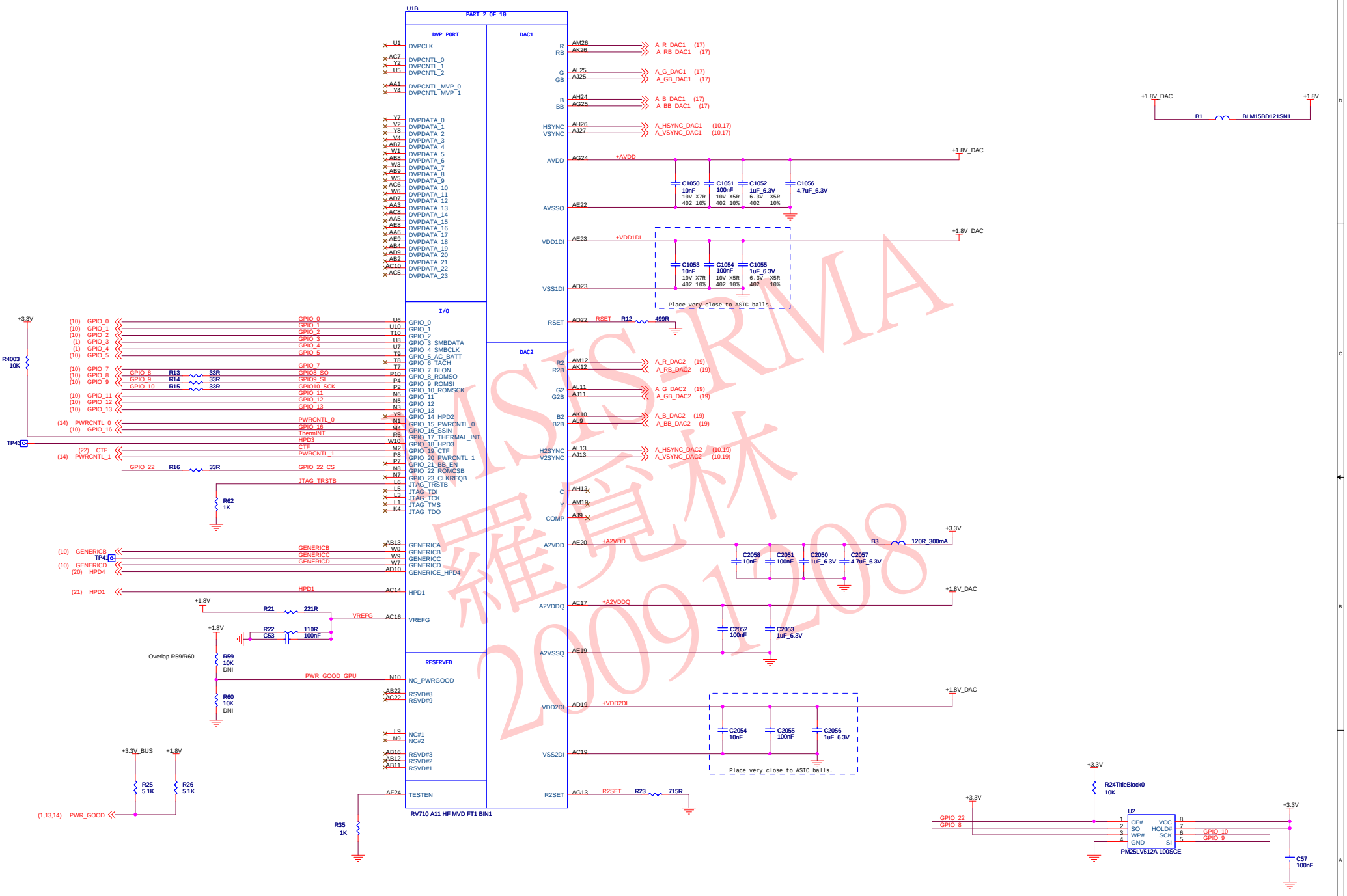
(3) RV710 Main



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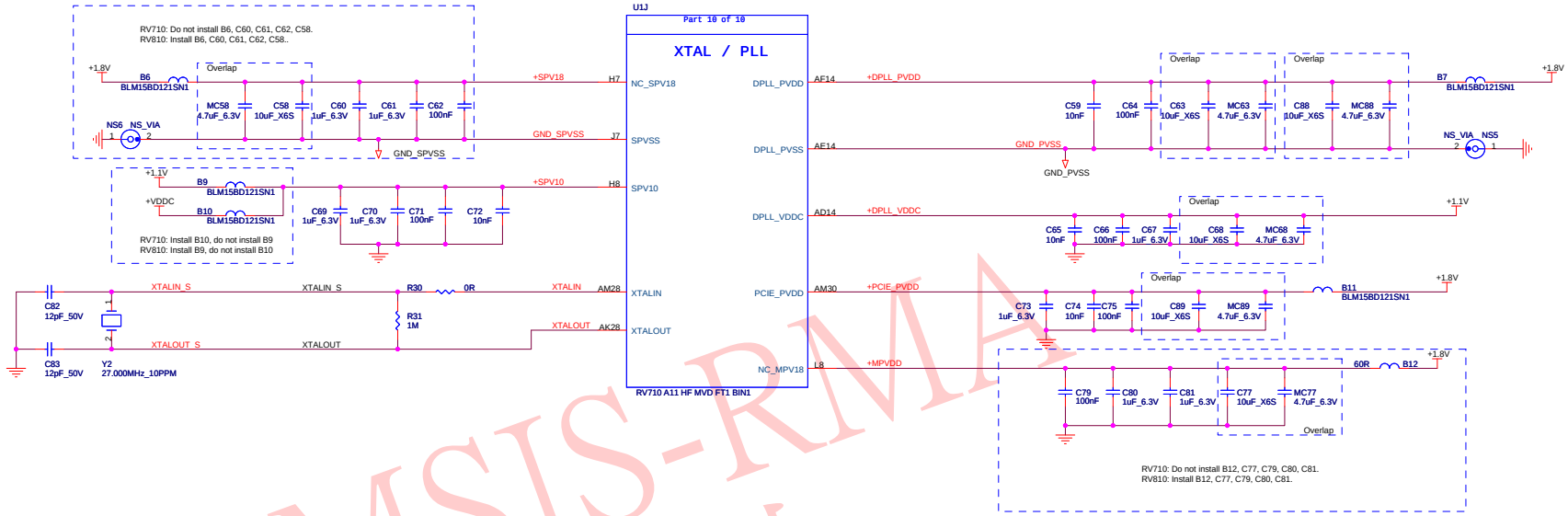
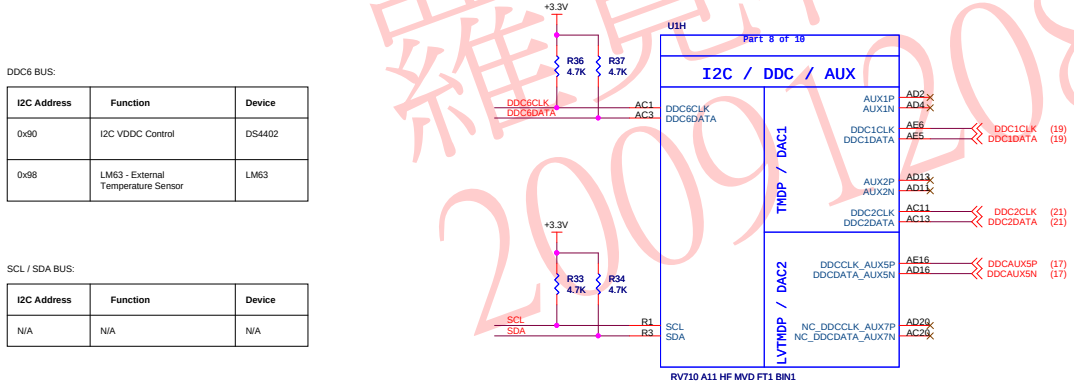
(04) RV710 GPIOs CF XTAL



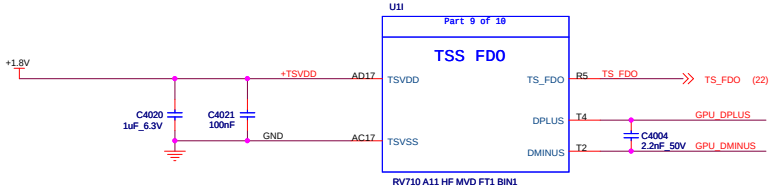


DDC6 BUS:

I2C Address	Function	Device
0x90	I2C VDDC Control	DS4402
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A



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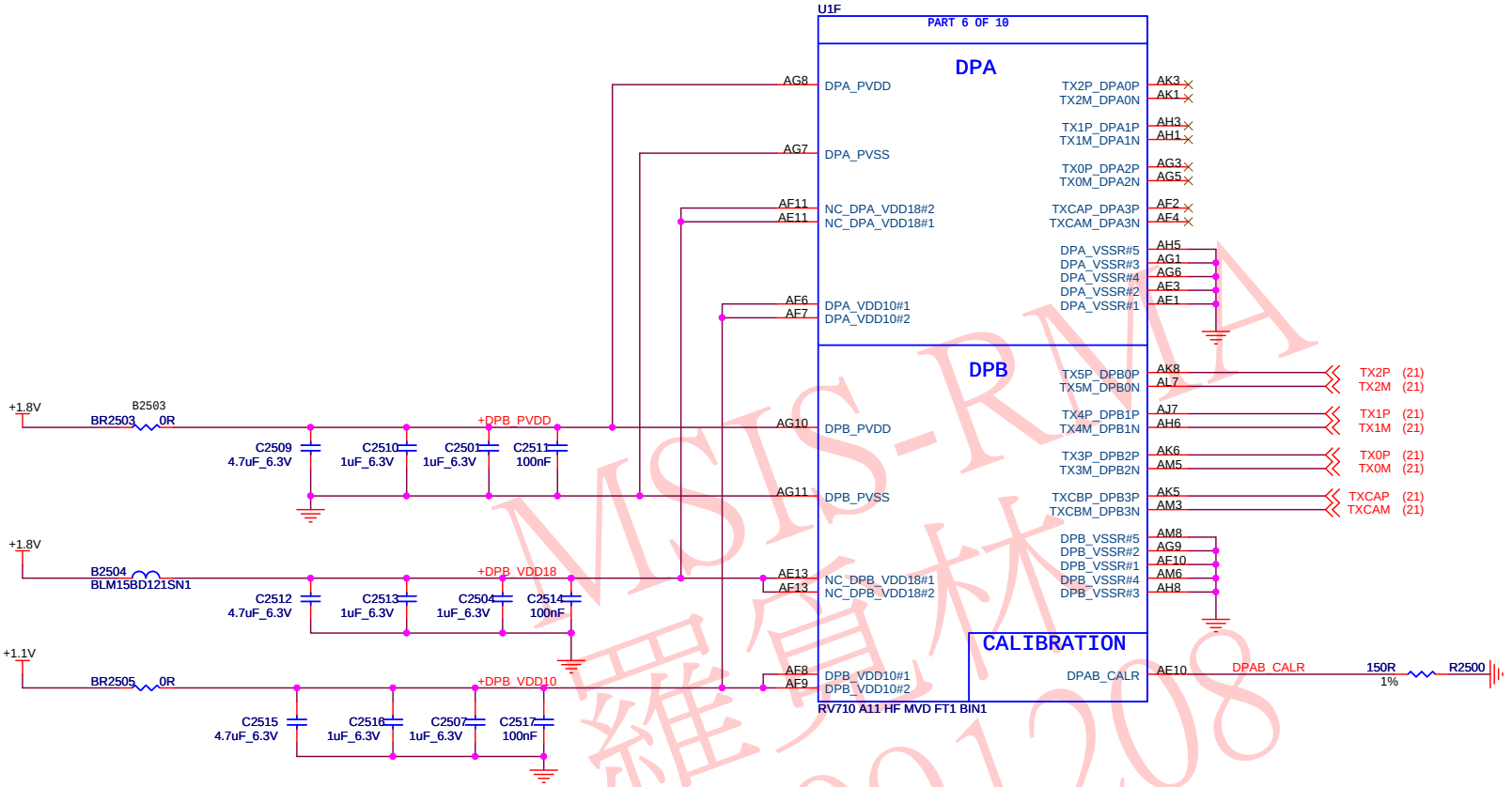
(05) RV710 TMDP A&B

TMDP INTERFACE



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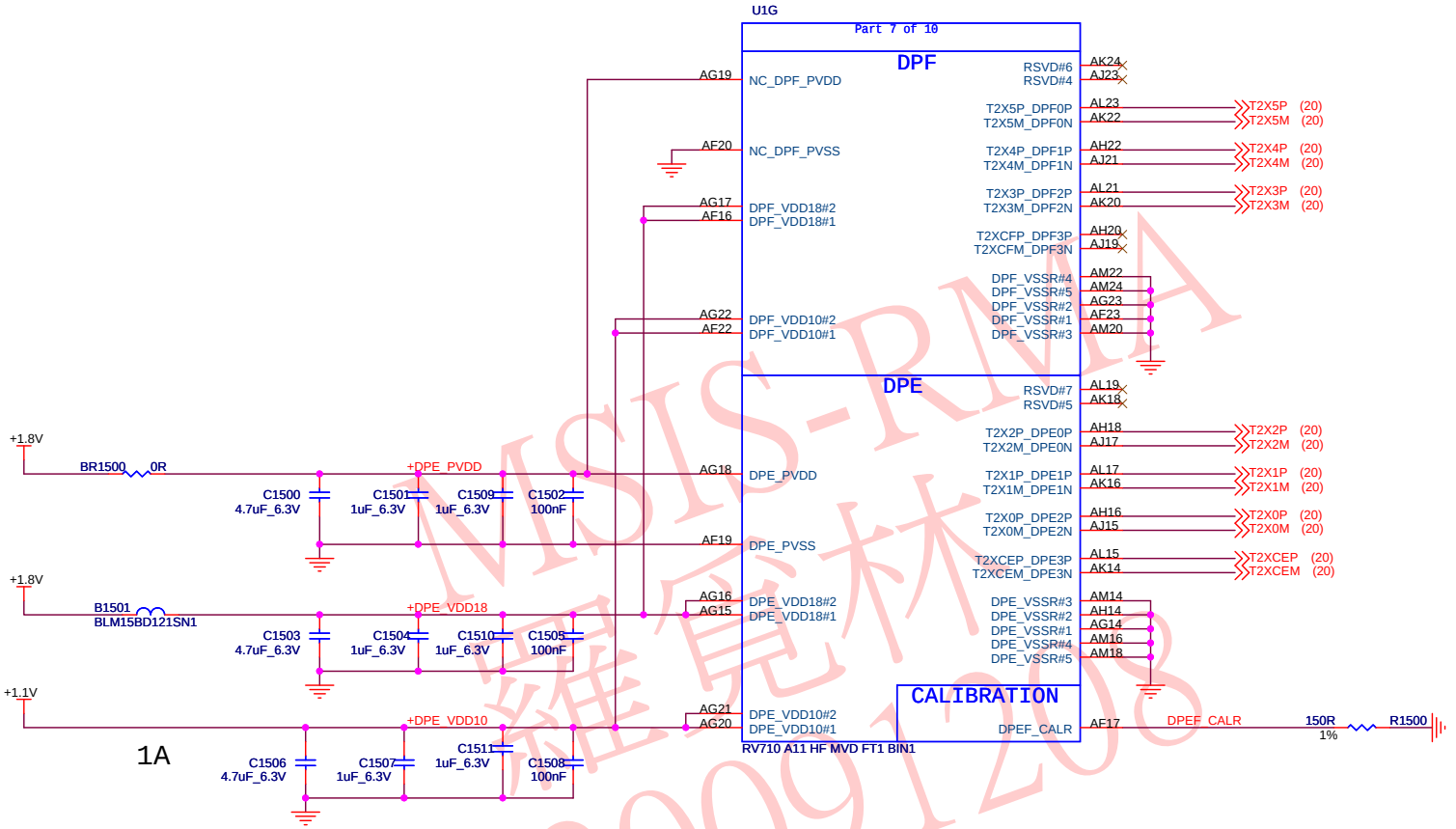
(06) RV710 TMDP E&F

LVTMDP INTERFACE



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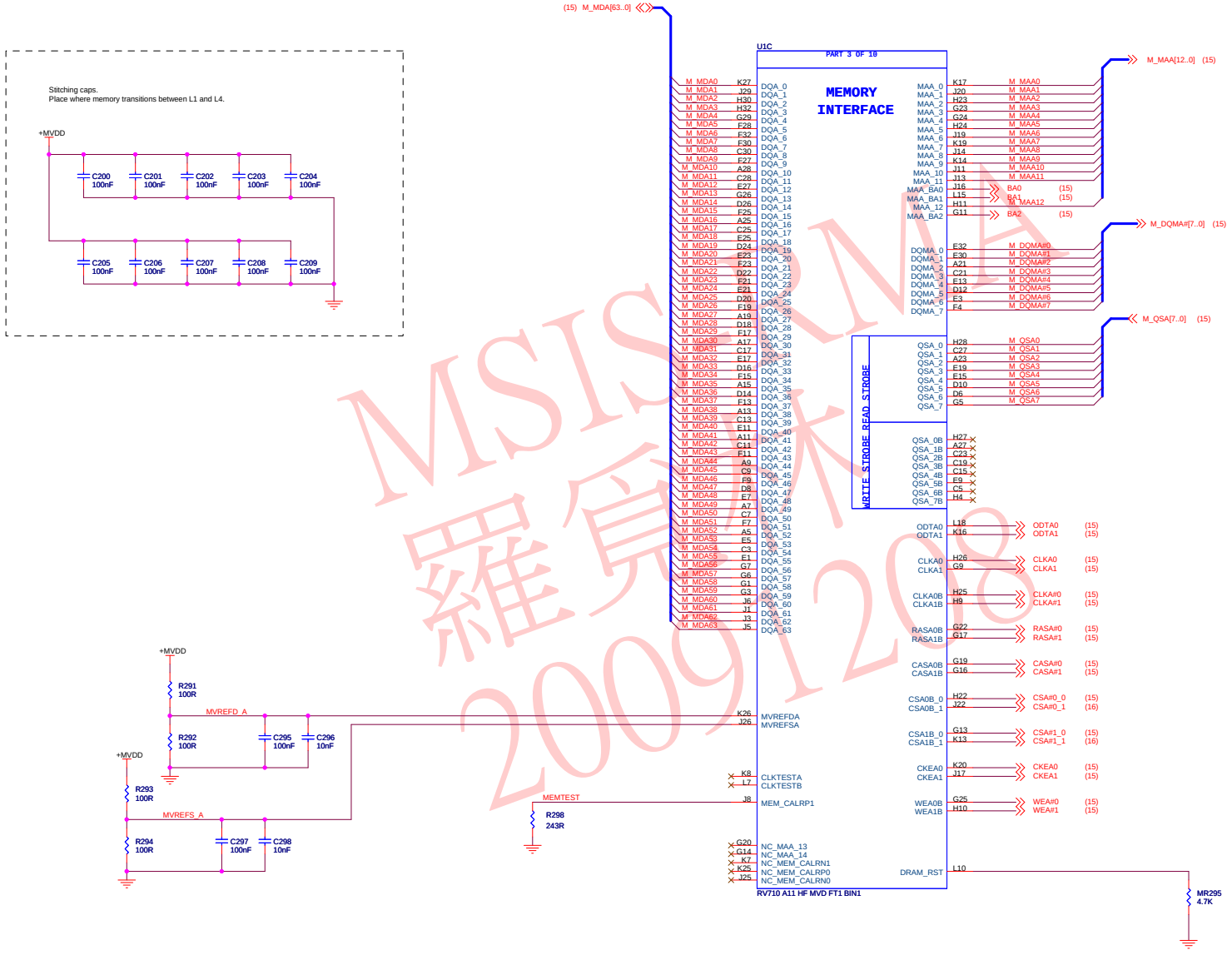
(07) RV710 MEM Interface Ch A

COPY FROM V161 2.1 DDR2 SCH.

MEMORY INTERFACE



DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R

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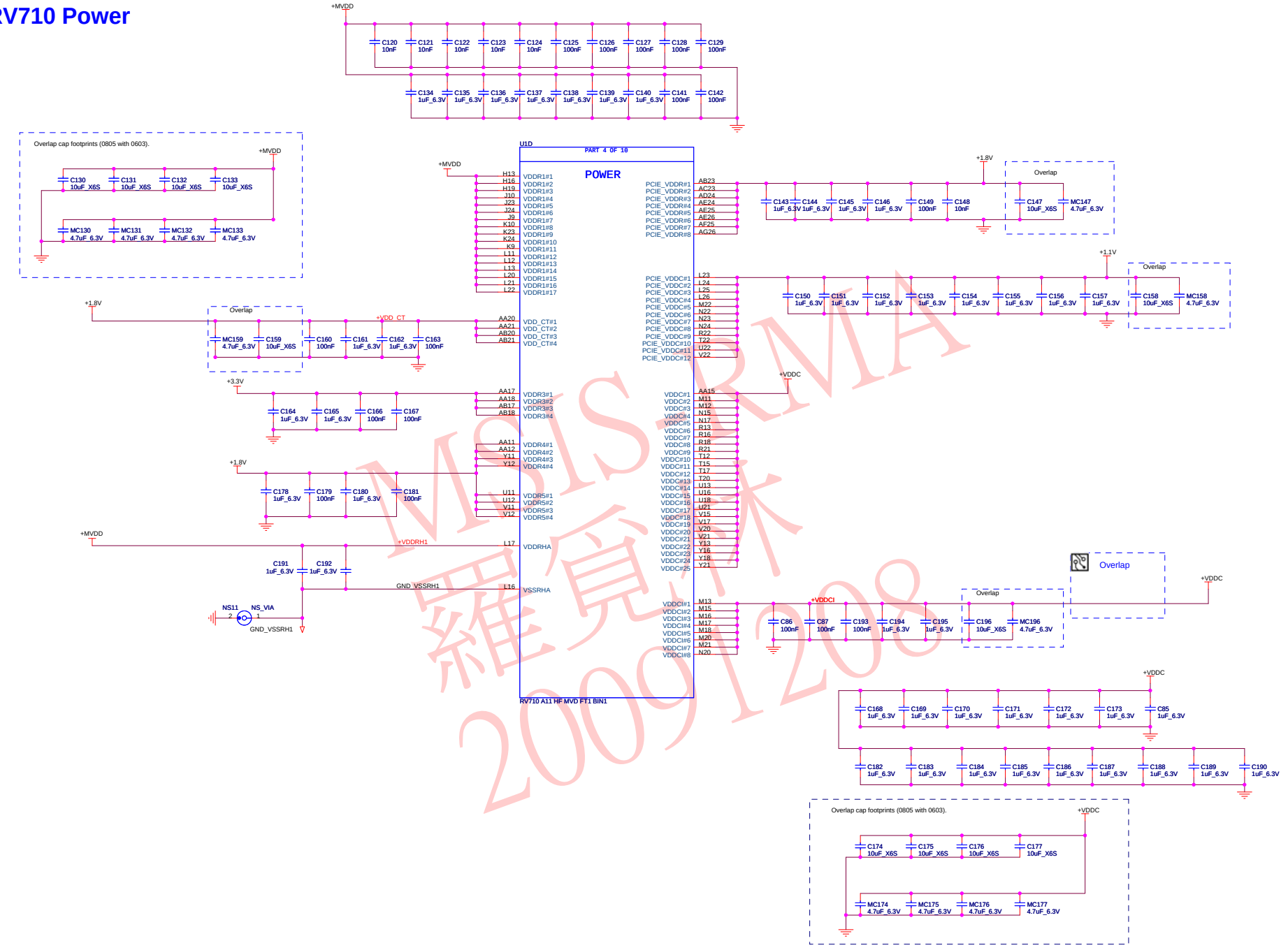
(08) RV710 Power



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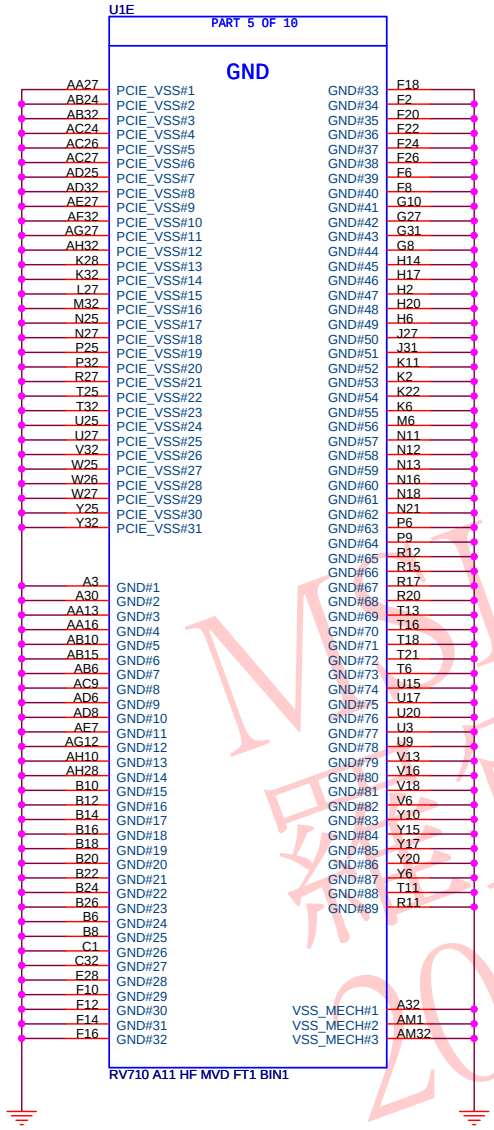
(09) RV710 GND



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(10) RV710 STRAPS

PIN BASED STRAPS

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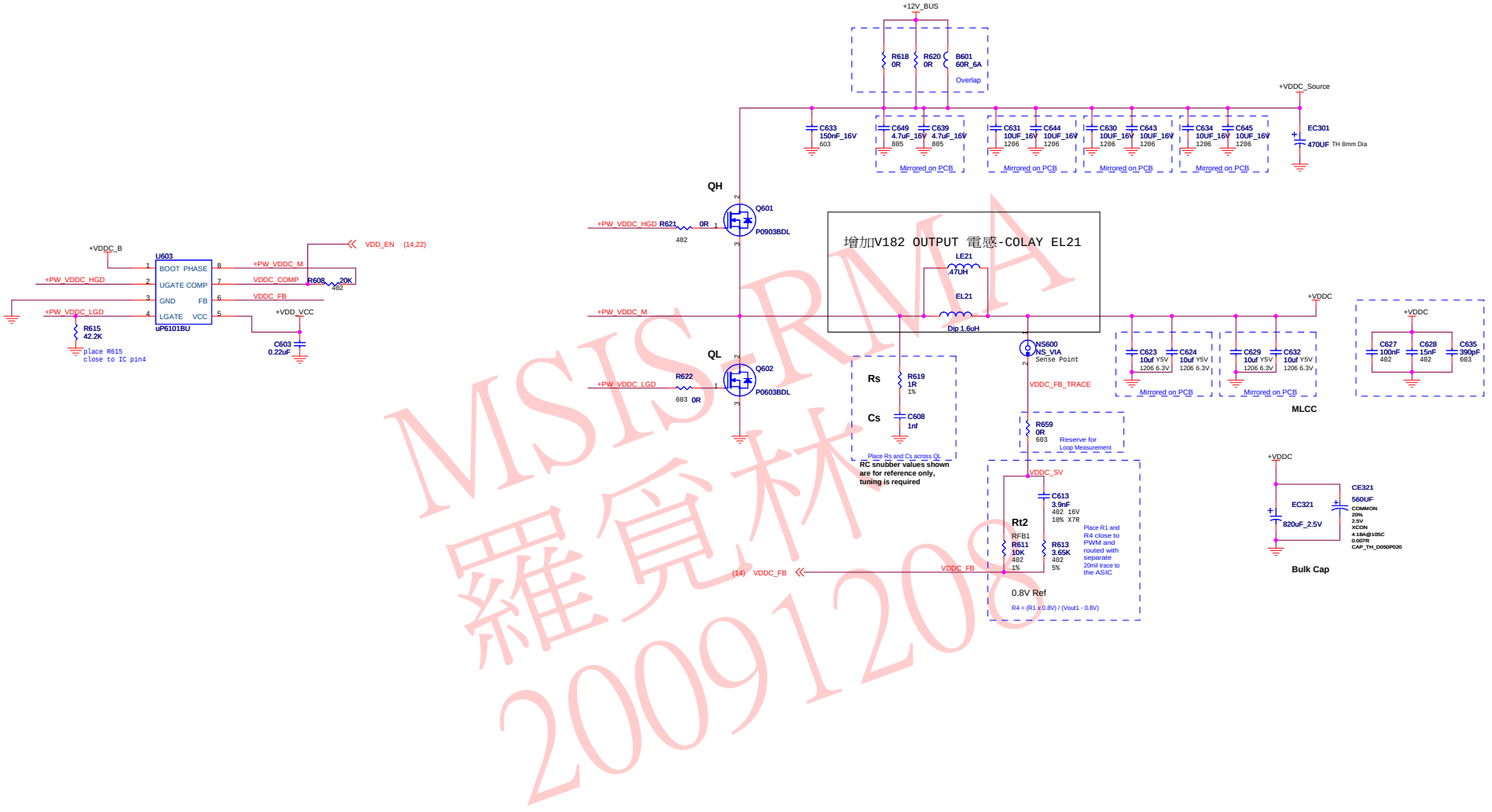
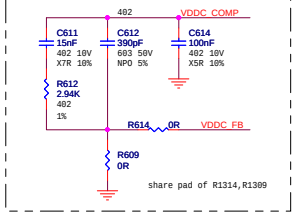
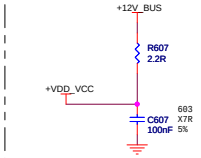
(11) VDDC



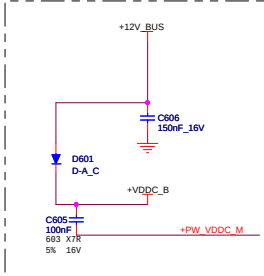
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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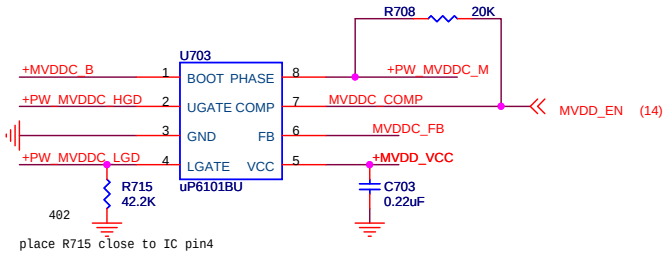
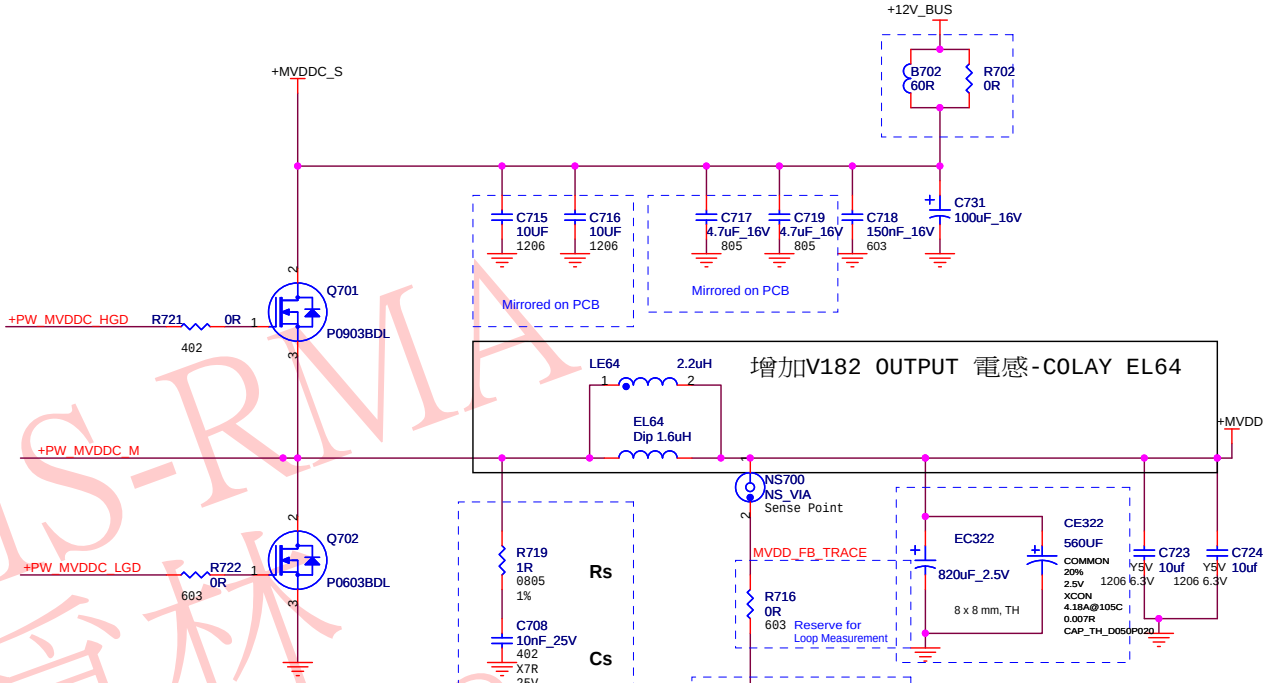
(12) MVDD

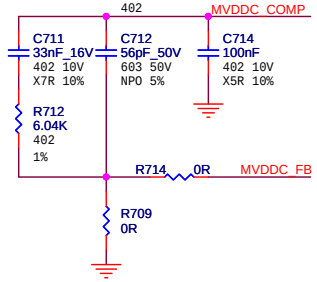


Layout guideline

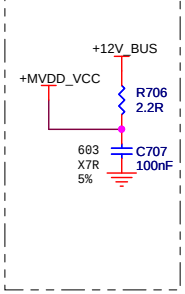
1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



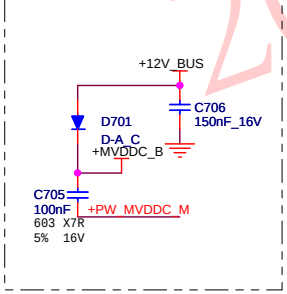
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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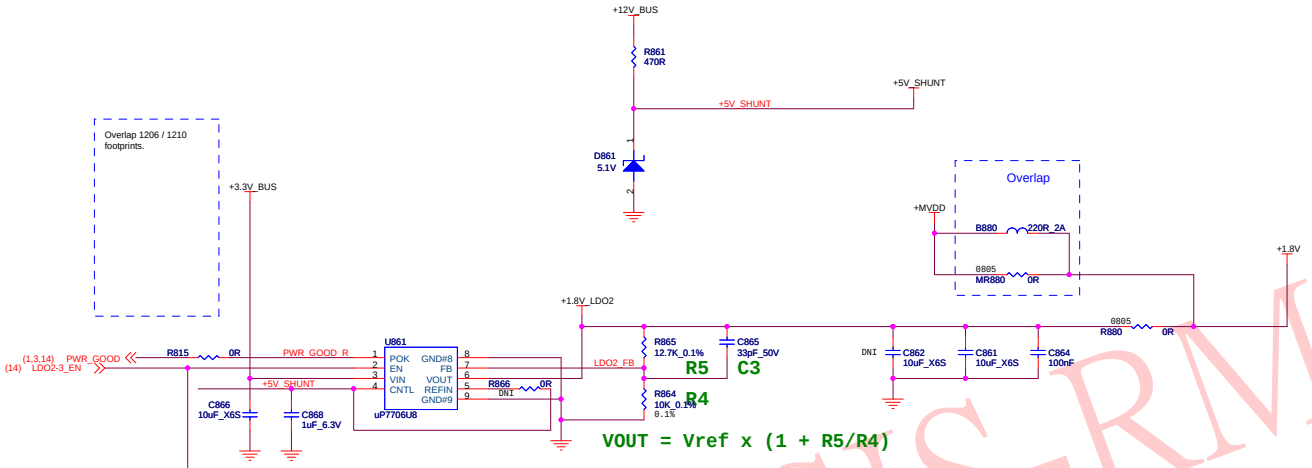
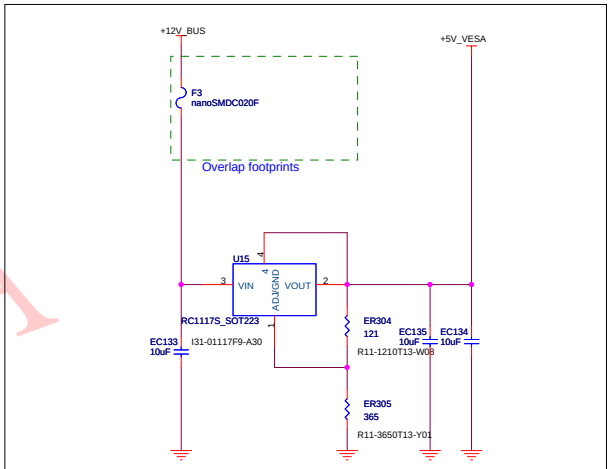
(13) Linear Regulators

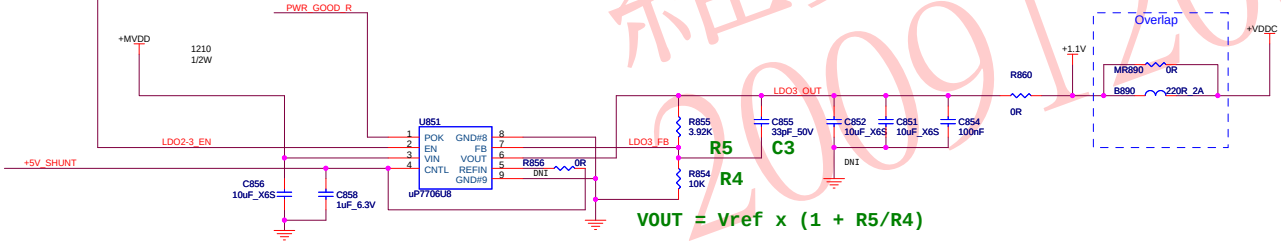
LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

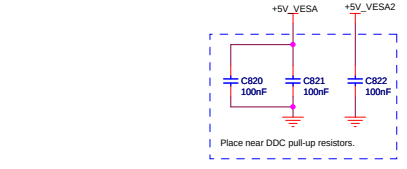


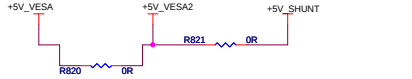
Regulators for +5V_VESA

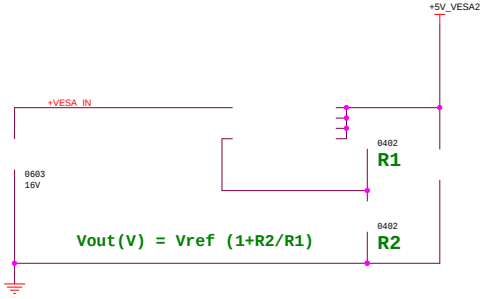


LDO #3: Vin = +1.4V to 2.087VMAX Vout = +1.1V +/- 2.5% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling









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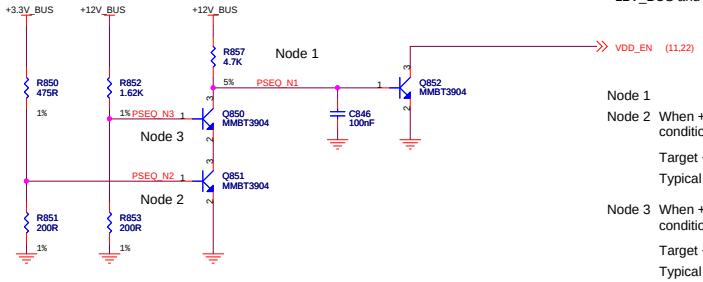
(14) Power Management

Power up/down Sequencing

Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.



Node 1

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

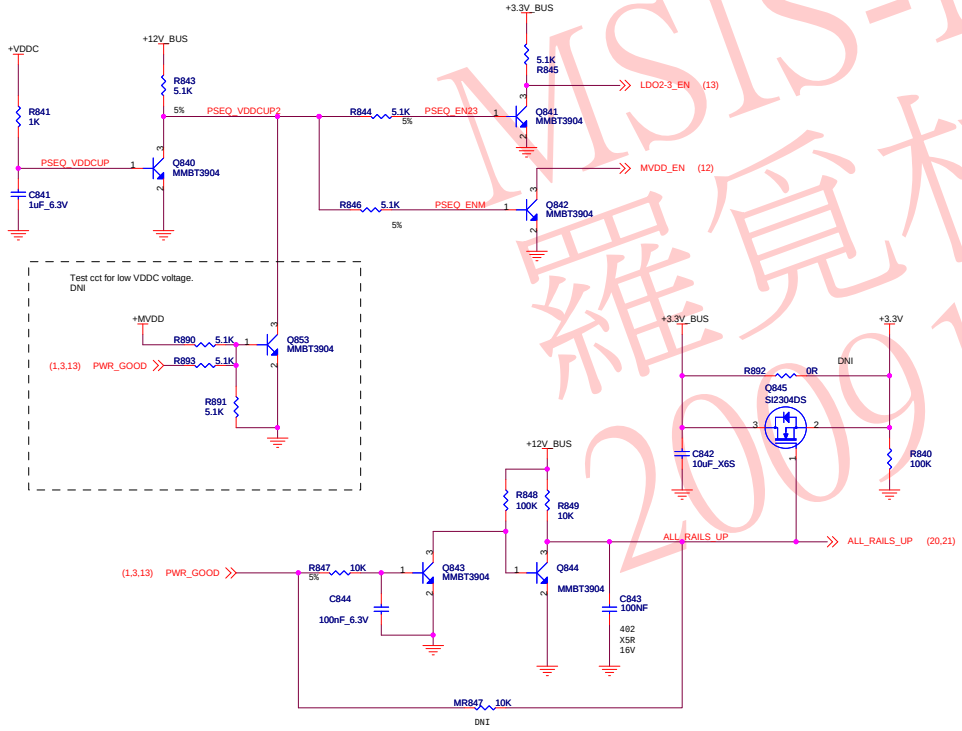
Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

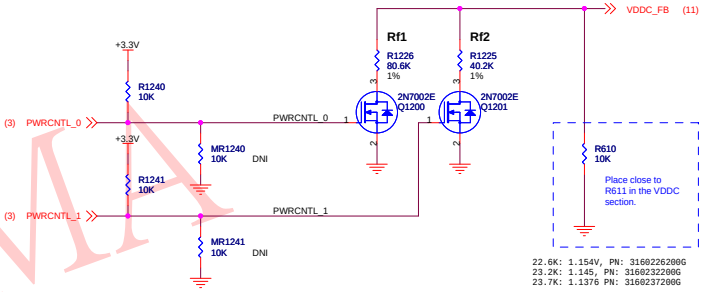
When +12V_BUS ramps above min Vbe, SMPS_EN will be held low



Power Play

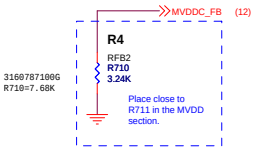
VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0	0				
0	1				
1	0				
1	1	1 0 1			Power-up Default



MVDD Voltage Settings Using GPIOs

PWRCNTL_2 GPIO_6	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0				
1	1 0 1			Power-up Default



3160787100G
R710=7.68K

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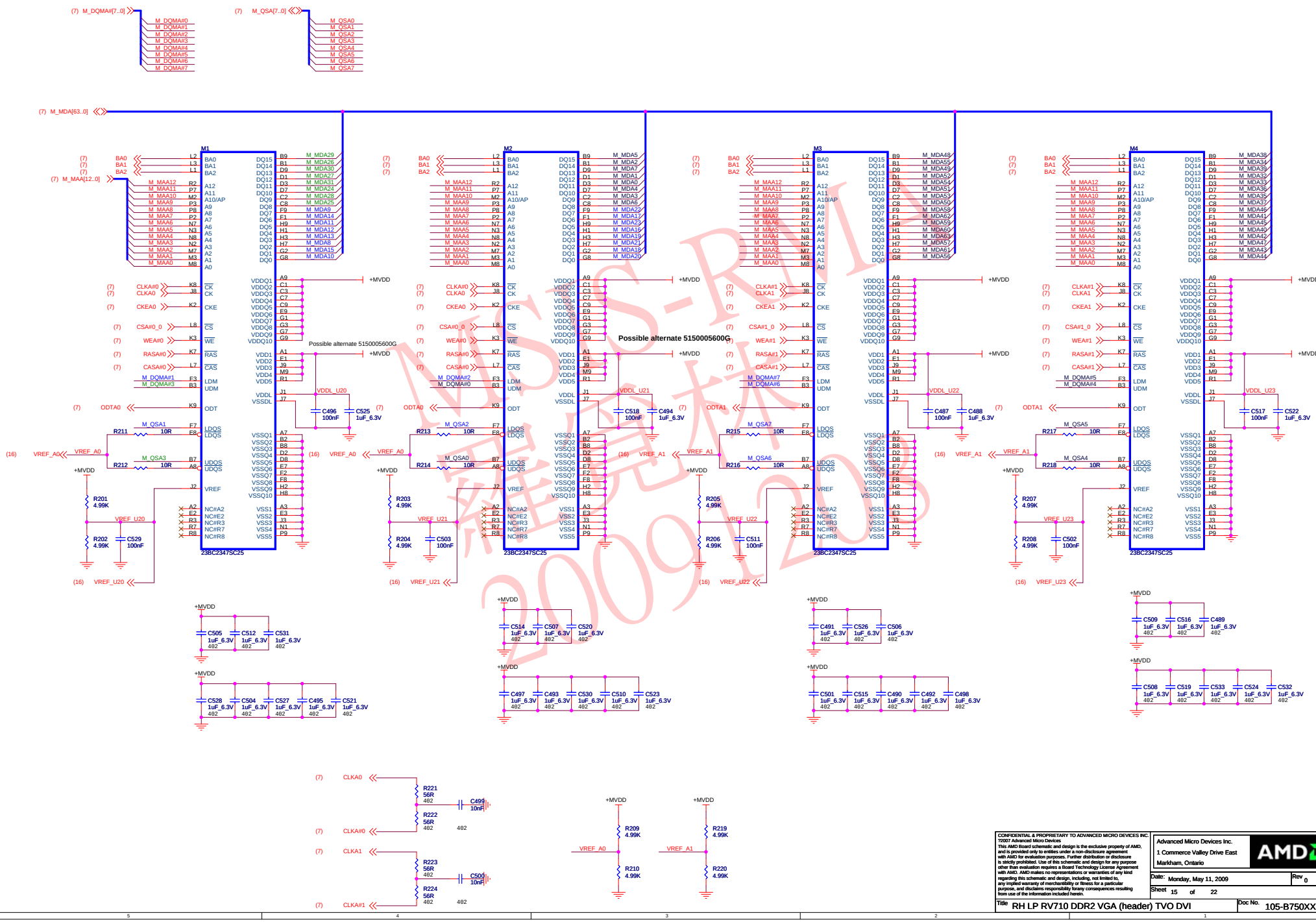
CHANNEL A: RANK 0 512MB DDR2

MAX DENSITY: 64Mx16



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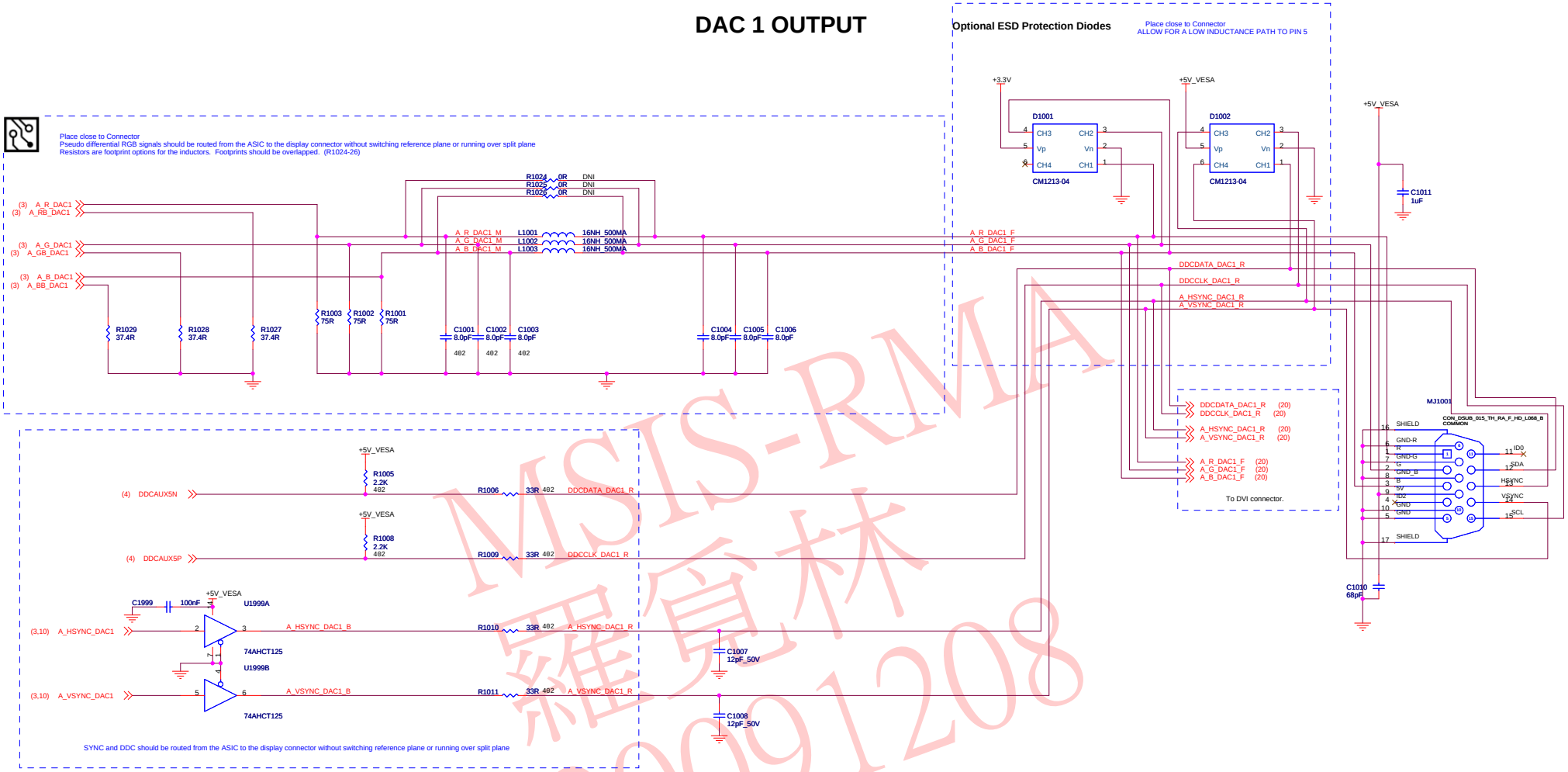
(18) DAC1 OUTPUT

DAC 1 OUTPUT



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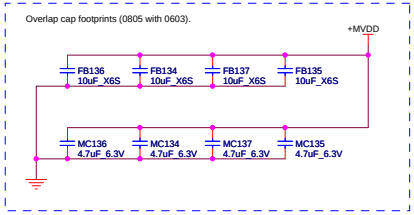
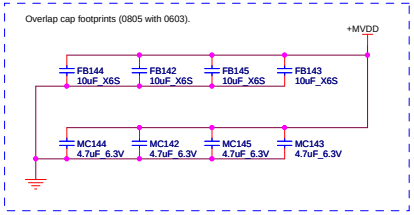
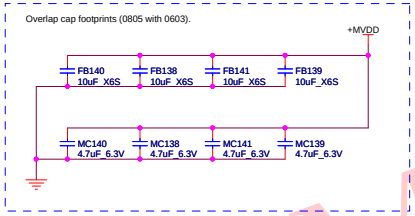
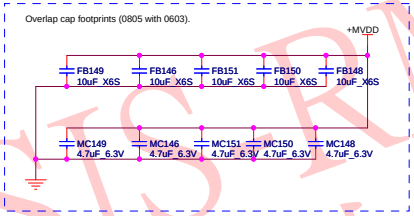
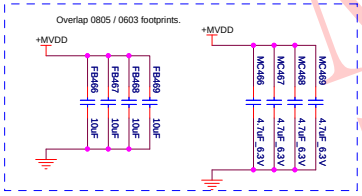
(17) DDR3 Termination

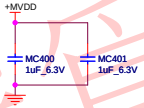












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(19) DAC2 OUTPUT

DAC 2 OUTPUT

Optional ESD Protection Diodes

Place near D2002, D2003, D2004, D2005

Place close to Connector

Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane

(3) A_R_DAC2
(3) A_RB_DAC2
(3) A_G_DAC2
(3) A_GB_DAC2
(3) A_B_DAC2
(3) A_BB_DAC2

R2024 0R DNI
R2025 0R DNI
R2026 0R DNI

A_R_DAC2_M L2001 16NH_500MA
A_G_DAC2_M L2002 16NH_500MA
A_B_DAC2_M L2003 16NH_500MA

OVERLAP

R2029 37.4R
R2028 37.4R
R2027 37.4R
R2003 75R
R2002 75R
R2001 75R
C2004 8.0pF
C2005 8.0pF
C2006 8.0pF

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R

+5V_VESA2
C2011 1uF
C2010 68pF

J2
A_R_DAC2_F
A_B_DAC2_F
A_G_DAC2_F
A_HSYNC_DAC2_R
DDCCLK_DAC2_R
DDCDATA_DAC2_R
A_VSYNC_DAC2_R
Header_16_Pin_2X8

2X8 HEADER FOR VGA RIBBON CONNECTOR

RV710: DDC2 is 5V tolerant. Do not install level shifter.
--> Do not install R2013, R2015, Q2001, Q2002. Install R2014, R2016.
RV810: DDC2 is NOT 5V tolerant. Install level shifter.
--> Do not install R2014, R2016. Install R2013, R2015, Q2001, Q2002.

+3.3V
R2014 0R
R2013 10K
BSH111 Q2001
+5V_VESA2
R2005 2.2K 402
(4) DDC1DATA
R2006 33R 402 DDCDATA_DAC2_R

R2016 0R
R2015 10K
BSH111 Q2002
R2008 2.2K 402
(4) DDC1CLK
R2009 33R 402 DDCCLK_DAC2_R

U1999C 74AHCT125
(3,10) A_HSYNC_DAC2
A_HSYNC_DAC2_B
R2010 33R 402 A_HSYNC_DAC2_R
C2007 12pF_50V

U1999D 74AHCT125
(3,10) A_VSYNC_DAC2
A_VSYNC_DAC2_B
R2011 33R 402 A_VSYNC_DAC2_R
C2008 12pF_50V

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

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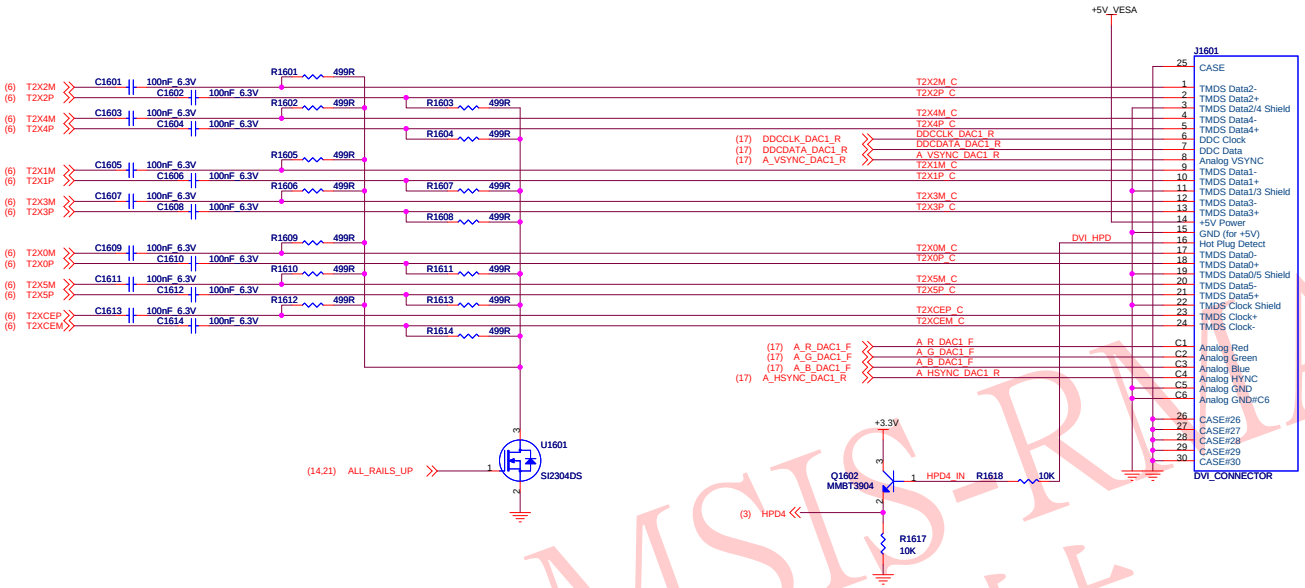
(20) DVI OUTPUT

DPE / DPF OUTPUT



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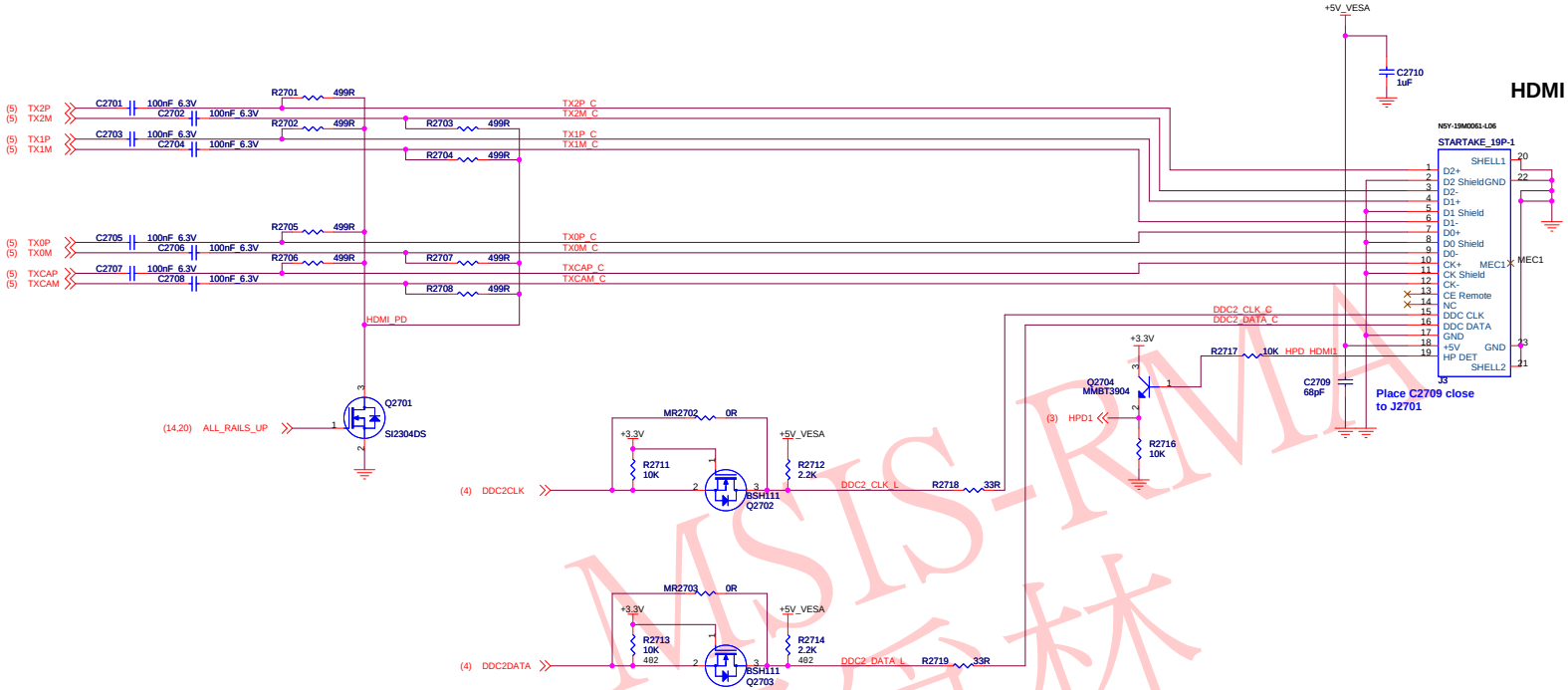
(21) HDMI OUTPUT

TMDP-B OUTPUT



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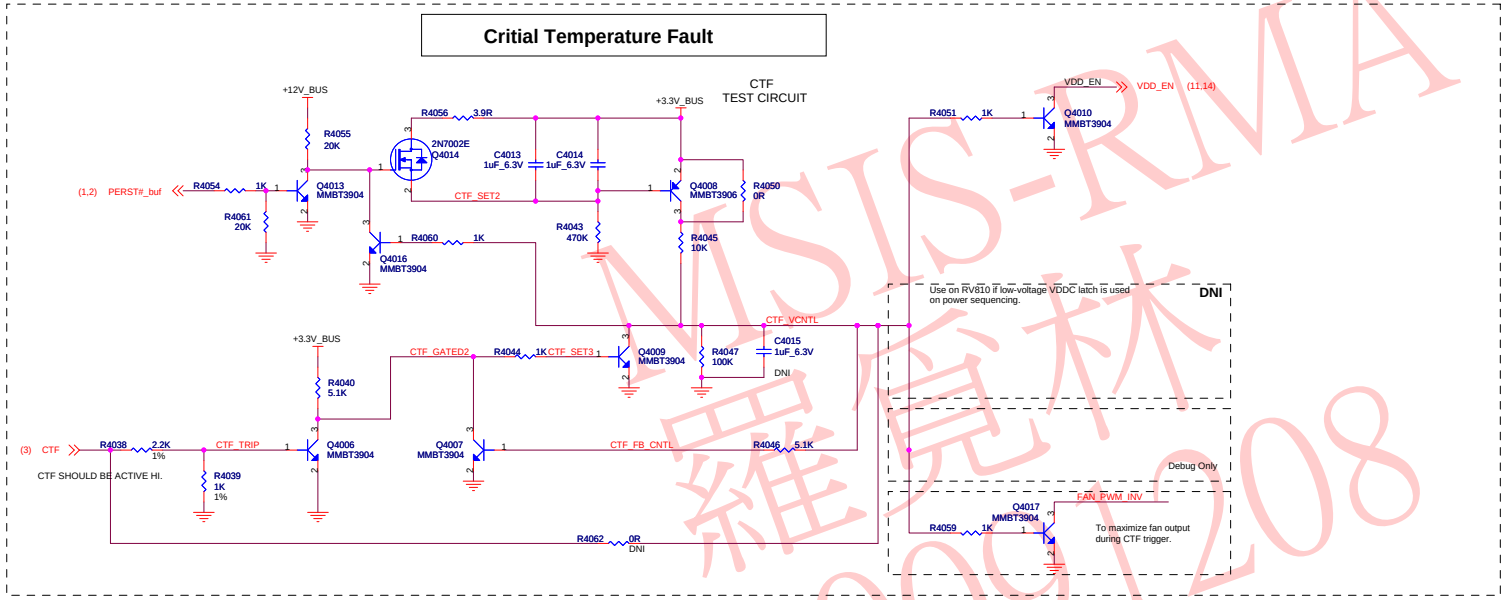
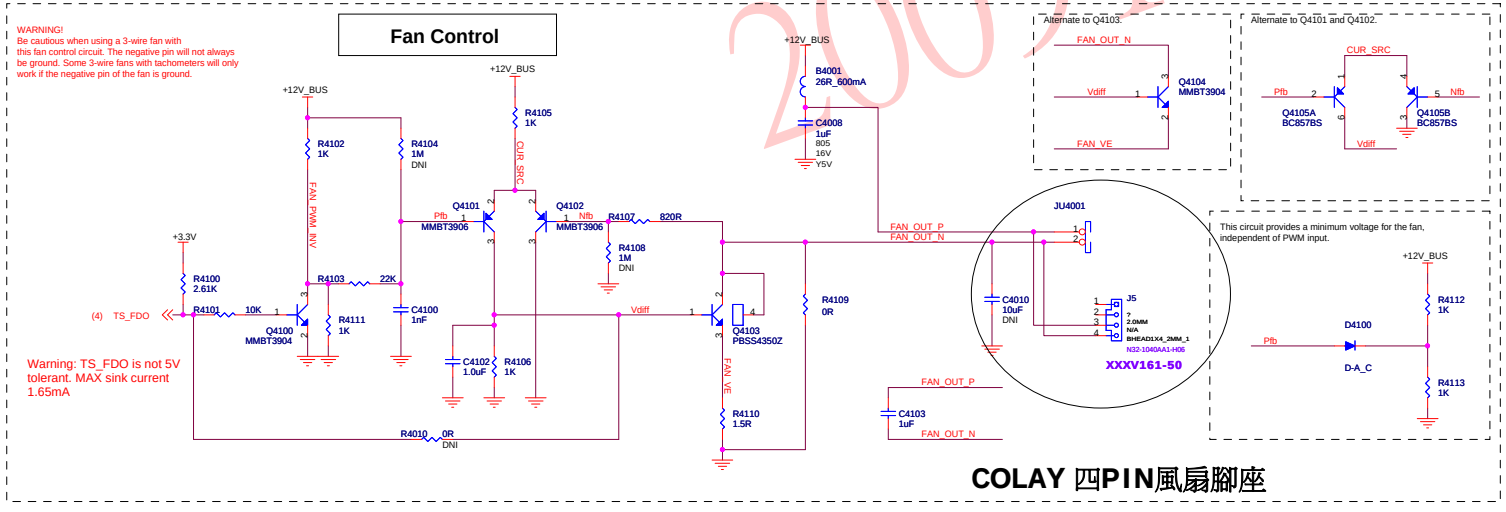
(22) Thermal Management





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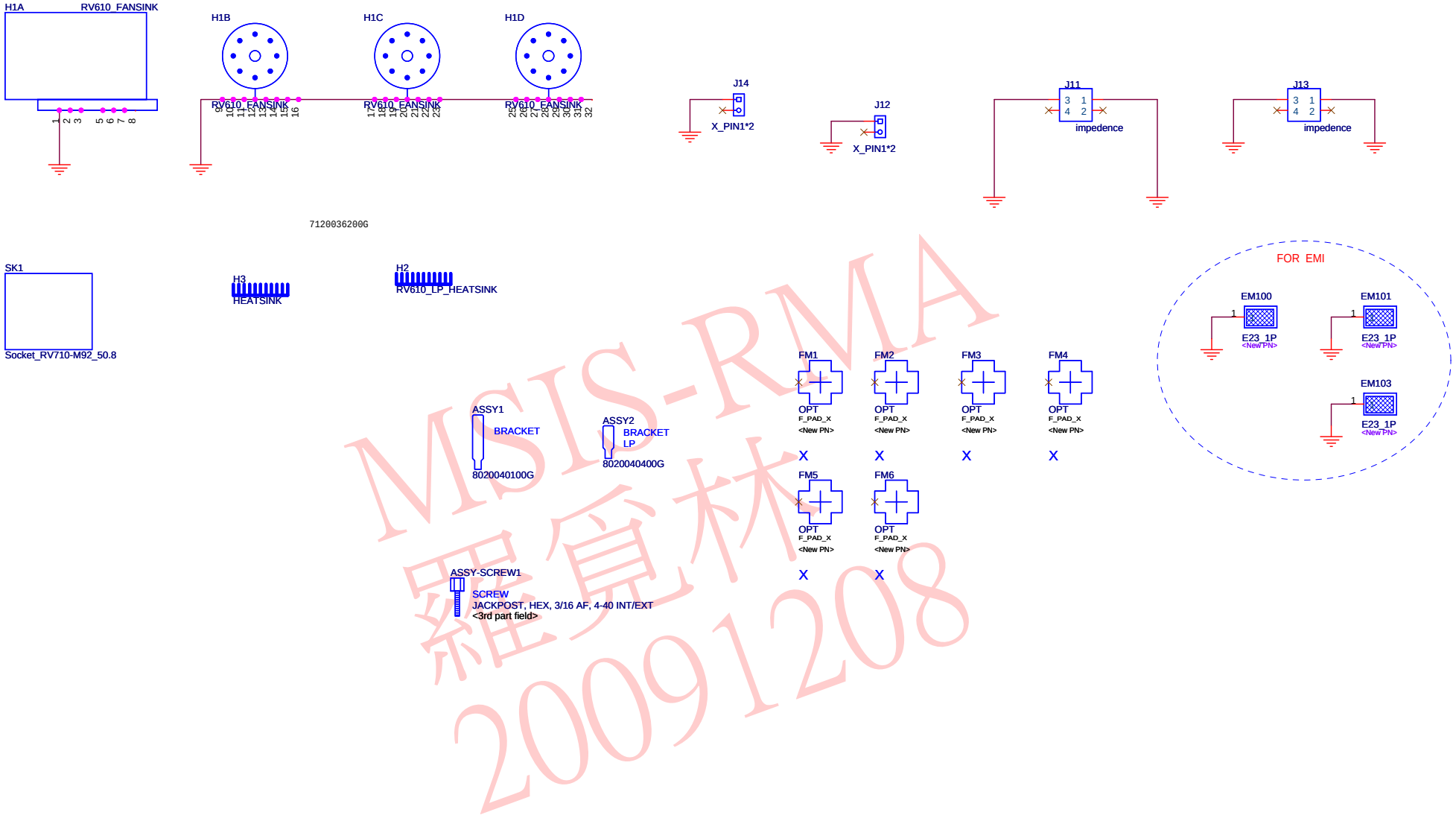

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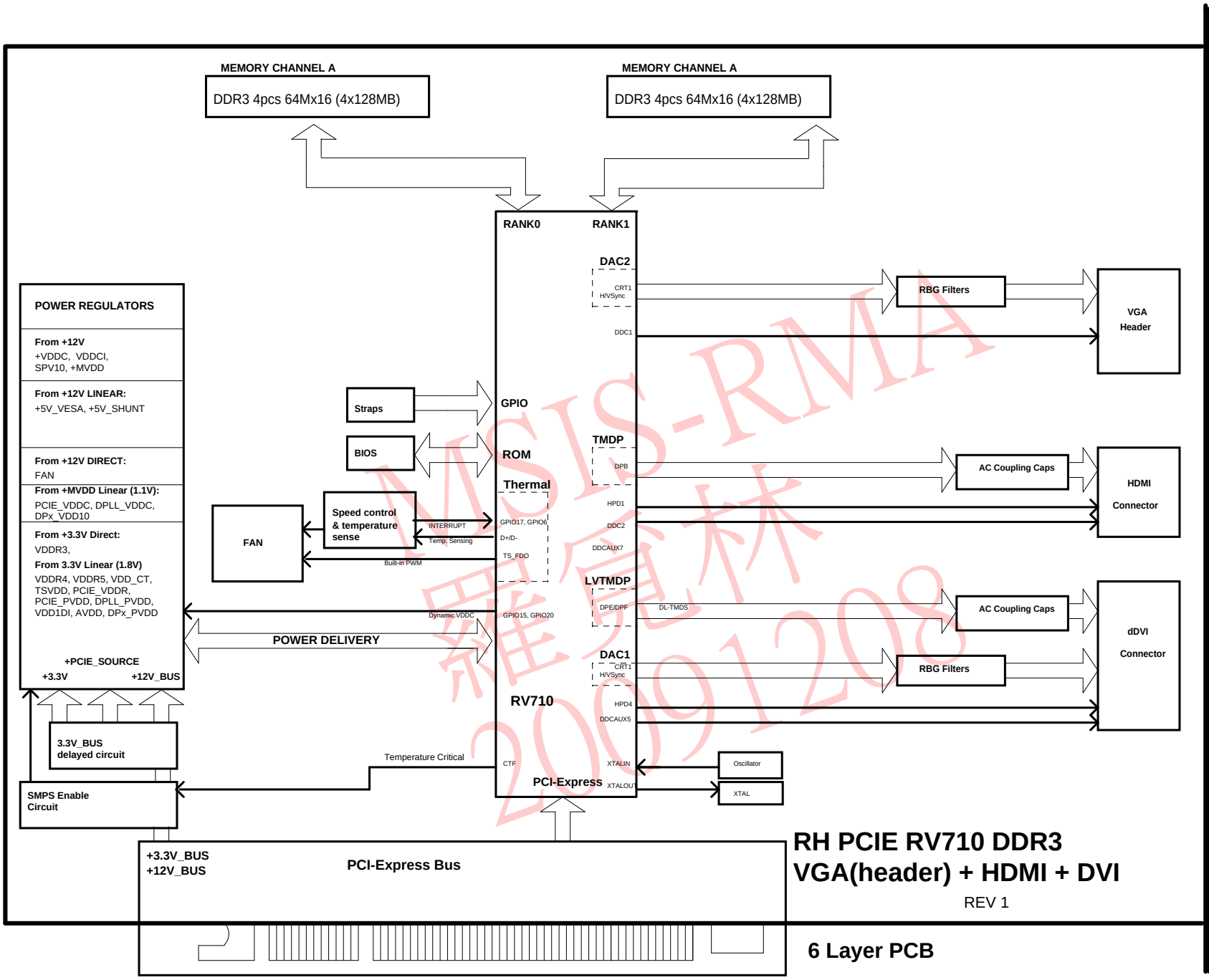

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Title	Schematic No.	Date:
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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

RV710 ENGINEERING BOARD

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	2008.12.30	INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.
1	00B	2009.01.22	Sch no change. just modify HDMI connnecro location on PCB