PCI-EXPRESS EDGE CONNECTOR

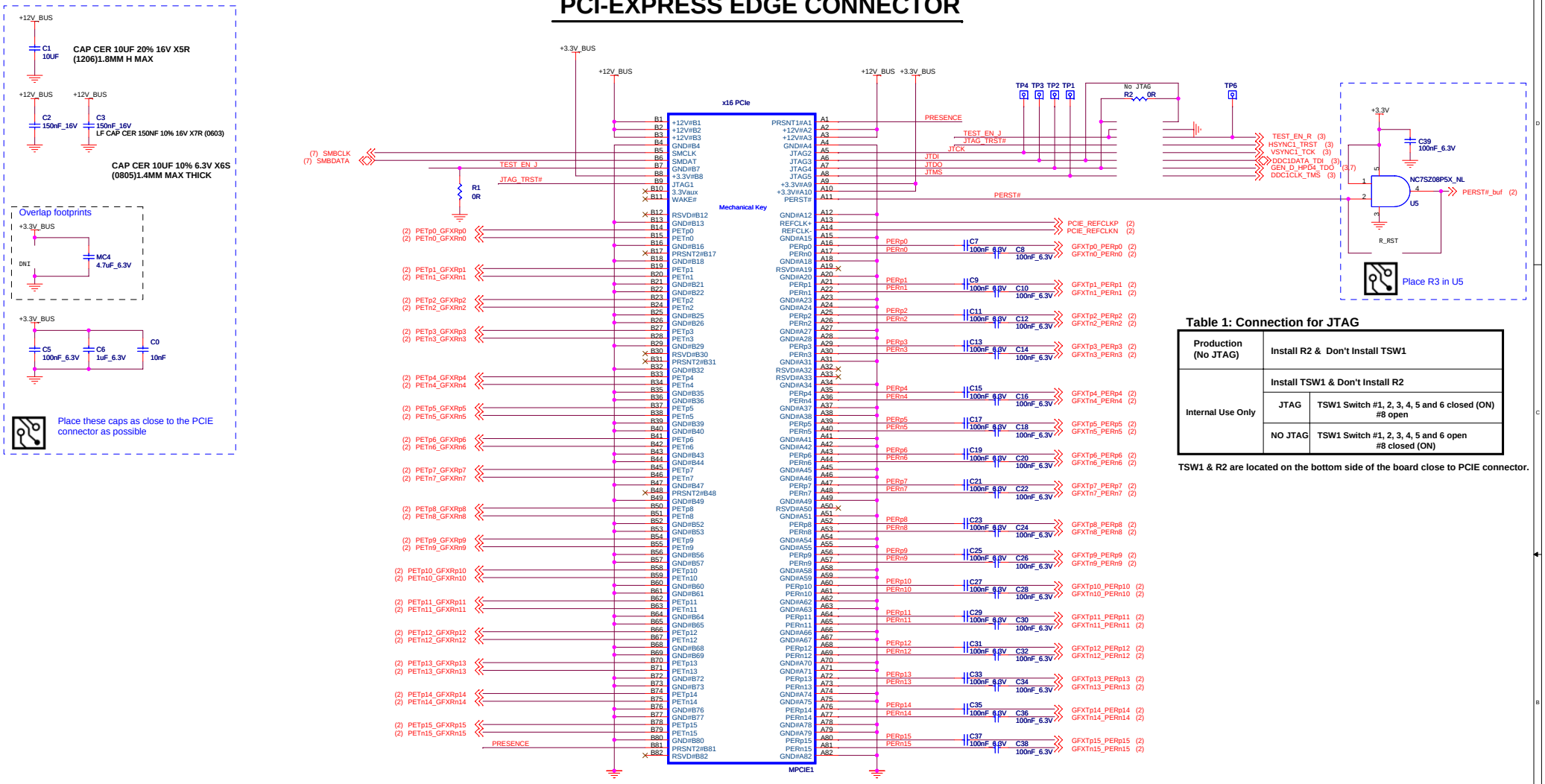

Table 1: Connection for JTAG

Production (No JTAG)	**Install R2 & Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 closed (ON)**

TSW1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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Title	RV635 GDDR3 - PCI-E Edge Connector
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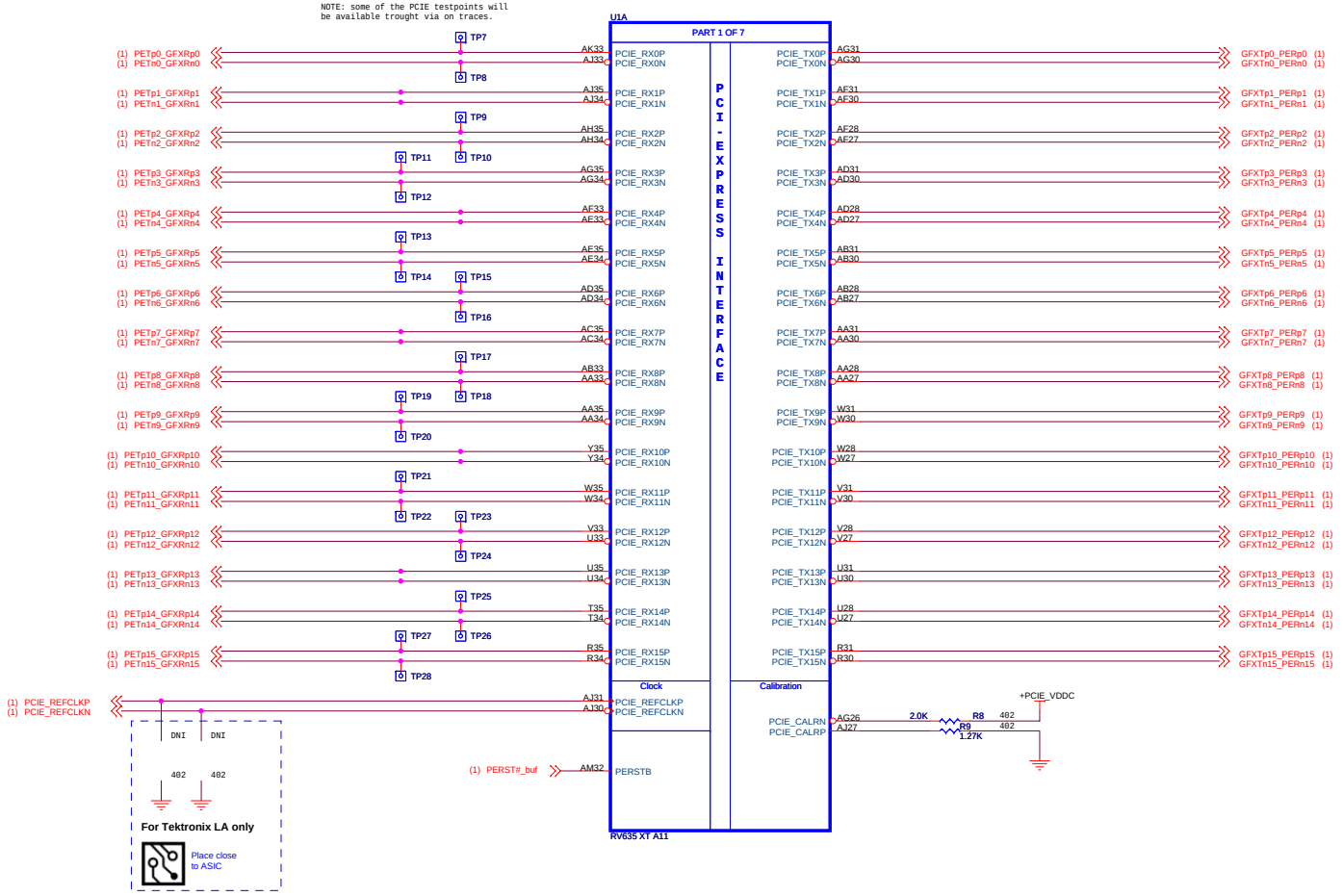

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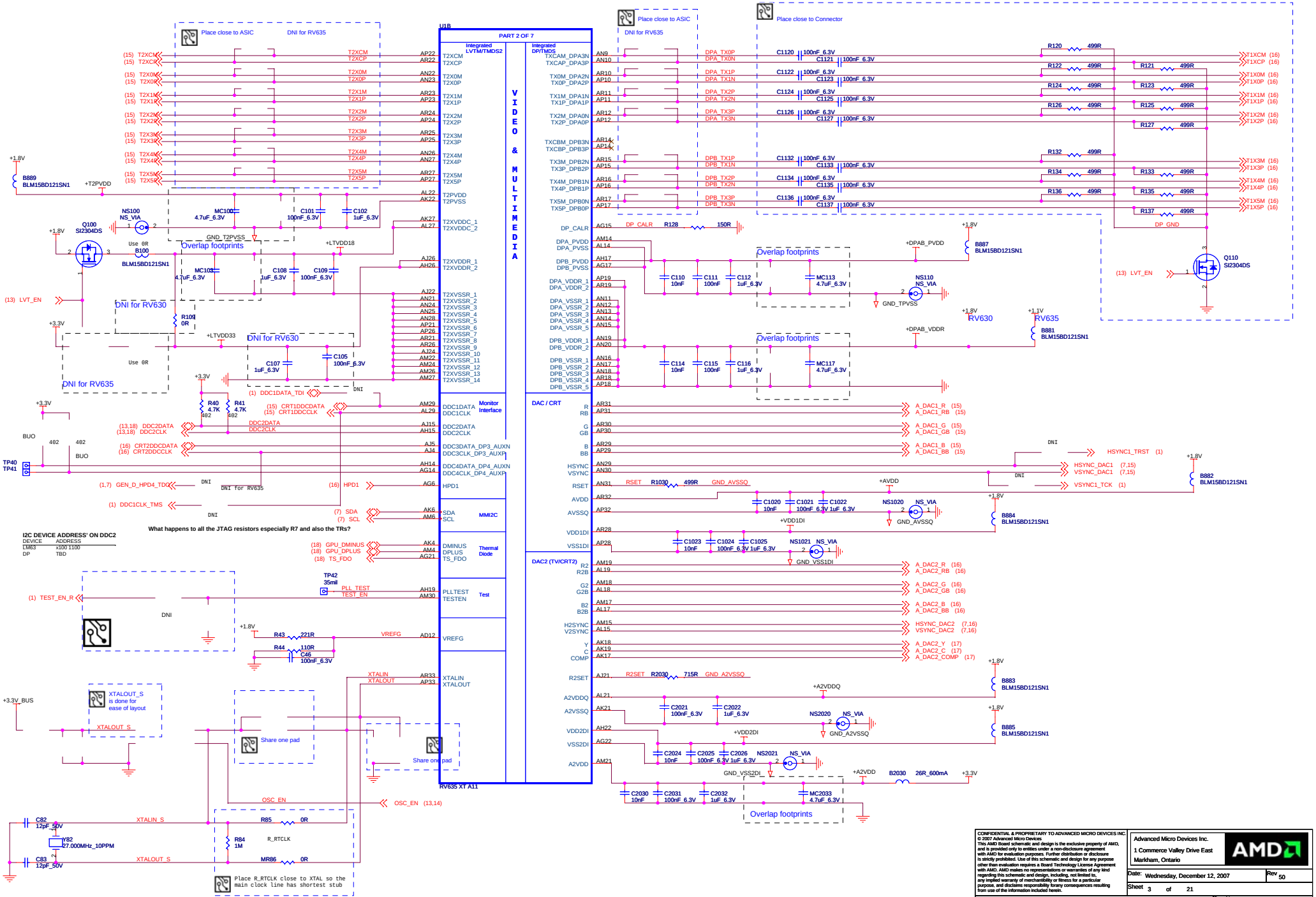
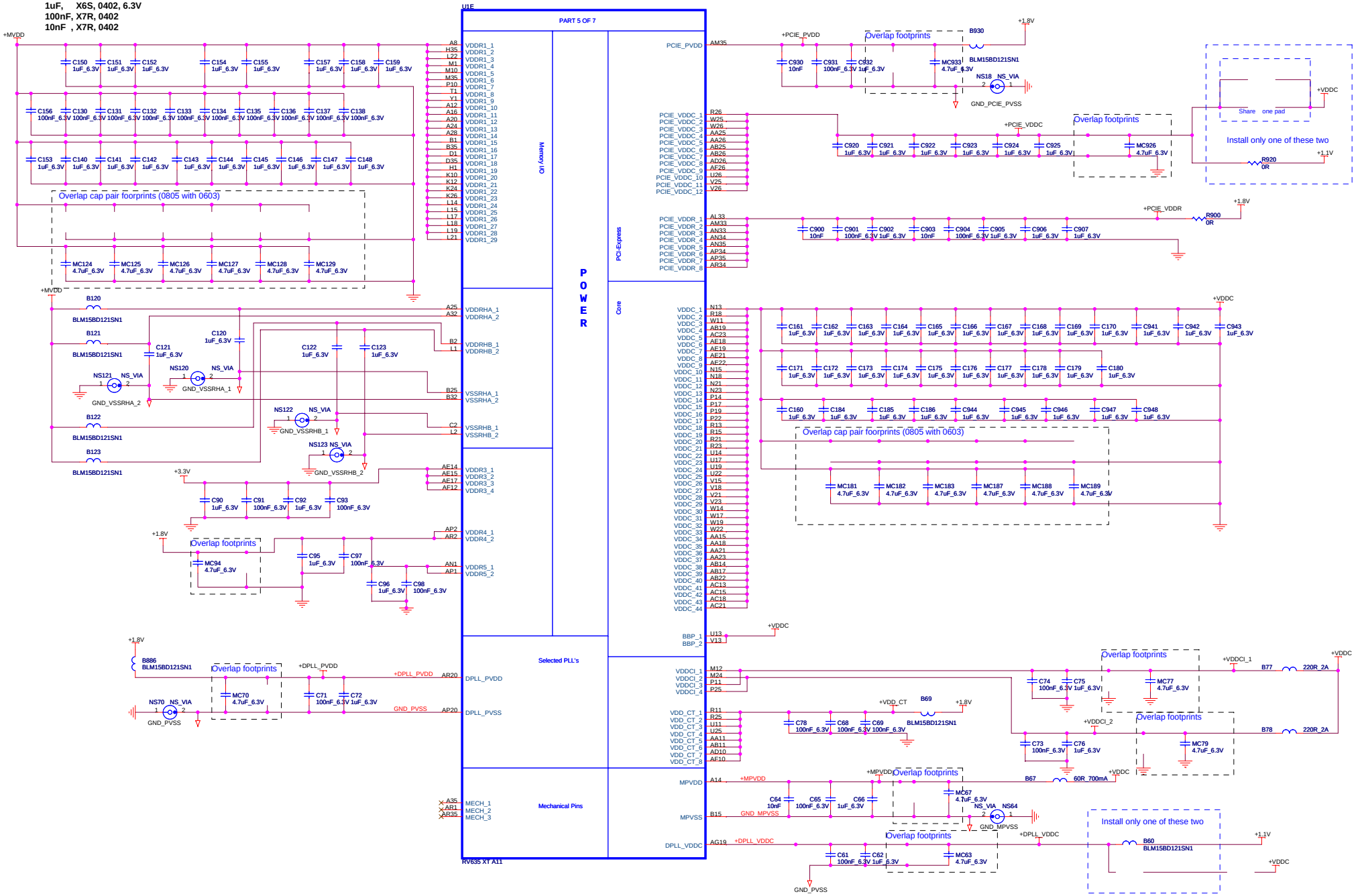
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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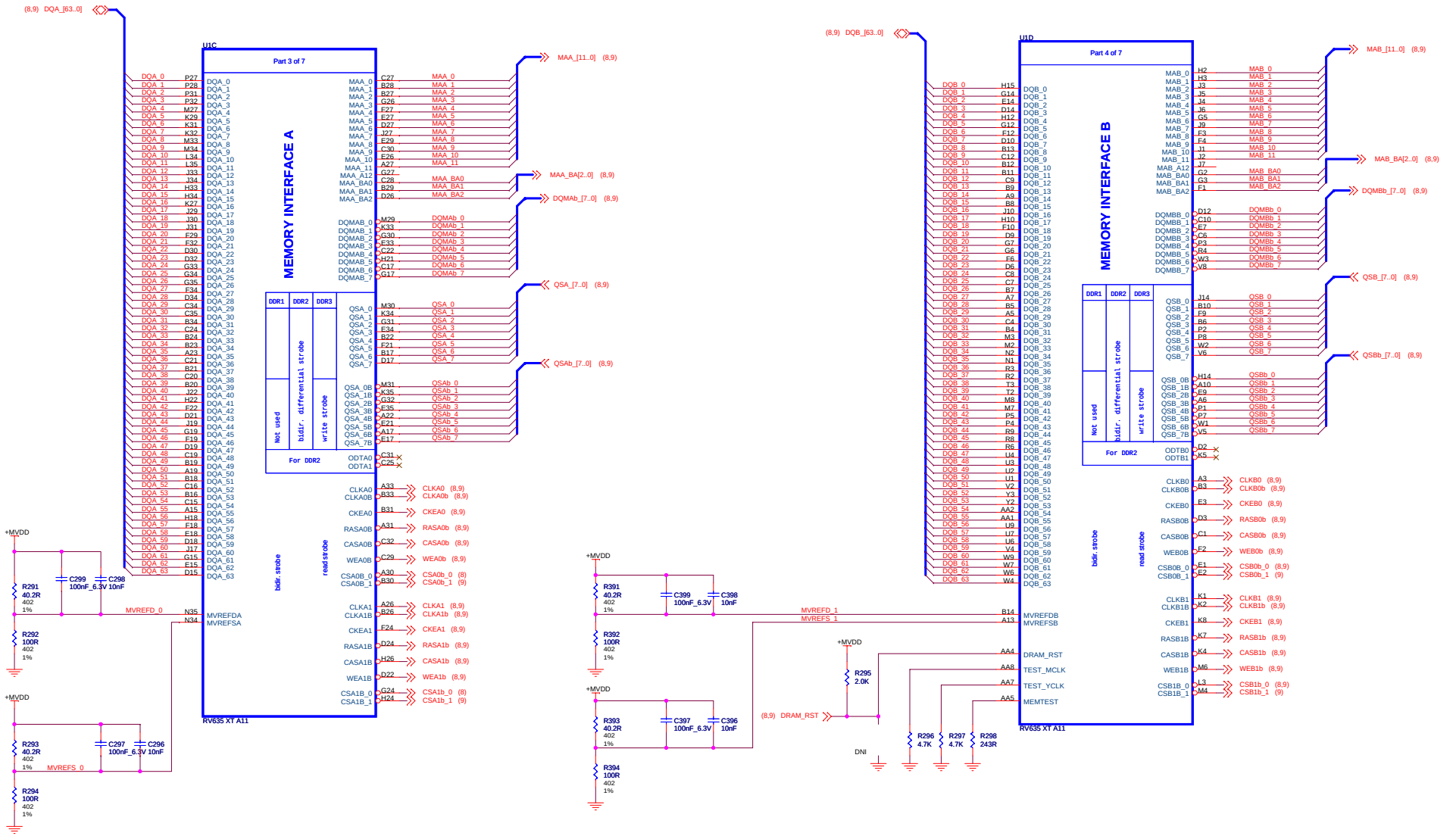
Title	RV635 GDDR3 - ASIC Power
Doc No.	102-B38001-00



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Title	RV635 GDDR3 - ASIC Memory Interface (Channel A & B)
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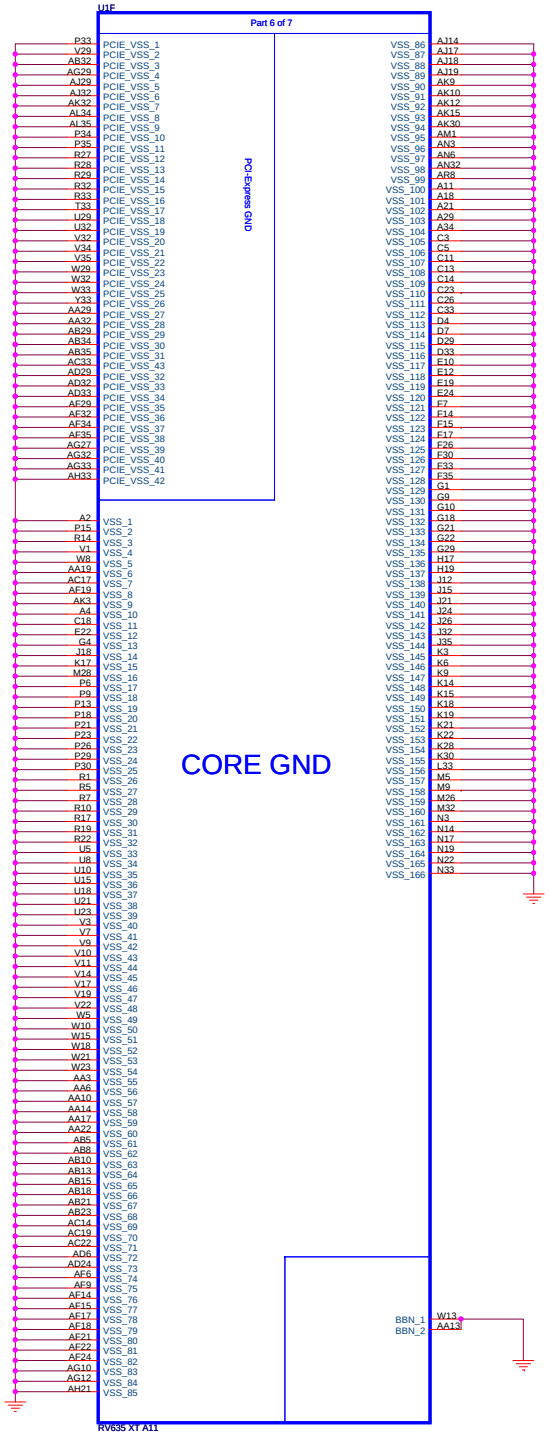

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Title RV635 GDDR3 - ASIC Grounds

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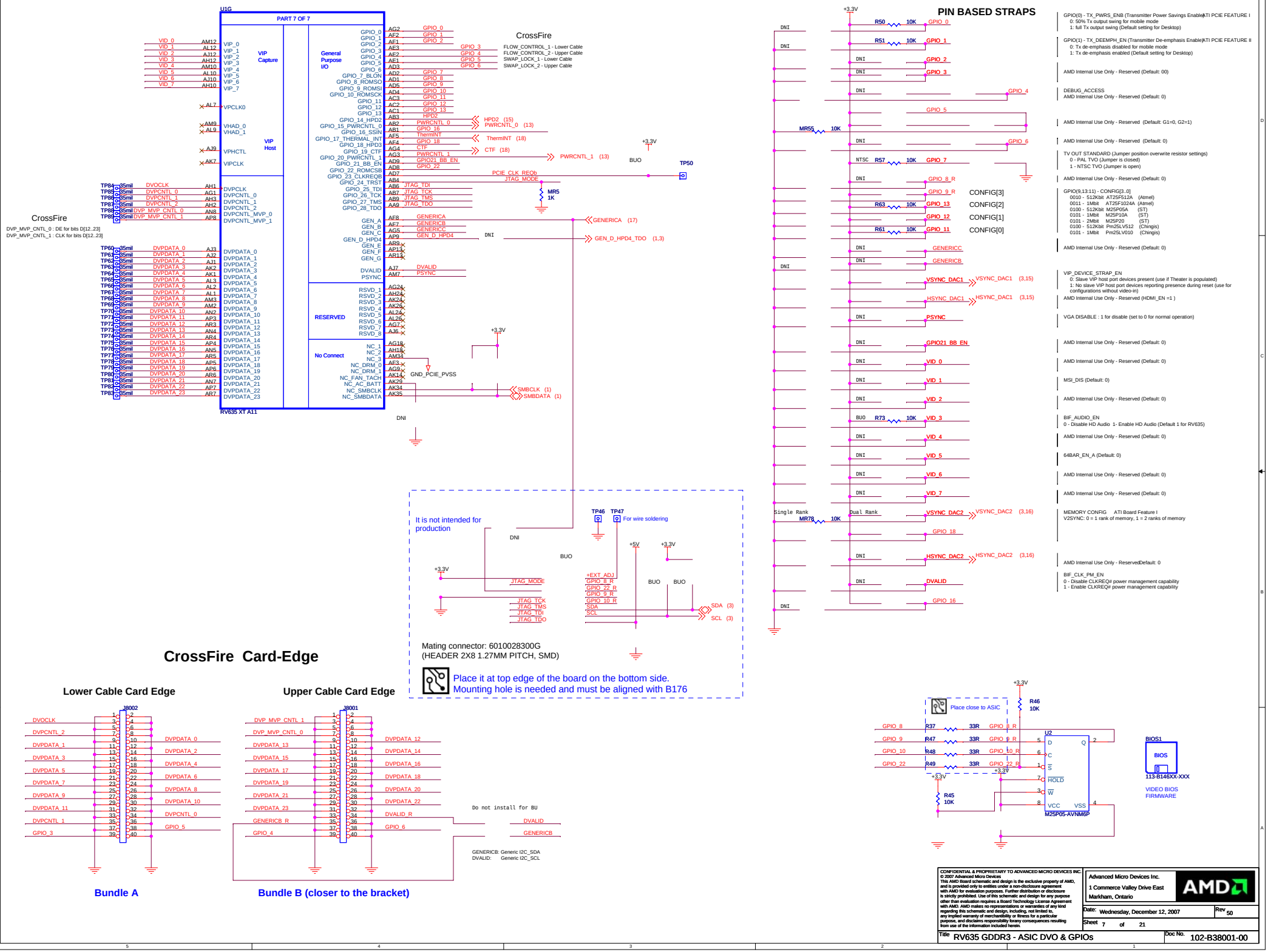
U1G
PART 7 OF 7
RV635 XT A11
VIP Capture
VIP Host
General Purpose I/O
RESERVED
No Connect
CrossFire
PIN BASED STRAPS
CrossFire Card-Edge
Lower Cable Card Edge
Upper Cable Card Edge
Bundle A
Bundle B (closer to the bracket)
It is not intended for production
For wire soldering
Mating connector: 6010028300G
(HEADER 2X8 1.27MM PITCH, SMD)
Place it at top edge of the board on the bottom side.
Mounting hole is needed and must be aligned with B176
Place close to ASIC
BIOS1
113-B146XX-XXX
VIDEO BIOS FIRMWARE
M25P05-AVNM6P
Do not install for BU
GENERICB: Generic I2C_SDA
DVALID: Generic I2C_SCL
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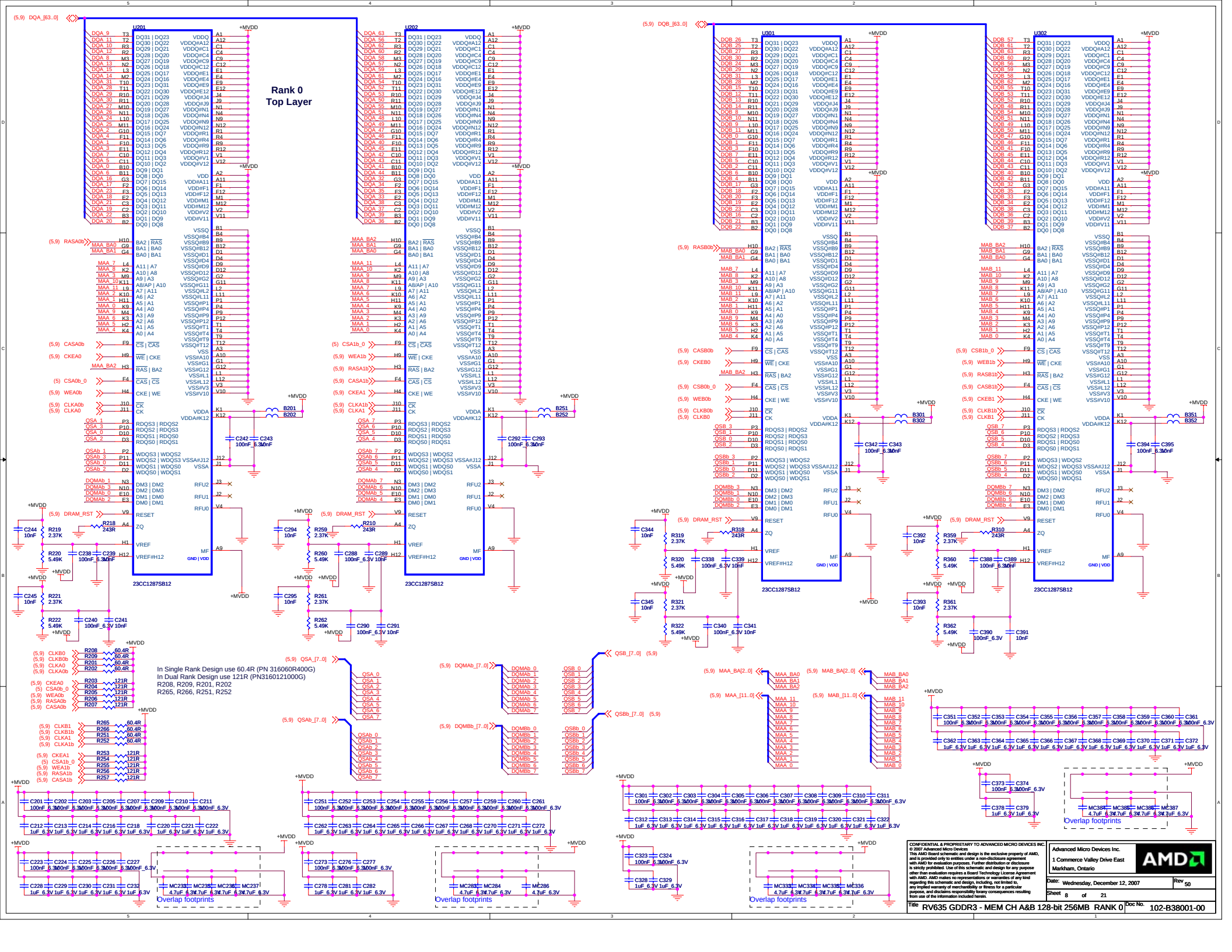
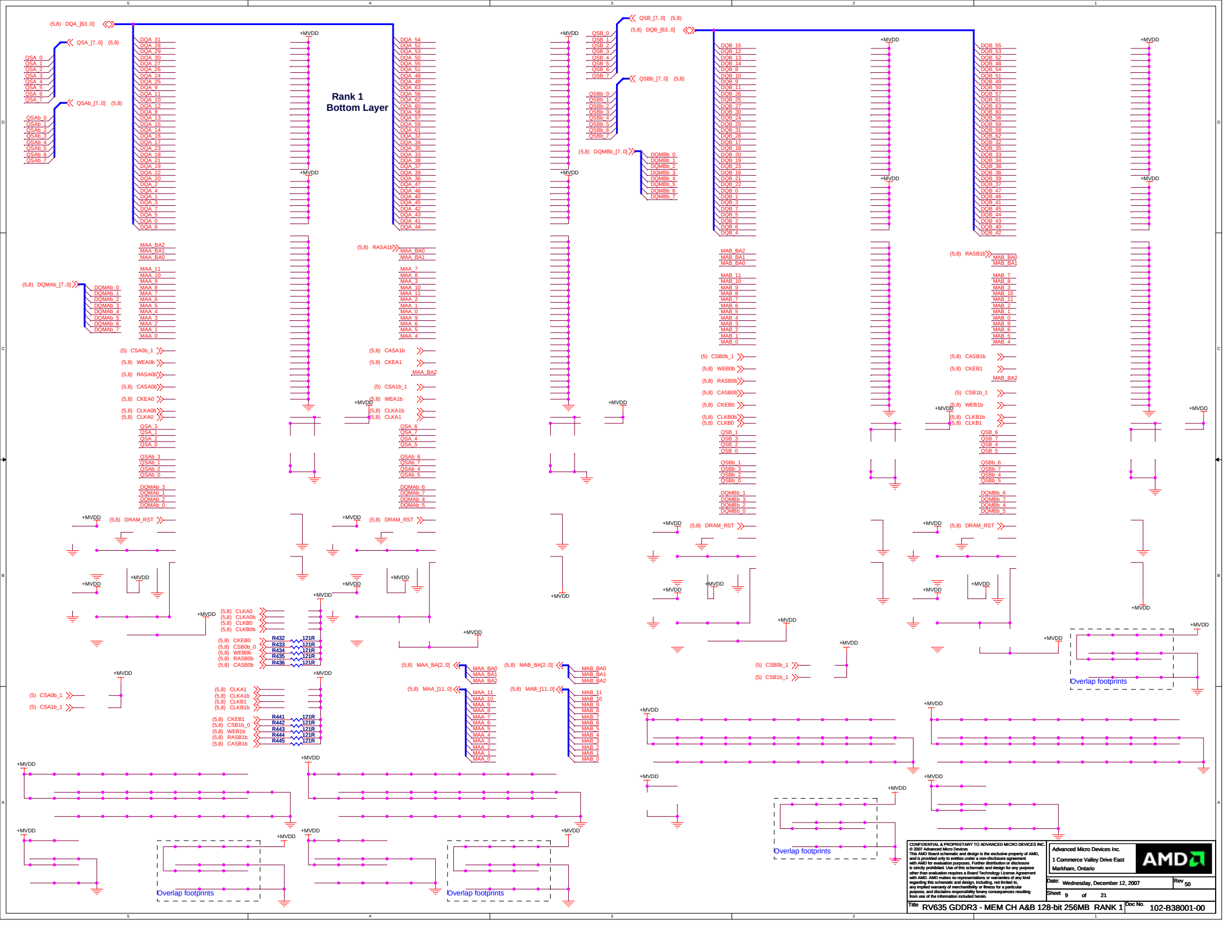
Title RV635 GDDR3 - ASIC DVO & GPIOs
Doc No. 102-B38001-00





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Title	RV635 GDDR3 - MEM CH A&B 128-bit 256MB RANK 1
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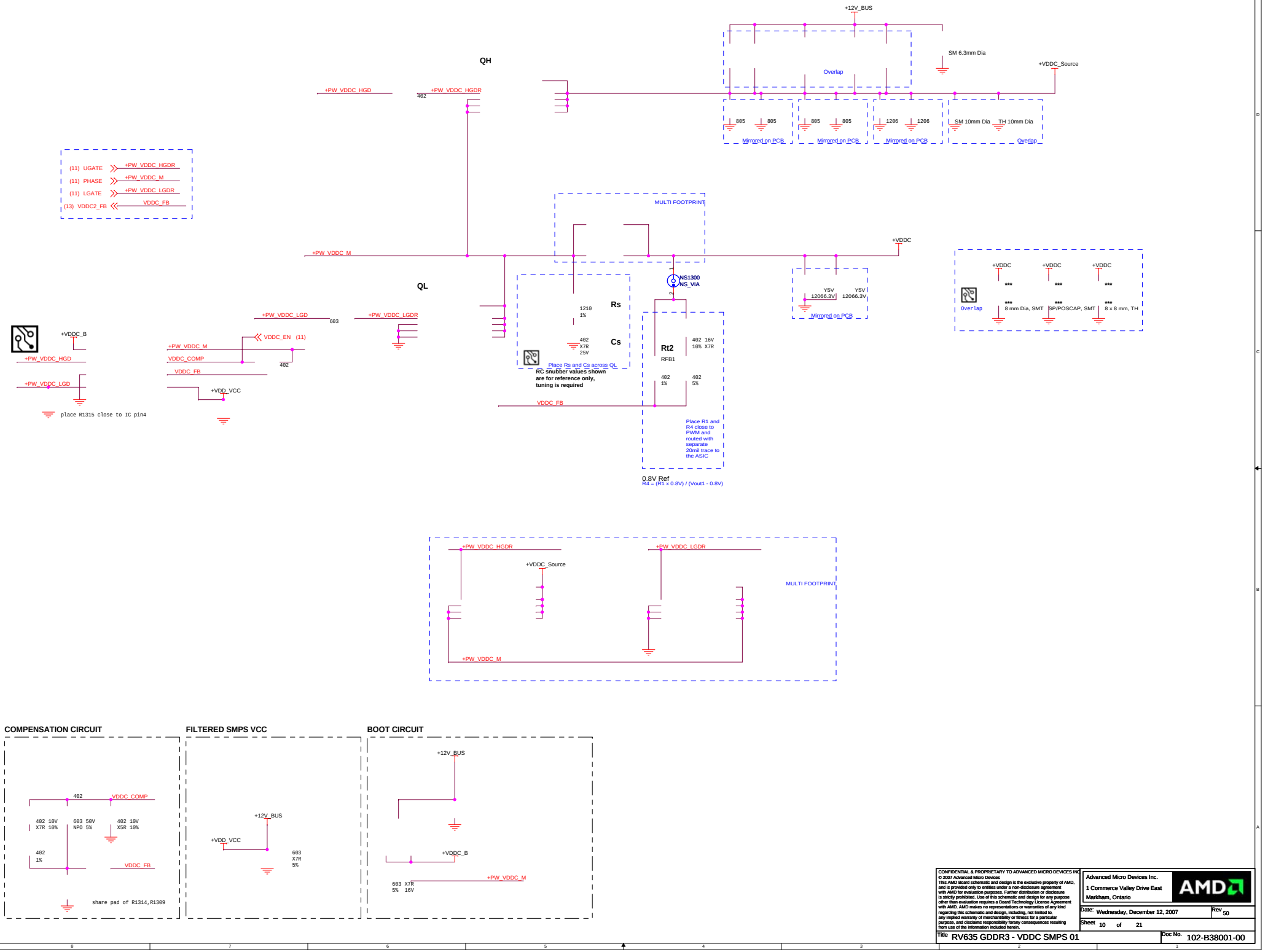

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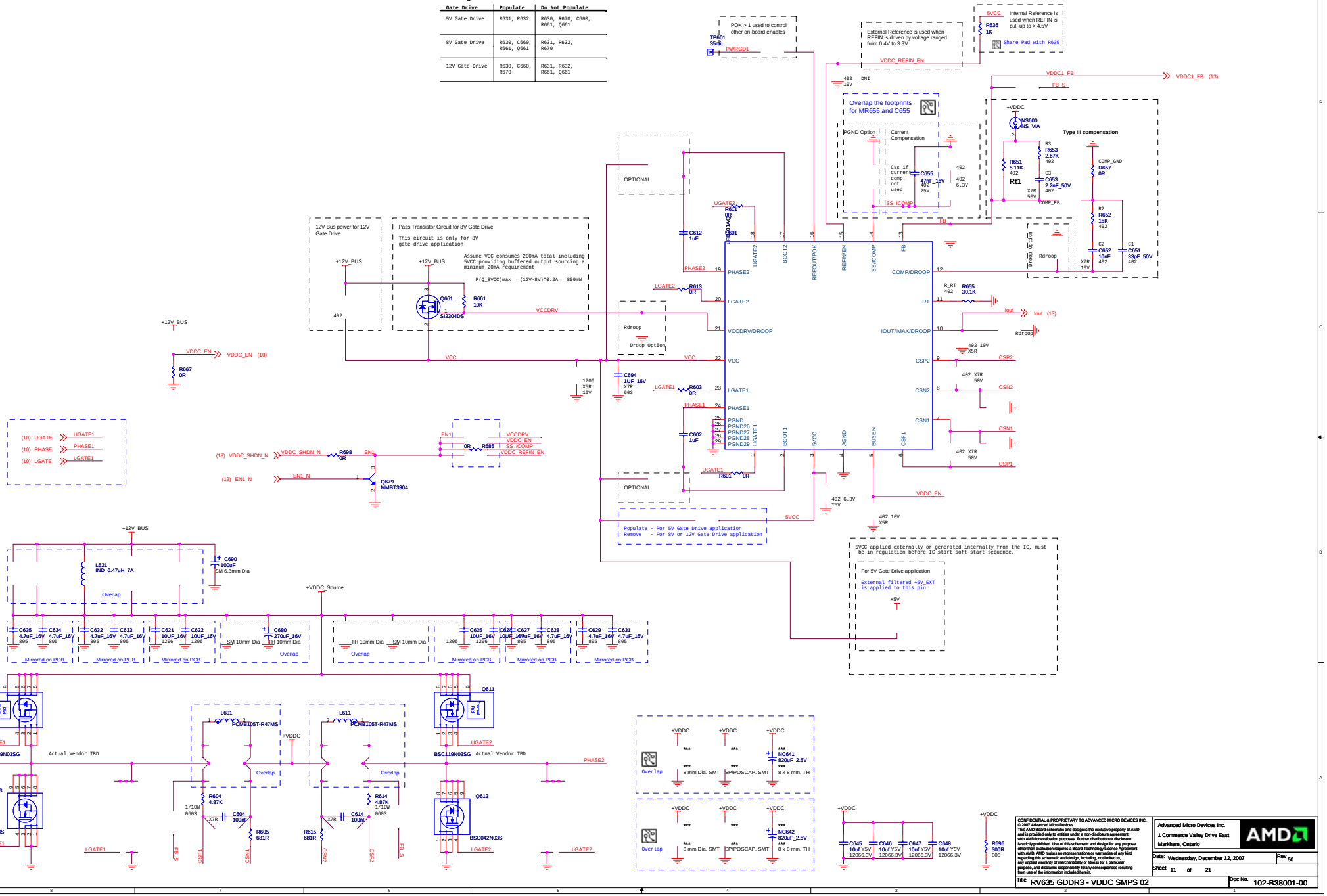
Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661



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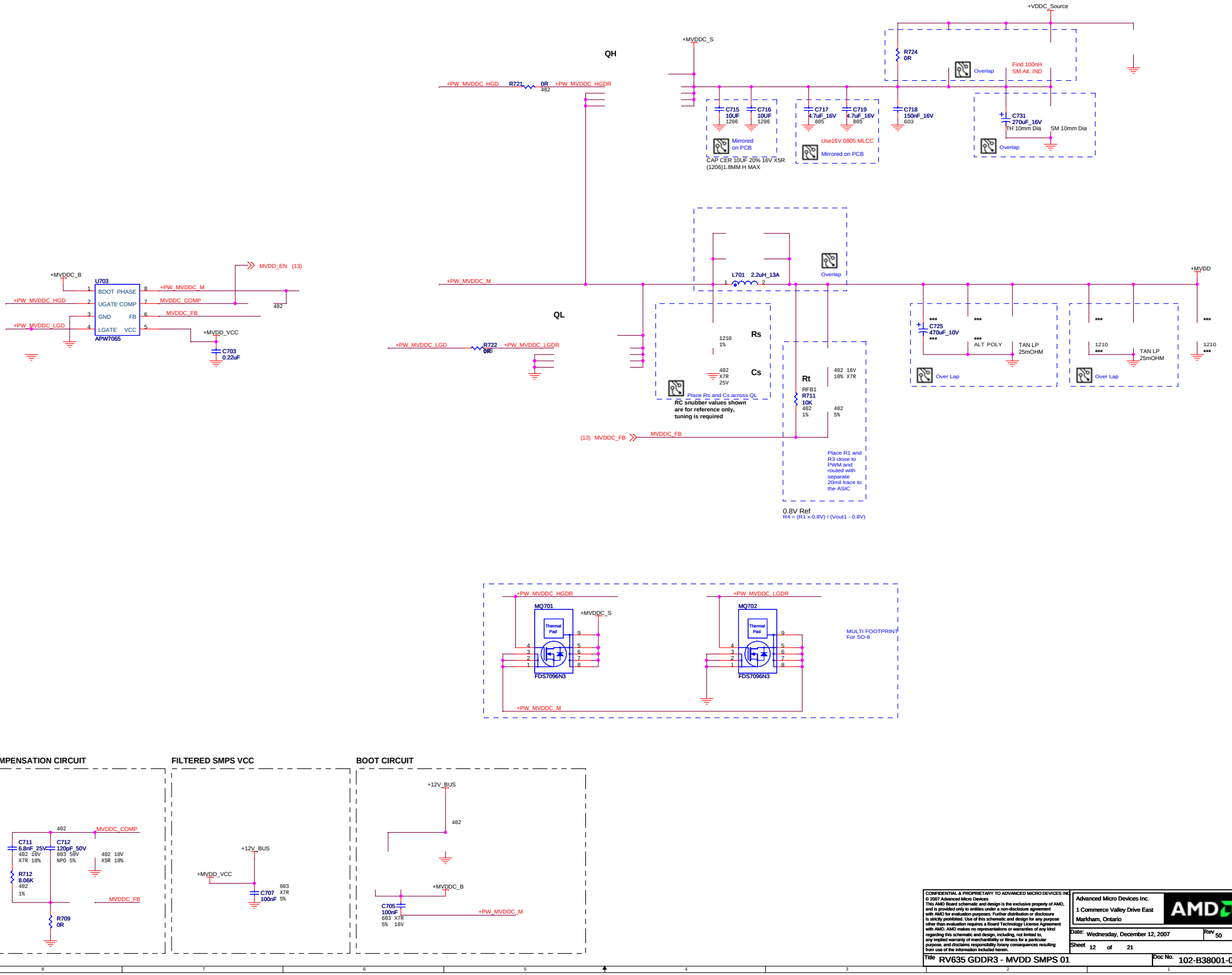
Title: RV635 GDDR3 - VDDC SMPS 02

Doc No. 102-B38001-00



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Title	RV635 GDDR3 - MVDD SMPS 01
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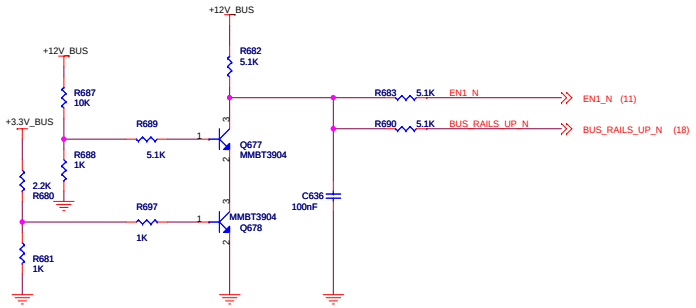
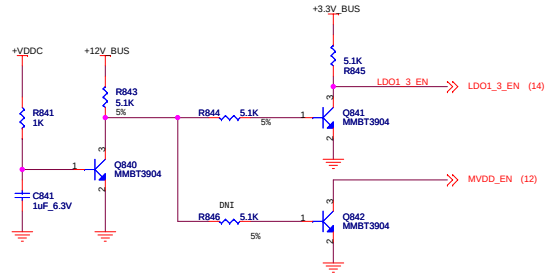
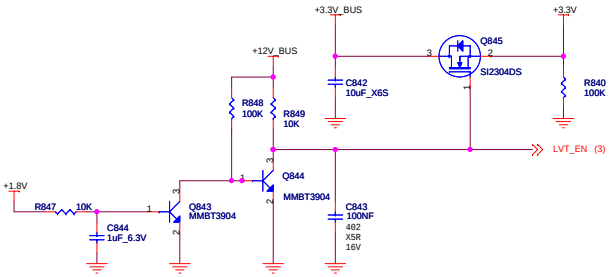
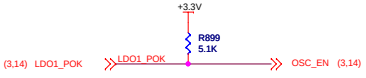
Power up Sequencing



VDDC Enable Circuit





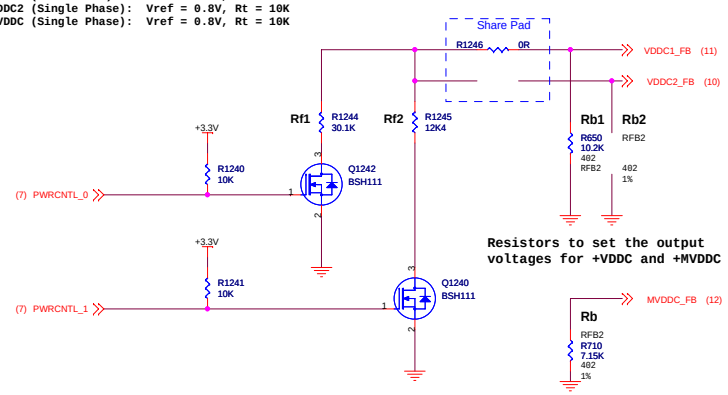


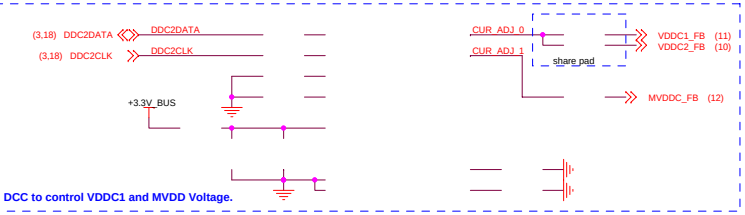
Power Play

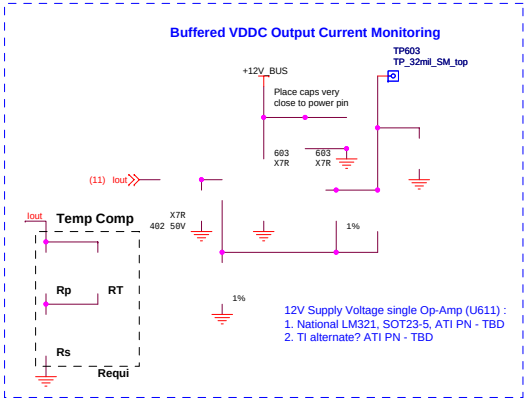
VDDC Voltage Settings Using GPIOs (for VDDC1 Dual Phase)

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1=42.2K Rf2=20.5K	Rf1= Rf2=	Rf1= Rf2=	
0	0	0.90V			
0	1	1.00V			
1	0	1.15V			
1	1	1.25V			Power-up Default

```
Vout = Vref * (1+Rt/Rb)
VDDC1 (Dual Phase):   Vref = 0.6V, Rt = 5.11K
VDDC2 (Single Phase):  Vref = 0.8V, Rt = 10K
MVDDC (Single Phase):  Vref = 0.8V, Rt = 10K
```







132-
For Testing purposes only

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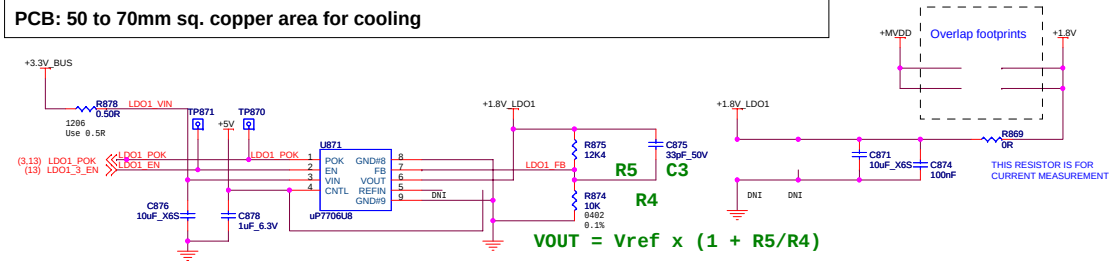
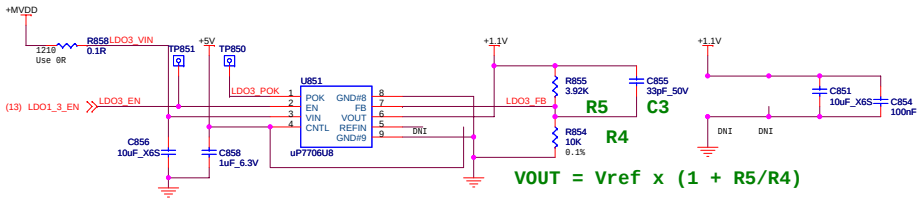
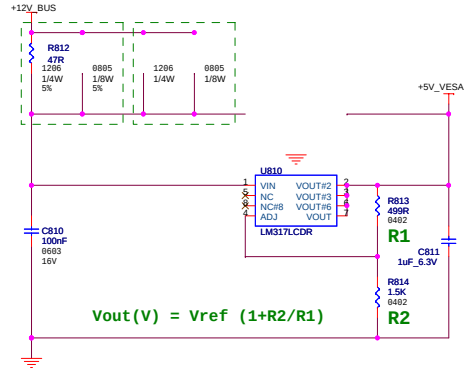
Regulators for +5V, +5V_VESA and +5V_VESA2

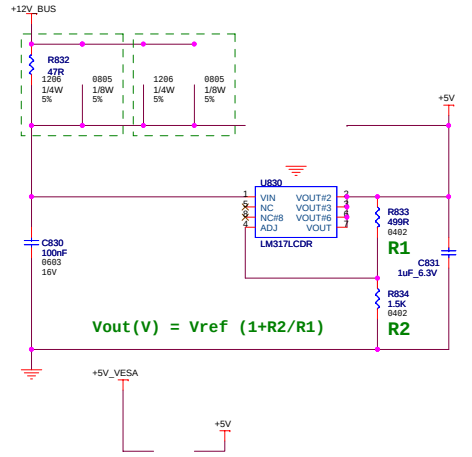
LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #3: Vin = +1.45V to 2.0VMAX Vout = +1.1V +/- 2% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling







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See BOM for qualified filters

(3) A_DAC1_R — R1001 75R — L1001 47nH — A_R_DAC1_M — L1004 36NH
(3) A_DAC1_RB — R1027 37.4R
(3) A_DAC1_G — R1002 75R — L1002 47nH — A_G_DAC1_M — L1005 36NH
(3) A_DAC1_GB — R1028 37.4R
(3) A_DAC1_B — R1003 75R — L1003 47nH — A_B_DAC1_M — L1006 36NH
(3) A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

For ESD Protection

+3.3V
+5V_VESA

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

+5V_VESA

603

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

RV635: 10K pull up on 3.3V, 2.2K pull up on 5V
RV630: 24.3K pull up on 3.3V, 19.1K on 5V

(3) CRT1DDCDATA — +3.3V — R1004 10K — +5V — R1005 2.2K — Q1001 BSH111 — DDCDATA_DAC1_5V — R1006 33R — DDCDATA_DAC1_R
(3) CRT1DDCCLK — +3.3V — R1007 10K — +5V — R1008 2.2K — Q1002 BSH111 — DDCCLK_DAC1_5V — R1009 33R — DDCCLK_DAC1_R

+5V — C1999 100nF 6.3V — U1999A

(3,7) HSYNC_DAC1 — 74VHC125 — HSYNC_DAC1_B — R1010 10R — HSYNC_DAC1_R

U1999B

(3,7) VSYNC_DAC1 — 74VHC125 — VSYNC_DAC1_B — R1011 10R — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

+3.3V — Q1021 MMBT3904 — R1022 10K — HPD_DVI2 — (7) HPD2
R1023 10K

+5V_VESA

J1001 DVI_CONNECTOR

(3) T2X2M	1	TMDS Data2-
(3) T2X2P	2	TMDS Data2+
	3	TMDS Data2/4 Shield
(3) T2X4M	4	TMDS Data4-
(3) T2X4P	5	TMDS Data4+
DDCCLK_DAC1_R	6	DDC Clock
DDCDATA_DAC1_R	7	DDC Data
VSYNC_DAC1_R	8	Analog VSYNC
(3) T2X1M	9	TMDS Data1-
(3) T2X1P	10	TMDS Data1+
	11	TMDS Data1/3 Shield
(3) T2X3M	12	TMDS Data3-
(3) T2X3P	13	TMDS Data3+
	14	+5V Power
	15	GND (for +5V)
HPD_DVI2	16	Hot Plug Detect
(3) T2X0M	17	TMDS Data0-
(3) T2X0P	18	TMDS Data0+
	19	TMDS Data0/5 Shield
(3) T2X5M	20	TMDS Data5-
(3) T2X5P	21	TMDS Data5+
	22	TMDS Clock Shield
(3) T2XCP	23	TMDS Clock+
(3) T2XCM	24	TMDS Clock-
A_R_DAC1_F	C1	Analog Red
A_G_DAC1_F	C2	Analog Green
A_B_DAC1_F	C3	Analog Blue
HSYNC_DAC1_R	C4	Analog HYNC
	C5	Analog GND
	C6	Analog GND#C6
	26	CASE#26
	27	CASE#27
	28	CASE#28
	29	CASE#29
	30	CASE#30
	25	CASE

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Title RV635 GDDR3 - DAC1&TMDS2 — Doc No. 102-B38001-00

See BOM for qualified filters

(3) A_DAC2_R — R2001 75R 402 — L2001 47nH — A_R_DAC2_M — L2004 36NH
(3) A_DAC2_RB — R2027 37.4R 402
(3) A_DAC2_G — R2002 75R 402 — L2002 47nH — A_G_DAC2_M — L2005 36NH
(3) A_DAC2_GB — R2028 37.4R 402
(3) A_DAC2_B — R2003 75R 402 — L2003 47nH — A_B_DAC2_M — L2006 36NH
(3) A_DAC2_BB — R2029 37.4R 402

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R

+3.3V
+5V_VESA

For ESD Protection

603

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

(3) CRT2DDCDATA — DNI for RV635 — +3.3V — +5V — R2005 2.2K 402 — DDCDATA_DAC2_5V — R2006 33R 402 — DDCDATA_DAC2_R
R2040 0R — DNI for RV630

(3) CRT2DDCCLK — DNI for RV635 — +3.3V — +5V — R2008 2.2K 402 — DDCCLK_DAC2_5V — R2009 33R 402 — DDCCLK_DAC2_R
R2041 0R — DNI for RV630

RV635: no pull up on 3.3V, 2.2K pull up on 5V
RV630: 24.3K pull up on 3.3V, 19.1K on 5V

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

U1999C
(3,7) HSYNC_DAC2 — 9 — 8 — HSYNC_DAC2_B — R2010 10R 402 — HSYNC_DAC2_R
74VHC125
13,10
U1999D
(3,7) VSYNC_DAC2 — 12 — 11 — VSYNC_DAC2_B — R2011 10R 402 — VSYNC_DAC2_R
74VHC125

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

+3.3V
Q2021 MMBT3904 — R2022 10K — HPD_DVI1
(3) HPD1
R2023 10K

+5V_VESA
J2001 DVI_CONNECTOR

25	CASE		
1	TMDS Data2-	(3) T1X2M	
2	TMDS Data2+	(3) T1X2P	
3	TMDS Data2/4 Shield		
4	TMDS Data4-	(3) T1X4M	
5	TMDS Data4+	(3) T1X4P	
6	DDC Clock		DDCCLK_DAC2_R
7	DDC Data		DDCDATA_DAC2_R
8	Analog VSYNC		VSYNC_DAC2_R
9	TMDS Data1-	(3) T1X1M	
10	TMDS Data1+	(3) T1X1P	
11	TMDS Data1/3 Shield		
12	TMDS Data3-	(3) T1X3M	
13	TMDS Data3+	(3) T1X3P	
14	+5V Power		
15	GND (for +5V)		
16	Hot Plug Detect		
17	TMDS Data0-	(3) T1X0M	
18	TMDS Data0+	(3) T1X0P	
19	TMDS Data0/5 Shield		
20	TMDS Data5-	(3) T1X5M	
21	TMDS Data5+	(3) T1X5P	
22	TMDS Clock Shield		
23	TMDS Clock+	(3) T1XCP	
24	TMDS Clock-	(3) T1XCM	
C1	Analog Red		A_R_DAC2_F
C2	Analog Green		A_G_DAC2_F
C3	Analog Blue		A_B_DAC2_F
C4	Analog HYNC		HSYNC_DAC2_R
C5	Analog GND		
C6	Analog GND#C6		
26	CASE#26		
27	CASE#27		
28	CASE#28		
29	CASE#29		
30	CASE#30		

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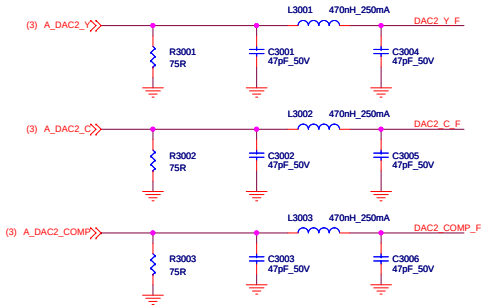
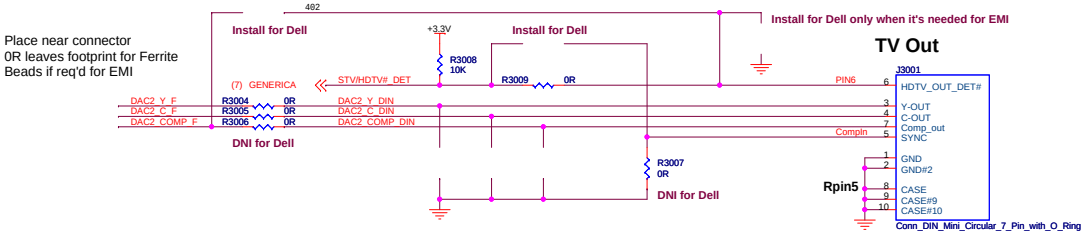
Title RV635 GDDR3 - DAC2/TMDS1 — Doc No. 102-B38001-00





The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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Title RV635 GDDR3 - TVO

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+VDDC_Source
+12V_BUS
B4002
26R_600mA
C4008
1uF
0805
16V

LM63 is for BU only, until built-in fan controller is verified.

+3.3V
R4032
2.61K
(3,13) DDC2CLK
(3,13) DDC2DATA
(7) ThermINT
SCL_R
SDA_R
TINT_R
GPU_DPLUS
GPU_DPLUS (3)
GPU_DMINUS
GPU_DMINUS (3)
LM63_PWM
For fan with 3.3V PWM (bypass) install 0R (TBV)
PWM
Q4001
MMBT3904
R4005
10K
(3) TS_FDO
TS_FDO
Place R4032, and R4033 on the bottom side. Easily accessiable.
DNI
Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

For 2-WIRE FAN ONLY
+12V_BUS
1%
DNI
805
16V
Y5V
+3.3V_BUS
MR4006
5.1K
R4039
1K
Q4030
MMBT3904
TP4001
35mil
TACH
R4030
100K
R4031
15K
R4014
0R
PWM
DNI (bypass for fan with 3.3V PWM)
For testing purposes only
For 4-WIRE FAN ONLY
Header is 2mm, and it does not follow 2.54mm spacing as 4-pin PWM Fan Specification
J4030
1X4 3A 2MM
Overlap MJ4030 and J4030

Not intended for production
LED off shows the fault
+3.3V_BUS

+3.3V_BUS
R1254
10K
(13) BUS_RAILS_UP_N
Q1252
MMBT3904
C1251
1uF_6.3V
C1250
100nF_6.3V
U1250
NC7SZ74K8X
D
Vcc
PR
Q
C
G
CL
QI
R1259
2.2K
R1260
1K
Q1253
MMBT3904
If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board.
VDDC_SHDN_N (11)
R1252
10K
Q1250
BSH111
(7) CTF
R1250
2.2K
R1255
5.1K
R1257
100K
Q1251
MMBT3904
Bypass Switch
(not for production)

See BOM for qualified option.

H1A
FANSINK
H1B
H1C
H1D
H1E
H1F
H1G
H1H
USE FANSINK FOR RV630 GDDR3, p/n 7121033200G

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DVI/DVI SCREWS with top tab

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

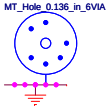
ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET
8020038600G

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

MT2
MT_Hole_0.136_in_6VIA



DNI

PCB1
PCB
109-B380xx-00

RV635 Socket

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Title RV635 GDDR3 - Mechanical
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Title	Schematic No.	Date:
RH PCIE RV635 2x256MB GDDR3 DUAL DL-DVI-I DL-DVI-I VO FH	102-B38001-00	Wednesday, December 12, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

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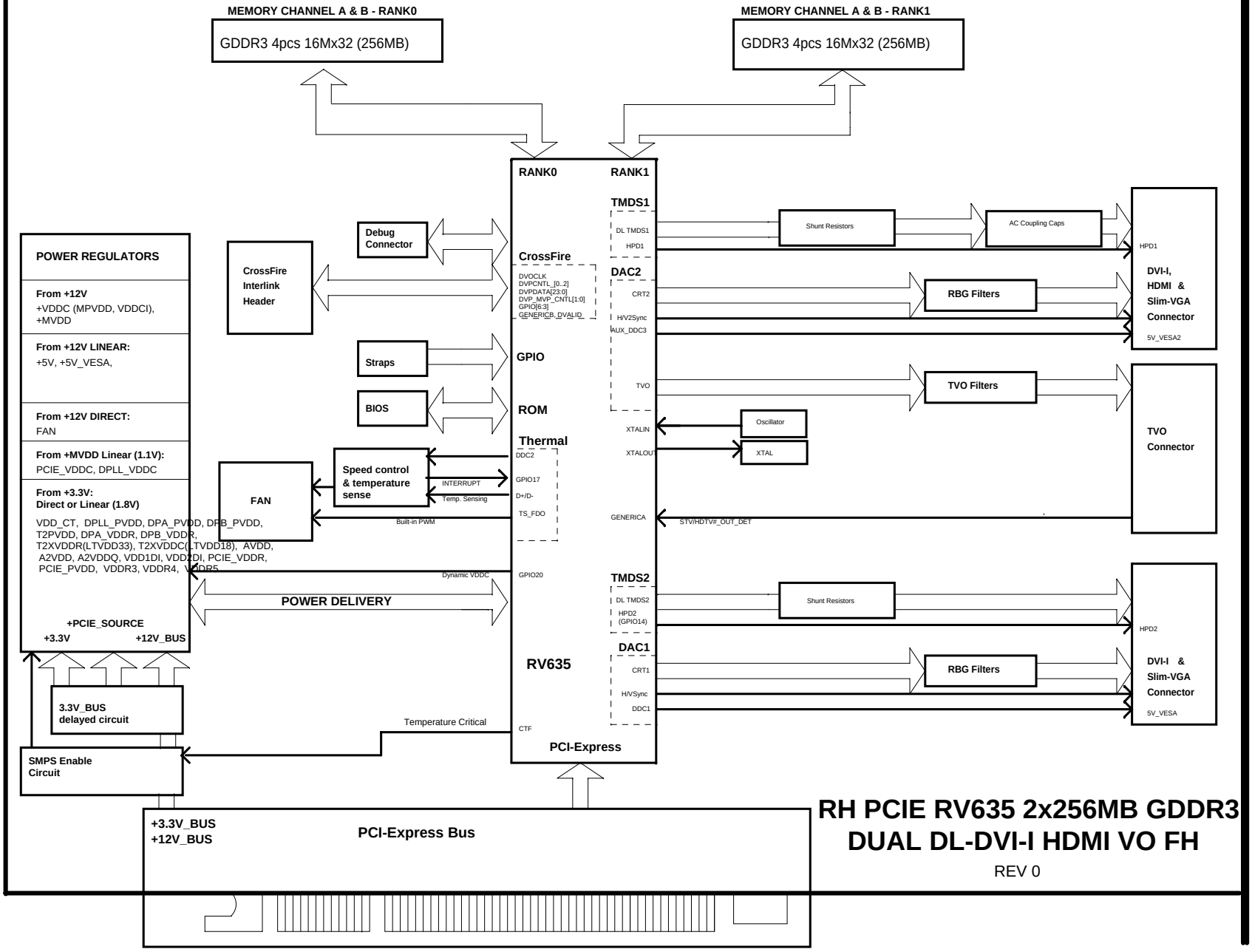
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/13/07	Initial design for RV635 GDDR3
1	00	10/25/07	Release To Rev 00



RH PCIE RV635 2x256MB GDDR3 DUAL DL-DVI-I HDMI VO FH

REV 0

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Title	RV635 GDDR3 - BLOCK DIAGRAM
Doc No.	102-B38001-00