PCI-EXPRESS EDGE CONNECTOR

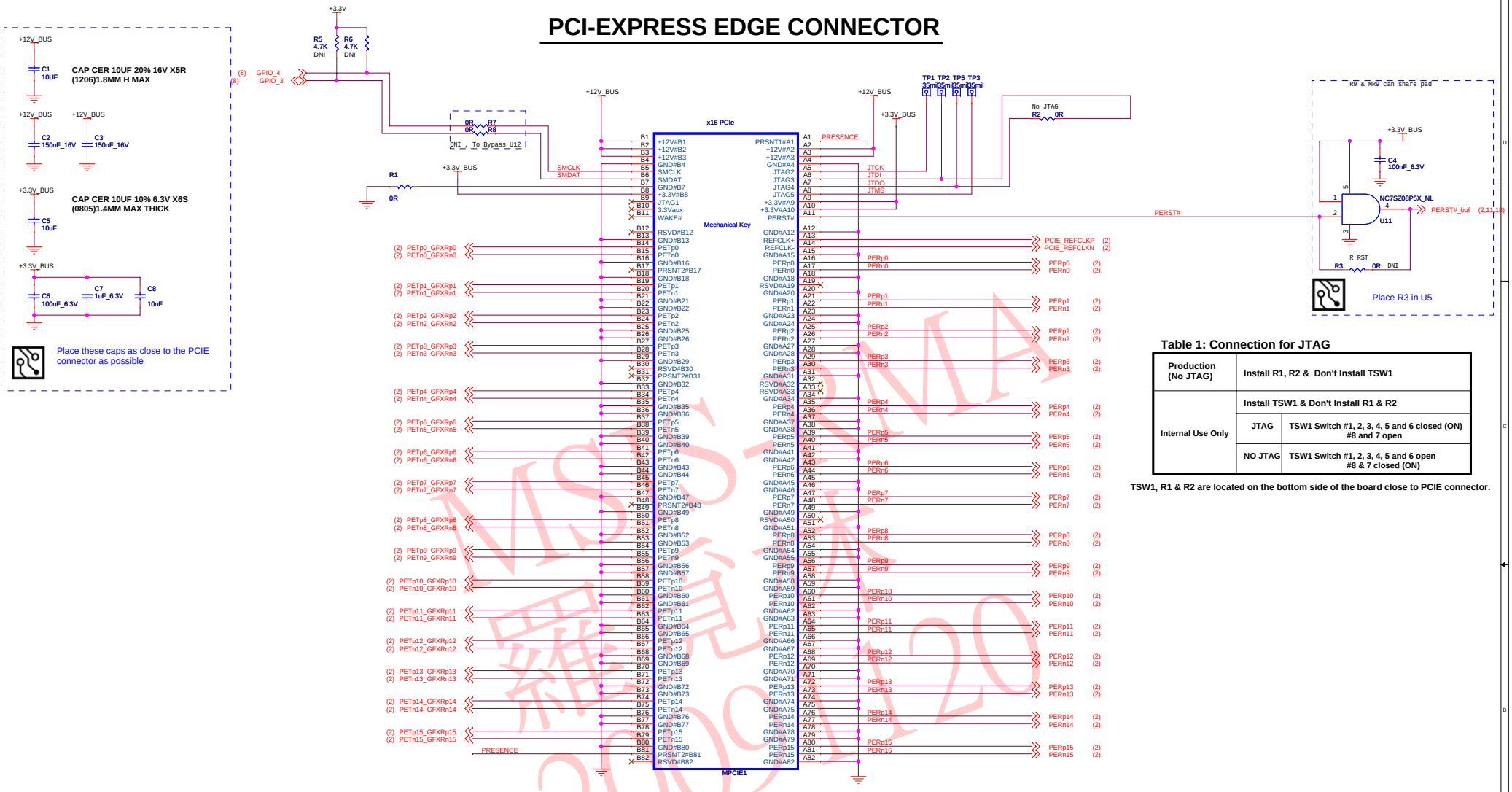

Table 1: Connection for JTAG

Production (No JTAG)	Install R1, R2 & Don't Install TSW1	
Internal Use Only	Install TSW1 & Don't Install R1 & R2	
	JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open
	NO JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
⏚	DIGITAL GROUND
⏚	ANALOG GROUND
BUO	BRING UP ONLY

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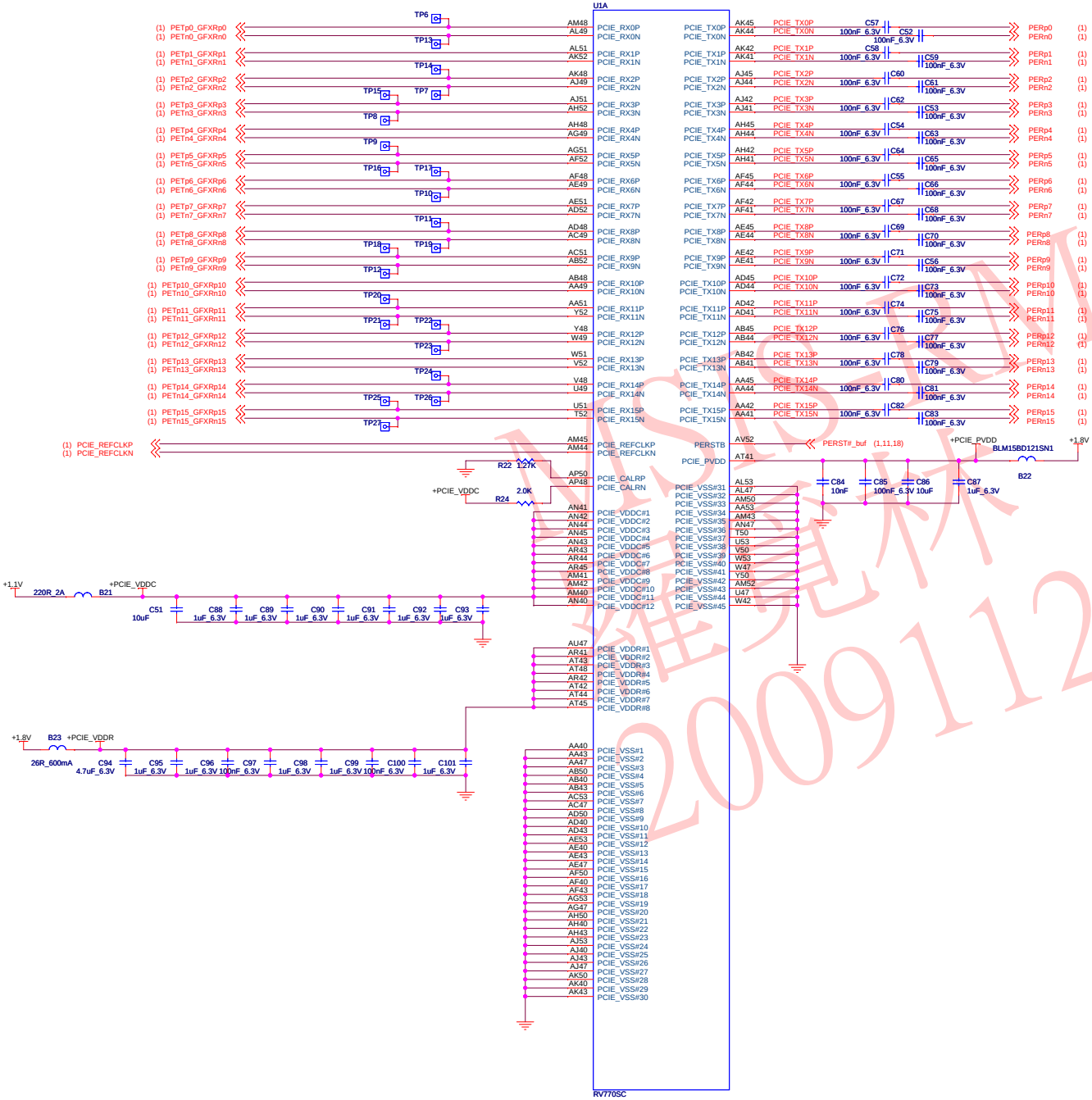
NOTE: some of the PCIE testpoints will
be available trought via on traces.



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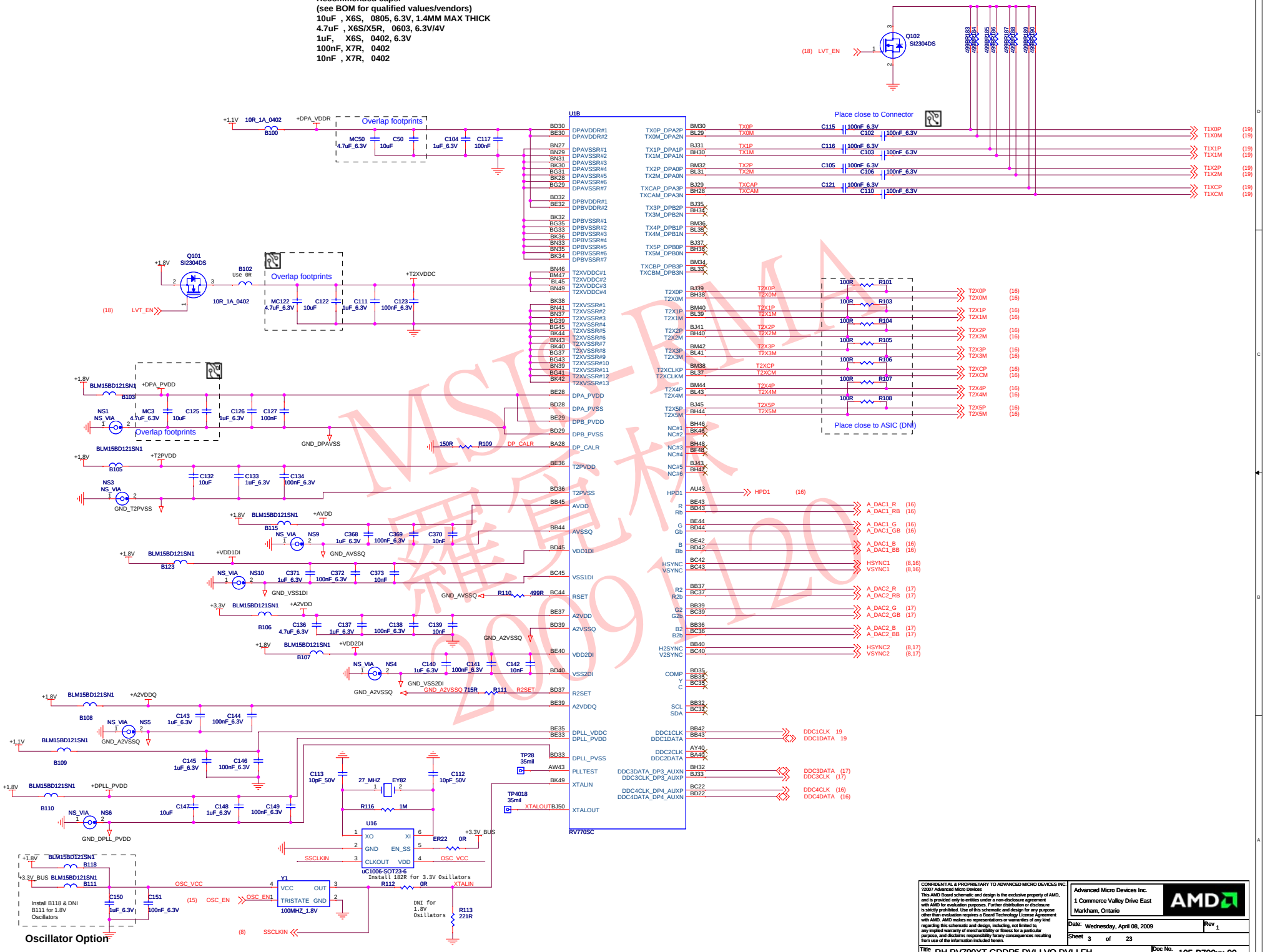
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402
Q102
SI2304DS
(18) LVT_EN
Place close to Connector
U1B
RV770SC
Overlap footprints
Q101
SI2304DS
B102
Use 0R
10R_1A_0402
Place close to ASIC (DNI)
Install B118 & DNI
B111 for 1.8V
Oscillators
Oscillator Option
U16
uC1006-SOT23-6
Install 182R for 3.3V Osillators
Y1
100MHZ_1.8V
DNI for
1.8V
Osillators
TP28
35mil
TP4018
35mil
27_MHZ
EY82
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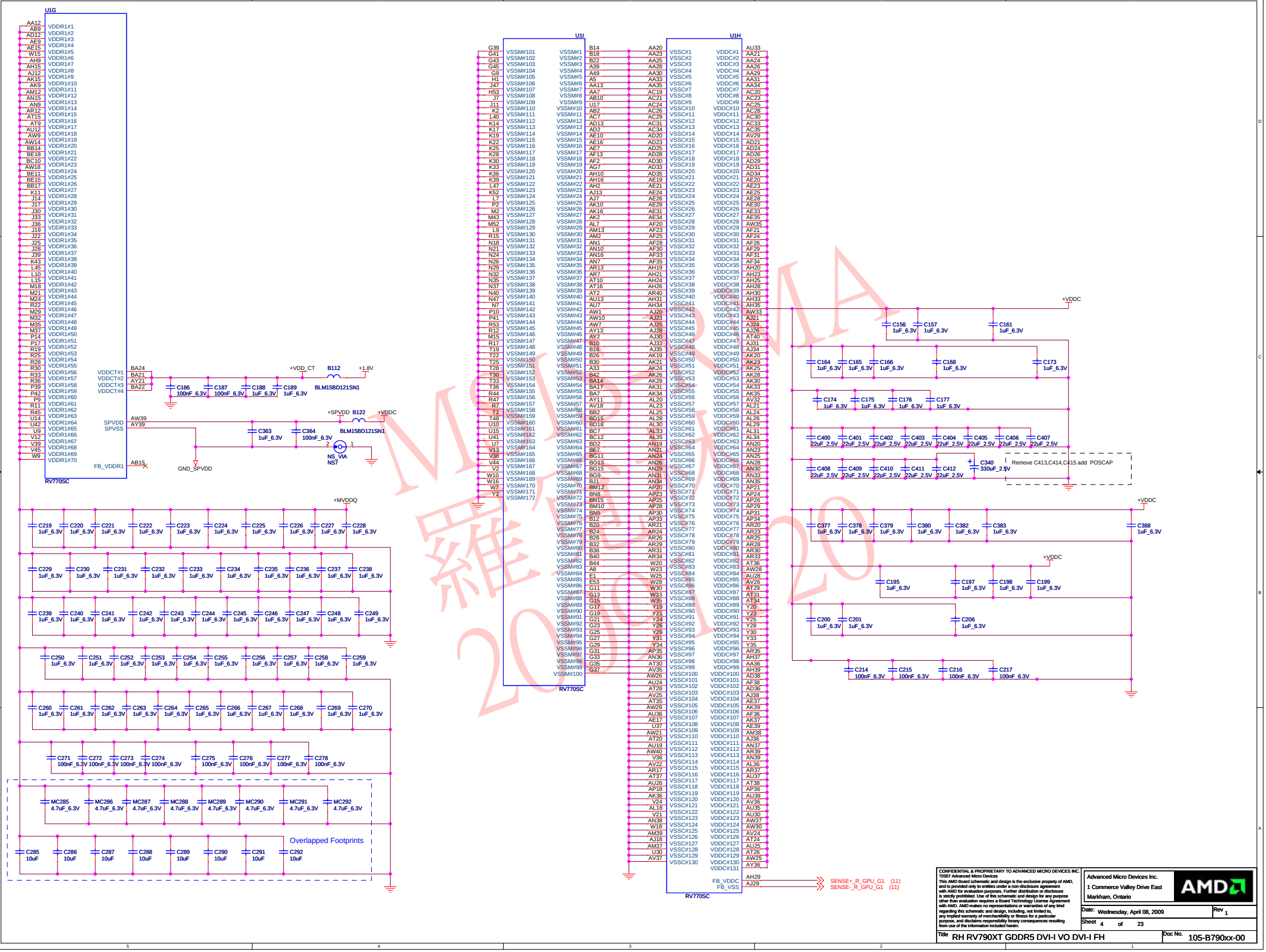

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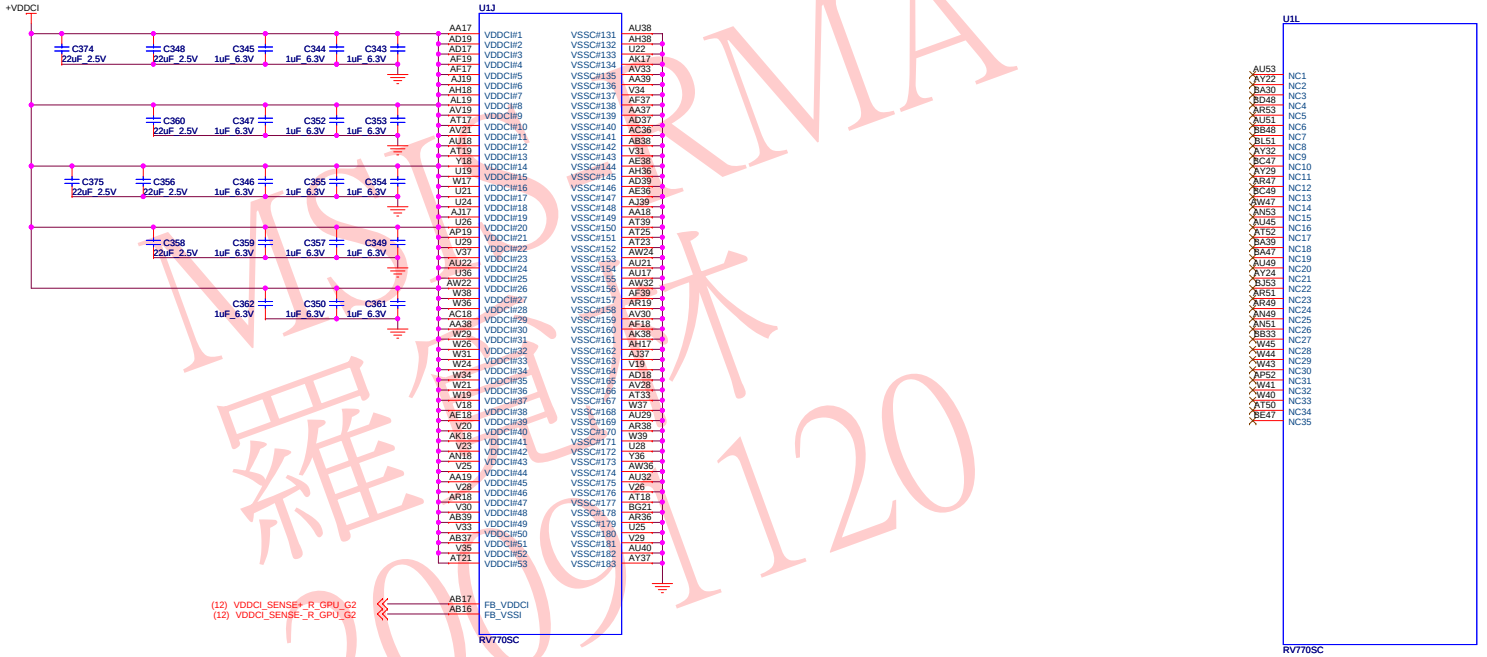

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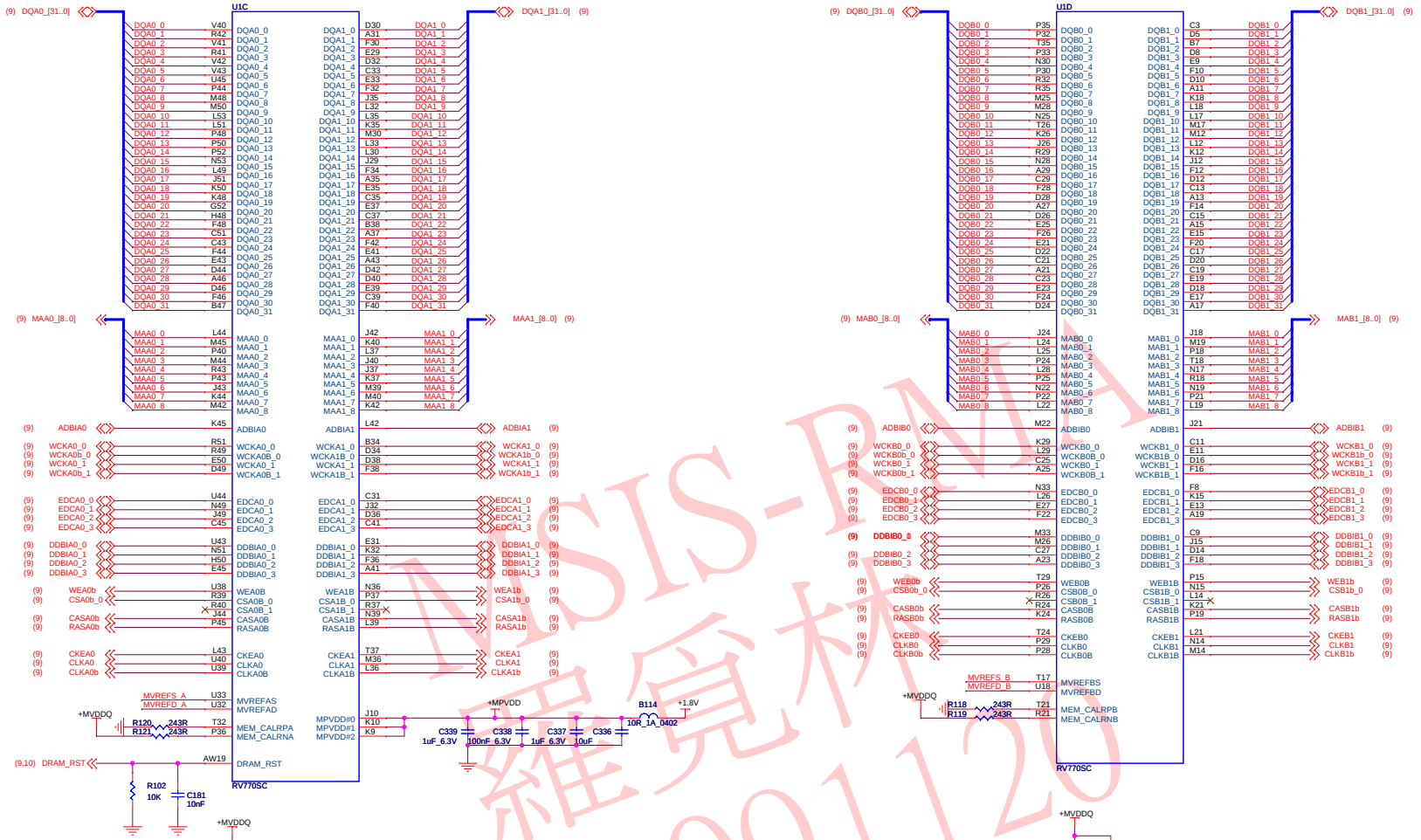

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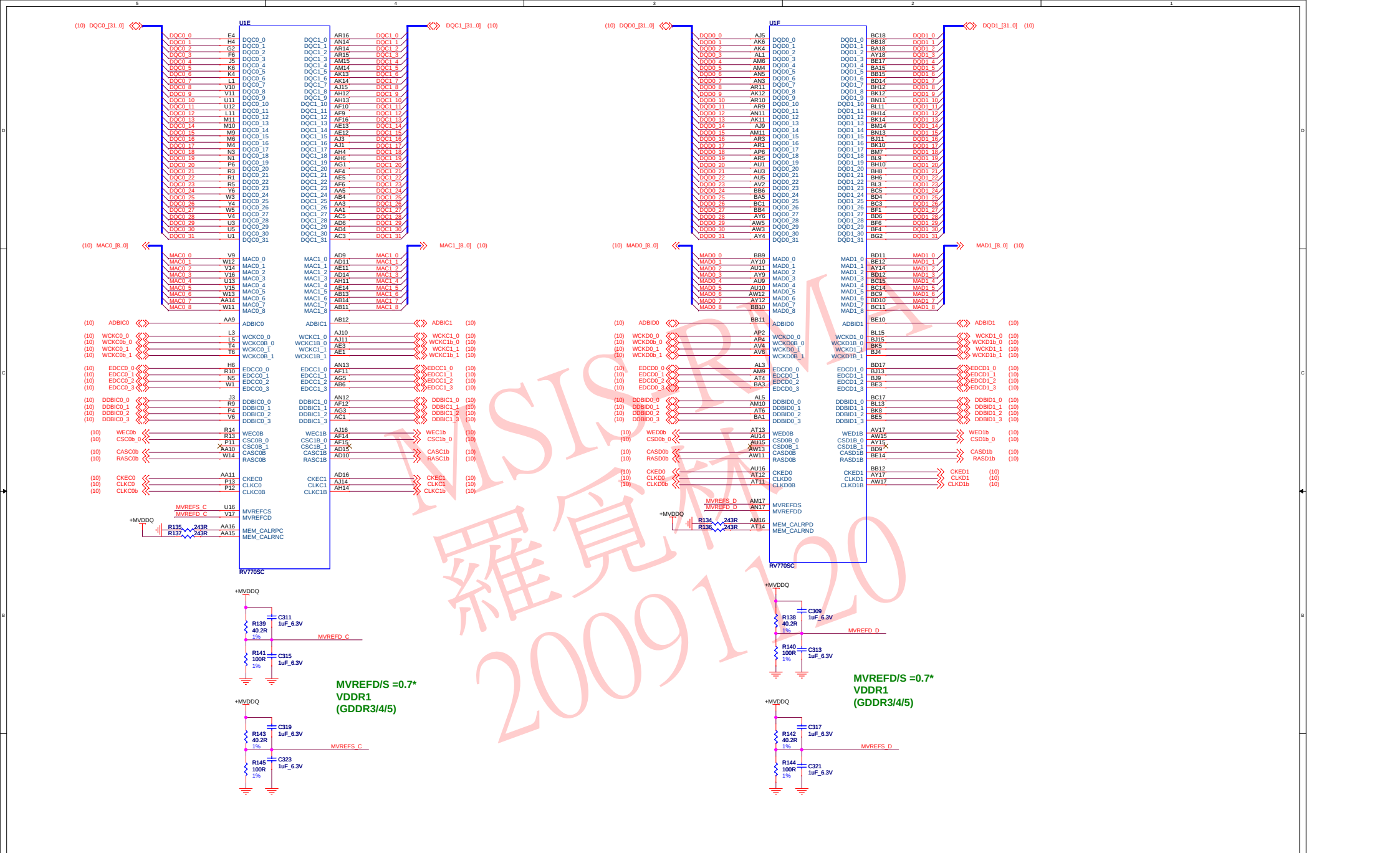

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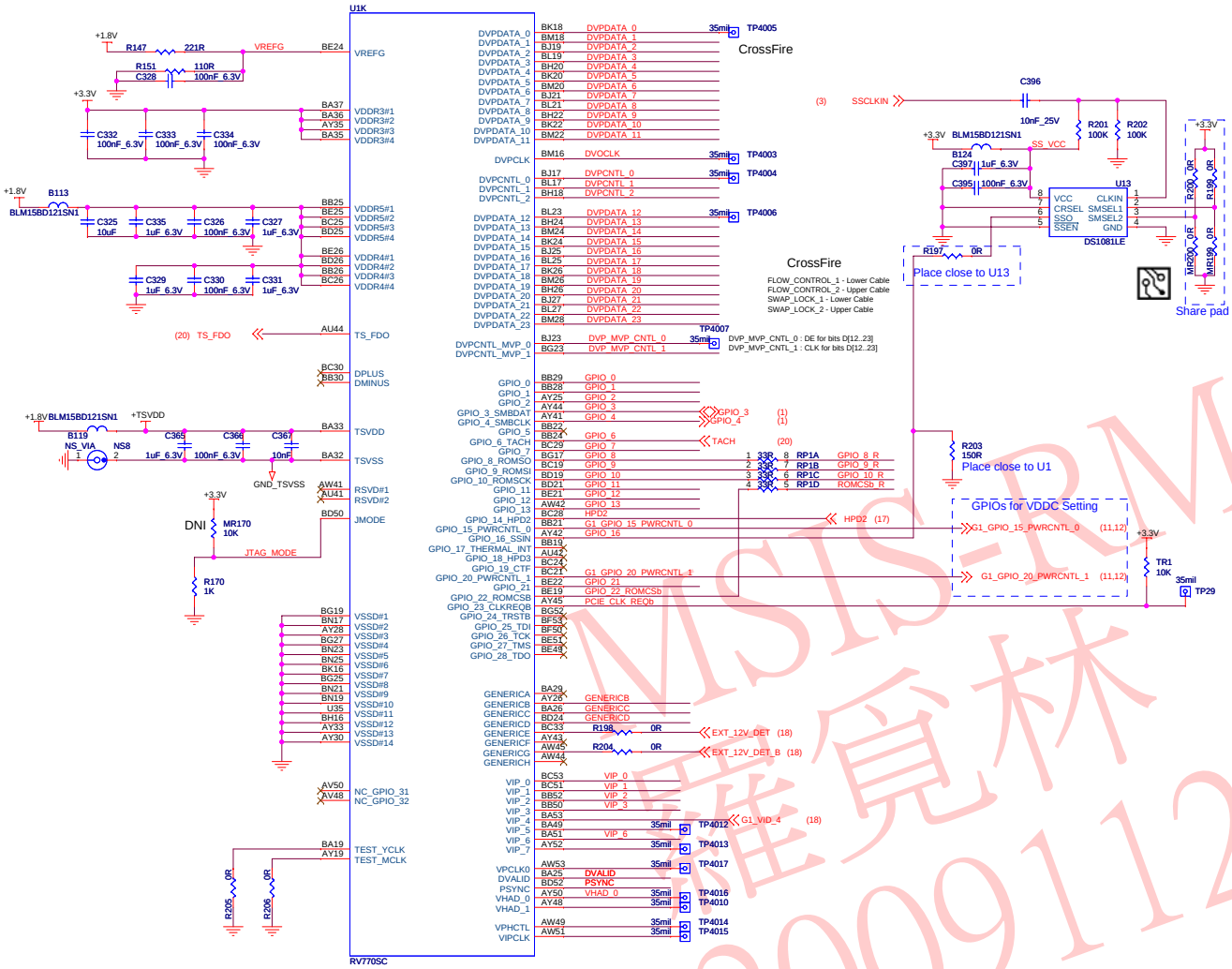
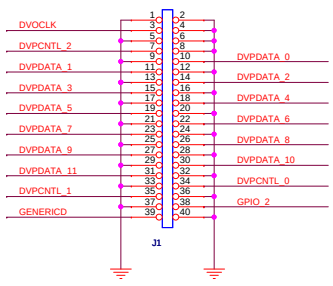
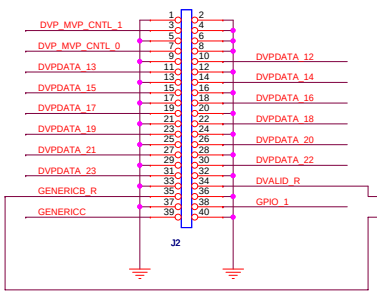


Lower Cable Card Edge

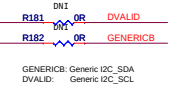


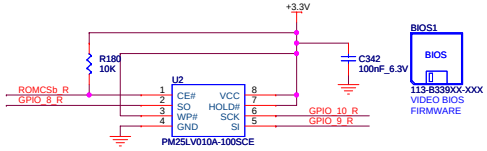
Bundle B

Upper Cable Card Edge



Bundle A (closer to the bracket)





PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

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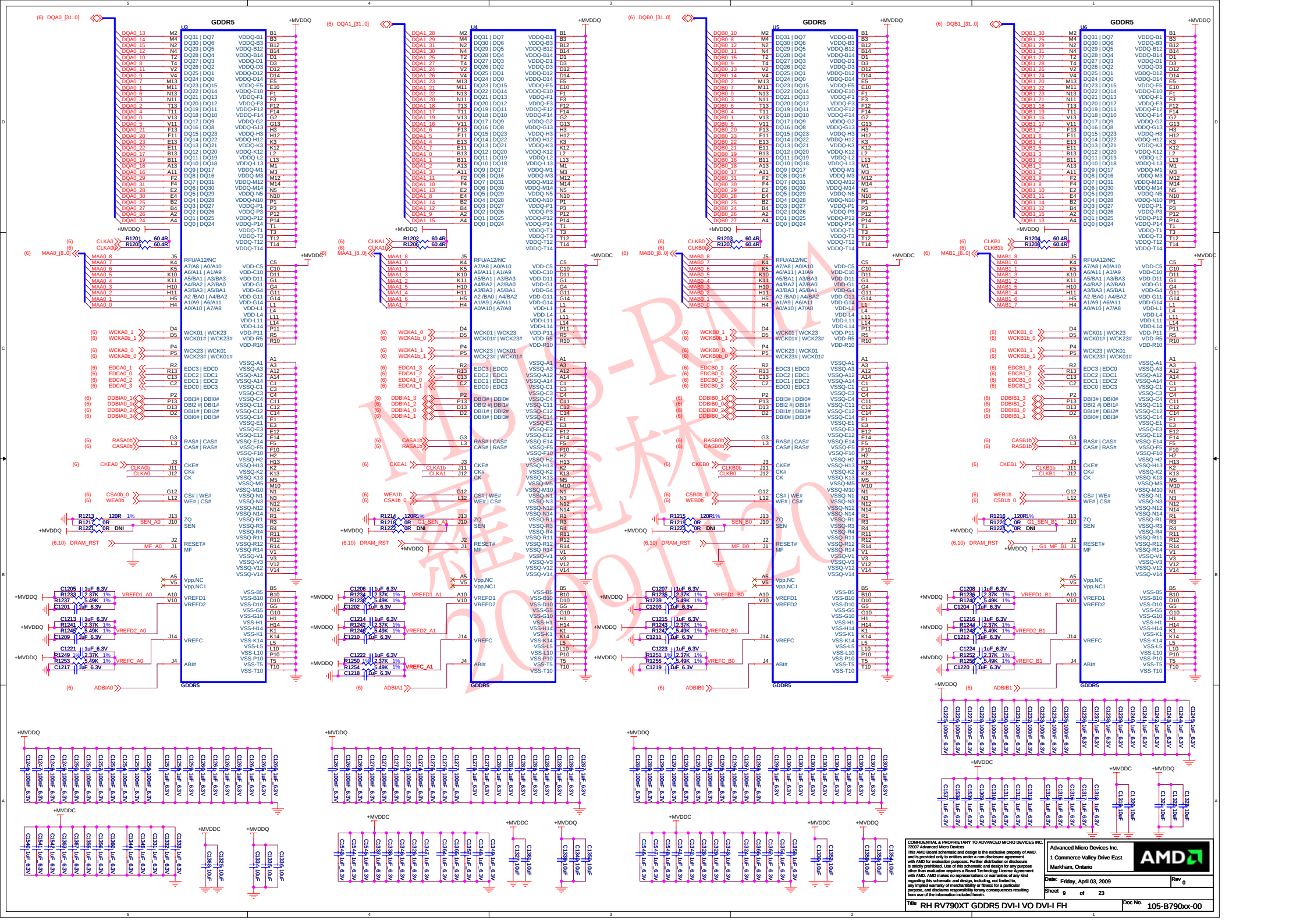

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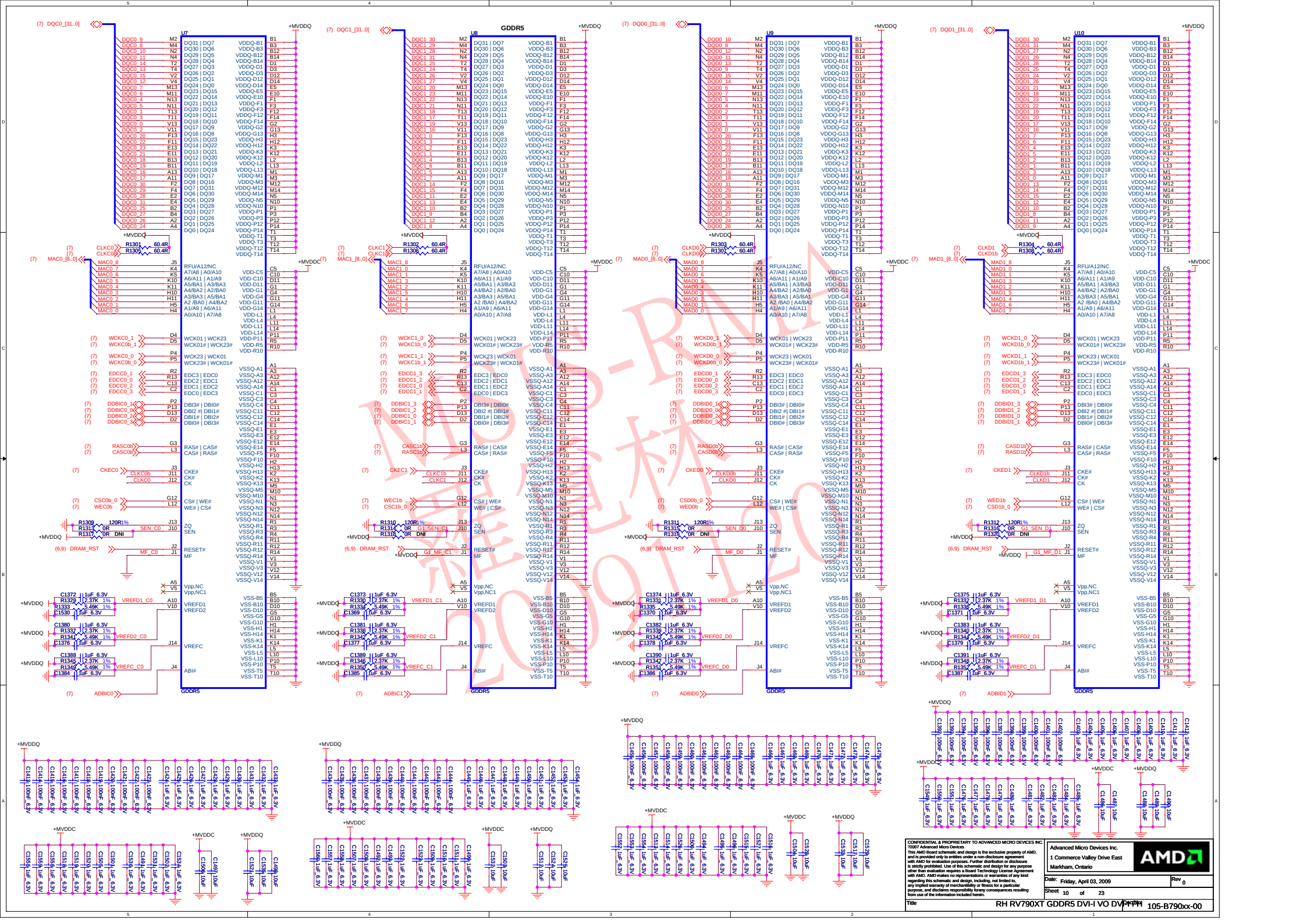

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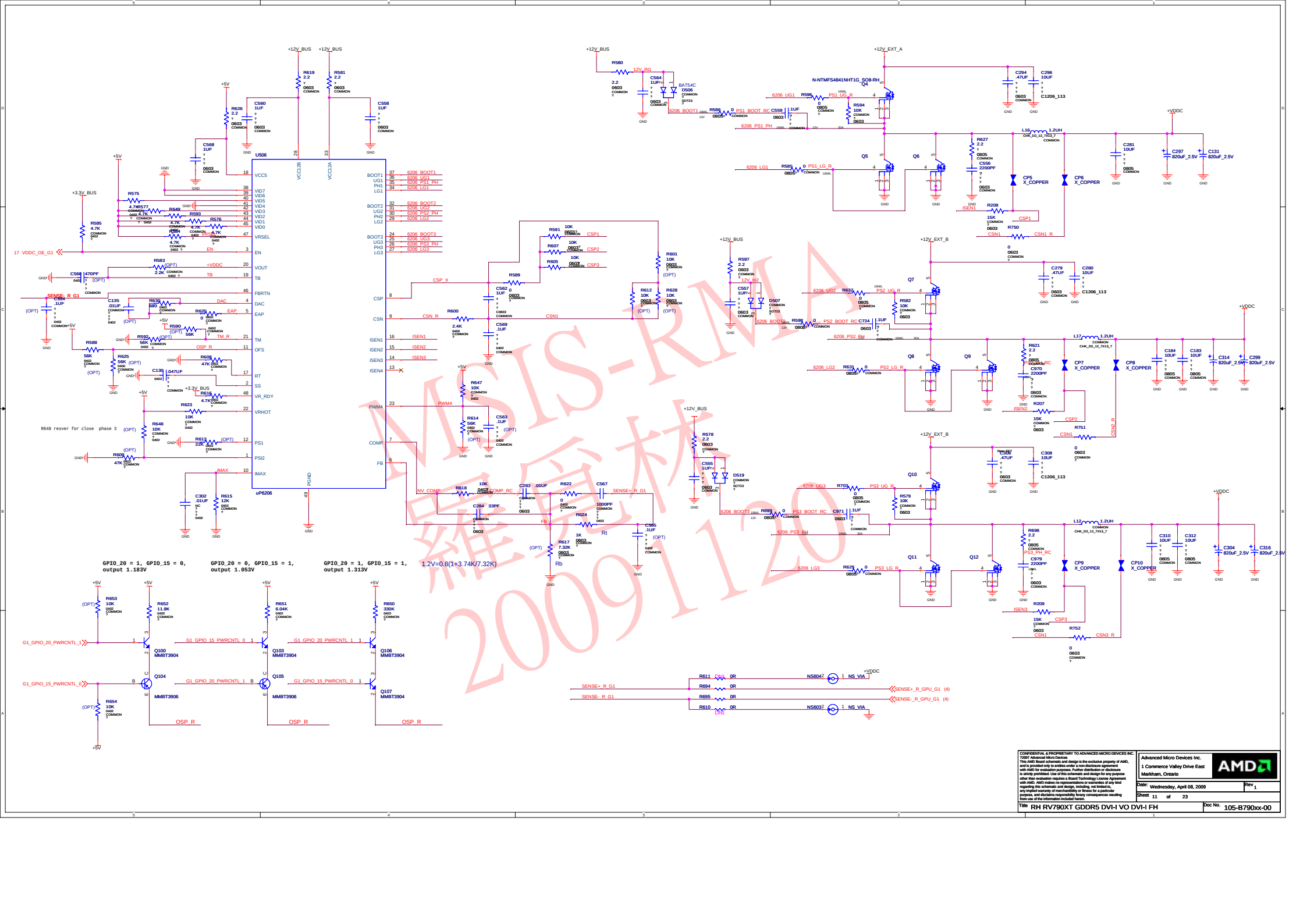

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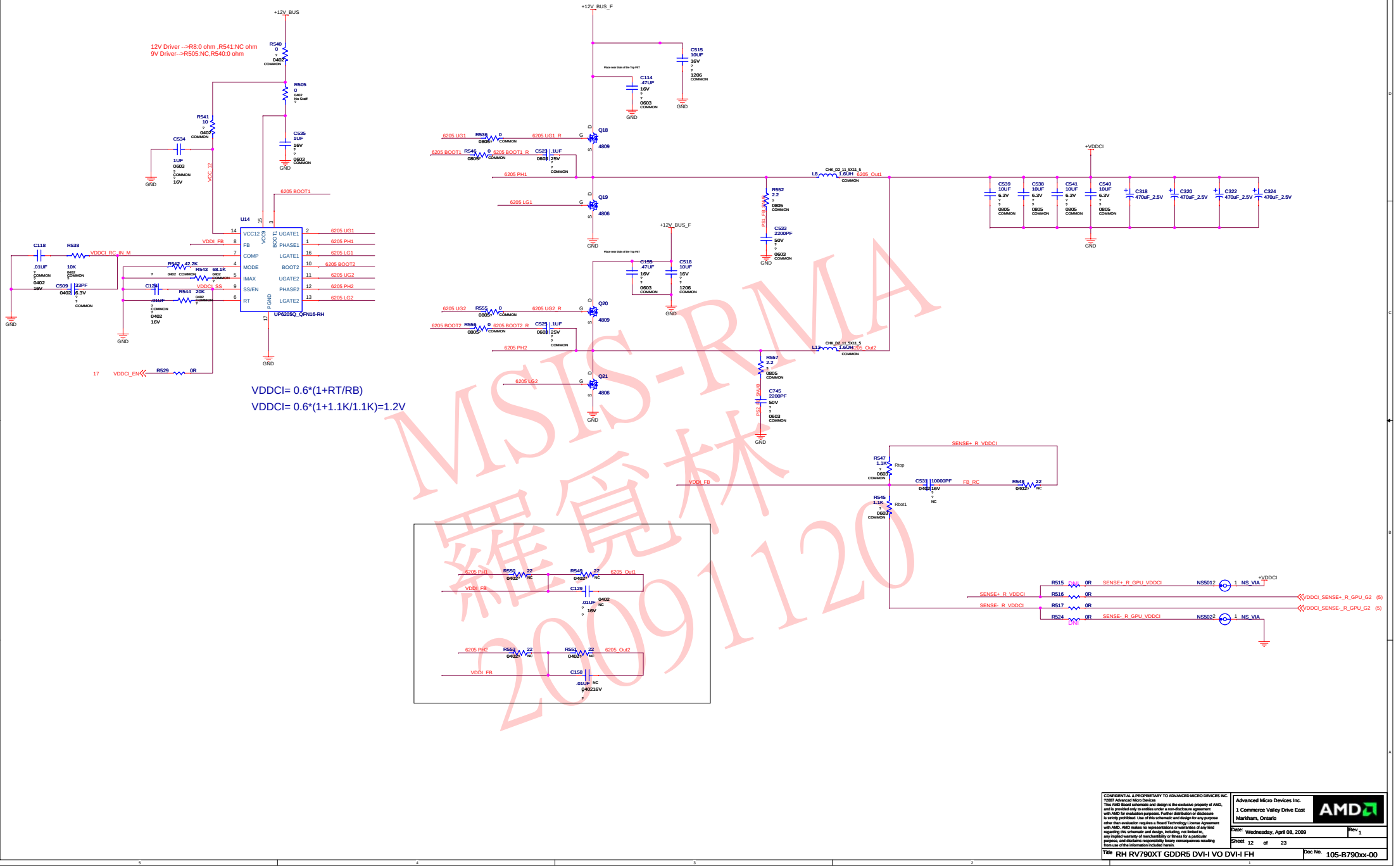

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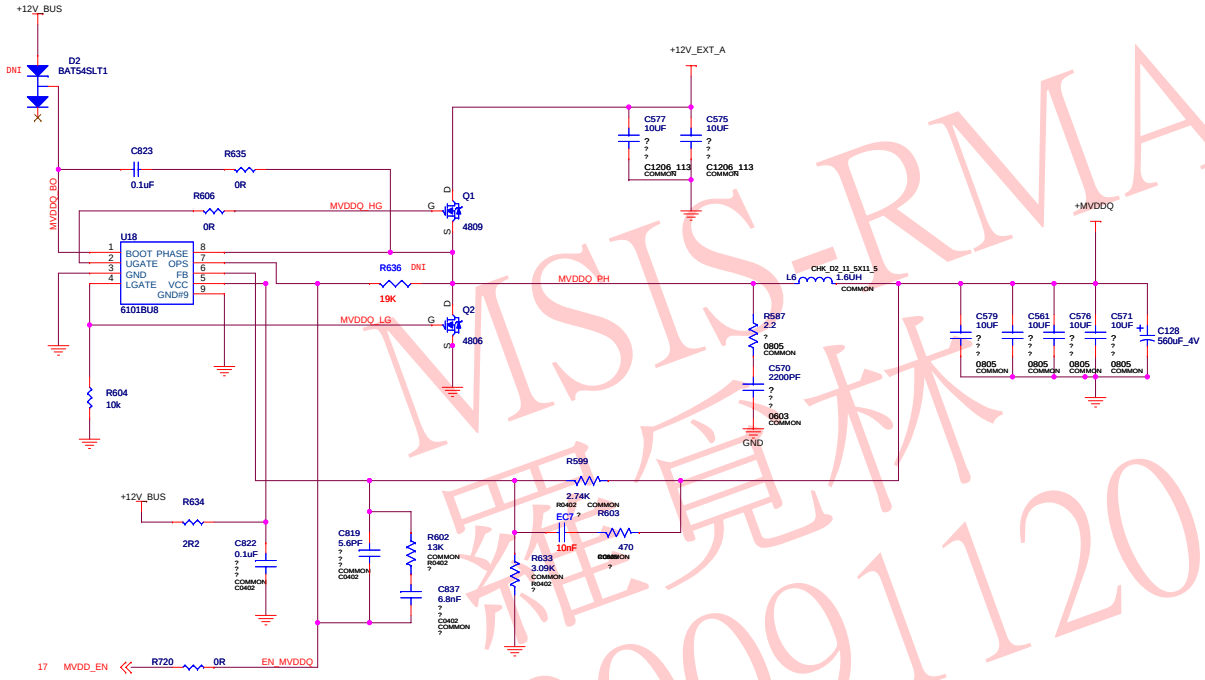

+MVDDQ=0.8*(1+(R592 / R591)

+MVDDQ=0.8*(1+(2.74 / 3.09)=1.509V
+MVDDQ=0.8*(1+(2.74 / 2.94)=1.545V

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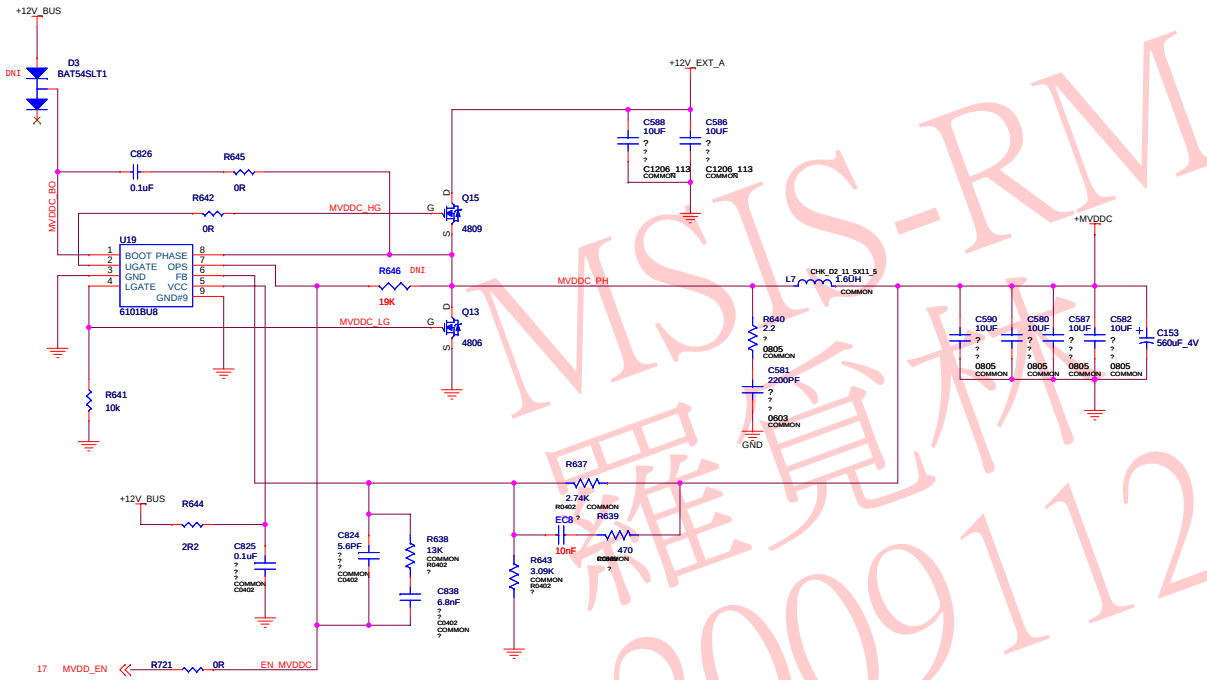

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+MVDDQ=0.8*(1+(R592 / R591)

+MVDDQ=0.8*(1+(2.74 / 3.09)=1.509V
+MVDDQ=0.8*(1+(2.74 / 2.94)=1.545V

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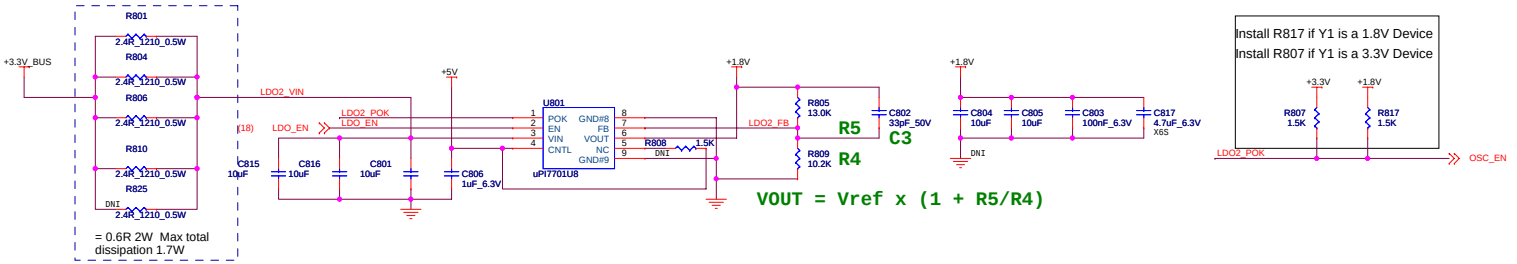
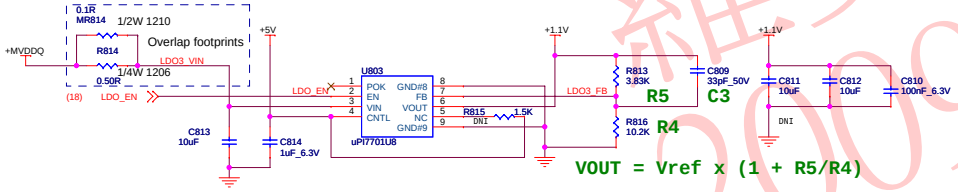
LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 1.7A (TBV) RMS MAX

PCB: Min 70mm sq. copper area for cooling



LDO #3: Vin = +1.50V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX

PCB: Min 70mm sq. copper area for cooling



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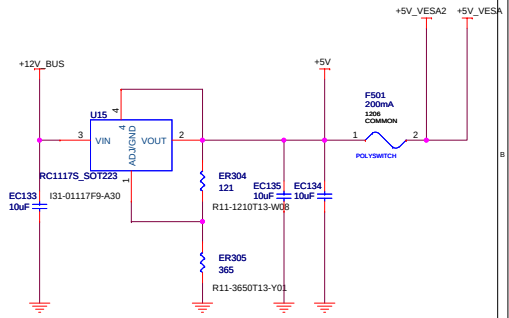
Regulators for +5V, +5V_VESA and +5V_VESA2



Vout=1.25V* [1+(ER305/ER304)]

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See BOM for qualified filters

(3) A_DAC1_R — R1001 75R 402 — C1004 8.0pF 402 — L1001 47nH ML1001 36NH — C1001 12pF_50V 402
(3) A_DAC1_RB — R1027 37.4R
(3) A_DAC1_G — R1002 75R 402 — C1005 8.0pF 402 — L1002 47nH ML1002 36NH — C1002 12pF_50V 402
(3) A_DAC1_GB — R1028 37.4R
(3) A_DAC1_B — R1003 75R 402 — C1006 8.0pF 402 — L1003 47nH ML1003 36NH — C1003 12pF_50V 402
(3) A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

L100x and ML100x footprints are overlapped

For ESD Protection

+3.3V — D1001 CM1213-04 (CH3, CH2, Vp, Vn, CH4, CH1)
+5V_VESA — D1002 CM1213-04 (CH3, CH2, Vp, Vn, CH4, CH1)

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

+5V_VESA — C1010 68pF 603

MJ1001 G3179C219-005
R, G, B, MS0, MS1, MS2, MS3, NC, HS, VS, VSS, VSS#6, VSS#7, VSS#8, VSS#10, CASE, CASE#17

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

(3) DDC4DATA — +5V — R1005 2.2K — DDCDATA_DAC1_5V — R1006 33R 402 — DDCDATA_DAC1_R
(3) DDC4CLK — +5V — R1008 2.2K — DDCCLK_DAC1_5V — R1009 33R 402 — DDCCLK_DAC1_R

(3,8) HSYNC1 — U1999C 74VHC125 — HSYNC_DAC1_B — R1010 10R 402 — HSYNC_DAC1_R
(3,8) VSYNC1 — U1999D 74VHC125 — VSYNC_DAC1_B — R1011 10R 402 — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

+3.3V — Q1021 MMBT3904 — R1022 10K — HPD_DVI2
(3) HPD1 — R1023 10K

+5V_VESA — J1001 DVI_CONNECTOR

25	CASE		
1	TMDS Data2-	(3)	T2X2M
2	TMDS Data2+	(3)	T2X2P
3	TMDS Data2/4 Shield		
4	TMDS Data4-	(3)	T2X4M
5	TMDS Data4+	(3)	T2X4P
6	DDC Clock		DDCCLK_DAC1_R
7	DDC Data		DDCDATA_DAC1_R
8	Analog VSYNC		VSYNC_DAC1_R
9	TMDS Data1-	(3)	T2X1M
10	TMDS Data1+	(3)	T2X1P
11	TMDS Data1/3 Shield		
12	TMDS Data3-	(3)	T2X3M
13	TMDS Data3+	(3)	T2X3P
14	+5V Power		
15	GND (for +5V)		
16	Hot Plug Detect		HPD_DVI2
17	TMDS Data0-	(3)	T2X0M
18	TMDS Data0+	(3)	T2X0P
19	TMDS Data0/5 Shield		
20	TMDS Data5-	(3)	T2X5M
21	TMDS Data5+	(3)	T2X5P
22	TMDS Clock Shield		
23	TMDS Clock+	(3)	T2XCP
24	TMDS Clock-	(3)	T2XCM
C1	Analog Red		A_R_DAC1_F
C2	Analog Green		A_G_DAC1_F
C3	Analog Blue		A_B_DAC1_F
C4	Analog HYNC		HSYNC_DAC1_R
C5	Analog GND		
C6	Analog GND#C6		
26	CASE#26		
27	CASE#27		
28	CASE#28		
29	CASE#29		
30	CASE#30		

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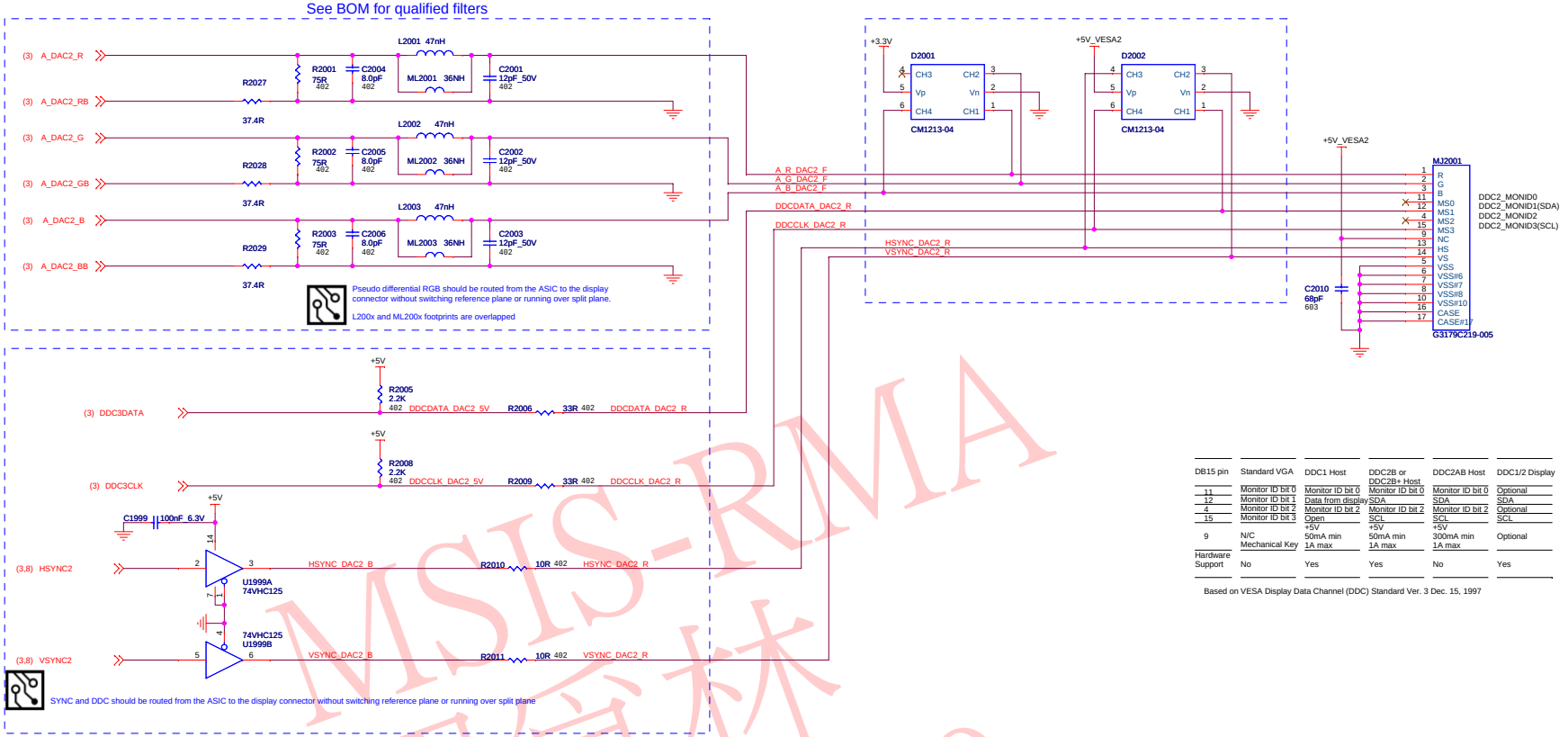
See BOM for qualified filters



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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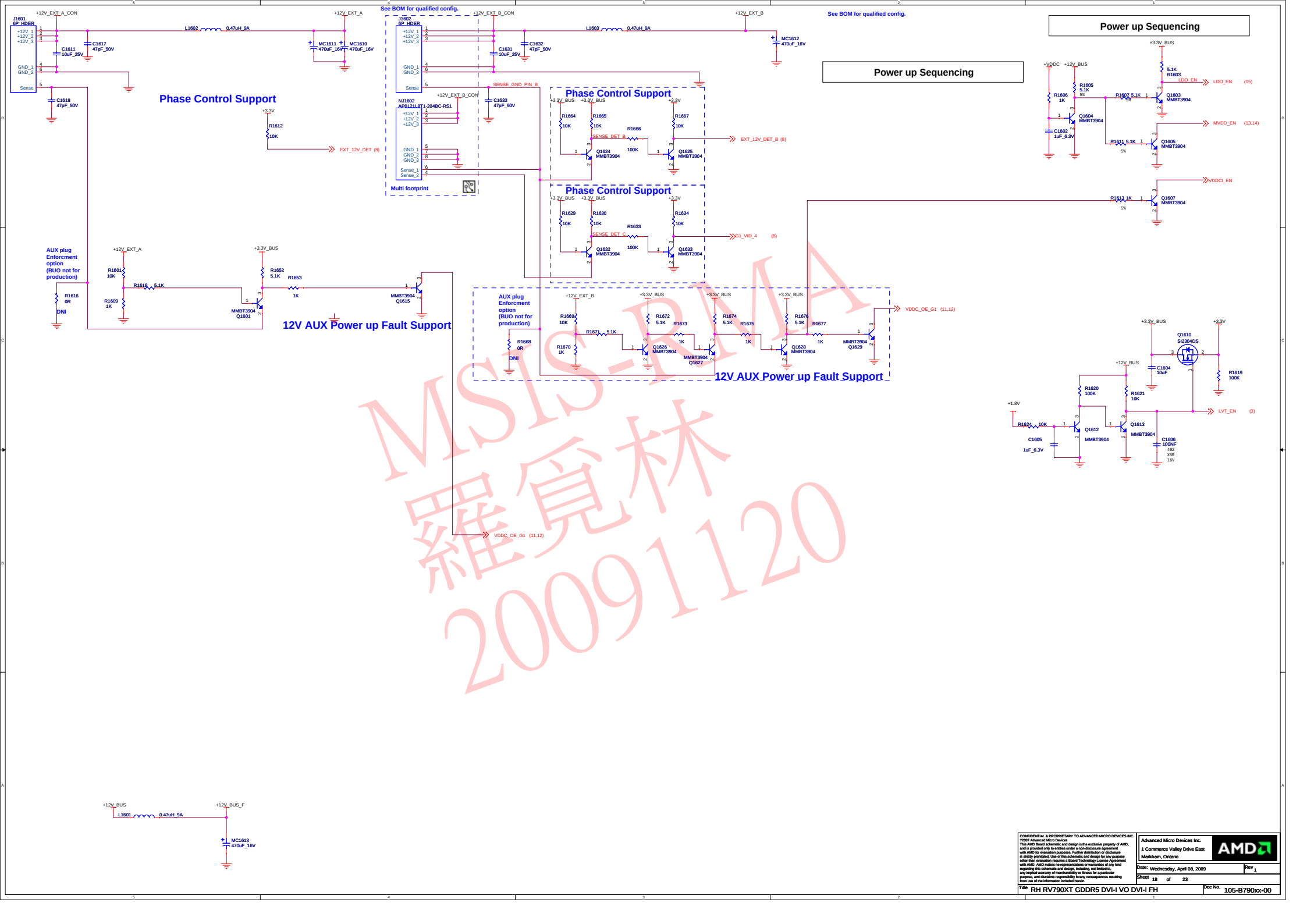

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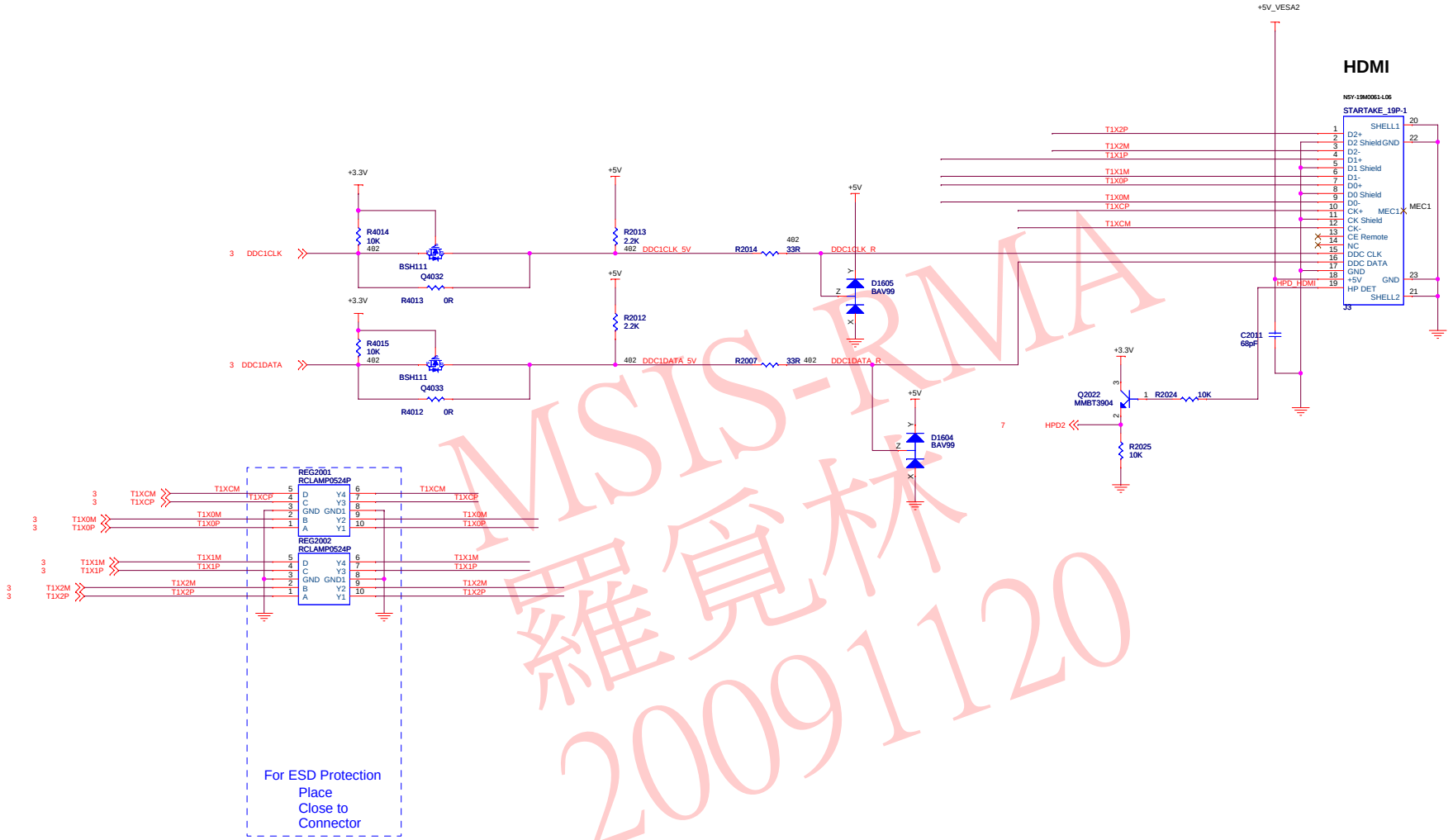

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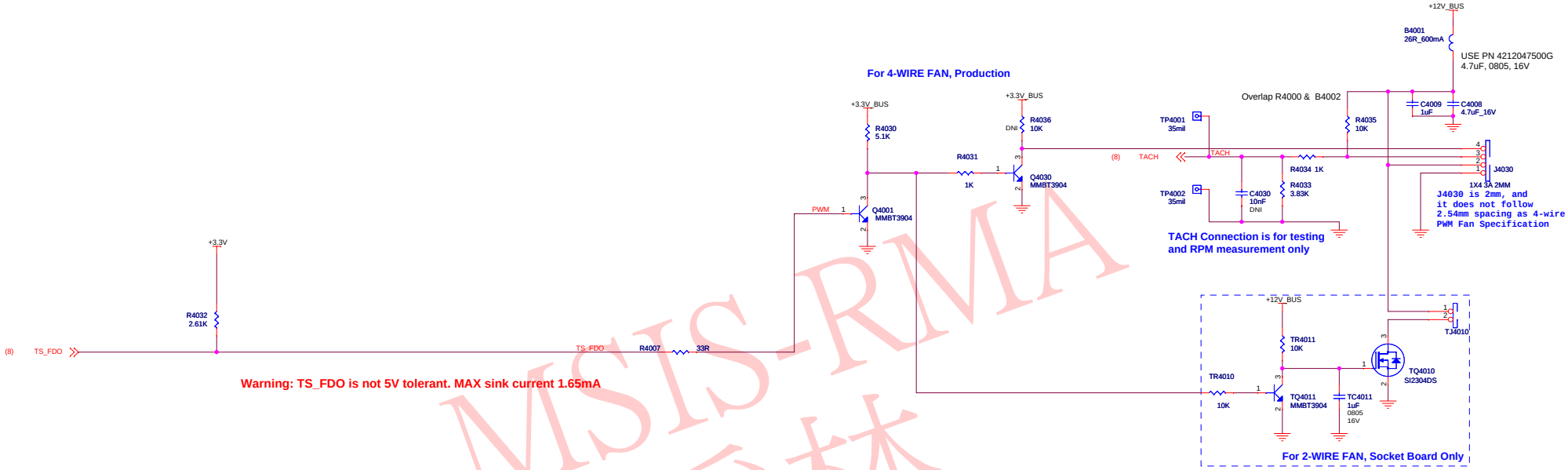

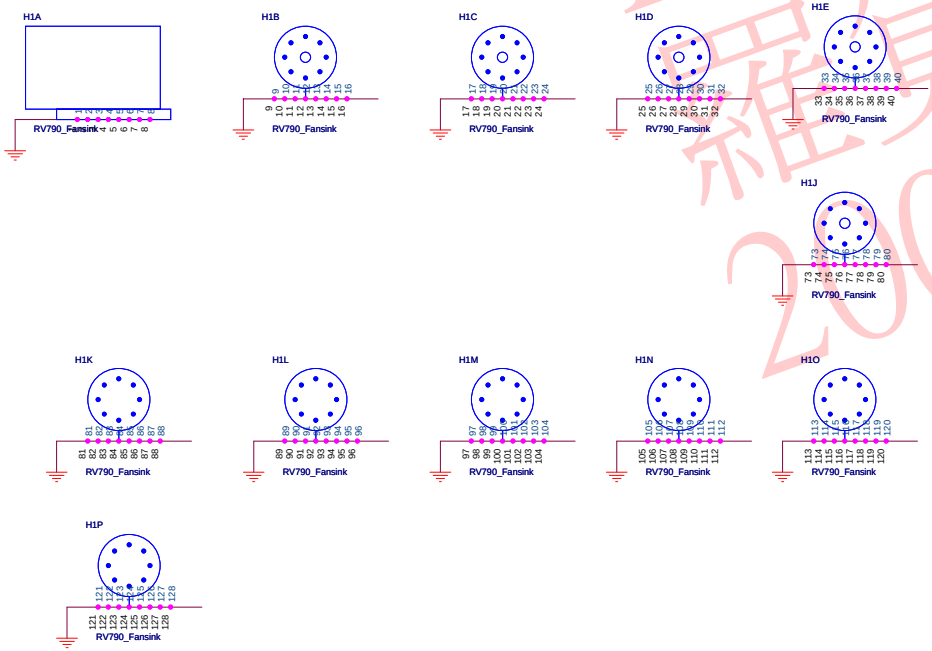

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SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
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FAN
Socket_RV770

PCB
PCB
V194-200

ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET DUAL
80200388B0G

SCREW5
SCREW
SCREW

BKT1: DS, DVI - DIN - DVI

FM1 FM2 FM3 FM4
OPT
F_PAD_X
<New PN>

FM5 FM6
OPT
F_PAD_X
<New PN>

J11 X_PIN1*2 GND
J12 X_PIN1*2 GND
J13 X_PIN1*2 GND
J14 impedence GND GND

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Title	Schematic No.	Date:
RH RV790XT GDDR5 DVI-I VO DVI-I FH	105-B790xx-00	Friday, April 03, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	08/01/04	Initial design for B790
	00	09/02/03	-00 Release with no Schematic change however C817 is refreshed to correct the footprint issue on rev A

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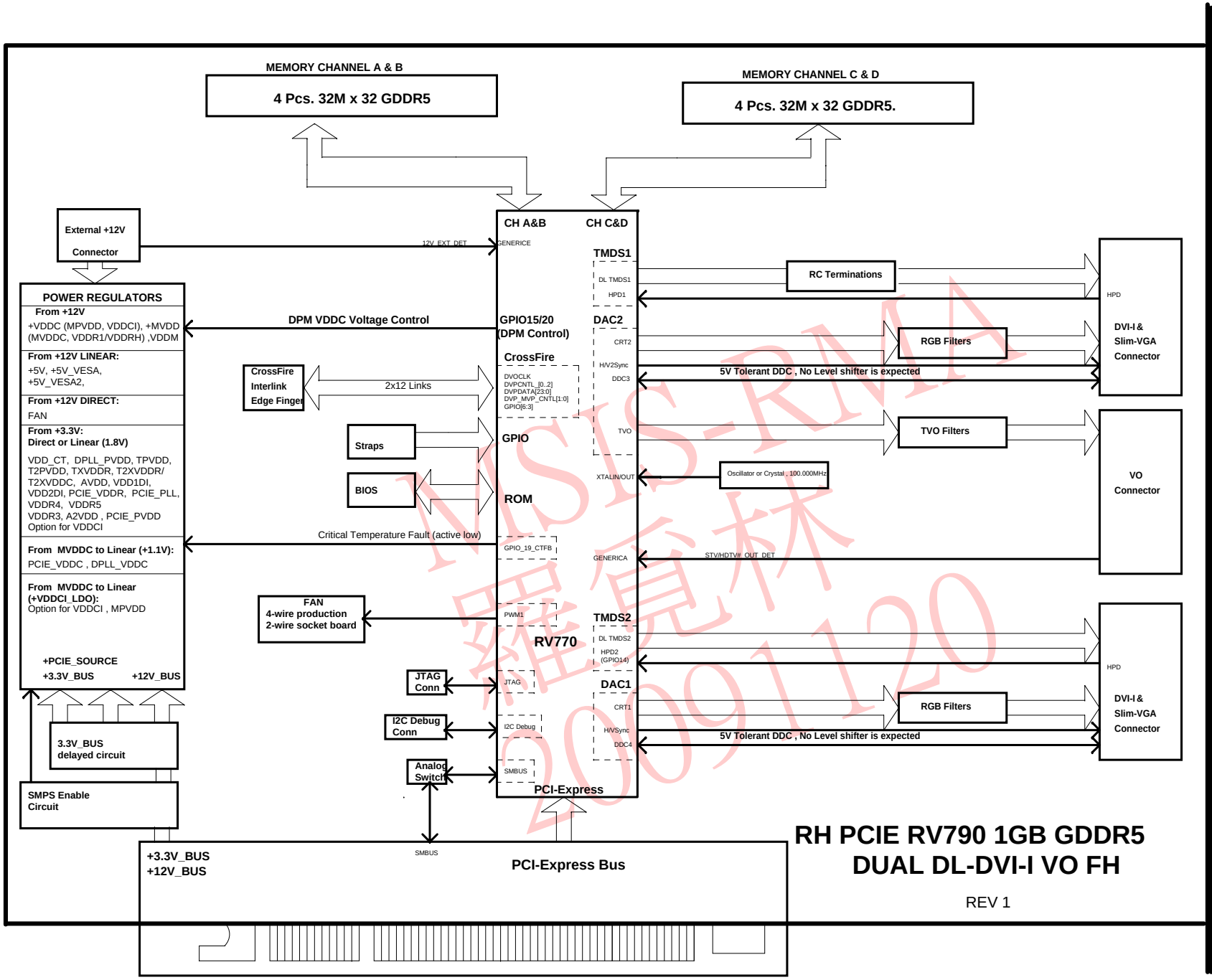

RH PCIE RV790 1GB GDDR5
DUAL DL-DVI-I VO FH

REV 1

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