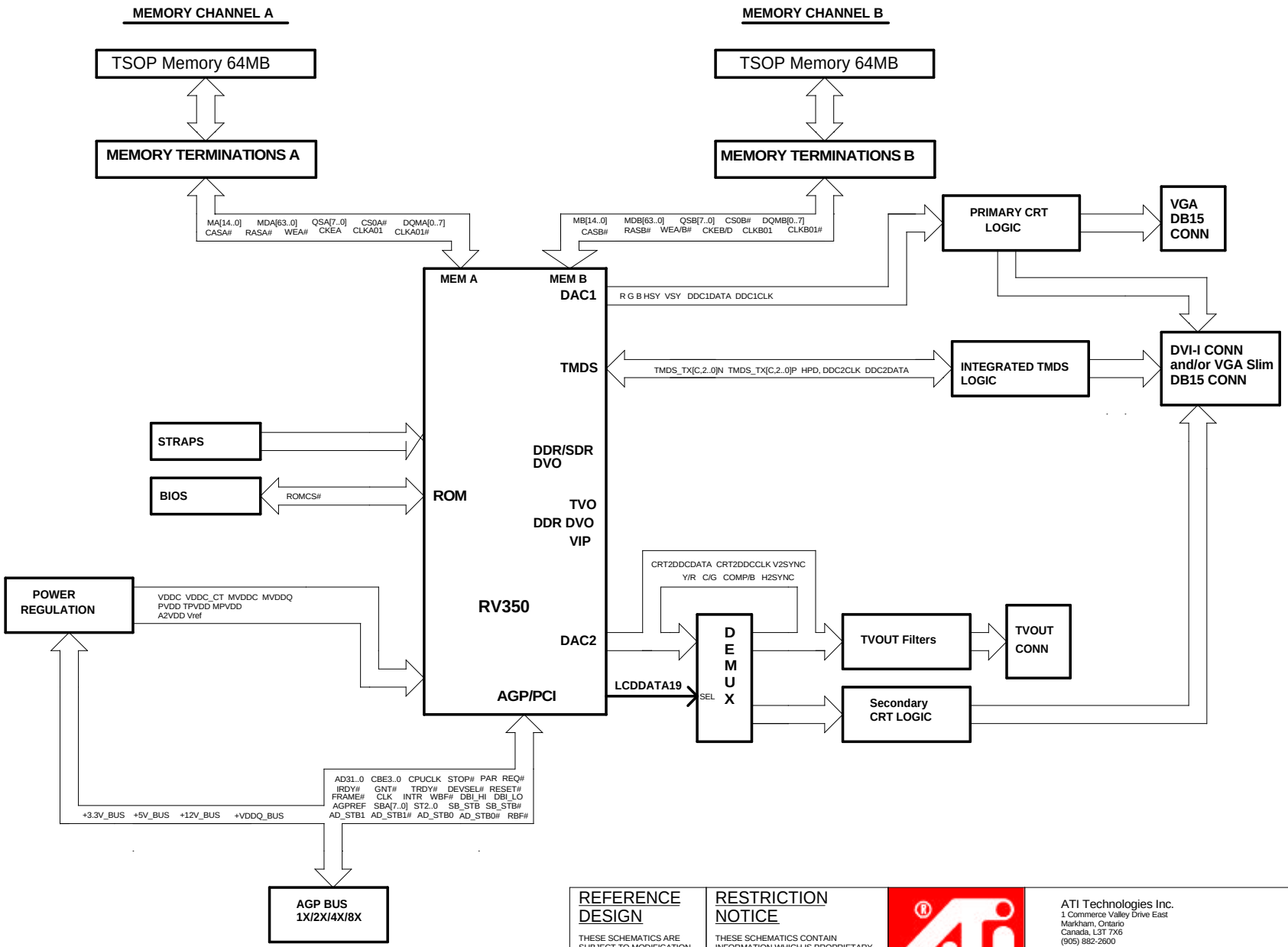


REFERENCE DESIGN

THESE SCHEMATICS ARE SUBJECT TO MODIFICATION AND DESIGN IMPROVEMENTS. PLEASE CONTACT ATI FIELD APPLICATION ENGINEERING BEFORE USING THE INFORMATION CONTAINED HEREIN.

RESTRICTION NOTICE

THESE SCHEMATICS CONTAIN INFORMATION WHICH IS PROPRIETARY TO AND IS THE PROPERTY OF ATI, AND MAY NOT BE USED, REPRODUCED OR DISCLOSED IN ANY MANNER WITHOUT EXPRESSED WRITTEN PERMISSION FROM ATI.

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO	
Size B	Document Number 105-A035XX-00	Rev 2
Date: Thursday, April 17, 2003	Sheet 1 of 16	

LAYOUT NOTE: SOME OF THE CAPS BELOW MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

+12V_BUS — C10 10uF_20V 4239010600
+5V_BUS — C5 47uF_6.3V
+3.3V_BUS — C8 47uF_6.3V
+VDDQ_BUS — C2 100uF_6.3V >= 6.3V

Use 47uF Tant. 16V 20% D size (P/N 4230047600), 800mR Max. ESR and Max. ripple 430mA @ 100kHz
or
100uF, Alum. 6.3V 20% 6.3mm dia (P/N 4261010700), 440mR Max. ESR and Max. ripple 230mA @ 100kHz
or
47uF, Alum. 6.3V 20% 5mm dia (P/N 4262047600), 760mR Max. ESR and Max. ripple 150mA @ 100kHz

Place C2 on left side of AGP connector

4X/8X AGP BUS

GND_MPVSS GND_TPVSS GND_A2VSSN GND_AVSSQ GND_RSET
GND_AVSSN GND_PVSS GND_TXVSSR GND_A2VSSQ GND_RZSET

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

SYMBOL LEGEND
DNI — DO NOT INSTALL
— ACTIVE LOW
DIGITAL GROUND
ANALOG GROUND

MAGP1
1.5V_AGP_BUS
614NOPN062

AGP_C/BE#[3..0] (3)
AGP_AD[31..0] (3)
AGP_SBA[7..0] (3)
AGP_ST[2..0] (3)

AGP_TYPEDET#
AGP_GC_8X_DET#
(3) AGP_INTR#
(3) AGP_RESET#
(3) AGP_GNT#
AGP_ST1
(3) AGP_MB_8X_DET#
(3) AGP_DBI_HI
(3) AGP_WBF#
AGP_SBA1
AGP_SBA3
(3) AGP_SBSTB#
AGP_SBA5
AGP_SBA7
AGP_AD30
AGP_AD28
AGP_AD26
AGP_AD24
(3) AGP_ADSTB1#
AGP_C/BE#3
AGP_AD22
AGP_AD20
AGP_AD18
AGP_AD16
(3) AGP_FRAME#
(3) AGP_TRDY#
(3) AGP_STOP#
(3) AGP_PAR
AGP_PAR_R
AGP_AD15
AGP_AD13
AGP_AD11
AGP_AD9
AGP_C/BE#0
(3) AGP_ADSTB0#
AGP_AD6
AGP_AD4
AGP_AD2
AGP_AD0
AGP_VREFGC

R1 0R
R5 0R
R12 0R

AGP_ST0
AGP_ST2
AGP_SBA0
AGP_SBA2
AGP_SBA4
AGP_SBA6
AGP_AD31
AGP_AD29
AGP_AD27
AGP_AD25
AGP_AD23
AGP_AD21
AGP_AD19
AGP_AD17
AGP_C/BE#2
AGP_C/BE#1
AGP_AD14
AGP_AD12
AGP_AD10
AGP_AD8
AGP_AD7
AGP_AD5
AGP_AD3
AGP_AD1
AGP_AGPREF

AGP_AGPCLK (3)
AGP_REQ# (3)
AGP_RBF# (3)
AGP_DBI_LO (3)
AGP_SBSTB_R R2 0R → AGP_SBSTB (3)
AGP_ADSTB1_R R6 0R → AGP_ADSTB1 (3)
AGP_IRDY# (3)
AGP_DEVSEL# (3)
AGP_ADSTB0_R R13 0R → AGP_ADSTB0 (3)

+12V_BUS +5V_BUS +3.3V_BUS
C4 100nF, C9 100nF, C15 100nF
Caps for EMI - install close to AGP connector

AGP_TYPEDET# — R19 0R
For retail, 1K ohm pull-down causes AMD system detects AGP2X only
+12V, TYPEDET# short protection for OEM (1KR)

AGP_GC_8X_DET# — R60 0R

UNIVERSAL VREFGC CIRCUIT (4X, 8X)

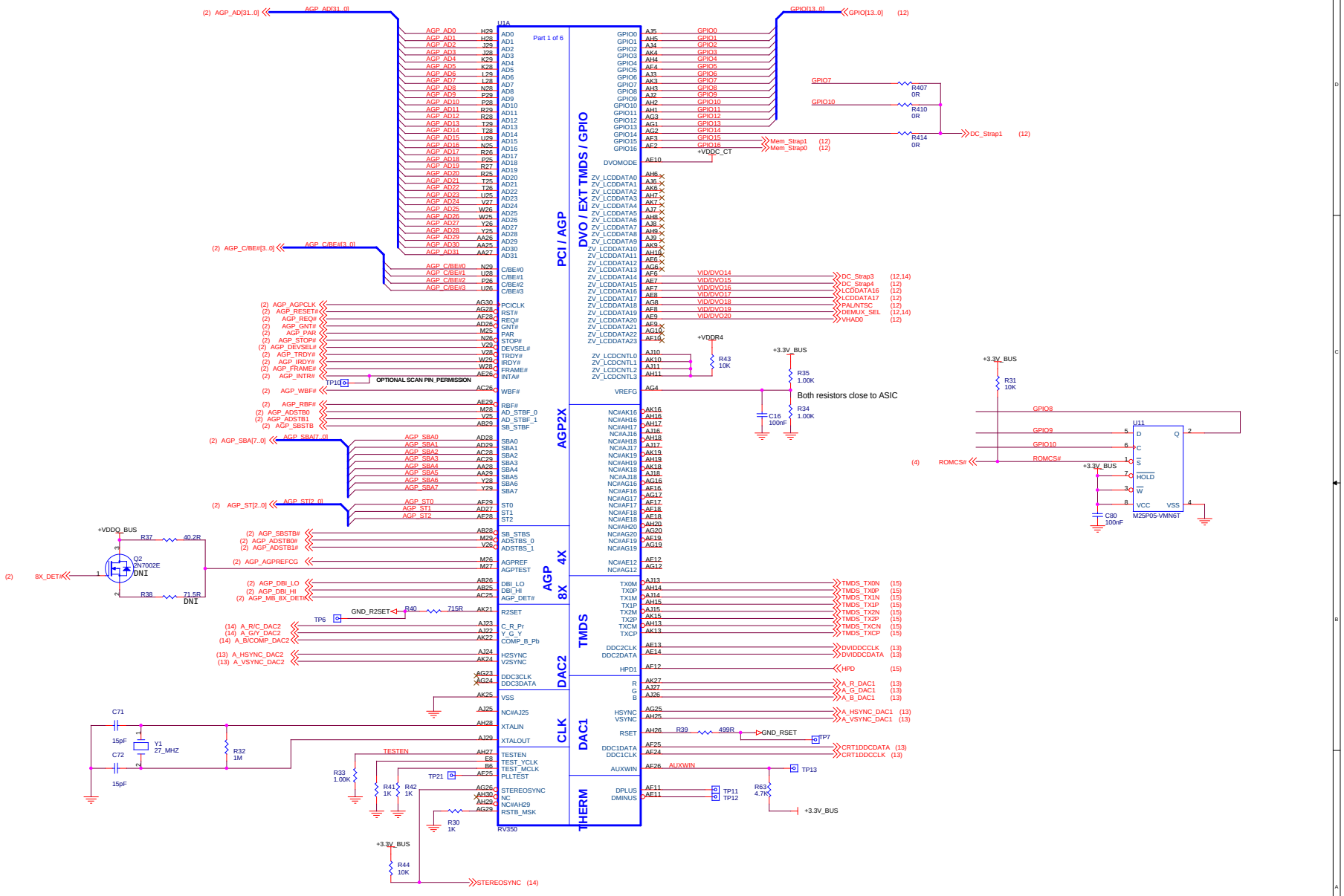
+3.3V_BUS, +12V_BUS, (3) 8X_DET#, +VDDQ_BUS
R17 47K, R3 20K, Q12 BSN20
(3) AGP_MB_8X_DET# → AGP_MB_8X_DET#
TEST
Q1 2N7002E, R20 324R, R21 147R
AGP_VREFGC
R24 100R, C6 10nF Close to ASIC
+5V_BUS, C3 100nF, U2 TC7SZ08FU, R23 1K
May be placed far from connector -- place C3 FAR from connector, on left side!!

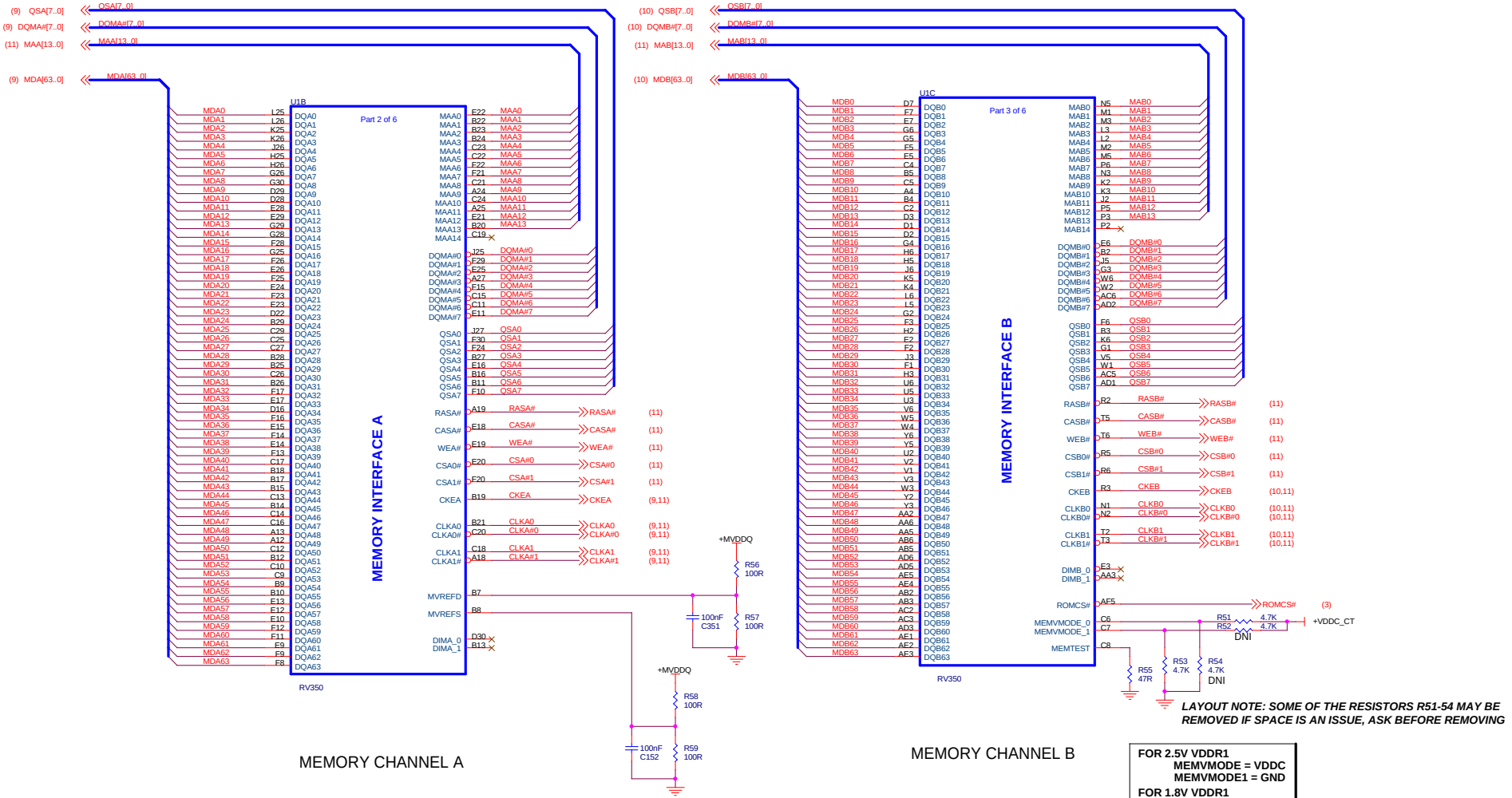
UNIVERSAL VREFCG CIRCUIT (4X, 8X)

AGP_AGPREF
+VDDQ_BUS
TEST
Q5 2N7002E
R66 324R, R64 DNI 0R
R67 147R
R65 100R, C7 10nF Close to ASIC
AGP_AGPREFCG → AGP_AGPREFCG (3)

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO	
Size C	Document Number 105-A035XX-00	Rev 2
Date: Thursday, April 17, 2003	Sheet 2 of 16	


U1A
Part 1 of 6
PCI / AGP
DVO / EXT TMDS / GPIO
AGP2X
AGP 4X
AGP 8X
TMDS
DAC2
CLK
DAC1
THERM
RV350
OPTIONAL SCAN PIN_PERMISSION
Both resistors close to ASIC
IT IS RECOMMENDED TO ALLOW SERIES RESISTOR FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS TO ADDRESS ANY LAYOUT NOISE RELATED SIGNAL DAMPING REQUIREMENTS
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600
Title
AGP RV350 128M TSOP VGA DVI VO
Size
Custom
Document Number
105-A035XX-00
Rev
2
Date: Thursday, April 17, 2003
Sheet 3 of 16



MEMORY CHANNEL A

MEMORY CHANNEL B

PLACE C351/152 VERY CLOSE TO ASIC

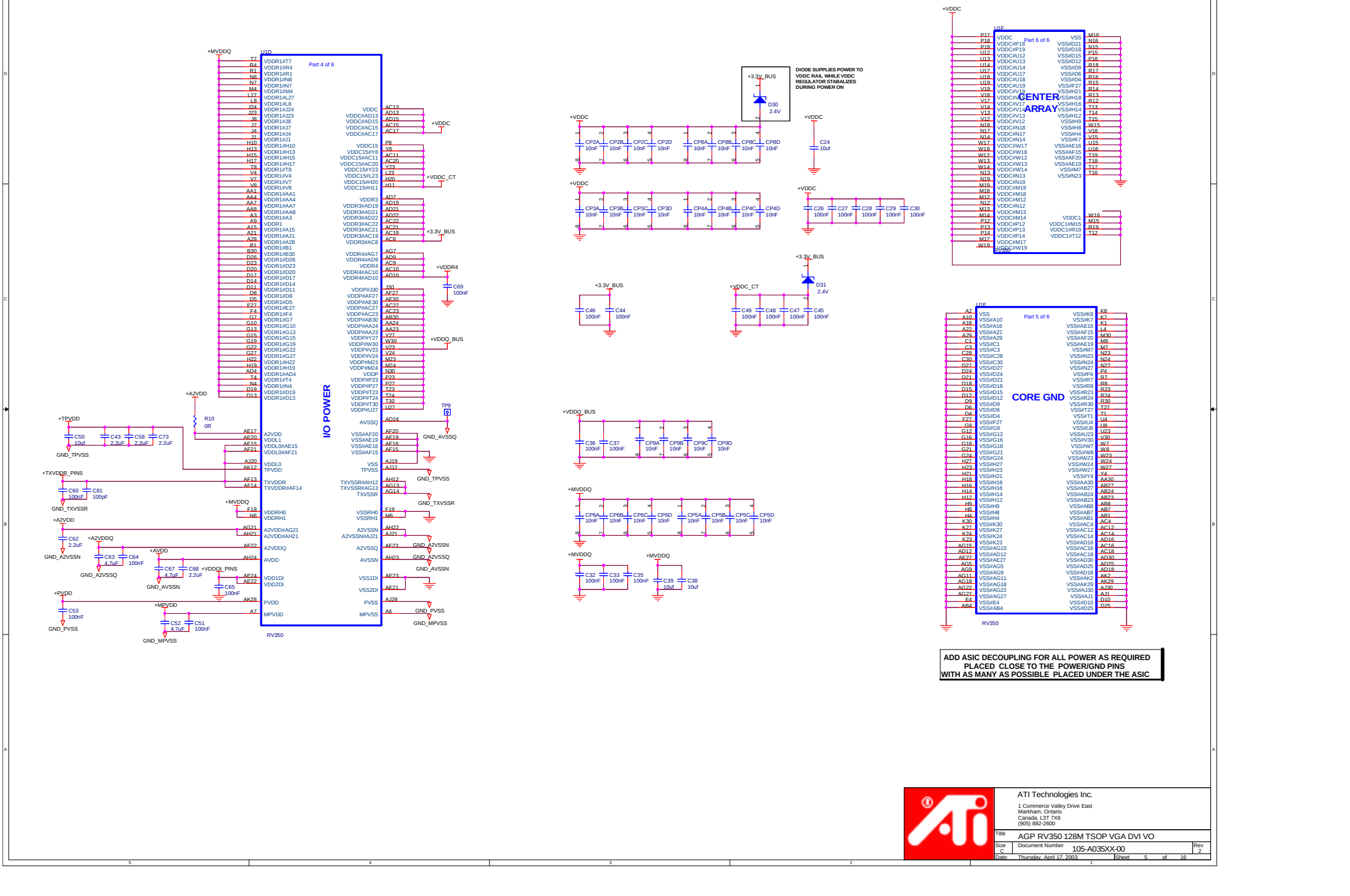
R56/57/58/59 CLOSE TO ASIC AS WELL

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

FOR 2.5V VDDR1
MEMVMODE = VDDC
MEMVMODE1 = GND
FOR 1.8V VDDR1
MEMVMODE = GND
MEMVMODE1 = VDDC
SEE DESIGN GUIDE

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO
Size	Custom
Document Number	105-A035XX-00
Rev	2
Date:	Thursday, April 17, 2003
Sheet	4 of 16



ATI Technologies Inc.

1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO	
Size: C	Document Number: 105-A035XX-00	Rev: 2
Date: Thursday, April 17, 2003	Sheet 5 of 16	

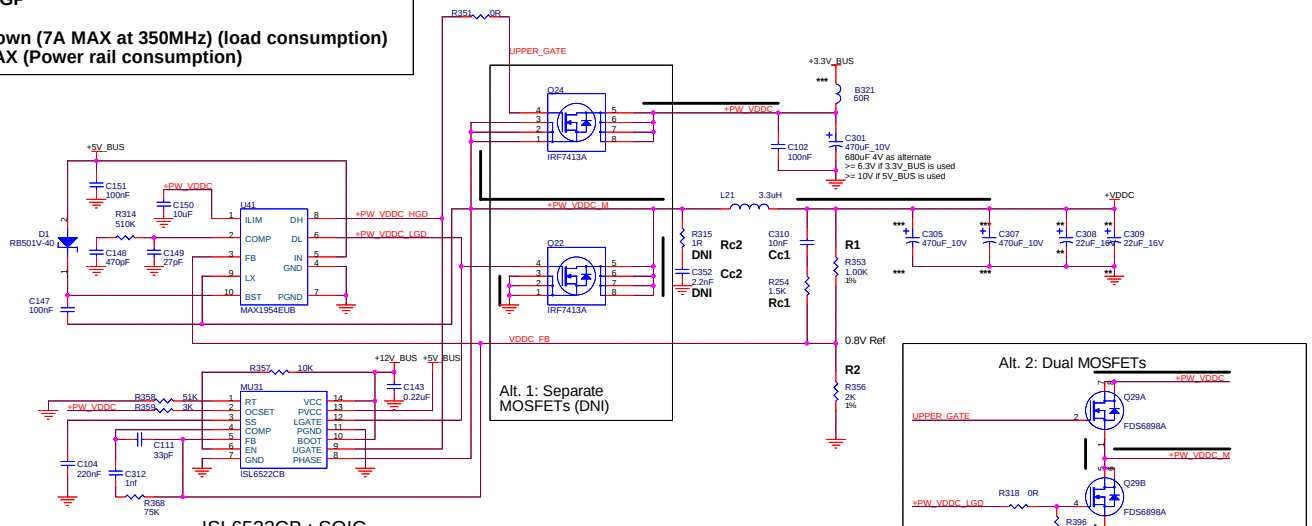
Regulator for VDDC (ASIC Core)

Vin = 3.3V AGP
Vout = 1.2V
Iout = Unknown (7A MAX at 350MHz) (load consumption)
Iout = 3A MAX (Power rail consumption)

Part	NOTES
MAX1954	Do not install Cc1, Rc1 Do not install Cc2, Rc2
ISL6522	Do not install Cc2, Rc2 Install Cc1, Rc1

*** Indicate number of via required for the connection

Part	Vout	R1	R2
MAX1954 ISL6522 0.8V Ref	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240110100
	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N
	1.62V	1.00K 1% ATI P/N 3240100100	976R 1% ATI P/N 3240976000
	2.5V	1.00K 1% ATI P/N 3240100100	475R 1% ATI P/N 3240475300
	3.3V TSOP Memory	1.00K 1% ATI P/N 3240100100	324R 1% ATI P/N 3240332000
	3.45V TSOP Memory	1.00K 1% ATI P/N 3240100100	301 1% ATI P/N 3240301000

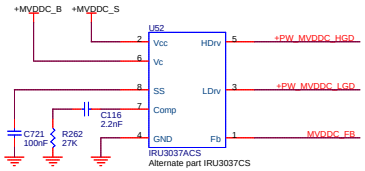


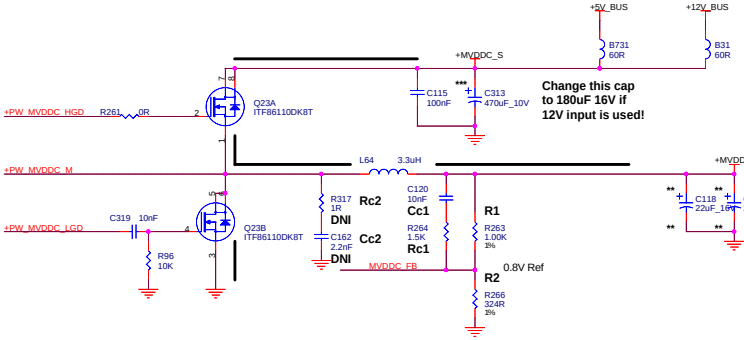
ISL6522CB : SOIC

Regulator for MVDDC (MEM Core)

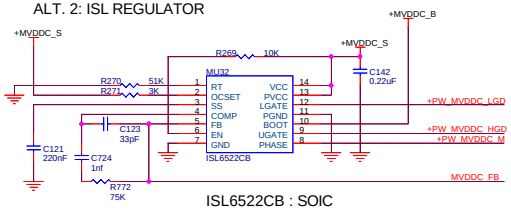
Vin = 5V AGP
Vout = 3.3V ~ 3.45V
Iout = 2.7A (330mA x 8) MAX, Burst Mode (load consumption)
Iout (5V) = 2A MAX (Power rail consumption)

ALT. 1: IRU REGULATOR



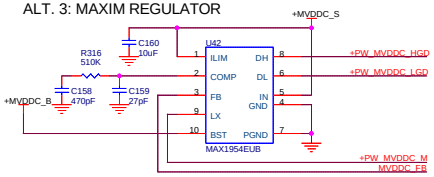


ALT. 2: ISL REGULATOR



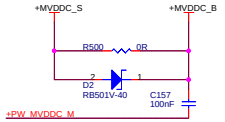
ISL6522CB : SOIC

ALT. 3: MAXIM REGULATOR



DO NOT USE MAXIM REGULATOR IF 12V INPUT IS USED!!!

Boot circuit



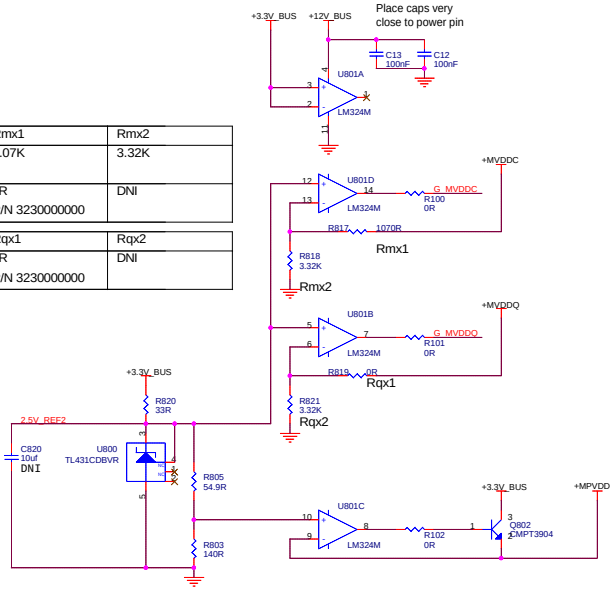
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO	
Size C	Document Number 105-A035XX-00	Rev 2
Date: Thursday, April 17, 2003	Sheet 6 of 16	

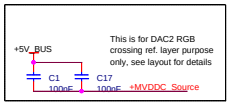
New regulator for MVDDQ, 64MB MVDDC and MPVDD

+MVDDC	Voltage Req.	Rmx1	Rmx2
Hynix	3.3V [-0.02V/+0.02V]	1.07K	3.32K
Sumsung	2.5V	0R P/N 3230000000	DNI

+MVDDQ	Voltage Req.	Rqx1	Rqx2
	2.5V	0R P/N 3230000000	DNI

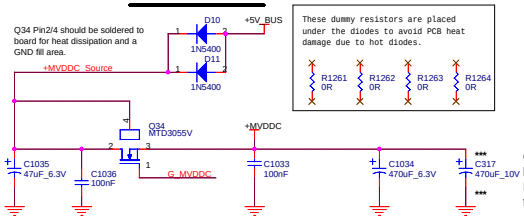


This is for DAC2 RGB crossing ref. layer purpose only, see layout for details

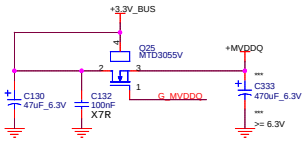


Q34 Pin2/4 should be soldered to board for heat dissipation and a GND fill area.

These dummy resistors are placed under the diodes to avoid PCB heat damage due to hot diodes.



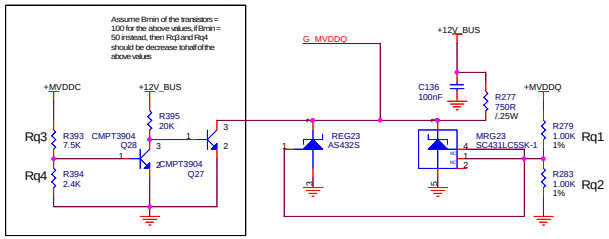
C1034 and C317 are both 470uF caps on MVDDC, populate the thru-hole if possible



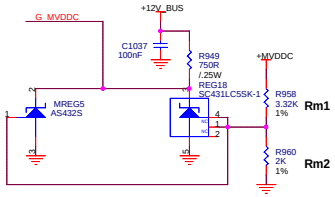
Old regulator for MVDDQ (MEM IO) & VDDR1
Vin = 3.3V AGP
Vout = 2.5V
Iout = 1200mA MAX
Iout = 1000mA Est. MAX

Type	Voltage Req.	Rq1	Rq2
Elpida	1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
	2.5V	1K 3240100100	1K 3240100100
	2.6V	4.75K 3240475100	4.32K 3240432100

+MVDDC	Rq3	Rq4
3.45V (TSOP)	7.5K 3230075200	2.4K 3230024200

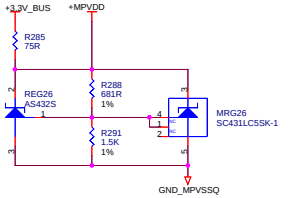


Regulator for MVDDC
Vin = 5V
Vout = 3.3V
Iout = 1.4A MAX



	Voltage Req.	Rm1	Rm2
Hynix	3.34V [-0.04V/+0.04V]	4.32K	2.55K
	3.45V [-0.04V/+0.04V]	4.32K	2.43K
Sumsung	2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100

Old regulator for +MPVDD
Vin = 3.3V
Vout = 1.8V
Iout = 10mA MAX

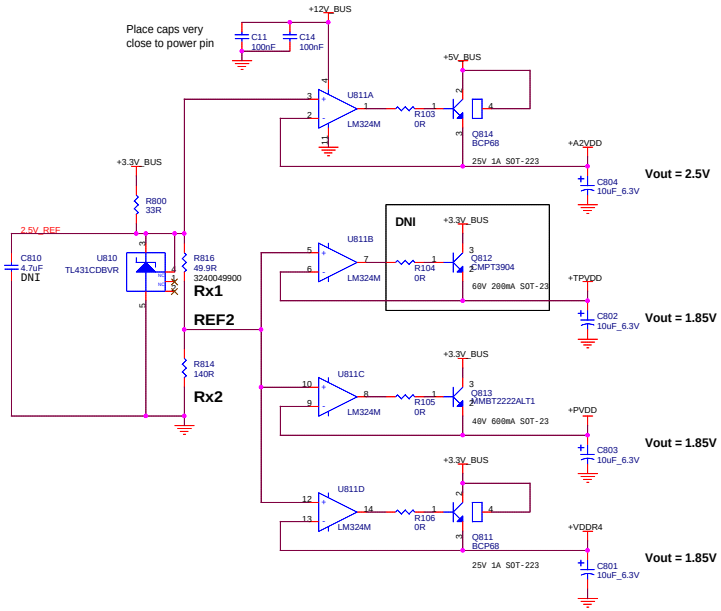


ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

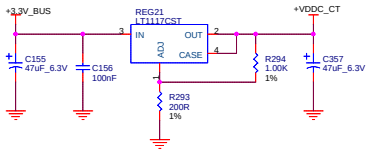
Title	AGP RV350 128M TSOP VGA DVI VO	
Size C	Document Number 105-A035XX-00	Rev 2
Date: Thursday, April 17, 2003	Sheet 7 of 16	

REF2	Rx1	Rx2
1.8V [-0.02V/+0.02V]	54.9R P/N 3240054900	140R P/N 3240140000
1.85V [-0.01V/+0.01V]	49.9R P/N 3240049900	140R P/N 3240140000

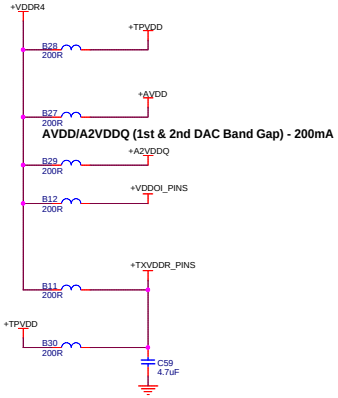
New regulator for VDDR4, PVDD, A2VDD and TPVDD



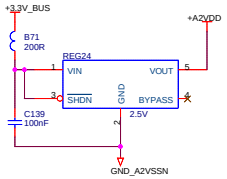
Regulator for +VDDC_CT (550mA)
Vin = 3.3V
Vout = 1.5V



Derived from VDDR4:

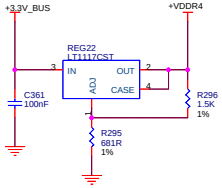


Old Regulator for +A2VDD (150mA)
Vin = +3.3V AGP
Vout = 2.5V



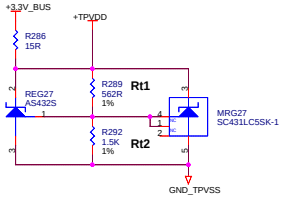
+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.

Old Regulator for +VDDR4
Vin = 3.3V
Vout = 1.8V

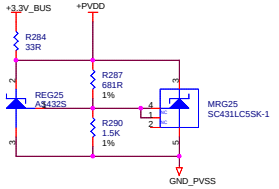


Regulator for +TPVDD (70mA)
Vin = +3.3V AGP
Vout = 1.7V

	Rt1		Rt2	
1.61V +0.01V/-0.01V	432R	3240432000	1.5K	3230015200
1.69V +0.01V/-0.01V	432R	3240432000	1.21K	3240121100
1.718V +0.01V/-0.01V	562R	3240562000	1.5K	3230015200
1.8175V +0.01V/-0.01V	681R	3240681000	1.5K	3230015200



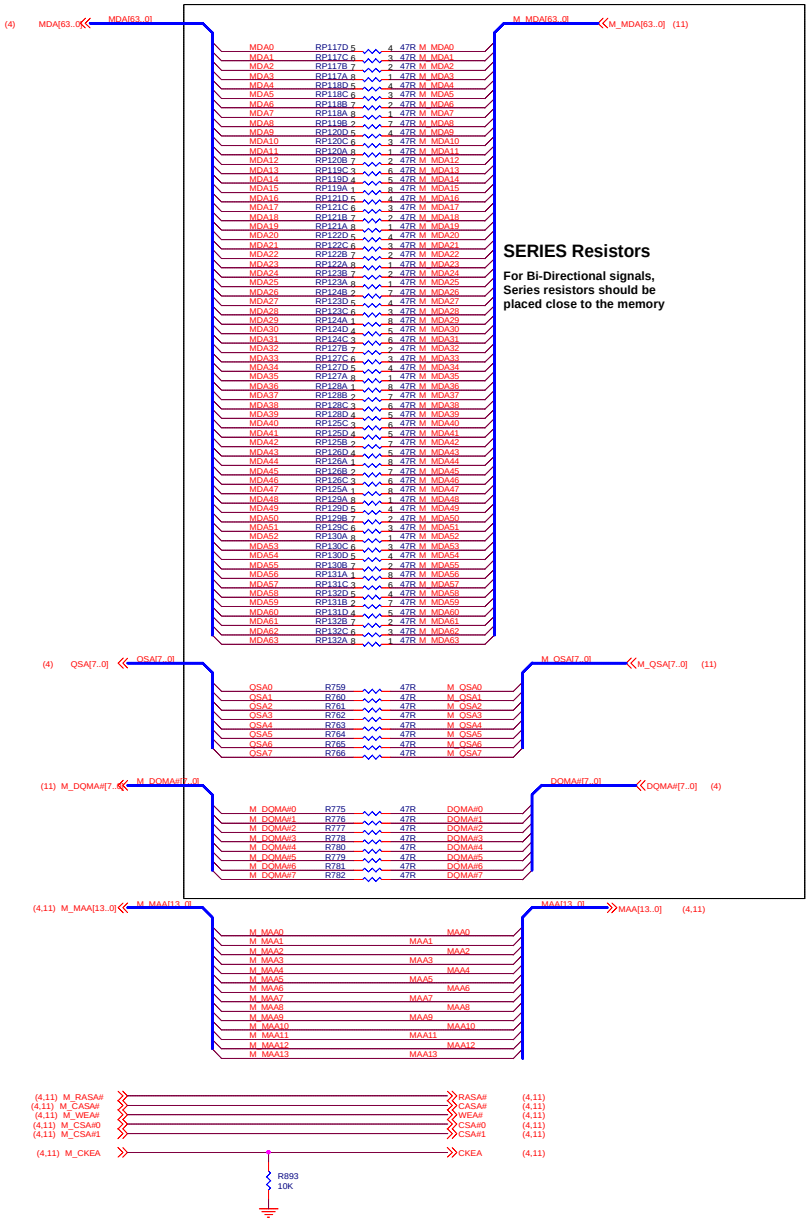
Old regulator for +PVDD (30mA)
Vin = 3.3V AGP
Vout = 1.8V



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO	
Size C	Document Number 105-A035XX-00	Rev 2
Date: Thursday, April 17, 2003	Sheet 8 of 16	

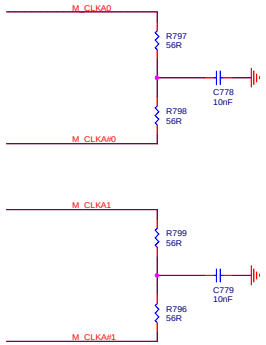
TERMINATION FOR MEMORY CHANNEL A



CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

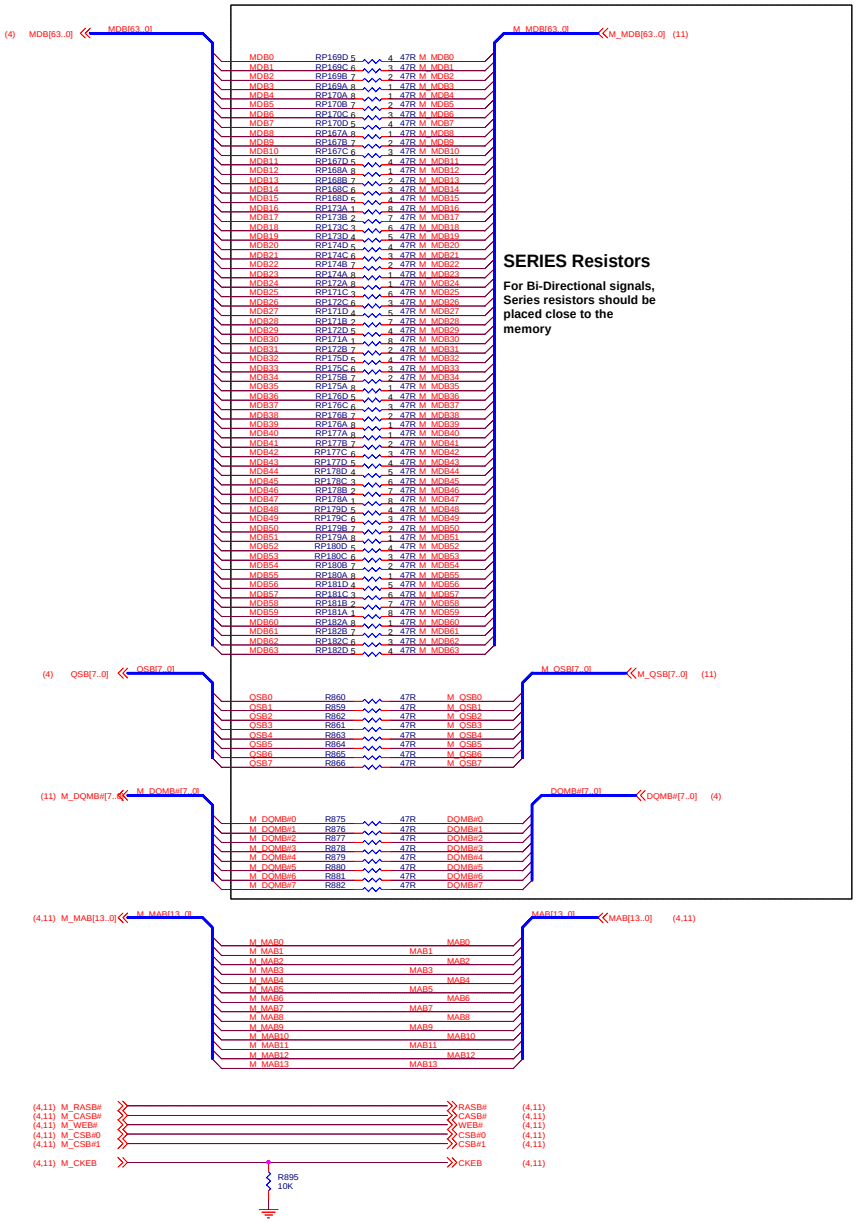


(4,11) M_CLKA0 → M_CLKA0 → CLKA0 (4,11)
(4,11) M_CLKA#0 → M_CLKA#0 → CLKA#0 (4,11)
(4,11) M_CLKA1 → M_CLKA1 → CLKA1 (4,11)
(4,11) M_CLKA#1 → M_CLKA#1 → CLKA#1 (4,11)

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO	
Size: Custom	Document Number: 105-A035XX-00	Rev: 2
Date: Thursday, April 17, 2003	Sheet 9 of 16	

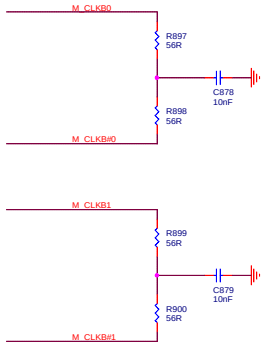
TERMINATION FOR MEMORY CHANNEL B



CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

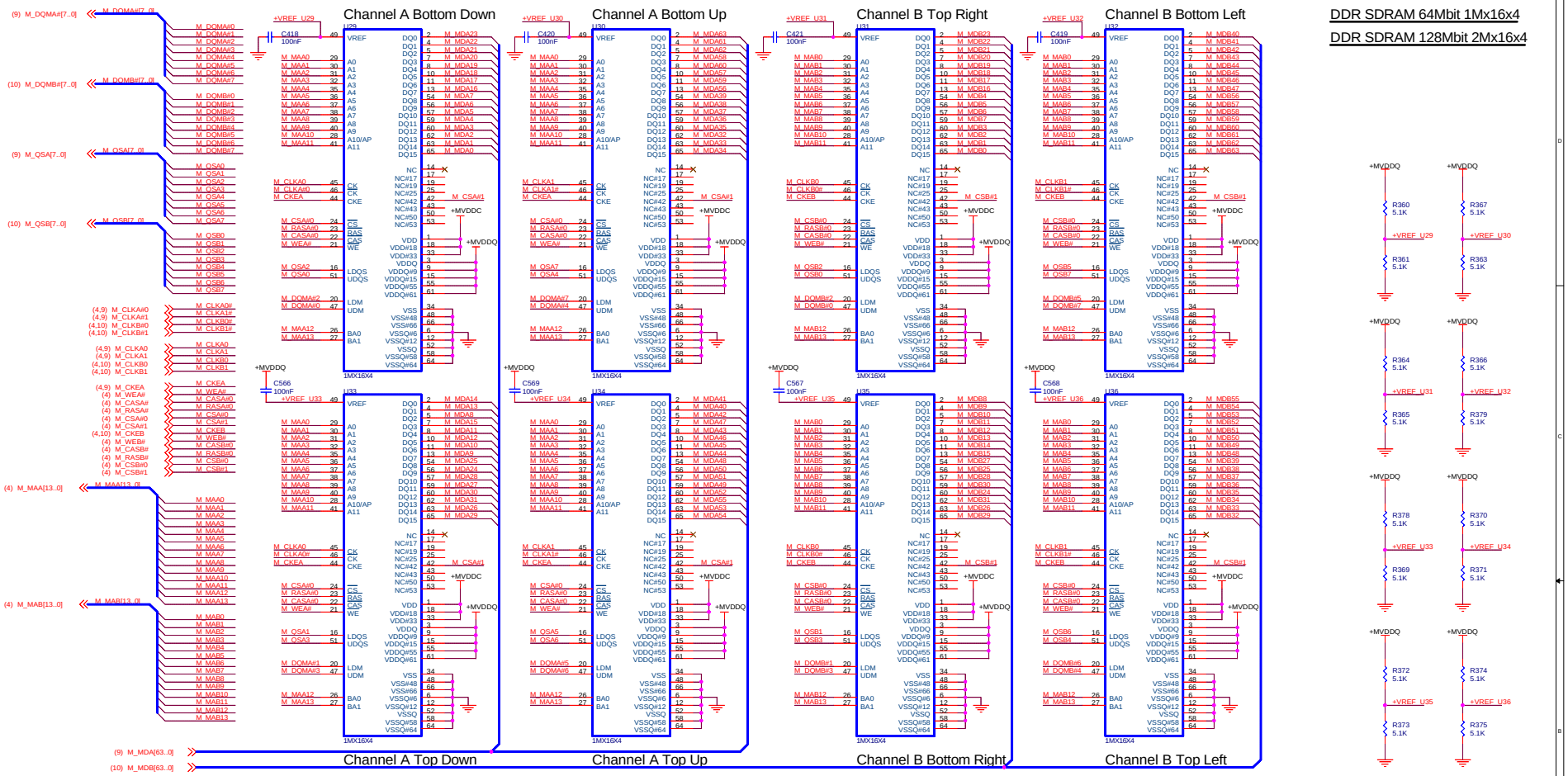
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



(4,11) M_CLKB0 — M_CLKB0 — CLKB0 (4,11)
(4,11) M_CLKB#0 — M_CLKB#0 — CLKB#0 (4,11)
(4,11) M_CLKB1 — M_CLKB1 — CLKB1 (4,11)
(4,11) M_CLKB#1 — M_CLKB#1 — CLKB#1 (4,11)

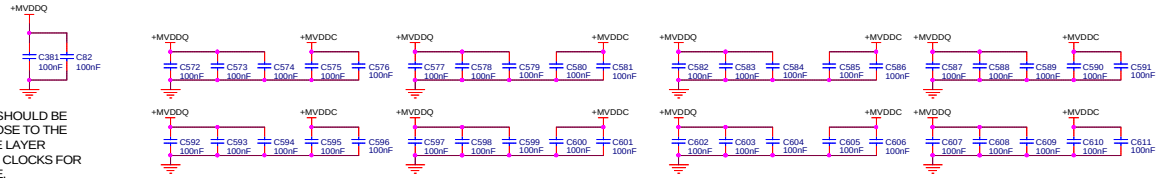
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO	
Size C	Document Number 105-A035XX-00	Rev 2
Date: Thursday, April 17, 2003	Sheet 10 of 16	



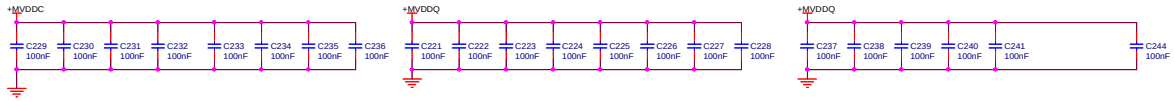
Note: These indications of the location of the memory for the solder side (bottom) are looking thru from the component side.

Put 1 100nF cap per power pin of memory



2 capacitors SHOULD BE PLACED CLOSE TO THE REFERENCE LAYER CHANGE OF CLOCKS FOR EMI REDUCE.

Place as many as possible.



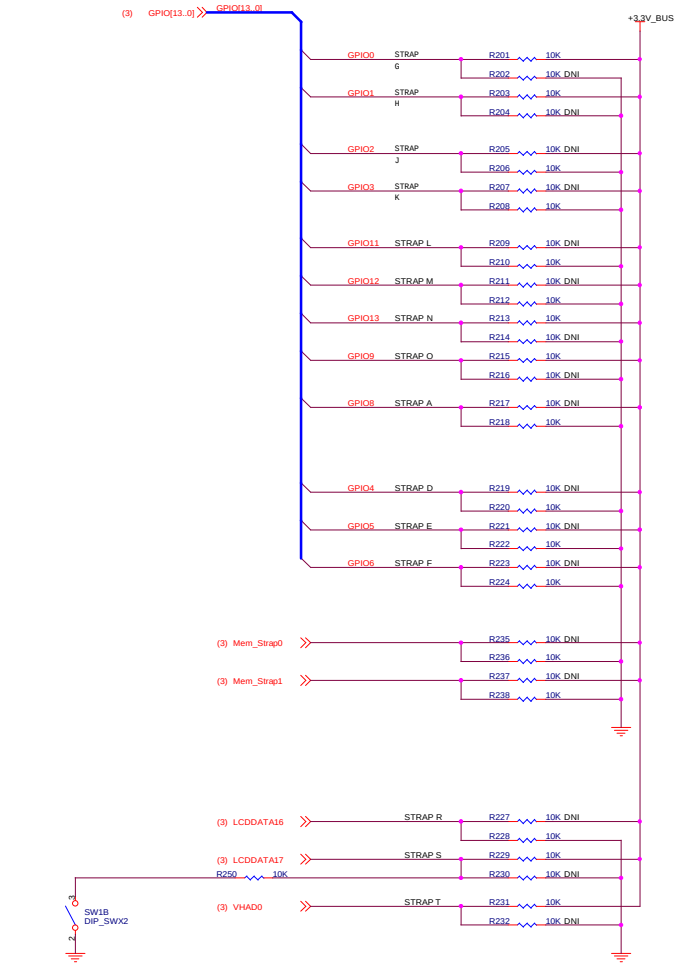
DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO	
Size: Custom	Document Number: 105-A035XX-00	Rev: 2
Date: Thursday, April 17, 2003	Sheet 11 of 16	

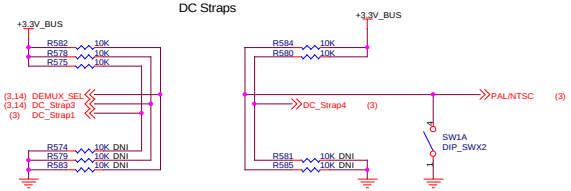
OPTION STRAPS



STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM **1011 - Serial M25P10 ROM (ST), chip IDis from ROM** 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1001
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000 (internal pull-down)
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select **00 - single function device.** 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	00
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

DC Straps

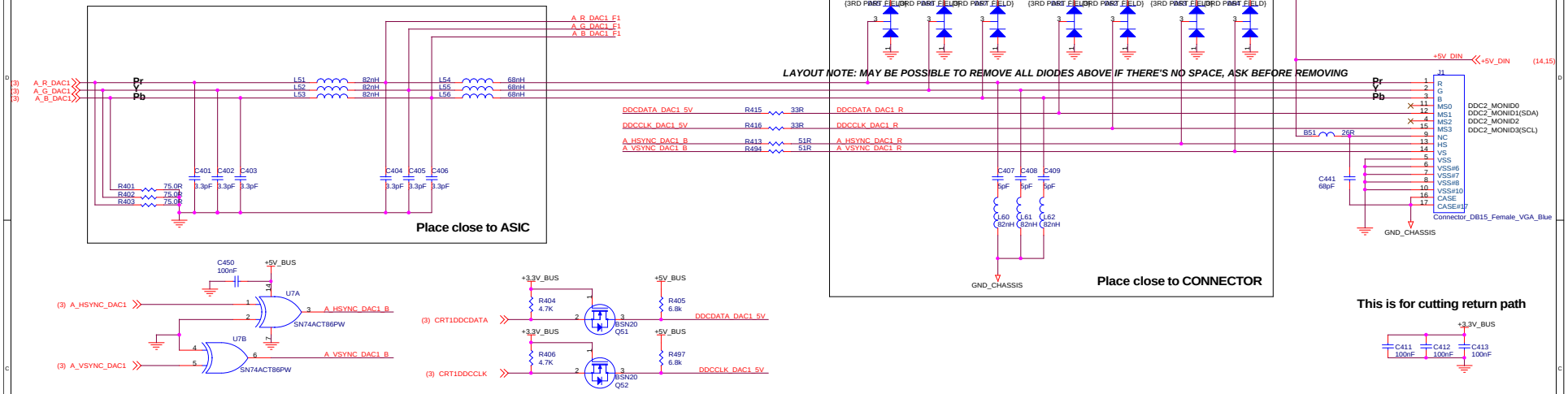


STRAPS	PIN	DESCRIPTION
DC_STRAP1	LCDDATA12	Internal TMDS Enabled **0 - Disabled** 1 - Enabled
DC_STRAP2	LCDDATA13	Video Capture Enabled **0 - Disabled** 1 - Enabled THIS STRAP IS NOT PRESENT ON THIS CARD!
DC_STRAP4 DC_STRAP5	LCDDATA15 LCDDATA19 0 0 0 1 1 0 1 1	DAC2 Configuration DAC2 Off DAC2 On as CRT DAC2 On as TVOUT DAC2 On as TVOUT and CRT
DC_STRAP6	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 -NTSC (on board resistor pull-up)
DC_STRAP3	LCDDATA14	Connected to Component TV-Out Detect pin Normally high, pulled low by Component TVO dongle

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

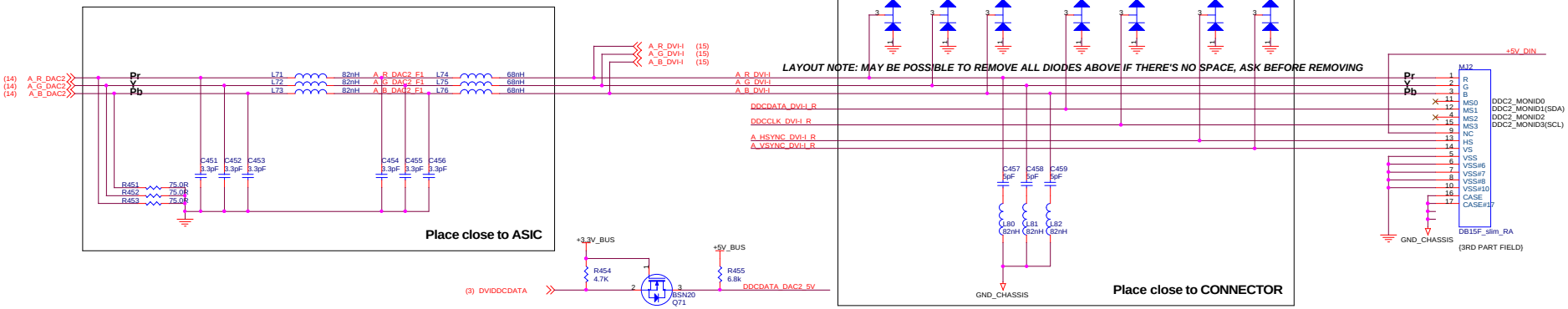
Title	AGP RV350 128M TSOP VGA DVI VO	
Size: Custom	Document Number: 105-A035XX-00	Rev: 2
Date: Thursday, April 17, 2003	Sheet 12 of 16	

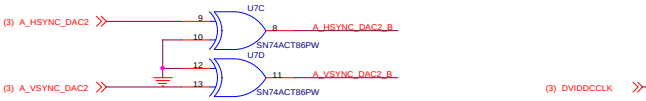
PRIMARY CRT

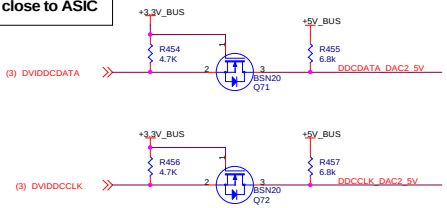


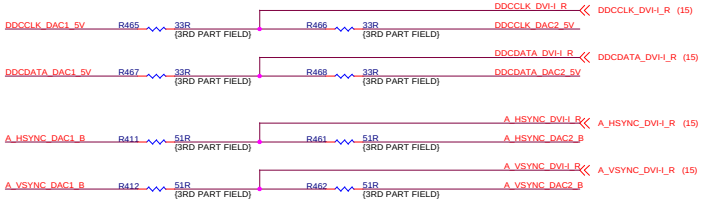
This is for cutting return path

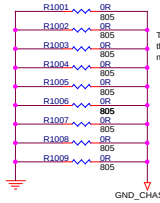
SECONDARY CRT



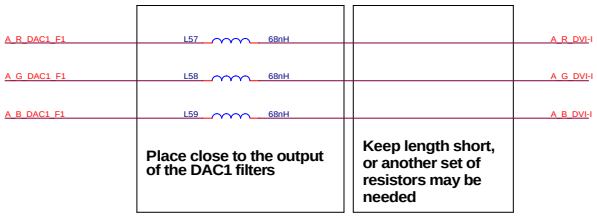






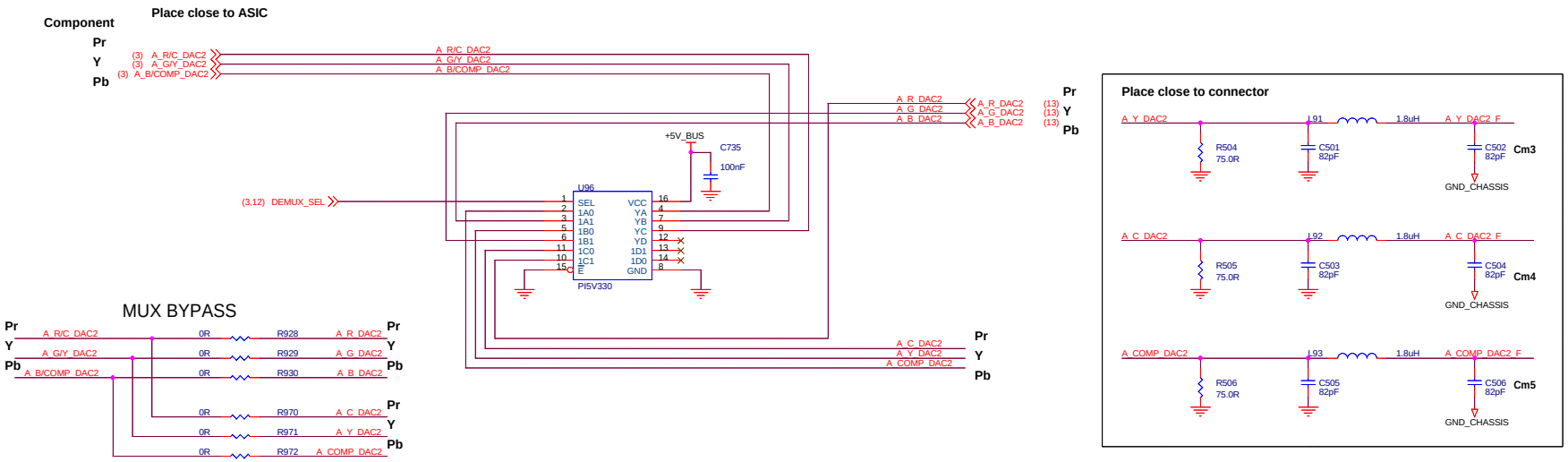


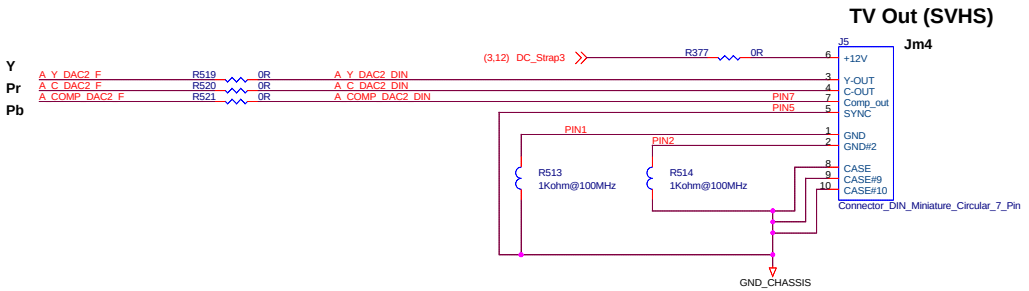
Three on top side, three at the bottom, spreaded high, middle and low vertically

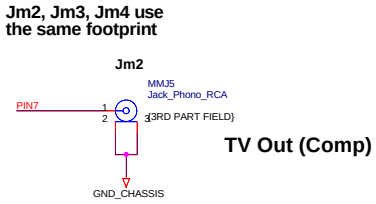


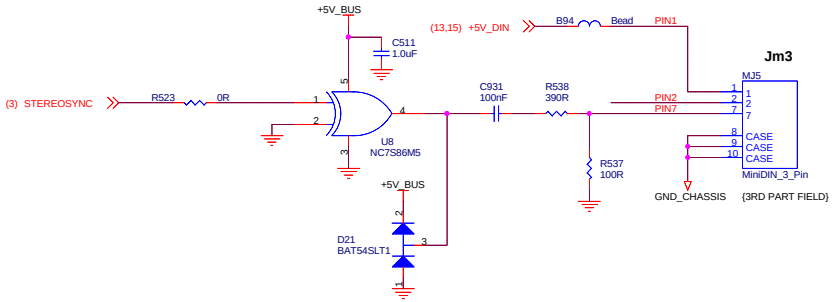
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO	
Size C	Document Number 105-A035XX-00	Rev 2
Date: Thursday, April 17, 2003	Sheet 13 of 16	


Component
Pr
Y
Pb
Place close to ASIC
(3) A_R/C_DAC2
(3) A_G/Y_DAC2
(3) A_B/COMP_DAC2
A_R/C_DAC2
A_G/Y_DAC2
A_B/COMP_DAC2
A_R_DAC2
A_G_DAC2
A_B_DAC2
(13) A_R_DAC2
(13) A_G_DAC2
(13) A_B_DAC2
Pr
Y
Pb
+5V_BUS
C735
100nF
U96
(3,12) DEMUX_SEL
SEL
1A0
1A1
1B0
1B1
1C0
1C1
E
VCC
YA
YB
YC
YD
1D1
1D0
GND
PI5V330
A_C_DAC2
A_Y_DAC2
A_COMP_DAC2
Pr
Y
Pb
MUX BYPASS
A_R/C_DAC2
A_G/Y_DAC2
A_B/COMP_DAC2
0R
R928
R929
R930
A_R_DAC2
A_G_DAC2
A_B_DAC2
R970
R971
R972
A_C_DAC2
A_Y_DAC2
A_COMP_DAC2
Place close to connector
A_Y_DAC2
L91
1.8uH
A_Y_DAC2_F
R504
75.0R
C501
82pF
C502
82pF
Cm3
GND_CHASSIS
A_C_DAC2
L92
A_C_DAC2_F
R505
75.0R
C503
C504
Cm4
A_COMP_DAC2
L93
A_COMP_DAC2_F
R506
75.0R
C505
C506
Cm5

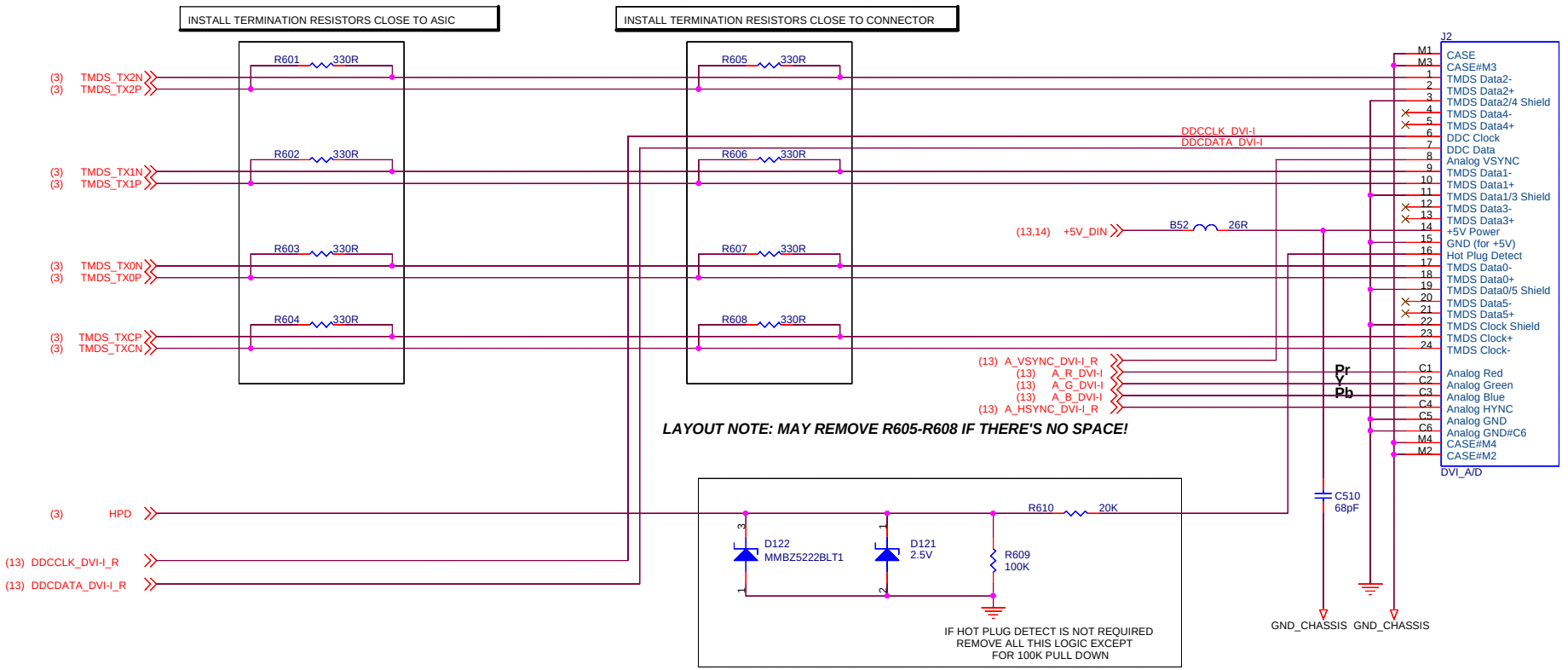

TV Out (SVHS)
Jm4
Y
Pr
Pb
A_Y_DAC2_F
A_C_DAC2_F
A_COMP_DAC2_F
R519
R520
R521
0R
A_Y_DAC2_DIN
A_C_DAC2_DIN
A_COMP_DAC2_DIN
(3,12) DC_Strap3
R377
0R
J5
+12V
Y-OUT
C-OUT
Comp_out
SYNC
GND
GND#2
CASE
CASE#9
CASE#10
PIN7
PIN5
PIN1
PIN2
R513
1Kohm@100MHz
R514
1Kohm@100MHz
Connector_DIN_Miniature_Circular_7_Pin
GND_CHASSIS


Jm2, Jm3, Jm4 use
the same footprint
Jm2
MMJ5
Jack_Phono_RCA
PIN7
{3RD PART FIELD}
GND_CHASSIS
TV Out (Comp)


+5V_BUS
C511
1.0uF
(13,15) +5V_DIN
B94
Bead
PIN1
Jm3
MJ5
(3) STEREOSYNC
R523
0R
C931
100nF
R538
390R
PIN2
PIN7
CASE
CASE
CASE
MiniDIN_3_Pin
U8
NC7S86M5
R537
100R
GND_CHASSIS
{3RD PART FIELD}
+5V_BUS
D21
BAT54SLT1


ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600
Title
AGP RV350 128M TSOP VGA DVI VO
Size
Custom
Document Number
105-A035XX-00
Rev
2
Date:
Thursday, April 17, 2003
Sheet
14
of
16

PRIMARY DVI-I CONNECTOR



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO	
Size B	Document Number 105-A035XX-00	Rev 2
Date: Thursday, April 17, 2003	Sheet 15 of 16	

CRT SCREWS

ASSY1
SCREW
JACKSCREW
{3rd part field}

ASSY2
SCREW
JACKSCREW
{3rd part field}

DVI SCREWS

ASSY3
SCREW
JACKSCREW
{3rd part field}

ASSY4
SCREW
JACKSCREW
{3rd part field}

MISC. BOARD PARTS

ASSY7
ANTISTATIC BAG
6_X_11
{3rd part field}

ASSY8
BLANK LABEL
1.50W_X_0.50H
ASSY

REF1
SCHEMATIC
105-A03500-00B
{3rd part field}

REF2
PCB
109-A03500-00B
{3rd part field}

REF5
ATI LOGO LABEL
ATI_LOGO_LABEL

ASSY11
BRACKET

WRONG SYMBOL, MUST BE UPDATED LATER

MH101
HEATSINK

PASSIVE HEATSINK

H103
HEATSINK
Hc

Heatsink cross-hatched finned 45X45X10mm black amodize w/o adhesive

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP RV350 128M TSOP VGA DVI VO	
Size B	Document Number 105-A035XX-00	Rev 2
Date: Thursday, April 17, 2003	Sheet 16 of 16	

{Variant Name}

Title	Schematic No.	Date:
AGP RV350 128M TSOP VGA DVI VO	105-A035XX-00	**Thursday, April 17, 2003**

REVISION HISTORY

Rev 2

Sch Rev	Date	REVISION DESCRIPTION
0	2002/11/27	PRELIMINARY BASED ON A034
1	2003/02/20	Add AND gate footprint for AGP_MB_8X_Det#, delete C3 Change C62 and C68 to 2.2uF (no footprint change) GND_AVSS, GND_A2VSSN and GND_A2VSSQ grounded at 100nF decapling cap (layout change only) Swap memory address 12 and 13 (both channels) Change ceramic caps at the output of the regulator U810 to 10uF tant. Move C55 close to ASIC (Layout change) Add stiching caps between +MVDDC_Source and +5V_BUS (C1 and C17) Add 3 more 0R for Chassis and Digital GND
2	2003/03/17 2003/03/31 2003/04/08 2003/04/09	(pg5) Update MAXIM compensation values (no footprint change) (pg5) Update IRF7413A (no footprint change) (pg5) Add 10uF C50 on TPVDD (pg8) Replace R286 and R284 with 805 footprint (pg2) Change crystal loading cap from 22pF to 15pF