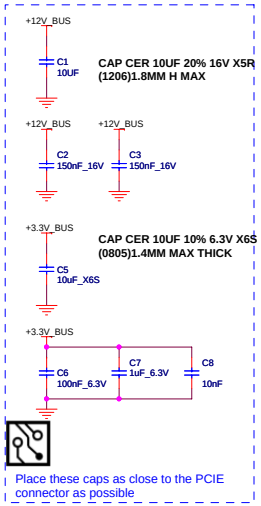
PCI-EXPRESS EDGE CONNECTOR



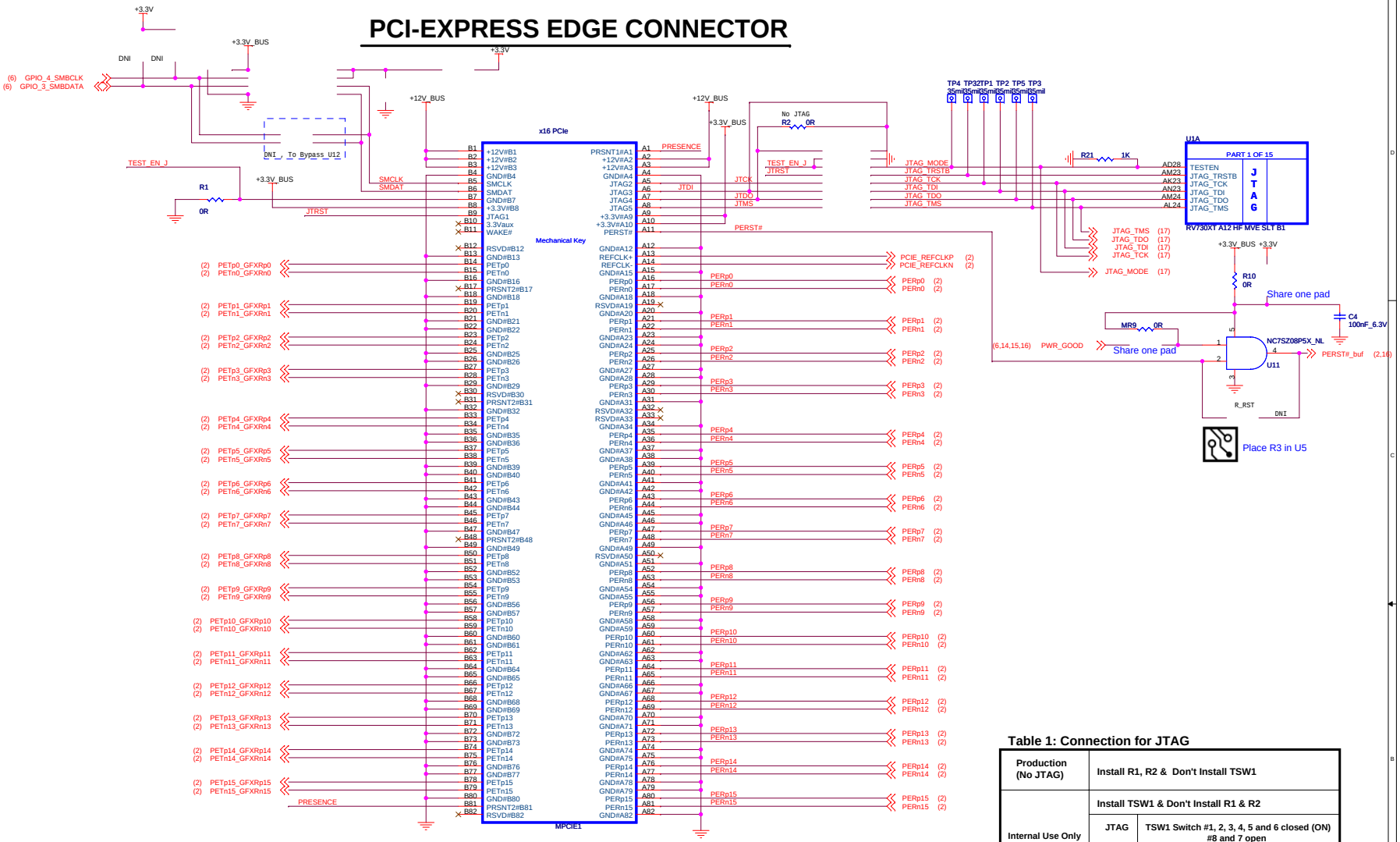


Table 1: Connection for JTAG

Production (No JTAG)	**Install R1, R2 & Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R1 & R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)**

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

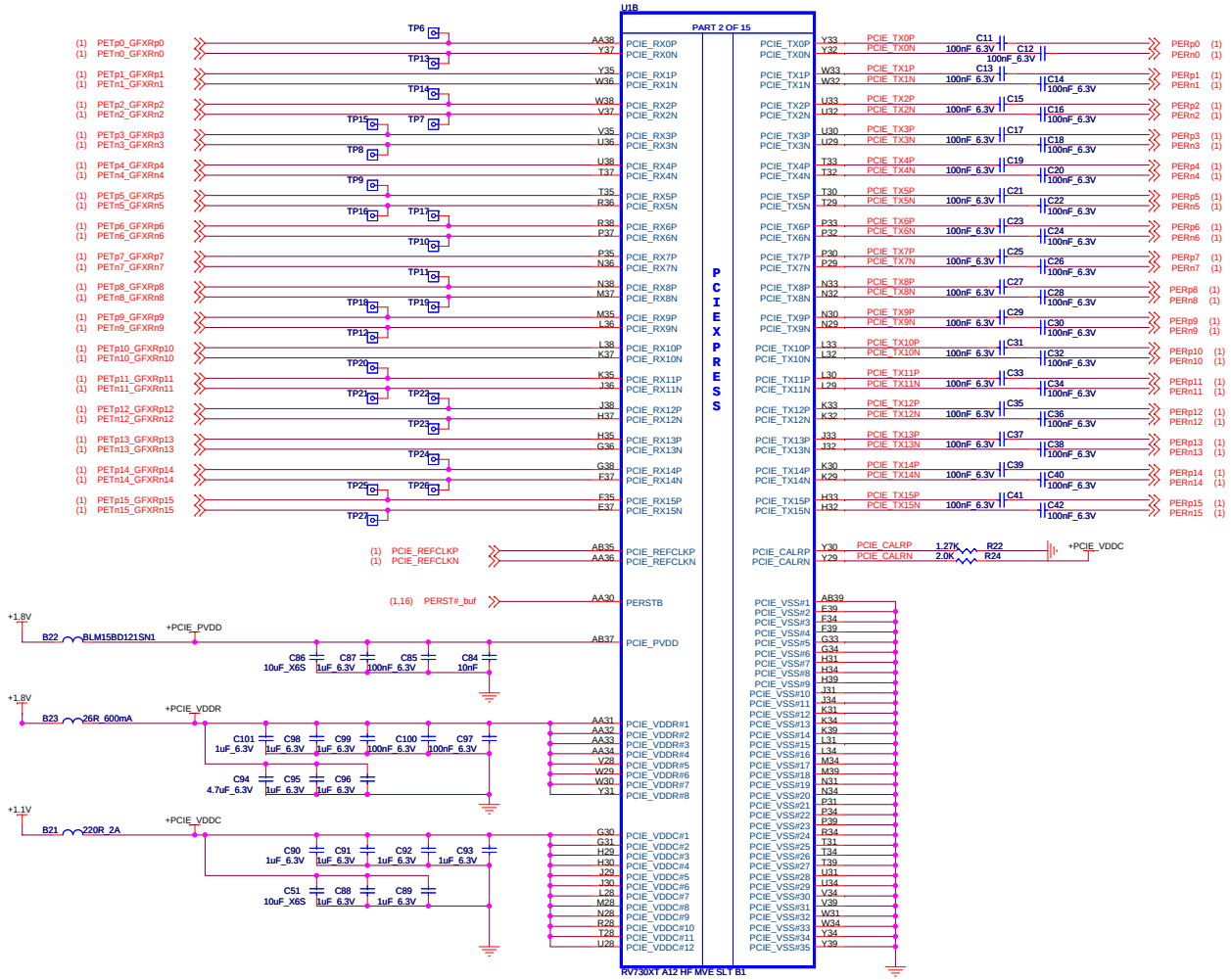
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Wednesday, August 20, 2008
Rev	50
Sheet	1 of 19
Title	RH RV730 GDDR3 DP-DP- DVII
Doc No.	102-B66601-00

(2) RV730 PCIE Interface

NOTE: some of the PCIE testpoints will
be available trought via on traces.



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Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

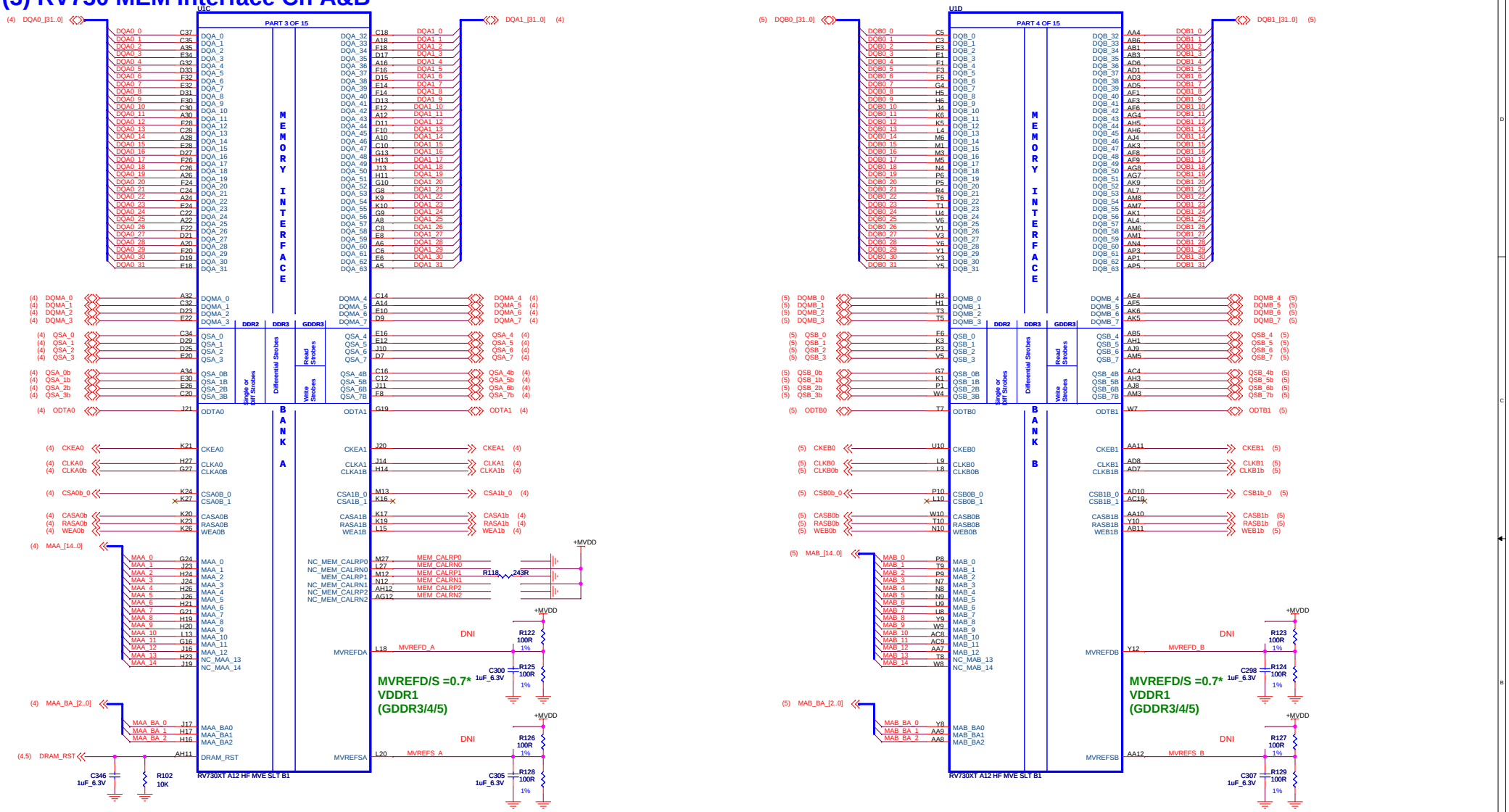
Date: Wednesday, August 20, 2008 Rev 50

Sheet 2 of 19

Title RH RV730 GDDR3 DP-DP- DVII

Doc No. 102-B66601-00

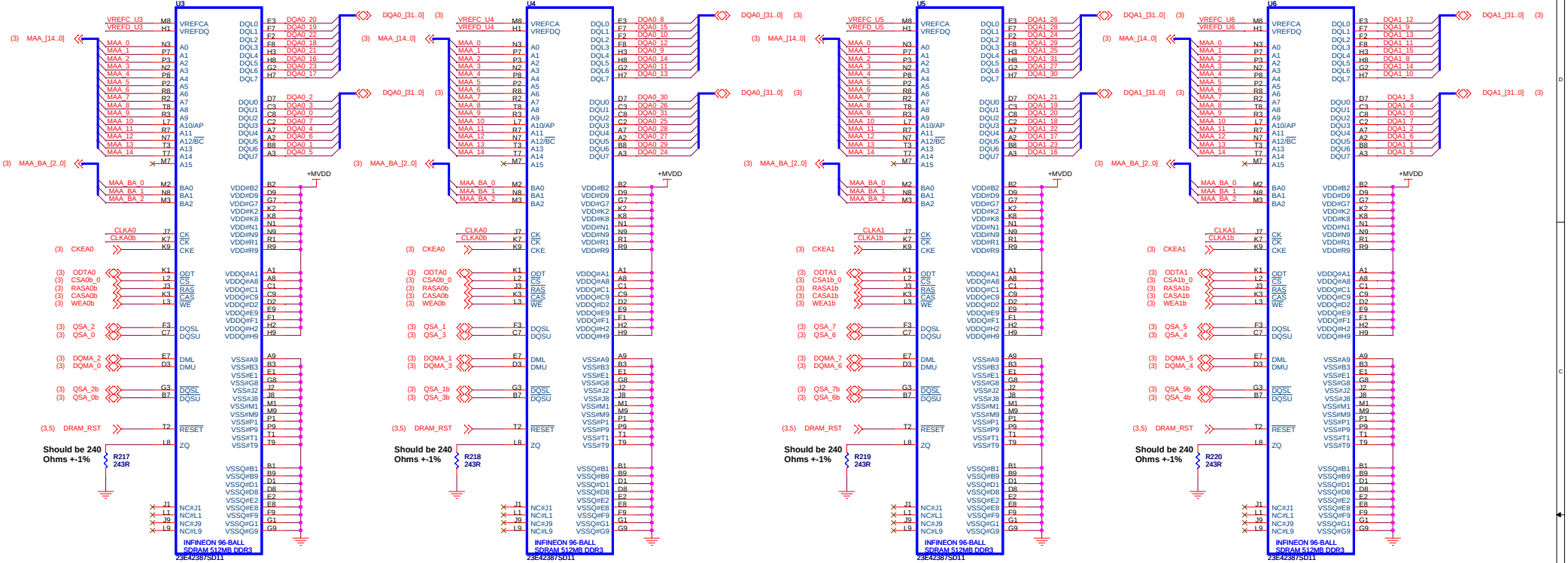
(3) RV730 MEM Interface Ch A&B

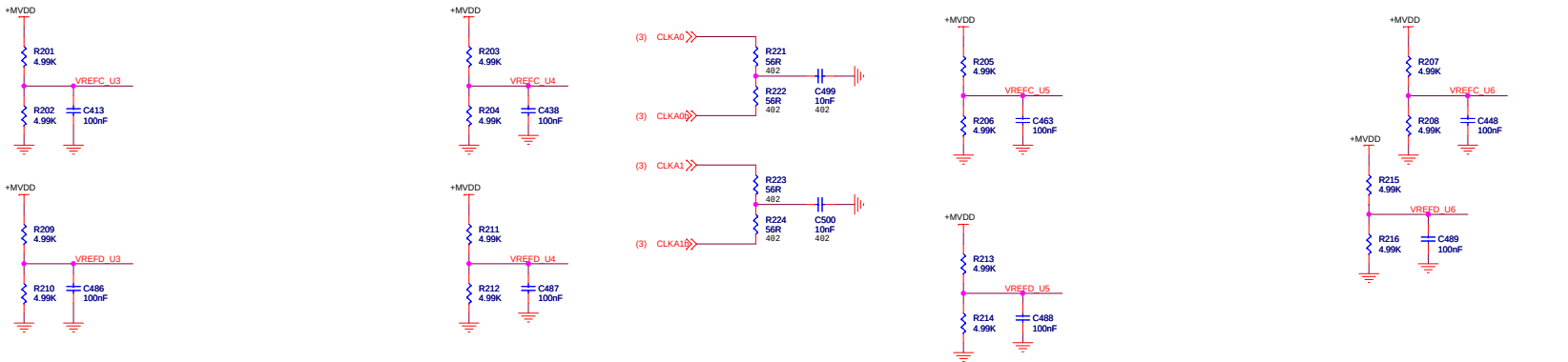


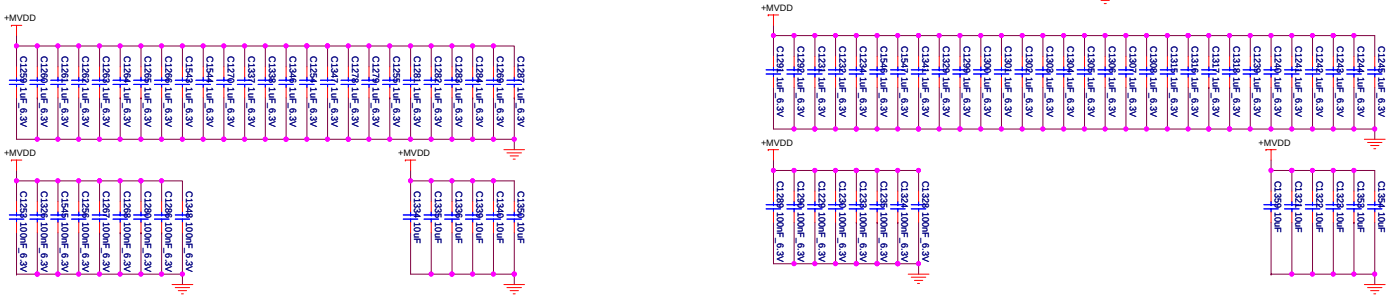
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Wednesday, August 20, 2008
Rev	50
Sheet	3 of 19
Title	RH RV730 GDDR3 DP-DP- DVII
Doc No.	102-B66601-00

(4) DDR3 Memory Channel A



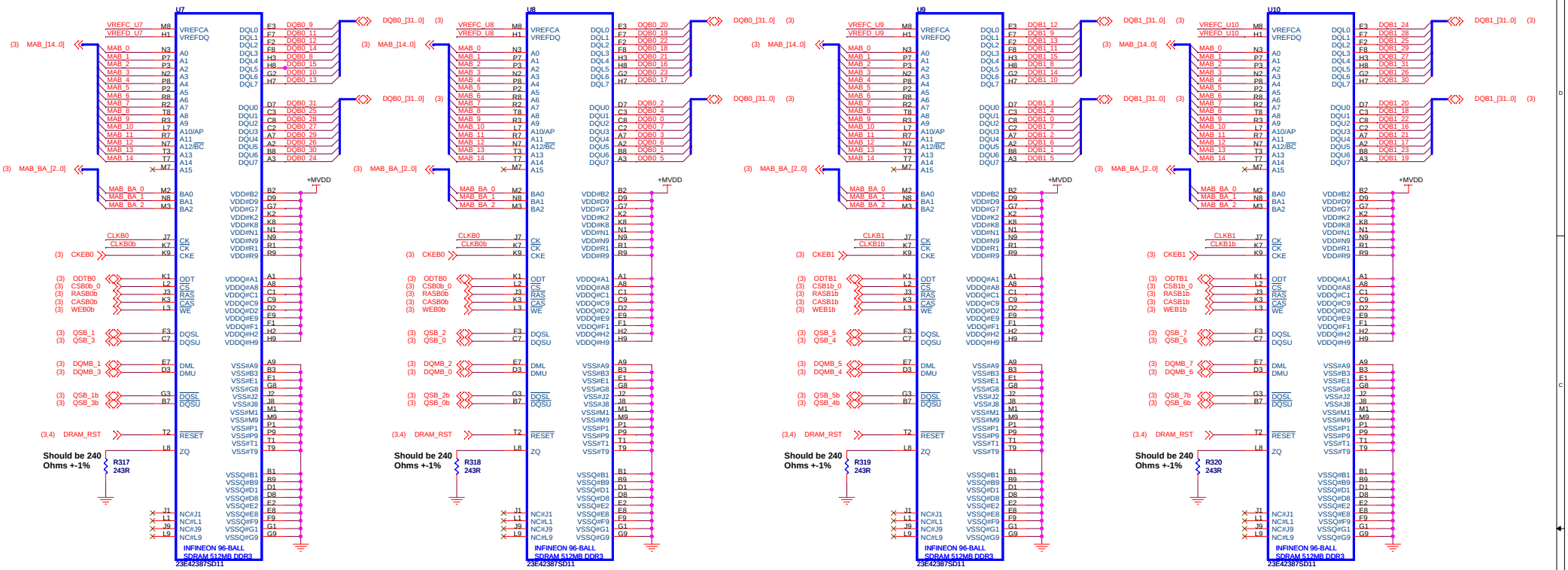


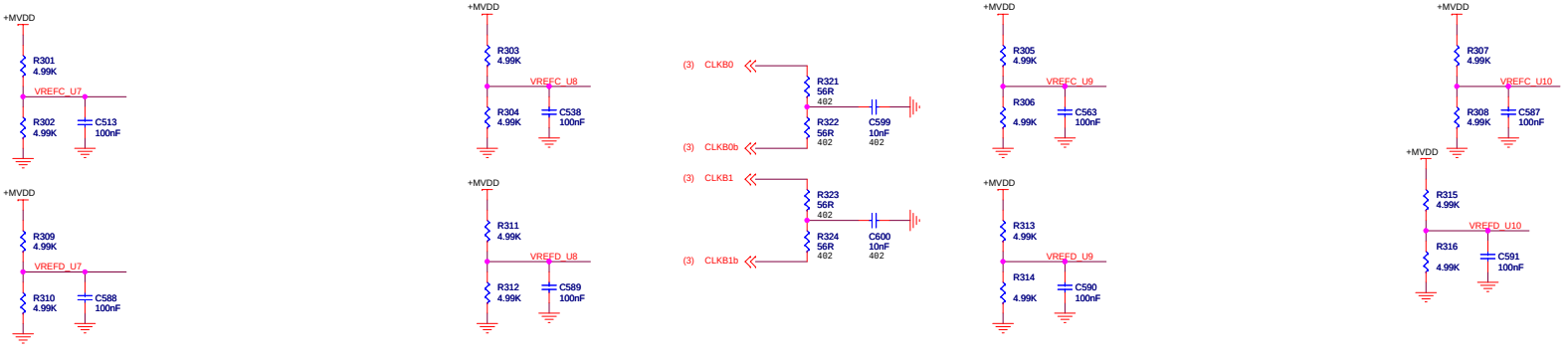


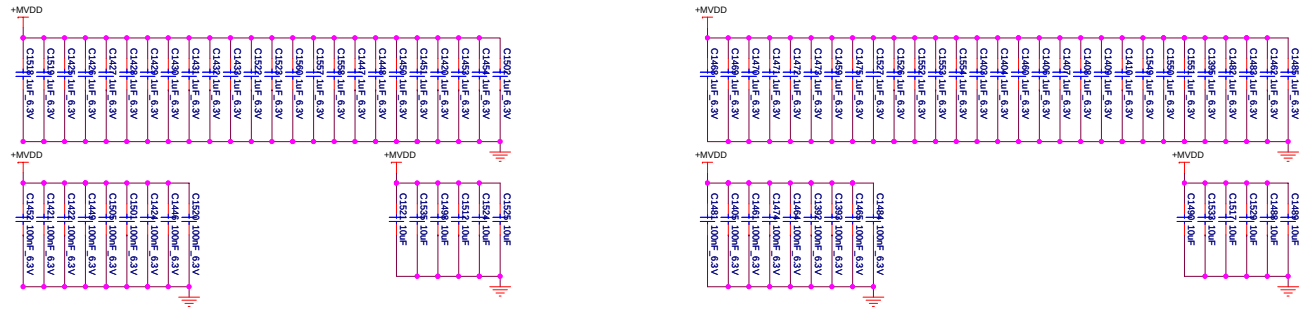
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Wednesday, August 20, 2008
Rev	50
Sheet	4 of 19
Title	RH RV730 GDDR3 DP-DP- DVII
Doc No.	102-B66601-00

(5) DDR3 Memory Channel B



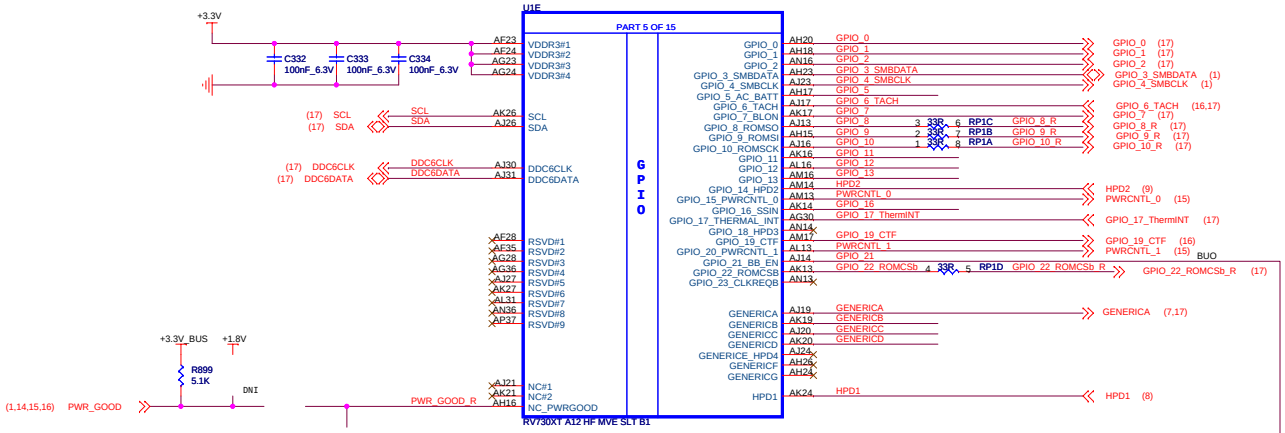


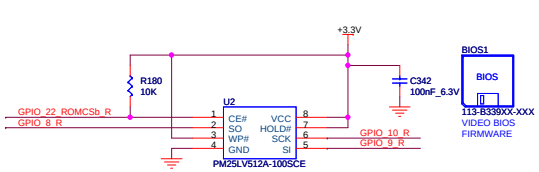


Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Wednesday, August 20, 2008
Rev	50
Sheet	5 of 19
Title	RH RV730 GDDR3 DP-DP- DVII
Doc No.	102-B66601-00

(06) RV730 GPIOs Strap CF XTAL

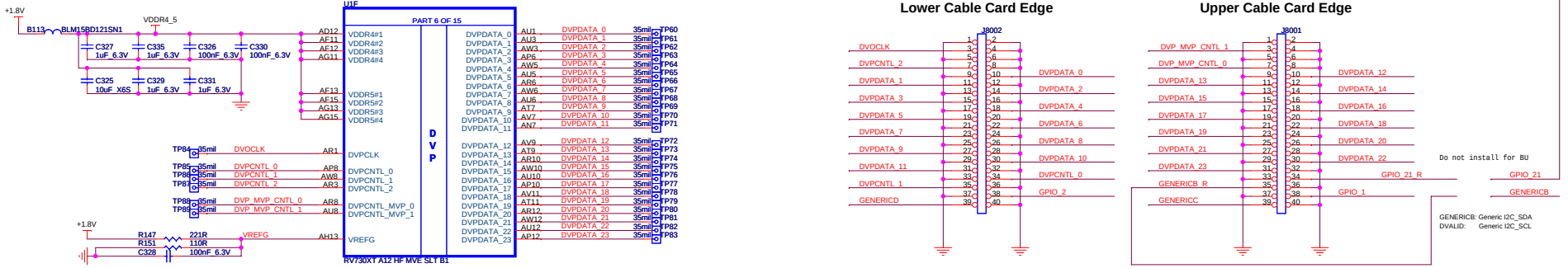




PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

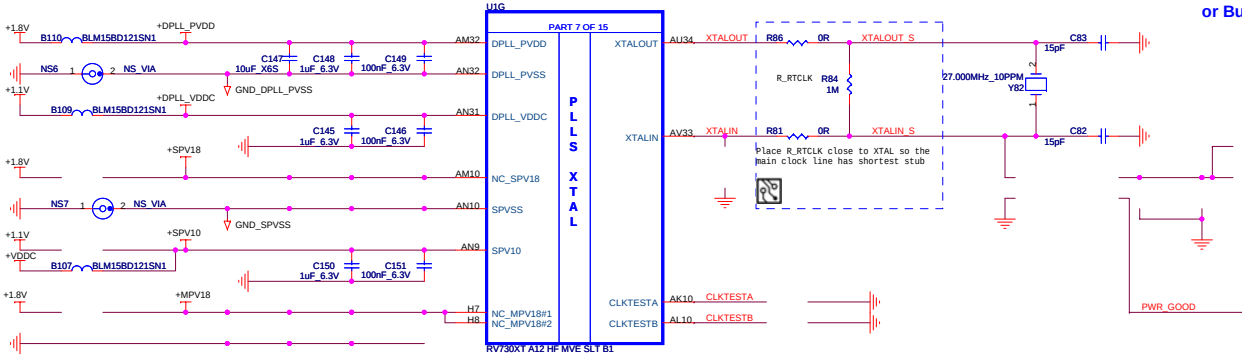
PIN BASED STRAPS

CrossFire Card-Edge



or Bundle B

or Bundle A (closer to the bracket)



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Wednesday, August 20, 2008
Rev	50
Sheet	6 of 19
Title	RH RV730 GDDR3 DP-DP- DVII
Doc No.	102-B66601-00

(07) RV730 DAC1 and DAC2/TV

See BOM for qualified filters
Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

U1H
PART 8 OF 15
DAC1
RV730XT A12 HF MVE SLT B1

U1I
PART 9 OF 15
DAC2/TV
RV730XT A12 HF MVE SLT B1

See BOM for qualified filters
Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI

Install for Dell
Install for Dell
Install for Dell only when it's needed for EMI
DNI for Dell
DNI for Dell

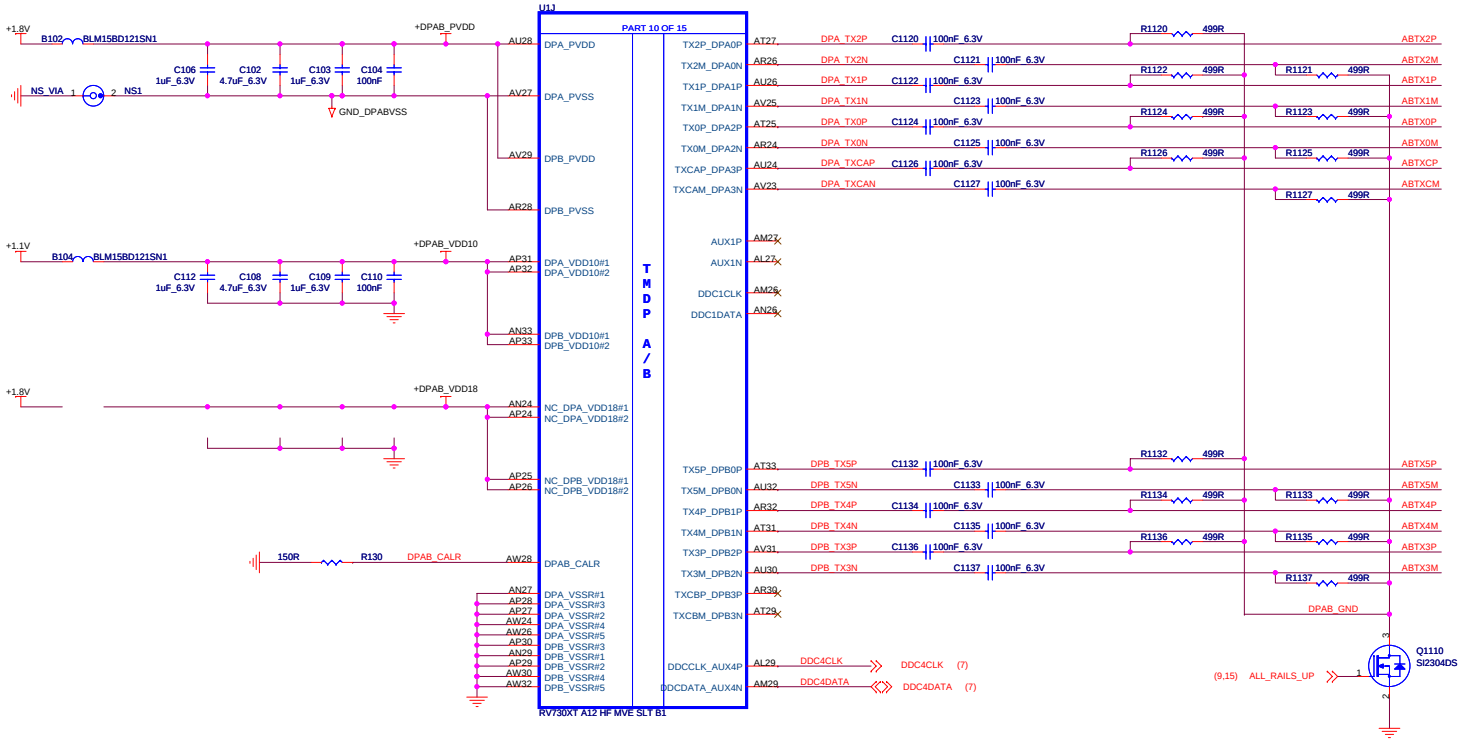
TV Out
J3001
Rpin5
Conn_DIN_Mini_Circular_7_Pin_with_O_Ring

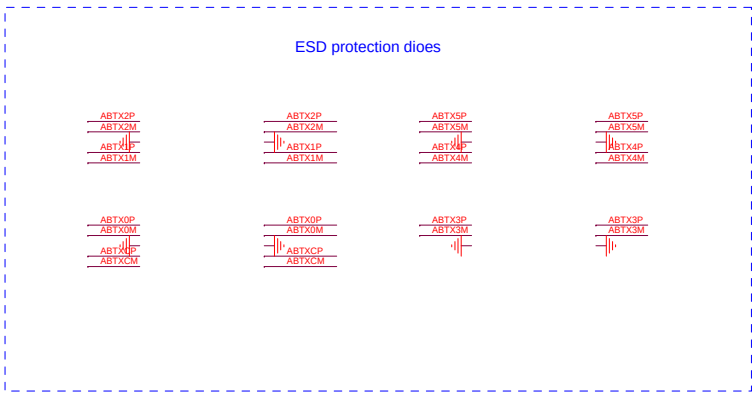
The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

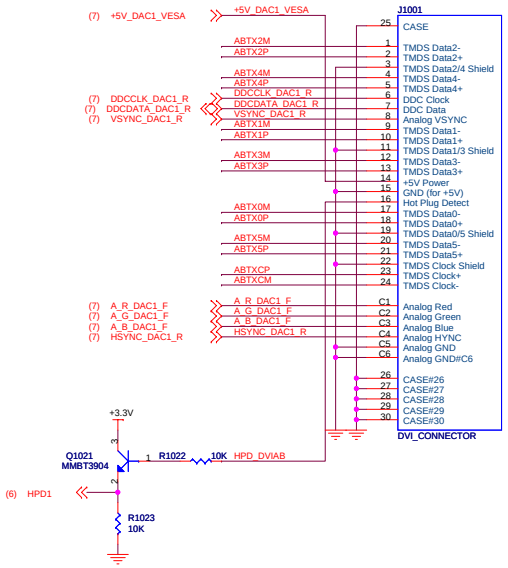
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Wednesday, August 20, 2008
Rev 50
Sheet 7 of 19
Title: RH RV730 GDDR3 DP-DP- DVII
Doc No. 102-B66601-00

(08) RV730 TMDS A&B







Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

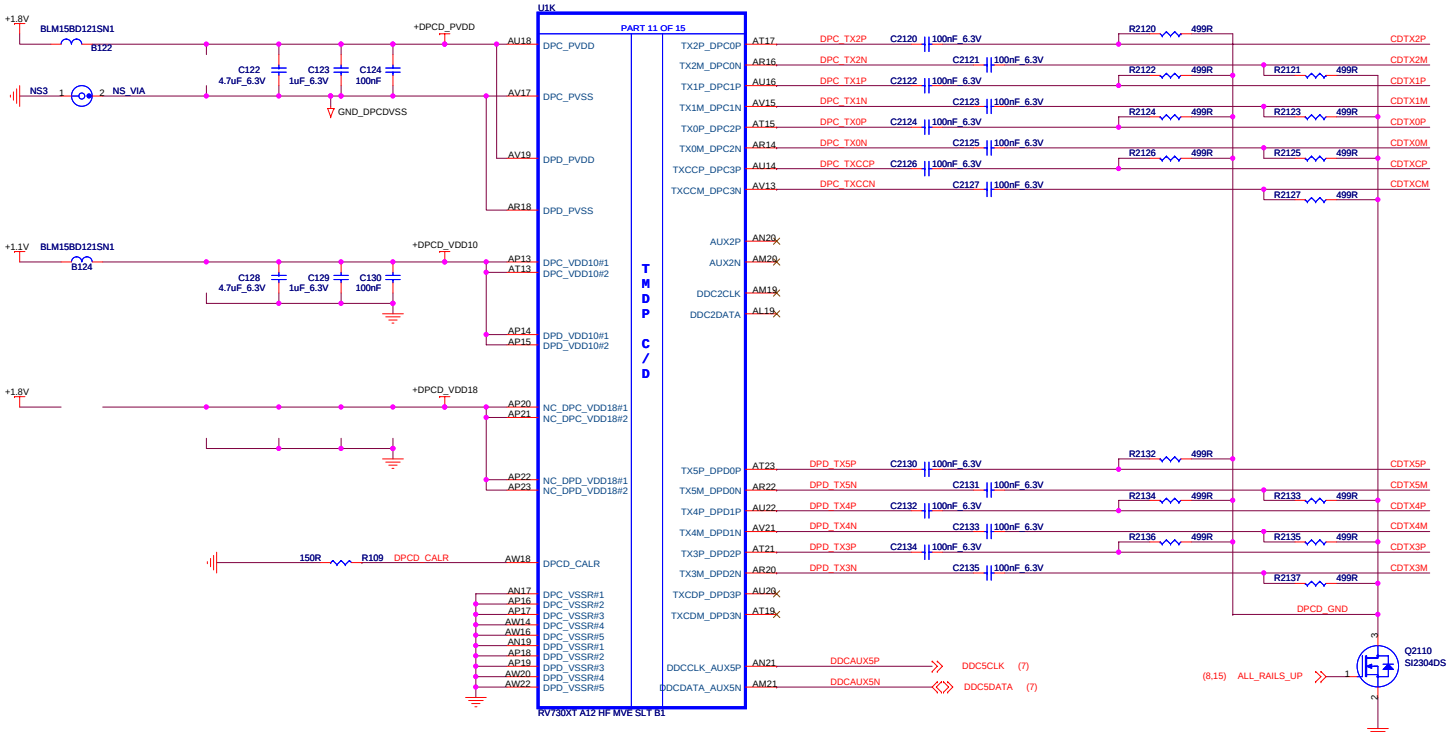
Date: Wednesday, August 20, 2008 Rev 50

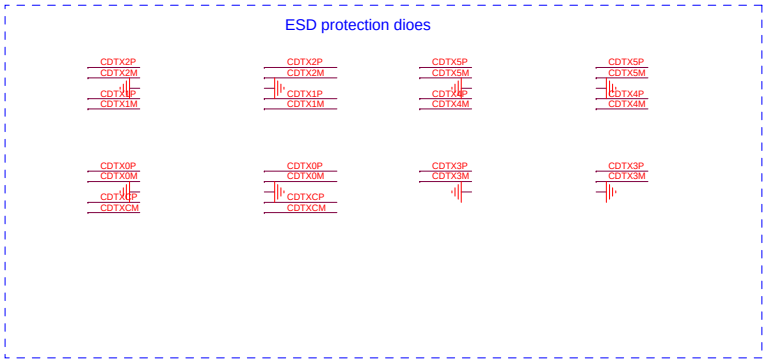
Sheet 8 of 19

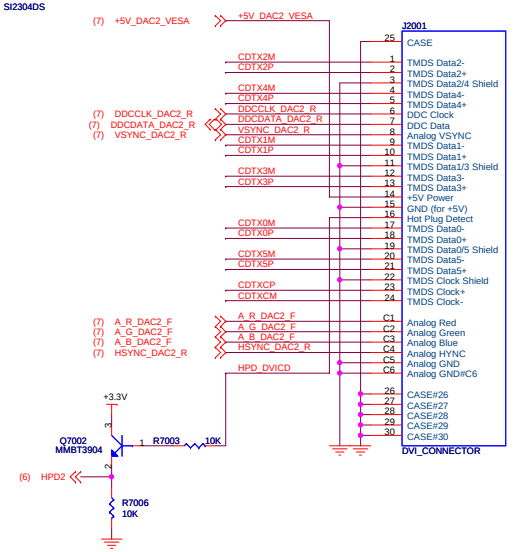
Title: RH RV730 GDDR3 DP-DP- DVII

Doc No. 102-B66601-00

(09) RV730 Display Port C&D



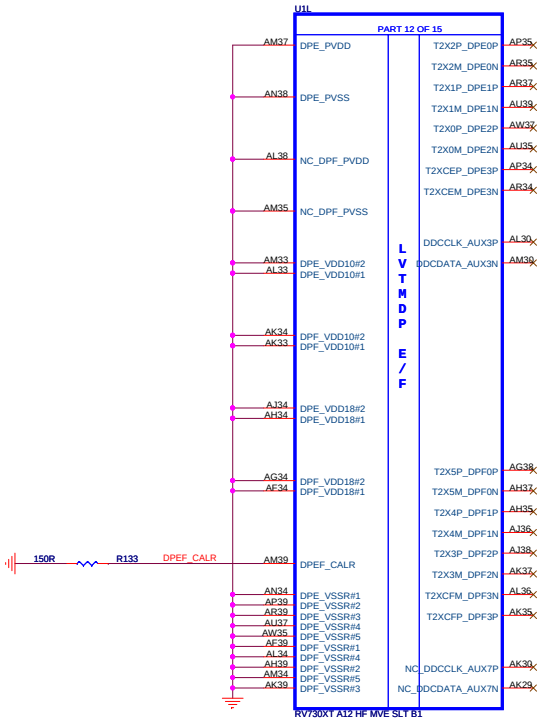




Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Wednesday, August 20, 2008
Rev	50
Sheet	9 of 19
Title	RH RV730 GDDR3 DP-DP- DVII
Doc No.	102-B66601-00

(10) No Connect E&F



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

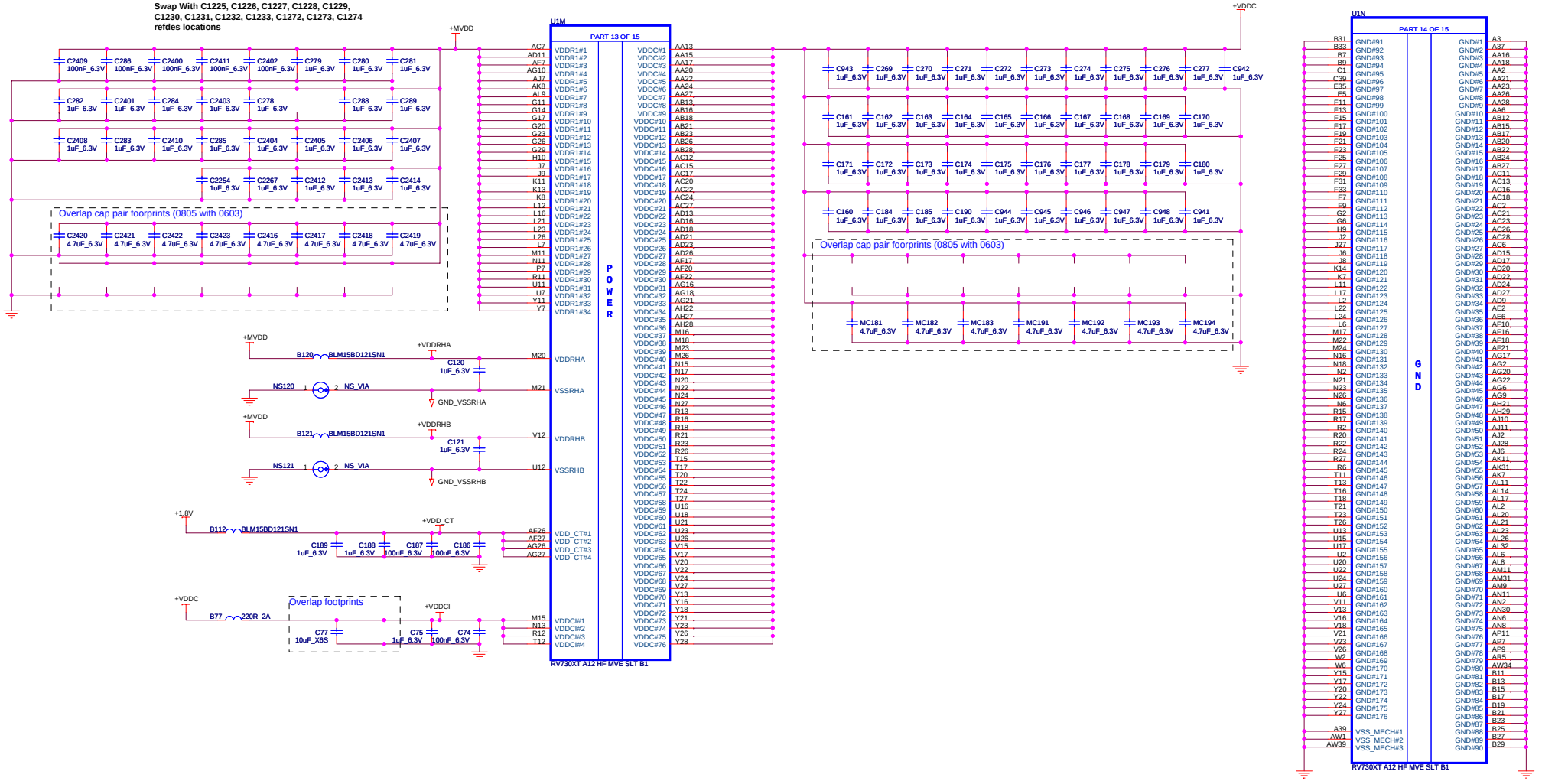
Date: Wednesday, August 20, 2008 Rev 50

Sheet 10 of 19

Title RH RV730 GDDR3 DP-DP- DVII

Doc No. 102-B66601-00

(11) RV730 Power & GND



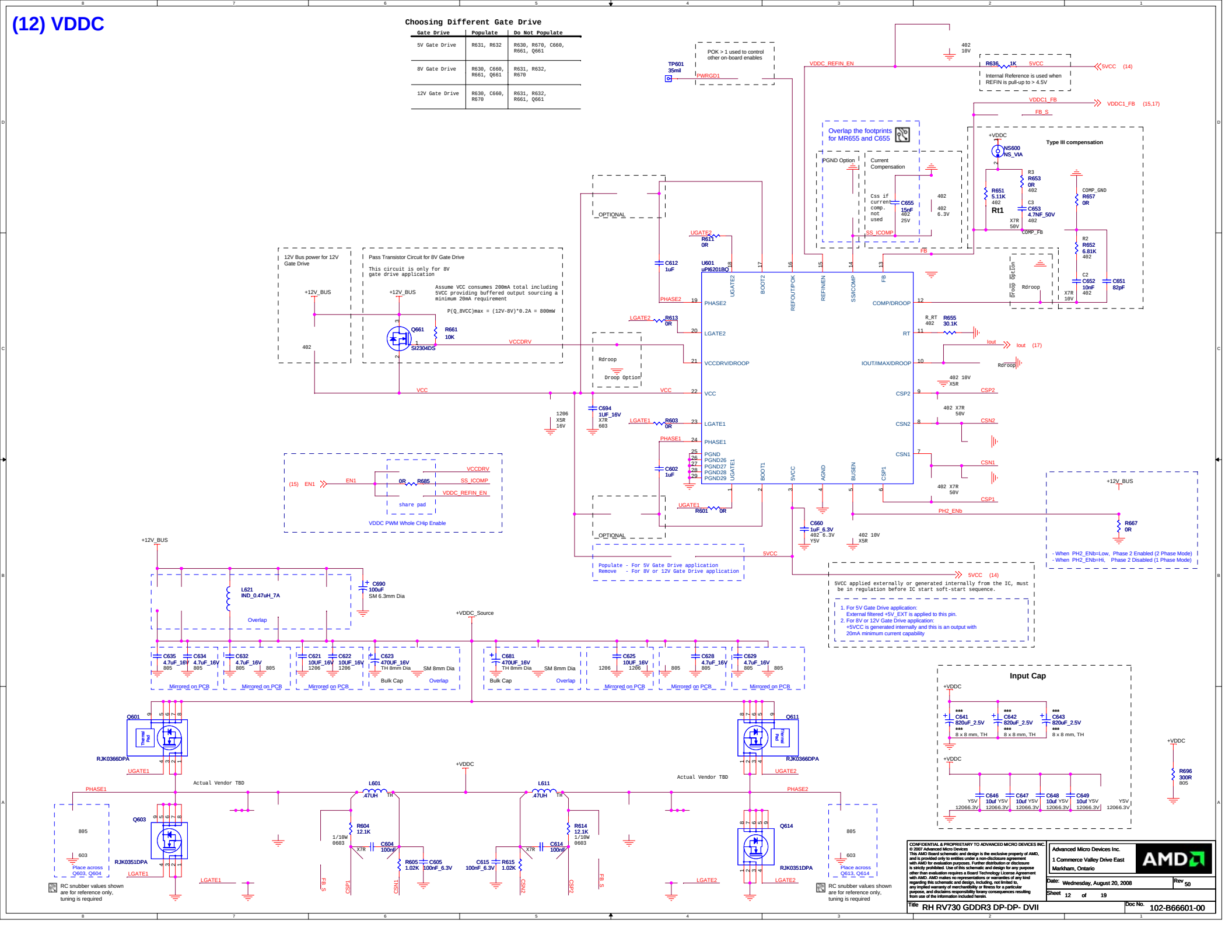
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Wednesday, August 20, 2008
Rev	50
Sheet	11 of 19
Title	RH RV730 GDDR3 DP-DP- DVII
Doc No.	102-B66601-00

(12) VDDC

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661



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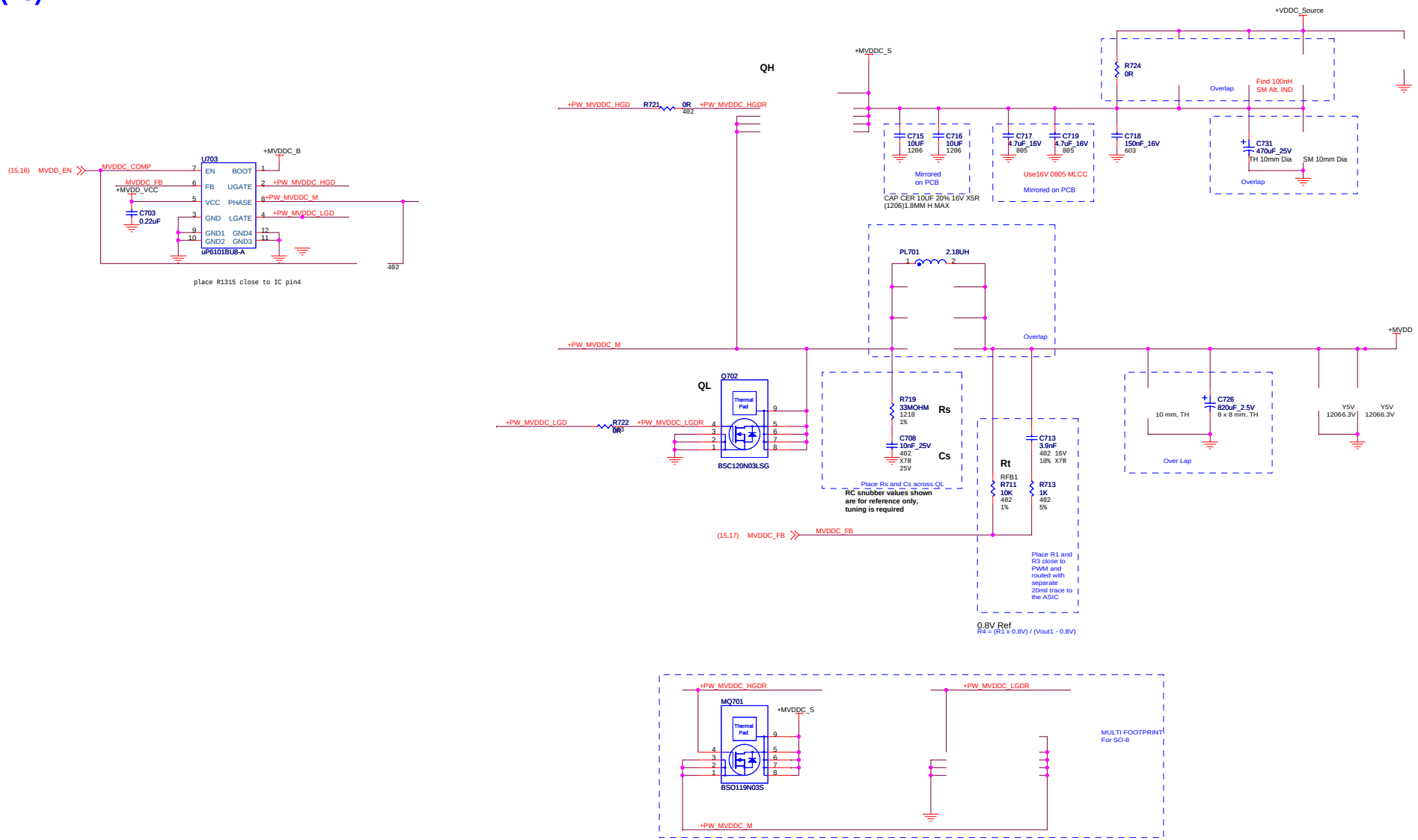
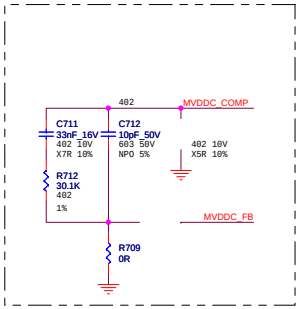
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Wednesday, August 20, 2008 Rev 50
Sheet 12 of 19
Title RH RV730 GDDR3 DP-DP- DVII
Doc No. 102-B66601-00

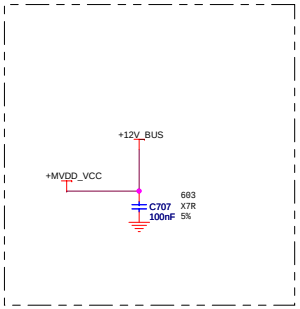
(13) MVDD



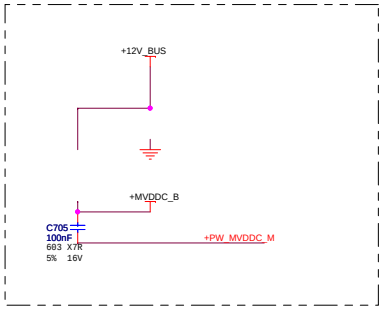
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



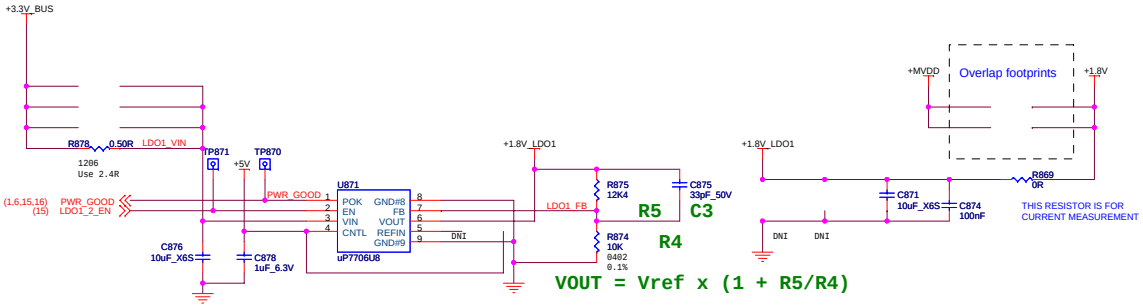
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Wednesday, August 20, 2008
Rev	50
Sheet	13 of 19
Title	RH RV730 GDDR3 DP-DP- DVII
Doc No.	102-B66601-00

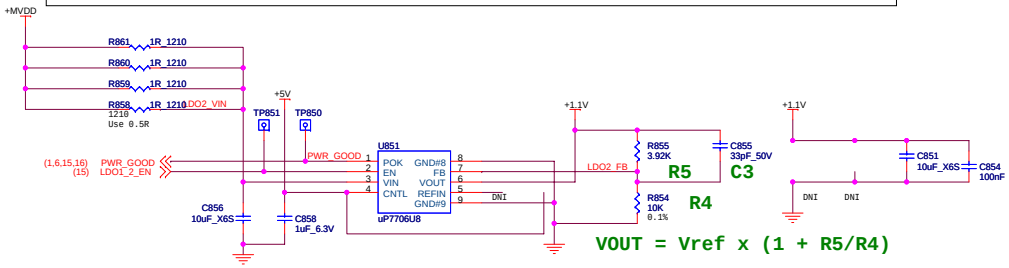
(14) Linear Regulators

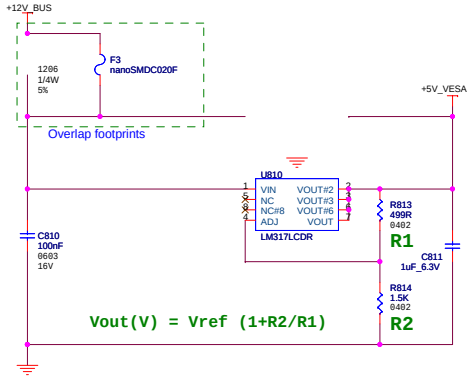
Regulators for +5V, +5V_VESA and +5V_VESA2

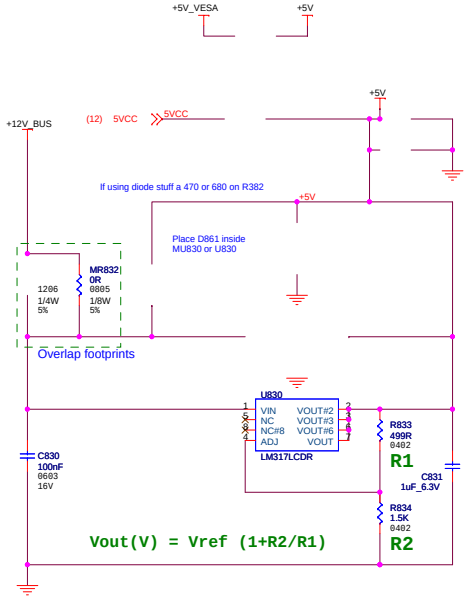
LDO #1: Vin = 3.0V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 1.0A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #2: Vin = +1.5V to 2.0VMAX Vout = +1.1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling





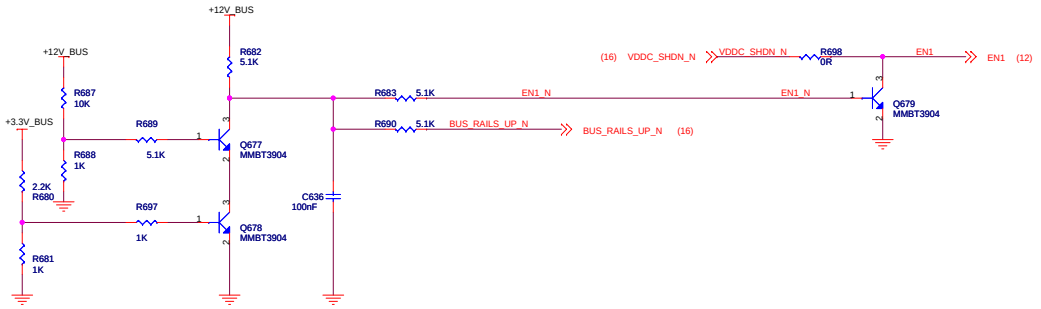


Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

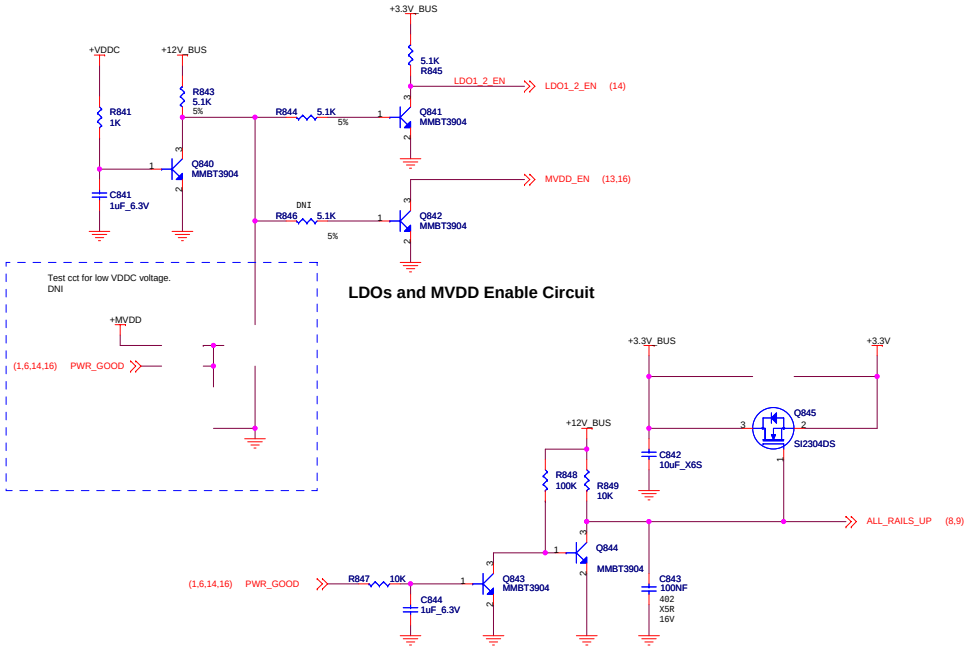
Date: Wednesday, August 20, 2008	Rev 50
Sheet 14 of 19	
Title RH RV730 GDDR3 DP-DP- DVII	Doc No. 102-B66601-00

(15) Power Management

Power up Sequencing



VDDC Enable Circuit



LDOs and MVDD Enable Circuit

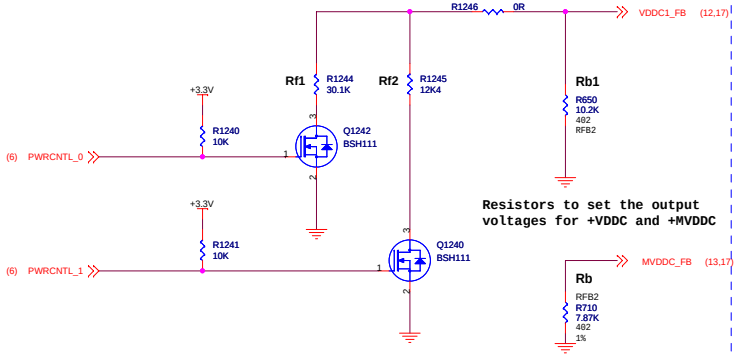
3.3V Enable Circuit

Power Play

VDDC Voltage Settings Using GPIOs (for VDDC1 Dual Phase)

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1=42.2K Rf2=20.5K	Rf1= Rf2=	Rf1= Rf2=	
0	0	0.90V			
0	1	1.00V			
1	0	1.15V			
1	1	1.25V			Power-up Default

Vout = Vref * (1+Rt/Rb)
VDDC1 (Dual Phase): Vref = 0.6V, Rt = 5.11K
VDDC2 (Single Phase): Vref = 0.8V, Rt = 10K
MVDDC (Single Phase): Vref = 0.8V, Rt = 10K

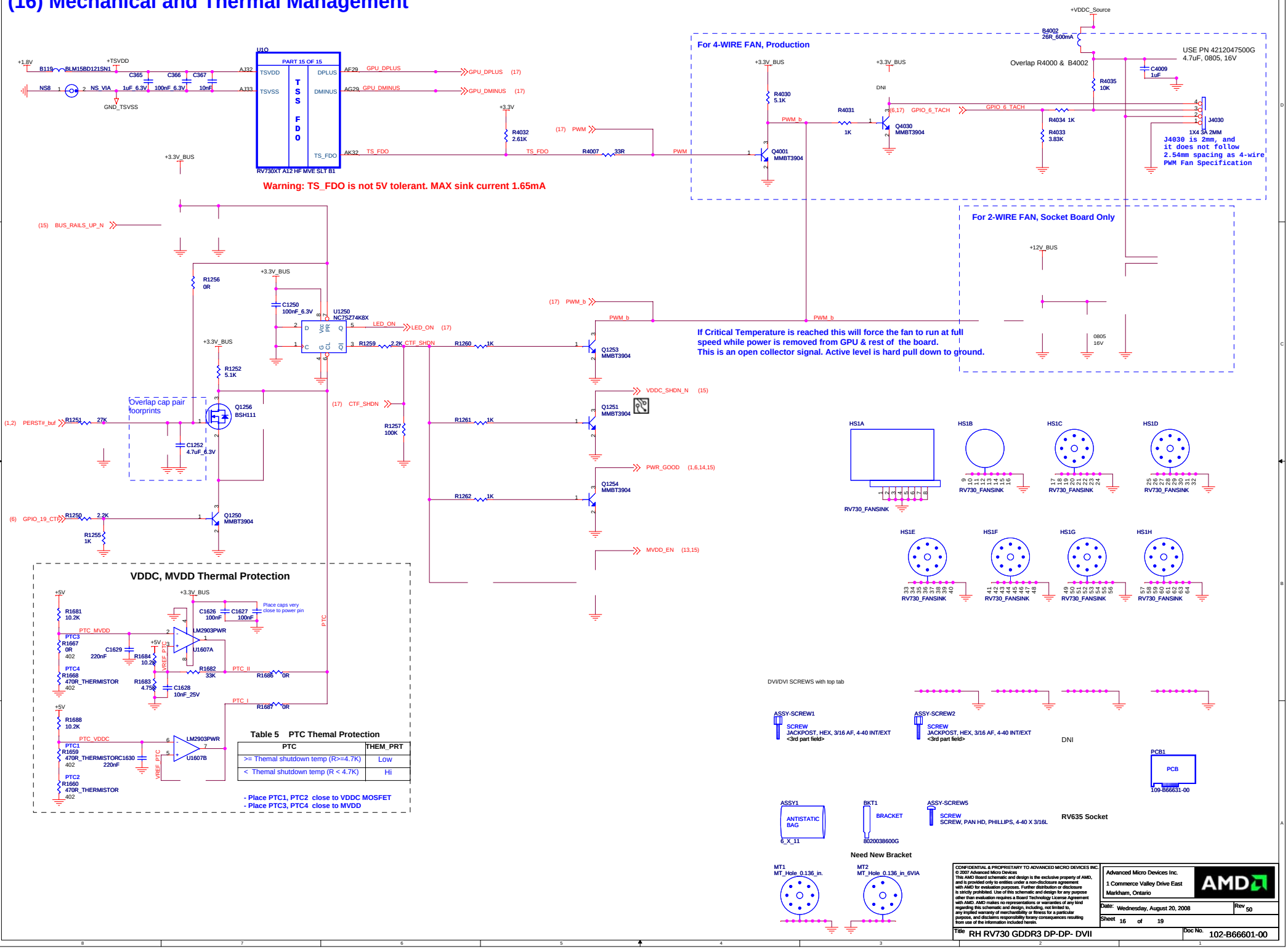


Resistors to set the output voltages for +VDDC and +MVDDC

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date: Wednesday, August 20, 2008	Rev 50
Sheet 15 of 19	
Title RH RV730 GDDR3 DP-DP- DVII	Doc No. 102-B66601-00

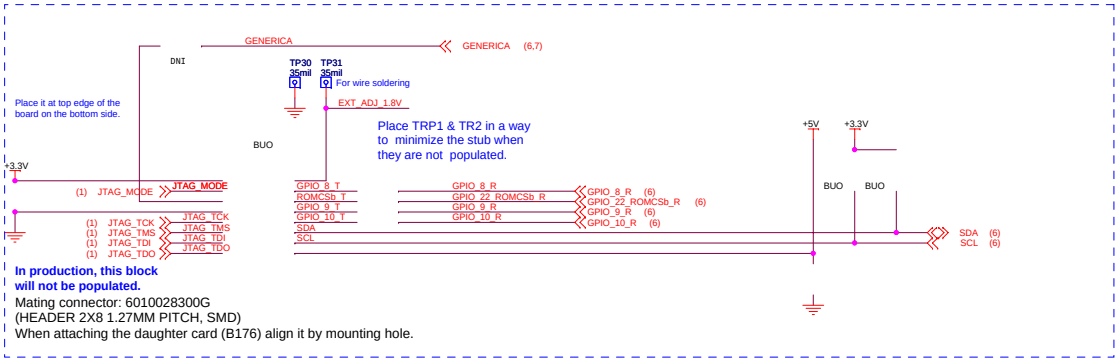
(16) Mechanical and Thermal Management



Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

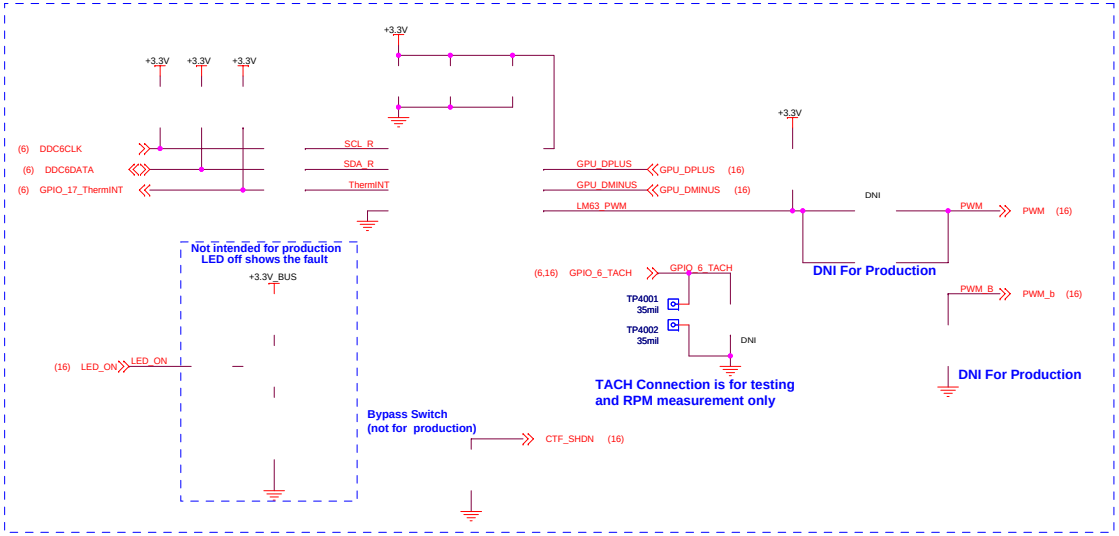
Date:	Wednesday, August 20, 2008
Rev	50
Sheet	16 of 19
Title	RH RV730 GDDR3 DP-DP- DVII
Doc No.	102-B66601-00

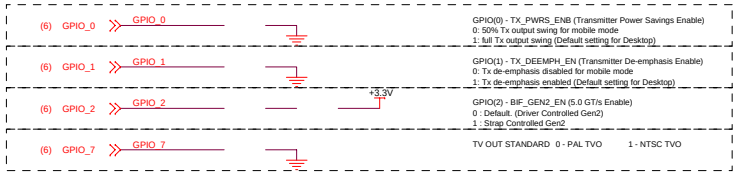
(17) Debug Circuits

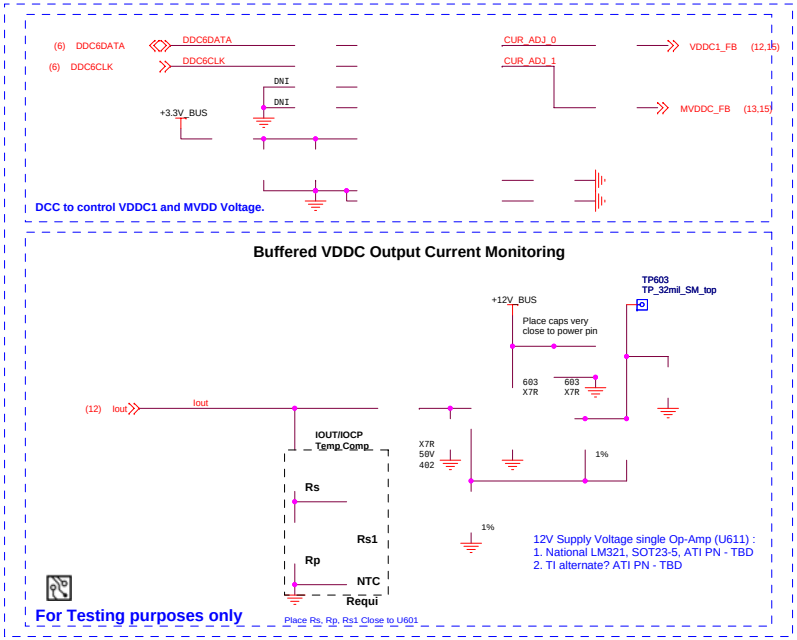


In production, this block will not be populated.

Mating connector: 6010028300G
(HEADER 2X8 1.27MM PITCH, SMD)
When attaching the daughter card (B176) align it by mounting hole.

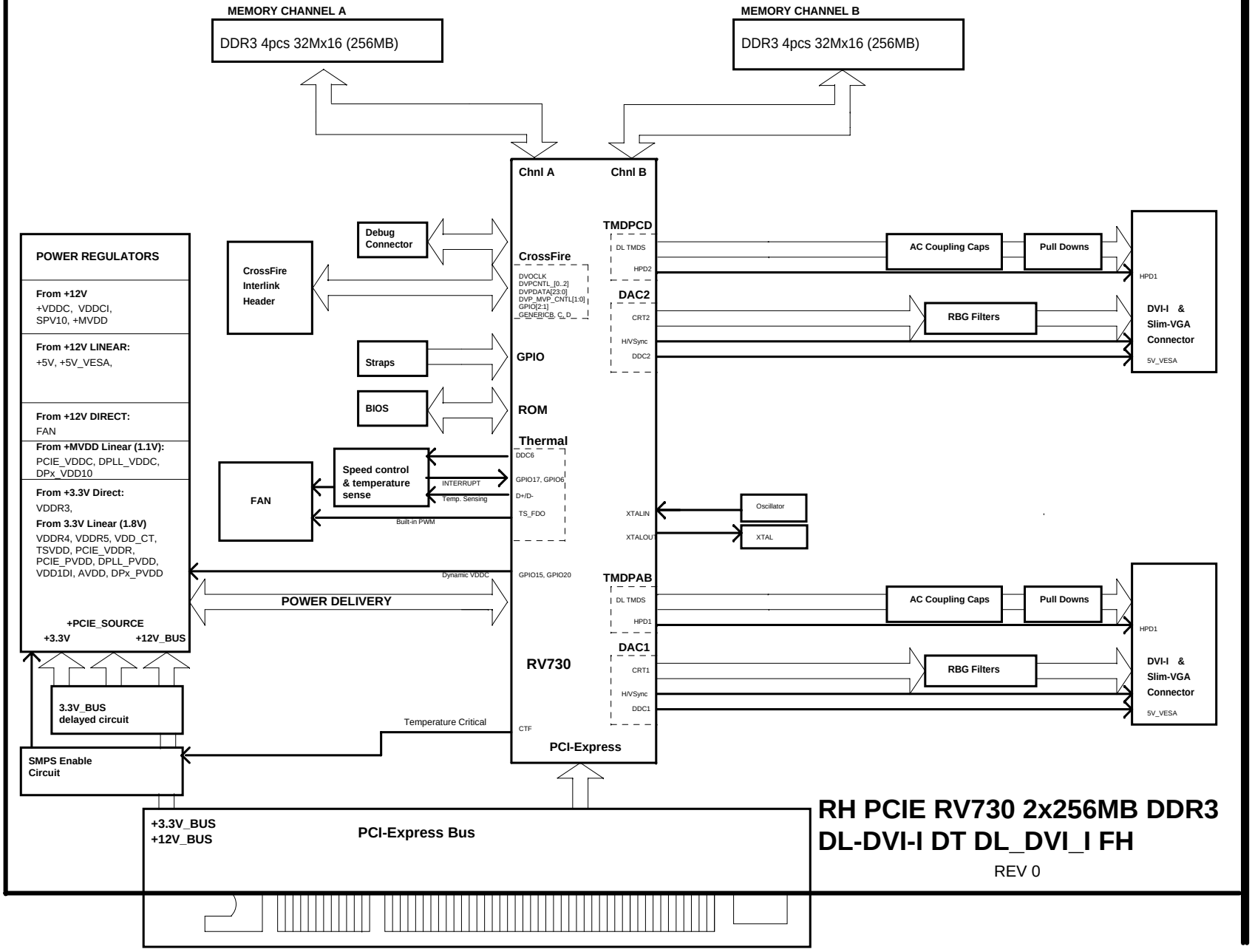






Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

Date:	Wednesday, August 20, 2008
Rev	50
Sheet	17 of 19
Title	RH RV730 GDDR3 DP-DP- DVII
Doc No.	102-B66601-00



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Title	RH-RV730 GDDR3 DP-DP- DVII	
C	102-B66601-00	
Wednesday, August 20, 2008	Doc No. 18	19

Title	Schematic No.	Date:
RH RV730 GDDR3 DP-DP- DVII	102-B66601-00	Wednesday, August 20, 2008

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 50

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	08/04/01	Initial design for RV730 GDDR3
1	00	08/06/14	Update the CTF circuit to include waiting for reset Rotate the VDDC power inductors based on the footprint change (layout) Add stiffener holes to the back of the board (laout) Update the keepout areas for the fansink mounting holes (layout) Add gating of reset with powergood. Update the fansink symbol with the increased keepouts (layout) Added a zener diode option for powering the +5V rail