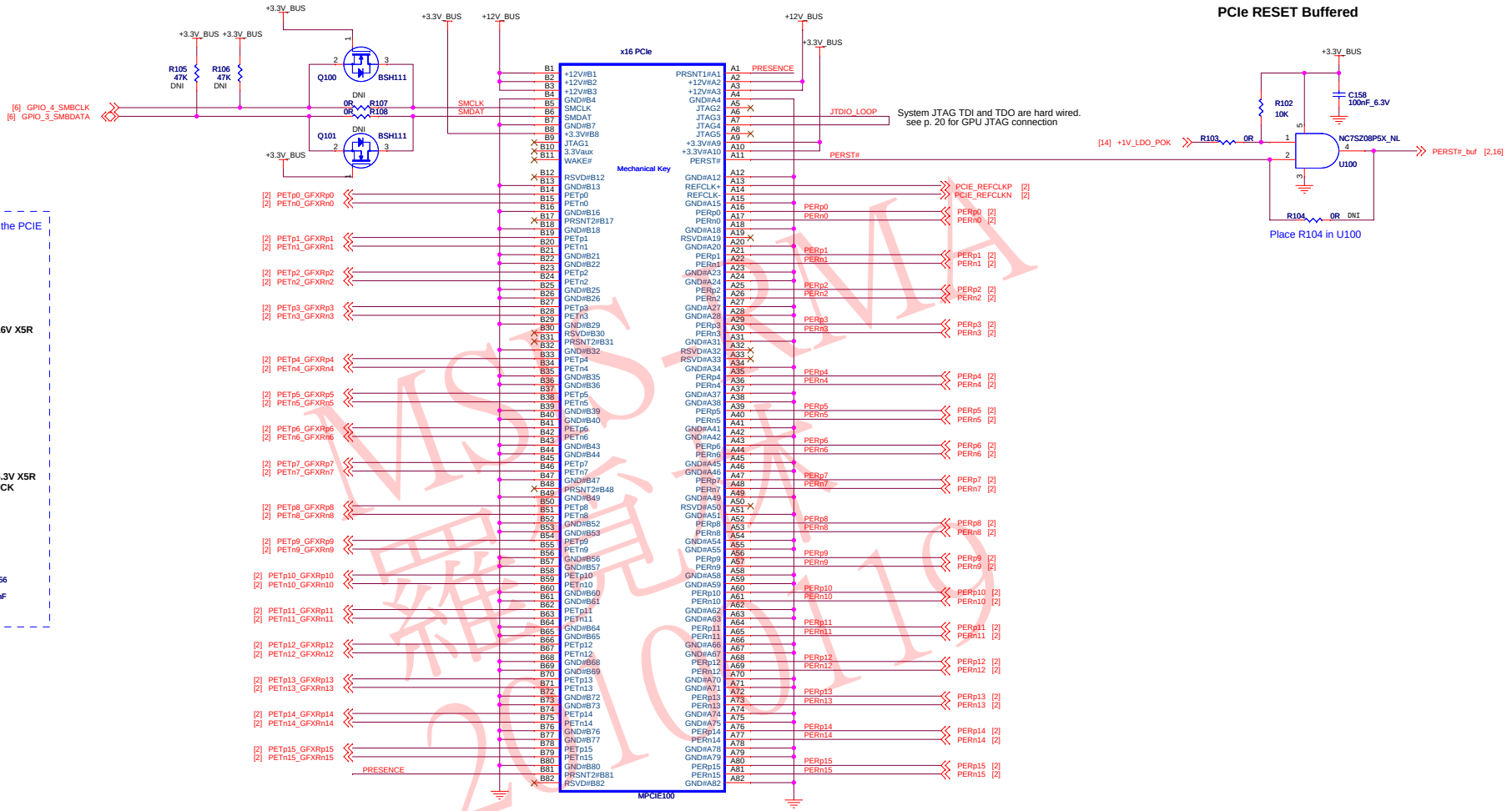
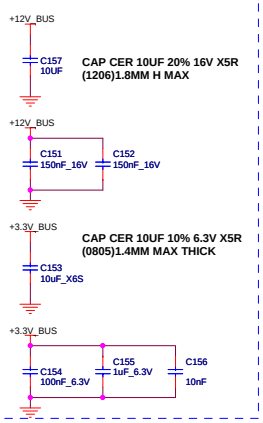
PCI-EXPRESS EDGE CONNECTOR

REDWOOD WOLVERINE



Place these caps as close to the PCIE connector as possible



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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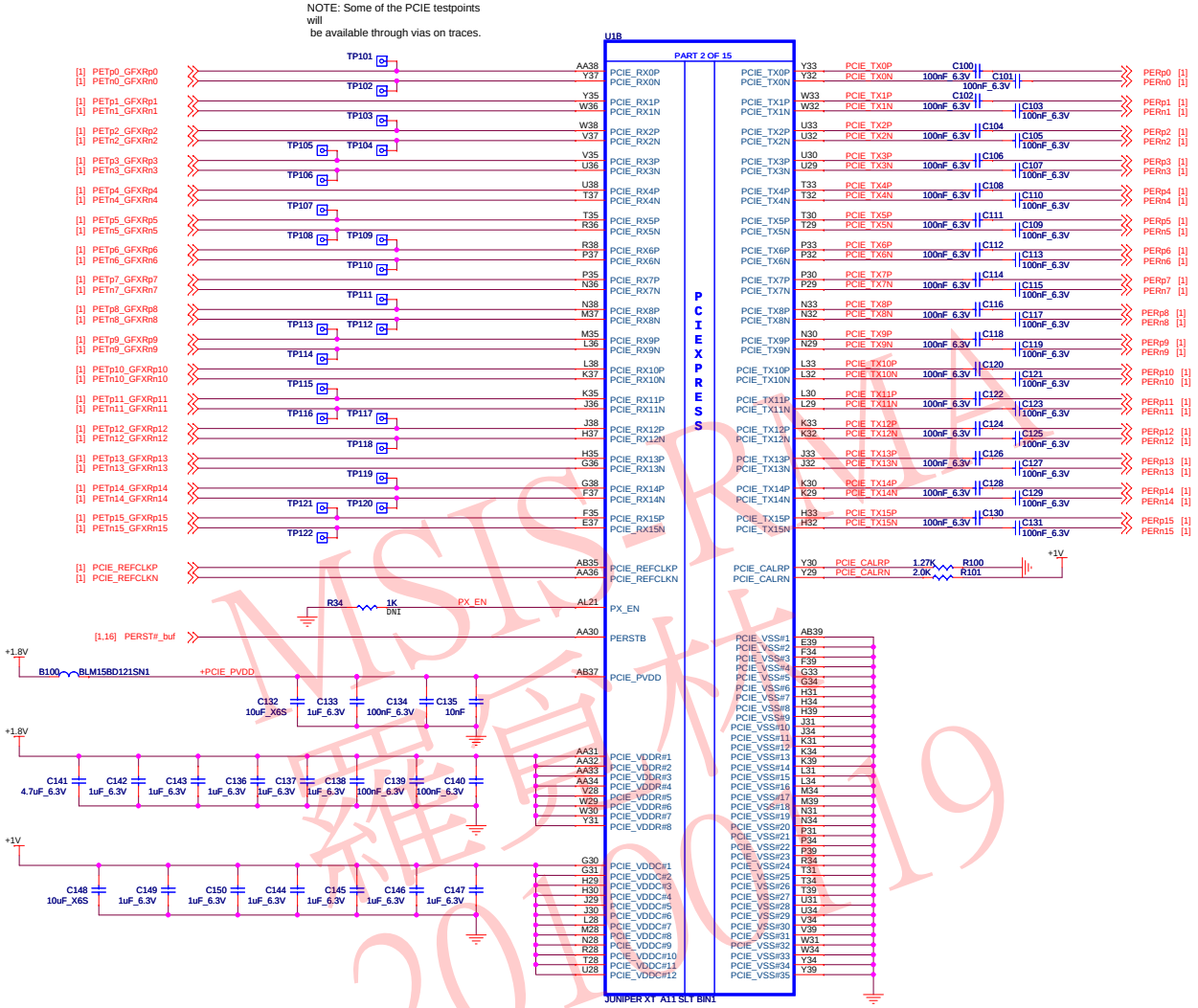
(2) REDWOOD PCIe Interface



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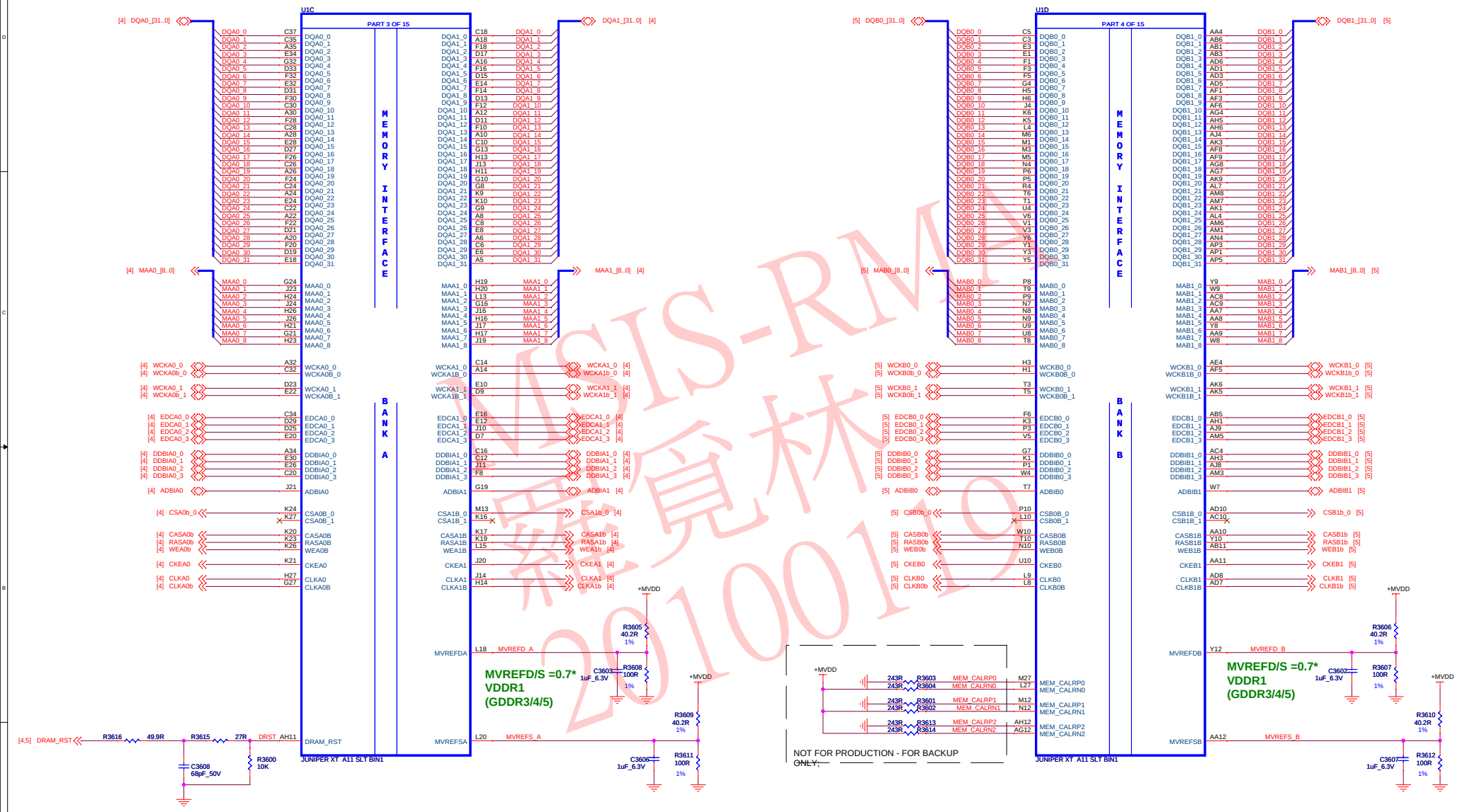
(3) REDWOOD MEM Interface Ch A&B



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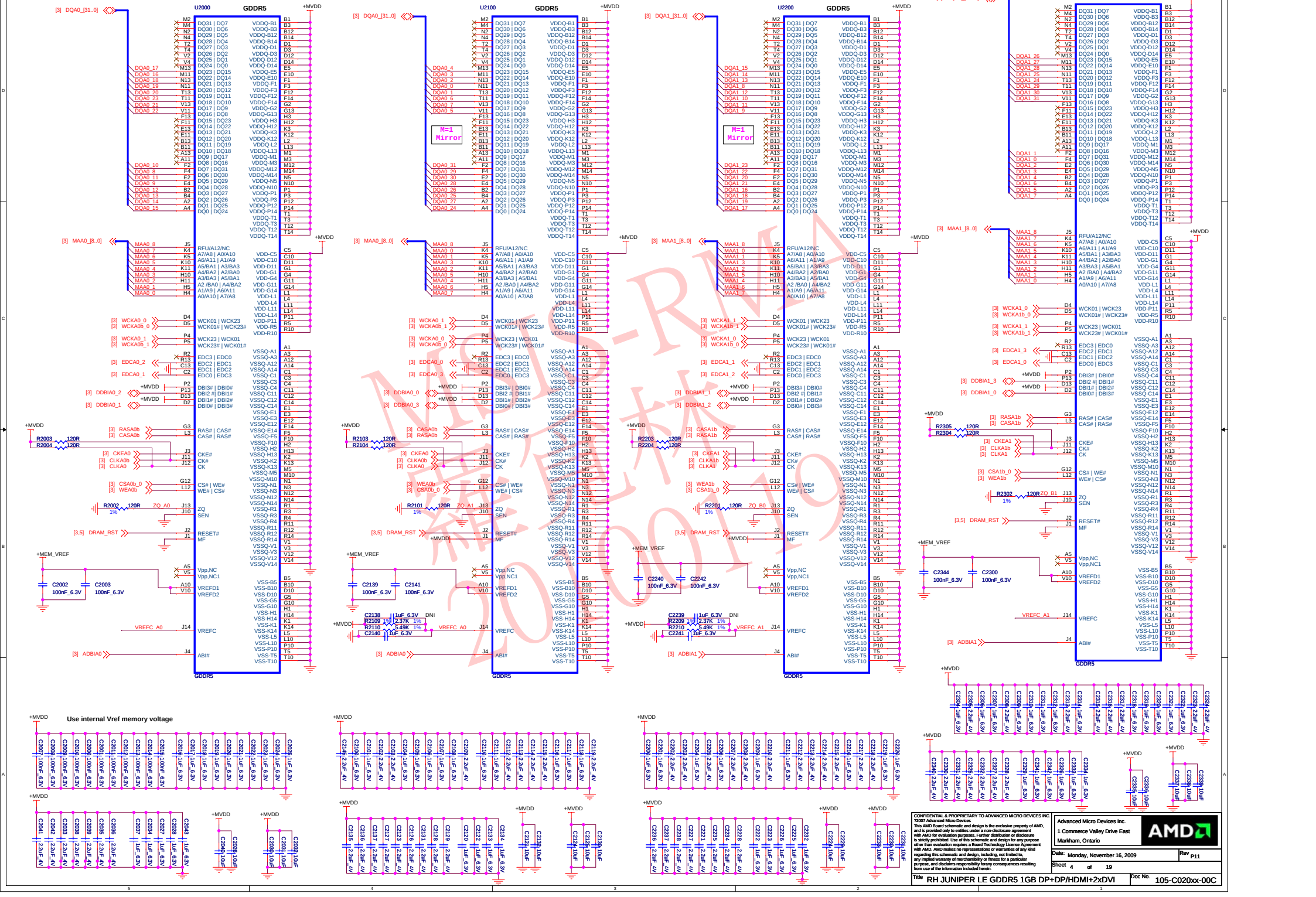
(4) GDDR5 x16 MEM Channel A



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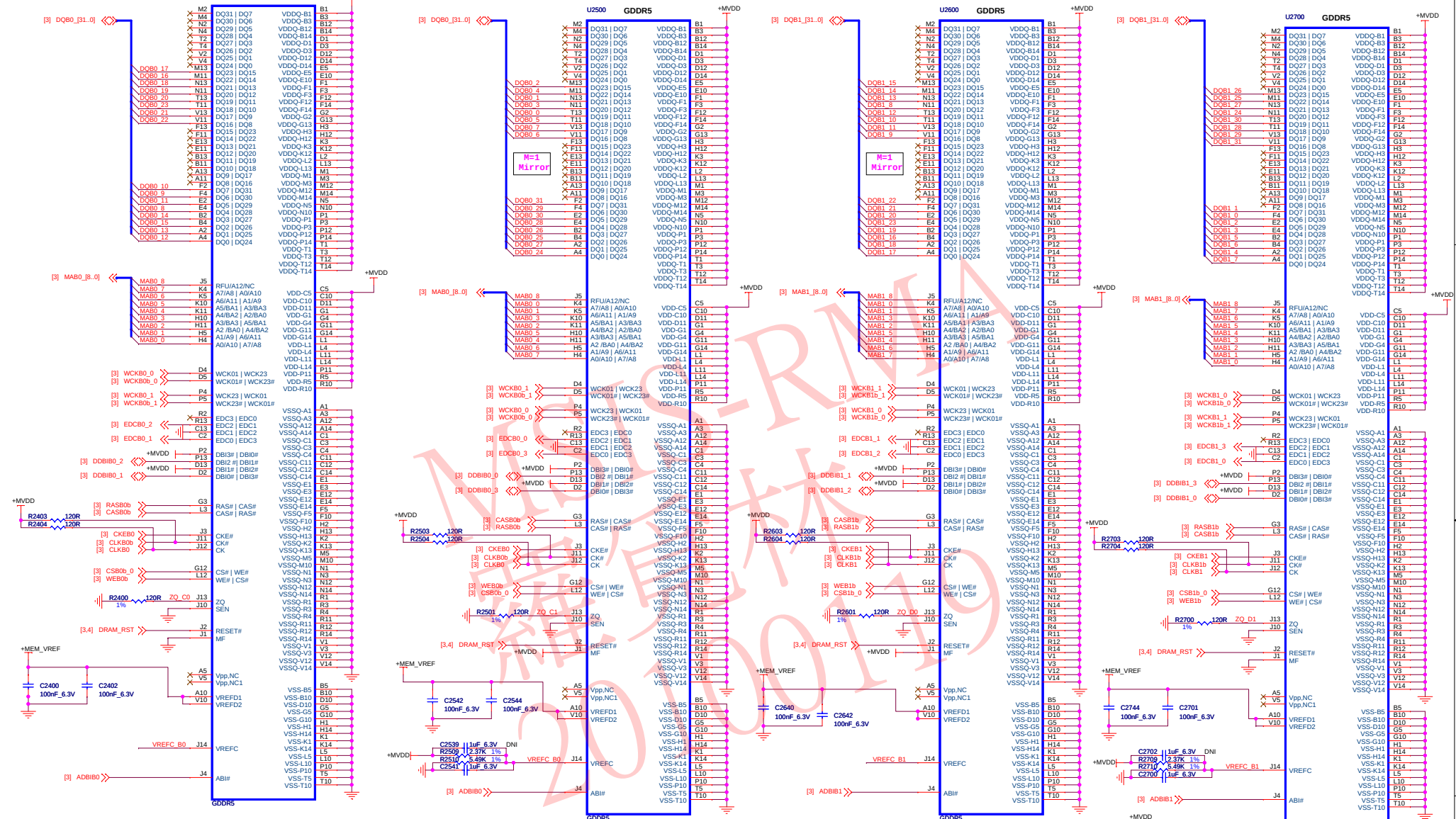
(5) GDDR5 x16 MEM Channel B

CH_B0 =U2400 & U2500

CH_B1 =U2600 & U2700

BOTTOM

TOP



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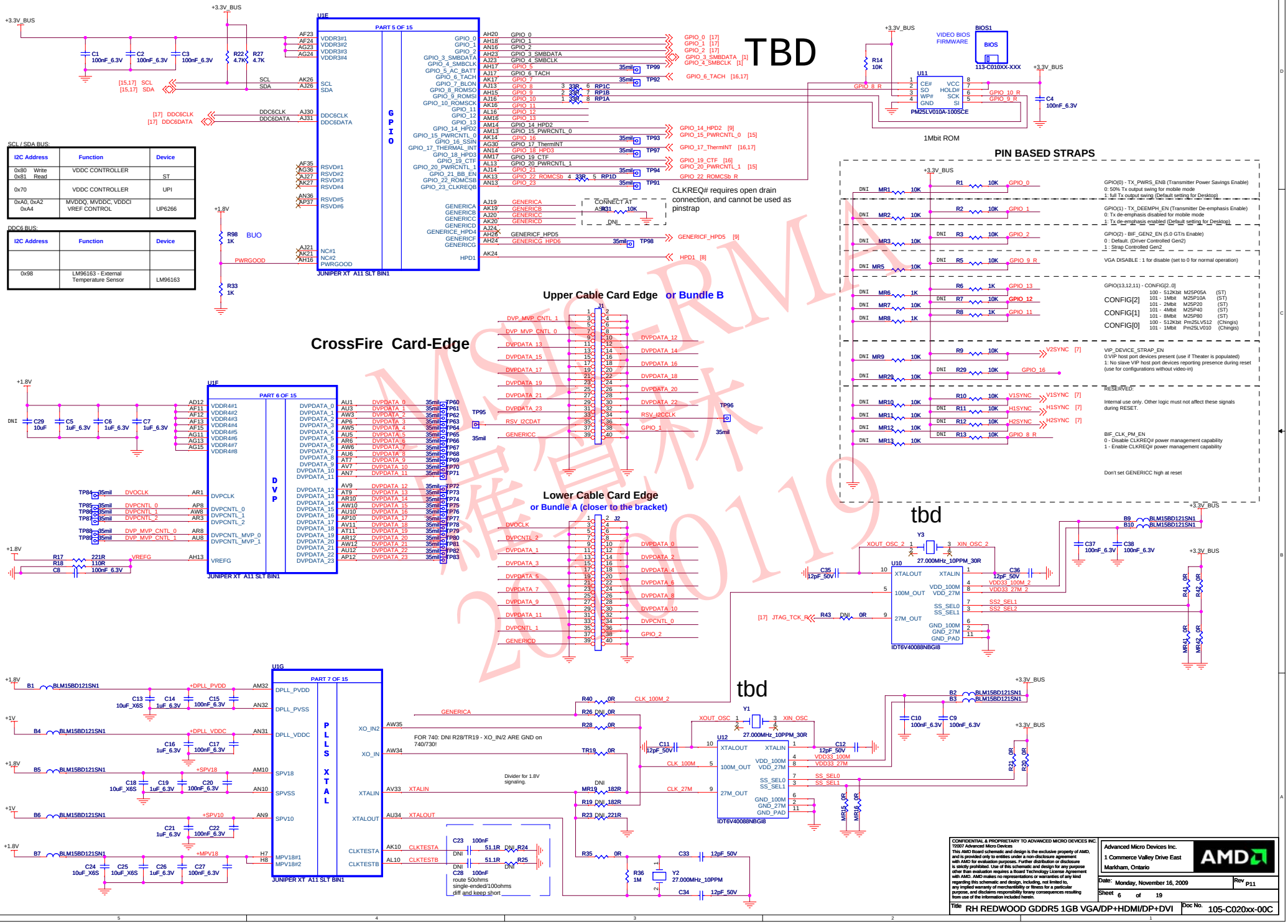
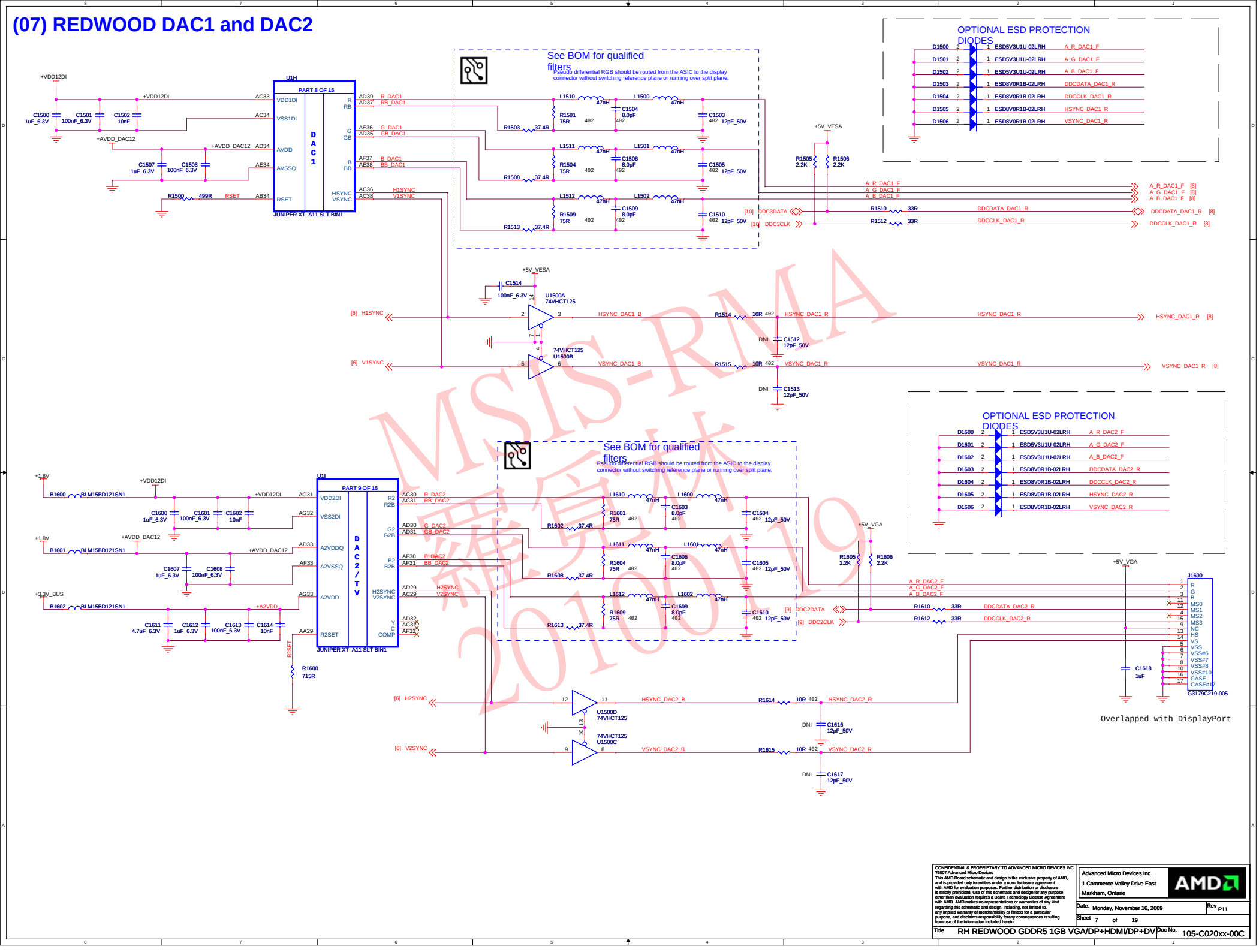
(06) REDWOOD GPIOs Strap CF XTAL OSC



(07) REDWOOD DAC1 and DAC2



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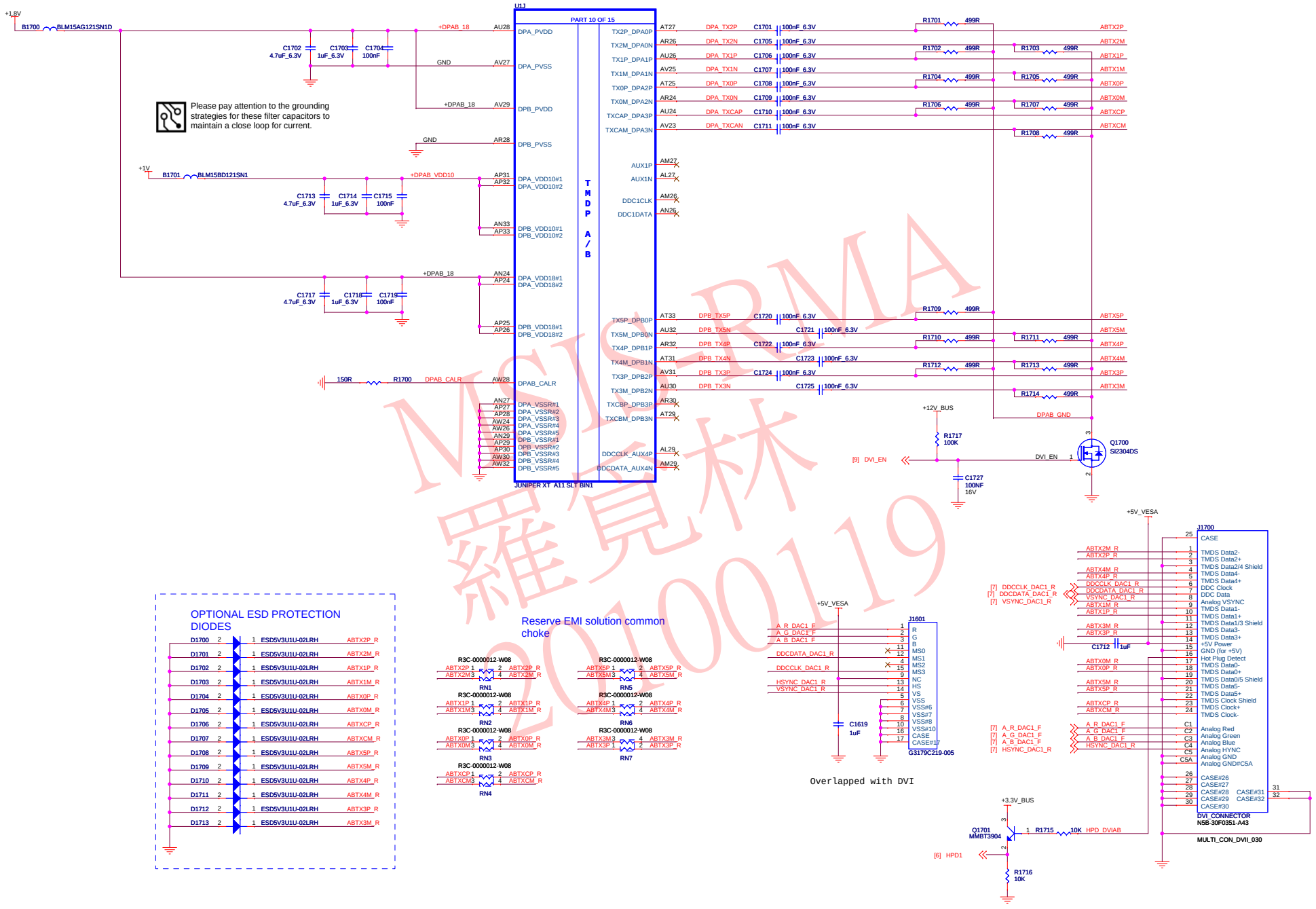
(08) REDWOOD TMDP A&B dDVI-I TOP



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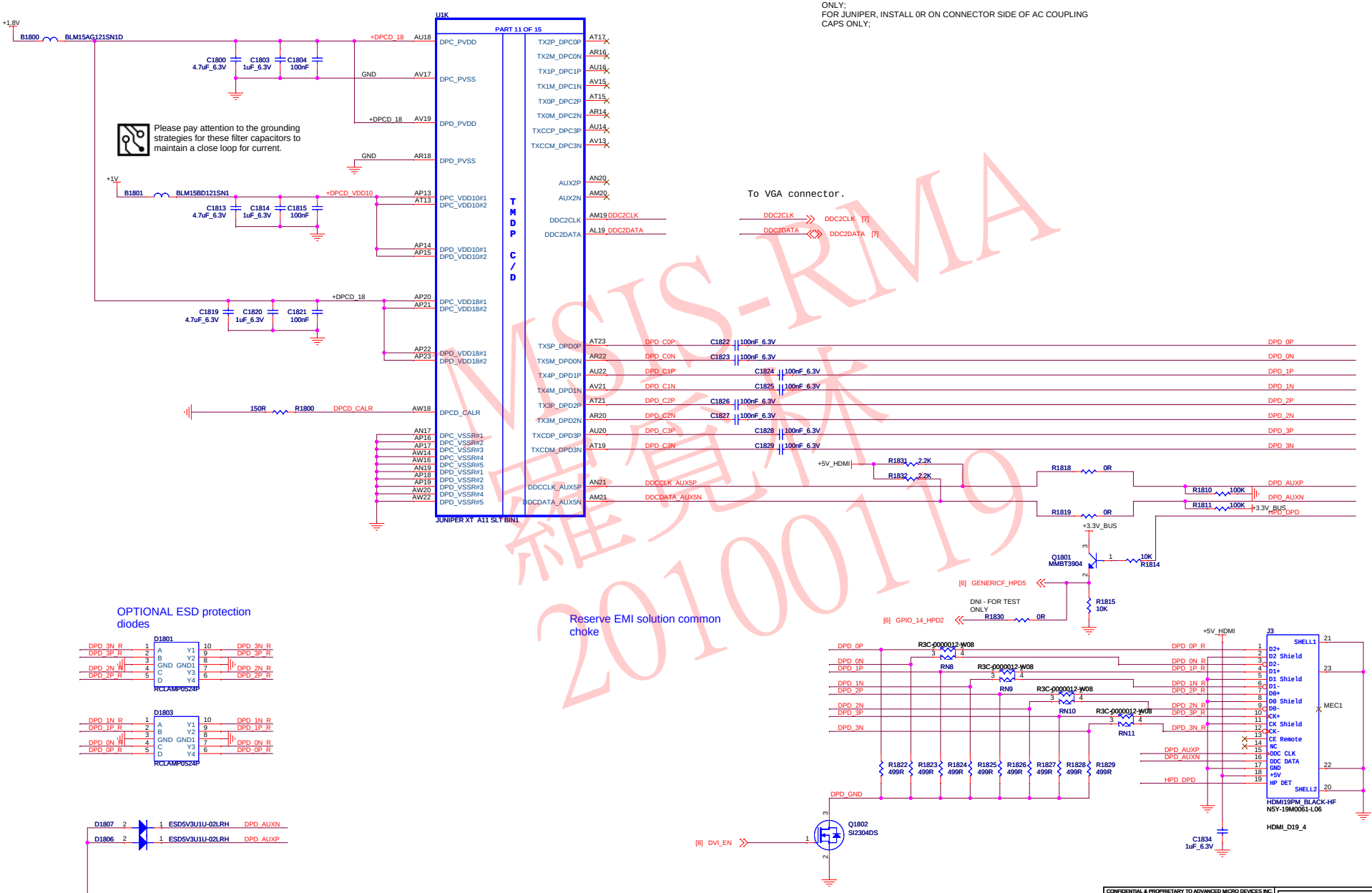
(09) REDWOOD Display Port C & Display Port/HDMI D



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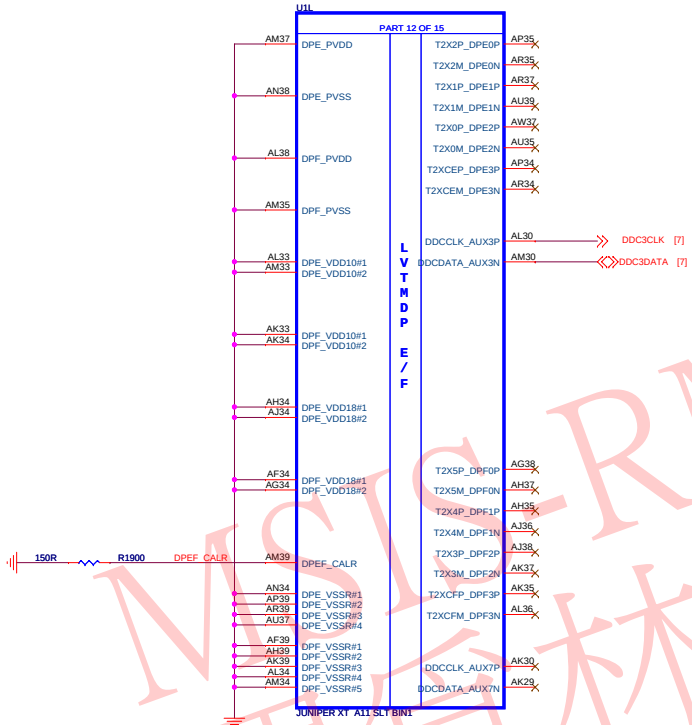
(10) REDWOOD LVTMDP E&F



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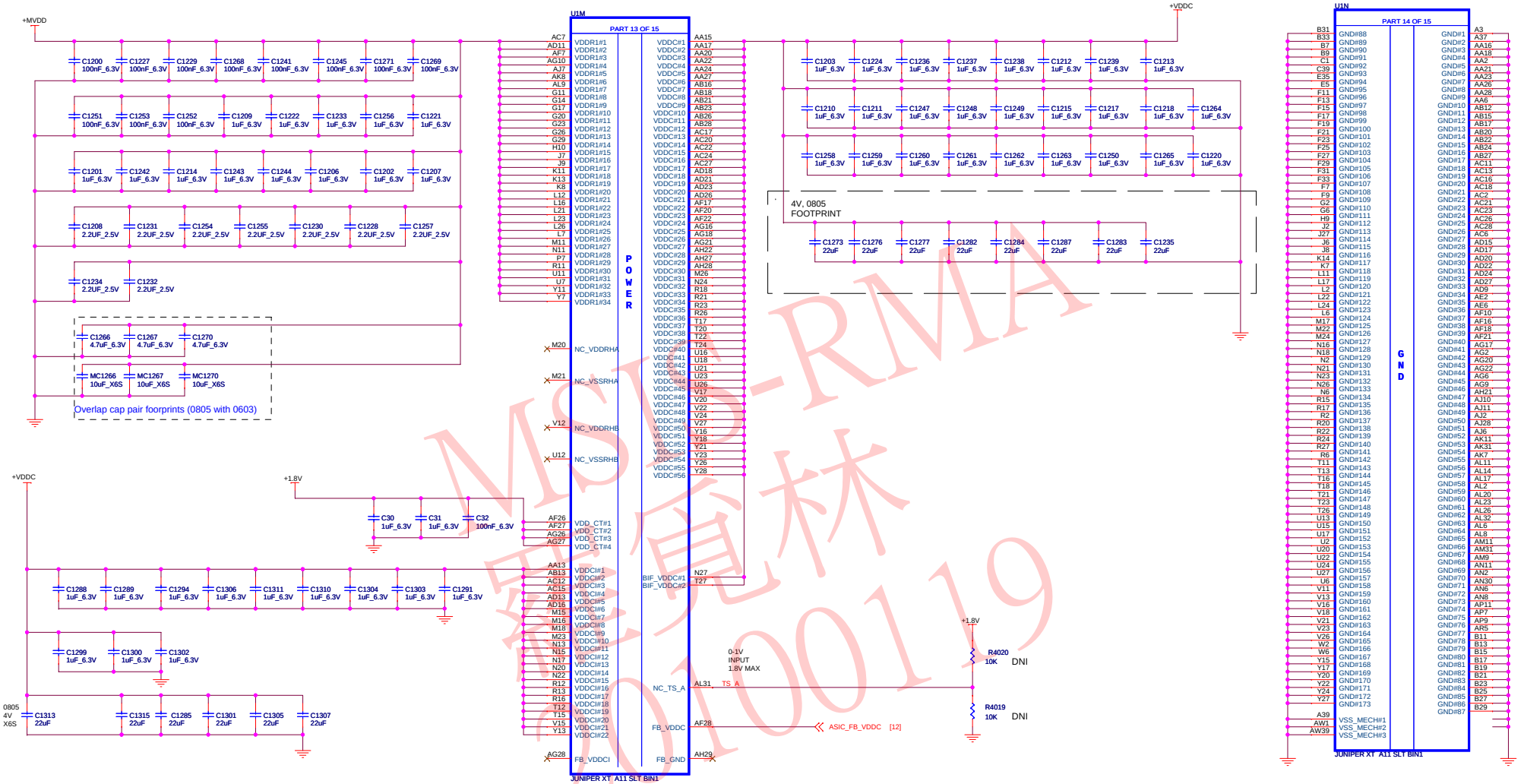
(11) REDWOOD Power & GND



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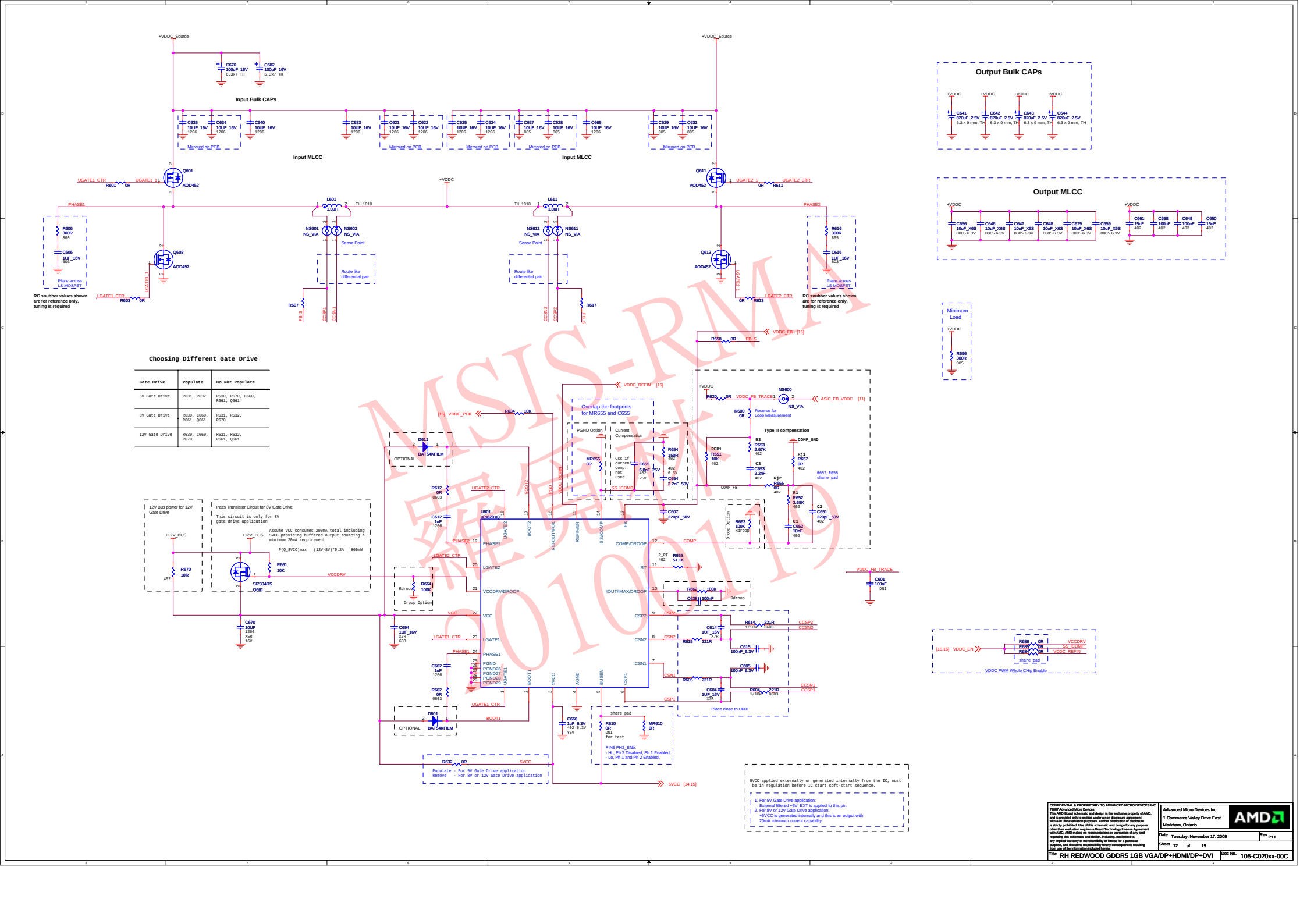
Input Bulk CAPs
Input MLCC
Output Bulk CAPs
Output MLCC
Minimum Load
Choosing Different Gate Drive
Gate Drive | Populate | Do Not Populate
5V Gate Drive | R631, R632 | R630, R670, C660, R661, Q661
8V Gate Drive | R630, C660, R661, Q661 | R631, R632, R670
12V Gate Drive | R630, C660, R670 | R631, R632, R661, Q661
12V Bus power for 12V Gate Drive
Pass Transistor Circuit for 8V Gate Drive
This circuit is only for 8V gate drive application
Assume VCC consumes 200mA total including 5VCC providing buffered output sourcing a minimum 20mA requirement
P(Q_BVCC)max = (12V-8V)*0.2A = 800mW
RC snubber values shown are for reference only, tuning is required
Place across LS MOSFET
Route like differential pair
Sense Point
Overlap the footprints for MR655 and C655
Reserve for Loop Measurement
Type III compensation
Droop Option
Place close to U601
share pad
PINS PH2_ENb:
- Hi , Ph 2 Disabled, Ph 1 Enabled.
- Lo, Ph 1 and Ph 2 Enabled.
5VCC applied externally or generated internally from the IC, must be in regulation before IC start soft-start sequence.
1. For 5V Gate Drive application:
External filtered +5V_EXT is applied to this pin.
2. For 8V or 12V Gate Drive application:
+5VCC is generated internally and this is an output with 20mA minimum current capability
VDDC PWM Whole Chip Enable
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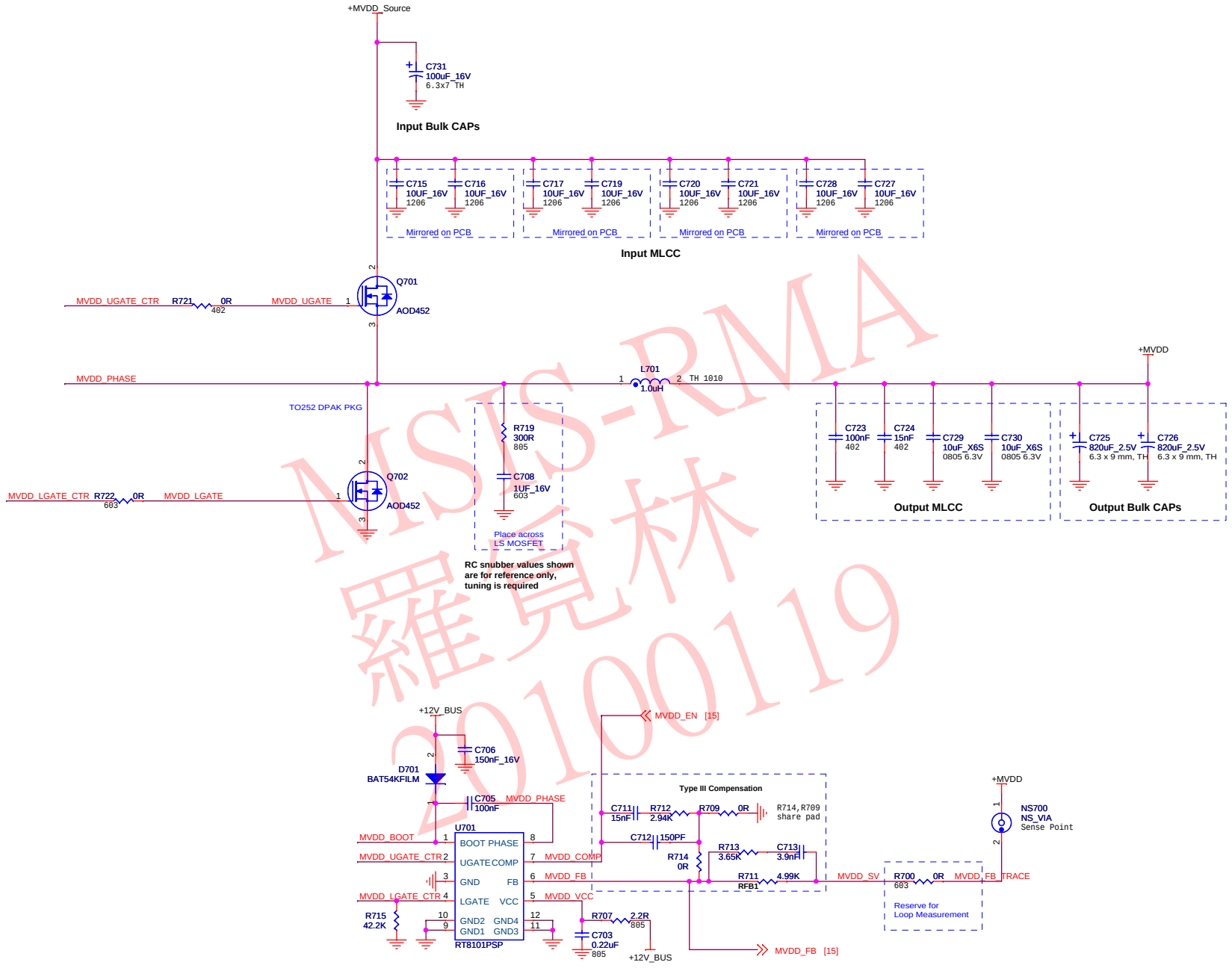

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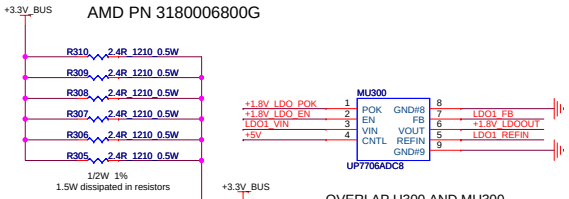
(15) Linear Regulators

Regulators for +5V, +5V_VESA and +5V_HDMI

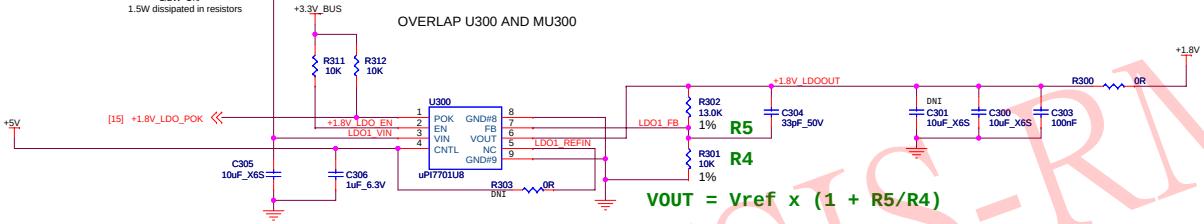
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

USE 6x 3.6R
AMD PN 3180006800G



1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

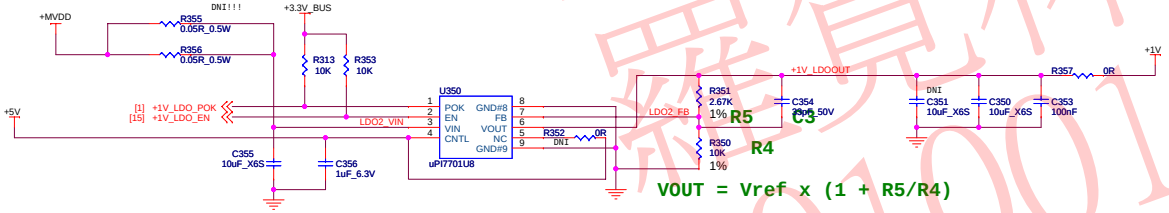
OVERLAP U300 AND MU300



VOUT = Vref x (1 + R5/R4)

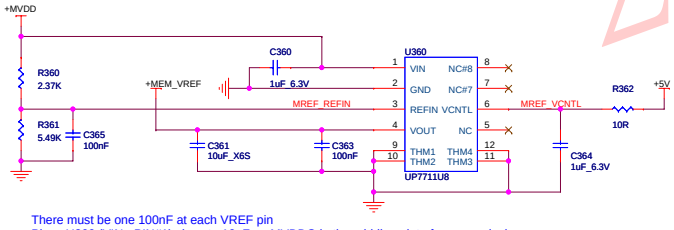
LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA

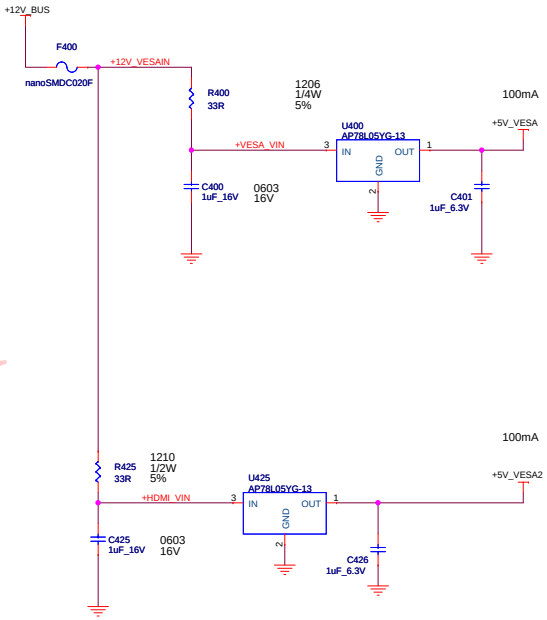


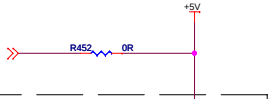
VOUT = Vref x (1 + R5/R4)

Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ

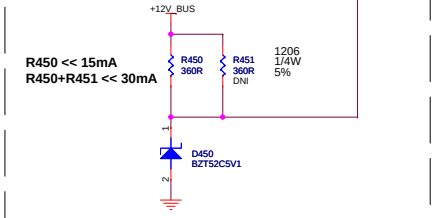


There must be one 100nF at each VREF pin
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices





BACKUP OPTION FOR +5V REGULATOR



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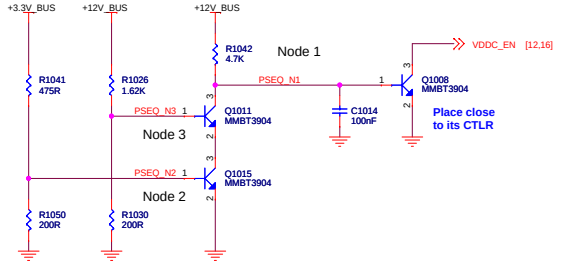
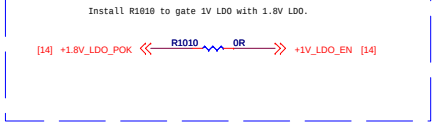
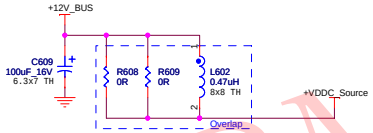
(16) Power Management - Power Gating and Dynamic Voltage Control

12V_BUS & 3V3_BUS POWER SEQUENCING

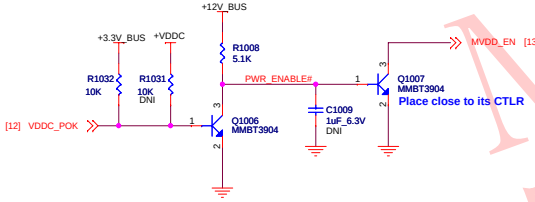


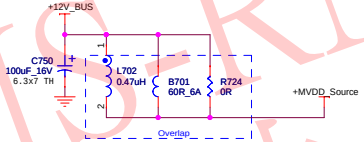




MVDD Low Side Divider

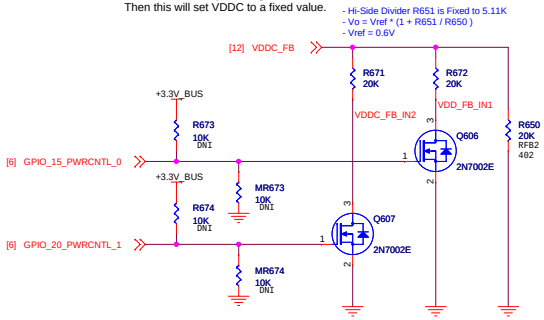
POWER SEQUENCING CIRCUIT



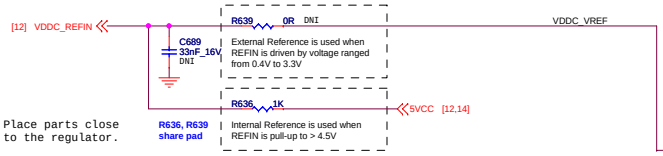


VDDC Low Side Divider

R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.



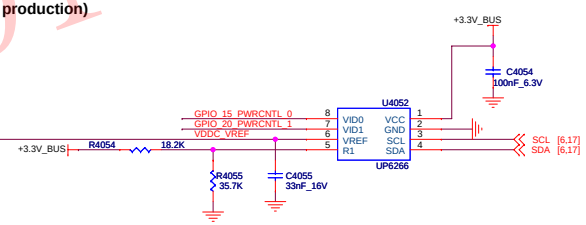
VDDC Reference Voltage Selection



VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

I2C VOLTAGE REFERENCE FOR VDDC (not for production)



I2C ADDRESS: A4

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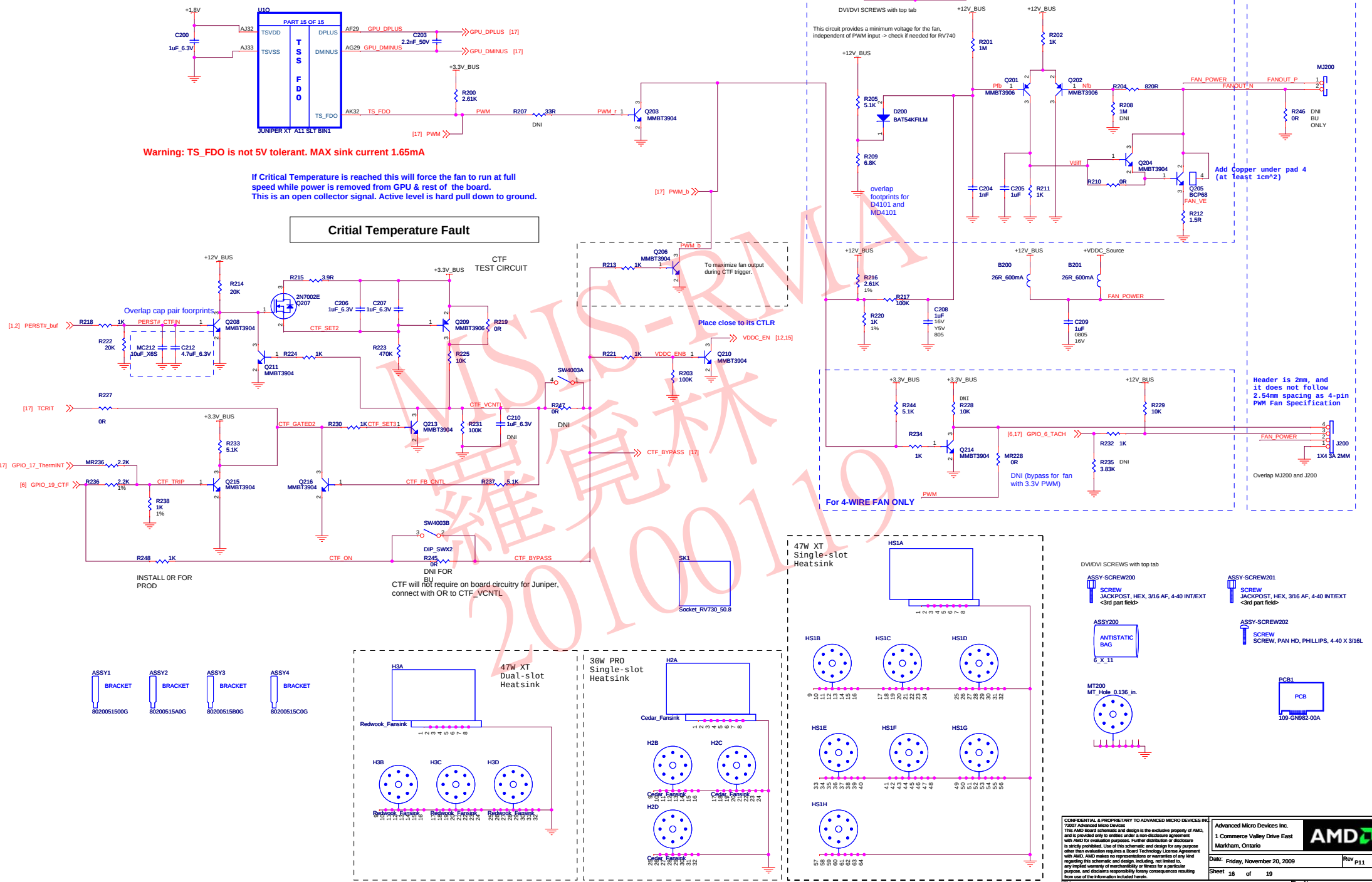
(19) Mechanical and Thermal Management



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Title	RH REDWOOD GDDR5 1GB VGA/DP+HDMI/DP+DVI
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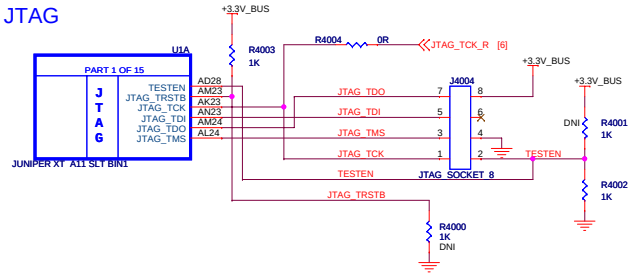
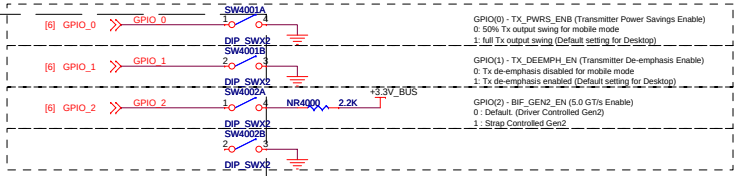
(19) Debug Circuits

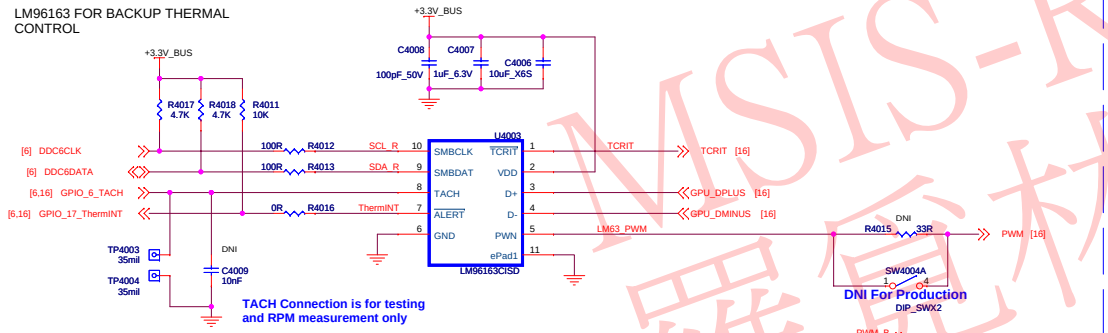
JTAG



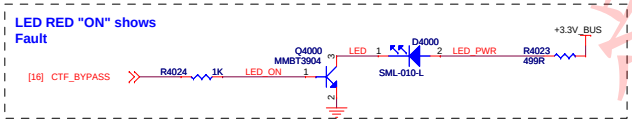
SWITCH CONNECTIONS TO PINSTRAPS



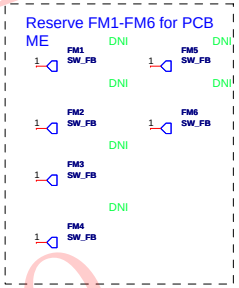
LM96163 FOR BACKUP THERMAL CONTROL



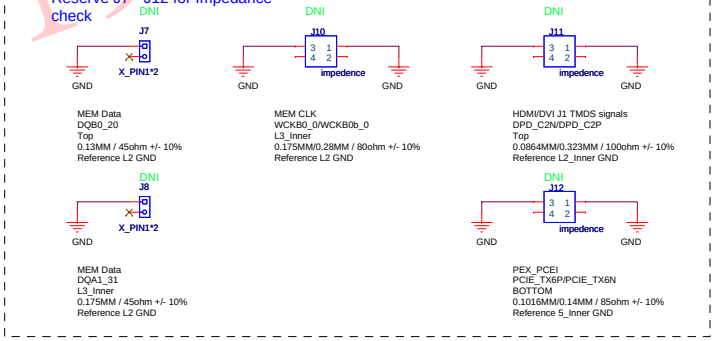
LED RED "ON" shows Fault



Reserve FM1-FM6 for PCB ME

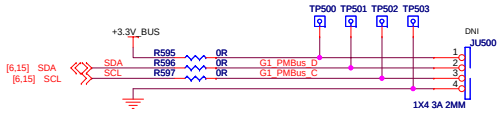


Reserve J7 - J12 for Impedance check



SCL/SDA PORT DEBUG ACCESS

Place connector on the back side
(easily accessible and not blocked by the heatsink).



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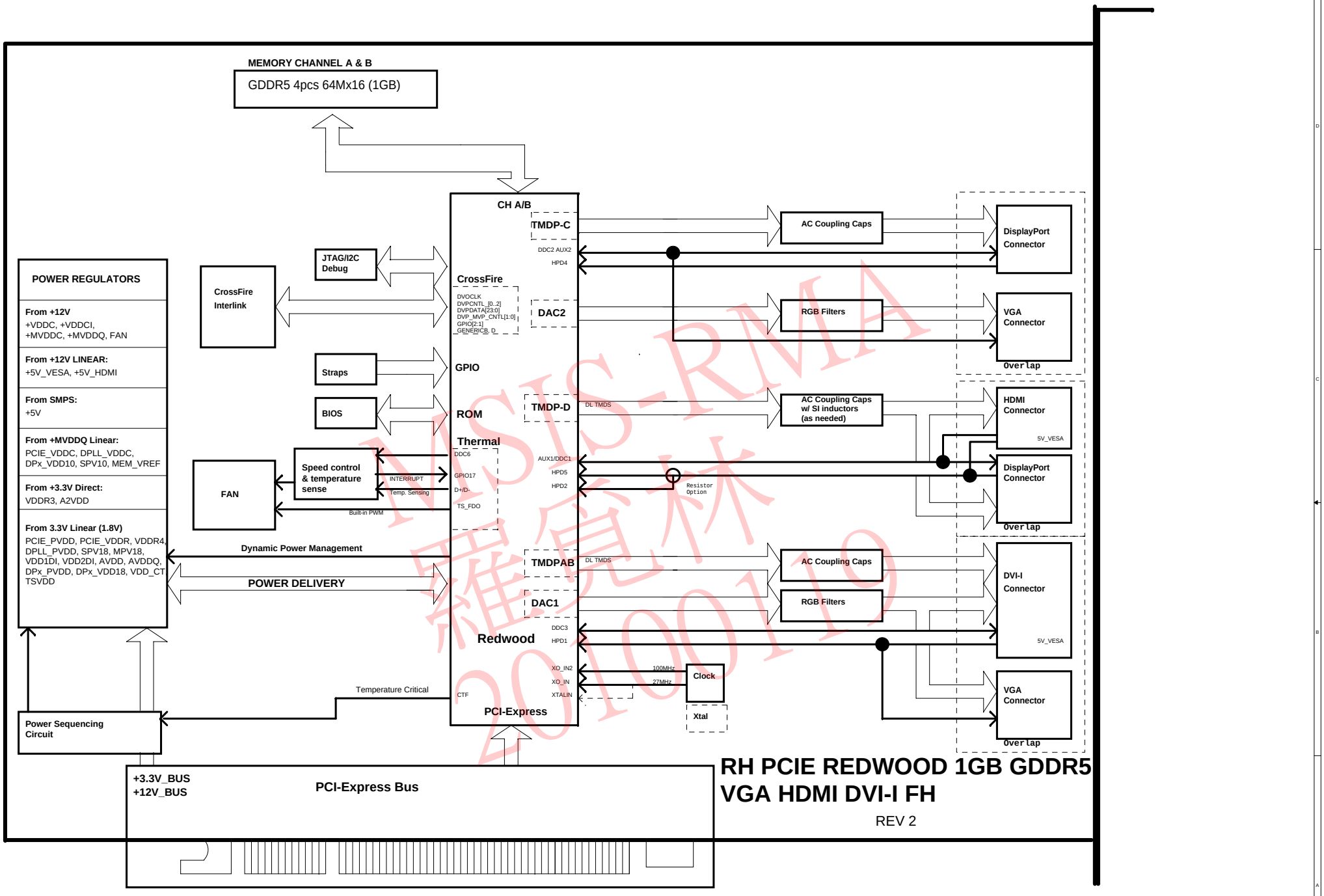

RH PCIE REDWOOD 1GB GDDR5 VGA HDMI DVI-I FH

REV 2

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Title	Schematic No.	Date:
RH REDWOOD GDDR5 1GB VGA/DP+HDMI/DP+DVI	105-C020xx-00C	Monday, November 16, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev P11

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/05/08	
01	00B	2009/08/20	
02	00C	2009/09/28	REDWOOD XT GDDR5 1GB - Initial Release

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