

PG210 B00

GP107 128b GDDR5, 75W , PCB 5.7"  
DVI-D\_DL (DP + DP) + HDMI (DP) + DP

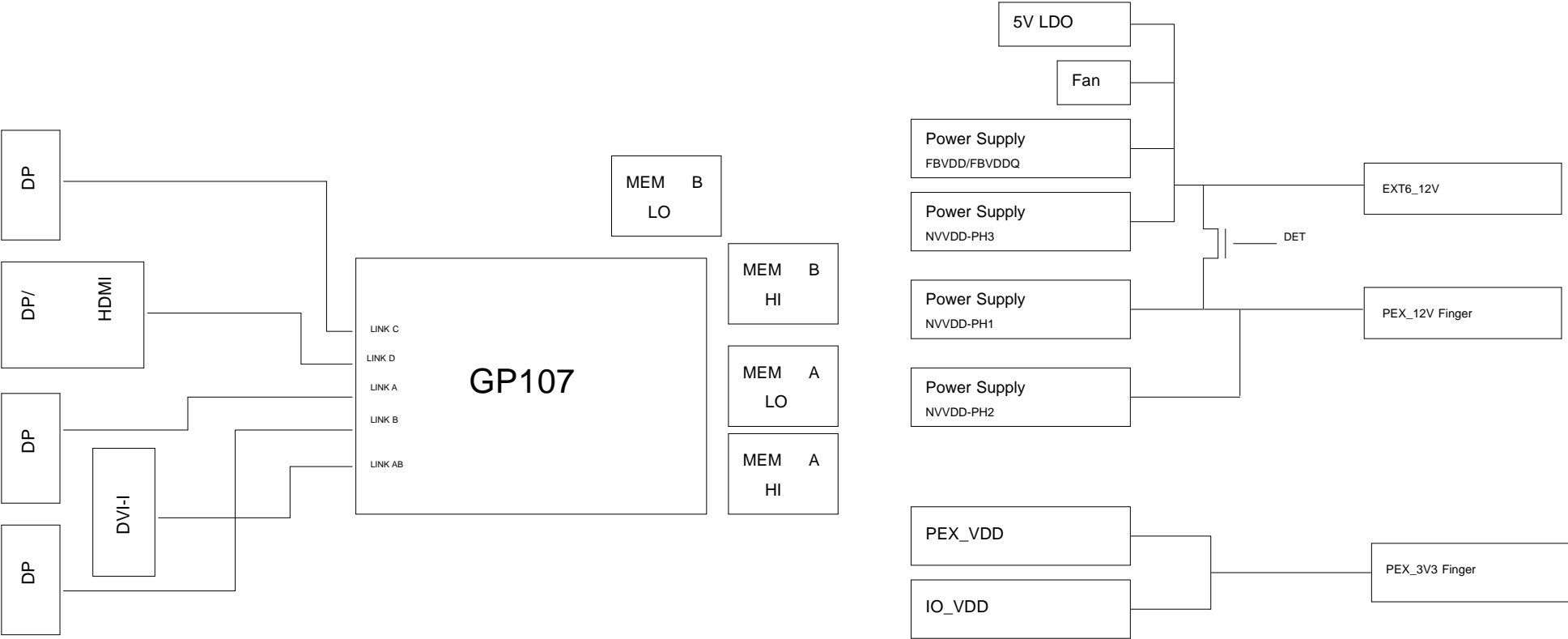
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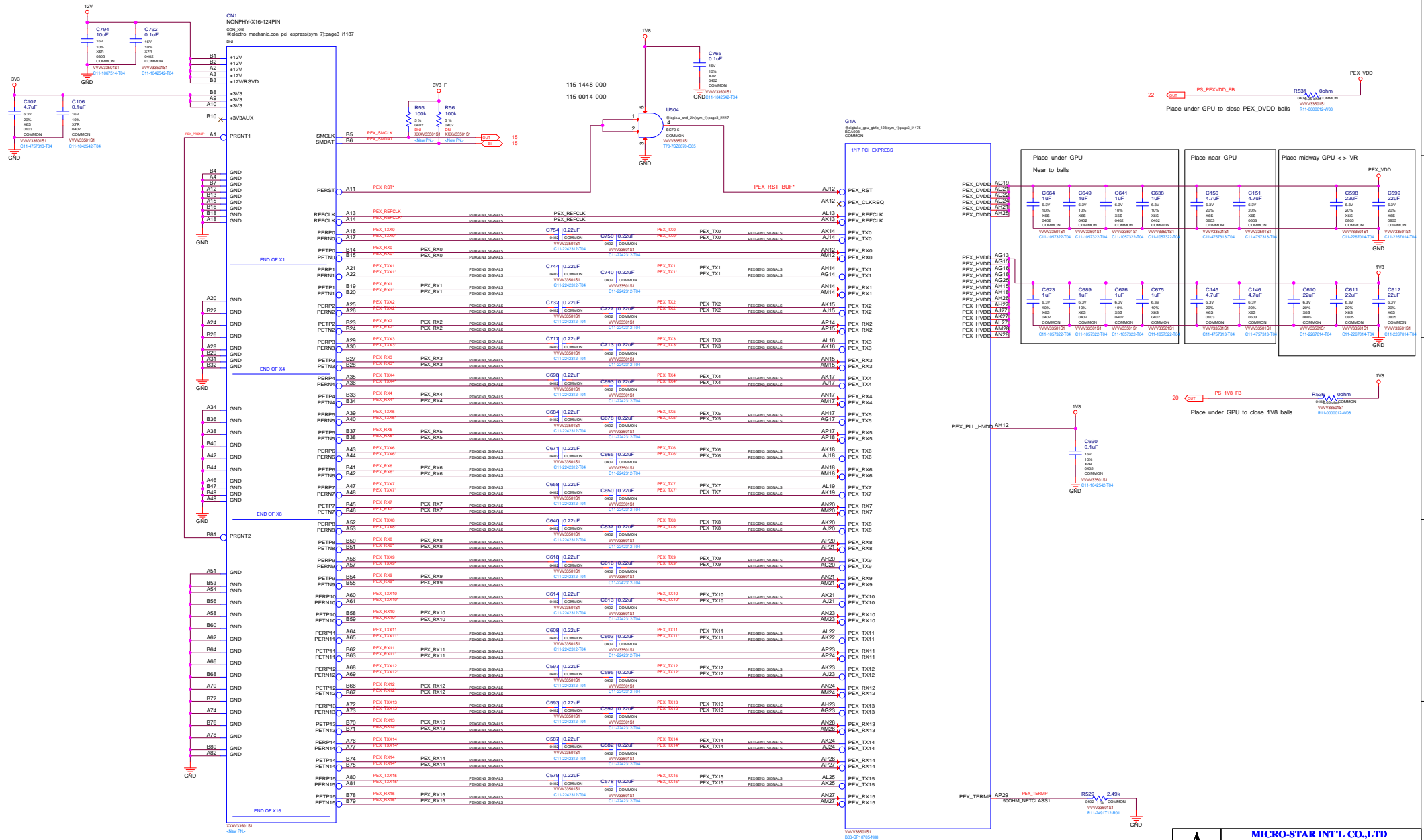
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Block Diagram



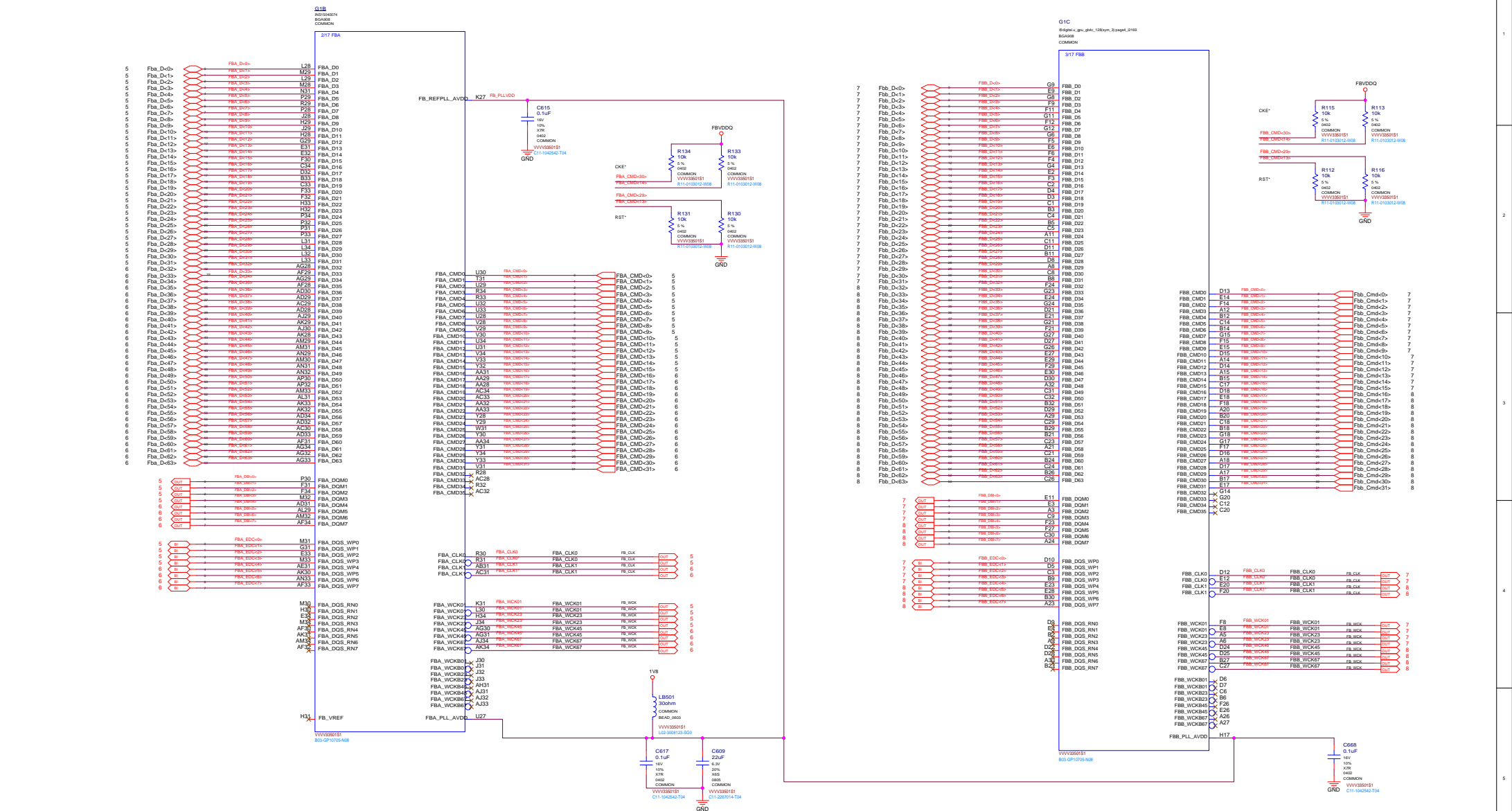
PCI Express



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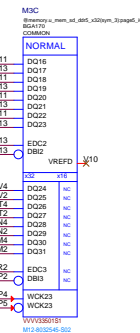
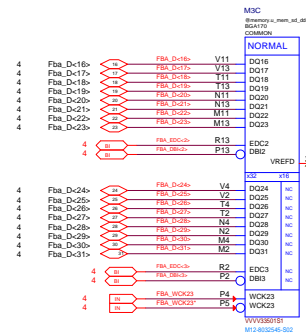
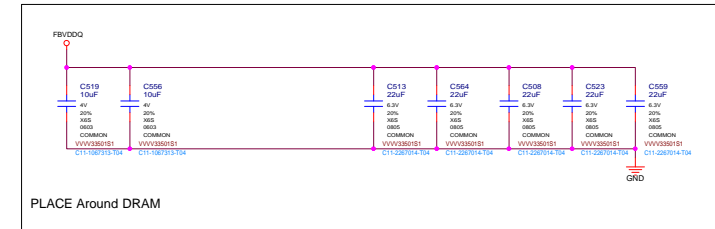
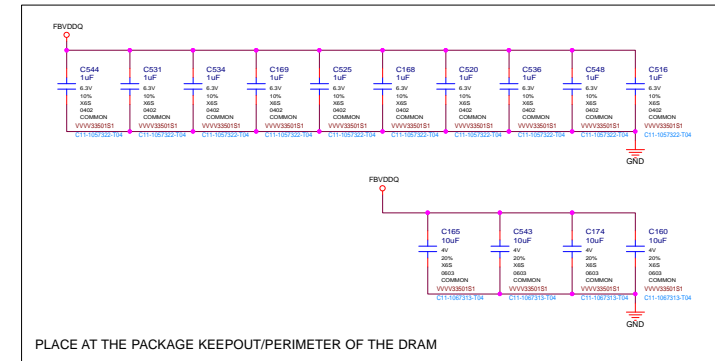
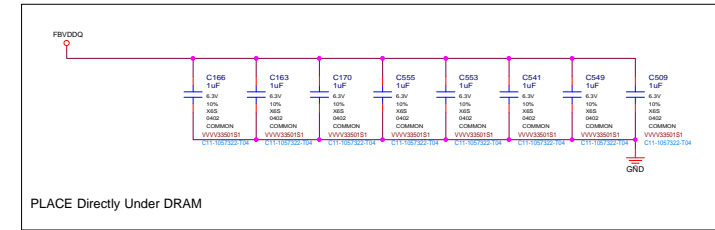
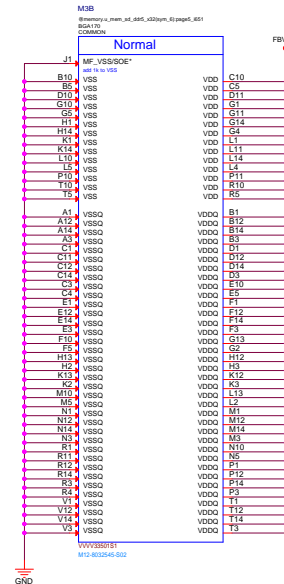
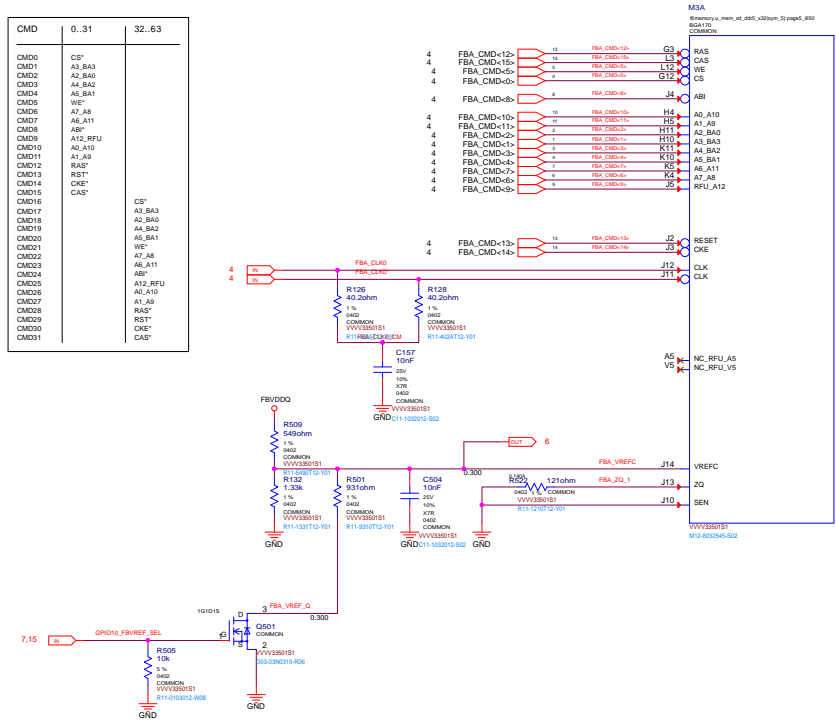
MEMORY: GPU Partition A/B



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Size Custom	Document Description <b>04_MEMORY: GPU Partition A/B</b>	Rev 1.0
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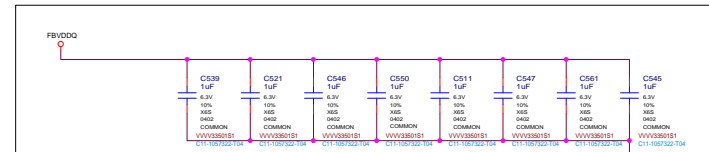
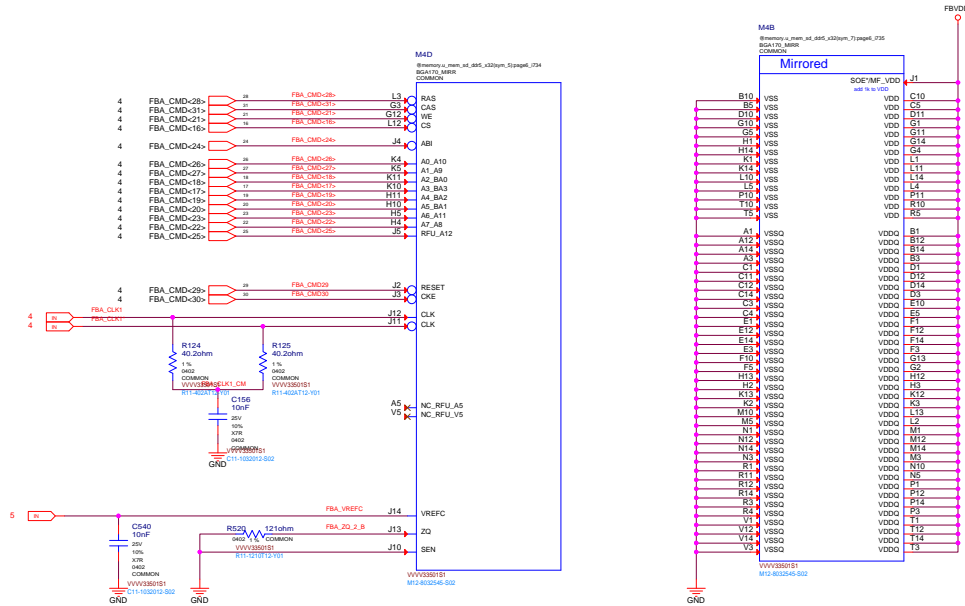
CMD	0..31	32..63
CMD0	CS*	
CMD1	A3..BA3	
CMD2	A2..BA2	
CMD3	A4..BA4	
CMD4	A5..BA1	
CMD5	WE*	
CMD6	A7..A8	
CMD7	A6..A11	
CMD8	AB*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A9	
CMD12	RA5*	
CMD13	RS1*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3..BA3
CMD18		A2..BA2
CMD19		A4..BA4
CMD20		A5..BA1
CMD21		WE*
CMD22		A7..A8
CMD23		A6..A11
CMD24		AB*
CMD25		A12..RFU
CMD26		RA5*
CMD27		A1..A9
CMD28		RS1*
CMD29		CKE*
CMD30		CAS*
CMD31		



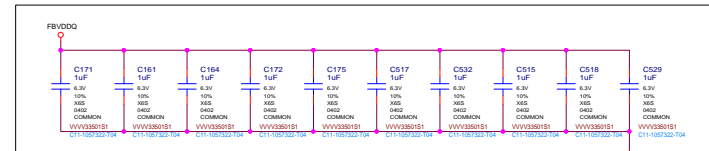
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# MEMORY: FBA Partition 63..32

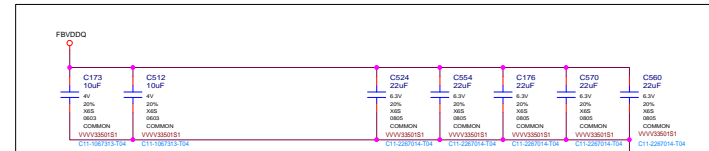
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CMD0	C0*	
CMD1	A0..BA0	
CMD2	A0..BA0	
CMD3	A0..BA0	
CMD4	A0..BA0	
CMD5	WE*	
CMD6	A0..BA0	
CMD7	A0..BA0	
CMD8	AB*	
CMD9	A0..BA0	
CMD10	A0..BA0	
CMD11	A0..BA0	
CMD12	RA0*	
CMD13	RA0*	
CMD14	RA0*	
CMD15	RA0*	
CMD16	RA0*	
CMD17	RA0*	
CMD18	RA0*	
CMD19	RA0*	
CMD20	RA0*	
CMD21	RA0*	
CMD22	RA0*	
CMD23	RA0*	
CMD24	RA0*	
CMD25	RA0*	
CMD26	RA0*	
CMD27	RA0*	
CMD28	RA0*	
CMD29	RA0*	
CMD30	RA0*	
CMD31	RA0*	



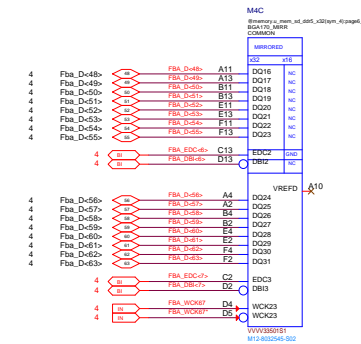
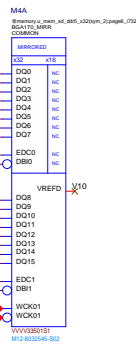
PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM

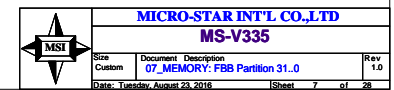
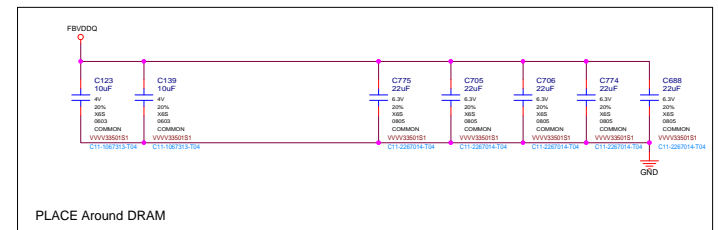
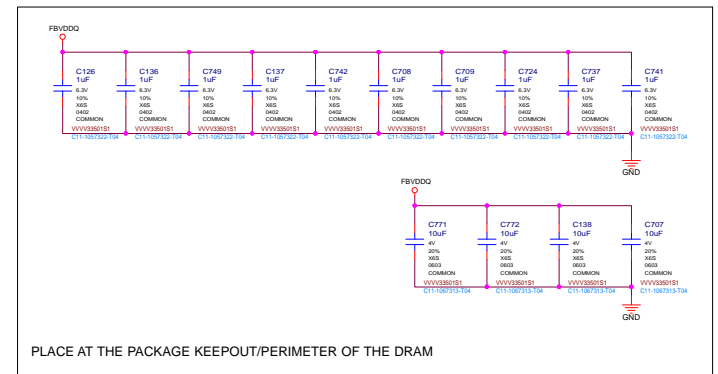
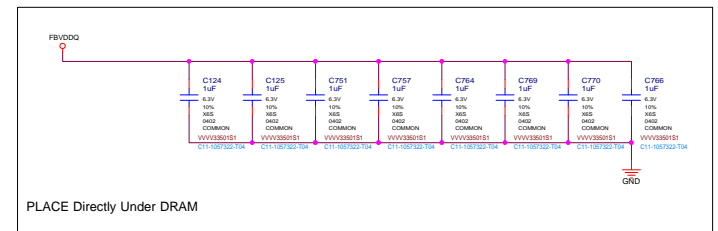
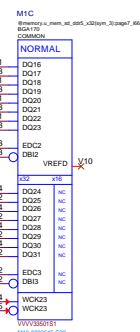
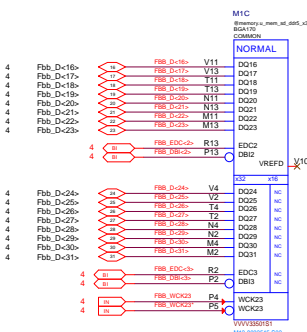
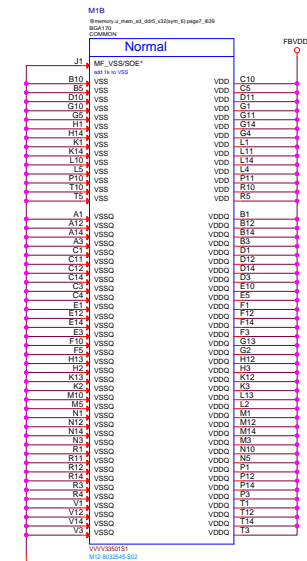
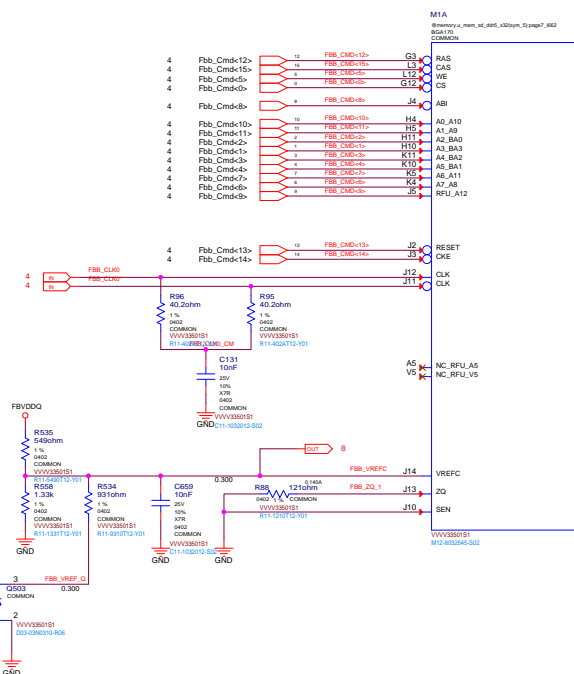


PLACE Around DRAM



MEMORY: FBB Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3..BA3	
CMD2	A2..BA0	
CMD3	A4..BA2	
CMD4	A5..BA1	
CMD5	WE*	
CMD6	A7..A8	
CMD7	AB..A11	
CMD8	AB*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A9	
CMD12	RA3*	
CMD13	RB3*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17	A3..BA3	
CMD18	A2..BA0	
CMD19	A4..BA2	
CMD20	A5..BA1	
CMD21	WE*	
CMD22	A7..A8	
CMD23	AB..A11	
CMD24	AB*	
CMD25	A12..RFU	
CMD26	A0..A10	
CMD27	A1..A9	
CMD28	RA3*	
CMD29	RB3*	
CMD30	CKE*	
CMD31	CAS*	



CMD	0.31	32..63
CMD0	C5*	
CMD1	A3_BA3	
CMD2	A2_BA2	
CMD3	A4_BA2	
CMD4	AS_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_RFU	
CMD12	RA5*	
CMD13	RS1*	
CMD14	CRK*	
CMD15	CAS*	
CMD16		C5*
CMD17		A3_BA3
CMD18		A2_BA2
CMD19		A4_BA2
CMD20		AS_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		AS_A11
CMD24		AB*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_RFU
CMD28		RA5*
CMD29		RS1*
CMD30		CRK*
CMD31		CAS*

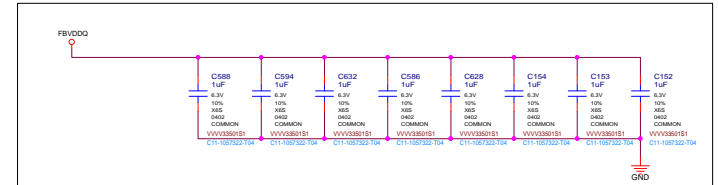
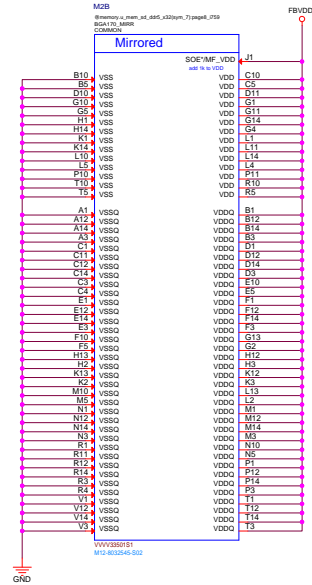
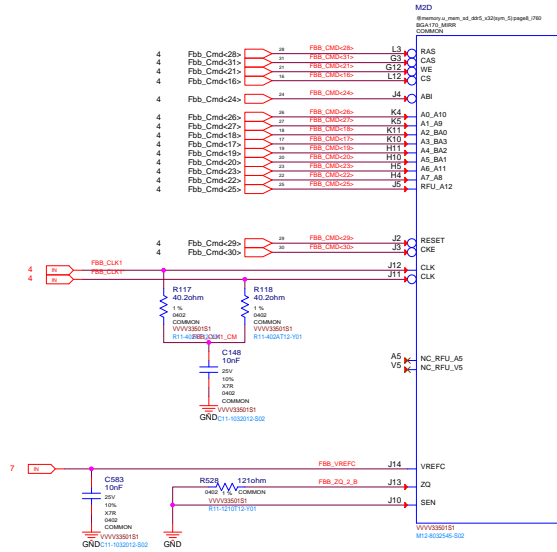
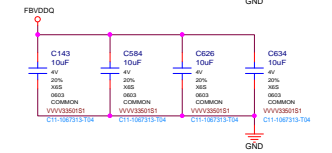
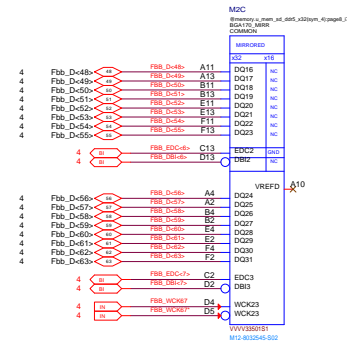
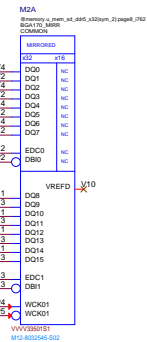


Figure 10 is a schematic diagram of the power supply circuit for the 100W 1000V MOSFET. The circuit consists of a series of capacitors (C141, C504, C144, C533, C596, C602, C589, C605, C607, and C585) connected to a common ground line labeled 'COMMON'. The input voltage is 100VDC. The output voltage is 100VDC. The capacitors are labeled with their values: C141 (100µF), C504 (100µF), C144 (100µF), C533 (100µF), C596 (100µF), C602 (100µF), C589 (100µF), C605 (100µF), C607 (100µF), and C585 (100µF). The circuit is labeled '100W 1000V MOSFET'.

[illegible]

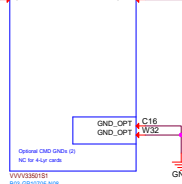
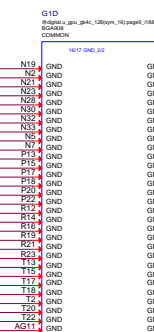
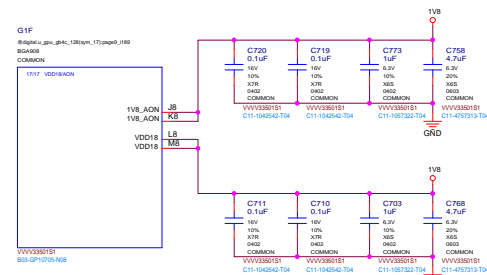
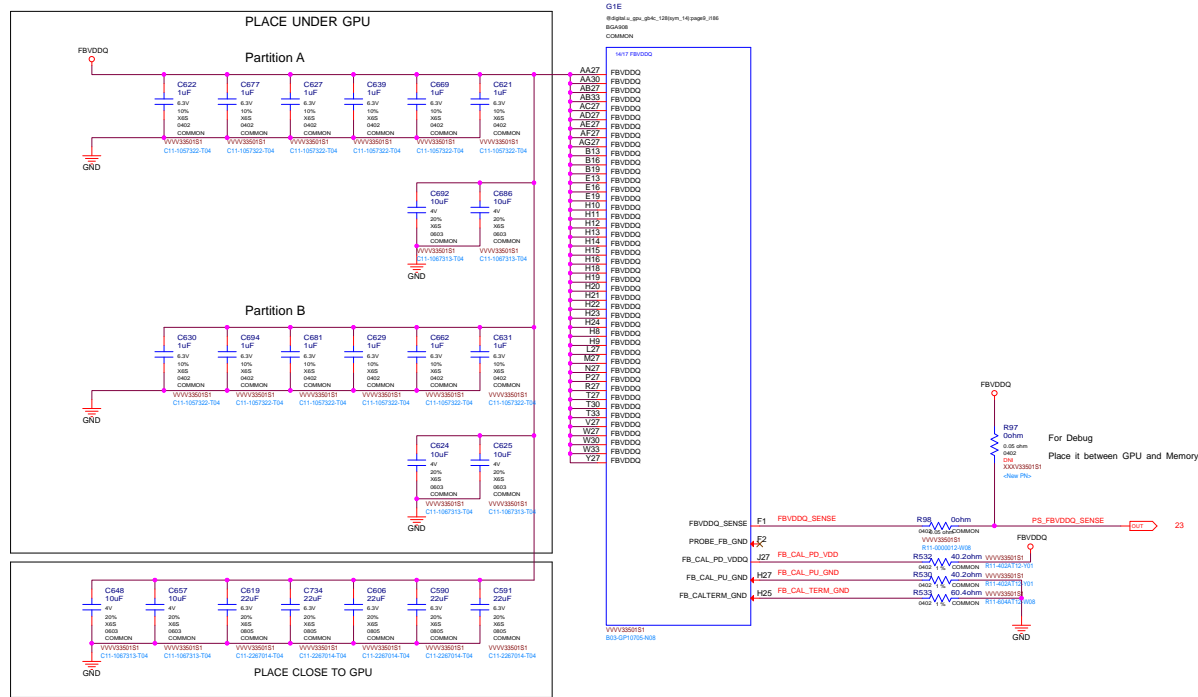
PLACE Around DRAM



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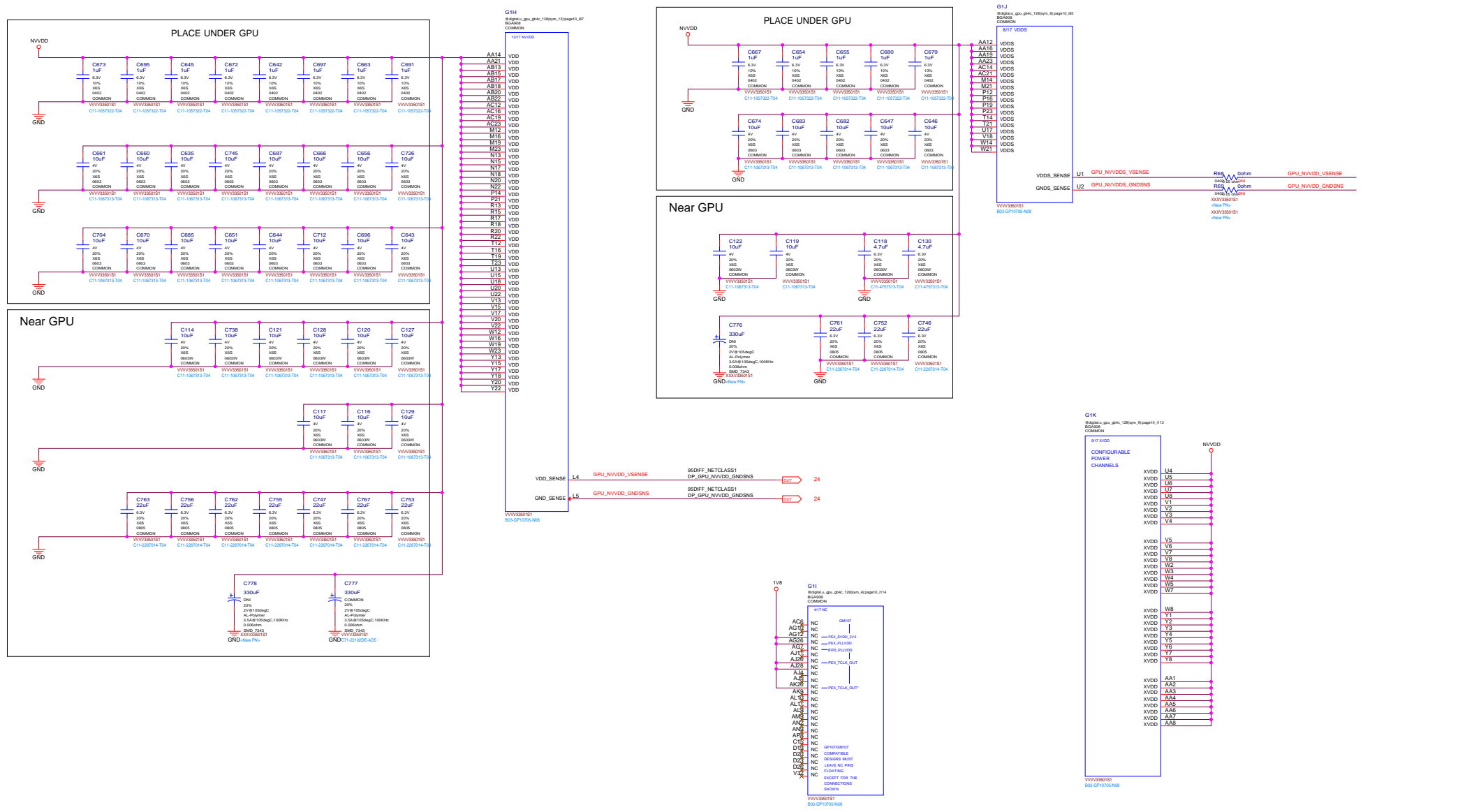
## GPU FBVDDQ & 1V8 Decoupling



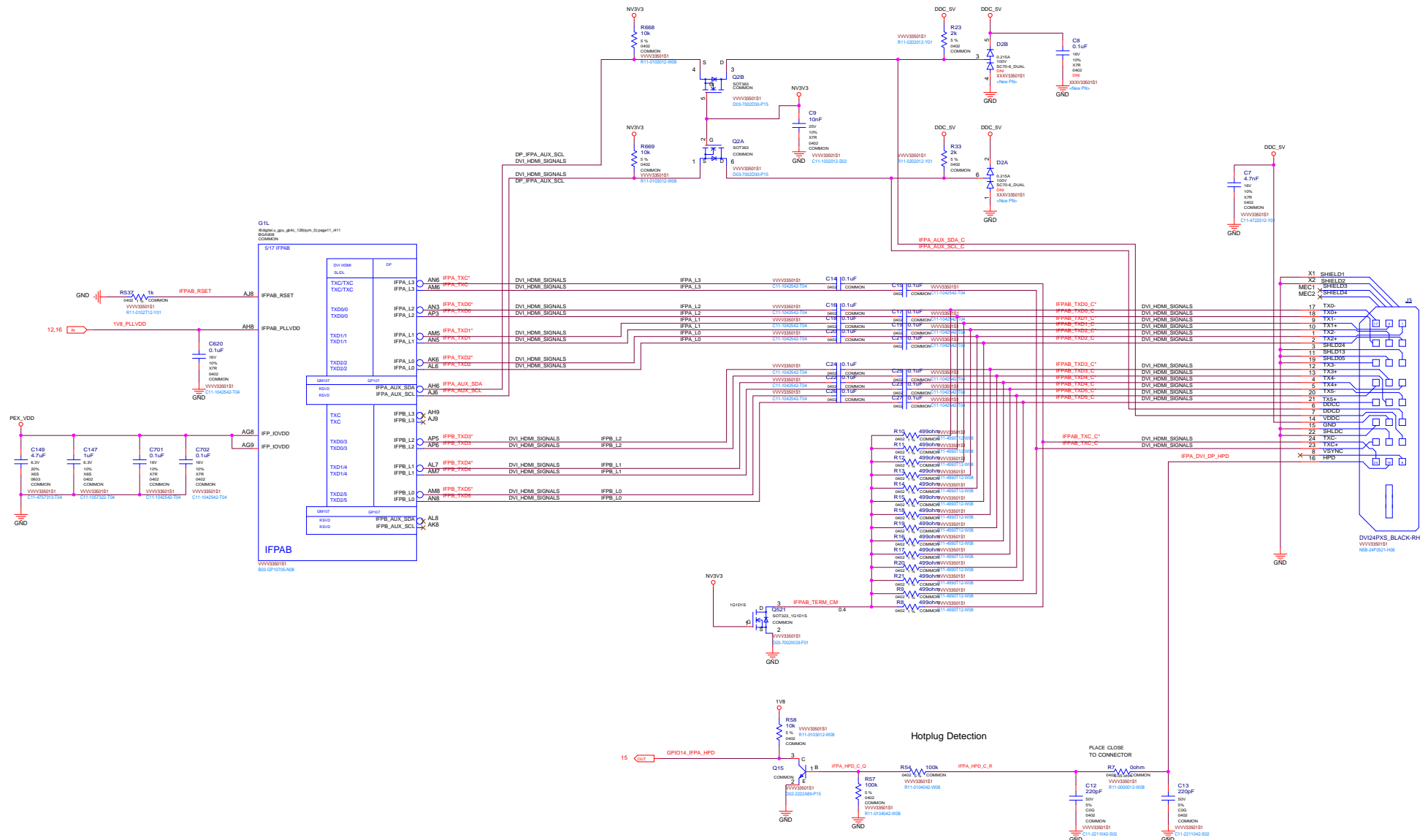
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GPU NVVDD & NVVDDS Decoupling



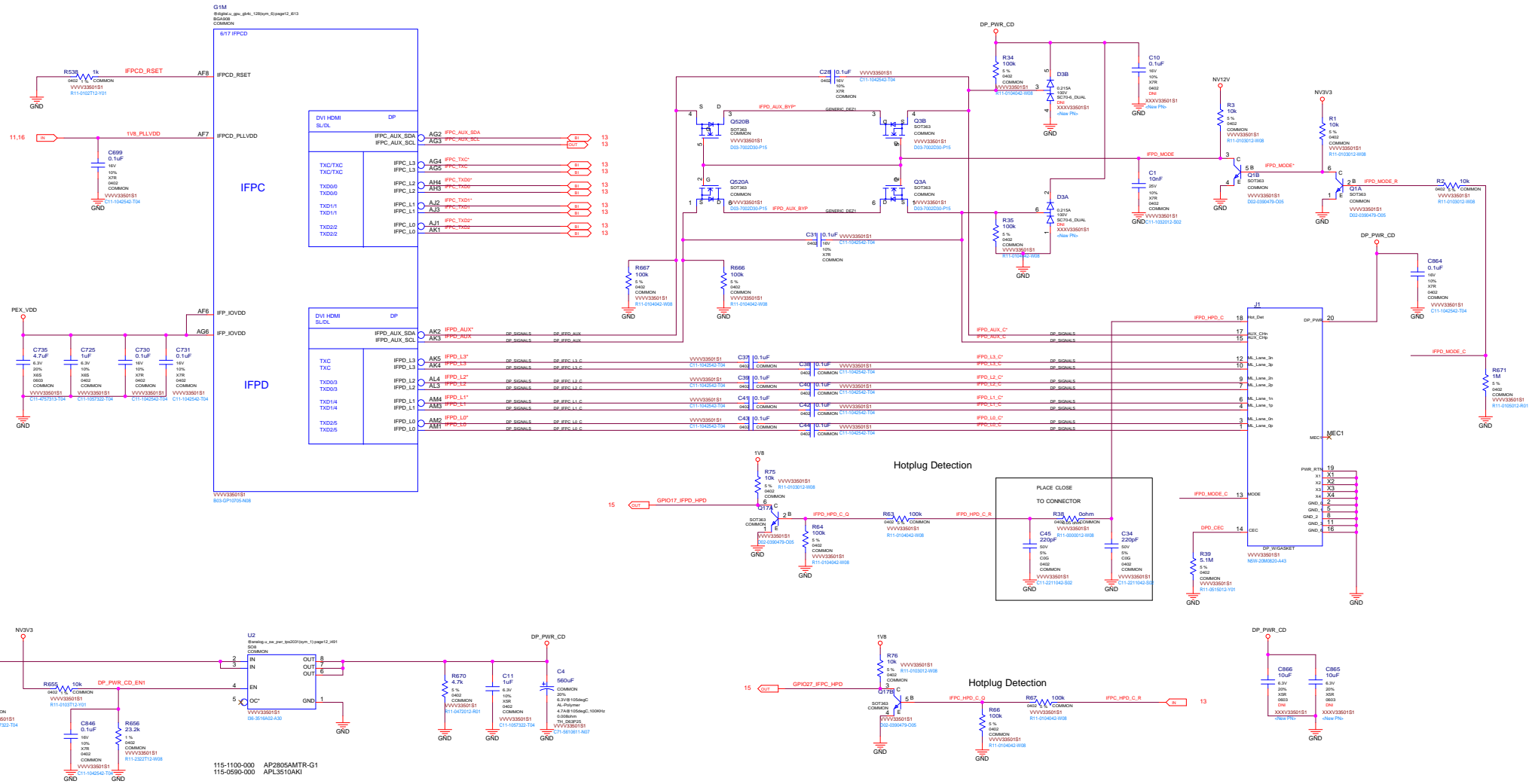
## IFPAB DVI-DL



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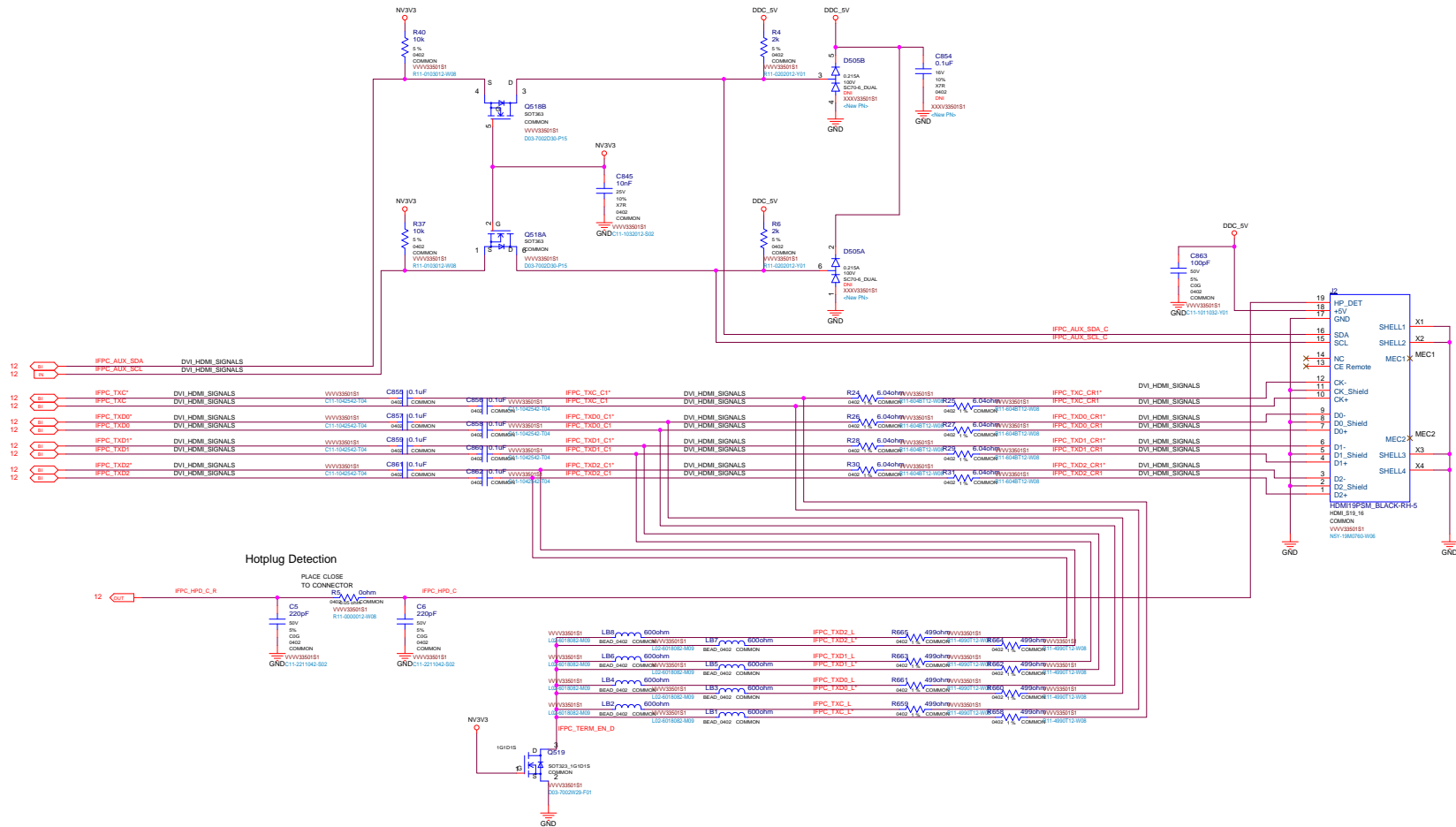
## IFPD DP



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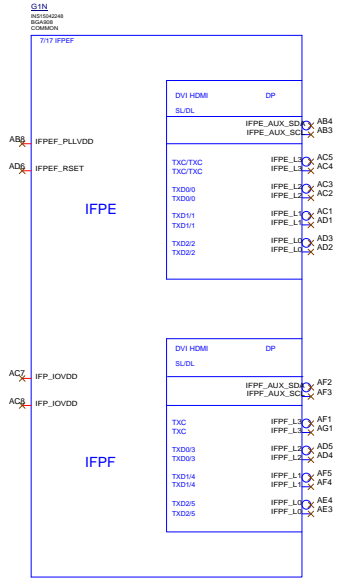
## IFPC HDMI



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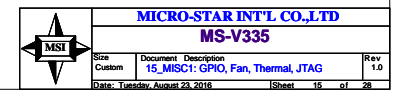
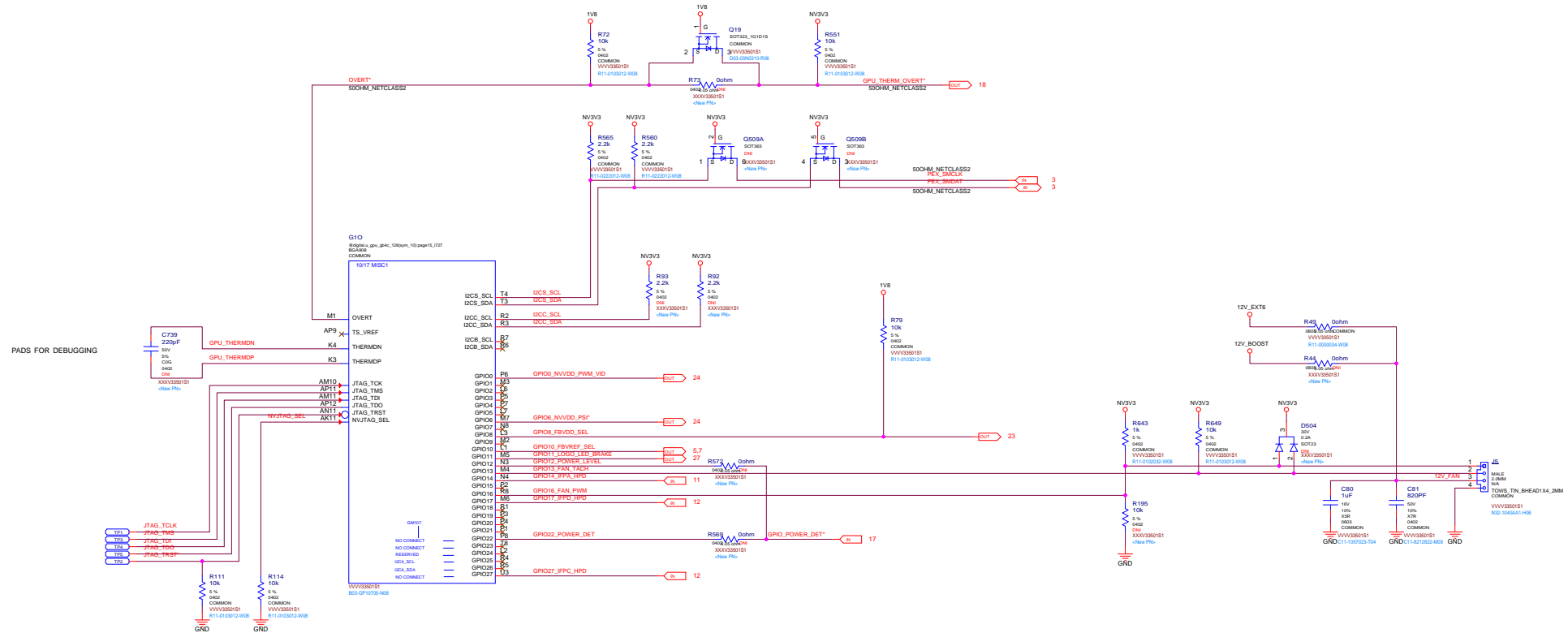
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IFPEF UNUSED



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Site Custom	Document Description 14_IFPEF UNUSED	Rev 1.0
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MISC1: GPIO, Fan, Thermal, JTAG



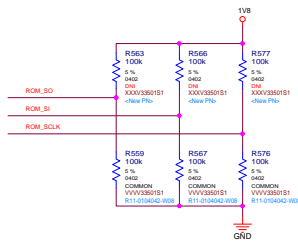
## MISC2: ROM, XTAL, Straps

ROM\_SO ROM\_SI ROM\_SCLK SOR\_EXPOSED[3:0] 1:ENABLE 0:DISABLE

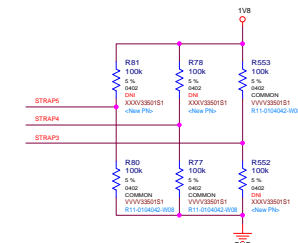
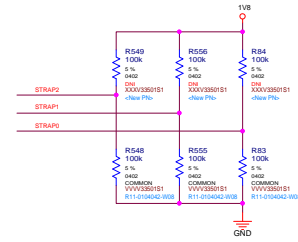
L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

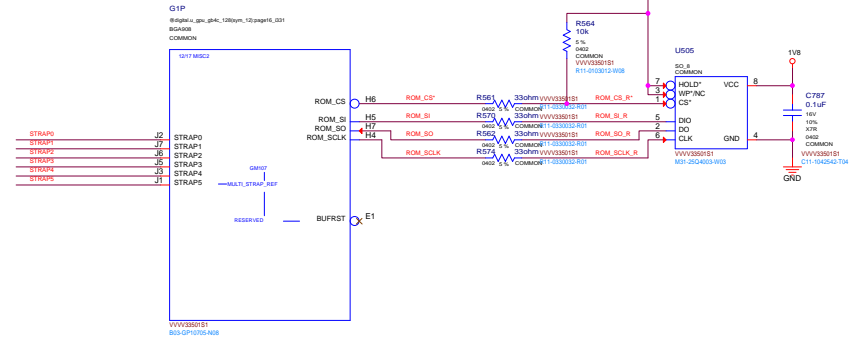
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0



H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

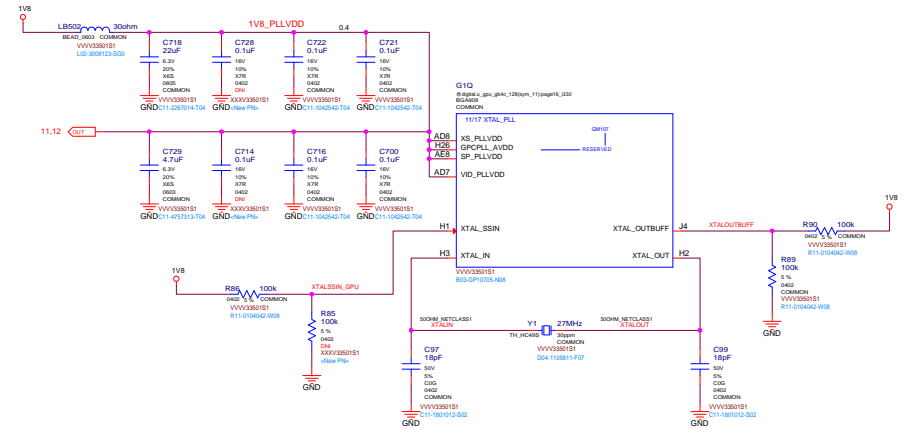


1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



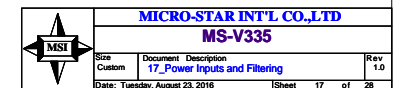
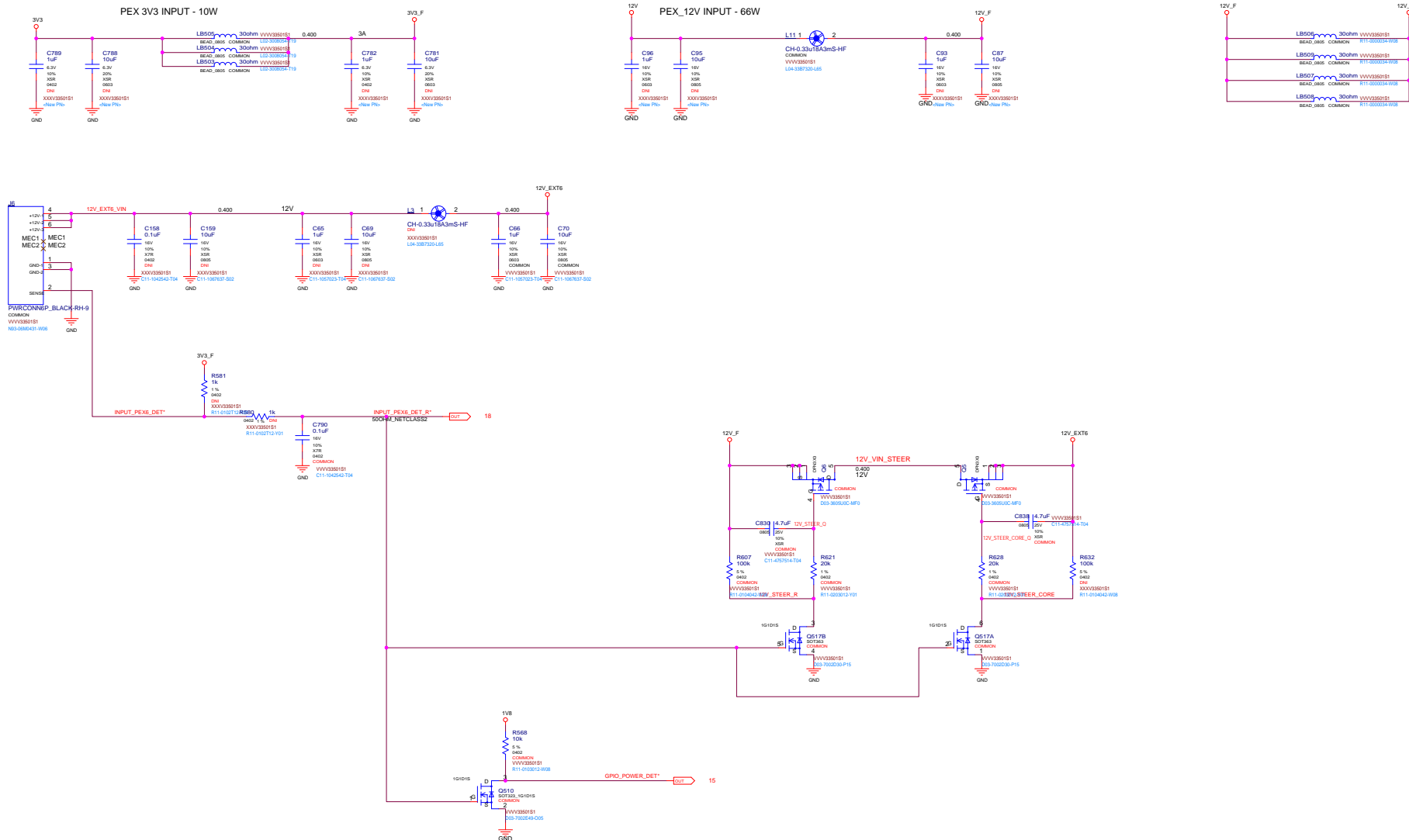
## Smart Fan

XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM

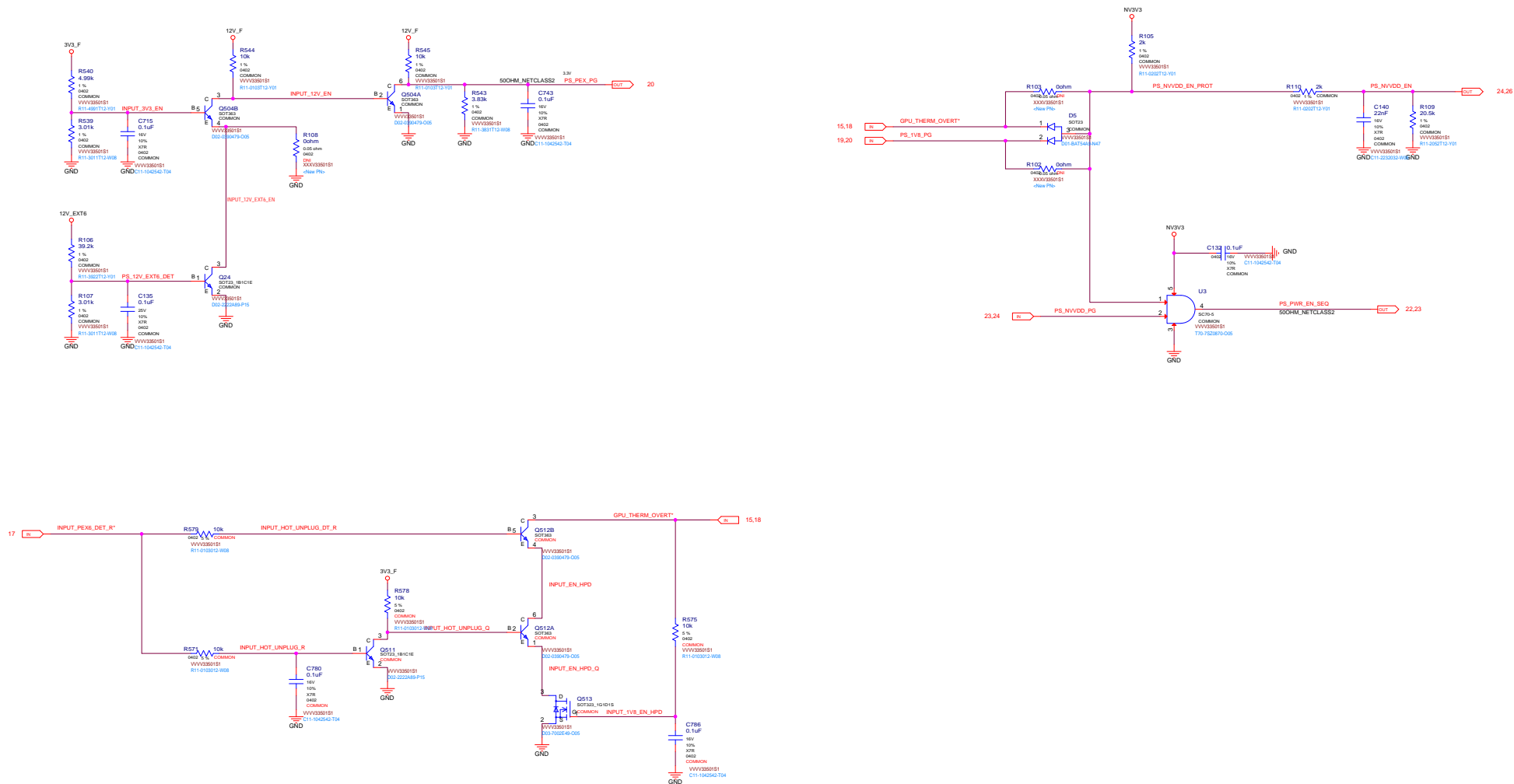




## Power Inputs and Filtering



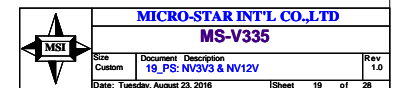
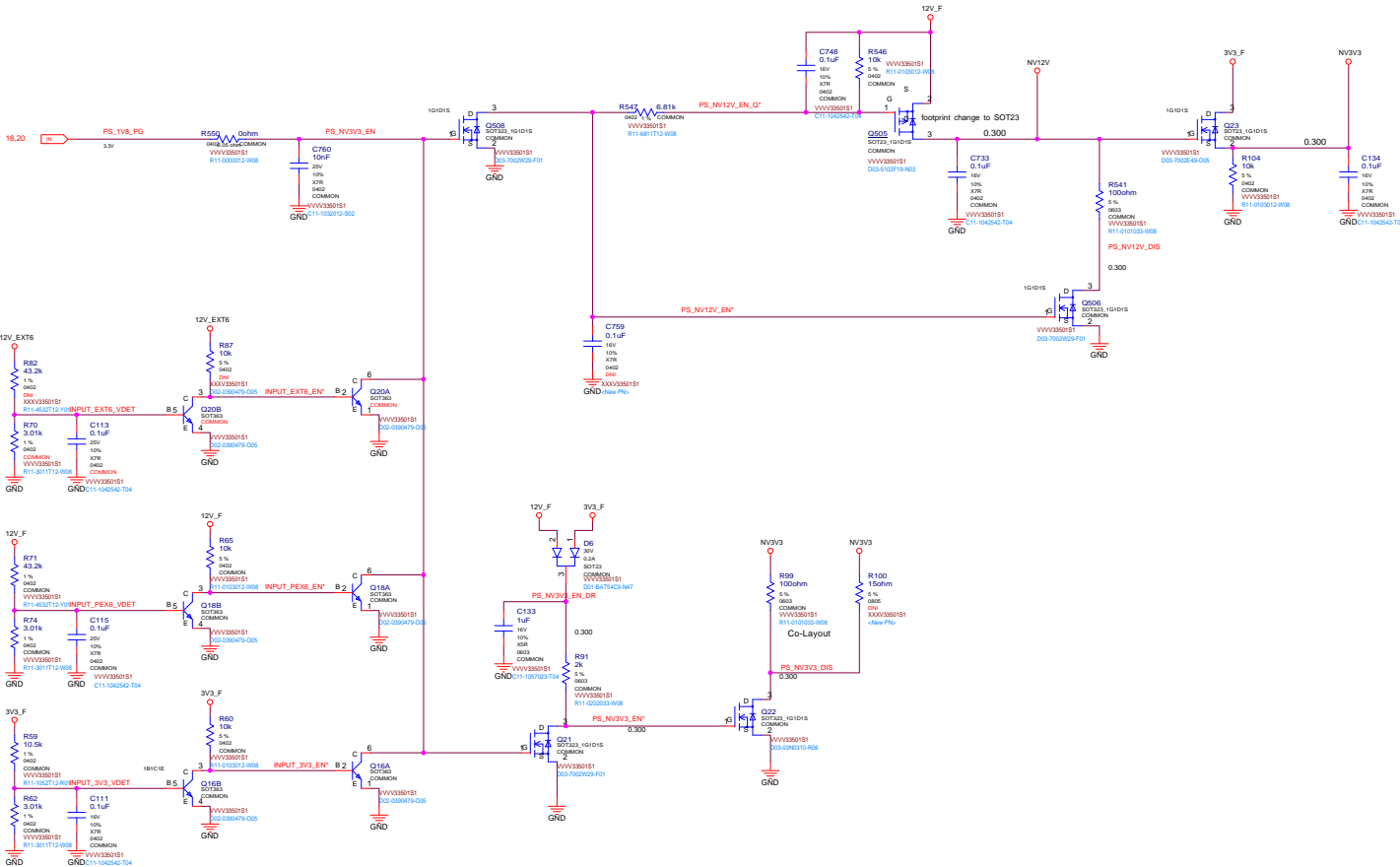
## Power sequence



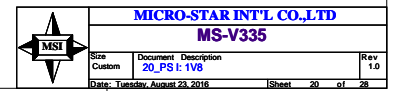
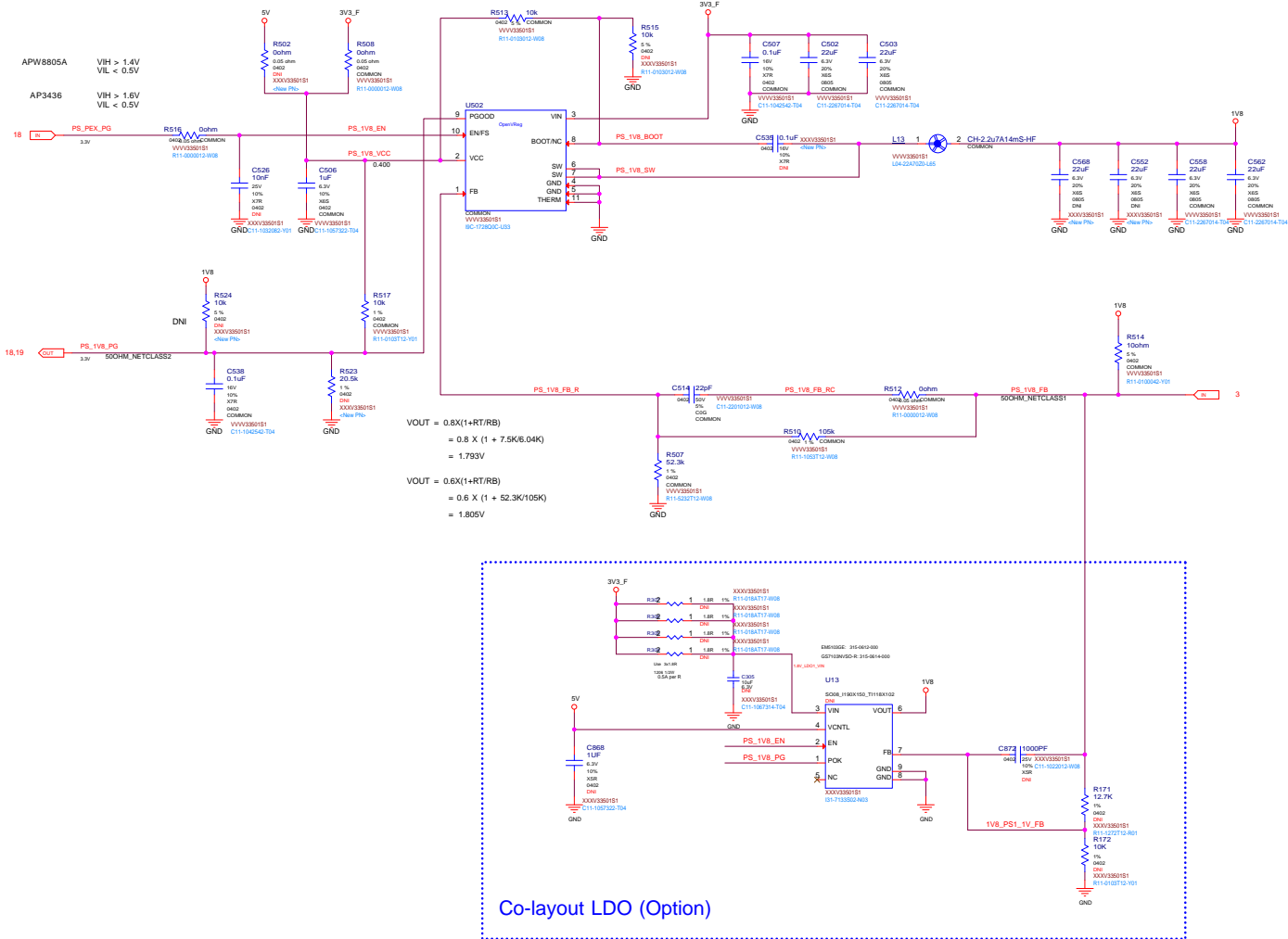
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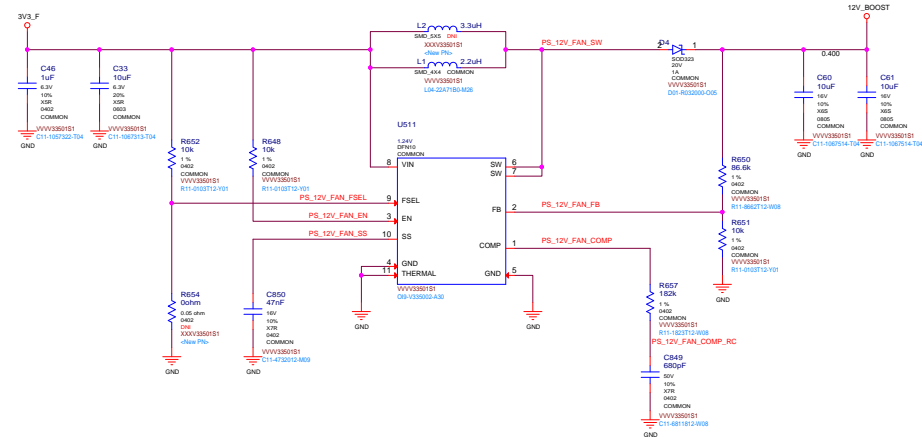
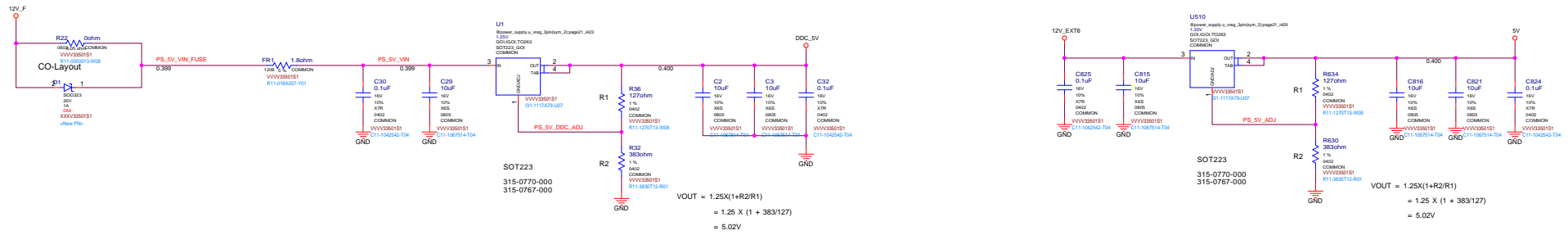
PS: NV3V3 & NV12V



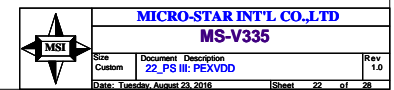
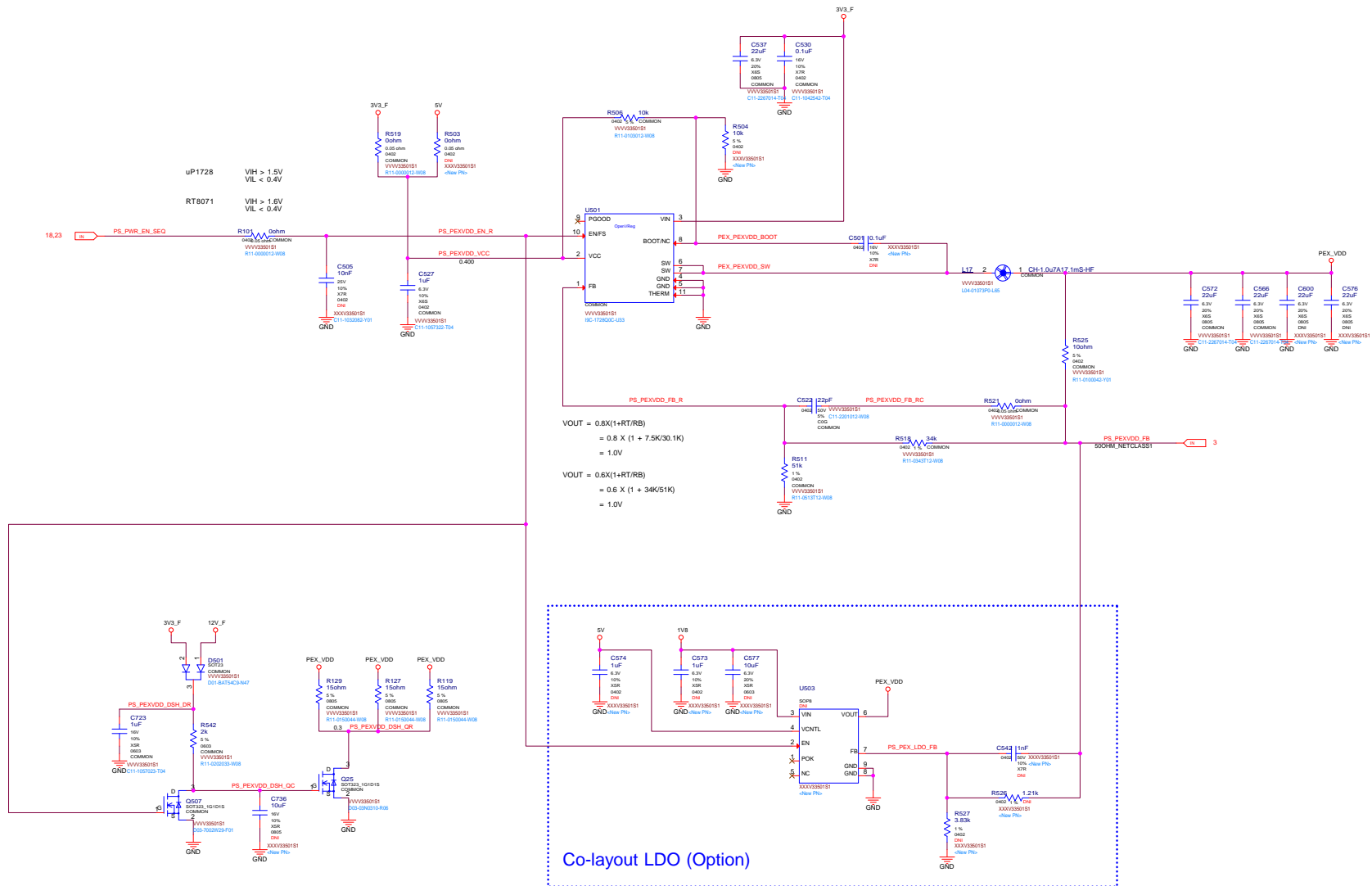
PS I: 1V8



## PSII:5V &amp; 12V\_FAN



## PS III: PEXVDD



## PS IV: FBVDDQ

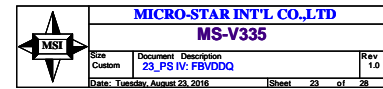
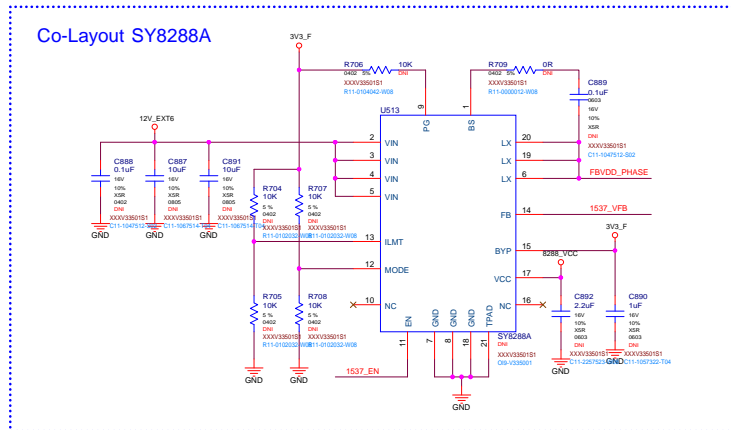
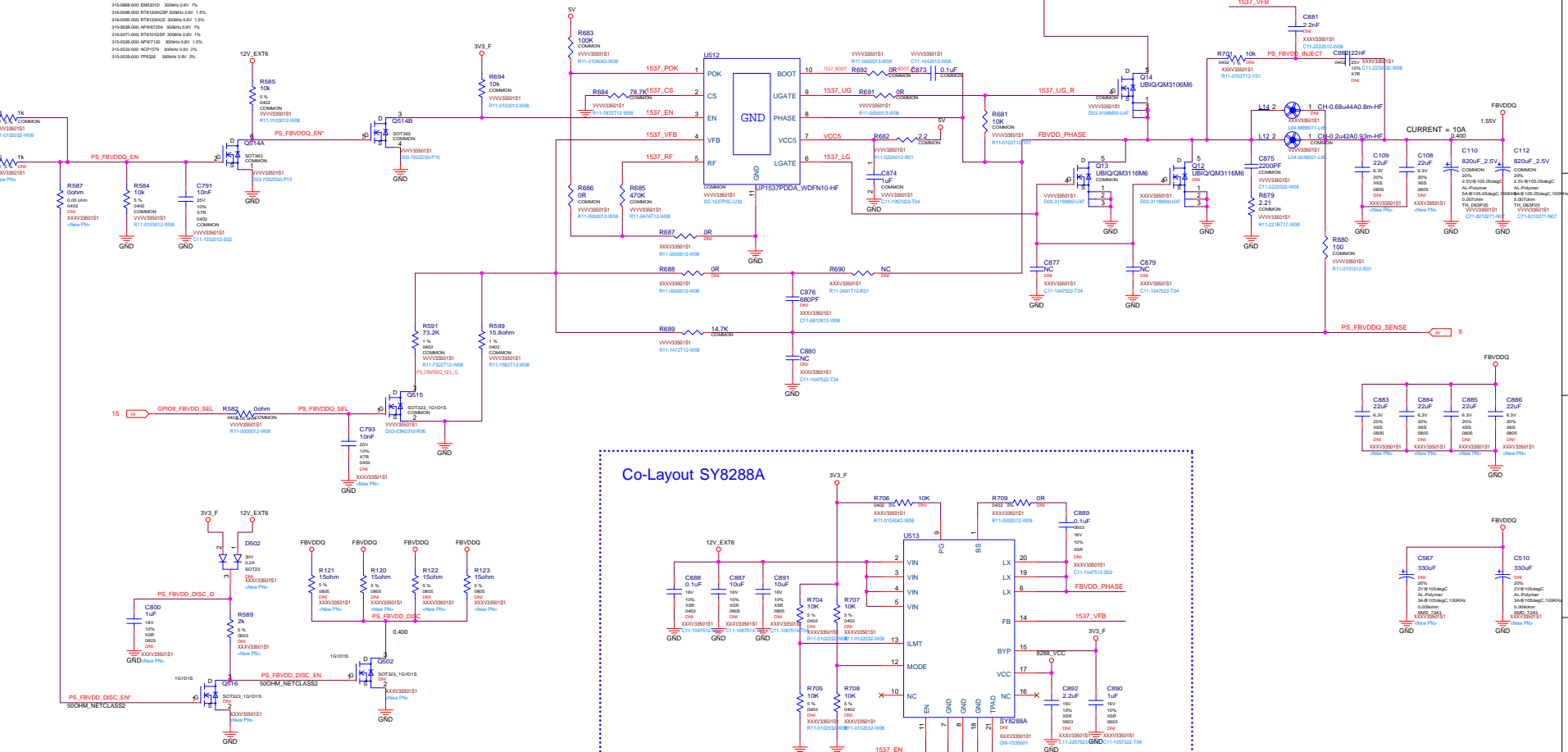
FBVDDQ_CTL	FBVDDQ	Non-DVS
X	1.5V	<= DEFAULT

FBVDDQ_CTL	FBVDDQ	For DVS
0	1.35V	
1	1.5V/1.55V	<= DEFAULT

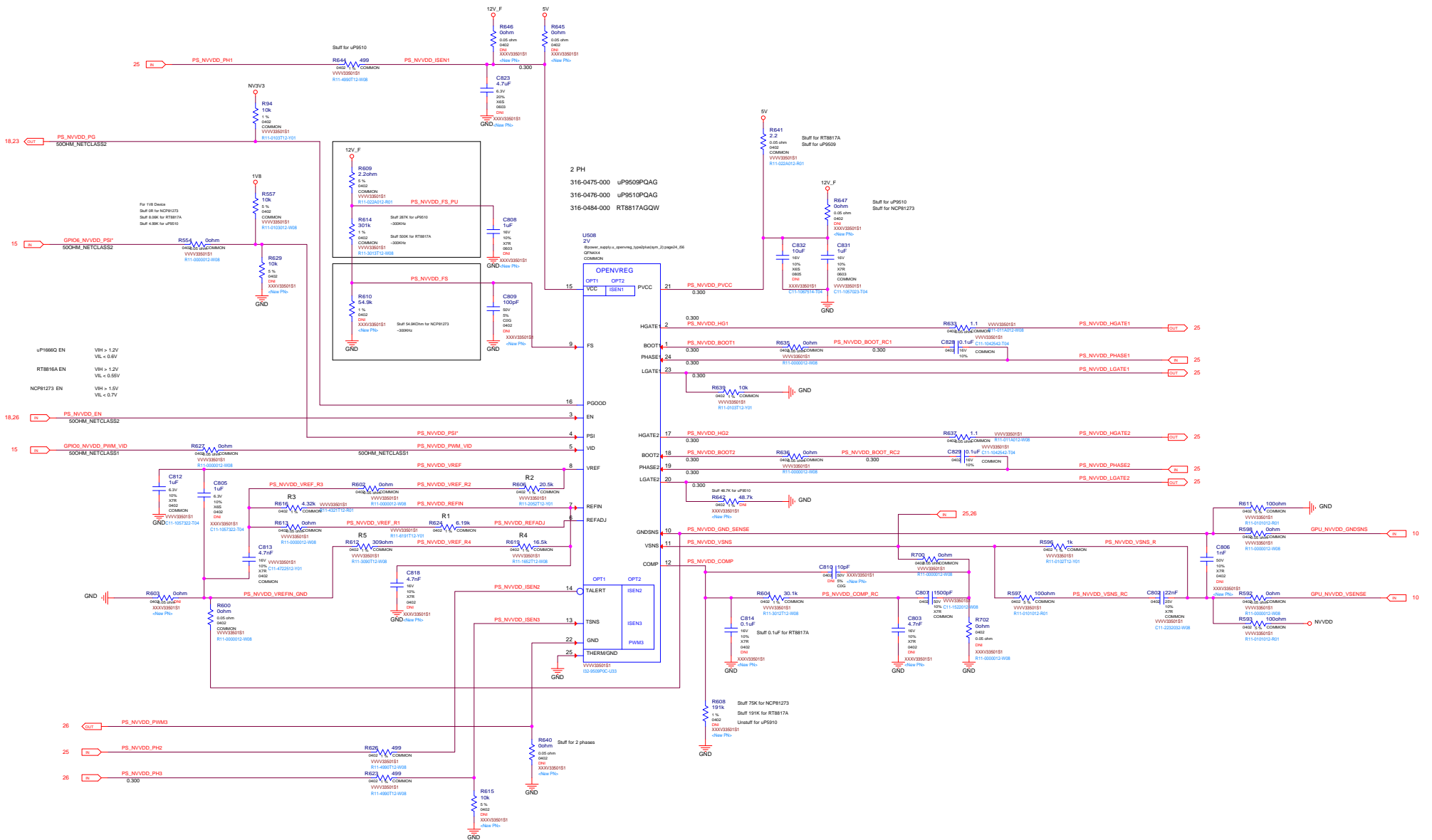
	$V_{out} = V_{ref} * (1 + 0.025)$
$V_{ref} = 0.6V$ :	$1.50V = 0.6V * (1 + 0.665)$ $1.55V = 0.6V * (1 + 0.634)$
$V_{ref} = 0.8V$ :	$1.50V = 0.8V * (1 + 0.875)$ $1.55V = 0.8V * (1 + 0.875)$

VOLT = VREF * (1+0.0025)	
Vref=0.5V:	$1.50V = 0.5V * (1+0.0025)$ $1.55V = 0.5V * (1+0.0025)$ $1.36V = 0.5V * (1+0.0025)$
Vref=0.8V:	$1.50V = 0.8V * (1+0.001438)$ $1.55V = 0.8V * (1+0.001438)$ $1.36V = 0.8V * (1+0.001438)$

	P5	Fonc	Vnel	Tot
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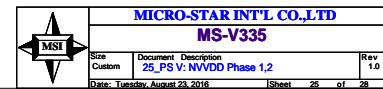
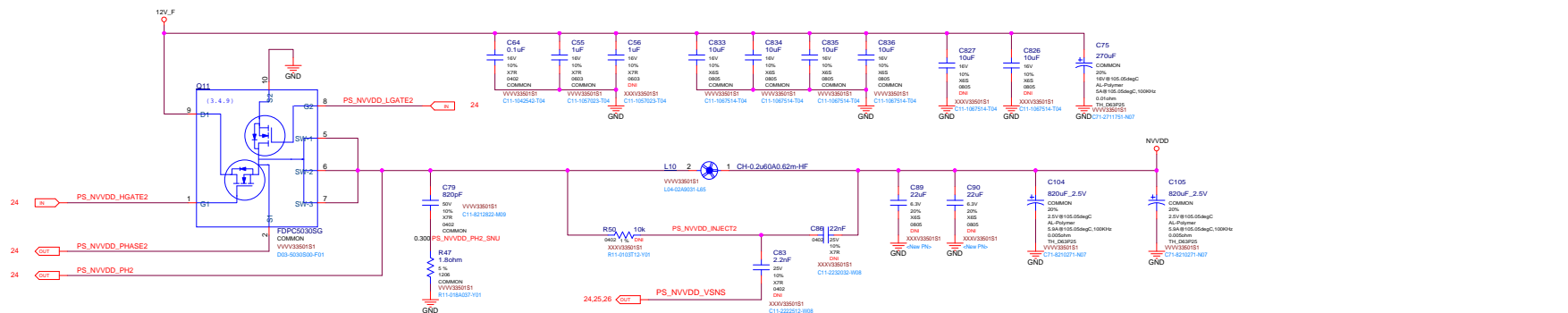
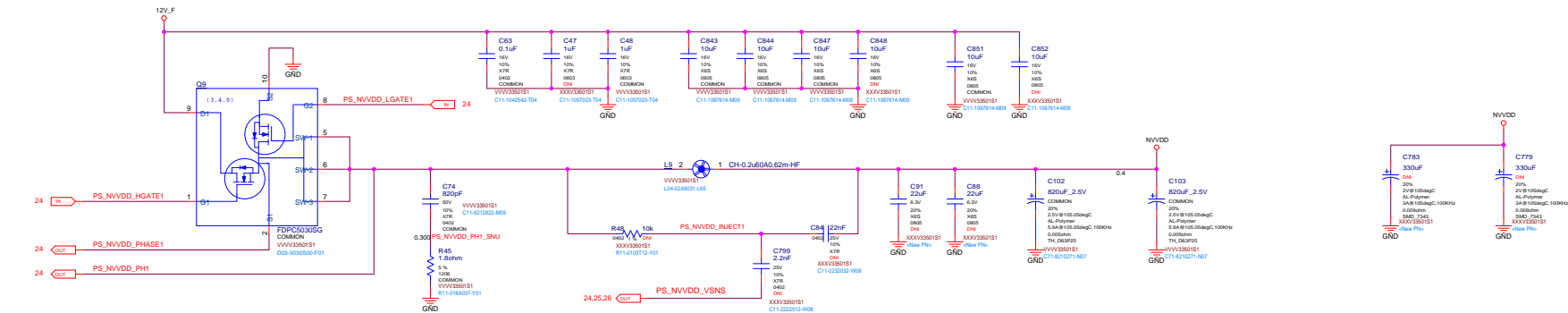
## PS V: NVVDD OVR2+1



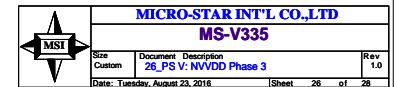
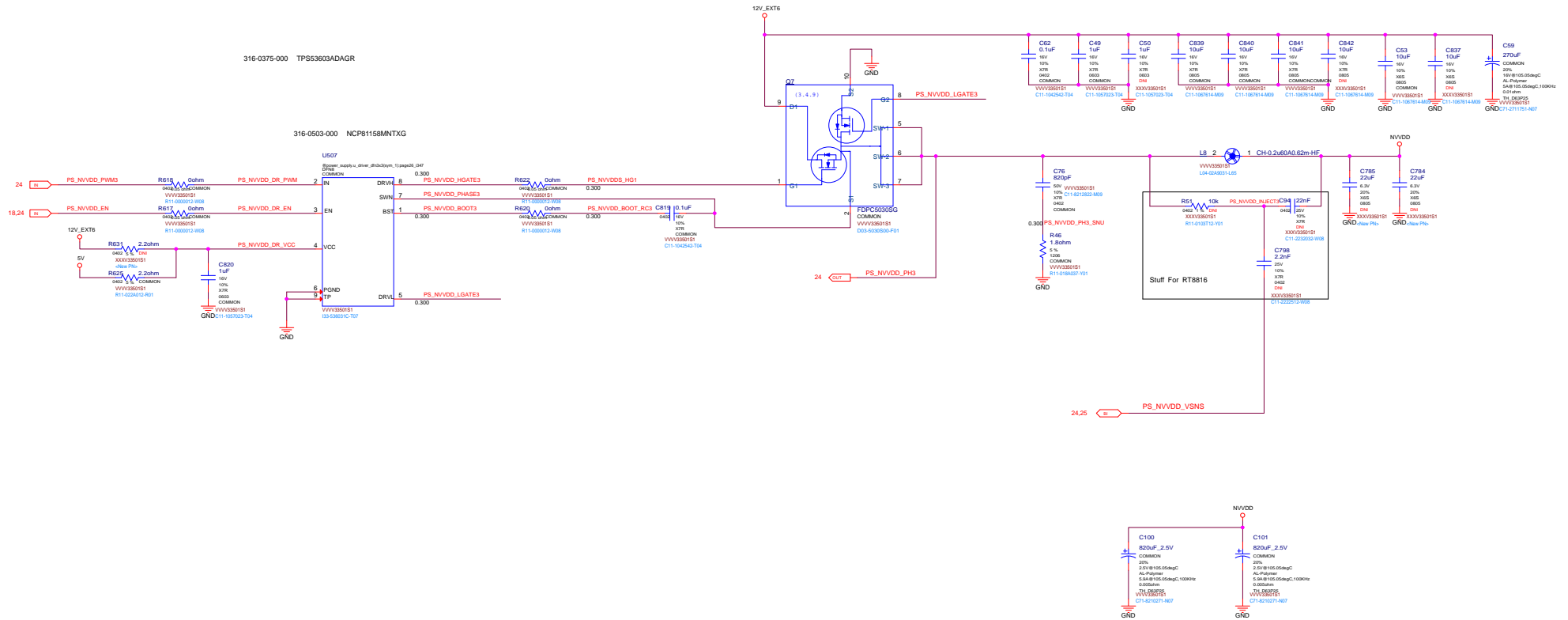
MICRO-STAR INT'L CO.,LTD			
MS-V335			
Doc No	Document Description	Rev	
24_PS V	24_PS V: NVDD OVR2+1	R0	
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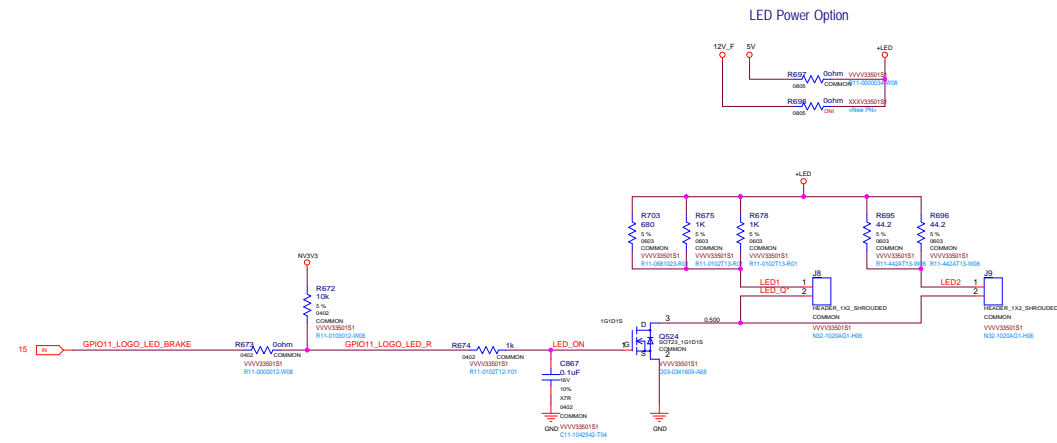
## PS V: NVVDD Phase 1,2



## PS V: NVVDD Phase 3



Logo LED



Mechanical: Bracket/Thermal Solution

Brackets:

