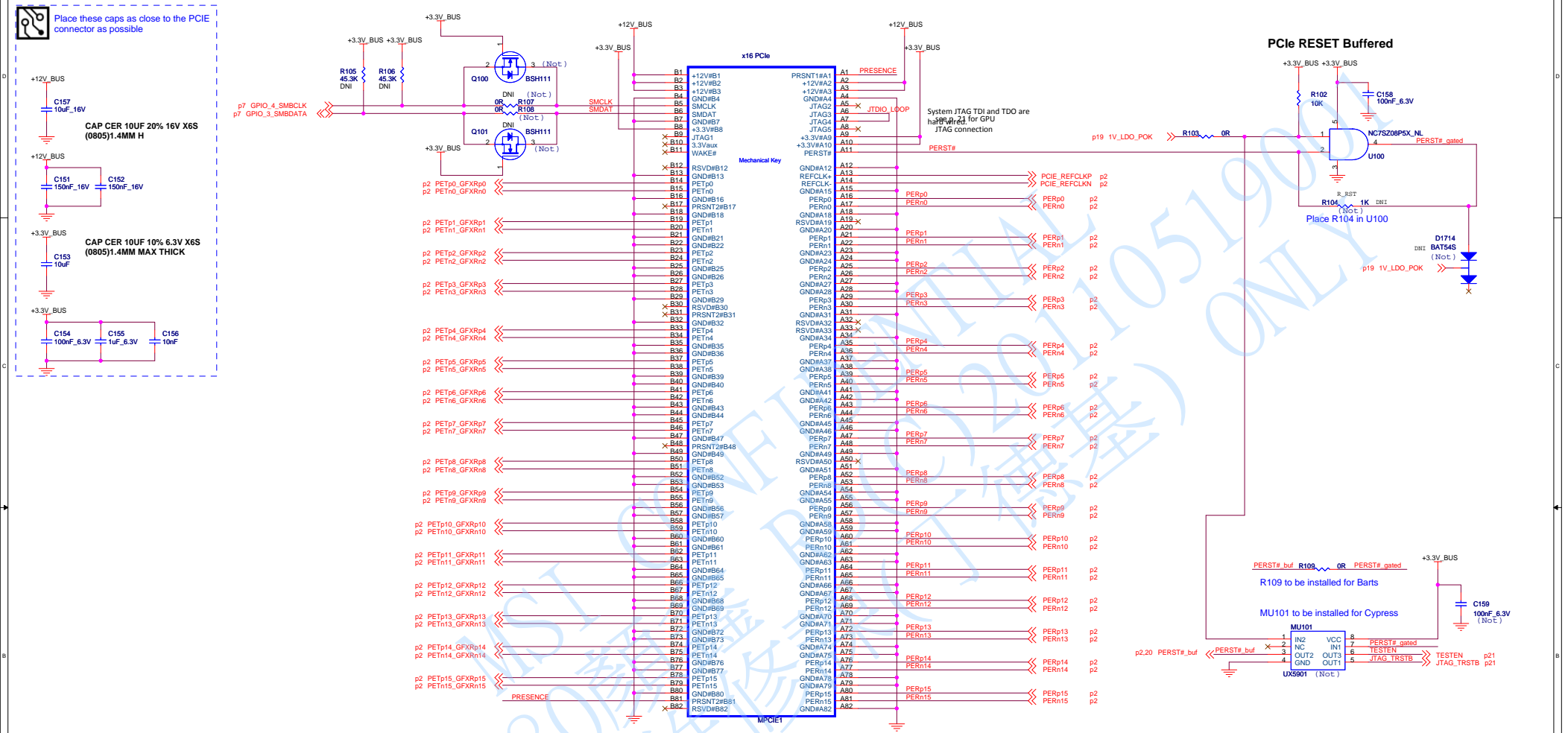
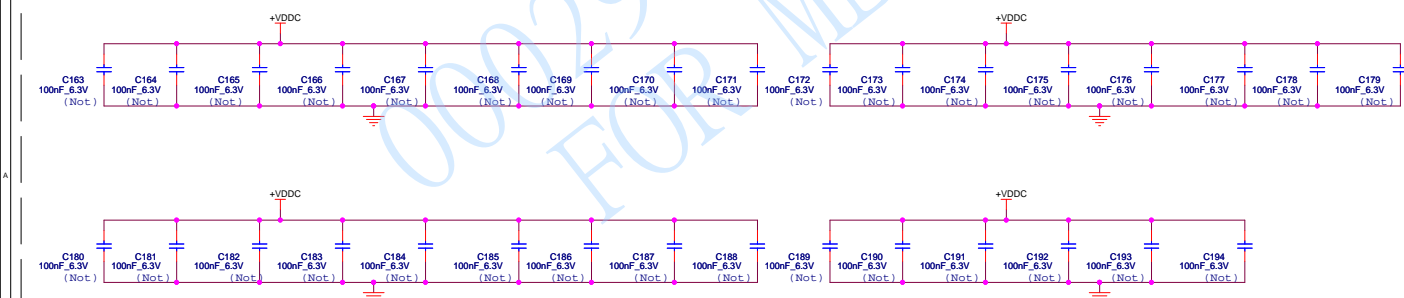




PCI-EXPRESS EDGE CONNECTOR



PCIe stitching caps: To be placed close to the PCIe diff pair routed on Layer 6 at the PCIe slot



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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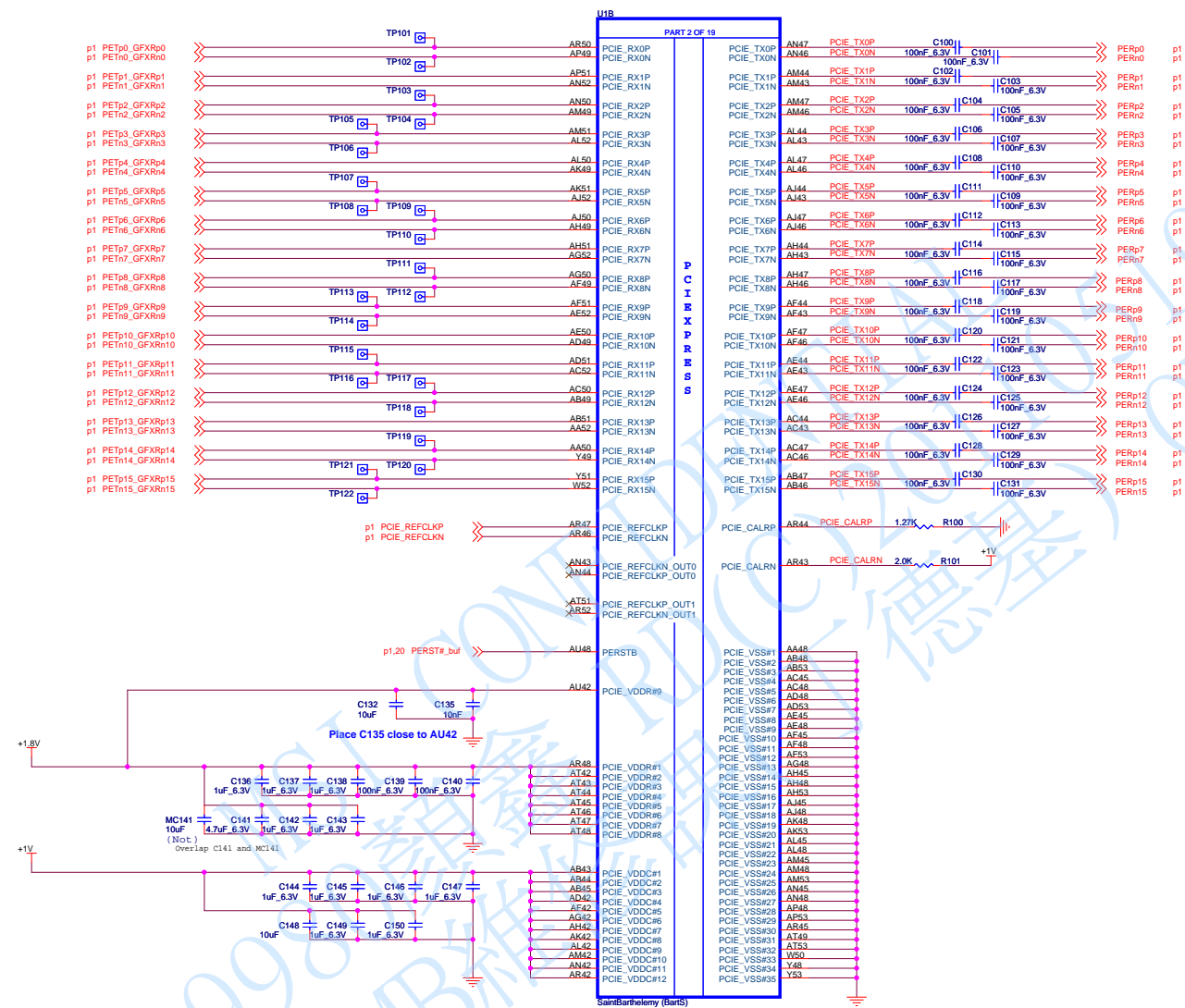
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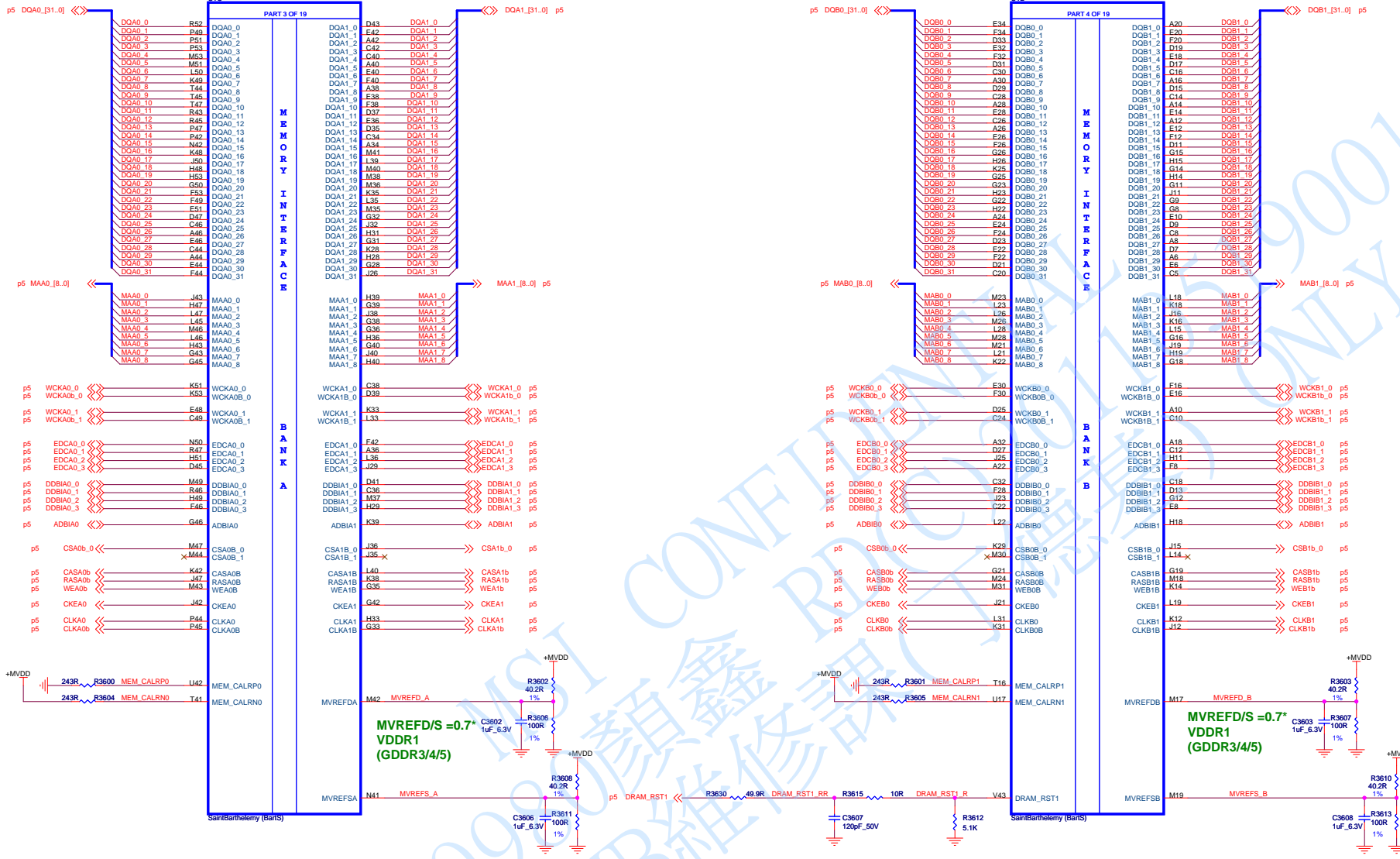
Date: Thursday, October 14, 2010	Rev 3
Sheet 1 of 23	

(2) BARTS/ CYPRESS PCIE Interface

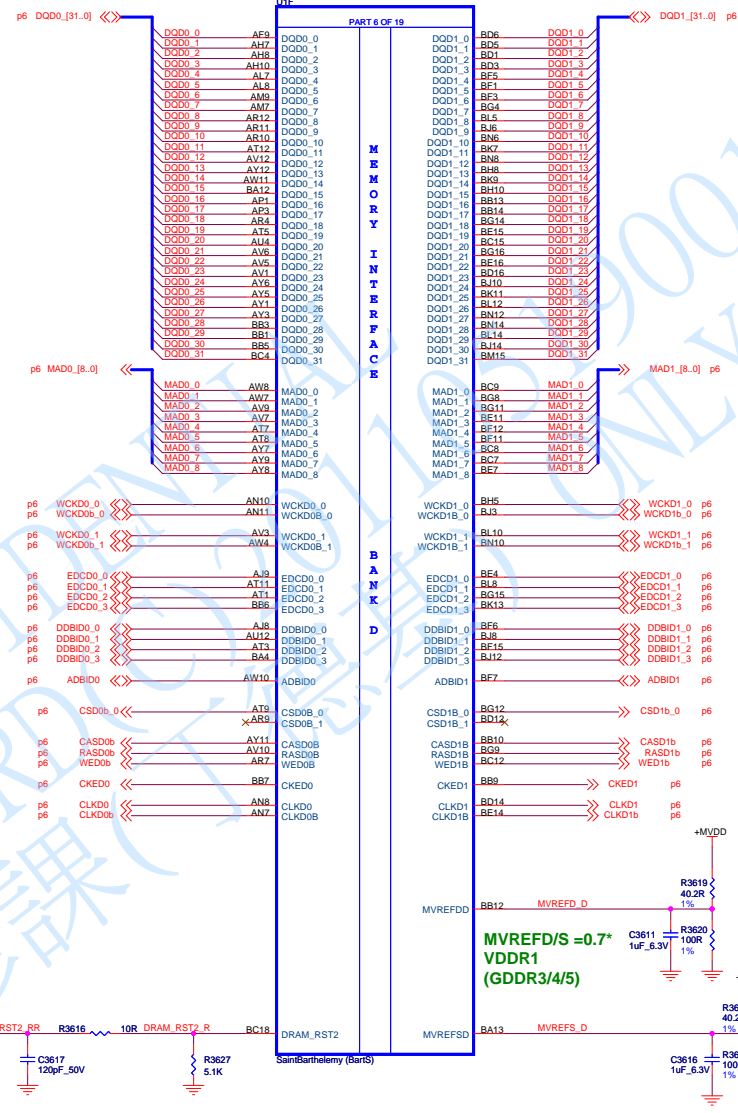
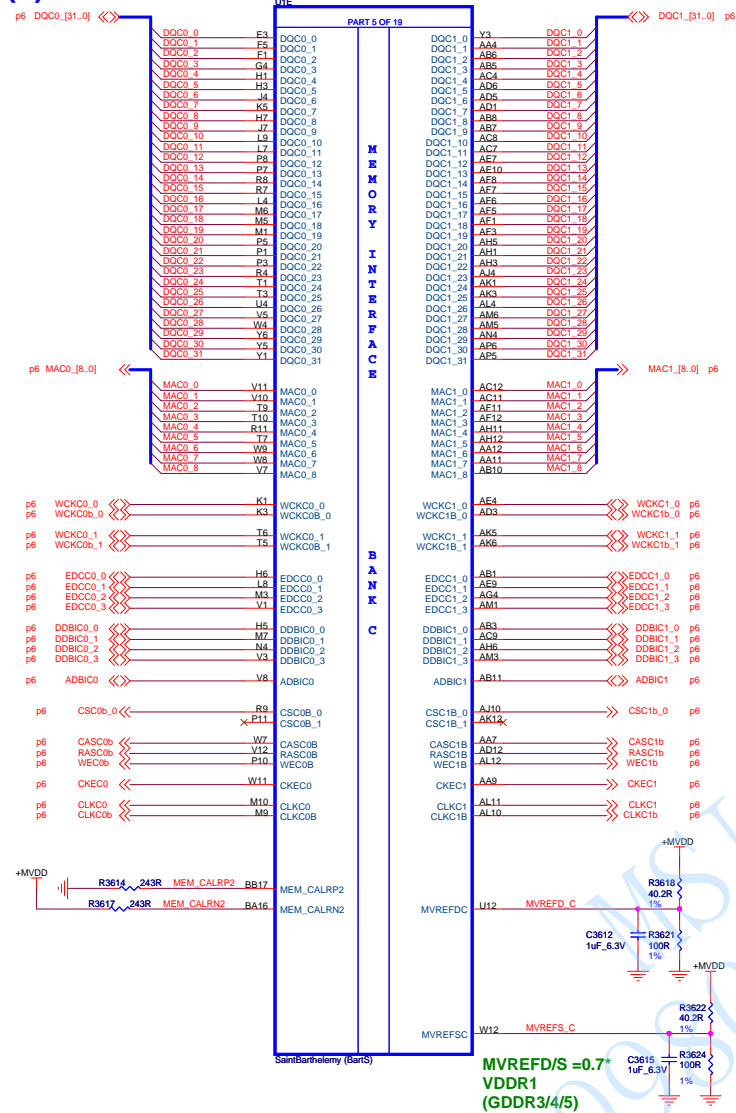
NOTE: Some of the PCIE testpoints will be available through vias on traces.



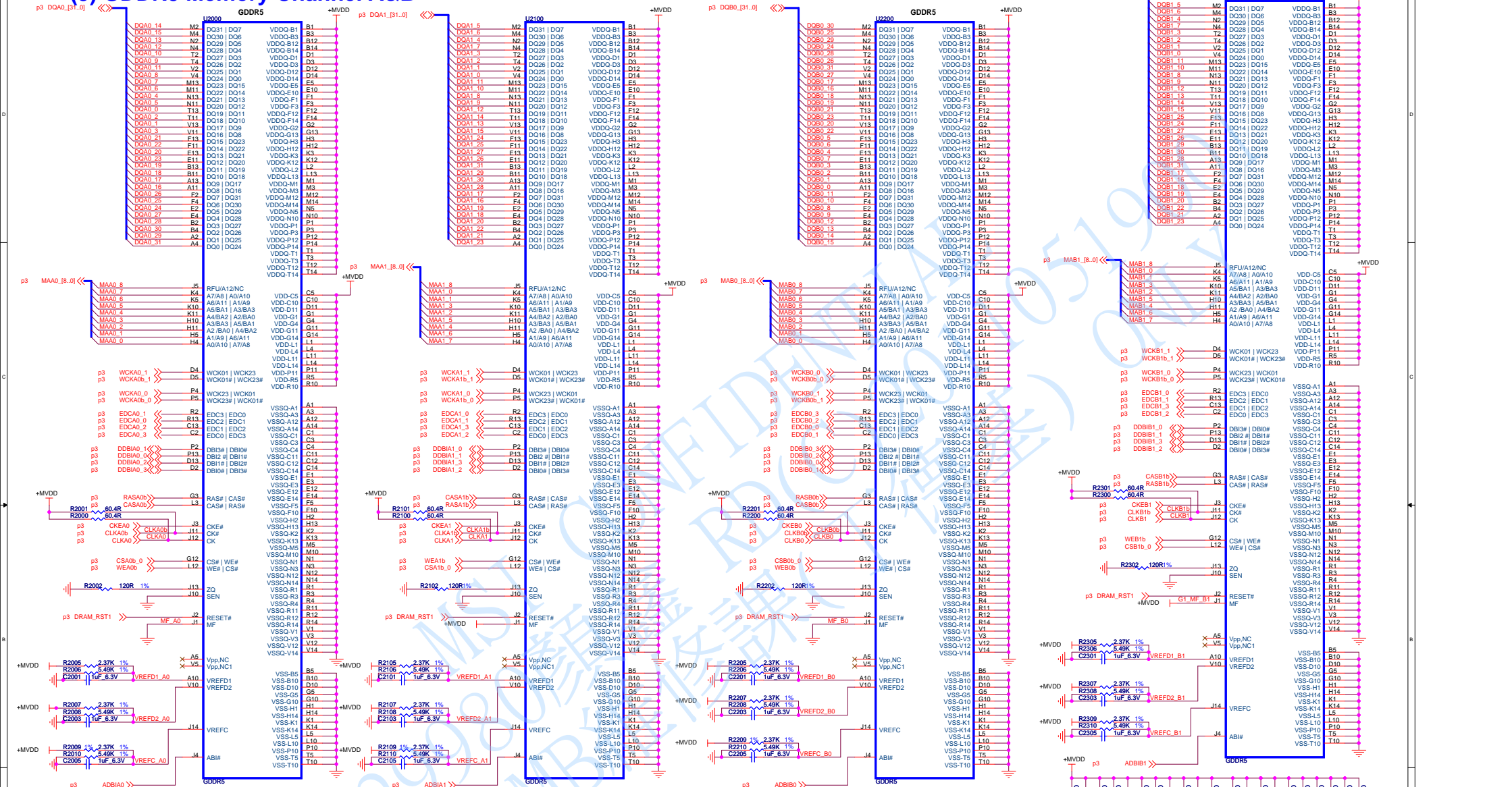
(3) BARTS / CYPRESS MEM Interface Ch A&B



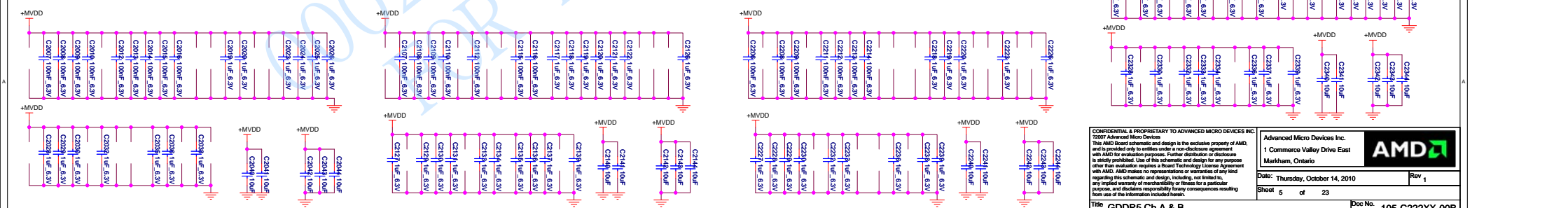
(4) BARTS / CYPRESS MEM Interface Ch C&D



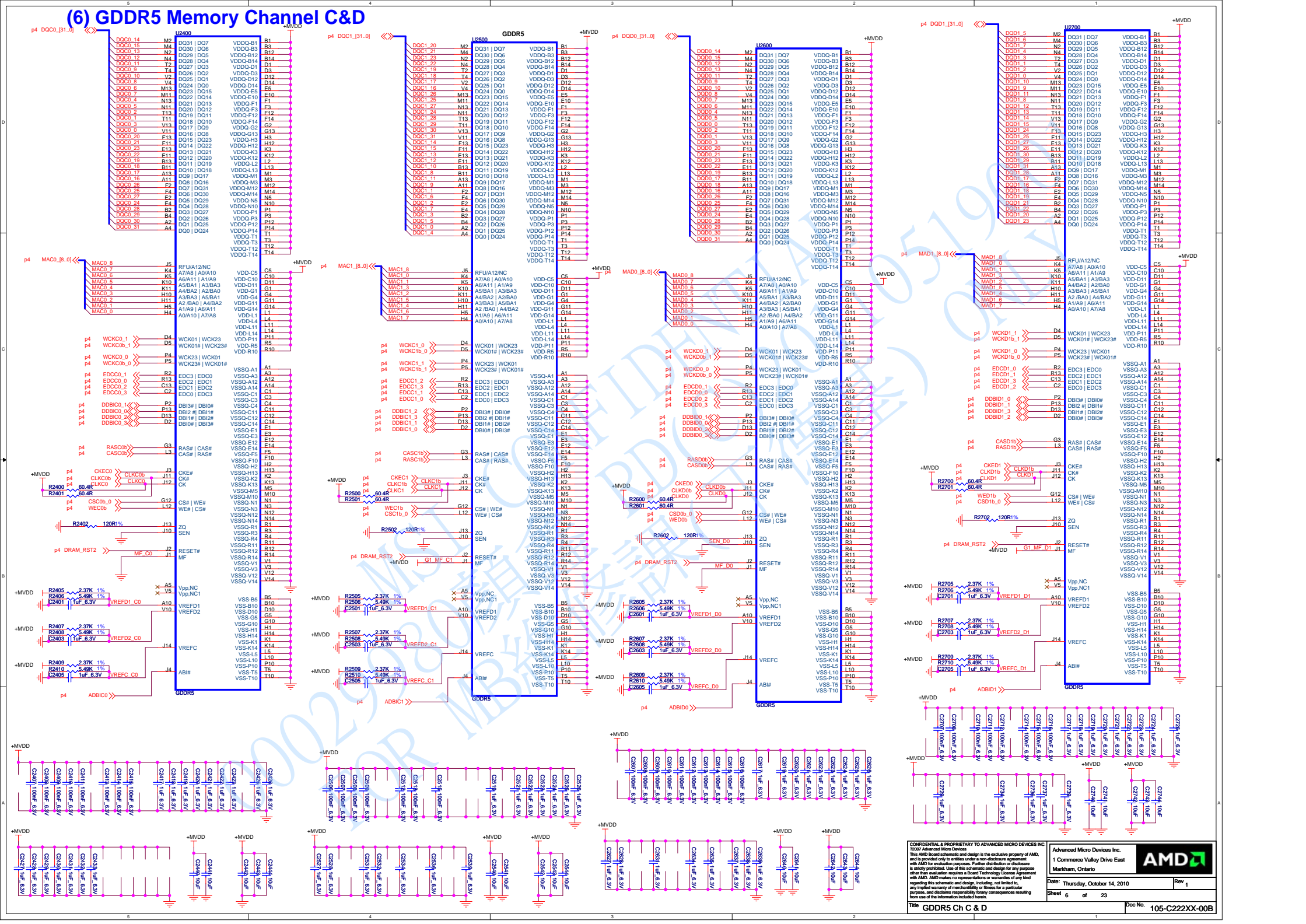
(5) GDDR5 Memory Channel A&B



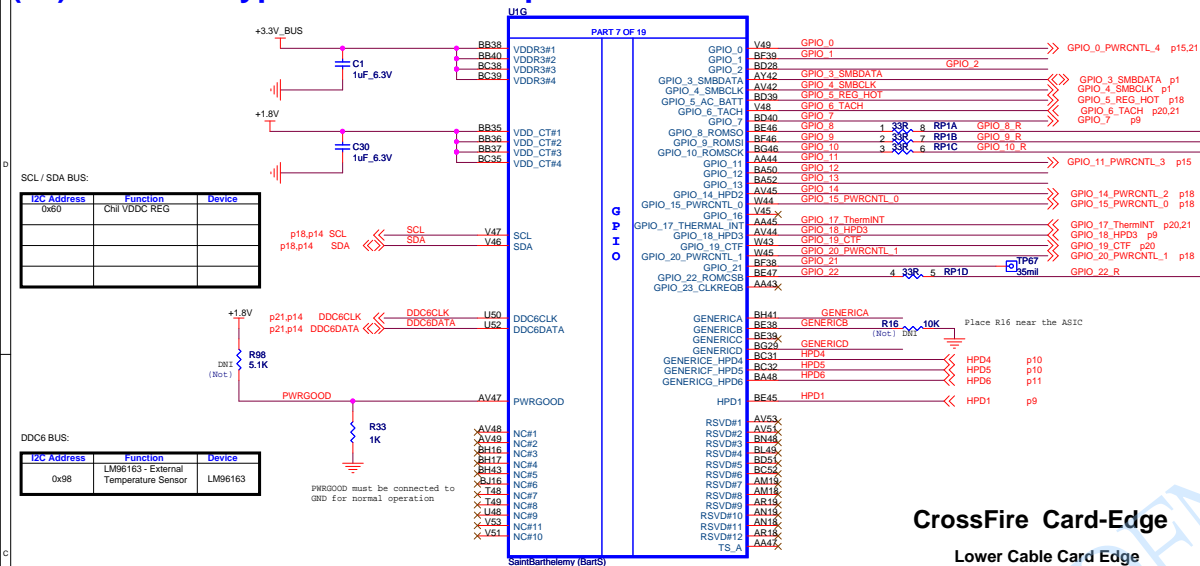
Use internal Vref memory voltage



(6) GDDR5 Memory Channel C&D

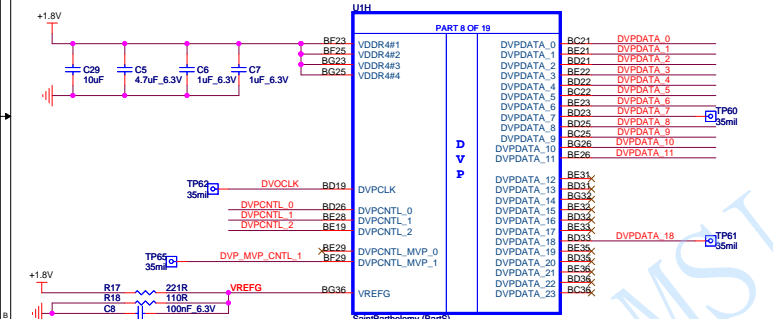
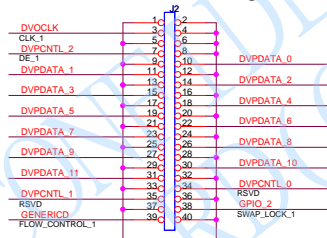



(07) BARTS / Cypress GPIOs Strap CF XTAL OSC




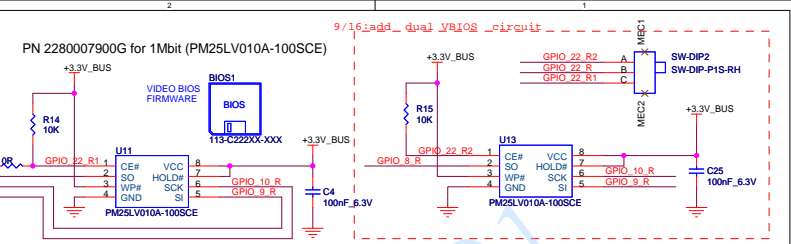
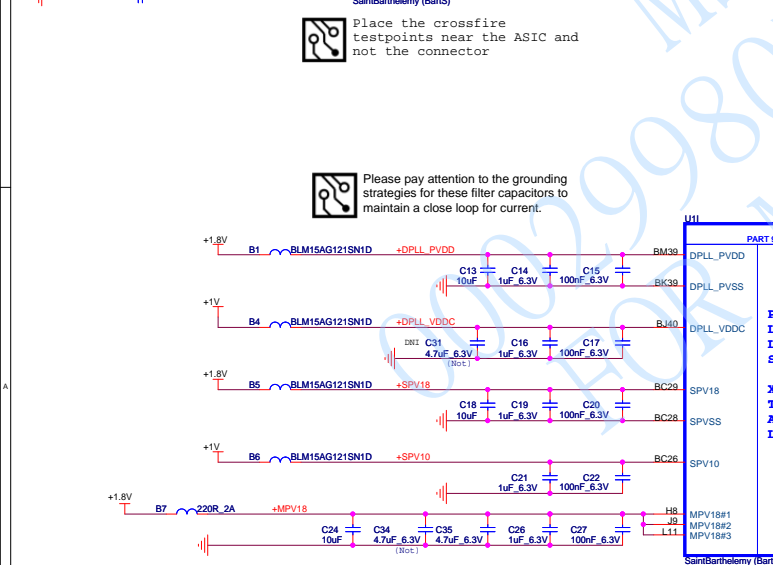
CrossFire Card-Edge

Lower Cable Card Edge

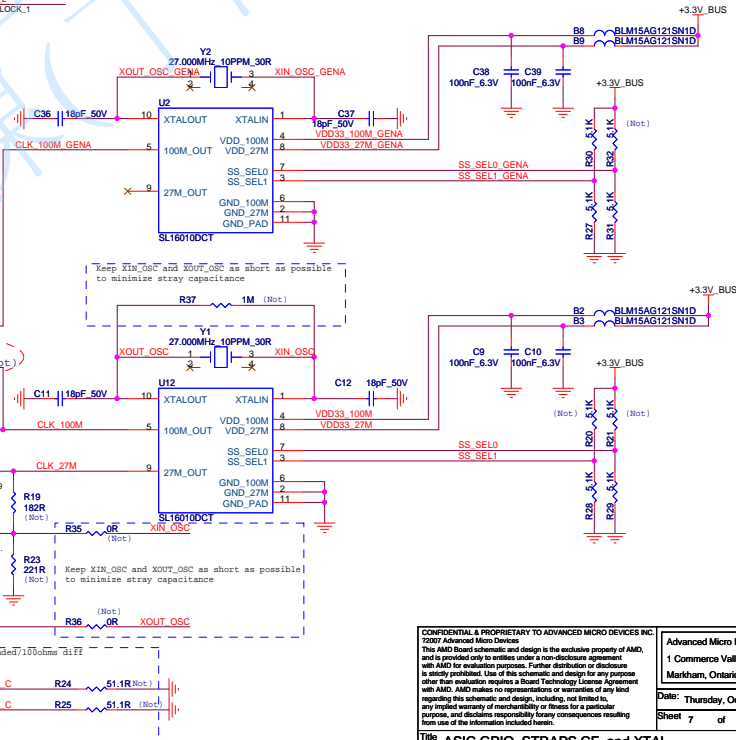
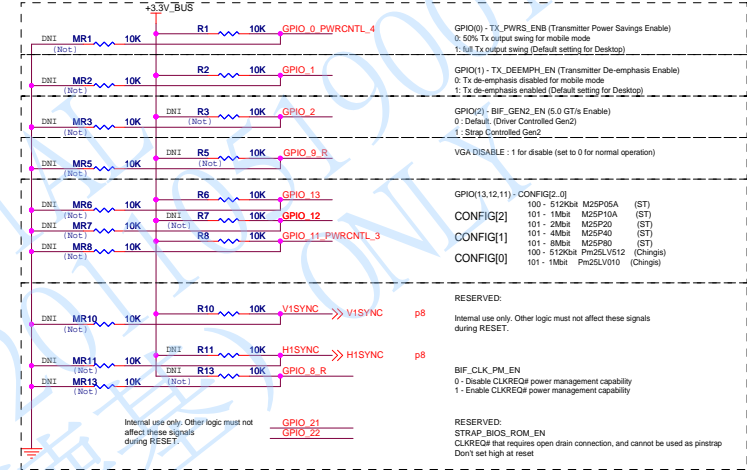


 Place the crossfire testpoints near the ASIC and not the connector

 Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.



PIN BASED STRAPS



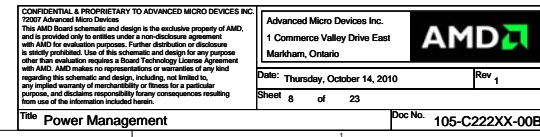
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Title _____

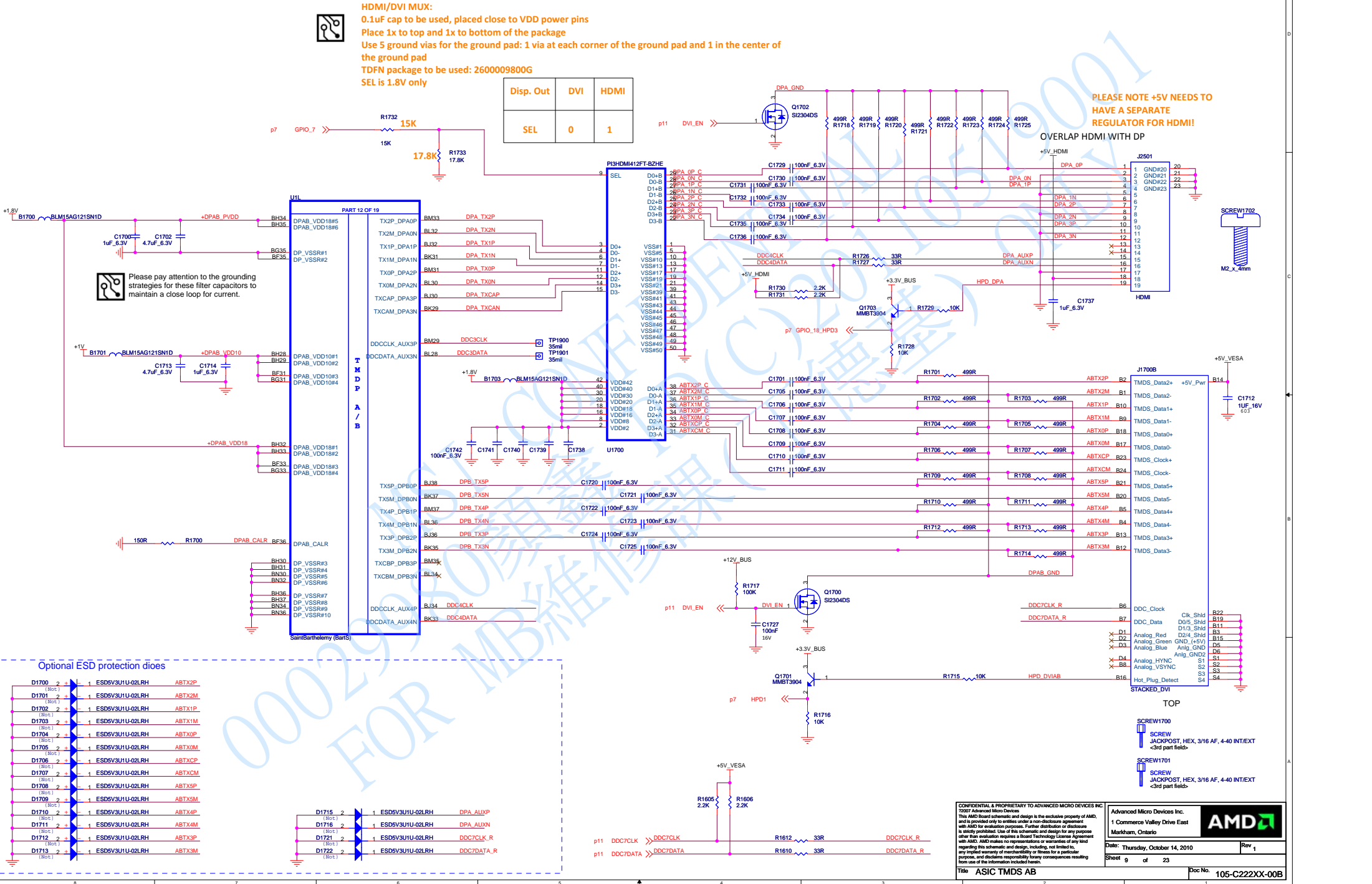
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Date:	Thursday, October 14, 2010	Rev 1
Sheet	7 of 23	

OPTIONAL ESD PROTECTION DIODES

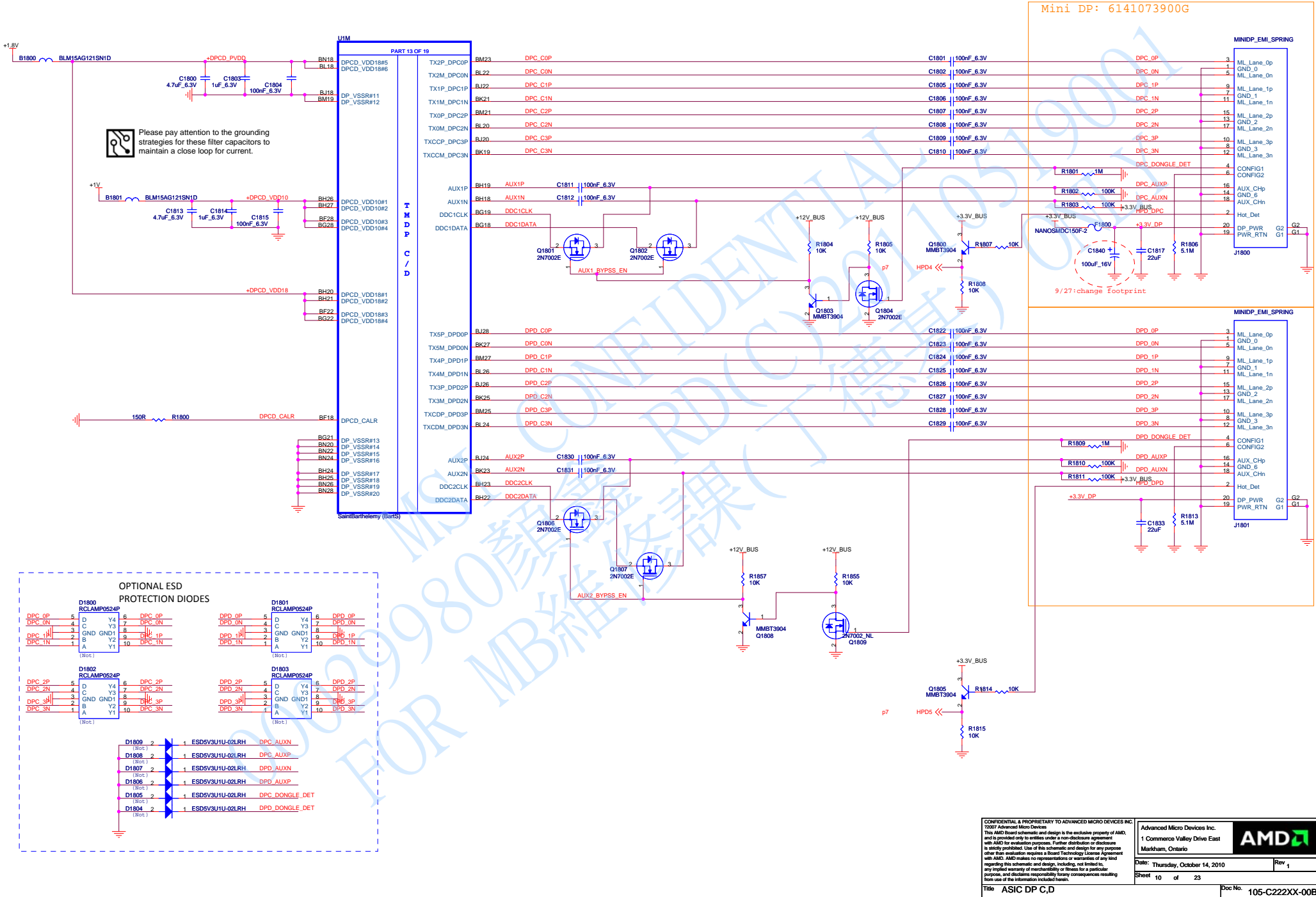
Diode	Rating	Part Number	Protected Signal
D1501	30V	ESD8V301U-Q2L RH	A_R, DAC1_F
D1501	30V	ESD8V301U-Q2L RH	A_G, DAC1_F
D1502	30V	ESD8V301U-Q2L RH	A_B, DAC1_F
D1503	30V	ESD8V0R1B-Q2L RH	D0CDATA, DAC1_R
D1504	30V	ESD8V0R1B-Q2L RH	D0CCLK, DAC1_R
D1505	30V	ESD8V0R1B-Q2L RH	HSYN, DAC1_R
D1506	30V	ESD8V0R1B-Q2L RH	VSYN, DAC1_R



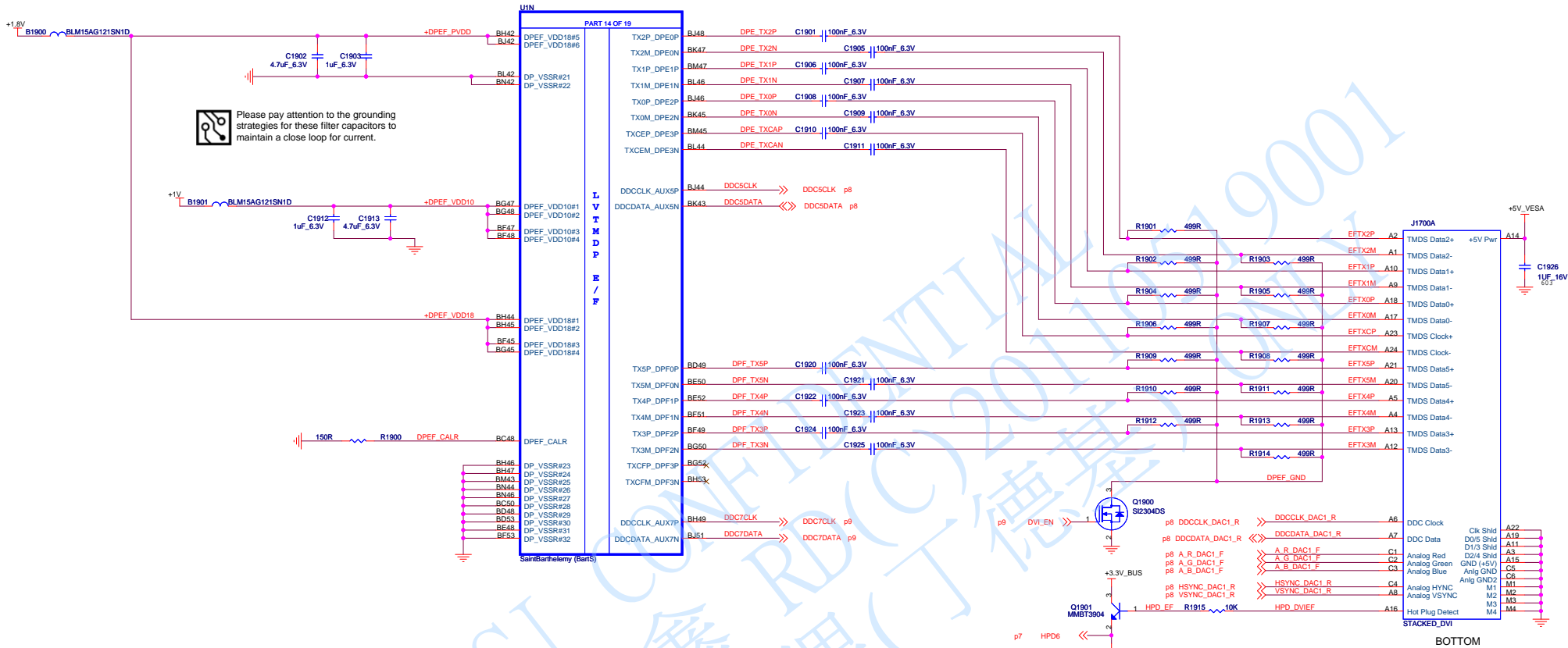
(09) BARTS / CYPRESS TMDS A&B



(10) BARTS / CYPRESS Display Port/HDMI C&D

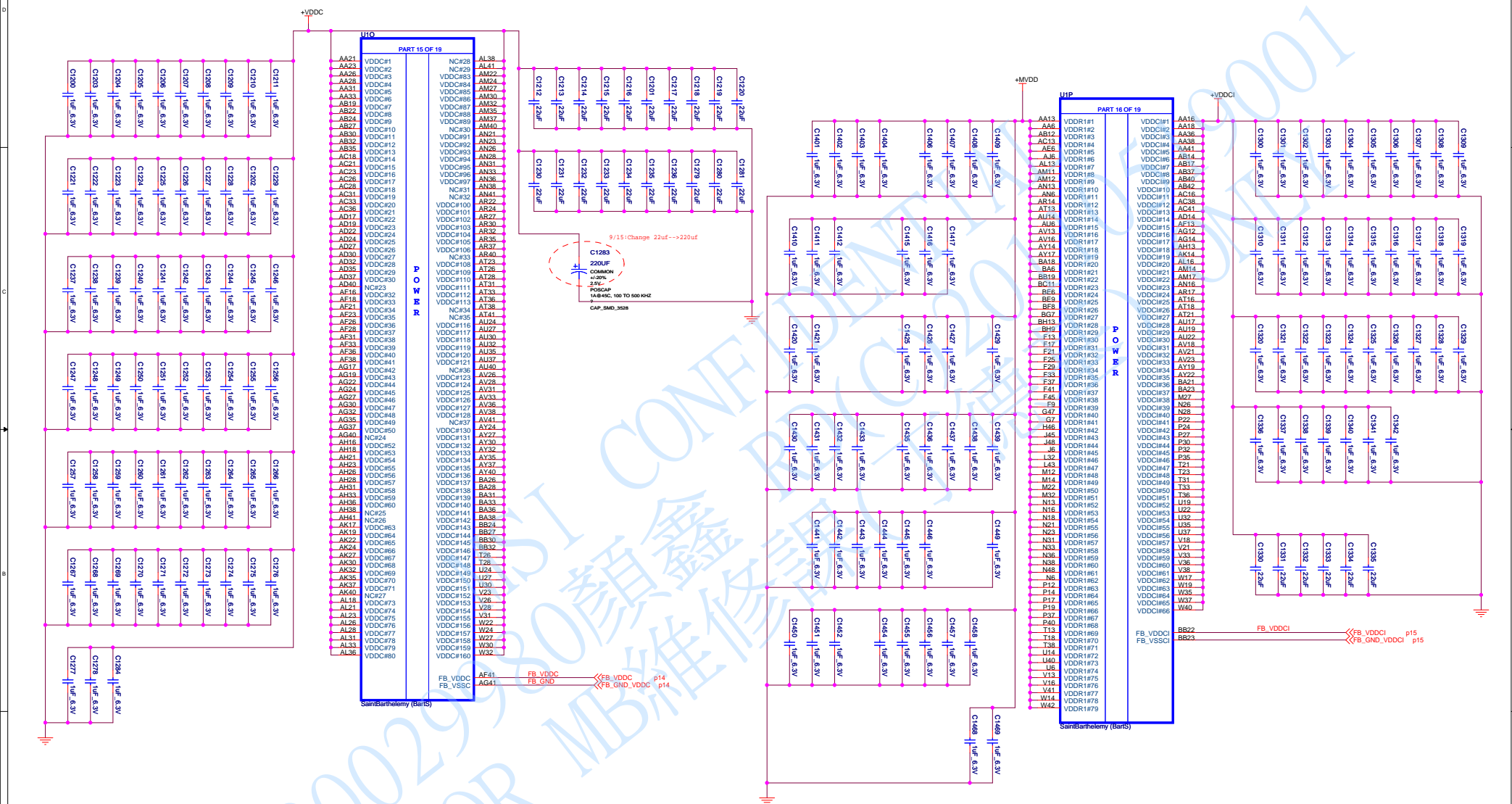


(11) BARTS / CYPRESS LVTMDP E&F



- SCREW1900
SCREW JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
-3rd part field-
- SCREW1901
SCREW JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
-3rd part field-

(12) BARTS / CYPRESS Power



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Title ASIC POWER

(13) BARTS / CYPRESS GND

UIC		
PART 17 OF 19		
A46	VSS#1	AM10
AA10	VSS#2	AM13
AA14	VSS#3	AM16
AA17	VSS#4	AM21
AA19	VSS#5	AM23
AA2	VSS#6	AM26
AA22	VSS#7	AM28
AA24	VSS#8	AM31
AA27	VSS#9	AM33
AA30	VSS#10	AM36
AA32	VSS#11	AM38
AA35	VSS#12	AM41
AA37	VSS#13	AM8
AA40	VSS#14	AN12
AA42	VSS#15	AN14
AA5	VSS#16	AN17
AB13	VSS#17	AN2
AB16	VSS#18	AN22
AB18	VSS#19	AN24
AB1	VSS#20	AN27
AB23	VSS#21	AN30
AB28	VSS#22	AN32
AB29	VSS#23	AN35
AB31	VSS#24	AN37
AB33	VSS#25	AN40
AB36	VSS#26	AN9
AB38	VSS#27	AR13
AB41	VSS#28	AR16
AB9	VSS#29	AR2
AC10	VSS#30	AR21
AC14	VSS#31	AR23
AC17	VSS#32	AR26
AC19	VSS#33	AR28
AC2	VSS#34	AR31
AC22	VSS#35	AR33
AC24	VSS#36	AR36
AC27	VSS#37	AR38
AC30	VSS#38	AR41
AC32	VSS#39	AR6
AC35	VSS#40	AR8
AC37	VSS#41	AT10
AC40	VSS#42	AT14
AC42	VSS#43	AT17
AC6	VSS#44	AT19
AD13	VSS#45	AT22
AD16	VSS#46	AT24
AD18	VSS#47	AT27
AD21	VSS#48	AT30
AD23	VSS#49	AT32
AD26	VSS#50	AT35
AD28	VSS#51	AT37
AD31	VSS#52	AT40
AD33	VSS#53	AT6
AD36	VSS#54	AU13
AD38	VSS#55	AU16
AD41	VSS#56	AU18
AE1	VSS#57	AU2
AE2	VSS#58	AU21
AE5	VSS#59	AU23
AE10	VSS#60	AU26
AE14	VSS#61	AU28
AE17	VSS#62	AU31
AE19	VSS#63	AU33
AE22	VSS#64	AU36
AE24	VSS#65	AU38
AE27	VSS#66	AU41
AE30	VSS#67	AU50
AE32	VSS#68	AU52
AE35	VSS#69	AV11
AE37	VSS#70	AV14
AE40	VSS#71	AV17
AG13	VSS#72	AV19
AG16	VSS#73	AV22
AG2	VSS#74	AV27
AG21	VSS#75	AV30
AG24	VSS#76	AV32
AG26	VSS#77	AV35
AG28	VSS#78	AV37
AG31	VSS#79	AV40
AG33	VSS#80	AV43
AG36	VSS#81	AV46
AG38	VSS#82	AV8
AG6	VSS#83	AW2
AH14	VSS#84	AW50
AH17	VSS#85	AW52
AH19	VSS#86	AW6
AH22	VSS#87	AW9
AH24	VSS#88	AY10
AH27	VSS#89	AY13
AH30	VSS#90	AY16
AH32	VSS#91	AY18
AH35	VSS#92	AY21
AH37	VSS#93	AY23
AH40	VSS#94	AY26
AH9	VSS#95	AY28
AI11	VSS#96	AY32
AI2	VSS#97	AY35
AI22	VSS#98	AY37
AI24	VSS#99	AY38
AK16	VSS#100	AY41
AK18	VSS#101	AY43
AK21	VSS#102	AY46
AK23	VSS#103	B11
AK26	VSS#104	B13
AK28	VSS#105	B15
AK31	VSS#106	B17
AK33	VSS#107	B19
AK36	VSS#108	B21
AK38	VSS#109	B23
AL14	VSS#110	B25
AL17	VSS#111	B27
AL19	VSS#112	B29
AL2	VSS#113	B31
AL22	VSS#114	B33
AL24	VSS#115	B35
AL27	VSS#116	B37
AL30	VSS#117	B39
AL32	VSS#118	B41
AL35	VSS#119	B43
AL37	VSS#120	B45
AL40	VSS#121	B47
AL6	VSS#122	B49
AL9	VSS#123	B51
	VSS#124	BA14
	VSS#125	

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UIR		
PART 18 OF 19		
BA17	VSS#251	VSS#376
BA19	VSS#252	VSS#377
BA2	VSS#253	VSS#378
BA22	VSS#254	VSS#379
BA24	VSS#255	VSS#380
BA27	VSS#256	VSS#381
BA30	VSS#257	VSS#382
BA32	VSS#258	VSS#383
BA35	VSS#259	VSS#384
BA37	VSS#260	VSS#385
BA40	VSS#261	VSS#386
BA41	VSS#262	VSS#387
BA43	VSS#263	VSS#388
BA46	VSS#264	VSS#389
BA49	VSS#265	VSS#390
BA51	VSS#266	VSS#391
BA53	VSS#267	VSS#392
BA56	VSS#268	VSS#393
BA59	VSS#269	VSS#394
BA62	VSS#270	VSS#395
BA65	VSS#271	VSS#396
BA68	VSS#272	VSS#397
BA71	VSS#273	VSS#398
BA74	VSS#274	VSS#399
BA77	VSS#275	VSS#400
BA80	VSS#276	VSS#401
BA83	VSS#277	VSS#402
BA86	VSS#278	VSS#403
BA89	VSS#279	VSS#404
BA92	VSS#280	VSS#405
BA95	VSS#281	VSS#406
BA98	VSS#282	VSS#407
BA101	VSS#283	VSS#408
BA104	VSS#284	VSS#409
BA107	VSS#285	VSS#410
BA110	VSS#286	VSS#411
BA113	VSS#287	VSS#412
BA116	VSS#288	VSS#413
BA119	VSS#289	VSS#414
BA122	VSS#290	VSS#415
BA125	VSS#291	VSS#416
BA128	VSS#292	VSS#417
BA131	VSS#293	VSS#418
BA134	VSS#294	VSS#419
BA137	VSS#295	VSS#420
BA140	VSS#296	VSS#421
BA143	VSS#297	VSS#422
BA146	VSS#298	VSS#423
BA149	VSS#299	VSS#424
BA152	VSS#300	VSS#425
BA155	VSS#301	VSS#426
BA158	VSS#302	VSS#427
BA161	VSS#303	VSS#428
BA164	VSS#304	VSS#429
BA167	VSS#305	VSS#430
BA170	VSS#306	VSS#431
BA173	VSS#307	VSS#432
BA176	VSS#308	VSS#433
BA179	VSS#309	VSS#434
BA182	VSS#310	VSS#435
BA185	VSS#311	VSS#436
BA188	VSS#312	VSS#437
BA191	VSS#313	VSS#438
BA194	VSS#314	VSS#439
BA197	VSS#315	VSS#440
BA200	VSS#316	VSS#441
BA203	VSS#317	VSS#442
BA206	VSS#318	VSS#443
BA209	VSS#319	VSS#444
BA212	VSS#320	VSS#445
BA215	VSS#321	VSS#446
BA218	VSS#322	VSS#447
BA221	VSS#323	VSS#448
BA224	VSS#324	VSS#449
BA227	VSS#325	VSS#450
BA230	VSS#326	VSS#451
BA233	VSS#327	VSS#452
BA236	VSS#328	VSS#453
BA239	VSS#329	VSS#454
BA242	VSS#330	VSS#455
BA245	VSS#331	VSS#456
BA248	VSS#332	VSS#457
BA251	VSS#333	VSS#458
BA254	VSS#334	VSS#459
BA257	VSS#335	VSS#460
BA260	VSS#336	VSS#461
BA263	VSS#337	VSS#462
BA266	VSS#338	VSS#463
BA269	VSS#339	VSS#464
BA272	VSS#340	VSS#465
BA275	VSS#341	VSS#466
BA278	VSS#342	VSS#467
BA281	VSS#343	VSS#468
BA284	VSS#344	VSS#469
BA287	VSS#345	VSS#470
BA290	VSS#346	VSS#471
BA293	VSS#347	VSS#472
BA296	VSS#348	VSS#473
BA299	VSS#349	VSS#474
BA302	VSS#350	VSS#475
BA305	VSS#351	VSS#476
BA308	VSS#352	VSS#477
BA311	VSS#353	VSS#478
BA314	VSS#354	VSS#479
BA317	VSS#355	VSS#480
BA320	VSS#356	VSS#481
BA323	VSS#357	VSS#482
BA326	VSS#358	VSS#483
BA329	VSS#359	VSS#484
BA332	VSS#360	VSS#485
BA335	VSS#361	VSS#486
BA338	VSS#362	
BA341	VSS#363	
BA344	VSS#364	VSS#487
BA347	VSS#365	VSS#488
BA350	VSS#366	VSS#489
BA353	VSS#367	VSS#490
BA356	VSS#368	VSS#491
BA359	VSS#369	VSS#492
BA362	VSS#370	VSS#493
BA365	VSS#371	VSS#494
BA368	VSS#372	VSS#495
BA371	VSS#373	VSS#496
BA374	VSS#374	VSS#497
BA377	VSS#375	VSS#498

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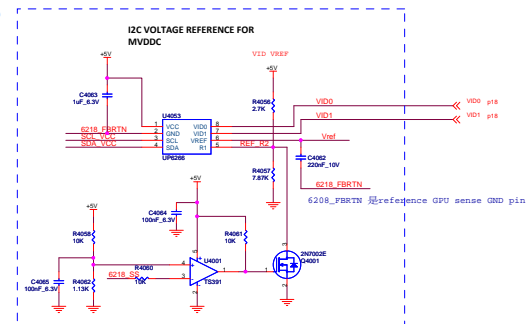
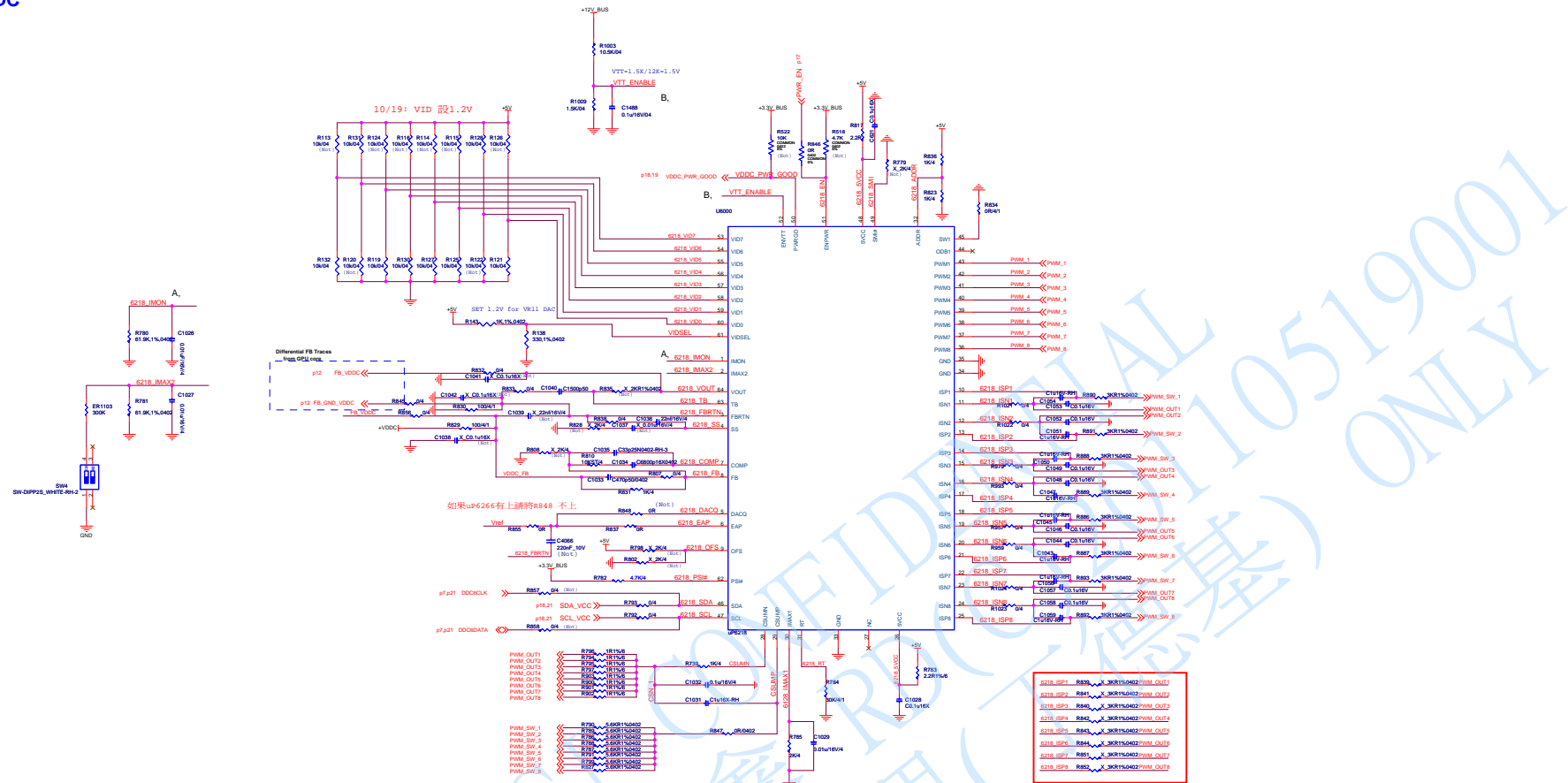
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ASIC GND

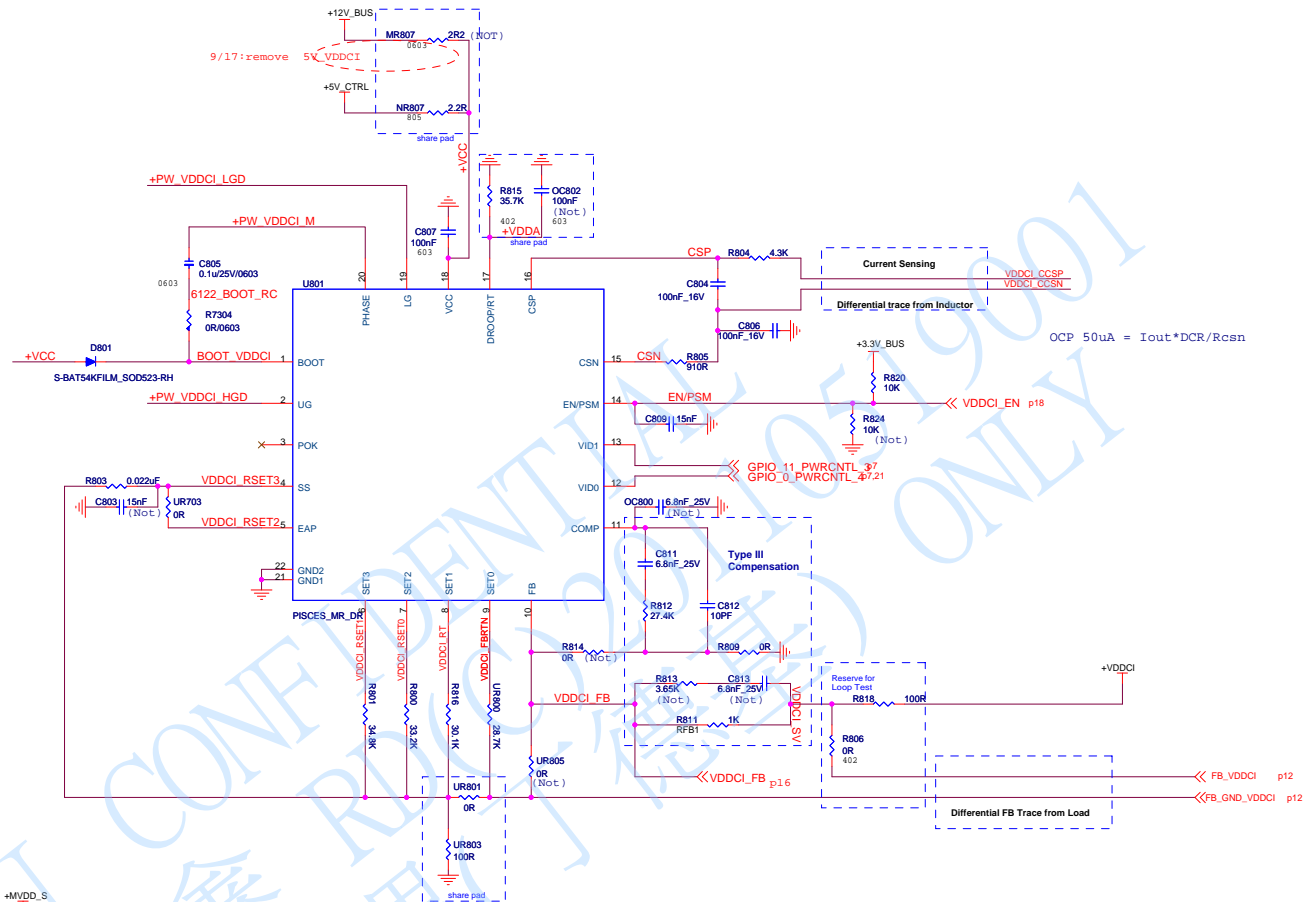
(14) VDDC



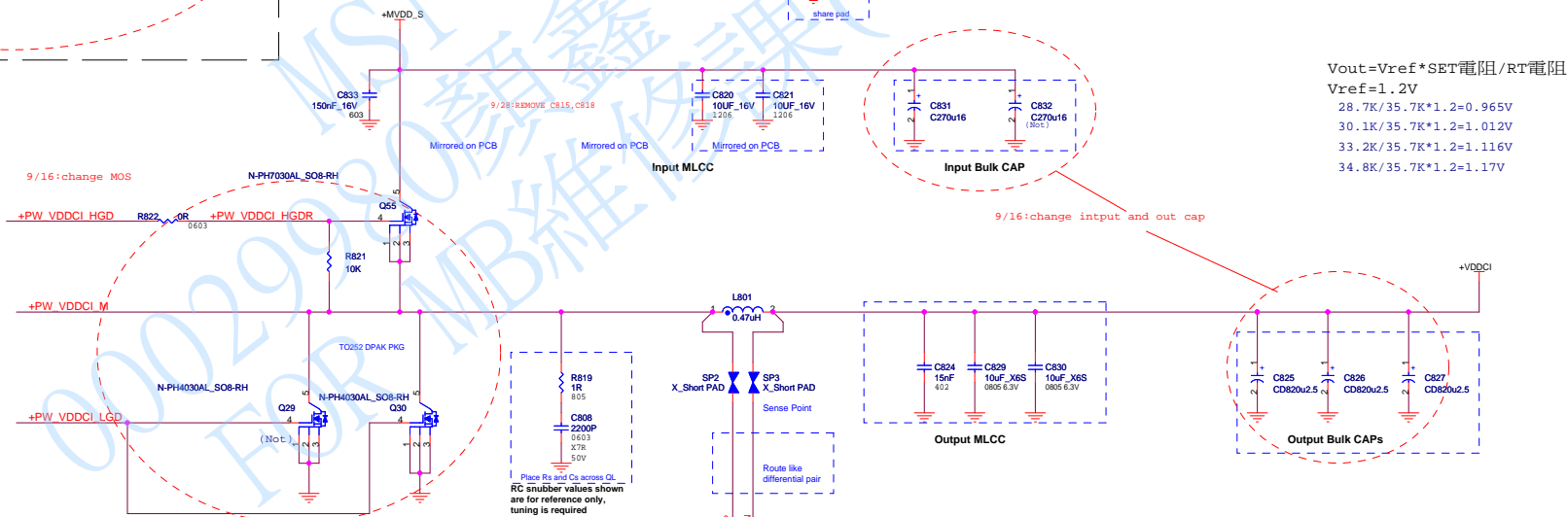
GPIO_15	GPIO_20	State	VDDC(V)
1	1	High	1.175
1	0	Medium	1.100
0	0	Low	0.950

(15) VDDCI

GPIO_0	GPIO_11	State	VDDCI(V)
1	1	High	1.15
1	1	Medium	1.15
0	0	Low	0.950



9/17:remove backup option for 5V VDDCI



```
VID11:1.1697V
VID10:1.159V
VID01:1.0118V
VID00:0.9647V
```

Vout=Vref*SET電阻/RT電阻
Vref=1.2V
28.7K/35.7K*1.2=0.965V
30.1K/35.7K*1.2=1.012V
33.2K/35.7K*1.2=1.116V
34.8K/35.7K*1.2=1.17V

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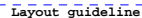
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Doc No.	105-C222XX-00B
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2-Position the controller (U703) such that LdGate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R718 and R722 next to the gate of the MOSFETs. Make the gate drive traces (PW MVECD Lcd and PW MVECD Hdd) as short and as wide as possible to reduce the trace inductance.

3-Place the decoupling capacitors (C701 and C702) as close as possible to the controller as possible. They are as follows:
Vec bypass cap is C703, and Boost cap is C705.

3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 6 and 5. These are R719, R711, C713, R712 and C711, C712.

Resistors to set the output voltages
for +VDDCI and +MVDD .

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Date: Monday, October 18, 2010

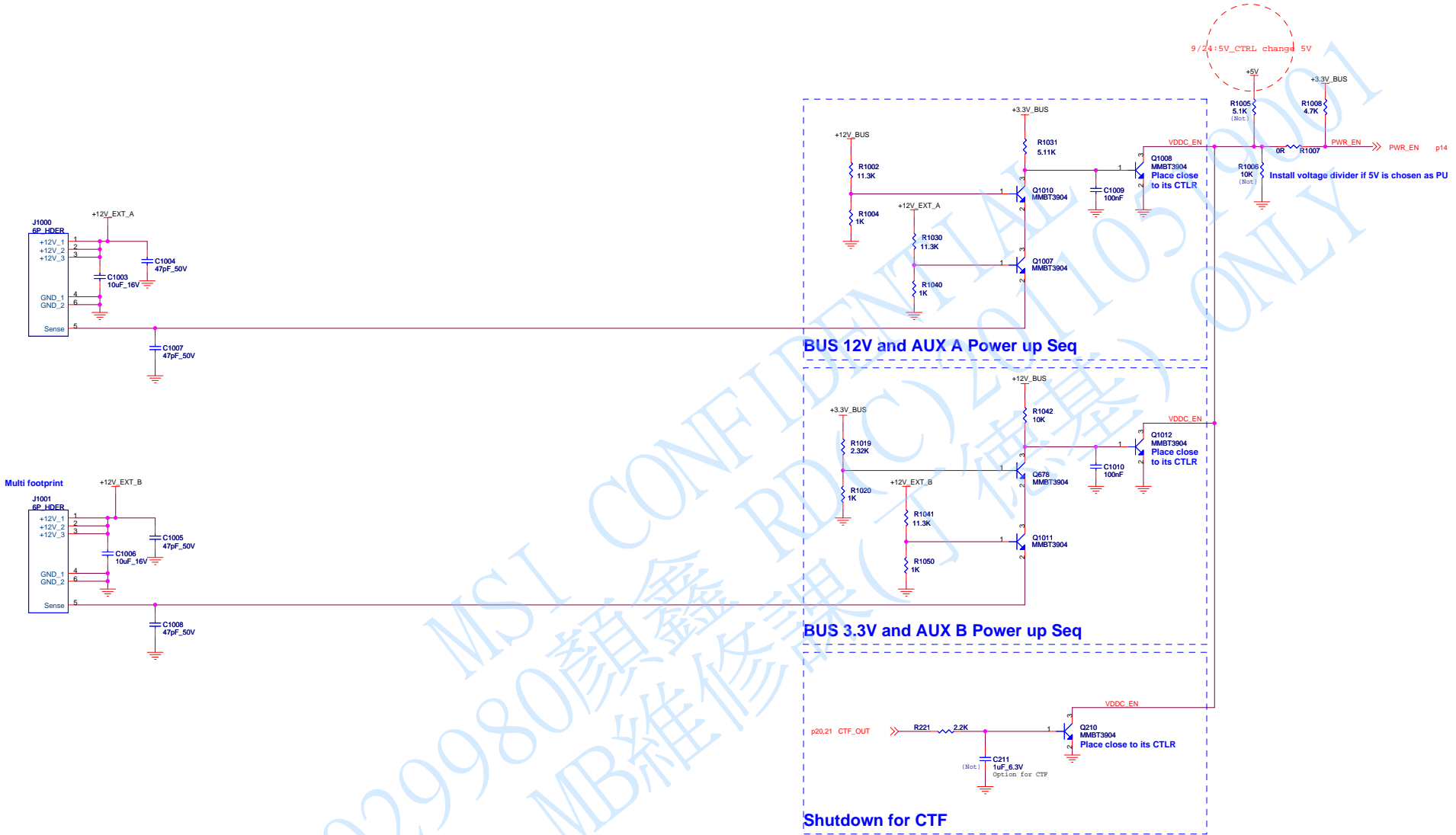
Sheet 16 of 23

Rev 1

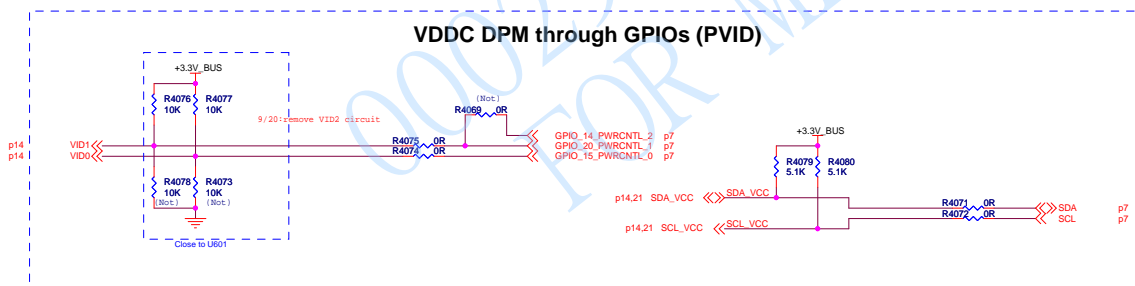
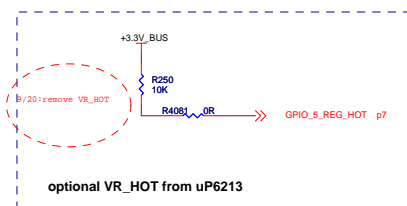
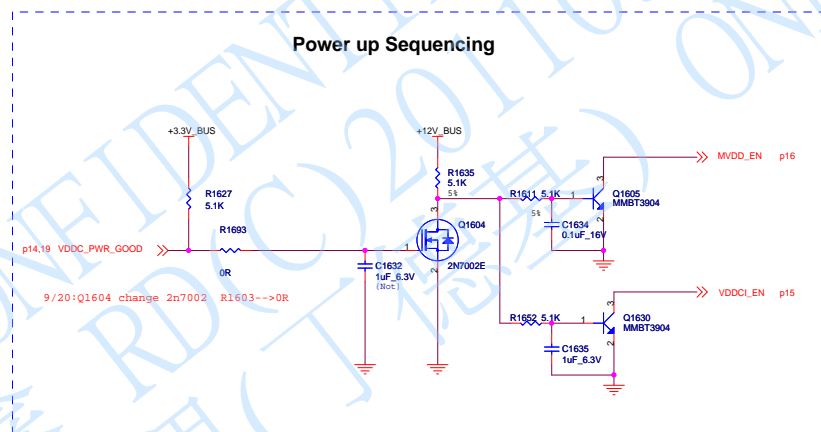
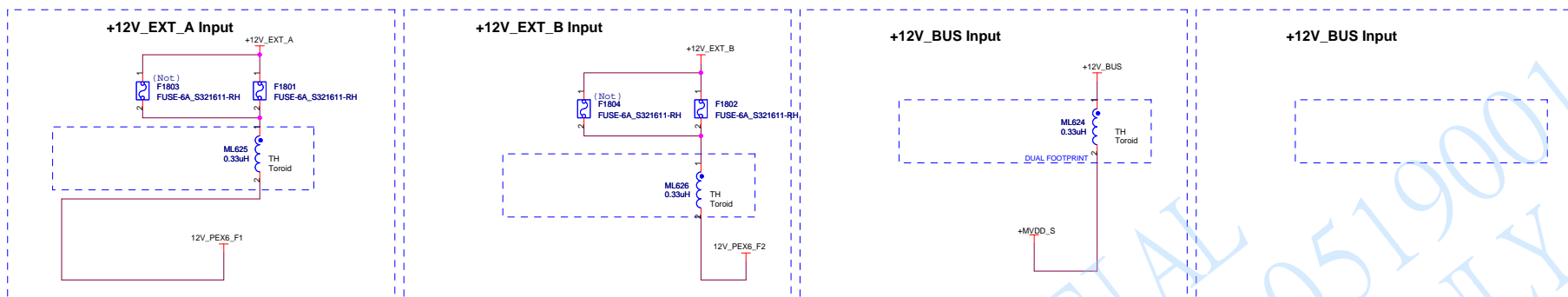
Title MVDD

Doc No.	105-C222XX-00B
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(19) BARTS / CYPRESS POWER MGMNT



(17) BARTS / CYPRESS VDDCI POWER PLAY



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Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario



Date: Thursday, October 14, 2010

Rev.

Sheet 18 of 23

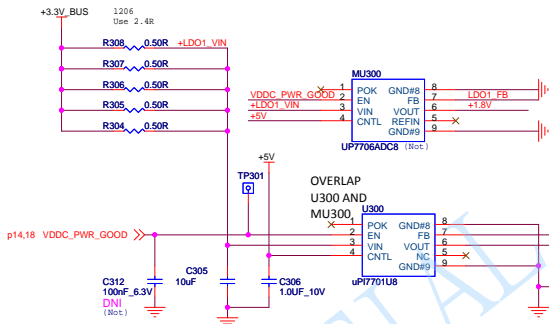
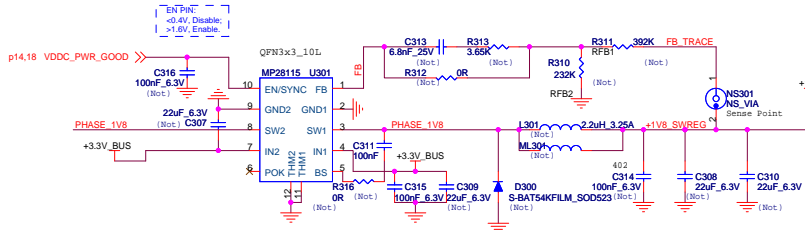
23

Title **Power Management 2**

Doc No. 105-C222XX-00B

(18) BARTS / CYPRESS Small Rail Regulators

LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

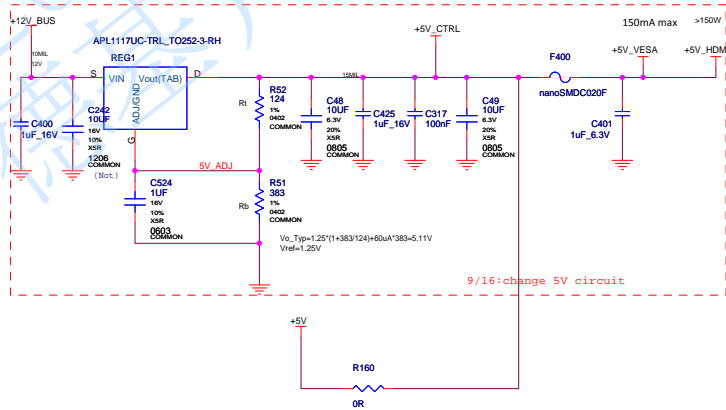


$$V_{OUT} = V_{ref} \times (1 + R5/R4)$$

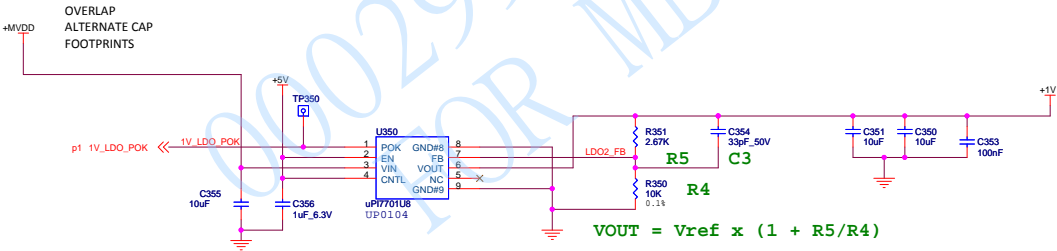
Other cheaper solution at 5MHz switching for 1.8V

Overlap 1206/0805

Regulators for +5V, +5V_VESA and +5V_HDMI
Iout max = 150mA (DVI+HDMI)



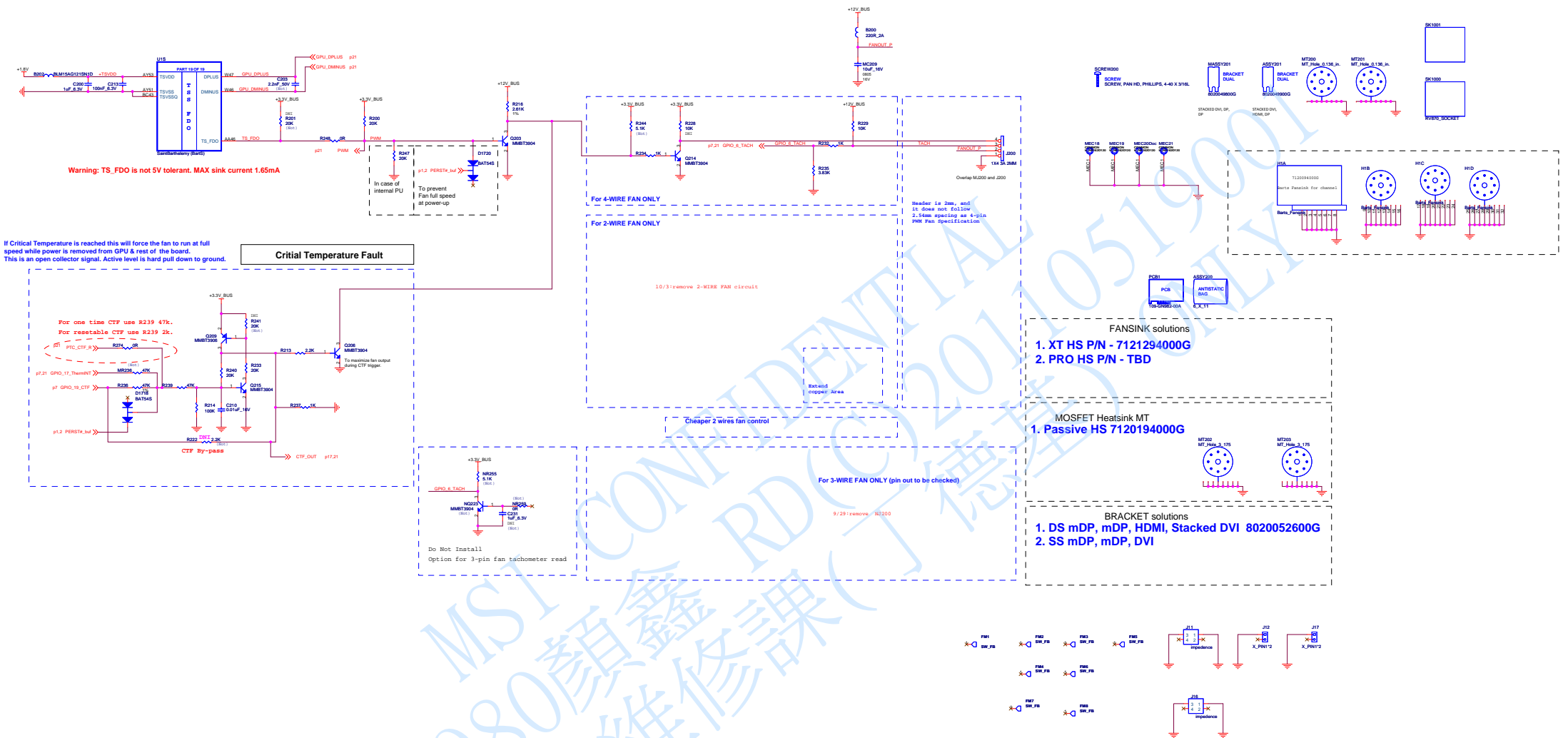
LDO #2: Vin = +1.35V to 1.8V MAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



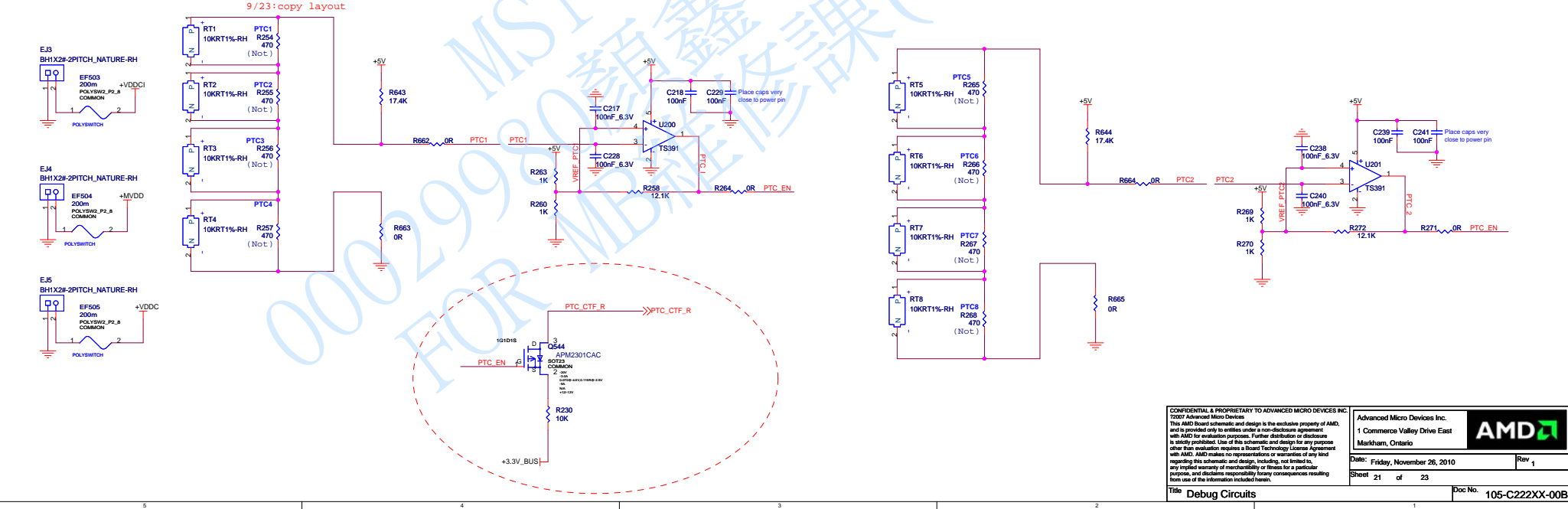
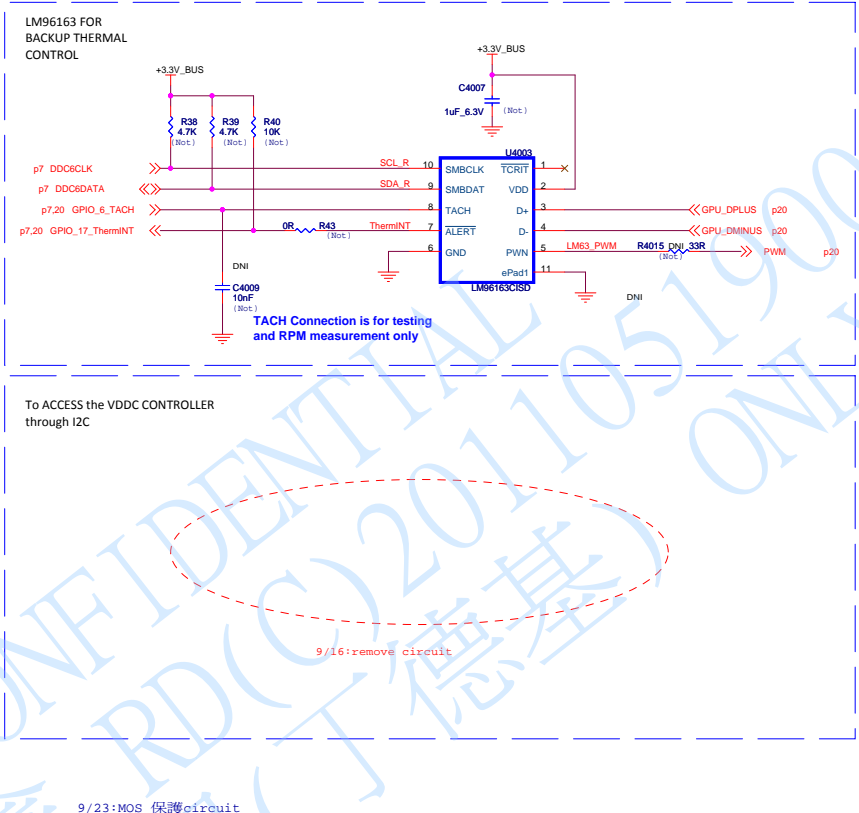
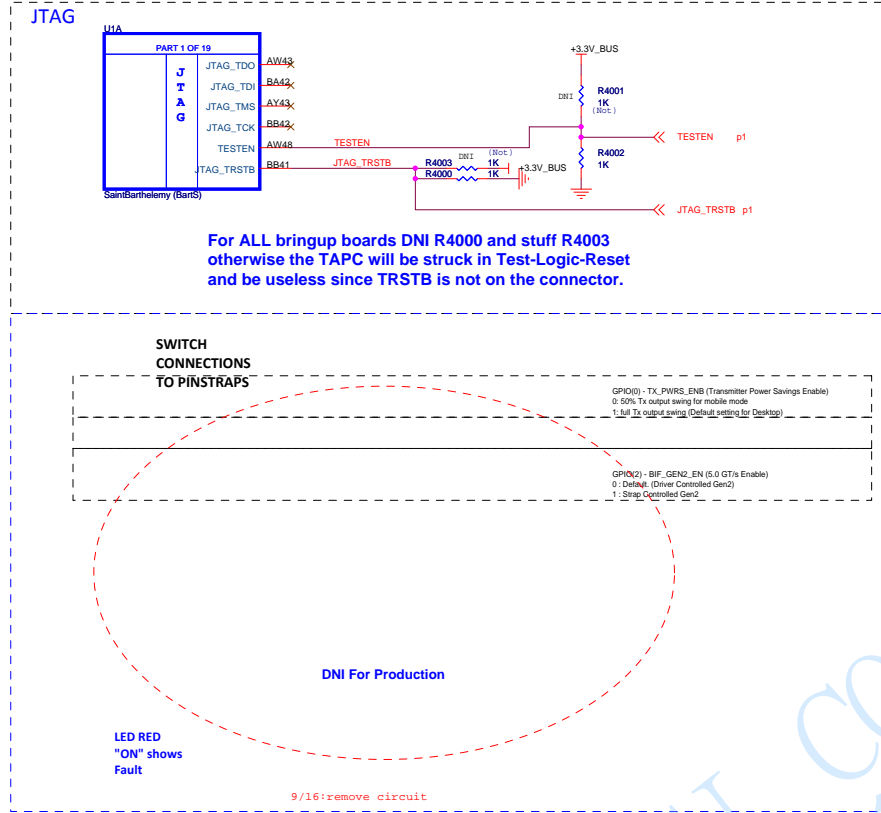
optional 5V power for VDDC regulator;

9/16:remove u426 circuit

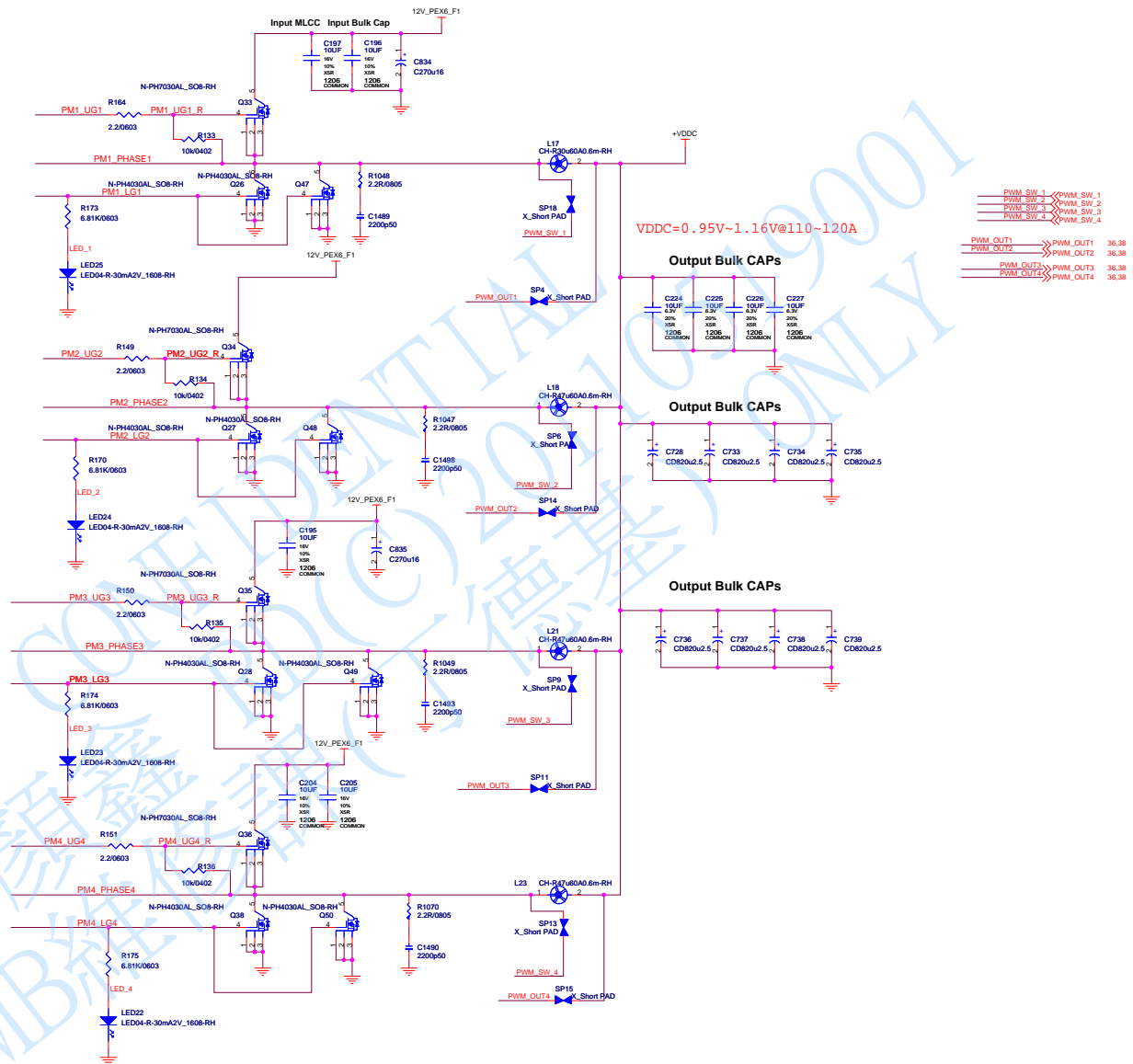
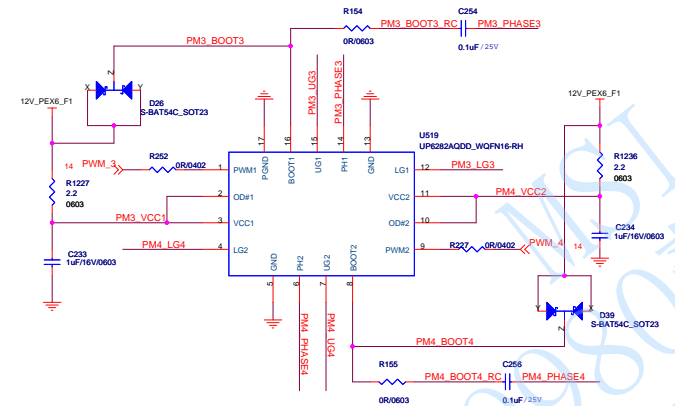
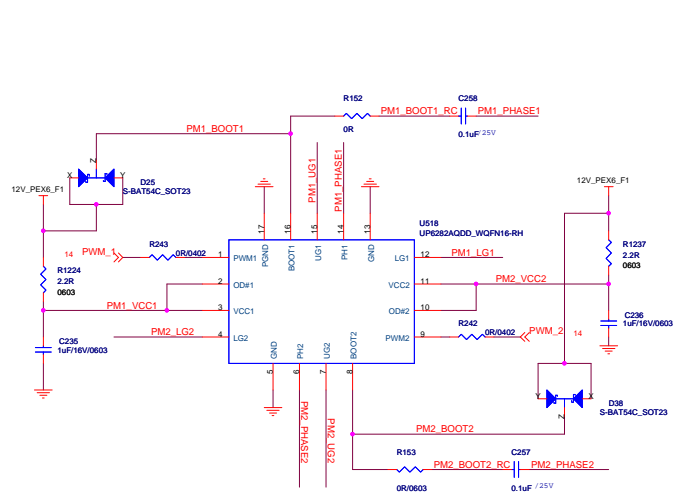
(20) BARTS / CYPRESS Mechanical and Thermal Management



(21) CYPRESS Debug Circuits



Power Supply: VDDC 1~4 Phase powered from external PEX 8PIN



PWM_SW_1	»	PWM_SW_1	
PWM_SW_2	»	PWM_SW_2	
PWM_SW_3	»	PWM_SW_3	
PWM_SW_4	»	PWM_SW_4	
PWM_OUT1	»	PWM_OUT1	36.38
PWM_OUT2	»	PWM_OUT2	36.38
PWM_OUT3	»	PWM_OUT3	36.38
PWM_OUT4	»	PWM_OUT4	36.38

VDDC=0.95V~1.16V@110~120A

Output Bulk CAPs

Output Bulk CAPs

Output Bulk CAPs

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVDD Phase 1-2 of 4



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Title RH BARTS CYPRESS GDDR5 mDP-mDP-HDMI-DVII-DVII		Schematic No. 105-C222XX-00B	Date: Tuesday, November 30, 2010
REVISION HISTORY		NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.	Rev 1
REVISION DESCRIPTION			
Initial release. Based on C220			
Page01: Added direct connection from Pull-Up for M0101 for Cypress Page09: remove the inductor for top DVI line Page14: update Q601,Q602,Q603,Q604 symbol Page17: add C211 Page20: add R201, R237, R241. Page18: add optional 3-pin fan tach circuitry/ Page50: update block diagram			
V251-0A bason C222 Page 07: add dual VBIOS circuit Page 12: add SP-CAP page14: change up6218 power circuit page15:modify up6122 circuit and change choke page16:change up6205 power circuit page17: pwr_en power sequency change 3.3V_BUS page18:change input choke page19:change 5V and remove u330 page21:remove LED circuit and switch and j404, add thermal diode for MOS protection page22/23:add VDDC up6128 driver ciruit			
V251-10 bason V251-0A page21:modify thermal diode for MOS protection			

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