

MS-V027 VER 20

NV44-PCIE NV44 128MB/64bit, BGA 16MX16 DDR2,VGA,DVI-I,TV-OUT(HT-10)

P295-A00 DESIGN NV44 350/333MHZ 64MB/128MB/256MB DDR2 84-FBGA

PAGE SUMMARY:

Page1: P295 Overview

Page2: PCI EXPRESS, NVVDD, VDD33

Page3: FB BANK A, FBVTT TERMINATIONS, FBVDDQ DECOUPLING

Page4: FB BANK C, FBVTT TERMINATIONS

Page5: MEMORY PARTITION A 0..31

Page6: MEMORY PARTITION A 32..63

Page7: GPU GND

Page8: DACA - VGA

Page9: DACB - TVOUT, VIDEO IN

Page10: DACC - VGA

Page11: STRAPS, FANSINK, MECHANICALS

Page12: GPIO, HDCP ROM, VBIOS ROM, FAN CONTROL

Page13: INTERNAL TMDS LINK A/B

Page14: INTERNAL TMDS LINK C/D

Page15: MIOA, MIOB, NVPLL

Page16: POWER SUPPLY (RT9218) for NVVDD,FBVDDQ

Page17: Other Powers - A3V3, DDC_5, TMDSPLL, TMDSIO, FBVTT and 5V-3V3 POWER SEQUENCING

DDR2 84-FBGA Clock setting 250/333MHZ

REV HISTORY

A00

-08/04/2005:

1.Page18: change power solution to RT9218 for NVVDD & FBVDDQ

10S

-08/04/2005:

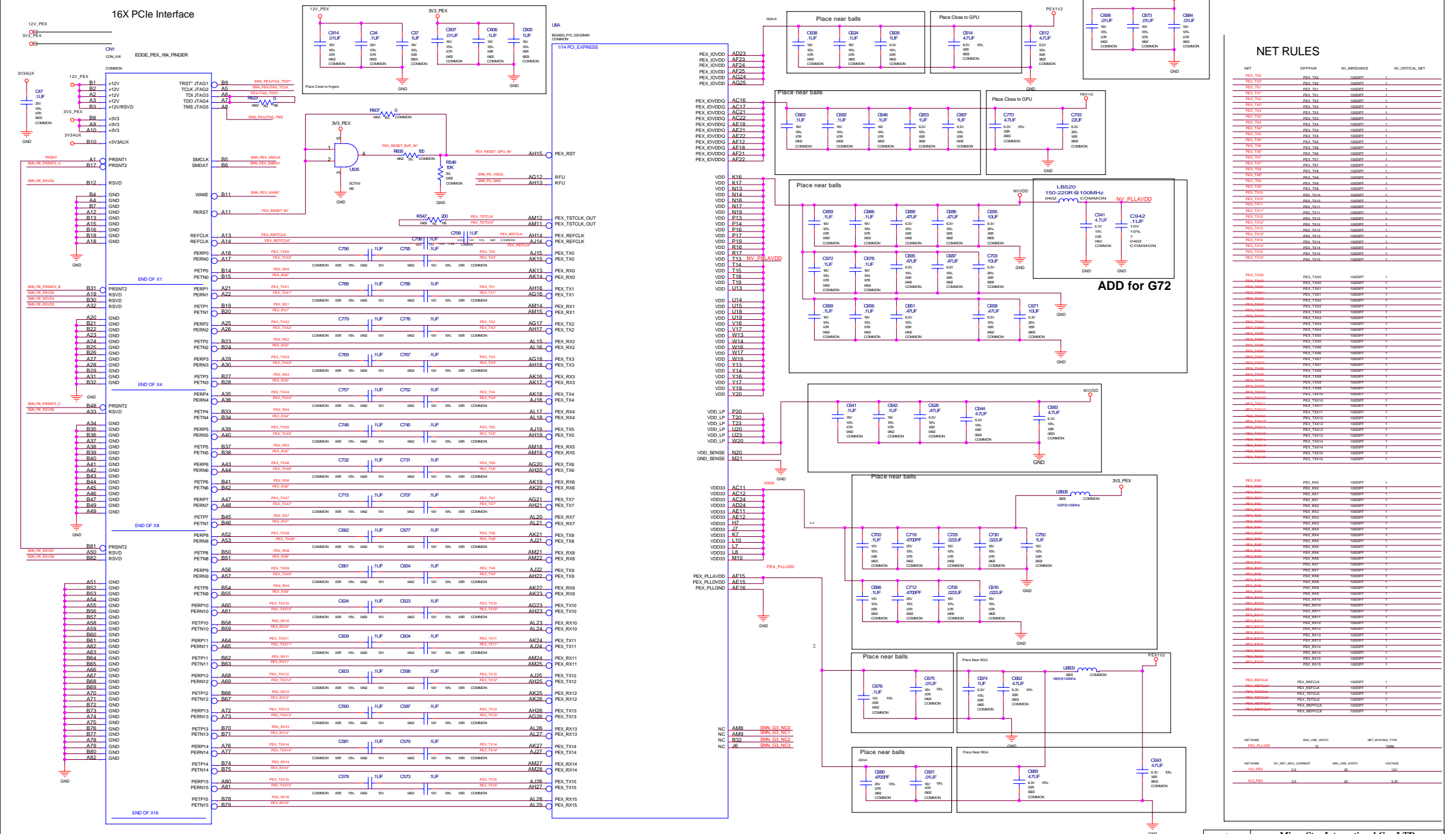
1.Page18: Move C913~C916 out form C910,C911 & Move C930,C931 out form C929

2.Page19: Add C940 near C36

3.Page19: Remove C16, C35, C55

REV	VARIANT	NVPN	ASSEMBLY
0	BASE	80210295-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	80210295-0000-000	GF-6600-AD4 GEN 300267MHZ 256MB 84-FBGA DDR2 16MX16 VGA+DVI+HDTV
2	SKU001	80210295-0001-000	GF-6600-AD4 GEN 300267MHZ 128MB 84-FBGA DDR2 8MX16 VGA+DVI+HDTV
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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02 PCI EXPRESS, NVVDD, VDD33

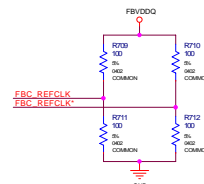


FB PARTITION A

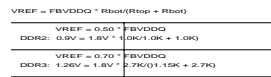


NC For G73

UBC

[illegible]

ADD for G72



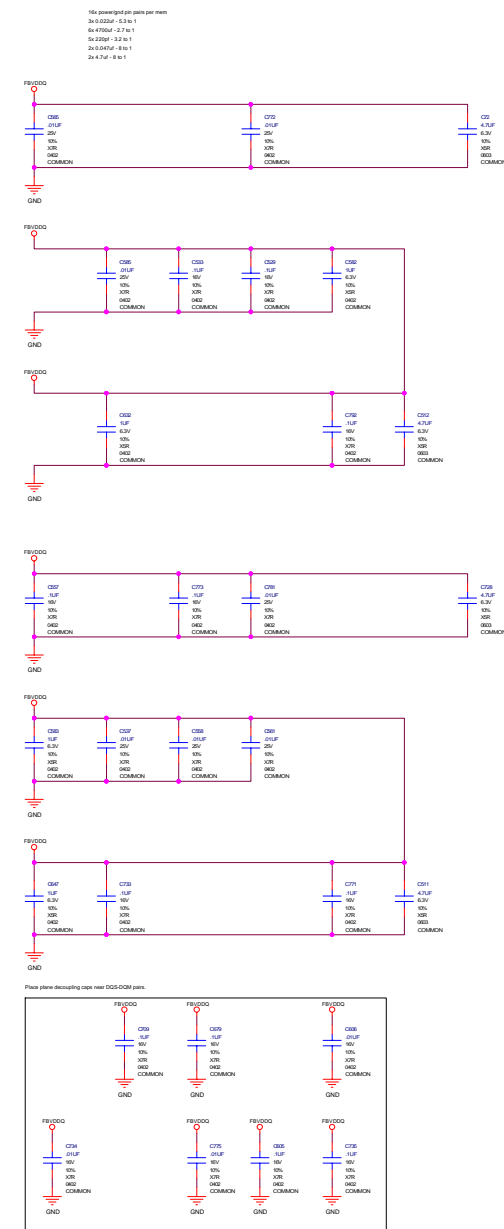
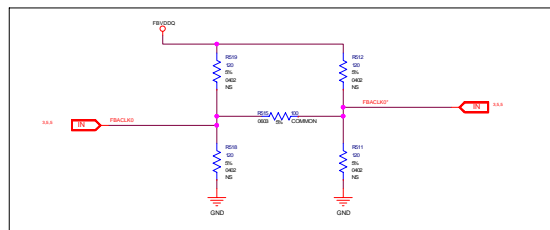
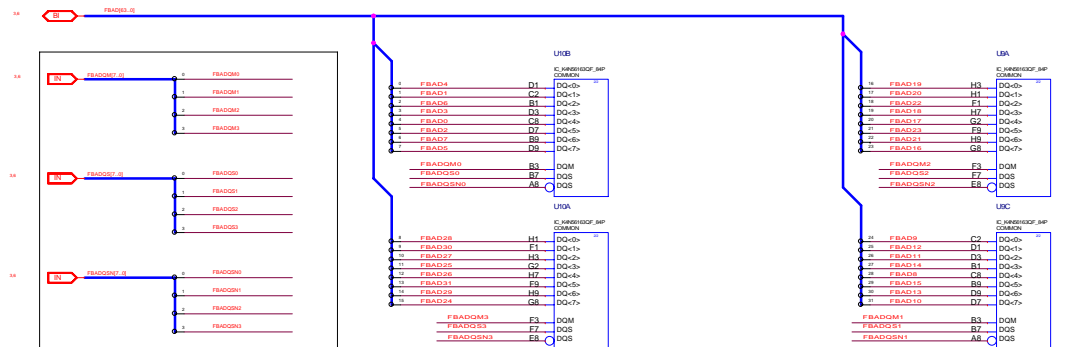
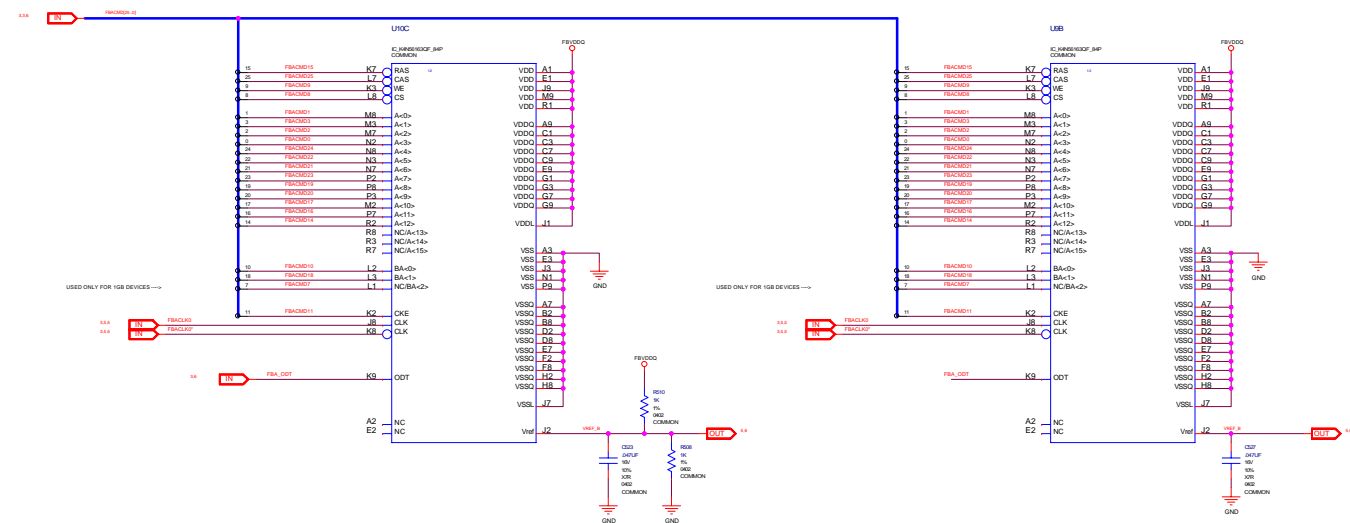
FISC_DOT	DOOM	1
FISC_PD		12
FISC_PU		12
FISC_TERM		12

- 1) During initialization CKE and ODT low
- 2) Runtime ... CKE High and ODT operated by debug state machine
- 3) No termination task for CKE or DEBUG pins

05 MEMORY PARTITION A 0..31

FBA MEMORY 1st bank 0..31

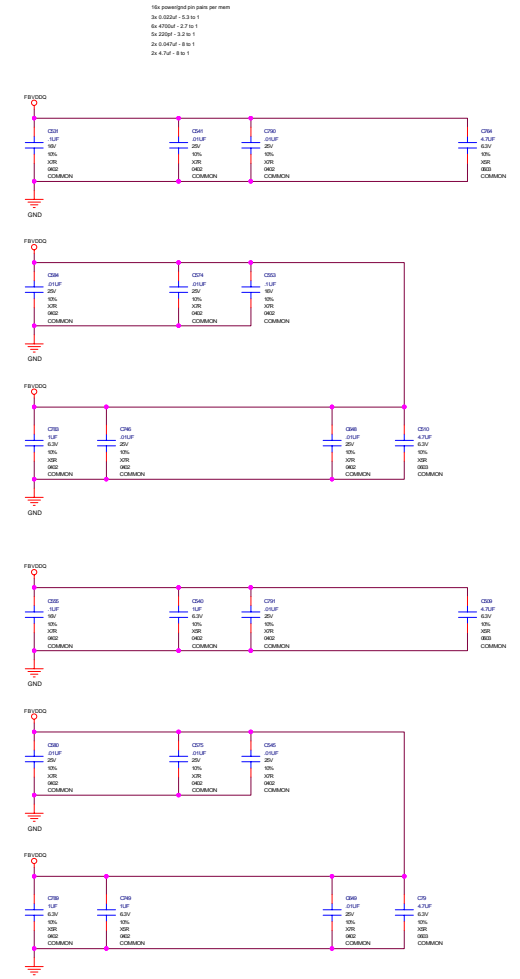
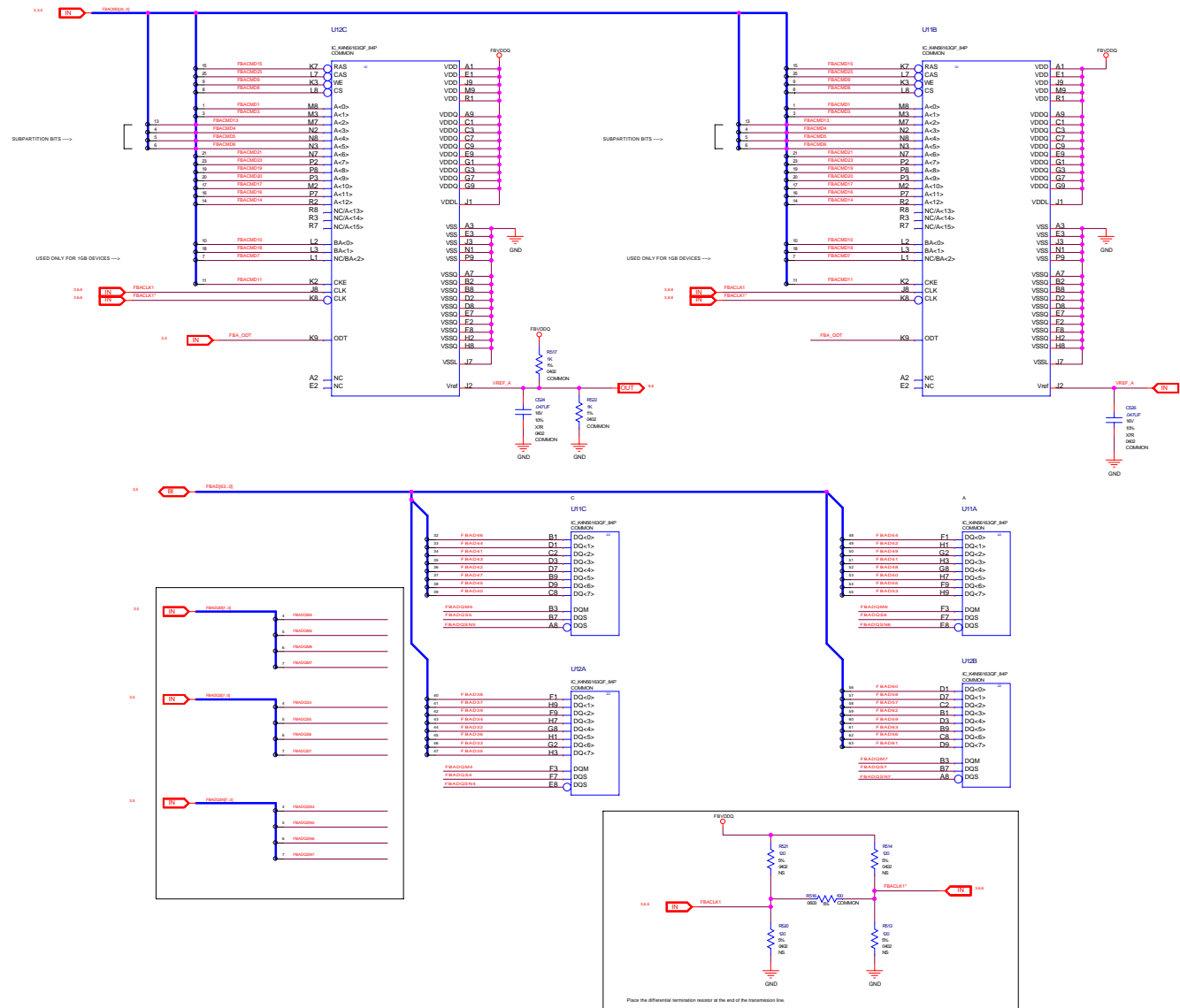
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



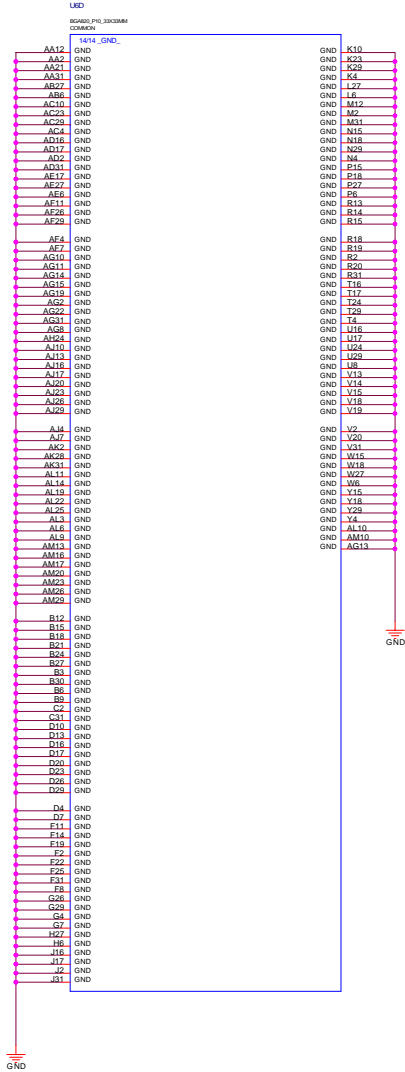
06 MEMORY PARTITION A 32..63

FBA MEMORY 1st bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



09 GPU GND



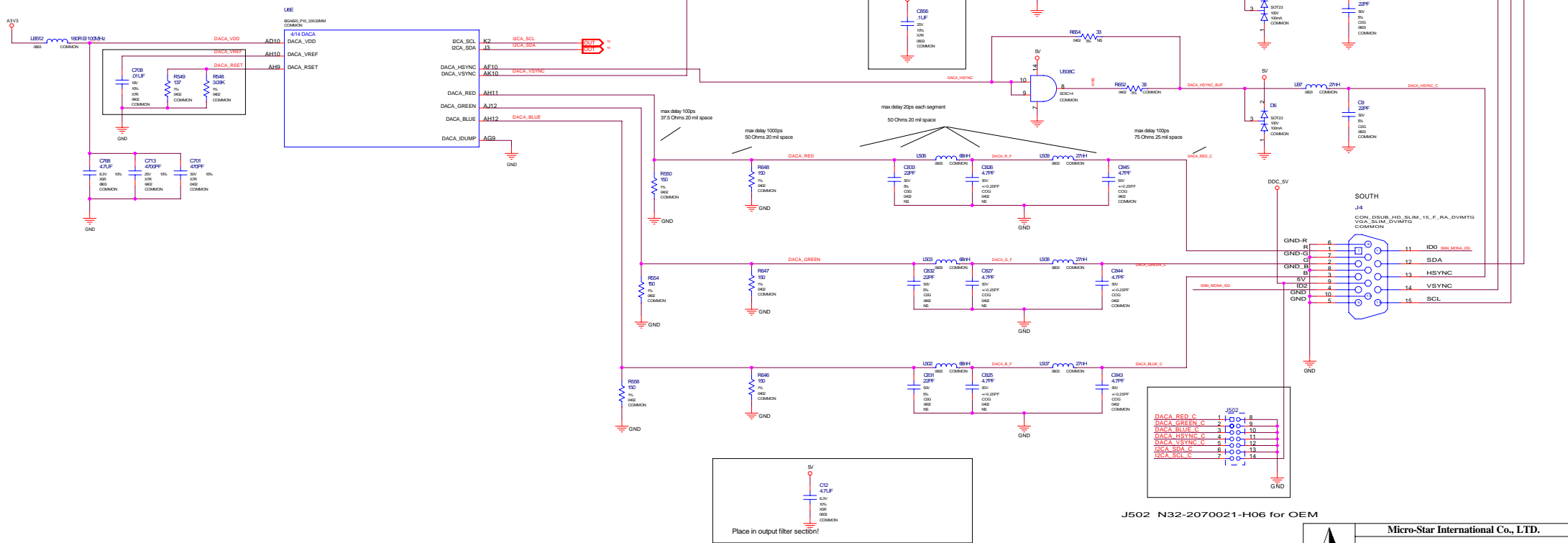
10 DACA - VGA

NET_NAME	MIN_LINE_WIDTH	CV_CRITICAL_NET	NV_IMPEDANCE
DACA_SCL			
DACA_SDA			
DACA_M5VINC		2	100OHM
DACA_V5VINC		2	100OHM
DACA_V5VINC_BUF		2	100OHM
DACA_V5VINC_BUF		2	100OHM
DACA_M5VINC_C		2	100OHM
DACA_V5VINC_C		2	100OHM
A_V5		2	100OHM
A_V5		2	100OHM
DACA_RED		1	100OHM
DACA_GREEN		1	100OHM
DACA_TELE		1	100OHM
DACA_I_T		1	100OHM
DACA_O_T		1	100OHM
DACA_S_T		1	100OHM
DACA_M5V_T		1	100OHM
DACA_M5VINC_T		1	100OHM
DACA_M5VINC_T		1	100OHM
DACA_M5VINC_T		1	100OHM
DACA_VDD	12		
DACA_VREFP	12		
DACA_VREFN	12		

Note that this impedance is the highest one on the x-net for a 4-layer stackup.

Change for G72

C708 0.1u
R549 124ohm
R548 1.78Kohm



J502 N32-2070021-H06 for OEM



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Size Document Number
Custom DACA - VGA

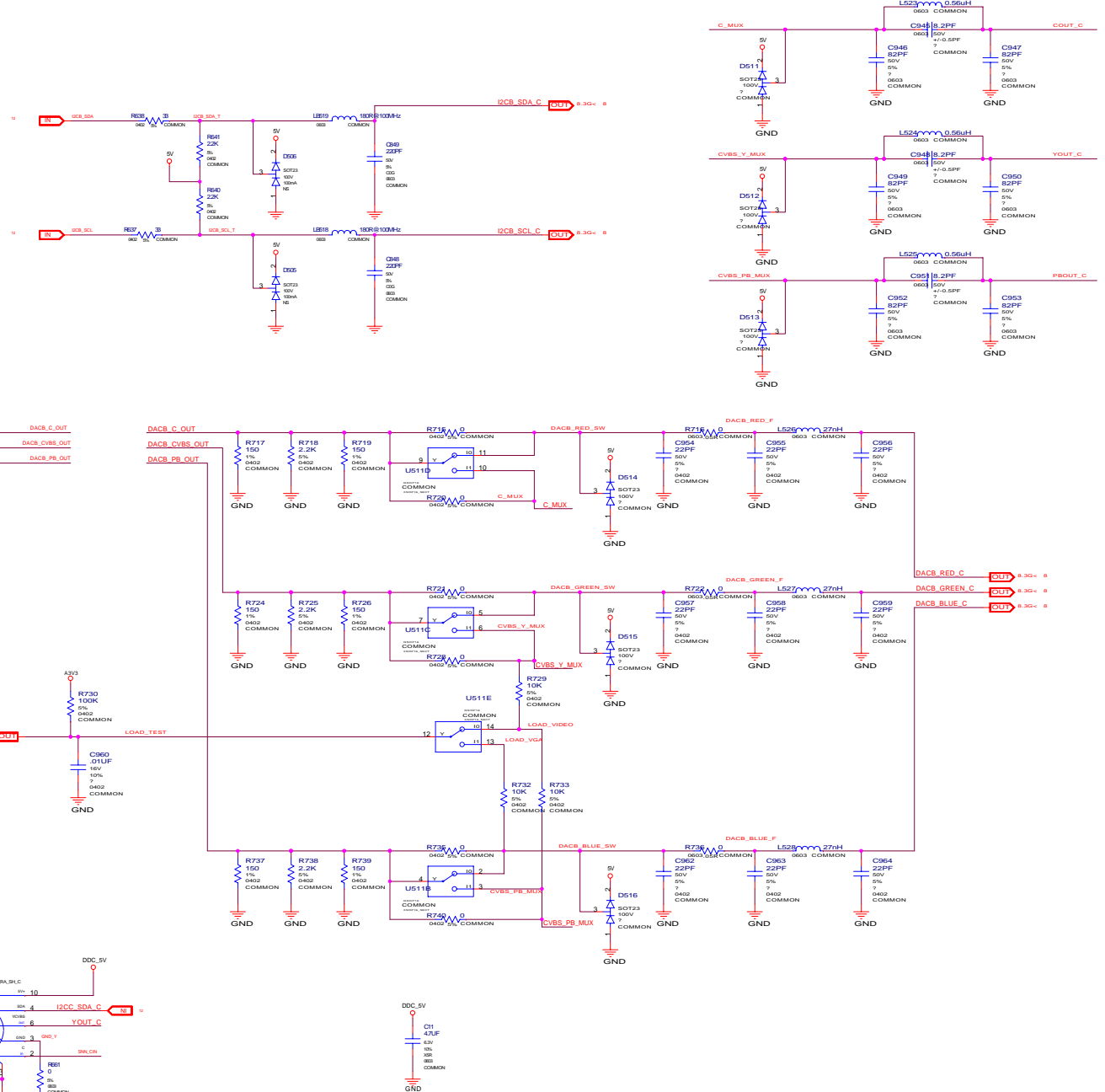
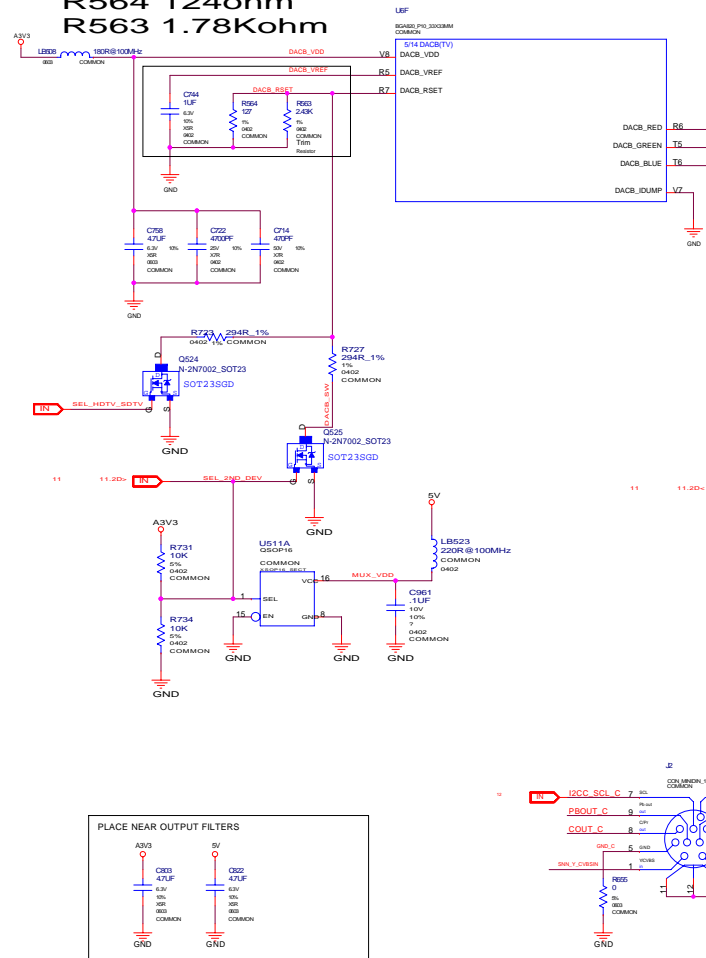
Date: Monday, January 23, 2006 Sheet 8 of 17

11 DACB - TVOUT, VIDEO IN

NET_NAME	MIN_LINE_WIDTH	NV_CRITICAL_NET	NV_IMPEDANCE
DACB_C_OUT		1	50OHM
DACB_CVBS_OUT		1	50OHM
DACB_PB_OUT		1	50OHM
DDOT_C		1	50OHM
YOUT_C		1	50OHM
PBOUT_C		1	50OHM
DACB_VDD	12		
DACB_VREF	12		
DACB_RESET	12		
YRESET	12		
GND_C	15		
GND_Y	15		

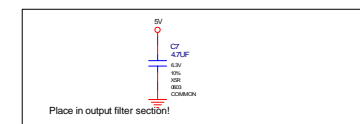
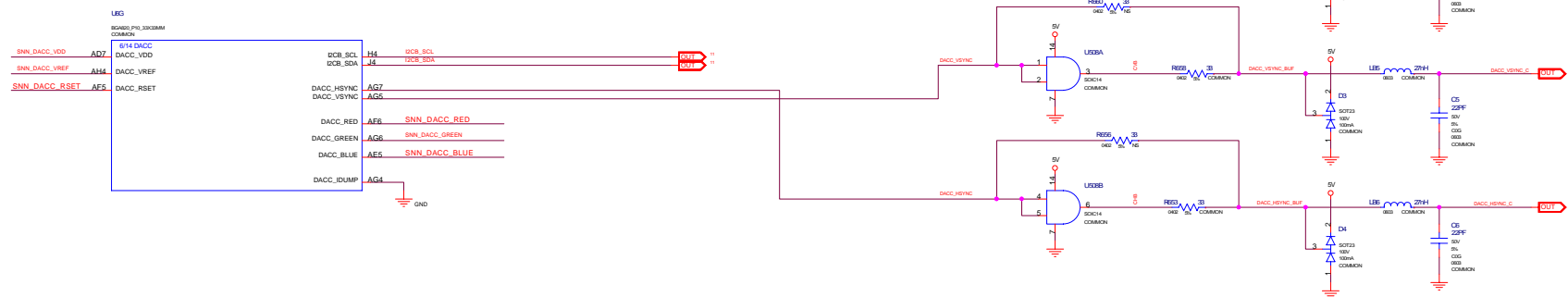
Note that this is the highest impedance on the net

Change for G72
C744 0.1u
R564 124ohm
R563 1.78Kohm



2 DACC - VGA

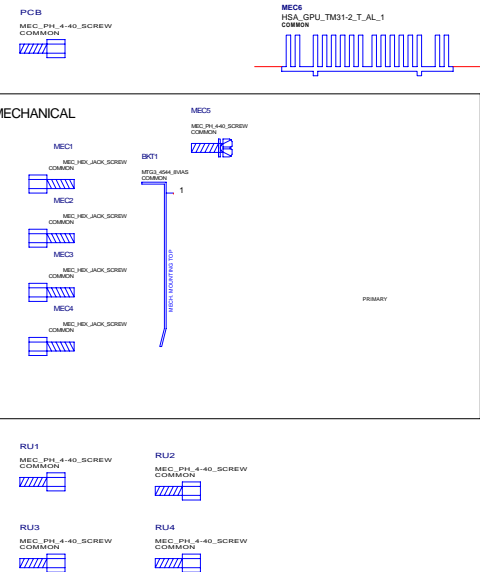
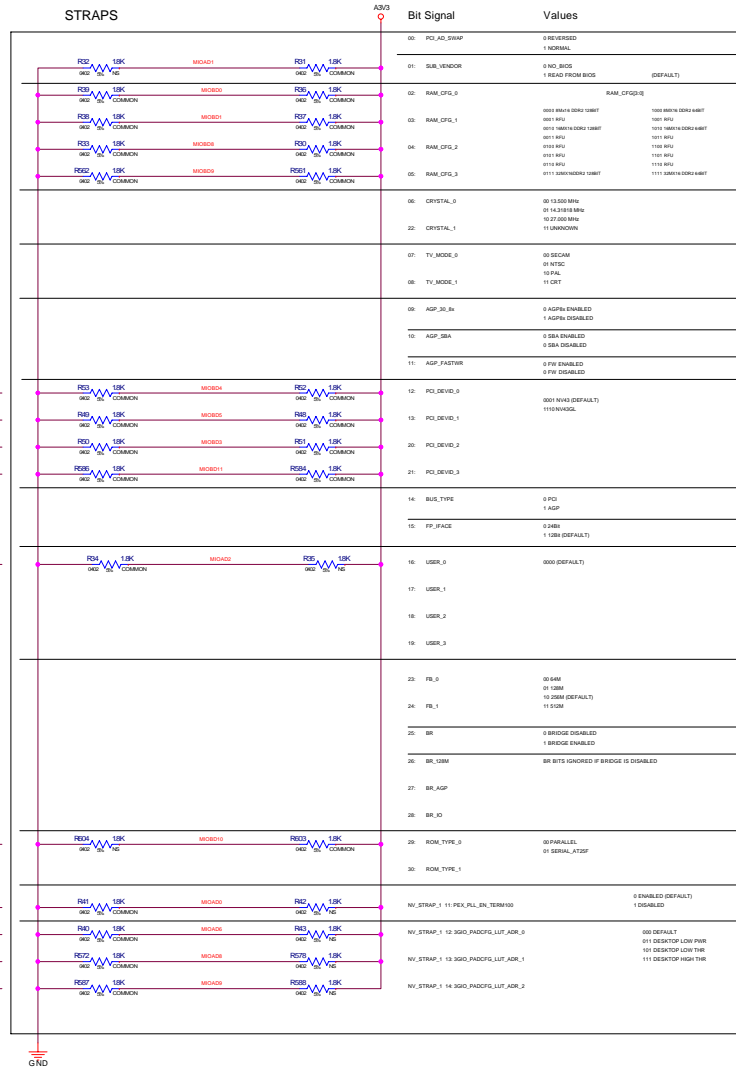
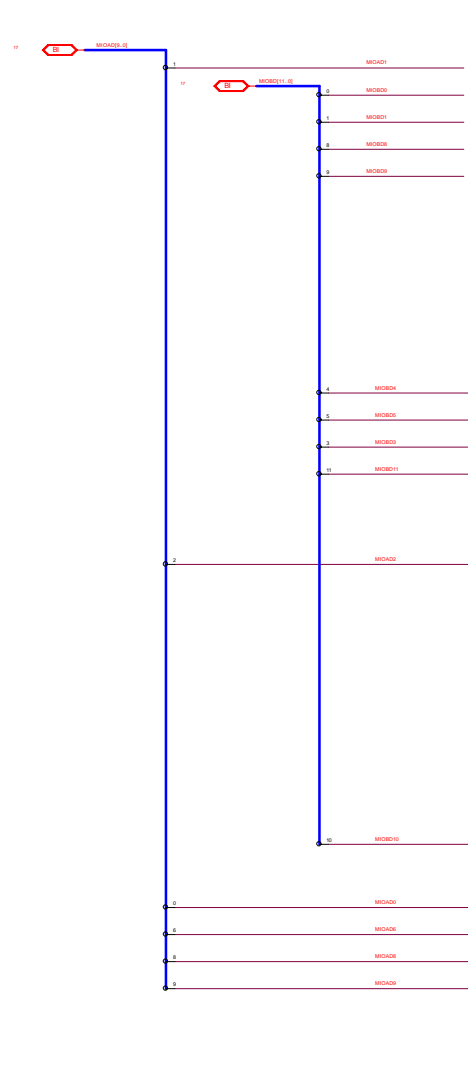
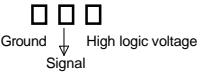
NET_NAME	MIN_WIDTH	NET_SPACING_RULE	NV_CRITICAL_NET	NV_IMPEDANCE
DCC_BCL				
DCC_BSA				
DACC_SCL				
DACC_HEYING		2	SIGM	
DACC_VERNIC		2	SIGM	
DACC_HSTING_RUP		2	SIGM	
DACC_VETNIC_RUP		2	SIGM	
DACC_OTPIC_C		2	SIGM	
DACC_HSTING_C		2	SIGM	
CHE		2	SIGM	
KVE		2	SIGM	
DACC_RED		1	SIGM	
DACC_GREEN		1	SIGM	
DACC_BLUE		1	SIGM	
DACC_X_F		1	SIGM	
DACC_X_T		1	SIGM	
DACC_X_F		1	SIGM	
DACC_REE_E		1	SIGM	
DACC_GREEN_C		1	SIGM	
DACC_BLUE_C		1	SIGM	
DACC_VDD	10			
DACC_VREF	50			
DACC_RESET	50			



13 STRAPS, FANSINK, MECHANICALS

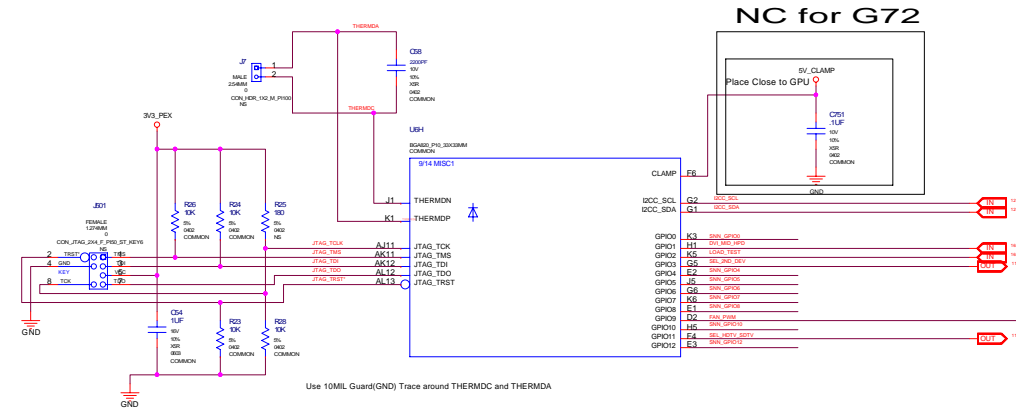
Overlap pads to save space
and to prevent assembly of
both resistors.

Layout



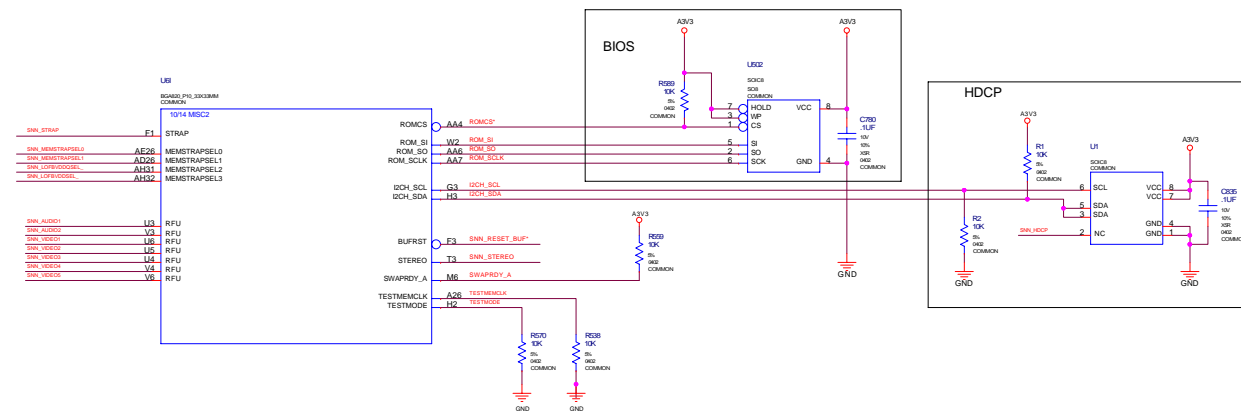
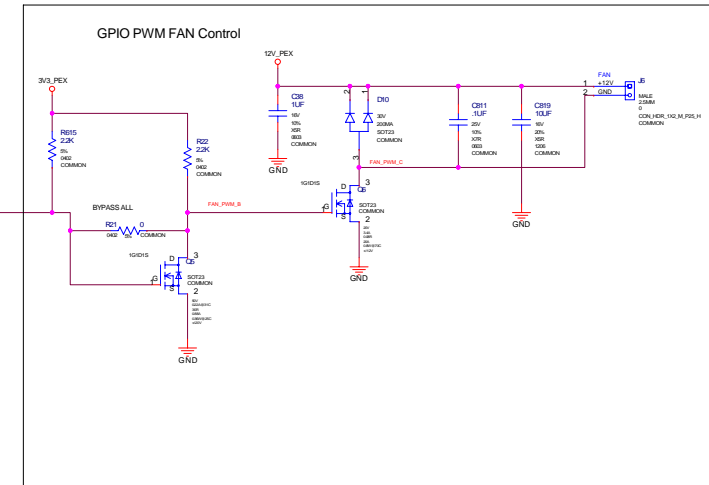
14 GPIO, HDCP, VBIOS, FAN CON

JTAG, GPIO, BIOS ROM



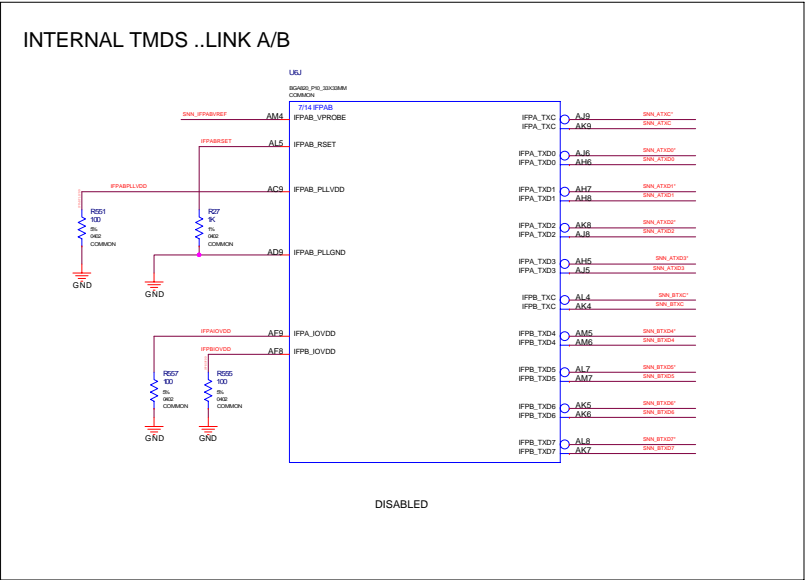
GPIO	I/O	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	RESERVED
2	IN	RESERVED
3	IN	RESERVED
4	IN	RESERVED
5	IN	RESERVED
6	IN	RESERVED
7	IN	RESERVED
8	IN	THERM ALERT/SLOW
9	OUT	FAN CONTROL
10	IN	RESERVED
11	OUT	NOTIFY/SEV SELECT
12	IN	RESERVED

NET	MIN_LINE_WIDTH
FAN_THRDS_BUPSES	10
FAN_ZONE	10
FAN_ZONE_B	10
FAN_ZONE_C	10
THRMDC	10
THRMDC2	10

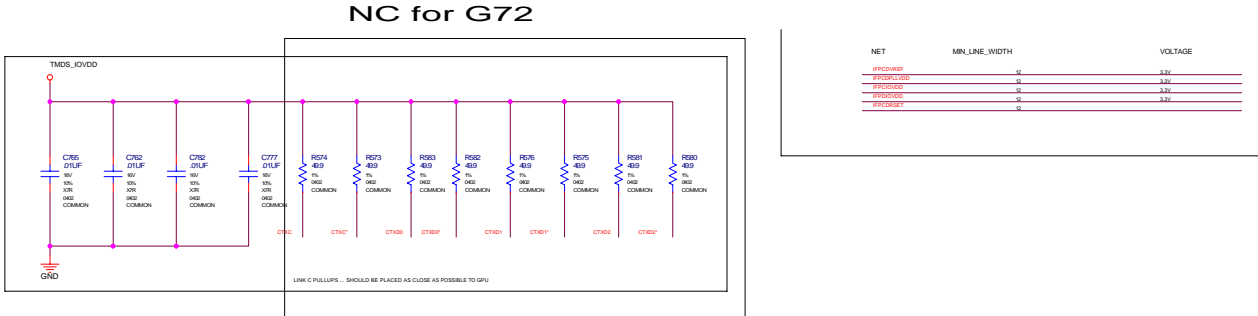


15 INTERNAL TMDS LINK A/B

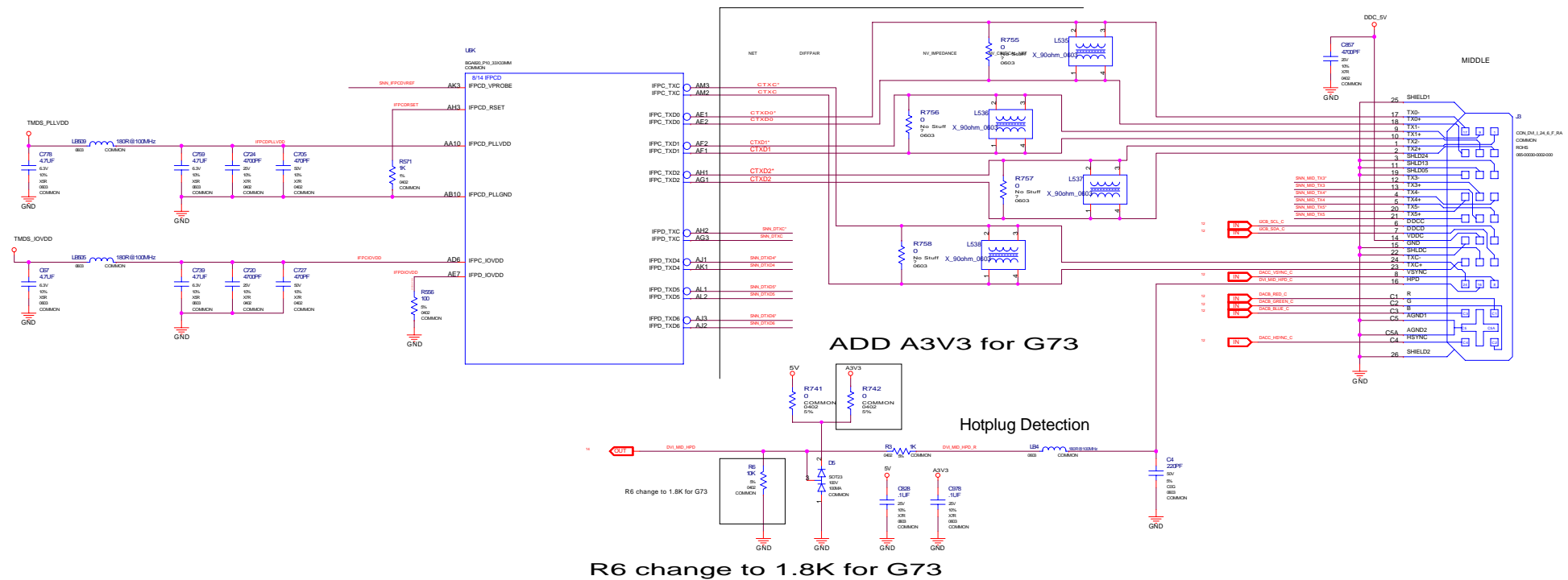
NET	MIN_LINE_WIDTH
IFPABSET	12
IFPABLLVDD	12
IFPABVDD	12
IFPBIOVDD	12



16 INTERNAL TMDS LINK C/D



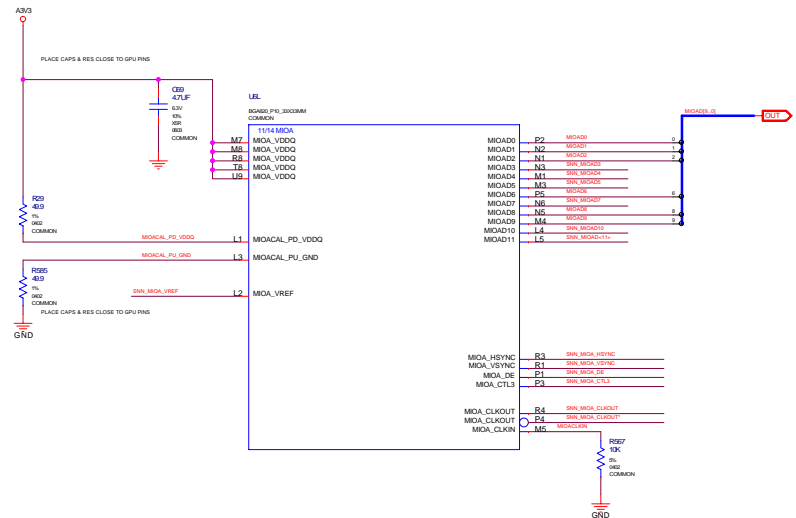
INTERNAL TMDS ..LINK C



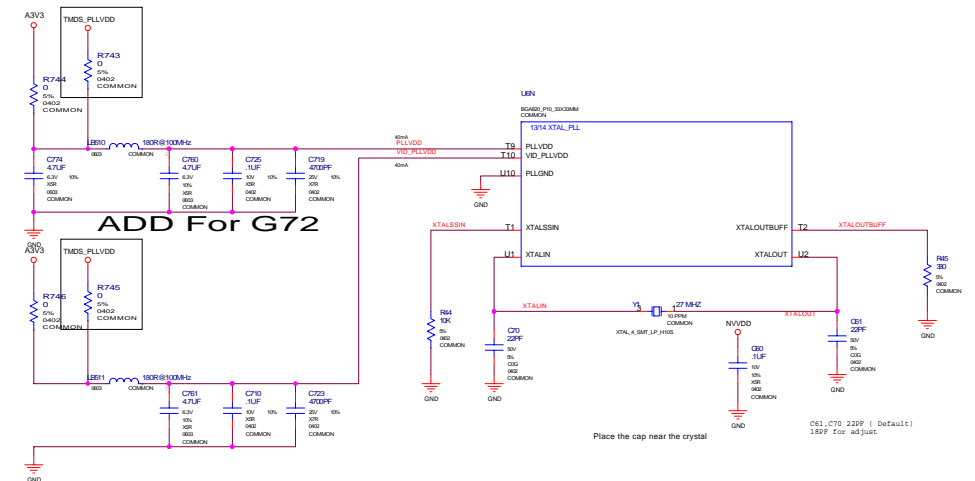
R6 change to 1.8K for G73

17 MIOA, MIOB, NVPLL

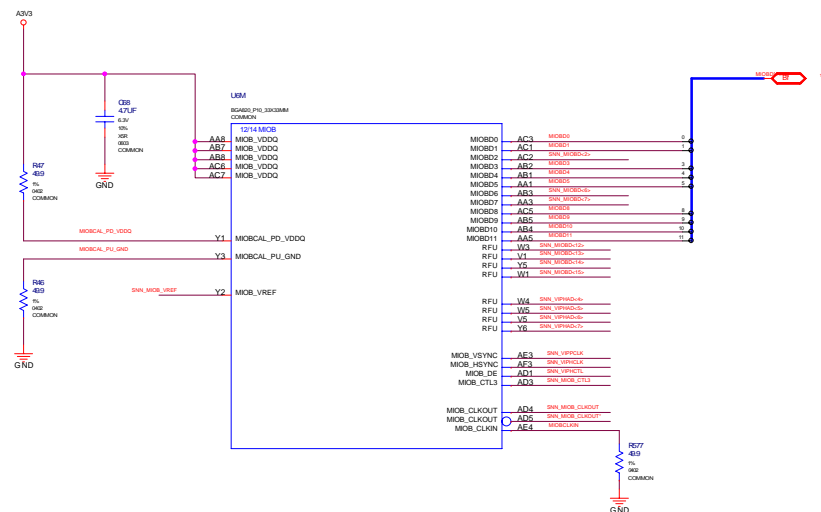
MIOA



XTAL/PLLVD
ADD For G72



MIOB



NET	MIN_LINE_WIDTH
VIO_PLLVDD	12
XTALIN	
XTALOUT	
PLLVD0	12



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Size	Document Number
Custom	MIOA, MIOB, NVPLL

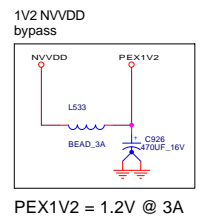
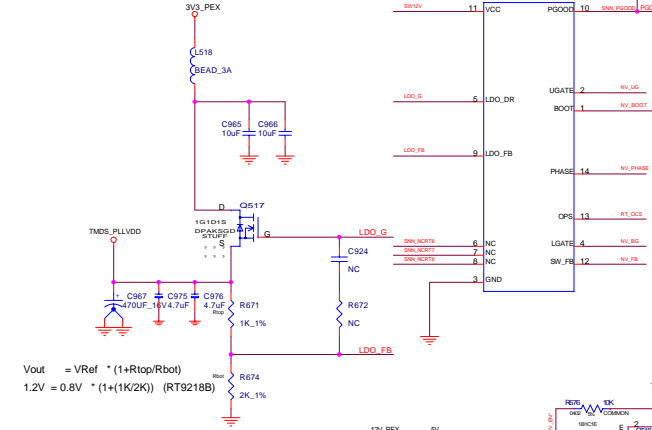
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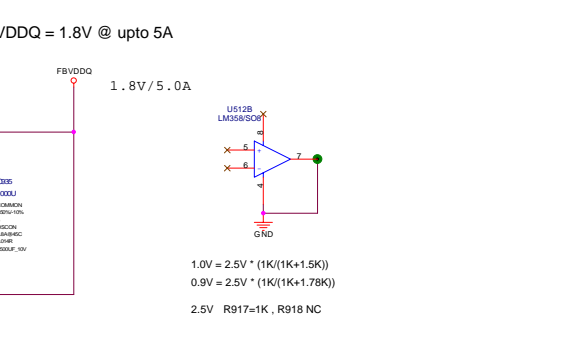
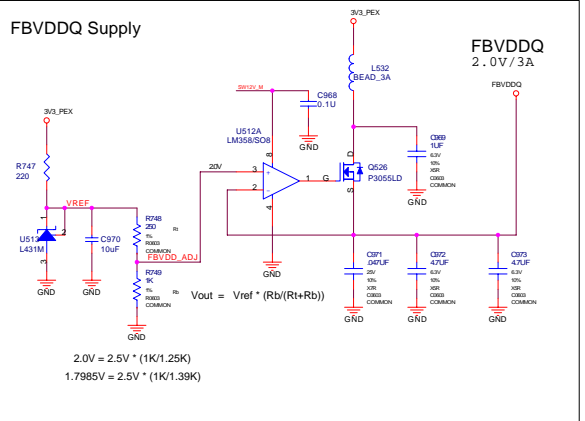
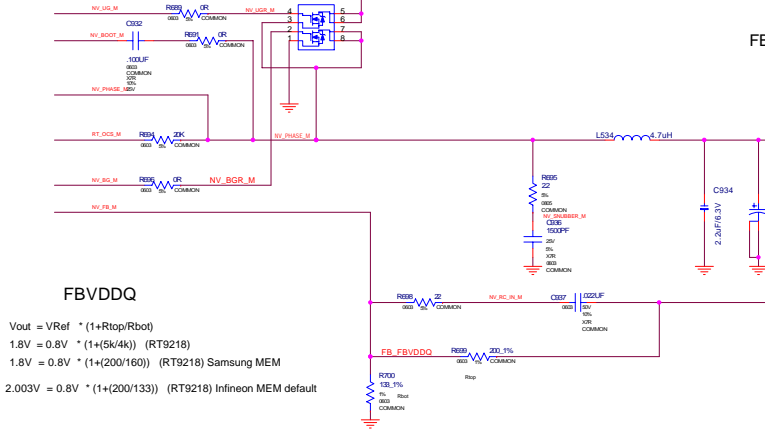
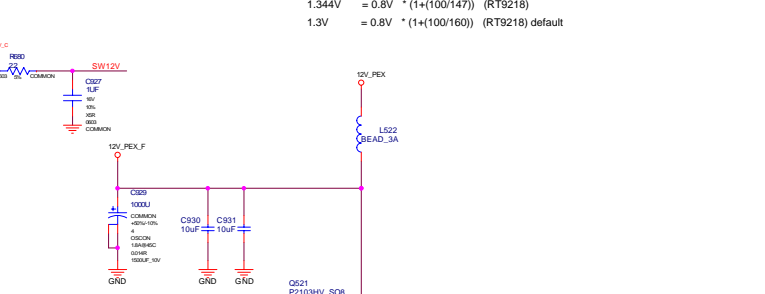
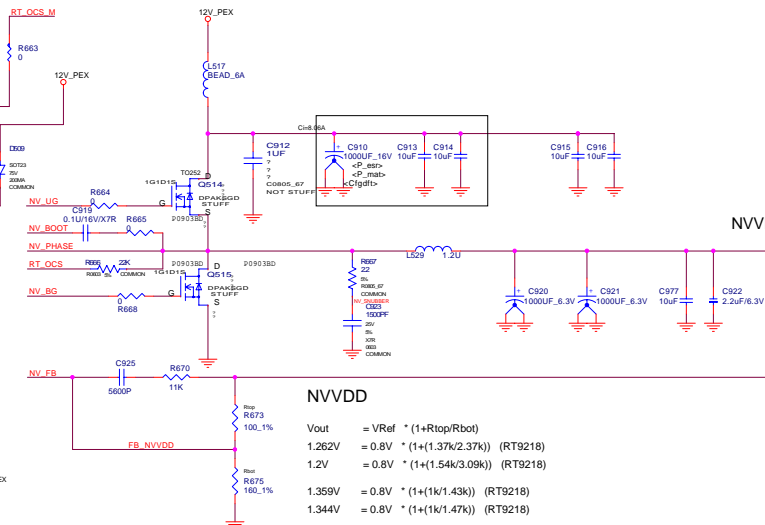
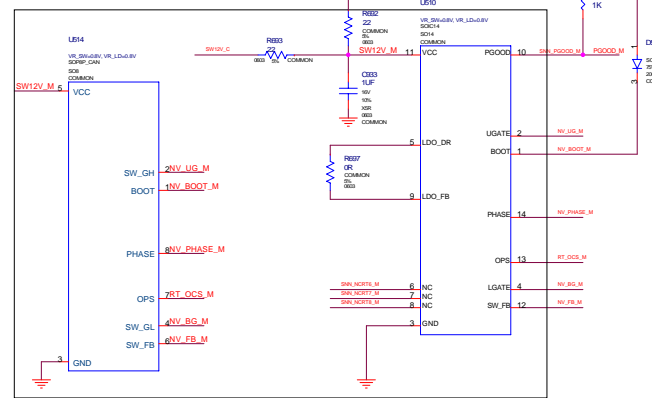
18 Power Supply (RT9218)

NVVD, PEX1V2, FBVDDQ

NV-Standard use FBVDDQ ,
Can't use RT9218 PGood power sequence
BOM added L821,C905
removed L819



Choose RT9218 PGood power sequence
Added BOM R883,R904
Removed R905



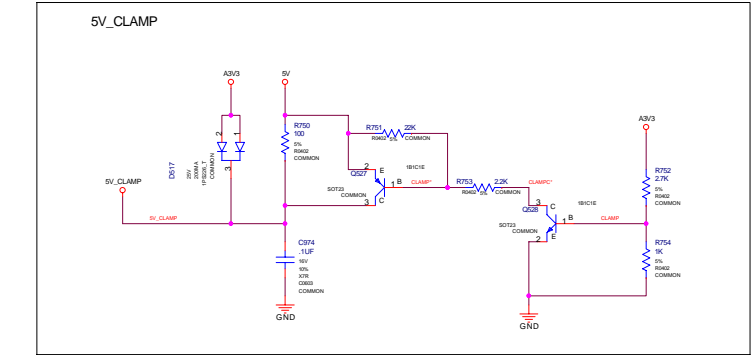
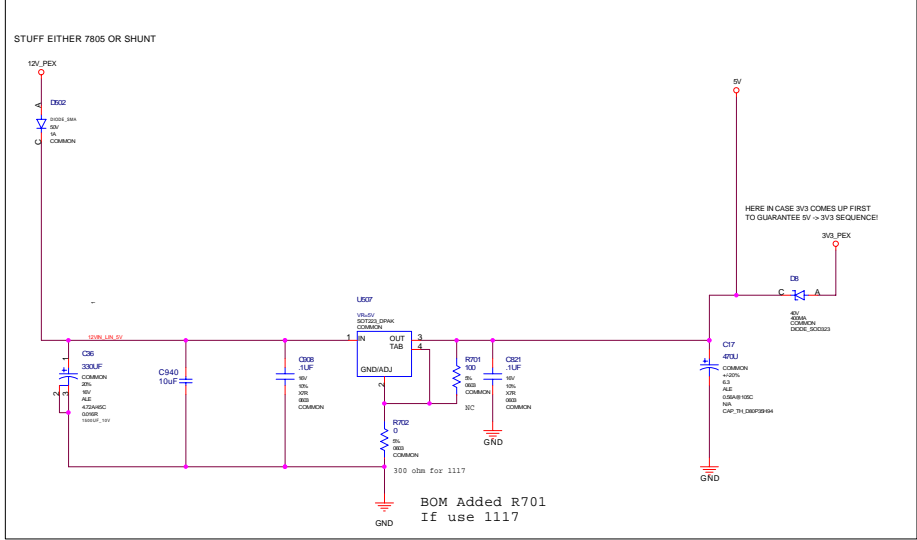
Net Name	MIN_LINE_WIDTH	VOLTAGE
5V	16	5V
NVVD	16	1.35V
12V_PEX	20	12V
PEX1V2	4	1.2V
12V_PEX_FILTER	16	12V
FBVTT	16	FBVTT2.0V

DRIVE3_1V2	20
UGATE_1	20
UGATE_2	20
UGATE_3	20
NODE_1	20
NODE_2	20
12V_PEX	20
BATTERY_VDD	20
COMPT_NVVD	10
COMPT_5V	10
COMPT_1V2	10
PEX1V2	10
REFIN_5V	10
REFIN_1V2	10
VREF_3V3	10
PEX1V2	10
BODY_1	10
BODY_2	10
FREQ_SEV	20
SS_NVVD	10
SS_1V2	10
UGATE_1_RS	20
UGATE_2_RS	20
COMPT_1V2	10
COMPT_5V	10
NVVD_RS	10
1V2_RS	10
NODE_1_SINUS	20
NODE_2_SINUS	20
UGATE_1	20
BODY_1	20
SWITCH1	20

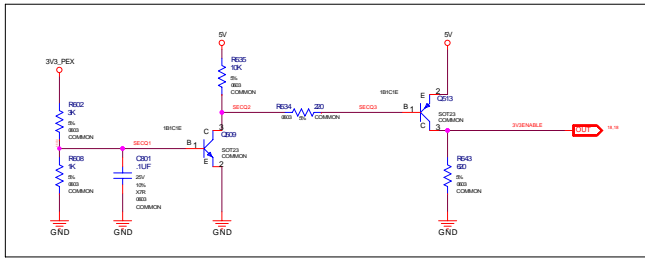
19 Others Power Supply (Linears)

5V,FBVDDQ,A3V3,3V3,TMDS_PLLVDD,TMDS_IOVDD,FBVTT

5V LOW COST REGULATOR

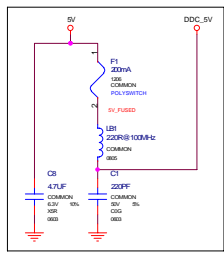


Power Sequencing

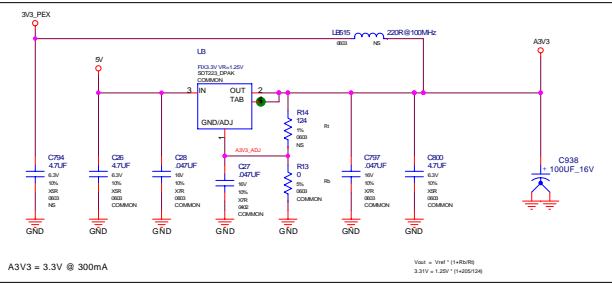


5V AND PEX3V3 UP ... ALL OTHER LINEARS UP

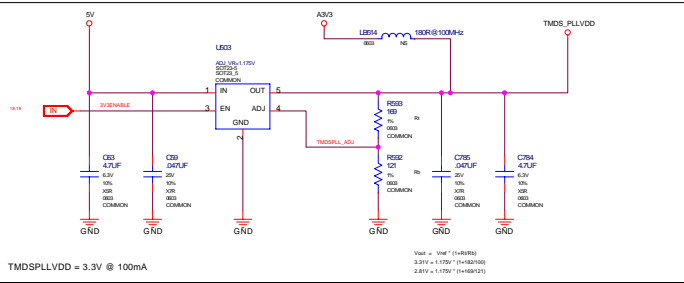
DDC 5V



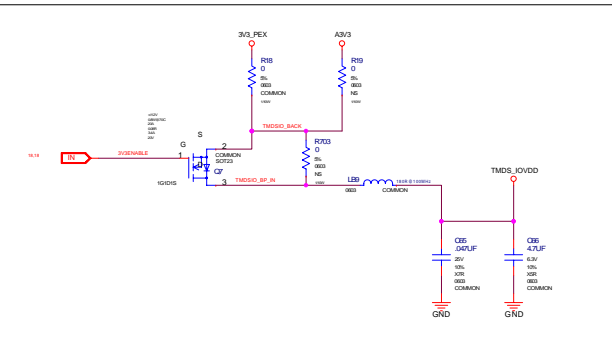
A3V3 Power Supply



TMDS PLL Supply



TMDS IO SUPPLY WITH BACKDRIVE PROTECTION



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Others Power Supply (Linears)

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