

V133-10

P729: G96, DDR2 MEMORY 32MX16/16MX16

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REV	VARIANT	WFPN	ASSEMBLY
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REV HISTORY

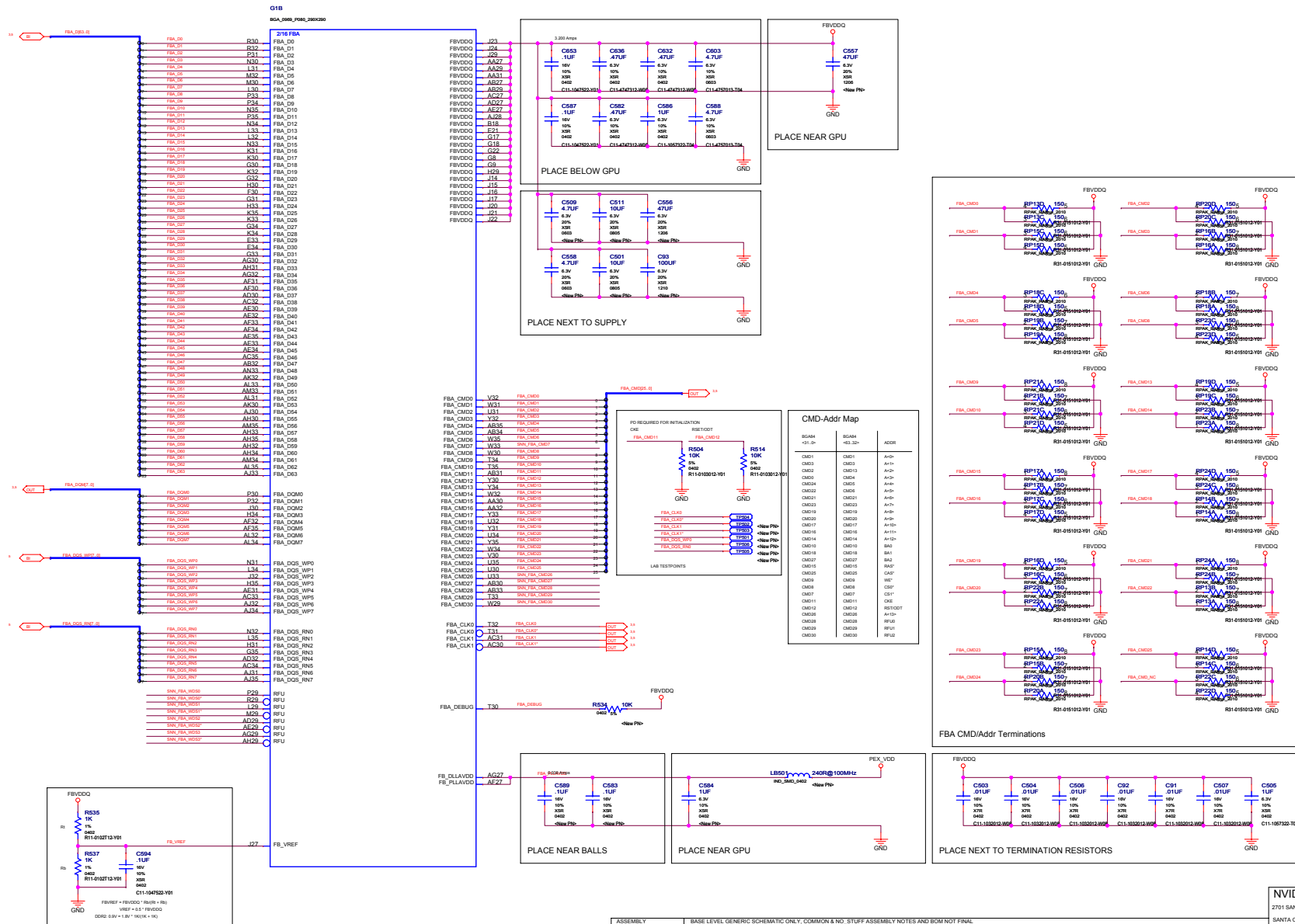
- Modify Power Sequencing
02/25
- PAGE 14.EDIT NET
R562 : I2CD_SCL_R to I2CC_SCL_R
R563 : I2CD_SDA_R to I2CC_SDA_R
R172,R173 Pull high 5V
- PAGE 19.change footprint
C87 footprint 0805 to 1206
- PAGE 11.Remove R130
HDMI gate pull down
- 02/26
- PAGE 2.Change 3V3_PEX to 3V3_AUX
- 03/03
- PAGE 11.Add commond chock
L21,L22,L23,L24
- PAGE 18.Change AZ7805 footprint to TO263
- 03/04
- PAGE 13.Remove SLI CN1 circuit
Change MIOB_VDD to 3V3_PEX
- PAGE 16.Change pullhigh to 3V3_PEX
- PAGE 19.Change C29 to 1500uF
Add CAP C24 C37 1500uF
Add CAP C60 C63 1500uF
Change Chock L10,L11 footprint
- 03/04
- PAGE 18.Change 1V8 circuit
Remove
C96,C156,C157,C158,C159,C160,C161,C162,C163
Q30,R152,R153,R154,R155,R156,R157
- 03/07
- PAGE 14.Add BAV99 D21,D22,D23,D24,D25,D26
PAGE 20.Change NVVDD circuit
Remove R517 R11-0101T12-C52
- 03/12
- PAGE 14.Add 2pin Fan control
PAGE 18.Change DDC_5V circuit
- 03/13
- PAGE 14.Remove J6
PAGE 15.Remove J8

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P729 Overview

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Partition A Frame Buffer Interface



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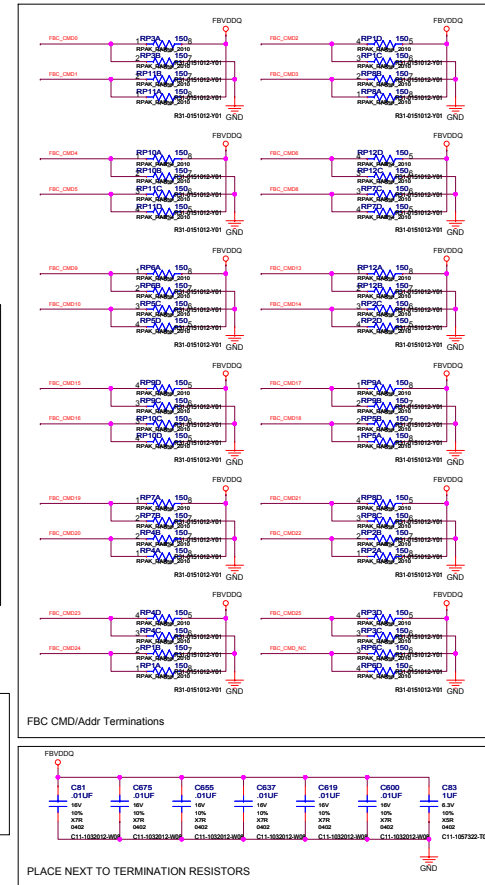
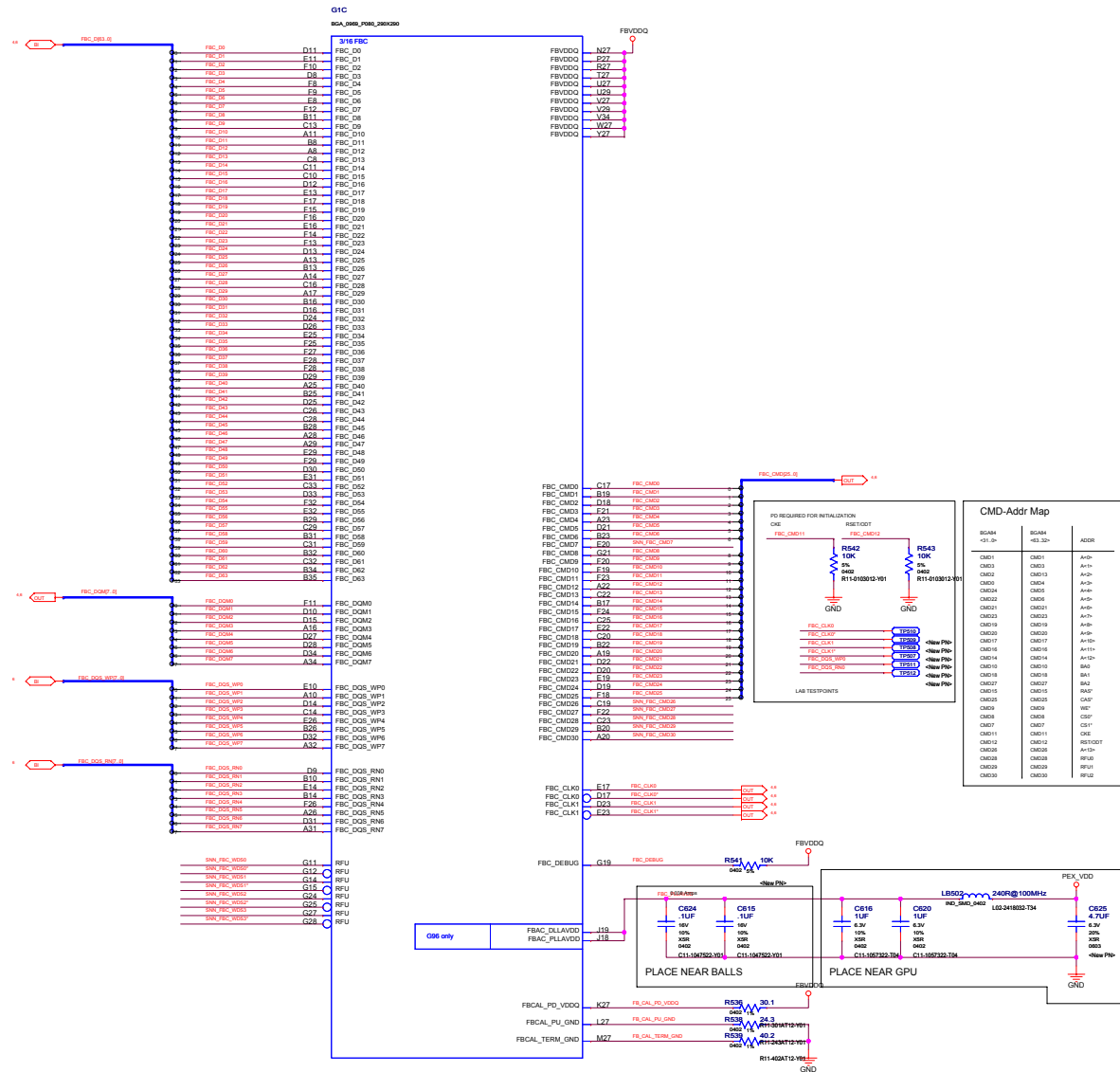
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PAGE DETAIL	Partition A Frame Buffer Interface

Partition C Frame Buffer Interface



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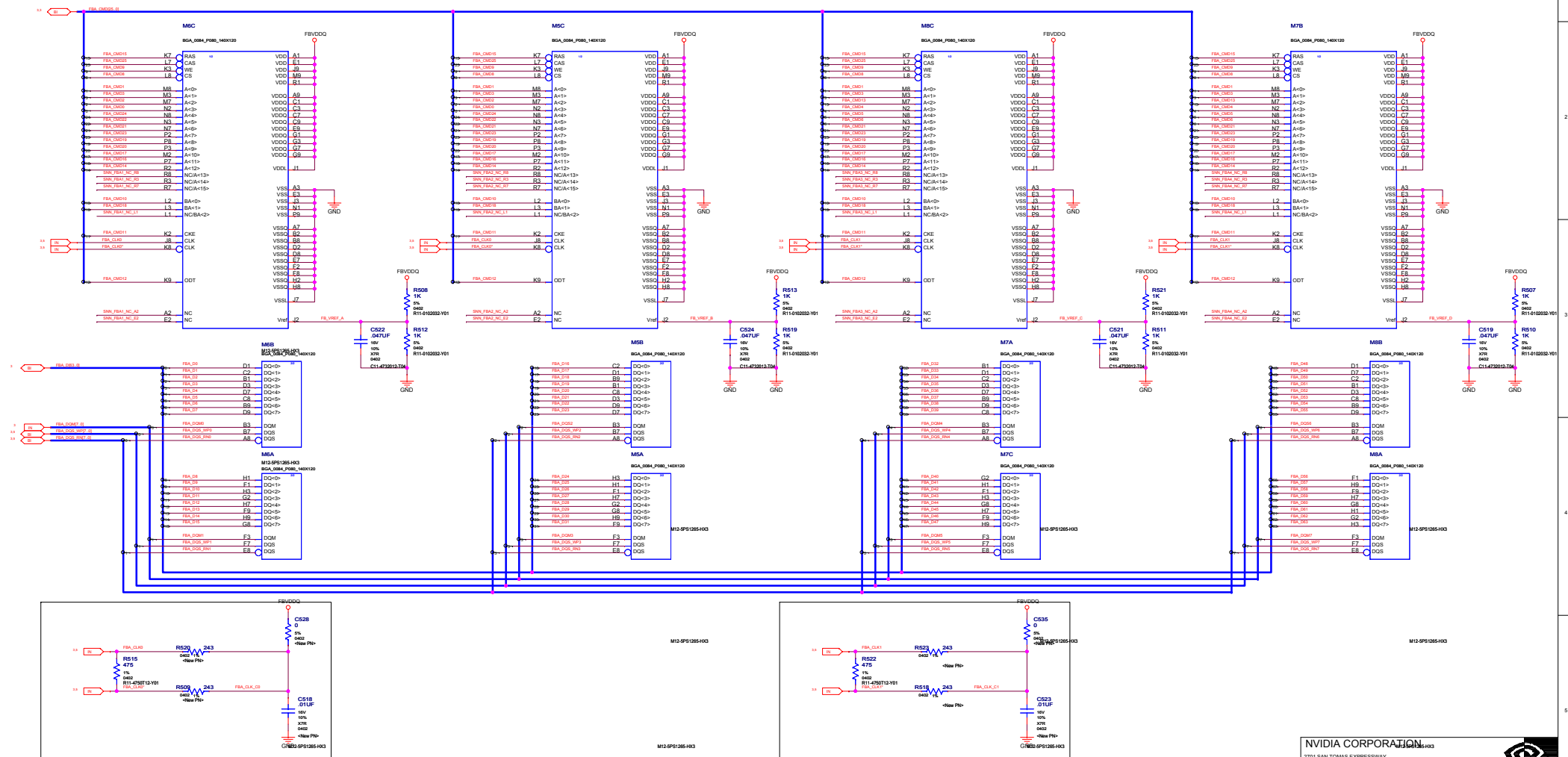
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PAGE DETAIL	Partition C Frame Buffer Interface

Partition A Memories



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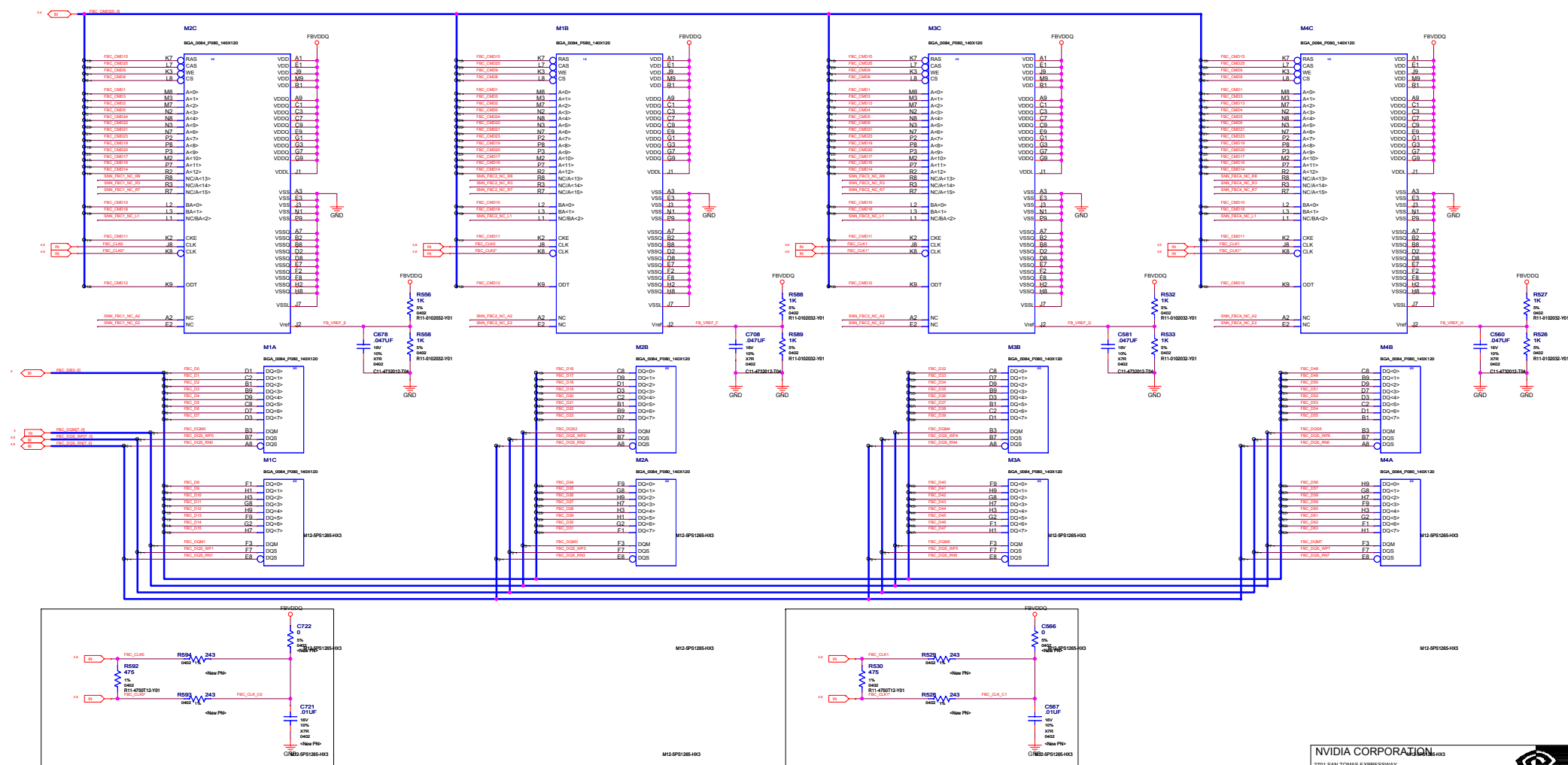
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NAME	DATE 26-OCT-2007



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PAGE DETAIL	Partition A Memories

Partition C Memories



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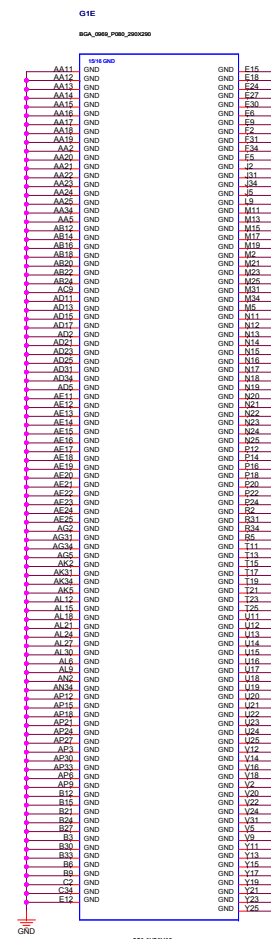
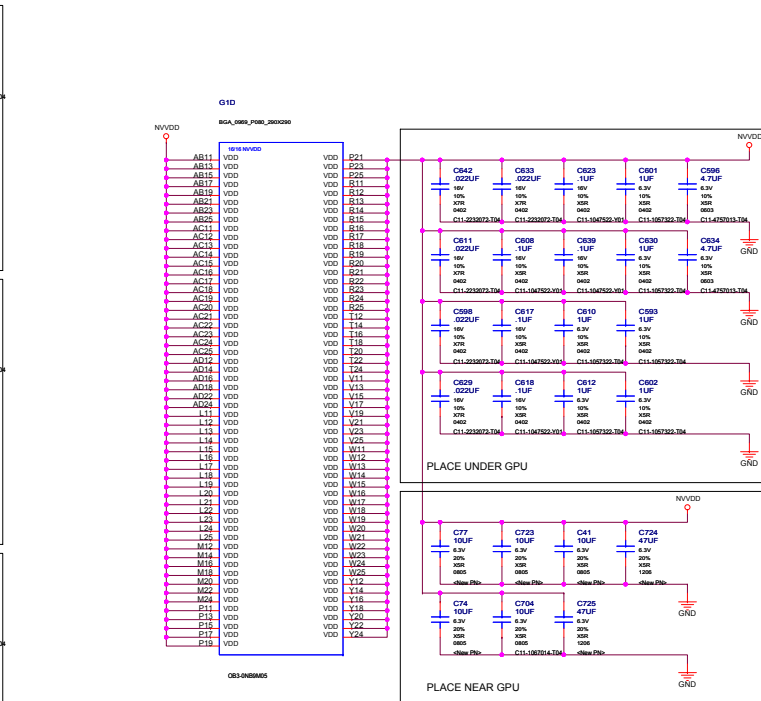
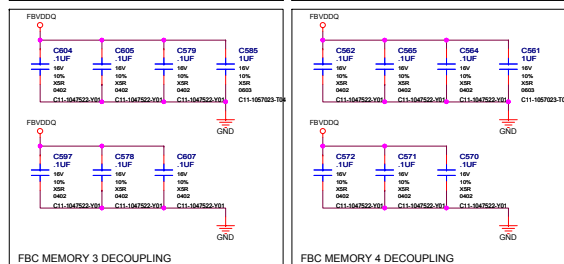
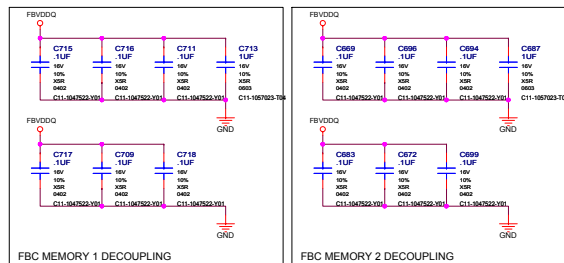
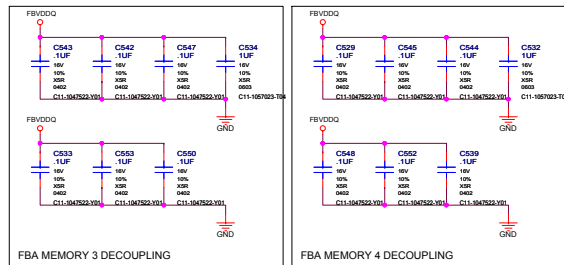
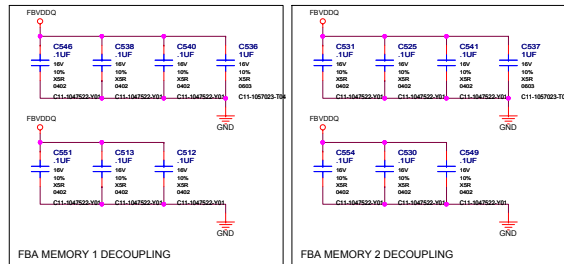
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PAGE DETAIL	Partition C Memories

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Decoupling Caps



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PAGE DETAIL	Decoupling Caps

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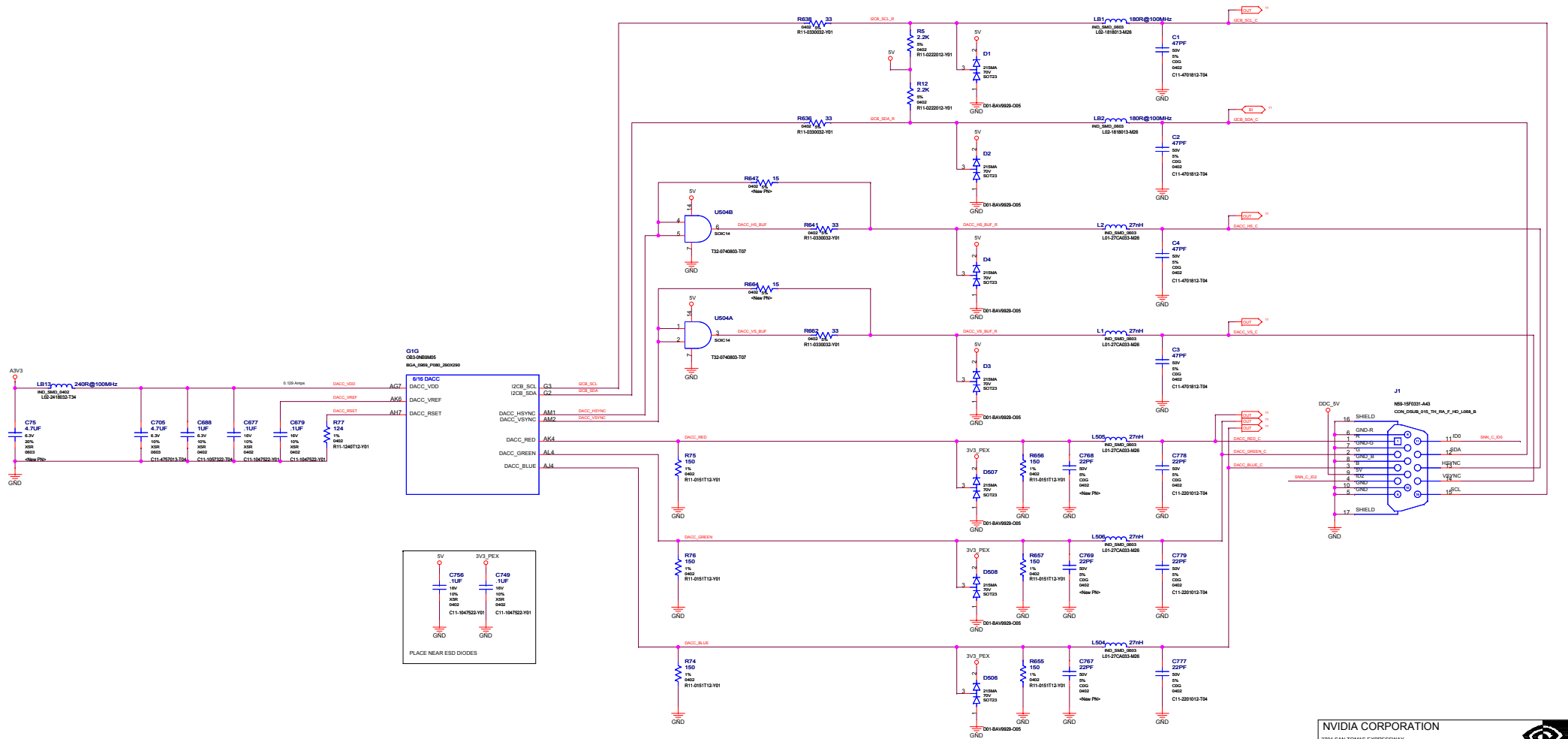
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DACC, Slim DB15 Connector



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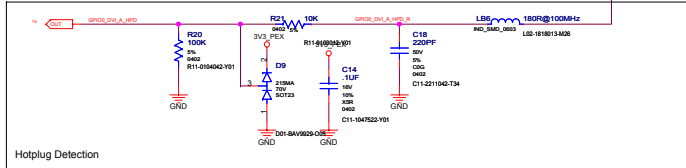
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO _STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC, Slim DB15 Connector

change FBVDDQ to 1V8

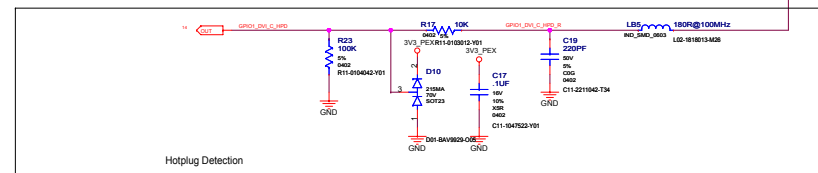
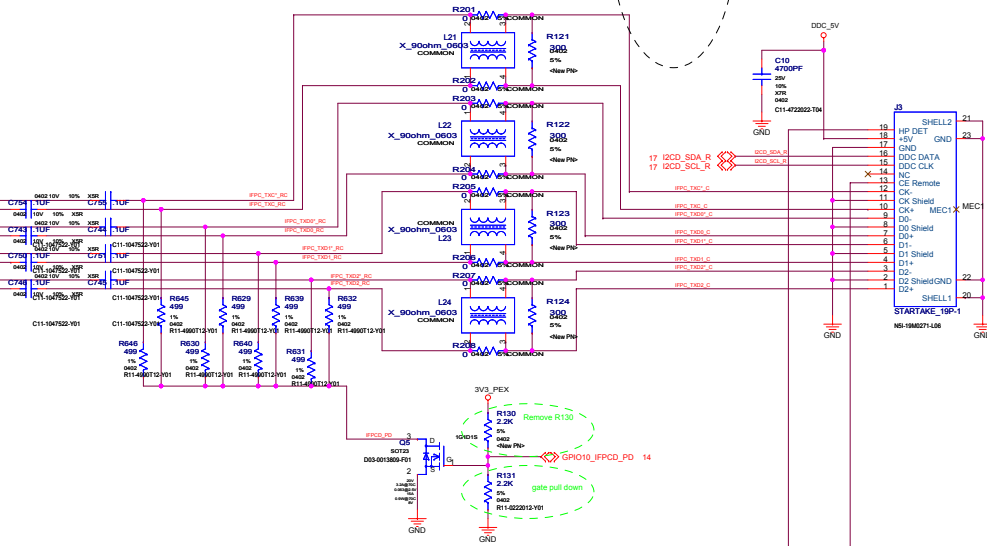
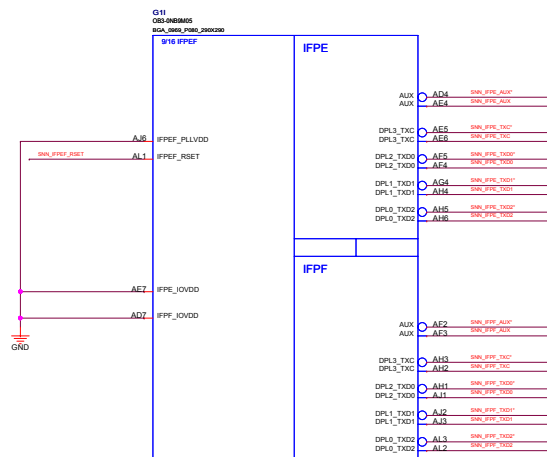
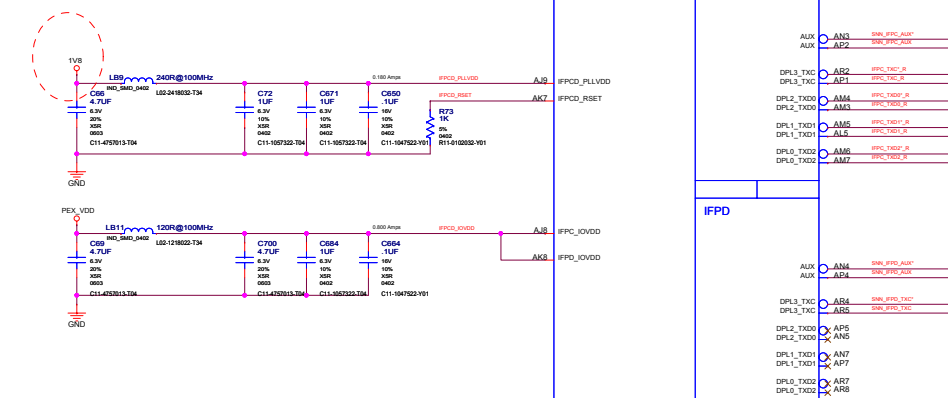


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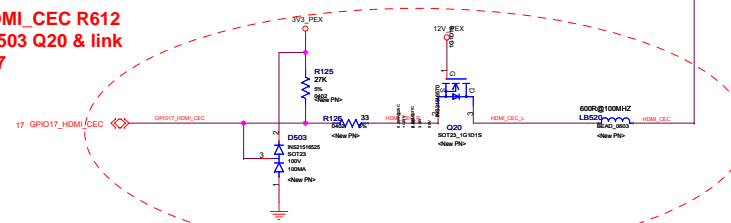
Internal TMDS .. Link C & D

add EMI bridge


Change DVI to HDMI



Add HDMI_CEC R612
R613 D503 Q20 & link
GPIO 17



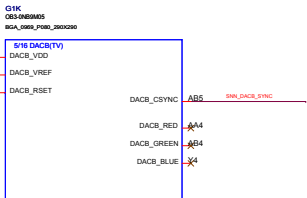
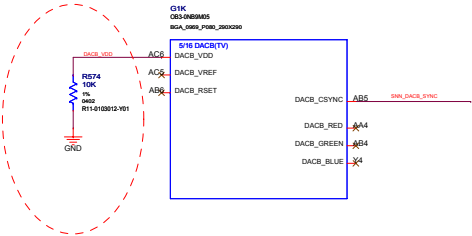
CEC pullup and damping must be disconnected from HDMI connector when Power d

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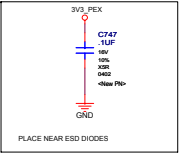
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DACB, MINIDIN Connector

Change R574 to 10K



Remove TV-OUT



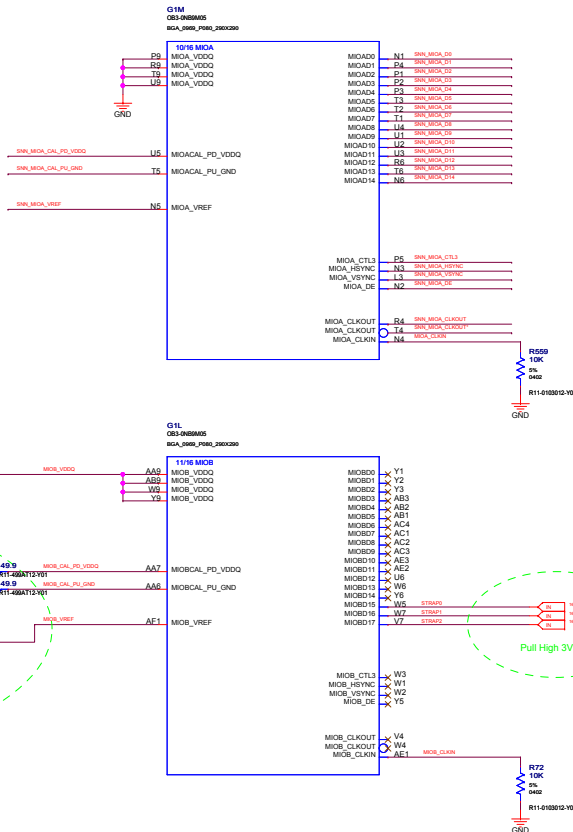
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ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL: DACB, MINIDIN Connector

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MIOA, MIOB Interface



Change A2V5 to 3V3_PEX

Remove component

Pull High 3V3_PEX

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MOA, MIOB Interface

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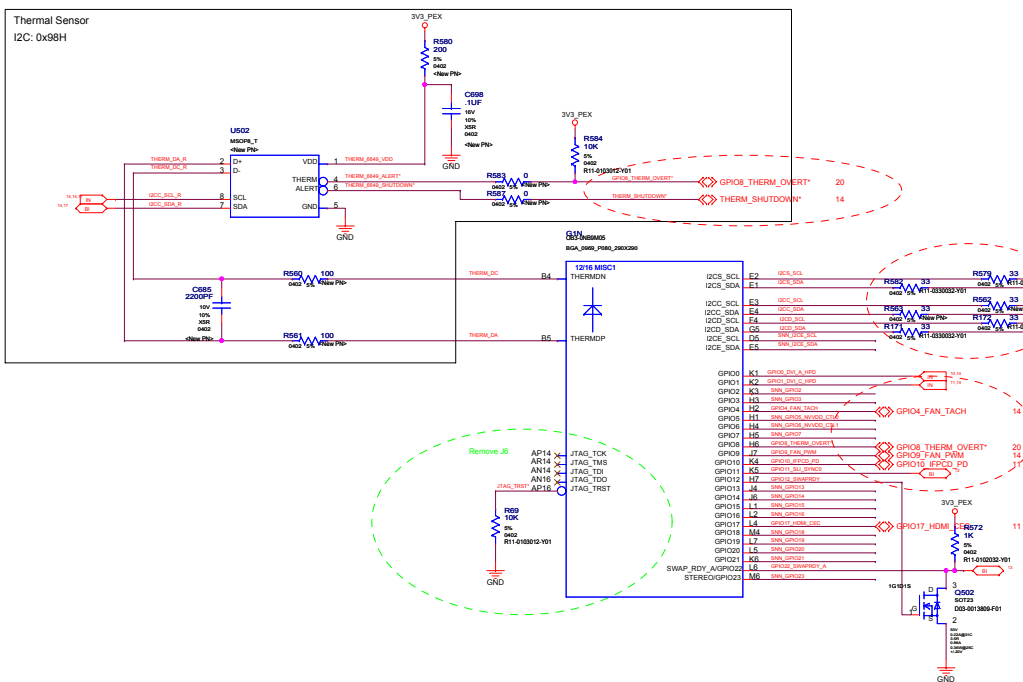


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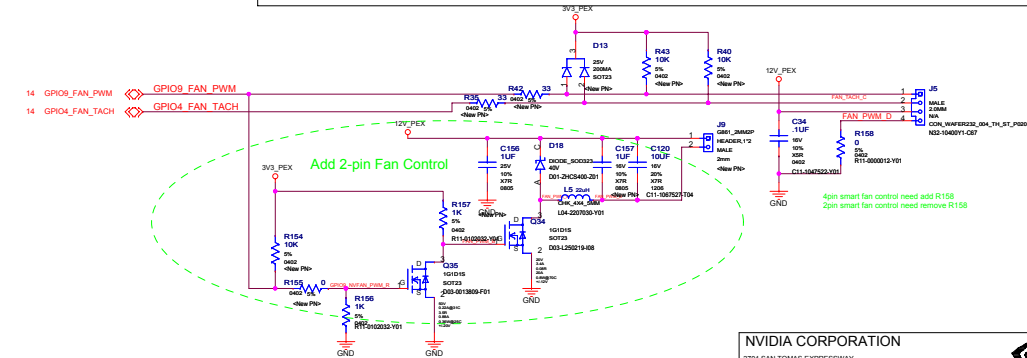
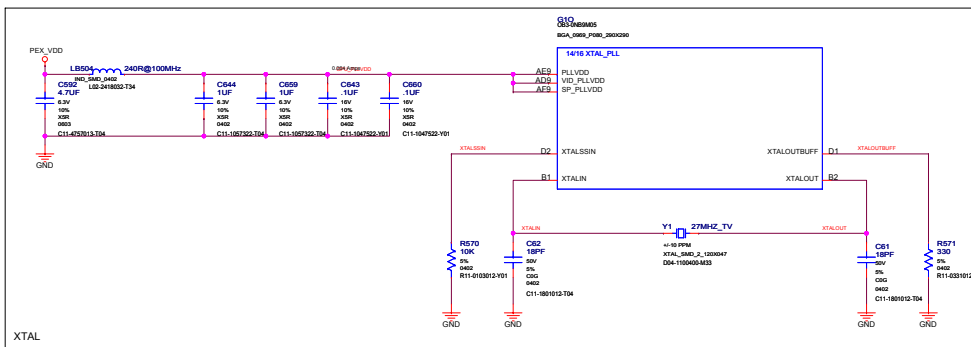
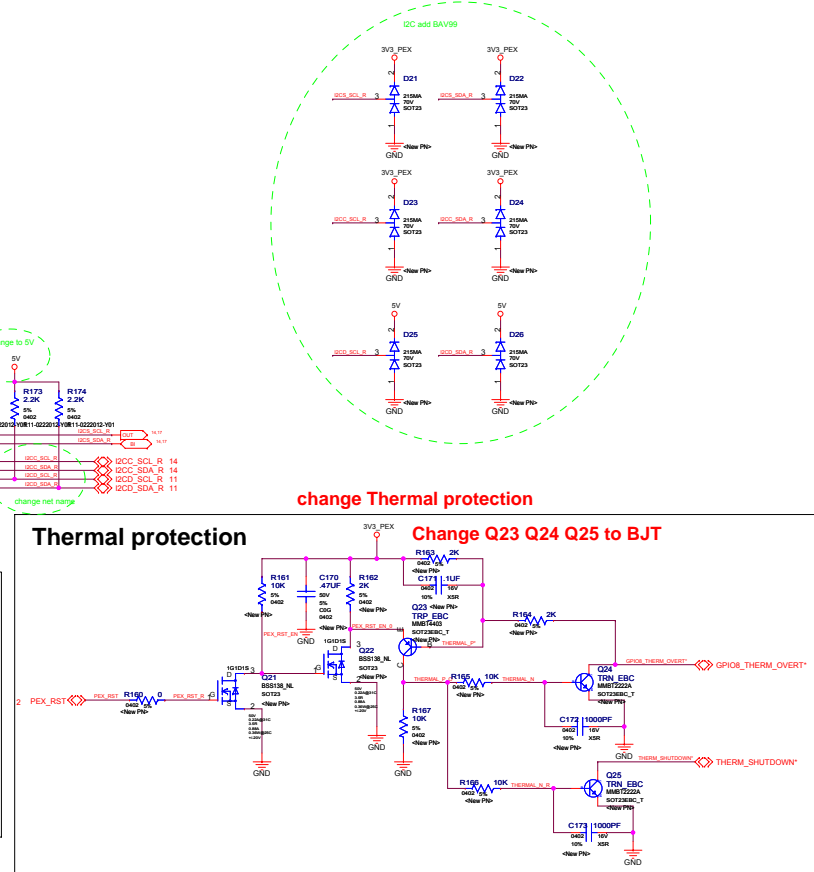
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Thermal Sensors, GPIOs, XTAL, JTAG, Fan



GPIO Table		
GPIO	I/O	Function
0	IN	ENX SOUTH HOTPLUG DETECT
1	IN	DVI MD HOTPLUG DETECT
2		
3		
4	OUT	FWM FAN
5	OUT	MOVED VOLTAGE SELECT 0
6	OUT	MOVED VOLTAGE SELECT 1
7		
8	IN	THERMAL SLOWDOWN
9	IN	FAN TACH
10		
11	INOUT	RASER SYNC 0
12	OUT	SWAP READY 0
13		
14		
15		
16		
17		
18		
19		
20		
21	IN	SWAP READY IN
22		
23		



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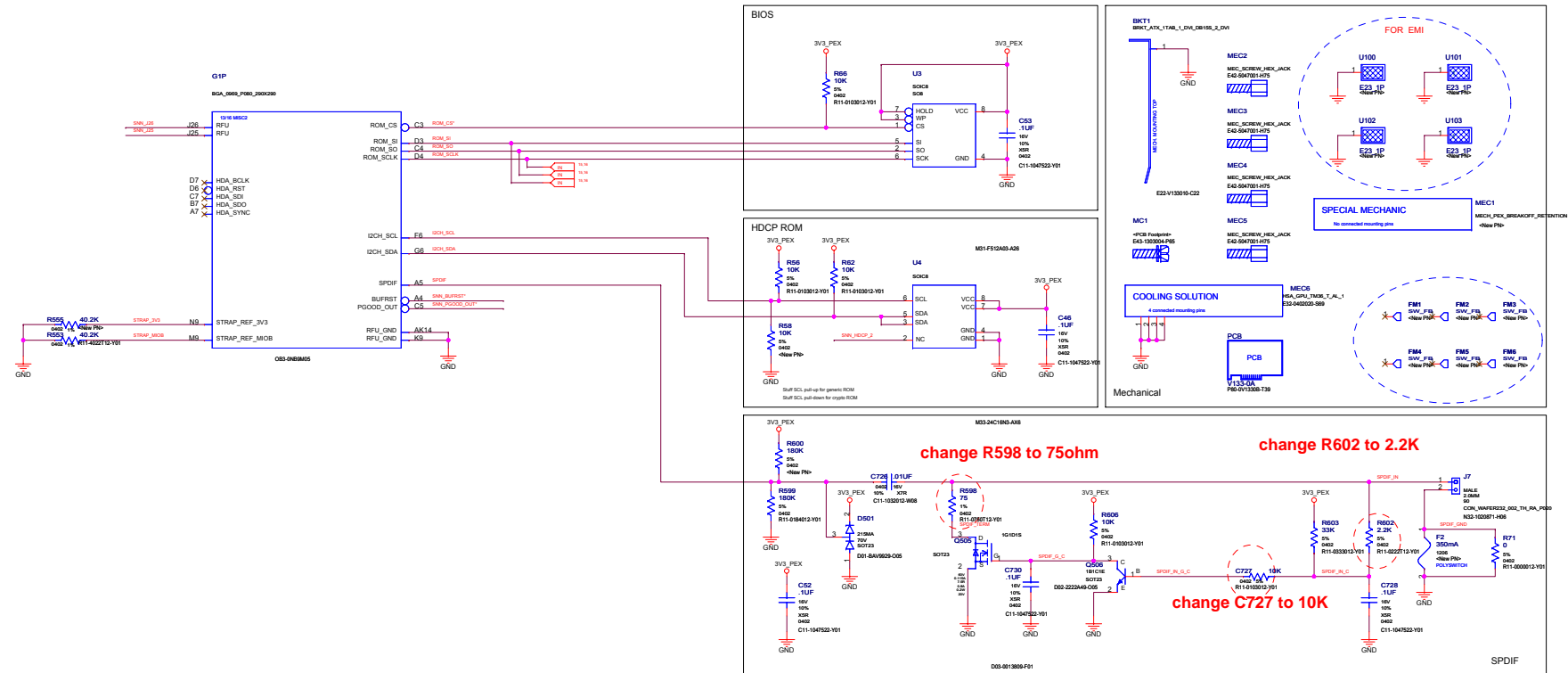
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Sensors, GPIOs, XTAL, JT4G, Fan

BIOS, HDCP, SPDIF, HDA, Mechanical



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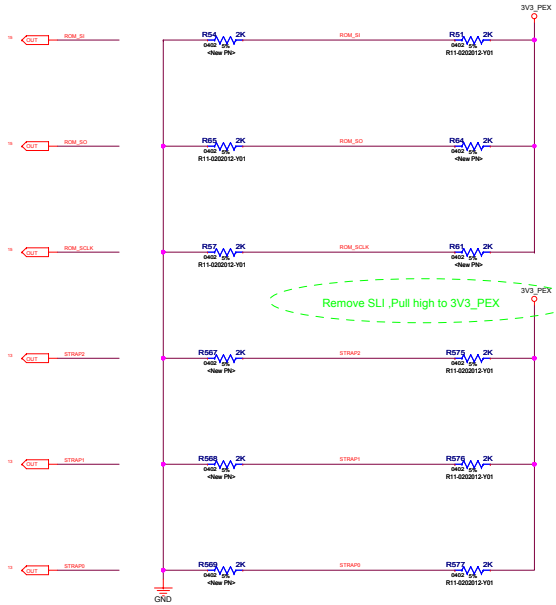
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS, HDCP, SPDIF, HDA, Mechanical

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A	B	C	D	E	F	G	H
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Straps



G94 Straps Multilevel Mode

Bit Signal

Values

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01	TWADD1	010 PAL_M 011 PAL_N 100 PAL_CK 101 PAL_BCD0 110 BCD0REV00 111 BCD0REV01
00	TWADD0	
03	PCL_DEV0_EXT	1 G00-300-A1
02	SUB_VENDOR	0 NO BIOS 1 BIOS
01	SLCT_CLK_CFG	0 DISABLE 1 ENABLE
00	PEX_PUL_DLA_TERM100	0 DIS 1 EN

Multilevel Straps

5K to GND	0000
10K to GND	0001
15K to GND	0010
20K to GND	0011
25K to GND	0100
30K to GND	0101
35K to GND	0110
40K to GND	0111
5K to VCC	1000
10K to VCC	1001
15K to VCC	1010
20K to VCC	1011
25K to VCC	1100
30K to VCC	1101
35K to VCC	1110
40K to VCC	1111

03:	RAMCFG[0]	0000 32Mx16/16Mx16 DDR2 128-bit Elgote 0001 16Mx16 DDR2 128-bit Samsung, Micron 0010 16Mx16 DDR2 128-bit G4 0011 16Mx16 DDR2 128-bit Hynix 0100 32Mx16/16Mx16 DDR2 128-bit Nanya 0101 32Mx16/16Mx16 DDR2 128-bit Samsung 0110 32Mx16/16Mx16 DDR2 128-bit G4 0111 32Mx16/16Mx16 DDR2 128-bit Hynix	1000 32Mx16/16Mx16 DDR2 64-bit Elgote 1001 16Mx16 DDR2 64-bit Samsung, Micron 1010 16Mx16 DDR2 64-bit G4 1011 16Mx16 DDR2 64-bit Hynix 1100 32Mx16/16Mx16 DDR2 64-bit Nanya 1101 32Mx16/16Mx16 DDR2 64-bit Samsung 1110 32Mx16/16Mx16 DDR2 64-bit G4 1111 32Mx16/16Mx16 DDR2 64-bit Hynix
02:	RAMCFG[0]		
01:	RAMCFG[0]		

0111 32Mx16 DDR2 128-bit Hynix

03	PCL_DEV00	0001 G00-300-A1	
02	PCL_DEV01		
01	PCL_DEV02		
00	PCL_DEV03		
03	SDIO_PANDCFG_LUT_ADR0	0000 G0KTOP_DEFAULT 0001 MOBILE_DEFAULT 0010 MOBILE_JTTRES_LLAMP 0011 MOBILE_JTTRES_LLAMP 0100 MOBILE_JTTRES_HAMP 0101 MOBILE_JTTRES_HAMP 0110 MOBILE_JTTRES_HAMP 0111 MOBILE_JTTRES_HAMP	1000 G0KTOP_JTTRES 1001 MOBILE_JTTRES_HAMP 1010 MOBILE_JTTRES_LLAMP 1011 MOBILE_JTTRES_LLAMP 1100 MOBILE_JTTRES_HAMP 1101 MOBILE_JTTRES_HAMP 1110 MOBILE_JTTRES_HAMP 1111 MOBILE_JTTRES_HAMP
02	SDIO_PANDCFG_LUT_ADR1		
01	SDIO_PANDCFG_LUT_ADR2		
00	SDIO_PANDCFG_LUT_ADR3		
03	USER0	0000 DEFAULT	
02	USER1		
01	USER2		
00	USER3		

G94 Straps Binary-Bringup Mode

Bit Signal

Values

SUB_VENDOR	0 NO BIOS 1 BIOS
SLCT_CLK_CFG	0 DISABLE 1 ENABLE
SDIO_PANDCFG_LUT_ADR0	0000 G0KTOP_DEFAULT 0001 MOBILE_JTTRES 0010 MOBILE_JTTRES_LLAMP 0011 MOBILE_JTTRES_LLAMP 0100 MOBILE_JTTRES_HAMP 0101 MOBILE_JTTRES_HAMP 0110 MOBILE_JTTRES_HAMP 0111 MOBILE_JTTRES_HAMP
SDIO_PANDCFG_LUT_ADR1	1000 G0KTOP_JTTRES 1001 MOBILE_JTTRES_HAMP 1010 MOBILE_JTTRES_LLAMP 1011 MOBILE_JTTRES_LLAMP 1100 MOBILE_JTTRES_HAMP 1101 MOBILE_JTTRES_HAMP 1110 MOBILE_JTTRES_HAMP 1111 MOBILE_JTTRES_HAMP
SDIO_PANDCFG_LUT_ADR2	
SDIO_PANDCFG_LUT_ADR3	

G94 Straps Binary-Production Mode

Bit Signal

Values

SLCT_CLK_CFG	0 DISABLE 1 ENABLE
PCL_DEV00_EXT	10 G00-300-A1
PCL_DEV00	
PCL_DEV01	
PCL_DEV02	
PCL_DEV03	
RAMCFG0	000 32Mx16/16Mx16 DDR2 E6xxx 001 16Mx16 DDR2 Samsung, Micron 010 16Mx16 DDR2 G4xxx 011 16Mx16 DDR2 Hynix 100 32Mx16/16Mx16 DDR2 Hynix 101 32Mx16/16Mx16 DDR2 Samsung 110 32Mx16/16Mx16 DDR2 G4xxx 111 32Mx16/16Mx16 DDR2 Hynix
RAMCFG1	
RAMCFG2	
RAMCFG3	

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ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Straps

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SANTA CLARA, CA 95050, USA

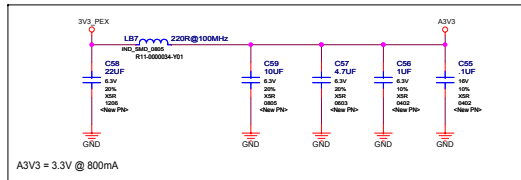
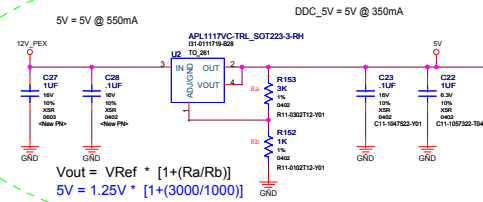


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DATE 25 OCT 2009

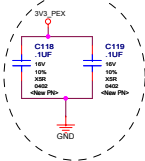
Power Supply I: 2V5, 3V3, 5V, IFP_IOVDD

Change DDC_5V circuit

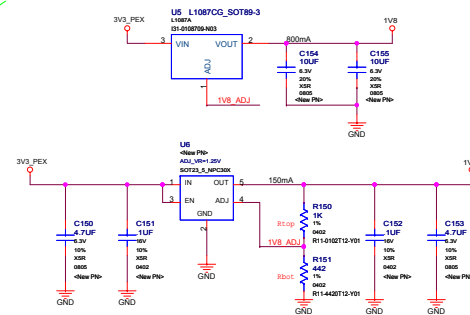


A3V3 = 3.3V @ 800mA

Add EMI CAP x 2pcs
3V3_PEX to GND

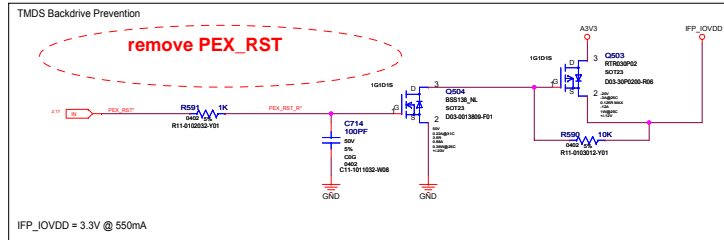


Change 1V8 circuit



$$V_{out} = V_{Ref} * [1 + (R_{bot}/R_{top})]$$

$$1.8V = 1.25V * [1 + (442/1000)]$$



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply I: 2V5, 3V3, 5V, IFF_JOVDD

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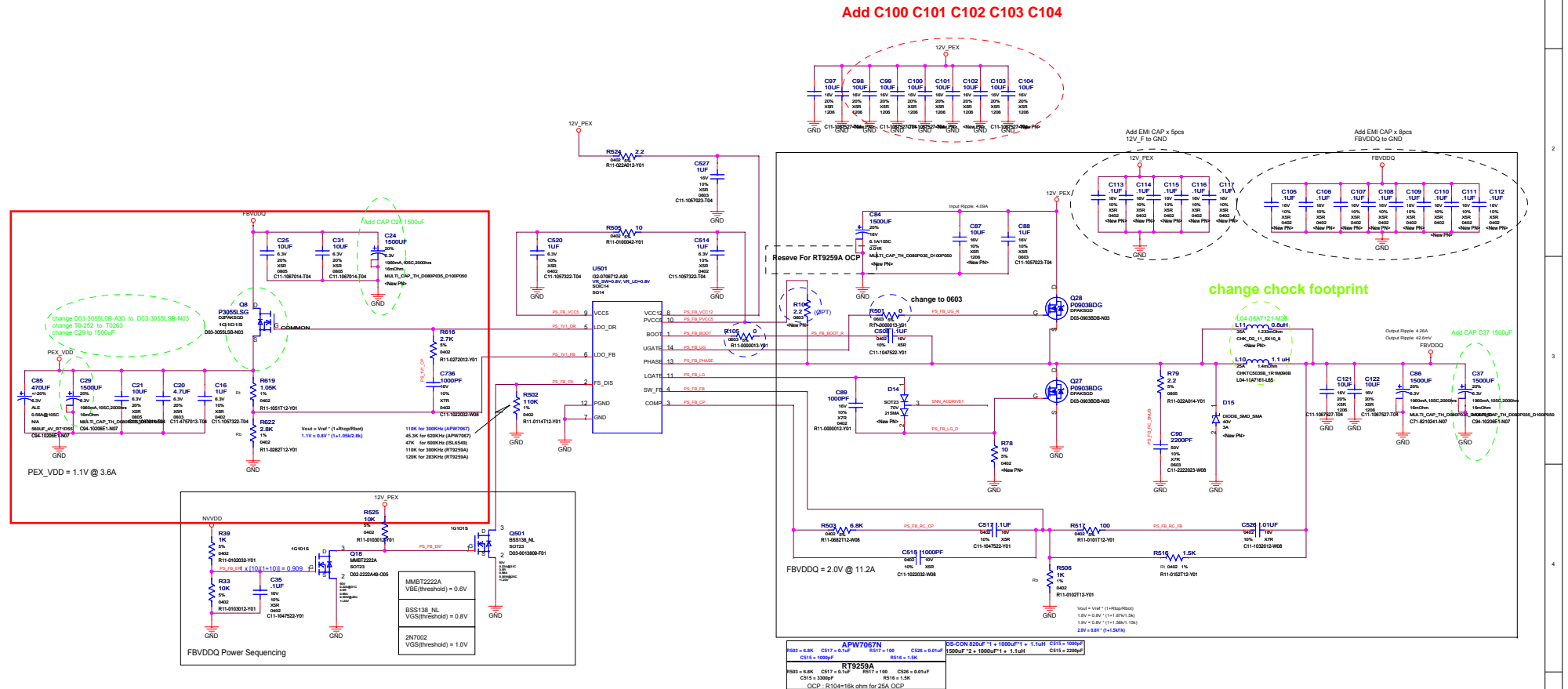
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Power Supply II: FBVDDQ



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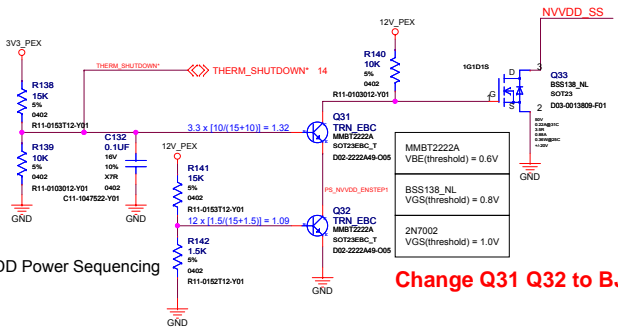
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ID	DATE	DESCRIPTION
1	25 OCT 2009	Initial Release

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ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL: Power Supply II: FBVDDQ

Power Supply III: NVVDD, PEX_VDD



NVVDD Power Sequencing

Change Q31 Q32 to BJT

RT9258
Switching Frequency 250KHz (R308=42K)
a. Inductance(L): L0=0.8+20%μH(100KHz/0.25V)
b. DC Resistance(RDC): 1.233mΩ +6%
c. Iout Max=35A
d. output CAP = 1500μF 25mohm
R303 = R305 = 7.2K
R306 = R318 = 0 ohm(OCP trigger point = 60A)
C302 = C310 = 0.1 uF
Compensation
C308 = NC F ; R314 = NC ohm
C306 = 33p F ; C307 = 22n F
R310 = 3k ohm ; R313 = 7k ohm

APW7088
Switching Frequency Fixed 300KHz
a. Inductance(L): L0=0.8+20%μH(100KHz/0.25V)
b. DC Resistance(RDC): 1.233mΩ +6%
c. Iout Max=35A
d. output CAP = 1500μF 25mohm
R303 = R305 = 4.3K
R306 = R318 = 620 ohm(OCP trigger point = 60A)
C302 = C310 = 0.22uF
Compensation
C308 = 3.3nF ; R314 = 220 ohm
C306 = 1000pF ; C307 = 10nF
R310 = 4.02K ohm ; R313 = 1.78K ohm

VID0,VID1,VID2 Float
Vref = 0.85V
R301,R317,R308,R302,R309,R315 = N/A

