

P672: GT215-128bit, 32Mx32 GDDR5

DL-DVI, VGA, HDMI

Page 1: TABLE OF CONTENTS

Page 2: PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS

Page 3: FBA MEMORY INTERFACE, GPU NVVDD & FBVDDQ DECOUPLING CAPS

Page 4: FBA 32Mx32 GDDR5 MEMORIES, FBA CLK TERMS

Page 5: FBA MEMORY FBVDDQ DECOUPLING CAPS

Page 6: FBC MEMORY INTERFACE

Page 7: FBC 32MX32 GDDR5 MEMORIES, FBC CLK TERMS

Page 8: FBC MEMORY FBVDDQ DECOUPLING CAPS

Page 9: DACA (PRIMARY DVI-I)

Page 10: DACB (SECONDARY VGA)

Page 11: TMDS LINK A/B: DVI-I (SOUTH)

Page 12: LINK C: HDMI (NORTH)

Page 13: LINK D (UNUSED)

Page 14: LINK E/F: (UNUSED)

Page 15: MIOA & MIOB (UNUSED)

Page 16: XTAL, MECHANICALS, THERMALS

Page 17: FAN CONTROL, THERMAL ALERT, GPIO, JTAG

Page 18: VBIOS ROM, INFOROM, STRAPPING OPTIONS

Page 19: 5V, DDC5V, IFP PLLVDD, IFP IOVDD, 3V3 FILTER, 12V FILTER

Page 20: FBVDDQ SINGLE PHASE SWITCHER, PEX_VDD LINEAR

Page 21: NVVDD DUAL PHASE SWITCHER

Page 22: BaseNet Report 1

Page 23: BaseNet Report 2

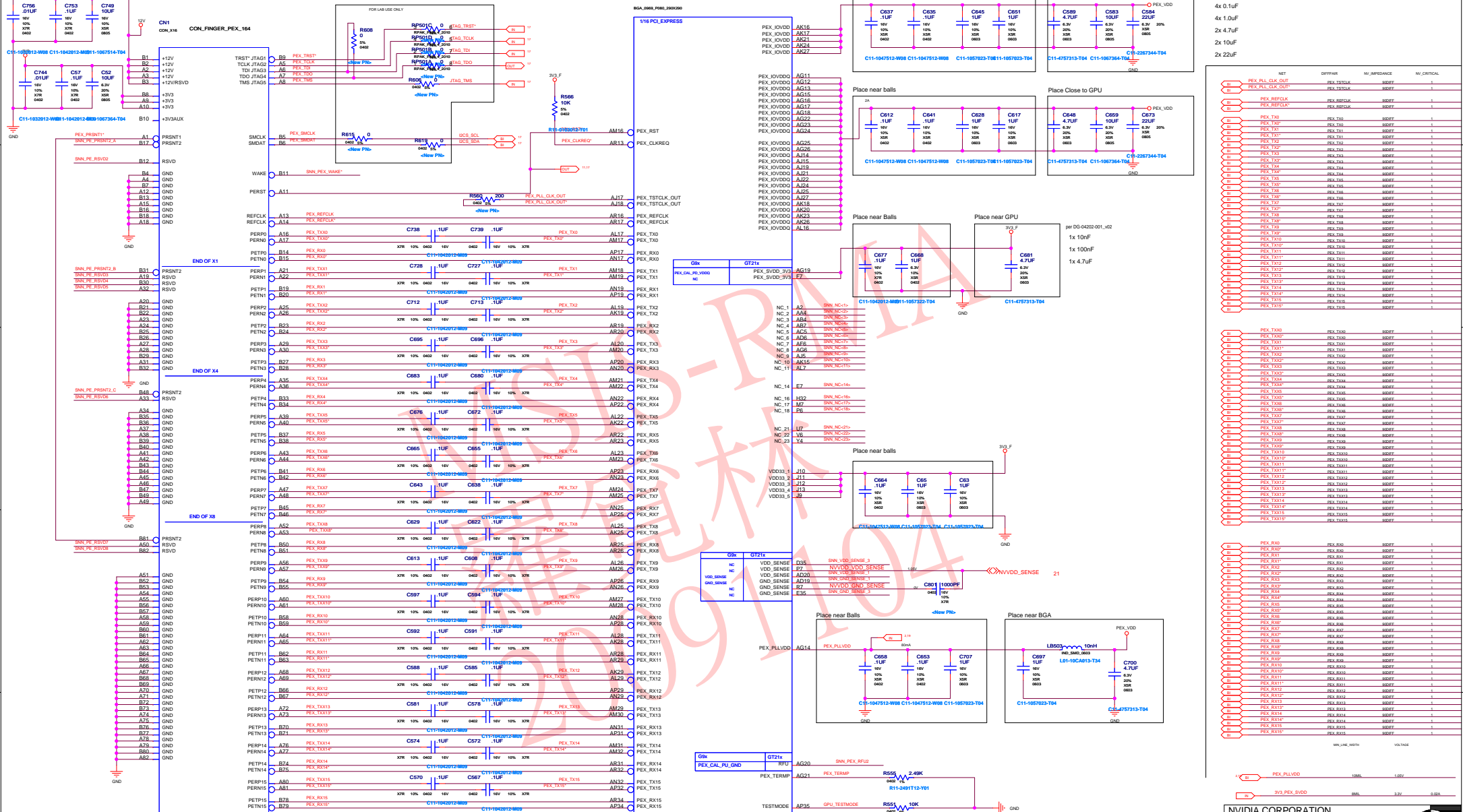
Page 24: CREFER Parts

MSIS-RMA

羅覓林


20091104

REV	VARIANT	NVPN	ASSEMBLY
0	BASE	600-10672-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SRU001	600-10672-0001-100	GT215-400, 550/1375MHz, 512MB, 32Mx16, 8GBx170, 1800MHz, GDDR5 DR-ANVGNOM
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

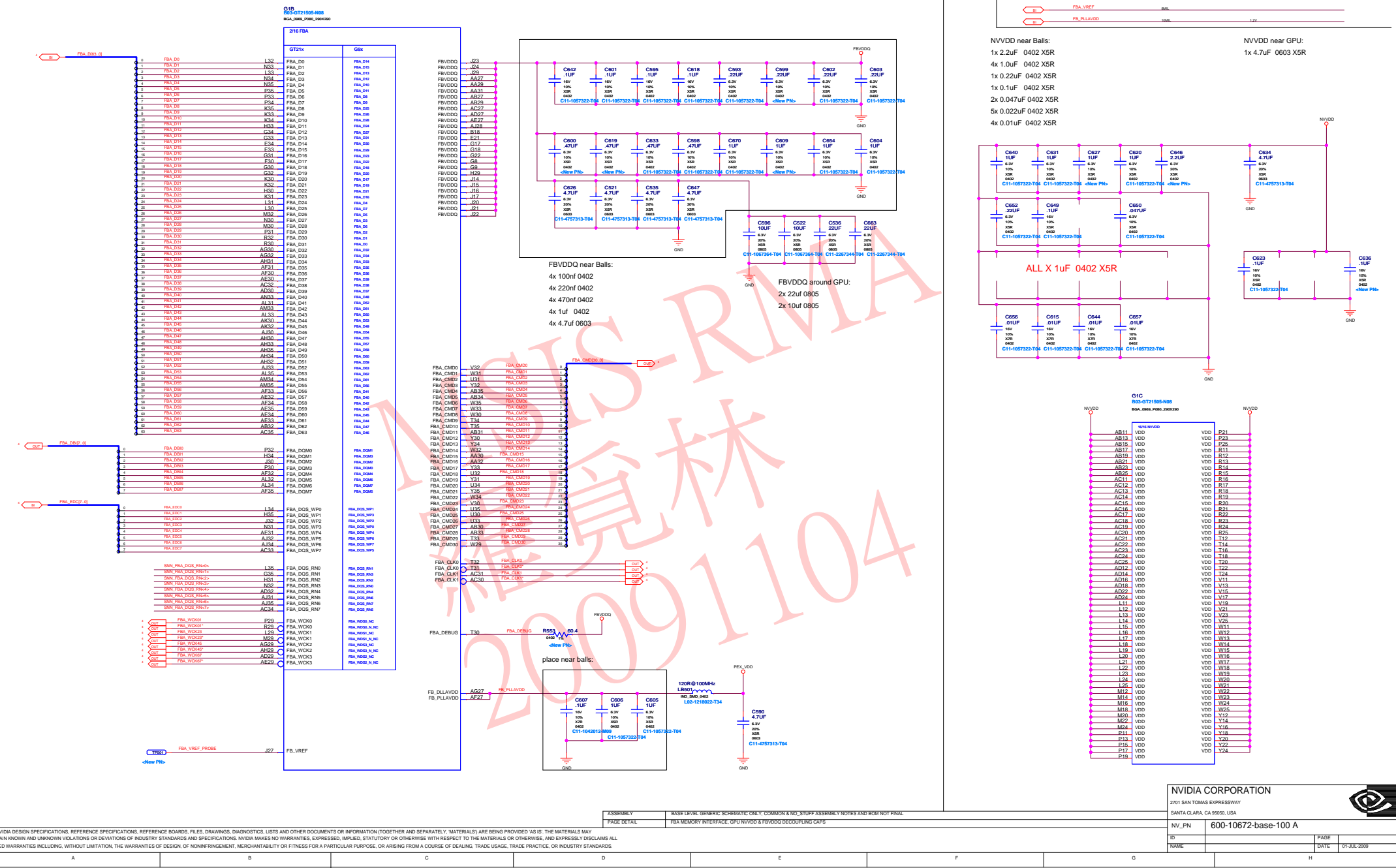


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE OR INDUSTRY STANDARDS.

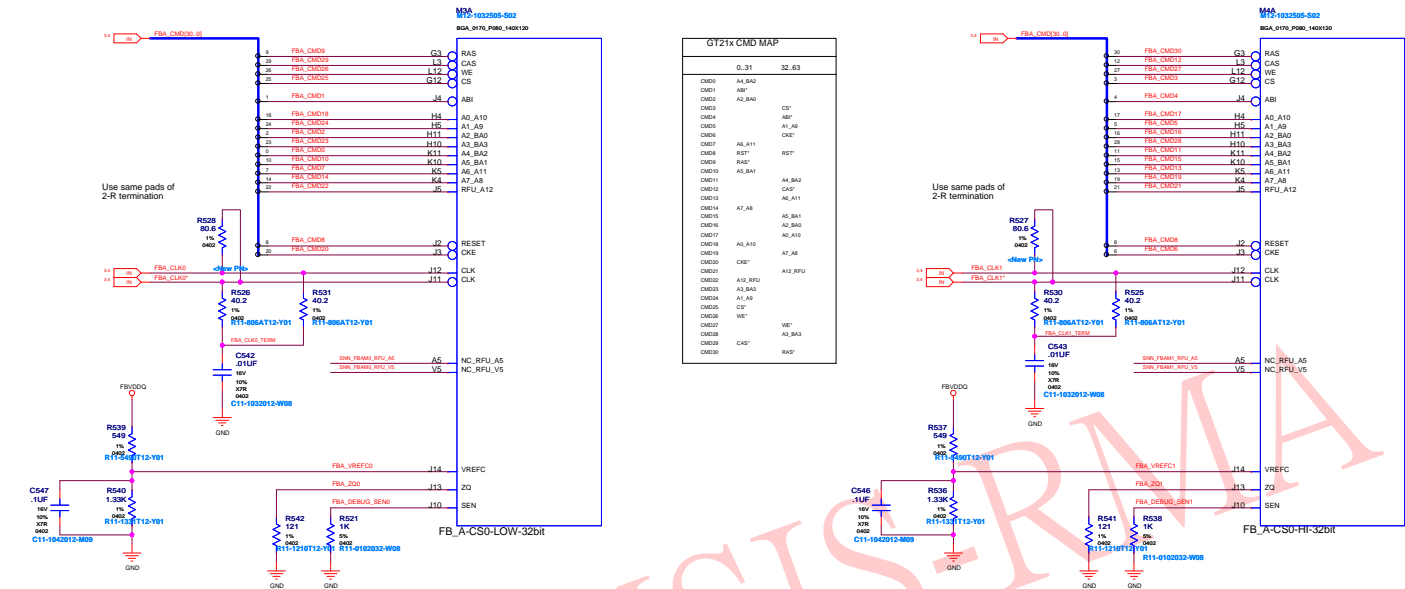
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN 600-10672-base-100 A			
ID		PAGE	
NAME		DATE	01-JUL-2009

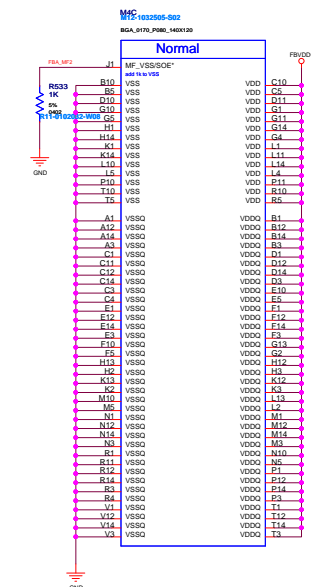
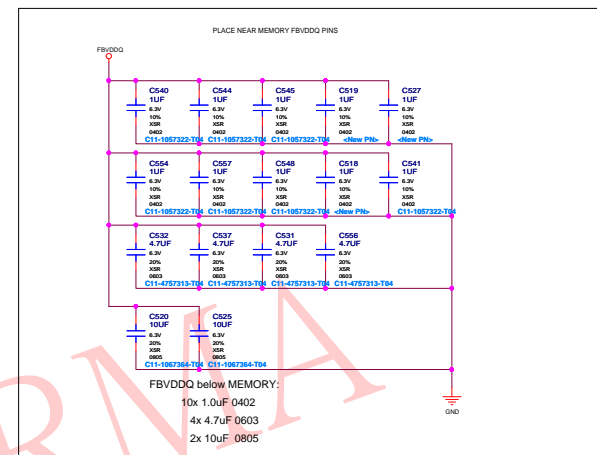
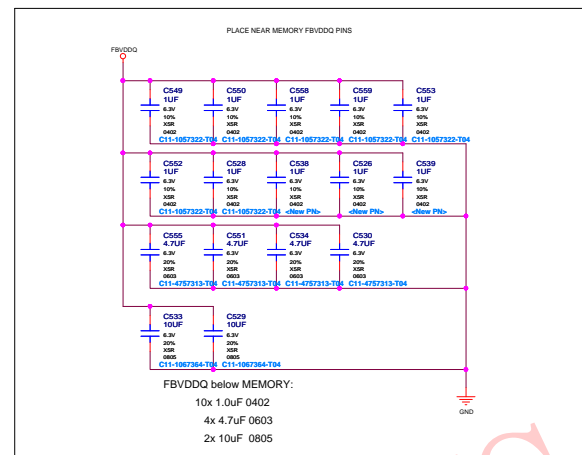
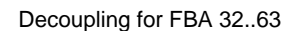
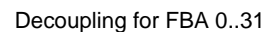
MEMORY Partition A - GPU, FBVDD/Q & NVVDD DECOUPLING



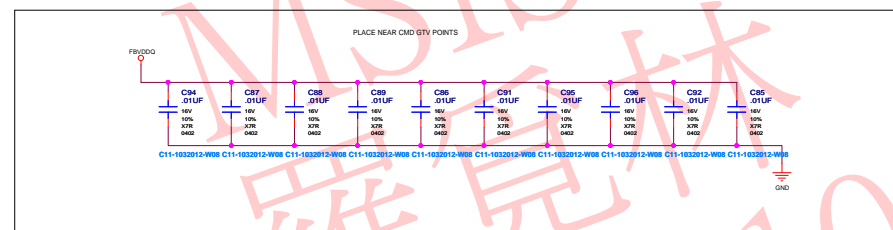
MEMORY Partition A



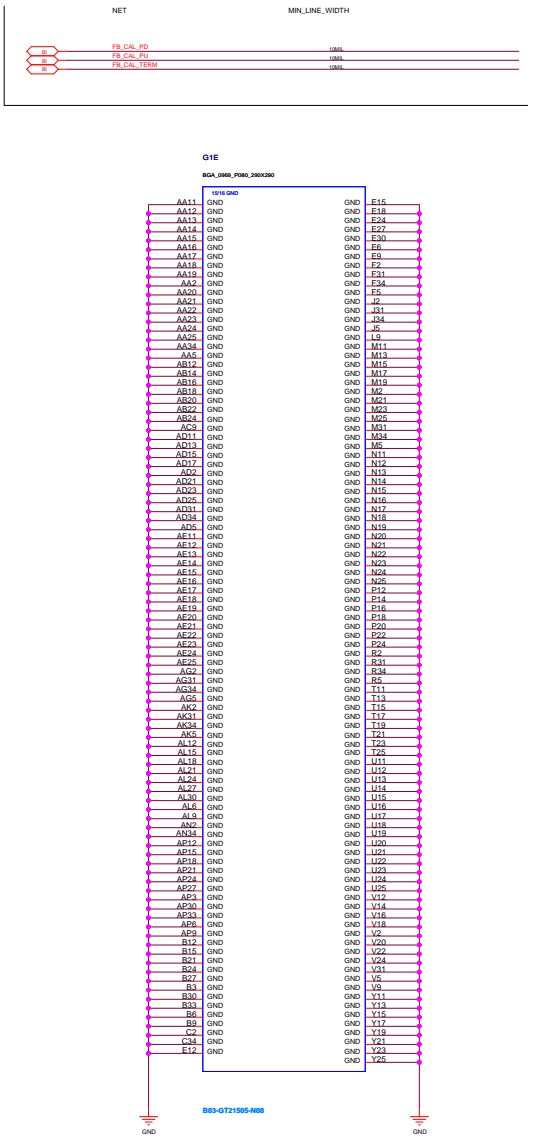
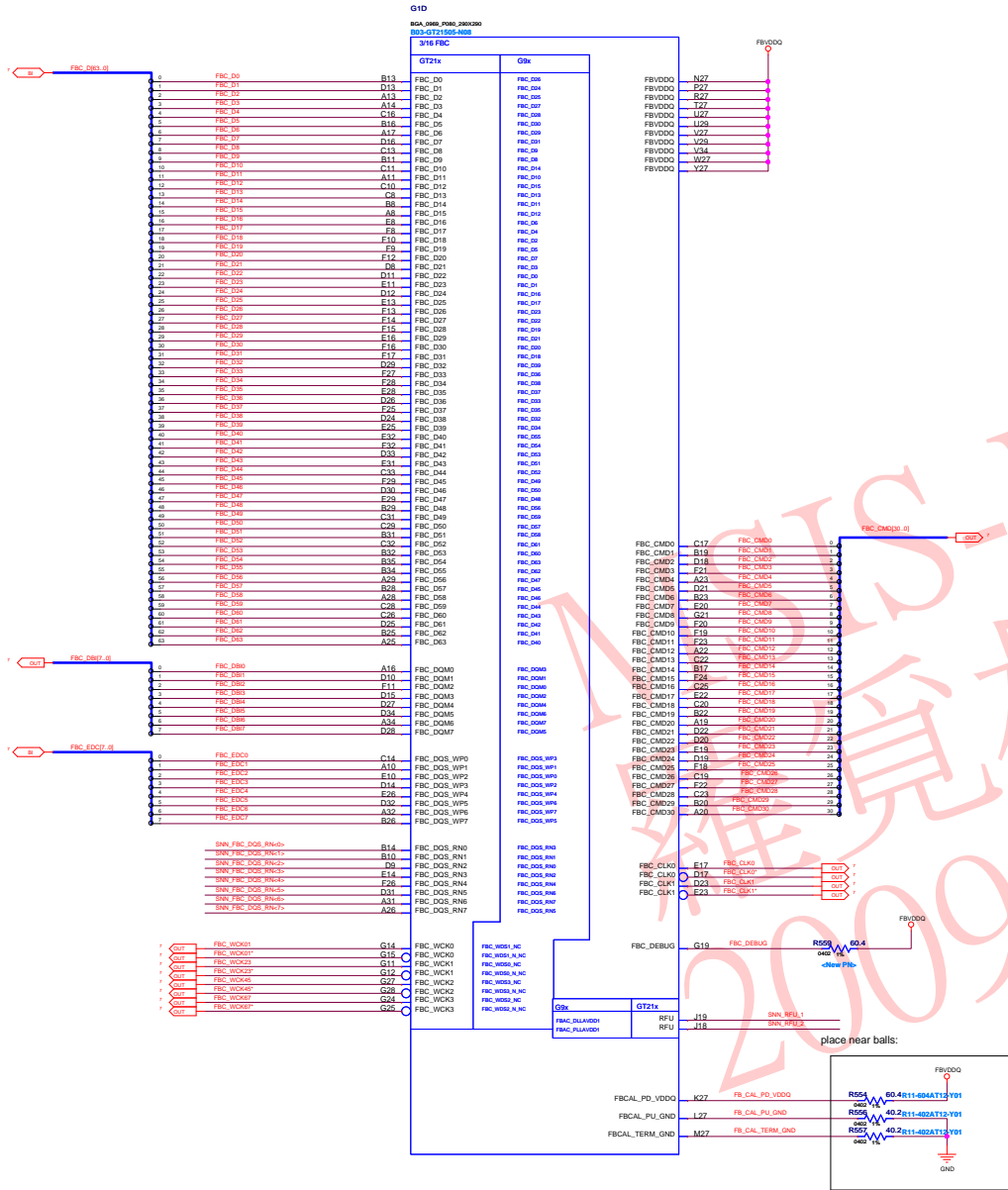
MEMORY Partition A - Decoupling



Return path coupling GND/FBVDDQ for FBA



MEMORY Partition C - GPU



NVIDIA CORPORATION

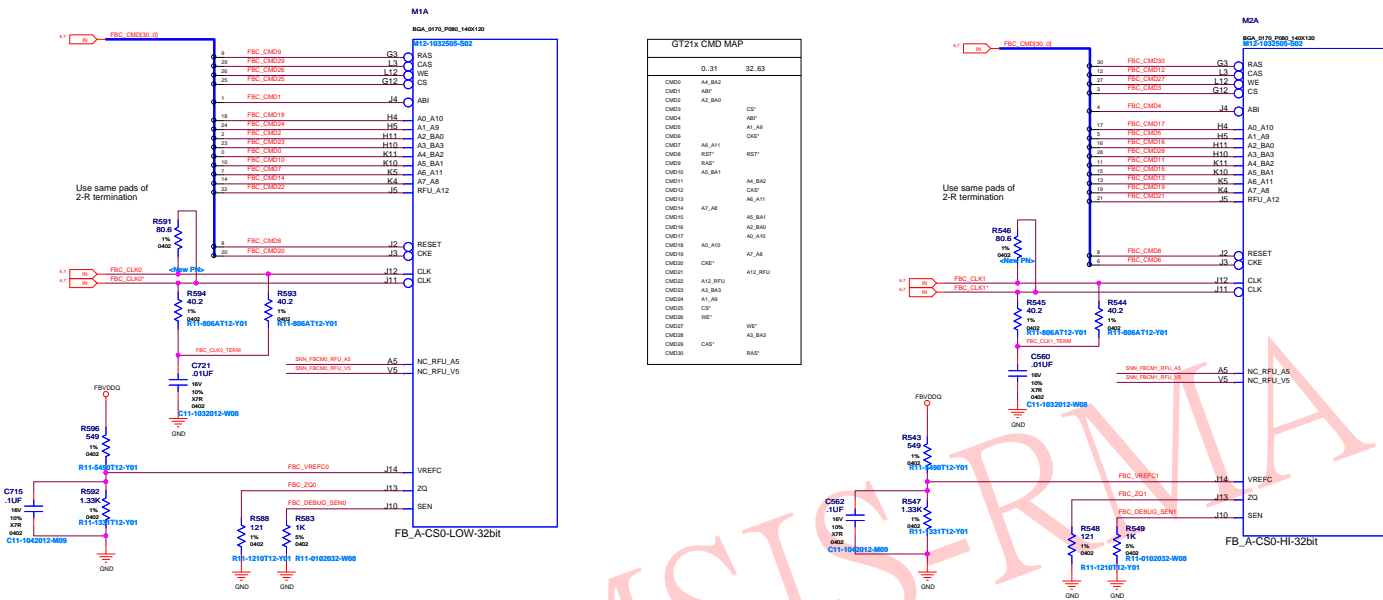
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10672-base-100 A
-------	----------------------

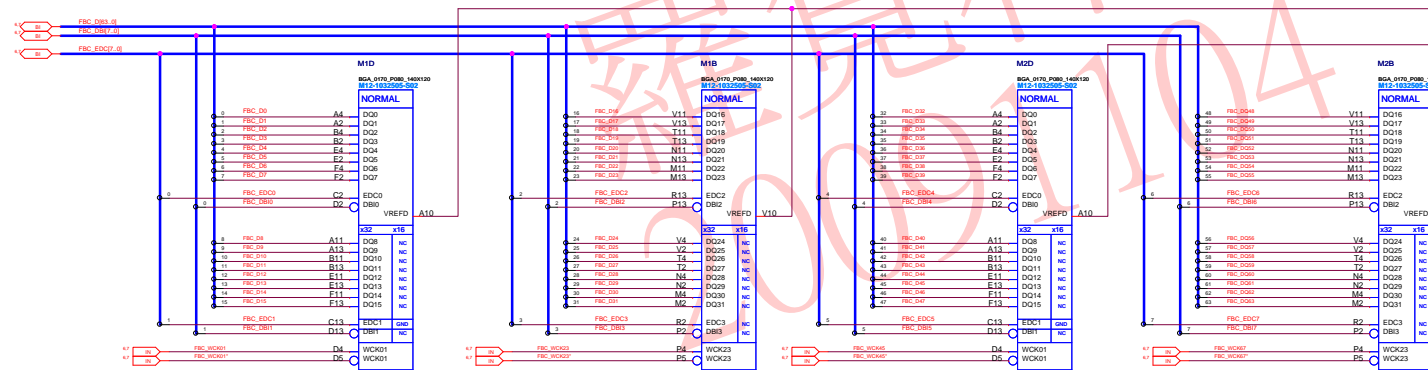
ID	PAGE
NAME	DATE 01-JUL-2009

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

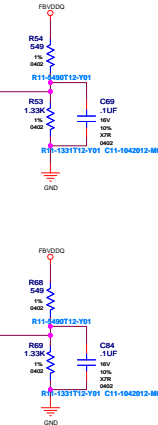
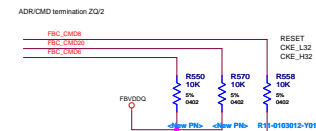
MEMORY Partition C



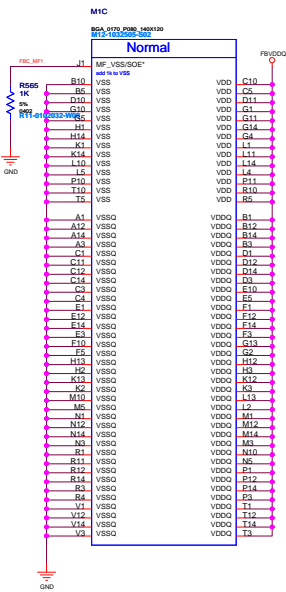
!!! Place all WCK termination inline instead at the memory near end (<50ps ~300MIL from DRAM pin)!!!



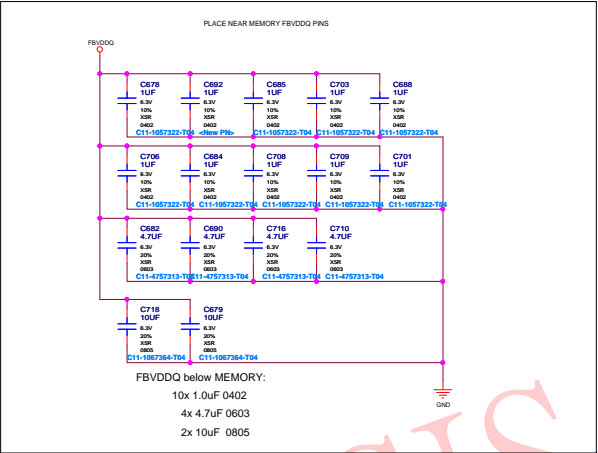
NET		DIFFPAIR		NV_IMPEDANCE		NV_CRITICAL_NET	
6	FRC_DBS_01			ADMM			
6	FRC_DBS_02			ADMM			
6	FRC_DBS_03			ADMM			
6	FRC_DBS_04			ADMM			
6	FRC_DBS_05			ADMM			
6	FRC_DBS_06			ADMM			
6	FRC_DBS_07			ADMM			
6	FRC_DBS_08			ADMM			
6	FRC_DBS_09			ADMM			
6	FRC_DBS_10			ADMM			
6	FRC_DBS_11			ADMM			
6	FRC_DBS_12			ADMM			
6	FRC_DBS_13			ADMM			
6	FRC_DBS_14			ADMM			
6	FRC_DBS_15			ADMM			
6	FRC_DBS_16			ADMM			
6	FRC_DBS_17			ADMM			
6	FRC_DBS_18			ADMM			
6	FRC_DBS_19			ADMM			
6	FRC_DBS_20			ADMM			
6	FRC_DBS_21			ADMM			
6	FRC_DBS_22			ADMM			
6	FRC_DBS_23			ADMM			
6	FRC_DBS_24			ADMM			
6	FRC_DBS_25			ADMM			
6	FRC_DBS_26			ADMM			
6	FRC_DBS_27			ADMM			
6	FRC_DBS_28			ADMM			
6	FRC_DBS_29			ADMM			
6	FRC_DBS_30			ADMM			
6	FRC_DBS_31			ADMM			
6	FRC_DBS_32			ADMM			
6	FRC_DBS_33			ADMM			
6	FRC_DBS_34			ADMM			
6	FRC_DBS_35			ADMM			
6	FRC_DBS_36			ADMM			
6	FRC_DBS_37			ADMM			
6	FRC_DBS_38			ADMM			
6	FRC_DBS_39			ADMM			
6	FRC_DBS_40			ADMM			
6	FRC_DBS_41			ADMM			
6	FRC_DBS_42			ADMM			
6	FRC_DBS_43			ADMM			
6	FRC_DBS_44			ADMM			
6	FRC_DBS_45			ADMM			
6	FRC_DBS_46			ADMM			
6	FRC_DBS_47			ADMM			
6	FRC_DBS_48			ADMM			
6	FRC_DBS_49			ADMM			
6	FRC_DBS_50			ADMM			
6	FRC_DBS_51			ADMM			
6	FRC_DBS_52			ADMM			
6	FRC_DBS_53			ADMM			
6	FRC_DBS_54			ADMM			
6	FRC_DBS_55			ADMM			
6	FRC_DBS_56			ADMM			
6	FRC_DBS_57			ADMM			
6	FRC_DBS_58			ADMM			
6	FRC_DBS_59			ADMM			
6	FRC_DBS_60			ADMM			
6	FRC_DBS_61			ADMM			
6	FRC_DBS_62			ADMM			
6	FRC_DBS_63			ADMM			
6	FRC_DBS_64			ADMM			
6	FRC_DBS_65			ADMM			
6	FRC_DBS_66			ADMM			
6	FRC_DBS_67			ADMM			
6	FRC_DBS_68			ADMM			
6	FRC_DBS_69			ADMM			
6	FRC_DBS_70			ADMM			
6	FRC_DBS_71			ADMM			
6	FRC_DBS_72			ADMM			
6	FRC_DBS_73			ADMM			
6	FRC_DBS_74			ADMM			
6	FRC_DBS_75			ADMM			
6	FRC_DBS_76			ADMM			
6	FRC_DBS_77			ADMM			
6	FRC_DBS_78			ADMM			
6	FRC_DBS_79			ADMM			
6	FRC_DBS_80			ADMM			
6	FRC_DBS_81			ADMM			
6	FRC_DBS_82			ADMM			
6	FRC_DBS_83			ADMM			
6	FRC_DBS_84			ADMM			
6	FRC_DBS_85			ADMM			
6	FRC_DBS_86			ADMM			
6	FRC_DBS_87			ADMM			
6	FRC_DBS_88			ADMM			
6	FRC_DBS_89			ADMM			
6	FRC_DBS_90			ADMM			
6	FRC_DBS_91			ADMM			
6	FRC_DBS_92			ADMM			
6	FRC_DBS_93			ADMM			
6	FRC_DBS_94			ADMM			
6	FRC_DBS_95			ADMM			
6	FRC_DBS_96			ADMM			
6	FRC_DBS_97			ADMM			
6	FRC_DBS_98			ADMM			
6	FRC_DBS_99			ADMM			
6	FRC_DBS_100			ADMM			
6	FRC_DBS_101			ADMM			
6	FRC_DBS_102			ADMM			
6	FRC_DBS_103			ADMM			
6	FRC_DBS_104			ADMM			
6	FRC_DBS_105			ADMM			
6	FRC_DBS_106			ADMM			
6	FRC_DBS_107			ADMM			
6	FRC_DBS_108			ADMM			
6	FRC_DBS_109			ADMM			
6	FRC_DBS_110			ADMM			
6	FRC_DBS_111			ADMM			
6	FRC_DBS_112			ADMM			
6	FRC_DBS_113			ADMM			
6	FRC_DBS_114			ADMM			
6	FRC_DBS_115			ADMM			
6	FRC_DBS_116			ADMM			
6	FRC_DBS_117			ADMM			
6	FRC_DBS_118			ADMM			
6	FRC_DBS_119			ADMM			
6	FRC_DBS_120			ADMM			
6	FRC_DBS_121			ADMM			
6	FRC_DBS_122			ADMM			
6	FRC_DBS_123			ADMM			
6	FRC_DBS_124			ADMM			
6	FRC_DBS_125			ADMM			
6	FRC_DBS_126			ADMM			
6	FRC_DBS_127			ADMM			
6	FRC_DBS_128			ADMM			
6	FRC_DBS_129			ADMM			
6	FRC_DBS_130			ADMM			
6	FRC_DBS_131			ADMM			
6	FRC_DBS_132			ADMM			
6	FRC_DBS_133			ADMM			
6	FRC_DBS_134			ADMM			
6	FRC_DBS_135			ADMM			
6	FRC_DBS_136			ADMM			
6	FRC_DBS_137			ADMM			
6	FRC_DBS_138			ADMM			
6	FRC_DBS_139			ADMM			
6	FRC_DBS_140			ADMM			
6	FRC_DBS_141			ADMM			
6	FRC_DBS_142			ADMM			
6	FRC_DBS_143			ADMM			
6	FRC_DBS_144			ADMM			
6	FRC_DBS_145			ADMM			
6	FRC_DBS_146			ADMM			
6	FRC_DBS_147			ADMM			
6	FRC_DBS_148			ADMM			
6	FRC_DBS_149			ADMM			
6	FRC_DBS_150			ADMM			
6	FRC_DBS_151			ADMM			
6	FRC_DBS_152			ADMM			
6	FRC_DBS_153			ADMM			
6	FRC_DBS_154			ADMM			
6	FRC_DBS_155			ADMM			
6	FRC_DBS_156			ADMM			
6	FRC_DBS_157			ADMM			
6	FRC_DBS_158			ADMM			
6	FRC_DBS_159			ADMM			
6	FRC_DBS_160			ADMM			
6	FRC_DBS_161			ADMM			
6	FRC_DBS_162			ADMM			
6	FRC_DBS_163			ADMM			
6	FRC_DBS_164			ADMM			
6	FRC_DBS_165			ADMM			
6	FRC_DBS_166			ADMM			
6	FRC_DBS_167			ADMM			
6	FRC_DBS_168			ADMM			
6	FRC_DBS_169			ADMM			
6	FRC_DBS_170			ADMM			
6	FRC_DBS_171			ADMM			
6	FRC_DBS_172			ADMM			
6	FRC_DBS_173			ADMM			
6	FRC_DBS_174			ADMM			
6	FRC_DBS_175			ADMM			
6	FRC_DBS_176			ADMM			
6	FRC_DBS_177			ADMM			
6	FRC_DBS_178			ADMM			
6	FRC_DBS_179			ADMM			
6	FRC_DBS_180			ADMM			
6	FRC_DBS_181			ADMM			
6	FRC_DBS_182			ADMM			
6	FRC_DBS_183			ADMM			
6	FRC_DBS_184			ADMM			
6	FRC_DBS_185			ADMM			
6	FRC_DBS_186			ADMM			
6	FRC_DBS_187			ADMM			
6	FRC_DBS_188			ADMM			
6	FRC_DBS_189			ADMM			
6	FRC_DBS_190			ADMM			
6	FRC_DBS_191			ADMM			
6	FRC_DBS_192			ADMM			
6	FRC_DBS_193			ADMM			
6	FRC_DBS_194			ADMM			
6	FRC_DBS_195			ADMM			
6	FRC_DBS_196			ADMM			
6	FRC_DBS_197			ADMM			
6	FRC_DBS_198			ADMM			
6	FRC_DBS_199			ADMM			
6	FRC_DBS_200			ADMM			
6	FRC_DBS_201			ADMM			
6	FRC_DBS_202			ADMM			
6	FRC_DBS_203			ADMM			
6	FRC_DBS_204			ADMM			
6	FRC_DBS_205			ADMM			
6	FRC_DBS_206			ADMM			
6	FRC_DBS_207			ADMM			
6	FRC_DBS_208			ADMM			
6	FRC_DBS_209			ADMM			
6	FRC_DBS_210			ADMM			
6	FRC_DBS_211			ADMM			
6	FRC_DBS_212			ADMM			
6	FRC_DBS_213			ADMM			
6	FRC_DBS_214			ADMM			
6	FRC_DBS_215			ADMM			
6	FRC_DBS_216			ADMM			
6	FRC_DBS_217			ADMM			
6	FRC_DBS_218			ADMM			
6	FRC_DBS_219			ADMM			
6	FRC_DBS_220			ADMM			
6	FRC_DBS_221			ADMM			
6	FRC_DBS_222			ADMM			
6	FRC_DBS_223			ADMM			
6	FRC_DBS_224			ADMM			
6	FRC_DBS_225			ADMM			
6	FRC_DBS_226			ADMM			
6	FRC_DBS_227			ADMM			
6	FRC_DBS_228			ADMM			
6	FRC_DBS_229			ADMM			
6	FRC_DBS_230			ADMM			
6	FRC_DBS_231			ADMM			
6	FRC_DBS_232			ADMM			
6	FRC_DBS_233			ADMM			
6	FRC_DBS_234			ADMM			
6	FRC_DBS_235			ADMM			
6	FRC_DBS_236			ADMM			
6	FRC_DBS_237			ADMM			
6	FRC_DBS_238			ADMM			
6	FRC_DBS_239			ADMM			
6	FRC_DBS_240			ADMM			
6	FRC_DBS_241			ADMM			
6	FRC_DBS_242			ADMM			
6	FRC_DBS_243			ADMM			
6	FRC_DBS_244			ADMM			
6	FRC_DBS_245			ADMM			
6	FRC_DBS_246			ADMM			
6	FRC_DBS_247			ADMM			
6	FRC_DBS_248			ADMM			
6	FRC_DBS_249			ADMM			
6	FRC_DBS_250			ADMM			
6	FRC_DBS_251			ADMM			
6	FRC_DBS_252			ADMM			
6	FRC_DBS_253			ADMM			
6	FRC_DBS_254			ADMM			



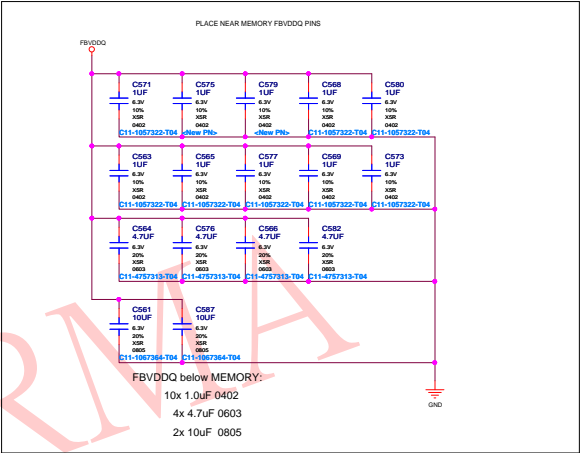
MEMORY PARTITION C DECOUPLING



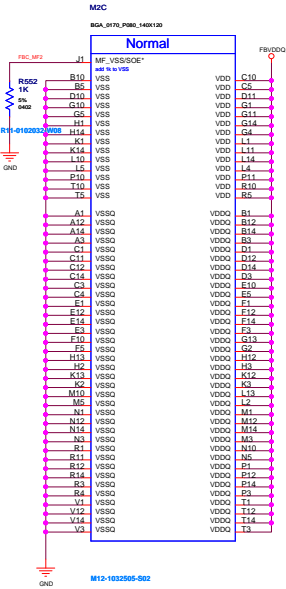
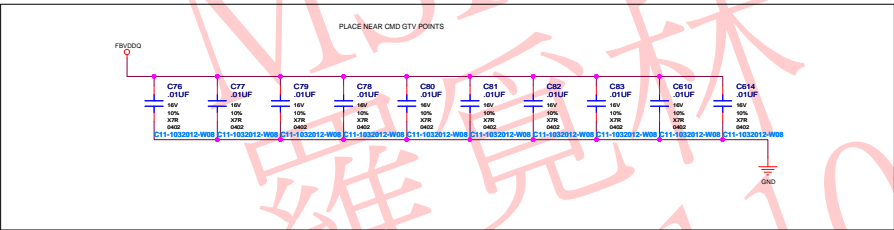
Decoupling for FBC 0..31



Decoupling for FBC 32..63



Return path coupling GND/FBVDDQ for FBC



NVIDIA CORPORATION

7701 SANTOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

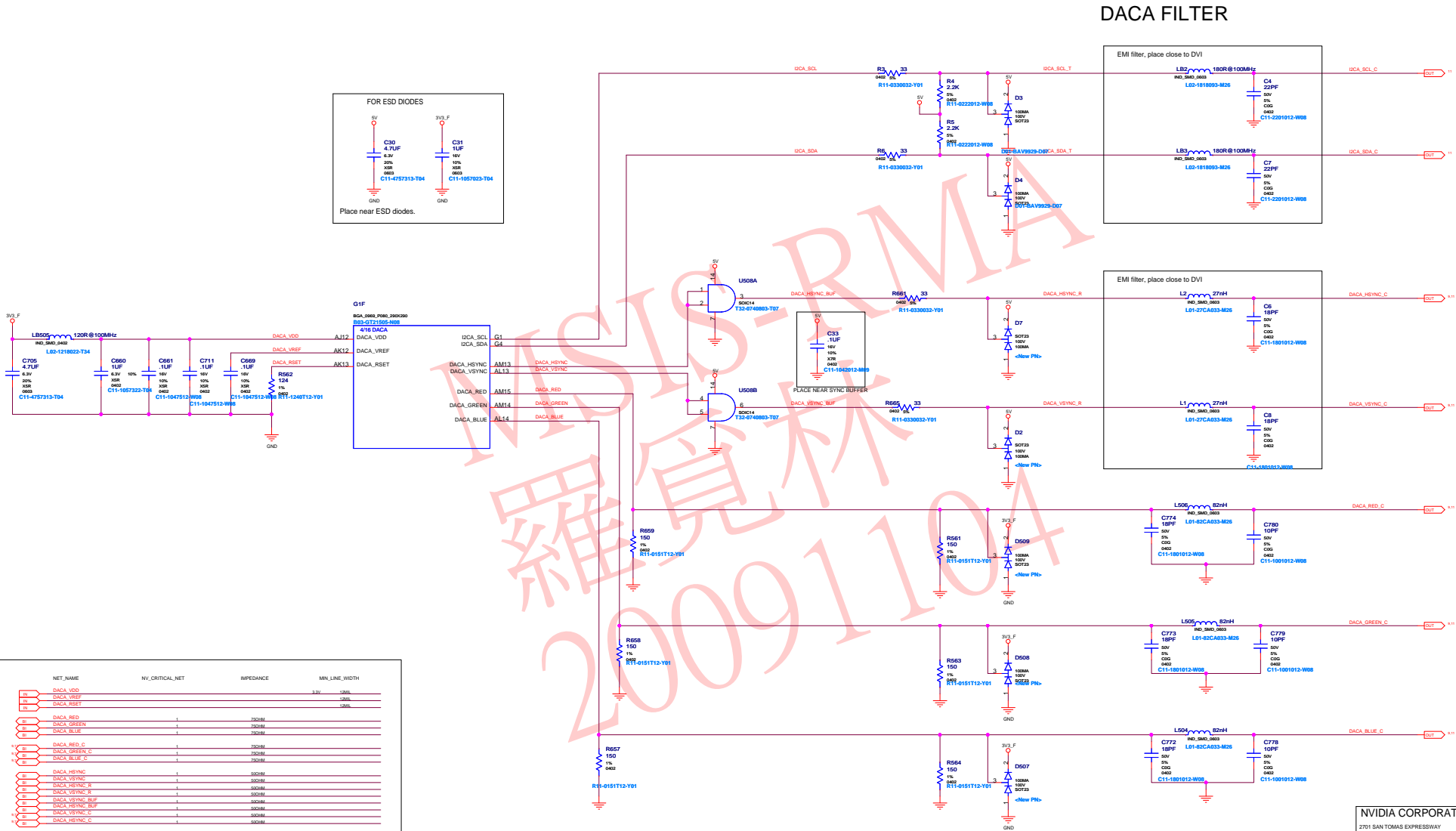


NV_PN	600-10672-base-100 A
ID	
NAME	
PAGE	
DATE	01-JUL-2009

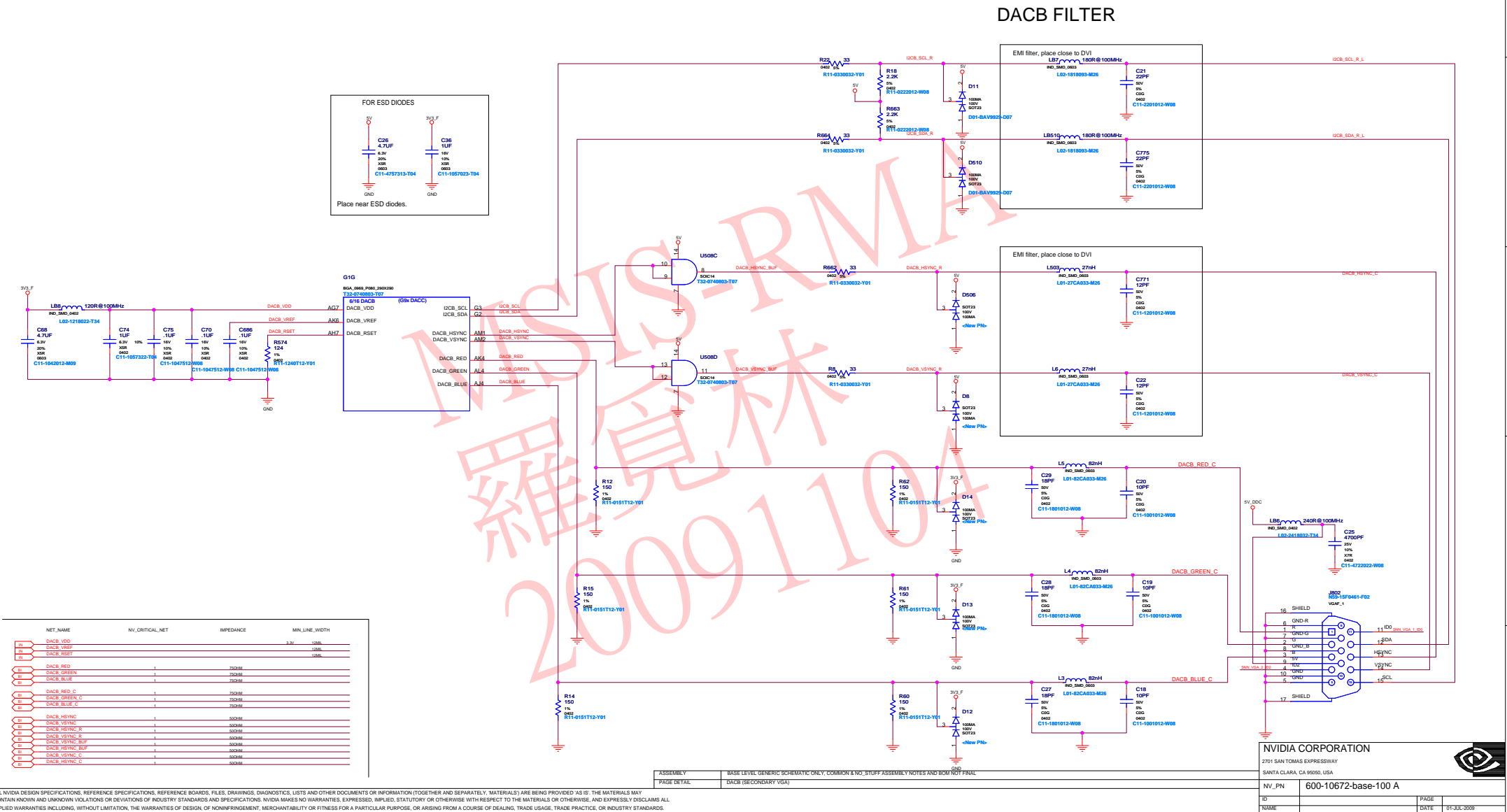
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE, WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. 310FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE/MATERIAL	FBC MEMORY FBVDDQ DECOUPLING CAPS

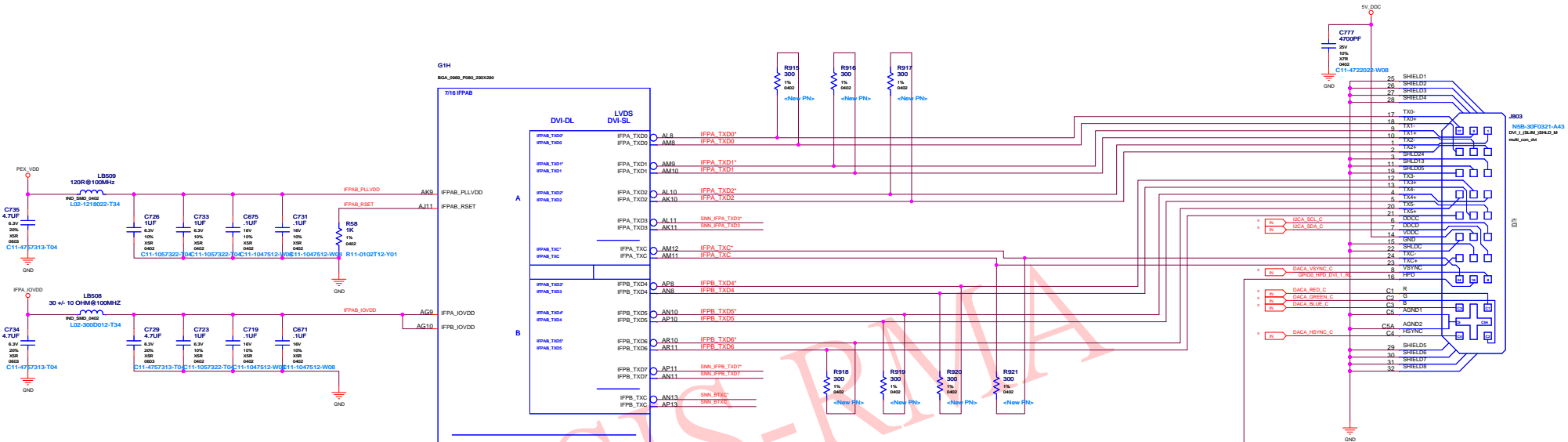
Primary Display (DACA), DVI-I (South)



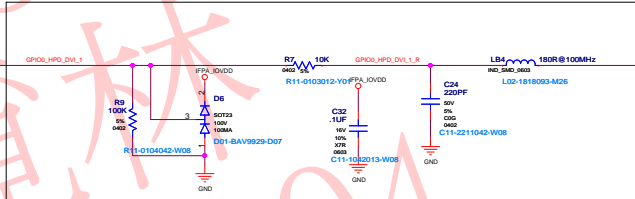
Secondary Display (DACB), VGA (Mid)



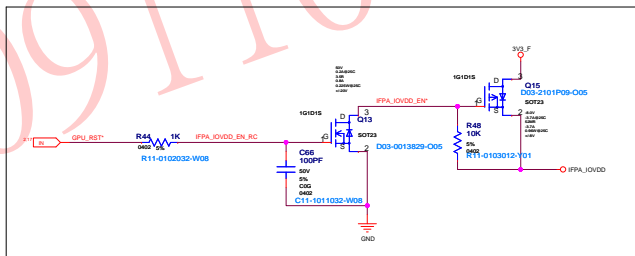
LINK A/B: TMDS, Primary DVI-I DL (South)



HOTPLUG DETECTION



IFP IOVDD BACKDRIVE PREVENTION



	NETNAME	DEF PART NAME	NO. CRITICAL	NO. DEFERENCE
10	IFPA_T0C1	F73B_T0C1	1	1000%
10	IFPA_T0C2	F73B_T0C2	1	1000%
10	IFPA_T0D0	F73B_T0D0	1	1000%
10	IFPA_T0D1	F73B_T0D1	1	1000%
10	IFPA_T0D2	F73B_T0D2	1	1000%
10	IFPA_T0D3	F73B_T0D3	1	1000%
10	IFPA_T0D4	F73B_T0D4	1	1000%
10	IFPA_T0D5	F73B_T0D5	1	1000%
10	IFPA_T0D6	F73B_T0D6	1	1000%
10	IFPA_T0D7	F73B_T0D7	1	1000%
10	IFPA_T0D8	F73B_T0D8	1	1000%
10	IFPA_T0D9	F73B_T0D9	1	1000%
10	IFPA_T1D0	F73B_T1D0	1	1000%
10	IFPA_T1D1	F73B_T1D1	1	1000%
10	IFPA_T1D2	F73B_T1D2	1	1000%
10	IFPA_T1D3	F73B_T1D3	1	1000%
10	IFPA_T1D4	F73B_T1D4	1	1000%
10	IFPA_T1D5	F73B_T1D5	1	1000%
10	IFPA_T1D6	F73B_T1D6	1	1000%
10	IFPA_T1D7	F73B_T1D7	1	1000%
10	IFPA_T1D8	F73B_T1D8	1	1000%
10	IFPA_T1D9	F73B_T1D9	1	1000%
10	IFPA_T2D0	F73B_T2D0	1	1000%
10	IFPA_T2D1	F73B_T2D1	1	1000%
10	IFPA_T2D2	F73B_T2D2	1	1000%
10	IFPA_T2D3	F73B_T2D3	1	1000%
10	IFPA_T2D4	F73B_T2D4	1	1000%
10	IFPA_T2D5	F73B_T2D5	1	1000%
10	IFPA_T2D6	F73B_T2D6	1	1000%
10	IFPA_T2D7	F73B_T2D7	1	1000%
10	IFPA_T2D8	F73B_T2D8	1	1000%
10	IFPA_T2D9	F73B_T2D9	1	1000%
10	IFPA_T3D0	F73B_T3D0	1	1000%
10	IFPA_T3D1	F73B_T3D1	1	1000%
10	IFPA_T3D2	F73B_T3D2	1	1000%
10	IFPA_T3D3	F73B_T3D3	1	1000%
10	IFPA_T3D4	F73B_T3D4	1	1000%
10	IFPA_T3D5	F73B_T3D5	1	1000%
10	IFPA_T3D6	F73B_T3D6	1	1000%
10	IFPA_T3D7	F73B_T3D7	1	1000%
10	IFPA_T3D8	F73B_T3D8	1	1000%
10	IFPA_T3D9	F73B_T3D9	1	1000%
10	IFPA_T3E0	F73B_T3E0	1	1000%
10	IFPA_T3E1	F73B_T3E1	1	1000%
10	IFPA_T3E2	F73B_T3E2	1	1000%
10	IFPA_T3E3	F73B_T3E3	1	1000%
10	IFPA_T3E4	F73B_T3E4	1	1000%
10	IFPA_T3E5	F73B_T3E5	1	1000%
10	IFPA_T3E6	F73B_T3E6	1	1000%
10	IFPA_T3E7	F73B_T3E7	1	1000%
10	IFPA_T3E8	F73B_T3E8	1	1000%
10	IFPA_T3E9	F73B_T3E9	1	1000%
10	IFPA_T4D0	F73B_T4D0	1	1000%
10	IFPA_T4D1	F73B_T4D1	1	1000%
10	IFPA_T4D2	F73B_T4D2	1	1000%
10	IFPA_T4D3	F73B_T4D3	1	1000%
10	IFPA_T4D4	F73B_T4D4	1	1000%
10	IFPA_T4D5	F73B_T4D5	1	1000%
10	IFPA_T4D6	F73B_T4D6	1	1000%
10	IFPA_T4D7	F73B_T4D7	1	1000%
10	IFPA_T4D8	F73B_T4D8	1	1000%
10	IFPA_T4D9	F73B_T4D9	1	1000%
10	IFPA_T4E0	F73B_T4E0	1	1000%
10	IFPA_T4E1	F73B_T4E1	1	1000%
10	IFPA_T4E2	F73B_T4E2	1	1000%
10	IFPA_T4E3	F73B_T4E3	1	1000%
10	IFPA_T4E4	F73B_T4E4	1	1000%
10	IFPA_T4E5	F73B_T4E5	1	1000%
10	IFPA_T4E6	F73B_T4E6	1	1000%
10	IFPA_T4E7	F73B_T4E7	1	1000%
10	IFPA_T4E8	F73B_T4E8	1	1000%
10	IFPA_T4E9	F73B_T4E9	1	1000%
10	IFPA_T5D0	F73B_T5D0	1	1000%
10	IFPA_T5D1	F73B_T5D1	1	1000%
10	IFPA_T5D2	F73B_T5D2	1	1000%
10	IFPA_T5D3	F73B_T5D3	1	1000%
10	IFPA_T5D4	F73B_T5D4	1	1000%
10	IFPA_T5D5	F73B_T5D5	1	1000%
10	IFPA_T5D6	F73B_T5D6	1	1000%
10	IFPA_T5D7	F73B_T5D7	1	1000%
10	IFPA_T5D8	F73B_T5D8	1	1000%
10	IFPA_T5D9	F73B_T5D9	1	1000%
10	IFPA_T5E0	F73B_T5E0	1	1000%
10	IFPA_T5E1	F73B_T5E1	1	1000%
10	IFPA_T5E2	F73B_T5E2	1	1000%
10	IFPA_T5E3	F73B_T5E3	1	1000%
10	IFPA_T5E4	F73B_T5E4	1	1000%
10	IFPA_T5E5	F73B_T5E5	1	1000%
10	IFPA_T5E6	F73B_T5E6	1	1000%
10	IFPA_T5E7	F73B_T5E7	1	1000%
10	IFPA_T5E8	F73B_T5E8	1	1000%
10	IFPA_T5E9	F73B_T5E9	1	1000%
10	IFPA_T6D0	F73B_T6D0	1	1000%
10	IFPA_T6D1	F73B_T6D1	1	1000%
10	IFPA_T6D2	F73B_T6D2	1	1000%
10	IFPA_T6D3	F73B_T6D3	1	1000%
10	IFPA_T6D4	F73B_T6D4	1	1000%
10	IFPA_T6D5	F73B_T6D5	1	1000%
10	IFPA_T6D6	F73B_T6D6	1	1000%
10	IFPA_T6D7	F73B_T6D7	1	1000%
10	IFPA_T6D8	F73B_T6D8	1	1000%
10	IFPA_T6D9	F73B_T6D9	1	1000%
10	IFPA_T6E0	F73B_T6E0	1	1000%
10	IFPA_T6E1	F73B_T6E1	1	1000%
10	IFPA_T6E2	F73B_T6E2	1	1000%
10	IFPA_T6E3	F73B_T6E3	1	1000%
10	IFPA_T6E4	F73B_T6E4	1	1000%
10	IFPA_T6E5	F73B_T6E5	1	1000%
10	IFPA_T6E6	F73B_T6E6	1	1000%
10	IFPA_T6E7	F73B_T6E7	1	1000%
10	IFPA_T6E8	F73B_T6E8	1	1000%
10	IFPA_T6E9	F73B_T6E9	1	1000%
10	IFPA_T7D0	F73B_T7D0	1	1000%
10	IFPA_T7D1	F73B_T7D1	1	1000%
10	IFPA_T7D2	F73B_T7D2	1	1000%
10	IFPA_T7D3	F73B_T7D3	1	1000%
10	IFPA_T7D4	F73B_T7D4	1	1000%
10	IFPA_T7D5	F73B_T7D5	1	1000%
10	IFPA_T7D6	F73B_T7D6	1	1000%
10	IFPA_T7D7	F73B_T7D7	1	1000%
10	IFPA_T7D8	F73B_T7D8	1	1000%
10	IFPA_T7D9	F73B_T7D9	1	1000%
10	IFPA_T7E0	F73B_T7E0	1	1000%
10	IFPA_T7E1	F73B_T7E1	1	1000%
10	IFPA_T7E2	F73B_T7E2	1	1000%
10	IFPA_T7E3	F73B_T7E3	1	1000%
10	IFPA_T7E4	F73B_T7E4	1	1000%
10	IFPA_T7E5	F73B_T7E5	1	1000%
10	IFPA_T7E6	F73B_T7E6	1	1000%
10	IFPA_T7E7	F73B_T7E7	1	1000%
10	IFPA_T7E8	F73B_T7E8	1	1000%
10	IFPA_T7E9	F73B_T7E9	1	1000%
10	IFPA_T8D0	F73B_T8D0	1	1000%
10	IFPA_T8D1	F73B_T8D1	1	1000%
10	IFPA_T8D2	F73B_T8D2	1	1000%
10	IFPA_T8D3	F73B_T8D3	1	1000%
10	IFPA_T8D4	F73B_T8D4	1	1000%
10	IFPA_T8D5	F73B_T8D5	1	1000%
10	IFPA_T8D6	F73B_T8D6	1	1000%
10	IFPA_T8D7	F73B_T8D7	1	1000%
10	IFPA_T8D8	F73B_T8D8	1	1000%
10	IFPA_T8D9	F73B_T8D9	1	1000%
10	IFPA_T8E0	F73B_T8E0	1	1000%
10	IFPA_T8E1	F73B_T8E1	1	1000%
10	IFPA_T8E2	F73B_T8E2	1	1000%
10	IFPA_T8E3	F73B_T8E3	1	1000%
10	IFPA_T8E4	F73B_T8E4	1	1000%
10	IFPA_T8E5	F73B_T8E5	1	1000%
10	IFPA_T8E6	F73B_T8E6	1	1000%
10	IFPA_T8E7	F73B_T8E7	1	1000%
10	IFPA_T8E8	F73B_T8E8	1	1000%
10	IFPA_T8E9	F73B_T8E9	1	1000%
10	IFPA_T9D0	F73B_T9D0	1	1000%
10	IFPA_T9D1	F73B_T9D1	1	1000%
10	IFPA_T9D2	F73B_T9D2	1	1000%
10	IFPA_T9D3	F73B_T9D3	1	1000%
10	IFPA_T9D4	F73B_T9D4	1	1000%
10	IFPA_T9D5	F73B_T9D5	1	1000%
10	IFPA_T9D6	F73B_T9D6	1	1000%
10	IFPA_T9D7	F73B_T9D7	1	1000%
10	IFPA_T9D8	F73B_T9D8	1	1000%
10	IFPA_T9D9	F73B_T9D9	1	1000%
10	IFPA_T9E0	F73B_T9E0	1	1000%
10	IFPA_T9E1	F73B_T9E1	1	1000%
10	IFPA_T9E2	F73B_T9E2	1	1000%
10	IFPA_T9E3	F73B_T9E3	1	1000%
10	IFPA_T9E4	F73B_T9E4	1	1000%
10	IFPA_T9E5	F73B_T9E5	1	1000%
10	IFPA_T9E6	F73B_T9E6	1	1000%
10	IFPA_T9E7	F73B_T9E7	1	1000%
10	IFPA_T9E8	F73B_T9E8	1	1000%
10	IFPA_T9E9	F73B_T9E9	1	1000%
10	IFPA_T0A0	F73B_T0A0	1	1000%
10	IFPA_T0A1	F73B_T0A1	1	1000%
10	IFPA_T0A2	F73B_T0A2	1	1000%
10	IFPA_T0A3	F73B_T0A3	1	1000%
10	IFPA_T0A4	F73B_T0A4	1	1000%
10	IFPA_T0A5	F73B_T0A5	1	1000%
10	IFPA_T0A6	F73B_T0A6	1	1000%
10	IFPA_T0A7	F73B_T0A7	1	1000%
10	IFPA_T0A8	F73B_T0A8	1	1000%
10	IFPA_T0A9	F73B_T0A9	1	1000%
10	IFPA_T1A0	F73B_T1A0	1	1000%
10	IFPA_T1A1	F73B_T1A1	1	1000%
10	IFPA_T1A2	F73B_T1A2	1	1000%
10	IFPA_T1A3	F73B_T1A3	1	1000%
10	IFPA_T1A4	F73B_T1A4	1	1000%
10	IFPA_T1A5	F73B_T1A5	1	1000%
10	IFPA_T1A6	F73B_T1A6	1	1000%
10	IFPA_T1A7	F73B_T1A7	1	1000%
10	IFPA_T1A8	F73B_T1A8	1	1000%
10	IFPA_T1A9	F73B_T1A9	1	1000%
10	IFPA_T2A0	F73B_T2A0	1	1000%
10	IFPA_T2A1	F73B_T2A1	1	1000%
10	IFPA_T2A2	F73B_T2A2	1	1000%
10	IFPA_T2A3	F73B_T2A3	1	1000%
10	IFPA_T2A4	F73B_T2A4	1	1000%
10	IFPA_T2A5	F73B_T2A5	1	1000%
10	IFPA_T2A6	F73B_T2A6	1	1000%
10	IFPA_T2A7	F73B_T2A7	1	1000%
10	IFPA_T2A8	F73B_T2A8	1	1000%
10	IFPA_T2A9	F73B_T2A9	1	1000%
10	IFPA_T3A0	F73B_T3A0	1	1000%
10	IFPA_T3A1	F73B_T3A1	1	1000%
10	IFPA_T3A2	F73B_T3A2	1	1000%
10	IFPA_T3A3	F73B_T3A3	1	1000%
10	IFPA_T3A4	F73B_T3A4	1	1000%
10	IFPA_T3A5	F73B_T3A5	1	1000%
10	IFPA_T3A6	F73B_T3A6	1	1000%
10	IFPA_T3A7	F73B_T3A7	1	1000%
10	IFPA_T3A8	F73B_T3A8	1	1000%
10	IFPA_T3A9	F73B_T3A9	1	1000%
10	IFPA_T4A0	F73B_T4A0	1	1000%
10	IFPA_T4A1	F73B_T4A1	1	1000%
10	IFPA_T4A2	F73B_T4A2	1	1000%
10	IFPA_T4A3	F73B_T4A3	1	1000%
10	IFPA_T4A4	F73B_T4A4	1	1000%
10	IFPA_T4A5	F73B_T4A5	1	1000%
10	IFPA_T4A6	F73B_T4A6	1	1000%
10	IFPA_T4A7	F73B_T4A7	1	1000%
10	IFPA_T4A8	F73B_T4A8	1	1000%
10	IFPA_T4A9	F73B_T4A9	1	1000%
10	IFPA_T5A0	F73B_T5A0	1	1000%
10	IFPA_T5A1	F73B_T5A1	1	1000%
10	IFPA_T5A2	F73B_T5A2	1	1000%
10	IFPA_T5A3	F73B_T5A3	1	1000%
10	IFPA_T5A4	F73B_T5A4	1	1000%
10	IFPA_T5A5	F73B_T5A5	1	1000%
10	IFPA_T5A6	F73B_T5A6	1	1000%
10	IFPA_T5A7	F73B_T5A7	1	1000%
10	IFPA_T5A8	F73B_T5A8	1	1000%
10	IFPA_T5A9	F73B_T5A9	1	1000%
10	IFPA_T6A0	F73B_T6A0	1	1000%
10	IFPA_T6A1	F73B_T6A1	1	1000%
10	IFPA_T6A2	F73B_T6A2	1	1000%
10	IFPA_T6A3	F73B_T6A3	1	1000%
10	IFPA_T6A4	F73B_T6A4	1	1000%
10	IFPA_T6A5	F73B_T6A5	1	1000%
10	IFPA_T6A6	F73B_T6A6	1	1000%
10	IFPA_T6A7	F73B_T6A7	1	1000%
10	IFPA_T6A8	F73B_T6A8	1	1000%
10	IFPA_T6A9	F73B_T6A9	1	1000%
10	IFPA_T7A0	F73B_T7A0	1	1000%
10	IFPA_T7A1	F73B_T7A1	1	1000%
10	IFPA_T7A2	F73B_T7A2	1	1000%
10	IFPA_T7A3	F73B_T7A3	1	1000%
10	IFPA_T7A4	F73B_T7A4	1	1000%
10	IFPA_T7A5	F73B_T7A5	1	1000%
10	IFPA_T7A6	F73B_T7A6	1	1000%
10	IFPA_T7A7	F73B_T7A7	1	1000%
10	IFPA_T7A8	F73B_T7A8	1	1000%
10	IFPA_T7A9	F73B_T7A9	1	10

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



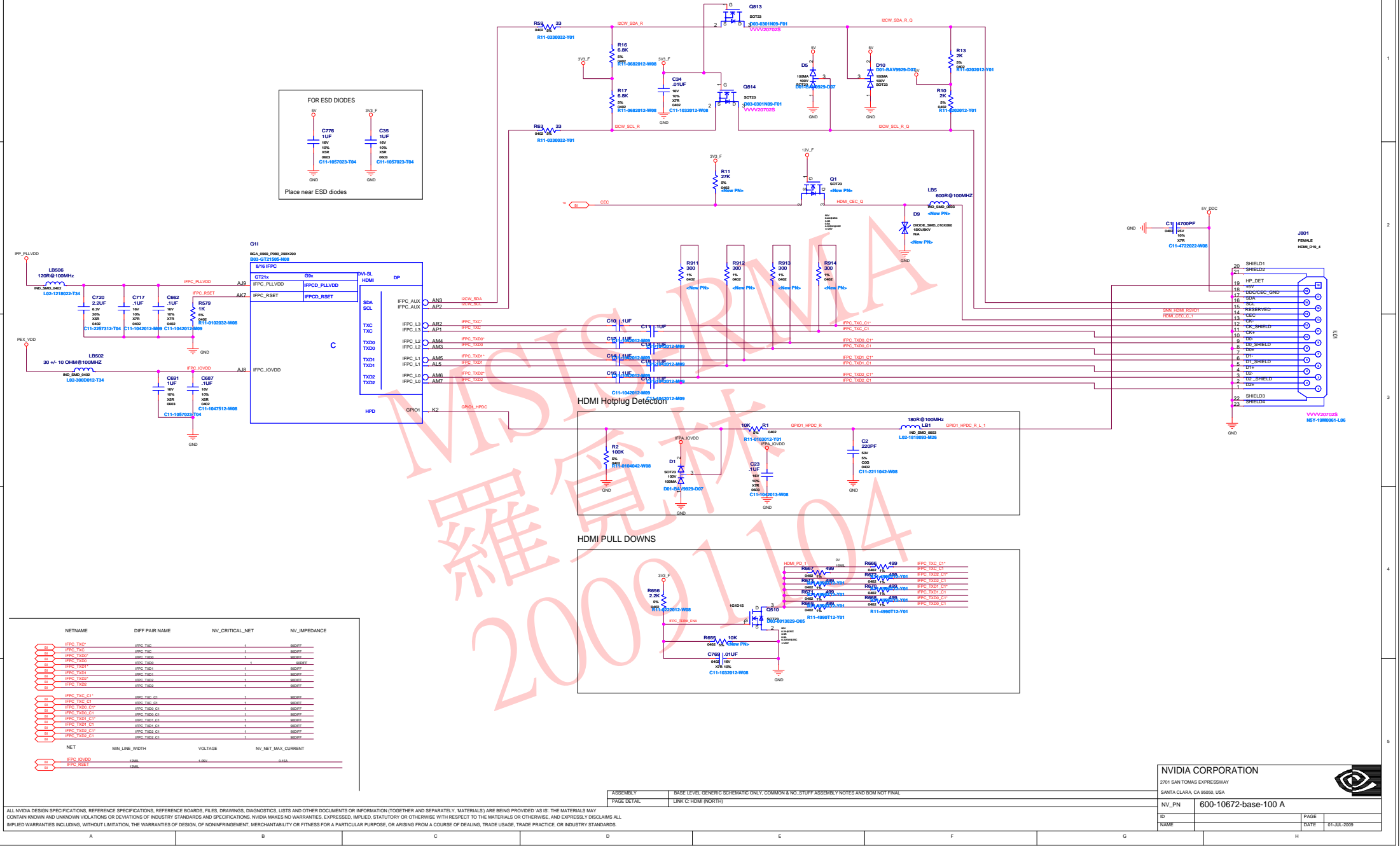
NV_PN	600-10672-base-100 A
-------	----------------------

ID		PAGE	
NAME		DATE	01-JUL-2009

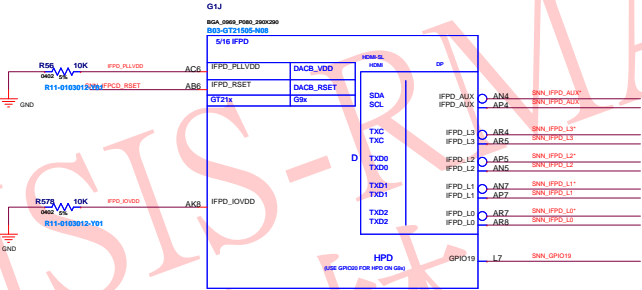
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK A/R: DVI-I (SOUTH)

LINK C: HDMI (North)



LINK D: UNUSED

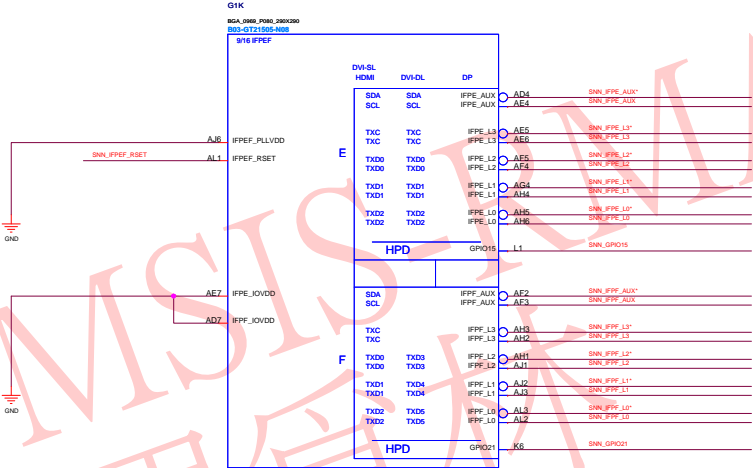


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK D (UNUSED)

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN		600-10672-base-100 A	
ID		PAGE	
NAME		DATE	01-JUL-2009

LINK E/F: (UNUSED)

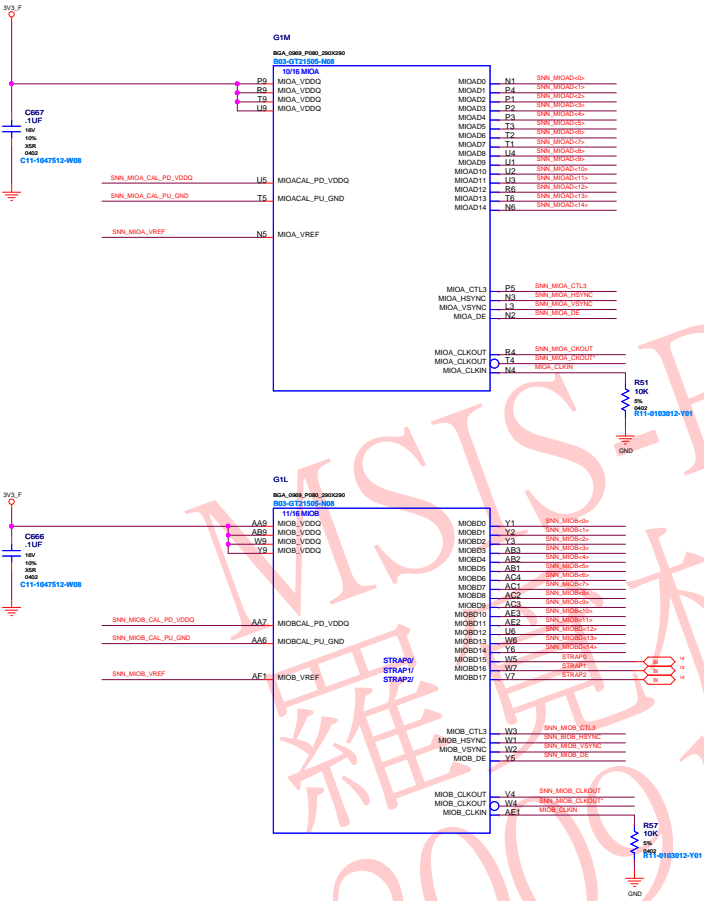


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE, WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LINK E/F: (UNUSED)

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN		600-10672-base-100 A	
ID		PAGE	
NAME		DATE	01-JUL-2009

MIOA/B UNUSED



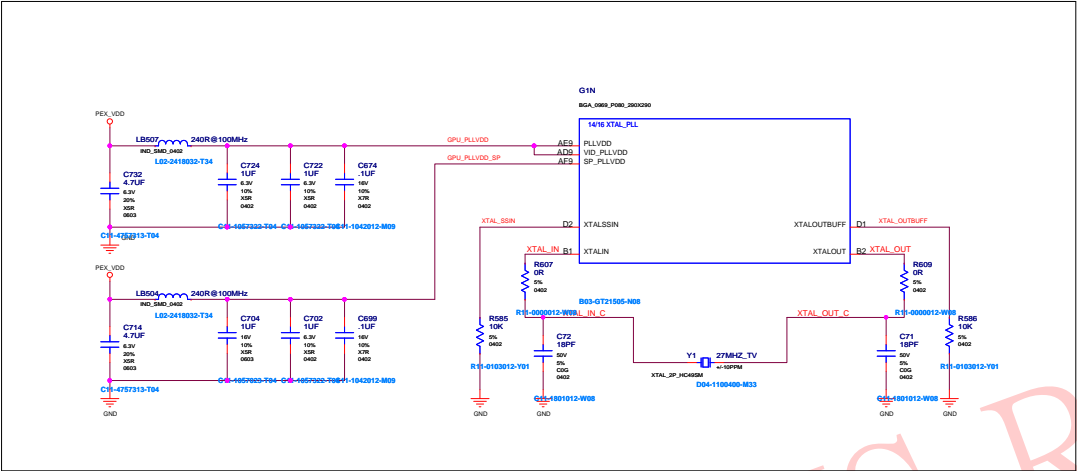
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE, WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB (UNUSED)

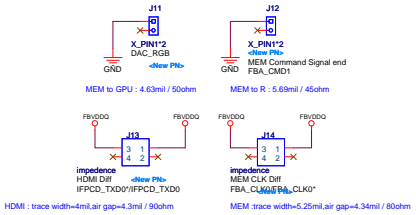
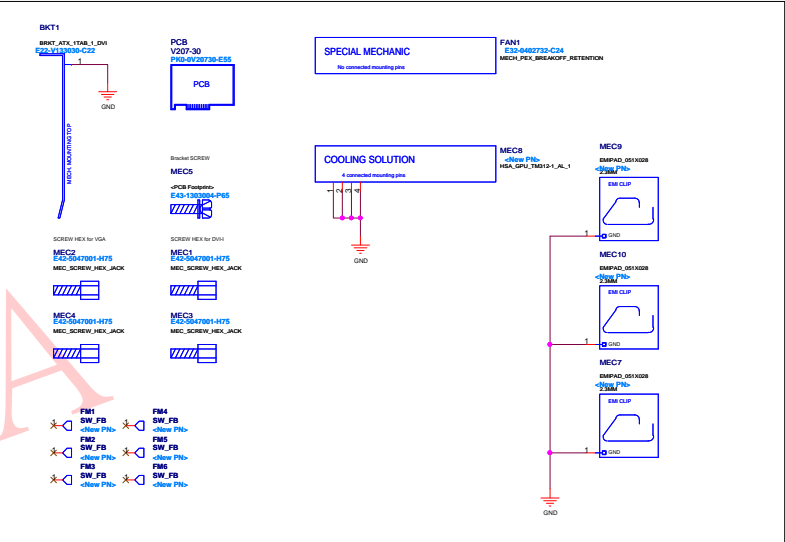
NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01 JUL 2009

XTAL, MECHANICALS

XTAL/GPU_PLLVDD



MECHANICALS & THERMALS



NETNAME	MIN. LINE WIDTH
GPU_PLLVDD	120µm
GPU_PLLVDD_SP	120µm
XTAL_IN	100µm
XTAL_OUT	100µm

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN

600-10672-base-100 A

ID

PAGE

1

NAME

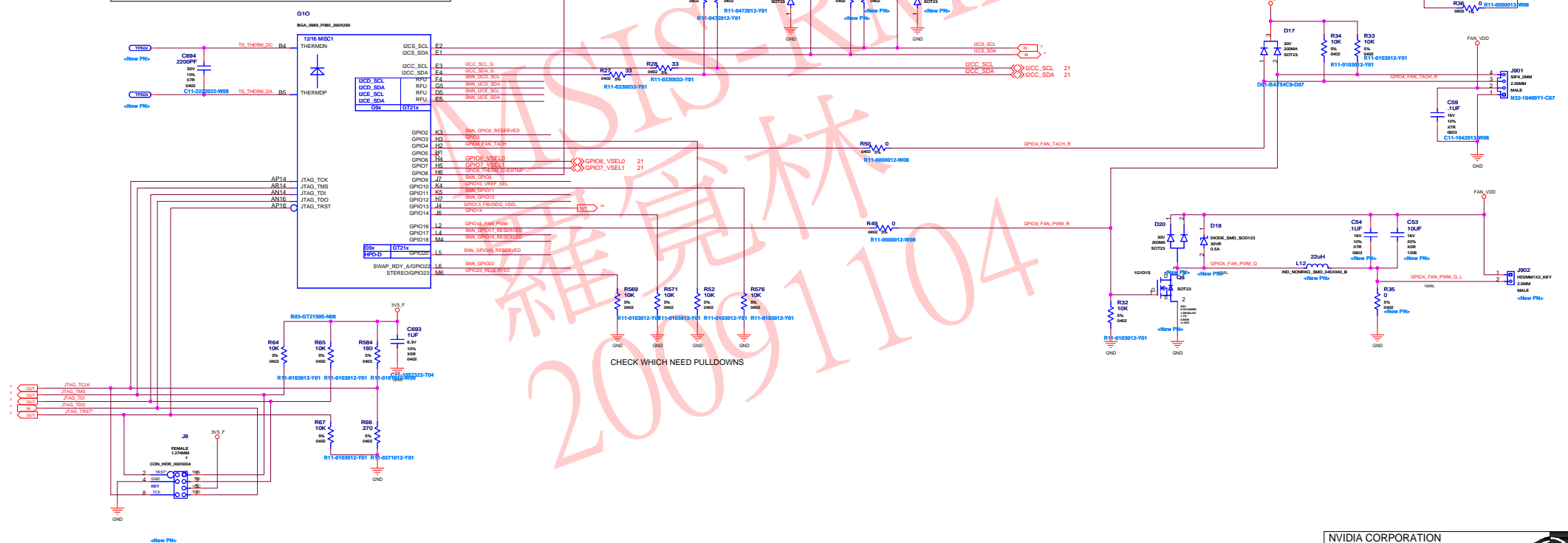
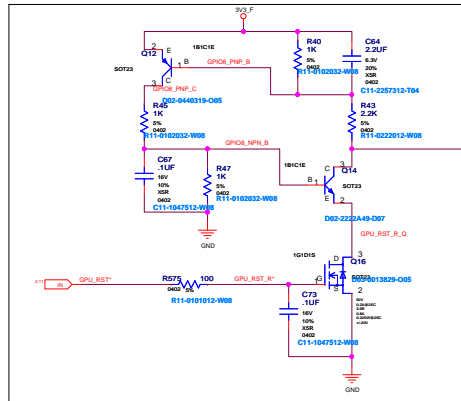
DATE

01-JUL-2009


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

THERM ALERT, FAN CONTROL, GPIO & JTAG

THERM ALERT LATCH



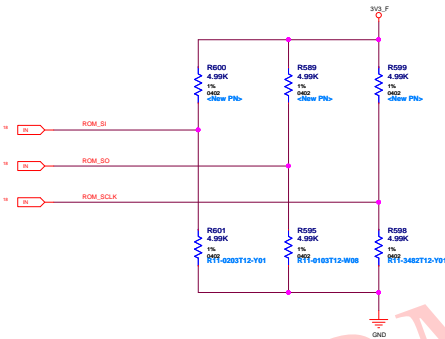
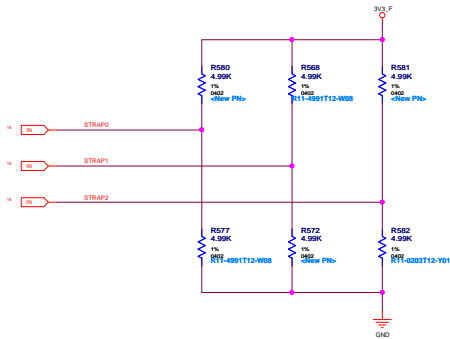
NETNAME		MIN_LINE_WIDTH	CURRENT
U1	THERM_DC	100MIL	
U2	THERM_CA	100MIL	
U3	FAN_VDD	80MIL	
U4	FAN_PWM	80MIL	
U5	THERM_CA_B	100MIL	
U6	THERM_DC_B	100MIL	
FAN_VDD	FAN_VDD	100MIL	3A

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-10672-base-100 A		
ID		PAGE	
NAME		DATE	01-JUL-2009

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

STRAPPING, VBIOS, INFOROM

STRAPPING OPTIONS

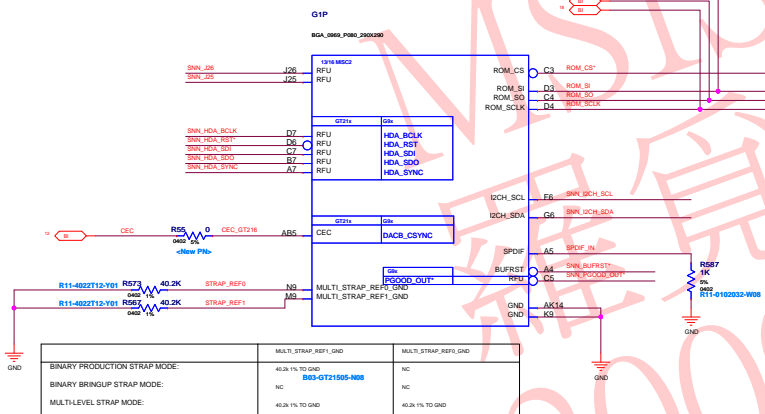
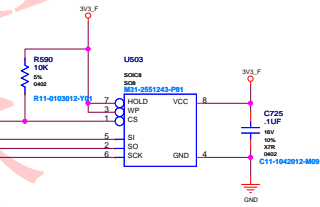


STRAP1[3..0] = 0x8 (JGIO_PADCFG DSKTOP default plus 0x8)
STRAP2[3..0] = 0x8 (PCL_DEVID = 0xCAB)
ROM_SC0[0] = 1 (VGA Device Enable)
ROM_SC0[1] = 0 (SMB_ALT_ADDR, default (1GPU))
ROM_SC0[2] = 0 (FB apert. size 256MB, default)
ROM_SC0[3] = 0 (XCLK_417, default)
ROM_SCLQ[0] = 0 (PEX_PLL_EN_TERM100 disabled, default)
ROM_SCLQ[1] = 1 (SLT_CLK_CFG, default)
ROM_SCLQ[2] = 1 (VBIOS RM present, default)
ROM_SCLQ[3] = 0 (PCL_DEVID[4] = 0)

ROM_SK[3..0] = RAMCFG[3..0]
0x0001 Qimonda
0x0010 Hynix
0x0011 Samsung

128-bit, GDDR5
128-bit, GDDR5
128-bit, GDDR5

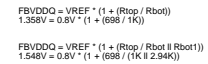
BIOS ROM(serial)



	MULTI_STRAP_REF0_GND	MULTI_STRAP_REF1_GND
BINARY PRODUCTION STRAP MODE:		
BINARY BRINGUP STRAP MODE:	NC	NC
MULTI-LEVEL STRAP MODE:	40.2K 1% TO GND	40.2K 1% TO GND

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE, WITH RESPECT TO THE MATERIALS AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

FBVDDQ Power Supply 1.35-1.50V@15A

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



NV_PN	600-10672-base-100 A
-------	----------------------

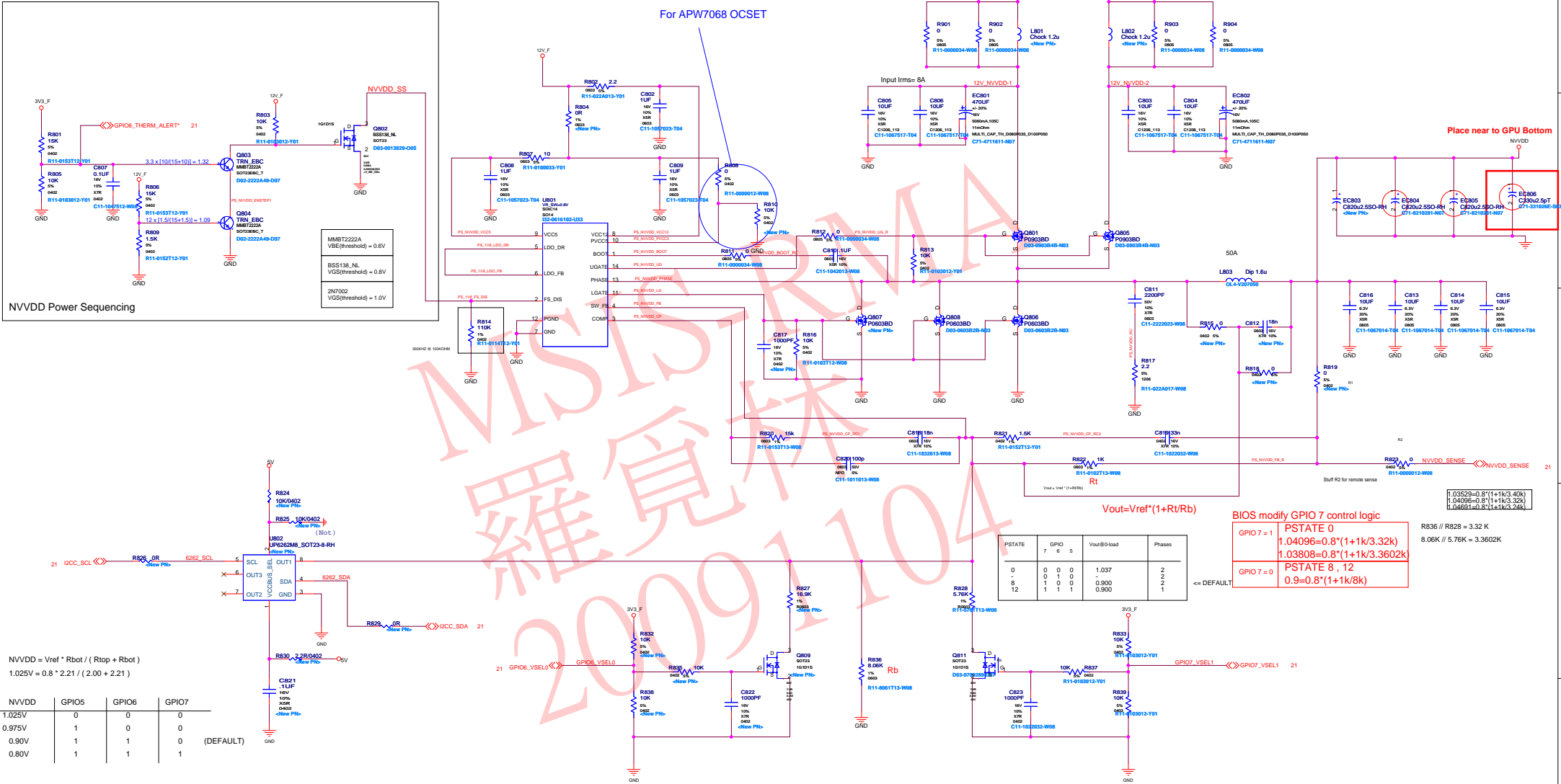
ID	PAGE
NAME	DATE 01-JUL-2009

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBVDDQ SINGLE PHASE SWITCHER, PEX_VDD LINEAR

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS AND HEREBY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

A		B		C		D		E		F		G		H	
Title: Baseunit Report		FBA_CMD<26> 3.4C 4.1B		FBA_CMD<26> 3.5B		FBC_D<4> 6.2A 7.4D		GPIOX_FAN_PWM_Q_1 17.4H		NVDDO_EAP 21.4C 21.5B		PEX_TX0* 2.2G 2.3C			
Design: design		FBA_CMD<27> 3.4C 4.1E		FBA_WOK01 3.4A 4.1F 4.5A		FBC_D<4> 6.2A 7.4D		GPIOX_PLVDDO 16.1B 16.5G		NVDDO_ENA 21.3C		PEX_T3B 2.2G 2.4D			
Date: Jun 10 09:58 2020		FBA_CMD<28> 3.4C 4.1E		FBA_WOK01* 3.4A 4.1F 4.5A		FBC_D<4> 6.2A 7.4D		GPIOX_BNAP 16.1B 16.5G		NVDDO_ENA2 21.3B		PEX_T3P 2.2G 2.4C			
		FBA_CMD<29> 3.4C 4.1B		FBA_WOK01_CT 4.2F 4.5B		FBC_D<4> 6.3A 7.5D		GPU_RST* 2.2G 11.5D 17.2A		NVDDO_ENA3 21.3B		PEX_T3Q 2.2G 2.4D			
		FBA_CMD<30> 3.4C 4.1E		FBA_WOK29 3.4A 4.1F 4.5C		FBC_D<4> 6.3A 7.5D		GPU_RST_R* 17.2B		NVDDO_PSI 21.3B 21.5A		PEX_T3R 2.2G 2.4D			
		FBA_D<0> 3.1B 4.4B		FBA_WOK29_CT 4.2F 4.5C		FBC_D<4> 6.3A		GPU_RST_R_Q 17.2B		NVDDO_PSBIN 21.4C 21.5B		PEX_TX10 2.2G 2.4D			
		FBA_D<0> 3.1A 4.1F 4.4A		FBA_WOK40 3.4A 4.1F 4.5D		FBC_D<4> 6.3A		GPU_TESTMODE 2.1B		NVDDO_PSL_R 21.3B 21.5D		PEX_TX1P 2.2G 2.4C			
		FBA_D<1> 3.1B 4.4B		FBA_WOK40* 3.4A 4.1F 4.5D		FBC_D<4> 6.3A		HDM_CEC_C_1 12.3G		NVDDO_SDA 21.3B 21.5A		PEX_TX11 2.2G 2.4D			
		FBA_D<2> 3.1B 4.4B		FBA_WOK45 3.4A 4.1F 4.5D		FBC_D<4> 6.3A		HDM_CEC_Q_1 12.2E		NVDDO_SDA2 2.4F 21.4A		PEX_TX11* 2.2G 2.4C			
		FBA_D<3> 3.1B 4.4B		FBA_WOK45_CT 4.2F 4.5D		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB 2.2G 9.3C		PEX_TX12 2.2G 2.4D			
		FBA_D<4> 3.1B 4.4B		FBA_WOK47 3.4A 4.1F 4.5E		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX12* 2.2G 2.4C			
		FBA_D<5> 3.1B 4.4B		FBA_WOK47* 3.4A 4.1F 4.5E		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX13 2.2G 2.4C			
		FBA_D<6> 3.1B 4.4B		FBA_ZD0 4.2B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX13 2.2G 2.4C			
		FBA_D<7> 3.1B 4.4B		FBA_ZD1 4.2E		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX14 2.2G 2.4C			
		FBA_D<8> 3.1B 4.4B		FBC_CLK0 6.4D 7.1G 7.2A		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<9> 3.1B 4.4B		FBC_CLK0* 6.4D 7.1G 7.2A		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<10> 3.1B 4.4B		FBC_CLK0_TERM 7.2B 7.2G		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<11> 3.1B 4.5B		FBC_CLK1 6.4D 7.1G 7.2D		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<12> 3.1B 4.5B		FBC_CLK1* 6.4D 7.1G 7.2D		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<13> 3.1B 4.5B		FBC_CLK1_TERM 7.2B 7.2G		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<14> 3.1B 4.5B		FBC_CMD<0> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<15> 3.2B 4.5B		FBC_CMD<0> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<16> 3.2B 4.4C		FBC_CMD<0> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<17> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<18> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<19> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<20> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<21> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<22> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<23> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<24> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<25> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<26> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<27> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<28> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<29> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<30> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<31> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<32> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<33> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<34> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<35> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<36> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<37> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<38> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<39> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<40> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<41> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<42> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<43> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<44> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<45> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<46> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<47> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<48> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<49> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<50> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<51> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<52> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<53> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<54> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<55> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<56> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<57> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<58> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<59> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<60> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<61> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<62> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<63> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<64> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<65> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<66> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<67> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<68> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<69> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 12.4E		NVDDO_SDB2 21.3B 21.5A		PEX_TX15 2.2G 2.4C			
		FBA_D<70> 3.2B 4.4C		FBC_CMD<1> 6.3C 7.1B		FBC_D<4> 6.3A		HDM_PD_1 1							

Power Supply III: NVVDD



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY) ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE, WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.