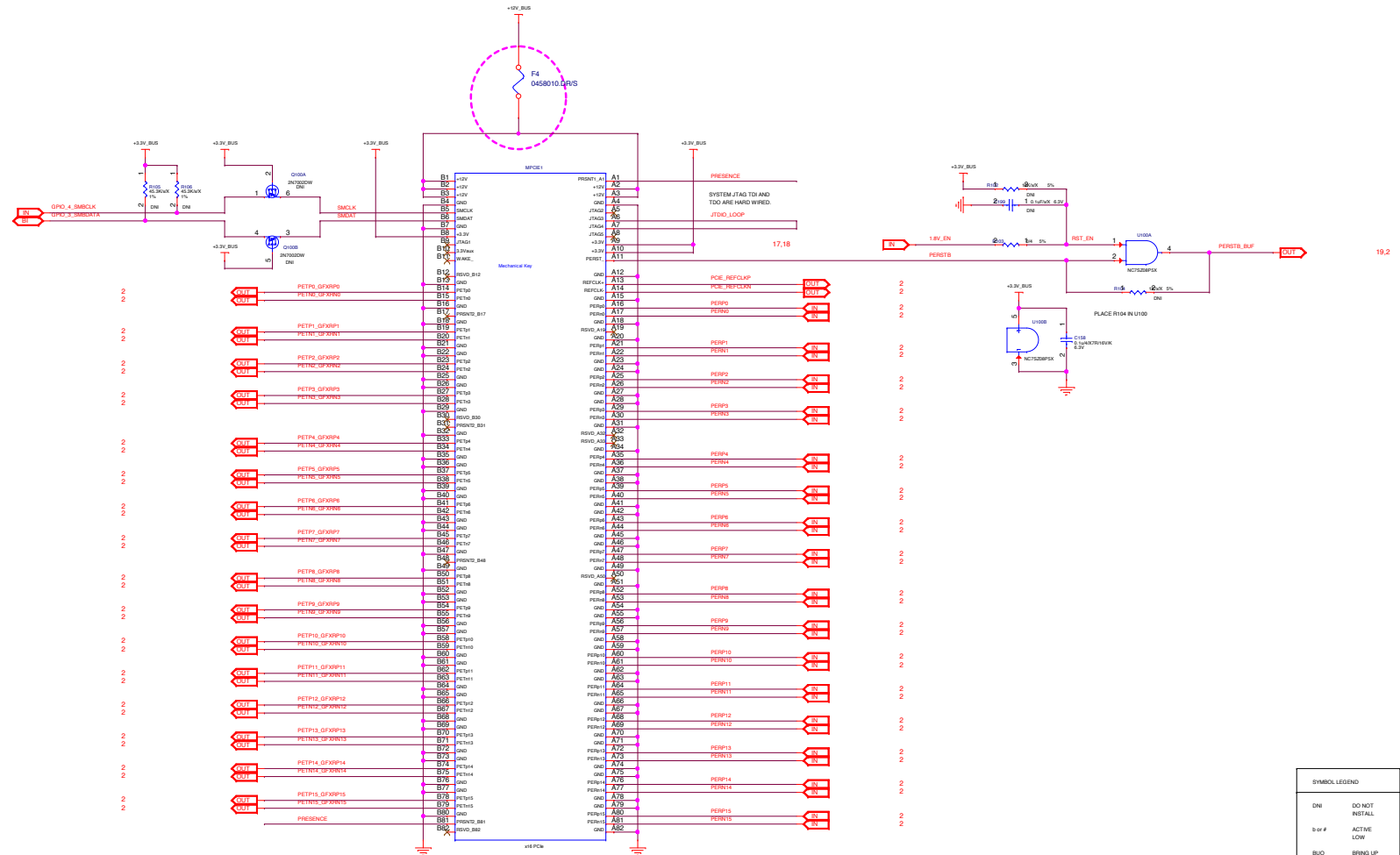
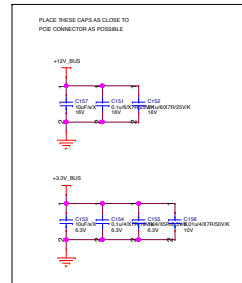
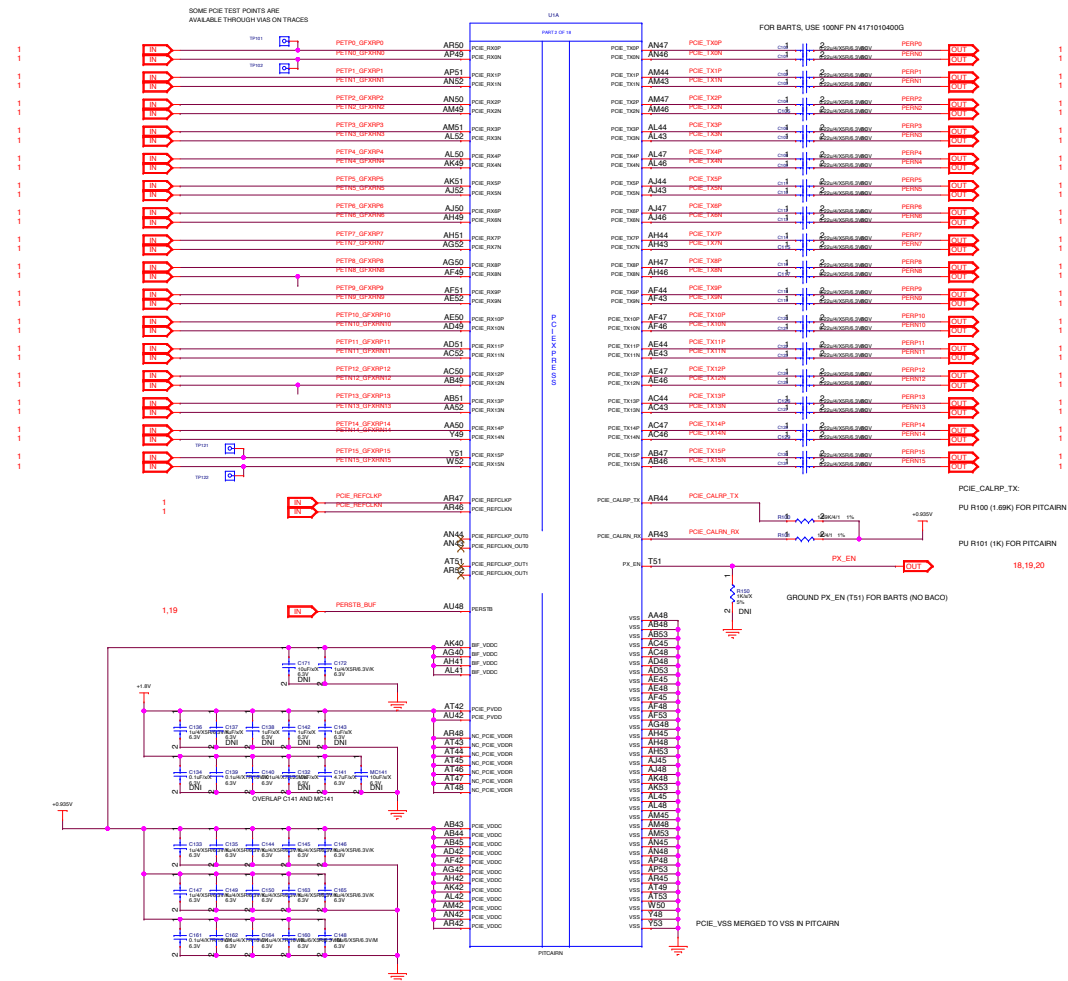


(1) PCI-EXPRESS EDGE CONNECTOR

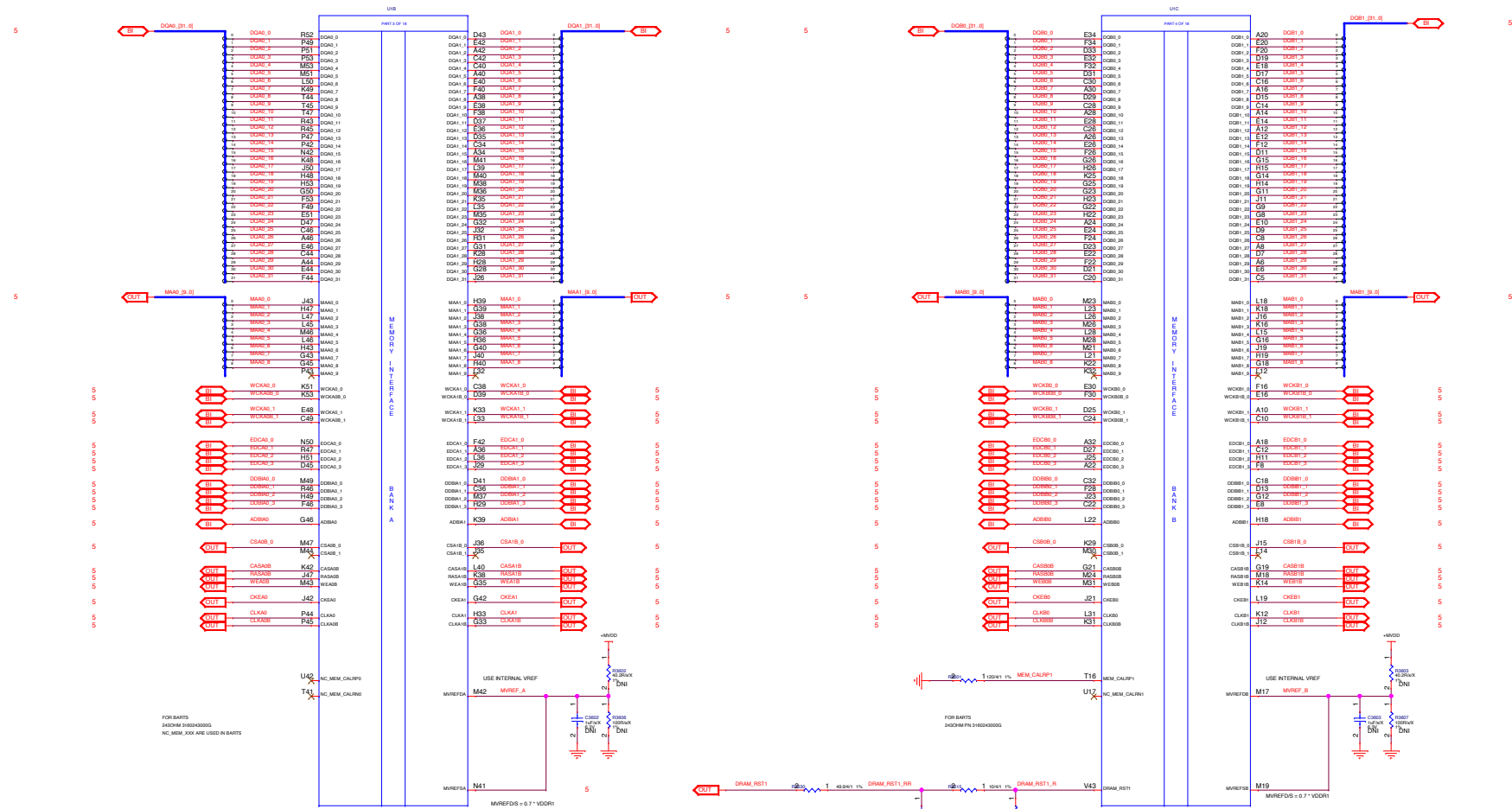


SYMBOL LEGEND	
DNI	DO NOT INSTALL
b or #	ACTIVE LOW
BLO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

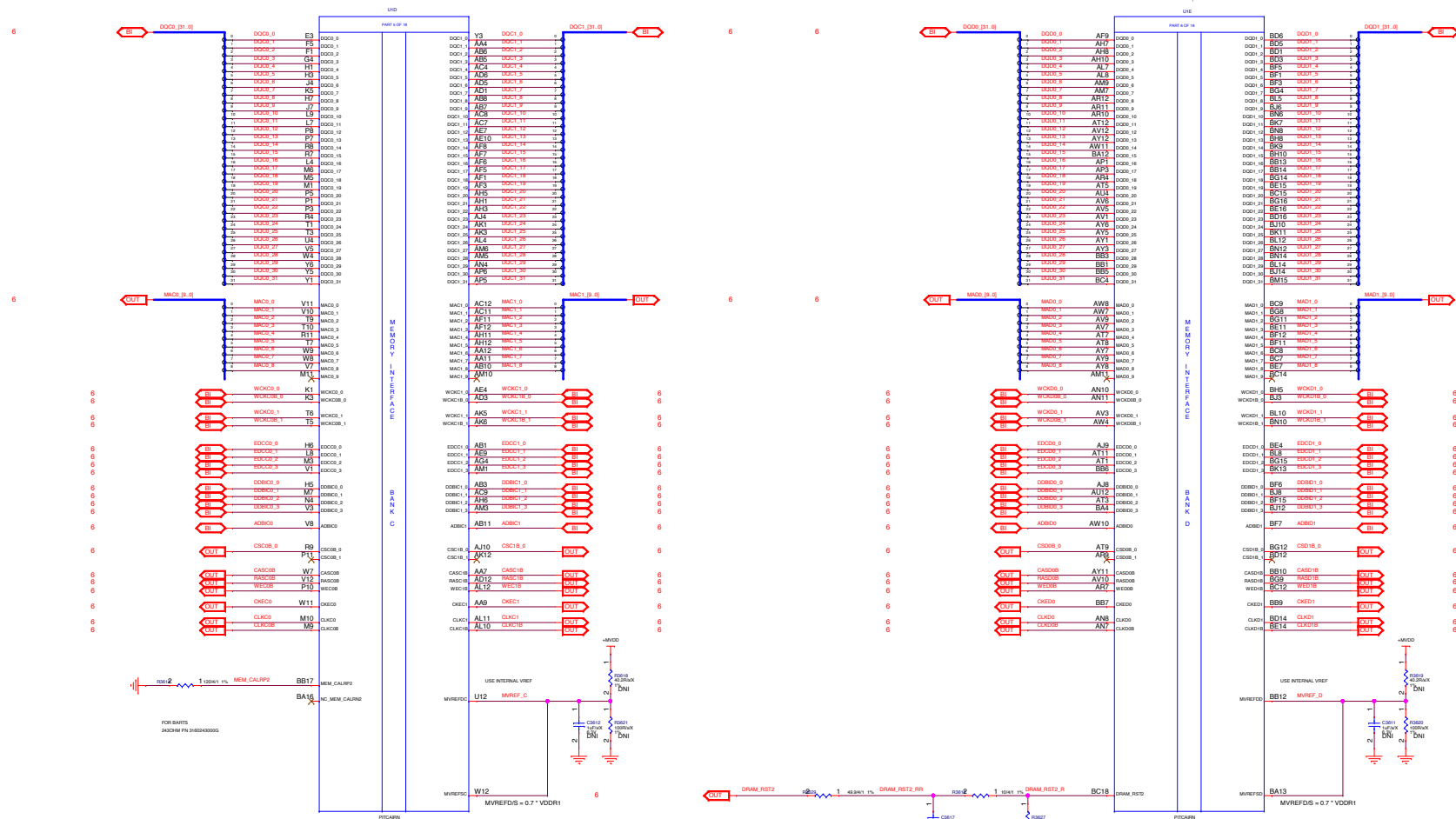
(2) CURACAO PCIE INTERFACE



(3) CURACAO MEM INTERFACE CH AB

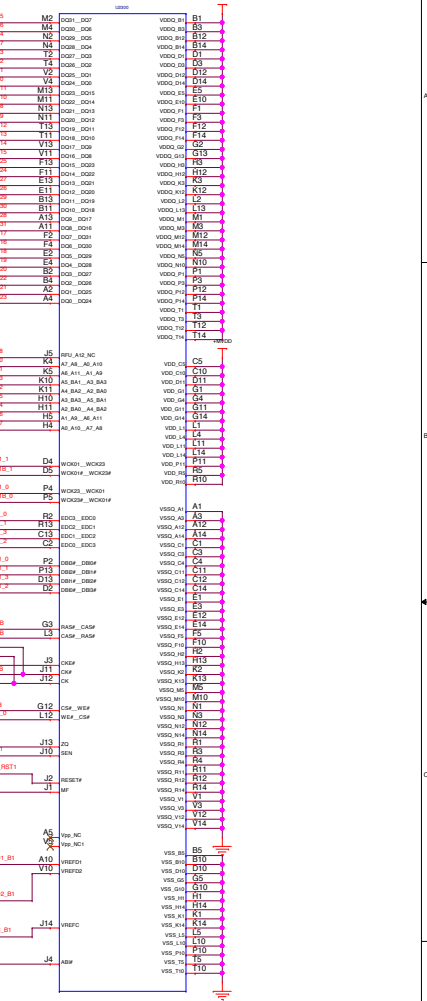
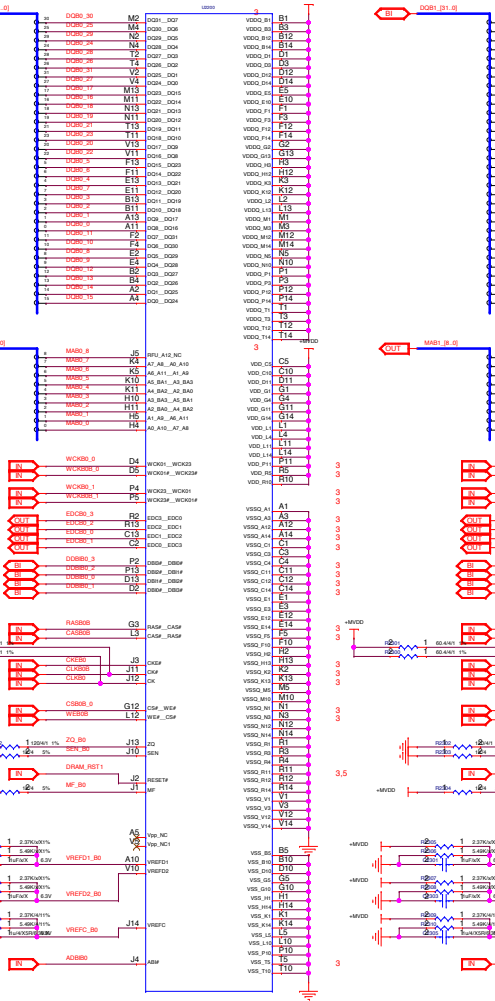
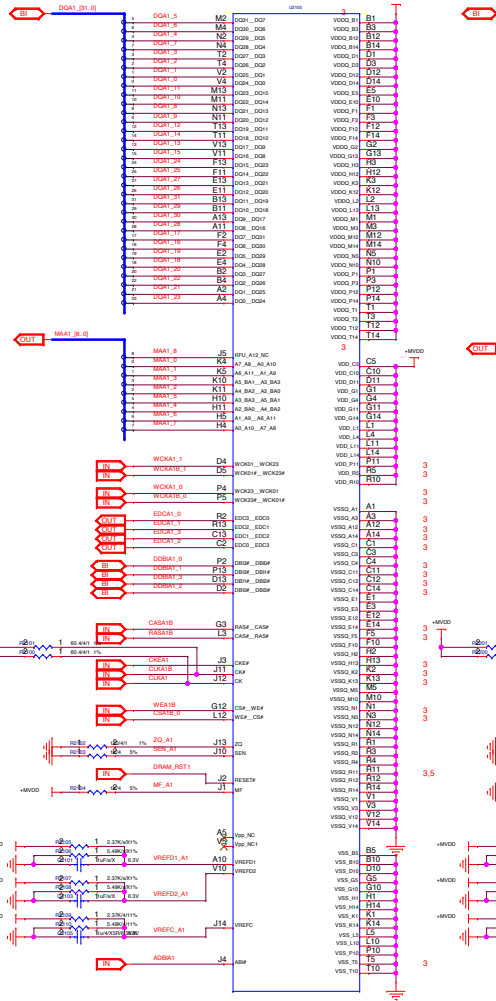


(4) CURACAO MEM INTERFACE CH CD



The diagram illustrates a complex PCB layout with a top layer (blue) and a bottom layer (red). It features a central microcontroller (M0) and various peripheral components. Key components and their connections include:

- Microcontroller (M0):** Connected to various pins (e.g., M0_0, M0_1, M0_2, M0_3, M0_4, M0_5, M0_6, M0_7, M0_8, M0_9, M0_10, M0_11, M0_12, M0_13, M0_14, M0_15, M0_16, M0_17, M0_18, M0_19, M0_20, M0_21, M0_22, M0_23, M0_24, M0_25, M0_26, M0_27, M0_28, M0_29, M0_30, M0_31, M0_32, M0_33, M0_34, M0_35, M0_36, M0_37, M0_38, M0_39, M0_40, M0_41, M0_42, M0_43, M0_44, M0_45, M0_46, M0_47, M0_48, M0_49, M0_50, M0_51, M0_52, M0_53, M0_54, M0_55, M0_56, M0_57, M0_58, M0_59, M0_60, M0_61, M0_62, M0_63, M0_64, M0_65, M0_66, M0_67, M0_68, M0_69, M0_70, M0_71, M0_72, M0_73, M0_74, M0_75, M0_76, M0_77, M0_78, M0_79, M0_80, M0_81, M0_82, M0_83, M0_84, M0_85, M0_86, M0_87, M0_88, M0_89, M0_90, M0_91, M0_92, M0_93, M0_94, M0_95, M0_96, M0_97, M0_98, M0_99, M0_100).
- USB-to-UART Bridge (M1):** Connected to various pins (e.g., M1_0, M1_1, M1_2, M1_3, M1_4, M1_5, M1_6, M1_7, M1_8, M1_9, M1_10, M1_11, M1_12, M1_13, M1_14, M1_15, M1_16, M1_17, M1_18, M1_19, M1_20, M1_21, M1_22, M1_23, M1_24, M1_25, M1_26, M1_27, M1_28, M1_29, M1_30, M1_31, M1_32, M1_33, M1_34, M1_35, M1_36, M1_37, M1_38, M1_39, M1_40, M1_41, M1_42, M1_43, M1_44, M1_45, M1_46, M1_47, M1_48, M1_49, M1_50, M1_51, M1_52, M1_53, M1_54, M1_55, M1_56, M1_57, M1_58, M1_59, M1_60, M1_61, M1_62, M1_63, M1_64, M1_65, M1_66, M1_67, M1_68, M1_69, M1_70, M1_71, M1_72, M1_73, M1_74, M1_75, M1_76, M1_77, M1_78, M1_79, M1_80, M1_81, M1_82, M1_83, M1_84, M1_85, M1_86, M1_87, M1_88, M1_89, M1_90, M1_91, M1_92, M1_93, M1_94, M1_95, M1_96, M1_97, M1_98, M1_99, M1_100).
- USB-to-UART Bridge (M2):** Connected to various pins (e.g., M2_0, M2_1, M2_2, M2_3, M2_4, M2_5, M2_6, M2_7, M2_8, M2_9, M2_10, M2_11, M2_12, M2_13, M2_14, M2_15, M2_16, M2_17, M2_18, M2_19, M2_20, M2_21, M2_22, M2_23, M2_24, M2_25, M2_26, M2_27, M2_28, M2_29, M2_30, M2_31, M2_32, M2_33, M2_34, M2_35, M2_36, M2_37, M2_38, M2_39, M2_40, M2_41, M2_42, M2_43, M2_44, M2_45, M2_46, M2_47, M2_48, M2_49, M2_50, M2_51, M2_52, M2_53, M2_54, M2_55, M2_56, M2_57, M2_58, M2_59, M2_60, M2_61, M2_62, M2_63, M2_64, M2_65, M2_66, M2_67, M2_68, M2_69, M2_70, M2_71, M2_72, M2_73, M2_74, M2_75, M2_76, M2_77, M2_78, M2_79, M2_80, M2_81, M2_82, M2_83, M2_84, M2_85, M2_86, M2_87, M2_88, M2_89, M2_90, M2_91, M2_92, M2_93, M2_94, M2_95, M2_96, M2_97, M2_98, M2_99, M2_100).
- USB-to-UART Bridge (M3):** Connected to various pins (e.g., M3_0, M3_1, M3_2, M3_3, M3_4, M3_5, M3_6, M3_7, M3_8, M3_9, M3_10, M3_11, M3_12, M3_13, M3_14, M3_15, M3_16, M3_17, M3_18, M3_19, M3_20, M3_21, M3_22, M3_23, M3_24, M3_25, M3_26, M3_27, M3_28, M3_29, M3_30, M3_31, M3_32, M3_33, M3_34, M3_35, M3_36, M3_37, M3_38, M3_39, M3_40, M3_41, M3_42, M3_43, M3_44, M3_45, M3_46, M3_47, M3_48, M3_49, M3_50, M3_51, M3_52, M3_53, M3_54, M3_55, M3_56, M3_57, M3_58, M3_59, M3_60, M3_61, M3_62, M3_63, M3_64, M3_65, M3_66, M3_67, M3_68, M3_69, M3_70, M3_71, M3_72, M3_73, M3_74, M3_75, M3_76, M3_77, M3_78, M3_79, M3_80, M3_81, M3_82, M3_83, M3_84, M3_85, M3_86, M3_87, M3_88, M3_89, M3_90, M3_91, M3_92, M3_93, M3_94, M3_95, M3_96, M3_97, M3_98, M3_99, M3_100).
- USB-to-UART Bridge (M4):** Connected to various pins (e.g., M4_0, M4_1, M4_2, M4_3, M4_4, M4_5, M4_6, M4_7, M4_8, M4_9, M4_10, M4_11, M4_12, M4_13, M4_14, M4_15, M4_16, M4_17, M4_18, M4_19, M4_20, M4_21, M4_22, M4_23, M4_24, M4_25, M4_26, M4_27, M4_28, M4_29, M4_30, M4_31, M4_32, M4_33, M4_34, M4_35, M4_36, M4_37, M4_38, M4_39, M4_40, M4_41, M4_42, M4_43, M4_44, M4_45, M4_46, M4_47, M4_48, M4_49, M4_50, M4_51, M4_52, M4_53, M4_54, M4_55, M4_56, M4_57, M4_58, M4_59, M4_60, M

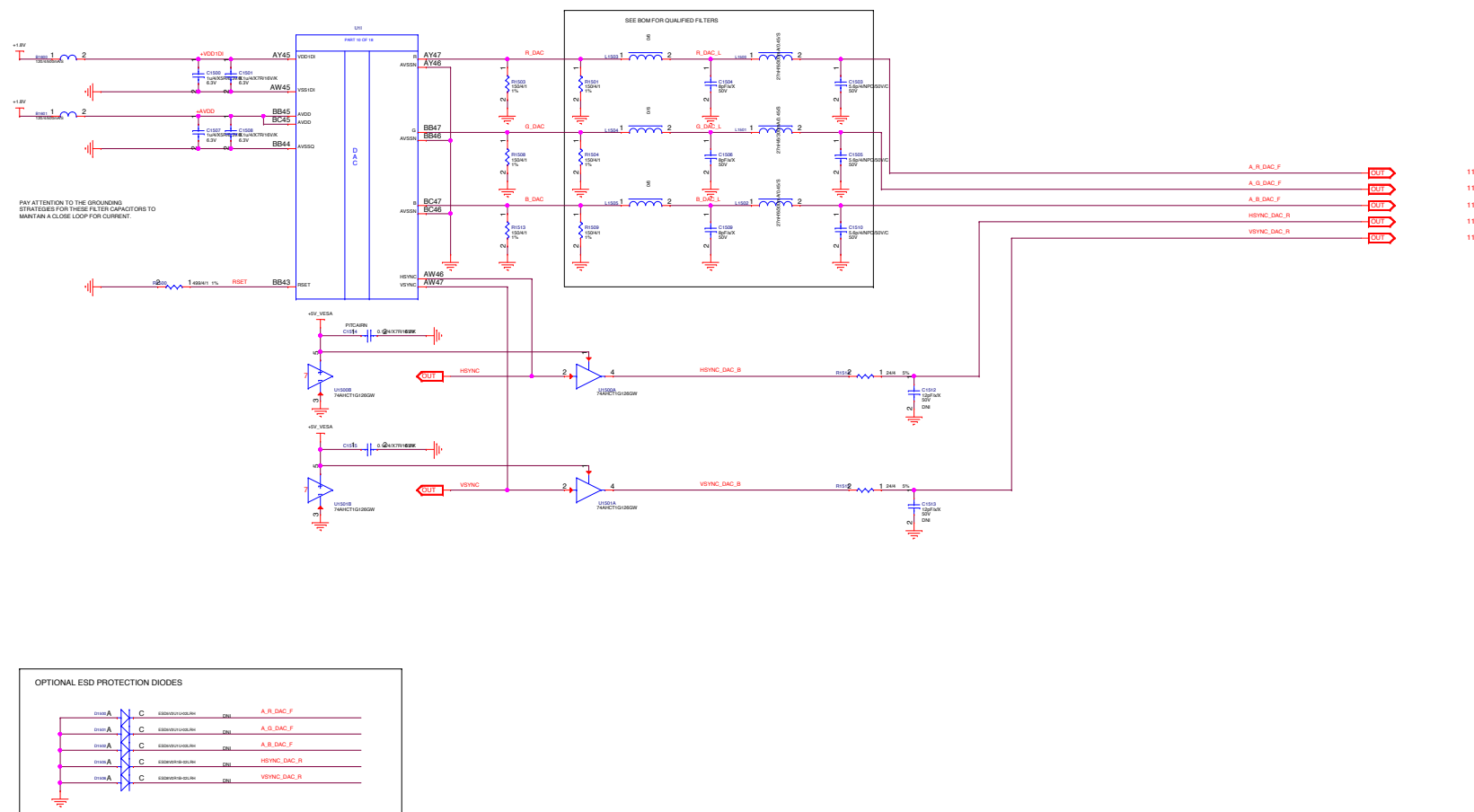


GIGABYTE			
GDDR5 MEM CH AB			
Size	Document Number		Rev
Custom	GV-R927XOC-2GD		1.02
Date:	Thursday, July 31, 2014	Sheet	5 of 26

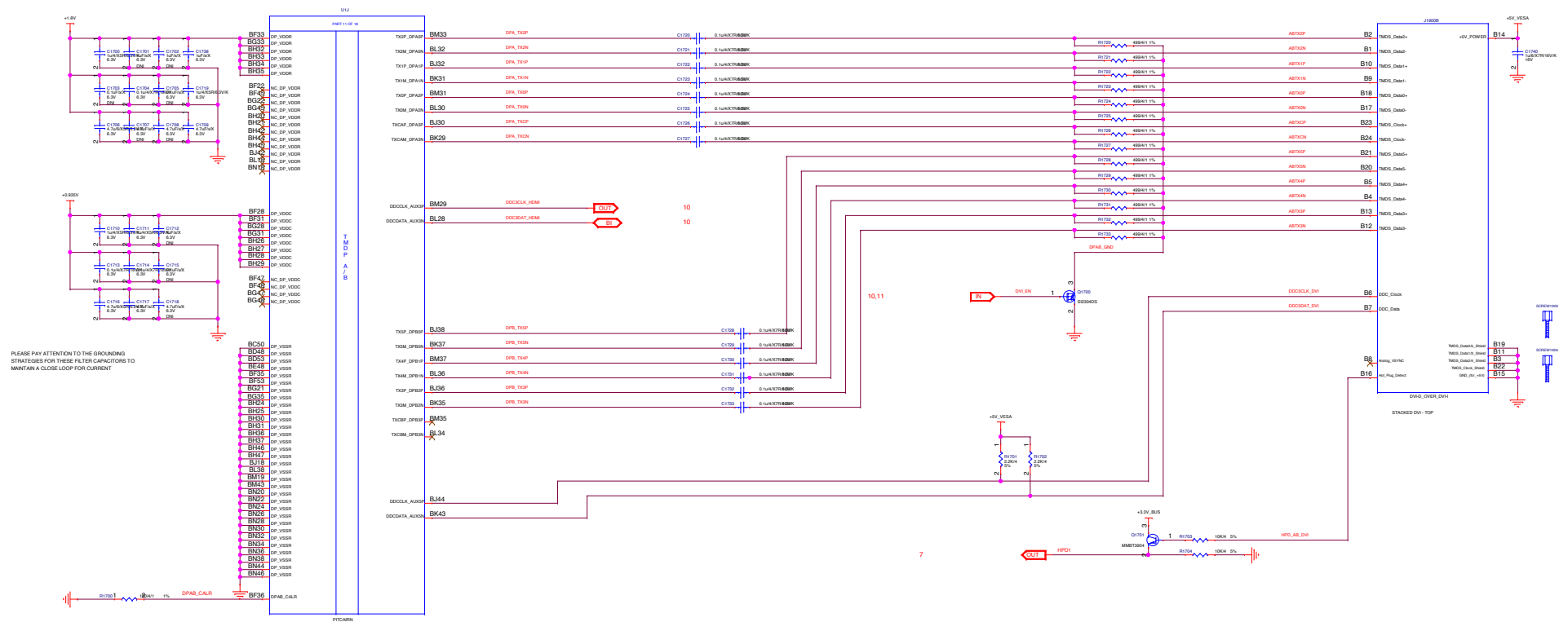
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(8) CURACAO DAC




(9) CURACAO TMDPAB sDVI

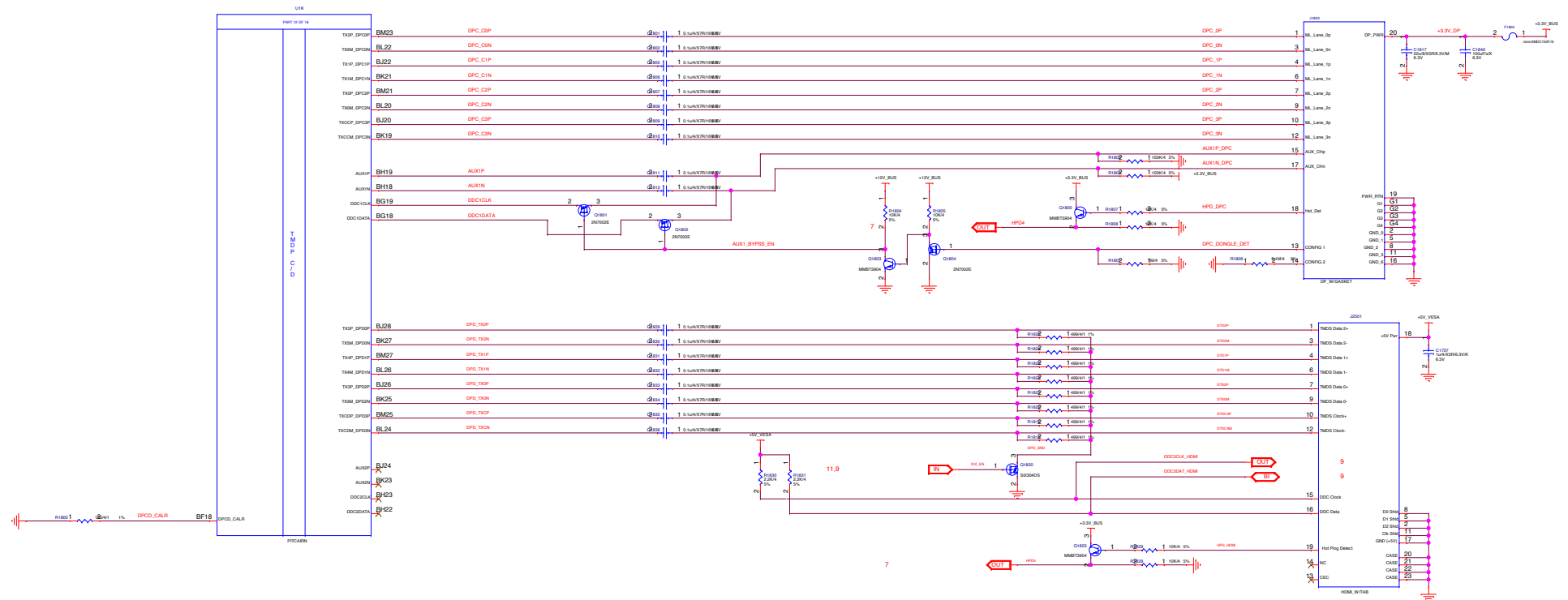


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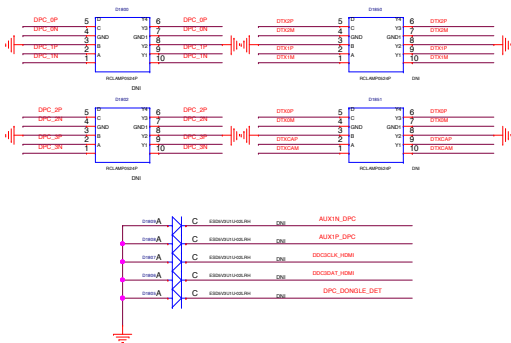



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<p>SHEET: CURACAO PITCARAO TMOFAB DEV1 TOP</p> <p>DATE: Wed Jul 17 02:26:13 2013</p>	<p>REV: 1.0</p>	<p>TITLE:</p> <p><TITLE></p>
<p>SHEET NUMBER: 9 OF 26</p>		
<p>DOCUMENT NUMBER: GV-P827XOC-XGD</p>		

(10) CURACAO TMDPCD DP HDMI

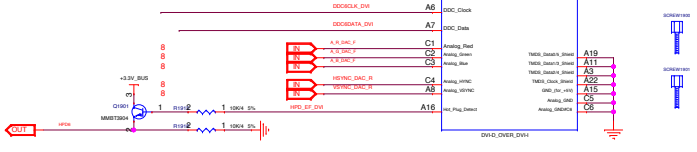
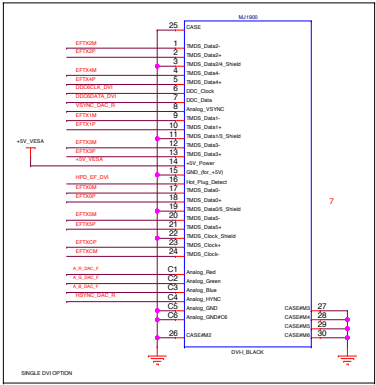
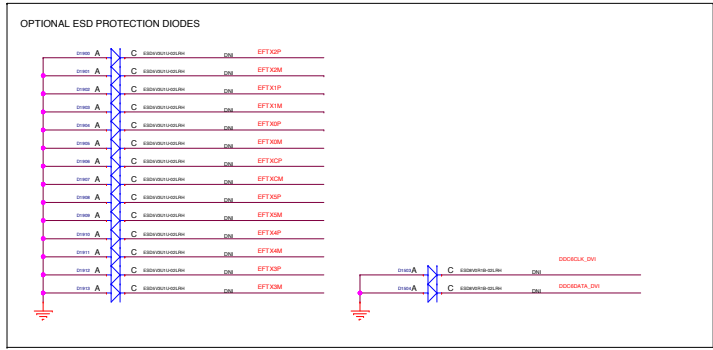
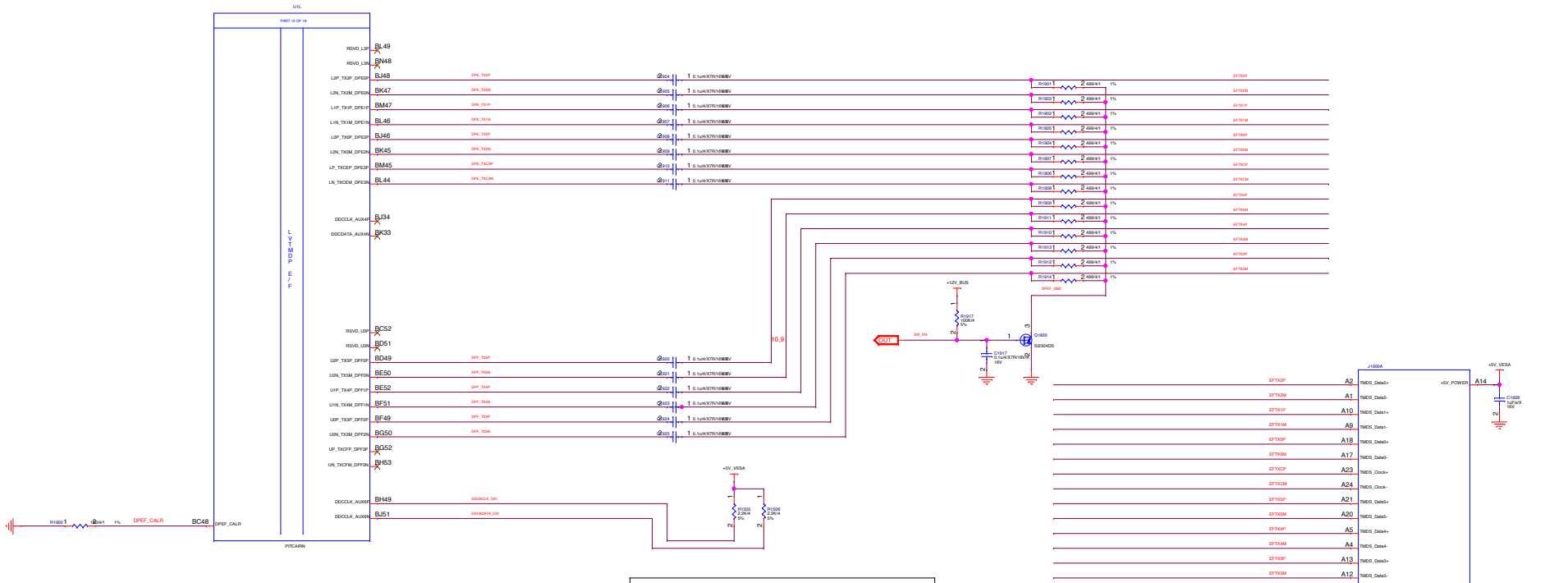


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SHEET NUMBER: 10 OF 26		TITLE:		<TITLE>	
DOCUMENT NUMBER: GV-F827XOC-200					

(11) CURACAO LVTMDPEF dDVI

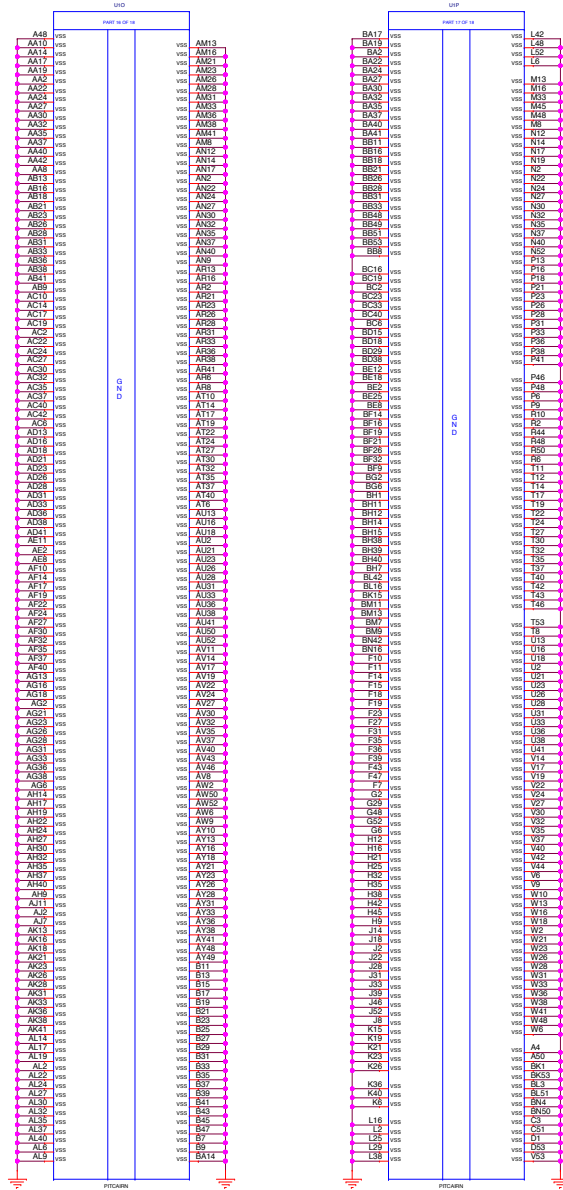


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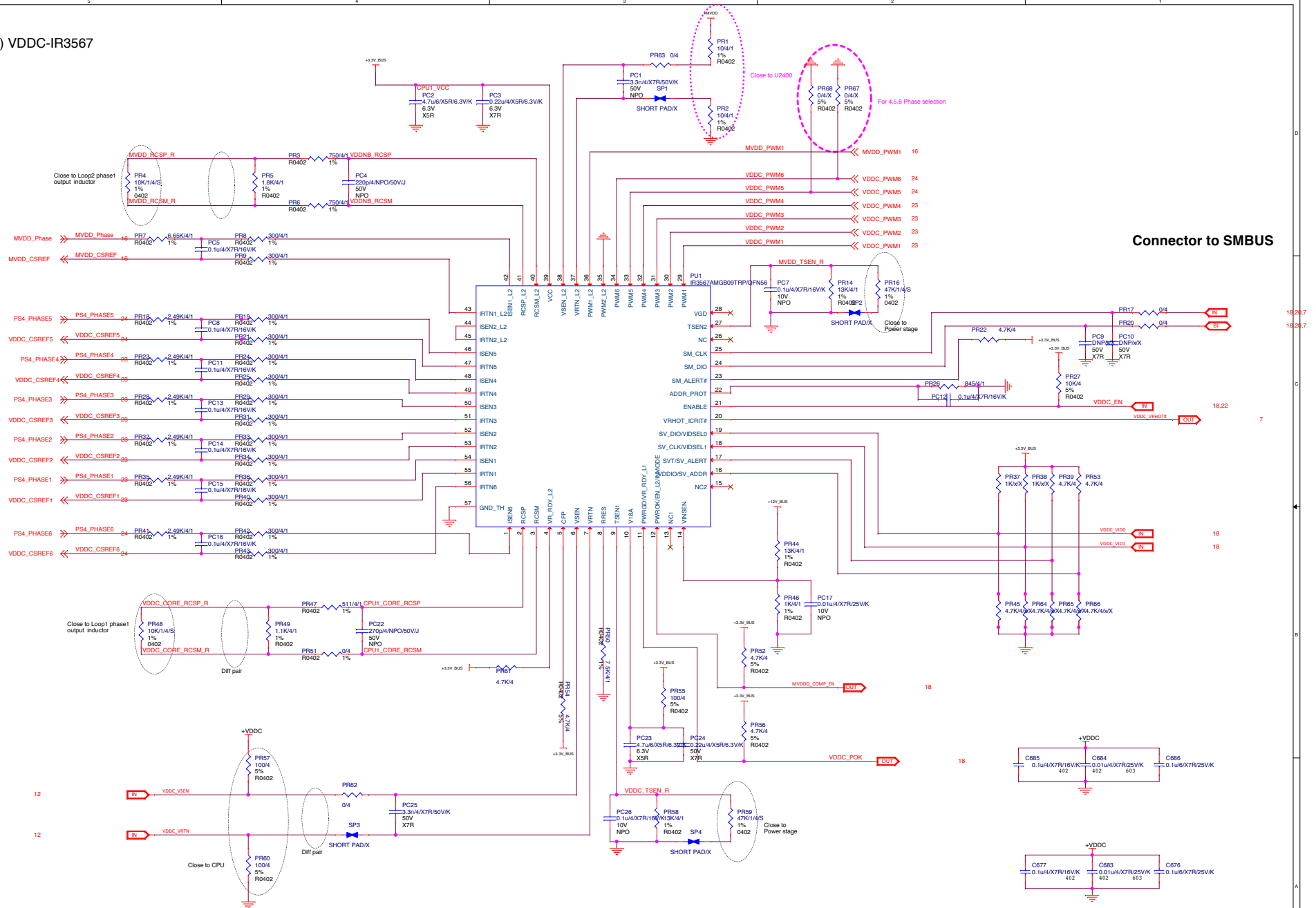
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<p>SHEET: CUMULATIVE POWER</p>		<p>DATE: Wed Jul 17 02:26:14 2013</p>		<p>REV: 1.0</p>	
<p>SHEET NUMBER: 12 OF 26</p>		<p>FILE: 1.0</p>		<p>INTERNAL</p>	
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(13) CURACAO GND

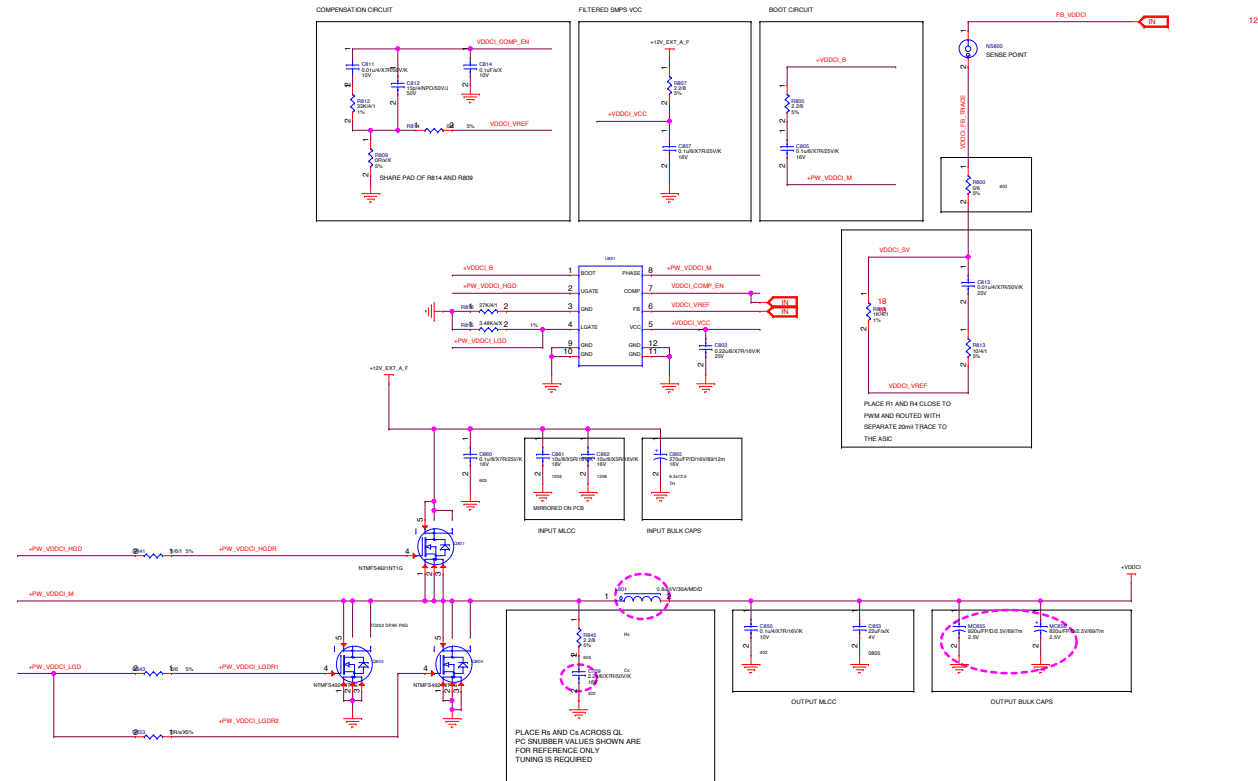


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SHEET NUMBER: 13 OF 26			DOCUMENT NUMBER: GV-R827XOC-2GD	

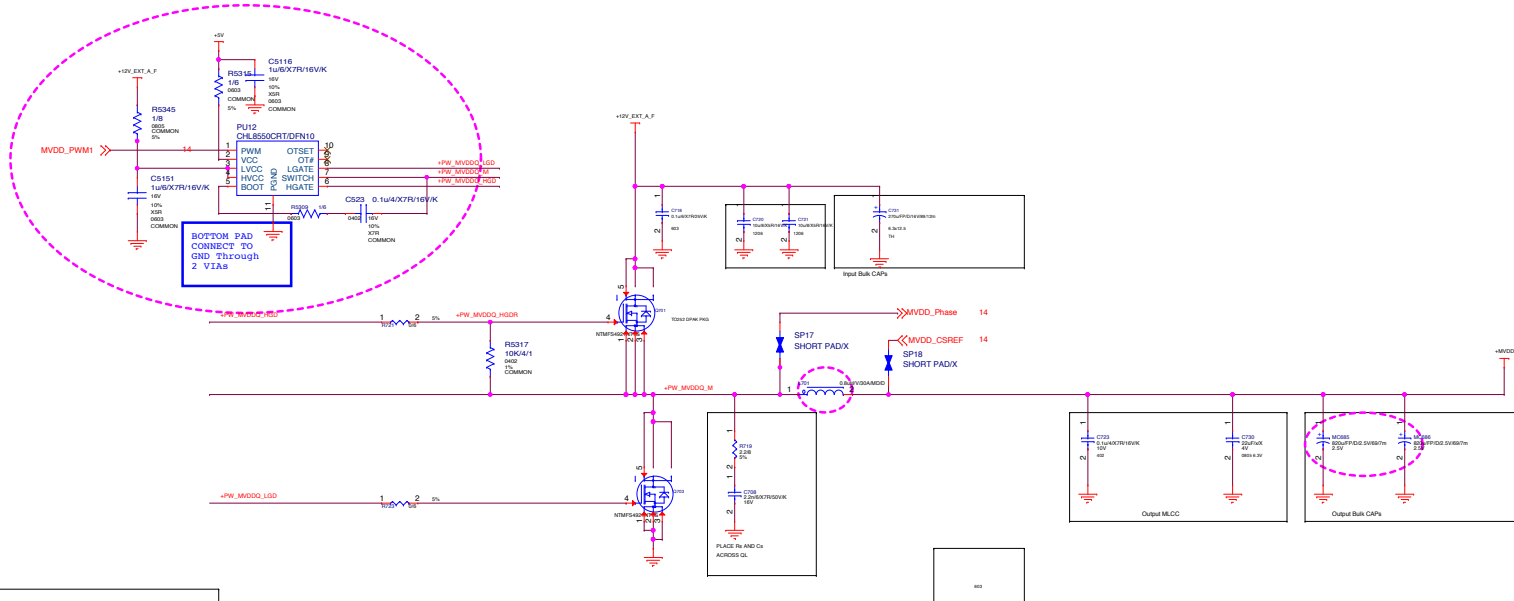
(14) VDDC-IR3567



(15) VDDCI



(16) MVDD



LAYOUT GUIDELINE

1. POSITION THE CONTROLLER (C702) SUCH THAT LGATE (P146) IS THE CLOSEST TO THE GATE OF THE MOSFETS. YOU CAN PLACE THE GATE RESISTORS R721 AND R722 NEXT TO THE GATE OF THE MOSFETS. MAKE THE GATE DRIVE TRACES (PW_MVDDQ_LGDMSQ) AS SHORT AS POSSIBLE TO REDUCE THE TRACE INDUCTANCE.
2. PLACE THE BYPASS CAPACITORS FOR VCC (C703) AS WELL AS BOOST CAPS (C705) AS CLOSE TO THE CONTROLLER AS POSSIBLE.
3. VOLTAGE AMPLIFIER COMPENSATION NETWORK: PLACE R714 CLOSE TO THE PIN 7.
4. PLACE THE REST OF THE COMPENSATION NETWORK (R716, R711, R712, R713, C711, C712 AND C713) CLOSE TO THE PINS 7 AND 8.

PLACE R1 AND R4
CLOSE TO PWM AND
ROUTE WITH
SEPARATE 20mil TRACE
RETURN LINE

COMPENSATION CIRCUIT

FILTERED SMPS VCC

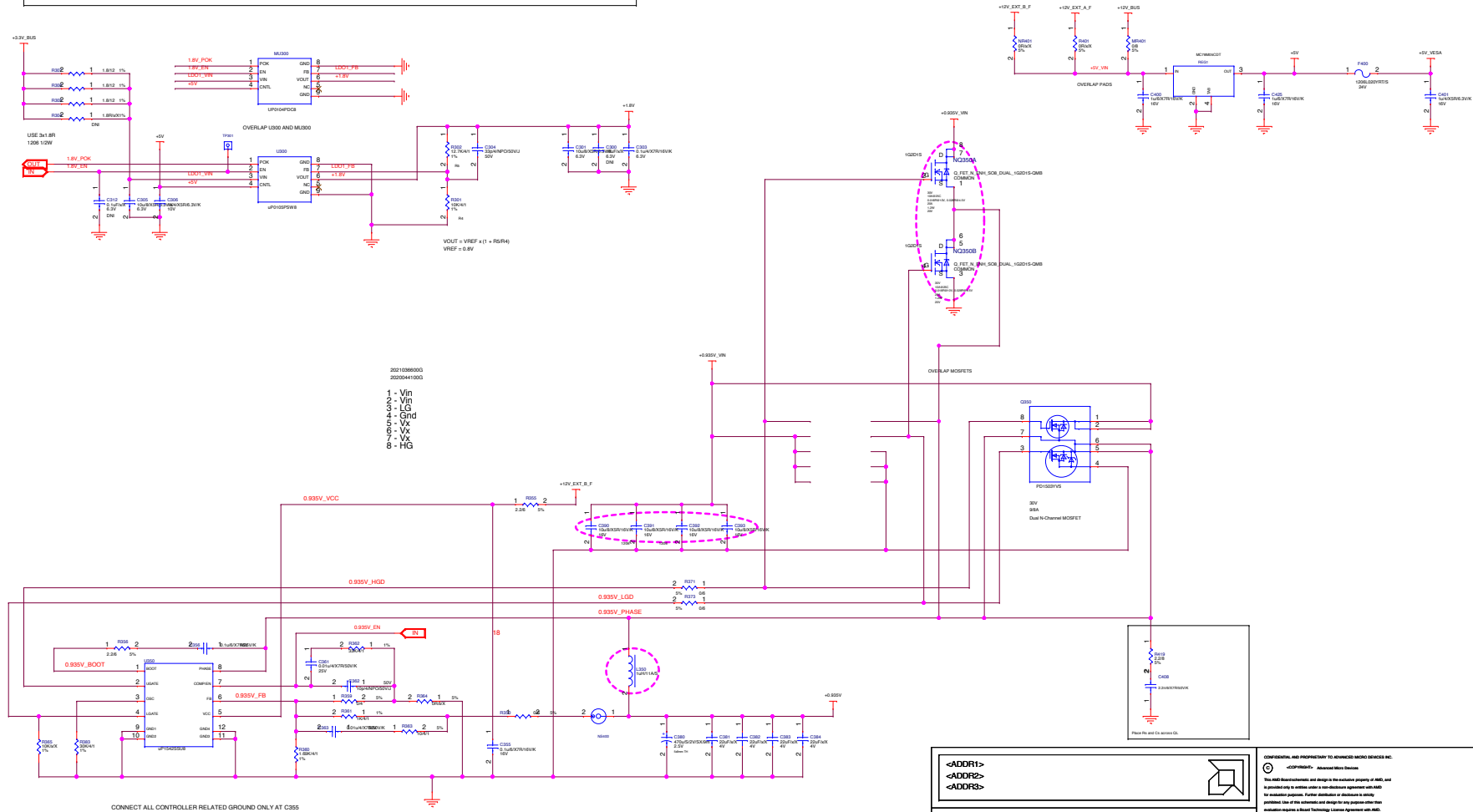
BOOT CIRCUIT

share pad of R371-4, R3702

(17) SMALL RAIL REGULATOR

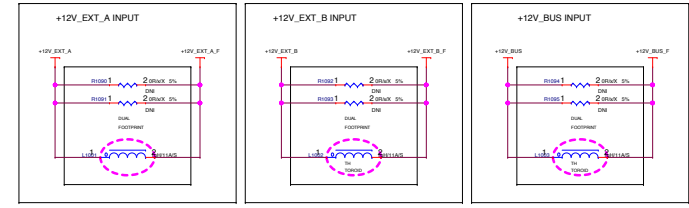
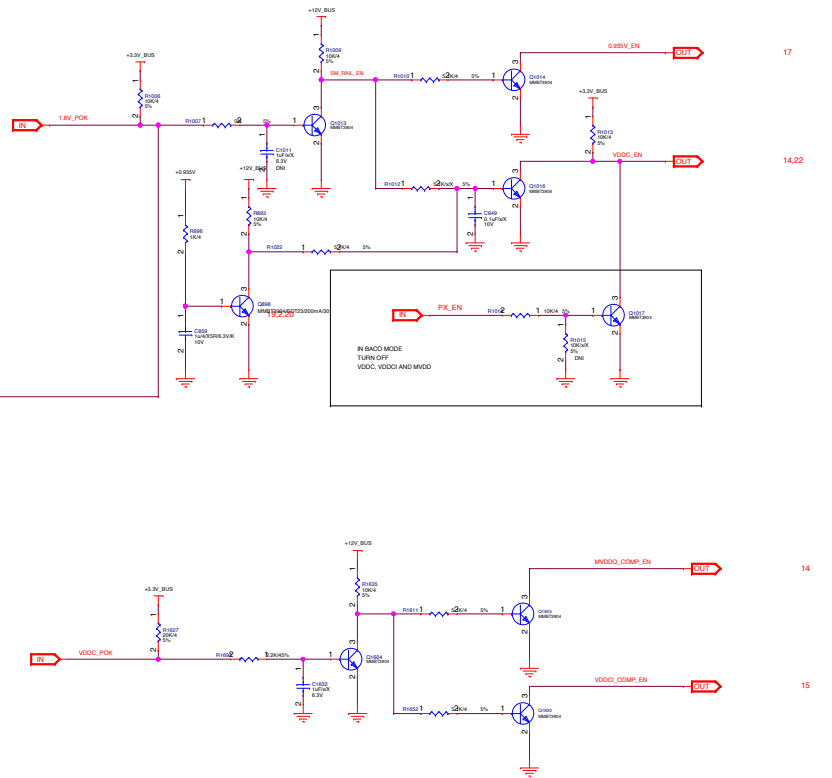
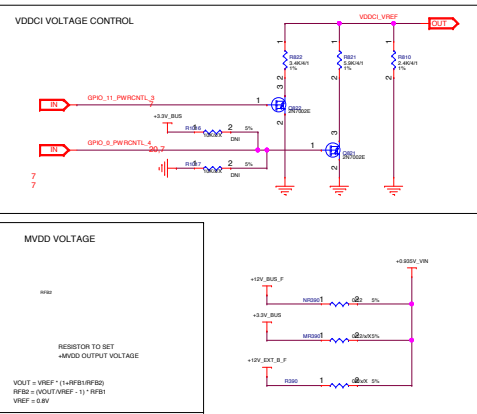
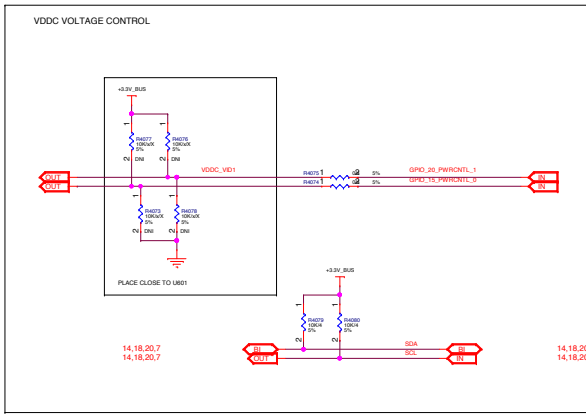
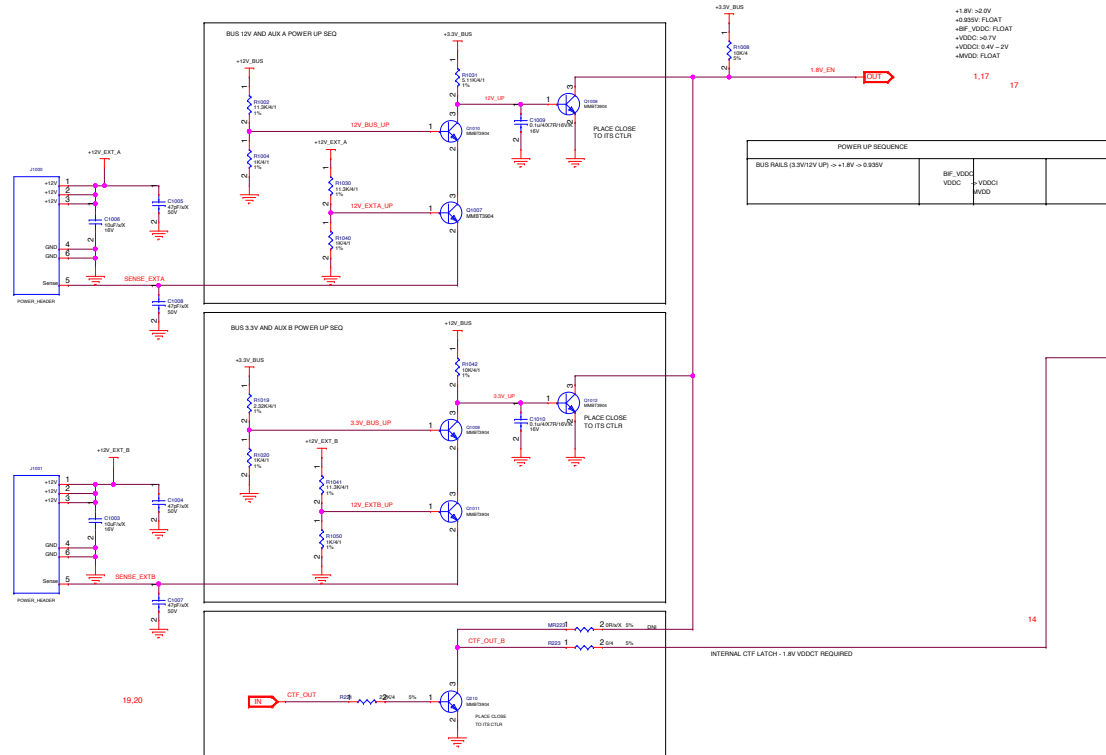
LDO #1: $V_{IN} = 3.0V \text{ TO } 3.6V \text{ MAX}$ $V_{OUT} = +1.8V \pm 2\%$ $I_{OUT} = 1.3A \text{ RMS MAX}$
PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING

REGULATOR FOR +5V RAILS
 $I_{OUT \text{ MAX}} = 150mA$



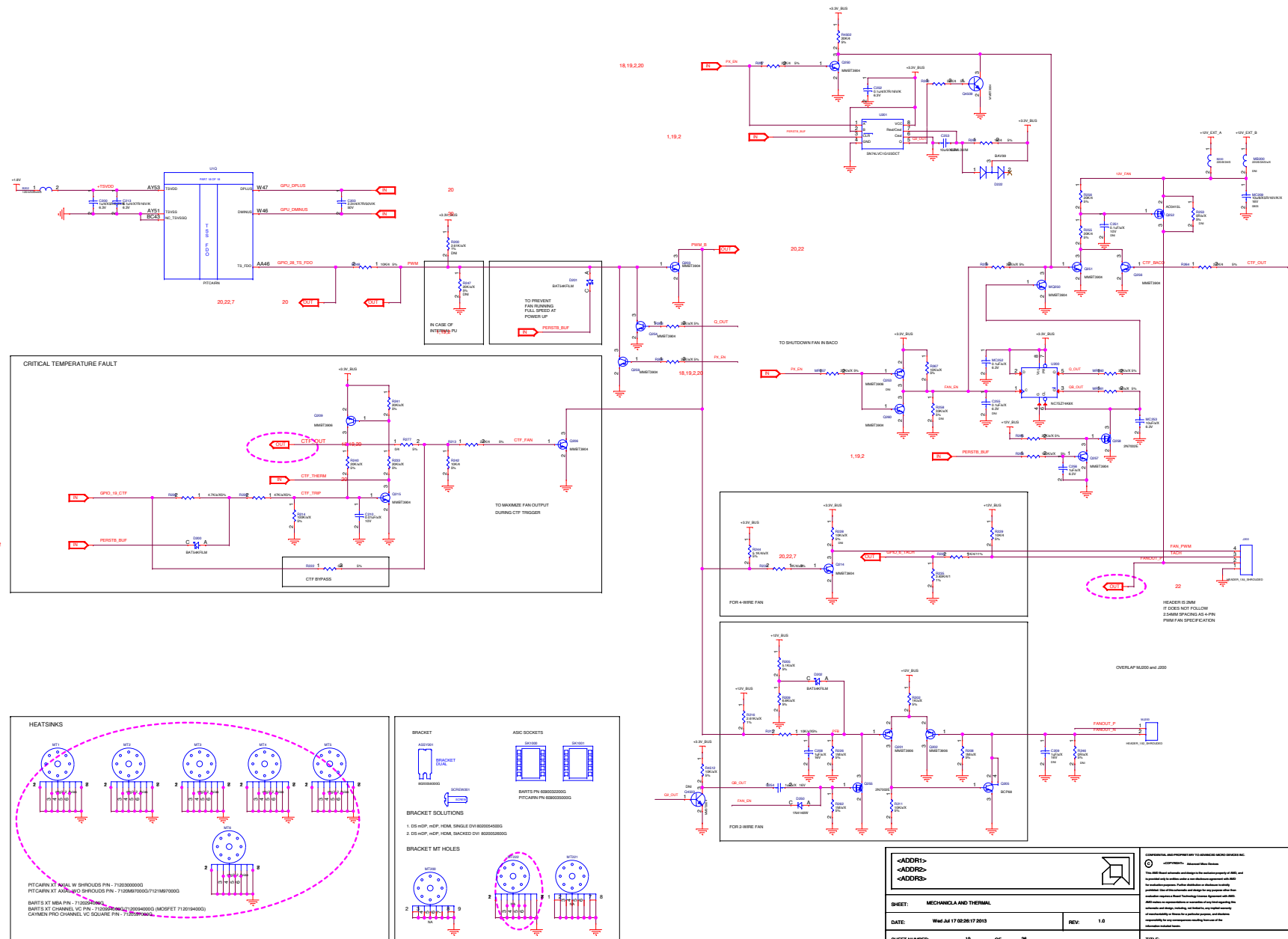
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DATE: Wed Jul 17 02:26:16 2013		SHEET NUMBER: 17 OF 28	
DOCUMENT NUMBER: GV-R027XOC-RGD		TITLE: <TITLE>	

(18) POWER MANAGEMENT

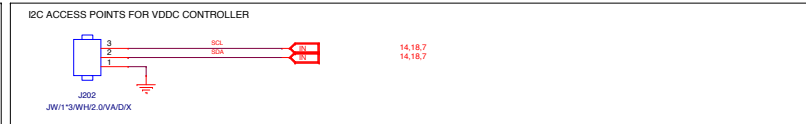
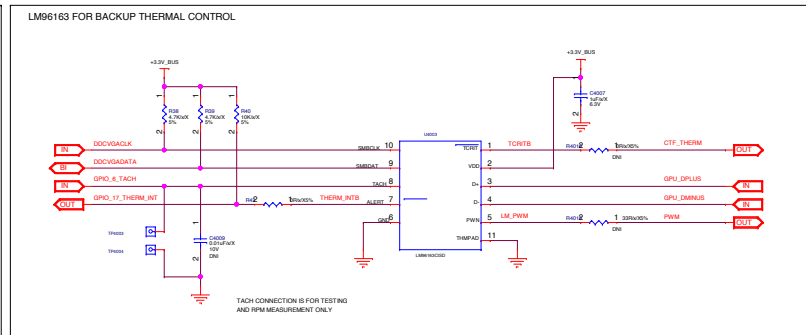
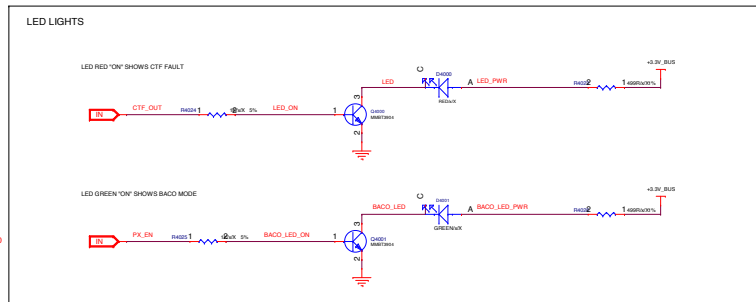
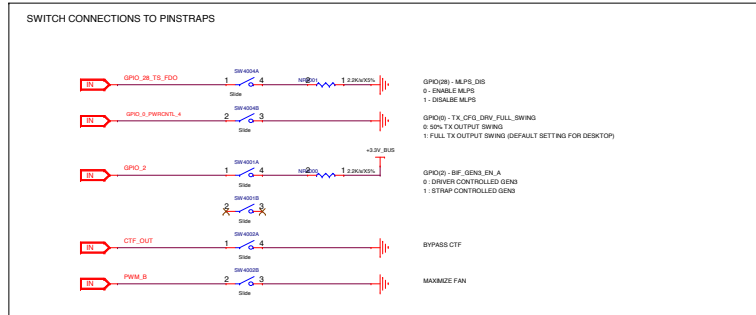
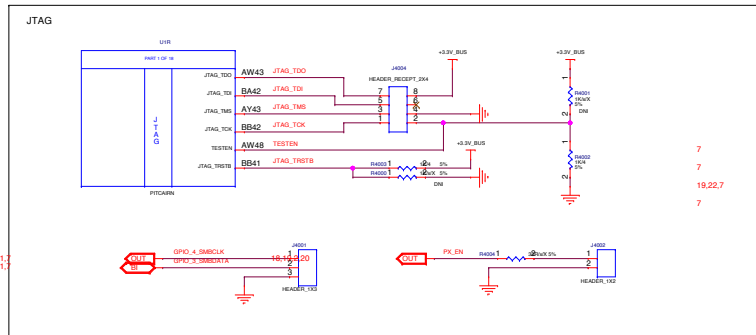




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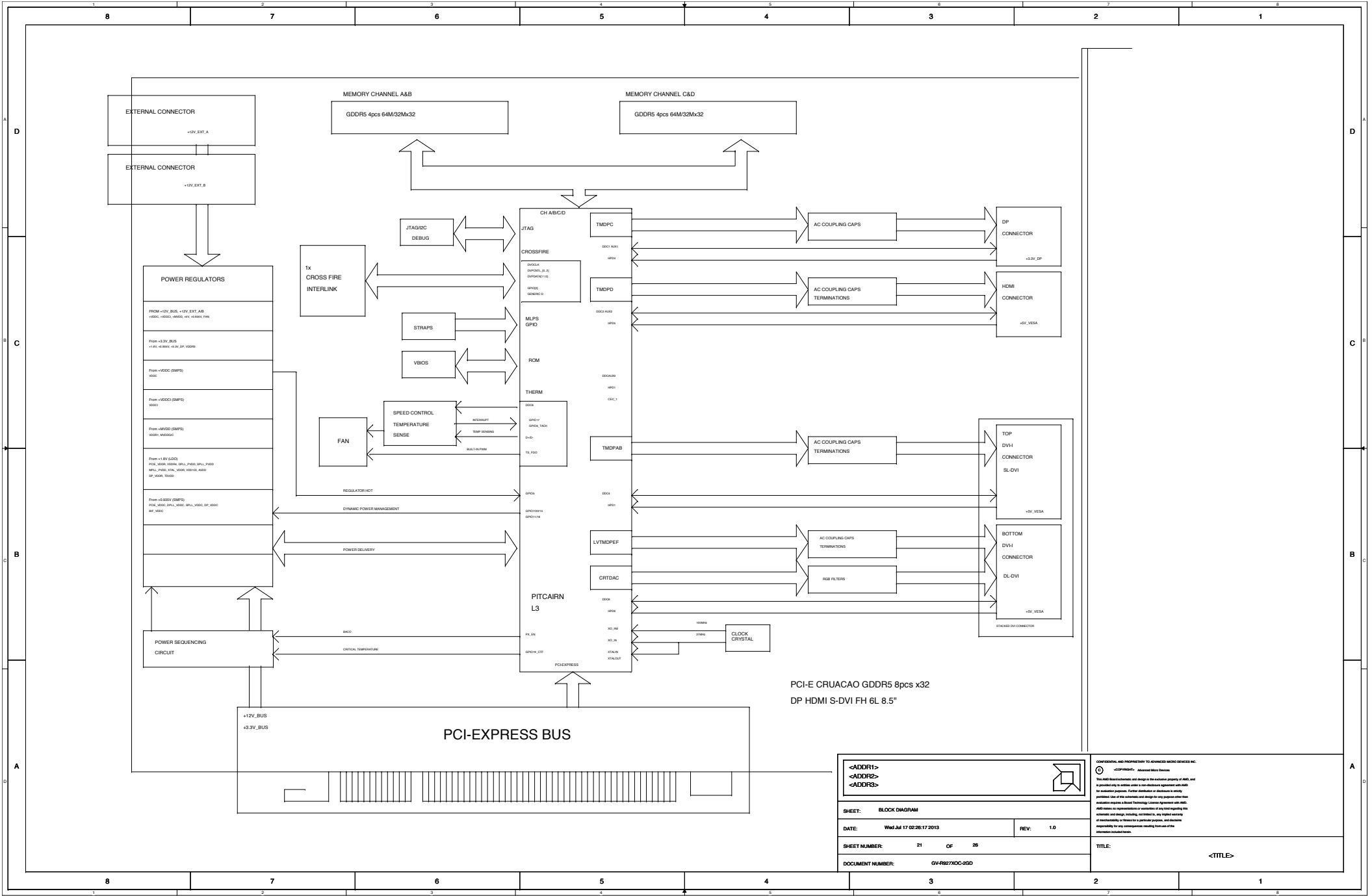
(19) MECH AND THERM MANAGEMENT

[illegible]

(20) DEBUG CIRCUIT



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SHEET: DESIGN CONCEPT		<div style="border: 1px solid black; padding: 5px;"> <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;">  <CONFIDENTIAL> Advanced Micro Devices </div> <div> <p>The AMD Secretariat and its divisions are the exclusive property of AMD, and is provided only to certain other individuals approved and used for essential purposes. Further distribution or disclosure is strictly prohibited. Any data contained and design for any system other than those contained in a Secret Technology Information Agreement will not be made in reproduction or execution of any other existing design, information and, similarly, not used in any other manner or for any other purpose, and is not to be disclosed, in whole or in part, to any other person, firm, company, or organization, without the express written consent of AMD.</p> </div> </div> </div>	
DATE: Wed Jan 17 02:26:17 2013		REV: 1.0	
SHEET NUMBER: 20 OF 26		TITLE:	
DOCUMENT NUMBER: GV-R82700-26D		<TITLE>	



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SHEET: BLOCK DIAGRAM

DATE: Wed Jul 17 02:26:17 2013

SHEET NUMBER: 21 OF 26

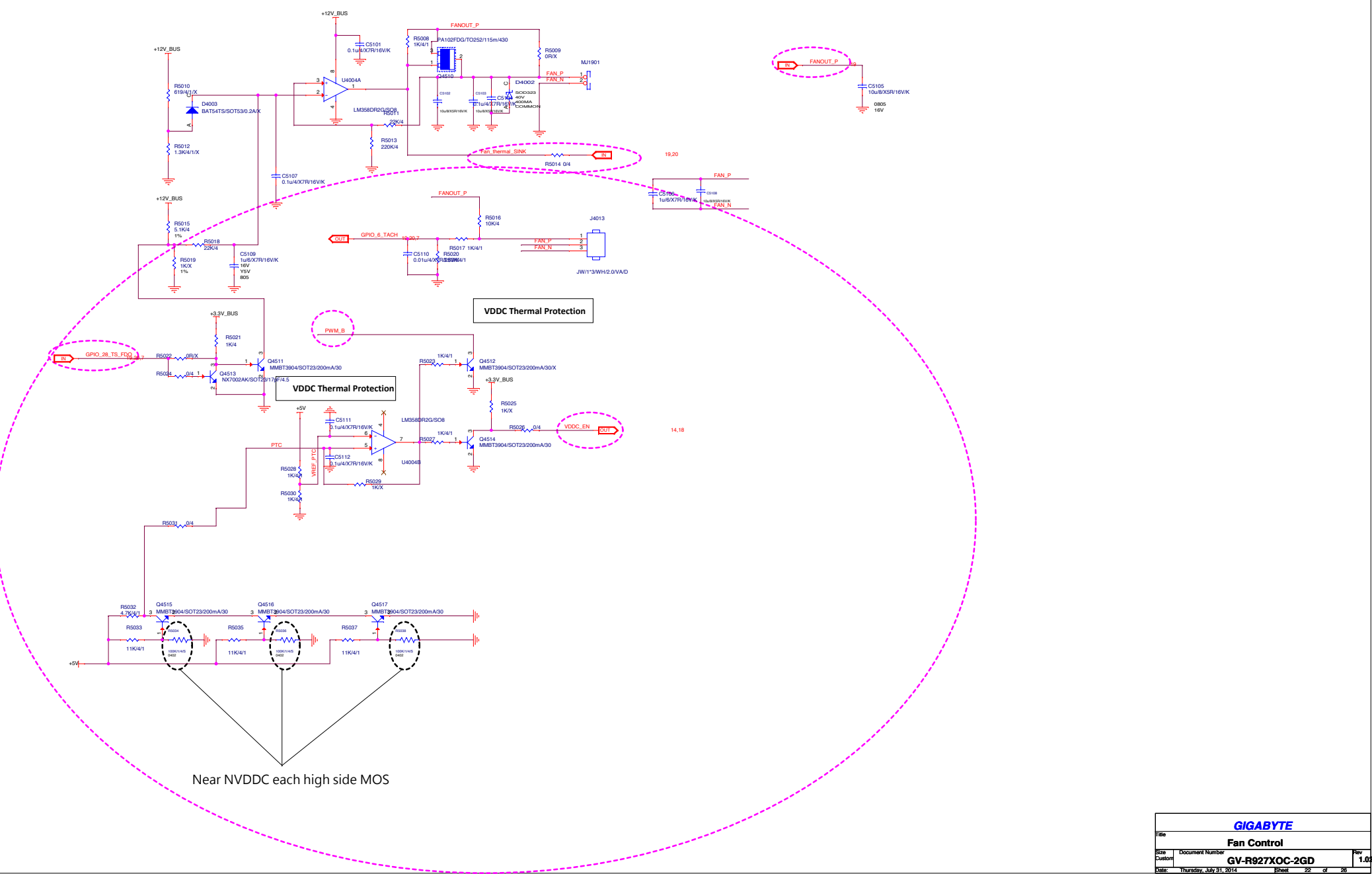
DOCUMENT NUMBER: GV-R827XOC-2GD

REV: 1.0

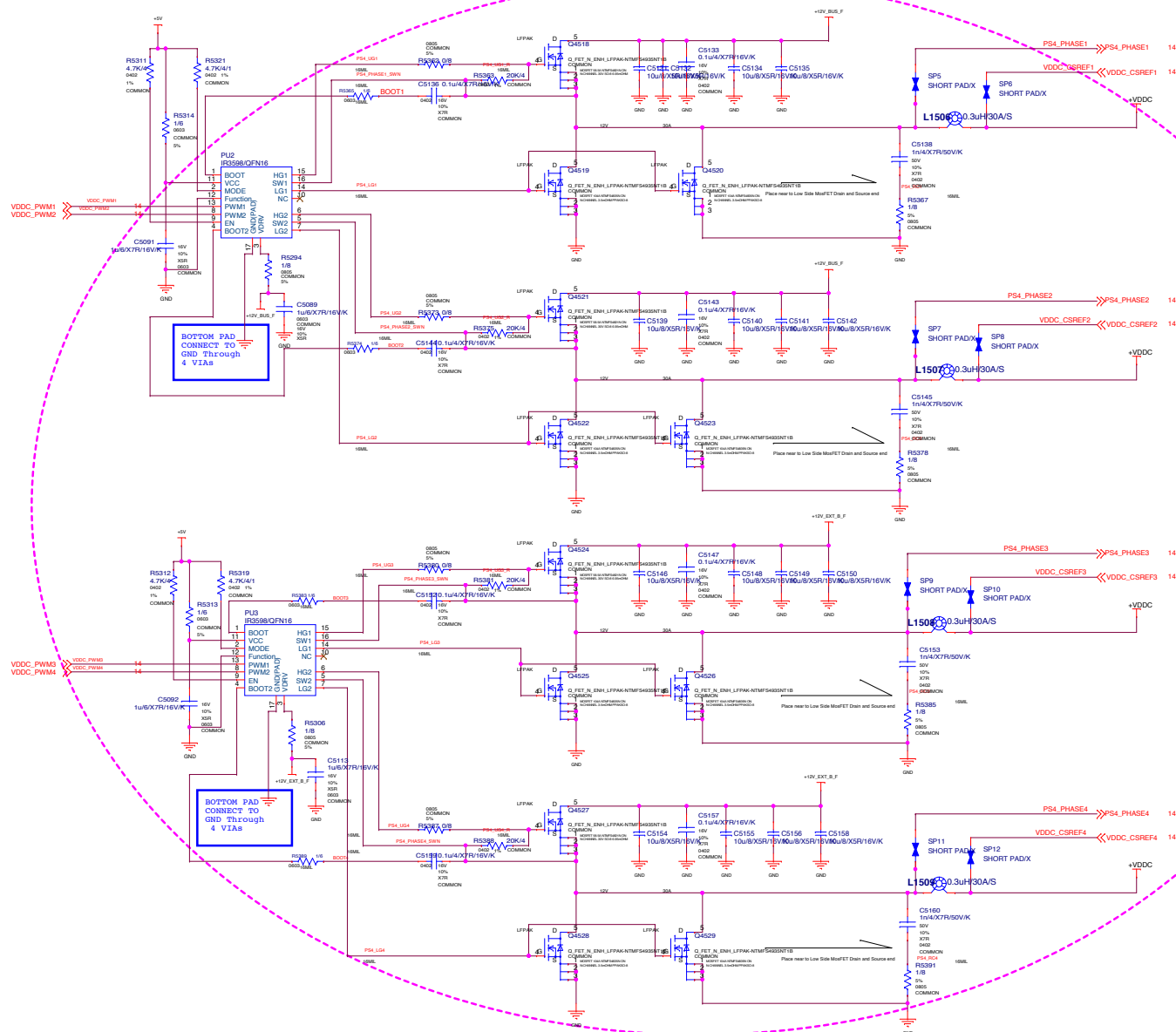
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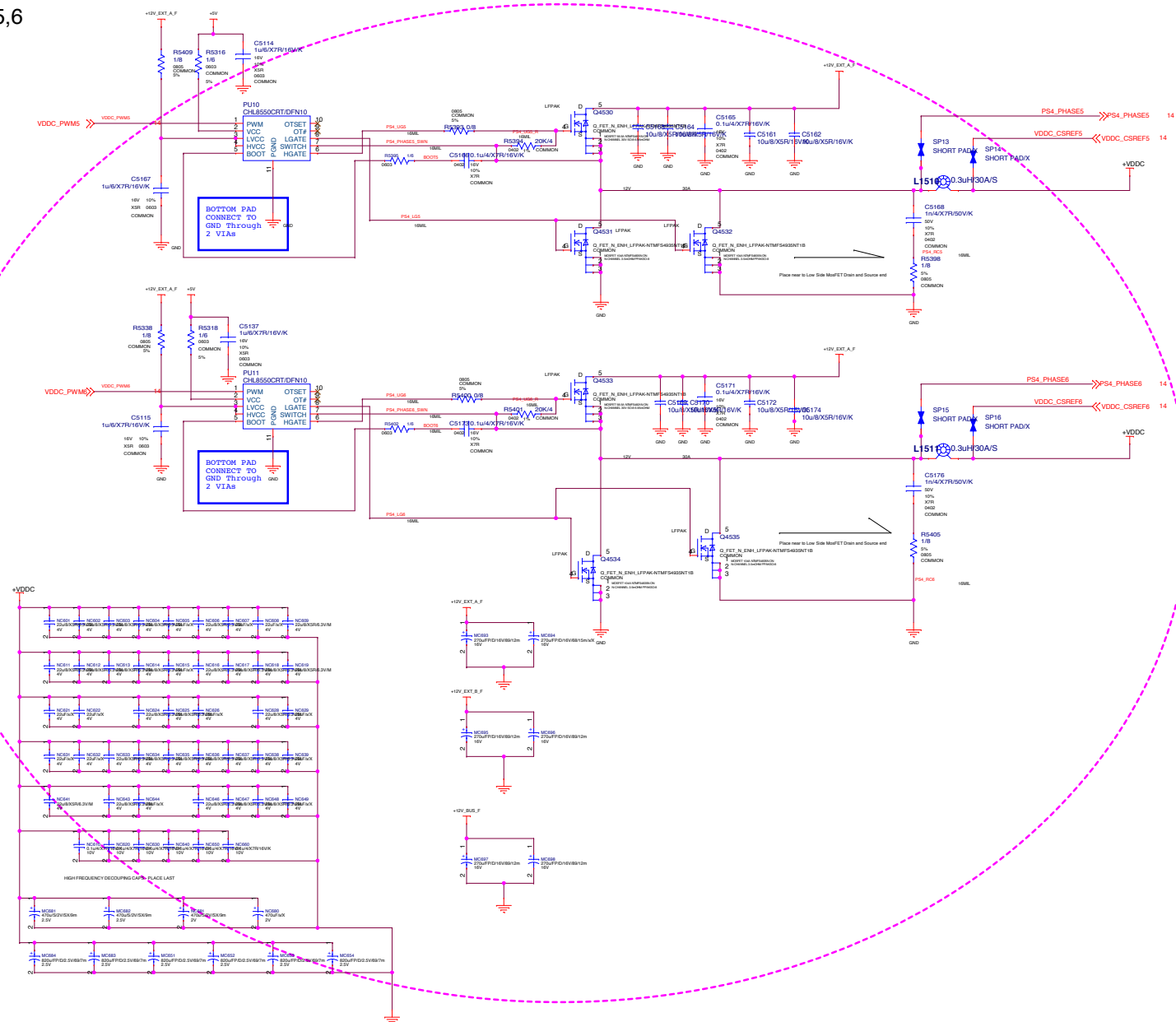
(22) 3 Pin Fan Control



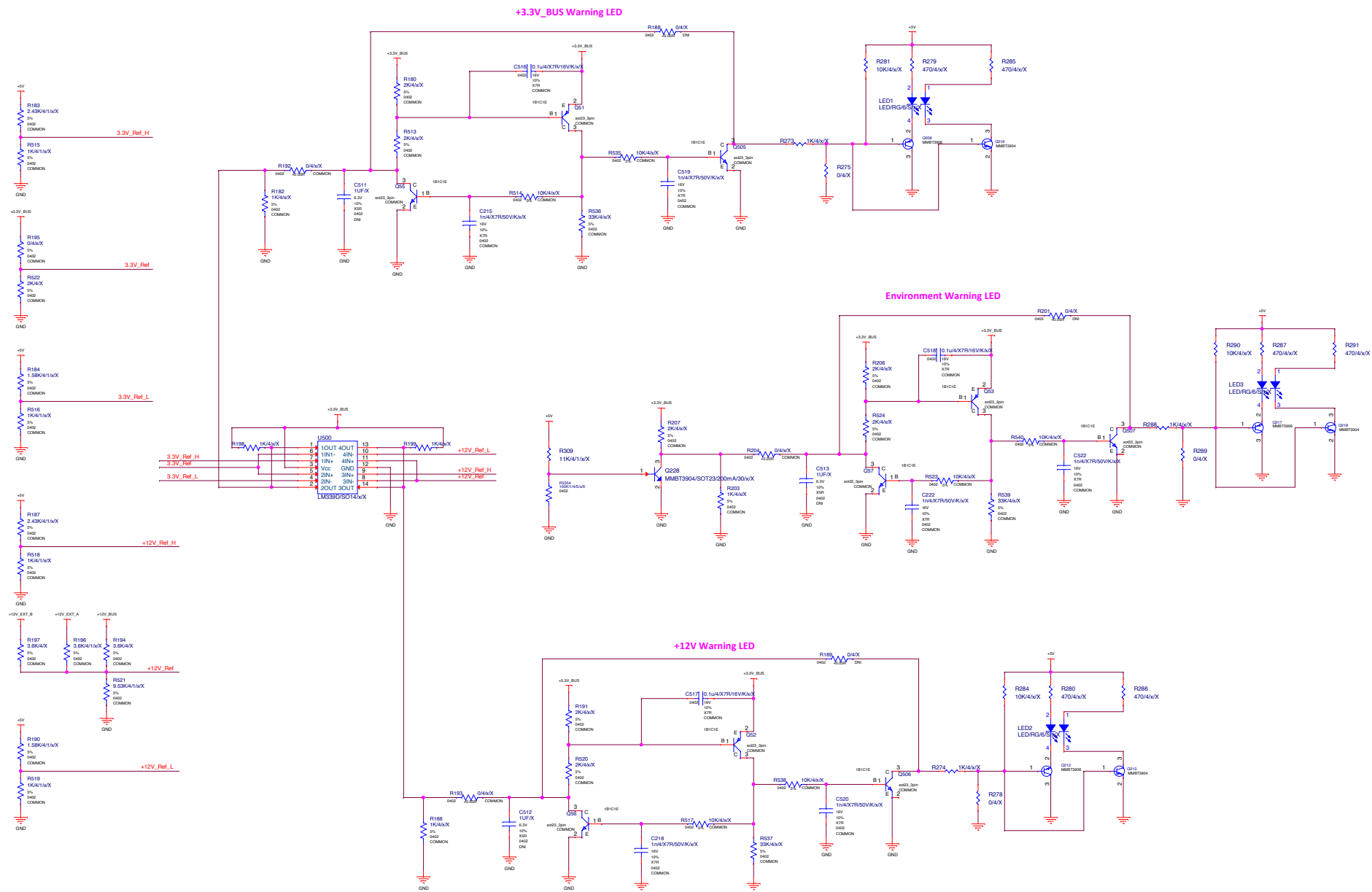
(23) VDDC Phase 1,2,3,4



(24) VDDC Phase 5,6



(25) Warning LED



AMD

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Wed Jul 17 02:26:17 2013

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23

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ENGINEER:

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NOTES:

NOTE

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<ADDR1>
<ADDR2>
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REVISION HISTORY

SCH Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/25/2013	INITIAL GIGABYTE/ASIC BASED ON CARD
1	00B	06/25/2013	ADD POWER CON. CHG
1	00C	06/25/2013	RENAME L1700 - L1730 RENAME RE pin for GP_VDDPWR_VDDC
00D	000001		update power sequence to make 0.05V power up before vddc

GIGABYTE

REVISION HISTORY

Size	Document Number	Rev
Custpm	GV-R927XOC-2GD	1.02
Date	Thursday, July 31, 2014	Sheet 26 of 26