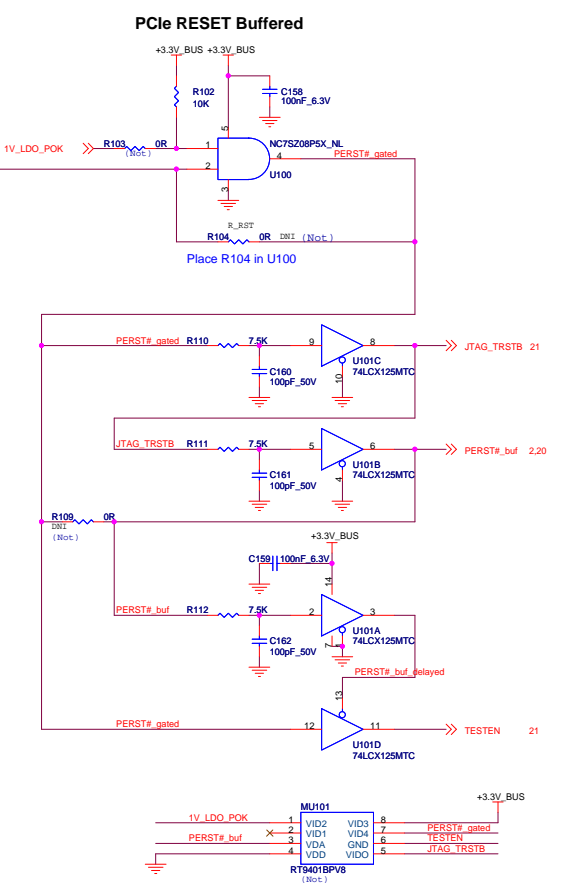
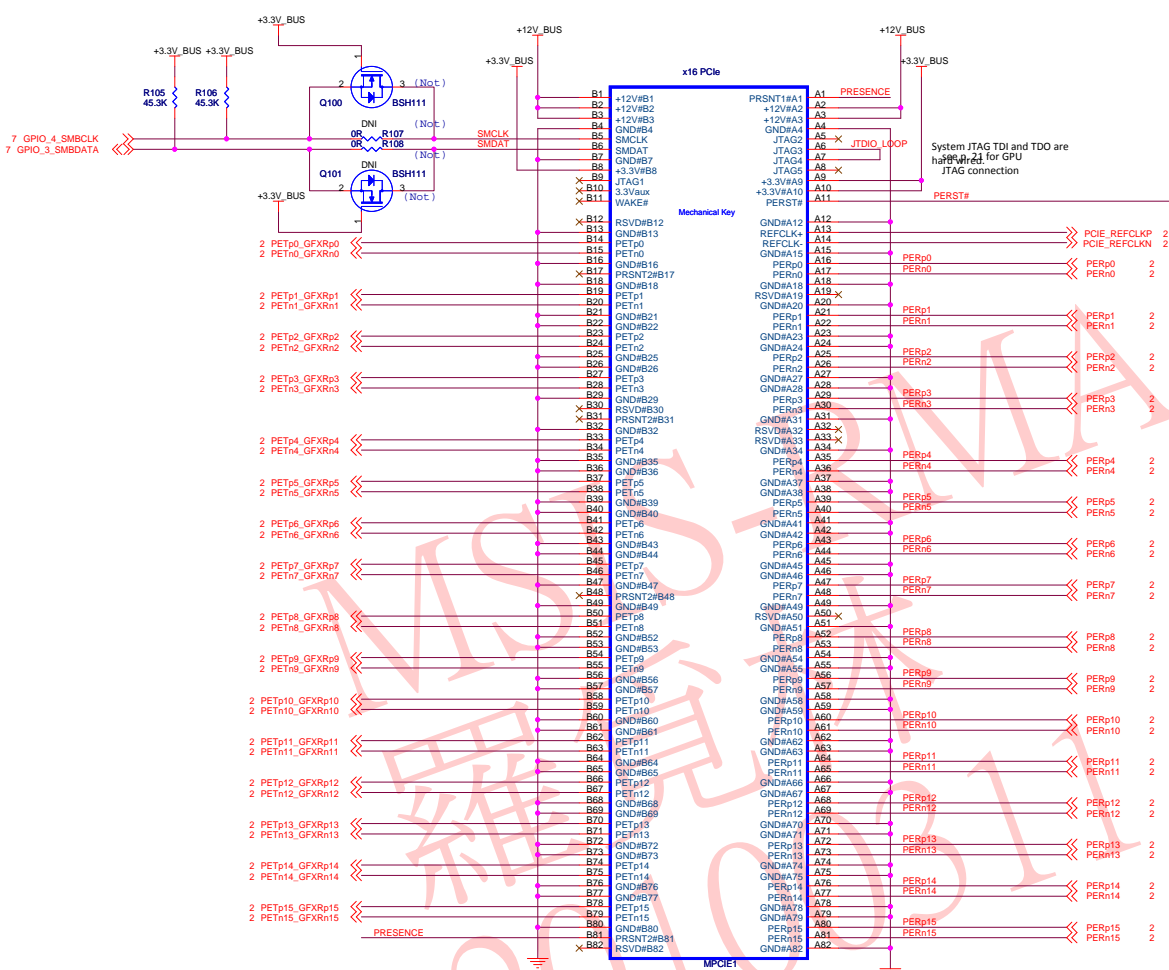
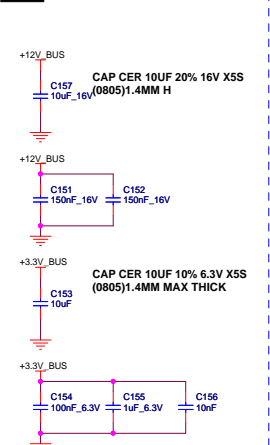


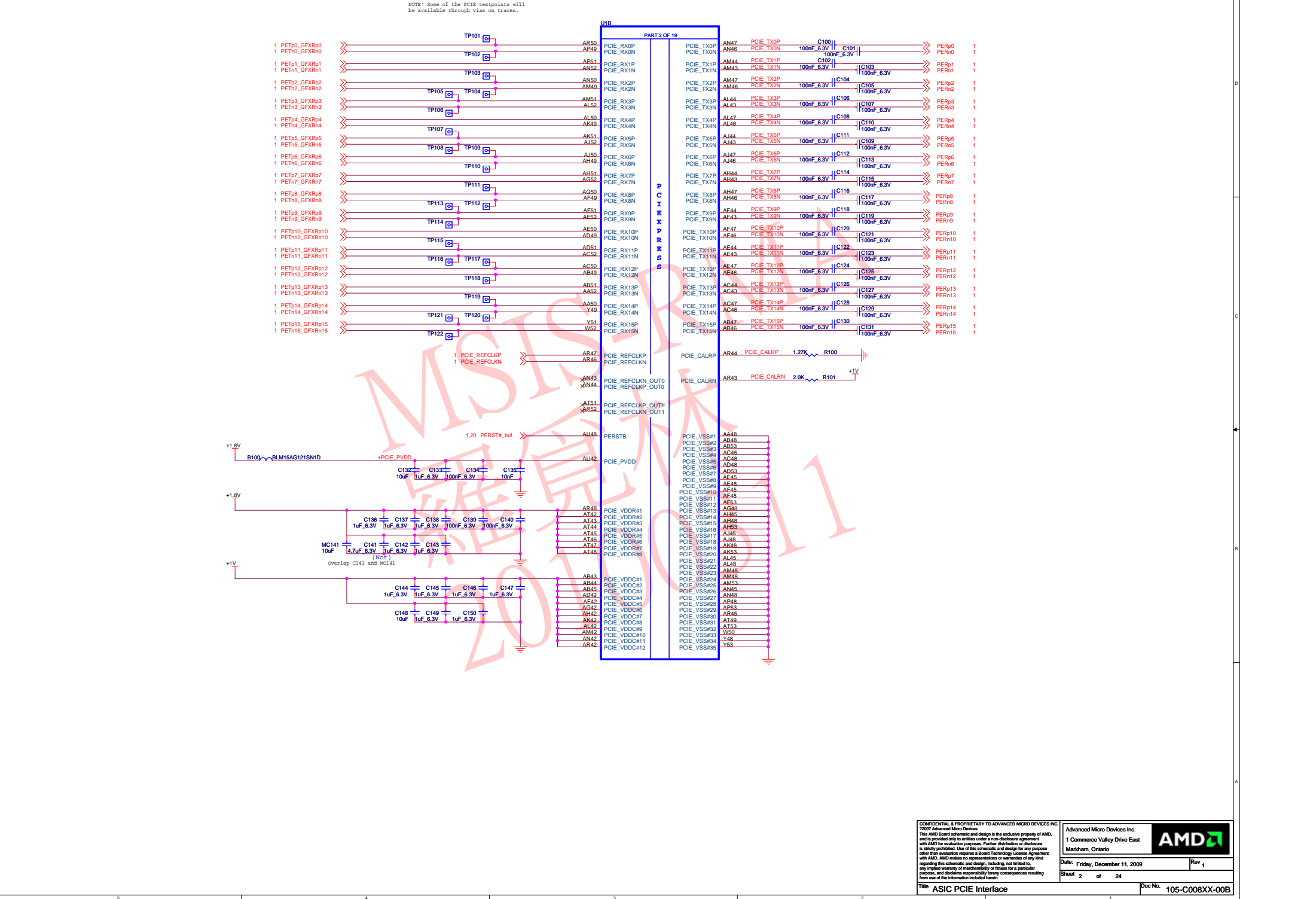
PCI-EXPRESS EDGE CONNECTOR

Place these caps as close to the PCIe connector as possible

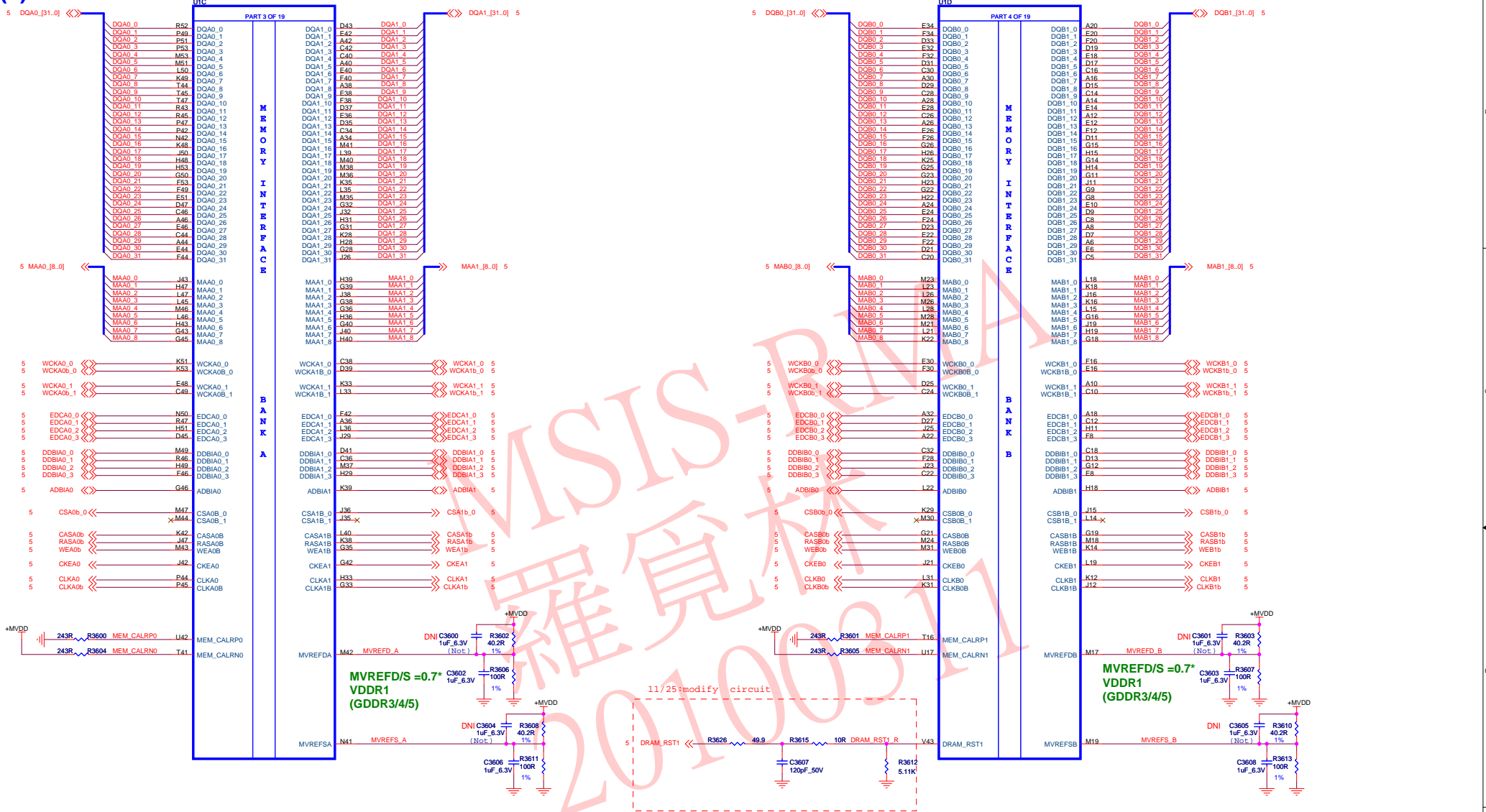


SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
	BRING UP ONLY

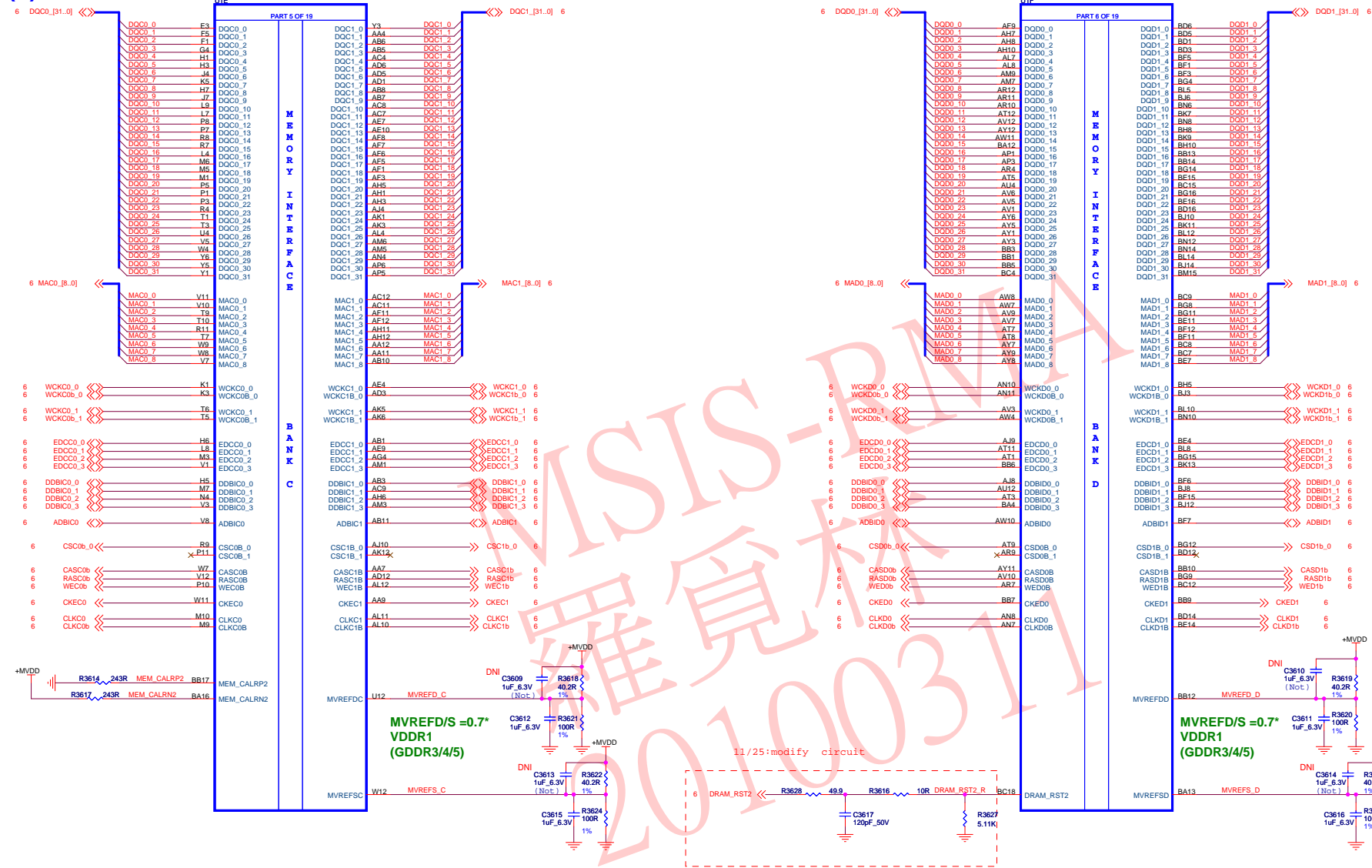
(2) CYPRESS PCIE Interface



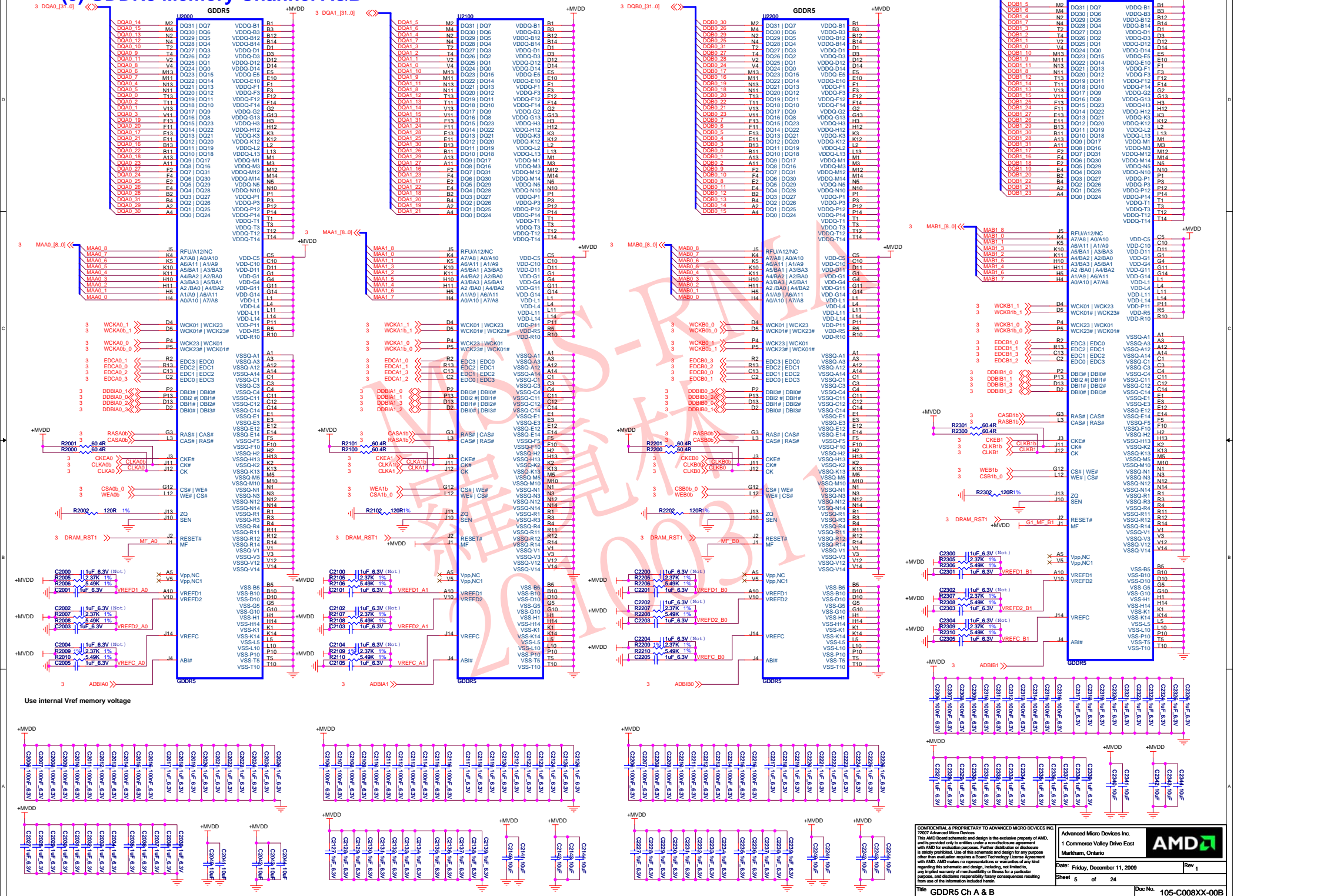
(3) CYPRESS MEM Interface Ch A&B



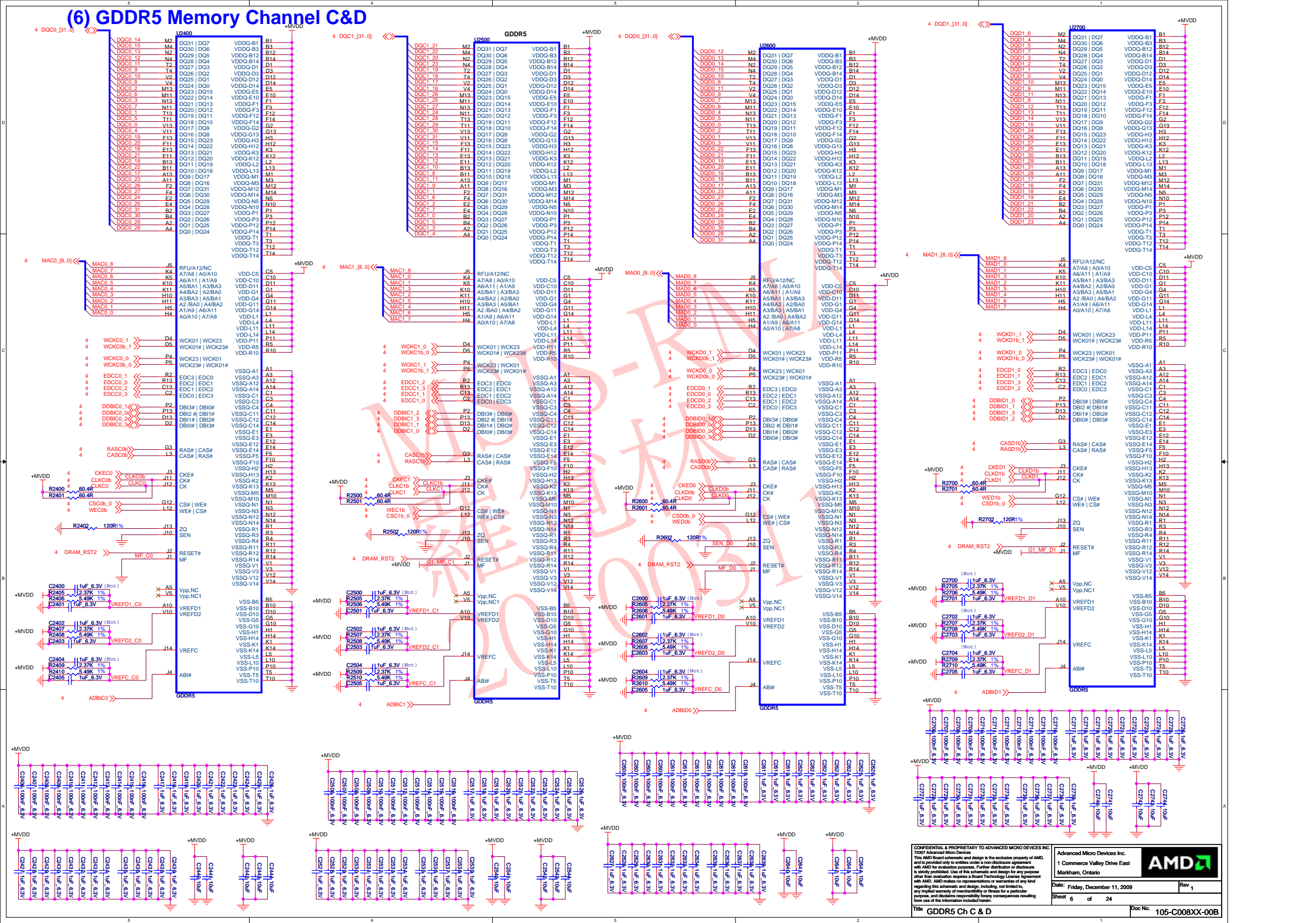
(4) CYPRESS MEM Interface Ch C&D



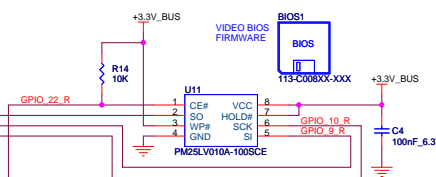
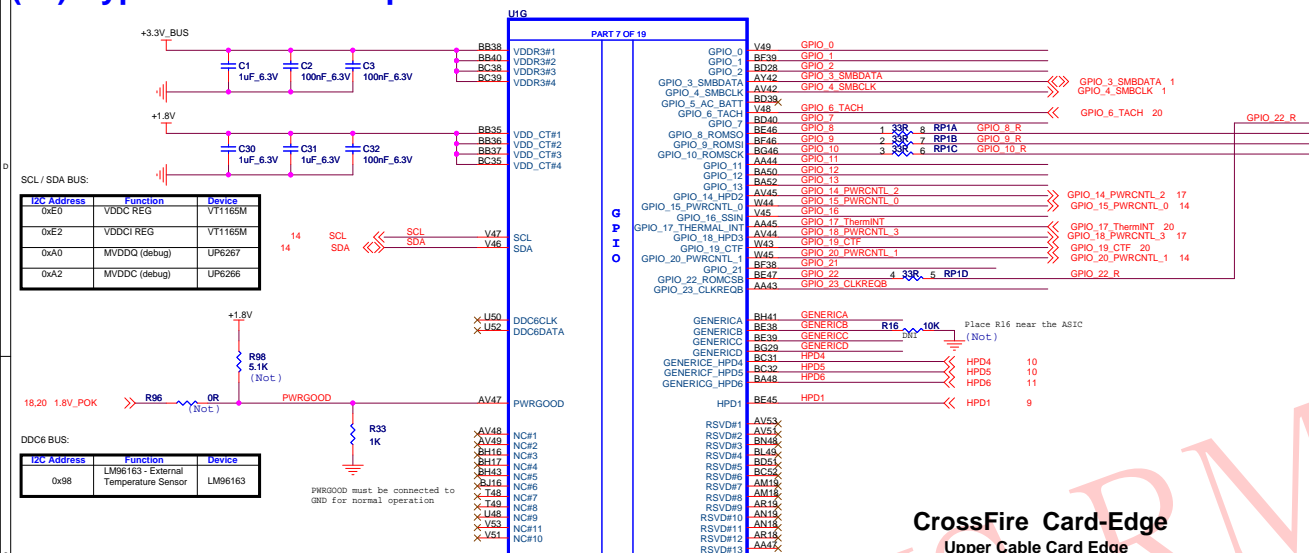
(5) GDDR5 Memory Channel A&B



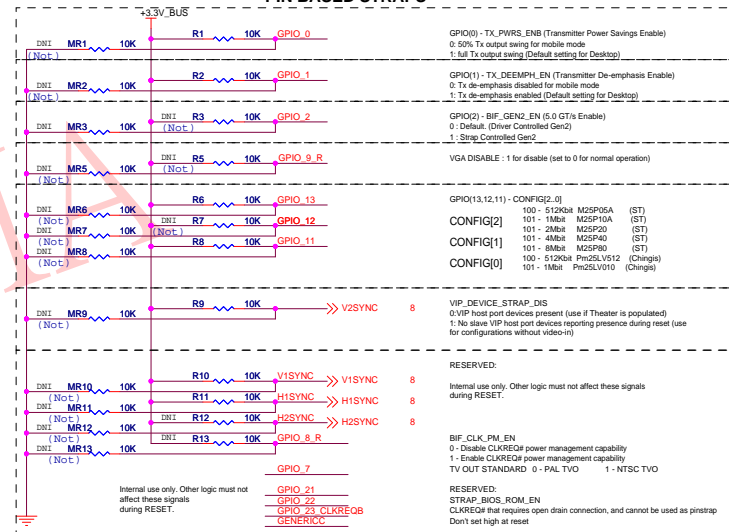
(6) GDDR5 Memory Channel C&D



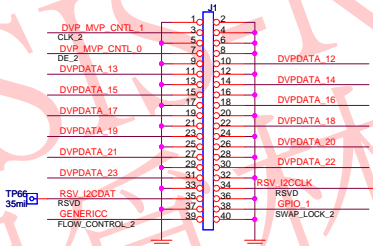
(07) Cypress GPIOs Strap CF XTAL OSC



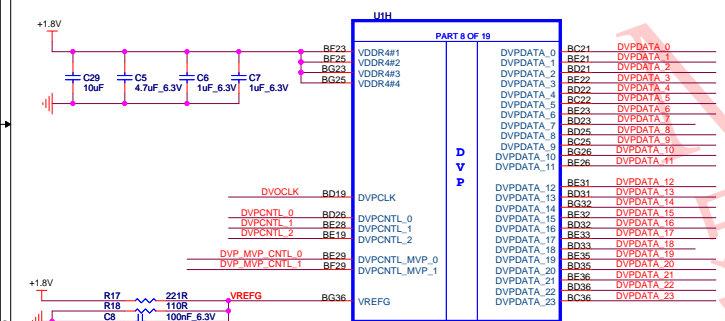
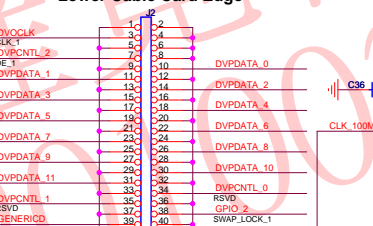
PIN BASED STRAPS



CrossFire Card-Edge



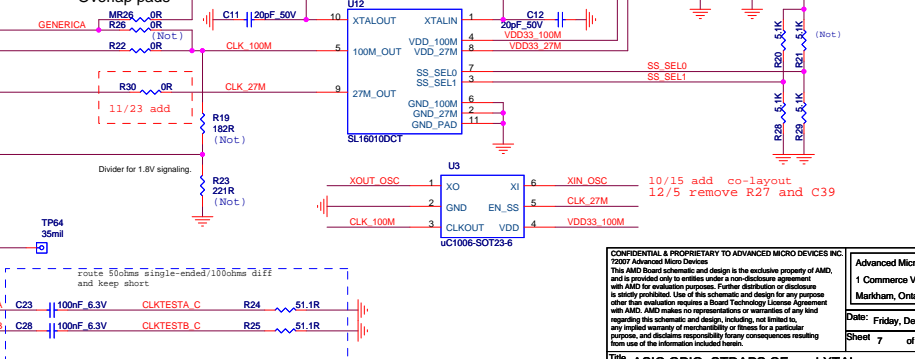
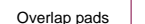
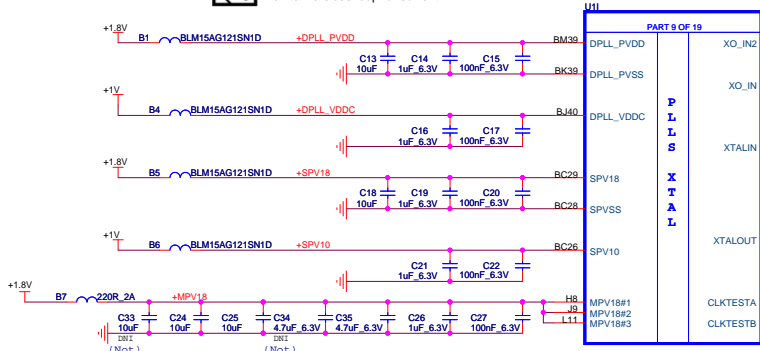
Lower Cable Card Edge



Place the crossfire
testpoints near the ASIC and
not the connector



Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.



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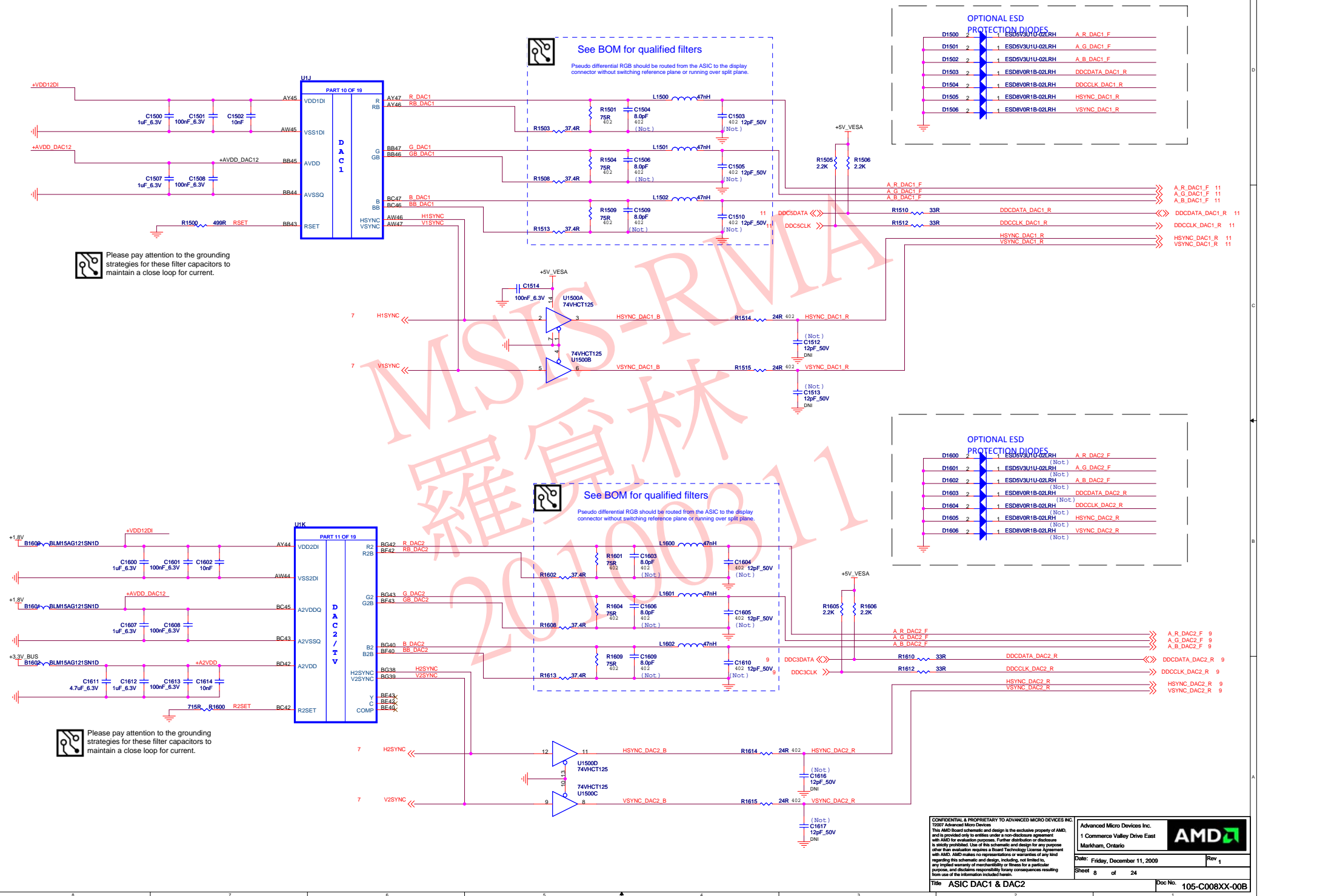
Sheet 7 of 24

Rev	
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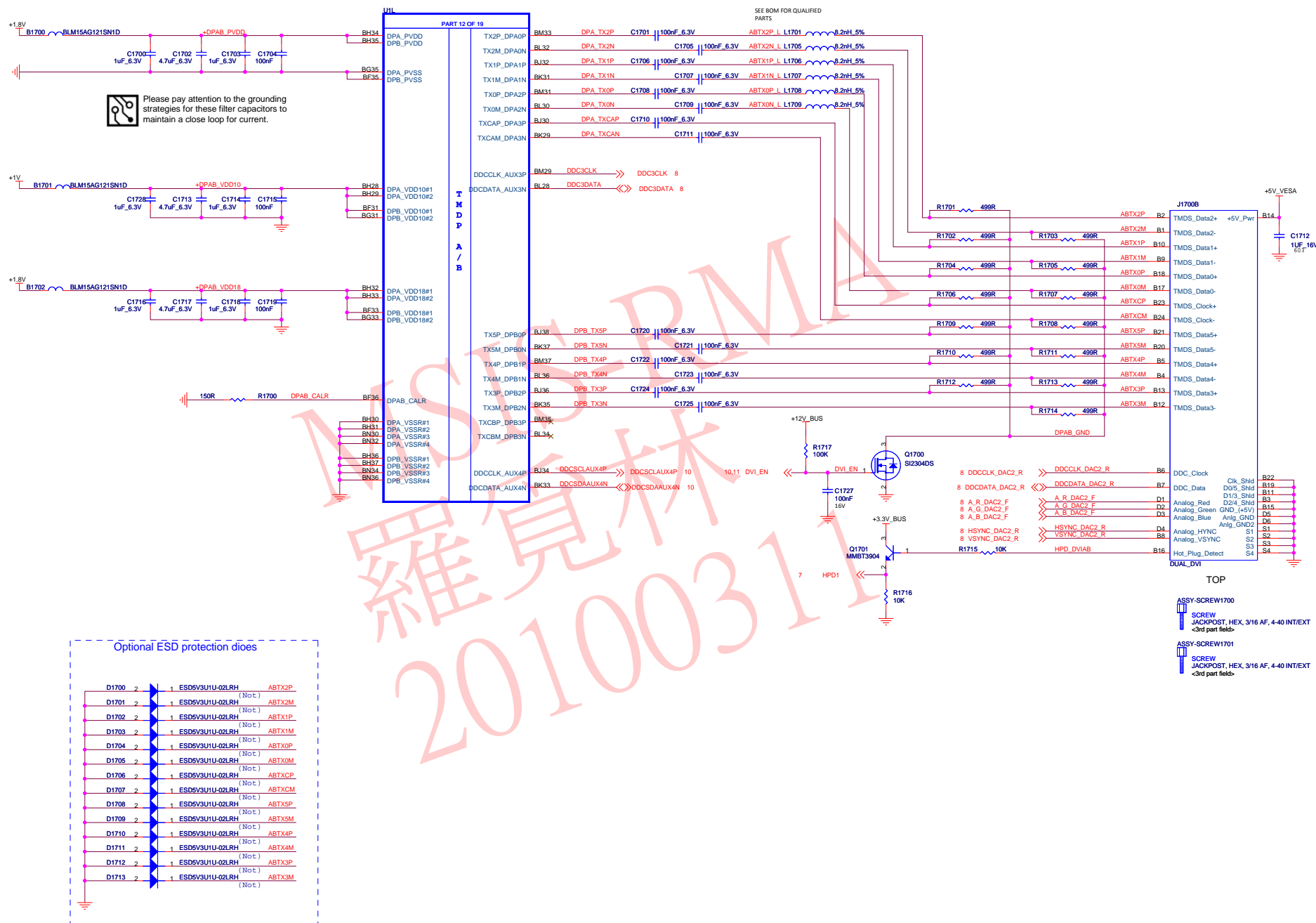
Title ASIC GPIO, STRAPS, CF, and XTAL

Doc No. 105-C008XY-00B

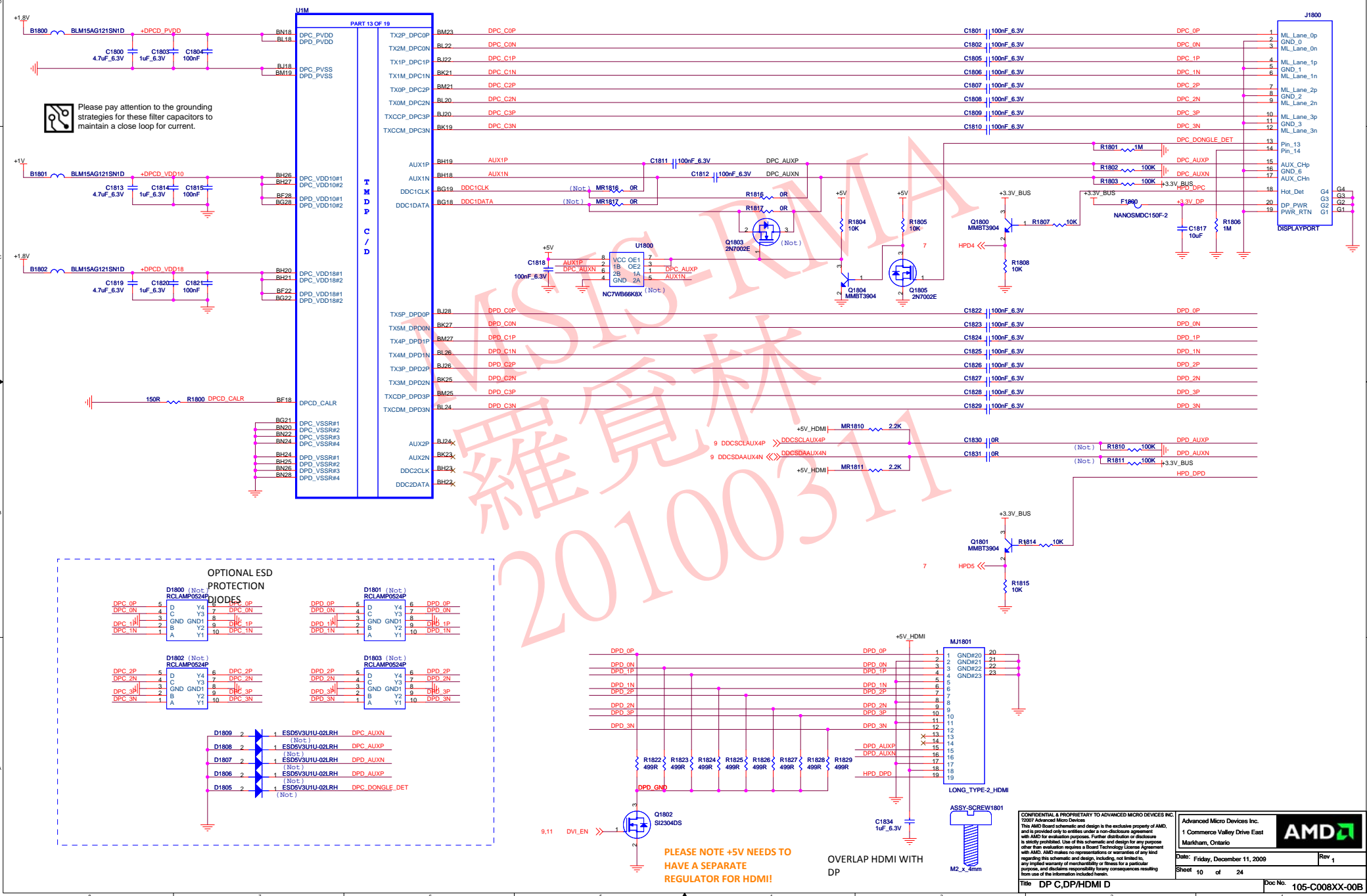
(08) CYPRESS DAC1 and DAC2



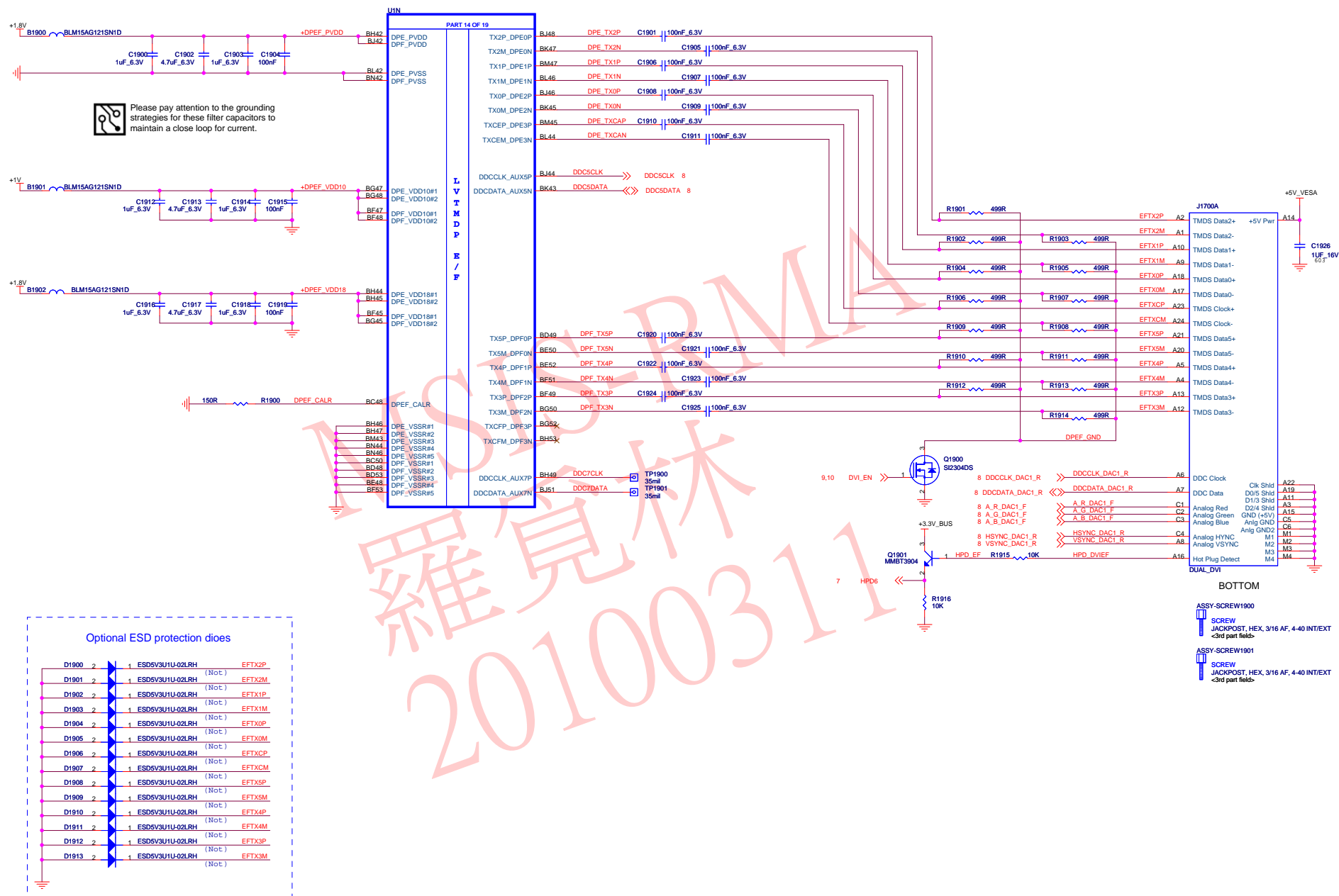
(09) CYPRESS TMDS A&B



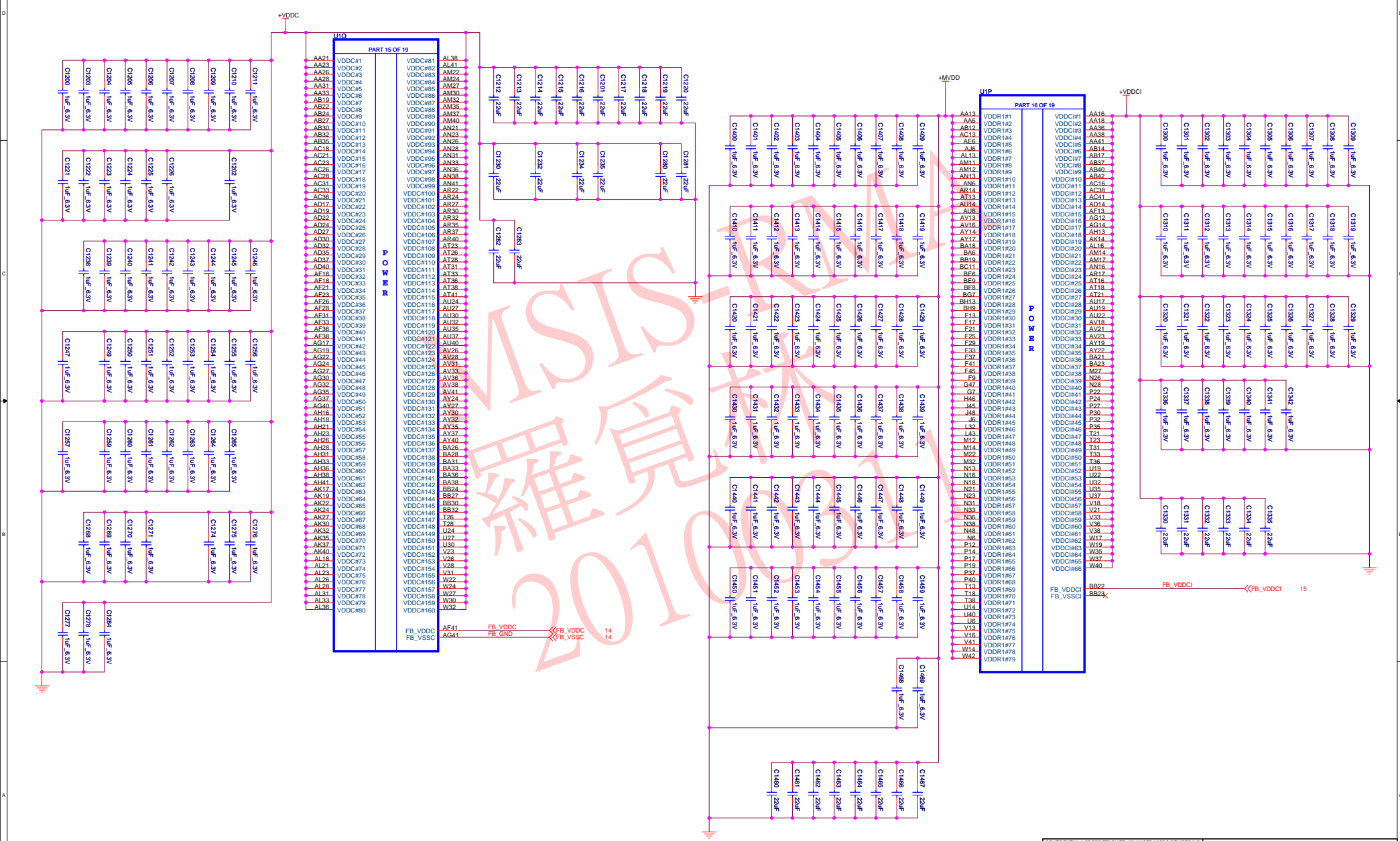
(10) CYPRESS Display Port/HDMI C&D



(11) CYPRESS LVTMDP E&F



(12) CYPRESS Power

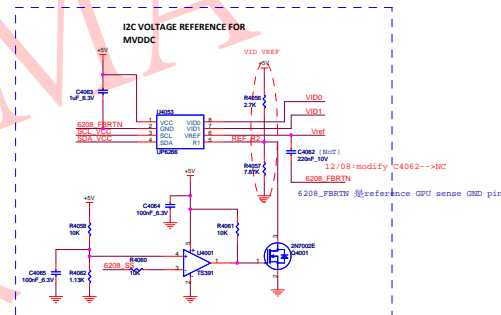
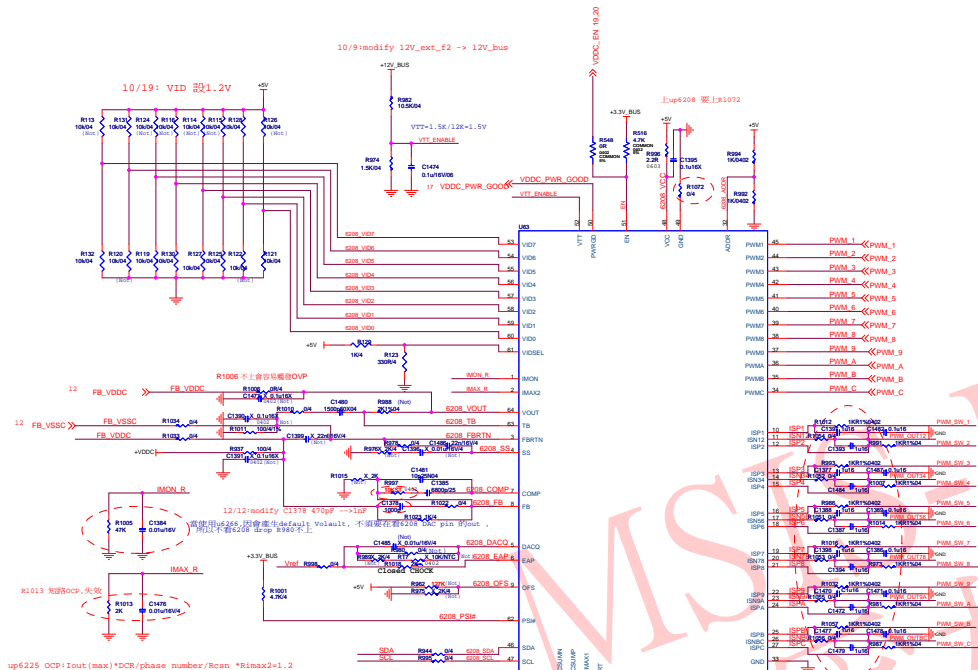


(13) CYPRESS GND

U10			U18		
PART 17 OF 19			PART 18 OF 19		
A46	VSS#1	VSS#126	BA17	VSS#251	VSS#376
AA10	VSS#2	VSS#127	BA19	VSS#252	VSS#377
AA14	VSS#3	VSS#128	BA2	VSS#253	VSS#378
AA17	VSS#4	VSS#129	BA22	VSS#254	VSS#379
AA19	VSS#5	VSS#130	BA24	VSS#255	VSS#380
AA2	VSS#6	VSS#131	BA27	VSS#256	VSS#381
AA22	VSS#7	VSS#132	BA30	VSS#257	VSS#382
AA24	VSS#8	VSS#133	BA32	VSS#258	VSS#383
AA27	VSS#9	VSS#134	BA33	VSS#259	VSS#384
AA30	VSS#10	VSS#135	BA37	VSS#260	VSS#385
AA32	VSS#11	VSS#136	BA40	VSS#261	VSS#386
AA35	VSS#12	VSS#137	BA41	VSS#262	VSS#387
AA37	VSS#13	VSS#138	BA11	VSS#263	VSS#388
AA40	VSS#14	VSS#139	BA12	VSS#264	VSS#389
AA42	VSS#15	VSS#140	BA18	VSS#265	VSS#390
AA5	VSS#16	VSS#141	BA21	VSS#266	VSS#391
AB13	VSS#17	VSS#142	BA23	VSS#267	VSS#392
AB16	VSS#18	VSS#143	BA28	VSS#268	VSS#393
AB18	VSS#19	VSS#144	BA31	VSS#269	VSS#394
AB1	VSS#20	VSS#145	BA33	VSS#270	VSS#395
AB23	VSS#21	VSS#146	BA40	VSS#271	VSS#396
AB28	VSS#22	VSS#147	BB51	VSS#272	VSS#397
AB33	VSS#23	VSS#148	BB53	VSS#273	VSS#398
AB36	VSS#24	VSS#149	BB9	VSS#274	VSS#399
AB38	VSS#25	VSS#150	BC14	VSS#275	VSS#400
AB41	VSS#26	VSS#151	BC16	VSS#276	VSS#401
AB8	VSS#27	VSS#152	BC19	VSS#277	VSS#402
AB9	VSS#28	VSS#153	BC2	VSS#278	VSS#403
AC10	VSS#29	VSS#154	BC23	VSS#279	VSS#404
AC14	VSS#30	VSS#155	BC33	VSS#280	VSS#405
AC17	VSS#31	VSS#156	BC40	VSS#281	VSS#406
AC19	VSS#32	VSS#157	BC6	VSS#282	VSS#407
AC22	VSS#33	VSS#158	BD15	VSS#283	VSS#408
AC24	VSS#34	VSS#159	BD18	VSS#284	VSS#409
AC27	VSS#35	VSS#160	BD29	VSS#285	VSS#410
AC30	VSS#36	VSS#161	BD38	VSS#286	VSS#411
AC32	VSS#37	VSS#162	BE12	VSS#287	VSS#412
AC35	VSS#38	VSS#163	BE19	VSS#288	VSS#413
AC37	VSS#39	VSS#164	BE2	VSS#289	VSS#414
AC40	VSS#40	VSS#165	BE25	VSS#290	VSS#415
AC42	VSS#41	VSS#166	BF14	VSS#291	VSS#416
AC6	VSS#42	VSS#167	BF16	VSS#292	VSS#417
AD13	VSS#43	VSS#168	BF19	VSS#293	VSS#418
AD16	VSS#44	VSS#169	BF21	VSS#294	VSS#419
AD18	VSS#45	VSS#170	BF26	VSS#295	VSS#420
AD21	VSS#46	VSS#171	BF32	VSS#296	VSS#421
AD23	VSS#47	VSS#172	BF9	VSS#297	VSS#422
AD28	VSS#48	VSS#173	BG6	VSS#298	VSS#423
AD31	VSS#49	VSS#174	BG2	VSS#299	VSS#424
AD33	VSS#50	VSS#175	BH1	VSS#300	VSS#425
AD38	VSS#51	VSS#176	BH11	VSS#301	VSS#426
AD41	VSS#52	VSS#177	BH12	VSS#302	VSS#427
AE2	VSS#53	VSS#178	BH14	VSS#303	VSS#428
AE5	VSS#54	VSS#179	BH15	VSS#304	VSS#429
AE10	VSS#55	VSS#180	BH38	VSS#305	VSS#430
AE14	VSS#56	VSS#181	BH39	VSS#306	VSS#431
AE17	VSS#57	VSS#182	BH40	VSS#307	VSS#432
AE22	VSS#58	VSS#183	BK15	VSS#308	VSS#433
AE24	VSS#59	VSS#184	BL16	VSS#309	VSS#434
AE27	VSS#60	VSS#185	BL38	VSS#310	VSS#435
AE30	VSS#61	VSS#186	BM11	VSS#311	VSS#436
AE32	VSS#62	VSS#187	BM13	VSS#312	VSS#437
AE35	VSS#63	VSS#188	BM15	VSS#313	VSS#438
AE37	VSS#64	VSS#189	BM2	VSS#314	VSS#439
AE40	VSS#65	VSS#190	BM9	VSS#315	VSS#440
AE42	VSS#66	VSS#191	BN16	VSS#316	VSS#441
AE46	VSS#67	VSS#192	BN38	VSS#317	VSS#442
AG13	VSS#68	VSS#193	F10	VSS#318	VSS#443
AG16	VSS#69	VSS#194	F14	VSS#319	VSS#444
AG18	VSS#70	VSS#195	F15	VSS#320	VSS#445
AG21	VSS#71	VSS#196	F19	VSS#321	VSS#446
AG23	VSS#72	VSS#197	F21	VSS#322	VSS#447
AG28	VSS#73	VSS#198	F23	VSS#323	VSS#448
AG30	VSS#74	VSS#199	F31	VSS#324	VSS#449
AG32	VSS#75	VSS#200	F35	VSS#325	VSS#450
AG35	VSS#76	VSS#201	F36	VSS#326	VSS#451
AG37	VSS#77	VSS#202	F39	VSS#327	VSS#452
AG40	VSS#78	VSS#203	F43	VSS#328	VSS#453
AG42	VSS#79	VSS#204	F47	VSS#329	VSS#454
AG46	VSS#80	VSS#205	F7	VSS#330	VSS#455
AG48	VSS#81	VSS#206	G2	VSS#331	VSS#456
AG51	VSS#82	VSS#207	G29	VSS#332	VSS#457
AG53	VSS#83	VSS#208	G48	VSS#333	VSS#458
AG55	VSS#84	VSS#209	G52	VSS#334	VSS#459
AG58	VSS#85	VSS#210	G6	VSS#335	VSS#460
AG61	VSS#86	VSS#211	G66	VSS#336	VSS#461
AG63	VSS#87	VSS#212	H12	VSS#337	VSS#462
AG66	VSS#88	VSS#213	H15	VSS#338	VSS#463
AG68	VSS#89	VSS#214	H21	VSS#339	VSS#464
AG71	VSS#90	VSS#215	H25	VSS#340	VSS#465
AG73	VSS#91	VSS#216	H38	VSS#341	VSS#466
AG75	VSS#92	VSS#217	H42	VSS#342	VSS#467
AG78	VSS#93	VSS#218	H46	VSS#343	VSS#468
AG81	VSS#94	VSS#219	H9	VSS#344	VSS#469
AG83	VSS#95	VSS#220	J2	VSS#345	VSS#470
AG86	VSS#96	VSS#221	J28	VSS#346	VSS#471
AG88	VSS#97	VSS#222	J31	VSS#347	VSS#472
AG91	VSS#98	VSS#223	J33	VSS#348	VSS#473
AG93	VSS#99	VSS#224	J39	VSS#349	VSS#474
AG95	VSS#100	VSS#225	K15	VSS#350	VSS#475
AG98	VSS#101	VSS#226	K19	VSS#351	VSS#476
AG101	VSS#102	VSS#227	K21	VSS#352	VSS#477
AG103	VSS#103	VSS#228	K23	VSS#353	VSS#478
AG105	VSS#104	VSS#229	K28	VSS#354	VSS#479
AG107	VSS#105	VSS#230	K32	VSS#355	VSS#480
AG109	VSS#106	VSS#231	K36	VSS#356	VSS#481
AG111	VSS#107	VSS#232	K40	VSS#357	VSS#482
AG113	VSS#108	VSS#233	K6	VSS#358	VSS#483
AG115	VSS#109	VSS#234	L12	VSS#359	VSS#484
AG117	VSS#110	VSS#235	L16	VSS#360	VSS#485
AG119	VSS#111	VSS#236	L2	VSS#361	VSS#486
AG121	VSS#112	VSS#237	L25	VSS#362	VSS#487
AG123	VSS#113	VSS#238	L29	VSS#363	VSS#488
AG125	VSS#114	VSS#239	L38	VSS#364	VSS#489
AG127	VSS#115	VSS#240		VSS#365	VSS#490
AG129	VSS#116	VSS#241		VSS#366	VSS#491
AG131	VSS#117	VSS#242		VSS#367	VSS#492
AG133	VSS#118	VSS#243		VSS#368	VSS#493
AG135	VSS#119	VSS#244		VSS#369	VSS#494
AG137	VSS#120	VSS#245		VSS#370	VSS#495
AG139	VSS#121	VSS#246		VSS#371	VSS#496
AG141	VSS#122	VSS#247		VSS#372	VSS#497
AG143	VSS#123	VSS#248		VSS#373	VSS#498
AG145	VSS#124	VSS#249		VSS#374	VSS#499
AG147	VSS#125	VSS#250		VSS#375	VSS#500

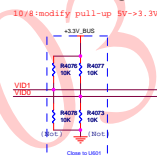
(14) VDDC

相数切换6208-->12phase 2,6,12
相数切换6208-->8phase 1,3,4
相数切换6225-->12phase 2,4,6,8,10,12(or 1,3,5,7,9,11)

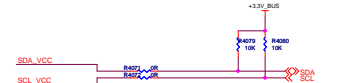


```
12/10:modify IS12,ISN34,ISN56,ISN78,ISN9A,ISNBC CIRCUIT
12/12:R1012,R991,R993,R1007,R986,R1014,R1016,R973,R1032,R981,R1057,R987 1.2K-->1K
```

VDDC DPM through GPIOs (PVID)



```
5_PWRCTRL_0 7 10/8:modify pull-up 5V->3.3V
```



```

11/20:modify
CYPRESS XT

```

State(SD)	VDDC	GPIO_15	GPIO_20
Boot-up	1.15V		
Low state	0.95V	1	1
Medium state	1.0625V	1	0
High state	1.125V	0	1
	1.175V	0	0

depends on leakage:1.125V for Night leakage
1.175V for Low leakage

State(DD)	VDDC	GPIO_15	GPIO_20
Boot-up	1.15V		
Low state	0.95V		
Low/Medium state	1.0625V	1	0
High state	1.125V	0	1
	1.175V	0	0

depends on leakage:1.125V for Night leakage
1.175V for Low leakage

CYPRESS Pro			
State(ID)	VDDC	GPIO_15	GPIO_20
Boot-up	1.0V		
Low state	1.0V	0	0
Medium state	1.038V	0	1
High state	1.088V	1	0

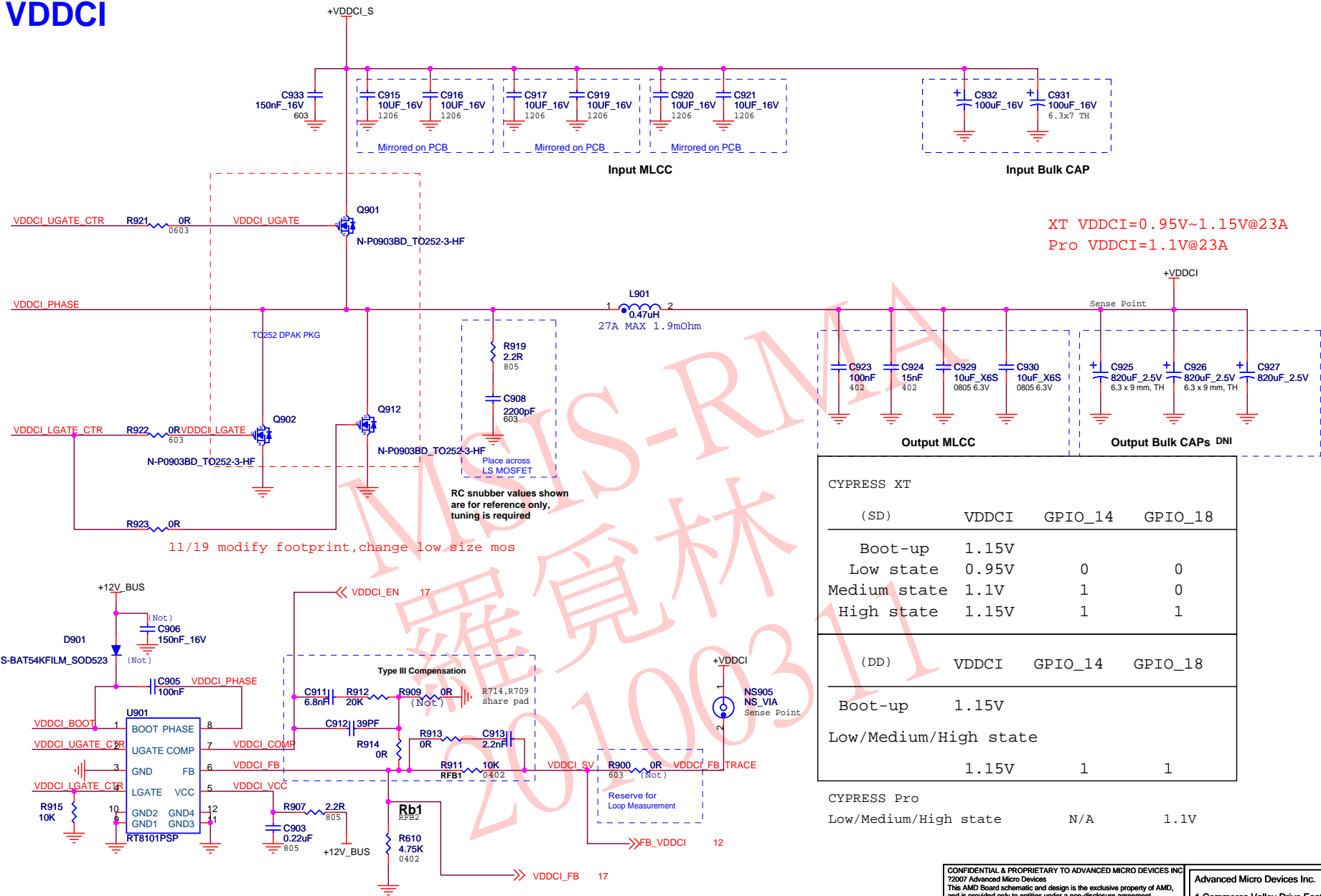
CYPRESS Pro			
State(ID)	VDDC	GPIO_15	GPIO_20
Boot-up	1.0V		
Low state	0.95V	1	1
Medium state	1.038V	0	1
High state	1.088V	1	0

	(N=6)	
SP1	R103 WT103-0402	PWM OUT12
SP2	R103 WT103-0402	PWM OUT12
SP3	R103 WT103-0402	PWM OUT34
SP4	R103 WT103-0402	PWM OUT34
SP5	R103 WT103-0402	PWM OUT56
	(N=2)	
SP6	R103 WT103-0402	PWM OUT56
	(N=2)	
SP7	R104 WT104-0402	PWM OUT78
	(N=2)	
SP8	R104 WT104-0402	PWM OUT78
	(N=1)	
SP9	R105 WT105-0402	PWM OUT9A
	(N=1)	
SP10	R105 WT105-0402	PWM OUT9A
	(N=1)	
SP11	R105 WT105-0402	PWM OUT9C
	(N=1)	
SP12	R105 WT105-0402	PWM OUT9C

State(SD)	VDDC	GPIO_15	GPIO_20
Boot-up	1.0V		
Low state	0.95V	1	1
Medium state	1.038V	0	1
High state	1.088V	1	0

	(N=6)	
SP1	R103 WT103-0402	PWM OUT12
SP2	R103 WT103-0402	PWM OUT12
SP3	R103 WT103-0402	PWM OUT34
SP4	R103 WT103-0402	PWM OUT34
SP5	R103 WT103-0402	PWM OUT56
	(N=2)	
SP6	R103 WT103-0402	PWM OUT56
	(N=2)	
SP7	R104 WT104-0402	PWM OUT78
	(N=2)	
SP8	R104 WT104-0402	PWM OUT78
	(N=1)	
SP9	R105 WT105-0402	PWM OUT9A
	(N=1)	
SP10	R105 WT105-0402	PWM OUT9A
	(N=1)	
SP11	R105 WT105-0402	PWM OUT9C
	(N=1)	
SP12	R105 WT105-0402	PWM OUT9C

(15) VDDCI



XT VDDCI=0.95V~1.15V@23A
Pro VDDCI=1.1V@23A

11/19 modify footprint, change low size mos

CYPRESS XT			
(SD)	VDDCI	GPIO_14	GPIO_18
Boot-up	1.15V		
Low state	0.95V	0	0
Medium state	1.1V	1	0
High state	1.15V	1	1
(DD)			
VDDCI	GPIO_14	GPIO_18	
Boot-up	1.15V		
Low/Medium/High state	1.15V	1	1

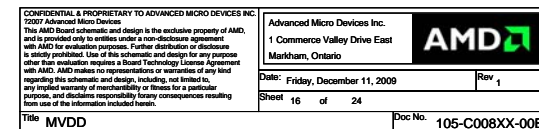
CYPRESS Pro
Low/Medium/High state N/A 1.1V

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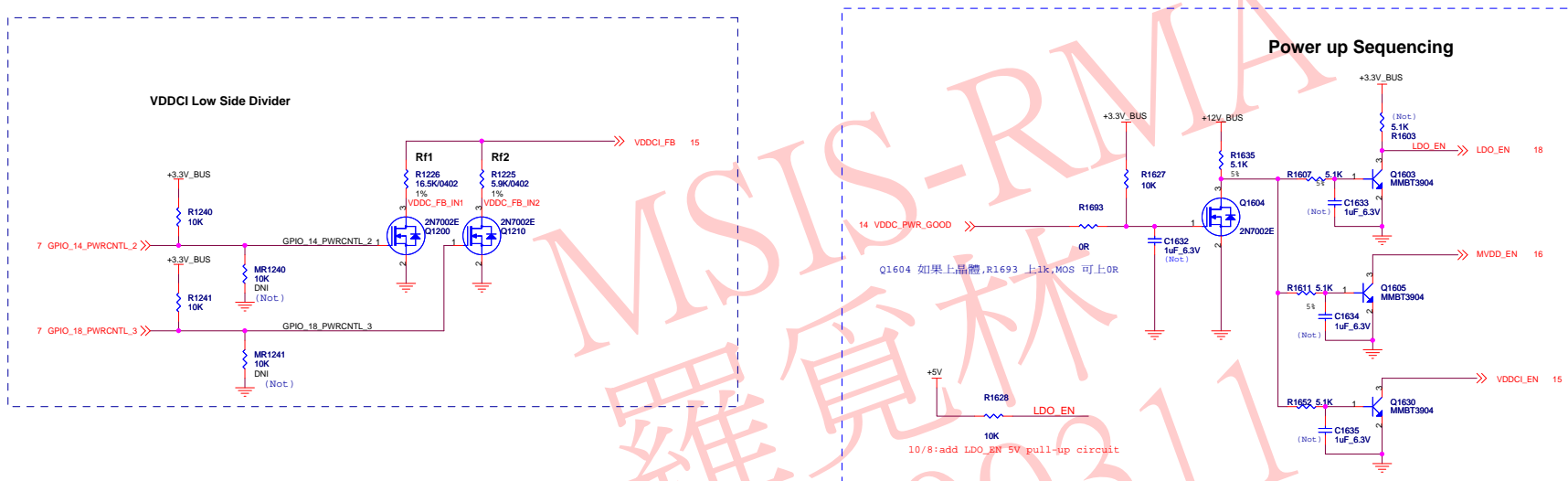
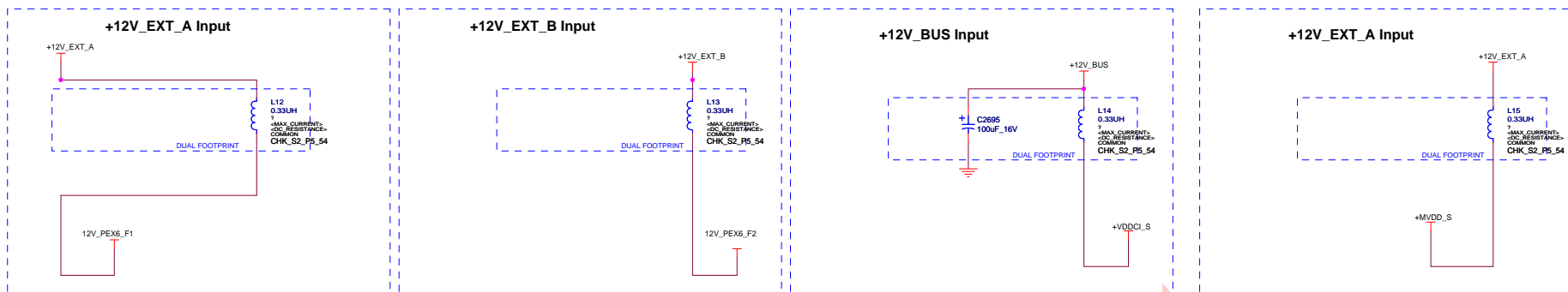
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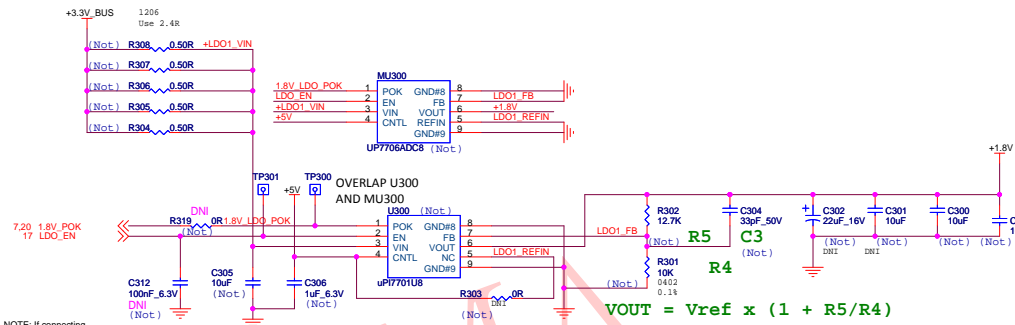
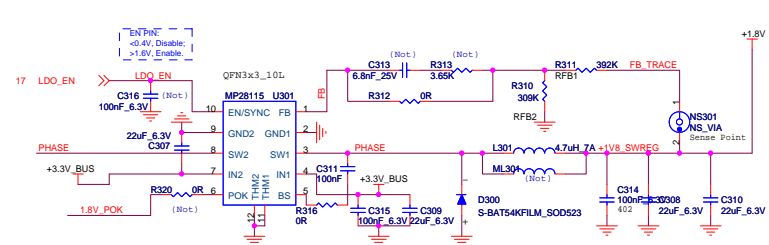


(17) CYPRESS VDDCI POWER PLAY



(18) CYPRESS Small Rail Regulators

LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



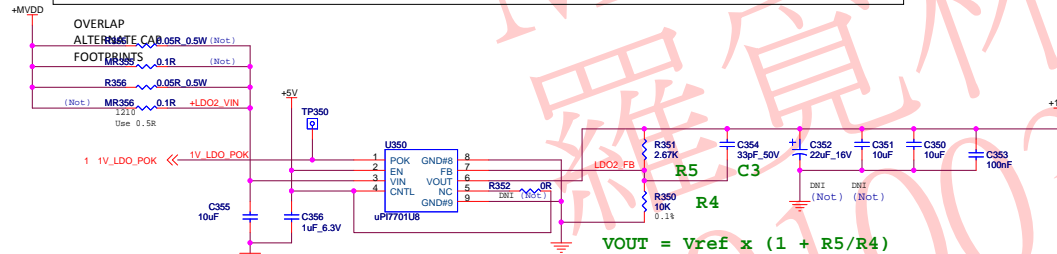
NOTE: If connecting 1V_LDO_POK, only one pull-up either to 1.8V or 3.3V

$$VOUT = Vref \times (1 + R5/R4)$$

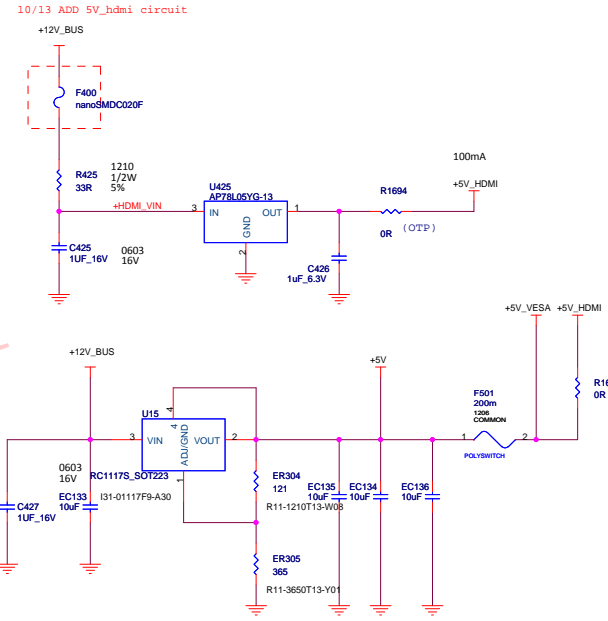
Regulators for +5V, +5V_VESA and +5V_HDMI

R450 << 15mA
R450+R451 << 30mA

LDO #2: Vin = +1.35V to 1.8V MAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

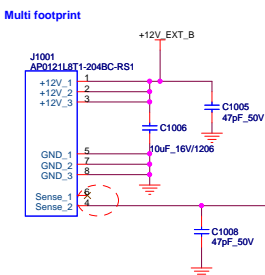


$$VOUT = Vref \times (1 + R5/R4)$$

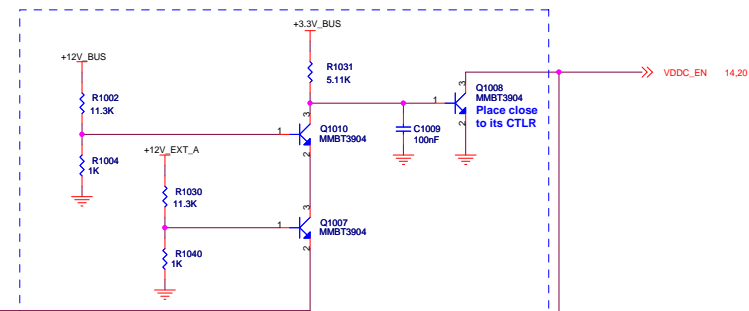


$$Vout = 1.25V \times [1 + (ER305/ER304)]$$

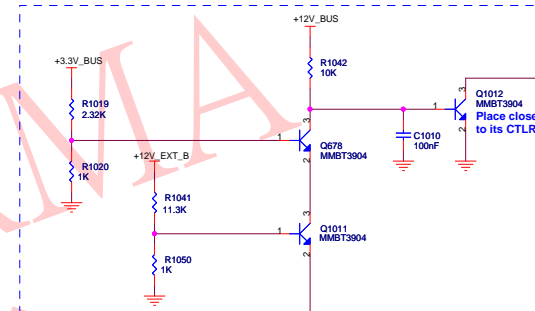
optional 5V power for VDDC regulator;



12/5 移除支援power compoent 6 pin

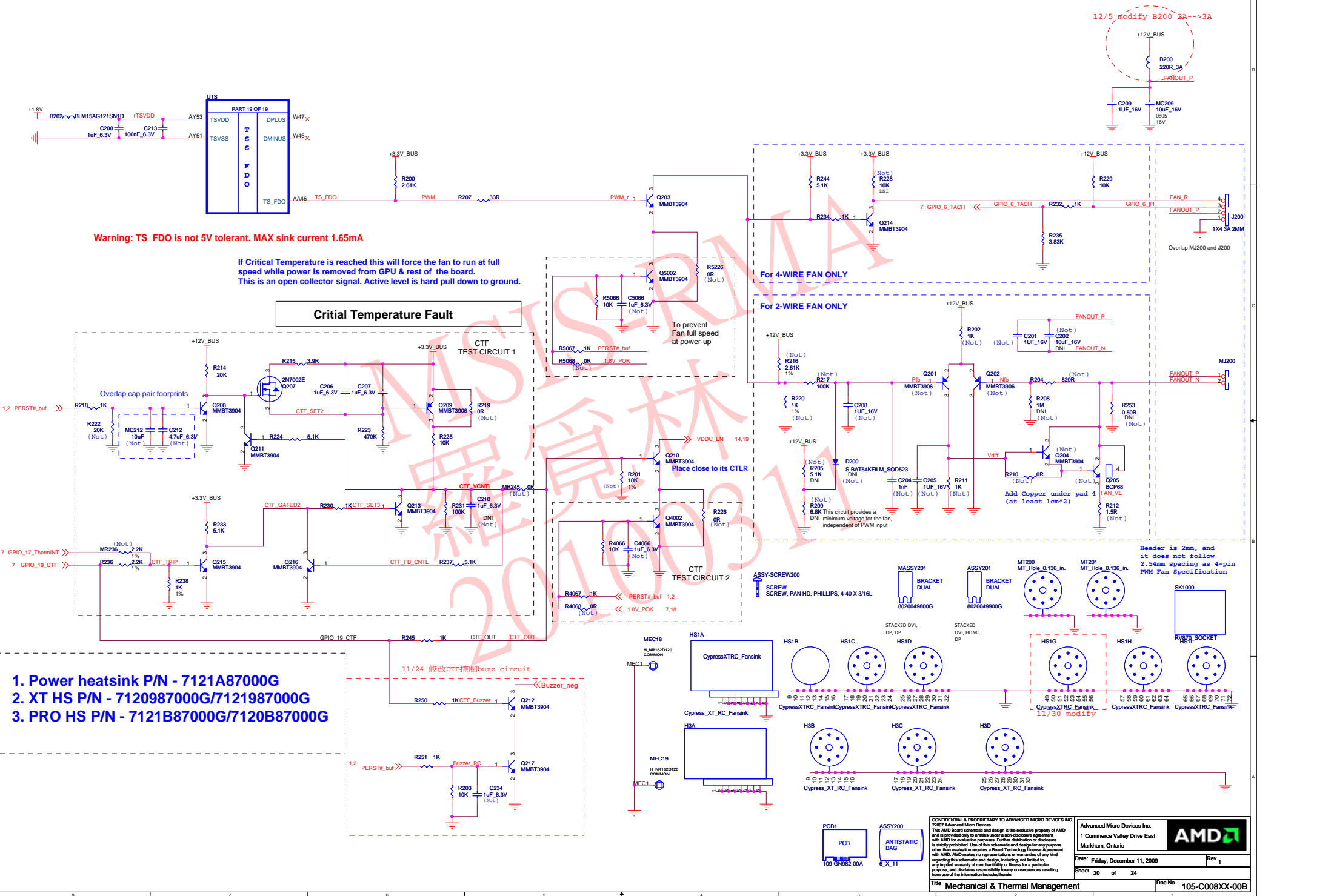


BUS 12V and AUX A Power up Seq

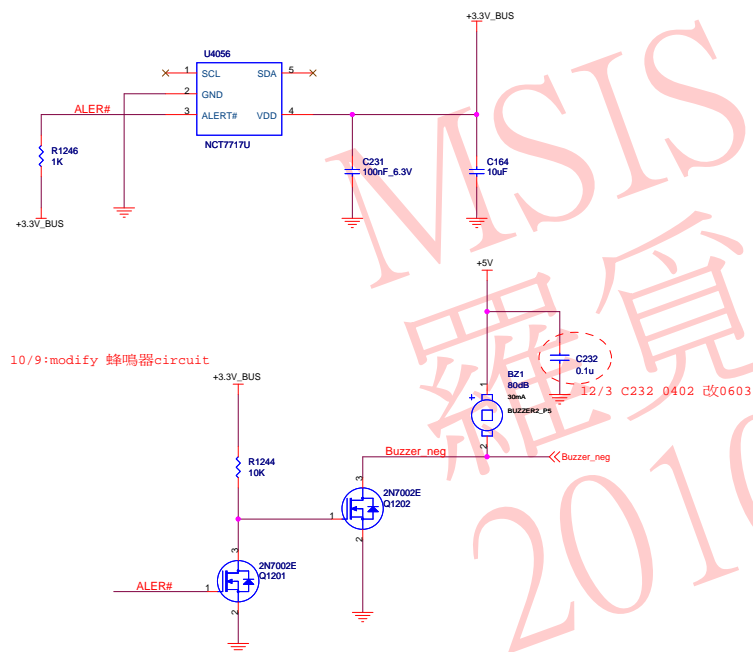
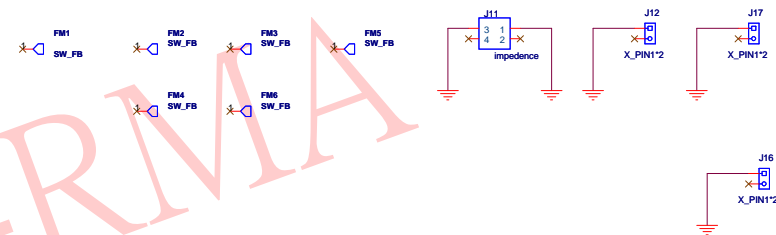
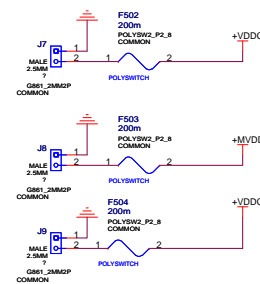
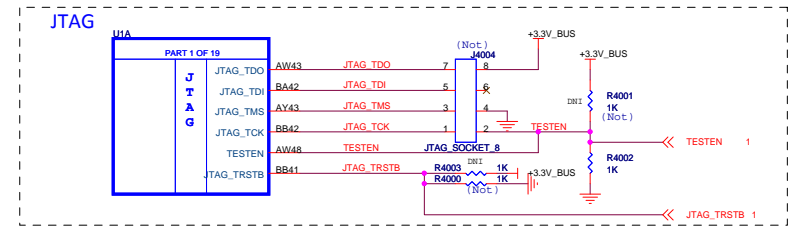


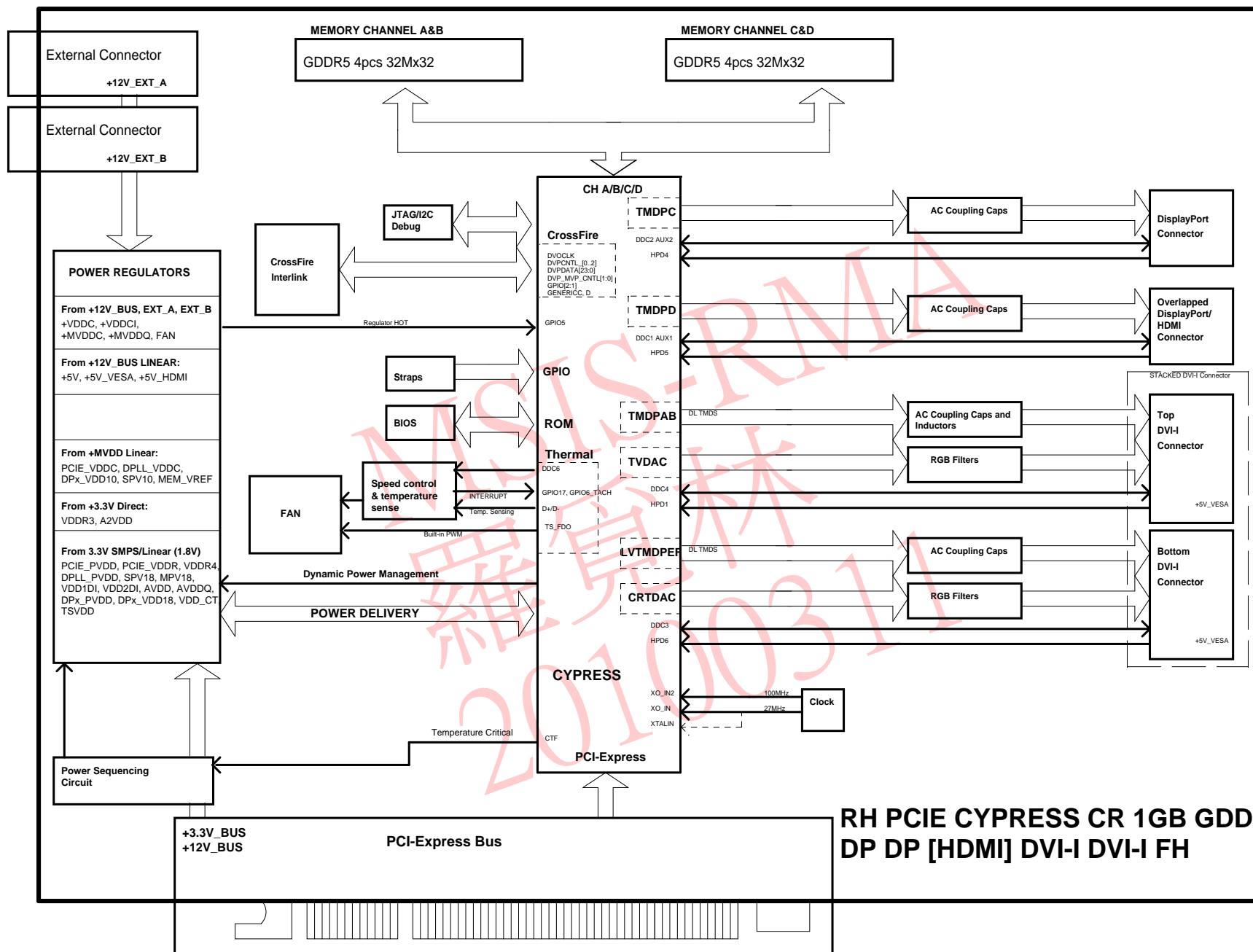
BUS 3.3V and AUX B Power up Seq

(20) CYPRESS Mechanical and Thermal Management

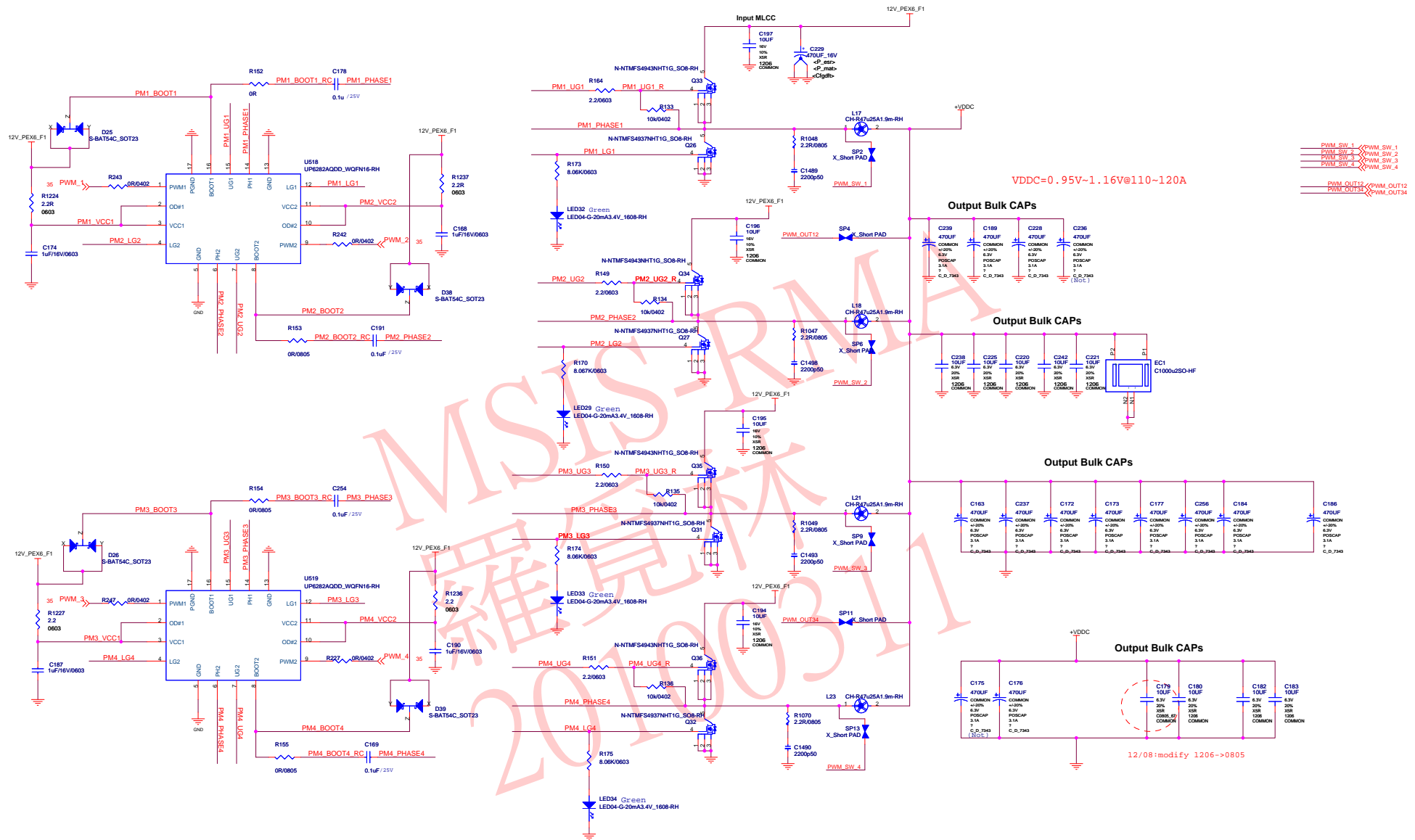


(21) CYPRESS Debug Circuits





Power Supply: VDDC 1~4 Phase powered from external PEX 8PIN



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ASSEMBLY PAGE DETAIL
SIZE: LEVEL: GENERIC BOREMATIC ONLY, COMMON & NO. 3100FF ASSEMBLY NOTES AND BOM NOT PAUL
Power Supply NVDDC Phase 1-2 of 4

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Date	Friday, December 11, 2009
Sheet	22 of 24



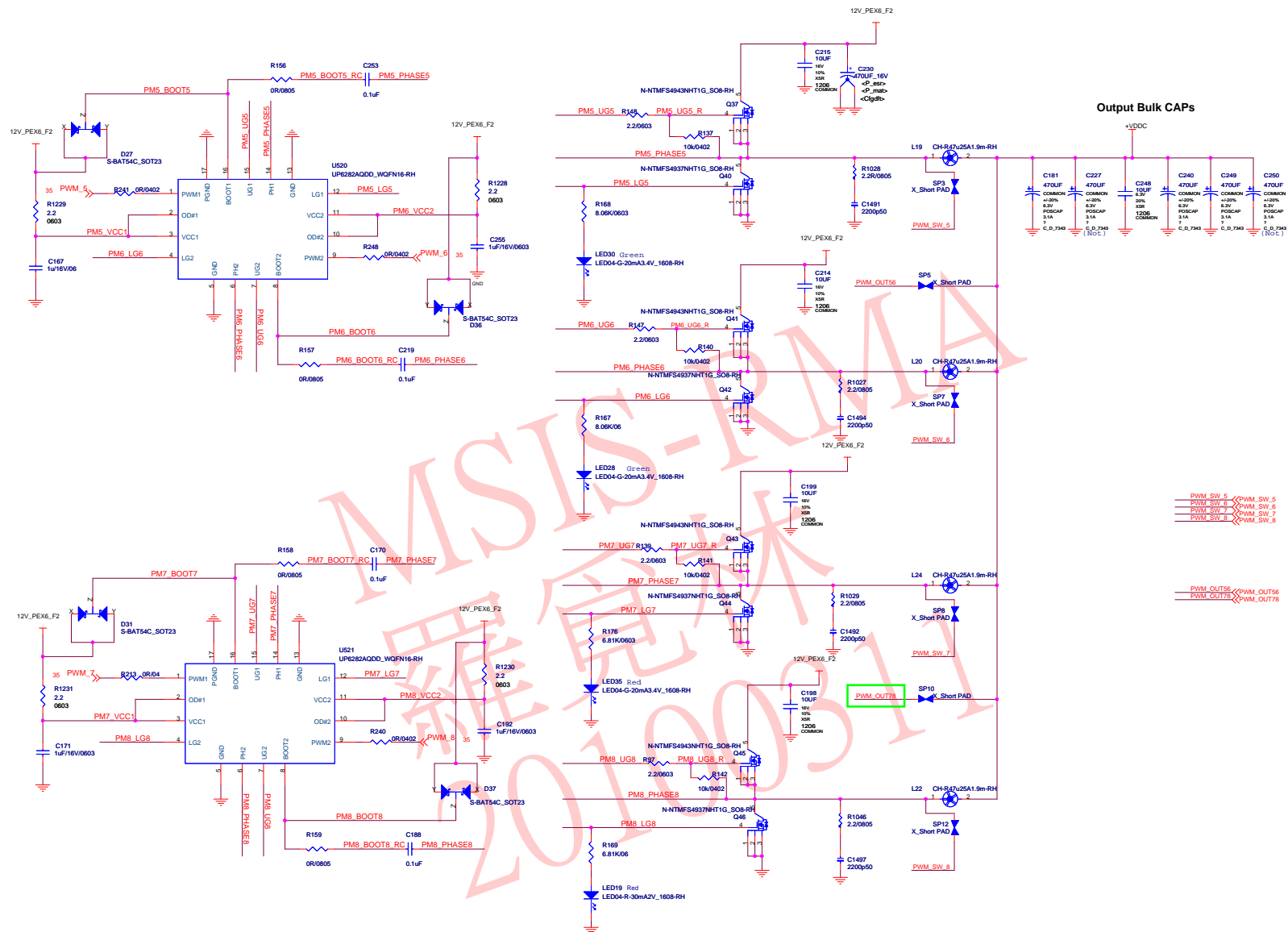
Title		Schematic No.	Date:
RH CYPRESS GDDR5 DP-HDMI-DVII-DVII		105-C008XX-00B	Friday, December 11, 2009

REVISION HISTORY		NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.	Rev 1
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Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	09/08/11	Initial release. Based on Cypress XT C001 00 PCB
1	00B	09/08/26	1. To use the Phoenix shroud with the heatsink solution Move the power connectors beside each other 2. Added PCIe reset delay circuitry;
			1.page7: co-layout CLK generator 2.page10 : remove co-layout DP component and circuit, HDMI SMD change DIP 3.page14 : remove up6213 PWM circuit , change Up6208 circuit 4.page15 : remove up6101 PWM circuit , change Up6205 circuit 5.page17 : change ML623, ML624,ML625,ML627 SMD, 12V_BUS Input 轉MVDD_S,改爲12V_EXT_A Input 6.page18 : change 5V circuit 7.page21 : add Voltage measure 8.page20 :add 1x4 Pin 風扇circuit 9.page21 : add thermal NCT7717u circuit 1.0 1.page3/4: modify DRAM_RST2 circuit 2.page7: add 27M 終端電阻

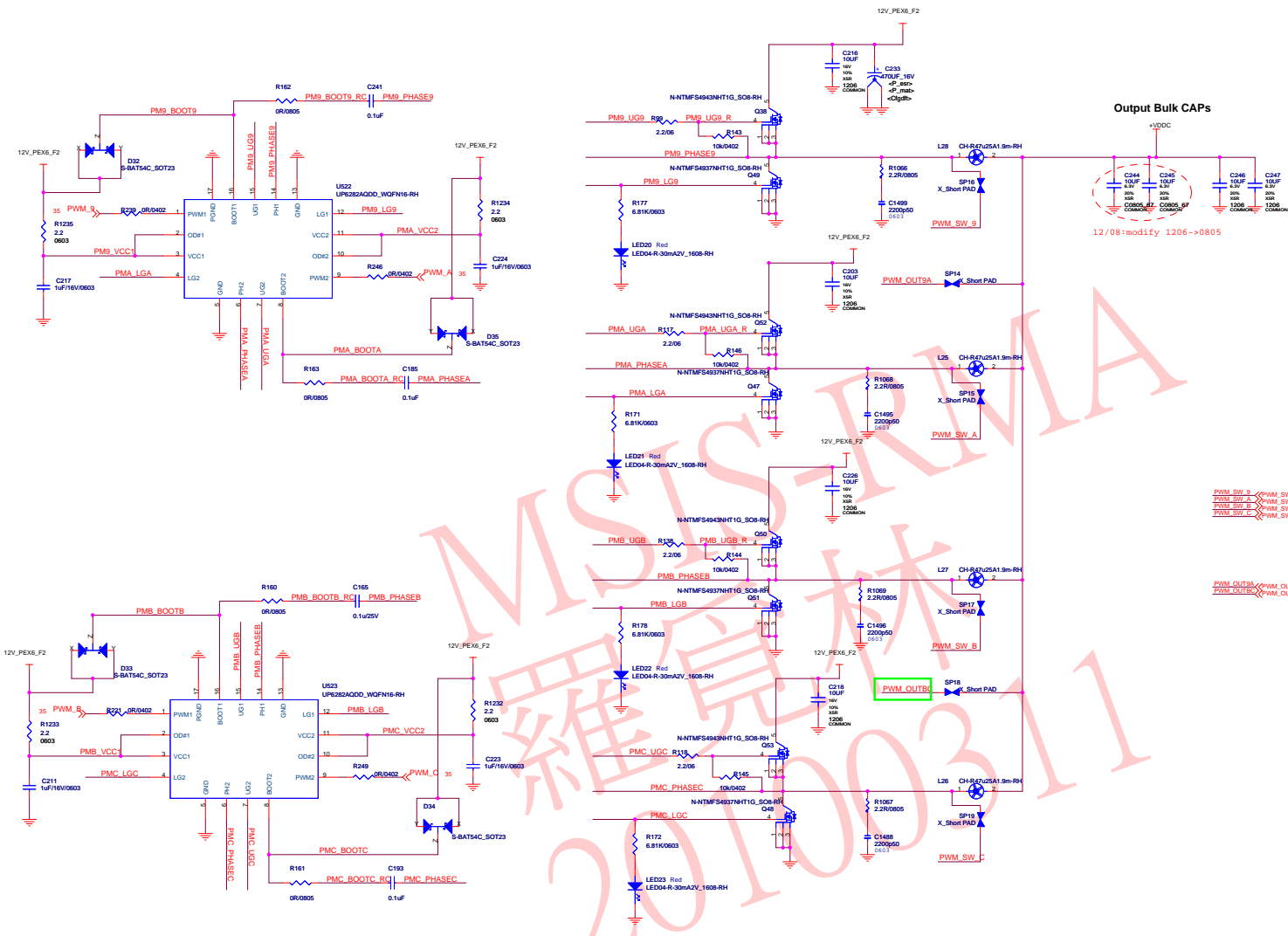
MSIS-RMA
羅覓林
20100311

Power Supply: NVVDD Phase 5~8 powered from internal PEX edge connector



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Power Supply: NVVDD Phase 9~12 powered from internal PEX edge connector



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVDD Phase 3-4 of 4



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