

PG410 A01

GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI + HDMI

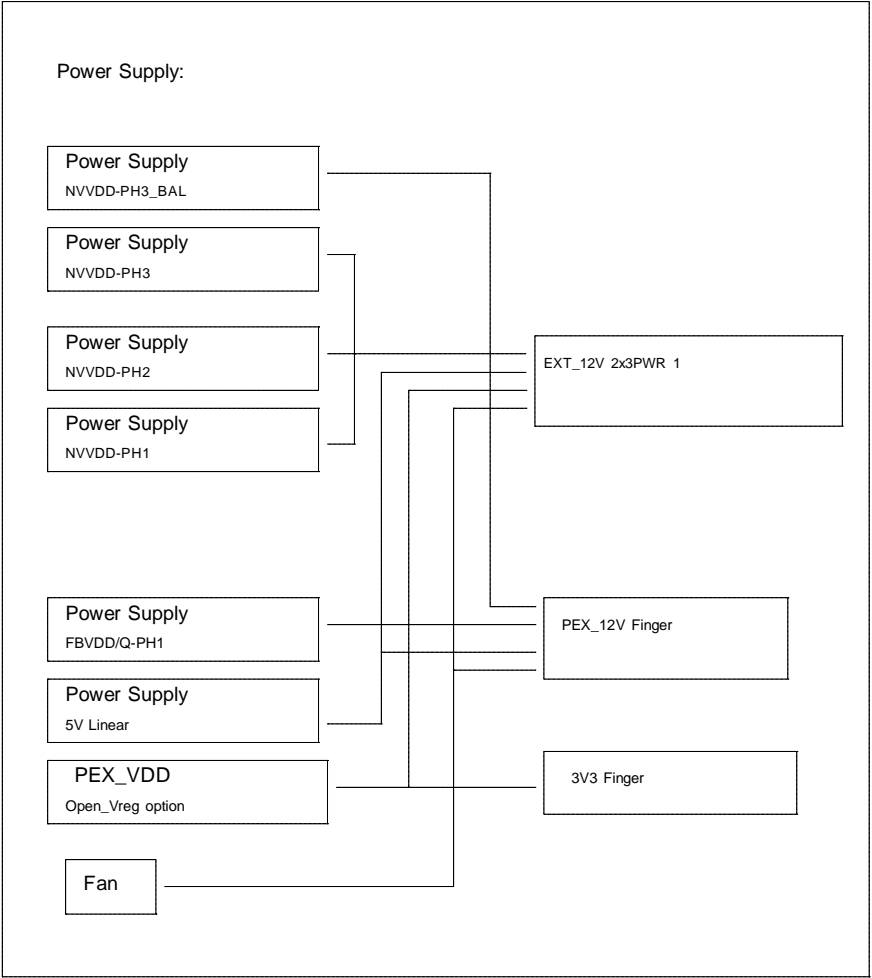
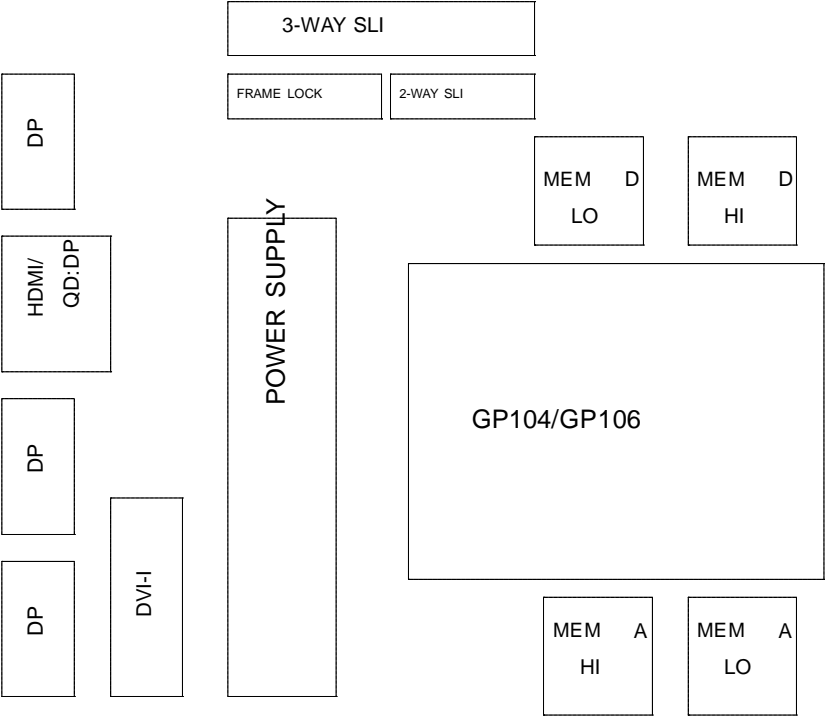
TABLE OF CONTENTS

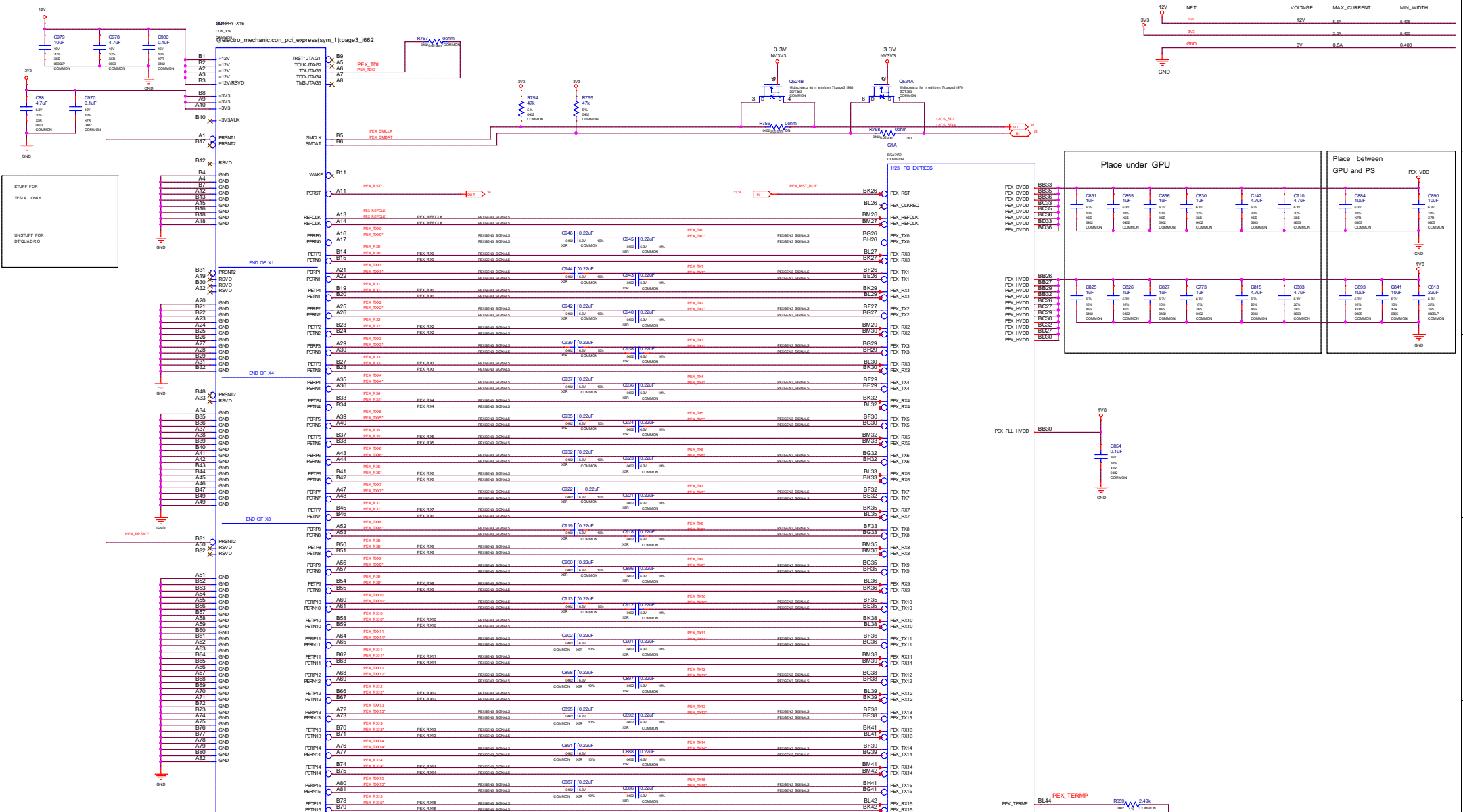
Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	GPU FB_AB
5	MEMORY: FBA[31:0]
6	MEMORY: FBA[63:32]
7	MEMORY: FBB[31:0]
8	MEMORY: FBB[63:32]
9	MEM FB_AB PWR
10	GPU FB_CD
11	MEMORY: FBC[31:0]
12	MEMORY: FBC[63:32]
13	MEMORY: FBD[31:0]
14	MEMORY: FBD[63:32]
15	MEM FB_CD PWR
16	GPU PWR & GND
17	GPU Decoupling
18	IFPAB DVI-D-DL
19	IFPE DP
20	IFPF DP
21	IFPC HDMI/DP
22	IFPD DP
23	MIOA/B Interface and Frame Lock
24	MISC1: Fan, Thermal, JTAG, GPIO,STEREO
25	MISC2: ROM, XTAL,STRAPS

Page	Description
26	PS: 1V8_PLL, 1V8_AON
27	PS: 5V, PEX_VDD
28	PS: NV3V3, NV12V
29	PS: FBVDD
30	PS: NVVDD Controller
31	PS: NVVDD Phase 1,2 & 3
32	PS: NVVDD Rail Balance Login & Dynamic Phase
33	PS: Input, Filtering, and Monitoring
34	PS: 12V Power Steering,PSI Control & LED
35	PS: Shut Down and Sequencing
36	PS: GC6 MISC
37	MECH

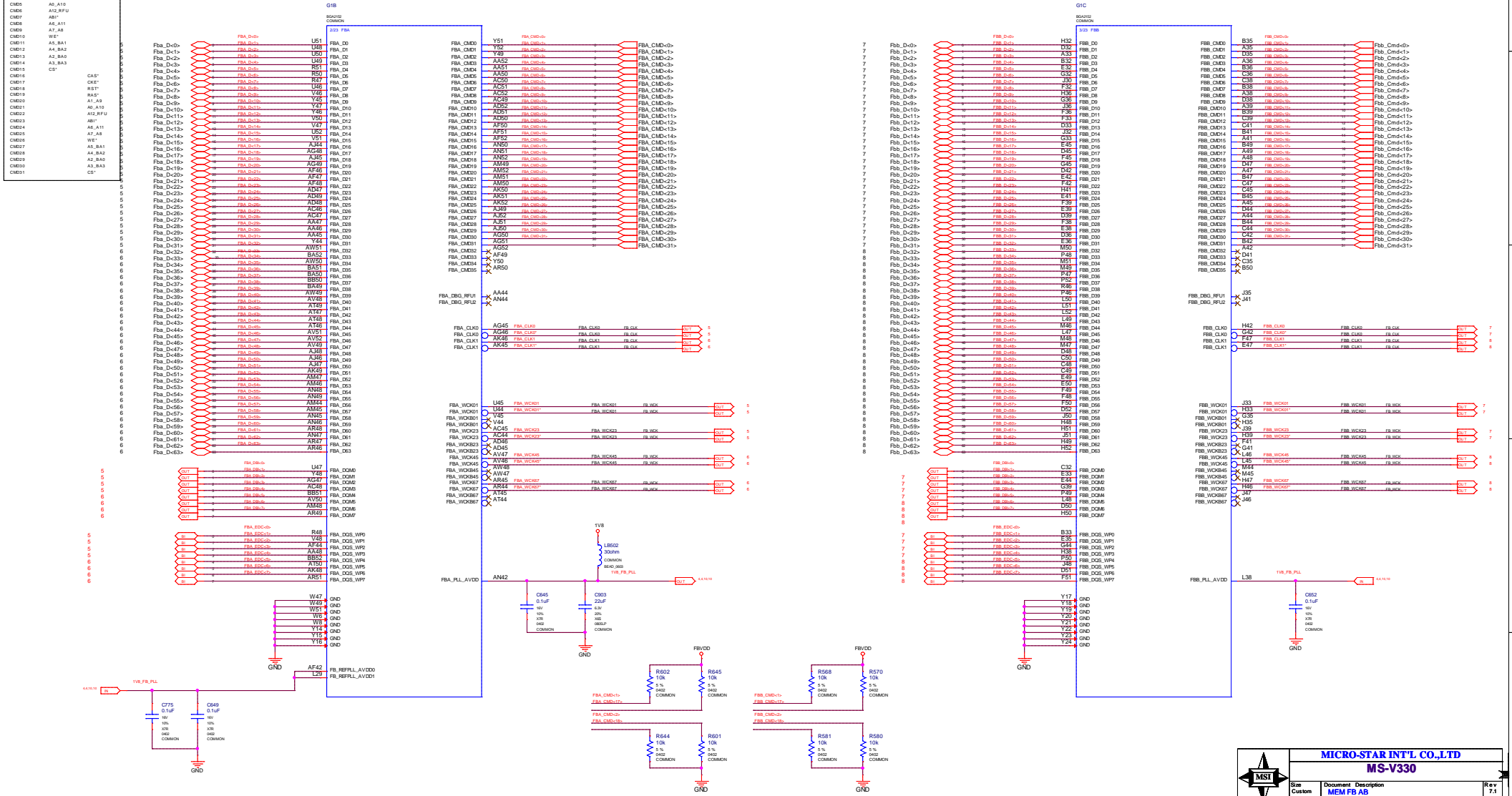
V330-7.0 修 PG41 00
1. 增加 5V 1 DO
2. PEX_VDD 5V 1 DO
3. NVVDD/FBVDD 修
4. 增加 PEX_C 5V 1 DO

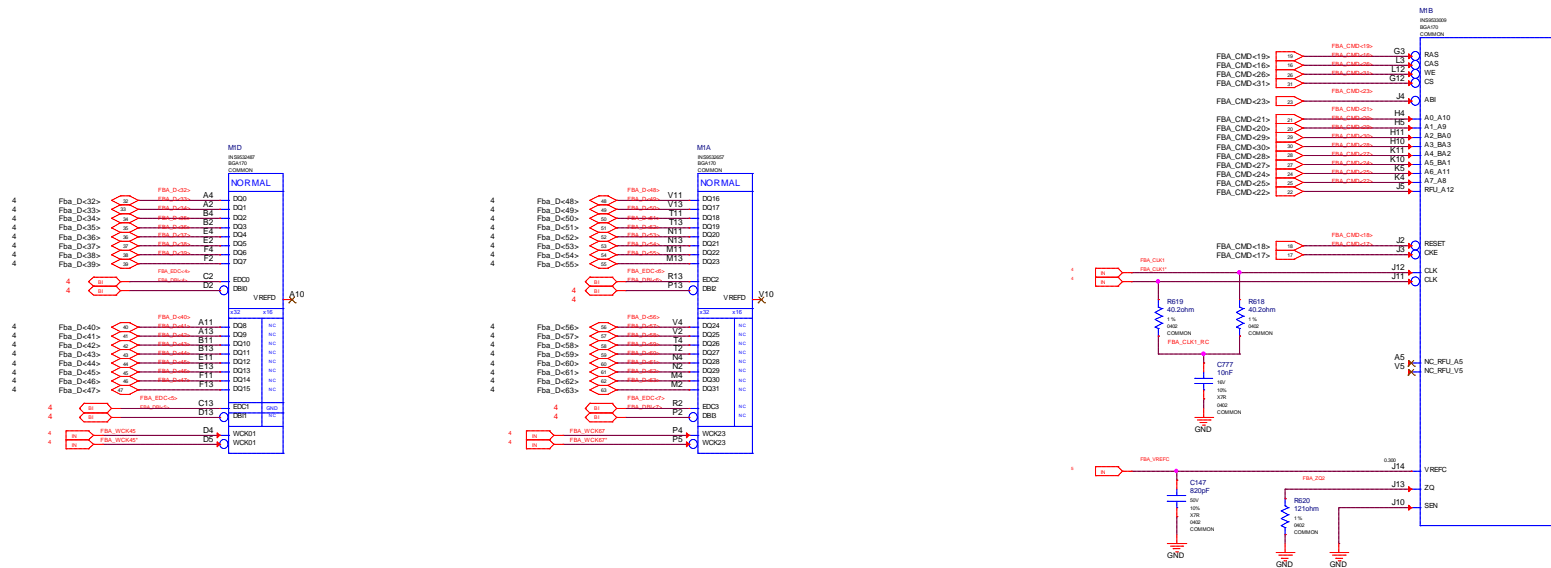
MICRO-STAR INT'L CO.,LTD			
MS-V330			
Size	Document	Description	Rev
Custom	TABLE		7.1
Date: Friday, January 06, 2017		Sheet 1 of 37	

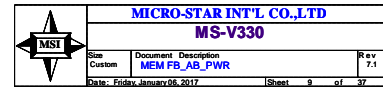
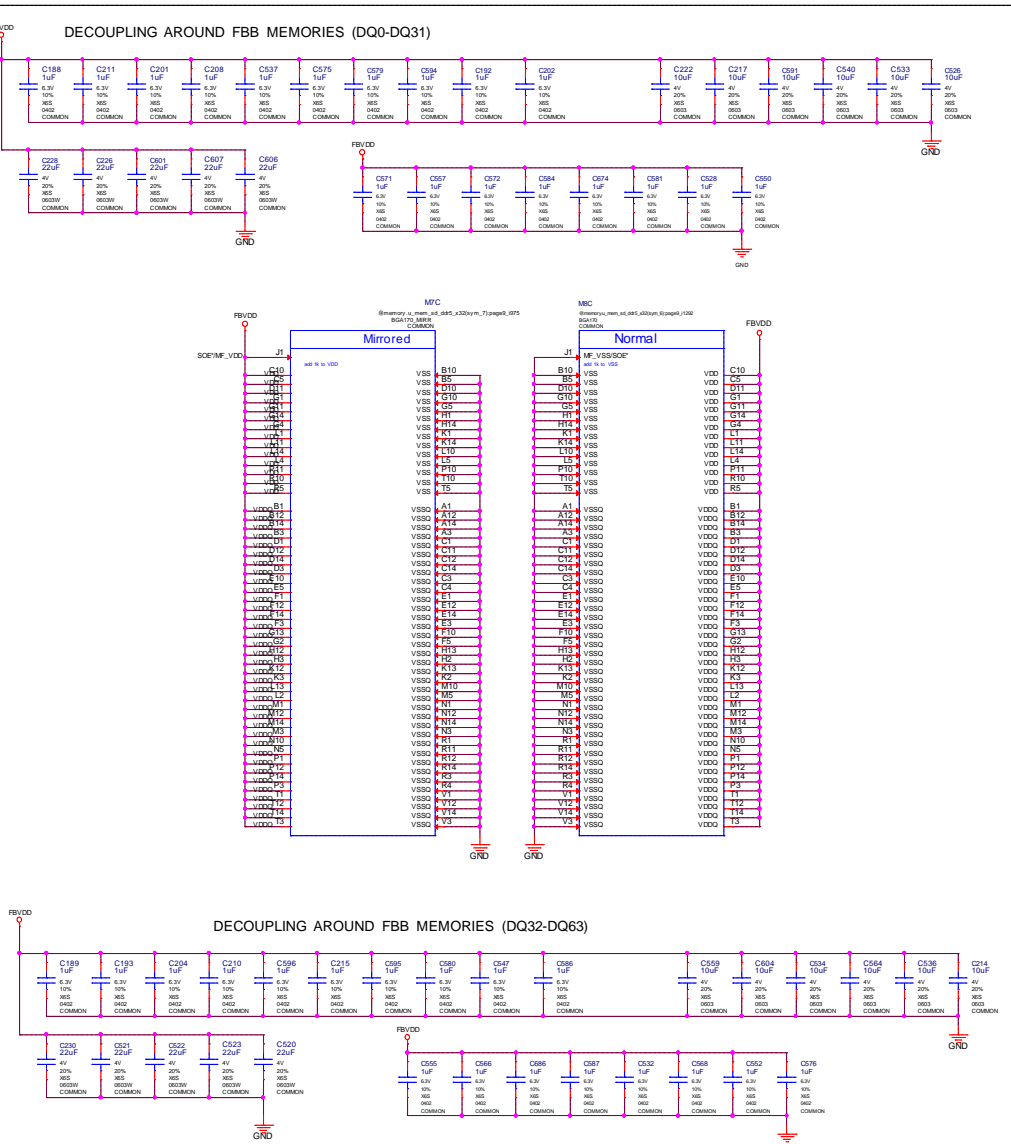
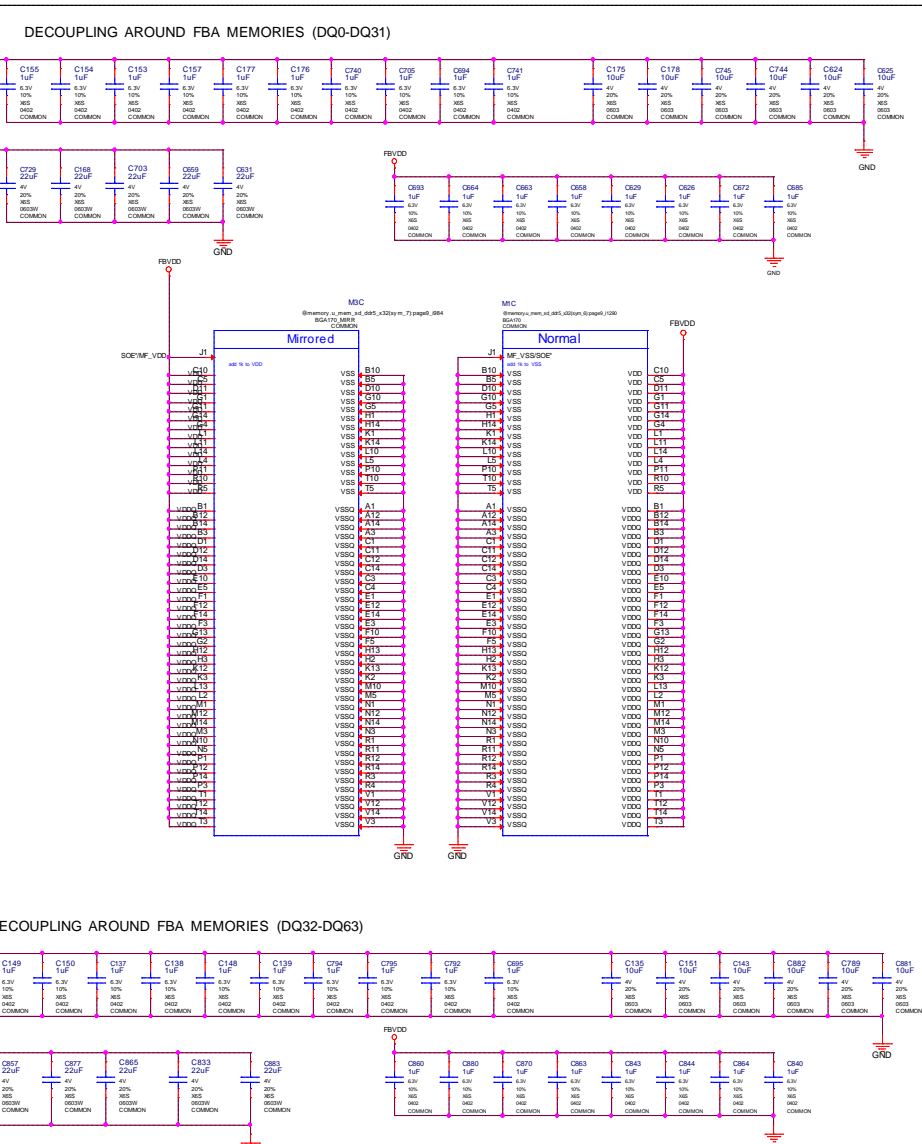


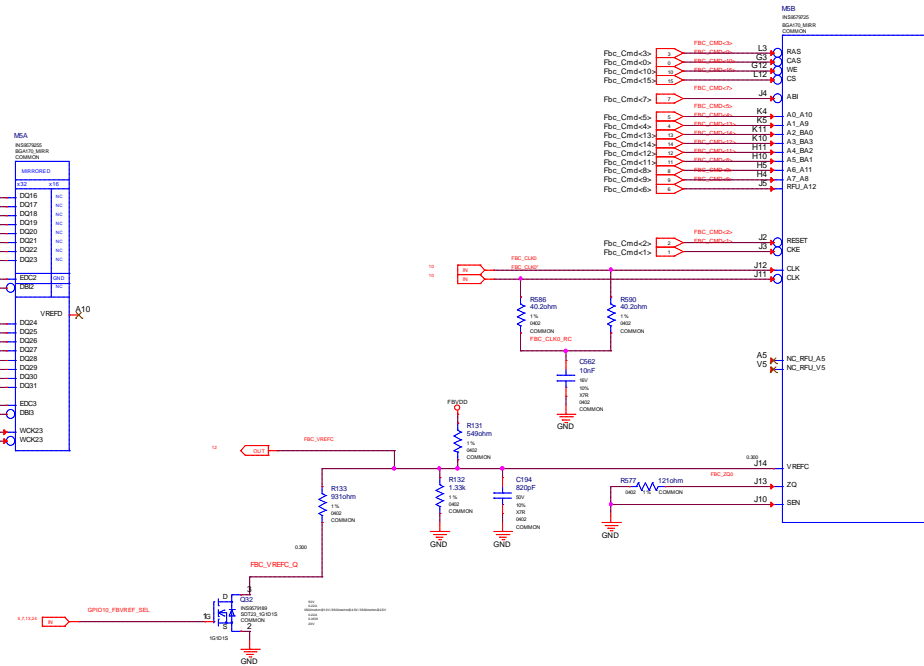
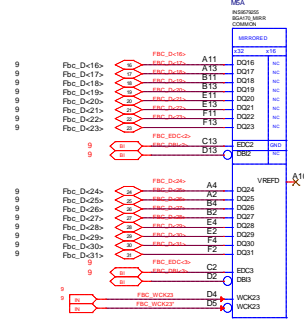
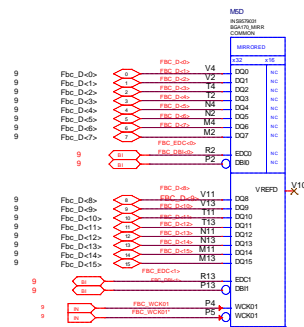


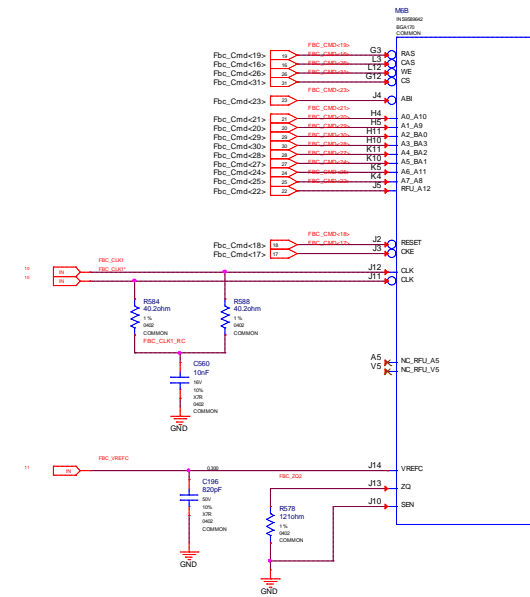
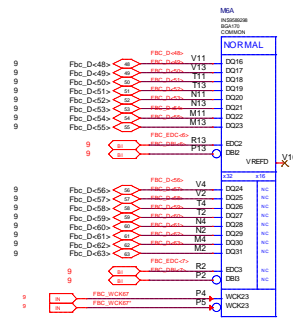
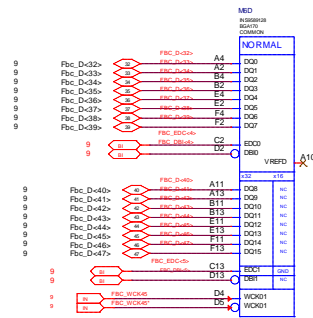
GDOR CMD Mapping		
CMD	S_A1	S_A2
CM00	CAS*	
CM01	CKE*	
CM02	RST*	
CM03	RA5*	
CM04	A1_A0	
CM05	A0_A10	
CM06	A10_RFU	
CM07	ABU*	
CM08	AS_A11	
CM09	A1_A0	
CM10	WE*	
CM11	A1_A0	
CM12	A1_A0	
CM13	A1_A0	
CM14	A1_A0	
CM15	CS*	
CM16	CAS*	
CM17	CKE*	
CM18	RST*	
CM19	RA5*	
CM20	A1_A0	
CM21	A1_A0	
CM22	A10_RFU	
CM23	ABU*	
CM24	AS_A11	
CM25	A1_A0	
CM26	WE*	
CM27	AS_A11	
CM28	A1_A0	
CM29	A1_A0	
CM30	A1_A0	
CM31	CS*	

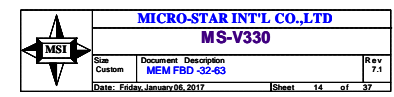
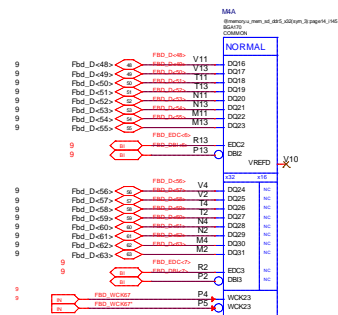


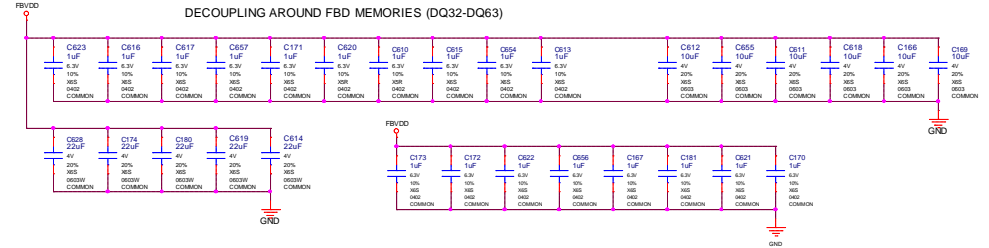
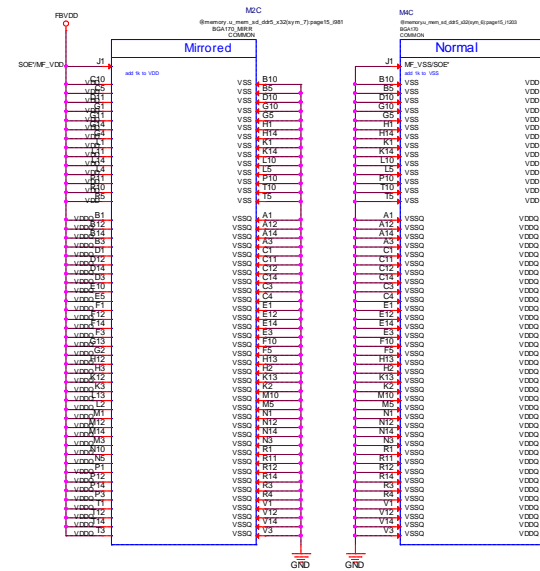
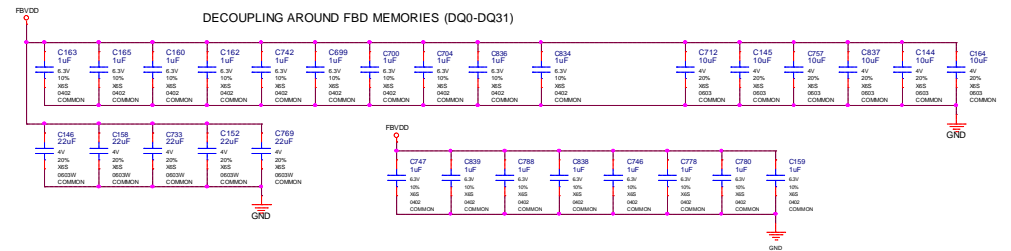


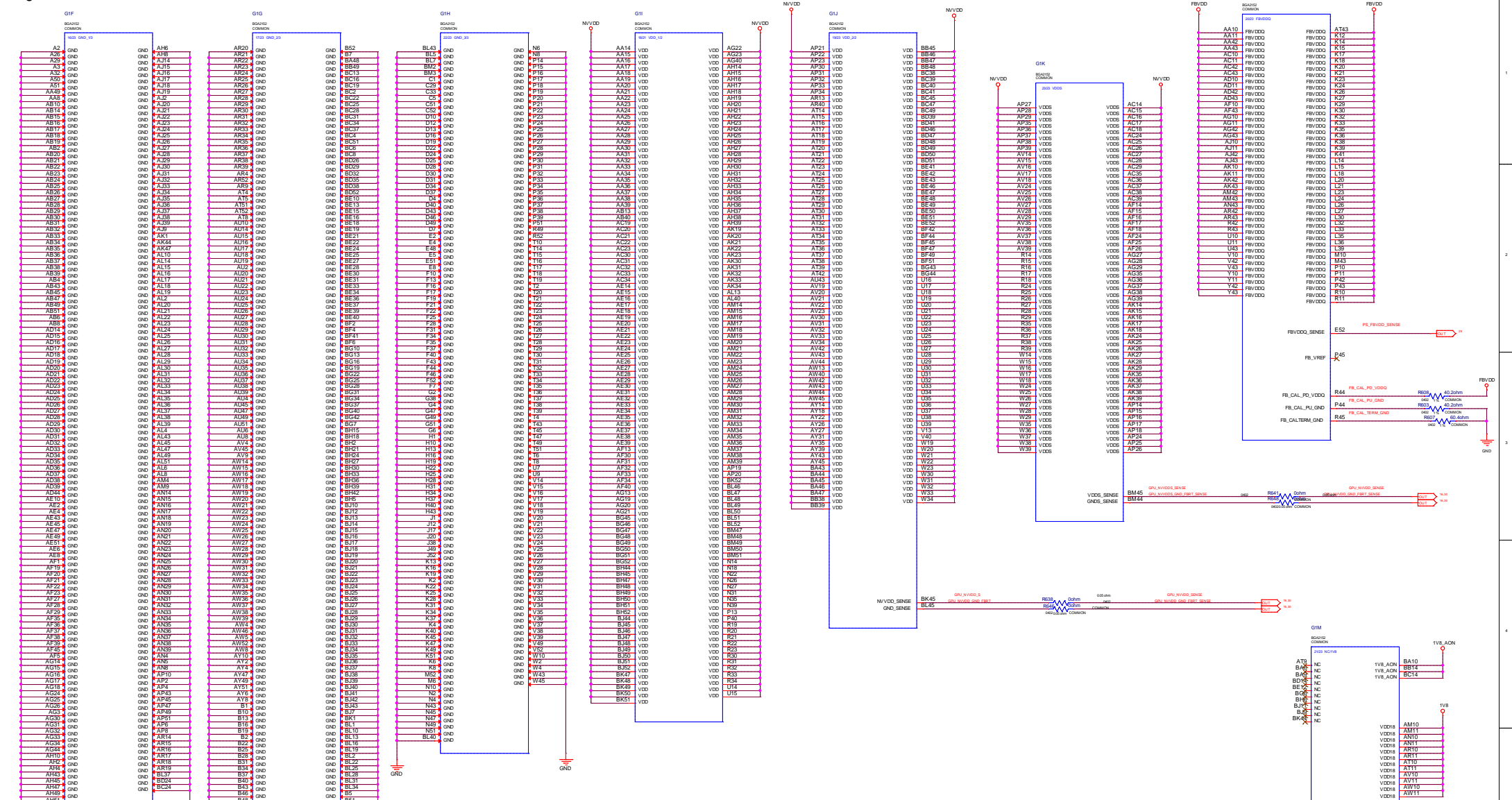




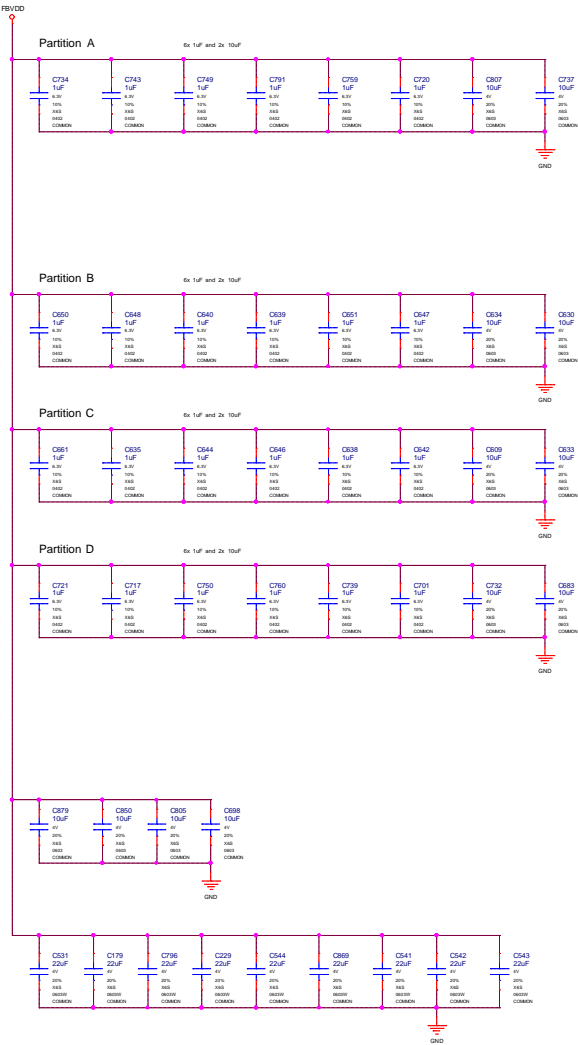




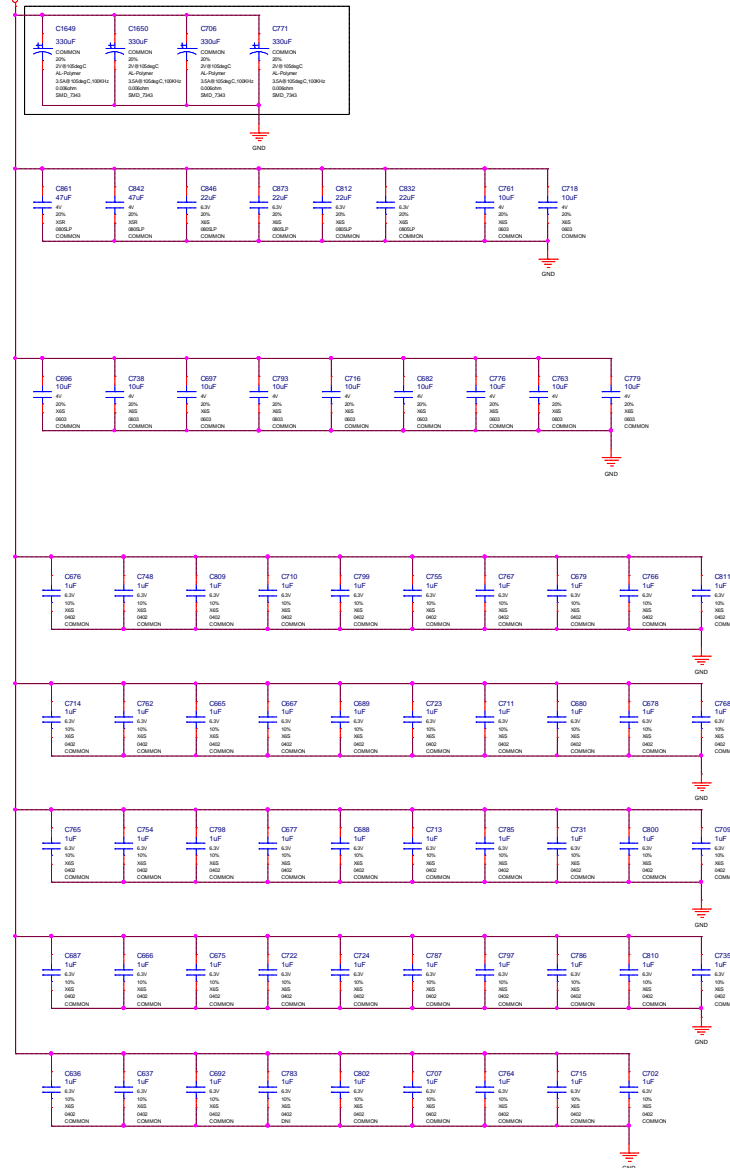




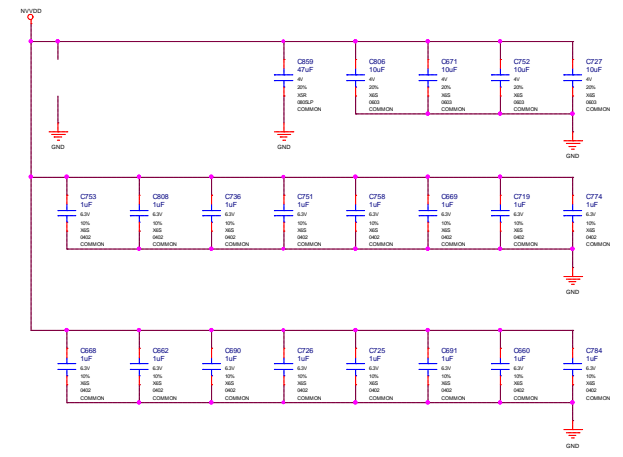
FBVDD



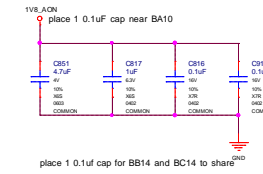
NVDD



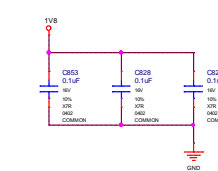
NVDD

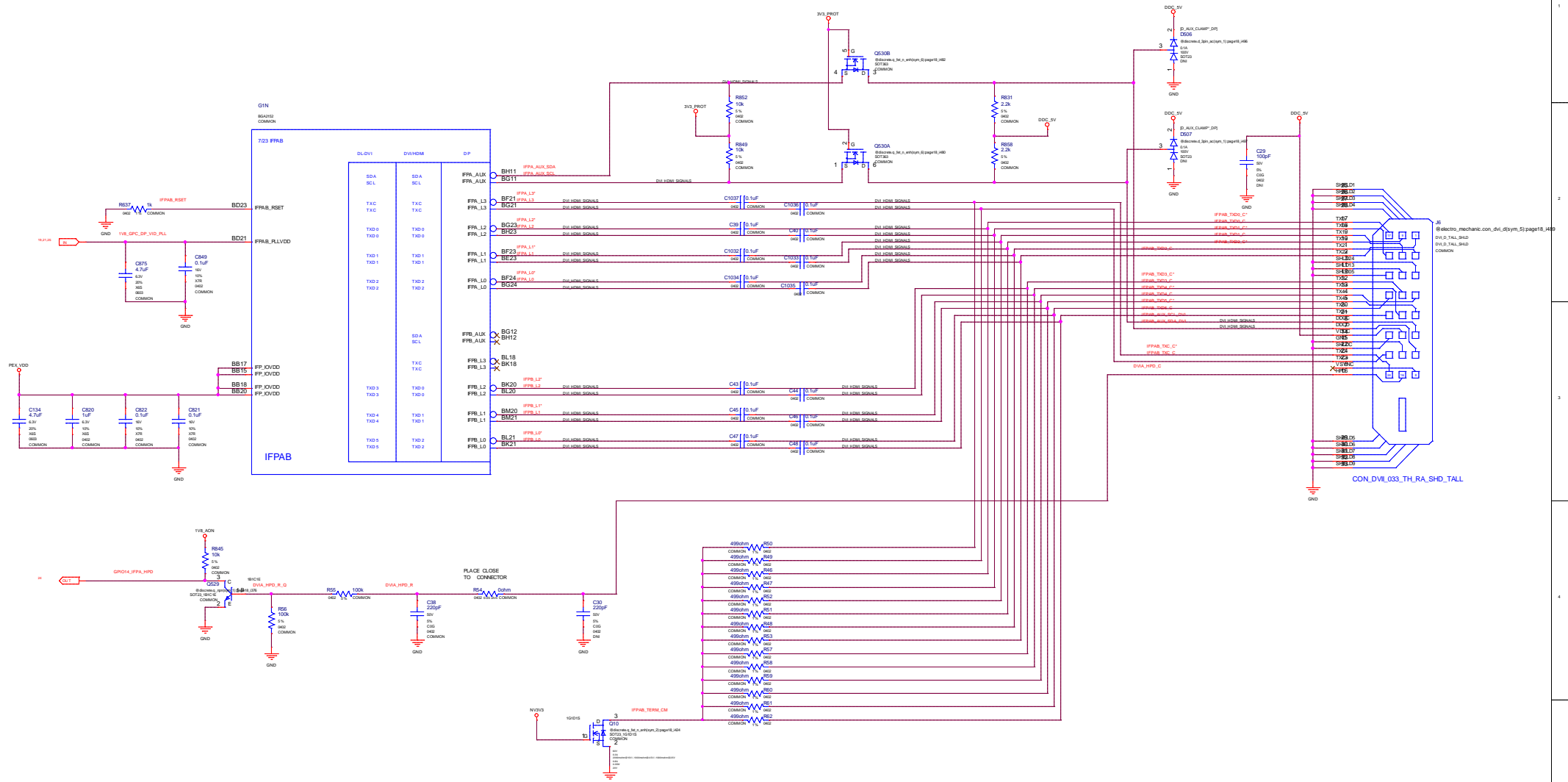


1V8_AON

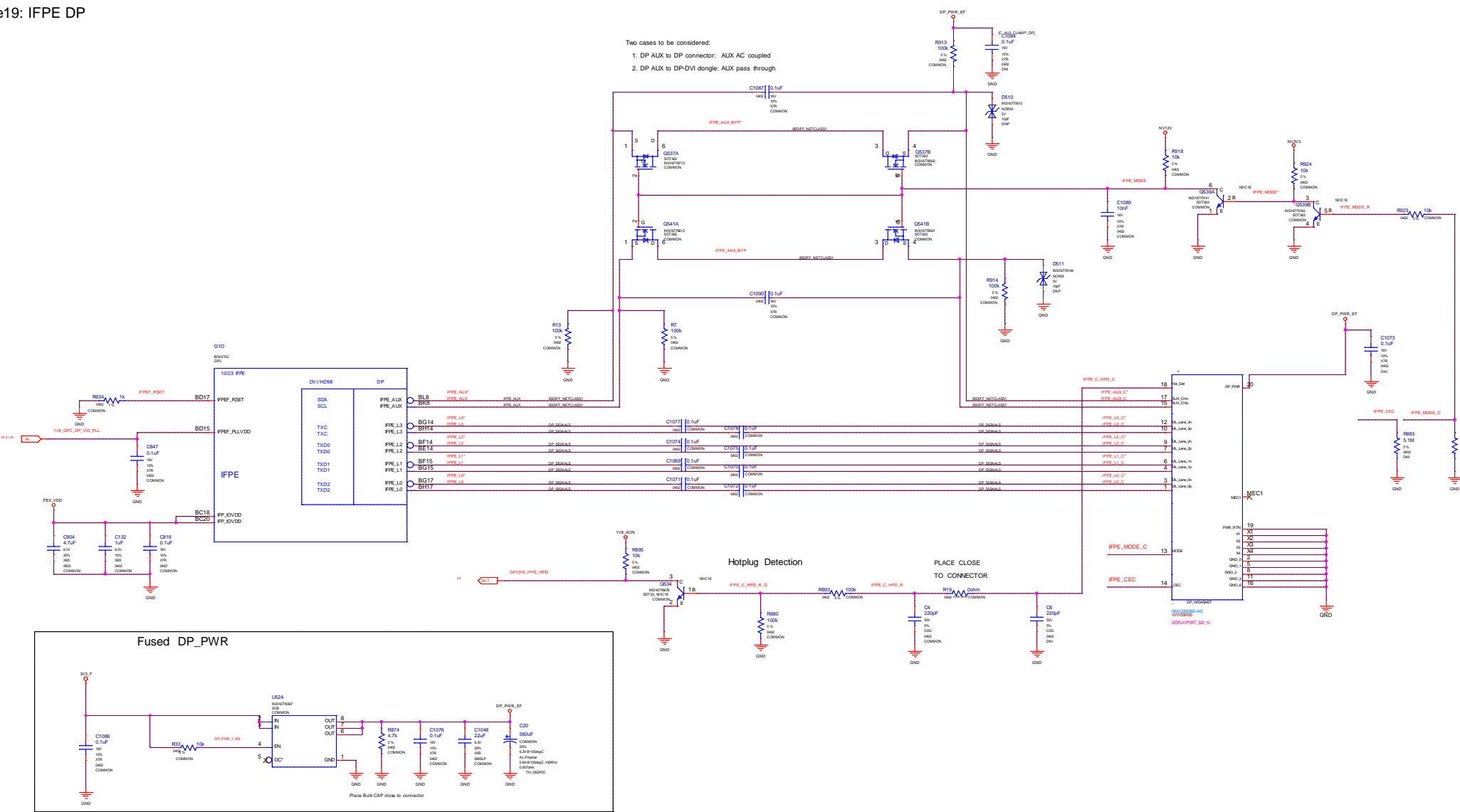


1V8_MAIN



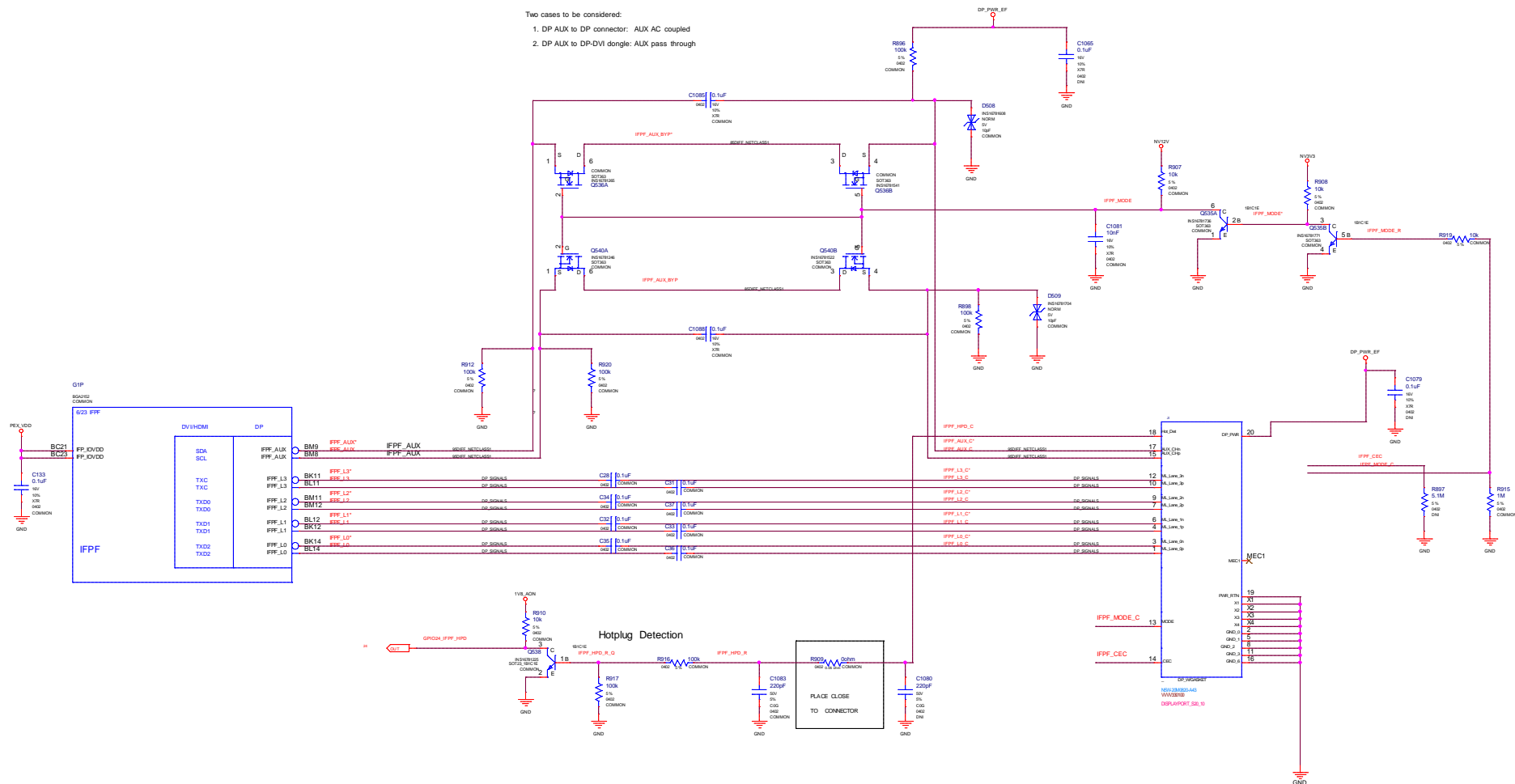


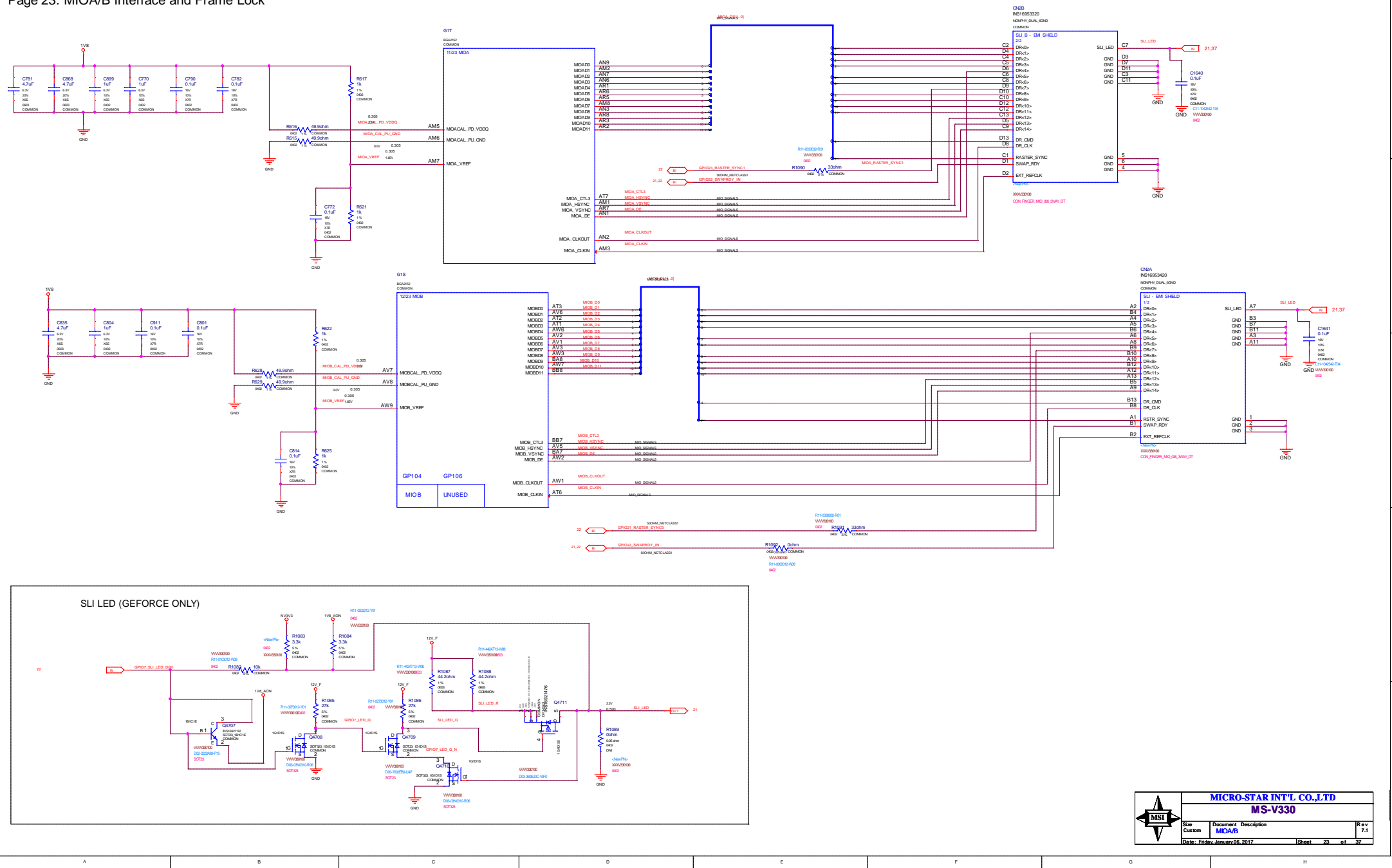
- Two cases to be considered:
- 1. DP AUX to DP connector: AUX AC coupled
 - 2. DP AUX to DP-DVI dongle: AUX pass through

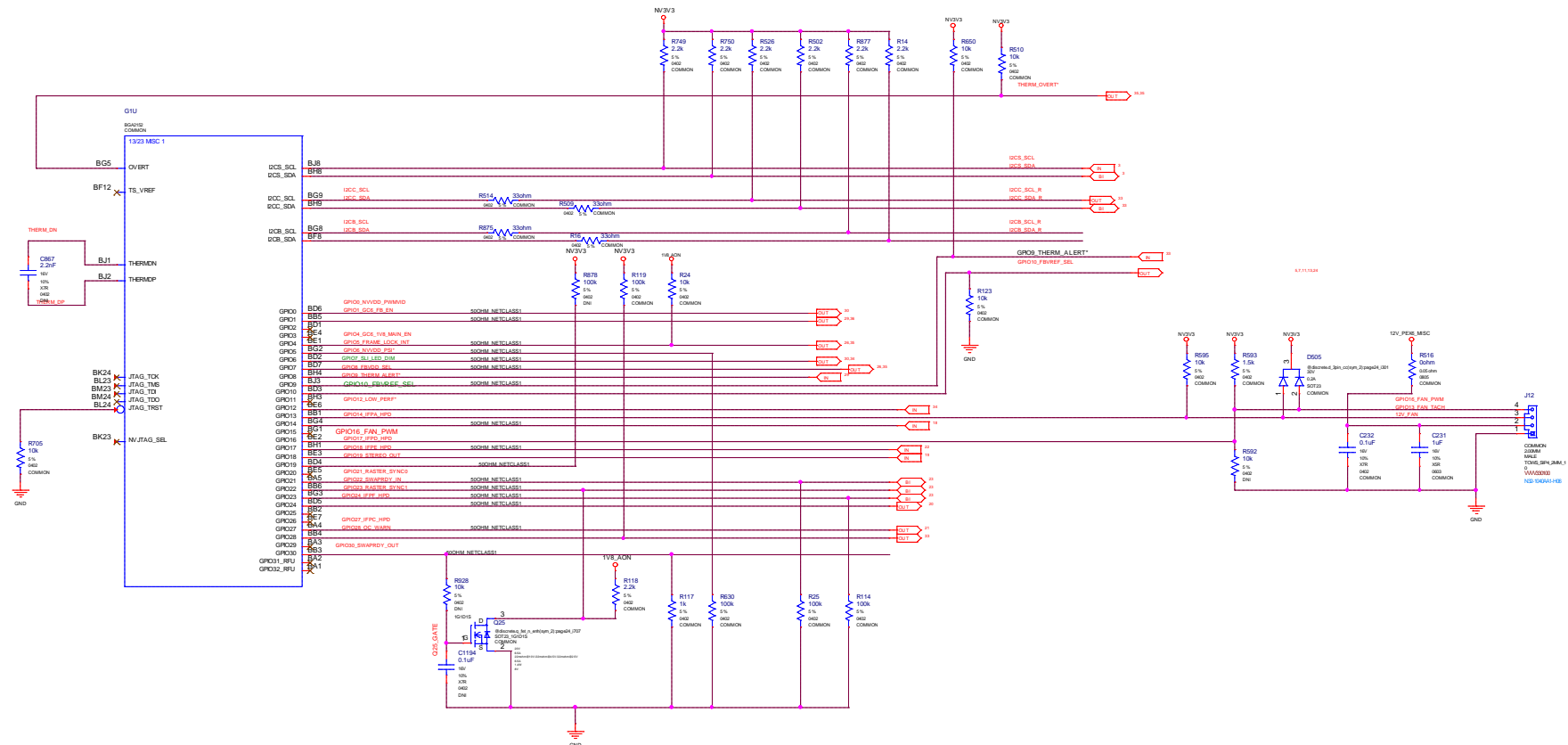


Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through







STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

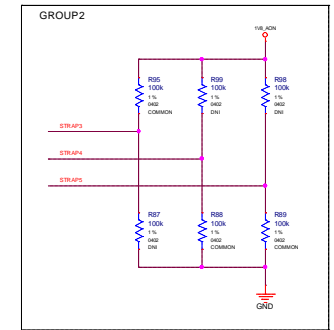
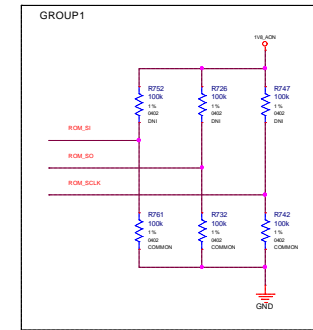
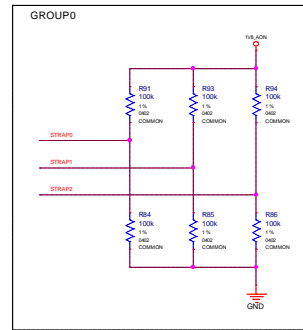
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

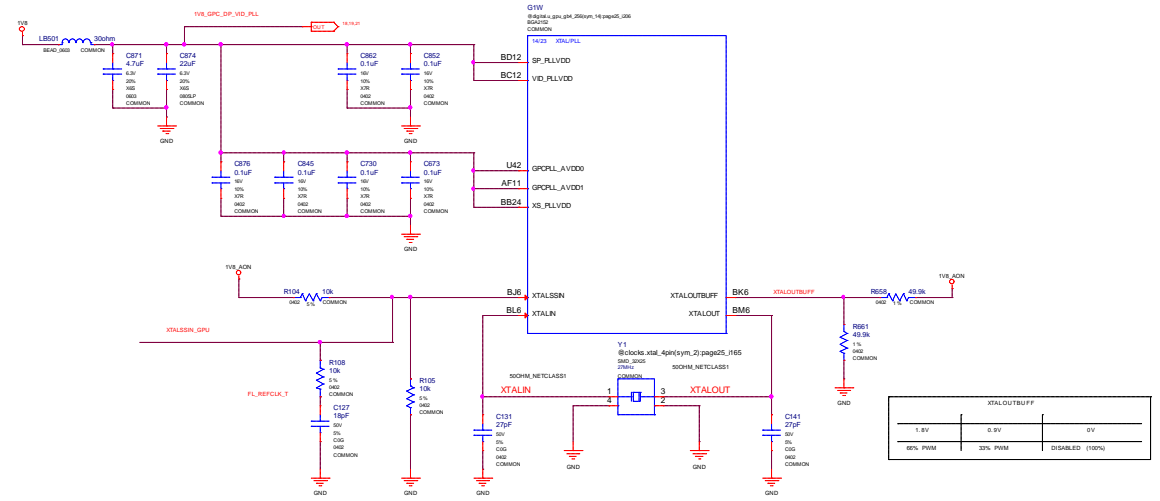
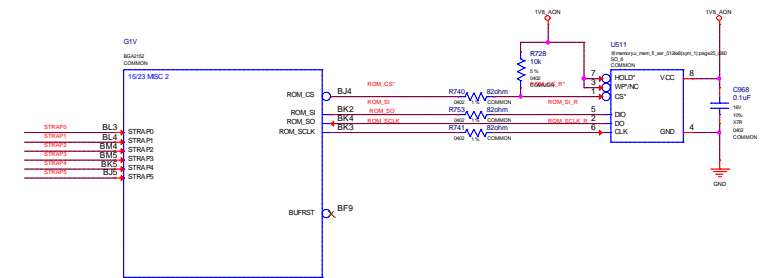
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

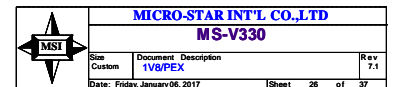
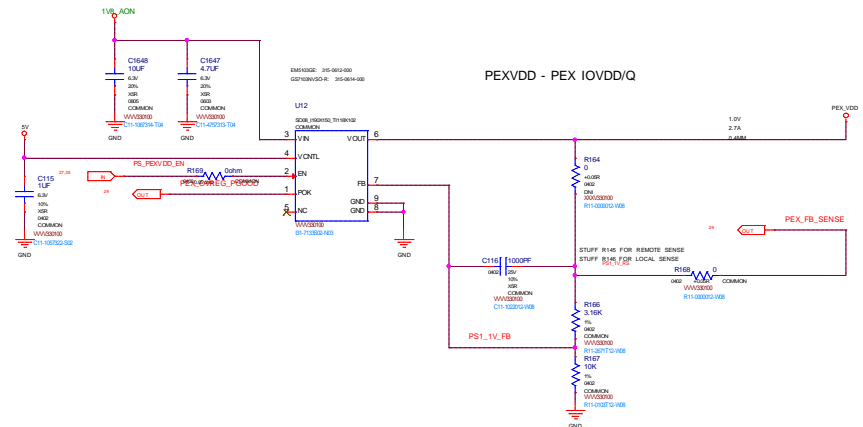
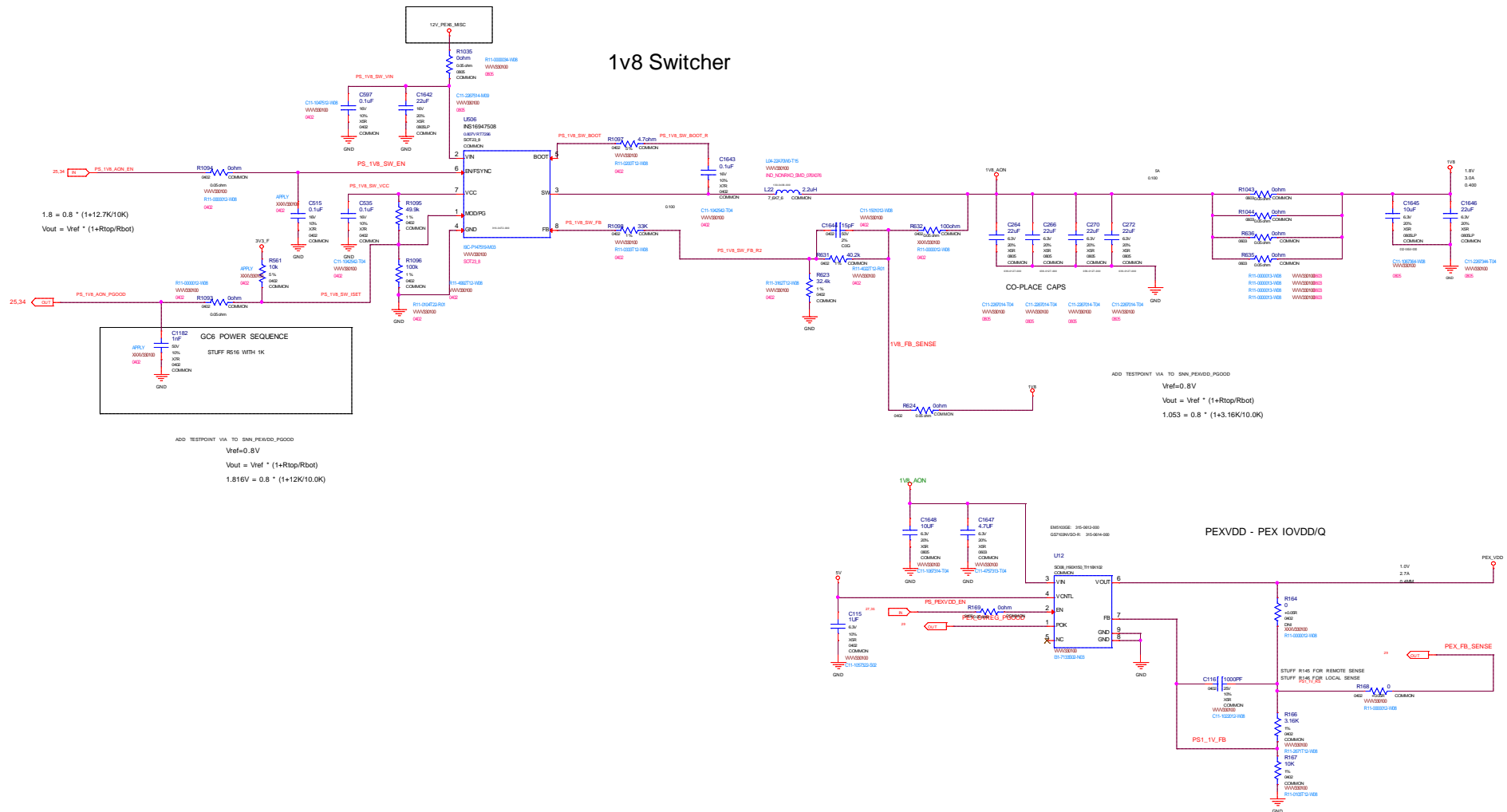
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

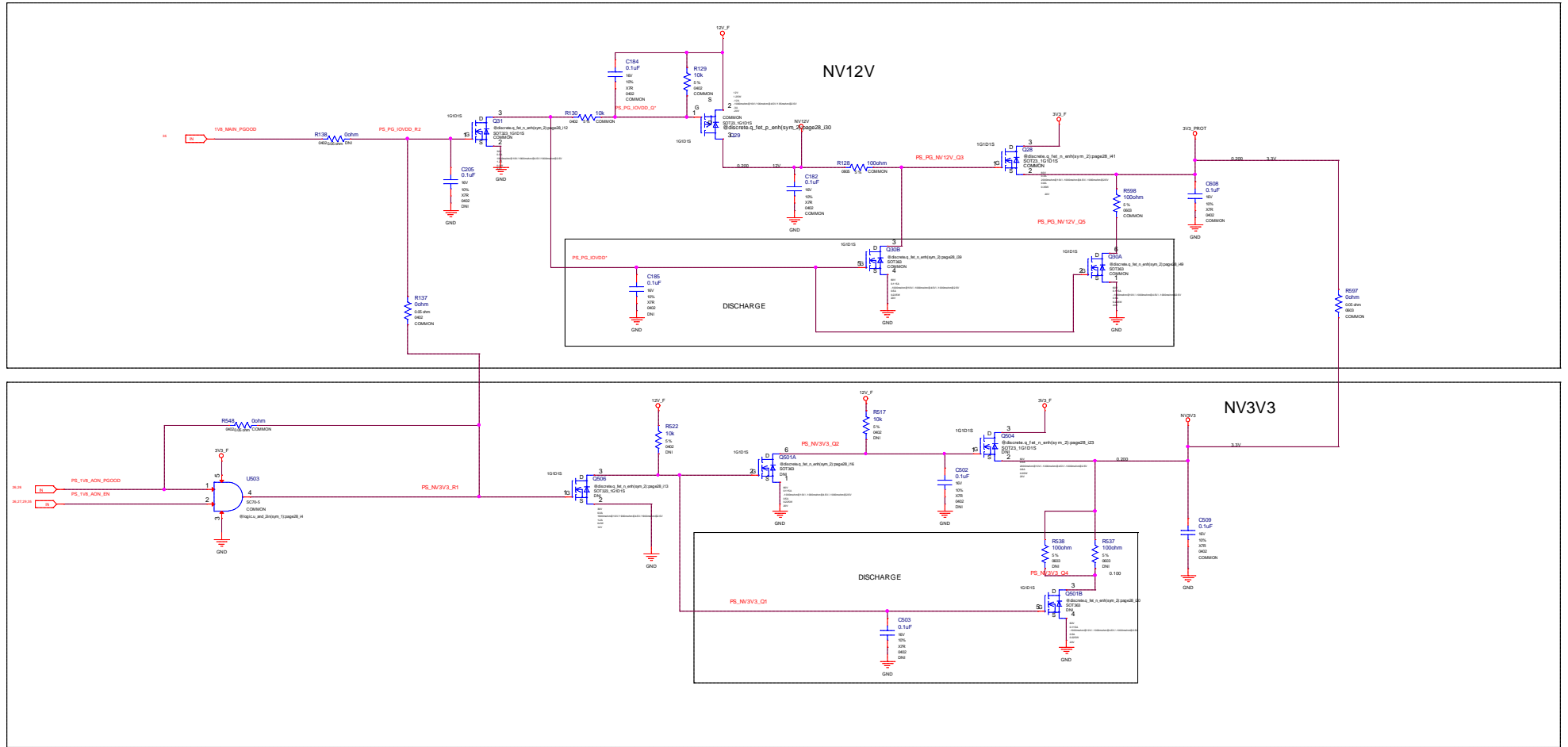


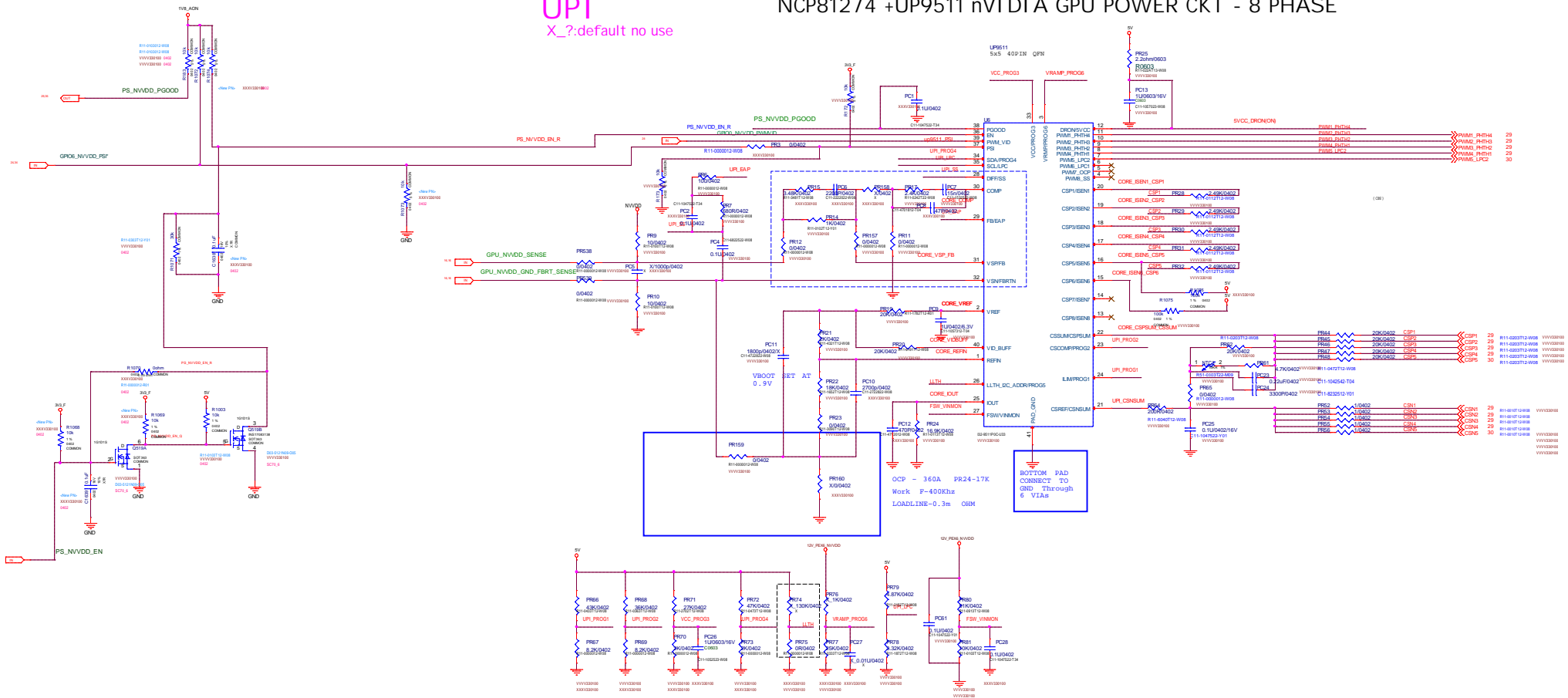
CFG(3:0)	Config	Width	Vendor
0000	256Mx32 256-bit		Samsung
0001	256Mx32 256-bit		Micron
0010	256Mx32 256-bit		Hynix
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		



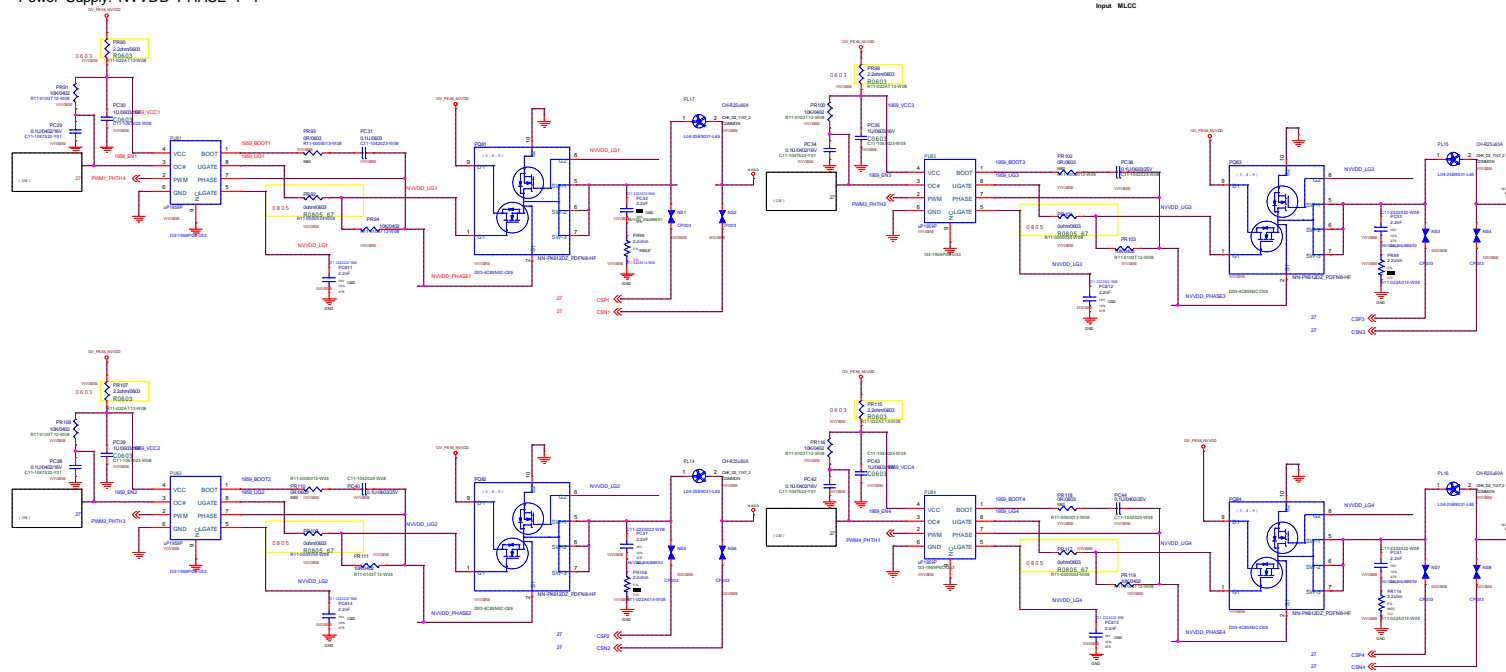
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MS-V330			
Size	Document Description	Rev	
Custom	STRAPS	7.1	
Date: Friday, January 06, 2017	Sheet: 26	of: 37	



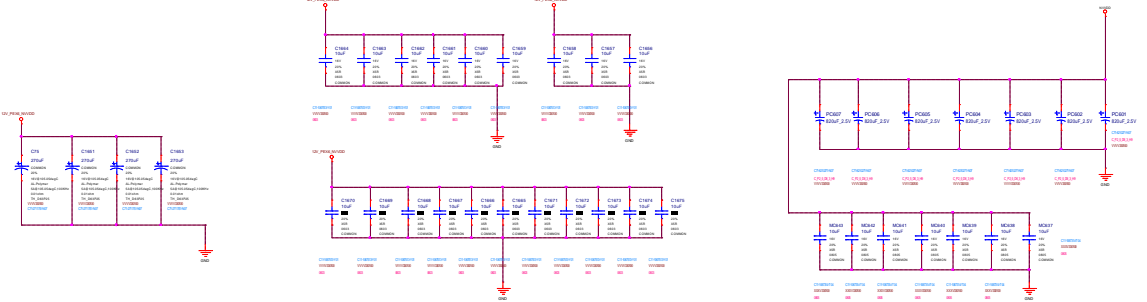


UP9511
5x5 40PIN QFN

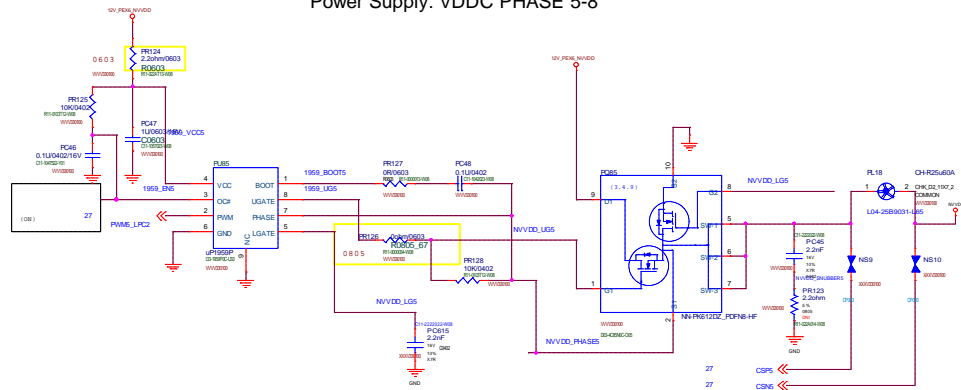
Power Supply: NVVDD PHASE 1~4

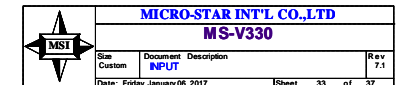
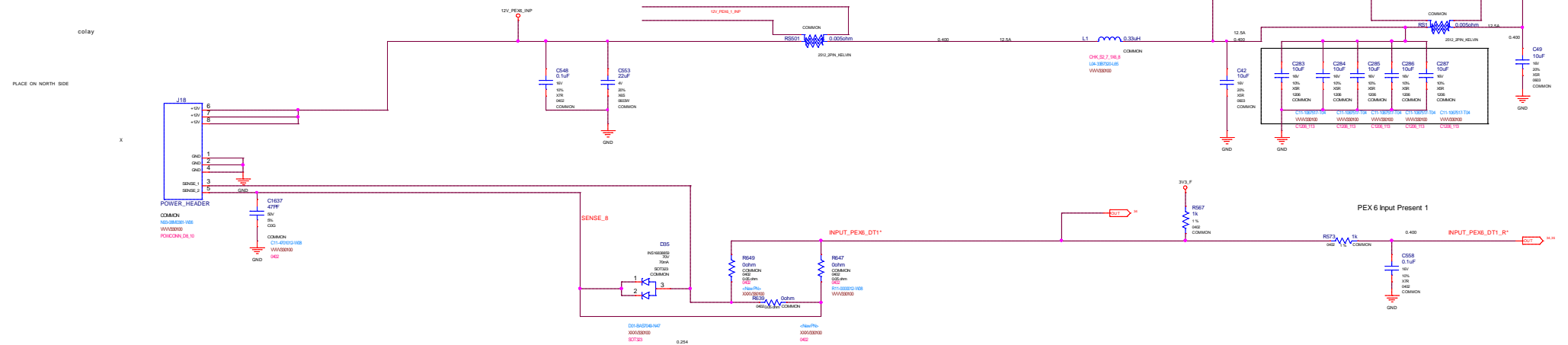
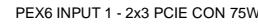
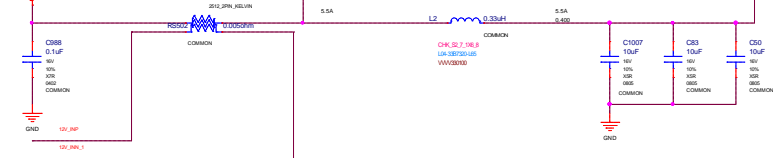
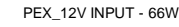
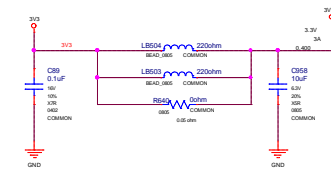
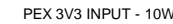
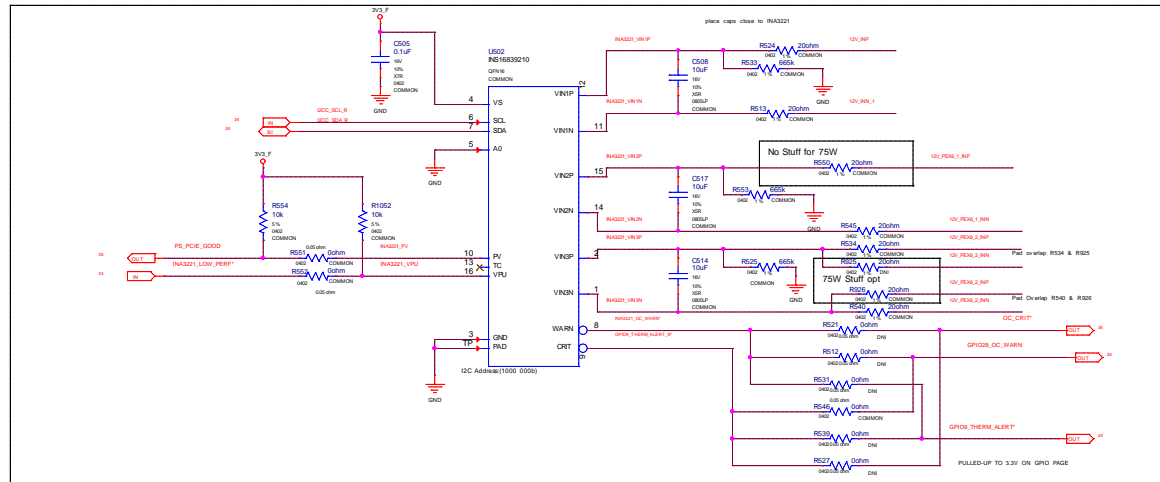


5V POWER SUPPLY FOR DRIVER VCC



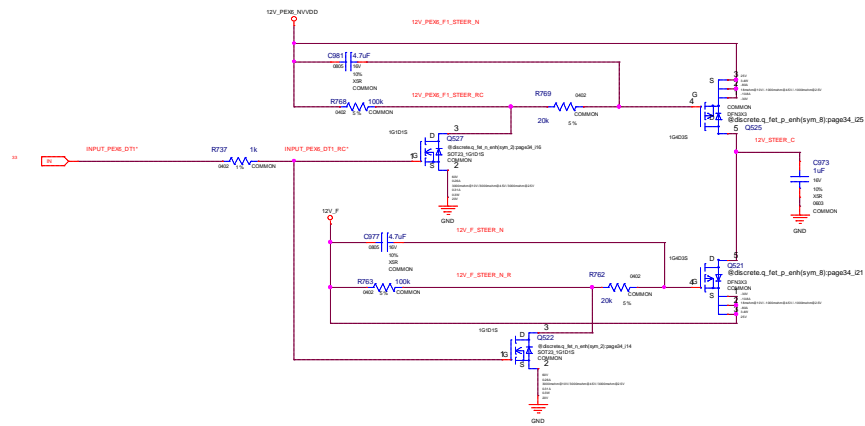
Power Supply: VDDC PHASE 5-8



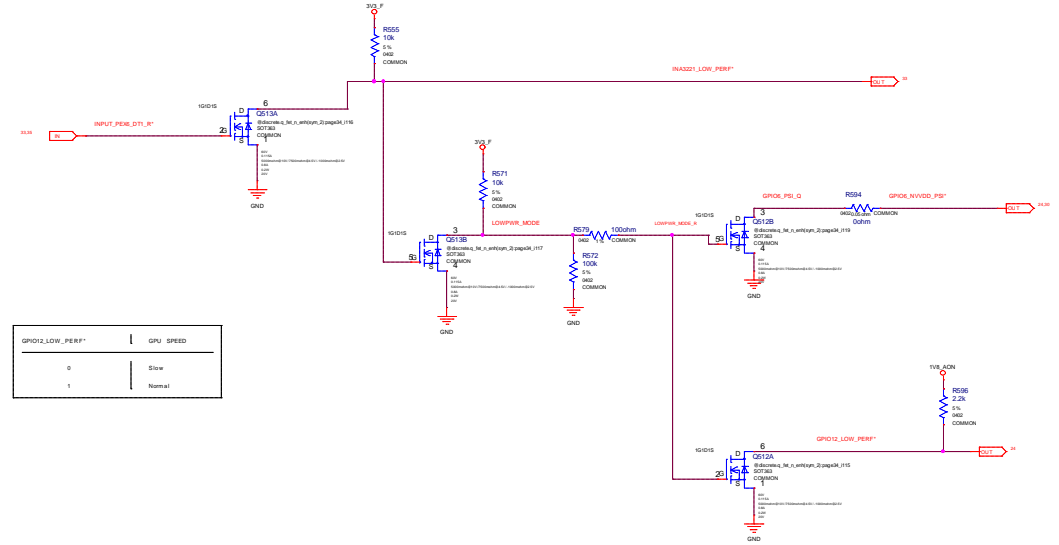


12V CURRENT STEERING (UNDER POWER BOOT):

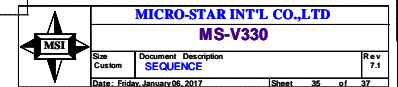
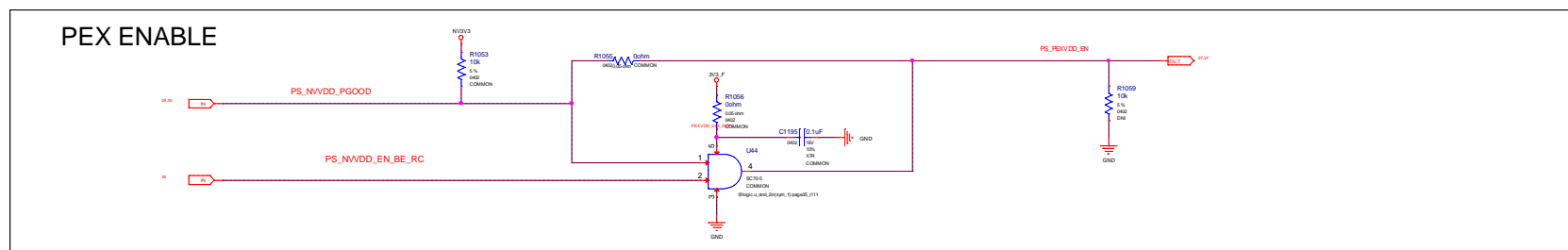
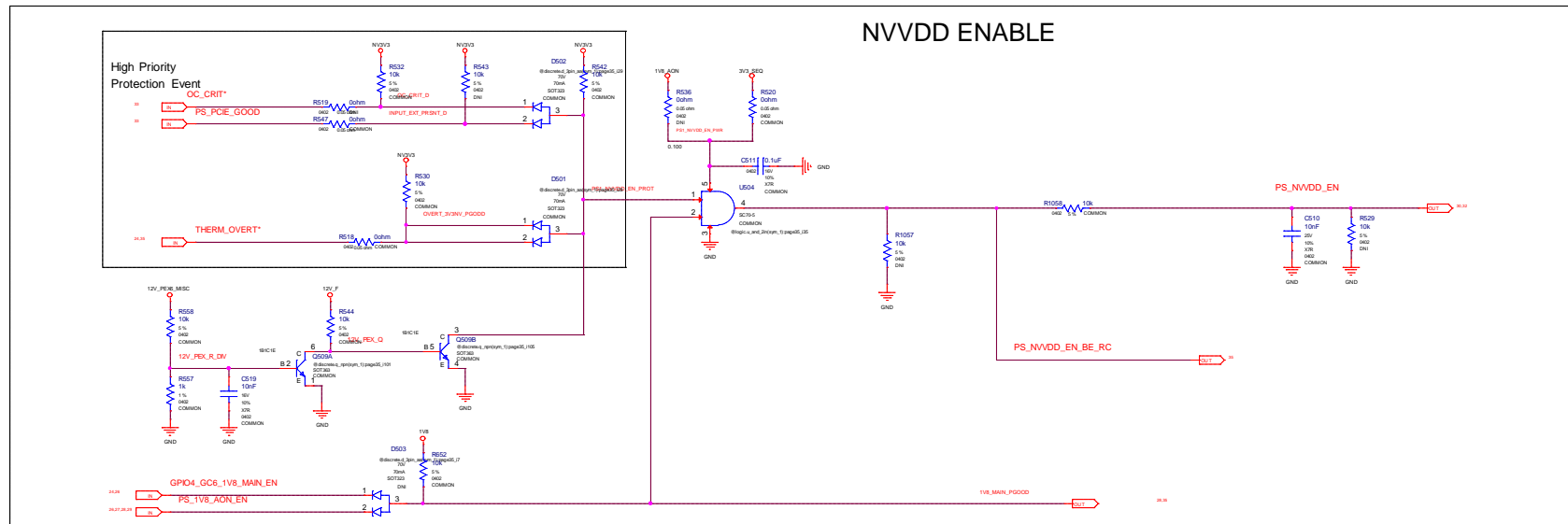
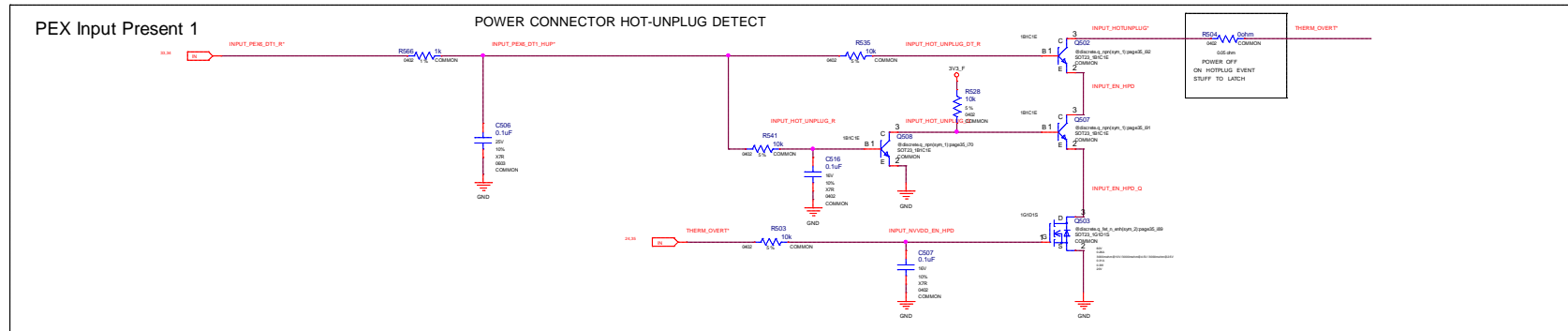
GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

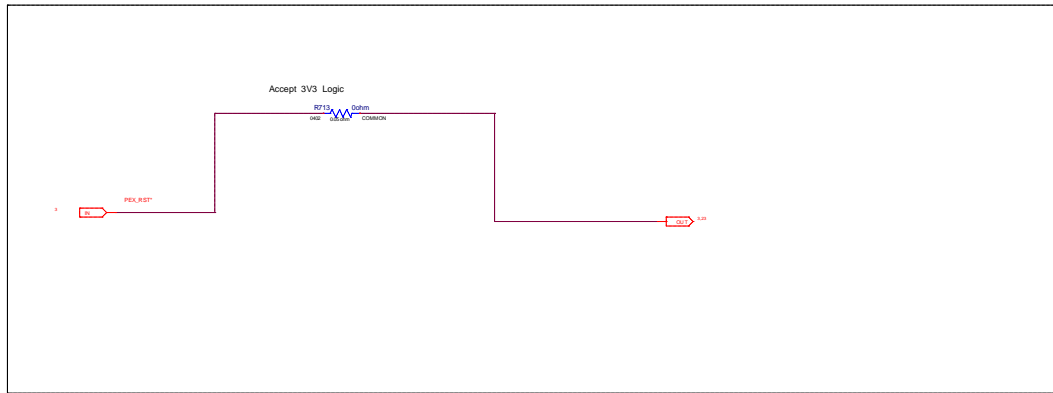


PEX Input - Power Level/PSI* Control




GeForce Logo LED





GC6 FB ENABLE
GPU_EVENT*
PEX_CLKREQ*
PEX_RST# LOGIC

	MICRO-STAR INT'L CO.,LTD		
	MS-V330		
	Size	Document	Rev
Custom	GC6	Description	7.1
Date: Friday, January 06, 2017		Sheet	38 of 37

