

PG177-A00

TU117, 128b GDDR6 2CH x16, 75W/90W
DVI-D DL + HDMI + DP

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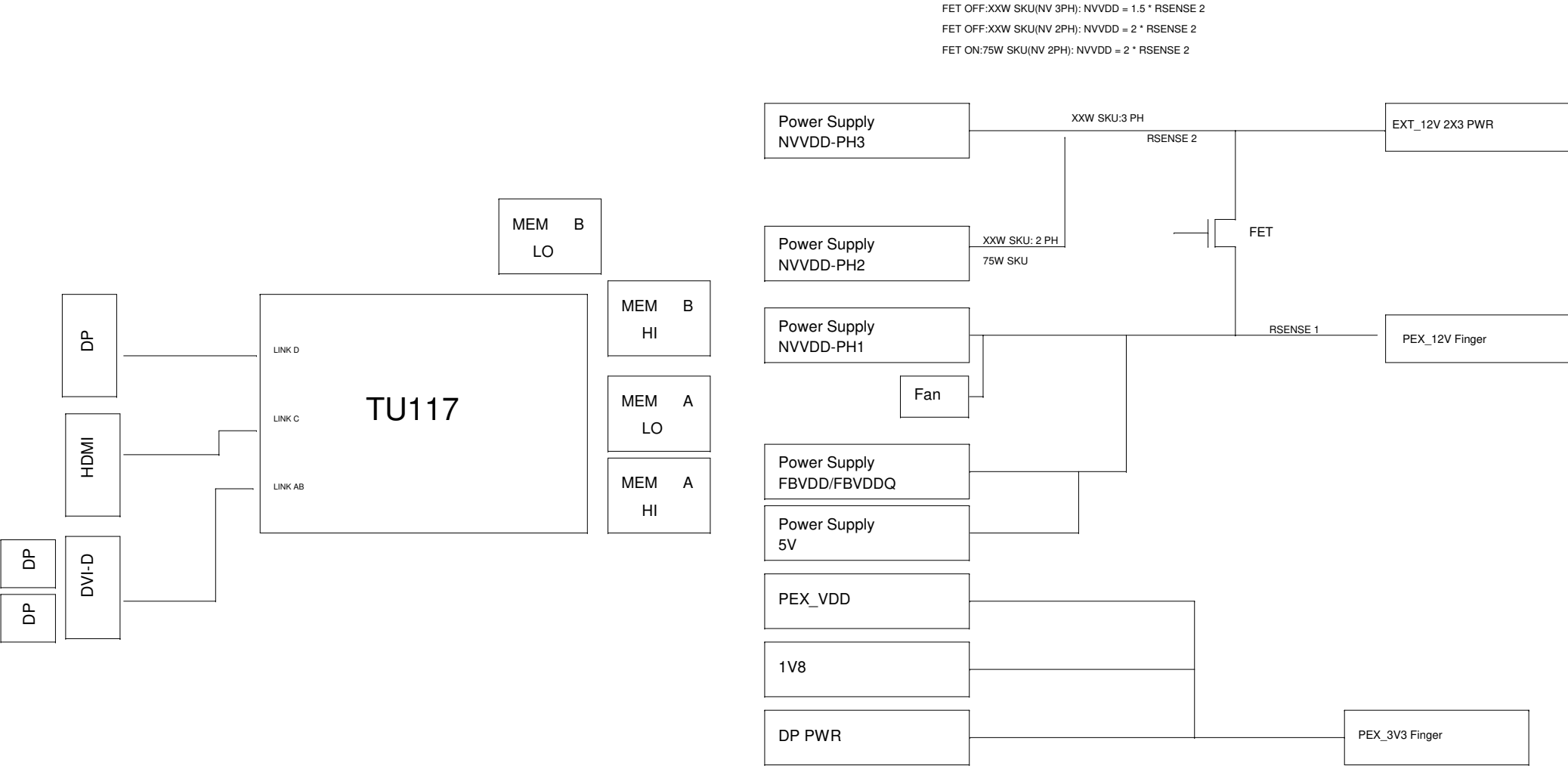


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Block Diagram



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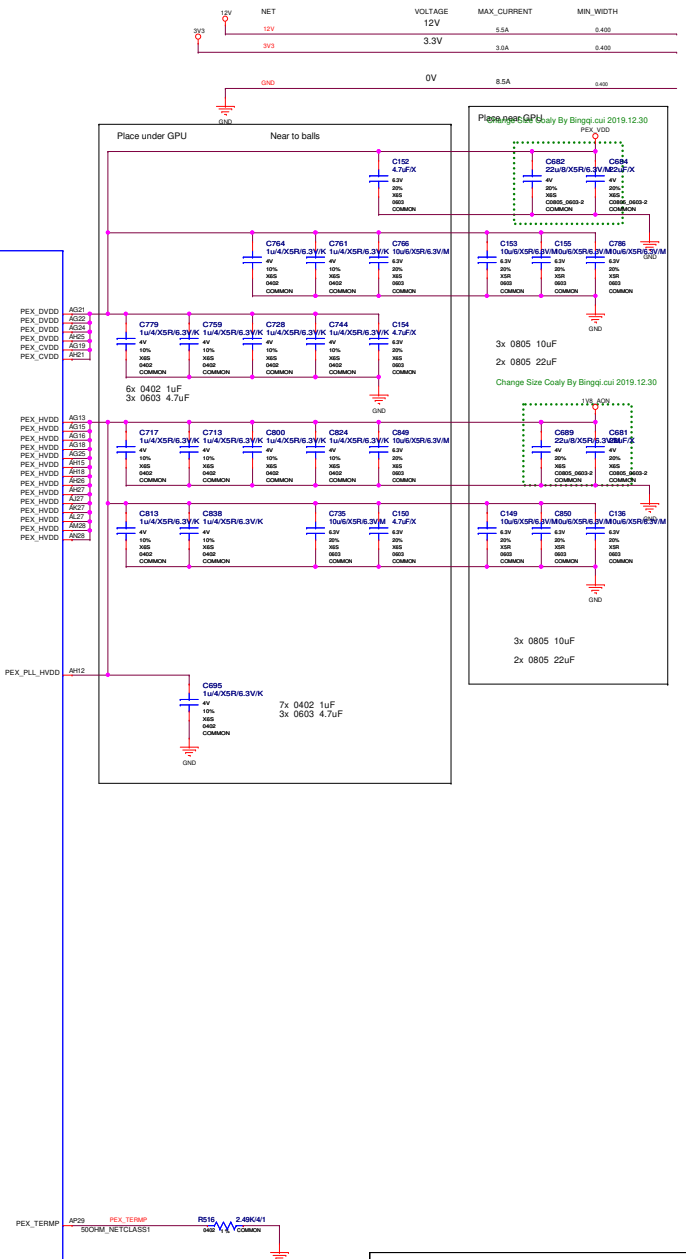
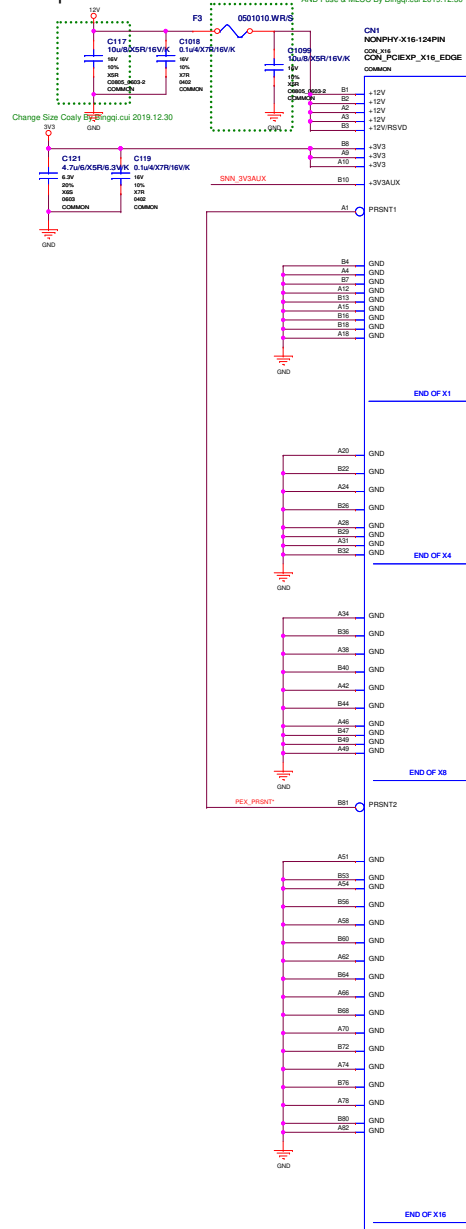
Block Diagram

GIGABYTE™

Block Diagram

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PCI Express

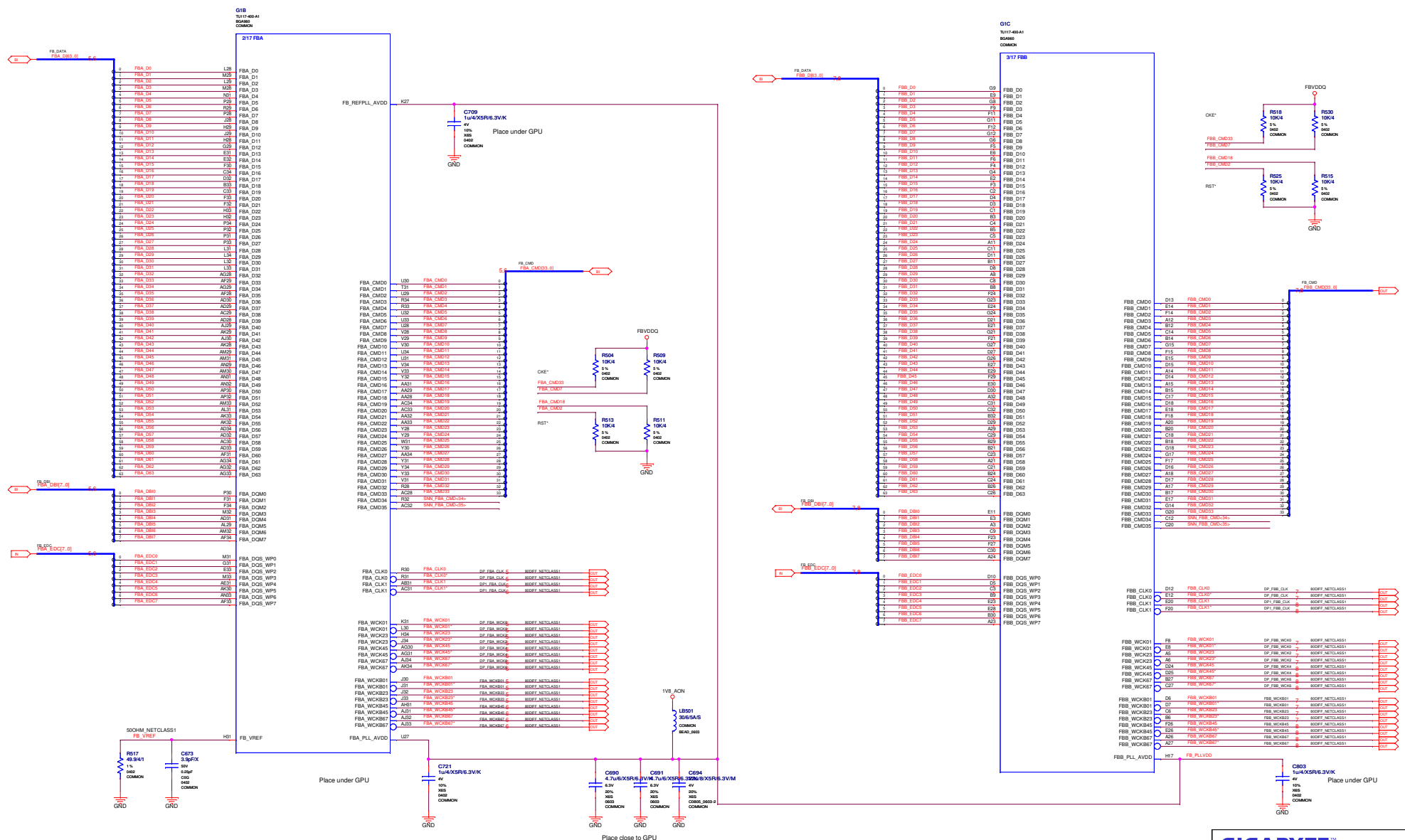


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 STANDARDS.

MEMORY: GPU Partition A/B

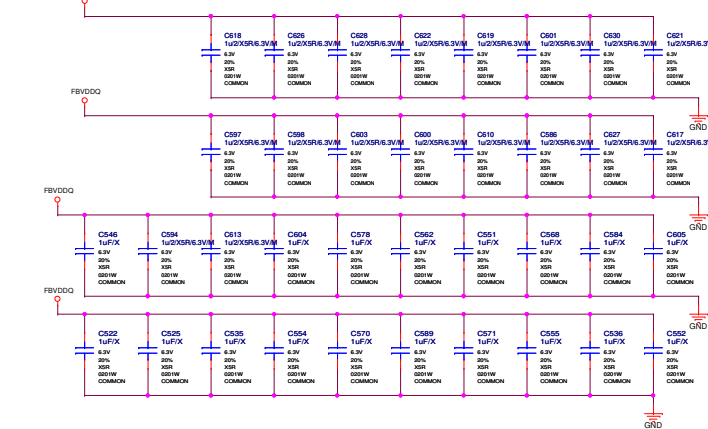
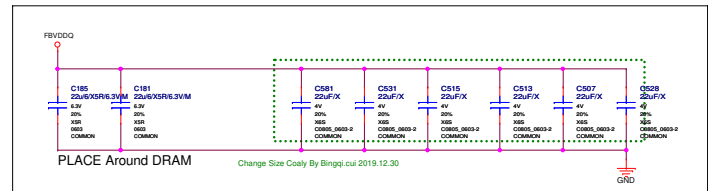
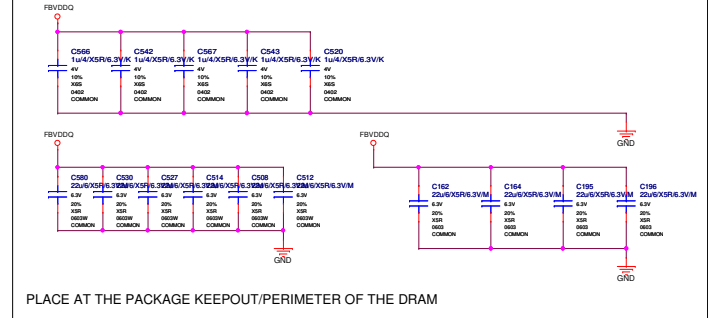
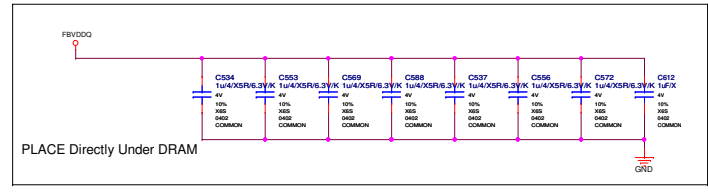
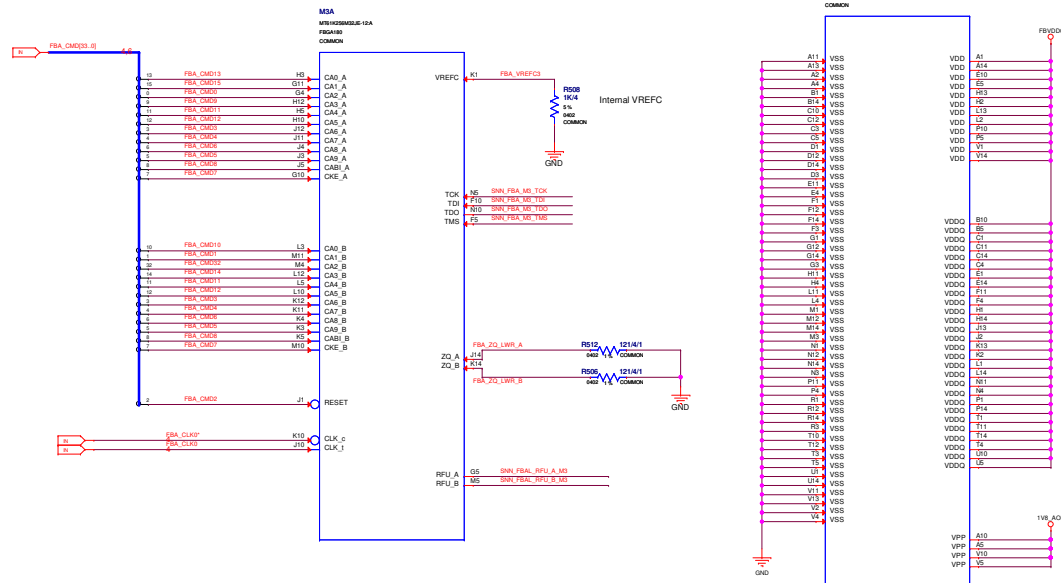


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MEMORY: FBA Partition 31..0

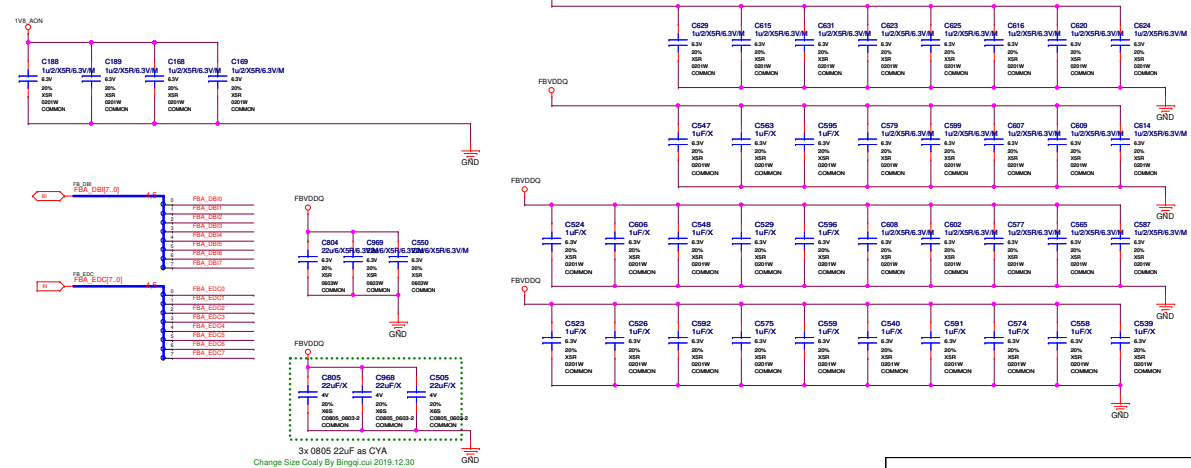
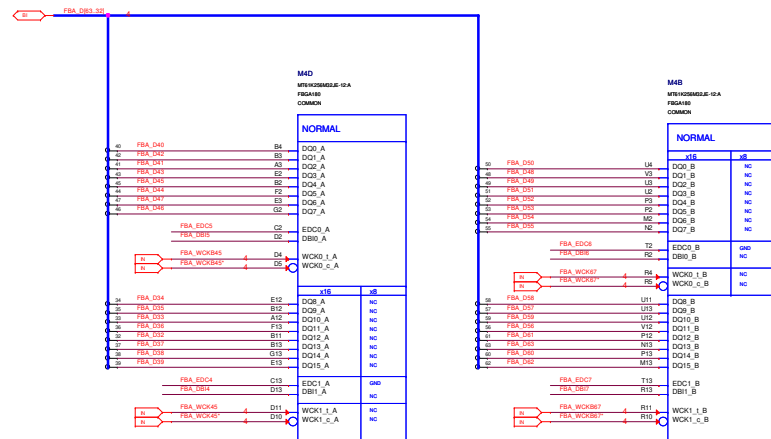
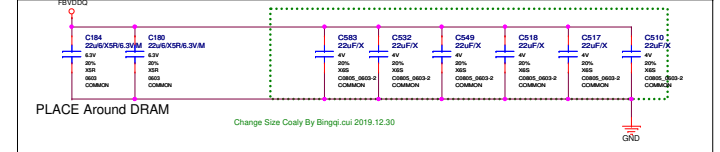
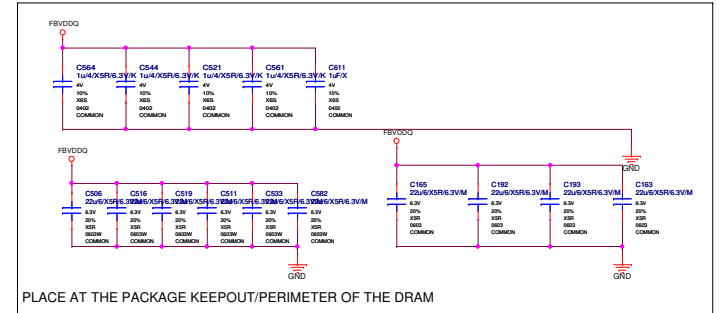
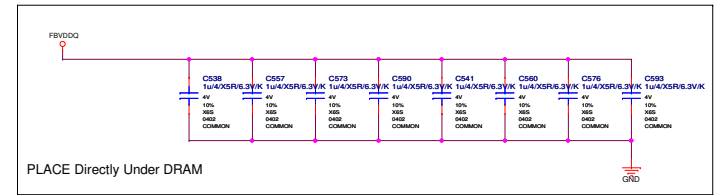
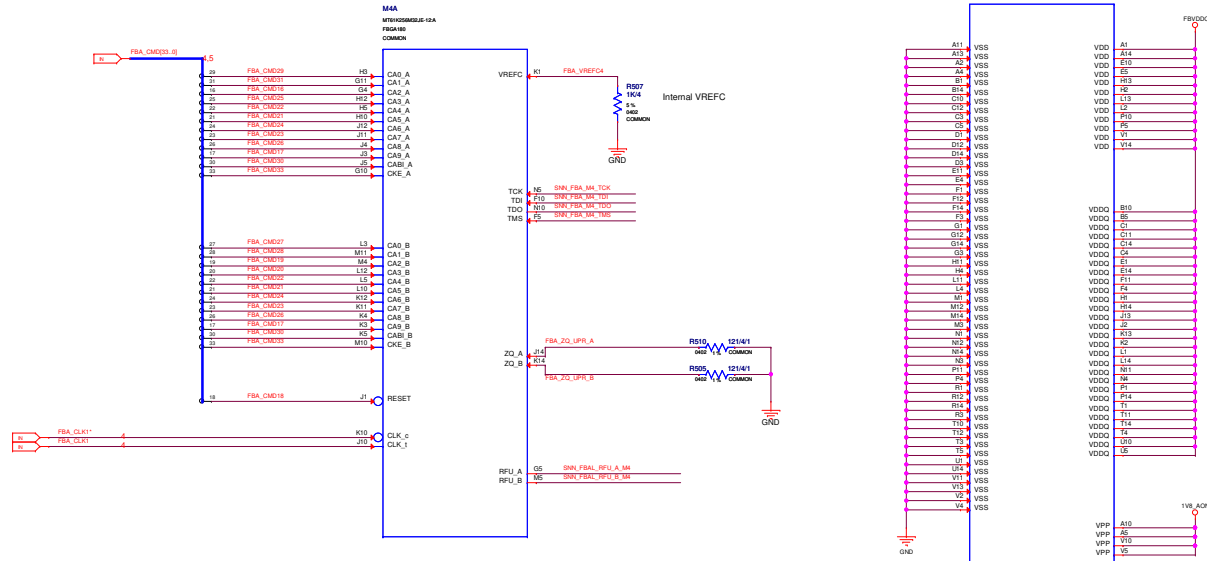


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FBA Partition 31..0

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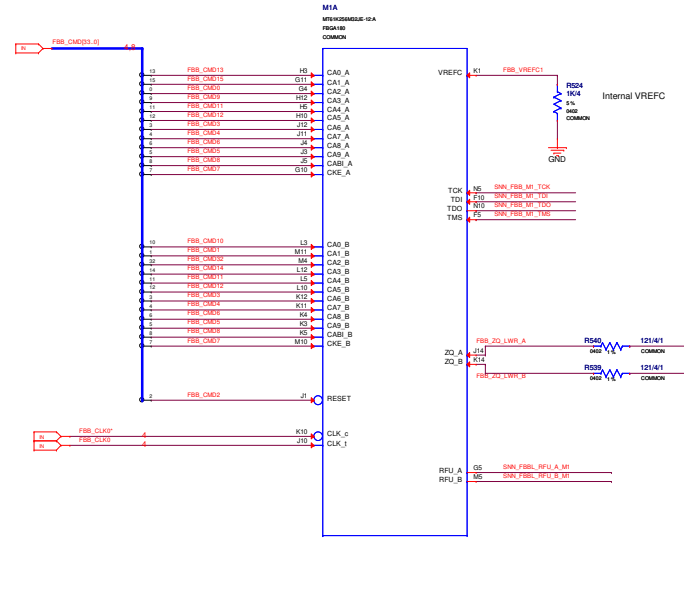
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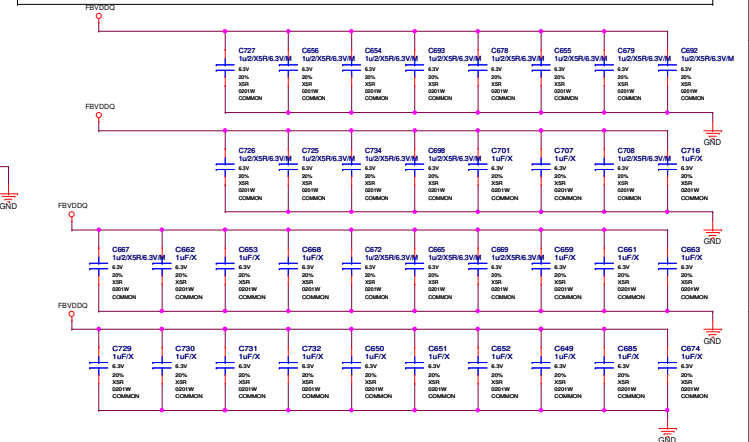
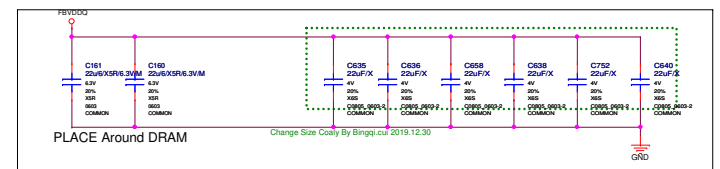
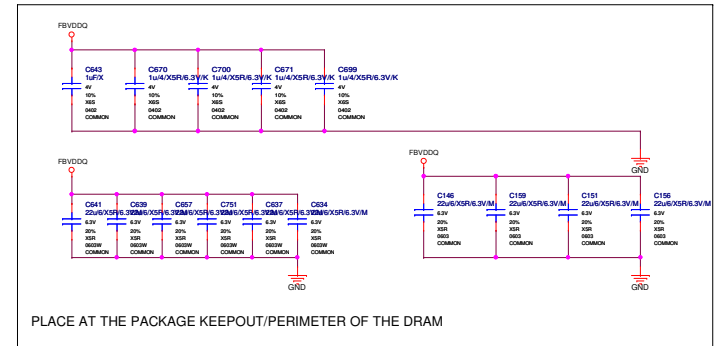
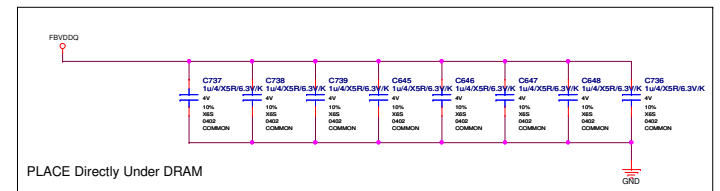
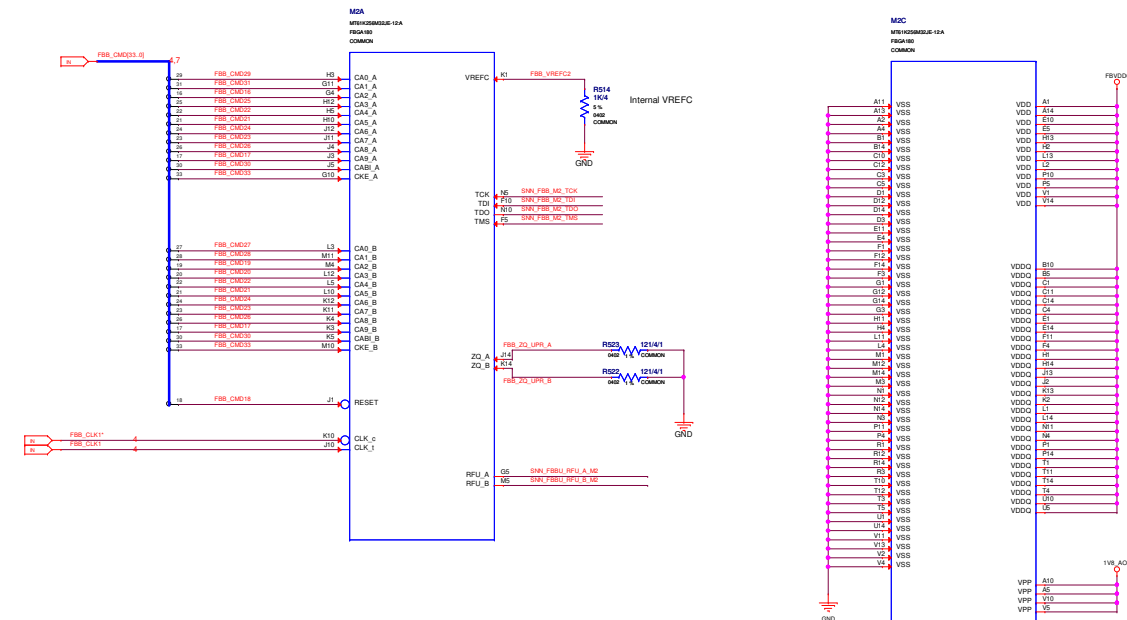
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MEMORY: FBB Partition 31..0



MEMORY: FBB Partition 63..32



MZD
FPGA480
COMMON

NORMAL

42	FBB D42	B4	DQ6_A	
43	FBB D43	A3	DQ1_A	
44	FBB D24	B3	DQ2_A	
45	FBB D45	B2	DQ3_A	
46	FBB D44	A3	DQ4_A	
47	FBB D25	F2	DQ5_A	
48	FBB D46	D2	DQ6_A	
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FBB ED05 C2 ED05_A
FBB DB07 C2 DB05_A

FBB WK04B D24 WK02_I_A
FBB WK04D D25 WK02_O_A

MZB
FPGA480
COMMON

NORMAL

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MZD
FPGA480
COMMON

ALL

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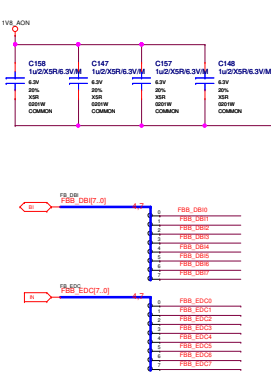
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FPGA480
COMMON

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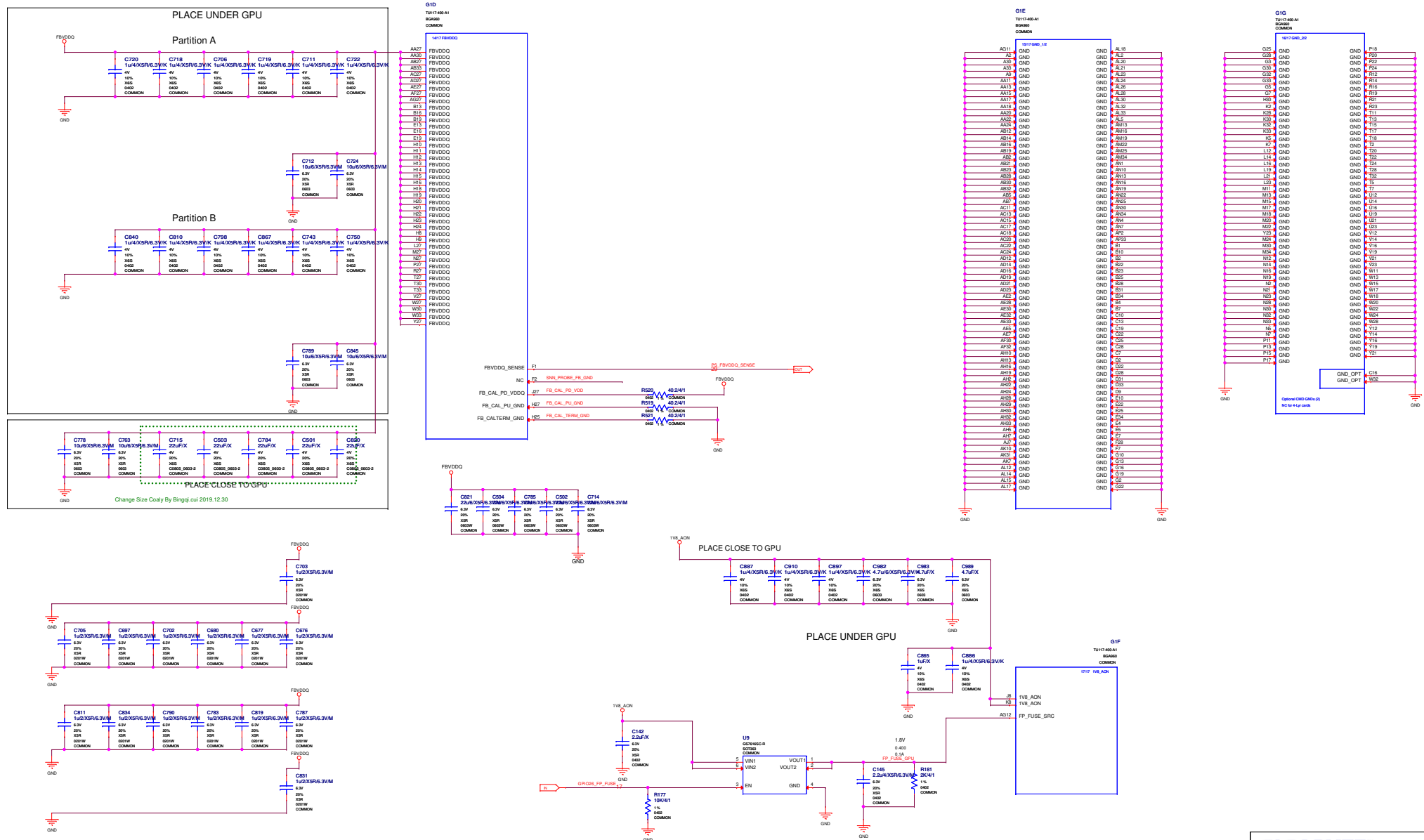
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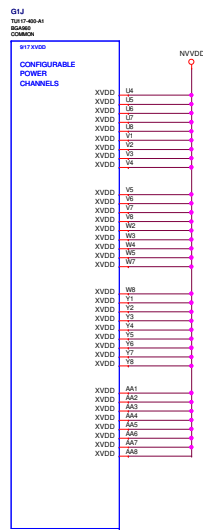
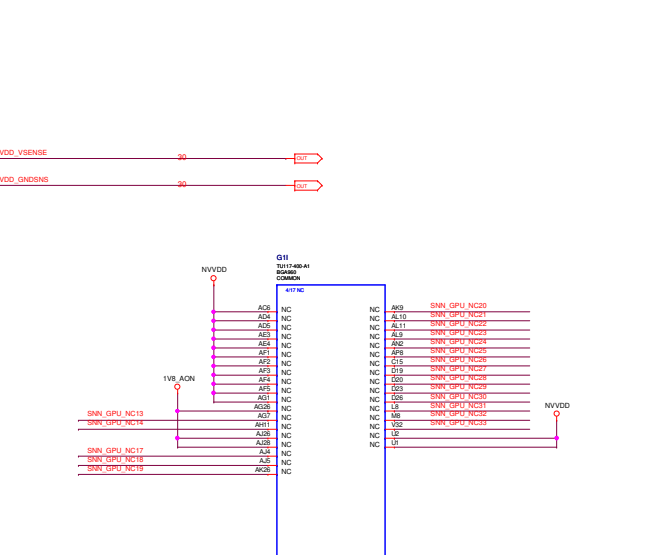
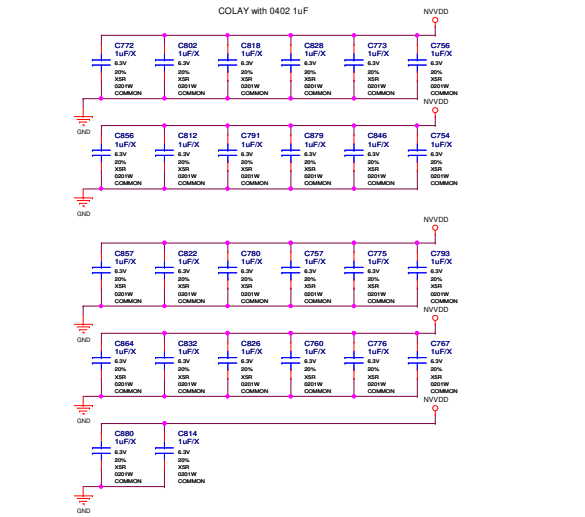
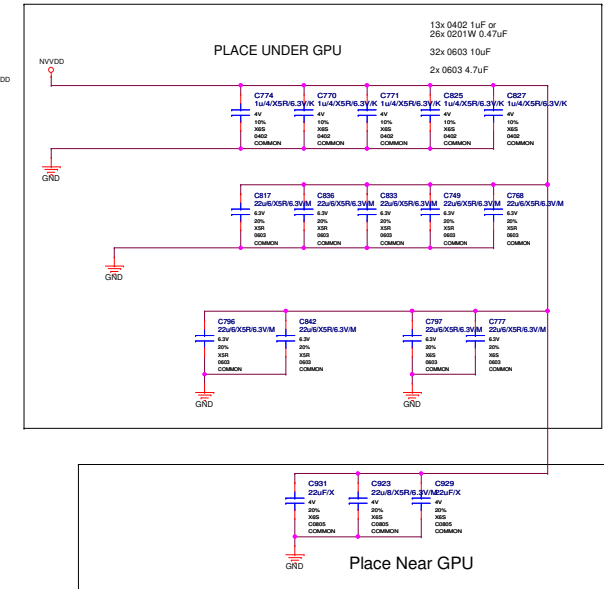
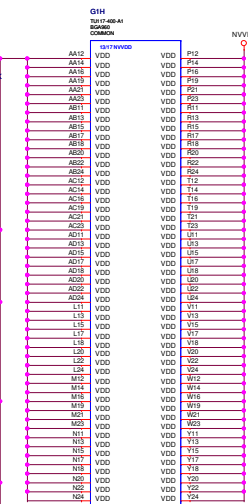
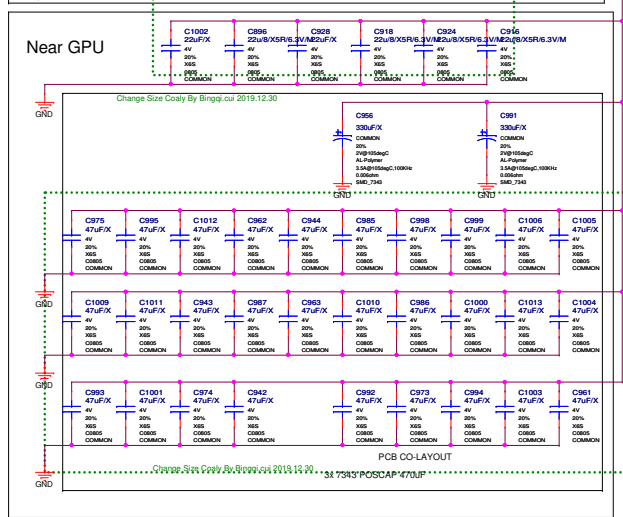
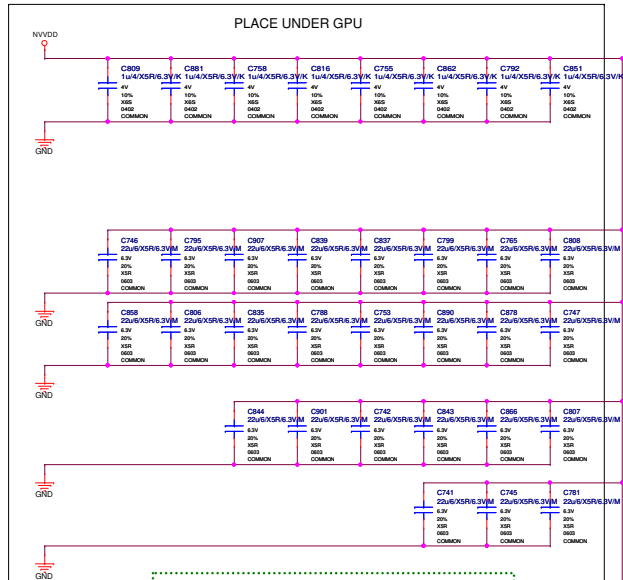
GPU FBVDDQ & 1V8 Decoupling



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GPU NVVDD Decoupling



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GPU NVVDD Decoupling

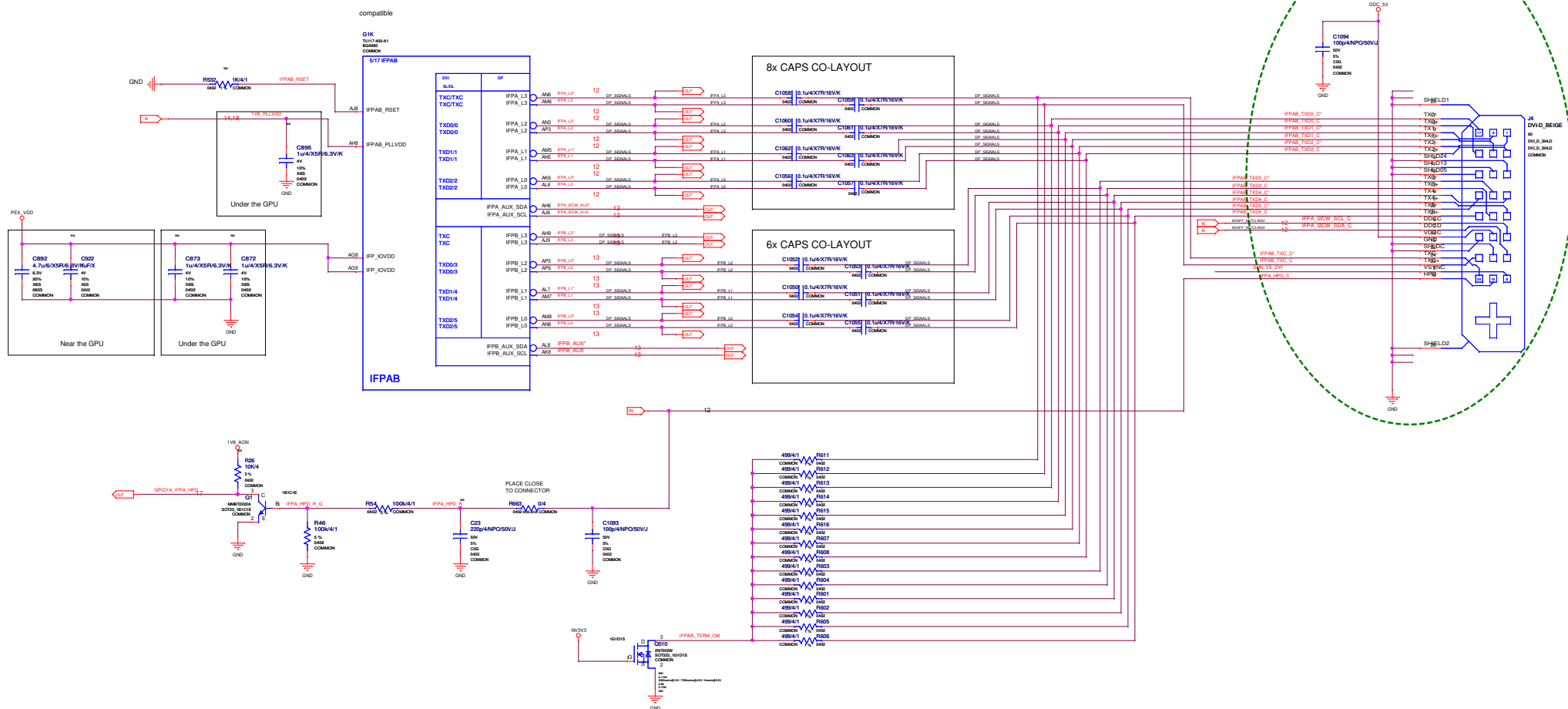
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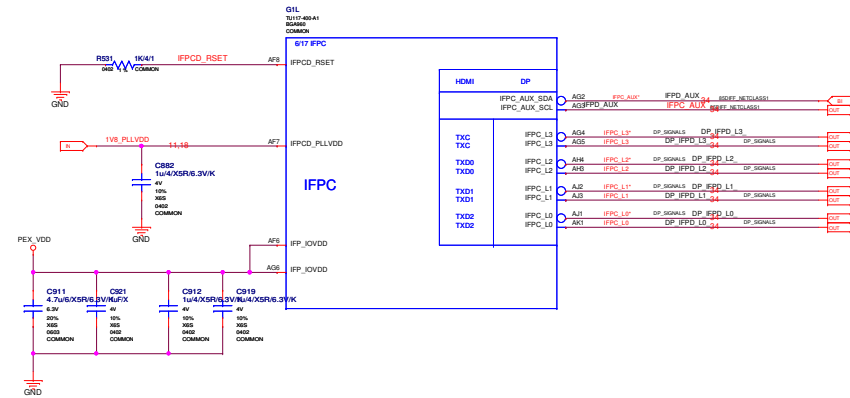
IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



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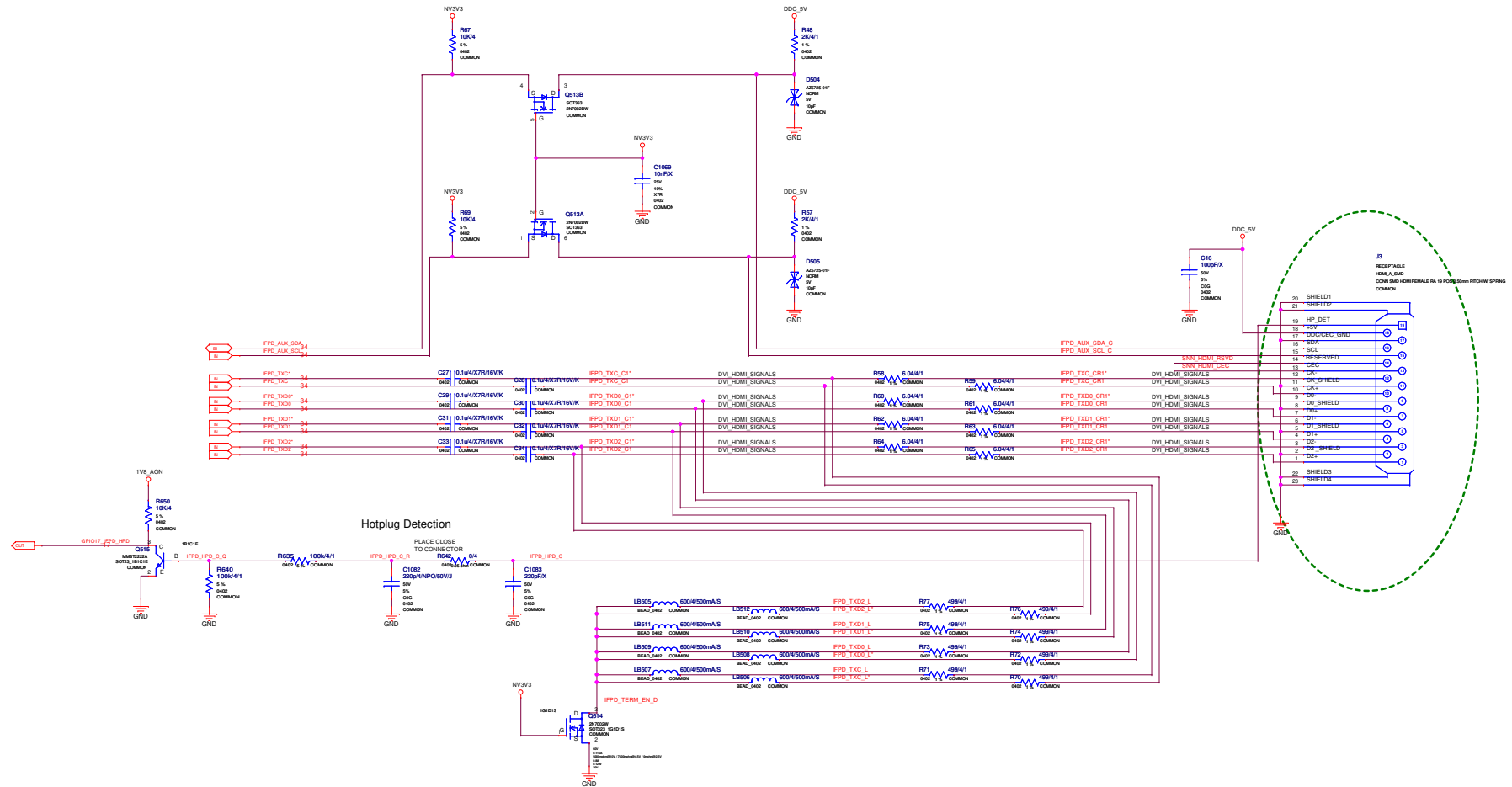


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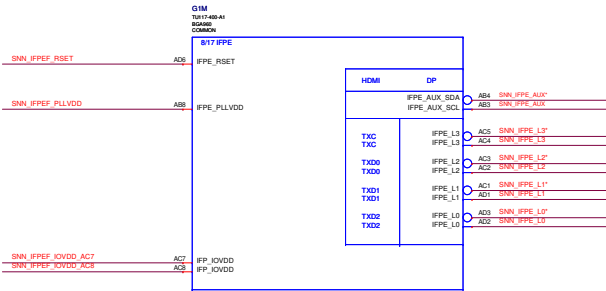
IFPC HDMI



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IFPDEF UNUSED



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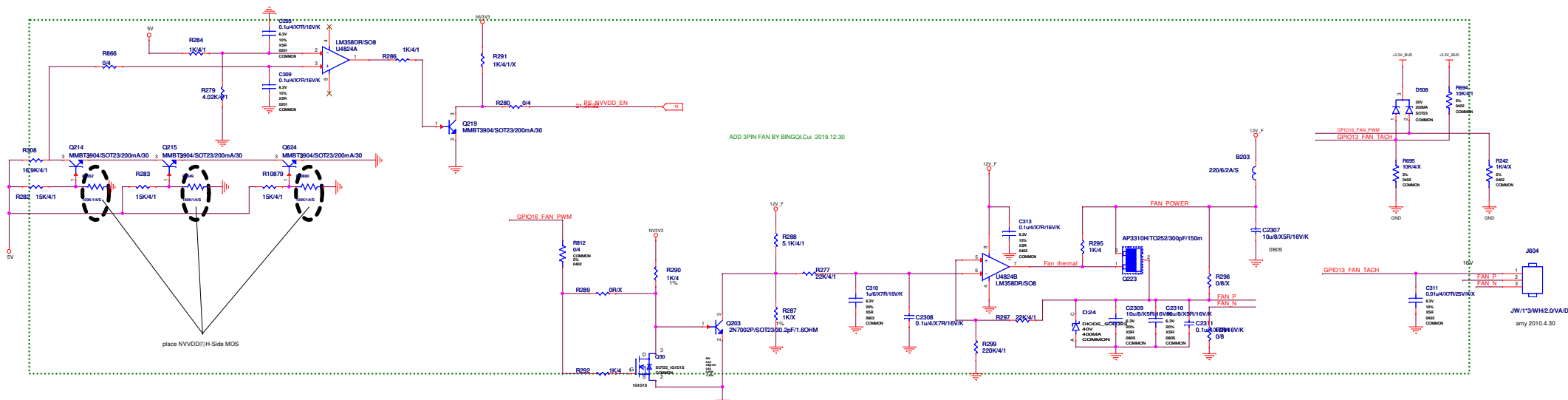
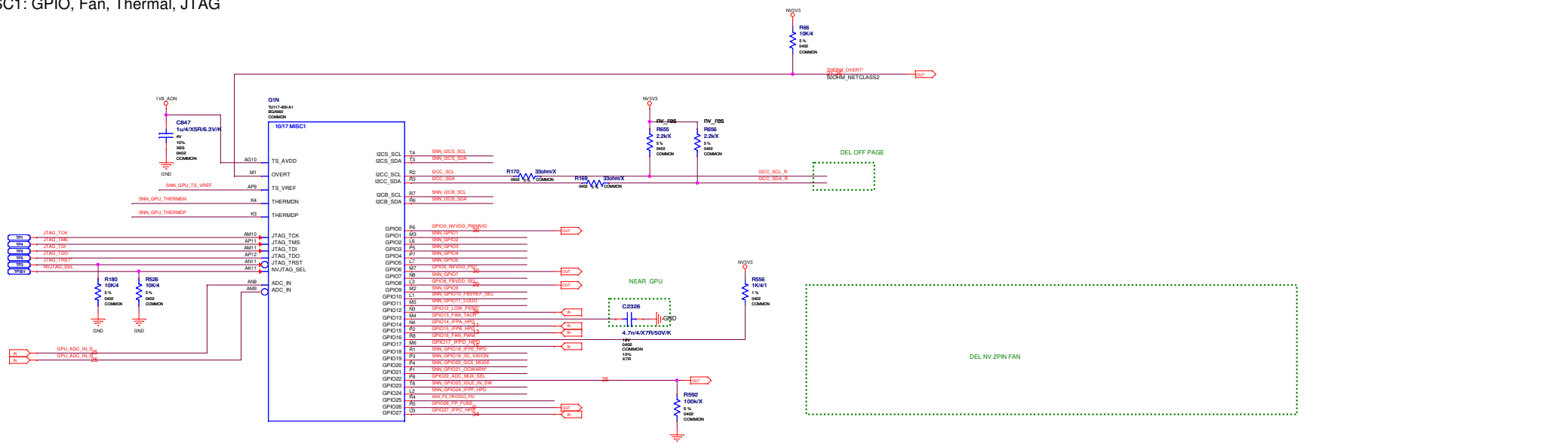
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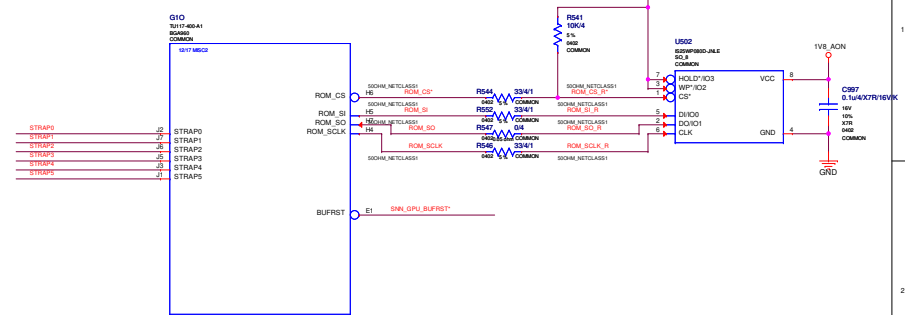
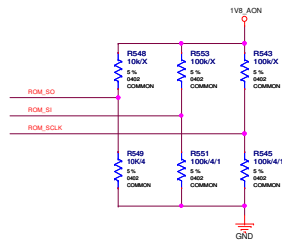
MISC1: GPIO, Fan, Thermal, JTAG



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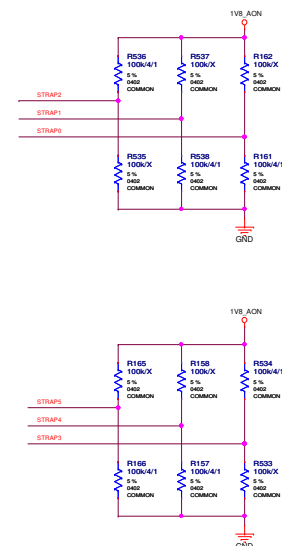
MISC2: ROM, XTAL, Straps

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]_FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	xxx1	FS_OVERT ENABLE	Default
L	L	M	xxx0	FS_OVERT DISABLE	



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung 8Gb 7GHz K4Z80325BC-HC14
L	L	H	0001	Micron 8Gb 7GHz MT61K256M32JE-14:A
L	H	L	0010	Hynix 8Gb 7GHz H56C8H24MJR-S2C
L	H	H	0011	Samsung 8Gb 6GHz K4Z80325BC-HC12
H	L	L	0100	Micron 8Gb 6GHz MT61K256M32JE-12:A
H	L	H	0101	Hynix 8Gb 6GHz H56C8H24MJR-S0C
H	H	L	0110	Samsung 16Gb K4ZAF325BM-HC14
H	H	H	0111	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V



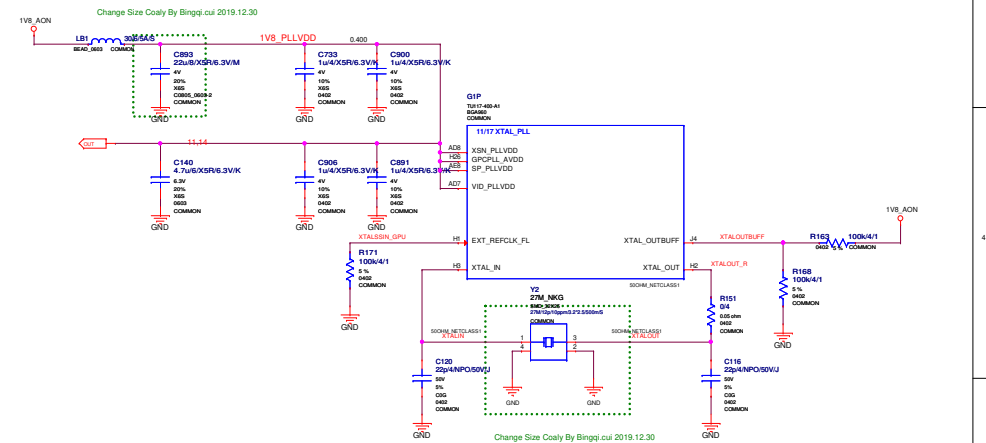
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1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
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L	L	M	1	0	0	0
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H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
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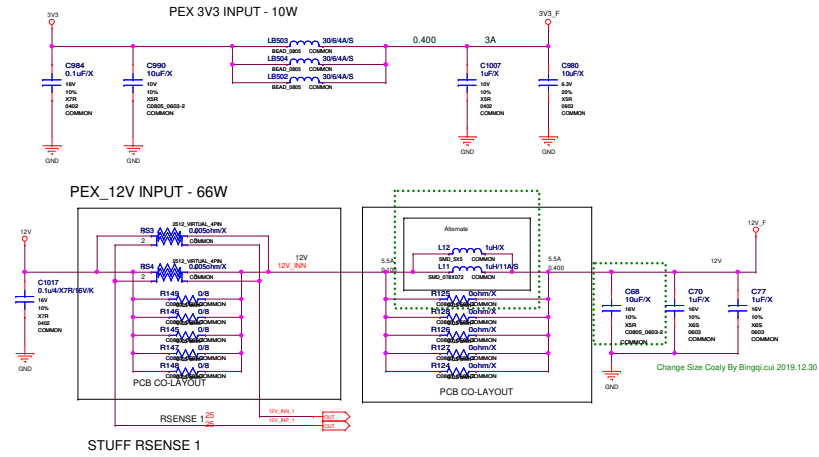
XTALOUTBUFF	Voltage	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM

ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	MISC2: ROM, XTAL, Straps

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GIGABYTE™			
ROM, XTAL, Straps			
Size	Document Number	Rev	
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Power Inputs and Filtering

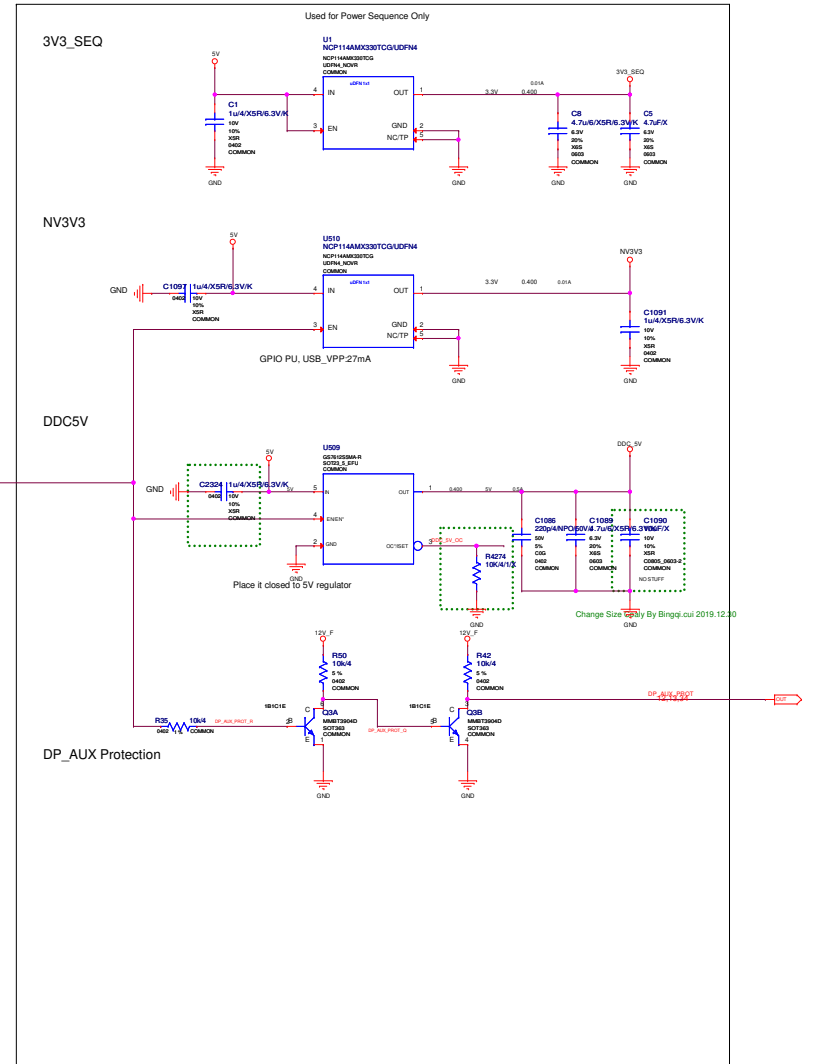
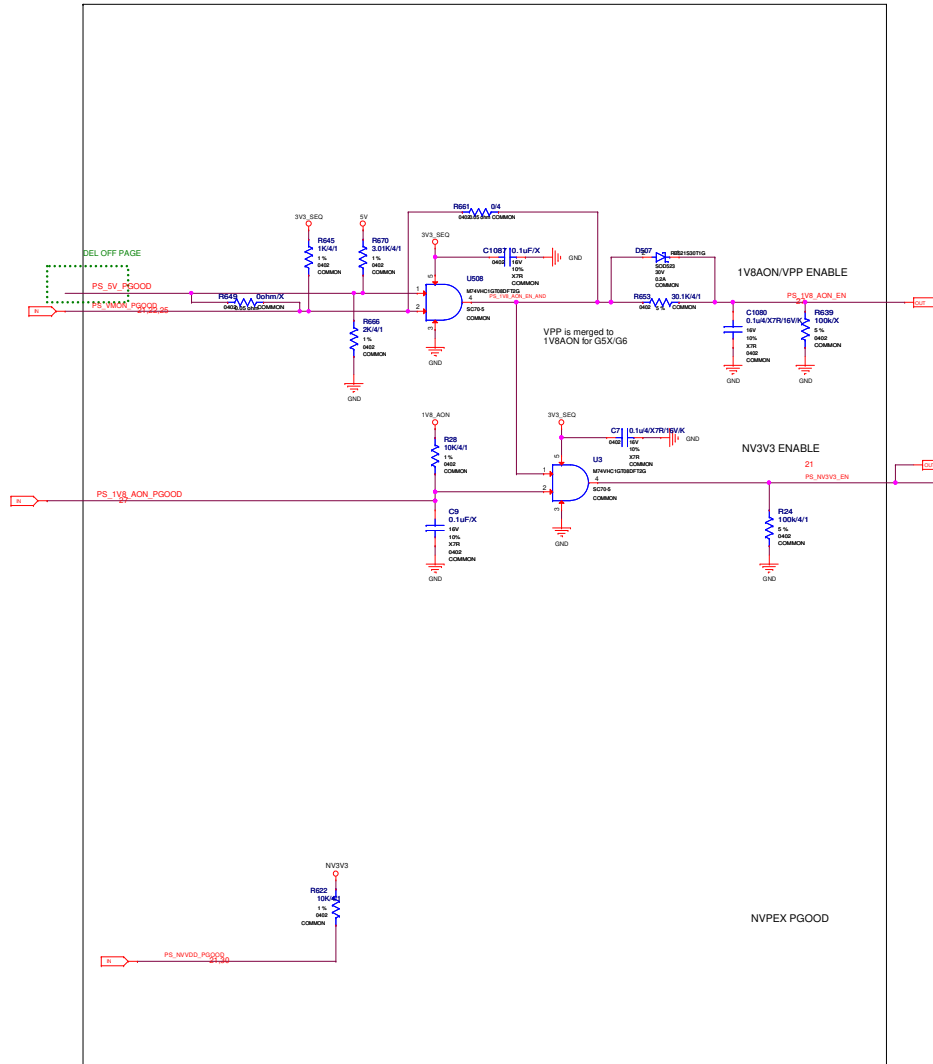


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PAGE DETAIL	Power Inputs and Filtering

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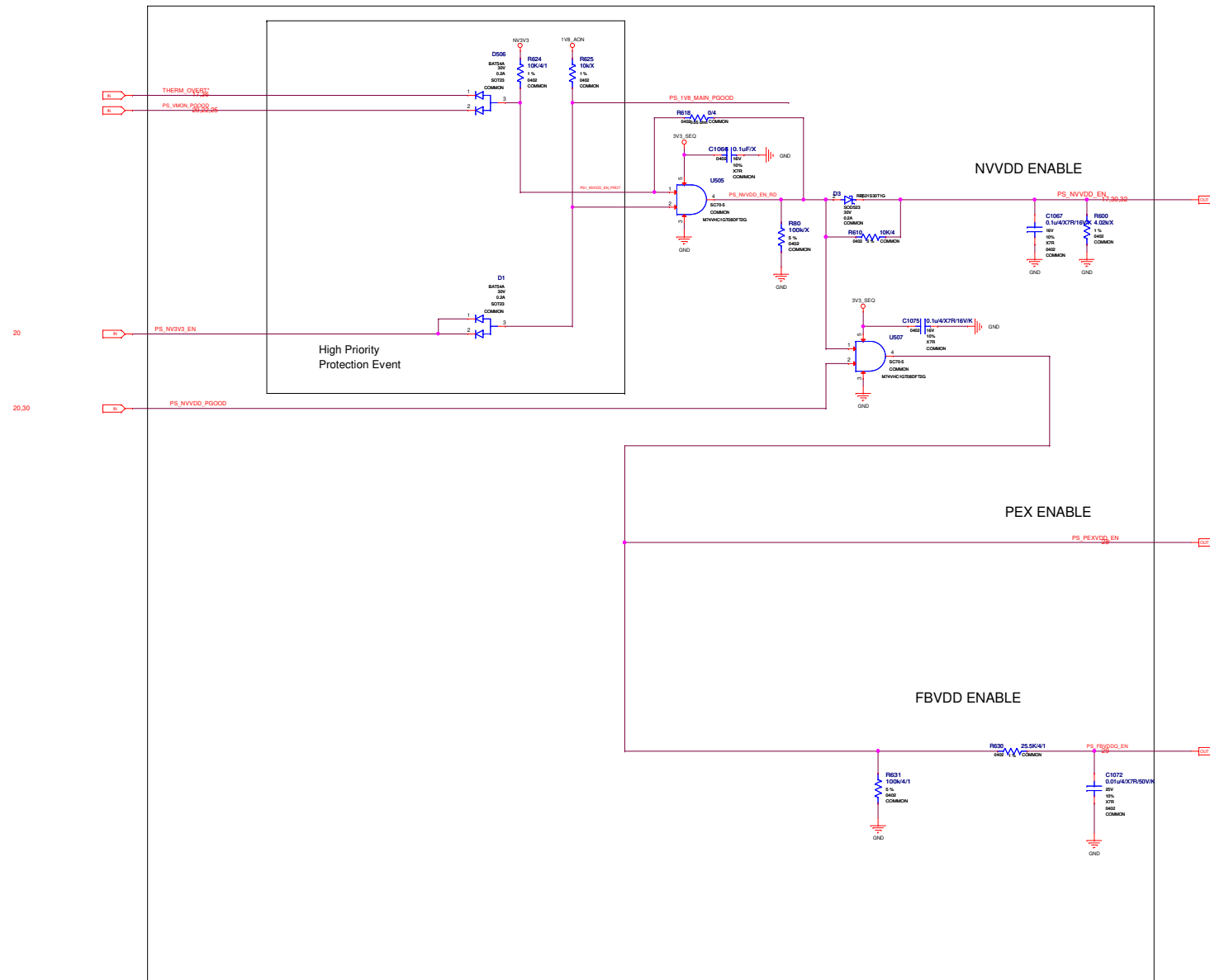
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SEQ:5V,1V8,NV3V3 ENABLE
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Size	Document Number	Rev	
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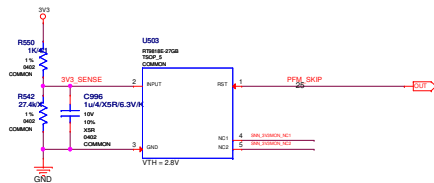
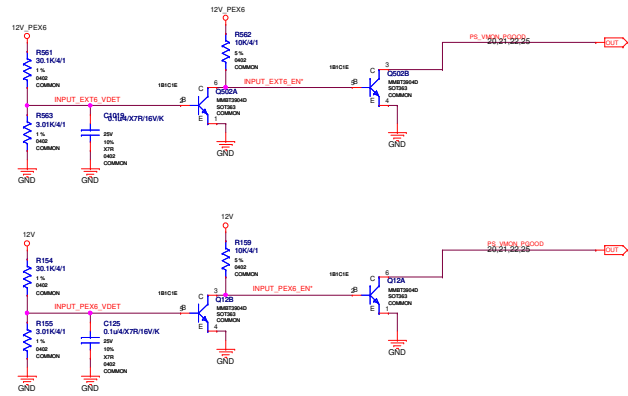


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Size	Document Number	Rev	
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Title			
NV,PEX,FB ENABLE			
Size	Document Number	Rev	
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SEQUENCE:Voltage Monitor



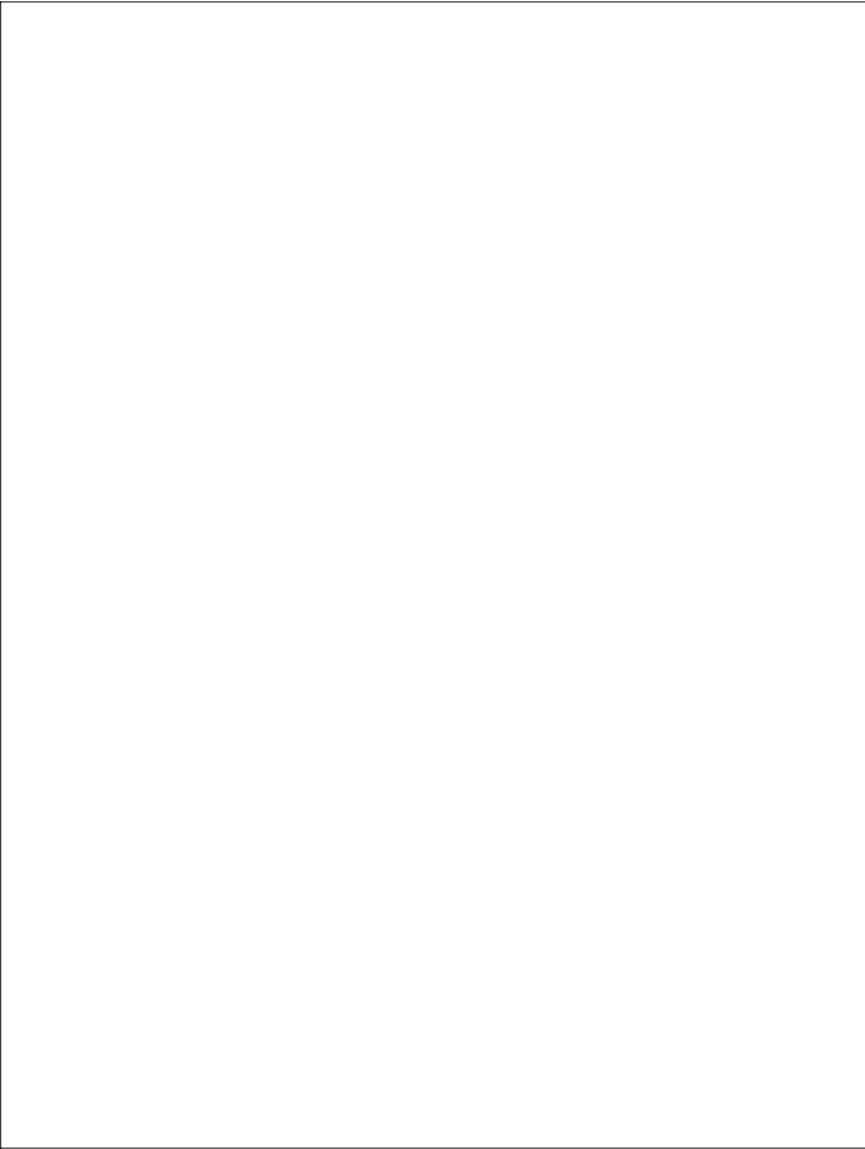
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Title			
Voltage Monitor			
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SEQUENCE:Discharge



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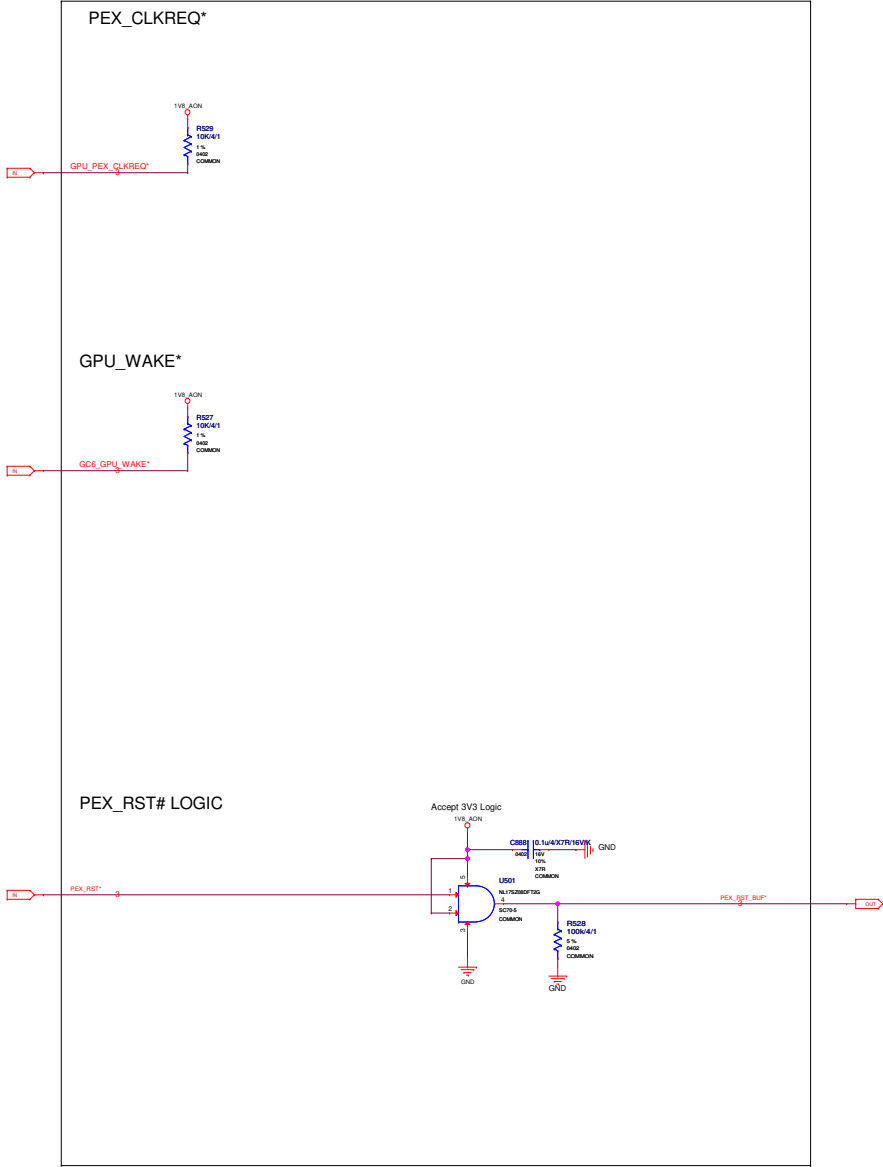
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Discharge

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SEQUENCE:MISC



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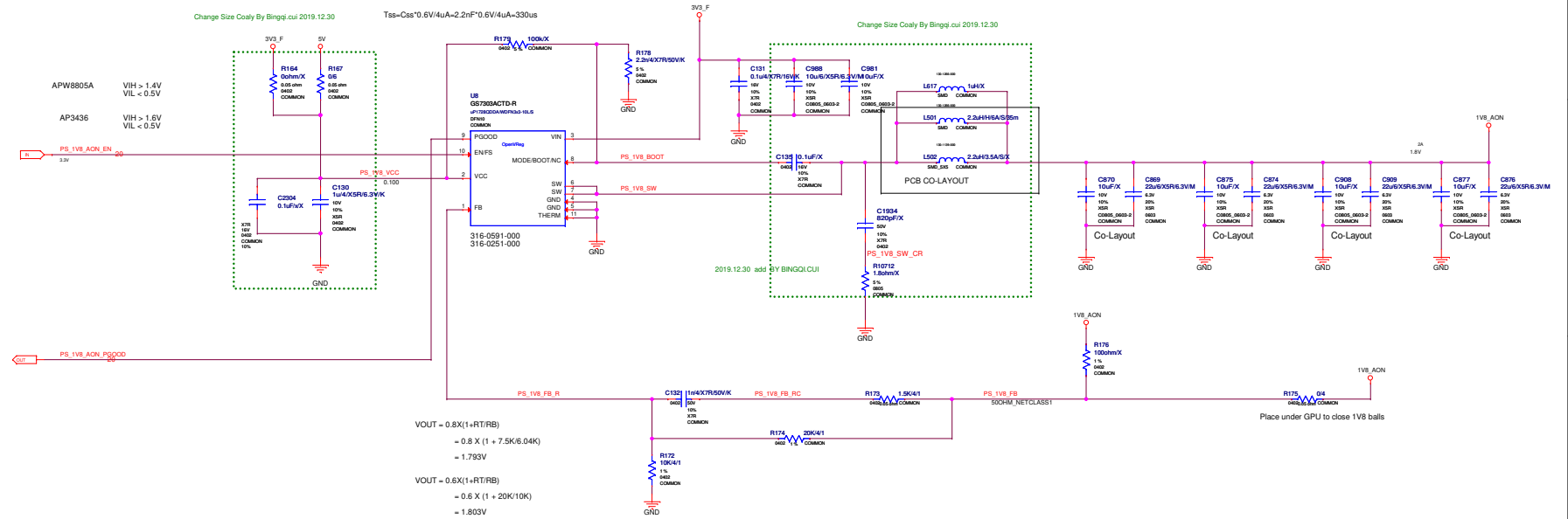
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PS: 1V8

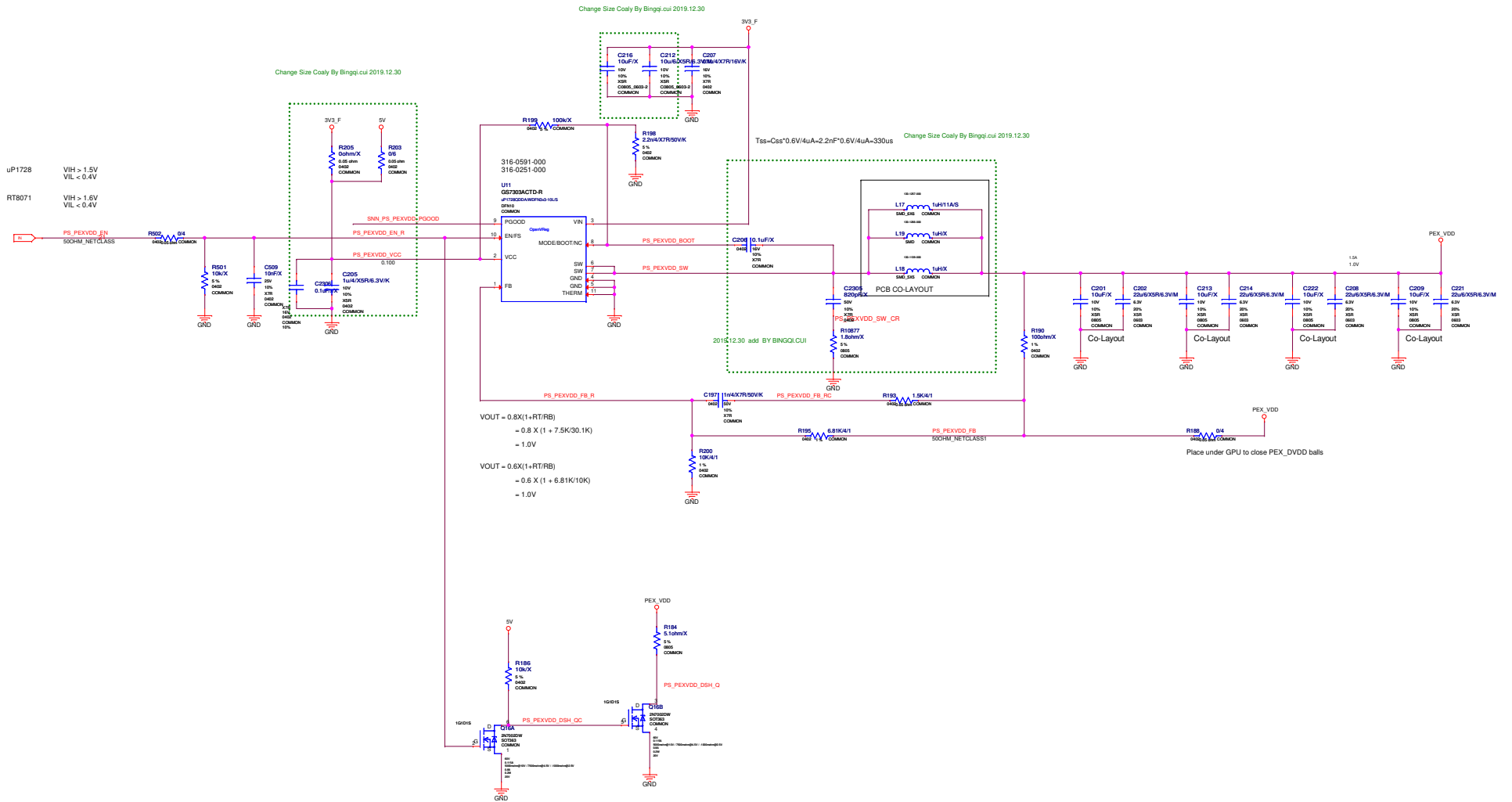


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Title			
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PS: PEXVDD



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
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Title PEXVDD			
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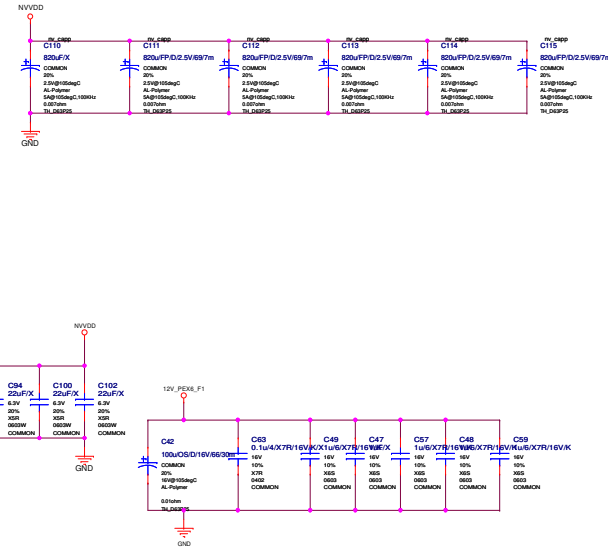
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PS: NVVDD PH2

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NCP81161 漏极驱动

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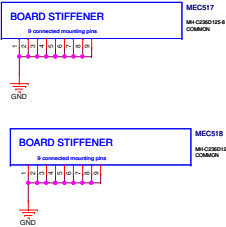
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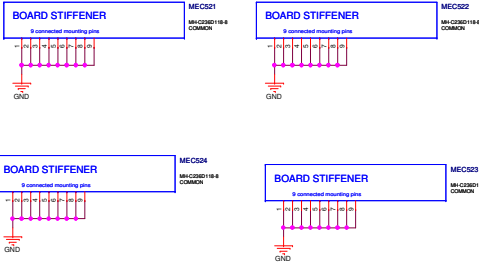
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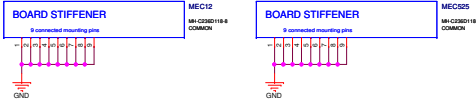
Brackets:



GPU



mos



bat



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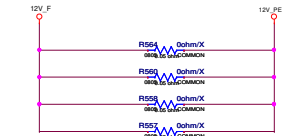
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Bracket/Thermal Solution

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Power Inputs and Filtering



Option for 75W ADC+MUX Capping SKU

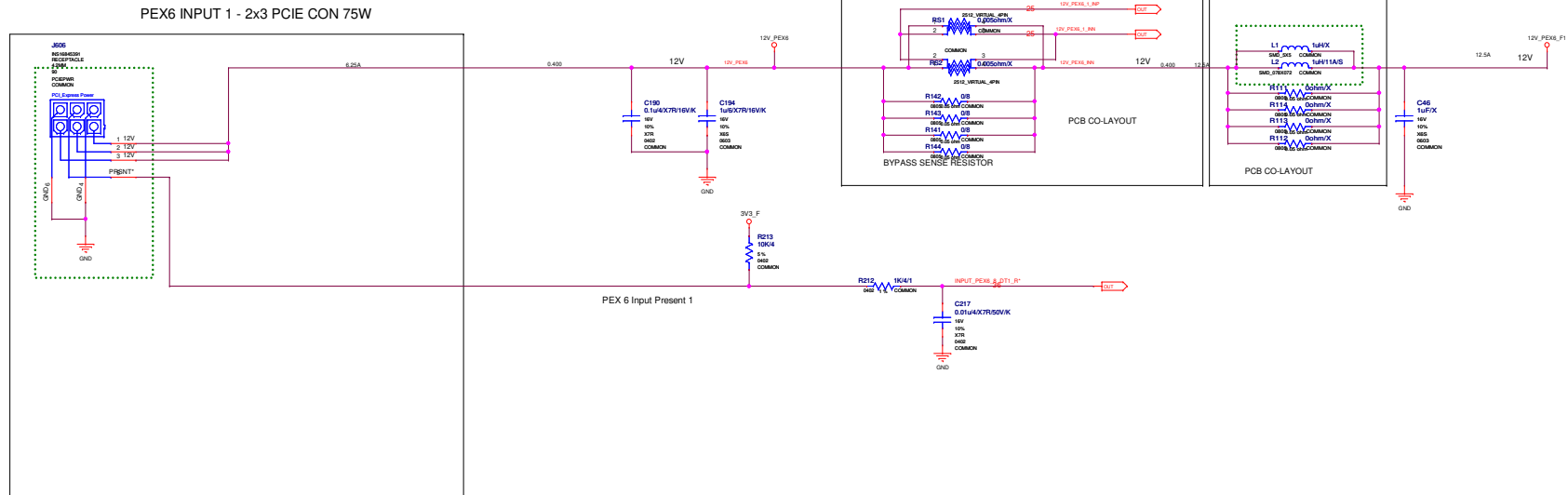


75W SKU: STUFF JUMPERS

Option for 75W BA Capping SKU

Shortest physical path

XXW SKU(NV 2PH): STUFF RSENSE 2, NVVDD = 2 * RSENSE 2
90W SKU(NV 3PH): STUFF RSENSE 2, NVVDD = 1.5 * RSENSE 2



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Power Inputs and Filtering

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: STEERING, UNDER POWER BOOT & HOF-IMPULS

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