

PG210 B00

GP107 128b GDDR5, 75W , PCB 5.7"
DVI-D_DL (DP + DP) + HDMI (DP) + DP

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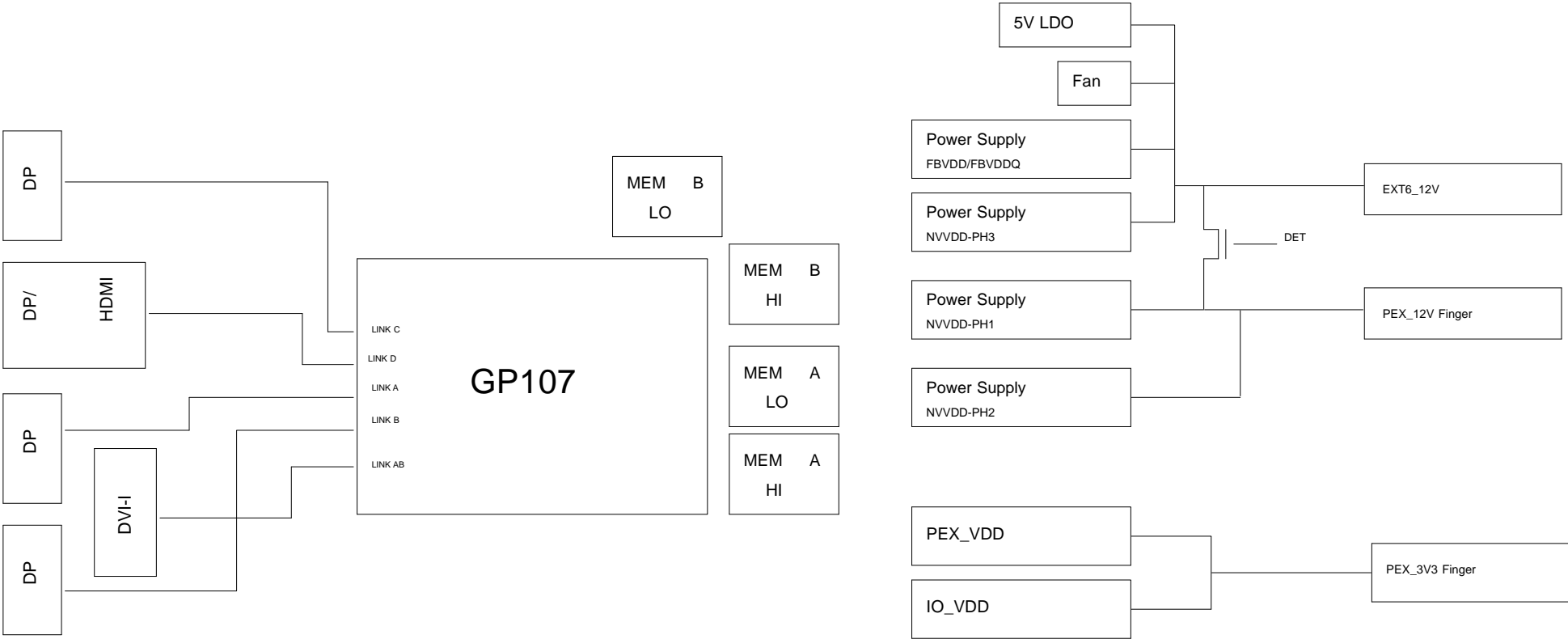
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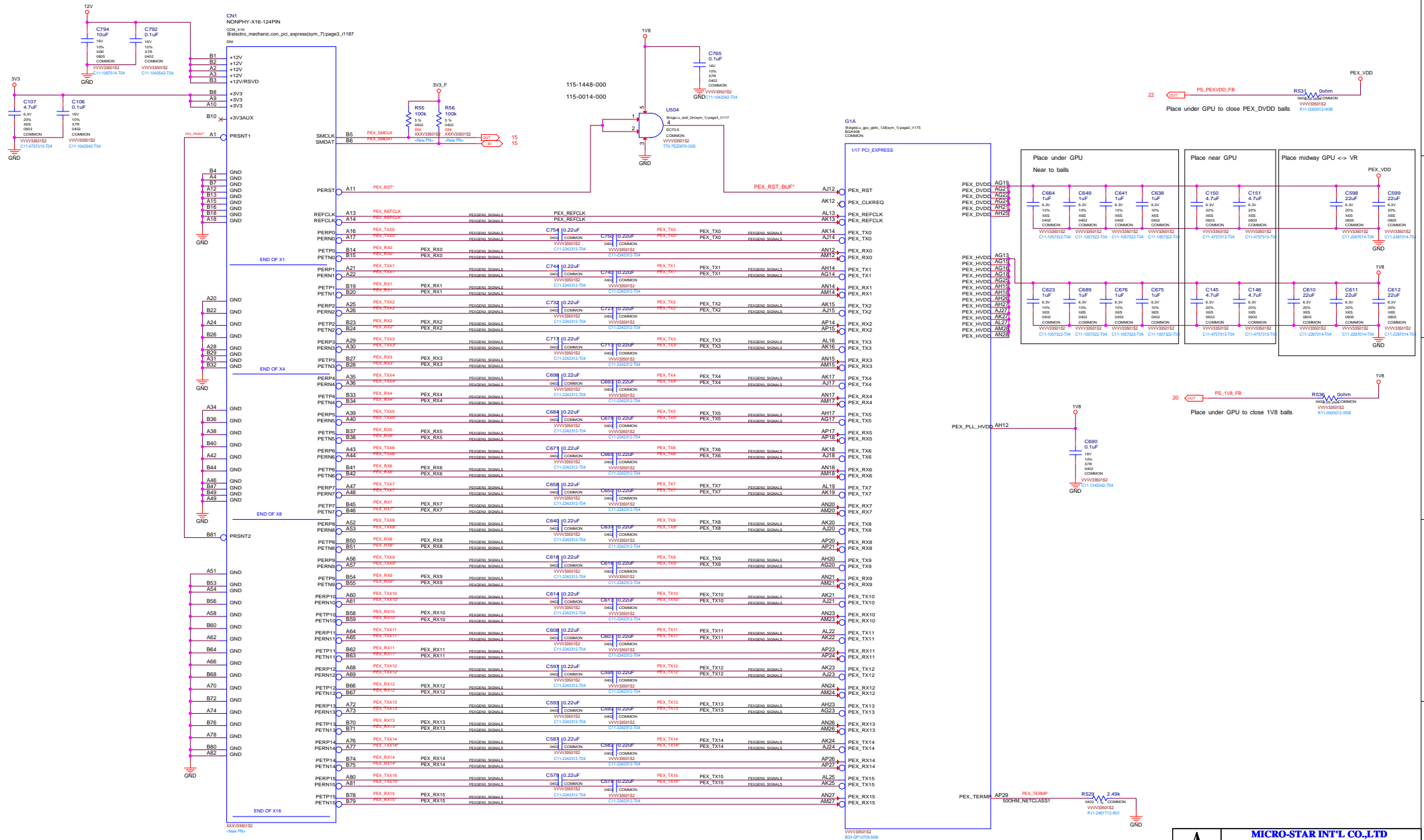
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1	No change

Block Diagram



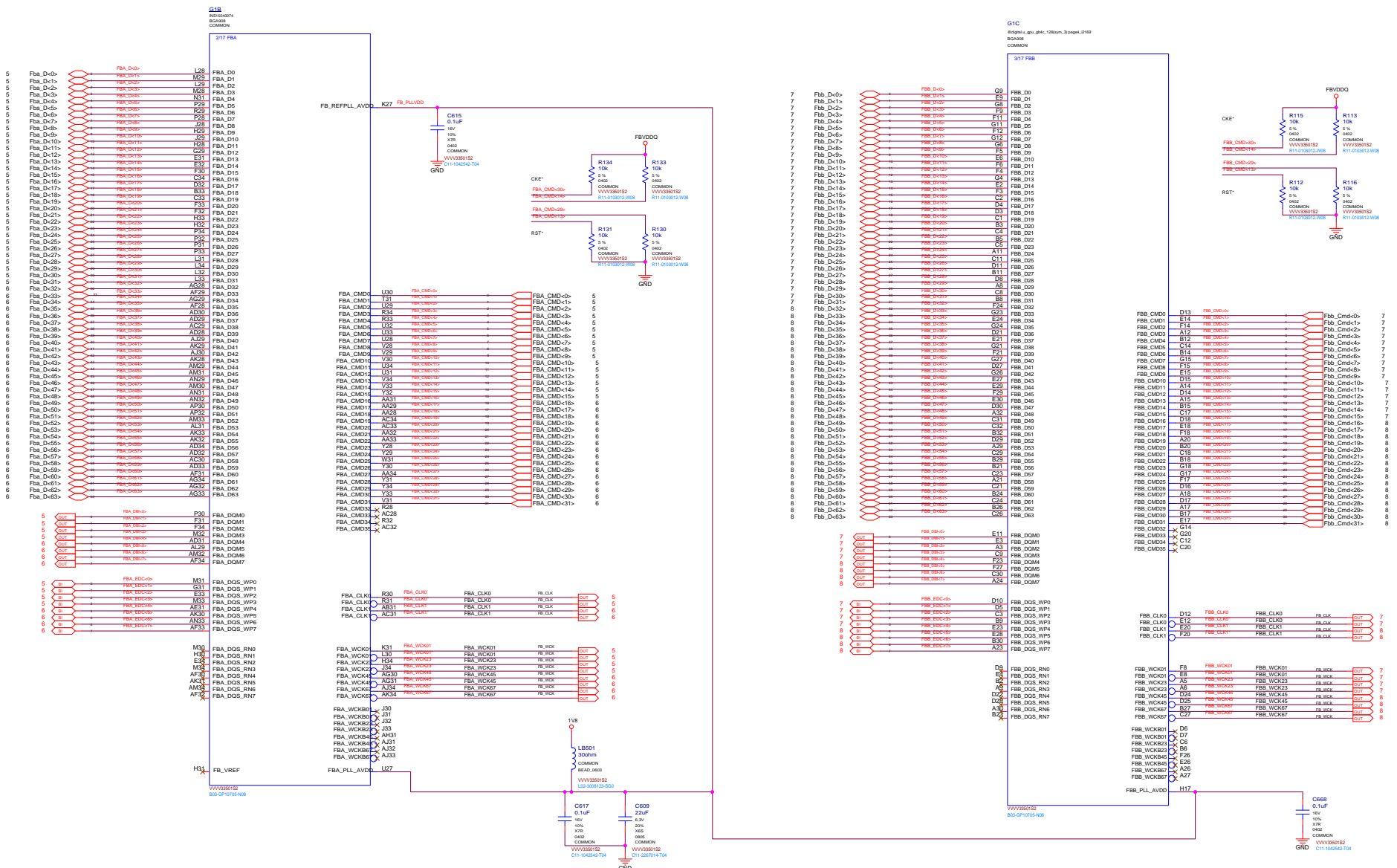
PCI Express



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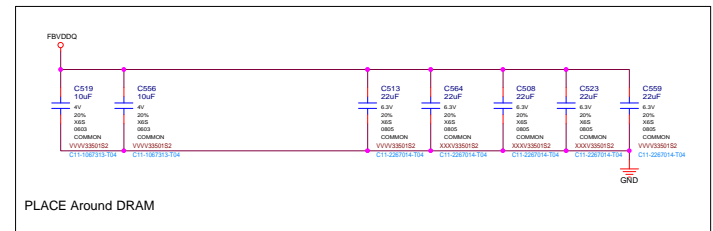
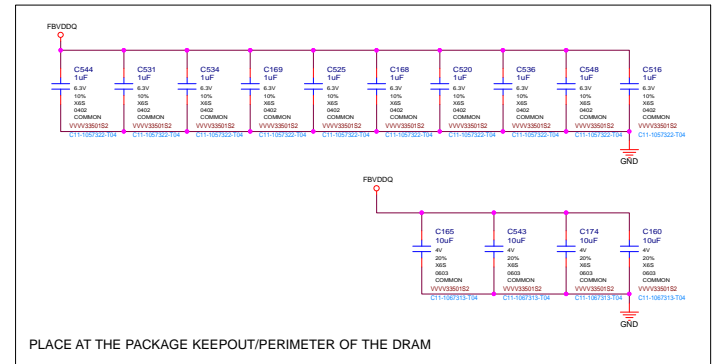
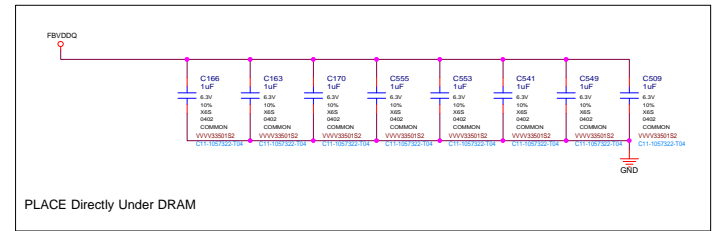
MEMORY: GPU Partition A/B



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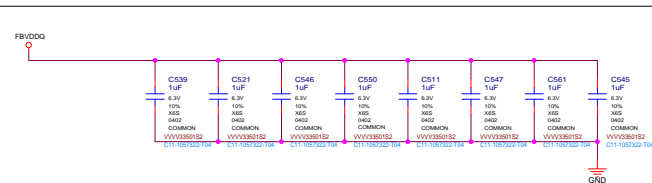
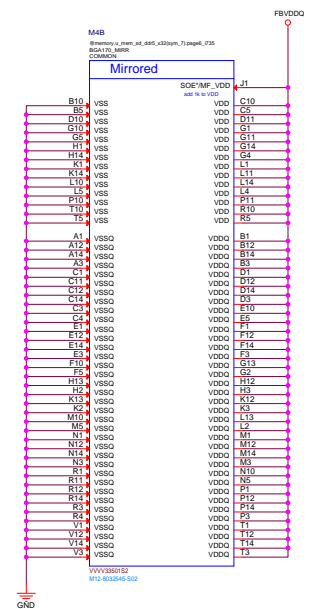
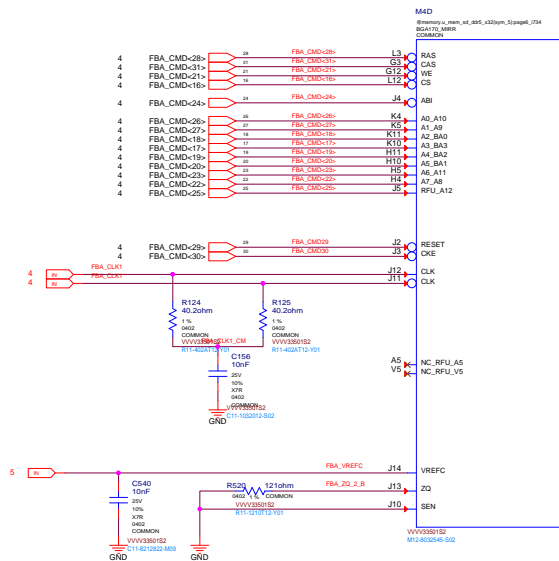
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CMD	0..31	32..63
CMD0	CS*	
CMD1	A3..BA3	
CMD2	A2..BA2	
CMD3	A4..BA4	
CMD4	A5..BA1	
CMD5	WE*	
CMD6	A7..A8	
CMD7	A6..A11	
CMD8	AB*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A9	
CMD12	RA5*	
CMD13	RS1*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3..BA3
CMD18		A2..BA2
CMD19		A4..BA4
CMD20		A5..BA1
CMD21		WE*
CMD22		A7..A8
CMD23		A6..A11
CMD24		AB*
CMD25		A12..RFU
CMD26		RA5*
CMD27		A1..A9
CMD28		RS1*
CMD29		CKE*
CMD30		CAS*
CMD31		

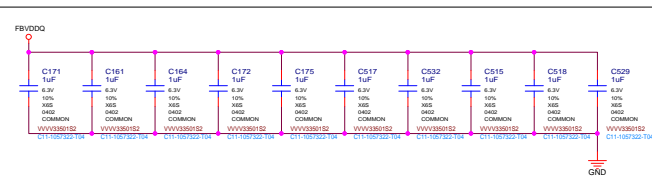


MEMORY: FBA Partition 63..32

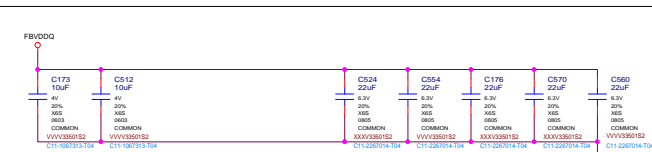
CMD	0..31	32..63
CMD0	CS*	
CMD1	A3..BA3	
CMD2	A2..BA2	
CMD3	A4..BA2	
CMD4	A5..BA1	
CMD5	WE*	
CMD6		
CMD7	AE..A11	
CMD8	AB*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A0	
CMD12	RA*	
CMD13	RB*	
CMD14	CK*	
CMD15	CA*	
CMD16		
CMD17		CS*
CMD18	A3..BA3	
CMD19	A2..BA2	
CMD20	A5..BA1	
CMD21	WE*	
CMD22	A7..AB	
CMD23	AE..AB1	
CMD24		
CMD25	A12..RFU	
CMD26	A0..A10	
CMD27	A1..A0	
CMD28	RA*	
CMD29	RB*	
CMD30	CK*	
CMD31	CA*	



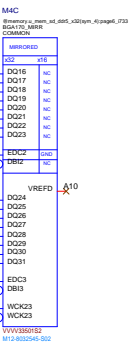
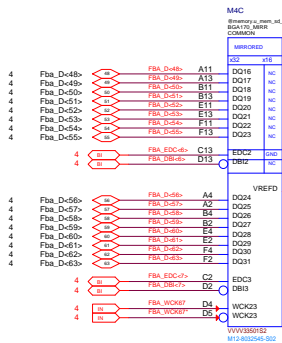
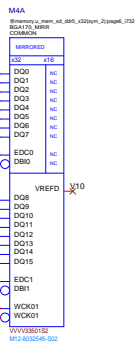
LACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM

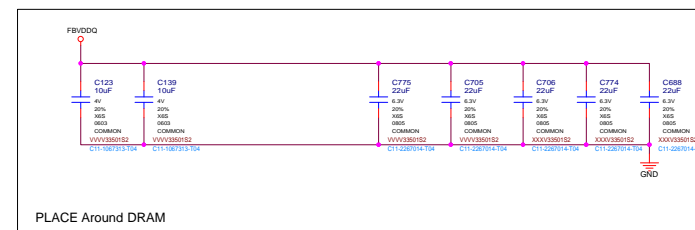
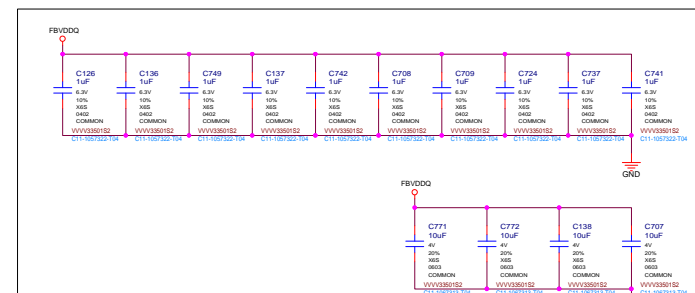
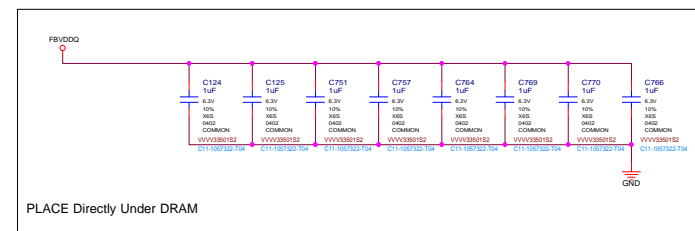
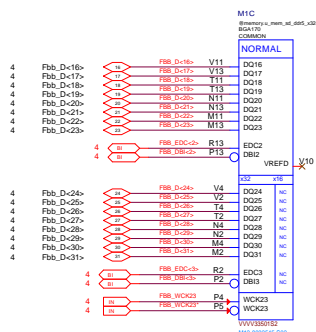
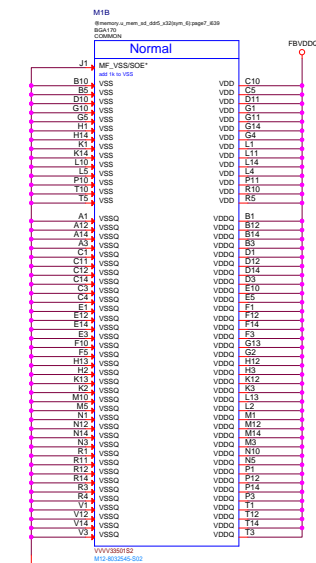
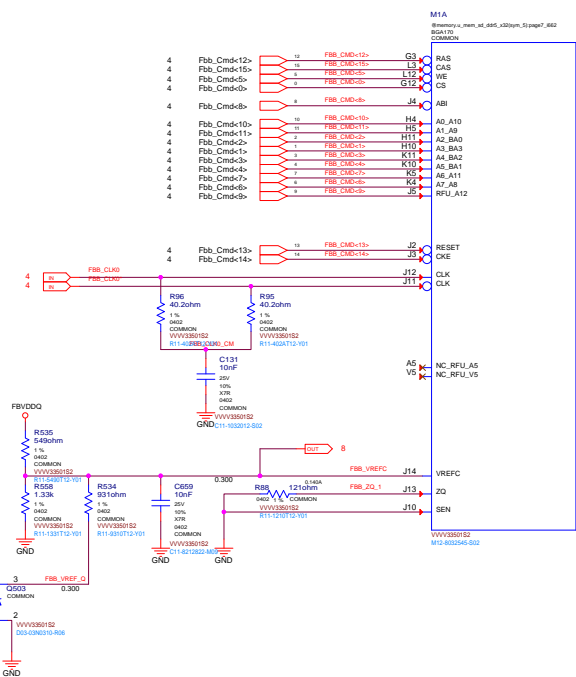


LACE Around DRAM



MEMORY: FBB Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3..BA3	
CMD2	A2..BA0	
CMD3	A4..BA2	
CMD4	A5..BA1	
CMD5	WE*	
CMD6	AF..A8	
CMD7	AB..A11	
CMD8	AB*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A9	
CMD12	RA*	
CMD13	RS1*	
CMD14	CK*	
CMD15	CAS*	
CMD16		
CMD17		CS*
CMD18		A3..BA3
CMD19		A2..BA0
CMD20		A4..BA2
CMD21		A5..BA1
CMD22		WE*
CMD23		AF..A8
CMD24		AB..A11
CMD25		AB*
CMD26		A12..RFU
CMD27		A0..A10
CMD28		A1..A9
CMD29		RA*
CMD30		RS1*
CMD31		CK*
		CAS*

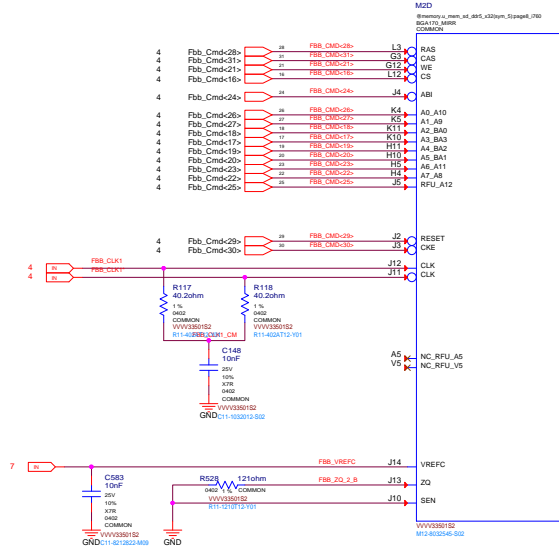


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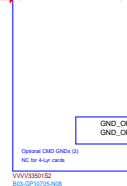
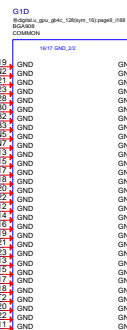
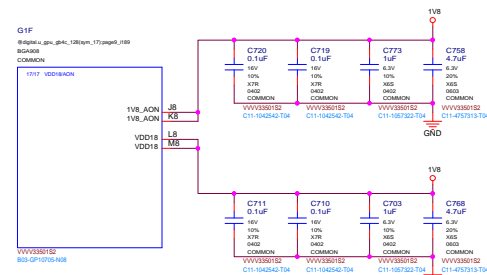
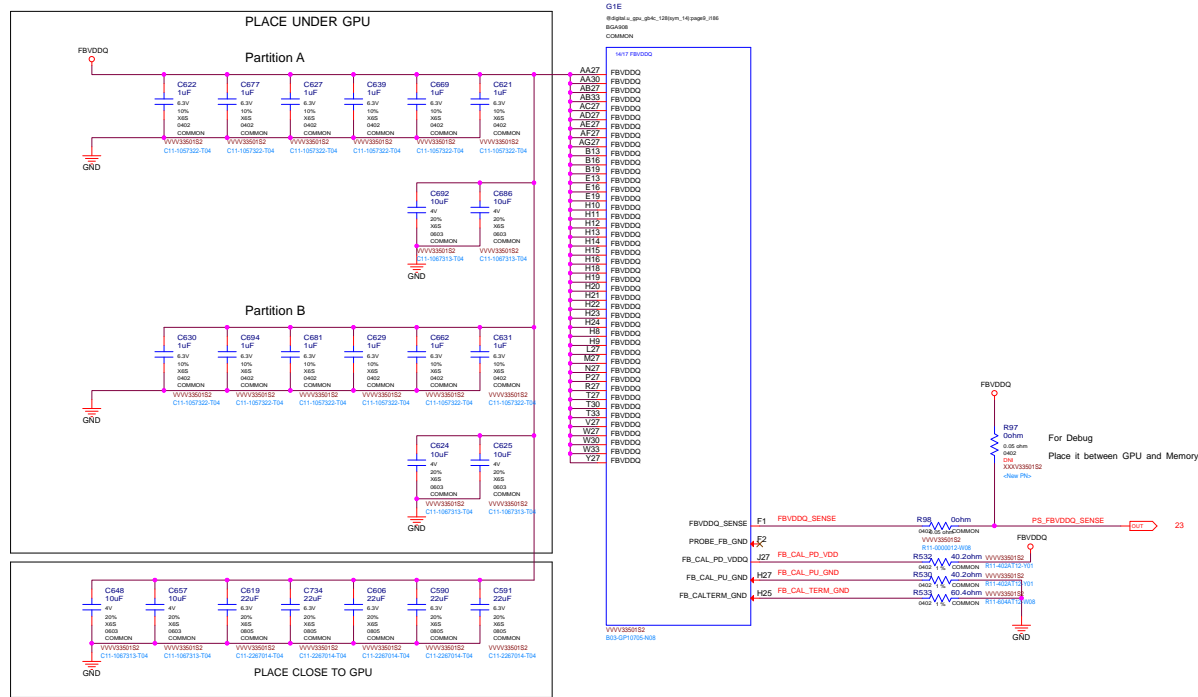
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MEMORY: FBB Partition 63..32

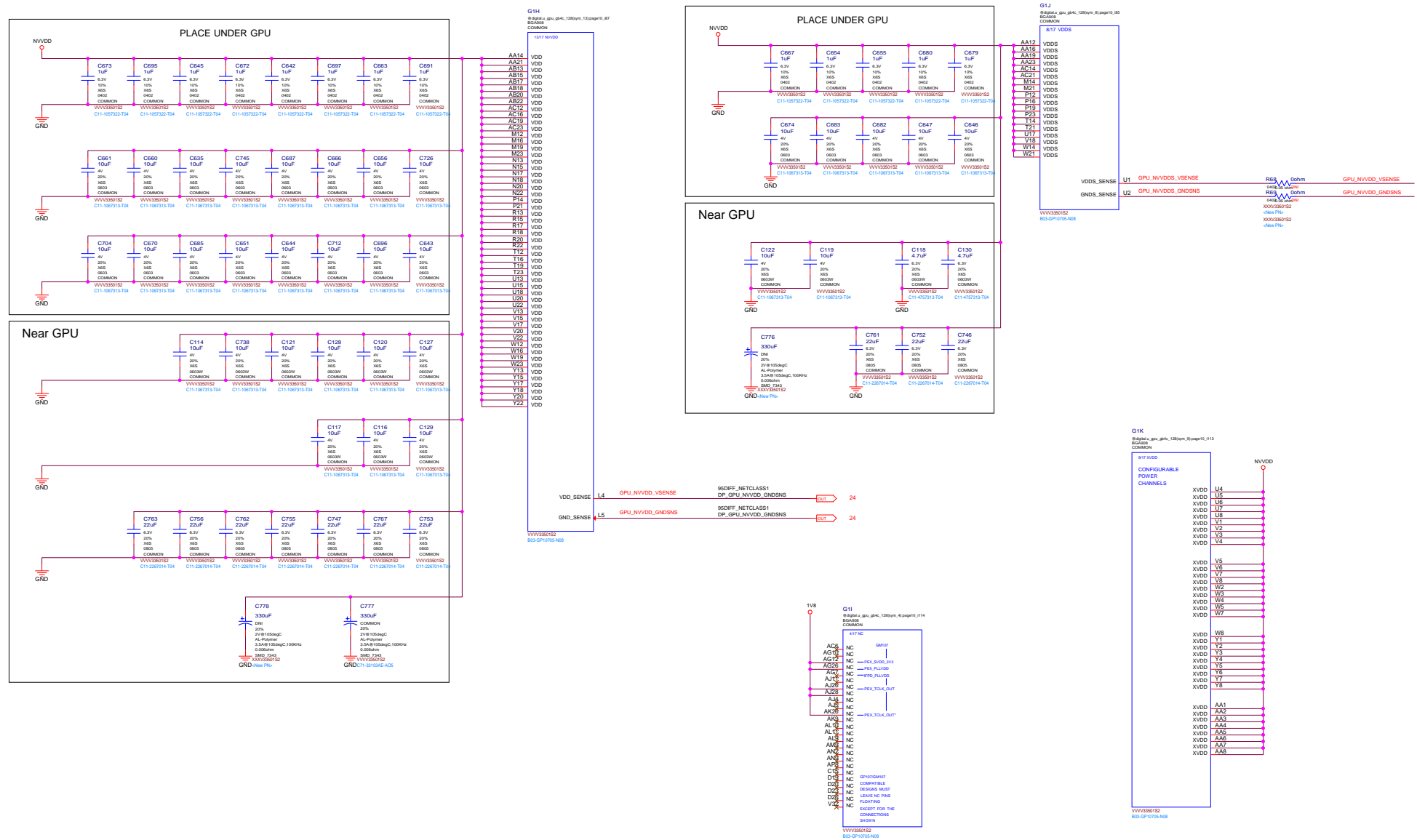
CMD	0..31	32..63
CMD0	CS*	
CMD1	A3, BA3	
CMD2	A2, BA2	
CMD3	A4, BA2	
CMD4	A3, BA1	
CMD5	WE*	
CMD6	A7, A8	
CMD7	AL, A11	
CMD8	AB*	
CMD9	A12, RFU	
CMD10	A0, A10	
CMD11	A1, A9	
CMD12	RA5*	
CMD13	RS*	
CMD14	CH*	
CMD15	CAS*	
CMD16		
CMD17		
CMD18	A3, BA3	
CMD19	A2, BA2	
CMD20	A4, BA2	
CMD21	A3, BA1	
CMD22	WE*	
CMD23	A7, A8	
CMD24	AL, A11	
CMD25	AB*	
CMD26	A12, RFU	
CMD27	A0, A10	
CMD28	A1, A9	
CMD29	RA5*	
CMD30	RS*	
CMD31	CH*	



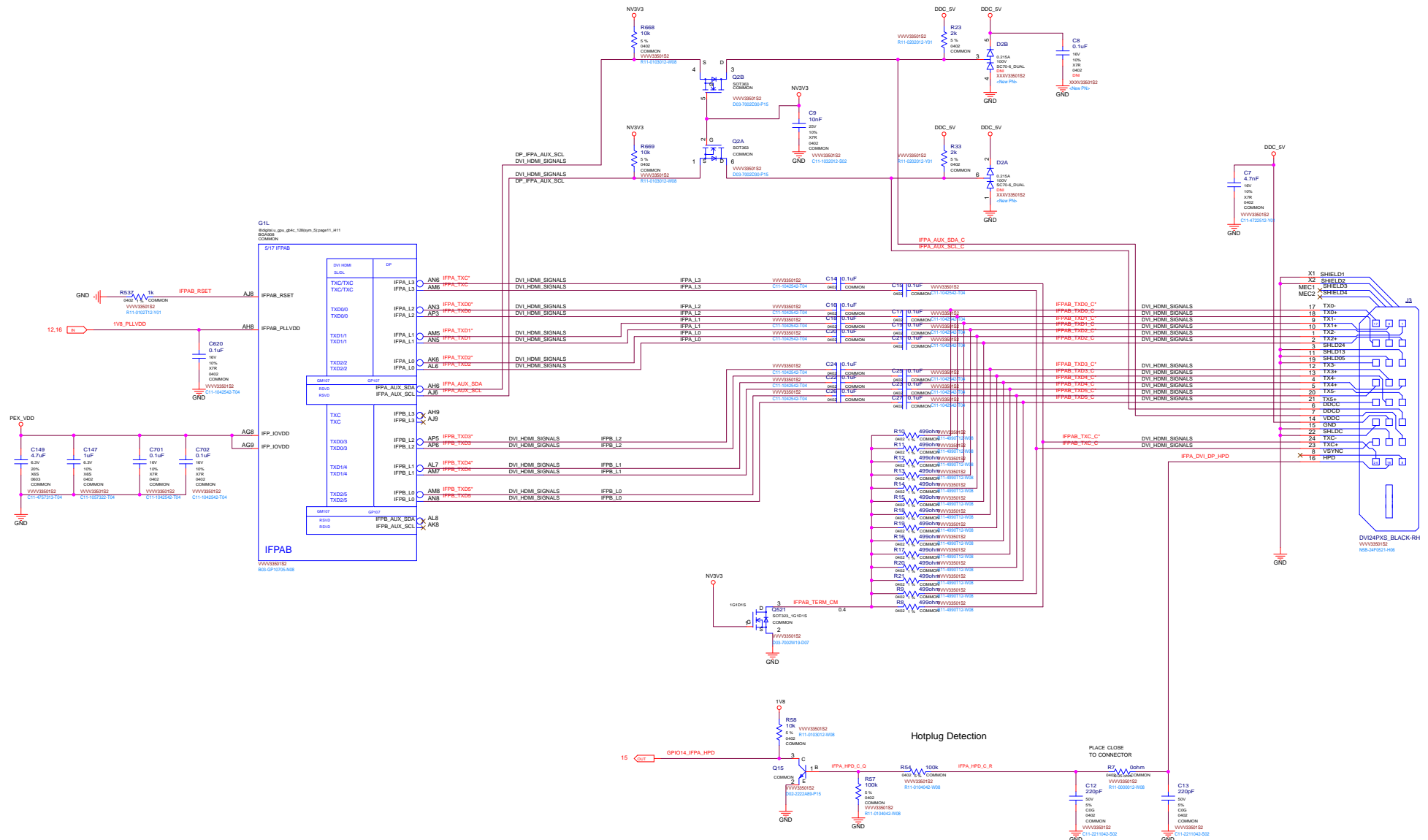
GPU FBVDDQ & 1V8 Decoupling



GPU NVVDD & NVVDDS Decoupling



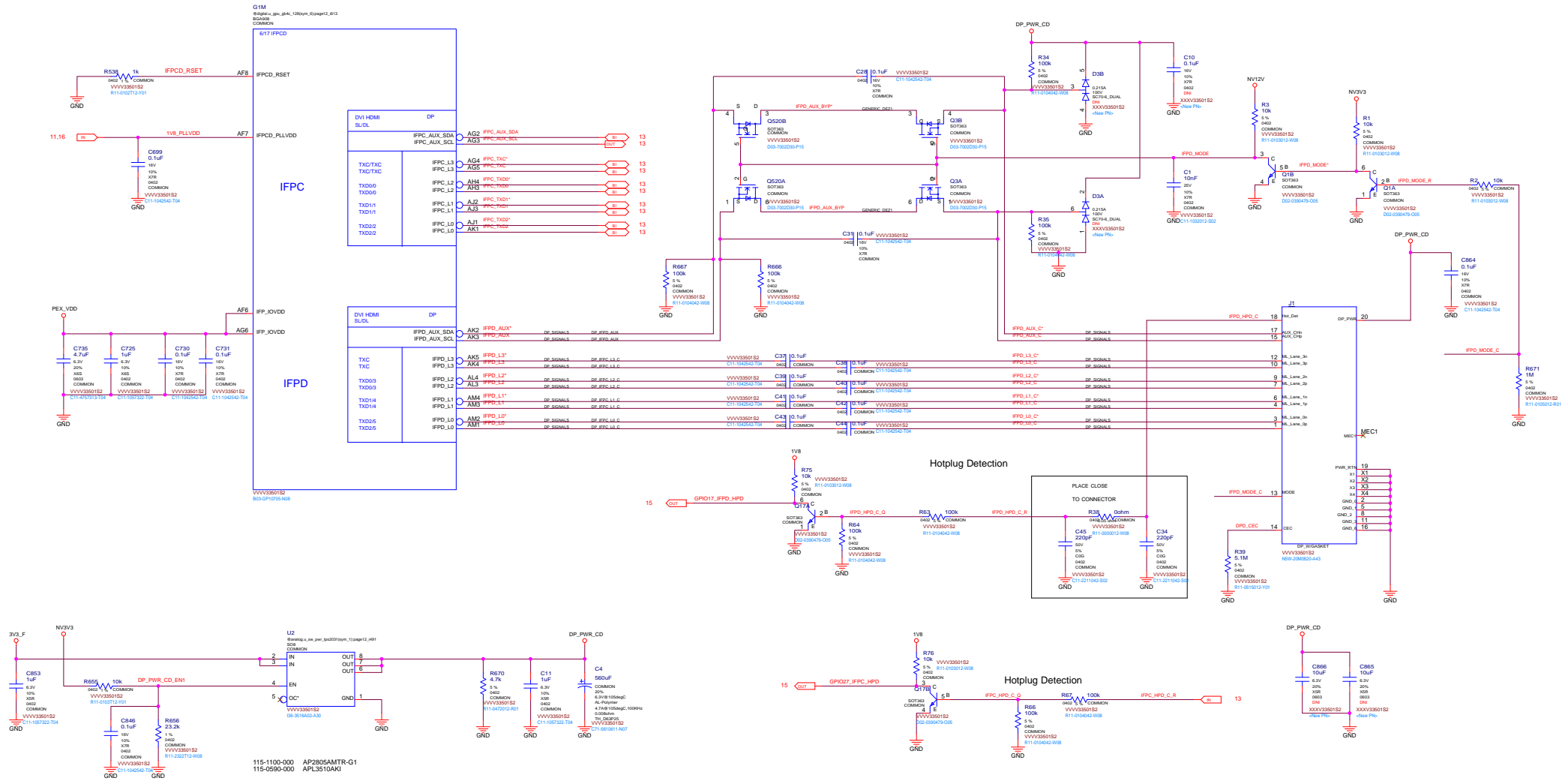
IFPAB DVI-DL



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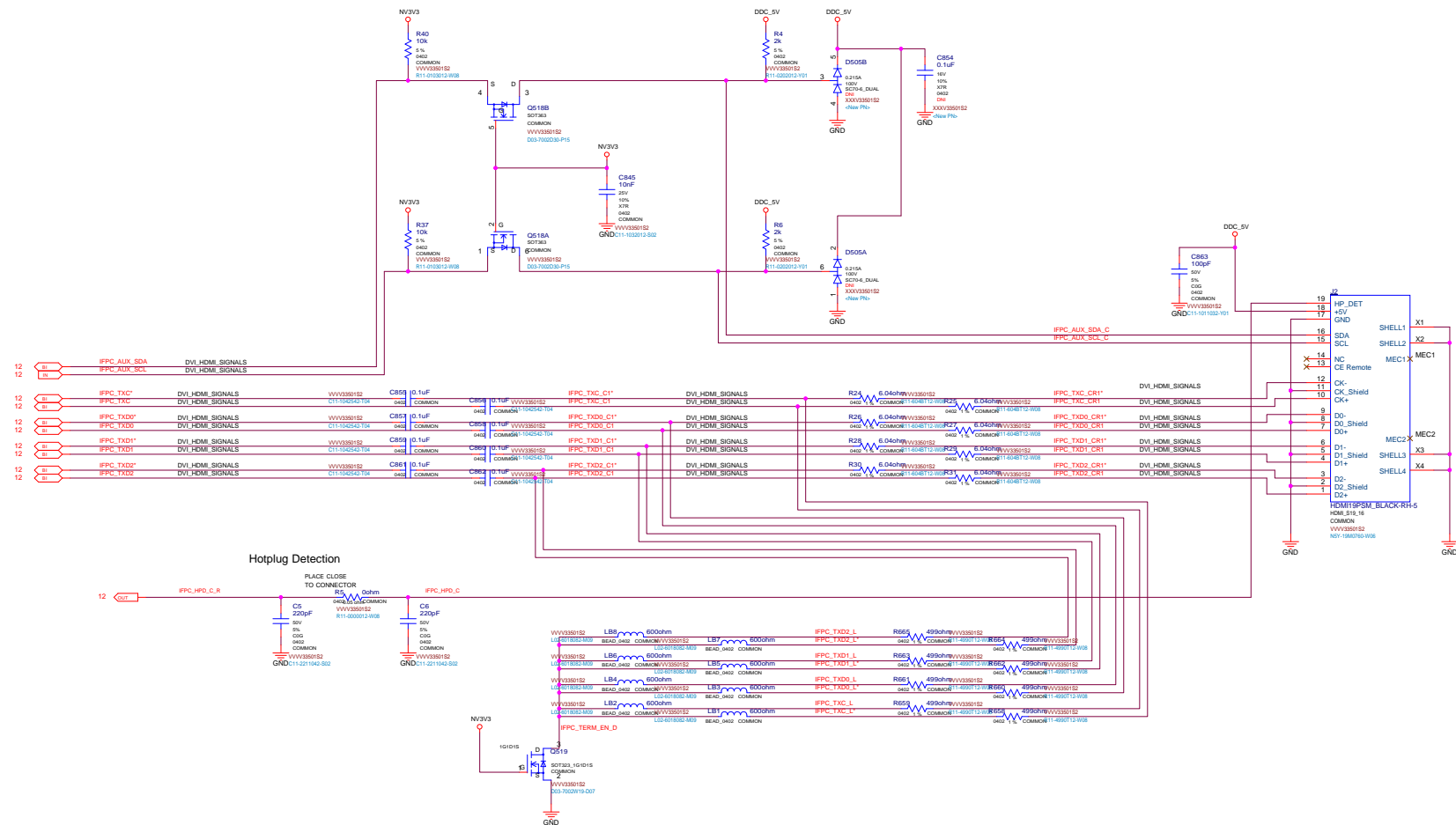
IFPD DP



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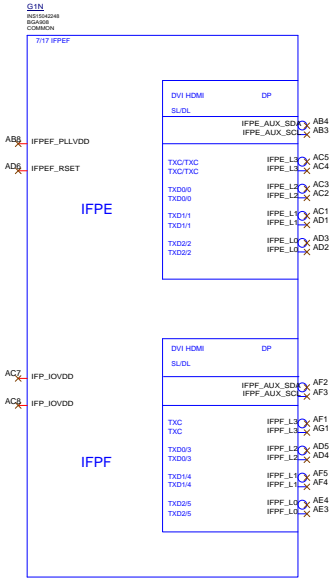
IFPC HDMI



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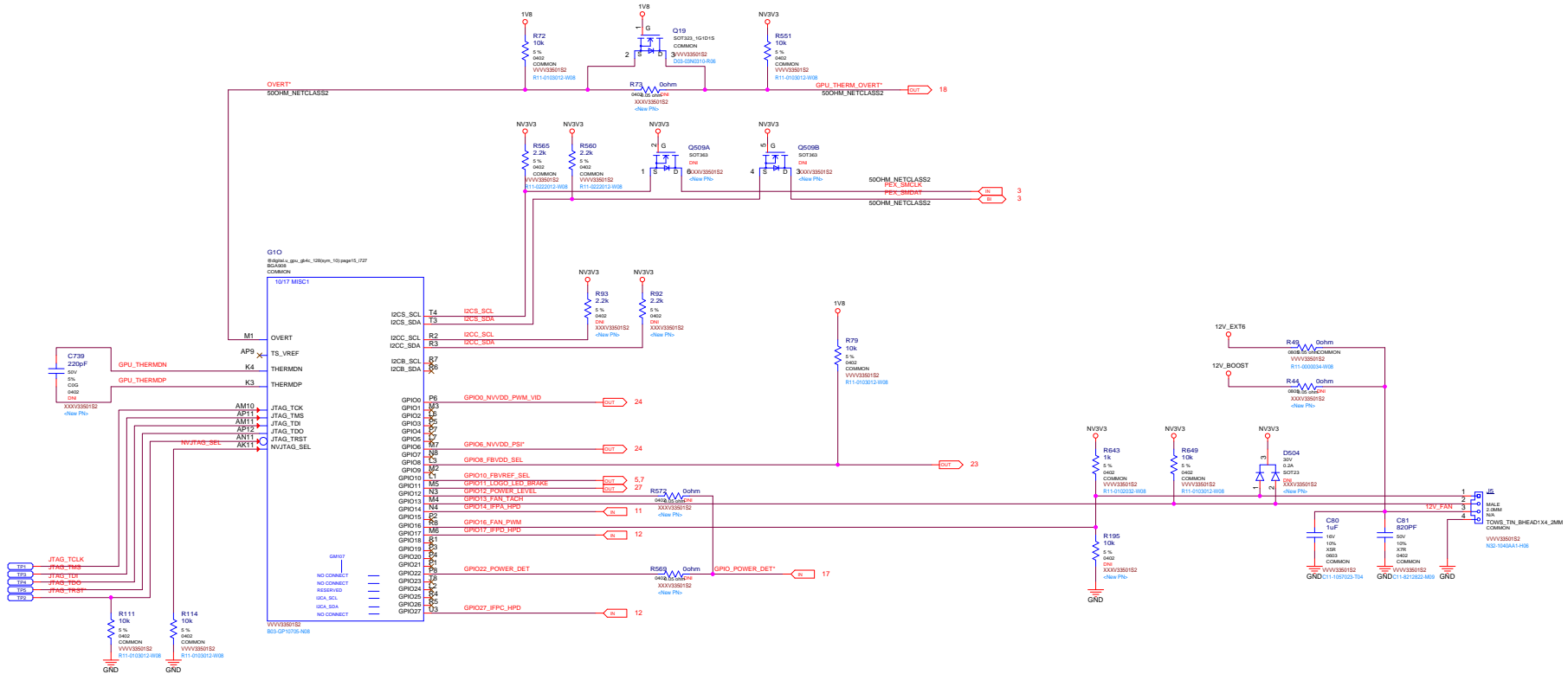
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IFPEF UNUSED



MISC1: GPIO, Fan, Thermal, JTAG

PADS FOR DEBUGGING



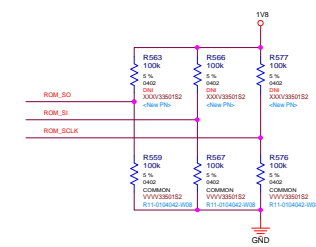
MISC2: ROM, XTAL, Straps

ROM_SO ROM_SI ROM_SCLK SOR_EXPOSED[3:0] 1:ENABLE 0:DISABLE

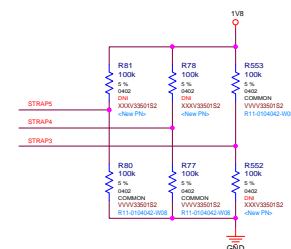
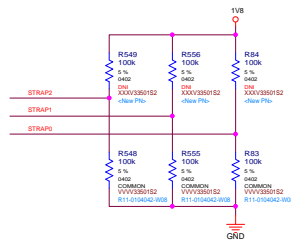
L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

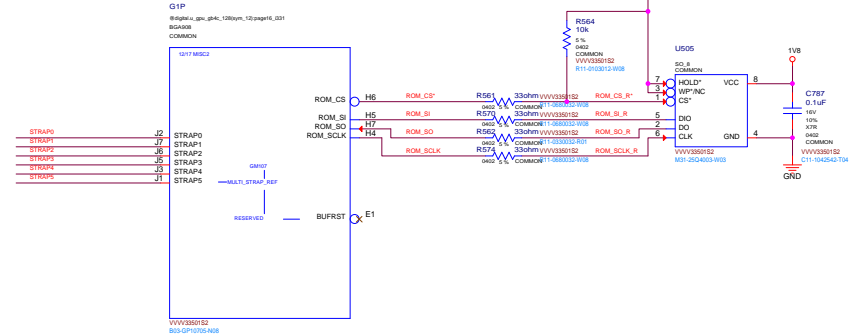
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

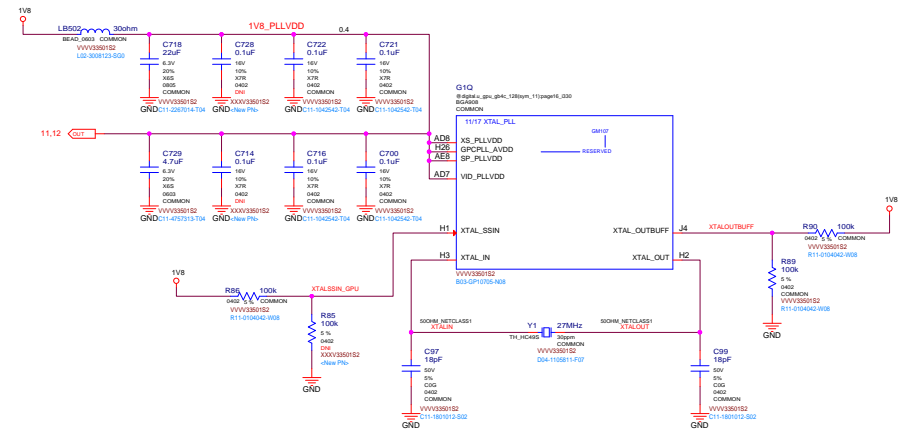


1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL SIGNAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

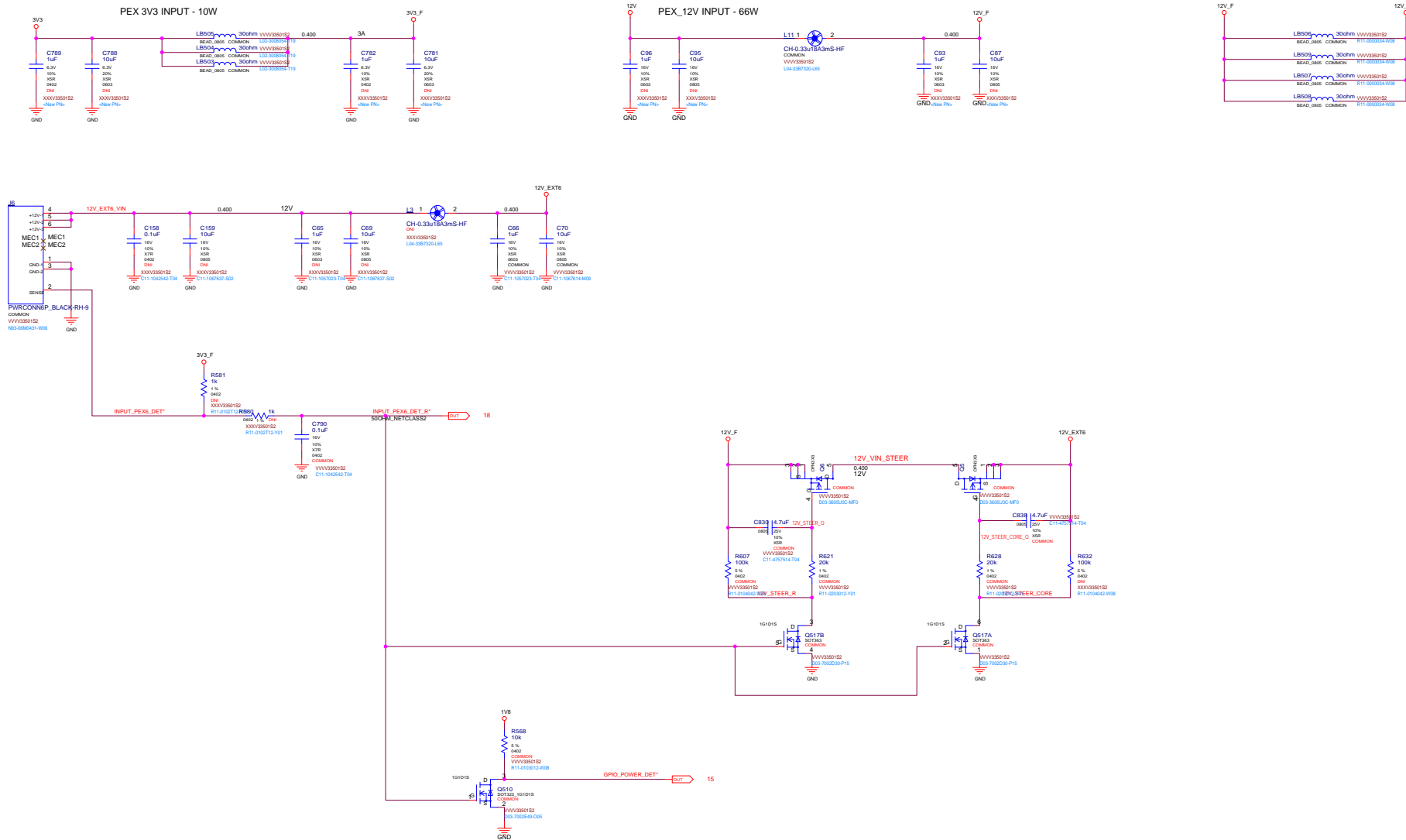


Smart Fan

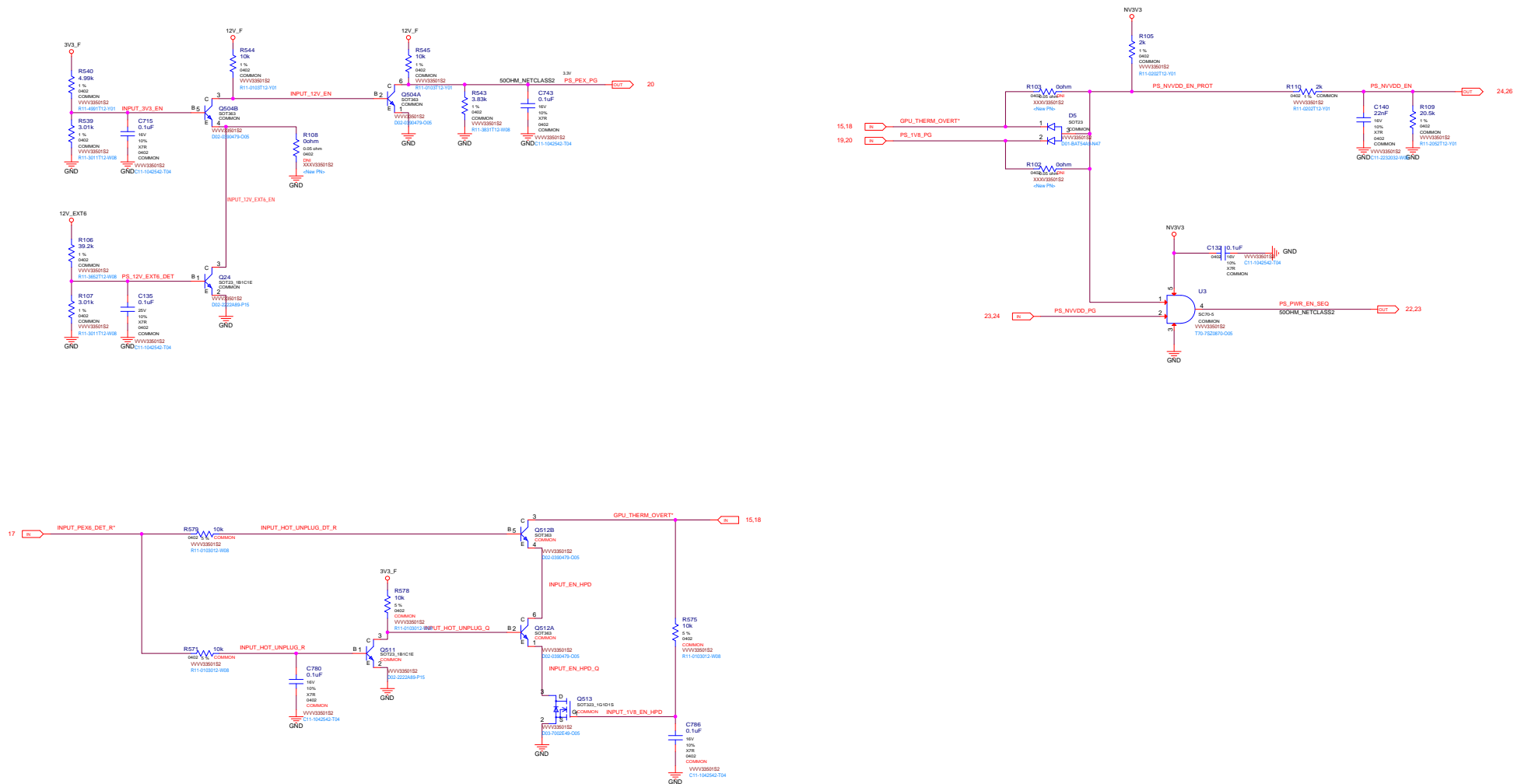
XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



Power Inputs and Filtering



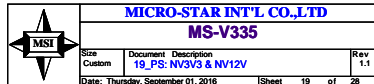
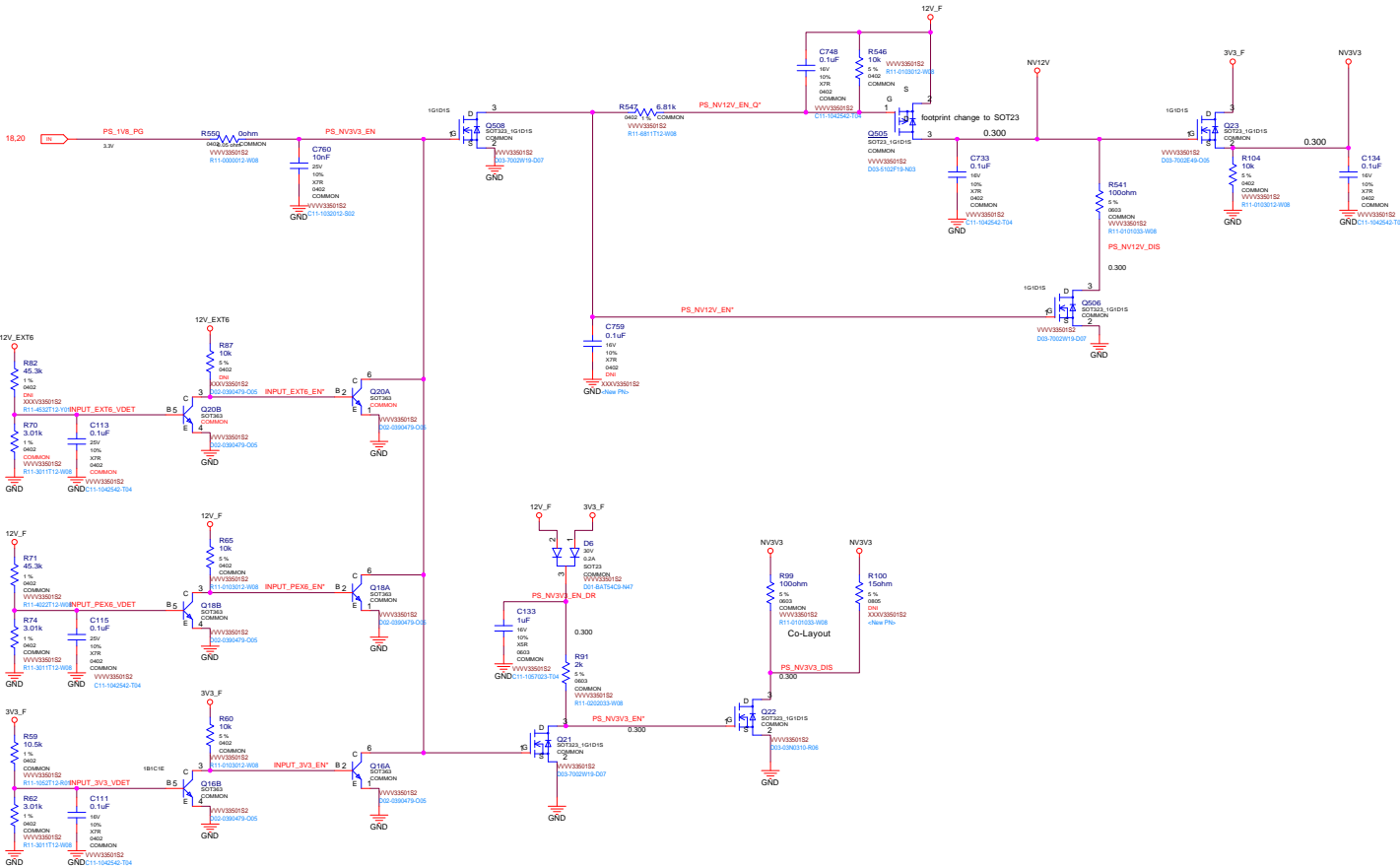
Power sequence



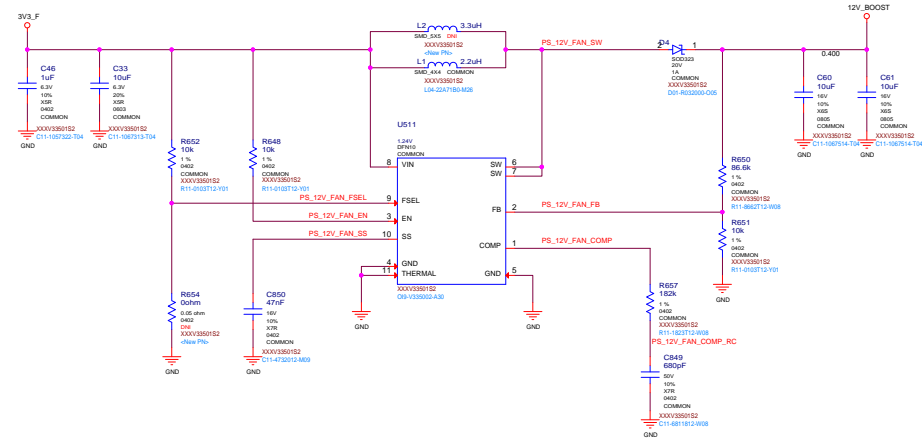
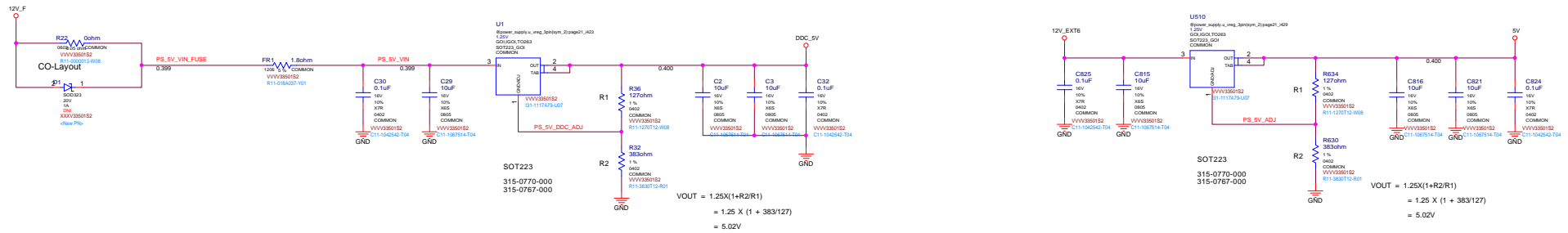
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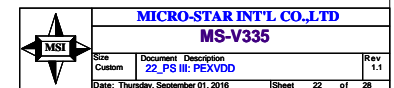
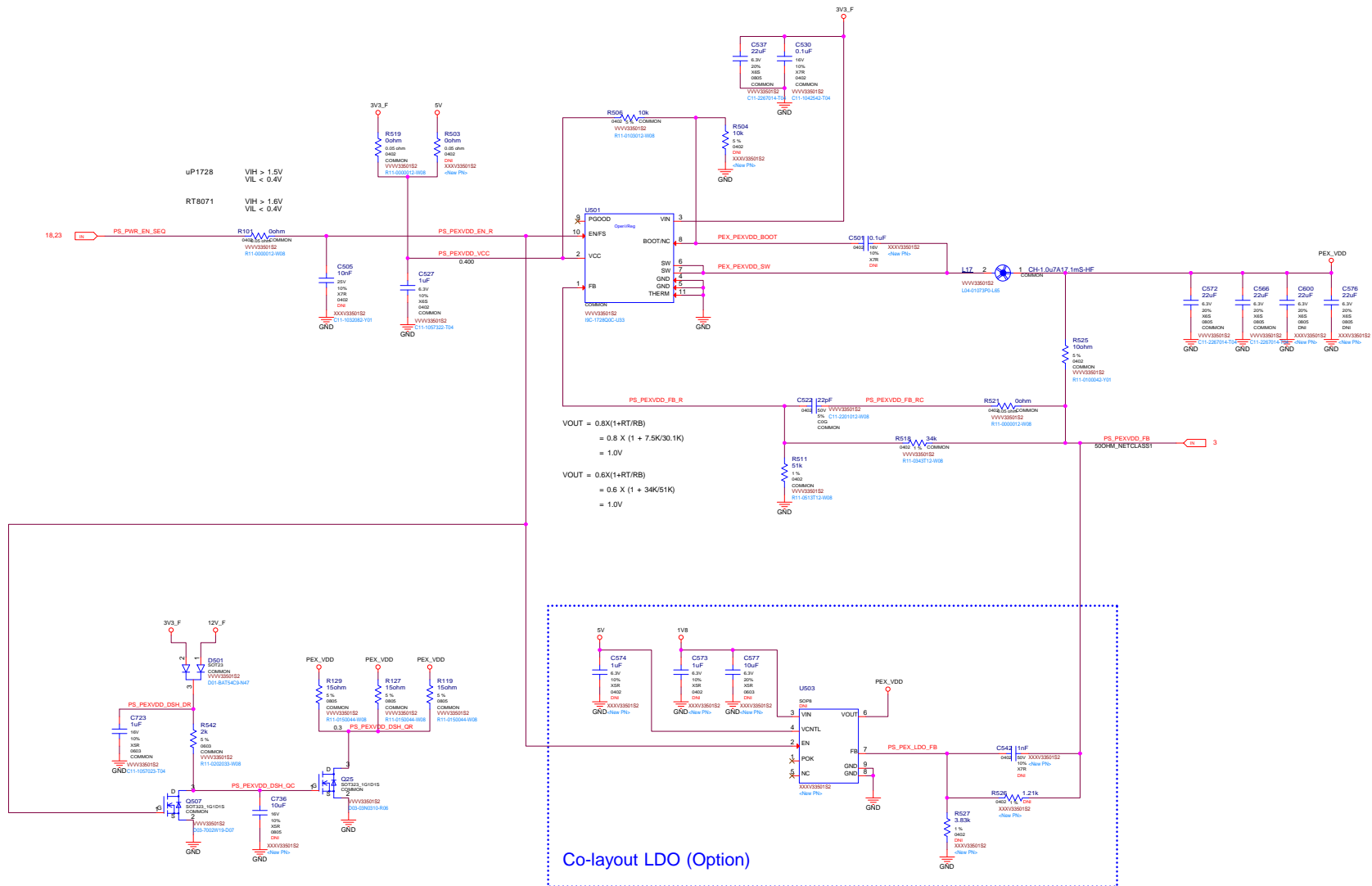
PS: NV3V3 & NV12V



PSII:5V & 12V_FAN



PS III: PEXVDD



PS IV: FBVDDQ

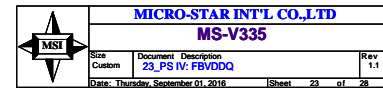
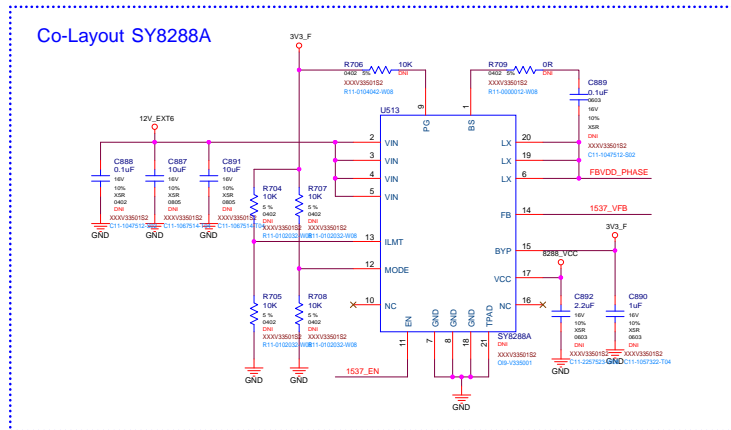
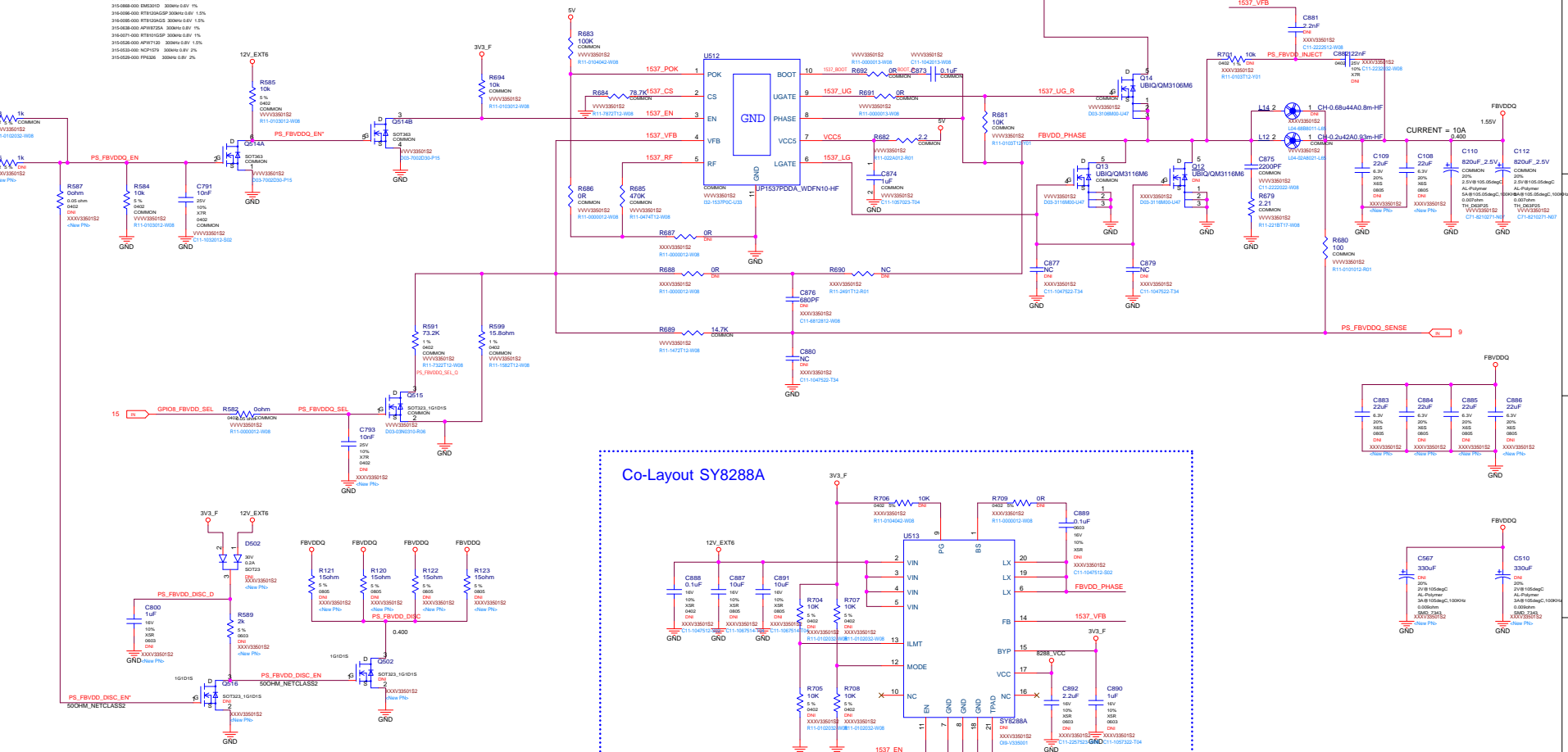
FBVDDQ_CTL	FBVDDQ	Non-DVS
X	1.5V	<= DEFAULT

FBVDDQ_CTL	FBVDDQ	For DVS
0	1.35V	
1	1.5V/1.55V	<= DEFAULT

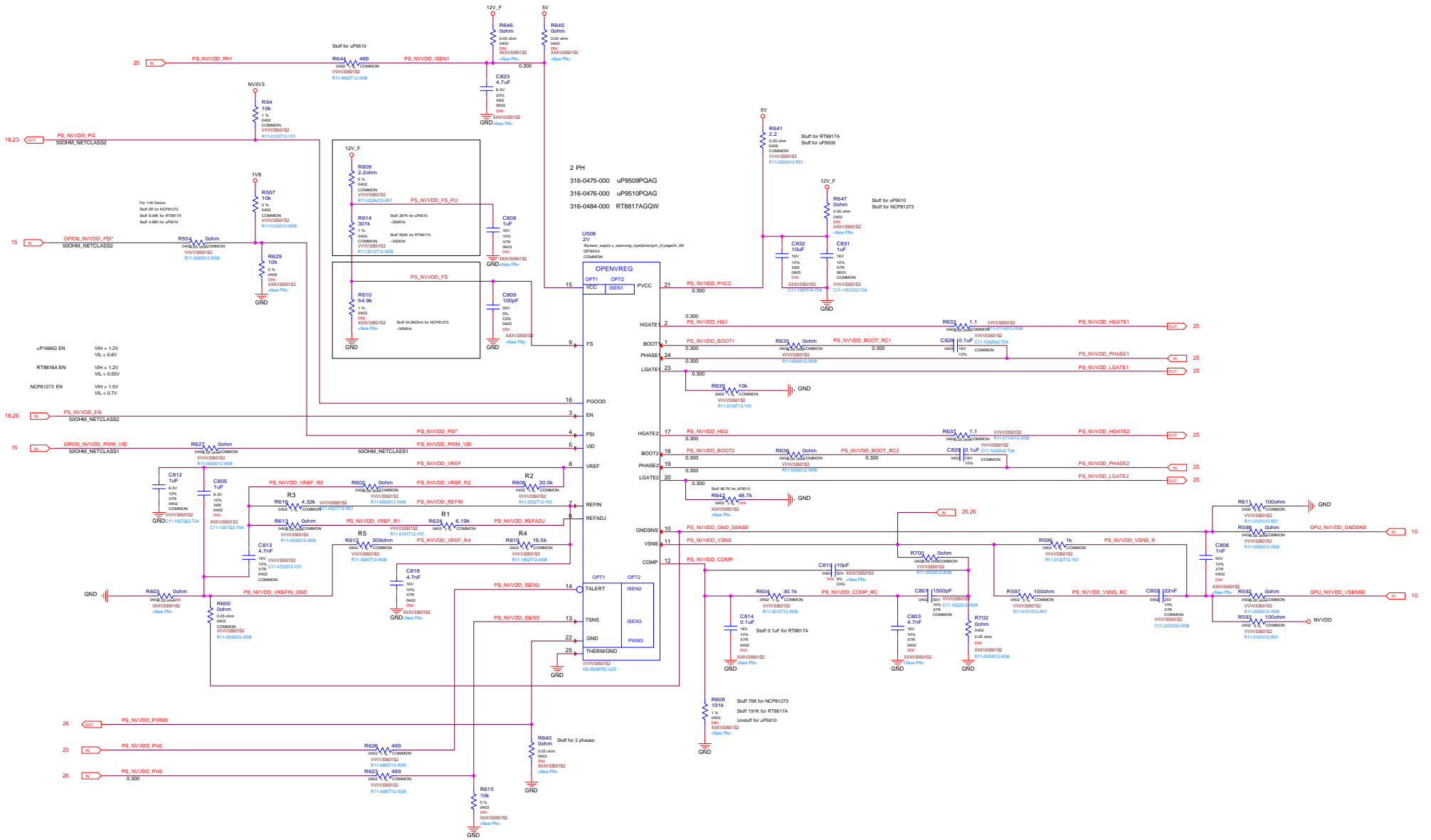
	$V_{out} = V_{ref} * (1 + 0.002)$
$V_{ref} = 0.6V$:	$1.50V = 0.6V * (1 + 0.665)$ $1.55V = 0.6V * (1 + 0.634)$
$V_{ref} = 0.8V$:	$1.50V = 0.8V * (1 + 0.912)$ $1.55V = 0.8V * (1 + 0.875)$

	$V_{out} = V_{ref} * (1 + R2/R1)$
$V_{ref} = 0.6V:$	$1.50V = 0.6V * (1 + R2/R1)$ $1.55V = 0.6V * (1 + R2/R1)$ $1.36V = 0.6V * (1 + R2/R1)$
$V_{ref} = 0.8V:$	$1.50V = 0.8V * (1 + R2/R1)$ $1.55V = 0.8V * (1 + R2/R1)$ $1.36V = 0.8V * (1 + R2/R1)$

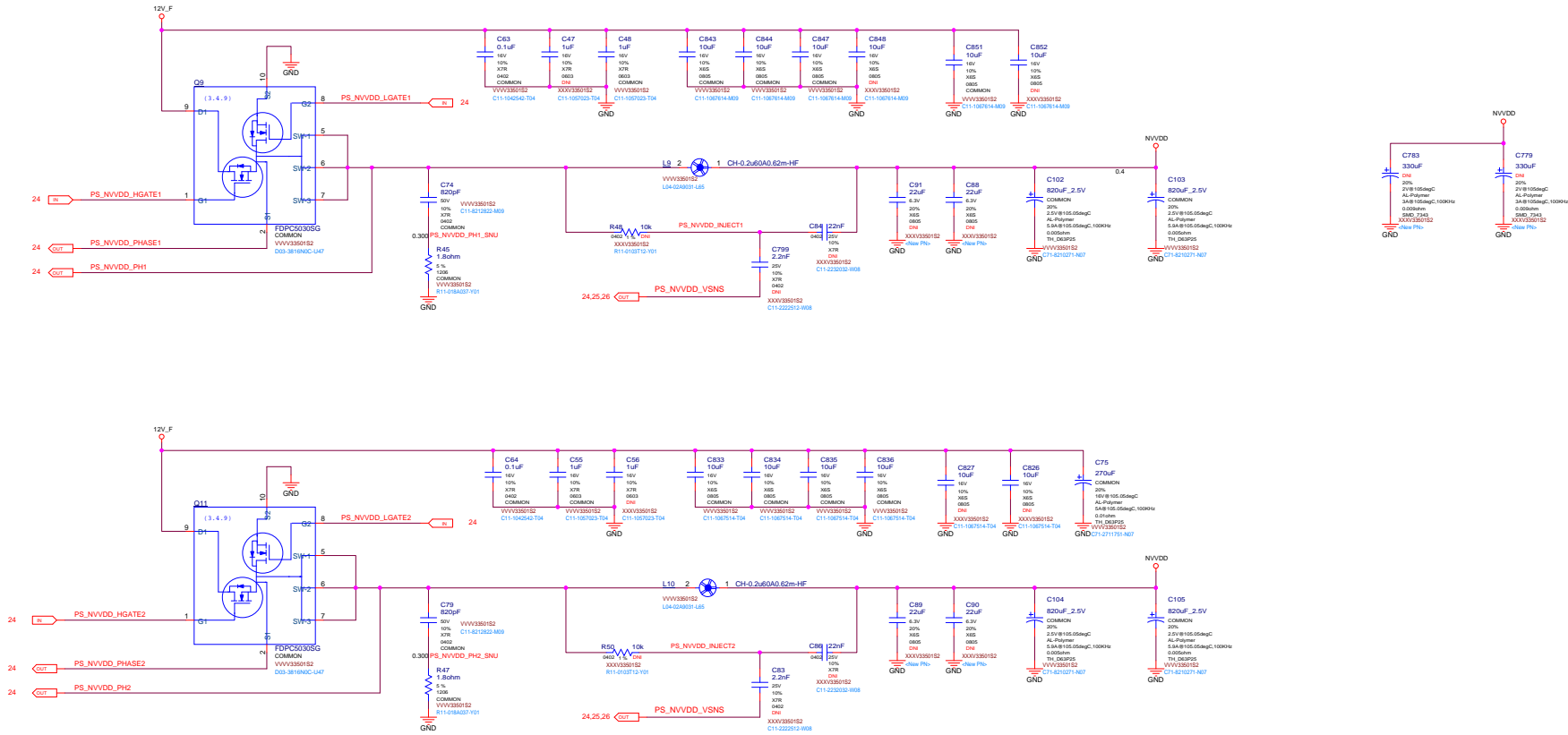
PS	Fonc	Vinf	Tot
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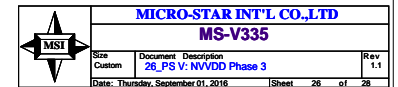
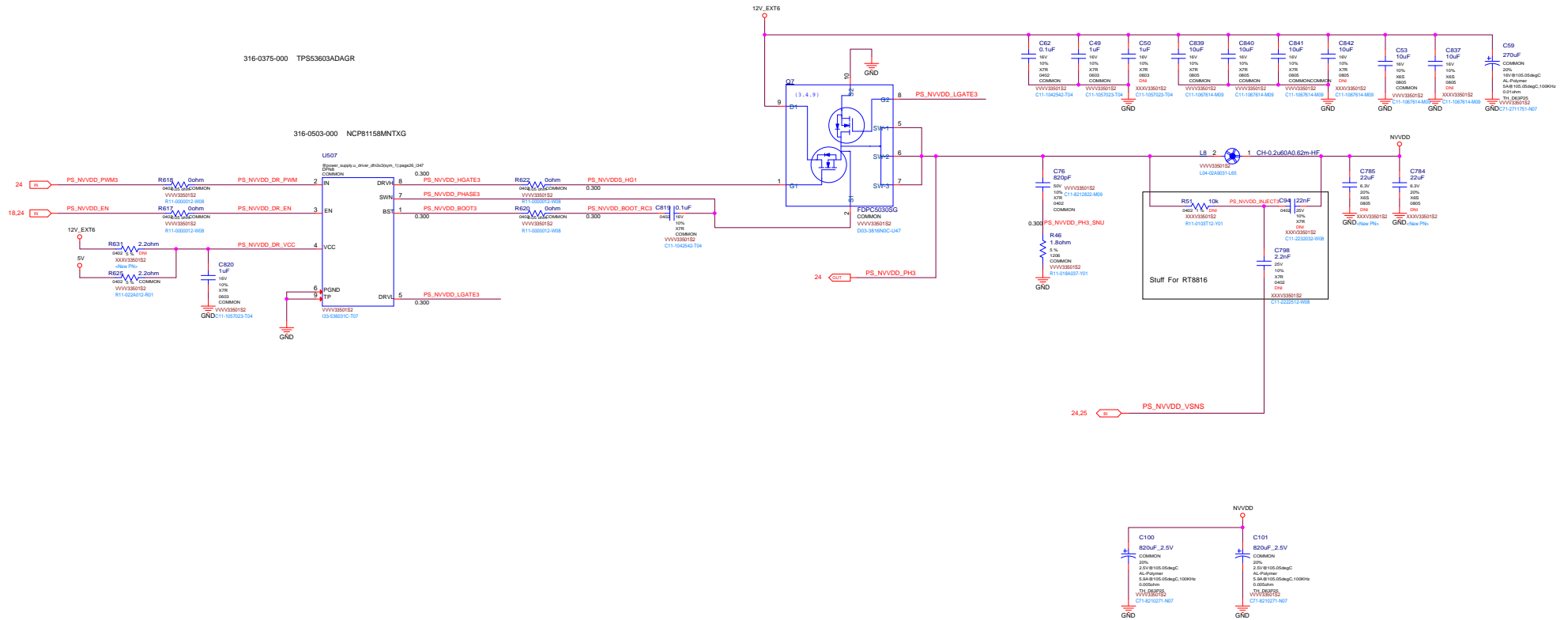


PS V: NVVDD OVR2+1

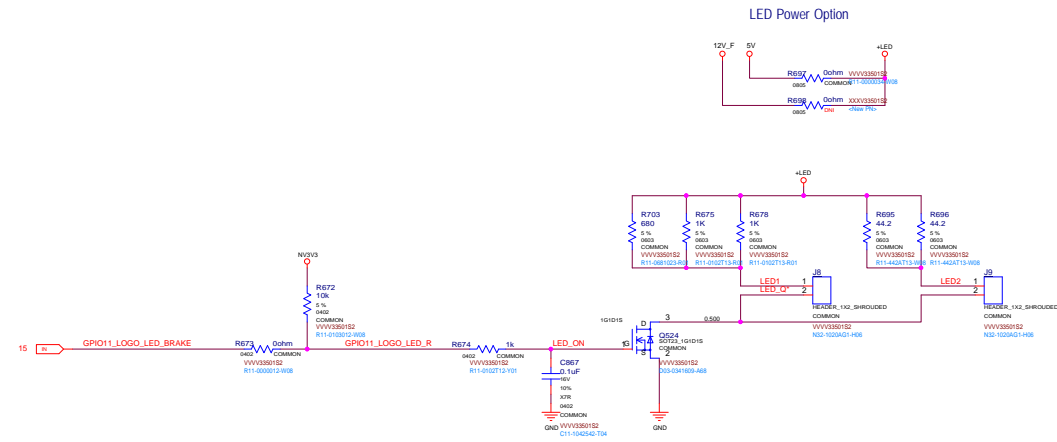


PS V: NVVDD Phase 1,2





Logo LED



Mechanical: Bracket/Thermal Solution

Brackets:

