NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X

PCI DEVICE ID 0X0=0X201 FOR NV20.

NVVDD SET TO: 1.52V
FBVDD SET TO: 3.47V
FBVDDQ SET TO: 2.631V

HISTORY REVISION:

X00: Based on P50-A06
- See change list in 149- file.
- Set FBVDDQ=2.59V

P50-A07-X01:

- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

P50-A08:

X04: - Delay PLL_VDD to come up after NVVDD.
X05: - Added 1UF accross R257.
X06: - Removed X04-5 above, added a switcher generated PLL delay option.
- SSENA cap for 2nd SW changed to 1UF.
- A05 Si, NVVDD=1.52V

P50-A09:

X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.
X03: - Added option to pull up power good to 12V
ECO1235: - Changed R841 PU to 10K (from 4.7K)

P50-A10: Removed unintended shorts between the analog ground and the digital ground (layout affected only).

P50-A11: Isolate analog and chassis GND from the main digital GND.
Generate clean 3.3V onboard (3.3VL), used on TV, TMDS and DAC/PLL.
Added 100R resistor on each of the lower FET in series with 680pf.
Removed Shunt Regulator TL431 used previously for external TMDS.
RGB filters are now back to P50-A09 style.
Removed SLI connector.
Added Linear bypass option resistor.
Reference PVCC1 and PVCC2 filtering caps to PGND pin (digital GND).
All plane bridge "X" components will be initially stuffed with 0R resistors.
Power Supply power sequencing to remain as P50-A09 style.
X76 is where A11 and B00 are brahced off.
B00 is official after Dell's review.

B00-X01: R241 and R242 silkscreens are swapped. The bd may look like R241=NOSTUFF and R242=STUFF (but it's the other way around: BOM is correct).

B00-X02:
Added diff pairs parallel terminations (Res, 0603, 300R)
Populated C897 with 150uF to lower DFP supply noise.

C00: Added 700mA circuit from 5V to 3.3V

B02: Cost reduced, using thru hole parts on PS and delete series termination resistors.
Removed catch diodes from PS page.
Updated TH inductor footprints "ind_t2_295_610"
Corrected Document number and NO STUFF on 3.3V Power Patch.
Set FBVDDQ to 2.631V
Stuff Fan circuit for now.

B03 : 1. Added L807 to connect PLL_VDD_SW to FBVDD
2. Changed R259 and R261 connected to PLL_VDD_SW net created, was connected to 3.3VL
3. Added two more ground termination 0-ohm resistors X13 and X14.
ECO 2070
4. Changed R821, R827, R814 to NO STUFF. Changed C823, C826 and C810 to 2.2K ohm Resistor.
5. Changed R540-R547, R556-R563 to 220 ohm, HYNIX only
6. Changed memory Strapping notes for Hynix and ESMT memories.
7. Created assemblies for HYNIX and ESMT.

{Item}\t{Quantity}\t{Reference}\t{Source Package} {USR DFINE} {Value}\t{NVPN}\t{MAIN}\t{P56CX871}\t{Assembly}
{Assembly}{Source Package} {Value}{PN}{AVL1}{AVL2}{AVL3}{AVL4}{AVL5}

0. TOP PAGE

NV20, 4MX16 DDR 64MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X

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NVIDIA Corporation

602-P0050-0000-B03

Size	CAGE Code	DWG NO	Rev
C			-

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Scale

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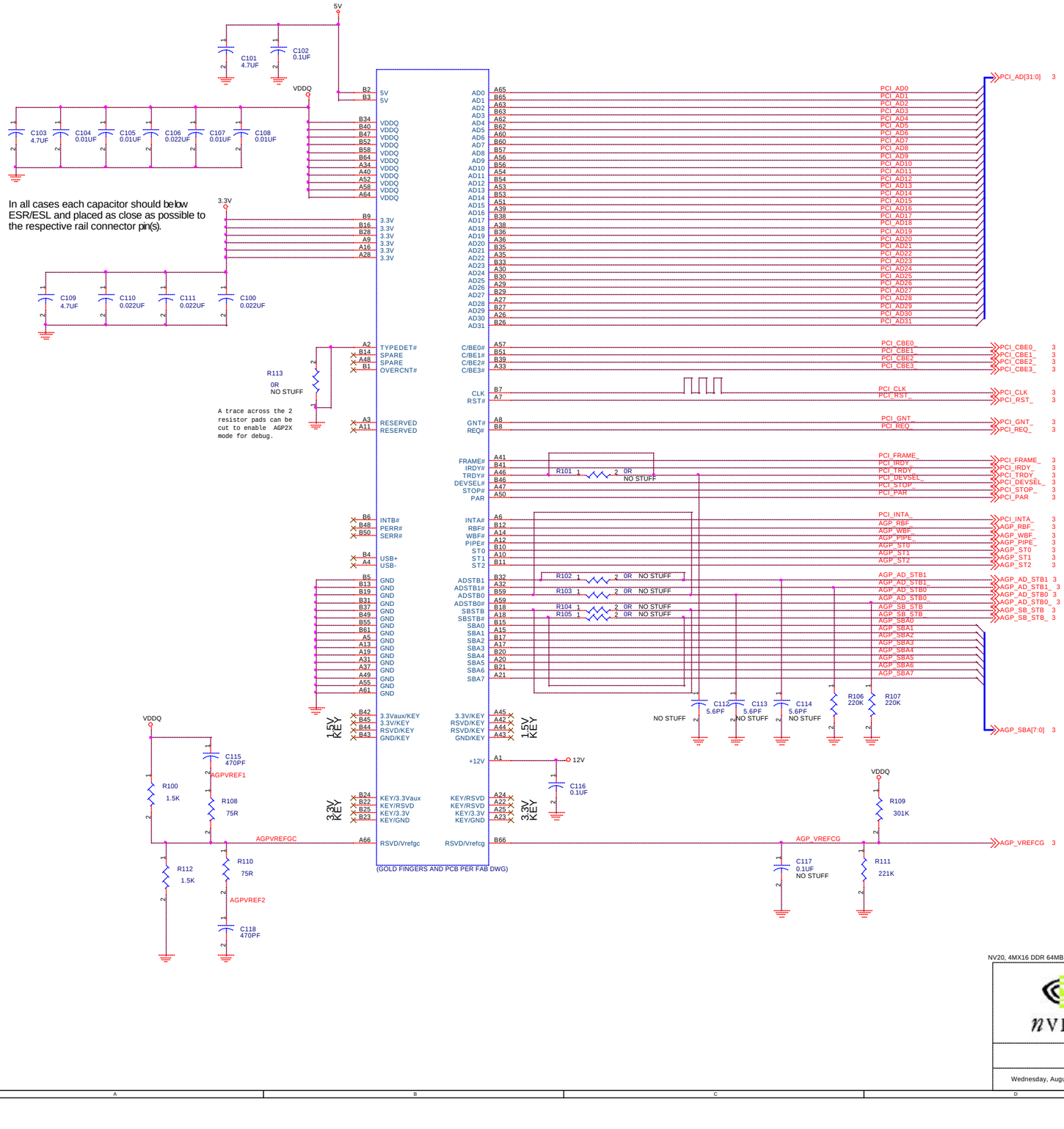

1.1 BUS I/O

NV20, 4MX16 DDR 64MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X

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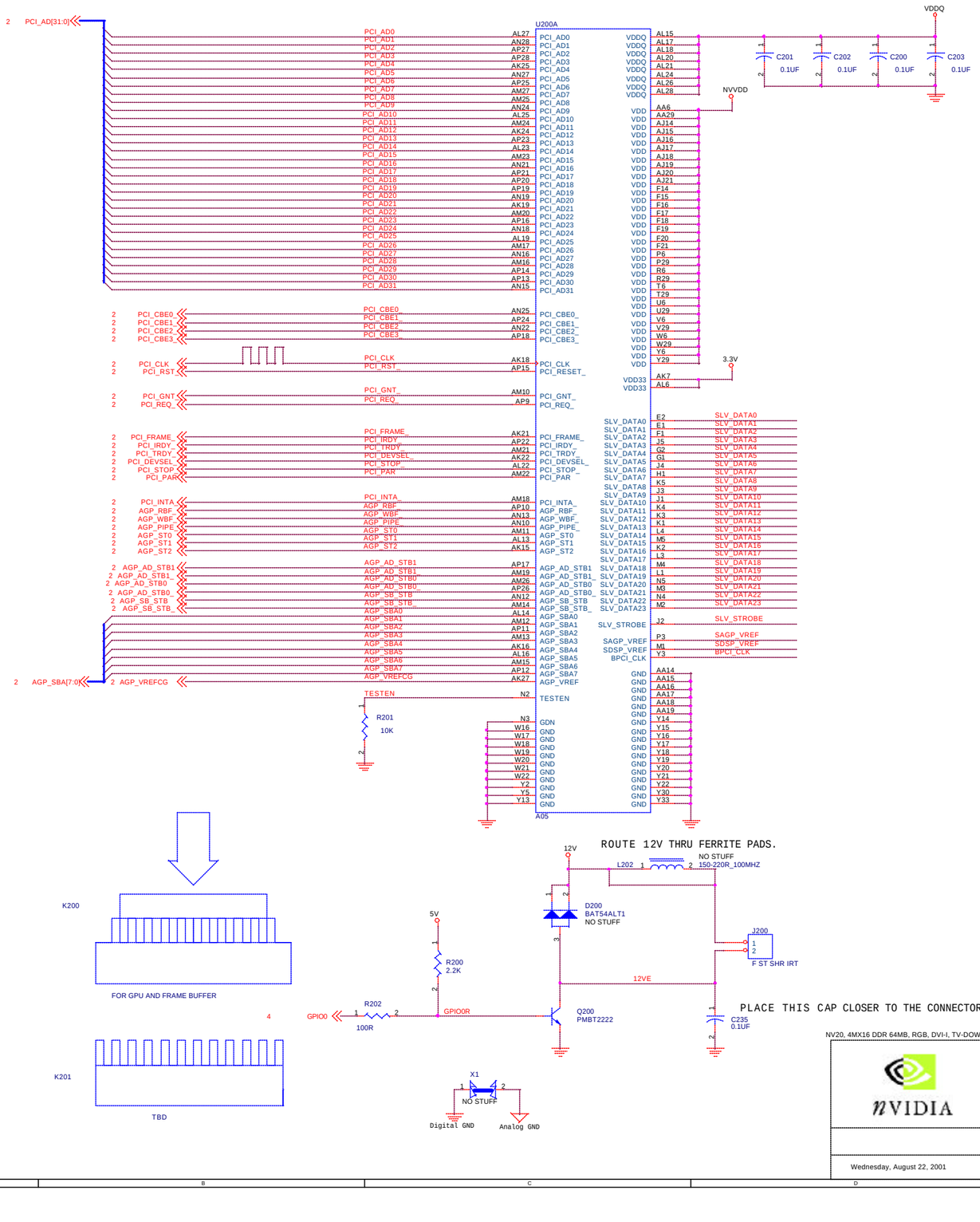

2.1 NV20 HOST

NV20, 4MX16 DDR 64MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X

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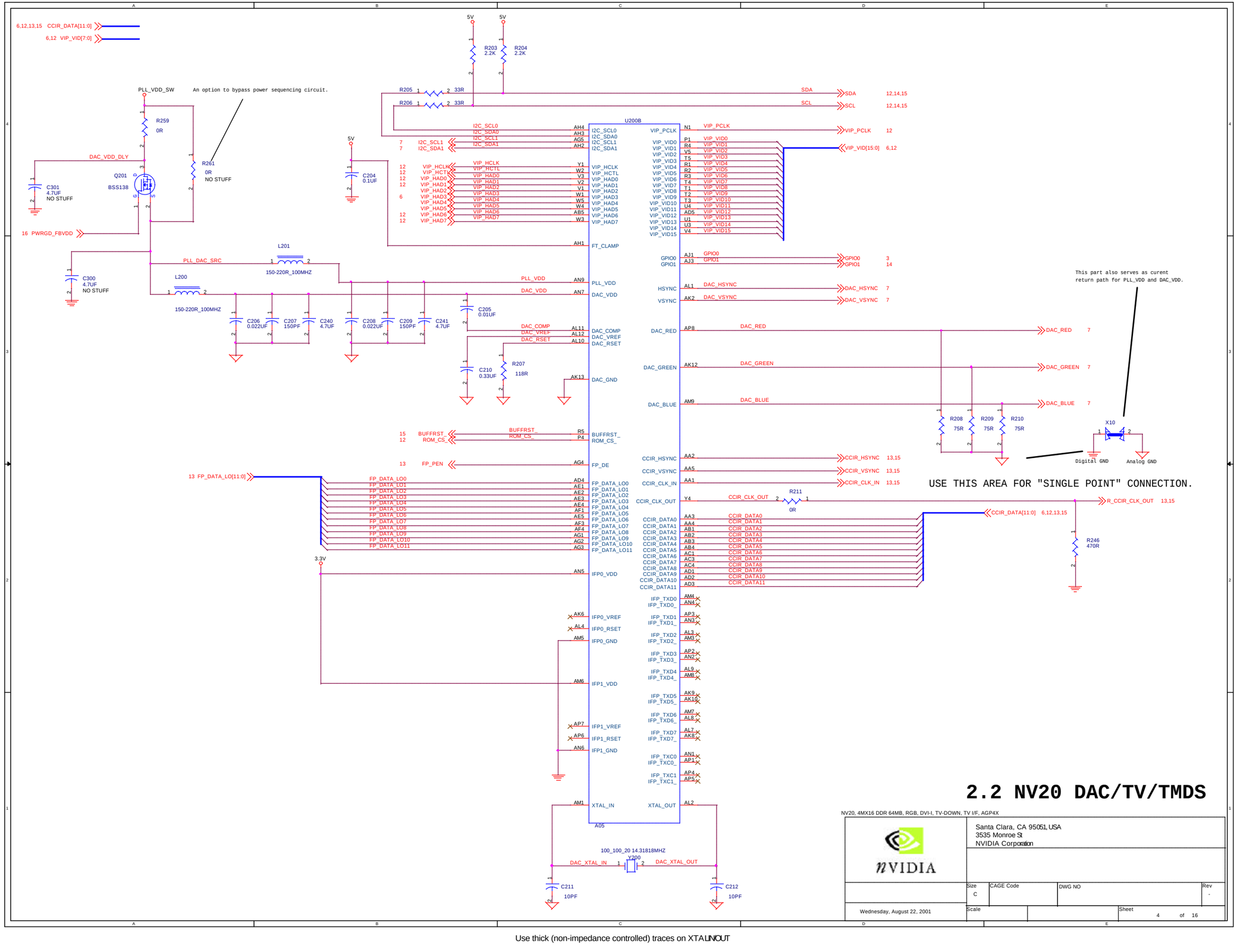

2.2 NV20 DAC/TV/TMDS

NV20, 4MX16 DDR 64MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X

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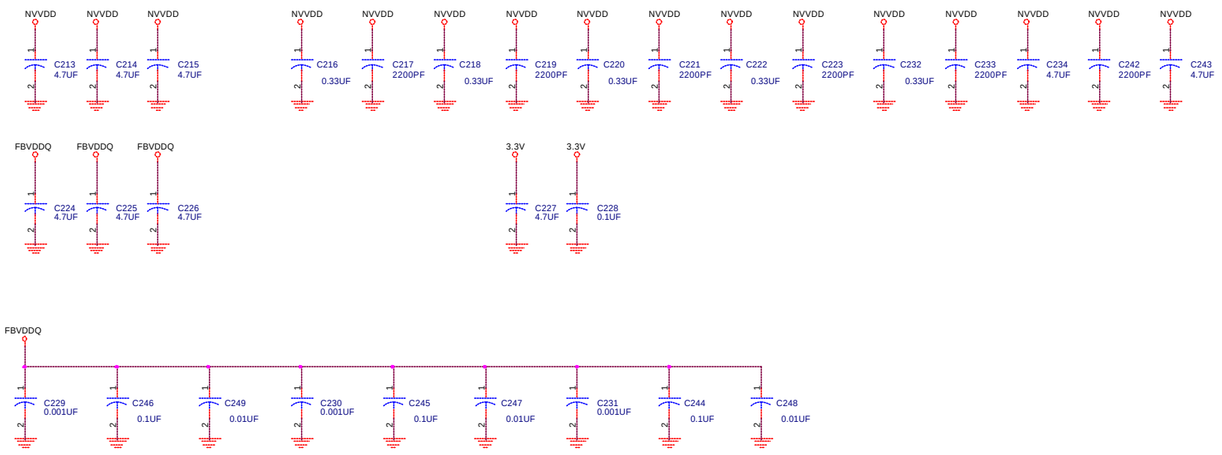
Use thick (non-impedance controlled) traces on XTALIN/OUT



2.3 NV20 DECOUPLING

NV20, 4MX16 DDR 64MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X

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Scale

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4,12,13,15 CCIR_DATA[11:0]
4,12 VIP_VID[15:0]
4,13 FP_DATA_LO[11:0]

4,12 VIP_HAD0
4,12 VIP_HAD1
4 VIP_HAD2
4 VIP_HAD3
4 VIP_HAD4
4 VIP_HAD5
4,12 VIP_HAD6
4,12 VIP_HAD7

3.3V

CCIR_DATA0 R212 2 10K
[0] STRAP_AD_SWAP
STRAP_AD_SWAP=0 : PCIAD bus [31:0] swapped
STRAP_AD_SWAP=1 : PCIAD bus [31:0] normal

CCIR_DATA5 R213 2 10K
[1] STRAP_SUB_VENDOR
STRAP_SUB_VENDOR=0 : System BIOS
STRAP_SUB_VENDOR=1 : Adaptor BIOS

[11] STRAP_FAST_WRITES
STRAP_FAST_WRITES=0 : FAST WRITE ENABLED
STRAP_FAST_WRITES=1 : FAST WRITE DISABLED

R214 2 10K VIP_VID9 R215 2 10K
NO STUFF

R216 2 10K VIP_VID11 R217 2 10K
NO STUFF
VID[11:10] PCI_DEV_ID
PCI_DEV_ID = 0x201 (Default)

R218 2 10K VIP_VID10 R219 2 10K
NO STUFF

R220 2 10K VIP_VID6 R221 2 10K
NO STUFF
[VID6:CCIR11] STRAP_TVMODE
STRAP_TVMODE=0 : PAL
STRAP_TVMODE=1 : NTSC
STRAP_TVMODE=2 : Reserved
STRAP_TVMODE=3 : Disabled

R222 2 10K CCIR_DATA11 R223 2 10K
NO STUFF

R224 2 10K CCIR_DATA10 R225 2 10K
NO STUFF
[CCIR10] STRAP_CRYSTAL
STRAP_CRYSTAL=0 : 13.50000MHz
STRAP_CRYSTAL=1 : 14.31818MHz

R226 2 10K CCIR_DATA9 R227 2 10K
NO STUFF
[9:6] STRAP_RAM_TYPE
1010 4Mx16 DDR ESMT/UMC
1110 4Mx16 DDR Hynix/Hyundai

SUB BOM FOR THE MEMORY TYPE WILL CALL OUT THE STUFF OPTIONS FOR R226-R233

R228 2 10K CCIR_DATA8 R229 2 10K
NO STUFF

R230 2 10K CCIR_DATA7 R231 2 10K
NO STUFF

R232 2 10K CCIR_DATA6 R233 2 10K
NO STUFF

R234 2 10K VIP_VID7 R235 2 10K
NO STUFF
[VID7] STRAP_AGP4X
STRAP_AGP4X=0 : AGP4X transfers enabled
STRAP_AGP4X=1 : AGP2X only

R236 2 10K VIP_VID8 R237 2 10K
NO STUFF
[VID8] STRAP_AGPSBA
STRAP_AGPSBA=0 : sideband enabled
STRAP_AGPSBA=1 : pipelined only transfers
Set SideBand OFF in the first prototype built.12/21/2K

R238 2 10K VIP_VID13 R239 2 10K
NO STUFF
[VID13] FP_INTERFACE
0=24 bit FP
1=12 bit FP

VIP_VID12 R240 2 10K
[VID12] AGP MODE
STRAP_HOST=1 : AGP Mode

R241 2 10K VIP_HAD3 R242 2 10K
NO STUFF
Strap_user[0]
Video Module Sense bit = TBD.

R243 2 10K VIP_VID4
BRIDGE_EN

VIP_VID3 R244 2 10K
MULTI_AGP

VIP_VID5 R245 2 10K
MULTI_IO

R249 2 10K VIP_VID15 R247 2 10K
NO STUFF
VID[15:14] Strap_FB[1:0]:
00 = 64MB.

R250 2 10K VIP_VID14 R248 2 10K
NO STUFF

2.4 NV20 HOST STRAPS

NV20, 4MX16 DDR 64MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X

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3.1 DAC I/O

Single point connection for digital and chassis GND.

This part serves as curent return path for BUFFHSYNC, BUFFVSYNC and SIIAVCC.

This part serves as curent return path for DDC+5V, DDCSCL and DDCSDA

BRACKET VGA (1.102), SVIDEO (2.053), DVI (3.122)

F RA VESA BLUE IRT

NV20, 4MX16 DDR 64MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X

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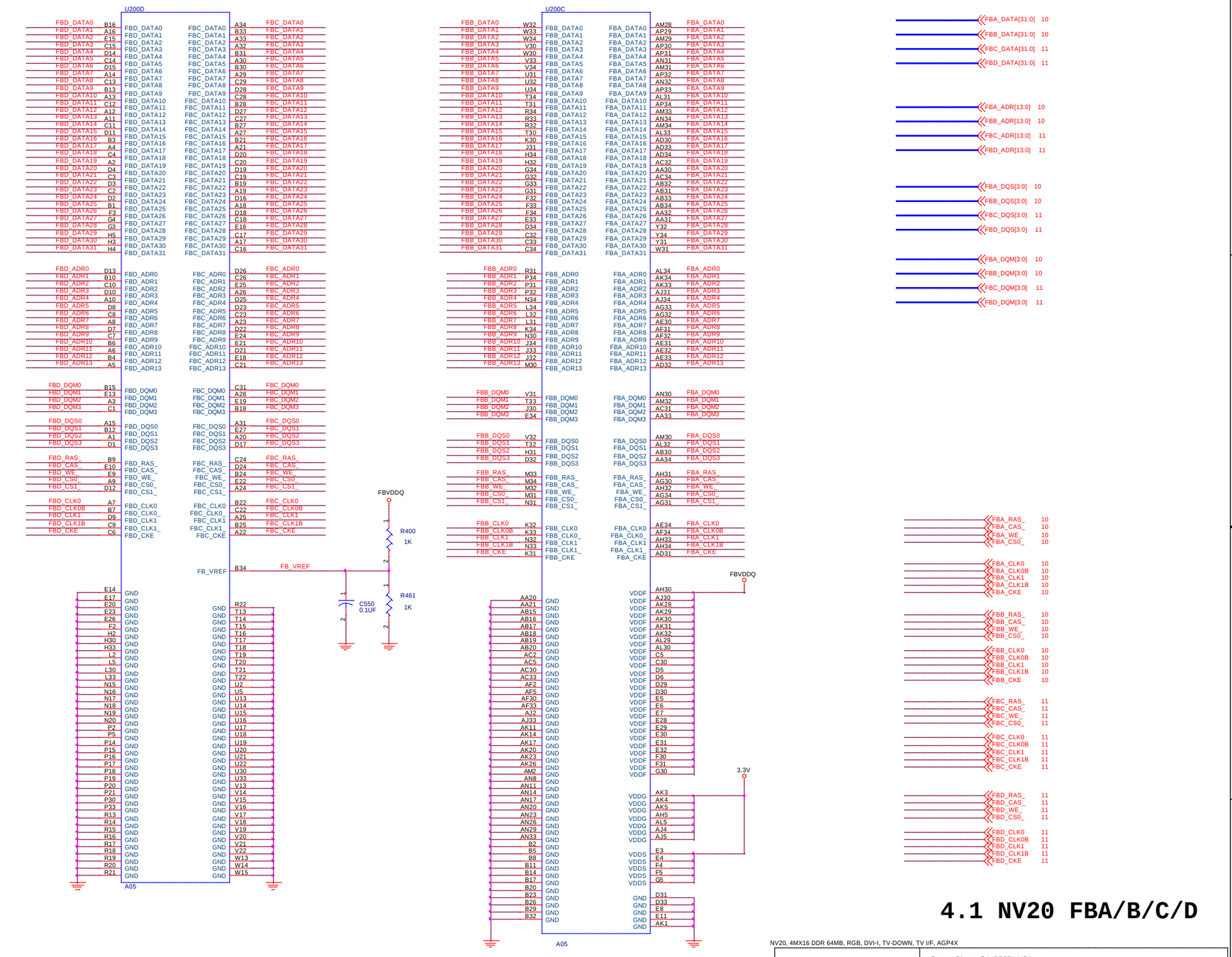
U200D
FBD_DATA0 B16
FBD_DATA1 A16
FBD_DATA2 E15
FBD_DATA3 C15
FBD_DATA4 D14
FBD_DATA5 C14
FBD_DATA6 D15
FBD_DATA7 A14
FBD_DATA8 C13
FBD_DATA9 B13
FBD_DATA10 A13
FBD_DATA11 C12
FBD_DATA12 A12
FBD_DATA13 A11
FBD_DATA14 C11
FBD_DATA15 D11
FBD_DATA16 B3
FBD_DATA17 A4
FBD_DATA18 C4
FBD_DATA19 A2
FBD_DATA20 D4
FBD_DATA21 C3
FBD_DATA22 D3
FBD_DATA23 C2
FBD_DATA24 D2
FBD_DATA25 B1
FBD_DATA26 F3
FBD_DATA27 G4
FBD_DATA28 G3
FBD_DATA29 H5
FBD_DATA30 H3
FBD_DATA31 H4
FBD_ADR0 D13
FBD_ADR1 B10
FBD_ADR2 C10
FBD_ADR3 D10
FBD_ADR4 A10
FBD_ADR5 D8
FBD_ADR6 C8
FBD_ADR7 A8
FBD_ADR8 D7
FBD_ADR9 C7
FBD_ADR10 B6
FBD_ADR11 A6
FBD_ADR12 B4
FBD_ADR13 A5
FBD_DQM0 B15
FBD_DQM1 E13
FBD_DQM2 A3
FBD_DQM3 C1
FBD_DQS0 A15
FBD_DQS1 B12
FBD_DQS2 A1
FBD_DQS3 D1
FBD_RAS_ B9
FBD_CAS_ E10
FBD_WE_ E9
FBD_CS0_ A9
FBD_CS1_ D12
FBD_CLK0 A7
FBD_CLK0B B7
FBD_CLK1 D9
FBD_CLK1B C9
FBD_CKE C6
FBD_DATA0 A34
FBD_DATA1 B33
FBD_DATA2 A33
FBD_DATA3 A32
FBD_DATA4 B31
FBD_DATA5 A30
FBD_DATA6 B30
FBD_DATA7 A29
FBD_DATA8 C29
FBD_DATA9 D28
FBD_DATA10 C28
FBD_DATA11 B28
FBD_DATA12 D27
FBD_DATA13 C27
FBD_DATA14 B27
FBD_DATA15 A27
FBD_DATA16 B21
FBD_DATA17 A21
FBD_DATA18 D20
FBD_DATA19 C20
FBD_DATA20 D19
FBD_DATA21 C19
FBD_DATA22 B19
FBD_DATA23 A19
FBD_DATA24 D16
FBD_DATA25 A18
FBD_DATA26 D18
FBD_DATA27 C18
FBD_DATA28 E16
FBD_DATA29 C17
FBD_DATA30 A17
FBD_DATA31 C16
FBD_ADR0 D26
FBD_ADR1 C26
FBD_ADR2 E25
FBD_ADR3 A26
FBD_ADR4 D25
FBD_ADR5 D23
FBD_ADR6 C23
FBD_ADR7 A23
FBD_ADR8 D22
FBD_ADR9 E24
FBD_ADR10 E21
FBD_ADR11 D21
FBD_ADR12 E18
FBD_ADR13 C21
FBD_DQM0 C31
FBD_DQM1 A28
FBD_DQM2 E19
FBD_DQM3 B18
FBD_DQS0 A31
FBD_DQS1 E27
FBD_DQS2 A20
FBD_DQS3 D17
FBD_RAS_ C24
FBD_CAS_ D24
FBD_WE_ B24
FBD_CS0_ E22
FBD_CS1_ A24
FBD_CLK0 B22
FBD_CLK0B C22
FBD_CLK1 A25
FBD_CLK1B B25
FBD_CKE A22
FB_VREF B34
E14 GND
E17 GND
E20 GND
E23 GND
E26 GND
F2 GND
H2 GND
H30 GND
H33 GND
L2 GND
L5 GND
L30 GND
L33 GND
N15 GND
N16 GND
N17 GND
N18 GND
N19 GND
N20 GND
P2 GND
P5 GND
P14 GND
P15 GND
P16 GND
P17 GND
P18 GND
P19 GND
P20 GND
P21 GND
P30 GND
P33 GND
R13 GND
R14 GND
R15 GND
R16 GND
R17 GND
R18 GND
R19 GND
R20 GND
R21 GND
R22 GND
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T15 GND
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T17 GND
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T20 GND
T21 GND
T22 GND
U2 GND
U5 GND
U13 GND
U14 GND
U15 GND
U16 GND
U17 GND
U18 GND
U19 GND
U20 GND
U21 GND
U22 GND
U30 GND
U33 GND
V13 GND
V14 GND
V15 GND
V16 GND
V17 GND
V18 GND
V19 GND
V20 GND
V21 GND
V22 GND
W13 GND
W14 GND
W15 GND
A05
FBVDDQ
R400
1K
FB_VREF
C550
0.1UF
R461
1K
U200C
FBB_DATA0 W32
FBB_DATA1 W33
FBB_DATA2 W34
FBB_DATA3 V30
FBB_DATA4 W30
FBB_DATA5 V33
FBB_DATA6 V34
FBB_DATA7 U31
FBB_DATA8 U32
FBB_DATA9 U34
FBB_DATA10 T34
FBB_DATA11 T31
FBB_DATA12 R34
FBB_DATA13 R33
FBB_DATA14 R32
FBB_DATA15 T30
FBB_DATA16 K30
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FBB_DATA19 H32
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FBB_ADR4 N34
FBB_ADR5 L34
FBB_ADR6 L32
FBB_ADR7 L31
FBB_ADR8 K34
FBB_ADR9 N30
FBB_ADR10 J34
FBB_ADR11 J33
FBB_ADR12 J32
FBB_ADR13 M30
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FBB_DQM2 J30
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FBB_DQS1 T32
FBB_DQS2 H31
FBB_DQS3 D32
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FBB_CAS_ M34
FBB_WE_ M32
FBB_CS0_ M31
FBB_CS1_ N31
FBB_CLK0 K32
FBB_CLK0B K33
FBB_CLK1 N32
FBB_CLK1B N33
FBB_CKE K31
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FBA_DATA1 AP29
FBA_DATA2 AM29
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FBA_DATA8 AN32
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FBA_DQM2 AC31
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FBA_DQS3 AA34
FBA_RAS_ AH31
FBA_CAS_ AG30
FBA_WE_ AH32
FBA_CS0_ AG34
FBA_CS1_ AG31
FBA_CLK0 AE34
FBA_CLK0B AF34
FBA_CLK1 AH33
FBA_CLK1B AH34
FBA_CKE AD31
AA20 GND
AA21 GND
AB15 GND
AB16 GND
AB17 GND
AB18 GND
AB19 GND
AB20 GND
AC2 GND
AC5 GND
AC30 GND
AC33 GND
AF2 GND
AF5 GND
AF30 GND
AF33 GND
AJ2 GND
AJ33 GND
AK11 GND
AK14 GND
AK17 GND
AK20 GND
AK23 GND
AK26 GND
AM2 GND
AN8 GND
AN11 GND
AN14 GND
AN17 GND
AN20 GND
AN23 GND
AN26 GND
AN29 GND
AN33 GND
B2 GND
B5 GND
B8 GND
B11 GND
B14 GND
B17 GND
B20 GND
B23 GND
B26 GND
B29 GND
B32 GND
AH30 VDDF
AJ30 VDDF
AK28 VDDF
AK29 VDDF
AK30 VDDF
AK31 VDDF
AK32 VDDF
AL29 VDDF
AL30 VDDF
C5 VDDF
C30 VDDF
D5 VDDF
D6 VDDF
D29 VDDF
D30 VDDF
E5 VDDF
E6 VDDF
E7 VDDF
E28 VDDF
E29 VDDF
E30 VDDF
E31 VDDF
E32 VDDF
F30 VDDF
F31 VDDF
G30 VDDF
AK3 VDDG
AK4 VDDG
AK5 VDDG
AH5 VDDG
AL5 VDDG
AJ4 VDDG
AJ5 VDDG
E3 VDDS
E4 VDDS
F4 VDDS
F5 VDDS
G5 VDDS
D31 GND
D33 GND
E8 GND
E11 GND
AK1 GND
A05
FBVDDQ
3.3V
FBA_DATA[31:0] 10
FBA_DATA[31:0] 10
FBC_DATA[31:0] 11
FBD_DATA[31:0] 11
FBA_ADR[13:0] 10
FBB_ADR[13:0] 10
FBC_ADR[13:0] 11
FBD_ADR[13:0] 11
FBA_DQS[3:0] 10
FBB_DQS[3:0] 10
FBC_DQS[3:0] 11
FBD_DQS[3:0] 11
FBA_DQM[3:0] 10
FBB_DQM[3:0] 10
FBC_DQM[3:0] 11
FBD_DQM[3:0] 11
FBA_RAS_ 10
FBA_CAS_ 10
FBA_WE_ 10
FBA_CS0_ 10
FBA_CLK0 10
FBA_CLK0B 10
FBA_CLK1 10
FBA_CLK1B 10
FBA_CKE 10
FBB_RAS_ 10
FBB_CAS_ 10
FBB_WE_ 10
FBB_CS0_ 10
FBB_CLK0 10
FBB_CLK0B 10
FBB_CLK1 10
FBB_CLK1B 10
FBB_CKE 10
FBC_RAS_ 11
FBC_CAS_ 11
FBC_WE_ 11
FBC_CS0_ 11
FBC_CLK0 11
FBC_CLK0B 11
FBC_CLK1 11
FBC_CLK1B 11
FBC_CKE 11
FBD_RAS_ 11
FBD_CAS_ 11
FBD_WE_ 11
FBD_CS0_ 11
FBD_CLK0 11
FBD_CLK0B 11
FBD_CLK1 11
FBD_CLK1B 11
FBD_CKE 11
4.1 NV20 FBA/B/C/D
NV20, 4MX16 DDR 64MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X
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CAGE Code
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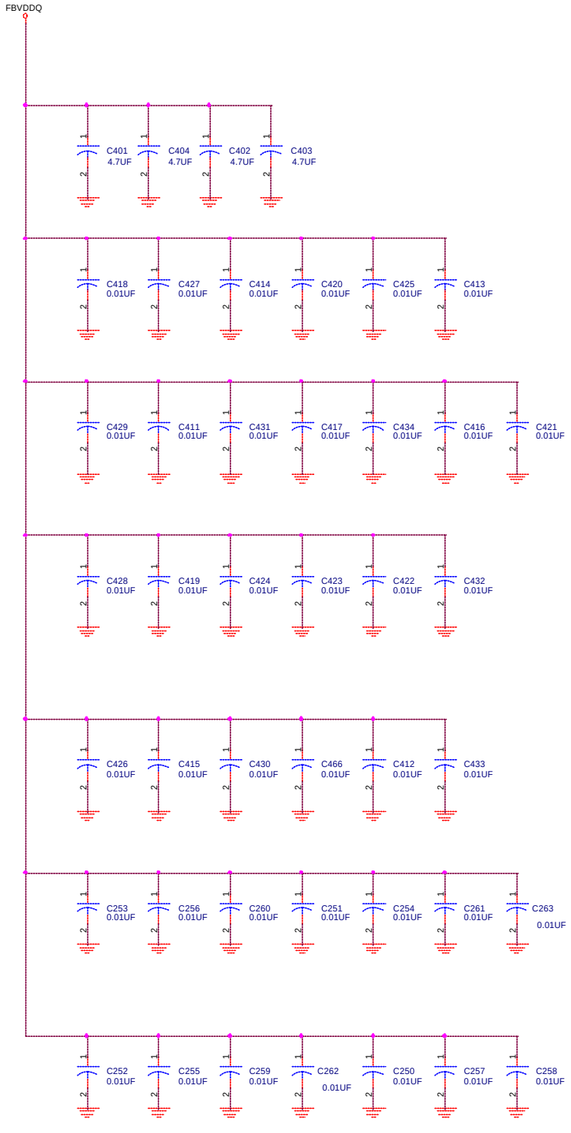

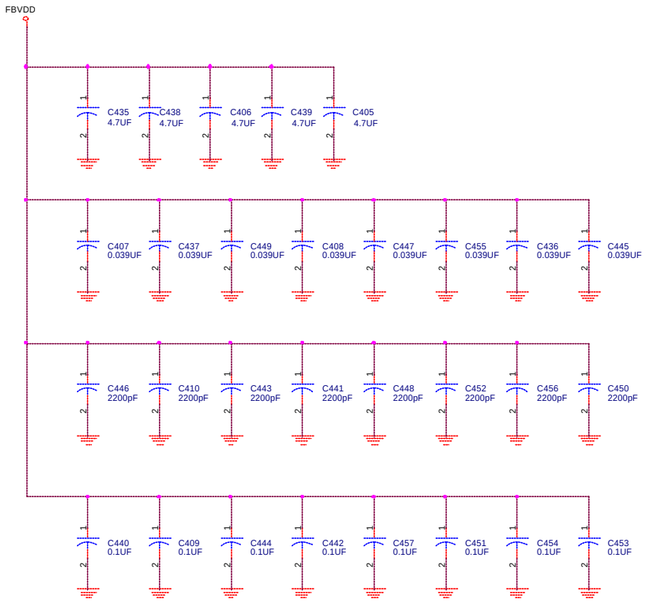

4.2 FB DECOUPLING 4MX16 SDRAM

NV20, 4MX16 DDR 64MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X

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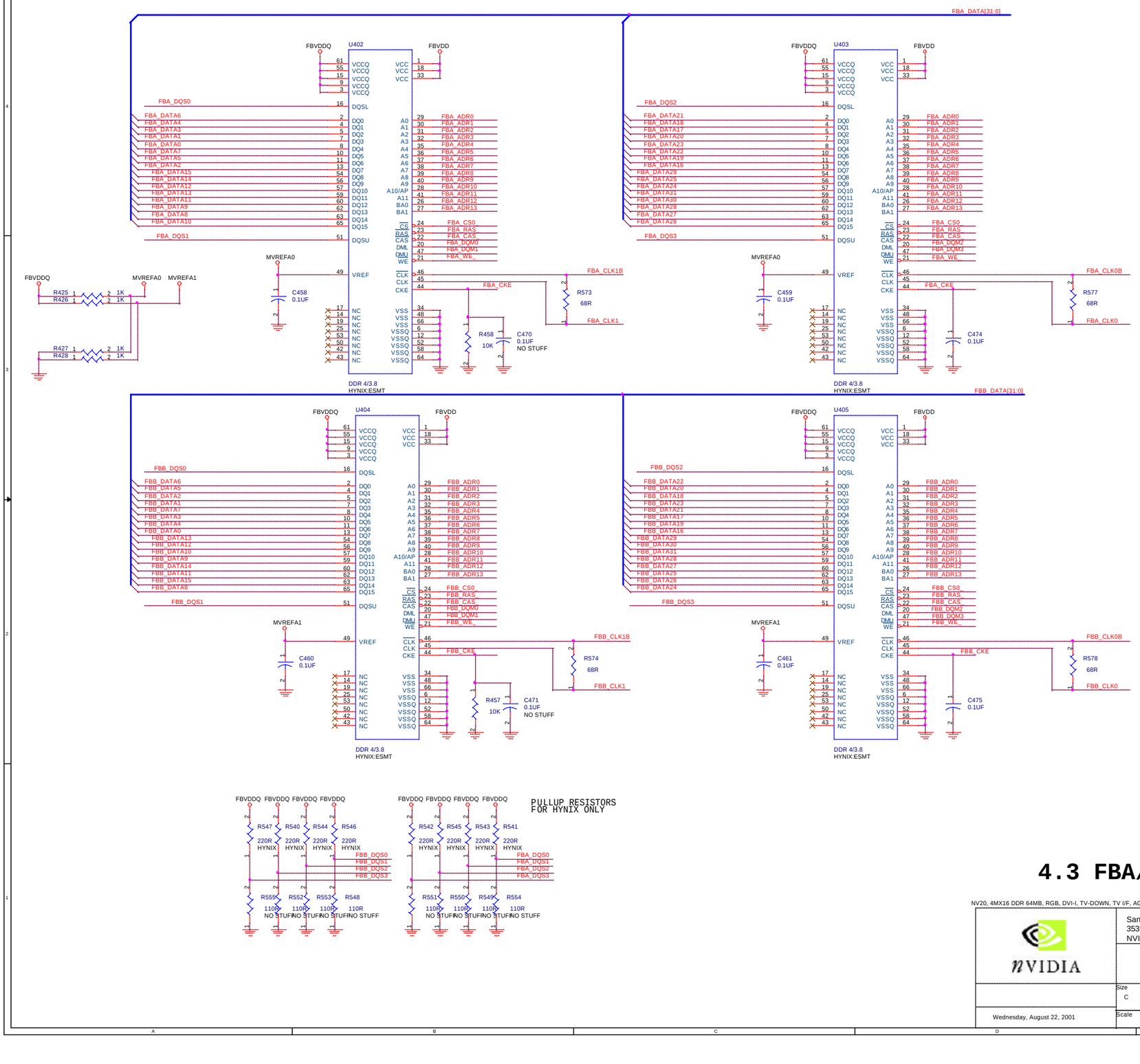

4.3 FBA/B DDR 4MX16 SDRAM

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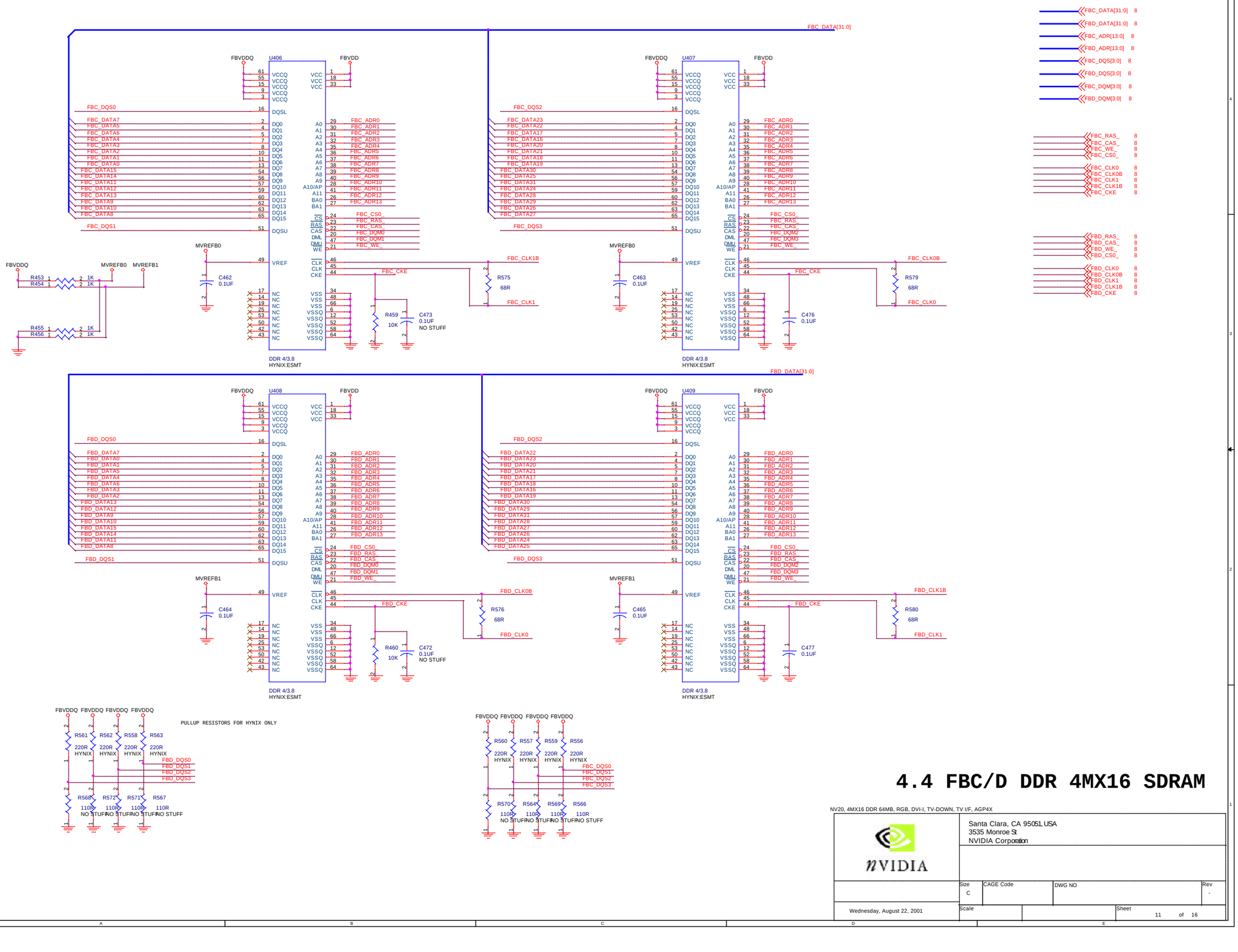

4.4 FBC/D DDR 4MX16 SDRAM

NV20, 4MX16 DDR 64MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X

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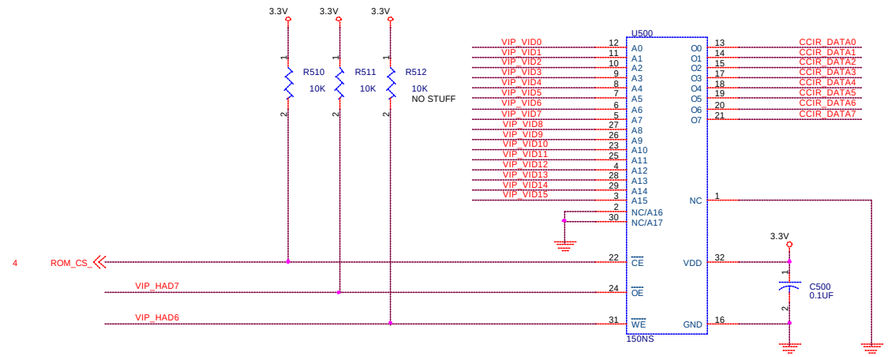
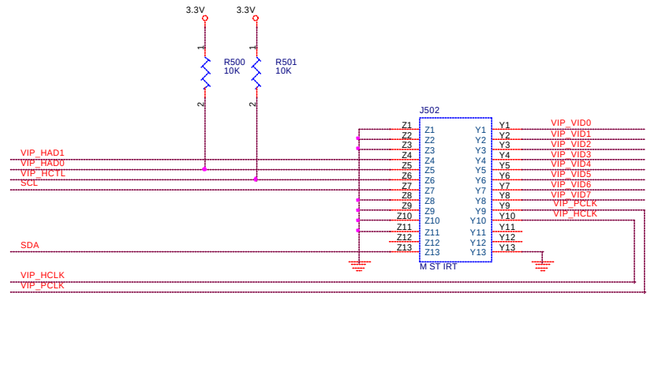
4,6 VIP_VID[15:0]
4 VIP_PCLK
4 VIP_HCLK
4 VIP_HCTL
4 VIP_HAD0
4 VIP_HAD1
4 VIP_HAD2
4,6 VIP_HAD3
4 VIP_HAD4
4 VIP_HAD5
4 VIP_HAD6
4 VIP_HAD7
4,6,13,15 CCIR_DATA[11:0]
4,13,15 CCIR_HSYNC
4,13,15 CCIR_VSYNC
4,13,15 CCIR_CLK_IN
4,13,15 R_CCIR_CLK_OUT
4,15 BUFFRST_
4,14,15 SCL
4,14,15 SDA





5.1 ROM VIP & VIDEO IF

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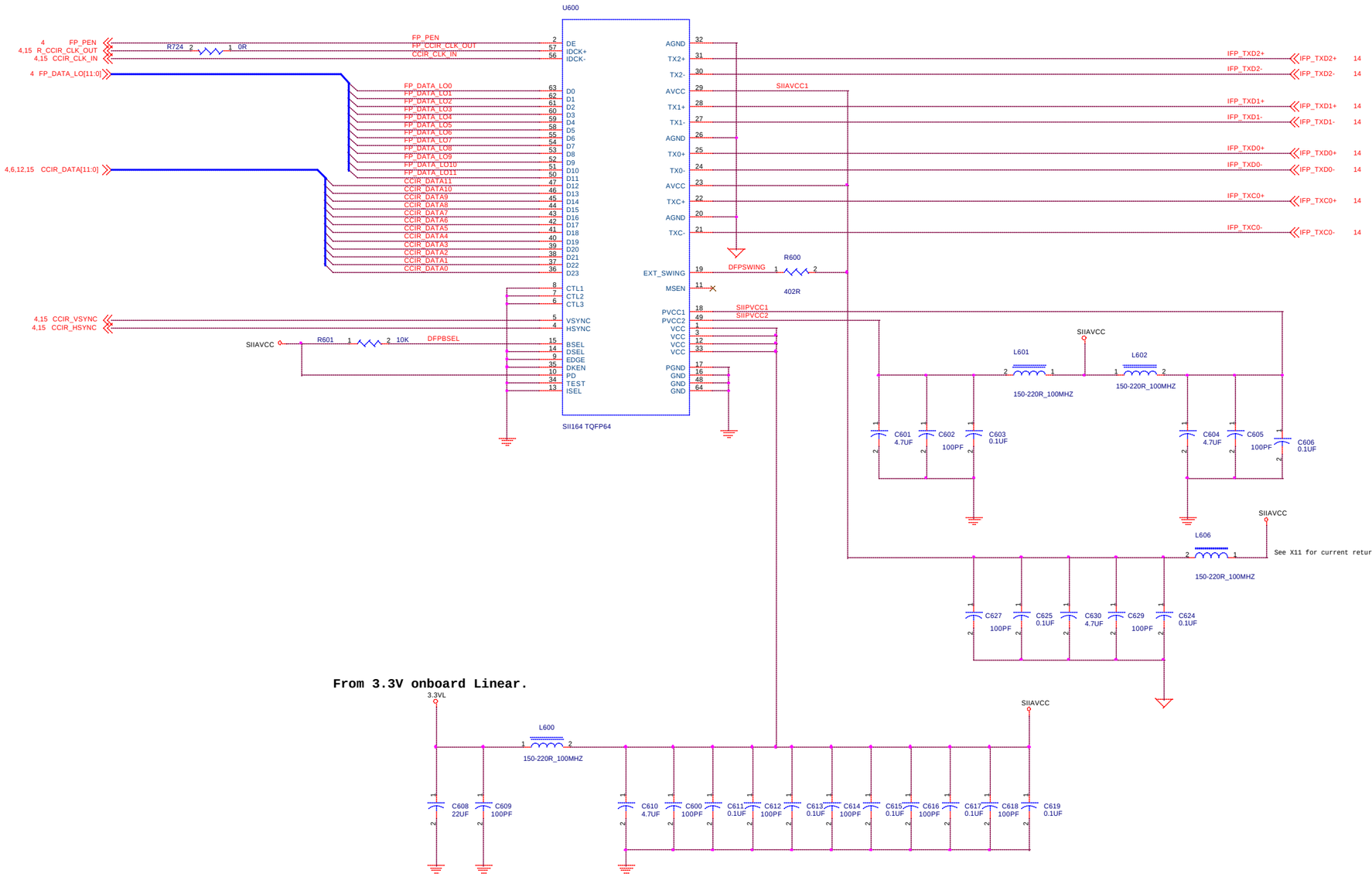

6.1 EXTERNAL DFP/DVI

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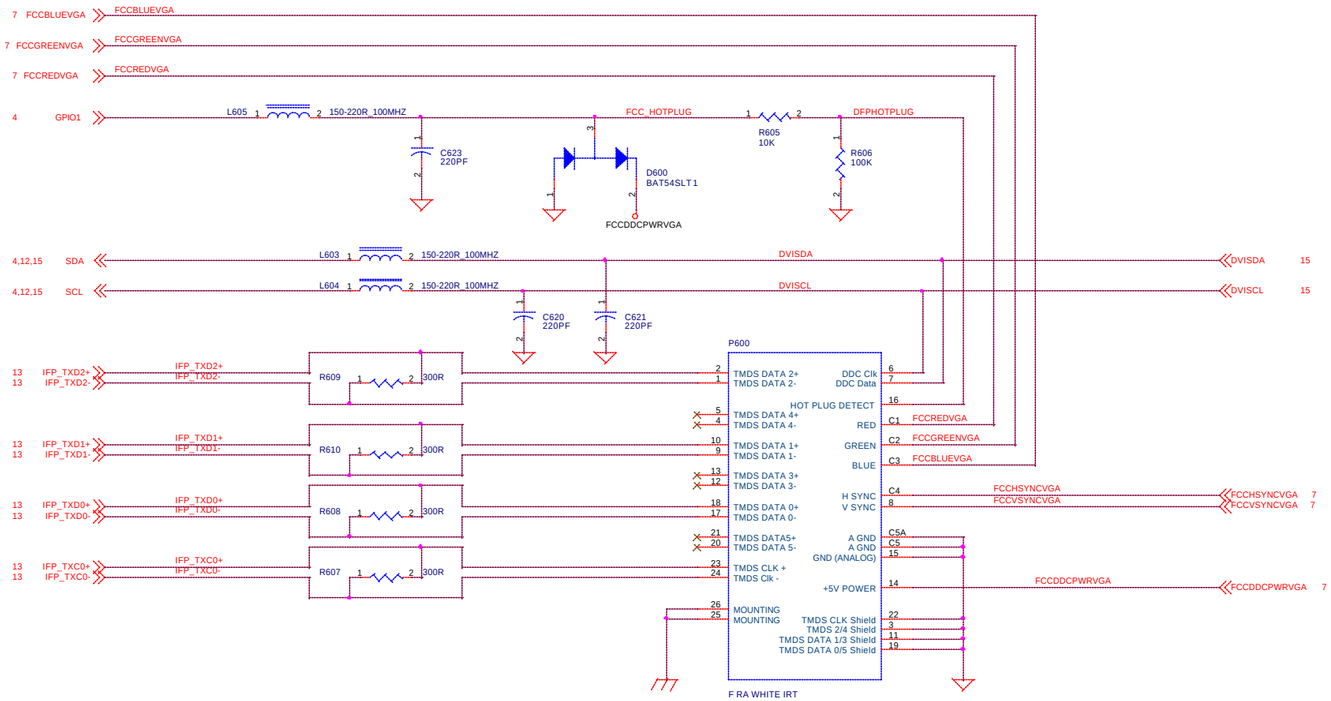
M600

SCREW , HEX FOR DVI CONNECTOR

M601

SCREW , HEX FOR DVI CONNECTOR



6.2 DVI-I I/O

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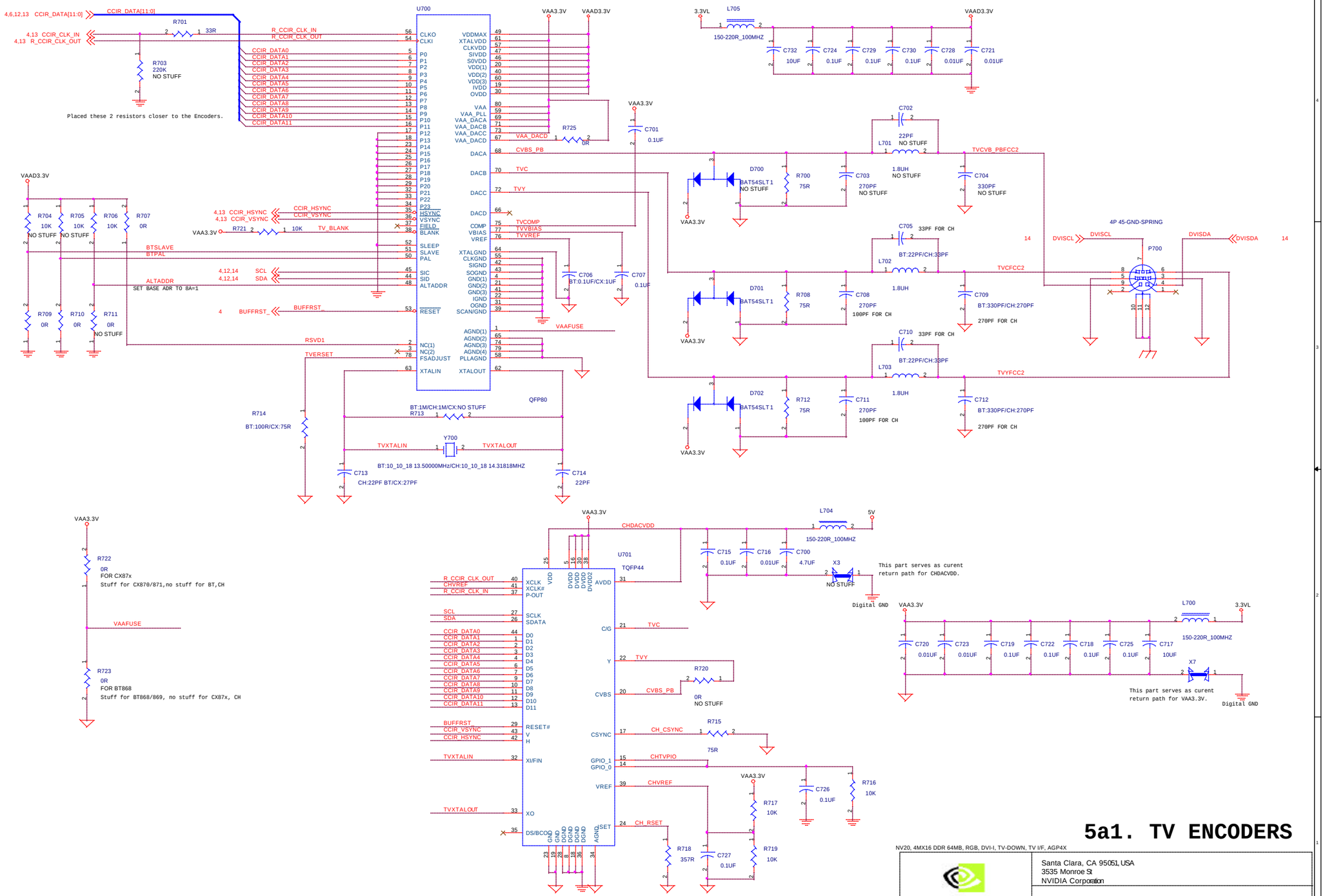

Parts for Chrontel CH7007/8

5a1. TV ENCODERS

NV20, 4MX16 DDR 64MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X

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8.1 NV20 POWER

Vout=1.25V*(1+Rvout/Rgnd)+Rgnd*(Ifb=2ua/10^6)

NVVDD

1.52V

Vout=1.2*((R1+R2)/R2)
Semtech SC1565 SO8
3.3V@500mA
Drop Out 225mV Typ.

Run trace thru resistor pads.

Large copper shape attached to the Reg. GND to act as heat sink to have RthJA within 65C/W.

I=(5-0.5-3.3)/(15/10)=800mA typ

I=(5-0.5-3.3)/(15/10)=800mA typ

0805, 1/8W

0805, 1/8W

FBVDD

3.47V

Vout=1.25V*(1+Rvout/Rgnd)+Rgnd*(Ifb=2ua/10^6)

Vout=1.25V*(1+Rvout/Rgnd)+Rgnd*(Ifb=2ua/10^6)

2.631V

FBVDDQ

Place Schottky Diode Closer to (or directly underneath) the FET.

Place Schottky Diode Closer to (or directly underneath) the FET.

*Note - C826, C823, C810 were stuffed with 0.01UF caps previously, now CL+ net is grounded using 1.5K ohm resistor.

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