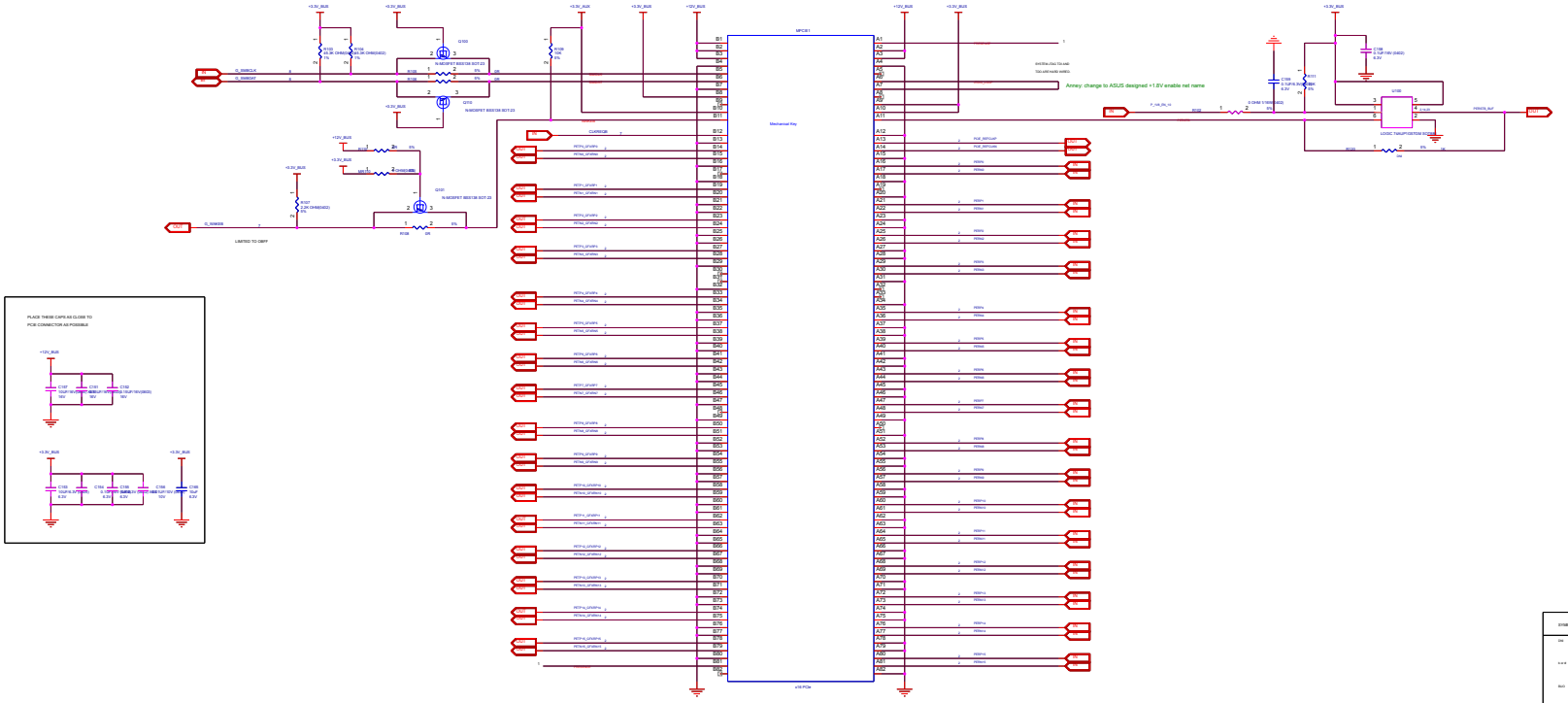
(1) PCI-EXPRESS EDGE CONNECTOR



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<OrgName>	Engineer:	Anney_Liu	
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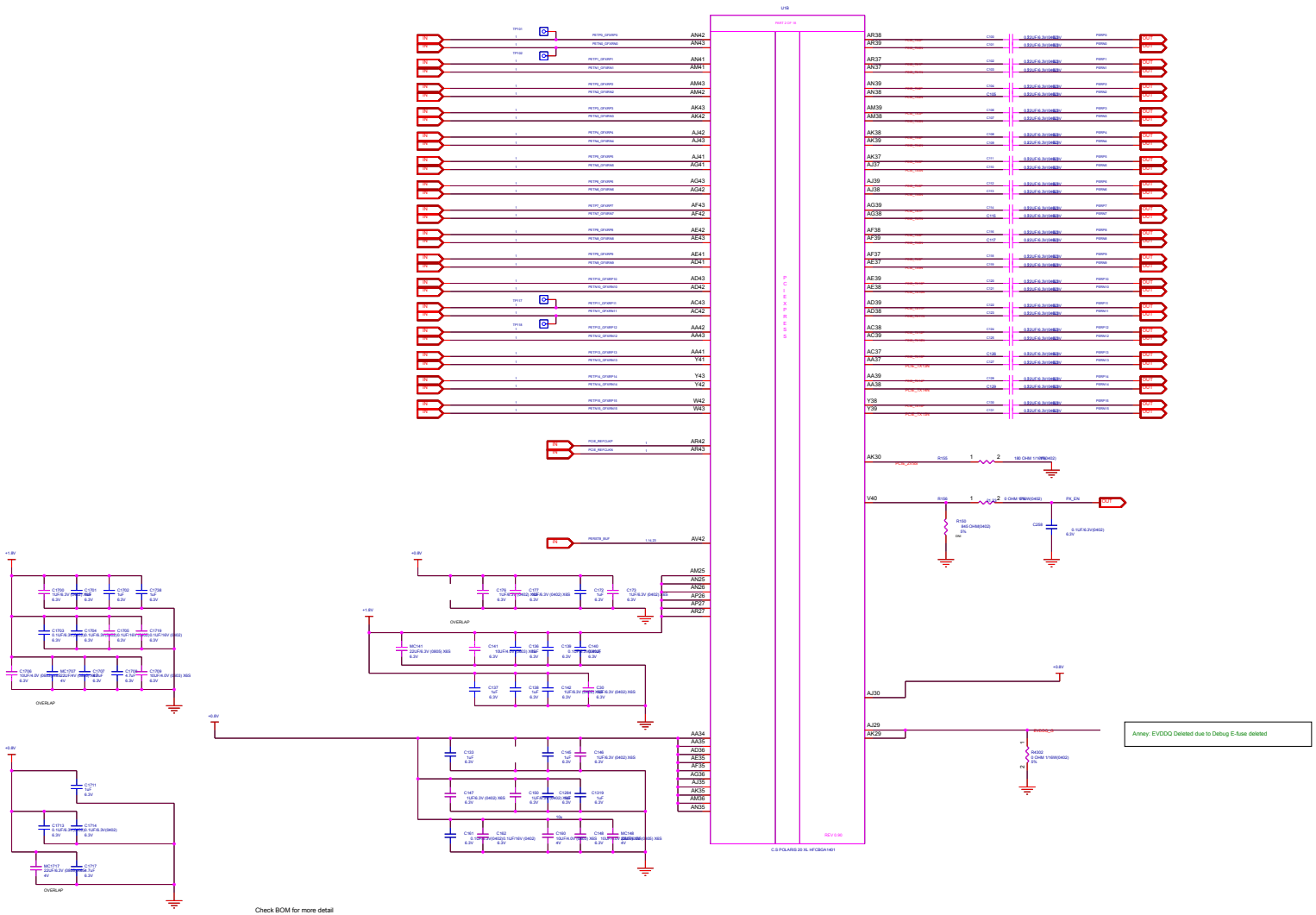
(2) ELLESMERE PCIE INTERFACE



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<OrgName>		Engineer:	
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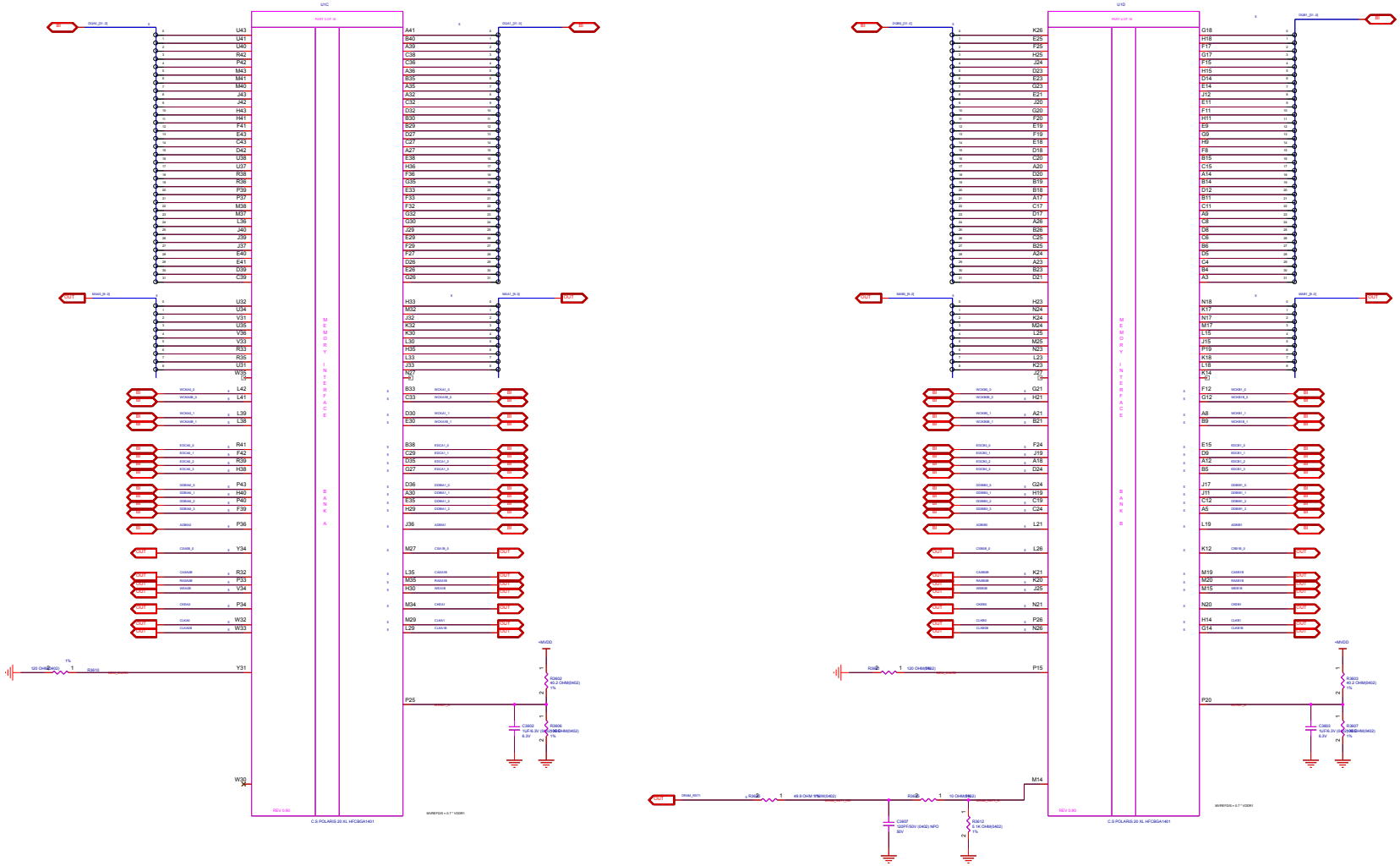
(3) ELLESMERE MEM INTERFACE CH A/B



Title :	POLARIS/D009P		
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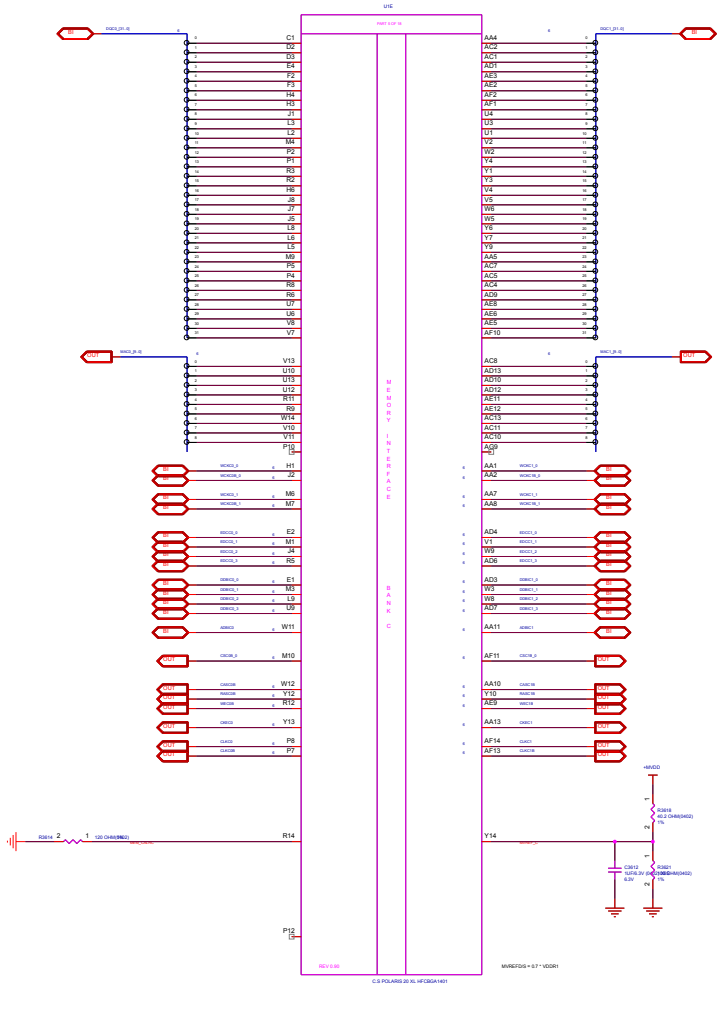
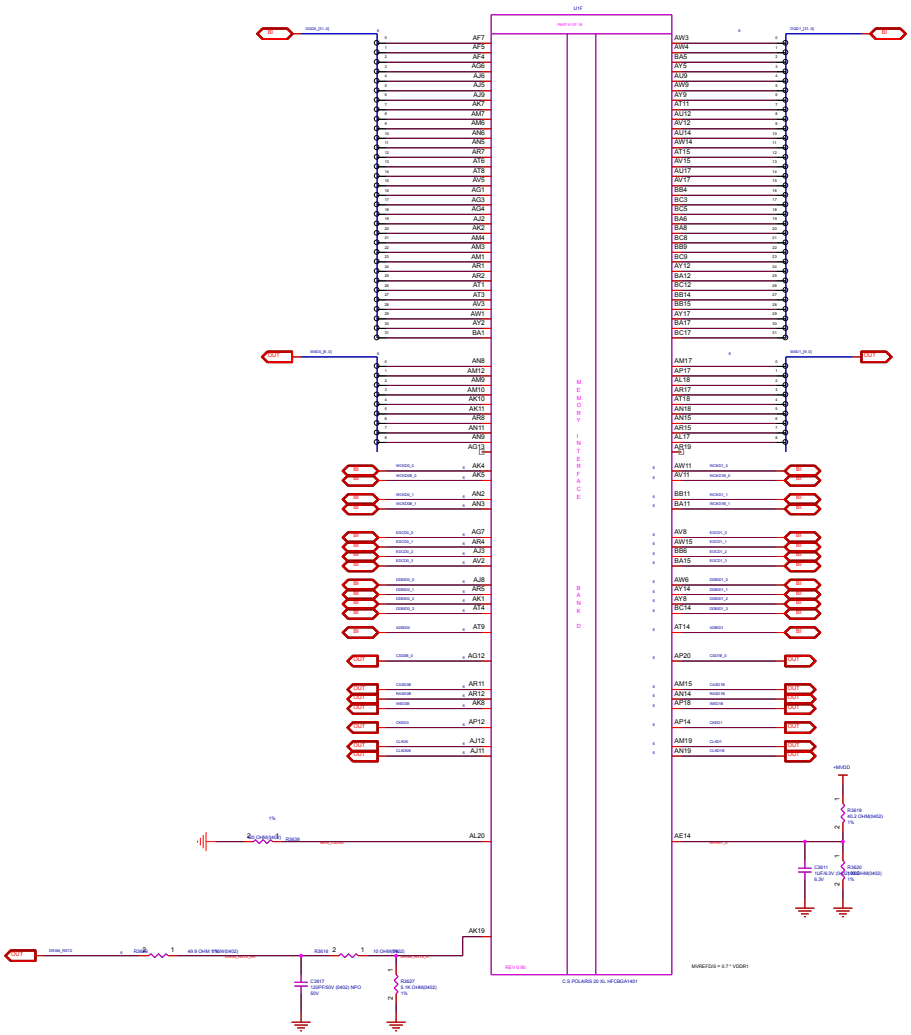
Size: Custom	Project Name: D009PI		

(4) ELLESMERE MEM INTERFACE CH C/D





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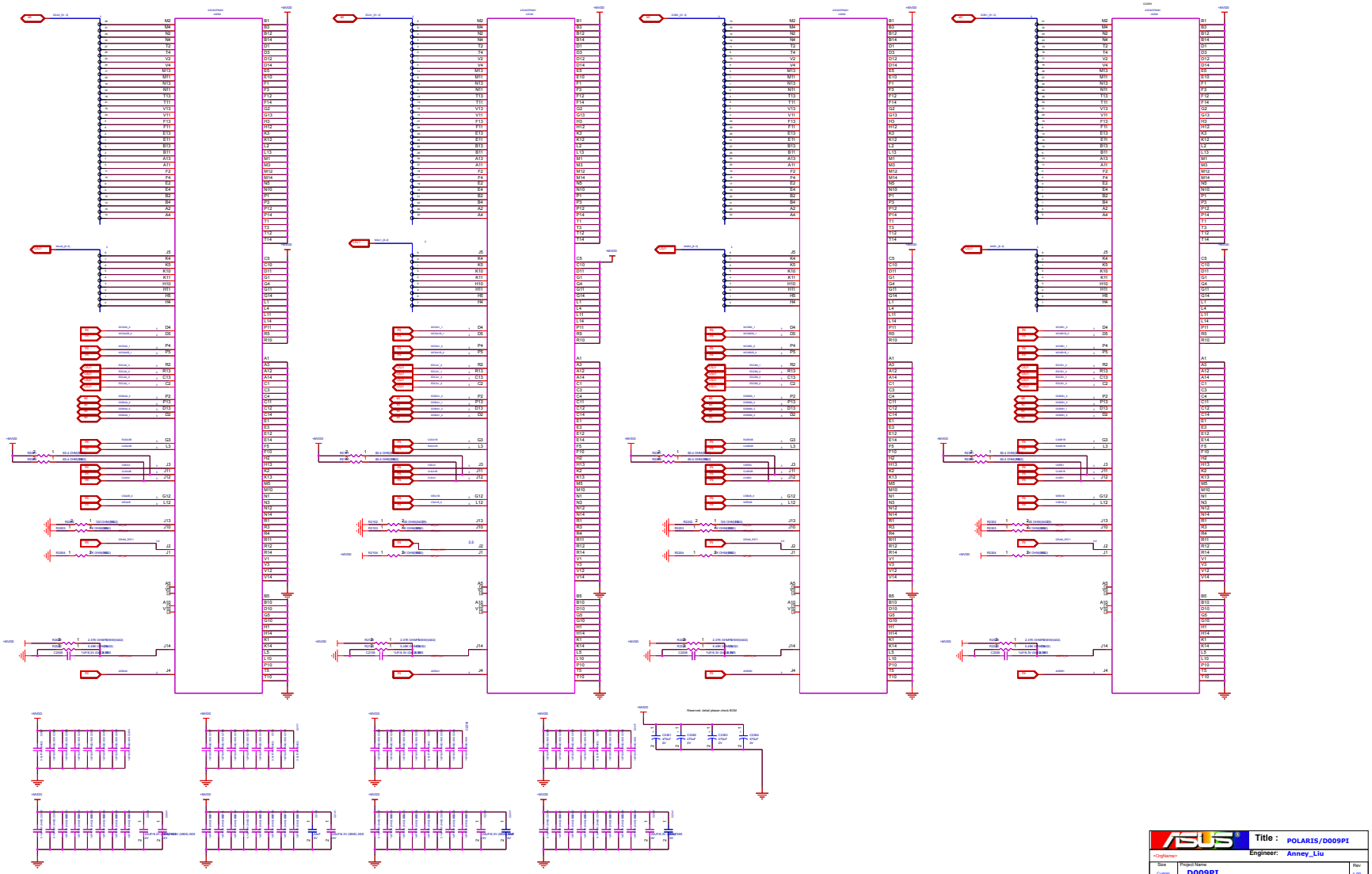
Size: Custom	Project Name: D009PI	

(5) GDDR5 MEMORY CH A/B



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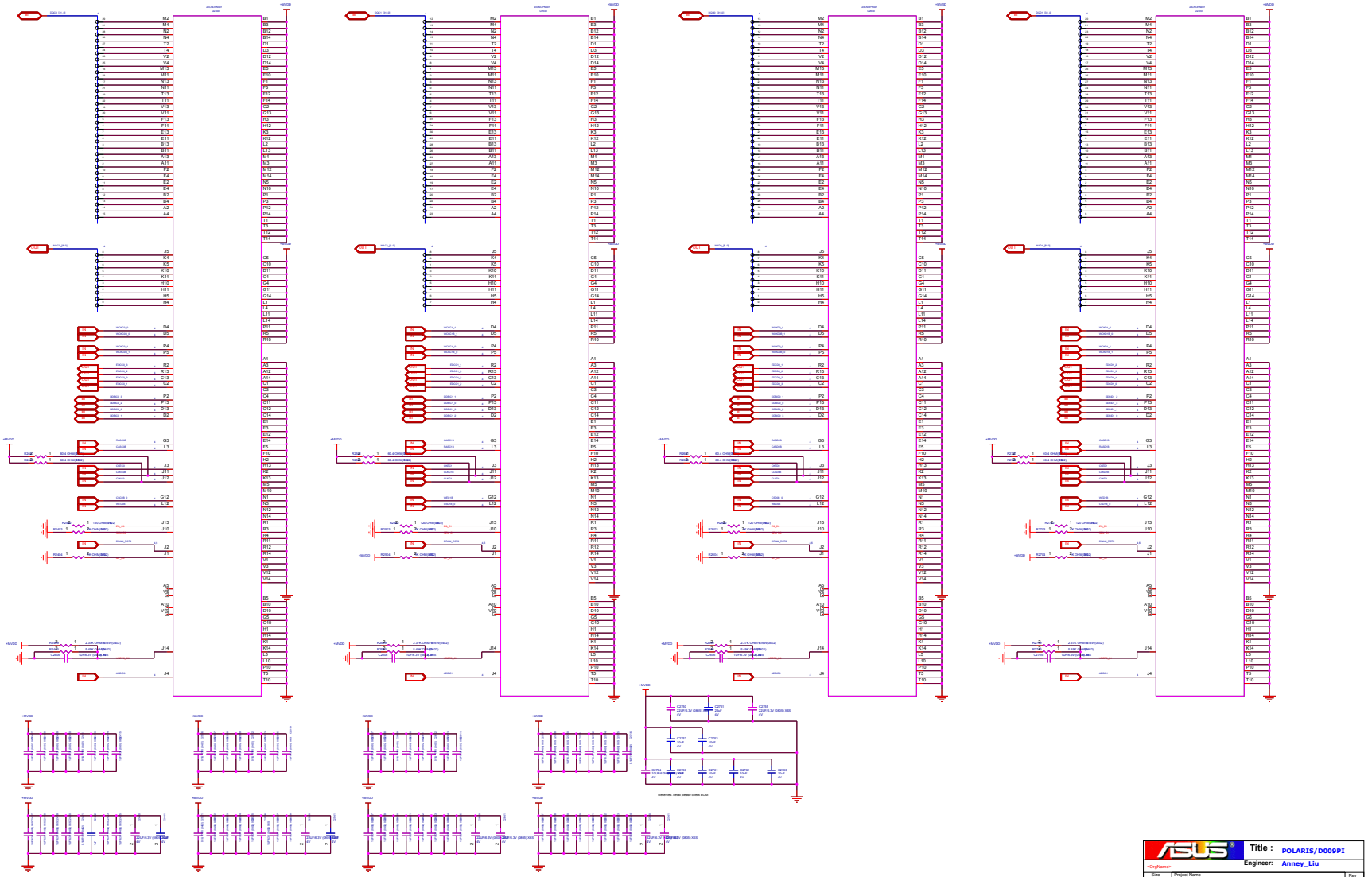
(6) GDDR5 MEMORY CH C/D



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<OrgName>		
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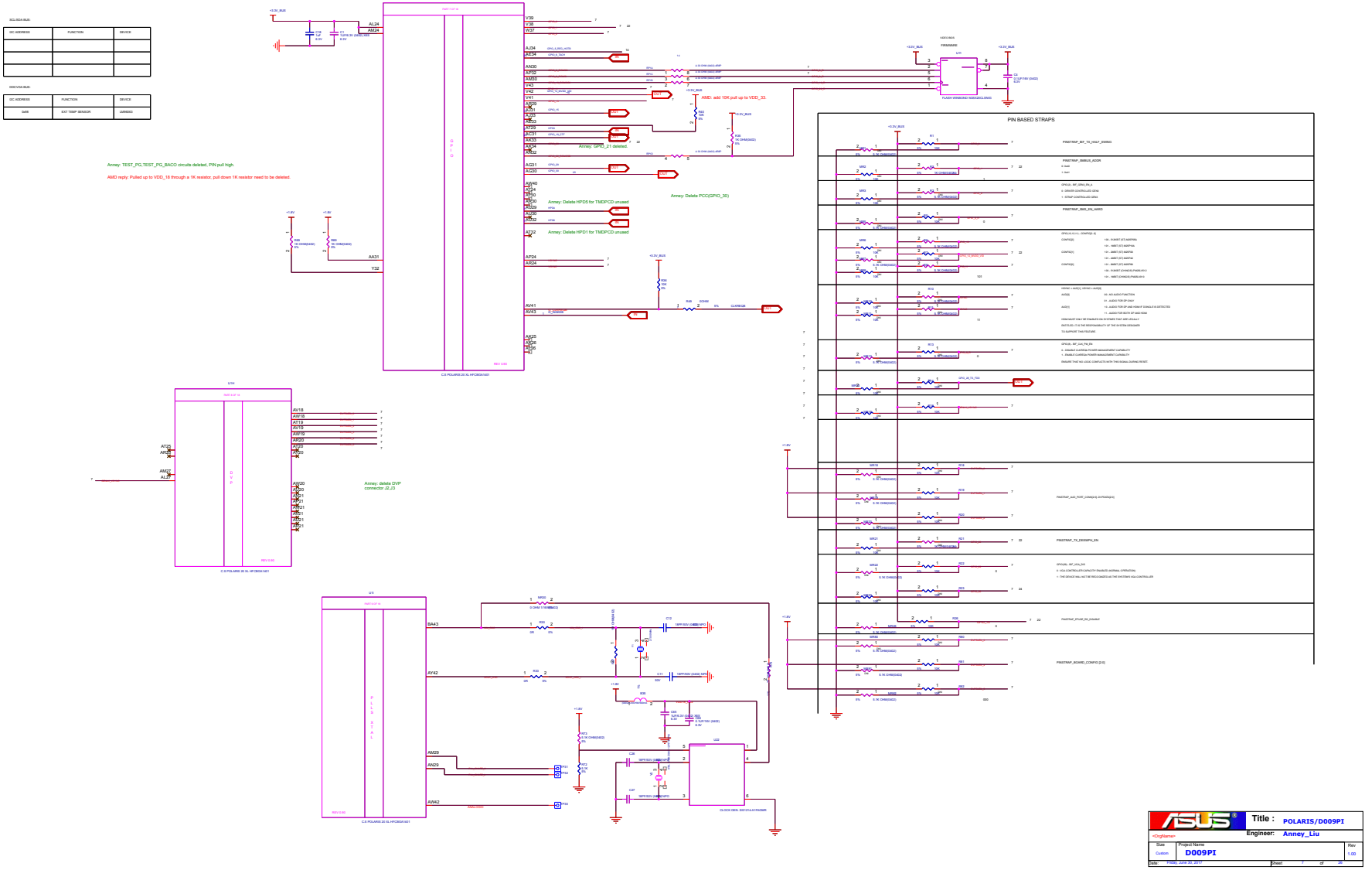
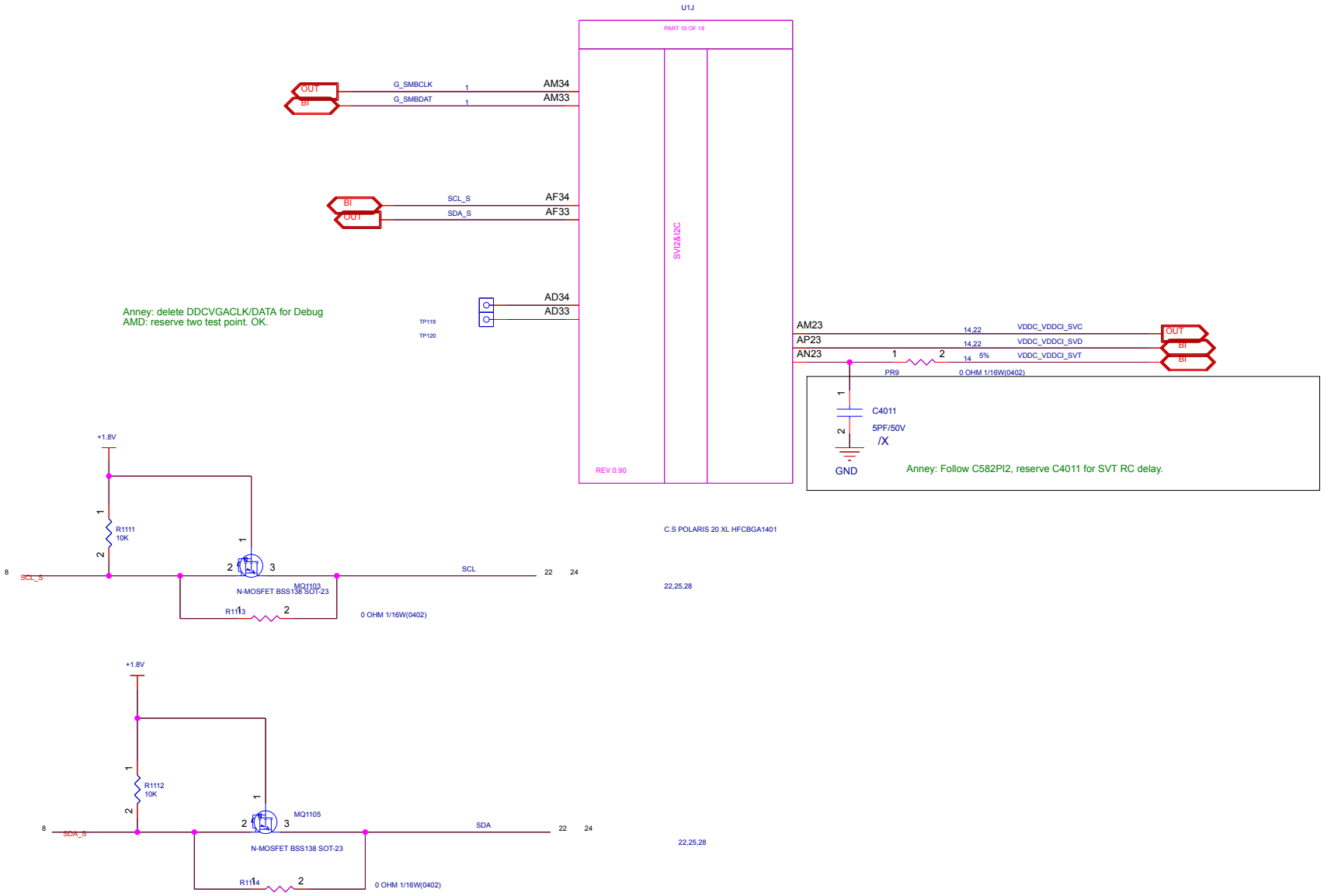
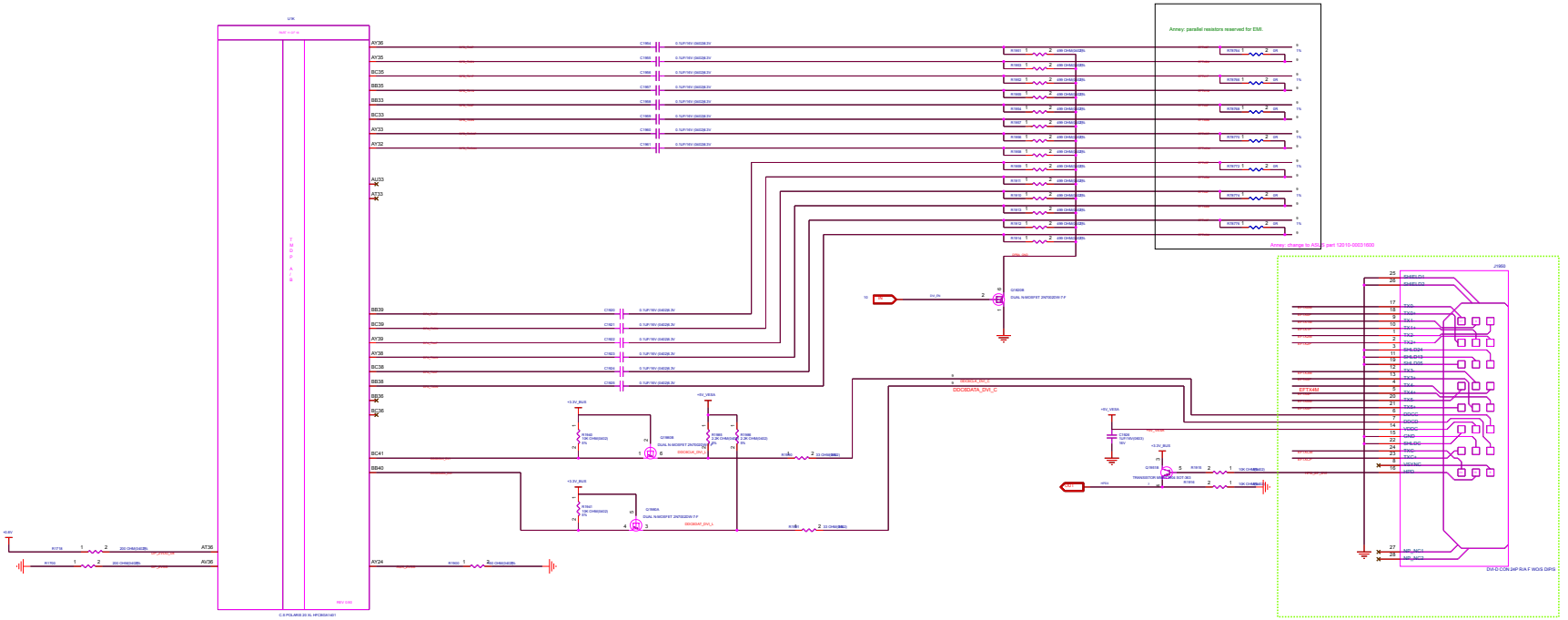
(7) ELLESMERE GPIO STRAP CF XTAL




U1J
PART 10 OF 18
OUT
BI
G_SMBCLK
G_SMBDAT
AM34
AM33
SCL_S
SDA_S
AF34
AF33
AD34
AD33
TP119
TP120
SVI2&I2C
REV 0.90
C.S POLARIS 20 XL HFCBGA1401
Anney: delete DDCVGACLK/DATA for Debug
AMD: reserve two test point. OK.
AM23
AP23
AN23
14,22
14
VDDC_VDDCI_SVC
VDDC_VDDCI_SVD
VDDC_VDDCI_SVT
5%
PR9
0 OHM 1/16W(0402)
C4011
5PF/50V
/X
GND
Anney: Follow C582PI2, reserve C4011 for SVT RC delay.
+1.8V
R1111
10K
R1113
MQ1103
N-MOSFET BSS138 SOT-23
SCL
SCL_S
22
24
22,25,28
0 OHM 1/16W(0402)
+1.8V
R1112
10K
R1114
MQ1105
N-MOSFET BSS138 SOT-23
SDA
SDA_S
22,25,28
0 OHM 1/16W(0402)

(9) ELLESMERE Dual-Link DVI



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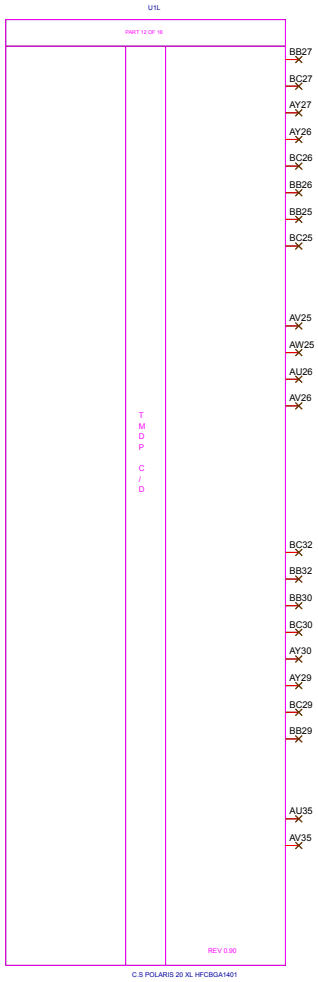
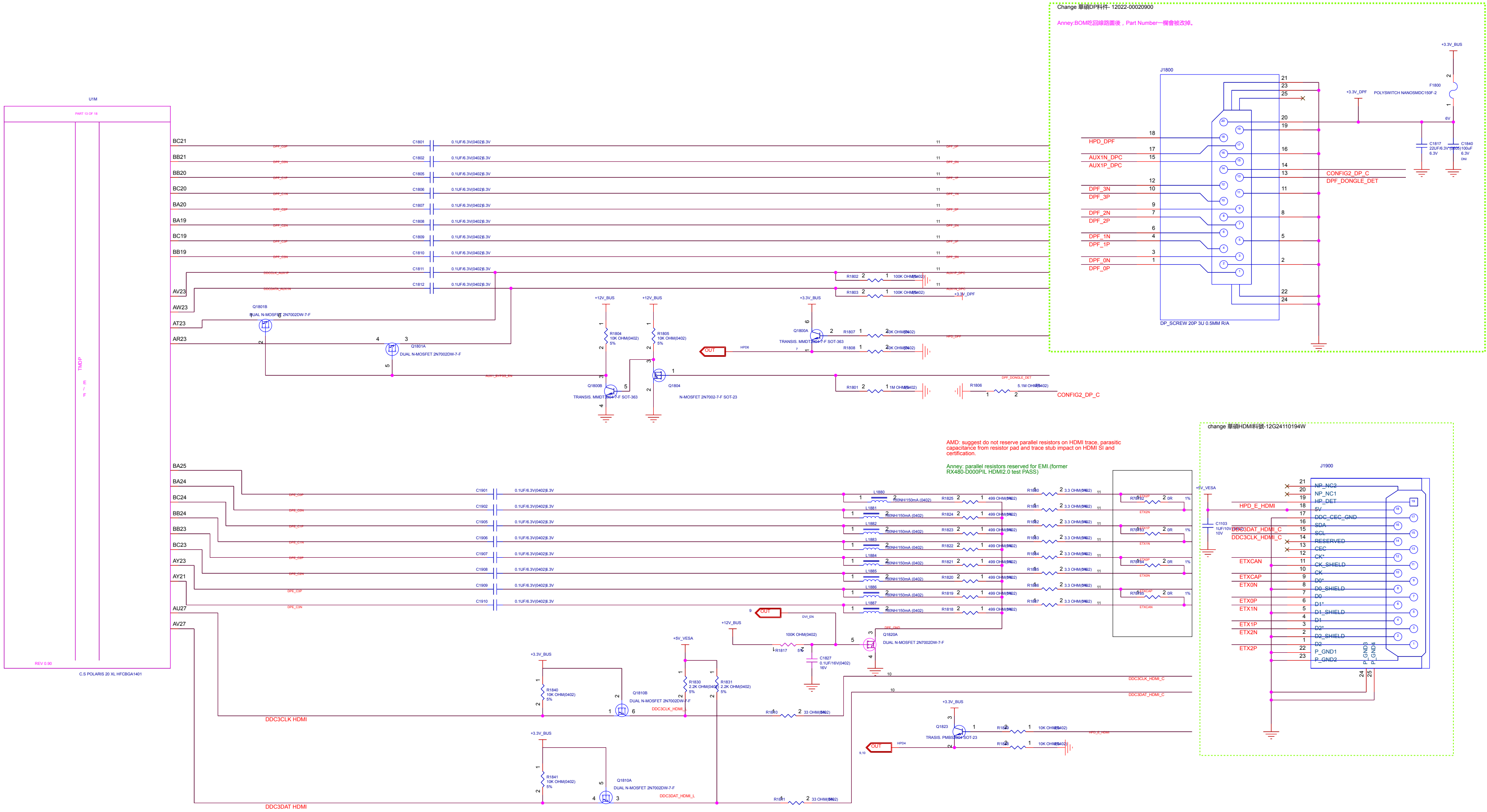
(10) ELLESMERE TMDPCD unused

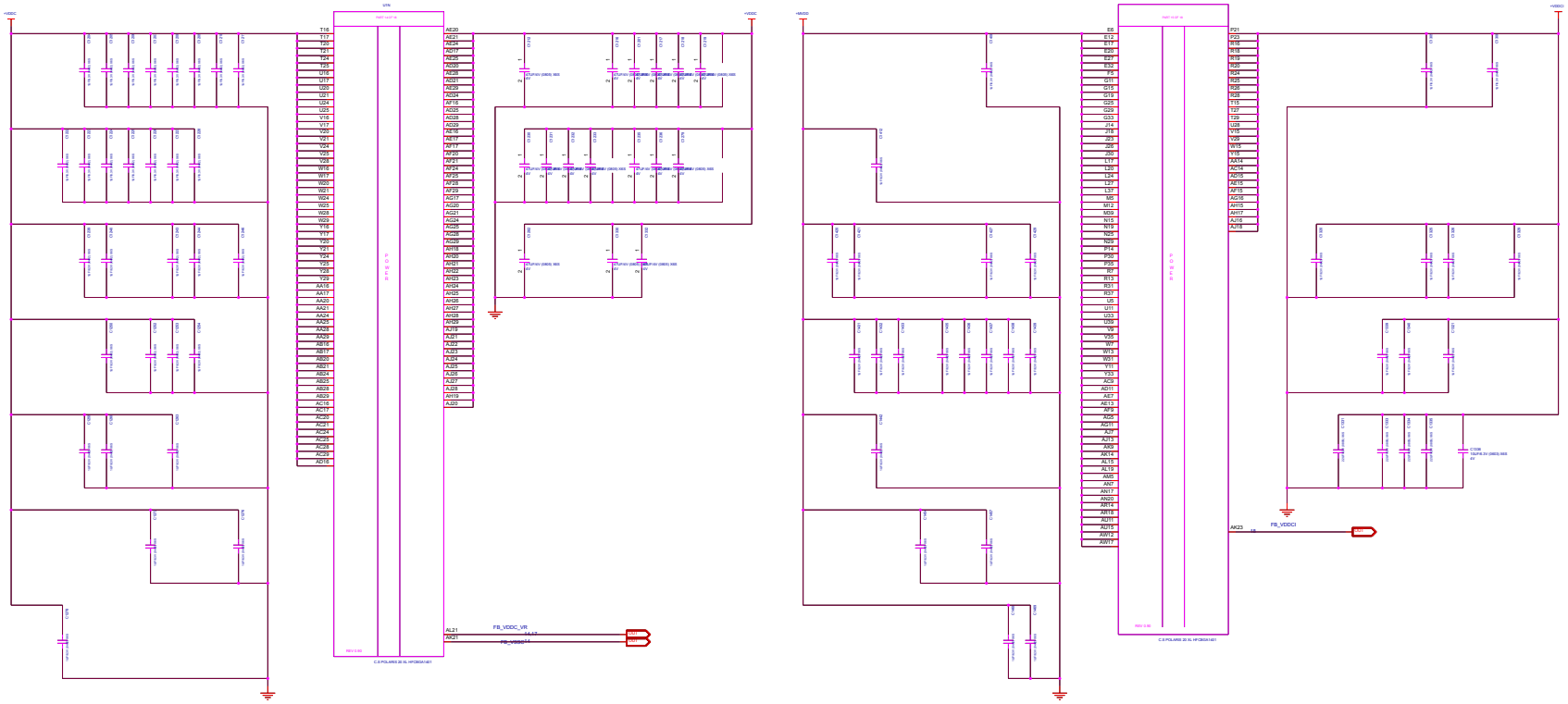


Anney: TMDPCD unused, all pins NC



Change 華碩DP料件- 12022-00020900
Anney:BOM吃回線路圖後，Part Number一欄會被改掉。
J1800
DP_SCREW 20P 3U 0.5MM R/A
HPD_DPF
AUX1N_DPC
AUX1P_DPC
DPF_3N
DPF_3P
DPF_2N
DPF_2P
DPF_1N
DPF_1P
DPF_0N
DPF_0P
CONFIG2_DP_C
DPF_DONGLE_DET
+3.3V_BUS
+3.3V_DPF
POLYSWITCH NANOSMDC150F-2
U1M
C.S POLARIS 20 XL HFCBGA1401
BC21
BB21
BB20
BC20
BA20
BA19
BC19
BB19
AV23
AW23
AT23
AR23
BA25
BA24
BC24
BB24
BB23
BC23
AY23
AY21
AU27
AV27
+12V_BUS
R1804
R1805
Q1801B
Q1801A
DUAL N-MOSFET 2N7002DW-7-F
Q1800B
Q1804
N-MOSFET 2N7002-7-F SOT-23
R1806
5.1M OHM(0402)
CONFIG2_DP_C
AMD: suggest do not reserve parallel resistors on HDMI trace, parasitic capacitance from resistor pad and trace stub impact on HDMI SI and certification.
Anney: parallel resistors reserved for EMI.(former RX480-D000PIL HDMI2.0 test PASS)
change 華碩HDMI料號-12G24110194W
J1900
+5V_VESA
C1103
NP_NC2
NP_NC1
HP_DET
5V
DDC_CEC_GND
SDA
SCL
RESERVED
CEC
CK-
CK_SHIELD
CK+
D0-
D0_SHIELD
D0+
D1-
D1_SHIELD
D1+
D2-
D2_SHIELD
D2+
P_GND1
P_GND2
HPD_E_HDMI
DDC3DAT_HDMI_C
DDC3CLK_HDMI_C
ETXCAN
ETXCAP
ETX0N
ETX0P
ETX1N
ETX1P
ETX2N
ETX2P
DDC3CLK HDMI
DDC3DAT HDMI
R1840
R1841
R1830
R1831
Q1810B
Q1810A
Q1820A
Q1823

(12) ELLESMERE POWER



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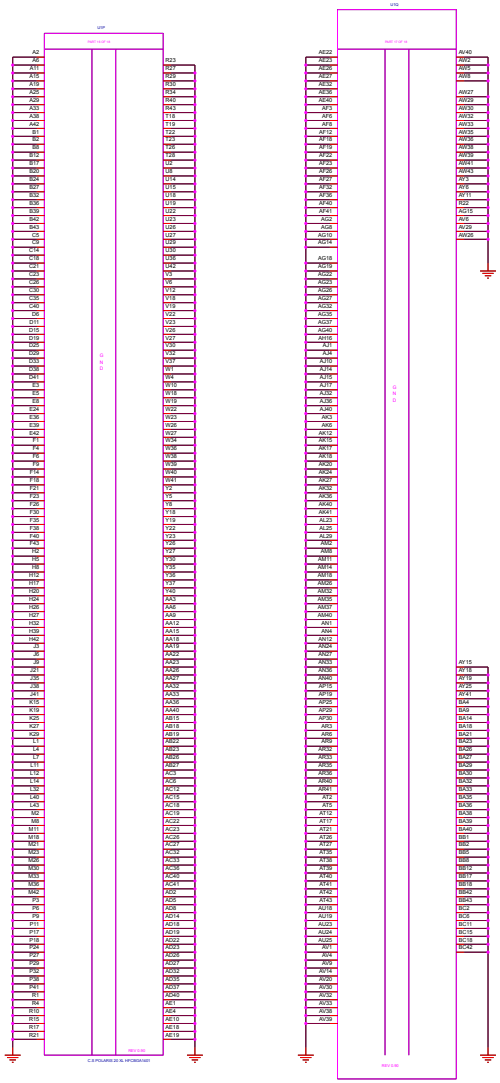
(13) ELLESMERE GROUND



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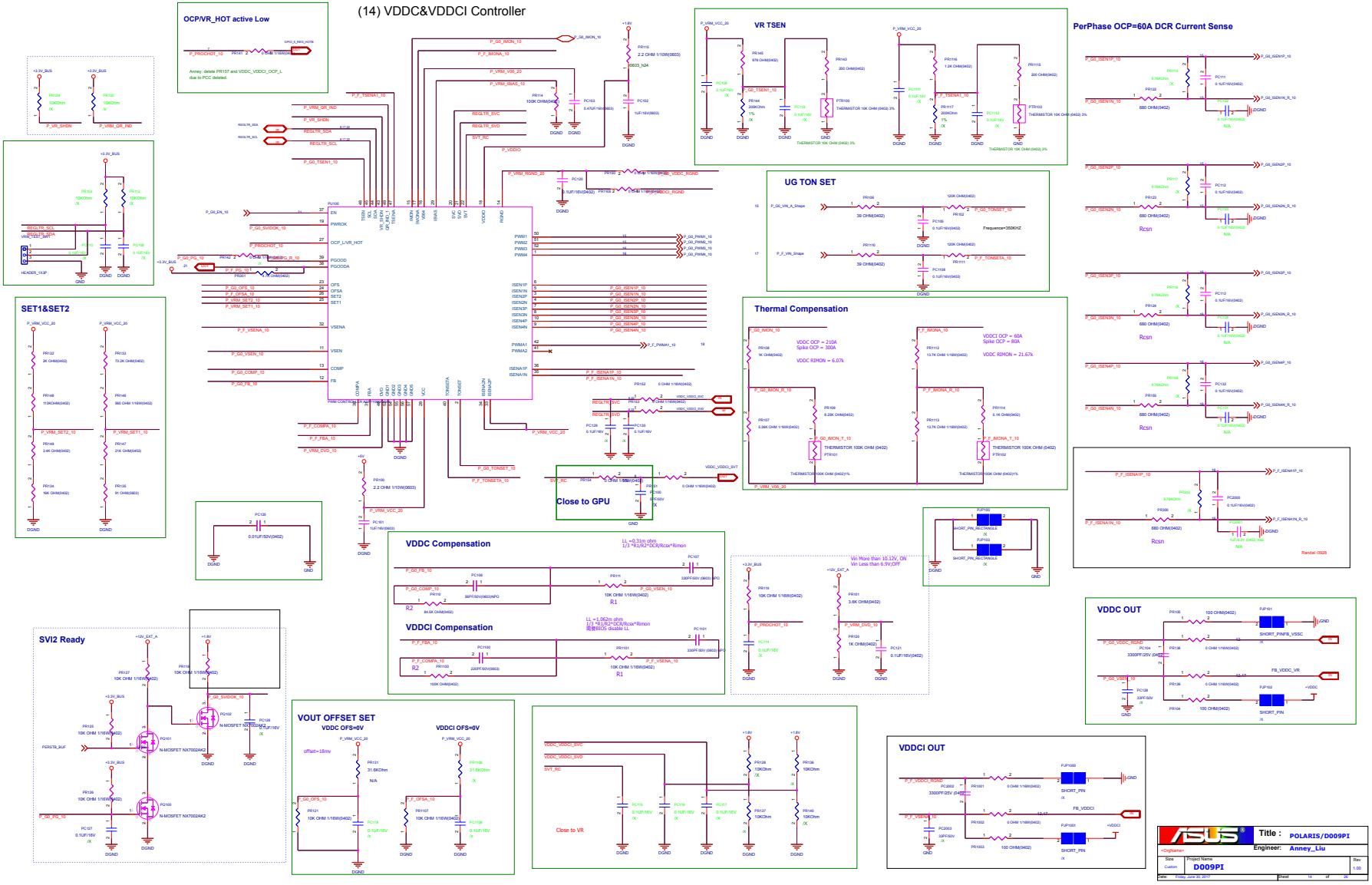
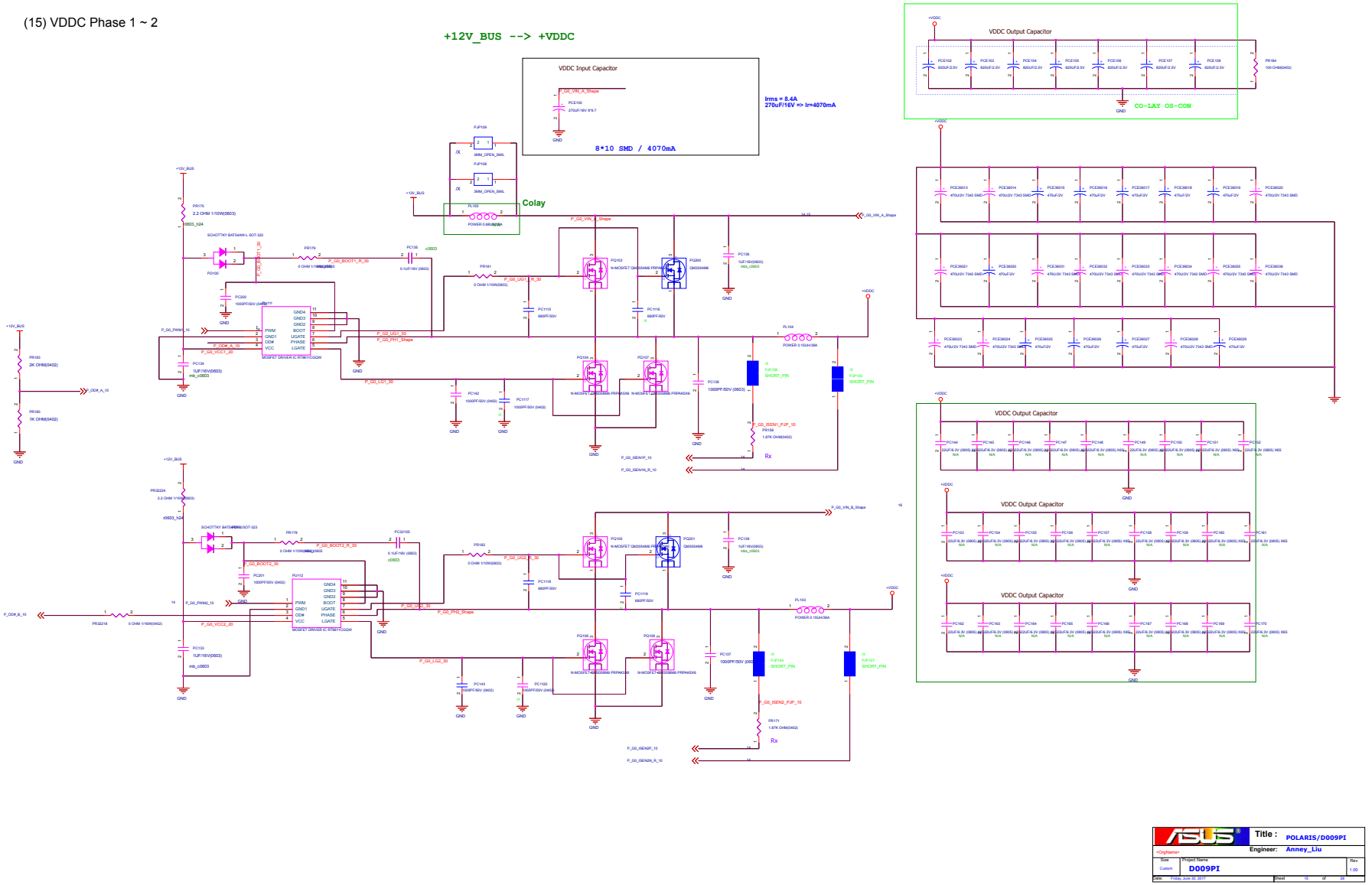
(14) VDDC&VDDCI Controller



(15) VDDC Phase 1 ~ 2



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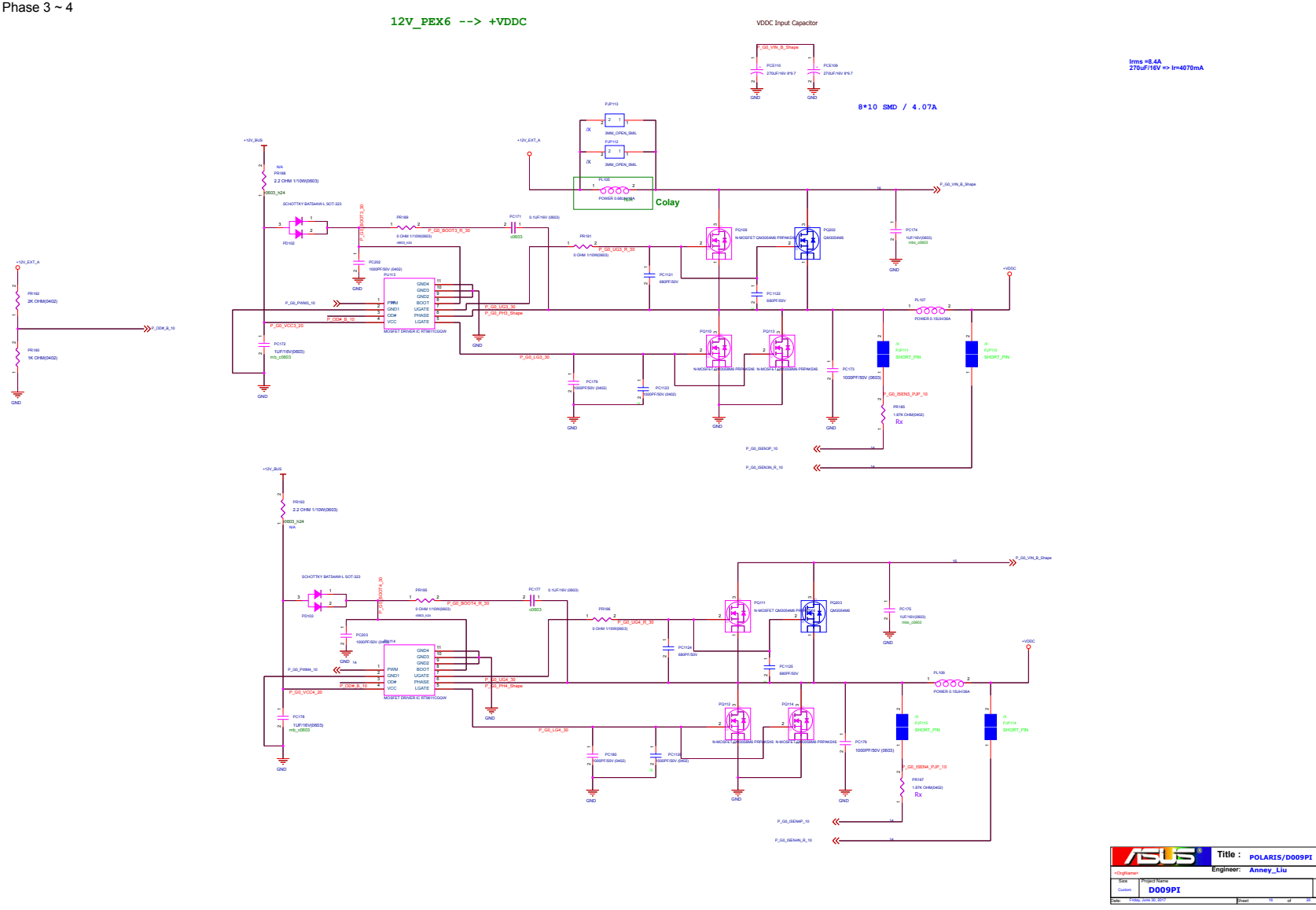
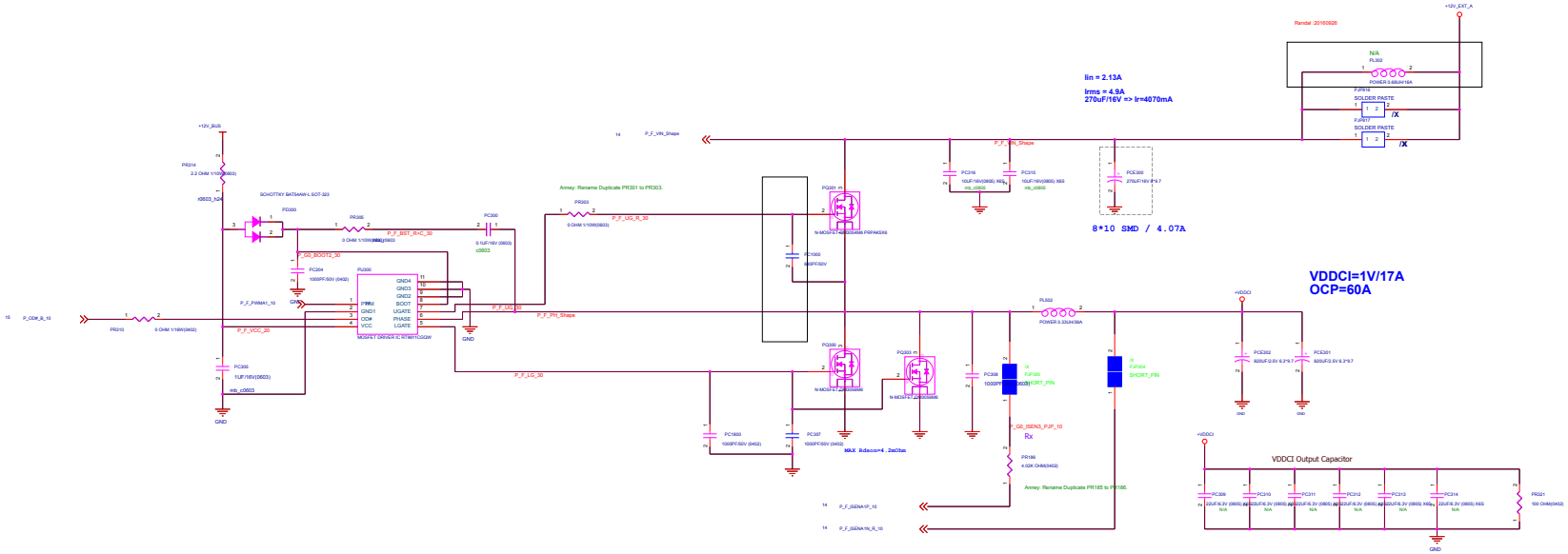
(16) VDDC Phase 3 ~ 4



(17) VDDCI 1 Phase

+12V_EXT_A --> +VDDCI



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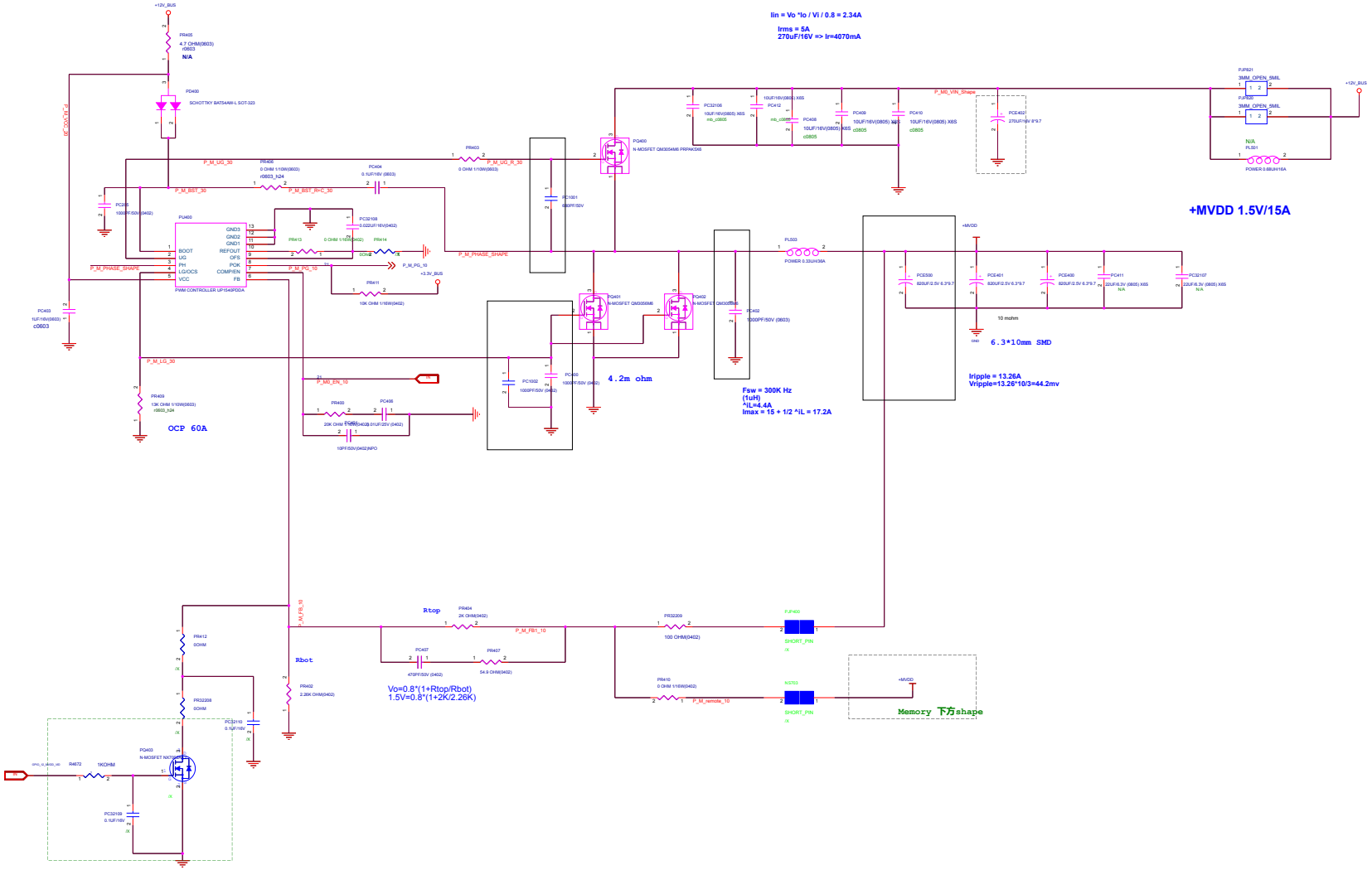
(18) MVDD 1 Phase

+12V_BUS--> +MVDD



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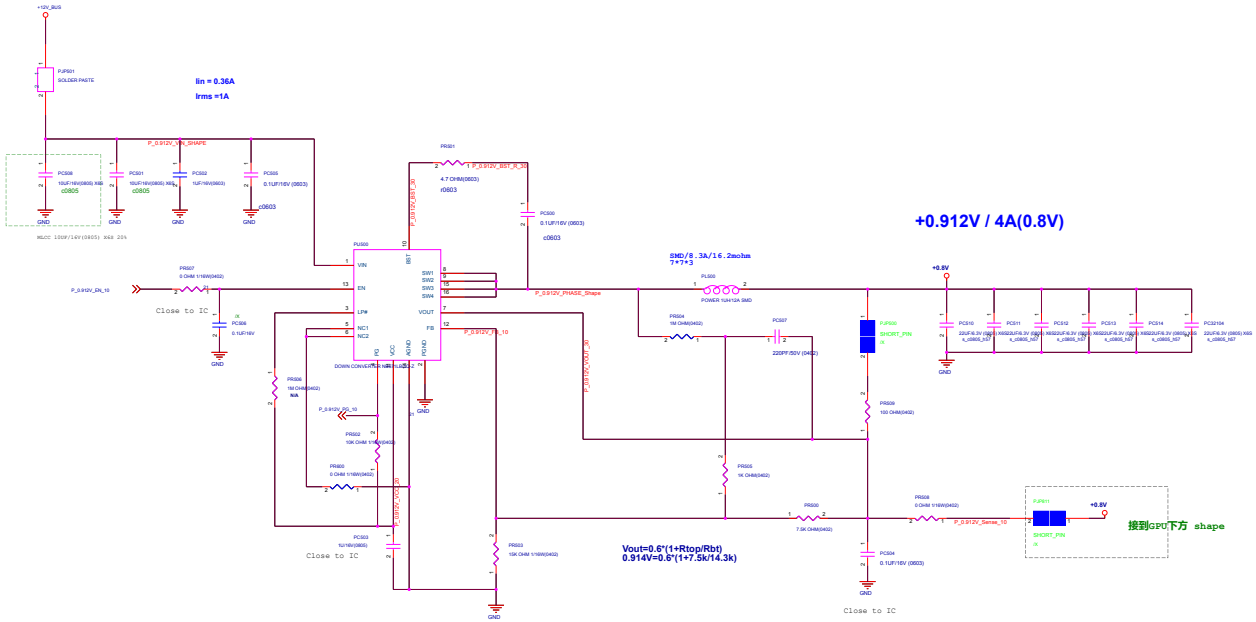
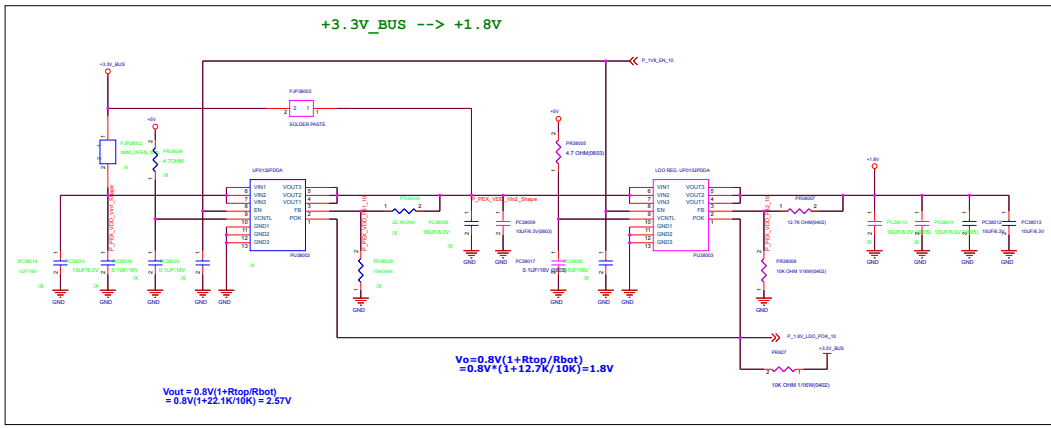
Size	Project Name
Rev	

(19) SMALL RAIL REGULATORS

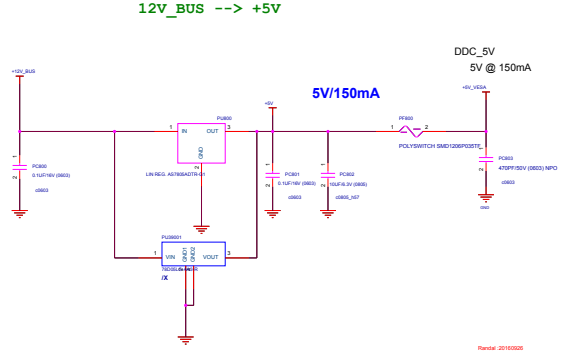
12V_PEX6 --> +0.875V



+3.3V_BUS --> +1.8V



12V_BUS --> +5V



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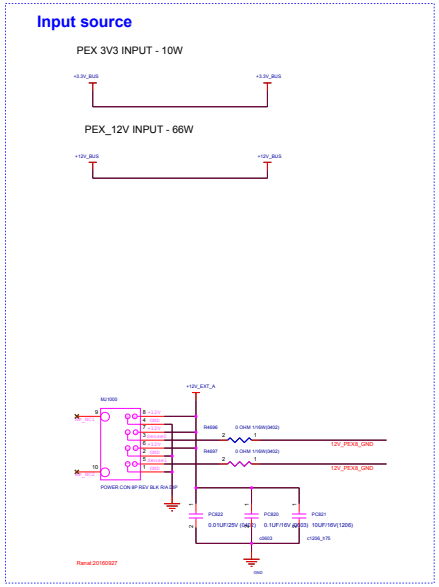
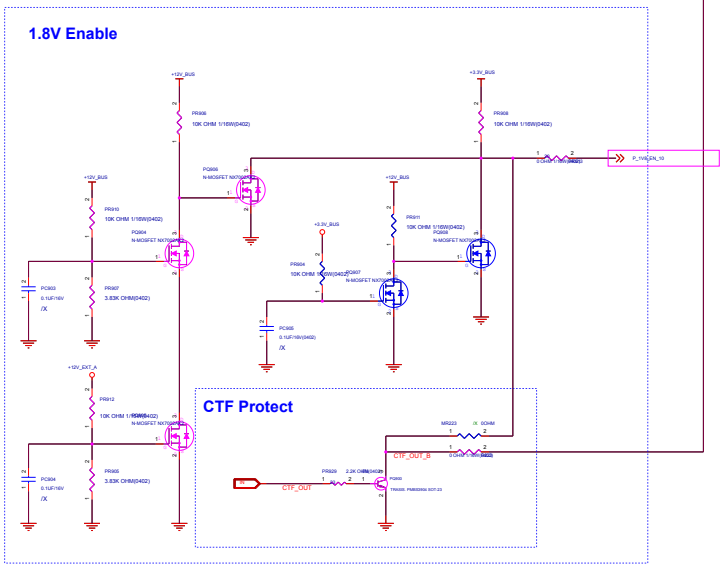
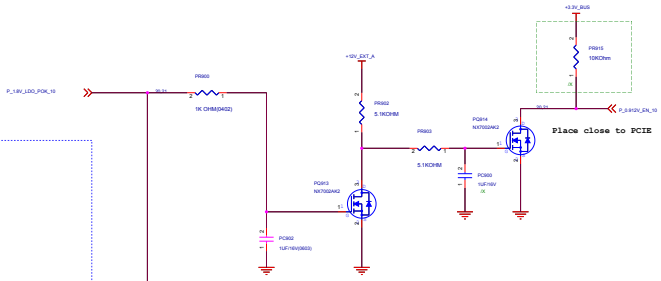
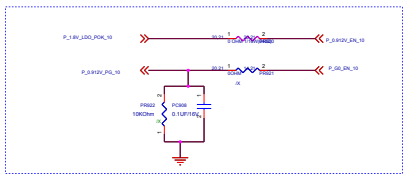
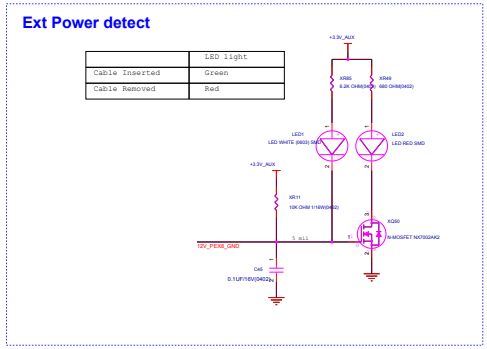
(20) POWER MANAGEMENT1

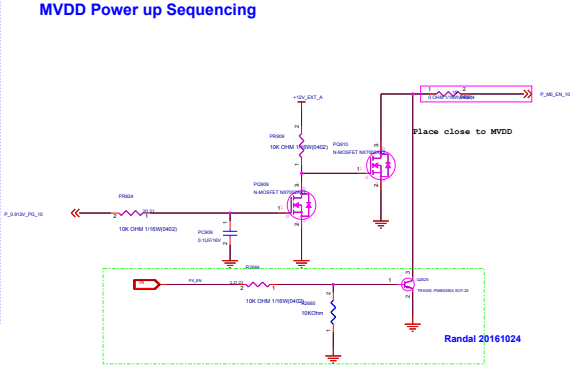


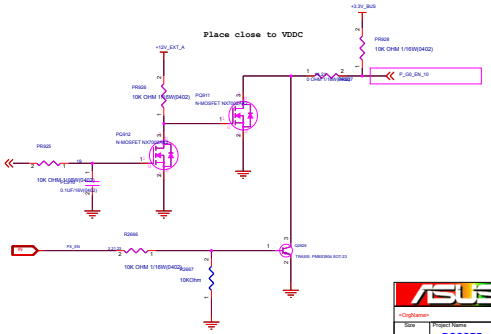




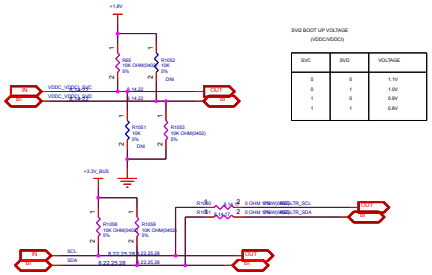






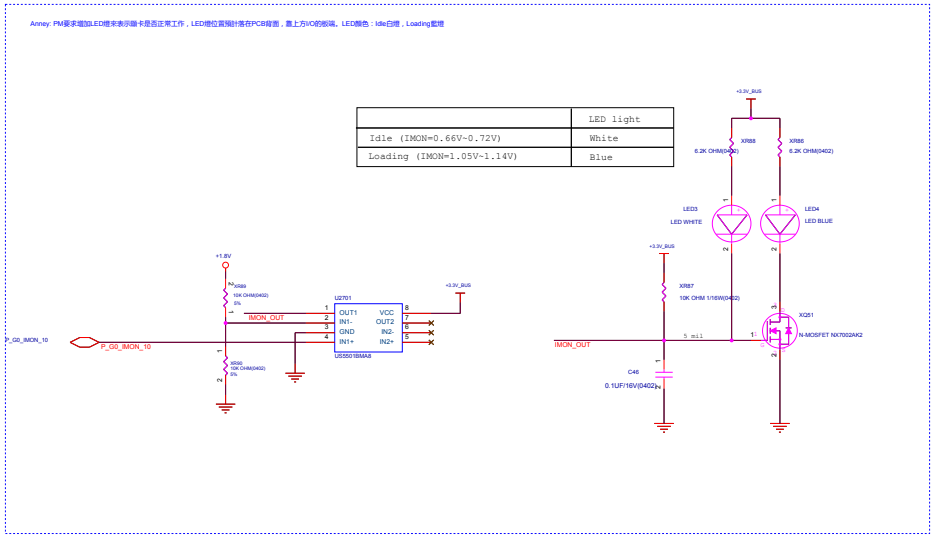


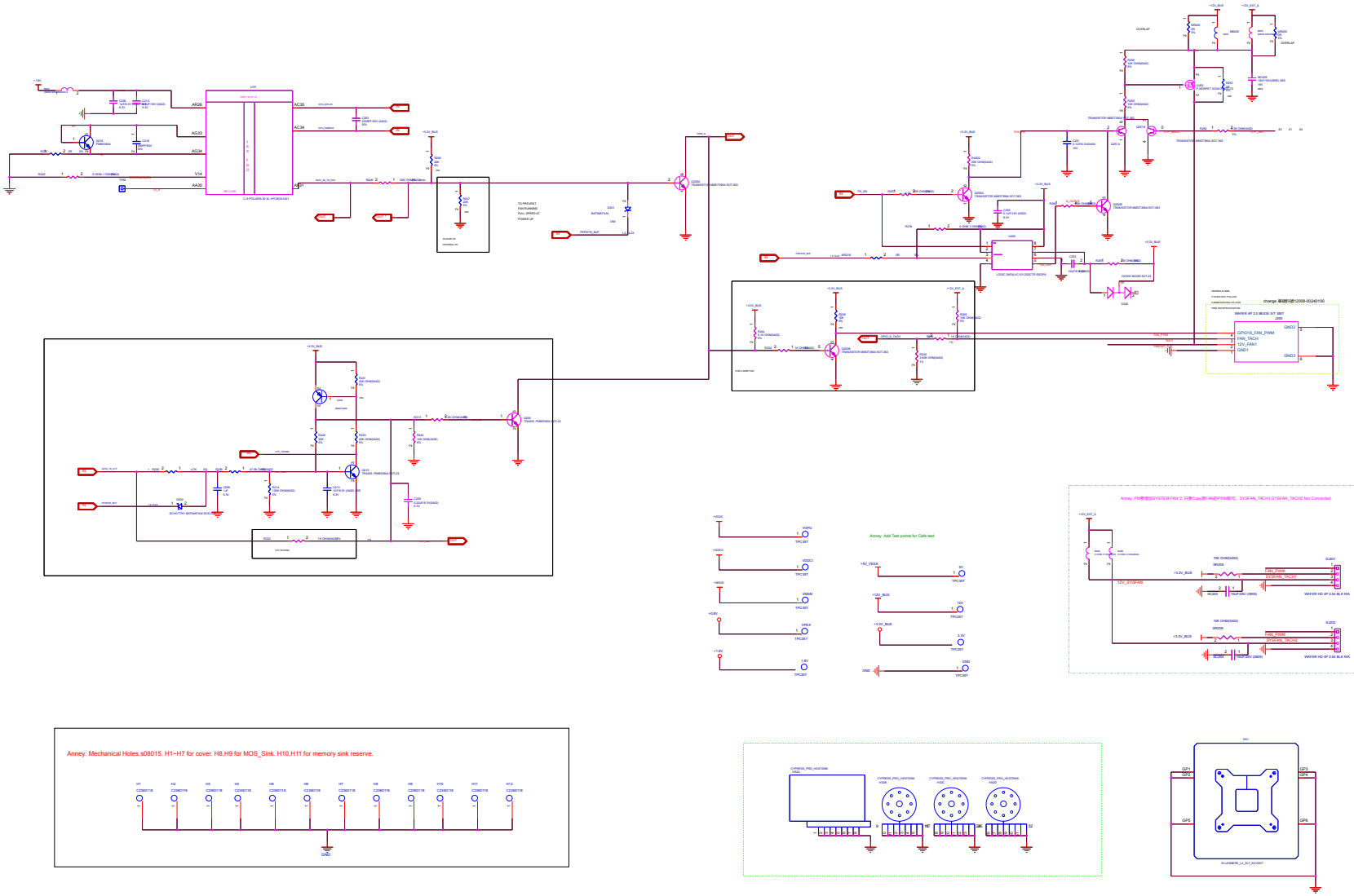
(21) POWER MANAGEMENT2



SVID BOOT UP VOLTAGE
(VDDCI/VDDCI)

SVC	SVD	VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V





Anney: Mechanical Holes.s08015. H1~H7 for cover. H8,H9 for MOS_Sink. H10,H11 for memory sink reserve.

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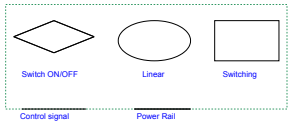
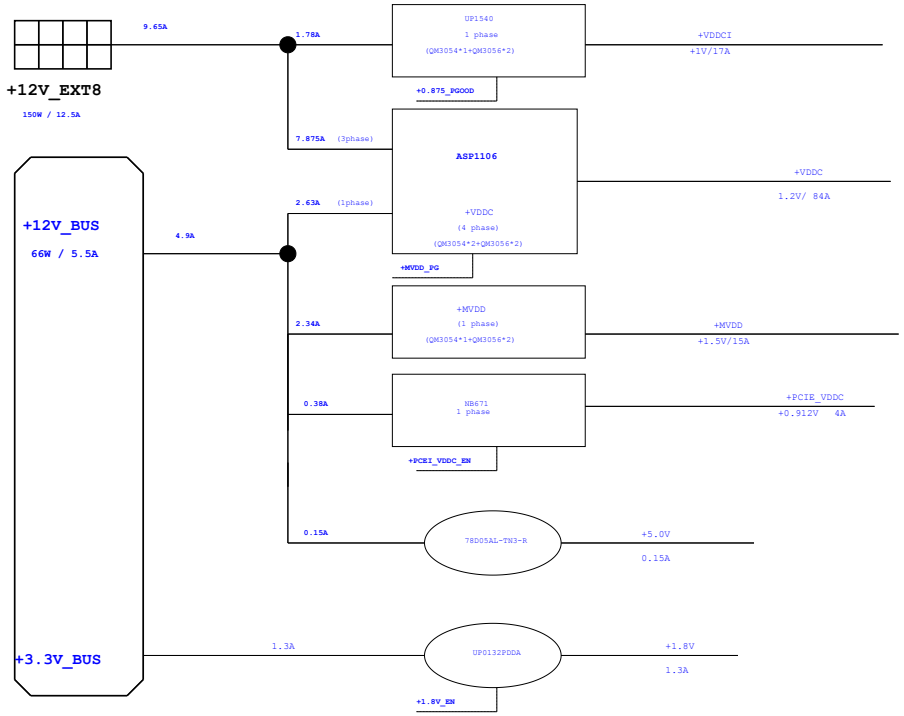
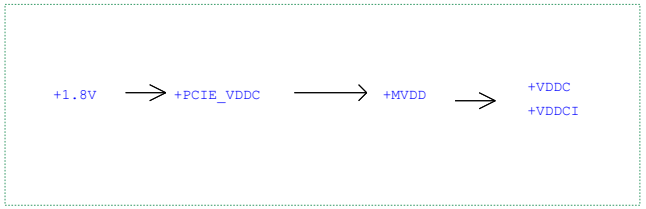
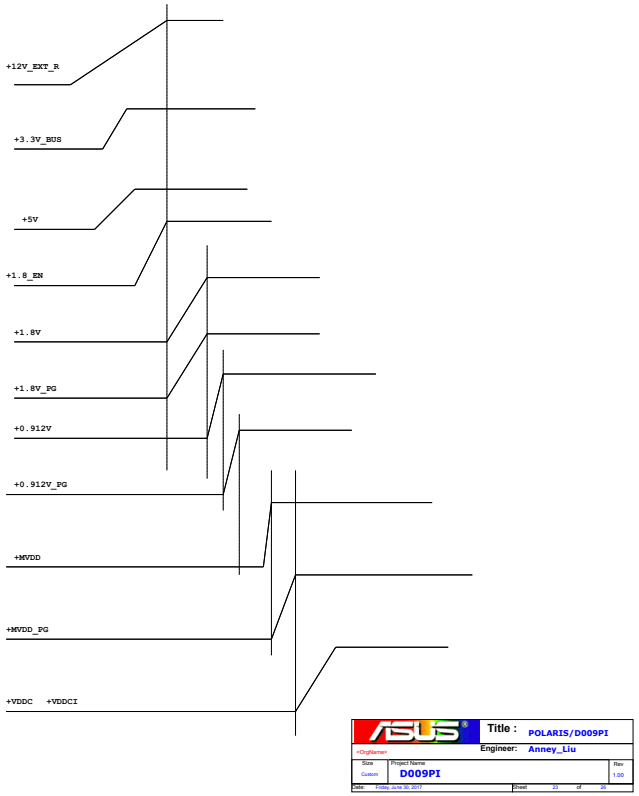
Power Flow





POWER SEQUENCE





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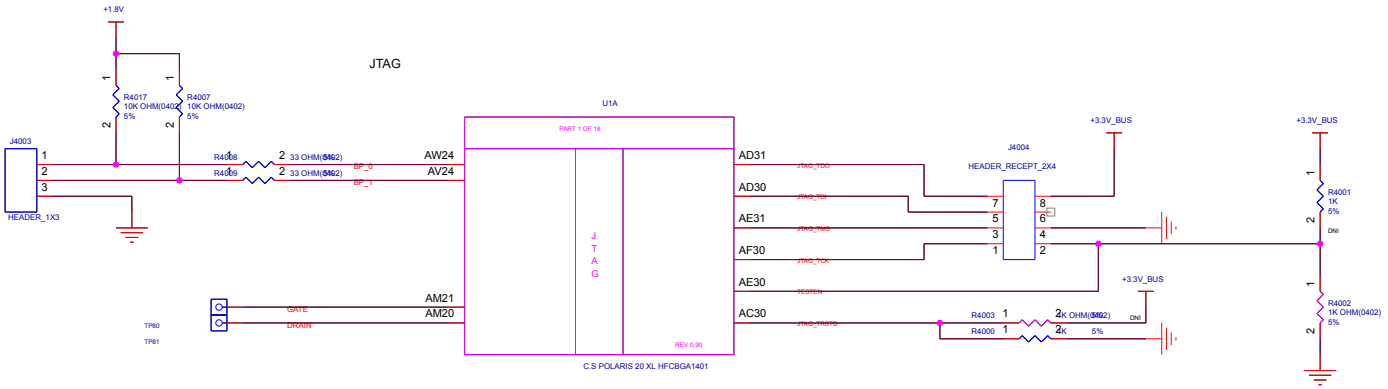
(24) DEBUG CIRCUITS

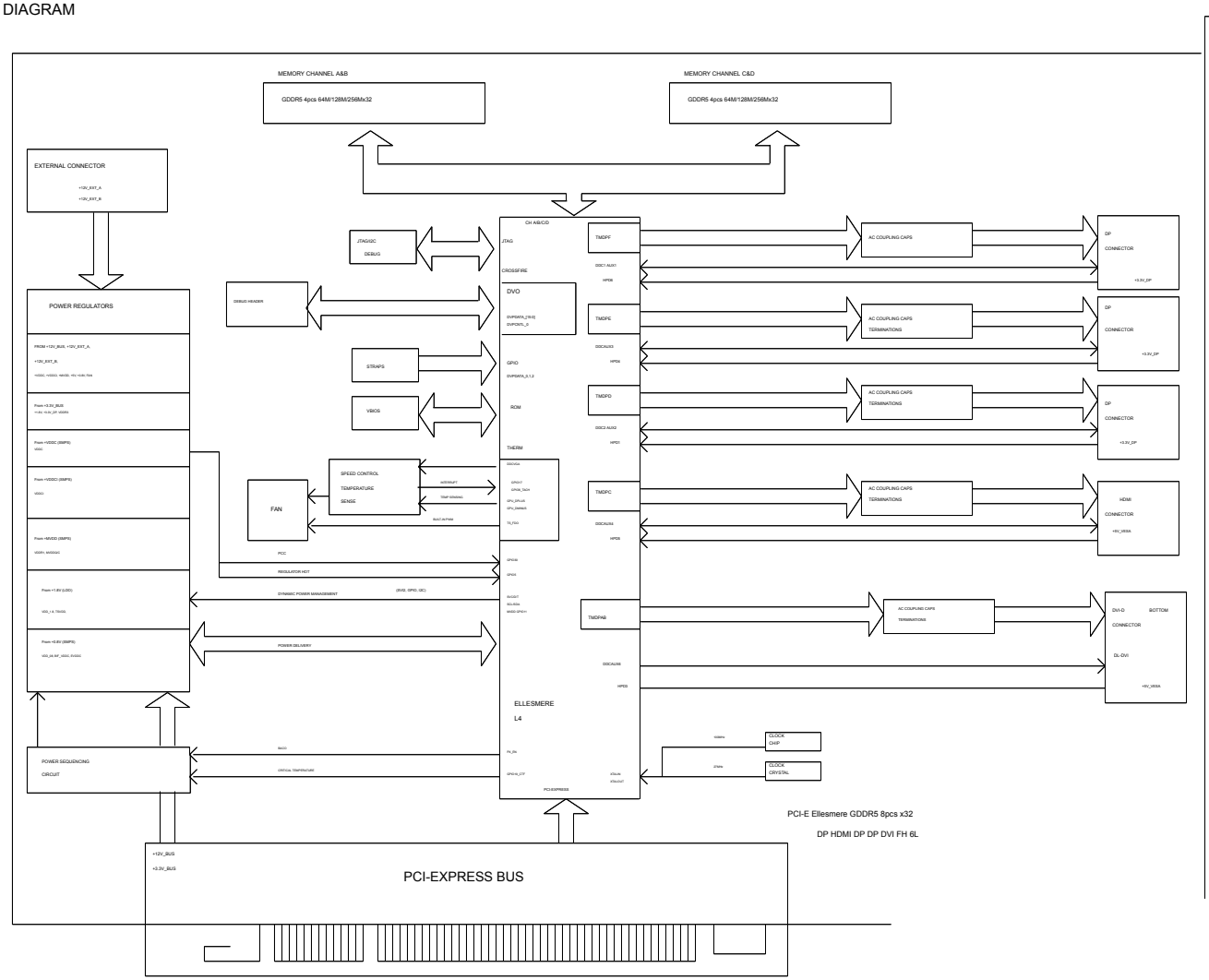


E-FUSE CAPABILITY

DEFAULT = GPIO-CONTROLLED
(MANUAL OPTION AS BACK-UP)

Anney: EVDDQ Debug E-fuse deleted

(25) BLOCK DIAGRAM



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