PG401 A02

4GB GDDR5, 256b, 128Mx32

Tall DVI-I + DP + DP + DP/HDMI + DP

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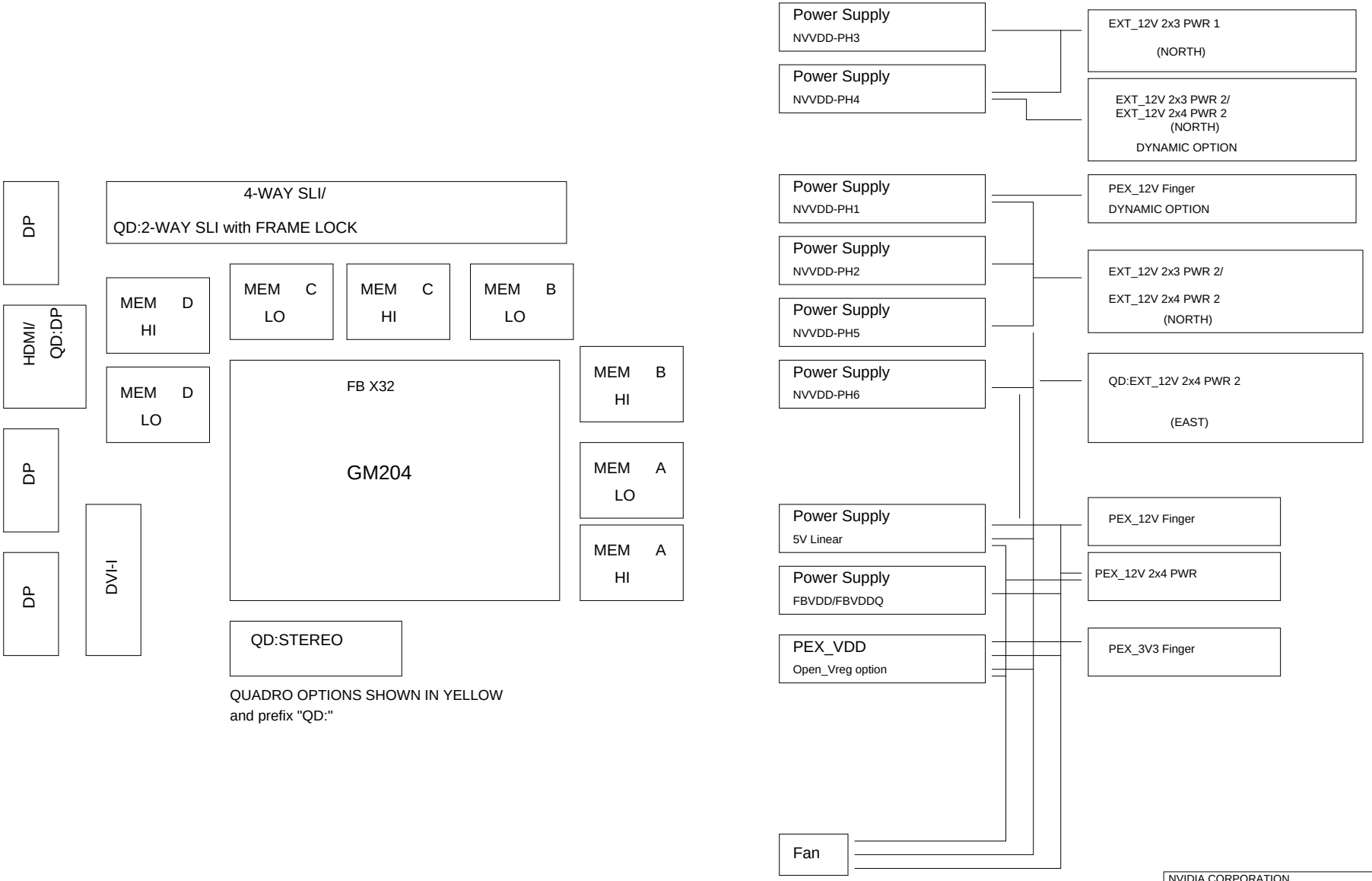

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
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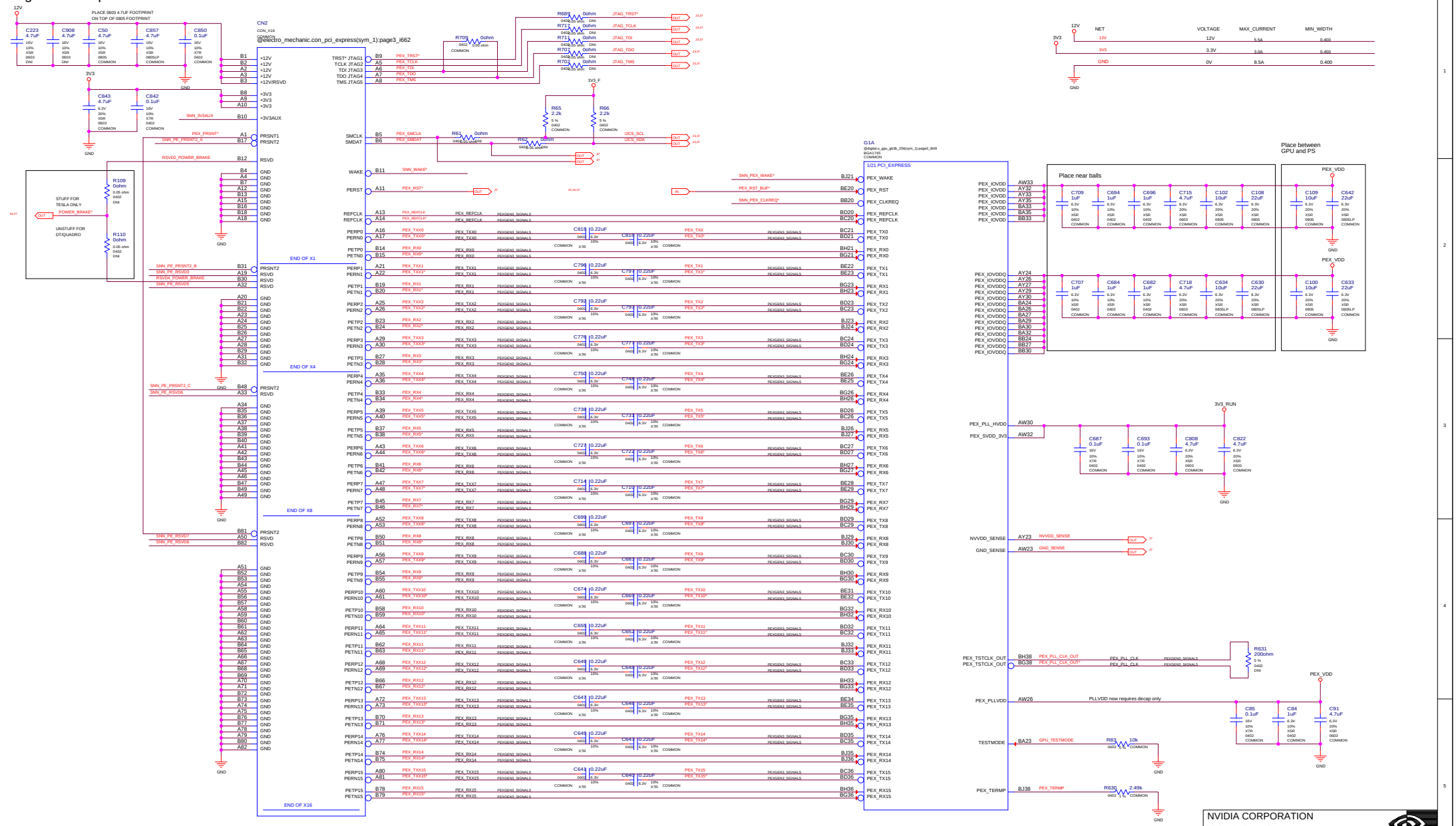
Page3: PCI Express



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
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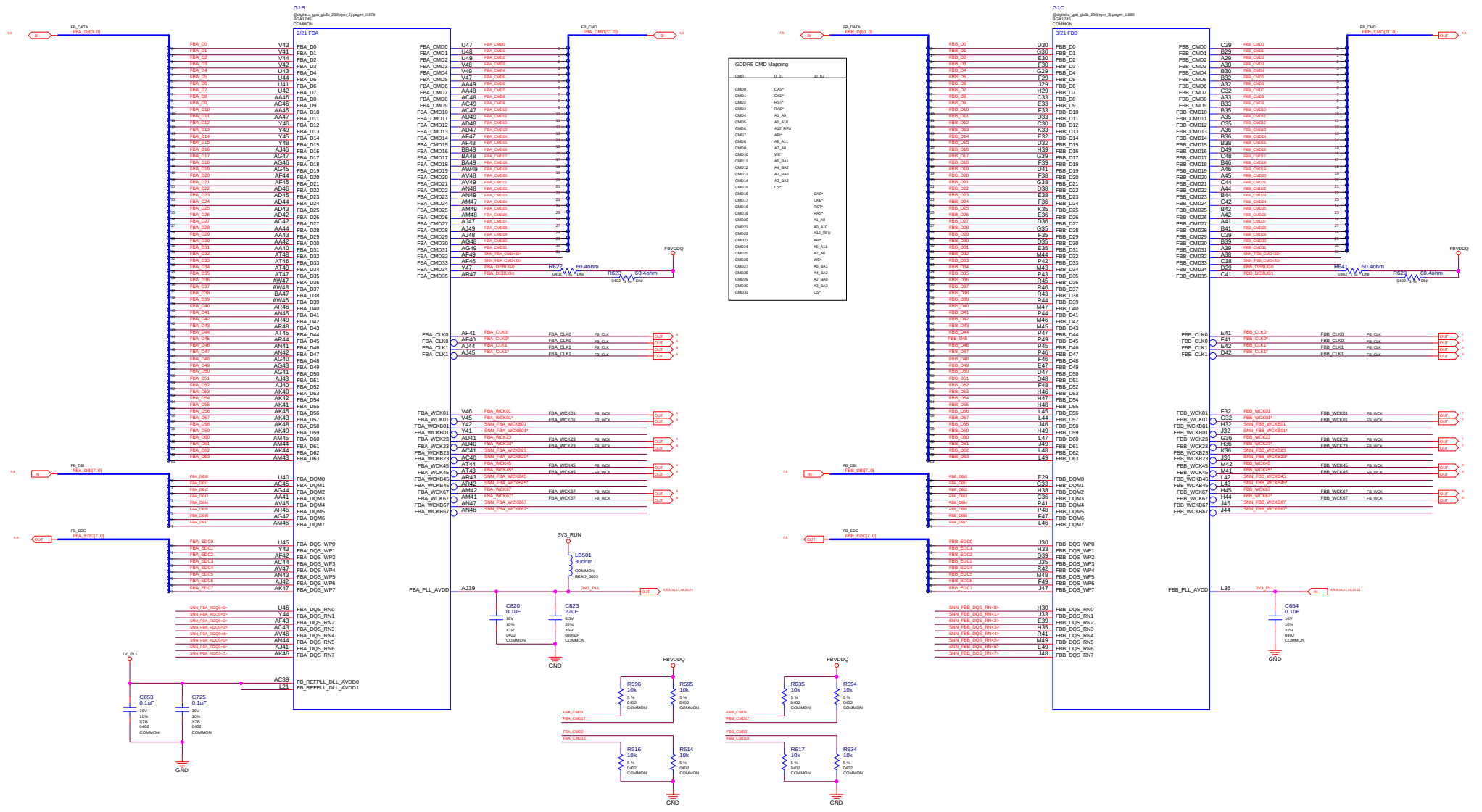
Page4: MEMORY: GPU Partition A/B



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: GPU Partition A/B

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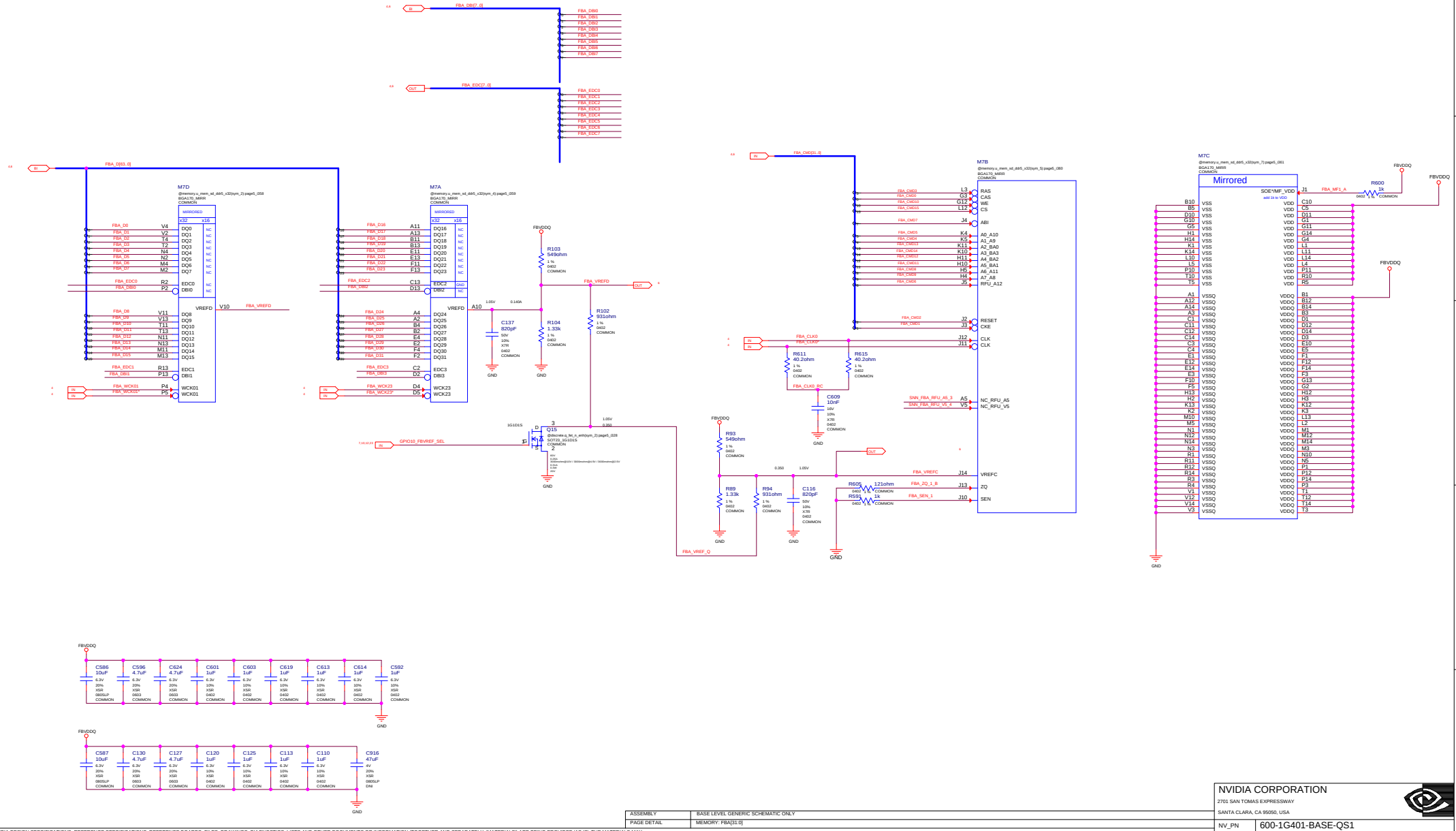
Page5: MEMORY: FBA Partition 31..0



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBA[31:0]

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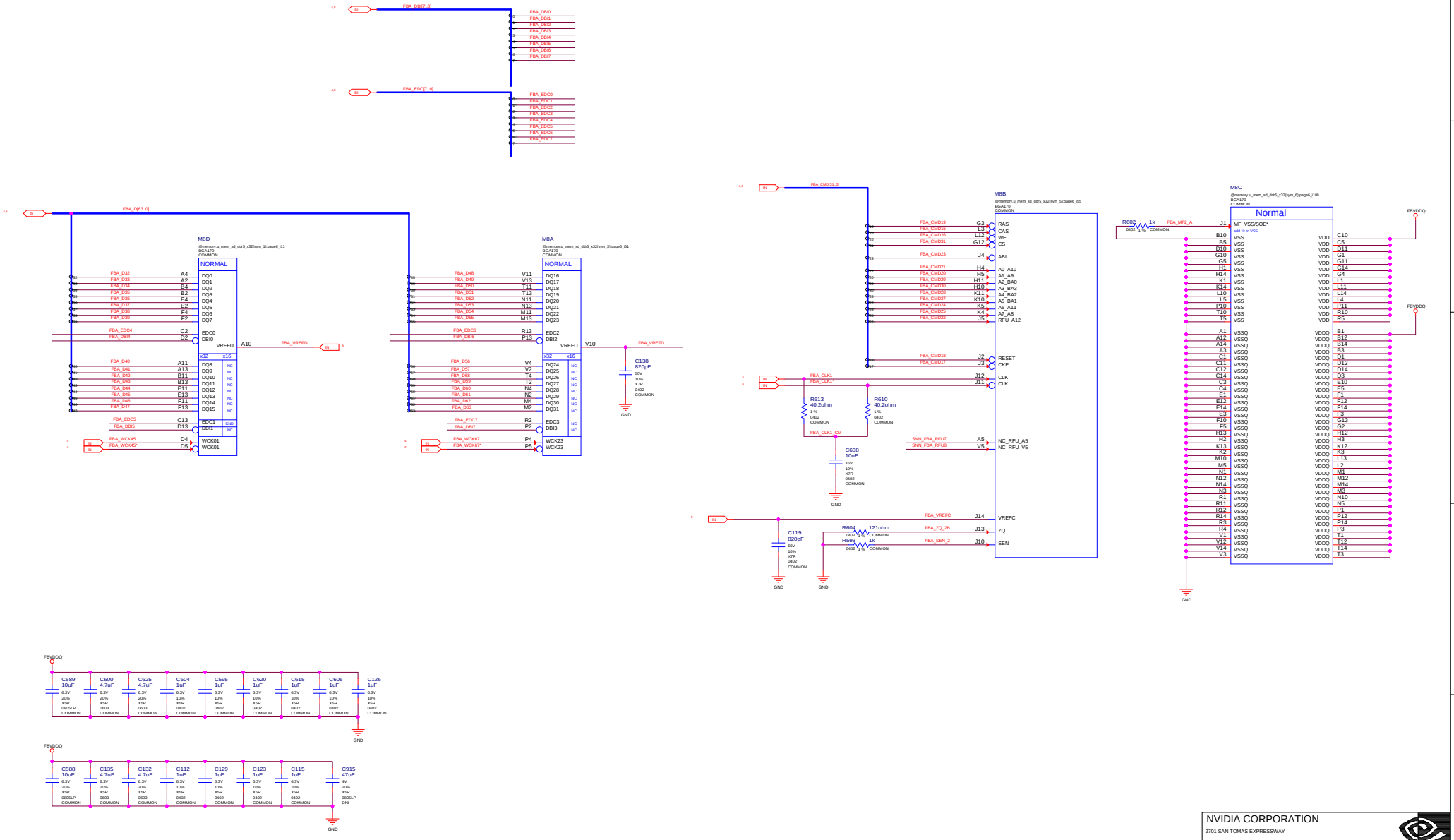
Page6: MEMORY: FBA Partition 63..32



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBA[63:32]

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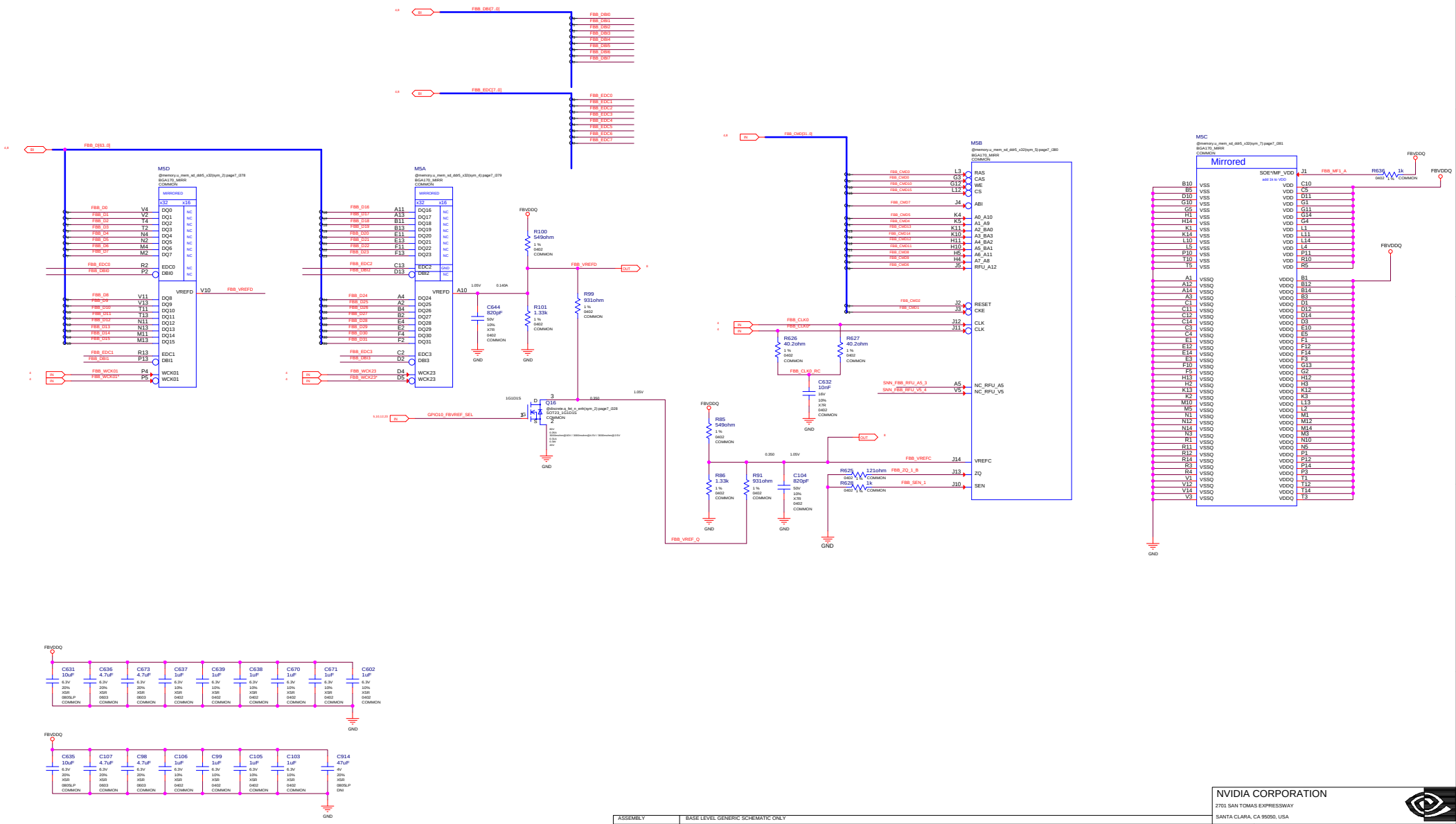
Page7: MEMORY: FBB Partition 31..0



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
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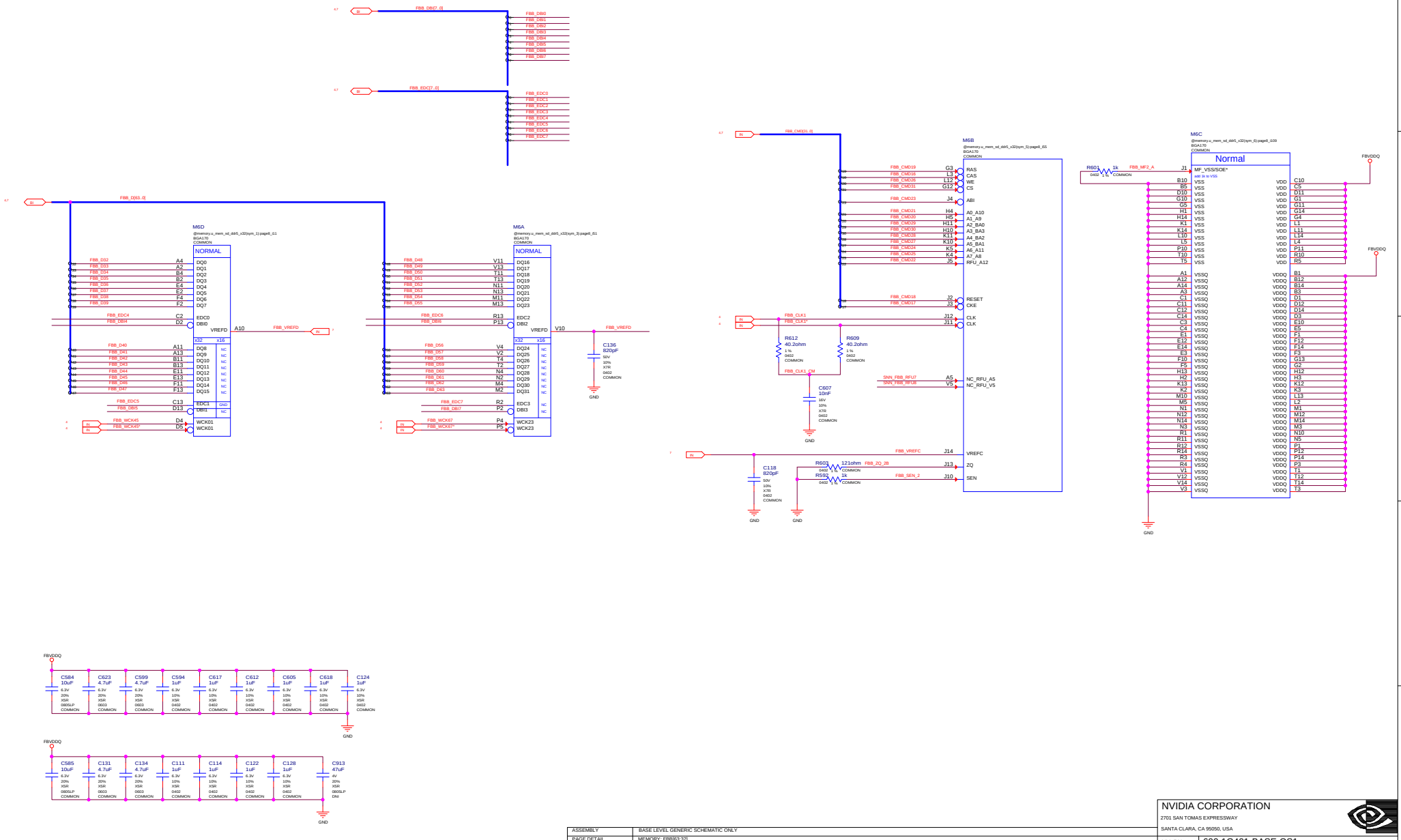
Page8: MEMORY: FBB Partition 63..32



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
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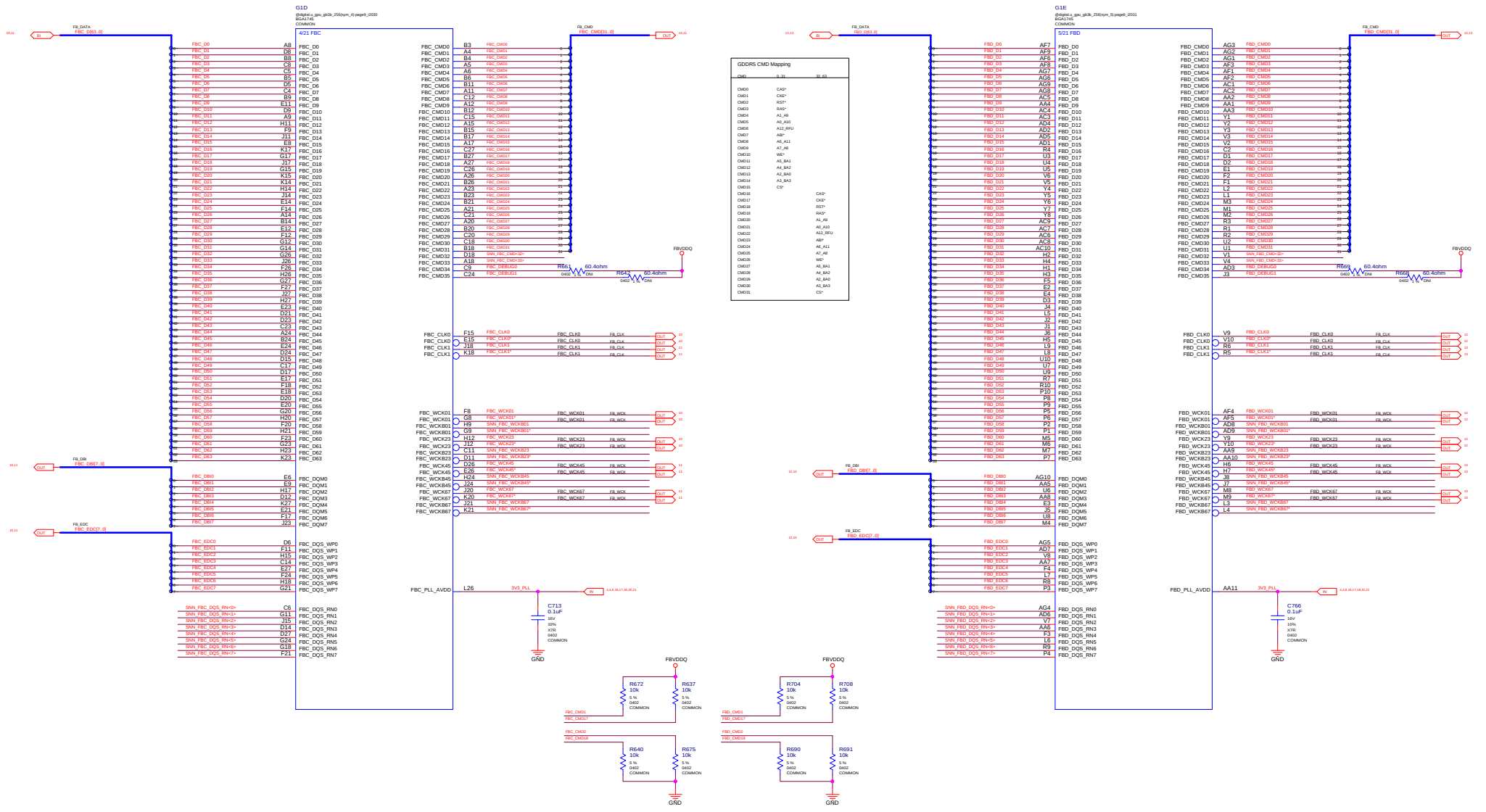
Page9: MEMORY: GPU Partition C/D



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: GPU Partition C/D

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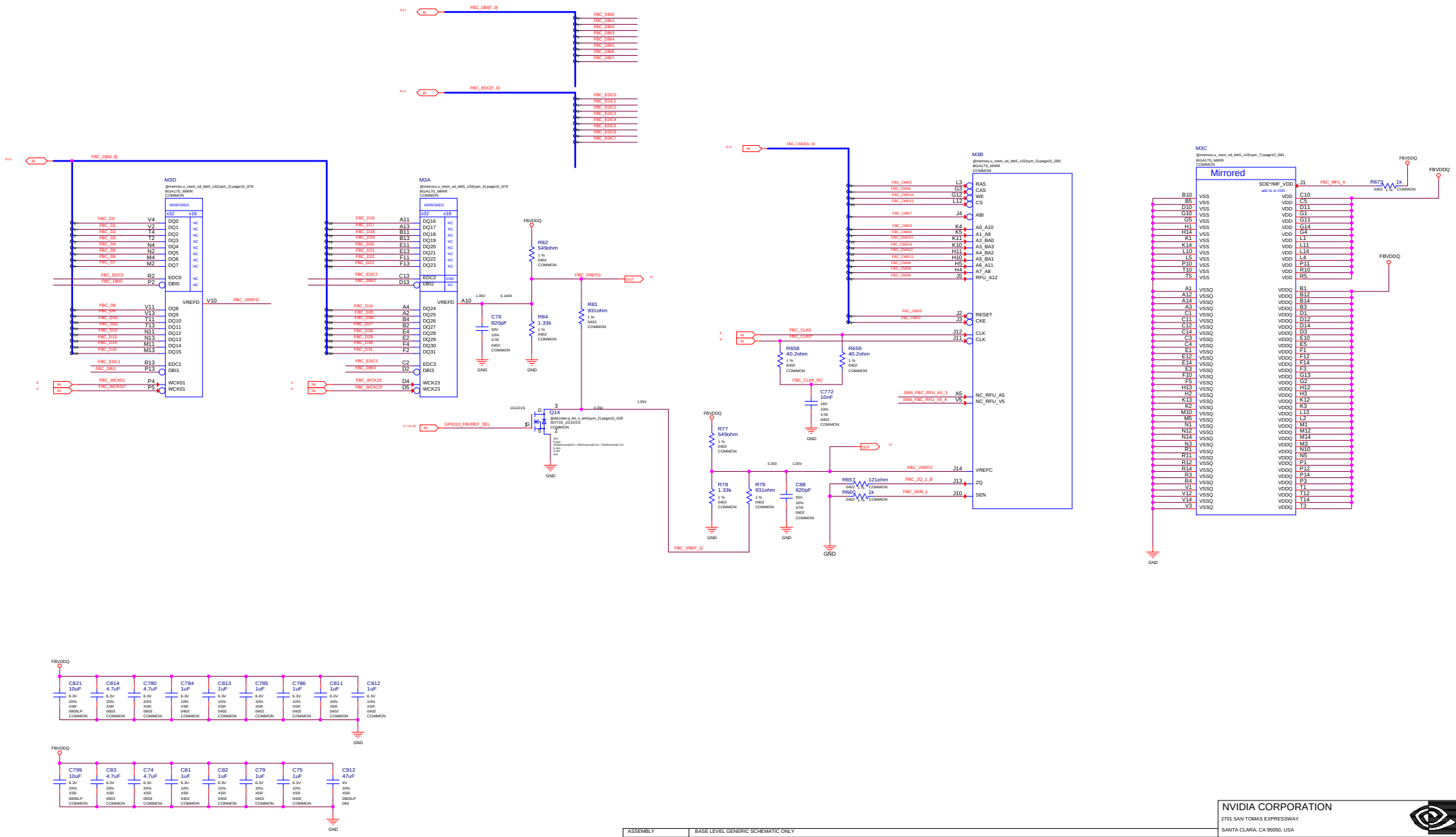
Page10: MEMORY: FBC Partition 31..0



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBC[31:0]

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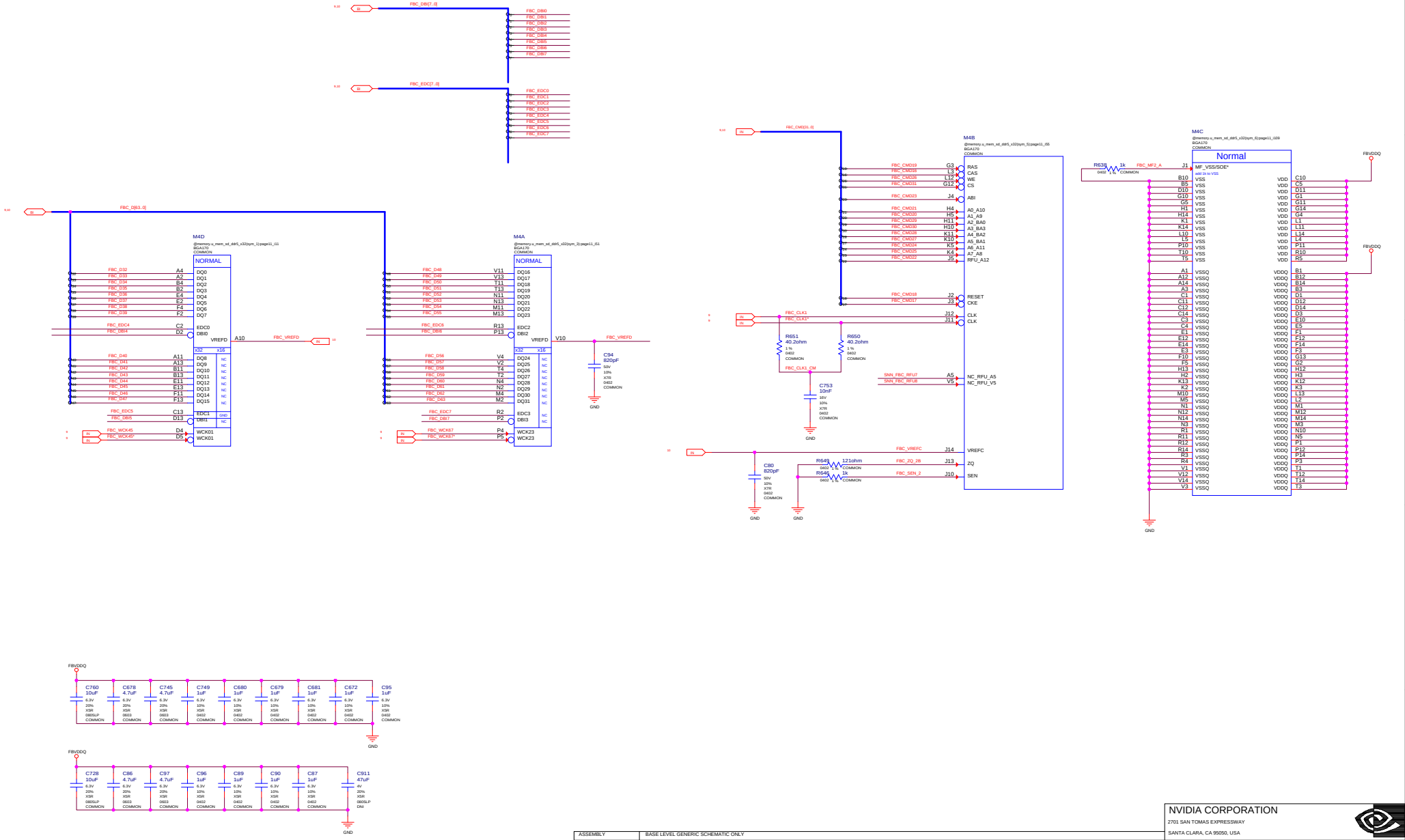
Page11: MEMORY: FBC Partition 63..32



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
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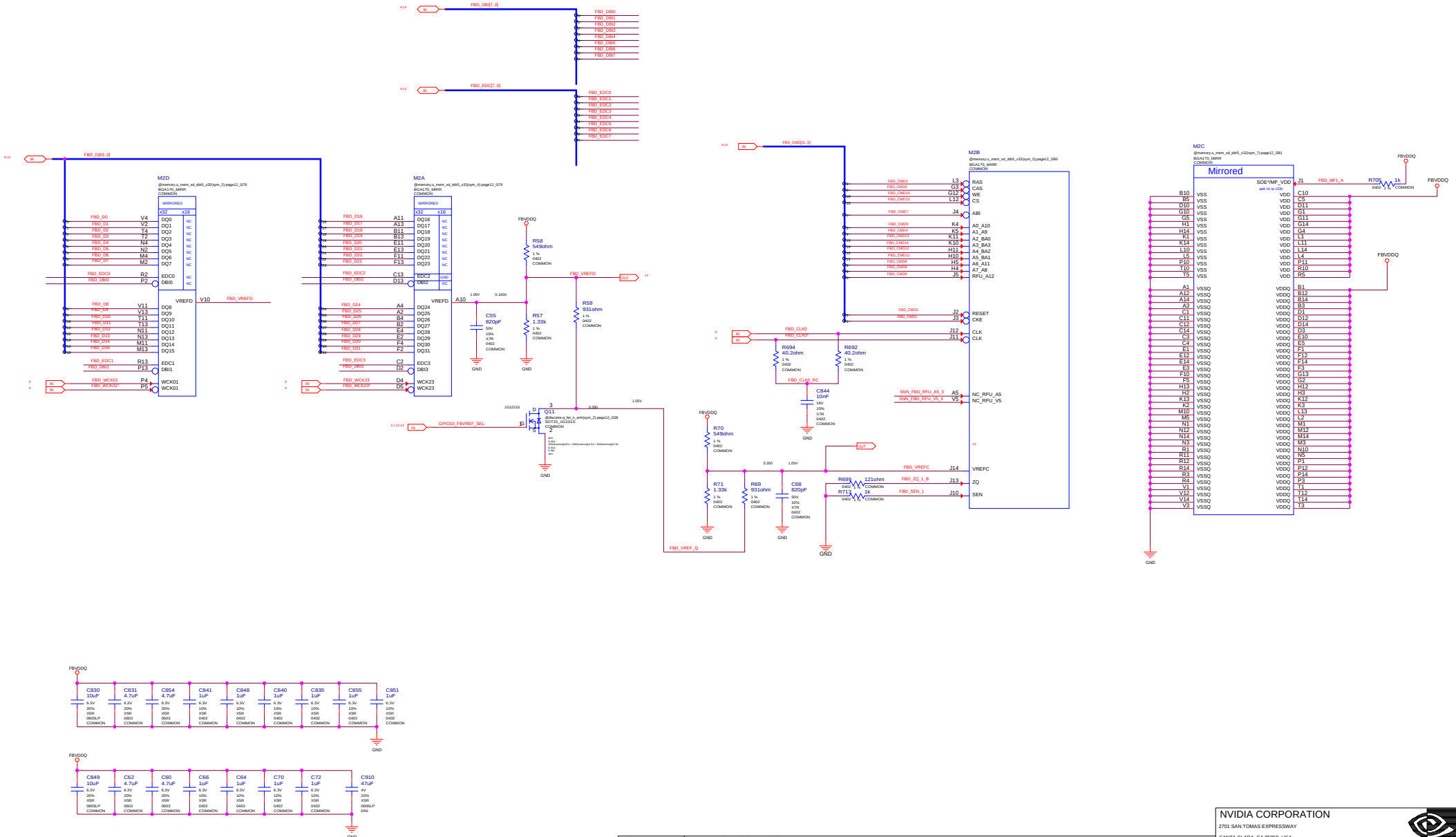
Page12: MEMORY: FBD Partition 31..0



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBD[31:0]

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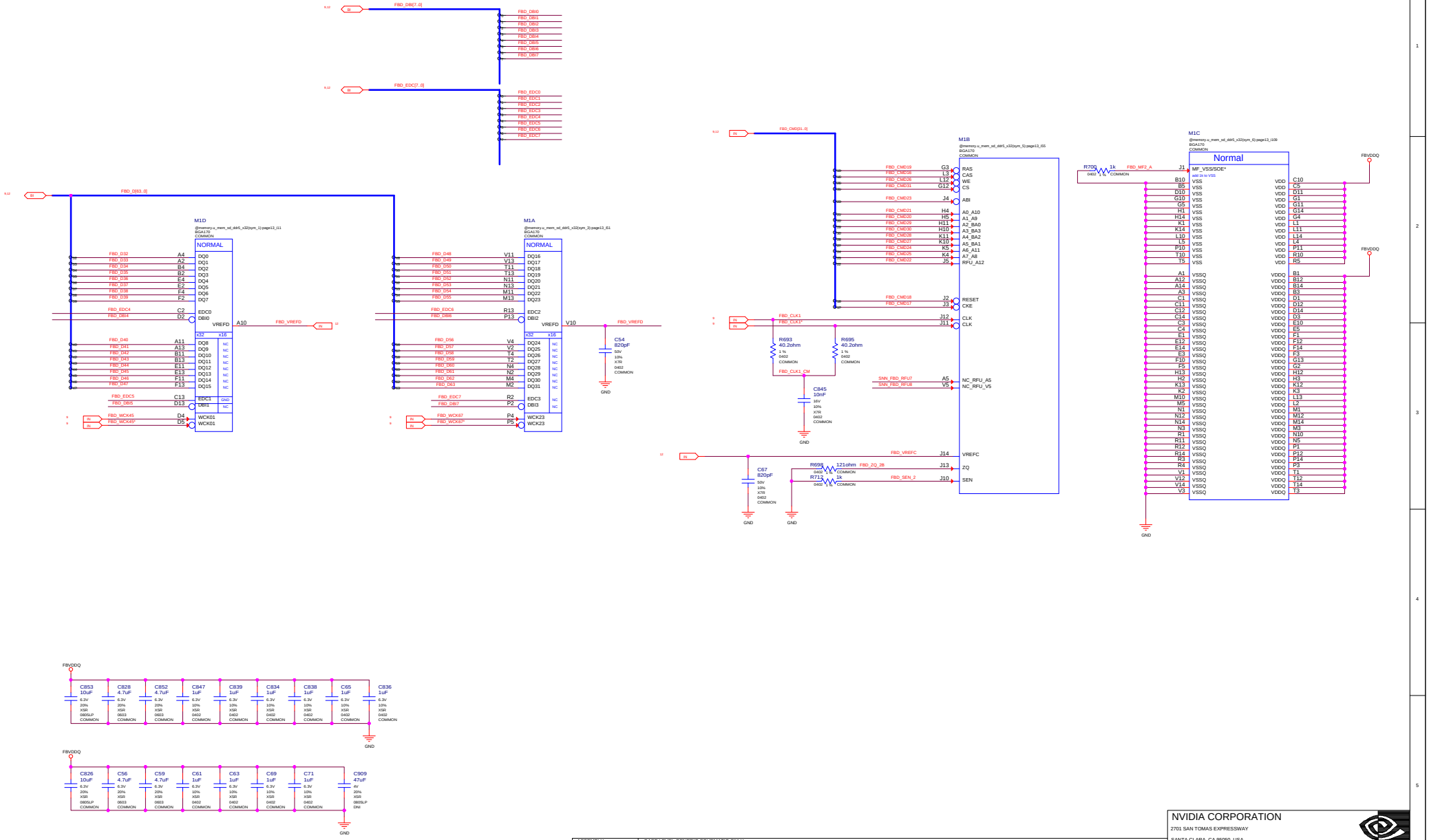
Page13: MEMORY: FBD Partition 63..32



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBD[63:32]

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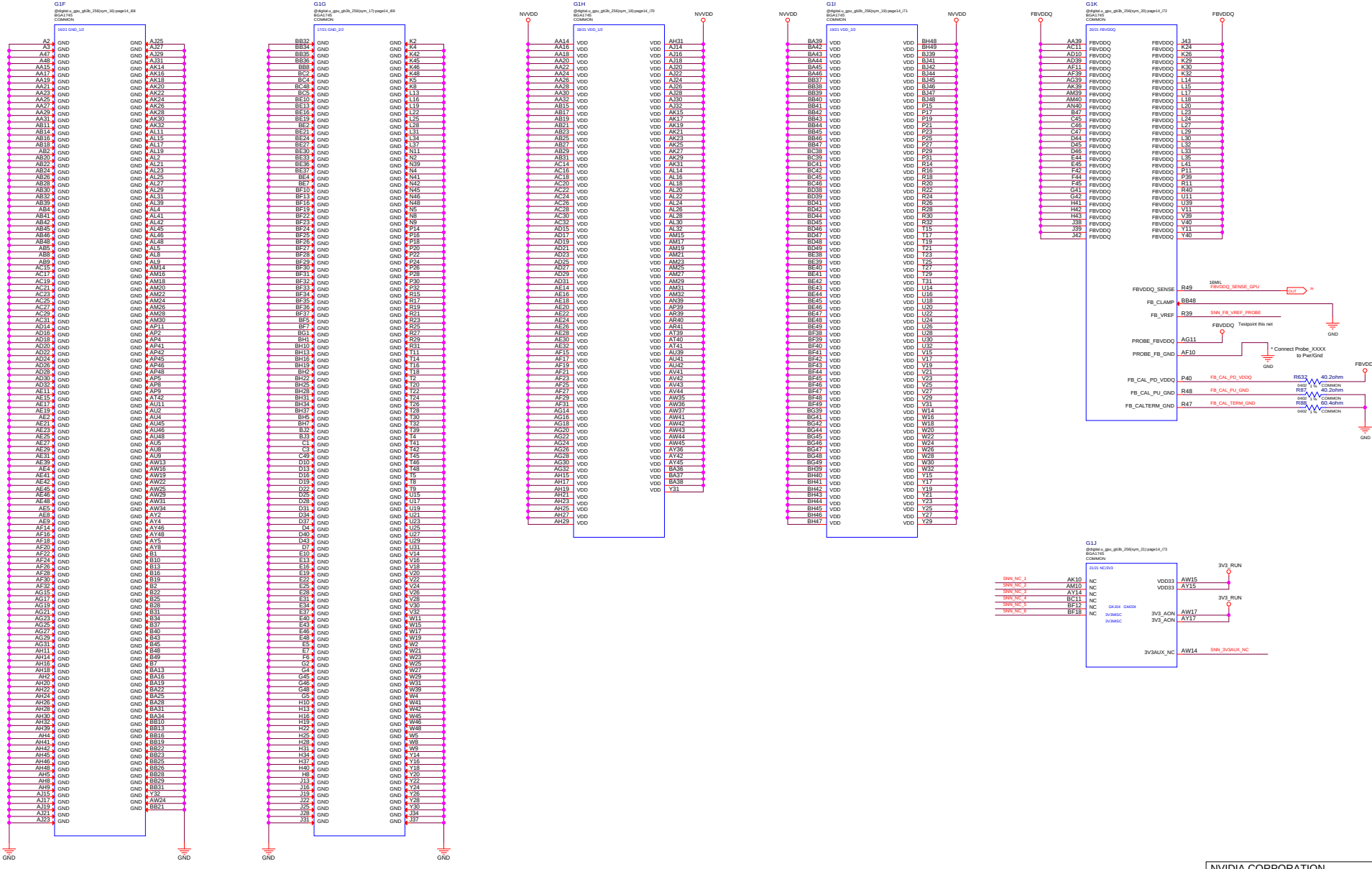
Page14: GPU PWR and GND



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU PWR and GND

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Page15: GPU Decoupling

Based on GB2-X GDDR5 FBVDDQ Decap Guideline

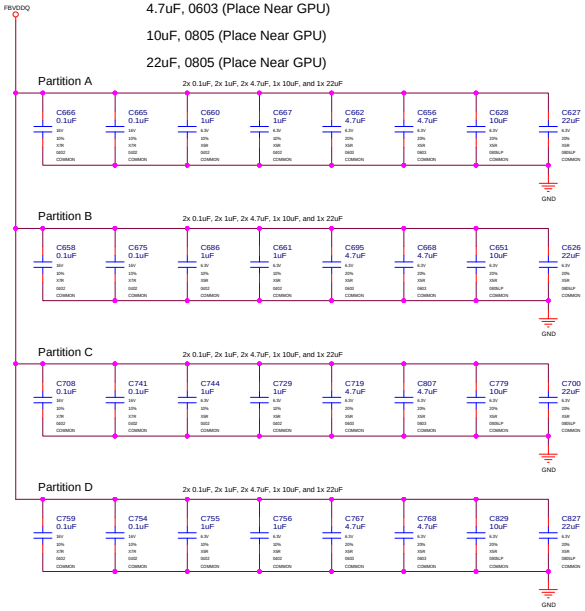
FBVDDQ

0.1uF, 0.47uF & 1uF, 0402 (Place Under GPU)

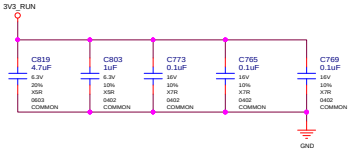
4.7uF, 0603 (Place Near GPU)

10uF, 0805 (Place Near GPU)

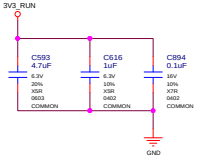
22uF, 0805 (Place Near GPU)



VDD33

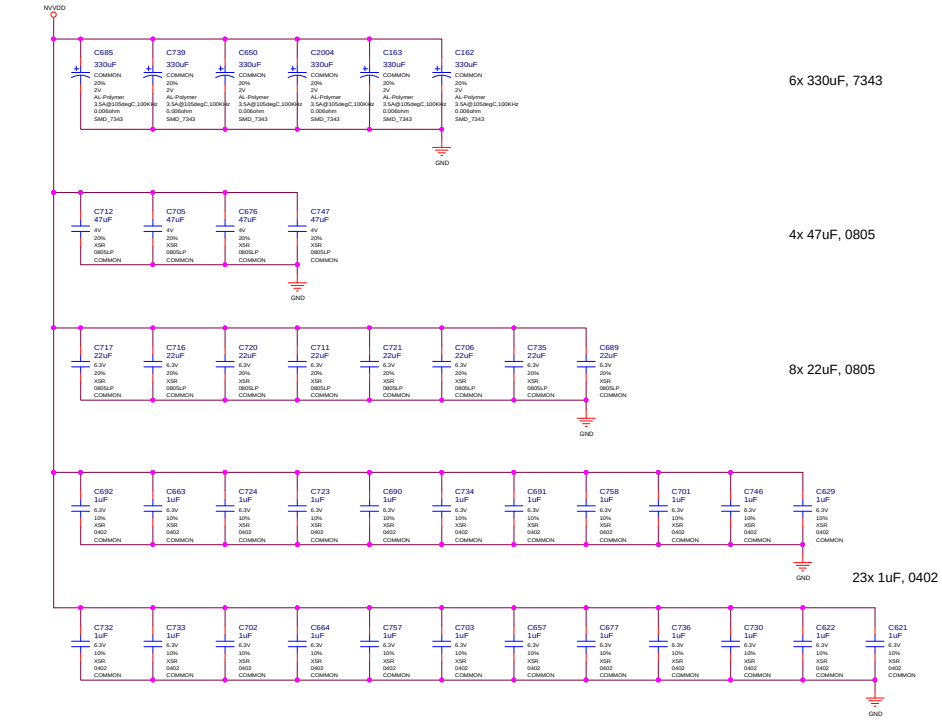


3V3_AON



NVVDD Decoupling caps. Place under GPU.

NVVDD



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU Decoupling

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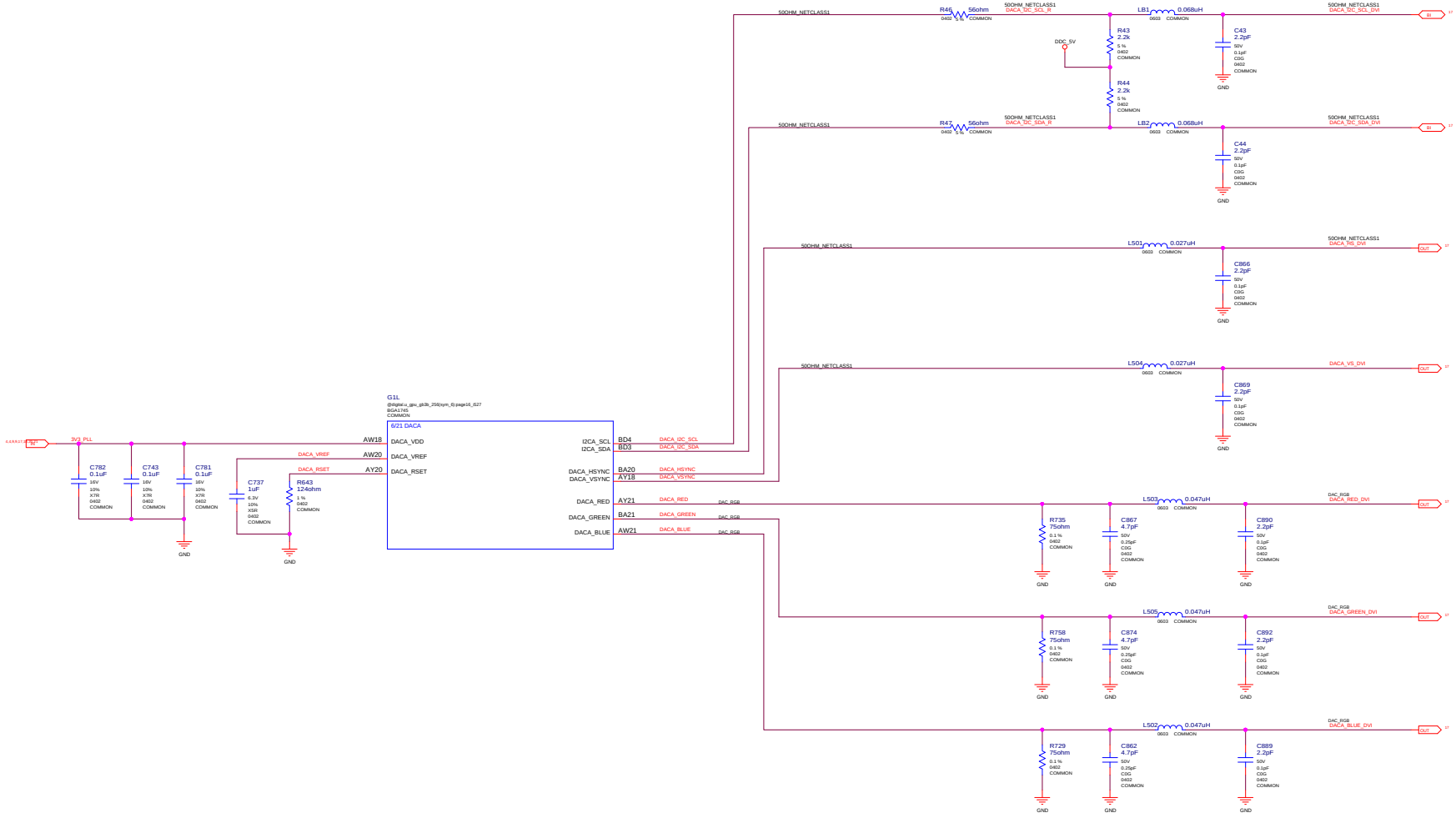
Page16: DACA Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DACA Interface

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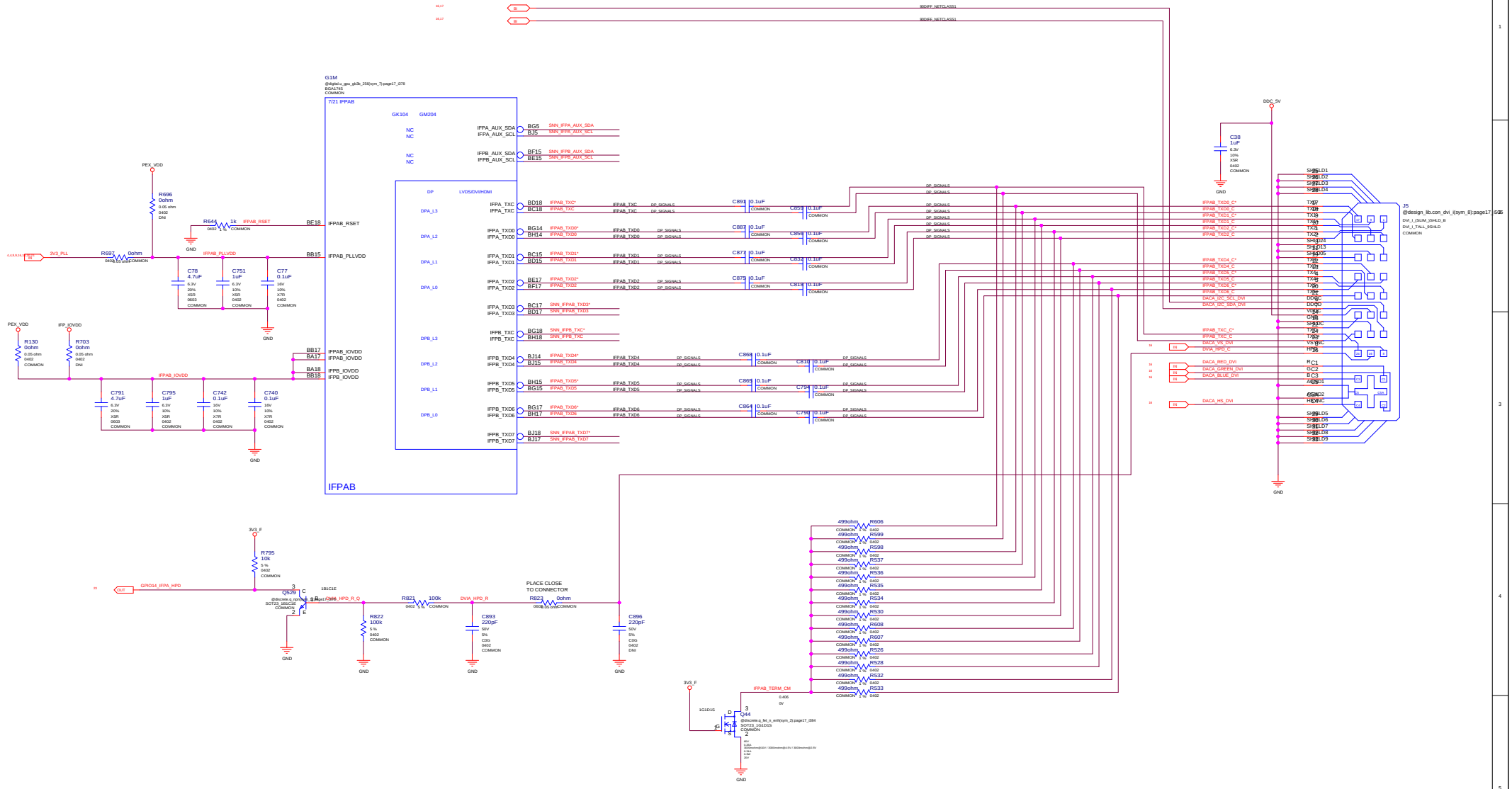
Page17: IFPAB DVI-I-DL



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPAB DVI-I-DL

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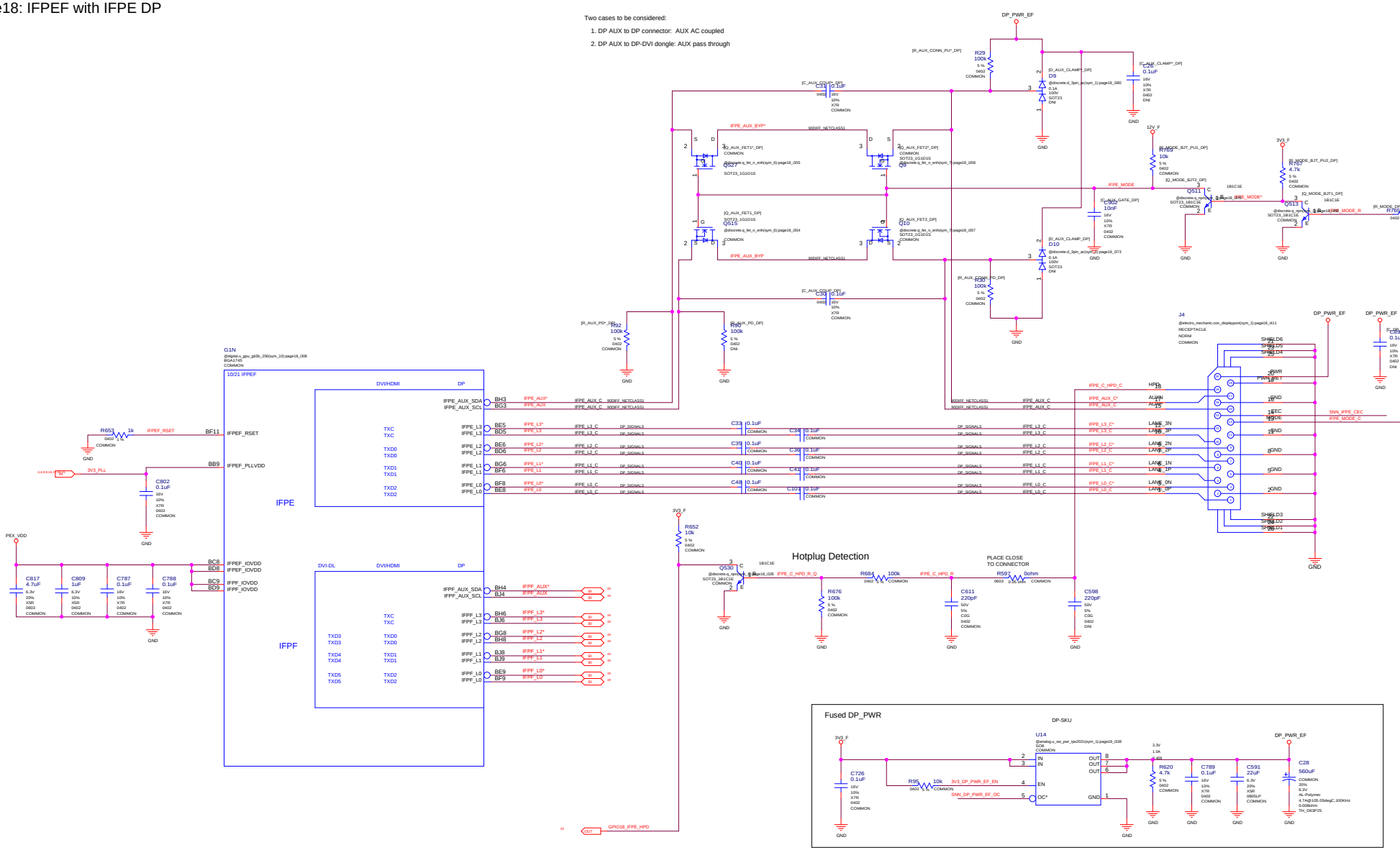
Page18: IFPEF with IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPEF with IFPE DP

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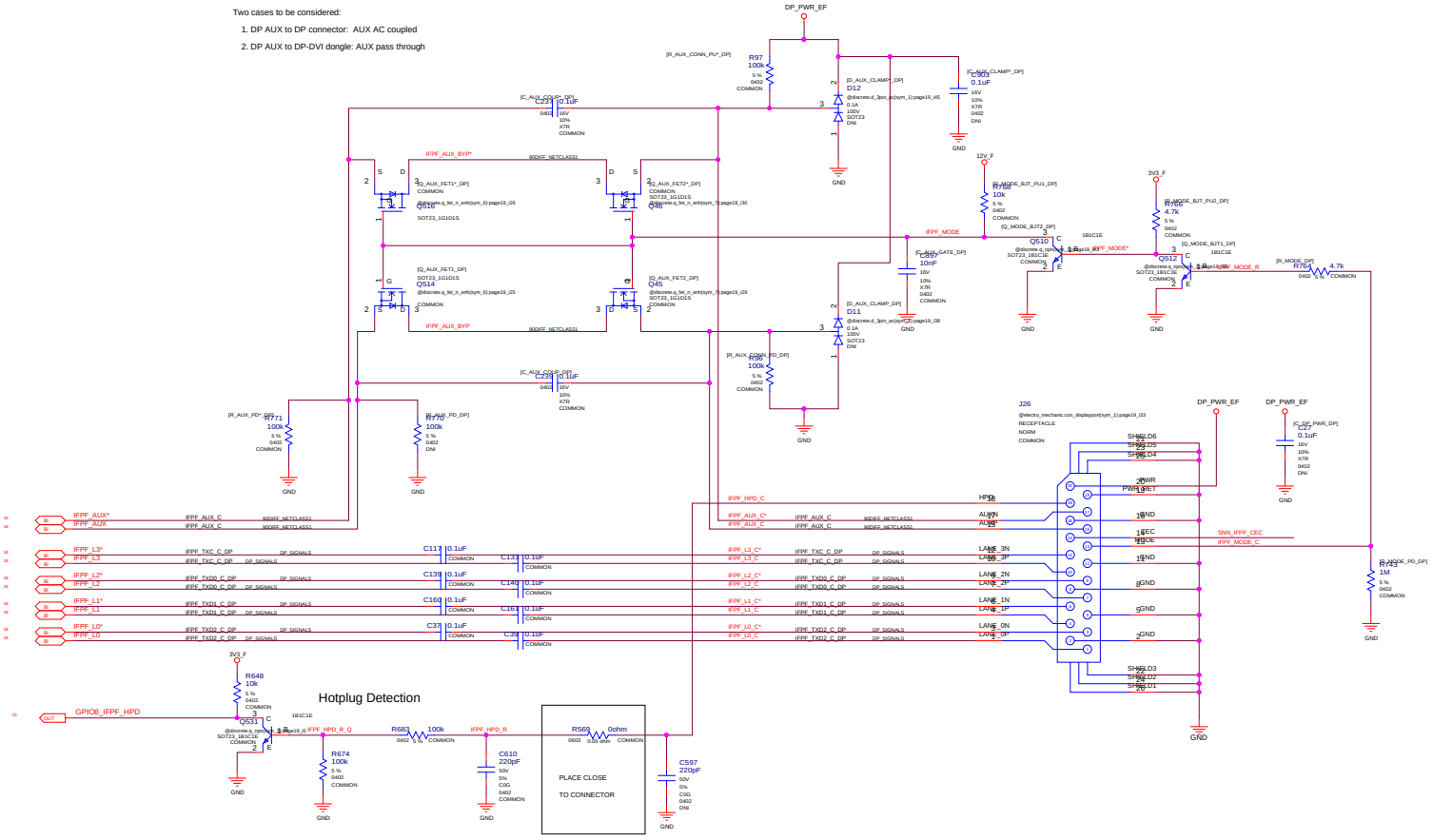
Page19: IFPF DP



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPF DP

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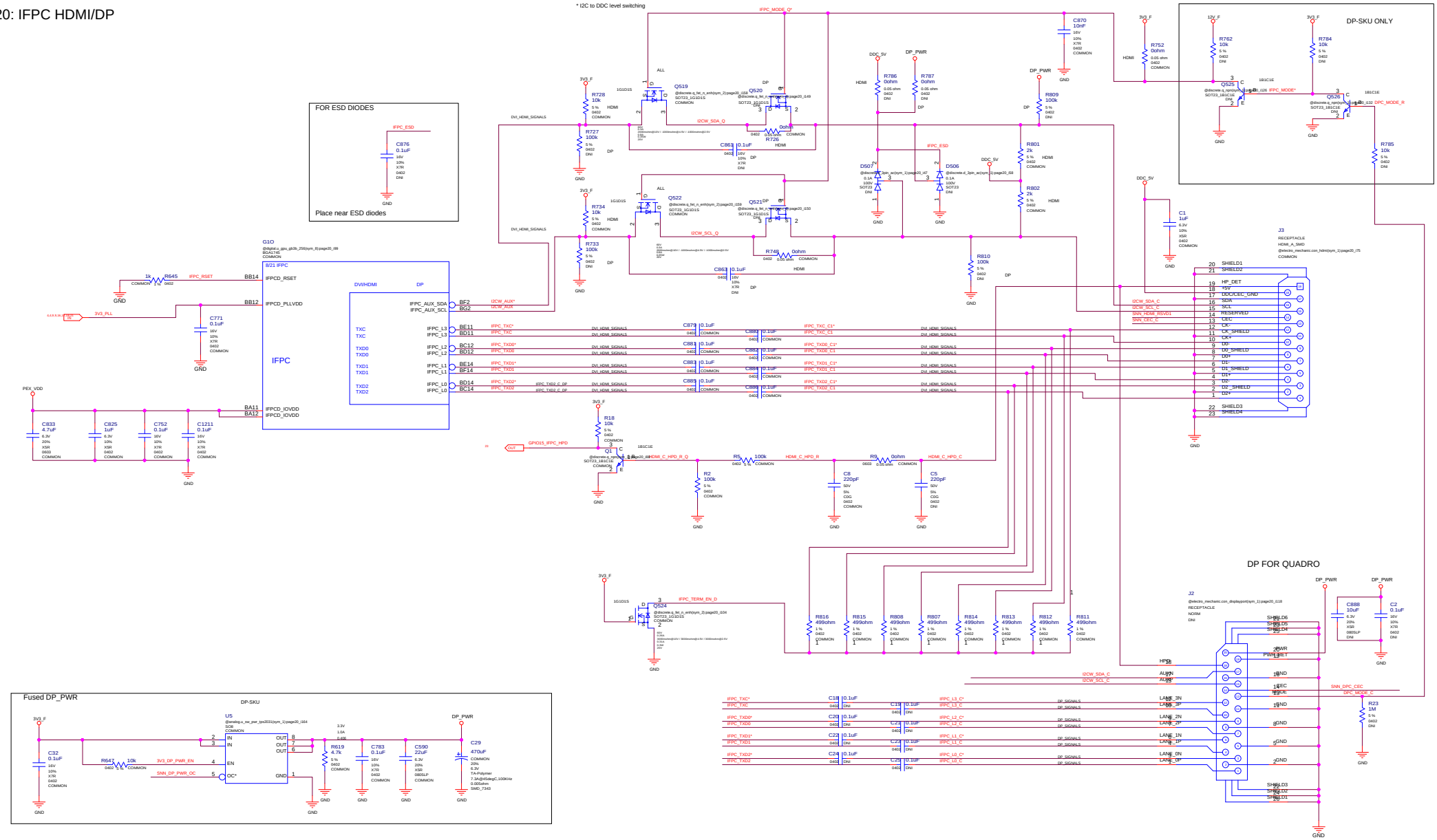
Page20: IFPC HDMI/DP



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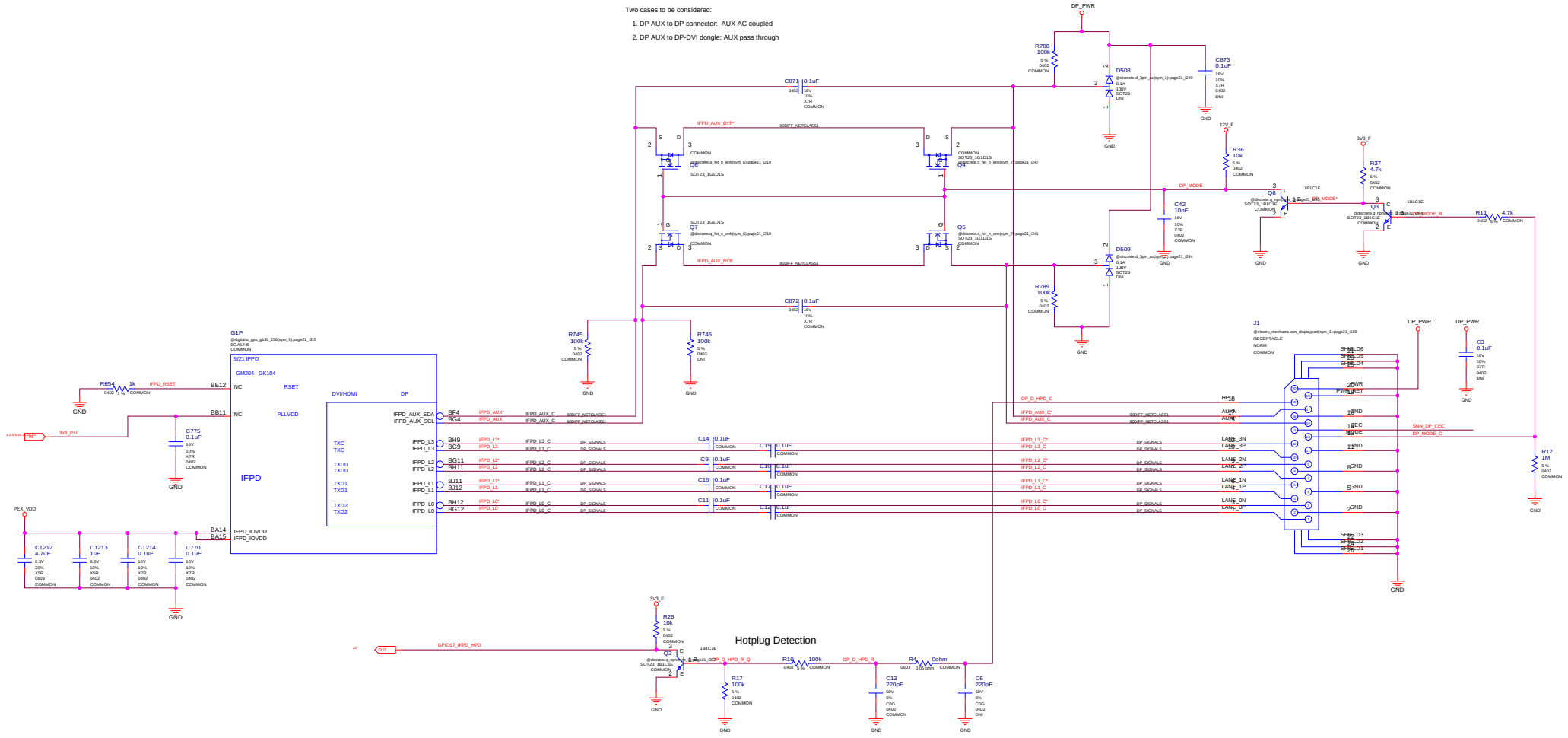
Page21: IFPD DP



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPD DP

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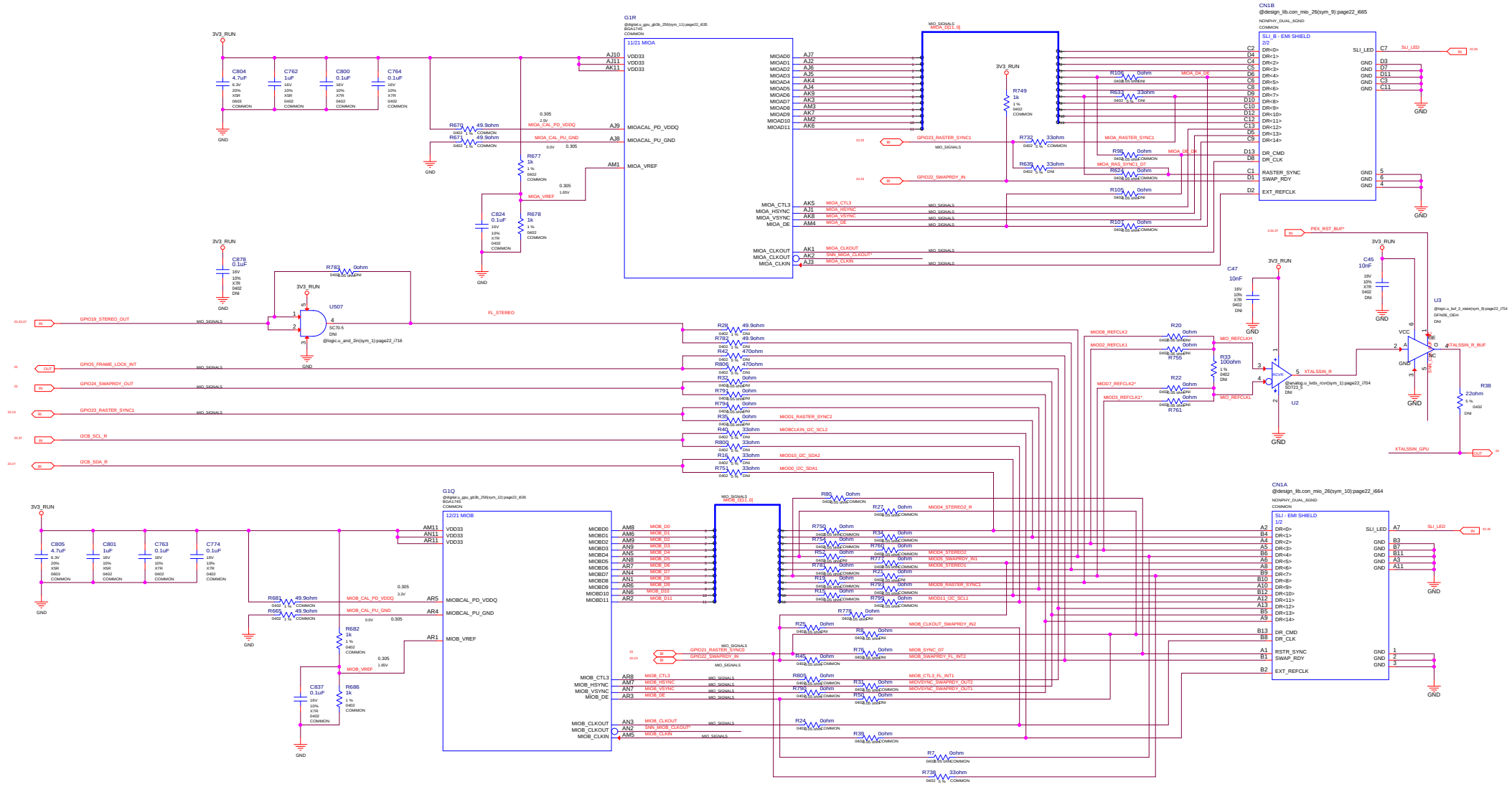
Page22: MIOA/B Interface and FRAME LOCK



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
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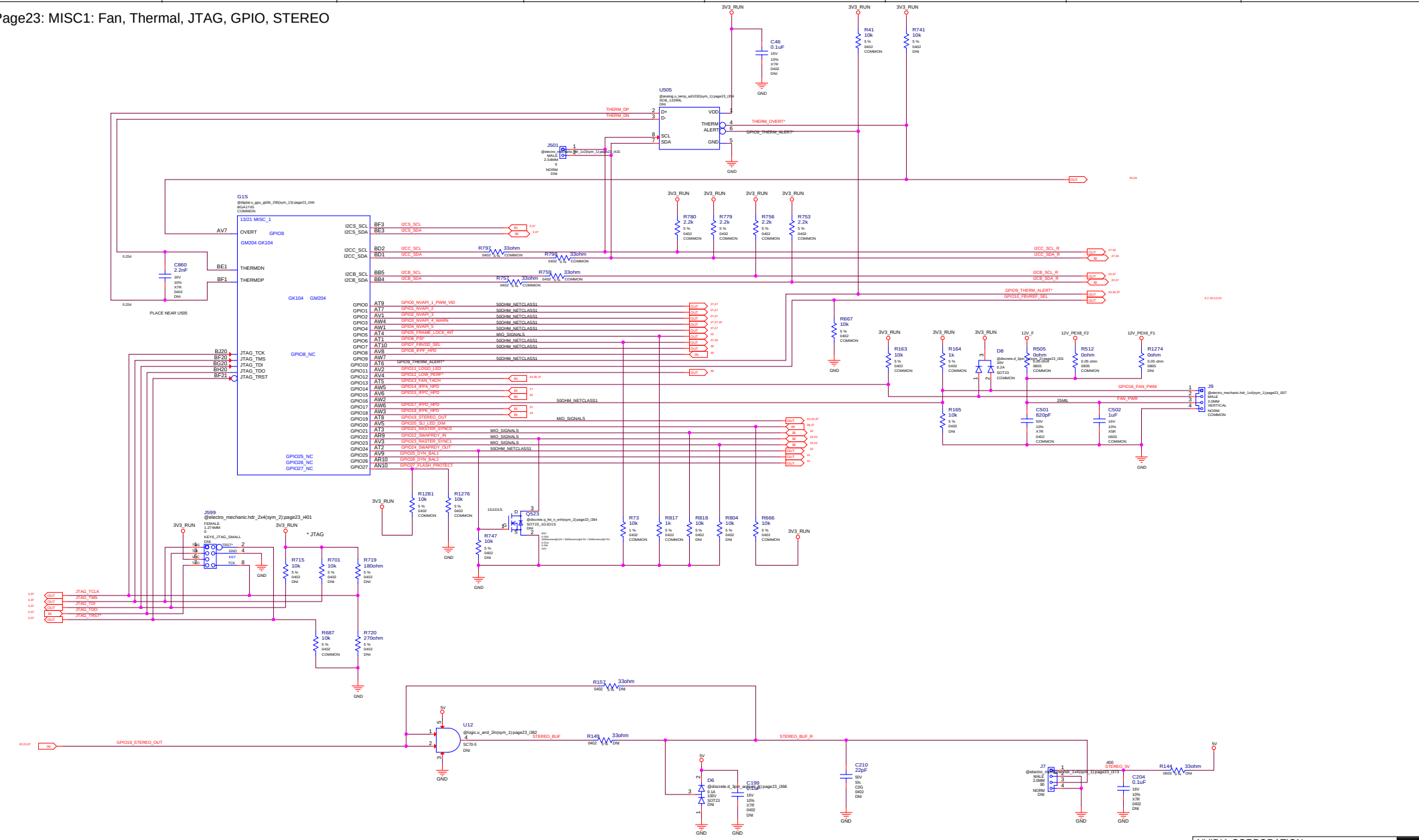
Page23: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO, Stereo

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Page24: MISC2: ROM, XTAL, Straps

	KEPLER			MAXWELL		
STRAP0	USER_BIT [3:0]*	0000*	5K PD*	GC6	SEE TABLE BELOW	
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*			
STRAP2	PCI_DEVID [3:0]*	0100 - (0x1184)*	25K PD -425 GPU*			
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*			
STRAP4	DP_PLL_VDD_33V*	1*	FOR 3_3V*			
	PEX_MAX_SPEED*	1*	FOR GEN2/3*			
	PEX_SPD_CHANGE_GEN3*	1*	ENABLED*			
	*					
ROM_SI	RAMCFG[0]*	1*		RAMCFG[0]*	1*	
	RAMCFG[1]*	1*	0111 for 64Mx32 256 bit SAMSUNG SAMSUNG for SKU 0 primary memory	RAMCFG[1]*	1*	20K PD*
	RAMCFG[2]*	1*	45K PD*	RAMCFG[2]*	0*	
	RAMCFG[3]*	0*		RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*		VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	30k PD*	SMB_ALT_ADDR*	0*	10K PD*
	FB[0]_APERTURE_SIZE*	1*	For 128MB*	PCIE_CFG*	0*	
	FB[1]_APERTURE_SIZE*	0*	For 128MB*	DEVID_SEL*	0*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0*	DISABLED*	SOR0_EXPOSED*	1*	
	PCI_DEVID_EXT[5]*	0*	For 0x1184*	SOR1_EXPOSED*	1*	45K PU*
	SUB_VENDOR*	1*	Dedicated BIOS*	SOR2_EXPOSED*	1*	
	PCI_DEVID_EXT[4]*	0*	For 0x1184*	SOR3_EXPOSED*	1*	

0x13C0

MULTI_STRAP_REF0_GND

BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND

MAXWELL

STRAP0

3.3V	1.65V	0V
GC6+ ISLAND ENABLED	GC6+ DEBUG MODE	GC6+ ISLAND DISABLED

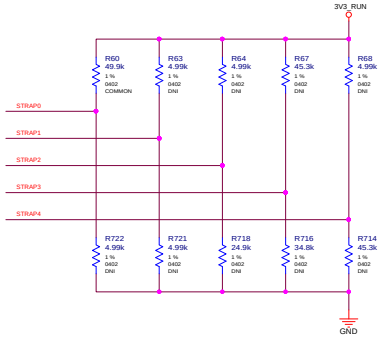
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

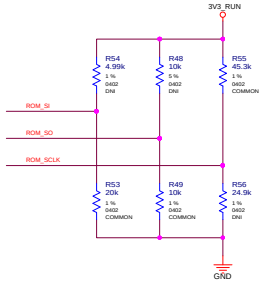
KEPLER

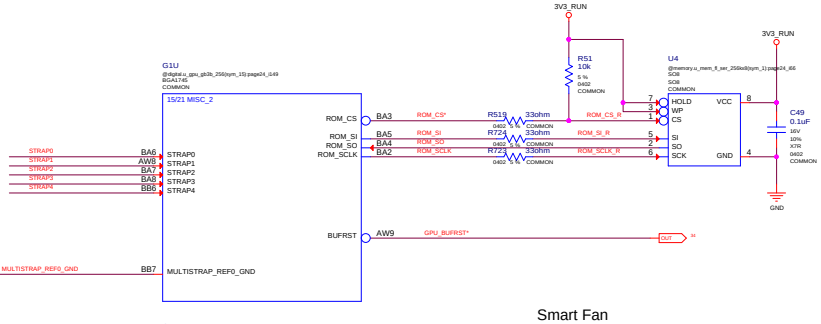
CFG[3:0] Config Width	Vendor
0000	Reserved
0001	32Mx32 256-bit Elpida
0010	32Mx32 256-bit Hynix
0011	32Mx32 256-bit Samsung
0100	Reserved
0101	64Mx32 256-bit Elpida
0110	64Mx32 256-bit Hynix
0111	64Mx32 256-bit Samsung
1000	Reserved
1001	32Mx32 192-bit Elpida
1010	32Mx32 192-bit Hynix
1011	32Mx32 192-bit Samsung
1100	Reserved
1101	64Mx32 192-bit Elpida
1110	64Mx32 192-bit Hynix
1111	64Mx32 192-bit Samsung

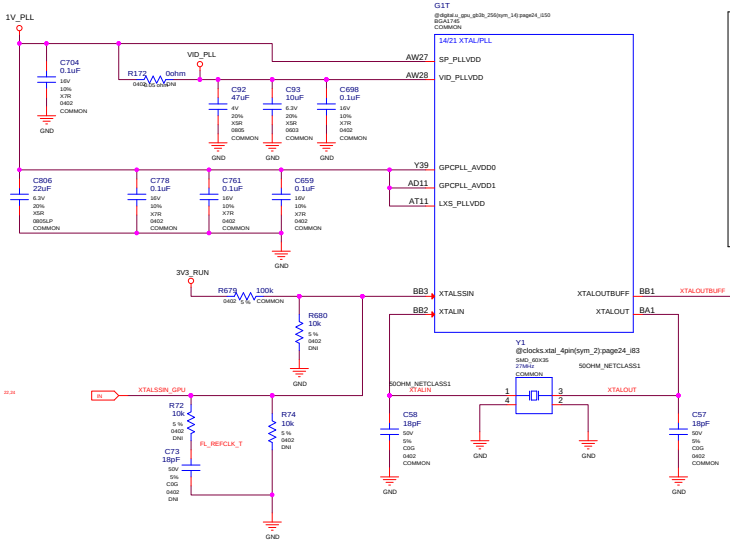
MAXWELL

CFG[3:0] Config Width	Vendor
0000	Reserved
0001	128Mx32 256-bit Elpida
0010	128Mx32 256-bit Hynix
0011	128Mx32 256-bit Samsung
0100	Reserved
0101	64Mx32 256-bit Elpida
0110	64Mx32 256-bit Hynix
0111	64Mx32 256-bit Samsung









Smart Fan

KEPLER

XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

MAXWELL

XTALOUTBUFF

3.3V	1.65V	0V
66% PWM	33% PWM	DISABLED

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC2: ROM, XTAL, Straps

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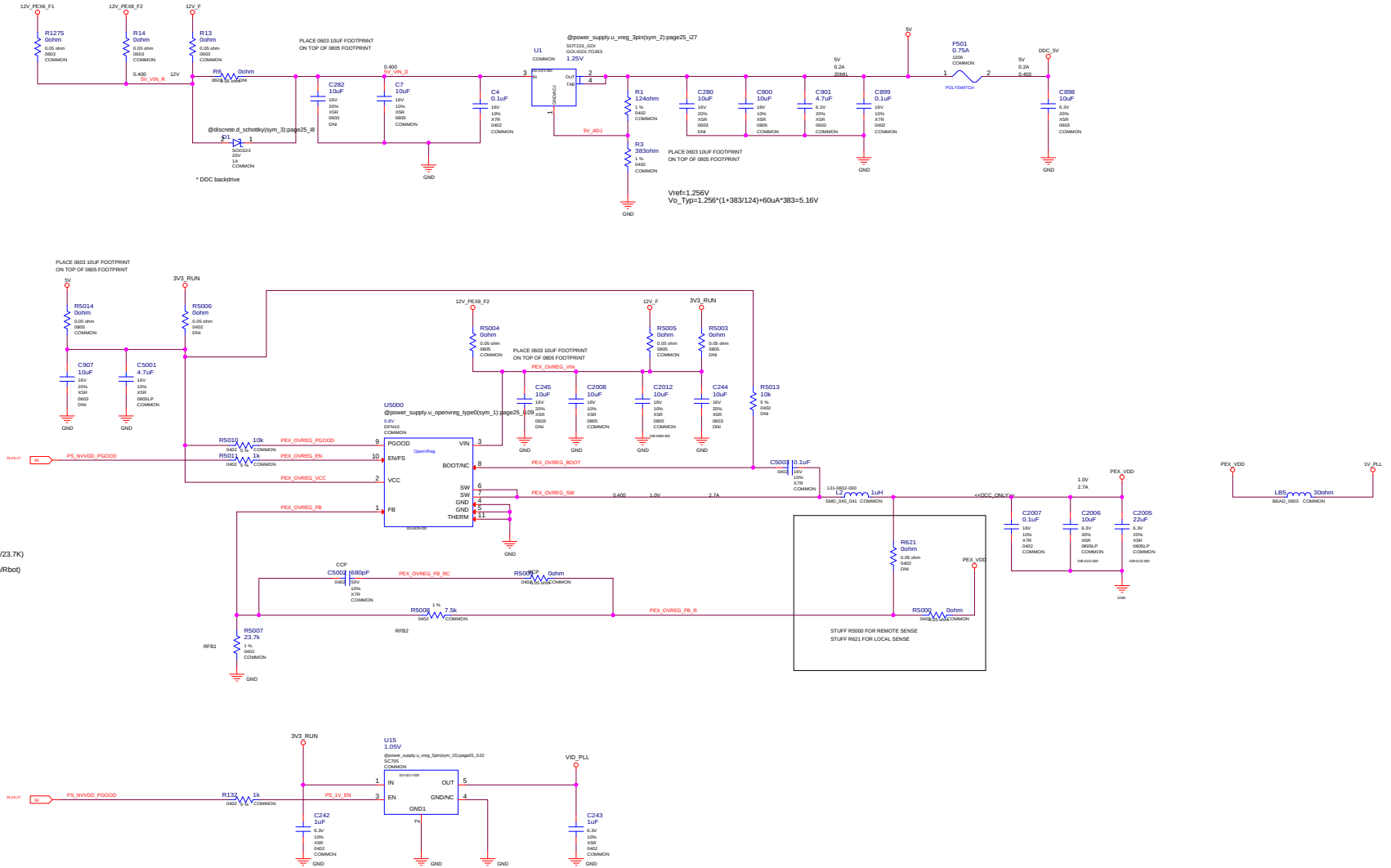
Page25: PS: 5V, PEX_VDD



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 5V, PEX_VDD

NVIDIA CORPORATION
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NV_PN	600-1G401-BASE-QS1		
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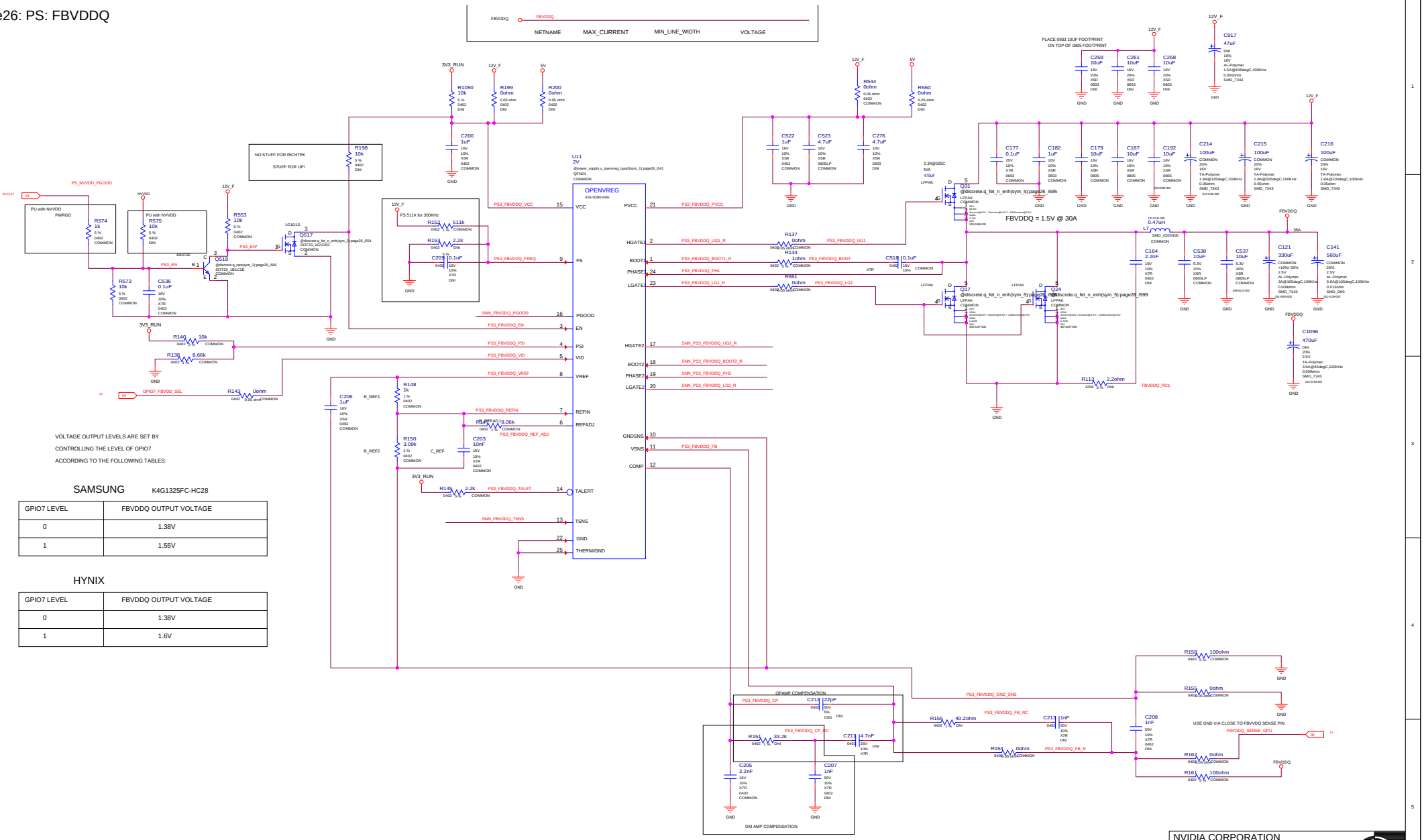
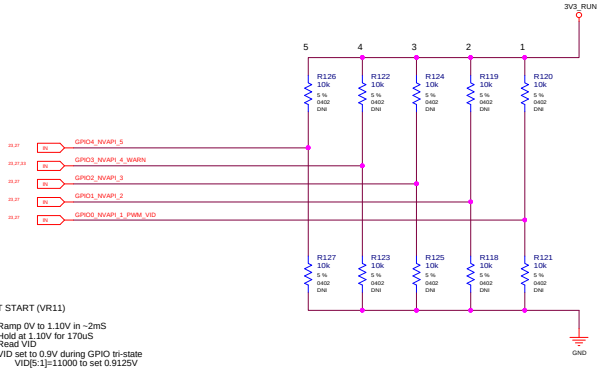
Page26: PS: FBVDDQ



Page27: PS: NVVDD Controller

VID Table

GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

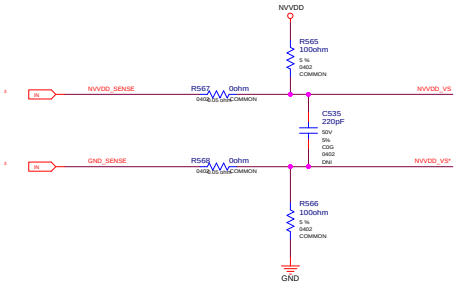


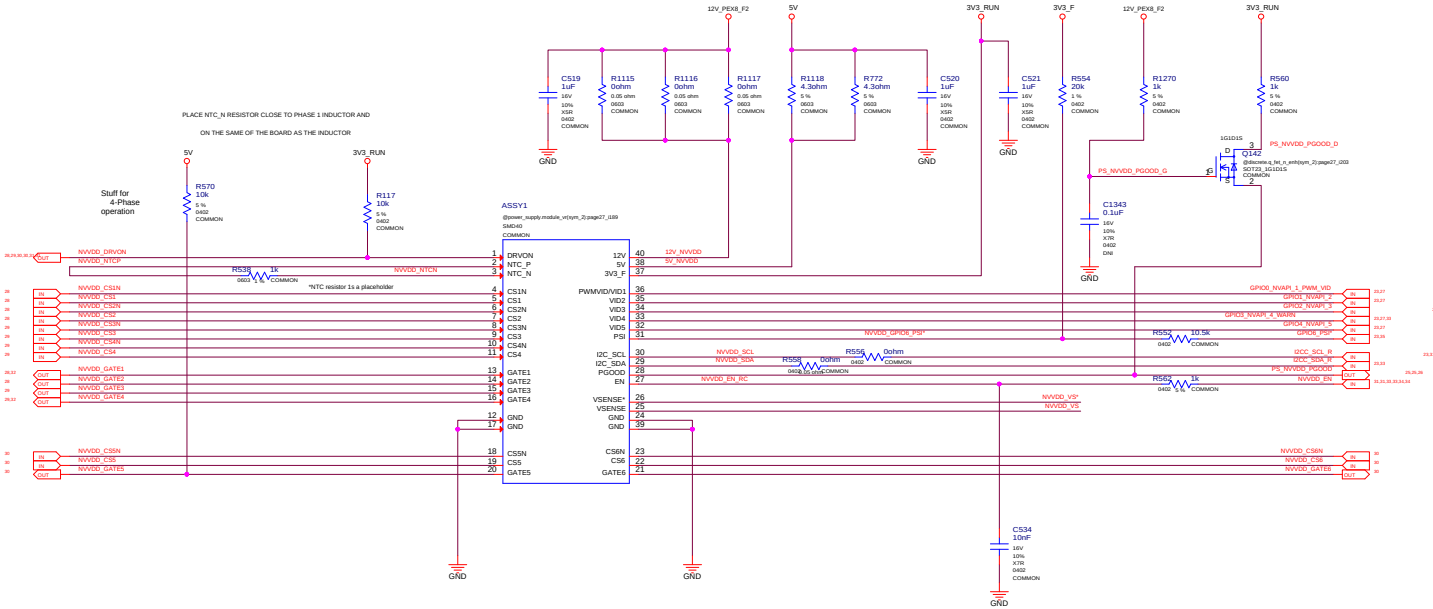
SOFT START (VR11)

1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPIO tri-state
   VID[5:1]=11000 to set 0.9125V

P-STATE VOLTAGES

1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Controller

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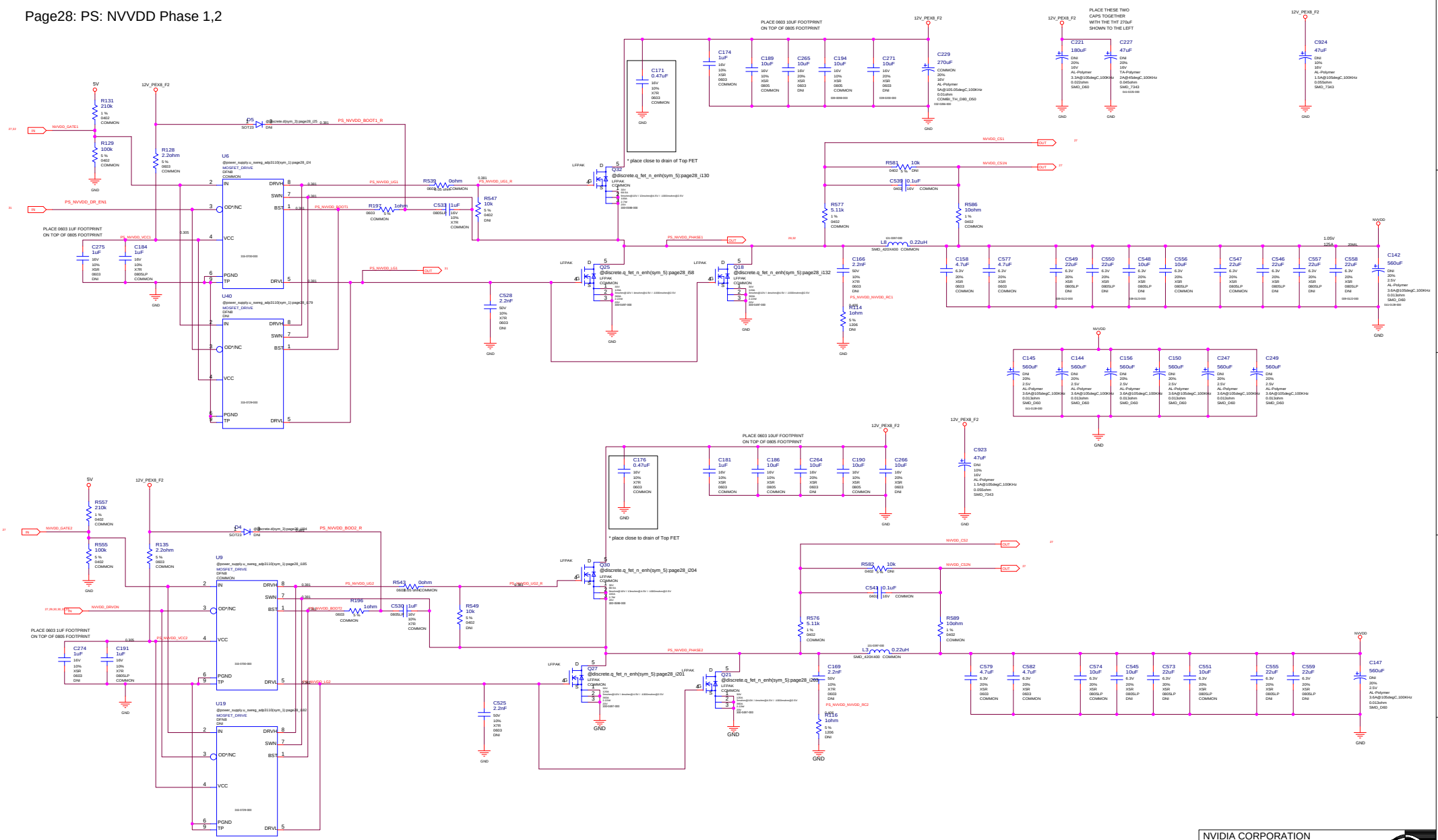
Page28: PS: NVVDD Phase 1,2



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 1,2

NVIDIA CORPORATION
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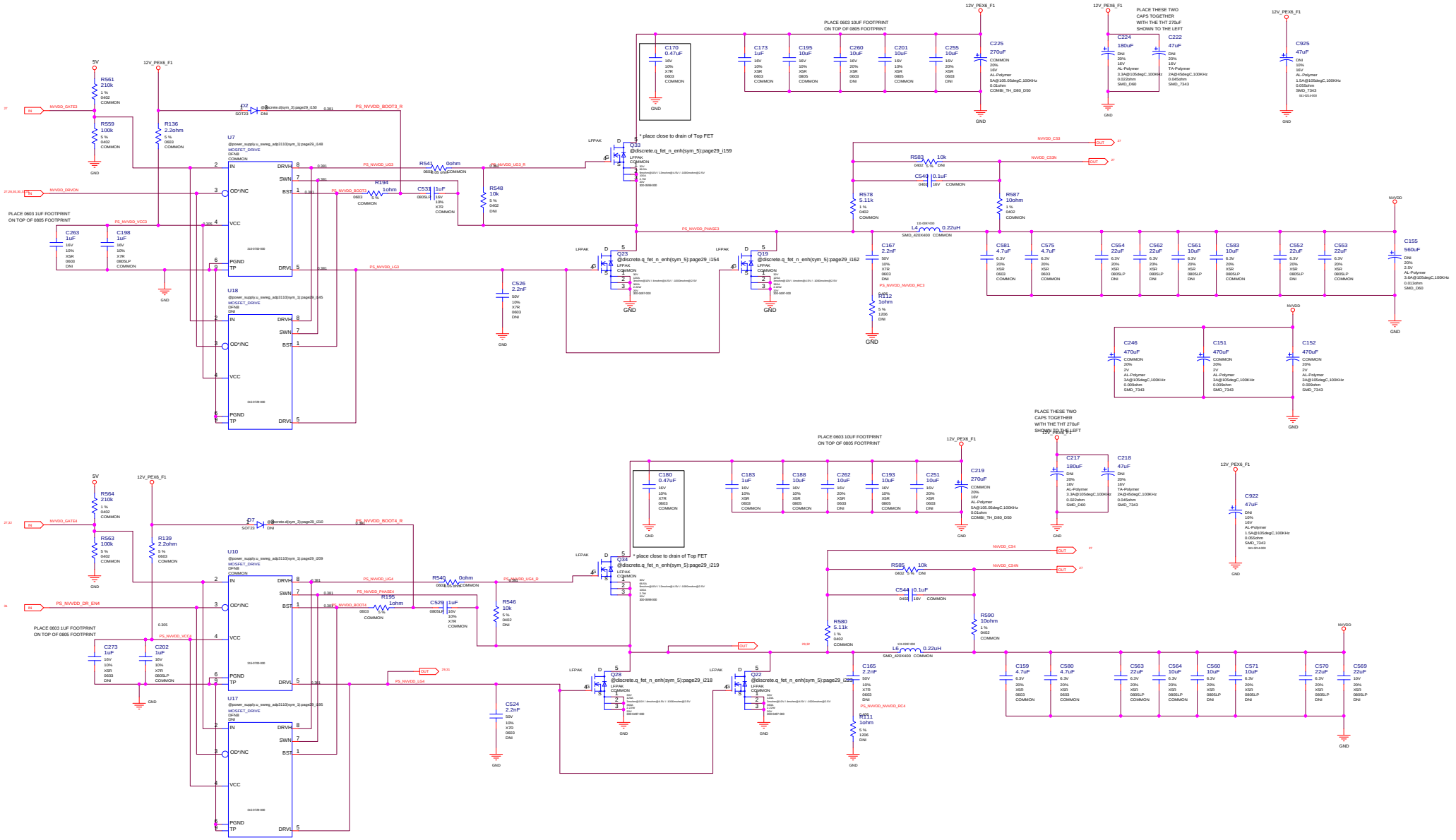
NV_PN	600-1G401-BASE-QS1		
PCB REV	PG401-A02	PAGE	28 OF 37
BOM REV	A	DATE	04-AUG-2014

Page29: PS: NVVDD Phase 3,4



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 3,4

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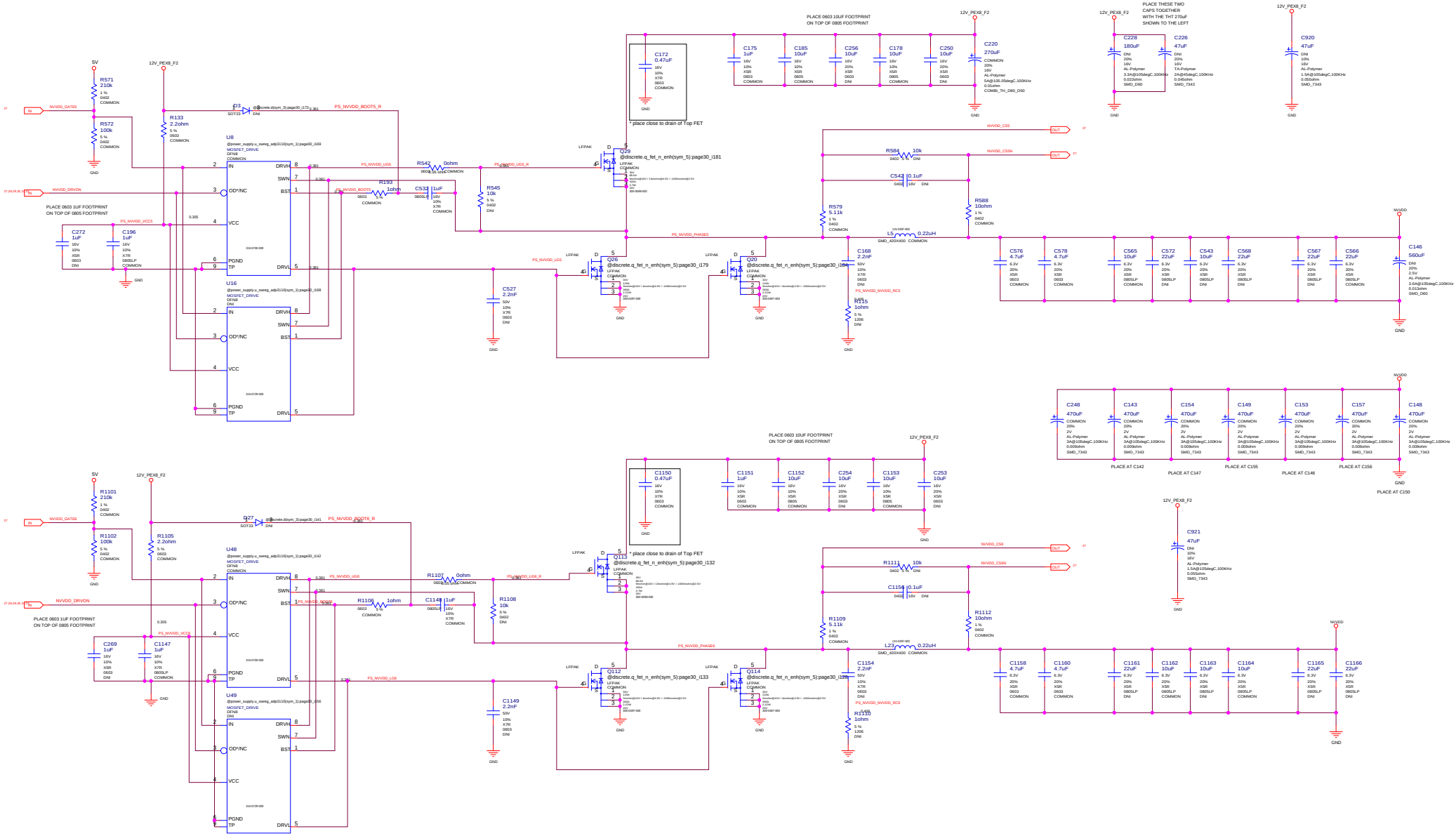
Page30: PS: NVVDD Phase 5,6



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 5, 6

NVIDIA CORPORATION
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NV_PN	600-1G401-BASE-QS1		
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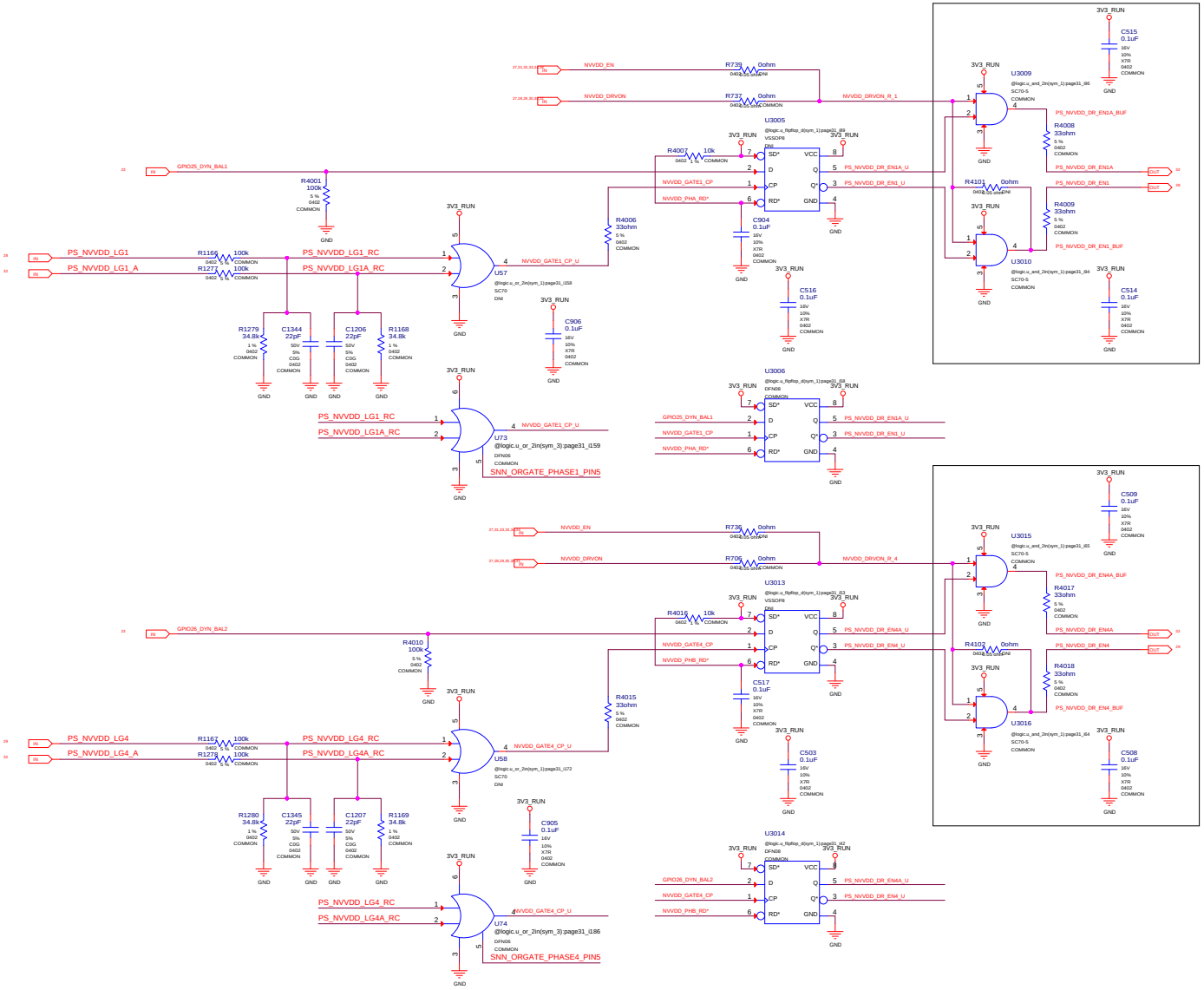
Page31: PS: Dynamic Power Balance Logic



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Dynamic Power Balance Logic

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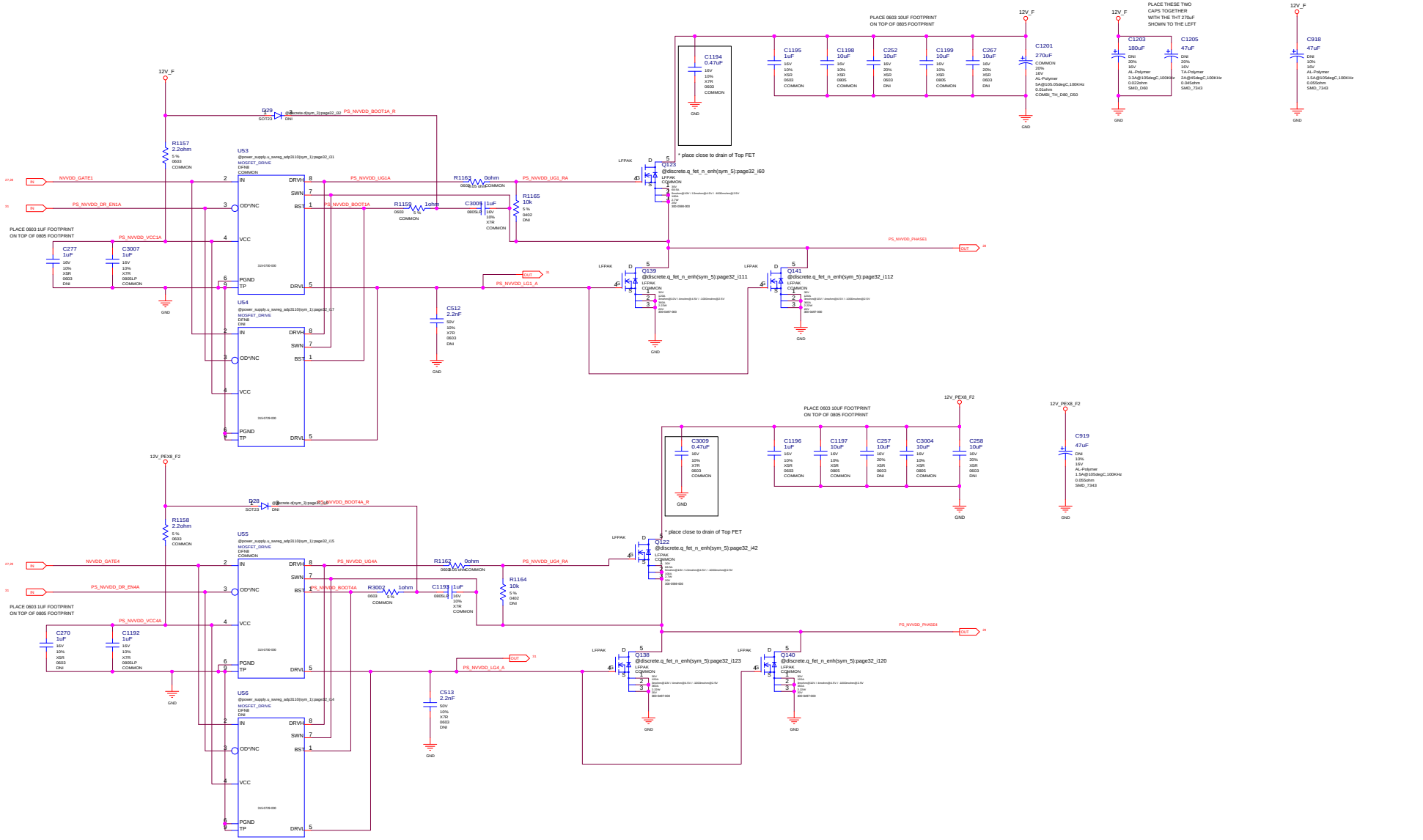
Page32: PS: Dynamic Power Balance Phases



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Dynamic Power Balance Phases

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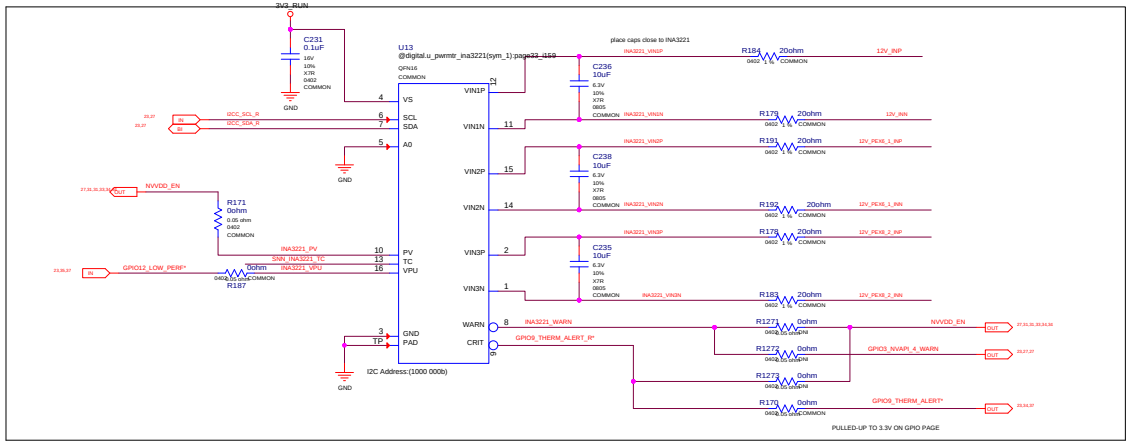
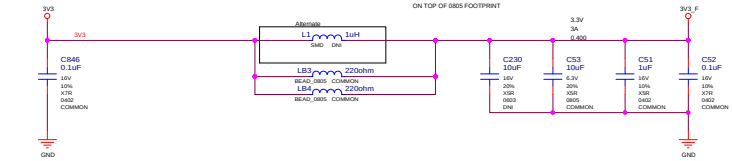
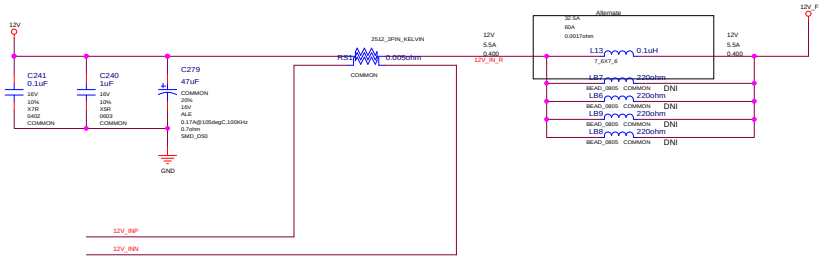
Page33: PS: Inputs, Filtering, and Monitoring



PEX 3V3 INPUT - 10W



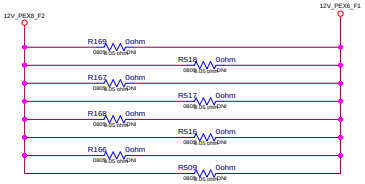
PEX_12V INPUT - 66W

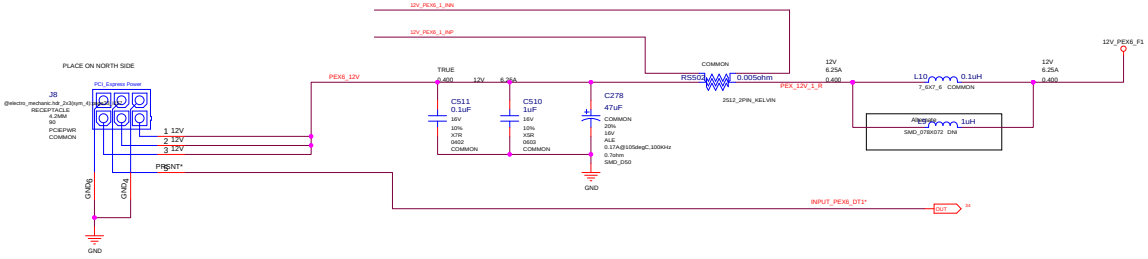


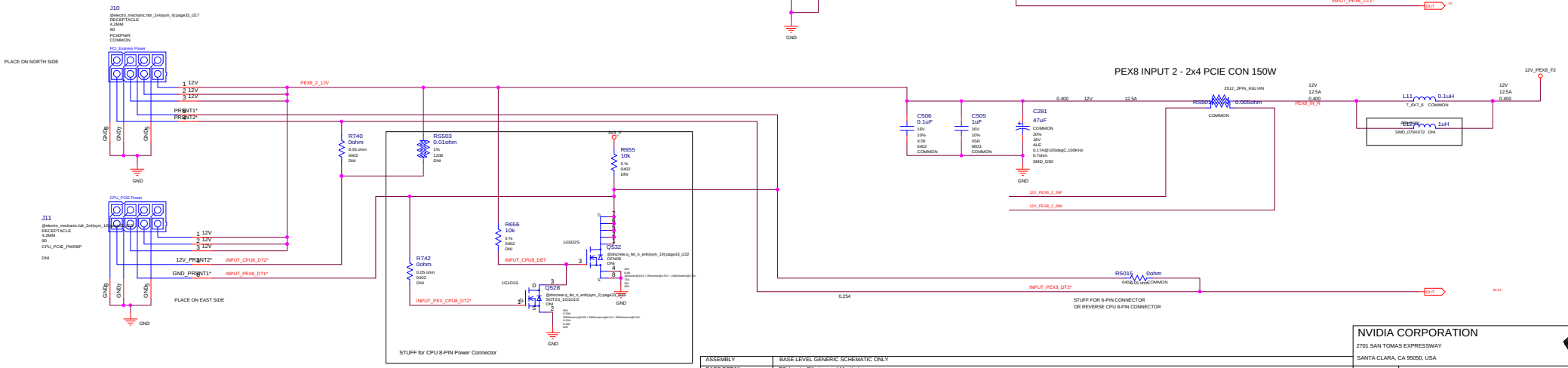
PEX6 INPUT 1 - 2x3 PCIE CON 75W

STUFF ALL EIGHT FOR QUADRO

STUFF BOTH FOR QUADRO
PLACE NEAR U502 (INA3221)







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

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PCB REV	PG401-A02	PAGE	33 OF 37
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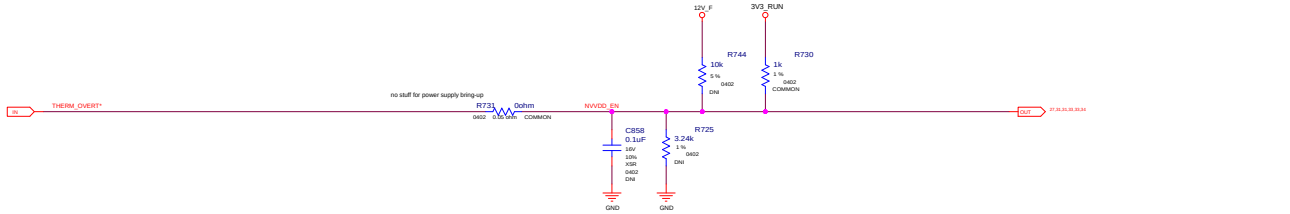
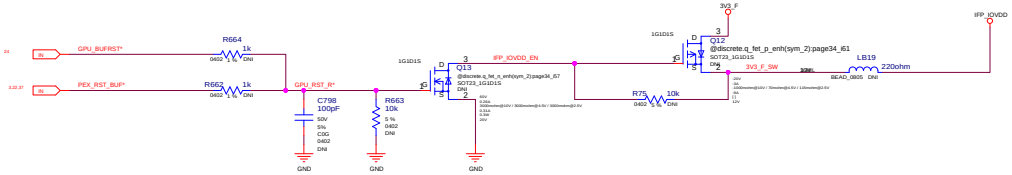
Page34: PS: Shutdown

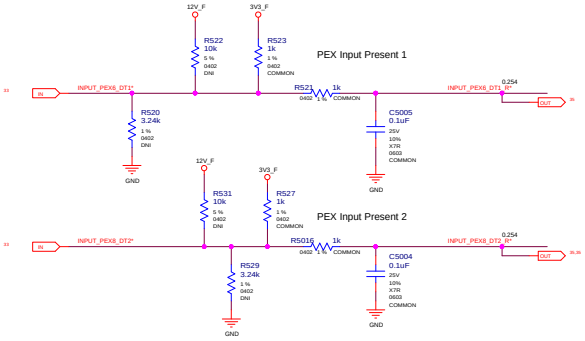
THERM OVERT SHUTDOWN LATCH



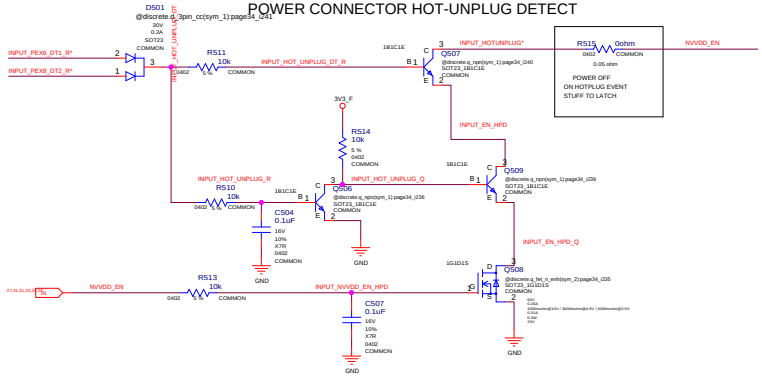
IFP_IOVDD (backdrive prevention)

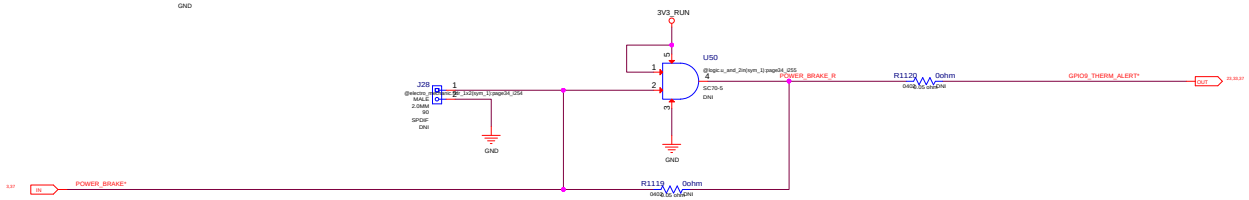


PEX Input - NVVDD Power Sequence



POWER CONNECTOR HOT-UNPLUG DETECT





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Shutdown

NVIDIA CORPORATION
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NV_PN	600-1G401-BASE-QS1		
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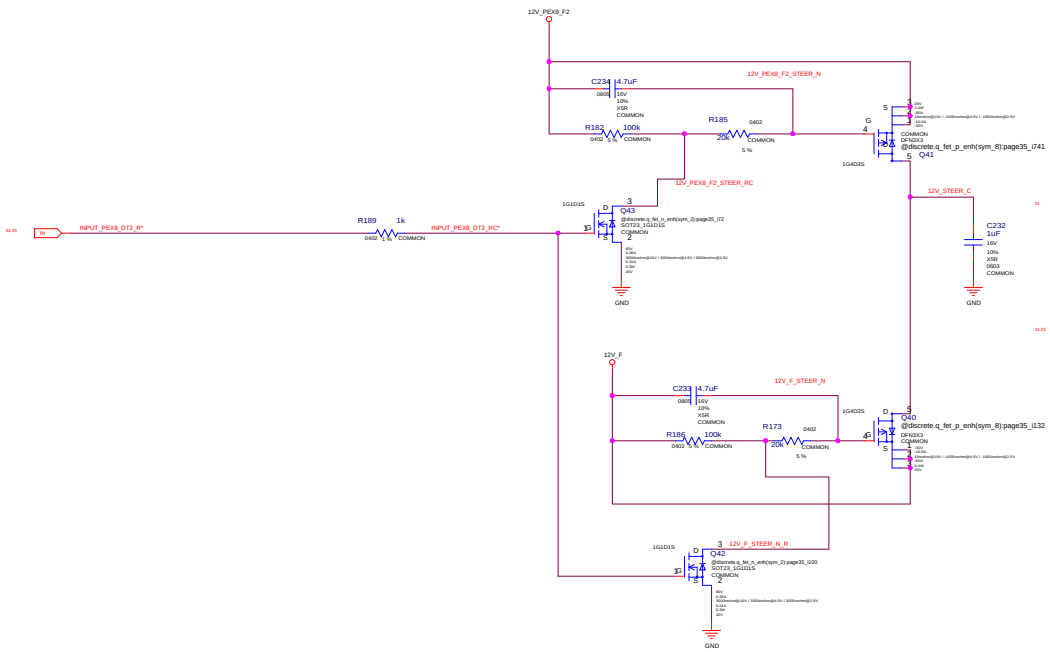
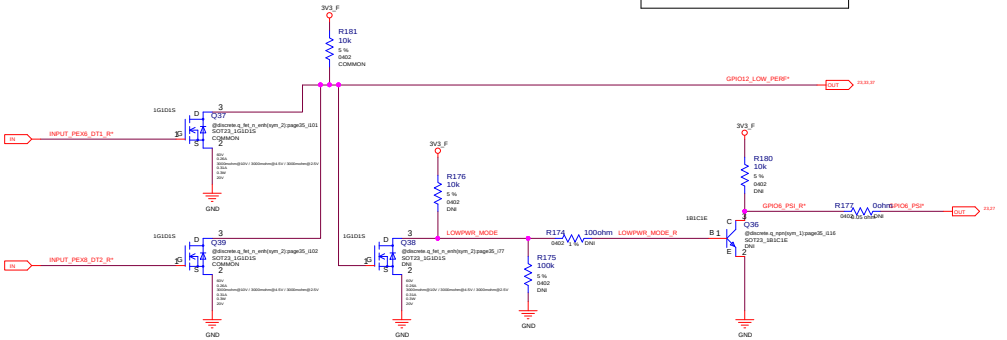
Page35: PS: 12V Current Steering, PSI Control, and LED

PEX Input - 12V Current Steering FETs

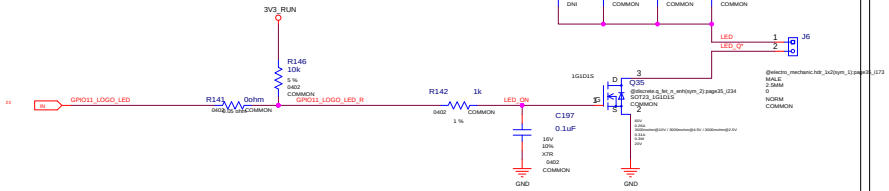


PEX Input - Power Level/PSI* Control



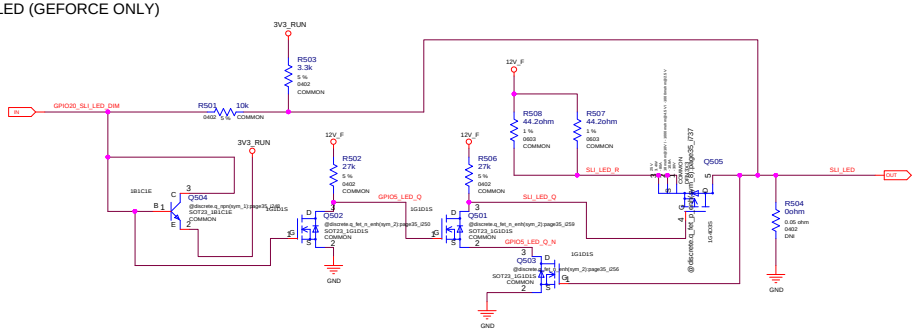
GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

GeForce Logo LED



LED HEADER (C0MM0N)

SLI LED (GEFORCE ONLY)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 12V Current Steering PSI Control and LED

NVIDIA CORPORATION
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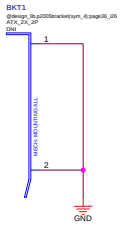
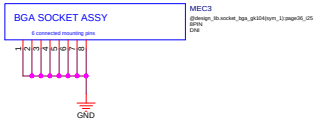
Page36: Mechanical: Bracket/Thermal Solution

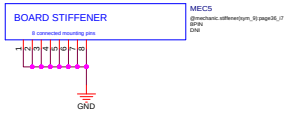
Brackets:



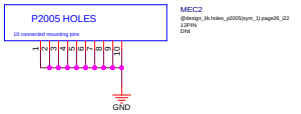
Bracket Screw

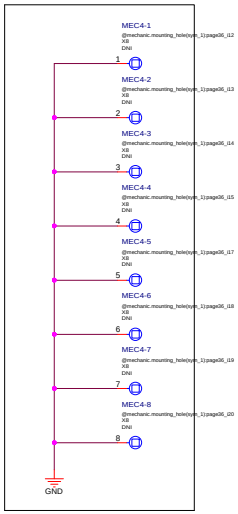


GPU Stiffner



Mechanical Holes Symbol





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MECH: Bracket/Thermal

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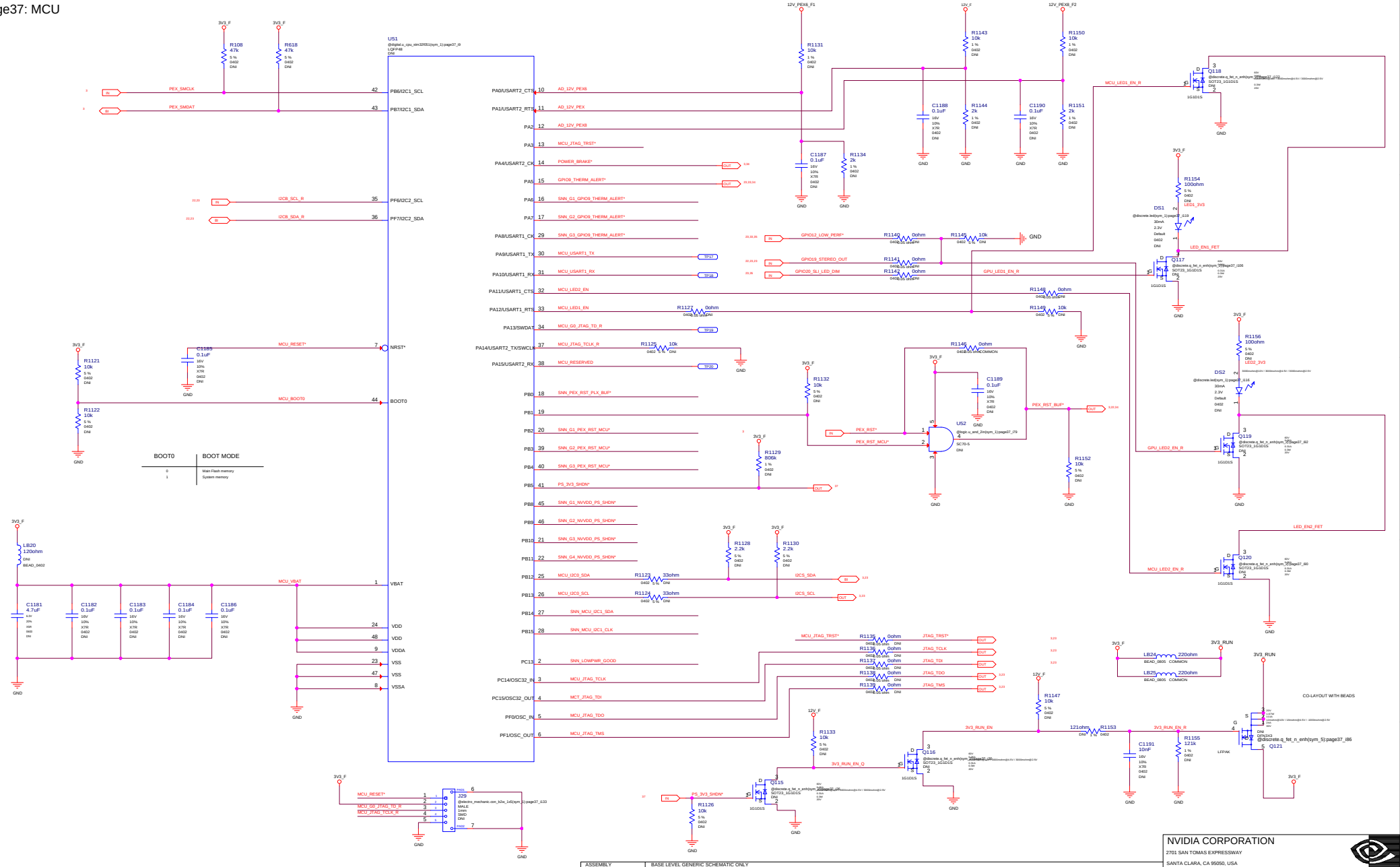
Page37: MCU



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MICROCONTROLLER

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