

PCI-EXPRESS EDGE CONNECTOR

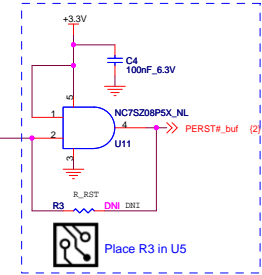
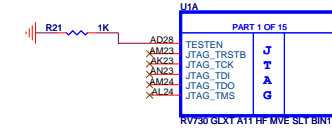
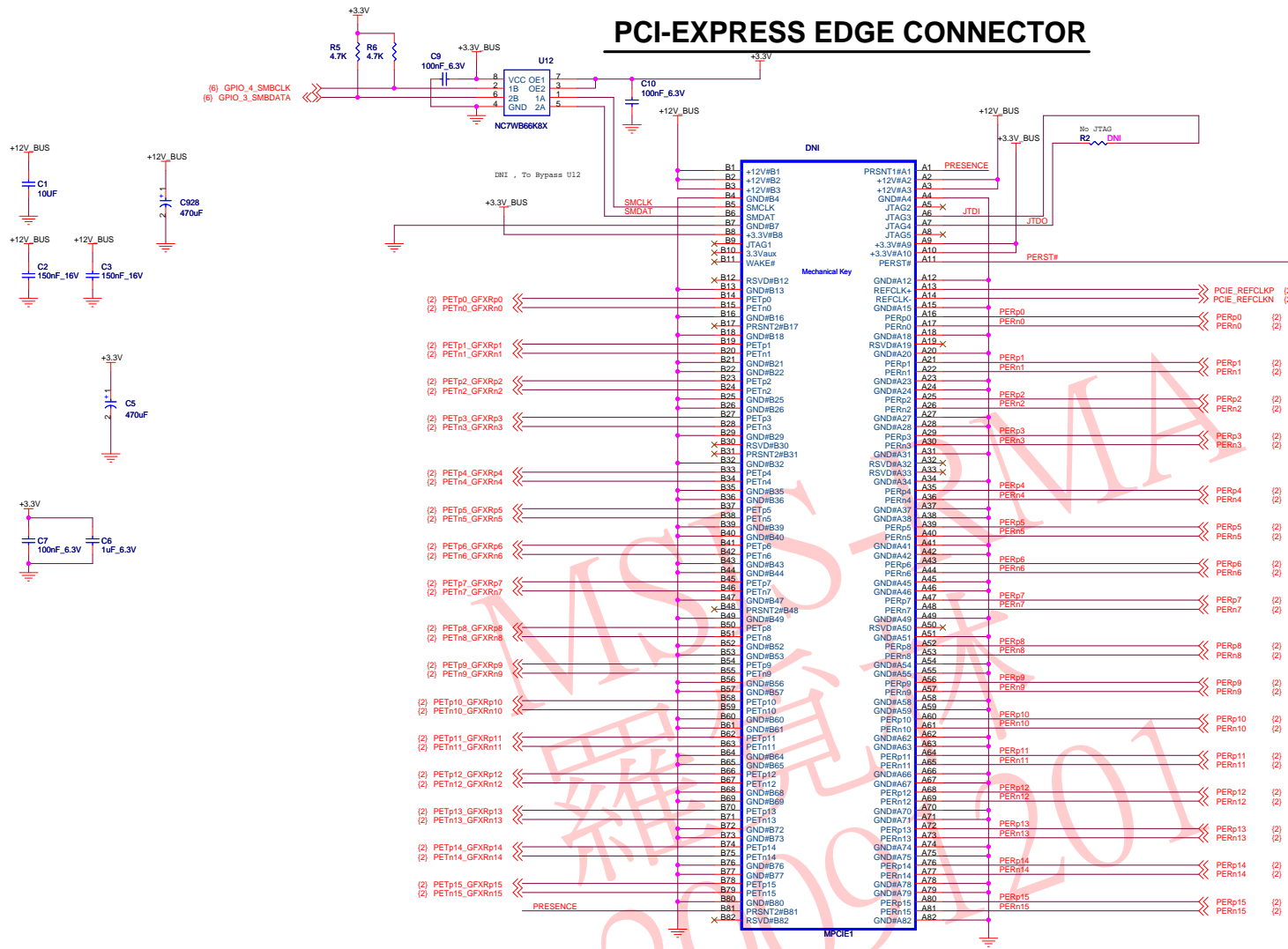


Table 1: Connection for JTAG

Production (No JTAG)	Install R1, R2 & Don't Install TSW1	
Internal Use Only	JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open
	NO JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)

TSW1, R1 & R2 are located on the bottom side of the board close to PCIe connector.

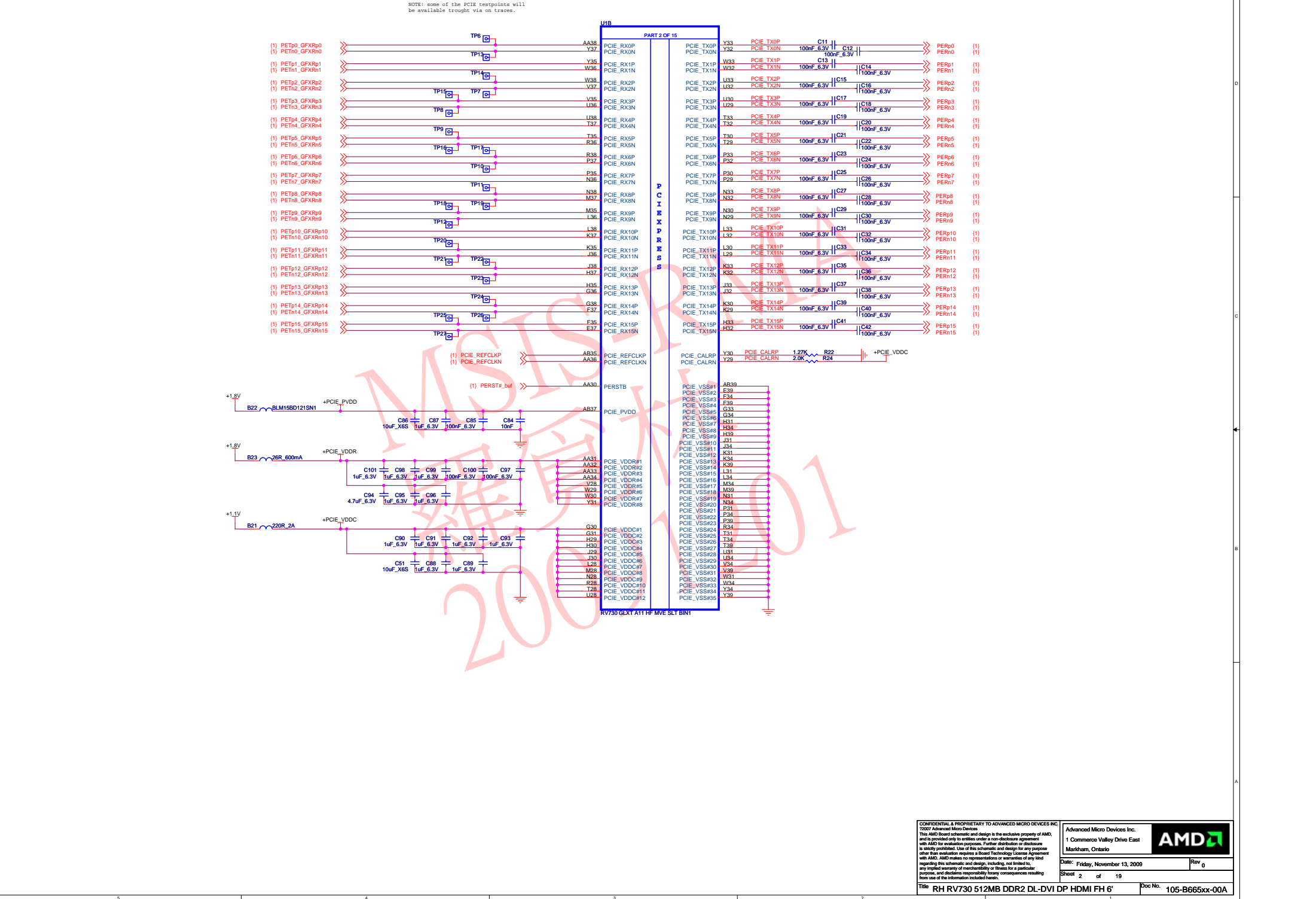
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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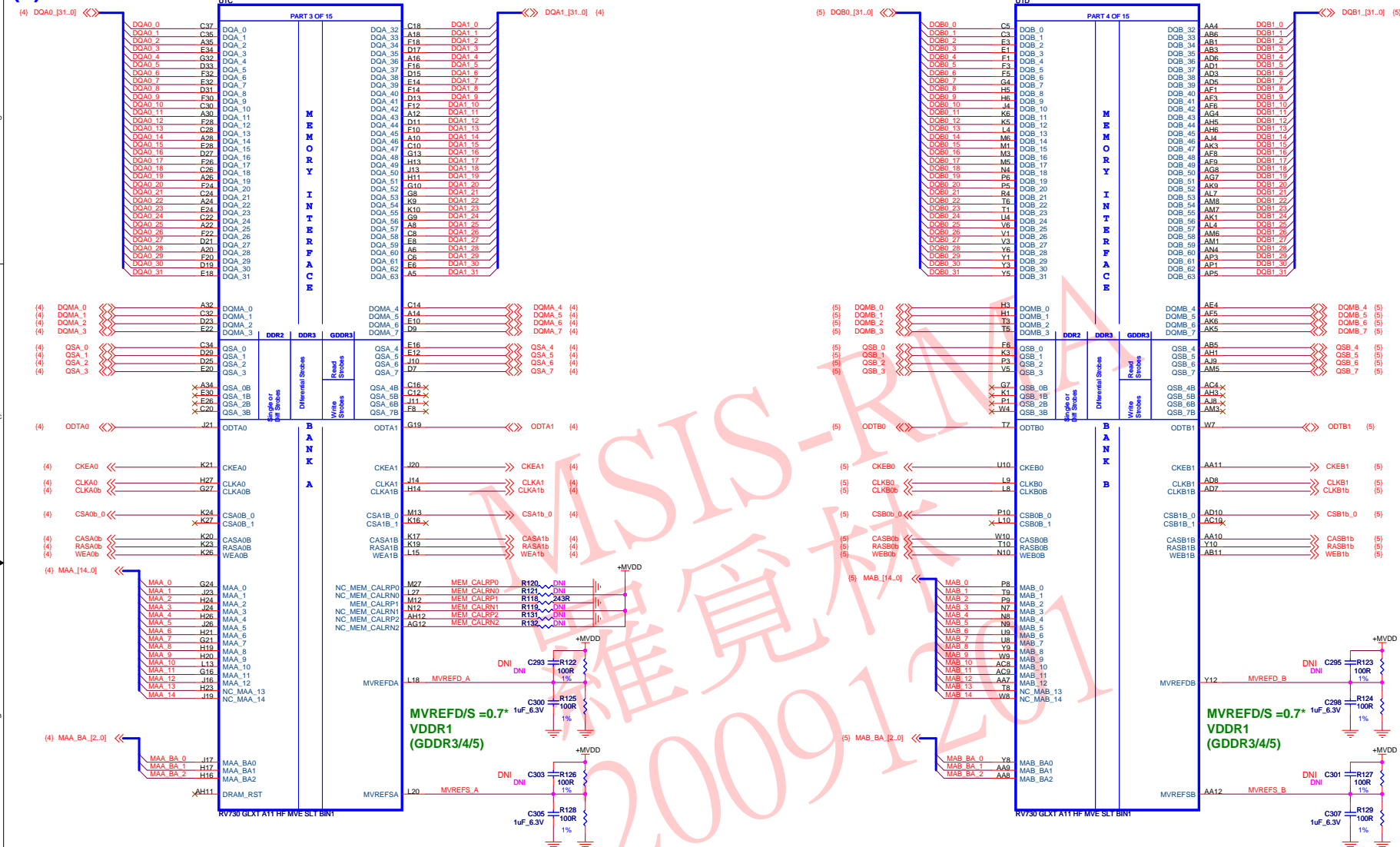
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1 Commerce Valley Drive East
Markham, Ontario
Date: Friday, November 13, 2009
Sheet 1 of 10
Rev 0
Title RH RV730 512MB DDR2 DL-DVI DP HDMI FH 6'

Doc No. 105-B665xx-00A

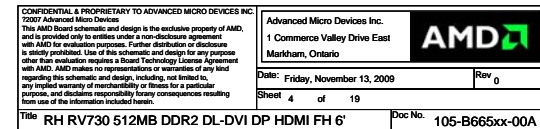
(2) RV730 PCIe Interface



(3) RV730 MEM Interface Ch A&B

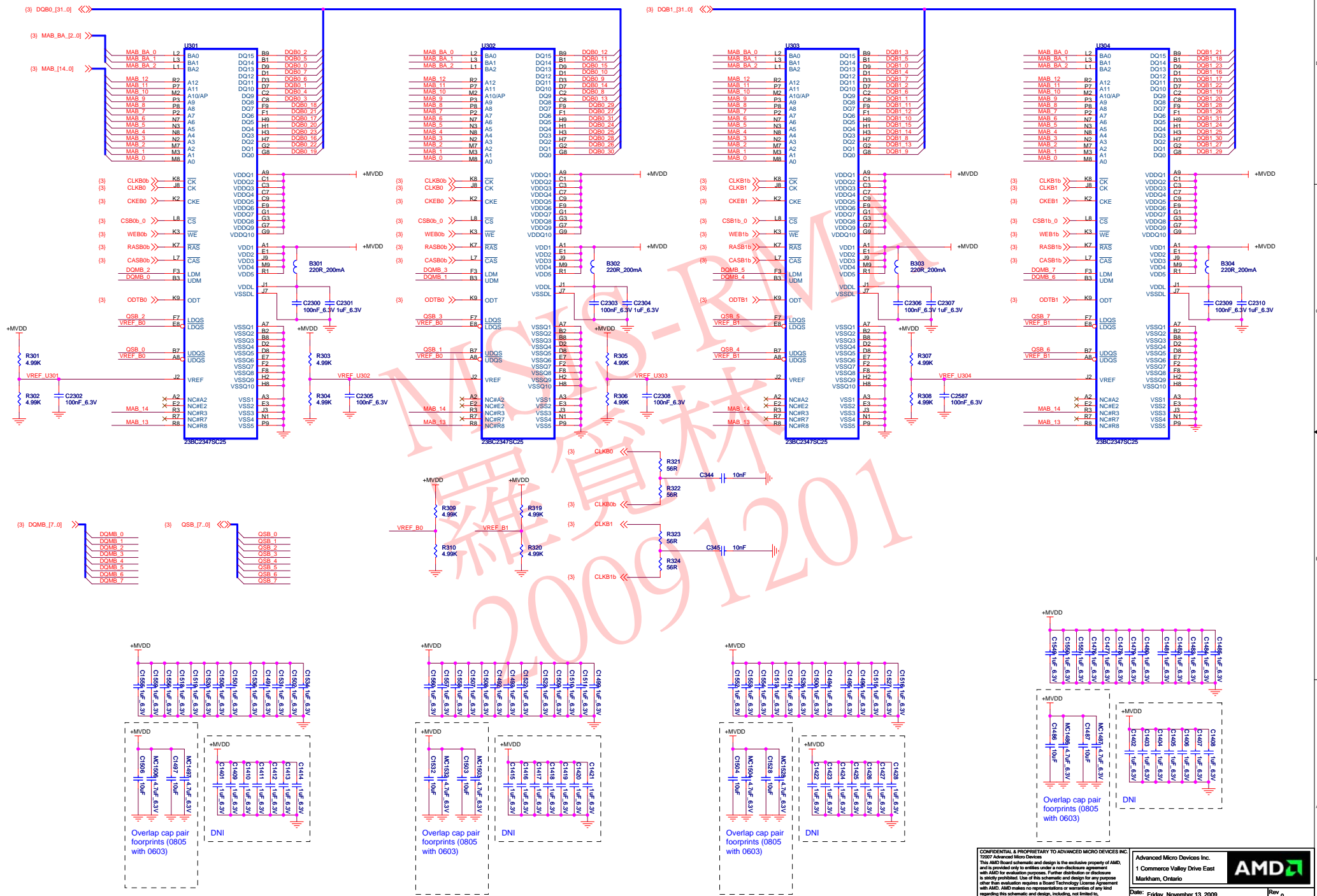


CHANNEL A: 128MB/256MB DDR2

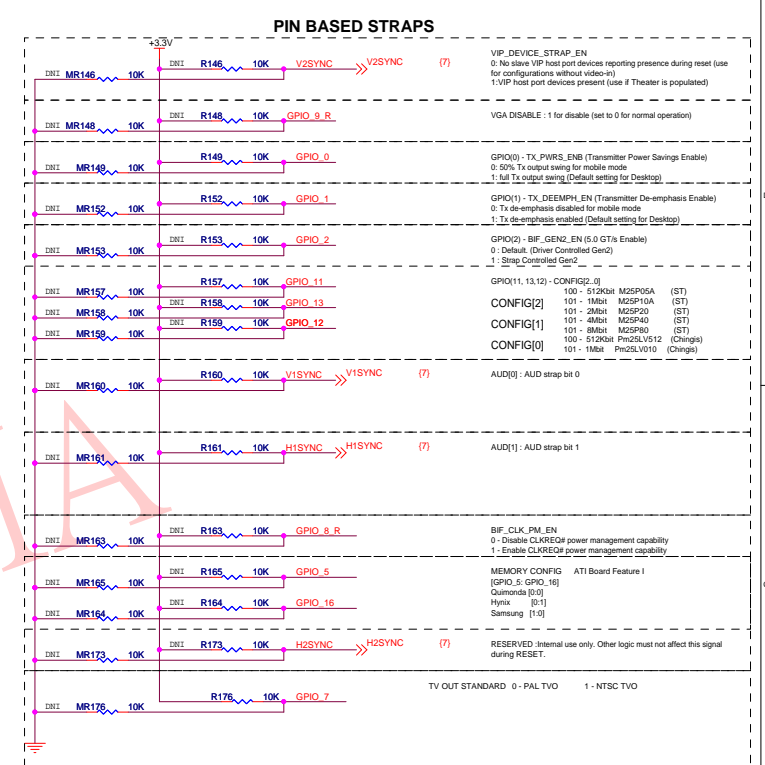
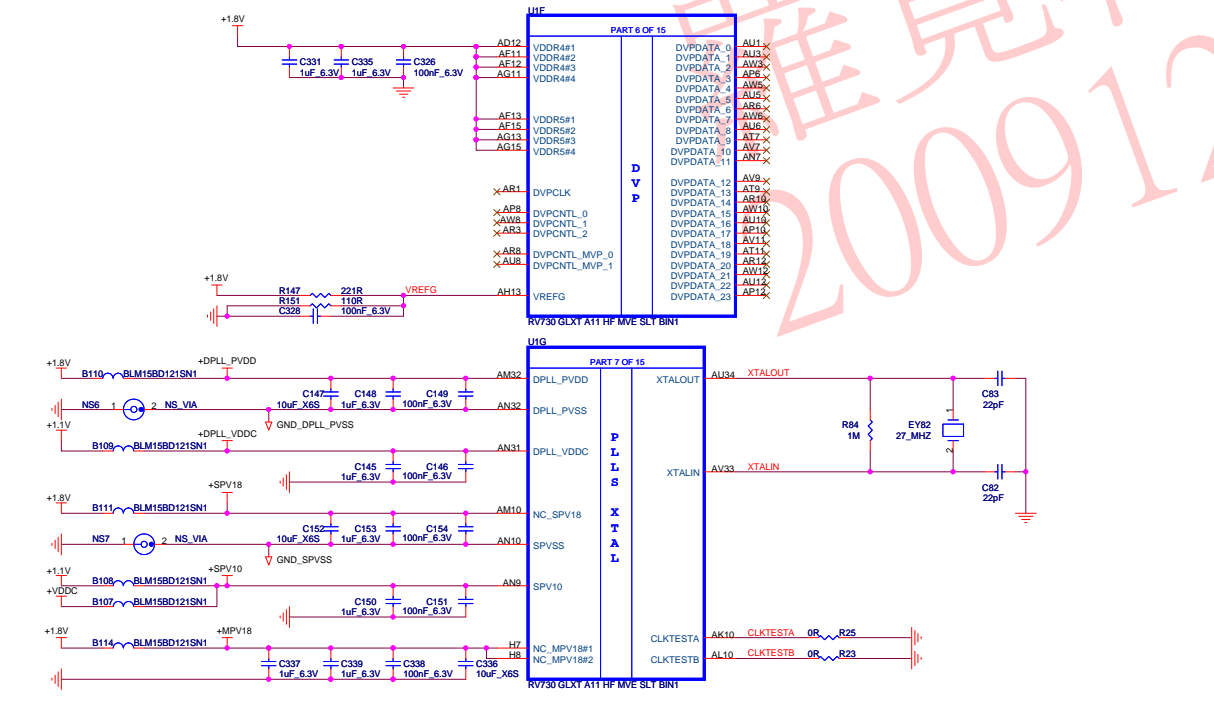
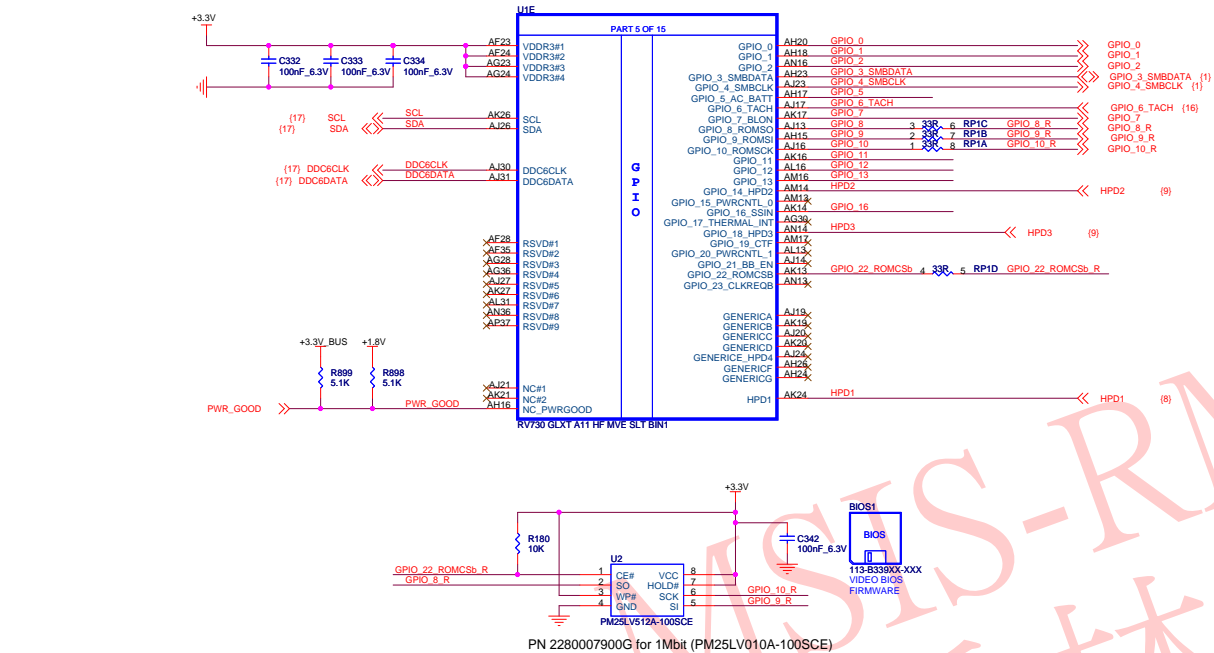


(5) DDR2 Ch B

CHANNEL B: 128MB/256MB DDR2



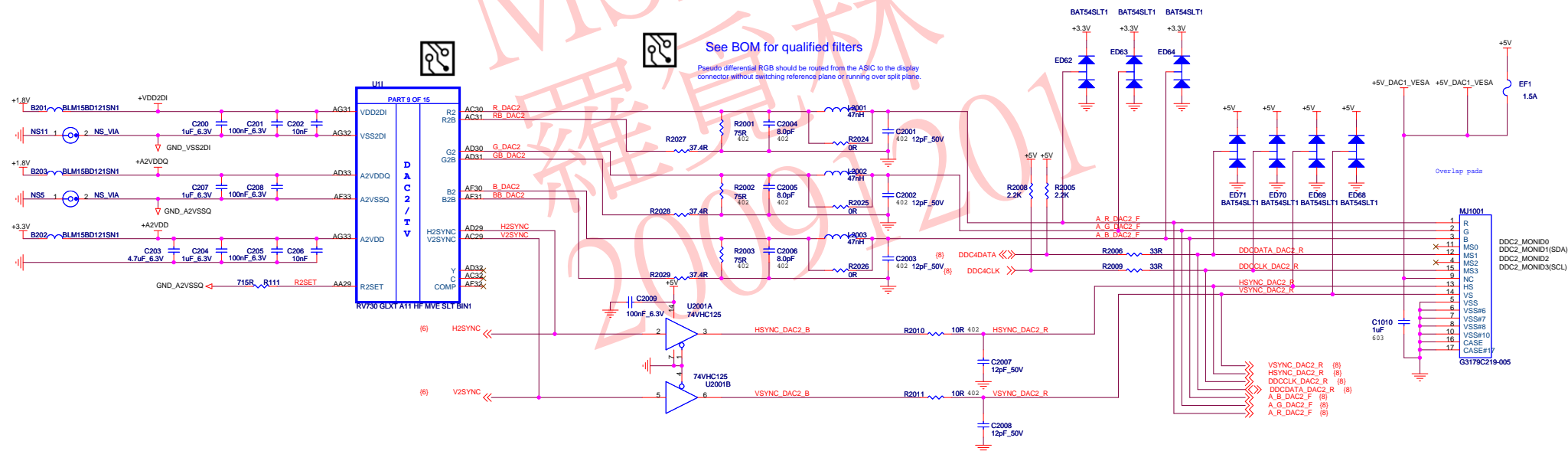
(06) RV730 GPIOs Strap CF XTAL





See BOM for qualified filters

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane



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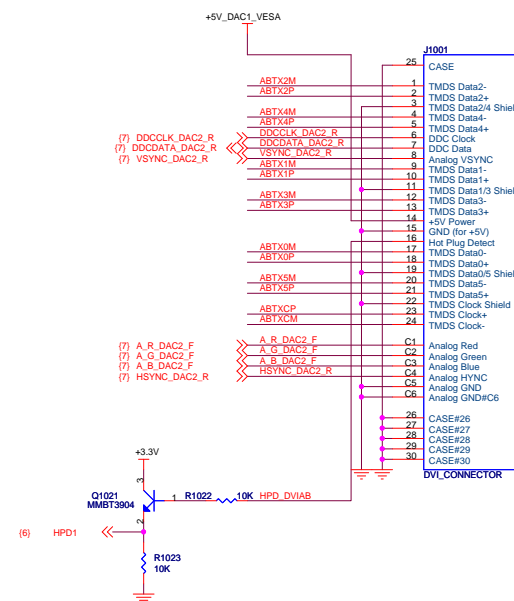
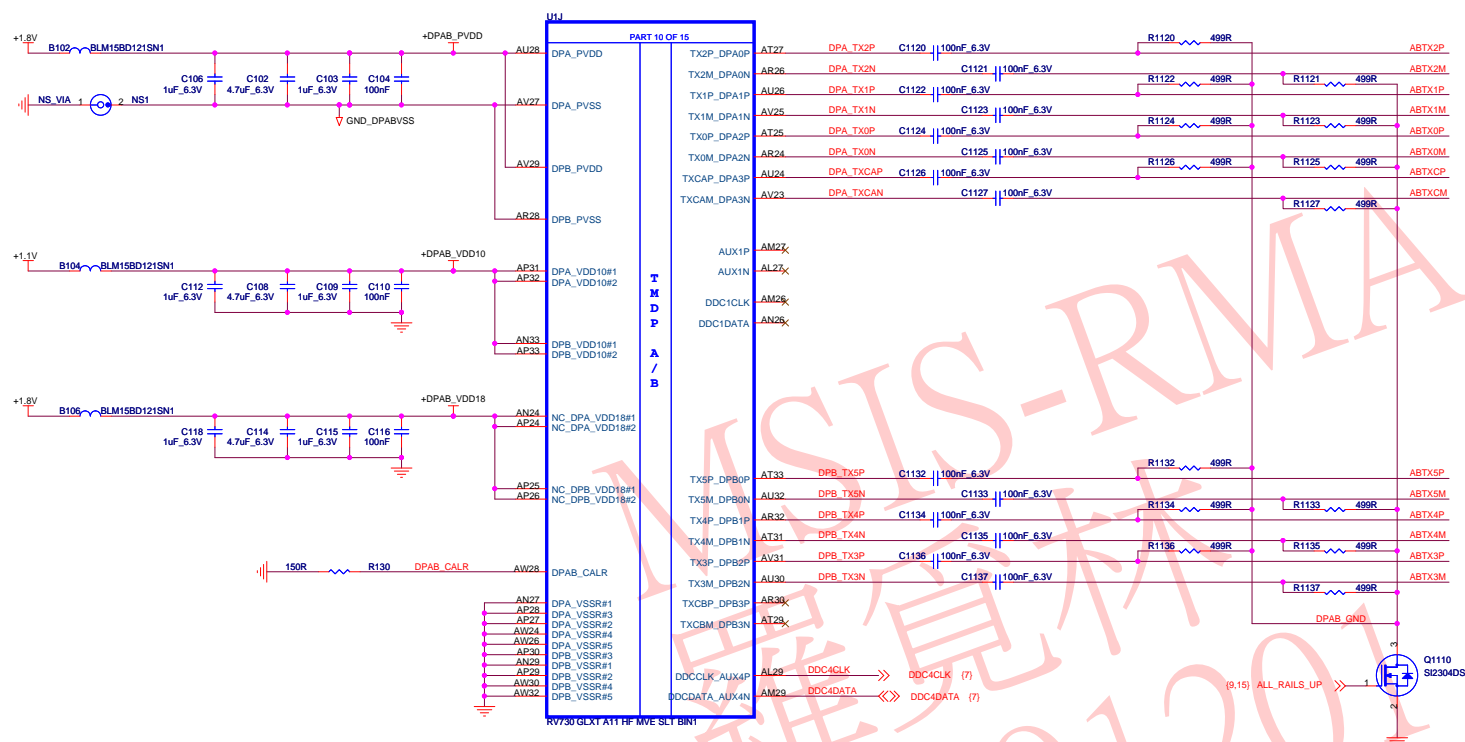
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(08) RV730 TMDS A&B



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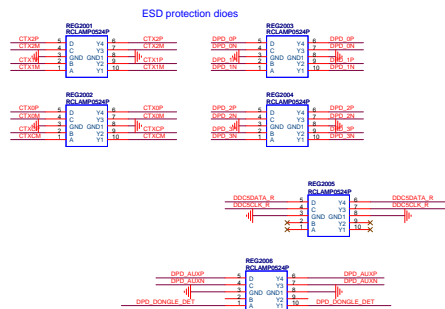
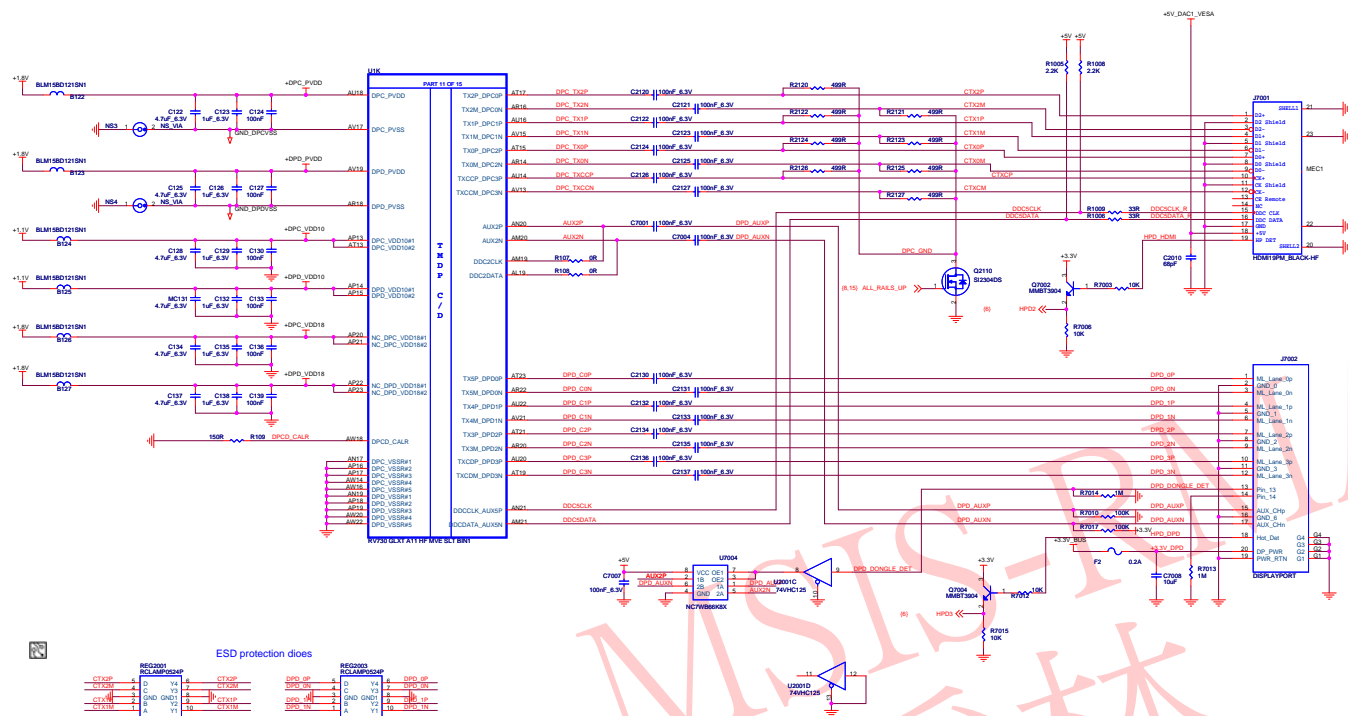
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Rev

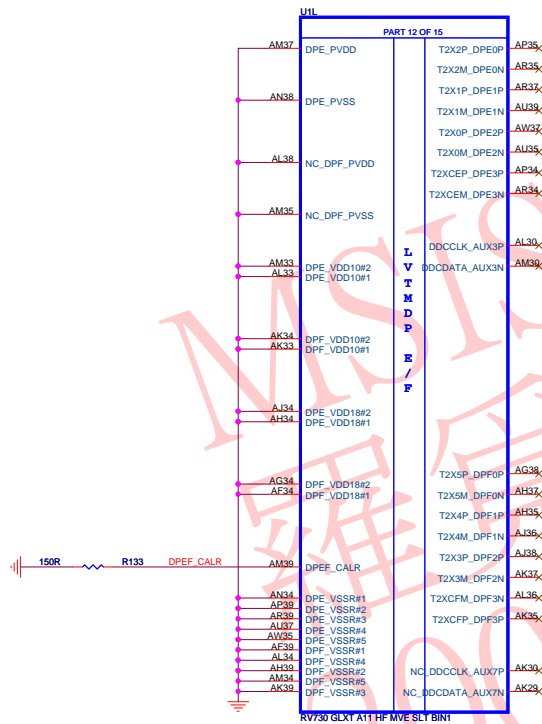
Title	RH RV730 512MB DDR2 DL-DVI DP HDMI FH 6'
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Doc No.	105-B665xy-00A
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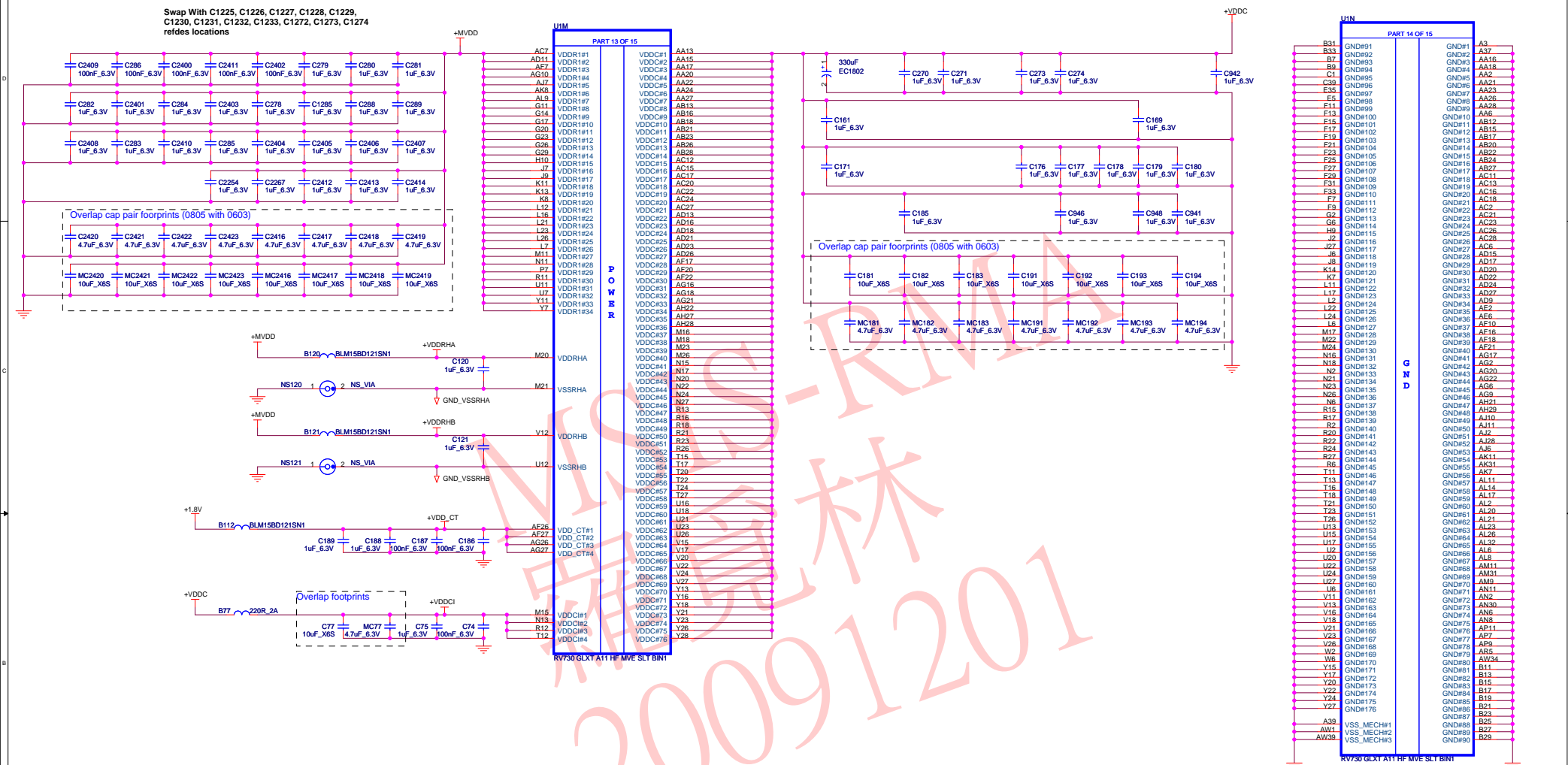
(09) RV730 HDMI and DisplayPort on C&D



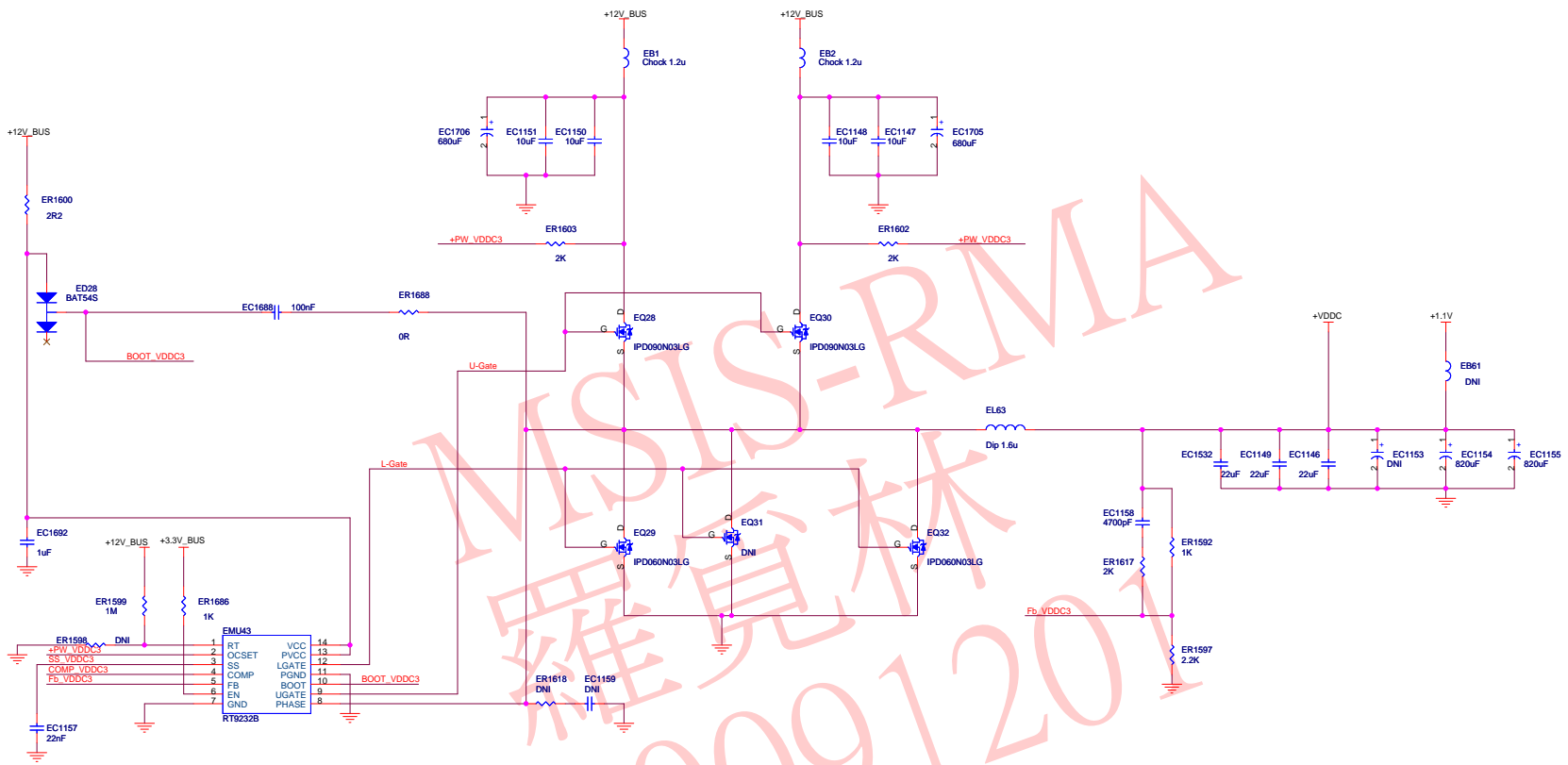
(10) No Connect E&F



(11) RV730 Power & GND

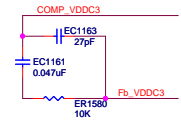


CORE REGULATOR VDDC

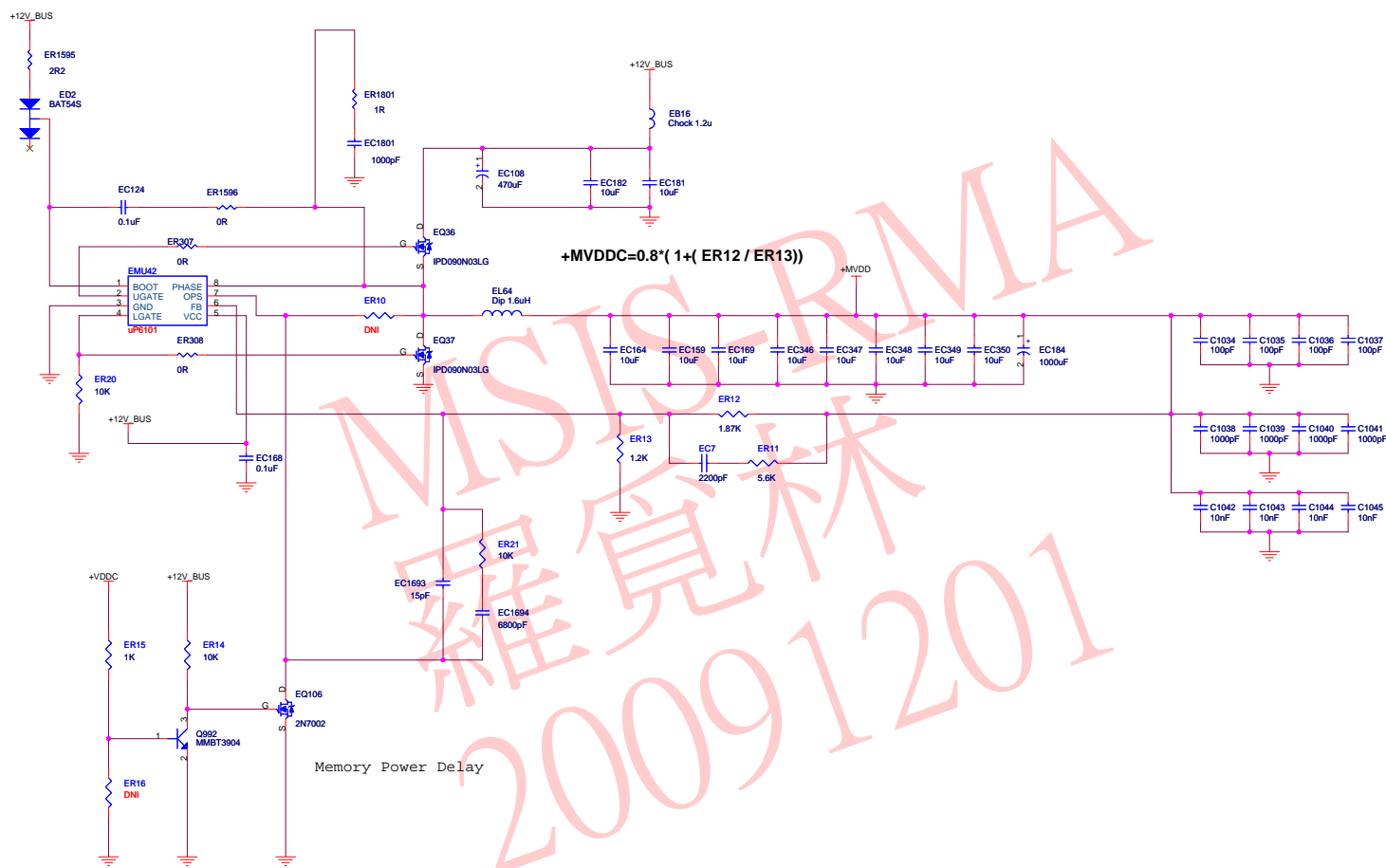


$$+VDDC=0.8*(1+(ER1592/ER1597))$$

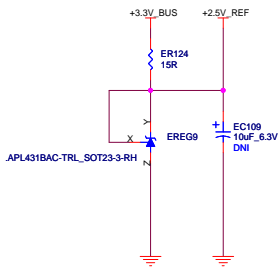
Compensation Circuit



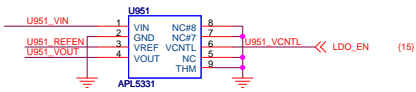
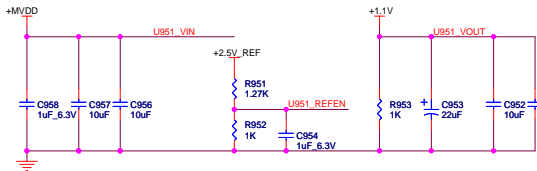
(13) MVDD



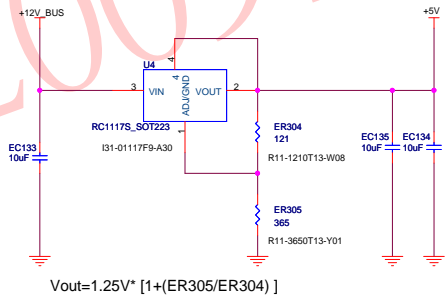
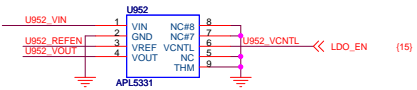
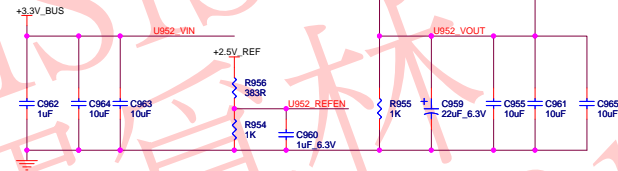
(14) Linear Regulators



Optional regulator for +1.1V
Vout = 1.1V



Optional regulator for +1.8V
Vout = 1.8V



$V_{out} = 1.25V \cdot [1 + (ER305/ER304)]$

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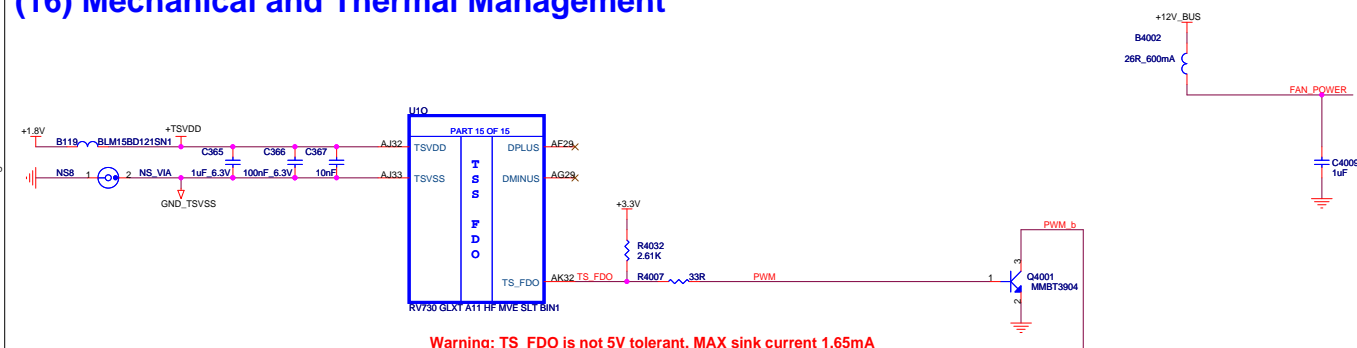
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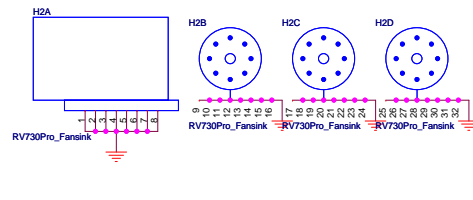
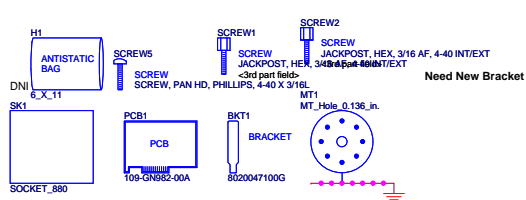
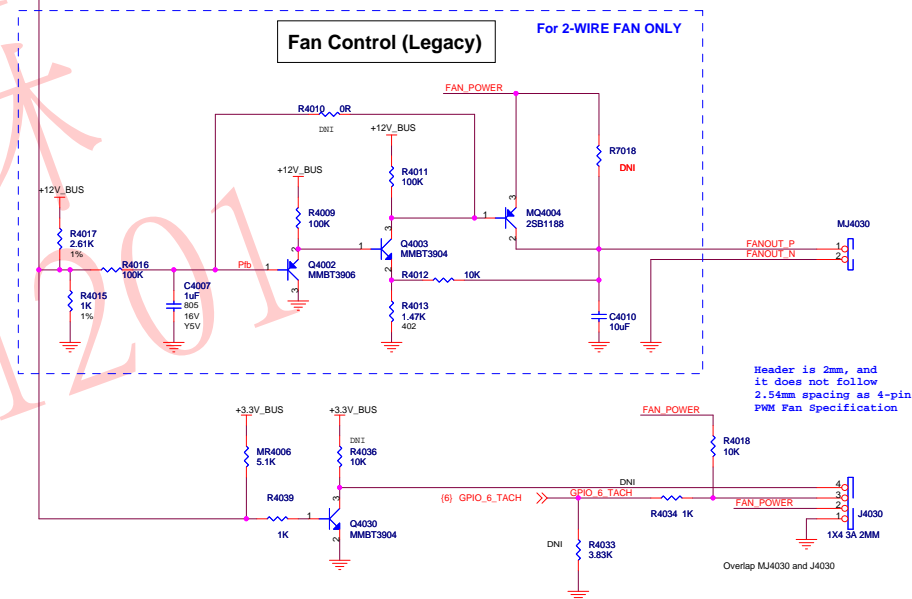
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Title RH RV730 512MB DDR2 DL-DVI DP HDMI FH G'

(16) Mechanical and Thermal Management




Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA



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(17) Debug Circuits



<div>AMD</div>			Title		Schematic No.		Date:		
			RH RV730 512MB DDR2 DL-DVI DP HDMI FH 6'		105-B665xx-00A		Friday, November 13, 2009		
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.					Rev	0
			REVISION DESCRIPTION						
Sch Rev	PCB Rev	Date							
0	00A	08/04/01	Initial design for RV730 GDDR3						
			<div>MSIS-RMA 羅覓林 20091201</div>						