45P211-NV45 Board

NV 45 P211_A03 - Front side 8pcs x (8Mx32MB) DDR3 = 256MB Total, PCI-Express X16
Internal TMDS (dual link) and External TMDS (dual link), Internal SVideo Out,
Video Capture (7114), optional Framelock/SDI connector, 5-pin PVA

Table of Contents:

Page1: Table of Contents
Page2: PCI EXPRESS INTERFACE
Page3: GPU: FB_A & FB_B Partitions
Page4: Memory: FB_A
Page5: Memory: FB_B
Page6: GPU: FB_C & FB_D Partitions
Page7: Memory: FB_C
Page8: Memory: FB_D
Page9: Memory Signal Constraints, GPU FB-CAL
Page10: FBIO refclock generator
Page11: BIOS, Strappings and Misc
Page12: DVO/VIP Interface, MIO connector
Page13: DACA Filter and VGA connector, SOUTH
Page14: DACB Filter, RGB SWITCH and VGA connector
Page15: DUAL LINK Internal TMDS, DVI Connectors
Page16: DUAL LINK TMDS External with Silicon Image
Page17: Video Capture (SAA7114)
Page18: Video In/Out Connector External/Internal (MiniDin)
Page19: FBVDDQ, FBVTT DECOUP
Page20: 3V3, NVVDD DECOUP
Page21: GPIOs, NVVDD VID, TEMP and FAN Control
Page22: POWER SUPPLY: FBVDD, FBVDDQ, FBVTT
Page23: POWER SUPPLY: NVVDD, PCI-EX EXTERNAL POWER
Page24: POWER SUPPLY: 5V AND PEX_VDD

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10211-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU10002_DVI_NORTH_SINGLE_VGA_SOUTH	600-10211-0002-300	SKU 1-0002: NV45-P211 A03, 256MB, 600MHZ GDDR3, DVI-NORTH, VGA-SOUTH, SVIDEO 4-PIN, ULTRA
2	SKU50000_DVI_NORTH_DUAL_DVI_SOUTH_DUAL	600-50211-0000-300	SKU 5-0000: NV45-P211 A03, 256MB, 600MHZ GDDR3, DVI-NORTH (DUAL-LINK), DVI-SOUTH (DUAL-LINK), STEREO, WRK-ST
3	SKU50001_DVI_NORTH_SINGLE_DVI_SOUTH_DUAL_DELL	600-50211-0001-300	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
4	SKU10003_DVI_NORTH_SINGLE_DVI_SOUTH_SINGLE	600-10211-0003-300	SKU 1-0003: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SINGLE-LINK), DVI-SOUTH (SINLE-LINK), SVIDEO, ULTRA
5	SKU10004_DVI_NORTH_SINGLE_DVI_SOUTH_SINGLE	600-10211-0004-300	SKU 1-0004: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SINGLE-LINK), DVI-SOUTH (SINGLE-LINK), SVIDEO, GT
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	Table of Contents

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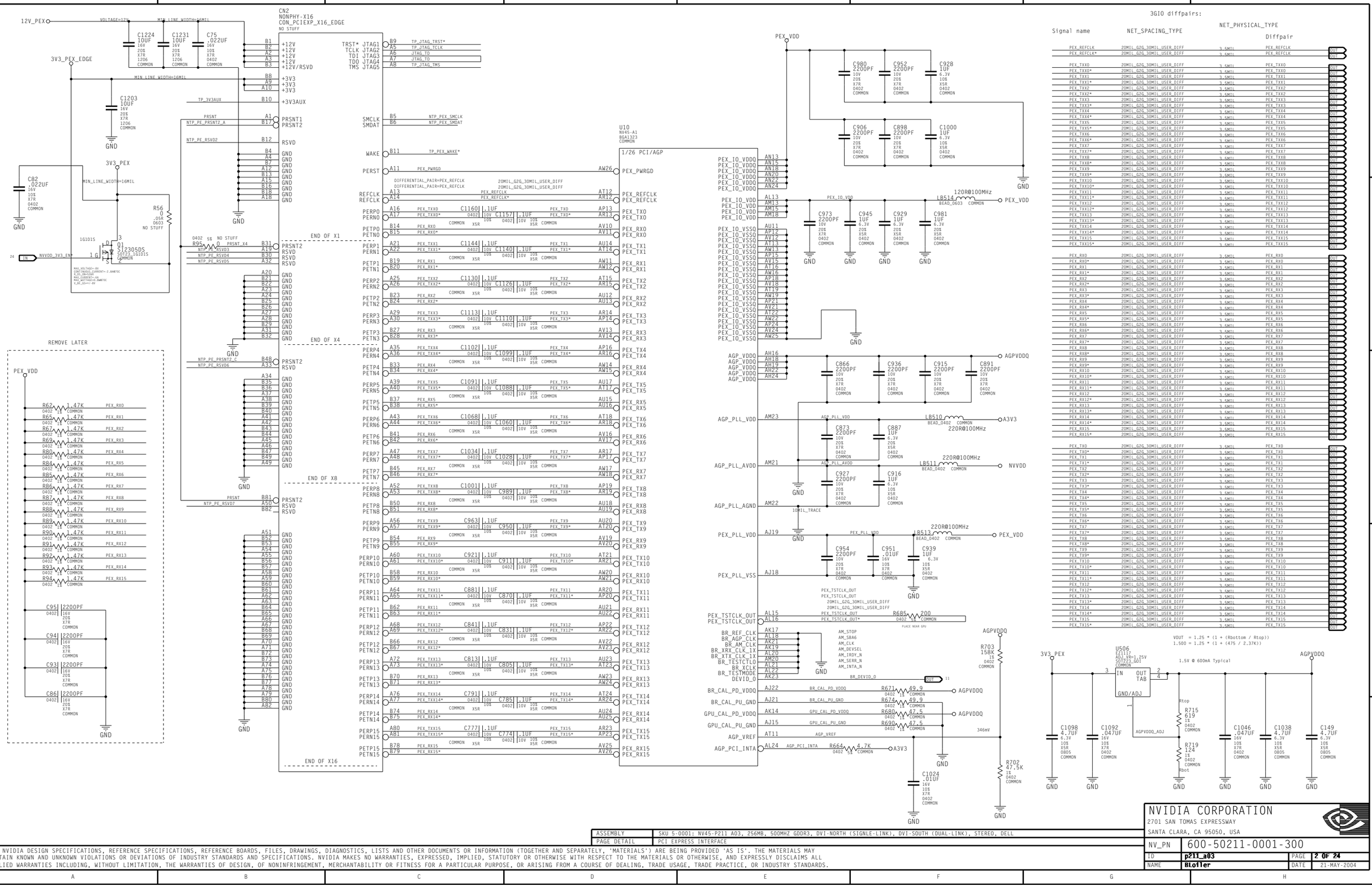
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	1 OF 24
NAME	BLoller	DATE	21-MAY-2004



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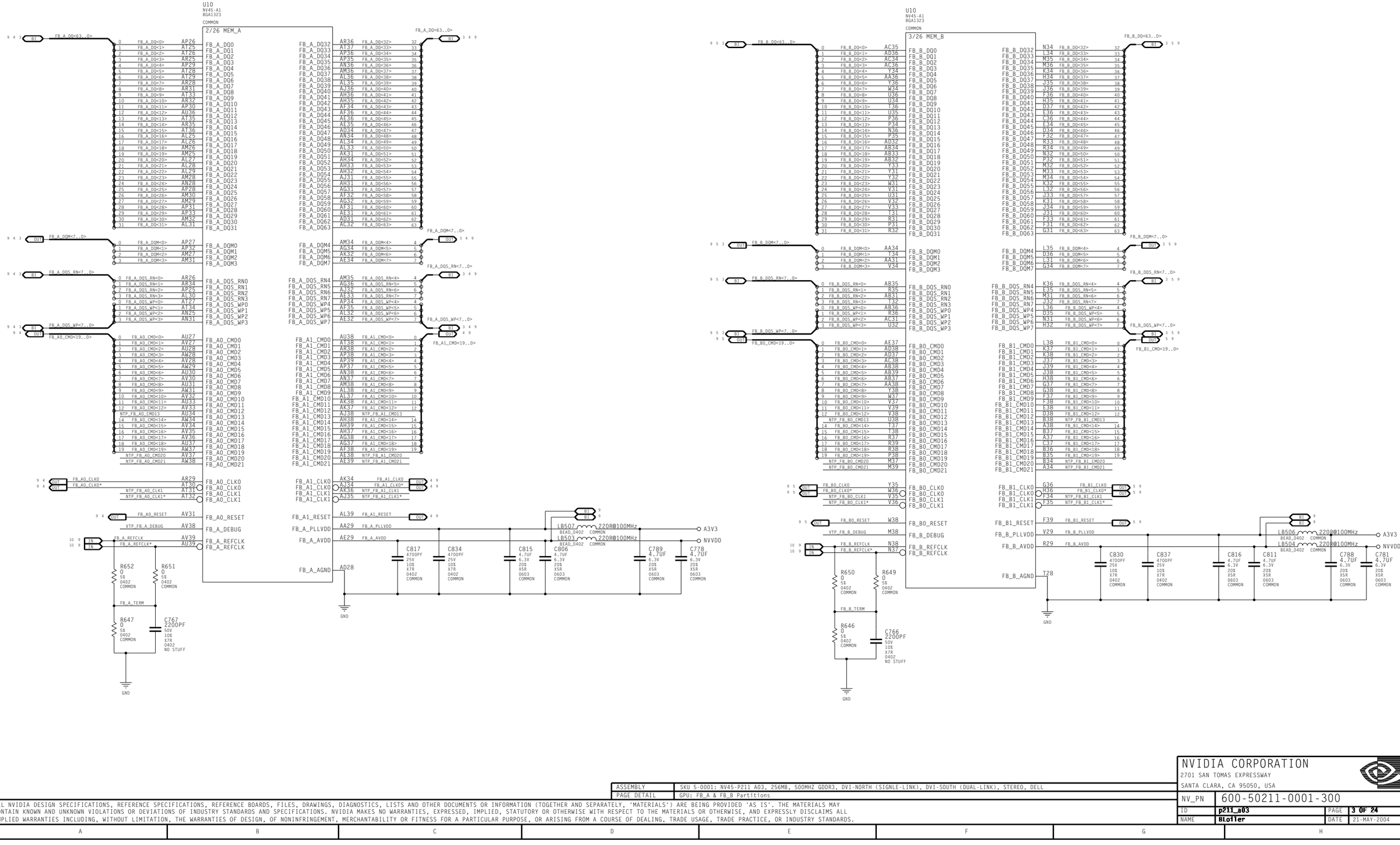

ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	GPU: FB_A & FB_B Partitions

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NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	3 OF 24
NAME	BLoller	DATE	21-MAY-2004

ASSY=FBIO_A

termination not required for DDR2

	144BGA
	TOP
	CS0
CMD0	A4
CMD1	A7
CMD2	A5
CMD3	A6
CMD4	A9
CMD5	A8
CMD6	CS0
CMD7	BA1
CMD8	WE*
CMD9	RAS*
CMD10	CKE
CMD11	CAS*
CMD12	BA0
CMD13	CS1
CMD14	A11
CMD15	A10
CMD16	A1
CMD17	A2
CMD18	A0
CMD19	A3
CMD20	<und>
CMD21	<und>

New CAPs.

Replicate to other pages!!

MEMORY BGA

placed TOP

MEMORY BGA

placed TOP

DDR3 = 0.75 * VDDQ
DDR2 = 0.5 * VDDQ

ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	Memory: FB_A

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NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	4 OF 24
NAME	Blotter	DATE	21-MAY-2004

ASSY=FBIO_B

	144BGA
	TOP
	CSO
CMD0	A4
CMD1	A7
CMD2	A5
CMD3	A6
CMD4	A9
CMD5	A8
CMD6	CS0
CMD7	BA1
CMD8	WE*
CMD9	RAS*
CMD10	CKE
CMD11	CAS*
CMD12	BA0
CMD13	CS1
CMD14	A11
CMD15	A10
CMD16	A1
CMD17	A2
CMD18	A0
CMD19	A3
CMD20	<und>
CMD21	<und>

termination not required for DDR2

New CAPs.

Replicate to other pages!!

MEMORY BGA

placed TOP

MEMORY BGA

placed TOP

H4 & H11 NC FOR DDR2

H4 & H11 NC FOR DDR2

ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	Memory: FB_B

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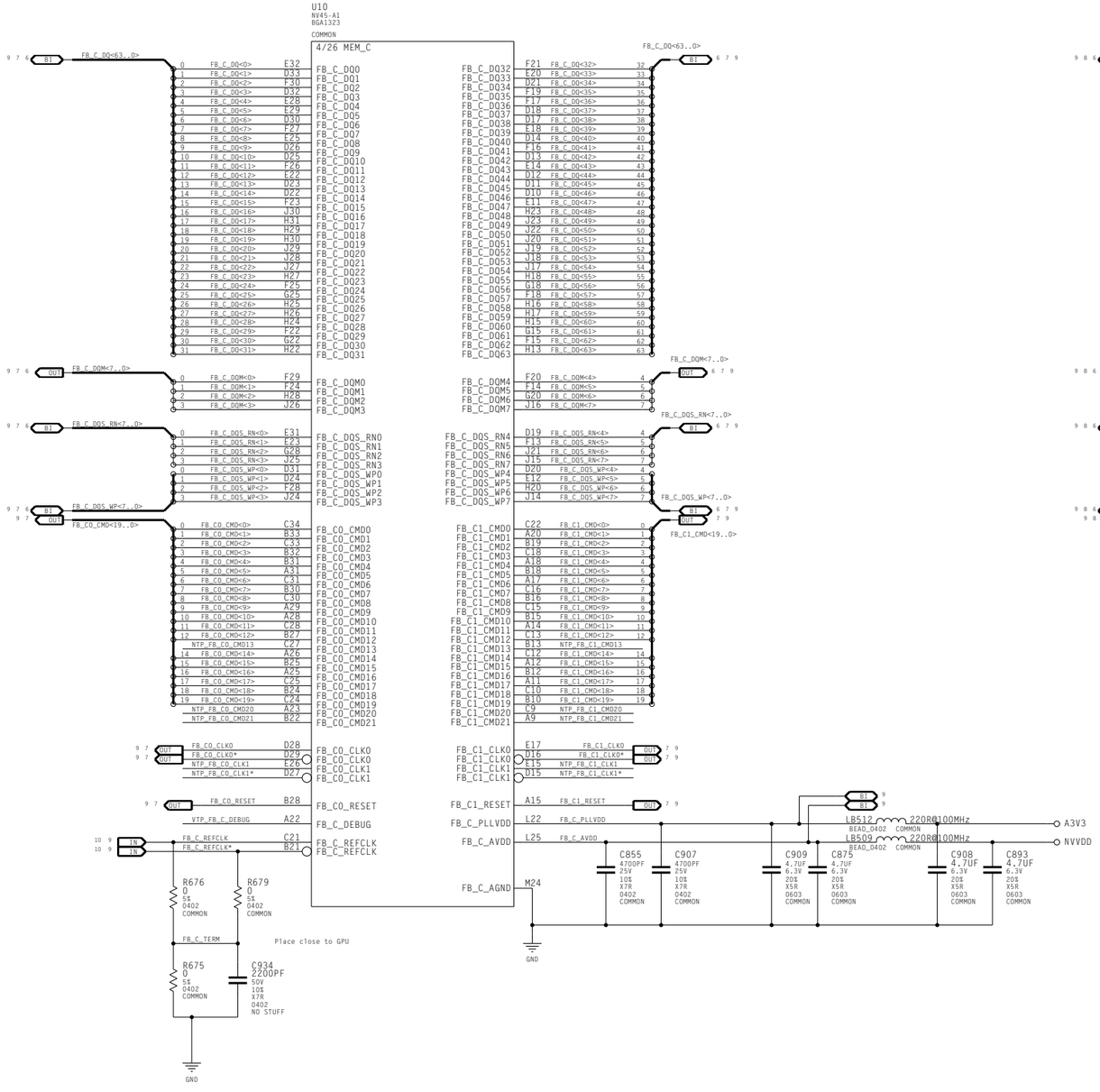
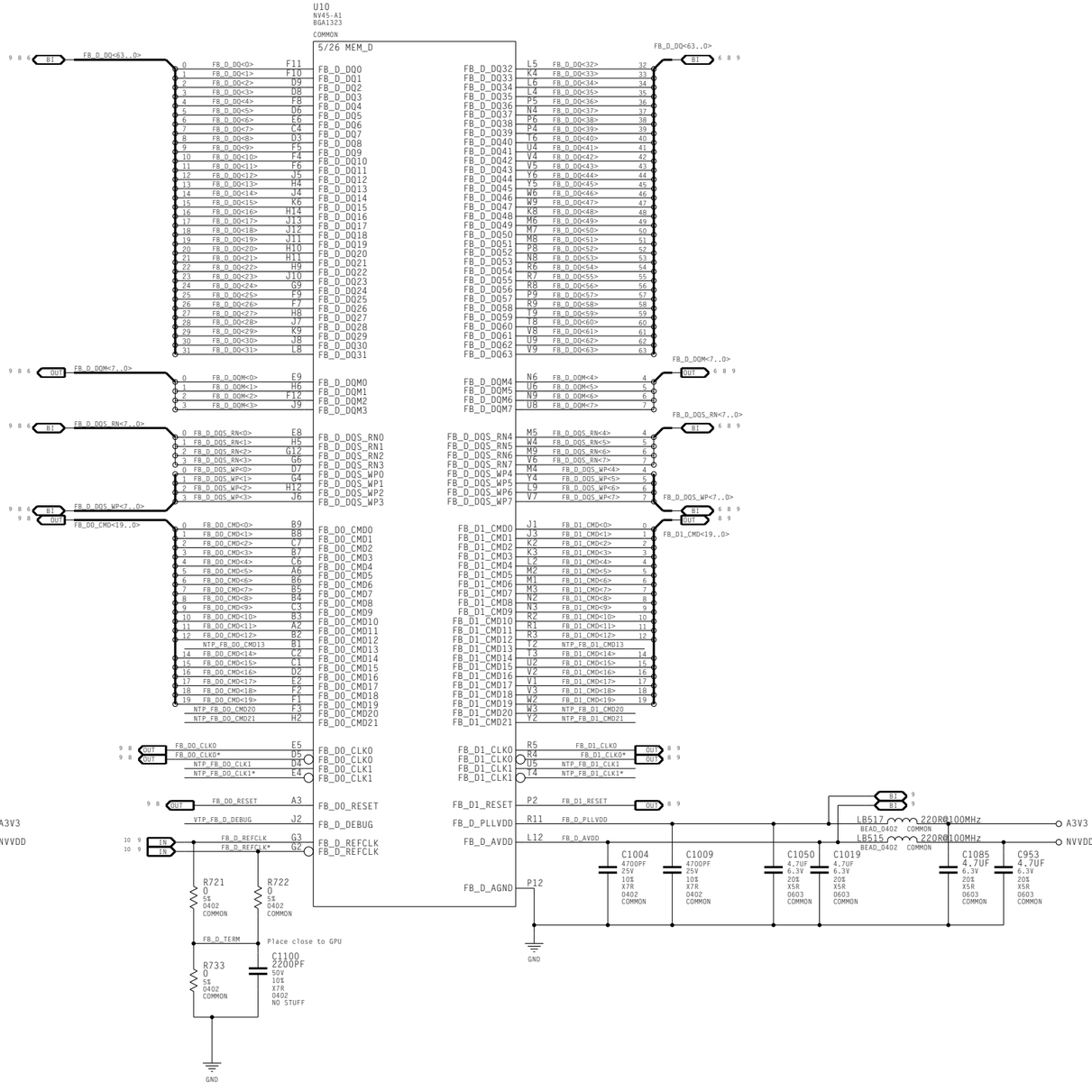
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	5 OF 24
NAME	Blotter	DATE	21-MAY-2004





ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	GPU: FB_C & FB_D Partitions

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NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	6 OF 24
NAME	Blotter	DATE	21-MAY-2004

ASSY=FBIO_C

	144BGA
	TOP
	CS0
CMD0	A4
CMD1	A7
CMD2	A5
CMD3	A6
CMD4	A9
CMD5	A8
CMD6	CS0
CMD7	BA1
CMD8	WE*
CMD9	RAS*
CMD10	CKE
CMD11	CAS*
CMD12	BA0
CMD13	CS1
CMD14	A11
CMD15	A10
CMD16	A1
CMD17	A2
CMD18	A0
CMD19	A3
CMD20	<und>
CMD21	<und>

termination not required for DDR2

H4 & H11 NC FOR DDR2

MEMORY BGA
placed TOP

MEMORY BGA
placed TOP

ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	Memory: FB_C

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NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	7 OF 24
NAME	Blotter	DATE	21-MAY-2004

ASSY=FBIO_D

termination not required for DDR2

	144BGA
	TOP
	CS0
CMD0	A4
CMD1	A7
CMD2	A5
CMD3	A6
CMD4	A9
CMD5	A8
CMD6	CS0
CMD7	BA1
CMD8	WE*
CMD9	RAS*
CMD10	CKE
CMD11	CAS*
CMD12	BA0
CMD13	CS1
CMD14	A11
CMD15	A10
CMD16	A1
CMD17	A2
CMD18	A0
CMD19	A3
CMD20	<und>
CMD21	<und>

MEMORY BGA
placed TOP

MEMORY BGA
placed TOP

H4 & H11 NC FOR DDR2

ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	Memory: FB_D

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NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	8 OF 24
NAME	Bloiler	DATE	21-MAY-2004

Memory FBA FBB

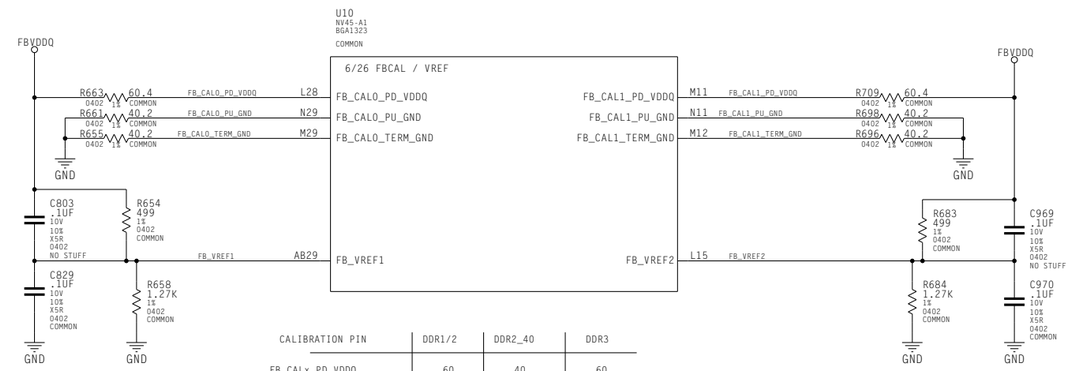
NET Name	Diffpair	Spacing	MIN_LINE_WIDTH	
FB_A0_CLK0	FBA0CLK0	80_OHM_DIFF	5MIL	
FB_A0_CLK0*	FBA0CLK0	80_OHM_DIFF	5MIL	
FB_A1_CLK0	FBA1CLK0	80_OHM_DIFF	5MIL	
FB_A1_CLK0*	FBA1CLK0	80_OHM_DIFF	5MIL	
FB_B0_CLK0	FBB0CLK0	80_OHM_DIFF	5MIL	
FB_B0_CLK0*	FBB0CLK0	80_OHM_DIFF	5MIL	
FB_B1_CLK0	FBB1CLK0	80_OHM_DIFF	5MIL	
FB_B1_CLK0*	FBB1CLK0	80_OHM_DIFF	5MIL	
FB_A_REFCLK	FBAREFCLK	20MIL	3.5MIL	100 ohm diff
FB_A_REFCLK*	FBAREFCLK	20MIL	3.5MIL	
FB_B_REFCLK	FBBREFCLK	20MIL	3.5MIL	
FB_B_REFCLK*	FBBREFCLK	20MIL	3.5MIL	100 ohm diff
FB_A_DQ<63..0>			10MIL	
FB_B_DQ<63..0>			10MIL	
FB_A_DQM<7..0>			10MIL	
FB_A_DQS_RN<7..0>			10MIL	
FB_A_DQS_WP<7..0>			10MIL	
FB_B_DQM<7..0>			10MIL	
FB_B_DQS_RN<7..0>			10MIL	
FB_B_DQS_WP<7..0>			10MIL	
FB_A0_CMD<19..0>			15MIL	
FB_A1_CMD<19..0>			15MIL	
FB_B0_CMD<19..0>			15MIL	
FB_B1_CMD<19..0>			15MIL	
FB_A0_RESET			10MIL	
FB_A1_RESET			10MIL	
FB_B0_RESET			10MIL	
FB_B1_RESET			10MIL	

NET Name	MIN_LINE_WIDTH	VOLTAGE
FB_A_AVDD	12MIL	3.3V
FB_A_PLLVDD	12MIL	3.3V
FB_B_AVDD	12MIL	3.3V
FB_B_PLLVDD	12MIL	3.3V
FB_A0_ZQ	12MIL	0.9V
FB_A1_ZQ	12MIL	0.9V
FB_B0_ZQ	12MIL	0.9V
FB_B1_ZQ	12MIL	0.9V
FB_A0_VREF1	12MIL	0.9V
FB_A0_VREF2	12MIL	0.9V
FB_A1_VREF1	12MIL	0.9V
FB_A1_VREF2	12MIL	0.9V
FB_B0_VREF1	12MIL	0.9V
FB_B0_VREF2	12MIL	0.9V
FB_B1_VREF1	12MIL	0.9V
FB_B1_VREF2	12MIL	0.9V

Memory FBC FBD

NET Name	Diffpair	Spacing		
FB_C0_CLK0	FBC0CLK0	80_OHM_DIFF	5MIL	
FB_C0_CLK0*	FBC0CLK0	80_OHM_DIFF	5MIL	
FB_C1_CLK0	FBC1CLK0	80_OHM_DIFF	5MIL	
FB_C1_CLK0*	FBC1CLK0	80_OHM_DIFF	5MIL	
FB_D0_CLK0	FBD0CLK0	80_OHM_DIFF	5MIL	
FB_D0_CLK0*	FBD0CLK0	80_OHM_DIFF	5MIL	
FB_D1_CLK0	FBD1CLK0	80_OHM_DIFF	5MIL	
FB_D1_CLK0*	FBD1CLK0	80_OHM_DIFF	5MIL	
FB_C_REFCLK	FBCREFCLK	20MIL	3.5MIL	100 ohm diff
FB_C_REFCLK*	FBCREFCLK	20MIL	3.5MIL	
FB_D_REFCLK	FBDREFCLK	20MIL	3.5MIL	
FB_D_REFCLK*	FBDREFCLK	20MIL	3.5MIL	100 ohm diff
FB_C_DQ<63..0>			10MIL	
FB_D_DQ<63..0>			10MIL	
FB_C_DQM<7..0>			10MIL	
FB_C_DQS_RN<7..0>			10MIL	
FB_C_DQS_WP<7..0>			10MIL	
FB_D_DQM<7..0>			10MIL	
FB_D_DQS_RN<7..0>			10MIL	
FB_D_DQS_WP<7..0>			10MIL	
FB_C0_CMD<19..0>			15MIL	
FB_C1_CMD<19..0>			15MIL	
FB_D0_CMD<19..0>			15MIL	
FB_D1_CMD<19..0>			15MIL	
FB_C0_RESET			10MIL	
FB_C1_RESET			10MIL	
FB_D0_RESET			10MIL	
FB_D1_RESET			10MIL	

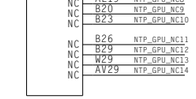
NET Name	MIN_LINE_WIDTH	VOLTAGE
FB_C_AVDD	12MIL	3.3V
FB_C_PLLVDD	12MIL	3.3V
FB_D_AVDD	12MIL	3.3V
FB_D_PLLVDD	12MIL	3.3V
FB_C0_ZQ	12MIL	0.9V
FB_C1_ZQ	12MIL	0.9V
FB_D0_ZQ	12MIL	0.9V
FB_D1_ZQ	12MIL	0.9V
FB_C0_VREF1	12MIL	0.9V
FB_C0_VREF2	12MIL	0.9V
FB_C1_VREF1	12MIL	0.9V
FB_C1_VREF2	12MIL	0.9V
FB_D0_VREF1	12MIL	0.9V
FB_D0_VREF2	12MIL	0.9V
FB_D1_VREF1	12MIL	0.9V
FB_D1_VREF2	12MIL	0.9V



CALIBRATION PIN	DDR1/2	DDR2_40	DDR3
FB_CALx_PD_VDDQ	60	40	60
FB_CALx_PU_GND	60	40	40
FB_CALx_TERM_GND	60	60	40
VREF RATIO	0.5 FBVDDQ		0.7 FBVDDQ

HIGH/LOW
VREF RATIO DDR2 RECOMMEND 1K/1K = 0.500 RATIO
VREF RATIO DDR3 RECOMMEND 511/1.21k = 0.703 RATIO

DEFAULT BASE SCHEMATICS ARE SETUP FOR DDR3



NET Name	Spacing
FB_CALO_PD_VDDQ	20MIL_G2G_25MIL
FB_CALO_PU_GND	20MIL_G2G_25MIL
FB_CALO_TERM_GND	20MIL_G2G_25MIL
FB_CAL1_PD_VDDQ	20MIL_G2G_25MIL
FB_CAL1_PU_GND	20MIL_G2G_25MIL
FB_CAL1_TERM_GND	20MIL_G2G_25MIL

NET Name	MIN_LINE_WIDTH	VOLTAGE
FB_VREF1	12MIL	3.3V
FB_VREF2	12MIL	3.3V

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ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	Memory Signal Constraints, GPU FB-CAL

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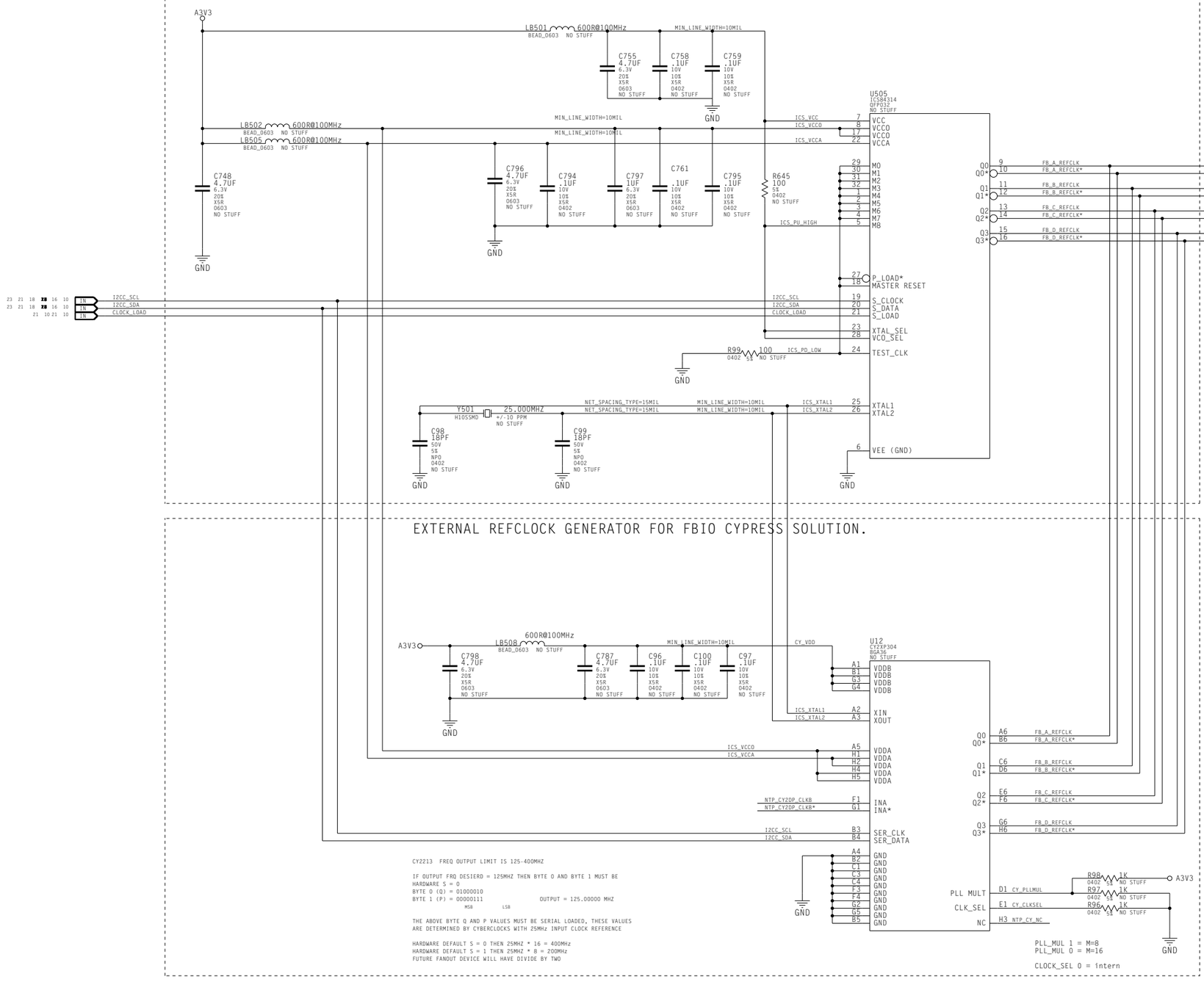
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	9 OF 24
NAME	Blotter	DATE	21-MAY-2004



ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	FBIO refclock generator

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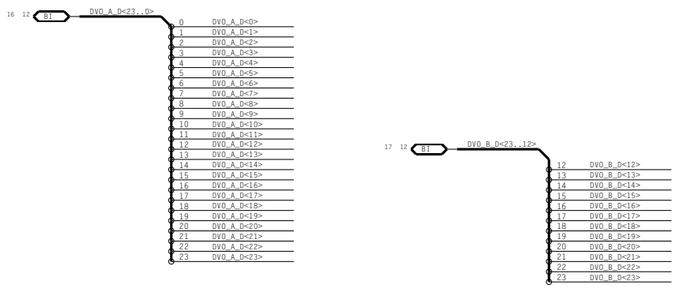
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	10 OF 24
NAME	Blotter	DATE	21-MAY-2004

Straps

Assembly: BIOS



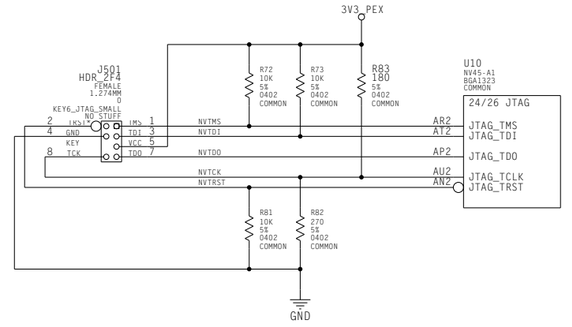
REG: NV_PEXTDEV_BOOT_0

Bit	Signal	VALUE_ID	VALUEs	
00:	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED	
			1 NORMAL	
01:	SUB_VENDOR	SUB_VENDOR	0 NO_BIOS	
			1 read_from_BIOS	
02:	RAM_CFG_0	RAM_CFG[3:0]	0000 RFU	1000 RFU
			0001 RFU	1001 RFU
03:	RAM_CFG_1		0010 RFU	1010 RFU
			0011 RFU	1011 RFU
04:	RAM_CFG_2		0100 RFU	1100 RFU
			0101 RFU	1101 RFU
05:	RAM_CFG_3		0110 RFU	1110 RFU
			0111 SMx32 GDDR3	1111 RFU
06:	CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz	
			01 14.31818 Mhz	
22:	CRYSTAL_1		10 27.000 Mhz	
			11 unknown	
07:	TV_MODE_0	TV_MODE[1:0]	00 SECAM	
			01 NTSC	
08:	TV_MODE_1		10 PAL	
			11 CRT	
09:	AGPBxEnable	AGP_30_Bx	0 AGPBx enabled	
			1 AGPBx disabled	
10:	AGP_SBA	AGP_SBA[0]	0 SBA enabled	
			1 SBA disabled	
11:	AGP_FASTWR	AGP_FASTWR[0]	0 enabled	
			1 disabled	
12:	PCI_DEVID_0	PCI_DEVID[3:0]	0000 0x400 ... 1111 0x40F	
			0000 (0x400)	
13:	PCI_DEVID_1		0001 (0x401)	
			0011 (0x403)	
20:	PCI_DEVID_2		0100 (0x404)	
21:	PCI_DEVID_3			
14:	BUS_TYPE	BUS_TYPE[0]	0 PCI	
			1 AGP	
15:	FP_IFACE	FP_IFACE[0]	0 24Bit	
			1 12Bit	
23:	FB_0	FB[1:0]	00 64M	
			01 128M	
24:	FB_1		10 256M	
			11 512M	
25:	BR	BR[0]	0 BRIDGE disabled	
			1 BRIDGE enabled	
26:	BR_128M	BR bits are ignored if BRIDGE is disabled		
27:	BR_AGP			
28:	BR_IO			
29:	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel	
			01 Serial_AT25F	
30:	ROM_TYPE_1		10 Serial_SST45VF	
			11 RFU	
16:	USER_0	STRAP_USER[3:0]	0000 (default)	
17:	USER_1			
18:	USER_2			
19:	USER_3			

BR02_ PCI DEV ID

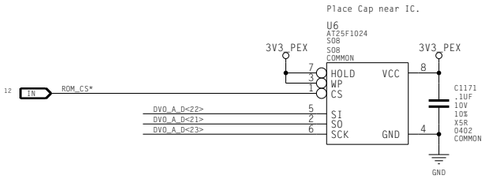
0 = 0x00F8
1 = 0x00F9

JTAG

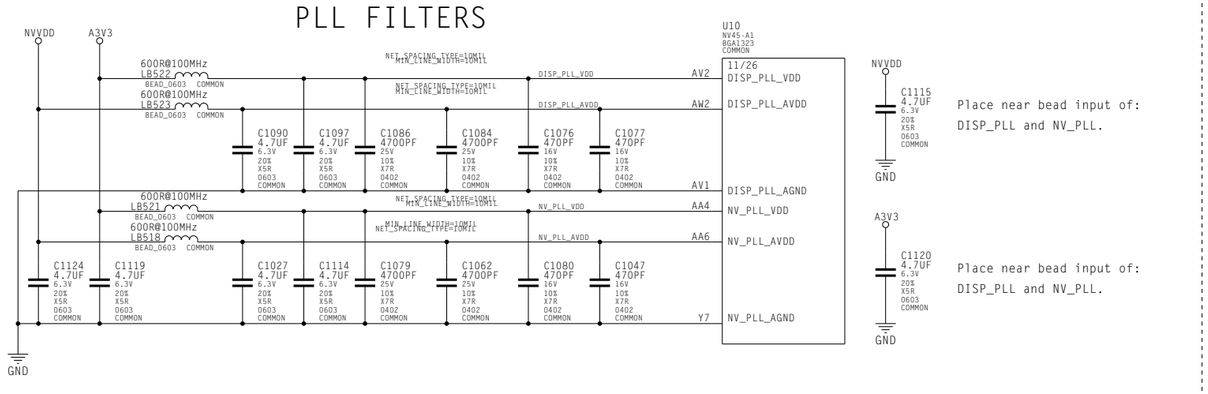


BIOS (serial)

Assembly: BIOS



PLL FILTERS



ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	BIOS, Strappings and Misc

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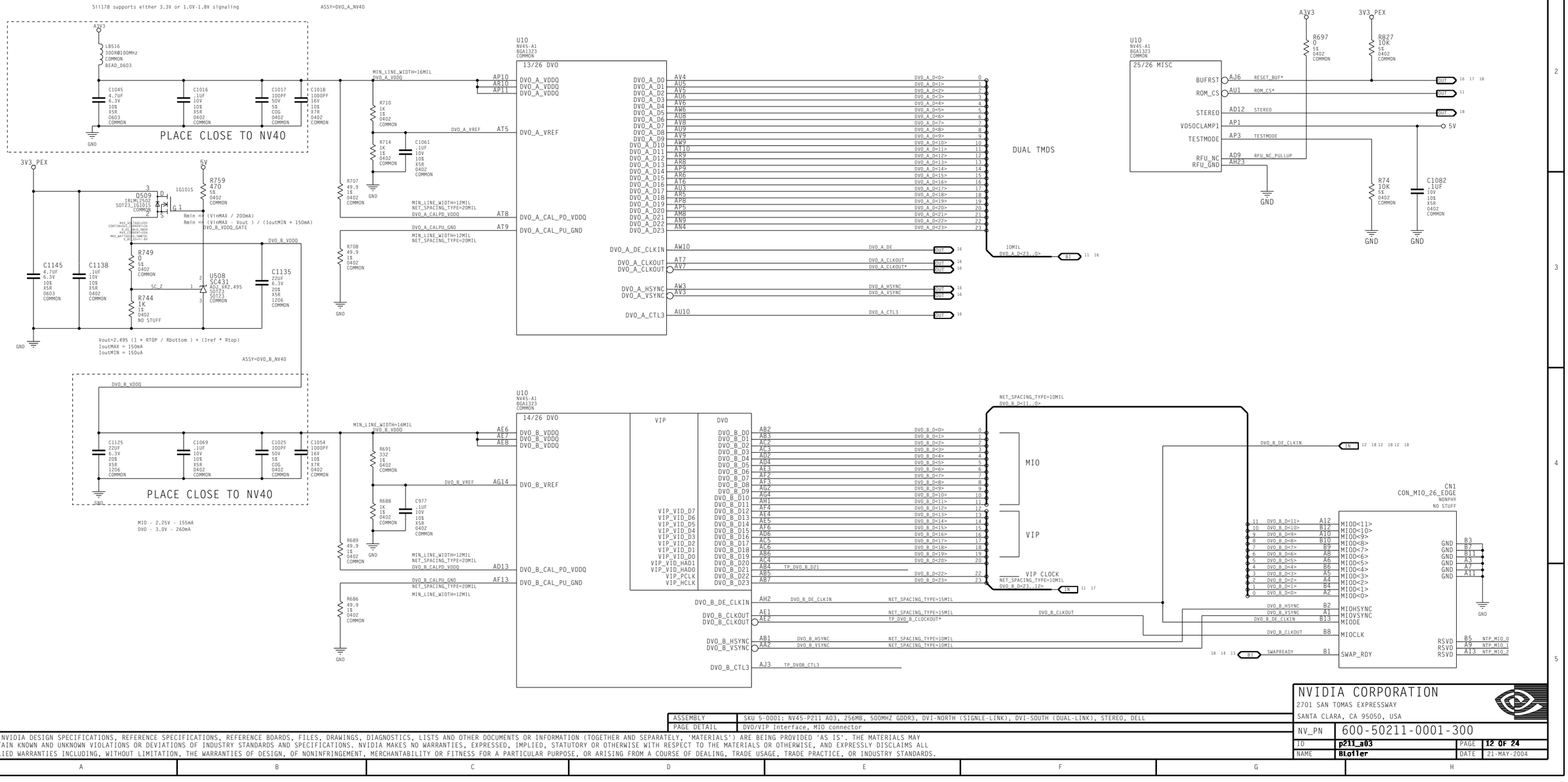
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	11 OF 24
NAME	BLoller	DATE	21-MAY-2004



ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	DVO/VIP Interface, MIO connector

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NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	12 OF 24
NAME	Blotter	DATE	21-MAY-2004

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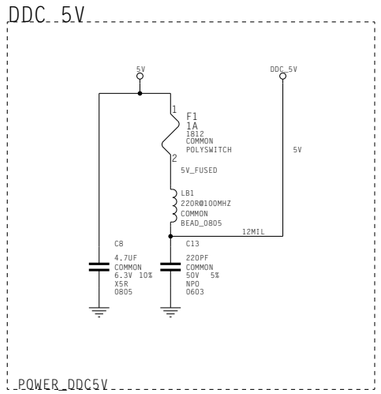

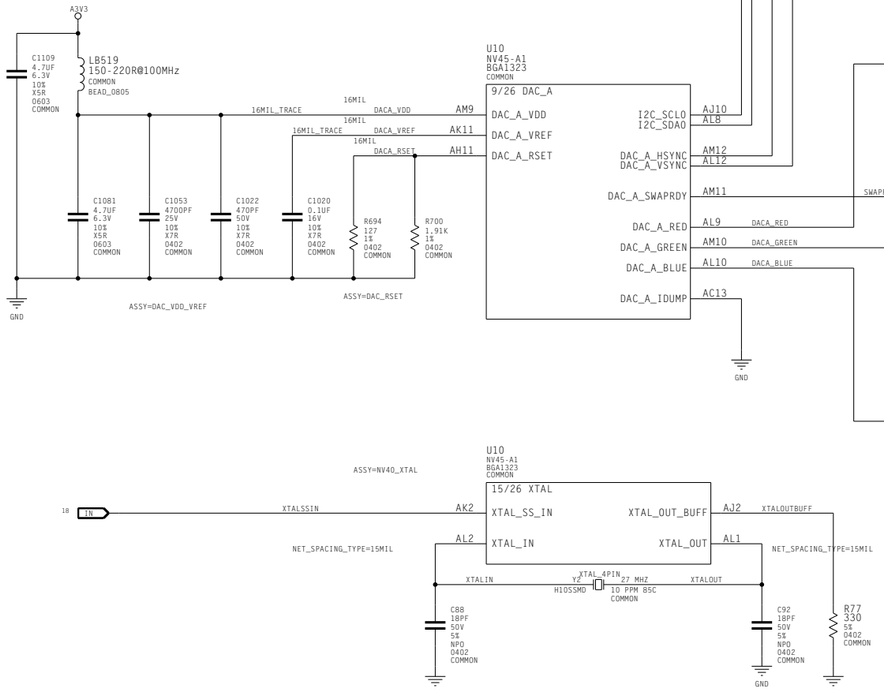

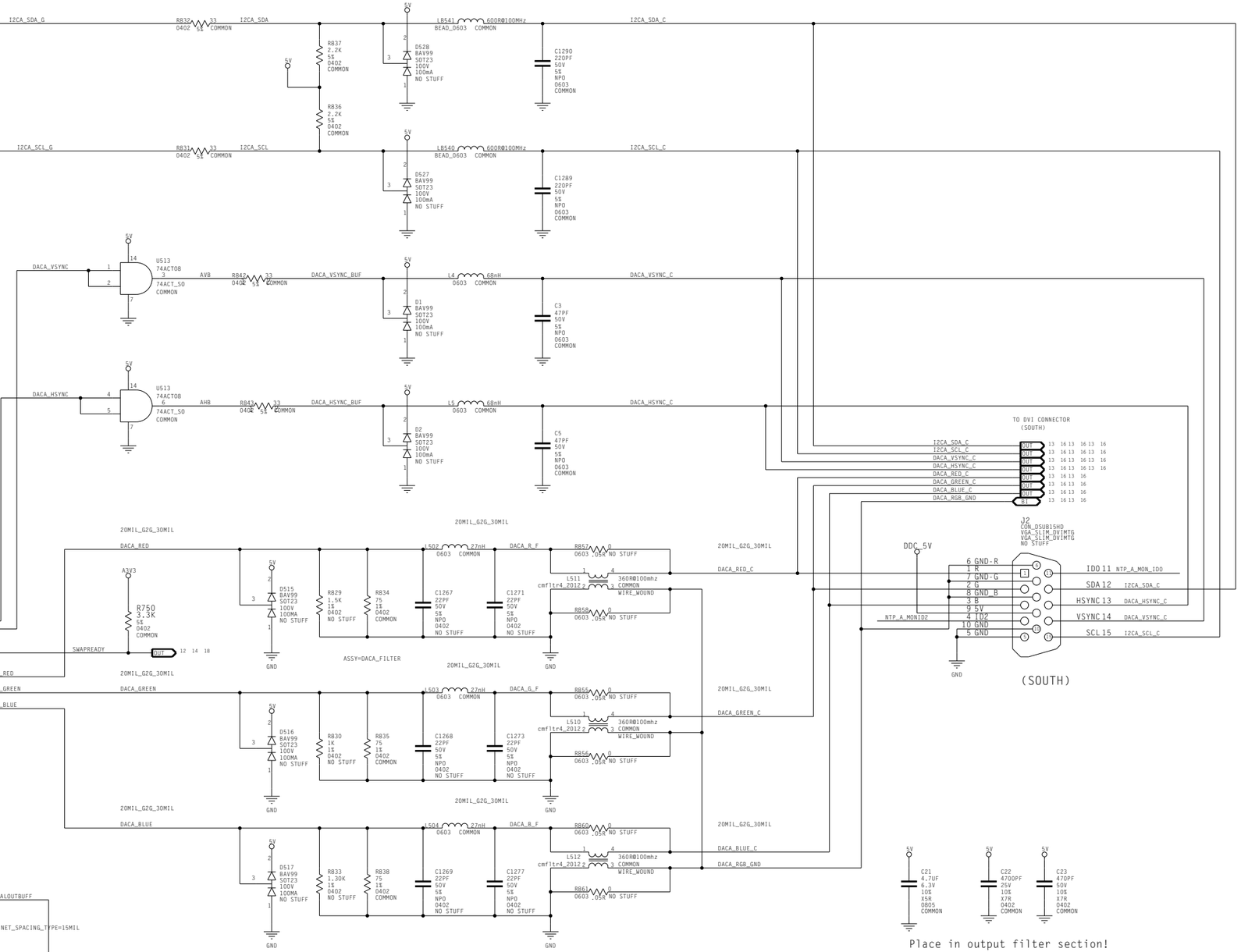

ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	DACA Filter and VGA connector, SOUTH

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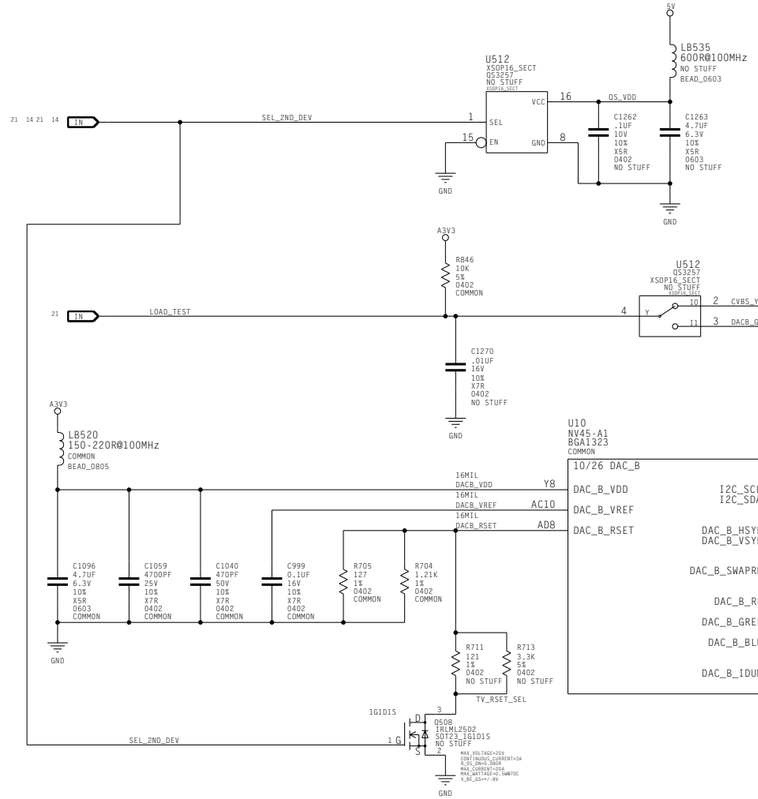
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	13 OF 24
NAME	Blotter	DATE	21-MAY-2004



ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	DACB Filter, RGB SWITCH and VGA connector

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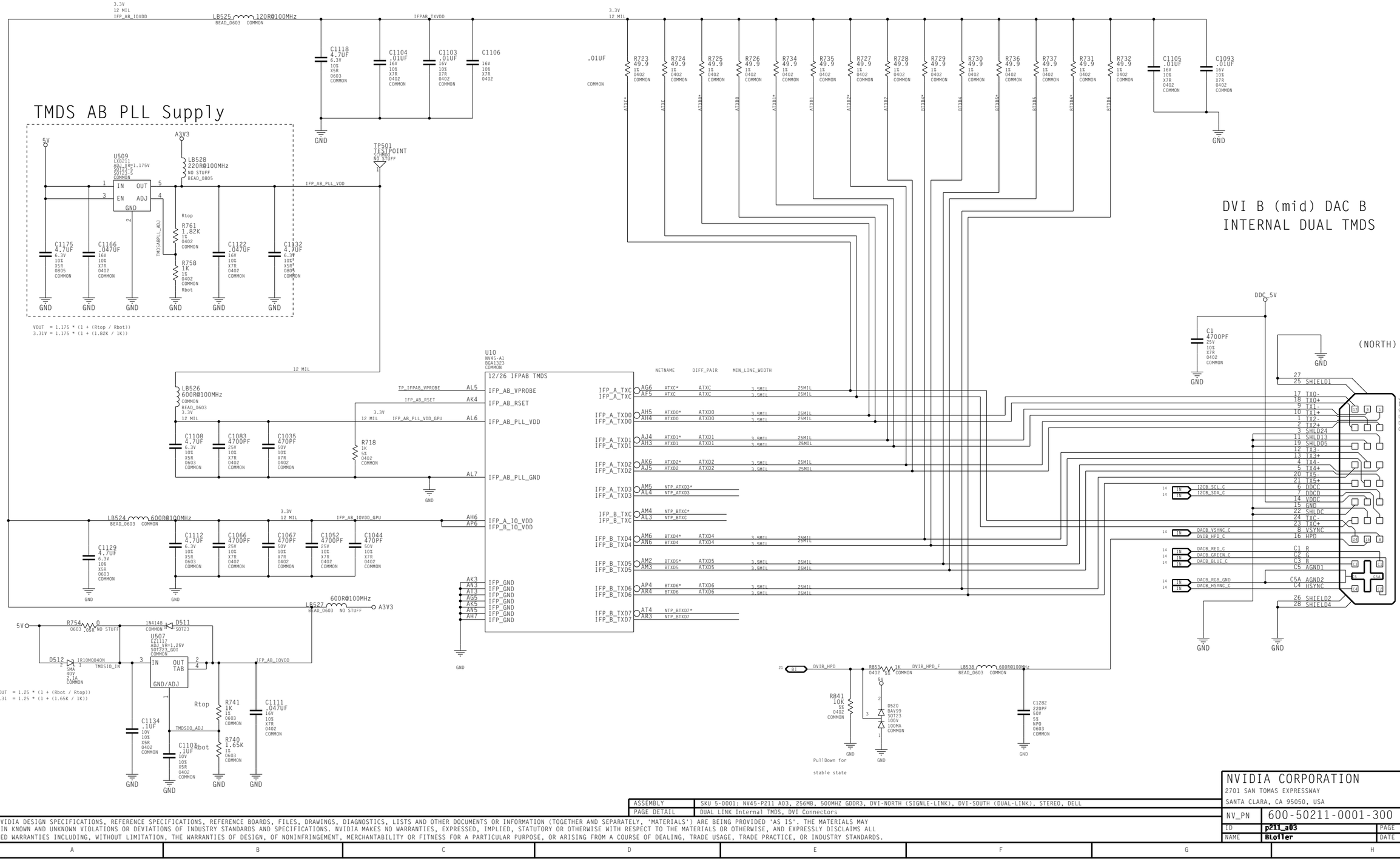
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	14 OF 24
NAME	Blotter	DATE	21-MAY-2004



ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	DUAL LINK Internal TMDS, DVI Connectors

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NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	15 OF 24
NAME	Bloller	DATE	21-MAY-2004

NET RULES (OTHER)

PHYSICAL

SIIA_VCC	12 MIL	SIIA_VCC
SIIA_AVCC	12 MIL	SIIA_AVCC
SIIA_PVCC1	12 MIL	SIIA_PVCC1
SIIA_PVCC2	12 MIL	SIIA_PVCC2

NET RULES

NET	DIFFPAIR	SPACING	MIN_LINE_WIDTH
SIIA_TXD3	SIIA_TXD3	25MIL	3.5MIL
SIIA_TXD3*	SIIA_TXD3	25MIL	3.5MIL
SIIA_TXD4	SIIA_TXD4	25MIL	3.5MIL
SIIA_TXD4*	SIIA_TXD4	25MIL	3.5MIL
SIIA_TXD5	SIIA_TXD5	25MIL	3.5MIL
SIIA_TXD5*	SIIA_TXD5	25MIL	3.5MIL

U510 SII178 78_TQFP64 COMMON — I2C=0x70 (Master) — MASTER — BOTTOM

SII1xx (combi_sym)

36	D<23>	TX0	25
37	D<22>	TX0	24
38	D<21>	TX1	28
39	D<20>	TX1	27
40	D<19>	TX2	31
41	D<18>	TX2	30
42	D<17>		
43	D<16>	TXCLK	22
44	D<15>	TXCLK	21
45	D<14>/SYNCOUT		
46	D<13>/MAST		
47	D<12>/DUAL		
50	D<11>	EXT_SWING	19
51	D<10>		
52	D<9>	AVCC	29
53	D<8>	AVCC	23
54	D<7>		
55	D<6>	PVCC1	18
58	D<5>	PVCC2	49
59	D<4>		
60	D<3>	VCC	1
61	D<2>	VCC	12
62	D<1>	VCC	33
63	D<0>		
		VREF	3
4	HSYNC/SYNCIN		
5	VSYNC		
2	DE		
		PD	10
57	IDCLK	RESVD(GND)	34
56	IDCLK		
		CTL1/A1/DK1/MCL	8
		CTL2/A2/DK2/MDA	7
		CTL3/A3/DK3/ .	6
15	BSEL/SCL		
14	DSEL/SDA		
		AGND	20
		AGND	32
		AGND	26
13	ISEL/RST#		
		PGND1	17
		PGND2	48
		GND	16
		GND	64
11	MSEN	DKEN/GND	35
9	EDG/HPD		

DVO_A_D<23..0> (IN) → SIIA_VCC 47; DVO_A_D<23>..DVO_A_D<12> 50..63

DUAL_SYNC_R 4; DVO_A_VSYNC 5; DVO_A_DE 2

DVO_A_CLKOUT 57; DVO_A_CLKOUT* 56

I2CC_SCL 15; I2CC_SDA 14

RESET_BUF* 13

SIIA_VCC → R801 4.7K 5% 0402 COMMON; R799 4.7K 5% 0402 COMMON → SIIA_MSEN 11; SIIA_HDP 9

For Single Link SIL164/166 is used

SIIA_VCC → R794 4.7K 5% 0402 COMMON; C1220 .1UF 10V 10% X5R 0402 COMMON

R50 4.7K 5% 0402 COMMON

SIIA_AVCC → C57 100PF 50V 5% C0G 0402 COMMON; C1249 100PF 50V 5% C0G 0402 COMMON; C59 .1UF 10V 10% X5R 0402 COMMON; C1251 .1UF 10V 10% X5R 0402 COMMON; C56 4.7UF 6.3V 10% X5R 0603 COMMON

600R@100MHz LB9 COMMON BEAD_0603 → A3V3 → C60 4.7UF 6.3V 10% X5R 0603 COMMON → GND

SIIA_PVCC1 → A3V3 → C1194 100PF 50V 5% C0G 0402 COMMON; C84 .1UF 10V 10% X5R 0402 COMMON; C85 4.7UF 6.3V 10% X5R 0603 COMMON

SIIA_PVCC2 → 600R@100MHz LB531 COMMON BEAD_0603

LB8 BEAD_0603 COMMON 600R@100MHz → C66 4.7UF 6.3V 10% X5R 0603 COMMON; C58 .1UF 10V 10% X5R 0402 COMMON; C1246 100PF 50V 5% C0G 0402 COMMON → GND

SIIA_VCC → C77 100PF 50V 5% C0G 0402 COMMON; C70 100PF 50V 5% C0G 0402 COMMON; C69 100PF 50V 5% C0G 0402 COMMON; C71 .1UF 10V 10% X5R 0402 COMMON; C72 .1UF 10V 10% X5R 0402 COMMON; C1200 4.7UF 6.3V 10% X5R 0603 COMMON

600R@100MHz LB532 COMMON BEAD_0603 → A3V3 → C1185 4.7UF 6.3V 10% X5R 0603 COMMON → GND

MODIFIED AC TERMINATION, USED FOR EMI

10MIL AC	10MIL A5	10MIL A4	10MIL A3	10MIL A2	10MIL A1	10MIL A0	
C39 22PF	C1256 22PF	C1260 22PF	C1261 22PF	C34 22PF	C46 22PF	C36 22PF	50V 5% NPO 0402 NO STUFF

GND

J5 DVI-I-SHLD 90 DVI_I_RA_VERT DVI_I — COMMON

SIIA_TXD0*	R31 150 1% 0402 COMMON	A0	R30 150 1% 0402 COMMON	27	SHIELD1
SIIA_TXD0				25	
SIIA_TXD1*	R36 150 1% 0402 COMMON	A1	R35 150 1% 0402 COMMON	17	TX0-
SIIA_TXD1				18	TX0+
SIIA_TXD2*	R29 150 1% 0402 COMMON	A2	R28 150 1% 0402 COMMON	9	TX1-
SIIA_TXD2				10	TX1+
SIIA_TXD3*	RR18 150 1% 0402 COMMON	A3	RR19 150 1% 0402 COMMON	1	TX2-
SIIA_TXD3				2	TX2+
SIIA_TXD4*	RR16 150 1% 0402 COMMON	A4	RR17 150 1% 0402 COMMON	3	SHLD24
SIIA_TXD4				11	SHLD13
SIIA_TXD5*	RR12 150 1% 0402 COMMON	A5	RR13 150 1% 0402 COMMON	19	SHLD05
SIIA_TXD5				12	TX3-
				13	TX3+
				4	TX4-
				5	TX4+
				20	TX5-
				21	TX5+
				6	DDC
				7	DDC0
				14	VDDC
				15	GND
				22	SHLDC
SIIA_TXC*	R34 150 1% 0402 COMMON	AC	R33 150 1% 0402 COMMON	24	TXC-
SIIA_TXC				23	TXC+
				8	VSYNC
				16	HPD
				C1	R
				C2	G
				C3	B
				C5	AGND1
				C5A	AGND2
				C4	HSYNC
				26	SHIELD2
				28	SHIELD4

IN: I2CA_SCL_C, I2CA_SDA_C, DDC_5V, DACA_VSYNC_C, DVIA_HPD_C, DACA_RED_C, DACA_GREEN_C, DACA_BLUE_C, DACA_RGB_GND, DACA_HSYNC_C

Place near connector

DDC_5V → C2 470DPF 25V 10% X7R 0402 COMMON → GND

(SOUTH)

DVIA_HPD → R13 1K 5% 0402 COMMON → DVIA_HPD_F → LB2 600R@100MHz BEAD_0603 COMMON → C4 220PF 50V 5% NPO 0603 COMMON → GND

R12 10K 5% 0402 COMMON → GND

PullDown for stable state

D4 BAV99 SOT23 100V 100MA COMMON → GND

NET RULES

NET	DIFFPAIR	SPACING	MIN_LINE_WIDTH
SIIA_TXD0	SIIA_TXD0	25MIL	3.5MIL
SIIA_TXD0*	SIIA_TXD0	25MIL	3.5MIL
SIIA_TXD1	SIIA_TXD1	25MIL	3.5MIL
SIIA_TXD1*	SIIA_TXD1	25MIL	3.5MIL
SIIA_TXD2	SIIA_TXD2	25MIL	3.5MIL
SIIA_TXD2*	SIIA_TXD2	25MIL	3.5MIL
SIIA_TXC	SIIA_TXC	25MIL	3.5MIL
SIIA_TXC*	SIIA_TXC	25MIL	3.5MIL

U4 SII178 78_TQFP64 COMMON — I2C=0x72 (Slave) — MASTER — TOP

SII1xx (combi_sym)

36	D<23>	TX0	25
37	D<22>	TX0	24
38	D<21>	TX1	28
39	D<20>	TX1	27
40	D<19>	TX2	31
41	D<18>	TX2	30
42	D<17>		
43	D<16>	TXCLK	22
44	D<15>	TXCLK	21
45	D<14>/SYNCOUT		
46	D<13>/MAST		
47	D<12>/DUAL		
50	D<11>	EXT_SWING	19
51	D<10>		
52	D<9>	AVCC	29
53	D<8>	AVCC	23
54	D<7>		
55	D<6>	PVCC1	18
58	D<5>	PVCC2	49
59	D<4>		
60	D<3>	VCC	1
61	D<2>	VCC	12
62	D<1>	VCC	33
63	D<0>		
		VREF	3
4	HSYNC/SYNCIN		
5	VSYNC		
2	DE		
		PD	10
57	IDCLK	RESVD(GND)	34
56	IDCLK		
		CTL1/A1/DK1/MCL	8
		CTL2/A2/DK2/MDA	7
		CTL3/A3/DK3/ .	6
15	BSEL/SCL		
14	DSEL/SDA		
		AGND	20
		AGND	32
		AGND	26
13	ISEL/RST#		
		PGND1	17
		PGND2	48
		GND	16
		GND	64
11	MSEN	DKEN/GND	35
9	EDG/HPD		

DVO_A_D<23..0> (IN) → SIIA_VCC 47; DVO_A_D<23>..DVO_A_D<12> 50..63

DUAL_SYNC 45; DUAL_SELECT 46

DVO_A_D<11>..DVO_A_D<0> 50..63

DVO_A_HSYNC 4; DVO_A_VSYNC 5; DVO_A_DE 2

DVO_A_CLKOUT 57; DVO_A_CLKOUT* 56

I2CC_SCL 15; I2CC_SDA 14

RESET_BUF* 13

SIIA_VCC → R46 4.7K 5% 0402 COMMON; R782 4.7K 5% 0402 COMMON → SIIA2_MSEN 11; SIIA2_HPD 9

R54 0 5% 0402 NO STUFF

R48 0 5% 0402 DUAL; R47 0 5% 0402 SINGLE NO STUFF

R792 1.5K 5% 0402 COMMON; R791 1.5K 5% 0402 SINGLE NO STUFF

SIIA2_SWING → R32 470 1% 0603 COMMON

SIIA_AVCC; SIIA_PVCC1; SIIA_PVCC2; SIIA_VCC

7114

C1193 .1UF 10V 10% X5R 0402 COMMON; C1192 100PF 50V 5% C0G 0402 COMMON; C1254 100PF 50V 5% C0G 0402 COMMON; C1250 .1UF 10V 10% X5R 0402 COMMON; C1255 4.7UF 6.3V 10% X5R 0603 COMMON → GND

SIIA_VREF

R51 4.7K 5% 0402 COMMON; R49 4.7K 5% 0402 COMMON; C76 .1UF 10V 10% X5R 0402 COMMON → GND

SIIA_VCC → C1238 .1UF 10V 10% X5R 0402 COMMON; C1208 100PF 50V 5% C0G 0402 COMMON; C1201 100PF 50V 5% C0G 0402 COMMON → GND

CTL3

R39 10K 5% 0402 NO STUFF SII164 (Rx); R41 0 5% 0402 COMMON SII178 (Ry) → SIIA_DKEN → GND

STUFF OPTION
Rx for SII164/166
Ry for SII178

Sil178 Dual-Link TMDS

ISEL/RST - I2C Interface Select.
HIGH - active (config programmed by I2C)

When ISEL/RST = HIGH
BSEL/SCL - I2C CLK
DSEL/SDA - I2C DATA

MASTER
I2C Address is 70h and is based on MAST and DUAL pins.

SLAVE
I2C Address is 72h

Notes:

Make sure Software knows and programs this correctly.
1. Detect Dual-Link Capable
2. Detect Master and Slave
3. Both Master and Slave transmitters must set bit 2 (BSEL) at register addr 0x08 to 0 for 12-biot mode
4. For frequencies less than or equal to 165Mhz, bit 0 (PD) at register addr 0x08 of Slave must be set to 0. For frequencies greater than 165Mhz, bit 0 (PD) at register addr 0x08 of Slave must be set to 1.
5. Skew beween Master and Slave can be controlled by DCTL[2:0] register
6. Both Single-Link and Dual-Link mode will be configured via I2CC

ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	DUAL LINK TMDS External with Silicon Image

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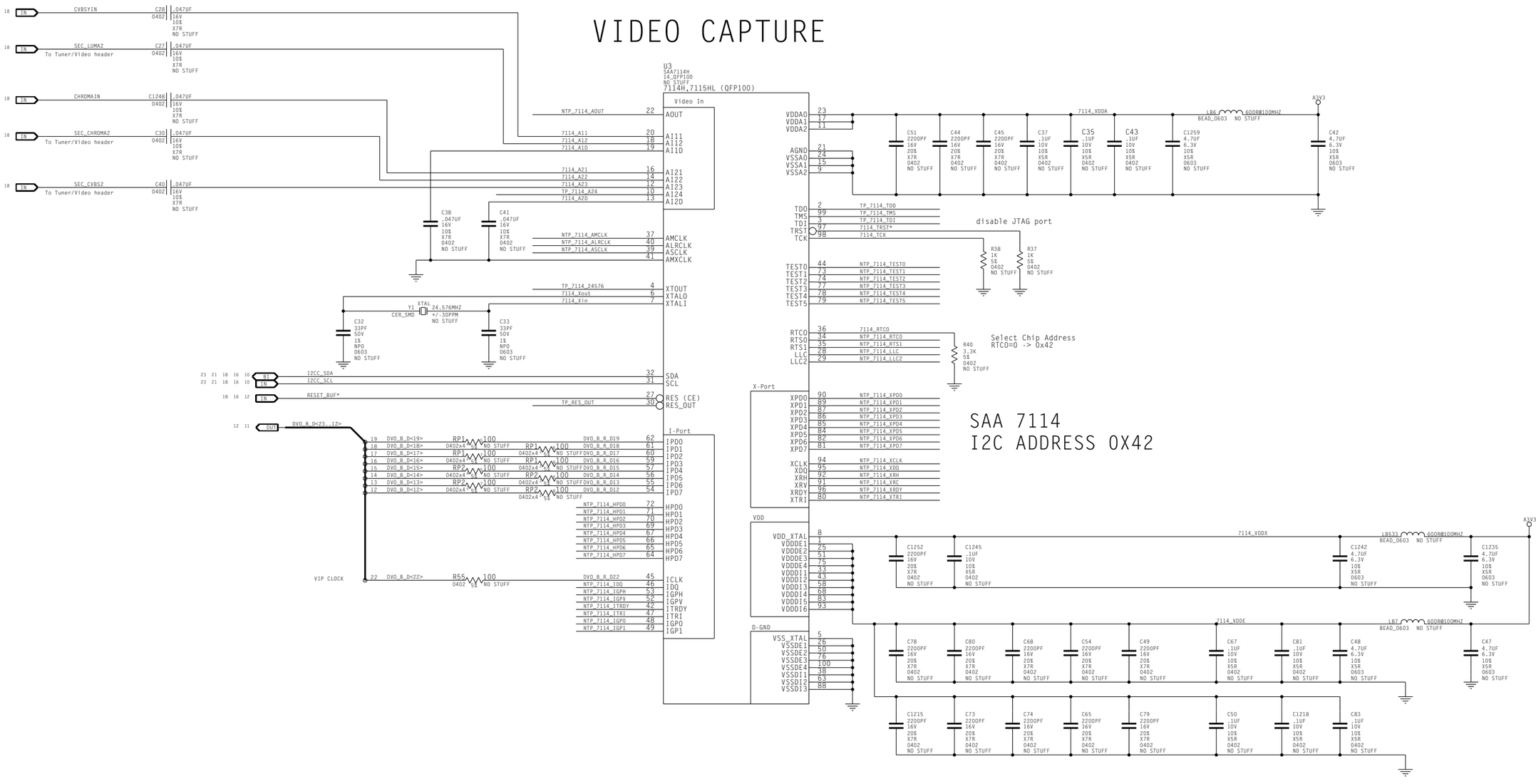
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	16 OF 24
NAME	BLoiler	DATE	21-MAY-2004

VIDEO CAPTURE

NET RULES

NET	SPACING	PHYSICAL	VOLTAGE
7114_VDDA		12 MIL	3.3V
7114_VDDE		12 MIL	3.3V
7114_VDDX		12 MIL	3.3V
7114_Xout	20MIL		
7114_Xin	20MIL		

ASSY: 7114_COMMON



ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	Video Capture (SAA7114)

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NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	17 OF 24
NAME	Bloiler	DATE	21-MAY-2004

BKT1
DB153152_DB151552_MDIN490_TEXT_1_2_DUAL_WIDE
ATX_2X_TOP
NO STUFF
MECH. MOUNTING TOP
GND

PCI TUNER / INTERNAL VIDEO NOTES:

1X5 header can be used if only internal video is required.
1X12 header will be populated for both PCI tuner and internal video.

ASSEMBLY=TUNER_VI*

SEC_CVBS2 → R42 18 0402 5% NO STUFF → SEC_CVBS2A → D10 BAV99 SOT23 100V 100mA NO STUFF (5V)
SEC_LUMA2 → R800 18 0402 5% NO STUFF → SEC_LUMA2A → D513 BAV99 SOT23 100V 100mA NO STUFF (5V)
SEC_CHROMA2 → R43 18 0402 5% NO STUFF → SEC_CHROMA2A → D11 BAV99 SOT23 100V 100mA NO STUFF (5V)

C61 22PF 0603 50V 5% NPO NO STUFF
L11 1.8uH 0603 NO STUFF
C63 330PF 50V 5% NPO 0603 NO STUFF
C52 270PF 50V 5% NPO 0603 NO STUFF
SEC_CVBS
C1247 22PF 0603 50V 5% NPO NO STUFF
L501 1.8uH 0603 NO STUFF
C1241 330PF 50V 5% NPO 0603 NO STUFF
C1257 270PF 50V 5% NPO 0603 NO STUFF
C62 22PF 0603 50V 5% NPO NO STUFF
L12 1.8uH 0603 NO STUFF
C64 330PF 50V 5% NPO 0603 NO STUFF
C53 270PF 50V 5% NPO 0603 NO STUFF
SEC_LUMA
SEC_CHROMA
J8 HDR_1X5 MALE 2MM YES con_hdr_1x5 NO STUFF

R44 56 5% 0402 NO STUFF
R79B 56 5% 0402 NO STUFF
R45 56 5% 0402 NO STUFF
GND

Filters are no stuff by default.

5V
R810 3.3K 5% 0402 COMMON
U511 74LVC1G08/NC7S08 SC70-5 COMMON
18 12 18 12 IN STEREO → BUFFSTEREO
C1258 .1UF 10V 10% X5R 0402 COMMON
D514 BAV99 SOT23 100V 100mA NO STUFF
DDC_5V
DNI FOR V1VO
R814 33 040Z 5% NO STUFF
R815 33 040Z 5% COMMON
BUFFSTEREO_4pin
LB5 220R@100MHz BEAD_0805 NO STUFF
LB534 600R@100MHz BEAD_0603 NO STUFF
I2CC_SCL_BUFFSTEREO_R
STEREO_5V
ST_INT_GND
BUFFSTEREO_C
ST_INT_SHLD
J7 HDR_1M4 MALE 2.0MM N/A NORM NO STUFF
C29 .1UF 10V 10% X5R 0402 NO STUFF
C31 220PF 50V 5% NPO 0603 NO STUFF
R27 0 .05R 0603 NO STUFF
R26 0 .05R 0603 NO STUFF
GND

DDC_5V
LB3 220R@100MHz BEAD_0805 COMMON
12MIL
MDIN_SCL_C_STEREO
LB539 600R@100MHz BEAD_0603 COMMON
C1287 220PF 50V 5% C0G 0402 COMMON
STUFF (3) FOR STEREO/VIVO
D524 BAV99 SOT23 100V 100mA NO STUFF (5V)
DNI FOR STEREO
R854 0 0402 5% NO STUFF
I2CC_SCL IN 10 16 17 18 21 23

J3 CON_MINIDIN_3_SPRING STEREO3D COMMON
Pb out 9 out
C/Pr 8 out
Y/CVBS 1 in
5 GND
GND 3
SDA 4
Y/CVBS out 6
C in 2

14 IN CVBS_PBOUT → R848 0 0402 5% NO STUFF → CVBS_PBOUT_F → L507 1.8uH 0603 NO STUFF → MDIN_PBout_C
C1274 .022UF 0402 16V 10% X7R NO STUFF
C1276 4700PF 25V 10% X7R 0402 NO STUFF
C12B5 .1UF 10V 10% X5R 0402 NO STUFF
D523 BAV99 SOT23 100V 100mA NO STUFF (5V)
COMPOSITE

14 IN COUT → R14 0 0402 5% NO STUFF → COUT_F → L6 1.8uH 0603 NO STUFF → MDIN_COut_C
C14 .022UF 0402 16V 10% X7R NO STUFF
C20 1UF 10V 10% X5R 0603 NO STUFF
C12 .022UF 16V 10% X7R 0402 NO STUFF
D8 BAV99 SOT23 100V 100mA NO STUFF (5V)

17 OUT CVBSYIN → R847 18 0402 5% NO STUFF → CVBSYIN_R → L509 1.8uH 0603 NO STUFF → MDIN_Yin_C
C1272 .1UF 0402 10V 10% X5R NO STUFF
C1279 .022UF 16V 10% X7R 0402 NO STUFF
C1288 470PF 25V 10% X7R 0402 NO STUFF
R850 56 5% 0402 NO STUFF
D522 BAV99 SOT23 100V 100mA NO STUFF (5V)

MDIN_PBout_C → MDIN_COut_C → MDIN_Yin_C
MDIN_GND
Rgnd R7 0 .05R 0603 COMMON
GND FOR STEREO
Rgnd_Video R8 1UF 10% 0603 COMMON
STUFF 1UF CAP WHEN STEREO ELSE 0 OHM R

MDIN_SDA_C → LB4 600R@100MHz BEAD_0603 NO STUFF → I2CC_SDA BI 10 16 17 18 21 23
C6 .022UF 16V 10% X7R 0402 NO STUFF
C19 .022UF 0402 16V 10% X7R NO STUFF
D3 BAV99 SOT23 100V 100mA NO STUFF (5V)

MDIN_Yout_C → L7 1.8uH 0603 NO STUFF → CVBS_YOUT_F → R16 0 0402 5% NO STUFF → CVBS_YOUT IN 14
C7 .1UF 10V 10% X5R 0402 NO STUFF
C15 .1UF 10V 10% X5R 0402 NO STUFF
D9 BAV99 SOT23 100V 100mA NO STUFF (5V)

MDIN_Cin_C → L508 1.8uH 0603 NO STUFF → CHROMAIN_R → R849 18 0402 5% NO STUFF → CHROMAIN OUT 17
C1275 .1UF 0402 10V 10% X5R NO STUFF
C12B6 .1UF 10V 10% X5R 0402 NO STUFF
C1278 4700PF 25V 10% X7R 0402 NO STUFF
D521 BAV99 SOT23 100V 100mA NO STUFF (5V)
R826 56 5% 0402 NO STUFF

NOTE:
Rgnd can be used for EMI purposes.

Framelock

Assembly: FRAMELOCK

J6 HDR_2M6 FEMALE 2.54MM 0 NO NORM NO STUFF
STEREO 1 STER
I2CC_SCL 3 SCK
I2CC_SDA 5 SDA
GPIO4_VTG_RST 7 VRST
9 SRDY
11 CLK
GND 2
GND 4
GND 6
RST* 8
12V 10
12V 12
FRAMELOCK
12VEXT_IN
RESET_BUF* IN 12 16 17

R19 0 0402 5% COMMON GPIO4_VTG_RST_C
C25 4.7K 50V 5% X7R 0402 COMMON
make 10k when header not stuffed
C26 .047UF 16V 10% X7R 0402 NO STUFF
RSV_FMLK

SWAPREADY IN 14 13 12
keep stubs very short.
XTALSSIN OUT 13 → R78 0 0402 5% NO STUFF
DVO_B_DE_CLKIN OUT 12 → R75 0 0402 5% NO STUFF
R79 0 5% 0402 NO STUFF
R76 0 5% 0402 NO STUFF
GND

ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	Video In/Out Connector External/Internal (MiniDin)

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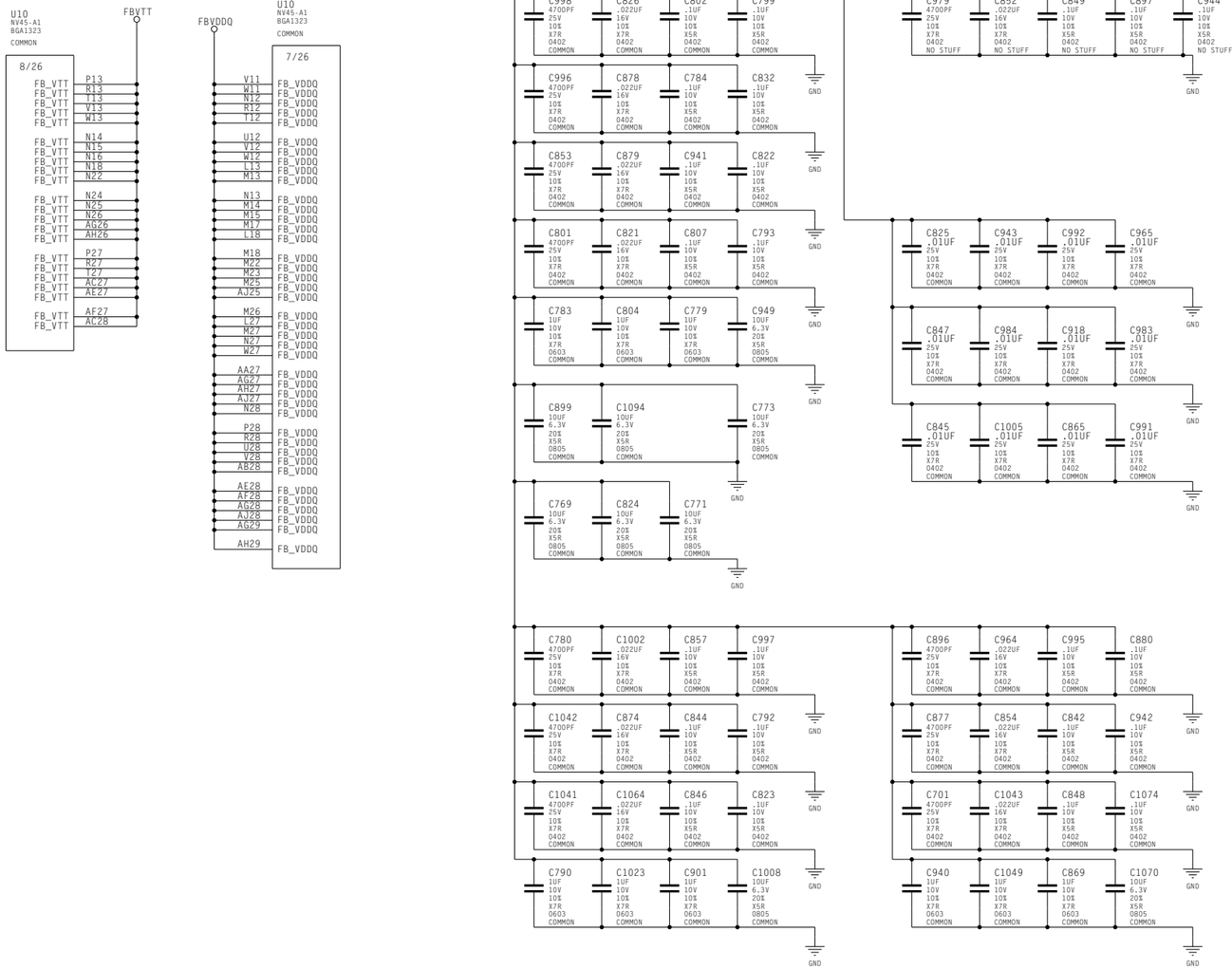
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	18 OF 24
NAME	Blotter	DATE	21-MAY-2004



ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	FBVDDQ, FBVTT DECOUP

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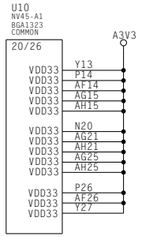
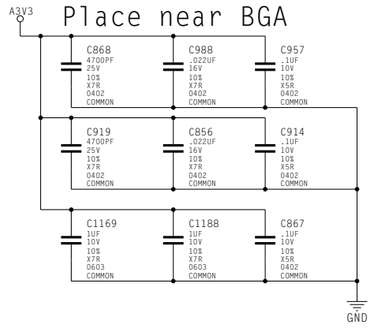
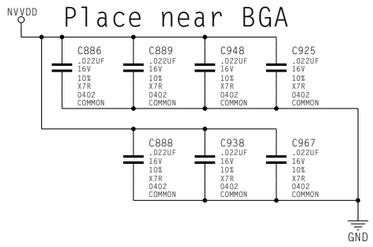
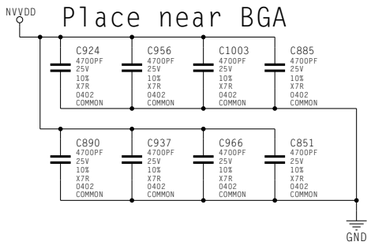
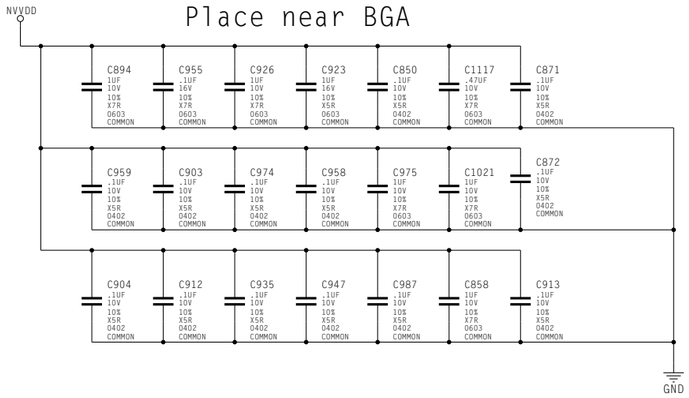
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	19 OF 24
NAME	Bloller	DATE	21-MAY-2004

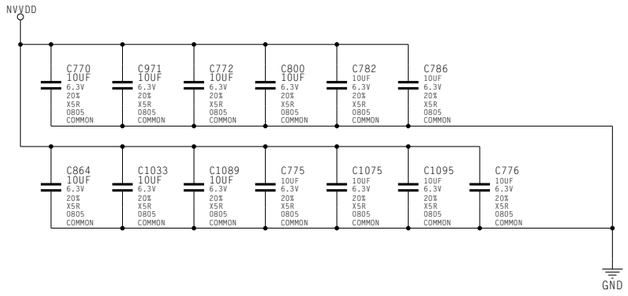


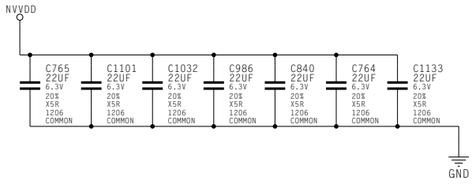


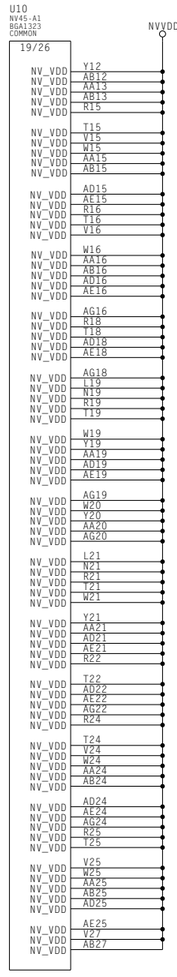












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ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	3V3, NVVDD DECOUP

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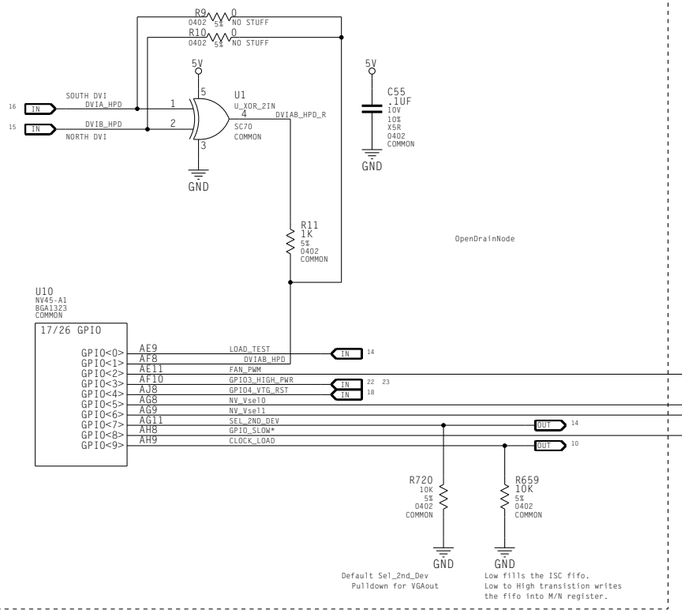
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	20 OF 24
NAME	Blotter	DATE	21-MAY-2004

NET RULES

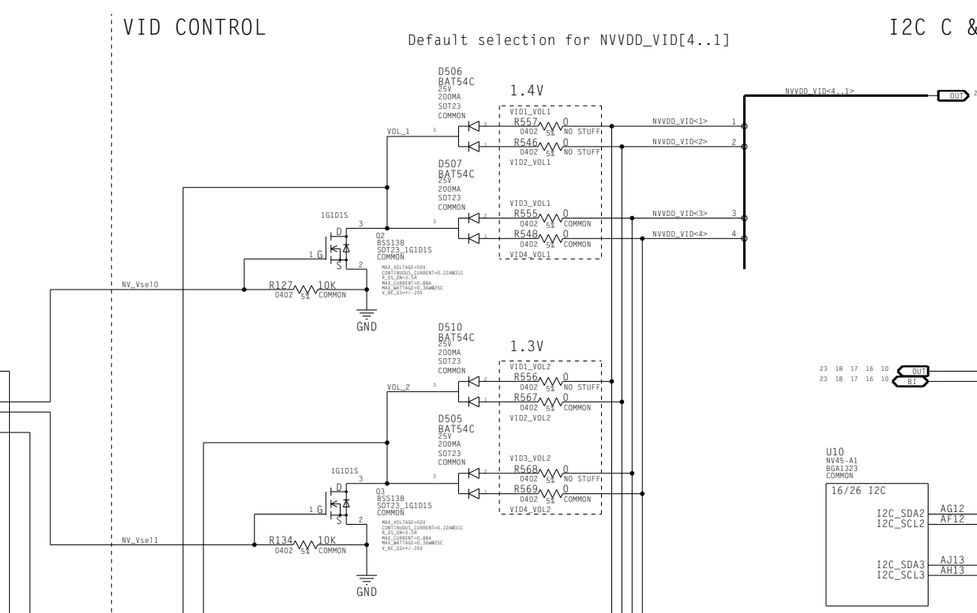
	NET	SPACING	PHYSICAL
BT	THERMDA		10MIL
BT	THERMDC		10MIL
BT	FAN_PWM	20MIL	10MIL
BT	FAN_PWM_B	20MIL	12MIL
BT	FAN_PWM_C	20MIL	12MIL

GPIO CONTROL

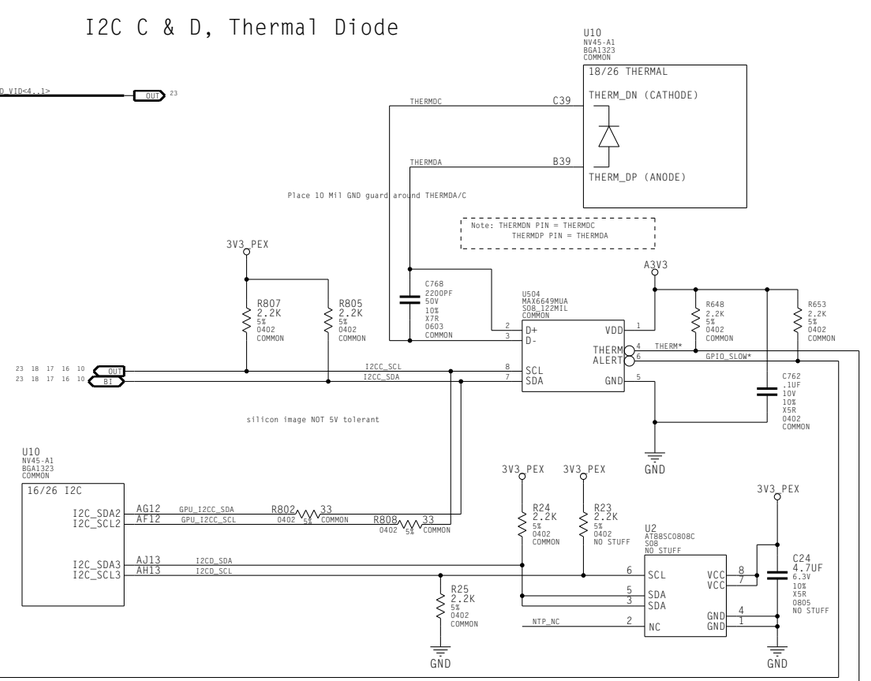


VID CONTROL

Default selection for NVVDD_VID[4..1]



I2C C & D, Thermal Diode



NVVDD Voltage Select

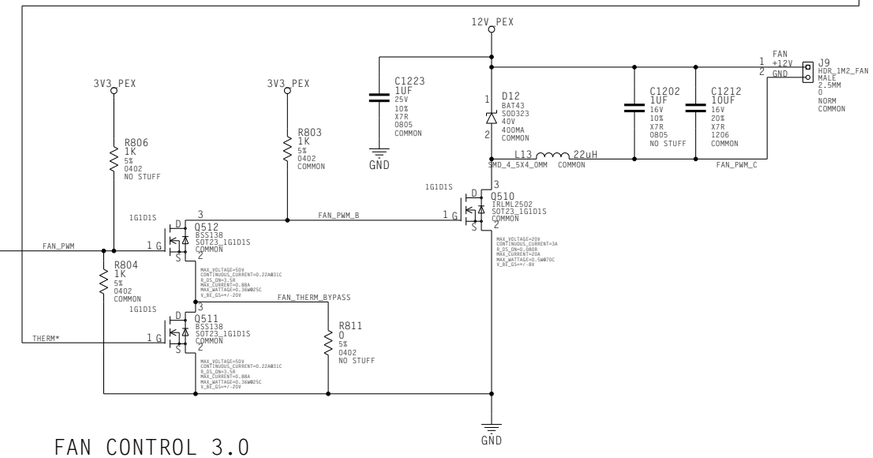
NVVDD = 0.8V-1.55V (30A)

Regulator: ISL6563

Control via NV_GPIOs NV_VSEL[2..0] :

VID 4 3 2 1	NVVDD Vout
1 1 1 1	0.80V
1 1 1 0	0.85V
1 1 0 1	0.90V
1 1 0 0	0.95V
1 0 1 1	1.00V
1 0 1 0	1.05V
1 0 0 1	1.10V
1 0 0 0	1.15V
0 1 1 1	0.20V
0 1 1 0	1.25V
0 1 0 1	1.30V
0 1 0 0	1.35V
0 0 1 1	1.40V
0 0 1 0	1.45V
0 0 0 1	1.50V
0 0 0 0	1.55V

FAN CONTROL 3.0



ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	GPIOs, NVVDD VID, TEMP and FAN Control

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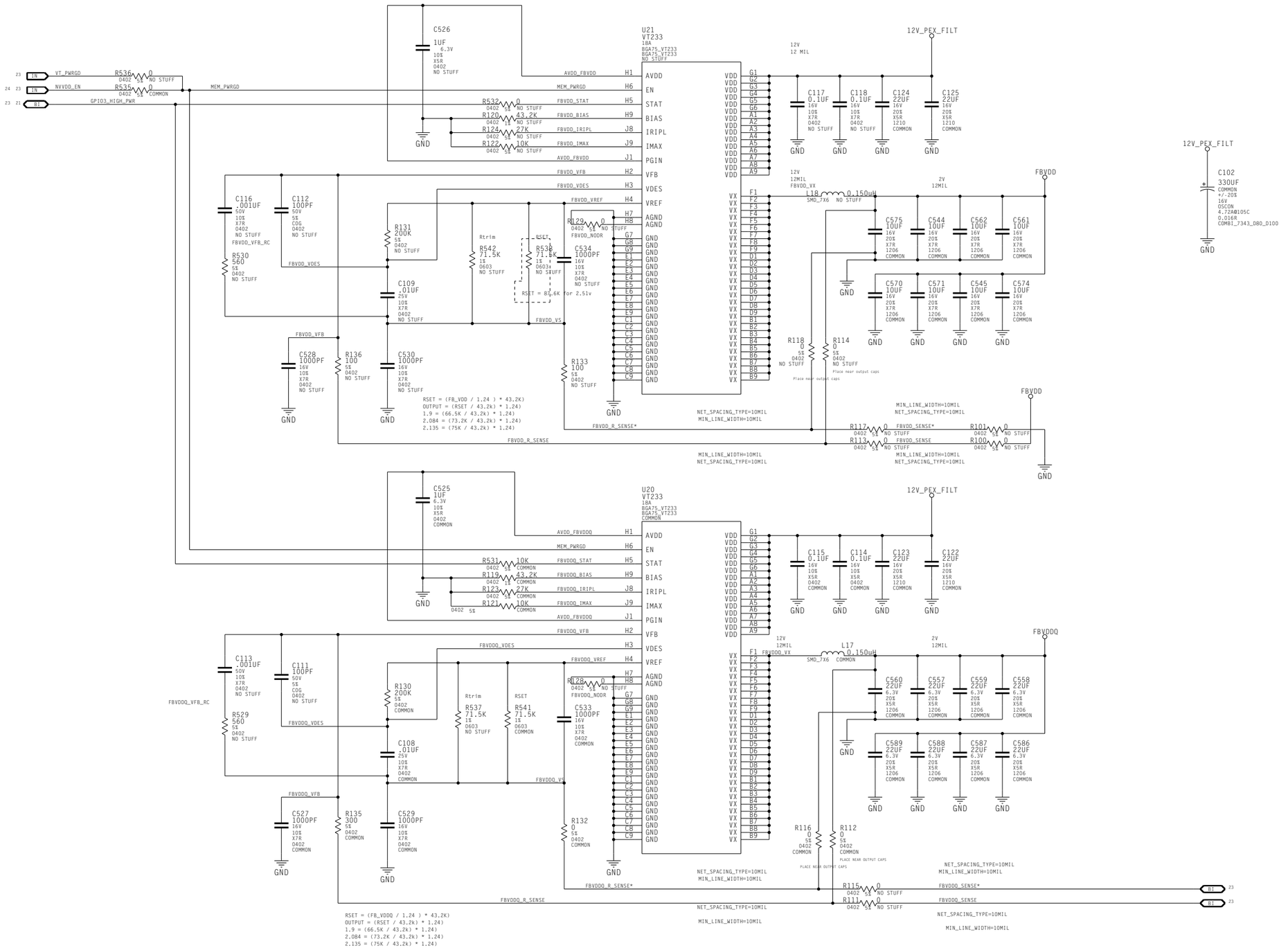
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	21 OF 24
NAME	Bloller	DATE	21-MAY-2004



ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	POWER SUPPLY: FBVDD, FBVDDQ

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NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	22 OF 24
NAME	Blotter	DATE	21-MAY-2004

NVVDD = 0.8V..1.5V (60A)

NOTES:
For each 1103S, the ground pins H6, H7, and Iref should be connected with traces to the input cap ground on J7 and there the via is located to tie to regular GND.

The analog ground amongst different 1103S should not be connected together.

NET RULES

NET	LINE WIDTH	VOLTAGE
5V	12 MIL	5V
NVVDD	24 MIL	1.4V
12V_EXT2	12 MIL	12V
12V_EXT1	12 MIL	12V
12V_PEX	12 MIL	12V

U503 VT1103M VID(0.8-1.6V) TQFP48 COMMON

U18 VT1103S N/A BGA59 COMMON

U19 VT1103S N/A BGA59 COMMON

U17 VT1103S N/A BGA59 COMMON

U10 NV45-A1 BGA1323 COMMON

4AMP SPEC Iripple each 22UF input CAP AT 100MF

0.005 OHM ESR AT 1MHZ, 100MF MLCC

PCIEX_EXTERNAL (3.3V) = EXTERNAL CONNECTOR IS PLUGGED IN
PCIEX_EXTERNAL (GND) = EXTERNAL CONNECTOR NOT PLUGGED IN, CLOCK DOWN MODE ACTIVE.

PRSNT* (GND) = NOT PLUGGED INTO SOURCE
PRSNT* (FLOAT) = NOT PLUGGED INTO SOURCE
PIN 1,4, 5 GO TO 4-PIN HD CONN#2
PIN 6,3,5 GO TO 4-PIN HD CONN#1

PLACE LED TOPSIDE, NOT UNDERNEATH ANY HEAT SINK

NVVDD Voltage Select

Regulator: VT1103

Control via NV_GPIOs NV_VSEL[2..0] :

NV_VSEL 2	VID 1	0	4	3	2	1	0	NVVDD (Vofs=0V) Vout
1	1	1	0	0	0	1	0	1.50V
1	1	0	0	0	1	1	0	1.40V
1	0	1	0	1	0	1	0	1.30V
1	0	0	0	1	1	1	0	1.20V
0	1	1	1	0	0	1	0	1.10V (default)
0	1	0	1	0	0	1	0	1.00V
0	0	1	1	1	0	1	0	0.90V
0	0	0	1	1	1	1	0	0.80V

* GPIO's are inverted

Defaults are defined on Page 23
Rofs = OR

ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	POWER SUPPLY: NVVDD, PCI-EX EXTERNAL POWER

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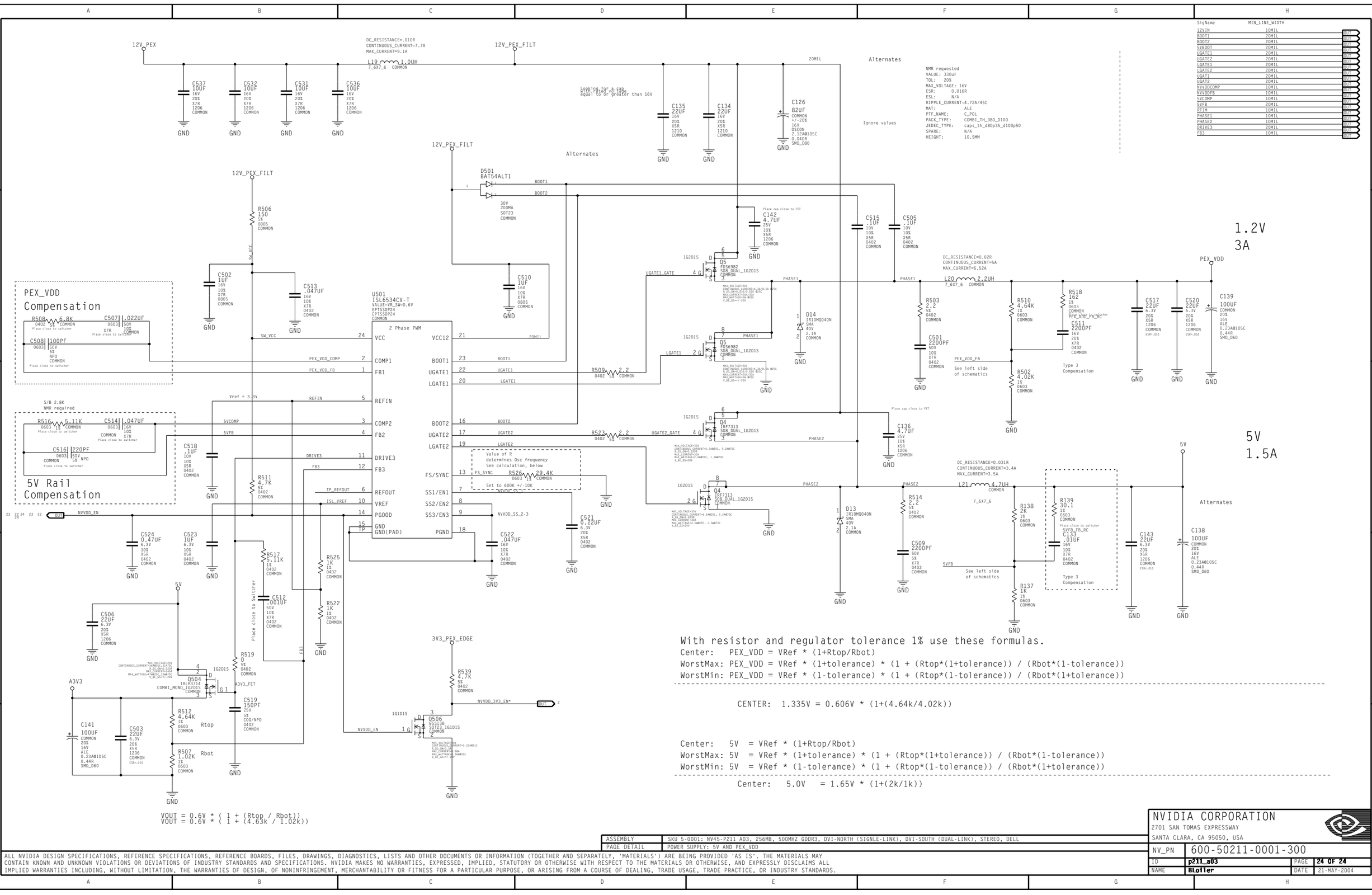
NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	23 OF 24
NAME	Blotter	DATE	21-MAY-2004



ASSEMBLY	SKU 5-0001: NV45-P211 A03, 256MB, 500MHZ GDDR3, DVI-NORTH (SIGNLE-LINK), DVI-SOUTH (DUAL-LINK), STEREO, DELL
PAGE DETAIL	POWER SUPPLY: 5V AND PEX_VDD

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NV_PN	600-50211-0001-300		
ID	p211_a03	PAGE	24 OF 24
NAME	Blotter	DATE	21-MAY-2004