P815-D01: G96 MXM V3.0
256/512MB 128-BIT GDDR3
LVDS, QUAD DP

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SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10815-base-400	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
1	SKU0000	600-10815-0000-400	G96M 128bit GDDR3 MXM V3.0
2	SKU0001	600-10815-0001-400	P815-D01 SKU1 G96-600 MXM3.0 TYPE-A 512MB 4pcs 32Mx32
3	SKU0002	600-10815-0002-400	P815-D01 SKU2 G96-750 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
4	SKU0003	600-10815-0003-400	P815-D01 SKU3 G96-630 MXM3.0 TPYE-A 256MB 4pcs 16MX32
5	SKU0004	600-10815-0004-400	P815-D01 SKU4 G96-630 MXM3.0 TPYE-A 256MB 4pcs 16MX32
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ASSEMBLY	P815-D01 SKU3 G96-630 MXM3.0 TPYE-A 256MB 4pcs 16MX32
PAGE DETAIL	Cover Page

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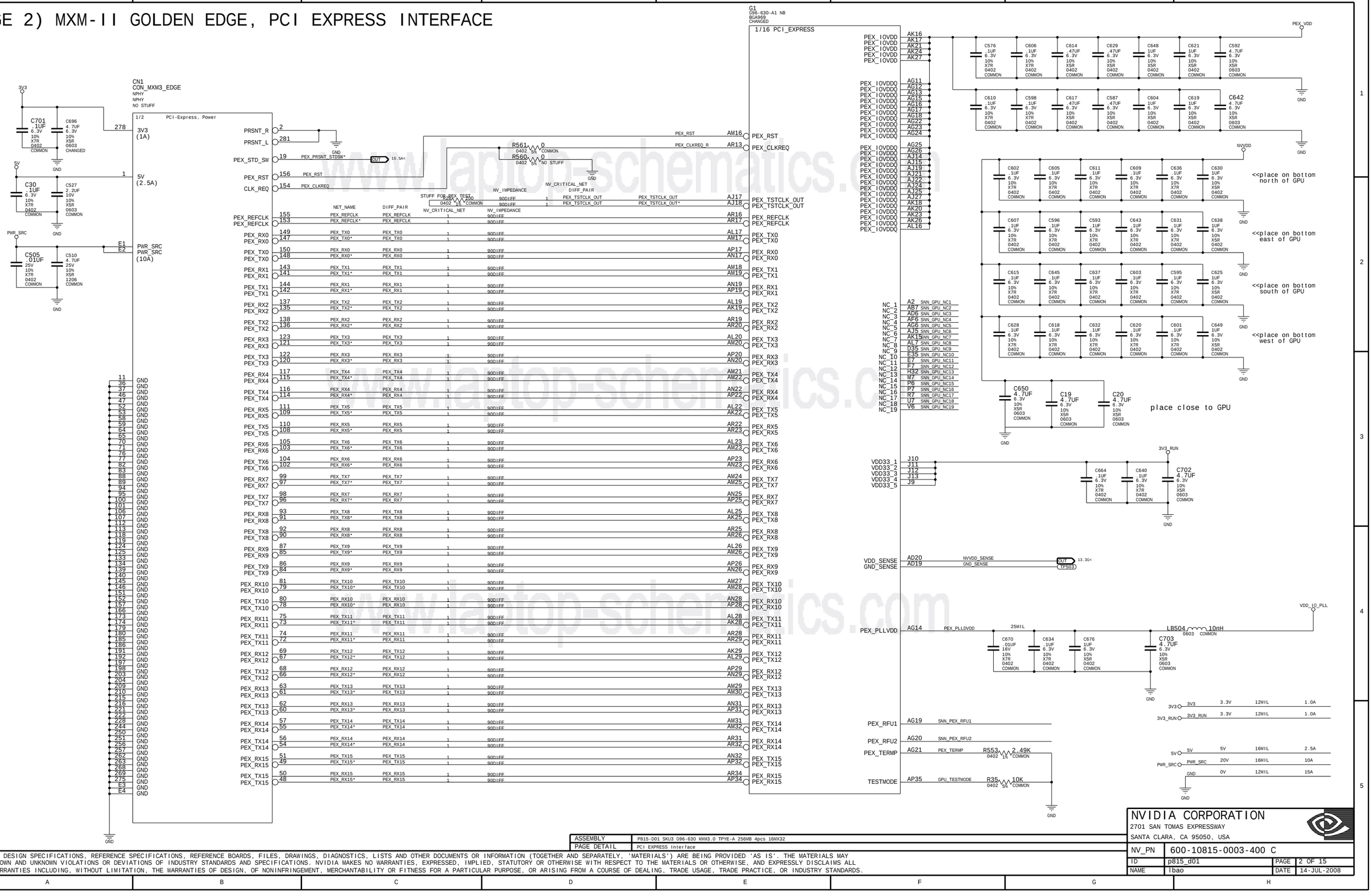
PAGE 2) MXM-II GOLDEN EDGE, PCI EXPRESS INTERFACE



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ASSEMBLY	P815-D01 SKU3 G96-630 MXM3.0 TPYE-A 256MB 4pcs 16MX32
PAGE DETAIL	PCI EXPRESS Interface

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PAGE 3) GPU MEMORY INTERFACE

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PAGE DETAIL	Frame Buffer GPU Interface

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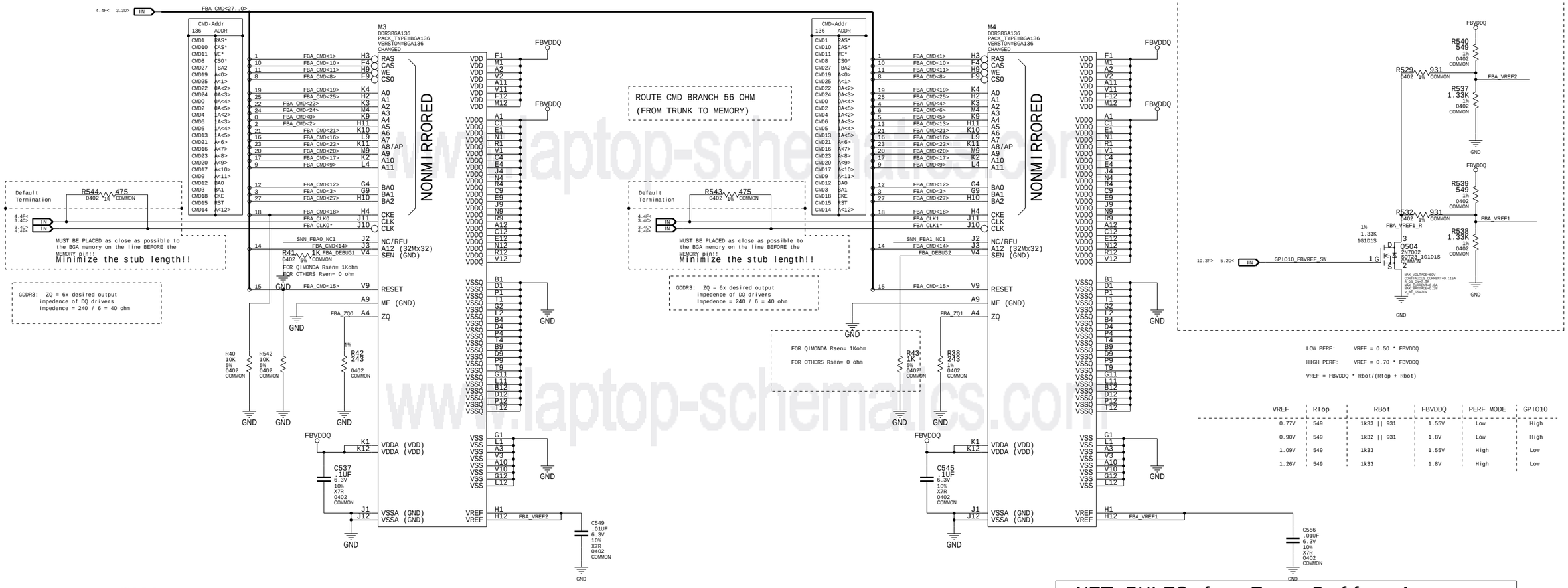
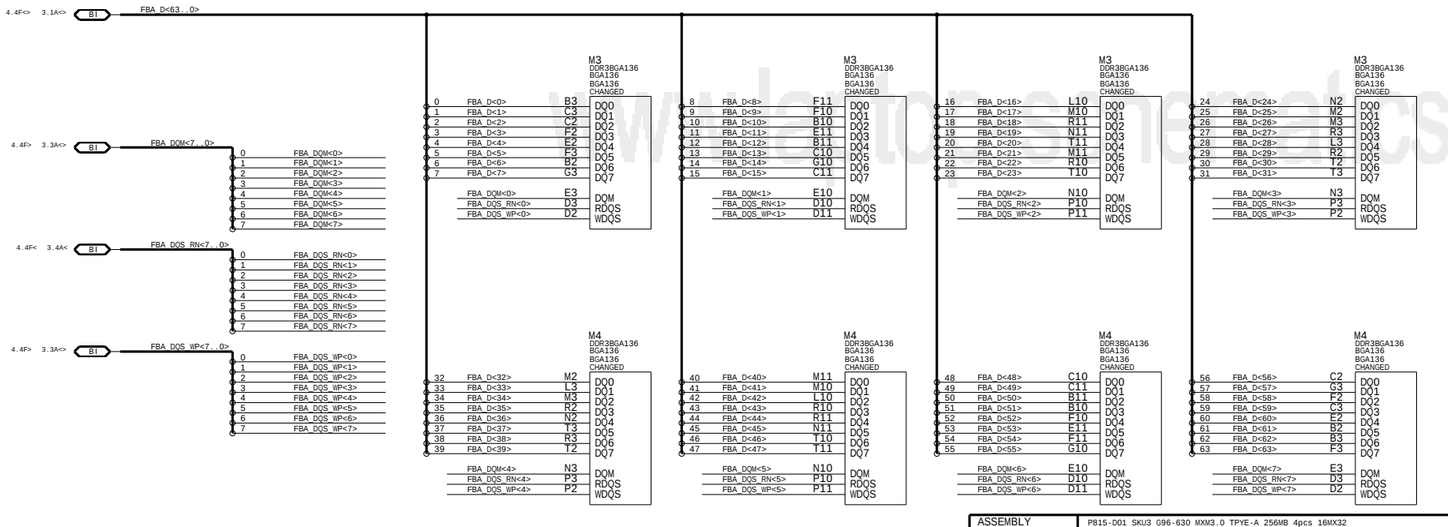
FRAME BUFFER PARTITION A



VREF	RTop	RBot	FBVDDQ	PERF MODE	GPIO10
0.77V	549	1k33 || 931	1.55V	Low	High
0.90V	549	1k32 || 931	1.8V	Low	High
1.09V	549	1k33	1.55V	High	Low
1.26V	549	1k33	1.8V	High	Low



NET RULES for FrameBuffer A

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBA_CLK0	1	80DIFF	FBA_CLK0
FBA_CLK0*	1	80DIFF	FBA_CLK0
FBA_CLK1	1	80DIFF	FBA_CLK1
FBA_CLK1*	1	80DIFF	FBA_CLK1

NET	NV_CRITICAL	NV_IMPEDANCE
FBA_DQS_WP<7..0>	1	40OHM
FBA_DQS_RN<7..0>	1	40OHM
FBA_DQM<7..0>	1	40OHM
FBA_D<63..0>	1	40OHM
FBA_CMD<27..0>	1	60OHM

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBA_VREF0	1.26V	0.02A	12MIL
FBA_VREF1	1.26V	0.02A	12MIL
FBA_VREF2	1.26V	0.02A	12MIL
FBA_VREF3	1.26V	0.02A	12MIL
FBA_ZQ0	1.26V	0.02A	12MIL
FBA_ZQ1	1.26V	0.02A	12MIL

ASSEMBLY	P815-D01 SKU3 G96-630 MXM3.0 TPYE-A 256MB 4pcs 16MX32
PAGE DETAIL	Frame Buffer Partition A Memories

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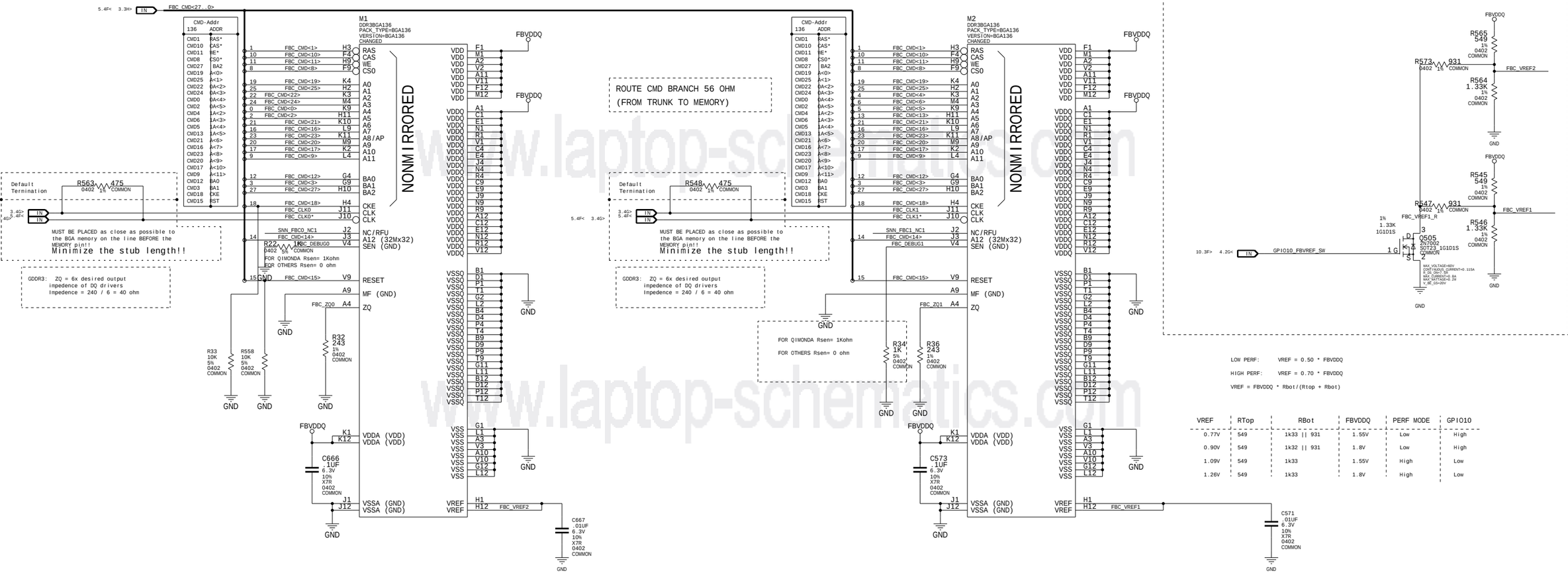
PAGE 5) MEMORY PARTITION C



VREF	RTop	RBot	FBVDDQ	PERF MODE	GPIO10
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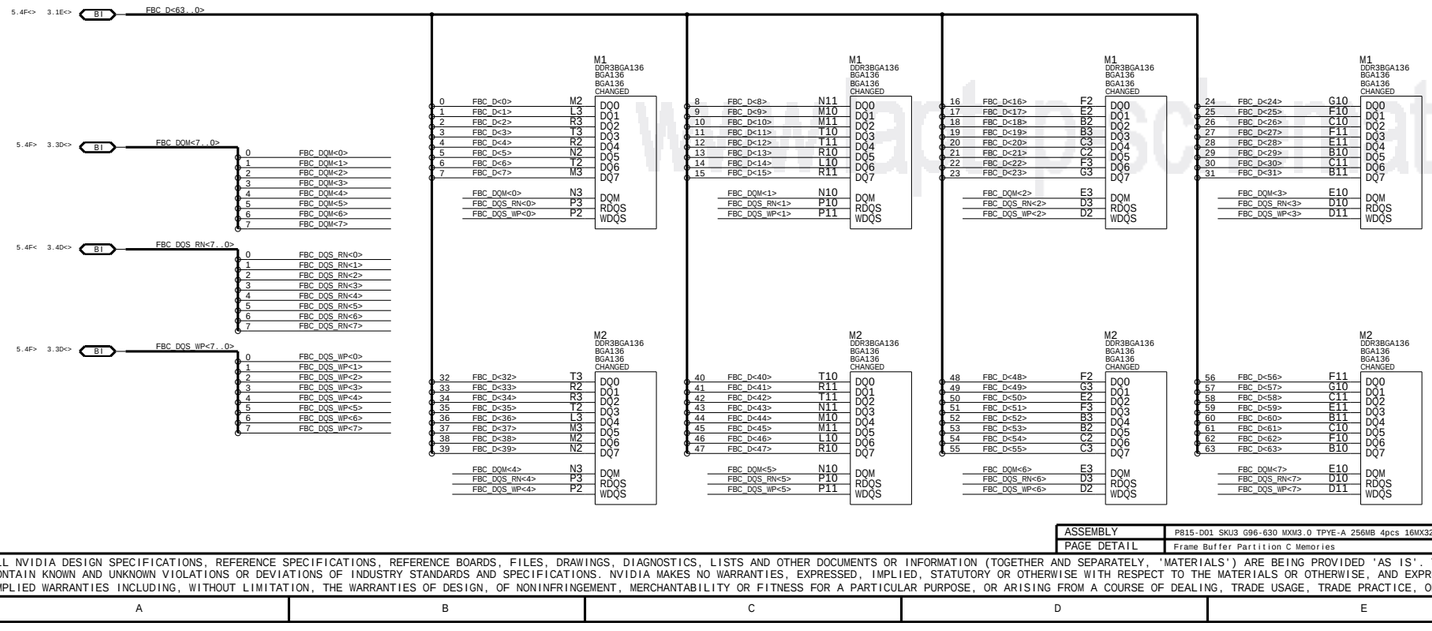
0.90V	549	1k32 || 931	1.8V	Low	High
1.09V	549	1k33	1.55V	High	Low
1.26V	549	1k33	1.8V	High	Low



NET RULES for FrameBuffer C

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBC_CLK0	1	80DIFF	FBC_CLK0
FBC_CLK0*	1	80DIFF	FBC_CLK0
FBC_CLK1	1	80DIFF	FBC_CLK1
FBC_CLK1*	1	80DIFF	FBC_CLK1
FBC_DQS_WP<7..0>	1	40OHM	
FBC_DQS_RN<7..0>	1	40OHM	
FBC_DQM<7..0>	1	40OHM	
FBC_D<63..0>	1	40OHM	
FBC_CMD<27..0>	1	60OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBC_VREF0	1.26V	0.02A	12MIL
FBC_VREF1	1.26V	0.02A	12MIL
FBC_VREF2	1.26V	0.02A	12MIL
FBC_VREF3	1.26V	0.02A	12MIL
FBC_ZQ0	1.26V	0.02A	12MIL
FBC_ZQ1	1.26V	0.02A	12MIL

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PAGE DETAIL	Frame Buffer Partition C Memories

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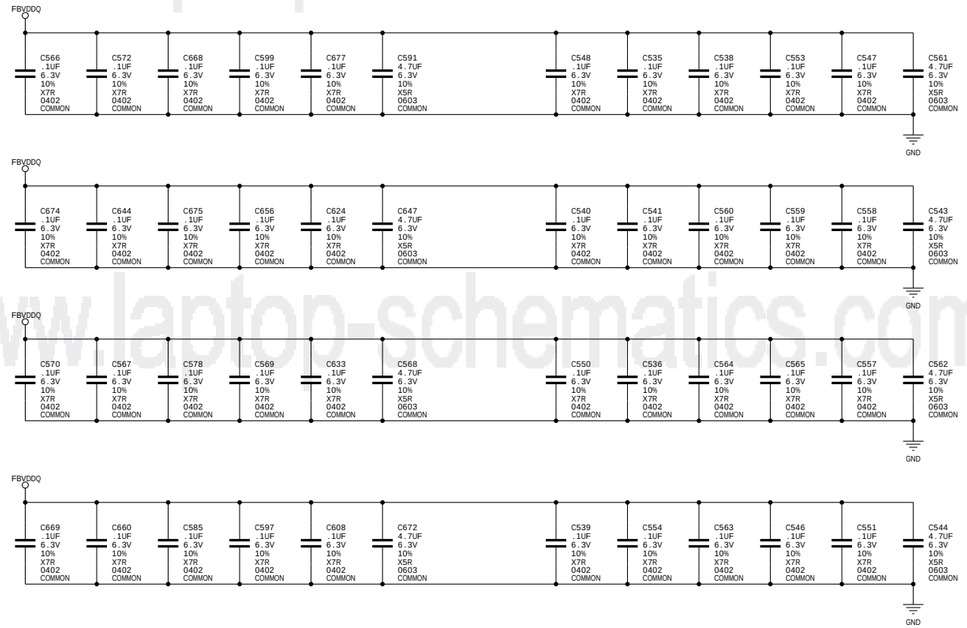
PAGE 6) MEMORY DECOUPLING CAPS

DECOUPLING CAPS FOR MEMORYS (PARTION A AND PARTION C)



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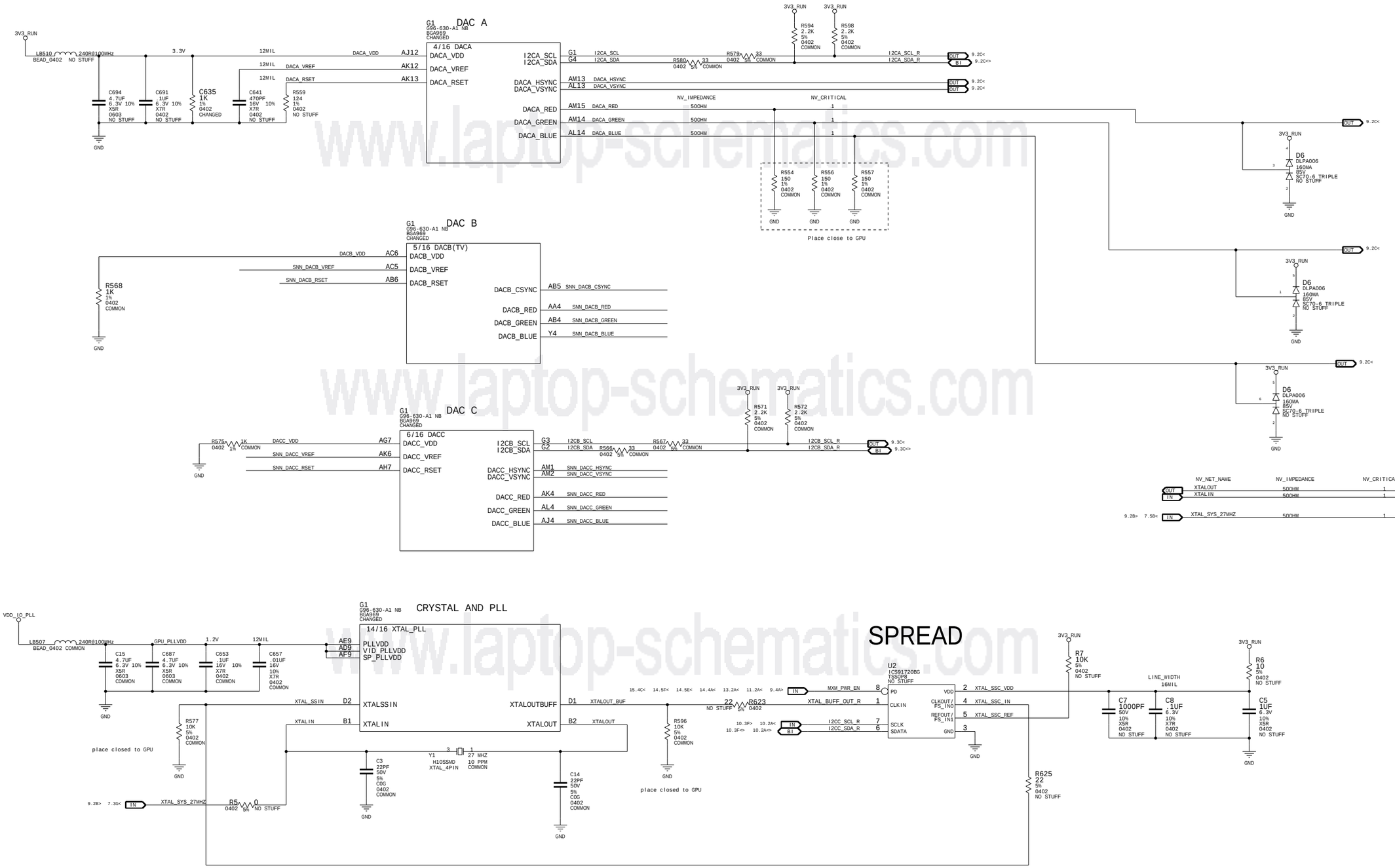
PAGE 7) DAC_A, DAC_B, DAC_C, PLL, CRYSTAL



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NV_NET_NAME	NV_IMPEDANCE	NV_CRITICAL_NET
XTALOUT	50OHM	1
XTALIN	50OHM	1
XTAL_SYS_27MHZ	50OHM	1

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PAGE DETAIL	DACs, Clock-Generation

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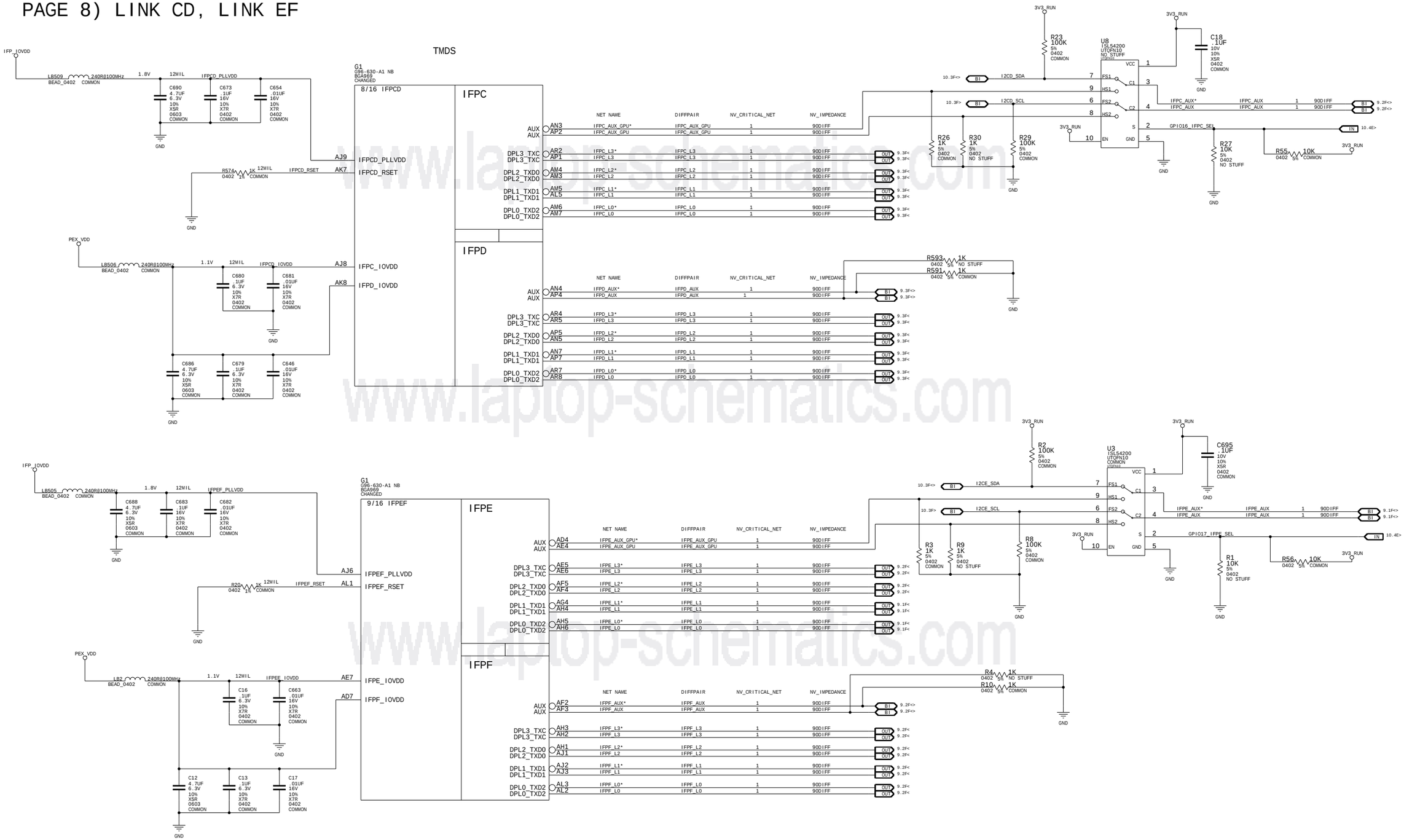
PAGE 8) LINK CD, LINK EF



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PAGE DETAIL	DP LINK C,D,E,F

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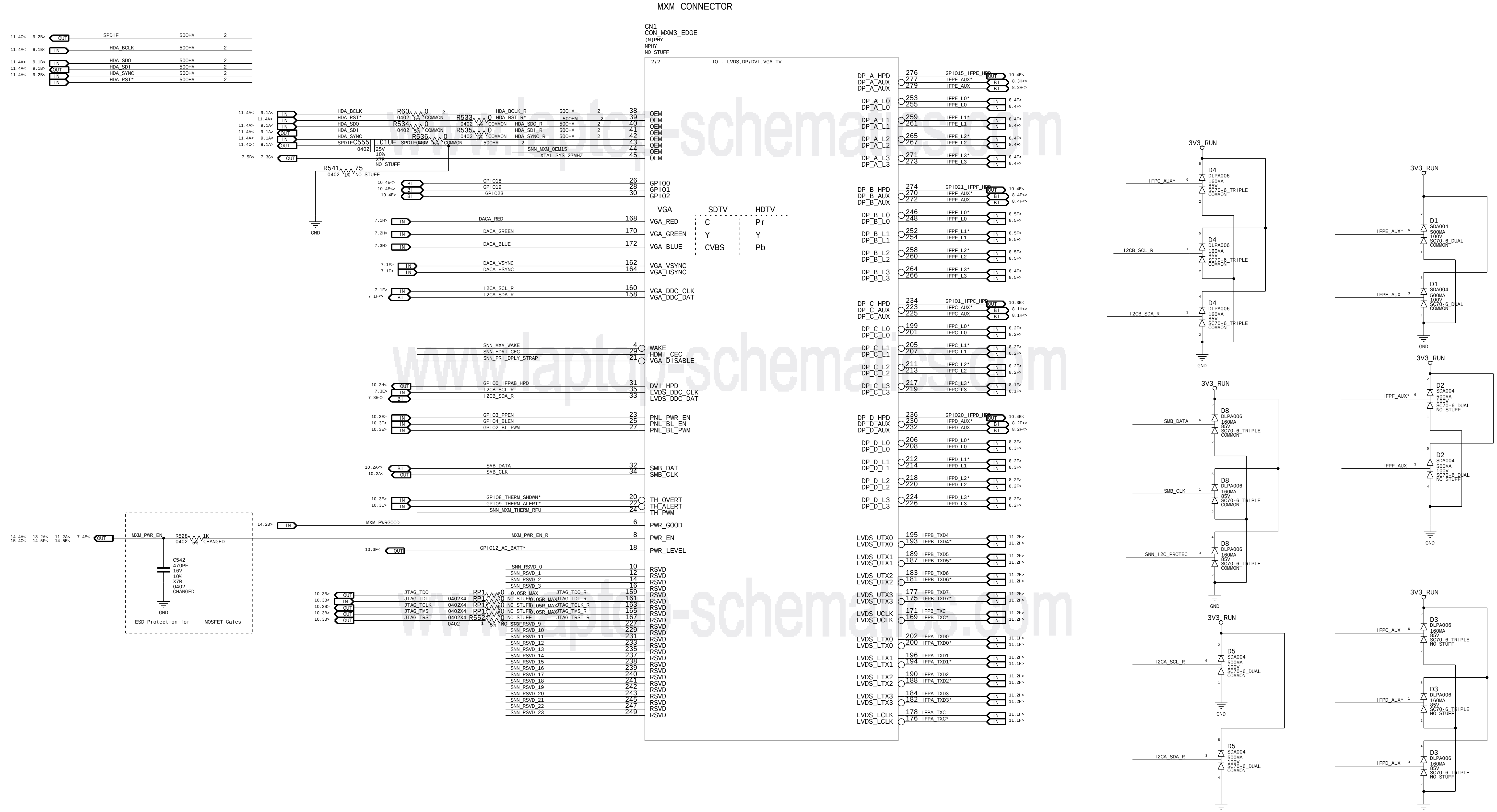
PAGE 9) MXM CONNECTOR



ASSEMBLY	P815-D01 SKU3 G96-630 MXM3.0 TPYE-A 256MB 4pcs 16MX32
PAGE DETAIL	MXM Connector, IO-Section

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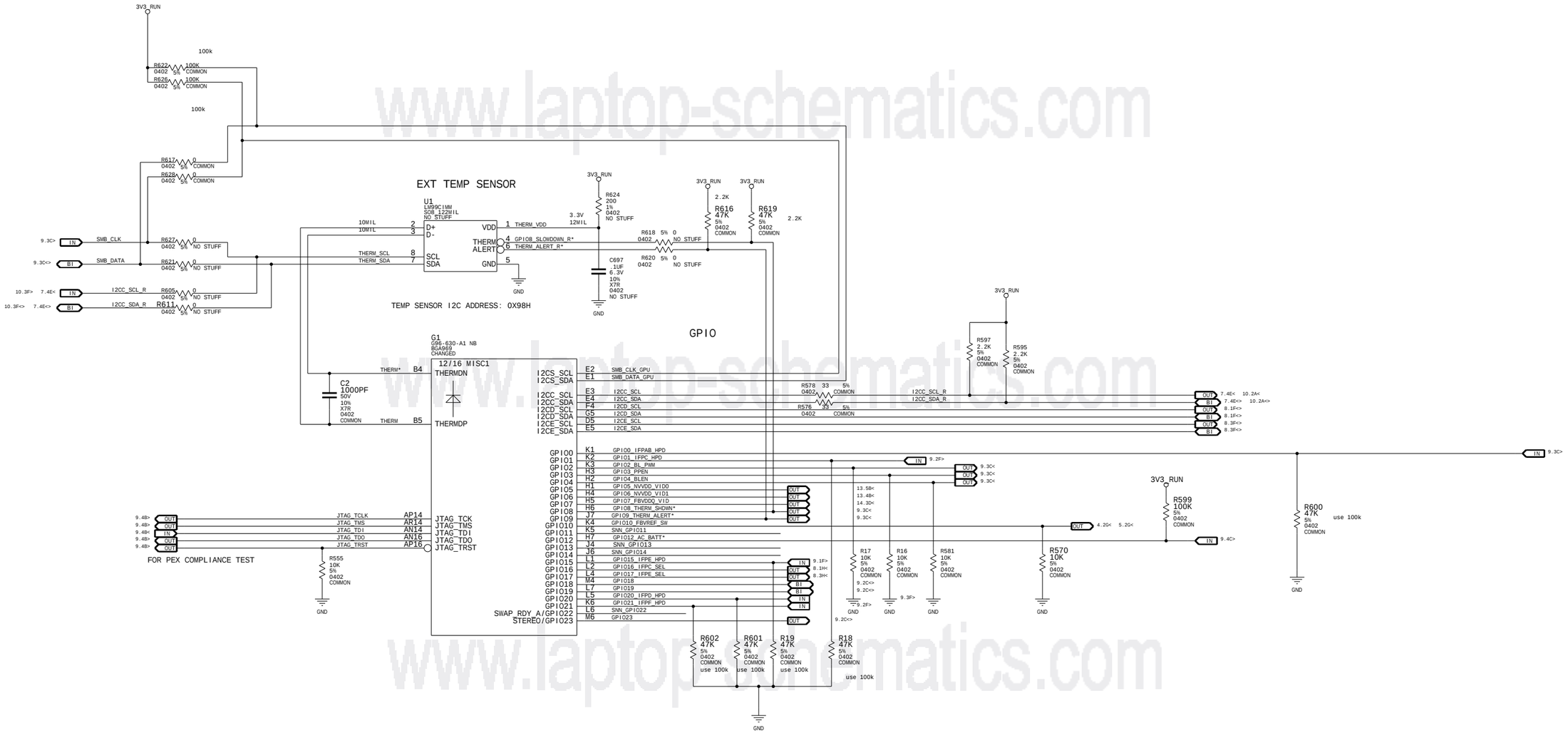
PAGE 10) GPIO, JTAG, TEMP SENSOR



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ASSEMBLY	P815-D01 SKU3 G96-630 MXM3.0 TPYE-A 256MB 4pcs 16MX32
PAGE DETAIL	GPIOs. JTAG, Thermal Senser

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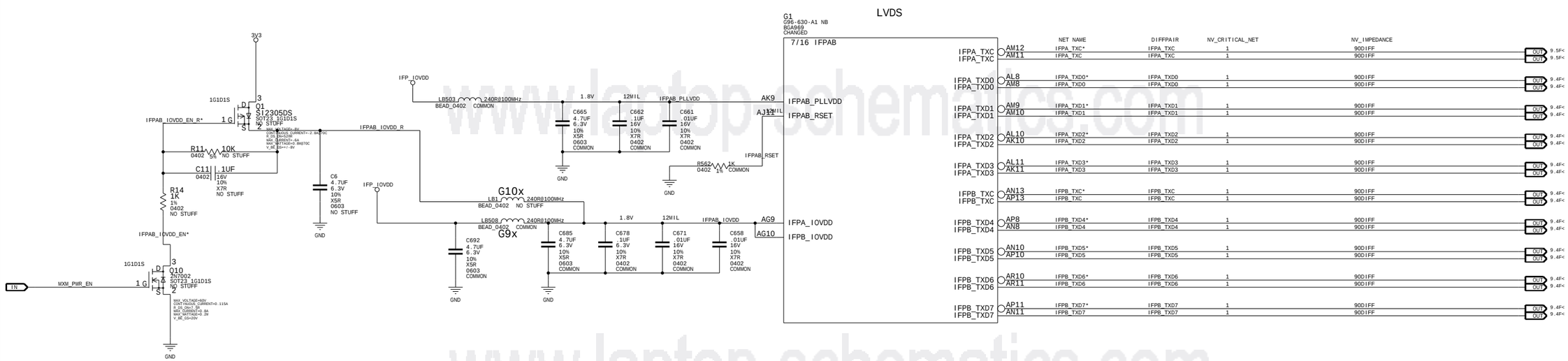
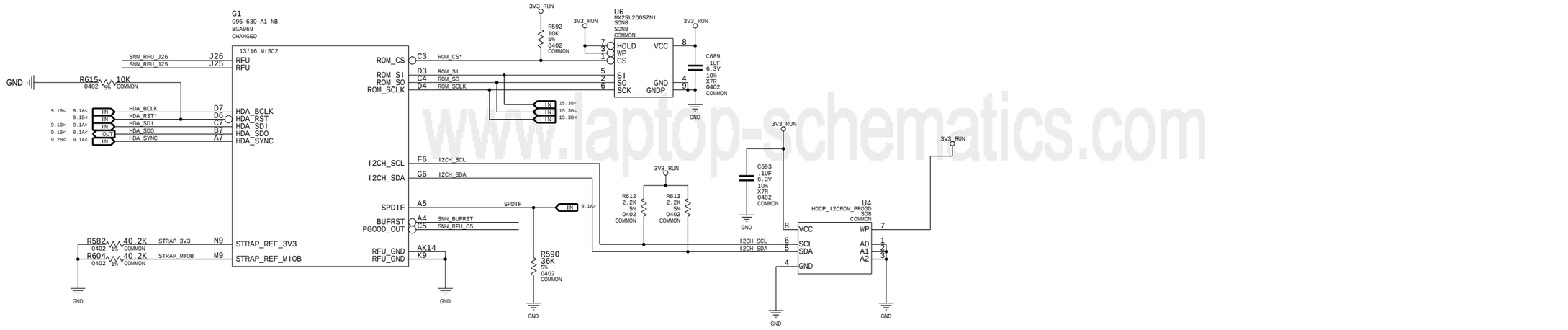
PAGE 11) LVDS, VBIOS, HDCP ROM

LVDS



VBIOS AND HDCP ROM



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PAGE DETAIL	LVDS, VBIOS and HDCP ROM

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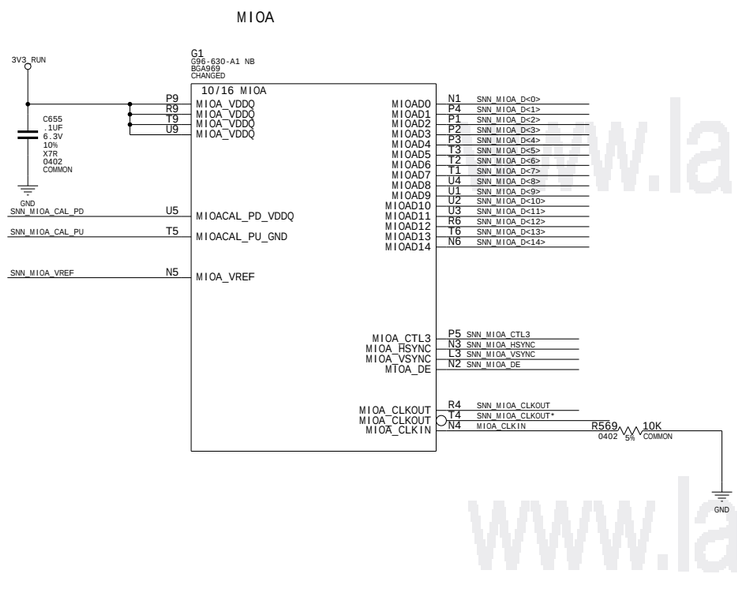
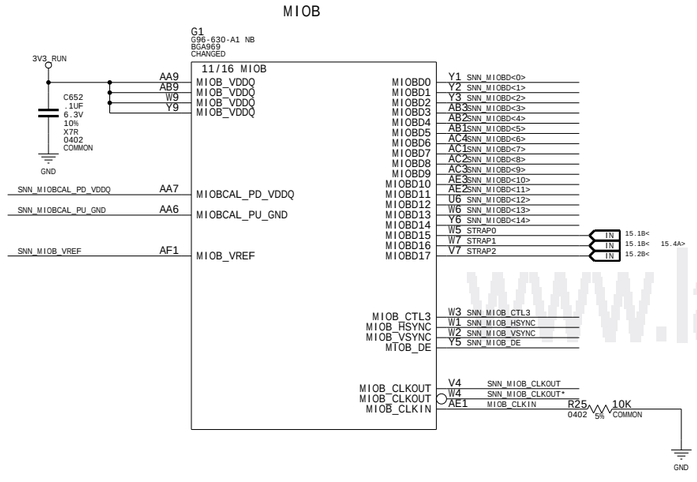
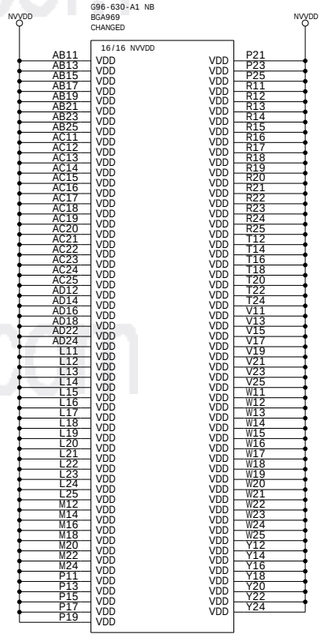
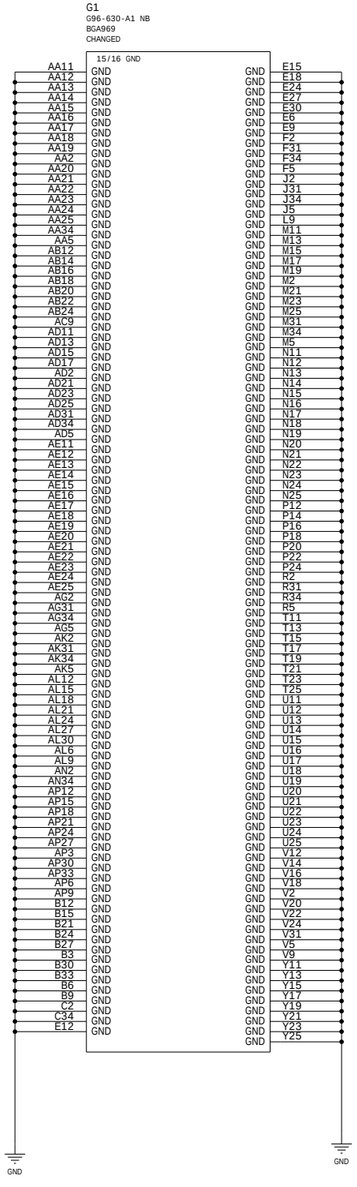
PAGE 12) MIOA(SLI), MIOB, GPU GND,









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PAGE DETAIL	MIOA, MIOB, GPU GND

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PAGE 13) NVVDD POWER SUPPLY

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
NVVDD	1V	12MIL	30A

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PAGE DETAIL	NVVDD Power Supply

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PAGE 14) FBVDDQ AND PEX1V2 POWER SUPPLY

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
PEX_VDD	1.2V	12MIL	3.48A
FBVDDQ	1.8V	12MIL	10A
PS_VIN_PEX		12MIL	

FBVDDQ=1.8V
APPROX. 5A @ 400KHZ
INPUT CURRENT RMS = 2.15A @ 7.5V INPUT
OUTPUT PEAK TO PEAK CURRENT = 1.51A @ 22V INPUT
SWITCHING FREQ = 500KHZ

U10 ISL6269ACRZ VR_Sb=0.6V MLFP16 COMMON

D502 BAT43 SOD323 40V 400MA NO STUFF

300-0309-000 can be the alternative

CONNECT TO R-TOP

place close to the inductor

Vout = Vref * (1 + Rtop / Rbot)
1.805V = 0.6V * (1 + 3.09K/(1.96K||7.15K))
1.546V = 0.6V * (1 + 3.09K/1.96K)

stuff for NCP5212

PEXVDD = 1.1V @ 4A
Vout = Vref * (1+R1/R2)
1.10V = 0.8V * (1+324K/866K)

U9 MP38115 VR=0.8V DFN10 COMMON

STUFF FOR G10x

STUFF FOR G9x (NO DYNAMIC FBVDDQ)

3V3_RUN

U5 UP7707M5-18 FIXED 1.8V SOT23-5 CHANGED

STUFF REGULATOR FOR G9x (WITH DYNAMIC FBVDDQ)

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PAGE DETAIL	FBVDDQ, PEX1V2 and IPF_VDD Power Supply

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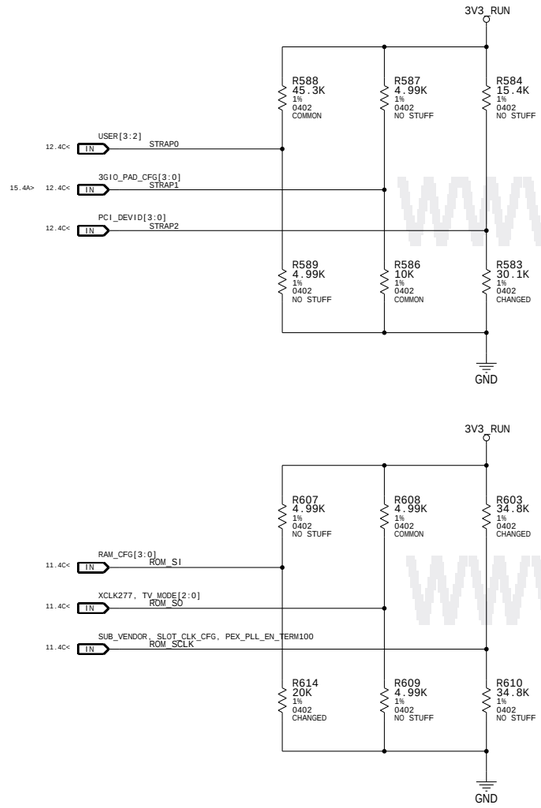
PAGE 15) STRAPS, MOUNTING HOLES



	3V3	GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

STRAP0

- USER_BIT0
- USER_BIT1
- USER_BIT2
- USER_BIT3

0xF: 45K PU (unused)

STRAP1

- 3GIO_PADCFG_LUT_ADR0
- 3GIO_PADCFG_LUT_ADR1
- 3GIO_PADCFG_LUT_ADR2
- 3GIO_PADCFG_LUT_ADR3

0x0: Desktop default (normal swing) - 5k PD
0x1: Mobile default (low swing) - 10k PD
acc. to //hw/tesla_g98b/manuals/dev_ext_devices.ref

STRAP2

- PCI_DEVID_0
- PCI_DEVID_1
- PCI_DEVID_2
- PCI_DEVID_3

all 4 bits set by HW strapping
0x064A: 15K PU (NB9E-GE)

ROM_SO

- TV_MODE_BIT0
- TV_MODE_BIT1
- TV_MODE_BIT2

0x0: NTSC-M
5K PU

- XCLK_277

1: PCI-E GEN2

ROM_SI

- RAM_CFG_0
- RAM_CFG_1
- RAM_CFG_2
- RAM_CFG_3

256 MB (4pcs. 16Mx32)

RAM_CFG[3:0]	Definitions
0000	Reserved
0001	Qimonda
0010	Hynix
0011	Samsung

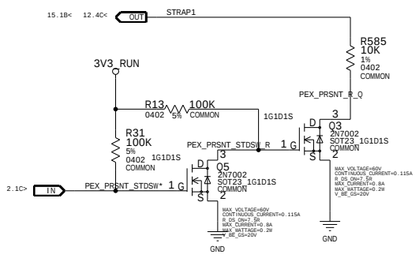
512 MB (4pcs. 32Mx32)

RAM_CFG[3:0]		Definitions
0100	25k PD	Reserved
0101	30k PD	Qimonda
0110	35k PD	Hynix
0111	45k PD	Samsung

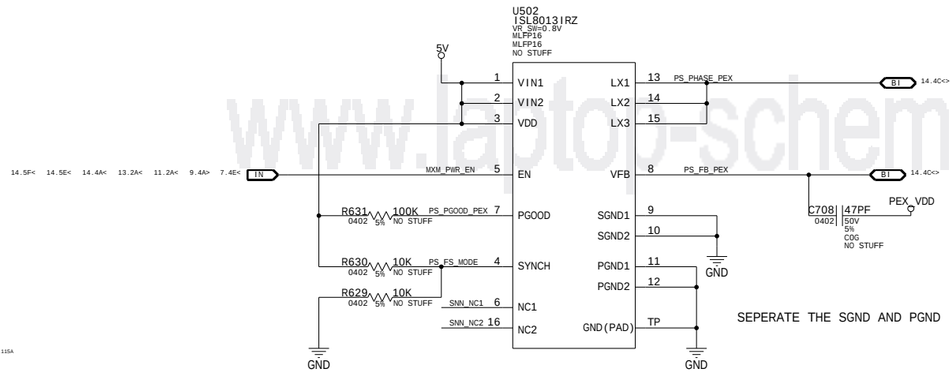
ROM_SCLK

- PCI_DEVID_EXT — 0:
- SUB_VENDOR — 1: SUB_VENDOR BIOS (30K PD)
- SLOT_CLK_CONFIG — 1:
- PEX_PLL_EN_TERM100 — 1: TERM100 ENABLED

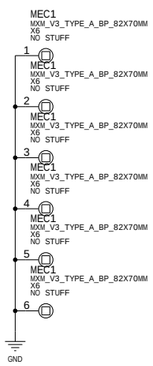
PEX_PADCFG



PEX_PRSNT_R*	R_STRAP1	3_GIO_PADCFG_LUT<3..0>
FLOAT	10k	0x1 MOBILE_DEFAULT
GND	5k (10k ll 10k)	0x0 DESKTOP_DEFAULT



SEPERATE THE SGND AND PGND



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