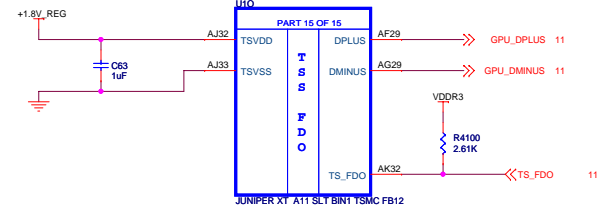
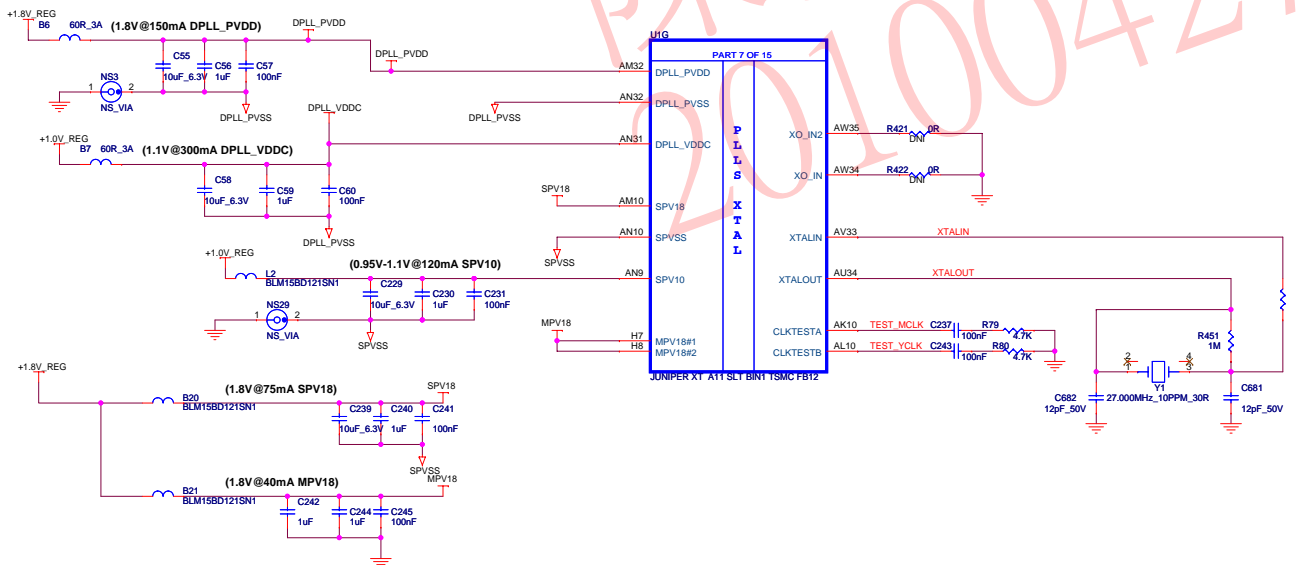


PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC



A 256MB MEMORY APERTURE SIZE CAN BE DEFINED USING A SEPARATE ROM OR STRAPPING  
A 256MB MEMORY APERTURE SIZE CAN BE DEFINED USING A SEPARATE ROM OR STRAPPING

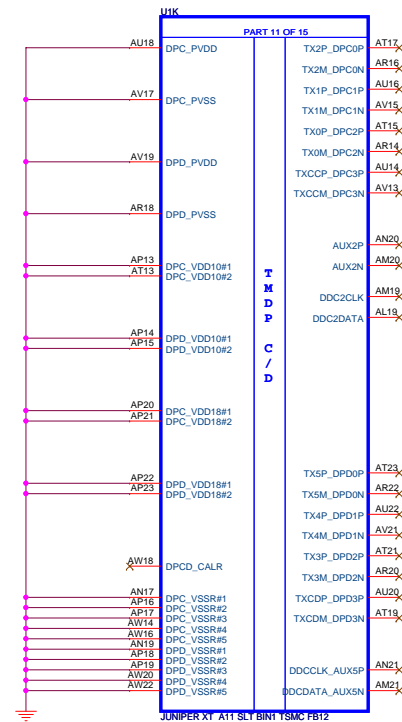
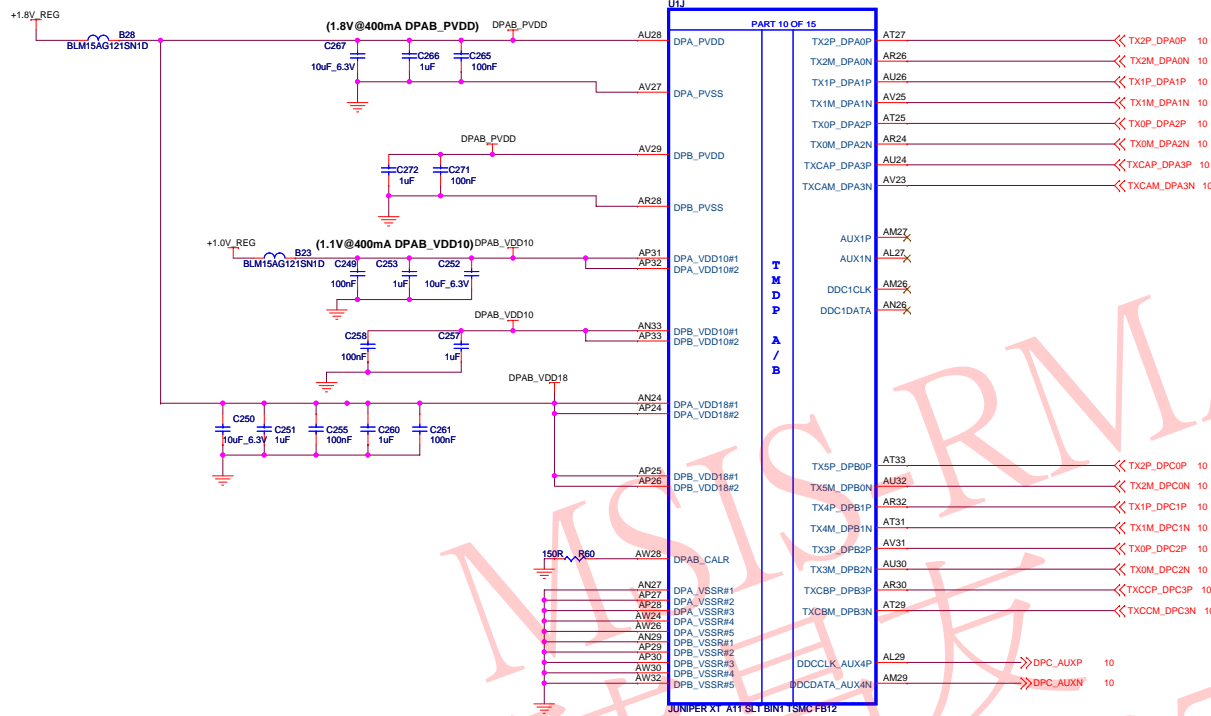
**SERIAL EEPROM 512K/1M**

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Title: RH Redwood/ Broadway M2 package MXM3.0 DDR3  
Doc No: 105-C076XX-00B



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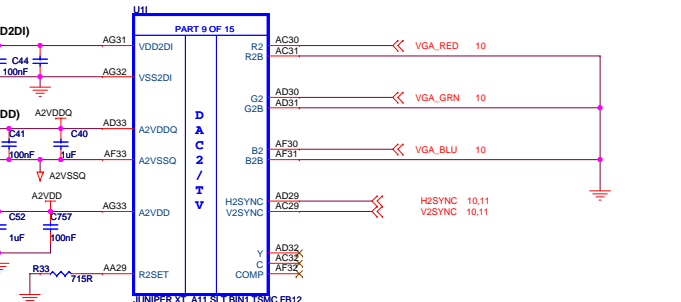
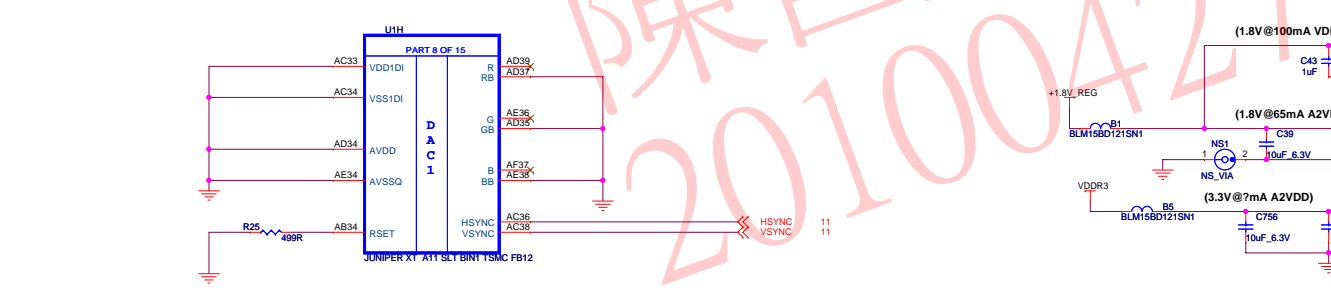
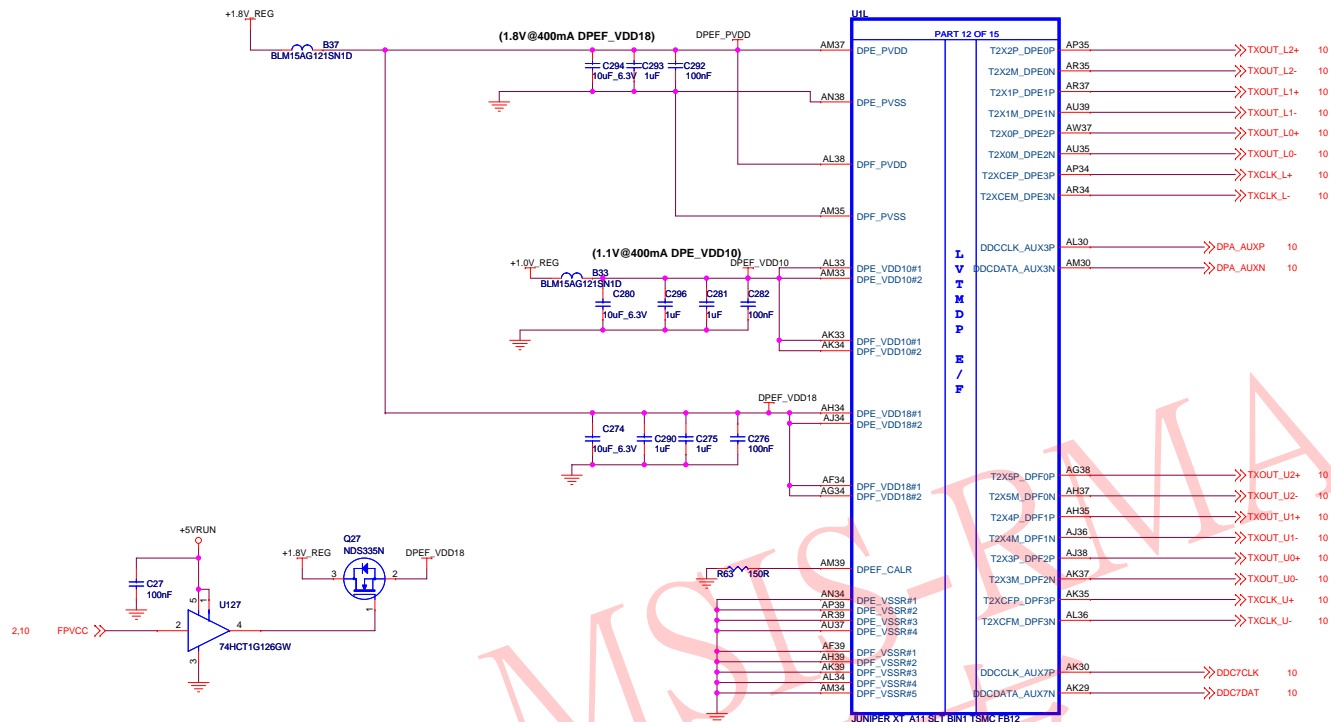
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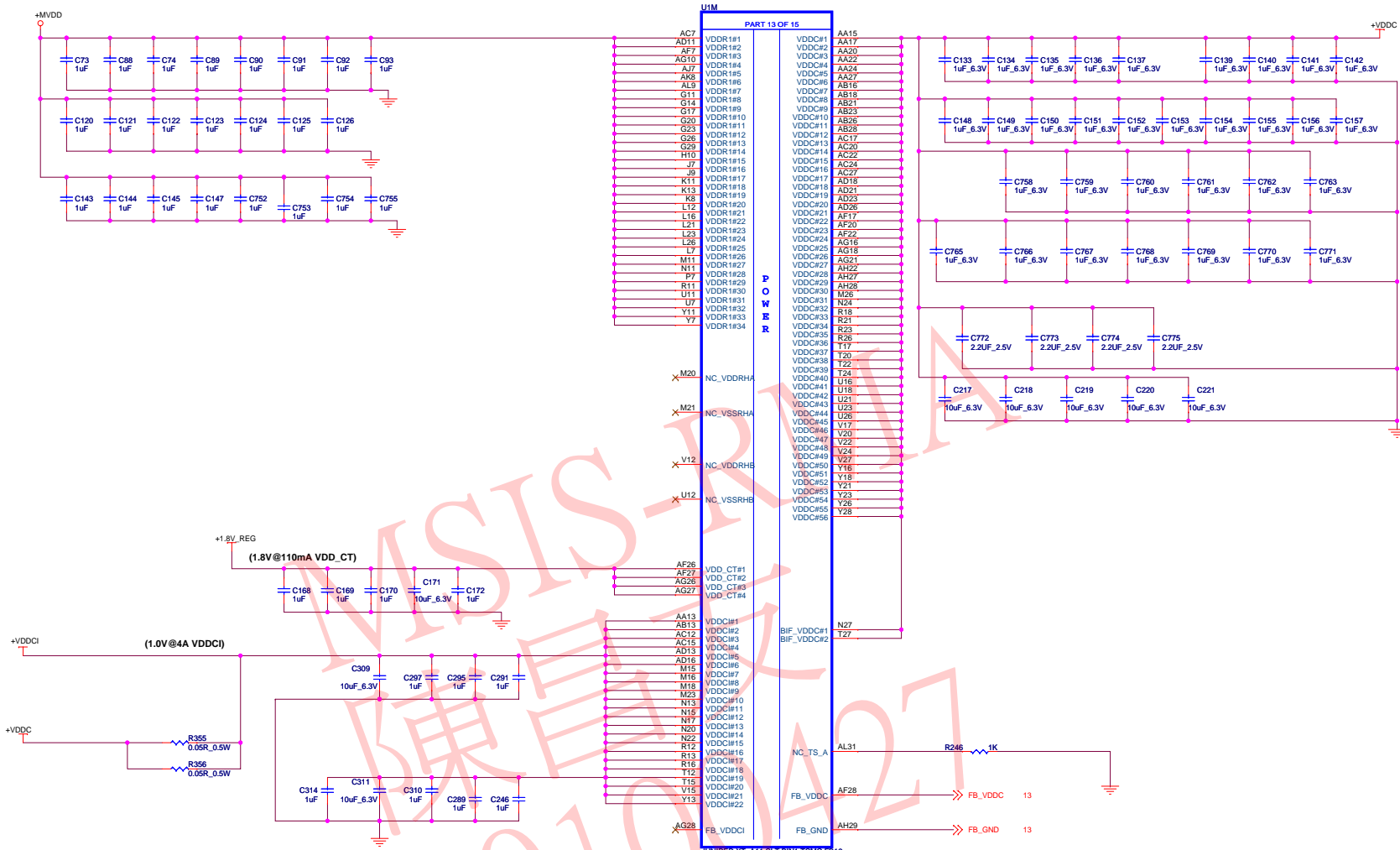
Date: Monday, December 07, 2009 Rev 0

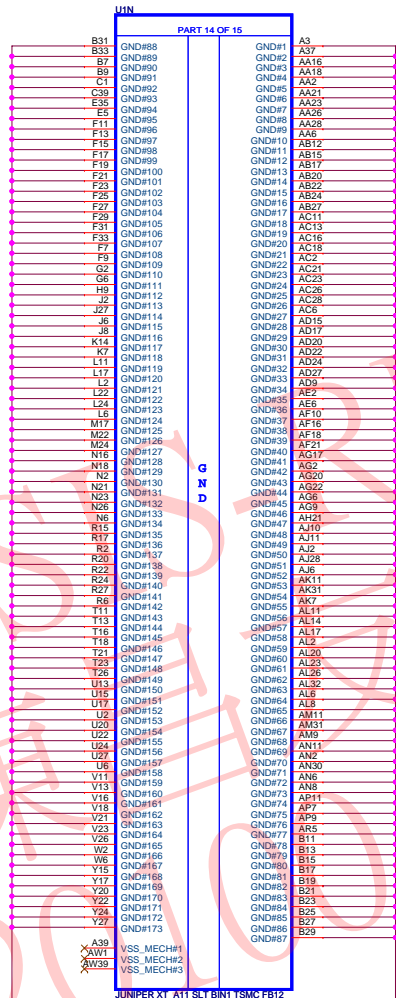
Sheet 3 of 16

Title RH Redwood/ Broadway M2 package MXM3.0 DDR3 Doc No. 105-C076XX-00B










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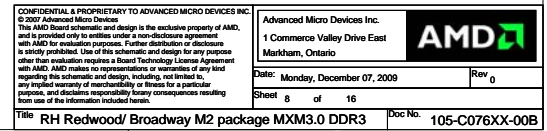
The schematic diagram illustrates the electrical connections for the 100-BALL SDRAM D0R3 (29F2238T/MNG8). The central pinout table lists the following signals and their corresponding pins:

Signal	Pin	Signal	Pin
QSA1	C7	VDDQIH9	H9
DOMA#3	D3	VSSIA9	A9
DOMA#3	D3	VSSIB3	E1
QSA#3	G3	VSSIF1	F1
QSA#1	B7	VSSIG8	G8
		VSSIJ2	J2
		VSSK4	K4
		VSSL8	L8
		VSSM1	M1
		VSSN9	N9
		VSSP1	P1
		VSSP9	P9
		VSSR1	R1
		VSSR9	R9
		VSSS1	S1
		VSSS9	S9
		VSST1	T1
		VSST9	T9
		VSSQB1	B1
		VSSQB9	B9
		VSSQD1	D1
		VSSQD8	D8
		VSSQE2	E2
		VSSQE8	E8
		VSSQF8	F8
		VSSQF9	F9
		VSSQG1	G1
		VSSQG9	G9

Additional connections shown include:

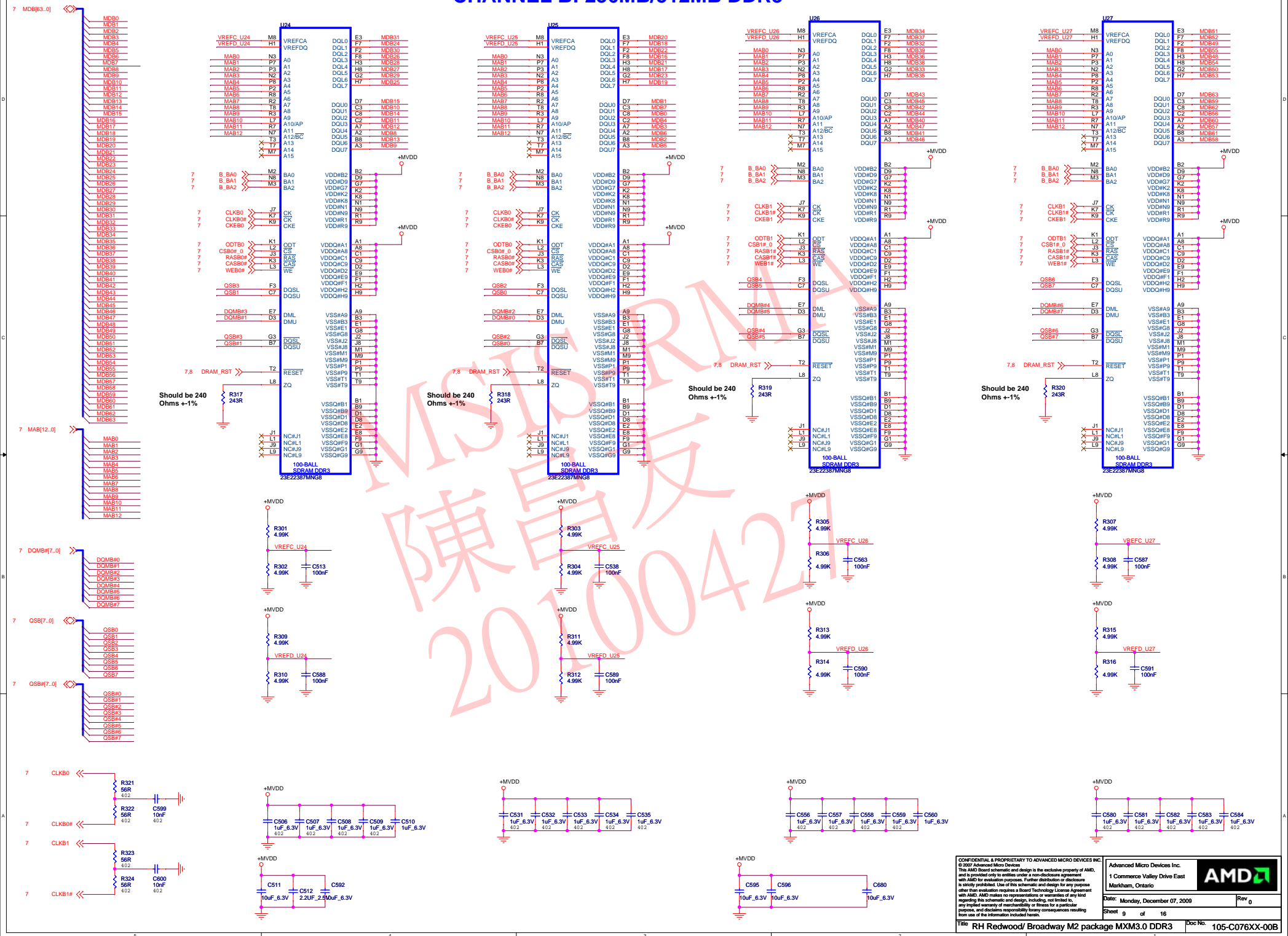
- DRAM\_RST** (7.9 Ohms  $\pm 1\%$ ) connected to pin T2 and L8.
- RESET** connected to pin T2 and L8.
- ZQ** connected to pin L8.
- VDD** connected to pins B1, B9, D1, D8, E2, E8, F8, F9, G1, G9, S1, S9, T1, T9.
- VREFC** connected to pins L1, L9, N1, N9, R1, R9, S1, S9, T1, T9.
- VREFD** connected to pins L1, L9, N1, N9, R1, R9, S1, S9, T1, T9.

The diagram also shows the internal structure of the SDRAM, including the 100-BALL SDRAM D0R3 (29F2238T/MNG8) and the 100-BALL SDRAM D0R3 (29F2238T/MNG8).

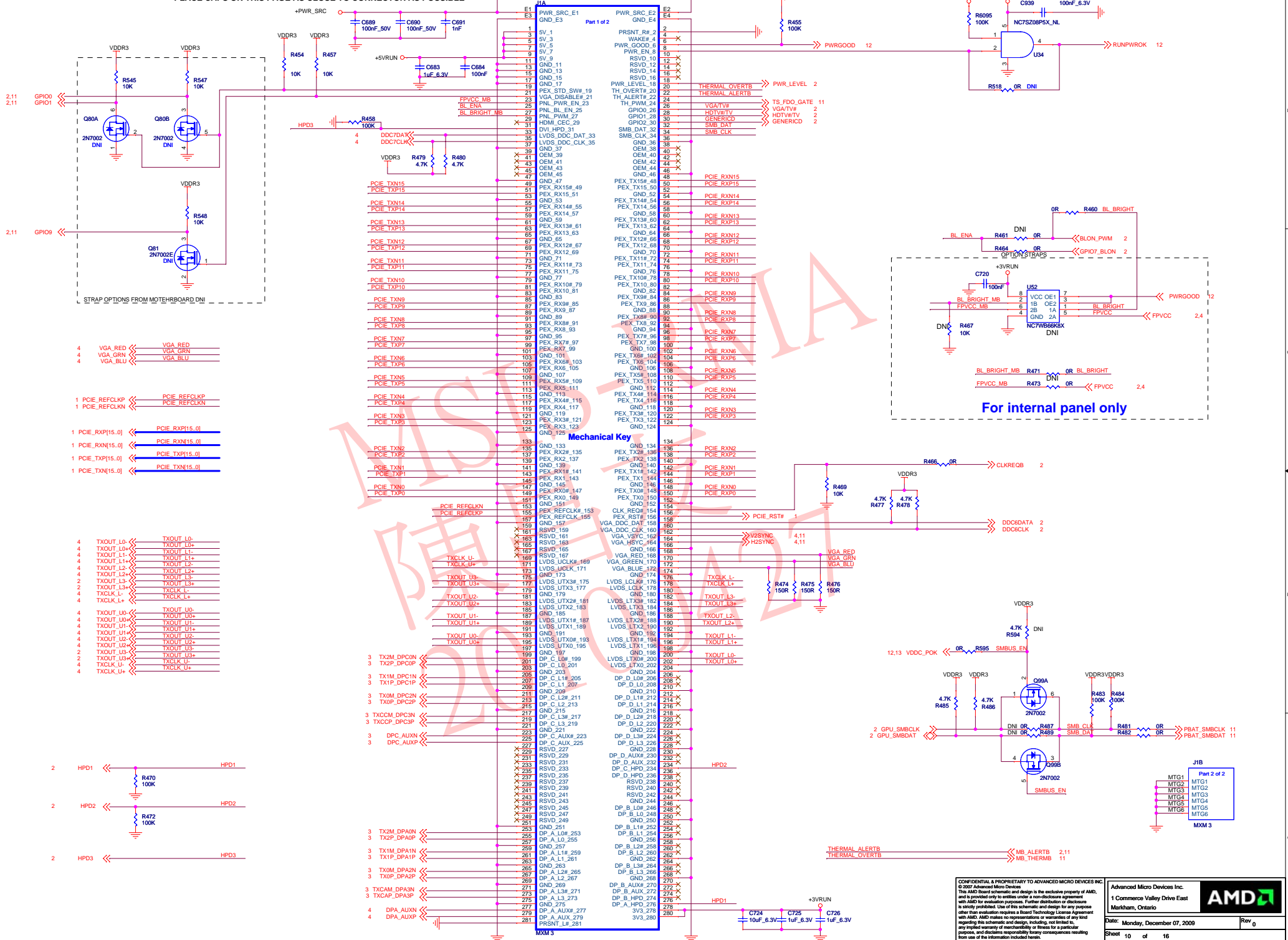




# CHANNEL B: 256MB/512MB DDR3




PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE

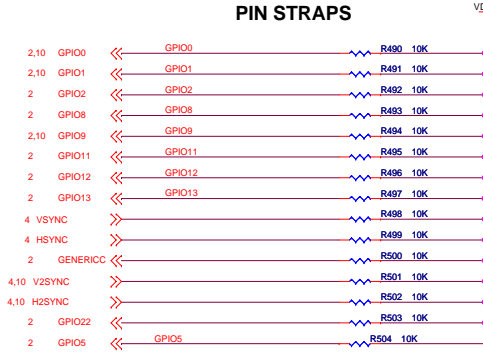


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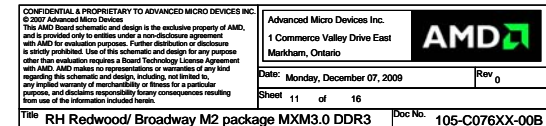
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<p>Date: Monday, December 07, 2009</p>		<p>Rev 0</p>	

Title	RH Redwood/ Broadway M2 package MXM3.0 DDR3	Doc No.	105-C076XX-00B
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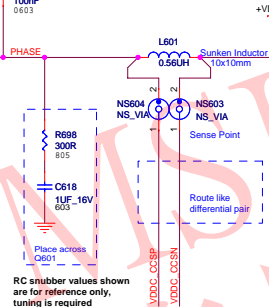
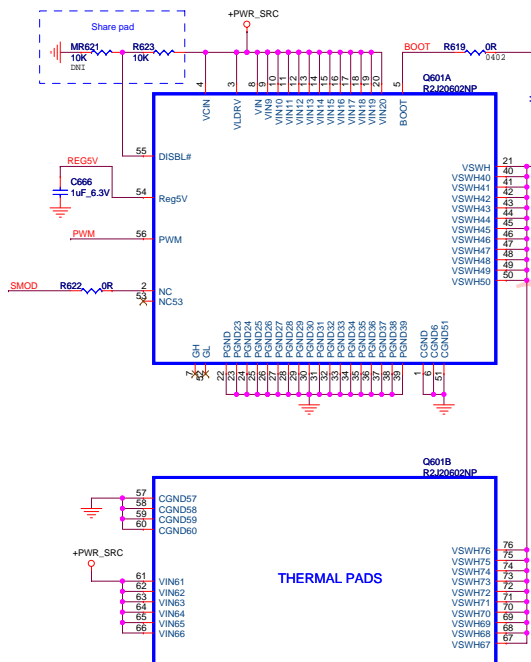
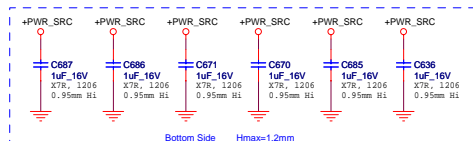
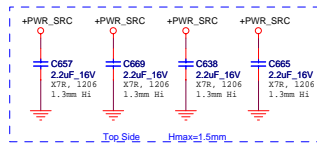
<h2 style="text-align: center;">AMD RESERVED CONFIGURATION STRAPS</h2> <p style="text-align: center;"><b>ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</b></p>	
H2SYNC	GENERICC
<p style="text-align: center;"><b>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</b></p>	
GPIO_28_TD0	GPIO21_BB_EN

### Critical Temperature Fault



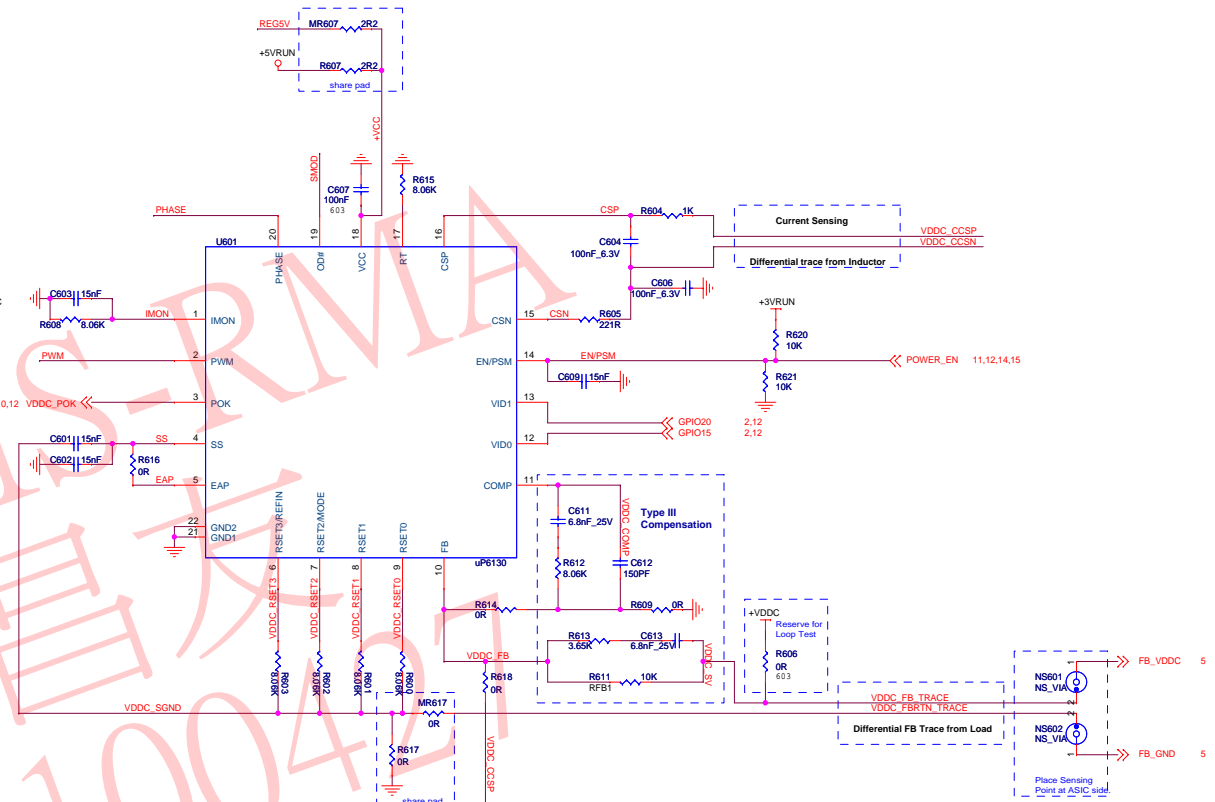
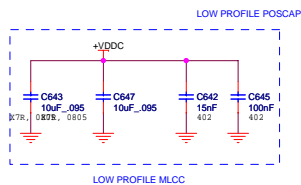
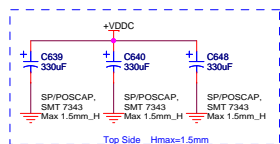


# INPUT CAP



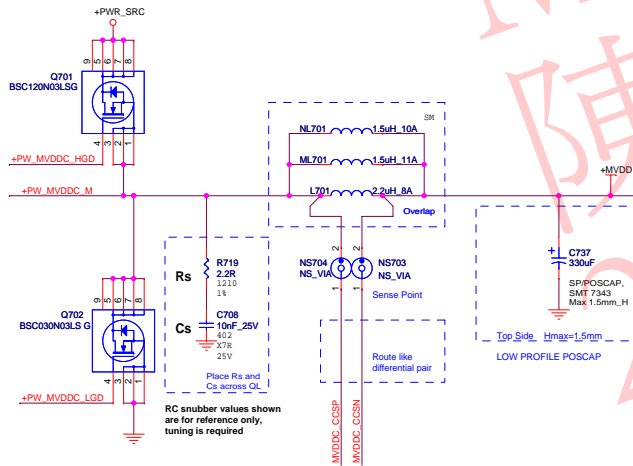
Pin	Difference Between R2J2062NP and R2J2065NP
3	VLDIV
8	VIN
2	NC
53	NC


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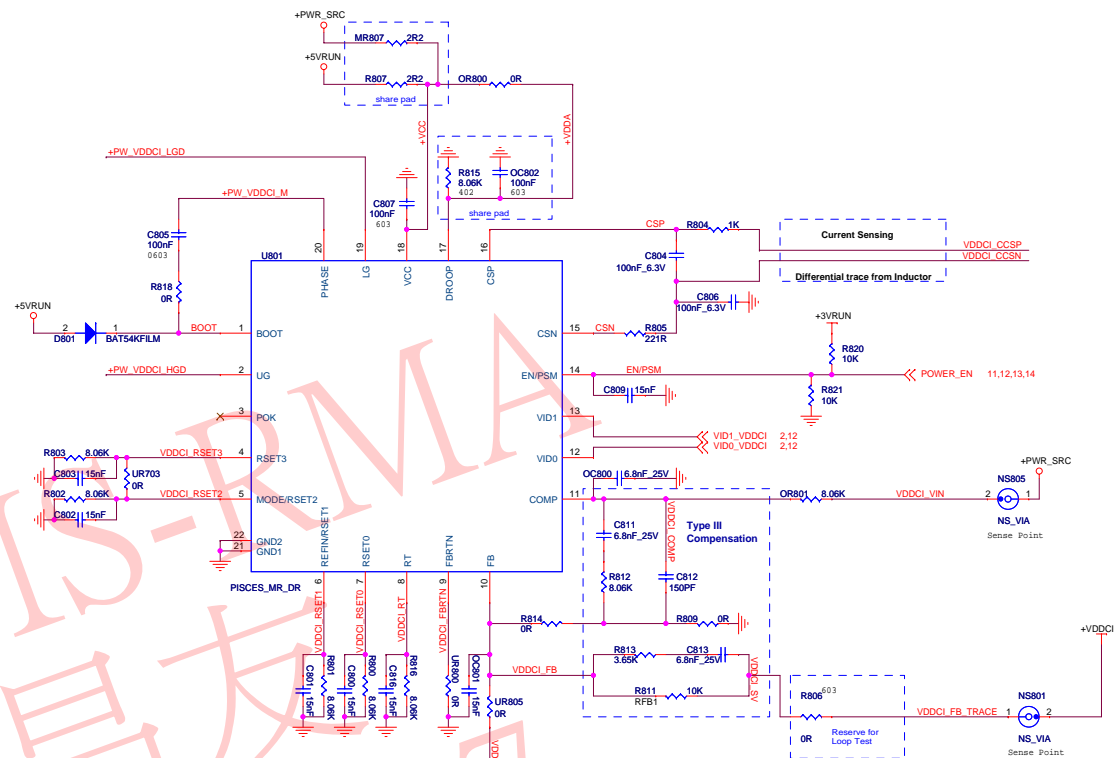
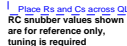
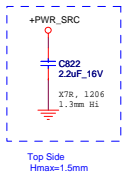



The diagram illustrates the power plane layout, divided into a Top Side and a Bottom Side. The Top Side features four capacitors (C721, C732, C729, C731) connected to PWR\_SRC and GND, with dimensions Hmax=1.5mm. The Bottom Side features two capacitors (C730, C733) connected to PWR\_SRC and GND, with dimensions Hmax=1.2mm.

Capacitor	Value	Part Number	Dimensions
C721	2.2uF, 16V	X7R, 1206	1.3mm H
C732	2.2uF, 16V	X7R, 1206	1.3mm H
C729	2.2uF, 16V	X7R, 1206	1.3mm H
C731	2.2uF, 16V	X7R, 1206	1.3mm H
C730	1uF, 16V	X7R, 1206	0.95mm H
C733	1uF, 16V	X7R, 1206	0.95mm H



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<div>AMD</div>			Title		Schematic No.	Date:	
			RH Redwood/ Broadway M2 package MXM3.0 DDR3		105-C076XX-00B	Monday, December 07, 2009	
			REVISION HISTORY				Rev 0
			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.				
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION				
0	00A	09/27/09	Create new SCHs				
	00B	12/03/09	Added PWR_EN short to DrMOS Added DrMOS Thermal Pad				
			<div>MSIS-RMA</div> <div>陳昌友</div> <div>20100427</div>				