P402-A02 DESIGN -- G84/G86, 600/700 128/256 MB DDR3, VGA, DVI-I, SD/HDTV

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10402-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10402-0000-200	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
2	SKU0010	600-10402-0010-200	G86-400-500/700Mhz 256/128 MB 16Mx32 BGA135 GDDR3 DVI+VGA_HDTV-Out
3	SKU0500	600-50402-0500-200	G84-875, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
4	SKU9100	600-10402-9100-200	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

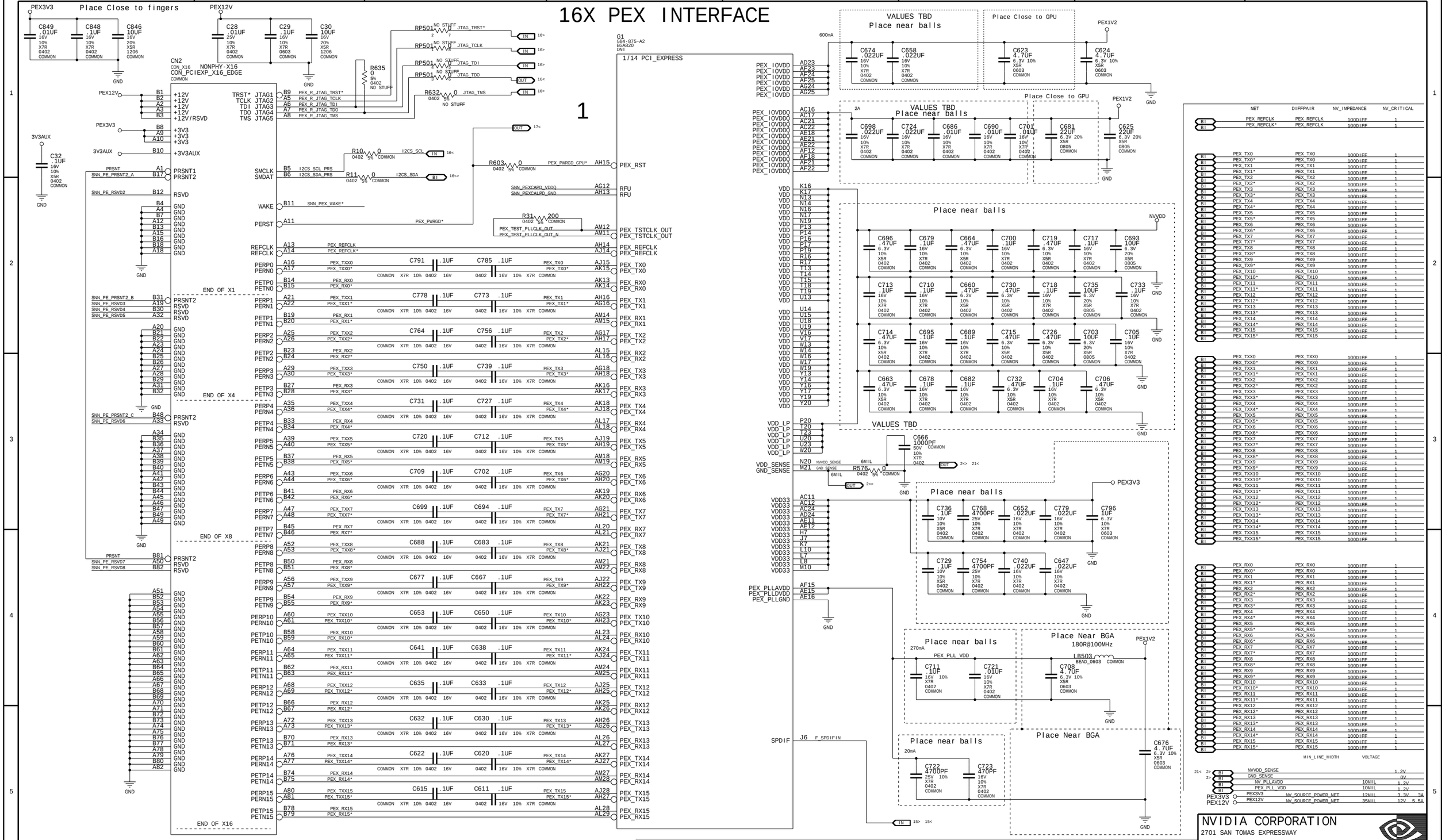
PAGE SUMMARY:

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	TABLE OF CONTENTS & REVISION HISTORY

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10402-0000-200 C		
ID	p402	PAGE	1 OF 21
NAME	broth	DATE	22-FEB-2007

16X PEX INTERFACE



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	PCI EXPRESS 16X, NVVDD DECOUPLING CAPS,PEX_IOVDD/Q DECOUPLING CAPS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10402-0000-200 C		
ID	p402	PAGE	2 OF 21
NAME	broth	DATE	22-FEB-2007

G1
G84-875-A2
BGA820
DN1

2/14 FBA

0	FBAD<0>	N27	FBAD0
1	FBAD<1>	M27	FBAD1
2	FBAD<2>	N28	FBAD2
3	FBAD<3>	L29	FBAD3
4	FBAD<4>	K27	FBAD4
5	FBAD<5>	K28	FBAD5
6	FBAD<6>	J29	FBAD6
7	FBAD<7>	J28	FBAD7
8	FBAD<8>	P30	FBAD8
9	FBAD<9>	N31	FBAD9
10	FBAD<10>	N30	FBAD10
11	FBAD<11>	N32	FBAD11
12	FBAD<12>	L31	FBAD12
13	FBAD<13>	L30	FBAD13
14	FBAD<14>	J30	FBAD14
15	FBAD<15>	L32	FBAD15
16	FBAD<16>	H30	FBAD16
17	FBAD<17>	K30	FBAD17
18	FBAD<18>	H31	FBAD18
19	FBAD<19>	F30	FBAD19
20	FBAD<20>	H32	FBAD20
21	FBAD<21>	E31	FBAD21
22	FBAD<22>	D30	FBAD22
23	FBAD<23>	E30	FBAD23
24	FBAD<24>	H28	FBAD24
25	FBAD<25>	H29	FBAD25
26	FBAD<26>	E29	FBAD26
27	FBAD<27>	J27	FBAD27
28	FBAD<28>	F27	FBAD28
29	FBAD<29>	E27	FBAD29
30	FBAD<30>	E28	FBAD30
31	FBAD<31>	F28	FBAD31
32	FBAD<32>	AD29	FBAD32
33	FBAD<33>	AE29	FBAD33
34	FBAD<34>	AD28	FBAD34
35	FBAD<35>	AC28	FBAD35
36	FBAD<36>	AB29	FBAD36
37	FBAD<37>	AA30	FBAD37
38	FBAD<38>	Y28	FBAD38
39	FBAD<39>	AB30	FBAD39
40	FBAD<40>	AM30	FBAD40
41	FBAD<41>	AF30	FBAD41
42	FBAD<42>	AJ31	FBAD42
43	FBAD<43>	AJ30	FBAD43
44	FBAD<44>	AJ32	FBAD44
45	FBAD<45>	AK29	FBAD45
46	FBAD<46>	AM31	FBAD46
47	FBAD<47>	AL30	FBAD47
48	FBAD<48>	AE32	FBAD48
49	FBAD<49>	AE30	FBAD49
50	FBAD<50>	AE31	FBAD50
51	FBAD<51>	AD30	FBAD51
52	FBAD<52>	AC31	FBAD52
53	FBAD<53>	AC32	FBAD53
54	FBAD<54>	AB32	FBAD54
55	FBAD<55>	AB31	FBAD55
56	FBAD<56>	AG27	FBAD56
57	FBAD<57>	AF28	FBAD57
58	FBAD<58>	AH28	FBAD58
59	FBAD<59>	AG28	FBAD59
60	FBAD<60>	AG29	FBAD60
61	FBAD<61>	AD27	FBAD61
62	FBAD<62>	AF27	FBAD62
63	FBAD<63>	AE28	FBAD63

4<> BI FBAD<63..0>

0	FBADQM<0>	M29	FBADQM0
1	FBADQM<1>	M30	FBADQM1
2	FBADQM<2>	G30	FBADQM2
3	FBADQM<3>	F29	FBADQM3
4	FBADQM<4>	AA29	FBADQM4
5	FBADQM<5>	AK30	FBADQM5
6	FBADQM<6>	AC30	FBADQM6
7	FBADQM<7>	AG30	FBADQM7

4<> OUT FBADQM<7..0>

0	FBADQS_WP<0>	L28	FBADQS_WP0
1	FBADQS_WP<1>	K31	FBADQS_WP1
2	FBADQS_WP<2>	G32	FBADQS_WP2
3	FBADQS_WP<3>	G28	FBADQS_WP3
4	FBADQS_WP<4>	AB28	FBADQS_WP4
5	FBADQS_WP<5>	AL32	FBADQS_WP5
6	FBADQS_WP<6>	AF32	FBADQS_WP6
7	FBADQS_WP<7>	AH30	FBADQS_WP7

4<> BI FBADQS_WP<7..0>

0	FBADQS_RN<0>	M28	FBADQS_RN0
1	FBADQS_RN<1>	K32	FBADQS_RN1
2	FBADQS_RN<2>	G31	FBADQS_RN2
3	FBADQS_RN<3>	G27	FBADQS_RN3
4	FBADQS_RN<4>	AA28	FBADQS_RN4
5	FBADQS_RN<5>	AL31	FBADQS_RN5
6	FBADQS_RN<6>	AF31	FBADQS_RN6
7	FBADQS_RN<7>	AH29	FBADQS_RN7

4<> BI FBADQS_RN<7..0>

FBVDD	A12	
FBVDD	A18	
FBVDD	A21	
FBVDD	A24	
FBVDD	A27	
FBVDD	A3	
FBVDD	A30	
FBVDD	A6	
FBVDD	A9	
FBVDD	AA32	
FBVDD	AD32	
FBVDD	AG32	
FBVDD	AK32	
FBVDD	C32	
FBVDD	F32	
FBVDD	J32	
FBVDD	M32	
FBVDD	R32	
FBVDDQ	AA25	
FBVDDQ	AA26	
FBVDDQ	AB25	
FBVDDQ	AB26	
FBVDDQ	G11	
FBVDDQ	G12	
FBVDDQ	G15	
FBVDDQ	G18	
FBVDDQ	G21	
FBVDDQ	G22	
FBVDDQ	H11	
FBVDDQ	H12	
FBVDDQ	H15	
FBVDDQ	H18	
FBVDDQ	H21	
FBVDDQ	H22	
FBVDDQ	L25	
FBVDDQ	L26	
FBVDDQ	M25	
FBVDDQ	M26	
FBVDDQ	R25	
FBVDDQ	R26	
FBVDDQ	V25	
FBVDDQ	V26	

2

FBVDDQ

C645 .47UF 6.3V 10% X5R 0402 COMMON
C725 .47UF 6.3V 10% X5R 0402 COMMON
C654 .1UF 16V 10% X7R 0402 COMMON
C757 .1UF 16V 10% X7R 0402 COMMON
C680 .1UF 16V 10% X7R 0402 COMMON
C697 .1UF 16V 10% X7R 0402 COMMON
C749 .1UF 16V 10% X7R 0402 COMMON
C687 .1UF 16V 10% X7R 0402 COMMON
C642 1UF 6.3V 10% X7R 0603 COMMON
C684 .47UF 6.3V 10% X5R 0402 COMMON
C661 .47UF 6.3V 10% X5R 0402 COMMON
C716 .1UF 16V 10% X7R 0402 COMMON
C662 .1UF 16V 10% X7R 0402 COMMON
C707 1UF 6.3V 10% X7R 0603 COMMON
C659 .1UF 16V 10% X7R 0402 COMMON
C675 .1UF 16V 10% X7R 0402 COMMON
C691 .1UF 16V 10% X7R 0402 COMMON
C692 .47UF 6.3V 10% X5R 0402 COMMON
C646 .47UF 6.3V 10% X5R 0402 COMMON

GND

PLACE BELOW GPU

NET	MIN_LINE_WIDTH
BI PLLAVDD	10MIL
BI FBA_PLLAVDD_R	10MIL

FBVDDQ

C601 10UF 6.3V 20% X5R 0805 COMMON
C602 10UF 6.3V 20% X5R 0805 COMMON
C607 10UF 6.3V 20% X5R 0805 COMMON
C840 10UF 6.3V 20% X5R 0805 COMMON

GND

PLACE MIDWAY BETWEEN GPU AND MEMORY

FBA_CMD0	P32	FBA_CMD<0>	0
FBA_CMD1	U27	FBA_CMD<1>	1
FBA_CMD2	P31	FBA_CMD<2>	2
FBA_CMD3	U30	FBA_CMD<3>	3
FBA_CMD4	Y31	FBA_CMD<4>	4
FBA_CMD5	W32	FBA_CMD<5>	5
FBA_CMD6	W31	FBA_CMD<6>	6
FBA_CMD7	T32	FBA_CMD<7>	7
FBA_CMD8	V27	FBA_CMD<8>	8
FBA_CMD9	T28	FBA_CMD<9>	9
FBA_CMD10	T31	FBA_CMD<10>	10
FBA_CMD11	U32	FBA_CMD<11>	11
FBA_CMD12	W29	FBA_CMD<12>	12
FBA_CMD13	W30	FBA_CMD<13>	13
FBA_CMD14	T27	SNN_FBA_CMD<14>	
FBA_CMD15	V28	FBA_CMD<15>	15
FBA_CMD16	V30	FBA_CMD<16>	16
FBA_CMD17	U31	FBA_CMD<17>	17
FBA_CMD18	R27	FBA_CMD<18>	18
FBA_CMD19	V29	FBA_CMD<19>	19
FBA_CMD20	T30	FBA_CMD<20>	20
FBA_CMD21	W28	FBA_CMD<21>	21
FBA_CMD22	R29	FBA_CMD<22>	22
FBA_CMD23	R30	FBA_CMD<23>	23
FBA_CMD24	P29	FBA_CMD<24>	24
FBA_CMD25	U28	FBA_CMD<25>	25
FBA_CMD26	Y32	SNN_FBA_CMD<26>	
FBA_CMD27	Y30	SNN_FBA_CMD<27>	
FBA_CMD28	V32	SNN_FBA_CMD<28>	

FBA_CMD<26..0> OUT 4<> 4<>

FBA_CLK0	P28	FBA_CLK0	OUT 4<
FBA_CLK0	R28	FBA_CLK0*	OUT 4<
FBA_CLK1	Y27	FBA_CLK1	OUT 4<
FBA_CLK1	AA27	FBA_CLK1*	OUT 4<

FBA_DEBUG AC27 LTP_FBA_DEBUG TP505

NO STUFF

PLACE close to balls

PEX1V2

240R@100MHz LB502 BEAD_0402 COMMON

H_PLLAVDD G23 PLLAVDD
FBA_PLLAVDD G25
FBA_PLLGND G24

C671 .01UF 16V 10% X7R 0402 COMMON
C670 .1UF 16V 10% X7R 0402 COMMON
C669 1UF 6.3V 10% X5R 0603 COMMON

GND

NC1 D31 SNN_GPU_NC1
NC2 D32 SNN_GPU_NC2

FBVDDQ

Rtop R590 1% 0402 NO STUFF
Rbot R562 1% 0402 1.27K NO STUFF

C627 .1UF 16V 10% X7R 0402 COMMON

FBA_VREF E32 FB_VREF1

GND

VREF = FBVDDQ * Rbot/(Rtop + Rbot)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 2.7K/(1.15K + 2.7K)

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBA MEMORY INTERFACE, GPU FBVDD/Q DECOUPLING CAPS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10402-0000-200 C		
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NAME	broth	DATE	22-FEB-2007

FrameBuffer: Partition A 8Mx32 BGA136 DDR3

A-CS0-LOW-32bit

M3 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

FBVDDQ

4<> 4< 3> IN FBA_CMD<26..0>

1	FBA_CMD<1>	H3	RAS	BA2	VDD	F1	
10	FBA_CMD<10>	F4	CAS	CS0	VDD	M1	
11	FBA_CMD<11>	H9	WE	CKE	VDD	A2	
8 CS0	FBA_CMD<8>	F9	CS0	CAS	VDD	V2	
					VDD	A11	
19	FBA_CMD<19>	K4	A0	A4	VDD	V11	
25	FBA_CMD<25>	H2	A1	A5	VDD	F12	
22	FBA_CMD<22>	K3	A2	A6	VDD	M12	
24	FBA_CMD<24>	M4	A3	A9			
0	FBA_CMD<0>	K9	A4	A0	VDDQ	A1	
2	FBA_CMD<2>	H11	A5	A1	VDDQ	C1	
21	FBA_CMD<21>	K10	A6	A2	VDDQ	E1	
16	FBA_CMD<16>	L9	A7	A11	VDDQ	N1	
23	FBA_CMD<23>	K11	A8/AP	A10	VDDQ	R1	
20	FBA_CMD<20>	M9	A9	A3	VDDQ	V1	
17	FBA_CMD<17>	K2	A10	A8/AP	VDDQ	C4	
9	FBA_CMD<9>	L4	A11	A7	VDDQ	E4	
					VDDQ	J4	
					VDDQ	N4	
12	FBA_CMD<12>	G4	BA0	BA1	VDDQ	R4	
3	FBA_CMD<3>	G9	BA1	BA0	VDDQ	C9	
7	FBA_CMD<7>	H10	BA2	RAS	VDDQ	E9	
					VDDQ	J9	
18	FBA_CMD<18>	H4	CKE	WE	VDDQ	N9	
4< 3> IN FBA_CLK0		J11	CLK		VDDQ	R9	
4< 3> IN FBA_CLK0*		J10	CLK		VDDQ	A12	
	SNN_FBA0_NC1	J2	NC/RFU		VDDQ	C12	
	SNN_FBA0_NC2	J3	NC/CS1	NC/CS1	VDDQ	E12	
		V4	SEN (GND)		VDDQ	N12	
					VDDQ	R12	
					VDDQ	V12	
15	FBA_CMD<15>	V9	RESET				
		A9	MIRROR		VSSQ	B1	
	FBA_ZQ0	A4	ZQ		VSSQ	D1	
					VSSQ	P1	
					VSSQ	T1	
					VSSQ	G2	
					VSSQ	L2	
					VSSQ	B4	
					VSSQ	D4	
					VSSQ	P4	
					VSSQ	T4	
					VSSQ	B9	
					VSSQ	D9	
					VSSQ	P9	
					VSSQ	T9	
					VSSQ	G11	
					VSSQ	L11	
					VSSQ	B12	
					VSSQ	D12	
					VSSQ	P12	
					VSSQ	T12	
					VSS	G1	
		K1	VDDA		VSS	L1	
		K12	VDDA		VSS	A3	
					VSS	V3	
					VSS	A10	
					VSS	V10	
					VSS	G12	
					VSS	L12	
		J1	VSSA				
		J12	VSSA		VREF	H1	FBA_VREF0
					VREF	H12	FBA_VREF1

Low Sub-Partition

NONMIRROR MIRROR

R552 10K 5% 0402 COMMON

R547 10K 5% 0402 COMMON

R550 243 1% 0402 COMMON

GND

DDR3: ZQ = 6x desired output
Impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

DDR3: CKE DETERMINES THE ODT VALUE FOR CMD PINS
CKE = 0 --> ODT = ZQ/2
CKE = 1 --> ODT = ZQ

FBVDDQ

R556 590 1% 0402 COMMON R1

R557 1.27K 1% 0402 COMMON R2

C597 .1UF 16V 10% X7R 0402 COMMON

C525 .047UF 16V 10% X7R 0402 COMMON

C598 .047UF 16V 10% X7R 0402 COMMON

R34 590 1% 0402 COMMON R1

R35 1.27K 1% 0402 COMMON R2

C51 .1UF 16V 10% X7R 0402 COMMON

*CS1 is required 32Mx32 Memories VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 1.3K/(511 + 1.3K)
1.4V = 2.0V * 1.3K/(511 + 1.3K)

FBA Partition

136BGA CMD Mapping

CMD	ADDR	
CMD1	RAS*	
CMD10	CAS*	
CMD11	WE*	
CMD18	CKE	
CMD15	RESET	
CMD8	CS0*	
CMD19	A<0>	
CMD25	A<1>	
CMD22	A<2>	Low Sub-Partition
CMD24	A<3>	Low Sub-Partition
CMD0	A<4>	Low Sub-Partition
CMD2	A<5>	Low Sub-Partition
CMD4	A<2>	Hi Sub-Partition
CMD6	A<3>	Hi Sub-Partition
CMD5	A<4>	Hi Sub-Partition
CMD13	A<5>	Hi Sub-Partition
CMD21	A<6>	
CMD16	A<7>	
CMD23	A<8>	
CMD20	A<9>	
CMD17	A<10	
CMD9	A<11>	
CMD12	BA0	
CMD3	BA1	
CMD7	BA2	

A-CS0-HI-32bit

M4 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

FBVDDQ

4<> 4< 3> IN FBA_CMD<26..0>

7	FBA_CMD<7>	H3	RAS	BA2	VDD	F1	
8 CS0	FBA_CMD<8>	F4	CAS	CS0	VDD	M1	
18	FBA_CMD<18>	H9	WE	CKE	VDD	A2	
10	FBA_CMD<10>	F9	CS0	CAS	VDD	V2	
					VDD	A11	
5	FBA_CMD<5>	K4	A0	A4	VDD	V11	
13	FBA_CMD<13>	H2	A1	A5	VDD	F12	
21	FBA_CMD<21>	K3	A2	A6	VDD	M12	
20	FBA_CMD<20>	M4	A3	A9			
19	FBA_CMD<19>	K9	A4	A0	VDDQ	A1	
25	FBA_CMD<25>	H11	A5	A1	VDDQ	C1	
4	FBA_CMD<4>	K10	A6	A2	VDDQ	E1	
9	FBA_CMD<9>	L9	A7	A11	VDDQ	N1	
17	FBA_CMD<17>	K11	A8/AP	A10	VDDQ	R1	
6	FBA_CMD<6>	M9	A9	A3	VDDQ	V1	
23	FBA_CMD<23>	K2	A10	A8/AP	VDDQ	C4	
16	FBA_CMD<16>	L4	A11	A7	VDDQ	E4	
					VDDQ	J4	
					VDDQ	N4	
3	FBA_CMD<3>	G4	BA0	BA1	VDDQ	R4	
12	FBA_CMD<12>	G9	BA1	BA0	VDDQ	C9	
1	FBA_CMD<1>	H10	BA2	RAS	VDDQ	E9	
					VDDQ	J9	
11	FBA_CMD<11>	H4	CKE	WE	VDDQ	N9	
4< 3> IN FBA_CLK1		J11	CLK		VDDQ	R9	
4< 3> IN FBA_CLK1*		J10	CLK		VDDQ	A12	
	SNN_FBA1_NC1	J2	NC/RFU		VDDQ	C12	
	SNN_FBA1_NC2	J3	NC/CS1	NC/CS1	VDDQ	E12	
		V4	SEN (GND)		VDDQ	N12	
					VDDQ	R12	
					VDDQ	V12	
15	FBA_CMD<15>	V9	RESET				
		A9	MIRROR		VSSQ	B1	
	FBA_ZQ1	A4	ZQ		VSSQ	D1	
					VSSQ	P1	
					VSSQ	T1	
					VSSQ	G2	
					VSSQ	L2	
					VSSQ	B4	
					VSSQ	D4	
					VSSQ	P4	
					VSSQ	T4	
					VSSQ	B9	
					VSSQ	D9	
					VSSQ	P9	
					VSSQ	T9	
					VSSQ	G11	
					VSSQ	L11	
					VSSQ	B12	
					VSSQ	D12	
					VSSQ	P12	
					VSSQ	T12	
					VSS	G1	
		K1	VDDA		VSS	L1	
		K12	VDDA		VSS	A3	
					VSS	V3	
					VSS	A10	
					VSS	V10	
					VSS	G12	
					VSS	L12	
		J1	VSSA				
		J12	VSSA		VREF	H1	FBA_VREF2
					VREF	H12	FBA_VREF3

Hi Sub-Partition

NONMIRROR MIRROR

R543 243 1% 0402 COMMON

GND

DDR3: ZQ = 6x desired output
impedence of DQ drivers
Impedence = 240 / 6 = 40 ohm

FBVDDQ

R37 590 1% 0402 COMMON R1

R36 1.27K 1% 0402 COMMON R2

C53 .1UF 16V 10% X7R 0402 COMMON

C599 .047UF 16V 10% X7R 0402 COMMON

C52 .047UF 16V 10% X7R 0402 COMMON

R559 590 1% 0402 COMMON R1

R558 1.27K 1% 0402 COMMON R2

C595 .1UF 16V 10% X7R 0402 COMMON

*CS1 is required 32Mx32 Memories VREF = FBVDDQ * R2/(R1 + R2)

DDR3: VREF = 0.70 * FBVDDQ
1.26V = 1.8V * 1.3K/(511 + 1.3K)
1.4V = 2.0V * 1.3K/(511 + 1.3K)

NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
4< 3> IN FBA_CLK0	FBA_CLK0	80DIFF	1
4< 3> IN FBA_CLK0*	FBA_CLK0	80DIFF	1
4< 3> IN FBA_CLK1	FBA_CLK1	80DIFF	1
4< 3> IN FBA_CLK1*	FBA_CLK1	80DIFF	1
4<> 3<> BI FBAD<63..0>		40OHM	1
4<> 3> BI FBADQM<7..0>		40OHM	1
4< 3> BI FBA_CMD<26:0>		40OHM	1

MIN_LINE_WIDTH

BI FBA_VREF0	12MIL
BI FBA_VREF1	12MIL
BI FBA_VREF2	12MIL
BI FBA_VREF3	12MIL

NV_IMPEDANCE	DIFFPAIR	NV_CRITICAL_NET
4<> 3<> BI FBADQS_WP<7:0>	40OHM	1
4<> 3<> BI FBADQS_RN<7:0>	40OHM	1

Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!

4<> 3<> BI FBAD<63..0>

4<> 3> BI FBADQM<7..0>

0	FBADQM<0>						
1	FBADQM<1>						
2	FBADQM<2>						
3	FBADQM<3>						
4	FBADQM<4>						
5	FBADQM<5>						
6	FBADQM<6>						
7	FBADQM<7>						

4<> 3<> BI FBADQS_RN<7..0>

0	FBADQS_RN<0>						
1	FBADQS_RN<1>						
2	FBADQS_RN<2>						
3	FBADQS_RN<3>						
4	FBADQS_RN<4>						
5	FBADQS_RN<5>						
6	FBADQS_RN<6>						
7	FBADQS_RN<7>						

4<> 3<> BI FBADQS_WP<7..0>

0	FBADQS_WP<0>						
1	FBADQS_WP<1>						
2	FBADQS_WP<2>						
3	FBADQS_WP<3>						
4	FBADQS_WP<4>						
5	FBADQS_WP<5>						
6	FBADQS_WP<6>						
7	FBADQS_WP<7>						

M3 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

0	FBAD<0>	R11	DQ0	DQM			
1	FBAD<1>	T11	DQ1	RDQS			
2	FBAD<2>	R10	DQ2	WDQS			
3	FBAD<3>	T10	DQ3				
4	FBAD<4>	N11	DQ4				
5	FBAD<5>	M11	DQ5				
6	FBAD<6>	L10	DQ6				
7	FBAD<7>	M10	DQ7				
	FBADQM<0>	N10	DOM				
	FBADQS_RN<0>	P10	RDQS				
	FBADQS_WP<0>	P11	WDQS				

M3 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

8	FBAD<8>	T3	DQ0	DQM			
9	FBAD<9>	R2	DQ1	RDQS			
10	FBAD<10>	R3	DQ2	WDQS			
11	FBAD<11>	T2	DQ3				
12	FBAD<12>	M2	DQ4				
13	FBAD<13>	N2	DQ5				
14	FBAD<14>	L3	DQ6				
15	FBAD<15>	M3	DQ7				
	FBADQM<1>	N3	DOM				
	FBADQS_RN<1>	P3	RDQS				
	FBADQS_WP<1>	P2	WDQS				

M3 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

16	FBAD<16>	B2	DQ0	DQM			
17	FBAD<17>	E2	DQ1	RDQS			
18	FBAD<18>	C2	DQ2	WDQS			
19	FBAD<19>	B3	DQ3				
20	FBAD<20>	C3	DQ4				
21	FBAD<21>	F3	DQ5				
22	FBAD<22>	G3	DQ6				
23	FBAD<23>	F2	DQ7				
	FBADQM<2>	E3	DOM				
	FBADQS_RN<2>	D3	RDQS				
	FBADQS_WP<2>	D2	WDQS				

M3 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

24	FBAD<24>	F11	DQ0	DQM			
25	FBAD<25>	E10	DQ1	RDQS			
26	FBAD<26>	B11	DQ2	WDQS			
27	FBAD<27>	B10	DQ3				
28	FBAD<28>	C11	DQ4				
29	FBAD<29>	E11	DQ5				
30	FBAD<30>	G10	DQ6				
31	FBAD<31>	C10	DQ7				
	FBADQM<3>	E10	DOM				
	FBADQS_RN<3>	D10	RDQS				
	FBADQS_WP<3>	D11	WDQS				

M4 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

32	FBAD<32>	L3	DQ0	DQM			
33	FBAD<33>	M2	DQ1	RDQS			
34	FBAD<34>	M3	DQ2	WDQS			
35	FBAD<35>	N2	DQ3				
36	FBAD<36>	T3	DQ4				
37	FBAD<37>	R2	DQ5				
38	FBAD<38>	T2	DQ6				
39	FBAD<39>	R3	DQ7				
	FBADQM<4>	N3	DOM				
	FBADQS_RN<4>	P3	RDQS				
	FBADQS_WP<4>	P2	WDQS				

M4 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

40	FBAD<40>	B10	DQ0	DQM			
41	FBAD<41>	G10	DQ1	RDQS			
42	FBAD<42>	F10	DQ2	WDQS			
43	FBAD<43>	E11	DQ3				
44	FBAD<44>	F11	DQ4				
45	FBAD<45>	C10	DQ5				
46	FBAD<46>	C11	DQ6				
47	FBAD<47>	B11	DQ7				
	FBADQM<5>	E10	DOM				
	FBADQS_RN<5>	D10	RDQS				
	FBADQS_WP<5>	D11	WDQS				

M4 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

48	FBAD<48>	R10	DQ0	DQM			
49	FBAD<49>	M11	DQ1	RDQS			
50	FBAD<50>	R11	DQ2	WDQS			
51	FBAD<51>	T11	DQ3				
52	FBAD<52>	N11	DQ4				
53	FBAD<53>	T10	DQ5				
54	FBAD<54>	M10	DQ6				
55	FBAD<55>	L10	DQ7				
	FBADQM<6>	N10	DOM				
	FBADQS_RN<6>	P10	RDQS				
	FBADQS_WP<6>	P11	WDQS				

M4 GDDR3_16MX32 PACK_TYPE=BGA136 VERSION=BGA136 COMMON

56	FBAD<56>	B3	DQ0	DQM			
57	FBAD<57>	F3	DQ1	RDQS			
58	FBAD<58>	C2	DQ2	WDQS			
59	FBAD<59>	C3	DQ3				
60	FBAD<60>	F2	DQ4				
61	FBAD<61>	E2	DQ5				
62	FBAD<62>	B2	DQ6				
63	FBAD<63>	G3	DQ7				
	FBADQM<7>	E3	DOM				
	FBADQS_RN<7>	D3	RDQS				
	FBADQS_WP<7>	D2	WDQS				

4<> 4< 3> IN FBA_CMD<26..0>

FBVDDQ

2	FBA_CMD<2>	120 COMMON 5%	R539 0402
0	FBA_CMD<0>	120 COMMON 5%	R545 0402
24	FBA_CMD<24>	120 COMMON 5%	R551 0402
22	FBA_CMD<22>	120 COMMON 5%	R546 0402
13	FBA_CMD<13>	120 COMMON 5%	R542 0402
4	FBA_CMD<4>	120 COMMON 5%	R548 0402
5	FBA_CMD<5>	120 COMMON 5%	R544 0402
6	FBA_CMD<6>	120 COMMON 5%	R549 0402
FBA_CLK0		121 COMMON 1%	R540 0402
FBA_CLK0*		121 COMMON 1%	R541 0402
FBA_CLK1		121 COMMON 1%	R555 0402
FBA_CLK1*		121 COMMON 1%	R553 0402

FBA_CLK0_PU

FBA_CLK1_PU

FBVDDQ

R538 80.6 1% 0402 NO STUFF

R554 80.6 1% 0402 NO STUFF

C527 .01UF 6.3V 10% X7R 0402 COMMON

C573 .01UF 6.3V 10% X7R 0402 COMMON

GND

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBA 8Mx32 DDR3 MEMORIES, FBA COMMAND BUS PU'S, FBA CLK TERMS

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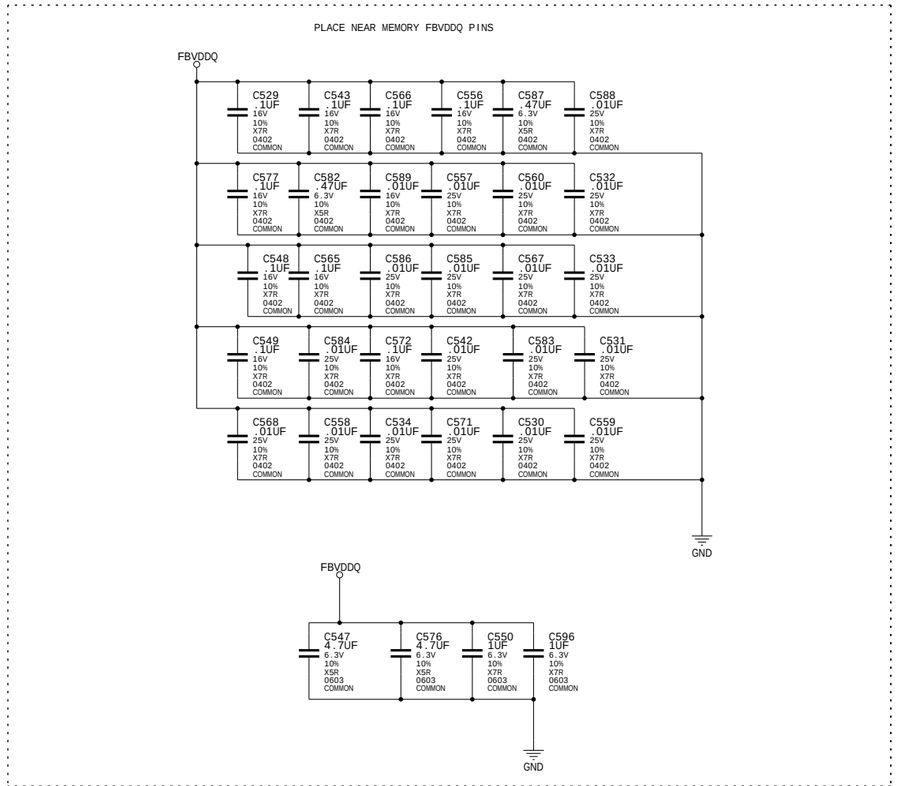
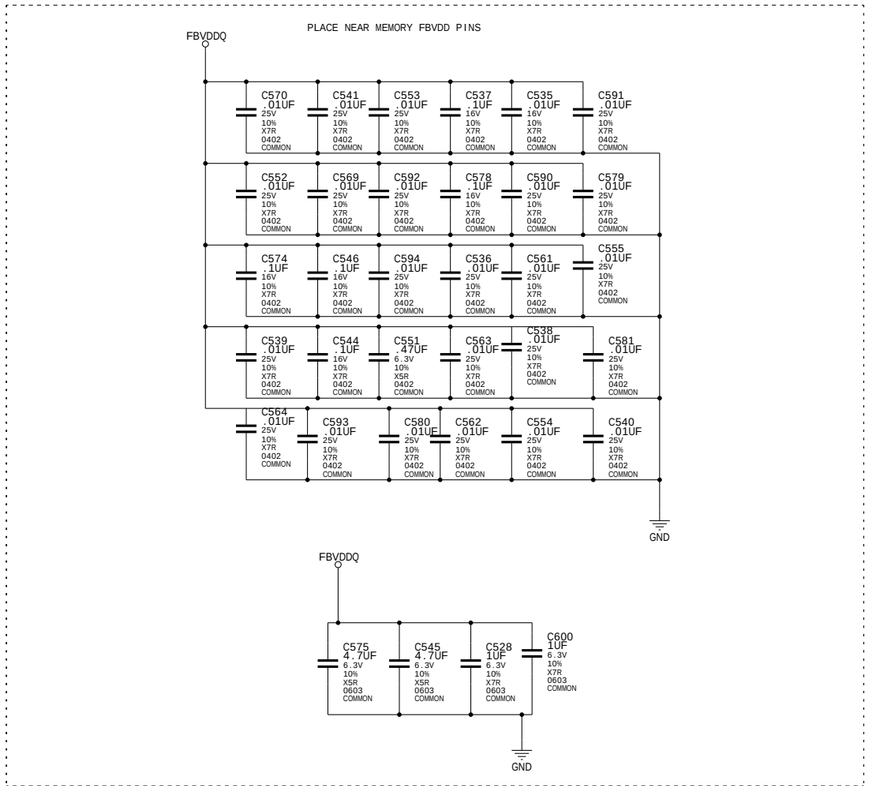
NV_PN	600-10402-0000-200 C		
ID	p402	PAGE	4 OF 21
NAME	broth	DATE	22-FEB-2007

FRAME BUFFER: PARTITION A DECOUPLING

Decoupling for FBA 0..31



Decoupling for FBA 32..63



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBA MEMORY FBVDD/Q DECOUPLING CAPS

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NV_PN	600-10402-0000-200 C		
ID	p402	PAGE	5 OF 21
NAME	broth	DATE	22-FEB-2007

NET	MIN_LINE_WIDTH
FBC_PLLVDD	10MIL
FBC_PLLAVDD	10MIL
FBC_PLLAVDD_R	10MIL

G1
G84-875-A2
BGA820
DNI

3/14 FBC

0	FBCD<0>	B7	FBCD0
1	FBCD<1>	A7	FBCD1
2	FBCD<2>	C7	FBCD2
3	FBCD<3>	A2	FBCD3
4	FBCD<4>	B2	FBCD4
5	FBCD<5>	C4	FBCD5
6	FBCD<6>	A5	FBCD6
7	FBCD<7>	B5	FBCD7
8	FBCD<8>	F9	FBCD8
9	FBCD<9>	F10	FBCD9
10	FBCD<10>	D12	FBCD10
11	FBCD<11>	D9	FBCD11
12	FBCD<12>	E12	FBCD12
13	FBCD<13>	D11	FBCD13
14	FBCD<14>	E8	FBCD14
15	FBCD<15>	D8	FBCD15
16	FBCD<16>	E7	FBCD16
17	FBCD<17>	F7	FBCD17
18	FBCD<18>	D6	FBCD18
19	FBCD<19>	D5	FBCD19
20	FBCD<20>	D3	FBCD20
21	FBCD<21>	E4	FBCD21
22	FBCD<22>	C3	FBCD22
23	FBCD<23>	B4	FBCD23
24	FBCD<24>	C10	FBCD24
25	FBCD<25>	B10	FBCD25
26	FBCD<26>	C9	FBCD26
27	FBCD<27>	A10	FBCD27
28	FBCD<28>	C11	FBCD28
29	FBCD<29>	C12	FBCD29
30	FBCD<30>	A11	FBCD30
31	FBCD<31>	B11	FBCD31
32	FBCD<32>	B28	FBCD32
33	FBCD<33>	C27	FBCD33
34	FBCD<34>	C26	FBCD34
35	FBCD<35>	B26	FBCD35
36	FBCD<36>	C30	FBCD36
37	FBCD<37>	B31	FBCD37
38	FBCD<38>	C29	FBCD38
39	FBCD<39>	A31	FBCD39
40	FBCD<40>	D28	FBCD40
41	FBCD<41>	D27	FBCD41
42	FBCD<42>	F26	FBCD42
43	FBCD<43>	D24	FBCD43
44	FBCD<44>	E23	FBCD44
45	FBCD<45>	E26	FBCD45
46	FBCD<46>	E24	FBCD46
47	FBCD<47>	F23	FBCD47
48	FBCD<48>	B23	FBCD48
49	FBCD<49>	A23	FBCD49
50	FBCD<50>	C25	FBCD50
51	FBCD<51>	C23	FBCD51
52	FBCD<52>	A22	FBCD52
53	FBCD<53>	C22	FBCD53
54	FBCD<54>	C21	FBCD54
55	FBCD<55>	B22	FBCD55
56	FBCD<56>	E22	FBCD56
57	FBCD<57>	D22	FBCD57
58	FBCD<58>	D21	FBCD58
59	FBCD<59>	E21	FBCD59
60	FBCD<60>	E18	FBCD60
61	FBCD<61>	D19	FBCD61
62	FBCD<62>	D18	FBCD62
63	FBCD<63>	E19	FBCD63

0	FBCDQM<0>	A4	FBCDQM0
1	FBCDQM<1>	E11	FBCDQM1
2	FBCDQM<2>	F5	FBCDQM2
3	FBCDQM<3>	C9	FBCDQM3
4	FBCDQM<4>	C28	FBCDQM4
5	FBCDQM<5>	F24	FBCDQM5
6	FBCDQM<6>	C24	FBCDQM6
7	FBCDQM<7>	E20	FBCDQM7

0	FBCDQS_WP<0>	C5	FBCDQS_WP0
1	FBCDQS_WP<1>	E10	FBCDQS_WP1
2	FBCDQS_WP<2>	E5	FBCDQS_WP2
3	FBCDQS_WP<3>	B8	FBCDQS_WP3
4	FBCDQS_WP<4>	A29	FBCDQS_WP4
5	FBCDQS_WP<5>	D25	FBCDQS_WP5
6	FBCDQS_WP<6>	B25	FBCDQS_WP6
7	FBCDQS_WP<7>	F20	FBCDQS_WP7

0	FBCDQS_RN<0>	C6	FBCDQS_RN0
1	FBCDQS_RN<1>	E9	FBCDQS_RN1
2	FBCDQS_RN<2>	E6	FBCDQS_RN2
3	FBCDQS_RN<3>	A8	FBCDQS_RN3
4	FBCDQS_RN<4>	B29	FBCDQS_RN4
5	FBCDQS_RN<5>	E25	FBCDQS_RN5
6	FBCDQS_RN<6>	A25	FBCDQS_RN6
7	FBCDQS_RN<7>	F21	FBCDQS_RN7

SNN_FBC_VREF_A28 — A28 — FB_VREF2

FBVTT	AA23	SNN_FBVTT_AA23
FBVTT	AB23	SNN_FBVTT_AB23
FBVTT	H16	SNN_FBVTT_H16
FBVTT	H17	SNN_FBVTT_H17
FBVTT	J10	SNN_FBVTT_J10
FBVTT	J23	SNN_FBVTT_J23
FBVTT	J24	SNN_FBVTT_J24
FBVTT	J9	SNN_FBVTT_J9
FBVTT	K11	SNN_FBVTT_K11
FBVTT	K12	SNN_FBVTT_K12
FBVTT	K21	SNN_FBVTT_K21
FBVTT	K22	SNN_FBVTT_K22
FBVTT	K24	SNN_FBVTT_K24
FBVTT	K9	SNN_FBVTT_K9
FBVTT	L23	SNN_FBVTT_L23
FBVTT	M23	SNN_FBVTT_M23
FBVTT	T25	SNN_FBVTT_T25
FBVTT	U25	SNN_FBVTT_U25

FBC_CMD<26..0> OUT 7<

FBC_CMD0	C13	FBC_CMD<0>	0
FBC_CMD1	A16	FBC_CMD<1>	1
FBC_CMD2	A13	FBC_CMD<2>	2
FBC_CMD3	B17	FBC_CMD<3>	3
FBC_CMD4	B20	FBC_CMD<4>	4
FBC_CMD5	A19	FBC_CMD<5>	5
FBC_CMD6	B19	FBC_CMD<6>	6
FBC_CMD7	B14	FBC_CMD<7>	7
FBC_CMD8	E16	FBC_CMD<8>	8
FBC_CMD9	A14	FBC_CMD<9>	9
FBC_CMD10	C15	FBC_CMD<10>	10
FBC_CMD11	B16	FBC_CMD<11>	11
FBC_CMD12	F17	FBC_CMD<12>	12
FBC_CMD13	C19	FBC_CMD<13>	13
FBC_CMD14	D15	SNN_FBC_CMD<14>	
FBC_CMD15	C17	FBC_CMD<15>	15
FBC_CMD16	A17	FBC_CMD<16>	16
FBC_CMD17	C16	FBC_CMD<17>	17
FBC_CMD18	D14	FBC_CMD<18>	18
FBC_CMD19	F16	FBC_CMD<19>	19
FBC_CMD20	C14	FBC_CMD<20>	20
FBC_CMD21	C18	FBC_CMD<21>	21
FBC_CMD22	E14	FBC_CMD<22>	22
FBC_CMD23	B13	FBC_CMD<23>	23
FBC_CMD24	E15	FBC_CMD<24>	24
FBC_CMD25	F15	FBC_CMD<25>	25
FBC_CMD26	A20	SNN_FBC_CMD<26>	
FBC_CMD27	C20	SNN_FBC_CMD<27>	
FBC_CMD28	A15	SNN_FBC_CMD<28>	

FBC_CLK0	E13	FBC_CLK0	OUT 7<
FBC_CLK0	F13	FBC_CLK0*	OUT 7<
FBC_CLK1	F18	FBC_CLK1	OUT 7<
FBC_CLK1	E17	FBC_CLK1*	OUT 7<

FBC_DEBUG — F12 — LTP_FBC_DEBUG — TP3

NO STUFF

FBC_PLLVDD	G8	SNN_FBC_PLLVDD_G8		
FBC_PLLAVDD	G10	FBC_PLLAVDD		
FBC_PLLGND	G9			GND
FBCAL_PD_VDDQ	K26	FBCAL_PD	R573 43.2 0402 1% COMMON	FBVDDQ
FBCAL_PU_GND	H26	FBCAL_PU	R575 40.2 0402 1% COMMON	
FBCAL_TERM_GND	J26	FBCAL_TERM	R572 40.2 0402 1% COMMON	GND

Place close to balls

FBC_PLLAVDD → LB504 240R@100MHz BEAD_0402 COMMON → PEX1V2

C743	.01UF	16V	10% X7R 0402 COMMON
C742	.1UF	16V	10% X7R 0402 COMMON
C741	1UF	6.3V	10% X5R 0402 COMMON
C746	4.7UF	6.3V	10% X5R 0603 COMMON

GND

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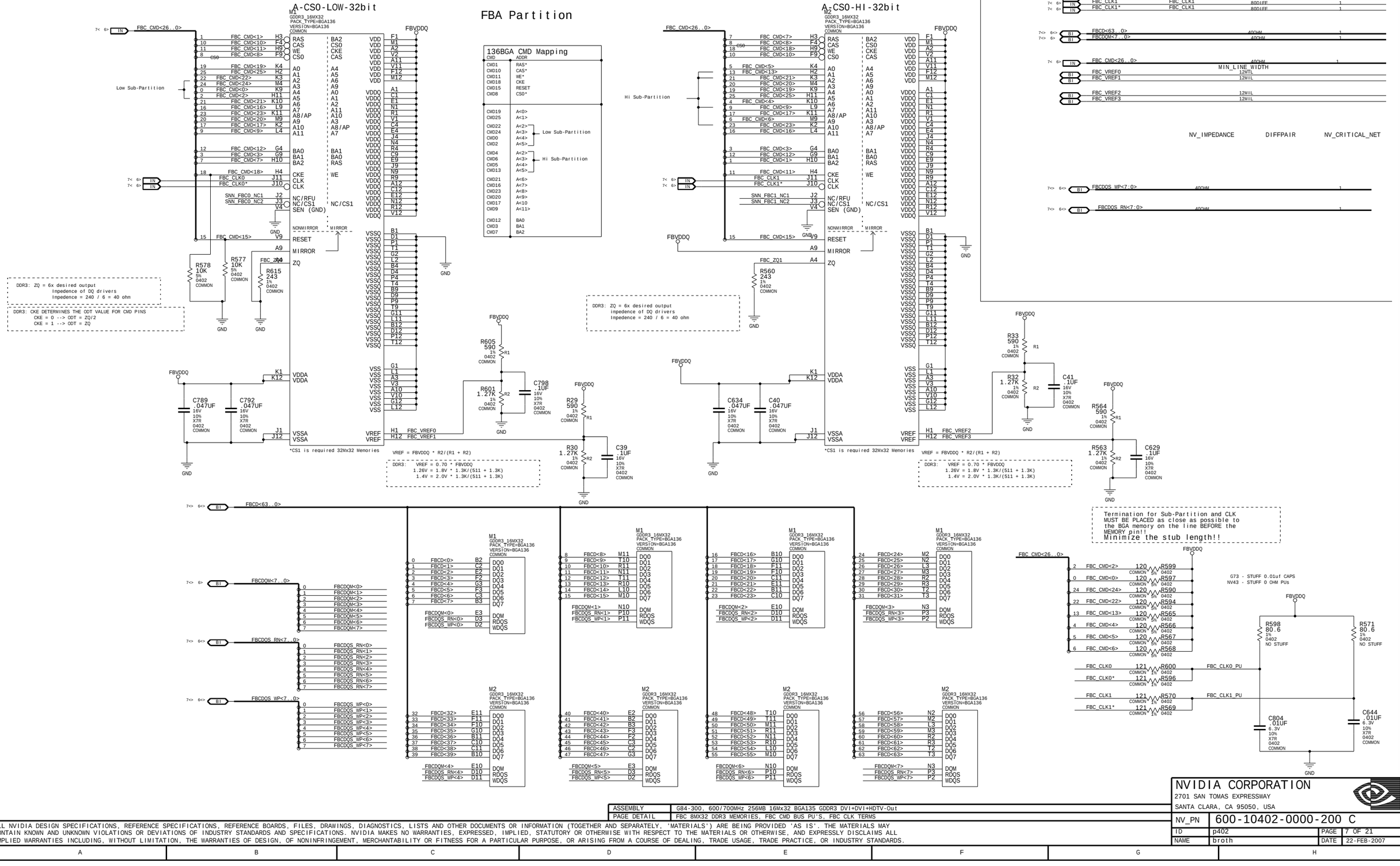
ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBC MEMORY INTERFACE, GPU FBVTT

NV_PN	600-10402-0000-200 C		
ID	p402	PAGE	6 OF 21
NAME	broth	DATE	22-FEB-2007

FRAMEBUFFER: PARTITION C 8Mx32 BGA136 DDR3



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBC 8MX32 DDR3 MEMORIES, FBC CMD BUS PU'S, FBC CLK TERMS

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NV_PN	600-10402-0000-200 C		
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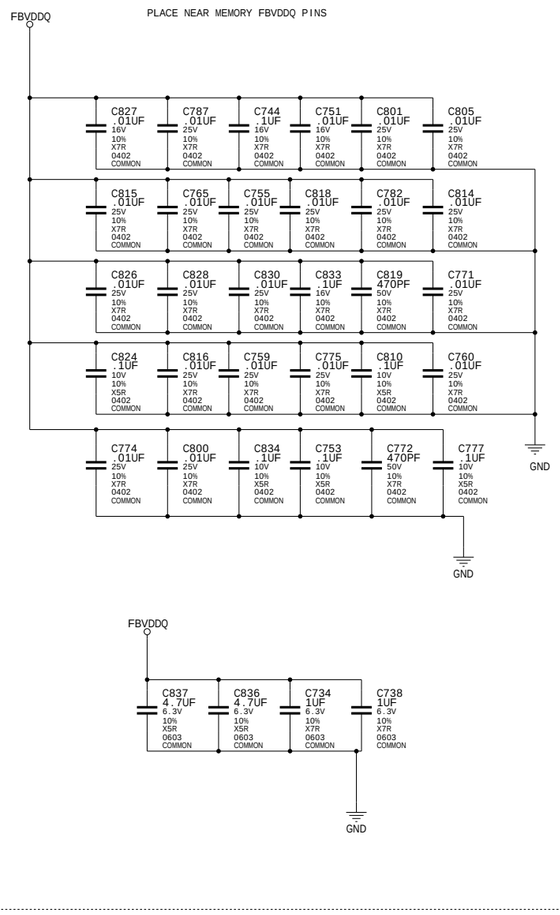
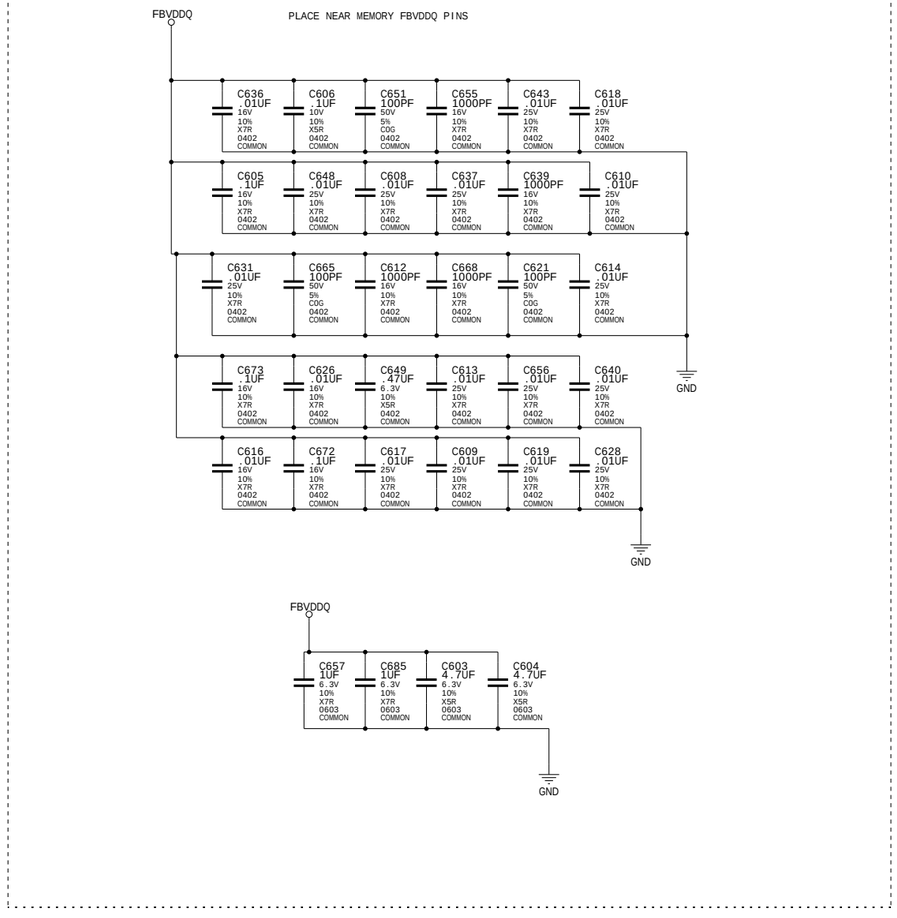
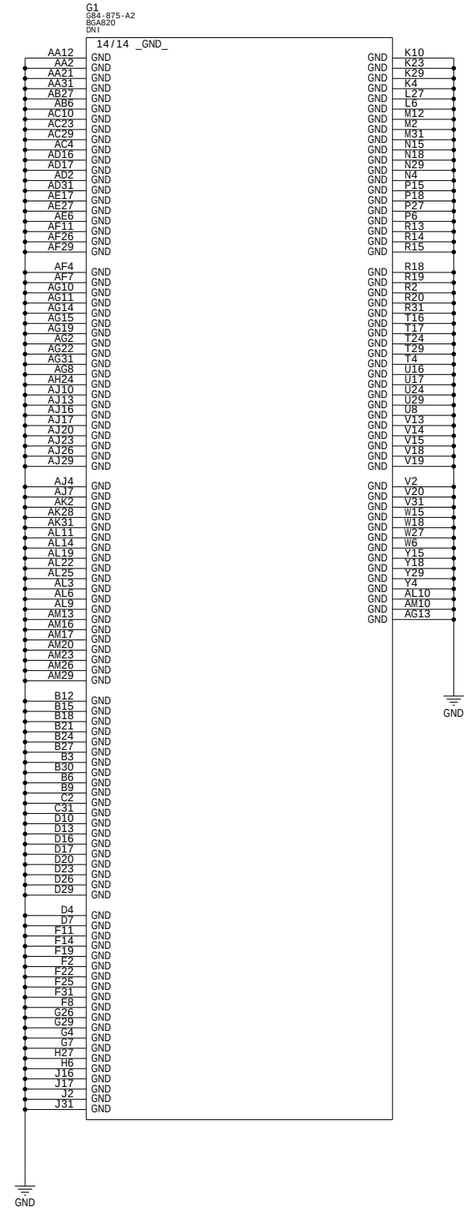
FRAMEBUFFER: PARTITION C DECOUPLING

Decoupling for FBC 0..31



Decoupling for FBC 32..63





ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	FBC MEMORY FBVDD/Q DECOUPLING CAPS, GPU GND CONNECTIONS

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NV_PN	600-10402-0000-200 C		
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Primary Display (DACA), Slim DB15

DACA RGB-FILTER

NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
IN DACA_VDD			12MIL
IN DACA_VREF			12MIL
IN DACA_RSET			12MIL
BI DACA_RED	1	75OHM	
BI DACA_GREEN	1	75OHM	
BI DACA_BLUE	1	75OHM	
11< 9> BI DACA_RED_C	1	75OHM	
11< 9> BI DACA_GREEN_C	1	75OHM	
11< 9> BI DACA_BLUE_C	1	75OHM	
BI DACA_HSYNC	1	50OHM	
BI DACA_VSYNC	1	50OHM	
BI AVB	1	50OHM	
BI AHB	1	50OHM	
BI DACA_VSYNC_BUF	1	50OHM	
BI DACA_HSYNC_BUF	1	50OHM	
11< 9> BI DACA_VSYNC_C	1	50OHM	
11< 9> BI DACA_HSYNC_C	1	50OHM	

4

PEX3V3
LB506 180R@100MHz BEAD_0603 COMMON
C737 470PF 50V X7R 10% 0402 COMMON
C745 .1UF 10V X5R 10% 0402 COMMON
R587 124 1% 0402 COMMON
C807 4.7UF 6.3V X5R 10% 0603 COMMON
C752 4700PF 25V X7R 10% 0402 COMMON
GND

G1
G84-875-A2
BGA820
DNI
4/14 DACA
DACA_VDD AD10
DACA_VREF AH10
DACA_RSET AH9
I2CA_SCL K2
I2CA_SDA J3
DACA_HSYNC AF10
DACA_VSYNC AK10
DACA_RED AH11
DACA_GREEN AJ12
DACA_BLUE AH12
DACA_IDUMP AG9

Route DAC RGB with ~37.5ohm Impedence

9> IN I2CA_SDA
R666 33 0402 5% COMMON I2CA_SDA_T
LB519 180R@100MHz BEAD_0603 COMMON
OUT 9> 11< 9> 11< I2CA_SDA_C
C876 22PF 50V 5% C0G 0402 COMMON
R670 2.2K 5% 0402 COMMON
5V
L505 0 0603 DNI
C871 .1UF 0603 16V 10% X7R NO STUFF
I2CA_PU_5V
R669 2.2K 5% 0402 COMMON
9> IN I2CA_SCL
R665 33 0402 5% COMMON I2CA_SCL_T
LB518 180R@100MHz BEAD_0603 COMMON
OUT 9> 11< 9> 11< I2CA_SCL_C
C875 22PF 50V 5% C0G 0402 COMMON

5V
U507 74ACT08 74ACT_SO COMMON
AVB
R662 33 0402 5% COMMON DACA_VSYNC_BUF
L508 27nH 0603 COMMON
OUT 9<> 9> 11< 9<> 9> 11< DACA_VSYNC_C
C879 47PF 50V 5% C0G 0603 COMMON
C861 .1UF 16V 10% X5R 0402 COMMON
PLACE NEAR SYNC BUFFER
D508 BAV99 SOT23 100V 100MA COMMON

5V
U507 74ACT08 74ACT_SO COMMON
AHB
R660 33 0402 5% COMMON DACA_HSYNC_BUF
L509 27nH 0603 COMMON
OUT 9<> 9> 11< 9<> 9> 11< DACA_HSYNC_C
C880 47PF 50V 5% C0G 0603 COMMON
D509 BAV99 SOT23 100V 100MA COMMON

DACA_RED
R585 150 1% 0402 COMMON
R5 150 1% 0402 COMMON
L5 27nH 0603 COMMON
C13 22PF 50V 5% C0G 0402 COMMON
C6 22PF 50V 5% C0G 0402 COMMON
DACA_RED_C

DACA_GREEN
R579 150 1% 0402 COMMON
R6 150 1% 0402 COMMON
L6 27nH 0603 COMMON
C14 22PF 50V 5% C0G 0402 COMMON
C7 22PF 50V 5% C0G 0402 COMMON
DACA_GREEN_C

DACA_BLUE
R580 150 1% 0402 COMMON
R4 150 1% 0402 COMMON
L4 27nH 0603 COMMON
C12 22PF 50V 5% C0G 0402 COMMON
C5 22PF 50V 5% C0G 0402 COMMON
DACA_BLUE_C

OUT 9<> 11<
OUT 9<> 11<
OUT 9<> 11<

DDC 5V
SOUTH
J2
CON_DSUB15HD
VGA_SLIM
NO STUFF
16
6 GND-R
1 R
7 GND-G
2 G
8 GND B
3 B
9 5V
4 ID2
10 GND
5 GND
17 SHIELD
ID0 11 SNN_A_MON_ID0
SDA 12 I2CA_SDA_C
HSYNC 13 DACA_HSYNC_C
VSYNC 14 DACA_VSYNC_C
SCL 15 I2CA_SCL_C
SNN_A_MON_ID2

FOR ESD DIODES
5V
C868 4.7UF 6.3V 10% X5R 0603 COMMON
Place in output filter section!

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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Secondary Display (DACC), Slim DB15

DACC RGB-FILTER

NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACC_VDD			12MIL
DACC_VREF			12MIL
DACC_RSET			12MIL
DACC_RED	1	75OHM	
DACC_GREEN	1	75OHM	
DACC_BLUE	1	75OHM	
DACC_RED_C	1	75OHM	
DACC_GREEN_C	1	75OHM	
DACC_BLUE_C	1	75OHM	
DACC_HSYNC	1	50OHM	
DACC_VSYNC	1	50OHM	
CVB	1	50OHM	
CHB	1	50OHM	
DACC_VSYNC_BUF	1	50OHM	
DACC_HSYNC_BUF	1	50OHM	
DACC_VSYNC_C	1	50OHM	
DACC_HSYNC_C	1	50OHM	

Place 0ohm Resistor Incident with Common Mode Choke

MIDDLE

FOR ESD DIODES

Place in output filter section!

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID

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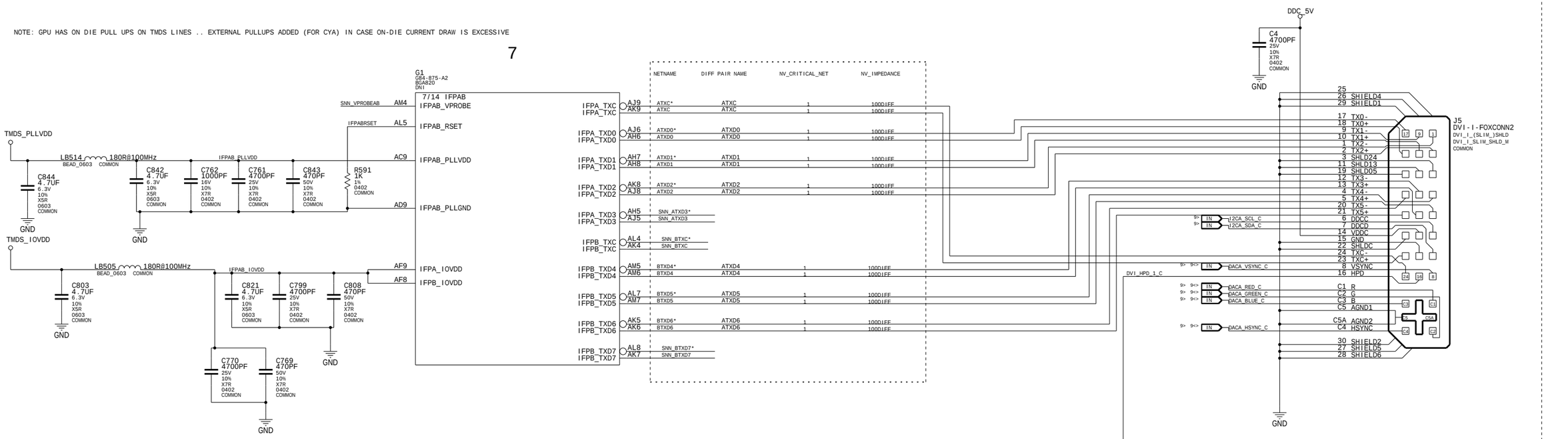
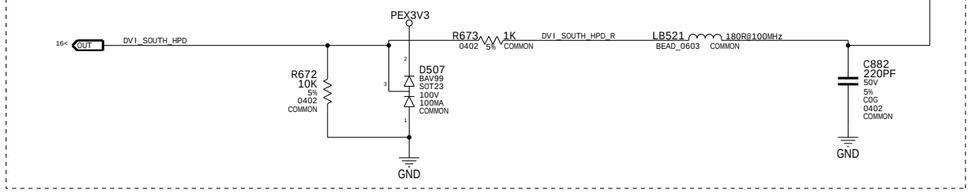
INTERNAL TMDS .. LINK A & B

NOTE: GPU HAS ON DIE PULL UPS ON TMDS LINES .. EXTERNAL PULLUPS ADDED (FOR CYA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE



Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
BI IFPAB_PLLVDD	12MIL	1.8V
TMDS_IOVDD TMDS_IOVDD	12MIL	3.3V
BI IFPAB_IOVDD	12MIL	3.3V
BI IFPABRSET	12MIL	
BI TMDS_IOBACK	12MIL	

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	TMDS LINK A/B & PU's, TMDS IO BACKDRIVE PREVENTION,DVI CONNECTOR SOUTH

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NV_PN	600-10402-0000-200 C		
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INTERNAL TMDS .. LINK C & D

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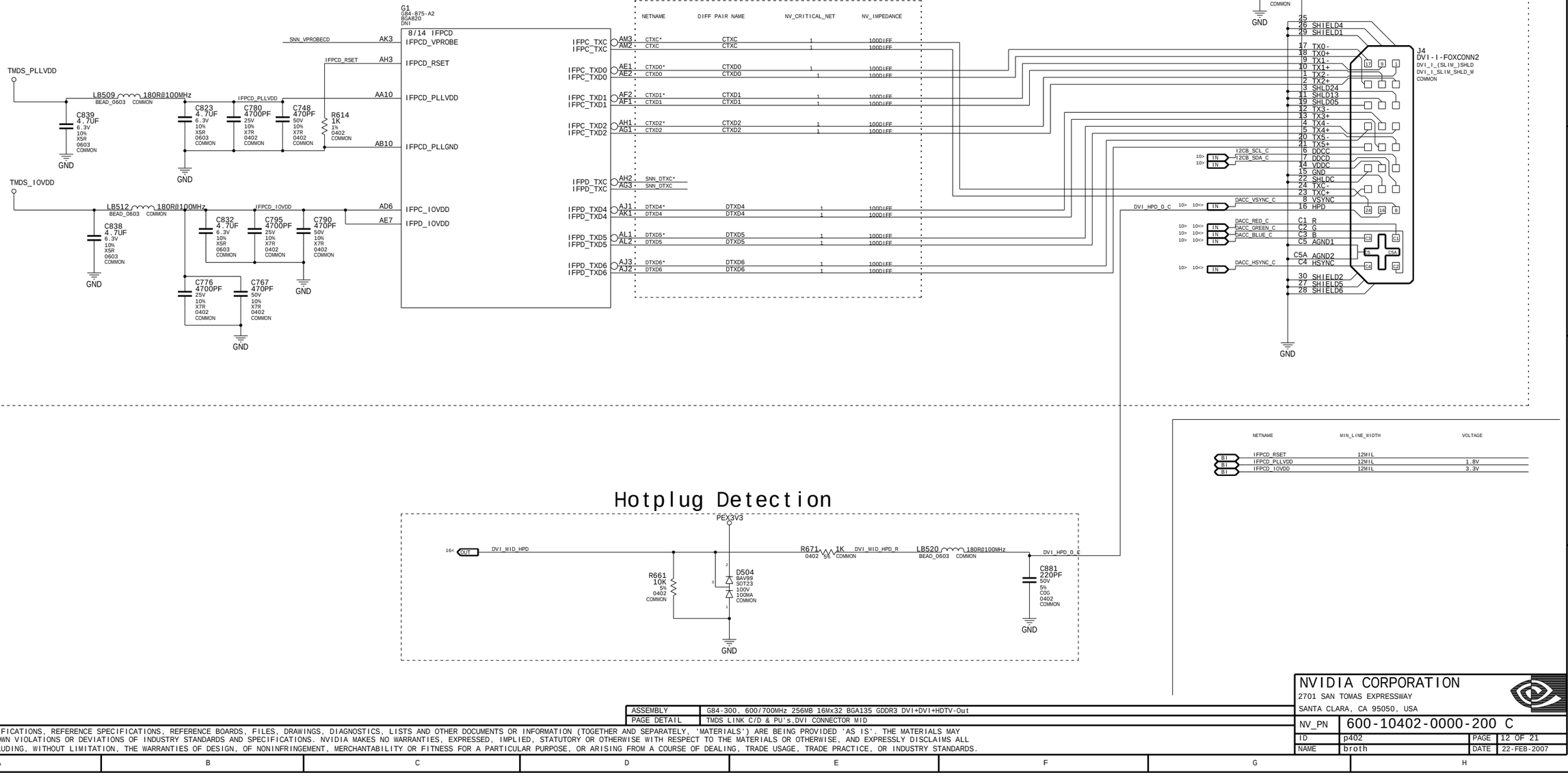

Hotplug Detection

NETNAME	MIN_LINE_WIDTH	VOLTAGE
IFPCD_RSET	12MIL	
IFPCD_PLLVDD	12MIL	1.8V
IFPCD_IOVDD	12MIL	3.3V

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	TMDS LINK C/D & PU's,DVI CONNECTOR MID

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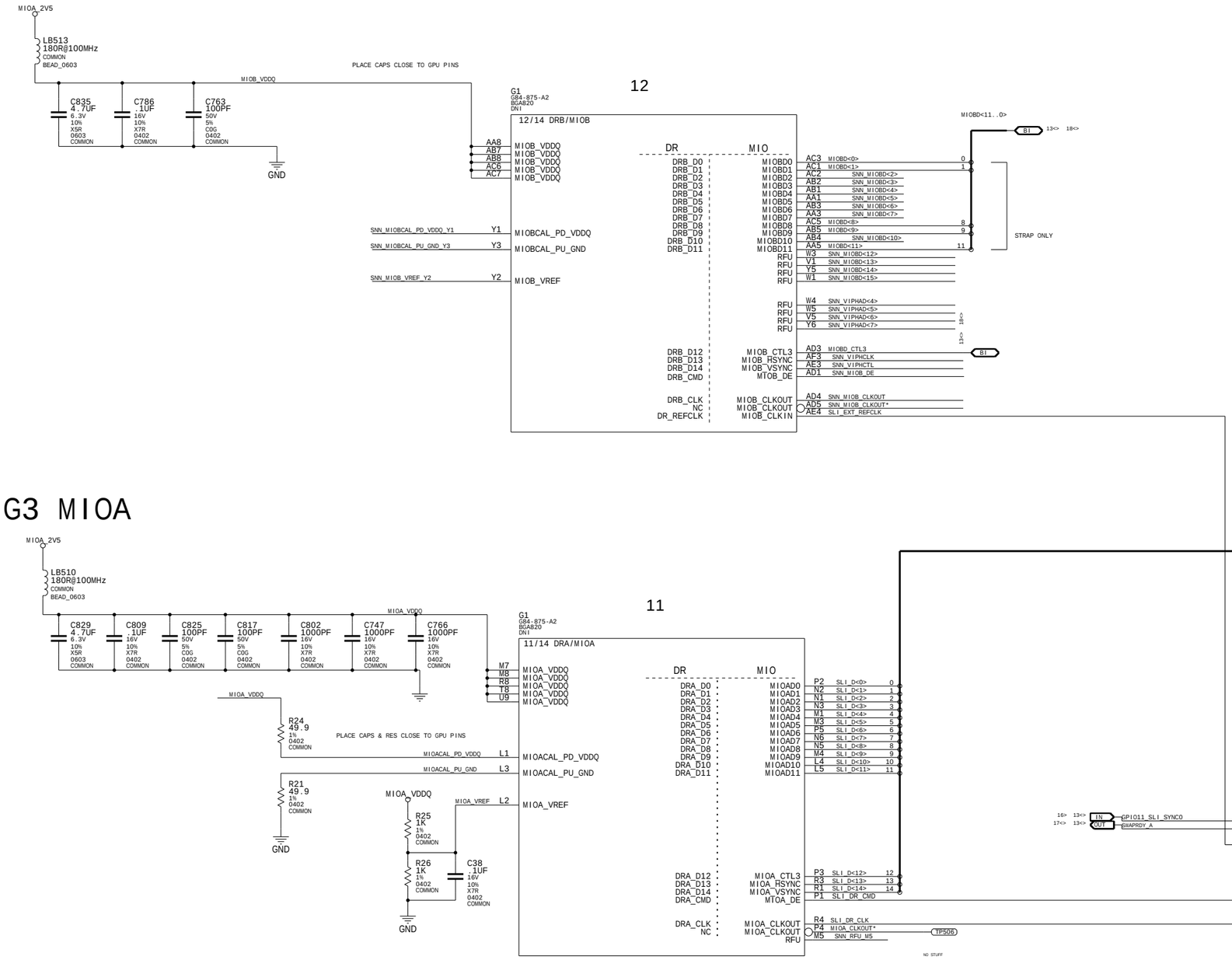
G3 VIP/MIOB



NETNAME	NV_CRITICAL_NET	NV_IMPEDANCE
SLI_D<14..0>	2	50OHM
SLI_DR_CMD	2	50OHM
SLI_DR_CLK	2	50OHM
SLI_EXT_REFCLK	2	50OHM
MIOA_CLKOUT	2	50OHM
GPIO11_SLI_SYNCO	2	50OHM
SWAPRDY_A	2	50OHM

NETNAME	MIN_LINE_WIDTH	
MIOBD<7..0>	2	50OHM
MIOB_VDDQ	12MIL	
MIOB_VREF	12MIL	
MIOBD_CTL3	12MIL	
MIOA_VDDQ	12MIL	
MIOA_VREF	12MIL	

G3 MIOA

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	MIOA & MIOB, SLI CONNECTOR

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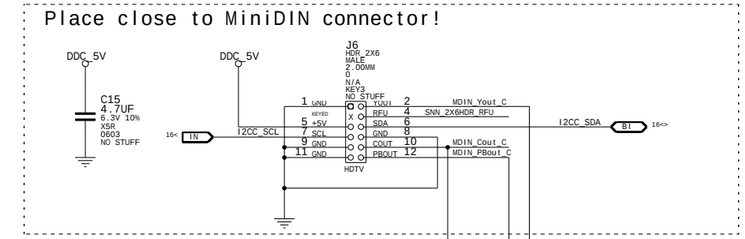
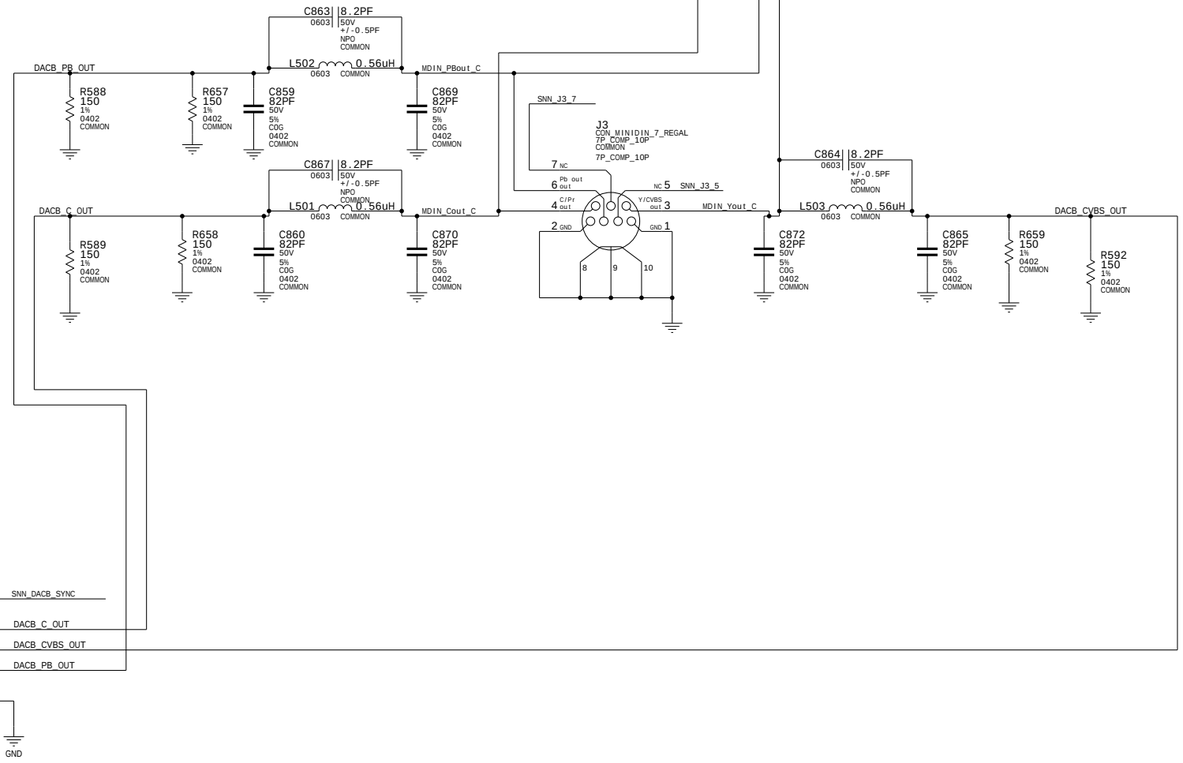
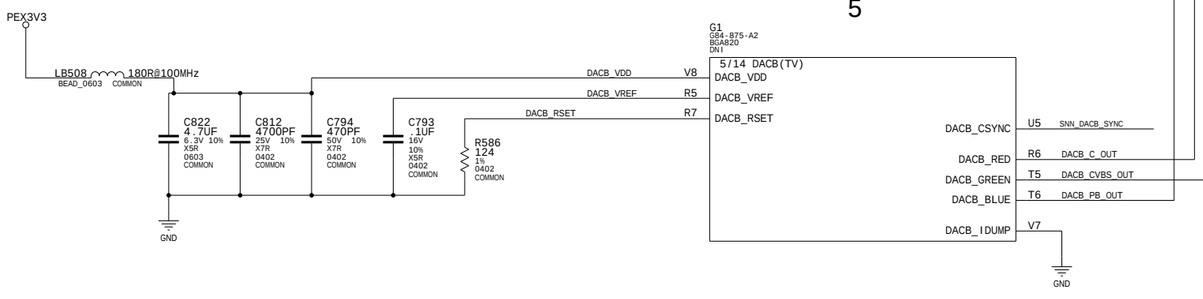
DACB .. MiniDIN VIDEO OUT CONNECTOR

	NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
OUT	DACB_C_OUT		75OHM	1
OUT	DACB_CVBS_OUT		75OHM	1
OUT	DACB_PB_OUT		75OHM	1
BI	MDIN_PBout_C		75OHM	1
BI	MDIN_Cout_C		75OHM	1
BI	MDIN_Yout_C		75OHM	1
IN	DACB_VDD	12MIL		
IN	DACB_VREF	12MIL		
IN	DACB_RSET	12MIL		







ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	DACB FILTERS, MINIDIN CONNECTOR NORTH, COMPONENT VIDEO OUTPUT CONNECTOR

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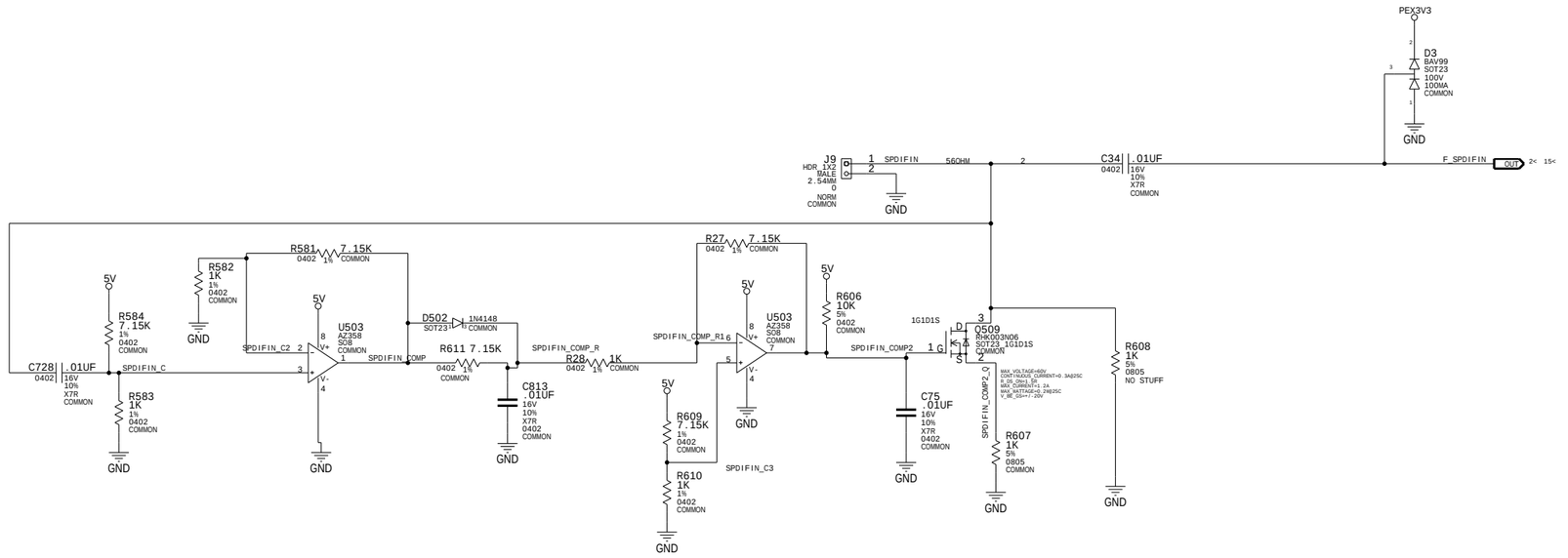
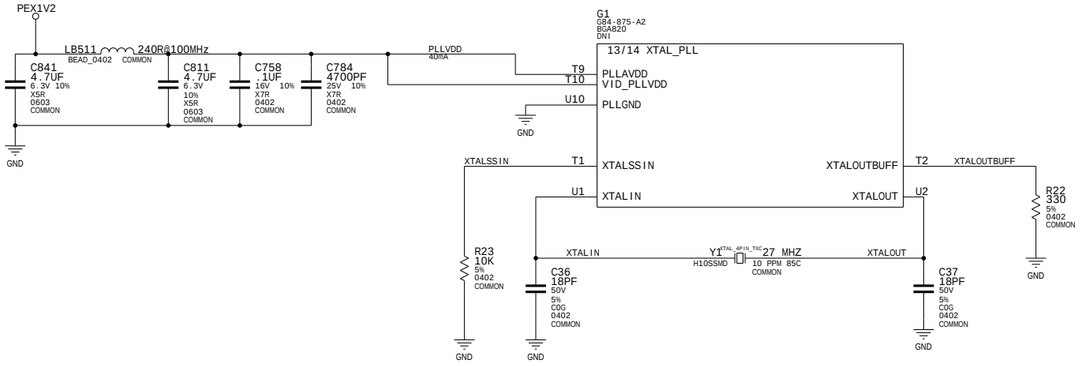
XTAL/PLLVDD/SPDIF IN

SPDIF IN



XTAL/PLLVDD

13



NETNAME		MIN_LINE_WIDTH	
XTALIN	IN	10MIL	
XTALOUT	IN	10MIL	
PLLVDD_R	IN	12MIL	
PLLVDD	IN	12MIL	
VID_PLLVDD	IN	12MIL	
XTALSSIN	IN	10MIL	
XTALOUTBUFF	IN	10MIL	
SPDIFIN	IN	56OHM	2
SPDIFIN_C	IN	56OHM	2
SPDIFIN_C2	IN	56OHM	2
SPDIFIN_COMP	IN	56OHM	2
SPDIFIN_COMP_R	IN	56OHM	2
SPDIFIN_COMP_R1	IN	56OHM	2
SPDIFIN_C3	IN	56OHM	2
SPDIFIN_COMP2	IN	56OHM	2
SPDIFIN_COMP2_Q	IN	56OHM	2
F_SPDIFIN	IN	56OHM	2

15> 2<

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	SPDIF-IN HEADER, XTAL

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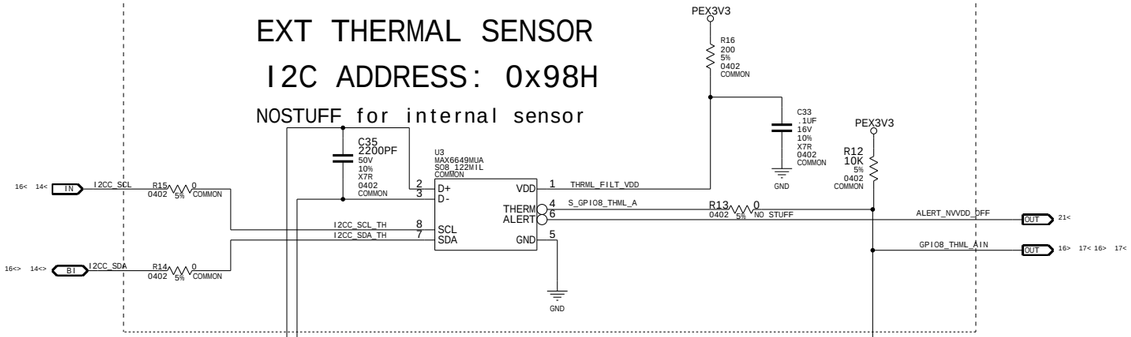
NETNAME	MIN_LINE_WIDTH	VOLTAGE
BI THERMDC	10MIL	
BI THERMDA	10MIL	
BI FAN_PWM	12MIL	
BI FAN_PWM_B	12MIL	
BI FAN_PWM_C	12MIL	
BI FAN_PWM_D	12MIL	

EXT THERMAL SENSOR

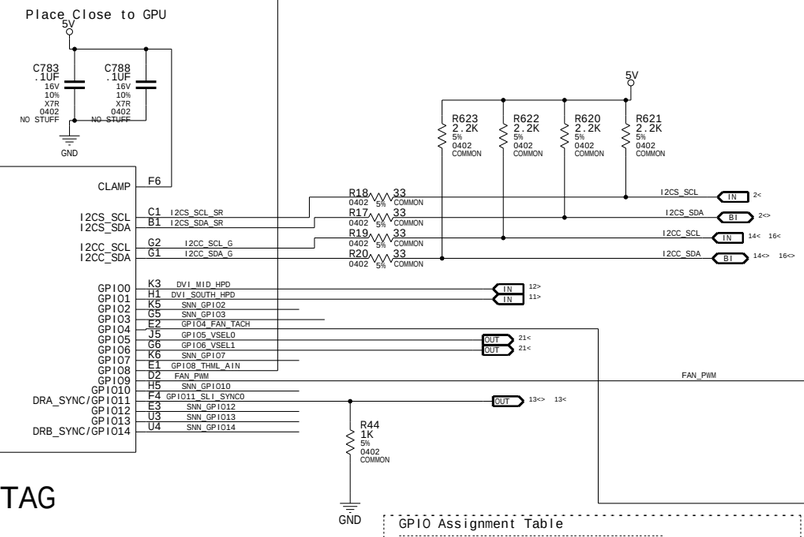
I2C ADDRESS: 0x98H

NOSTUFF for internal sensor

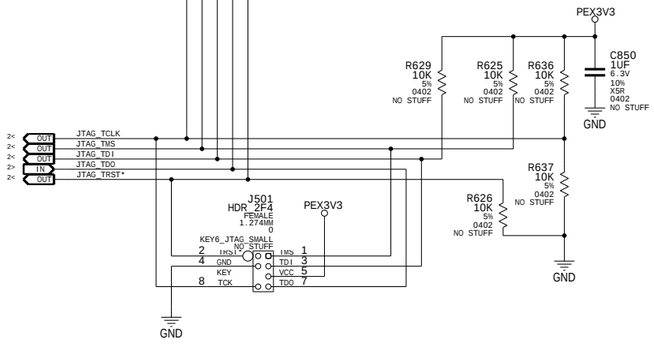


Use 10MIL Guard(GND) Trace around THERMDC and THERMDA

Place Close to GPU

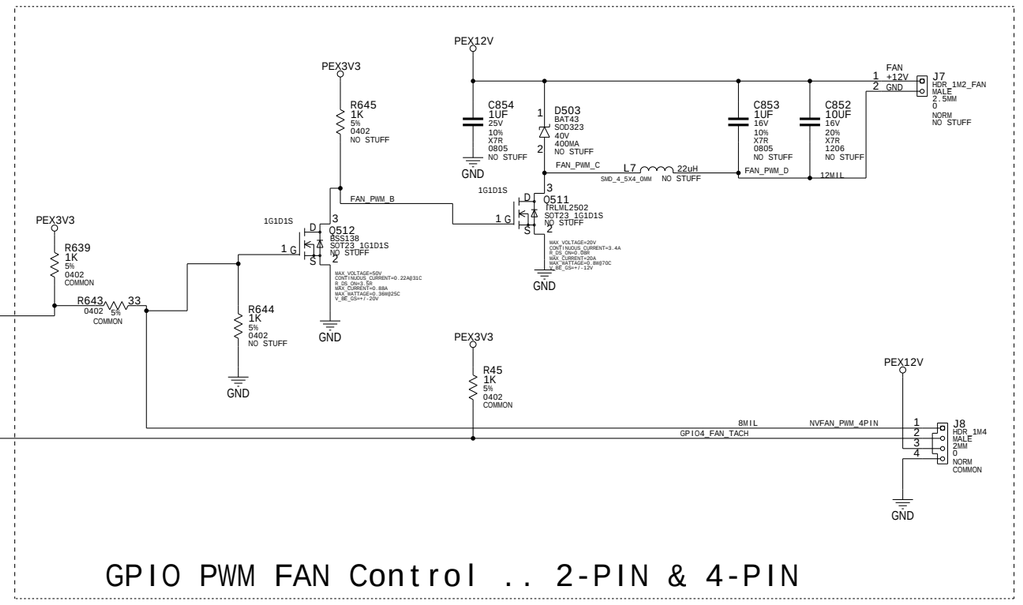


GPIO & JTAG



GPIO Assignment Table

GPIO	I/O	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	DVI SOUTH HOTPLUG DET
2	IN/OUT	RESERVED
3	IN	G84 THERMAL ODS IN
4	IN	FAN_TACH
5	OUT	NVVDD VOLTAGE SELECT 0
6	OUT	NVVDD VOLTAGE SELECT 1
7	OUT	RESERVED
8	IN	THERMAL ALERT IN
9	OUT	PWM FAN
10	OUT	RESERVED
11	OUT	SLI_SYNC0
12	OUT	RESERVED
13	IN	RESERVED
14	IN	RESERVED



GPIO PWM FAN Control .. 2-PIN & 4-PIN

ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	EXTERNAL THERMAL SENSOR, 2PIN / 4PIN FAN CONTROL, GPIO

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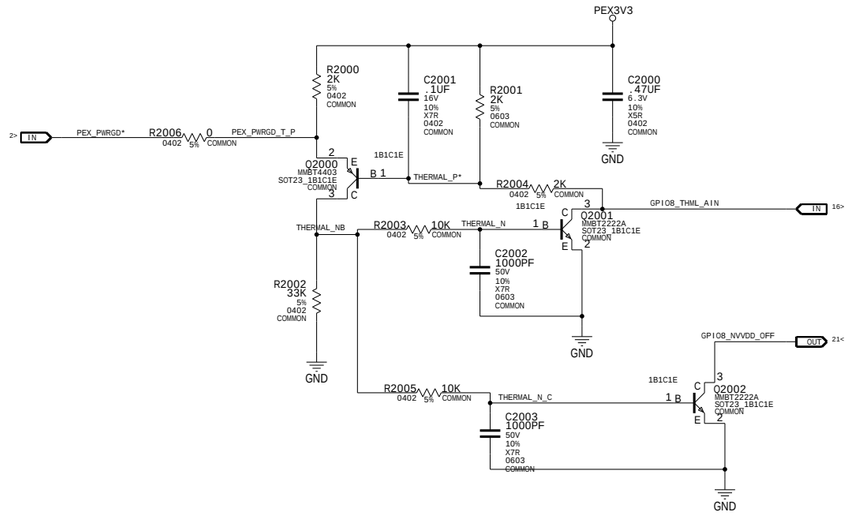
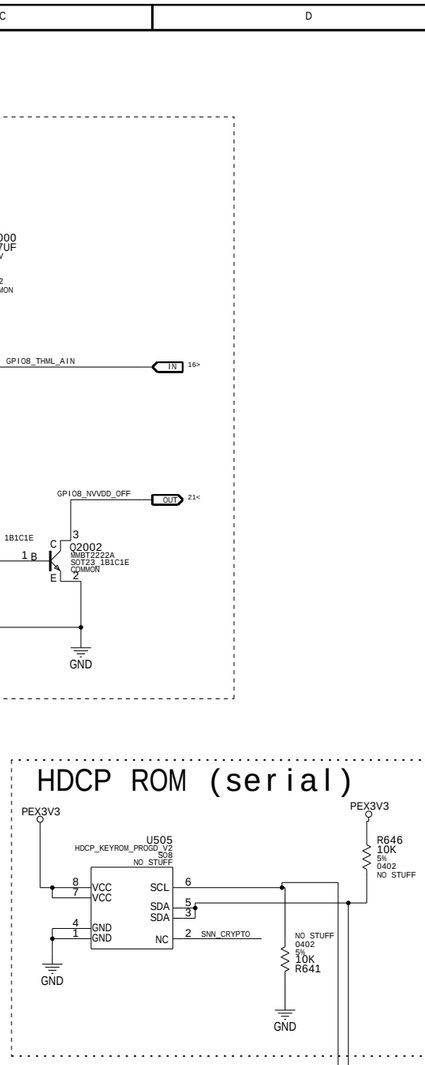
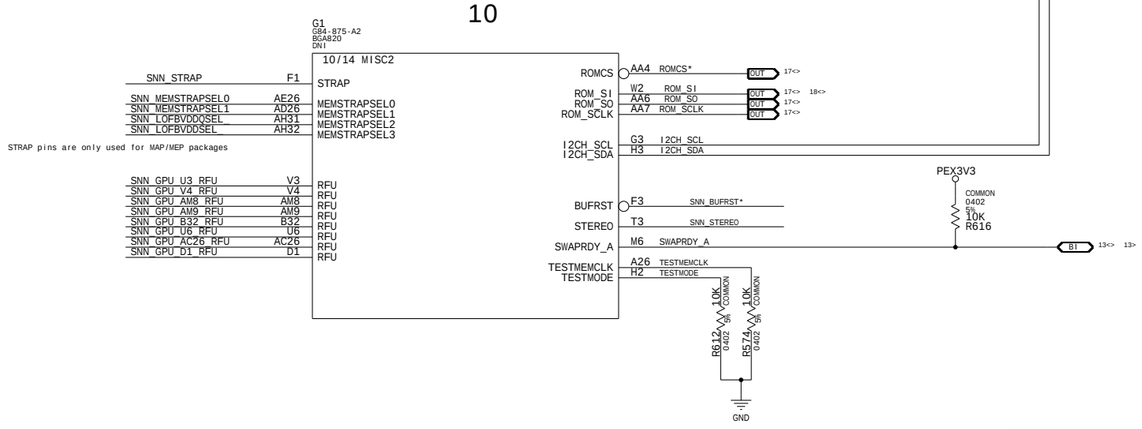
Thermal Protection



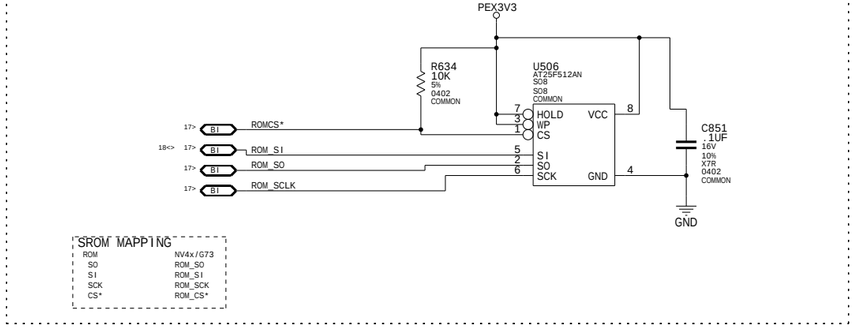
HDCP ROM (serial)



10



BIOS ROM(serial)



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	BIOS ROM, HDCP ROM

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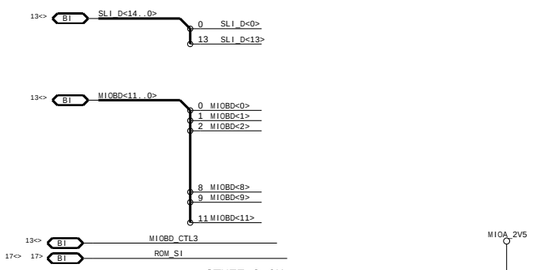
BIOS, Straps, Misc

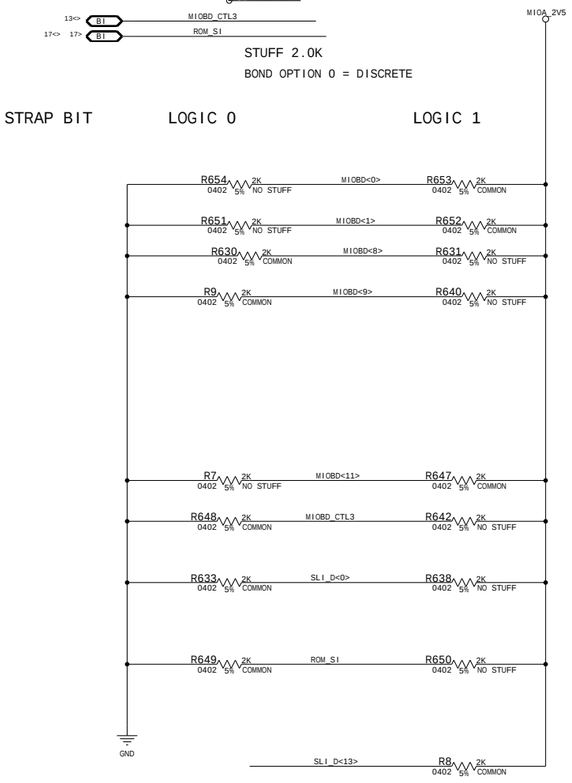
STRAPS

Assembly: BIOS



STUFF 2.0K

BOND OPTION 0 = DISCRETE



REG: NV_STRAP_0

RAM_CFG_0

RAM_CFG_1

RAM_CFG_2

RAM_CFG_3

PCI_DEVID_0

PCI_DEVID_1

PCI_DEVID_2

PCI_DEVID_3

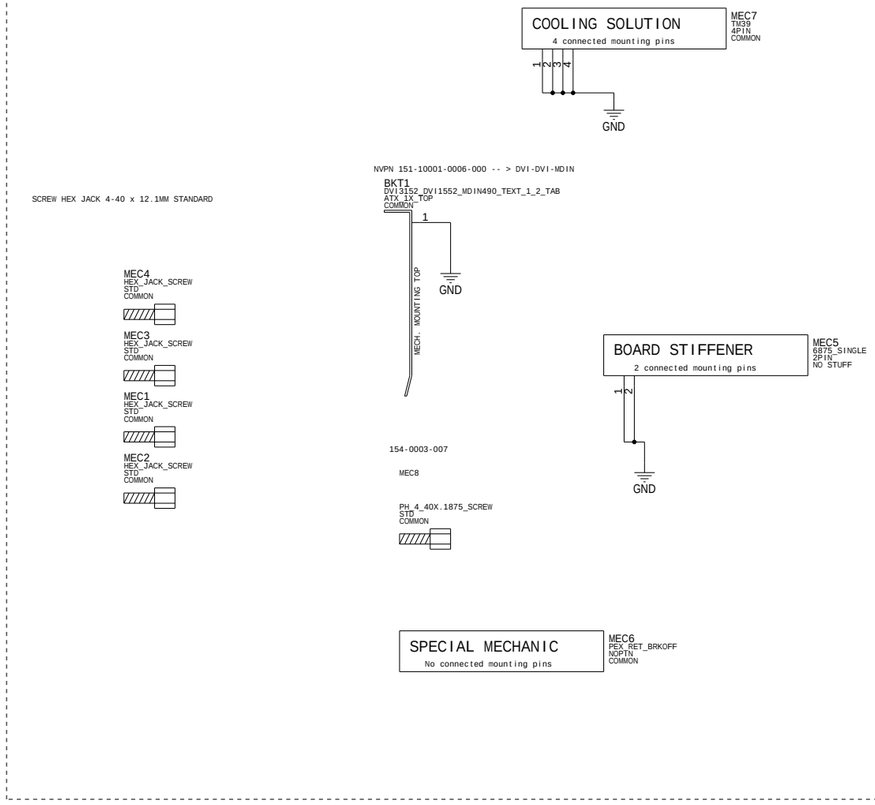
PCI_DEVID_EXT (4)

PEX_PLL_EN_TERM100

MIO_EN_33V_0

Slot Clock Configuration

MECHANICALS & THERMALS



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	BIOS STRAPS & MECHANICALS

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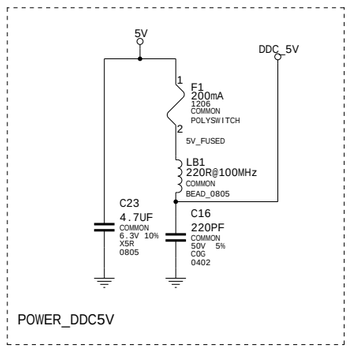
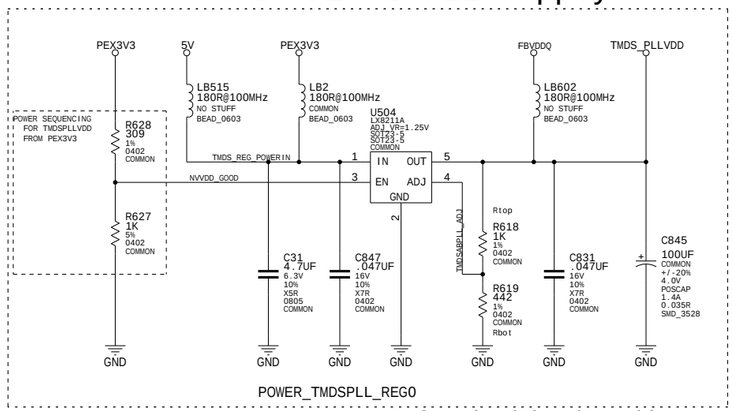
Power Supply ... TMDS, MIOA_VDDQ, DDC5V

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
BI 5V_FUSED	1A	12MIL	5V
DDC_5V		12MIL	5V
5V	1A		5V
BI TMDSABPLL_ADJ		10MIL	3.3V
TMDS_PLLVDD		12MIL	1.8V
MIOA_2V5	1A	12MIL	2.5V
GND		16MIL	0V

DDC 5V

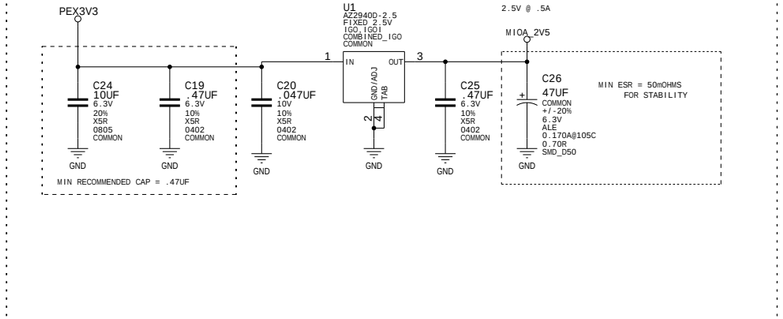


TMDS AB/CD PLL Supply



$$Vout = VRef * (1+(Rbot/Rtop))$$
$$1.8V = 1.25V * (1+(442/1000))$$

MIOA_VDDQ



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	POWER SUPPLY LINEARS: DDC5V, TMDS PLLVDD, DACB VDD, MIOA_VDDQ

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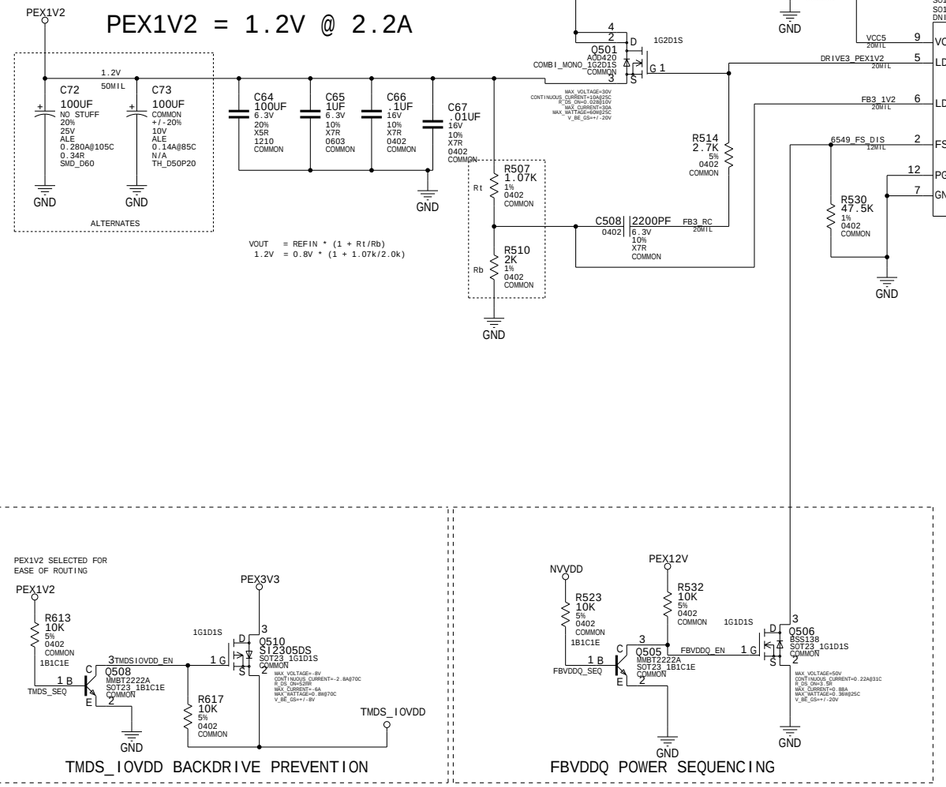
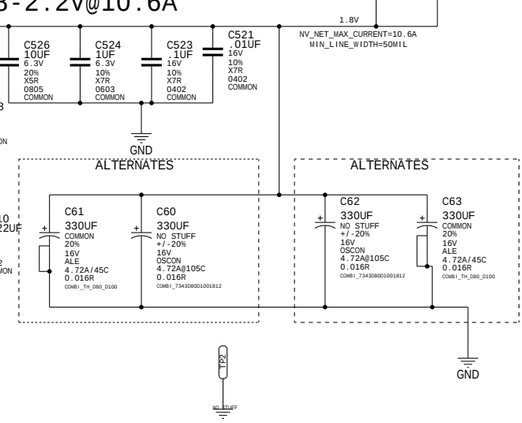
POWER SUPPLY .. FBVDDQ, PEX1V2

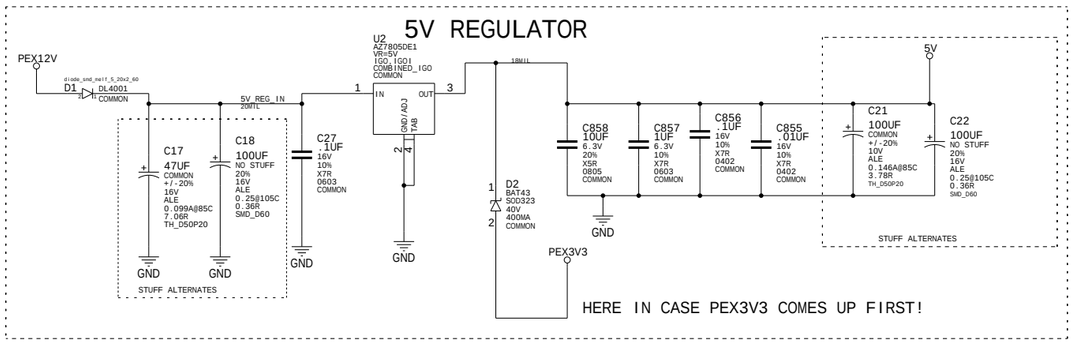
PEX1V2 = 1.2V @ 2.2A



FBVDDQ: 1.8-2.2V@10.6A



5V REGULATOR



ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	POWER SUPPLY: 5V, TMDSIOVDD, PEX1V2 AND FBVDDQ SWITCHER

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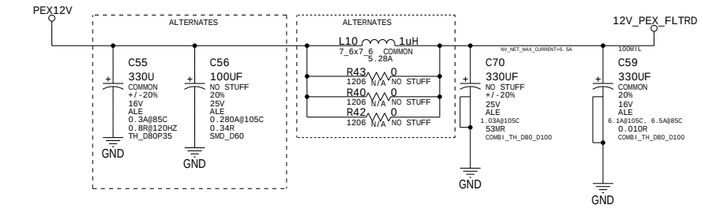
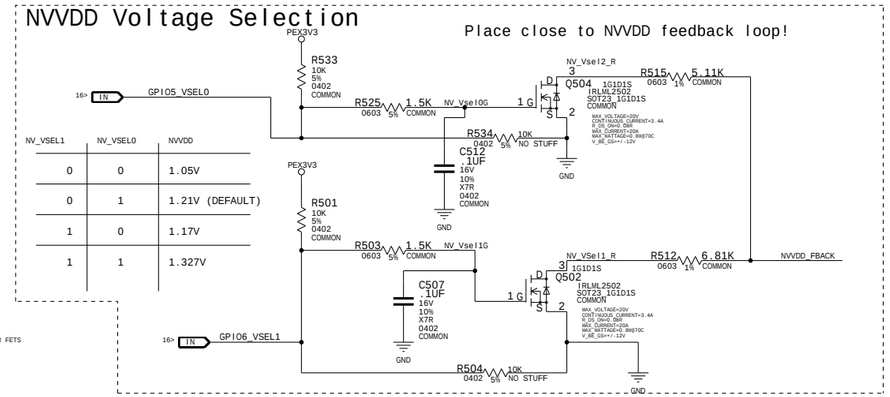
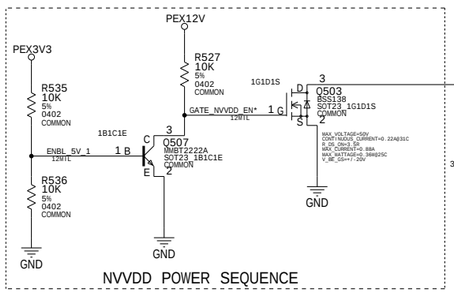
NVVDD POWER SUPPLY







ASSEMBLY	G84-300, 600/700MHz 256MB 16Mx32 BGA135 GDDR3 DVI+DVI+HDTV-Out
PAGE DETAIL	POWER SUPPLY: SINGLE PHASE NVVDD, NVVDD SET CONTROL

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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