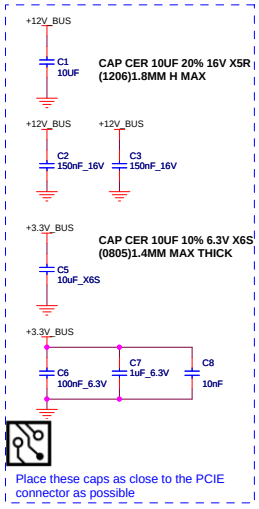
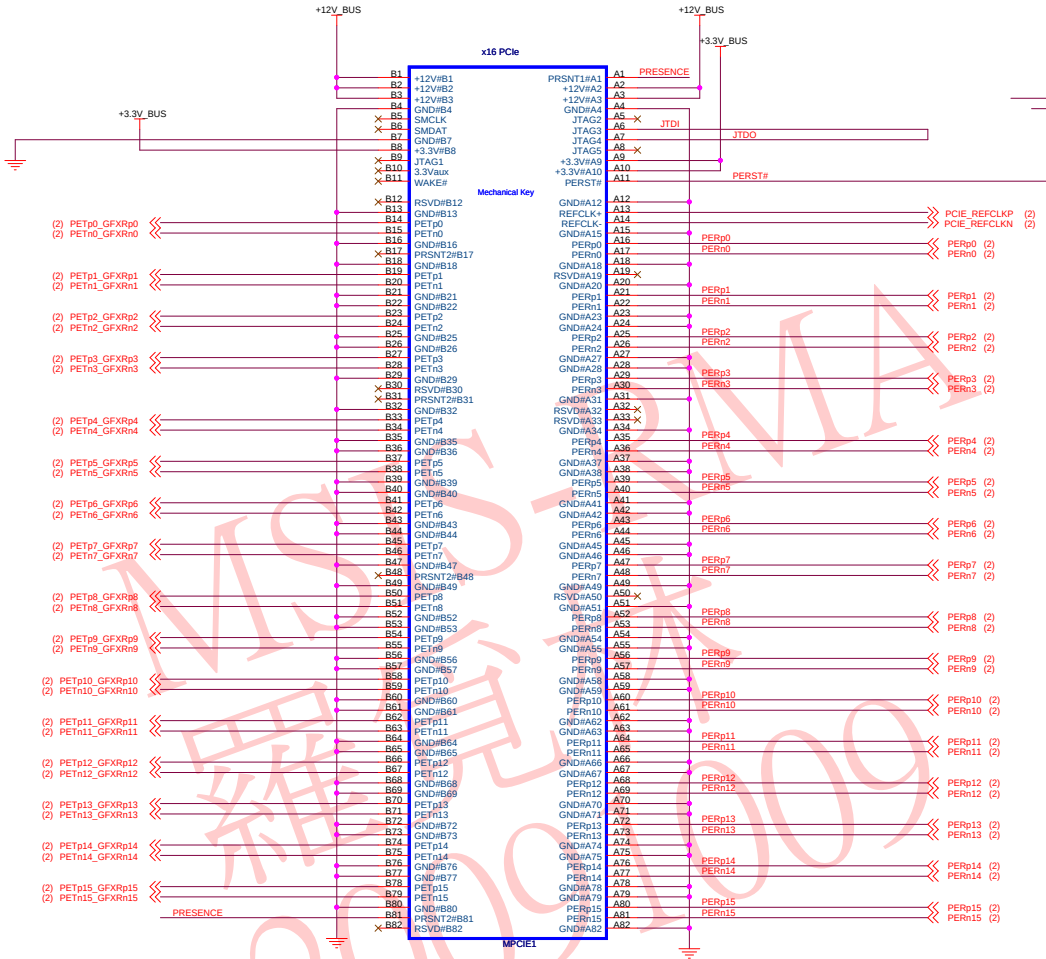
PCI-EXPRESS EDGE CONNECTOR





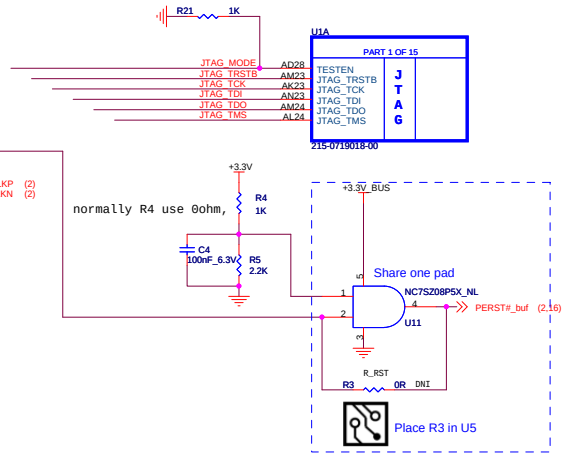


Table 1: Connection for JTAG

Production (No JTAG)	**Install R1, R2 & Don't Install TSW1**	
Internal Use Only	**Install TSW1 & Don't Install R1 & R2**	
	JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open**
	NO JTAG	**TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)**

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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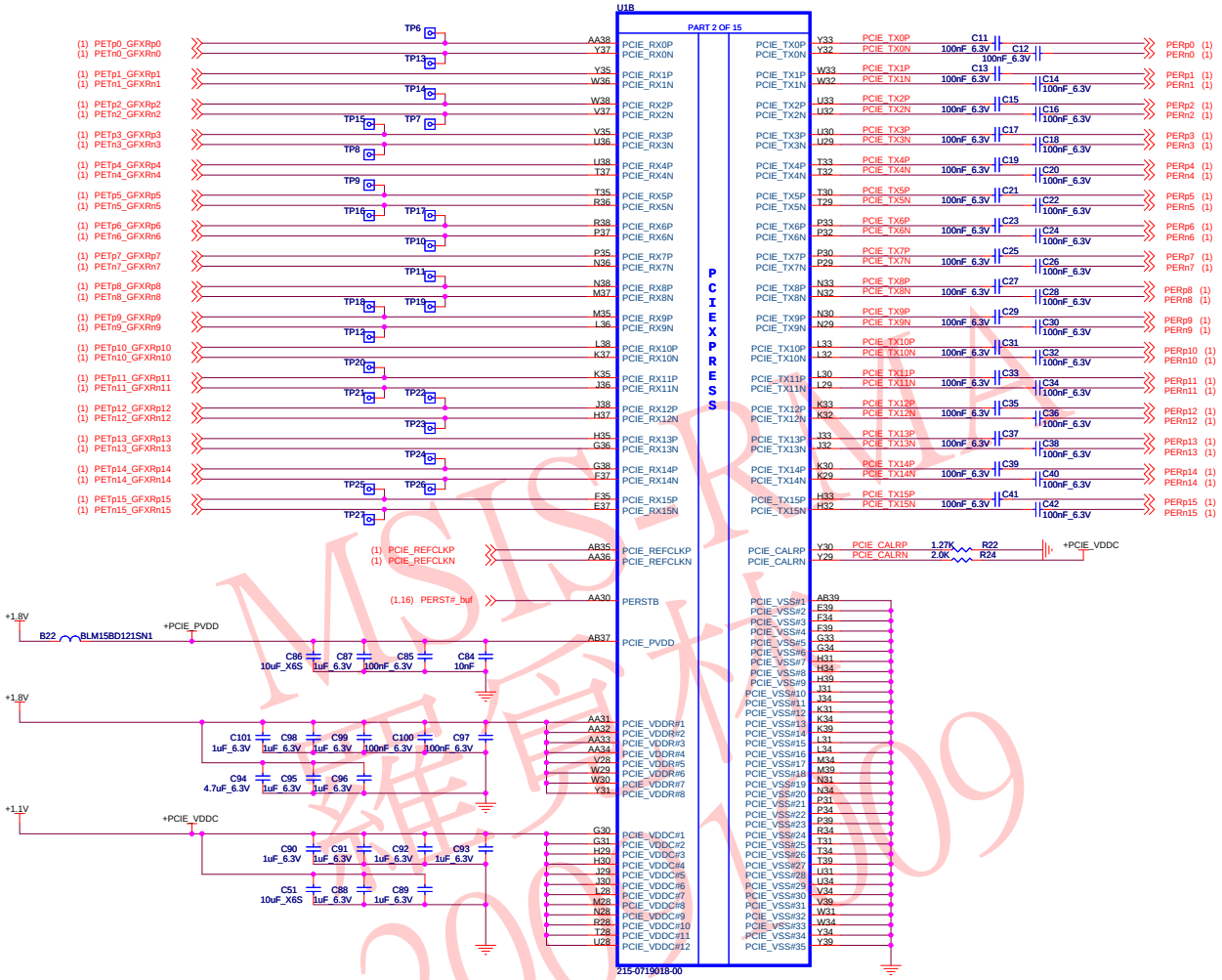
(2) RV730 PCIE Interface

NOTE: some of the PCIE testpoints will
be available trought via on traces.



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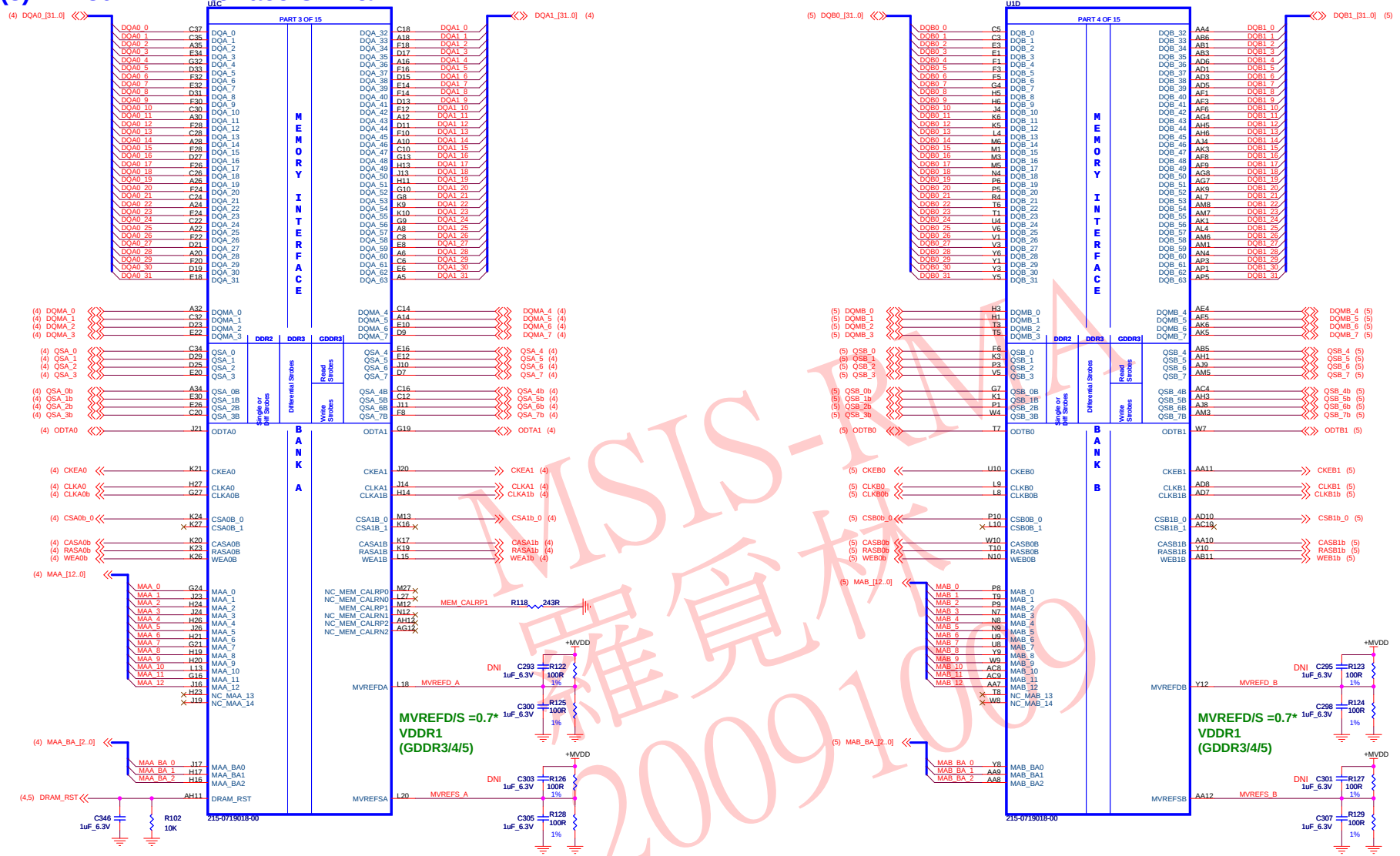
(3) RV730 MEM Interface Ch A&B



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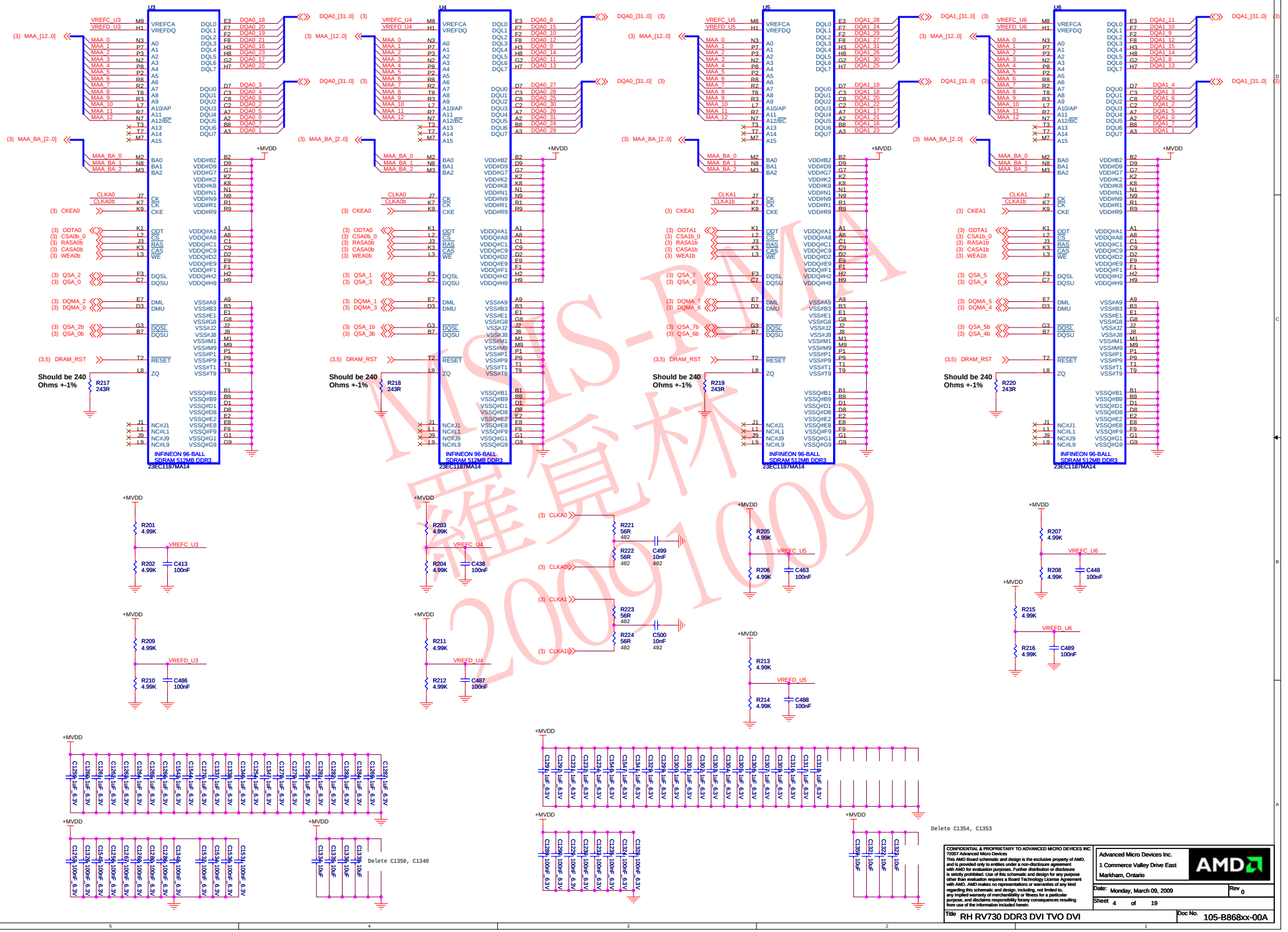
(4) DDR3 Memory Channel A



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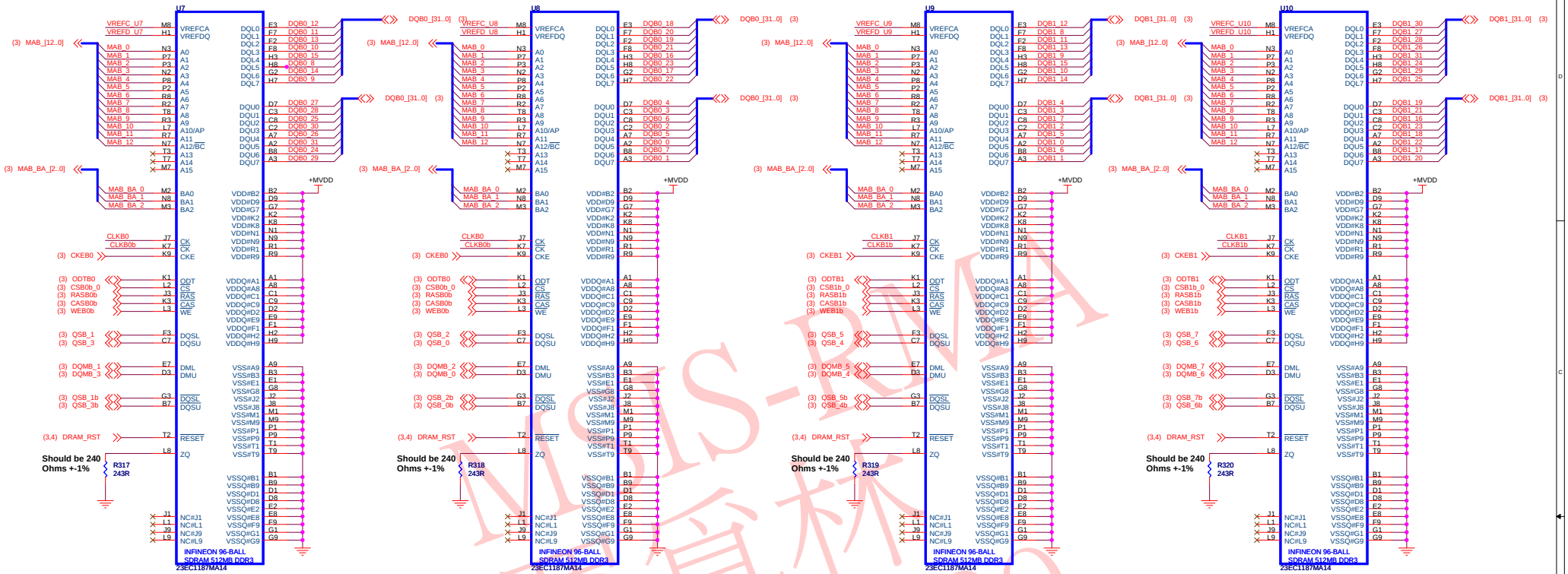
(5) DDR3 Memory Channel B



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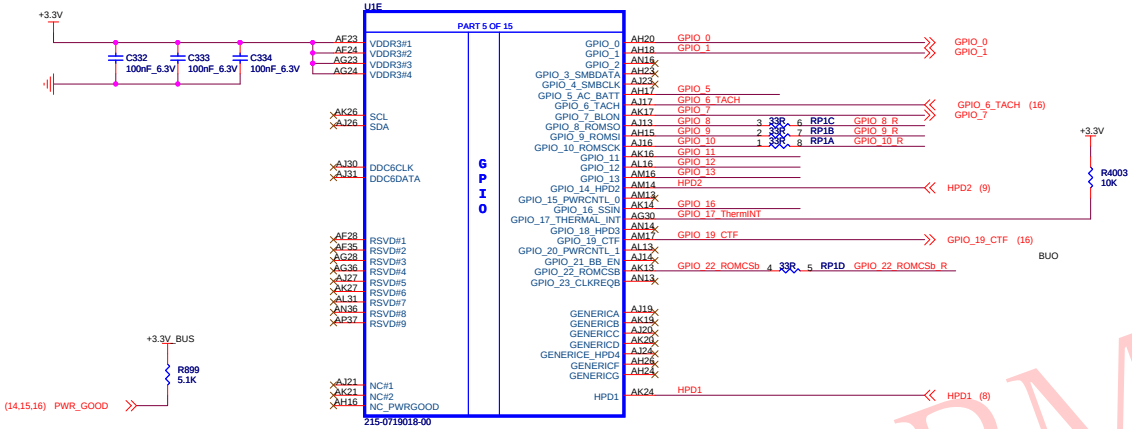
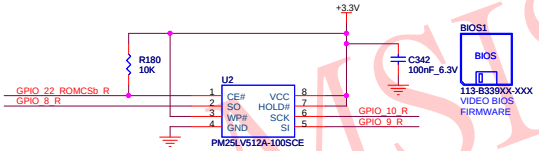
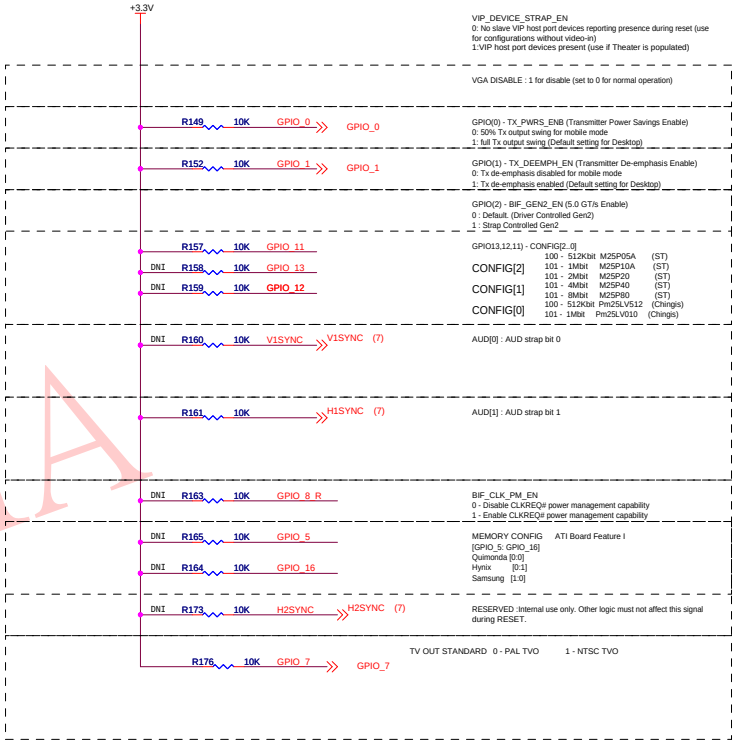
(06) RV730 GPIOs Strap CF XTAL

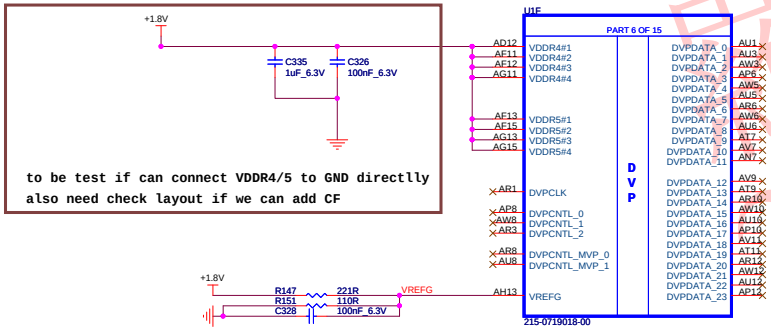


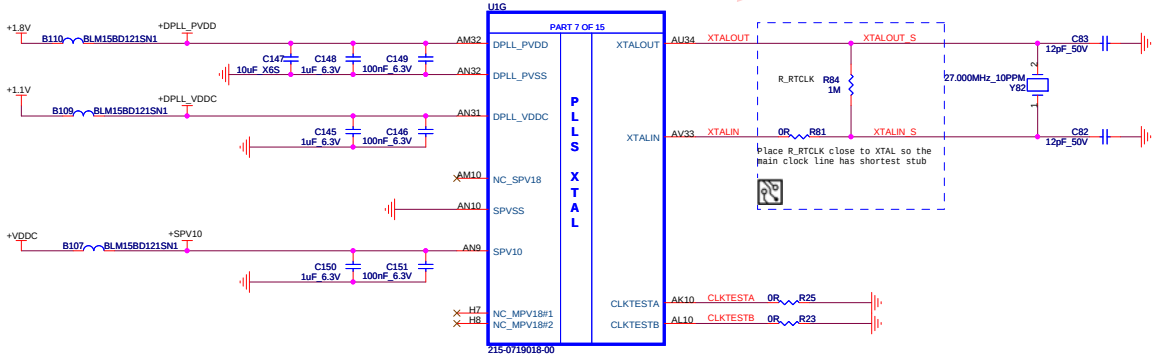


PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

PIN BASED STRAPS







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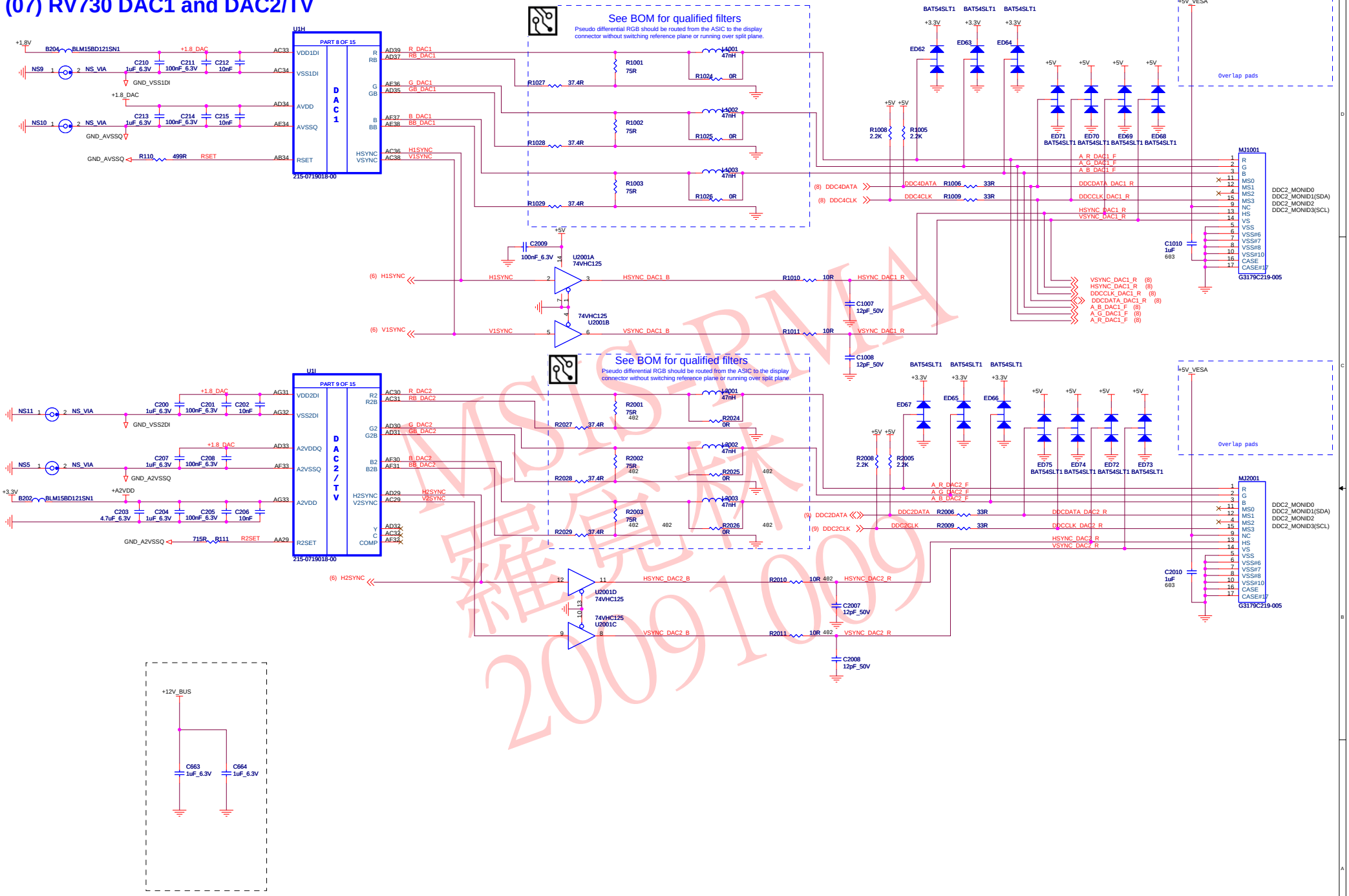
(07) RV730 DAC1 and DAC2/TV



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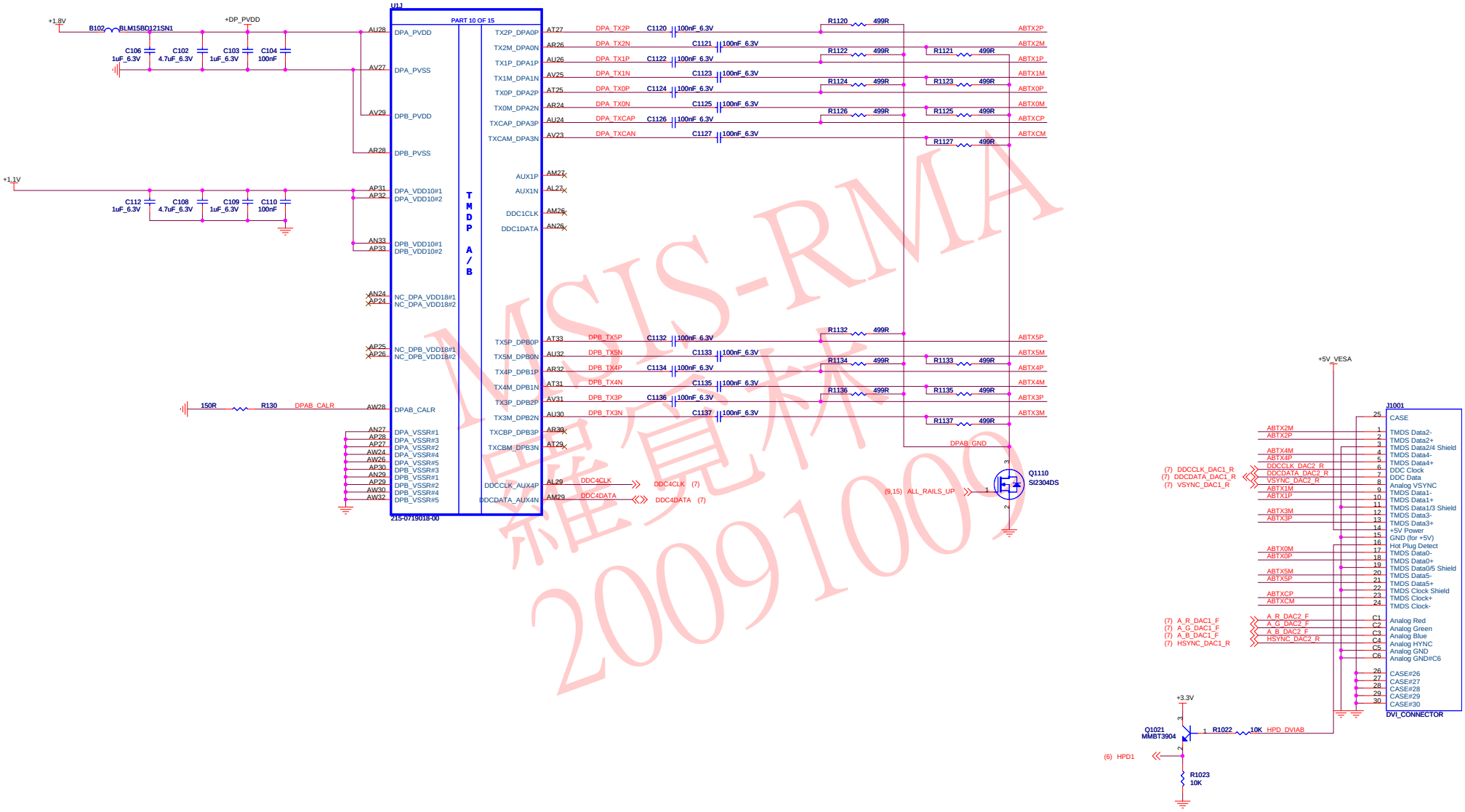
(08) RV730 TMDS A&B



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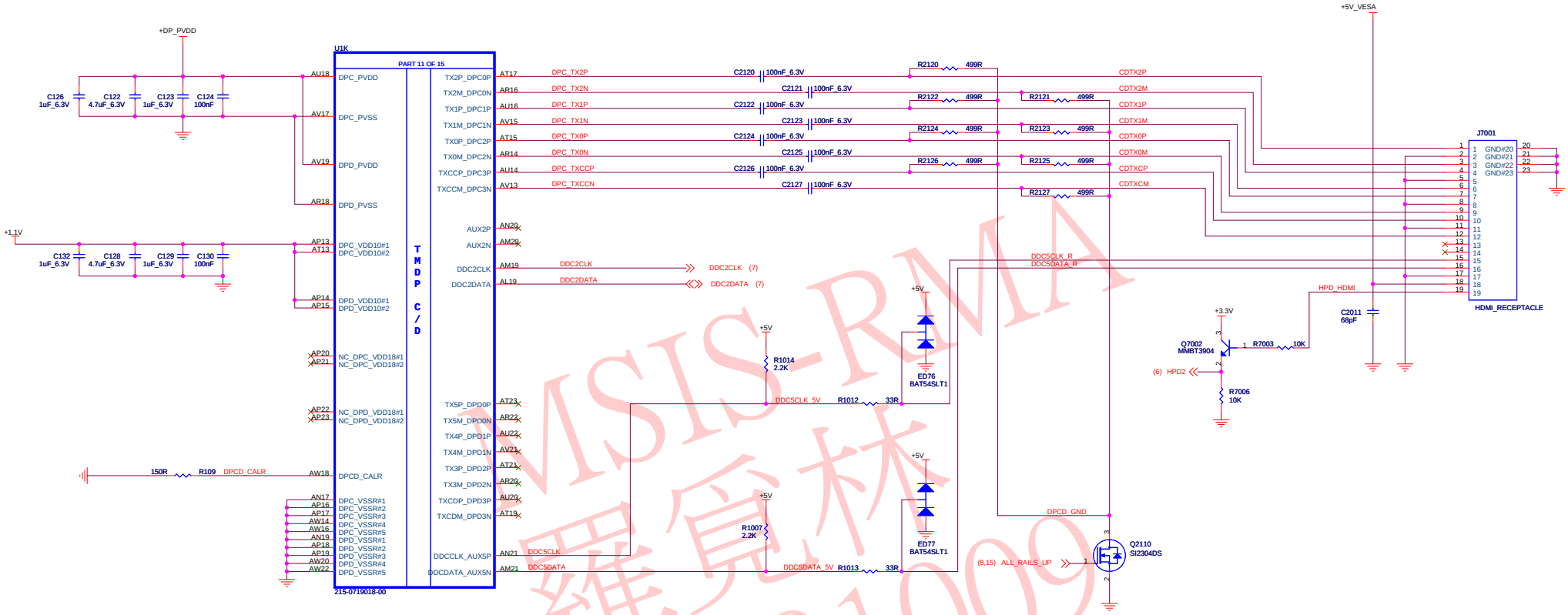
(09) RV730 Display Port C&D



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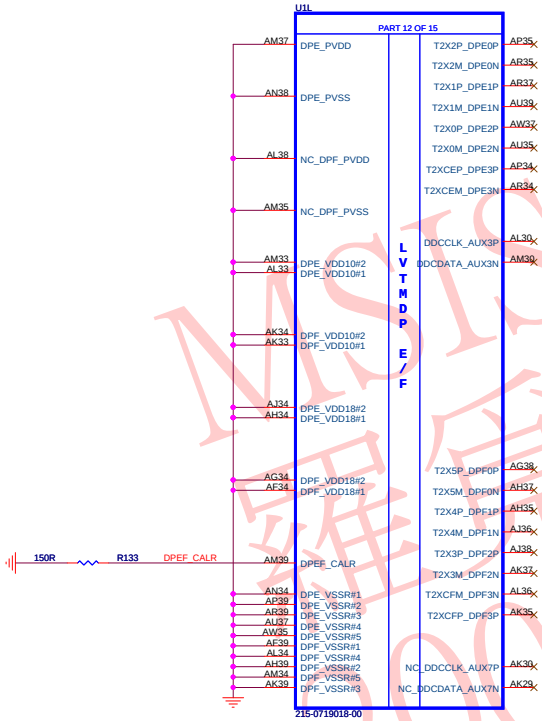
(10) No Connect E&F



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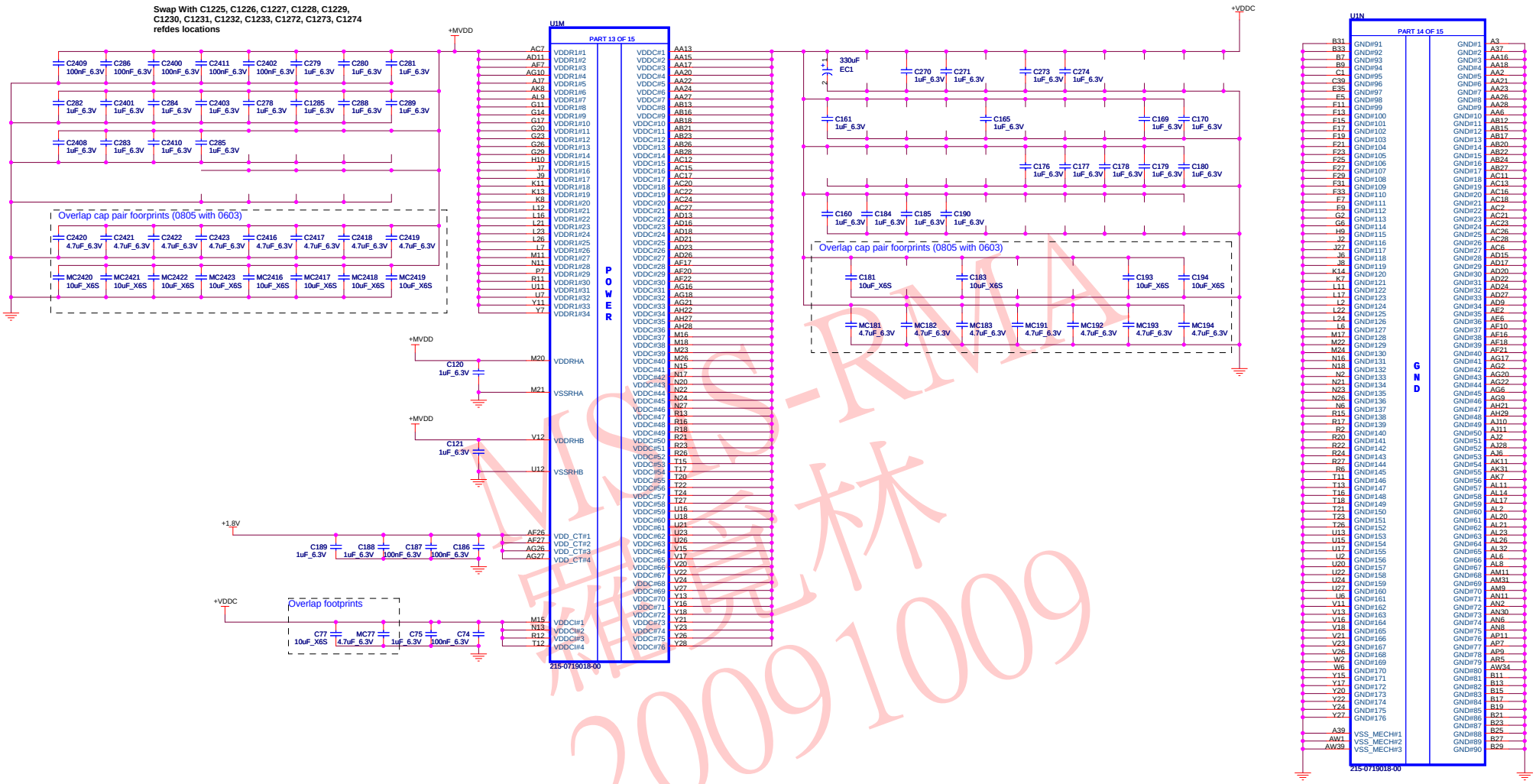
(11) RV730 Power & GND



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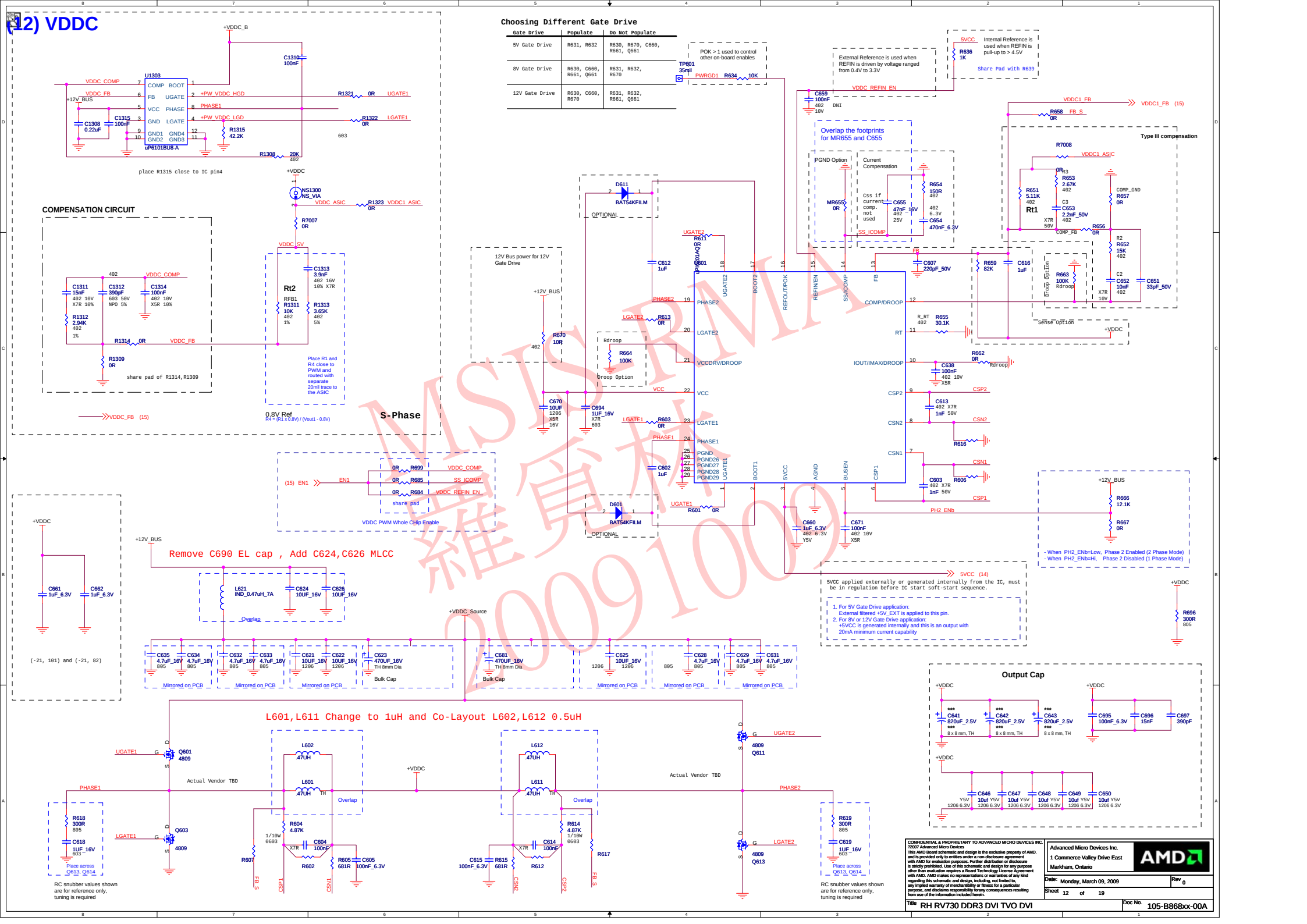
(12) VDDC

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661



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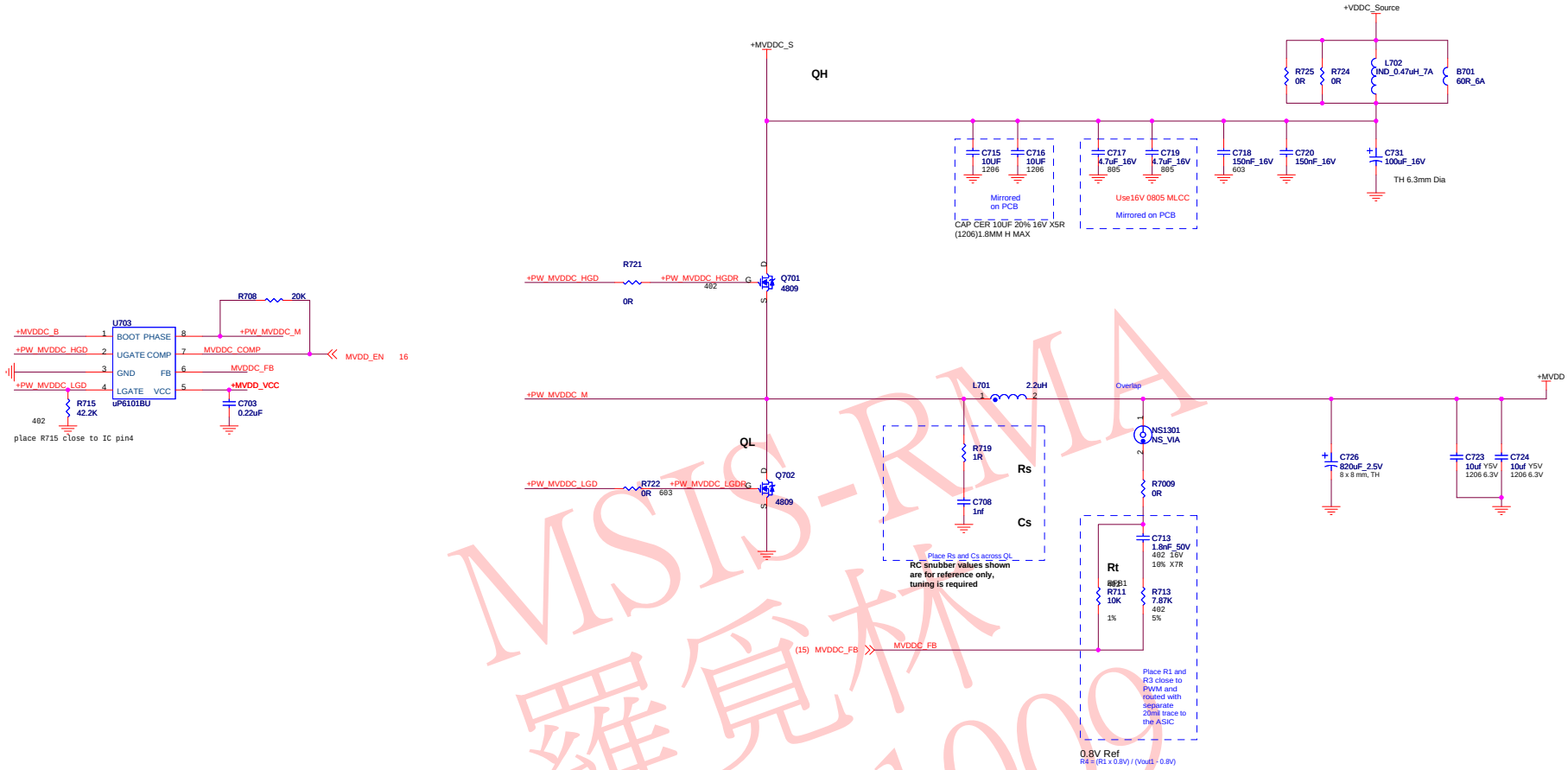
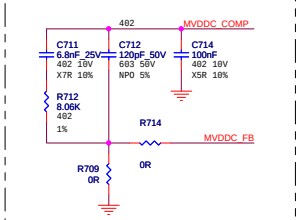
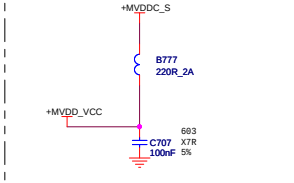
(13) MVDD



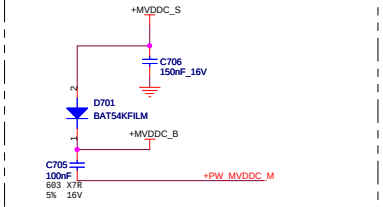
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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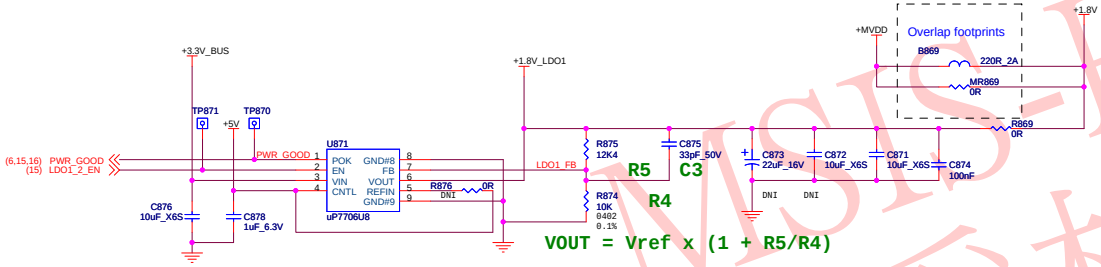
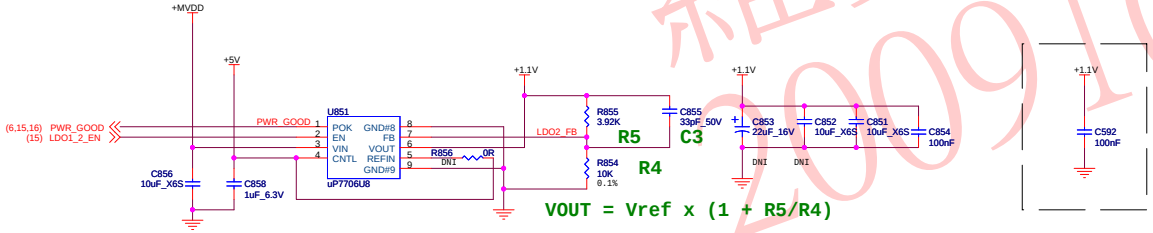
(14) Linear Regulators

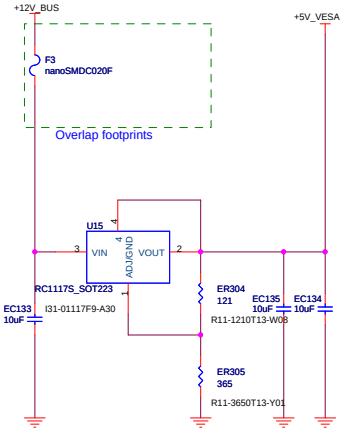
Regulators for +5V, +5V_VESA and +5V_VESA2

LDO #1: Vin = 3.0V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 1.0A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

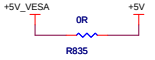


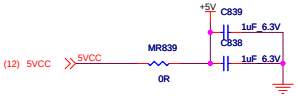
LDO #2: Vin = +1.5V to 2.0VMAX Vout = +1.1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling





Vout=1.25V* [1+(ER305/ER304)]





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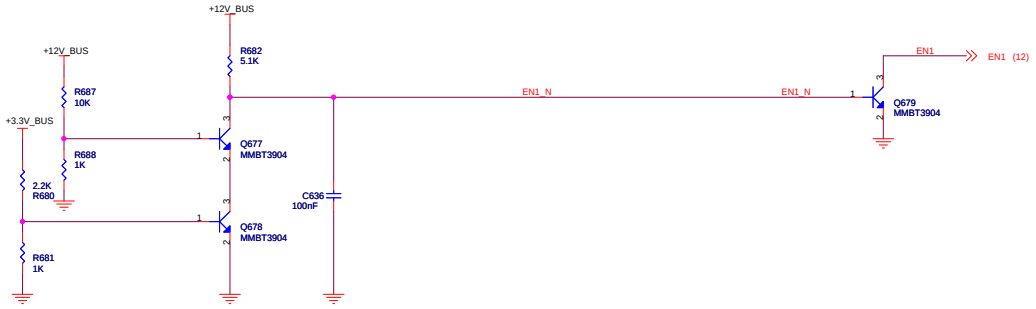
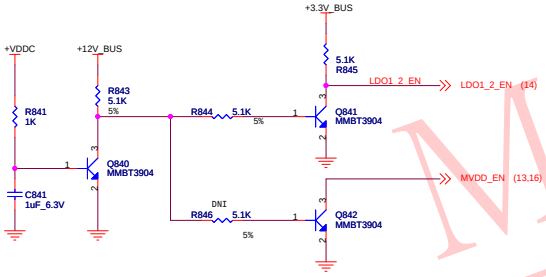
(15) Power Management

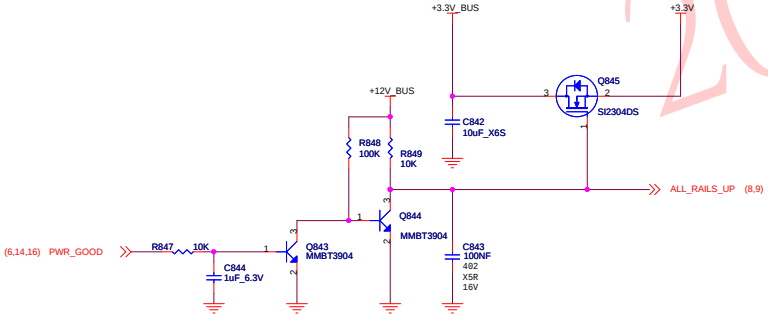
Power up Sequencing



VDDC Enable Circuit



LDOs and MVDD Enable Circuit

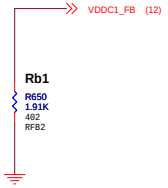


3.3V Enable Circuit

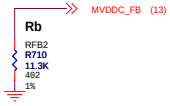
Power Play

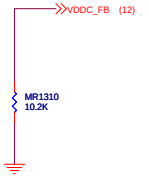
VDDC Voltage Settings Using GPIOs (for VDDC1 Dual Phase)

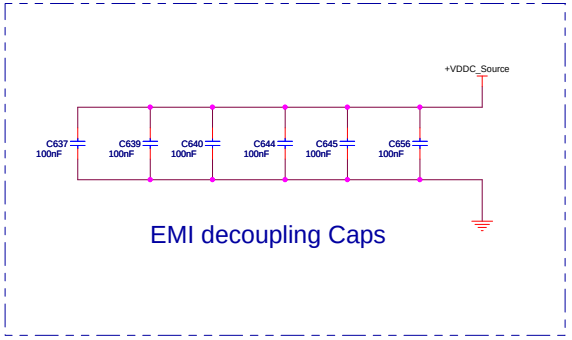
PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1=82.5K Rf2=63.4K	Rf1= Rf2=	Rf1= Rf2=	
0	0	0.90V			
0	1	1.00V			
1	0	1.03V			
1	1	1.125V			Power-up Default



Resistors to set the output voltages for +VDDC and +MVDDC







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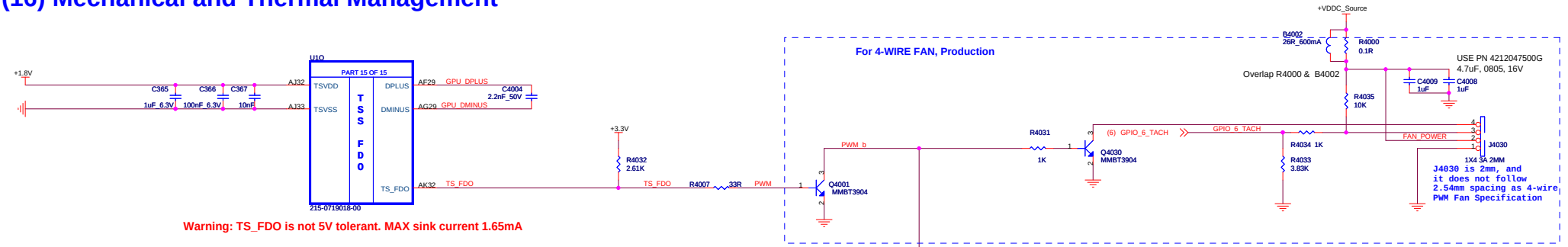
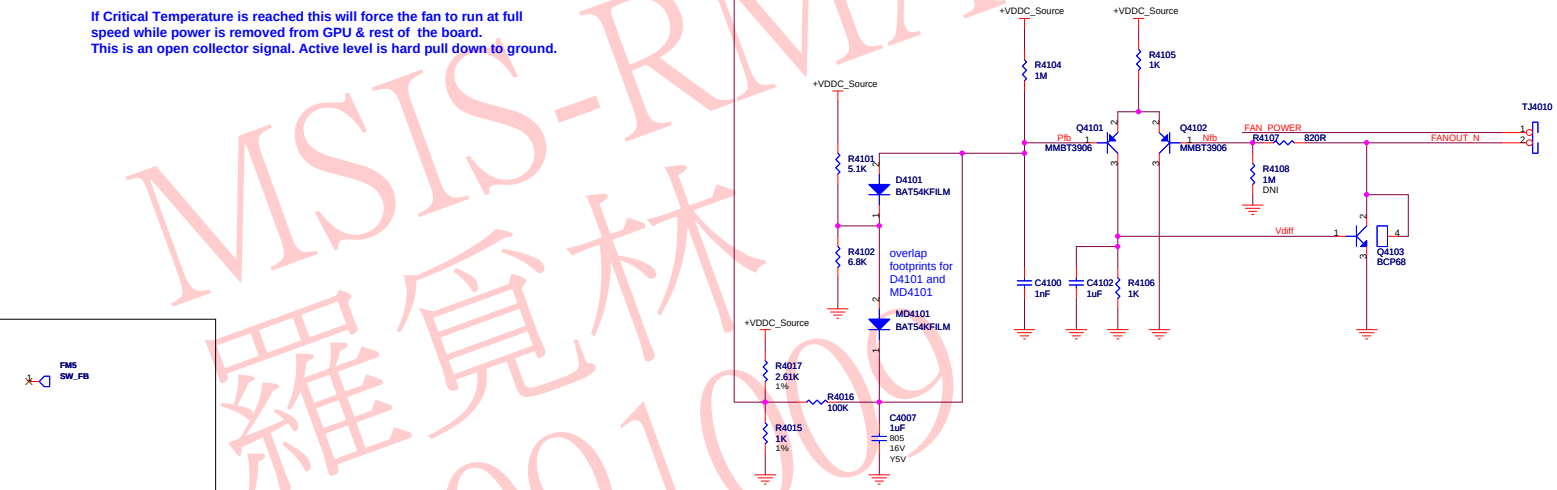
(16) Mechanical and Thermal Management

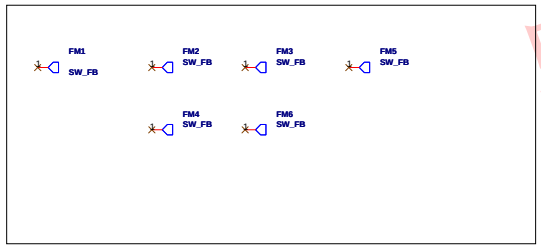


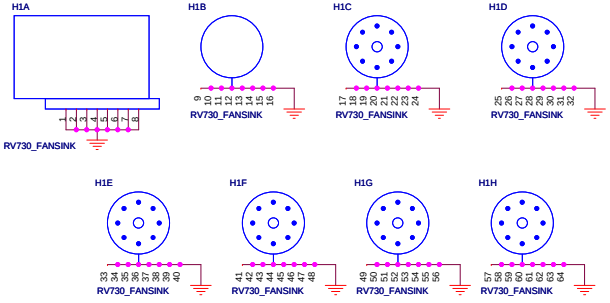
Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

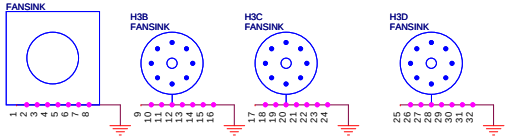
If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.

For 2-WIRE FAN, Socket Board Only

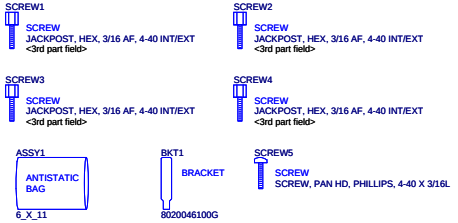




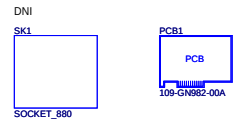




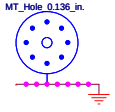
DVI/DVI SCREWS with top tab



Need New Bracket



RV635 Socket



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Title RH RV730 DDR3 DVI TVO DVI

Doc No. 105-B868xx-00A

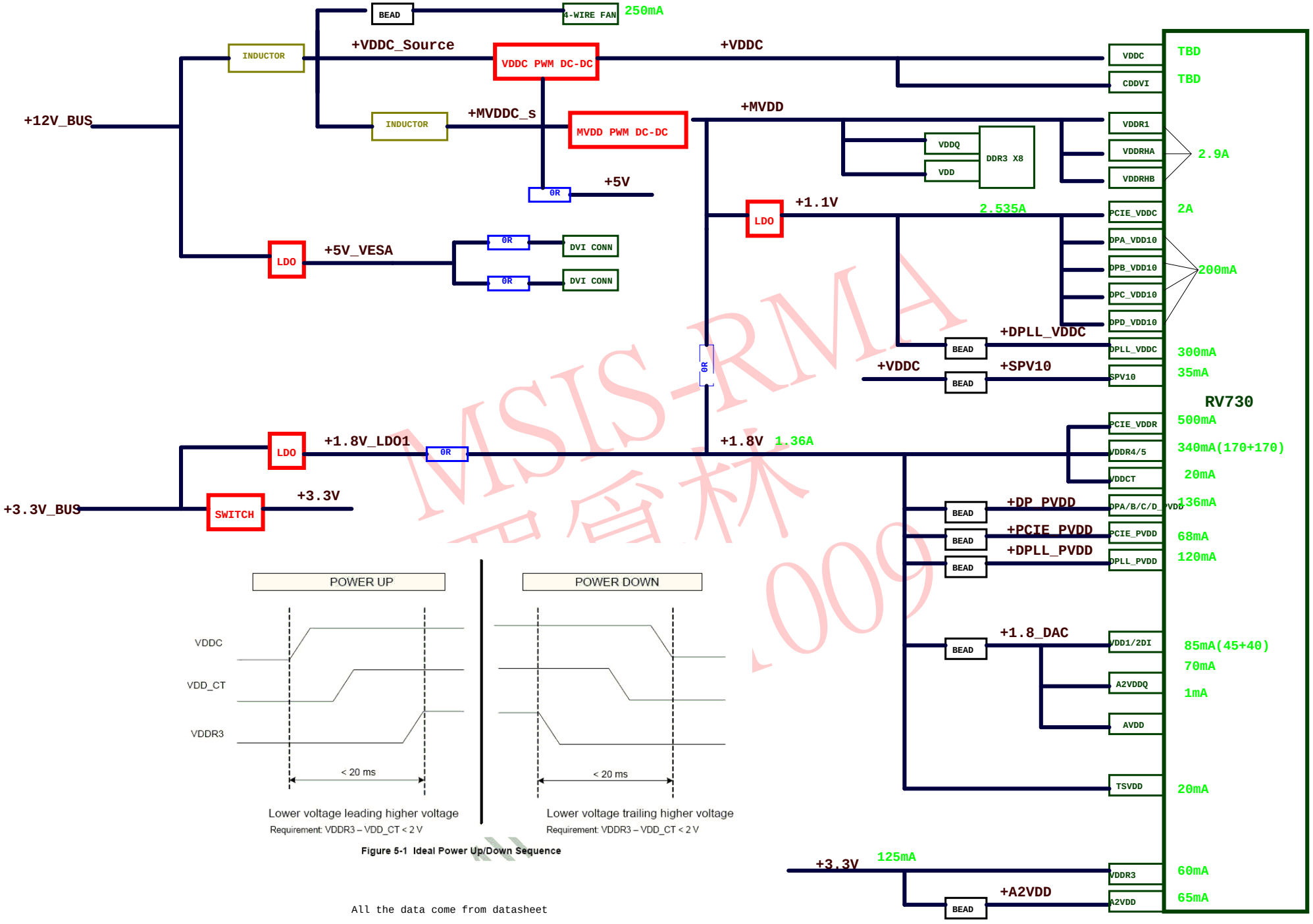

Figure 5-1 Ideal Power Up/Down Sequence

All the data come from datasheet

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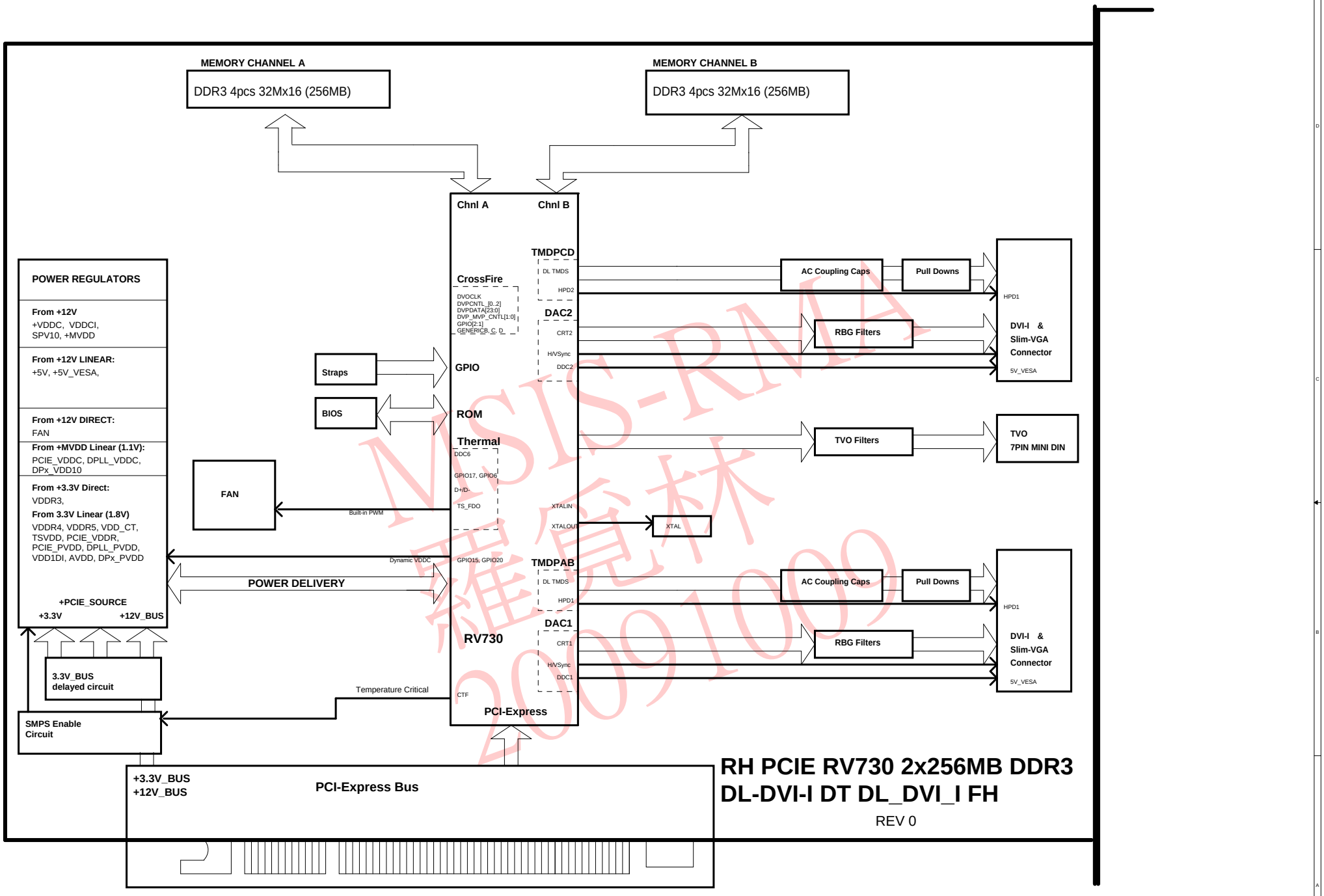

RH PCIE RV730 2x256MB DDR3
DL-DVI-I DT DL_DVI_I FH

REV 0

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Title	Schematic No.	Date:
RH RV730 DDR3 DVI TVO DVI	105-B868xx-00A	Monday, March 09, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	08/04/01	Initial design for RV730 GDDR3
	10	09/01/09	1.Page6 Close GENERICA 2.Page7 Remove TV-OUT, add D-Sub,add protect diode ED62~ED75 3.Page8 Add protect diode REG1001~REG1004 4.Page9 Add HDMI, protect diode REG2001~REG2002,ED76~ED77 5.Page12 co-layout L602,L612, Remove input choke L620,B600,change L621 footprint 6.Page13 change L701 footprint 7.Page14 Change +5V circuit
		12/01/09	1.Page12 Remove +12V_Bus C690 EL cap , Add C624 C626 10uF MLCC
		13/01/09	1.Page16 Add FM1~FM6
		14/01/09	1.Page8 Remove REG1001~REG1004 2.Page9 Remove REG2001~REG2002 3.Page16 Remove MT2
	11	28/02/09	1.Page11 Add EC1 poscap Remove C943,C269,C272,C275,C276,C277,C162,C163,C164,C166,C167,C168,C171,C172,C173,C174,C175 2.Page12 Add R659,C616 connect to +VDDC