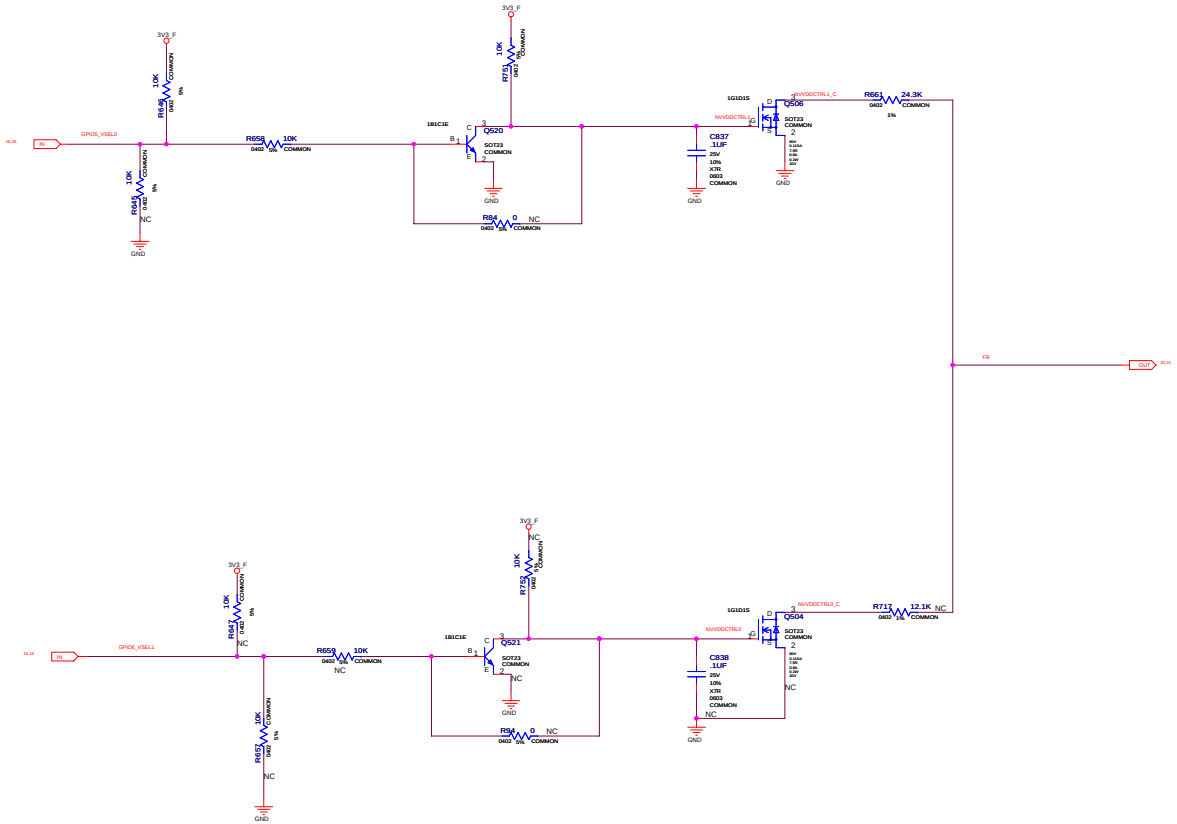
DYNAMIC NVVDD



Dynamic NVVDD

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: NVDD DUAL PHASE SWITCHER

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

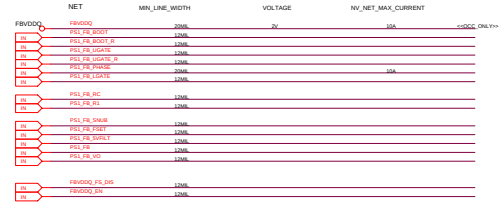
NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

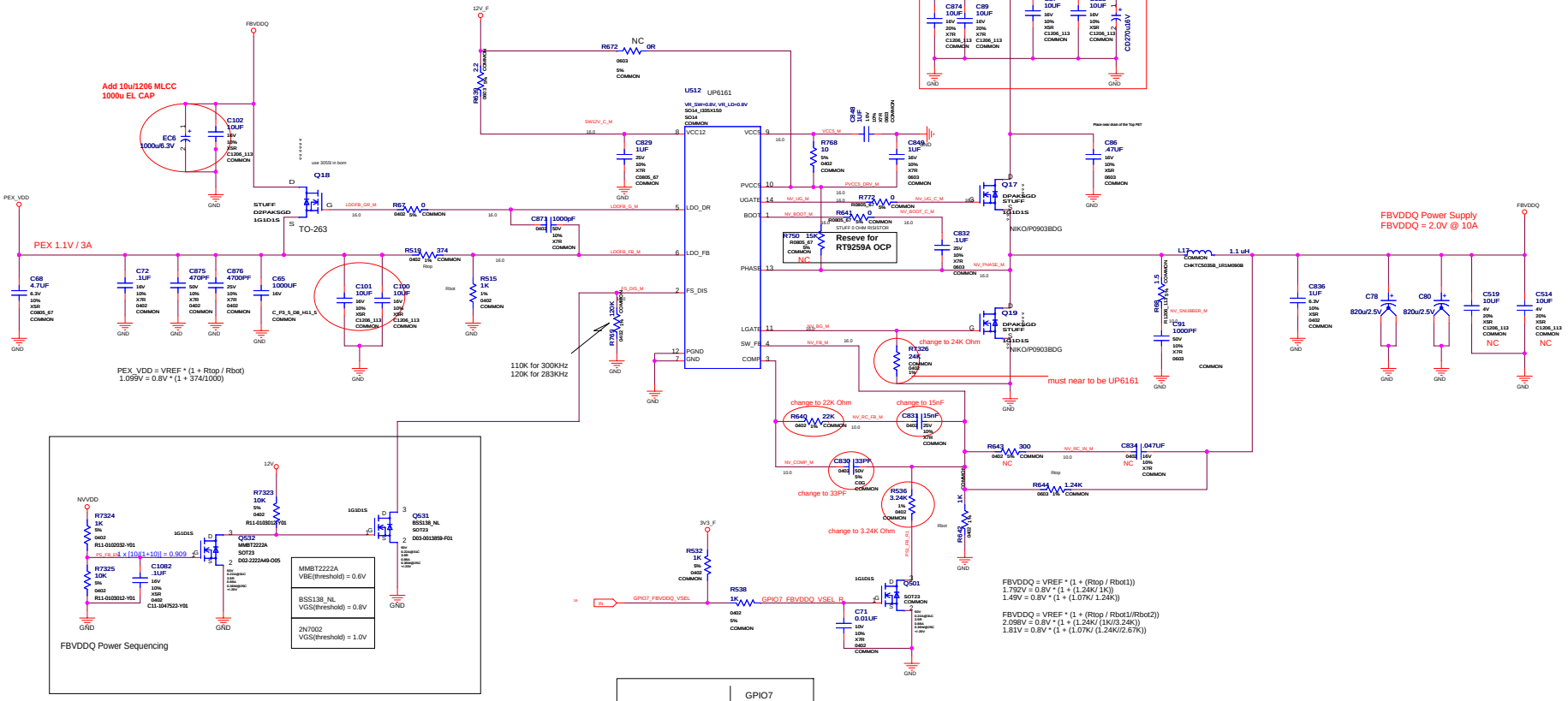
POWER SUPPLY: FBVDD/Q

FBVDDQ: 1.2mil internal plane
500 mil wide from VRM to MEM
3inch from VRM to farthest MEM

FBVDDQ: 1.8-2.0V @ 9A

FBVDDQ/Q decap near VRM:
1x 47uF 1206
2x 1500uF ALE/OSCON





	GPIO7
FBVDDQ = 1.792V / 1.49V	0
FBVDDQ = 2.098V / 1.81V	1

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: FBVDDQ SINGLE PHASE SWITCHER

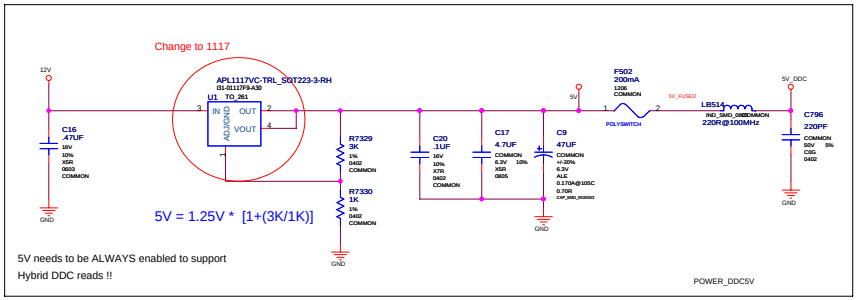
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A
ID	
PAGE	
NAME	
DATE	31-OCT-2007

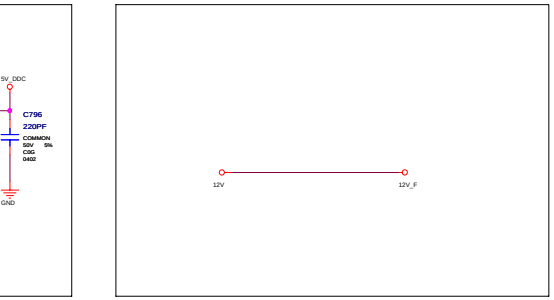
Power Supply: 5V, 5V_DDC, TMDS, MIOA_VDDQ

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	0.1A	12MIL	5V
5V_DDC	0.1A	12MIL	5V
5V	0.15A	12MIL	5V
PS_1V8_ADJ		10MIL	1.8V
1V8	0.12A	12MIL	1.8V
2V5	0.3A	12MIL	2.5V
GND		16MIL	0V
3V3_F	3.5A	16MIL	3.3V
12V_F	6A	20MIL	12V

5V REGULATOR

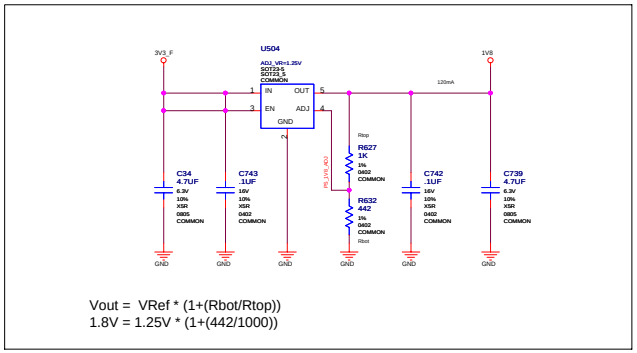


5V DDC

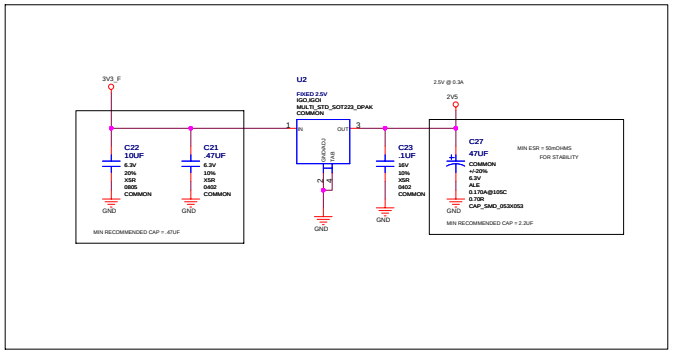


12V filter

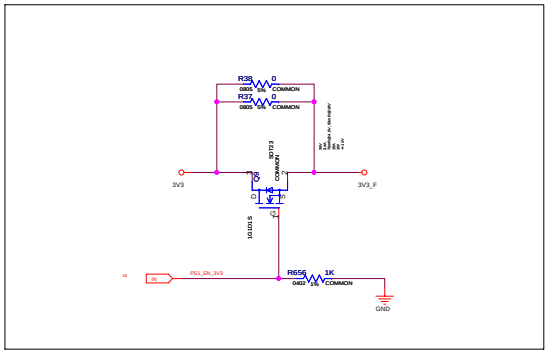
IFP PLL Supply 1.8V



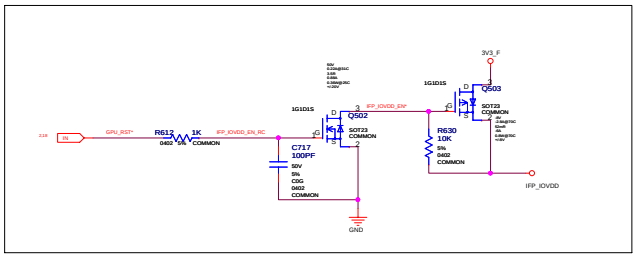
MIO_VDD 2.5V



3V3 switch



IFP_IOVDD BACKDRIVE PREVENTION



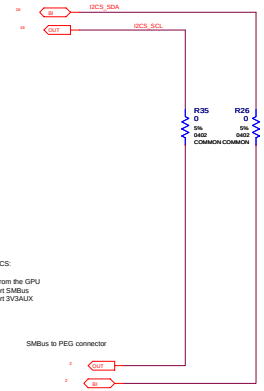
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY LINEARS: 5V, DDC5V, IFP PLLVDD, IFP IOVDD, MIO VDD, 3V3 FILTER, 12V FILTER

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

HYBRID POWER

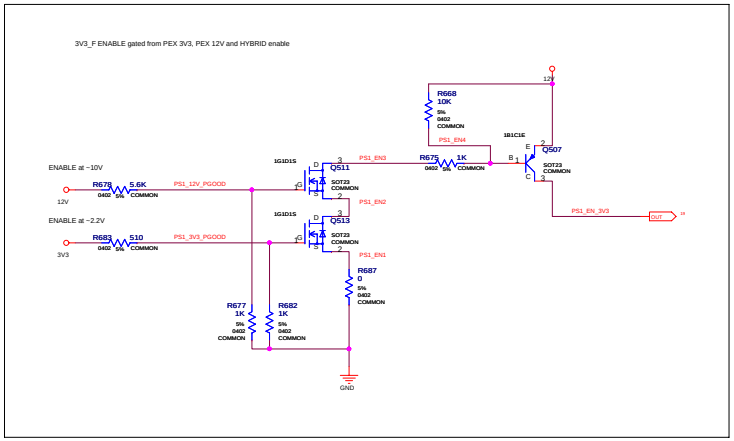
SMBus to GPU



Weak pull-ups needed for I2CS:

* if SMBus is isolated from the GPU
* if MB does not support SMBus
* if MB does not support 3V3AUX

SMBus to PEG connector



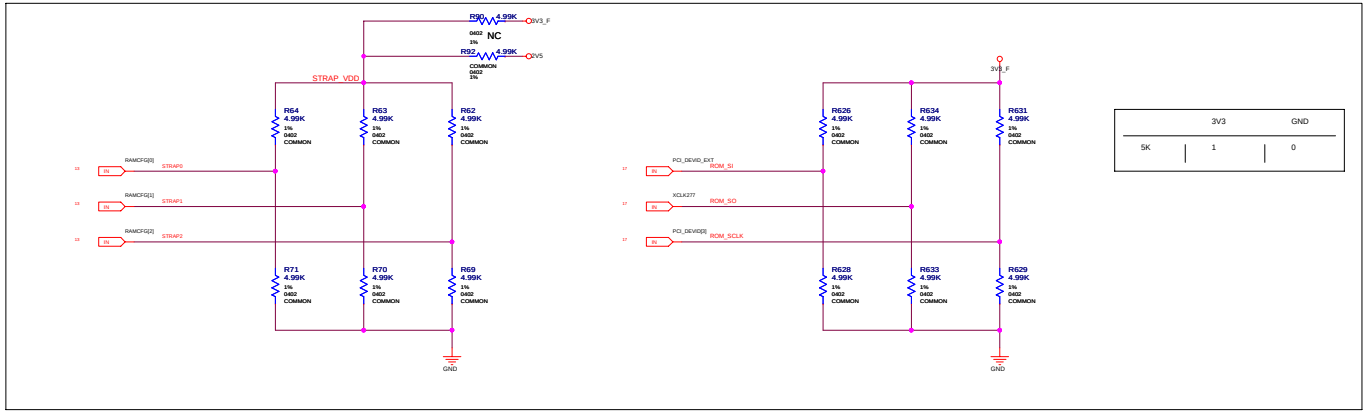
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	HYBRID POWER CIRCUIT

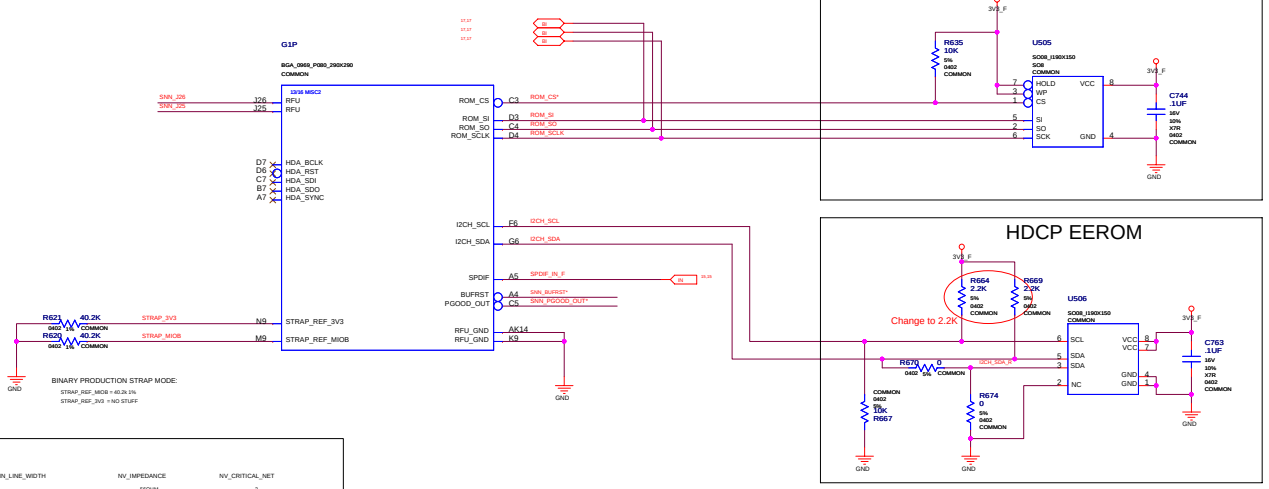
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

STRAPPING OPTIONS

Assembly: BIOS





NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
OUT HDA_BCLK		55OHM	2
OUT HDA_RST*		55OHM	2
OUT HDA_SDI		55OHM	2
OUT HDA_SDO		55OHM	2
OUT HDA_SYNC		55OHM	2

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

GPIO & JTAG

NETNAME	MIN_LINE_WIDTH	VOLTAGE
THERM_DC	10MIL	
THERM_DA	10MIL	
FAN_PWM	8MIL	
FAN_PWM_R	8MIL	
THERM_DA_R	10MIL	
THERM_DC_R	10MIL	

Use 10MIL Guard(GND) Trace
around THERMDC and THERMDA

G10
BGA_0869_P080_29X29
COMMON
12/16 MISC1
B4 THERMDN
B5 THERMDP
AP14 JTAG_TCK
AR14 JTAG_TMS
AN14 JTAG_TDI
AN16 JTAG_TDO
AP16 JTAG_TRST
I2CS_SCL E2
I2CS_SDA E1
I2CC_SCL E3
I2CC_SDA F4
I2CD_SCL F5
I2CD_SDA D5
I2CE_SCL D5
I2CE_SDA E5
GPIO0 K1
GPIO1 K2
GPIO2 K3
GPIO3 H3
GPIO4 H2
GPIO5 H1
GPIO6 H4
GPIO7 H5
GPIO8 M6
GPIO9 J7
GPIO10 K4
GPIO11 K5
GPIO12 H7
GPIO13 J4
GPIO14 J6
GPIO15 L1
GPIO16 L2
GPIO17 L4
GPIO18 M4
GPIO19 L7
GPIO20 L5
GPIO21 K6
SWAP_RDY_A/GPIO22 L6
STEREO/GPIO23 M6

R650 2.2K 5% 0402 COMMON
R653 2.2K 5% 0402 COMMON
R651 47K 5% 0402 COMMON
R652 47K 5% 0402 COMMON
R43 33 5% 0402 COMMON
R42 33 5% 0402 COMMON
R44 33 5% 0402 COMMON
R41 33 5% 0402 COMMON
R666 0 0402 5% COMMON
R671 0 0402 5% COMMON
R40 1K 5% 0402 COMMON
Q10 SOT23 COMMON
1G1D1S

GPIO PWM FAN Control 4-PIN
DS10 30V 200MA SOT23 COMMON
R673 10K 5% 0402 COMMON
R665 10K 5% 0402 COMMON
C26 .1UF 16V 10% X7R 0603 COMMON
J7 MALE 2MM 0 CON_WAFER232_004_TH_ST_PG26 COMMON

R654 10K 5% 0402 COMMON
R649 10K 5% 0402 COMMON
R662 10K 5% 0402 COMMON
C764 1UF 6.3V 10% X5R 0402 COMMON
R663 10K 5% 0402 COMMON
R648 10K 5% 0402 COMMON
J501 TSW-XLE 1.27MM 0 CON_HDR_050X004 COMMON

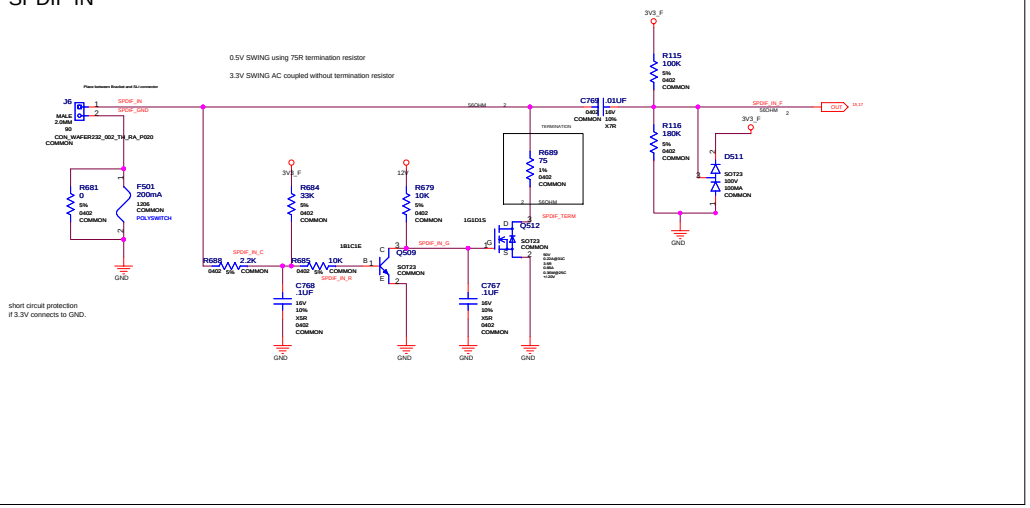
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	EXTERNAL THERMAL SENSOR, 4PIN FAN CONTROL, GPIO

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

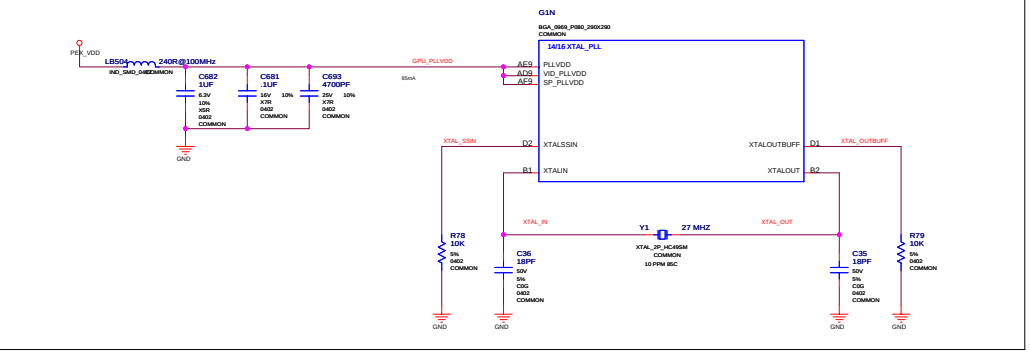
NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

XTAL/PLLVDD/SPDIF IN

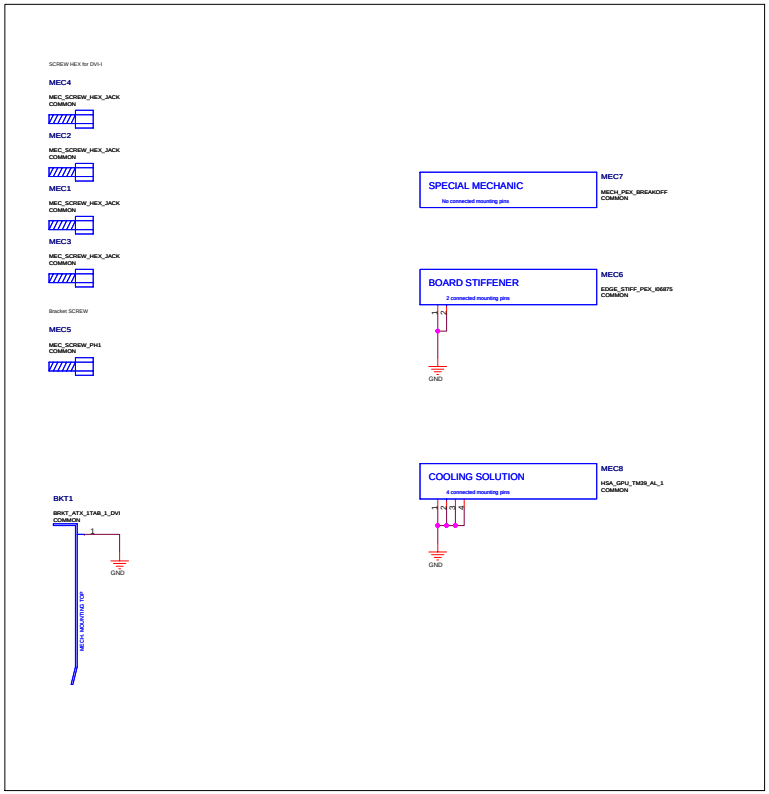
SPDIF IN



XTAL/GPU_PLLVDD



MECHANICALS & THERMALS



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF-IN, XTAL, MECHANICALS, THERMALS

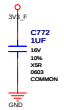
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

DACB: SD/HD VIDEO OUT CONNECTOR

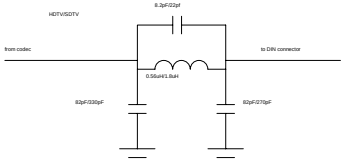
NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
OUT DACB_C_OUT		75OHM	1
OUT DACB_CVBS_OUT		75OHM	1
OUT DACB_PB_OUT		75OHM	1
BI TV_PROUT_C		75OHM	1
BI TV_COUT_C		75OHM	1
BI TV_YOUT_C		75OHM	1
IN DACB_VREF	12MIL		
IN DACB_RSET	12MIL		

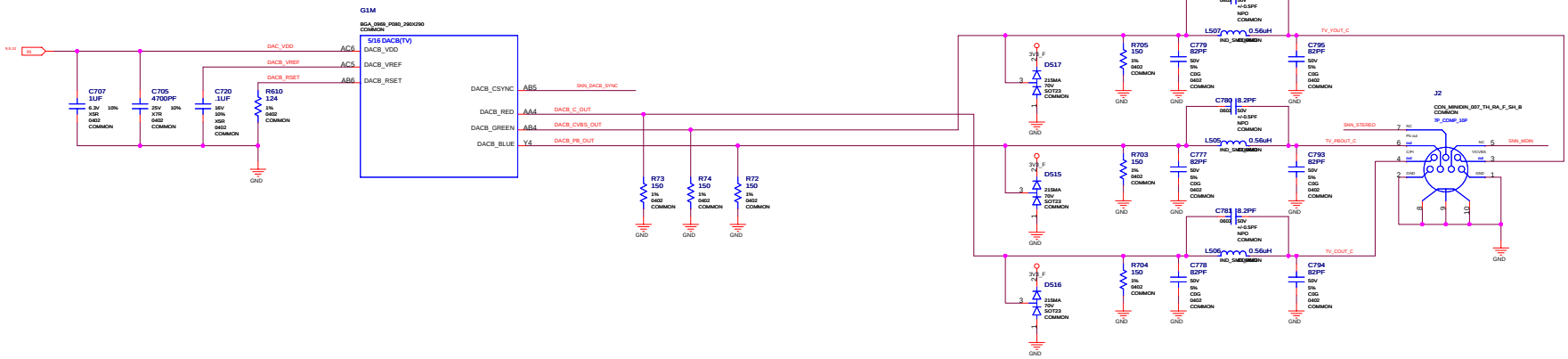
FOR ESD DIODES



Place near ESD diodes.

FILTER CIRCUIT



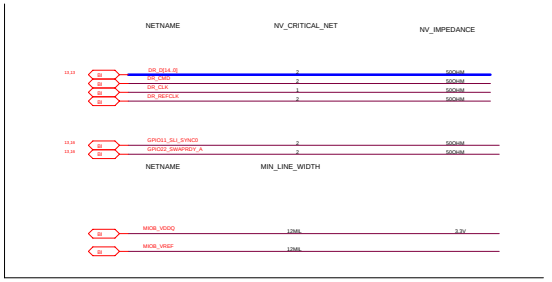


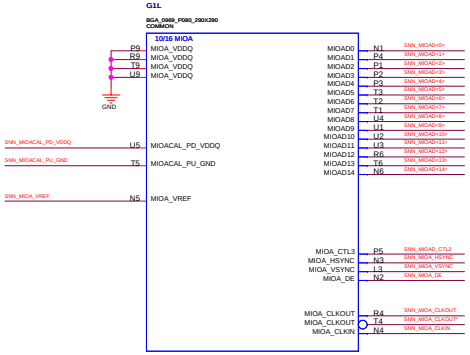
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, MINIDIN CONNECTOR NORTH, SD/HD VIDEO OUTPUT CONNECTOR

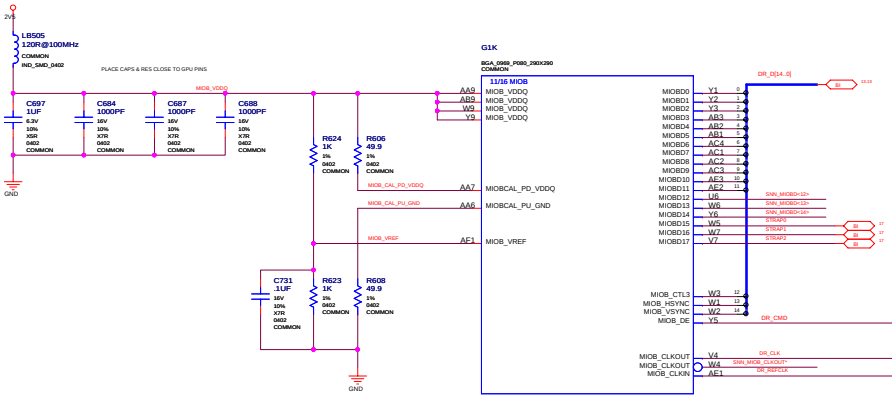
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

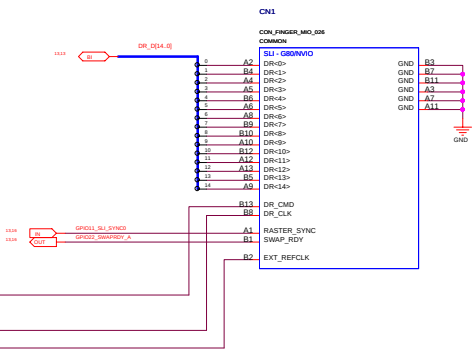
MIOA/B SLI







SLI Connector

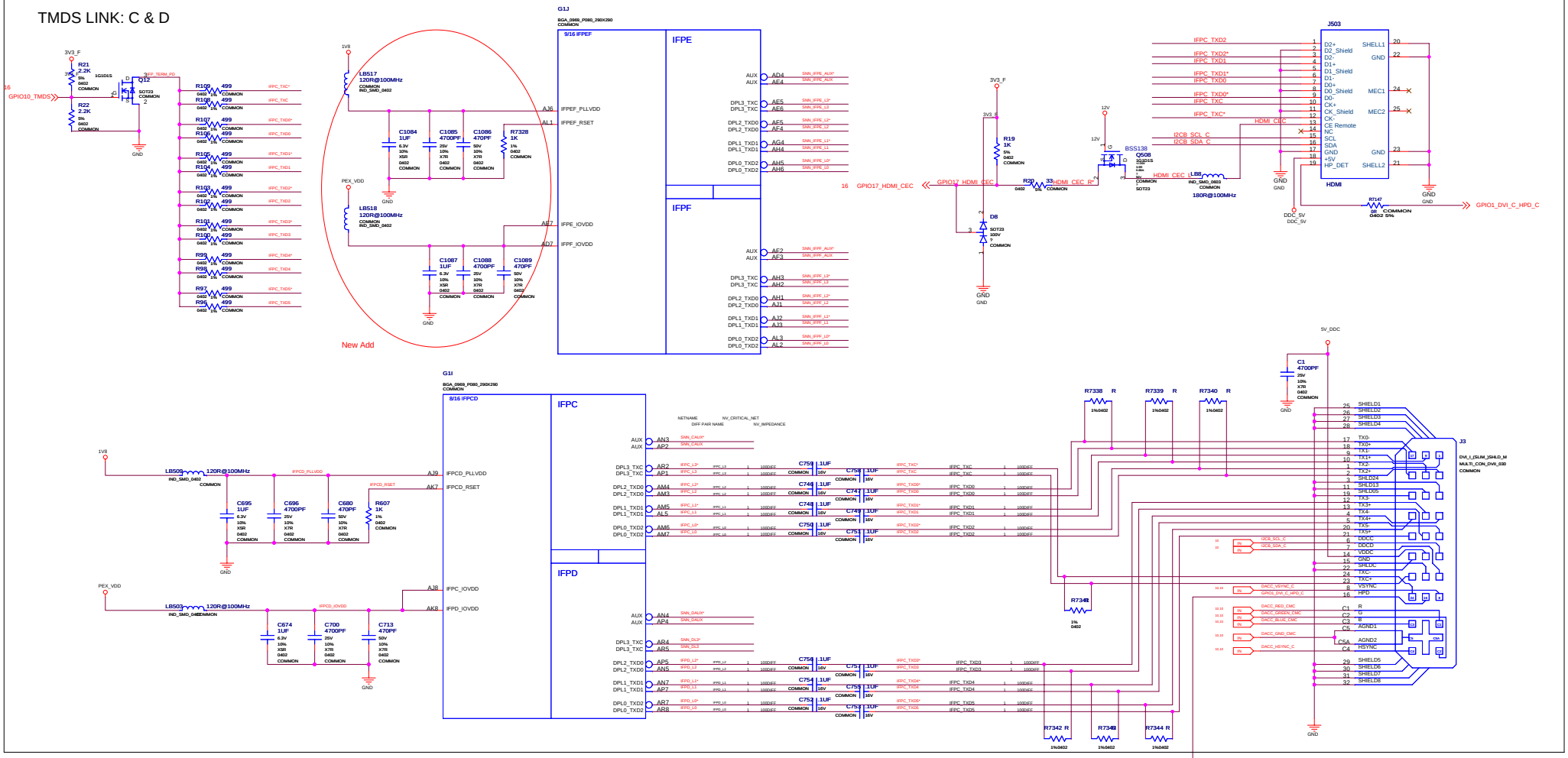


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB, SLI CONNECTOR

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

TMDS LINK: C & D



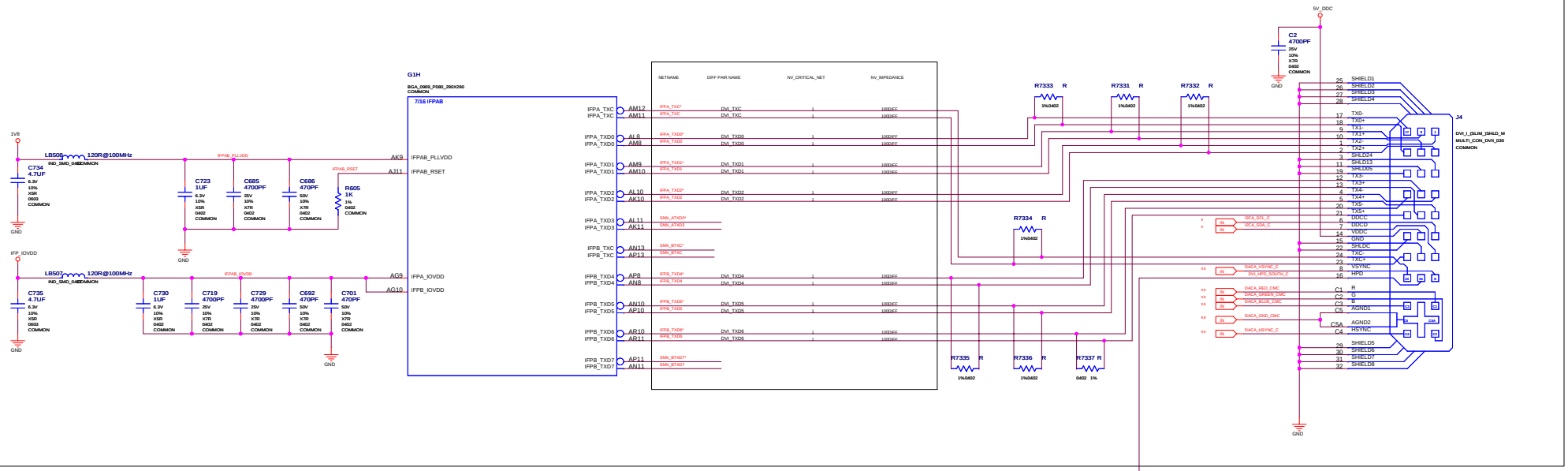
Hotplug Detection

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK C/D, AC COUPLING, PDS, DVI CONNECTOR MID

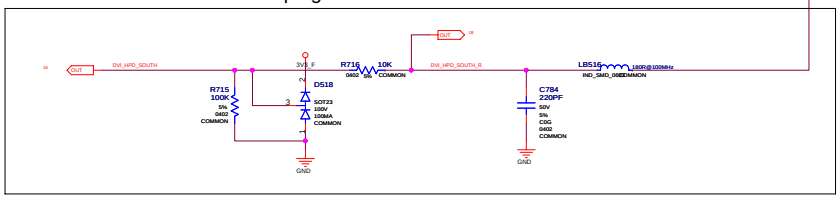
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

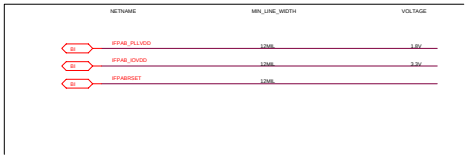
NV_PN	600-10727-base-sch A
ID	
NAME	
PAGE	
DATE	31-OCT-2007

TMDS LINK: A & B



Hotplug Detection





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK A/B, DVI CONNECTOR SOUTH

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

Secondary Display (DACC), Slim DB15

DACC RGB-FILTER

NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACC_VREF			12MIL
DACC_RSET			12MIL
DACC_RED	1	75OHM	
DACC_GREEN	1	75OHM	
DACC_BLUE	1	75OHM	
DACC_RED_C	1	75OHM	
DACC_GREEN_C	1	75OHM	
DACC_BLUE_C	1	75OHM	
DACC_GND_CMC	0V		12MIL
DACC_RED_CMC	1	75OHM	
DACC_GREEN_CMC	1	75OHM	
DACC_BLUE_CMC	1	75OHM	
DACC_HSYNC	1	50OHM	
DACC_VSYNC	1	50OHM	
DACC_VSYNC_R	1	50OHM	
DACC_HSYNC_R	1	50OHM	
DACC_VSYNC_BUF	1	50OHM	
DACC_HSYNC_BUF	1	50OHM	
DACC_VSYNC_C	1	50OHM	
DACC_HSYNC_C	1	50OHM	

FOR ESD DIODES

C771 1UF 16V 10% X5R 0603 COMMON

C19 1UF 16V 10% X5R 0603 COMMON

Place near ESD diodes.

EMI filter, place close to DVI

EMI filter, place close to DVI

Place 0ohm Resistor Incident with Common Mode Choke

MIDDLE

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A
ID	
NAME	
PAGE	
DATE	31-OCT-2007

Primary Display (DACA), DVI-I

DACA RGB-FILTER

NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DAC_VDD		3.3V	12MIL
DACA_VREF			12MIL
DACA_RSET			12MIL
DACA_RED	1	75OHM	
DACA_GREEN	1	75OHM	
DACA_BLUE	1	75OHM	
DACA_RED_C	1	75OHM	
DACA_GREEN_C	1	75OHM	
DACA_BLUE_C	1	75OHM	
DACA_GND_CMC		0V	12MIL
DACA_RED_CMC	1	75OHM	
DACA_GREEN_CMC	1	75OHM	
DACA_BLUE_CMC	1	75OHM	
DACA_HSYNC	1	50OHM	
DACA_VSYNC	1	50OHM	
DACA_HSYNC_R	1	50OHM	
DACA_VSYNC_R	1	50OHM	
DACA_VSYNC_BUF	1	50OHM	
DACA_HSYNC_BUF	1	50OHM	
DACA_VSYNC_C	1	50OHM	
DACA_HSYNC_C	1	50OHM	

EMI filter, place close to DVI

EMI filter, place close to DVI

PLACE NEAR SYNC BUFFER

Route DAC RGB with ~37.5ohm impedence

Place 0ohm Resistor Incident with Common Mode Choke

FOR ESD DIODES

Place near ESD diodes.

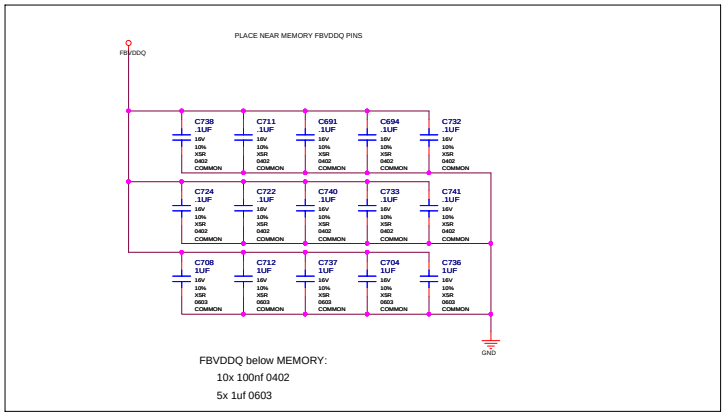
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

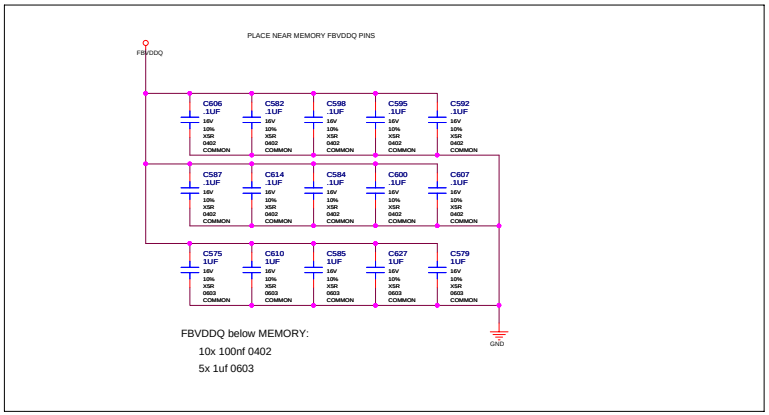
NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

FRAMEBUFFER: PARTITION C DECOUPLING

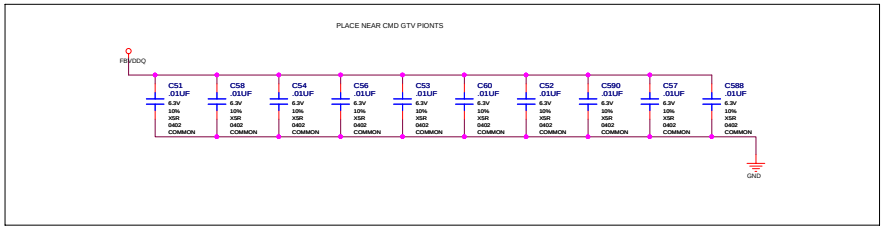
Decoupling for FBC 0..31

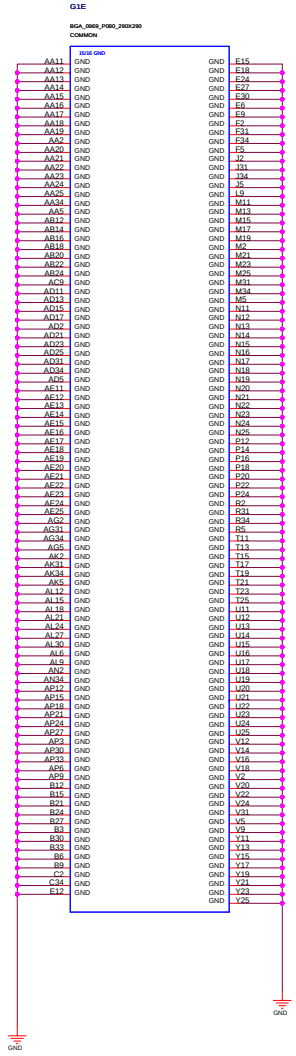


Decoupling for FBC 32..63



Return path coupling GND/FBVDDQ for FBC



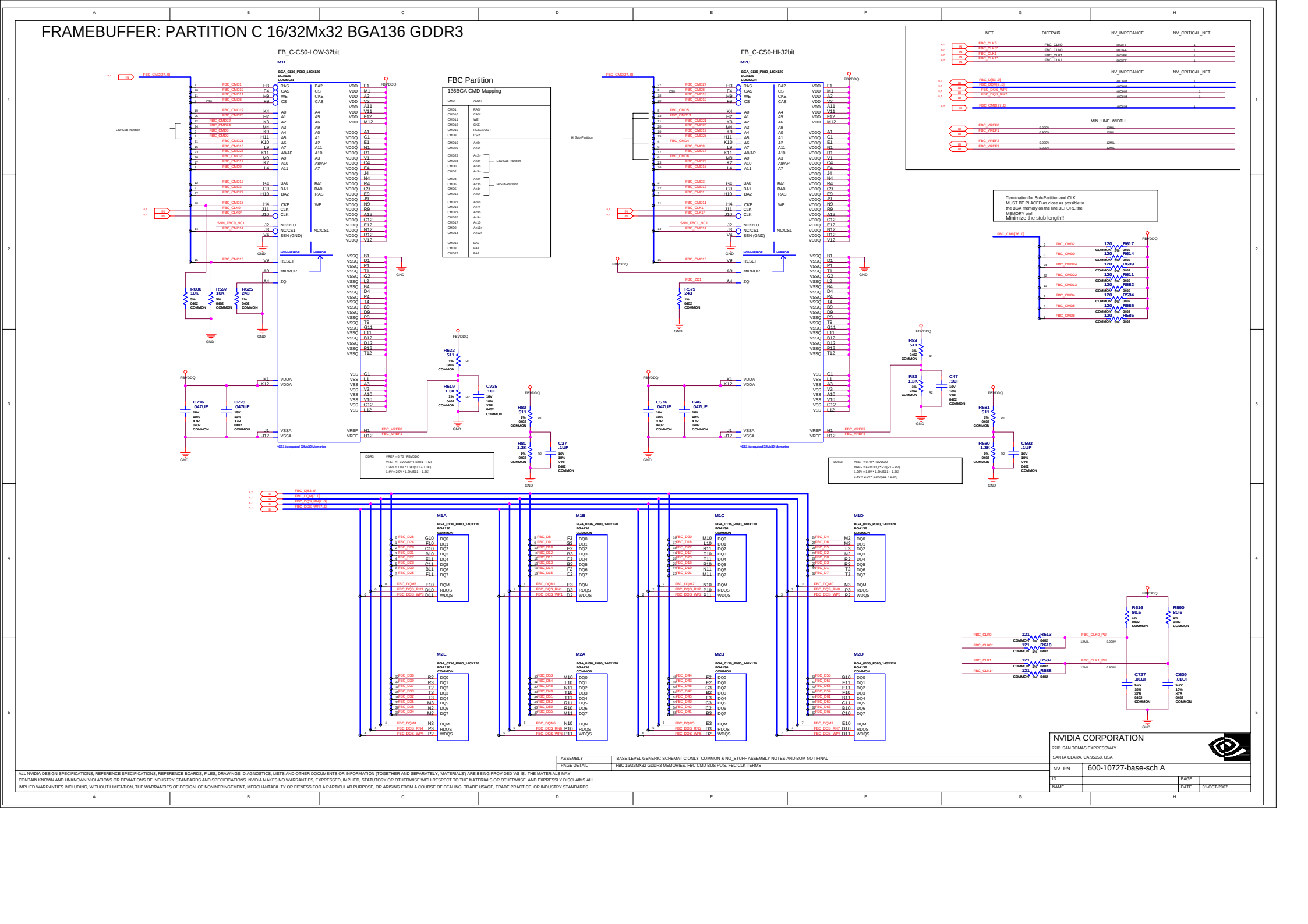


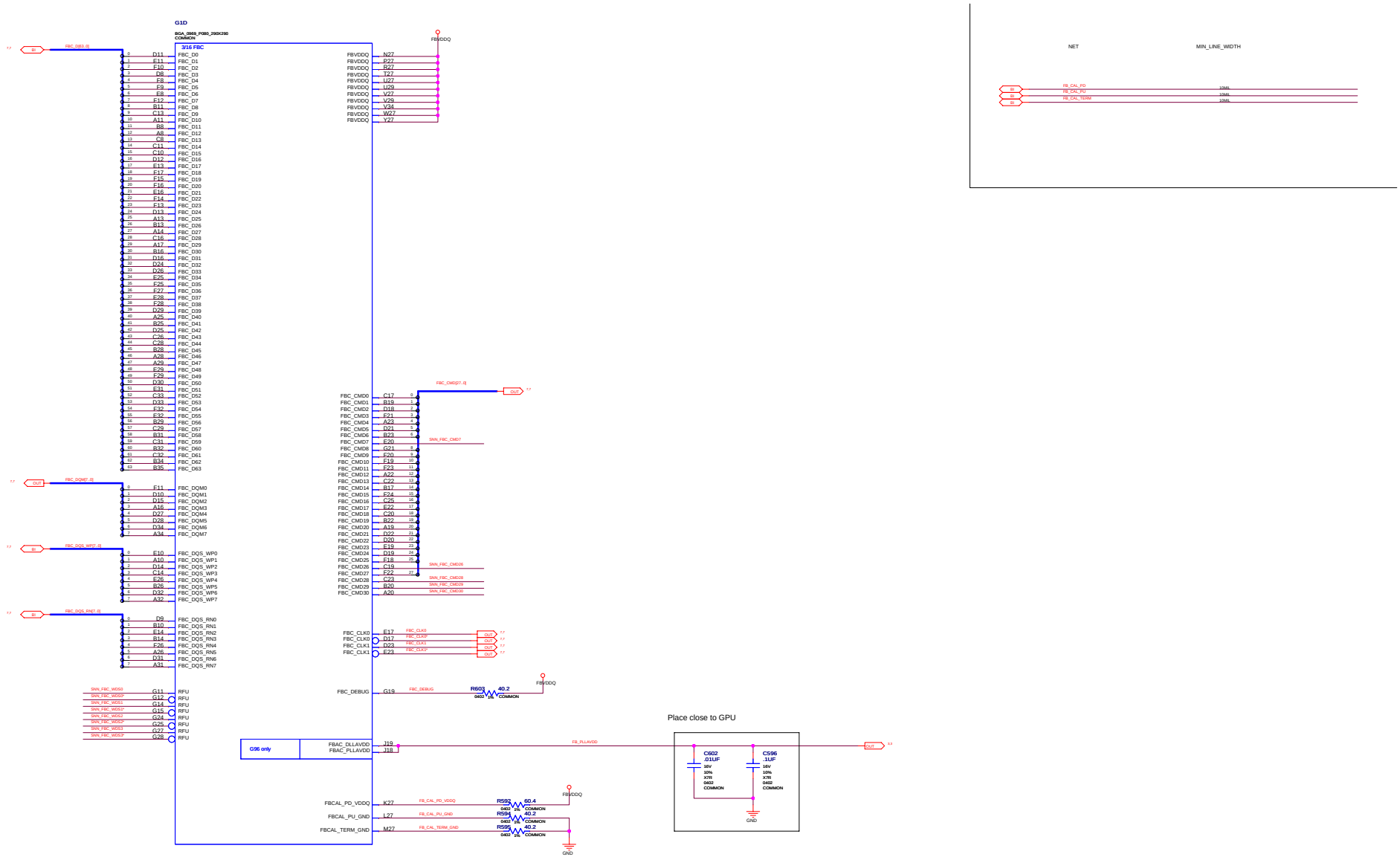
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS, GPU GND CONNECTIONS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3





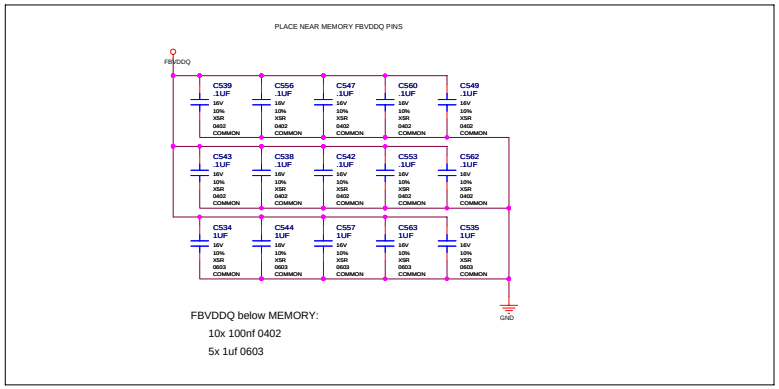
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY INTERFACE

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

FRAME BUFFER: PARTITION A DECOUPLING

Decoupling for FBA 0..31

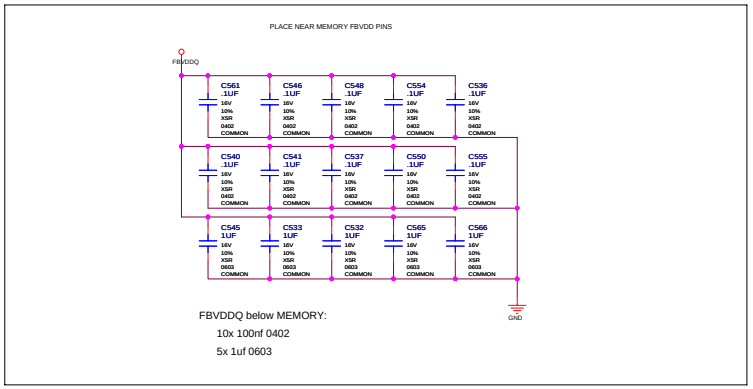


FBVDDQ below MEMORY:

10x 100nf 0402

5x 1uf 0603

Decoupling for FBA 32..63

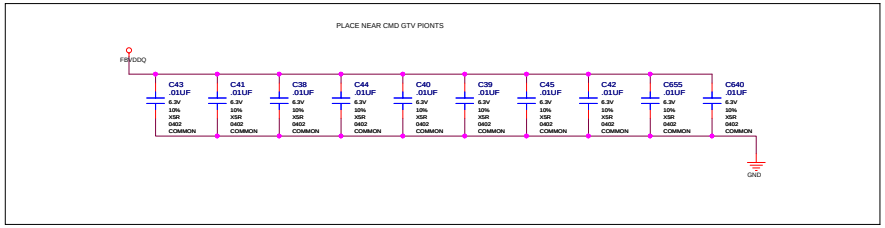


FBVDDQ below MEMORY:

10x 100nf 0402

5x 1uf 0603

Return path coupling GND/FBVDDQ for FBA

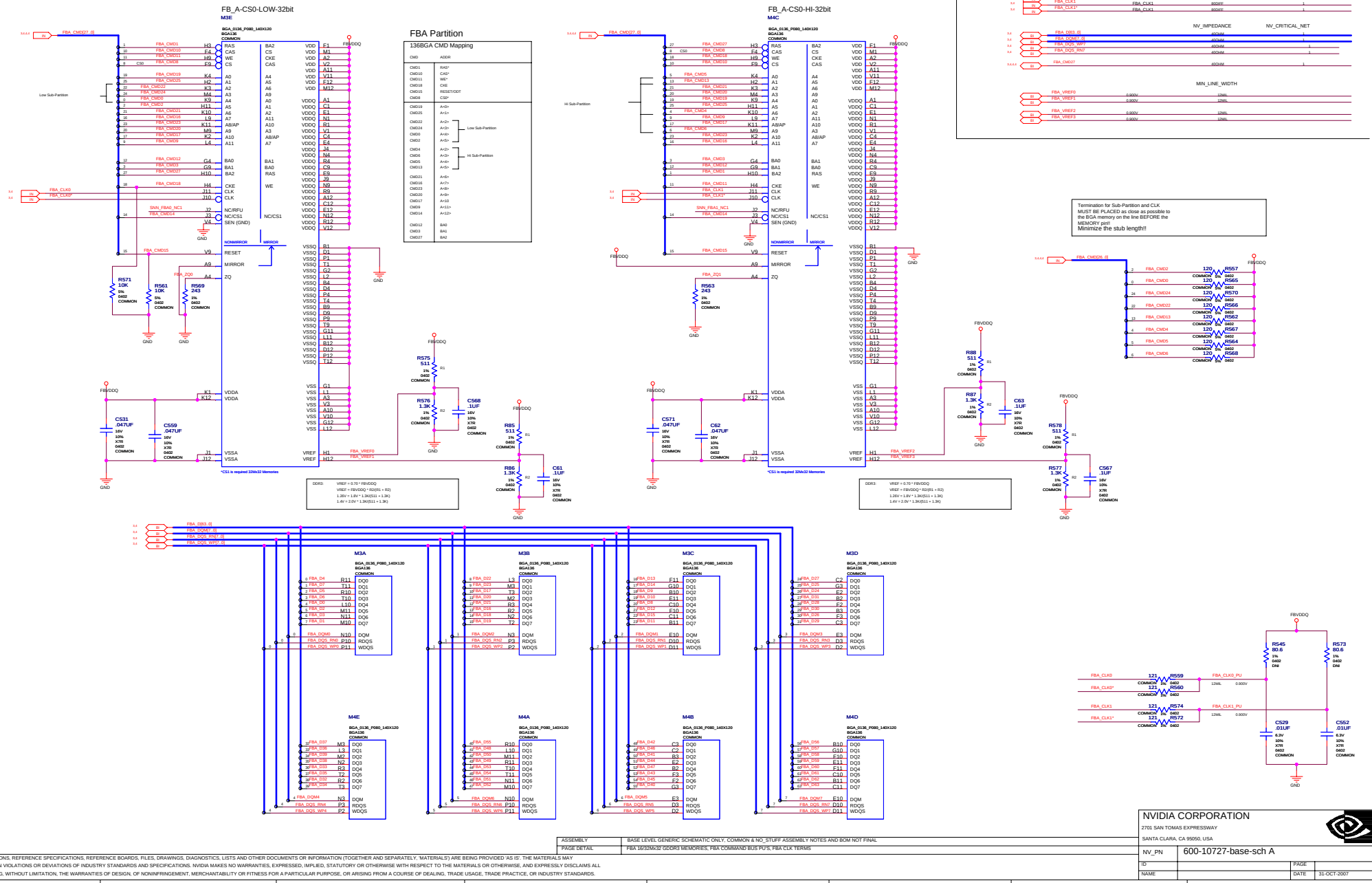


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3



NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
FBA_CLK0	FBA_CLK0	80DIFF	1
FBA_CLK0*	FBA_CLK0	80DIFF	1
FBA_CLK1	FBA_CLK1	80DIFF	1
FBA_CLK1*	FBA_CLK1	80DIFF	1

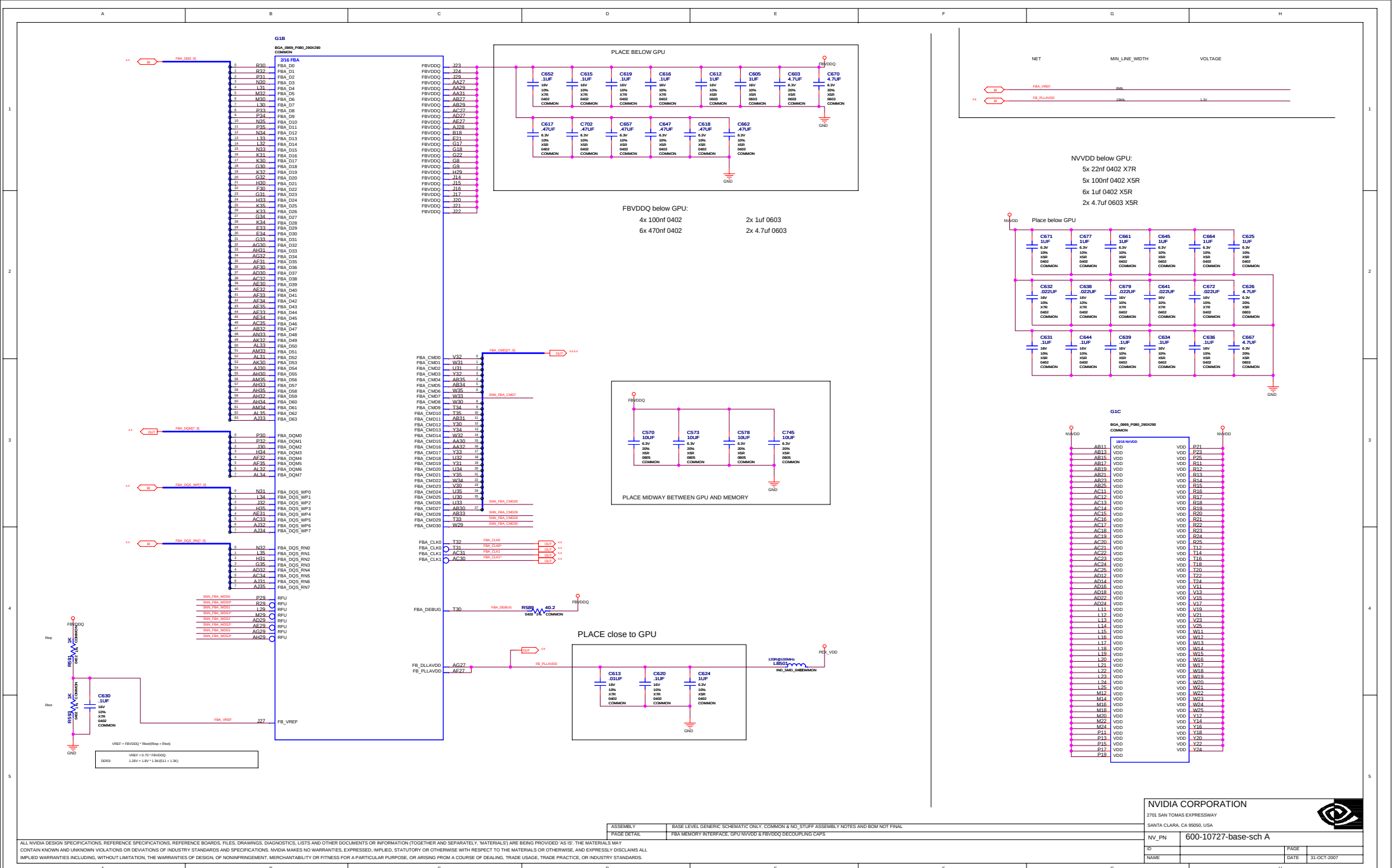
NET	NV_IMPEDANCE	NV_CRITICAL_NET
FBA_DBI_0	40OHM	1
FBA_DQM7_0	40OHM	1
FBA_DQS_WP7	40OHM	1
FBA_DQS_RN7	40OHM	1
FBA_CMD27	40OHM	1

NET	MIN_LINE_WIDTH
FBA_VREF0	12MIL
FBA_VREF1	12MIL
FBA_VREF2	12MIL
FBA_VREF3	12MIL

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16/32Mx32 GDDR3 MEMORIES, FBA COMMAND BUS PU'S, FBA CLK TERMS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

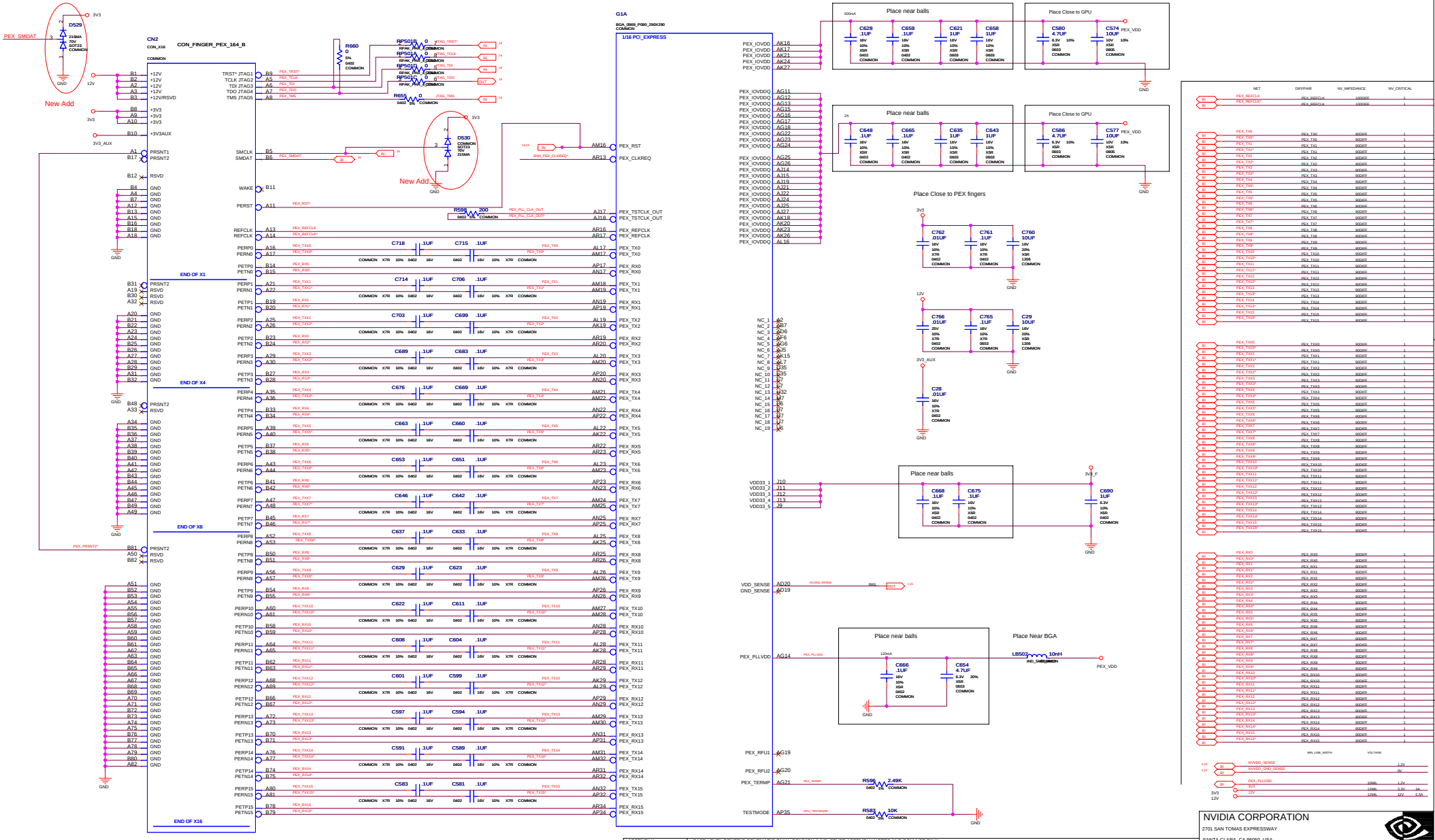


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY INTERFACE; GPU NVVDD & FBVDDQ DECOUPLING CAPS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

16X PEX INTERFACE



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS` INTERFACE, PEX_VDD DECOUPLING CAPS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

P727-A01: G96, GB1-128, GDDR3, DL-DVI, DL-DVI/VGA, SD/HDTV

PAGE SUMMARY:

Modify history from P727-A01

1.Page21/22: NVVDD PWM change to RT8805

2.Page20: FBVDDQ/PEX_VDD change to RT9259A

3.Page18: Remove U3

Page2␣PEX_RST*/GPU_RST*
PEX_PRSNT1*/PEX_PRSNT2*

Page9/10␣DACA/C I2C (remove U508 and add ESD)

4.Page15 Net SPDIF_IN_F add pull high and low R

5.Page17 Remove J5

6.Page12 Add J503

VAR	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10727-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10727-0000-100	G96-400, 625/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
2	SKU0001	600-10727-0001-100	G96-300, 550/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
3	SKU0002	600-10727-0002-100	G96-300, 550/800Mhz 256MB 16Mx32 GDDR3, DVI DVI
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

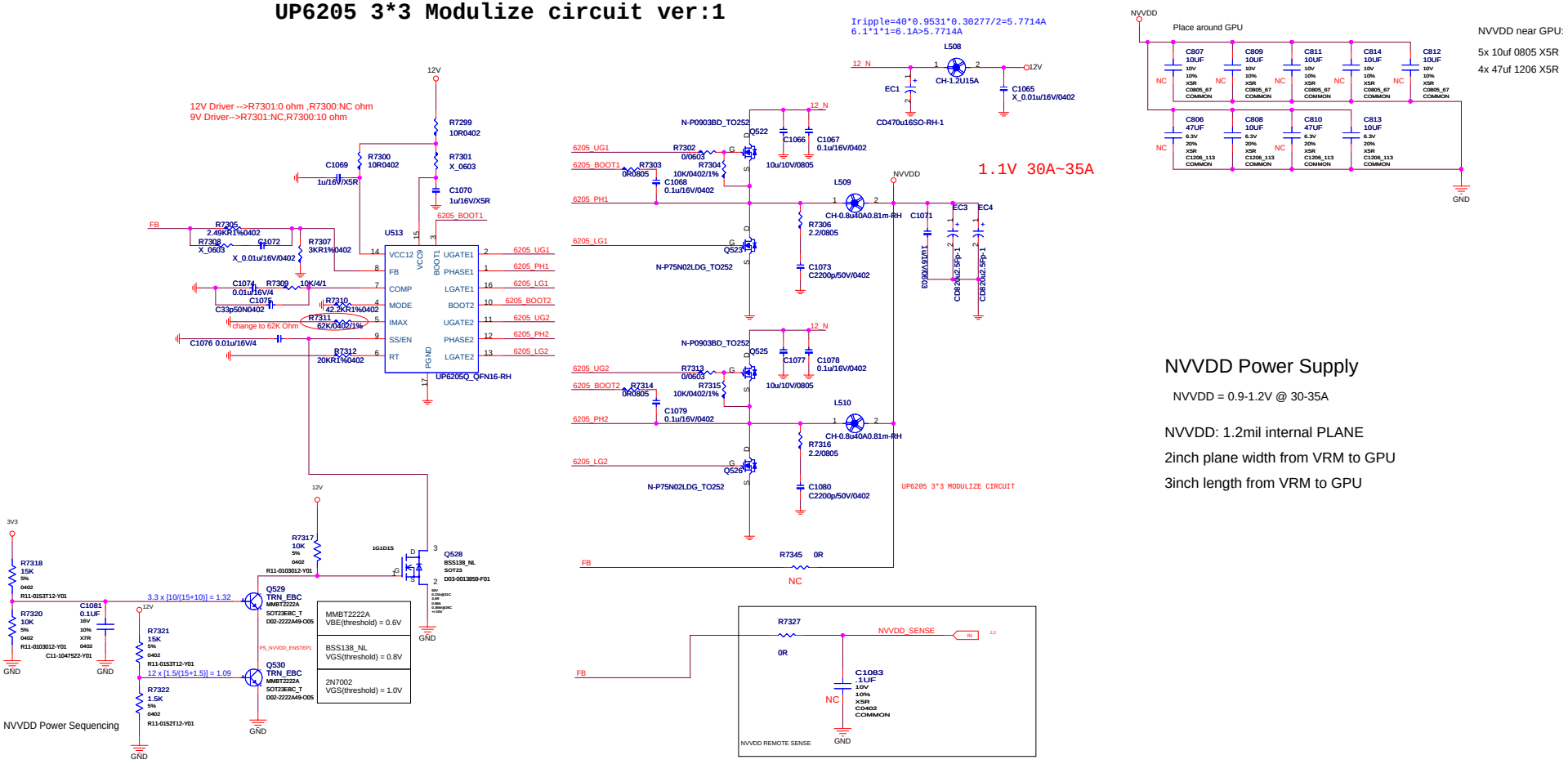
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TABLE OF CONTENTS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

Net Name	LINE_WIDTH	Current	Voltage
NVVDD	36MIL	15A	1.2V
PEX1V2	24MIL	1.5A	1.20000
NVVDD_SENSE	16MIL	0.5A	1.2V
NVVDD_SENSE_M	16MIL	0.5A	1.2V

UP6205 3*3 Modulize circuit ver:1



NVVDD Power Supply

NVVDD = 0.9-1.2V @ 30-35A

NVVDD: 1.2mil internal PLANE

2inch plane width from VRM to GPU

3inch length from VRM to GPU

Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Friday, March 21, 2008	Sheet 21 of 22		