P395-A01 Base Design

P395-A01, G92, 16Mx32/32Mx32 GDDR3
DVI-I-DL, DVI-I-DL, HDTVout

Table of Contents:

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10395-base-100	P395 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0050	600-10395-0050-100	P395 G92 512MB GDDR3 16Mx32 DVI-I+DVI-I
2	SKU0051	600-10395-0051-100	p395 G92 512MB GDDR3 32MX32 DVI-I+DVI-I
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	P395 G92 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	Overview

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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Page2: PCI Express 1.0

PEX NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
PEX_REFCLK	1	90DIFF	PEX_REFCLK
PEX_REFCLK*	1	90DIFF	PEX_REFCLK
PEX_TX0_C	1	90DIFF	PEX_TX0_C
PEX_TX0_C*	1	90DIFF	PEX_TX0_C
PEX_TX1_C	1	90DIFF	PEX_TX1_C
PEX_TX1_C*	1	90DIFF	PEX_TX1_C
PEX_TX2_C	1	90DIFF	PEX_TX2_C
PEX_TX2_C*	1	90DIFF	PEX_TX2_C
PEX_TX3_C	1	90DIFF	PEX_TX3_C
PEX_TX3_C*	1	90DIFF	PEX_TX3_C
PEX_TX4_C	1	90DIFF	PEX_TX4_C
PEX_TX4_C*	1	90DIFF	PEX_TX4_C
PEX_TX5_C	1	90DIFF	PEX_TX5_C
PEX_TX5_C*	1	90DIFF	PEX_TX5_C
PEX_TX6_C	1	90DIFF	PEX_TX6_C
PEX_TX6_C*	1	90DIFF	PEX_TX6_C
PEX_TX7_C	1	90DIFF	PEX_TX7_C
PEX_TX7_C*	1	90DIFF	PEX_TX7_C
PEX_TX8_C	1	90DIFF	PEX_TX8_C
PEX_TX8_C*	1	90DIFF	PEX_TX8_C
PEX_TX9_C	1	90DIFF	PEX_TX9_C
PEX_TX9_C*	1	90DIFF	PEX_TX9_C
PEX_TX10_C	1	90DIFF	PEX_TX10_C
PEX_TX10_C*	1	90DIFF	PEX_TX10_C
PEX_TX11_C	1	90DIFF	PEX_TX11_C
PEX_TX11_C*	1	90DIFF	PEX_TX11_C
PEX_TX12_C	1	90DIFF	PEX_TX12_C
PEX_TX12_C*	1	90DIFF	PEX_TX12_C
PEX_TX13_C	1	90DIFF	PEX_TX13_C
PEX_TX13_C*	1	90DIFF	PEX_TX13_C
PEX_TX14_C	1	90DIFF	PEX_TX14_C
PEX_TX14_C*	1	90DIFF	PEX_TX14_C
PEX_TX15_C	1	90DIFF	PEX_TX15_C
PEX_TX15_C*	1	90DIFF	PEX_TX15_C
PEX_RX0	1	90DIFF	PEX_RX0
PEX_RX0*	1	90DIFF	PEX_RX0
PEX_RX1	1	90DIFF	PEX_RX1
PEX_RX1*	1	90DIFF	PEX_RX1
PEX_RX2	1	90DIFF	PEX_RX2
PEX_RX2*	1	90DIFF	PEX_RX2
PEX_RX3	1	90DIFF	PEX_RX3
PEX_RX3*	1	90DIFF	PEX_RX3
PEX_RX4	1	90DIFF	PEX_RX4
PEX_RX4*	1	90DIFF	PEX_RX4
PEX_RX5	1	90DIFF	PEX_RX5
PEX_RX5*	1	90DIFF	PEX_RX5
PEX_RX6	1	90DIFF	PEX_RX6
PEX_RX6*	1	90DIFF	PEX_RX6
PEX_RX7	1	90DIFF	PEX_RX7
PEX_RX7*	1	90DIFF	PEX_RX7
PEX_RX8	1	90DIFF	PEX_RX8
PEX_RX8*	1	90DIFF	PEX_RX8
PEX_RX9	1	90DIFF	PEX_RX9
PEX_RX9*	1	90DIFF	PEX_RX9
PEX_RX10	1	90DIFF	PEX_RX10
PEX_RX10*	1	90DIFF	PEX_RX10
PEX_RX11	1	90DIFF	PEX_RX11
PEX_RX11*	1	90DIFF	PEX_RX11
PEX_RX12	1	90DIFF	PEX_RX12
PEX_RX12*	1	90DIFF	PEX_RX12
PEX_RX13	1	90DIFF	PEX_RX13
PEX_RX13*	1	90DIFF	PEX_RX13
PEX_RX14	1	90DIFF	PEX_RX14
PEX_RX14*	1	90DIFF	PEX_RX14
PEX_RX15	1	90DIFF	PEX_RX15
PEX_RX15*	1	90DIFF	PEX_RX15
PEX_TX0	1	90DIFF	PEX_TX0
PEX_TX0*	1	90DIFF	PEX_TX0
PEX_TX1	1	90DIFF	PEX_TX1
PEX_TX1*	1	90DIFF	PEX_TX1
PEX_TX2	1	90DIFF	PEX_TX2
PEX_TX2*	1	90DIFF	PEX_TX2
PEX_TX3	1	90DIFF	PEX_TX3
PEX_TX3*	1	90DIFF	PEX_TX3
PEX_TX4	1	90DIFF	PEX_TX4
PEX_TX4*	1	90DIFF	PEX_TX4
PEX_TX5	1	90DIFF	PEX_TX5
PEX_TX5*	1	90DIFF	PEX_TX5
PEX_TX6	1	90DIFF	PEX_TX6
PEX_TX6*	1	90DIFF	PEX_TX6
PEX_TX7	1	90DIFF	PEX_TX7
PEX_TX7*	1	90DIFF	PEX_TX7
PEX_TX8	1	90DIFF	PEX_TX8
PEX_TX8*	1	90DIFF	PEX_TX8
PEX_TX9	1	90DIFF	PEX_TX9
PEX_TX9*	1	90DIFF	PEX_TX9
PEX_TX10	1	90DIFF	PEX_TX10
PEX_TX10*	1	90DIFF	PEX_TX10
PEX_TX11	1	90DIFF	PEX_TX11
PEX_TX11*	1	90DIFF	PEX_TX11
PEX_TX12	1	90DIFF	PEX_TX12
PEX_TX12*	1	90DIFF	PEX_TX12
PEX_TX13	1	90DIFF	PEX_TX13
PEX_TX13*	1	90DIFF	PEX_TX13
PEX_TX14	1	90DIFF	PEX_TX14
PEX_TX14*	1	90DIFF	PEX_TX14
PEX_TX15	1	90DIFF	PEX_TX15
PEX_TX15*	1	90DIFF	PEX_TX15
PEX_PLL_CLK_OUT	1	90DIFF	PEX_PLL_CLK_OUT
PEX_PLL_CLK_OUT*	1	90DIFF	PEX_PLL_CLK_OUT
PEX_RST*	3	50OHM	
PEX_TRST*	3	50OHM	
PEX_TCLK	3	50OHM	
PEX_TDI	3	50OHM	
PEX_TDO	3	50OHM	
PEX_TMS	3	50OHM	
JTAG_TCLK	3	50OHM	
JTAG_TMS	3	50OHM	
JTAG_TDI	3	50OHM	
JTAG_TDO	3	50OHM	
JTAG_TRST*	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
PEX_PLLAVDD	1.2V	0.25A	12MIL
PEX_PLLDVDD	1.2V	0.10A	12MIL

ASSEMBLY	P395 G92 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	PCI Express

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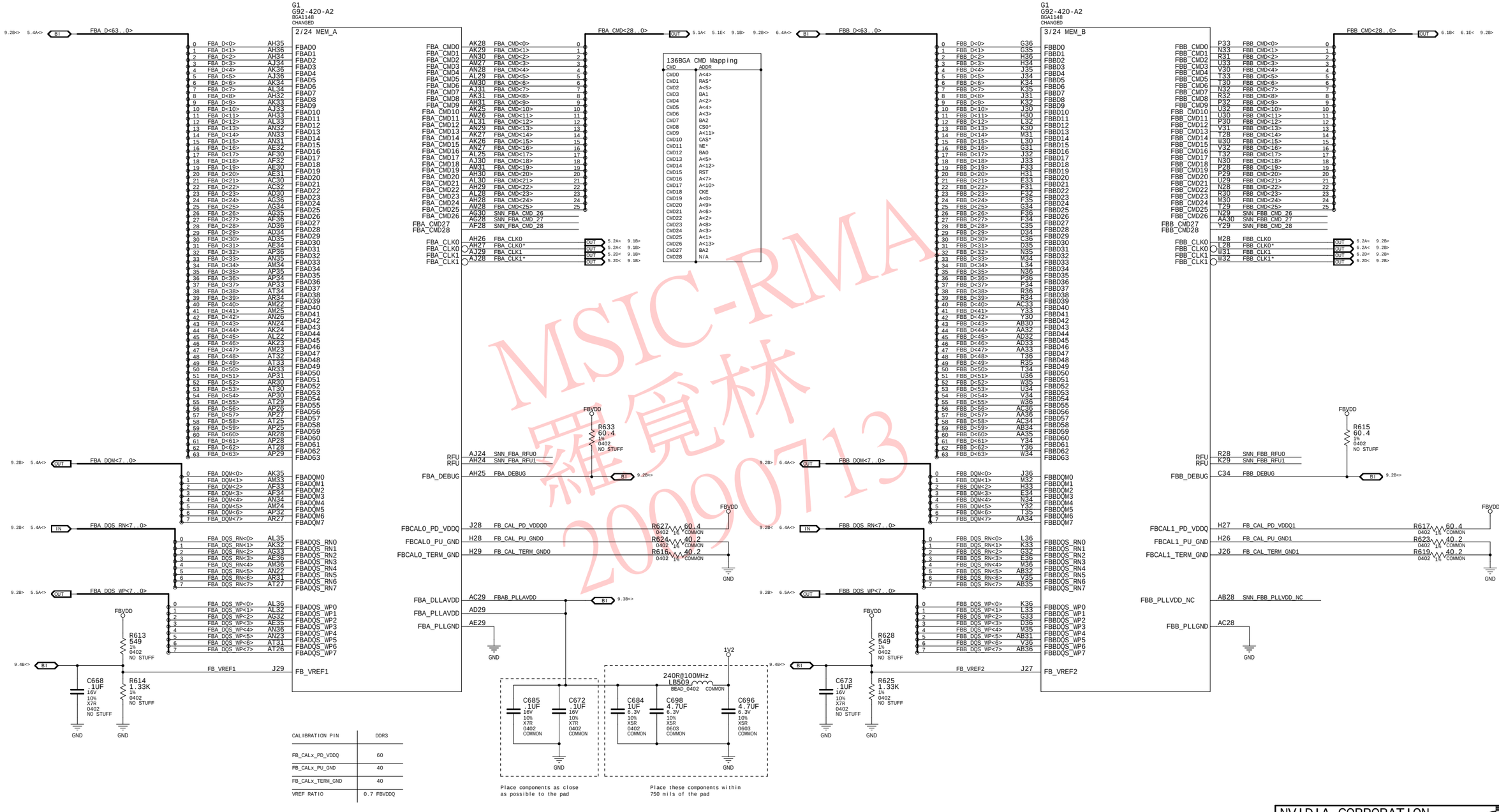
Page3: MEMORY: GPU Partition A/B



ASSEMBLY	P395 G92 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	MEMORY: GPU Partition A/B

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Page4: MEMORY: GPU Partition C/D

ASSEMBLY	P395 G92 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	MEMORY: GPU Partition C/D

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Page5: FBA Partition

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
A<2>	CMD22
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

M6 / M7
HY5RS123235BFP-11L
PACK_TYPE=BGA136_V2
VERSION=BGA136
COMMON

1	FBA_CMD<1>	H3	RAS	BA2	VDD	F1	FBVDD
10	FBA_CMD<10>	F4	CAS	CS0	VDD	M1	
11	FBA_CMD<11>	H9	WE	CKE	VDD	A2	
8	FBA_CMD<8>	F9	CS0	CAS	VDD	V2	
19	FBA_CMD<19>	K4	A0	A4	VDD	A11	
25	FBA_CMD<25>	H2	A1	A5	VDD	V11	
22	FBA_CMD<22>	K3	A2	A6	VDD	F12	
24	FBA_CMD<24>	M4	A3	A9	VDD	M12	
0	FBA_CMD<0>	K9	A4	A0	VDDQ	A1	FBVDD
2	FBA_CMD<2>	H11	A5	A1	VDDQ	C1	
21	FBA_CMD<21>	K10	A6	A2	VDDQ	E1	
16	FBA_CMD<16>	L9	A7	A11	VDDQ	N1	
23	FBA_CMD<23>	K11	A8/AP	A10	VDDQ	R1	
20	FBA_CMD<20>	M9	A9	A3	VDDQ	V1	
17	FBA_CMD<17>	K2	A10	A8/AP	VDDQ	C4	
9	FBA_CMD<9>	L4	A11	A7	VDDQ	E4	
					VDDQ	J4	
12	FBA_CMD<12>	G4	BA0	BA1	VDDQ	N4	
3	FBA_CMD<3>	G9	BA1	BA0	VDDQ	R4	
7	FBA_CMD<7>	H10	BA2	RAS	VDDQ	C9	
					VDDQ	E9	
18	FBA_CMD<18>	H4	CKE	WE	VDDQ	J9	
	FBA_CLK0	J11	CLK		VDDQ	N9	
	FBA_CLK0*	J10	CLK		VDDQ	R9	
					VDDQ	A12	
	SNN_FBA_NC0	J2	NC/RFU		VDDQ	C12	
14	FBA_CMD<14>	J3	NC/CS1	NC/CS1	VDDQ	E12	
	FBA_DEBUG_SEN0	V4	SEN (GND)		VDDQ	N12	
					VDDQ	R12	
					VDDQ	V12	
			NONMIRROR	MIRROR			
15	FBA_CMD<15>	V9	RESET		VSSQ	B1	GND
		A9	MIRROR		VSSQ	D1	
		A4	ZQ		VSSQ	P1	
					VSSQ	T1	
					VSSQ	G2	
					VSSQ	L2	
					VSSQ	B4	
					VSSQ	D4	
					VSSQ	P4	
					VSSQ	T4	
					VSSQ	B9	
					VSSQ	D9	
					VSSQ	P9	
					VSSQ	T9	
					VSSQ	G11	
					VSSQ	L11	
					VSSQ	B12	
					VSSQ	D12	
					VSSQ	P12	
					VSSQ	T12	
					VSS	G1	GND
					VSS	L1	
					VSS	A3	
					VSS	V3	
					VSS	A10	
					VSS	V10	
					VSS	G12	
					VSS	L12	
		K1	VDDA		VREF	H1	FBA_VREF0
		K12	VDDA		VREF	H12	FBA_VREF2
		J1	VSSA				
		J12	VSSA				

*CS1 is required 32Mx32 Memories

M6 / M7
HY5RS123235BFP-11L
PACK_TYPE=BGA136_V2
VERSION=BGA136
COMMON

0	FBA_D<0>	N2	DQ0	DQ0	VDD	F1	FBVDD
1	FBA_D<1>	M3	DQ1	DQ1	VDD	M1	
2	FBA_D<2>	L3	DQ2	DQ2	VDD	A2	
3	FBA_D<3>	M2	DQ3	DQ3	VDD	V2	
4	FBA_D<4>	T2	DQ4	DQ4	VDD	A11	
5	FBA_D<5>	R3	DQ5	DQ5	VDD	V11	
6	FBA_D<6>	R2	DQ6	DQ6	VDD	F12	
7	FBA_D<7>	T3	DQ7	DQ7	VDD	M12	
8	FBA_D<8>	L10	DQ0	DQ0	VDDQ	A1	FBVDD
9	FBA_D<9>	M10	DQ1	DQ1	VDDQ	C1	
10	FBA_D<10>	M11	DQ2	DQ2	VDDQ	E1	
11	FBA_D<11>	N11	DQ3	DQ3	VDDQ	N1	
12	FBA_D<12>	R10	DQ4	DQ4	VDDQ	R1	
13	FBA_D<13>	T11	DQ5	DQ5	VDDQ	V1	
14	FBA_D<14>	R11	DQ6	DQ6	VDDQ	C4	
15	FBA_D<15>	T10	DQ7	DQ7	VDDQ	E4	
					VDDQ	J4	
	FBA_DQM<0>	N3	DQM	DQM	VDDQ	N4	
	FBA_DQS_RN<0>	P3	RDQS	RDQS	VDDQ	R4	
	FBA_DQS_WP<0>	P2	WDQS	WDQS	VDDQ	C9	
					VDDQ	E9	
					VDDQ	J9	
					VDDQ	N9	
					VDDQ	R9	
					VDDQ	A12	
					VDDQ	C12	
					VDDQ	E12	
					VDDQ	N12	
					VDDQ	R12	
					VDDQ	V12	
16	FBA_D<16>	C11	DQ0	DQ0	VSSQ	B1	GND
17	FBA_D<17>	F10	DQ1	DQ1	VSSQ	D1	
18	FBA_D<18>	C10	DQ2	DQ2	VSSQ	P1	
19	FBA_D<19>	G10	DQ3	DQ3	VSSQ	T1	
20	FBA_D<20>	F11	DQ4	DQ4	VSSQ	G2	
21	FBA_D<21>	B11	DQ5	DQ5	VSSQ	L2	
22	FBA_D<22>	B10	DQ6	DQ6	VSSQ	B4	
23	FBA_D<23>	E11	DQ7	DQ7	VSSQ	D4	
					VSSQ	P4	
	FBA_DQM<2>	E10	DQM	DQM	VSSQ	T4	
	FBA_DQS_RN<2>	D10	RDQS	RDQS	VSSQ	B9	
	FBA_DQS_WP<2>	D11	WDQS	WDQS	VSSQ	D9	
					VSSQ	P9	
					VSSQ	T9	
					VSSQ	G11	
					VSSQ	L11	
					VSSQ	B12	
					VSSQ	D12	
					VSSQ	P12	
					VSSQ	T12	
					VSS	G1	GND
					VSS	L1	
					VSS	A3	
					VSS	V3	
					VSS	A10	
					VSS	V10	
					VSS	G12	
					VSS	L12	
		K1	VDDA		VREF	H1	FBA_VREF1
		K12	VDDA		VREF	H12	FBA_VREF3
		J1	VSSA				
		J12	VSSA				

*CS1 is required 32Mx32 Memories

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

Clock Term MUST BE PLACED as close as possible to the BGA memory on the line AFTER the memory pin!

Minimize STUB length!

Clock Term MUST BE PLACED as close as possible to the BGA memory on the line AFTER the memory pin!

Minimize STUB length!

Decoupling for FBA Lo

Decoupling for FBA Hi

Place 1uF caps at center of memory

Place 1uF caps at center of memory

ASSEMBLY	
PAGE DETAIL	FBA Partition

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2701 SAN TOMAS EXPRESSWAY
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Page6: FBB Partition

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
1A<6>	CMD21
1A<7>	CMD16
1A<8>	CMD23
1A<9>	CMD20
1A<10>	CMD17
1A<11>	CMD9
CKE	CMD18
RST	CMD15

Clock Term MUST BE PLACED as close as possible to the BGA memory on the line AFTER the memory pin!
Minimize STUB length!

M5 / M8 HY5RS123235BFP-11L PACK_TYPE=BGA136_V2 VERSION=BGA136 COMMON

*CS1 is required 32Mx32 Memories

Decoupling for FBB Lo

Decoupling for FBB Hi

Place 1uF caps at center of memory

ASSEMBLY	
PAGE DETAIL	FBB Partition

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Page7: FBC Partition

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

M3 / M4: HY5RS123235BFP-11L, PACK_TYPE=BGA136_V2, VERSION=BGA136, COMMON

FBC_CMD<28..0> (M3) / FBC_CMD<28..0> (M4)

FBC_D<63..0>

FBC_DQM<7..0>

FBC_DQS_RN<7..0>

FBC_DQS_WP<7..0>

Clock Term MUST BE PLACED as close as possible to the BGA memory on the line AFTER the memory pin!

Minimize STUB length!

*CS1 is required 32Mx32 Memories

Decoupling for FBC Lo

Decoupling for FBC Hi

Place 1uF caps at center of memory

ASSEMBLY	P395 G92 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	FBC Partition

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Page8: FBD Partition

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

M1 / M2: HY5RS123235BFP-11L, PACK_TYPE=BGA136_V2, VERSION=BGA136, COMMON

FBD_CMD<28..0> — FBD_CMD<0>, FBD_CMD<1>, FBD_CMD<2>, FBD_CMD<3>, FBD_CMD<4>, FBD_CMD<5>, FBD_CMD<6>, FBD_CMD<7>, FBD_CMD<8>, FBD_CMD<9>, FBD_CMD<10>, FBD_CMD<11>, FBD_CMD<12>, FBD_CMD<13>, FBD_CMD<14>, FBD_CMD<15>, FBD_CMD<16>, FBD_CMD<17>, FBD_CMD<18>, FBD_CMD<19>, FBD_CMD<20>, FBD_CMD<21>, FBD_CMD<22>, FBD_CMD<23>, FBD_CMD<24>, FBD_CMD<25>, FBD_CMD<28>

RAS, CAS, WE, CS0, A0, A1, A2, A3, A4, A5, A6, A7, A8/AP, A9, A10, A11, BA0, BA1, BA2, CKE, CLK, NC/RFU, NC/CS1, SEN (GND), RESET, MIRROR, ZQ

FBD_CLK0, FBD_CLK0* — R723 121 1% 0402 NO STUFF; FBD_CLK0_MIDPT — R722 243 1% 0402 COMMON; R721 243 1% 0402 COMMON; C940 .01UF 16V 10% X7R 0402 COMMON

FBD_CLK1, FBD_CLK1* — R673 121 1% 0402 NO STUFF; FBD_CLK1_MIDPT — R679 243 1% 0402 COMMON; R681 243 1% 0402 COMMON; C892 .01UF 16V 10% X7R 0402 COMMON

SNN_FBD0_NC1, FBD_CMD<14>, FBD_DEBUG_SEN0 — R710 0 5% 0402 COMMON

SNN_FBD1_NC1, FBD_CMD<14>, FBD_DEBUG_SEN1 — R29 0 5% 0402 COMMON

FBD_ZQ0 — R709 10K 5% 0402 COMMON; R714 10K 5% 0402 COMMON; R19 243 1% 0402 COMMON

FBD_ZQ1 — R45 243 1% 0402 COMMON

Clock Term MUST BE PLACED as close as possible to the BGA memory on the line AFTER the memory pin!
Minimize STUB length!

VDDA — C914 .047UF 16V 10% X7R 0402 COMMON; C932 .047UF 16V 10% X7R 0402 COMMON

VDDA — C904 .047UF 16V 10% X7R 0402 COMMON; C899 .047UF 16V 10% X7R 0402 COMMON

FBD_VREF0, FBD_VREF2 — R718 698 1% 0402 CHANGED R1; R716 1.33K 1% 0402 COMMON R2; C925 .1UF 16V 10% X7R 0402 COMMON; R15 698 1% 0402 CHANGED R1; R20 1.33K 1% 0402 COMMON R2; C17 .1UF 16V 10% X7R 0402 COMMON

FBD_VREF1, FBD_VREF3 — R31 698 1% 0402 CHANGED R1; R35 1.33K 1% 0402 COMMON R2; C39 .1UF 16V 10% X7R 0402 COMMON; R692 698 1% 0402 CHANGED R1; R687 1.33K 1% 0402 COMMON R2; C894 .1UF 16V 10% X7R 0402 COMMON

*CS1 is required 32Mx32 Memories

FBD_D<63..0>

FBD_DQM<7..0>

FBD_DQS_RN<7..0>

FBD_DQS_WP<7..0>

Decoupling for FBD Lo

FBVDD — C937 .1UF 16V 10% X7R 0402 COMMON; C929 .1UF 16V 10% X7R 0402 COMMON; C924 .1UF 16V 10% X7R 0402 COMMON; C919 .1UF 16V 10% X7R 0402 COMMON; C920 .1UF 16V 10% X7R 0402 COMMON; C926 .1UF 16V 10% X7R 0402 COMMON; C916 .1UF 16V 10% X7R 0402 COMMON; C942 .1UF 16V 10% X7R 0402 COMMON; C18 .1UF 16V 10% X7R 0402 COMMON; C930 .1UF 16V 10% X7R 0402 COMMON

C918 1UF 6.3V 10% X5R 0603 COMMON; C931 1UF 6.3V 10% X5R 0603 COMMON; C938 1UF 6.3V 10% X5R 0603 COMMON; C922 1UF 6.3V 10% X5R 0603 COMMON

Place 1uF caps at center of memory

C933 4.7UF 6.3V 10% X5R 0805 COMMON; C943 4.7UF 6.3V 10% X5R 0805 COMMON; C935 4.7UF 6.3V 10% X5R 0805 COMMON

C939 .1UF 16V 10% X7R 0402 NO STUFF; C921 .1UF 16V 10% X7R 0402 NO STUFF; C941 .1UF 16V 10% X7R 0402 NO STUFF; C936 .1UF 16V 10% X7R 0402 NO STUFF; C934 .1UF 16V 10% X7R 0402 NO STUFF; C923 .1UF 16V 10% X7R 0402 NO STUFF

Decoupling for FBD Hi

FBVDD — C905 .1UF 16V 10% X7R 0402 COMMON; C908 .1UF 16V 10% X7R 0402 COMMON; C901 .1UF 16V 10% X7R 0402 COMMON; C911 .1UF 16V 10% X7R 0402 COMMON; C910 .1UF 16V 10% X7R 0402 COMMON; C907 .1UF 16V 10% X7R 0402 COMMON; C903 .1UF 16V 10% X7R 0402 COMMON; C906 .1UF 16V 10% X7R 0402 COMMON; C898 .1UF 16V 10% X7R 0402 COMMON; C887 .1UF 16V 10% X7R 0402 COMMON

C912 1UF 6.3V 10% X7R 0603 COMMON; C882 1UF 6.3V 10% X7R 0603 COMMON; C896 1UF 6.3V 10% X7R 0603 COMMON; C900 1UF 6.3V 10% X7R 0603 COMMON

Place 1uF caps at center of memory

C913 4.7UF 6.3V 10% X5R 0805 COMMON; C881 4.7UF 6.3V 10% X5R 0805 COMMON; C889 4.7UF 6.3V 10% X5R 0805 COMMON

C915 .1UF 16V 10% X7R 0402 NO STUFF; C917 .1UF 16V 10% X7R 0402 NO STUFF; C35 .1UF 16V 10% X7R 0402 NO STUFF; C902 .1UF 16V 10% X7R 0402 NO STUFF; C885 .1UF 16V 10% X7R 0402 NO STUFF; C888 .1UF 16V 10% X7R 0402 NO STUFF

R688 121 1% 0402 COMMON; R694 121 1% 0402 COMMON; R693 121 1% 0402 COMMON; R700 121 1% 0402 COMMON; R715 121 1% 0402 COMMON; R711 121 1% 0402 COMMON; R717 121 1% 0402 COMMON; R720 121 1% 0402 COMMON

ASSEMBLY	
PAGE DETAIL	FBD Partition

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Page9: FrameBuffer Net Rules

NET RULES for FrameBuffer A/B

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBA_CLK0	1	80DIFF	FBA_CLK0
FBA_CLK0*	1	80DIFF	FBA_CLK0
FBA_CLK1	1	80DIFF	FBA_CLK1
FBA_CLK1*	1	80DIFF	FBA_CLK1
FBA_CMD<28..0>	1	40OHM	
FBA_DQS_WP<7..0>	1	40OHM	
FBA_DQS_RN<7..0>	1	40OHM	
FBA_DQ#<7..0>	1	40OHM	
FBA_D<63..0>	1	40OHM	

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBB_CLK0	1	80DIFF	FBB_CLK0
FBB_CLK0*	1	80DIFF	FBB_CLK0
FBB_CLK1	1	80DIFF	FBB_CLK1
FBB_CLK1*	1	80DIFF	FBB_CLK1
FBB_CMD<28..0>	1	40OHM	
FBB_DQS_WP<7..0>	1	40OHM	
FBB_DQS_RN<7..0>	1	40OHM	
FBB_DQ#<7..0>	1	40OHM	
FBB_D<63..0>	1	40OHM	
FBA_DEBUG	1	40OHM	
FBB_DEBUG	1	40OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBAB_PLLAVDD	1.2V	0.02A	12MIL
FBA_VREF0	1.40V	0.02A	12MIL
FBA_VREF1	1.40V	0.02A	12MIL
FBA_VREF2	1.40V	0.02A	12MIL
FBA_VREF3	1.40V	0.02A	12MIL
FBA_ZQ0	2.0V	0.02A	12MIL
FBA_ZQ1	2.0V	0.02A	12MIL
FBB_VREF0	1.40V	0.02A	12MIL
FBB_VREF1	1.40V	0.02A	12MIL
FBB_VREF2	1.40V	0.02A	12MIL
FBB_VREF3	1.40V	0.02A	12MIL
FBB_ZQ0	2.0V	0.02A	12MIL
FBB_ZQ1	2.0V	0.02A	12MIL
FB_VREF1	1.40V	0.02A	12MIL
FB_VREF2	1.40V	0.02A	12MIL

NET RULES for FrameBuffer C/D

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBC_CLK0	1	80DIFF	FBC_CLK0
FBC_CLK0*	1	80DIFF	FBC_CLK0
FBC_CLK1	1	80DIFF	FBC_CLK1
FBC_CLK1*	1	80DIFF	FBC_CLK1
FBC_CMD<28..0>	1	40OHM	
FBC_DQS_WP<7..0>	1	40OHM	
FBC_DQS_RN<7..0>	1	40OHM	
FBC_DQ#<7..0>	1	40OHM	
FBC_D<63..0>	1	40OHM	

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBD_CLK0	1	80DIFF	FBD_CLK0
FBD_CLK0*	1	80DIFF	FBD_CLK0
FBD_CLK1	1	80DIFF	FBD_CLK1
FBD_CLK1*	1	80DIFF	FBD_CLK1
FBD_CMD<28..0>	1	40OHM	
FBD_DQS_WP<7..0>	1	40OHM	
FBD_DQS_RN<7..0>	1	40OHM	
FBD_DQ#<7..0>	1	40OHM	
FBD_D<63..0>	1	40OHM	
FBC_DEBUG	1	450HM	
FBD_DEBUG	1	40OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBCD_PLLAVDD	1.2V	0.02A	12MIL
FBC_VREF0	1.40V	0.02A	12MIL
FBC_VREF1	1.40V	0.02A	12MIL
FBC_VREF2	1.40V	0.02A	12MIL
FBC_VREF3	1.40V	0.02A	12MIL
FBC_ZQ0	2.0V	0.02A	12MIL
FBC_ZQ1	2.0V	0.02A	12MIL
FBD_VREF0	1.40V	0.02A	12MIL
FBD_VREF1	1.40V	0.02A	12MIL
FBD_VREF2	1.40V	0.02A	12MIL
FBD_VREF3	1.40V	0.02A	12MIL
FBD_ZQ0	2.0V	0.02A	12MIL
FBD_ZQ1	2.0V	0.02A	12MIL

ASSEMBLY	P395_G92_512MB_GDDR3_16Mx32_DVI-I+DVI-I
PAGE DETAIL	FrameBuffer Net Rules

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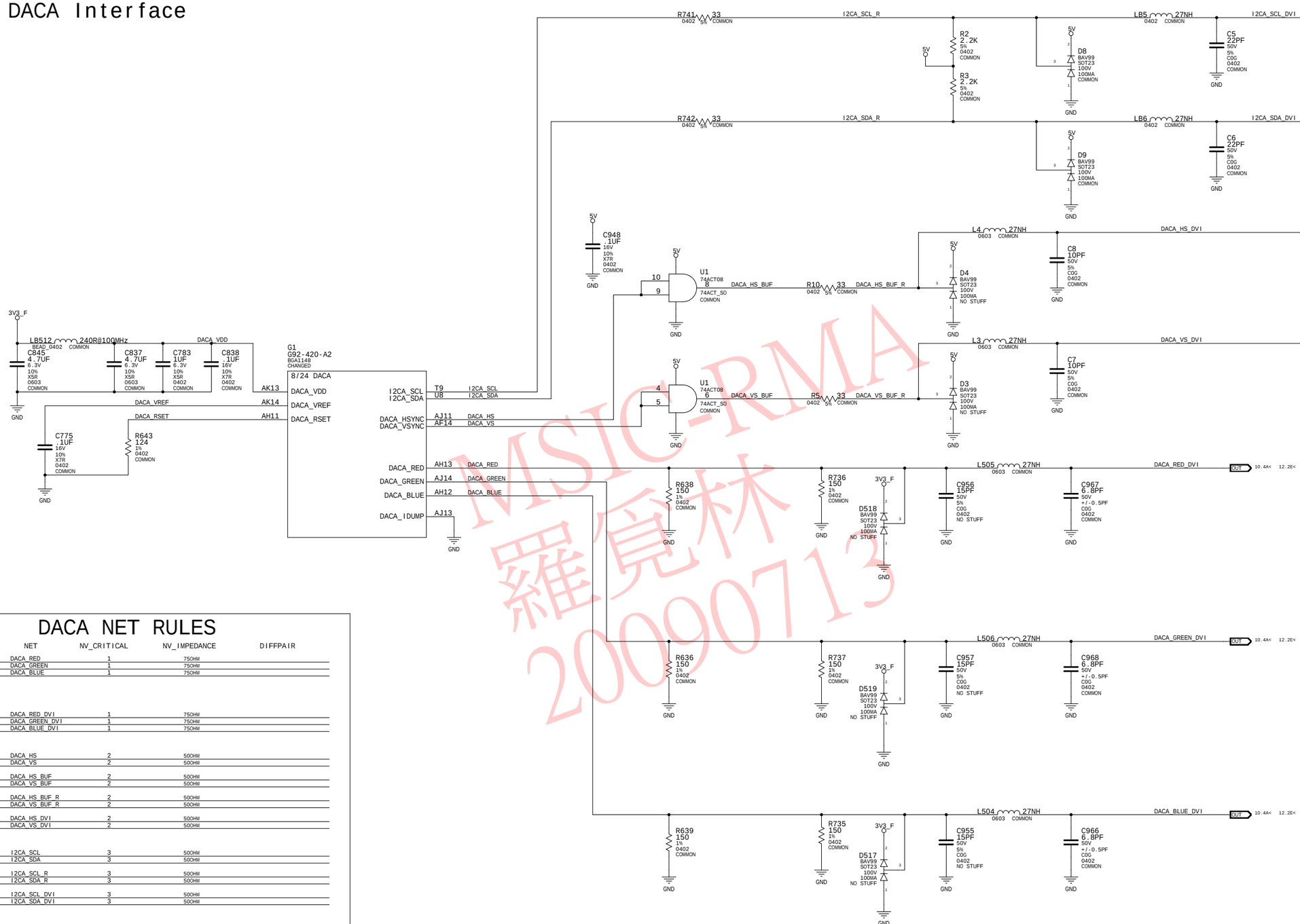
Page10: DACA Interface



DACA NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	DACA_RED	1	75OHM	
IN	DACA_GREEN	1	75OHM	
IN	DACA_BLUE	1	75OHM	
12.2E< 10.3G> IN	DACA_RED_DVI	1	75OHM	
12.2E< 10.4G> IN	DACA_GREEN_DVI	1	75OHM	
12.2E< 10.4G> IN	DACA_BLUE_DVI	1	75OHM	
IN	DACA_HS	2	50OHM	
IN	DACA_VS	2	50OHM	
IN	DACA_HS_BUF	2	50OHM	
IN	DACA_VS_BUF	2	50OHM	
IN	DACA_HS_BUF_R	2	50OHM	
IN	DACA_VS_BUF_R	2	50OHM	
12.2E< 10.2H> IN	DACA_HS_DVI	2	50OHM	
12.2E< 10.2H> IN	DACA_VS_DVI	2	50OHM	
IN	I2CA_SCL	3	50OHM	
IN	I2CA_SDA	3	50OHM	
IN	I2CA_SCL_R	3	50OHM	
IN	I2CA_SDA_R	3	50OHM	
12.2E< 10.1H> IN	I2CA_SCL_DVI	3	50OHM	
12.2E< 10.1H> IN	I2CA_SDA_DVI	3	50OHM	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	DACA_VREF			12MIL
IN	DACA_RSET			12MIL
BI	DACA_VDD	3.3V	0.100A	16MIL
IN	DACA_GND	0.0V		16MIL

ASSEMBLY	P395 G92 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	DACA Interface

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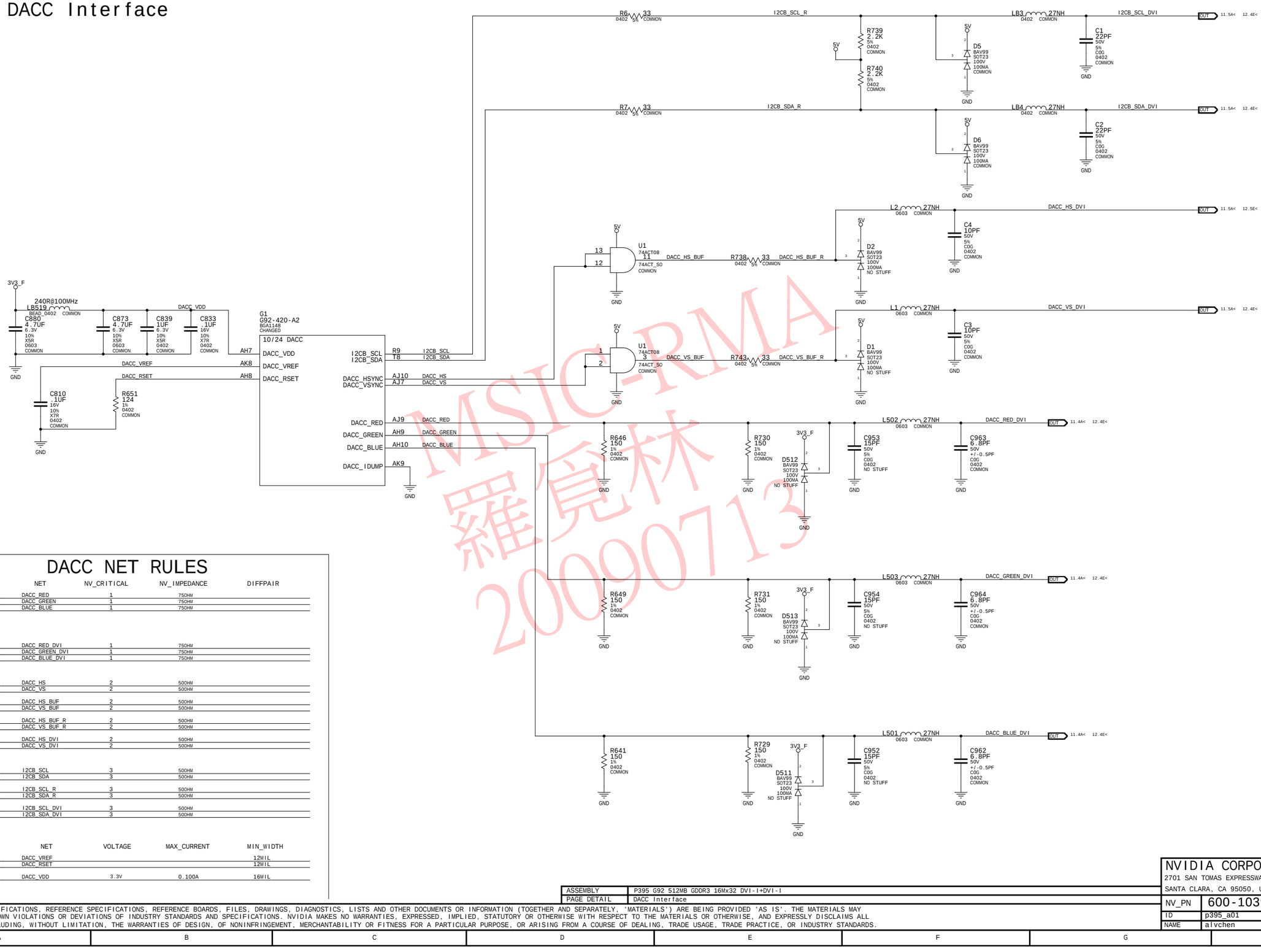
Page11: DACC Interface



DACC NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	DACC_RED	1	75OHM	
IN	DACC_GREEN	1	75OHM	
IN	DACC_BLUE	1	75OHM	
12.4E< 11.3G> IN	DACC_RED_DVI	1	75OHM	
12.4E< 11.4G> IN	DACC_GREEN_DVI	1	75OHM	
12.4E< 11.4G> IN	DACC_BLUE_DVI	1	75OHM	
IN	DACC_HS	2	50OHM	
IN	DACC_VS	2	50OHM	
IN	DACC_HS_BUF	2	50OHM	
IN	DACC_VS_BUF	2	50OHM	
IN	DACC_HS_BUF_R	2	50OHM	
IN	DACC_VS_BUF_R	2	50OHM	
12.5E< 11.2H> IN	DACC_HS_DVI	2	50OHM	
12.4E< 11.2H> IN	DACC_VS_DVI	2	50OHM	
IN	I2CB_SCL	3	50OHM	
IN	I2CB_SDA	3	50OHM	
IN	I2CB_SCL_R	3	50OHM	
IN	I2CB_SDA_R	3	50OHM	
12.4E< 11.1H> IN	I2CB_SCL_DVI	3	50OHM	
12.4E< 11.1H> IN	I2CB_SDA_DVI	3	50OHM	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	DACC_VREF			12MIL
IN	DACC_RSET			12MIL
BI	DACC_VDD	3.3V	0.100A	16MIL

ASSEMBLY	P395 G92 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	DACC Interface

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Page12: IFP A/B and C/D Interface

IFPABCD NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	IFPAB_RSET			12MIL
IN	IFPCD_RSET			12MIL

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	IFPAB_PLLVDD	1.8V	0.03A	16MIL
IN	IFPAB_IOVDD	3.3V	0.09A	16MIL
IN	IFPCD_IOVDD	3.3V	0.09A	16MIL

NET RULES

	NET	DIFFPAIR	NV_CRITICAL	NV_IMPEDANCE
IFPA_TXC / IFPA_TXC	IFPAB_TXC*	IFPAB_TXC	1	90DIFF
	IFPAB_TXC	IFPAB_TXC	1	90DIFF
IFPA_TXD0 / IFPA_TXD0	IFPAB_TXD0*	IFPAB_TXD0	1	90DIFF
	IFPAB_TXD0	IFPAB_TXD0	1	90DIFF
IFPA_TXD1 / IFPA_TXD1	IFPAB_TXD1*	IFPAB_TXD1	1	90DIFF
	IFPAB_TXD1	IFPAB_TXD1	1	90DIFF
IFPA_TXD2 / IFPA_TXD2	IFPAB_TXD2*	IFPAB_TXD2	1	90DIFF
	IFPAB_TXD2	IFPAB_TXD2	1	90DIFF
IFPA_TXD3 / IFPA_TXD3	SNN_IFPAB_TXD3*			
	SNN_IFPAB_TXD3			
IFPB_TXC / IFPB_TXC	SNN_IFPB_TXC*			
	SNN_IFPB_TXC			
IFPB_TXD4 / IFPB_TXD4	IFPAB_TXD4*	IFPAB_TXD4	1	90DIFF
	IFPAB_TXD4	IFPAB_TXD4	1	90DIFF
IFPB_TXD5 / IFPB_TXD5	IFPAB_TXD5*	IFPAB_TXD5	1	90DIFF
	IFPAB_TXD5	IFPAB_TXD5	1	90DIFF
IFPB_TXD6 / IFPB_TXD6	IFPAB_TXD6*	IFPAB_TXD6	1	90DIFF
	IFPAB_TXD6	IFPAB_TXD6	1	90DIFF
IFPB_TXD7 / IFPB_TXD7	SNN_IFPAB_TXD7*			
	SNN_IFPAB_TXD7			

NET RULES

	NET	DIFFPAIR	NV_CRITICAL	NV_IMPEDANCE
IFPC_TXC / IFPC_TXC	IFPCD_TXC*	IFPC_TXC	1	90DIFF
	IFPCD_TXC	IFPC_TXC	1	90DIFF
IFPC_TXD0 / IFPC_TXD0	IFPCD_TXD0*	IFPCD_TXD0	1	90DIFF
	IFPCD_TXD0	IFPCD_TXD0	1	90DIFF
IFPC_TXD1 / IFPC_TXD1	IFPCD_TXD1*	IFPCD_TXD1	1	90DIFF
	IFPCD_TXD1	IFPCD_TXD1	1	90DIFF
IFPC_TXD2 / IFPC_TXD2	IFPCD_TXD2*	IFPCD_TXD2	1	90DIFF
	IFPCD_TXD2	IFPCD_TXD2	1	90DIFF
IFPD_TXC / IFPD_TXC	SNN_IFPD_TXC*			
	SNN_IFPD_TXC			
IFPD_TXD4 / IFPD_TXD4	IFPCD_TXD4*	IFPCD_TXD4	1	90DIFF
	IFPCD_TXD4	IFPCD_TXD4	1	90DIFF
IFPD_TXD5 / IFPD_TXD5	IFPCD_TXD5*	IFPCD_TXD5	1	90DIFF
	IFPCD_TXD5	IFPCD_TXD5	1	90DIFF
IFPD_TXD6 / IFPD_TXD6	IFPCD_TXD6*	IFPCD_TXD6	1	90DIFF
	IFPCD_TXD6	IFPCD_TXD6	1	90DIFF

ASSEMBLY	P395 G92 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	IFP A/B and C/D Interface

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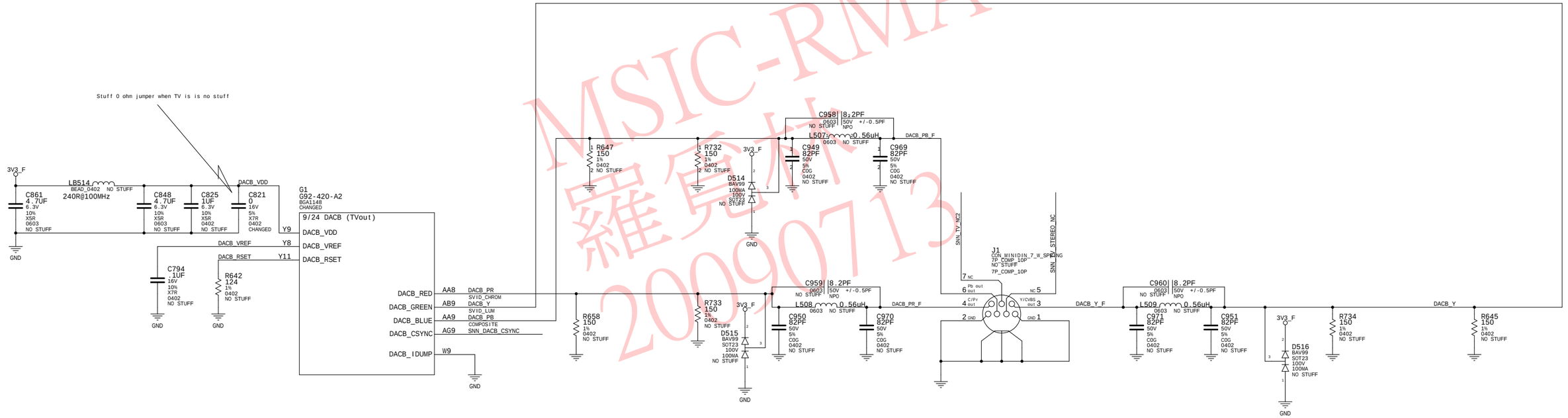
Page13: DACB ,HDTV

DACB NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	DACB_PR	1	75OHM	
IN	DACB_Y	1	75OHM	
IN	DACB_PB	1	75OHM	
IN	DACB_PR_F	1	75OHM	
IN	DACB_Y_F	1	75OHM	
IN	DACB_PB_F	1	75OHM	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	DACB_VDD	3.3V	0.2A	12MIL
IN	DACB_VREF			12MIL
IN	DACB_RSET			12MIL



ASSEMBLY	P395 G92 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	DACB

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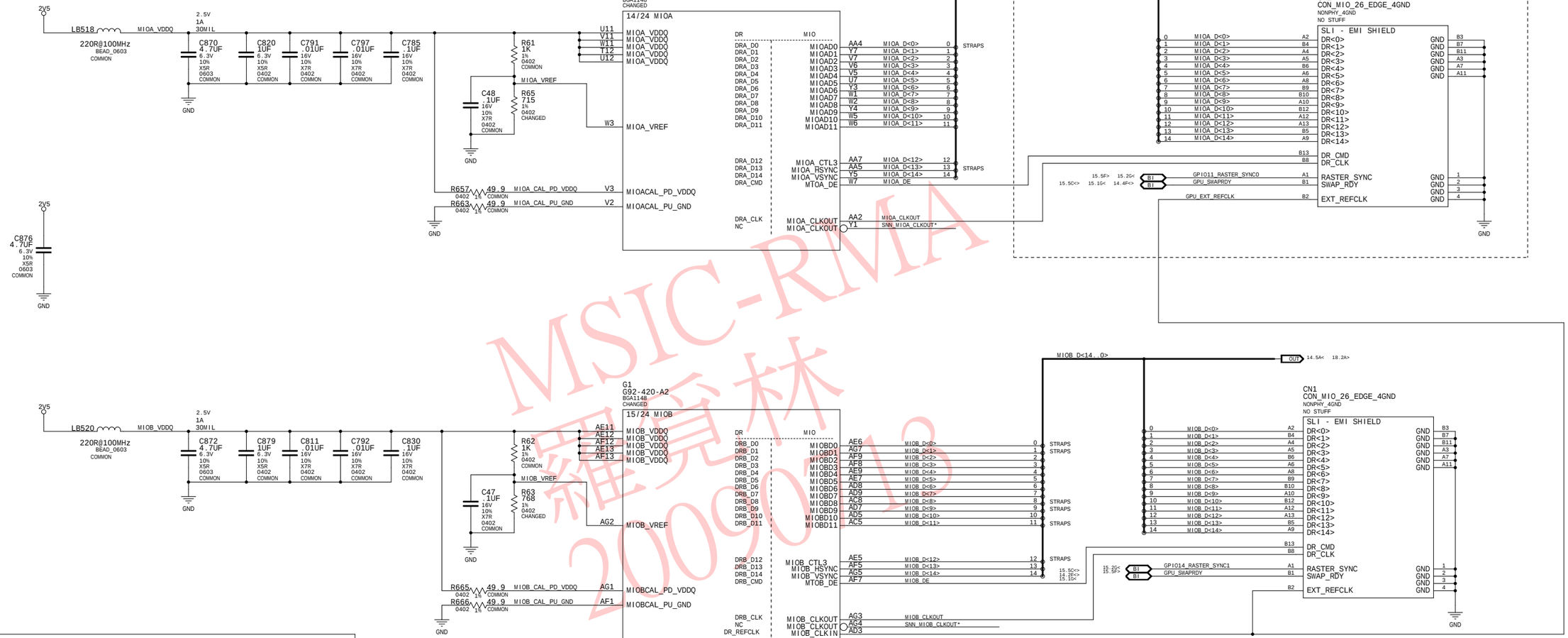
Page14: Multi-use IO(MIO) Interface



MIO NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
18.2A> 14.1H<	MIOA D<14..0>	1	50OHM	
	MIOA CLKOUT	1	50OHM	
	MIOA_DE	1	50OHM	
18.2A> 14.3G>	MIOB D<14..0>	1	50OHM	
	MIOB_CLKOUT	1	50OHM	
	MIOB_DE	1	50OHM	
	GPU_EXT_REFCLK	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	1.25V		12MIL
MIOACAL_PD_VDDQ			12MIL
MIOACAL_PU_GND			12MIL
MIOB_VREF	1.25V		12MIL
MIOBCAL_PD_VDDQ			12MIL
MIOBCAL_PU_GND			12MIL

ASSEMBLY	P395 G92 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	Multi-use IO(MIO) Interface

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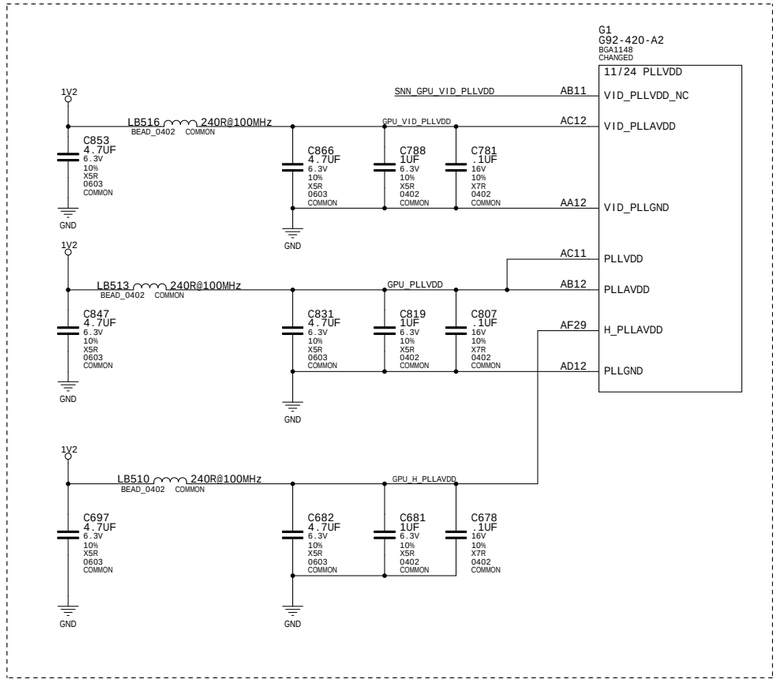
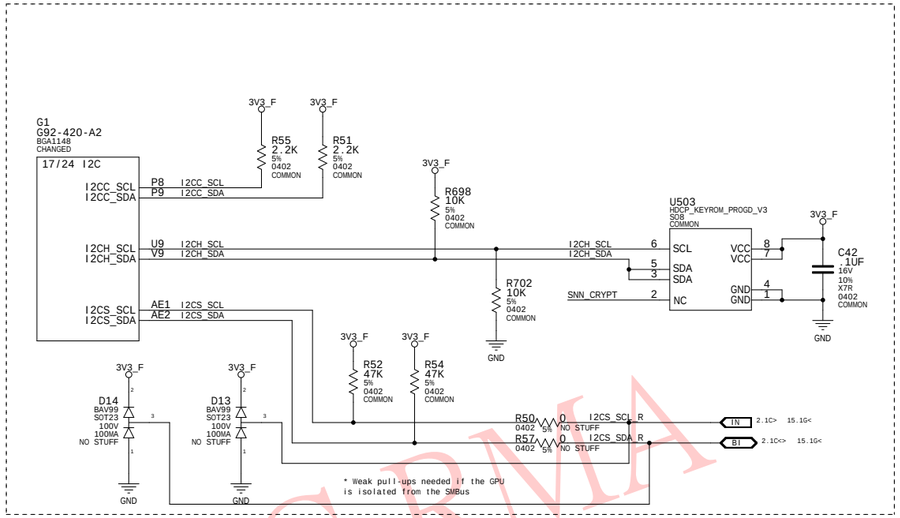
Page15: MISC: GPIO, I2C, BIOS, and PLL

PLLVDD/VID_PLLVDD



I2CC / I2CH(+ HDCP ROM) / I2CS

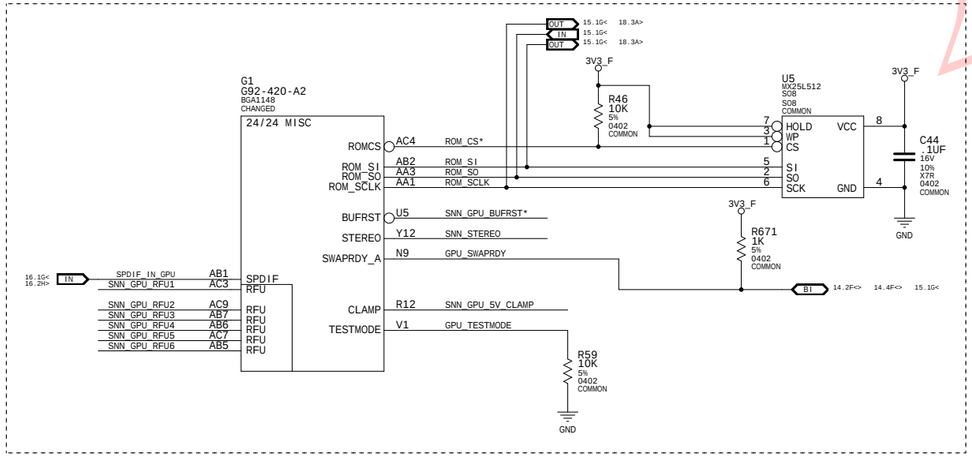


MISC NET RULES

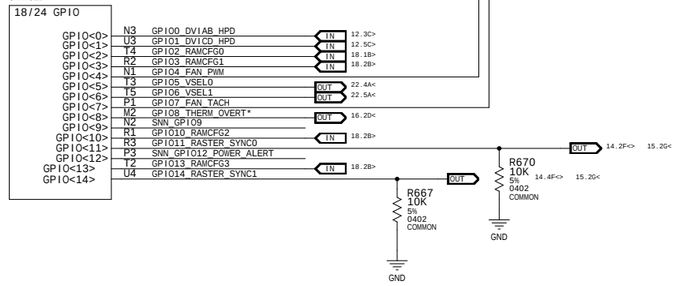
NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN I2CC_SCL	3	50OHM	
IN I2CC_SDA	3	50OHM	
IN I2CH_SCL	3	50OHM	
IN I2CH_SDA	3	50OHM	
IN I2CS_SCL	3	50OHM	
IN I2CS_SDA	3	50OHM	
15.2F< 2.1C> IN I2CS_SCL_R	3	50OHM	
15.2F<> 2.1C<> IN I2CS_SDA_R	3	50OHM	
IN ROM_CS*	3	50OHM	
18.3A> 15.4B> IN ROM_SI	3	50OHM	
15.4B< IN ROM_SO	3	50OHM	
18.3A> 15.4B> IN ROM_SCLK	3	50OHM	
15.5C<> 14.4F<> 14.2F<> IN GPU_SWAPRDY	3	50OHM	
15.5F> 14.4F<> IN GPIO14_RASTER_SYNC1	3	50OHM	
15.5F> 14.2F<> IN GPIO11_RASTER_SYNC0	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN GPU_PLLVDD	1.2V	0.05A	12MIL
IN GPU_VID_PLLVDD	1.2V	0.05A	12MIL
IN GPU_H_PLLAVDD	1.2V	0.05A	12MIL

ROM / MISC (BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)



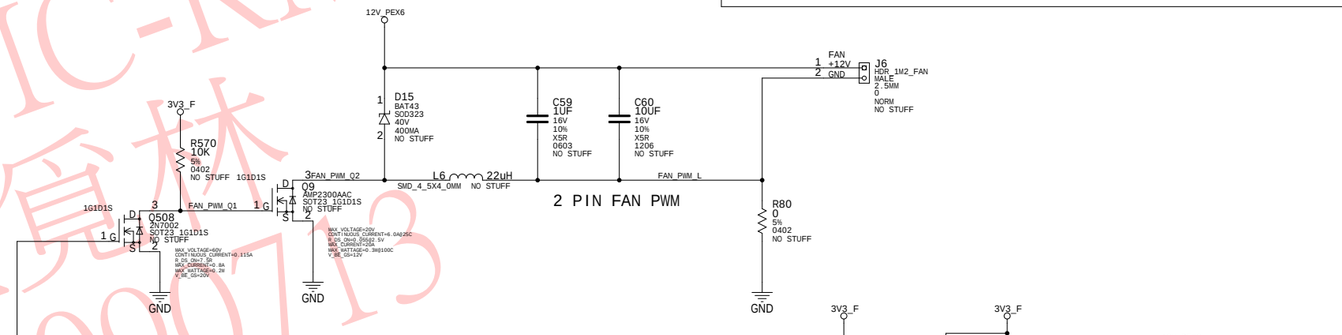
GPIO



GPIO Assignment Table

GPIO	I/O	Function
0	IN	DVI Hotplug Detect South
1	IN	DVI Hotplug Detect MID
2	IN	FB CFG0
3	IN	FB CFG1
4	OUT	Fan PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fan Tach Input
8	OUT	THERM_OVERT*
9	N/A	NOT USED
10	IN	FB CFG2
11	OUT	RASTER (SLI) SYNC0
12	N/A	NOT USED
13	IN	FB CFG3
14	IN	RASTER (SLI) SYNC1

2 PIN FAN PWM



ASSEMBLY	
PAGE DETAIL	MISC: GPIO, I2C, BIOS, and PLL

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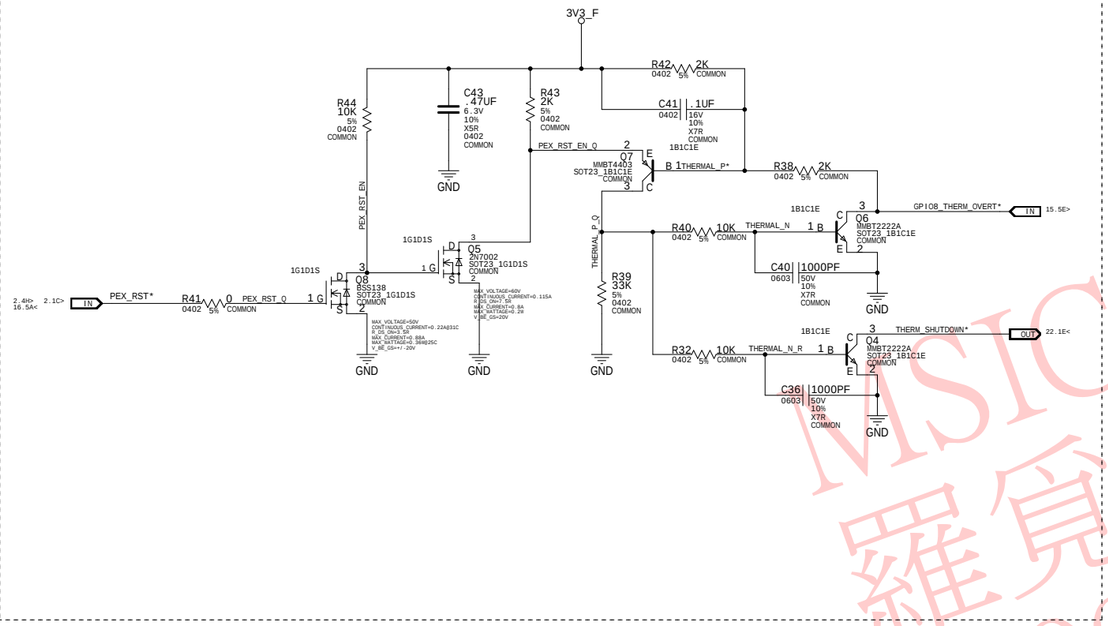
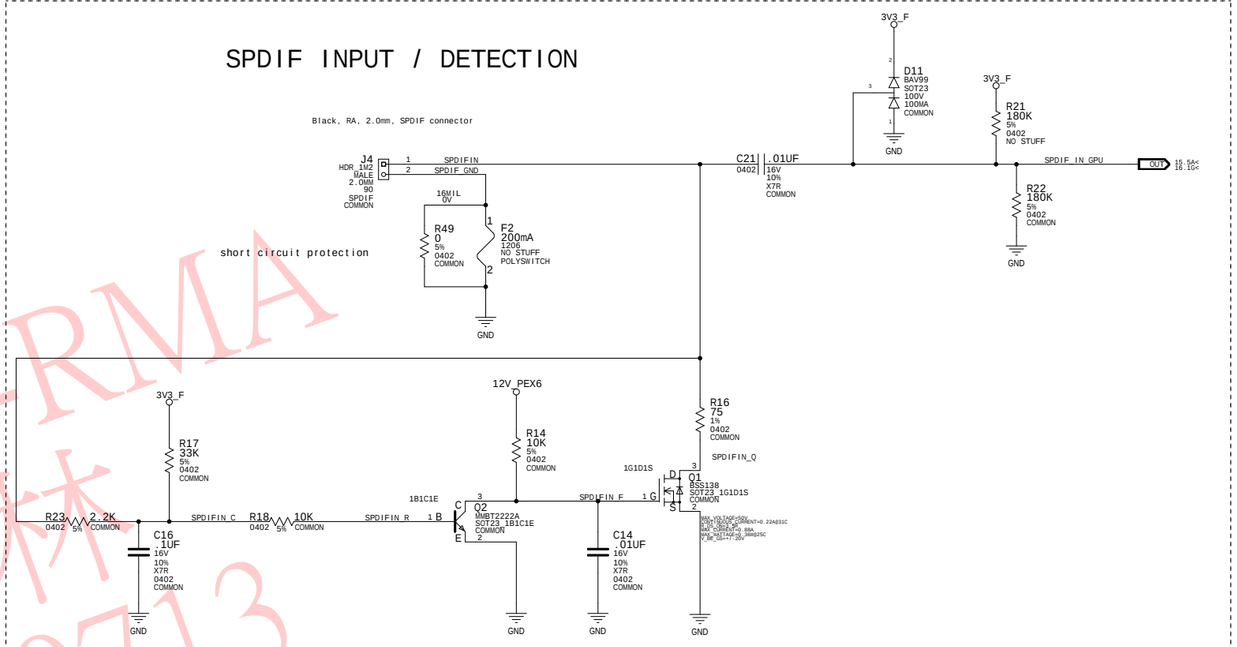
Page16: Thermal Control/Protection , XTAL and SPDIF Input

NET	IMPEDANCE	NV_CRITICAL_NET	MIN_LINE_WIDTH
SPDIFIN	50OHM	1	
SPDIFIN_Q	50OHM	1	
SPDIF_IN_GPU	50OHM	1	
XTAL_SSIN	1	50OHM	
XTAL_IN	1	50OHM	
XTAL_OUT	1	50OHM	
XTAL_OUTBUFF	1	50OHM	

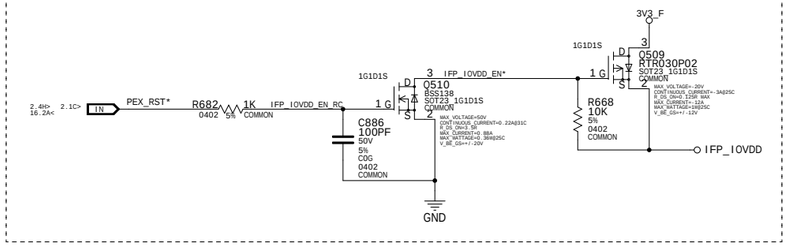
Thermal Protection



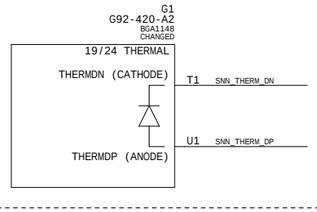
SPDIF INPUT / DETECTION



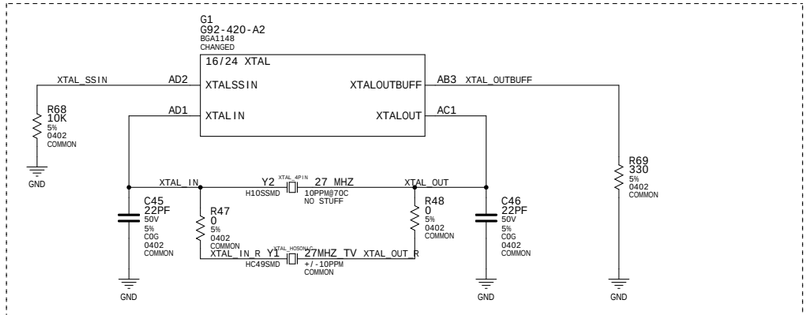
TMDS BACKDRIVE



THERMAL CONTROL



XTAL



ASSEMBLY	
PAGE DETAIL	Thermal Control/Protection, XTAL and SPDIF Input

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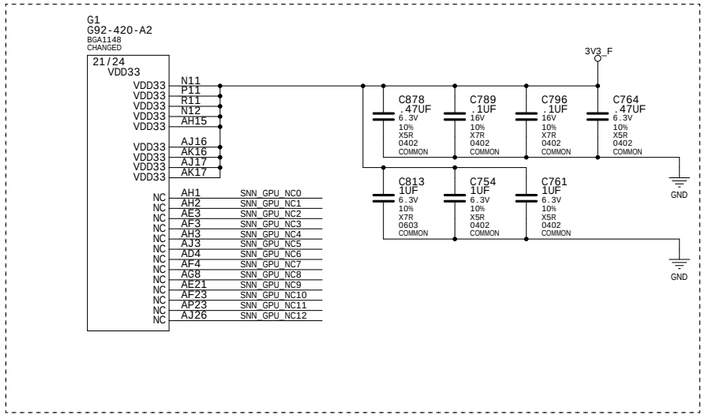
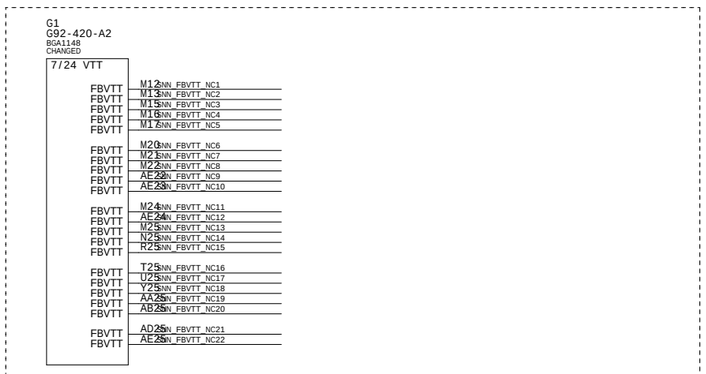
Page17: Power/GND and Decoupling

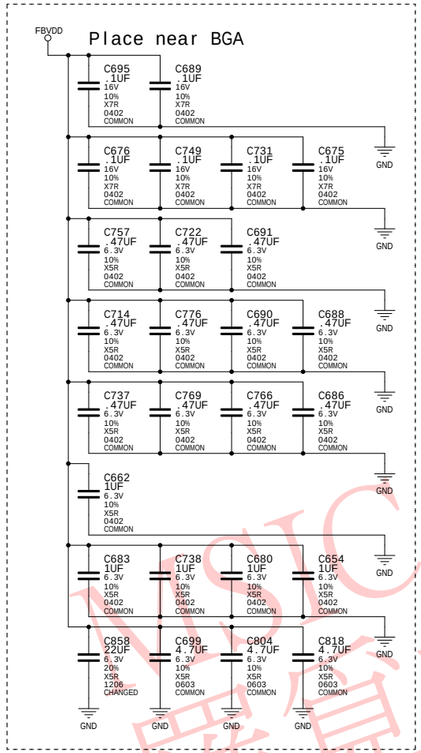
VDD33



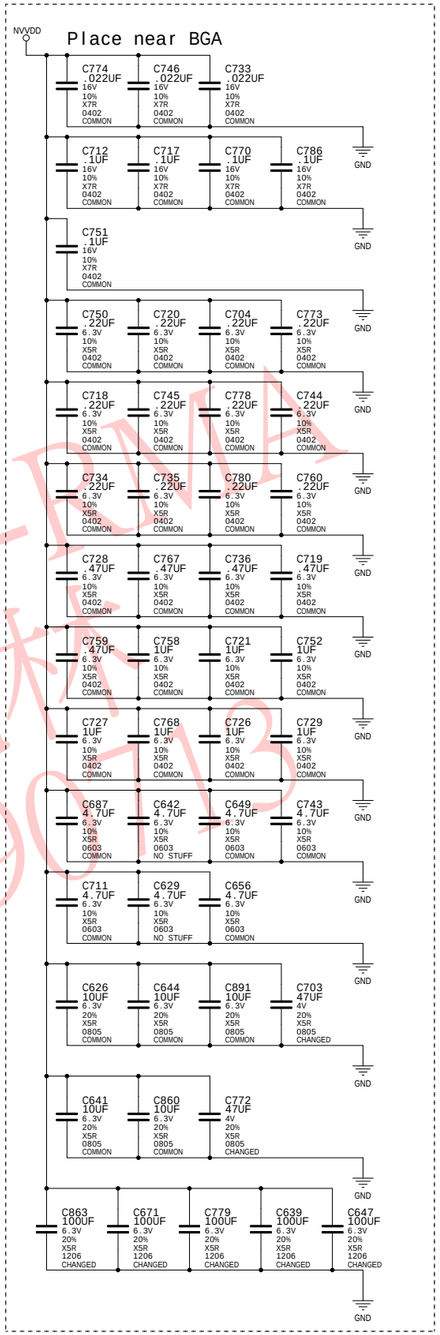
FBVTT

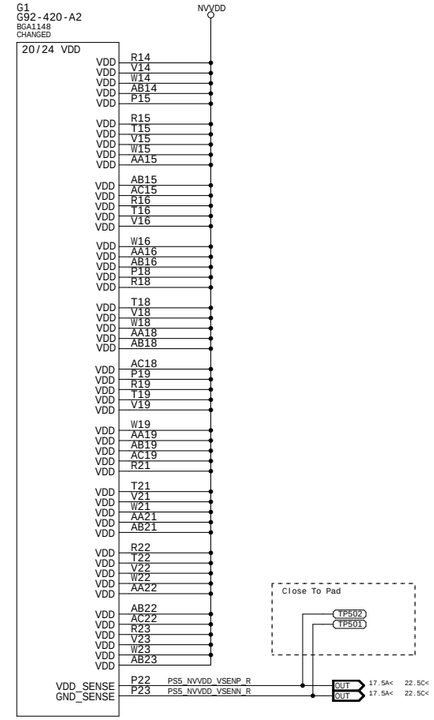


FBVDDQ



NVVDD





NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
PS5_NVVDD_VSENP_R	1	80DIFF	NVVDD_SENSE
PS5_NVVDD_VSENN_R	1	80DIFF	NVVDD_SENSE

ASSEMBLY	
PAGE DETAIL	Power/GND and Decoupling

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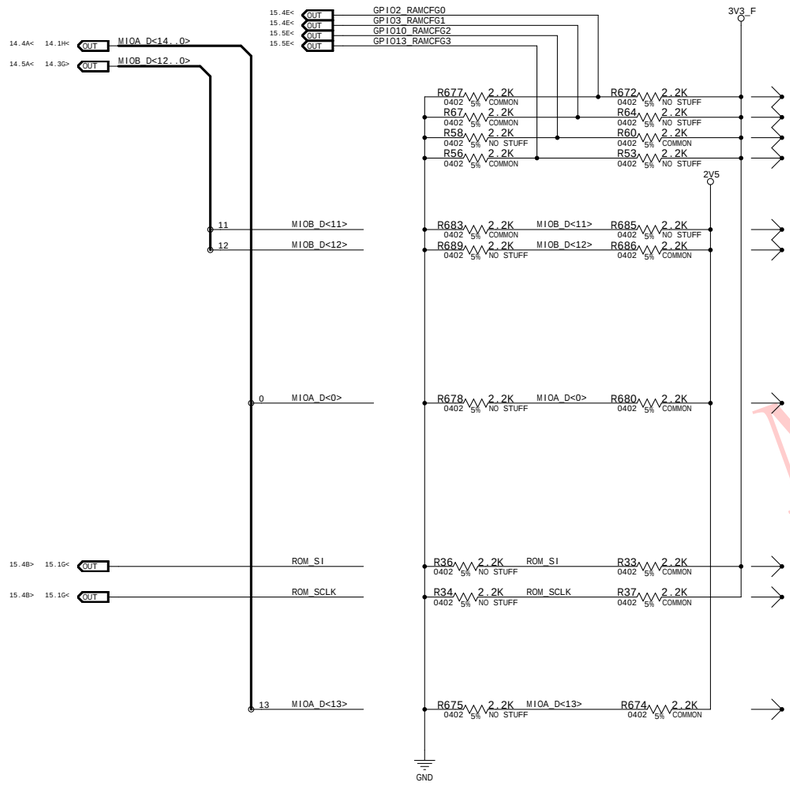
Page18: Configuration Straps and Mechanical

STRAPS



STRAP 0

		Samsung	Hynix	Hynix
		256b 16Mx32 512MB	256b 16Mx32 512MB	256b 32Mx32 1024MB
* 02:	RAM_CFG[0]	0	0	0
* 03:	RAM_CFG[1]	0	1	1
* 04:	RAM_CFG[2]	1	0	1
* 05:	RAM_CFG[3]	0	0	0

* 13:	PCI_DEVID[3]	DEVID = 0x0615 DT G92-428 0001 0101
* 28:	PCI_DEVID[4]	

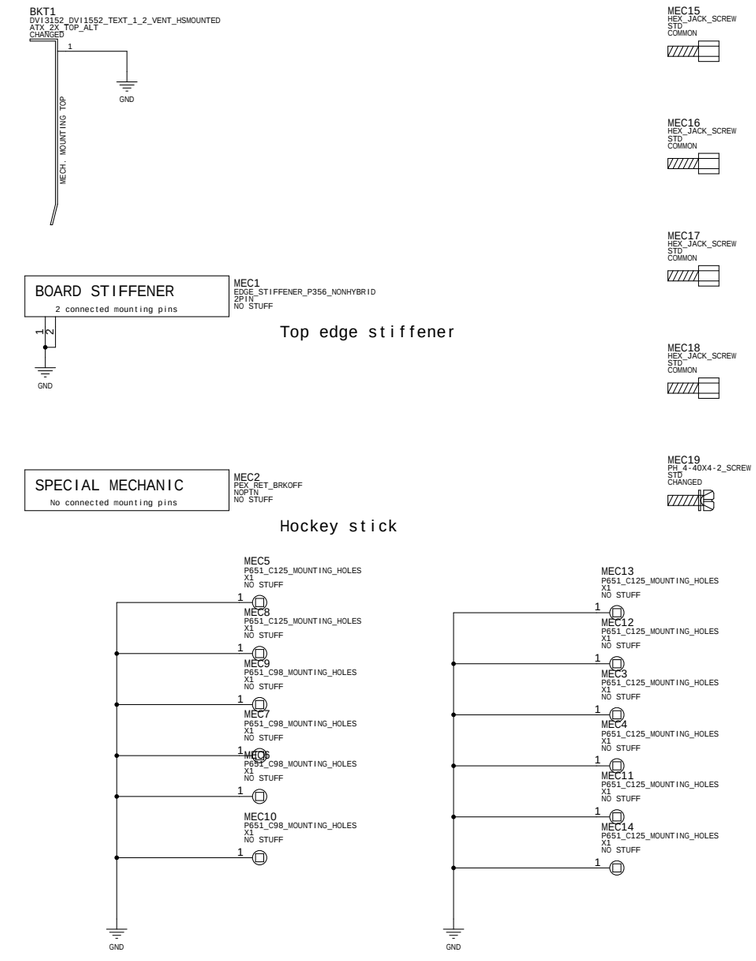
4 3

* 17:	PEX_PLL_EN_TERM100	Per G92 Guide (PEX term).. * Strap definition inverted - set to 0x1 to enable - set to 0x0 to disable

STRAP 1

* 12:	MIO_EN_33V_0	DEFAULT = 1 (3.3V) MIOA = 0 (2.5V)
* 13:	MIO_EN_33V_1	DEFAULT = 1 (3.3V) MIOB = 0 (2.5V)
* 15:	SLOT_CLK_CFG	DISABLE = 0; ENABLE = 1

MECHANICAL



ASSEMBLY	
PAGE DETAIL	Configuration Straps and Mechanical

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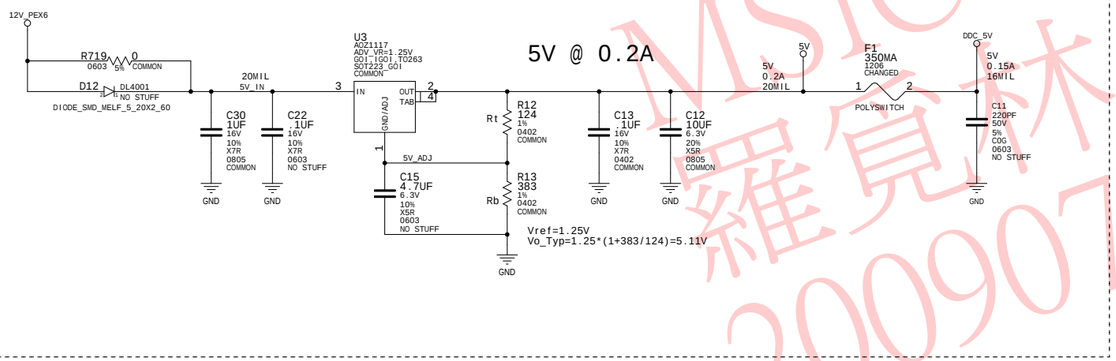
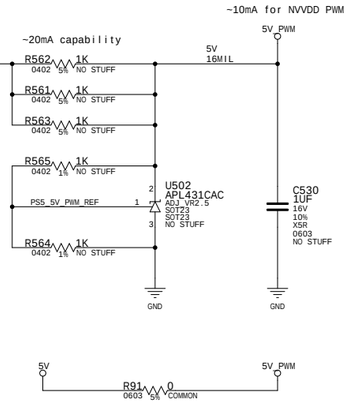
Page19: Power Supply: 5V

5V and DDC5V Supply



NVVDD PWM 5V Supply



ASSEMBLY	
PAGE DETAIL	Power Supply: 5V

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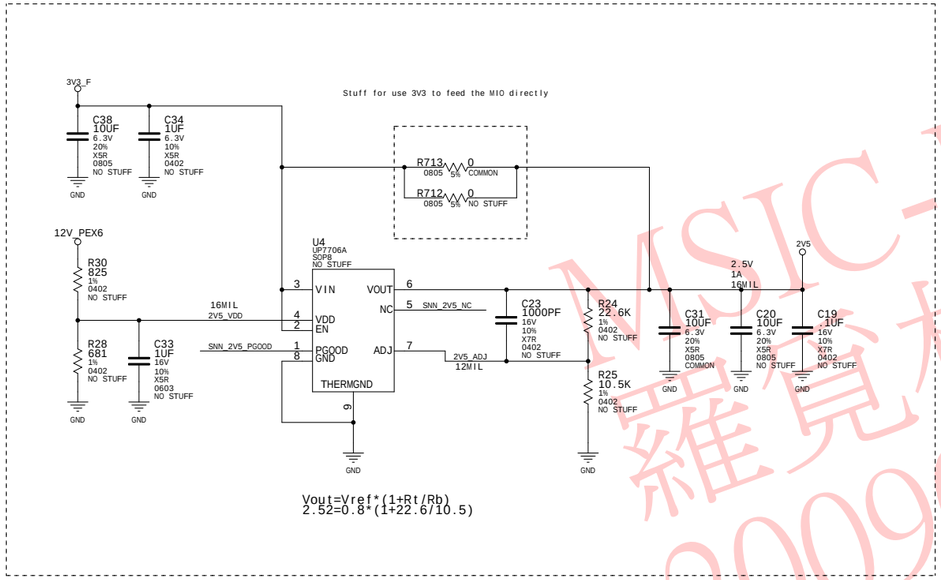
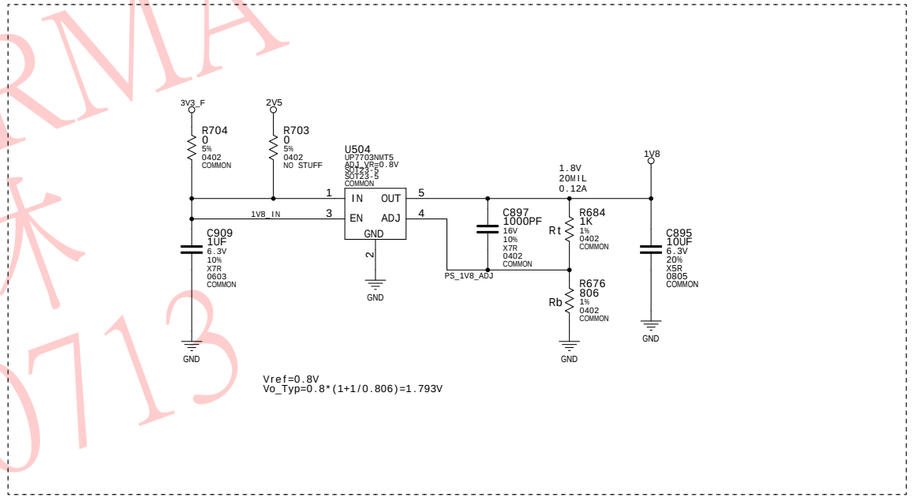
Page20: Power Supply: 2V5 and 1V8





ASSEMBLY	
PAGE DETAIL	Power Supply: 2V5 and 1V8

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Page21: Combined FBVDD and 1V2

Input ripple Irms 5.3@14A from PEX12V

Option for feed 12V directly

Place near drain of top FET

Place near Low Side Mosfet

FBVDD = 2.05V @ 14

Stuff with 0ohm for using OP driver

Vout = Vref * (1 + Rt/Rb)
1.172V = 0.8V * (1 + 1.74K/3.74K)

FREQ_SET = 110K for 300kHz
68.0K for 400kHz

Compensation for FBVDD

Remote sense

FBVDD = VREF * (1 + Rtop/Rbot)
FBVDD = 0.8V * (1 + 1.27K/1K) = 1.8V
FBVDD = 0.8V * (1 + 1.37K/1K) = 1.9V
FBVDD = 0.8V * (1 + 1.50K/1K) = 2.0V
FBVDD = 0.8V * (1 + 1.62K/1.05K) = 2.034V

NVVDD->FBVDDQ Sequencing

ASSEMBLY	
PAGE DETAIL	Power Supply: FBVDD/Q, PEXVDD

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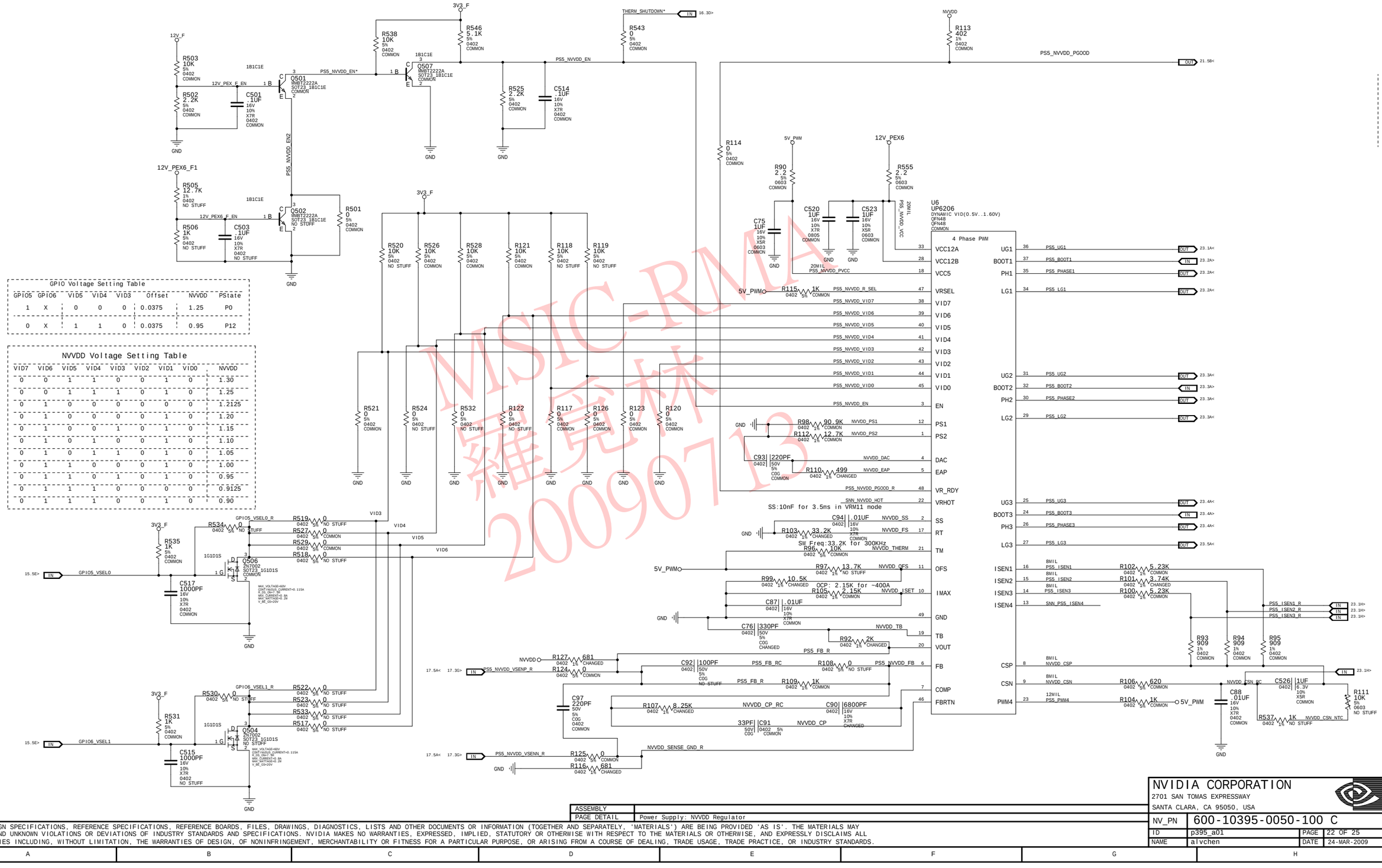
Page22: Power Supply: NVVDD Regulator



GPIO Voltage Setting Table

GPIO5	GPIO6	VID5	VID4	VID3	Offset	NVVDD	PState
1	X	0	0	0	0.0375	1.25	P0
0	X	1	1	0	0.0375	0.95	P12

NVVDD Voltage Setting Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	NVVDD
0	0	1	1	0	0	1	0	1.30
0	0	1	1	1	0	1	0	1.25
0	1	0	0	0	0	0	0	1.2125
0	1	0	0	0	0	1	0	1.20
0	1	0	0	1	0	1	0	1.15
0	1	0	1	0	0	1	0	1.10
0	1	0	1	1	0	1	0	1.05
0	1	1	0	0	0	1	0	1.00
0	1	1	0	1	0	1	0	0.95
0	1	1	1	0	0	0	0	0.9125
0	1	1	1	0	0	1	0	0.90

ASSEMBLY	
PAGE DETAIL	Power Supply: NVVDD Regulator

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Page23: Power Supply: NVVDD Mosfet

PS5_ISEN1_R — BUII — OUT — 22.4Hc
PS5_ISEN2_R — BUII — OUT — 22.4Hc
PS5_ISEN3_R — BUII — OUT — 22.4Hc
NVVDD_CSN_RC — BUII — OUT — 22.5Hc

Input ripple Irms ~11@80A from EXT_PEX12V(Phase1 and Phase3)

Total output current 80A

Input ripple Irms ~8A@80A from PEX12V

Share the Input Cap with FBVDDQ

ASSEMBLY	
PAGE DETAIL	Power Supply: NVVDD Mosfet

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Page24: Blank

ASSEMBLY	
PAGE DETAIL	Blank

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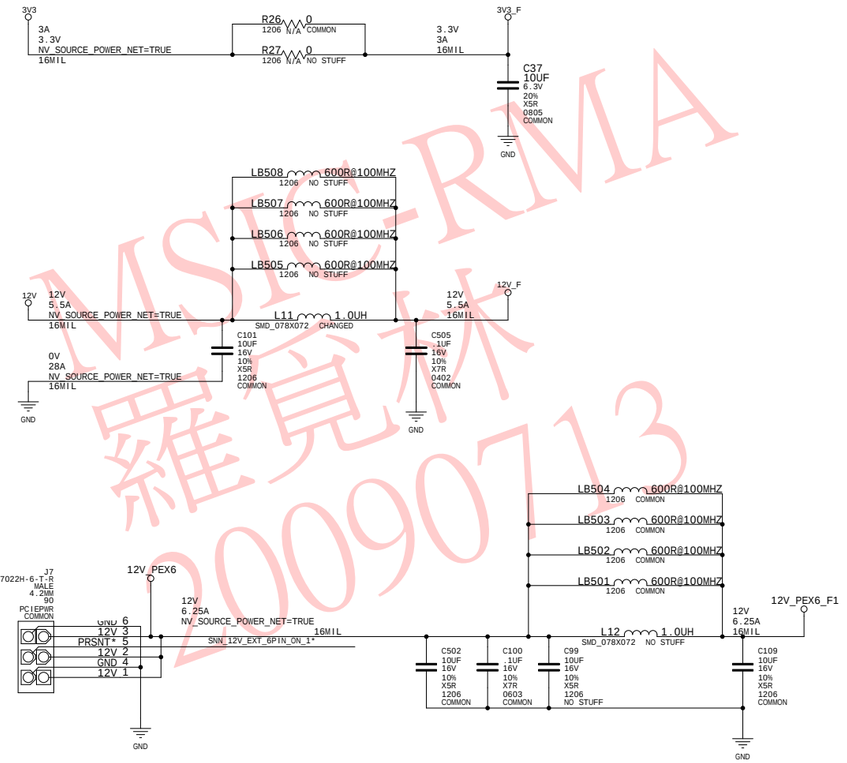
Page25: Power Supply: Filter/Detection of 3V3,12V,12V_PEX

POWER FILTER 3.3V

POWER FILTER 12V



ASSEMBLY	
PAGE DETAIL	Power Supply: Filter/Detection of 3V3, 12V, 12V_PEX6

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