TU104-400A GPU

NPN-09105-001_v01 | July 2018

New Product Notice

New Product Notice

NPN-09105-001_v01

New Product Introduction

This NPN specifies the following new NVIDIA® TU104-400A GPU. This GPU is offered in the GB4B-256 (2228-ball BGA, 37.5 mm × 37.5 mm) package only.

Notification	July 2018	**Planned Implementation**	Now

Product Information

These new products represent the high-end of the Enthusiast consumer desktop GPU segment. They are based on the new NVIDIA Turing graphics architecture and will be manufactured using qualified suppliers per our approved suppliers' list and are RoHS and Halogen-free compliant.

Key Specifications:

	TU104-400A
Chip	TU104-400A-A1
Device ID	0x1E87
Memory interface	256-bit GDDR6
Package	GB4B-256

Impact of Change and Recommended Action

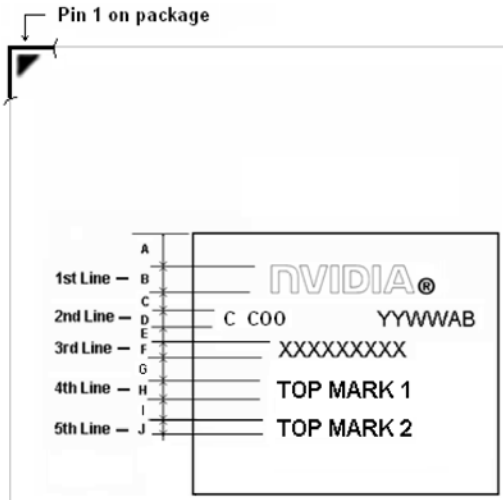
NVIDIA is committed to providing our customers with quality products that push the edge of technology and at the same time enable product segmentation. To help guarantee a rapid time-to-market launch and smooth and uninterrupted product supply, NVIDIA strongly recommends that customers qualify these GPUs as soon as possible.

Forecasted Key Milestones

TU104-400A-A1: QS ..... July 30, 2018
TU104-400A-A1: Production ..... August 17, 2018

Product Marking and Traceability

TU104-400A Markings



Pin 1: Location of Pin 1 in upper left when reading the marking.

Line 1: Company Name

Line 2: Assembly information: plant identifier (C) and country of origin (COO):
- C = Plant identifier: A (ASE), B (Amkor K5), K (Amkor K4), R (ATT - Amkor Tech), S (SPIL), T (TSMC).
- COO = Country of origin: Taiwan for ASE, ATT, SPIL and TSMC, and Korea for Amkor K4 and Amkor K5.
- YYWW = Assembly date code
- AB = Mask revision

Line 3: Assembly lot number (XXXXXXXXX).
The first character identifies the wafer Fab location:
- P = TSMC Fab 14

Line 4: Product Part Number, for example:
XXXXX-XX-XX

Line 5: <BLANK>

Products Affected/Ordering Codes

Product	NVIDIA Part Number [1]	Marketing Part Number for P.O.	Comments
TU104-400A	TU104-400A-A1	TU104-400A-A1	37.5 mm × 37.5 mm 2228-ball BGA (GB4B-256)

Note:

[1] The NVIDIA part number is provided in this document as a reference for product shipping and handling at factory. This part number is NVIDIA confidential.

Revision History

Version	Date	Authors	Description of Change
01	July 24, 2018	QL, DR	Initial release

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TU104 Graphics Processing Units

DS-08840-001_v01 | July 2018
NVIDIA CONFIDENTIAL | Prepared and Provided Under NDA

Data Sheet

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DOCUMENT CHANGE HISTORY

DS-08840-001_v01

Version	Date	Authors	Description of Change
01	July 27, 2018	RT, DR	Initial Release

1 INTRODUCTION

Overview

The Graphics Processing Units (GPUs) covered in this data sheet are designed using a new architecture to bring a new level of performance to visual graphics and computing software applications. These GPUs fully integrate hardware acceleration for both graphics and computing code. This means that these GPUs can enable hardware acceleration of a wider class of software applications than ever before.

The NVIDIA® (TU104) GPUs are fabricated using TSMC 12FFB process technology to provide maximum performance. The TU104 GPUs supports GDDR6 memories.

Features and Technologies

The TU104 GPUs supports the following features and technologies:

- Direct3D 12 and Shader Model 7.0
- OpenGL 4.5
- Vulkan 1.0
- NVIDIA® PhysX™ (Ageia PhysX) technology
- NVIDIA® CUDA® technology

Memory Support

The TU104 GPU supports a 256 bits wide frame buffer memory interface using GDDR6 memories.

Display

Key display features include:

- Four display pipelines for quad independent display
- Pipeline pixel depth 12 bits per each color
- HDMI version: 2.0b
  - Full backwards compatibility with HDMI 1.x
- DisplayPort (DP) version: 1.4a
  - Max resolution 7680 x 4320 at 60Hz (DSC)
- DVI-D: Dual-link resolution of 2560 × 1600 × 24 bpp 60 Hz refresh rate
- USB-C

Digital Audio

Digital audio features include:

- Support for HD Audio over PCI Express
- Data rates of 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz, 176 KHz, and 192 KHz with HDMI. Only 48 KHz supported over DP.
- Word sizes of 16-bit, 20-bit, and 24-bit

Video

The TU104 GPU introduces a new video engine, which is backward compatible with the video engine in earlier GPUs. The following video formats are supported:

- Decode
  - H264 (MPEG4 AVC)
  - H265 (HEVC)
  - VP8/VP9
  - MVC
  - MV-HEVC
  - MPEG2
  - MPEG4 ASP
  - VC1
- Encode
  - H264 (MPEG4 AVC)
  - H265 (HEVC)
  - MVC
  - MV-HEVC

A full range of resolutions are supported including 2160p, 1080p, 1080i, 720p, 480p, and 480i. The TU104 GPUs provide hardware acceleration for the computationally intensive parts of video processing. The TU104 video processor provides improved video playback speeds via faster decode and transcode.

PCI Express 3.0

The TU104 GPU supports PCI Express 3.0 with 16 lanes of PCIe traffic for a peak bandwidth (counting both directions) of up to 16 gigabytes (GBps) per second.

NVLink

The TU104 GPU supports one x8 wide NVIDIA NVLink™2 interface, which can support up to 25.78 GBps/direction raw bandwidth.

GPIOs

The GPIO interface allows for basic control of devices on the graphics card.

Power Management Technologies

The TU104 GPU employs enhanced power management to achieve very low GPU power consumption. The following features are supported:

- ASLM and ASPM power management
- PLLs on lower voltage rails
- Dynamic memory termination
- Adaptive clocking
- Adaptive Power States

2 SIGNAL DESCRIPTIONS

The signal description section contains definitions grouped under the following functions:

- Conventions
- PCI Express Interface
- NVLink Interface
- Frame Buffer Memory Interface
- ROM Access Signals
- Digital Display Interface
- USB-C Display Interface
- I2C Interface
- Clock Reference Signals
- Power Rail Signals
- Test Signals
- Miscellaneous

Conventions

The following conventions are used to describe the signals for the TU104 GPUs:

- Signal names listed in the ballout are written in bold *sans serif* font to distinguish them from other text. Single-ended active low signals are identified by an underscore and the letter "n" (**_N**) after the signal. For example, **PEX_TX1_N** indicates an active low signal. Signal names that do not appear in the ballout, but that are used for alternate interfaces are written in *sans serif* font without bold.
- Vendor signals appear as are standard for the vendor data sheets. For instance, $\overline{\text{CAS}}$ represents the active low Column Address Strobe signal in the frame buffer memory interface.
- I/O Type
  The signal I/O state is represented as a code to indicate the operational characteristics of the signal. Table 2.1 lists the I/O codes used in the signal description tables.

Table 2.1 I/O Codes for Signal Descriptions

I/O Code	Meaning
I	Input signal
I/O	Input/output signal
O	Output signal
P, GND	Power/ground
B	Bidirectional signal
Z	Tri-state output
AB	Analog bidirectional signal
AO	AO = Analog output signal

PCI Express Interface

The PCI Express Interface signals are given in Table 2.2.

Table 2.2 PCI Express Interface

Signal	I/O	Description
PEX_RX[15:0] PEX_RX[15:0]_N	I	PCI Express Receive Data Bus This is the high-speed unidirectional differential input data bus. The raw data rate is 2.5 Gbps per differential pair for PCI Express 1.1, 5.0 Gbps for PCI Express 2.0, 8.0 Gbps for PCI Express 3.0, including the symbol overhead for an embedded clock.

Table 2.2 PCI Express Interface

Signal	I/O	Description
PEX_TX[15:0] PEX_TX[15:0]_N	O	PCI Express Transmit Data Bus This is the high-speed unidirectional differential output data bus. The raw data rate is 2.5 Gbps per differential pair for PCI Express 1.1, 5.0 Gbps for PCI Express 2.0, 8.0 Gbps for PCI Express 3.0, including the symbol overhead for an embedded clock.
PEX_REFCLK PEX_REFCLK_N	I	PCI Express Reference Clock The reference clock is a differential low-jitter input the GPU uses for its internal timing purposes. This input clock may be spread spectrum. Refer to the latest PCI Express specification for details on the reference clock spread spectrum.
PEX_RST_N	I	PCI Express Reset The PEX_RST_N signal indicates when the power supply is within its specified voltage tolerance and is stable. It goes inactive after a delay time from the power rails, achieving specified tolerance and power up. Refer to the latest PCI Express specification for details on the PCI Express reset.
PEX_TERMP	AB	PCI Express Input/Output Termination Calibration The PEX_TERMP signal provides the reference for the internal calibation of the PCI Express input/output termination. Use a pull-down to GND that is the same value as the desired termination.
PEX_CLKREQ_N	O	PCI Express Clock Request This active low signal is driven to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data.
PEX_WAKE_N	I/O	PCI Express Wake Request This active low signal is driven to request that the PCI Express interfaces wakes up from a lower power state.

NVLink Interface

The NVLink Interface signals are given in Table 2.3.

Table 2.3 NVLink Interfaces

Signal	I/O	Description
NVHSx_RX[7:0] NVHSx_RX[7:0]_N (x=0)	I	NVLink Receive Data Bus This is the high-speed unidirectional differential input data bus. The raw data rate is 2.5 Gbps per differential pair.
NVHSx_TX[7:0] NVHSx_TX[7:0]_N (x=0)	O	NVLink Receive Data Bus This is the high-speed unidirectional differential input data bus. The raw data rate is 2.5 Gbps per differential pair.
NVHS_REFCLK NVHS_REFCLK_N	I	NVLink Reference Clock The reference clock is a differential low-jitter input the GPU uses for its internal timing purposes. Refer to the latest NVIDIA NVLink specification for details.
NVHSx_TERMP (x=0)	I/O	NVLink Input/Output Termination Calibration The **NVHSx_TERMP** signal provides the reference for the internal calibration of the NVLink input/output termination. Refer to the NVIDIA Hardware Design Guide for the recommended resistor value.

Frame Buffer Memory Interface

The TU104 frame buffer memory interface supports GDDR6 memories. Each memory partition has its own set of command signals. To see how the frame buffer control signals map to the memory command signals, refer to the Hardware Design Guide.

Table 2.4 and Table 2.5 describes the data and clock signals for each memory partition.

Table 2.4 Frame Buffer Command Interface for GDDR6

Signal	I/O	Description
FBx_CMD[35:0] (x = A,B,C,D)	O	Command Address Bus Inversion (CABI_n) Used to reduce power consumption on the command Address bus.
	O	Reset (RESET_n) Asynchronous DRAM reset signal
	O	Memory Clock Enable (CKE_n) Enables the clock receivers for the target RAM.
	O	Command Address Inputs (CA[9:0]) The CA inputs receive DDR Command and Address inputs

Table 2.5 Frame Buffer Interface

Signal	I/O	Description
FBx_CLK[1:0] FBx_CLK[1:0]_N (x=A,B,C,D)	O	Memory Clock Signals These are separate sets of clock signals for each memory partition. For a further reduction in loading, there are two sets of clocks per partition. Each partition has two clock pairs that control either the most significant 32 bits or the least significant 32 bits per partition. The active low CA signals switch on the falling clock edge. The active high CA signals switch on the rising clock edge. The memory clock signals are as follows: **FBx_CLK0** and **FBx_CLK0_N** → **FBx_D[31:0]** **FBx_CLK1** and **FBx_CLK1_N** → **FBx_D[63:32]** **x= A,B,C,D**
FBx_D[63:0] (x=A,B,C,D)	I/O	Memory Data Bus These signals connect to data signals of the memory device for each 64-bit partition.

Table 2.5 Frame Buffer Interface

Signal	I/O	Description
FBx_DQM[7:0] (x=A,B,C,D)	I/O	Data Bus Inversion (DBI) **FBx_DQM[7:0]** signals are connected to DBI[7:0] signals of the memory. Used to reduce power consumption and VDD noise of the DRAM.
FBx_DQS_WP[7:0] (x=A,B,C,D)	I	Error Detection Code (EDC) **FBx_DQS_WP[7:0]** signals are connected to the EDC[7:0] signals of the memory. The CRC data is communicated on these signals
FBx_WCK01 FBx_WCK01_N FBx_WCK23 FBx_WCK23_N FBx_WCK45 FBx_WCK45_N FBx_WCK67 FBx_WCK67_N (x=A,B,C,D)	O	Reference for read and write data.
FBx_WCKB01 FBx_WCKB01_N FBx_WCKB23 FBx_WCKB23_N FBx_WCKB45 FBx_WCKB45_N FBx_WCKB67 FBx_WCKB67_N (x=A,B,C,D)	O	Reference for read and write data.
FB_CAL_PD_VDDQ FB_CAL_PU_GND	AO	Calibration Pull-Down/Pull-Up When the frame buffer bus operates in high-speed source-synchronous mode, several signals require dynamic calibration. Other slower signals are calibrated once on power-up. **FB_CAL_PD_VDDQ** and **FB_CAL_PU_ GND** are used to compute the drive strength of the frame buffer pads. **FB_CAL_PD_VDDQ** connects to **FBVDDQ** and is pulled up through a precision resistor. **FB_CAL_PU_GND** is pulled down to **GND** through a precision resistor.

Table 2.5 Frame Buffer Interface

Signal	I/O	Description
FB_CAL_TERM_GND	AO	Termination Calibration Signal When the frame buffer bus operates in high-speed source-synchronous mode, it may use internal termination provided by the GPU. This signal provides the calibration for the internal termination. It should be tied to **GND** through a precision resistor that is the same value as the desired termination.
FB_VREF	I	Frame Buffer Voltage Reference Sets switching threshold for inputs on the frame buffer when the frame buffer input pads are set to input mode.
FBVDDQ_SENSE	AO	Frame Buffer Power Rail Sense Signal

ROM Access Signals

Table 2.6 Serial ROM Access Signals

Signal	I/O	Description
ROM_SCLK	O	Serial ROM Clock **ROM_SCLK** supplies the clock signal for accessing serial ROM data.
ROM_CS_N	O	Chip Select.
ROM_SI	O	Serial Output **ROM_SI** supplies the data signal to the **SROM_SI** serial ROM signal.
ROM_SO	I	Serial Input **ROM_SO** accepts the data signal input from **SROM_SO** of the serial ROM as input.

Digital Display Interface

The TU104 GPUs enables Links A, B, C, D, E, and F to support DisplayPort. Links can also be configured to support DVI and HDMI.

Table 2.7 Digital Display Interface Signals, Links A & B

Signal	I/O	Description
IFPA_AUX_SCL/ IFPA_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link A)
IFPA_L0/IFPA_L0_N	O	DisplayPort Main Link Lane 0 (Link A)
IFPA_L1/IFPA_L1_N	O	DisplayPort Main Link Lane 1 (Link A)
IFPA_L2/IFPA_L2_N	O	DisplayPort Main Link Lane 2 (Link A)
IFPA_L3/IFPA_L3_N	O	DisplayPort Main Link Lane 3 (Link A)
IFPB_AUX_SCL IFPB_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link B)
IFPB_L0/IFPB_L0_N	O	DisplayPort Main Link Lane 0 (Link B)
IFPB_L1/IFPB_L1_N	O	DisplayPort Main Link Lane 1 (Link B)
IFPB_L2/IFPB_L2_N	O	DisplayPort Main Link Lane 2 (Link B)
IFPB_L3/IFPB_L3_N	O	DisplayPort Main Link Lane 3 (Link B)
IFPAB_RSET	I/O	Set Reference Current Generate a reference current through connecting an external resistor to this signal.

Table 2.8 Digital Display Interface Signals, Links C, D, E, and F

Signal	I/O	Description
IFPC_AUX_SCL / IFPC_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link C)
IFPC_L0/IFPC_L0_N	O	DisplayPort Main Link Lane 0 (Link C)
IFPC_L1/IFPC_L1_N	O	DisplayPort Main Link Lane 1 (Link C)
IFPC_L2/IFPC_L2_N	O	DisplayPort Main Link Lane 2 (Link C)
IFPC_L3/IFPC_L3_N	O	DisplayPort Main Link Lane 3 (Link C)
IFPCD_RSET	I/O	Set Reference Current Generates a reference current through connecting an external resistor to this signal

Table 2.8 Digital Display Interface Signals, Links C, D, E, and F

Signal	I/O	Description
IFPD_AUX_SCL/ IFPD_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link D)
IFPD_L0/IFPD_L0_N	O	DisplayPort Main Link Lane 0 (Link D)
IFPD_L1/IFPD_L1_N	O	DisplayPort Main Link Lane 1 (Link D)
IFPD_L2/IFPD_L2_N	O	DisplayPort Main Link Lane 2 (Link D)
IFPD_L3/IFPD_L3_N	O	DisplayPort Main Link Lane 3 (Link D)
IFPE_AUX_SCL/ IFPE_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link E)
IFPE_L0/IFPE_L0_N	O	DisplayPort Main Link Lane 0 (Link E)
IFPE_L1/IFPE_L1_N	O	DisplayPort Main Link Lane 1 (Link E)
IFPE_L2/IFPE_L2_N	O	DisplayPort Main Link Lane 2 (Link E)
IFPE_L3/IFPE_L3_N	O	DisplayPort Main Link Lane 3 (Link E)
IFPE_RSET	I/O	Set Reference Current Generates a reference current through connecting an external resistor to this signal
IFPF_AUX_SCL/ IFPF_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane (Link F)
IFPF_L0/IFPF_L0_N	O	DisplayPort Main Link Lane 0 (Link F);
IFPF_L1/IFPF_L1_N	O	DisplayPort Main Link Lane 1 (Link F)
IFPF_L2/IFPF_L2_N	O	DisplayPort Main Link Lane 2 (Link F)
IFPF_L3/IFPF_L3_N	O	DisplayPort Main Link Lane 3 (Link F)

USB-C Display Interface

Link F and IFPB_AUX support USB-C, as described in Table 2.9.

Table 2.9 USB Interface Signals

Signal	I/O	Description
IFPF_AUX_SCL/ IFPF_AUX_SDA_N	I/O	DisplayPort Auxiliary Lane/USB-C Sideband signals SBU1/SBU2
IFPB_AUX_SCL/ IFPB_AUX_SDA_N	I/O	Master I2C to USB-C PPC
IFPF_L0/IFPF_L0_N	O	USB3 RX+ / USB3 RX- **Note:** This signal pad is used as USB3 RX+/ USB3 RX- for USB-C interface
IFPF_L1/IFPF_L1_N	O	USB3 TX+ / USB3 TX- **Note:** This signal pad is used as USB3 TX+/ USB3 TX- for USB-C interface

Table 2.9 USB Interface Signals

Signal	I/O	Description
IFPF_L2/IFPF_L2_N	O	USB3 TX+ / USB3 TX- **Note:** This signal pad is used as USB3 TX+/ USB3 TX- for USB-C interface
IFPF_L3/IFPF_L3_N	O	USB3 RX+ / USB3 RX- **Note:** This signal pad is used as USB3 RX+/ USB3 RX- for USB-C interface
USB_L0/USB_LO_N	O	USB3 TX+ or USB2+/USB3 TX- or USB2- **Note:** This signal pad is used as USB3 TX+/USB3 TX- for USB-C interface
USB_L1/USB_L1_N	O	USB3 RX+ or USB2+/USB3 RX- or USB2 **Note:** This signal pad is used as USB3 RX+/ USB3 RX- for USB-C interface
USB_RBIAS	AI	USB Reference Resistor
USB_SCL	I/O	Slave I2C Clock interface for controlling integrated DP/USB cross-connect
USB_SDA	I/O	Slave I2C Data interface for controlling integrated DP/USB cross-connect
USB_TERMP0	AI	USB PLL Reference Resistor 0
USB_TERMP1	AI	USB PLL Reference Resistor 1

I2C Interface

Table 2.10 I2C Interface Signals

Signal	I/O	Description
I2CB_SCL I2CB_SDA	I/O	If not used for any external Bus, this bus may be used for embedded devices.
I2CC_SCL I2CC_SDA	I/O	Restricted to embedded devices such as voltage regulators and power monitors.
I2CS_SCL I2CS_SDA	I/O	Slave I2C-Compatible Bus Signal.

Clock Reference Signals

Table 2.11 Clock Reference Signals

Signal	I/O	Description
XTAL_IN XTAL_OUT	I O	A series resonant crystal is connected between these two points to provide the reference clock for the internal clock synthesizers. Alternately, an external LVTTL clock oscillator output may be driven in XTAL_IN, leaving XTAL_OUT unconnected.
XTAL_OUTBUFF	O	**XTAL_OUTBUFF** is a buffered version of the **XTAL_IN**/ **XTAL_OUT**. Used as a startup strap to set the fan PWM.

Power Rail Signals

IFP Power Rail Signals

Table 2.12 IFP Power Rail Signals

Signal	I/O	Description
IFP_IOVDD	P	1.0V supply for integrated Digital Display I/O Power Rails for all IFP links.
IFPAB_PLLVDD	P	1.8V supply for integrated Digital Display PLL Power Rails for the IFP-A and IFP-B links.
IFPCD_PLLVDD	P	1.8V supply for Integrated Digital Display PLL Power Rails for the IFP-C and IFP-D links.
IFPE_PLLVDD	P	1.8V supply for Integrated Digital Display PLL Power Rails for the IFP-E link.

PEX Power Rail Signals

Table 2.13 PEX Power Rail Signals

Signal	I/O	Description
PEX_CVDD / PEX_DVDD	P	1.0V supply for PCIe interface/PLL digital power rail
PEX_HVDD	P	1.8V supply for PCIe interface/PLL analog power rail
PEX_PLL_HVDD	P	1.8V supply for the PEX PLL

Frame Buffer Power Rail Signals

Table 2.14 FrameBuffer Power Rail Signals

Signal	I/O	Description
FB_REFPLL_AVDDx (x=0,1)	P	1.8V supply for Frame Buffer Digital Power Rails
FBVDDQ	P	Frame Buffer Power Rail
FBVDDQ_SENSE	O	Frame Buffer Power Rail Sense Signal
FBx_PLL_AVDD (x=A,B,C,D)	P	1.8V supply for Frame Buffer PLL Analog Power Rails

NVLink Rail Signals

Table 2.15 General Power Rail Signals

Signal	I/O	Description
NVHS_CVDD / NVHS_DVDD	P	NVLink Internal Core Power Rail
NVHS_HVDD	P	NVLink High Voltage Power Rail
NVHSx_PLL_HVDD (x=0)	P	NVLink PLL Power Rail

General Power Rail Signals

Table 2.16 General Power Rail Signals

Signal	I/O	Description
GPCPLL_AVDDx (x=0,1)	P	1.8V supply for Analog Power Rails for GPCs
SP_PLLVDD	P	1.8V supply for Core Clock PLL Analog Power Rail
VDD	P	Core Power Rail. Connect to NVVDD power supply.
1V8_AON	P	1.8V Always On Power Rail
VID_PLLVDD	P	1.8V supply for Video Pixel Clock PLL Analog power rail
XS_PLLVDD	P	1.8V supply for Core PLL Analog rail

USB Power Rail Signals

Table 2.17 USB Power Rail Signals

Signal	I/O	Description
USB_DVDD	P	USB 1.0V Core Power Rail
USB_HVDD	P	USB 1.8V Voltage Power Rail
USB_PLL_HVDD	P	USB 1.8V PLL Power Rail
USB_VDDP	P	USB 3.3V Analog Supply

Note: Refer to the Hardware Design Guide for detailed functionality and usage.

Test Signals

Table 2.18 Test Signals

Signals	I/O	Description
JTAG_TCK JTAG_TDI JTAG_TDO JTAG_TMS	I I Z I	JTAG Test Signals
NVJTAG_SEL	I	JTAG Select

Miscellaneous

Table 2.19 Miscellaneous Signals

Signal	I/O	Description
STRAP[5:0]	I	Strap Signals
THERMDP THERMDN	I O	Thermal Monitor Signals Leave floating and unconnected.
ADC_IN / ADC_IN_N	I	External current sense for power monitoring
GPIO [30:0]	I	General Purpose I/O
BUFRST_N	O	Behaves as a buffered copy of the system PEX_RST* signal in all operating modes **when 1V8 is present**. Tri-state when **1V8 is not present**.
FP_FUSE_SRC	I	TBD

3 ELECTRICAL SPECIFICATIONS

This section provides absolute maximum ratings and operating conditions for the TU104 GPUs.

For more information about the core graphics voltage (NVVDD), frame buffer clock frequency (MCLK), and core clock frequency (GPCCLK) values and electrical and thermal design guidelines for these products, refer to the SKU specific Electrical and Thermal Design Guidelines.

The frame buffer memory clock, MCLK, is defined as an actual clock output (not as a data rate). The NVIDIA® GPU Boost™ technology manages the clocks dynamically.

Table 3.1 lists the absolute maximum ratings of the power rails.

Table 3.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.[1]	Units	Notes
FBVDDQ	Frame buffer power rail	-0.3	1.98	V	
FBx_PLL_AVDD (x=A,B,C,D)	Frame buffer PLL analog power rail	-0.3	1.854	V	
GPCPLL_AVDD0 GPCPLL_AVDD1	Core PLL Analog Rails	-0.3	1.854	V	
IFP_IOVDD	Integrated Digital Display I/O power rails	-0.3	1.1	V	
IFPAB_PLLVDD	Integrated Digital Display PLL power rails	-0.3	1.854	V	

Table 3.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.[1]	Units	Notes
IFPCD_PLLVDD	Integrated Digital Display PLL power rails	-0.3	1.854	V	
IFPE_PLLVDD	Integrated Digital Display PLL power rails	-0.3	1.854	V	
PEX_DVDD	PCIe interface/PLL digital power rail	-0.3	1.1	V	
PEX_HVDD	PCIe interface/PLL analog power rail	-0.3	1.854	V	
PEX_PLL_HVDD	PCIe interface PLL supply power rail	-0.3	1.854	V	
SP_PLLVDD	Core clock PLL analog power rail	-0.3	1.854	V	
VDD	Core (NVVDD) power rail	-0.3	TBD	V	
VDD_SENSE	VDD Power Plane Sense signal				
1V8_AON	1.8 V power rail	-0.3	1.854	V	
VID_PLLVDD	Thermal controller and Video pixel clock PLL analog power rail	-0.3	1.854	V	
XS_PLLVDD	Core PLL Analog Rails	-0.3	1.854	V	
T_j	Die junction temperature	Refer to the Product Specification		°C	

Notes:

1. Stress greater than those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note: Voltage settings may vary with the reference design; please refer to the specific reference design to get the required values.

Table 3.2 lists the operating conditions of the clock and power rail signals.

Table 3.2 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.[1]	Units	Notes
FBVDDQ	Frame buffer power rail		1.25	1.35	V	Note 2
FBx_PLL_AVDD (x=A,B,C,D)	Frame buffer PLL analog power rail	1.746	1.800	1.854	V	
GPCPLL_AVDD0 GPCPLL_AVDD1	Core PLL Analog Rails	1.746	1.800	1.854	V	
IFP_IOVDD	Integrated Digital Display I/O power rails	0.97	1.00	1.03	V	
IFPAB_PLLVDD	Integrated Digital Display PLL power rails	1.746	1.800	1.854	V	
IFPCD_PLLVDD	Integrated Digital Display PLL power rails	1.746	1.800	1.854	V	
IFPE_PLLVDD	Integrated Digital Display PLL power rails	1.746	1.800	1.854	V	
PEX_DVDD/ PEX_CVDD	PCIe interface/PLL digital power rail	0.97	1.00	1.03	V	
PEX_HVDD	PCIe interface/PLL analog power rail	1.746	1.800	1.854	V	
PEX_PLL_HVDD	PCIe interface PLL supply power rail	1.746	1.800	1.854	V	
SP_PLLVDD	Core clock PLL analog power rail	1.746	1.800	1.854	V	
VDD or NVVDD	Core power rail	NVVDD-2.5%	NVVDD	NVVDD+2.5%	V	
VDD_SENSE	VDD Power Plane Sense signal				V	
1V8_AON	1.8 V power rail	-0.3		1.854	V	
VID_PLLVDD	Thermal controller and Video pixel clock PLL analog power rail	1.746	1.800	1.854	V	
XS_PLLVDD	Core PLL Analog Rails	1.746	1.800	1.854	V	
T_j	Die junction temperature	0	Refer to the product specific Thermal Design Guide	Refer to the product specific Thermal Design Guide	°C	See Note 3.

Notes:

1 This specification defines the goals for the DC supply at **VDD**. Short pulses due to switching noise on **VDD** may exceed this limit.
2 Min/Typ/Max/ should meet memory vendor spec which can vary from 1.35V to 1.55V.

3 T_j is the maximum die temperature at which the GPU can operate at its maximum clock frequencies, as defined in the NVIDIA Product Specification.

Table 3.3 GPIO Electrical Specifications

Voh,Vih/min	Voh,Vih/max	Vol,Vil/min	Vol,Vil/max	Vi_mid max	Vi_mid min
1.50V	1.854V	0V	0.3V	1.3V	0.5V

4 MASTER SIGNAL LIST

This chapter contains the master signal list for the TU104 GPUs.

Table 4.1 Master Signal List

Master Signal List for TU104 GPUs					
IOB Key: B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z= Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		Reset & Initial Value Key: Z= Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	**IOB**	**Reset Value**	**Initial Value**	**Drive**	**Notes**
I2C					
I2CB_SCL	O			+1.8V_AON	
I2CB_SDA	B			+1.8V_AON	
I2CC_SCL	O			+1.8V_AON	
I2CC_SDA	B			+1.8V_AON	
I2CS_SCL	O			+1.8V_AON	
I2CS_SDA	B			+1.8V_AON	
IFP					
IFPA_L0_N	O				
IFPA_L0	O				
IFPA_L1_N	O				
IFPA_L1	O				
IFPA_L2_N	O				
IFPA_L2	O				
IFPA_L3_N	O				
IFPA_L3	O				
IFPB_L0_N	O				

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Signal Name	**IOB**	**Reset Value**	**Initial Value**	**Drive**	**Notes**
IFPB_L0	O				
IFPB_L1_N	O				
IFPB_L1	O				
IFPB_L2_N	O				
IFPB_L2	O				
IFPB_L3_N	O				
IFPB_L3	O				
IFPAB_RSET	AI				
IFPC_L0_N	O				
IFPC_L0	O				
IFPC_L1_N	O				
IFPC_L1	O				
IFPC_L2_N	O				
IFPC_L2	O				
IFPC_L3_N	O				
IFPC_L3	O				
IFPD_L0_N	O				
IFPD_L0	O				
IFPD_L1_N	O				
IFPD_L1	O				
IFPD_L2_N	O				
IFPD_L2	O				
IFPD_L3_N	O				
IFPD_L3	O				
IFPCD_RSET	AI				
IFPE_L0_N	O				
IFPE_L0	O				
IFPE_L1_N	O				
IFPE_L1	O				
IFPE_L2_N	O				
IFPE_L2	O				
IFPE_L3_N	O				
IFPE_L3	O				
IFPF_L0_N	O				
IFPF_L0	O				
IFPF_L1_N	O				
IFPF_L1	O				
IFPF_L2_N	O				
IFPF_L2	O				

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Signal Name	**IOB**	**Reset Value**	**Initial Value**	**Drive**	**Notes**
IFPF_L3_N	O				
IFPF_L3	O				
IFPE_RSET	AI				
IFPA_AUX_SCL	O				
IFPA_AUX_SDA_N	B				
IFPB_AUX_SCL	O				
IFPB_AUX_SDA_N	B				
IFPC_AUX_SCL	O				
IFPC_AUX_SDA_N	B				
IFPD_AUX_SCL	O				
IFPD_AUX_SDA_N	B				
IFPE_AUX_SCL	O				
IFPE_AUX_SDA_N	B				
IFPF_AUX_SCL	O				
IFPF_AUX_SDA_N	B				
IFPAB_PLLVDD	P				
IFP_IOVDD	P				
IFPCD_PLLVDD	P				
IFPE_PLLVDD	P				
IFPE_PLLVDD	P				
Frame Buffer A					
FBA_D[63:0]	B			FBVDDQ	
FBA_DQM[7:0]	B			FBVDDQ	
FBA_DQS_WP[7:0]	I			FBVDDQ	
FBA_WCK01	O			FBVDDQ	
FBA_WCK01_N	O			FBVDDQ	
FBA_WCKB01	O			FBVDDQ	
FBA_WCKB01_N	O			FBVDDQ	
FBA_WCK23	O			FBVDDQ	
FBA_WCK23_N	O			FBVDDQ	
FBA_WCKB23	O			FBVDDQ	
FBA_WCKB23_N	O			FBVDDQ	
FBA_WCK45	O			FBVDDQ	
FBA_WCK45_N	O			FBVDDQ	
FBA_WCKB45	O			FBVDDQ	
FBA_WCKB45_N	O			FBVDDQ	
FBA_WCK67	O			FBVDDQ	
FBA_WCK67_N	O			FBVDDQ	
FBA_WCKB67	O			FBVDDQ	

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Signal Name	**IOB**	**Reset Value**	**Initial Value**	**Drive**	**Notes**
FBA_WCKB67_N	O			FBVDDQ	
FBA_CMD[35:0]	O			FBVDDQ	
FBA_CLK0	O			FBVDDQ	
FBA_CLK0_N	O			FBVDDQ	
FBA_CLK1	O			FBVDDQ	
FBA_CLK1_N	O			FBVDDQ	
Frame Buffer B					
FBB_D[63:0]	B			FBVDDQ	
FBB_DQM[7:0]	B			FBVDDQ	
FBB_DQS_WP[7:0]	I			FBVDDQ	
FBB_WCK01	O			FBVDDQ	
FBB_WCK01_N	O			FBVDDQ	
FBB_WCKB01	O			FBVDDQ	
FBB_WCKB01_N	O			FBVDDQ	
FBB_WCK23	O			FBVDDQ	
FBB_WCK23_N	O			FBVDDQ	
FBB_WCKB23	O			FBVDDQ	
FBB_WCKB23_N	O			FBVDDQ	
FBB_WCK45	O			FBVDDQ	
FBB_WCK45_N	O			FBVDDQ	
FBB_WCKB45	O			FBVDDQ	
FBB_WCKB45_N	O			FBVDDQ	
FBB_WCK67	O			FBVDDQ	
FBB_WCK67_N	O			FBVDDQ	
FBB_WCKB67	O			FBVDDQ	
FBB_WCKB67_N	O			FBVDDQ	
FBB_CMD[35:0]	O			FBVDDQ	
FBB_CLK0	O			FBVDDQ	
FBB_CLK0_N	O			FBVDDQ	
FBB_CLK1	O			FBVDDQ	
FBB_CLK1_N	O			FBVDDQ	
Frame Buffer C					
FBC_D[63:0]	B			FBVDDQ	
FBC_DQM[7:0]	B			FBVDDQ	
FBC_DQS_WP[7:0]	I			FBVDDQ	
FBC_WCK01	O			FBVDDQ	
FBC_WCK01_N	O			FBVDDQ	
FBC_WCKB01	O			FBVDDQ	
FBC_WCKB01_N	O			FBVDDQ	

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Signal Name	**IOB**	**Reset Value**	**Initial Value**	**Drive**	**Notes**
FBC_WCK23	**O**			**FBVDDQ**	
FBC_WCK23_N	**O**			**FBVDDQ**	
FBC_WCKB23	**O**			**FBVDDQ**	
FBC_WCKB23_N	**O**			**FBVDDQ**	
FBC_WCK45	**O**			**FBVDDQ**	
FBC_WCK45_N	**O**			**FBVDDQ**	
FBC_WCKB45	**O**			**FBVDDQ**	
FBC_WCKB45_N	**O**			**FBVDDQ**	
FBC_WCK67	**O**			**FBVDDQ**	
FBC_WCK67_N	**O**			**FBVDDQ**	
FBC_WCKB67	**O**			**FBVDDQ**	
FBC_WCKB67_N	**O**			**FBVDDQ**	
FBC_CMD[35:0]	**O**			**FBVDDQ**	
FBC_CLK0	**O**			**FBVDDQ**	
FBC_CLK0_N	**O**			**FBVDDQ**	
FBC_CLK1	**O**			**FBVDDQ**	
FBC_CLK1_N	**O**			**FBVDDQ**	
Frame Buffer D					
FBD_D[63:0]	**B**			**FBVDDQ**	
FBD_DQM[7:0]	**B**			**FBVDDQ**	
FBD_DQS_WP[7:0]	**I**			**FBVDDQ**	
FBD_WCK01	**O**			**FBVDDQ**	
FBD_WCK01_N	**O**			**FBVDDQ**	
FBD_WCKB01	**O**			**FBVDDQ**	
FBD_WCKB01_N	**O**			**FBVDDQ**	
FBD_WCK23	**O**			**FBVDDQ**	
FBD_WCK23_N	**O**			**FBVDDQ**	
FBD_WCKB23	**O**			**FBVDDQ**	
FBD_WCKB23_N	**O**			**FBVDDQ**	
FBD_WCK45	**O**			**FBVDDQ**	
FBD_WCK45_N	**O**			**FBVDDQ**	
FBD_WCKB45	**O**			**FBVDDQ**	
FBD_WCKB45_N	**O**			**FBVDDQ**	
FBD_WCK67	**O**			**FBVDDQ**	
FBD_WCK67_N	**O**			**FBVDDQ**	
FBD_WCKB67	**O**			**FBVDDQ**	
FBD_WCKB67_N	**O**			**FBVDDQ**	
FBD_CMD[35:0]	**O**			**FBVDDQ**	
FBD_CLK0	**O**			**FBVDDQ**	

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Signal Name	**IOB**	**Reset Value**	**Initial Value**	**Drive**	**Notes**
FBD_CLK0_N	O			FBVDDQ	
FBD_CLK1	O			FBVDDQ	
FBD_CLK1_N	O			FBVDDQ	
Mem Miscellaneous Signals					
FB_CAL_VDDQ	AI			FBVDDQ	
FB_CAL_GND	AI			FBVDDQ	
FB_CAL_TERM	AI			FBVDDQ	
FBVDDQ	P				
FB_VREF	AI			FBVDDQ	
FBVDDQ_SENSE	P				
PCI Express					
PEX_RX[15:0]	I				
PEX_RX[15:0]_N	I				
PEX_TX[15:0]	O				
PEX_TX[15:0]_N	O				
PEX_TERMP	AI				
PEX_REFCLK	I				
PEX_REFCLK_N	I				
PEX_CLKREQ_N	O			+1.8V_AON	
PEX_RST_N	I			+1.8V_AON	
PEX_HVDD	P				
PEX_DVDD	P				
PEX_PLL_HVDD	P				
PEX_DVDD	P				
PEX_WAKE_N	O				
JTAG Interface					
JTAG_TMS	I			+1.8V_AON	
JTAG_TCK	I			+1.8V_AON	
JTAG_TRST_N	I			+1.8V_AON	
JTAG_TDI	I			+1.8V_AON	
JTAG_TDO	O			+1.8V_AON	
NVJTAG_SEL	I			+1.8V_AON	
Other Clocks					
ROM_CS_N	O			+1.8V_AON	
ROM_SCLK	B			+1.8V_AON	
ROM_SI	B			+1.8V_AON	
ROM_SO	B			+1.8V_AON	
XTAL_OUTBUFF	O			+1.8V_AON	
EXT_REFCLCK_FL	I			+1.8V_AON	

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Signal Name	**IOB**	**Reset Value**	**Initial Value**	**Drive**	**Notes**
XTAL_IN	AI			+1.8V_AON	
XTAL_OUT	AO			+1.8V_AON	
GPIO					
GPIO0	B			+1.8V_AON	
GPIO1	B			+1.8V_AON	
GPIO2	B			+1.8V_AON	
GPIO3	B			+1.8V_AON	
GPIO4	B			+1.8V_AON	
GPIO5	B			+1.8V_AON	
GPIO6	B			+1.8V_AON	
GPIO7	B			+1.8V_AON	
GPIO8	B			+1.8V_AON	
GPIO9	B			+1.8V_AON	
GPIO10	B			+1.8V_AON	
GPIO11	B			+1.8V_AON	
GPIO12	B			+1.8V_AON	
GPIO13	B			+1.8V_AON	
GPIO14	B			+1.8V_AON	
GPIO15	B			+1.8V_AON	
GPIO16	B			+1.8V_AON	
GPIO17	B			+1.8V_AON	
GPIO18	B			+1.8V_AON	
GPIO19	B			+1.8V_AON	
GPIO20	B			+1.8V_AON	
GPIO21	B			+1.8V_AON	
GPIO22	B			+1.8V_AON	
GPIO23	B			+1.8V_AON	
GPIO24	B			+1.8V_AON	
GPIO25	B			+1.8V_AON	
GPIO26	B			+1.8V_AON	
GPIO27	B			+1.8V_AON	
GPIO28	B			+1.8V_AON	
GPIO29	B			+1.8V_AON	
GPIO30	B			+1.8V_AON	
System Interfaces					
BUFRST_N	O			+1.8V_AON	
STRAP0	I			+1.8V_AON	
STRAP1	I			+1.8V_AON	
STRAP2	I			+1.8V_AON	

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Signal Name	**IOB**	**Reset Value**	**Initial Value**	**Drive**	**Notes**
STRAP3	I			+1.8V_AON	
STRAP4	I			+1.8V_AON	
STRAP5	I			+1.8V_AON	
OVERT	B			+1.8V_AON	
THERMDP	AO				
THERMDN	AO				
TS_VREF	AI				
GND_SENSE	P				
VDD_SENSE	P				
ADC_IN	AI				
ADC_IN_N	AI				
Power Direct Drills - IO voltage Rails & Core Voltages					
VDD	P				
GND	P				
1V8_AON	P			+1.8V_AON	
PLLs					
XS_PLLVDD	P				
FB_REFPLL_AVDD0	P				
FB_REFPLL_AVDD1	P				
VID_PLLVDD	P				
SP_PLLVDD	P				
XS_PLLVDD	P				
GPCPLL_AVDD0	P				
GPCPLL_AVDD1	P				
FBA_PLL_AVDD	P				
FBB_PLL_AVDD	P				
FBC_PLL_AVDD	P				
FBD_PLL_AVDD	P				
NVHS					
NVHS_CVDD	P				
NVHS_DVDD	P				
NVHS_HVDD	P				
NVHS_PLL_HVDD	P				
NVHS_REFCLK	I				
NVHS_REFCLK_N	I				
EXT_REFCLK_SLI	B				
NVHS_TERMP	AI				
NVHS0_RX0	I				
NVHS0_RX0_N	I				

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Signal Name	**IOB**	**Reset Value**	**Initial Value**	**Drive**	**Notes**
NVHS0_RX1	I				
NVHS0_RX1_N	I				
NVHS0_RX2	I				
NVHS0_RX2_N	I				
NVHS0_RX3	I				
NVHS0_RX3_N	I				
NVHS0_RX4	I				
NVHS0_RX4_N	I				
NVHS0_RX5	I				
NVHS0_RX5_N	I				
NVHS0_RX6	I				
NVHS0_RX6_N	I				
NVHS0_RX7	I				
NVHS0_RX7_N	I				
NVHS0_TX0	O				
NVHS0_TX0_N	O				
NVHS0_TX1	O				
NVHS0_TX1_N	O				
NVHS0_TX2	O				
NVHS0_TX2_N	O				
NVHS0_TX3	O				
NVHS0_TX3_N	O				
NVHS0_TX4	O				
NVHS0_TX4_N	O				
NVHS0_TX5	O				
NVHS0_TX5_N	O				
NVHS0_TX6	O				
NVHS0_TX6_N	O				
NVHS0_TX7	O				
NVHSO_TX7_N	O				
USB					
USB_DVDD	P				
USB_HVDD	P				
USB_L0	O				
USB_L0_N	O				
USB_L1	O				
USB_L1_N	O				
USB_PLL_HVDD	P				
USB_RBIAS	AI				

Table 4.1 Master Signal List

Master Signal List for TU104 GPUs					
IOB Key: B = Bidirectional signal I = Input signal O = Output signal P = Power-related signal Z= Tri-state output AB = Analog bidirectional signal AI = Analog input signal AO = Analog output signal		Reset & Initial Value Key: Z= Tri-state X = Indeterminate 0 = Drive 0 1 = Drive 1 C = Drive with toggle (clock) Note: Reset Value refers to the value while reset is being asserted to the GPU. Initial Value refers to the value after reset is released, but prior to any hardware or VBIOS execution.			
Signal Name	**IOB**	**Reset Value**	**Initial Value**	**Drive**	**Notes**
USB_SCL	O				
USB_SDA	B				
USB_TERMP0	AI				
USB_TERMP1	AI				
USB_VDDP	P				

5 PACKAGE DESCRIPTIONS

Mechanical Specifications

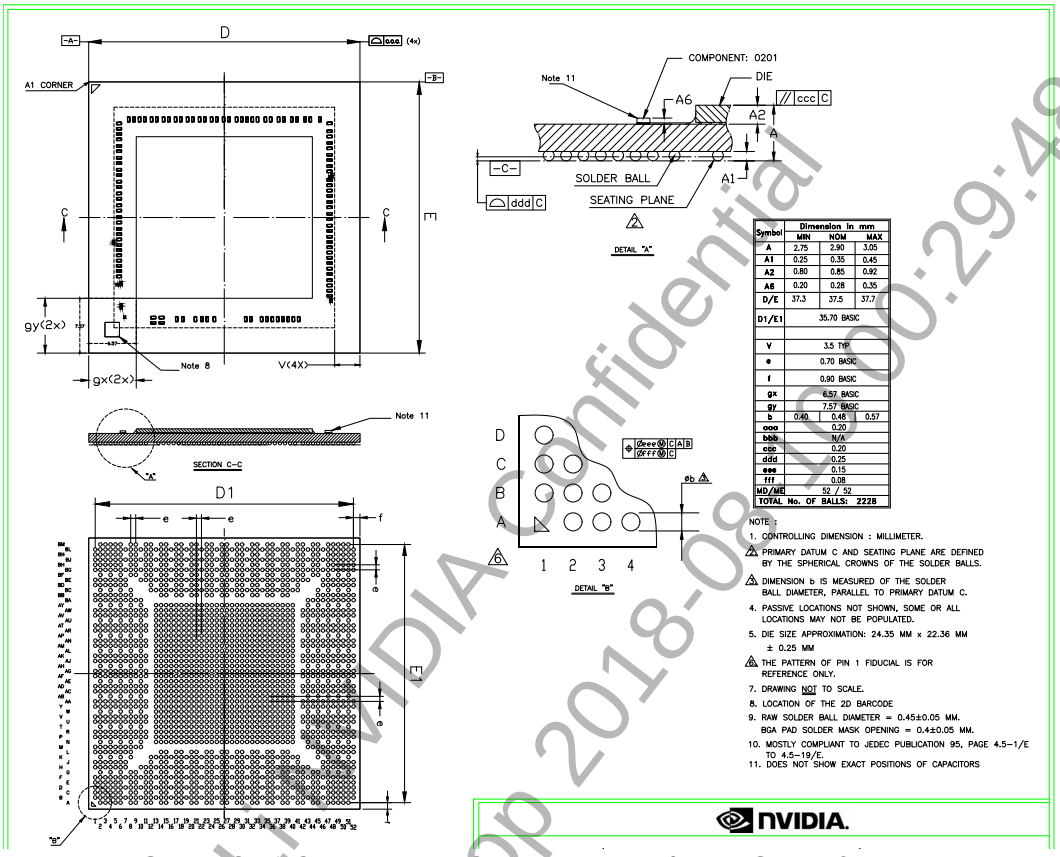
This section provides the following mechanical specifications and characteristics for the GB4B-256 GPUs.

Figure 5.1 shows the package specifications for the GB4B-256 GPUs in a 37.5 mm x 37.5 mm FCBGA package with 2228 balls. Table 5.1 provides the package measurements.

GB4B-256 37.5 mm x 37.5 mm Package Specification

Note: Drawings are not to scale.

Figure 5.1 shows the GB4B-256 package.



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	2.75	2.90	3.05
A1	0.25	0.35	0.45
A2	0.80	0.85	0.92
A6	0.20	0.28	0.35
D/E	37.3	37.5	37.7
D1/E1	35.70 BASIC		
V	3.5 TYP		
e	0.70 BASIC		
f	0.90 BASIC		
gx	6.57 BASIC		
gy	7.57 BASIC		
b	0.40	0.48	0.57
aaa	0.20		
bbb	N/A		
ccc	0.20		
ddd	0.25		
eee	0.15		
fff	0.08		
MD/ME	52 / 52		
TOTAL No. OF BALLS: 2228			

Figure 5.1 GB4B-256 37.5 mm x 37.5 mm Package Specification

Mechanical and Environmental Specifications

Table 5.1 describes the mechanical characteristics for the packages.

Table 5.1 Mechanical Characteristics

Symbol	Parameter	Min.	Nominal	Max.	Units	Notes
P_{cont}	Maximum allowable pressure during PCA, system assembly and operation.	-	≤60	≤80	psi	1
T_{pkg}	Maximum allowable package temperature during device operation	-	-	≤ TBD	˚C	2
T_{reflow}	Maximum package temperature during surface mount to printed circuit board	Refer to NVIDIA specifications 630-0011-001				
e_{max}	Maximum allowable strain during PCA, system assembly or operation			≤500	µstrains	3

Notes:

1) This specification is based on the following conditions:
   a. This specification is based on solder ball deformation and die chips and cracks. Additional requirements may be needed to meet the thermal performance and/or long term reliability as to specific application,
   b. When a compliant thermal interface is used between die and heat sink, the bond line thickness must have less than 20% in variation.
   c. The pressure should be measured on the top of the die surface by an instrument equipped pressure sensors. See details in "GPU Load Distribution Measurement Application Note".
   d. Nominal pressure is the total force divided by the die surface area. Since the pressure may have variations across the whole surfaces. The following additional requirement is applied:
      i. The pressure has to be measured from the top of the die surface with a grid resolution of 1x1mm2 for the pressure sensor.
   e. Both nominal and maximum pressure requirement must be met.
2) Maximum package temperature allowed. It includes device case and/or junction temperature.
3) Strain measurement shall follow IPC-9704, particularly on following items:
   a. The strain shall be measured on the top side of PCB close to the four corners of the package. A rigid PCB is assumed.
   b. For generic application, the max. allowable strain must be no more than 500 µstrains for a board thickness from 1.0 to 3.2mm. A separate requirement may be specified and the qualification test should be performed if
      i. A sensitive PCB laminate and build up structure is used where the pad cratering occurs at a PCB strain of 500 µstrains or below.
      ii. A weak surface finish of PCB is used where cracked solder joint has been observed at a PCB strain of 500 µstrains or below.
      iii. The strain rate is too high (.5000 µstrains/second) during the PCA operations.
   c. For PCB thickness less than 1,0mm, the max. allowable strain shall follow IPC 9704.

Table 5.2 contains information regarding environmental specifications and conditions.

Table 5.2 Environmental Specifications and Conditions

Specifications	Conditions
Storage temperature	-40 °C to 125 °C
Operating humidity	5% to 90% RH
Storage humidity	5% to 95% RH

6 BALL INFORMATION

The TU104 GPUs use the GB4B-256 package. The GB4B-256 ball list and ball map are included in this chapter.

GB4B-256 Ball List (Sorted by Ball Name)

Table 6.1 GB4B-256 Ball List

Ball Name	Ball #
1V8_AON	BA10
1V8_AON	BB14
1V8_AON	BC14
ADC_IN	BJ9
ADC_IN*	BJ11
BUFRST*	BF9
EXT_REFCLK_FL	BJ6
EXT_REFCLK_SLI	AM2
FB_CAL_PD_VDDQ	R44
FB_CAL_PU_GND	P44
FB_CAL_TERM_GND	R45
FB_REFPLL_AVDD0	AF42
FB_REFPLL_AVDD1	L29
FB_VREF	P45
FBA_CLK0	AG45
FBA_CLK0*	AG46
FBA_CLK1	AK46
FBA_CLK1*	AK45
FBA_CMD0	Y51
FBA_CMD1	Y52
FBA_CMD10	AD52
FBA_CMD11	AD51
FBA_CMD12	AD50
FBA_CMD13	AF50
FBA_CMD14	AF51
FBA_CMD15	AF52
FBA_CMD16	AN50
FBA_CMD17	AN51
FBA_CMD18	AN52
FBA_CMD19	AM49
FBA_CMD2	Y49
FBA_CMD20	AM52
FBA_CMD21	AM51
FBA_CMD22	AM50
FBA_CMD23	AK50
FBA_CMD24	AK51
FBA_CMD25	AK52
FBA_CMD26	AJ49
FBA_CMD27	AJ52
FBA_CMD28	AJ51
FBA_CMD29	AJ50
FBA_CMD3	AA52
FBA_CMD30	AG50
FBA_CMD31	AG51
FBA_CMD32	AF49
FBA_CMD33	AG52
FBA_CMD34	Y50
FBA_CMD35	AR50
FBA_CMD4	AA51
FBA_CMD5	AA50
FBA_CMD6	AC50
FBA_CMD7	AC51
FBA_CMD8	AC52
FBA_CMD9	AC49
FBA_D0	U51
FBA_D1	U48
FBA_D10	Y47
FBA_D11	Y46
FBA_D12	V50
FBA_D13	V47
FBA_D14	U52
FBA_D15	V51
FBA_D16	AJ44
FBA_D17	AG48
FBA_D18	AJ45
FBA_D19	AG49
FBA_D2	U50
FBA_D20	AF46
FBA_D21	AF47
FBA_D22	AF48
FBA_D23	AD47
FBA_D24	AD49
FBA_D25	AD48
FBA_D26	AC46
FBA_D27	AC47
FBA_D28	AA47
FBA_D29	AA46
FBA_D3	U49
FBA_D30	AA45
FBA_D31	Y44
FBA_D32	AW51
FBA_D33	BA52
FBA_D34	AW50
FBA_D35	BA51
FBA_D36	BA50
FBA_D37	BB50
FBA_D38	BA49
FBA_D39	AW49
FBA_D4	R51
FBA_D40	AV48
FBA_D41	AT49
FBA_D42	AT47
FBA_D43	AT48
FBA_D44	AT46
FBA_D45	AV51
FBA_D46	AV52
FBA_D47	AV49
FBA_D48	AJ48
FBA_D49	AJ46
FBA_D5	R50
FBA_D50	AJ47
FBA_D51	AK49
FBA_D52	AM47
FBA_D53	AM46
FBA_D54	AN48
FBA_D55	AN49
FBA_D56	AM44
FBA_D57	AM45
FBA_D58	AN45
FBA_D59	AN46
FBA_D6	R47
FBA_D60	AR48
FBA_D61	AN47
FBA_D62	AR47
FBA_D63	AR46
FBA_D7	U46
FBA_D8	V46
FBA_D9	Y45
FBA_DBG_RFU1	AA44
FBA_DBG_RFU2	AN44
FBA_DQM0	U47
FBA_DQM1	Y48
FBA_DQM2	AG47
FBA_DQM3	AC48
FBA_DQM4	BB51
FBA_DQM5	AV50
FBA_DQM6	AM48
FBA_DQM7	AR49
FBA_DQS_WP0	R48
FBA_DQS_WP1	V48

Ball Name	Ball #
FBA_DQS_WP2	AF44
FBA_DQS_WP3	AA48
FBA_DQS_WP4	BB52
FBA_DQS_WP5	AT50
FBA_DQS_WP6	AK48
FBA_DQS_WP7	AR51
FBA_PLL_AVDD	AN42
FBA_WCK01	U45
FBA_WCK01*	U44
FBA_WCK23	AC45
FBA_WCK23*	AC44
FBA_WCK45	AV47
FBA_WCK45*	AV46
FBA_WCK67	AR45
FBA_WCK67*	AR44
FBA_WCKB01	V45
FBA_WCKB01*	V44
FBA_WCKB23	AD46
FBA_WCKB23*	AD45
FBA_WCKB45	AW48
FBA_WCKB45*	AW47
FBA_WCKB67	AT45
FBA_WCKB67*	AT44
FBB_CLK0	H42
FBB_CLK0*	G42
FBB_CLK1	F47
FBB_CLK1*	E47
FBB_CMD0	B35
FBB_CMD1	A35
FBB_CMD10	A39
FBB_CMD11	B39
FBB_CMD12	C39
FBB_CMD13	C41
FBB_CMD14	B41
FBB_CMD15	A41
FBB_CMD16	B49
FBB_CMD17	A49
FBB_CMD18	A48
FBB_CMD19	D47
FBB_CMD2	D35
FBB_CMD20	A47
FBB_CMD21	B47
FBB_CMD22	C47
FBB_CMD23	C45
FBB_CMD24	B45
FBB_CMD25	A45
FBB_CMD26	D44
FBB_CMD27	A44

Ball Name	Ball #
FBB_CMD28	B44
FBB_CMD29	C44
FBB_CMD3	A36
FBB_CMD30	C42
FBB_CMD31	B42
FBB_CMD32	D41
FBB_CMD33	A42
FBB_CMD34	C35
FBB_CMD35	B50
FBB_CMD4	B36
FBB_CMD5	C36
FBB_CMD6	C38
FBB_CMD7	B38
FBB_CMD8	A38
FBB_CMD9	D38
FBB_D0	H32
FBB_D1	D32
FBB_D10	J36
FBB_D11	F36
FBB_D12	F33
FBB_D13	D33
FBB_D14	J32
FBB_D15	G33
FBB_D16	E45
FBB_D17	D45
FBB_D18	F45
FBB_D19	G45
FBB_D2	A33
FBB_D20	D42
FBB_D21	E42
FBB_D22	F42
FBB_D23	H41
FBB_D24	E41
FBB_D25	F39
FBB_D26	E39
FBB_D27	D39
FBB_D28	F38
FBB_D29	E38
FBB_D3	B32
FBB_D30	D36
FBB_D31	E36
FBB_D32	M50
FBB_D33	P48
FBB_D34	M51
FBB_D35	M49
FBB_D36	P47
FBB_D37	P52
FBB_D38	R46

Ball Name	Ball #
FBB_D39	P46
FBB_D4	E32
FBB_D40	L50
FBB_D41	L51
FBB_D42	L52
FBB_D43	L49
FBB_D44	M46
FBB_D45	L47
FBB_D46	M48
FBB_D47	M47
FBB_D48	D48
FBB_D49	C50
FBB_D5	G32
FBB_D50	C48
FBB_D51	C49
FBB_D52	E49
FBB_D53	E50
FBB_D54	F49
FBB_D55	F48
FBB_D56	F50
FBB_D57	D52
FBB_D58	J50
FBB_D59	H48
FBB_D6	J30
FBB_D60	H51
FBB_D61	J51
FBB_D62	H49
FBB_D63	H52
FBB_D7	F32
FBB_D8	H36
FBB_D9	G36
FBB_DBG_RFU1	J35
FBB_DBG_RFU2	J41
FBB_DQM0	C32
FBB_DQM1	E33
FBB_DQM2	E44
FBB_DQM3	G39
FBB_DQM4	P49
FBB_DQM5	L48
FBB_DQM6	D50
FBB_DQM7	H50
FBB_DQS_WP0	B33
FBB_DQS_WP1	E35
FBB_DQS_WP2	G44
FBB_DQS_WP3	H38
FBB_DQS_WP4	P50
FBB_DQS_WP5	J48
FBB_DQS_WP6	D51

Ball Name	Ball #
FBB_DQS_WP7	F51
FBB_PLL_AVDD	L38
FBB_WCK01	J33
FBB_WCK01*	H33
FBB_WCK23	J39
FBB_WCK23*	H39
FBB_WCK45	L46
FBB_WCK45*	L45
FBB_WCK67	H47
FBB_WCK67*	H46
FBB_WCKB01	G35
FBB_WCKB01*	H35
FBB_WCKB23	F41
FBB_WCKB23*	G41
FBB_WCKB45	M44
FBB_WCKB45*	M45
FBB_WCKB67	J47
FBB_WCKB67*	J46
FBC_CLK0	G15
FBC_CLK0*	F15
FBC_CLK1	H21
FBC_CLK1*	J21
FBC_CMD0	C11
FBC_CMD1	B11
FBC_CMD10	D14
FBC_CMD11	A15
FBC_CMD12	B15
FBC_CMD13	C15
FBC_CMD14	C17
FBC_CMD15	B17
FBC_CMD16	B24
FBC_CMD17	A24
FBC_CMD18	D23
FBC_CMD19	A23
FBC_CMD2	A11
FBC_CMD20	B23
FBC_CMD21	C23
FBC_CMD22	C21
FBC_CMD23	B21
FBC_CMD24	A21
FBC_CMD25	D20
FBC_CMD26	A20
FBC_CMD27	B20
FBC_CMD28	C20
FBC_CMD29	C18
FBC_CMD3	D11
FBC_CMD30	B18
FBC_CMD31	A18

Ball Name	Ball #
FBC_CMD32	A17
FBC_CMD33	D17
FBC_CMD34	A9
FBC_CMD35	C24
FBC_CMD4	A12
FBC_CMD5	B12
FBC_CMD6	C12
FBC_CMD7	C14
FBC_CMD8	B14
FBC_CMD9	A14
FBC_D0	C6
FBC_D1	D6
FBC_D10	E9
FBC_D11	B9
FBC_D12	B8
FBC_D13	A8
FBC_D14	F6
FBC_D15	E6
FBC_D16	F18
FBC_D17	G18
FBC_D18	E18
FBC_D19	H18
FBC_D2	A6
FBC_D20	D15
FBC_D21	E15
FBC_D22	G17
FBC_D23	H17
FBC_D24	J15
FBC_D25	H15
FBC_D26	E14
FBC_D27	F14
FBC_D28	H11
FBC_D29	G11
FBC_D3	B6
FBC_D30	F11
FBC_D31	E11
FBC_D32	J29
FBC_D33	F30
FBC_D34	H29
FBC_D35	G30
FBC_D36	B30
FBC_D37	A30
FBC_D38	H30
FBC_D39	C30
FBC_D4	B4
FBC_D40	D27
FBC_D41	J26
FBC_D42	F27

Ball Name	Ball #
FBC_D43	G27
FBC_D44	C27
FBC_D45	B27
FBC_D46	A27
FBC_D47	G29
FBC_D48	H20
FBC_D49	D18
FBC_D5	A4
FBC_D50	G20
FBC_D51	E20
FBC_D52	F23
FBC_D53	E21
FBC_D54	D21
FBC_D55	E23
FBC_D56	G24
FBC_D57	H26
FBC_D58	F24
FBC_D59	G26
FBC_D6	B3
FBC_D60	F26
FBC_D61	D26
FBC_D62	B26
FBC_D63	C26
FBC_D7	C4
FBC_D8	D9
FBC_D9	C9
FBC_DBG_RFU1	J14
FBC_DBG_RFU2	J23
FBC_DQM0	A5
FBC_DQM1	C8
FBC_DQM2	J18
FBC_DQM3	F12
FBC_DQM4	D29
FBC_DQM5	E27
FBC_DQM6	F20
FBC_DQM7	E26
FBC_DQS_WP0	D5
FBC_DQS_WP1	D8
FBC_DQS_WP2	E17
FBC_DQS_WP3	E12
FBC_DQS_WP4	E30
FBC_DQS_WP5	B29
FBC_DQS_WP6	G21
FBC_DQS_WP7	E24
FBC_PLL_AVDD	L17
FBC_WCK01	F8
FBC_WCK01*	G8
FBC_WCK23	H12

Ball Name	Ball #
FBC_WCK23*	G12
FBC_WCK45	J27
FBC_WCK45*	H27
FBC_WCK67	G23
FBC_WCK67*	H23
FBC_WCKB01	G9
FBC_WCKB01*	F9
FBC_WCKB23	G14
FBC_WCKB23*	H14
FBC_WCKB45	E29
FBC_WCKB45*	F29
FBC_WCKB67	H24
FBC_WCKB67*	J24
FBD_CLK0	Y8
FBD_CLK0*	Y7
FBD_CLK1	R8
FBD_CLK1*	R7
FBD_CMD0	AD2
FBD_CMD1	AD1
FBD_CMD10	Y1
FBD_CMD11	Y2
FBD_CMD12	Y3
FBD_CMD13	V3
FBD_CMD14	V2
FBD_CMD15	V1
FBD_CMD16	L3
FBD_CMD17	L2
FBD_CMD18	L1
FBD_CMD19	M4
FBD_CMD2	AD4
FBD_CMD20	M1
FBD_CMD21	M2
FBD_CMD22	M3
FBD_CMD23	P3
FBD_CMD24	P2
FBD_CMD25	P1
FBD_CMD26	R4
FBD_CMD27	R1
FBD_CMD28	R2
FBD_CMD29	R3
FBD_CMD3	AC1
FBD_CMD30	U3
FBD_CMD31	U2
FBD_CMD32	V4
FBD_CMD33	U1
FBD_CMD34	AD3
FBD_CMD35	J3
FBD_CMD4	AC2

Ball Name	Ball #
FBD_CMD5	AC3
FBD_CMD6	AA3
FBD_CMD7	AA2
FBD_CMD8	AA1
FBD_CMD9	AA4
FBD_D0	AK8
FBD_D1	AK4
FBD_D10	AG6
FBD_D11	AG7
FBD_D12	AJ4
FBD_D13	AJ5
FBD_D14	AJ6
FBD_D15	AG5
FBD_D16	Y6
FBD_D17	Y5
FBD_D18	V5
FBD_D19	Y4
FBD_D2	AK2
FBD_D20	AA6
FBD_D21	AA5
FBD_D22	AC5
FBD_D23	AC4
FBD_D24	AD7
FBD_D25	AC6
FBD_D26	AF6
FBD_D27	AD6
FBD_D28	AF7
FBD_D29	AF8
FBD_D3	AK3
FBD_D30	AF2
FBD_D31	AF3
FBD_D32	F4
FBD_D33	E1
FBD_D34	F3
FBD_D35	F5
FBD_D36	D2
FBD_D37	D1
FBD_D38	C3
FBD_D39	C2
FBD_D4	AK5
FBD_D40	J5
FBD_D41	J4
FBD_D42	L8
FBD_D43	J2
FBD_D44	F1
FBD_D45	F2
FBD_D46	H4
FBD_D47	H5

Ball Name	Ball #
FBD_D48	V7
FBD_D49	V8
FBD_D5	AK6
FBD_D50	V6
FBD_D51	V9
FBD_D52	U4
FBD_D53	R5
FBD_D54	R6
FBD_D55	U8
FBD_D56	P6
FBD_D57	R9
FBD_D58	P4
FBD_D59	P5
FBD_D6	AK9
FBD_D60	L7
FBD_D61	L6
FBD_D62	L4
FBD_D63	L5
FBD_D7	AK7
FBD_D8	AG4
FBD_D9	AF9
FBD_DBG_RFU1	AC9
FBD_DBG_RFU2	P9
FBD_DQM0	AJ1
FBD_DQM1	AG1
FBD_DQM2	AA7
FBD_DQM3	AD5
FBD_DQM4	D3
FBD_DQM5	H3
FBD_DQM6	U5
FBD_DQM7	M9
FBD_DQS_WP0	AJ3
FBD_DQS_WP1	AG2
FBD_DQS_WP2	AA9
FBD_DQS_WP3	AF4
FBD_DQS_WP4	E3
FBD_DQS_WP5	H2
FBD_DQS_WP6	U6
FBD_DQS_WP7	M5
FBD_PLL_AVDD	V11
FBD_WCK01	AJ8
FBD_WCK01*	AJ7
FBD_WCK23	AD8
FBD_WCK23*	AD9
FBD_WCK45	J6
FBD_WCK45*	J7
FBD_WCK67	P8
FBD_WCK67*	P7

Ball Name	Ball #
FBD_WCKB01	AG8
FBD_WCKB01*	AG9
FBD_WCKB23	AC7
FBD_WCKB23*	AC8
FBD_WCKB45	H7
FBD_WCKB45*	H6
FBD_WCKB67	M7
FBD_WCKB67*	M8
FBVDDQ	AA10
FBVDDQ	AA11
FBVDDQ	AA42
FBVDDQ	AA43
FBVDDQ	AC10
FBVDDQ	AC11
FBVDDQ	AC42
FBVDDQ	AC43
FBVDDQ	AD10
FBVDDQ	AD11
FBVDDQ	AD42
FBVDDQ	AD43
FBVDDQ	AF10
FBVDDQ	AF43
FBVDDQ	AG10
FBVDDQ	AG11
FBVDDQ	AG42
FBVDDQ	AG43
FBVDDQ	AJ10
FBVDDQ	AJ11
FBVDDQ	AJ42
FBVDDQ	AJ43
FBVDDQ	AK10
FBVDDQ	AK11
FBVDDQ	AK42
FBVDDQ	AK43
FBVDDQ	AM42
FBVDDQ	AM43
FBVDDQ	AN43
FBVDDQ	AR42
FBVDDQ	AR43
FBVDDQ	AT43
FBVDDQ	K12
FBVDDQ	K14
FBVDDQ	K15
FBVDDQ	K17
FBVDDQ	K18
FBVDDQ	K20
FBVDDQ	K21
FBVDDQ	K23

Ball Name	Ball #
FBVDDQ	K24
FBVDDQ	K26
FBVDDQ	K27
FBVDDQ	K29
FBVDDQ	K30
FBVDDQ	K32
FBVDDQ	K33
FBVDDQ	K35
FBVDDQ	K36
FBVDDQ	K38
FBVDDQ	K39
FBVDDQ	K41
FBVDDQ	L14
FBVDDQ	L15
FBVDDQ	L18
FBVDDQ	L20
FBVDDQ	L21
FBVDDQ	L23
FBVDDQ	L24
FBVDDQ	L26
FBVDDQ	L27
FBVDDQ	L30
FBVDDQ	L32
FBVDDQ	L33
FBVDDQ	L35
FBVDDQ	L36
FBVDDQ	L39
FBVDDQ	M10
FBVDDQ	M43
FBVDDQ	P10
FBVDDQ	P11
FBVDDQ	P42
FBVDDQ	P43
FBVDDQ	R10
FBVDDQ	R11
FBVDDQ	R42
FBVDDQ	R43
FBVDDQ	U10
FBVDDQ	U11
FBVDDQ	U43
FBVDDQ	V10
FBVDDQ	V42
FBVDDQ	V43
FBVDDQ	Y10
FBVDDQ	Y11
FBVDDQ	Y42
FBVDDQ	Y43
FBVDDQ_SENSE	E52

Ball Name	Ball #
FP_FUSE_SRC	BD14
GND	A2
GND	A26
GND	A29
GND	A3
GND	A32
GND	A50
GND	A51
GND	AA49
GND	AA8
GND	AB10
GND	AB14
GND	AB15
GND	AB16
GND	AB17
GND	AB18
GND	AB19
GND	AB2
GND	AB20
GND	AB21
GND	AB22
GND	AB23
GND	AB24
GND	AB25
GND	AB26
GND	AB27
GND	AB28
GND	AB29
GND	AB30
GND	AB31
GND	AB32
GND	AB33
GND	AB34
GND	AB35
GND	AB36
GND	AB37
GND	AB38
GND	AB39
GND	AB4
GND	AB43
GND	AB45
GND	AB47
GND	AB49
GND	AB51
GND	AB6
GND	AB8
GND	AD14
GND	AD15

Ball Name	Ball #
GND	AD16
GND	AD17
GND	AD18
GND	AD19
GND	AD20
GND	AD21
GND	AD22
GND	AD23
GND	AD24
GND	AD25
GND	AD26
GND	AD27
GND	AD28
GND	AD29
GND	AD30
GND	AD31
GND	AD32
GND	AD33
GND	AD34
GND	AD35
GND	AD36
GND	AD37
GND	AD38
GND	AD39
GND	AD44
GND	AE10
GND	AE2
GND	AE4
GND	AE43
GND	AE45
GND	AE47
GND	AE49
GND	AE51
GND	AE6
GND	AE8
GND	AF1
GND	AF19
GND	AF20
GND	AF21
GND	AF22
GND	AF23
GND	AF27
GND	AF28
GND	AF29
GND	AF35
GND	AF36
GND	AF37
GND	AF38

Ball Name	Ball #
GND	AF39
GND	AF45
GND	AF5
GND	AG14
GND	AG15
GND	AG16
GND	AG17
GND	AG18
GND	AG24
GND	AG25
GND	AG26
GND	AG3
GND	AG30
GND	AG31
GND	AG32
GND	AG33
GND	AG34
GND	AG44
GND	AH10
GND	AH2
GND	AH4
GND	AH43
GND	AH45
GND	AH47
GND	AH49
GND	AH51
GND	AH6
GND	AH8
GND	AJ14
GND	AJ15
GND	AJ16
GND	AJ17
GND	AJ18
GND	AJ19
GND	AJ2
GND	AJ20
GND	AJ21
GND	AJ22
GND	AJ23
GND	AJ24
GND	AJ25
GND	AJ26
GND	AJ27
GND	AJ28
GND	AJ29
GND	AJ30
GND	AJ31
GND	AJ32

Ball Name	Ball #
GND	AJ33
GND	AJ34
GND	AJ35
GND	AJ36
GND	AJ37
GND	AJ38
GND	AJ39
GND	AJ9
GND	AK1
GND	AK44
GND	AK47
GND	AL10
GND	AL14
GND	AL15
GND	AL16
GND	AL17
GND	AL18
GND	AL19
GND	AL2
GND	AL20
GND	AL21
GND	AL22
GND	AL23
GND	AL24
GND	AL25
GND	AL26
GND	AL27
GND	AL28
GND	AL29
GND	AL30
GND	AL31
GND	AL32
GND	AL33
GND	AL34
GND	AL35
GND	AL36
GND	AL37
GND	AL38
GND	AL39
GND	AL4
GND	AL43
GND	AL45
GND	AL47
GND	AL49
GND	AL51
GND	AL6
GND	AL8
GND	AM4

Ball Name	Ball #
GND	AM9
GND	AN14
GND	AN15
GND	AN16
GND	AN17
GND	AN18
GND	AN19
GND	AN20
GND	AN21
GND	AN22
GND	AN23
GND	AN24
GND	AN25
GND	AN26
GND	AN27
GND	AN28
GND	AN29
GND	AN30
GND	AN31
GND	AN32
GND	AN33
GND	AN34
GND	AN35
GND	AN36
GND	AN37
GND	AN38
GND	AN39
GND	AN4
GND	AN5
GND	AN8
GND	AP10
GND	AP2
GND	AP4
GND	AP43
GND	AP45
GND	AP47
GND	AP49
GND	AP51
GND	AP6
GND	AP8
GND	AR14
GND	AR15
GND	AR16
GND	AR17
GND	AR18
GND	AR19
GND	AR20
GND	AR21

Ball Name	Ball #
GND	AR22
GND	AR23
GND	AR24
GND	AR25
GND	AR26
GND	AR27
GND	AR28
GND	AR29
GND	AR30
GND	AR31
GND	AR32
GND	AR33
GND	AR34
GND	AR35
GND	AR36
GND	AR37
GND	AR38
GND	AR39
GND	AR4
GND	AR52
GND	AR9
GND	AT4
GND	AT5
GND	AT51
GND	AT52
GND	AT8
GND	AU10
GND	AU14
GND	AU15
GND	AU16
GND	AU17
GND	AU18
GND	AU19
GND	AU2
GND	AU20
GND	AU21
GND	AU22
GND	AU23
GND	AU24
GND	AU25
GND	AU26
GND	AU27
GND	AU28
GND	AU29
GND	AU30
GND	AU31
GND	AU32
GND	AU33

Ball Name	Ball #
GND	AU34
GND	AU35
GND	AU36
GND	AU37
GND	AU38
GND	AU39
GND	AU4
GND	AU45
GND	AU47
GND	AU49
GND	AU51
GND	AU6
GND	AU8
GND	AV4
GND	AV45
GND	AV9
GND	AW14
GND	AW15
GND	AW16
GND	AW17
GND	AW18
GND	AW19
GND	AW20
GND	AW21
GND	AW22
GND	AW23
GND	AW24
GND	AW25
GND	AW26
GND	AW27
GND	AW28
GND	AW29
GND	AW30
GND	AW31
GND	AW32
GND	AW33
GND	AW34
GND	AW35
GND	AW36
GND	AW37
GND	AW38
GND	AW39
GND	AW4
GND	AW46
GND	AW5
GND	AW52
GND	AW8
GND	AY10

Ball Name	Ball #
GND	AY2
GND	AY4
GND	AY47
GND	AY49
GND	AY51
GND	AY6
GND	AY8
GND	B1
GND	B10
GND	B13
GND	B16
GND	B19
GND	B2
GND	B22
GND	B25
GND	B28
GND	B31
GND	B34
GND	B37
GND	B40
GND	B43
GND	B46
GND	B48
GND	B5
GND	B51
GND	B52
GND	B7
GND	BA48
GND	BA9
GND	BB49
GND	BC13
GND	BC16
GND	BC19
GND	BC2
GND	BC22
GND	BC25
GND	BC28
GND	BC31
GND	BC34
GND	BC37
GND	BC4
GND	BC51
GND	BC6
GND	BC8
GND	BD26
GND	BD29
GND	BD32
GND	BD35

Ball Name	Ball #
GND	BD38
GND	BD52
GND	BE10
GND	BE13
GND	BE15
GND	BE16
GND	BE18
GND	BE19
GND	BE21
GND	BE22
GND	BE24
GND	BE25
GND	BE27
GND	BE28
GND	BE30
GND	BE31
GND	BE33
GND	BE34
GND	BE36
GND	BE37
GND	BE39
GND	BE40
GND	BF2
GND	BF4
GND	BF41
GND	BF6
GND	BG10
GND	BG13
GND	BG16
GND	BG19
GND	BG22
GND	BG25
GND	BG28
GND	BG31
GND	BG34
GND	BG37
GND	BG40
GND	BG42
GND	BG7
GND	BH15
GND	BH18
GND	BH2
GND	BH21
GND	BH24
GND	BH27
GND	BH30
GND	BH33
GND	BH36

Ball Name	Ball #
GND	BH39
GND	BH42
GND	BH5
GND	BJ10
GND	BJ12
GND	BJ13
GND	BJ14
GND	BJ15
GND	BJ16
GND	BJ17
GND	BJ18
GND	BJ19
GND	BJ20
GND	BJ21
GND	BJ22
GND	BJ23
GND	BJ24
GND	BJ25
GND	BJ26
GND	BJ27
GND	BJ28
GND	BJ29
GND	BJ30
GND	BJ31
GND	BJ32
GND	BJ33
GND	BJ34
GND	BJ35
GND	BJ36
GND	BJ37
GND	BJ38
GND	BJ39
GND	BJ40
GND	BJ41
GND	BJ42
GND	BJ43
GND	BJ7
GND	BK1
GND	BL1
GND	BL10
GND	BL13
GND	BL16
GND	BL19
GND	BL2
GND	BL22
GND	BL25
GND	BL28
GND	BL31

Ball Name	Ball #
GND	BL34
GND	BL37
GND	BL40
GND	BL43
GND	BL5
GND	BL7
GND	BM2
GND	BM3
GND	C1
GND	C29
GND	C33
GND	C5
GND	C51
GND	C52
GND	D10
GND	D12
GND	D13
GND	D16
GND	D19
GND	D22
GND	D24
GND	D25
GND	D28
GND	D30
GND	D31
GND	D34
GND	D37
GND	D4
GND	D40
GND	D43
GND	D46
GND	D49
GND	D7
GND	E2
GND	E4
GND	E48
GND	E5
GND	E51
GND	E8
GND	F10
GND	F13
GND	F16
GND	F17
GND	F19
GND	F21
GND	F22
GND	F25
GND	F28

Ball Name	Ball #
GND	F31
GND	F34
GND	F35
GND	F37
GND	F40
GND	F43
GND	F44
GND	F46
GND	F52
GND	F7
GND	G2
GND	G38
GND	G4
GND	G47
GND	G49
GND	G51
GND	G6
GND	H1
GND	H10
GND	H13
GND	H16
GND	H19
GND	H22
GND	H25
GND	H28
GND	H31
GND	H34
GND	H37
GND	H40
GND	H43
GND	J1
GND	J12
GND	J17
GND	J20
GND	J38
GND	J49
GND	J52
GND	K13
GND	K16
GND	K19
GND	K2
GND	K22
GND	K25
GND	K28
GND	K31
GND	K34
GND	K37
GND	K4

Ball Name	Ball #
GND	K40
GND	K45
GND	K47
GND	K49
GND	K51
GND	K6
GND	K8
GND	M52
GND	M6
GND	N10
GND	N2
GND	N4
GND	N43
GND	N45
GND	N47
GND	N49
GND	N51
GND	N6
GND	N8
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	P20
GND	P21
GND	P22
GND	P23
GND	P24
GND	P25
GND	P26
GND	P27
GND	P28
GND	P29
GND	P30
GND	P31
GND	P32
GND	P33
GND	P34
GND	P35
GND	P36
GND	P37
GND	P38
GND	P39
GND	P51
GND	R49
GND	R52

Ball Name	Ball #
GND	T10
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T2
GND	T20
GND	T21
GND	T22
GND	T23
GND	T24
GND	T25
GND	T26
GND	T27
GND	T28
GND	T29
GND	T30
GND	T31
GND	T32
GND	T33
GND	T34
GND	T35
GND	T36
GND	T37
GND	T38
GND	T39
GND	T4
GND	T43
GND	T45
GND	T47
GND	T49
GND	T51
GND	T6
GND	T8
GND	U7
GND	U9
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V20
GND	V21
GND	V22
GND	V23

Ball Name	Ball #
GND	V24
GND	V25
GND	V26
GND	V27
GND	V28
GND	V29
GND	V30
GND	V31
GND	V32
GND	V33
GND	V34
GND	V35
GND	V36
GND	V37
GND	V38
GND	V39
GND	V49
GND	V52
GND	W10
GND	W2
GND	W4
GND	W43
GND	W45
GND	W47
GND	W49
GND	W51
GND	W6
GND	W8
GND	Y14
GND	Y15
GND	Y16
GND	Y17
GND	Y18
GND	Y19
GND	Y20
GND	Y21
GND	Y22
GND	Y23
GND	Y24
GND	Y25
GND	Y26
GND	Y27
GND	Y28
GND	Y29
GND	Y30
GND	Y31
GND	Y32
GND	Y33

Ball Name	Ball #
GND	Y34
GND	Y35
GND	Y36
GND	Y37
GND	Y38
GND	Y39
GND	Y9
GND	BC24
GND_SENSE	BL45
GPCPLL_AVDD0	U42
GPCPLL_AVDD1	AF11
GPIO0	BD6
GPIO1	BB5
GPIO10	BD3
GPIO11	BH3
GPIO12	BE6
GPIO13	BB1
GPIO14	BG4
GPIO15	BG1
GPIO16	BE2
GPIO17	BH1
GPIO18	BE3
GPIO19	BD4
GPIO2	BD1
GPIO20	BE5
GPIO21	BA5
GPIO22	BB6
GPIO23	BG3
GPIO24	BD5
GPIO25	BB2
GPIO26	BE7
GPIO27	BA4
GPIO28	BB4
GPIO29	BA3
GPIO3	BE4
GPIO30	BB3
GPIO4	BE1
GPIO5	BG2
GPIO6	BD2
GPIO7	BD7
GPIO8	BH4
GPIO9	BJ3
I2CB_SCL	BG8
I2CB_SDA	BF8
I2CC_SCL	BG9
I2CC_SDA	BH9
I2CS_SCL	BJ8
I2CS_SDA	BH8

Ball Name	Ball #
IFP_IOVDD	BB17
IFP_IOVDD	BC23
IFP_IOVDD	BB18
IFP_IOVDD	BB20
IFP_IOVDD	BB21
IFP_IOVDD	BB23
IFP_IOVDD	BC17
IFP_IOVDD	BC18
IFP_IOVDD	BC20
IFP_IOVDD	BC21
IFPA_AUX_SCL	BG11
IFPA_AUX_SDA*	BH11
IFPA_L0	BG24
IFPA_L0*	BF24
IFPA_L1	BE23
IFPA_L1*	BF23
IFPA_L2	BH23
IFPA_L2*	BG23
IFPA_L3	BG21
IFPA_L3*	BF21
IFPAB_PLLVDD	BD21
IFPAB_RSET	BD23
IFPB_AUX_SCL	BH12
IFPB_AUX_SDA*	BG12
IFPB_L0	BK21
IFPB_L0*	BL21
IFPB_L1	BM21
IFPB_L1*	BM20
IFPB_L2	BL20
IFPB_L2*	BK20
IFPB_L3	BK18
IFPB_L3*	BL18
IFPC_AUX_SCL	BK9
IFPC_AUX_SDA*	BL9
IFPC_L0	BE20
IFPC_L0*	BF20
IFPC_L1	BH20
IFPC_L1*	BG20
IFPC_L2	BG18
IFPC_L2*	BF18
IFPC_L3	BE17

Ball Name	Ball #
IFPC_L3*	BF17
IFPCD_PLLVDD	BD18
IFPCD_RSET	BD20
IFPD_AUX_SCL	BE11
IFPD_AUX_SDA*	BF11
IFPD_L0	BM18
IFPD_L0*	BM17
IFPD_L1	BL17
IFPD_L1*	BK17
IFPD_L2	BK15
IFPD_L2*	BL15
IFPD_L3	BM15
IFPD_L3*	BM14
IFPE_AUX_SCL	BK8
IFPE_AUX_SDA*	BL8
IFPE_L0	BH17
IFPE_L0*	BG17
IFPE_L1	BG15
IFPE_L1*	BF15
IFPE_L2	BE14
IFPE_L2*	BF14
IFPE_L3	BH14
IFPE_L3*	BG14
IFPE_PLLVDD	BD15
IFPE_RSET	BD17
IFPF_AUX_SCL	BM8
IFPF_AUX_SDA*	BM9
IFPF_L0	BL14
IFPF_L0*	BK14
IFPF_L1	BK12
IFPF_L1*	BL12
IFPF_L2	BM12
IFPF_L2*	BM11
IFPF_L3	BL11
IFPF_L3*	BK11
JTAG_TCK	BK24
JTAG_TDI	BM23
JTAG_TDO	BM24
JTAG_TMS	BL23
JTAG_TRST*	BL24
NC	BD24
NC	BM44

Ball Name	Ball #
NC	BM45
NVHS_CVDD	AR10
NVHS_CVDD	AT11
NVHS_DVDD	AT10
NVHS_DVDD	AT9
NVHS_DVDD	AV10
NVHS_DVDD	AV11
NVHS_HVDD	AM10
NVHS_HVDD	AM11
NVHS_HVDD	AN10
NVHS_HVDD	AN11
NVHS_HVDD	AR11
NVHS_PLL_HVDD	AN9
NVHS_REFCLK	AM6
NVHS_REFCLK*	AM5
NVHS_TERMP	AM3
NVHS0_RX0	AM1
NVHS0_RX0*	AN1
NVHS0_RX1	AN2
NVHS0_RX1*	AN3
NVHS0_RX2	AR3
NVHS0_RX2*	AR2
NVHS0_RX3	AR1
NVHS0_RX3*	AT1
NVHS0_RX4	AT2
NVHS0_RX4*	AT3
NVHS0_RX5	AV3
NVHS0_RX5*	AV2
NVHS0_RX6	AV1
NVHS0_RX6*	AW1
NVHS0_RX7	AW2
NVHS0_RX7*	AW3
NVHS0_TX0	AM7
NVHS0_TX0*	AM8
NVHS0_TX1	AN7
NVHS0_TX1*	AN6
NVHS0_TX2	AR6
NVHS0_TX2*	AR5
NVHS0_TX3	AR7
NVHS0_TX3*	AR8
NVHS0_TX4	AT7
NVHS0_TX4*	AT6
NVHS0_TX5	AV6
NVHS0_TX5*	AV5
NVHS0_TX6	AV7
NVHS0_TX6*	AV8
NVHS0_TX7	AW7
NVHS0_TX7*	AW6

Ball Name	Ball #
NVJTAG_SEL	BK23
OVERT	BG5
PEX_CLKREQ*	BL26
PEX_CVDD	BB33
PEX_CVDD	BC33
PEX_DVDD	BB35
PEX_DVDD	BB36
PEX_DVDD	BC35
PEX_DVDD	BC36
PEX_DVDD	BD33
PEX_DVDD	BD36
PEX_HVDD	BB26
PEX_HVDD	BB27
PEX_HVDD	BB29
PEX_HVDD	BB32
PEX_HVDD	BC26
PEX_HVDD	BC27
PEX_HVDD	BC29
PEX_HVDD	BC30
PEX_HVDD	BC32
PEX_HVDD	BD27
PEX_HVDD	BD30
PEX_PLL_HVDD	BB30
PEX_REFCLK	BM26
PEX_REFCLK*	BM27
PEX_RST*	BK26
PEX_RX0	BL27
PEX_RX0*	BK27
PEX_RX1	BK29
PEX_RX1*	BL29
PEX_RX10	BK38
PEX_RX10*	BL38
PEX_RX11	BM38
PEX_RX11*	BM39
PEX_RX12	BL39
PEX_RX12*	BK39
PEX_RX13	BK41
PEX_RX13*	BL41
PEX_RX14	BM41
PEX_RX14*	BM42
PEX_RX15	BL42
PEX_RX15*	BK42
PEX_RX2	BM29
PEX_RX2*	BM30
PEX_RX3	BL30
PEX_RX3*	BK30
PEX_RX4	BK32
PEX_RX4*	BL32

Ball Name	Ball #
PEX_RX5	BM32
PEX_RX5*	BM33
PEX_RX6	BL33
PEX_RX6*	BK33
PEX_RX7	BK35
PEX_RX7*	BL35
PEX_RX8	BM35
PEX_RX8*	BM36
PEX_RX9	BL36
PEX_RX9*	BK36
PEX_TERMP	BL44
PEX_TX0	BG26
PEX_TX0*	BH26
PEX_TX1	BF26
PEX_TX1*	BE26
PEX_TX10	BF35
PEX_TX10*	BE35
PEX_TX11	BF36
PEX_TX11*	BG36
PEX_TX12	BG38
PEX_TX12*	BH38
PEX_TX13	BF38
PEX_TX13*	BE38
PEX_TX14	BF39
PEX_TX14*	BG39
PEX_TX15	BH41
PEX_TX15*	BG41
PEX_TX2	BF27
PEX_TX2*	BG27
PEX_TX3	BG29
PEX_TX3*	BH29
PEX_TX4	BF29
PEX_TX4*	BE29
PEX_TX5	BF30
PEX_TX5*	BG30
PEX_TX6	BG32
PEX_TX6*	BH32
PEX_TX7	BF32
PEX_TX7*	BE32
PEX_TX8	BF33
PEX_TX8*	BG33
PEX_TX9	BG35
PEX_TX9*	BH35
PEX_WAKE_N*	BK44
ROM_CS*	BJ4
ROM_SCLK	BK3
ROM_SI	BK2
ROM_SO	BK4

Ball Name	Ball #
SP_PLLVDD	BD12
STRAP0	BL3
STRAP1	BL4
STRAP2	BM4
STRAP3	BM5
STRAP4	BK5
STRAP5	BJ5
THERMDN	BJ1
THERMDP	BJ2
TS_VREF	BF12
USB_DVDD	BB15
USB_DVDD	BC15
USB_HVDD	AW10
USB_HVDD	AW11
USB_L0	BA2
USB_L0*	BA1
USB_L1	BA8
USB_L1*	BA7
USB_PLL_HVDD	AW9
USB_RBIAS	BA6
USB_SCL	BB8
USB_SDA	BB7
USB_TERMP0	BG6
USB_TERMP1	BH6
USB_VDDP	BE12
VDD	AA13
VDD	AA14
VDD	AA15
VDD	AA16
VDD	AA17
VDD	AA18
VDD	AA19
VDD	AA20
VDD	AA21
VDD	AA22
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VDD	AA28
VDD	AA29
VDD	AA30
VDD	AA31
VDD	AA32

Ball Name	Ball #
VDD	AA33
VDD	AA34
VDD	AA35
VDD	AA36
VDD	AA37
VDD	AA38
VDD	AA39
VDD	AA40
VDD	AB13
VDD	AB40
VDD	AC13
VDD	AC14
VDD	AC15
VDD	AC16
VDD	AC17
VDD	AC18
VDD	AC19
VDD	AC20
VDD	AC21
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VDD	AC33
VDD	AC34
VDD	AC35
VDD	AC36
VDD	AC37
VDD	AC38
VDD	AC39
VDD	AC40
VDD	AD13
VDD	AD40
VDD	AE13
VDD	AE14
VDD	AE15
VDD	AE16
VDD	AE17
VDD	AE18
VDD	AE19
VDD	AE20

Ball Name	Ball #
VDD	AE21
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VDD	AE28
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VDD	AE36
VDD	AE37
VDD	AE38
VDD	AE39
VDD	AE40
VDD	AF13
VDD	AF14
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VDD	AG38

Ball Name	Ball #
VDD	AG39
VDD	AG40
VDD	AH13
VDD	AH14
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VDD	AH18
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VDD	AH38
VDD	AH39
VDD	AH40
VDD	AJ13
VDD	AJ40
VDD	AK13
VDD	AK14
VDD	AK15
VDD	AK16
VDD	AK17
VDD	AK18
VDD	AK19
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VDD	AK21
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VDD	AK27
VDD	AK28

Ball Name	Ball #
VDD	AK29
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VDD	AK33
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VDD	AK35
VDD	AK36
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VDD	AK40
VDD	AL13
VDD	AL40
VDD	AM13
VDD	AM14
VDD	AM15
VDD	AM16
VDD	AM17
VDD	AM18
VDD	AM19
VDD	AM20
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VDD	AM37
VDD	AM38
VDD	AM39
VDD	AM40
VDD	AN13
VDD	AN40
VDD	AP13
VDD	AP14
VDD	AP15
VDD	AP16

Ball Name	Ball #
VDD	AP17
VDD	AP18
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VDD	AT34

Ball Name	Ball #
VDD	AT35
VDD	AT36
VDD	AT37
VDD	AT38
VDD	AT39
VDD	AT40
VDD	AT42
VDD	AU13
VDD	AU40
VDD	AU43
VDD	AV13
VDD	AV14
VDD	AV15
VDD	AV16
VDD	AV17
VDD	AV18
VDD	AV19
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VDD	AV44
VDD	AW13
VDD	AW40
VDD	AW42
VDD	AW43
VDD	AW44
VDD	AW45
VDD	AY13

Ball Name	Ball #
VDD	AY14
VDD	AY15
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VDD	AY18
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VDD	AY45
VDD	BA43
VDD	BA44
VDD	BA45
VDD	BA46
VDD	BA47
VDD	BB38
VDD	BB39
VDD	BB45
VDD	BB46
VDD	BB47
VDD	BB48
VDD	BC38
VDD	BC39
VDD	BC40
VDD	BC41
VDD	BC45
VDD	BC47
VDD	BC49
VDD	BD39

Ball Name	Ball #
VDD	BD41
VDD	BD46
VDD	BD47
VDD	BD48
VDD	BD49
VDD	BD50
VDD	BD51
VDD	BE41
VDD	BE42
VDD	BE43
VDD	BE46
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VDD	BE48
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VDD	BG43
VDD	BG44
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VDD	BG52
VDD	BH44
VDD	BH45
VDD	BH47
VDD	BH48
VDD	BH49
VDD	BH50
VDD	BH51
VDD	BH52
VDD	BJ44
VDD	BJ45
VDD	BJ46
VDD	BJ47
VDD	BJ48
VDD	BJ49
VDD	BJ50

Ball Name	Ball #
VDD	BJ51
VDD	BJ52
VDD	BK47
VDD	BK48
VDD	BK49
VDD	BK50
VDD	BK51
VDD	BK52
VDD	BL46
VDD	BL47
VDD	BL48
VDD	BL49
VDD	BL50
VDD	BL51
VDD	BL52
VDD	BM47
VDD	BM48
VDD	BM49
VDD	BM50
VDD	BM51
VDD	N13
VDD	N14
VDD	N15
VDD	N16
VDD	N17
VDD	N18
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VDD	N33
VDD	N34
VDD	N35
VDD	N36
VDD	N37
VDD	N38
VDD	N39
VDD	N40

Ball Name	Ball #
VDD	P13
VDD	P40
VDD	R13
VDD	R14
VDD	R15
VDD	R16
VDD	R17
VDD	R18
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VDD	R20
VDD	R21
VDD	R22
VDD	R23
VDD	R24
VDD	R25
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VDD	R28
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VDD	R30
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VDD	R34
VDD	R35
VDD	R36
VDD	R37
VDD	R38
VDD	R39
VDD	R40
VDD	T13
VDD	T40
VDD	U13
VDD	U14
VDD	U15
VDD	U16

Ball Name	Ball #
VDD	U17
VDD	U18
VDD	U19
VDD	U20
VDD	U21
VDD	U22
VDD	U23
VDD	U24
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VDD	U27
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VDD	U29
VDD	U30
VDD	U31
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VDD	U33
VDD	U34
VDD	U35
VDD	U36
VDD	U37
VDD	U38
VDD	U39
VDD	U40
VDD	V13
VDD	V40
VDD	W13
VDD	W14
VDD	W15
VDD	W16
VDD	W17
VDD	W18
VDD	W19
VDD	W20
VDD	W21
VDD	W22

Ball Name	Ball #
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VDD	W29
VDD	W30
VDD	W31
VDD	W32
VDD	W33
VDD	W34
VDD	W35
VDD	W36
VDD	W37
VDD	W38
VDD	W39
VDD	W40
VDD	Y13
VDD	Y40
VDD_SENSE	BK45
VID_PLLVDD	BC12
XSN_PLLVDD	BB24
XTAL_IN	BL6
XTAL_OUT	BM6
XTAL_OUTBUFF	BK6

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52		
1	A		GND	GND	FBC_D5	FBC_DQM0	FBC_D2		FBC_D13	FBC_CMD34		FBC_CMD2	FBC_CMD4		FBC_CMD9	FBC_CMD11		FBC_CMD32	FBC_CMD31		FBC_CMD26	FBC_CMD24		FBC_CMD19	FBC_CMD17		GND	FBC_D46		GND	FBC_D37		GND	FBB_D2		FBB_CMD1	FBB_CMD3		FBB_CMD8	FBB_CMD10		FBB_CMD15	FBB_CMD33		FBB_CMD27	FBB_CMD25		FBB_CMD20	FBB_CMD18	FBB_CMD17	GND	GND		A	1
2	B	GND	GND	FBC_D6	FBC_D4	GND	FBC_D3	GND	FBC_D12	FBC_D11	GND	FBC_CMD1	FBC_CMD5	GND	FBC_CMD8	FBC_CMD12	GND	FBC_CMD15	FBC_CMD30	GND	FBC_CMD27	FBC_CMD23	GND	FBC_CMD20	FBC_CMD16	GND	FBC_D62	FBC_D45	GND	FBC_DQS_WP5	FBC_D36	GND	FBB_D3	FBB_DQS_WP0	GND	FBB_CMD0	FBB_CMD4	GND	FBB_CMD7	FBB_CMD11	GND	FBB_CMD14	FBB_CMD31	GND	FBB_CMD28	FBB_CMD24	GND	FBB_CMD21	GND	FBB_CMD16	FBB_CMD35	GND	GND	B	2
3	C	GND	FBD_D39	FBD_D38	FBC_D7	GND	FBC_D0		FBC_DQM1	FBC_D9		FBC_CMD0	FBC_CMD6		FBC_CMD7	FBC_CMD13		FBC_CMD14	FBC_CMD29		FBC_CMD28	FBC_CMD22		FBC_CMD21	FBC_CMD35		FBC_D63	FBC_D44		GND	FBC_D39		FBB_DQM0	GND		FBB_CMD34	FBB_CMD5		FBB_CMD6	FBB_CMD12		FBB_CMD13	FBB_CMD30		FBB_CMD29	FBB_CMD23		FBB_CMD22	FBB_D50	FBB_D51	FBB_D49	GND	GND	C	3
4	D	FBD_D37	FBD_D36	FBD_DQM4	GND	FBC_DQS_WP0	FBC_D1	GND	FBC_DQS_WP1	FBC_D8	GND	FBC_CMD3	GND	GND	FBC_CMD10	FBC_D20	GND	FBC_CMD33	FBC_D49	GND	FBC_CMD25	FBC_D54	GND	FBC_CMD18	GND	GND	FBC_D61	FBC_D40	GND	FBC_DQM4	GND	GND	FBB_D1	FBB_D13	GND	FBB_CMD2	FBB_D30	GND	FBB_CMD9	FBB_D27	GND	FBB_CMD32	FBB_D20	GND	FBB_CMD26	FBB_D17	GND	FBB_CMD19	FBB_D48	GND	FBB_DQM6	FBB_DQS_WP6	FBB_D57	D	4
5	E	FBD_D33	GND	FBD_DQS_WP4	GND	GND	FBC_D15		GND	FBC_D10		FBC_D31	FBC_DQS_WP3		FBC_D26	FBC_D21		FBC_DQS_WP2	FBC_D18		FBC_D51	FBC_D53		FBC_D55	FBC_DQS_WP7		FBC_DQM7	FBC_DQM5		FBC_WCKB45	FBC_DQS_WP4		FBB_D4	FBB_DQM1		FBB_DQS_WP1	FBB_D31		FBB_D29	FBB_D26		FBB_D24	FBB_D21		FBB_DQM2	FBB_D16		FBB_CLK1_N	GND	FBB_D52	FBB_D53	GND	FBVDDQ_SENSE	E	5
6	F	FBD_D44	FBD_D45	FBD_D34	FBD_D32	FBD_D35	FBC_D14	GND	FBC_WCK01	FBC_WCKB01_N	GND	FBC_D30	FBC_DQM3	GND	FBC_D27	FBC_CLK0_N	GND	GND	FBC_D16	GND	FBC_DQM6	GND	GND	FBC_D52	FBC_D58	GND	FBC_D60	FBC_D42	GND	FBC_WCKB45_N	FBC_D33	GND	FBB_D7	FBB_D12	GND	GND	FBB_D11	GND	FBB_D28	FBB_D25	GND	FBB_WCKB23	FBB_D22	GND	GND	FBB_D18	GND	FBB_CLK1	FBB_D55	FBB_D54	FBB_D56	FBB_DQS_WP7	GND	F	6
7	G		GND		GND		GND		FBC_WCK01_N	FBC_WCKB01		FBC_D29	FBC_WCK23_N		FBC_WCKB23	FBC_CLK0		FBC_D22	FBC_D17		FBC_D50	FBC_DQS_WP6		FBC_WCK67	FBC_D56		FBC_D59	FBC_D43		FBC_D47	FBC_D35		FBB_D5	FBB_D15		FBB_WCKB01	FBB_D9		GND	FBB_DQM3		FBB_WCKB23_N	FBB_CLK0_N		FBB_DQS_WP2	FBB_D19		GND		GND		GND		G	7
8	H	GND	FBD_DQS_WP5	FBD_DQM5	FBD_D46	FBD_D47	FBD_WCKB45_N	FBD_WCKB45			GND	FBC_D28	FBC_WCK23	GND	FBC_WCKB23_N	FBC_D25	GND	FBC_D23	FBC_D19	GND	FBC_D48	FBC_CLK1	GND	FBC_WCK67_N	FBC_WCKB67	GND	FBC_D57	FBC_WCK45_N	GND	FBC_D34	FBC_D38	GND	FBB_D0	FBB_WCK01_N	GND	FBB_WCKB01_N	FBB_D8	GND	FBB_DQS_WP3	FBB_WCK23_N	GND	FBB_D23	FBB_CLK0	GND			FBB_WCK67_N	FBB_WCK67	FBB_D59	FBB_D62	FBB_DQM7	FBB_D60	FBB_D63	H	8
9	J	GND	FBD_D43	FBD_CMD35	FBD_D41	FBD_D40	FBD_WCK45	FBD_WCK45_N					GND		FBC_DBG_RFU1	FBC_D24		GND	FBC_DQM2		GND	FBC_CLK1_N		FBC_DBG_RFU2	FBC_WCKB67_N		FBC_D41	FBC_WCK45		FBC_D32	FBB_D6		FBB_D14	FBB_WCK01		FBB_DBG_RFU1	FBB_D10		GND	FBB_WCK23		FBB_DBG_RFU2					FBB_WCKB67_N	FBB_WCKB67	FBB_DQS_WP5	GND	FBB_D58	FBB_D61	GND	J	9
10	K		GND		GND		GND		GND				FBVDDQ	GND	FBVDDQ	FBVDDQ	GND	FBVDDQ	FBVDDQ	GND	FBVDDQ	FBVDDQ	GND	FBVDDQ	FBVDDQ	GND	FBVDDQ	FBVDDQ	GND	FBVDDQ	FBVDDQ	GND	FBVDDQ	FBVDDQ	GND	FBVDDQ	FBVDDQ	GND	FBVDDQ	FBVDDQ	GND	FBVDDQ				GND		GND		GND		GND		K	10
11	L	FBD_CMD18	FBD_CMD17	FBD_CMD16	FBD_D62	FBD_D63	FBD_D61	FBD_D60	FBD_D42						FBVDDQ	FBVDDQ		FBC_PLL_AVDD	FBVDDQ		FBVDDQ	FBVDDQ		FBVDDQ	FBVDDQ		FBVDDQ	FBVDDQ		FB_REFPLL_AVDD1	FBVDDQ		FBVDDQ	FBVDDQ		FBVDDQ	FBVDDQ		FBB_PLL_AVDD	FBVDDQ						FBB_WCK45_N	FBB_WCK45	FBB_D45	FBB_DQM5	FBB_D43	FBB_D40	FBB_D41	FBB_D42	L	11
12	M	FBD_CMD20	FBD_CMD21	FBD_CMD22	FBD_CMD19	FBD_DQS_WP7	GND	FBD_WCKB67	FBD_WCKB67_N	FBD_DQM7	FBVDDQ																																	FBVDDQ	FBB_WCKB45	FBB_WCKB45_N	FBB_D44	FBB_D47	FBB_D46	FBB_D35	FBB_D32	FBB_D34	GND	M	12
13	N		GND		GND		GND		GND		GND			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD			GND		GND		GND		GND		GND		N	13
14	P	FBD_CMD25	FBD_CMD24	FBD_CMD23	FBD_D58	FBD_D59	FBD_D56	FBD_WCK67_N	FBD_WCK67	FBD_DBG_RFU2	FBVDDQ	FBVDDQ		VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD		FBVDDQ	FBVDDQ	FB_CAL_PU_GND	FB_VREF	FBB_D39	FBB_D36	FBB_D33	FBB_DQM4	FBB_DQS_WP4	GND	FBB_D37	P	14
15	R	FBD_CMD27	FBD_CMD28	FBD_CMD29	FBD_CMD26	FBD_D53	FBD_D54	FBD_CLK1_N	FBD_CLK1	FBD_D57	FBVDDQ	FBVDDQ		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		FBVDDQ	FBVDDQ	FB_CAL_PD_VDDQ	FB_CAL_TERM_GND	FBB_D38	FBA_D6	FBA_DQS_WP0	GND	FBA_D5	FBA_D4	GND	R	15
16	T		GND		GND		GND		GND		GND			VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD			GND		GND		GND		GND		GND		T	16
17	U	FBD_CMD33	FBD_CMD31	FBD_CMD30	FBD_D52	FBD_DQM6	FBD_DQS_WP6	GND	FBD_D55	GND	FBVDDQ	FBVDDQ		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		GPCPLL_AVDD0	FBVDDQ	FBA_WCK01_N	FBA_WCK01	FBA_D7	FBA_DQM0	FBA_D1	FBA_D3	FBA_D2	FBA_D0	FBA_D14	U	17
18	V	FBD_CMD15	FBD_CMD14	FBD_CMD13	FBD_CMD32	FBD_D18	FBD_D50	FBD_D48	FBD_D49	FBD_D51	FBVDDQ	FBD_PLL_AVDD		VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD		FBVDDQ	FBVDDQ	FBA_WCKB01_N	FBA_WCKB01	FBA_D8	FBA_D13	FBA_DQS_WP1	GND	FBA_D12	FBA_D15	GND	V	18
19	W		GND		GND		GND		GND		GND			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD			GND		GND		GND		GND		GND		W	19
20	Y	FBD_CMD10	FBD_CMD11	FBD_CMD12	FBD_D19	FBD_D17	FBD_D16	FBD_CLK0_N	FBD_CLK0	GND	FBVDDQ	FBVDDQ		VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD		FBVDDQ	FBVDDQ	FBA_D31	FBA_D9	FBA_D11	FBA_D10	FBA_DQM1	FBA_CMD2	FBA_CMD34	FBA_CMD0	FBA_CMD1	Y	20
21	AA	FBD_CMD8	FBD_CMD7	FBD_CMD6	FBD_CMD9	FBD_D21	FBD_D20	FBD_DQM2	GND	FBD_DQS_WP2	FBVDDQ	FBVDDQ		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		FBVDDQ	FBVDDQ	FBA_DBG_RFU1	FBA_D30	FBA_D29	FBA_D28	FBA_DQS_WP3	GND	FBA_CMD5	FBA_CMD4	FBA_CMD3	AA	21
22	AB		GND		GND		GND		GND		GND			VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD			GND		GND		GND		GND		GND		AB	22
23	AC	FBD_CMD3	FBD_CMD4	FBD_CMD5	FBD_D23	FBD_D22	FBD_D25	FBD_WCKB23	FBD_WCKB23_N	FBD_DBG_RFU1	FBVDDQ	FBVDDQ		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		FBVDDQ	FBVDDQ	FBA_WCK23_N	FBA_WCK23	FBA_D26	FBA_D27	FBA_DQM3	FBA_CMD9	FBA_CMD6	FBA_CMD7	FBA_CMD8	AC	23
24	AD	FBD_CMD1	FBD_CMD0	FBD_CMD34	FBD_CMD2	FBD_DQM3	FBD_D27	FBD_D24	FBD_WCK23	FBD_WCK23_N	FBVDDQ	FBVDDQ		VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD		FBVDDQ	FBVDDQ	GND	FBA_WCKB23_N	FBA_WCKB23	FBA_D23	FBA_D25	FBA_D24	FBA_CMD12	FBA_CMD11	FBA_CMD10	AD	24
25	AE		GND		GND		GND		GND		GND			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD			GND		GND		GND		GND		GND		AE	25
26	AF	GND	FBD_D30	FBD_D31	FBD_DQS_WP3	GND	FBD_D26	FBD_D28	FBD_D29	FBD_D9	FBVDDQ	GPCPLL_AVDD1		VDD	VDD	VDD	VDD	VDD	VDD	GND	GND	GND	GND	GND	VDD	VDD	VDD	GND	GND	GND	VDD	VDD	VDD	VDD	VDD	GND	GND	GND	GND	GND	VDD		FB_REFPLL_AVDD0	FBVDDQ	FBA_DQS_WP2	GND	FBA_D20	FBA_D21	FBA_D22	FBA_CMD32	FBA_CMD13	FBA_CMD14	FBA_CMD15	AF	26
27	AG	FBD_DQM1	FBD_DQS_WP1	GND	FBD_D8	FBD_D15	FBD_D10	FBD_D11	FBD_WCKB01	FBD_WCKB01_N	FBVDDQ	FBVDDQ		VDD	GND	GND	GND	GND	GND	VDD	VDD	VDD	VDD	VDD	GND	GND	GND	VDD	VDD	VDD	GND	GND	GND	GND	GND	VDD	VDD	VDD	VDD	VDD	VDD		FBVDDQ	FBVDDQ	GND	FBA_CLK0	FBA_CLK0_N	FBA_DQM2	FBA_D17	FBA_D19	FBA_CMD30	FBA_CMD31	FBA_CMD33	AG	27
28	AH		GND		GND		GND		GND		GND			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD			GND		GND		GND		GND		GND		AH	28
29	AJ	FBD_DQM0	GND	FBD_DQS_WP0	FBD_D12	FBD_D13	FBD_D14	FBD_WCK01_N	FBD_WCK01	GND	FBVDDQ	FBVDDQ		VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD		FBVDDQ	FBVDDQ	FBA_D16	FBA_D18	FBA_D49	FBA_D50	FBA_D48	FBA_CMD26	FBA_CMD29	FBA_CMD28	FBA_CMD27	AJ	29
30	AK	GND	FBD_D2	FBD_D3	FBD_D1	FBD_D4	FBD_D5	FBD_D7	FBD_D0	FBD_D6	FBVDDQ	FBVDDQ		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		FBVDDQ	FBVDDQ	GND	FBA_CLK1_N	FBA_CLK1	GND	FBA_DQS_WP6	FBA_D51	FBA_CMD23	FBA_CMD24	FBA_CMD25	AK	30
31	AL		GND		GND		GND		GND		GND			VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD			GND		GND		GND		GND		GND		AL	31
32	AM	NVHS0_RX0	EXT_REFCLK_SLI	NVHS_TERMP	GND	NVHS_REFCLK_N	NVHS_REFCLK	NVHS0_TX0	NVHS0_TX0_N	GND	NVHS_HVDD	NVHS_HVDD		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		FBVDDQ	FBVDDQ	FBA_D56	FBA_D57	FBA_D53	FBA_D52	FBA_DQM6	FBA_CMD19	FBA_CMD22	FBA_CMD21	FBA_CMD20	AM	32
33	AN	NVHS0_RX0_N	NVHS0_RX1	NVHS0_RX1_N	GND	GND	NVHS0_TX1_N	NVHS0_TX1	GND	NVHS_PLL_HVDD	NVHS_HVDD	NVHS_HVDD		VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD		FBA_PLL_AVDD	FBVDDQ	FBA_DBG_RFU2	FBA_D58	FBA_D59	FBA_D61	FBA_D54	FBA_D55	FBA_CMD16	FBA_CMD17	FBA_CMD18	AN	33
34	AP		GND		GND		GND		GND		GND			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD			GND		GND		GND		GND		GND		AP	34
35	AR	NVHS0_RX3	NVHS0_RX2_N	NVHS0_RX2	GND	NVHS0_TX2_N	NVHS0_TX2	NVHS0_TX3	NVHS0_TX3_N	GND	NVHS_CVDD	NVHS_HVDD		VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD		FBVDDQ	FBVDDQ	FBA_WCK67_N	FBA_WCK67	FBA_D63	FBA_D62	FBA_D60	FBA_DQM7	FBA_CMD35	FBA_DQS_WP7	GND	AR	35
36	AT	NVHS0_RX3_N	NVHS0_RX4	NVHS0_RX4_N	GND	GND	NVHS0_TX4_N	NVHS0_TX4	GND	NVHS_DVDD	NVHS_DVDD	NVHS_CVDD		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		VDD	FBVDDQ	FBA_WCKB67_N	FBA_WCKB67	FBA_D44	FBA_D42	FBA_D43	FBA_D41	FBA_DQS_WP5	GND	GND	AT	36
37	AU		GND		GND		GND		GND		GND			VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD			VDD		GND		GND		GND		GND		AU	37
38	AV	NVHS0_RX6	NVHS0_RX5_N	NVHS0_RX5	GND	NVHS0_TX5_N	NVHS0_TX5	NVHS0_TX6	NVHS0_TX6_N	GND	NVHS_DVDD	NVHS_DVDD		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		VDD	VDD	VDD	GND	FBA_WCK45_N	FBA_WCK45	FBA_D40	FBA_D47	FBA_DQM5	FBA_D45	FBA_D46	AV	38
39	AW	NVHS0_RX6_N	NVHS0_RX7	NVHS0_RX7_N	GND	GND	NVHS0_TX7_N	NVHS0_TX7	GND	USB_PLL_HVDD	USB_HVDD	USB_HVDD		VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD		VDD	VDD	VDD	VDD	GND	FBA_WCKB45_N	FBA_WCKB45	FBA_D39	FBA_D34	FBA_D32	GND	AW	39
40	AY		GND		GND		GND		GND		GND			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD			VDD		VDD		GND		GND		GND		AY	40
41	BA	USB_L0_N	USB_L0	GPIO29	GPIO27	GPIO21	USB_RBIAS	USB_L1_N	USB_L1	GND	1V8_AON																																	VDD	VDD	VDD	VDD	VDD	GND	FBA_D38	FBA_D36	FBA_D35	FBA_D33	BA	41
42	BB	GPIO13	GPIO25	GPIO30	GPIO28	GPIO1	GPIO22	USB_SDA	USB_SCL						1V8_AON	USB_DVDD		IFP_IOVDD	IFP_IOVDD		IFP_IOVDD	IFP_IOVDD		IFP_IOVDD	XSN_PLLVDD		PEX_HVDD	PEX_HVDD		PEX_HVDD	PEX_PLL_HVDD		PEX_HVDD	PEX_CVDD		PEX_DVDD	PEX_DVDD		VDD	VDD						VDD	VDD	VDD	VDD	GND	FBA_D37	FBA_DQM4	FBA_DQS_WP4	BB	42
43	BC		GND		GND		GND		GND				VID_PLLVDD	GND	1V8_AON	USB_DVDD	GND	IFP_IOVDD	IFP_IOVDD	GND	IFP_IOVDD	IFP_IOVDD	GND	IFP_IOVDD	GND	GND	PEX_HVDD	PEX_HVDD	GND	PEX_HVDD	PEX_HVDD	GND	PEX_HVDD	PEX_CVDD	GND	PEX_DVDD	PEX_DVDD	GND	VDD	VDD	VDD	VDD				VDD		VDD		VDD		GND		BC	43
44	BD	GPIO2	GPIO6	GPIO10	GPIO19	GPIO24	GPIO0	GPIO7					SP_PLLVDD		FP_FUSE_SRC	IFPE_PLLVDD		IFPE_RSET	IFPCD_PLLVDD		IFPCD_RSET	IFPAB_PLLVDD		IFPAB_RSET	NC		GND	PEX_HVDD		GND	PEX_HVDD		GND	PEX_DVDD		GND	PEX_DVDD		GND	VDD		VDD					VDD	VDD	VDD	VDD	VDD	VDD	GND	BD	44
45	BE	GPIO4	GPIO16	GPIO18	GPIO3	GPIO20	GPIO12	GPIO26			GND	IFPD_AUX_SCL	USB_VDDP	GND	IFPE_L2	GND	GND	IFPC_L3	GND	GND	IFPC_L0	GND	GND	IFPA_L1	GND	GND	PEX_TX1_N	GND	GND	PEX_TX4_N	GND	GND	PEX_TX7_N	GND	GND	PEX_TX10_N	GND	GND	PEX_TX13_N	GND	GND	VDD	VDD	VDD			VDD	VDD	VDD	VDD	VDD	VDD	VDD	BE	45
46	BF		GND		GND		GND		I2CB_SDA	BUFRST_N		IFPD_AUX_SDA_N	TS_VREF		IFPE_L2_N	IFPE_L1_N		IFPC_L3_N	IFPC_L2_N		IFPC_L0_N	IFPA_L3_N		IFPA_L1_N	IFPA_L0_N		PEX_TX1	PEX_TX2		PEX_TX4	PEX_TX5		PEX_TX7	PEX_TX8		PEX_TX10	PEX_TX11		PEX_TX13	PEX_TX14		GND	VDD		VDD	VDD		VDD		VDD		VDD		BF	46
47	BG	GPIO15	GPIO5	GPIO23	GPIO14	OVERT	USB_TERMP0	GND	I2CB_SCL	I2CC_SCL	GND	IFPA_AUX_SCL	IFPB_AUX_SDA_N	GND	IFPE_L3_N	IFPE_L1	GND	IFPE_L0_N	IFPC_L2	GND	IFPC_L1_N	IFPA_L3	GND	IFPA_L2_N	IFPA_L0	GND	PEX_TX0	PEX_TX2_N	GND	PEX_TX3	PEX_TX5_N	GND	PEX_TX6	PEX_TX8_N	GND	PEX_TX9	PEX_TX11_N	GND	PEX_TX12	PEX_TX14_N	GND	PEX_TX15_N	GND	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	BG	47
48	BH	GPIO17	GND	GPIO11	GPIO8	GND	USB_TERMP1		I2CS_SDA	I2CC_SDA		IFPA_AUX_SDA_N	IFPB_AUX_SCL		IFPE_L3	GND		IFPE_L0	GND		IFPC_L1	GND		IFPA_L2	GND		PEX_TX0_N	GND		PEX_TX3_N	GND		PEX_TX6_N	GND		PEX_TX9_N	GND		PEX_TX12_N	GND		PEX_TX15	GND		VDD	VDD		VDD	VDD	VDD	VDD	VDD	VDD	BH	48
49	BJ	THERMDN	THERMDP	GPIO9	ROM_CS_N	STRAP5	EXT_REFCLK_FL	GND	I2CS_SCL	ADC_IN	GND	ADC_IN_N	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	BJ	49
50	BK	GND	ROM_SI	ROM_SCLK	ROM_SO	STRAP4	XTAL_OUTBUFF		IFPE_AUX_SCL	IFPC_AUX_SCL		IFPF_L3_N	IFPF_L1		IFPF_L0_N	IFPD_L2		IFPD_L1_N	IFPB_L3		IFPB_L2_N	IFPB_L0		NVJTAG_SEL	JTAG_TCK		PEX_RST_N	PEX_RX0_N		PEX_RX1	PEX_RX3_N		PEX_RX4	PEX_RX6_N		PEX_RX7	PEX_RX9_N		PEX_RX10	PEX_RX12_N		PEX_RX13	PEX_RX15_N		PEX_WAKE_N	VDD_SENSE		VDD	VDD	VDD	VDD	VDD	VDD	BK	50
51	BL	GND	GND	STRAP0	STRAP1	GND	XTAL_IN	GND	IFPE_AUX_SDA_N	IFPC_AUX_SDA_N	GND	IFPF_L3	IFPF_L1_N	GND	IFPF_L0	IFPD_L2_N	GND	IFPD_L1	IFPB_L3_N	GND	IFPB_L2	IFPB_L0_N	GND	JTAG_TMS	JTAG_TRST_N	GND	PEX_CLKREQ_N	PEX_RX0	GND	PEX_RX1_N	PEX_RX3	GND	PEX_RX4_N	PEX_RX6	GND	PEX_RX7_N	PEX_RX9	GND	PEX_RX10_N	PEX_RX12	GND	PEX_RX13_N	PEX_RX15	GND	PEX_TERMP	GND_SENSE	VDD	VDD	VDD	VDD	VDD	VDD	VDD	BL	51
52	BM		GND	GND	STRAP2	STRAP3	XTAL_OUT		IFPF_AUX_SCL	IFPF_AUX_SDA_N		IFPF_L2_N	IFPF_L2		IFPD_L3_N	IFPD_L3		IFPD_L0_N	IFPD_L0		IFPB_L1_N	IFPB_L1		JTAG_TDI	JTAG_TDO		PEX_REFCLK	PEX_REFCLK_N		PEX_RX2	PEX_RX2_N		PEX_RX5	PEX_RX5_N		PEX_RX8	PEX_RX8_N		PEX_RX11	PEX_RX11_N		PEX_RX14	PEX_RX14_N		NC	NC		VDD	VDD	VDD	VDD	VDD		BM	52
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