

P654 - GT200/NVIO2

P654, GT200-100, 896MB/1792MB - GDDR3 BGA136 16M/32Mx32

DVI-I + DVI-I/DP + HD/SD/TVout, SPDIF, Dual SLI

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NO	VARIANT	NPIN	ASSEMBLY
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1	SKJ0000	600-10654-0001-000	DT: GT200-100, 55013501000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I + HDTV
2	SKJ0001	600-10654-0001-000	DT: GT200-100, 55013501000, 896MB - 16Mx32 GDDR3, DVI-I + DP + HDTV
3	SKJ0051	600-10654-0051-300	DT: GT200B-100, 57612421000, 896MB - 16Mx32 GDDR3, DVI-I + DP + DVI-I
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MS-V180 -0A
PAGE 21:VGS SLIM
PAGE-22 remove DACB HDTV Circuit
PAGE 24:DVI change HDMI
PAGE 25:DP modify DSDA/DSCL circuit
PAGE 28:ADD I2C0_SCL/SDA and GPIO 3 circuit,remove GPIO 12
PAGE 29:remove R112,R113 and GPIO8_FAN_TACH link to U21
PAGE 33:remove R671,R572
PAGE 35:remove RT8805CQVA change UPI6205 and UPI6262 circuit
PAGE 36:remove NCP5388MNR2G change UPI6208 circuit
PAGE 37/38 :remove NCP3418B change UPI6281 circuit
PAGE 39 :Add WL83L786G circuit

MS-V180 -10
1.PAGE 37,38 modify D15--D21 footprint
2..PAGE 37,38 add CAP

MS-V180 -20

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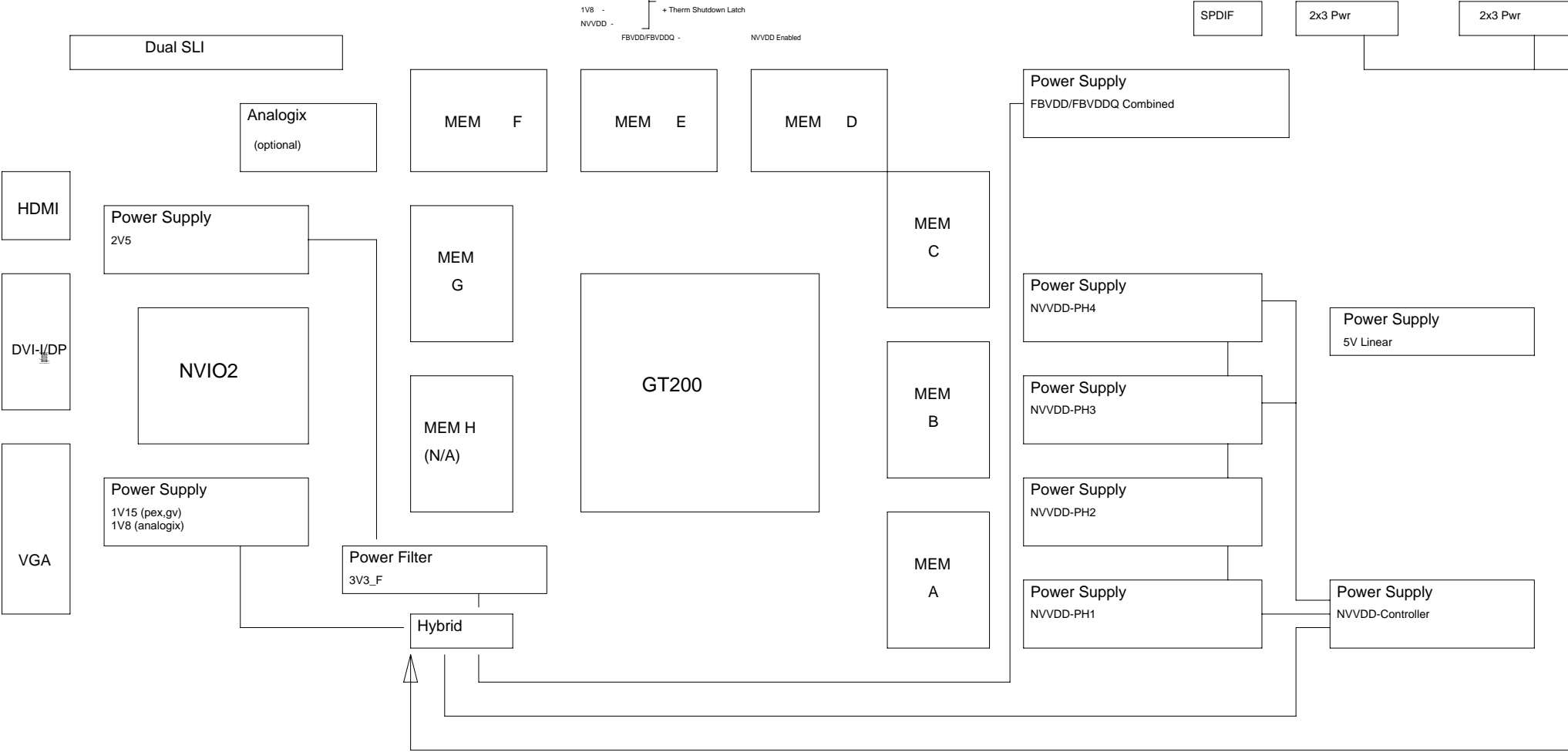
Block Diagram

Power Sequence

5V - Always On
3V3 - Always On
12V_F - Always On
12V_PEX6_F1 - Always On
12V_PEX6_F2 - Always On
3V3_DP - Always On


3V3_F -
2V5 -
1V15 -
1V8 -
NVVDD -
FBVDD/FBVDDQ -
NVVDD Enabled

Hybrid Enable
+ Input_PEX_Enable
+ Therm Shutdown Latch



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Block Diagram



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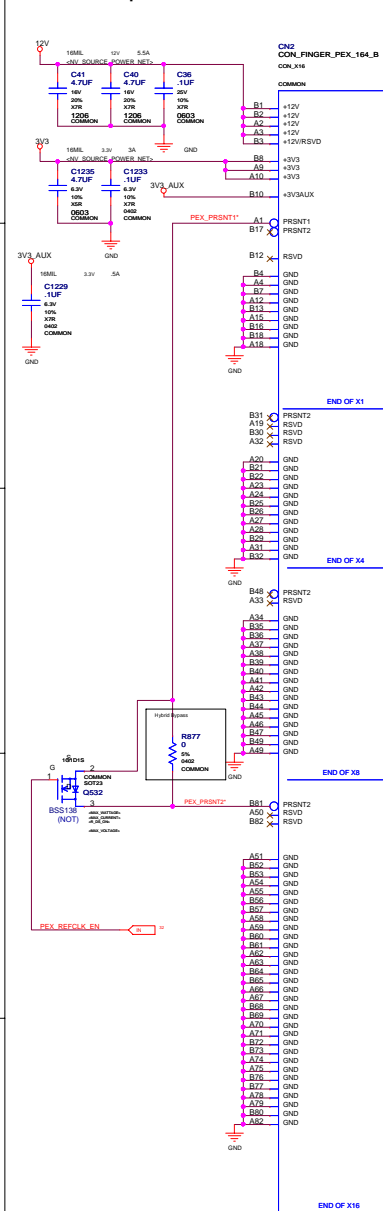
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PCI Express / JTAG

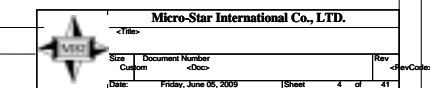
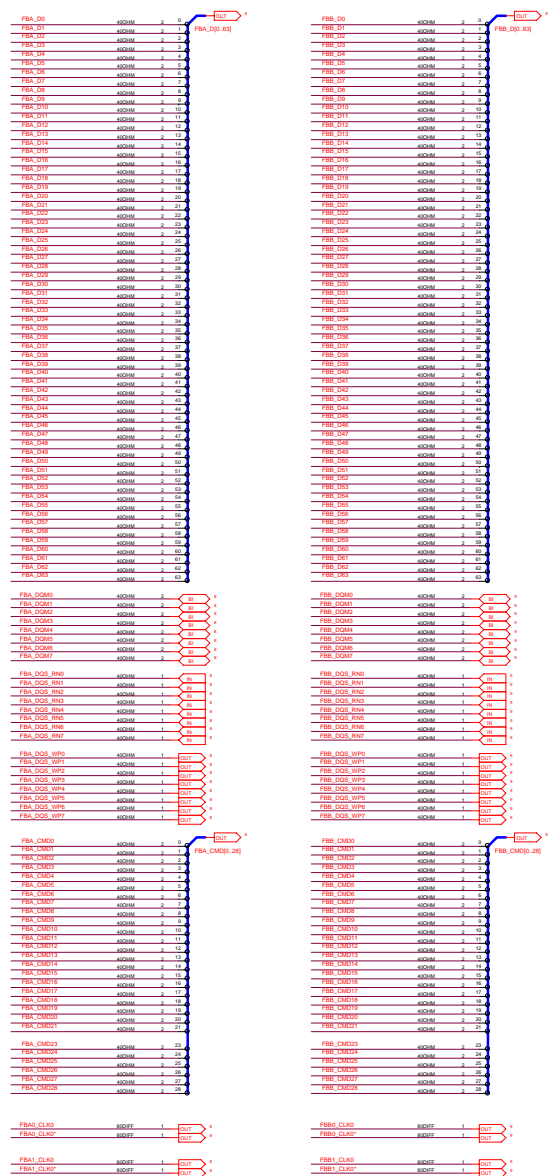
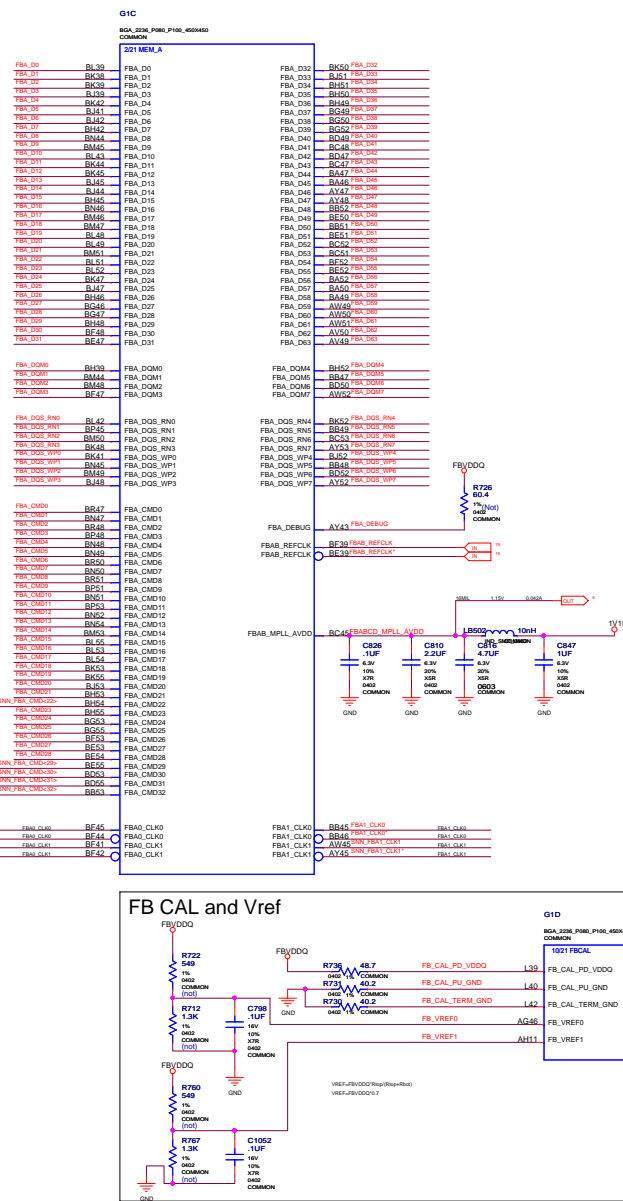


JTAG



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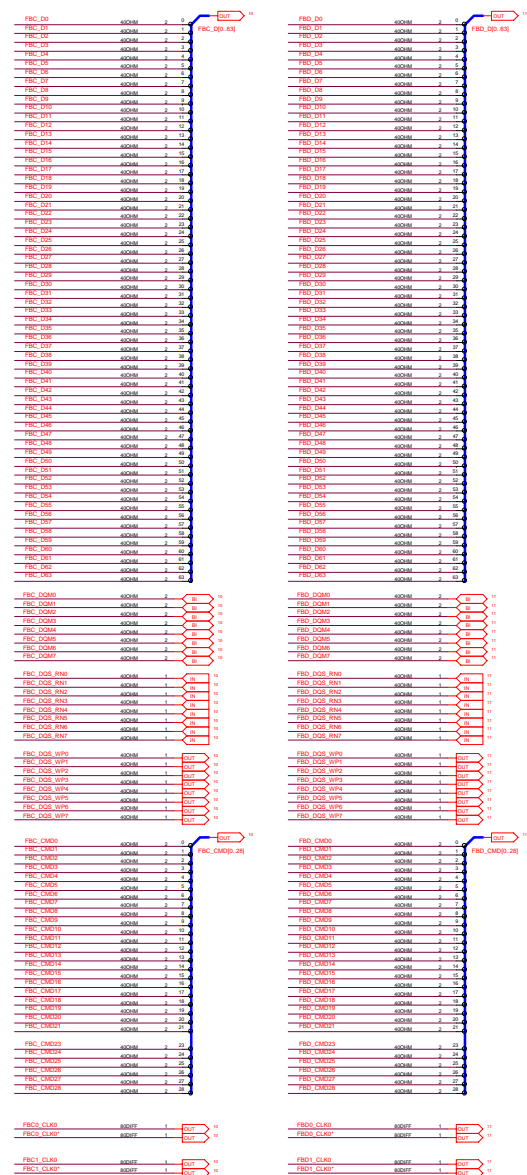
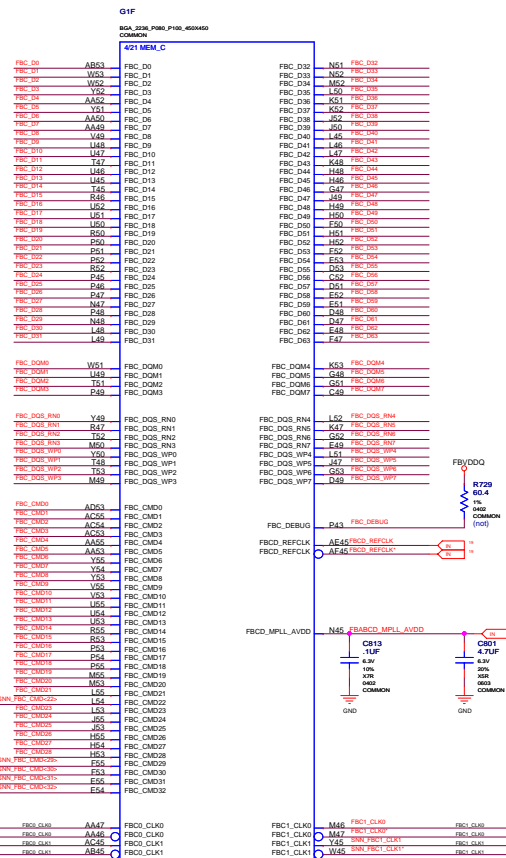
Framebuffer A,B: GPU Section + Calibration



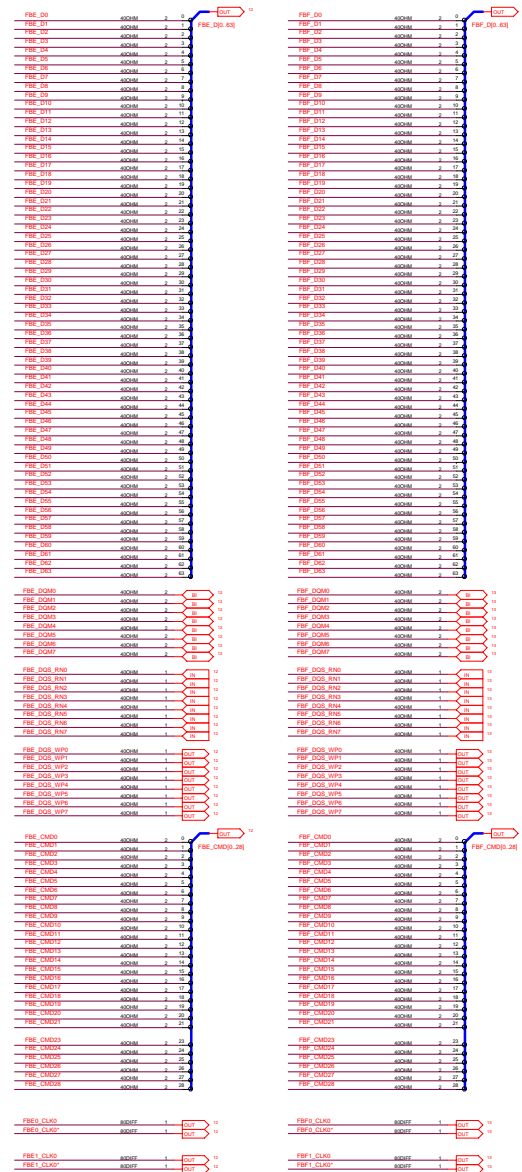
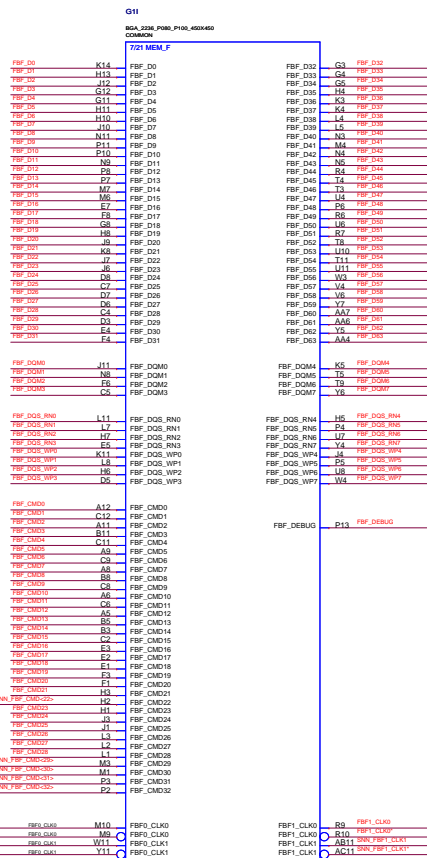
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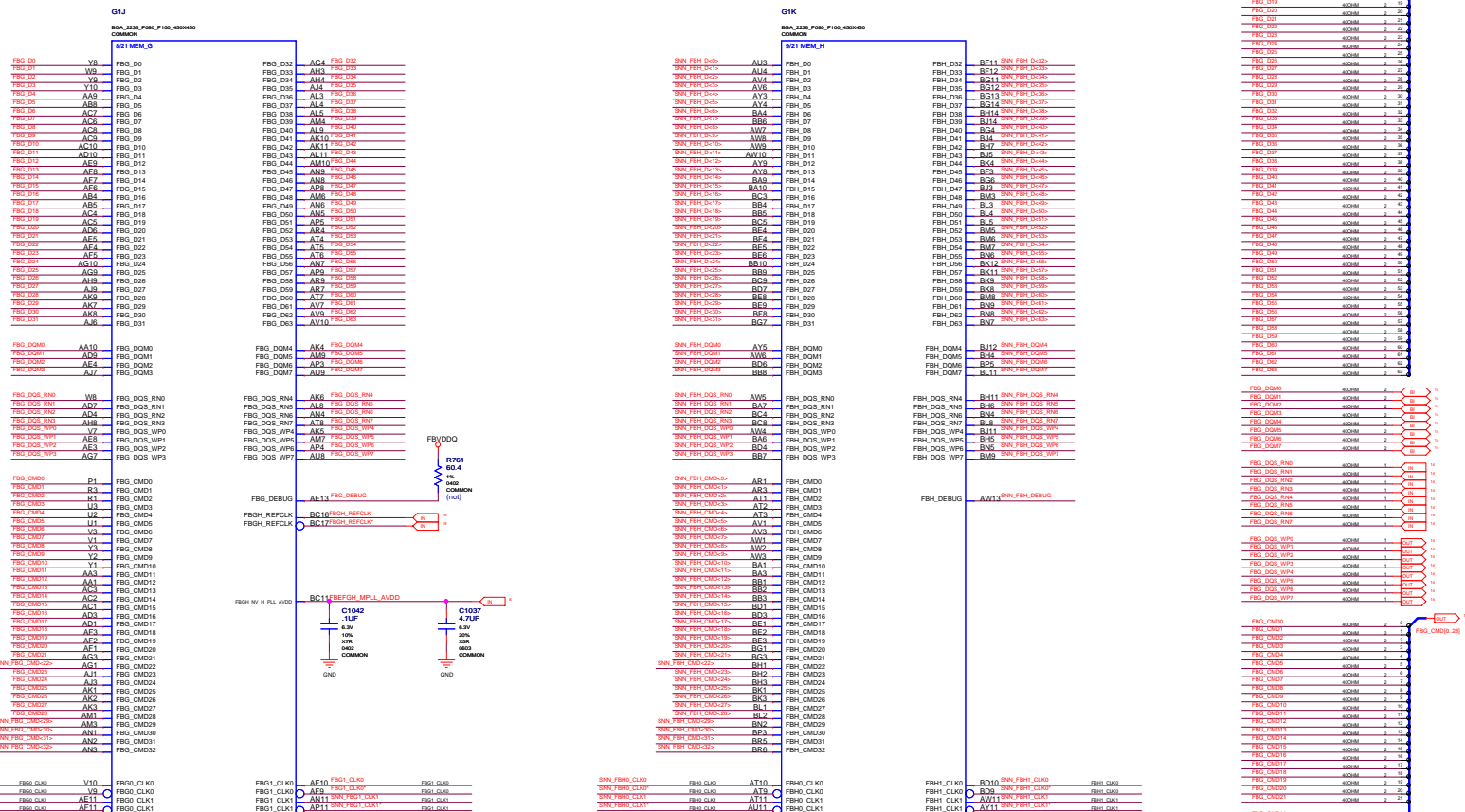
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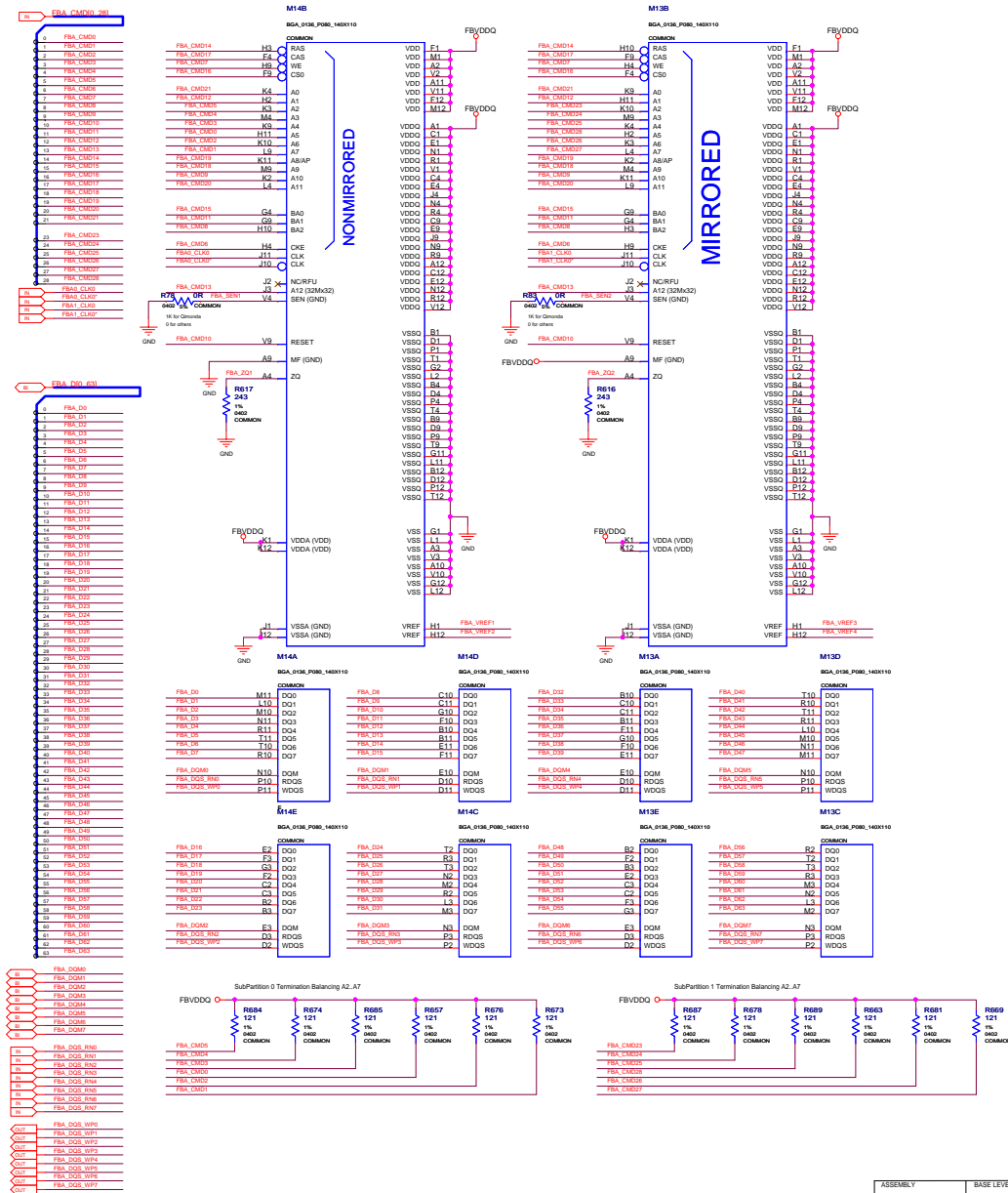
Framebuffer E,F: GPU Section



Framebuffer G,H: GPU Section



Framebuffer A: Memory Section



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Framebuffer A: Memory Section

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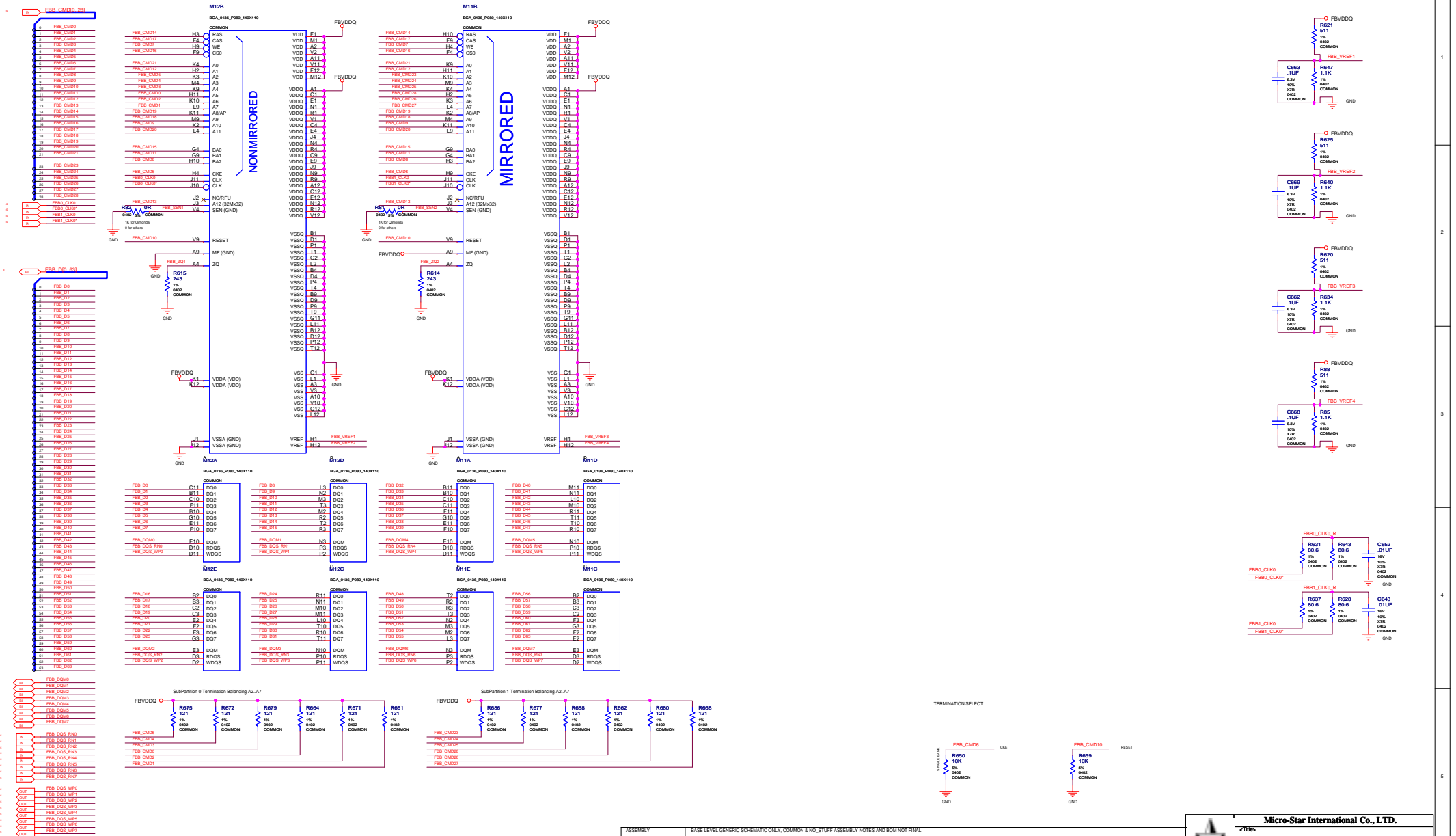


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Framebuffer B: Memory Section



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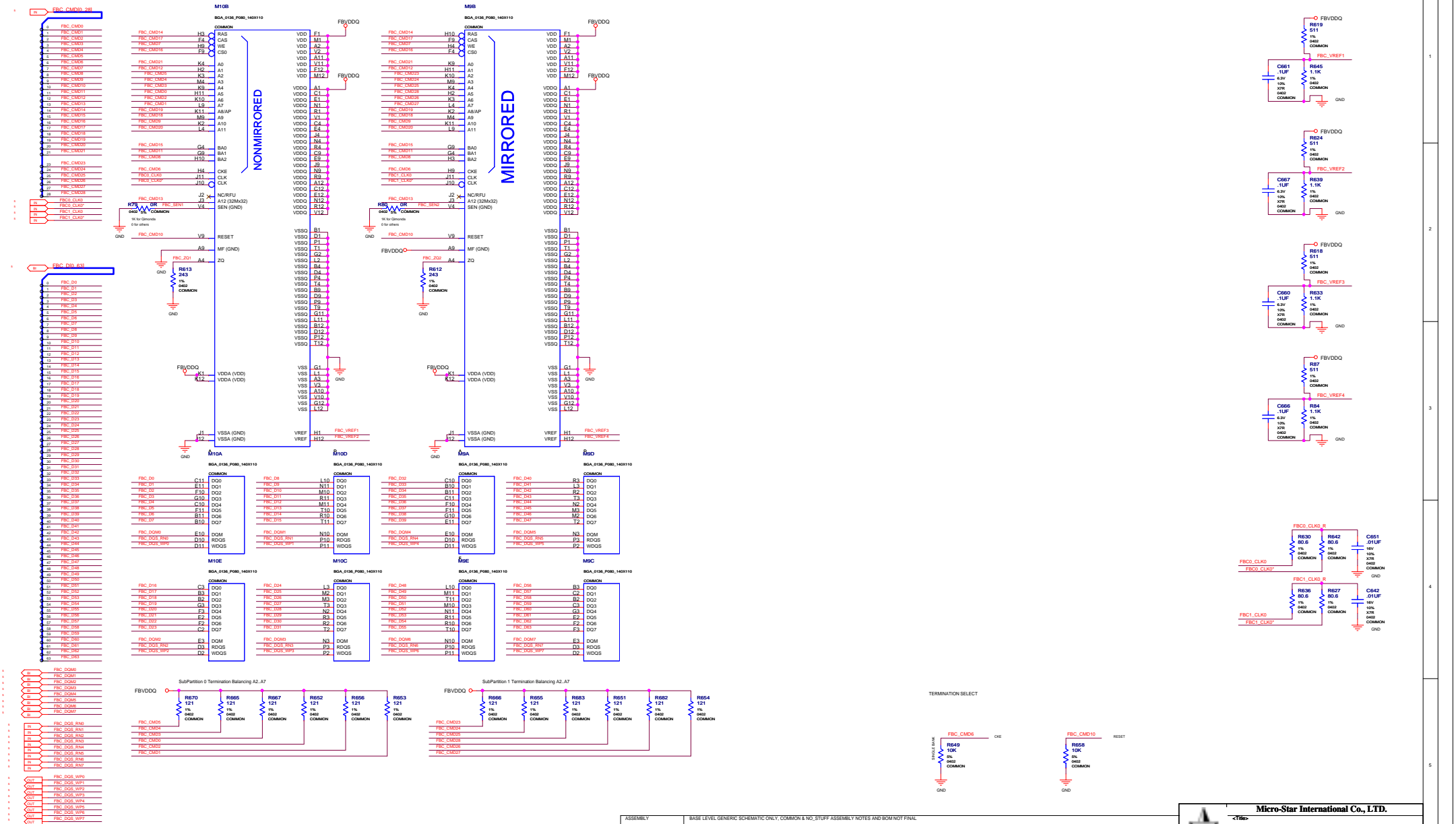
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Framebuffer C: Memory Section



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2. Kinetic Study of the Hydrolysis of Acetic Anhydride	Jane Smith	2017	Journal of Physical Chemistry	120	456-468
3. The Influence of Catalyst Concentration on Reaction Rate	Michael Brown	2019	Journal of Catalysis	320	789-801
4. Kinetic Analysis of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Sarah White	2016	Journal of Analytical Chemistry	85	234-246
5. The Effect of pH on the Rate of Enzymatic Reaction	David Green	2018	Journal of Biochemistry	150	567-579
6. Kinetic Study of the Reaction of Nitrogen Dioxide with Carbon Monoxide	Emily Black	2017	Journal of Environmental Chemistry	60	345-357
7. The Effect of Solvent Polarity on the Rate of Nucleophilic Substitution	Robert Grey	2019	Journal of Organic Chemistry	84	678-690
8. Kinetic Investigation of the Reaction Between Iodine and Sulfur Dioxide	Laura Pink	2016	Journal of Inorganic Chemistry	50	101-113
9. The Influence of Temperature on the Rate of Polymerization	James Blue	2018	Journal of Polymer Science	55	201-213
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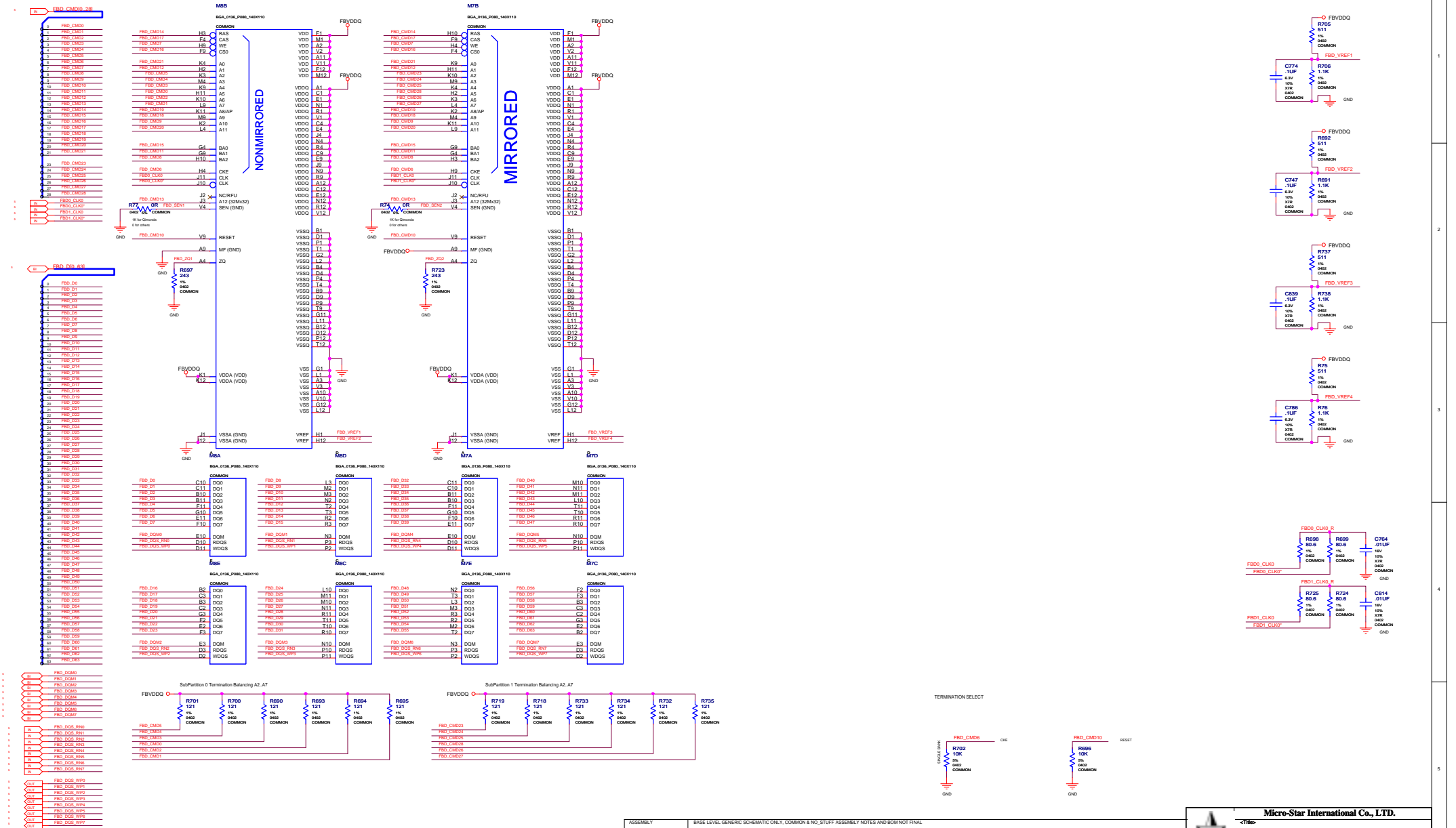
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Framebuffer D: Memory Section



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2. Kinetic Analysis of the Decomposition of Hydrogen Peroxide	Jane Smith	2017	Chemical Science	8	2101-2115
3. The Role of Catalysts in Accelerating Chemical Reactions	Michael Brown	2019	Journal of Catalysis	375	45-58
4. Kinetic Modeling of Enzyme Activity Under Varying Conditions	Sarah White	2016	Biophysical Journal	110	1001-1015
5. The Effect of pH on the Stability of Protein Enzymes	David Green	2015	Journal of Molecular Biology	525	100-115
6. Kinetic Studies of the Reaction Between Nitric Oxide and Ozone	Emily Black	2014	Journal of Physical Chemistry	118	12345-12355
7. The Kinetics of the Reaction Between Hydrogen and Chlorine	Robert Grey	2013	Journal of Chemical Physics	138	100001-100015
8. Kinetic Analysis of the Reaction Between Sulfur Dioxide and Hydrogen Sulfide	Olivia Blue	2012	Journal of Environmental Science	234	100-110
9. The Kinetics of the Reaction Between Carbon Monoxide and Oxygen	Thomas Yellow	2011	Journal of Chemical Thermodynamics	43	100-110
10. Kinetic Studies of the Reaction Between Nitrogen Dioxide and Carbon Monoxide	Alexander Purple	2010	Journal of Environmental Science	224	100-110

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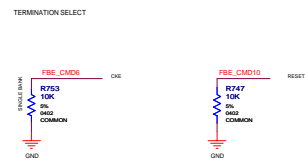
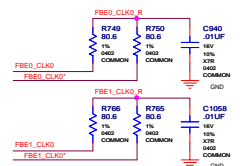
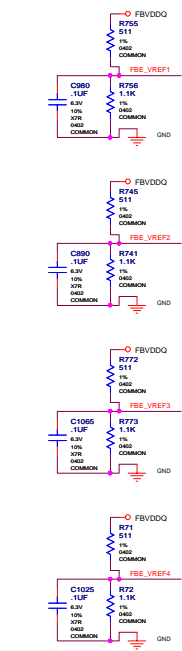
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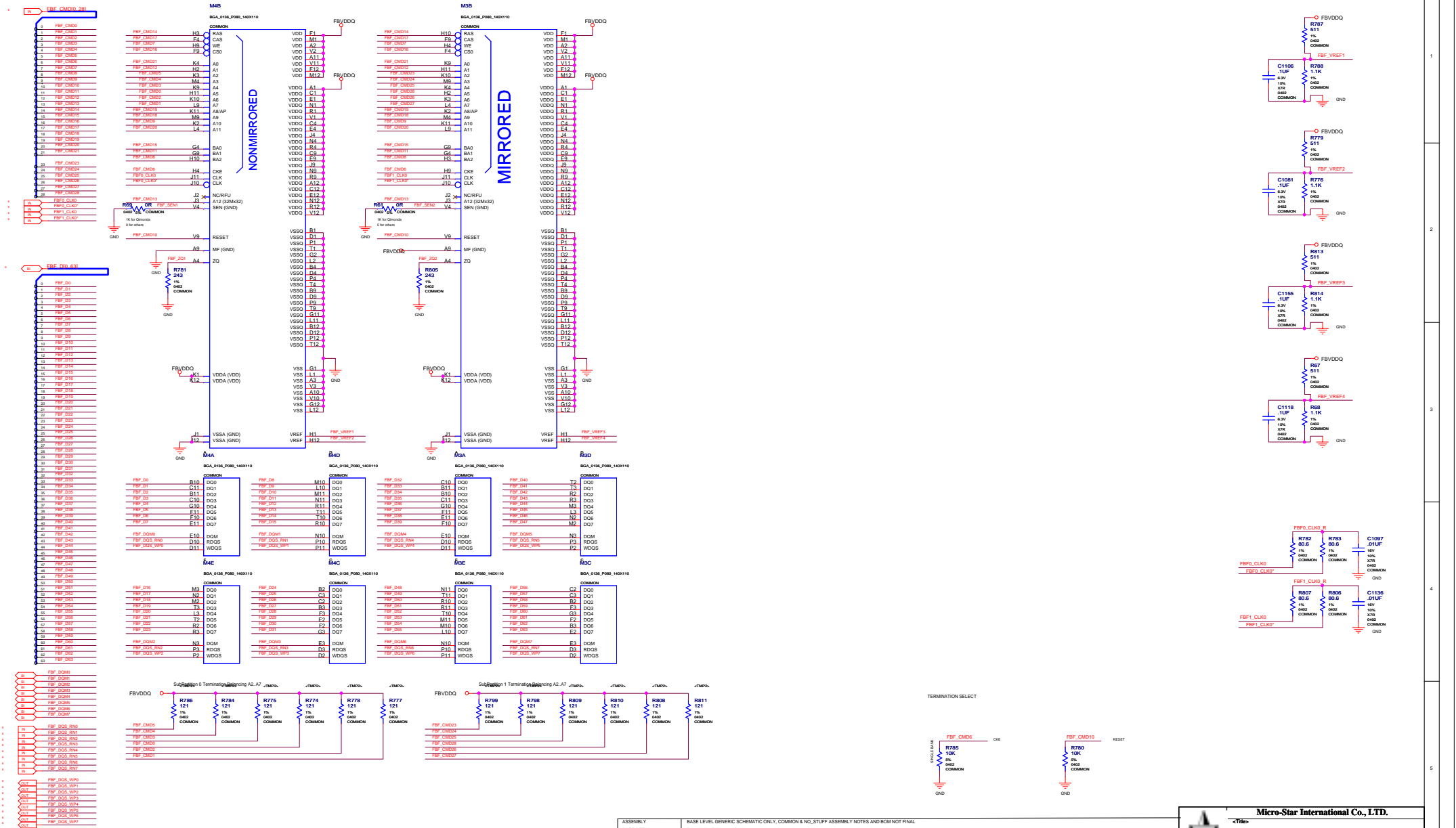
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Framebuffer F: Memory Section



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Framebuffer F: Memory Section

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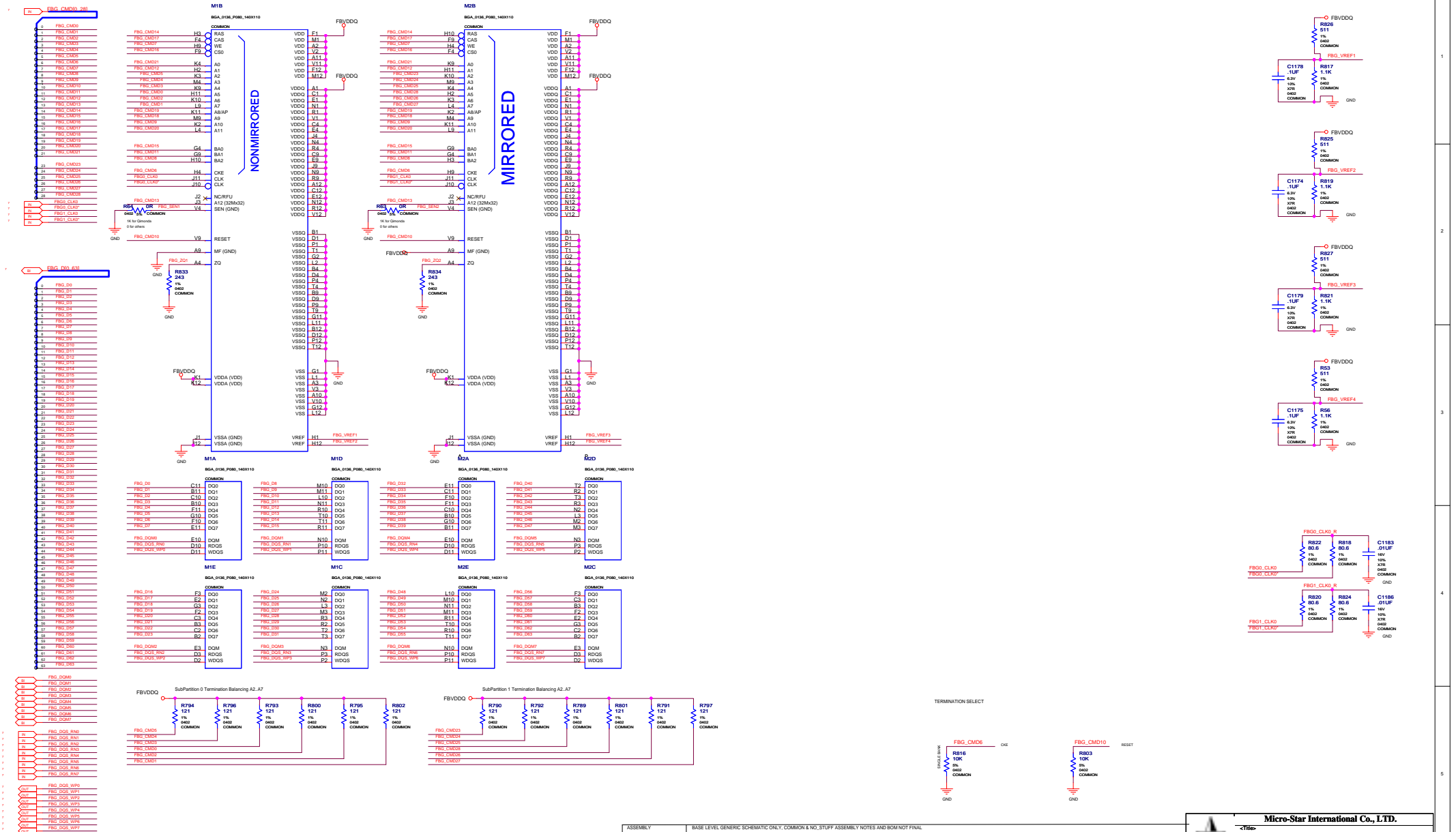
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Framebuffer G: Memory Section



Framebuffer H: N/A

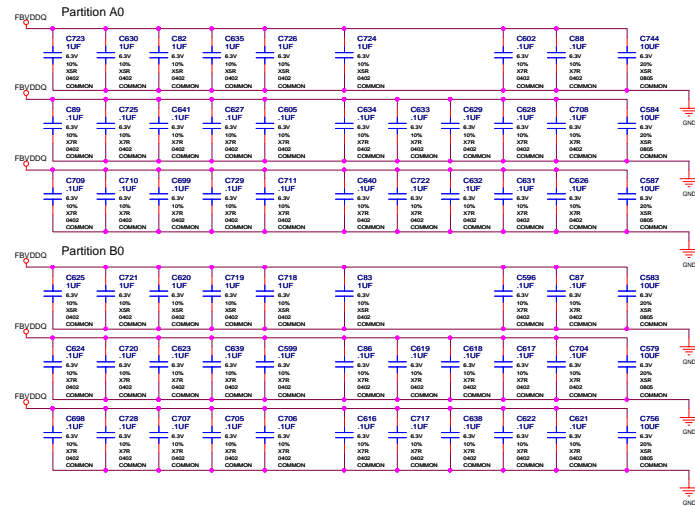
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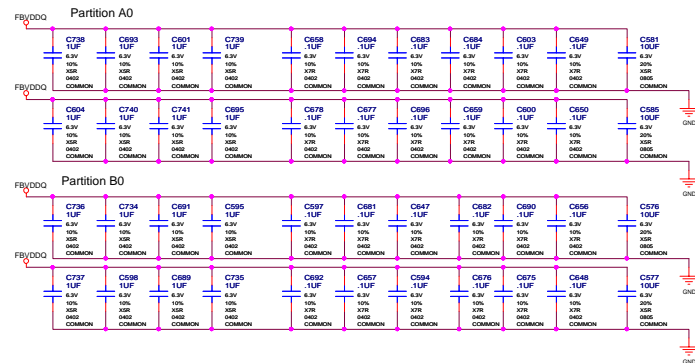
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Decoupling: Memory Section A-D

Decoupling for FBVDDQ

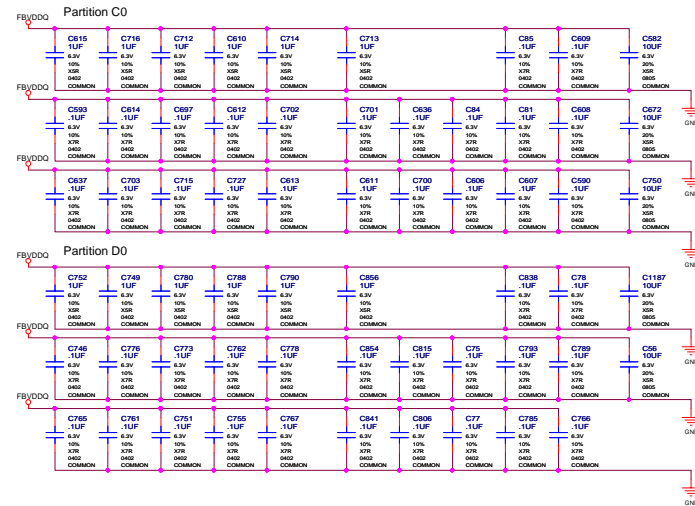


Decoupling for FBVDDQ



Banks A-D FBVDDQ
Combined Distributed Capacitance

280 uF



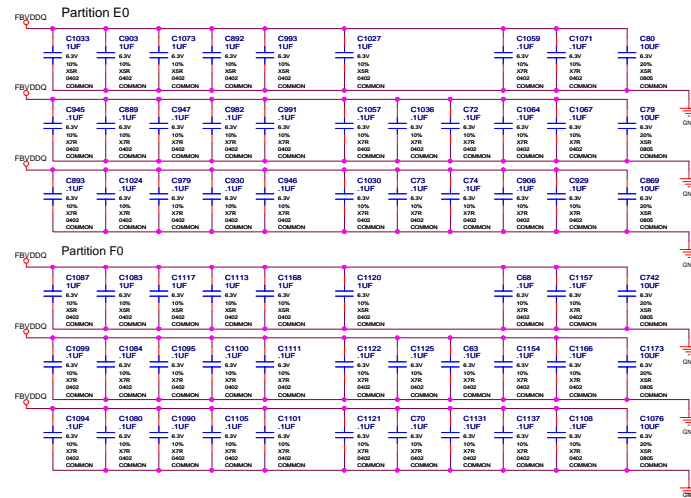
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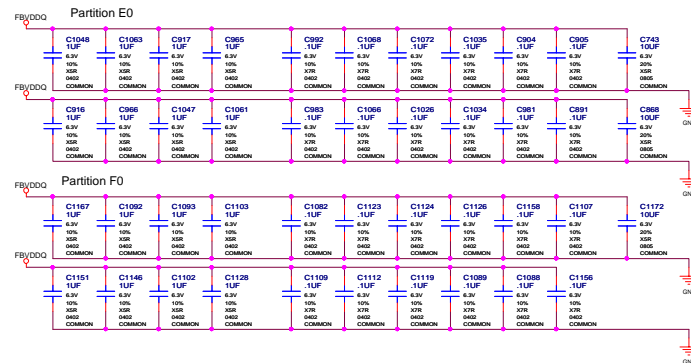
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Decoupling: Memory Section E-G

Decoupling for FBVDDQ

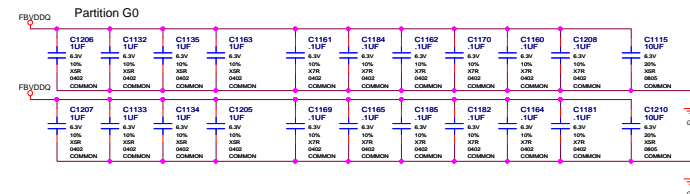
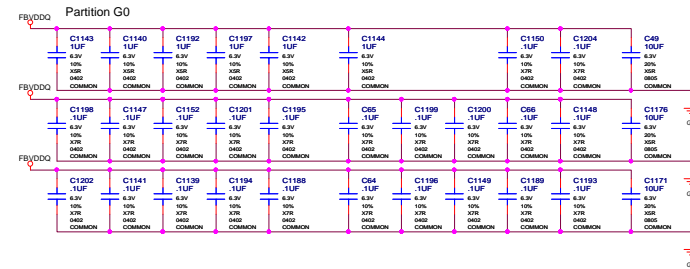


Decoupling for FBVDDQ



Banks E-G FBVDDQ
Combined Distributed Capacitance

210 uF



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Date Friday, June 05, 2009	Sheet 17 of 41

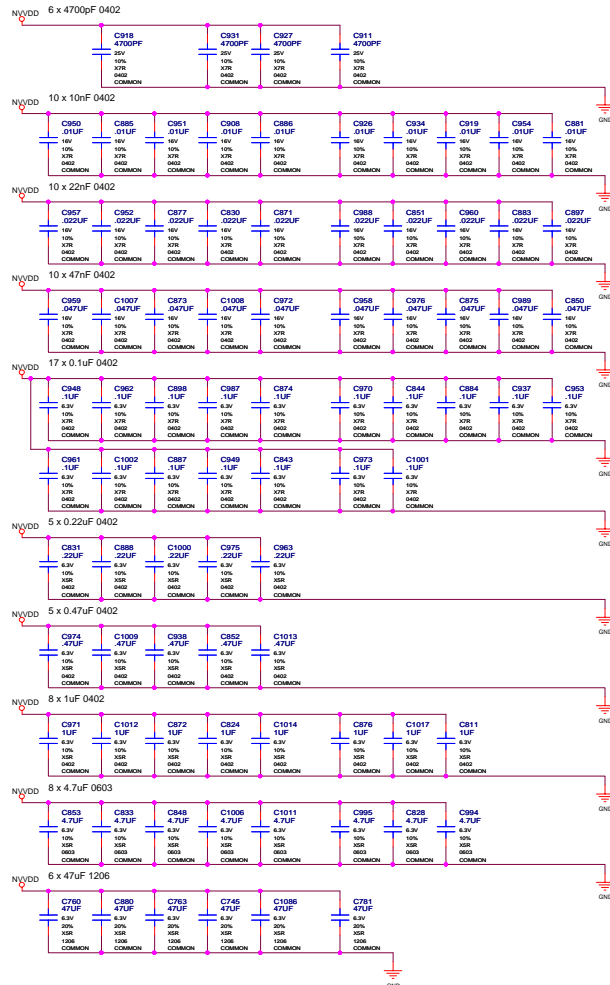
Decoupling: GPU (NVVDD, FBVDDQ)

Decoupling for NVVDD (under GPU)

GPU - NVVDD

Combined Distributed Capacitance

494 uF

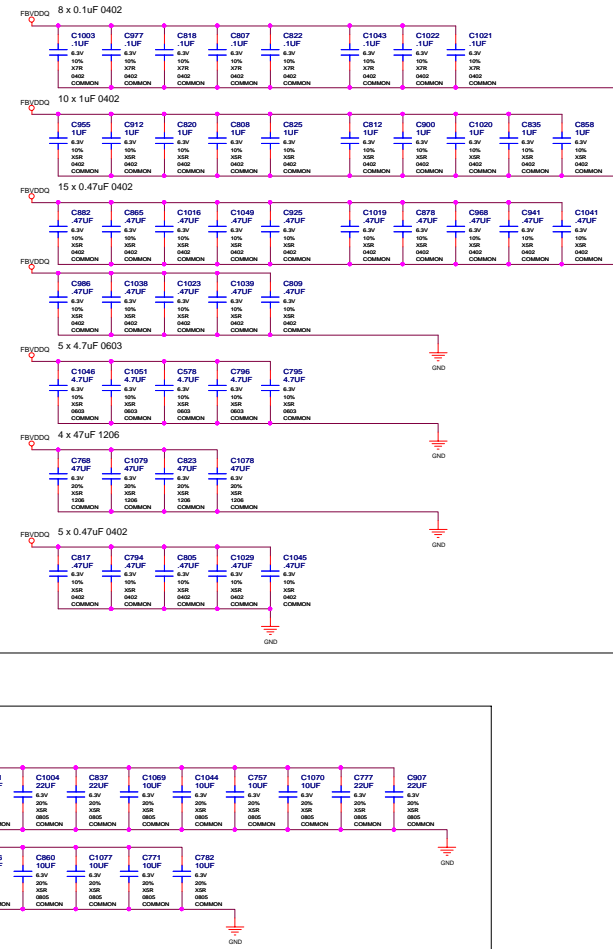


Decoupling for FBVDDQ (under GPU)

GPU - FBVDDQ

Combined Distributed Capacitance

230 uF



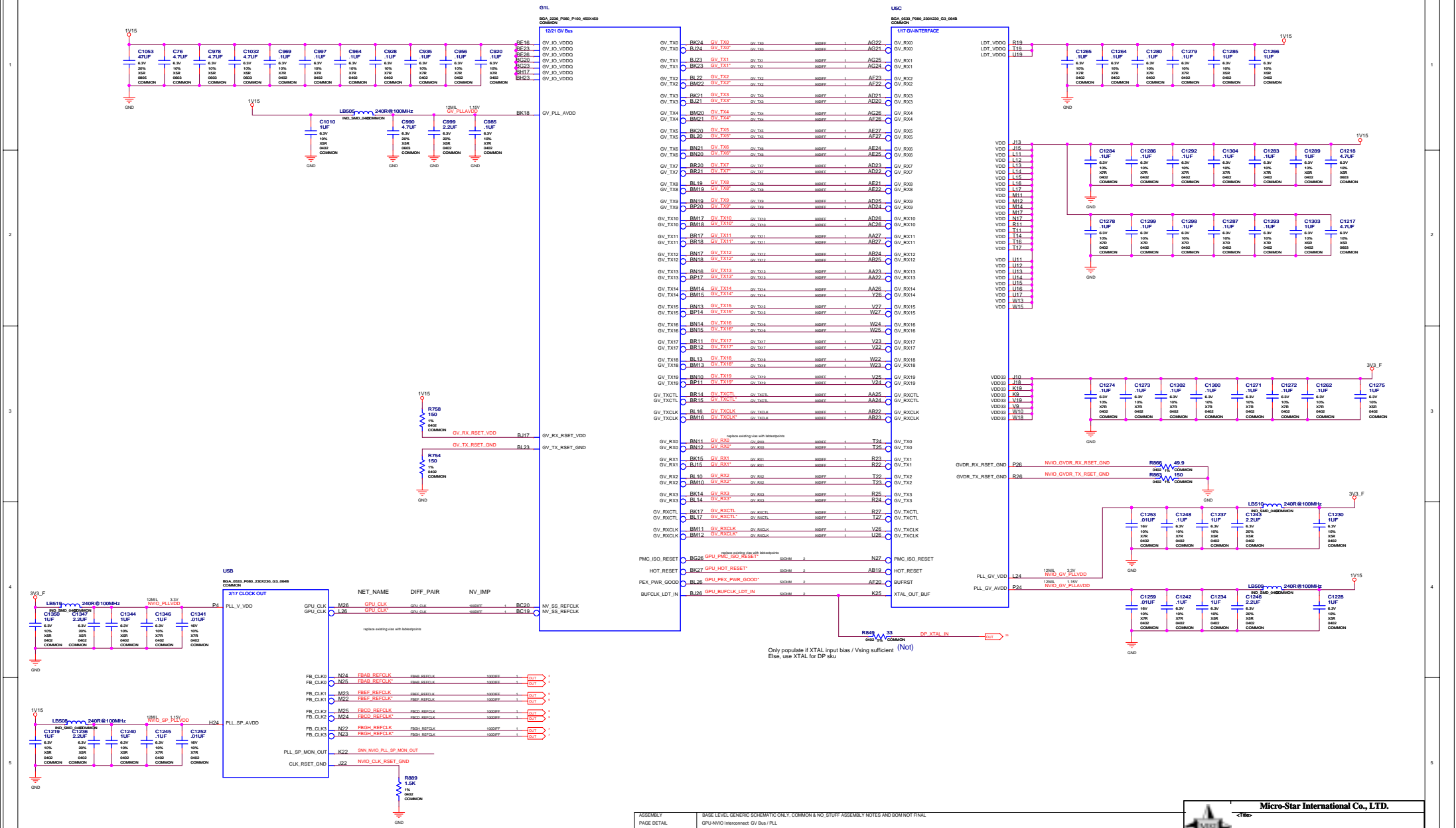
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ASSEMBLY
PAGE DETAIL

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Decoupling GPU (NVVDD, FBVDDQ)

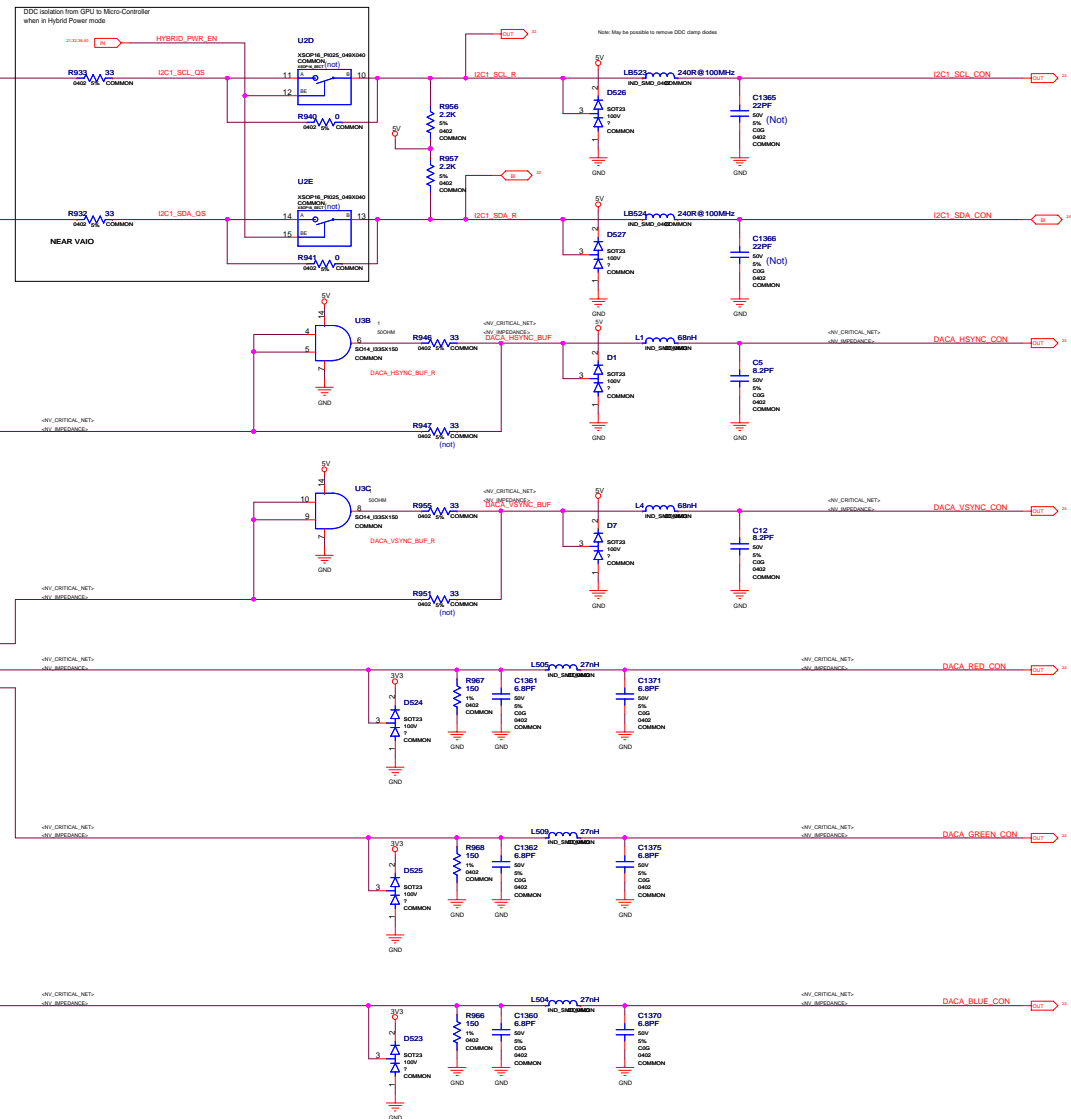
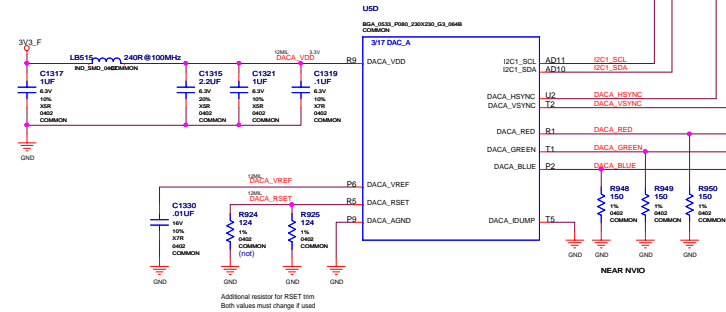
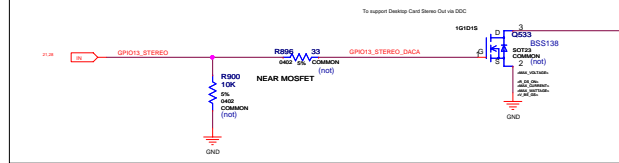
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GPU-NVIO Interconnect: GV Bus / PLL



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Display: DACA (Middle DVI-I)



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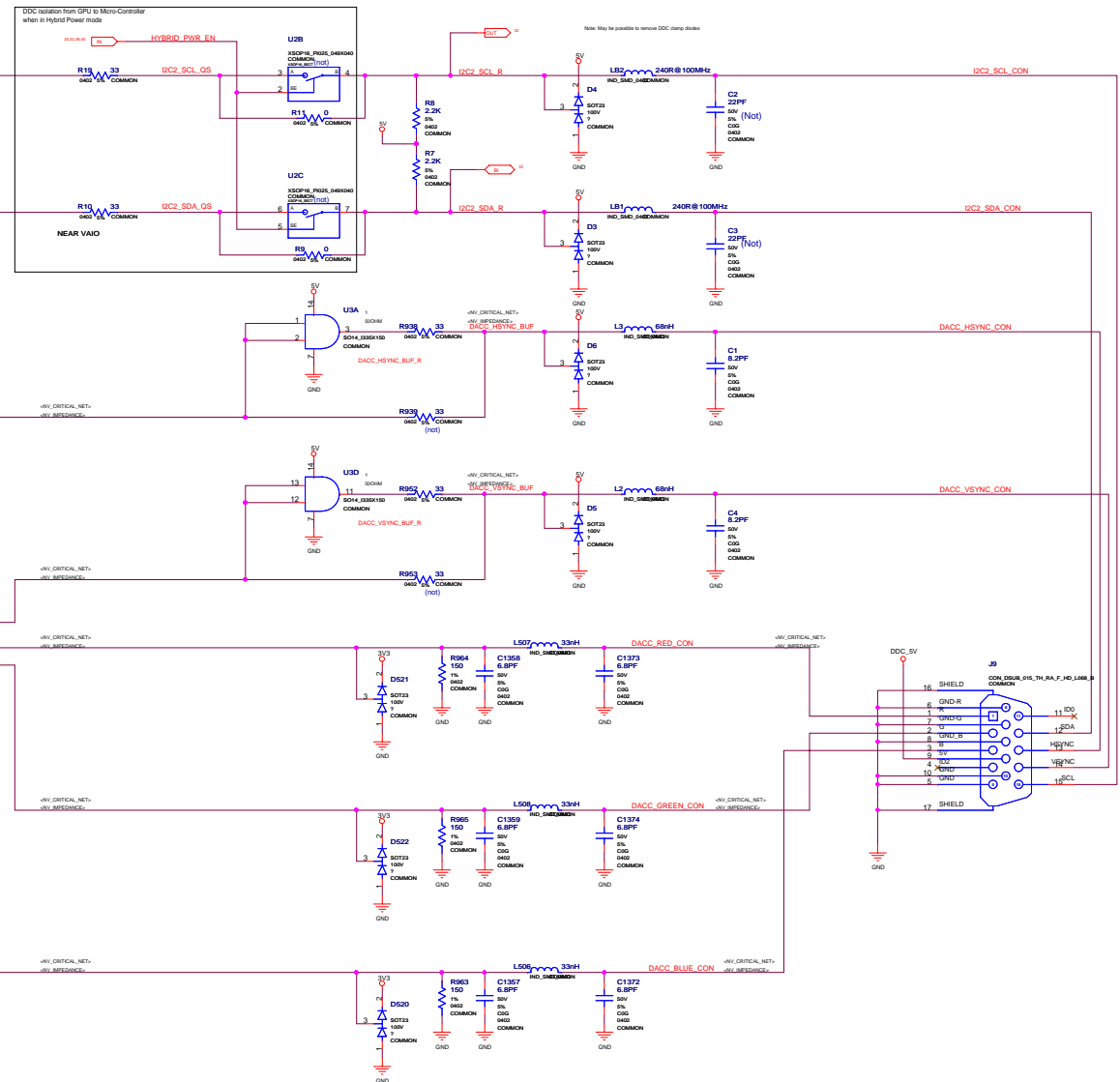
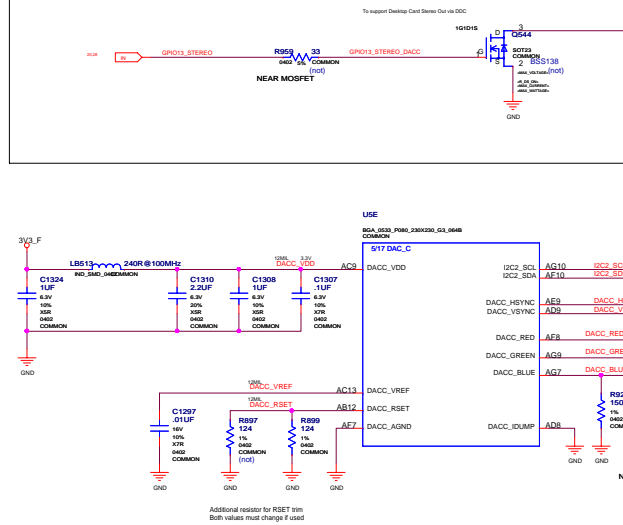
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PAGE DETAIL	Display: DACA (Middle DVI-I)



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Display: DACC (South DVI-I)



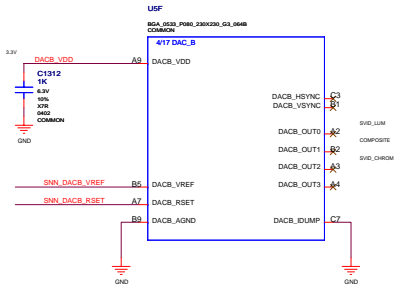
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: DACC (South DVI-I)

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	<Title>		
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Display: DACB (North MiniDIN) SD/HDTV out

11/21 remove TV



Additional resistor for RESET trim
Both values must change if used

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ASSEMBLY
PAGE DETAIL

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Display: DACB (North MiniDIN) SD/HDTV out



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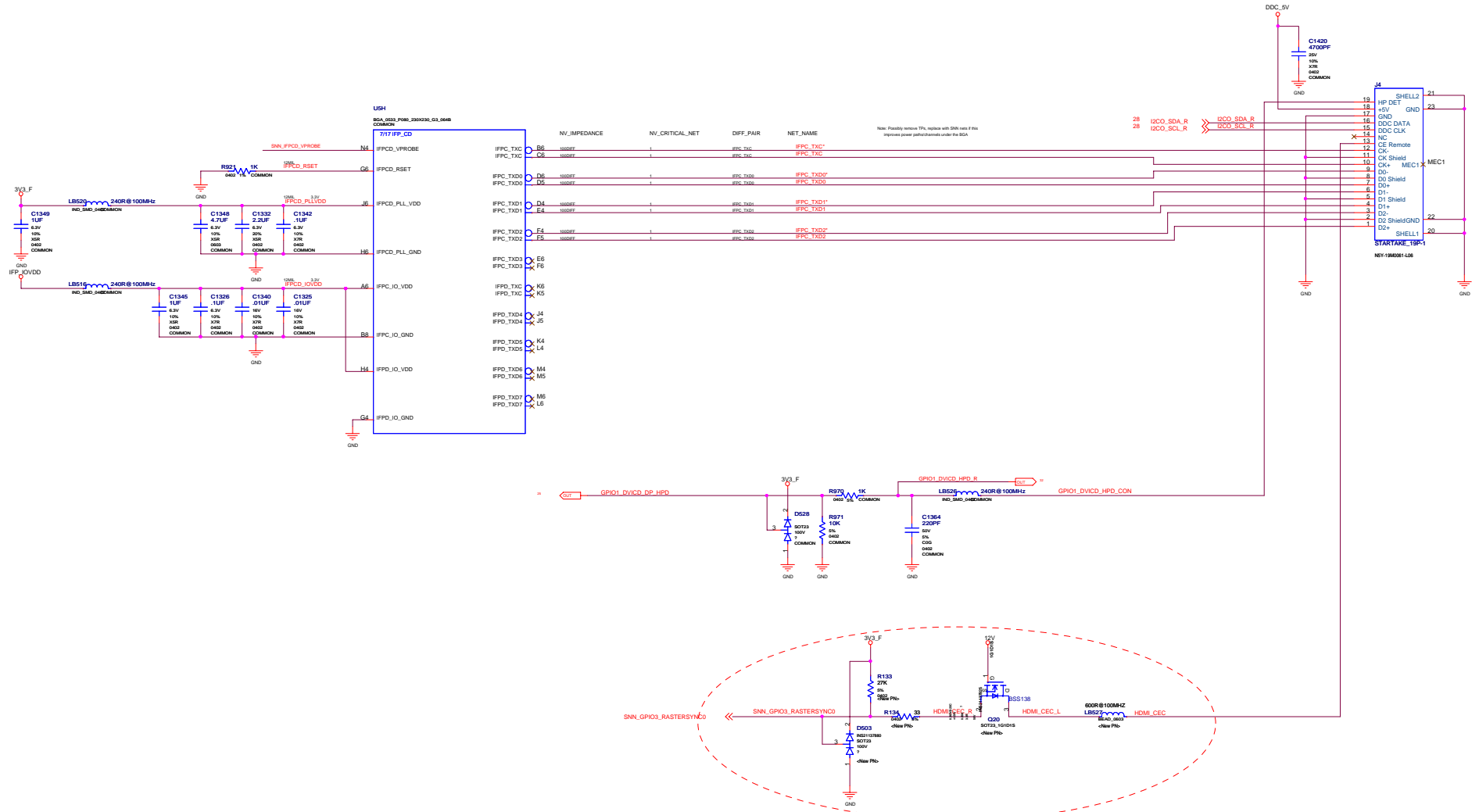
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Display: IFPCD for middle DVI-I (with DACA)



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PAGE DETAIL	Display: IFPCD for middle DVI-I (with DACA)



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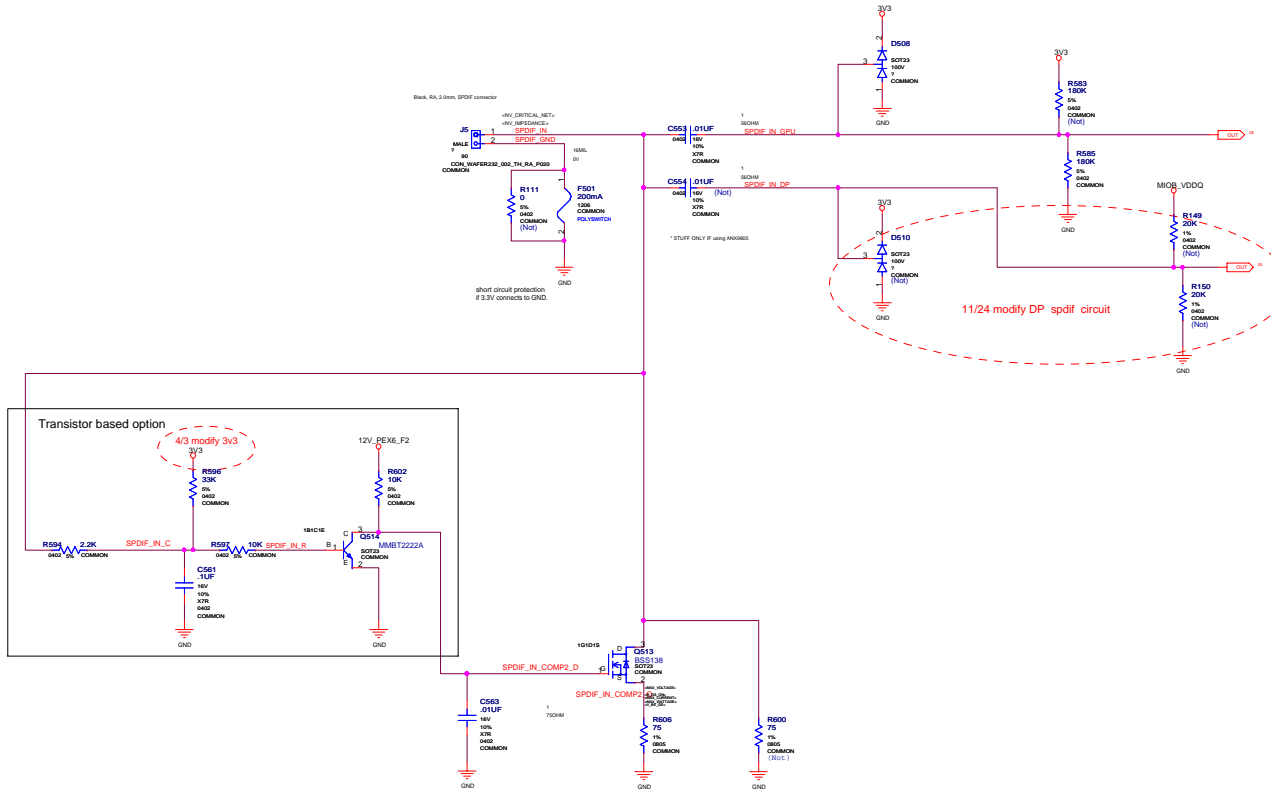
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41			

Connectors: SPDIF

SPDIF INPUT / Level Detection



Transistor based option

4/3 modify 3v3

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PAGE DETAIL

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Connectors: SPDIF



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Friday, June 05, 2009

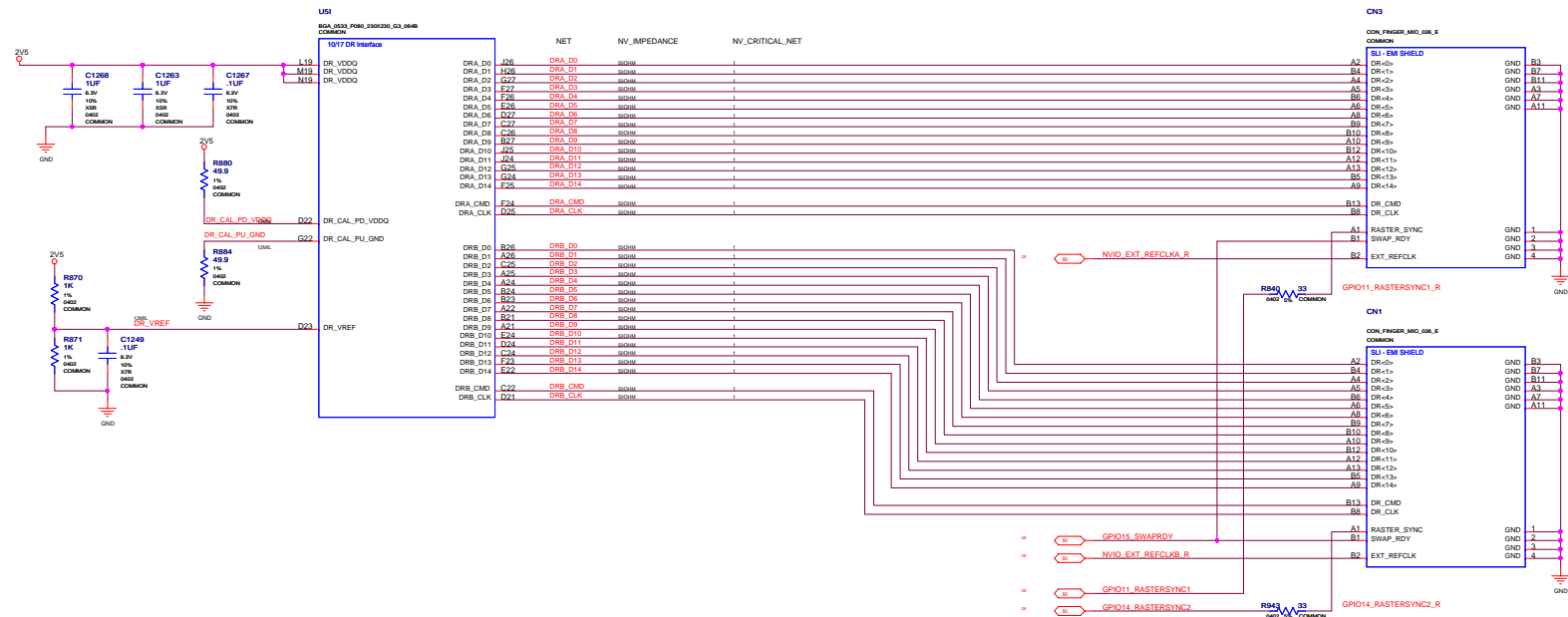
Sheet

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Connectors: DR Interface (Dual SLI)



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Connectors: DR Interface (Dual SLI)



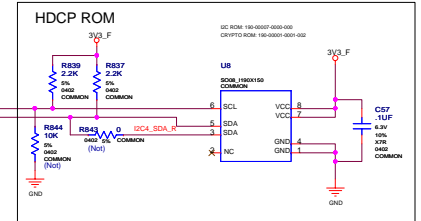
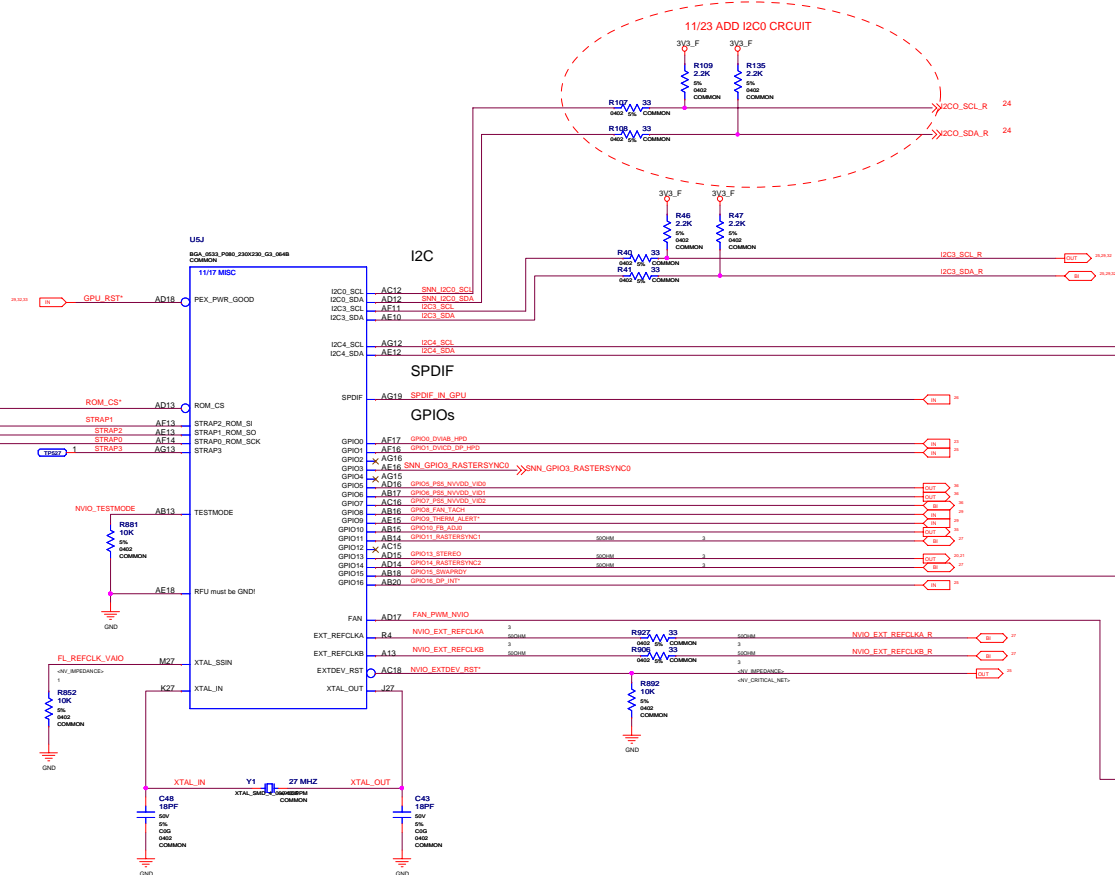
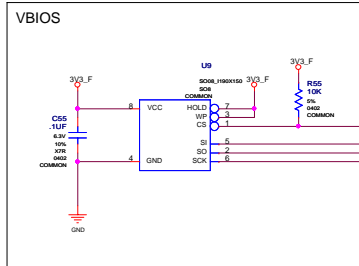
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VBIOS



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO / XTAL / VBIOS / HDCP / I2C



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Date: Friday, June 08

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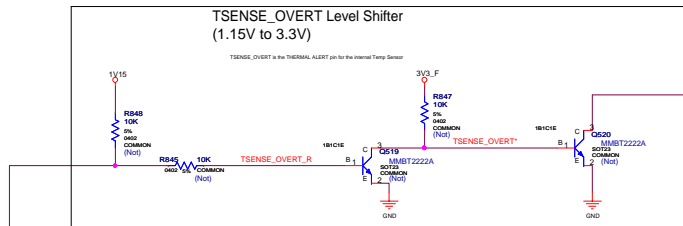
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MISC: FAN / THERM

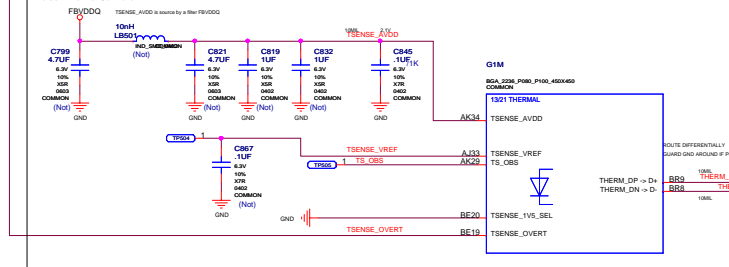
TSENSE_OVERT Level Shifter (1.15V to 3.3V)

TSENSE_OVERT is the THERMAL_ALERT pin for the Internal Temp Sensor



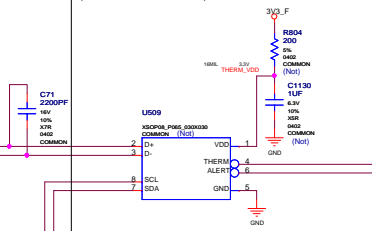
Internal GPU Thermal Sensor

Default Thermal Controller



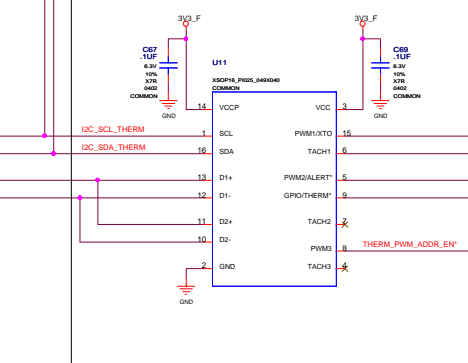
Notes: TSENSE_OVERT is connected to a 1V15 (internal) sensor pin.
TSENSE_OVERT is connected to a 1V15 (internal) sensor pin.

LM99/MAX6649 (Alternate Thermal Controller)

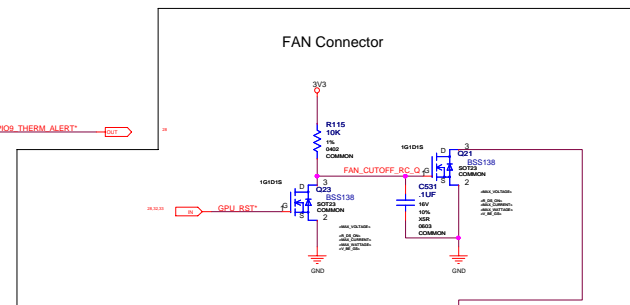


Note: POR internal thermal control external controls will be ON

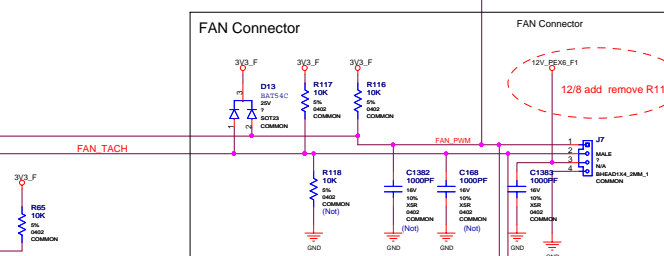
ADT7473 (Secondary thermal controller choice)



FAN Connector



FAN Connector



GPU Driven Fan and Tach

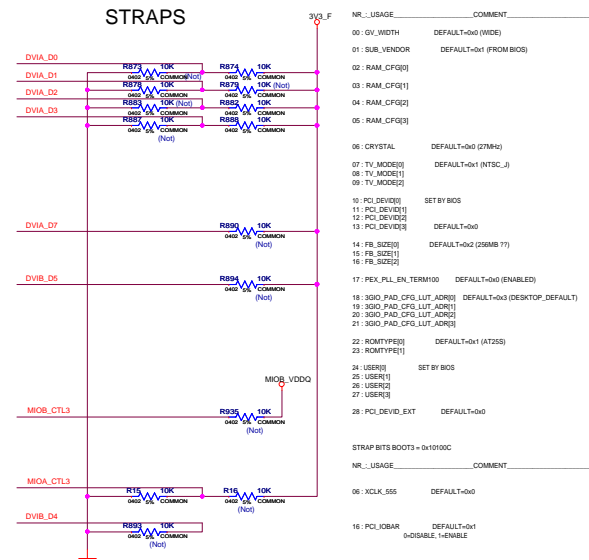
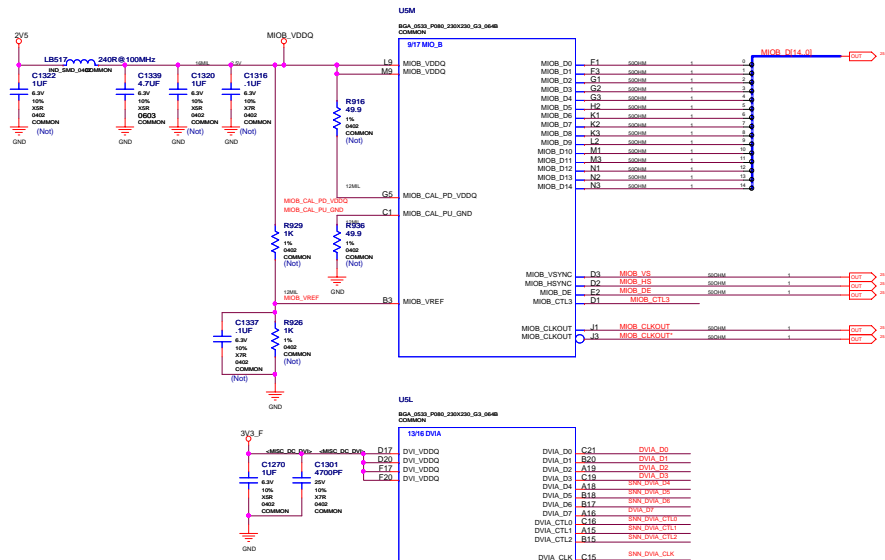
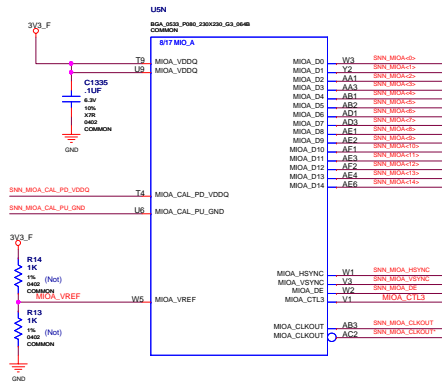


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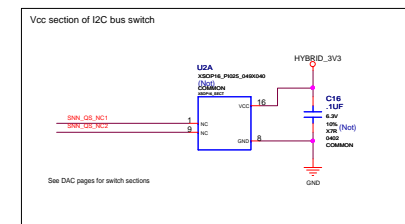
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Size	Document Number	Rev	
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MISC: MIO / DVI / STRAPS



CFG	Config	Width	Vendor
0000	Reserved		
0001	16Mx32	512-bit	Qimonda
0010	16Mx32	512-bit	Hynix
0011	16Mx32	512-bit	Samsung
0100	Reserved		
0101	32Mx32	512-bit	Qimonda
0110	32Mx32	512-bit	Hynix
0111	32Mx32	512-bit	Samsung
1000	Reserved		
1001	16Mx32	448-bit	Qimonda
1010	16Mx32	448-bit	Hynix
1011	16Mx32	448-bit	Samsung
1100	Reserved		
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1110	32Mx32	448-bit	Hynix
1111	32Mx32	448-bit	Samsung

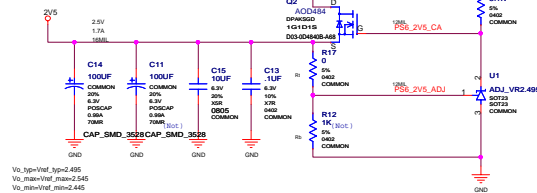
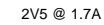
Power: Hybrid Power



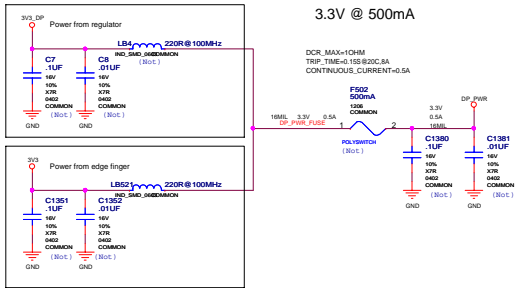
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	Date: Friday, June 05, 2009	Sheet 32 of 41	

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2V5

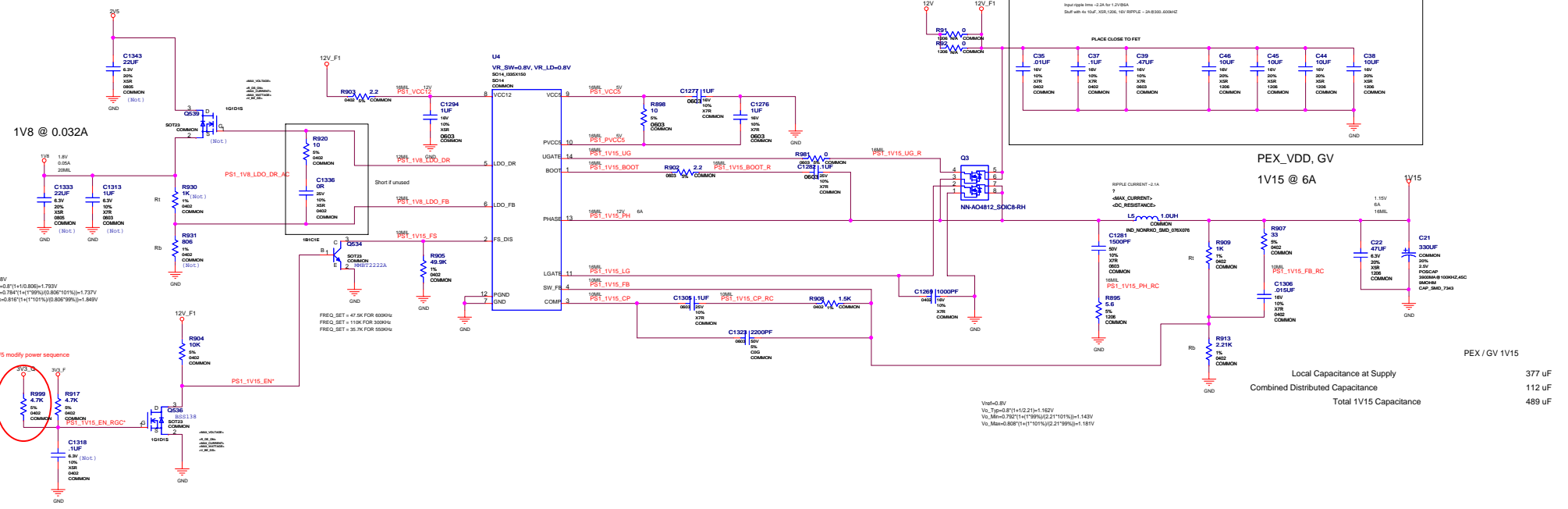


3V3_DP 3.3V @ 500mA



8V5	11/21:remove 8V5 circuit
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1V8 @ 0.032A



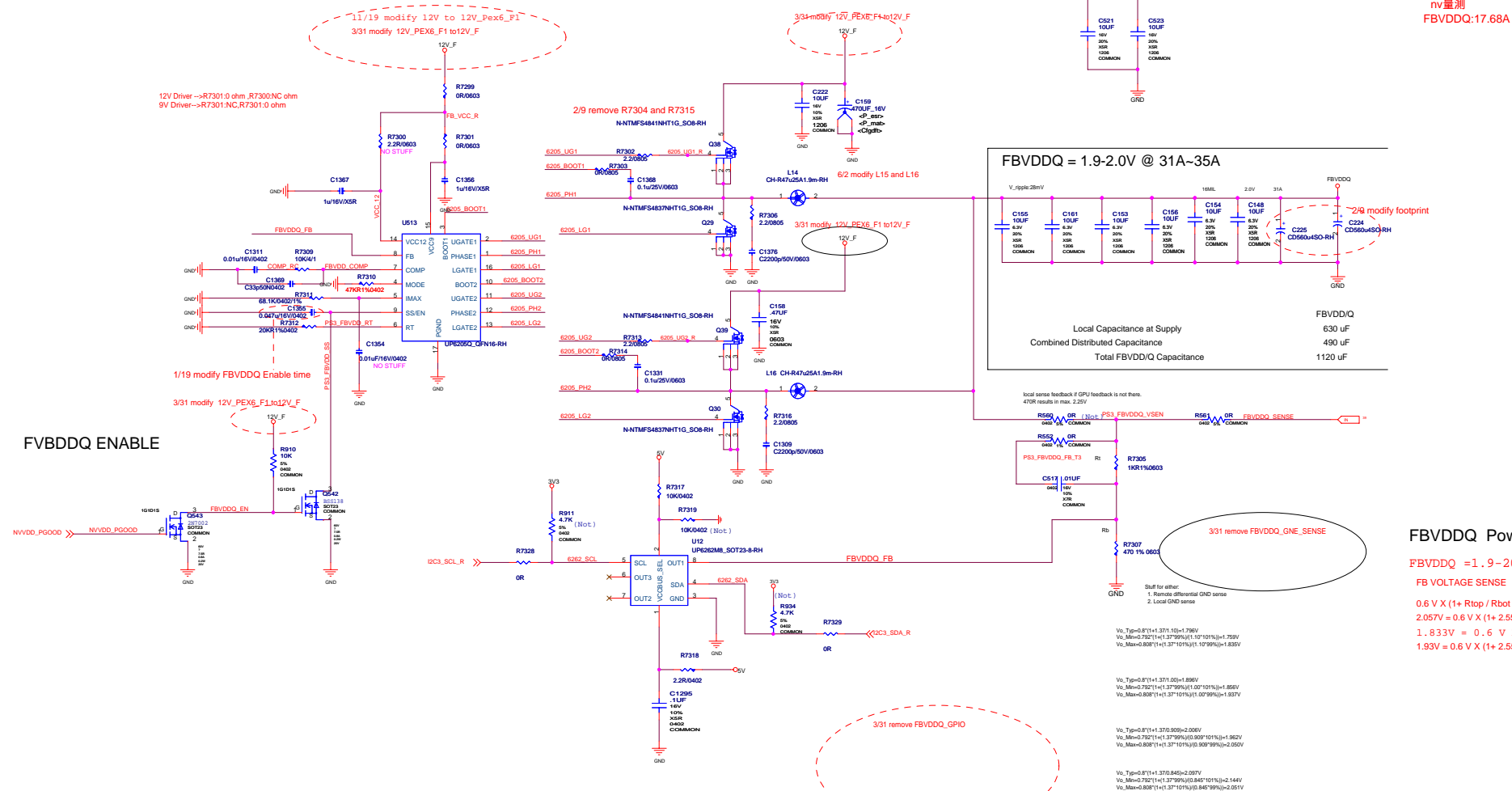
PEX / GV 1V15

377 uF

112 uF

489 uF

Power Supply: Combined FBVDD/Q



FBVDDQ Power Supply

FBVDDQ = 1.9-20V @ 31A~35A

FB VOLTAGE SENSE

$0.6\text{ V X } (1 + R_{top} / R_{bot})$
 $2.057\text{V} = 0.6\text{ V X } (1 + 2.55\text{K} / 1.05\text{K})$
 $1.833\text{V} = 0.6\text{ V X } (1 + 2.55\text{K} / 1.24\text{K})$
 $1.93\text{V} = 0.6\text{ V X } (1 + 2.55\text{K} / 1.15\text{K})$

```

Vo_Type=0.8*(1+1.371/10)=1.796V
Vo_Min=0.792*(1+(1.37/99%)*(1.10/101%))=1.799V
Vo_Max=0.808*(1+(1.37/101%)*(1.10/99%))=1.839V

Vo_Type=0.8*(1+1.371/10)=1.896V
Vo_Min=0.792*(1+(1.37/99%)*(1.00/101%))=1.856V
Vo_Max=0.808*(1+(1.37/101%)*(1.00/99%))=1.937V

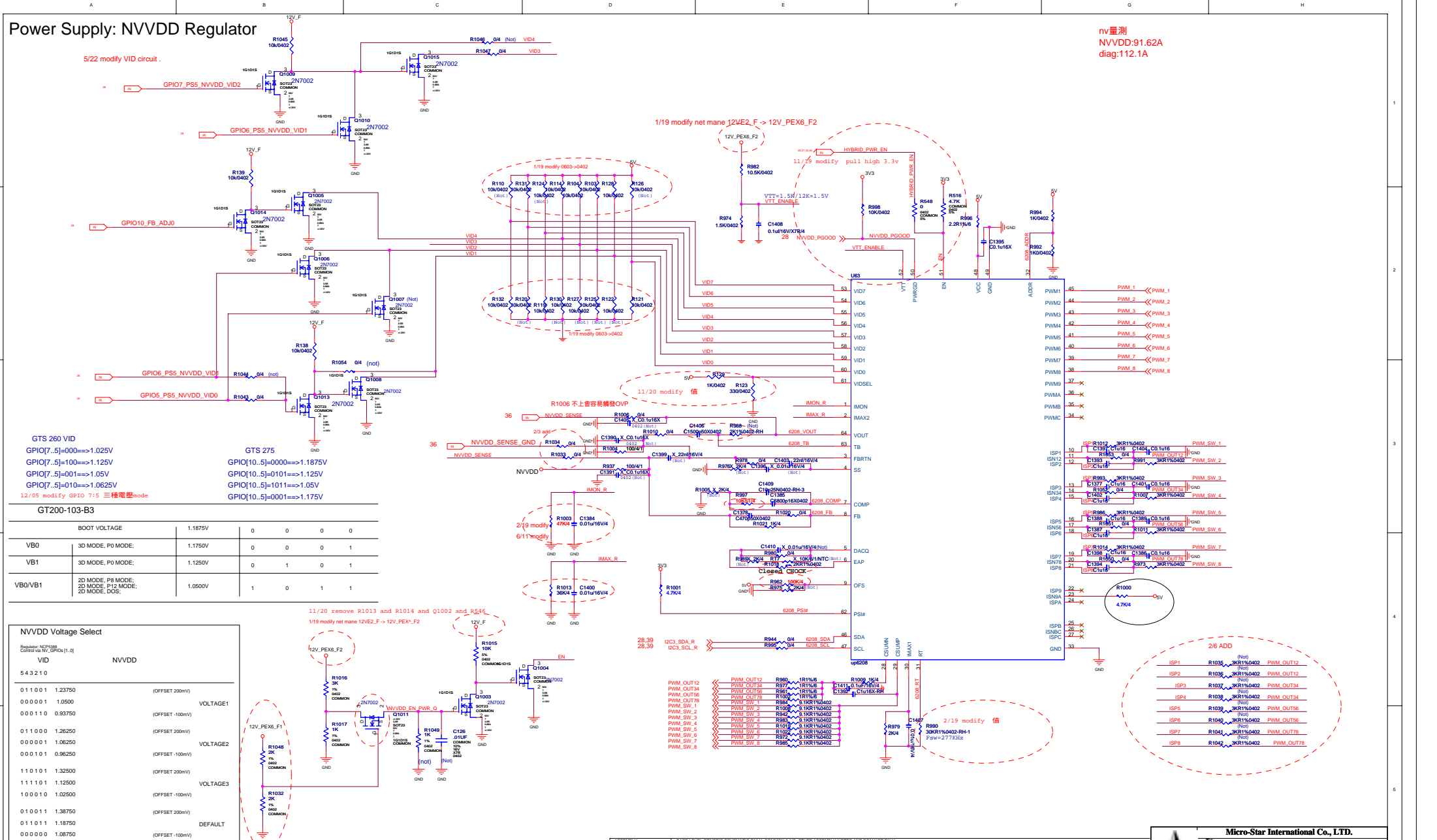
Vo_Type=0.8*(1+1.370/909)=2.006V
Vo_Min=0.792*(1+(1.37/99%)*(0.909/101%))=1.962V
Vo_Max=0.808*(1+(1.37/101%)*(0.909/99%))=2.050V

Vo_Type=0.8*(1+1.370/845)=2.097V
Vo_Min=0.792*(1+(1.37/99%)*(0.845/101%))=2.144V
Vo_Max=0.808*(1+(1.37/101%)*(0.845/99%))=2.051V

```

Power Supply: NVVDD Regulator

nv量測
NVVDD:91.62A
diag:112.1A




GT200-103-B3						
BOOT VOLTAGE		1.1875V	0	0	0	0
VB0	3D MODE, P0 MODE:	1.1750V	0	0	0	1
VB1	3D MODE, P0 MODE:	1.1250V	0	1	0	1
VB0/VB1	2D MODE, P8 MODE: 2D MODE, P12 MODE: 2D MODE, DQS:	1.0500V	1	0	1	1

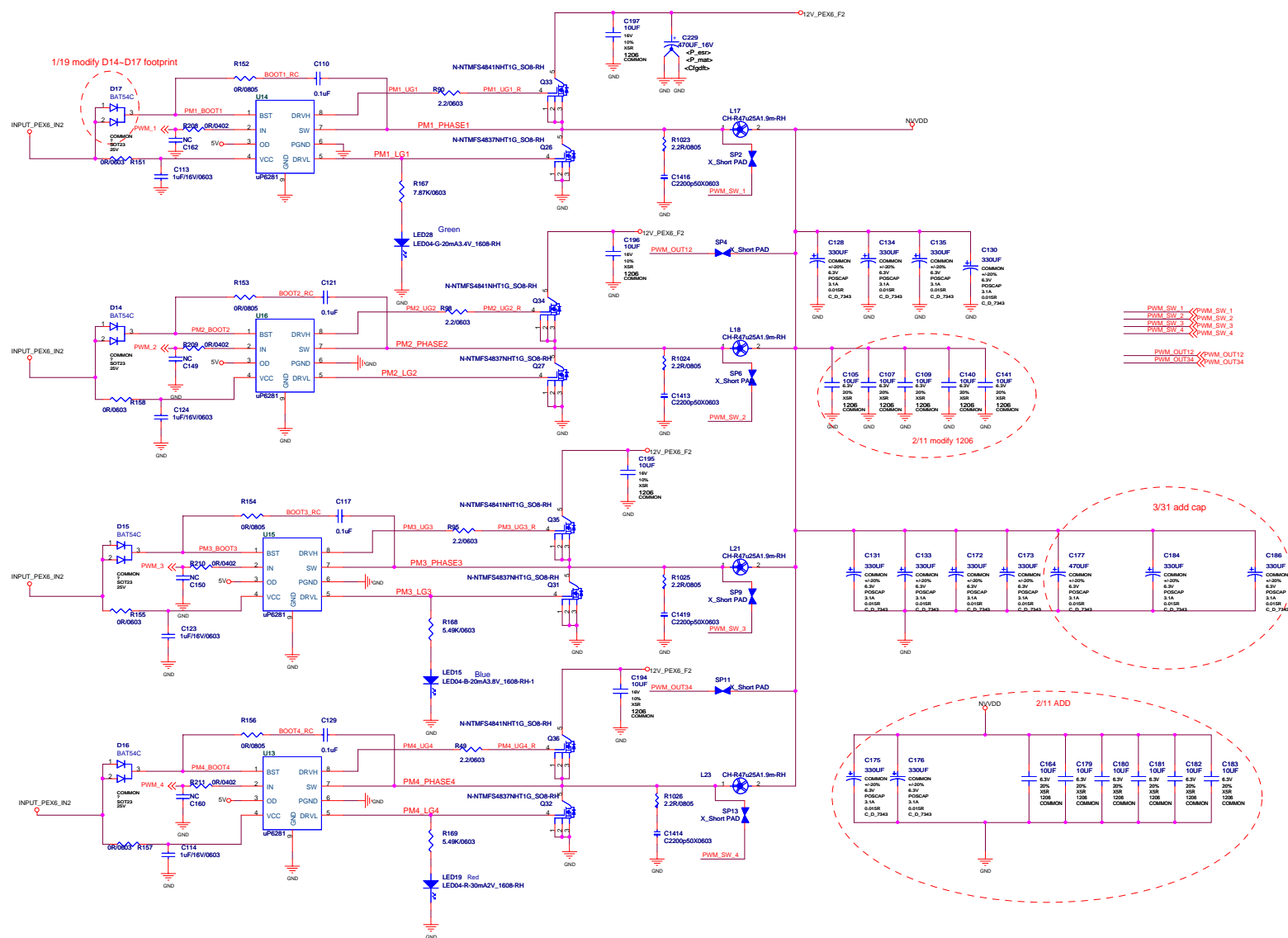
NVDD Voltage Select					
Register: NVDSPSR Control bits: NV, CFC[1], Q					
VID		NV/DD			
543210					
011001	1.23750	(OFFSET=200mV)	VOLTAGE1		
000001	1.05000				
000110	0.93750	(OFFSET=-100mV)			
011000	1.26250	(OFFSET=200mV)	VOLTAGE2		
000001	1.06250				
000101	0.96250	(OFFSET=-100mV)			
110101	1.32500	(OFFSET=200mV)	VOLTAGE3		
111101	1.12500				
100010	1.02500	(OFFSET=-100mV)			
010011	1.38750	(OFFSET=200mV)	DEFAULT		
010111	1.18750				
000000	1.08750	(OFFSET=-100mV)			

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVDD REGULATOR

	Micro-Star International Co., LTD.			
	<Title>			
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Power Supply: NVVDD Phase 1,2 powered from external PEX 6PIN



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PAGE DETAIL	Power Supply: NVVDD Phase 1-2 of 4

Micro-Star International Co., LTD.

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Size	Document Number
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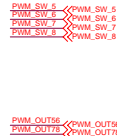
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Date:	Thursday, June

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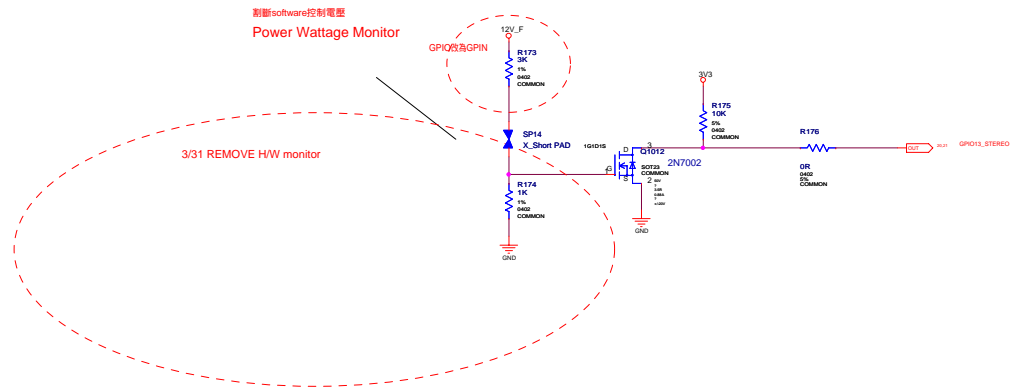
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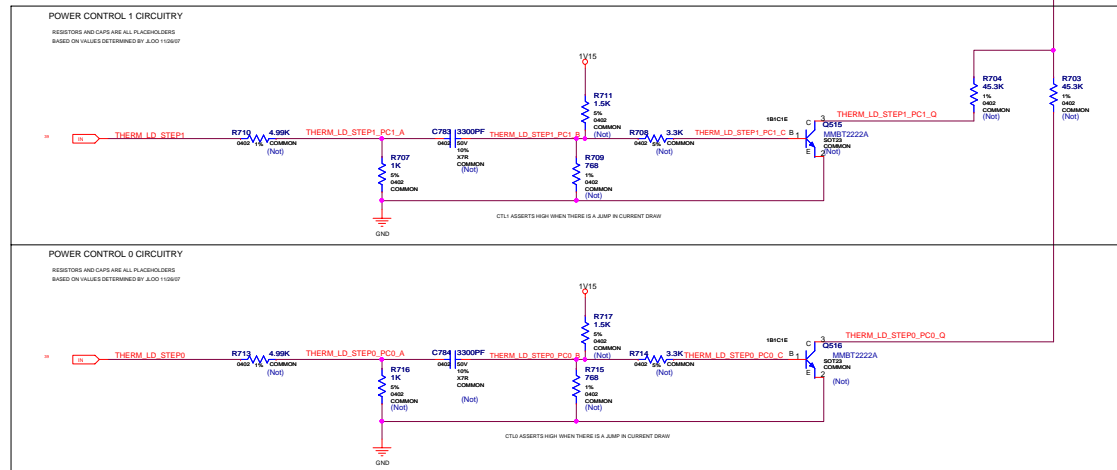
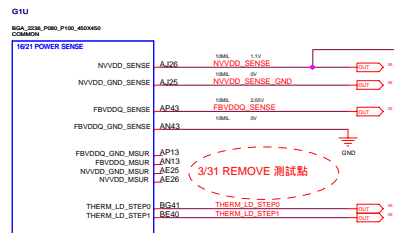


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Power Supply: NVVDD power control



NVVDD & FBVDDQ SENSE/MSUR

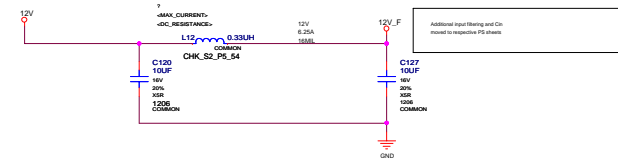


Power: Input Rail Filter and Detection Logic

Connector Power State Table

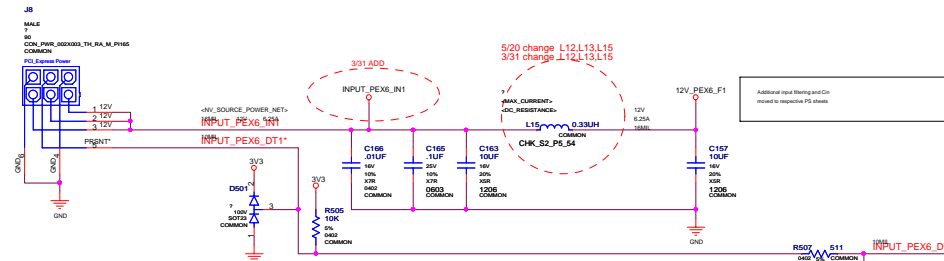
2d Connector	2d Connector	Power	STATE
Connected	Connected	225W	Full Perf
Connected	Not Connected	150W	Board Off
Not Connected	Connected	150W	Board Off
Not Connected	Not Connected	75W	Board Off

PEX_12V INPUT - 66W



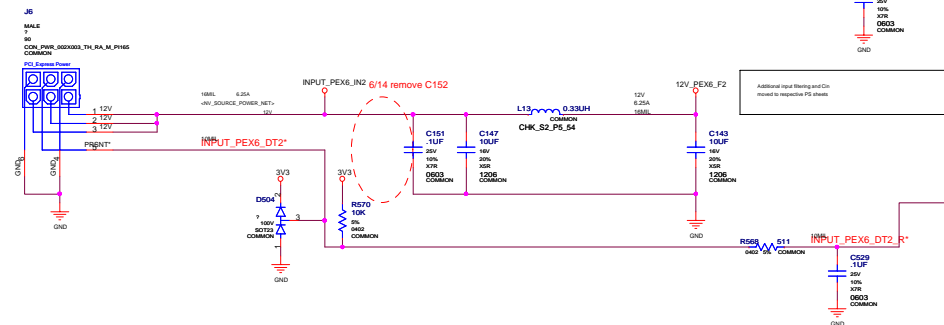
PEX6 INPUT 1 - 2x3 PCIE CON 75W

MUST BE ATTACHED AND POWERED TO START BOARD

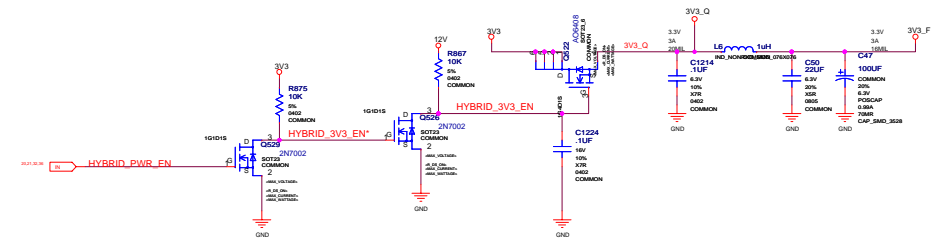


PEX6 INPUT 2 - 2x3 PCIE CON 75W

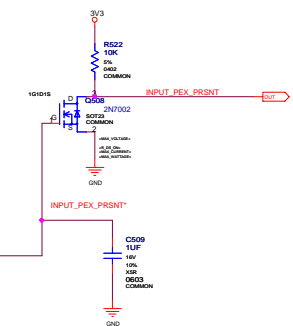
MUST BE ATTACHED AND POWERED TO START BOARD



PEX 3V3 INPUT - 10W

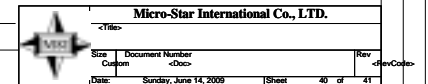


Summary PEX input present



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PAGE DETAIL	Power: Input Rail Filter and Detection Logic



Thermal/Mechanical/ID

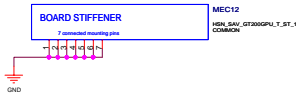
Bracket and Assembly



GPU Socket



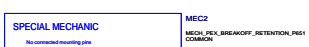
GPU Stiffener



NVIOx Socket

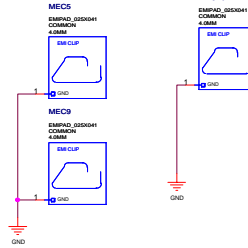


Hockey Stick Retention Mechanism

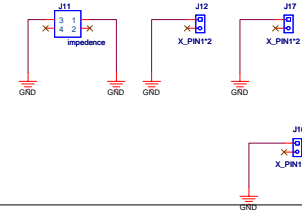
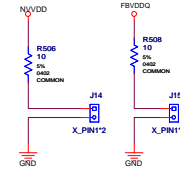


EMI Gnd Clips

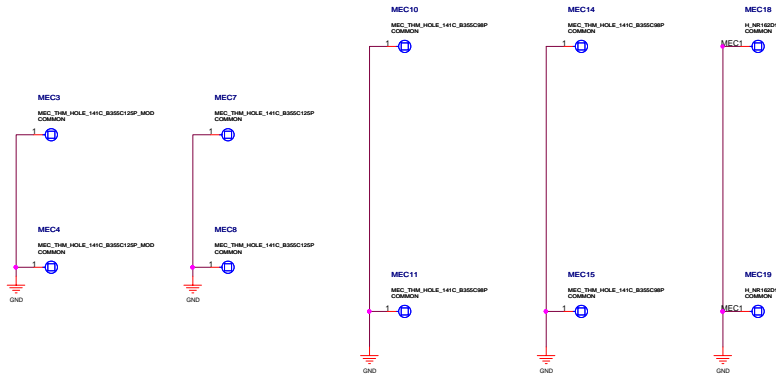
Top Side Clips



電源量測點



THERMAL/MECHANICAL HOLES



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ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Thermal/Mechanical

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