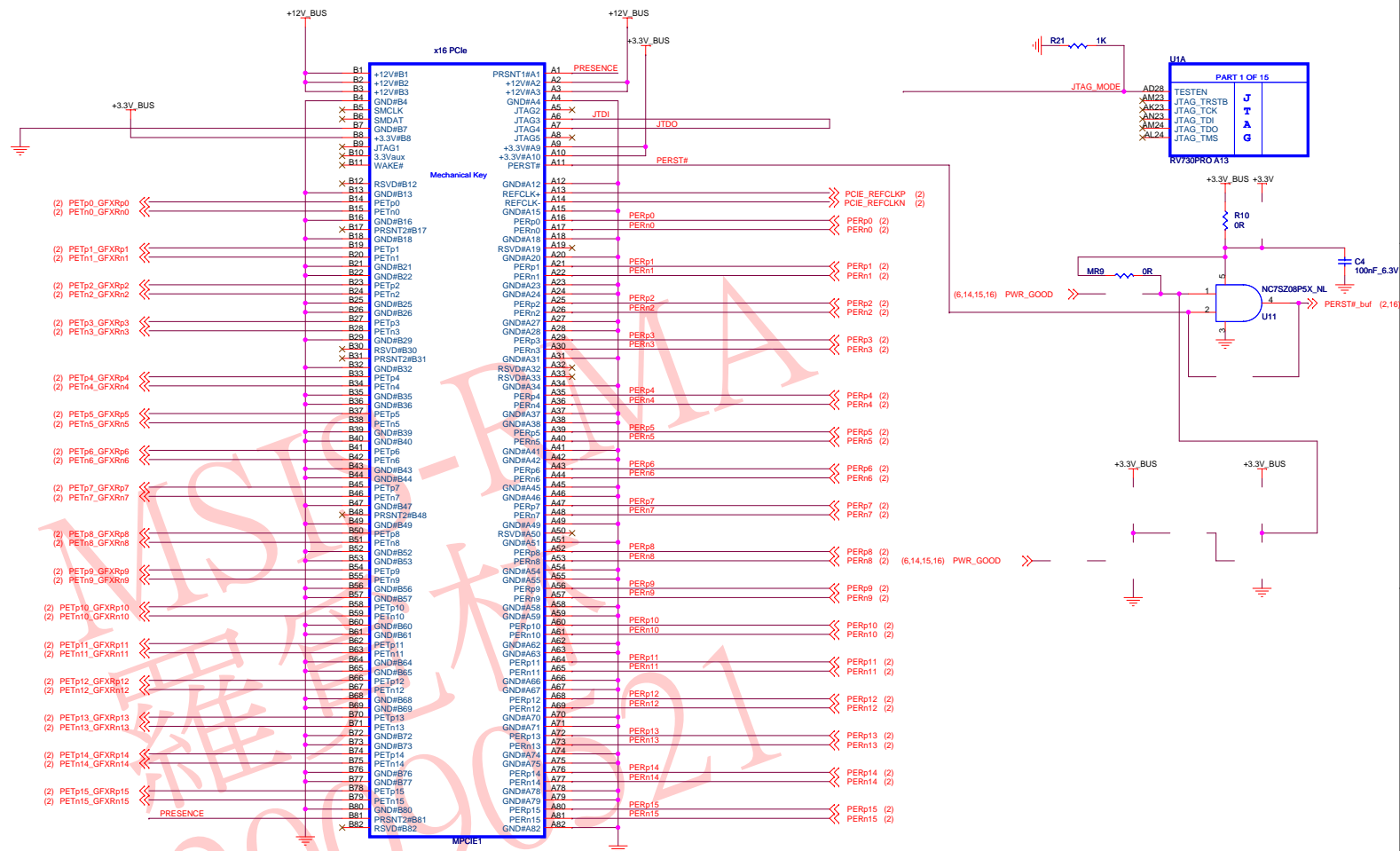
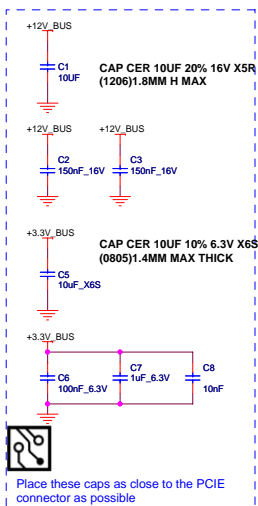




## PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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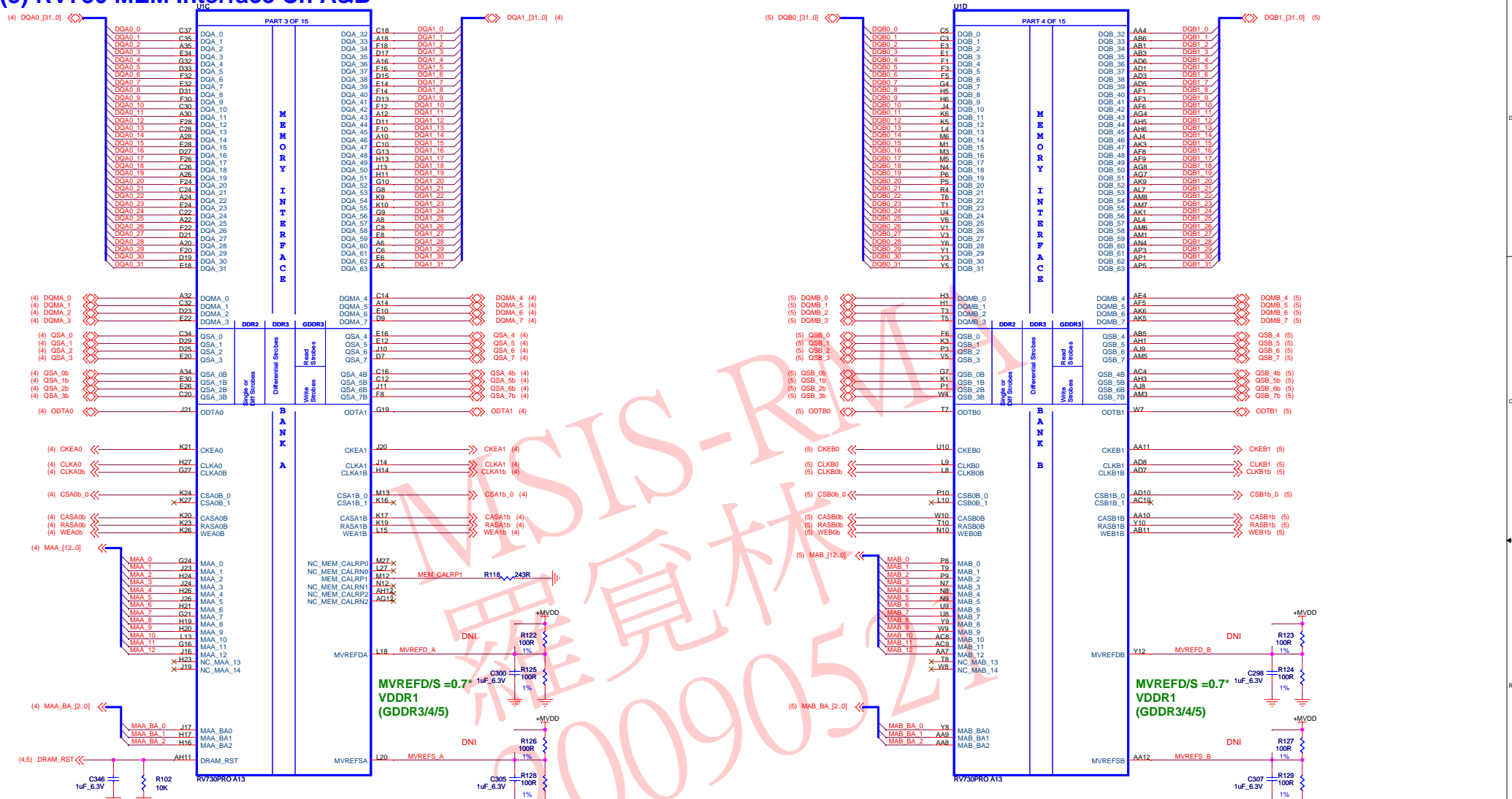
Rev 06


Title	RH RV730 DDR3 DP DP DVI
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Doc No.	102-B83401-00A
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Doc No. 102-B83401-00A

### (3) RV730 MEM Interface Ch A&B

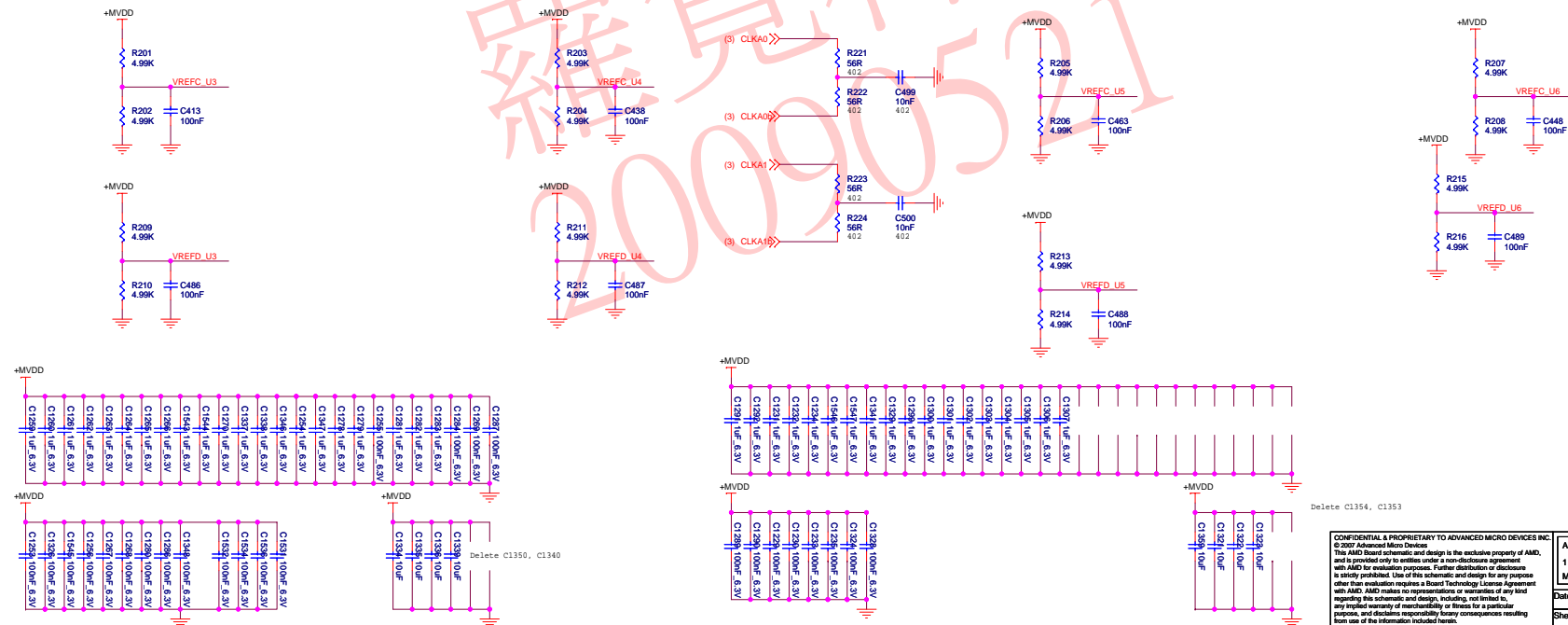
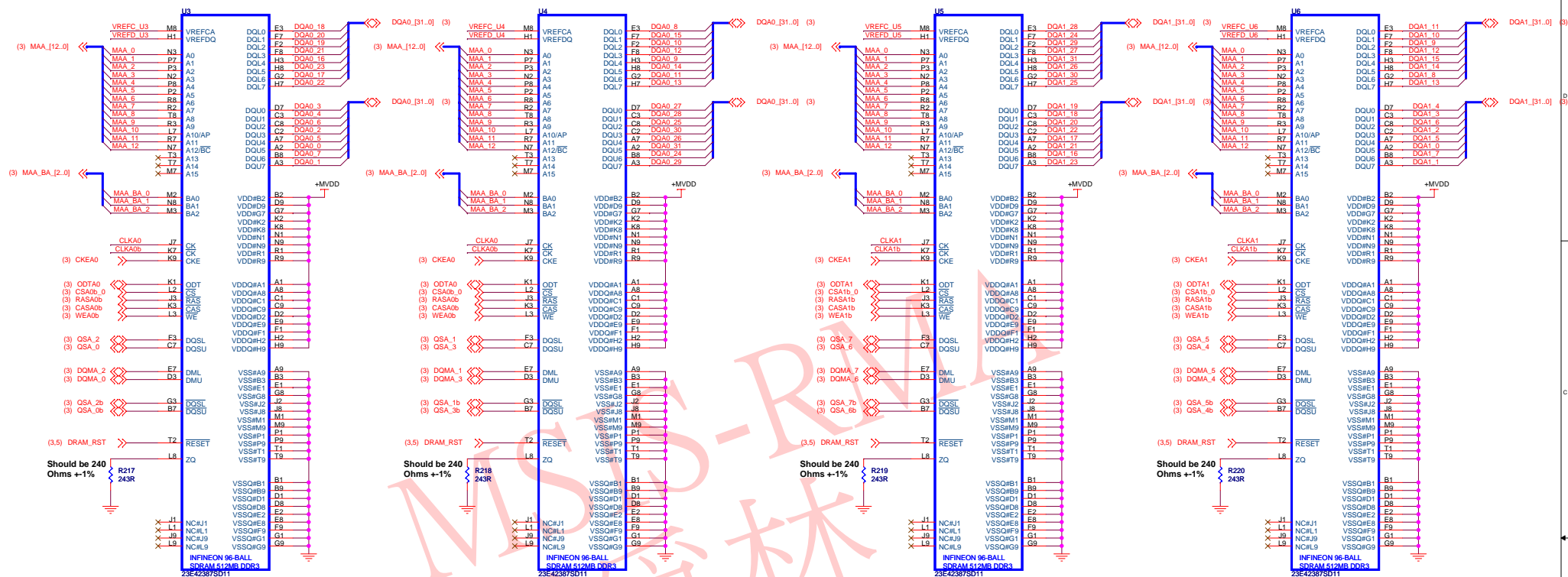


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Date: Tuesday, January 13, 2009		Rev 06	
Sheet	3	of	19

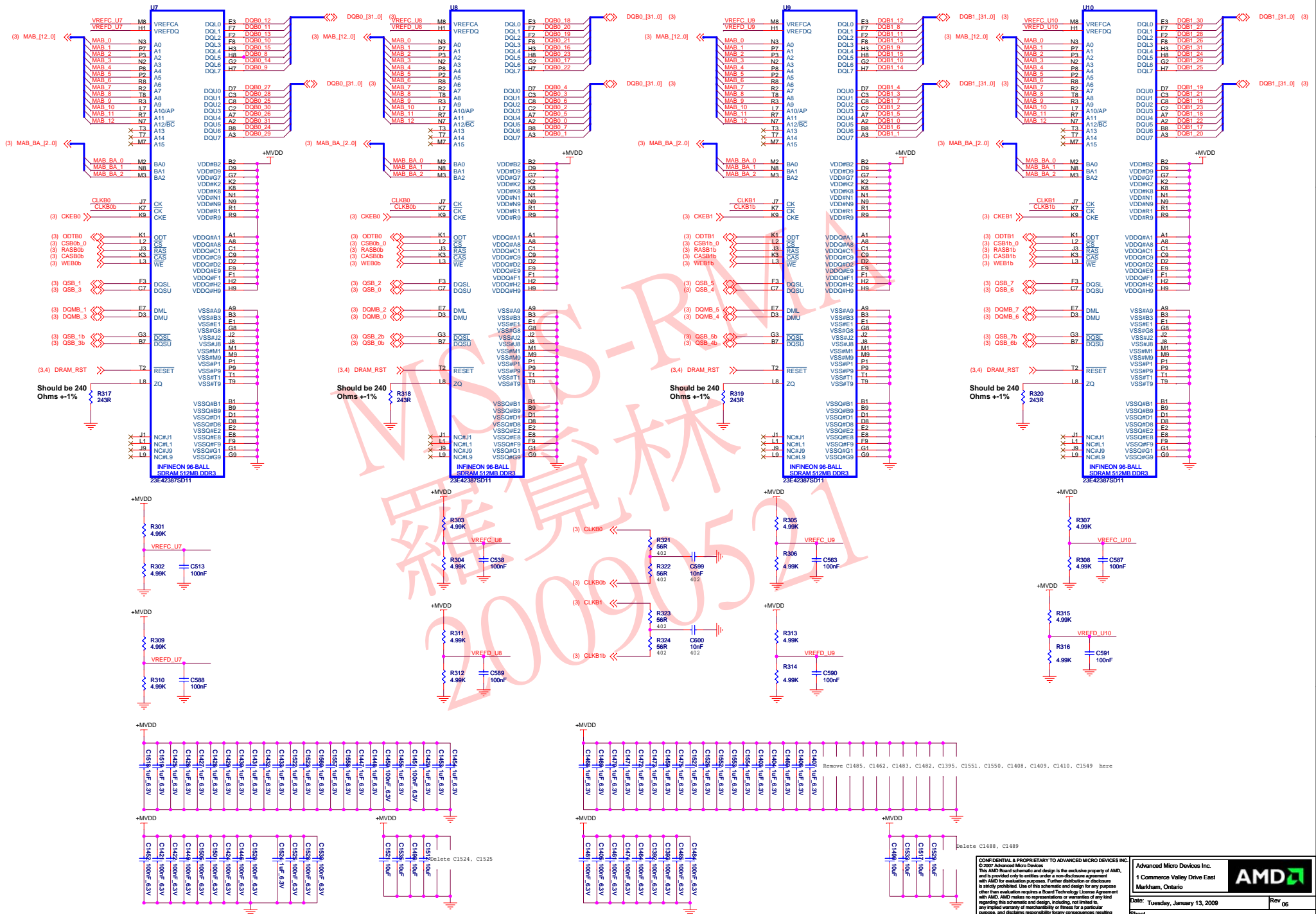
Title	RH RV730 DDR3 DP DP DVI	Doc No.	102-B83401-00A
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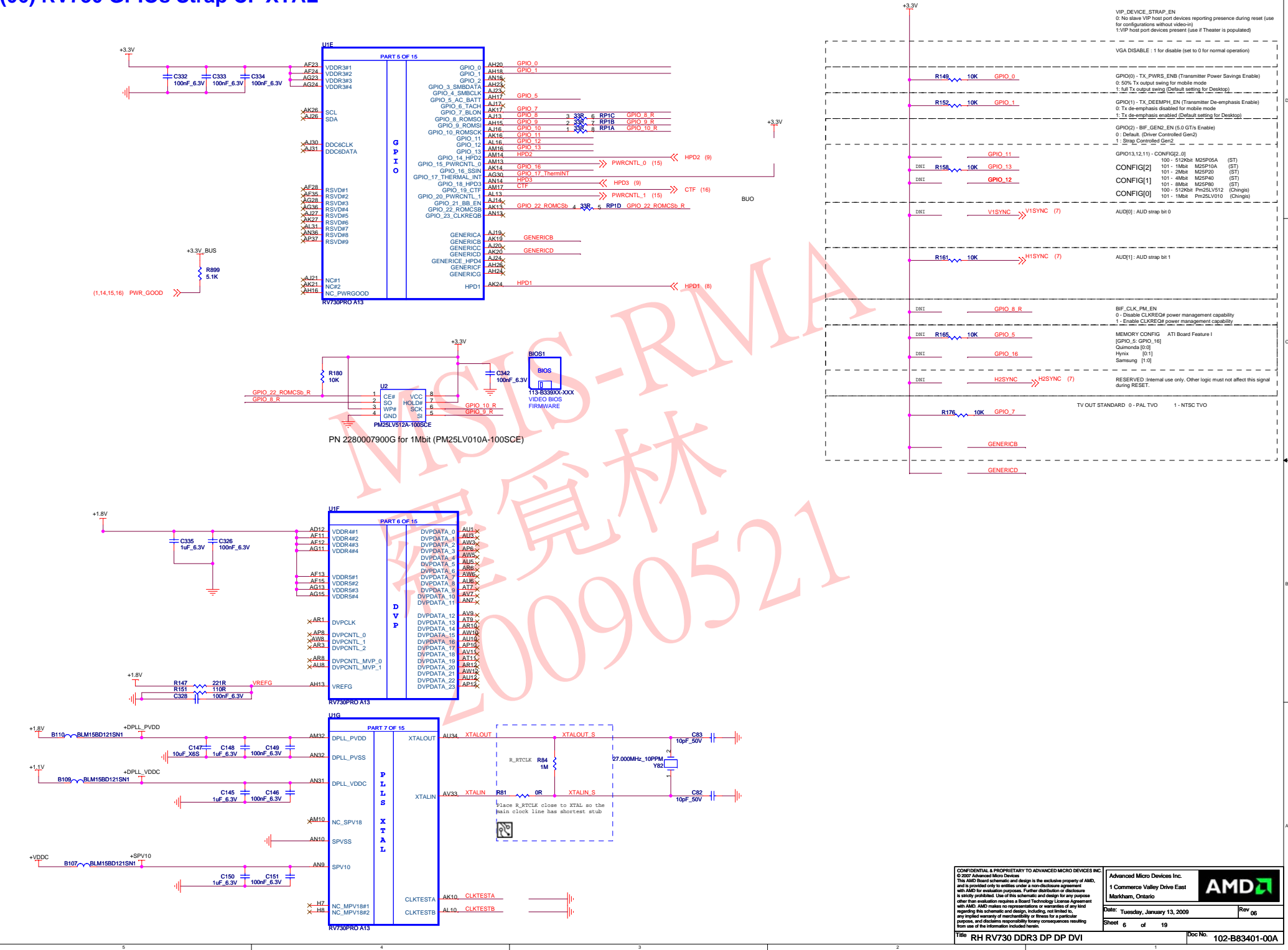
#### (4) DDR3 Memory Channel A



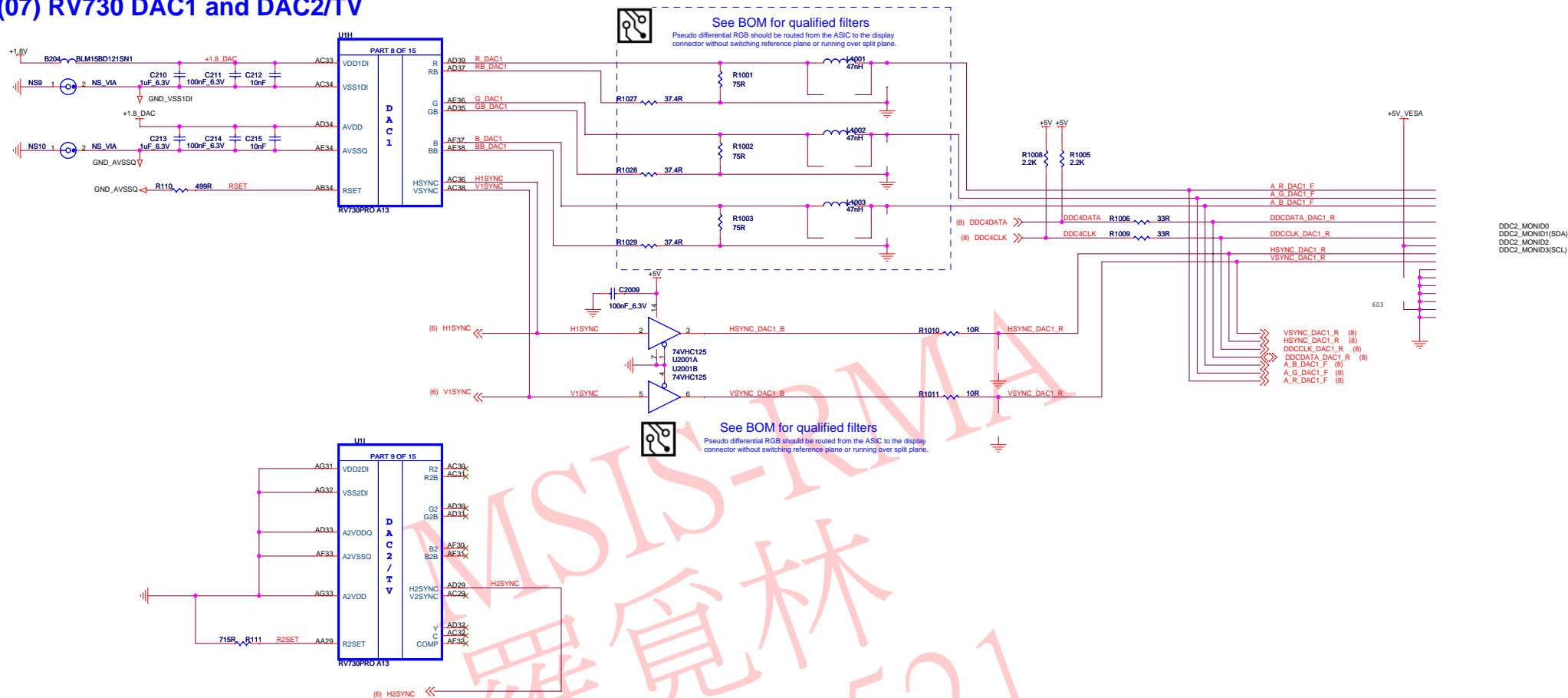
### (5) DDR3 Memory Channel B



(06) RV730 GPIOs Strap CF XTAL

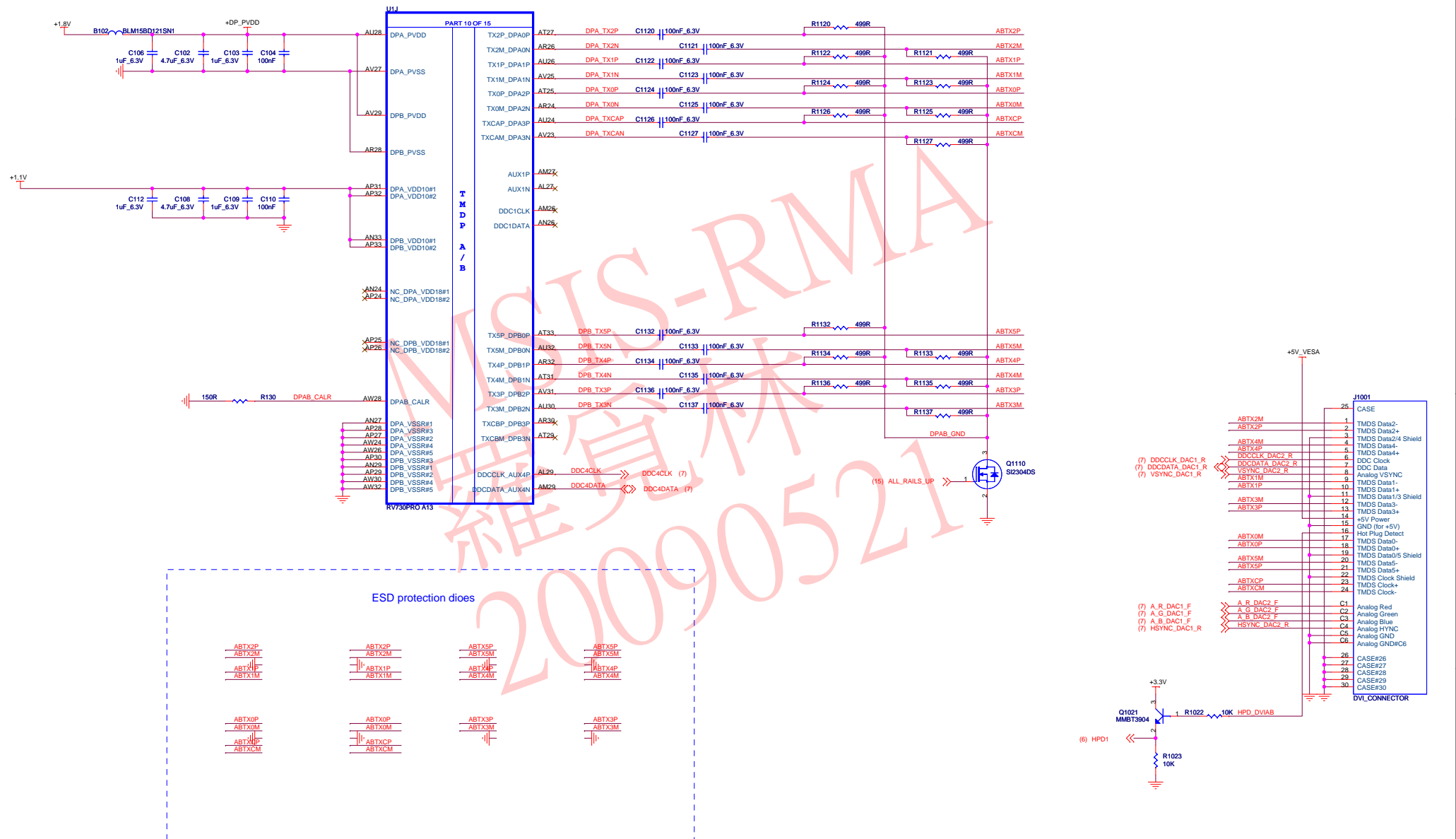


### (07) RV730 DAC1 and DAC2/TV





**(08) RV730 TMDS A&B**



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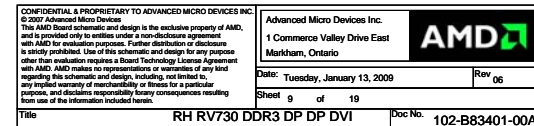
**AMD**

Date: Tuesday, January 13, 2009 Rev 06

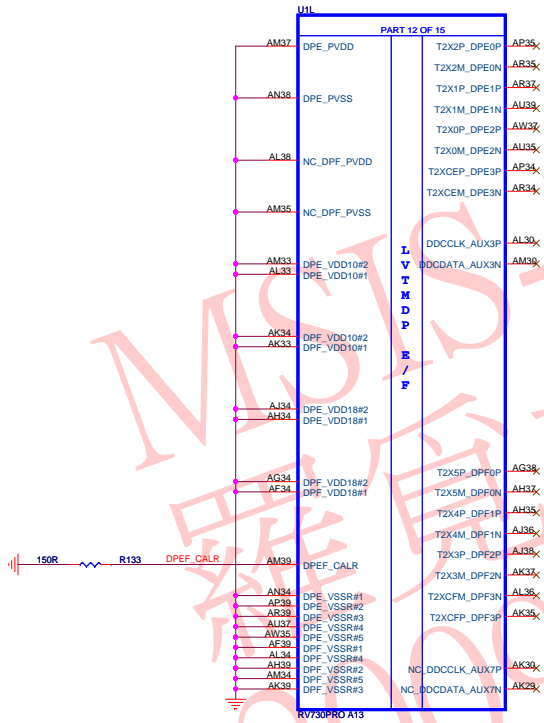
Sheet 8 of 19

Title RH RV770 DDR3 DP DP DVI Doc No: 102-883401-00A

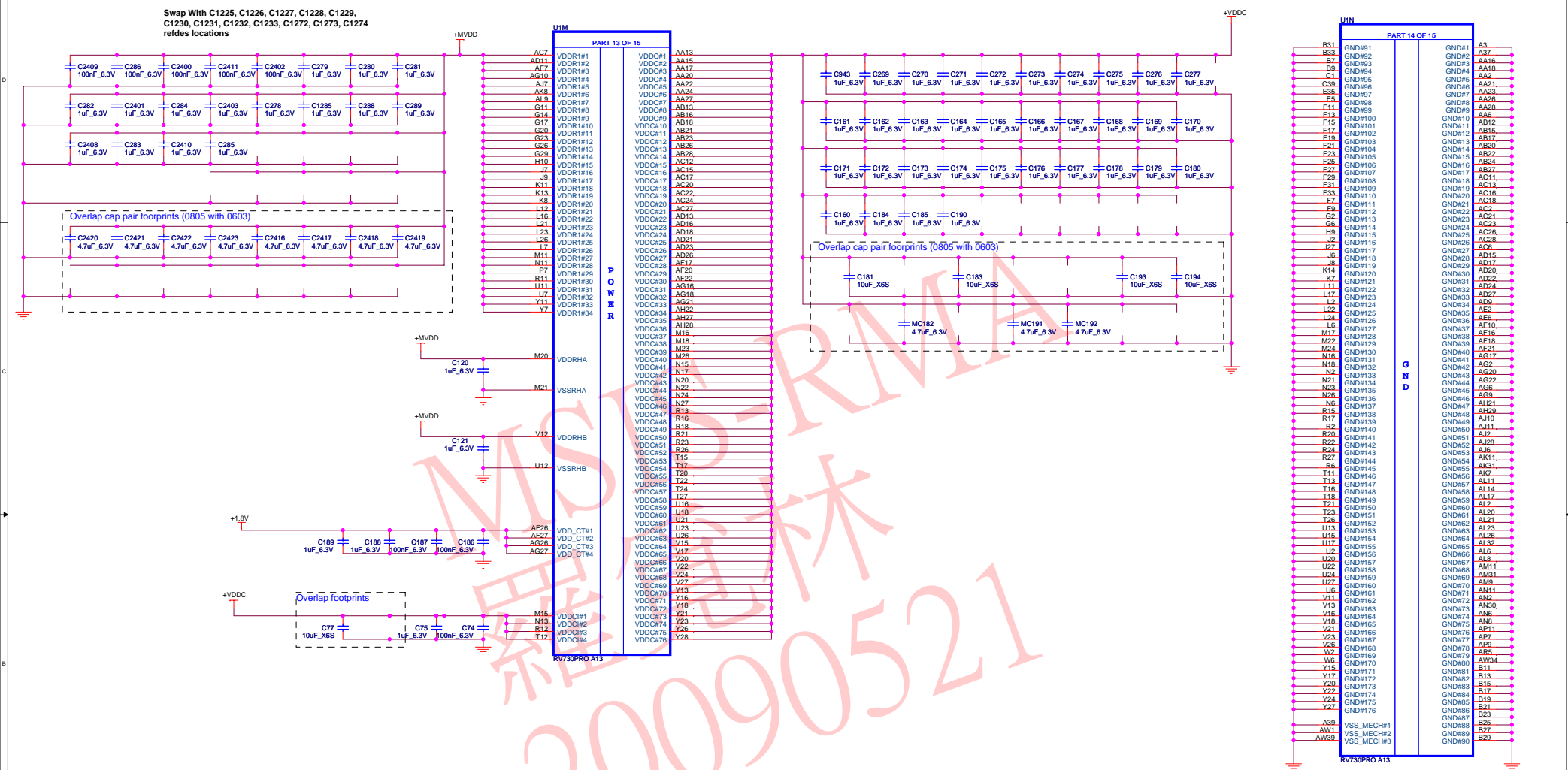




(10) No Connect E&F



## (11) RV730 Power & GND



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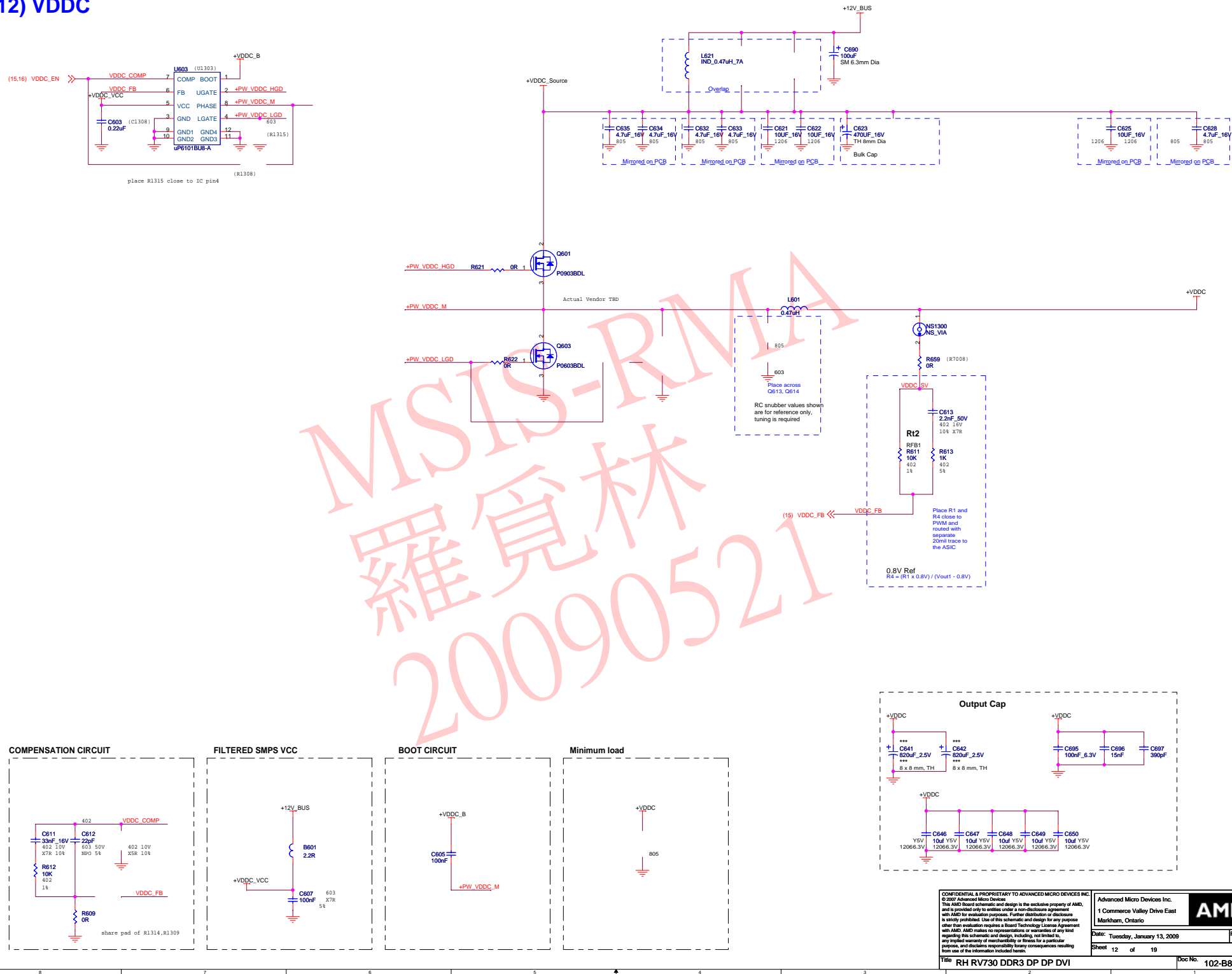
Date: Tuesday, January 13, 2009

Rev 06

Title RH RV730 DDR3 DP DP DVI

Doc No. 102-B83401-00A

## (12) VDDC



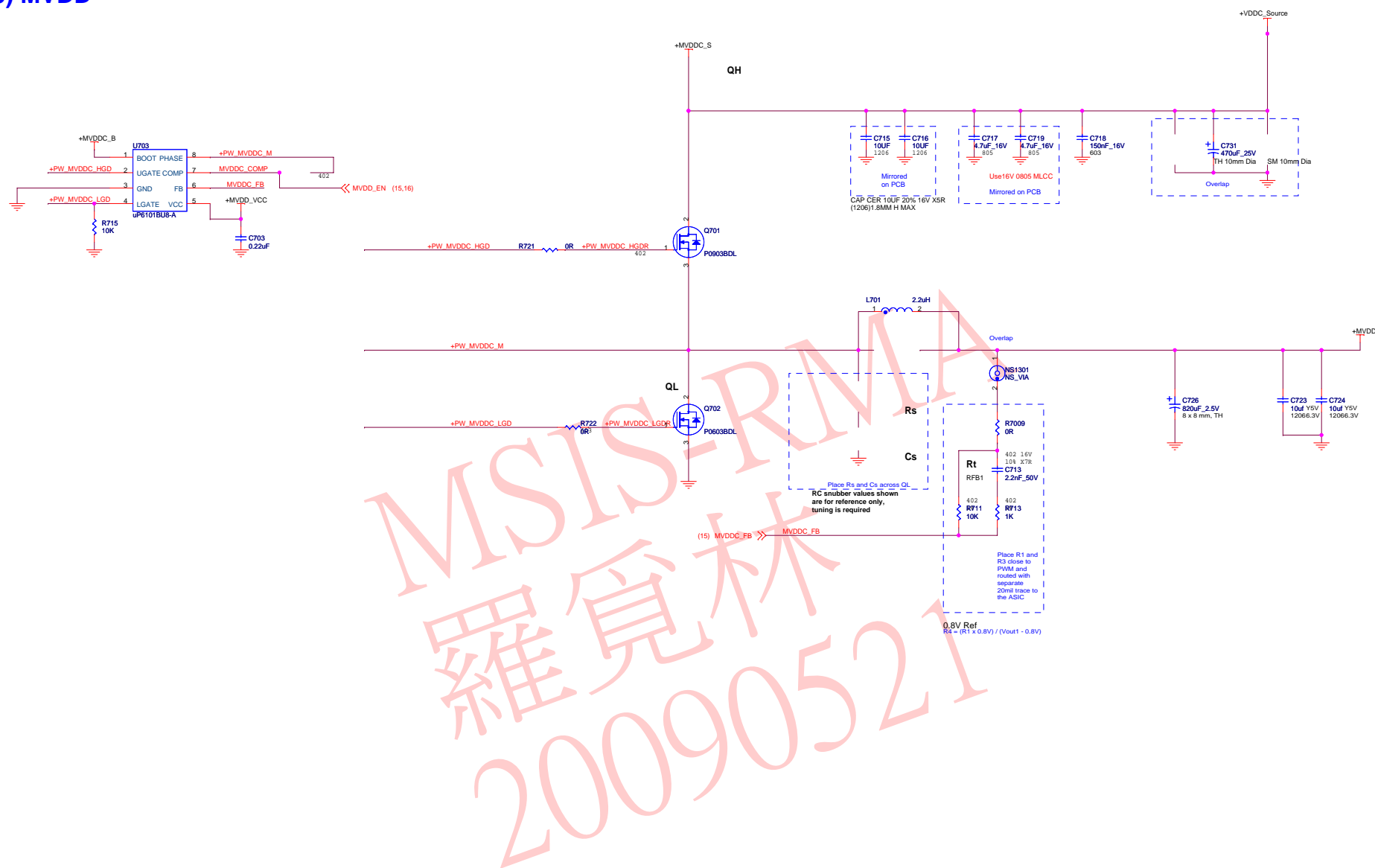
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Rev 06

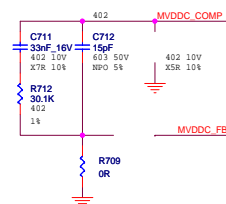


Title: RH RV730 DDR3 DP DP DVI Doc No: 102-B83401-00A

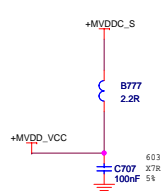
### (13) MVDD



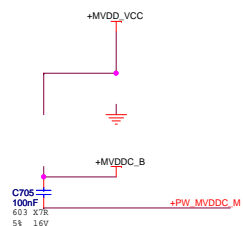
### COMPENSATION CIRCUIT



**FILTERED SMPS VCC**



## BOOT CIRCUIT



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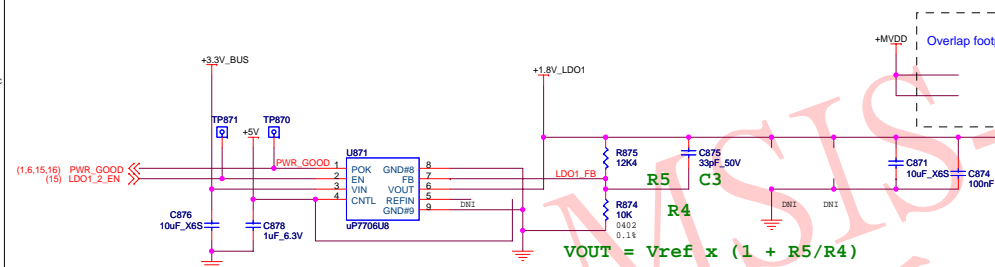
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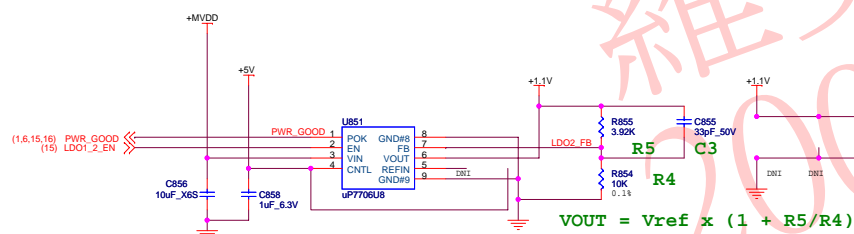
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## (14) Linear Regulators

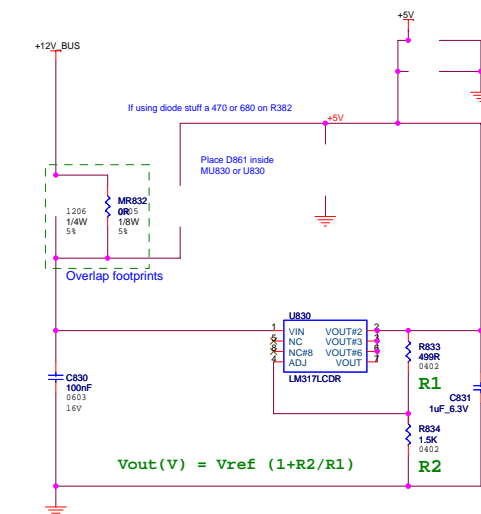
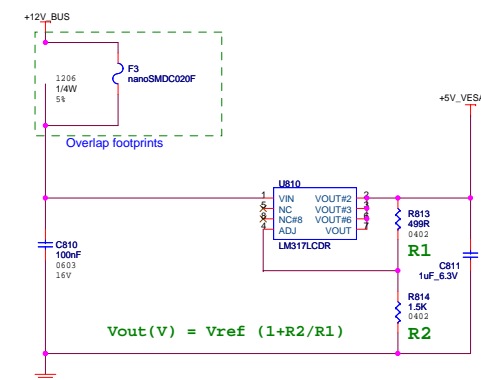
**LDO #1: Vin = 3.0V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 1.0A (TBV) RMS MAX**  
**PCB: 50 to 70mm sq. copper area for cooling**



**LDO #2: Vin = +1.5V to 2.0VMAX    Vout = +1.1V +/- 2%    Iout = 1.7A (TBV) RMS MAX**  
**PCB: 50 to 70mm sq. copper area for cooling**



### Regulators for +5V, +5V\_VESA and +5V\_VESA2



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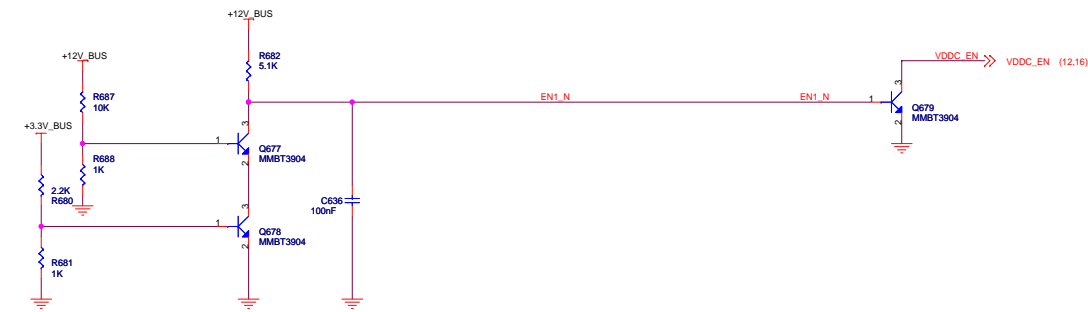
Rev 06

Title RH RV730 DDR3 DP DP DVI

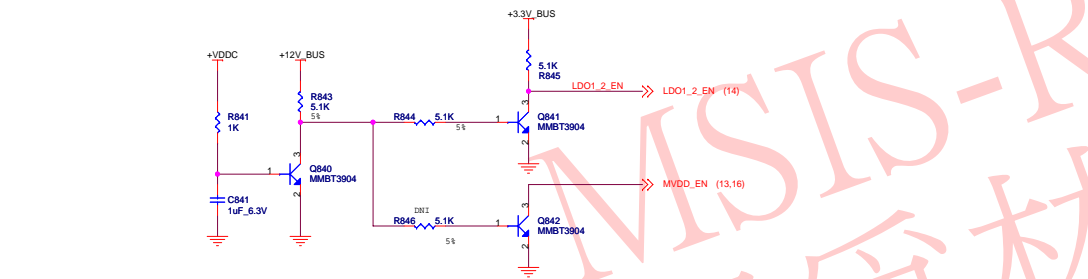
Doc No. 102-B83401-00A

(15) Power Management

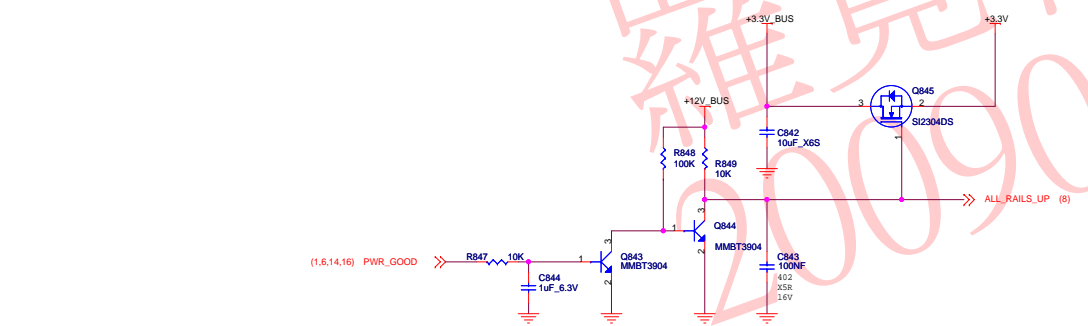
Power up Sequencing



VDDC Enable Circuit



LDOs and MVDD Enable Circuit

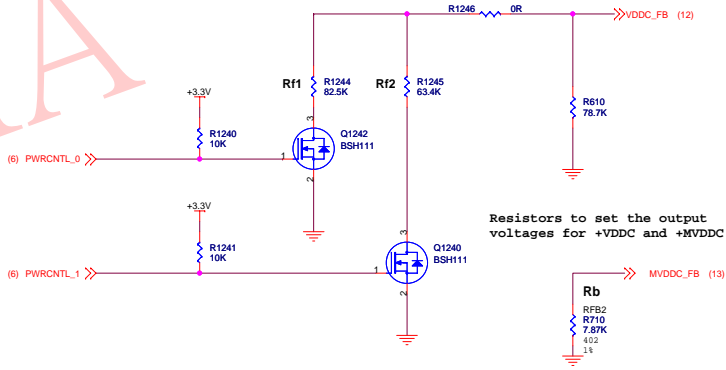


3.3V Enable Circuit

Power Play

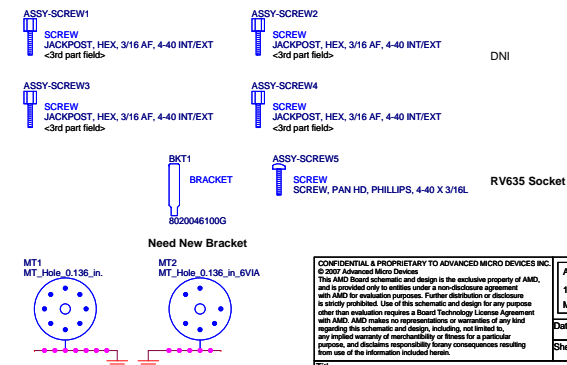
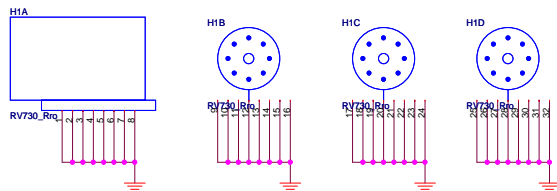
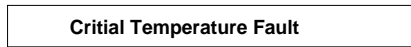
VDDC Voltage Settings Using GPIOs (for VDDC1 Dual Phase)					
PWRCTRL_1 GPIO_20	PWRCTRL_0 GPIO_15	Output Voltage (V)		R1=	
		R1=42.2K	R2=20.5K	R1=	R2=
0	0	0.90V			
0	1	1.00V			
1	0	1.15V			
1	1	1.25V			

Vout = Vref \* (1+Rt/Rb)  
VDDC2 (Single Phase): Vref = 0.8V, Rt = 10K  
MVDDC (Single Phase): Vref = 0.8V, Rt = 10K



Resistors to set the output voltages for +VDDC and +MVDDC





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<p><b>Title</b> RH RV730 DDR3 DP DP DVI</p>	<p><b>Date:</b> Tuesday, January 13, 2009 <b>Rev</b> 06  <b>Sheet</b> 16 of 19 <b>Doc No.</b> 102-B38401-00A</p>

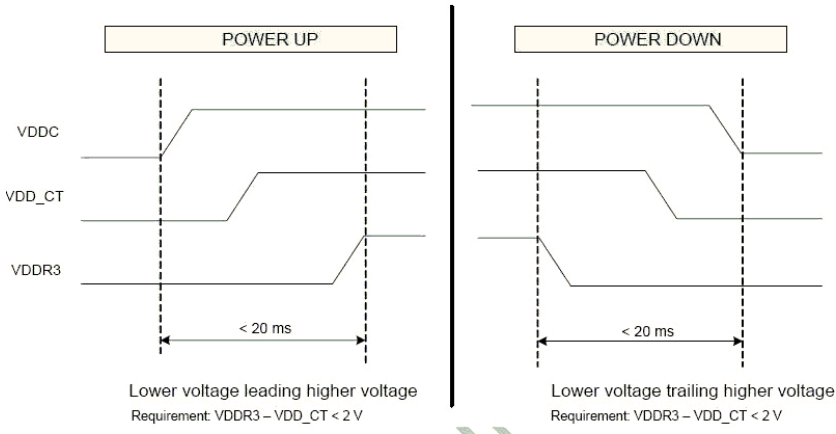
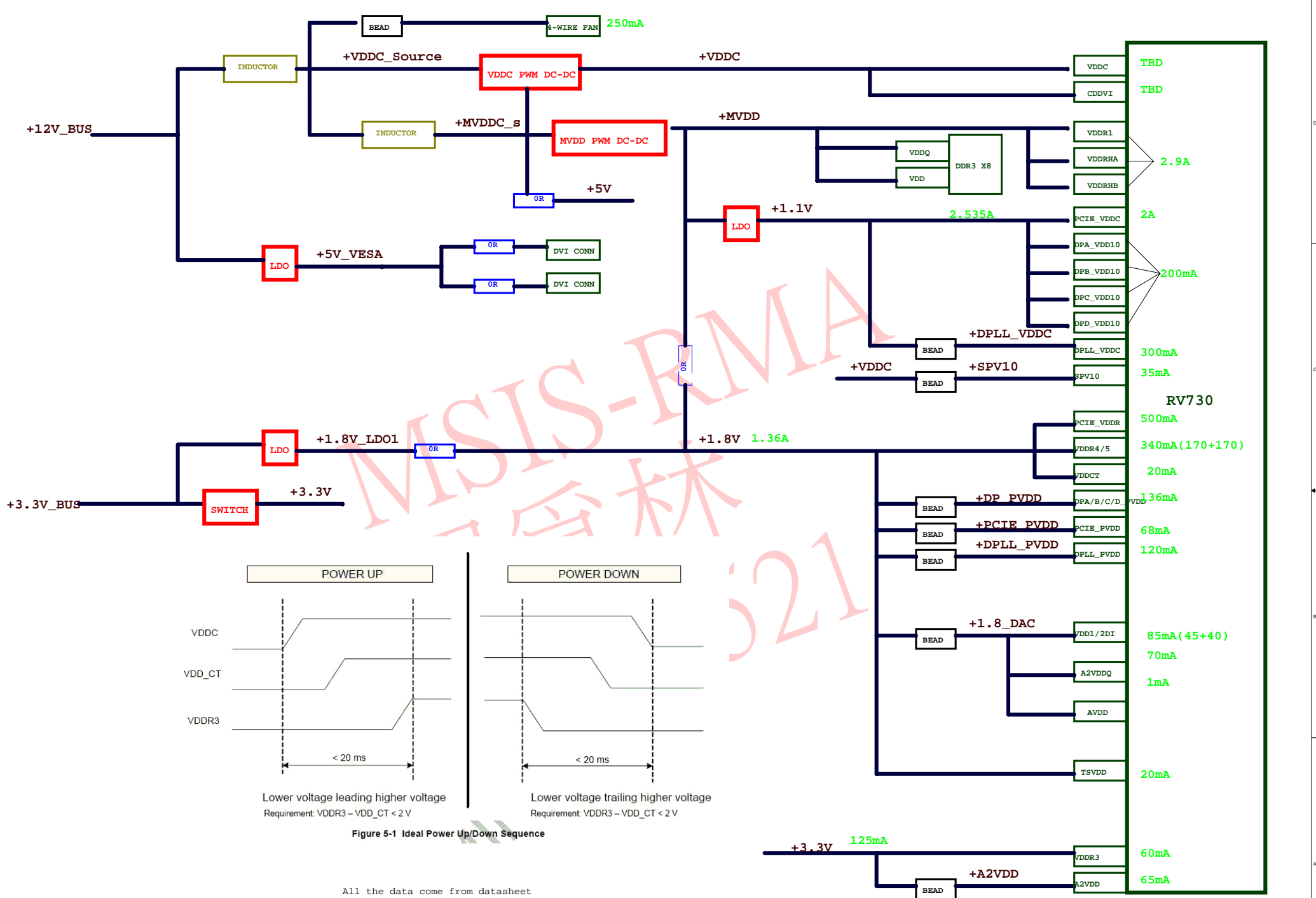
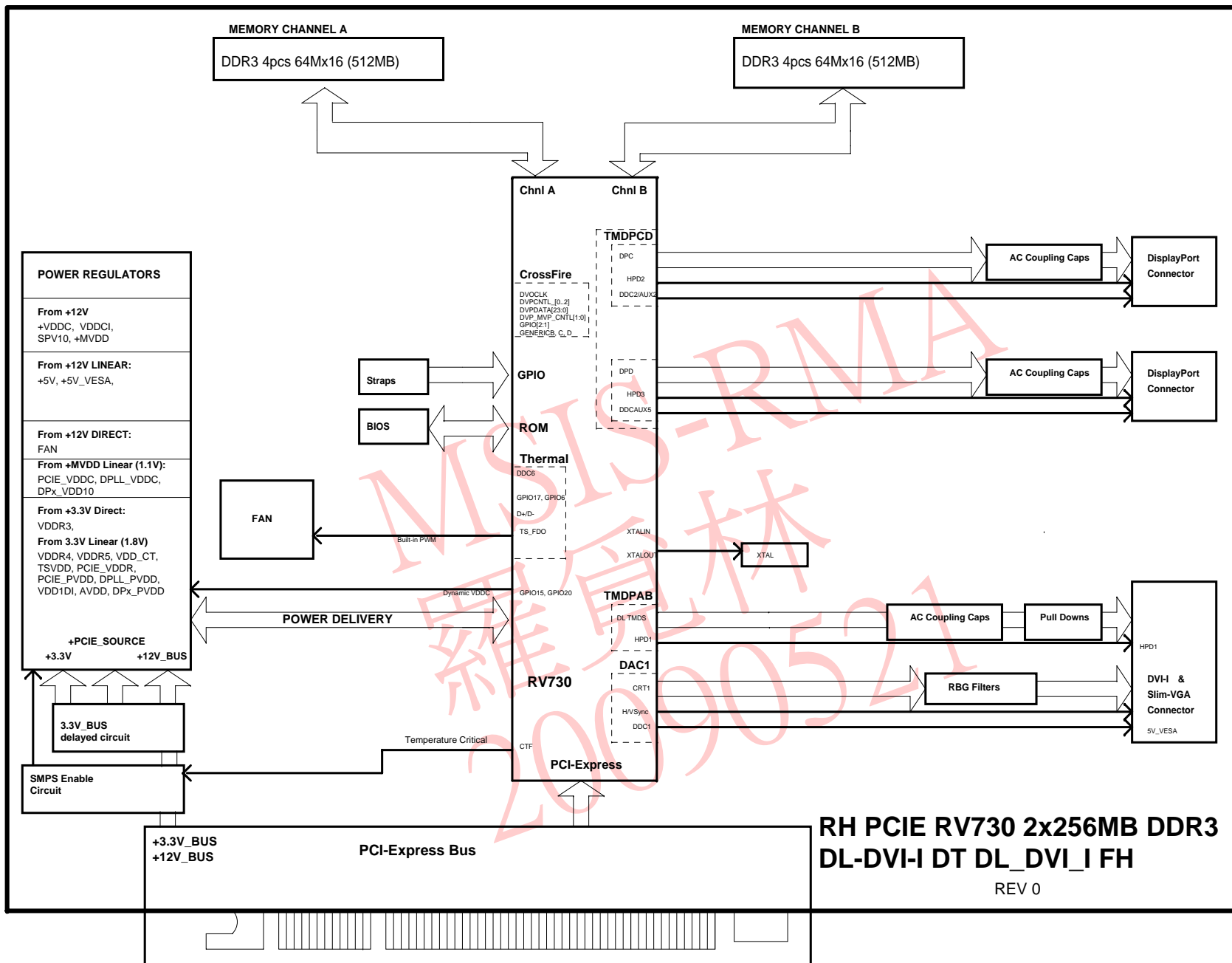


Figure 5-1 Ideal Power Up/Down Sequence

All the data come from datasheet



**RH PCIE RV730 2x256MB DDR3  
DL-DVI-I DT DL\_DVI\_I FH**  
REV 0

<div>AMD</div>			Title			Schematic No.		Date:	
			RH RV730 DDR3 DP DP DVI			102-B83401-00A		Tuesday, January 13, 2009	
			REVISION HISTORY					NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.	
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION						
0	00A	08/11/11	Initial design for RV730 DDR3						
			<div>MSIS-RMA</div> <div>羅覓林</div> <div>20090521</div>						