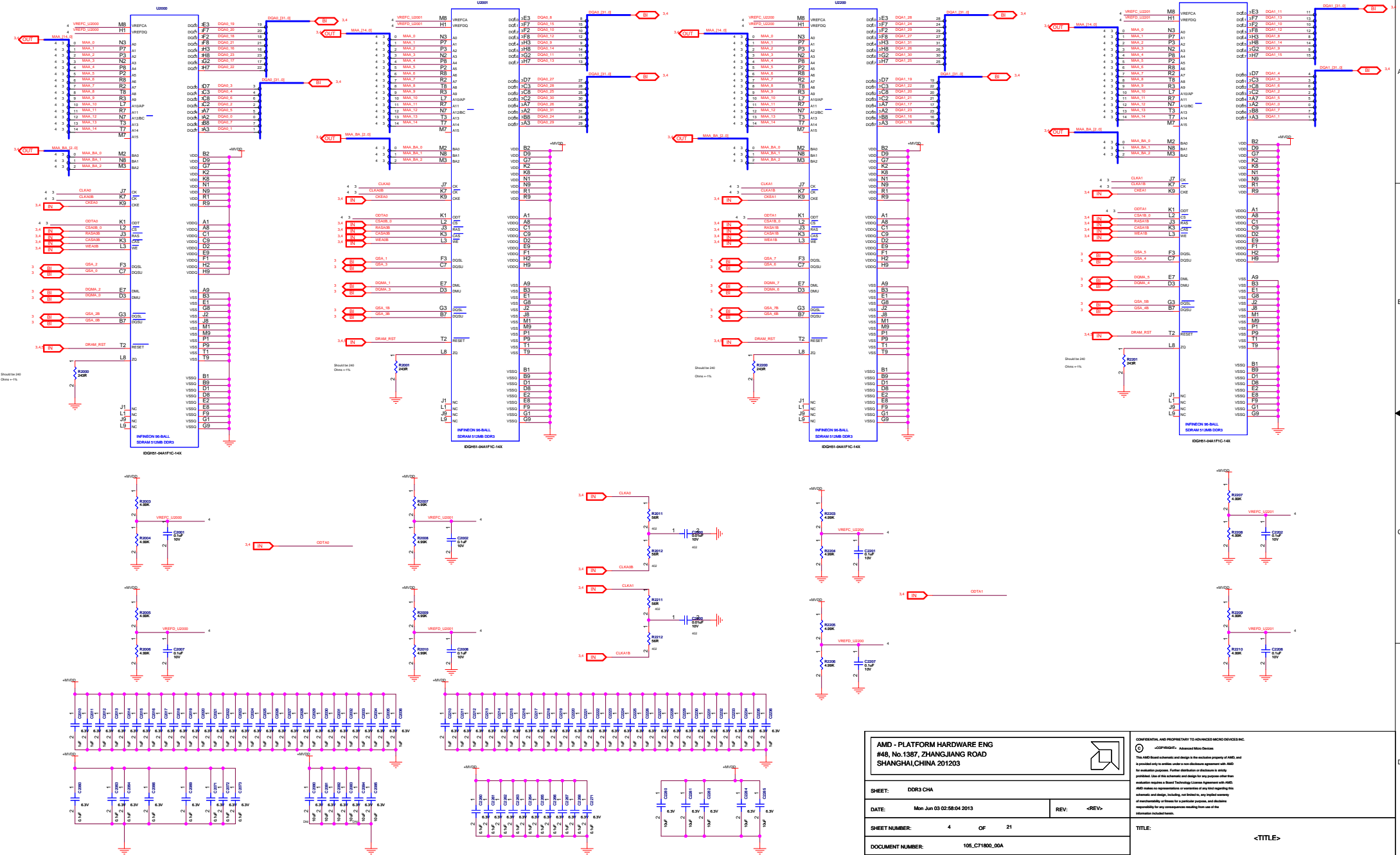


#### (4) DDR3 Memory Channel A



AMD - PLATFORM HARDWARE EN  
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SHANGHAI,CHINA 201203

SHEET: DDR3 CHA

DATE: Mon Jun 03 02:58:04 2013

SHEET NUMBER: 4 OF

DOCUMENT NUMBER:

NOTES:	NOTE
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**TITLE:**

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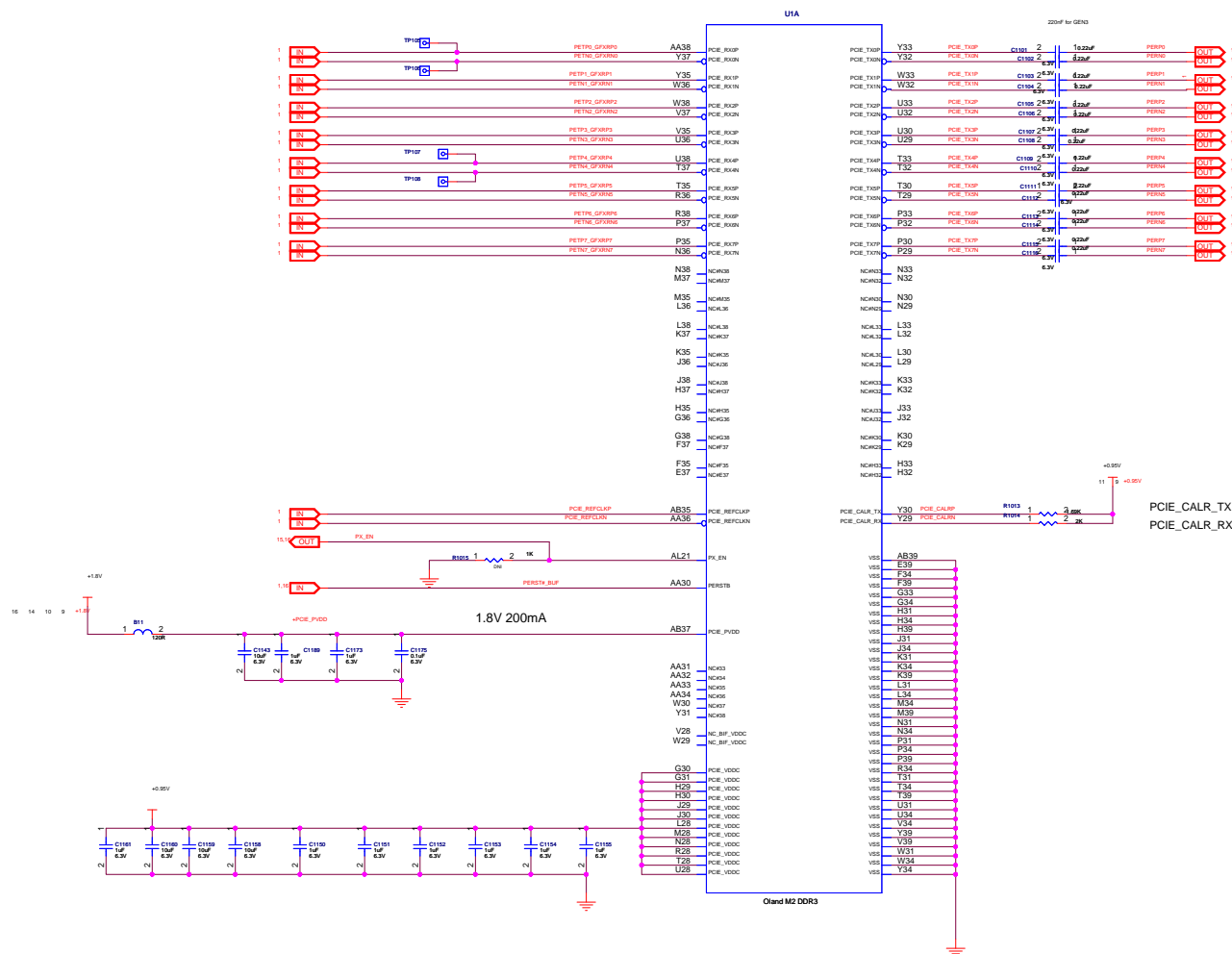
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
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## Oland M2 PCIe Interface

NOTE: Some of the PCIE testpoints will be available through vias on traces.



PCIE\_CALR\_TX 1.69k pull up for Oland  
PCIE\_CALR\_RX 1k pull up for Oland

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<p>SHEET:      Oland PCIe Interface</p>		<p>DATE:      Mon Jun 03 02:58:09 2013      REV:      &lt;REV&gt;</p>	
<p>SHEET NUMBER:      2      OF      21</p>		<p>TITLE:</p>	
<p>DOCUMENT NUMBER:      105_C71800_00A</p>		<p>&lt;TITLE&gt;</p>	
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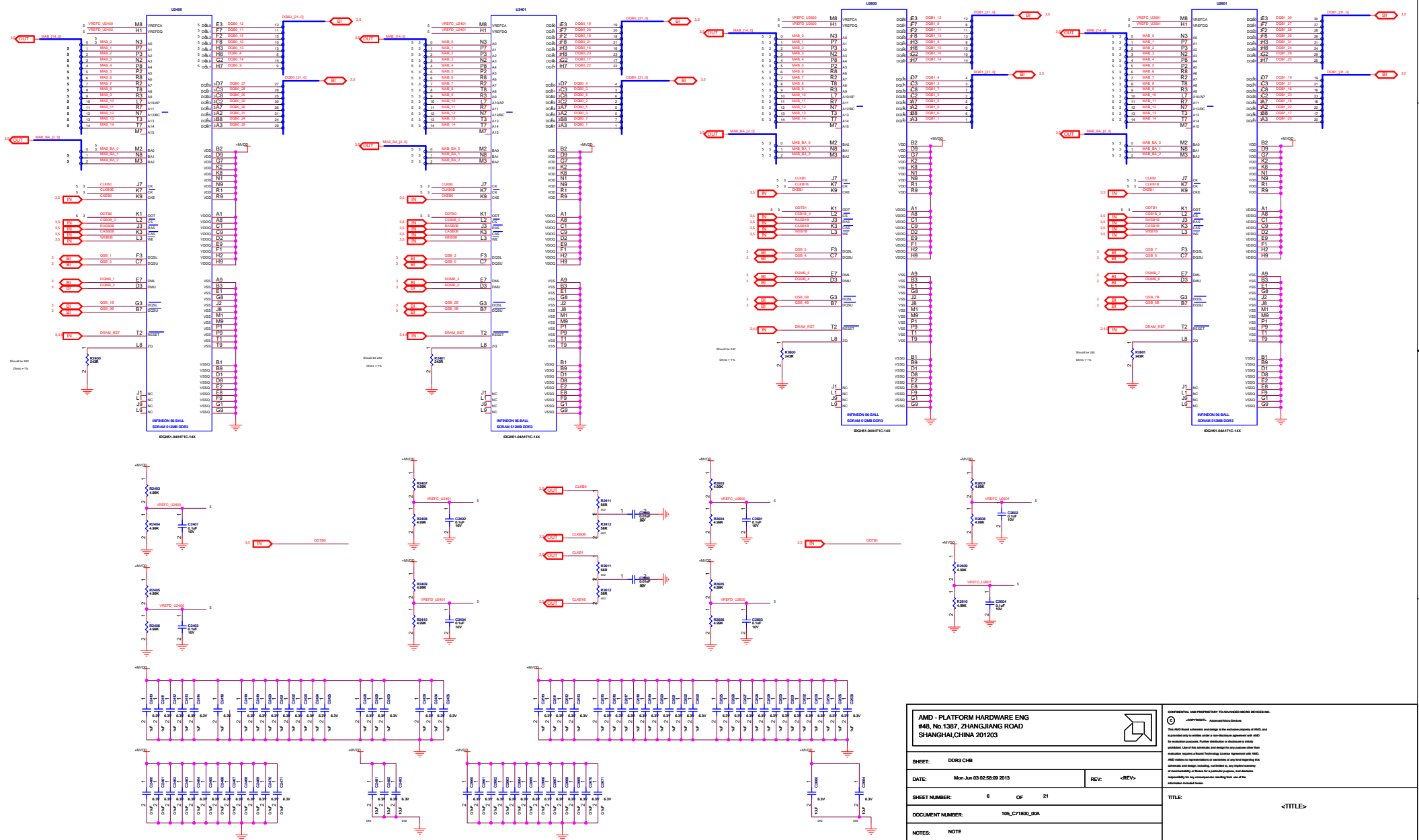


&lt;TITLE&gt;

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100

(5) DDR3 Memory Channel B



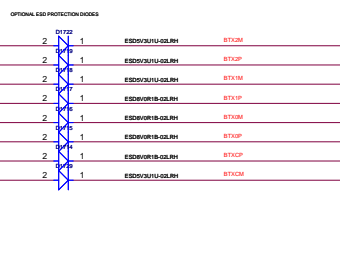
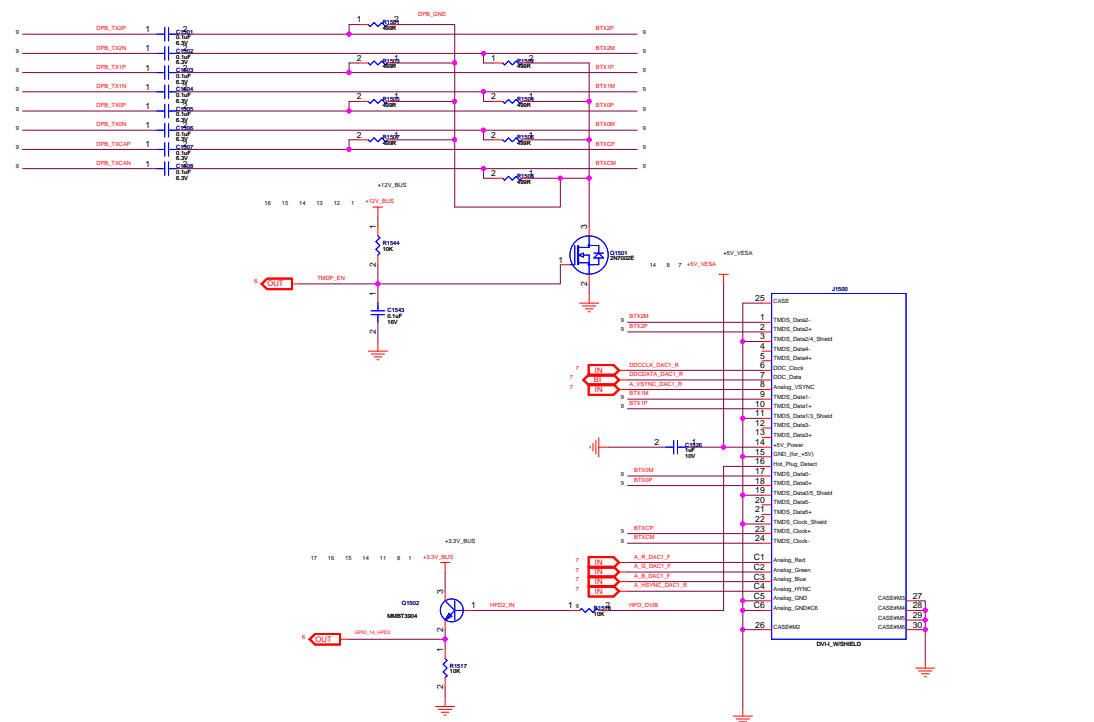
<p>RE32P10D2</p> <p>Internal use only. Other logic must not affect these signals during RE32P.</p>	
<p>AUD[1]</p> <p>AUD[0]</p>	<p>HG1NC</p> <p>VS1NC</p>
<p>AUD[2:0]</p> <p>00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.</p> <p>HDMI must only be enabled on systems that are legally entitled to use HDMI.</p> <p>- It is the responsibility of the system designer to ensure that the system is entitled to support this feature</p>	

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<p><b>SHEET:</b>      <b>Stand Onlap STRIP PLL</b></p>		<p><b>DATE:</b>      <b>Mon Jun 03 05:58:09 2013</b></p>	
<p><b>SHEET NUMBER</b>      <b>6</b>      <b>OF</b>      <b>21</b></p>		<p><b>REV:</b>      <b>&lt;REV&gt;</b></p>	
<p><b>DOCUMENT NUMBER:</b>      <b>106_C71803_00A</b></p>		<p><b>TITLE:</b>      <b>&lt;TITLE&gt;</b></p>	
<p><b>NOTES:</b>      <b>NOTE</b></p>		<p><b>NOTES:</b>      <b>NOTE</b></p>	









&lt;TITLE&gt;

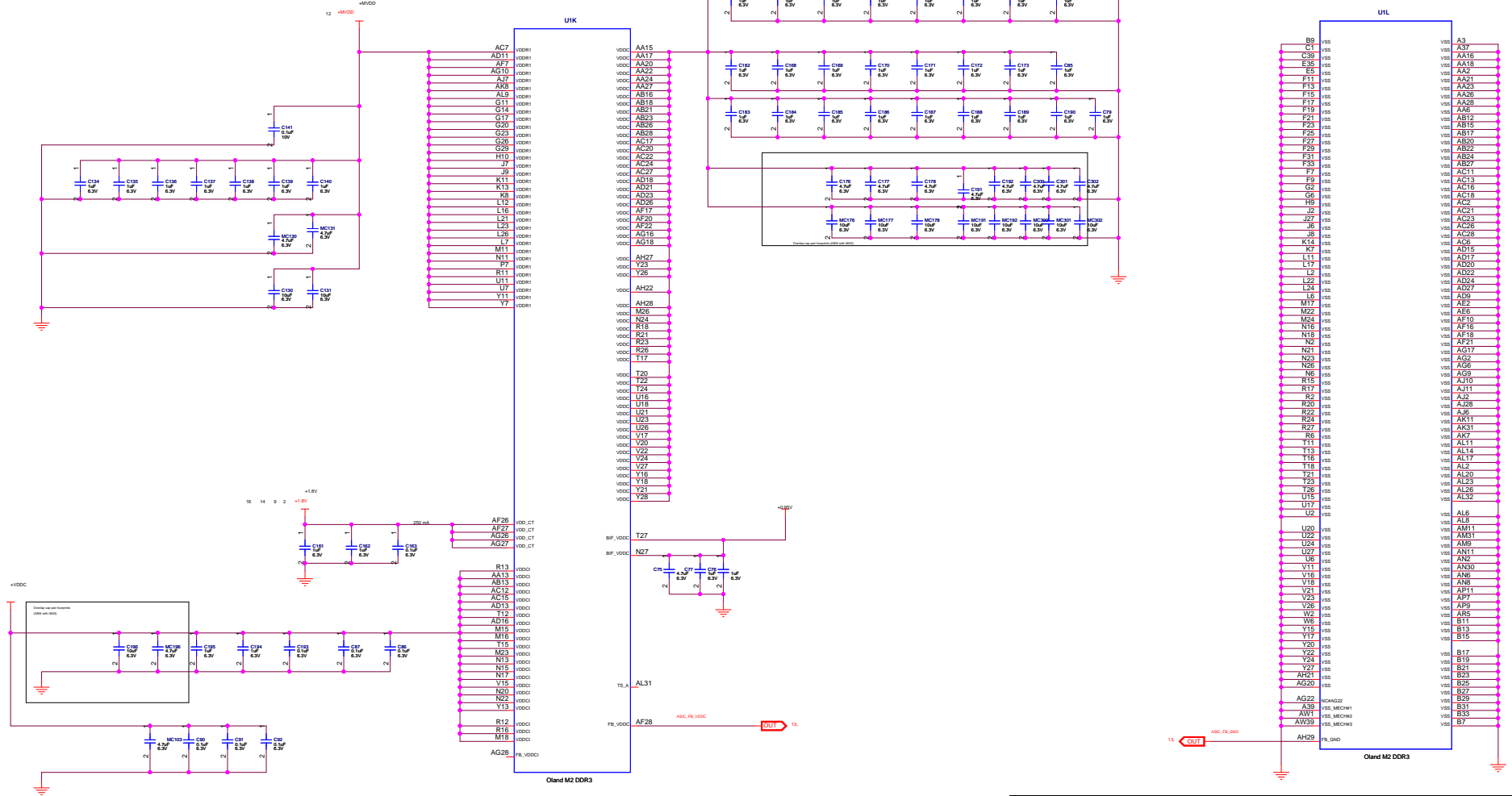
TIME:

**<TITLE>**

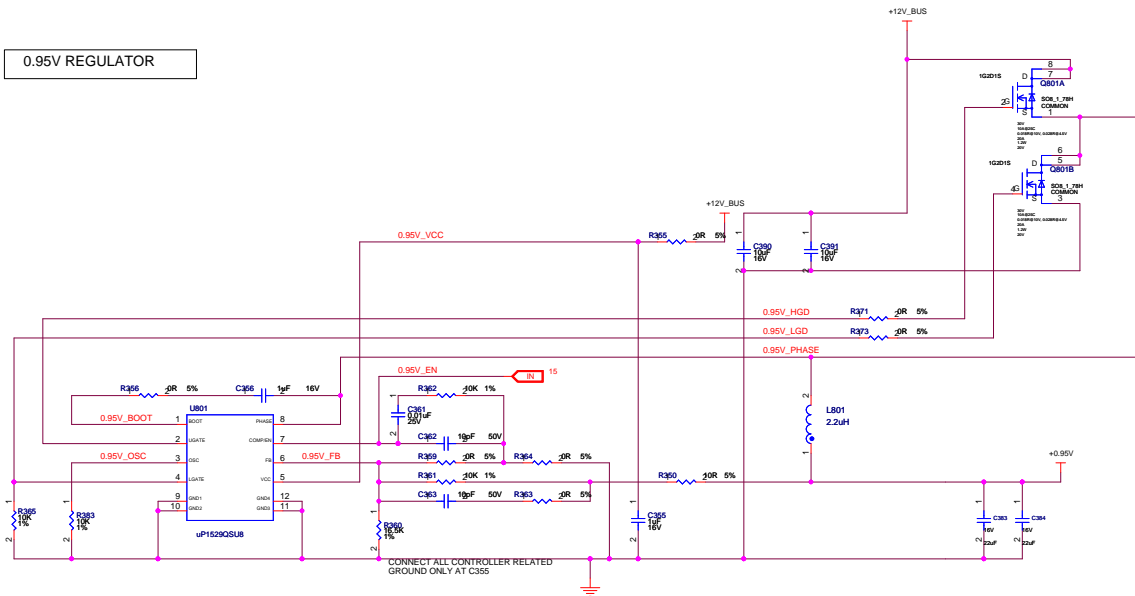
STILL


NOTES:	NOTE
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# Oland M2 Power & GND



0.95V REGULATOR



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SHEET NUMBER: 11 OF 21		DOCUMENT NUMBER: 105_C71800_00A		TITLE: <TITLE>	
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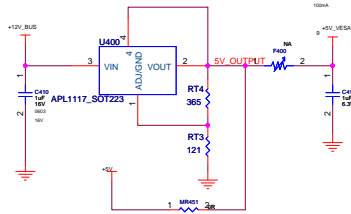
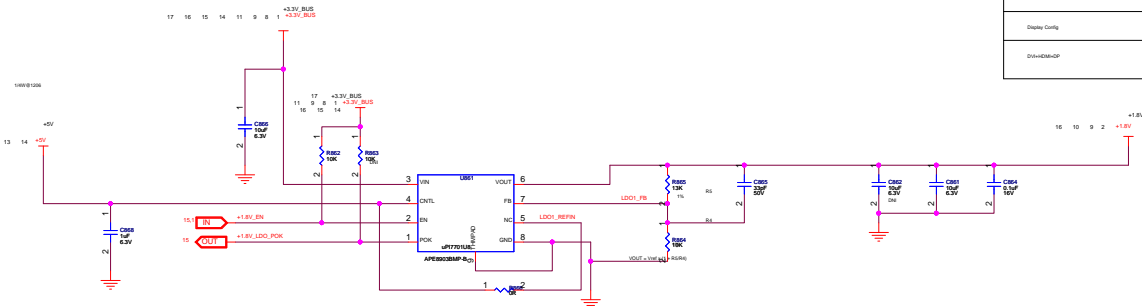


Linear Regulators

LDO #1:	$V_{in} = 3.00V \text{ to } 3.60V \text{ (3.3V } \pm 5\%)$	$V_{out} = +1.8V \pm 2\%$	load = 1.6A (TYP) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling			

Regulators for +5V, +5V_VESA and +5V_VESA2
--

1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVA+DM-QP	1580mA



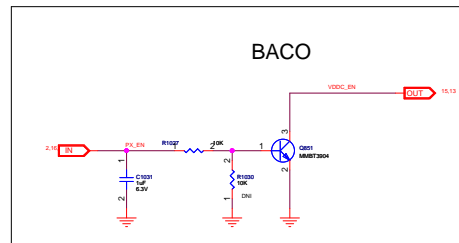
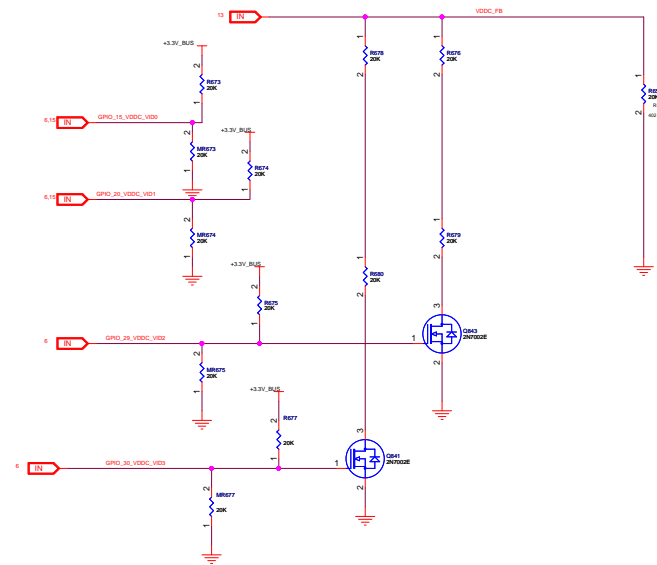
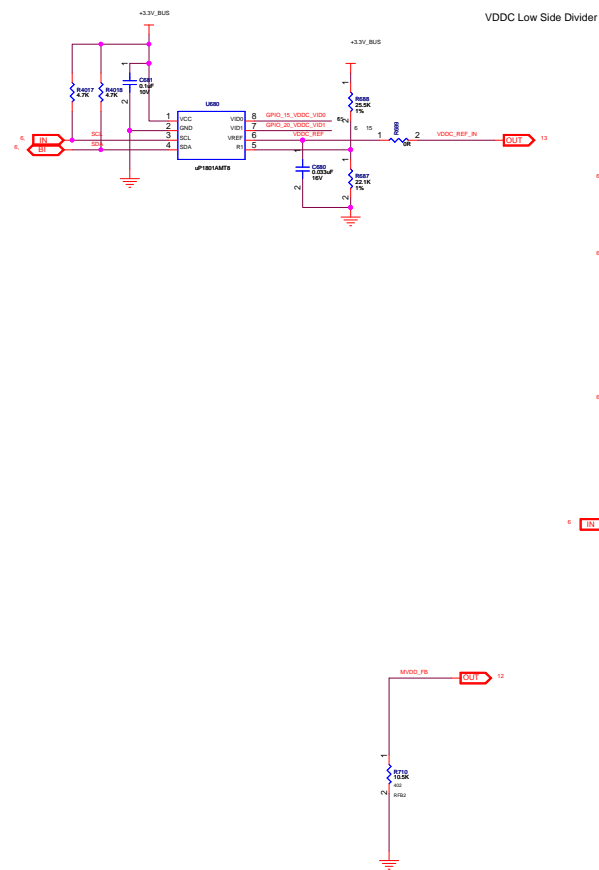
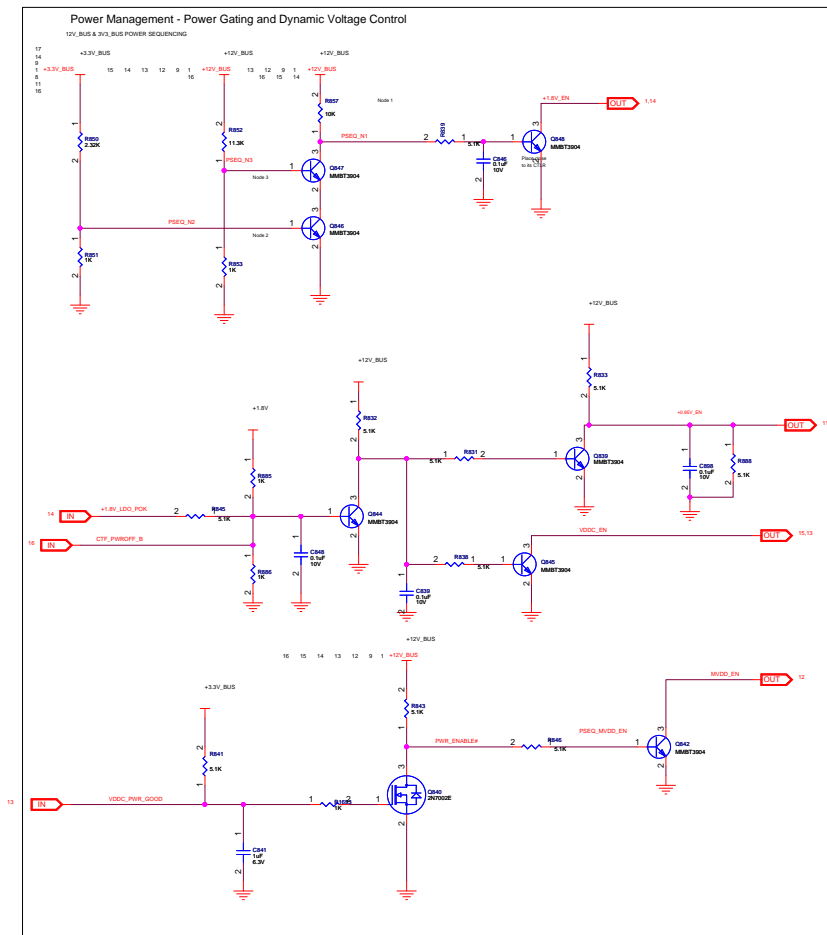
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


SHEET:	Linear Regulators	
DATE:	Mon Jun 03 02:58:09 2013	REV: <REV>
SHEET NUMBER:	14	OF 21
DOCUMENT NUMBER:	108_C71800_00A	
NOTES:	NOTE	

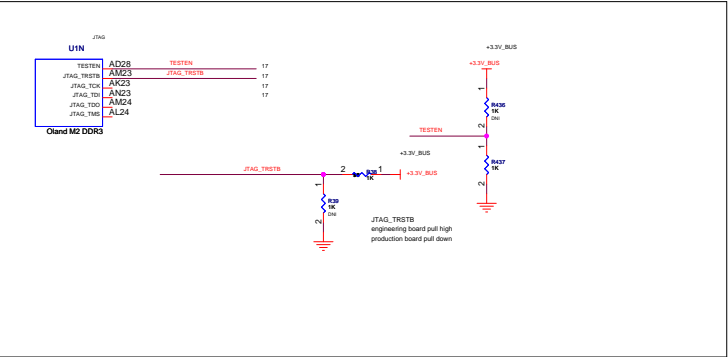
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TITLE: <TITLE>



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DATE: Mon Jun 03 02:58:09 2013		REV: <REV>		TITLE:	
SHEET NUMBER: 15 OF 21				<TITLE>	
DOCUMENT NUMBER: 106_C71800_00A					
NOTES: NOTE					

(19) Debug Circuits

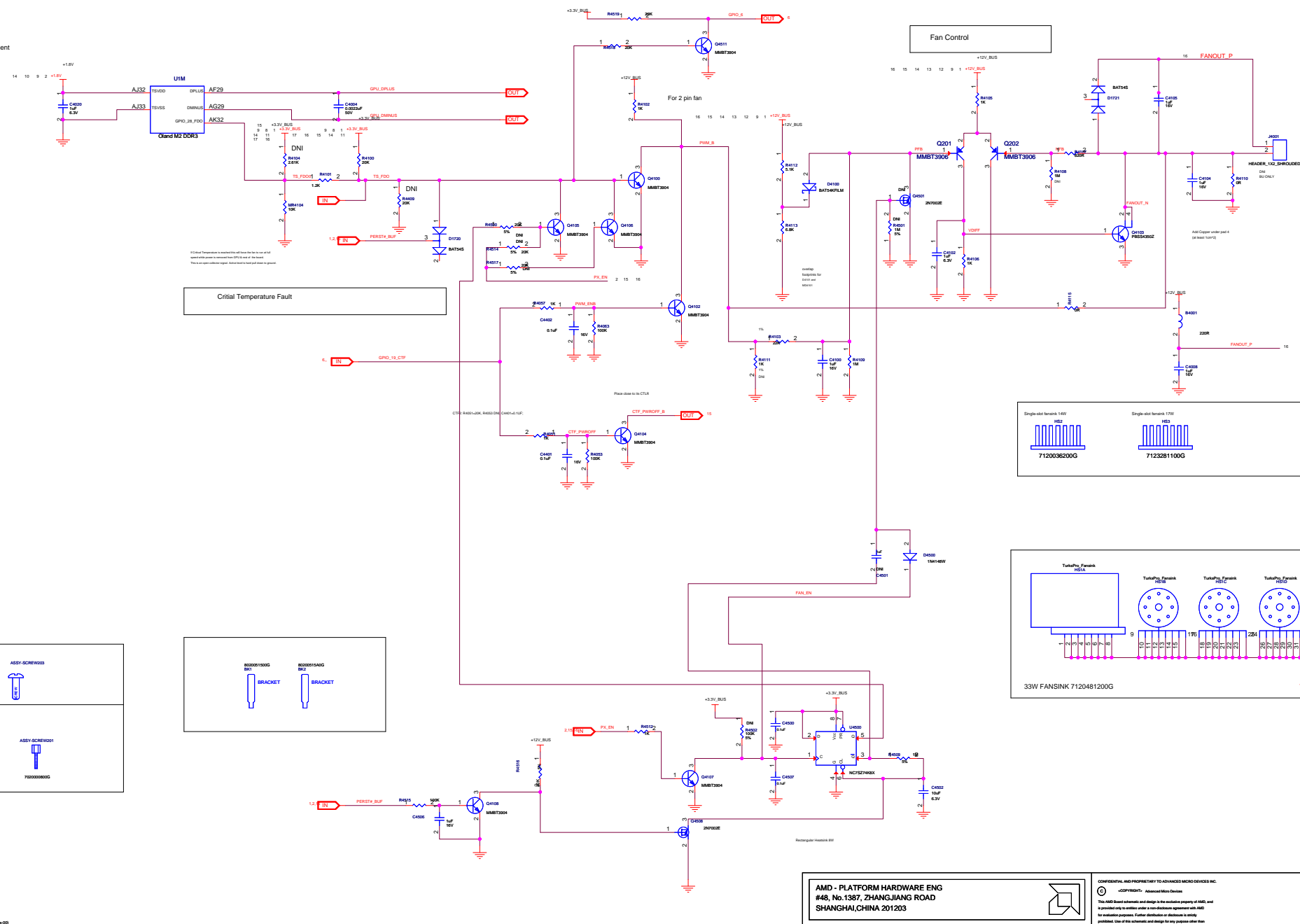


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DATE: Mon Jun 03 02:58:09 2013			REV: <REV>					
SHEET NUMBER: 17 OF 21						TITLE: <TITLE>		
DOCUMENT NUMBER: 105_C71800_00A								
NOTES: NOTE								
6			7			8		









REV: 4.0 REV: 4.0

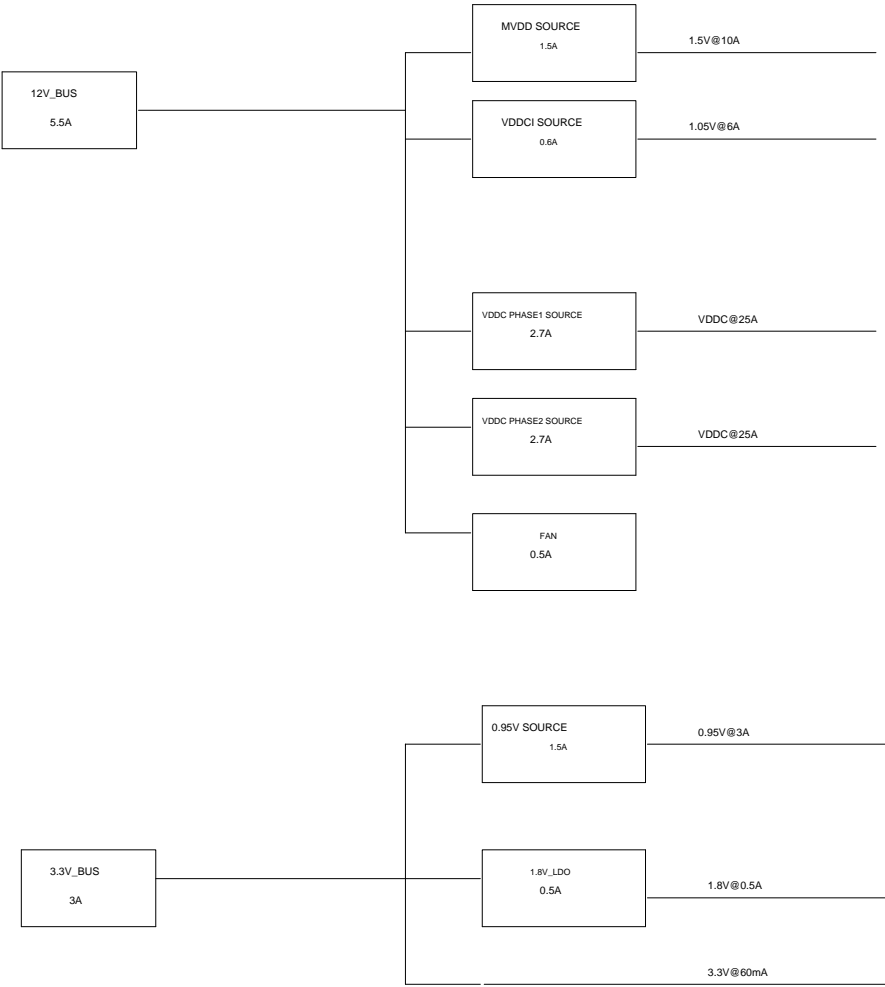
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DATE	TIME	LOCATION	ATTENDANCE	REMARKS
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10/12/2019	10:00 AM	...	...	...
10/13/2019	10:00 AM	...	...	...
10/14/2019	10:00 AM	...	...	...
10/15/2019	10:00 AM	...	...	...
10/16/2019	10:00 AM	...	...	...
10/17/2019	10:00 AM	...	...	...
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10/30/2019	10:00 AM	...	...	...
10/31/2019	10:00 AM	...	...	...

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DMA1	HPD2	DDCAUX2
HDMI0P	HPD1	DDCAUX1

GPIO15	VDDC_VD9	
GPIO20	VDDC_VD1	
GPIO28	VDDC_VD2	
GPIO30	VDDC_VD3	
GPIO21	MVDD_VD	



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SHEET: GPIO DDC HPD map			REV: <REV>			TITLE:  <TITLE>		
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SHEET NUMBER: 18 OF 21								
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