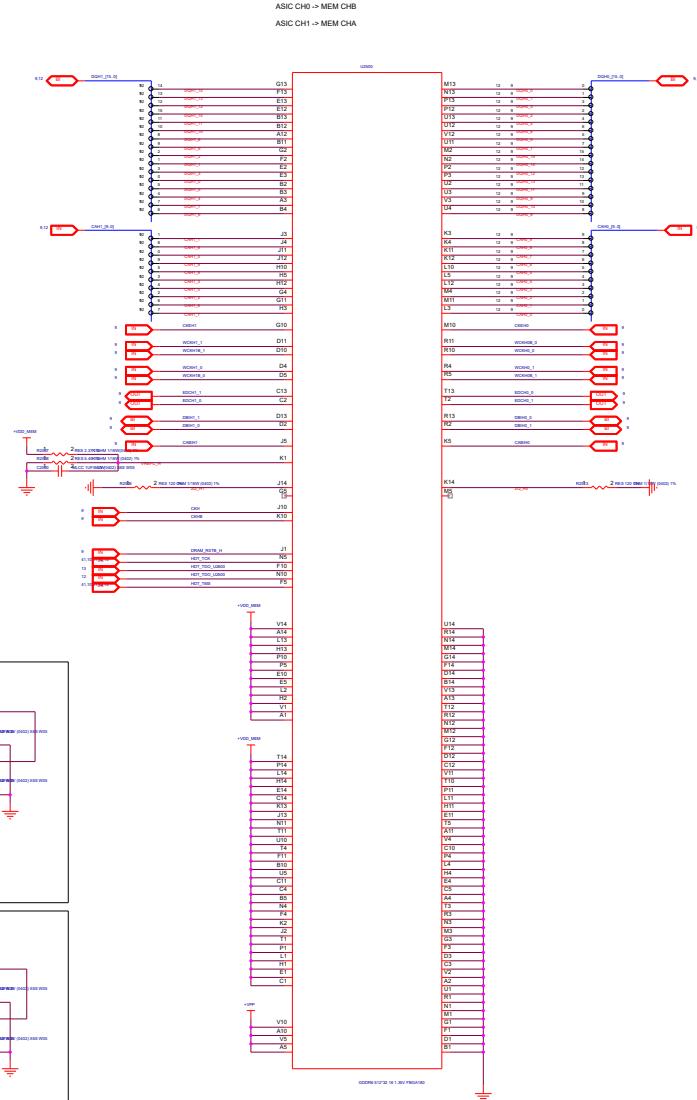
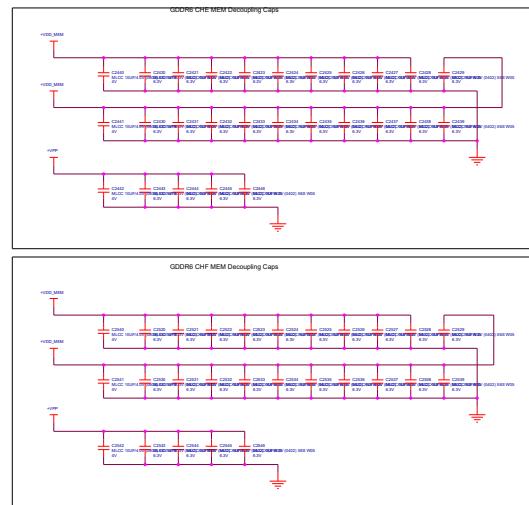
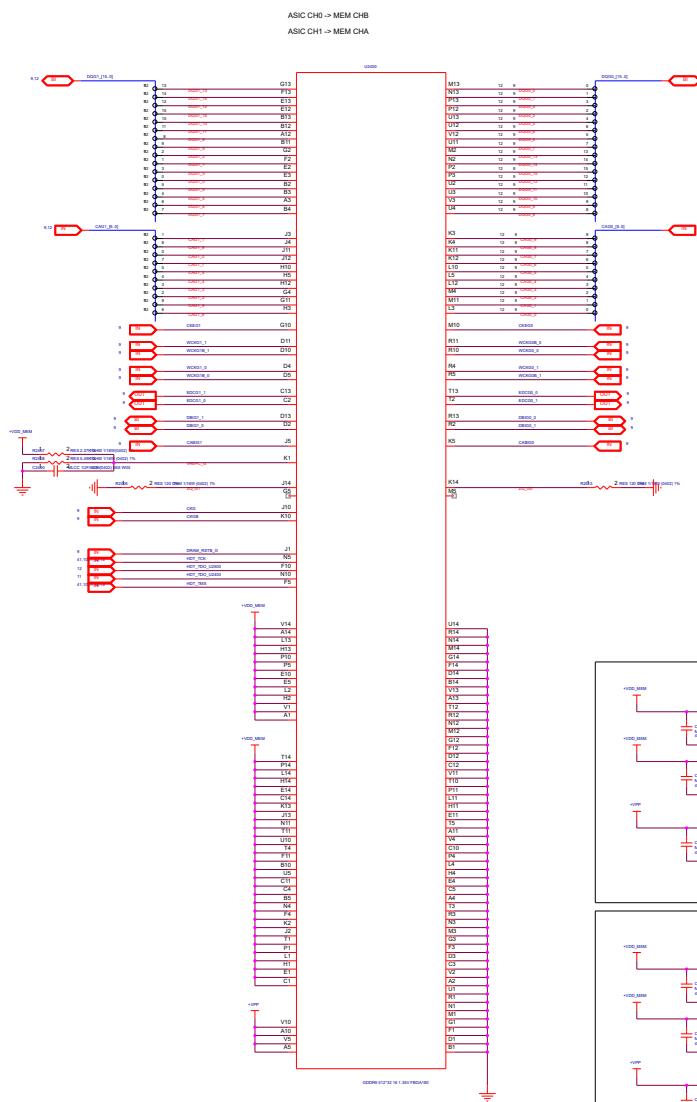
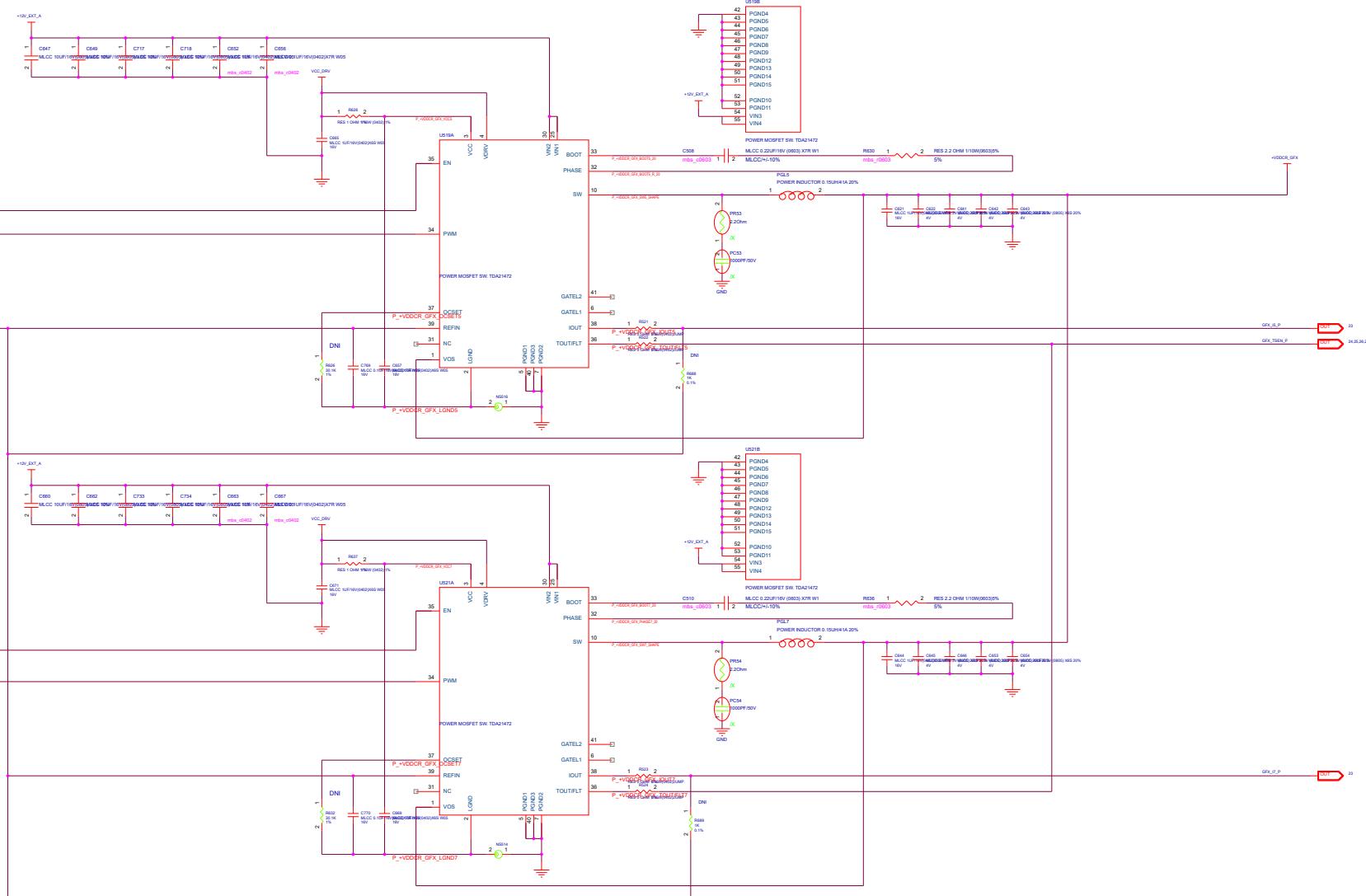
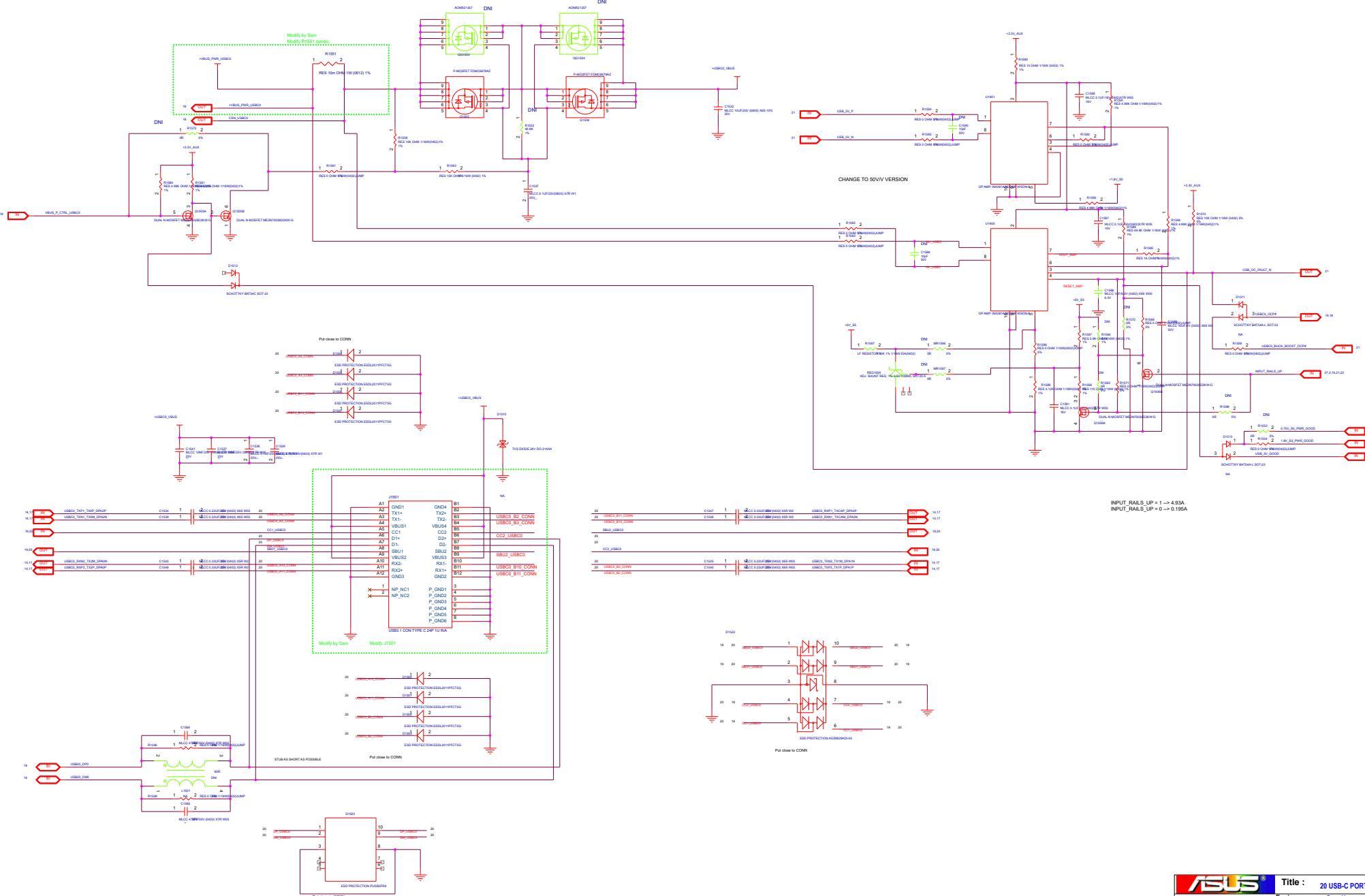


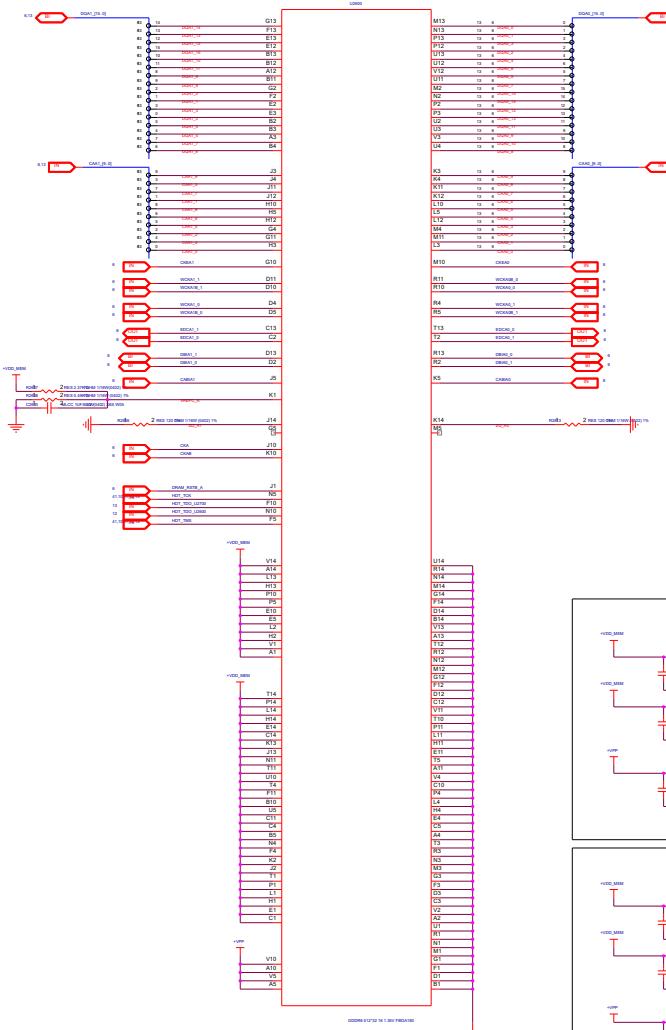
CCG5	Navi10	Note
SCB1	SDA/SCL	Firmware update/SMU
SCB2	USBDP_I2C_SLAVE_SDA/SCL	
SCB2	USBC_VR_SDA/SCL	Navi10 MUX/PD_Regulator/re-driver
SCB3	USBDP_I2C_MASTER_SDA/SCL	UCSI



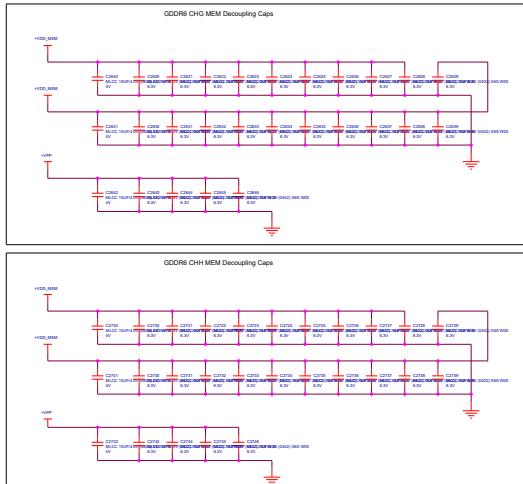
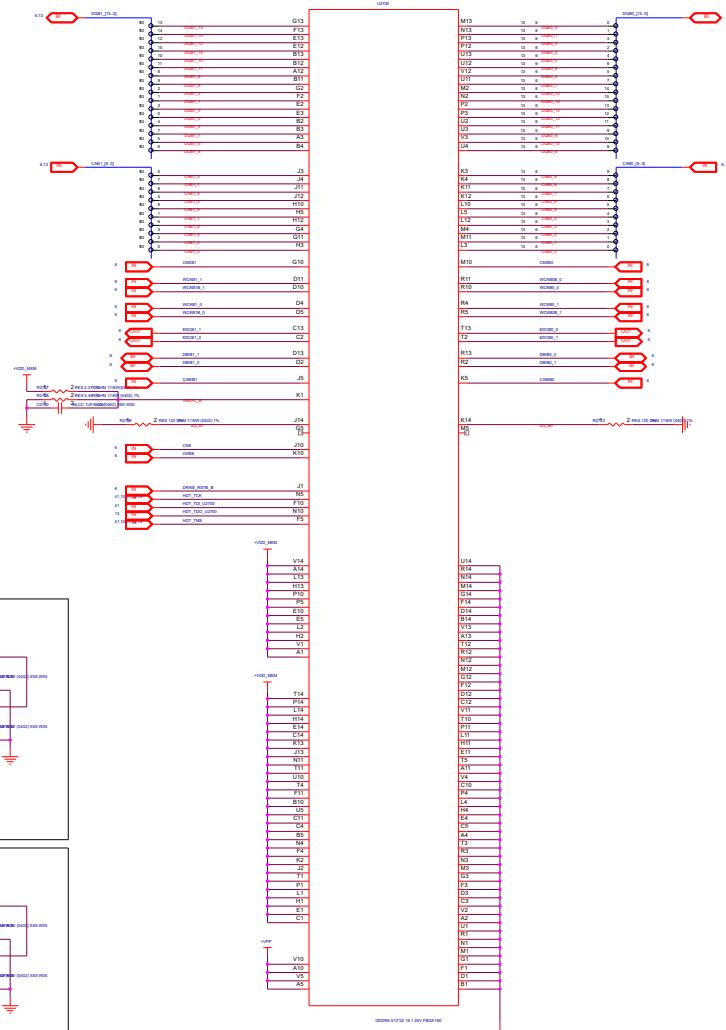


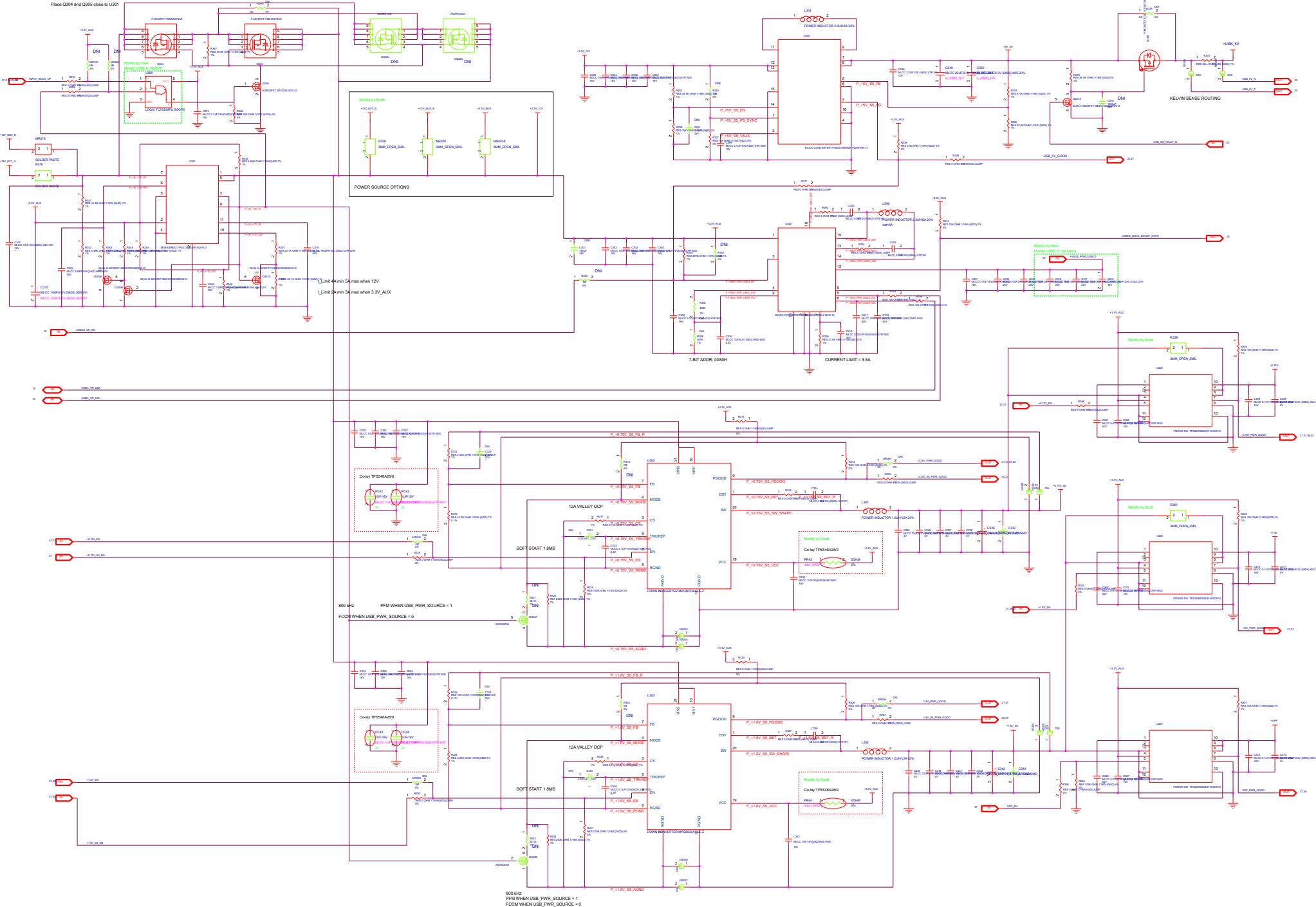


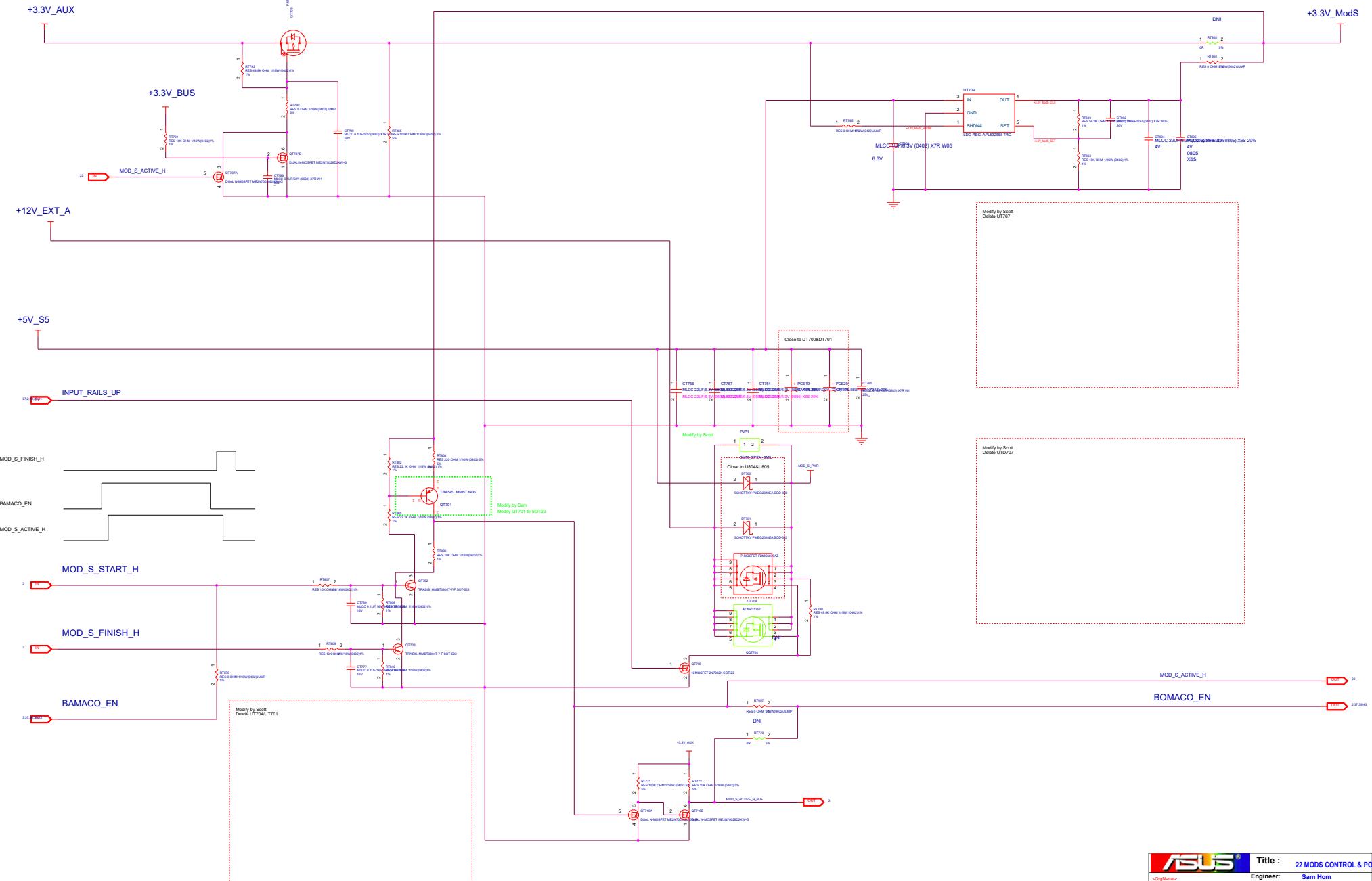
ASIC CH0 → MEM CHB
ASIC CH1 → MEM CHA

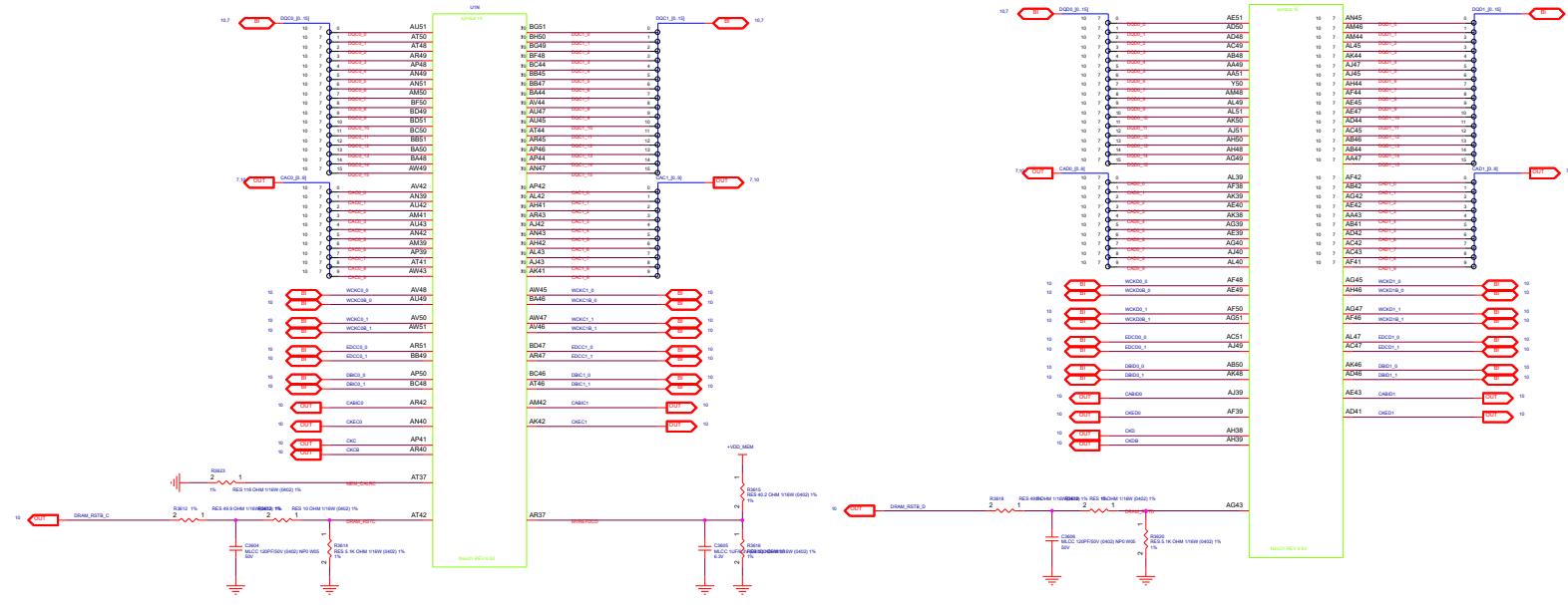


ASIC CH0 → MEM CHB
ASIC CH1 → MEM CHA









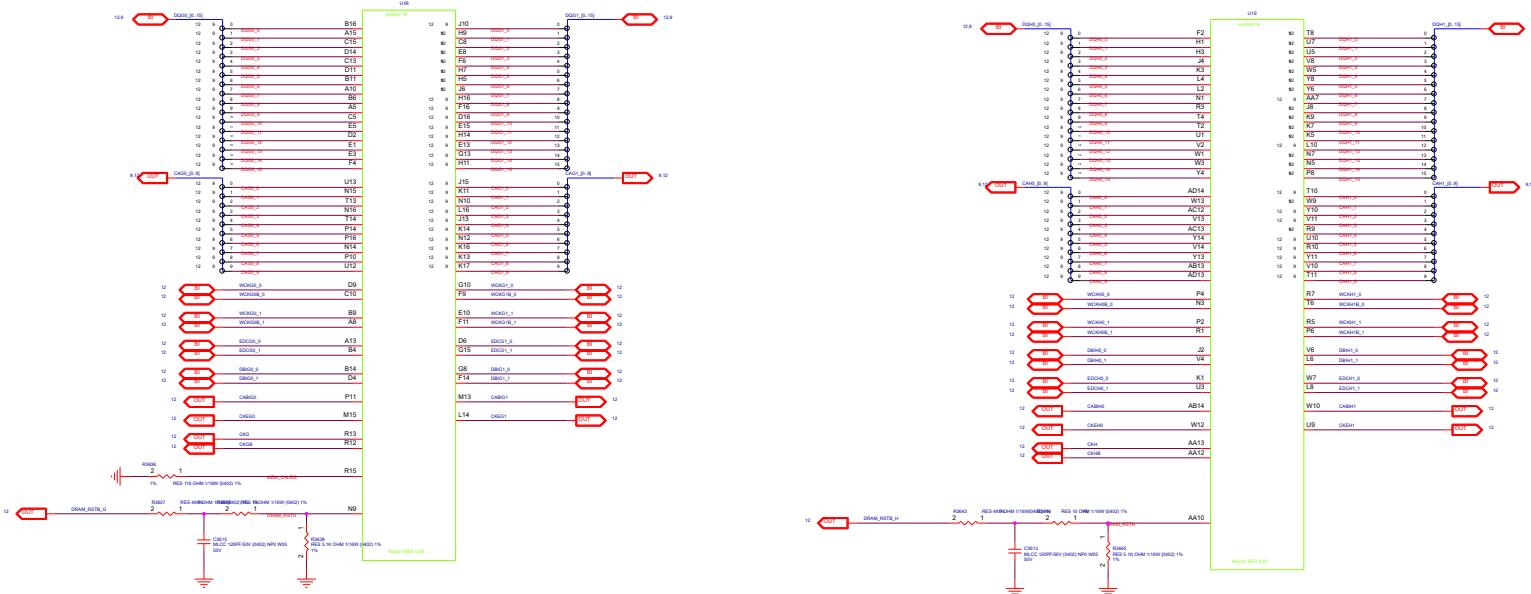
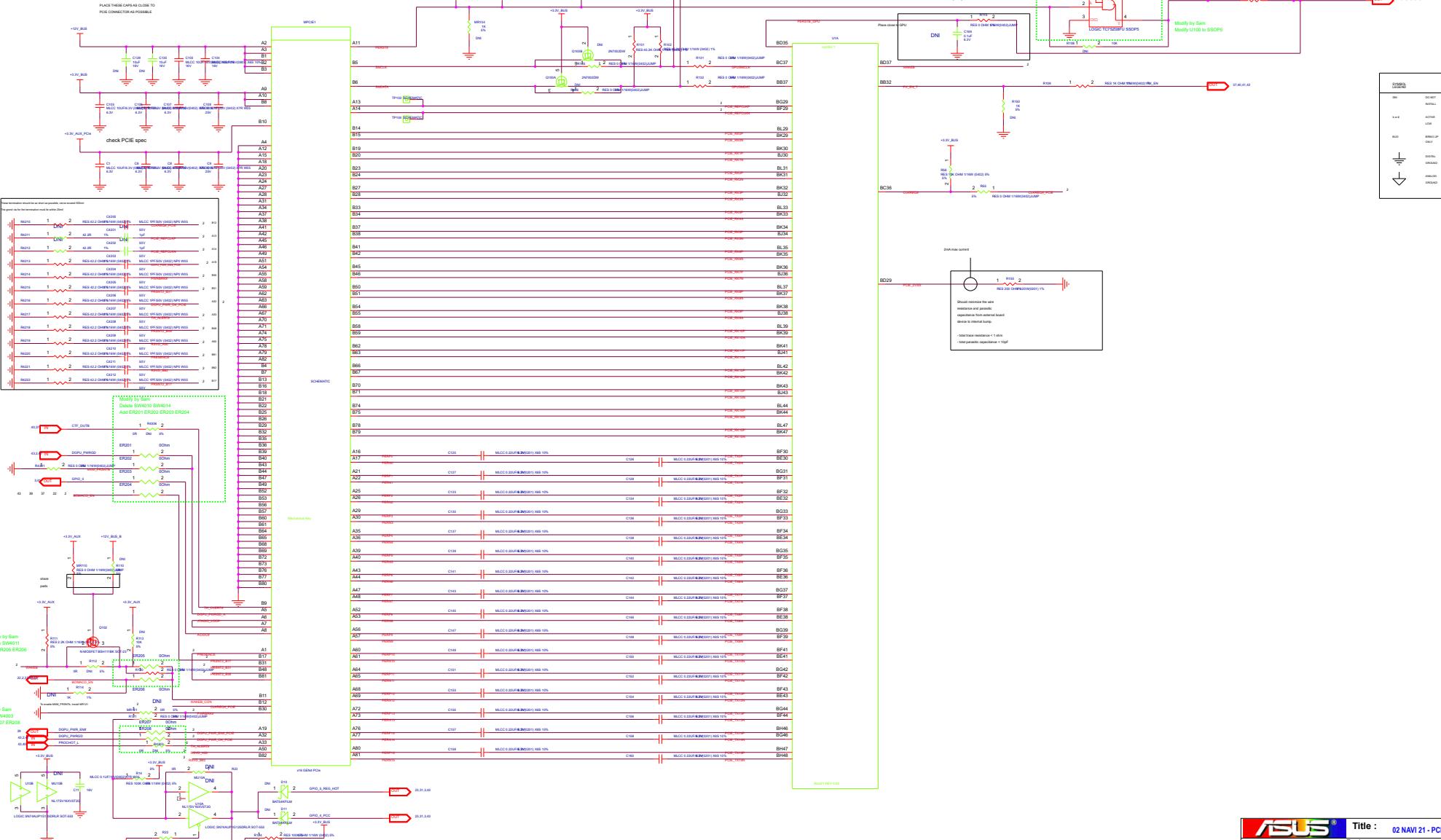
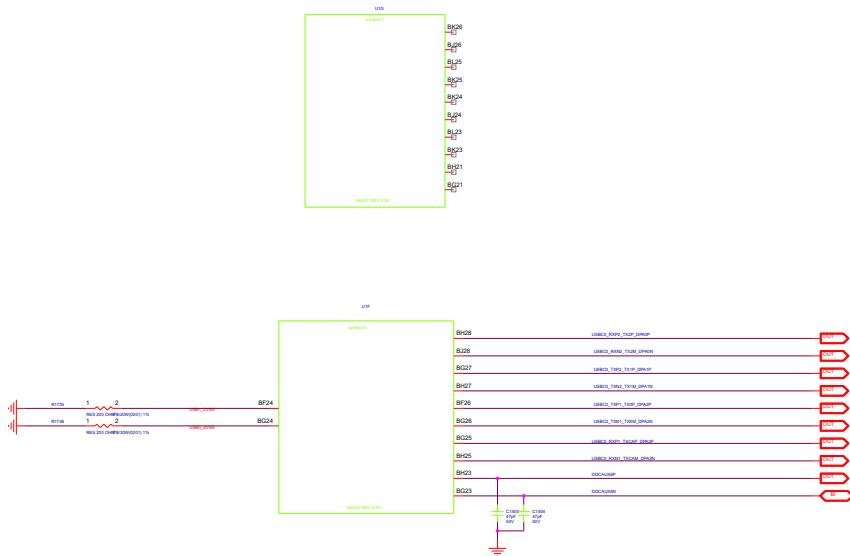
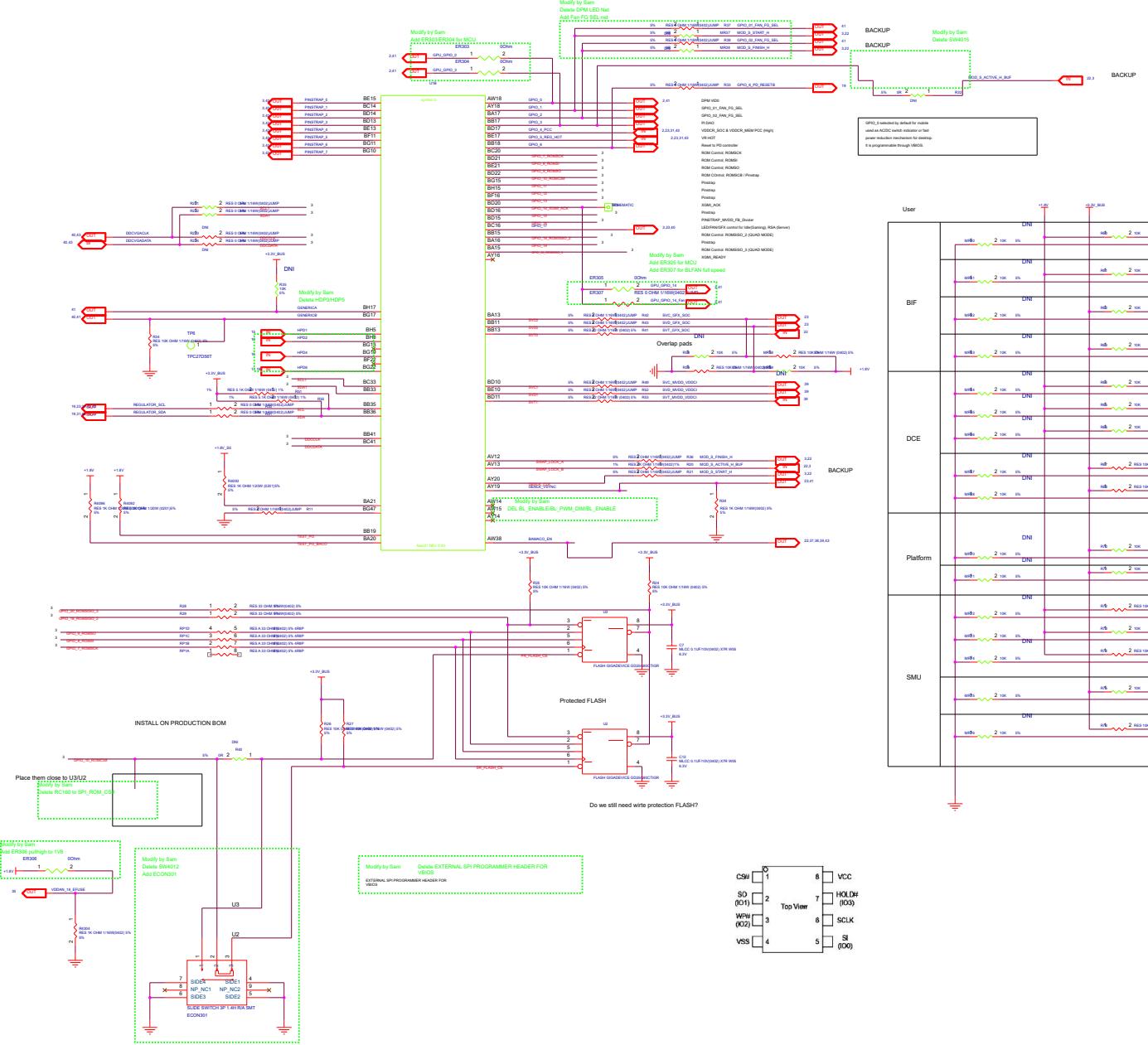


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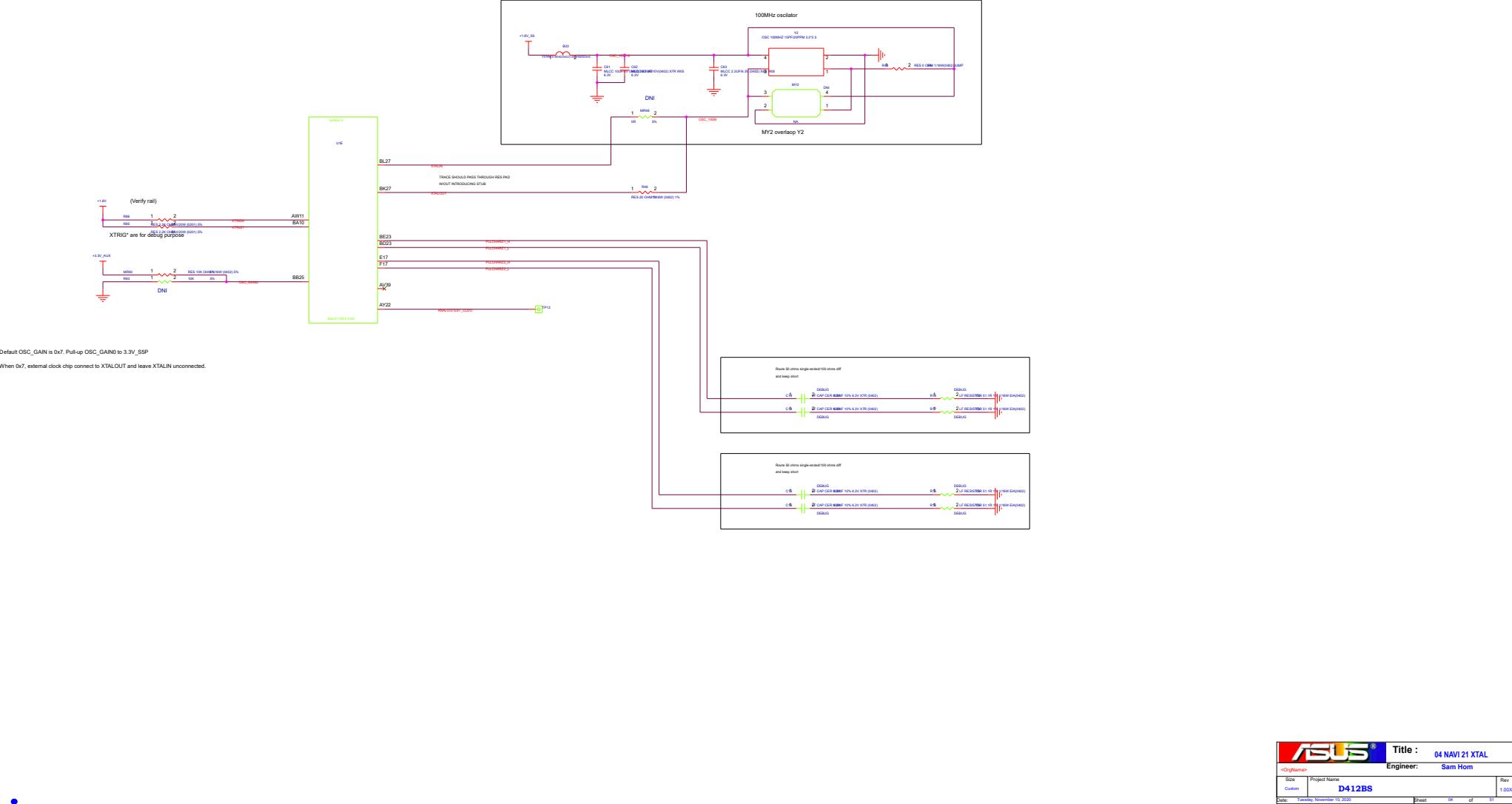
SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	GFX PHASES 8&9
2	NAVI 21 - PCIe Interface	27	GFX PHASES 11
3	NAVI 21 - GPIOs	28	GFX PHASES 5&7
4	NAVI 21 XTAL	29	GFX PHASES 3&10
5	XGMI	30	SOC PHASE 1&2
6	NAVI 21 MEM CH AB	31	VDD_MEM & VDDCI CONTROLLER
7	NAVI 21 MEM CH CD	32	VDD_MEM PHASES 1&2
8	NAVI 21 MEM CH EF	33	VDDCI_MEM PHASE 1
9	NAVI 21 MEM CH GH	34	NAVI 21 DECAPS
10	GDDR6 MEM CH CD	35	NAVI 21 POWER
11	GDDR6 MEM CH EF	36	NAVI 21_POWER and GND
12	GDDR6 MEM CH GH	37	POWER_MANAGEMENT
13	GDDR6 MEM CH AB	38	ClampWA
14	NAV121 TMDPA - USB-C	39	SVI2 & BxMACO
15	NAV121 TMDPF - HDMI	40	THERMAL
16	NAV121 TMDPC&E - DP	41	DPM_Status_LED & GDDR6_JTAG
17	NAV121 TMDPA	42	Pi Debug
18	NAV121 USB	43	DEBUG
19	PD Controller	44	History
20	USB-C PORT 1		
21	USB_5V_1.8V_0.75V		
22	MODS CONTROL & POWER		
23	GFX & SOC CONTROLLER		
24	GFX PHASES 1&2		
25	GFX PHASES 4&6		

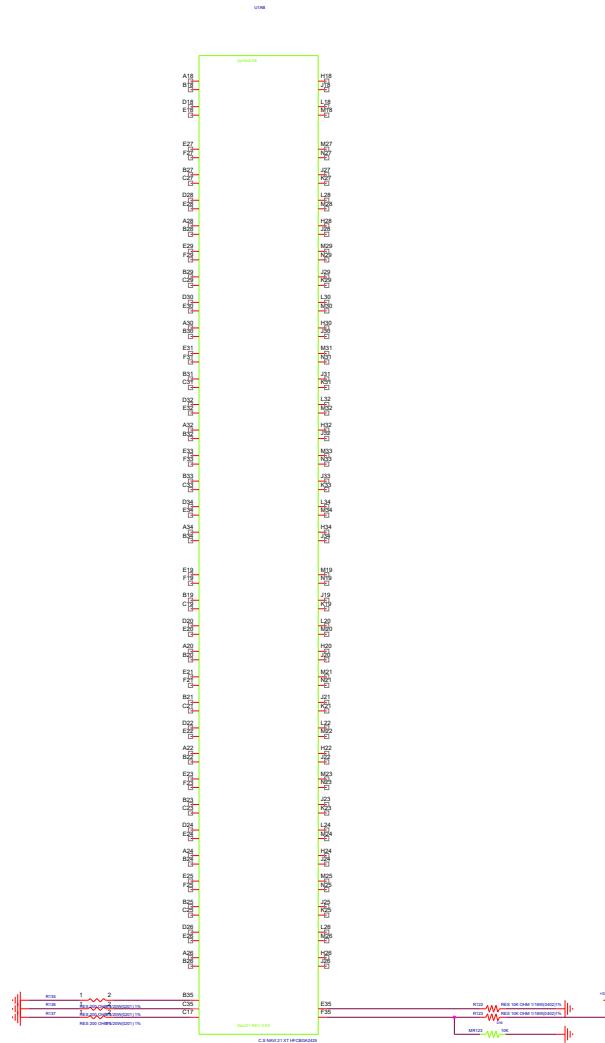


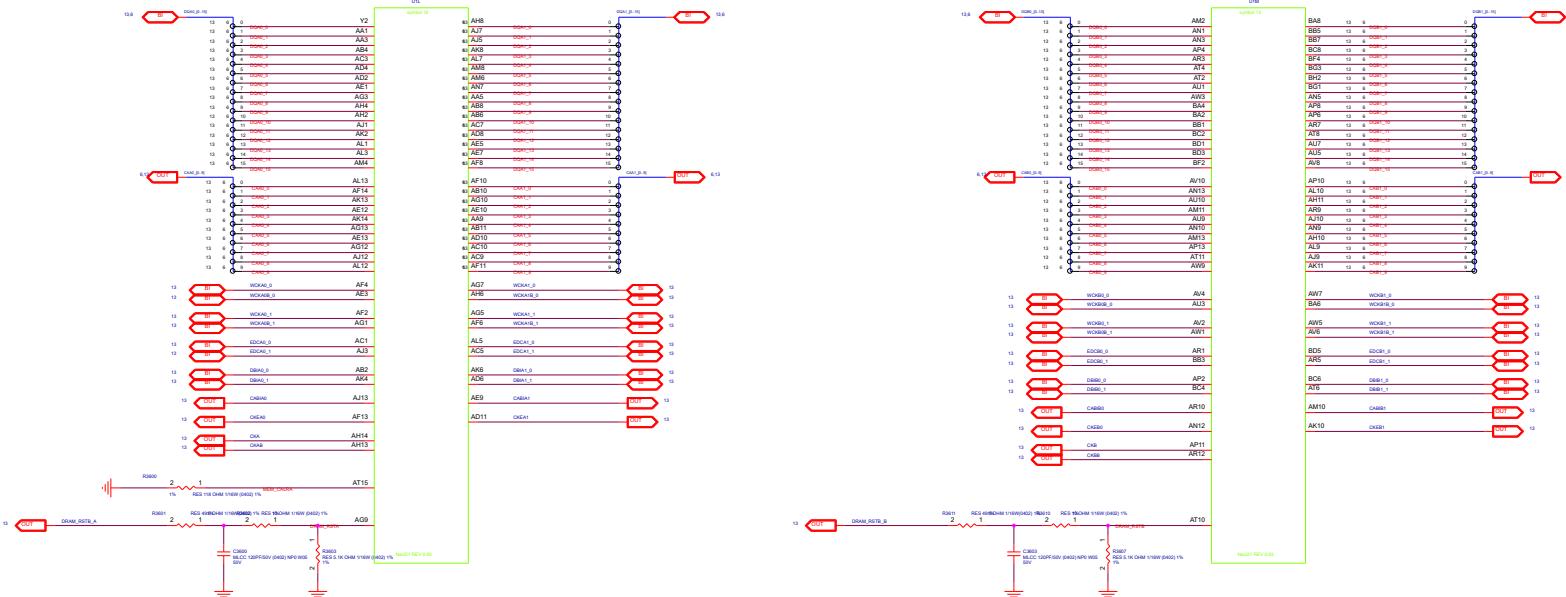


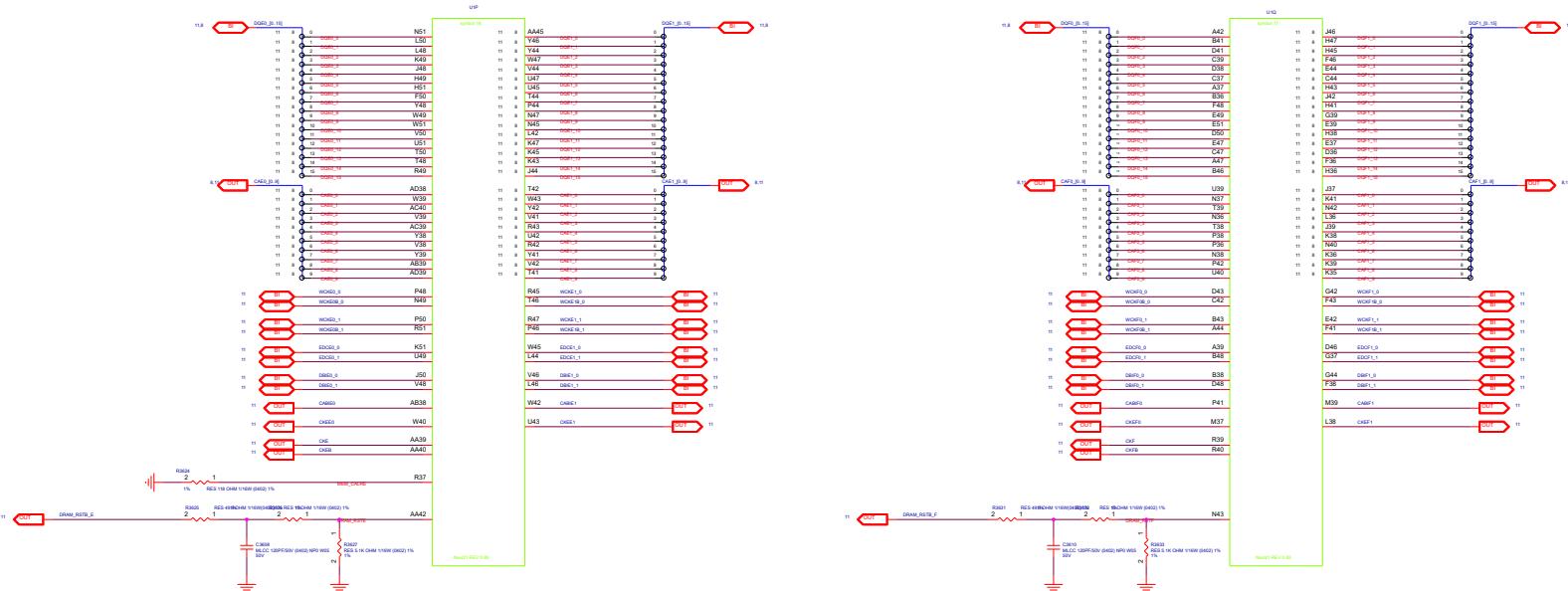


User		Internal Default Value		Definition
BIF	DNI	0	PINSTRAP_BIF_GEN4_DIS_A 0 PCIe GbE is supported 1 PCIe GbE is not supported	
	DNI	0	PINSTRAP_BIF_CLK_PM_EN 0 CLK/GP power management is disabled 1 CLK/GP power management capability is enabled	
	DNI	0	PINSTRAP_BIF_LC_TX_SWING	
	DNI	0	PINSTRAP_BIF_VGA_DIS 0 VGA controller capacity needed 1 The device must be recognized as the system's VGA controller	
	DNI	0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display connectors	
	DNI	0	0 All displays connected 1 1 displays connected 2 2 displays connected 3 3 displays connected 4 4 displays connected	
	DNI	0	PINSTRAP_AUD[1:0] 1 Audio via DisplayPort only 2 Audio via DisplayPort and HDMI or analog 3 Audio via DisplayPort and native HDMI	
	DNI	0	PINSTRAP_BOARD_CONFIG[2:0] TBD	
	DNI	0	PINSTRAP_MVND_BOOT_VID_CONFIG 0 Both with feedback device 1 Both w/o with feedback device	
	DNI	1	PINSTRAP_ROM_CONFIG[2:0] 101	
Platform	DNI	0	PINSTRAP_SMBUS_ADDR 0 0x000 1 0x001	
	DNI	0	PINSTRAP_BIOS_ROM_EN 0 Disable the external BIOS ROM device 1 Enable the external BIOS ROM device	
	DNI	1		
	DNI	1		
	DNI	1		
SMU	DNI	0		
	DNI	1		



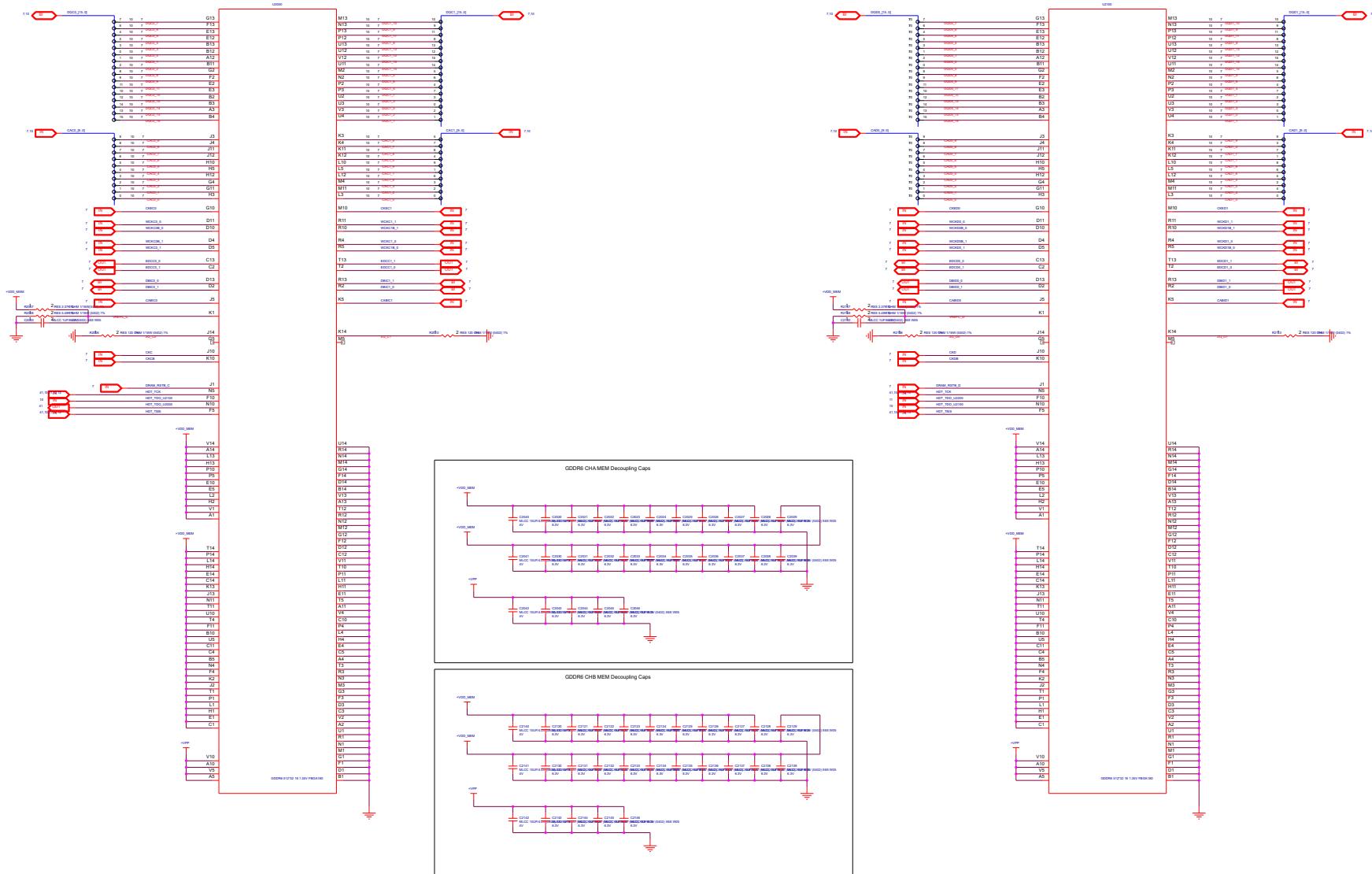




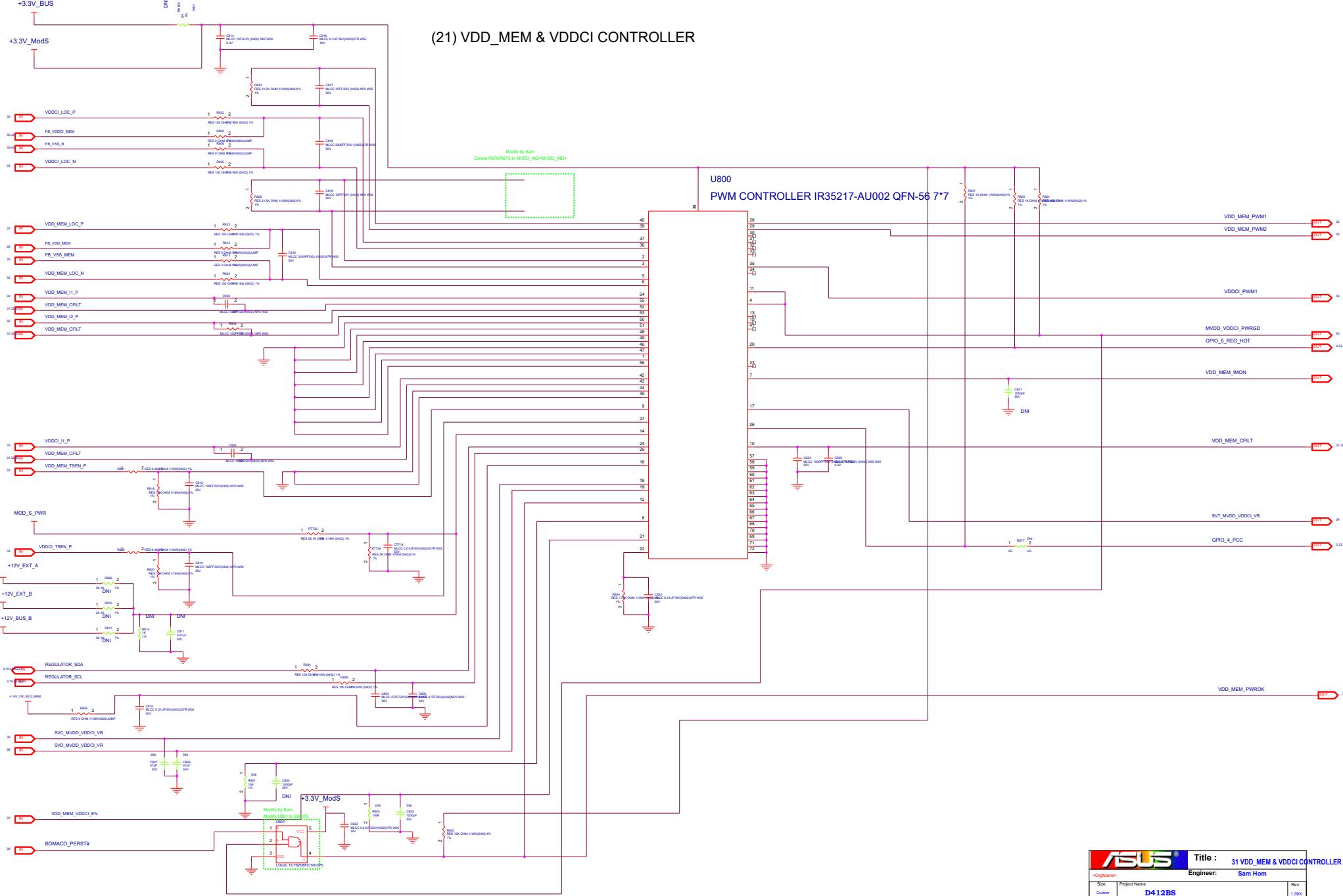


ASIC CH0 → MEM CHA
ASIC CH1 → MEM CHB

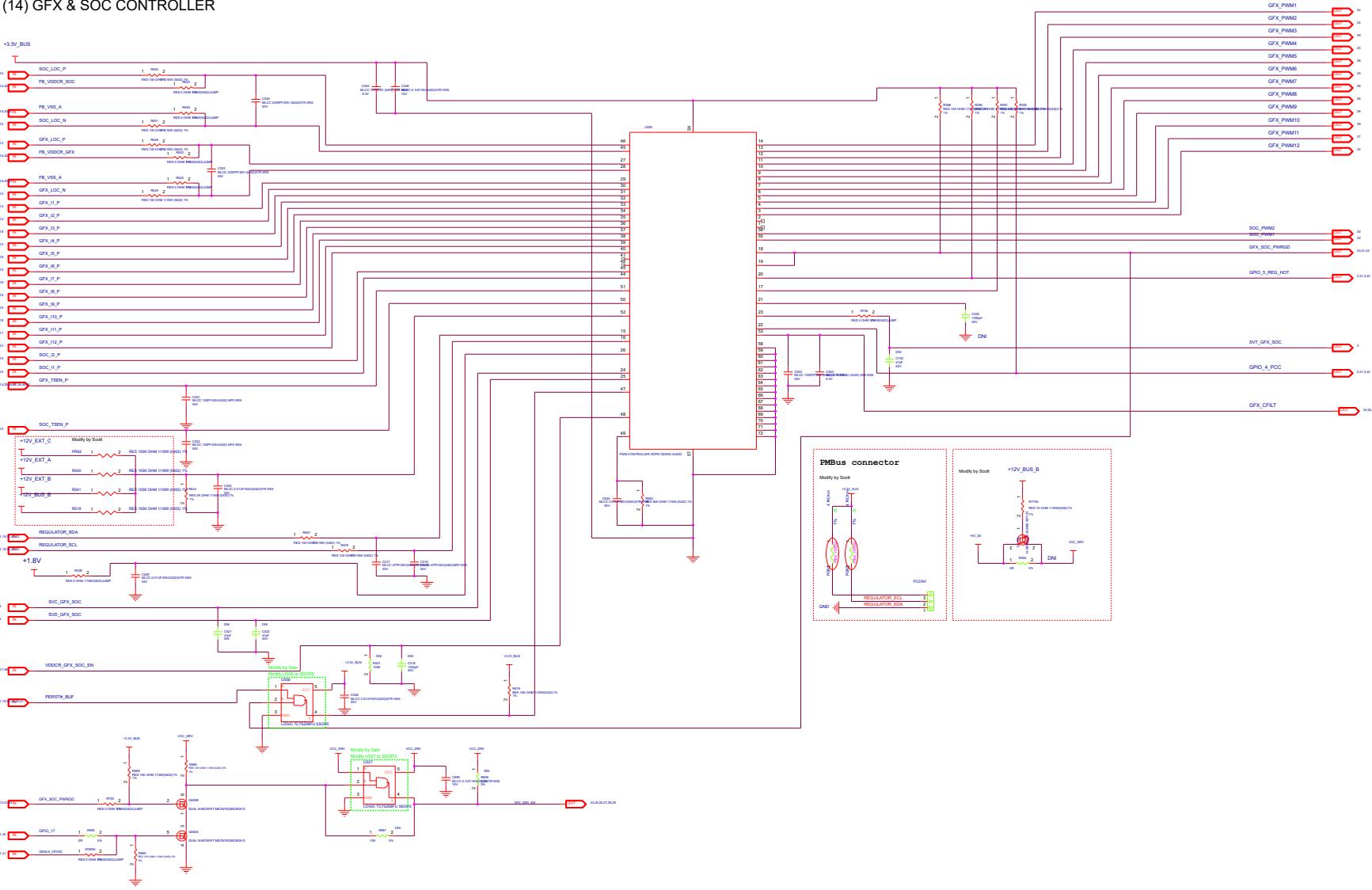
ASIC CH0 → MEM CHA
ASIC CH1 → MEM CHB



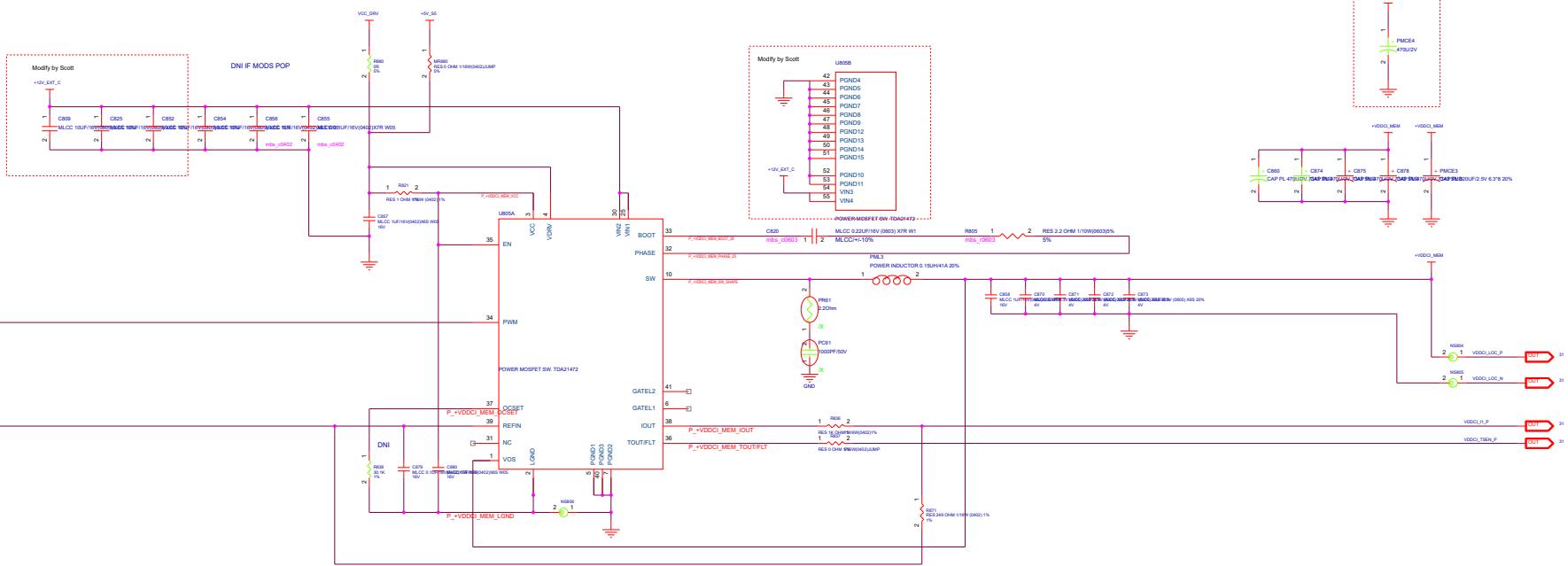
(21) VDD_MEM & VDDCI CONTROLLER

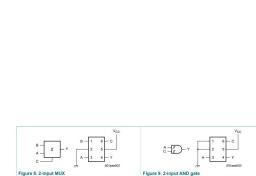
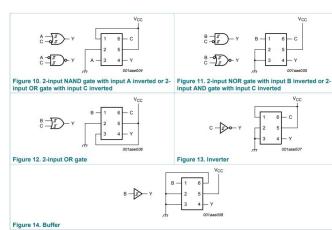


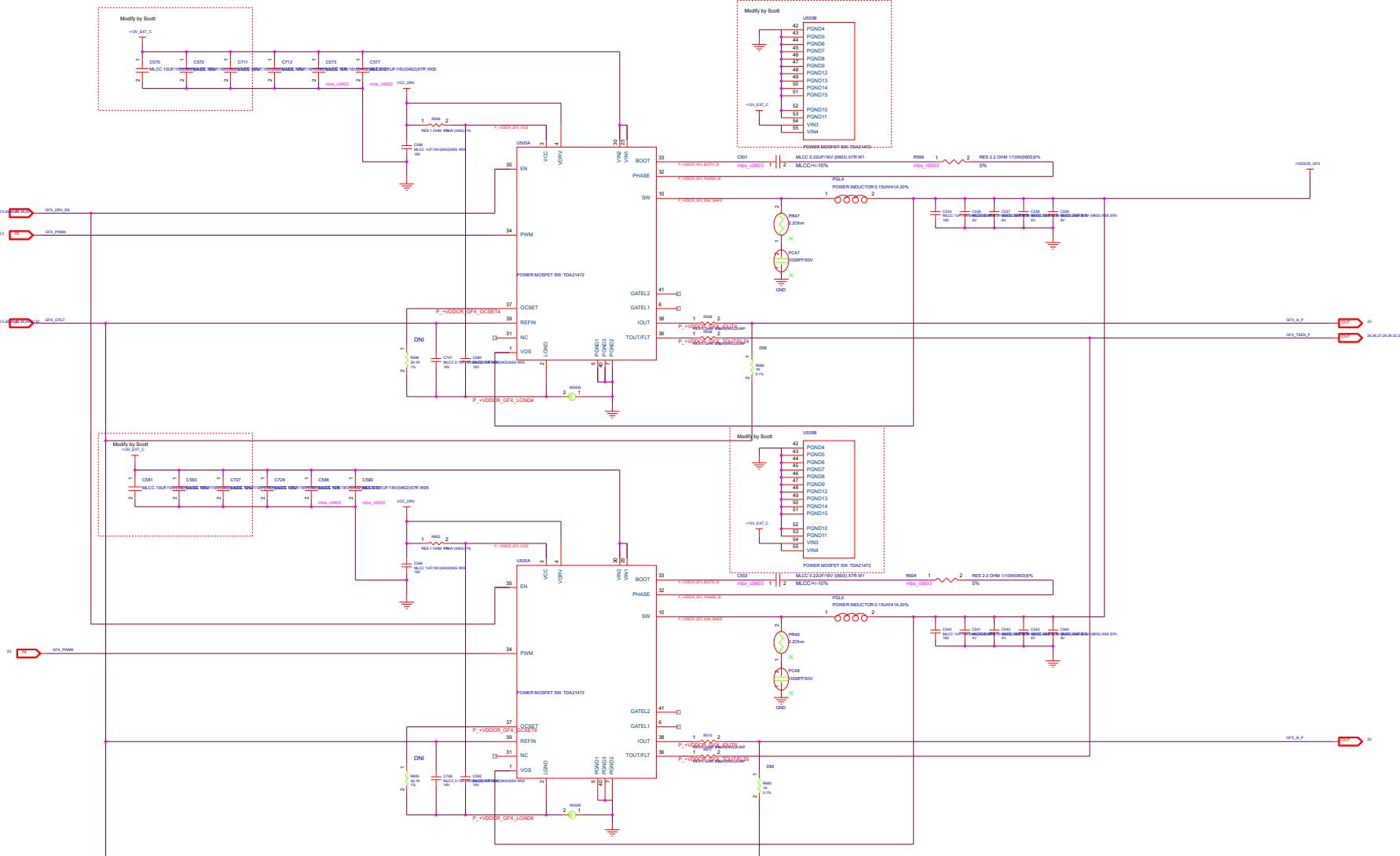
(14) GFX & SOC CONTROLLER

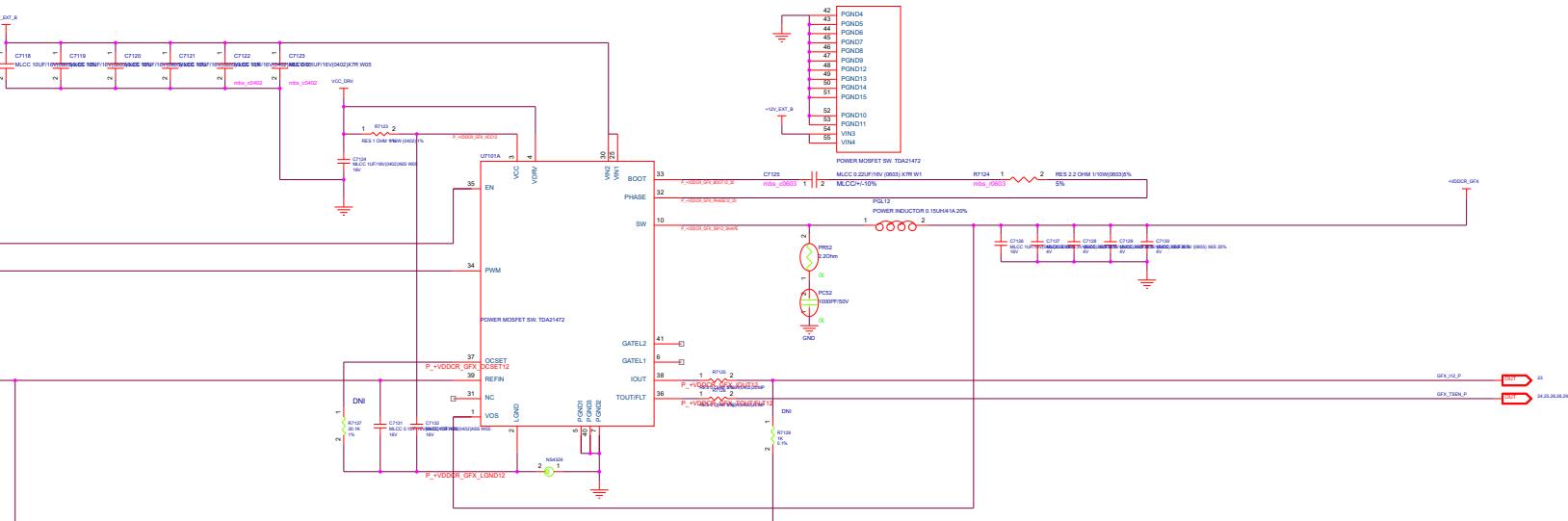
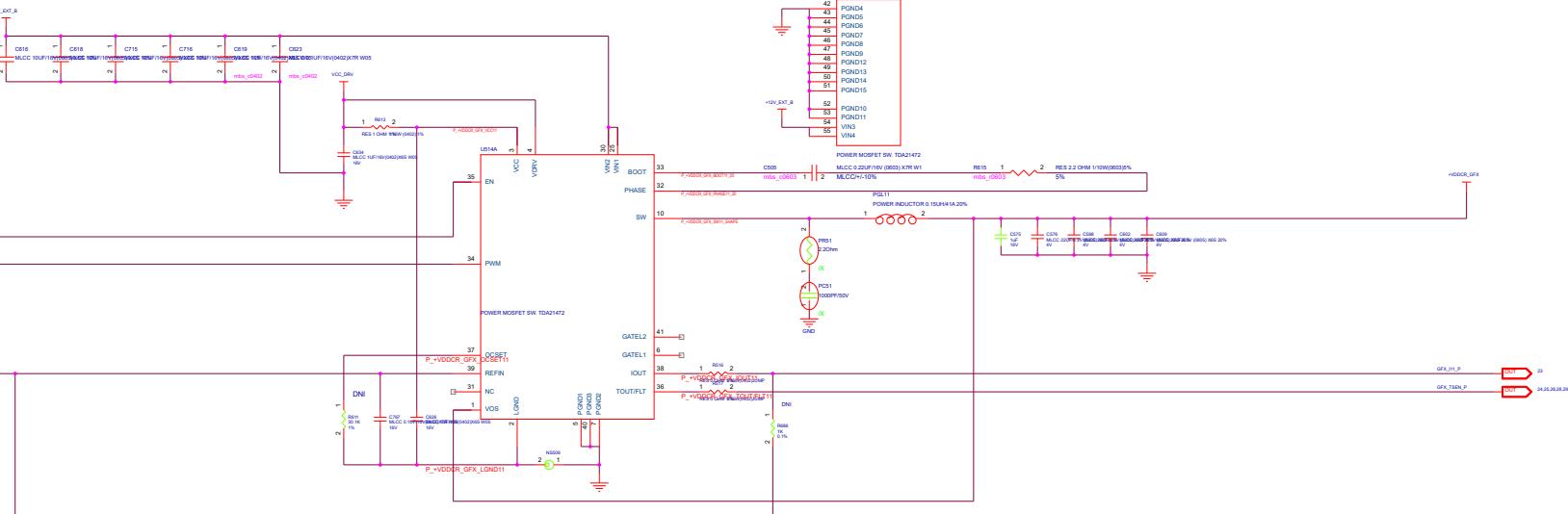


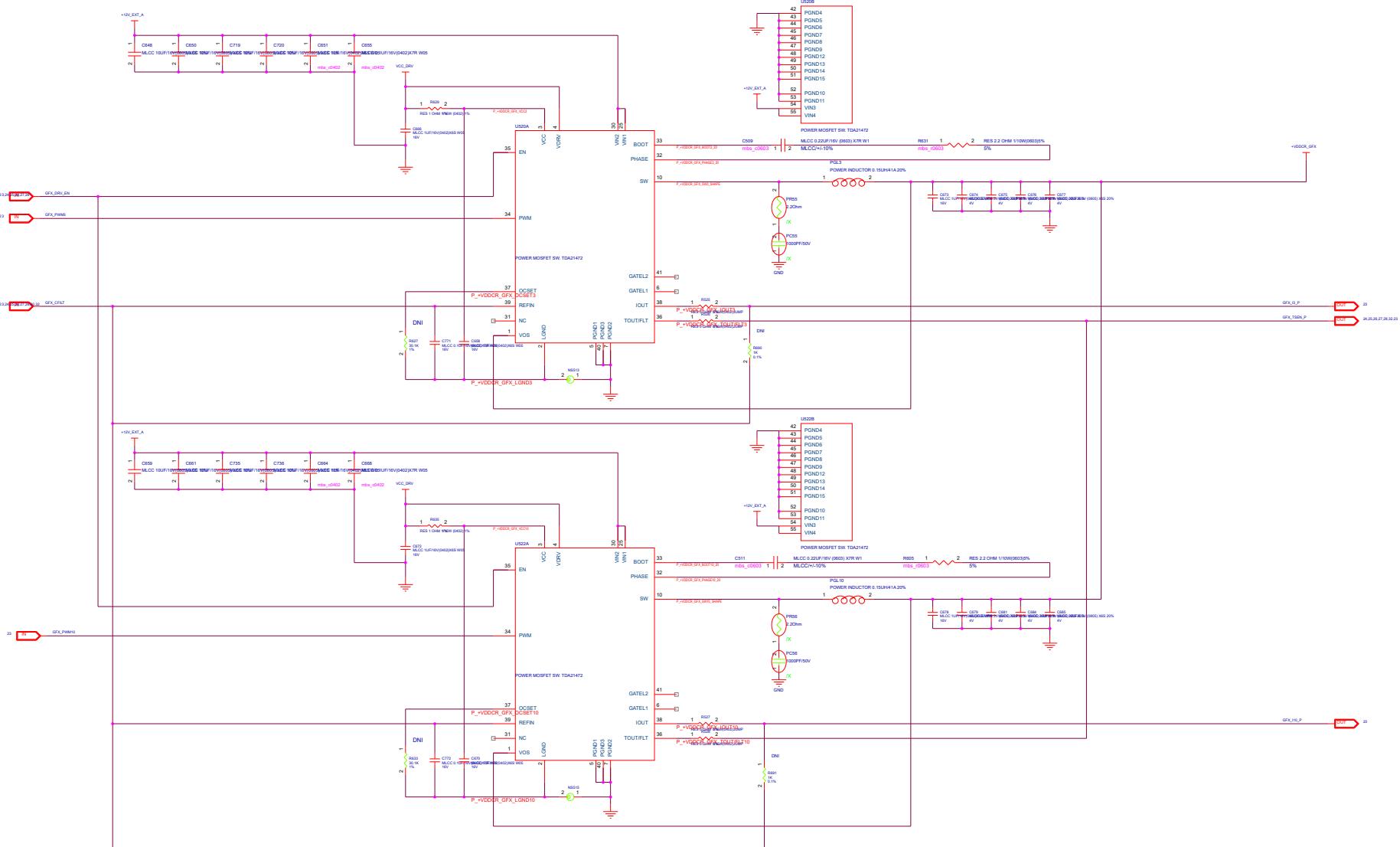
	Title :	23 GFX & SOC CONTROLLER
<OrgName>	Engineer:	Sam Hom
Size Custom	Project Name D412BS	Rev 1.00X
Date Tuesday, November 15, 2005	Check	35
	rd	50

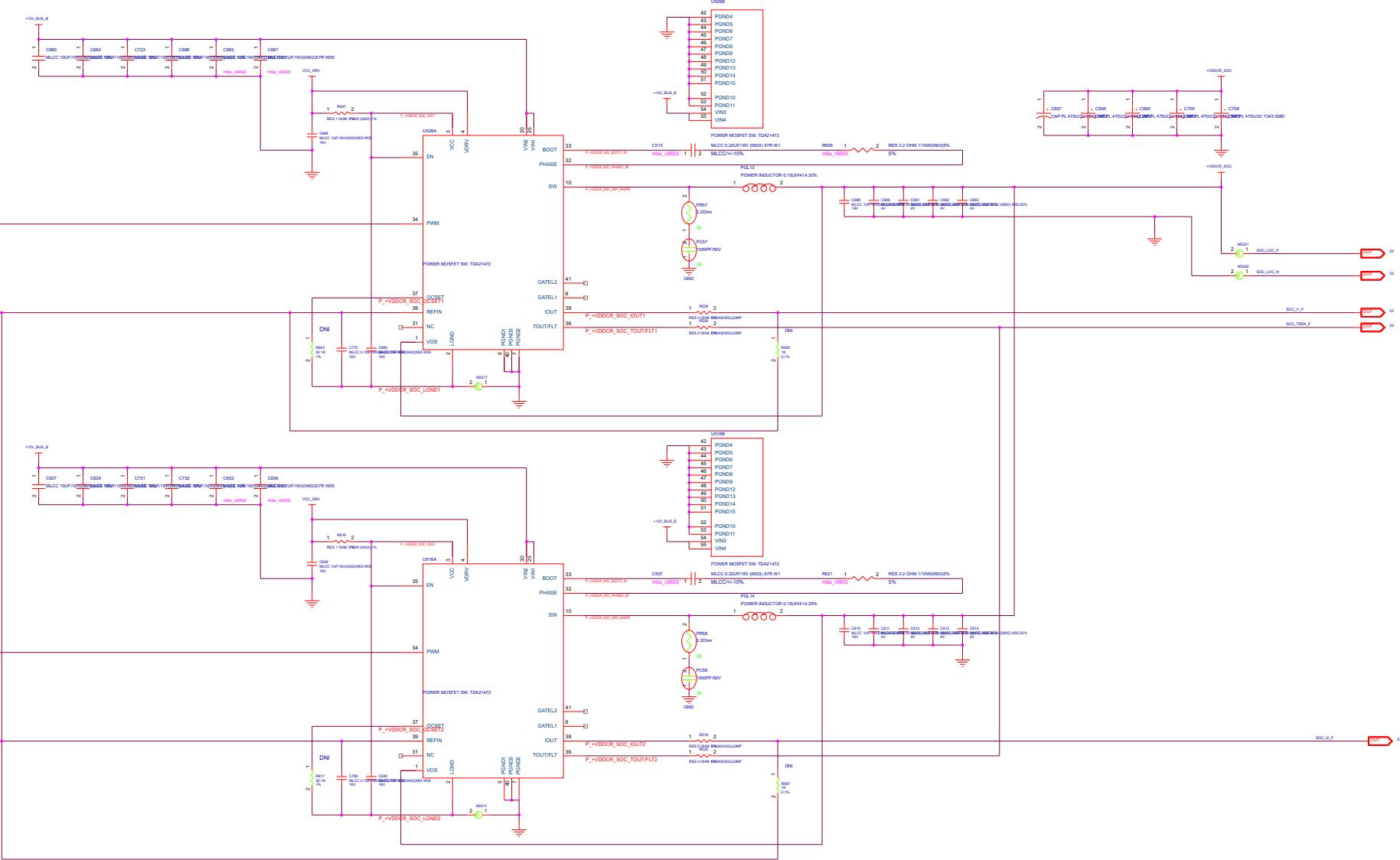


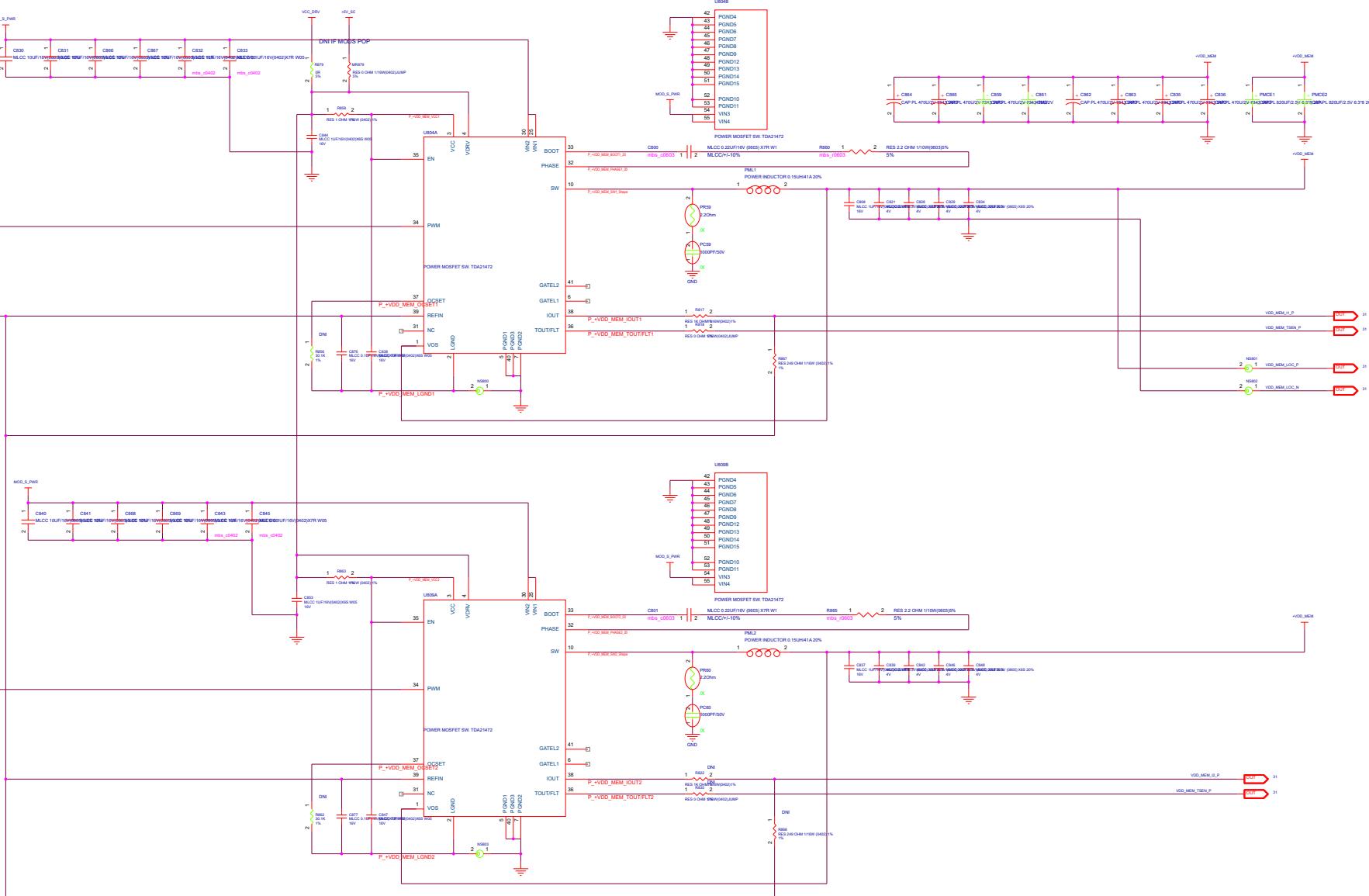












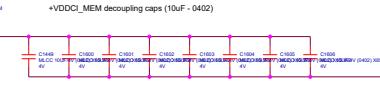
+VDDCR_GFX



+VDDCR_GFX



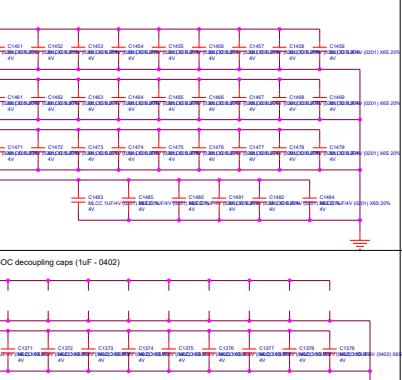
+VDDCI_MEM



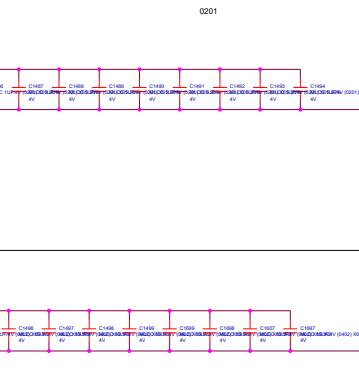
DNI these six caps to match SLT board and keep the design consistent across SKUs

C1218
C1208
C1200
C1438
C1413
C1384

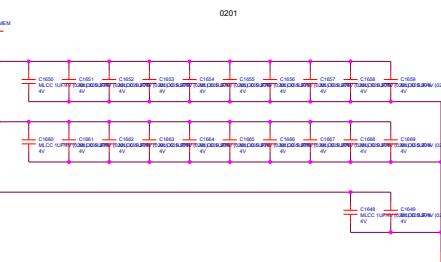
+VDDIO_MEM decoupling caps (1uF - 0201)



VDDCR_SOC decoupling caps (1uF)



+VDDIO_MEM decoupling caps (1uF)



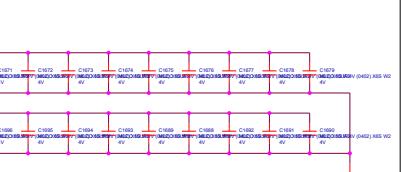
+VDDCR_SOC decoupling caps (1uF - 0402)



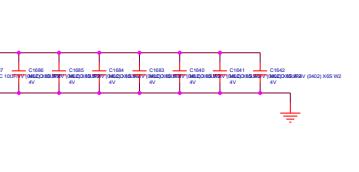
+VDDCR_SOC decoupling caps (1uF)

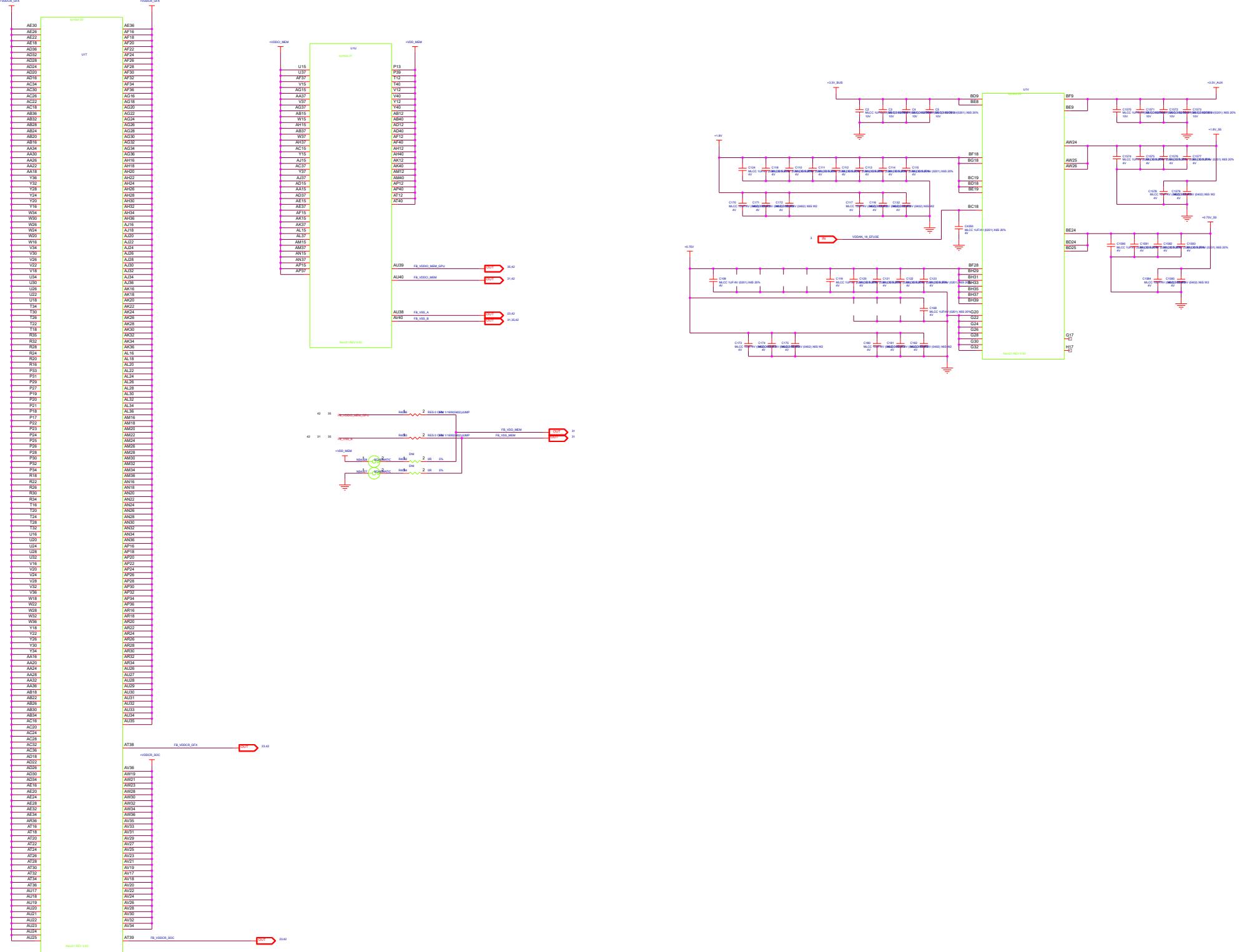


+VDDCI_MEM decoupling caps (10uF - 0402)



+VDDCI_MEM decoupling caps (10uF - 0402)





FOR PI DAUGHTER CARD
Modify by Sam
Date 12/05/14 08:03 AM 2012

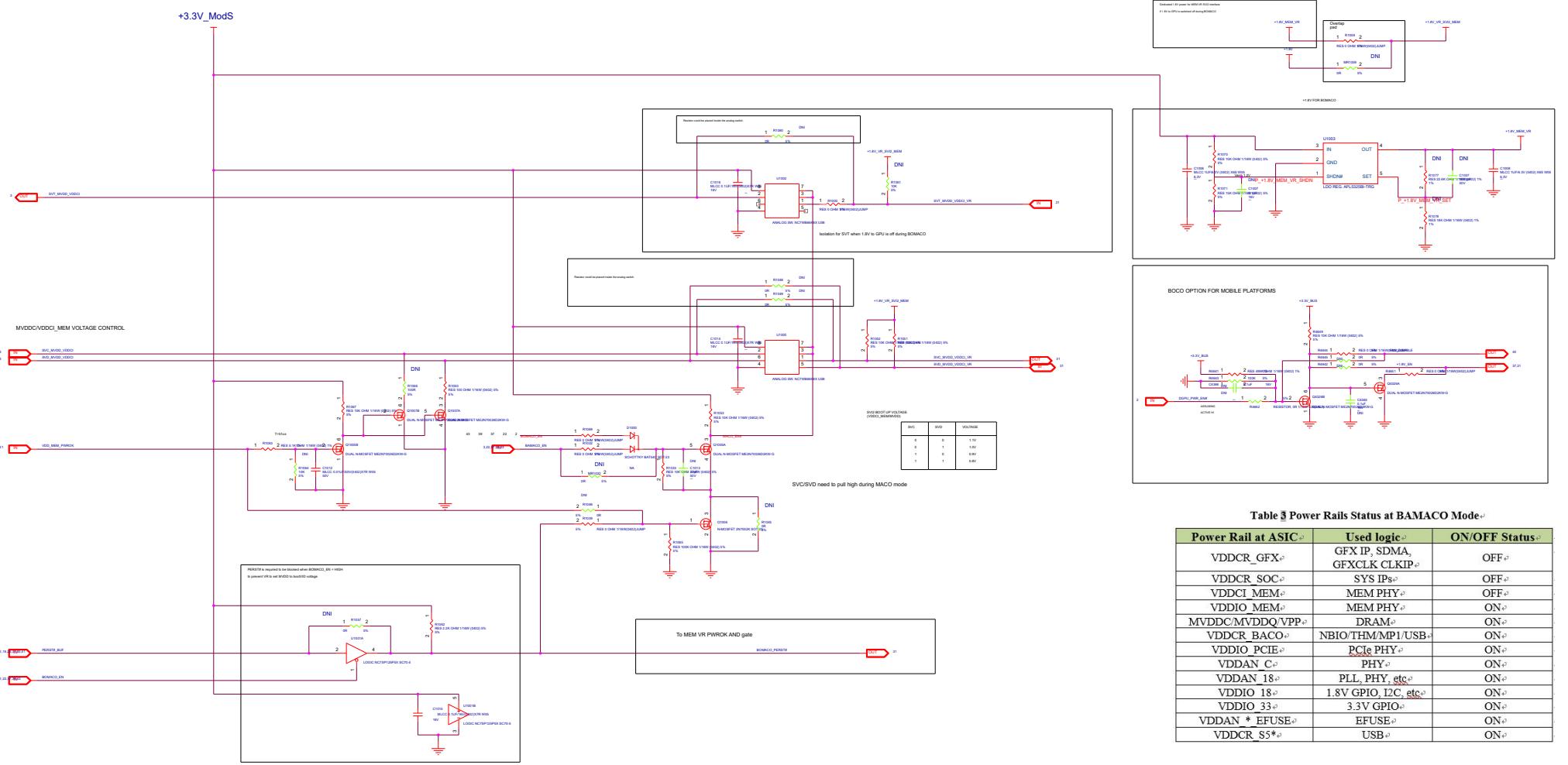


Table 3 Power Rails Status at BAMACO Mode^v

Power Rail at ASIC ^v	Used logic ^v	ON/OFF Status ^v
VDDCR_GFX ^v	GFX IP, SDMA, GFXCLK CLKIP ^v	OFF ^v
VDDCR_SOC ^v	SYS IP ^v	OFF ^v
VDDCI_MEM ^v	MEM PHY ^v	OFF ^v
VDDIO_MEM ^v	MEM PHY ^v	ON ^v
MVDDC/MVDDQ/VPP ^v	DRAM ^v	ON ^v
VDDCR_BACO ^v	NBIO/THM/MP1/USB ^v	ON ^v
VDDIO_PCIE ^v	PCIe PHY ^v	ON ^v
VDDAN_C ^v	PHY ^v	ON ^v
VDDAN_18 ^v	PLL, PHY, etc ^v	ON ^v
VDDIO_18 ^v	1.8V GPIO, I2C, etc ^v	ON ^v
VDDAN_33 ^v	3.3V GPIO ^v	ON ^v
VDDAN * EFUSE ^v	EFUSE ^v	ON ^v
VDDCR_S5 ^v	USB ^v	ON ^v

Table 3 Power Rails Status at BOMACO Mode^v

Power Rail at ASIC ^v	Used logic ^v	ON/OFF Status for BOMACO-A ^v
VDDCR_GFX ^v	GFX IP, SDMA, GFXCLK CLKIP ^v	OFF ^v
VDDCR_SOC ^v	SYS IP ^v	OFF ^v
VDDCI_MEM ^v	MEM PHY ^v	OFF ^v
VDDIO_MEM ^v	MEM PHY ^v	ON ^v
MVDDC/MVDDQ/VPP ^v	DRAM ^v	ON ^v
VDDCR_BACO ^v	NBIO/THM/MP1/USB ^v	OFF ^v
VDDIO_PCIE ^v	PCIe PHY ^v	OFF ^v
VDDAN_C ^v	PHY ^v	OFF ^v
VDDAN_18 ^v	PLL, PHY, etc ^v	OFF ^v
VDDIO_18 ^v	1.8V GPIO, I2C, etc ^v	OFF ^v
VDDAN_33 ^v	3.3V GPIO ^v	OFF ^v
VDDCR_S5 ^v	USB ^v	ON ^v

Table 4 Key Signals at Different PM Modes^v

Signals ^v	Default ^v	BOCO ^v	BOMACO ^v
PX_EN ^v	LOW ^v	N/A ^v	N/A ^v
MACO_EN ^v	N/A ^v	N/A ^v	N/A ^v
PERSTb ^v	HIGH ^v	1>0->1 ^v	1>0->1 ^v
PWR_EN ^v	HIGH ^v	LOW ^v	LOW ^v
BOMACO_EN ^v	LOW ^v	LOW ^v	HIGH ^v

Table 5 Platform to Support BOMACO^v

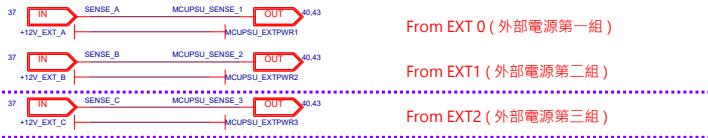
BOMACO_EN	SVC PU/PD	SVD PU/PD
HIGH ^v	PU ^v	PU ^v
LOW ^v	bootVID ^v	bootVID ^v

Power



From 12V (for 外接式風扇使用, 任一組12V皆可)
 From PCIE 3V3_AUX (for ITE)
 From BUS 3V3 (for ITE logic判斷)
 For 12V to 5V RGB PWR

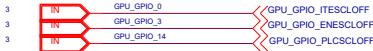
PSU DETECT INPUT



I2C



GPU_GPIO



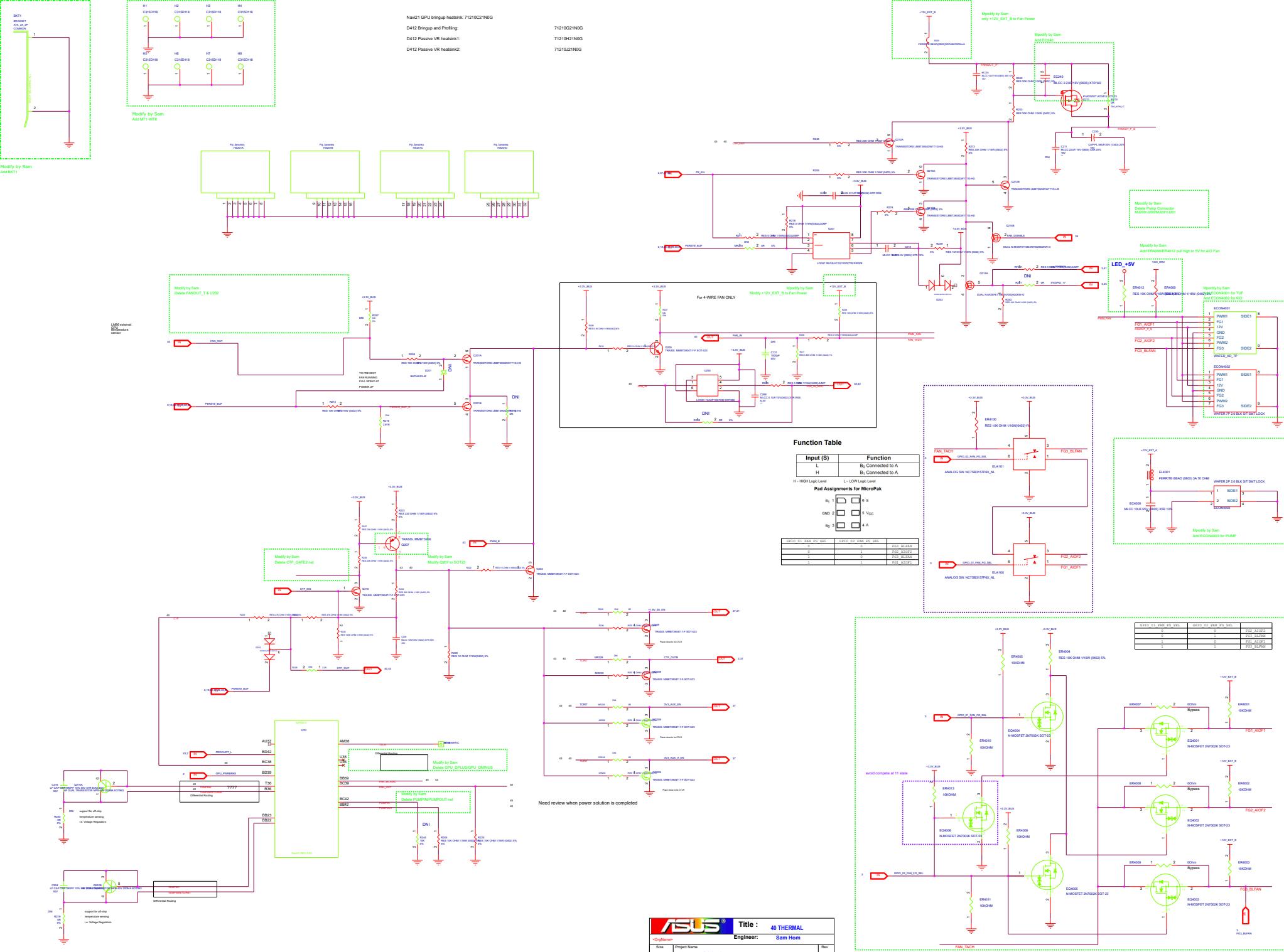
Title : STRIX000_POWER & OFF-PAGE

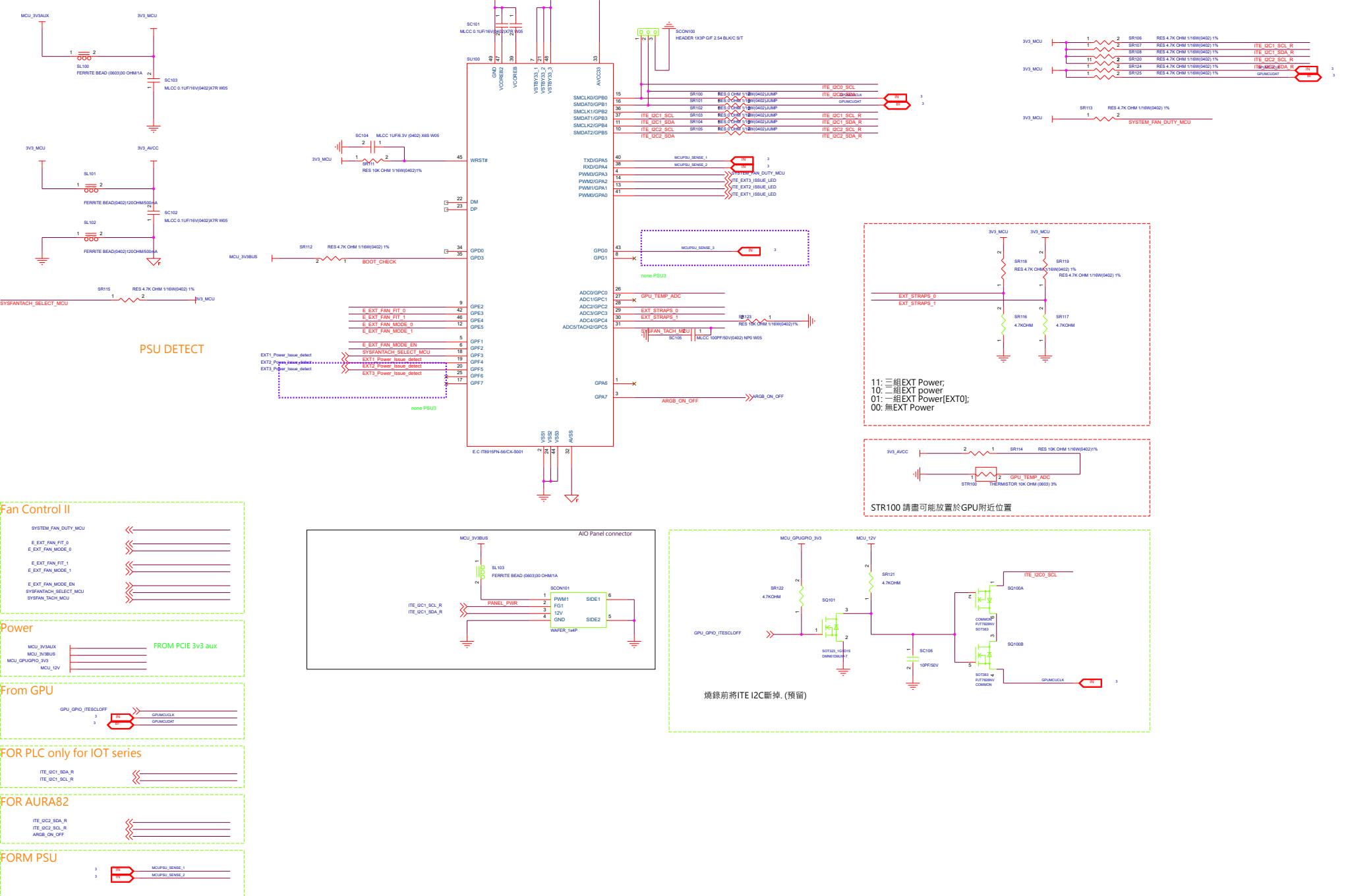
Engineer: Sam Horn

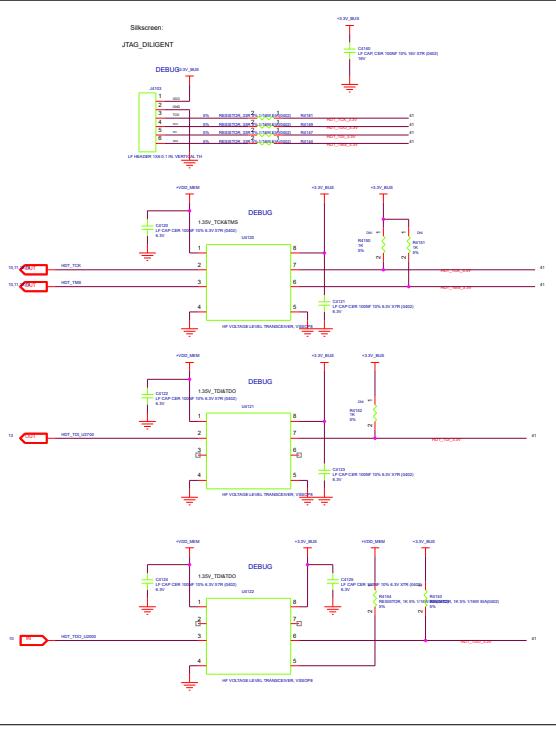
Size	Project Name	Rev
B	D412BS	1.00X

Date: Tuesday, November 10, 2020

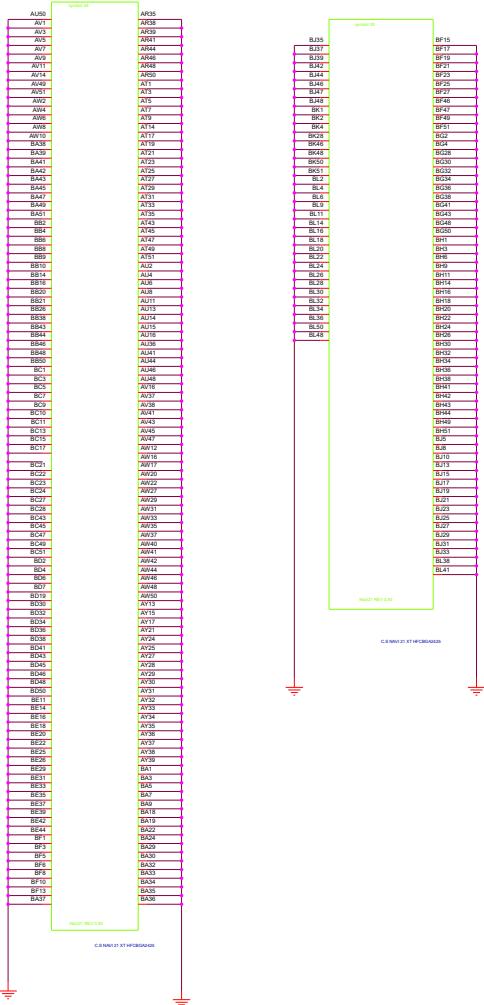
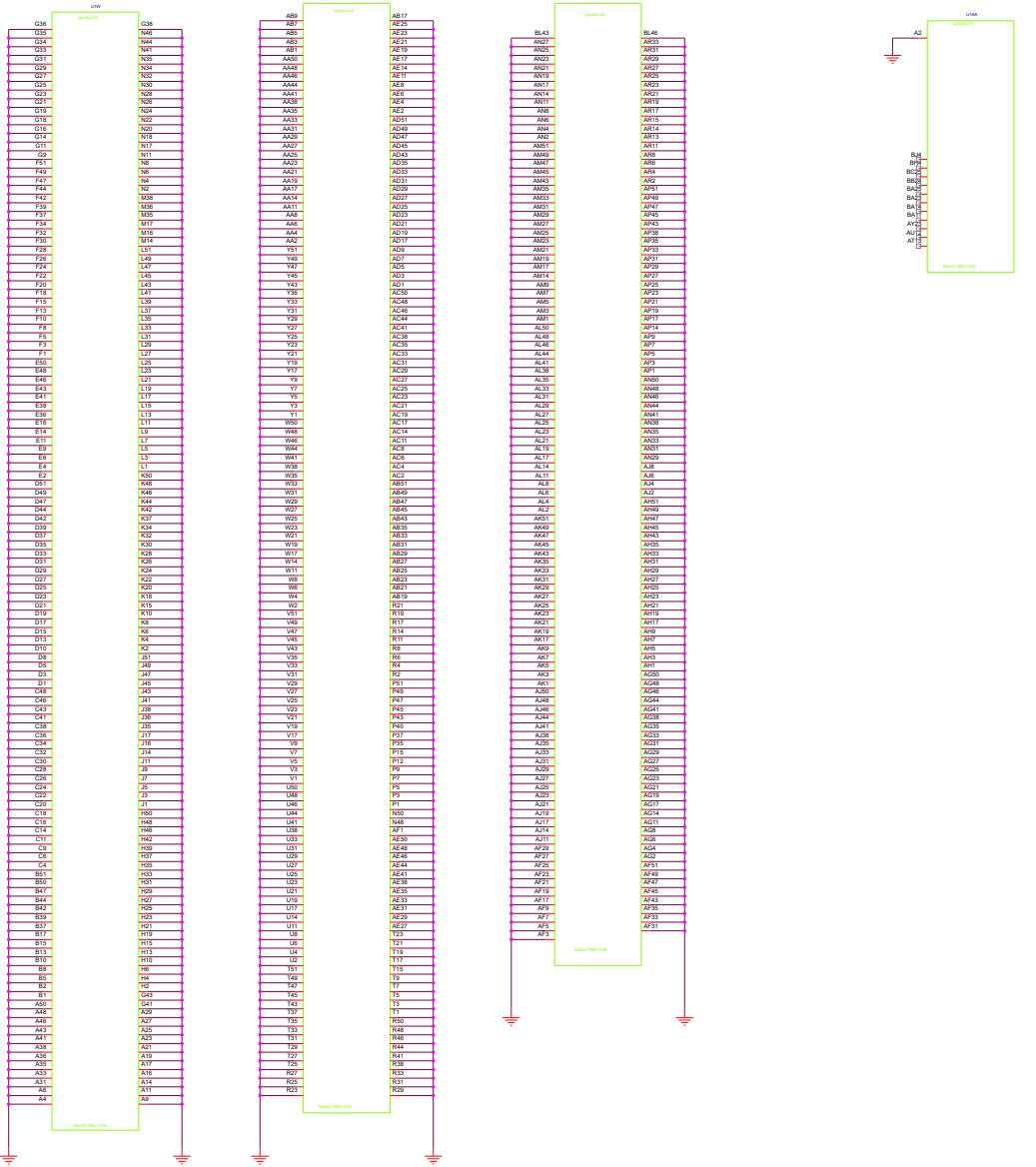
Sheet 46 of 51

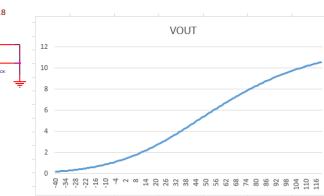
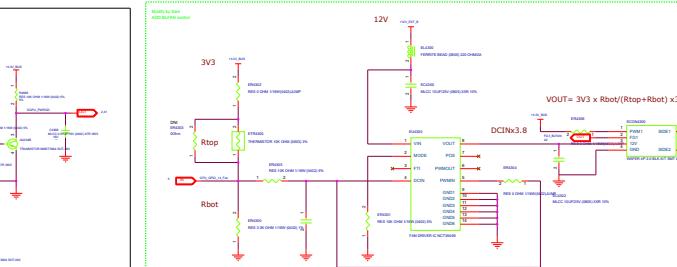
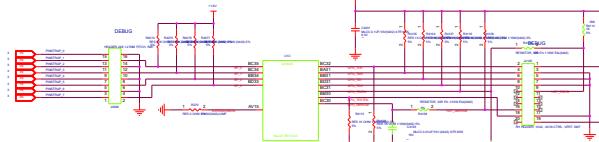
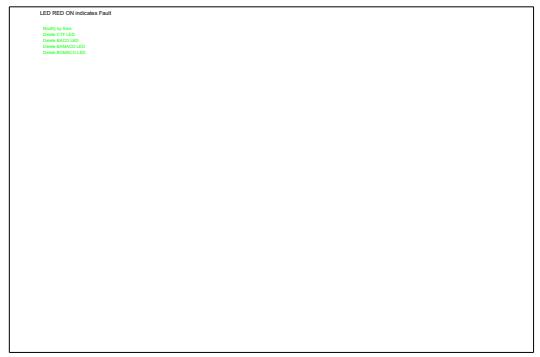
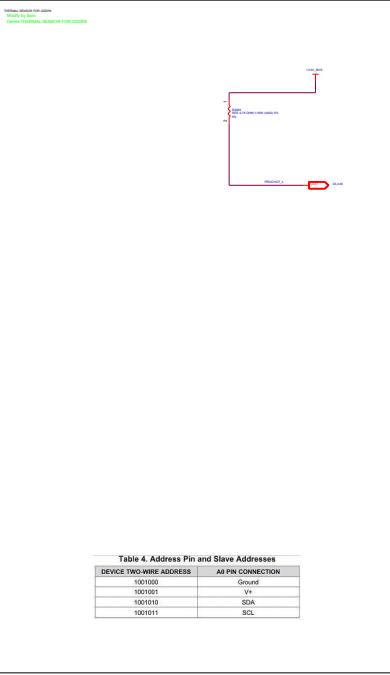


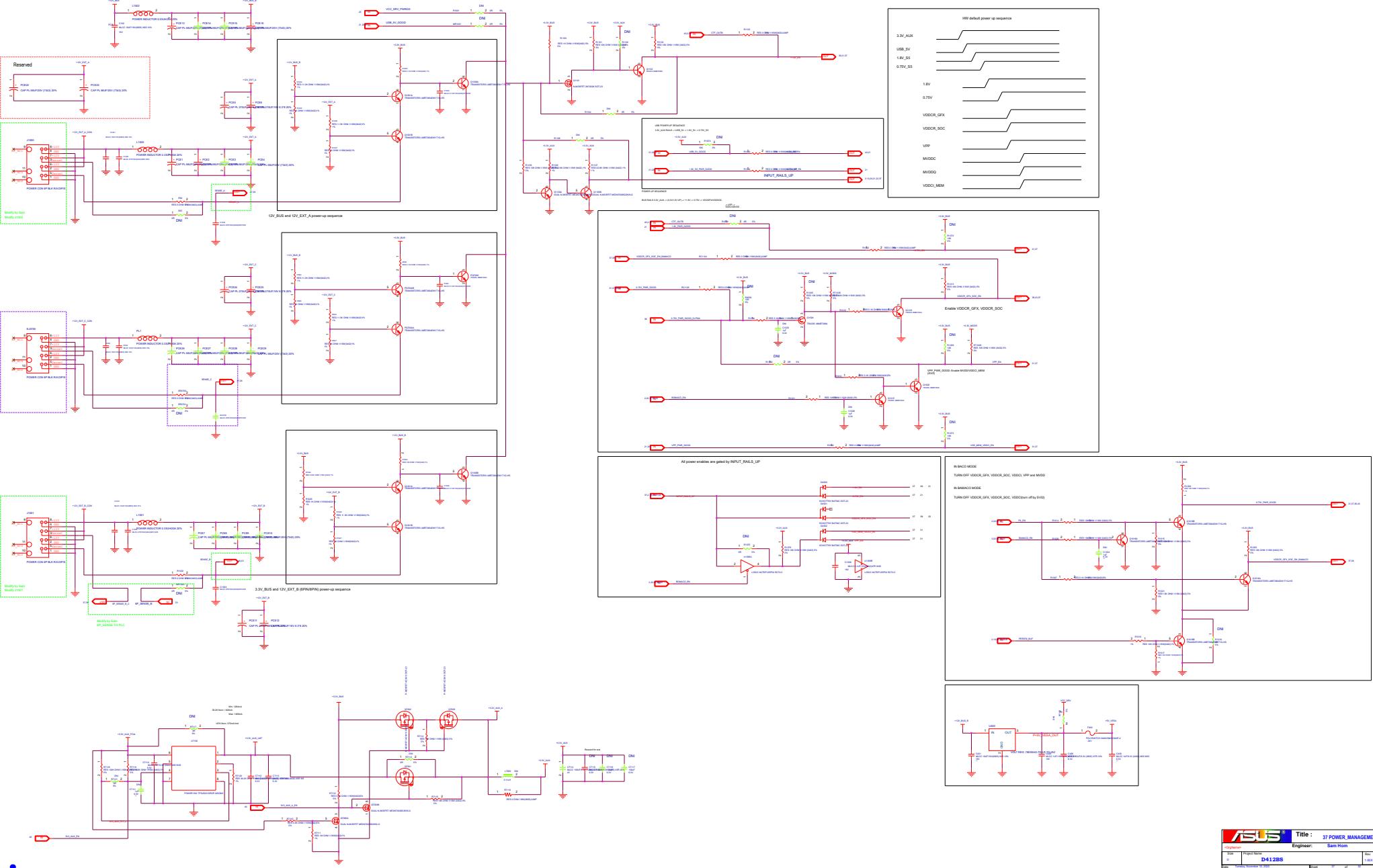




Modify by Sam
Delete RGB LED header
Delete RADEON Lightbar header



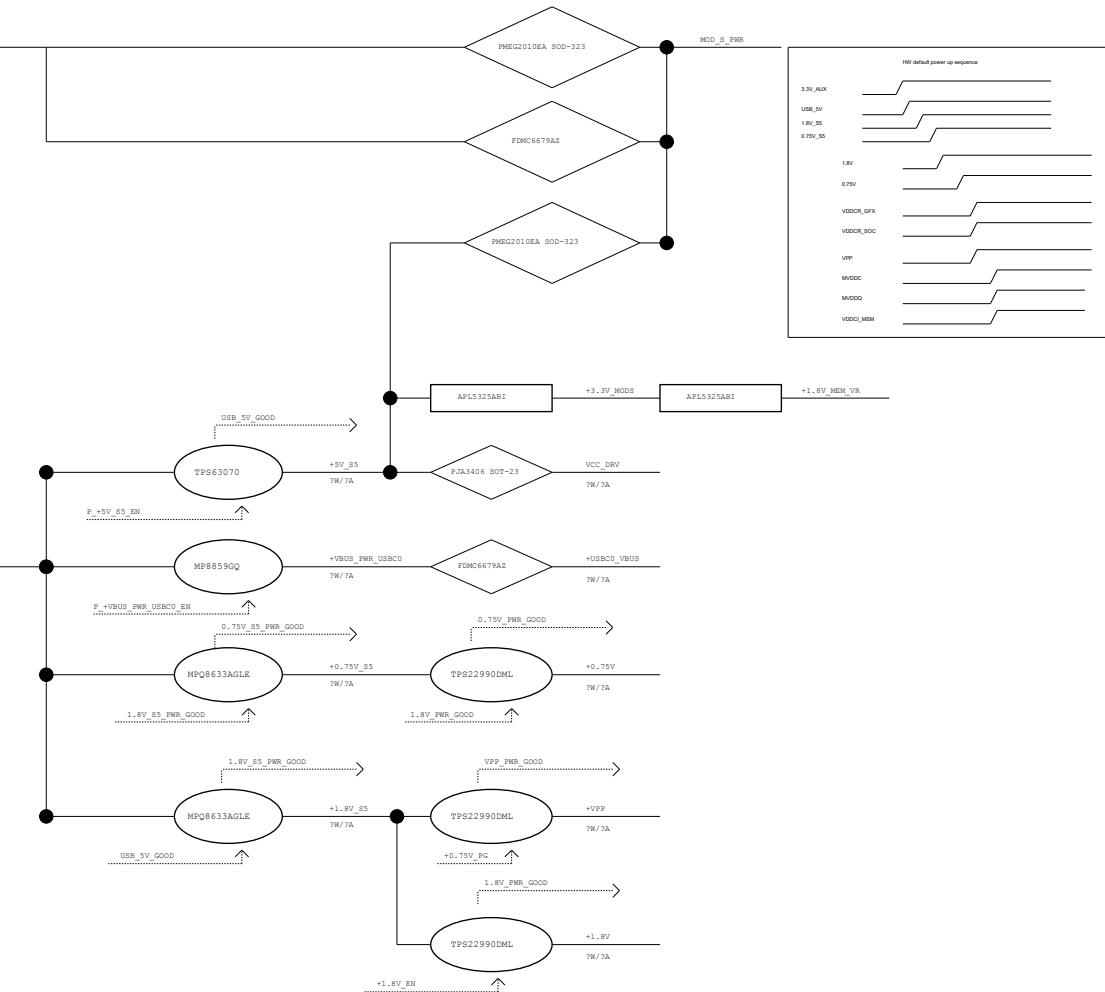
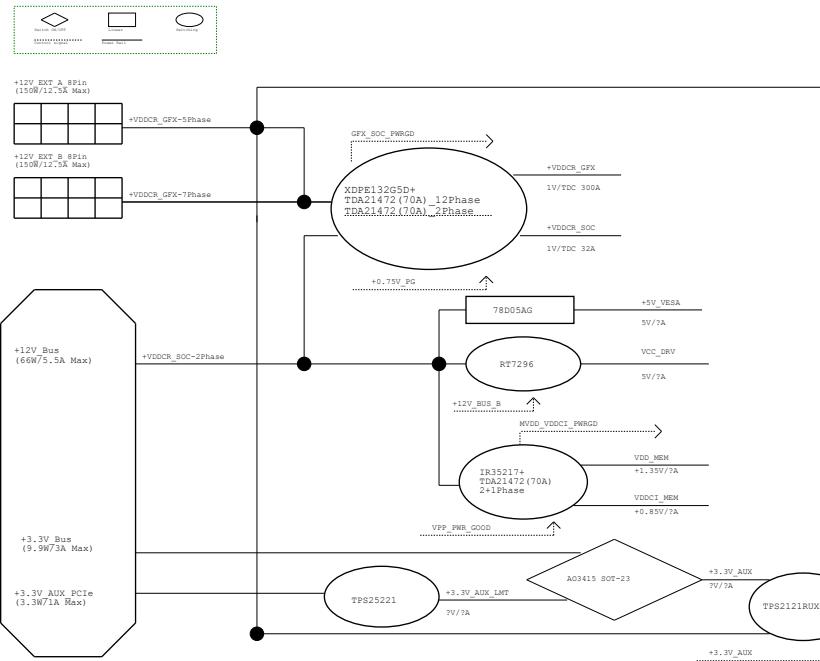


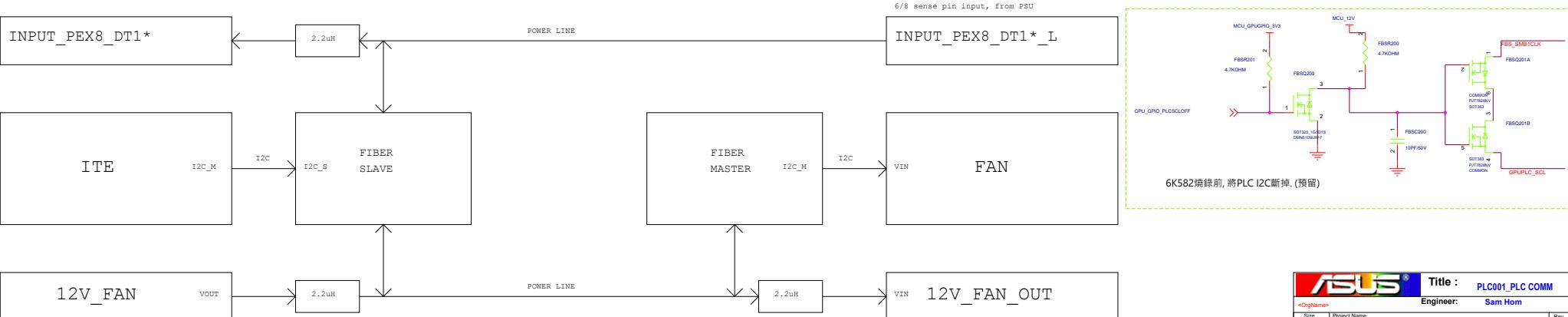
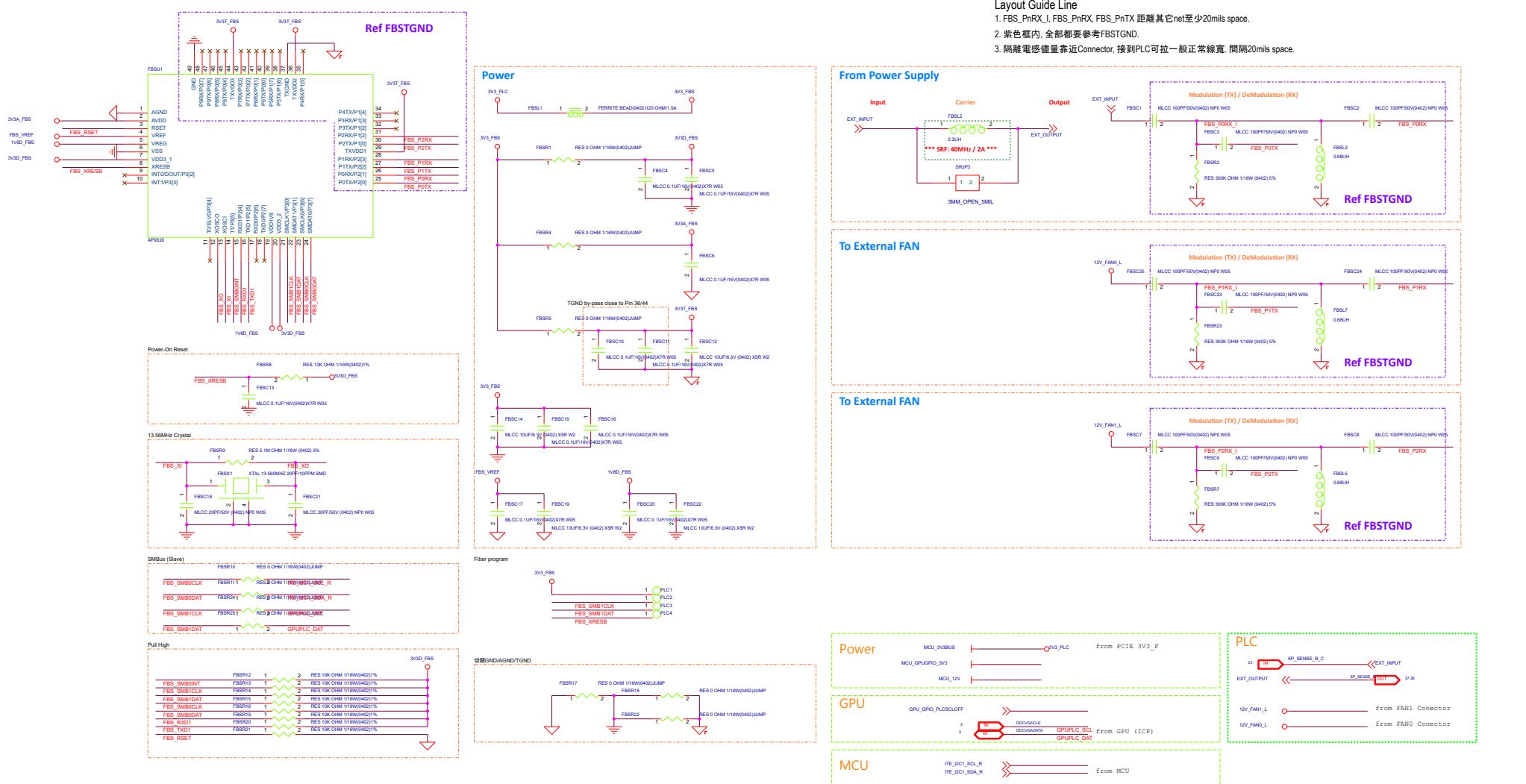


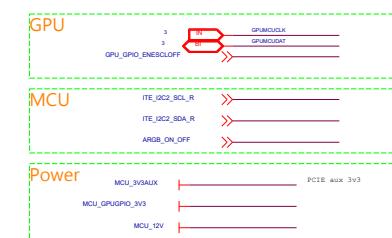
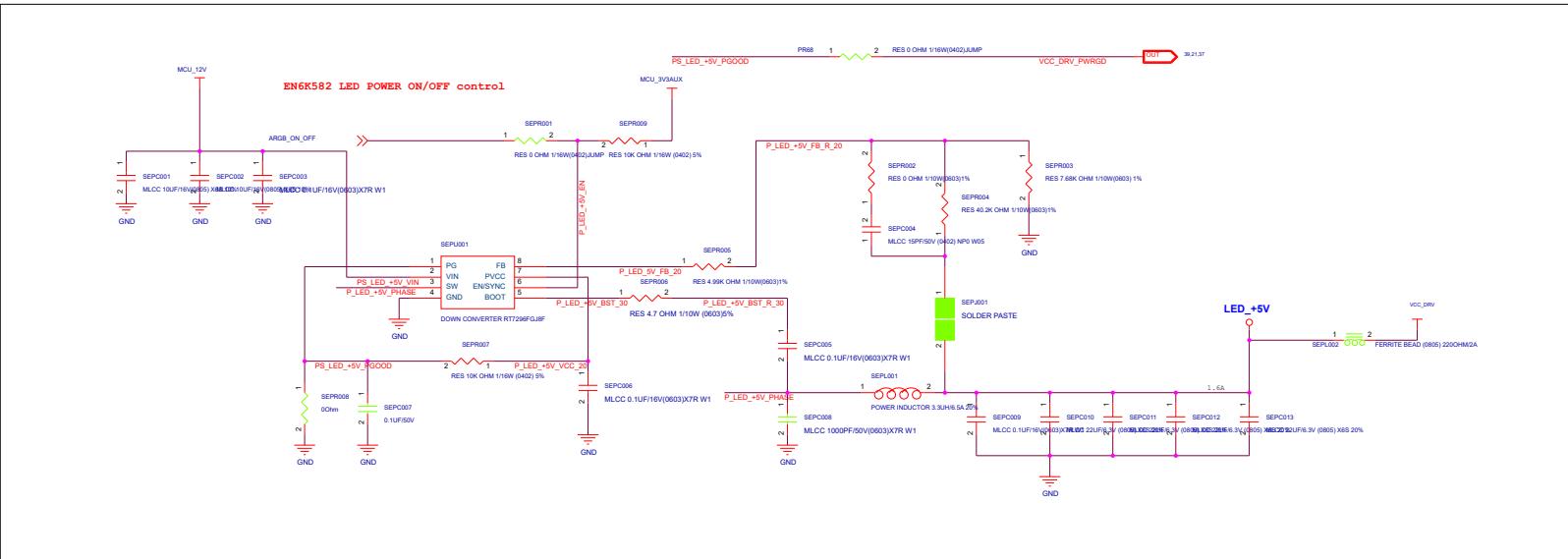
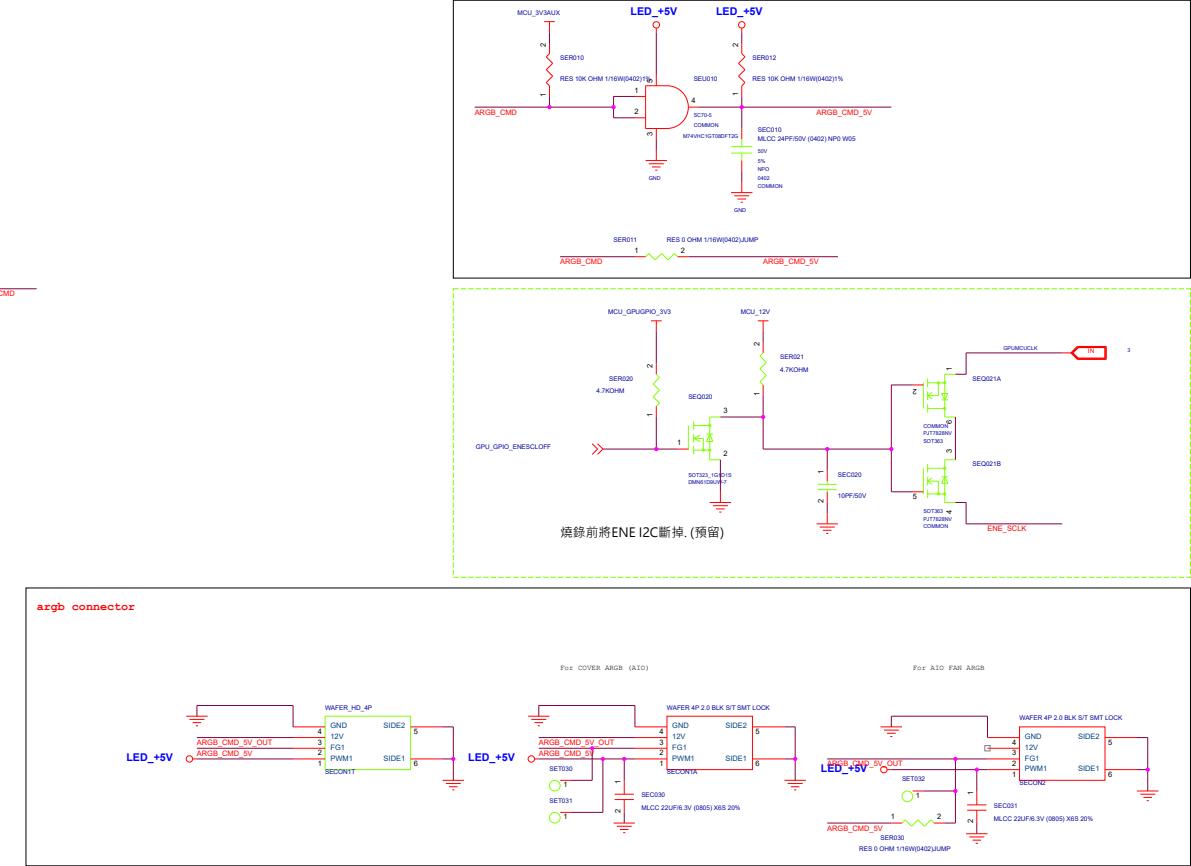
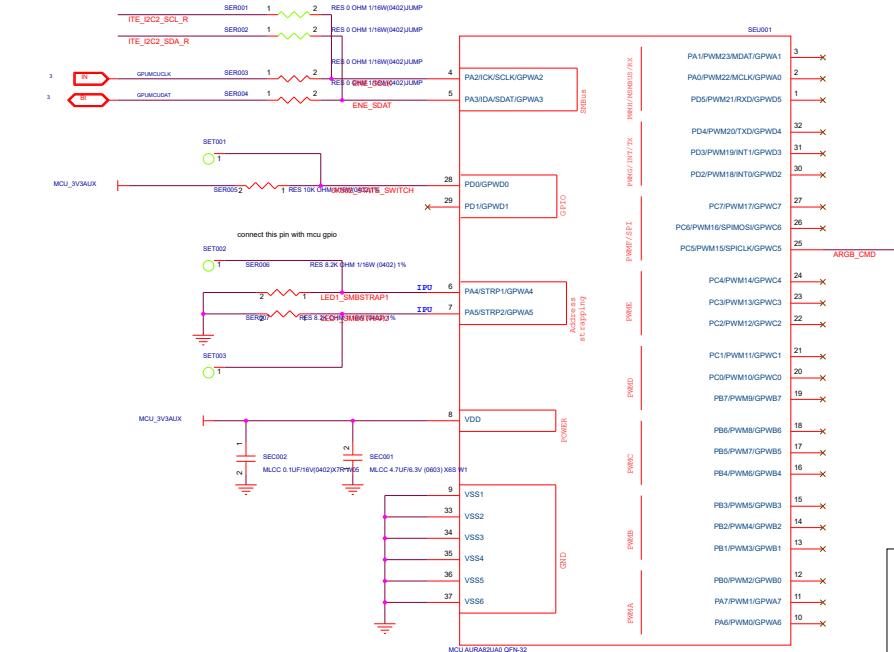
1 -00B
Nov 11 Added MODS circuit
2018

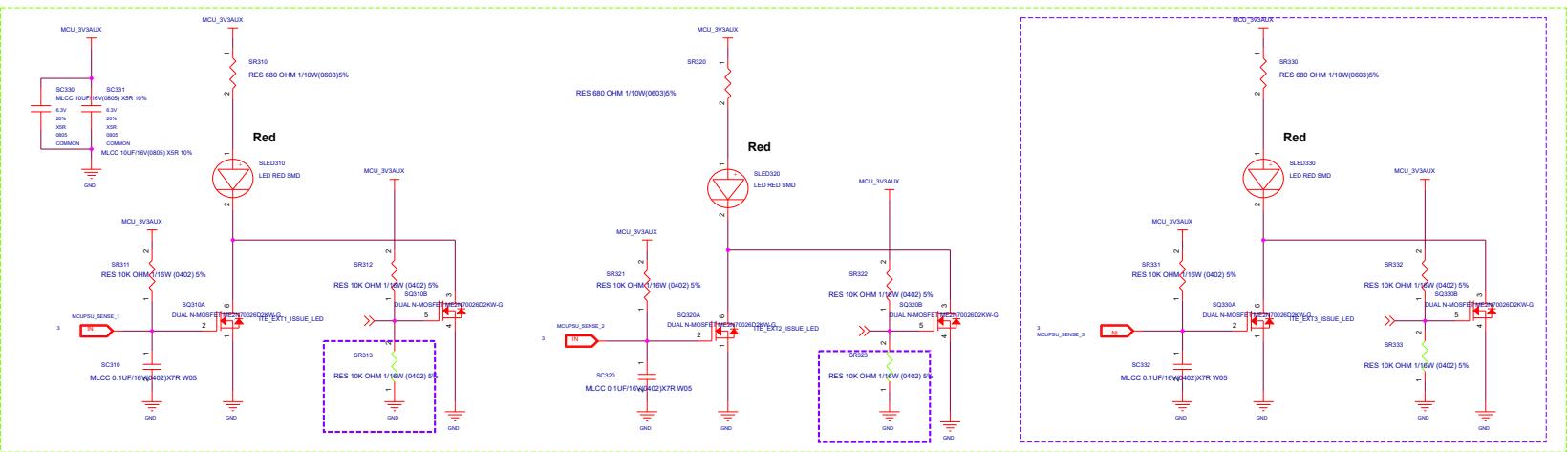
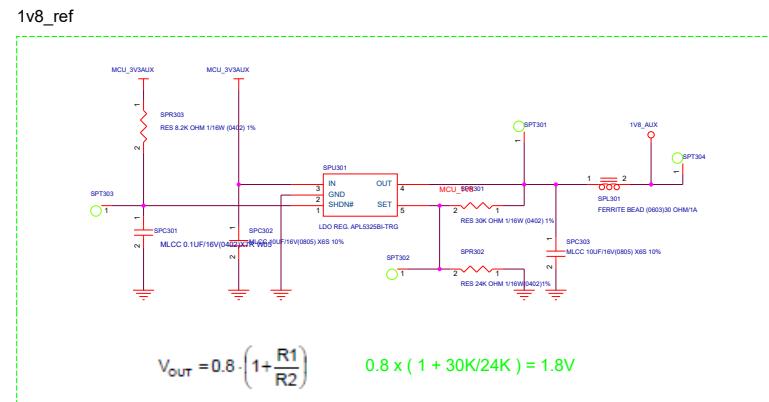
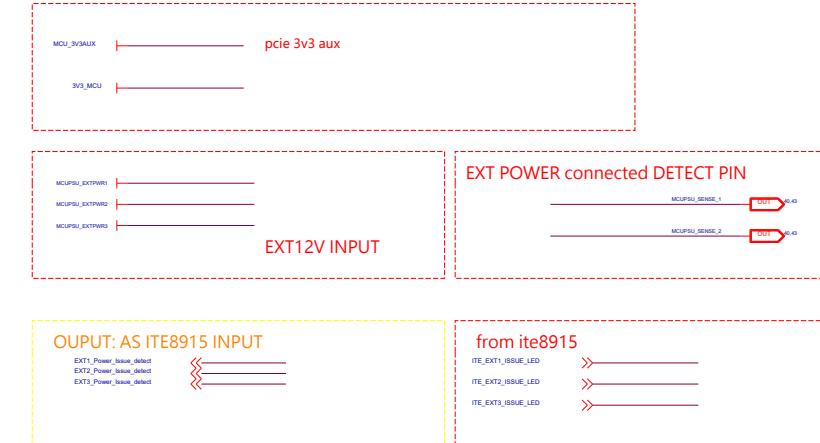
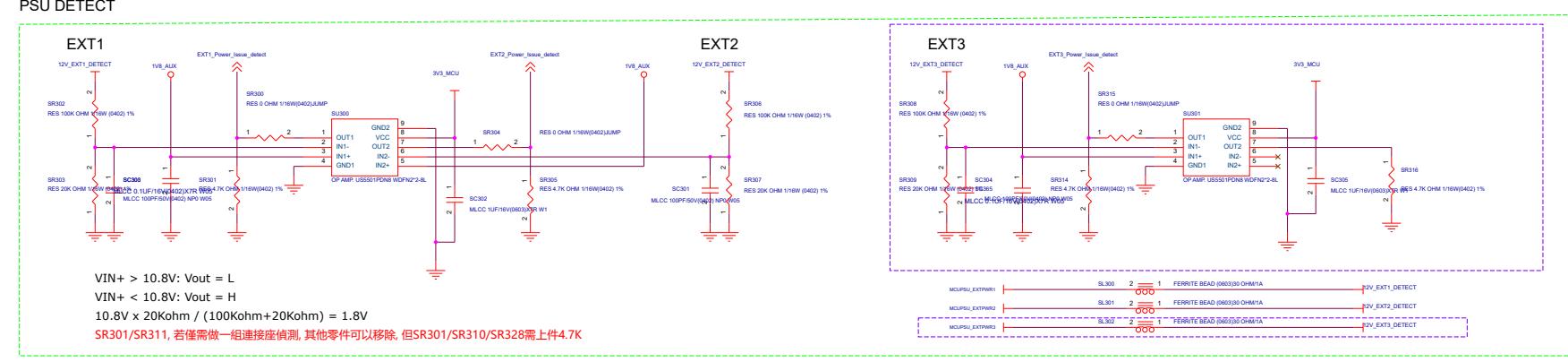
1 -00C
Jan 19 Connected +12V_S0 to OSC_VDD18
2018
Gated +VBUS_U_PWR_USB03 by
USB_A_C_D_S007 Power protection
2018

POWER FLOW

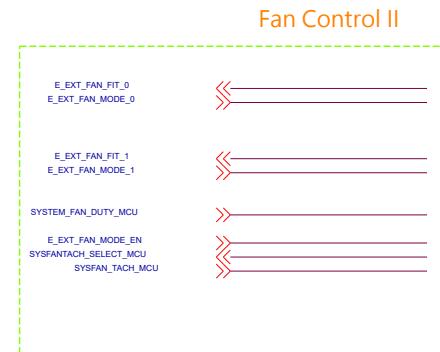
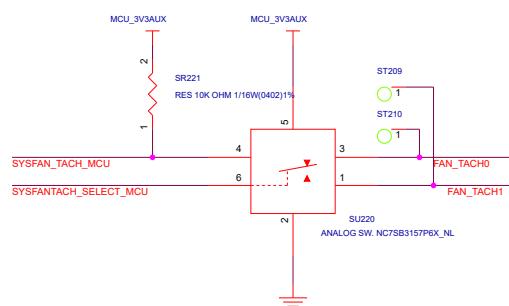
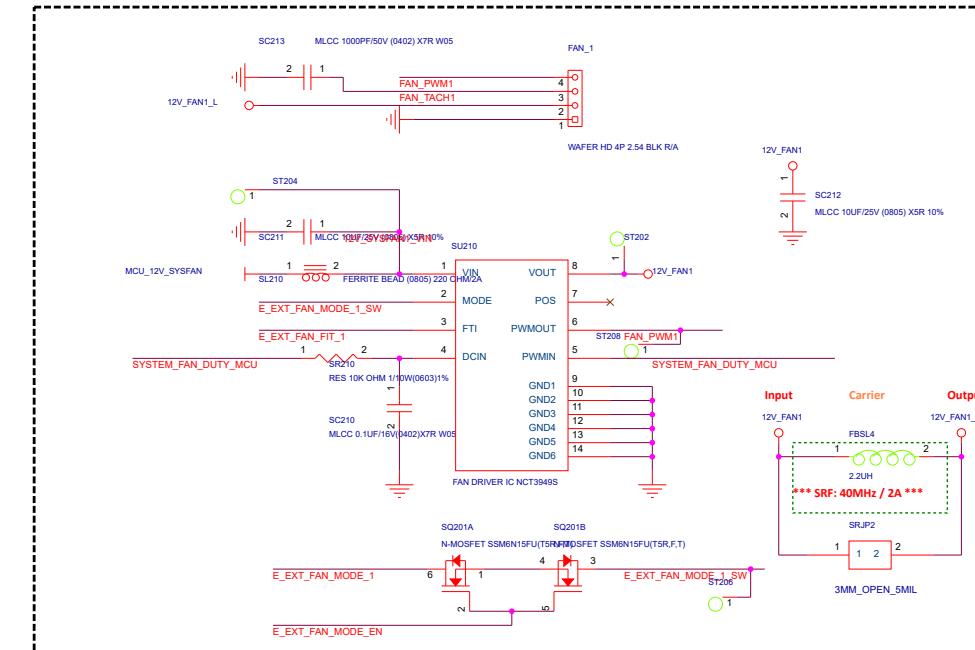
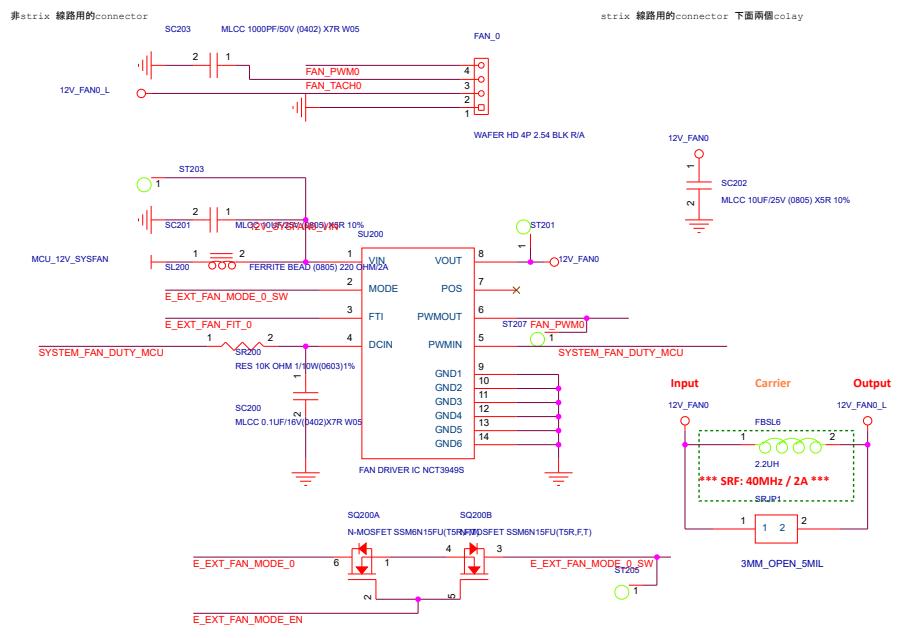




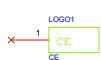




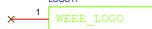
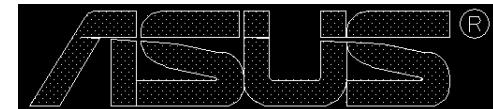
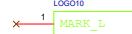
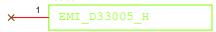
- 1.EXT power is not connected, the led is always on
- 2.EXT power is connected
EXT 12V is over 10.8V, the led turns off
EXT 12v is below 10.8v the led blink



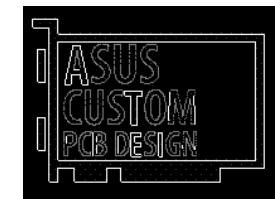
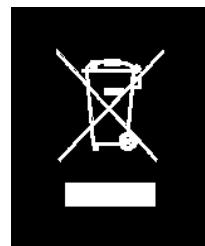
ASUS VGA PCB Logo



PCB MADE IN CHINA



ASUS Re-design logo
Do not place this on reference board



CAN ICES-3 (B) / NMB-3(B)



Title : XX ASUS PCB Logo	
<OrgName>	Project Name
Size	Rev
A3	D412BS
Date: Tuesday November 10, 2020	Sheet S1 of S1