PCI-EXPRESS EDGE CONNECTOR

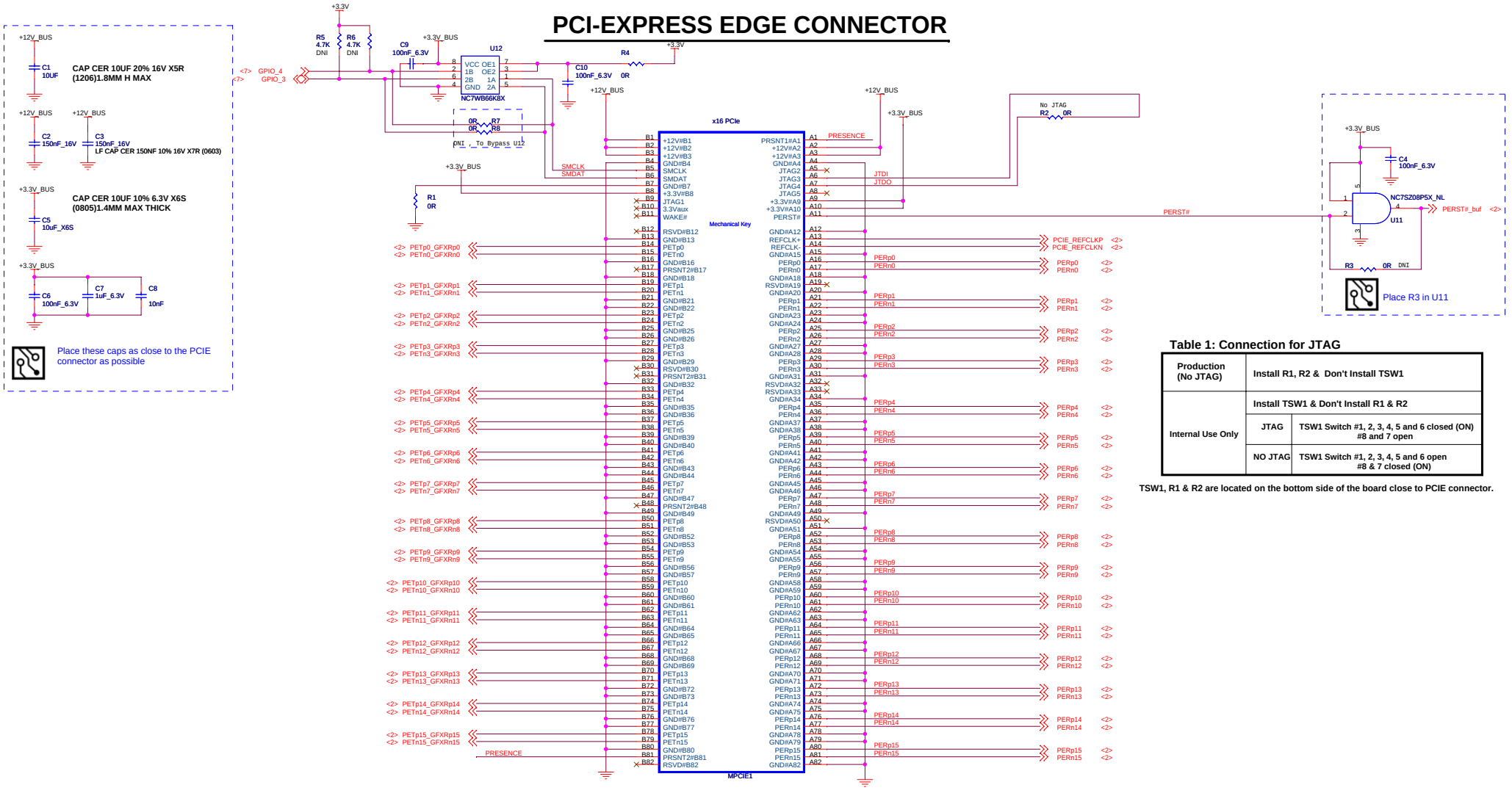

Table 1: Connection for JTAG

Production (No JTAG)	Install R1, R2 & Don't Install TSW1	
Internal Use Only	Install TSW1 & Don't Install R1 & R2	
	JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open
	NO JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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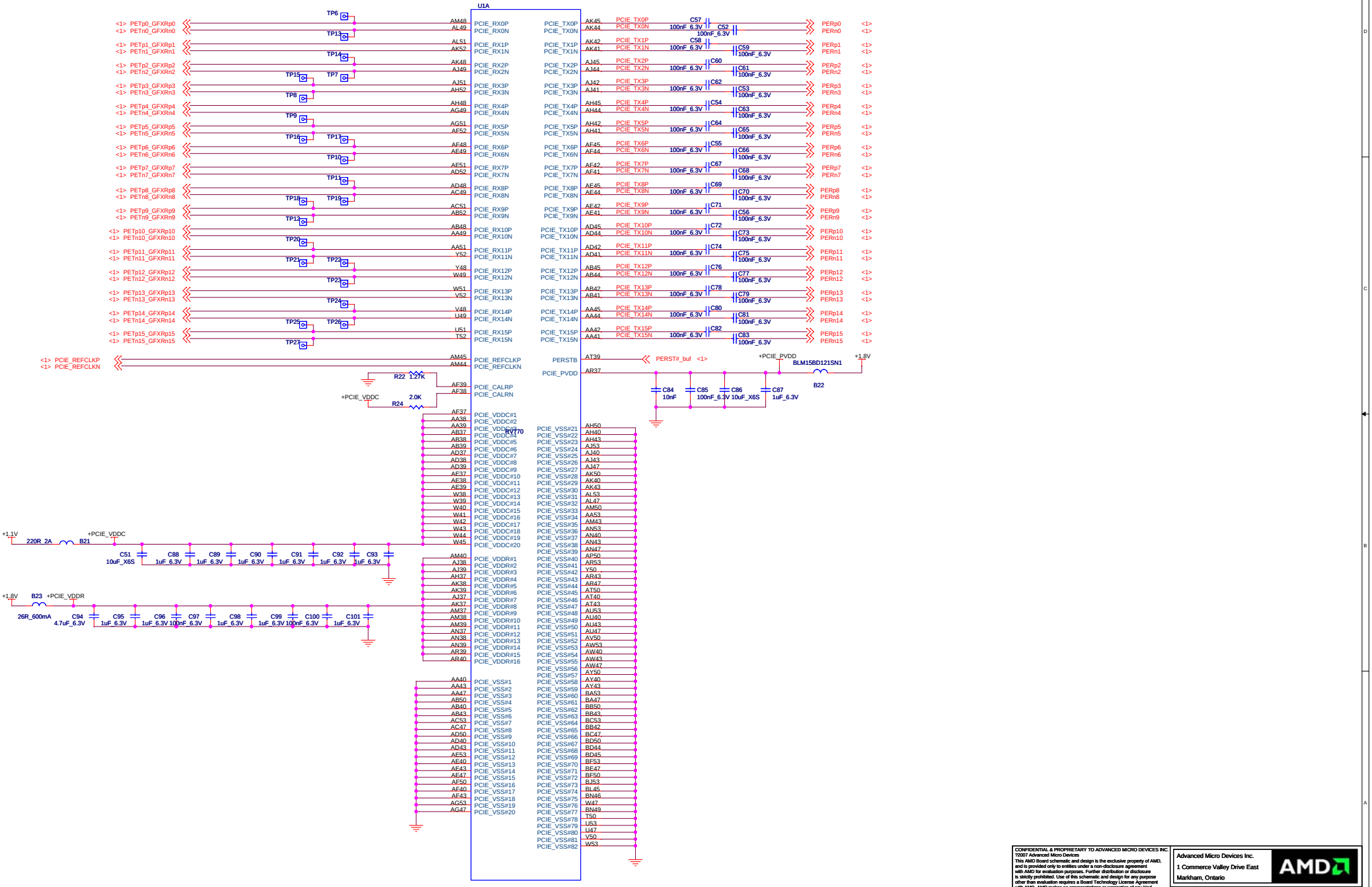
Title: RH PCIE RV770 512MB GDDR3 DVI DL DVI LVO FH

Doc No: 105-B50102-00

NOTE: some of the PCIE testpoints will
be available trought via on traces.



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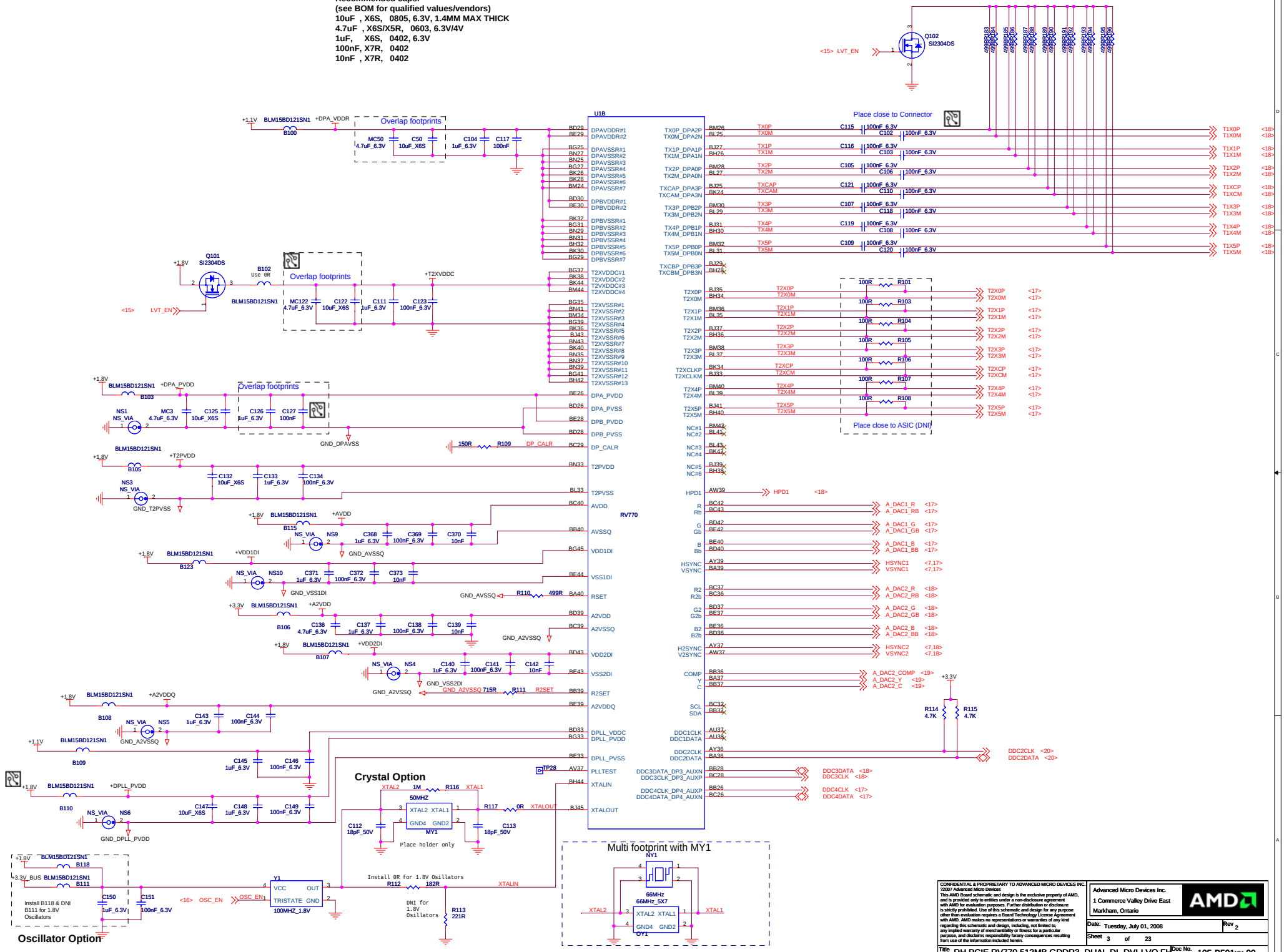
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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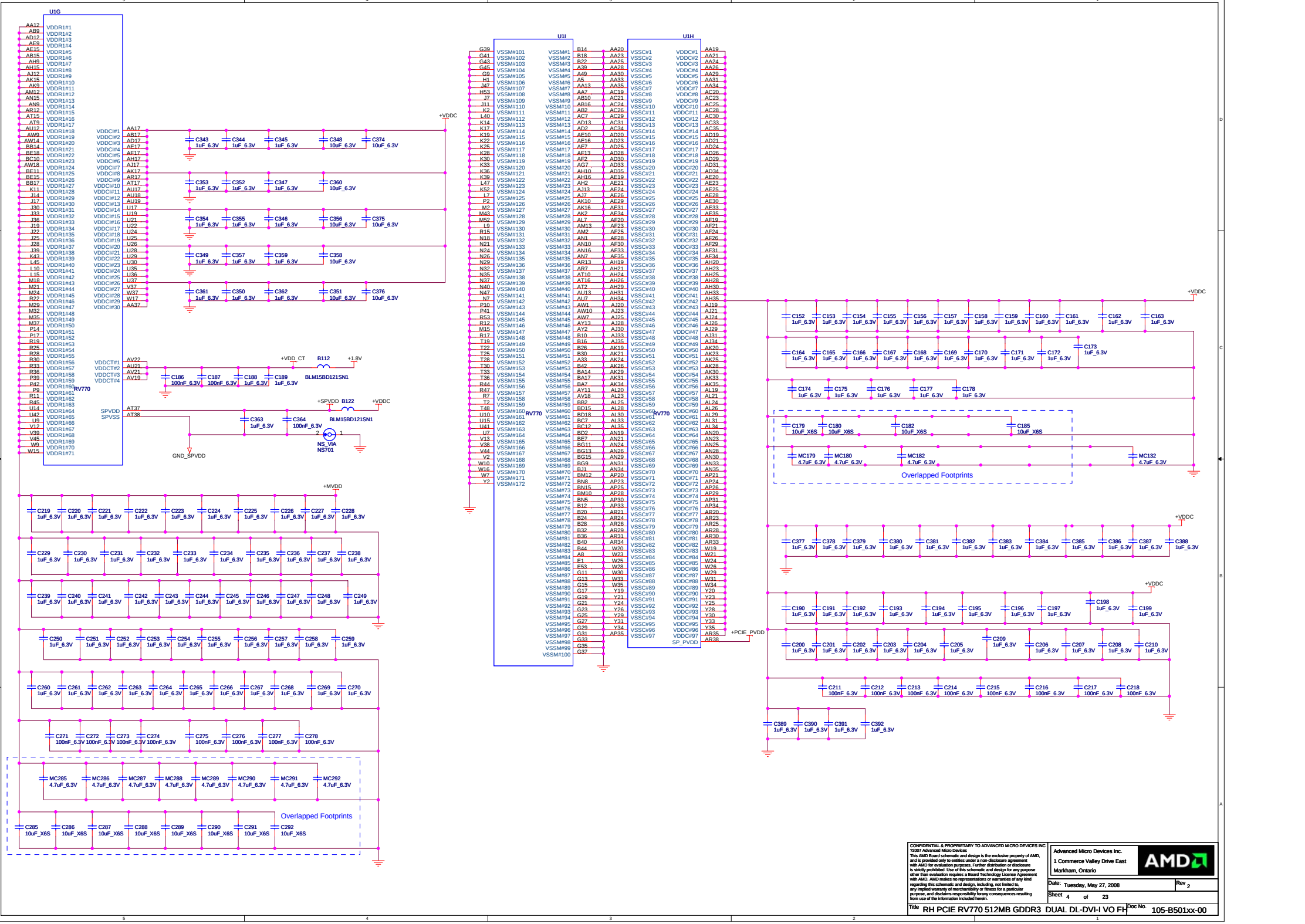

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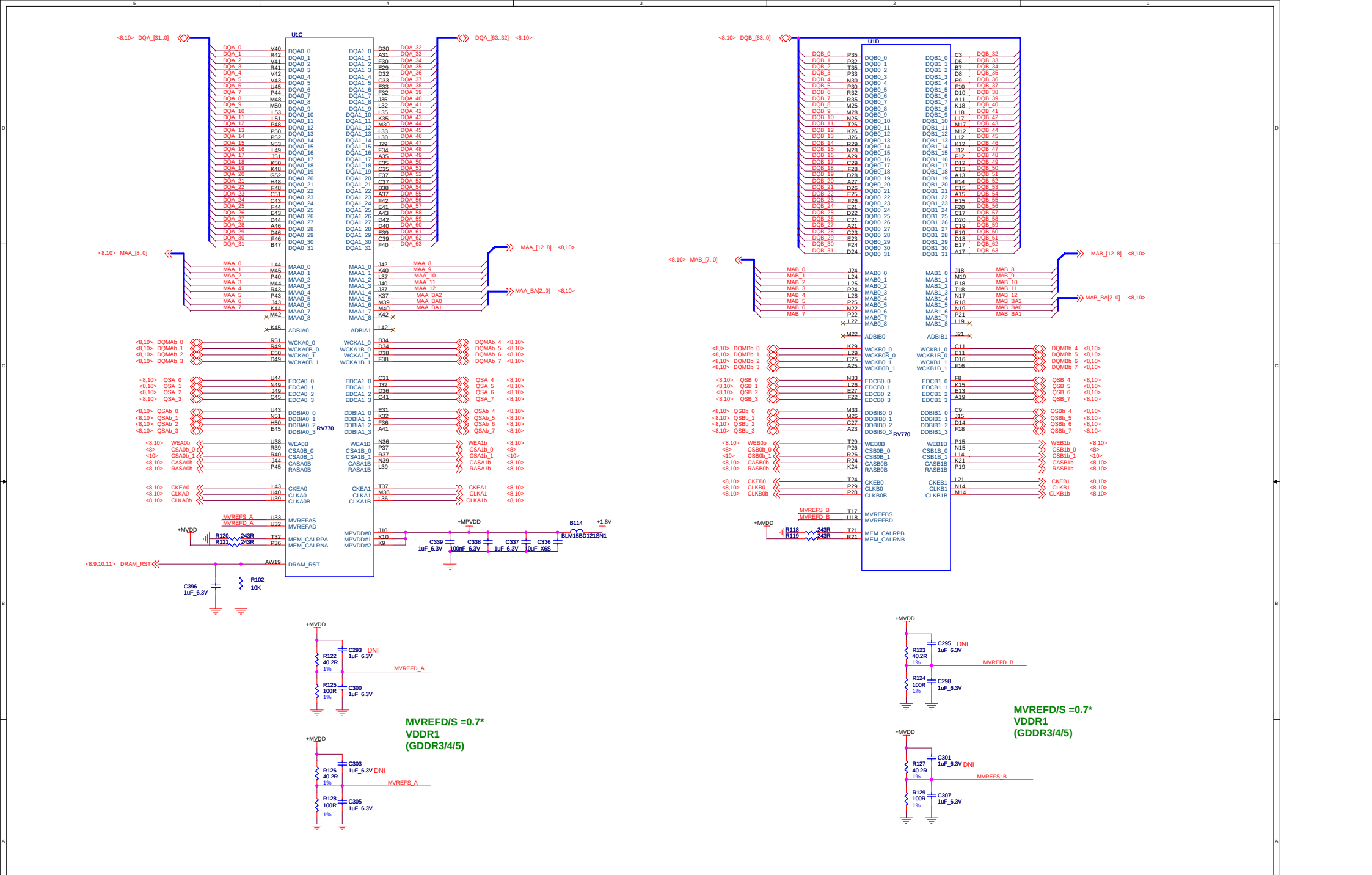

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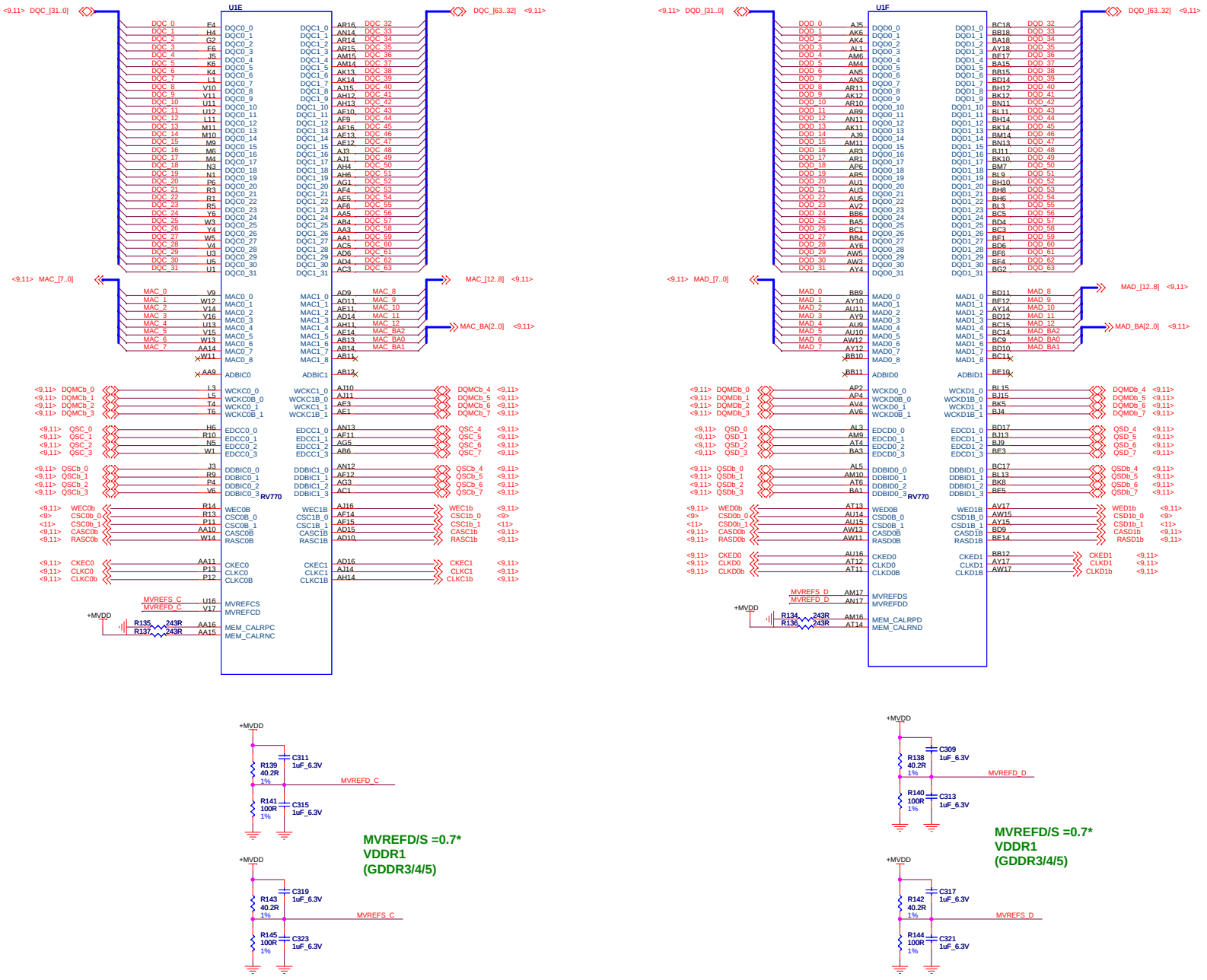
DAL 105-B50100-00



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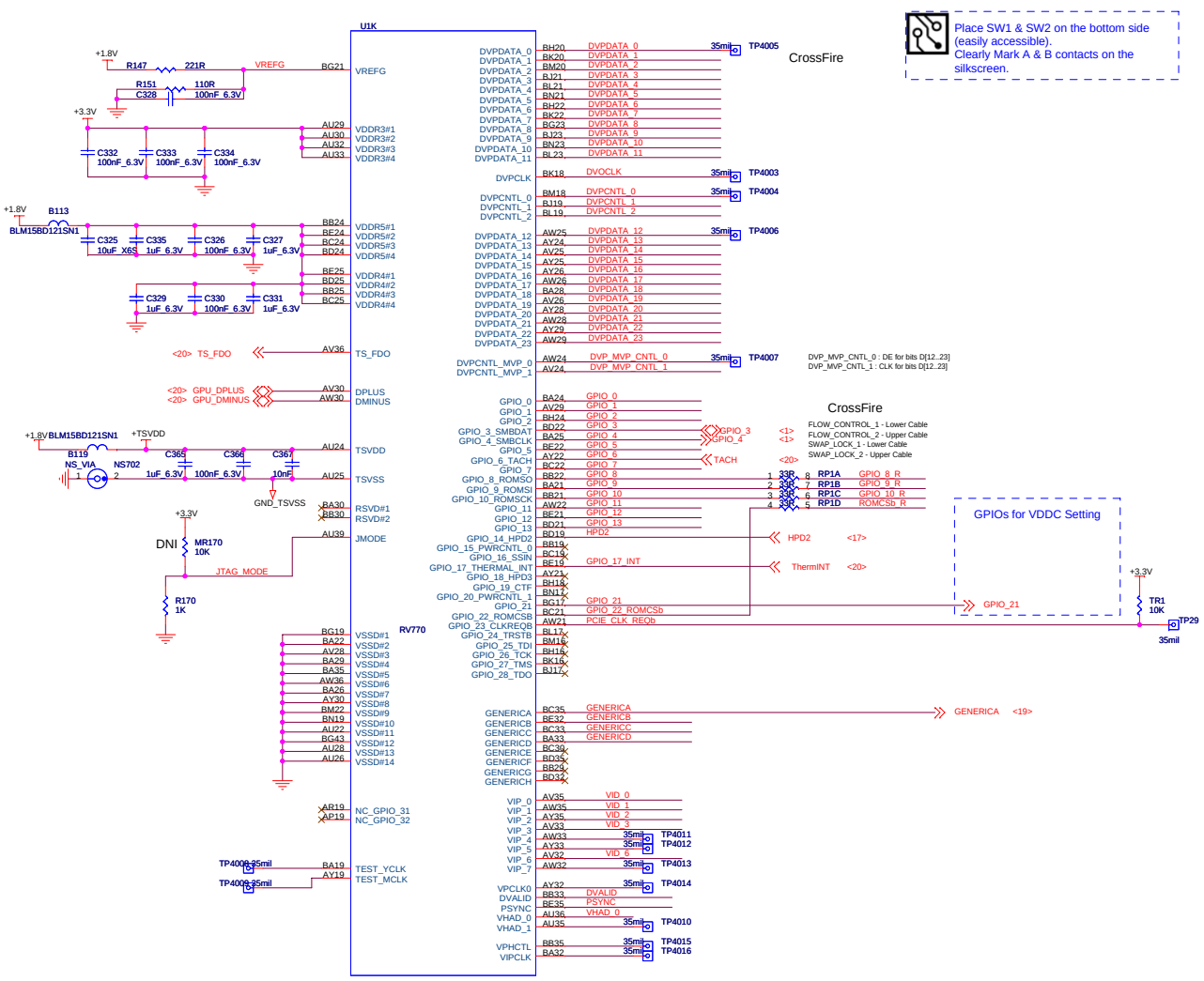
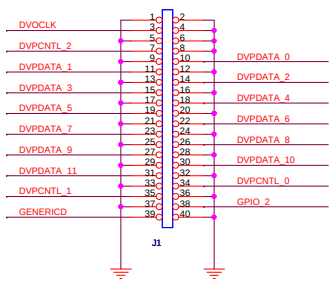
Title: RH PCIE RV770 512MB GDDR3 DDR4 DL DVI-I VO FH

Drawing No: 105-B50100-00



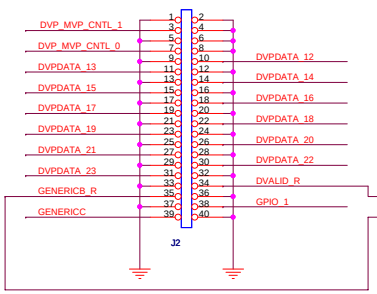
CrossFire Card-Edge

Lower Cable Card Edge

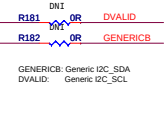


Bundle B

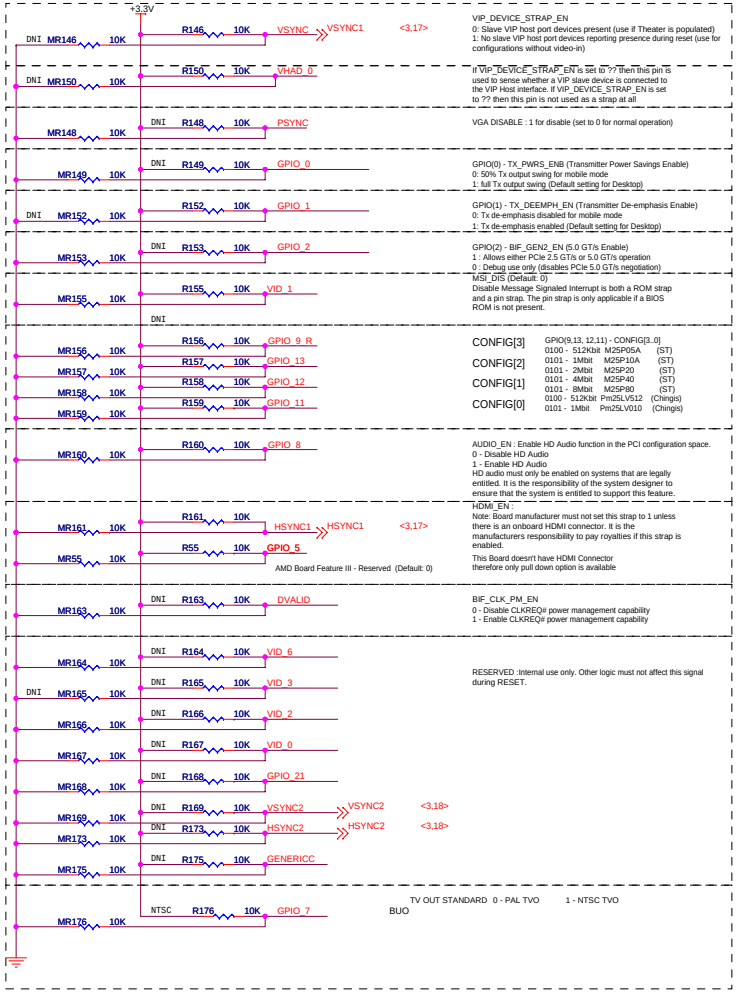
Upper Cable Card Edge



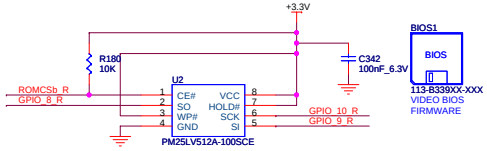
Bundle A (closer to the bracket)



PIN BASED STRAPS



Pull-Down Resistors are for BU until built-in pull-downs are verified.



PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

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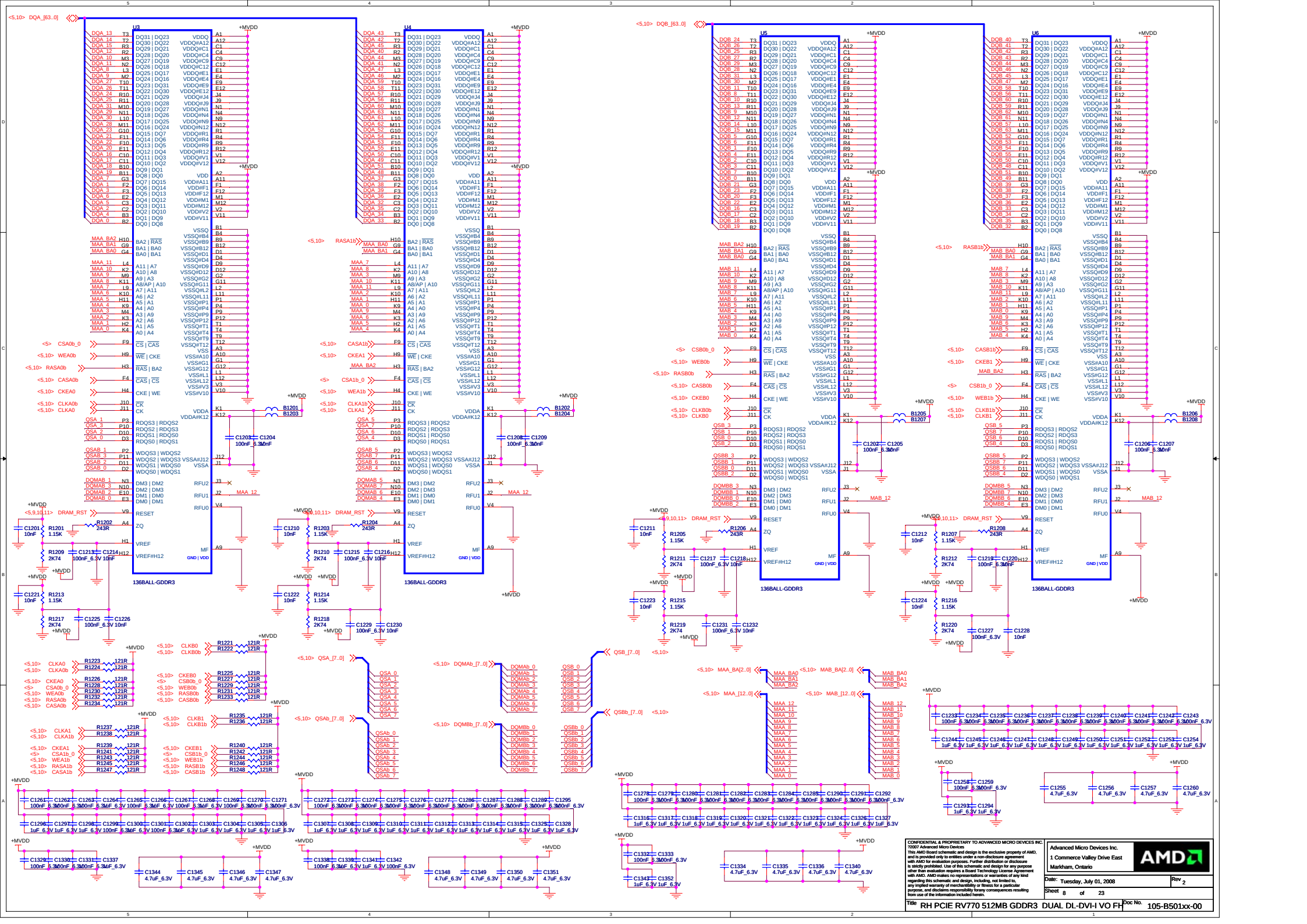

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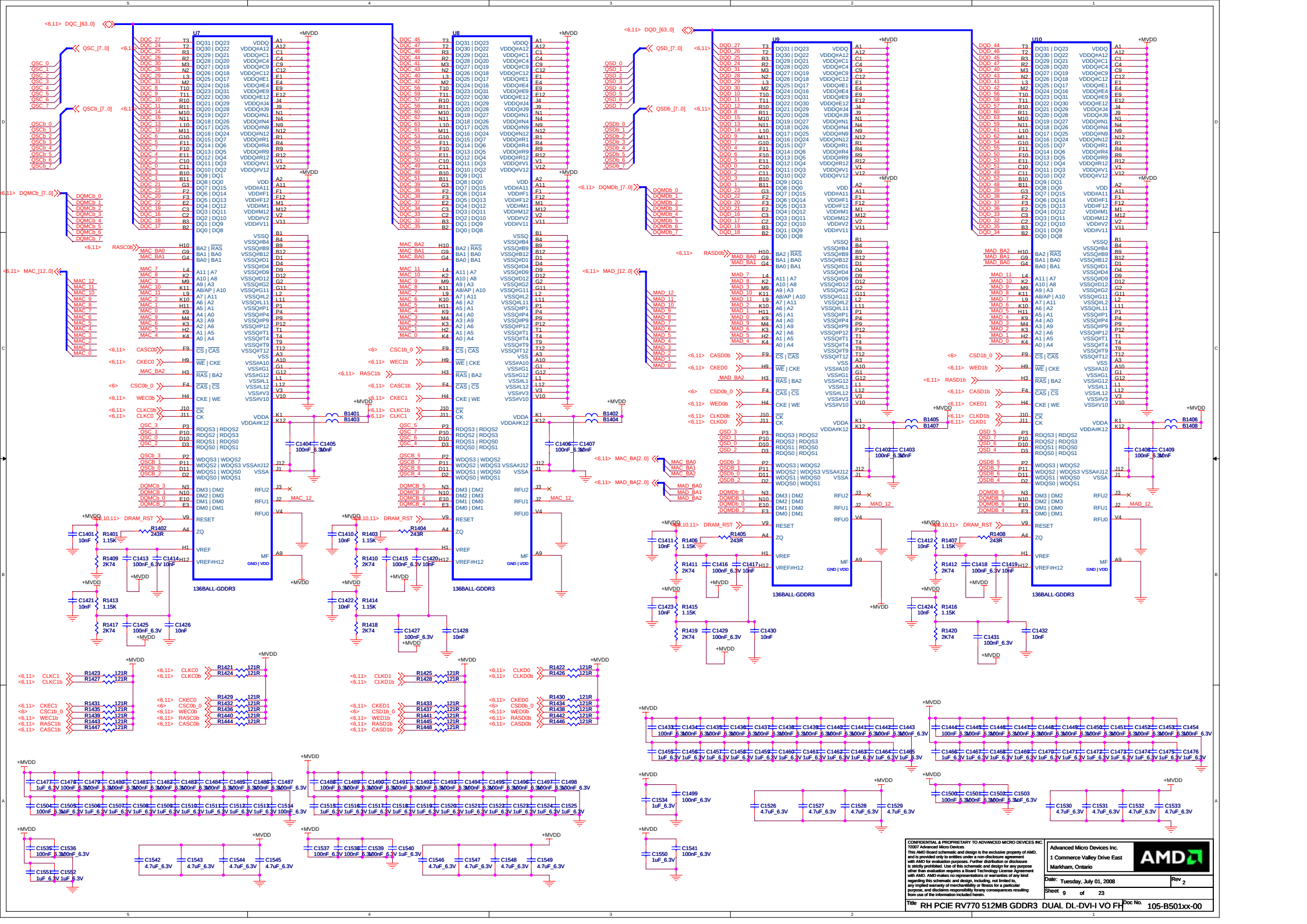

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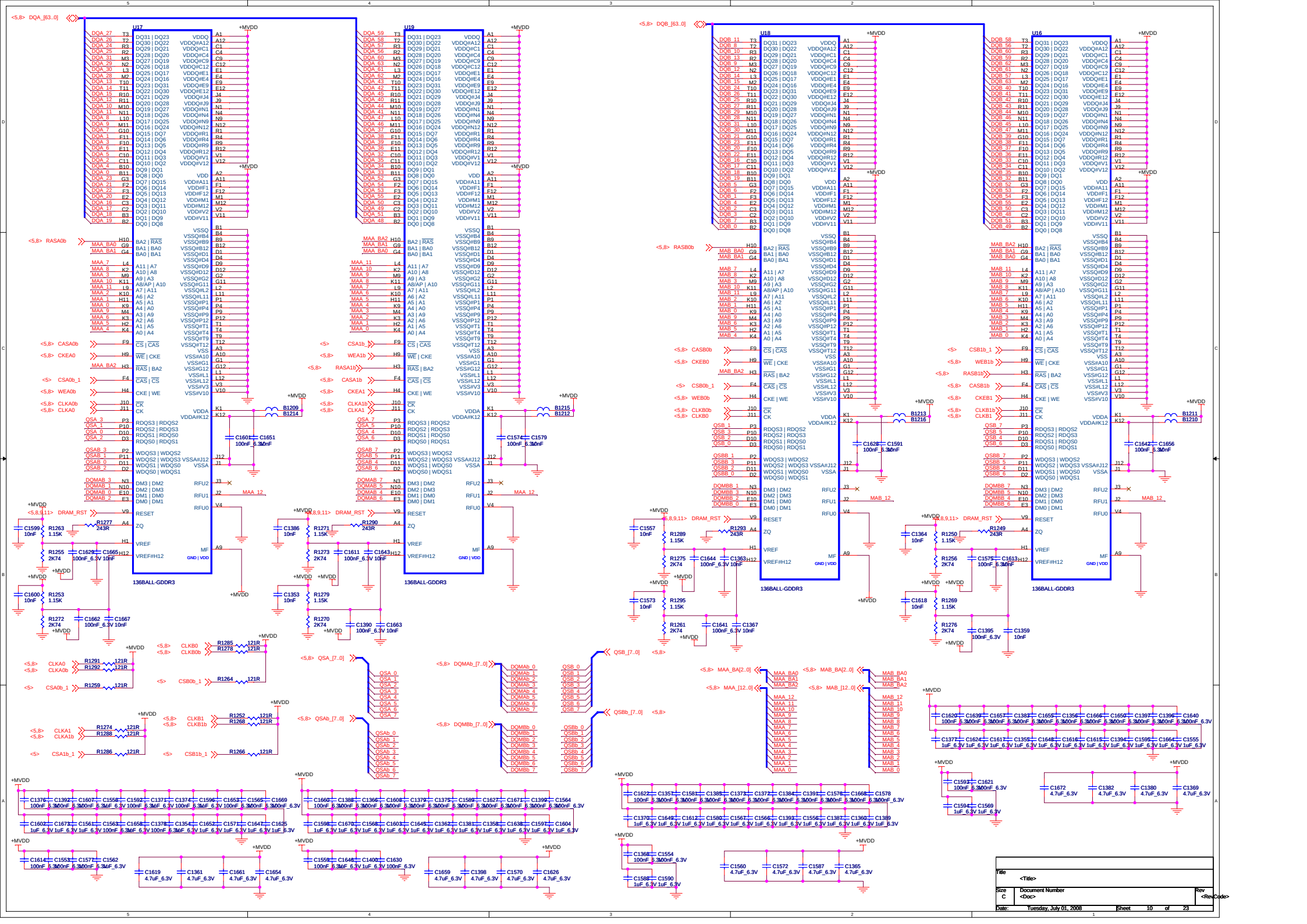

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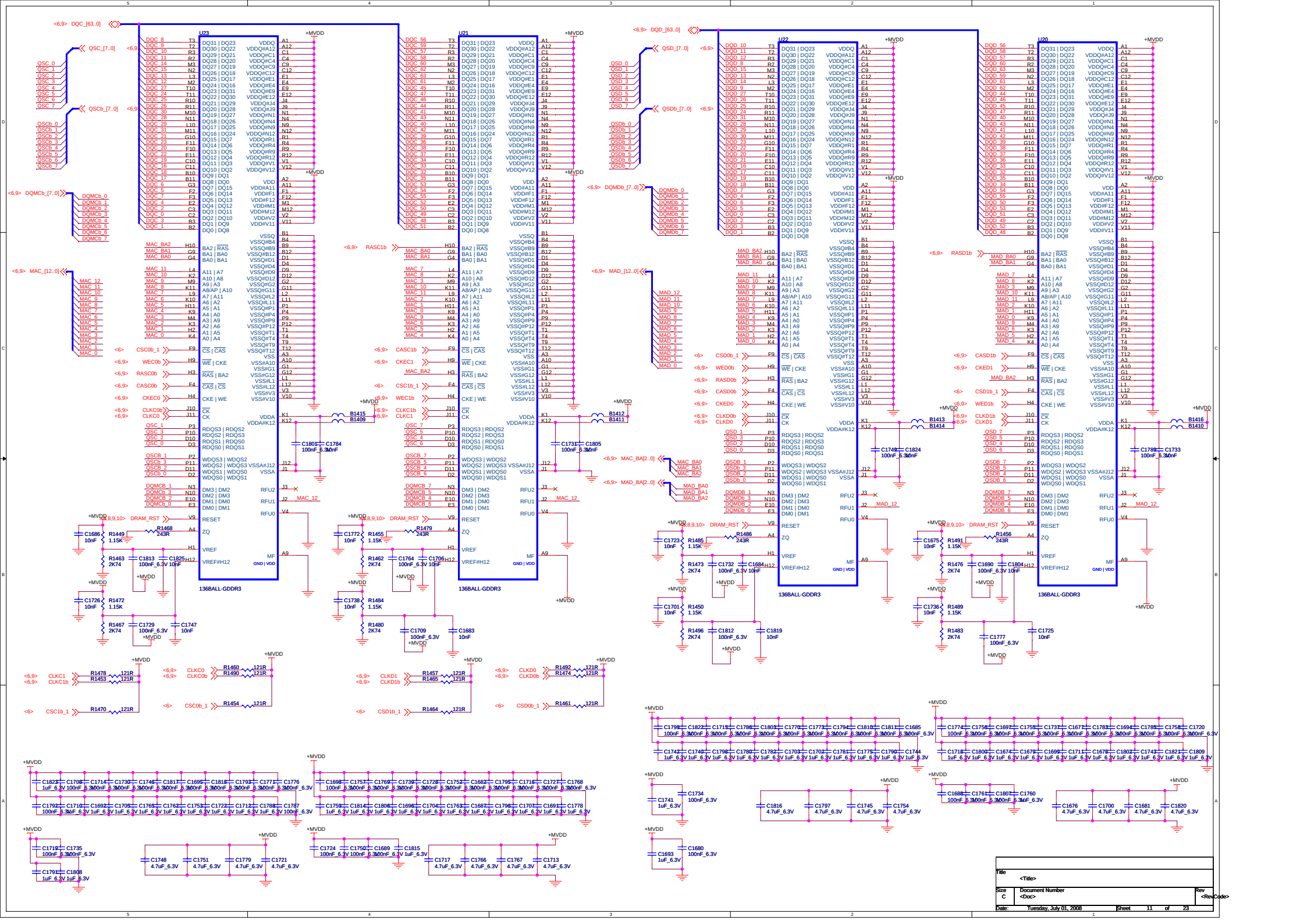
U23
U21
U22
U20
136BALL-GDDR3
136BALL-GDDR3
136BALL-GDDR3
136BALL-GDDR3
+MVDD
DQC_[63..0]
QSC_[7..0]
QSCb_[7..0]
DQMCb_[7..0]
MAC_[12..0]
DQD_[63..0]
QSD_[7..0]
QSDb_[7..0]
DQMDb_[7..0]
MAD_[12..0]
RASC1b
CASC1b
CKEC1
CSC1b_1
WEC1b
CLKC1b
CLKC1
RASD1b
CASD1b
CKED1
CSD1b_1
WED1b
CLKD1b
CLKD1
CSC0b_1
WEC0b
RASC0b
CASC0b
CKEC0
CLKC0b
CLKC0
CSD0b_1
WED0b
RASD0b
CASD0b
CKED0
CLKD0b
CLKD0
MAC_BA[2..0]
MAD_BA[2..0]
DRAM_RST
CLKC1
CLKC1b
CLKC0
CLKC0b
CLKD1
CLKD1b
CLKD0
CLKD0b
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CSC0b_1
CSD1b_1
CSD0b_1
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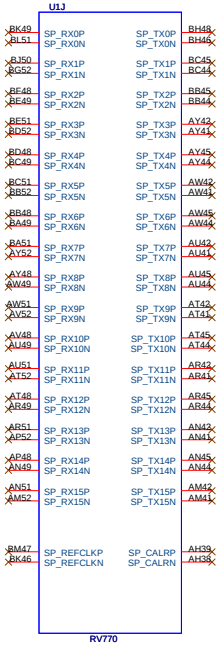

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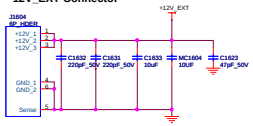
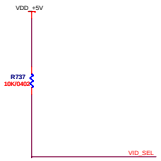
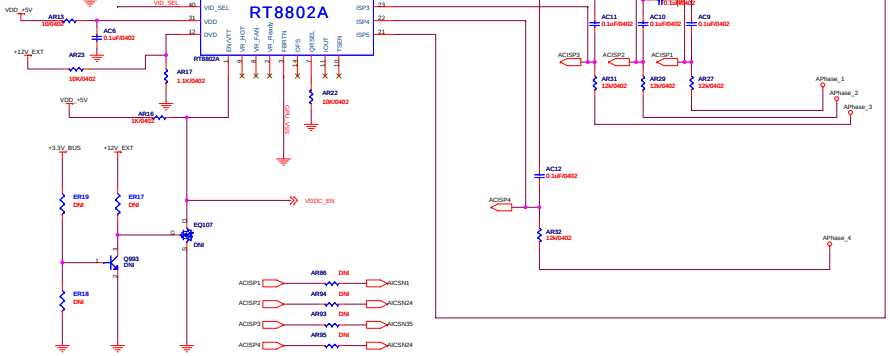
Install AR47 for Disable PWM3 function

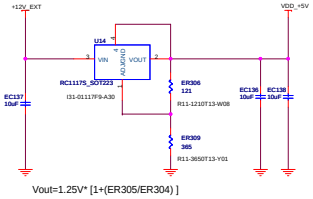
+VDDC=0.8 * (1+ (AR49 / AR82))

12V_EXT Connector

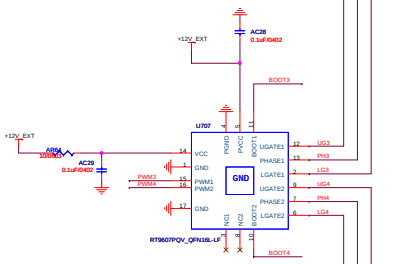


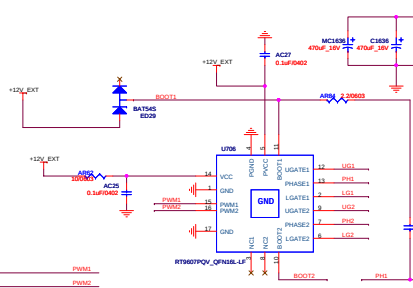


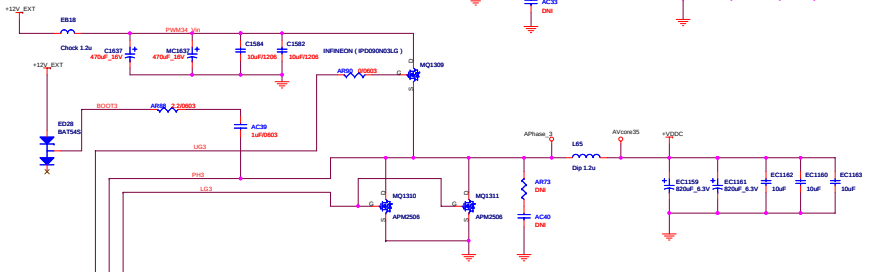


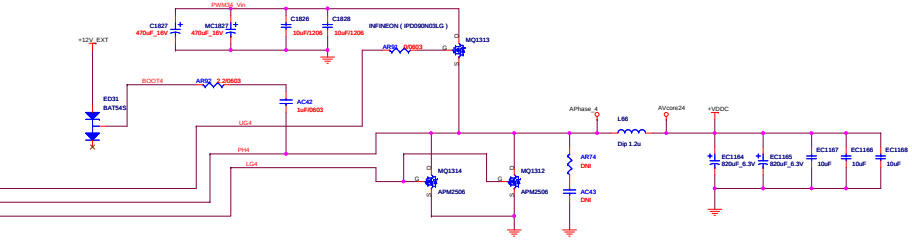


Vout=1.25V* [1+(ER305/ER304)]









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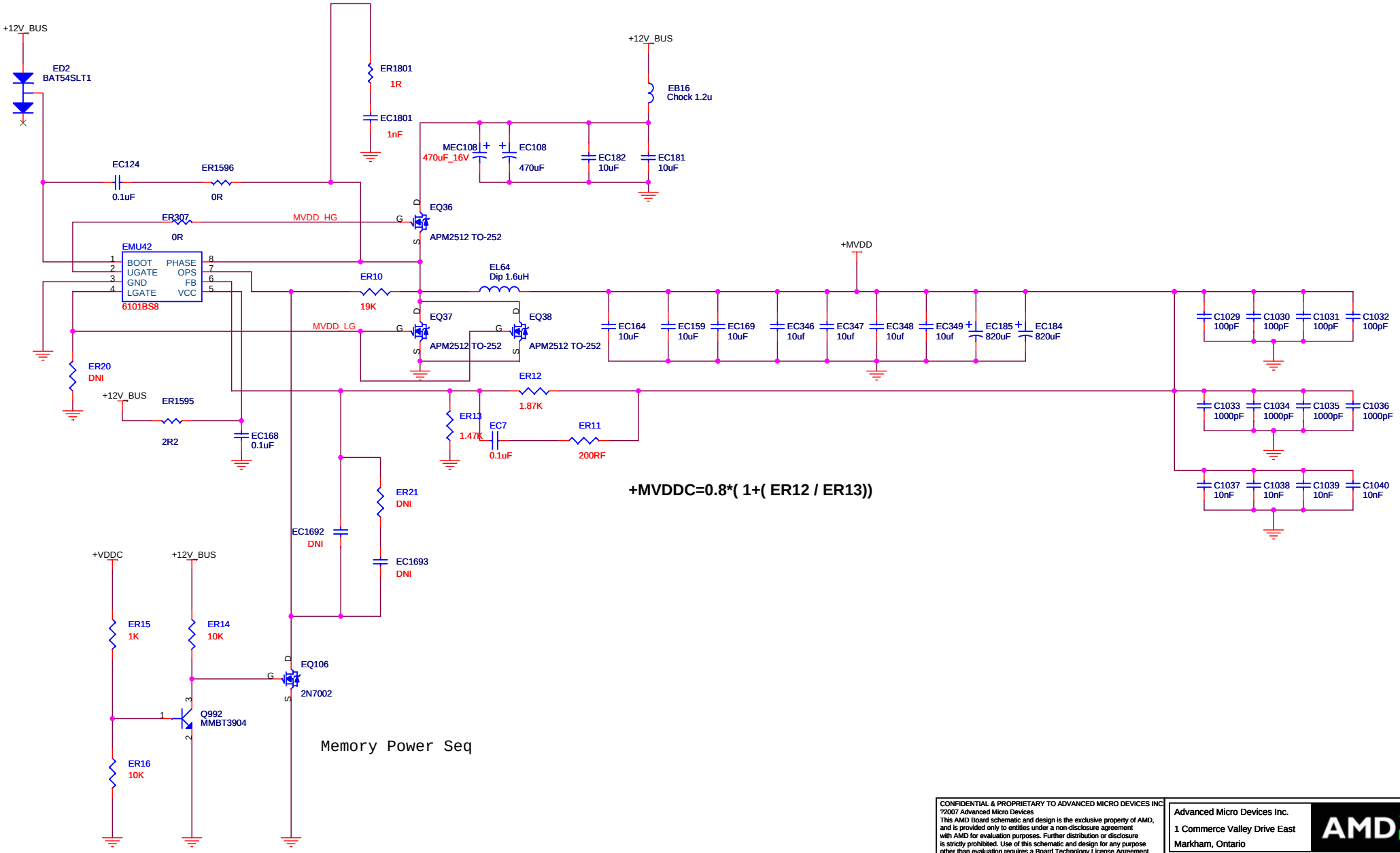

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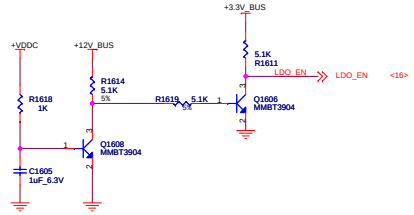
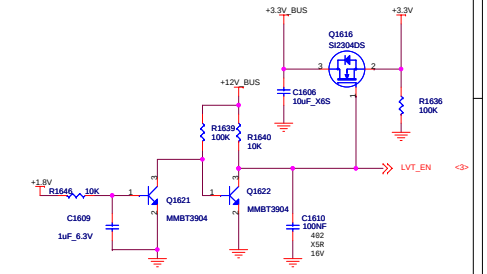
Power up Sequencing





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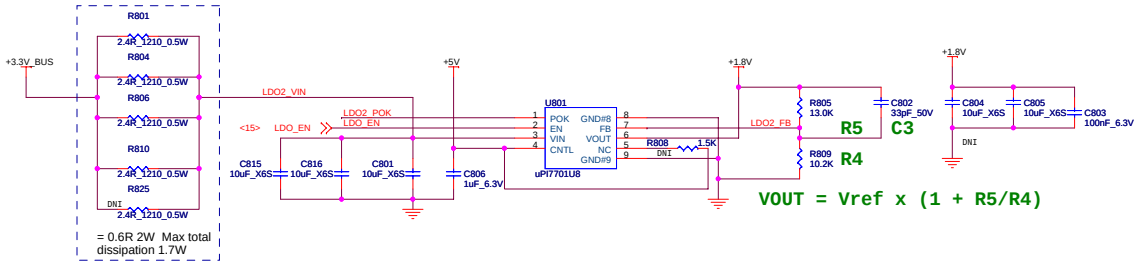
Regulators for +5V, +5V_VESA and +5V_VESA2

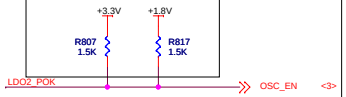
LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 1.7A (TBV) RMS MAX

PCB: Min 70mm sq. copper area for cooling



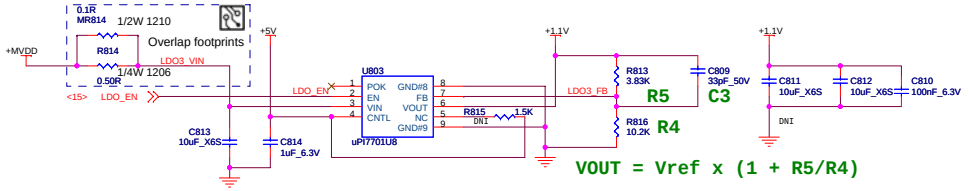
Install R817 if Y1 is a 1.8V Device

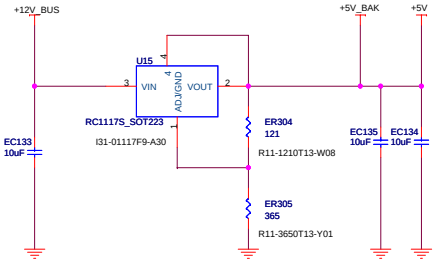
Install R807 if Y1 is a 3.3V Device

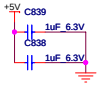


LDO #3: Vin = +1.50V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX

PCB: Min 70mm sq. copper area for cooling







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Doc No.	105-B501xx-00

See BOM for qualified filters

<3> A_DAC1_R — R1001 75R 402 — C1004 8.0pF 402 — L1001 47nH ML1001 36NH — C1001 12pF_50V 402
R1027 37.4R
<3> A_DAC1_RB

<3> A_DAC1_G — R1002 75R 402 — C1005 8.0pF 402 — L1002 47nH ML1002 36NH — C1002 12pF_50V 402
R1028 37.4R
<3> A_DAC1_GB

<3> A_DAC1_B — R1003 75R 402 — C1006 8.0pF 402 — L1003 47nH ML1003 36NH — C1003 12pF_50V 402
R1029 37.4R
<3> A_DAC1_BB

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

L100x and ML100x footprints are overlapped

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

For ESD Protection

+3.3V — D1001 CM1213-04 (CH3, CH2, Vp, Vn, CH4, CH1)
+5V_VESA — D1002 CM1213-04 (CH3, CH2, Vp, Vn, CH4, CH1)

+5V_VESA2 — +5V_VESA — +5V — EF1 0.2A

MJ1001 G3179C219-005
R, G, B, MS0, MS1, MS2, MS3, NC, HS, VS, VSS, VSS#6, VSS#7, VSS#8, VSS#10, CASE, CASE#17
DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

C1010 68pF 603

<3> DDC4DATA — +5V — R1005 2.2K — DDCDATA_DAC1_5V — R1006 33R 402 — DDCDATA_DAC1_R
<3> DDC4CLK — +5V — R1008 2.2K — DDCCLK_DAC1_5V — R1009 33R 402 — DDCCLK_DAC1_R

<3,7> HSYNC1 — C1999 100nF 6.3V — U1999A 74VHC125 — HSYNC_DAC1_B — R1010 10R 402 — HSYNC_DAC1_R
<3,7> VSYNC1 — 74VHC125 U1999B — VSYNC_DAC1_B — R1011 10R 402 — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

+3.3V — Q1021 MMBT3904 — R1022 10K — HPD_DVI2
<7> HPD2 — R1023 10K

+5V_VESA

J1001 DVI_CONNECTOR

<3> T2X2M	1	25	CASE
<3> T2X2P	2		TMDS Data2-
	3		TMDS Data2+
<3> T2X4M	4		TMDS Data2/4 Shield
<3> T2X4P	5		TMDS Data4-
DDCCLK_DAC1_R	6		TMDS Data4+
DDCDATA_DAC1_R	7		DDC Clock
VSYNC_DAC1_R	8		DDC Data
	9		Analog VSYNC
<3> T2X1M	10		TMDS Data1-
<3> T2X1P	11		TMDS Data1+
	12		TMDS Data1/3 Shield
<3> T2X3M	13		TMDS Data3-
<3> T2X3P	14		TMDS Data3+
	15		+5V Power
	16		GND (for +5V)
HPD_DVI2	17		Hot Plug Detect
<3> T2X0M	18		TMDS Data0-
<3> T2X0P	19		TMDS Data0+
	20		TMDS Data0/5 Shield
<3> T2X5M	21		TMDS Data5-
<3> T2X5P	22		TMDS Data5+
	23		TMDS Clock Shield
<3> T2XCP	24		TMDS Clock+
<3> T2XCM			TMDS Clock-
A_R_DAC1_F		C1	Analog Red
A_G_DAC1_F		C2	Analog Green
A_B_DAC1_F		C3	Analog Blue
HSYNC_DAC1_R		C4	Analog HYNC
		C5	Analog GND
		C6	Analog GND#C6
	26		CASE#26
	27		CASE#27
	28		CASE#28
	29		CASE#29
	30		CASE#30

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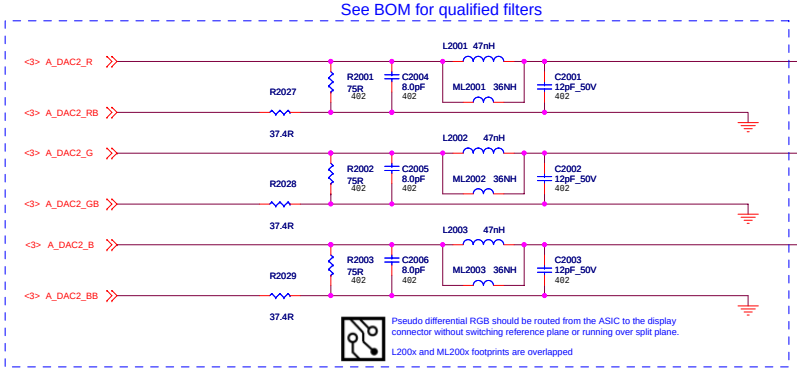
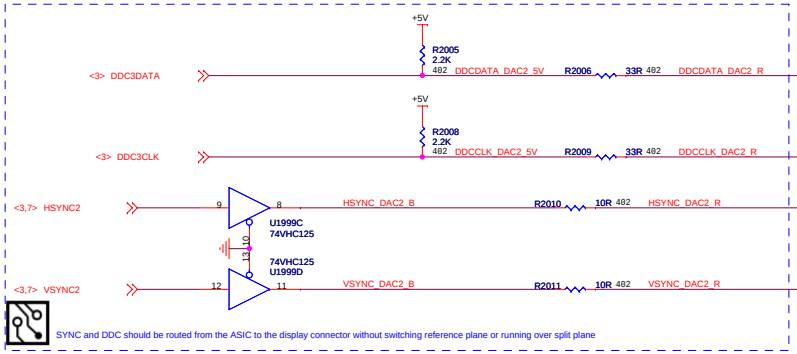
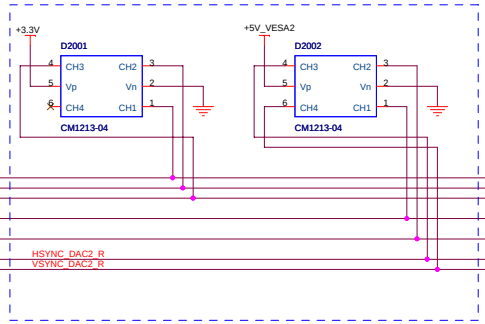
Title: RH PCIE RV770 512MB GDDR3 DUAL DL-DVI-I VO FH — Doc No. 105-B501xx-00

See BOM for qualified filters







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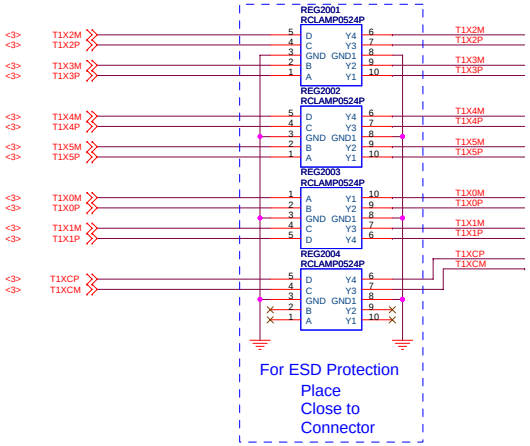
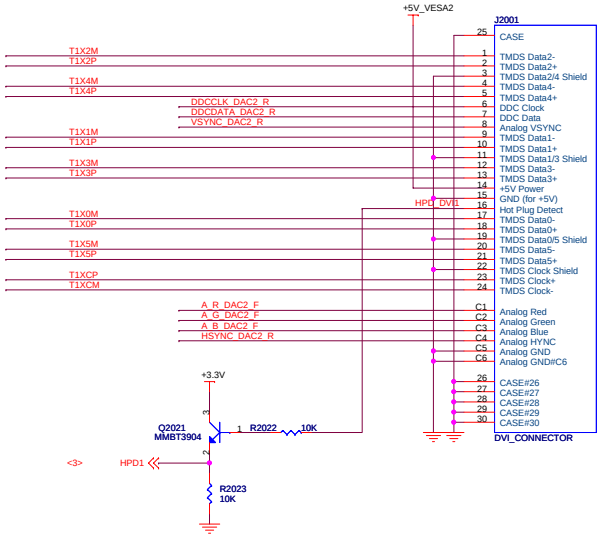
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





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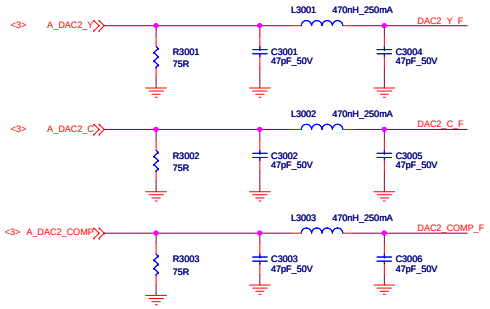

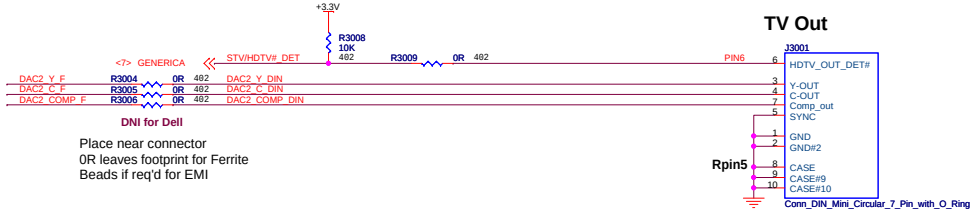

- 4-pin Svideo MiniDIN P/N 6070001000G

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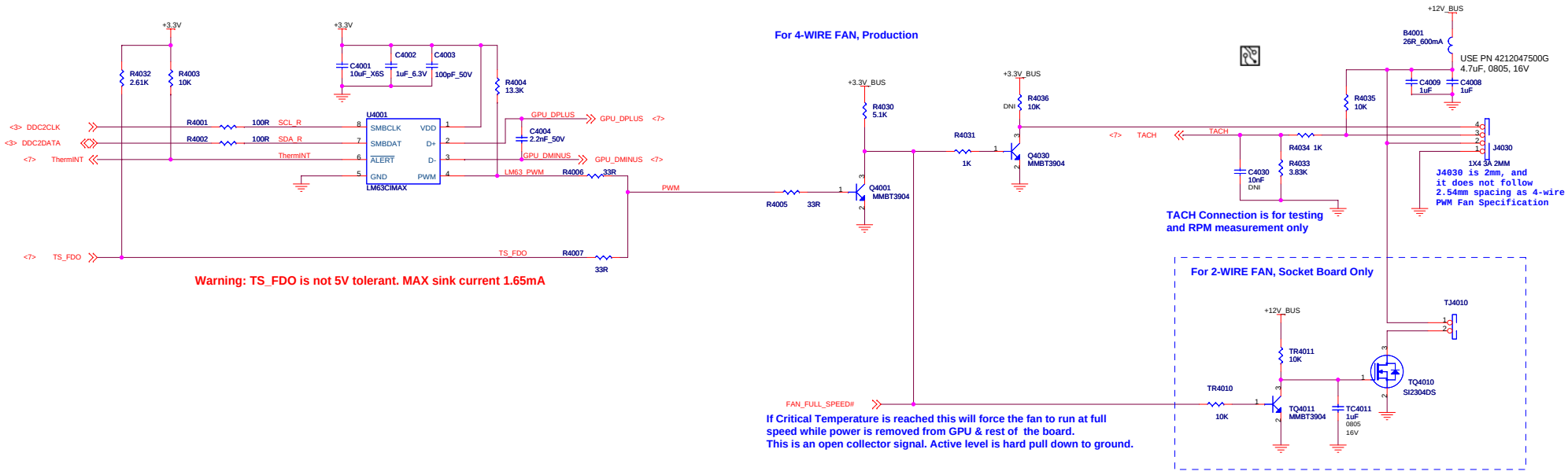

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ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

MT1
MT_Hole_0.136 TM 5.5 BM 7.0

PCB1
PCB
109-B33931-00A

ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET
80200386B0G

ASSY-SCREW5
SCREW
SCREW

BKT1: DS, DVI - DIN - DVI

BKT2
BRACKET
8020038600G

SK1
Socket_RV770

PCIE 12V/3.3V Power up Bonding support

VDDC1

MVDD1

TPC1

IOT1

FM1
SW_FB

FM2
SW_FB

FM3
SW_FB

FM4
SW_FB

FM5
SW_FB

FM6
SW_FB

J7
3 1
4 2
impedence

J4
3 1
4 2
impedence

J5
3 1
4 2
impedence

J8
3 1
4 2
impedence

J3
X_PIN1*2

J6
X_PIN1*2

J9
X_PIN1*2

J11
X_PIN1*2

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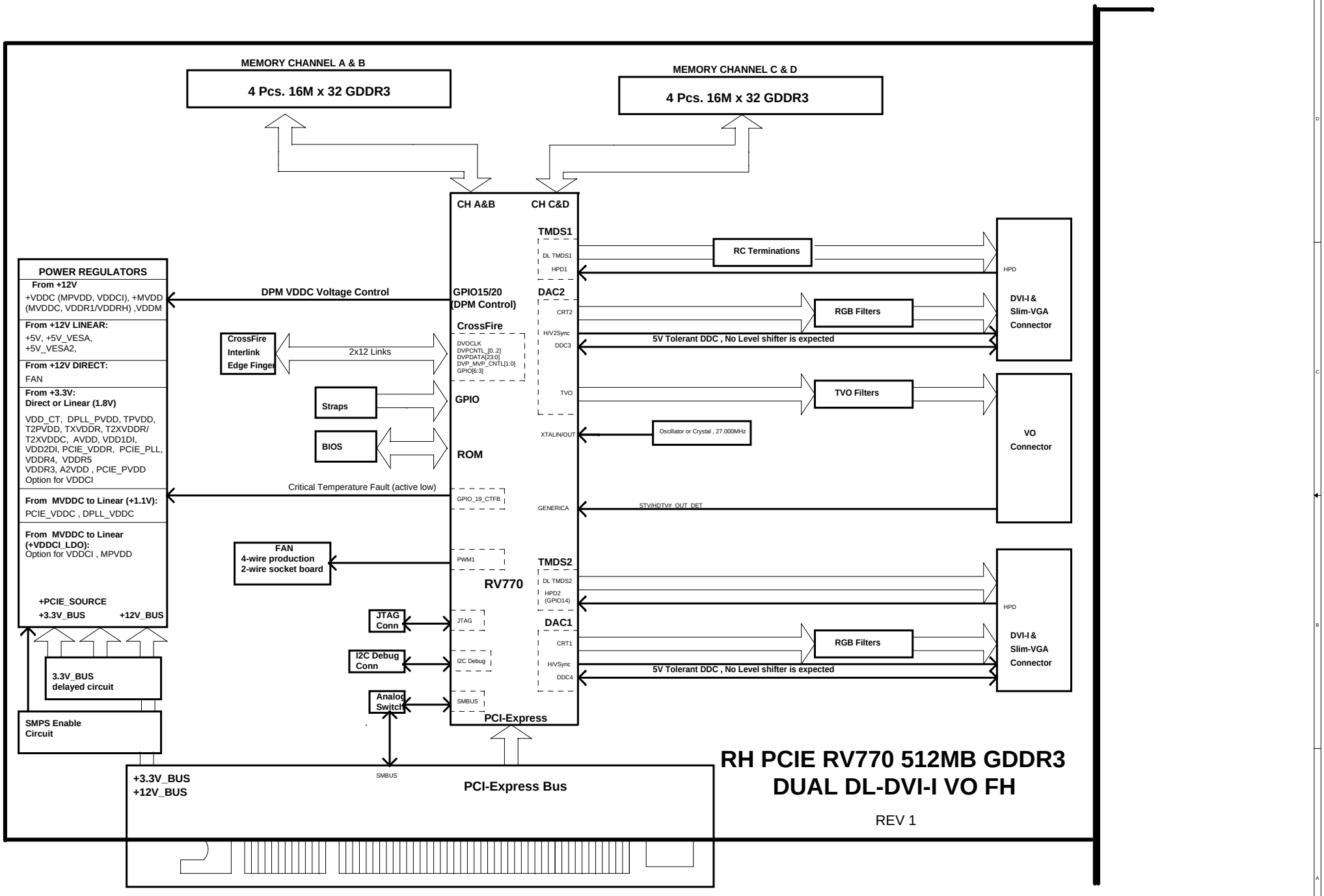
Title	Schematic No.	Date:
RH PCIE RV770 512MB GDDR3 DUAL DL-DVI-I VO FH	105-B501xx-00	Tuesday, May 27, 2008

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/10/11	Initial design for RV770 GDDR3
1	00B	08/02/25	Improvement: 1) Add 1 uF CAP on memory reset, Pg5 2) MVDDC current leakage board workaround; Pg13 3) MVDD Themal Protection, Pg 13 4) Improvement on Hot Plug protection Pg13 5) 12V_BUS & 12V_EXT Input Switch Circuit Page 13
2	00	08/03/27	1.Correct PTC comparator power connection. 2. Add Fuse NF1200 on page 13



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