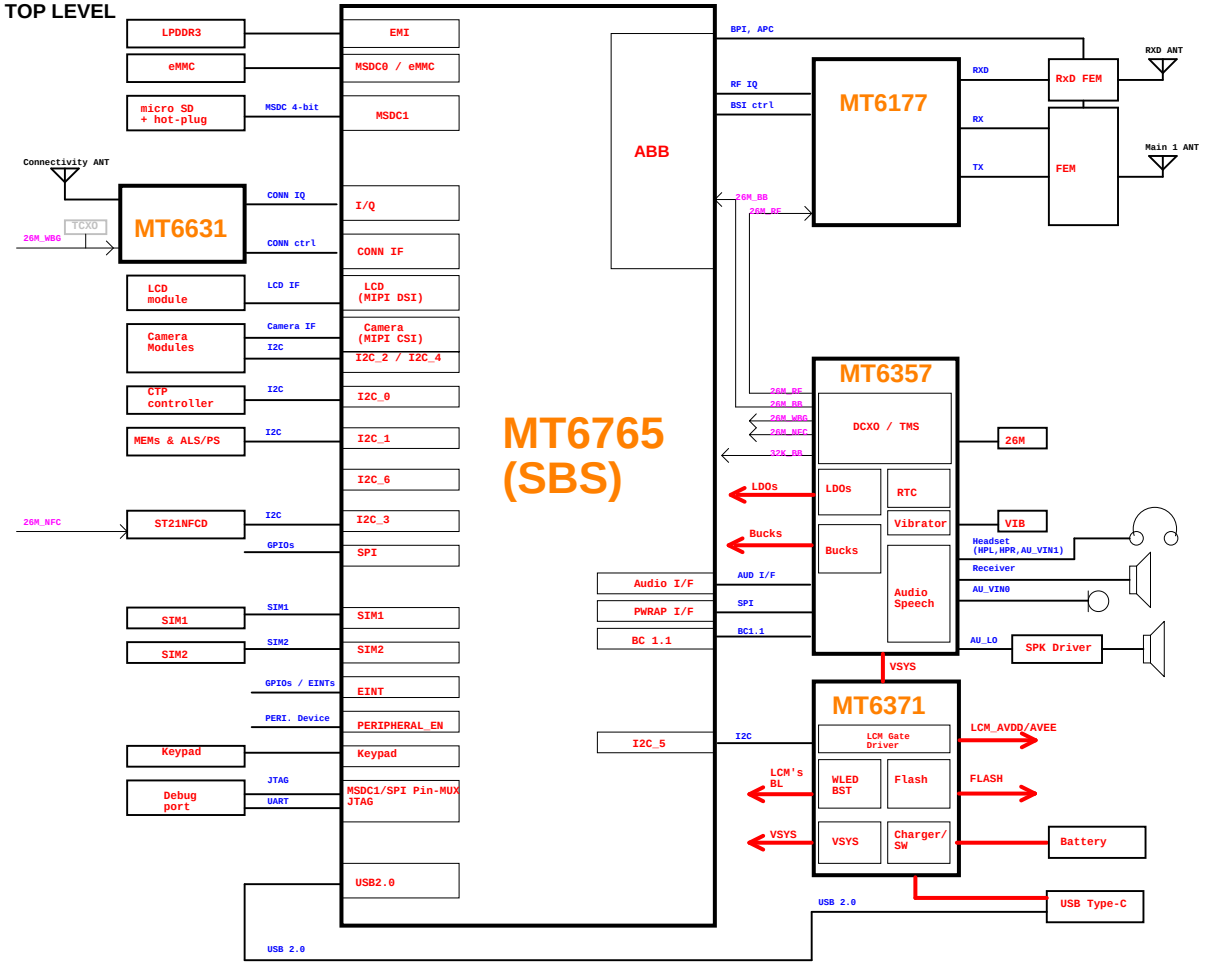
Project : MT6765 LPDDR3
REF_SCH TOP LEVEL



OPPO		
Title	01_Block_Diagram	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 1 of 35	

I2C	Sub SYS	Function	Part Number	I2C Spec.		i2C Slave Address / Write / Read (7-bit mode)	
I2C-0	AP	Cap Touch controller	GT1151	400 Kbps		0x5D	Write:0xBA / Read:0xBB
I2C-1 (I3C)	AP Sensor Hub	Magnetic Sensor	AK09918C	400 Kbps		0x0C	Write:0x18 / Read:0x19
		Ambient Light Sensor Proximity Sensor	CM36558	400 Kbps		0x51	Write:0xA2 / Read:0xA3
		Pressure Sensor	BMP280	400 Kbps		0x77	Write:0xEE / Read:0xEF
I2C-2 (I3C)	AP	Rear Camera	IMX230	400 Kbps		0x1A	Write:0x34 / Read:0x35
			EEPROM	400 Kbps		0x50	Write:0xA0 / Read:0xA1
			AF driver	400 Kbps		0x0C	Write:0x18 / Read:0x19
I2C-3	AP	Audio Smart PA	RT5510	400 Kbps		0x34	Write:0x68 / Read:0x69
		NFC	ST21NFCD	400 Kbps		0x08	Write:0x10 / Read:0x11
I2C-4 (I3C)	AP	Front Camera	S5K2T7	400 Kbps		0x2D	Write:0x5A / Read:0x5B
			EEPROM	400 Kbps		0x52	Write:0xA4 / Read:0xA5
			AF driver=NA				
I2C-5	AP	Sub-PMIC	MT6371 PMU	3.4 Mbps		0x34	Write:0x68 / Read:0x69
			MT6371 PD	3.4 Mbps		0x4E	Write:0x9C / Read:0x9D
I2C-6	AP						

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

OPPO		
Title	02_I2C_ID_Overview	
Size C	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 2 of 35	

OPPO		
Title	03_Change_Notice	
Size C	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 3 of 35	

1，BQ25601电路优化

2，ADD USB 电压侦测电路

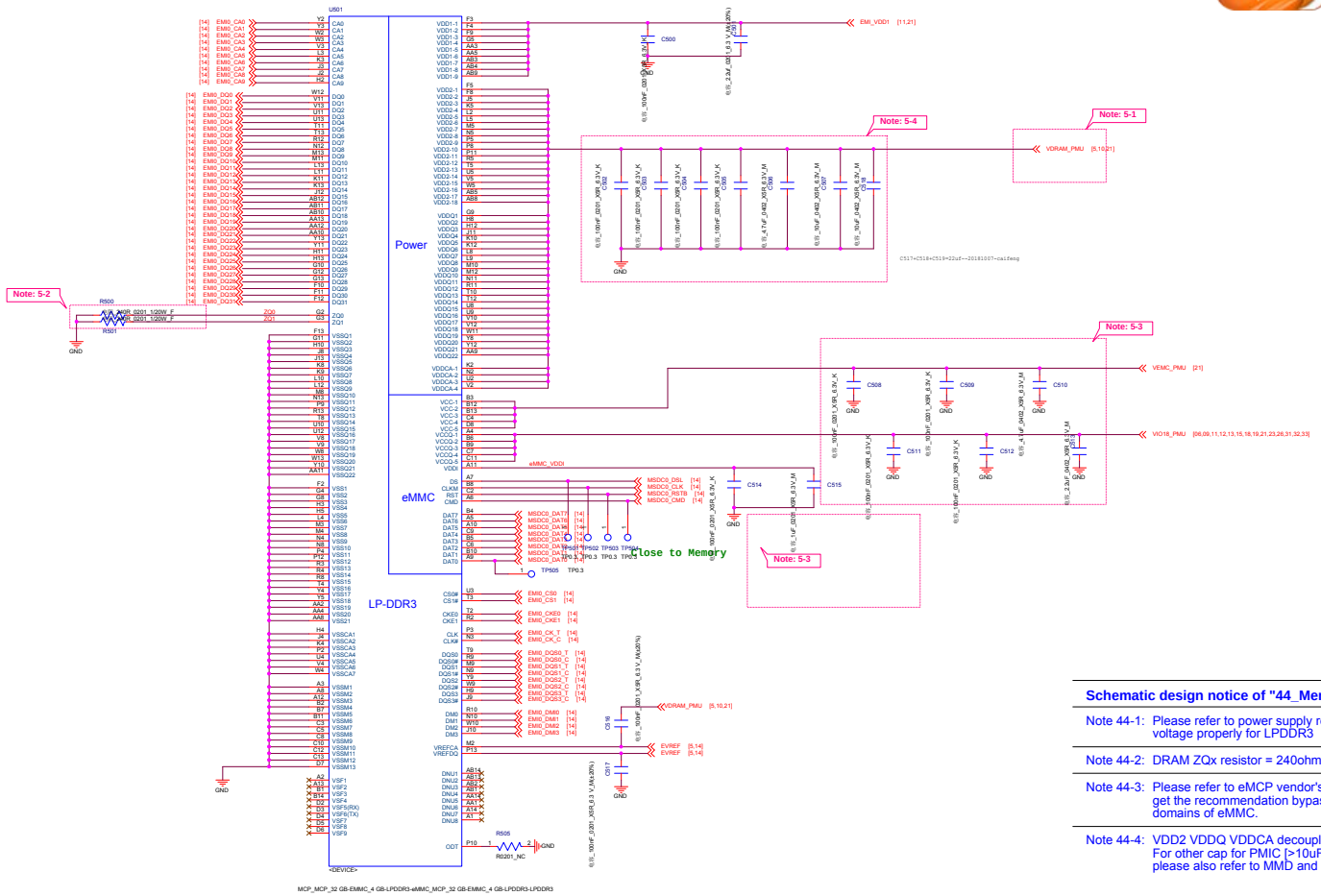
3， WS3218 兼容设计优化 去掉4颗 TVS

4，增加CONFIG0/1测试点 换D2200物料

5，更正 U5101 WIFI/GPS合路器

08.24:
1. J7506更换库为HQ11910421000
2.

OPPO		
Title	04_CHANGELIST	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018		Sheet 04 of 35



Schematic design notice of "44_Memory_eMMC_LPDDR3"

Note 44-1: Please refer to power supply related page select VDRAM1 output voltage properly for LPDDR3

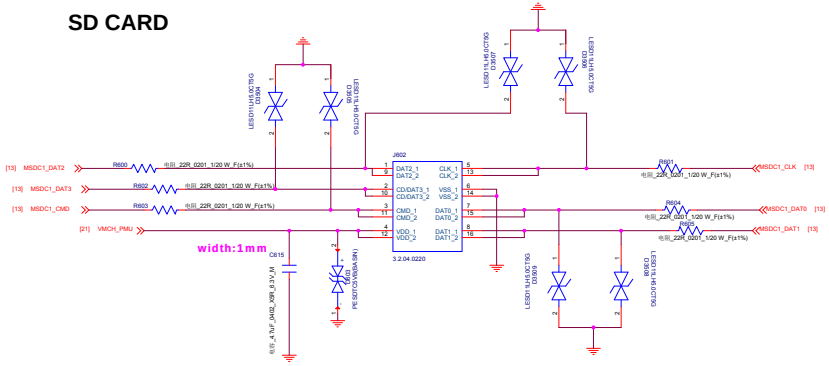
Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to GND

Note 44-3: Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

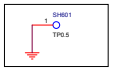
Note 44-4: VDD2 VDDQ VDDCA decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.

OPPO		
Title	5_Memory_eMMC_LPDDR3	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018		Sheet 5 of 35

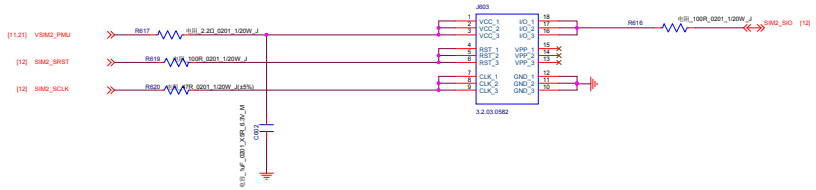
SD CARD



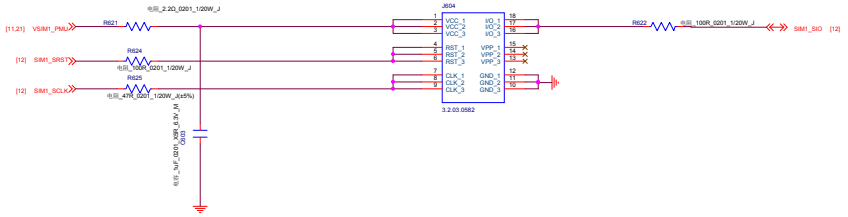
SIM1/SIM2 Card 挡块

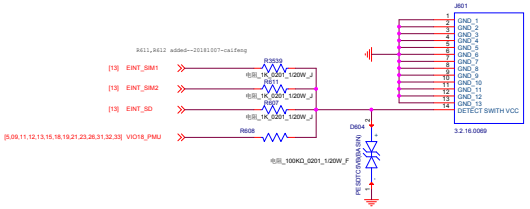


SIM1/SIM2



SIM1/SIM2



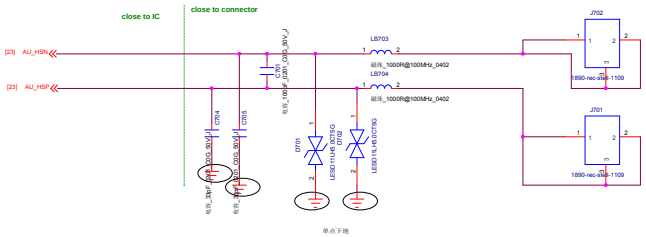


Schematic design notice of "46_MEMORY_SD Card" page.

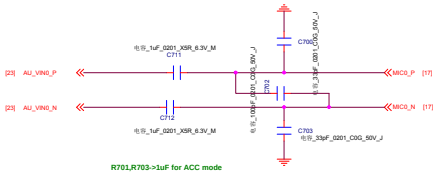
Note 46-1: For better ESD performance, please select suitable components for system protection.

OPPO		
Title	06_Memory_SD_SIM_Card	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018		Sheet 06 of 35

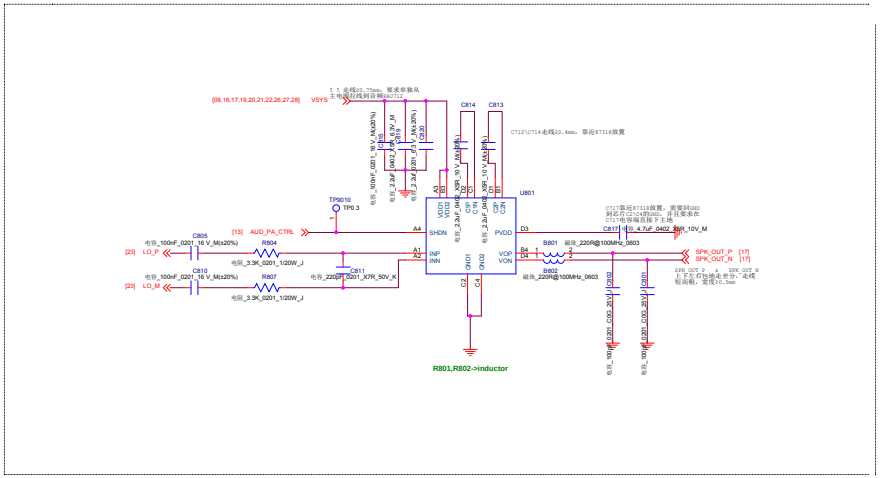
Receiver



Main MIC

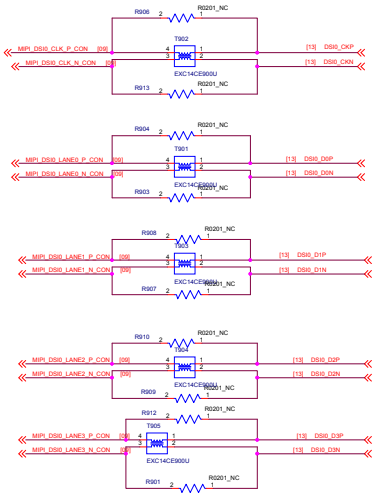


OPPO		
Title	07_AUDIO_REC_MAIN_MIC	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 07 of 35	



OPPO			
Title	08_AUDIO_SPEAKER_AMP		
Size D	Project	A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018		Sheet 08 of 35	

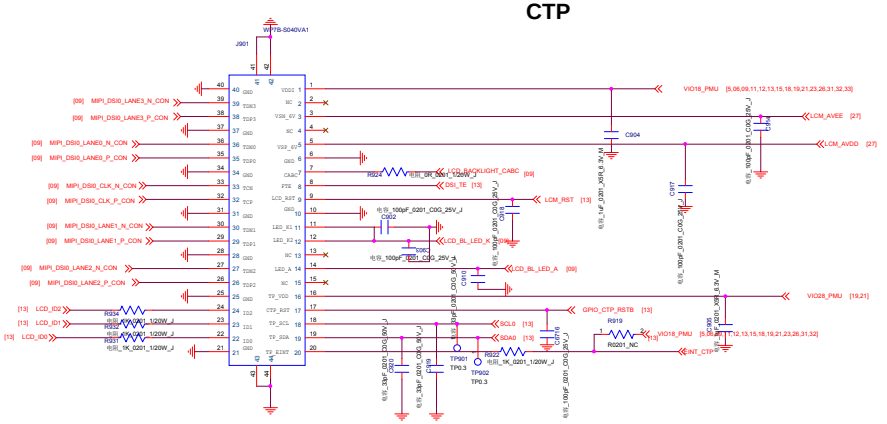
LCD MIPI Common Mode Filter



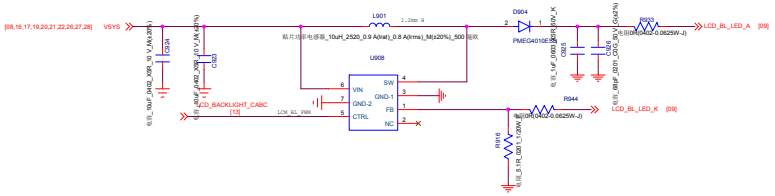
First using 0R ,Second using EMI Filter.

Main LCM+CTP INCELL

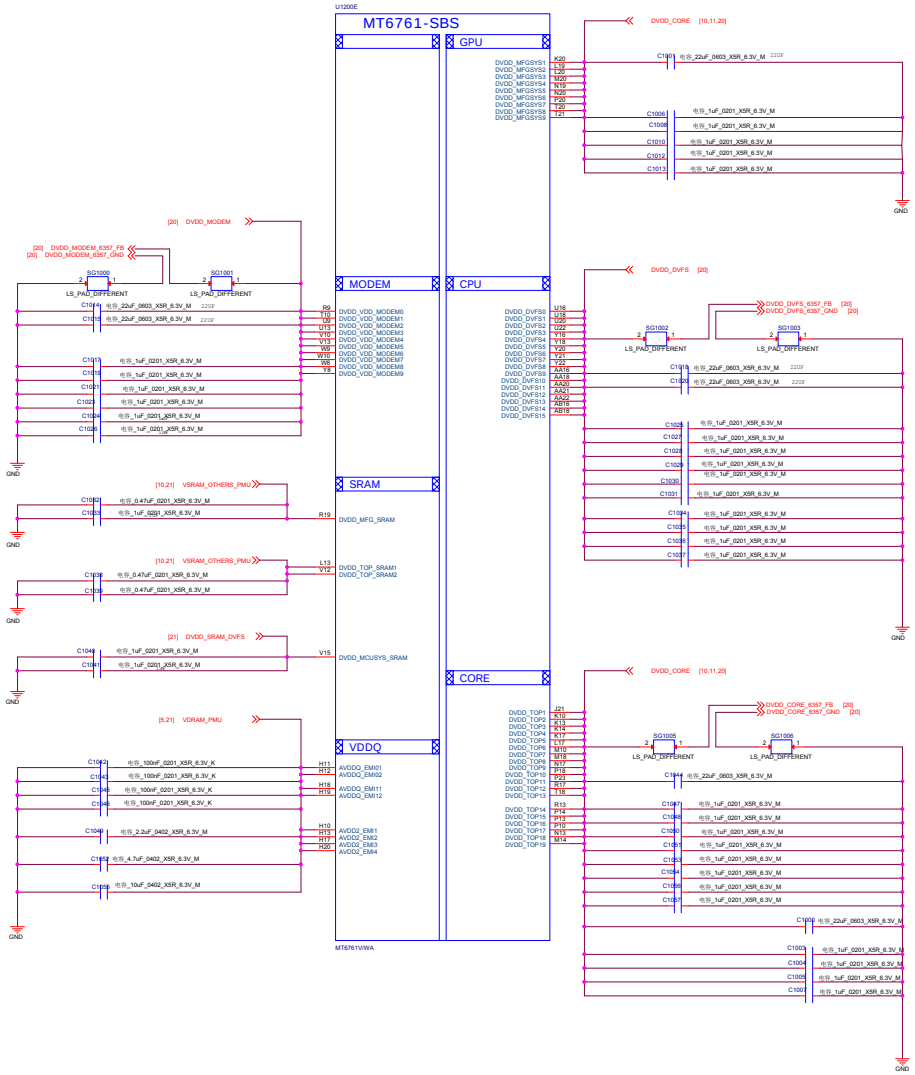
CTP



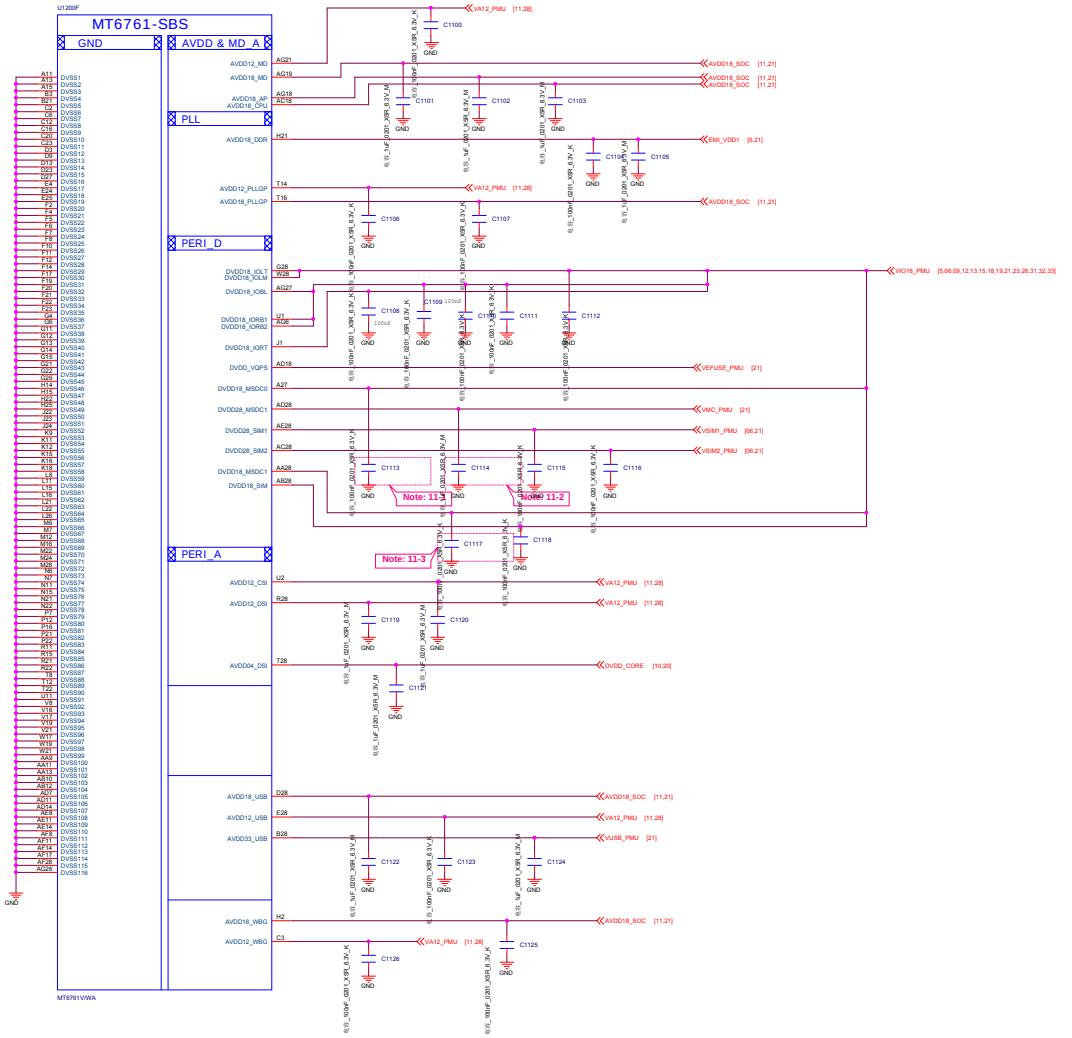
LCD-BACKLIGHT



OPPO			
Title	09_LCD_CTP_BL		
Size D	Project A5S_MB_V1		Rev V1
Date: Friday, December 28, 2018		Sheet 09 of 35	



OPPO		
Title	10_MT6762_BB_POWER_PDN	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 10 of 35	



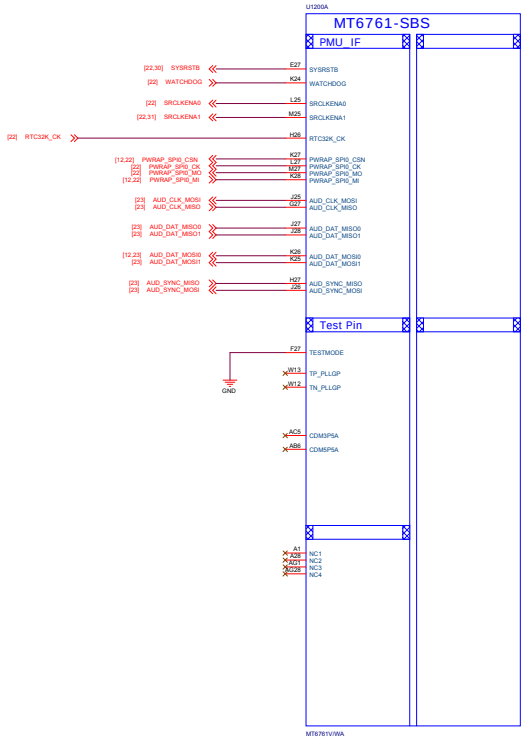
Schematic design notice of "11_BB_POWER_IO" page.

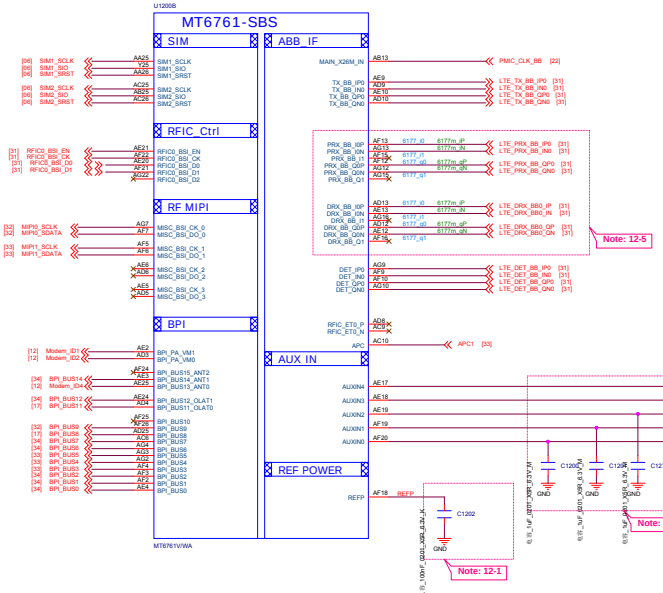
Note 11-1: C4101 closed DVDD18_MSDC0 150mil

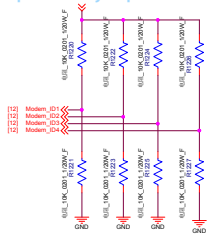
Note 11-2: C4302 closed DVDD28_MSDC1 150mil

Note 11-3: C4301 closed DVDD18_MSDC1 150mil

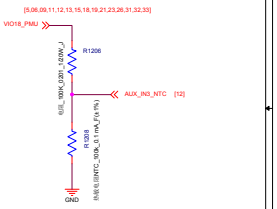
OPPO		
Title	11_MT6762_BB_POWER_IO	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 11 of 34	

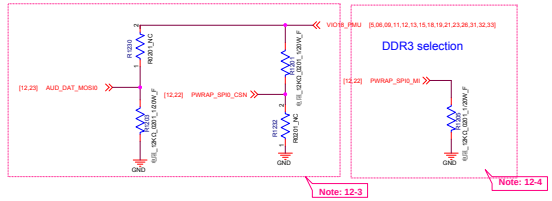






Thermistor to sense Charger IC (U2601) temperature





Schematic design notice of "12_BB_1" page.

Note 12-1: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-3: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pin to select which interface will be the JTAG pin out.

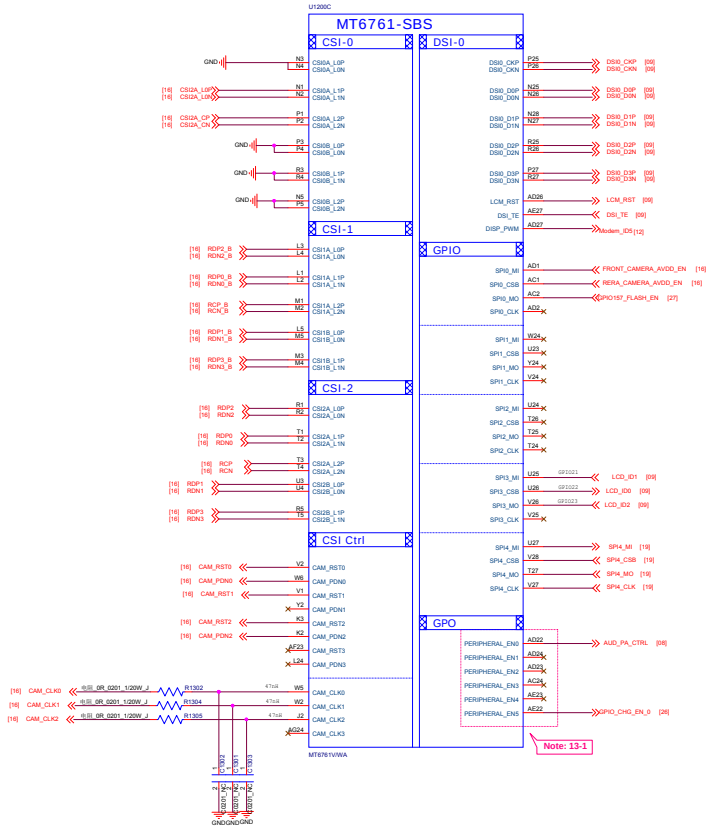
PWRAP_SPI0_CSN	AUD_DAT_MOSI0	JTAG Function	
default=PU	default=PD	AP_JTAG	MD_JTAG
HI	LO	N/A	N/A
HI	HI (by ext. PU)	SPI0+EINT8	SPI1+SPI3
LO (by ext. PD)	LO	SPI0+EINT8	N/A
LO (by ext. PD)	HI (by ext. PU)	MSDC1	N/A

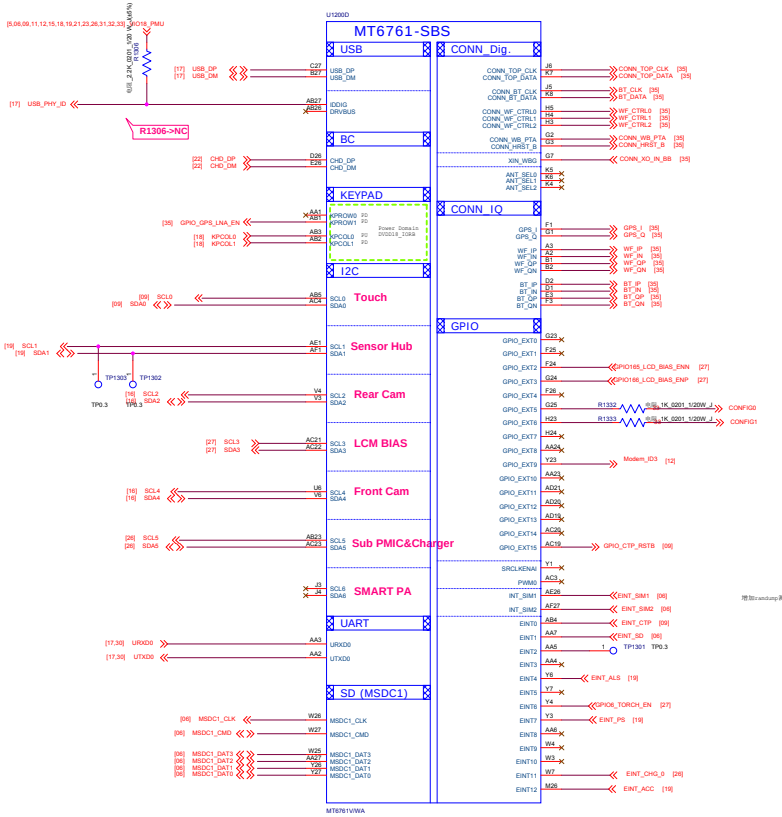
Note 12-4: PWRAP_SPI0_MO and PWRAP_SPI0_MI are DDR type feature in bootstrap

PWRAP_SPI0_MI	Booting interface	
default=PU	DDR	MSDC0 pin mux
LO (by ext. PD)	LPDDR3	follow LP3 Ref SCH.
HI	LPDDR4X	follow LP4X Ref SCH.

Note 12-5: Please set unused IO pins in NC

OPPO		
Title	12_MT6762_BB_1	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 12 of 35	

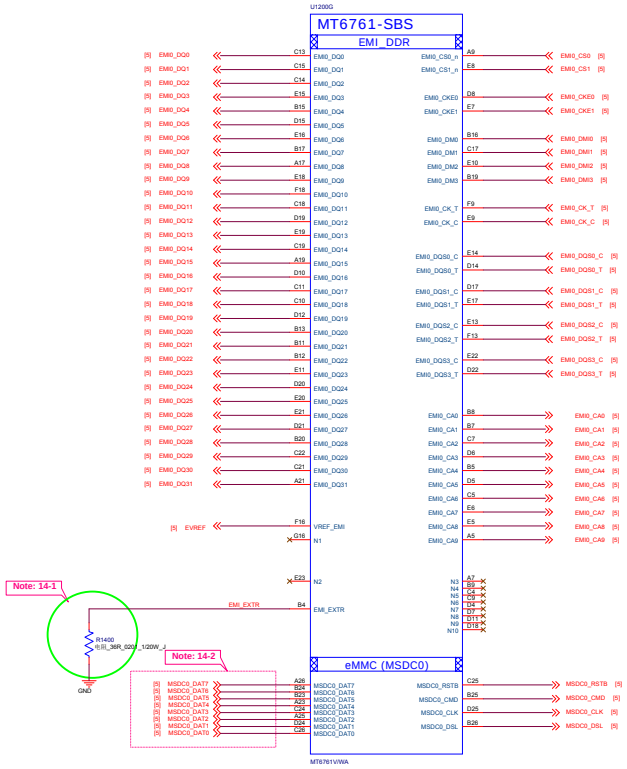




Schematic design notice of "13_BB_2" page.

Note 13-1: The enable pin of acoustic or optoelectronic devices (e.g. SPK AMP/Backlight/Charger OCP/OVP) suggest to use Peripheral_EN[0:5]
If use other GPIOs as enable pin, suggest to reserve 0201 NC to GND

OPPO		
Title	13_MT6762_BB_2	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018		Sheet 13 of 35

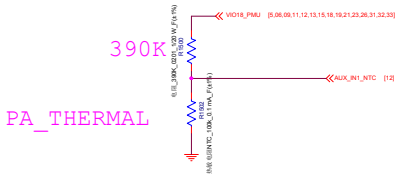


Schematic design notice of "14_BB_3" page.

Note 14-1: R4001 please select 34.8 ohm (1%) resistor

Note 14-2: Please check eMCP LP3 and eMCP LP4X pin mux

OPPO		
Title	14_MT6762_BB_3	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018		Sheet 14 of 35

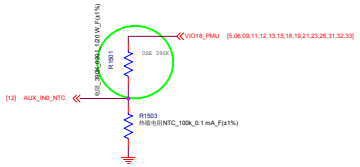


change to NCP03WF104F05RL Murata

Thermistor to sense RF PA temperature

1. NTC1502 must close to LTE Band 7 PA or the hottest PA <2mm.
2. The distance is the shortest distance from package edge to edge.

Thermistor / To sense board level temperature



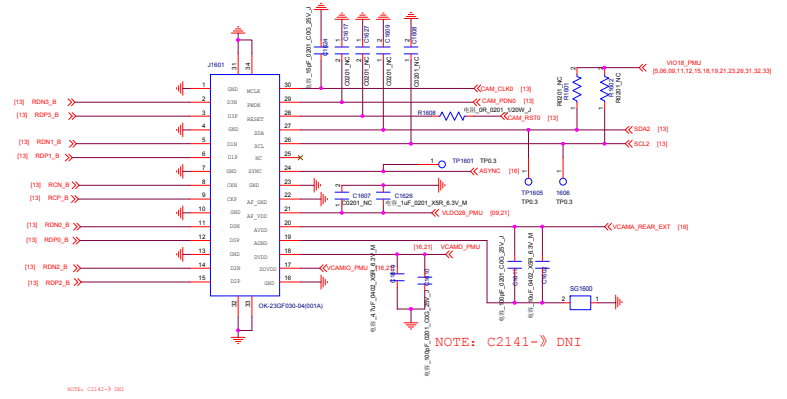
Distance to AP is 5~7mm and away form other heat resource 10mm~12mm

OPPO			
Title	15_BB_AUXADC_Thermal		
Size D	Project A5S_MB_V1		Rev V1
Date:	Friday, December 28, 2018	Sheet 15 of 35	

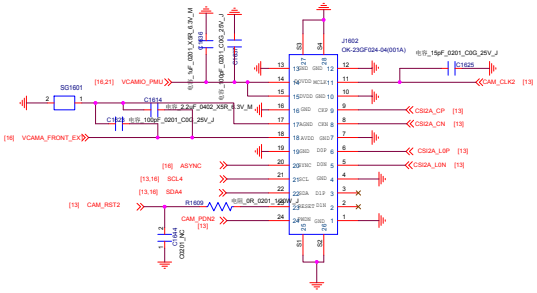
Dual cam

Rear Camera

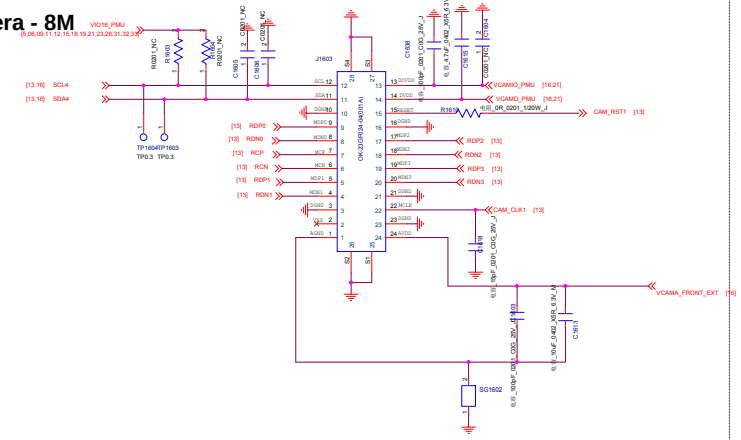
注意：AGND AFGND都要单独下主地

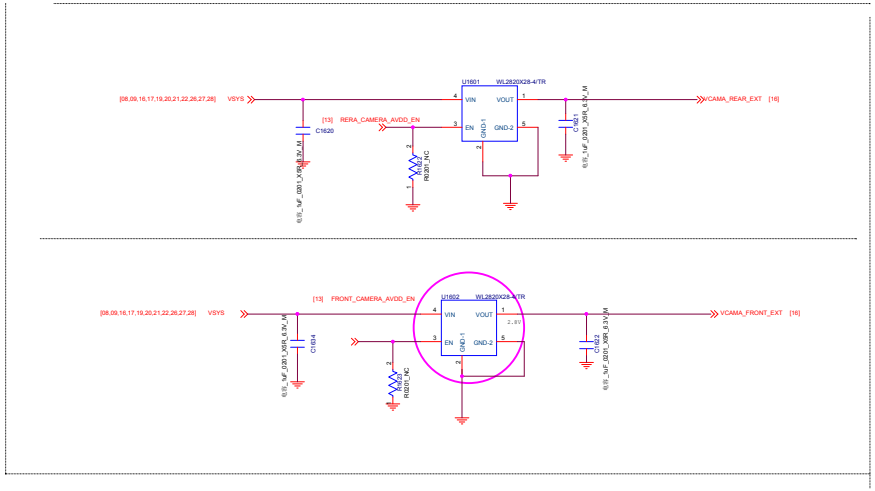


Rear Camera 2



Front Camera - 8M





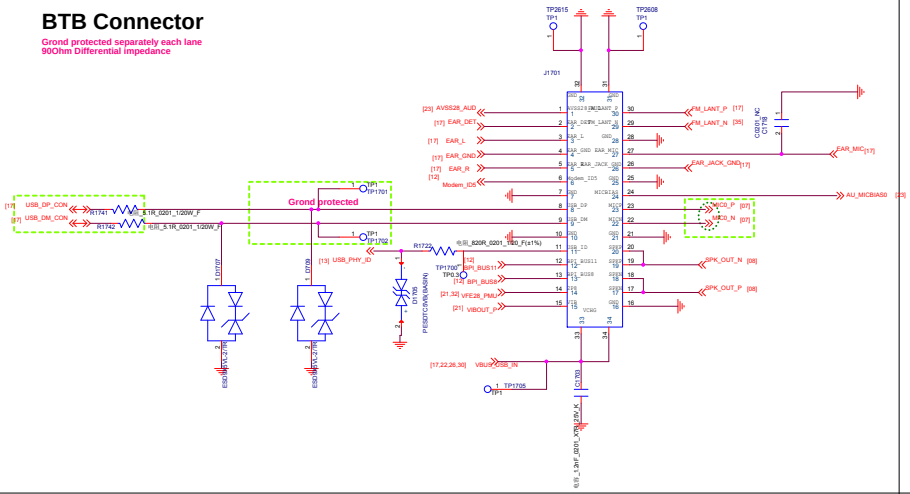
OPPO		
Title	16_CAMERA_INTERFACE	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 16 of 35	

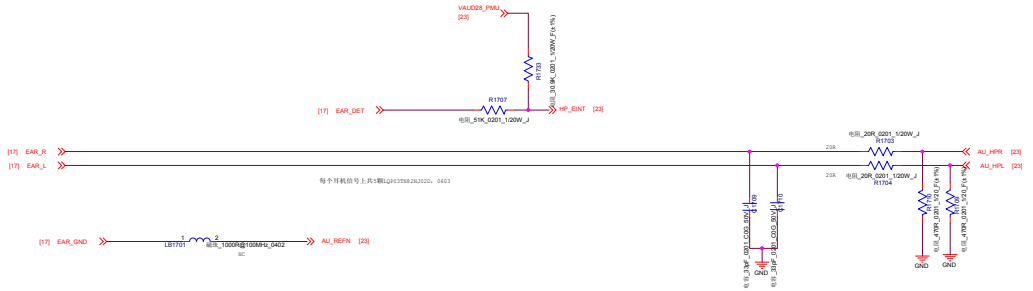
Schematic design notice of "71_PERI_USB 2.0" page.

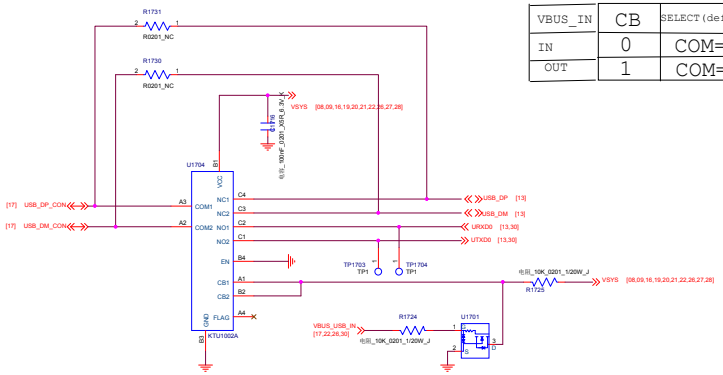
Note 71-1: For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

BTB Connector

Grond protected separately each lane
90Ohm Differential impedance

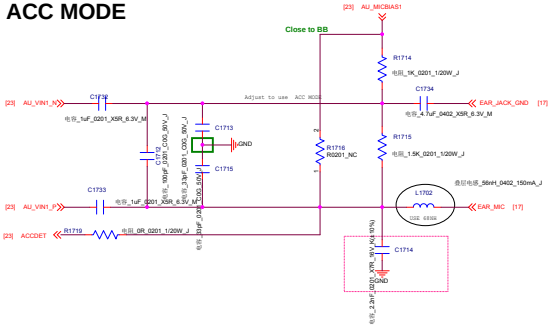






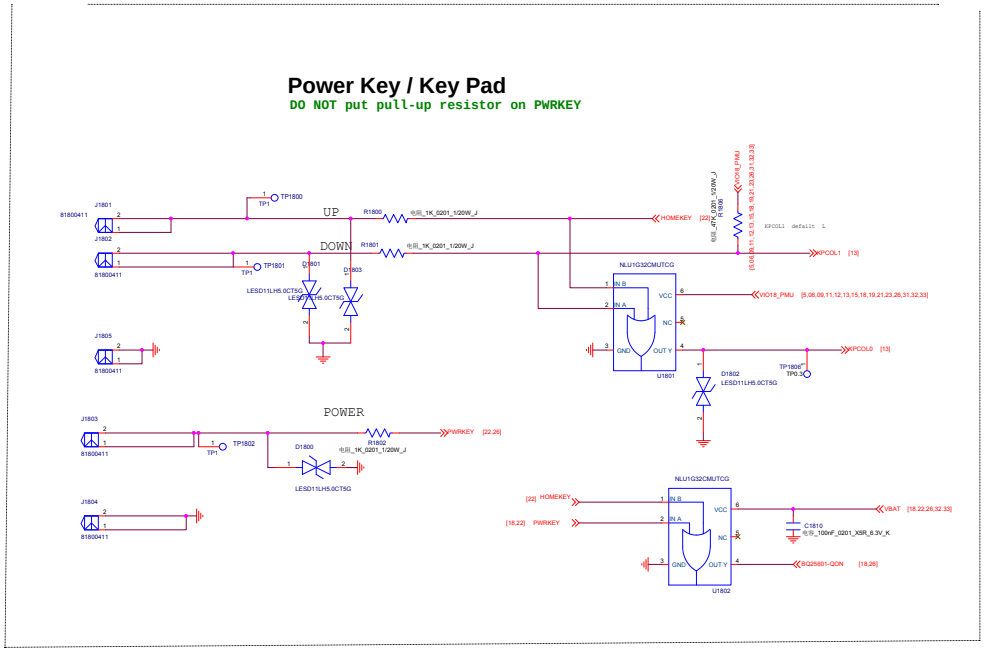
VBUS_IN	CB	SELECT(default PD)
IN	0	COM=NC
OUT	1	COM=NO

Earphone MICPHONE
ACC MODE



Platform	MT6357	
Mode	ACC mode	DCC mode
EINT	HP_EINT	HP_EINT
Key-Detection	ACCDET	AU_VIN1_P
R7112	1uF	0 ohm
R7113	1uF	0 ohm
R7114	1K	NC
R7115	1.5K	NC
R7116	NC	2.49K
R7118	4.7uF	0 ohm
R7119	0 ohm	NC
R7107	47K ohm	47K ohm

OPPO		
Title	17_B2B_OVP_AUDIO_JACK	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 17 of 35	

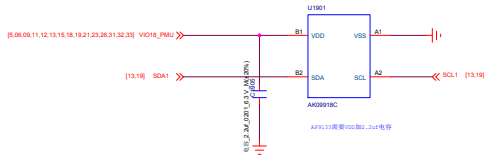


Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.
Note 75-1: DO NOT put pull-up resistor on PWRKEY
Note 75-2: Volume Up : HOME Key / GND Volume Down : KPROW0/KPCOL0
Note 75-3: For better ESD performance, please select suitable components for system protection.

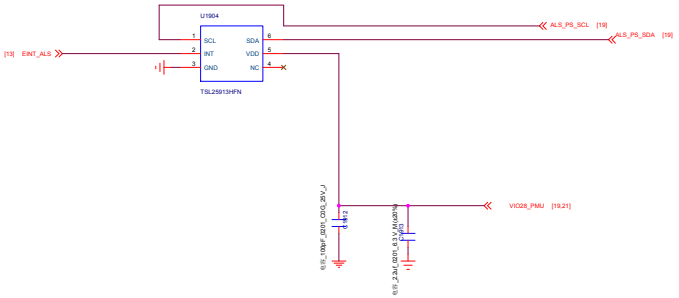
OPPO		
Title	18_KEYPAD_INTERFACE	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 18 of 35	

M-Sensor

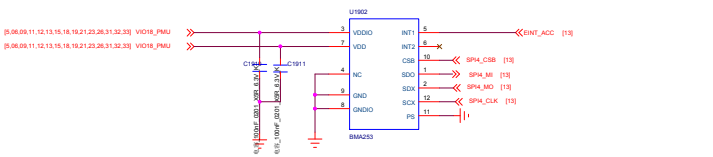
AK09918 / M-Sensor I2C Address : 0x0C (Write:0x18, Read:0x19)



ALS SENSOR

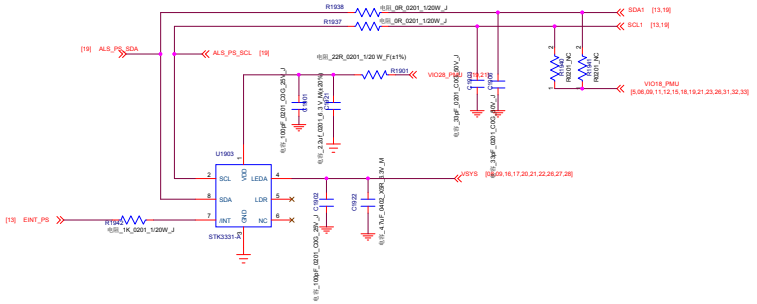


G Sensor

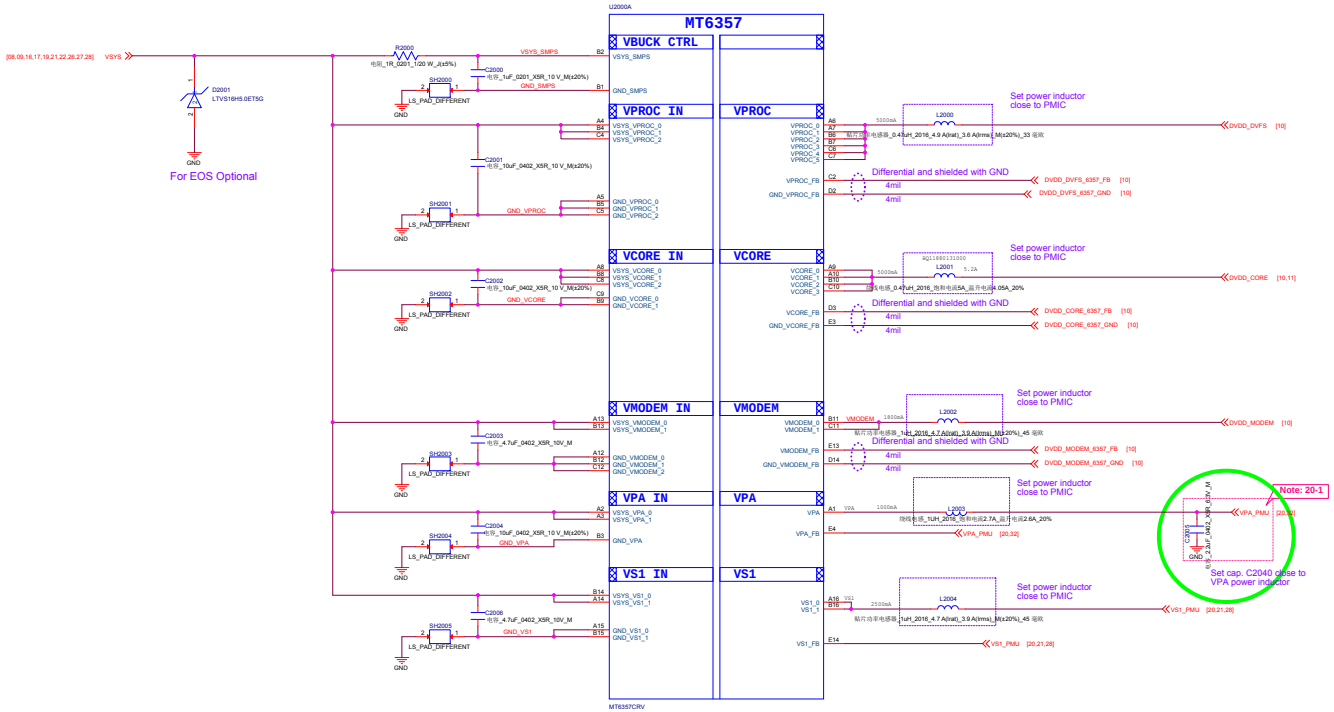


PS Or ALS&PS SENSOR

VDD 1.7~3.0V VLEDA 2.8~4.6V STK3332 4X1.5X1mm



OPPO			
Title	19_SENSORS_ALS_PS_M_A		
Size D	Project A5S_MB_V1		Rev V1
Date: Friday, December 28, 2018		Sheet 19 of 35	

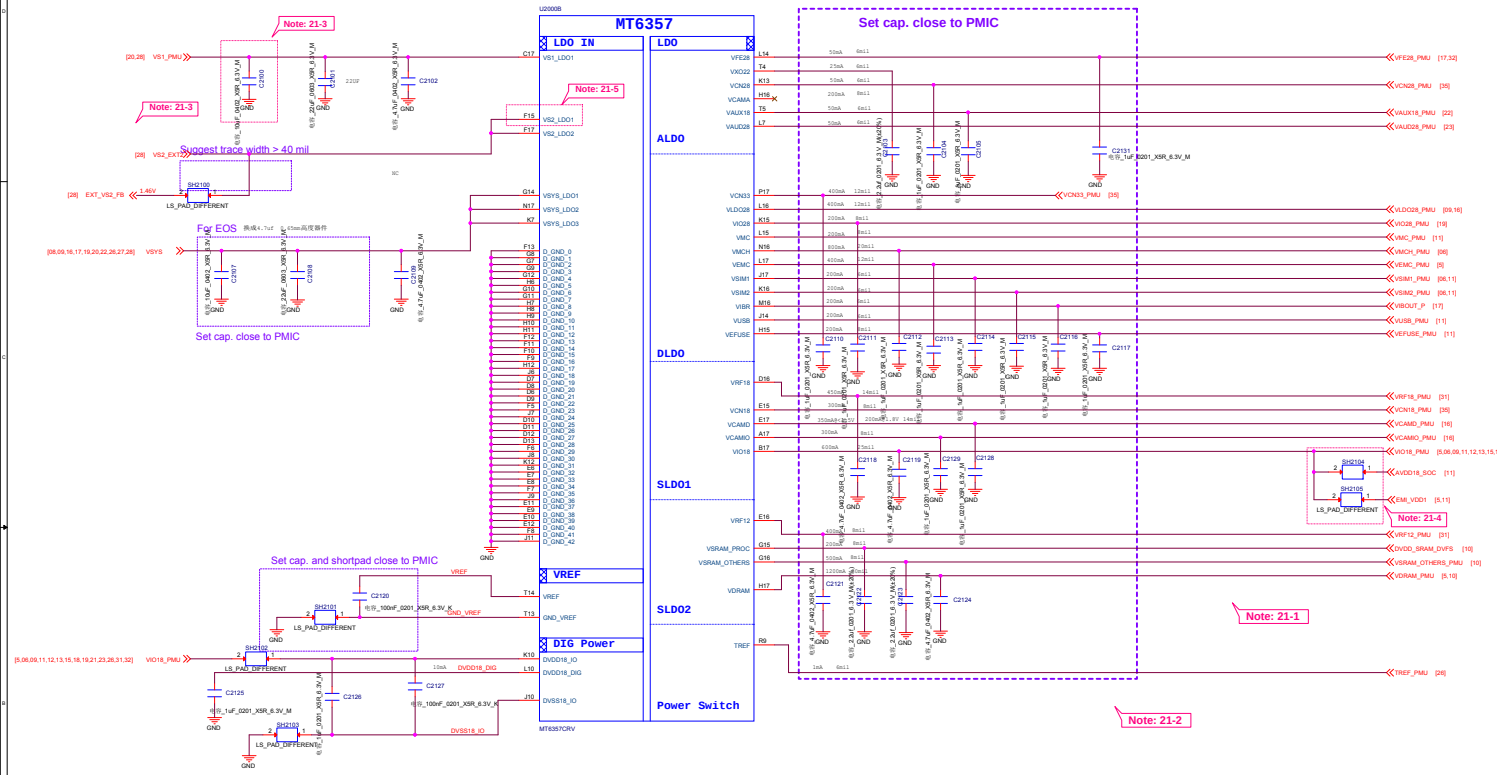


Schematic design notice of "20_POWER_MT6357_Buck"

Note 20-1: C2040, please choose 0603 size

OPPO		
Title	20_POWER_MT6357_Buck	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 20 of 35	

1. "Typical Cap" defined in design notice is the minimum cap. to LDO Cout.
2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2 ohm)
=> value and placement of Cap, please refer design notice



MT6356 LDO output

Input Power	Power Name	Output Voltage (V)	Output Current	Default Voltage
LDO from VBAT	VFE28	2.8	40mA	2.8V
	VXO22	2.24	25mA	2.24V
	VCN28	2.8	40mA	2.8V
	VCAMA	1.8/2.5/2.8	200mA	2.8V
	VAUX18	1.8	20mA	1.8V
	VAUD28	2.8	50mA	2.8V
	VBIF28	2.8	1mA	2.8V
	VCN33	3.3/3.4/3.5/3.6	800mA	3.3V
	VLDO28	2.8/3.0	360mA	2.8V
	VIO28	2.8	200mA	2.8V
	VMC	1.86/2.9/3.0/3.3	200mA	3.0V
	VMCH	2.9/3.0/3.3	800mA	3.0V
	VEMC	2.9/3.0/3.3	800mA	3.3V
	VSIM1	1.7/1.8/1.86/2.76/3.0/3.1	200mA	1.86V
	VSIM2	1.7/1.8/1.86/2.76/3.0/3.1	200mA	1.86V
	VIBR	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	200mA	2.8V
	VUSB	3.07	50mA	3.07V
LDO from VS1	VRF18	1.81	450mA	1.81V
	VMIPI	1.71/1.8/1.84	300mA	1.84V
	VCN18	1.8	200mA	1.8V
	VCAMD	1/1.05/1.1/1.2/1.3/1.5/1.8	600mA	1.2V
	VCAMIO	1.8	300mA	1.8V
	VIO18	1.8	1200mA	1.8V
LDO from VS2	VRF12	1.2	200mA	1.2V
	VA12	1.2	300mA	1.2V
	VSRAM_PROC	0.6-1.31	400mA	1.1V
	VSRAM_OTHERS	0.6-1.31	200mA	0.9V
	VSRAM_GPU	0.6-1.31	400mA	1.0V
	VDRAM	1.12/1.24	1000mA	1.24v

Schematic design notice of "21_POWER_MT6357_LDO"

Note 21-1: If these power trace can meet LDO layout constraint, these CAP can be NC or removed. Please refer to MT6357 design notice.

Note 21-2: Output cap range please follow MT6357CRV LDO design notice

Note 21-3: Ext Buck BOM option

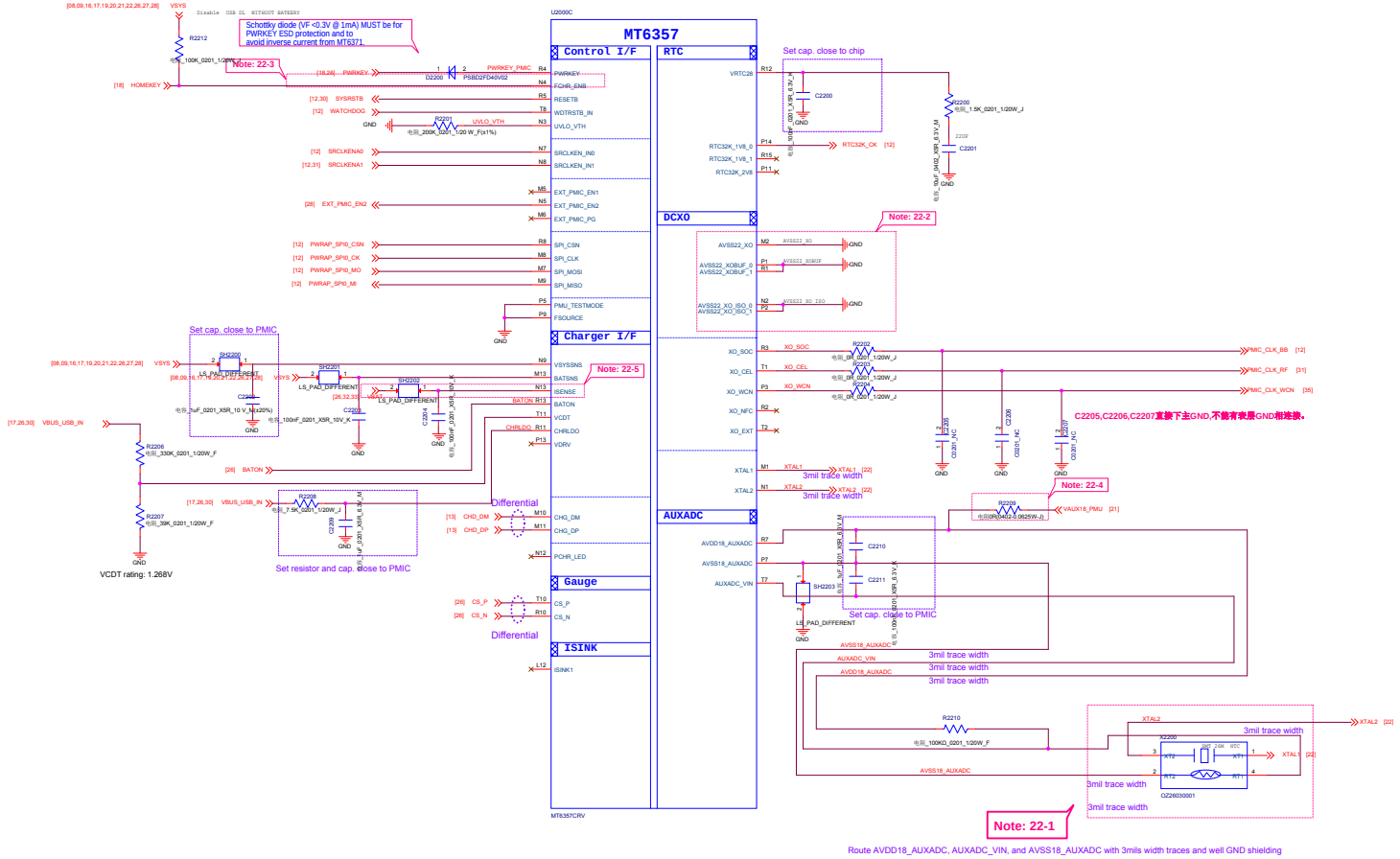
	Ext. buck option	
	w/ EXT VS2 Buck	w/o EXT VS2 Buck
C2104	10uF	22uF
R2851	0-ohm , 0603	NC
R2852	NC	0-ohm , 0603

Note 21-4: Please set SH2101 and SH2102 close to C2141, making star connection among VIO18_PMU, AVDD18_SOC, and EMI_VDD1 near to LDO cap. C2141

Please also refer to MT6357 design notice for further detail design information

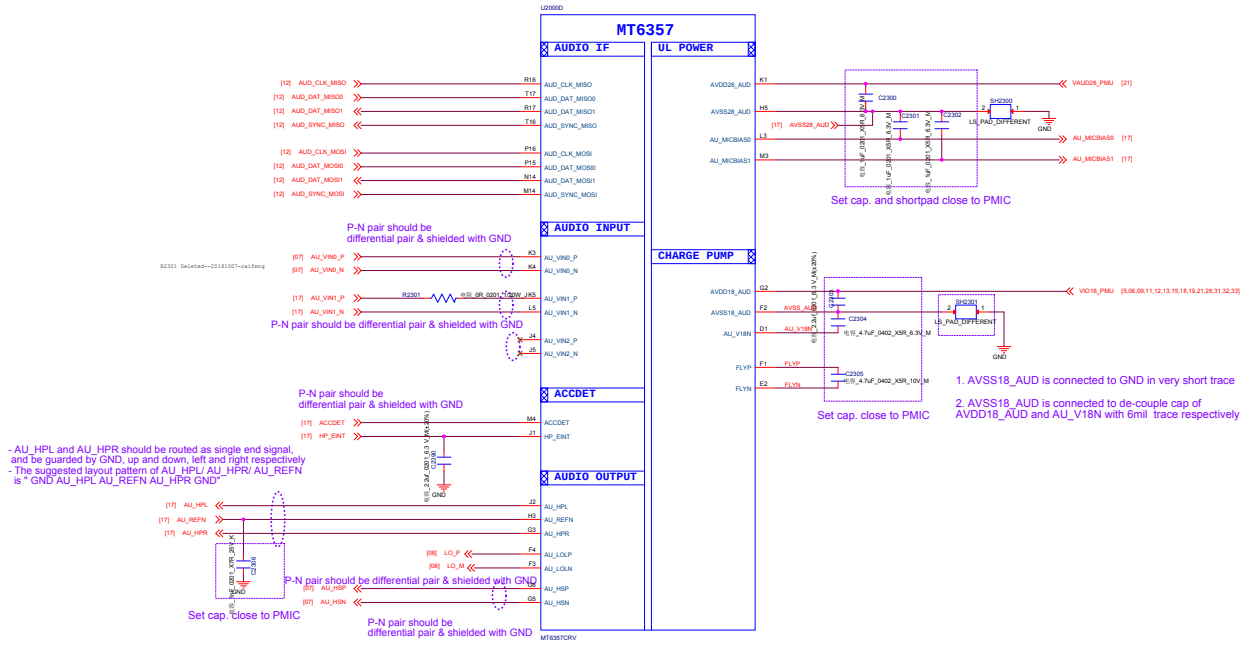
Note 21-5: Please connect VS2_LDO1(F15) to VS1_PMU if voltage applied to VCAMD(E17) >= 1.3 V

OPPO			
Title	21_POWER_MT6357_LDO		
Size D	Project A5S_MB_V1		Rev V1
Date: Friday, December 28, 2018		Sheet 21 of 35	



Schematic design notice of "22_POWER_MT6357-IF"			
Note 22-1:	Please implement 2520 & 2016 Size TMS PCB co-layout. Please refer to MT6765_MT6357 Co-Clock Design Notice for co-layout guide		
Note 22-2:	1. Please Connect P1 and R1 ball first and then to GND 2. Please Connect P2 and N2 ball first and then to GND 3. Please connect DCXO GND to main GND by independent L1-2 GND via.; DO NOT connect it through L1 GND		
Note 22-3:	Let floating if disable HOMEKEY function		
Note 22-4:	Please follow MT6765_MT6357 Co-Clock Design Notice for Layout guide of VAUX18, then R8101 can use 0 ohm to replace BEAD.	Note 22-5:	Please connect to battery connector

OPPO			
Title	22_POWER_MT6357_IF		
Size D	Project A5S_MB_V1		Rev V1
Date: Friday, December 28, 2018		Sheet 22 of 35	

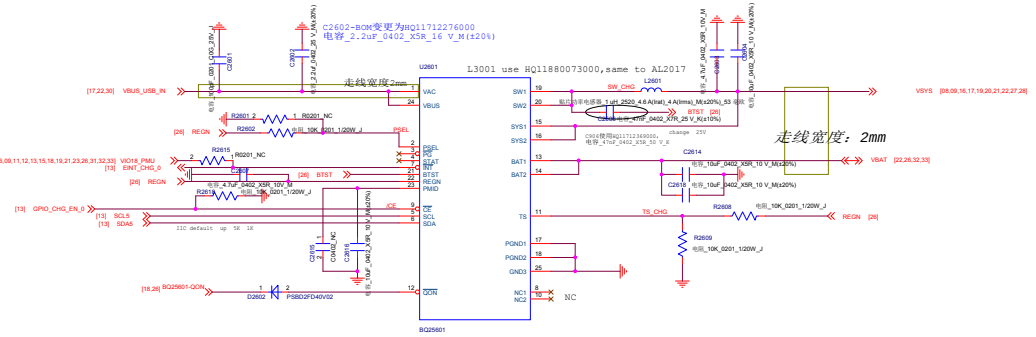


OPPO		
Title	23_POWER_MT6357_Audio	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 23 of 35	

Title	24_ Reserved
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Friday, December 28, 2018
Sheet	24 of 35

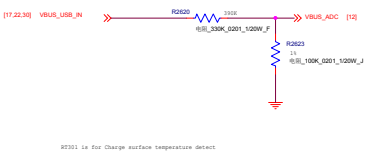
Title	25_ Reserved
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Friday, December 28, 2018
Sheet	25 of 35

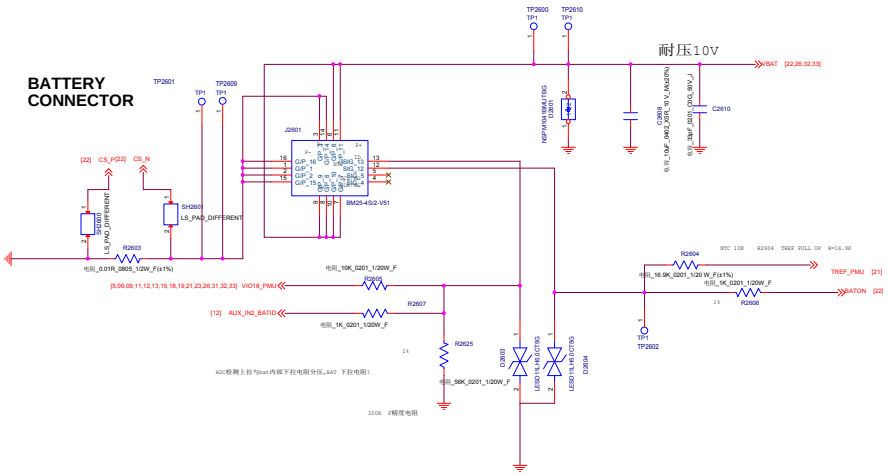
BQ25601 Charger



BQ25601 I2C address:0x6BH

Note1:PSEL pin,Power source selection input. Set 500 mA input current limit by pulling this pin high and set 2.4A input current limit by pulling this pin low.
Once the device gets into host mode, the host can program different input current limits to IINDPM register



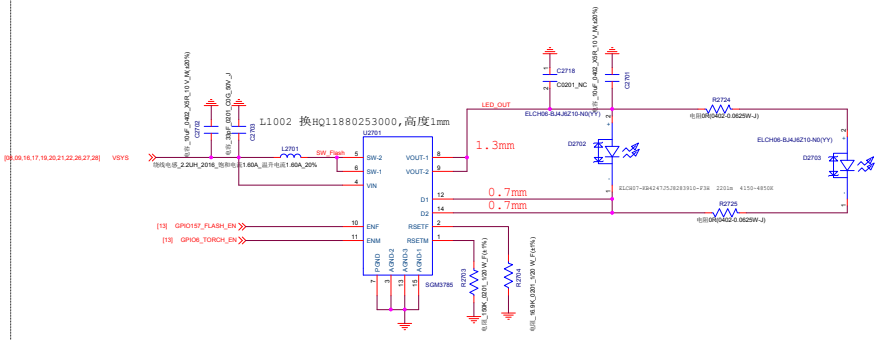


Schematic design notice of "26_POWER_SubPMIC-Charger + PP" page.

Note 26-1: For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

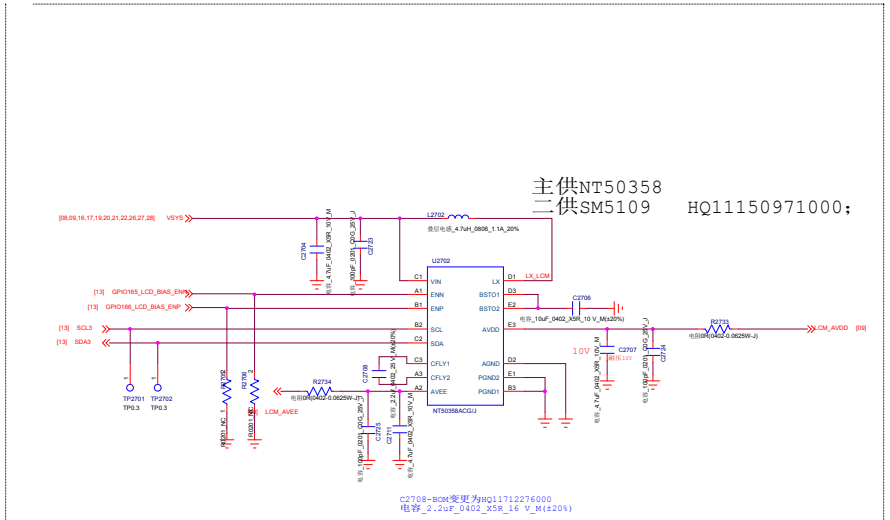
OPPO		
Title	26_Charger_IC_BQ25601+BATTERY	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 26 of 35	

Rear Camera Flash



Iflash=8556/16.9*2=1012mA;R2704->16.9K

Imovie=7063/150*2=94mA;R2703->150k HQ11600244000



Schematic design notice of "27_POWER_SubPMIC-HV powers" page:

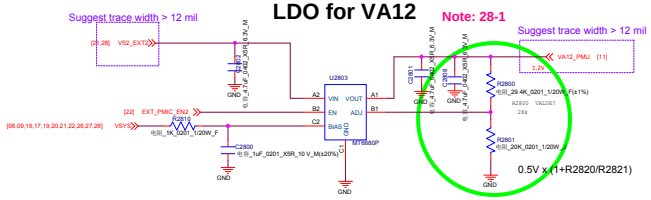
Note 27-1: To minimize RF de-sense, it is recommended to reserve 0-ohm and 0402 cap for BOM fine tuning.

Note 27-2: To minimize RF de-sense, it is recommended to reserve 0-ohm and 0201 cap. for BOM fine tuning.

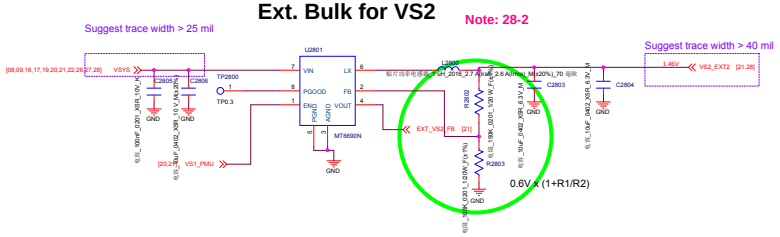
Note 27-3: C2705 could be replaced with C / 1 / uF / 50V + C / 1 / uF / 50V

OPPO		
Title	27_LCD+-5V_TORCH_DRIVER_IC	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 27 of 35	

LDO for VA12



Ext. Bulk for VS2

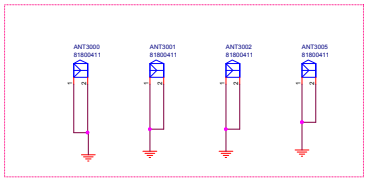


Schematic design notice of "28_POWER_ThirdParty-Power"	
Note 28-1:	VA12 Layout placement please close to AP
Note 28-2:	VS2 Buck Layout placement please close to PMIC MT6357
Note 28-3:	VCN33 LDO Layout placement please close to MT6631

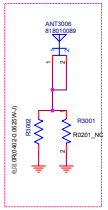
OPPO		
Title	28_POWER_ThirdParty_Powers	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 28 of 35	

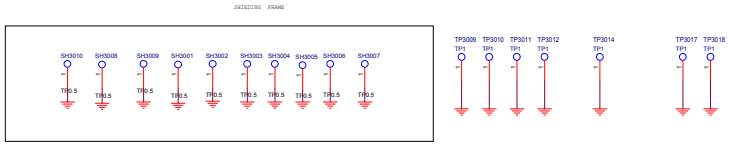
Title	29_ Reserved
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Friday, December 28, 2018
Sheet	29 of 35

RF_PCB TO A-COVER

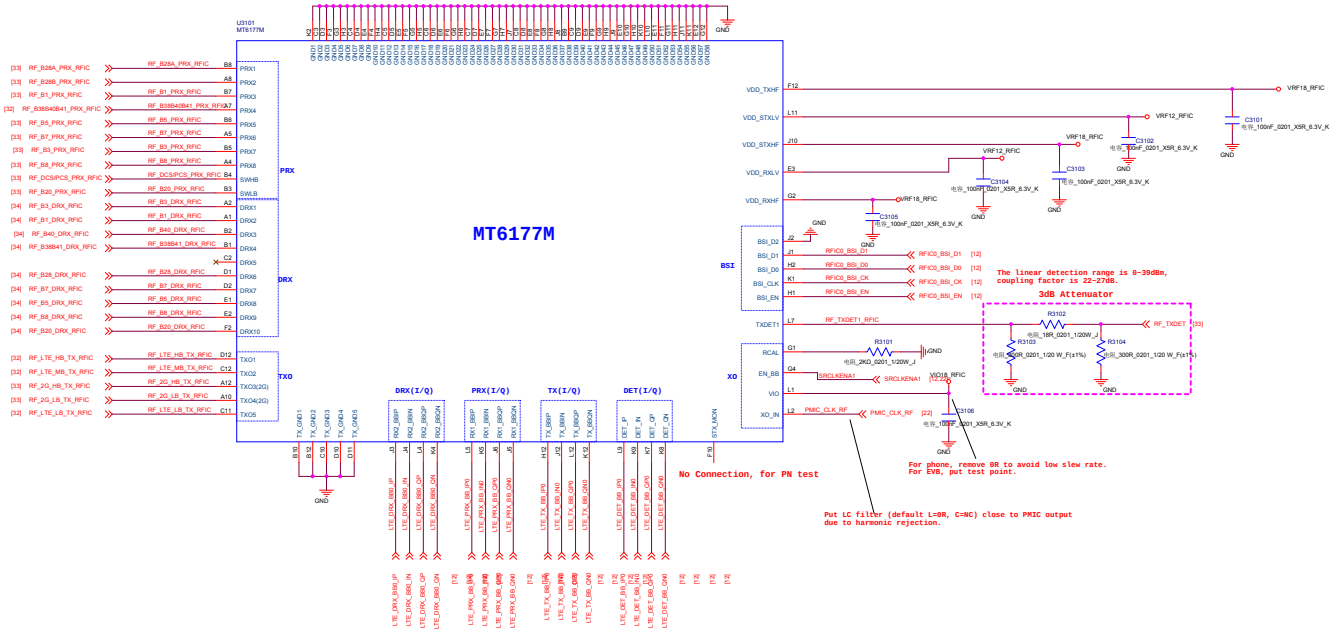


Rear Camera TO GND

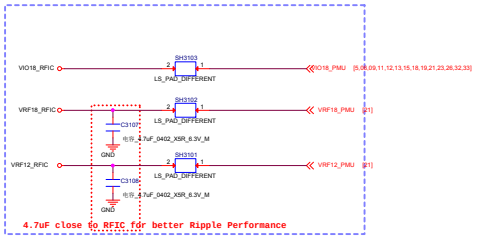




OPPO			
Title	30_DEBUG_IO		
Size D	Project	A5S_MB_V1	Rev V1
Date:	Friday, December 28, 2018	Sheet 30 of 35	



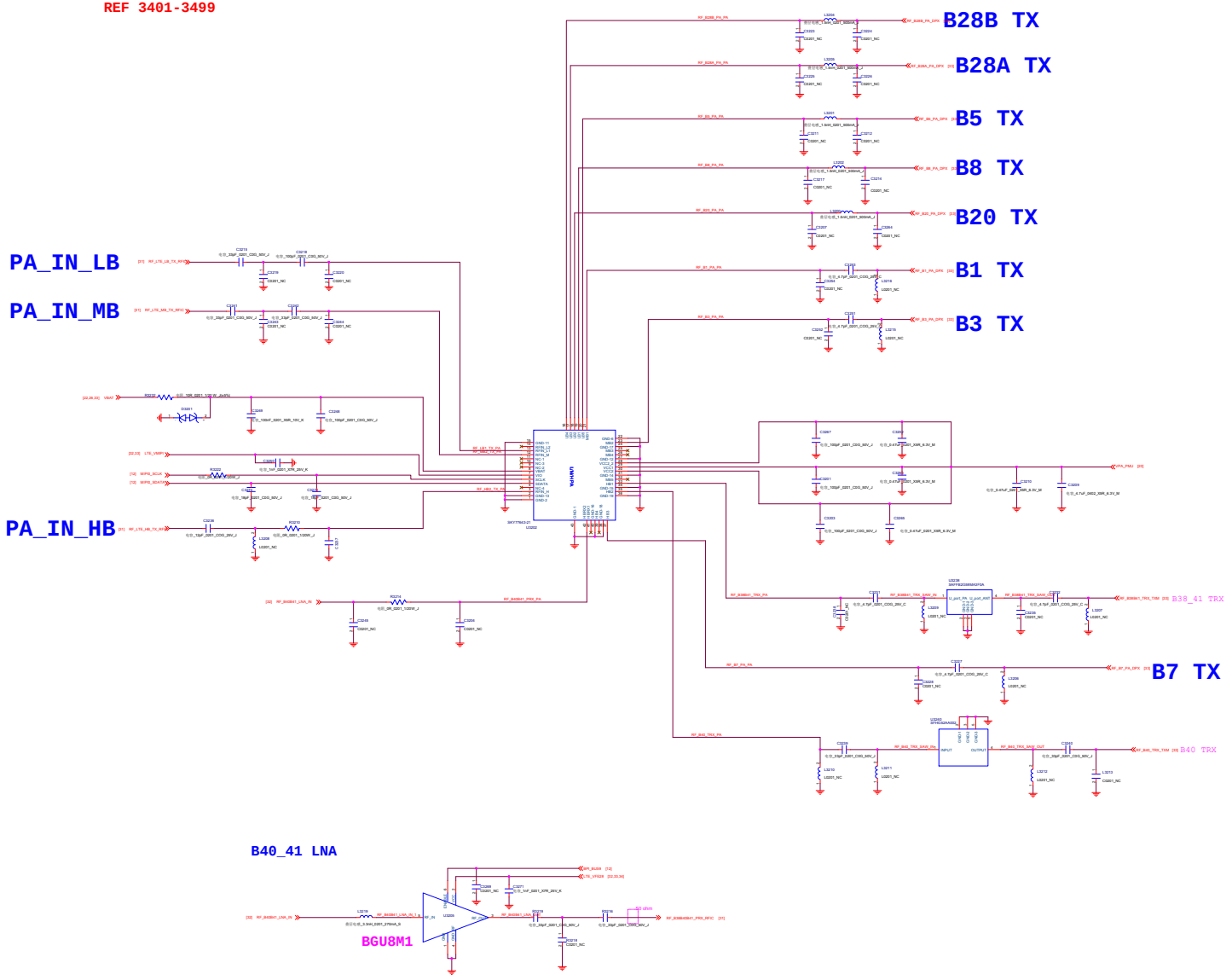
Power domain of MT6177M



OPPO		
Title	31_RF_MT6177_Pin_Out	
Size D	Project A59A_5GBM_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 31 of 35	

PA & PA THERMAL

REF 3401-3499

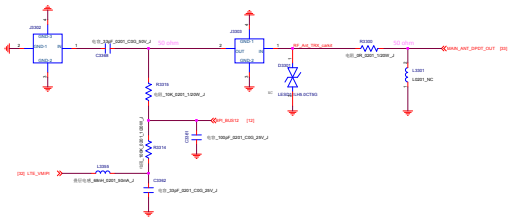


RF Power S

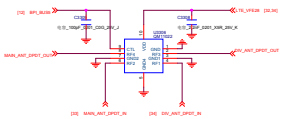
OPPO			
Title	32_RF_MT6177_RF_TX		
Size E	Project A5S_MB_V1		Rev V1
Date: Friday, December 28, 2018		Sheet 32 of 35	

TXM_GSM

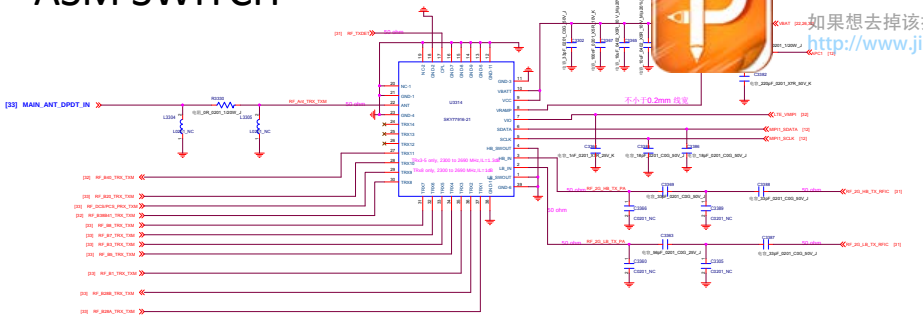
DPDT SWITCH



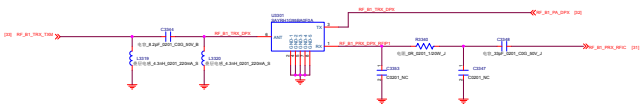
优先保证射频走线，避容通路，不要有断头线



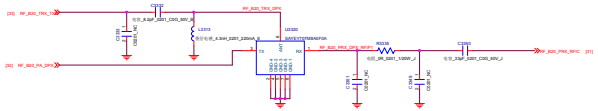
ASM SWITCH



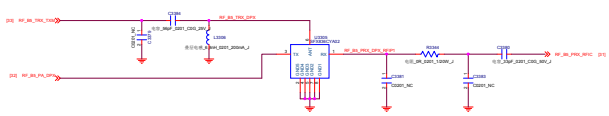
B1 DPX



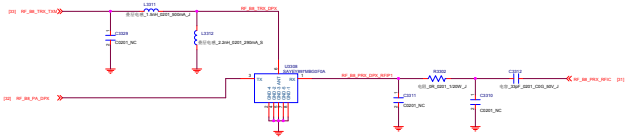
B20 DPX



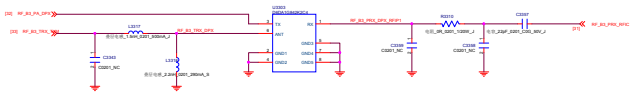
B5 DPX



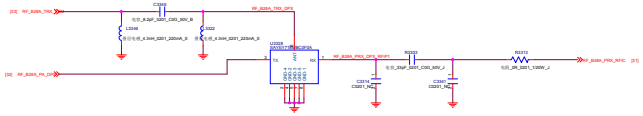
B8 DPX



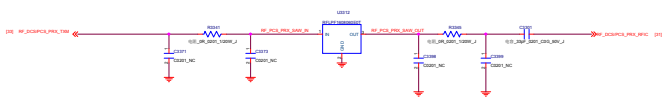
B3 DPX



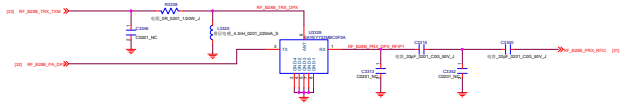
B28A DPX



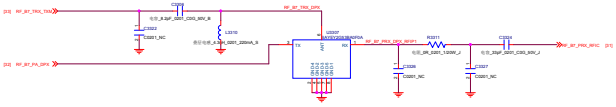
GSM DCS/PCS RX



B28B DPX

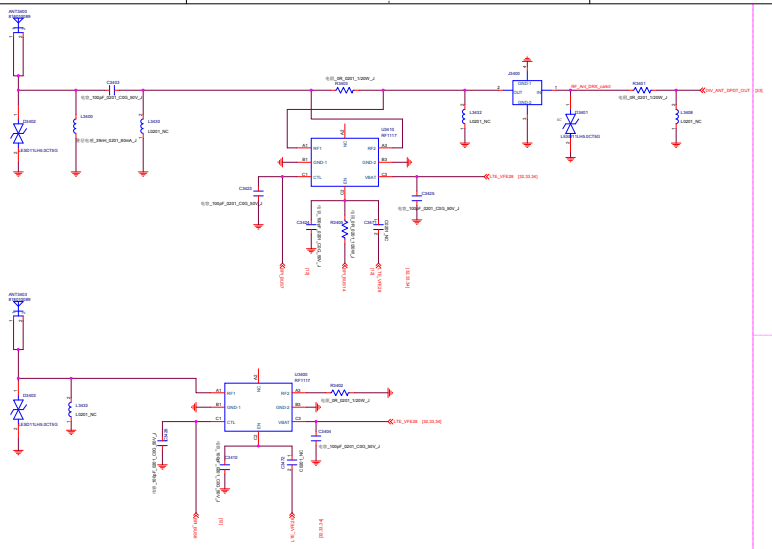


B7 DPX

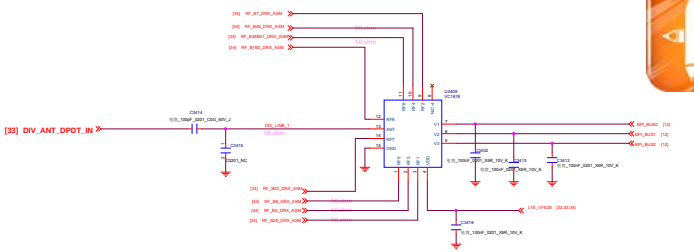


OPPO			
Title	33_RF_MT6177_RF_PRX		
Size E	Project	A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 33 of 35		

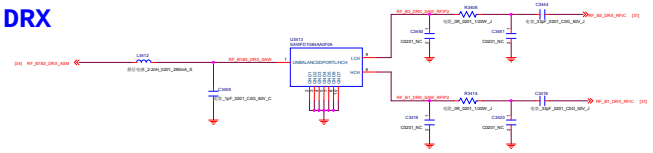
DIV_ANT



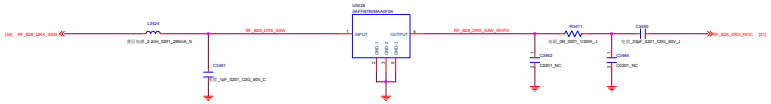
DRX Switch



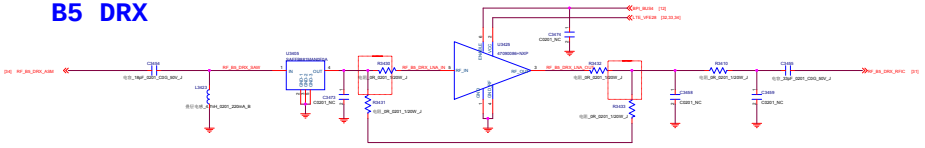
B1/B3 DRX



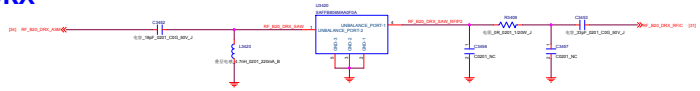
B28 DRX



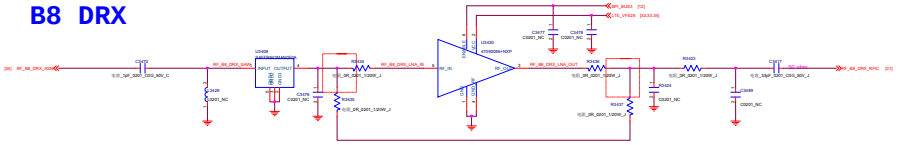
B5 DRX



B20 DRX

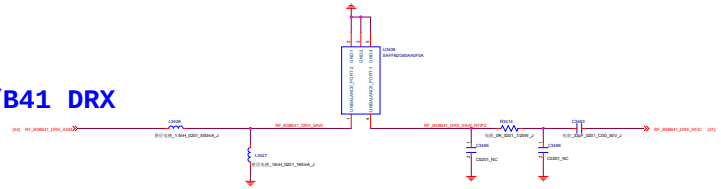


B8 DRX

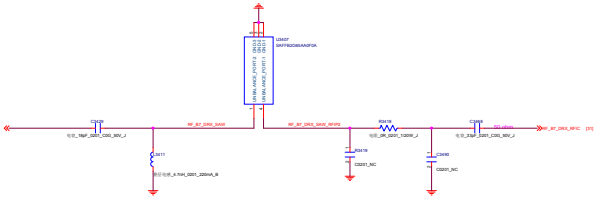


B40 DRX

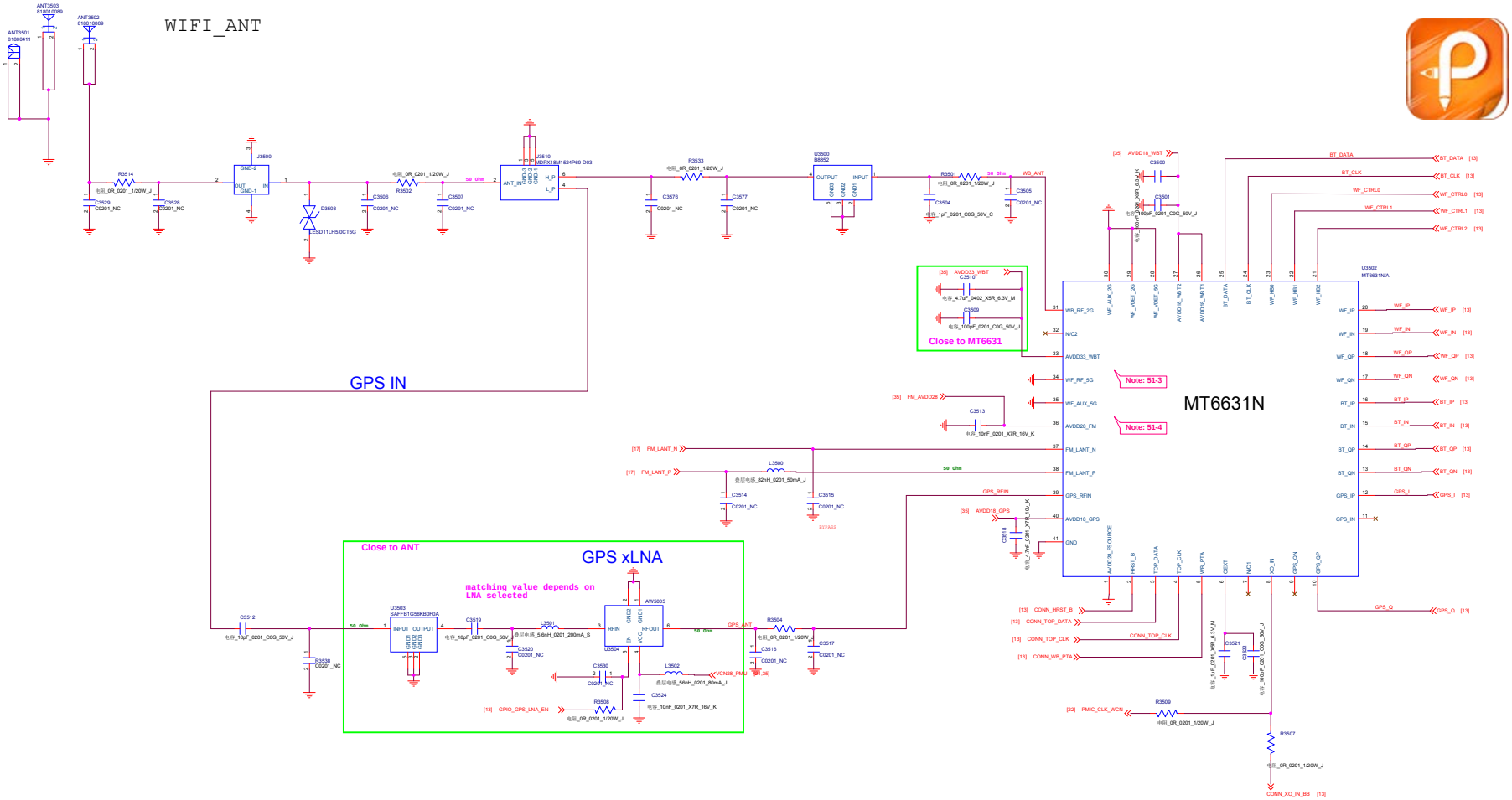
B38/B41 DRX



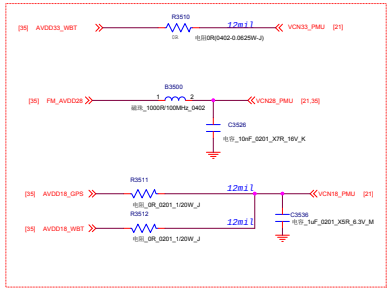
B7 DRX



OPPO			
Title	34_RF_MT6177_RF_DRX		
Size E	Project	A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018		Sheet 34 of 35	



WCN Power Supply



Schematic design notice of "51_CONNECTIVITY_CONSYS_MT6631"	
Note 51-1:	For R5015 size, please select 0402 size or larger one
Note 51-2:	Please refer to MT6765 Baseband design notice for VCN33 LDO selection guide
Note 51-3:	If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND
Note 51-4:	Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support

OPPO		
Title	35_CONNECTIVITY_CONSYS_MT6631	
Size D	Project A5S_MB_V1	Rev V1
Date: Friday, December 28, 2018	Sheet 35 of 35	