

P283: LOW PROFILE NV44/G3-64, TSOP MEMORY x16

REV HISTORY

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- Page14: NVVDD & FBVDDQ
- Page15: TMDS\_IOVDD,TMDS\_PLLVDD,5V,F3V3

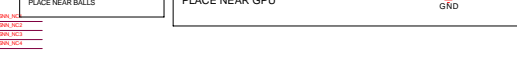
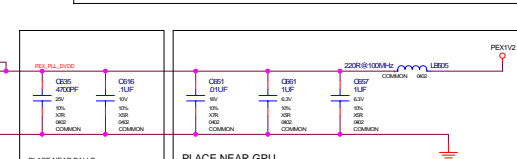
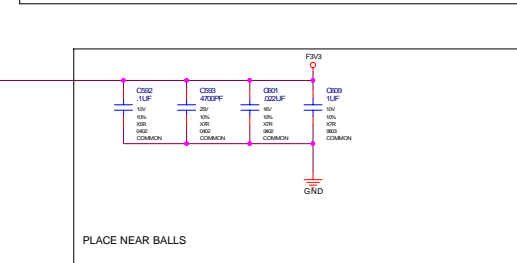
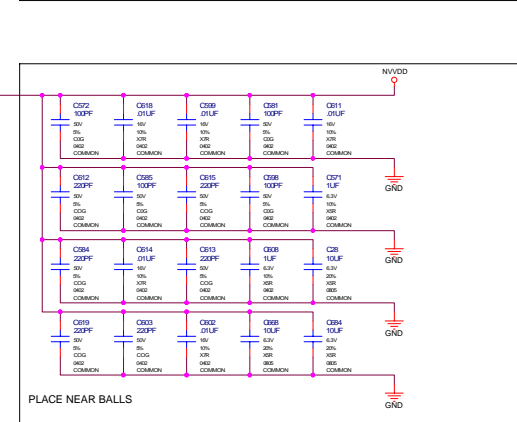
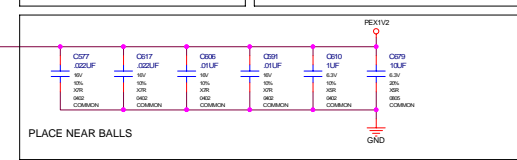
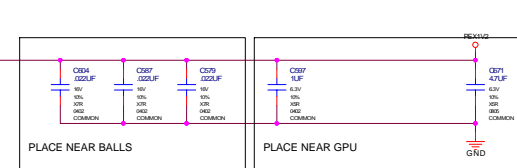
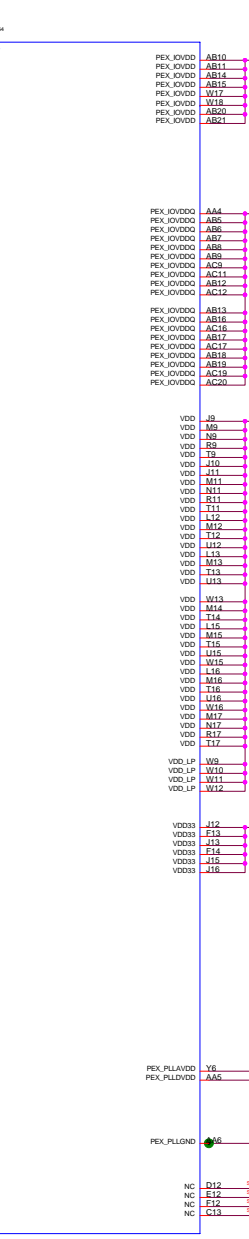
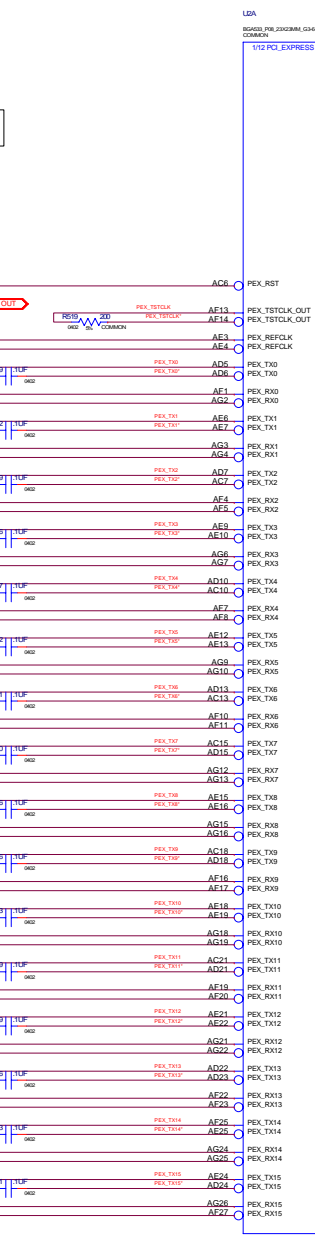
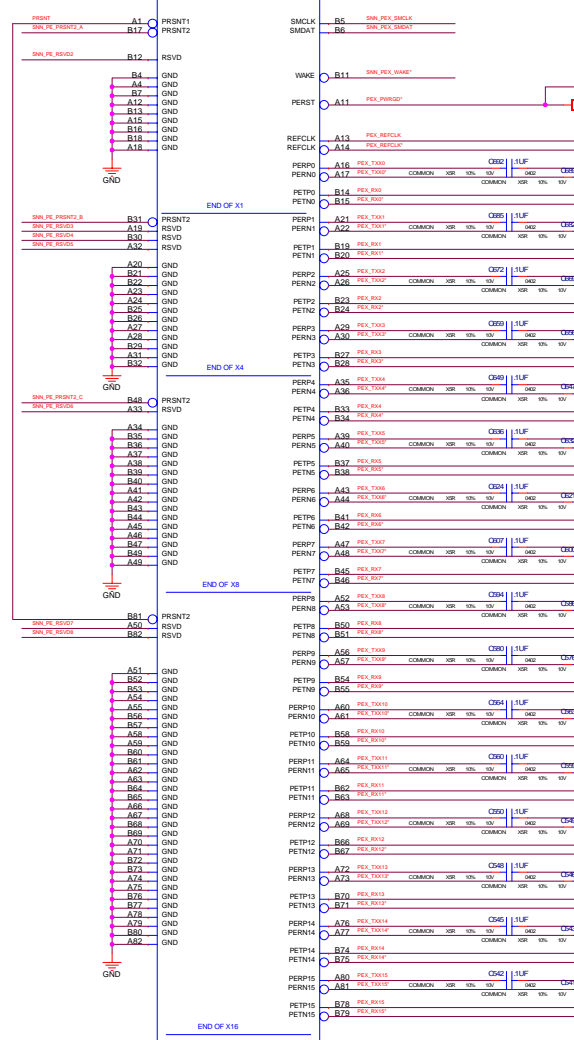
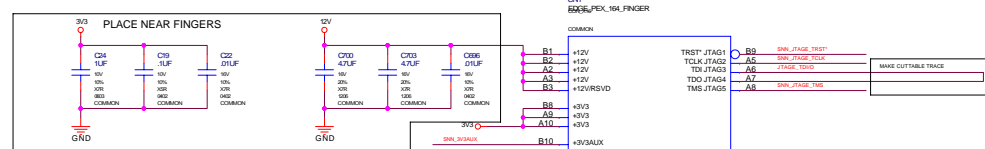
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2	001	800-100B3-0001-000	SR1.01 - NV44 G3-64, VGA+HDTV, 350275MHz, 64 bit 64MB MEMORY INTERFACE
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P203 Overview

A	B	C	D	E	F	G	H
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## PEX-Interface

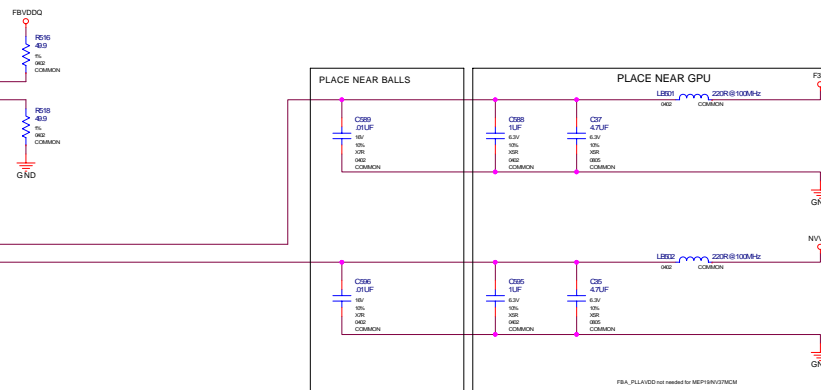
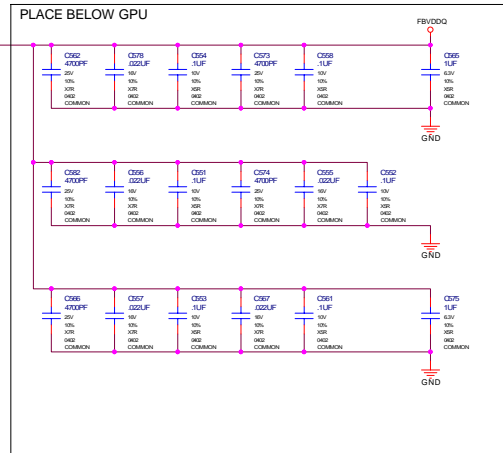
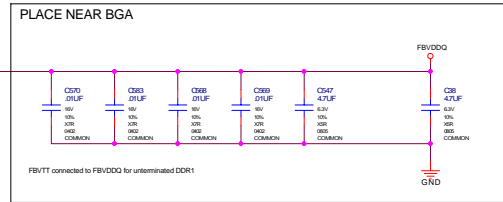
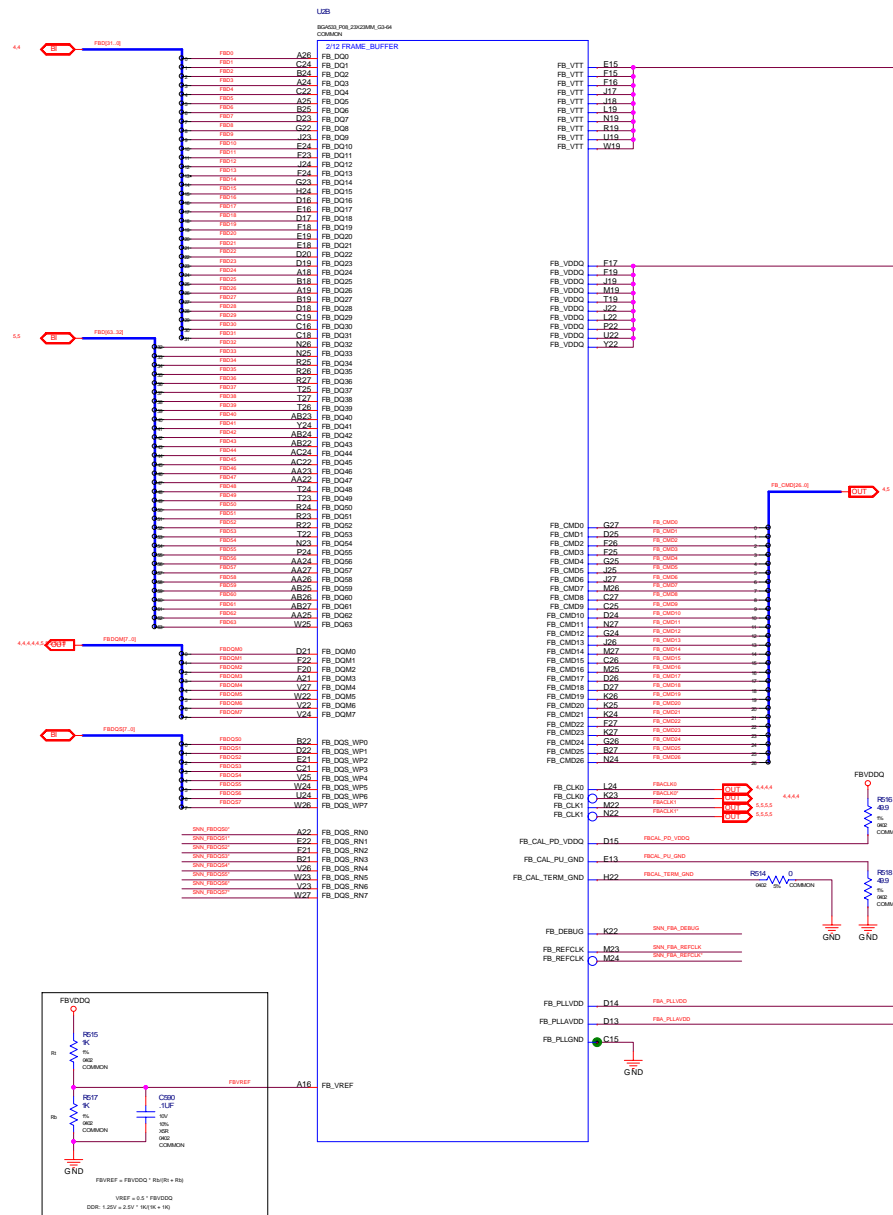


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PCB_10T04	PCB_10T04	PCB_10T	200M
PCB_10T04P	PCB_10T04P	PCB_10T	200M
PCB_110	PCB_110	PCB_110	200M
PCB_110P	PCB_110P	PCB_110	200M
PCB_120	PCB_120	PCB_120	200M
PCB_120P	PCB_120P	PCB_120	200M
PCB_125	PCB_125	PCB_125	200M
PCB_125P	PCB_125P	PCB_125	200M
PCB_130	PCB_130	PCB_130	200M
PCB_130P	PCB_130P	PCB_130	200M
PCB_140	PCB_140	PCB_140	200M
PCB_140P	PCB_140P	PCB_140	200M
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PCB_150P	PCB_150P	PCB_150	200M
PCB_160	PCB_160	PCB_160	200M
PCB_160P	PCB_160P	PCB_160	200M
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PCB_170P	PCB_170P	PCB_170	200M
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PCB_180P	PCB_180P	PCB_180	200M
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PCB_210	PCB_210	PCB_210	200M
PCB_210P	PCB_210P	PCB_210	200M
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PCB_230	PCB_230	PCB_230	200M
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PCB_270P	PCB_270P	PCB_270	200M
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PCB_290	PCB_290	PCB_290	200M
PCB_290P	PCB_290P	PCB_290	200M
PCB_300	PCB_300	PCB_300	200M
PCB_300P	PCB_300P	PCB_300	200M
PCB_310	PCB_310	PCB_310	200M
PCB_310P	PCB_310P	PCB_310	200M
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PCB_330P	PCB_330P	PCB_330	200M
PCB_340	PCB_340	PCB_340	200M
PCB_340P	PCB_340P	PCB_340	200M
PCB_350	PCB_350	PCB_350	200M
PCB_350P	PCB_350P	PCB_350	200M
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PCB_360P	PCB_360P	PCB_360	200M
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PCB_390	PCB_390	PCB_390	200M
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PCB_500	PCB_500	PCB_500	200M
PCB_500P	PCB_500P	PCB_500	200M
PCB_500T04	PCB_500T04	PCB_500T	200M
PCB_500T04P	PCB_500T04P	PCB_500T	200M

ASSEMBLY PAGE DETAIL	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL PCI Express Interface
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## GPU: FB-Interface



	Net Name	NET_SPACING_RULE
IN1	FIBCAL_PD_VDD0	10MIL
IN2	FIBCAL_PC_GND	10MIL
IN3	FIBCAL_VTDR_GND	10MIL
IN4	PB_3V3VDD	10MIL
IN5	FIB_P_LAVDD	10MIL
IN6	FIBVEE1	10MIL

# LABTESTPOINTS

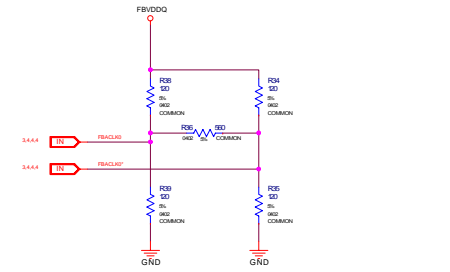
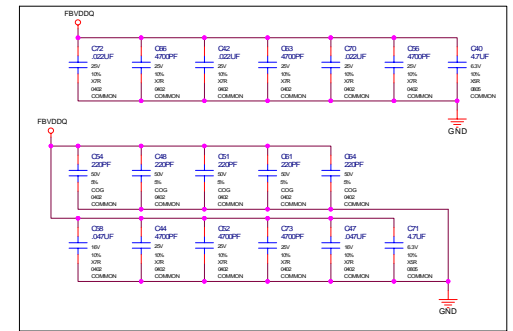
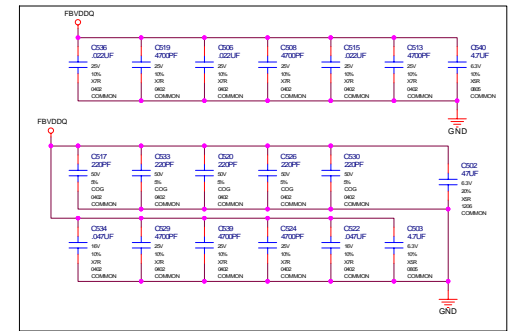
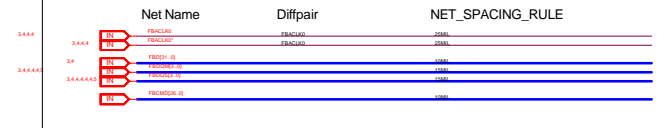
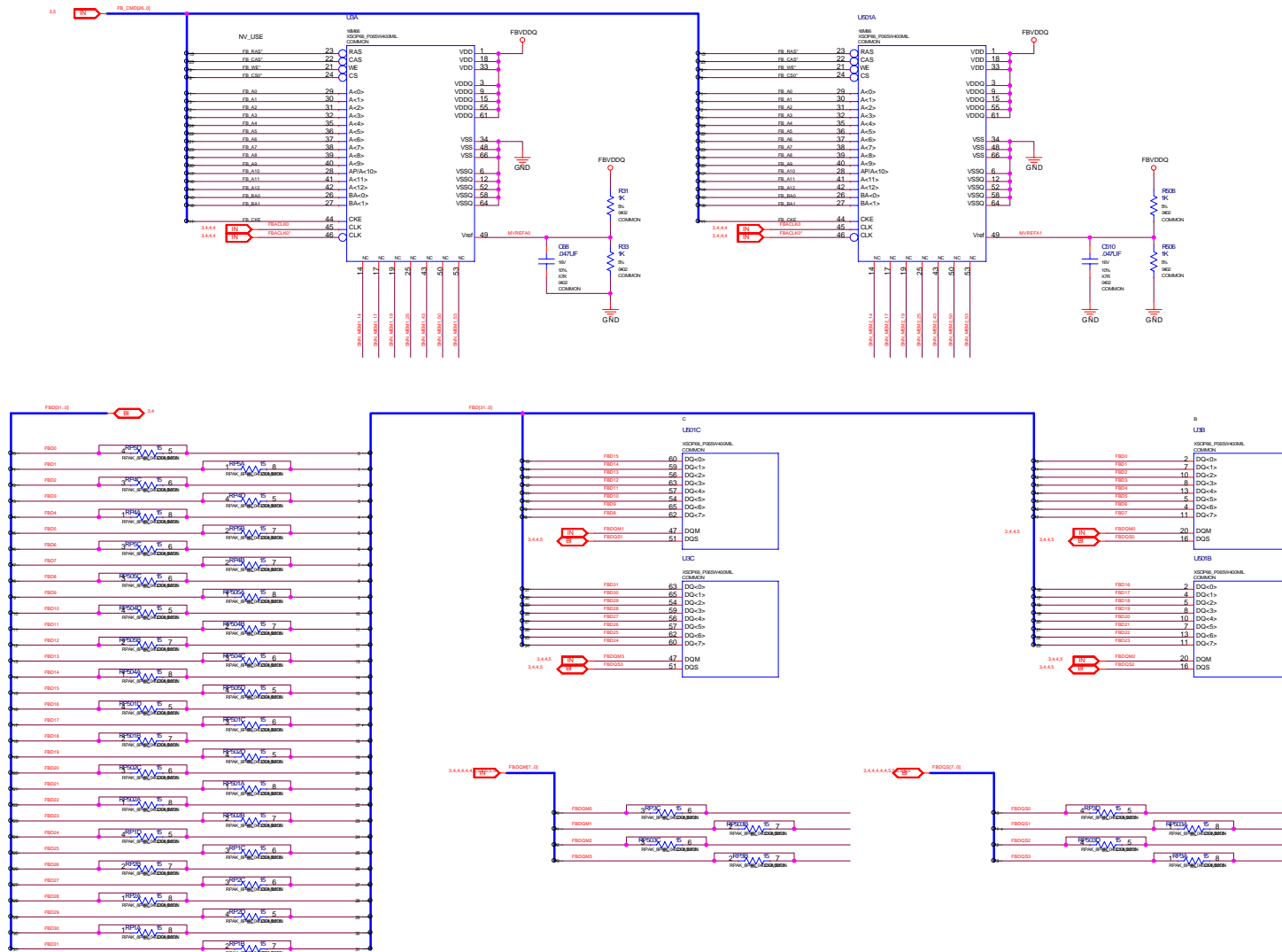
The diagram illustrates the connections for Lab Test Points. It features a central column of test points: FID005, FID001, FID002, FID003, FID004, FID005, FID006, and FID007. To the left, there are two groups of test points: a top group with FID001, FID002, and FID003, and a bottom group with FID004, FID005, FID006, and FID007. To the right, there are two groups of test points: a top group with FID001 and FID002, and a bottom group with FID003 and FID004. The connections are as follows: FID005 is connected to FID001, FID002, FID003, FID004, FID005, FID006, and FID007. FID001 is connected to FID001, FID002, and FID003. FID002 is connected to FID001, FID002, and FID003. FID003 is connected to FID001, FID002, and FID003. FID004 is connected to FID004, FID005, FID006, and FID007. FID005 is connected to FID004, FID005, FID006, and FID007. FID006 is connected to FID004, FID005, FID006, and FID007. FID007 is connected to FID004, FID005, FID006, and FID007. FID001 is connected to FID001 and FID002. FID002 is connected to FID001 and FID002. FID003 is connected to FID001 and FID002.

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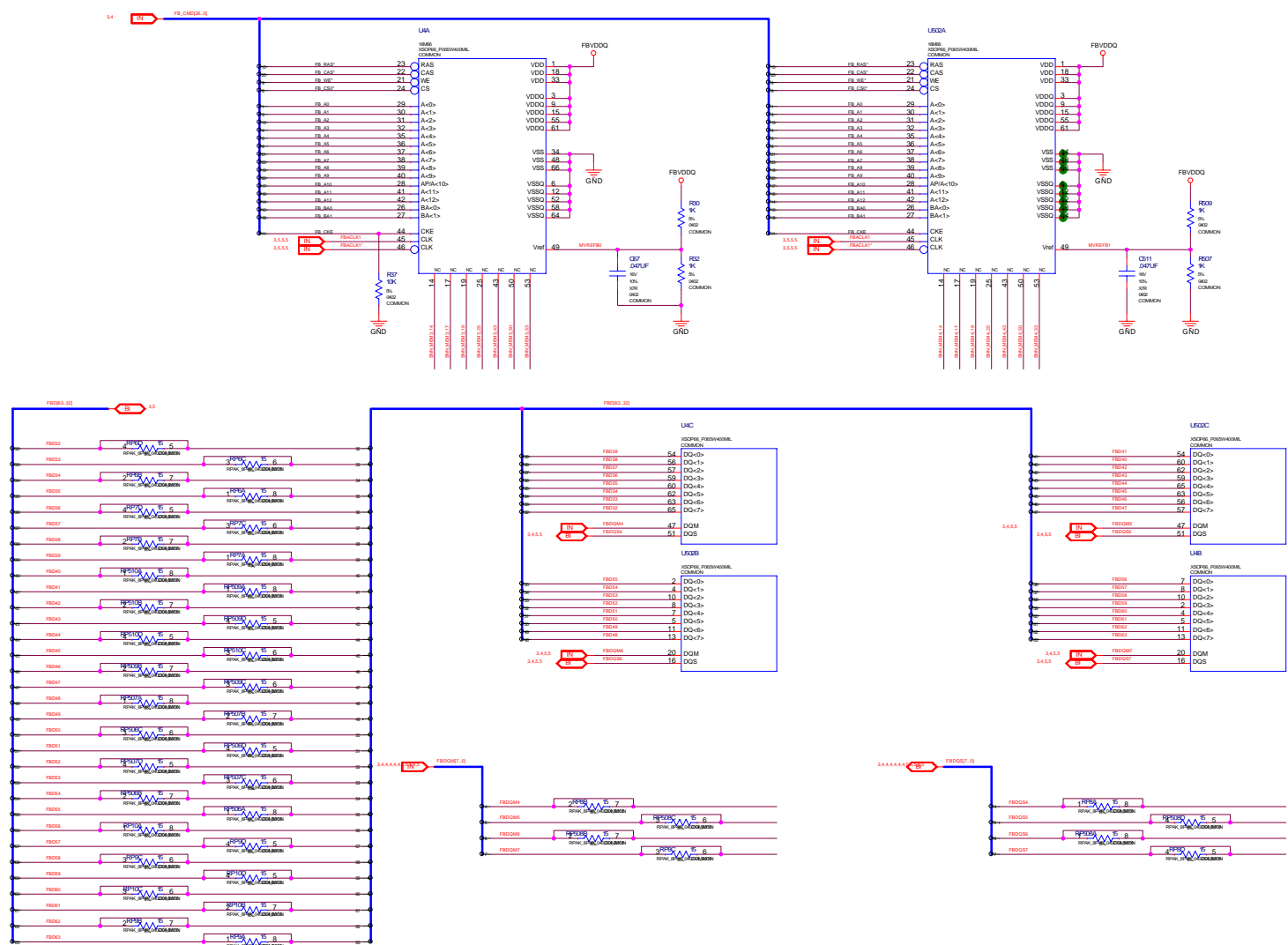
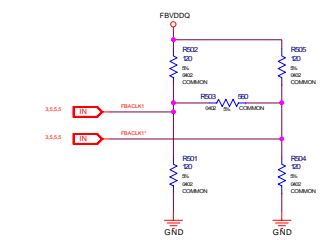
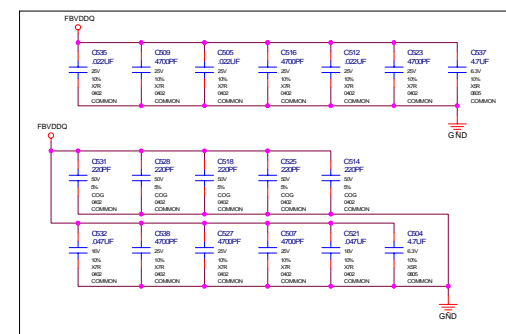
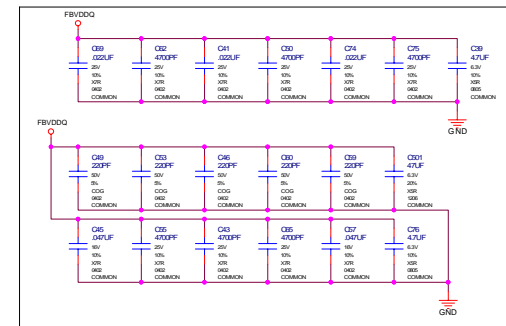
ASSEMBLY  
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO\_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

## Memory Bit 0..31

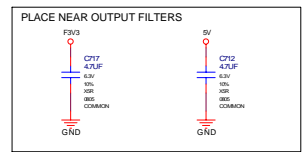
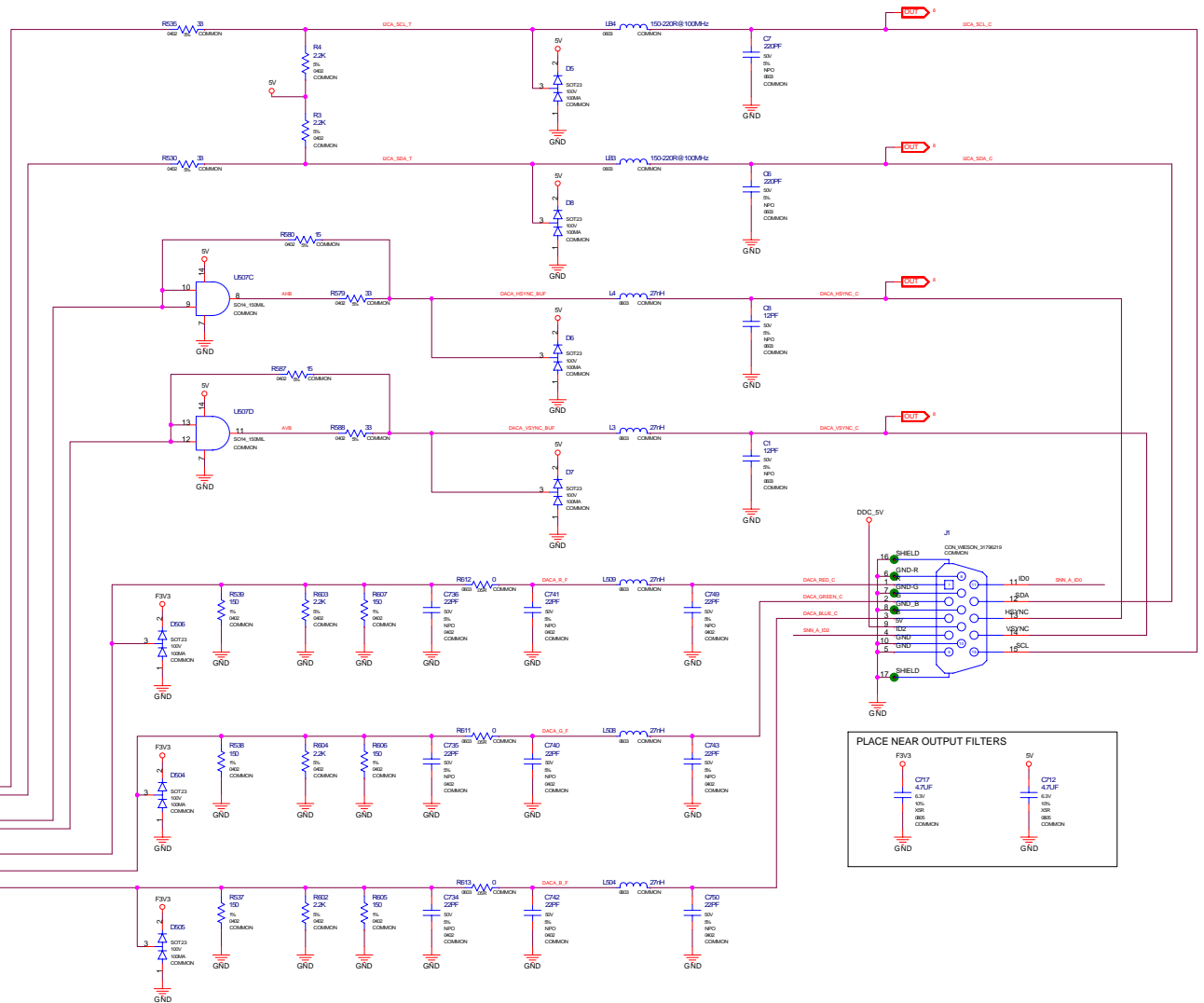
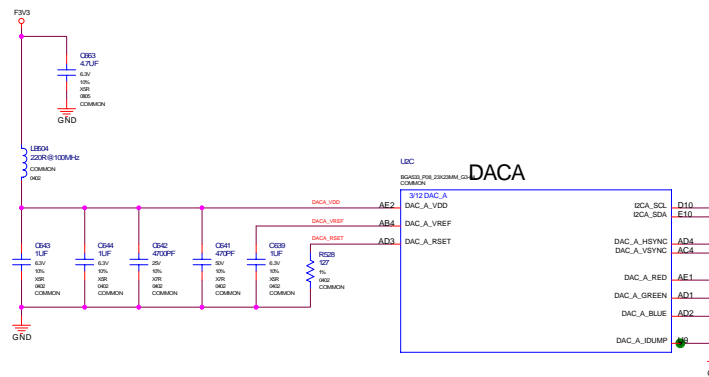
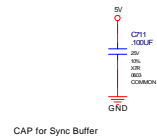


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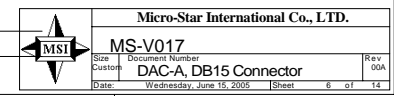


## DAC-A, DB15 Connector

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100%	DATA_B1		100%
100%	DATA_D0T0M1		100%
100%	DATA_D0T0M2		100%
100%	DATA_D0T0		100%
100%	DATA_D0T1		100%
100%	DATA_D0T2		100%
100%	DATA_D0T3		100%
100%	DATA_D0T4		100%
100%	DATA_D0T5		100%
100%	DATA_D0T6		100%
100%	DATA_D0T7		100%
100%	DATA_D0T8		100%
100%	DATA_D0T9		100%
100%	DATA_D0T10	120%	120%
100%	DATA_D0T11		100%
100%	DATA_D0T12		100%
100%	DATA_D0T13		100%
100%	DATA_D0T14		100%
100%	DATA_D0T15		100%
100%	DATA_D0T16		100%
100%	DATA_D0T17		100%
100%	DATA_D0T18		100%
100%	DATA_D0T19		100%
100%	DATA_D0T20		100%
100%	DATA_D0T21		100%
100%	DATA_D0T22		100%
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100%	DATA_D0T24		100%
100%	DATA_D0T25		100%
100%	DATA_D0T26		100%
100%	DATA_D0T27		100%
100%	DATA_D0T28		100%
100%	DATA_D0T29		100%
100%	DATA_D0T30		100%
100%	DATA_D0T31		100%
100%	DATA_D0T32		100%
100%	DATA_D0T33		100%
100%	DATA_D0T34		100%
100%	DATA_D0T35		100%
100%	DATA_D0T36		100%
100%	DATA_D0T37		100%
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100%	DATA_D0T40		100%
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100%	DATA_D0T58		100%
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100%	DATA_D0T60		100%
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100%	DATA_D0T72		100%
100%	DATA_D0T73		100%
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100%	DATA_D0T75		100%
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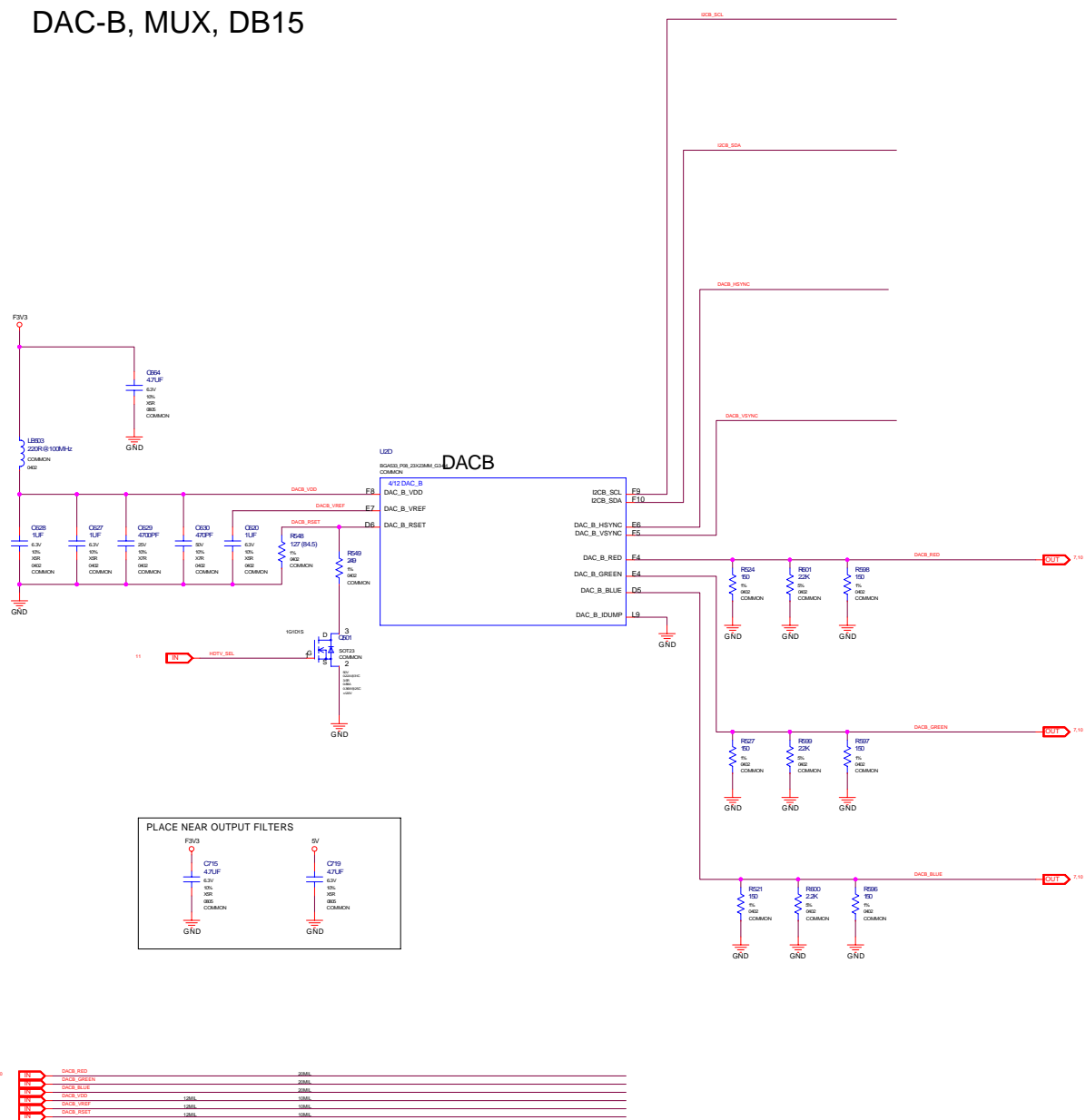


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA, DACB, DACC, Sync Buffers



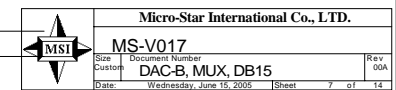
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## DAC-B, MUX, DB15



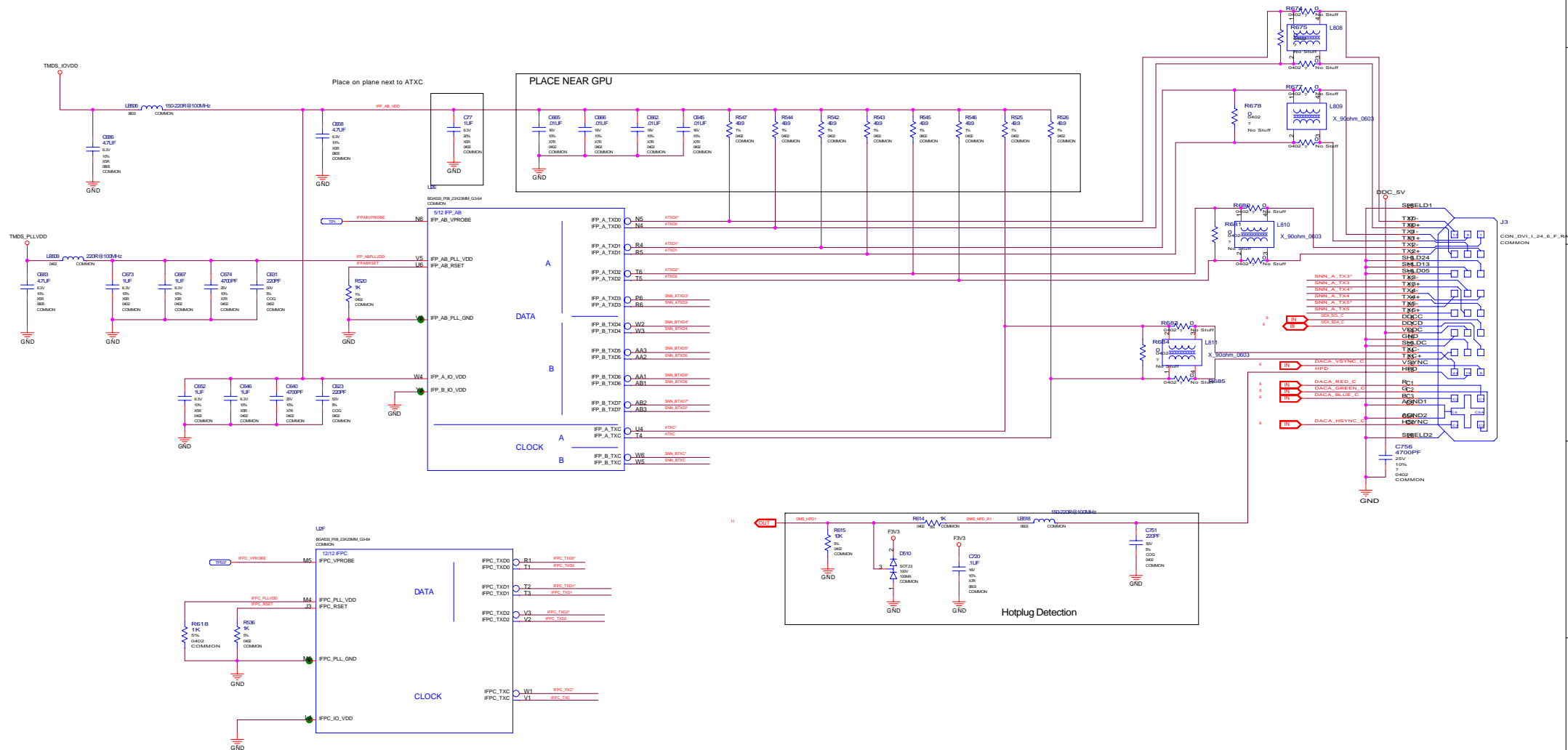
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	VGA Output, TV Out

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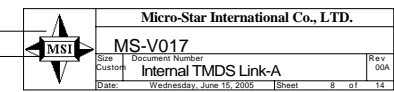
## Internal TMDS LINK-A DMS Connector

	Net Name	Diffpair	NET_SPACING_RULE	Voltage
101	REF_ABN1_VDD			3.3V
102	REF_AB_VDD			3.3V
103	AT01	AT02	250M	
104	AT03	AT04	250M	
105	AT05	AT06	250M	
106	AT07	AT08	250M	
107	AT09	AT10	250M	
108	AT11	AT12	250M	
109	AT13	AT14	250M	
110	AT15	AT16	250M	



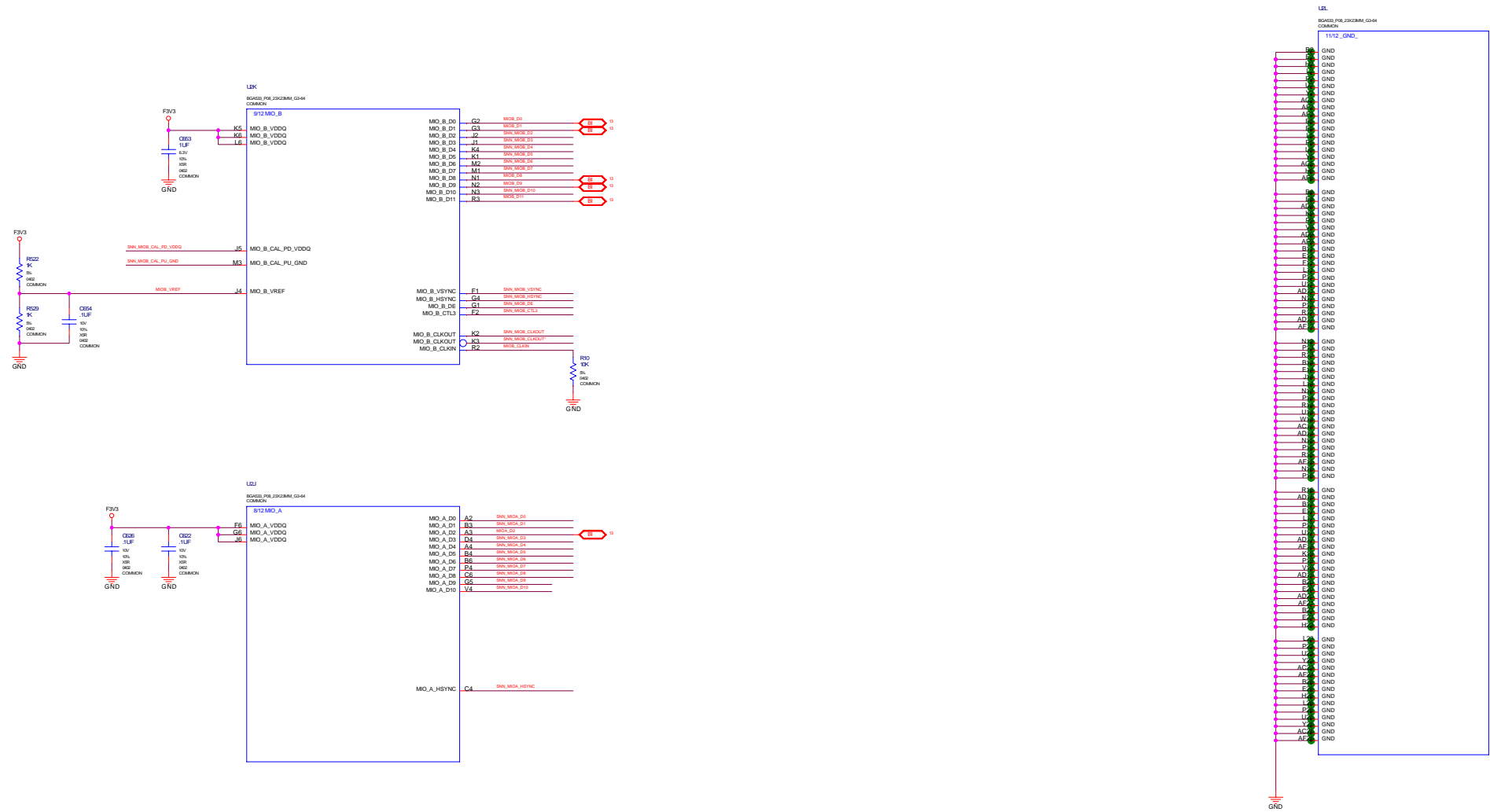
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS Interface

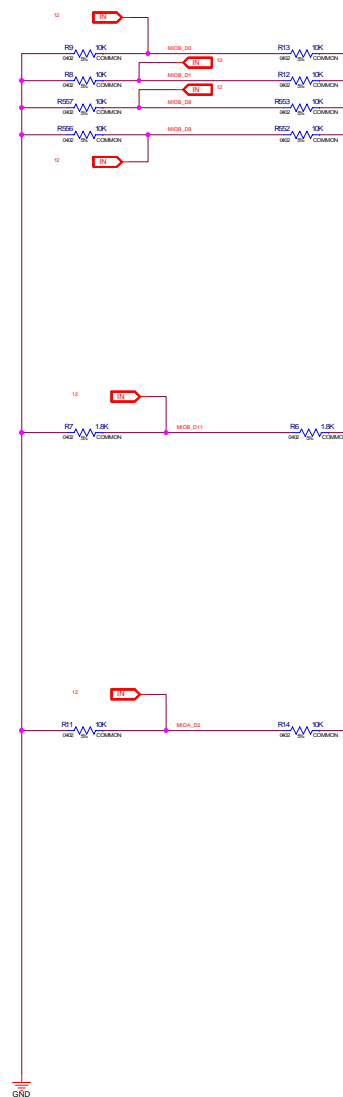




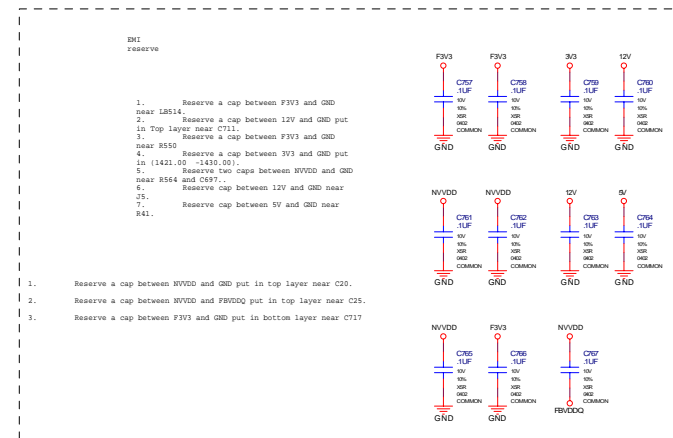
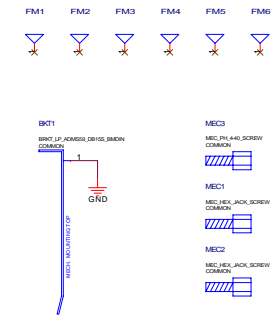
MIOA, MIOB Interface, LPC-ROM



## STRAPS, Mechanical Parts

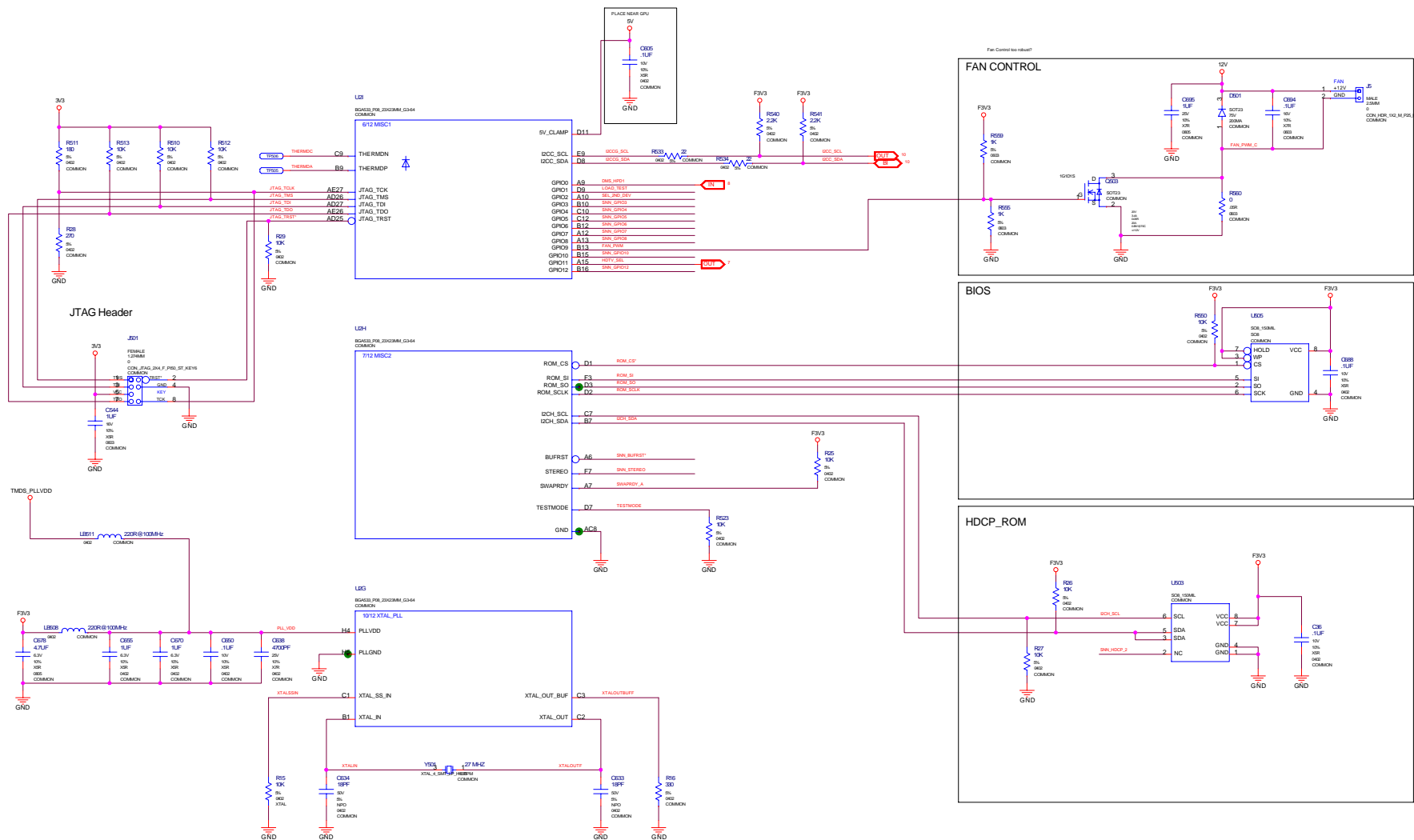


00	PCI_ID_SWAP	UNREVERSED 1 NORMAL
01	SEN_VENDOR	0 NO_BIOS 1 1542 FROM BIOS
02	RAM_CTL0_0	000 KBU 001 8Mx16KDR TSCP 002 KBU 003 8Mx16KDR TSCP 004 KBU 005 8Mx16KDR TSCP 006 KBU 007 8Mx16KDR TSCP 008 KBU 009 8Mx16KDR TSCP 010 16Mx16KDR TSCP 011 KBU 110 KBU 111 KBU
03	RAM_CTL0_1	000 KBU 001 8Mx16KDR TSCP 002 KBU 003 8Mx16KDR TSCP 004 KBU 005 8Mx16KDR TSCP 006 KBU 007 8Mx16KDR TSCP 008 KBU 009 8Mx16KDR TSCP 010 16Mx16KDR TSCP 011 KBU 110 KBU 111 KBU
04	RAM_CTL0_2	000 KBU 001 8Mx16KDR TSCP 002 KBU 003 8Mx16KDR TSCP 004 KBU 005 8Mx16KDR TSCP 006 KBU 007 8Mx16KDR TSCP 008 KBU 009 8Mx16KDR TSCP 010 16Mx16KDR TSCP 011 KBU 110 KBU 111 KBU
05	RAM_CTL0_3	000 KBU 001 8Mx16KDR TSCP 002 KBU 003 8Mx16KDR TSCP 004 KBU 005 8Mx16KDR TSCP 006 KBU 007 8Mx16KDR TSCP 008 KBU 009 8Mx16KDR TSCP 010 16Mx16KDR TSCP 011 KBU 110 KBU 111 KBU
06	CRYSCTL_0	00 13.000 MHz 01 14.31818 MHz 02 27.000 MHz 03 33.000 MHz 11 33.000 MHz
07	CRYSCTL_1	00 13.000 MHz 01 14.31818 MHz 02 27.000 MHz 03 33.000 MHz 11 33.000 MHz
08	TV_MODE_0	00 SECAM 01 NTSC 10 PAL 11 CRT
09	AGP_30_0h	0 AGP0 ENABLED 1 AGP0 DISABLED
10	AGP_30h	0 SBA ENABLED 1 SBA DISABLED
11	AGP_F4F0Fh	0 F70 ENABLED 1 F70 DISABLED
12	PCI_DEV0_0	1100 (default 0000F0)
13	PCI_DEV0_1	1100 (default 0000F0)
14	PCI_DEV0_2	1100 (default 0000F0)
15	PCI_DEV0_3	1100 (default 0000F0)
16	BUS_TYPE	0 PCI 1 AGP
17	FP_FFACE	0 48h 1 128h (DEFAULT)
18	FB_0	00 0MB 01 128M 10 256M (DEFAULT) 11 512M
19	FB_1	00 0MB 01 128M 10 256M (DEFAULT) 11 512M
20	BR	0 BRIDGE DISABLED 1 BRIDGE ENABLED
21	BR_10Mh	BR BITS KNOWN IF BRIDGE IS DISABLED
22	BR_40Fh	BR BITS KNOWN IF BRIDGE IS DISABLED
23	BR_ID	BR ID
24	ROM_TYPE_0	0 PARALLEL 01 SERIAL_40F0F 10 SERIAL_5ET40F 11 LPC
25	ROM_TYPE_1	0 PARALLEL 01 SERIAL_40F0F 10 SERIAL_5ET40F 11 LPC
26	USER_0	0000 (DEFAULT)
27	USER_1	0000 (DEFAULT)
28	USER_2	0000 (DEFAULT)
29	USER_3	0000 (DEFAULT)
30	PCI_P0P0Fh_LUT_ADDRESS	PCI_P0P0Fh_LUT_ADDRESS
31	PCI_P0P0Fh_LUT_ADDRESS	PCI_P0P0Fh_LUT_ADDRESS

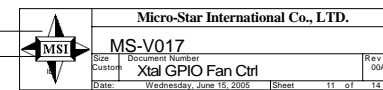


## XTAL, GPIO, BIOS, Fan Control, JTAG Headers

	Net Name	NET_PHYSICAL_TYPE	NET_SPACING_RULE
Net1	XTALIN	DIFF_PAIR_TRACK	DIFF_PAIR
Net2	XTALOUT	DIFF_PAIR_TRACK	DIFF_PAIR
Net3	PLUG0	DIFF_PAIR_TRACK	DIFF_PAIR
Net4	DRP_PLUG0	DIFF_PAIR_TRACK	DIFF_PAIR

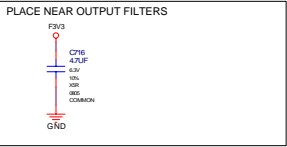



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, GPIO, BIOS, Fan Control, JTAG Headers



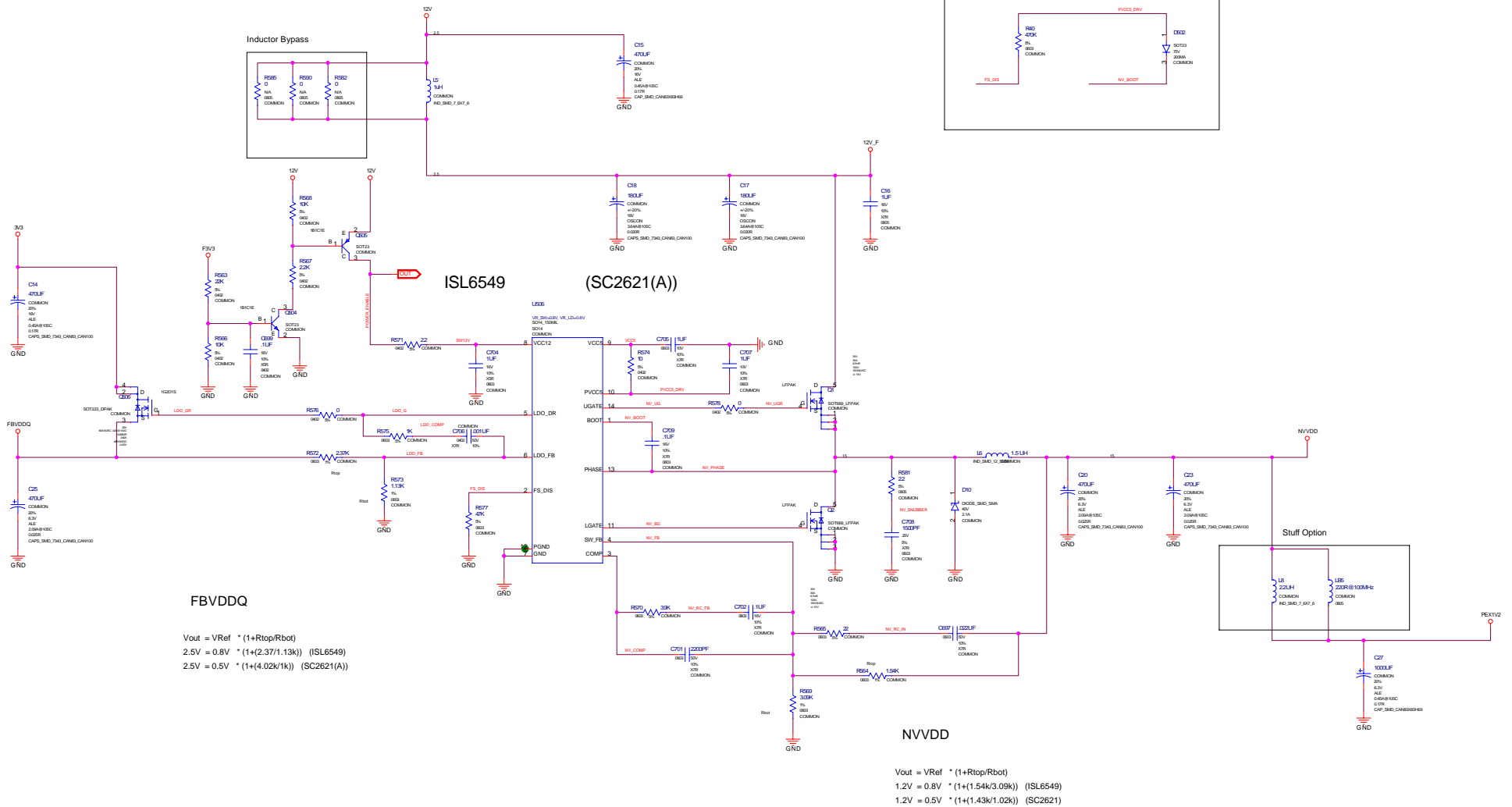
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Timing diagram for SV\_FUSED signal. The signal is high for a duration of 12MIL before transitioning to low. The transition is labeled SV.

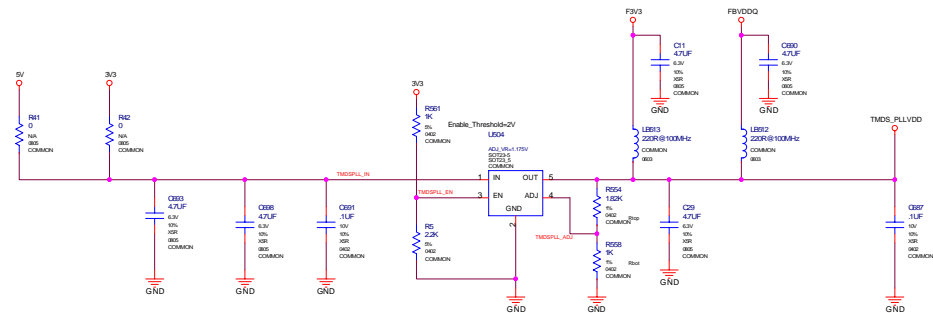
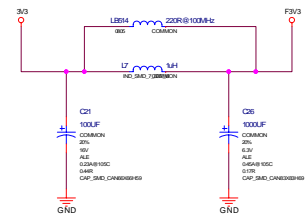
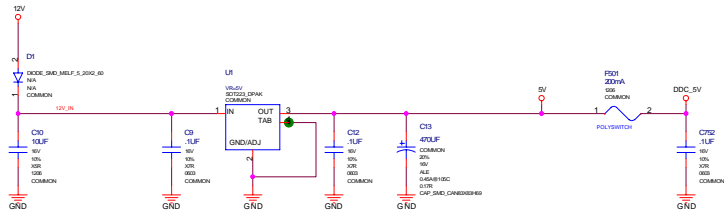


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	<b>MS-V017</b>		
	Size Custom	Document Number <b>VIDEO CONN:MiniDIN AV out</b>	Rev 00A
	Date: Wednesday, June 15, 2005	Sheet 12 of 14	

PowerSupply: NVVDD, FBVDDQ



PowerSupplyII: 5V, DDC5V, A3V3, F3V3, TMDS\_PLLVDD

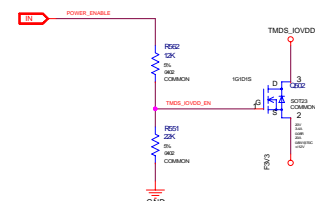


TMDS\_PLLVDD

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

$$2.5 = V_{Ref} \cdot (1 + R_{top}/R_{bot})$$

Net Name	NET_PHYSICAL_TYPE	Voltage
SV	SV	3V
DDC_SV	DDC_SV	3V
F3V3	F3V3	3.3V
TMD5_PLLVDD	TMD5_PLLVDD	3.3V
TMD5_PLLVDD	TMD5_PLLVDD	3.3V
SV	SV	3V
TMD5_J0VDD	TMD5_J0VDD	3V
TMD5_J0VDD	TMD5_J0VDD	3V



ASSEMBLY  
PAGE DETAIL

PowerSupply1t: 5V, DDC5V, A3V3, F3V3, TMDS\_PLLVDD



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MS-V017

Size	Document Number
Custom	PowerSupply11: 5V DDC5V A3

Date: Wednesday, June 15, 2005		Sheet 14 of 14	
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