B C D E F G

MS8888

18P112, NV18, 4Mx32DDR, 64MB, Video IN, TV OUT, DVI-I, VGA, AGP8X, Hardware Monitor, Twin BIOS

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A00 INITIAL VERSION Removed MBDET circuit bypass resistor STRAP resistors, stuffing options set STRAP resistors. USER strap :=0 DACB RSET modification resistor 1%->5% SYNC amplifier, bypass resistors removed DACB RGB filter, bypass capacitors set to NO STUFF DVI-HPD signal, voltage dividor 10k/15k set near DVI 24MHZ signal to 1394, changed stuffing option to disable trace VIDEO in connector internal, added A3V3 decoupling caps. DVOCLKOUT signal, series termination added PD input 1394, stuffing option of series resistor set to NO STUFF LDOs, calculation information added LDO for TMDSPLL, changed resistor values to create 3V3 LDO for TMDSPLL, complex bypass resistors simplified. 1394 POWERCLASS, 5VSENSE signal renamed to EXTsense and generated from 12VEXT ADDED OFFPAGE SYMBOLS, OPTICAL IMPROVEMENTS A01 Replaced NV18 symbol_9. Pin changes Thermal sensor Changed TMDS constraints to 10MIL_G2G_30MIL Changed THERM, THERM* constraints to 10MIL_G2G_10MIL Added SST45VF BIOS type with necessary strap resistors. Added Pullup on ROMCS* Replaced backdrive diode TMDS3V3 by SCHOTTKY type with 1A Added bypass resistors to Sync Amplifier Changed GND pinusage on internal 1394 connector Added compensation to FBVDD regulator Added supply rail from 3V3 for switching regulator to solve 3V3 shutdown Added alternative circuit to solve switch reg. 3v3 shutdown Added hex iack screws as symbols Added cap for CG_VREF on AGP Added bypass resistors for primary inductor of switch regulator Added pulldown for 7114 TRST Jtag signal

Changed AGPVREF_CG rule to 12mil tracewidth
Page2: changed AGPVREF_CG generation for 8X mode
Page6: Added series resistor in FRWR_PME_

HISTORY:

A02

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