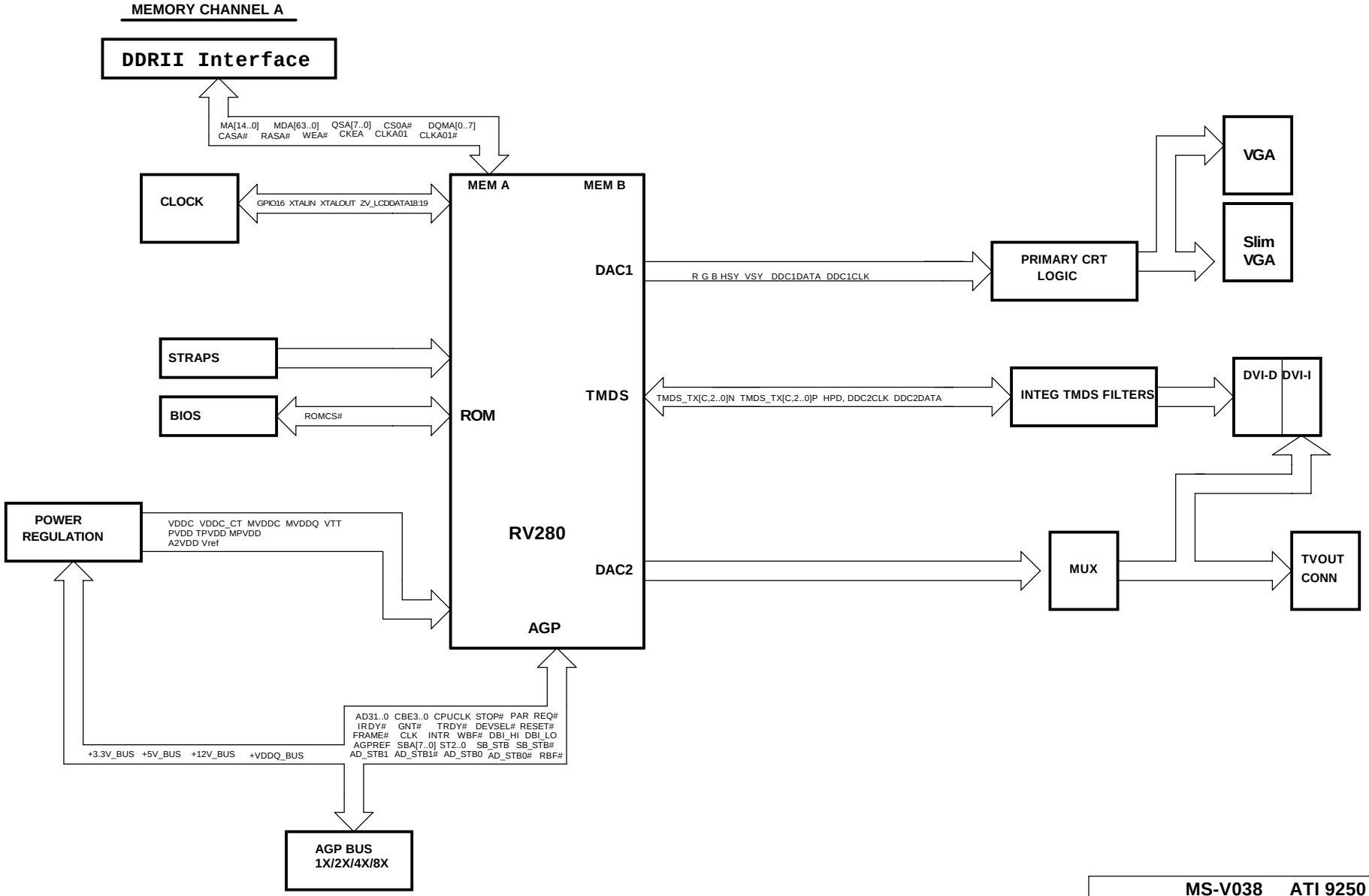
V038-0A



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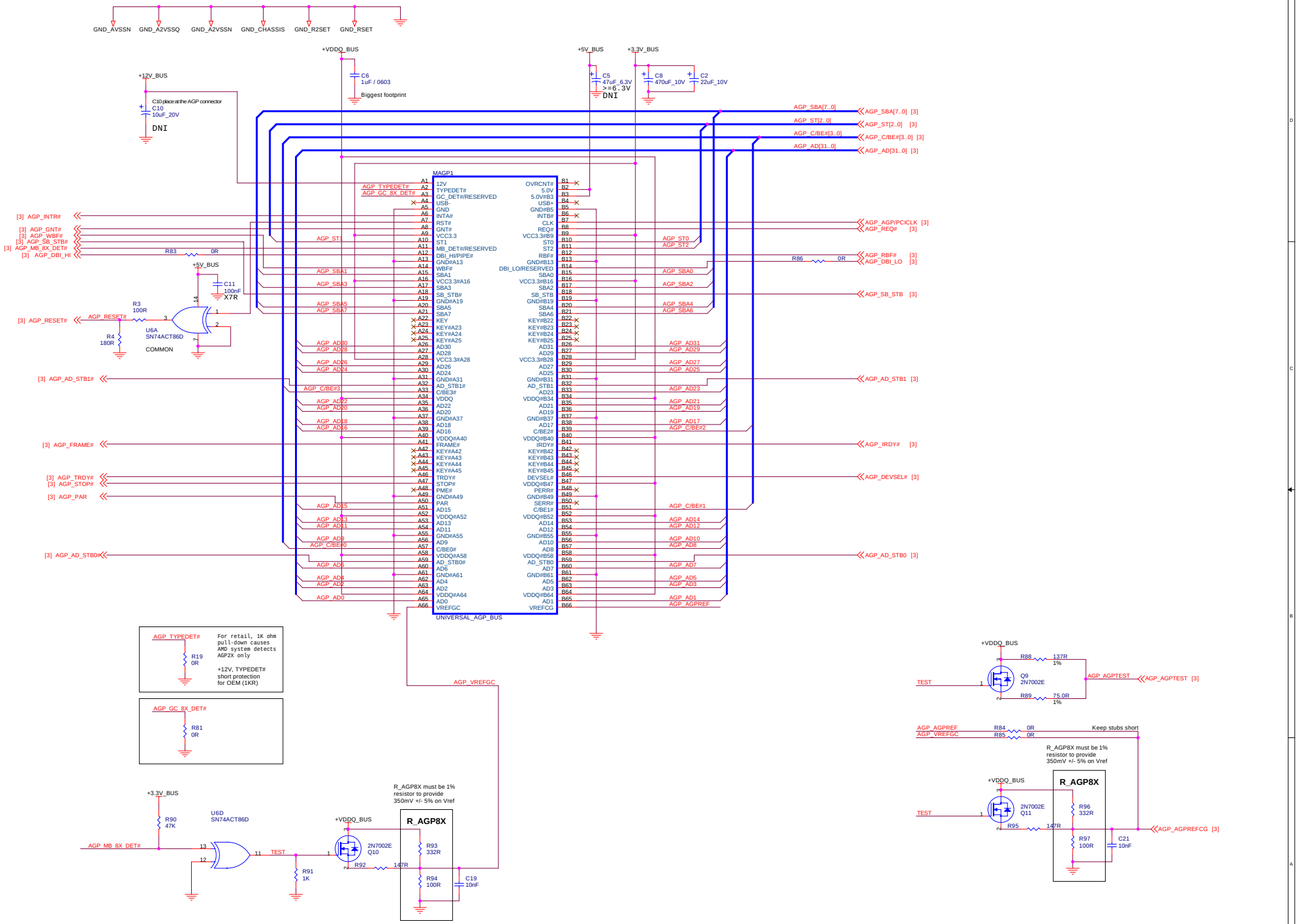

UNIVERSAL VREFGC CIRCUIT (2X, 4X, 8X)

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Size: Custom	Document Number	Rev: 10
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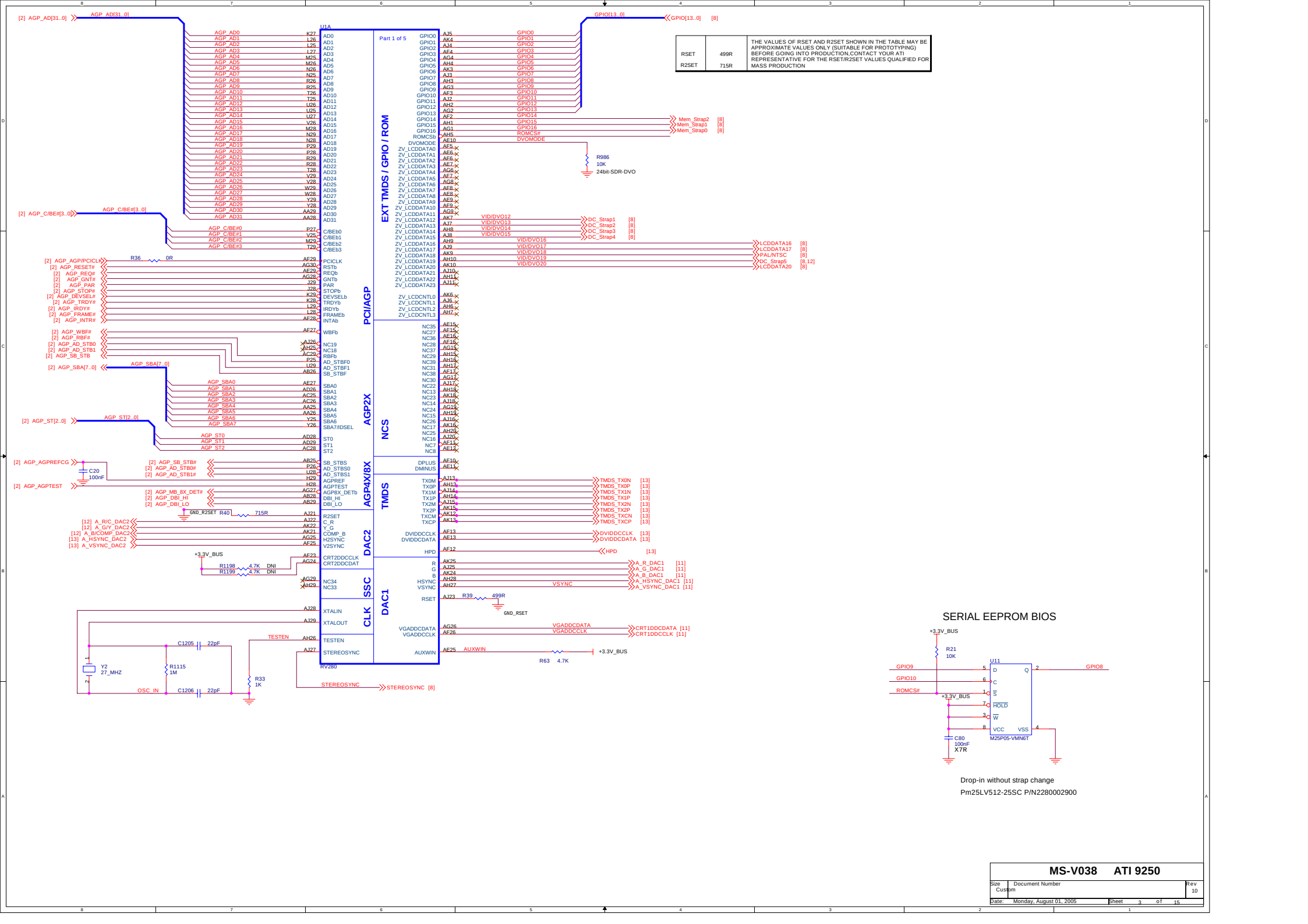
U1A
Part 1 of 5
EXT TMDS / GPIO / ROM
PCI/AGP
AGP2X
NCS
AGP4X/8X
TMDS
DAC2
SSC
CLK
DAC1
AGP_AD[31..0]
AGP_C/BE#[3..0]
AGP_SBA[7..0]
AGP_ST[2..0]
GPIO[13..0]
GPIO[13..0] [8]
RSET 499R
R2SET 715R
THE VALUES OF RSET AND R2SET SHOWN IN THE TABLE MAY BE APPROXIMATE VALUES ONLY (SUITABLE FOR PROTOTYPING) BEFORE GOING INTO PRODUCTION,CONTACT YOUR ATI REPRESENTATIVE FOR THE RSET/R2SET VALUES QUALIFIED FOR MASS PRODUCTION
R986 10K 24bit-SDR-DVO
R36 0R
C20 100nF
R40 715R
GND_R2SET
R1198 4.7K DNI
R1199 4.7K DNI
+3.3V_BUS
Y2 27_MHZ
R1115 1M
C1205 22pF
C1206 22pF
R33 1K
OSC_IN
TESTEN
STEREOSYNC
STEREOSYNC [8]
R39 499R
GND_RSET
R63 4.7K
AUXWIN
VSYNC
HPD
SERIAL EEPROM BIOS
R21 10K
C80 100nF X7R
U11
M25P05-VMN6T
GPIO8
GPIO9
GPIO10
ROMCS#
Drop-in without strap change
Pm25LV512-25SC P/N2280002900
MS-V038 ATI 9250
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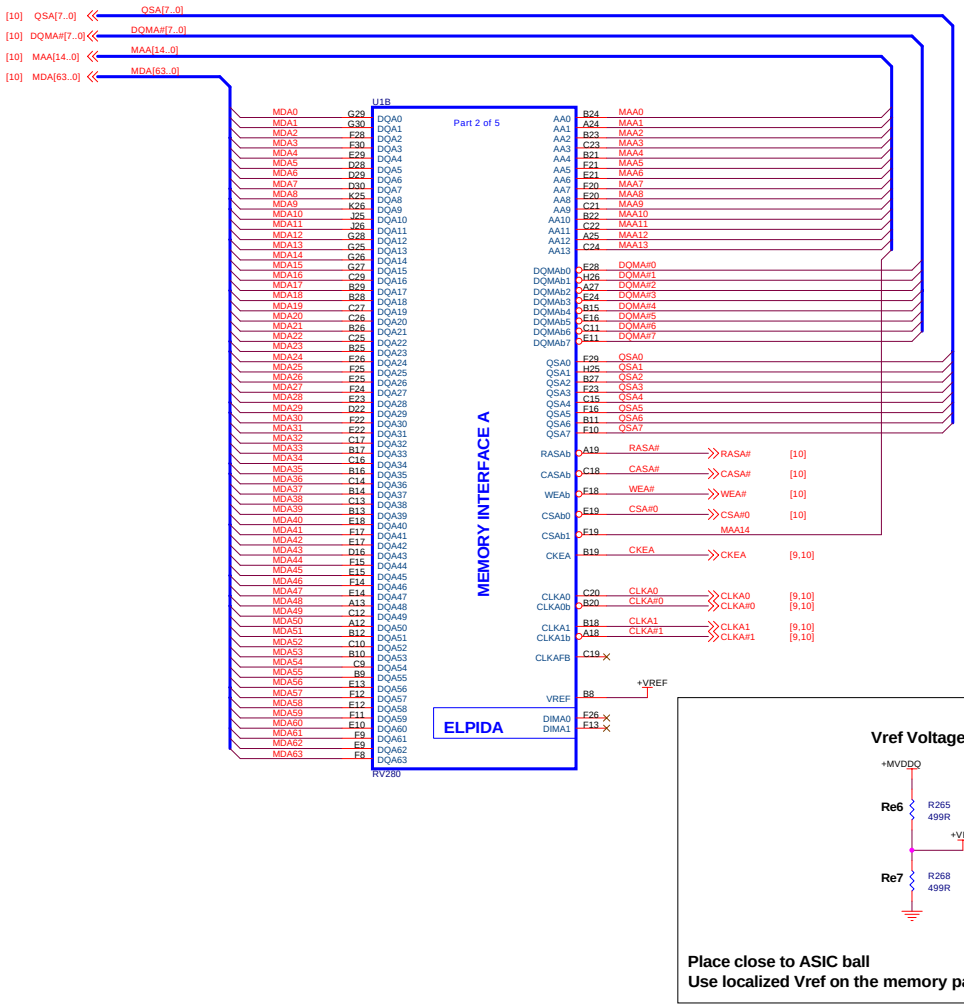
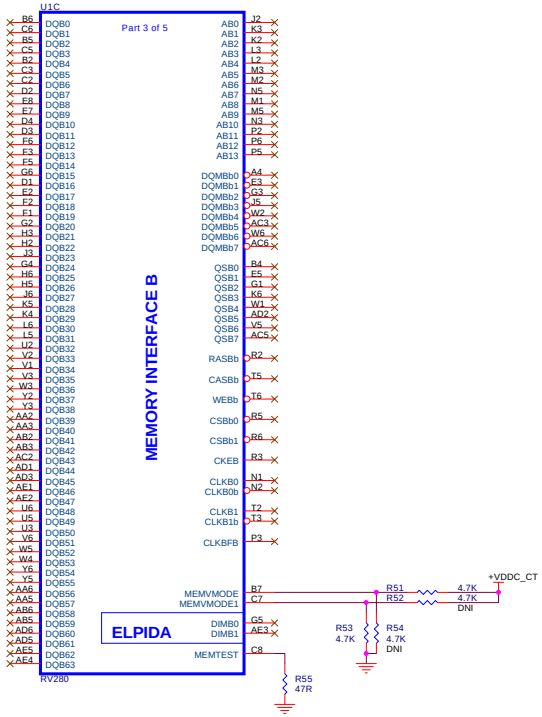
MEMORY CHANNEL A



Vref Voltage

Place close to ASIC ball
Use localized Vref on the memory page

MEMORY CHANNEL B



MEMVMODE[1:0]	MEMORY IO VOLTAGE	
01	2.5V (DDR)	Default
1 0	1.8V (DDR)	
11	3.3V (SDR)	

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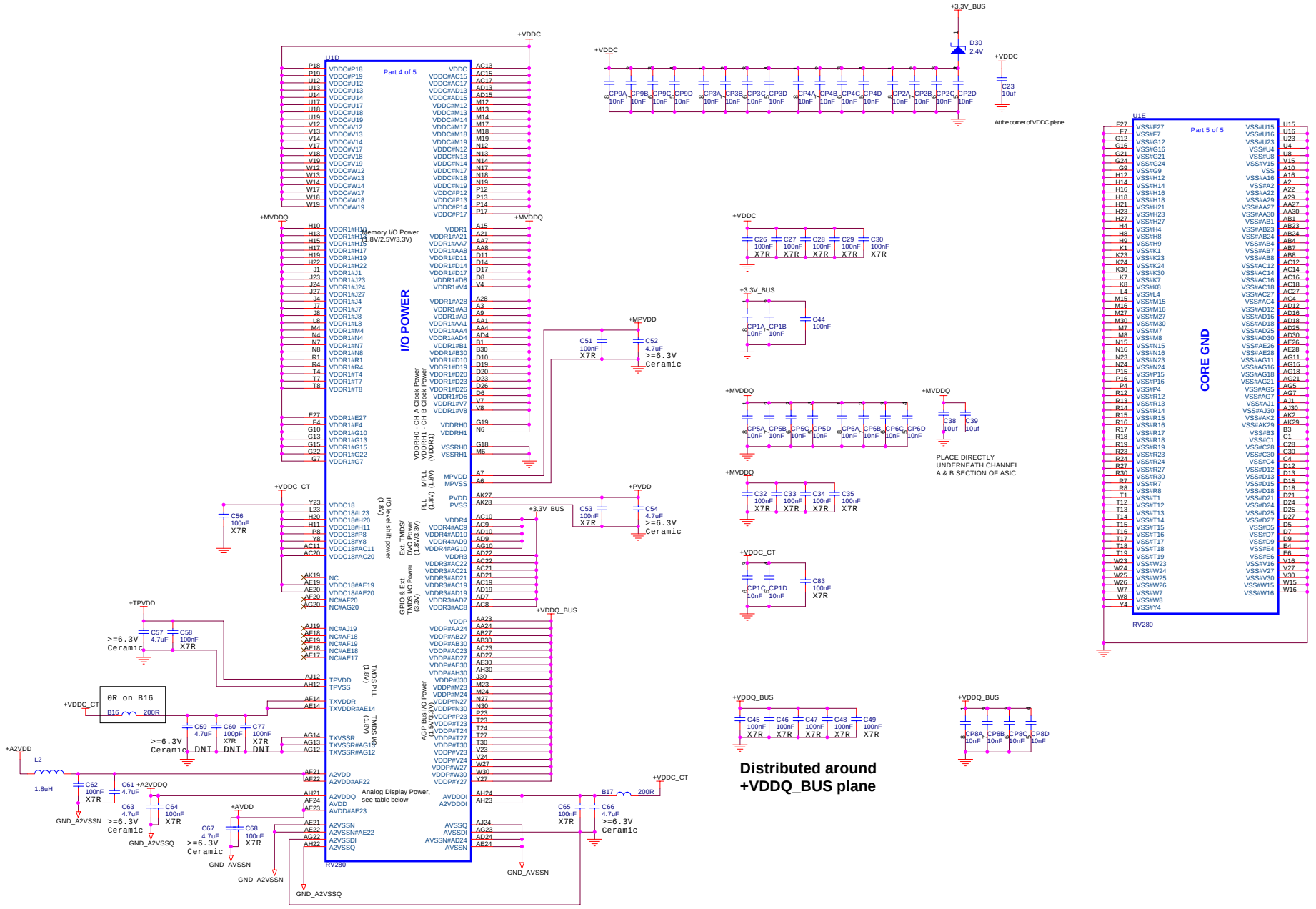

Pin Names	+AVDD	Matching Ground	+A2VDD	Matching Ground	+A2VDDQ	Matching Ground	+AVDDDI +A2VDDDI	Matching Ground
Voltage	1.8V		2.5V		1.8V		1.8V	
Usage	DAC1 VDD (80mA) DAC1 Band Gap Ref.	AVSSN (Noisy) AVSSQ (Quiet)	DAC2 VDD (120mA)	A2VSSN (Noisy)	DAC2 Band Gap Ref.	A2VSSQ (Quiet)	Digital Power for DAC1 and DAC2	AVSSDI A2VSSDI (Digital)
Board power and ground option(s)	AVDD sourced from VDDC_CT thru bead at least 15 mil trace and not longer than 1.5 inch. AVSSN and AVSSQ with single via to GND close to the pin.		(1) A2VDD regulated source and A2VSSN return path routed with at least 15 mil trace and not longer than 1.5 inch. AVSSN with single via to GND at the regulator. (2) Sourced from VDD thru bead instead of the regulator		Source from AVDD thru bead. A2VSSQ with sigle via to GND close to the pin.		Source from VDDC_CT thru bead	

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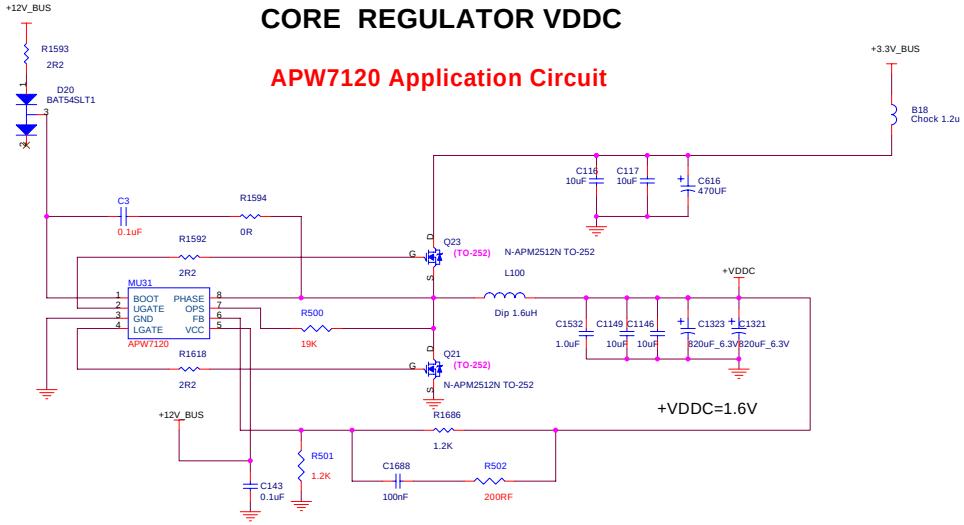
CORE REGULATOR VDDC

APW7120 Application Circuit



VDDC=0.8 * [1+ (R1686 / R501)]

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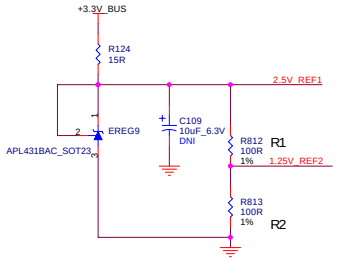
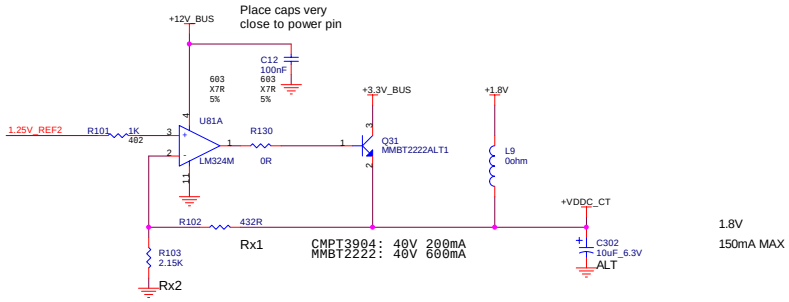
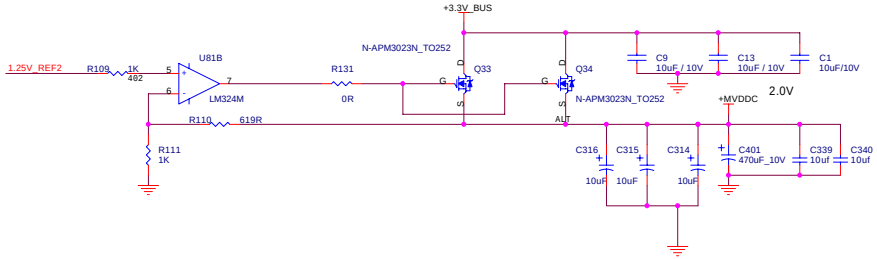
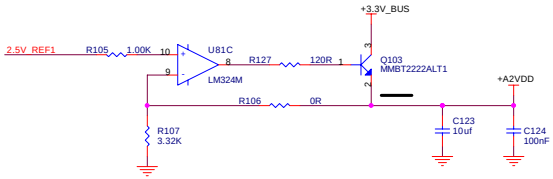
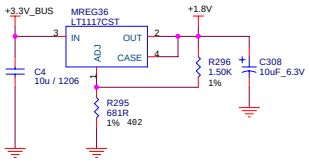


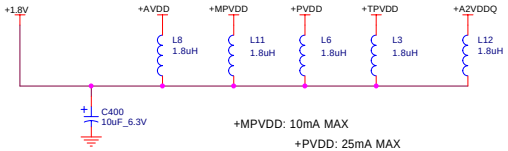






Alt. regulator for +1.8V
Vout = 1.8V
Iout = 500mA MAX





I31-0111719-A35

I31-0111719-N03

I31-0111719-A30

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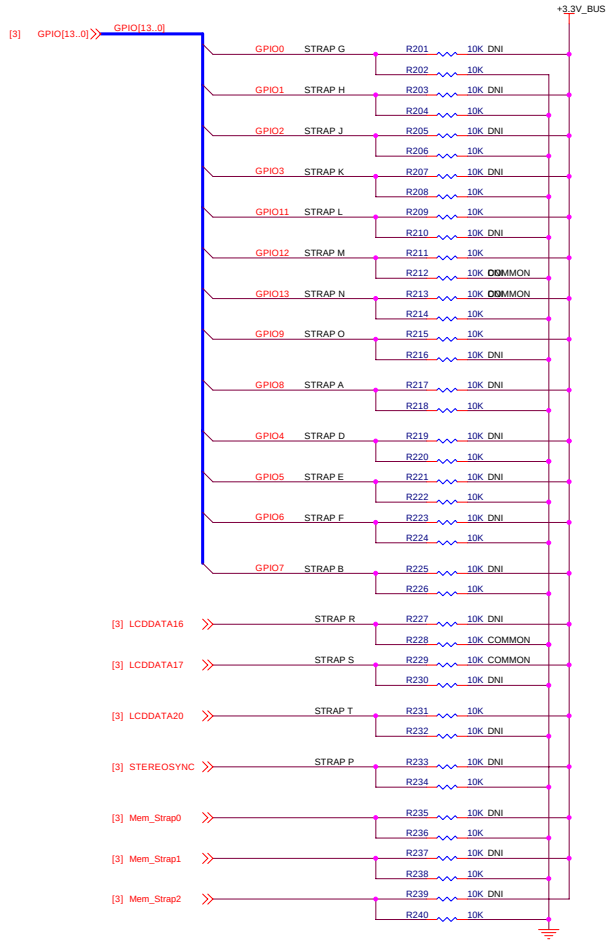
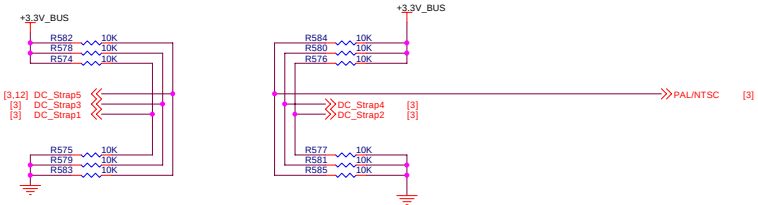


OPTION STRAPS

STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM **1011 - Serial M25P05/10 ROM (ST), chip IDis from ROM** 1100 - Reserved 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1100
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000 (internal pull-down)
VGA_DISABLE	GPIO(7)	**0 - VGA controller capabillity enabled.** 1 - The device will not be recognized as the systemis VGA controller.	0
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select 00 - single function device. 01 - two function device. No AGP in either function **10 - two function device. AGP only in function 0** 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	10
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. **0 - Slave VIP host port devices present** 1 - No slave VIP host port devices reporting presence during reset	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

Daughter Card Straps



STRAPS	PIN	DESCRIPTION
DC_STRAP1	LCDDATA12	Internal TMDS Enabled **0 - Disabled** 1 - Enabled
DC_STRAP2	LCDDATA13	Video Capture Enabled **0 - Disabled** 1 - Enabled
DC_STRAP4 DC_STRAP5	LCDDATA15 LCDDATA19 0 0 0 1 1 0 1 1	DAC2 Configuration DAC2:Off DAC2:On as CRT DAC2:On as TVOUT DAC2:On as TVOUT and CRT
DC_STRAP6	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 -NTSC (on board resistor pull-up)

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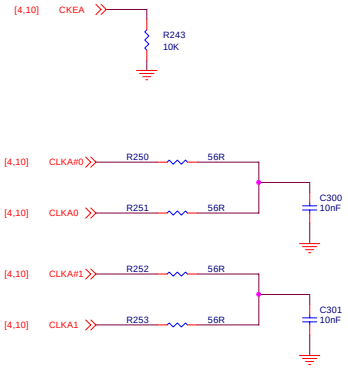

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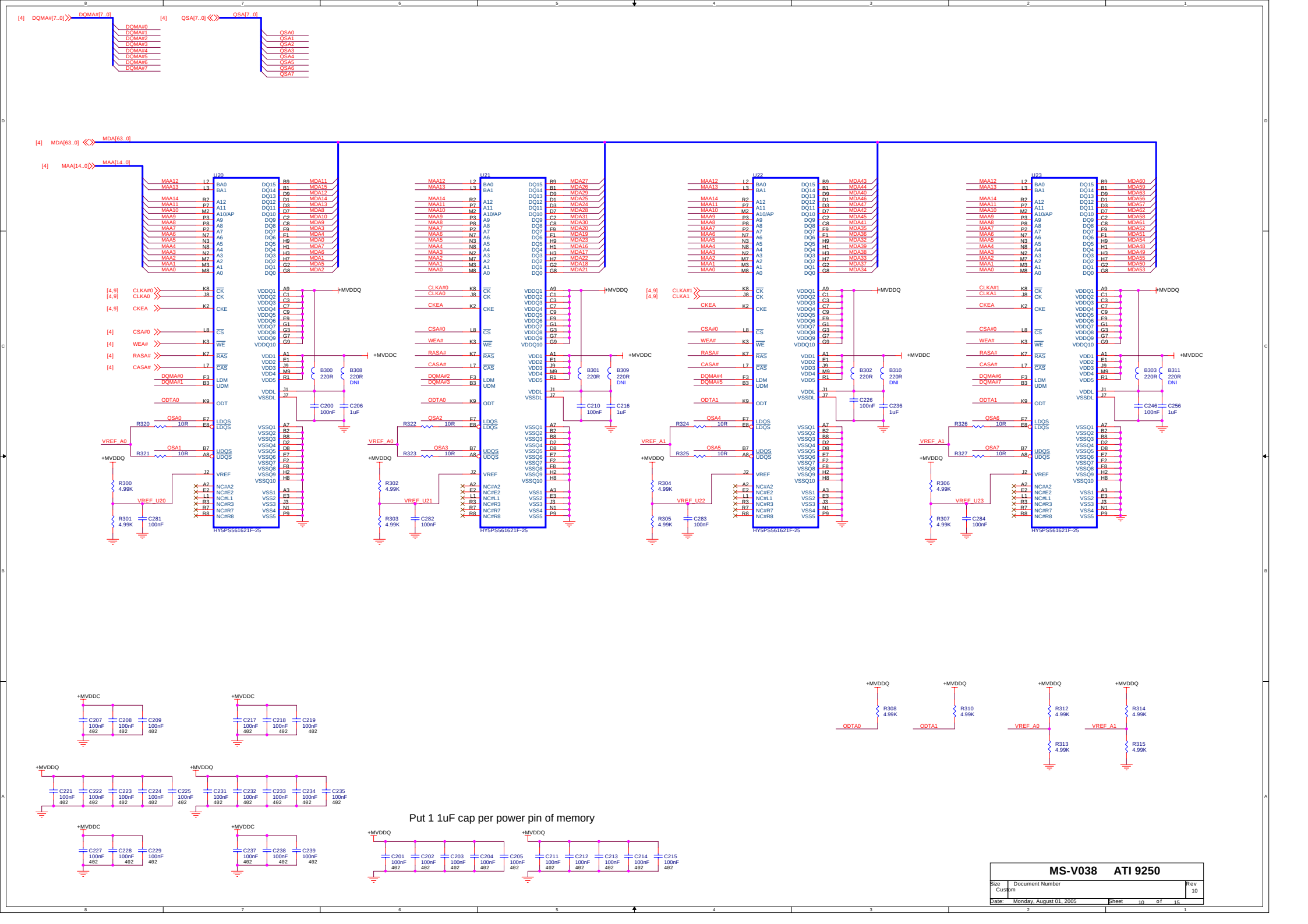
[4] DQMA#[7..0]
DQMA#[7..0]
DQMA#0
DQMA#1
DQMA#2
DQMA#3
DQMA#4
DQMA#5
DQMA#6
DQMA#7
[4] QSA[7..0]
QSA[7..0]
QSA0
QSA1
QSA2
QSA3
QSA4
QSA5
QSA6
QSA7
[4] MDA[63..0]
MDA[63..0]
[4] MAA[14..0]
MAA[14..0]
U20
U21
U22
U23
HY5PS561621F-25
+MVDDQ
+MVDDC
VREF_A0
VREF_A1
VREF_U20
VREF_U21
VREF_U22
VREF_U23
ODTA0
ODTA1
Put 1 1uF cap per power pin of memory
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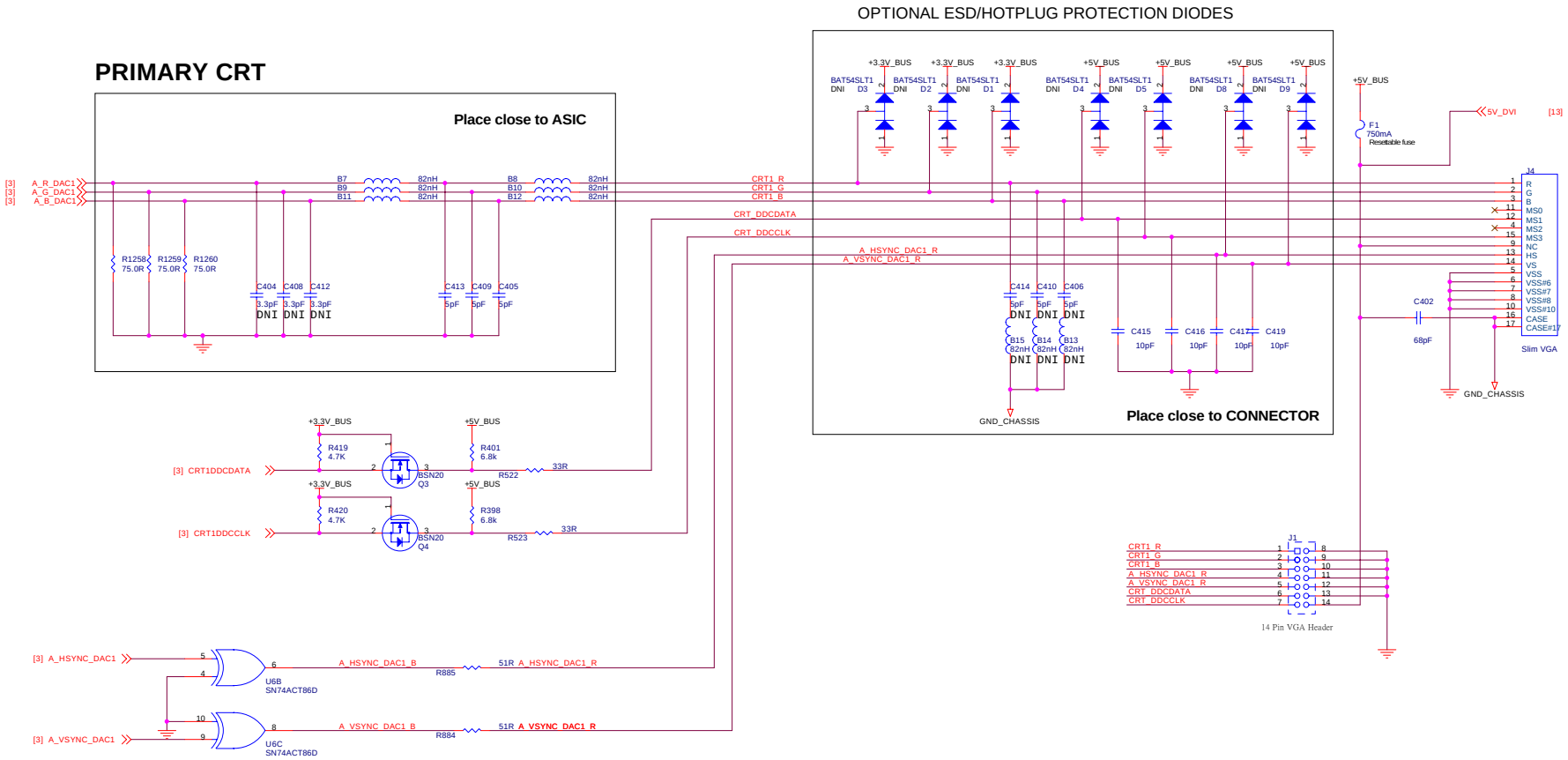

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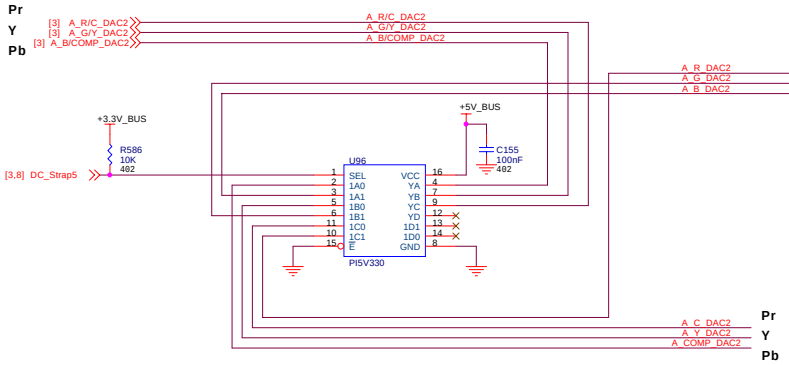
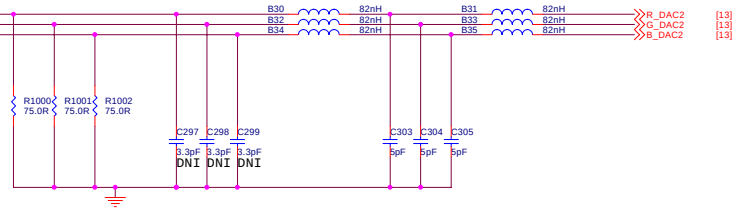
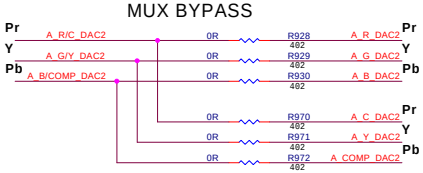
Place close to ASIC



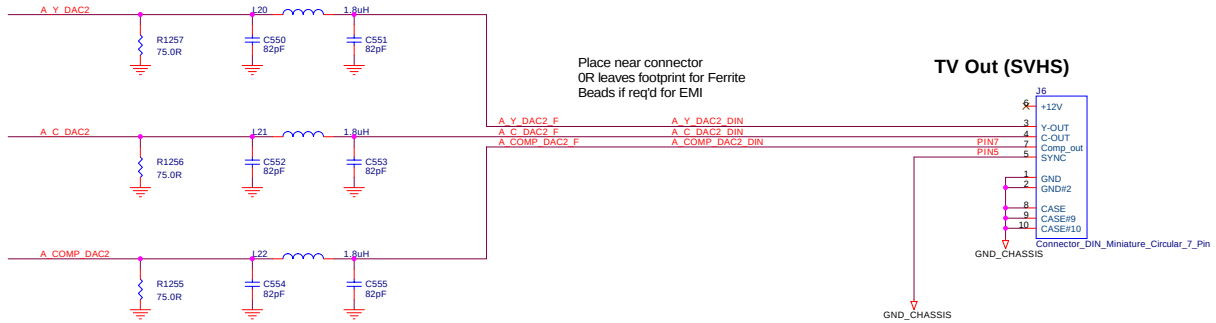
Place close to ASIC



MUX BYPASS



Place Resistors close to ASIC.



Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI

TV Out (SVHS)

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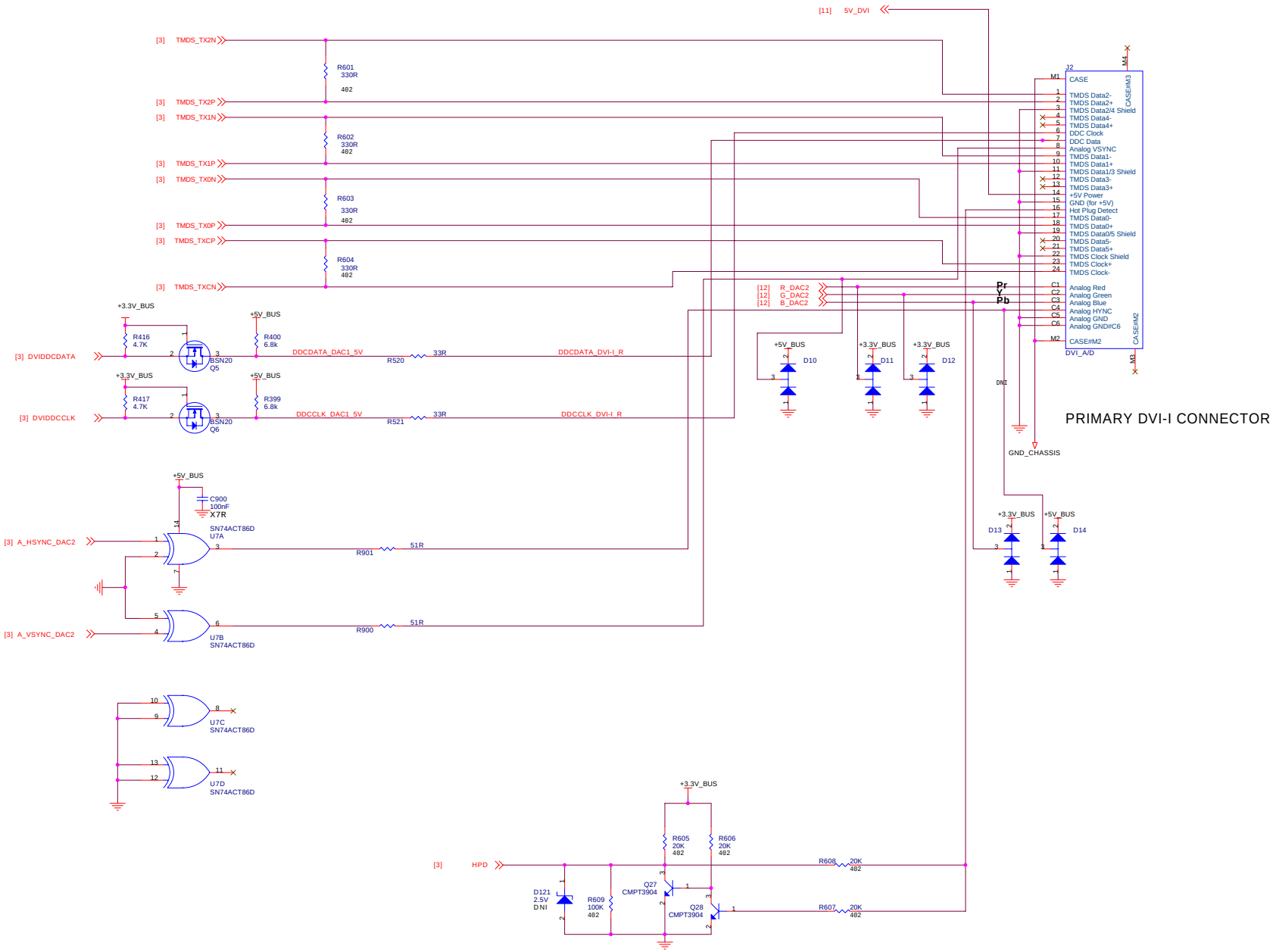

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CRT SCREWS

ASSY1

SCREW
JACKSCREW
ASSY

ASSY2

SCREW
JACKSCREW
ASSY

Heatsink

MH101

HEATSINK

PCB

PCB

PCB

+12V_BUS

B40
Bead

JU1

C901
100nF
0Ω
X7R
5%

Header_1X3

JUI1

MJU1

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM4 SW_FB
FM5 SW_FB
FM6 SW_FB
FM7 SW_FB
FM8 SW_FB

BRACKET

BRACKET

BRACKET

CABLE

D-Sub Cable

D-sub Cable

STD
COMMON SCREW-1
MEC_SCREW

STD
COMMON SCREW-2
MEC_SCREW

STD
COMMON SCREW-3
MEC_SCREW

STD
COMMON SCREW-4
MEC_SCREW

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<Variant Name>

Title	Schematic No.	Date:
RV280 LP AGP8x 128MB 16Mx16 DDR	105-A165XX-00	**Friday, July 29, 2005**

REVISION HISTORY

Rev 10

Sch Rev		Date	REVISION DESCRIPTION
0	00A	03/25/03	Based on 105-A062xx-00 schematic (pg2) Add pull-up on CS# for flashrom (pg5) Replace swiching VDDC regulator with Op-Amp regulator circuit (pg5) Add Op-Amp regulator circuit for low-cost design (pg6) Add Op-Amp regulator circuit for low-cost design (pg6) Remove C317 Thru-hole Alum. Cap for MVDDC (pg6) Add +3.3V_BUS directly to +MVDDC option (pg11) Modify VO connector filter chassis ground connections
		04/01/03	(pg5) Replace VDDC 470uF with thru-hole (pg6) Add thru-hole 470uF on +MVDDC for option
		04/10/03	(pg6) Remove C1, C17 and C1034
1	00B	05/14/03	(pg5) Remove Q811 and Q814 (pg6) Add C805 10uF tant. cap on +MPVDD (pg6) Add R112 to bypass opamp for +MVDDC (pg6) Remove diodes (D10 and D11) and resistors (R111, R1261, R1262, R1263 and R1264) for +MVDDC (pg5, 6) Add R104 to drive +MVDDC from alternate shunt reference (pg7) Add jumper J1 for PAL TVO default (Layout) Add silscreen for switch and jumper (Layout) Correct MiniDIN J6 footprint (Layout) Correct diode clearance for manufacturing request (Layout) Move sticker location
2	00	05/30/03	(pg9) Replace a 2-pin with a 3-pin jumper for NTSC/PAL section. (pg5) Add R812, R813 and R815 for +MVDDC voltage adjustment (Layout) Change footprint of P/N4238010600
3	0A	07/15/05	Redesign form 8999-1A schematic