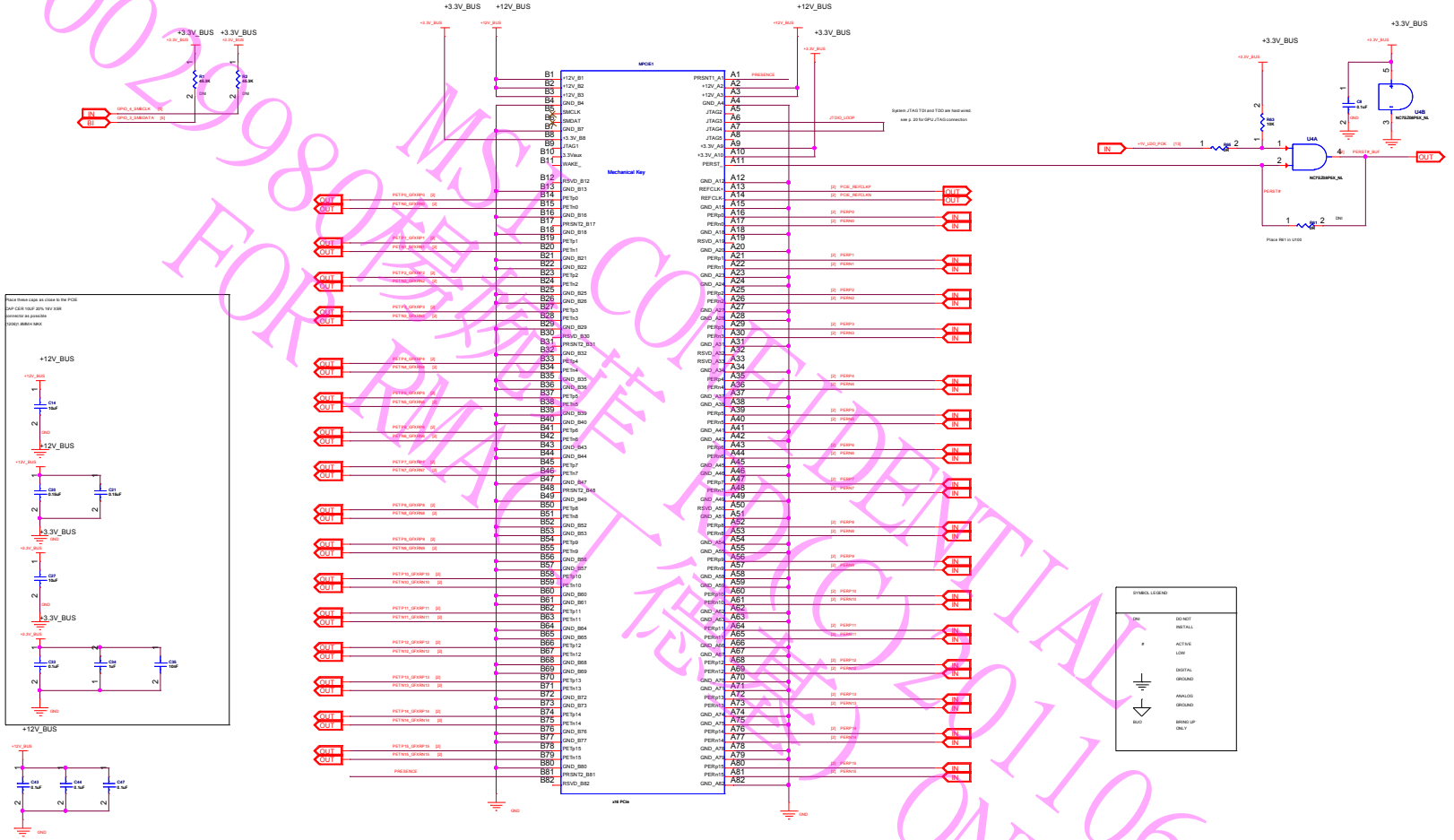
PCI-EXPRESS EDGE CONNECTOR



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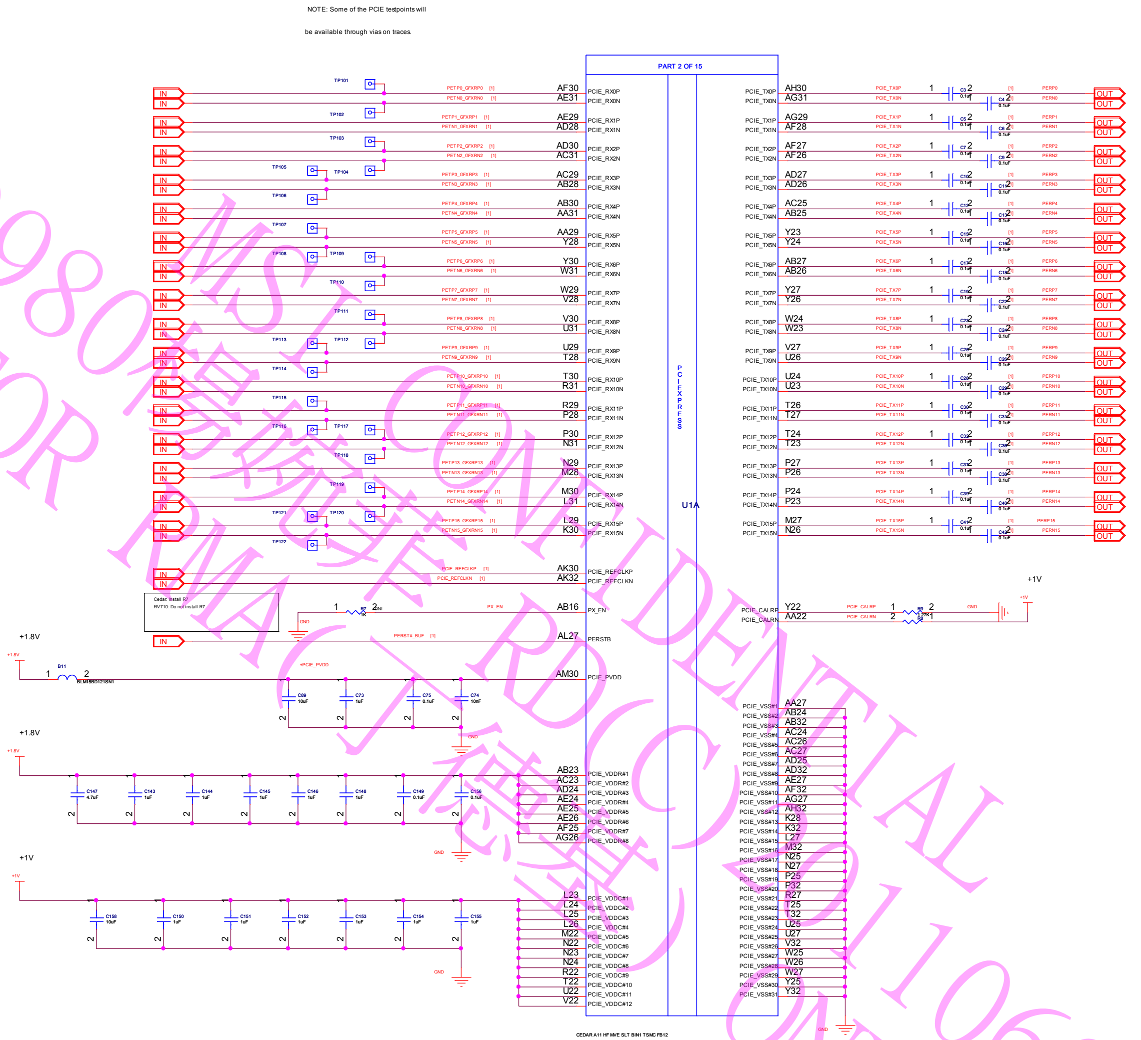
Date: Friday, May 20, 2011	Rev P00
Sheet 1 of 18	
Title PCI-E Edge Connector	Doc No. 105-C2800008A

CAICOS/CEDAR PCIe Interface



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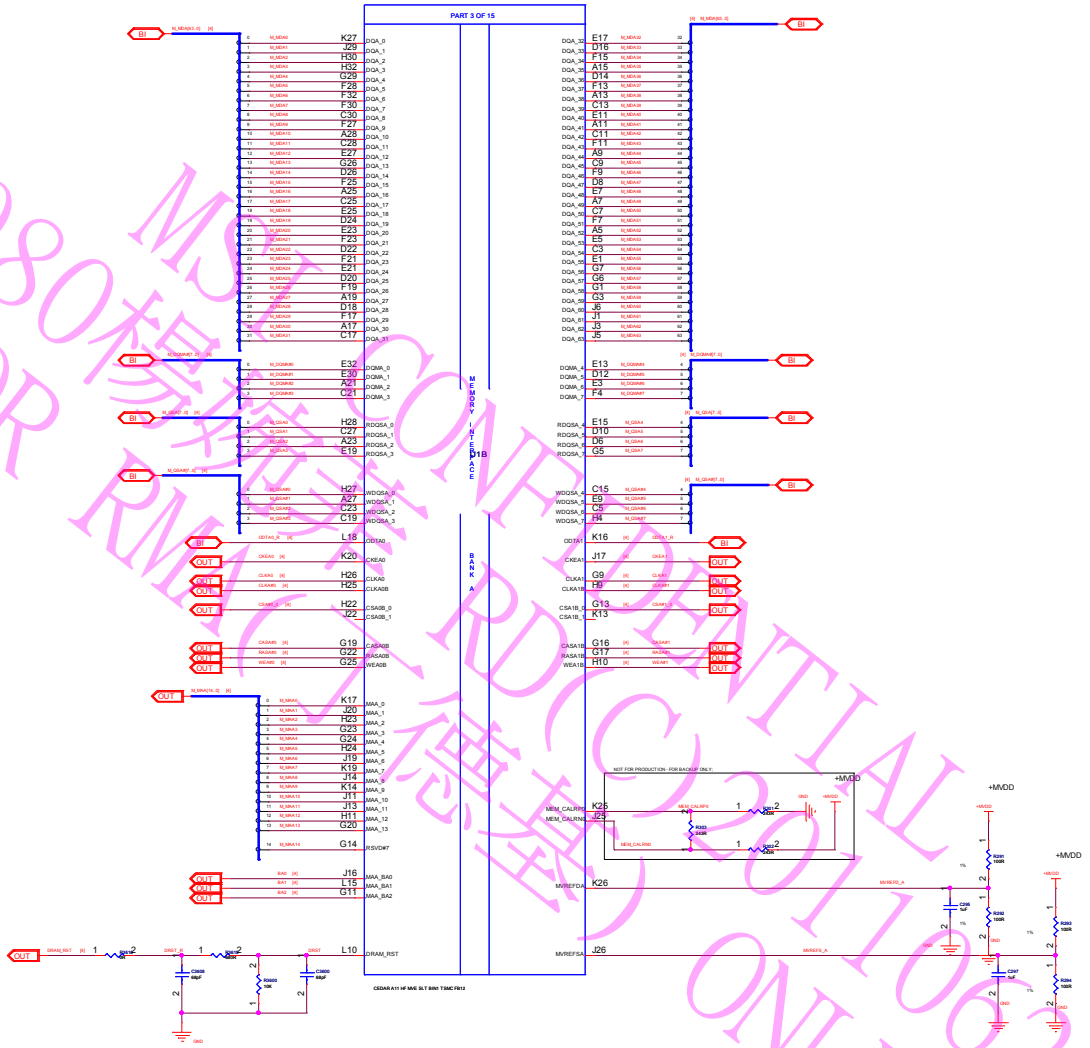
Date: Friday, May 20, 2011	Rev P00
Sheet 2 of 18	
Title HP CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA CAICOS PCIE Interface	Doc No. 105-C264XX-00A



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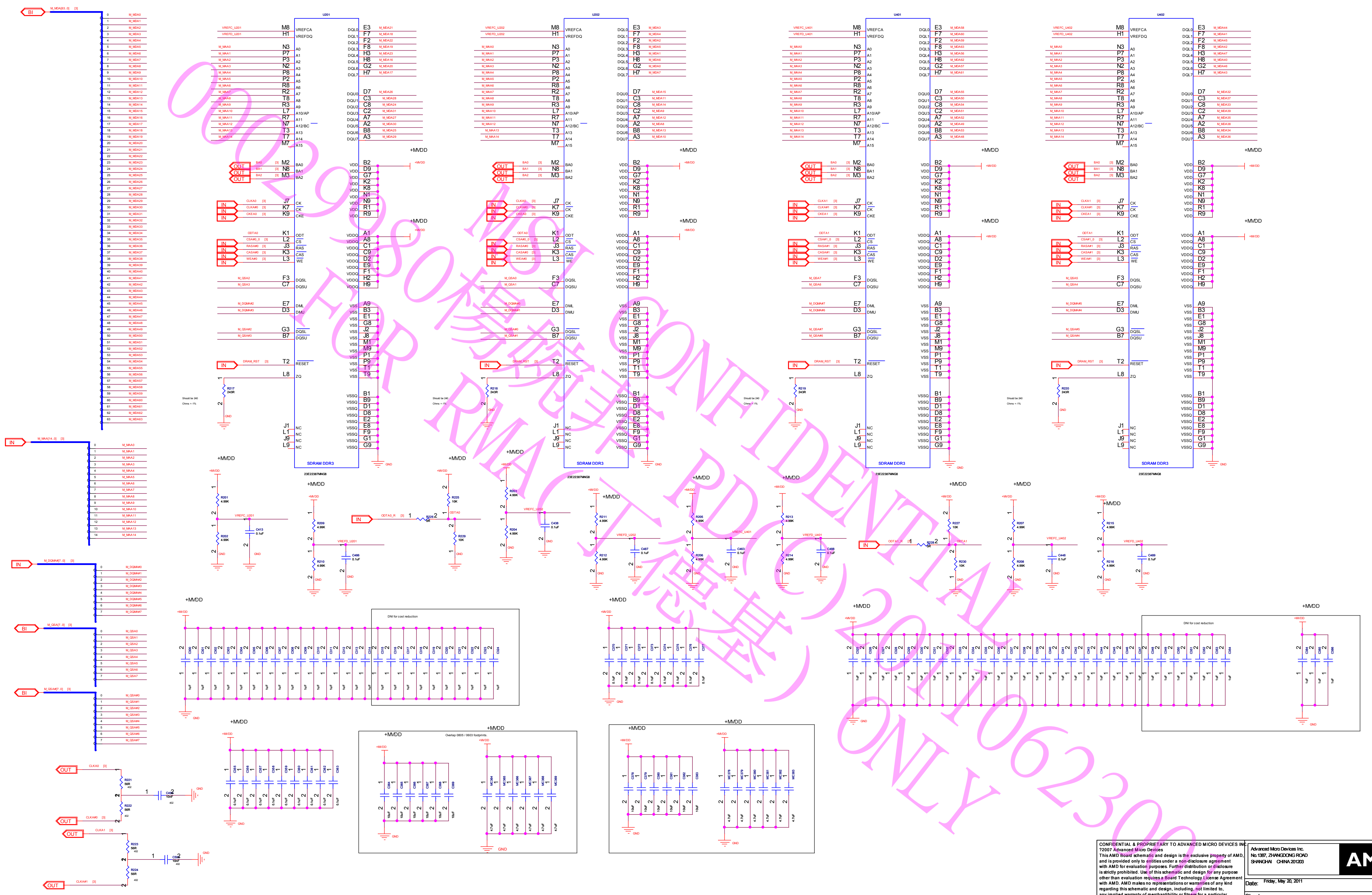
Date:	Friday, May 20, 2011
Rev	P00
Sheet	3 of 18
Title	CACOS MEM I/F CHA
Doc No.	105-C26000-00A

CHANNEL A: 256MB/512MB DDR3



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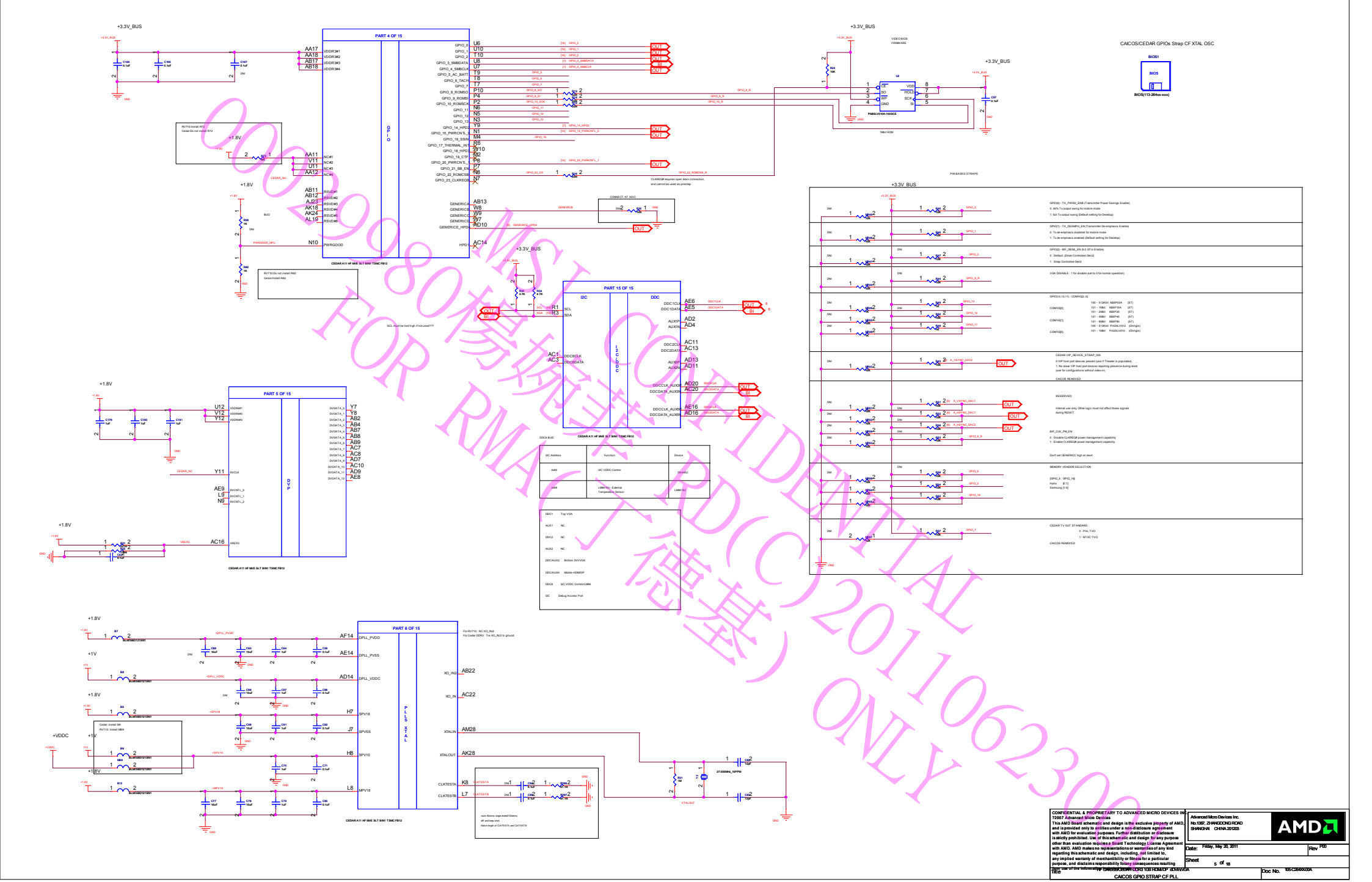
Date: Friday, May 20, 2011	Rev P00
Sheet 4 of 18	
Title PF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA DDR3 CHA	Doc No. 105-C264XX-00A



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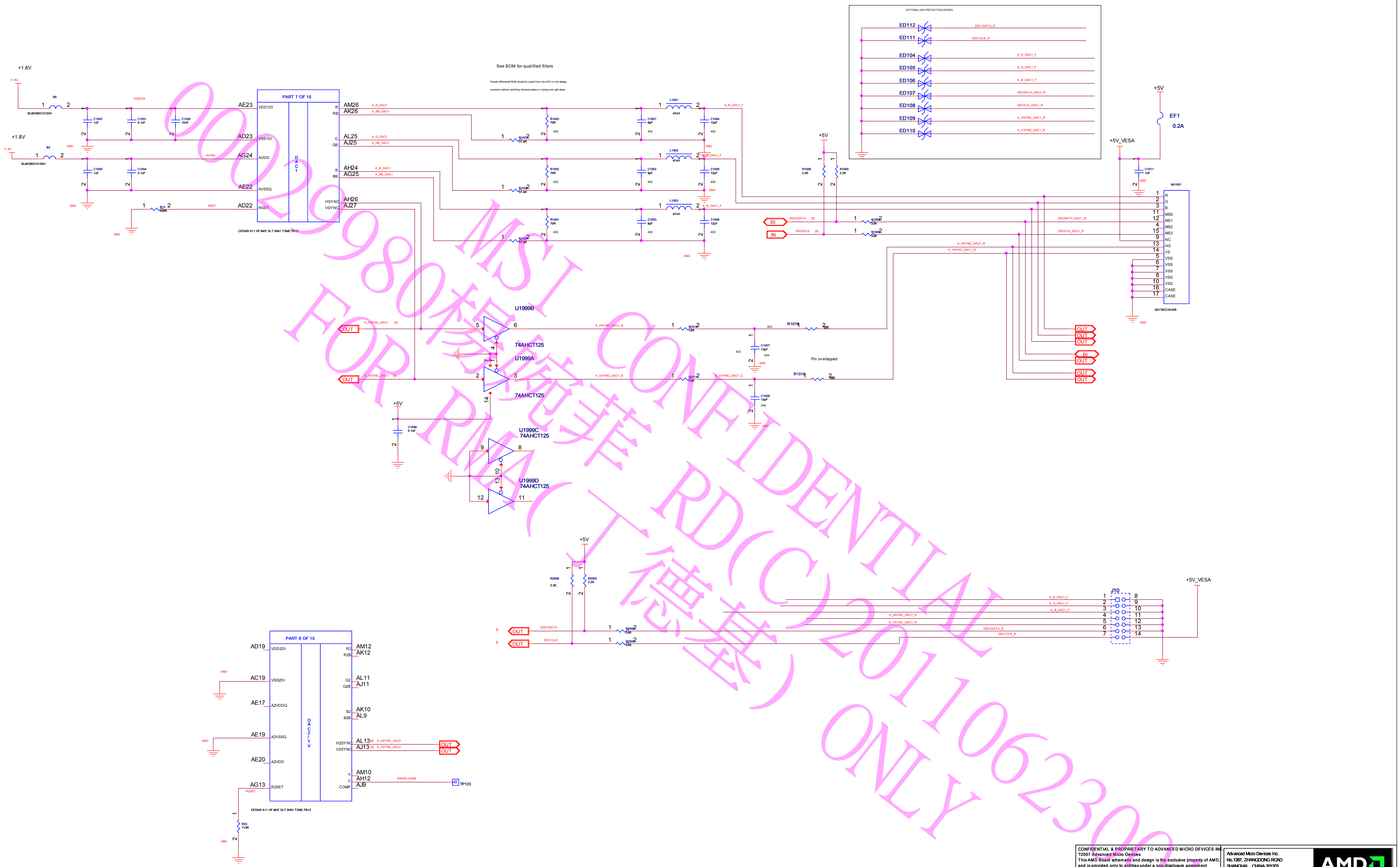
Date:	Friday, May 20, 2011
Rev	P00
Sheet	5 of 18
Title	CAICOS GPIO STRAP CF PLL
Doc No.	105-C26000-00A



See BOM for qualified filters
OPTIONAL ESD PROTECTION DIODES
+1.8V
+5V
+5V_VESA
PART 7 OF 15
DAC1
CEDAR A11 HF M/E SLT BIN1 TSMC FB12
AE23 VDD1DI
AD23 VSS1DI
AG24 AVDD
AE22 AVSSQ
AD22 RSET
AM26 R
AK26 RB
AL25 G
AJ25 GB
AH24 B
AG25 BB
AH26 HSYNC
AJ27 VSYNC
ED112
ED111
ED104
ED105
ED106
ED107
ED108
ED109
ED110
EF1
0.2A
U1999B
74AHCT125
U1999A
74AHCT125
U1999C
74AHCT125
U1999D
74AHCT125
Pin overlapped
J10
PART 8 OF 15
DAC2/TV
CEDAR A11 HF M/E SLT BIN1 TSMC FB12
AD19 VDD2DI
AC19 VSS2DI
AE17 A2VDDQ
AE19 A2VSSQ
AE20 A2VDD
AG13 R2SET
AM12 R2
AK12 R2B
AL11 G2
AJ11 G2B
AK10 B2
AL9 B2B
AL13 H2SYNC
AJ13 V2SYNC
AM10 Y
AH12 C
AJ9 COMP
TP123

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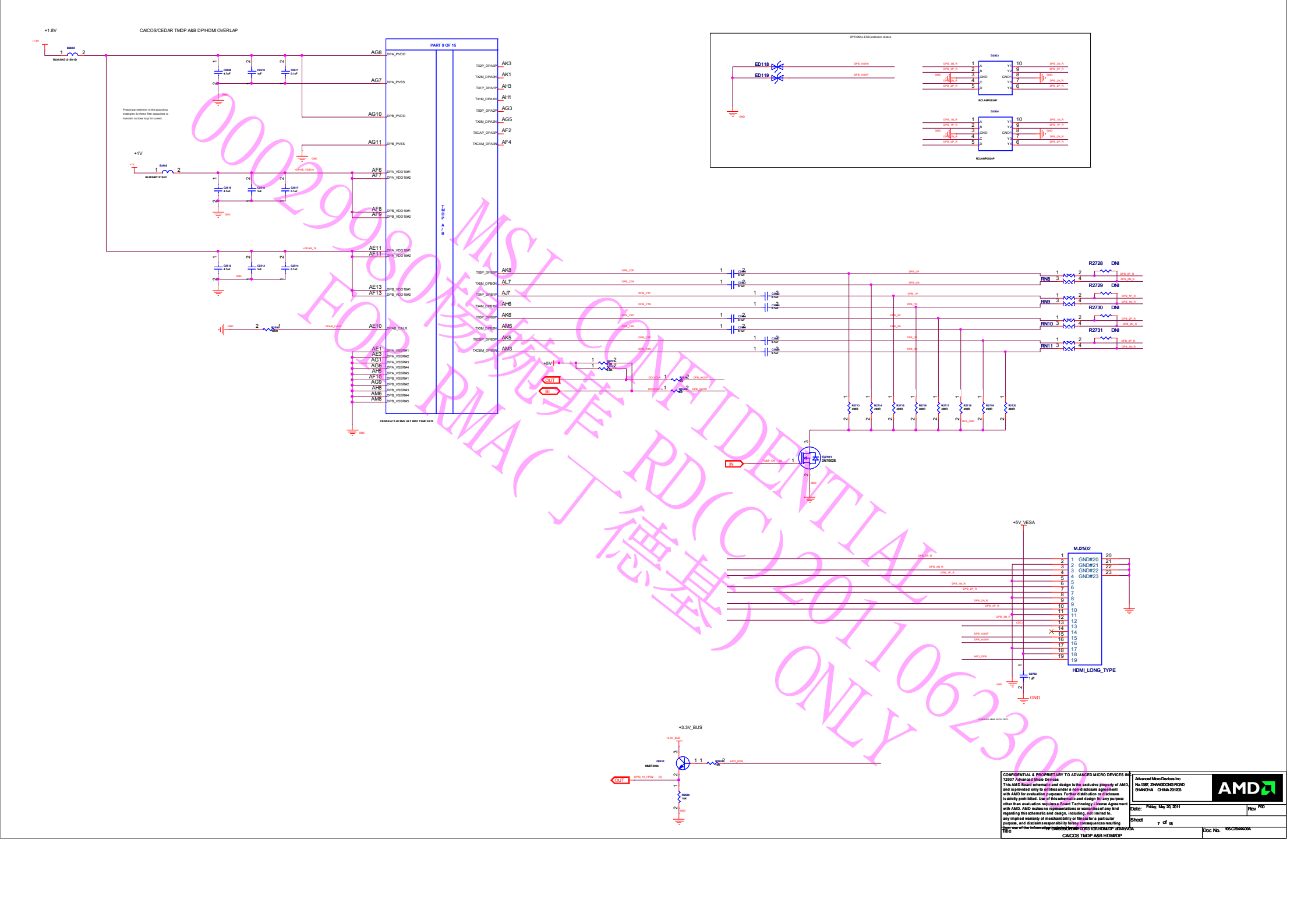
Date: Friday, May 20, 2011
Rev P00
Sheet 6 of 18
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA
CAICOS DAC
Doc No. 105-C264XX-00A



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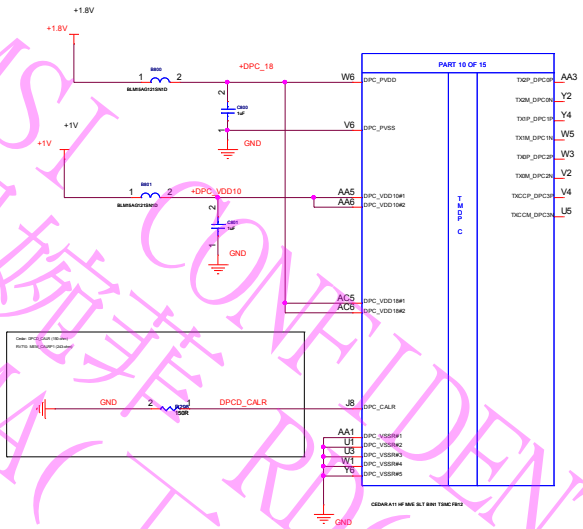
SHANGHAI CHINA 201203

Date: Friday, May 20, 2011
Rev: P00
Sheet: 7 of 18
Title: CAICOS TMDP A&B HDMI/DP
Doc No.: 105-C26000-00A

CAICOS/CEDAR Display Port C (Unused)



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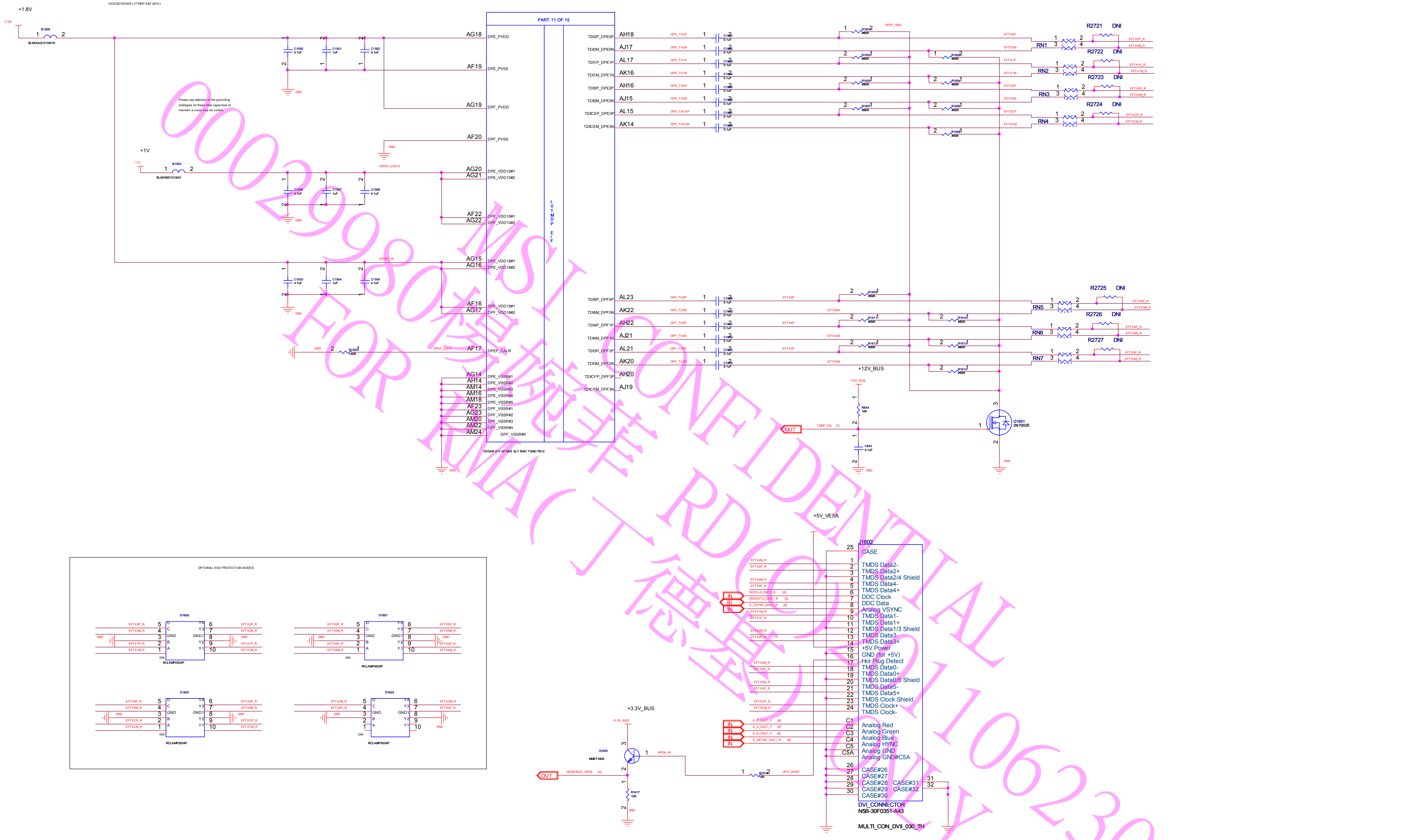
Date: Friday, May 20, 2011	Rev P00
Sheet 8 of 18	
Title CAICOS TMDP C (UNUSED)	Doc No. 105-C26000-00A


CAICOS/CEDAR LVTMDP E&F dDVI-I
+1.8V
B1500
BLM15AG121SN1D
C1500 4.7uF
C1501 1uF
C1502 0.1uF
GND
Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.
+1V
B1502
BLM15BD121SN1
C1506 4.7uF
C1507 1uF
C1508 0.1uF
C1503 4.7uF
C1504 1uF
C1505 0.1uF
PART 11 OF 15
AG18 DPE_PVDD
AF19 DPE_PVSS
AG19 DPF_PVDD
AF20 DPF_PVSS
AG20 DPE_VDD10#1
AG21 DPE_VDD10#2
AF22 DPF_VDD10#1
AG22 DPF_VDD10#2
AG15 DPE_VDD18#1
AG16 DPE_VDD18#2
AF16 DPF_VDD18#1
AG17 DPF_VDD18#2
AF17 DPEF_CALR
R1500 150R
AG14 DPE_VSSR#1
AH14 DPE_VSSR#2
AM14 DPE_VSSR#3
AM16 DPE_VSSR#4
AM18 DPE_VSSR#5
AF23 DPF_VSSR#1
AG23 DPF_VSSR#2
AM20 DPF_VSSR#3
AM22 DPF_VSSR#4
AM24 DPF_VSSR#5
LVTMDP E/F
CEDAR A11 HF M/E SLT BIN1 TSMC FB12
T2X2P_DPE0P AH18
T2X2M_DPE0N AJ17
T2X1P_DPE1P AL17
T2X1M_DPE1N AK16
T2X0P_DPE2P AH16
T2X0M_DPE2N AJ15
T2XCEP_DPE3P AL15
T2XCEM_DPE3N AK14
T2X5P_DPF0P AL23
T2X5M_DPF0N AK22
T2X4P_DPF1P AH22
T2X4M_DPF1N AJ21
T2X3P_DPF2P AL21
T2X3M_DPF2N AK20
T2XCFP_DPF3P AH20
T2XCFM_DPF3N AJ19
0.1uF
499R
RN1 RN2 RN3 RN4 RN5 RN6 RN7
R2721 DNI
R2722 DNI
R2723 DNI
R2724 DNI
R2725 DNI
R2726 DNI
R2727 DNI
EFTX2P_R EFTX2M_R EFTX1P_R EFTX1M_R EFTX0P_R EFTX0M_R EFTXCP_R EFTXCM_R
EFTX5P_R EFTX5M_R EFTX4P_R EFTX4M_R EFTX3P_R EFTX3M_R
+12V_BUS
R844 10K
C843 0.1uF
OUT
TMDP_EN
Q1601 2N7002E
OPTIONAL ESD PROTECTION DIODES
D1600 D1601 D1602 D1603
RCLAMP0524P
DNI
+5V_VESA
J1602
CASE
TMDS Data2-
TMDS Data2+
TMDS Data2/4 Shield
TMDS Data4-
TMDS Data4+
DDC Clock
DDC Data
Analog VSYNC
TMDS Data1-
TMDS Data1+
TMDS Data1/3 Shield
TMDS Data3-
TMDS Data3+
+5V Power
GND (for +5V)
Hot Plug Detect
TMDS Data0-
TMDS Data0+
TMDS Data0/5 Shield
TMDS Data5-
TMDS Data5+
TMDS Clock Shield
TMDS Clock+
TMDS Clock-
Analog Red
Analog Green
Analog Blue
Analog HYNC
Analog GND
Analog GND#C5A
CASE#26
CASE#27
CASE#28 CASE#31
CASE#29 CASE#32
CASE#30
DVI_CONNECTOR
N5B-30F0351-A43
MULTI_CON_DVII_030_TH
+3.3V_BUS
Q1602
MMBT3904
GENERICE_HPD4
HPD4_IN
HPD_DVIEF
R1617 10K
IN
BI

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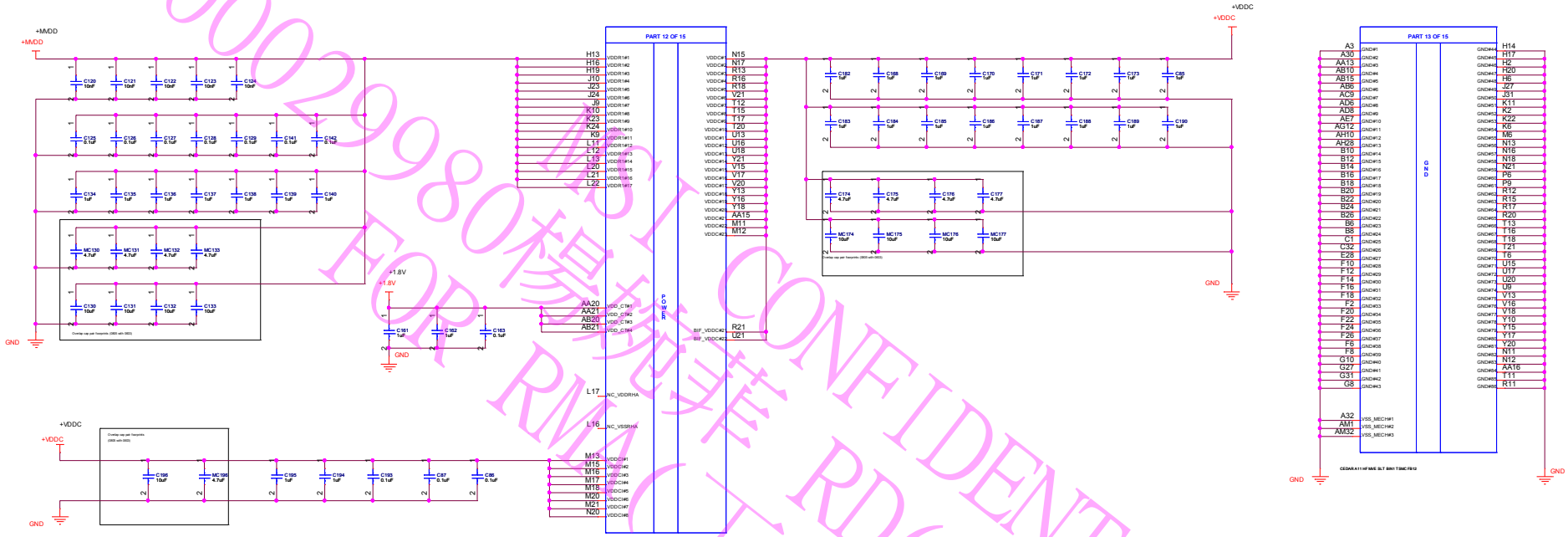
Sheet 9 of 18
Title CAICOS LVTMDP E&F dDVI-I
Doc No. 105-C264XX-00A

CAICOS/CEDAR Power & GND



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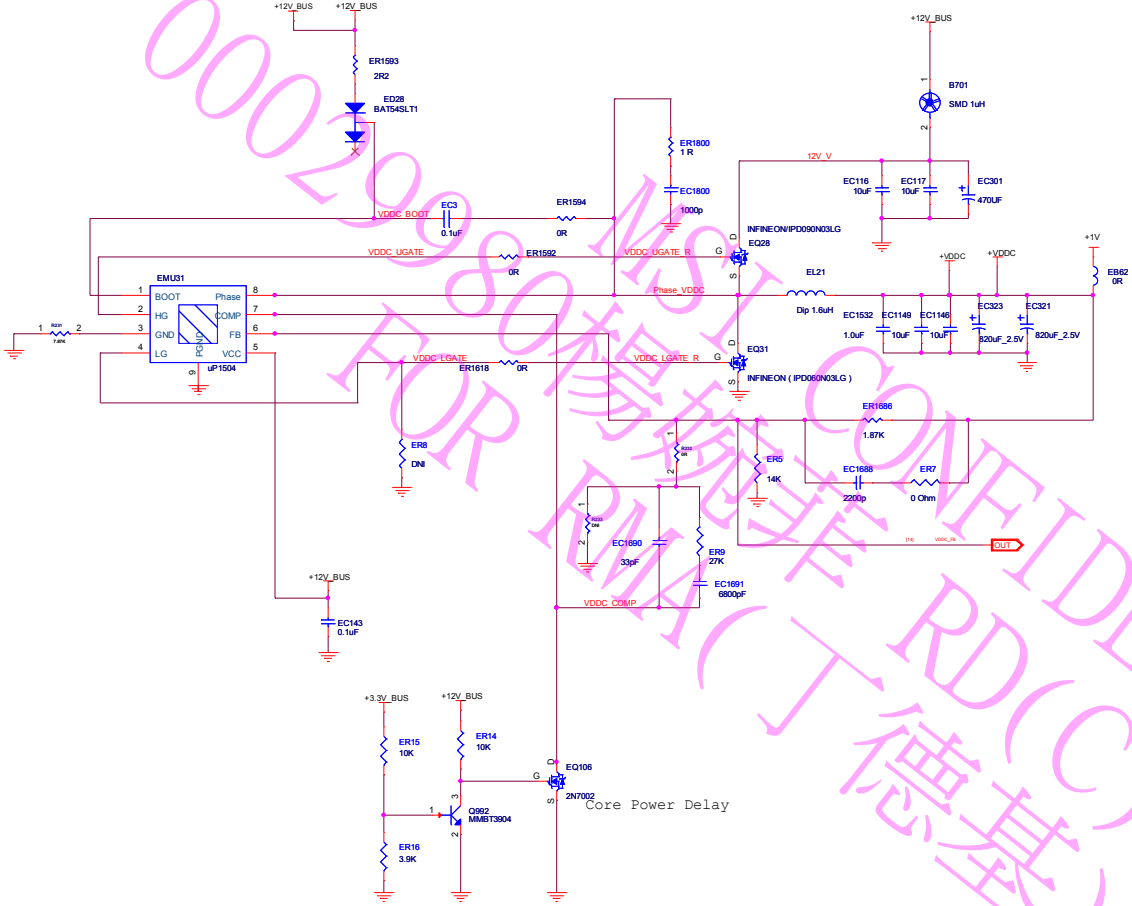
Date:	Friday, May 20, 2011
Rev	P00
Sheet	10 of 18
Title	CAICOS POWER&GND
Doc No.	105-C26900(0)A



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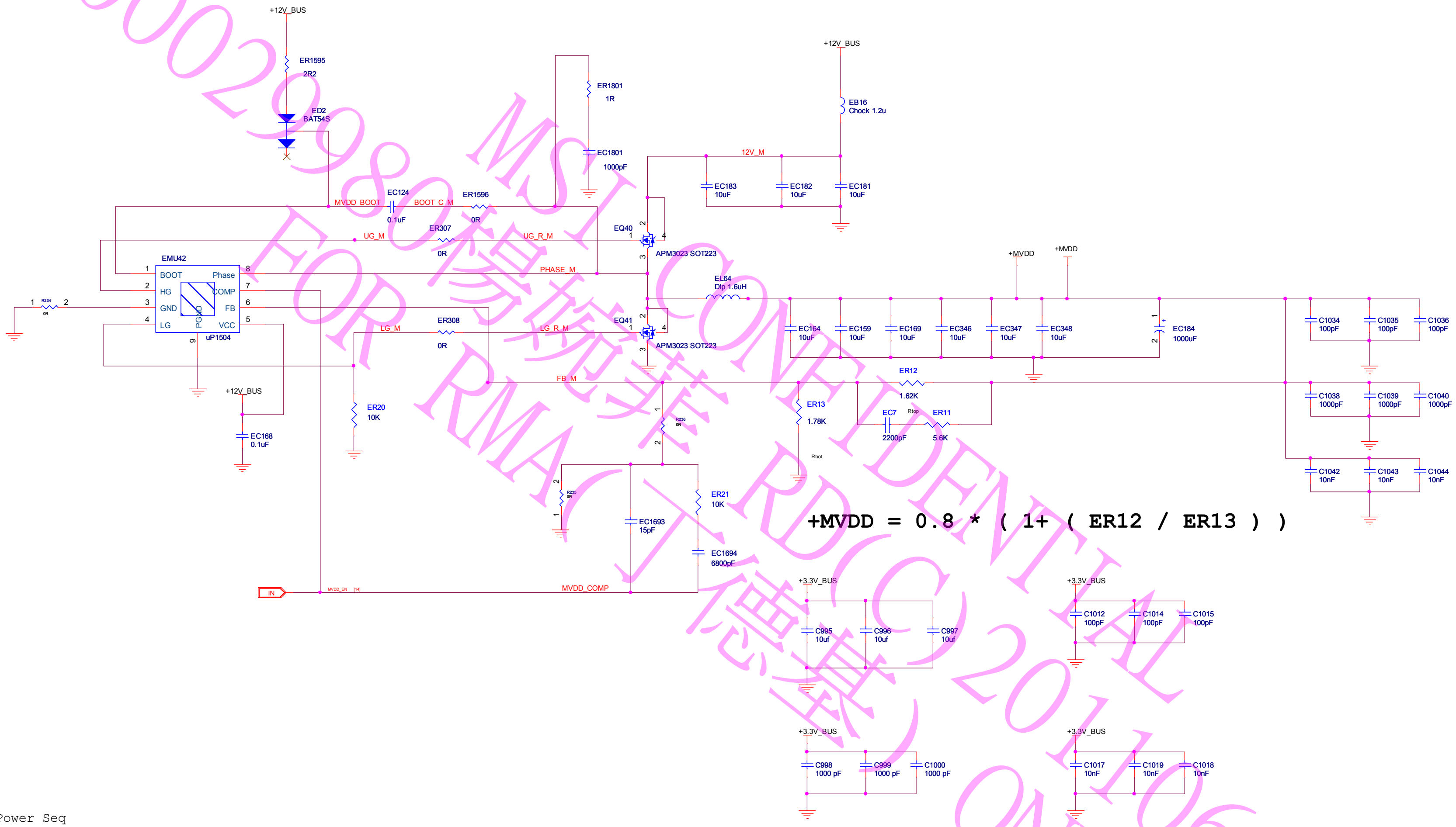
SHANGHAI CHINA 201203

Date: Friday, May 20, 2011	Rev P00
Sheet 11 of 18	
Title VDDC	Doc No. 105-C26000-00A


+12V_BUS
ER1595
2R2
ED2
BAT54S
ER1801
1R
EC1801
1000pF
+12V_BUS
EB16
Chock 1.2u
12V_M
EC183
10uF
EC182
10uF
EC181
10uF
MVDD_BOOT
EC124
0.1uF
BOOT_C_M
ER1596
0R
EQ40
UG_M
ER307
0R
UG_R_M
APM3023 SOT223
EMU42
BOOT
Phase
HG
COMP
GND
FB
LG
VCC
PGND
uP1504
PHASE_M
+MVDD
+MVDD
EL64
Dip 1.6uH
EC164
10uF
EC159
10uF
EC169
10uF
EC346
10uF
EC347
10uF
EC348
10uF
EC184
1000uF
C1034
100pF
C1035
100pF
C1036
100pF
R234
0R
ER308
0R
LG_M
LG_R_M
EQ41
APM3023 SOT223
+12V_BUS
EC168
0.1uF
ER20
10K
FB_M
ER12
1.62K
ER13
1.78K
Rbot
EC7
2200pF
Rtop
ER11
5.6K
C1038
1000pF
C1039
1000pF
C1040
1000pF
C1042
10nF
C1043
10nF
C1044
10nF
ER21
10K
EC1693
15pF
EC1694
6800pF
IN
MVDD_EN
MVDD_COMP
+3.3V_BUS
C995
10uf
C996
10uf
C997
10uf
+3.3V_BUS
C1012
100pF
C1014
100pF
C1015
100pF
+3.3V_BUS
C998
1000 pF
C999
1000 pF
C1000
1000 pF
+3.3V_BUS
C1017
10nF
C1019
10nF
C1018
10nF

+MVDD = 0.8 * (1+ (ER12 / ER13))

Memory Power Seq

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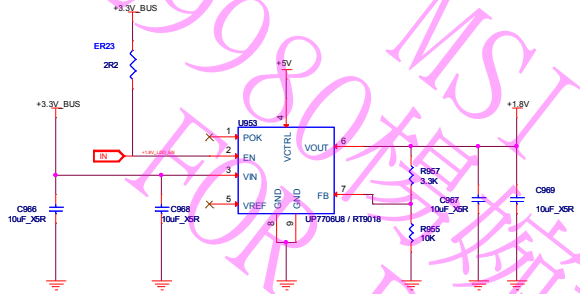
Date: Friday, May 20, 2011 | Rev P00
Sheet 12 of 18
Title: MVDD
Doc No. 105-C264XX-00A

Linear Regulators

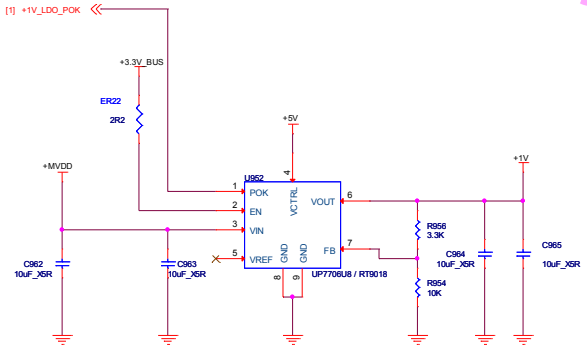
LDO #1:	Vin = 3.00V to 3.60V (3.3V +/-.5%)	Vout = +1.8V +/- 2%;	Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling			



Vout=0.8V * (1+ R957 / R955)

1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

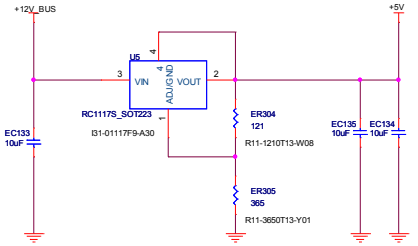
LDO #2:	Vin = +1.32V to 1.84VMAX	Vout = +1.01V +/- 2%	Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling			



Vout=0.8V * (1+ R956 / R954)

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1380mA

Regulators for +5V, +5V_VESA and +5V_VESA2



Vout=1.25V* [1+(ER305/ER304)]

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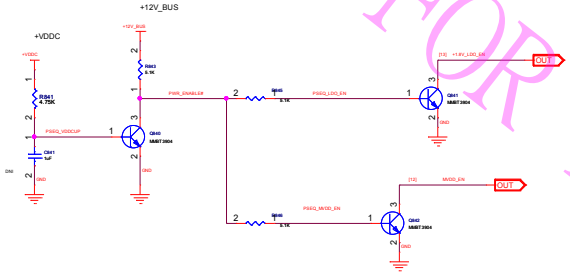
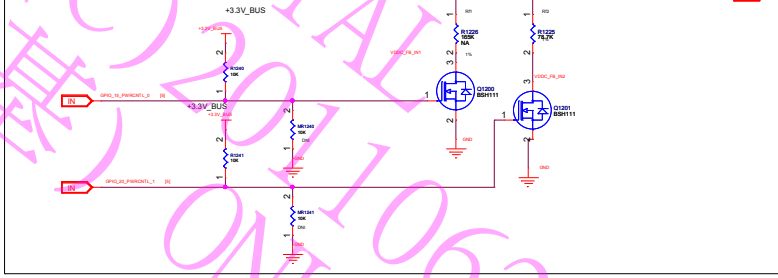
Date:	Friday, May 20, 2011	Rev	P00
Sheet	13 of 18		
Title	LINEAR REGULATORS	Doc No.	105-C26000-00A

POWER SEQUENCING CIRCUIT



VDDC Low Side Divider



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SHANGHAI CHINA 201203

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Date: Friday, May 20, 2011 | Rev P00

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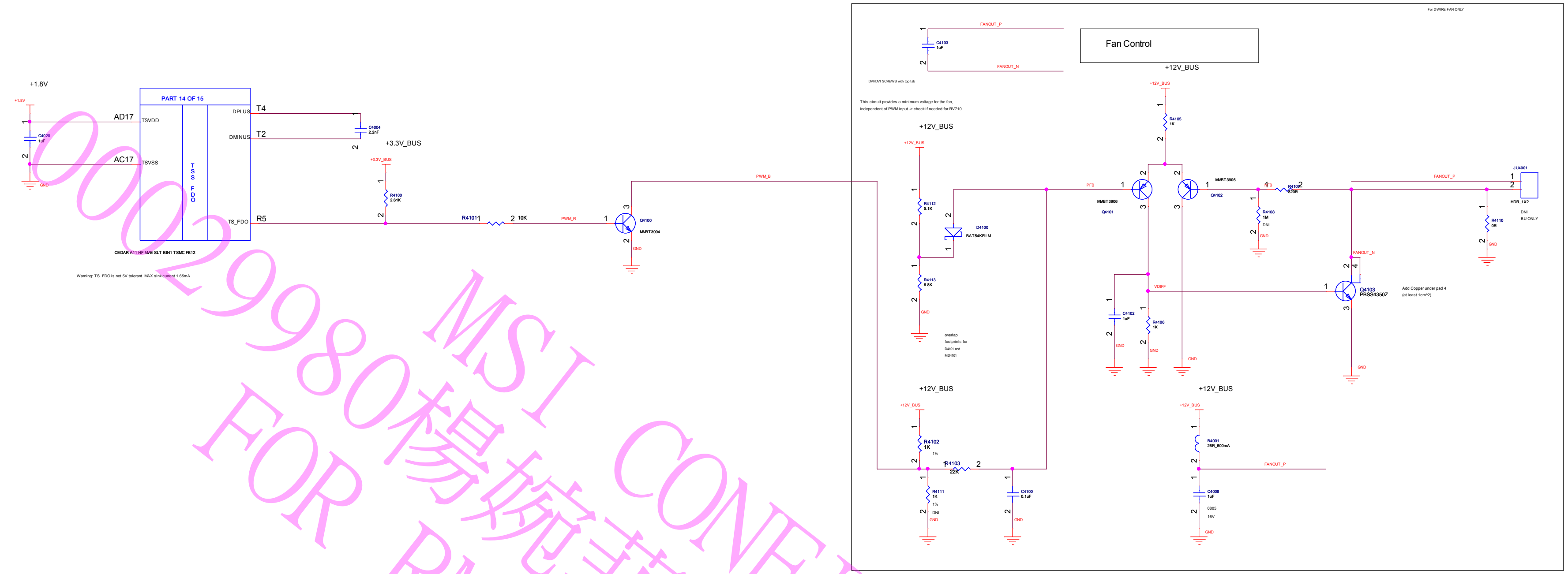
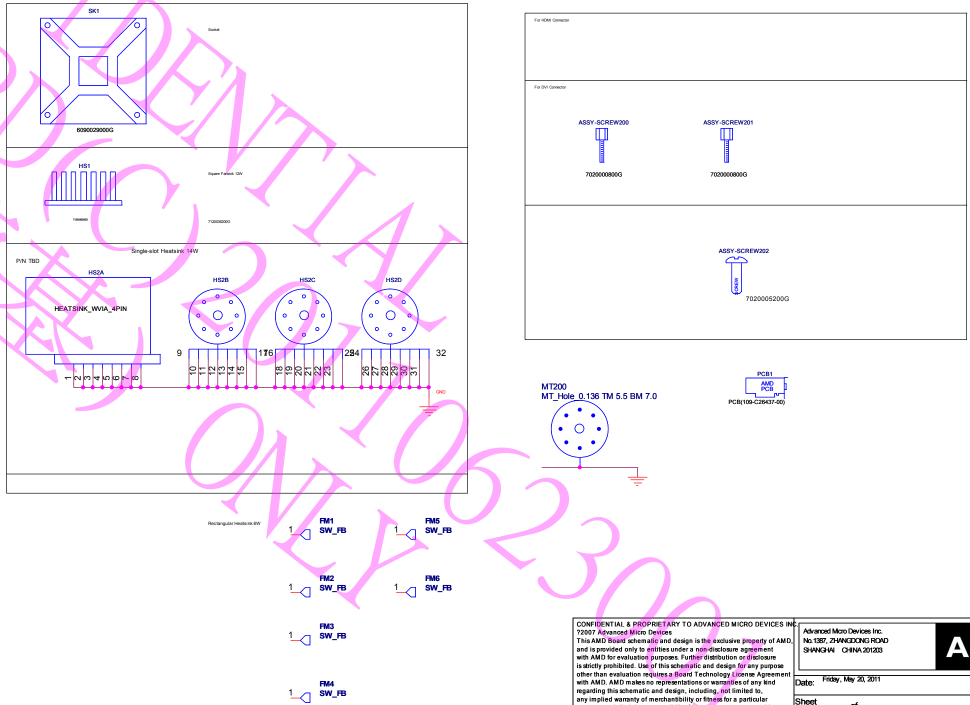
Title PWR& MGMT &SEQ | Doc No. 105-C26000-00A

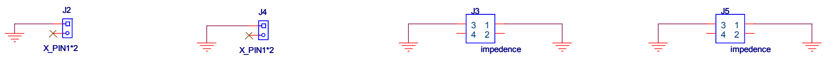
Mechanical and Thermal Management



+1.8V
AD17
AC17
TSVDD
TSVSS
PART 14 OF 15
DPLUS
DMINUS
TS_FDO
T4
T2
R5
CEDAR A11 IF M/E SLT BIN1 TSMC FB12
+3.3V_BUS
R4100
2.61K
R4101
10K
PWM_R
Q4100
MMBT3904
GND
Warning: TS_FDO is not 5V tolerant, MAX sink current 1.65mA
Fan Control
+12V_BUS
FANOUT_P
FANOUT_N
This circuit provides a minimum voltage for the fan, independent of PWM input -> check if needed for RV710
R4112
5.1K
R4113
6.8K
D4100
BAT54KFILM
R4105
1K
MMBT3906
Q4101
Q4102
R4106
1K
C4102
1uF
VDFF
Q4103
PBSS4350Z
Add Copper under pad 4 (at least 1cm^2)
R4108
1M
DNI
R4110
0R
JU4001
HDR_1X2
DNI
BU ONLY
R4102
1K
1%
R4103
22K
R4111
1K
1%
DNI
C4100
0.1uF
B4001
26R_800mA
C4006
1uF
0805
16V



SK1
Socket
6090029000G
HS1
Square Fansink 10W
Single-slot Heatsink 14W
P/N TBD
HS2A
HEATSINK_WVIA_4PIN
HS2B
HS2C
HS2D
Rectangular Heatsink 8W
FM1
SW_FB
FM2
SW_FB
FM3
SW_FB
FM4
SW_FB
FM5
SW_FB
FM6
SW_FB
For HDMI Connector
For DVI Connector
ASSY-SCREW200
7020000800G
ASSY-SCREW201
7020000800G
ASSY-SCREW202
7020005200G
MT200
MT_Hole_0.136 TM 5.5 BM 7.0
PCB1
AMD PCB
PCB(109-C26437-00)



TOP
Single end
Address branch
50 ohm +/- 5 ohm
3.82 mils

Bottom
Single end
Memory data
45 ohm +/- 5 ohm
4.724 mils

TOP
Different
TMDS
85 ohm +/- 10 %
4.33 mils / 5.511 mils

Bottom
Different
PEX_PCIE
85 ohm +/- 10 %
4.921 mils / 6.889 mils

SKU	P/N	CONFIGURATION	Form Factor
JUNBONATOR	80200528A0G	dDVI-I + HDMI	FH / SS
JUNBONATOR-COMMERCIAL	8020052800G	dDVI-I + DP	FH / SS
JUNBONATOR-COMMERCIAL	8020051600G	DVI + DP	LP / SS
JUNBONATOR	80200516A0G	DVI +HDMI	LP / SS
	8020051700G	DVI + DP + VGA	FH / DS
	80200517A0G	DVI +HDMI+ VGA	FH / DS

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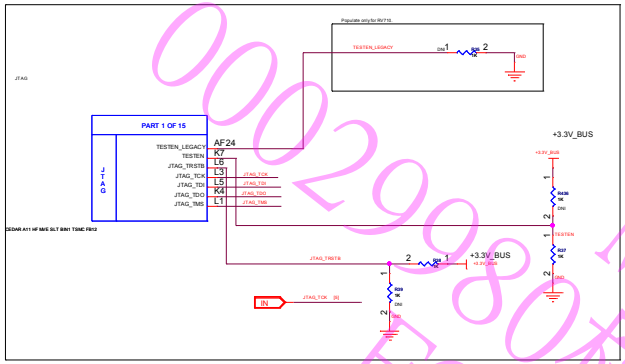
SHANGHAI CHINA 201203

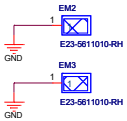
Date: Friday, May 20, 2011 | Rev P00

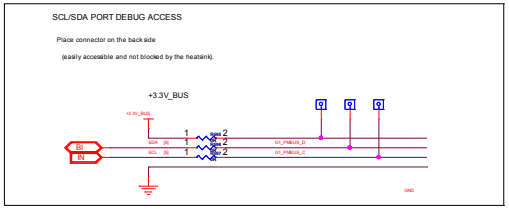
Title: PF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA
MECH/THERMAL MANAGEMENT

Doc No. 105-C264XX-00A

(19) Debug Circuits







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Date: Friday, May 20, 2011 | Rev P00

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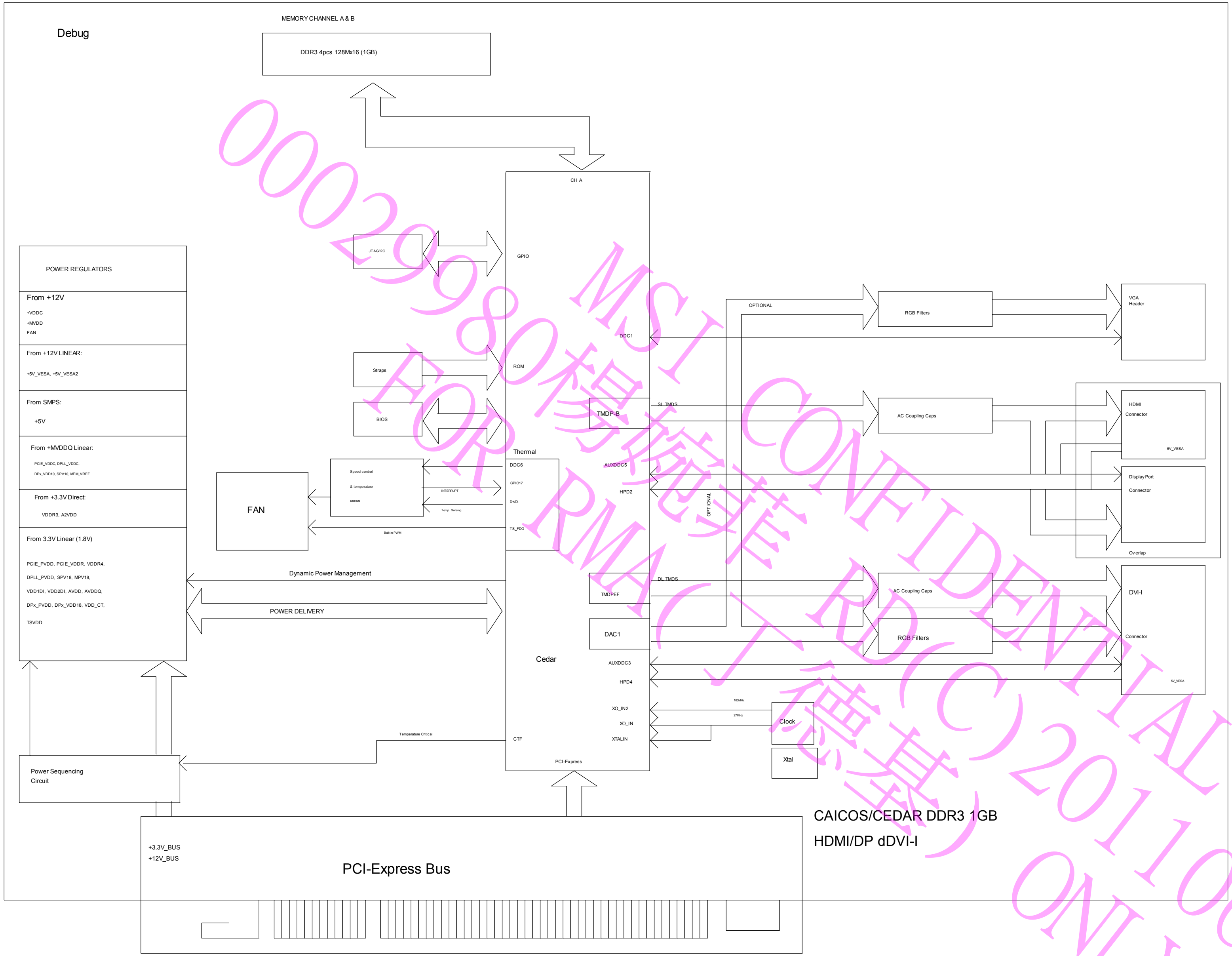
Title: DEBUG CIRCUIT | Doc No. 105-C26000-00A



Debug
MEMORY CHANNEL A & B
DDR3 4pcs 128Mx16 (1GB)
CH A
POWER REGULATORS
From +12V
+VDDC
+MVDD
FAN
From +12V LINEAR:
+5V_VESA, +5V_VESA2
From SMPS:
+5V
From +MVDDQ Linear:
PCIE_VDDC, DPLL_VDDC,
DPx_VDD10, SPV10, MEM_VREF
From +3.3V Direct:
VDDR3, A2VDD
From 3.3V Linear (1.8V)
PCIE_PVDD, PCIE_VDDR, VDDR4,
DPLL_PVDD, SPV18, MPV18,
VDD1DI, VDD2DI, AVDD, AVDDQ,
DPx_PVDD, DPx_VDD18, VDD_CT,
TSVDD
JTAG/I2C
GPIO
Straps
ROM
BIOS
FAN
Speed control
& temperature
sense
Thermal
DDC6
GPIO17
D+/D-
TS_FDO
INTERRUPT
Temp. Sensing
Built-in PWM
Dynamic Power Management
POWER DELIVERY
Cedar
Temperature Critical
CTF
PCI-Express
Power Sequencing
Circuit
+3.3V_BUS
+12V_BUS
PCI-Express Bus
OPTIONAL
RGB Filters
VGA
Header
DDC1
SL_TMDS
TMDP-B
AC Coupling Caps
HDMI
Connector
5V_VESA
AUXDDC5
HPD2
OPTIONAL
Display Port
Connector
Overlap
DL_TMDS
TMDPEF
AC Coupling Caps
DVI-I
Connector
DAC1
RGB Filters
AUXDDC3
HPD4
5V_VESA
XO_IN2
XO_IN
XTALIN
100MHz
27MHz
Clock
Xtal
CAICOS/CEDAR DDR3 1GB
HDMI/DP dDVI-I

Advanced Micro Devices Inc.
No.1387, ZHANGDONG ROAD
SHANGHAI CHINA 201203

Date: Friday, May 20, 2011	Rev P00
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Title PF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA BLOCK DIAGRAM	Doc No. 105-C264XX-00A

AMD	Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA	Schematic No. 105-C264XX-00A	Date: Friday, May 20, 2011

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev P00

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2010/03/31	Initial Caicos Schematic, based on C026XX-10
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