

P654 - GT200/NVIO2

P654, GT200-100, 896MB/1792MB - GDDR3 BGA136 16M/32Mx32

DVI-I + DVI-I/DP + HD/SD/TVout, SPDIF, Dual SLI

Table of Contents


Page 1: Title Page
Page 2: Block Diagram
Page 3: PCI Express / JTAG
Page 4: Framebuffer A,B: GPU Section + Calibration
Page 5: Framebuffer C,D: GPU Section
Page 6: Framebuffer E,F: GPU Section
Page 7: Framebuffer G,H: GPU Section
Page 8: Framebuffer A: Memory Section
Page 9: Framebuffer B: Memory Section
Page 10: Framebuffer C: Memory Section
Page 11: Framebuffer D: Memory Section
Page 12: Framebuffer E: Memory Section
Page 13: Framebuffer F: Memory Section
Page 14: Framebuffer G: Memory Section
Page 15: Framebuffer H: N/A
Page 16: Decoupling: Memory Section A-D
Page 17: Decoupling: Memory Section E-G
Page 18: Decoupling: GPU (NVVDD, FBVDDQ)
Page 19: GPU-NVIO Interconnect: GV Bus / PLL
Page 20: Display: DACA (Middle DVI-I)
Page 21: Display: DACC (South DVI-I)
Page 22: Display: DACB (North MiniDIN) SD/HDTV out
Page 23: Display: IFPAB for south DVI-I (with DACC)
Page 24: Display: IFPCD for middle DVI-I (with DACA)
Page 25: Display: DP - Analogix
Page 26: Connectors: SPDIF
Page 27: Connectors: DR Interface (Dual SLI)
Page 28: MISC: GPIO / XTAL / VBIOS / HDCP / I2C
Page 29: MISC: FAN / THERM
Page 30: MISC: MIO / DVI / STRAPS
Page 31: Power and GND (GPU and NVIOx)
Page 32: Power: Hybrid Power
Page 33: Power Supply: 5V + 5V Alt / SHDN LATCH / IFP_IOVDD
Page 34: Power Supply: 2V5, DP_PWR, 1V15 (PEX_VDD, GV_VDD)
Page 35: Power Supply: Combined FBVDD/Q
Page 36: Power Supply: NVVDD REGULATOR

Page 39: NVVDD & FBVDDQ SENSE/MSUR
Page 40: Power: Input Rail Filter and Detection Logic
Page 41: Thermal/Mechanical

REV	VARIANT	NPIN	ASSEMBLY
B	BASE	600-10654-BASE-A03	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	600-10654-0000-000	DT: GT200-100, 550/350/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I + HDTV
2	SKU001	600-10654-0001-000	DT: GT200-100, 550/350/1000, 896MB - 16MX32 GDDR3, DVI-I + DP + HDTV
3	SKU001	600-10654-0051-300	DT: GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

MS-V180 -0A
PAGE 21:VGS SLIM
PAGE-22 remove DACB HDTV Circuit
PAGE 24:DVI change HDMI
PAGE 25:DP modify DSDA/DSCL circuit
PAGE 28:ADD I2C0_SCL/SDA and GPIO 3 circuit,remove GPIO 12
PAGE 29:remove R112,R113 and GPIO8_FAN_TACH link to U21
PAGE 33:remove R671,R572
PAGE 35:remove RT8805CQVA change UPI6205 and UPI6262 circuit
PAGE 36:remove NCP5388MNR2G change UPI6208 circuit
PAGE 37/38 :remove NCP3418B change UPI6281 circuit
PAGE 39 :Add WL83L786G circuit

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.



Micro-Star International Co., LTD.

<Title>

Size

Document Number

Custom

<Doc>

MS-V180

Rev

<Rev Code>

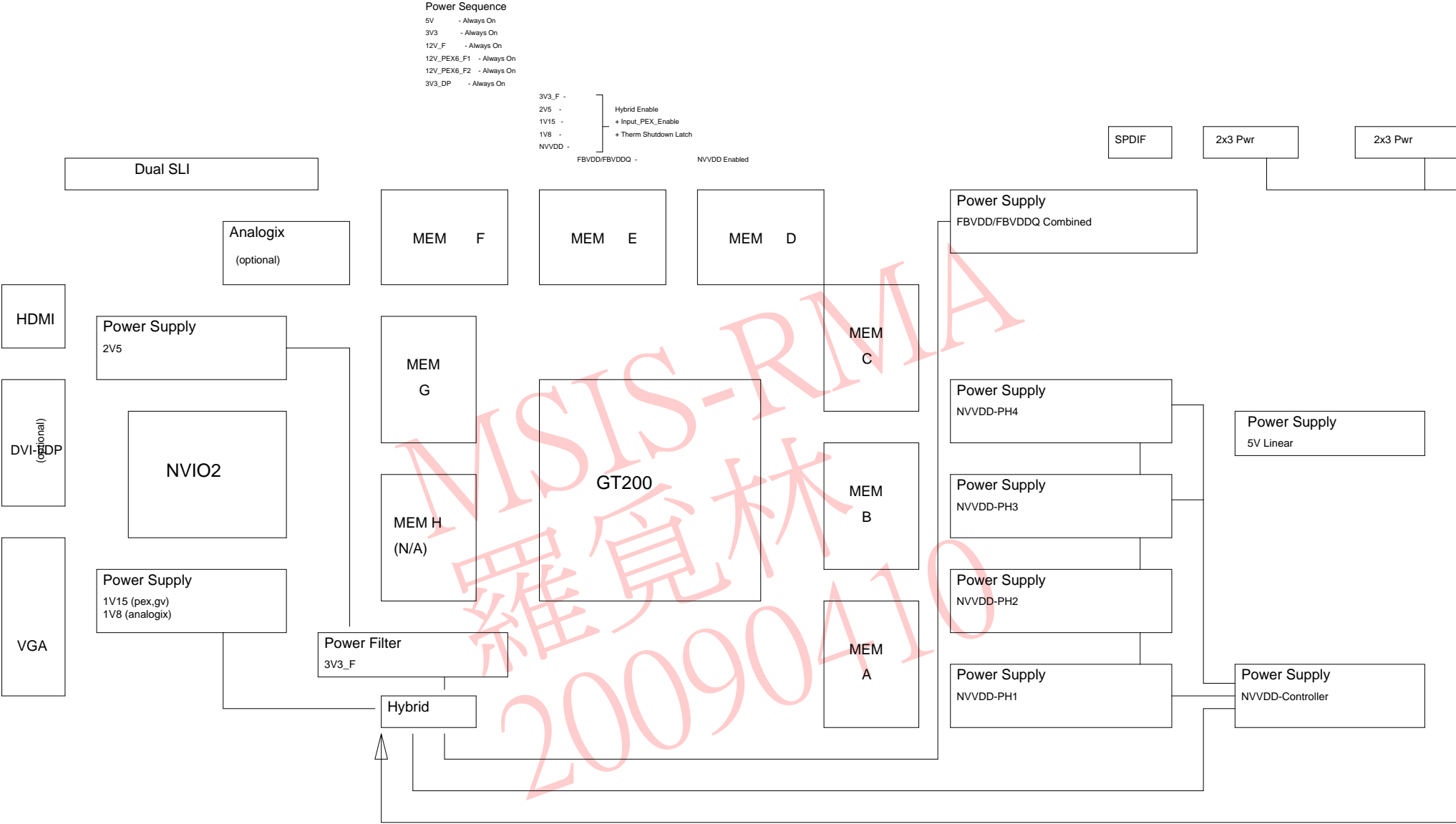
Date

Wednesday, February 11, 2009 13:08

Sheet

1 of 41

Block Diagram



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE PRACTICE, OR INDUSTRY STANDARDS.

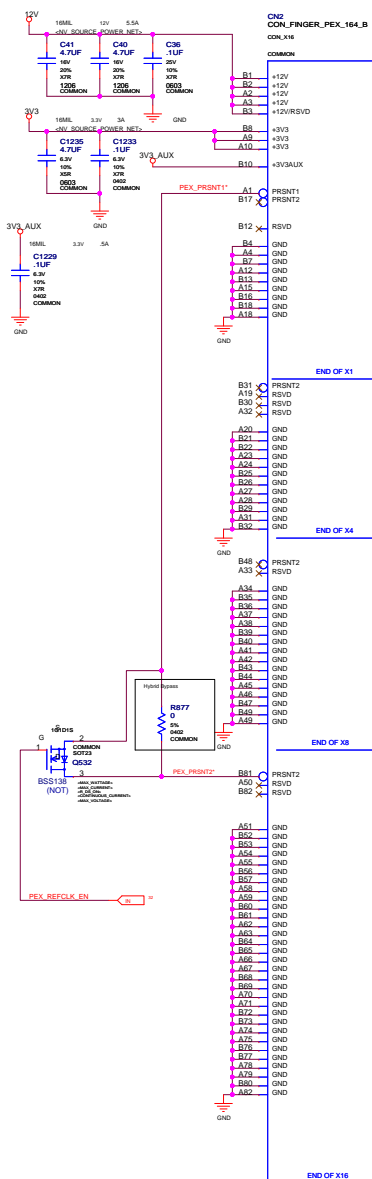
ASSEMBLY PAGE DETAIL
BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Block Diagram

Micro-Star International Co., LTD.

MSI

Size	Document Number	Rev
Custom	<Doc>	<RevCode>
Date	Wednesday, February 11, 2009	Sheet 2 of 41

PCI Express / JTAG

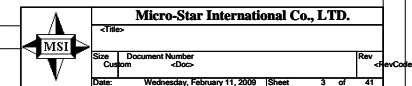


JTAG

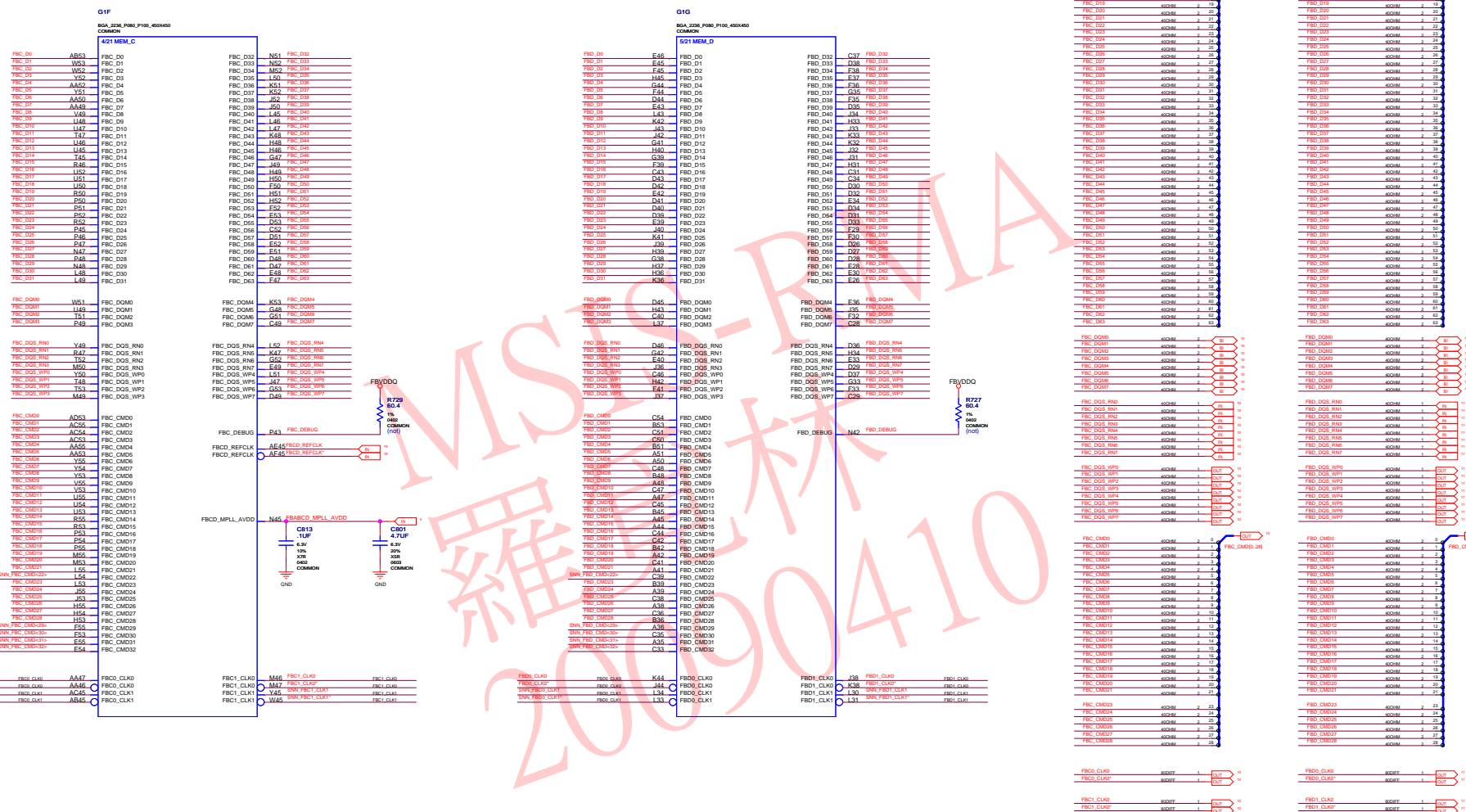


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express / JTAG

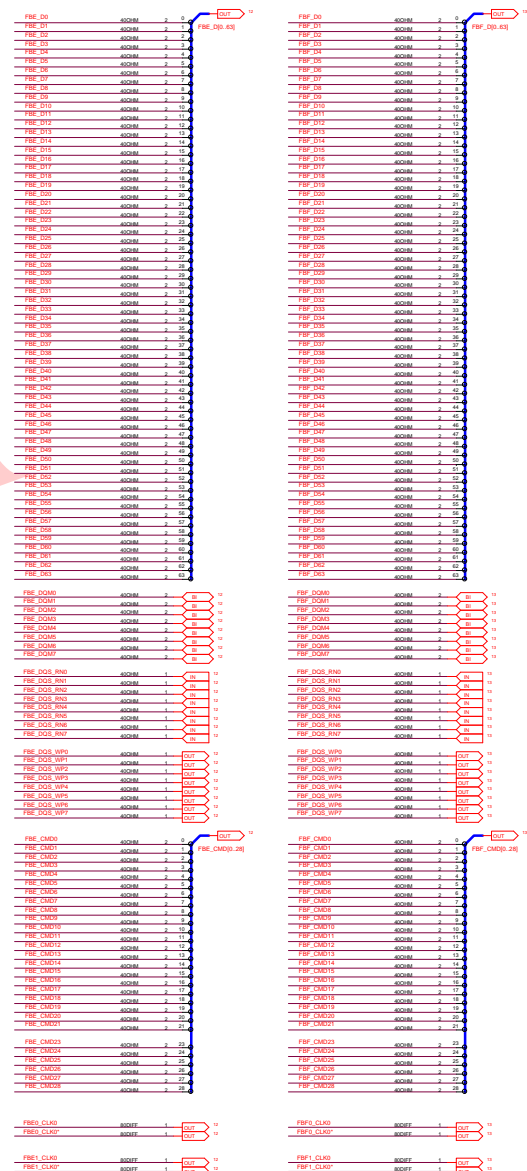
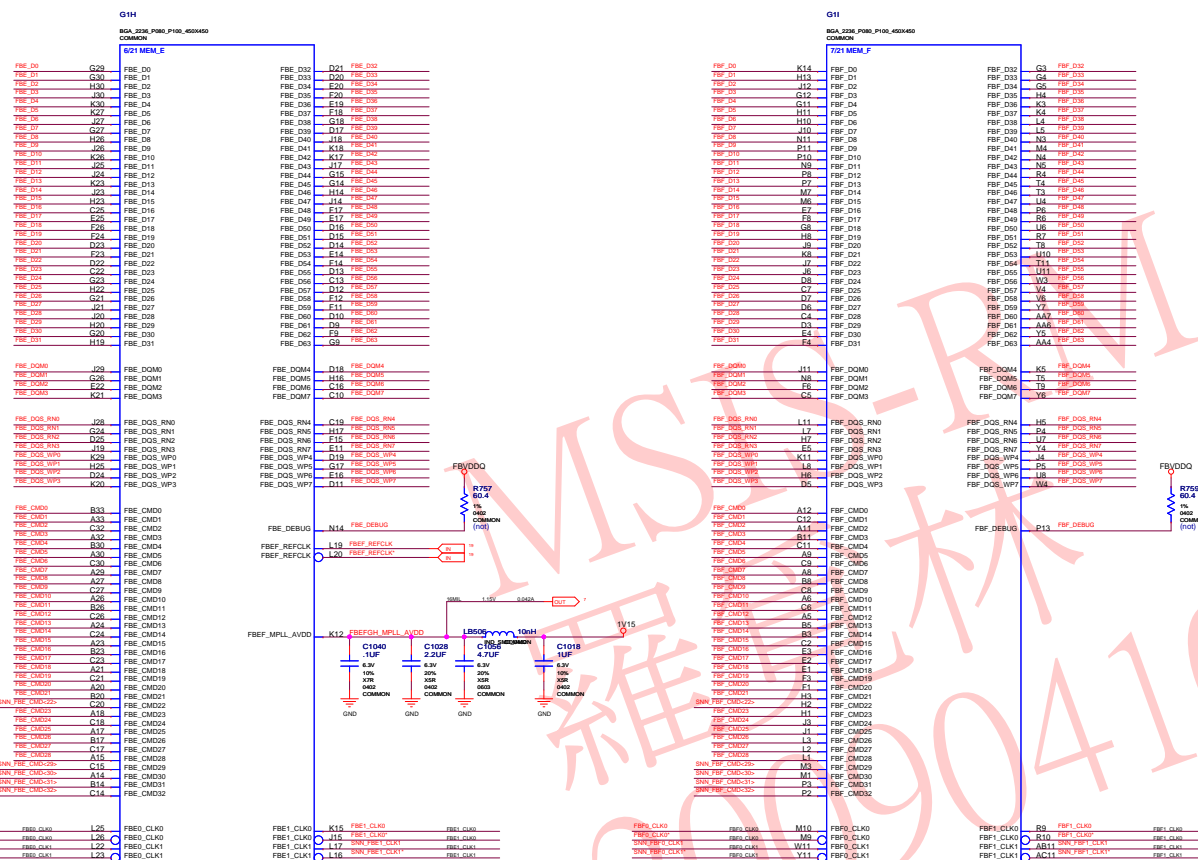


Framebuffer C,D: GPU Section



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

Framebuffer E,F: GPU Section



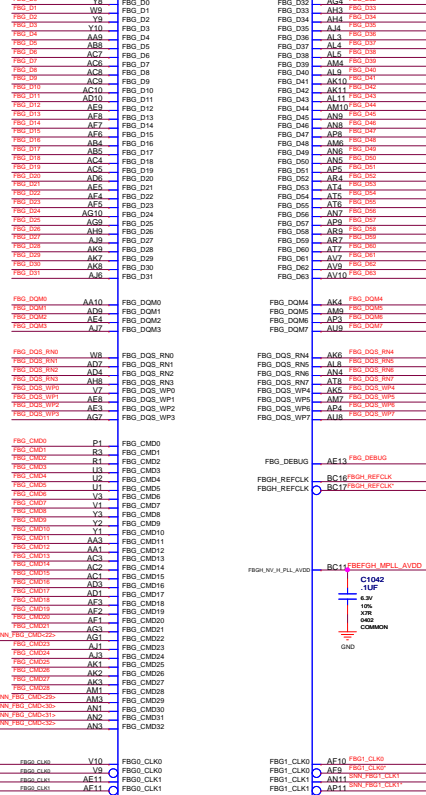
Framebuffer G,H: GPU Section

G1J

REG_230E_FBG0_F100_400460

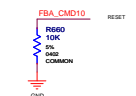
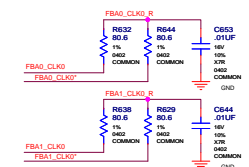
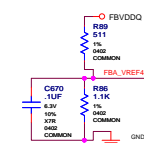
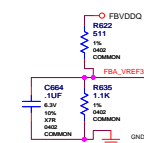
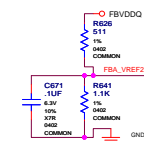
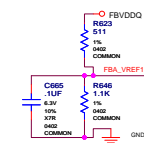
COMMON

B721 MEM_0

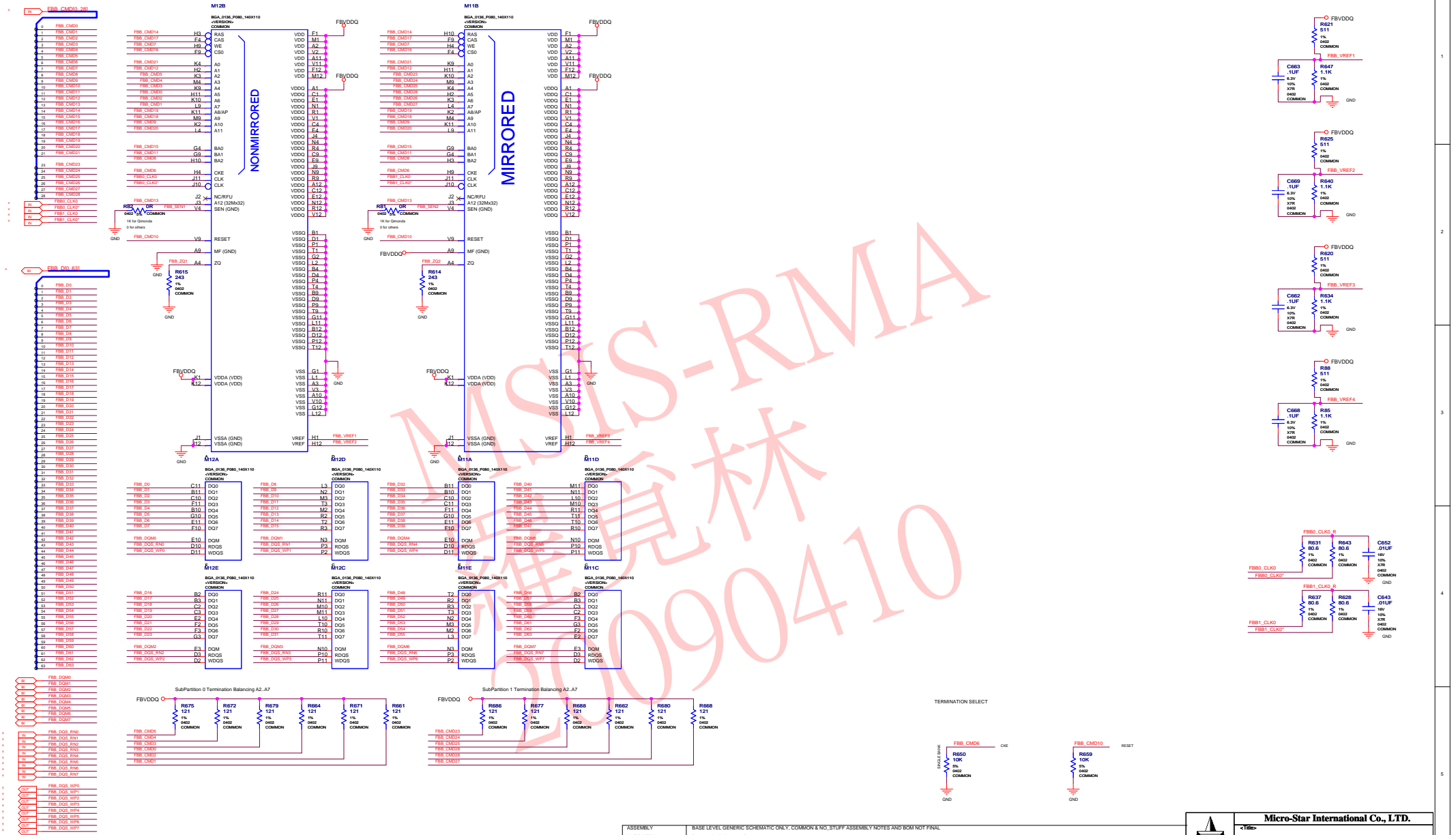


The diagram illustrates the PCB layout for the M138 and M139 components, showing the arrangement of components, pin connections, and termination balancing. The layout is divided into four quadrants, each representing a different component or section of the board.

Top-Left Quadrant (M138): This section shows the M138 component layout. It includes a large 'NONMIRRORED' label. The layout features various components such as resistors (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152, R153, R154, R155, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172, R173, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R185, R186, R187, R188, R189, R190, R191, R192, R193, R194, R195, R196, R197, R198, R199, R200, R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R212, R213, R214, R215, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R226, R227, R228, R229, R230, R231, R232, R233, R234, R235, R236, R237, R238, R239, R240, R241, R242, R243, R244, R245, R246, R247, R248, R249, R250, R251, R252, R253, R254, R255, R256, R257, R258, R259, R260, R261, R262, R263, R264, R265, R266, R267, R268, R269, R270, R271, R272, R273, R274, R275, R276, R277, R278, R279, R280, R281, R282, R283, R284, R285, R286, R287, R288, R289, R290, R291, R292, R293, R294, R295, R296, R297, R298, R299, R300, R301, R302, R303, R304, R305, R306, R307, R308, R309, R310, R311, R312, R313, R314, R315, R316, R317, R318, R319, R320, R321, R322, R323, R324, R325, R326, R327, R328, R329, R330, R331, R332, R333, R334, R335, R336, R337, R338, R339, R340, R341, R342, R343, R344, R345, R346, R347, R348, R349, R350, R351, R352, R353, R354, R355, R356, R357, R358, R359, R360, R361, R362, R363, R364, R365, R366, R367, R368, R369, R370, R371, R372, R373, R374, R375, R376, R377, R378, R379, R380, R381, R382, R383, R384, R385, R386, R387, R388, R389, R390, R391, R392, R393, R394, R395, R396, R397, R398, R399, R400, R401, R402, R403, R404, R405, R406, R407, R408, R409, R410, R411, R412, R413, R414, R415, R416, R417, R418, R419, R420, R421, R422, R423, R424, R425, R426, R427, R428, R429, R430, R431, R432, R433, R434, R435, R436, R437, R438, R439, R440, R441, R442, R443, R444, R445, R446, R447, R448, R449, R450, R451, R452, R453, R454, R455, R456, R457, R458, R459, R460, R461, R462, R463, R464, R465, R466, R467, R468, R469, R470, R471, R472, R473, R474, R475, R476, R477, R478, R479, R480, R481, R482, R483, R484, R485, R486, R487, R488, R489, R490, R491, R492, R493, R494, R495, R496, R497, R498, R499, R500, R501, R502, R503, R504, R505, R506, R507, R508, R509, R510, R511, R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R528, R529, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R540, R541, R542, R543, R544, R545, R546, R547, R548, R549, R550, R551, R552, R553, R554, R555, R556, R557, R558, R559, R560, R561, R562, R563, R564, R565, R566, R567, R568, R569, R570, R571, R572, R573, R574, R575, R576, R577, R578, R579, R580, R581, R582, R583, R584, R585, R586, R587, R588, R589, R590, R591, R592, R593, R594, R595, R596, R597, R598, R599, R600, R601, R602, R603, R604, R605, R606, R607, R608, R609, R610, R611, R612, R613, R614, R615, R616, R617, R618, R619, R620, R621, R622, R623, R624, R625, R626, R627, R628, R629, R630, R631, R632, R633, R634, R635, R636, R637, R638, R639, R640, R641, R642, R643, R644, R645, R646, R647, R648, R649, R650, R651, R652, R653, R654, R655, R656, R657, R658, R659, R660, R661, R662, R663, R664, R665, R666, R667, R668, R669, R670, R671, R672, R673, R674, R675, R676, R677, R678, R679, R680, R681, R682, R683, R684, R685, R686, R687, R688, R689, R690, R691, R692, R693, R694, R695, R696, R697, R698, R699, R700, R701, R702, R703, R704, R705, R706, R707, R708, R709, R710, R711, R712, R713, R714, R715, R716, R717, R718, R719, R720, R721, R722, R723, R724, R725, R726, R727, R728, R729, R730, R731, R732, R733, R734, R735, R736, R737, R738, R739, R740, R741, R742, R743, R744, R745, R746, R747, R748, R749, R750, R751, R752, R753, R754, R755, R756, R757, R758, R759, R760, R761, R762, R763, R764, R765, R766, R767, R768, R769, R770, R771, R772, R773, R77



Framebuffer B: Memory Section



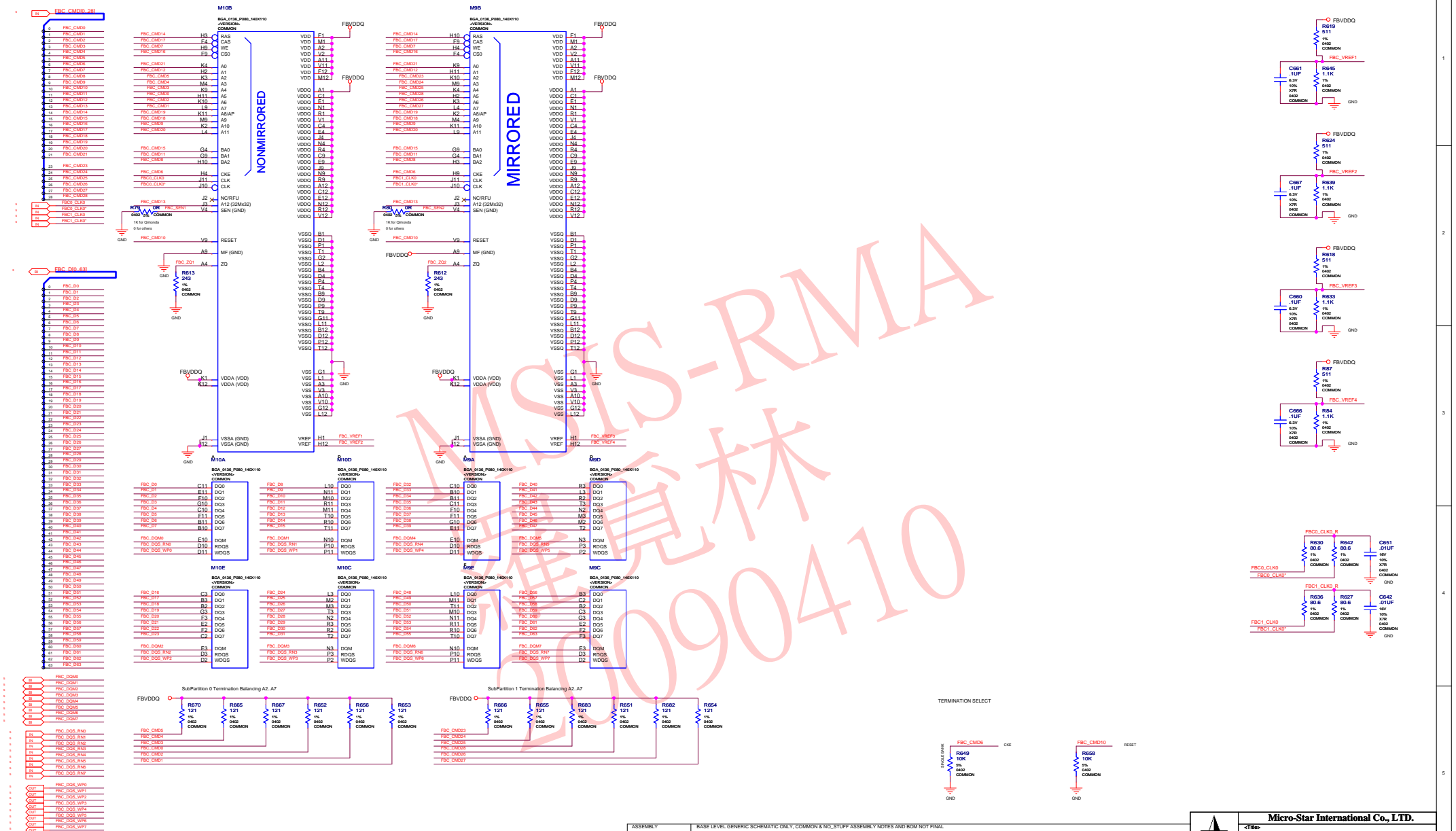
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE Schematics, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY PAGE DETAIL
BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 10107 ASSEMBLY NOTES AND BOM NOT FINAL
Framebuffer B: Memory Section

Micro-Star International Co., LTD.

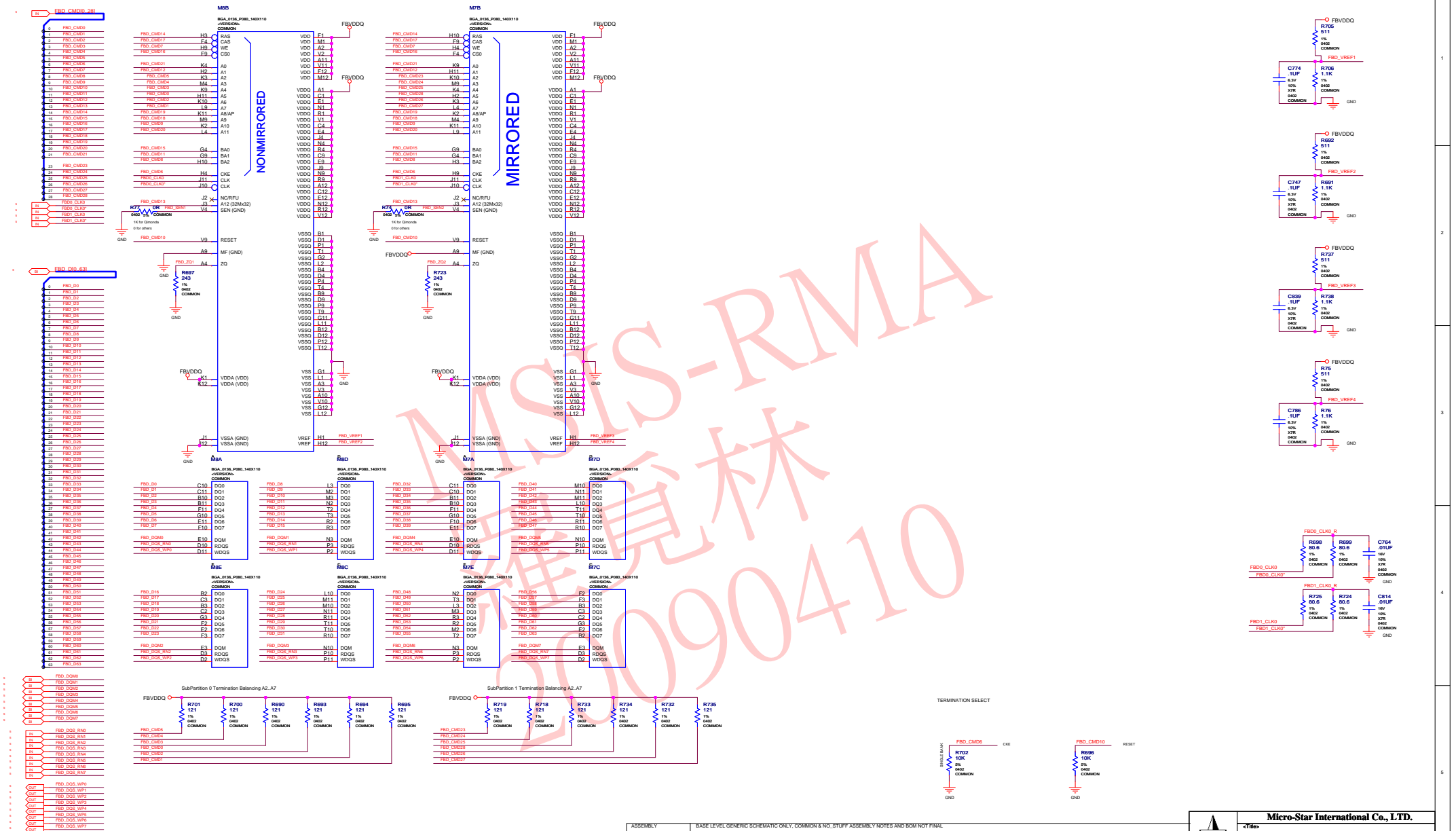
Size Custom Document Number <Doc> MS-V180
Date: Wednesday, February 11, 2009 8:41 AM

Framebuffer C: Memory Section



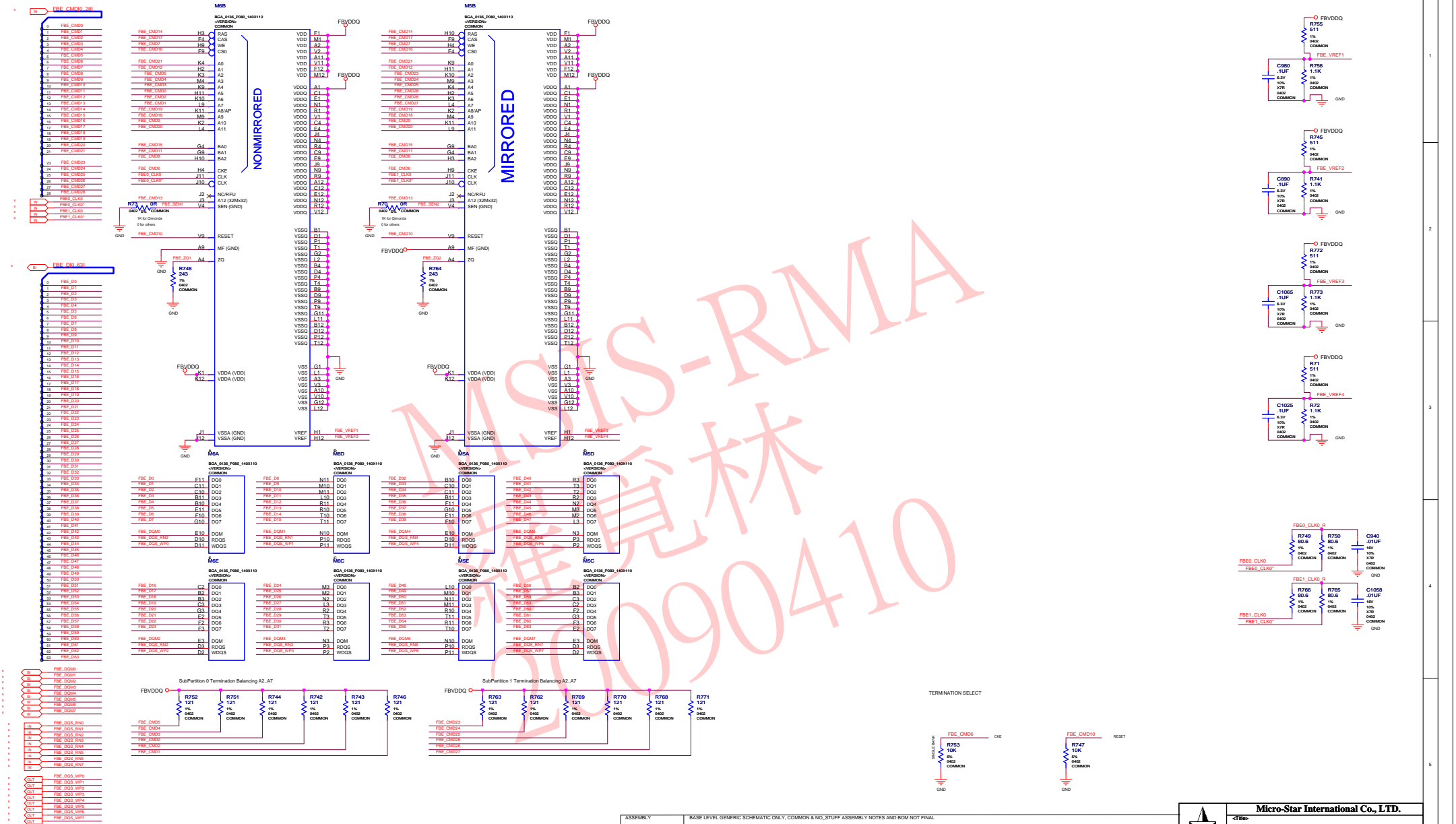
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VARIATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

Framebuffer D: Memory Section



1. ALL NVIDIA DEVICE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (OR INFORMATION THEREON AND SEPARATELY, "MATERIALS") ARE PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE OR INDUSTRY STANDARDS.		ASSEMBLY PAGE DETAIL
--	--	-------------------------

Framebuffer E: Memory Section

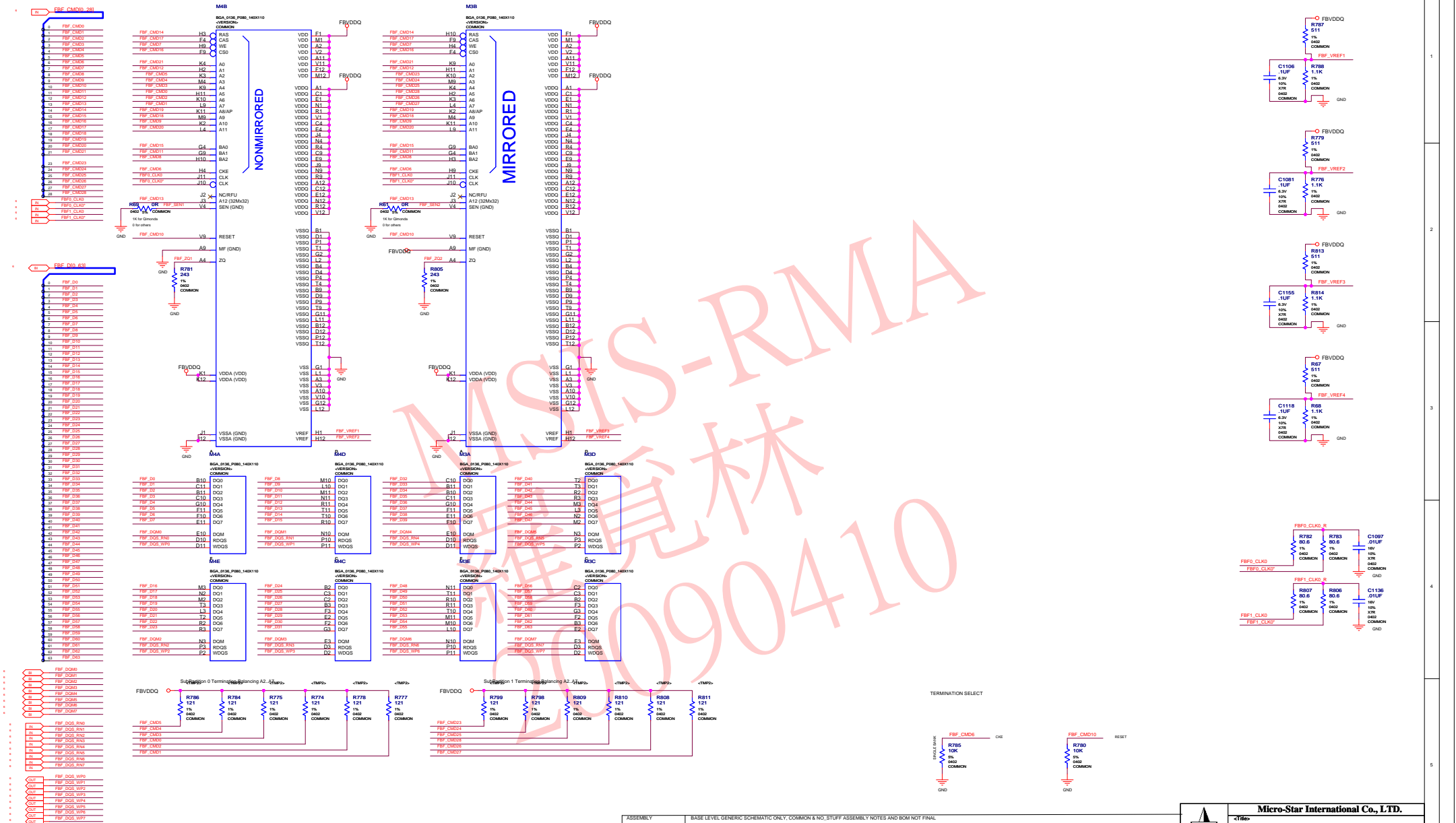
[illegible]

Micro-Star International Co., LTD.

<Title>	
Size Custom	Document Number <Doc>
Date: Wednesday, Feb	

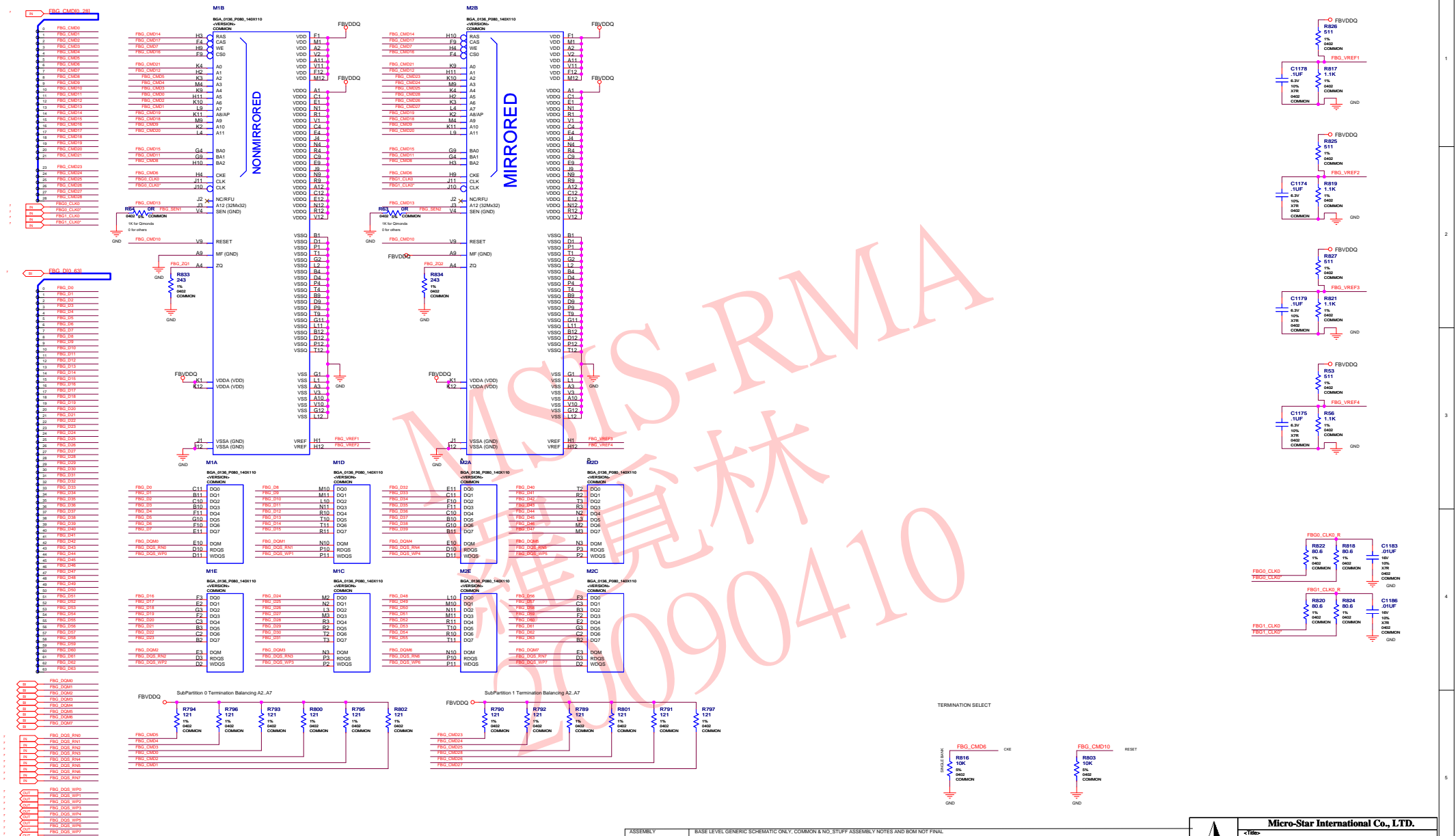
ev	<FevCode>
----	-----------

Framebuffer F: Memory Section



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGRAMS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED FOR INFO. THE MATERIALS MAY
CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS AND EXPRESSLY DISCLAIMS ALL
IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE OR INDUSTRY STANDARD.

Framebuffer G: Memory Section




	FED. GOV. WPA	ASSEMBLY
	CAN. PROV. WPA	PAGE DETAIL
<p>ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGRAMS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARD.</p>		

Framebuffer H: N/A

MSIS-RMA
羅覓林
20090410

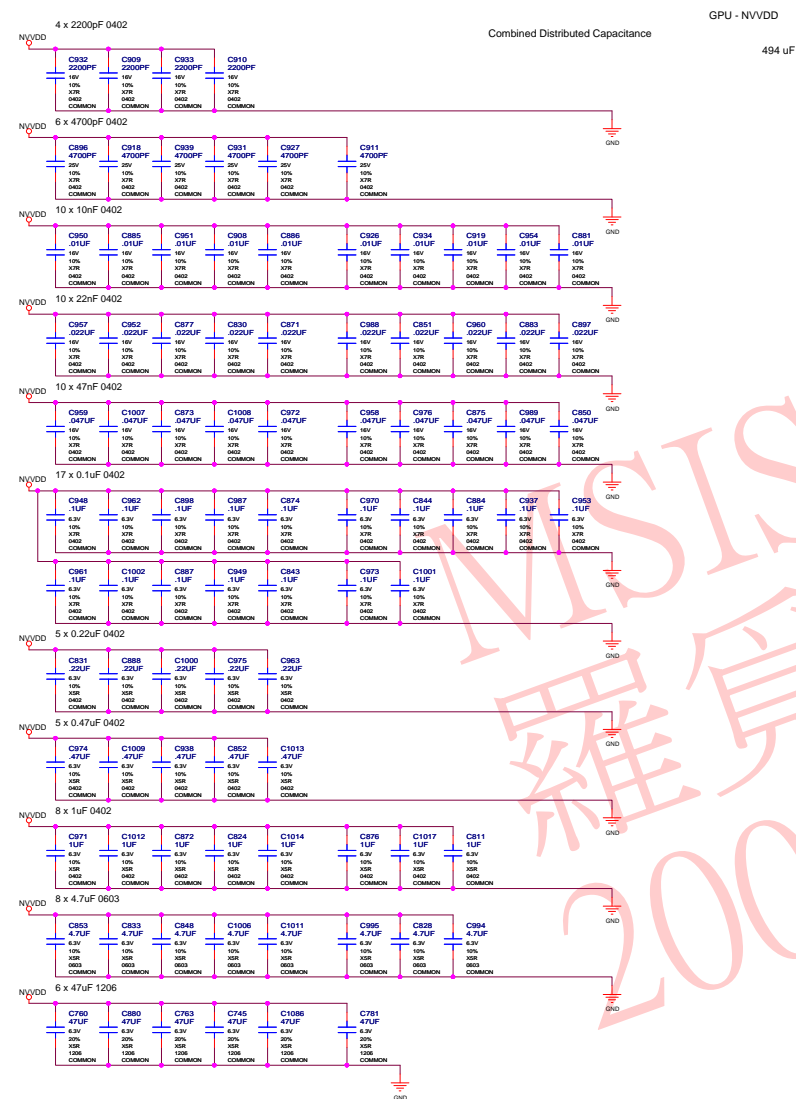
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY PAGE DETAIL	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL Framebuffer H: N/A
-------------------------	---

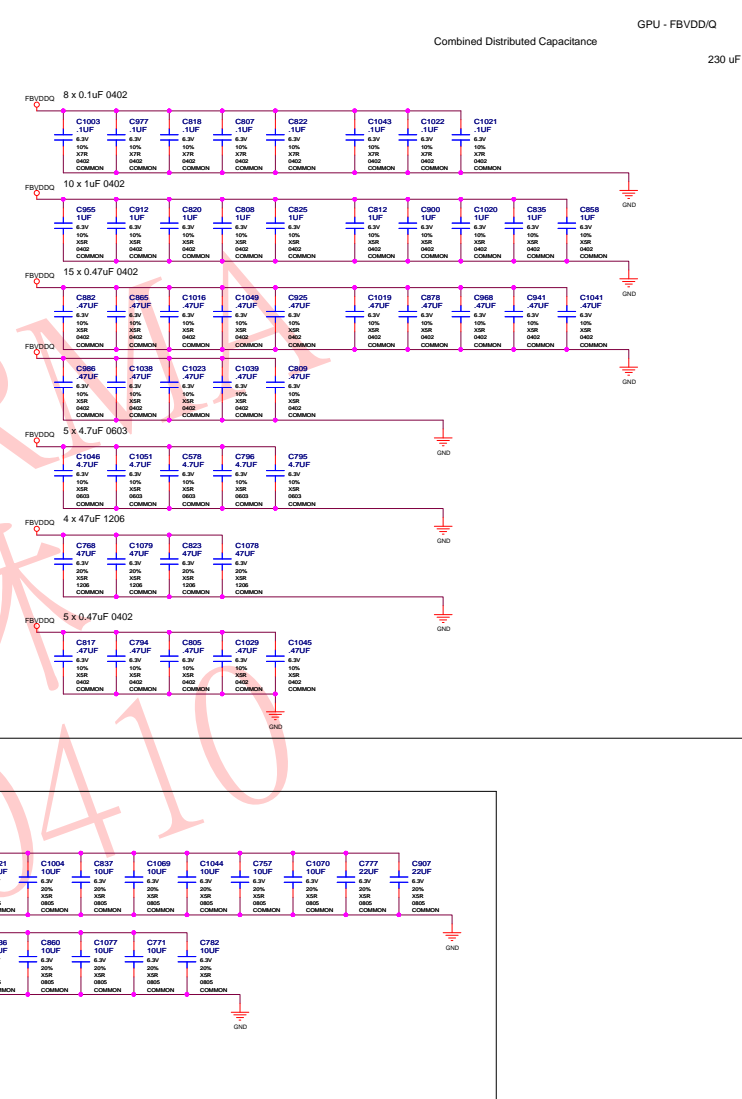
	Micro-Star International Co., LTD.		
	<Title>		
	Site	Document Number	Rev
	Custom	<Doc>	
Date	Wednesday, February 11, 2009		Sheet 15 of 41

Decoupling: GPU (NVVDD, FBVDDQ)

Decoupling for NVVDD (under GPU)



Decoupling for FBVDDQ (under GPU)



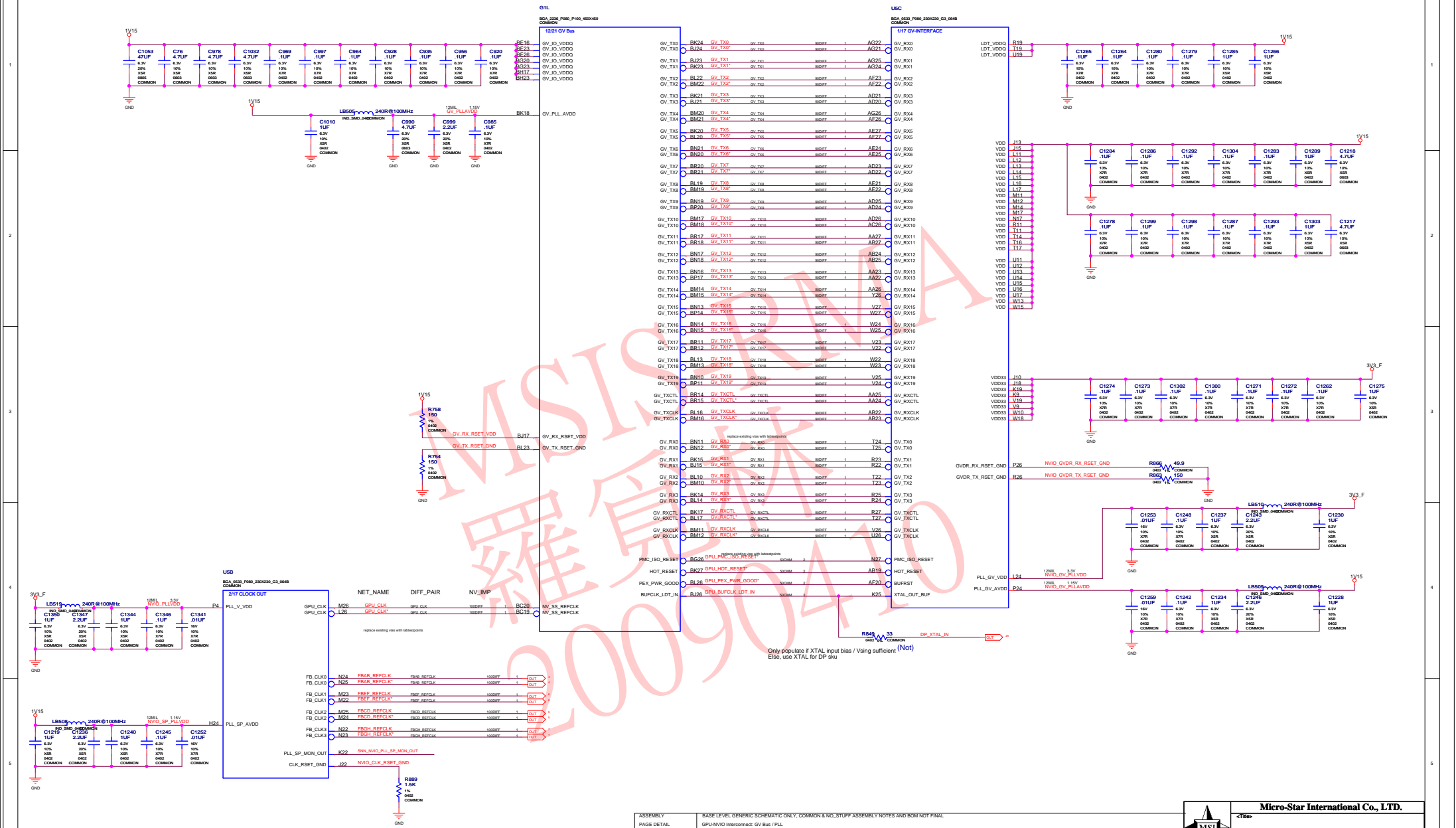
ASSEMBLY
PAGE DETAIL

DATE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Decoupling GPU (NVVDD, FBVDDQ)

Micro-Star International Co., Ltd.	
<Tab>	
Size	Document Number
Custom	<Doc>
Date:	Wednesday, February 11, 2009
Sheet	18 of 41

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTIC LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

GPU-NVIO Interconnect: GV Bus / PLL



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	GPU-NVIO Interconnect: GV Bus / PLL



Micro-Star International Co., LTD.

Size	D
------	---

Size	Document Number
Custom	<Doc>

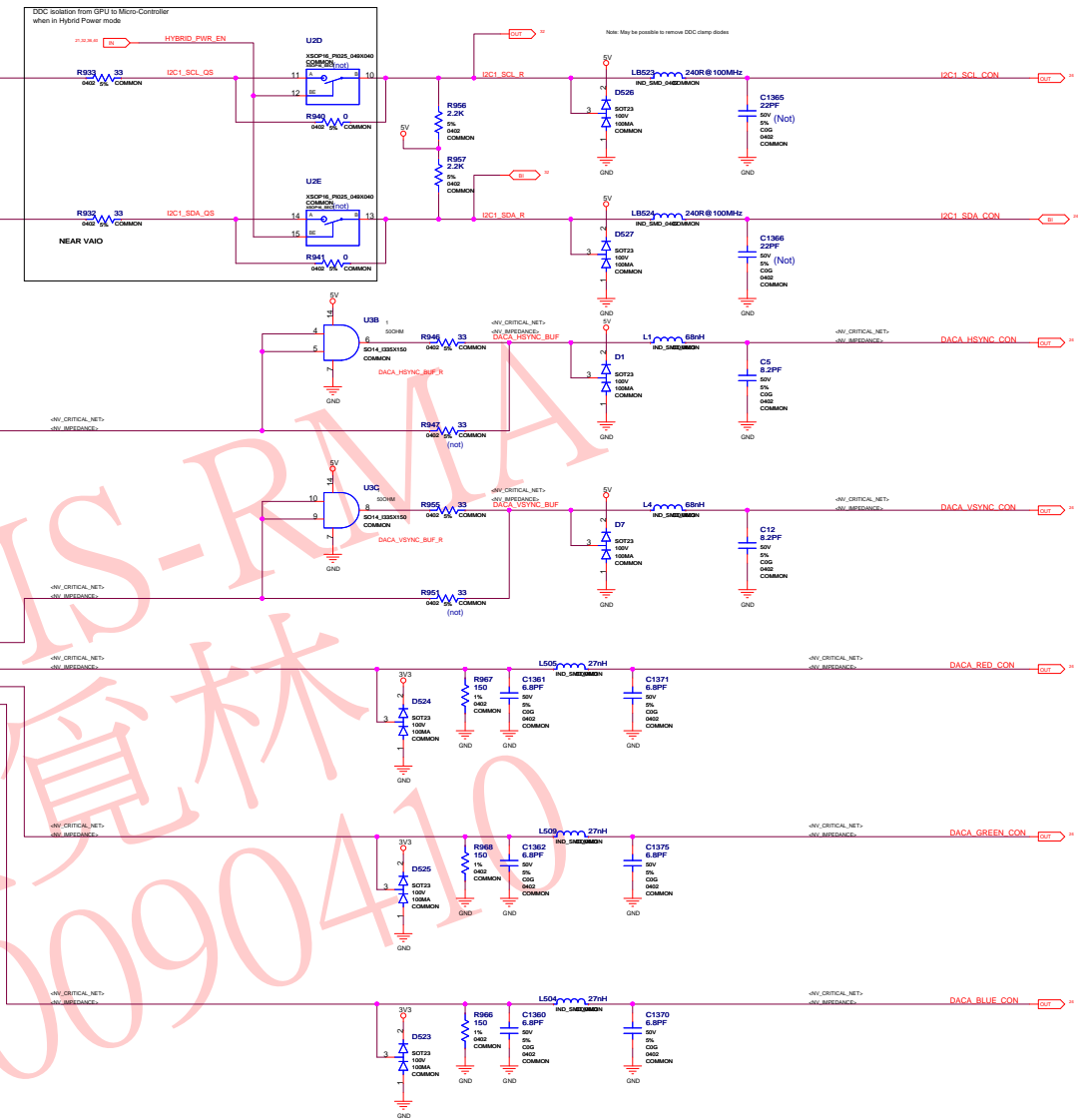
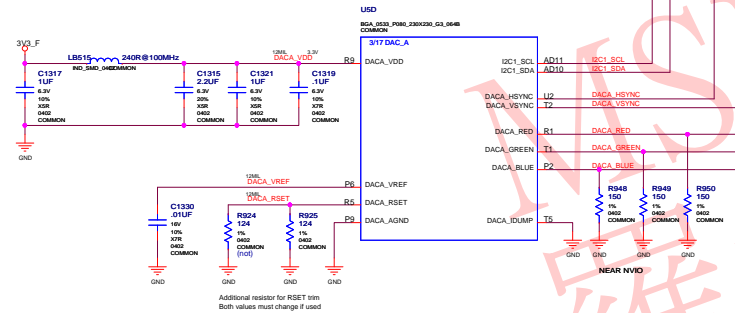
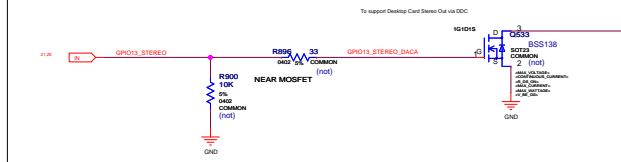
Date: Wednesday, Feb 22, 2012 12:00 PM

«Результат»

31	
----	--

Display: DACA (Middle DVI-I)

Desktop STEREO (option)

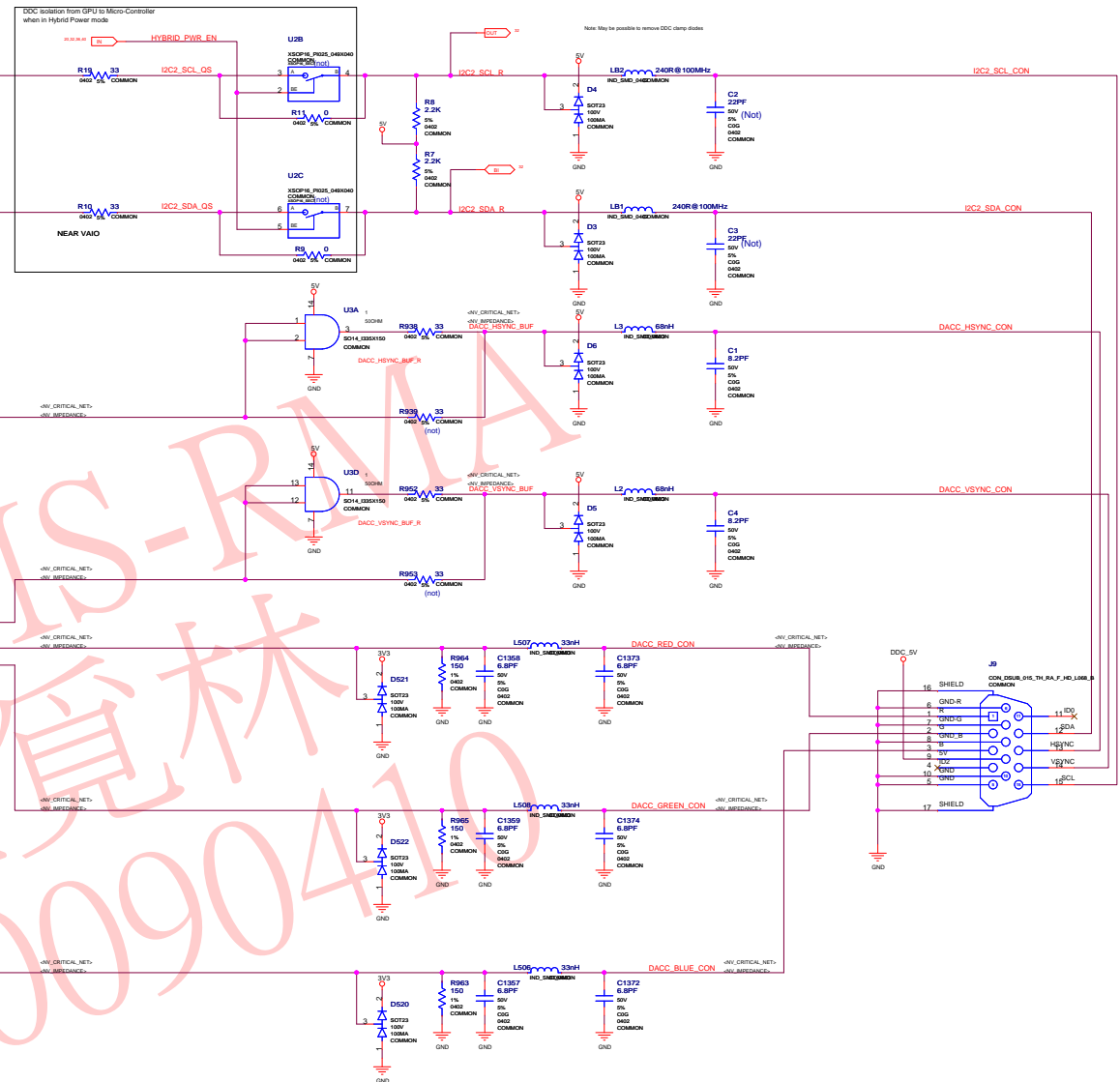
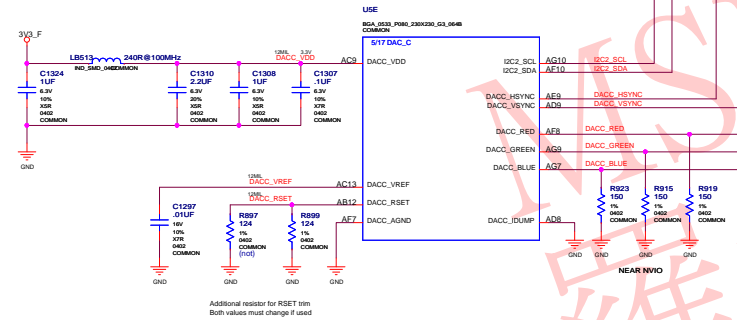
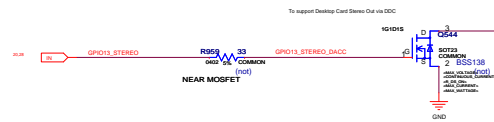


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTIC LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY PAGE DETAIL
NVIDIA LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_310F ASSEMBLY NOTES AND BOM NOT FINAL
Display: DACA (Middle DVI-I)

Micro-Star International Co., LTD.			
<Title>			
Size	Document Number	Rev	
Date	Wednesday, February 11, 2009	Sheet	20 of 41

Display: DACC (South DVI-I)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: DACC (South DVI-I)



Micro-Star International Co., LTD.

	<Title>
--	---------

Size	Document Number
Custom	<Doc>

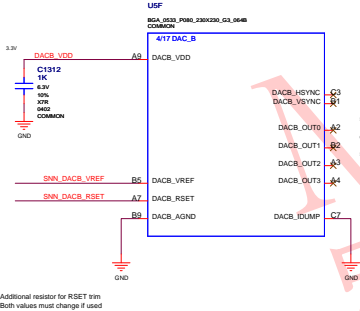
Date: Wednesday, February 11, 2009 Sheet 21 of 41

RevCode:

41		
----	--	--

Display: DACB (North MiniDIN) SD/HDTV out

11/21 remove TV

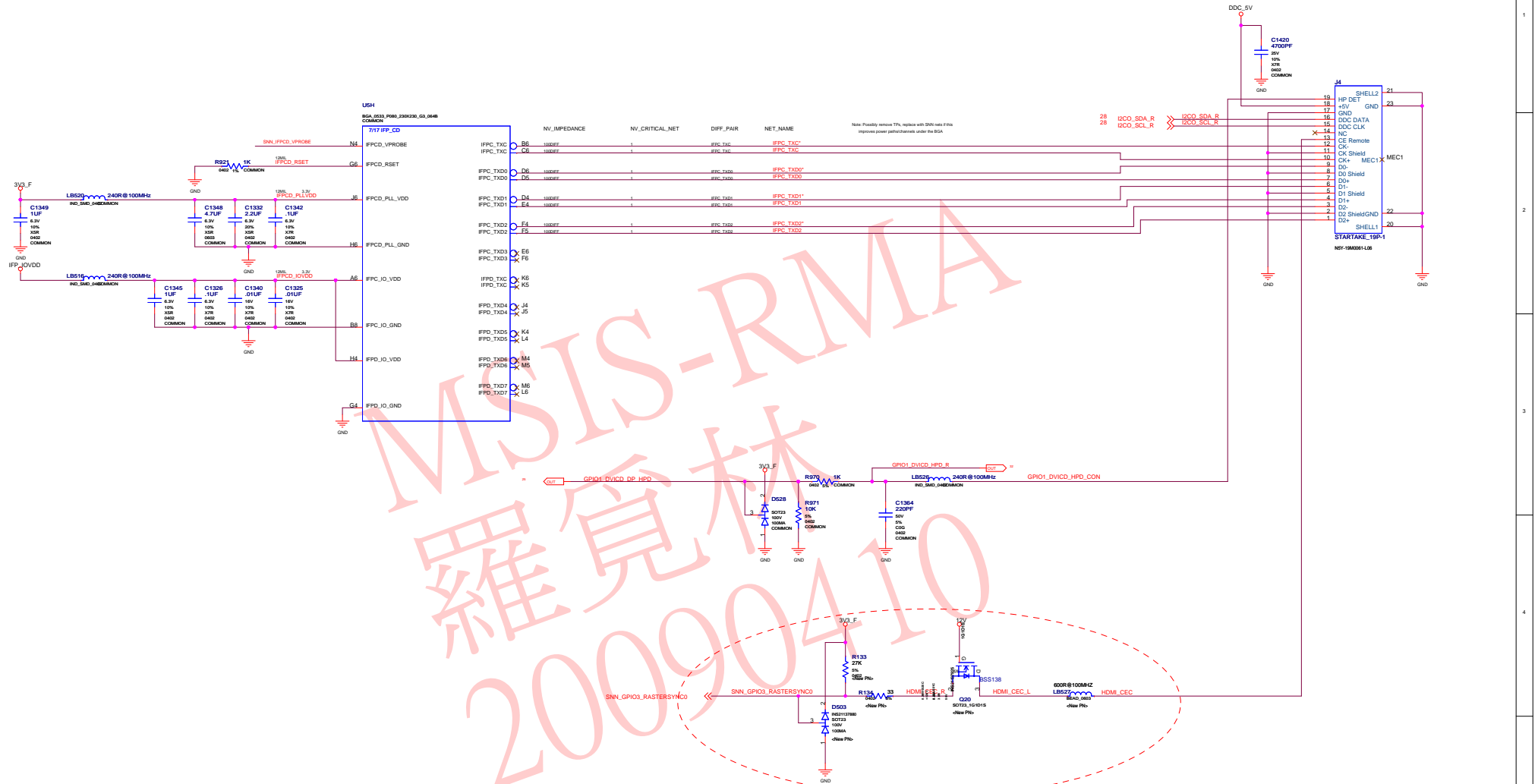


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY
PAGE DETAIL
STATE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO, STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Display: DACB (North MiniDIN) SD/HDTV out

Micro-Star International Co., LTD.			
<Title>			
Size	Document Number	Rev	<RevCode>
Custom	<Doc>		
Date:	Wednesday, February 11, 2009	Sheet	22 of 41

Display: IFPCD for middle DVI-I (with DACA)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: IFPCD for middle DVI-I (with DACA)



Micro-Star International Co., LTD.

Size	1
Custom	

Size	Document Number
Custom	Doc

Custom	Edouard
Order	Wednesday, 5/1/2013

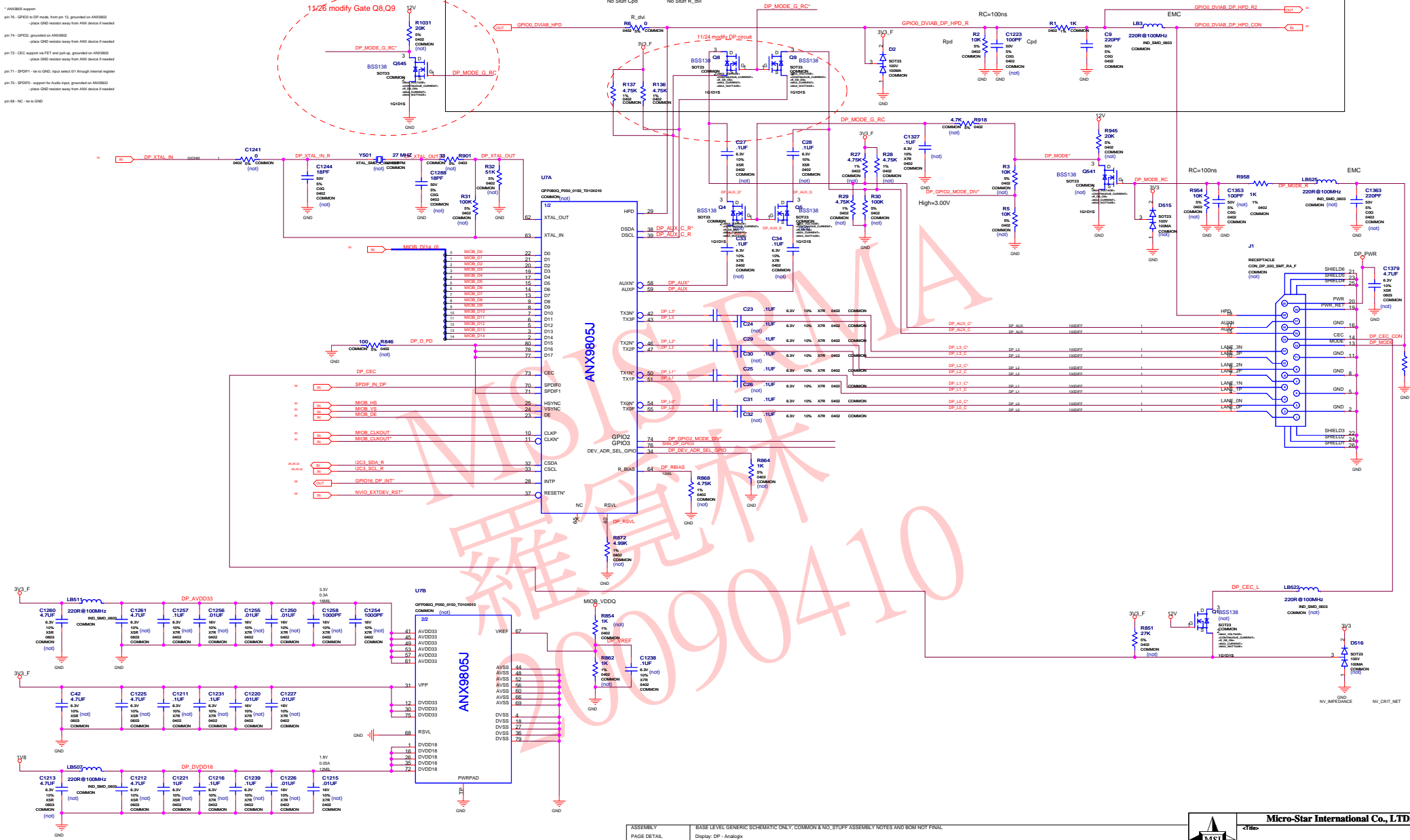
Page 10

Area	Frequency
Area 1	10
Area 2	20
Area 3	30
Area 4	40
Area 5	50
Area 6	60
Area 7	70
Area 8	80
Area 9	90
Area 10	100

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE OR INDUSTRY STANDARDS.

Display: DP - Analogix

- * AN0805 support
- pin 76 - GPIO3 to DP mode, from pin 13, grounded on AN0802
 - place GND resistor away from ANK device if needed
- pin 74 - GPIO2, grounded on AN0802
 - place GND resistor away from ANK device if needed
- pin 73 - CEC support via FET and pull-up, grounded on AN0802
 - place GND resistor away from ANK device if needed
- pin 71 - SPDIF1 - I_S to GND, input select 01 through internal registers
- pin 70 - SPDIF2 - support for Audio input, grounded on AN0802
 - place GND resistor away from ANK device if needed
- pin 68 - NC - tie to GND



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BLOCKS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: DP - Analogix



Micro-Star International Co., LTD.

	<Title>
--	---------

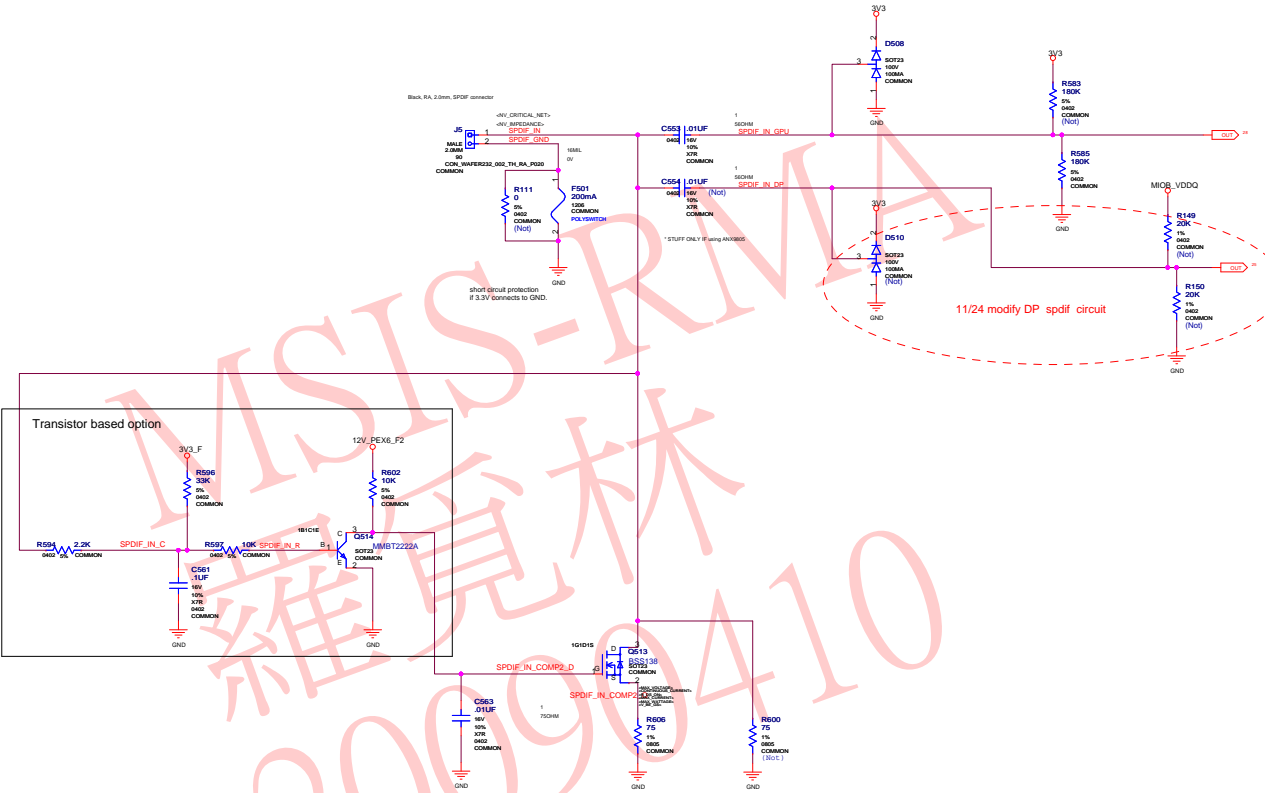
Size	Document Number
------	-----------------

Custom	<Doc>
Doc	Wednesday, 20

Page 10 of 10

Connectors: SPDIF

SPDIF INPUT / Level Detection



Transistor based option

11/24 modify DP spdif circuit

ASSEMBLY
PAGE DATA

BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL



Micro-Star International Co., LTD.

	<Title>
--	---------

Size	Document Number
------	-----------------

Custom	<Doc>
--------	-------

Rev	
-----	--

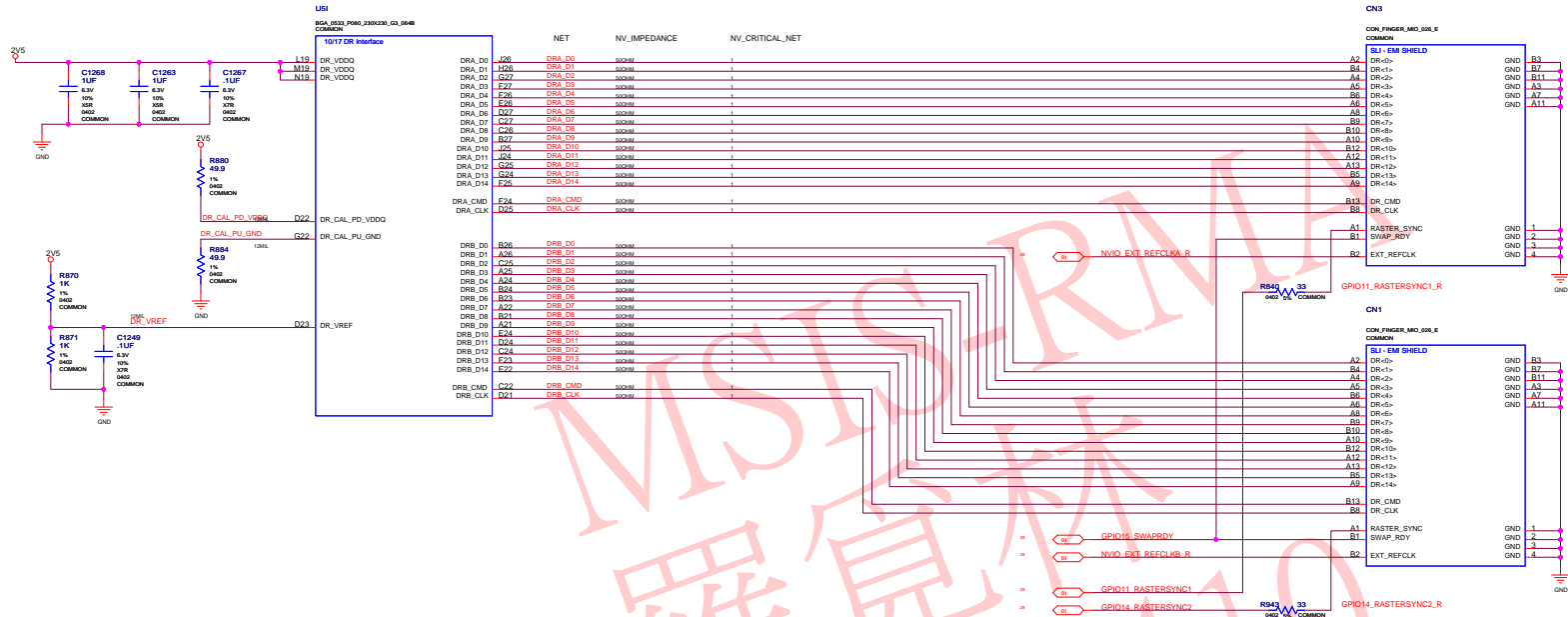
	<RevCode>
--	-----------

Date: Wednesday, February 11, 2009 Sheet 26 of 41

[illegible]

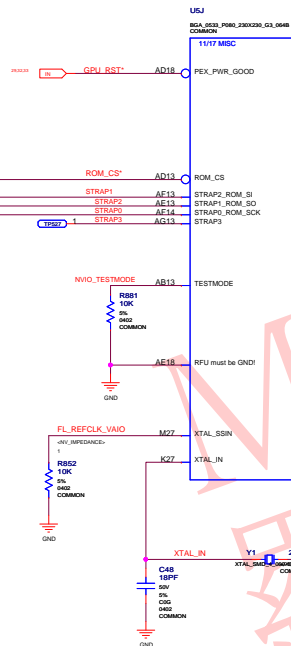
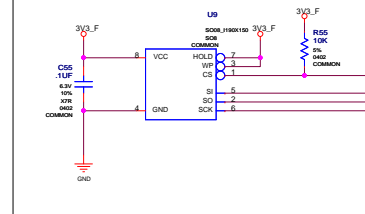
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

Connectors: DR Interface (Dual SLI)

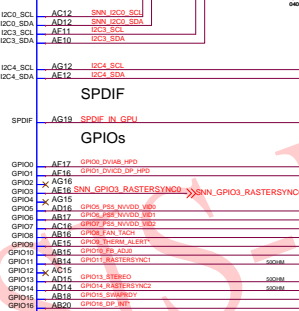


MISC: GPIO / XTAL / VBIOS / HDCP / I2C

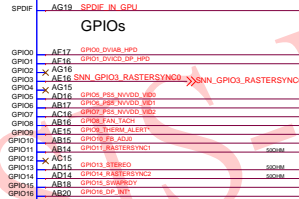
VBIOS



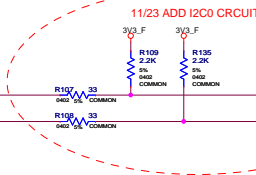
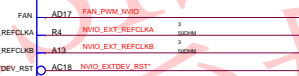
I2C



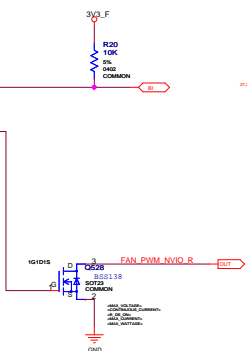
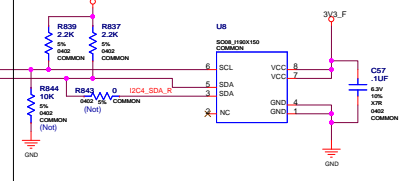
SPDIF



GPIOs



HDCP ROM

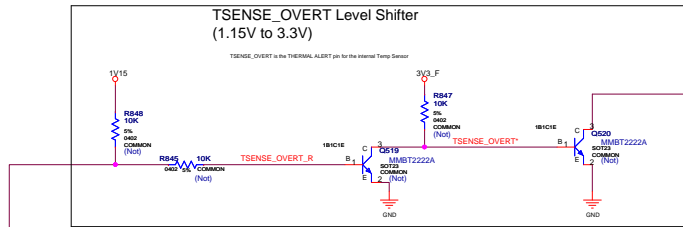


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

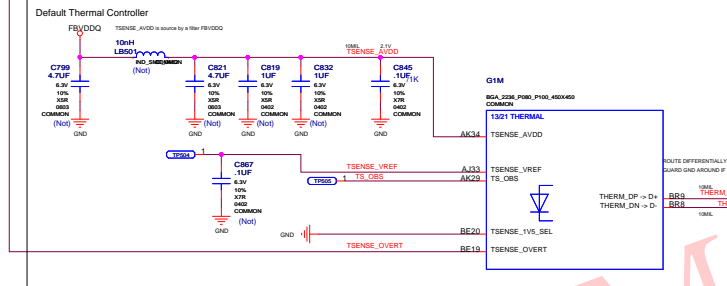
ASSEMBLY	MAX LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO / XTAL / VBIOS / HDCP / I2C

Micro-Star International Co., LTD.	
Size	Custom
Document Number	<Doc>
Date	Wednesday, February 11, 2009
Sheet	28 of 41

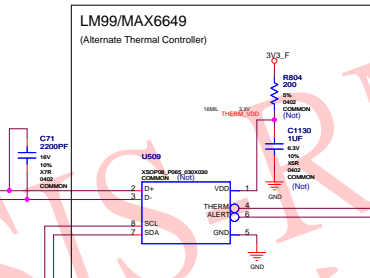
MISC: FAN / THERM



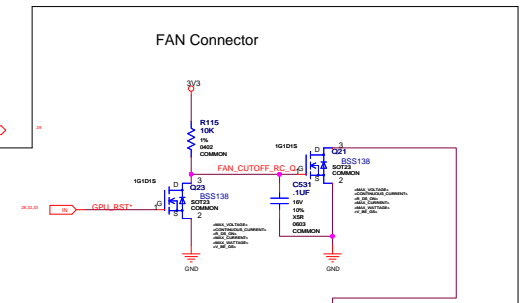
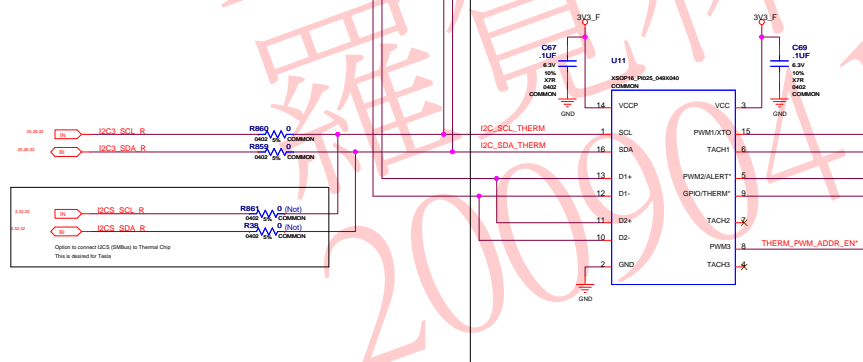
Default Thermal Controller



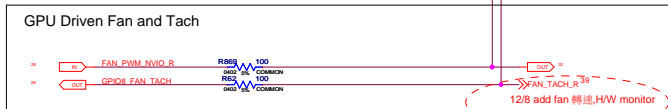
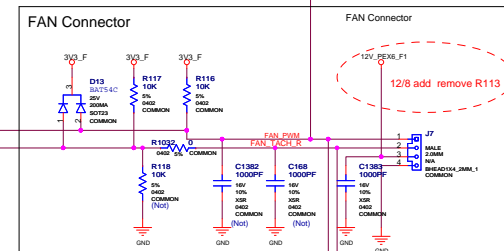
tsense_1v5_sel = 0:	TS_AVDD = 1.7v - 2.1v (default) (wired to gnd)
tsense_1v5_sel = 1:	TS_AVDD = 1.45v - 1.7v (wired to NVVDD)



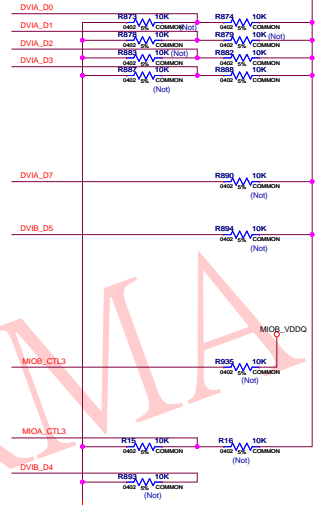
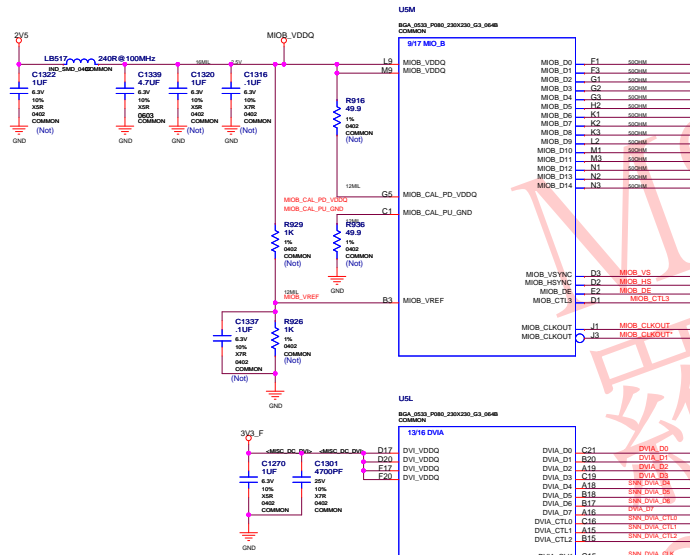
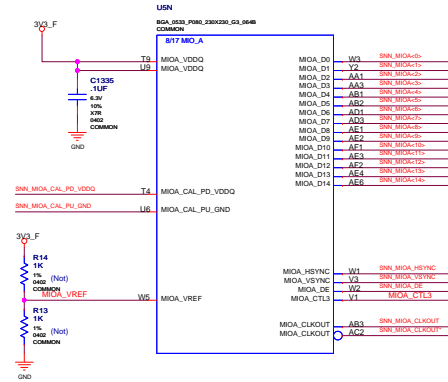
Note: POR internal thermal controls will be DNI
external controls will be DNI



1000



MISC: MIO / DVI / STRAPS

STRAP BITS BOOT0 = 0x101000

NR.	USAGE	COMMENT
00:	GV_WIDTH	DEFAULT=0x00 (WIDE)
01:	SUB_VENDOR	DEFAULT=0x1 (FROM BIOS)
02:	RAM_CFG[0]	
03:	RAM_CFG[1]	
04:	RAM_CFG[2]	
05:	RAM_CFG[3]	
06:	CRYSTAL	DEFAULT=0x00 (27MHz)
07:	TV_MODE[0]	DEFAULT=0x1 (NTSC_J)
08:	TV_MODE[1]	
09:	TV_MODE[2]	
10:	PCI_DEV[0]	SET BY BIOS
11:	PCI_DEV[1]	
12:	PCI_DEV[2]	
13:	PCI_DEV[3]	DEFAULT=0x0
14:	FB_SIZE[0]	DEFAULT=0x0 (256MB ??)
15:	FB_SIZE[1]	
16:	FB_SIZE[2]	
17:	PEX_FLL_EN_TERM100	DEFAULT=0x0 (ENABLED)
18:	3XIO_PAD_CFG_LUT_ADDR[0]	DEFAULT=0x0 (DESKTOP_DEFAULT)
19:	3XIO_PAD_CFG_LUT_ADDR[1]	
20:	3XIO_PAD_CFG_LUT_ADDR[2]	
21:	3XIO_PAD_CFG_LUT_ADDR[3]	
22:	ROMTYP[0]	DEFAULT=0x1 (AT25)
23:	ROMTYP[1]	
24:	USER[0]	SET BY BIOS
25:	USER[1]	
26:	USER[2]	
27:	USER[3]	
28:	PCI_DEV_EXT	DEFAULT=0x0

STRAP BITS BOOT3 = 0x10100C

NR.	USAGE	COMMENT
06	XCLK_555	DEFAULT=0x0
16	PC_LJOBAR	DEFAULT=0x1 0=DISABLE, 1=ENABLE

CFG	Config With	Vendor
0000	Reserved	
0001	16Mx32 512-bb Qimonda	
0010	16Mx32 512-bb Hynix*	
0011	16Mx32 512-bb Samsung*	
0100	Reserved	
0101	32Mx32 512-bb Qimonda	
0110	32Mx32 512-bb Hynix	
0111	32Mx32 512-bb Samsung	
1000	Reserved	
1001	16Mx32 448-bb Qimonda	
1010	16Mx32 448-bb Hynix	
1011	16Mx32 448-bb Samsung	
1100	Reserved	
1101	32Mx32 448-bb Qimonda	
1110	32Mx32 448-bb Hynix	
1111	32Mx32 448-bb Samsung	



Micro-Star International Co., LTD.

Size	D
Custom	

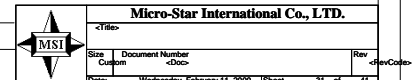
Size	Document Number
Custom	<Doc>

Date: Wednesday, Feb 22, 2012 12:00 PM

Rev	RevCode
-----	--------------------

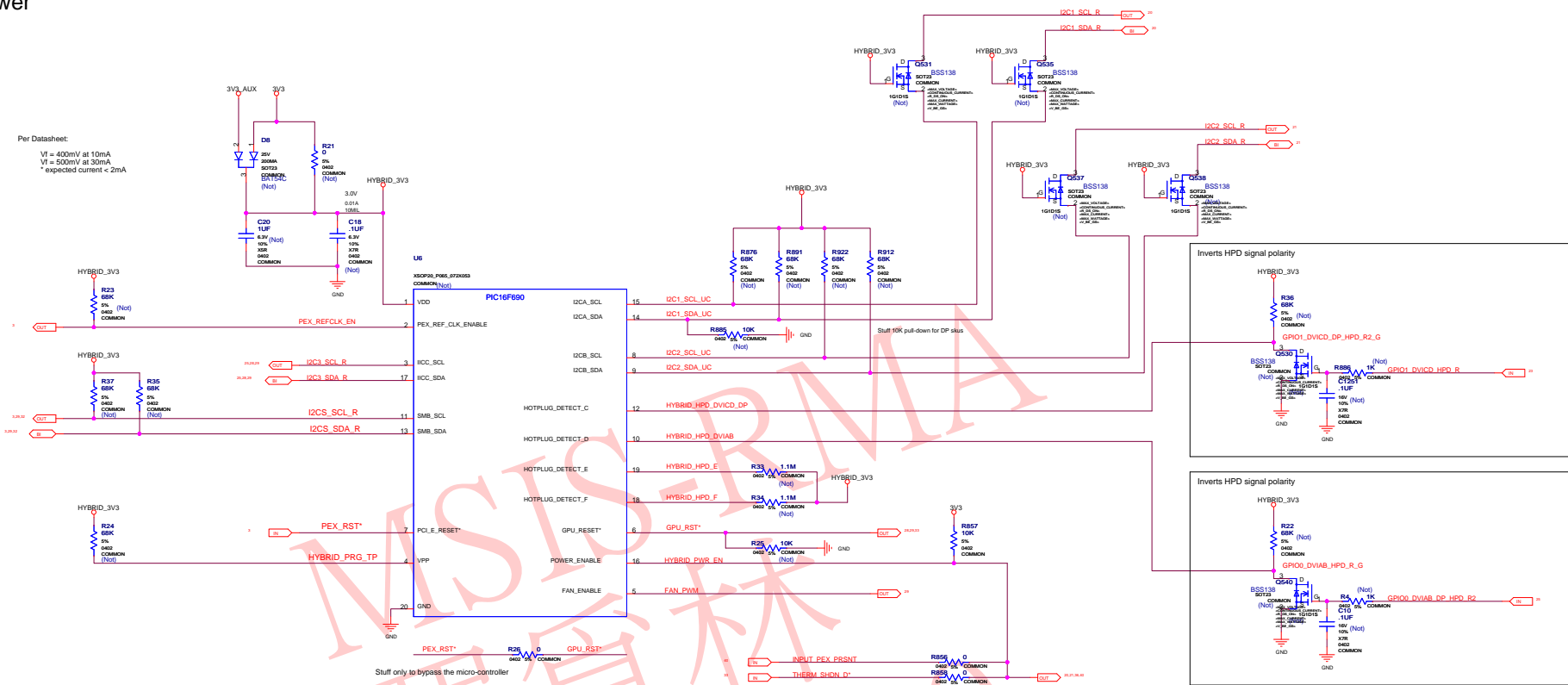
41	
----	--

NVIOx SECTION GND



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power and GND (GPU and NVIOx)

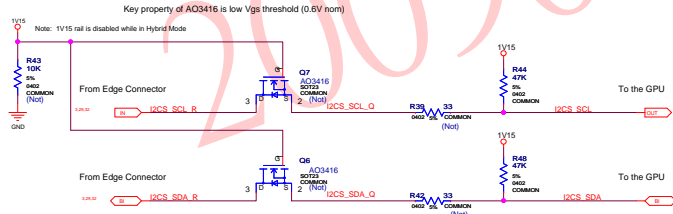
Power: Hybrid Power



I2CS Isolation for Hybrid Power and Level Shifting(3.3V to 1.15V)

Isolates SMBus to the GPU when in Hybrid mode

GT200 I2CS lanes are 1.2V tolerant signals



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FIN
PAGE DETAIL	Power: Hybrid Power



Micro-Star International Co., LTD.

Size	Document Number
------	-----------------

Custom <Doc>

Rev		
-----	--	--

the codes

41

Power Supply: 2V5, DP_PWR, 8V5 1V15 (PEX_VDD, GV_VDD)

2V5

2V5 @ 1.7A

V_o_typ=V_{ref}_typ=2.495
V_o_max=V_{ref}_max=2.545
V_o_min=V_{ref}_min=2.445

DP Dongle Supply

3.3V @ 500mA

8V5 11/21:remove 8V5 circuit

1V15 (PEX_VDD AND GV_VDD/Q) and 1V8(For Analog)

1V8 @ 0.032A

V_{ref}=0.8V
V_o_Typ=0.811*(1+0.808%)+1.792V
V_o_Max=0.782*(1+1.199%)/(0.808%+101%)=1.737V
V_o_Min=0.816*(1+1.101%)/(0.808%+99%)=1.849V

V_{ref}=0.8V
V_o_Typ=0.811*(1+0.808%)+1.162V
V_o_Max=0.782*(1+1.199%)/(0.808%+101%)=1.143V
V_o_Min=0.808*(1+1.101%)/(0.808%+99%)=1.181V

PEX_VDD, GV
1V15 @ 6A

PEX / GV 1V15
Local Capacitance at Supply 377 uF
Combined Distributed Capacitance 112 uF
Total 1V15 Capacitance 489 uF

ASSEMBLY PAGE DETAIL
S136 LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 310FF ASSEMBLY NOTES AND BOM NOT FINAL
Power Supply: 2V5, DP_PWR, 1V15 (PEX_VDD, GV_VDD)

MSI

<Title>

Size

Date

Document Number

Wednesday, February 11, 2009

<Doc>

34 of 41

Micro-Star International Co., LTD.
Rev
Rev Code

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTIC LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

Power Supply: Combined FBVDD/Q

FVBDDQ ENABLE

NVDD_PG000 >> NVDD_PG000

12V Driver -> R7301:0 ohm, R7300:NC ohm
9V Driver -> R7301:NC, R7301:0 ohm

11/19 modify 12V to 12V_Pex6_F1

2/9 remove R7304 and R7315
N-NTMFS4841NHT1G_S08-RH

FBVDDQ = 1.9-2.0V @ 31A~35A

FBVDDQ Power Supply


FBVDDQ = 1.9~20V @ 31A~35A

FB VOLTAGE SENSE

$0.6 V \times (1 + R_{top} / R_{bot})$
 $2.057V = 0.6 V \times (1 + 2.55K / 1.05K)$
 $1.833V = 0.6 V \times (1 + 2.55K / 1.24K)$
 $1.93V = 0.6 V \times (1 + 2.55K / 1.15K)$

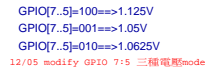
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTIC LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY PAGE DETAIL
MAX LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Power Supply: Combined FBVDDQ

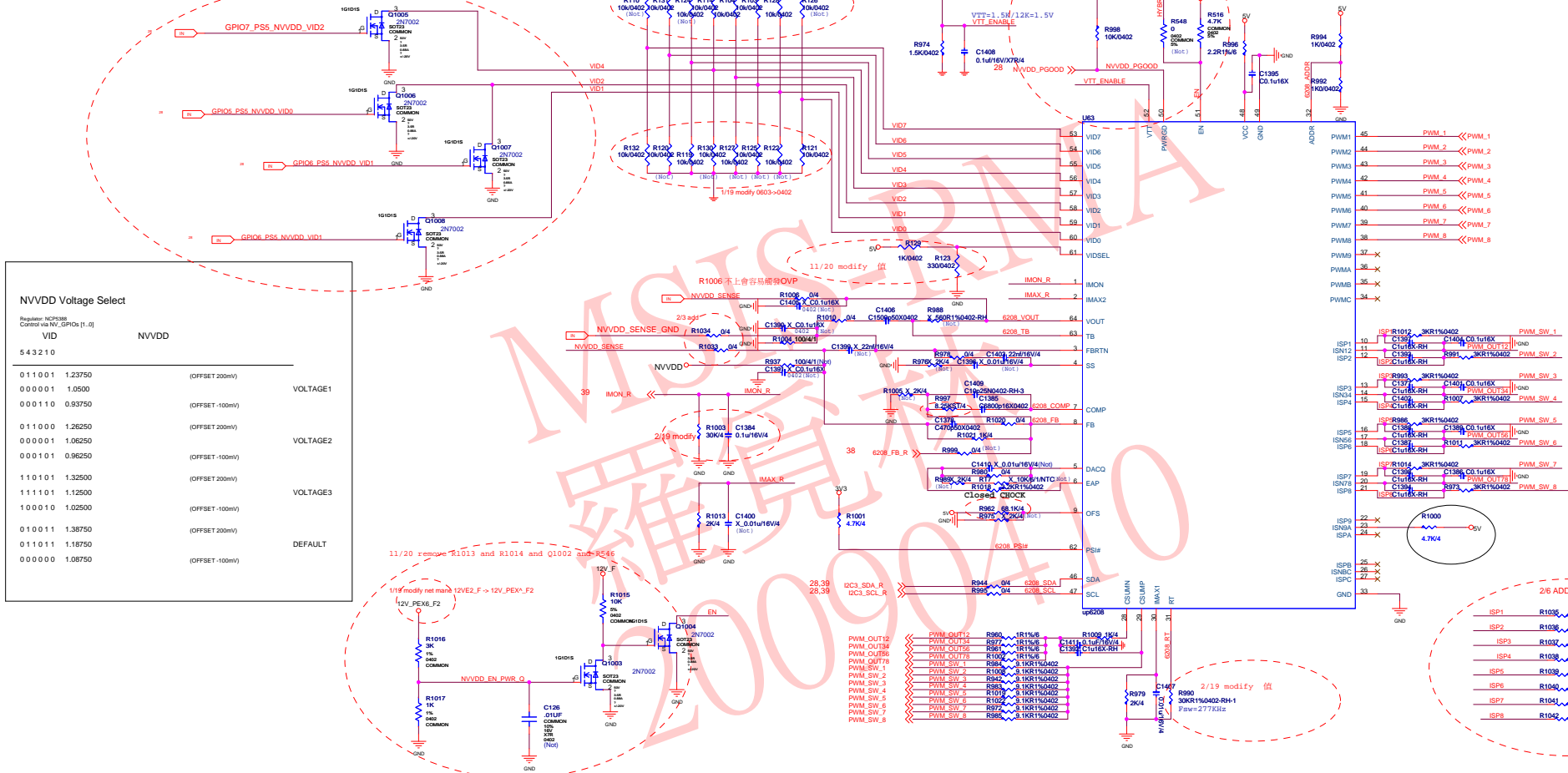


Micro-Star International Co., LTD.
Size Custom
Document Number <Doc>
Date: Wednesday, February 11, 2009 Sheet 35 of 41

Power Supply: NVVDD Regulator



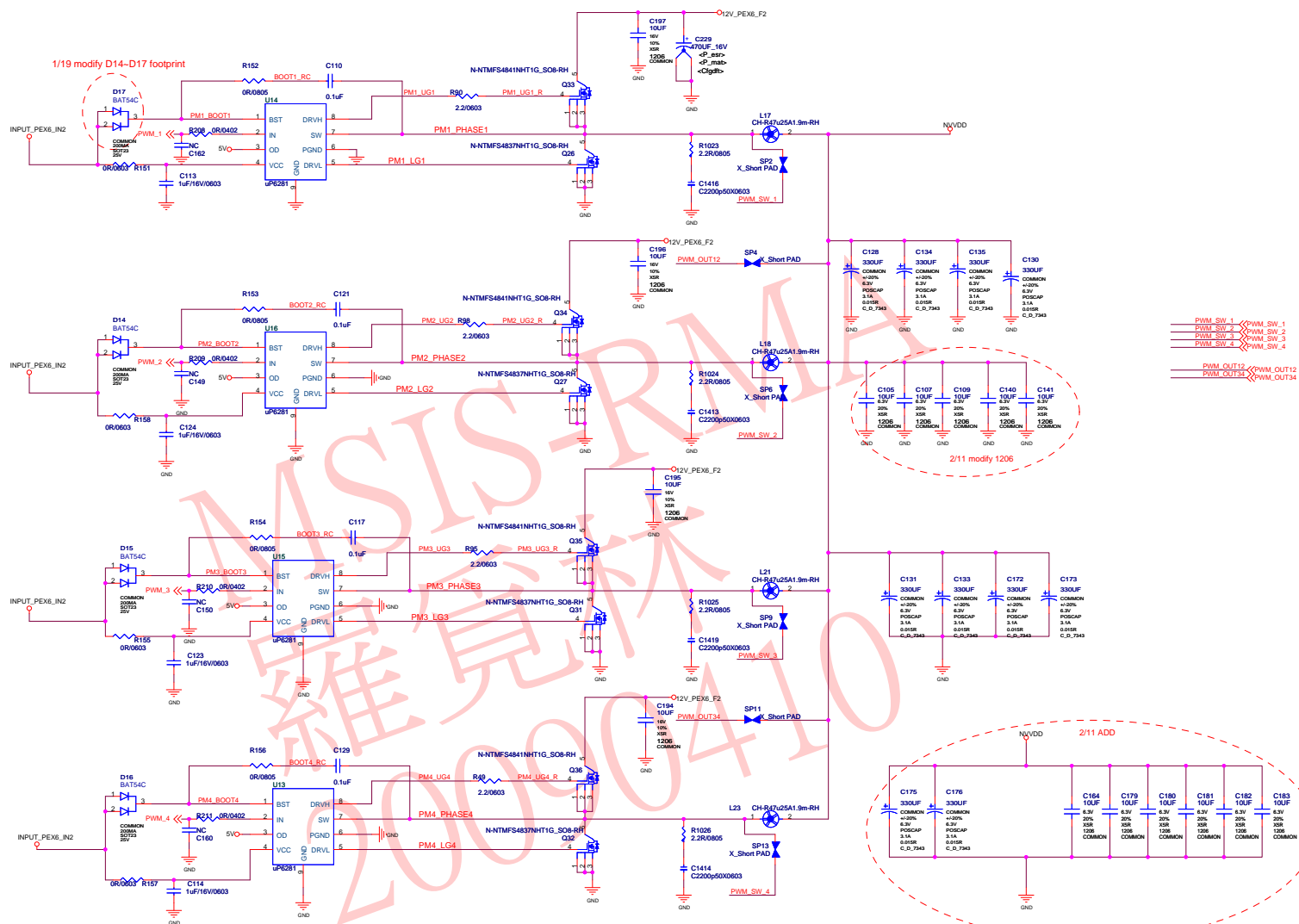
1/19 modify net mane ~~12VE2_F~~ -> 12V_PEX6_F2



2/6 ADD

ISP1	R103 ₆	(Not) RKR104002	PWM_OUT12
ISP2	R103 ₆	(Not) RKR104002	PWM_OUT12
ISP3	R103 ₆	(Not) RKR104002	PWM_OUT34
ISP4	R103 ₆	(Not) RKR104002	PWM_OUT34
ISP5	R103 ₆	(Not) RKR104002	PWM_OUT56
ISP6	R104 ₀	(Not) RKR104002	PWM_OUT56
ISP7	R104 ₁	(Not) RKR104002	PWM_OUT78
ISP8	R104 ₂	(Not) RKR104002	PWM_OUT78

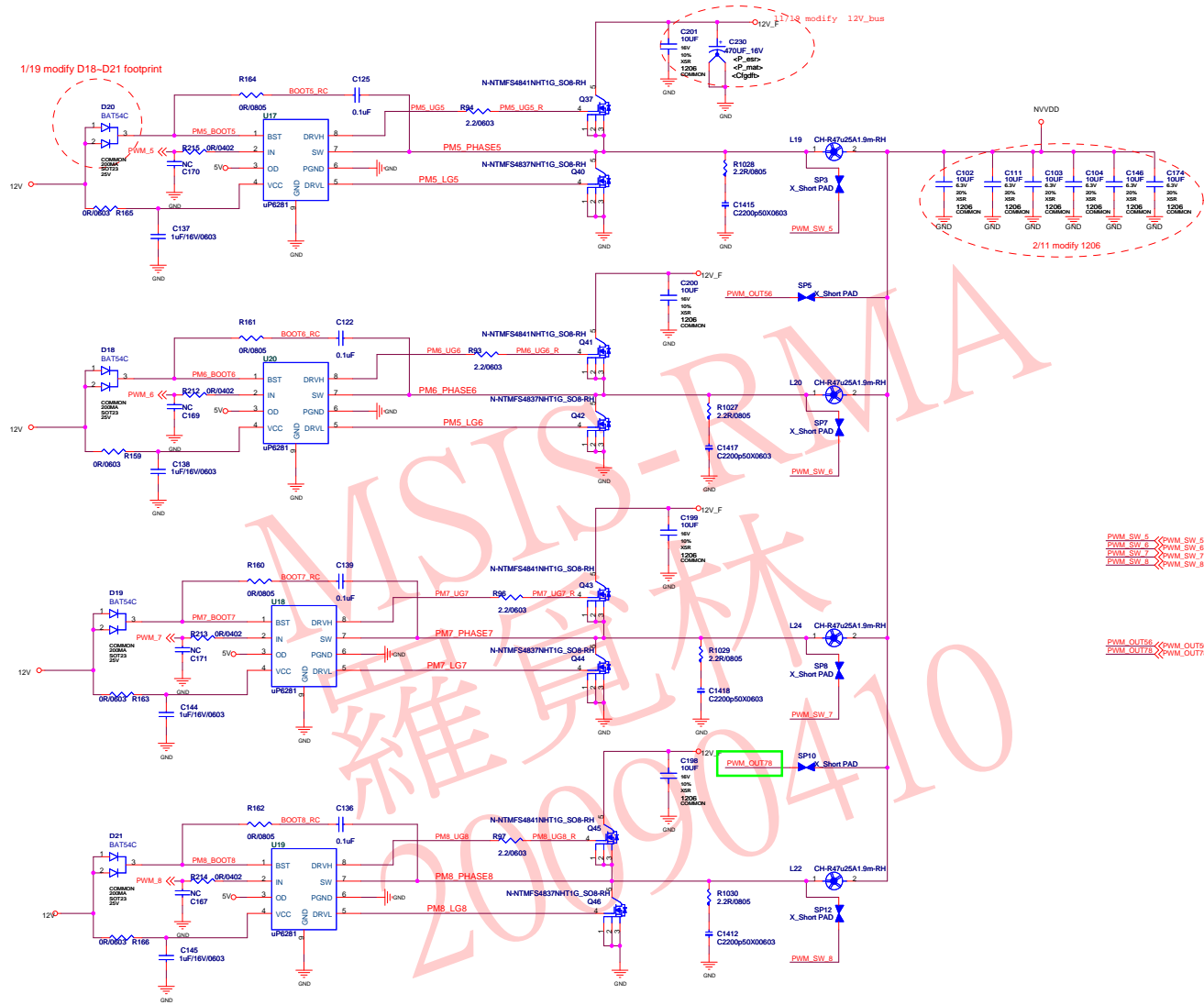
Power Supply: NVVDD Phase 1,2 powered from external PEX 6PIN



The diagram shows the 48VDC input connection. On the left, four horizontal lines represent the input wires. The top two lines are labeled 'PWM_SW_1' and 'PWM_SW_2'. The bottom two lines are labeled 'PWM_SW_3' and 'PWM_SW_4'. On the right, four horizontal lines represent the output wires. The top two lines are labeled 'PWM_OUT12' and 'PWM_OUT34'. The connections are as follows: the top input line connects to the top output line, the second input line connects to the second output line, the third input line connects to the third output line, and the bottom input line connects to the bottom output line.

The schematic diagram illustrates the 2P11 ADD circuit. A 6X4 vacuum tube is shown with its grid connected to the 2P11 ADD input. The tube has six anodes, each with a 330kΩ resistor (C176) and a 100μF capacitor (C164-C183) connected to a common cathode. The cathode is connected to ground through a 100kΩ resistor (C.D. 749).

Power Supply: NVVDD Phase 5~8 powered from internal PEX edge connector



```
PWM_SW_5 <-- PWM_SW_5
PWM_SW_6 <-- PWM_SW_6
PWM_SW_7 <-- PWM_SW_7
PWM_SW_8 <-- PWM_SW_8
```

PWM_OUT56 >> PWM_OUT5
PWM_OUT78 >> PWM_OUT7

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 3-4 of 4



Micro-Star International Co., LTD.

	<Title>
--	----------------------

Size	Document Number
------	-----------------

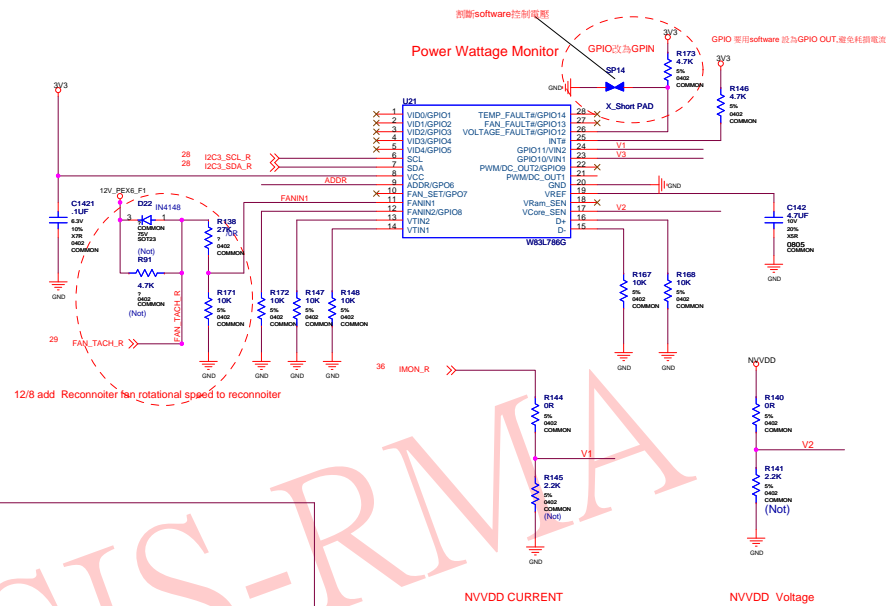
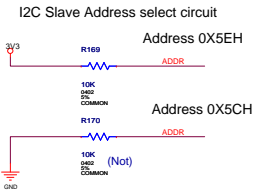
Custom <Doc>
Date: Wednesday, Feb

ev		
----	--	--

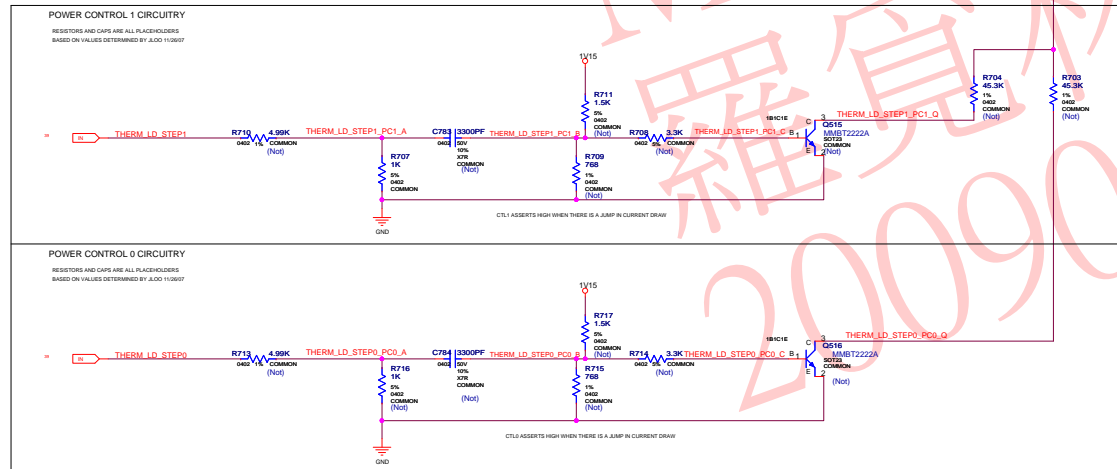
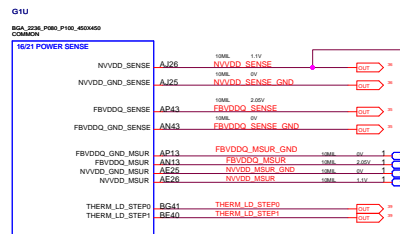
<RevCode>	
41	

[illegible]

Power Supply: NVVDD power control

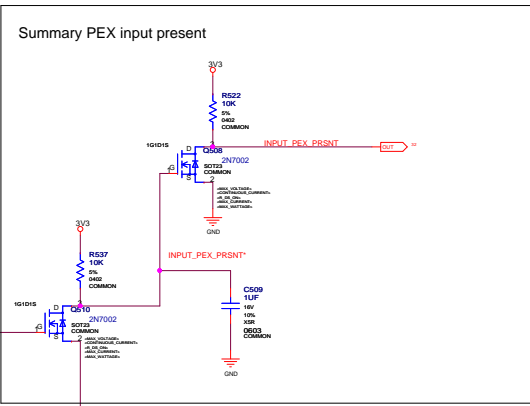
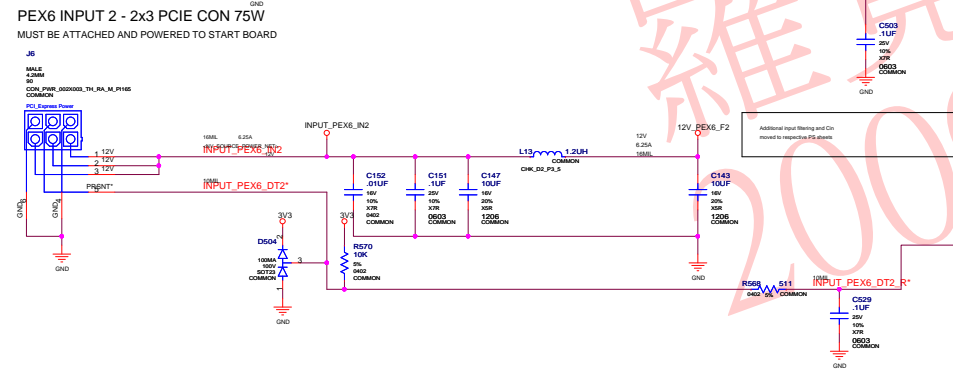
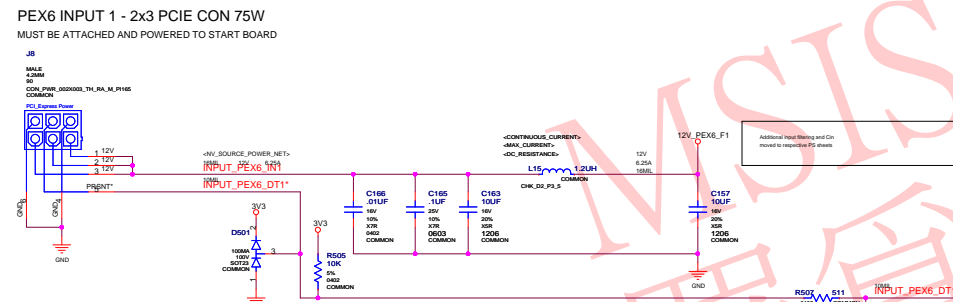
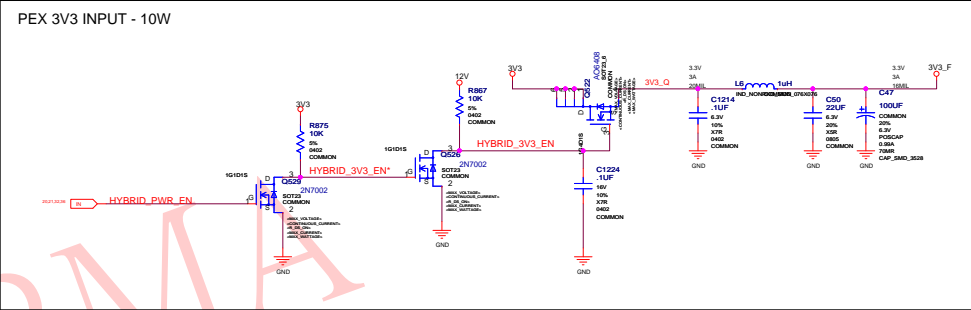
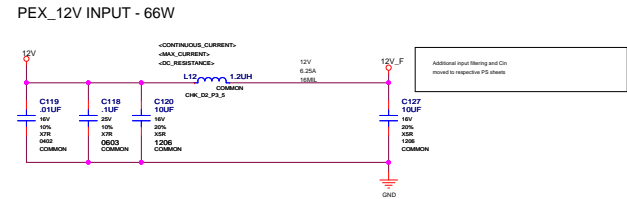


NVVDD & FBVDDQ SENSE/MSUR



Power: Input Rail Filter and Detection Logic

Connector Power State Table			
J33 Connector	J33 Connector	Power	STATE
Connected	Connected	225W	Full Post
Connected	Not Connected	105W	Board Off
Not Connected	Connected	105W	Board Off
Not Connected	Not Connected	75W	Board Off



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY
PAGE DETAIL
BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_310FF ASSEMBLY NOTES AND BOM NOT FINAL
Power: Input Rail Filter and Detection Logic

Micro-Star International Co., LTD.

Size: Custom
Document Number: <Doc>
Date: Wednesday, February 11, 2009
Sheet: 40 of 41

Thermal/Mechanical/ID

Bracket and Assembly

MEC1
MEC_SCREW_PN1
COMMON
MEC502
MEC_SCREW_JACK
COMMON
MEC503
MEC_SCREW_JACK
COMMON
MEC501
MEC_SCREW_JACK
COMMON
MEC504
MEC_SCREW_JACK
COMMON

GPU Socket

BGA SOCKET ASSY
8 connected mounting pins
MEC13
BKT_MGA_POGO_488X480_PN10_HIS
COMMON

GPU Stiffener

BOARD STIFFENER
7 connected mounting pins
MEC12
BKT_MGA_OT200GPU_T_ST_1
COMMON

NVIOx Socket

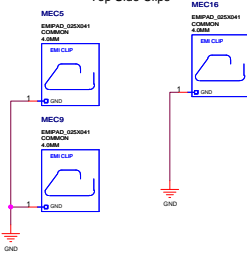
BGA SOCKET ASSY
4 connected mounting pins
MEC6
BKT_MGA_POGO_238X230
COMMON

Hockey Stick Retention Mechanism

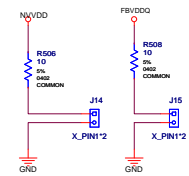
SPECIAL MECHANIC
No connected mounting pins
MEC2
MECH_PEL_BREAKOFF_RETENTION_PN01
COMMON

EMI Gnd Clips

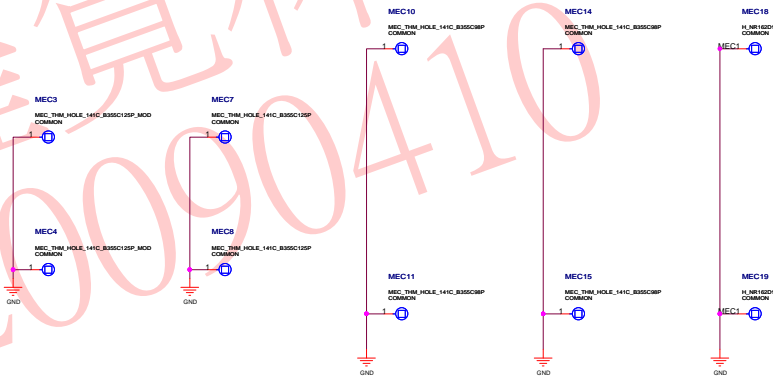
Top Side Clips



電源量測點



THERMAL/MECHANICAL HOLES



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY
PAGE DETAIL
BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
Thermal/Mechanical

Micro-Star International Co., LTD.			
<Title>			
Size	Document Number	Rev	
Custom	<Doc>	<RevCode>	
Date:	Wednesday, February 11, 2009	Sheet	41 of 41