NV25, P80, DUAL DAC/TMDS, 128MB 4MX32 BGA DDR, TV IN/OUT, GOGGLES, AGP

P80-A00: Based on P53-A00.

A00-X00:

Populate R1034 with 0.01 Ohm
Populate 68R parallel terminations on FBCLK/CLK#

A00-X01:
Isolated GND, AGND and Chassis GND
Corrected Multichip Strap
Changed sync buffers inputs from pin 2 to pin 1 for easy probing.
Corrected PWRGD_FBVDD on memory PS

A00-X02:
Combined CX and SA power filters.
Connected memory PS bootstrap to 12V.
X0R Hotplugs to GPIO1
Isolated PLL_VDD from 3.3VL to get rid of 350mV stray voltage.
Combined GND, AGND and Chassis GND

A00-X03
Changed both TMDS digital powers from 3.3V to 3.3VL.
Added a resistor to Base transistor PLL_VDD sequencer.
Added 2nd fan connector.
Added various placement and routing notes.

P80-A01:

A02-X00
Fixed serial rom connections.
Added, again GND isolations.
Added testpoints to various (SAA7108) pins.
Changed DVO clocks series termination to 10R.

A02-X01
Moved VGA con and Bracket to new Sheet 3.2
Moved SROM to new Sheet 5.2
Moved SROM to new Sheet 5.2
Moved SEC-DVI Connector to Sheet 6.5
C1262, R1129 Changed to No stuff.
131-60102-0063-02 is SUB for 131-10102-0061-006
R1072 is changed to 2.2K from 1.5K, Put in BOM.
R1204(Nostuff), R1205-0R Added for FBVDDQ Power sequence after 3.3VL
R207 Changed from 118R to 105 Ohm
R927 Changed from 118R to 102 Ohm
C1405, C1406 Value changed to 330uf

A02-X02
Design file under Perforce Control.
Changed DACA IDUMP resistor to 0402pkg

A02-X03
Turned DACA SYN buffers into "analog" to ease the AGND antietch.
Added 5 caps on VDDDVO pins.
Changed R1116 to 0402 pkg.
Enabled AGP Fast Write.
Changed PS snubber's resistor to 2.2R (from 100R) per Semtech recommendation.

A02-X04
Combined FCCDDCPWRVGA and DDC+5V nets (del. L711 and C1116) for ease of routing.

A02-X05
Changed R1115 and R1116 back to SMD0603

A02-X06
Isolate SC1175 and SC1102 AGNDs per Semtech recommendations.
Removed 5V power option from SC1102.
Changed crystal loading caps to 10pF and have them reference to digitial GND.

A02-X07
Changed snubber resistors to 0805 pkgs
Added Rc to SC1102 VREF pin (NO_STUFF)
Removed extra X elements.
A02-X10
Added a 2A fuse on 12V input due to SC1102 current limit bug.
A02-X11
Added ICT to MCHIP_RST_ (GPU_AK5)
Removed SMD0805_SHORT symbols from PS pages (nets merged to GND)

P80-A03: Re-spin

A03-X00

Add two 5-3.0 VR for DVOA and B BUS power supply and change Flash Rom power to DVOA_PWR (3.0V) on Page 6.1

Change the decoupling cap. C1349,C1350,C1351,C1362,C907 connect to DVOA_PWR from 3.3V on page 5.1

Change the decoupling cap. C1443,C1444,C1445,C1446,C920 connect to DVOA_PWR from 3.3V on page 5.1

Change series P-ROM U505 power to DVOA_PWR (3.0V) on page 5.2

Change GPU pin AH1,AD1,AC7 connect to DVOA_PWR and change GPU pin AH15,AP8,AP12 connect to DVOB_PWR on Page 6.0.

Connection AGND to GND on page 3.1

Remove R1179,R1180,R1183,R1184,R1198,R1199,C1447

Change R1196,R1197 to "NO STUFF" on page 3.2

P80-A04: Schematics For P Release

A04-X00

Put NO_STUUF for C1123, C1126, C1129, C304, C307, C310

Replace C303, C306, C309, C1122, C1125, C1128 with CAP NPO 0603 15PF 16V 5% (035-20150-0006-000)

Replace L715, L717, L719, L300, L305, L309 with IND 0805 MTLR 5% 0.068UH (130-30680-0006-000)

Replace L716, L718, L720, L302, L306, L310 with IND 0603 MTLR 5% 0.068UH (130-20680-0006-000)

A04-X01

Change C29, C30 value from 33PF to 27PF to improve the color burst stability for conexent and philips TV chip

Change R23 to 12 Ohm from 1K Ohm

A04-X02

Clean up the page number

A04-X03

Clean up the Sch. part description dismatch with the BOM

MS-8875-00A:

A00-X00

*based on P80-A04-X03.
*I/O function modify (Dual D-sub,TV-out,Video capture.

1. .from 3.1 DAC-I2C0--Pri(page7) change to MS-8863 3.c DAC_A.
2. 3.2 VGA CON, BRACKET(page 8) remove P300.
3. remove page
   a. 5.2 S-ROM(page 16)
   b. 6.1 DVOA EXT. TMDSA PRI(page 18)
   c. 6.2 DVOA EXT. TMDSA I/O PRI(page 19)
   d. 6.3 DVOB EXT. TMSB SEC(page 20)
   e. 6.5 DVOB/DACA CONNECTOR(page 22)
   f. 7.1 TV-CX ENCODER(page 23)
4. 6.0 DVOA/B(page 17)
   a. remove U822,R1174,R1175.
   b. DVOCLKOUT add cap pulldown 10PF/C1175 for EMI.
5. 7.2 TV-PH CODEC(page 24)
   a. COUT and YOUT and CVBSOUT add D2,D4,D6 2.7UH indutor
   b. ADD 3.3V to VAAD3.3 and 3.3V to AA3.3V transducer from 7.1 TV-CX ENCODER(page 23).
   c. ADD R701 ENC_DVO_CLKO form (page 23).
   d. DVOCLK_IN add cap pulldown 10PF/C1174 for EMI.

*POWER function cahnge list

1. 5.1 P-ROM(page 15) from U824&U825(FAN2500S) change to (AMS1117).
2. 8.1 NVVDD POWER SUPPLY(page 26)& 8.2 MEM POWER SUPPLY
   a.IRU3007 to supersede U813(SC1175)&U816(SC1102)&U819(SC1565).
   b.cahnge all power SMT check by DIP one.
   c. remove U815(US1150)

A00-X01

1. page 10,11,12,13
   R425-R428 & R453-R456 from 10K cahnge to 1K.
2. page 7, modify some References.
3. page 20 a. add HIP6019 dual-lay circuit.
   b. add IRU3007 preserve "FBVDDQ" circuit.
   c. modify some References.
4. page 2 add RE1 & CE1 by pass for EMI(close GPU).
5. page 8 add CE2-CE17 for EMI
6. page 4 Remove J202 & J201
7. page 20 "FBVDD" & "FBVDDQ" swap.

A00-X02

1. page 2 add "PCIRST" not gate(7414).
2. page 20 add power sequence.
3. page 8 add "EMI" cap.

COMMON -- ALL
NO_STUFF - NOT STUFFED
PRI_VGA - Primary VGA Support
PRI_DVI - Primary DVI-D (Digital) Support
PRI_DVI_I - Primary DVI-I - (Digital & Analog) Support
SEC_DVI_I - Secondary DVI-I (Digital & Analog) Support
PRI_PROT - Primary DVI-VGA protection diodes.
SEC_PROT - Secondary DVI-I protection diodes
MEM128 - 128MB EXTENDED MEMORY

NO_STUFF FOR FIRST BUILD
ROM_SER - Serial ROM used
ROM_PAR - Parallel ROM used.

STEREO - USED FOR STEREO GOGGLES
STEREOSYNC1 - USED FOR STEREO GOGGLES
STEREOSYNC2 - USED FOR STEREO GOGGLES
STEREOSYNCS - USED FOR STEREO SYNC BUFFERS
SAA8 - PHILIPS ENCODER/DECODER SAA7108
SAA2 - PHILIPS ENCODER SAA7192
CX - CONEXENT ENCODER CX25871

NO_STUFF FOR FIRST BUILD

EZ1586 - USED TO REGULATE FBVDDQ FROM FBVDD - LINEAR
SC1102 - USED TO REGULATE FBVDD FROM 12V - SWITCHER
SC1565 - USED TO REGULATE 3.3VL FROM 3.3V - LINEAR
SC1175 - USED TO REGULATE NVVDD FROM 3.3V AND 5V - SWITCHER

NO_STUFF FOR FIRST BUILD

PS_SEQ - USED FOR POWER SUPPLY SEQUENCE PROTECTION

VGA-TV-DVI - Used for Primary VGA / TV / Secondary DVI
VGA-DVI - Used for Primary VGA / Secodary DVI only
VGA-TV - Used for Primary VGA / TV
VGA - Used for Primary VGA only
DVI-TV-DVI - Used for Primary DVI / TV / Secondary DVI
DVI-DVI - Used for Primary DVI / Secondary DVI Only
DVI-TV - Used for Primary DVI / TV
DVI - Used for Secondary DVI
PASSIVE_HS - Used for Passive heat sink
FAN_HS - Used for Fan heat sink
SOCKET - PARTS REMOVED WHEN USING A SOCKET

0. TOP PAGE

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

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MS-8875 based on P80-A04

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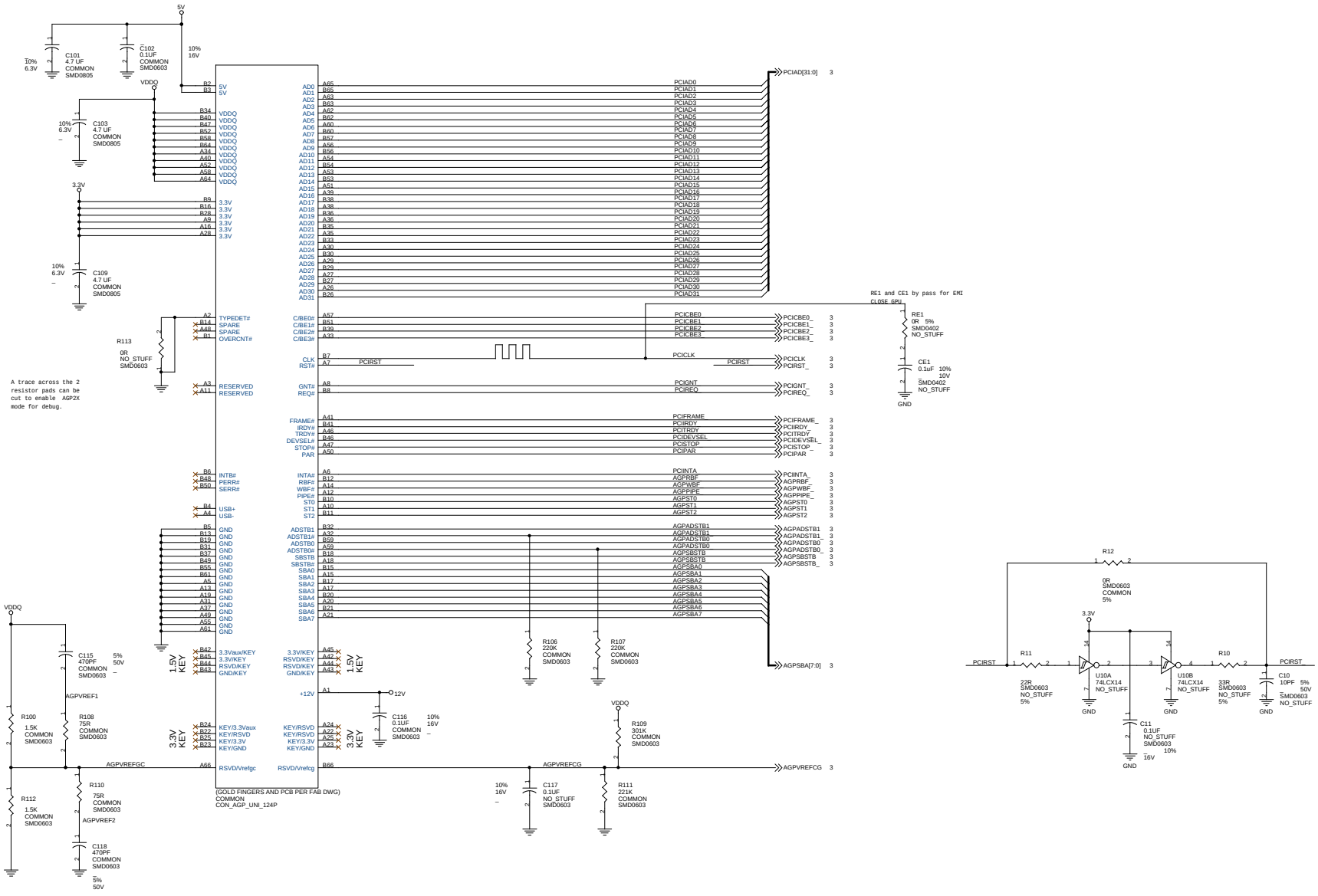
Date: Monday, March 25, 2002 Sheet 1 of 20



1.1 BUS I/O

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

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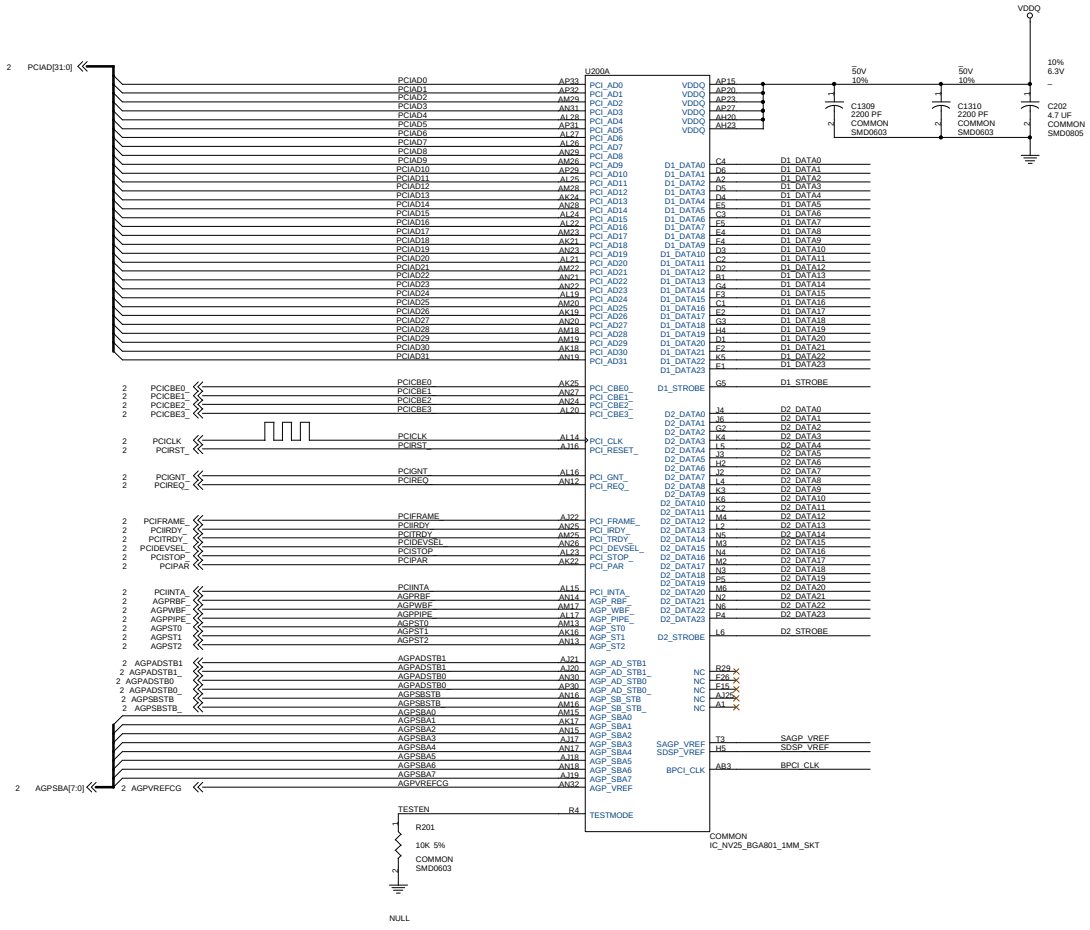

2.1 NV HOST IF

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

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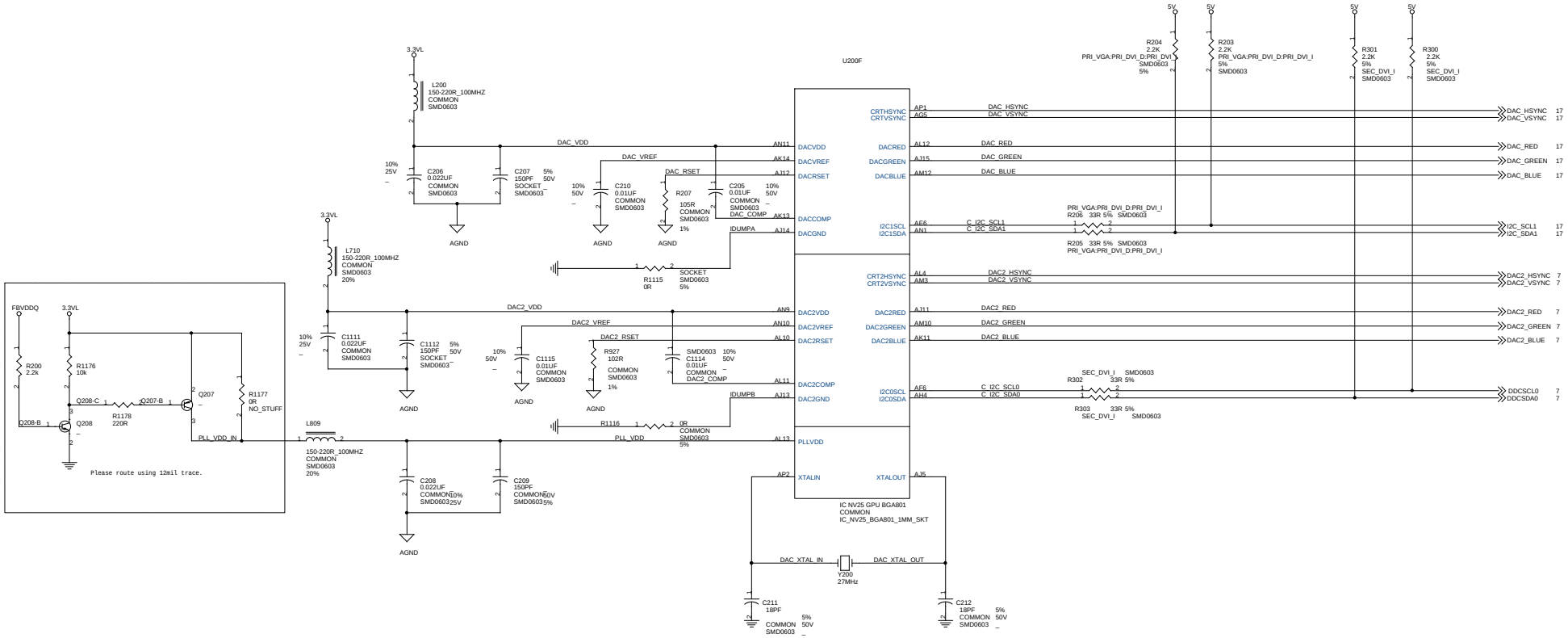
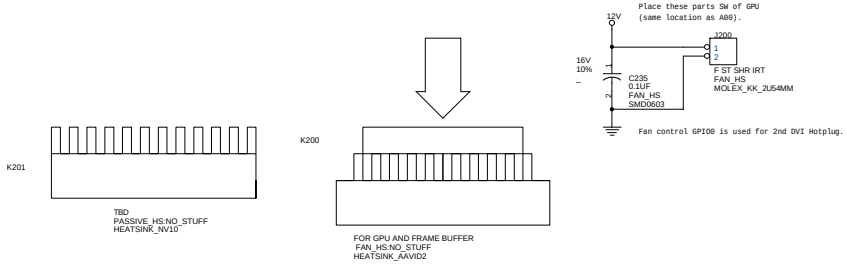


Use thick (non-impedance controlled) traces on XTALIN/OUT



2.2 NV DAC/PLL/I2C

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

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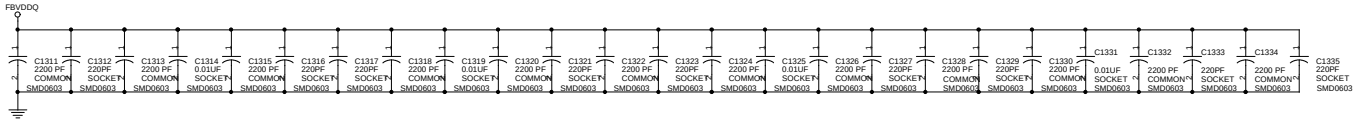
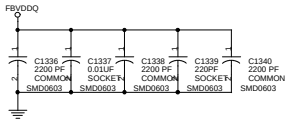
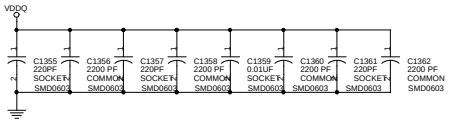
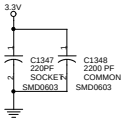
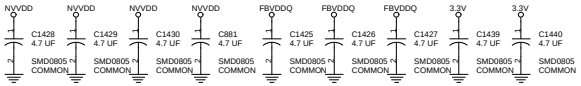




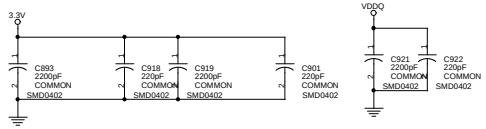


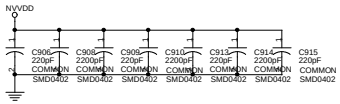


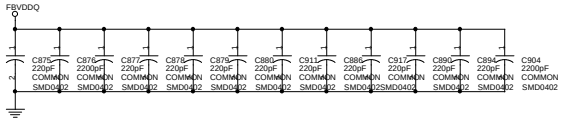
TOP SIDE CAPS

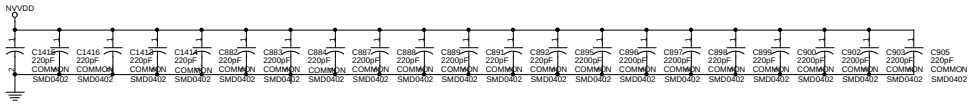


BOT SIDE CAPS









2.3 NV DECOUPLING

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

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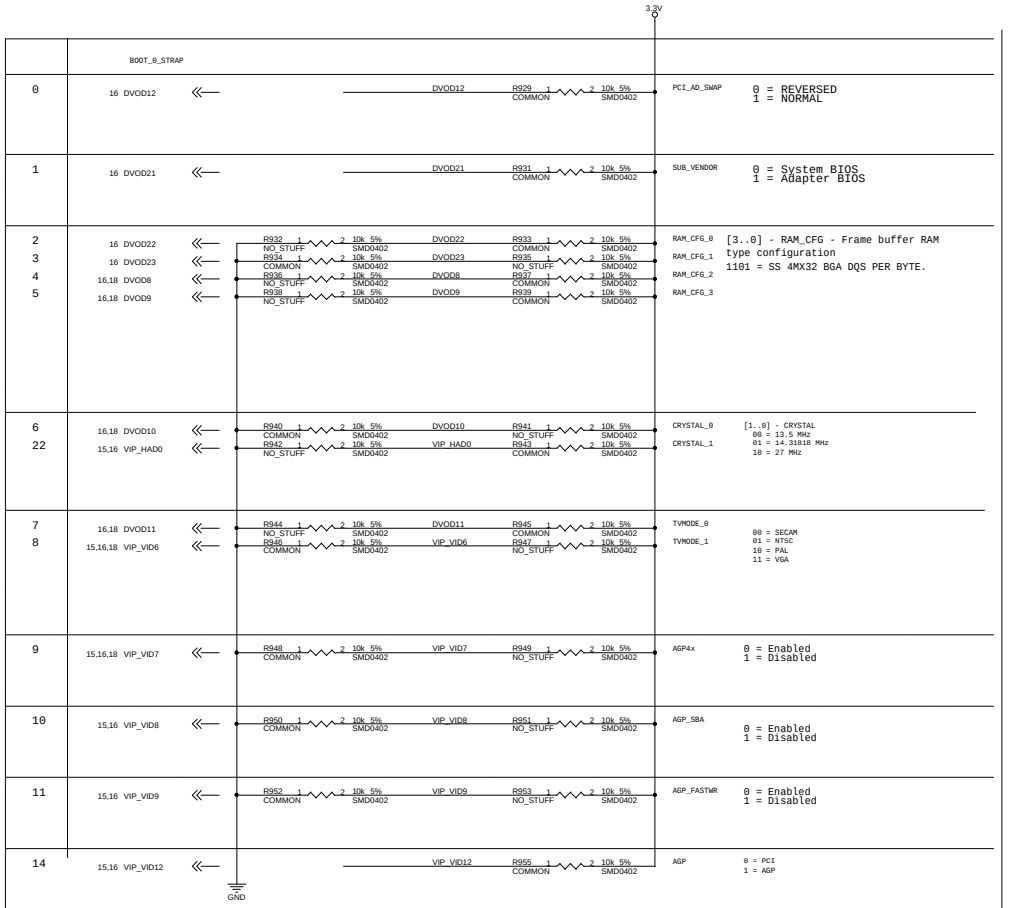
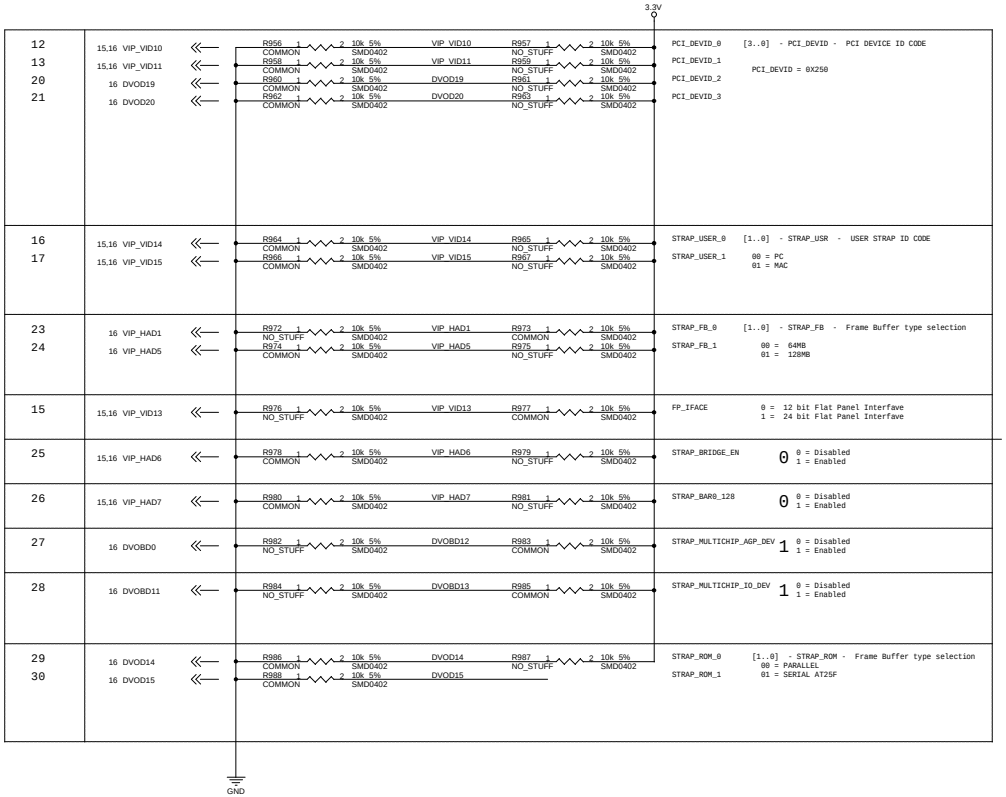
NV25 BOOT STRAP REGISTER

[1..0] - TVMODE

0 =
Enabled





15,16,18 DVOD[23:0] >> DVOD[23:0]
16 DVOBD[23:0] >> DVOBD[23:0]
15,16,18 VIP_VID[15:0] >> VIP_VID[15:0]

3.0 NV STRAP

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

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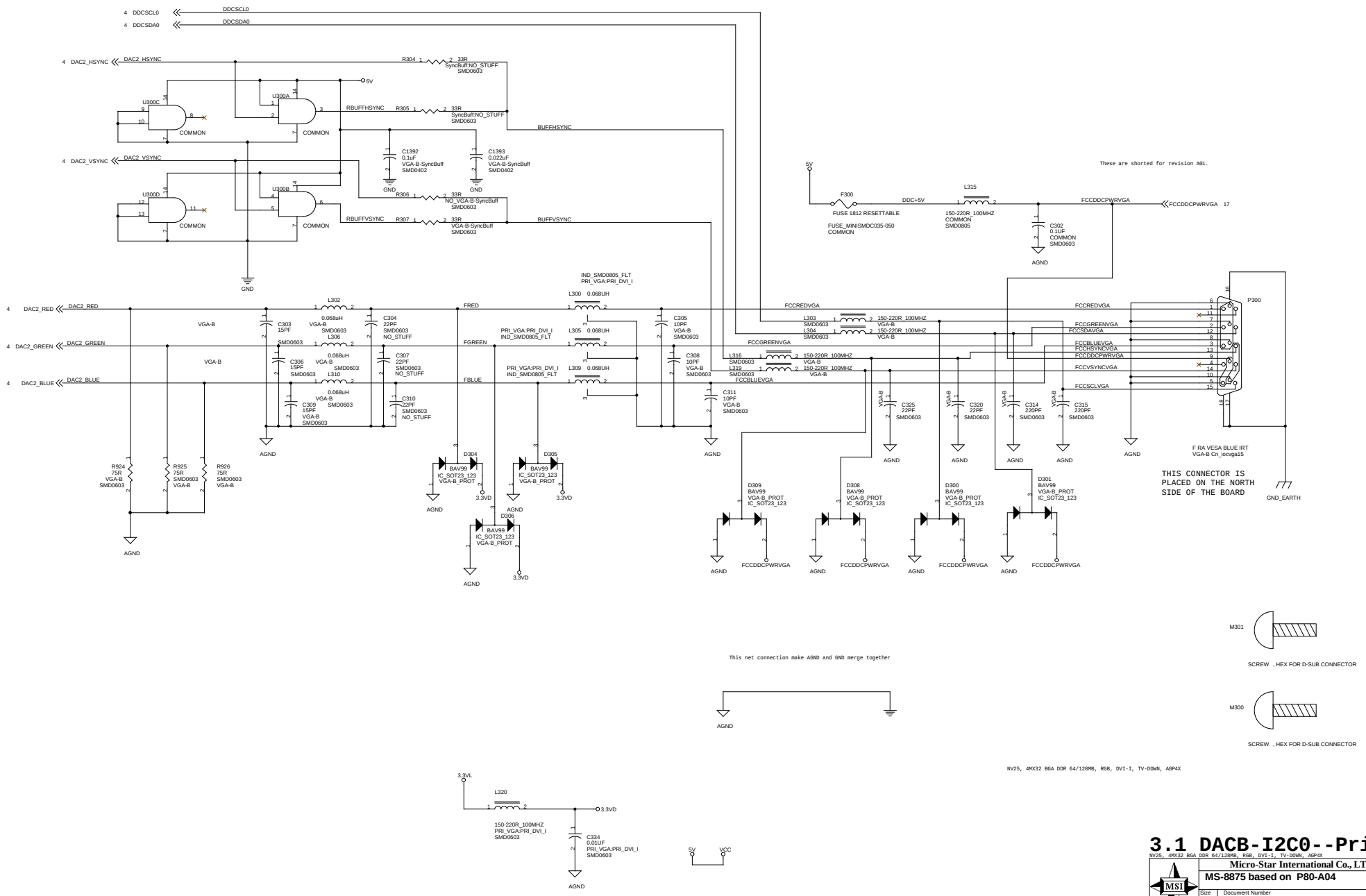

3.1 DACB-I2C0--Pri

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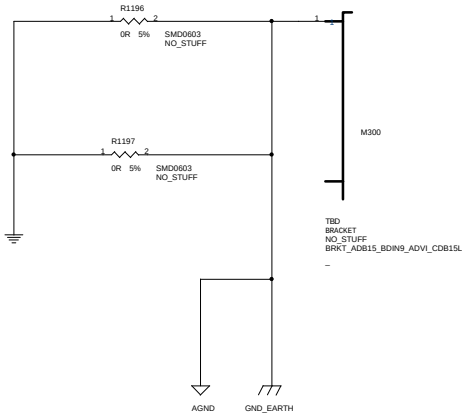
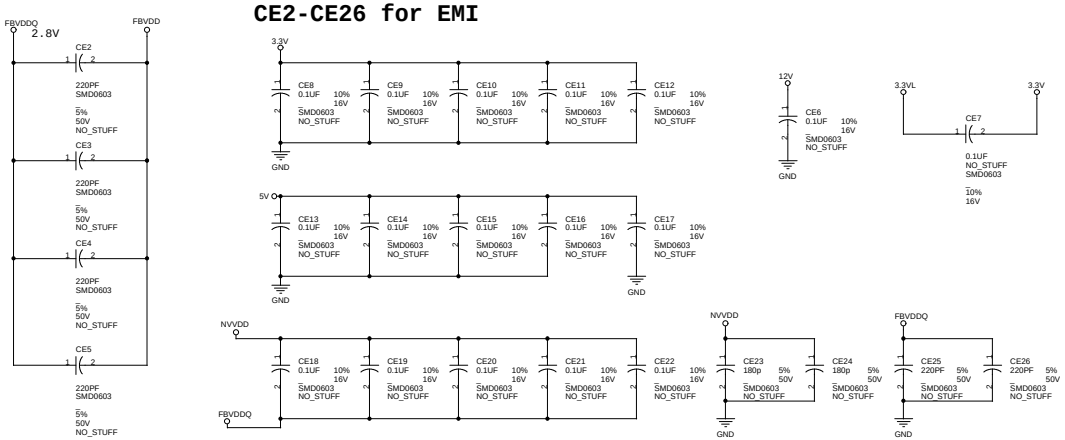
Single point connection for
digital and chassis GND.



VGA-TV-DVI - Used for Primary VGA / TV / Secondary DVI

DVI-TV-DVI - Used for Primary DVI / TV / Secondary DVI

CE2-CE26 for EMI



3.2 BRACKET & EMI cap

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

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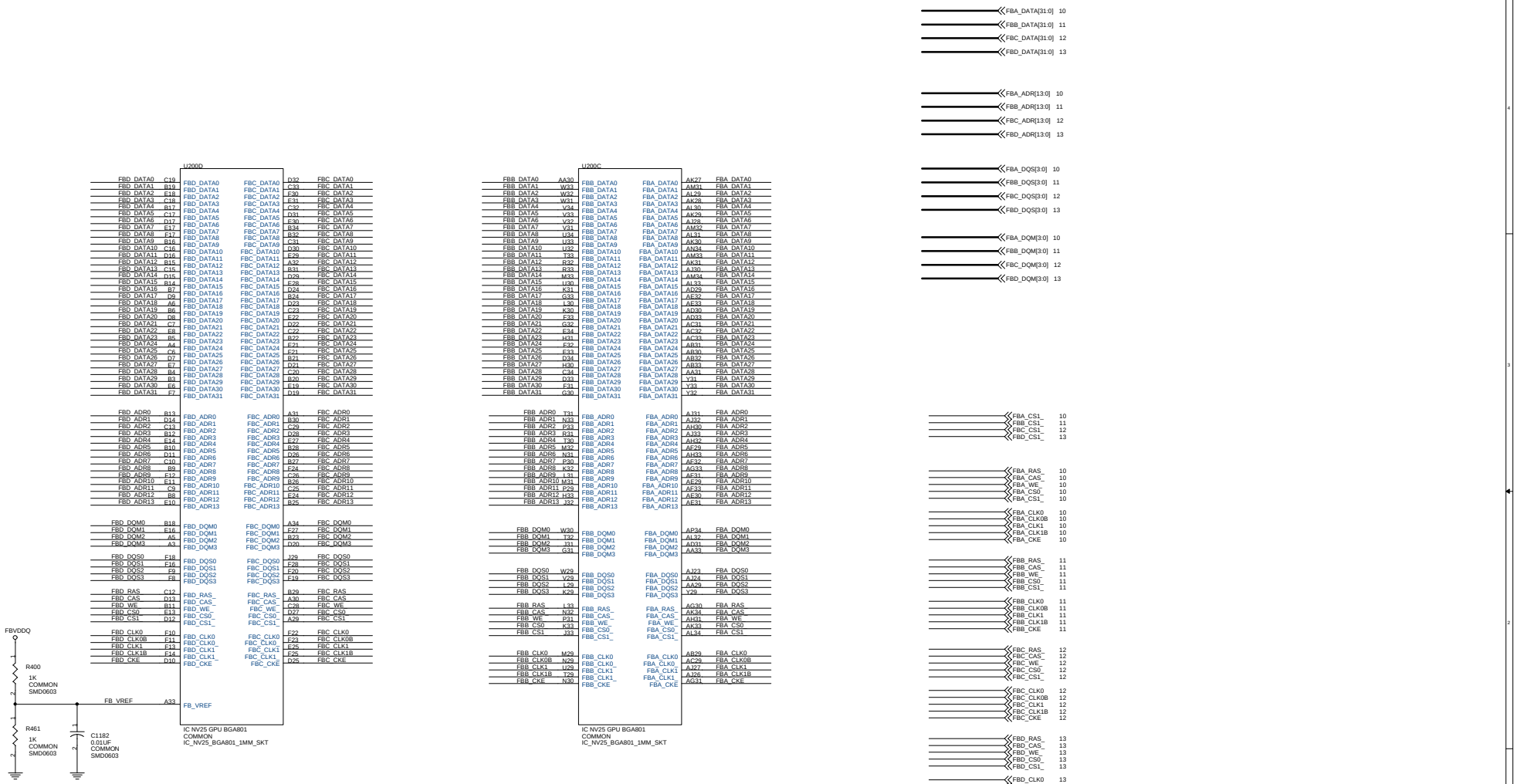

4.1 NV FBA/B/C/D

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

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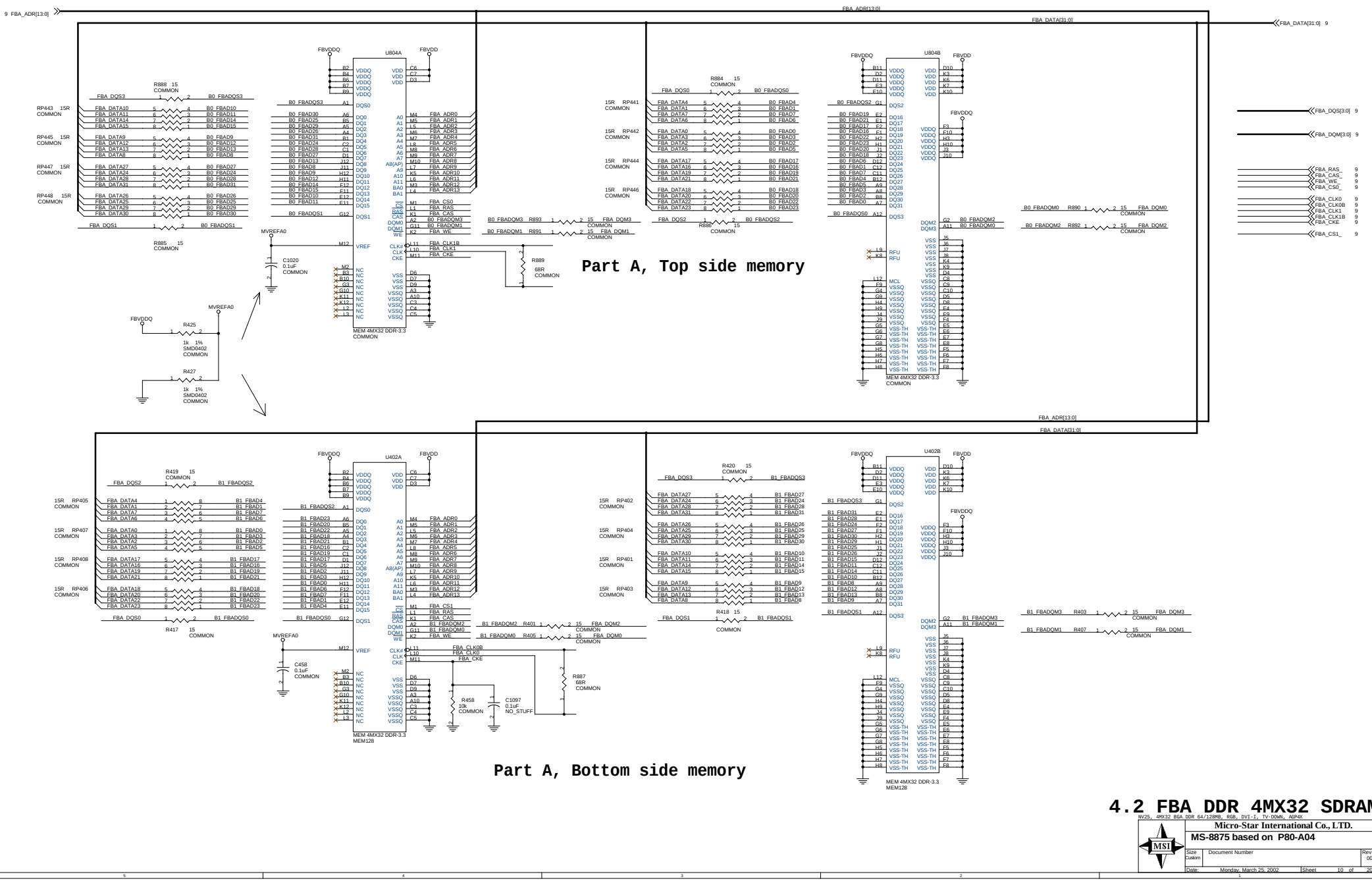

4.2 FBA DDR 4MX32 SDRAM

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

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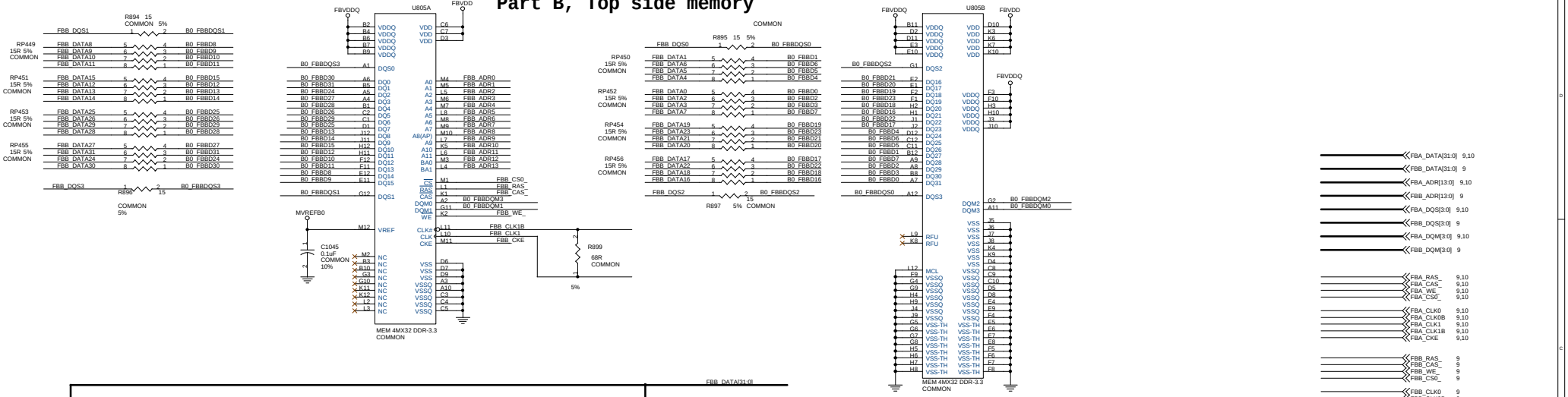
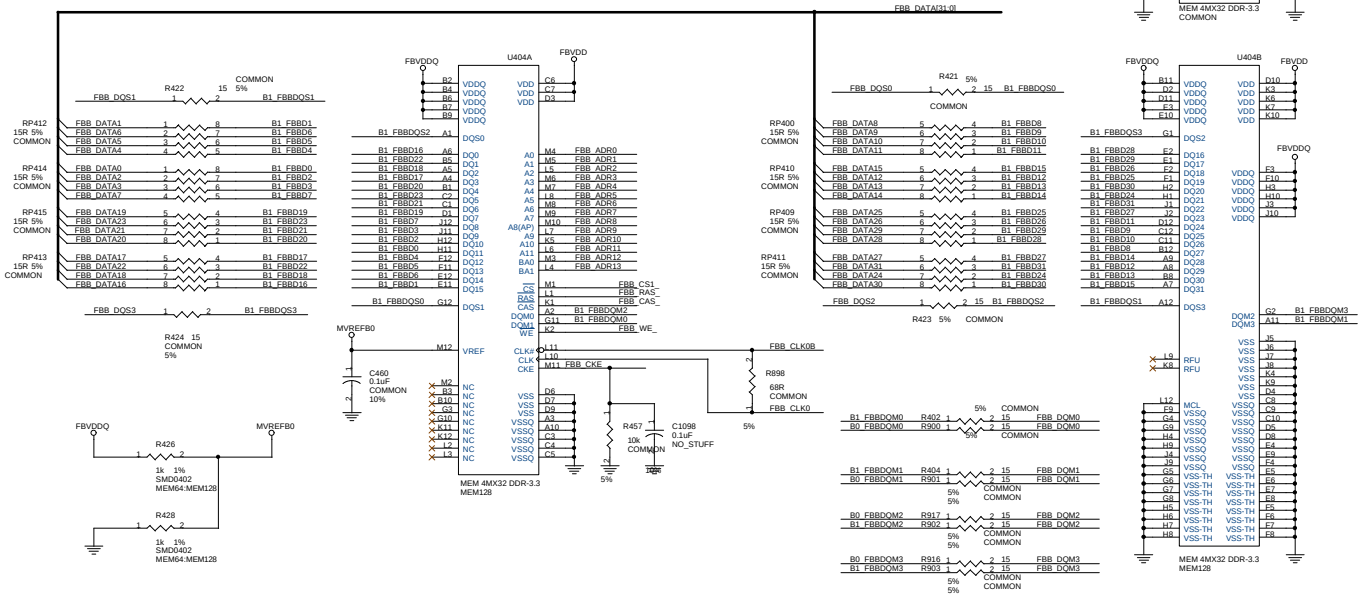
Part B, Top side memory





Part B, Bottom side memory

4.3 FBB DDR 4MX32 SDRAM

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGPAX

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MS-8875 based on P80-A04

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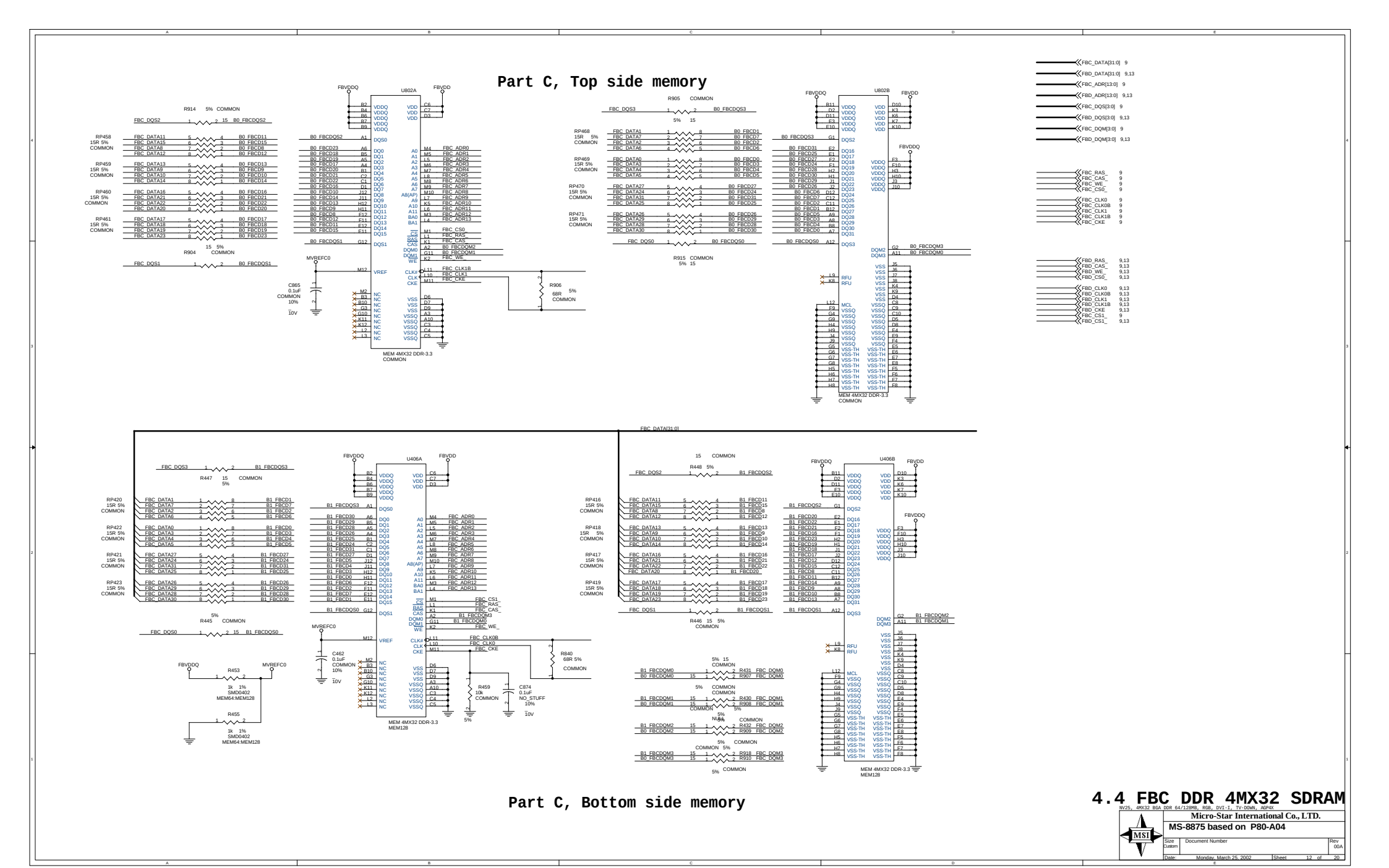

4.4 FBC DDR 4MX32 SDRAM

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGPAX

Micro-Star International Co., LTD.

MS-8875 based on P80-A04

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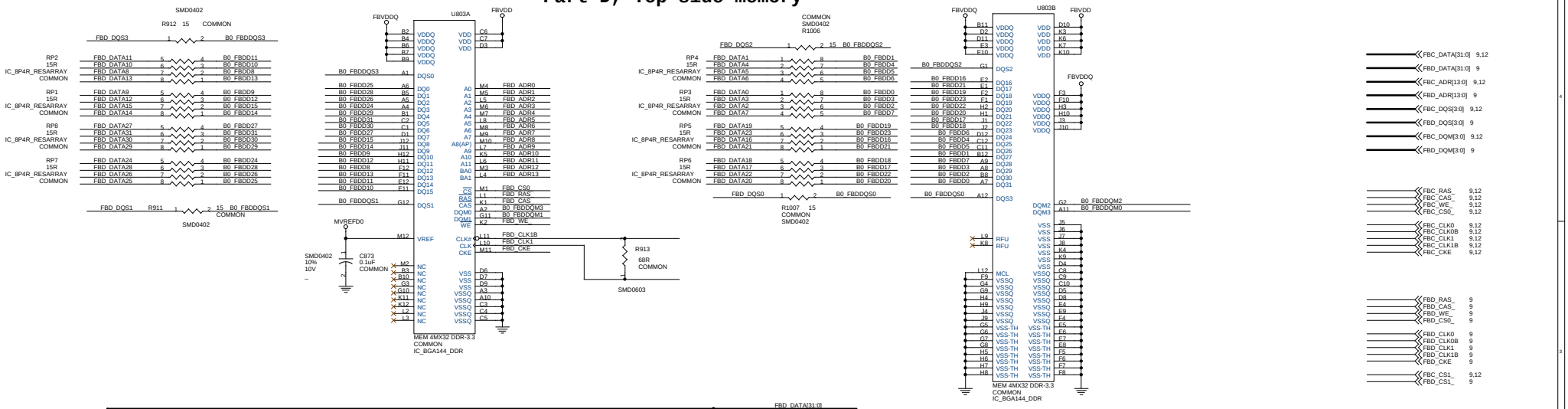
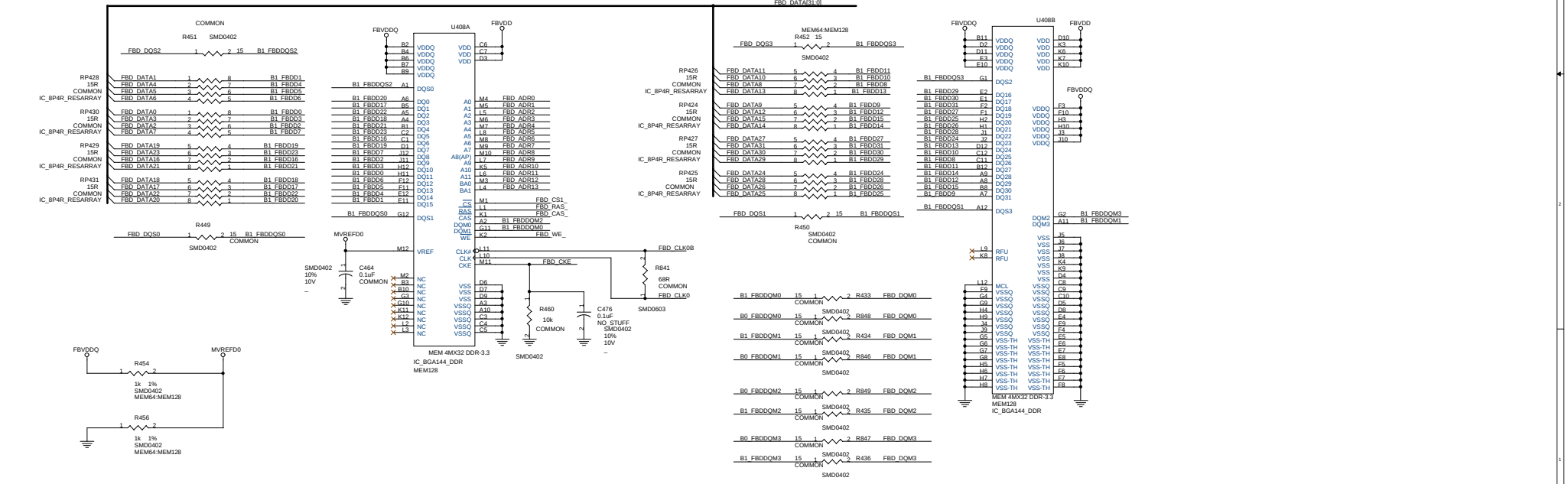
Part D, Top side memory



Part D, Bottom side memory



4.5 FBD DDR 4MX32 SDRAM

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGPAX

Micro-Star International Co., LTD.

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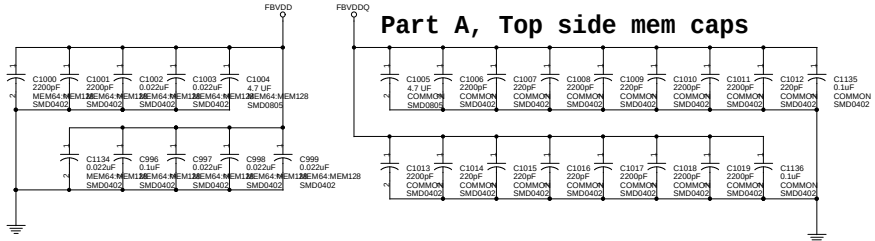
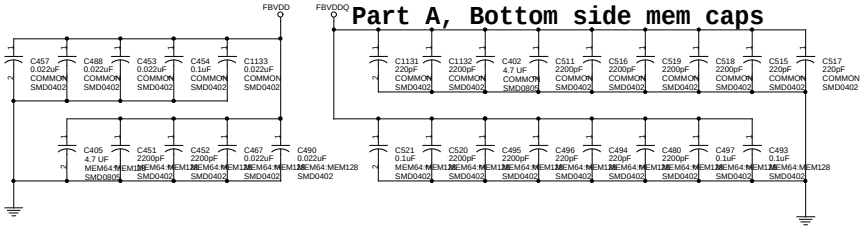
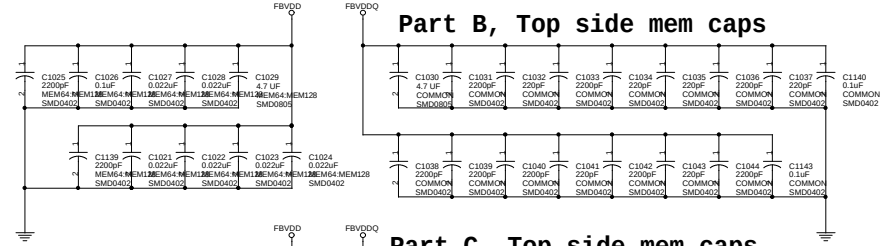


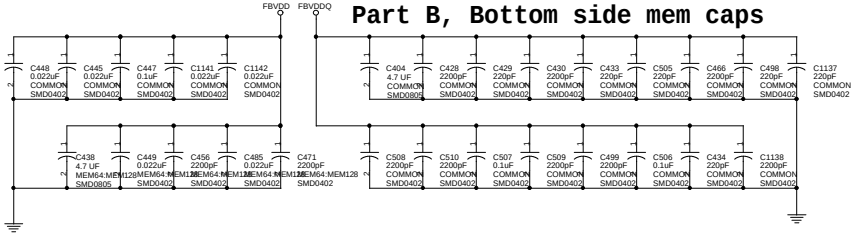
Part A, Top side mem caps



Part A, Bottom side mem caps



Part B, Top side mem caps



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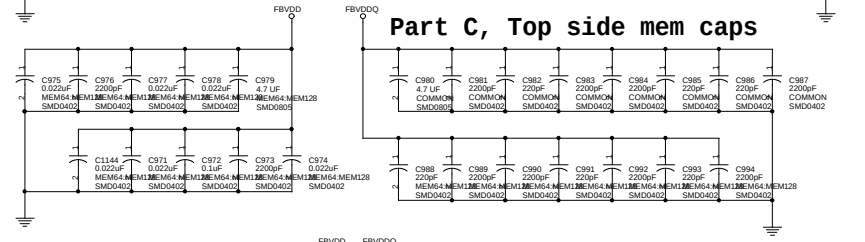
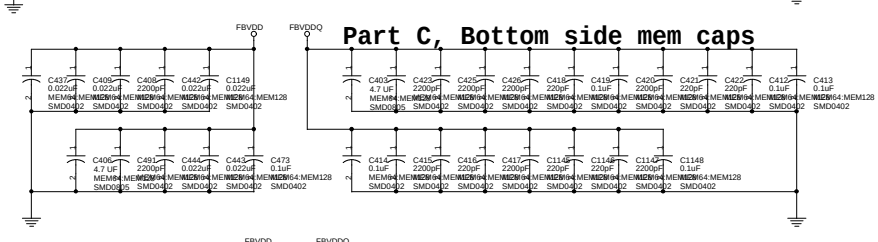
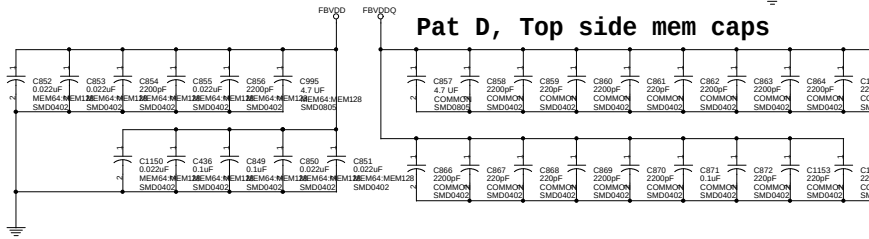


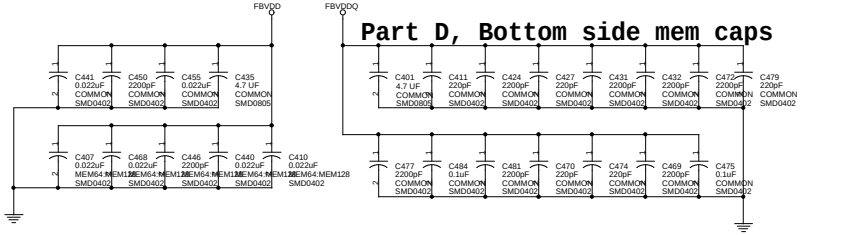
Part C, Top side mem caps



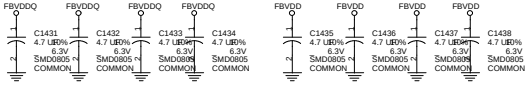
Part C, Bottom side mem caps



Pat D, Top side mem caps



Part D, Bottom side mem caps



4.6 BGA MEMORY DECOUPLING

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

Micro-Star International Co., LTD.

MS-8875 based on P80-A04

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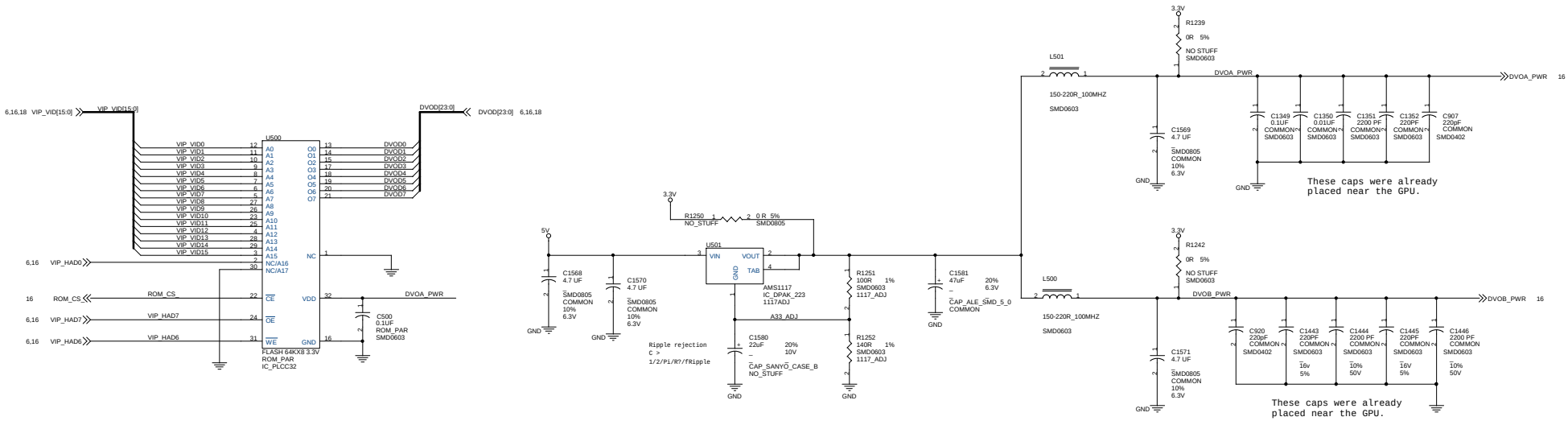

5.1 P-ROM

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

Micro-Star International Co., LTD.	
MS-8875 based on P80-A04	
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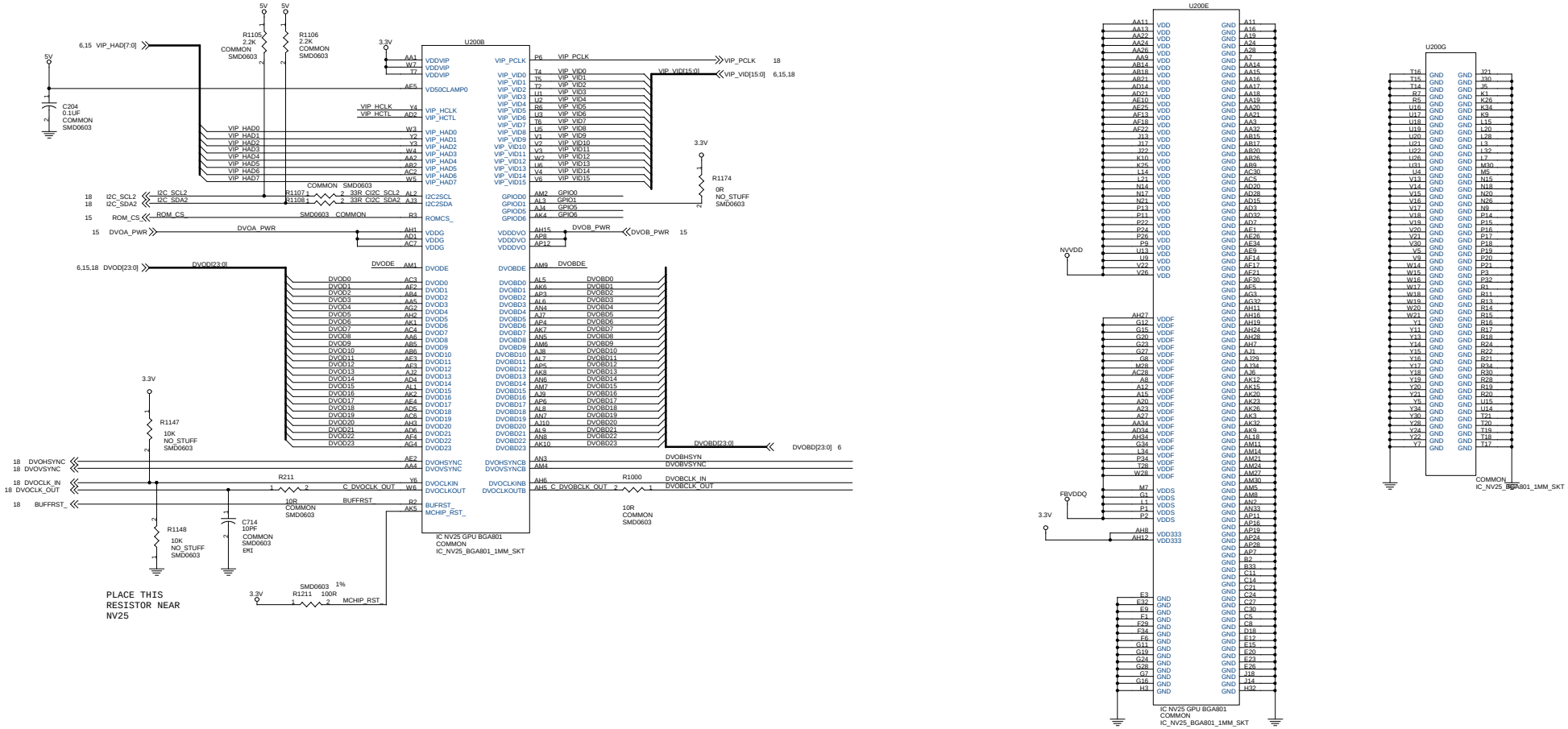

6.0 DVOA/B

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

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	MS-8875 based on P80-A04	
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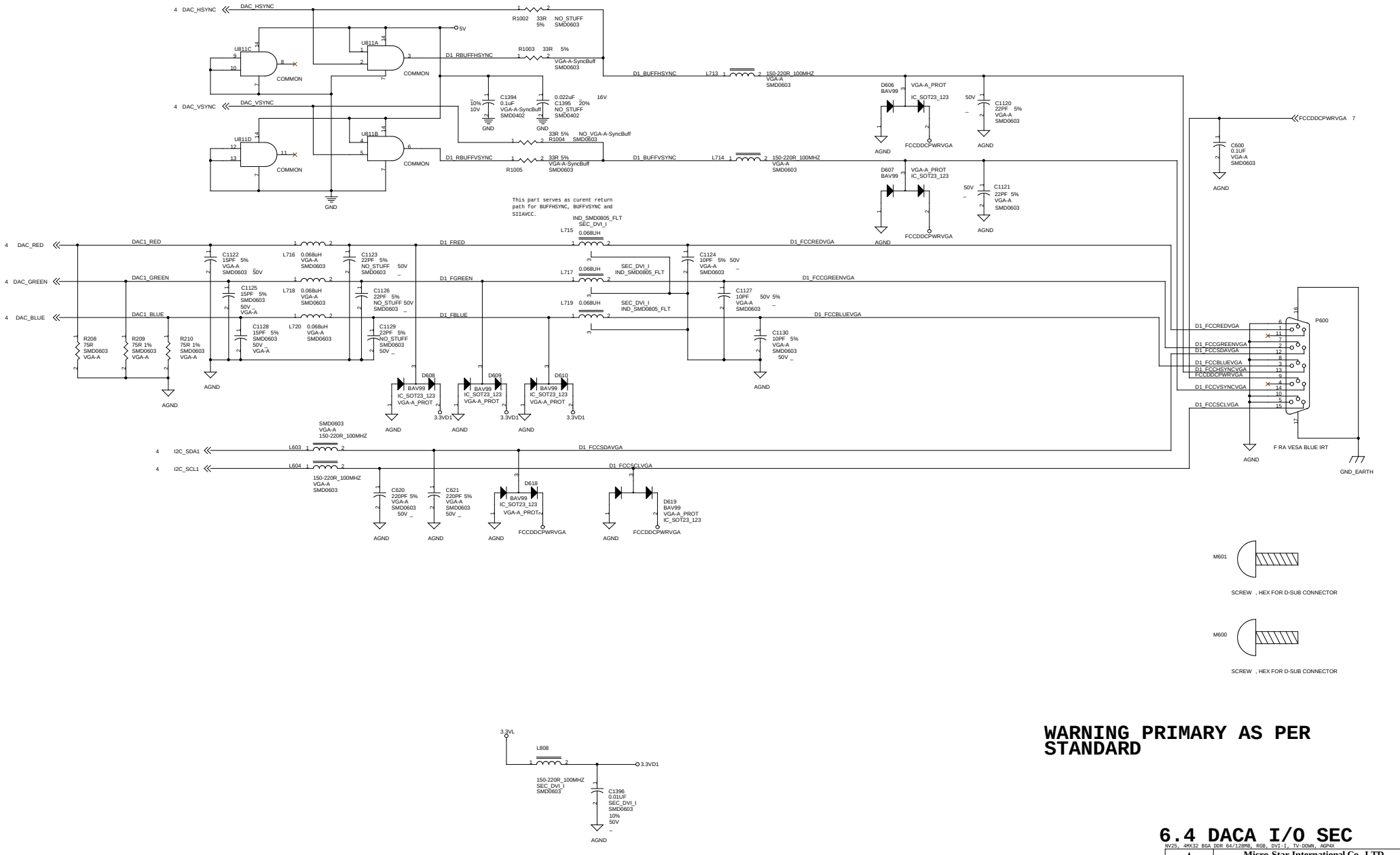

WARNING PRIMARY AS PER STANDARD

6.4 DACA I/O SEC

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

Micro-Star International Co., LTD.

MS-8875 based on P80-A04

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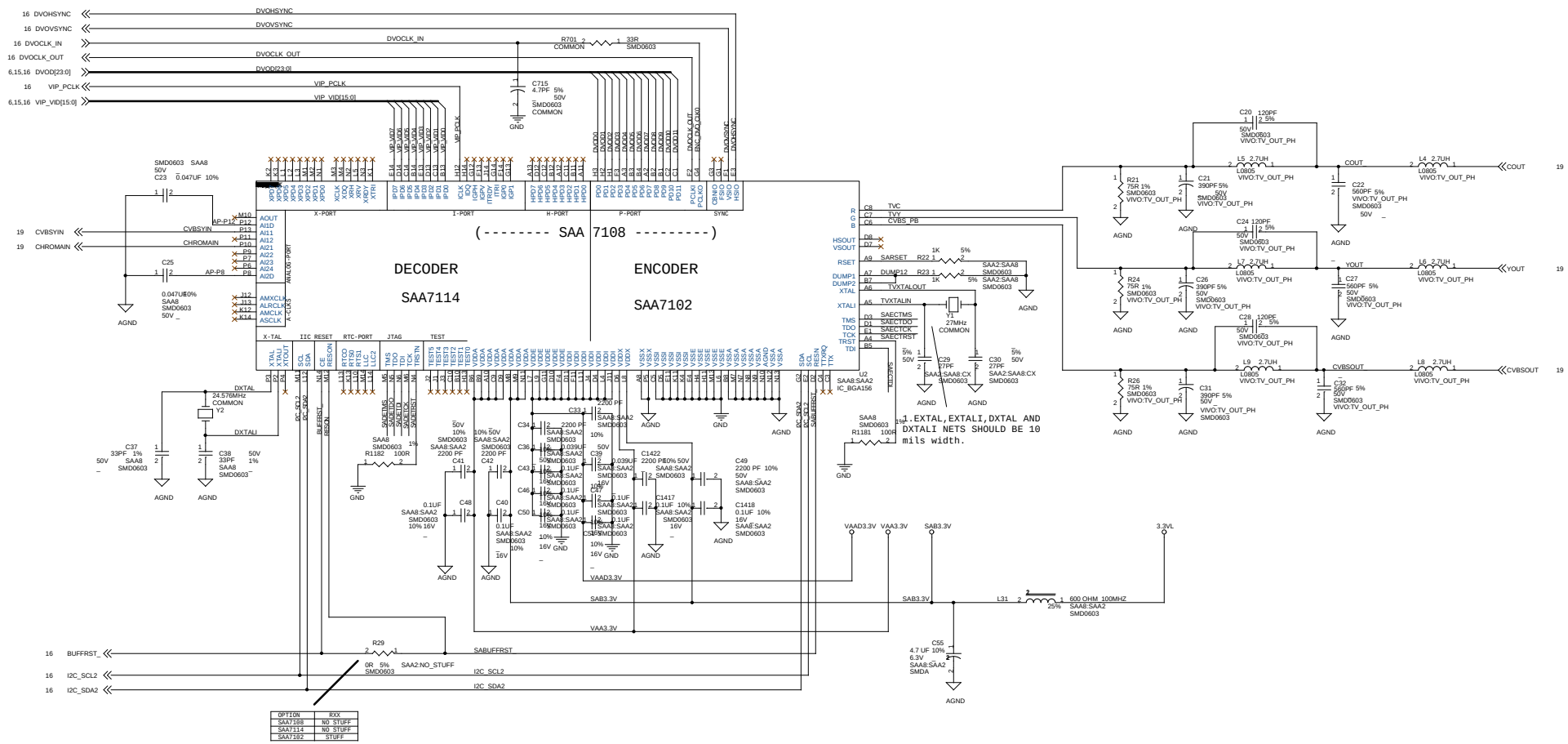

7.2 TV-PH CODEC

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

Micro-Star International Co., LTD.

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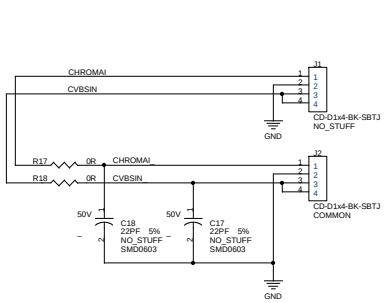

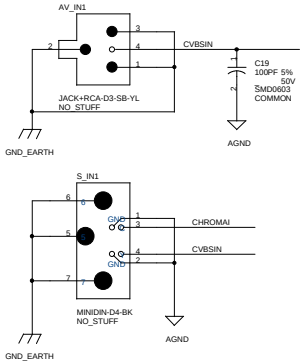

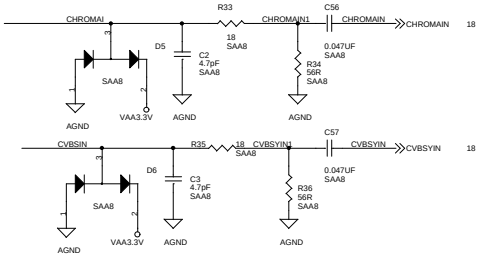

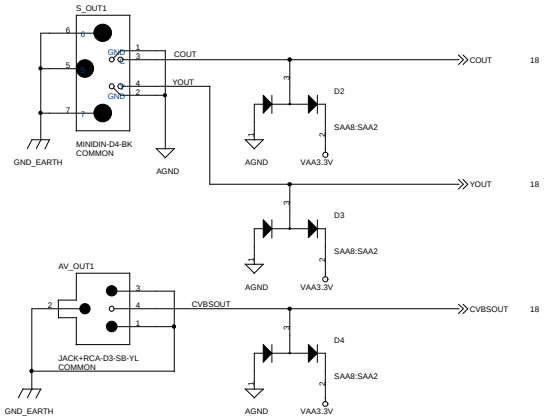

7.3 tv-out/video capture CON

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOMN, AGP4X

Micro-Star International Co., LTD.

MS-8875 based on P80-A04

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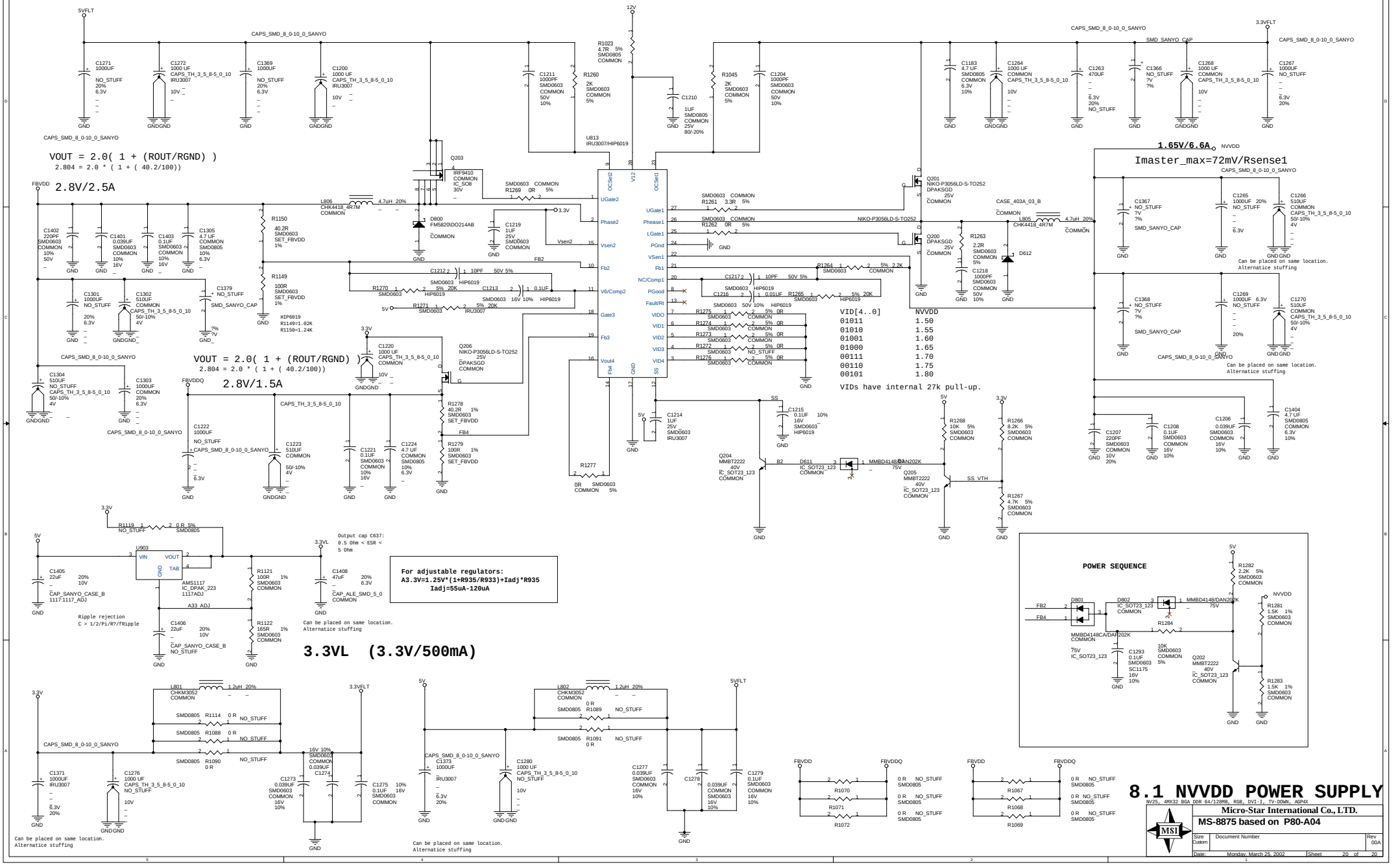
VOUT = 2.0(1 + (ROUT/RGND))
2.804 = 2.0 * (1 + (40.2/100))
2.8V/2.5A
VOUT = 2.0(1 + (ROUT/RGND))
2.804 = 2.0 * (1 + (40.2/100))
2.8V/1.5A
3.3VL (3.3V/500mA)
1.65V/6.6A
Imaster_max=72mV/Rsense1
VID[4..0] NVVDD
01011 1.50
01010 1.55
01001 1.60
01000 1.65
00111 1.70
00110 1.75
00101 1.80
VIDs have internal 27k pull-up.
For adjustable regulators:
A3.3V=1.25V*(1+R935/R933)+Iadj*R935
Iadj=55uA-120uA
POWER SEQUENCE
8.1 NVVDD POWER SUPPLY
NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X
Micro-Star International Co., LTD.
MS-8875 based on P80-A04
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