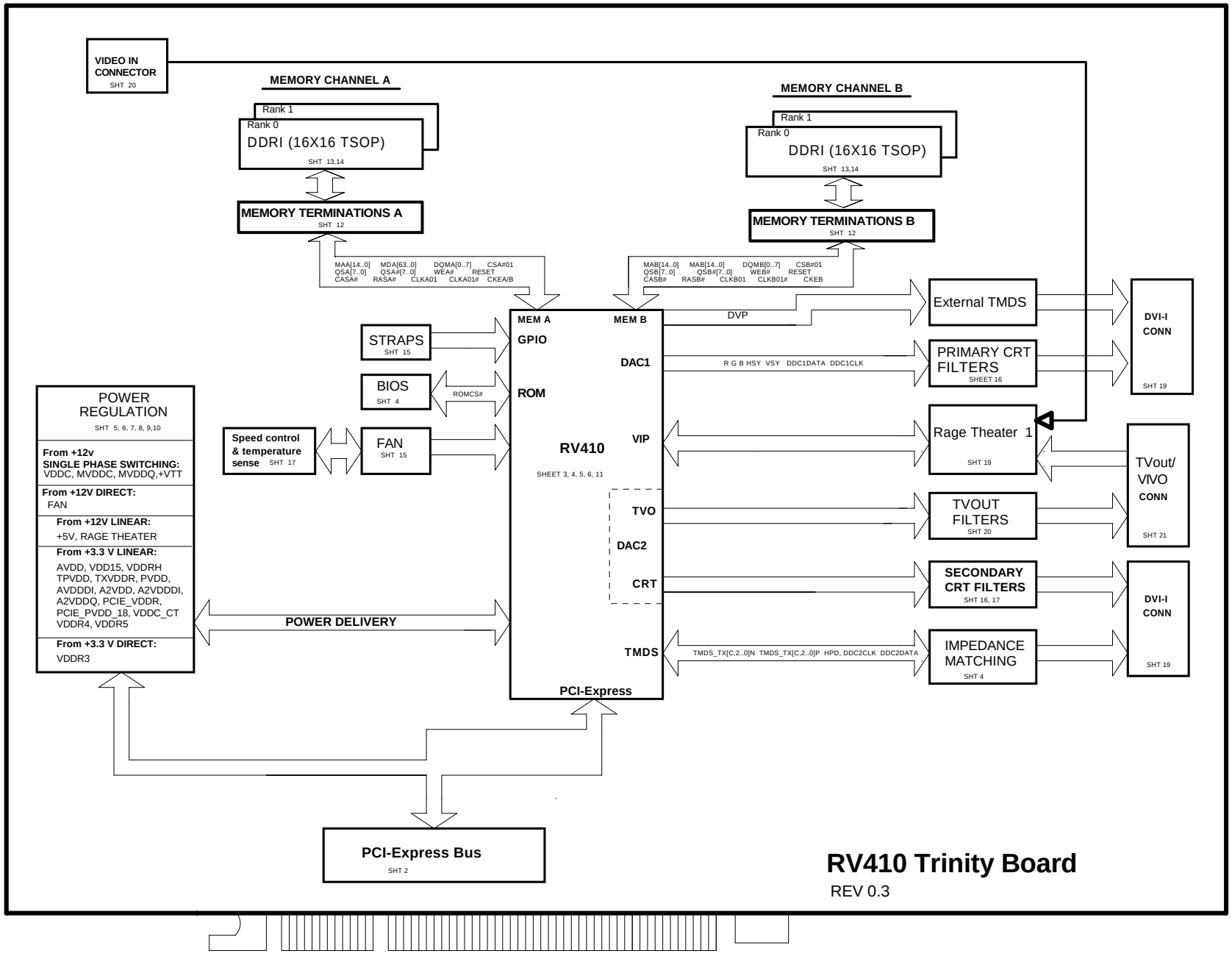

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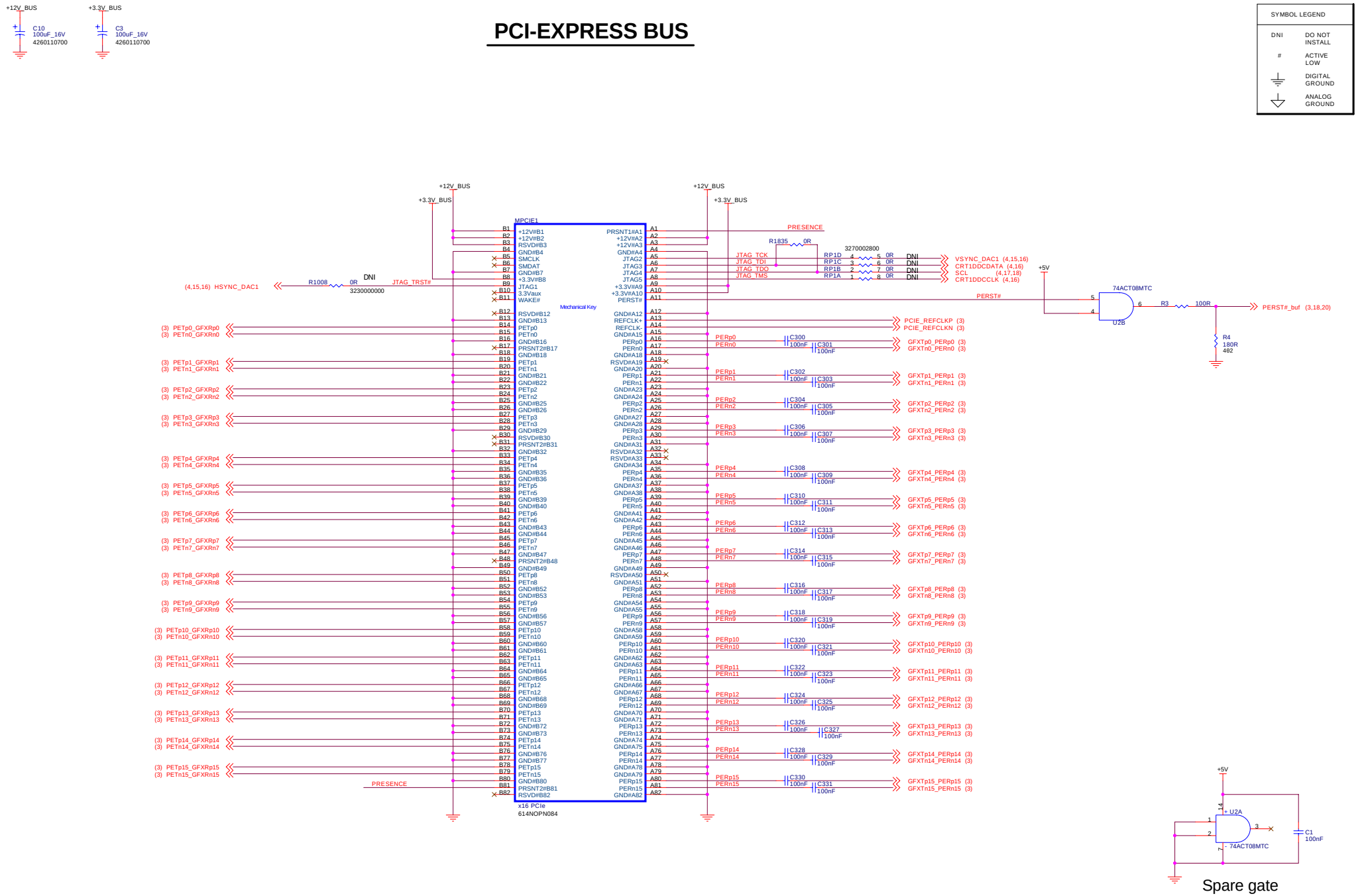
PCI-EXPRESS BUS



MS-V016		ATI RV410	
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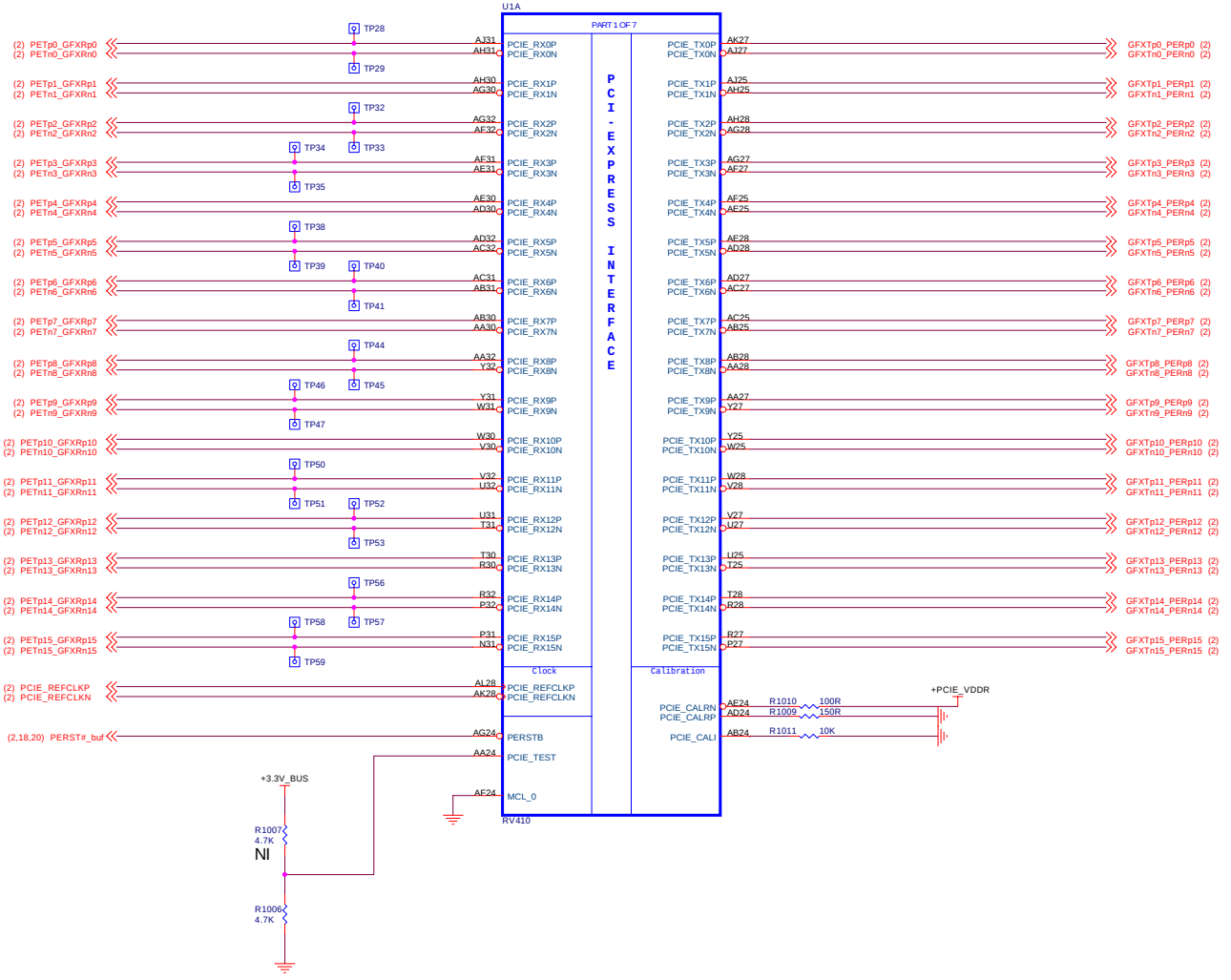
NOTE: some of the PCIE testpoints will
be available trought via on traces.



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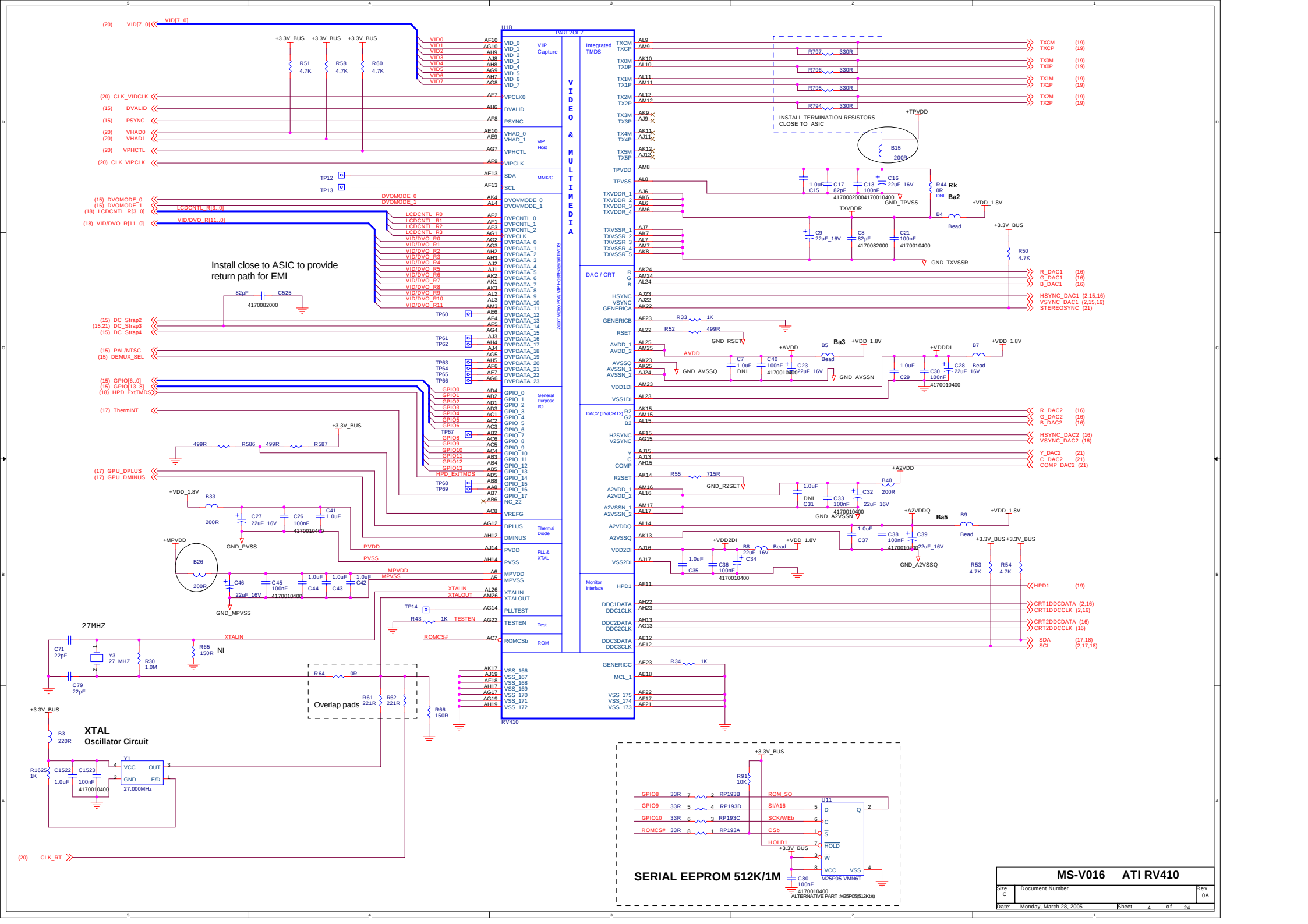
U1B
PART 2 OF 7
VIDEO & MULTIMEDIA
VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
VID_7
VIP Capture
VPCLK0
DVALID
PSYNC
VIP Host
VHAD_0
VHAD_1
VPHCTL
VIPCLK
MMI2C
SDA
SCL
DVOVMODE_0
DVOVMODE_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
Zoom/Video Port/ VIP Host/External TMDS
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_15
GPIO_16
GPIO_17
NC_22
General Purpose I/O
VREFG
DPLUS
DMINUS
Thermal Diode
PVDD
PVSS
PLL & XTAL
MPVDD
MPVSS
XTALIN
XTALOUT
PLLTEST
TESTEN
Test
ROMCSb
ROM
VSS_166
VSS_167
VSS_168
VSS_169
VSS_170
VSS_171
VSS_172
RV410
Integrated TMDS
TXCM
TXCP
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TX3M
TX3P
TX4M
TX4P
TX5M
TX5P
INSTALL TERMINATION RESISTORS CLOSE TO ASIC
TPVDD
TPVSS
TXVDDR_1
TXVDDR_2
TXVDDR_3
TXVDDR_4
TXVSSR_1
TXVSSR_2
TXVSSR_3
TXVSSR_4
TXVSSR_5
DAC / CRT
R
G
B
HSYNC
VSYNC
GENERICA
GENERICB
RSET
AVDD_1
AVDD_2
AVSSQ
AVSSN_1
AVSSN_2
VDD1DI
VSS1DI
DAC2 (TV/CRT2)
H2SYNC
V2SYNC
Y
C
COMP
R2SET
A2VDD_1
A2VDD_2
A2VSSN_1
A2VSSN_2
A2VDDQ
A2VSSQ
VDD2DI
VSS2DI
Monitor Interface
HPD1
DDC1DATA
DDC1CLK
DDC2DATA
DDC2CLK
DDC3DATA
DDC3CLK
GENERICC
MCL_1
VSS_175
VSS_174
VSS_173
GENERICD
Install close to ASIC to provide return path for EMI
27MHZ
XTAL
Oscillator Circuit
Overlap pads
SERIAL EEPROM 512K/1M
M25P05-VMN6T
ALTERNATIVE PART :M25P05(512Kbit)
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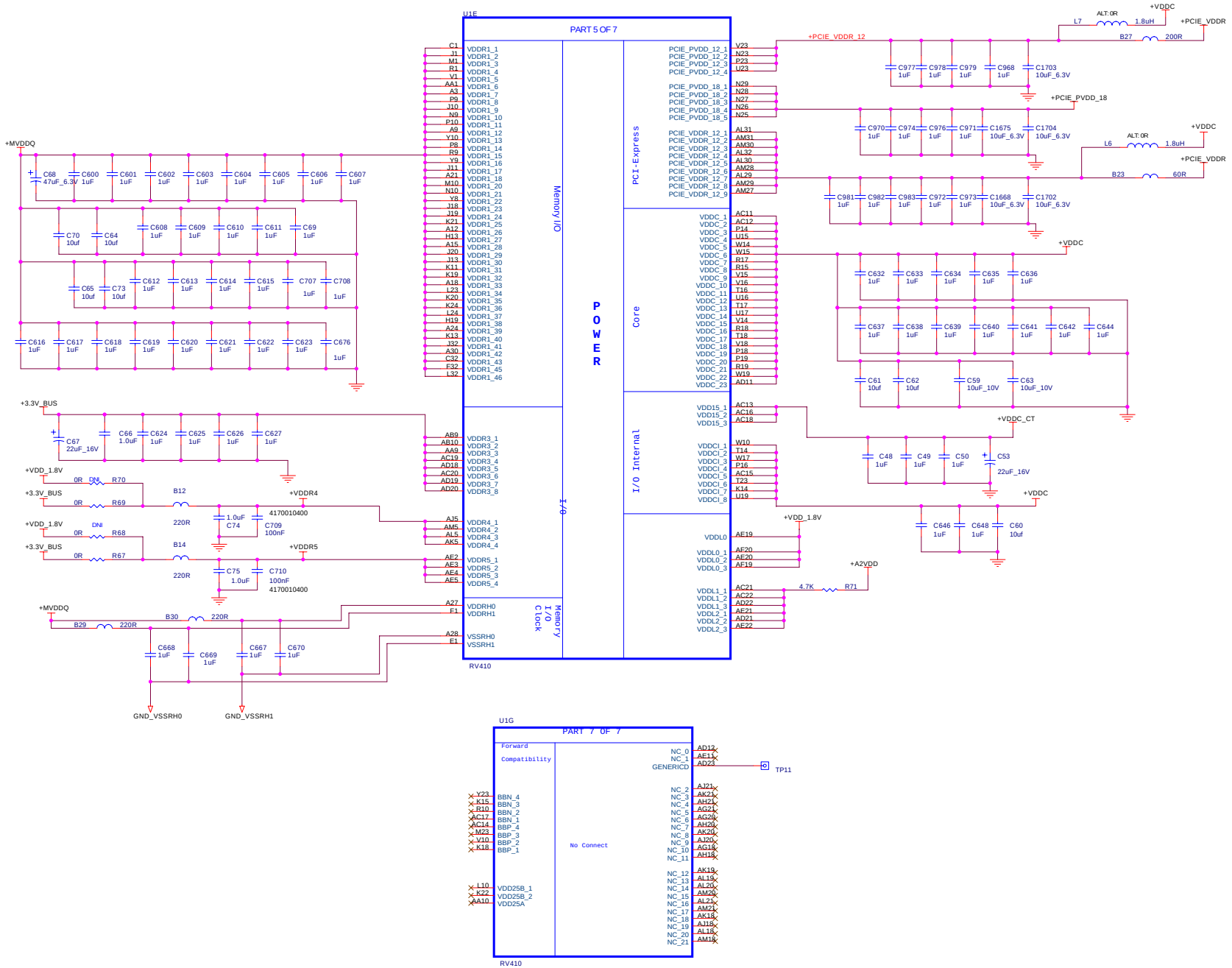

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GND_MPVSS GND_TPVSS GND_A2VSSN GND_AVSSQ GND_RSET GND_VSSRH1

GND_AVSSN GND_PVSS GND_TXVSSR GND_A2VSSQ GND_R2SET GND_VSSRH0 GND_TVVSSN

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

U1F

Part 6 of 7

PCI-EXPRESS GND

AH27	PCIE_VSS_1		VSS_45	AD16	
AC23	PCIE_VSS_2		VSS_44	AA6	
AL27	PCIE_VSS_3		VSS_43	P7	
R23	PCIE_VSS_4		VSS_42	P5	
P25	PCIE_VSS_5		VSS_41	M3	
R25	PCIE_VSS_6		VSS_40	M9	
T26	PCIE_VSS_7		VSS_39	L7	
U26	PCIE_VSS_8		VSS_38	M7	
W26	PCIE_VSS_9		VSS_47	AD17	
Y26	PCIE_VSS_10		VSS_48	AH11	
AB26	PCIE_VSS_11		VSS_49	A8	
AC26	PCIE_VSS_12		VSS_50	U7	
AD25	PCIE_VSS_13		VSS_51	C10	
AE26	PCIE_VSS_14		VSS_52	E9	
AF26	PCIE_VSS_15		VSS_53	F3	
AD26	PCIE_VSS_16		VSS_54	J9	
AC25	PCIE_VSS_17		VSS_55	N7	
AH26	PCIE_VSS_18		VSS_56	N3	
AC28	PCIE_VSS_19		VSS_57	Y5	
Y28	PCIE_VSS_20		VSS_58	AM13	
U28	PCIE_VSS_21		VSS_59	AC10	
P28	PCIE_VSS_22		VSS_60	Y6	
AH29	PCIE_VSS_23		VSS_61	U6	
AF28	PCIE_VSS_24		VSS_62	E5	
V29	PCIE_VSS_25		VSS_63	AL13	
AC29	PCIE_VSS_26		VSS_64	A11	
W27	PCIE_VSS_27		VSS_65	U8	
AB27	PCIE_VSS_28		VSS_66	U9	
V26	PCIE_VSS_29		VSS_67	U10	
AJ26	PCIE_VSS_30		VSS_68	R6	
AJ32	PCIE_VSS_31		VSS_69	AD6	
AK29	PCIE_VSS_32		VSS_70	V6	
P26	PCIE_VSS_33		VSS_71	AD14	
P29	PCIE_VSS_34		VSS_72	AD13	
R29	PCIE_VSS_35		VSS_73	D11	
T29	PCIE_VSS_36		VSS_74	J12	
U29	PCIE_VSS_37		VSS_75	K12	
W29	PCIE_VSS_38		VSS_77	A13	
Y29	PCIE_VSS_39		VSS_78	F13	
AA29	PCIE_VSS_40		VSS_79	E13	
AB29	PCIE_VSS_41		VSS_80	F15	
AD29	PCIE_VSS_42		VSS_81	K16	
AE29	PCIE_VSS_43		VSS_82	J21	
AF29	PCIE_VSS_44		VSS_83	H16	
AG29	PCIE_VSS_45		VSS_84	T15	
AJ29	PCIE_VSS_46		VSS_85	V17	
AK26	PCIE_VSS_47		VSS_86	C15	
AK30	PCIE_VSS_48		VSS_87	C4	
AG26	PCIE_VSS_49		VSS_88	U14	
N30	PCIE_VSS_50		VSS_89	P15	
R31	PCIE_VSS_51		VSS_90	A16	
AF30	PCIE_VSS_52		VSS_91	E16	
AC30	PCIE_VSS_53		VSS_92	G13	
V31	PCIE_VSS_54		VSS_93	G16	
P30	PCIE_VSS_55		VSS_94	P17	
AA31	PCIE_VSS_56		VSS_95	R16	
U30	PCIE_VSS_57		VSS_97	R14	
AD31	PCIE_VSS_58		VSS_98	W16	
AK32	PCIE_VSS_59		VSS_99	C18	
AJ28	PCIE_VSS_60		VSS_100	F16	
Y30	PCIE_VSS_61		VSS_101	W18	
AJ30	PCIE_VSS_62		VSS_102	U18	
AK31	PCIE_VSS_63		VSS_103	AE16	
AA23	PCIE_VSS_64		VSS_104	AE17	
AG31	PCIE_VSS_65		VSS_105	A19	
N24	PCIE_VSS_66		VSS_106	H32	
W23	PCIE_VSS_67		VSS_107	E19	
AB23	PCIE_VSS_69		VSS_108	G19	
P24	PCIE_VSS_70		VSS_109	N8	
R24	PCIE_VSS_71		VSS_110	Y7	
T24	PCIE_VSS_72		VSS_112	T19	
U24	PCIE_VSS_73		VSS_113	V19	
V24	PCIE_VSS_74		VSS_114	G21	
W24	PCIE_VSS_75		VSS_115	C21	
Y24	PCIE_VSS_76		VSS_116	F21	
AC24	PCIE_VSS_77		VSS_117	AE14	
AH24	PCIE_VSS_78		VSS_118	AK16	
V25	PCIE_VSS_79		VSS_119	U5	
AA25	PCIE_VSS_80		VSS_120	F22	
R26	PCIE_VSS_81		VSS_121	F18	
AA26	PCIE_VSS_82		VSS_122	K30	
T27	PCIE_VSS_83		VSS_124	C24	
AE27	PCIE_VSS_84		VSS_125	F24	
			VSS_126	M24	
B1	VSS_1		VSS_127	A25	
H1	VSS_2		VSS_128	D30	
L1	VSS_3		VSS_129	E25	
P1	VSS_4		VSS_130	G25	
U1	VSS_5		VSS_131	G20	
Y1	VSS_6		VSS_132	G22	
AD7	VSS_7		VSS_133	F27	
AE8	VSS_8		VSS_134	E28	
AL1	VSS_9		VSS_135	H21	
A2	VSS_10		VSS_136	C27	
AM2	VSS_11		VSS_137	E32	
AD10	VSS_12		VSS_138	H28	
E8	VSS_13		VSS_139	J30	
H5	VSS_14		VSS_140	K17	
K10	VSS_15		VSS_141	K27	
M8	VSS_16		VSS_142	M32	
T10	VSS_17		VSS_143	A22	
E12	VSS_18		VSS_144	C20	
AC9	VSS_19		VSS_145	E19	
AF14	VSS_20		VSS_146	H20	
AD8	VSS_21		VSS_147	J24	
C5	VSS_22		VSS_148	M28	
F10	VSS_23		VSS_149	J28	
J3	VSS_24		VSS_150	J16	
L6	VSS_25		VSS_151	F30	
M6	VSS_26		VSS_152	K23	
P6	VSS_27		VSS_153	L29	
AA4	VSS_28		VSS_154	A31	
AG11	VSS_29		VSS_155	B32	
V3	VSS_30		VSS_156	E30	
AG16	VSS_31		VSS_157	AE15	
R3	VSS_32		VSS_158	AG23	
C6	VSS_33		VSS_159	AD9	
C9	VSS_34		VSS_160	AF16	
F6	VSS_35		VSS_161	AH10	
H7	VSS_36		VSS_163	AJ10	
J6	VSS_37		VSS_164	AD15	
			VSS_165	AH16	

CORE GND

RV410

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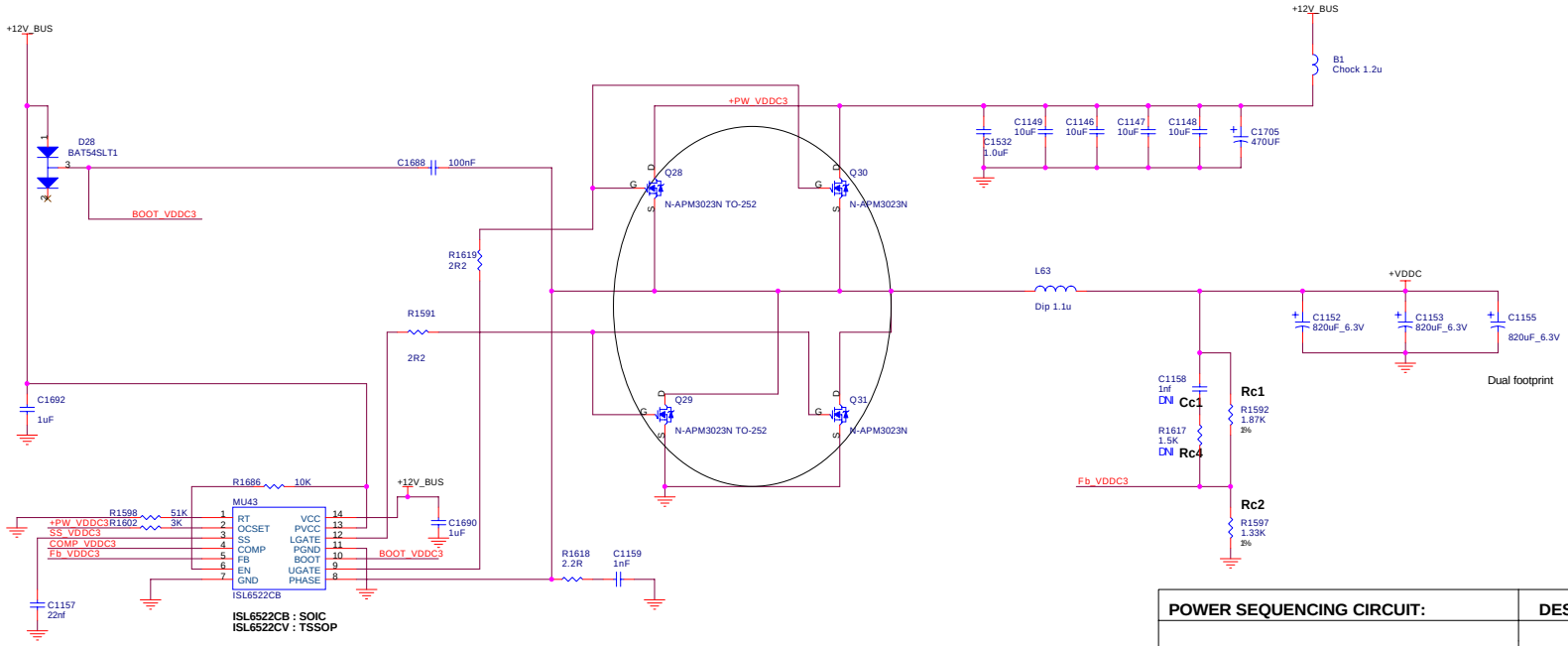
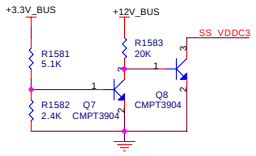
CORE REGULATOR VDDC



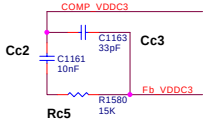
Lower MOSFET should be surrounded by
a lot of copper for heat dissipation

POWER SEQUENCING CIRCUIT:



DESIGN NOTES:

Compensation Circuit



FOR ALTERNATE #1

Remove R374, R375, R371, C168 and U32

Install R370, R112, R954, R305-R308, C160 C159 and MU32

FOR ALTERNATE #2

Change C157 for 10 uF and C121 for 1 uF
Replace C764 by 0 Ohm resistor
Replace R314 with a bead
Remove R954, R370, R305-R308, C159, R112, C160 and MU32
Install R374, R375, R371, C168 and U32

Compensation circuit

Rc1 = 10K, Rc2 = 8.06K
R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF

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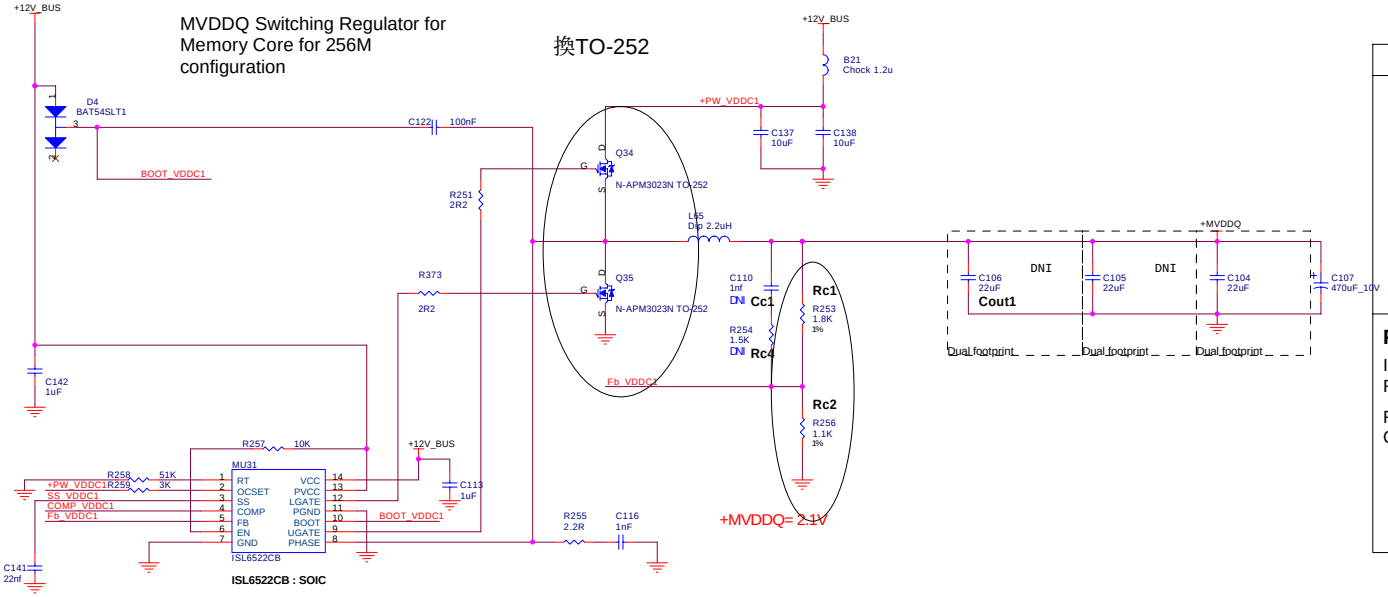
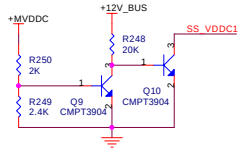
MVDDQ Switching Regulator for Memory Core for 256M configuration

換TO-252

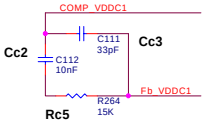


POWER SEQUENCING CIRCUIT:



DESIGN NOTES:

Compensation Circuit



FOR ALTERNATE #1

Install R372, D4, R376, C113, R257, R258, R259, MU31, R255 and C116

Remove R373, R377, R378, C122, C140 and U31

FOR ALTERNATE #2

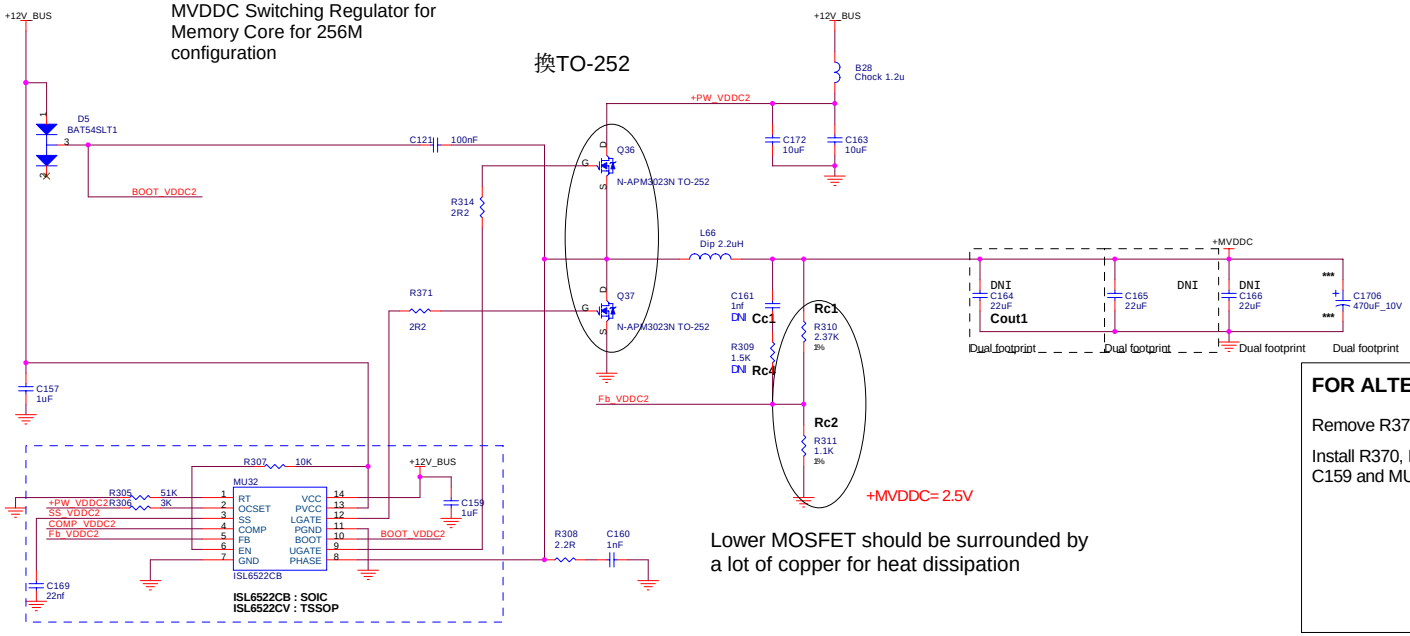
Change C142 for 10uF
Install R377, R378, R373, C122, C140 and U31
Remove R255, C116, R372, R376, D4, MU31, R257, R258, R259 and C113

Compensation circuit

Rc1 = 10K, Rc2 = 8.06K
R264 = 41.2K, C111 = 27 pF

MVDDC Switching Regulator for Memory Core for 256M configuration

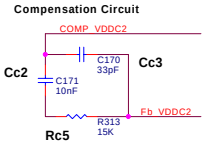
換TO-252



Lower MOSFET should be surrounded by a lot of copper for heat dissipation

DESIGN NOTES:

Compensation Circuit



FOR ALTERNATE #1

Remove R374, R375, R371, C168 and U32

Install R370, R112, R954, R305-R308, C160 C159 and MU32

FOR ALTERNATE #2

Change C157 for 10 uF and C121 for 1 uF
Replace C764 by 0 Ohm resistor
Replace R314 with a bead
Remove R954, R370, R305-R308, C159, R112, C160 and MU32
Install R374, R375, R371, C168 and U32

Compensation circuit

Rc1 = 10K, Rc2 = 8.06K
R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF

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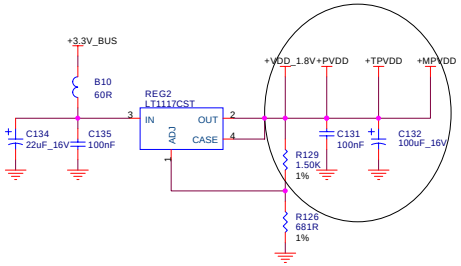
REGULATOR FOR +VDD_1.8V/ PVDD / TPVDD / MPVDD (+1.8V)

PVDD Max: 55 mA
TPVDD Max: 20 mA
MPVDD Max: 20 mA

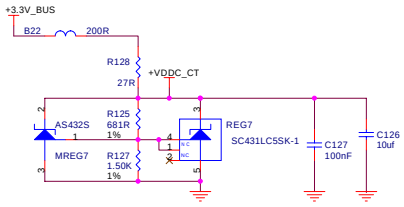
+1.8V Regulator



REG2 SPEC :
ANPEC/APL1117VC-TR,SOT223,REGULATOR(ADJ)/1A,Vin=15Vmax

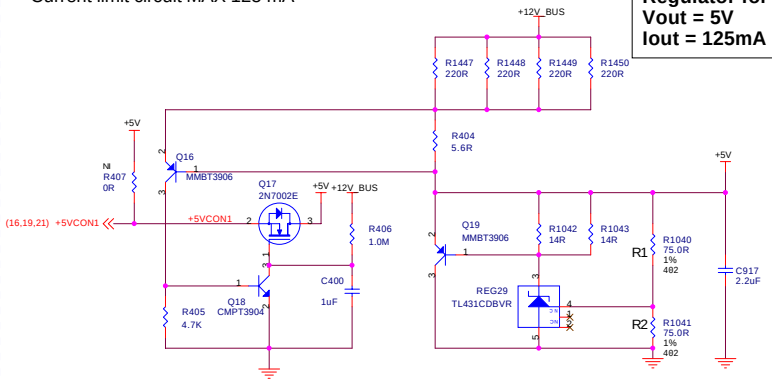
+1.5V Regulator for VDDC_CT (VDD15)

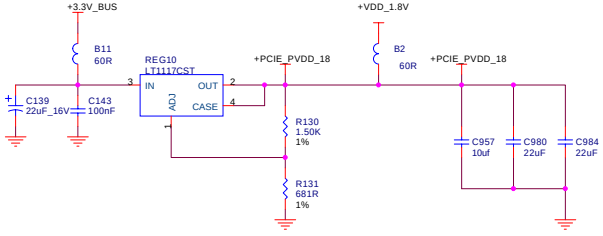
Max: 55 mA



Current limit circuit MAX 125 mA

Regulator for +5V
Vout = 5V
Iout = 125mA MAX

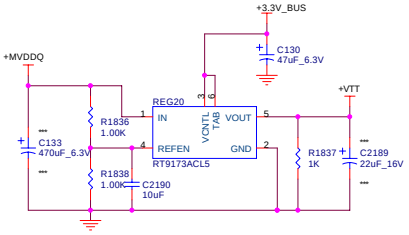




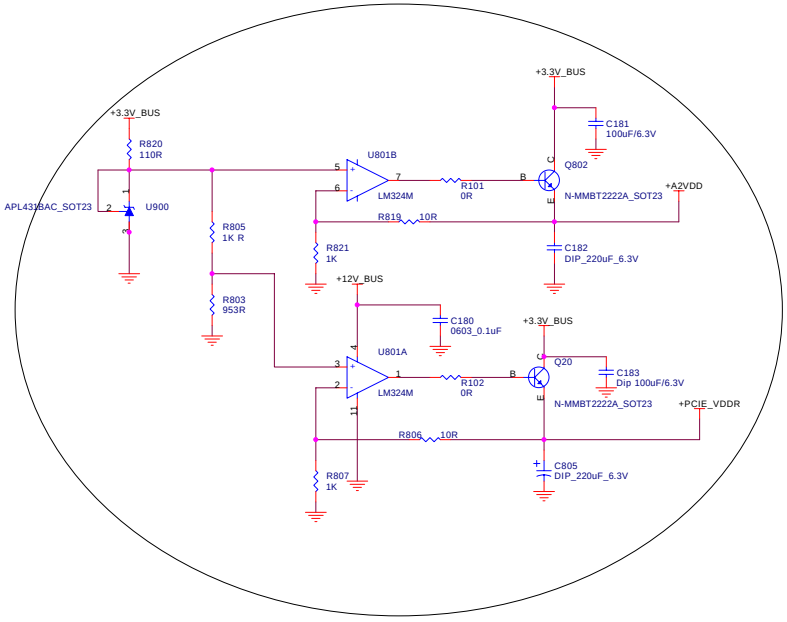
+VTT Linear Regulator

Vin = +MVDDQ
Vout = 1.25V
Iout = 2000mA MAX
Iout = 750mA Est. MAX

	R273	R275
1.4V	1K	1K



Regulator for PCIE_VDDR & +A2VDD



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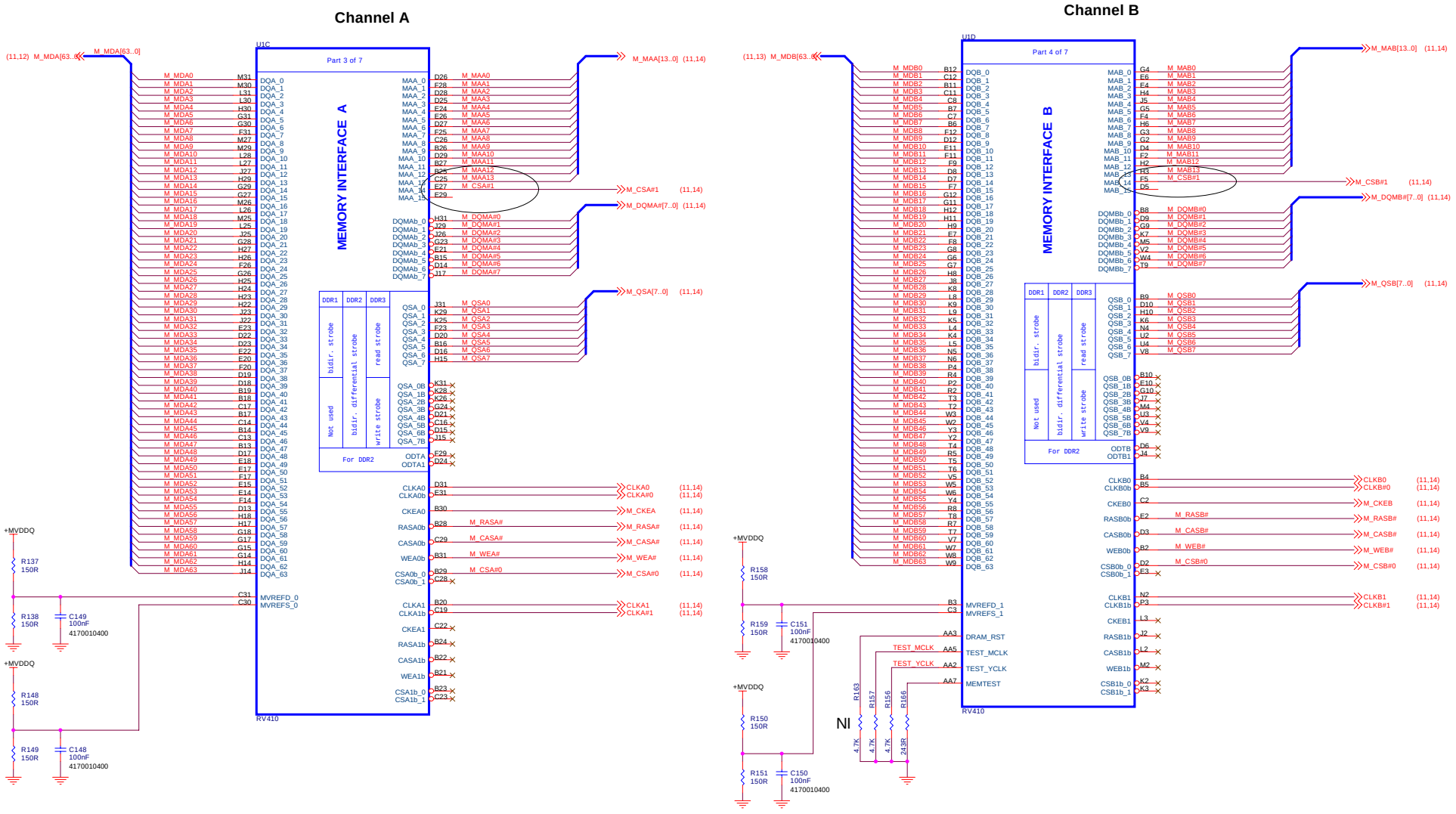
RV410 MEMORY CHANNELS A and B



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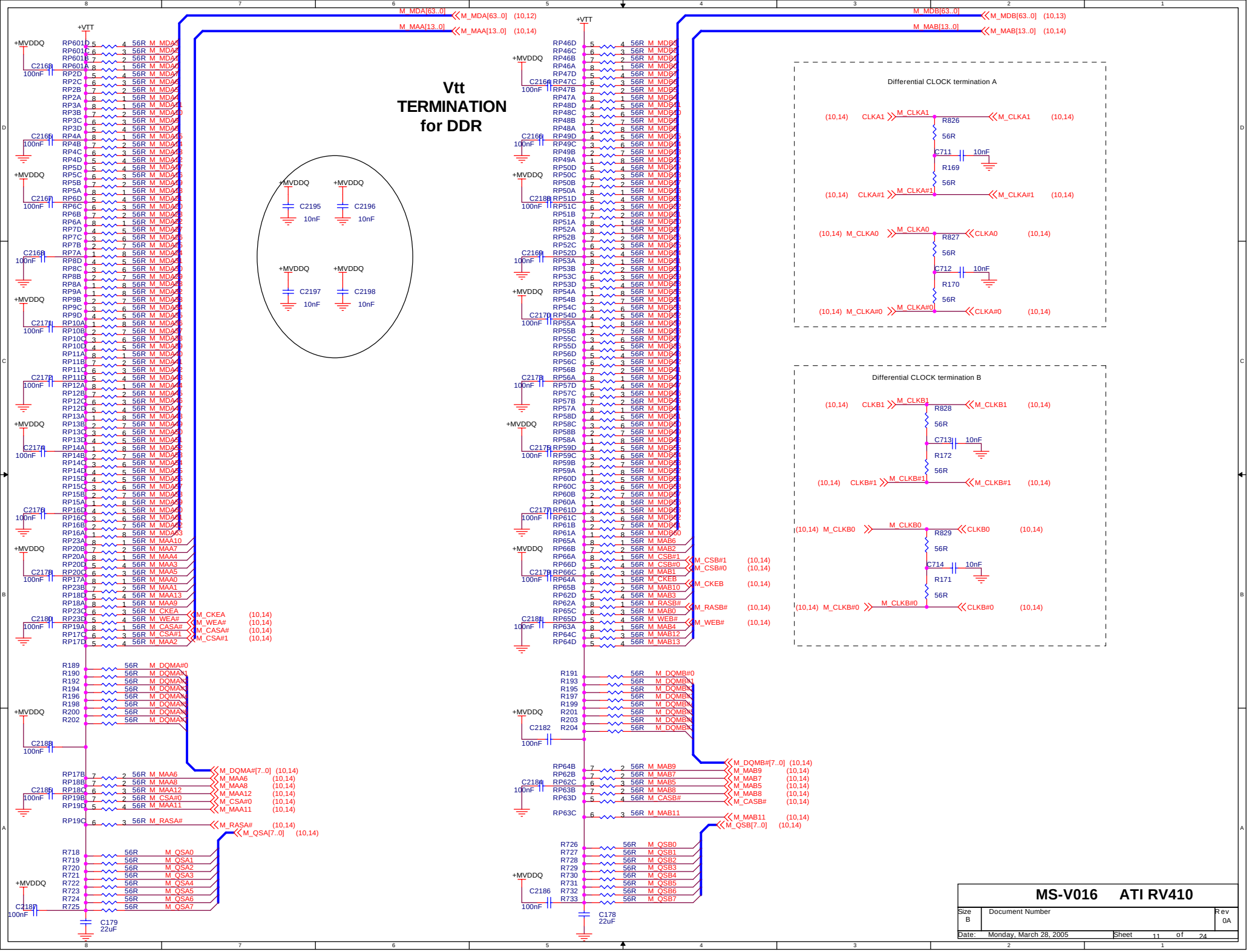
Vtt TERMINATION for DDR



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TERMINATION FOR MEMORY CHANNEL A

SERIES Resistors

For Bi-Directional signals, Series resistors should be placed close to the memory

Proper Termination of QSA?

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TERMINATION FOR MEMORY CHANNEL B

SERIES Resistors

For Bi-Directional signals, Series resistors should be placed close to the memory

Proper Termination of QSB?

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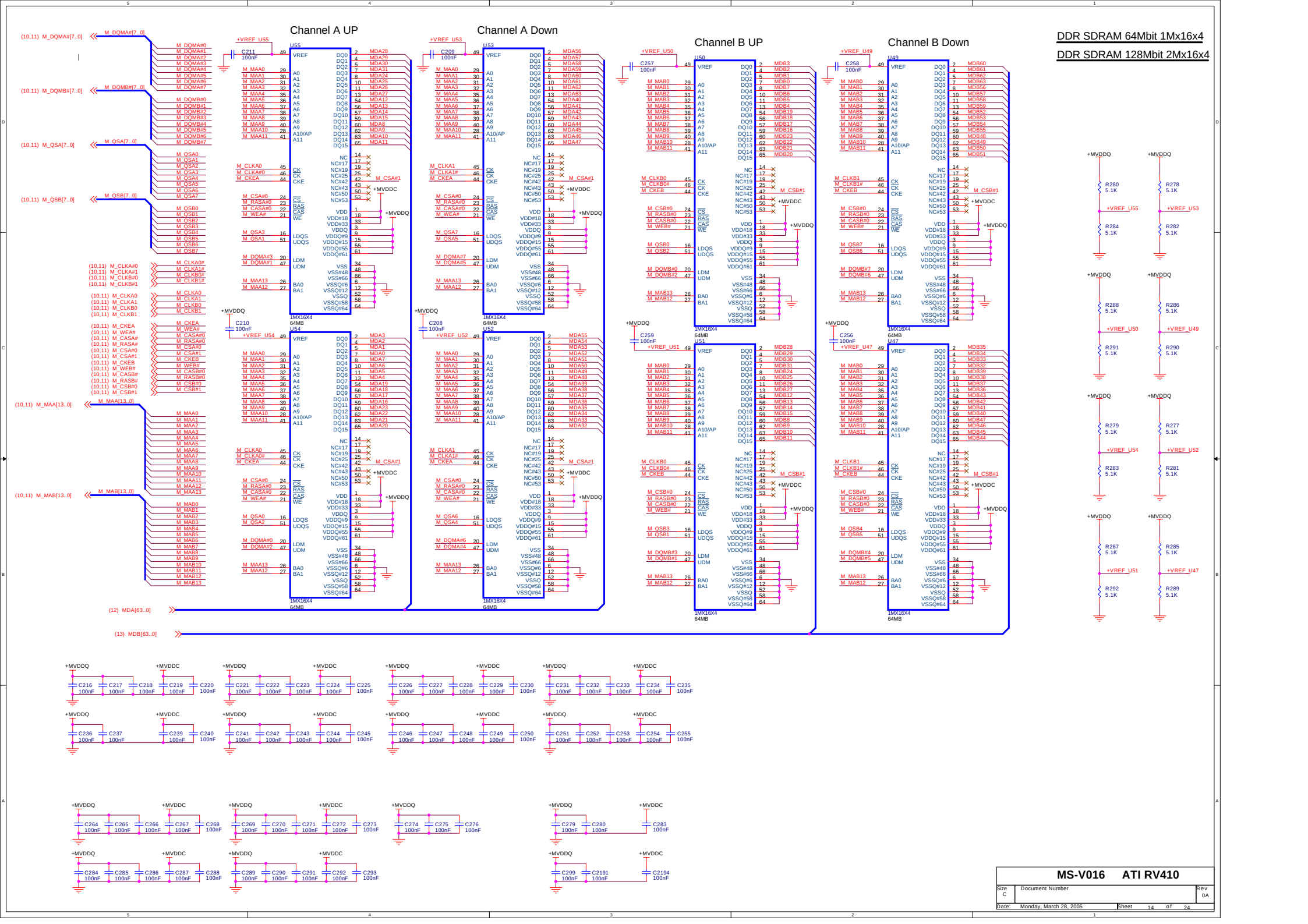
Channel A UP
Channel A Down
Channel B UP
Channel B Down
DDR SDRAM 64Mbit 1Mx16x4
DDR SDRAM 128Mbit 2Mx16x4
U55
U54
U53
U52
U50
U51
U49
U47
1MX16X4
64MB
M_CSA#1
M_CSB#1
+MVDDQ
+VREF_U55
+VREF_U54
+VREF_U53
+VREF_U52
+VREF_U50
+VREF_U51
+VREF_U49
+VREF_U47
R280 5.1K
R278 5.1K
R284 5.1K
R282 5.1K
R288 5.1K
R286 5.1K
R291 5.1K
R290 5.1K
R279 5.1K
R277 5.1K
R283 5.1K
R281 5.1K
R287 5.1K
R285 5.1K
R292 5.1K
R289 5.1K
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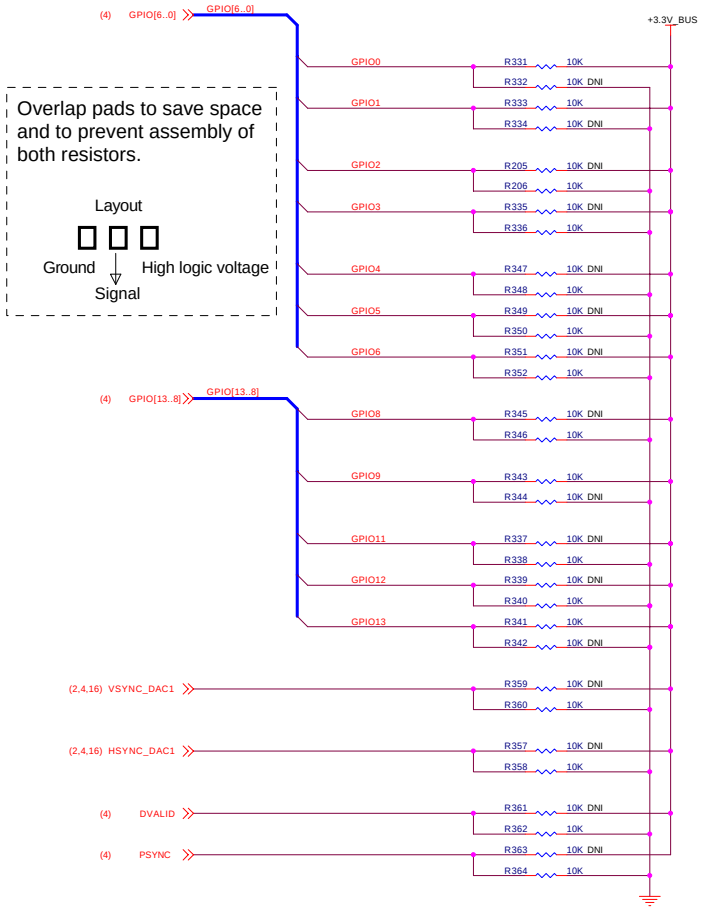
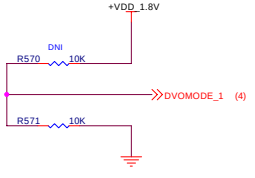
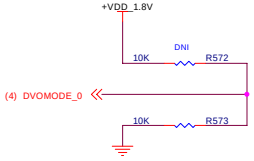
OPTION STRAPS







RV410 Shared Straps — REV. 0.5

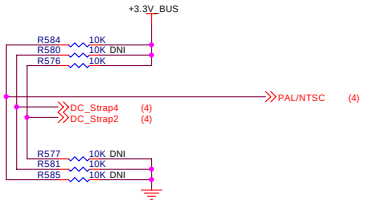
STRAPS	PIN	DESCRIPTION	VALUE
PCIE_SWING	GPIO(0)	Transmitter Swing Control 0: 50% Tx output swing mode 1: full Tx output swing	1
TRANSMIT_DE-EMPHASIS	GPIO(1)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	1
PCIE_MODE (ATI Internal)	GPIO(3:2)	PCIE mode: 00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: RESERVED	00
TX_IEXT	GPIO(4)	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage	0
FORCE _COMPLIANCE	GPIO(5)	Force chip to get to compliance state quickly for Tester purposes 0: Normal operation 1: Force to compliance state	0
PLL_BW (ATI Internal)	GPIO(6)	0: Full PLL Bandwidth 1: Reduced PLL bandwidth	0
DEBUG_ACCESS	GPIO(8)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible 0: Disable debug access 1: Enable debug access	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type. GPIO[9,13,12,11] 000x - No ROM,CHG_ID=00 001x - No ROM, CHG_ID=01 010x - No ROM, CHG_ID=10 011x - No ROM, CHG_ID=11 1001 - 1M Serial AT25F1024 ROM (Atmel) 1010 - 1M Serial AT45DB011 ROM (Atmel) 1011 - 1M Serial M25P10 ROM (ST) 1100 - 512K Serial M25P05 ROM (ST) 1101 - 1M Serial SST45LF010 ROM (SST) 1M Serial W45B512 ROM (WinBond) 512K Serial W45B012 ROM (WinBond) 1110 - 1M Serial SST25VF010 ROM (SST) 512K Serial SST25VF512 ROM (SST) 1111 - 1M NX25F011B ROM (NexFlash) **Chip IDs:** Chip ID is based on substrate fuses and CHG_ID strap (which comes from ROM if used, or pin straps if no ROM is connected): CHG_ID = ROMIDCFG[2:1] = GPIO[13:12]	1100
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this in low during reset. **0 - Slave VIP host port devices present** **1 - No slave VIP host port devices reporting presence during reset**	1
RFU	HSYNC	RFU **0 - Normal** 1 - Not used	0

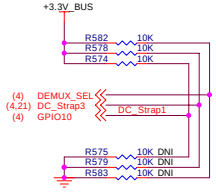
RV410 Dedicated Straps — REV. 0.2

ZV_VOLTAGE_SEL0	DVOVMODE_0	DVOVMODE_0 is for ZV_LCDCNTL and ZV_LCDDATA(11:0). **0 - 3.3 V signaling** 1 - 1.8 V signaling	0
ZV_VOLTAGE_SEL1	DVOVMODE_1	DVOVMODE_1 is for ZV_LCDDATA(23:12) **0 - 3.3 V signaling** 1 - 1.8 V signaling	0

Board Straps — REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	DVALID, PSYNC.	Memory connected to R420 identification for BIOS **00 - Samsung GDDR 3 memory 144 Ball BGA package** 01 - TBD 10 - TBD 11 - TBD	000
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Not detected	0
DC_Strap3	LCDDATA(14)	HDTV out detect **0 - Detected** 1 - Enabled	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off **01 - DAC2 On as CRT** 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1





WARNING

Some of those straps must be connected to +VDD_1.8V if ZV_LCDATA bus is set to 1.8 V.

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PRIMARY DISPLAY

(19) VSYNC_DAC1_R
(19) HSYNC_DAC1_R
(19) DDCCLK_DAC1_5V
(19) DDCDATA_DAC1_5V
(19) B_DAC1_F
(19) G_DAC1_F
(19) R_DAC1_F

PRIMARY CRT INTERFACE

(4) R_DAC1
(4) G_DAC1
(4) B_DAC1

L51 47nH
L52 47nH
L53 47nH
L54 47nH
L55 47nH
L56 47nH

R403 75.0R
R402 75.0R
R401 75.0R

C401 6.8pF
C402 6.8pF
C403 6.8pF
C404 8pF
C405 8pF
C406 8pF
NI C407 5pF
NI C408 5pF
NI C409 5pF

PLACE CLOSE TO ASIC

R_DAC1_F
G_DAC1_F
B_DAC1_F
DDCDATA_DAC1_5V
DDCCLK_DAC1_5V
HSYNC_DAC1_R
VSYNC_DAC1_R

+3.3V_BUS
R467 4.7K
BSN20 Q12
R463 6.8K
+5V
(2,4) CRT1DDCDAT

+3.3V_BUS
R468 4.7K
BSN20 Q13
R464 6.8K
+5V
(2,4) CRT1DDCCLK

(2,4,15) HSYNC_DAC1
U3B
R859 33R

U3C SN74ACT86PW

(2,4,15) VSYNC_DAC1
R860 33R

SN74ACT86PW

OPTIONAL ESD/HOTPLUG PROTECTION DIODES

+3.3V_BUS +3.3V_BUS +3.3V_BUS +12V_BUS +12V_BUS +12V_BUS +12V_BUS
D10 D11 D12 D13 D14 D15 D16
BAT54SLT1
DNI

R465 33R
R466 33R

PLACE CLOSE TO CONNECTOR
NI C751 22pF
C752 22pF NI

PRIMARY VGA CONNECTOR

F1 750mA +5V
+5VCON1 +5VCON1 (9,19,21)
B39 Bead
+5V_DIN2 (19)
C562 100nF

J5
R
G
B
MS0
MS1
MS2
MS3
NC
HS
VS
VSS
VSS#6
VSS#7
VSS#8
VSS#10
CASE
CASE#17
SLIM VGA HT 6.27MM

SECONDARY DISPLAY

PLACE CLOSE TO ASIC

(4) R_DAC2
(4) G_DAC2
(4) B_DAC2

L71 47nH
L72 47nH
L73 47nH
L74 47nH
L75 47nH
L76 47nH

R451 75.0R
R452 75.0R
R453 75.0R

C451 6.8pF
C452 6.8pF
C453 6.8pF
C454 8pF
C455 8pF
C456 8pF
NI C573 5pF
NI C574 5pF
NI C575 5pF

R_DAC2_F
G_DAC2_F
B_DAC2_F
R_DAC2_F (19)
G_DAC2_F (19)
B_DAC2_F (19)

+3.3V_BUS
R479 4.7K
BSN20 Q14
6.8K R480
+5V
(4) CRT2DDCDATA
R825 33R
DDCDATA_DAC2_R (19)

+3.3V_BUS
R481 4.7K
BSN20 Q15
6.8K R482
+5V
(4) CRT2DDCCLK
R824 33R
DDCCLK_DAC2_R (19)

74ACT08MTC U2C
(4) HSYNC_DAC2
+5V
R31 33R
HSYNC_DAC2_R (19)

74ACT08MTC U2D
(4) VSYNC_DAC2
R32 33R
VSYNC_DAC2_R (19)

OPTIONAL ESD/HOTPLUG PROTECTION DIODES

+3.3V_BUS +3.3V_BUS +3.3V_BUS +12V_BUS +12V_BUS +12V_BUS +12V_BUS
D17 D18 D19 D20 D21 D22 D23
BAT54SLT1
DNI

C749 22pF DNI
C750 22pF DNI

PLACE CLOSE TO CONNECTOR

+5V_DIN1 +5V_DIN1 (19)

MJ4 DNI
R
G
B
MS0
MS1
MS2
MS3
NC
HS
VS
VSS
VSS#6
VSS#7
VSS#8
VSS#10
CASE
CASE#17
SLIM VGA HT 6.27MM

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

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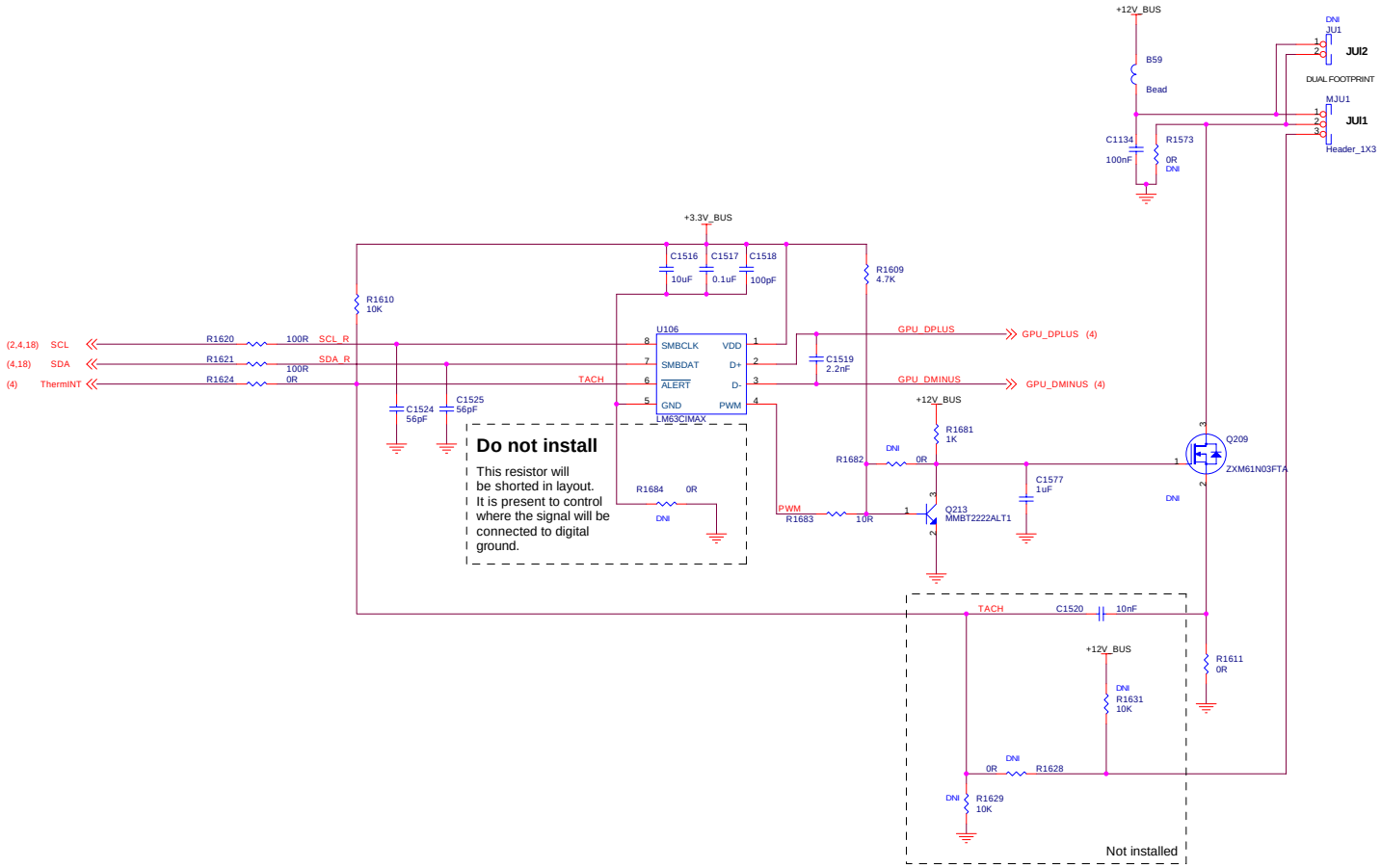
TEMPERATURE SENSE AND SPEED CONTROLLED FAN



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MUST BE INSTALLED IF NO
TMDS IS INSTALLED

LCDCNTL_R[3..0]

+3.3V_BUS

LCDCNTL_R0 RP600A 1 8 10K
LCDCNTL_R1 RP600B 2 7 10K
LCDCNTL_R2 RP600C 3 6 10K
LCDCNTL_R3 RP600D 4 5 10K

Place close to TMDS

(4) VID/DVO_R[11..0]

VID/DVO_R[11..0]

U37

VID/DVO_R0 18 D0
VID/DVO_R1 17 D1
VID/DVO_R2 16 D2
VID/DVO_R3 15 D3
VID/DVO_R4 14 D4
VID/DVO_R5 13 D5
VID/DVO_R6 10 D6
VID/DVO_R7 9 D7
VID/DVO_R8 8 D8
VID/DVO_R9 7 D9
VID/DVO_R10 6 D10
VID/DVO_R11 5 D11

TX0- 35 TXOM_EXT
TX0+ 36 TXOP_EXT
TX1- 38 TX1M_EXT
TX1+ 39 TX1P_EXT
TX2- 41 TX2M_EXT
TX2+ 42 TX2P_EXT
TXC- 32 TXCM_EXT
TXC+ 33 TXCP_EXT

TXCP_EXT (19)
TXCM_EXT (19)
TX2P_EXT (19)
TX2M_EXT (19)
TX1P_EXT (19)
TX1M_EXT (19)
TX0P_EXT (19)
TX0M_EXT (19)

R1240 330R C481 100nF
R1241 330R C482 100nF
R1242 330R C483 100nF
R1243 330R C484 100nF

+AVCC_TMDS

+3.3V_BUS

B31 150R

AVCC 34
AVCC#40
AGND 37
AGND#43

C460 100pF C461 2.2nF C462 100nF C463 100pF C464 2.2nF C465 100nF
C466 47uF_6.3V

+3.3V_BUS
R625 1K
R620 1K
I2C_ADDR 24 CTL3/A2

(4) LCDCNTL_R[3..0]

LCDCNTL_R[3..0]

LCDCNTL_R1 20 HDYNC
LCDCNTL_R0 21 VSYNC
LCDCNTL_R2 19 DE
LCDCNTL_R3

+VREF_TMDS
12 IDICK+
11 IDCK-

+VREF_TMDS

VREF 2

EXT_SWING 30

EXT_SWING R485 680R

+3.3V_BUS
R483 5.1K
MSEN_TMDS 48 MSEN

(2,3,20) PERST#_buf

INSTALL FOR Si164
HI = I2C SELECT,LO = I2C CTRL RESET

R1103 33K
R1104 0R
HPD_ExtTMDS 44 EDGE/HTPLG
I2C_RST 25 ISEL/RST#

(4,17) SDA 26 SDA
(2,4,17) SCL 27 SCL

+PVCC_TMDS

PVCC1 28
PVCC2 46

C469 100pF C470 100nF C479 100pF C480 100nF C471 22uF_10V

PGND 29
PGND#45 45
VCC#22 22
VCC 3

+3.3V_BUS

GND 4
GND#23 23

C472 100pF C473 100nF C474 2.2nF C475 100nF C476 100pF C477 2.2nF

TH_GND 49

+3.3V_BUS
Do not install
R484 0R
R492 0R

1 RSVD
31 RSVD#31
47 RSVD#47

Sil1162

+3.3V_BUS
B32 200R
22uF_10V C1236

Max 25 mA

+12V_BUS
R301 360R
R304 680R
R491 2K

REG9 TL431CDBVR

(4) HPD_ExtTMDS

HPD_ExtTMDS

+3.3V_BUS
R486 20K 402
R487 20K 402

R488 20K 402
R489 20K 402

HPD_ExtTMDS_DVI (19)

D35 MMBZ5222BLT1
R490 100K
Q32 CMPT3904
Q33 CMPT3904

SELECT VREF ACCORDING
TO SWING ON D[23:0]

+VDDR4

C478 100nF X7R
R302 1.0K
+VREF_TMDS
C467 100nF X7R
R303 1.0K

SELECT VREF ACCORDING
TO SWING ON D[23:0]

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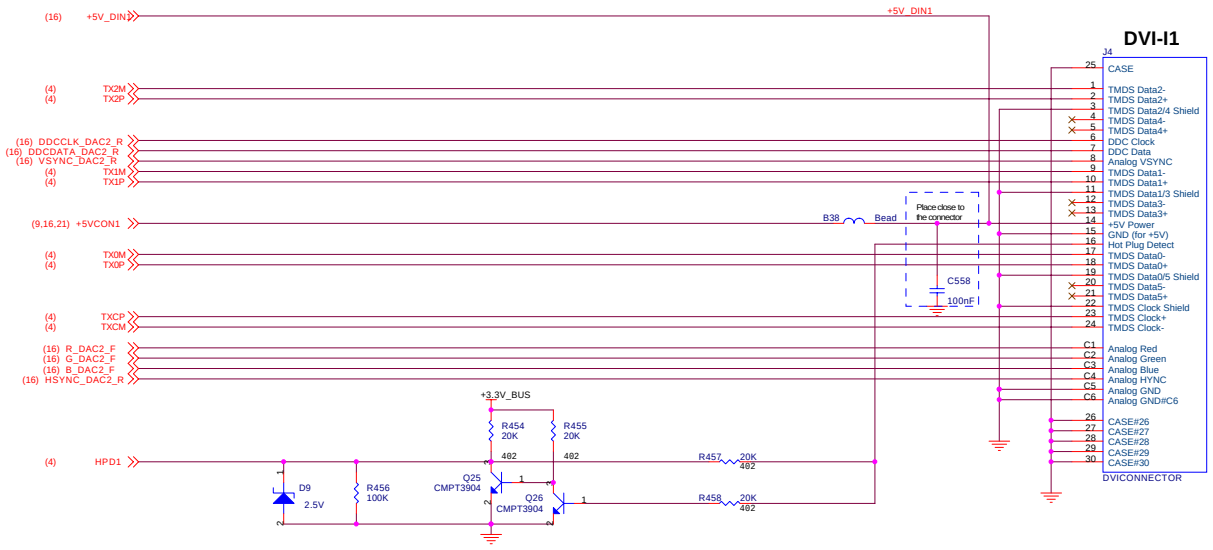
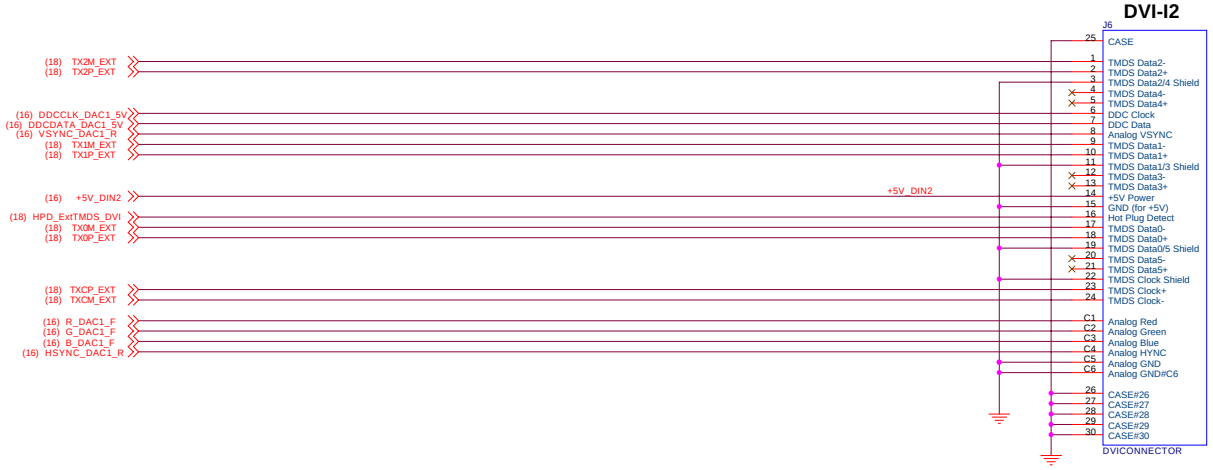
PRIMARY DVI-I CONNECTOR (DVI-I1)





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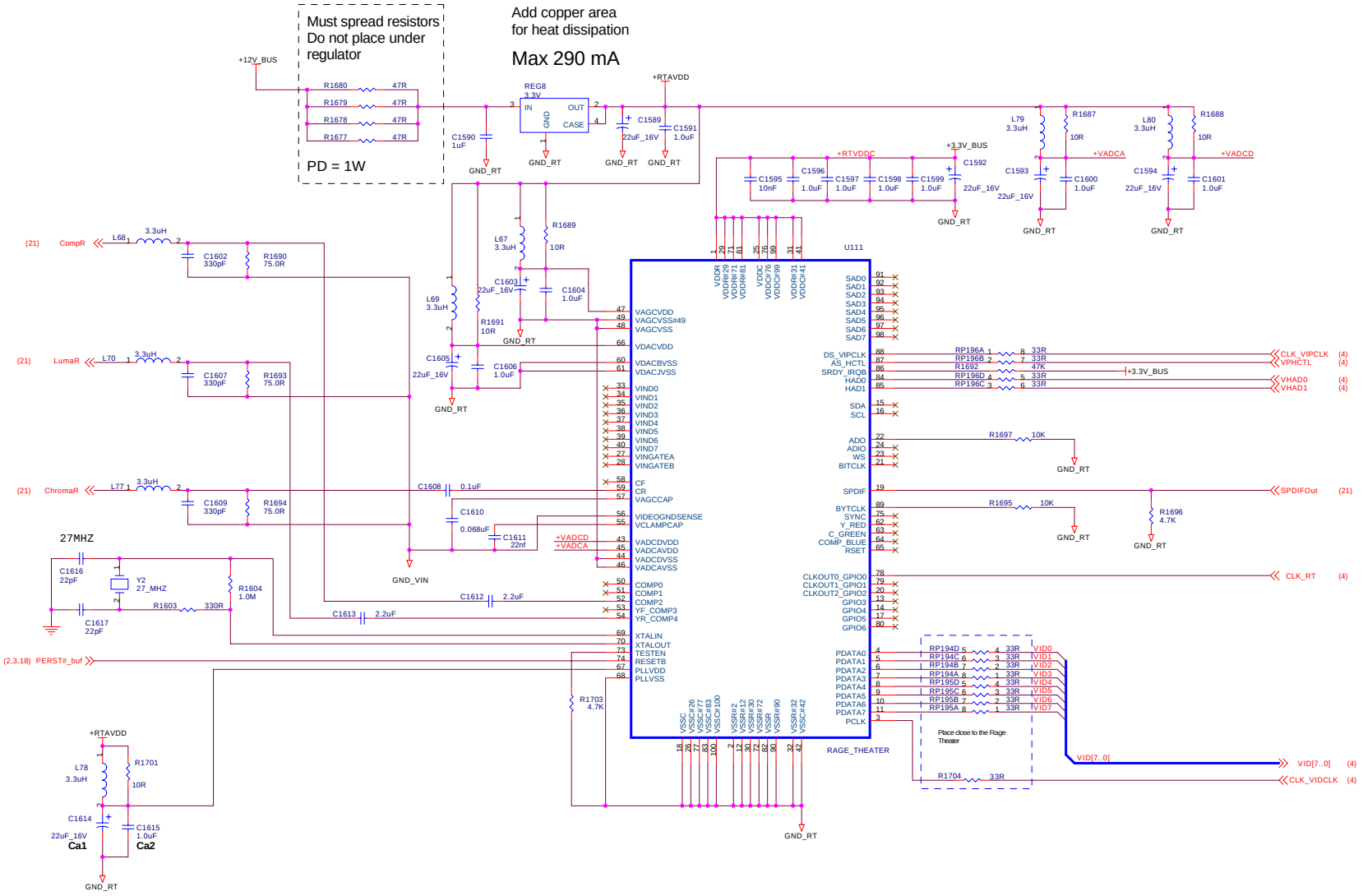

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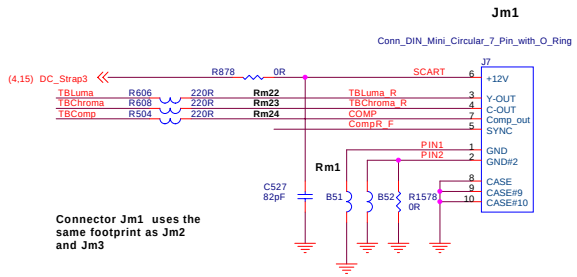
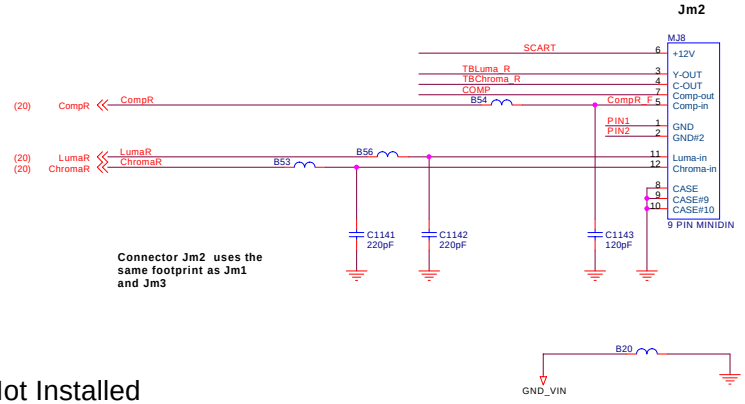
TV Out (SVHS) MiniDIN 7-pin

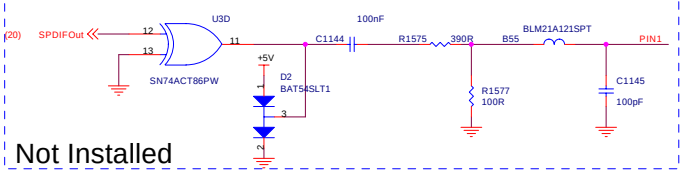


ViVO connector (Installed only if Rage Theater is installed)



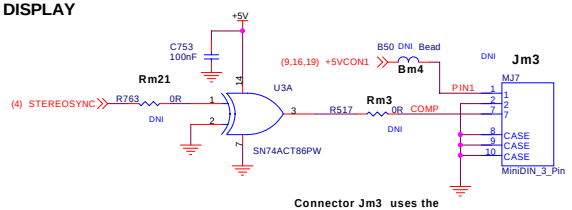
Not Installed

SPDIF - OUT



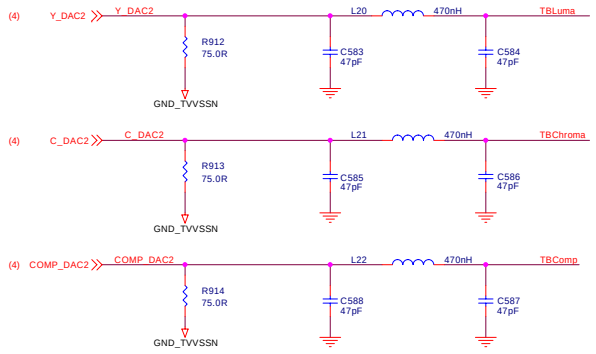
Not Installed

STEREOSCOPIC DISPLAY CONNECTOR



Not Installed

TV-OUT



Not Installed

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CRT
SCREWS

DVI SCREWS

ASSY1
SCREW
JACKSCREW
ASSY

ASSY2
SCREW
JACKSCREW
ASSY

ASSY4
SCREW
JACKSCREW
ASSY

ASSY5
SCREW
JACKSCREW
ASSY

REF2
PCB
109-A38700-00A

Bracket
ANTISTATIC BAG
6_X_11
ASSY

REF3
ATI LOGO LABEL
ATI_LOGO_LABEL

MT1
MT_Hole_0.136_in.
620MOPN004

H103
HEATSINK

H104
NA

FM1
SW_FB

FM2
SW_FB

FM3
SW_FB

FM4
SW_FB

FM5
SW_FB

FM6
SW_FB

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