

NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X

PCI DEVICE ID 0X0=0X200 FOR NV20.

NVVDG SET TO: 1.52V
FBVDD SET TO: 3.47V
FBVDDQ SET TO: 2.59V

HISTORY REVISION:

X00: Based on P50-A06

- See change list in 149- file.
- Set FBVDDQ=2.59V

P50-A07-X01:

- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

P50-A08:

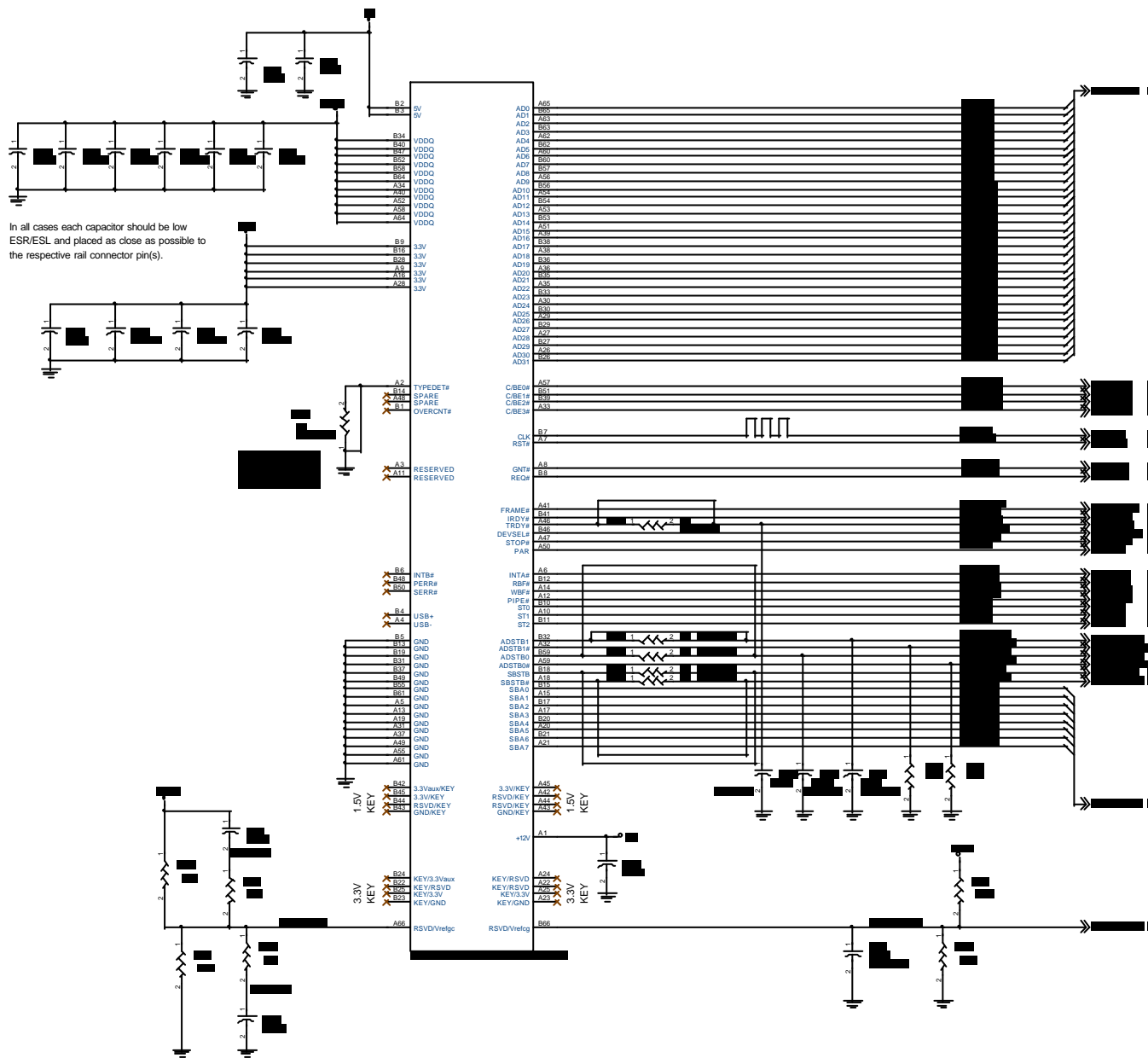
- X04: - Delay PLL_VDD to come up after NVVDG.
- X05: - Added 1UF accross R257.
- X06: - Removed X04-5 above, added a switcher generated PLL delay option.
 - SSEN A cap for 2nd SW changed to 1UF.
 - A05 Si, NVVDG=1.52V

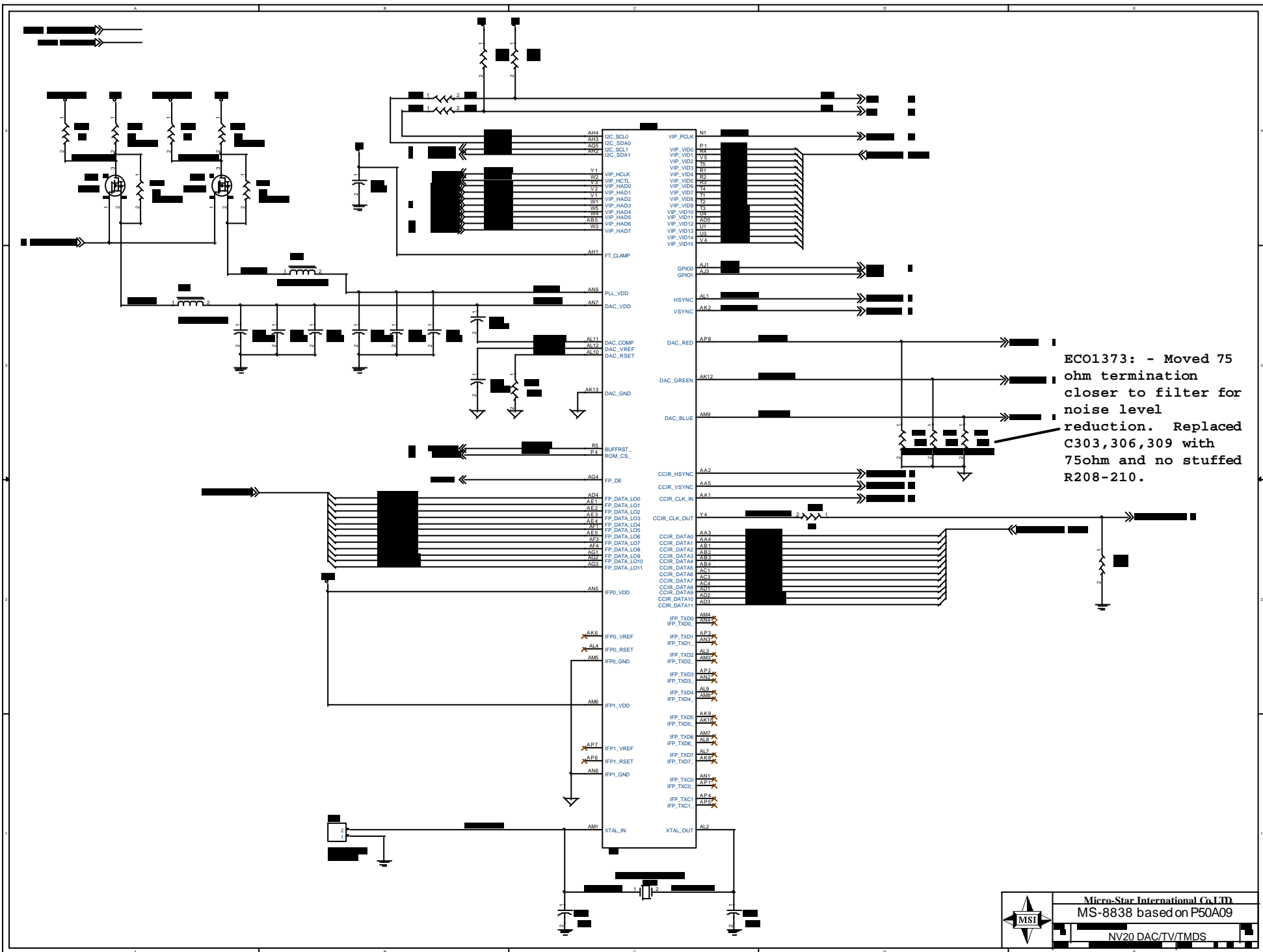
P50-A09:

- X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.
- X03: - Added option to pull up power good to 12V

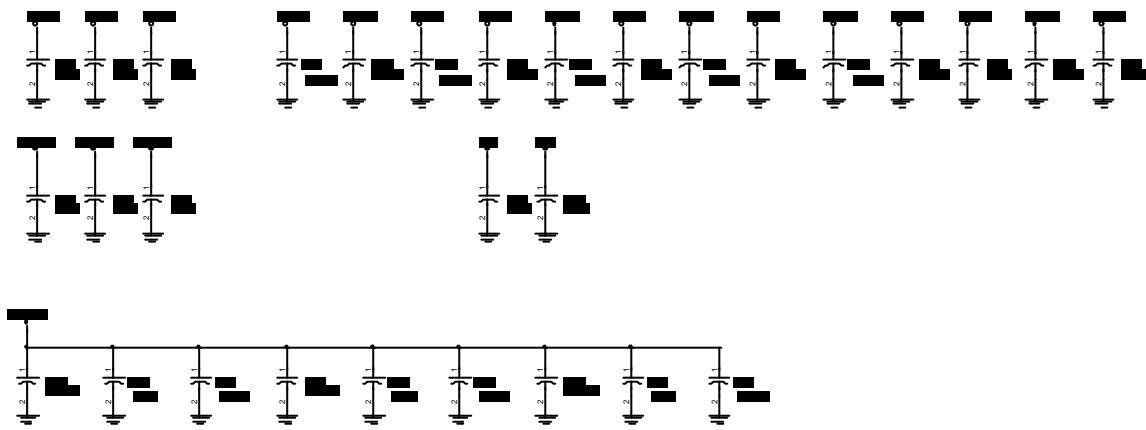
EC01235: - Changed R841 PU to 10K (from 4.7K)

EC01373: - Moved 75 ohm termination closer to filter for noise level reduction.
Replaced C303,306,309 with 75ohm and no stuffed R208-210.





Use thick (non-impedance controlled) traces on XTALIN/OUT



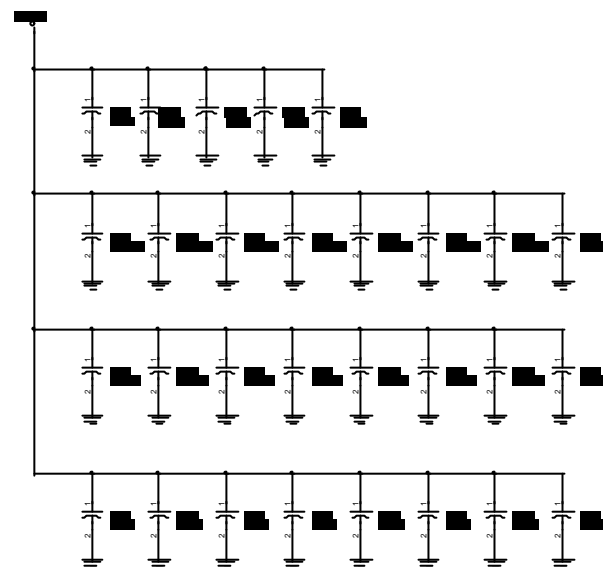
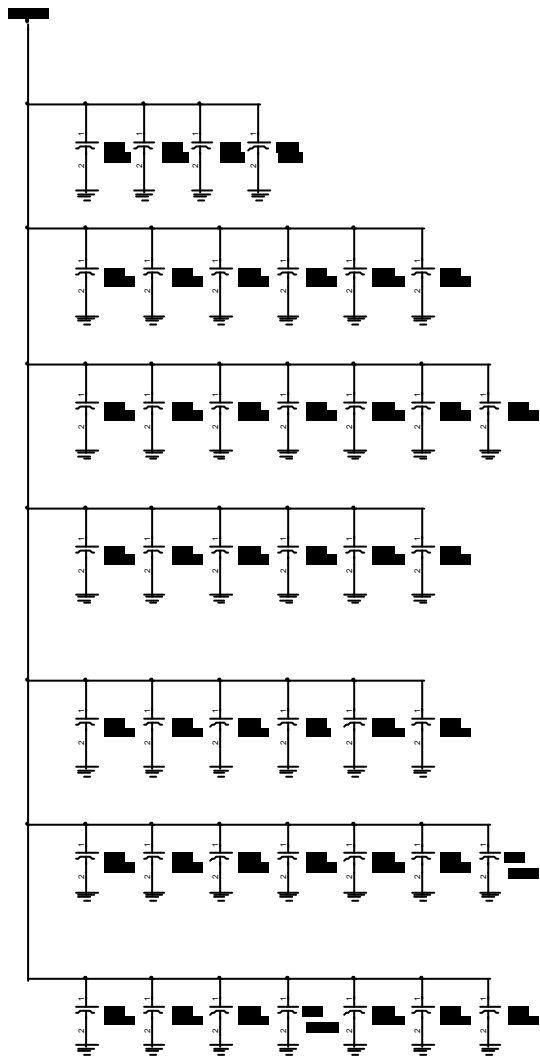
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NV20 DECOUPLING



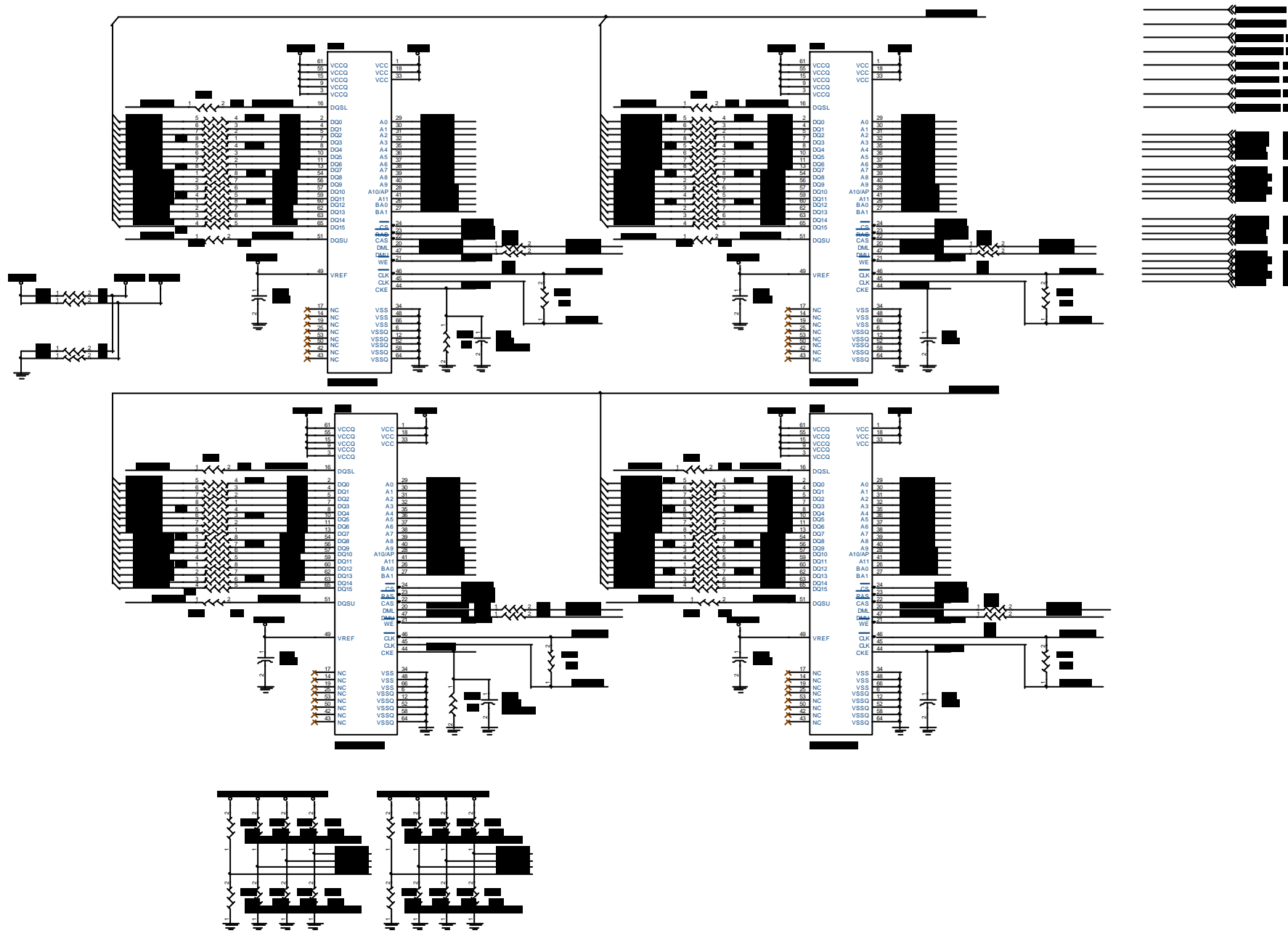
ECO1373: - Moved 75 ohm
termination closer to filter
for noise level reduction.
Replaced C303,306,309 with
75ohm and no stuffed R208-210.

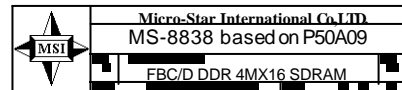
NV20 FBA/B/C/D



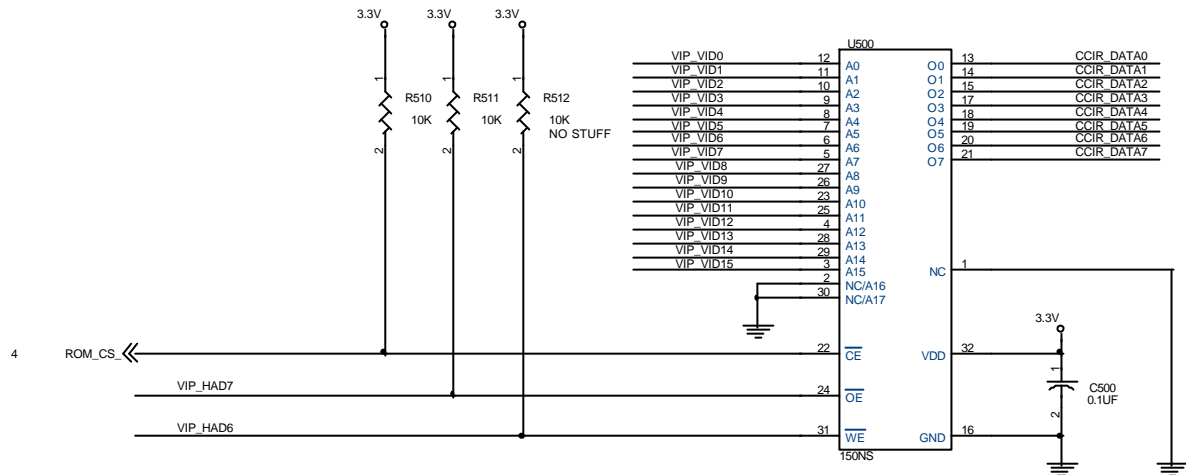
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FB DECOUPLING 4MX16 SDRAM





4,6,13 VIP_VID[15:0] >>
 4,13 VIP_PCLK <<
 4 VIP_HCLK <<
 4 VIP_HCTL <<
 4 VIP_HAD0 >>
 4 VIP_HAD1 >>
 4 VIP_HAD2 >>
 4,6 VIP_HAD3 >>
 4 VIP_HAD4 >>
 4 VIP_HAD5 >>
 4 VIP_HAD6 >>
 4 VIP_HAD7 >>
 4,6,13 CCIR_DATA[11:0] >>
 4,13 CCIR_HSYNC <<
 4,13 CCIR_VSYNC <<
 4,13 CCIR_CLK_IN <<
 4,13 R_CCIR_CLK_OUT <<
 4,13 BUFFRST_ <<
 4,13 SCL <<
 4,13 SDA <<



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