

NV25, P80, DUAL DAC/TMDS, 128MB 4MX32 BGA DDR, TV IN/OUT, GOGGLES, AGP

P80-A03: Re-spin

P80-A00: Based on P53-A00.

A00-X00:
Populate R1034 with 0.01 Ohm
Populate 68K parallel terminations on FBCLK/CLK#

A00-X01:
Isolated GND, AGND and Chassis GND
Corrected Multichip Strap
Changed sync buffers inputs from pin 2 to pin 1 for easy probing.
Corrected PWRGD_FBVDD on memory PS

A00-X02:
Combined CX and SA power filters.
Connected memory PS bootstrap to 12V.
XOR Hotplugs to CS101.
Isolated PLL_VDD from 3.3VL to get rid of 350mV stray voltage.
Combined GND, AGND and Chassis GND

A00-X03:
Changed both TMDS digital powers from 3.3V to 3.3VL.
Added a resistor to base transistor PLL_VDD sequencer.
Added 2nd fan connector.
Added various placement and routing notes.

P80-A01:

A02-X00
Fixed serial rom connections.
Added, again GND isolations.
Added testpoints to various (SAA7108) pins.
Changed DVD clocks series termination to 10R.

A02-X01
Moved VGA con and Bracket to new Sheet 3.2
Moved SR0M to new Sheet 5.2
Moved SR0M to new Sheet 5.2
Moved SEC-DVI Connector to Sheet 6.5
C1162, R1129 changed to No stuff
131-60102-0063-02 is SUB for 131-10102-0061-006
R1072 is changed to 4.2K from 1.5K. Put in BOM.
R1204(Nostuff), R1205=0R Added for FBVDDQ Power sequence after 3.3VL
R207 changed from 118R to 105 Ohm
R277 changed from 118R to 102 Ohm
C1405, C1406 Value changed to 330uf

A02-X02
Design file under Perforce Control.
Changed DACA IDUMP resistor to 0402pkg

A02-X03
Turned DACA SYN buffers into "analog" to ease the AGND antitech.
Added 5 caps on VDDDDV0 pins.
Changed R116 to 0402 pkg.
Enabled AGP Part Write.
Changed PS snubber's resistor to 2.2R (from 100R) per Semtech recommendation.

A02-X04
Combined FCCDDCPWRVGA and DDC+5V nets (del. L711 and C1116) for ease of routing.

A02-X05
Changed R1115 and R1116 back to SMD0603

A02-X06
Isolate SC1175 and SC1102 AGNDs per Semtech recommendations.
Removed 5V power option from SC1102.
Changed crystal loading caps to 10pF and have them reference to digital GND.

A02-X07
Changed snubber resistors to 0805 pkgs
Added RC to SC1102 VREF pin (NO_STUFF)
Removed extra X elements.

A02-X10
Added a 2A fuse on 12V input due to SC1102 current limit bug.

A02-X11
Added ICT to MCHIP_RST_ (GPU.AK5)
Removed SMD0805_SHORT symbols from PS pages (nets merged to GND)

A03-X00
Add two 5-3.0 VR for DVOA and B BUS power supply and change Flash Rom power to DVOA_PWR (3.0V) on Page
Change the decoupling cap. C1349,C1350,C1351,C1362,C907 connect to DVOA_PWR from 3.3V on page 5.1
Change the decoupling cap. C1443,C1444,C1445,C1446,C920 connect to DVOA_PWR from 3.3V on page 5.1
Change series P-ROM U505 power to DVOA_PWR (3.0V) on page 5.2
Change GPU pin AH1,AD1,AC7 connect to DVOA_PWR and change GPU pin AH15,AP8,AD12 connect to DVOB_PWR on Page 6.0.
Connection AGND to GND on page 3.1
Remove R1179,R1180,R1183,R1184,R1198,R1199,C1447
Change R1196,R1197 to "NO STUFF" on page 3.2

A00-X02

1. page 2 add "PCIRST" not gate(7414).
2. page 20 add power sequence.
3. page 8 add "EMI" cap.

P80-A04: Schematics For P Release

A04-X00
Put NO_STUFF for C1123, C1126, C1129, C304, C307, C310
Replace C303, C306, C309, C1122, C1125, C1128 with CAP NPO 0603 15PF 16V 5% (035-20150-0006-000)
Replace L715, L717, L719, L300, L305, L309 with IND 0805 MTLR 5% 0.068UH (130-30680-0006-000)
Replace L716, L718, L720, L302, L306, L310 with IND 0603 MTLR 5% 0.068UH (130-20680-0006-000)

A04-X01
Change C29, C30 value from 33PF to 27PF to improve the color burst stability for conexent and philips TV chip
Change R23 to 12 Ohm from 1K Ohm

A04-X02
Clean up the page number

A04-X03
Clean up the Sch. part description mismatch with the BOM

MS-8875-00A:

A00-X00

*based on P80-A04-X03.
*I/O function modify (Dual D-sub,TV-out,Video capture).

- from 3.1 DAC-I2C0--Pri(page7) change to MS-8863 3.c DAC_A.
- 3.2 VGA CON, BRACKET(page 8) remove P300.
- remove page
 - 5.2 S-ROM(page 16)
 - 6.1 DVOA EXT. TMDSA PRI(page 18)
 - 6.2 DVOA EXT. TMDSA I/O PRI(page 19)
 - 6.3 DVOB EXT. TMSB SEC(page 20)
 - 6.5 DVOB/DACA CONNECTOR(page 22)
 - 7.1 TV-CX ENCODER(page 23)
- 6.0 DVOA/B(page 17)
 - remove U822,R1174,R1175.
 - DVOCCLKOUT add cap pulldown 10PF/C1175 for EMI.
- 7.2 TV-PH CODEC(page 24)
 - COUT and YOUT and CVBSOUT add D2,D4,D6 2.7UH indutor
 - ADD 3.3V to VAAD3.3 and 3.3V to AA3.3V transducer from 7.1 TV-CX ENCODER(page 23).
 - ADD R701 ENC_DVO_CLK0 form (page 23).
 - DVOCCLK_IN add cap pulldown 10PF/C1174 for EMI.

*POWER function cahnge list

- 5.1 P-ROM(page 15) from U824&U825(FAN2500S) change to (AMS1117).
- 8.1 NVVDD POWER SUPPLY(page 26)& 8.2 MEM POWER SUPPLY
 - IRU3007 to supersede U813(SC1175)&U816(SC1102)&U819(SC1565).
 - change all power SWF check by DIP one.
 - remove U815(US1150)

A00-X01

- page 10,11,12,13
R425-R428 & R453-R456 from 10K cahnge to 1K.
- page 7, modify some References.
- page 20 a. add HIP6019 dual-lay circuit.
 - add IRU3007 preserve "FBVDDQ" circuit.
 - modify some References.
- page 2 add RE1 & CE1 by pass for EMI(close GPU).
- page 8 add CE2-CE17 for EMI
- page 4 Remove J202 & J201
- page 20 "FBVDD" & "FBVDDQ" swap.

COMMON -- ALL
NO_STUFF - NOT STUFFED
PRI_VGA - Primary VGA Support
PRI-DVI - Primary DVI-D (Digital) Support
PRI-DVI-I - Primary DVI-I - (Digital & Analog) Support
SEC-DVI-I - Secondary DVI-I (Digital & Analog) Support
PRI-PROT - Primary DVI-VGA protection diodes
SEC-PROT - Secondary DVI-I protection diodes
MEM128 - 128MB EXTENDED MEMORY

NO_STUFF FOR FIRST BUILD
ROM_SER - Serial ROM used
ROM_PAR - Parallel ROM used.

STEREO - USED FOR STEREO GOOGLES
STEREOSYNC1 - USED FOR STEREO GOOGLES
STEREOSYNC2 - USED FOR STEREO GOOGLES
STEREOSYNCS - USED FOR STEREO SYNC BUFFERS
SAA8 - PHILIPS ENCODER/DECODER SAA7108
SAA2 - PHILIPS ENCODER SAA7102
CX - CONEXENT ENCODER CX2587

NO_STUFF FOR FIRST BUILD
EZ1586 - USED TO REGULATE FBVDDQ FROM FBVDD - LINEAR
SC1102 - USED TO REGULATE FBVDD FROM 12V - SWITCHER
SC1565 - USED TO REGULATE 3.3VL FROM 3.3V - LINEAR
SC1175 - USED TO REGULATE NVVDD FROM 3.3V AND 5V - SWITCHER

NO_STUFF FOR FIRST BUILD
PS_SEQ - USED FOR POWER SUPPLY SEQUENCE PROTECTION

VGA-TV-DVI - Used for Primary VGA / TV / Secondary DVI
VGA-DVI - Used for Primary VGA / Secondary DVI only
VGA-TV - Used for Primary VGA / TV
VGA - Used for Primary VGA only
DVI-TV-DVI - Used for Primary DVI / TV / Secondary DVI
DVI-DVI - Used for Primary DVI / Secondary DVI only
DVI-TV - Used for Primary DVI / TV
DVI - Used for Secondary DVI
PASSIVE_HS - Used for Passive heat sink
FAN_HS - Used for Fan heat Sink
SOCKET - PARTS REMOVED WHEN USING A SOCKET

0. TOP PAGE

0025, 4MX32 BGA DDR 64/128MB, 800M, DVI-I, TV-D08M, 20P4K			
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2.1 NV HOST IF

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP-4X

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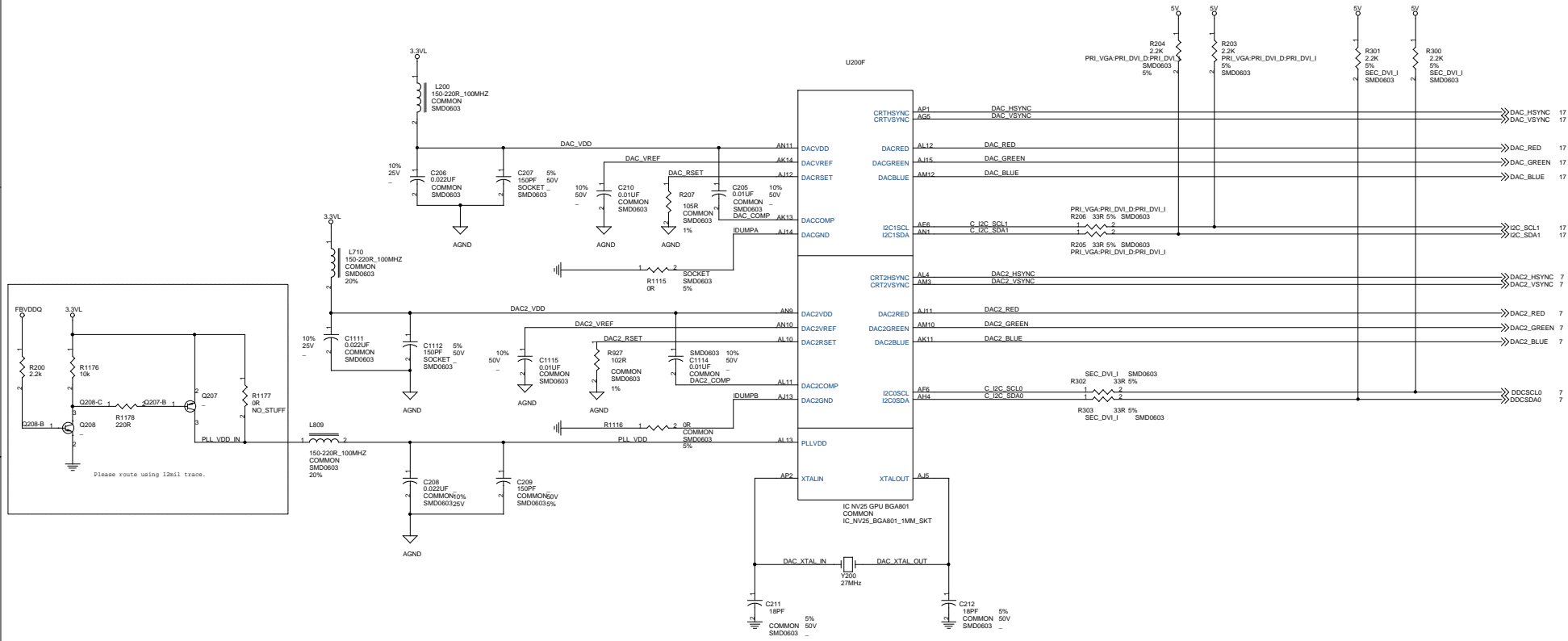
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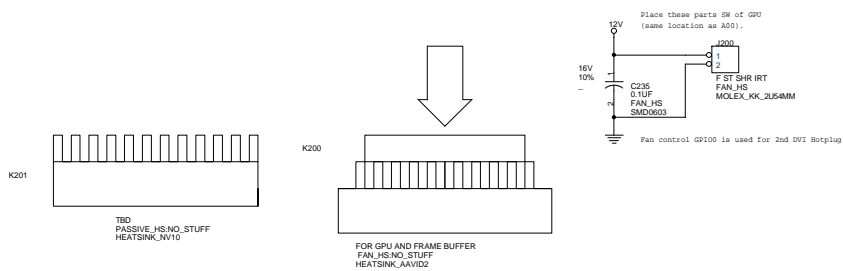
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Use thick (non-impedance controlled) traces on XTALIN/OUT



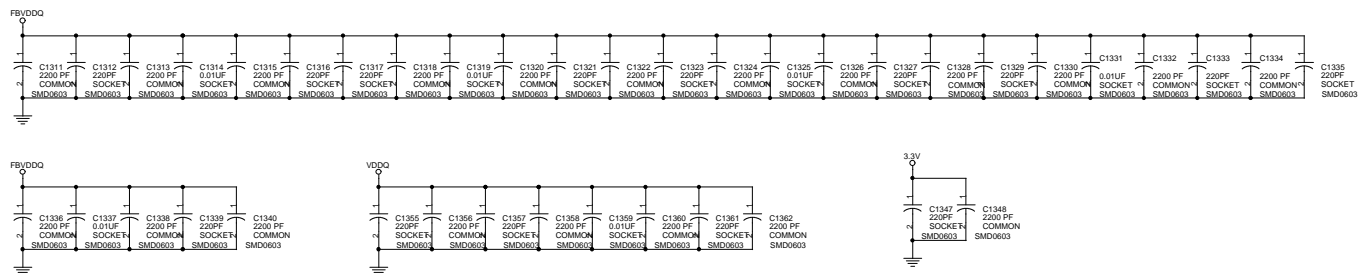
2.2 NV DAC/PLL/I2C

3V25, 4M012, BGA, D08, 64/128MB, B0B, DVI-I, TV-D08B, 32P-61

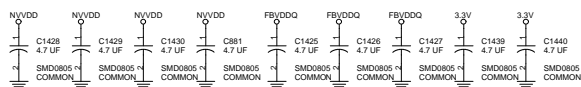
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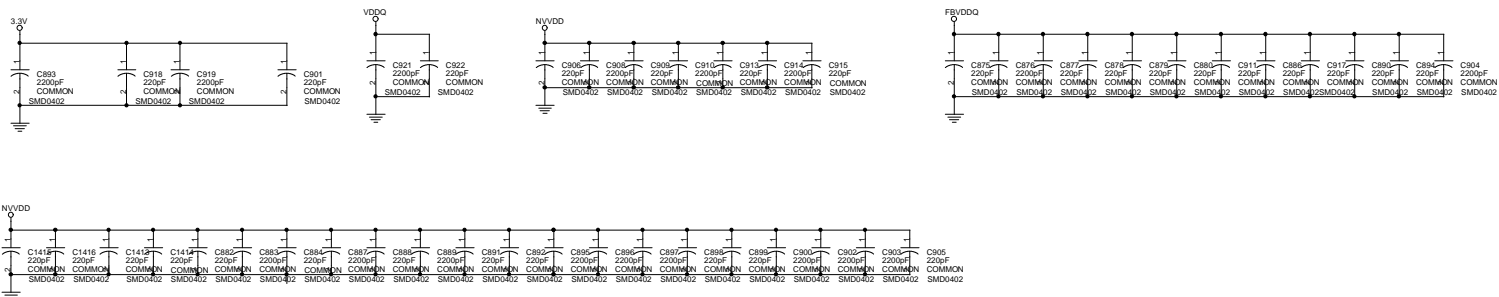
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TOP SIDE CAPS



BOT SIDE CAPS



2.3 NV DECOUPLING

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NV25 BOOT STRAP REGISTER

[1..0] - TWRDGE

0 =
Enabled

BOOT_0_STRAP					
0	16 DVOD12	←	DVOD12	R929 1 2 10k 5% COMMON SMD0402	PCI_AD_STRAP 0 = REVERSED 1 = NORMAL
1	16 DVOD21	←	DVOD21	R931 1 2 10k 5% COMMON SMD0402	SUB_VENDOR 0 = System BIOS 1 = Adapter BIOS
2	16 DVOD22	←	DVOD22	R932 1 2 10k 5% NO STUFF SMD0402	RAM_CFG_0 [3..0] - RAM_CFG - Frame buffer RAM Type configuration 1101 = SS 4MX32 BGA DQS PER BYTE.
3	16 DVOD23	←	DVOD23	R934 1 2 10k 5% NO STUFF SMD0402	
4	16,18 DVOD8	←	DVOD8	R936 1 2 10k 5% NO STUFF SMD0402	
5	16,18 DVOD9	←	DVOD9	R938 1 2 10k 5% NO STUFF SMD0402	
6	16,18 DVOD10	←	DVOD10	R940 1 2 10k 5% COMMON SMD0402	CRYSTAL_0 [1..0] - CRYSTAL 00 = 13.5 MHz 01 = 14.7518 MHz 10 = 27 MHz
22	15,16 VIP_HAD0	←	VIP_HAD0	R942 1 2 10k 5% NO STUFF SMD0402	
7	16,18 DVOD11	←	DVOD11	R944 1 2 10k 5% NO STUFF SMD0402	TWRDGE_0 00 = SSCAN 01 = BTEC 10 = DAL 11 = VGA
8	15,16,18 VIP_VID6	←	VIP_VID6	R946 1 2 10k 5% COMMON SMD0402	
9	15,16,18 VIP_VID7	←	VIP_VID7	R948 1 2 10k 5% COMMON SMD0402	AGP4x 0 = Enabled 1 = Disabled
10	15,16 VIP_VID8	←	VIP_VID8	R950 1 2 10k 5% COMMON SMD0402	AGP_SBA 0 = Enabled 1 = Disabled
11	15,16 VIP_VID9	←	VIP_VID9	R952 1 2 10k 5% COMMON SMD0402	AGP_FASTTR 0 = Enabled 1 = Disabled
14	15,16 VIP_VID12	←	VIP_VID12	R955 1 2 10k 5% COMMON SMD0402	AGP 0 = PCI 1 = AGP

15,16,18 DVOD23[0] >> DVOD23[0]
16 DVOD23[0] >> DVOD23[0]
15,16,18 VIP_VID15[0] >> VIP_VID15[0]

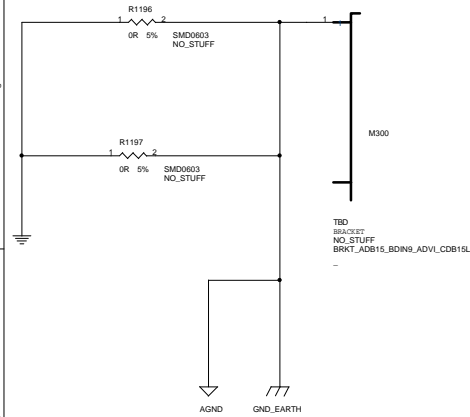
12	15,16 VIP_VID10	←	VIP_VID10	R957 1 2 10k 5% COMMON SMD0402	PCI_DEVID_0 [3..0] - PCI_DEVID - PCI DEVICE ID CODE
13	15,16 VIP_VID11	←	VIP_VID11	R959 1 2 10k 5% COMMON SMD0402	PCI_DEVID_1
20	16 DVOD19	←	DVOD19	R961 1 2 10k 5% NO STUFF SMD0402	PCI_DEVID_2
21	16 DVOD20	←	DVOD20	R963 1 2 10k 5% NO STUFF SMD0402	PCI_DEVID_3
16	15,16 VIP_VID14	←	VIP_VID14	R965 1 2 10k 5% COMMON SMD0402	STRAP_USER_0 [1..0] - STRAP_USER - USER STRAP ID CODE
17	15,16 VIP_VID15	←	VIP_VID15	R967 1 2 10k 5% COMMON SMD0402	
23	16 VIP_HAD1	←	VIP_HAD1	R973 1 2 10k 5% NO STUFF SMD0402	STRAP_FB_0 [1..0] - STRAP_FB - Frame Buffer type selection
24	16 VIP_HAD5	←	VIP_HAD5	R975 1 2 10k 5% COMMON SMD0402	STRAP_FB_1 00 = 64MB 01 = 128MB
15	15,16 VIP_VID13	←	VIP_VID13	R977 1 2 10k 5% COMMON SMD0402	FP_IFACE 0 = 12 bit Flat Panel Interface 1 = 24 bit Flat Panel Interface
25	15,16 VIP_HAD6	←	VIP_HAD6	R979 1 2 10k 5% COMMON SMD0402	STRAP_BRIDGE_EN 0 = Disabled 1 = Enabled
26	15,16 VIP_HAD7	←	VIP_HAD7	R981 1 2 10k 5% COMMON SMD0402	STRAP_BARD_128 0 = Disabled 1 = Enabled
27	16 DVOD00	←	DVOD00	R983 1 2 10k 5% NO STUFF SMD0402	STRAP_MULTICHIP_AGP_DEV 1 0 = Disabled 1 = Enabled
28	16 DVOD01	←	DVOD01	R985 1 2 10k 5% NO STUFF SMD0402	STRAP_MULTICHIP_IO_DEV 1 0 = Disabled 1 = Enabled
29	16 DVOD14	←	DVOD14	R987 1 2 10k 5% COMMON SMD0402	STRAP_ROM_0 [1..0] - STRAP_ROM - Frame Buffer type selection
30	16 DVOD15	←	DVOD15	R989 1 2 10k 5% COMMON SMD0402	

3.0 NV STRAP

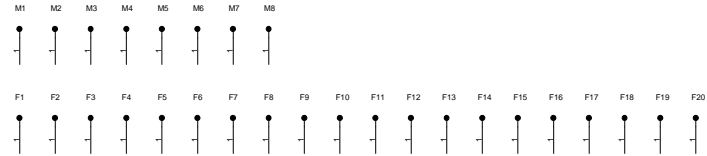
NV25, 4MX32 BGA DQS 64/128MB, SUB, DVI-I, TV-DOSS, AGP4x

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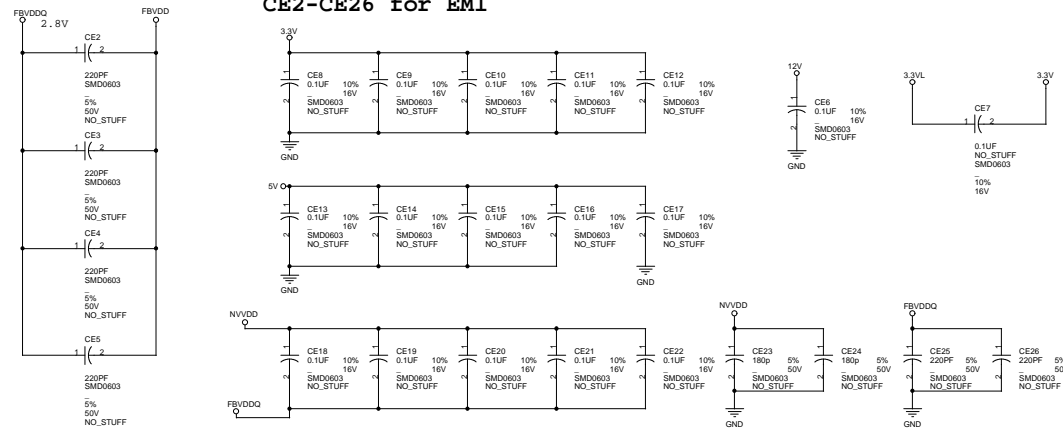
Single point connection for digital and chassis GND.



VGA-TV-DVI - Used for Primary VGA / TV / Secondary DVI
DVI-TV-DVI - Used for Primary DVI / TV / Secondary DVI

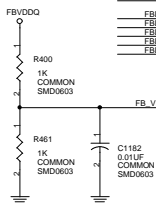


CE2-CE26 for EMI



3.2 BRACKET & EMI cap

3025, 40032, BGA, DIB, 64/128MB, 800, DVI-I, TV-D080, 2up-6K		
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FBD_DATA0_C10	FBD_DATA0	FBC_DATA0	D32	FBC_DATA0
FBD_DATA1_B15	FBD_DATA1	FBC_DATA1	D33	FBC_DATA1
FBD_DATA2_C14	FBD_DATA2	FBC_DATA2	F30	FBC_DATA2
FBD_DATA3_B17	FBD_DATA3	FBC_DATA3	F31	FBC_DATA3
FBD_DATA4_C12	FBD_DATA4	FBC_DATA4	C32	FBC_DATA4
FBD_DATA5_D17	FBD_DATA5	FBC_DATA5	D33	FBC_DATA5
FBD_DATA6_C17	FBD_DATA6	FBC_DATA6	F30	FBC_DATA6
FBD_DATA7_F17	FBD_DATA7	FBC_DATA7	F31	FBC_DATA7
FBD_DATA8_B16	FBD_DATA8	FBC_DATA8	C32	FBC_DATA8
FBD_DATA9_C16	FBD_DATA9	FBC_DATA9	D33	FBC_DATA9
FBD_DATA10_D16	FBD_DATA10	FBC_DATA10	E29	FBC_DATA10
FBD_DATA11_B15	FBD_DATA11	FBC_DATA11	A32	FBC_DATA11
FBD_DATA12_C14	FBD_DATA12	FBC_DATA12	B33	FBC_DATA12
FBD_DATA13_D14	FBD_DATA13	FBC_DATA13	D32	FBC_DATA13
FBD_DATA14_B14	FBD_DATA14	FBC_DATA14	E28	FBC_DATA14
FBD_DATA15_C13	FBD_DATA15	FBC_DATA15	D28	FBC_DATA15
FBD_DATA16_D13	FBD_DATA16	FBC_DATA16	D28	FBC_DATA16
FBD_DATA17_B12	FBD_DATA17	FBC_DATA17	D28	FBC_DATA17
FBD_DATA18_C12	FBD_DATA18	FBC_DATA18	D28	FBC_DATA18
FBD_DATA19_D12	FBD_DATA19	FBC_DATA19	D28	FBC_DATA19
FBD_DATA20_B11	FBD_DATA20	FBC_DATA20	D28	FBC_DATA20
FBD_DATA21_C11	FBD_DATA21	FBC_DATA21	D28	FBC_DATA21
FBD_DATA22_D11	FBD_DATA22	FBC_DATA22	D28	FBC_DATA22
FBD_DATA23_B10	FBD_DATA23	FBC_DATA23	D28	FBC_DATA23
FBD_DATA24_C10	FBD_DATA24	FBC_DATA24	D28	FBC_DATA24
FBD_DATA25_D10	FBD_DATA25	FBC_DATA25	D28	FBC_DATA25
FBD_DATA26_B09	FBD_DATA26	FBC_DATA26	D28	FBC_DATA26
FBD_DATA27_C09	FBD_DATA27	FBC_DATA27	D28	FBC_DATA27
FBD_DATA28_D09	FBD_DATA28	FBC_DATA28	D28	FBC_DATA28
FBD_DATA29_B08	FBD_DATA29	FBC_DATA29	D28	FBC_DATA29
FBD_DATA30_C08	FBD_DATA30	FBC_DATA30	D28	FBC_DATA30
FBD_DATA31_D08	FBD_DATA31	FBC_DATA31	D28	FBC_DATA31

FBB_DATA0_A40	FBB_DATA0	FBA_DATA0	A427	FBA_DATA0
FBB_DATA1_V33	FBB_DATA1	FBA_DATA1	A428	FBA_DATA1
FBB_DATA2_W32	FBB_DATA2	FBA_DATA2	A429	FBA_DATA2
FBB_DATA3_V31	FBB_DATA3	FBA_DATA3	A430	FBA_DATA3
FBB_DATA4_V34	FBB_DATA4	FBA_DATA4	A431	FBA_DATA4
FBB_DATA5_V31	FBB_DATA5	FBA_DATA5	A432	FBA_DATA5
FBB_DATA6_V32	FBB_DATA6	FBA_DATA6	A433	FBA_DATA6
FBB_DATA7_V31	FBB_DATA7	FBA_DATA7	A434	FBA_DATA7
FBB_DATA8_V34	FBB_DATA8	FBA_DATA8	A435	FBA_DATA8
FBB_DATA9_V32	FBB_DATA9	FBA_DATA9	A436	FBA_DATA9
FBB_DATA10_V32	FBB_DATA10	FBA_DATA10	A437	FBA_DATA10
FBB_DATA11_T33	FBB_DATA11	FBA_DATA11	A438	FBA_DATA11
FBB_DATA12_V32	FBB_DATA12	FBA_DATA12	A439	FBA_DATA12
FBB_DATA13_R34	FBB_DATA13	FBA_DATA13	A440	FBA_DATA13
FBB_DATA14_M33	FBB_DATA14	FBA_DATA14	A441	FBA_DATA14
FBB_DATA15_V30	FBB_DATA15	FBA_DATA15	A442	FBA_DATA15
FBB_DATA16_K31	FBB_DATA16	FBA_DATA16	A443	FBA_DATA16
FBB_DATA17_C30	FBB_DATA17	FBA_DATA17	A444	FBA_DATA17
FBB_DATA18_V30	FBB_DATA18	FBA_DATA18	A445	FBA_DATA18
FBB_DATA19_K30	FBB_DATA19	FBA_DATA19	A446	FBA_DATA19
FBB_DATA20_F33	FBB_DATA20	FBA_DATA20	A447	FBA_DATA20
FBB_DATA21_G32	FBB_DATA21	FBA_DATA21	A448	FBA_DATA21
FBB_DATA22_E34	FBB_DATA22	FBA_DATA22	A449	FBA_DATA22
FBB_DATA23_E32	FBB_DATA23	FBA_DATA23	A450	FBA_DATA23
FBB_DATA24_E32	FBB_DATA24	FBA_DATA24	A451	FBA_DATA24
FBB_DATA25_E33	FBB_DATA25	FBA_DATA25	A452	FBA_DATA25
FBB_DATA26_D30	FBB_DATA26	FBA_DATA26	A453	FBA_DATA26
FBB_DATA27_H30	FBB_DATA27	FBA_DATA27	A454	FBA_DATA27
FBB_DATA28_C34	FBB_DATA28	FBA_DATA28	A455	FBA_DATA28
FBB_DATA29_D33	FBB_DATA29	FBA_DATA29	A456	FBA_DATA29
FBB_DATA30_F31	FBB_DATA30	FBA_DATA30	A457	FBA_DATA30
FBB_DATA31_G30	FBB_DATA31	FBA_DATA31	A458	FBA_DATA31

<<FBA_DATA[31:0] 10
 <<FBB_DATA[31:0] 11
 <<FBC_DATA[31:0] 12
 <<FBD_DATA[31:0] 13

<<FBA_ADR[13:0] 10
 <<FBB_ADR[13:0] 11
 <<FBC_ADR[13:0] 12
 <<FBD_ADR[13:0] 13

<<FBA_DQS[3:0] 10
 <<FBB_DQS[3:0] 11
 <<FBC_DQS[3:0] 12
 <<FBD_DQS[3:0] 13

<<FBA_DM[3:0] 10
 <<FBB_DM[3:0] 11
 <<FBC_DM[3:0] 12
 <<FBD_DM[3:0] 13

<<FBA_CS[1:0] 10
 <<FBB_CS[1:0] 11
 <<FBC_CS[1:0] 12
 <<FBD_CS[1:0] 13

<<FBA_RAS 10
 <<FBB_RAS 10
 <<FBC_RAS 10
 <<FBD_RAS 10

<<FBA_CLK0 10
 <<FBB_CLK0 10
 <<FBC_CLK0 10
 <<FBD_CLK0 10

<<FBB_RAS 11
 <<FBB_CAS 11
 <<FBB_WE 11
 <<FBB_CS0 11
 <<FBB_CS1 11

<<FBB_CLK0 11
 <<FBB_CLK0B 11
 <<FBB_CLK1 11
 <<FBB_CLK1B 11
 <<FBB_CS1 11

<<FBC_RAS 12
 <<FBC_CAS 12
 <<FBC_WE 12
 <<FBC_CS0 12
 <<FBC_CS1 12

<<FBC_CLK0 12
 <<FBC_CLK0B 12
 <<FBC_CLK1 12
 <<FBC_CLK1B 12
 <<FBC_CKE 12

<<FBD_RAS 13
 <<FBD_CAS 13
 <<FBD_WE 13
 <<FBD_CS0 13
 <<FBD_CS1 13

<<FBD_CLK0 13
 <<FBD_CLK0B 13
 <<FBD_CLK1 13
 <<FBD_CLK1B 13
 <<FBD_CKE 13

4.1 NV FBA/B/C/D

NV25, 4Mx12 BGA, DFB 64/128MB, 30MB, DVI-L, TV-D080, 300MHz

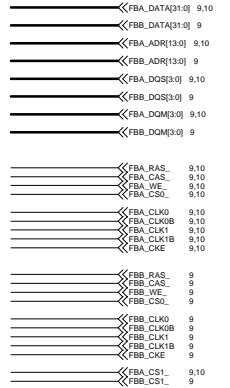
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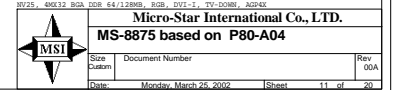
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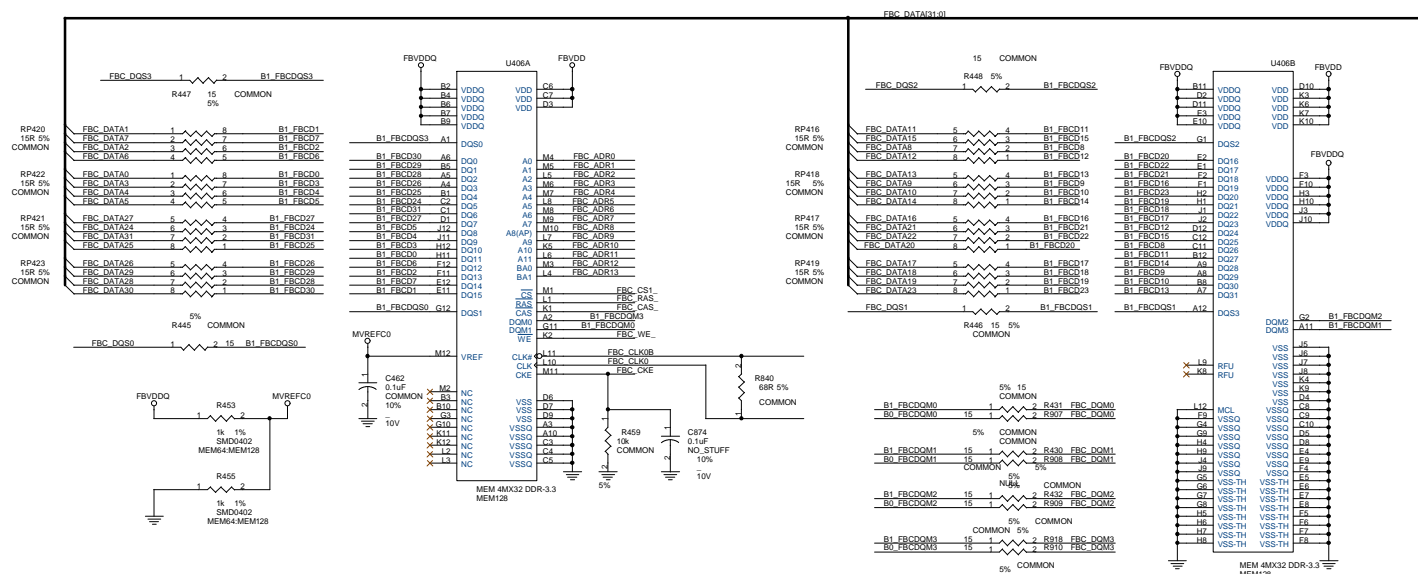
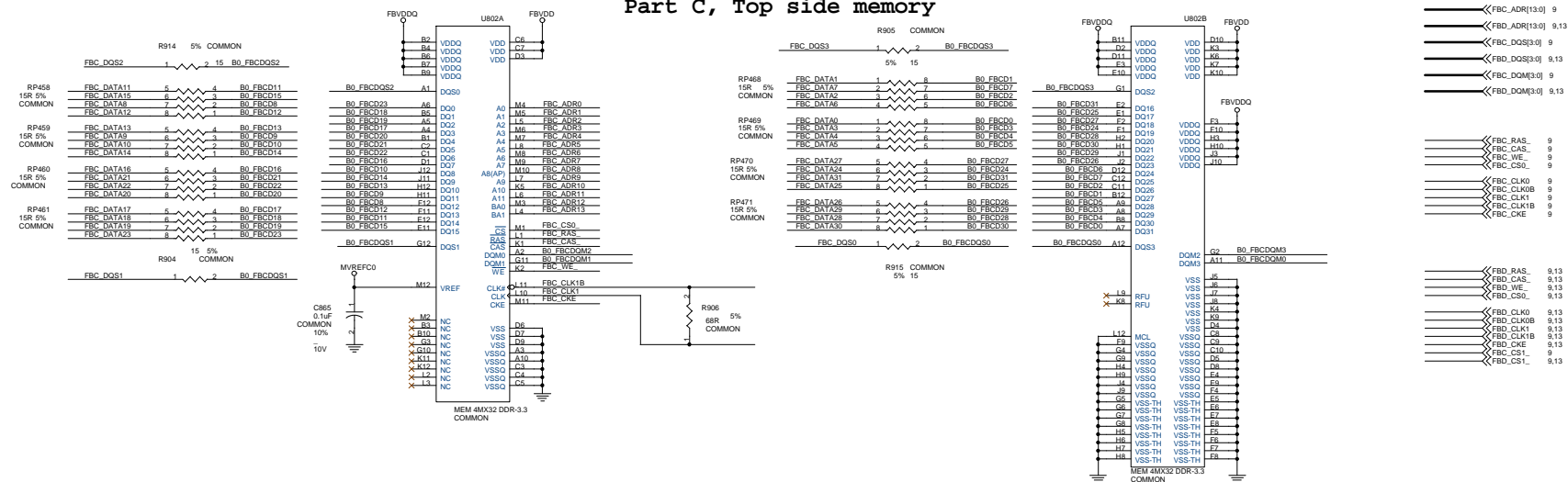
FDUSD URO5B FDUSD



4.3 FBB DDR 4MX32 SDRAM



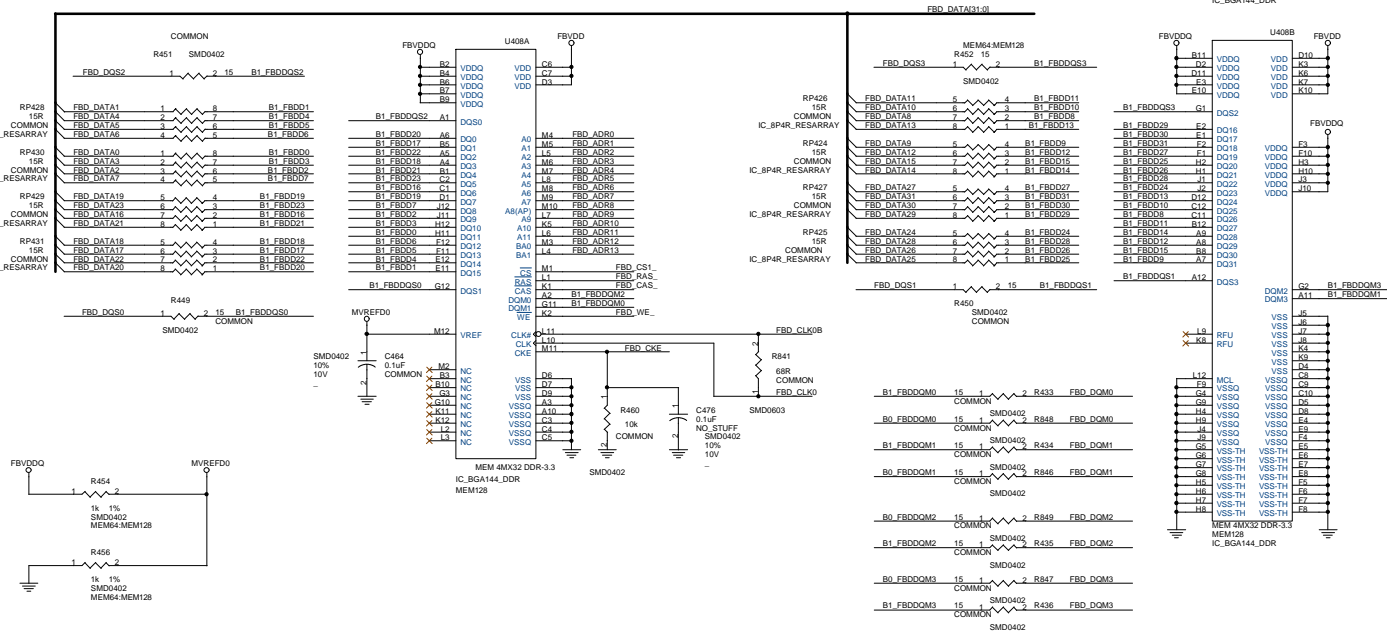
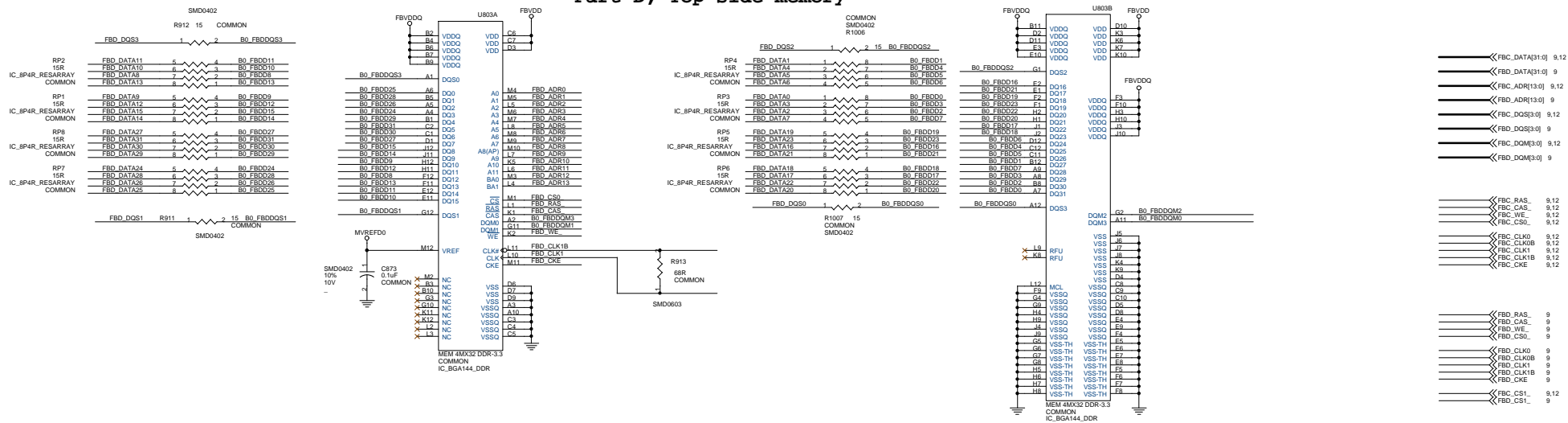
Part C, Top side memory



Part C, Bottom side memory

4.4 FBC DDR 4MX32 SDRAM

Part D, Top side memory



Part D, Bottom side memory

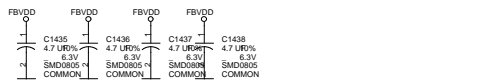
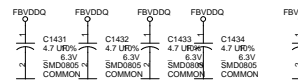
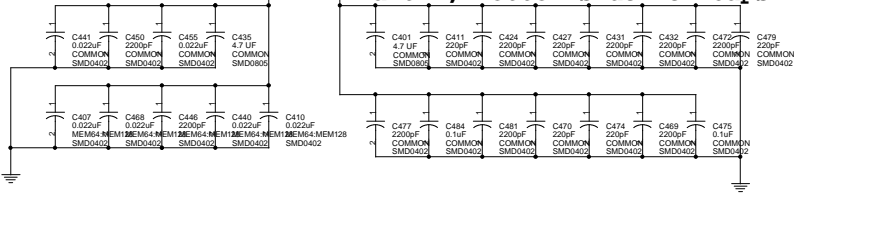
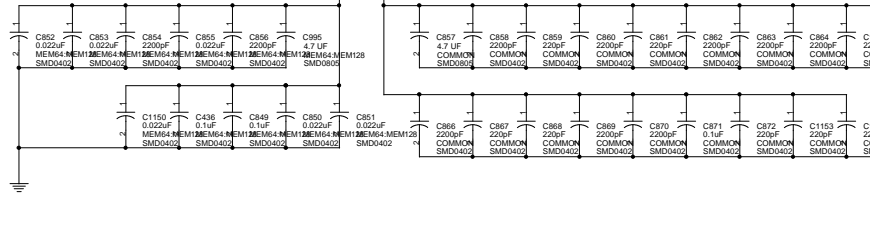
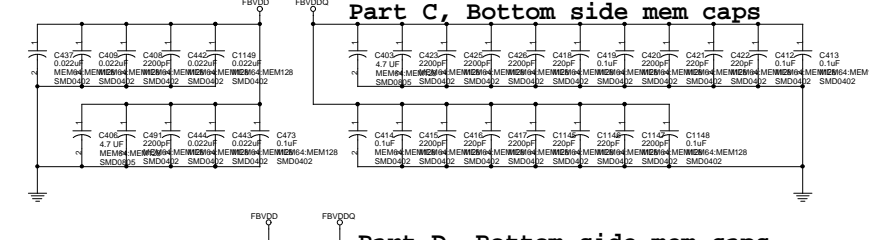
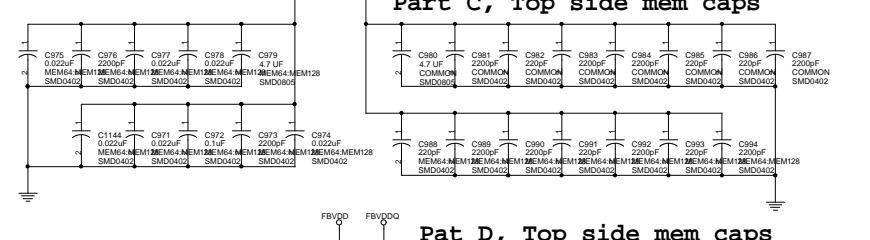
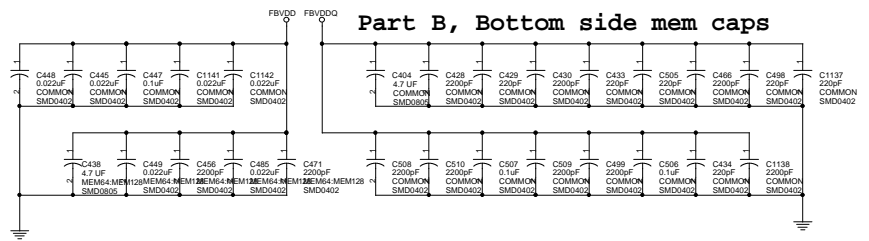
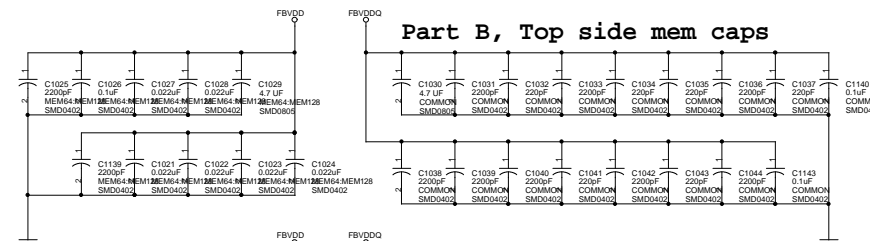
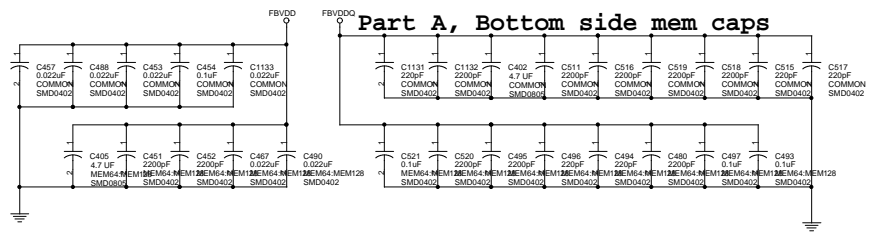
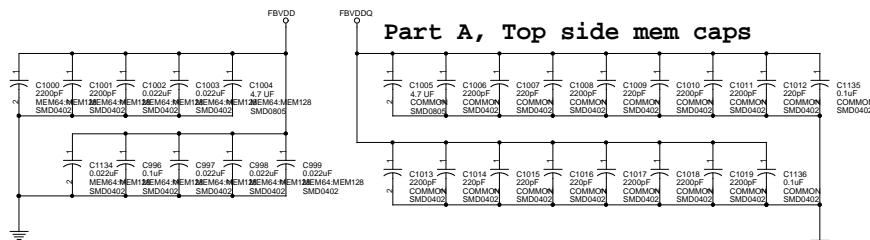
4.5 FBD DDR 4MX32 SDRAM

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-OUT, AGP-EX



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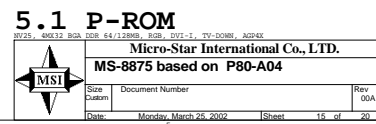
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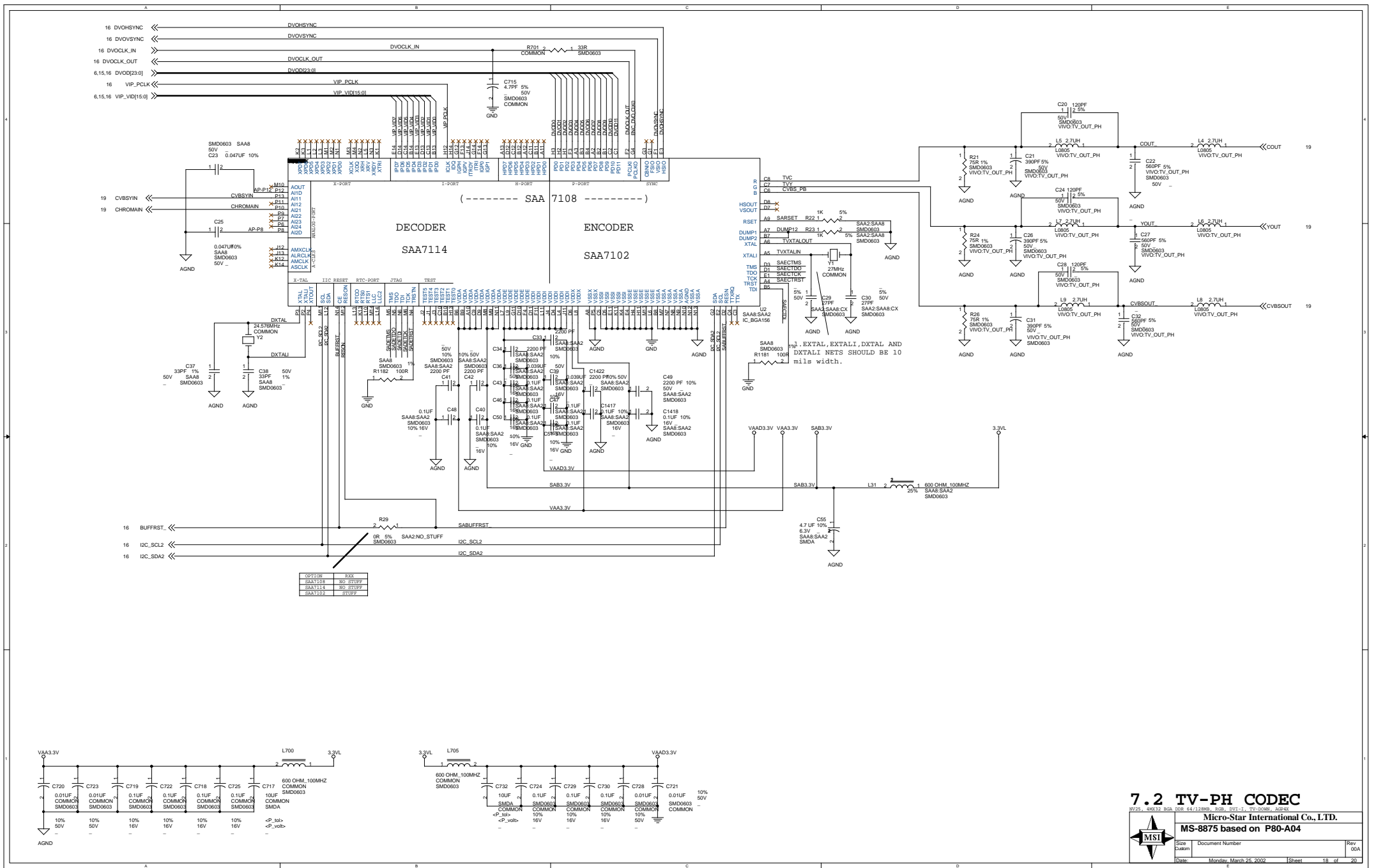


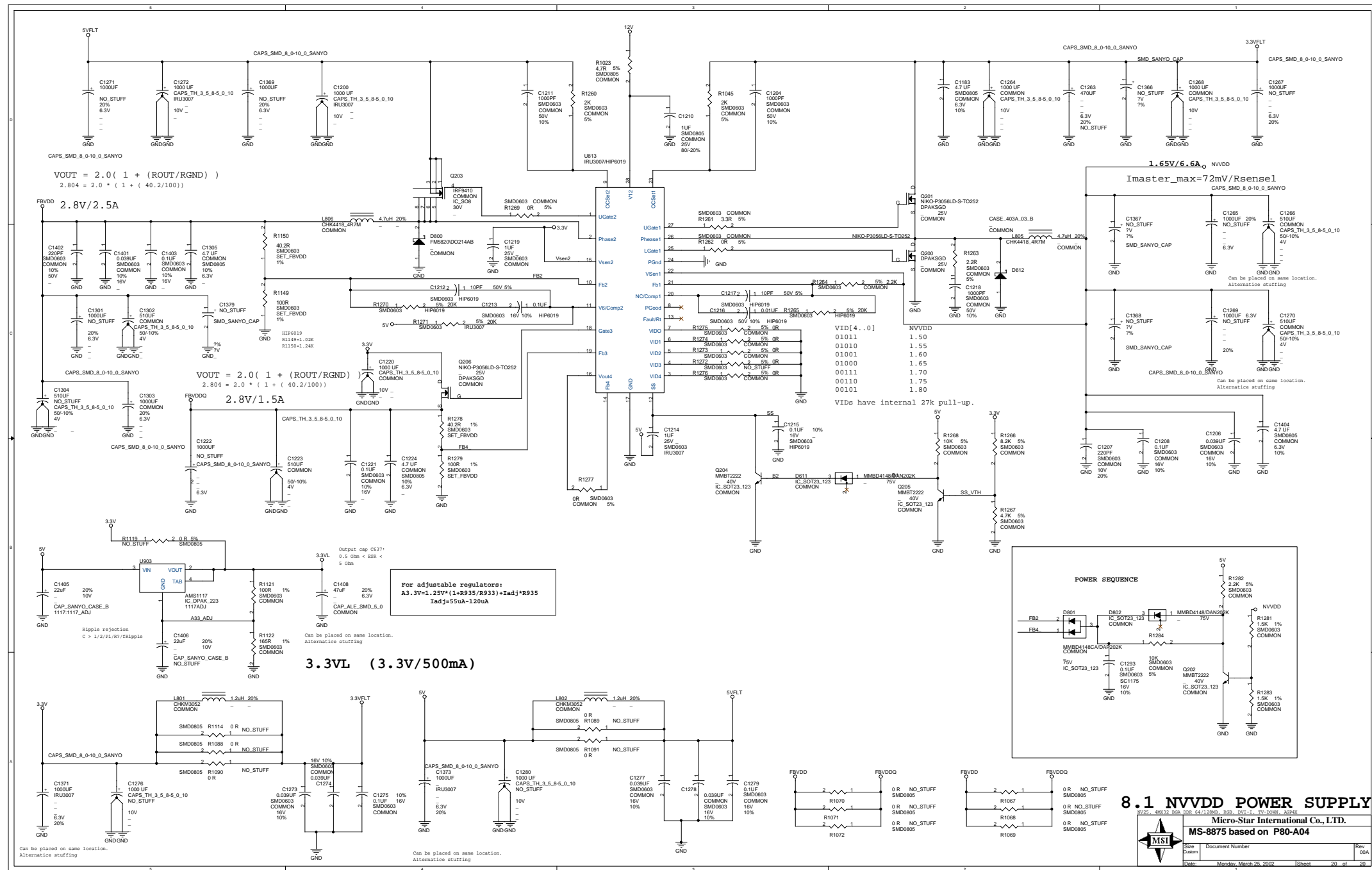
4.6 BGA MEMORY DECOUPLING

02/21, 402132 BGA D08 64/128MB, 800, DVI-I, TV-D08B, J2041

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8.1 NVVDD POWER SUPPLY

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-OUT, AGP4X

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Date: Monday, March

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