

P1001-B02

GA100-883 PCIe Gen4 HBM2

TESLA PASSIVE

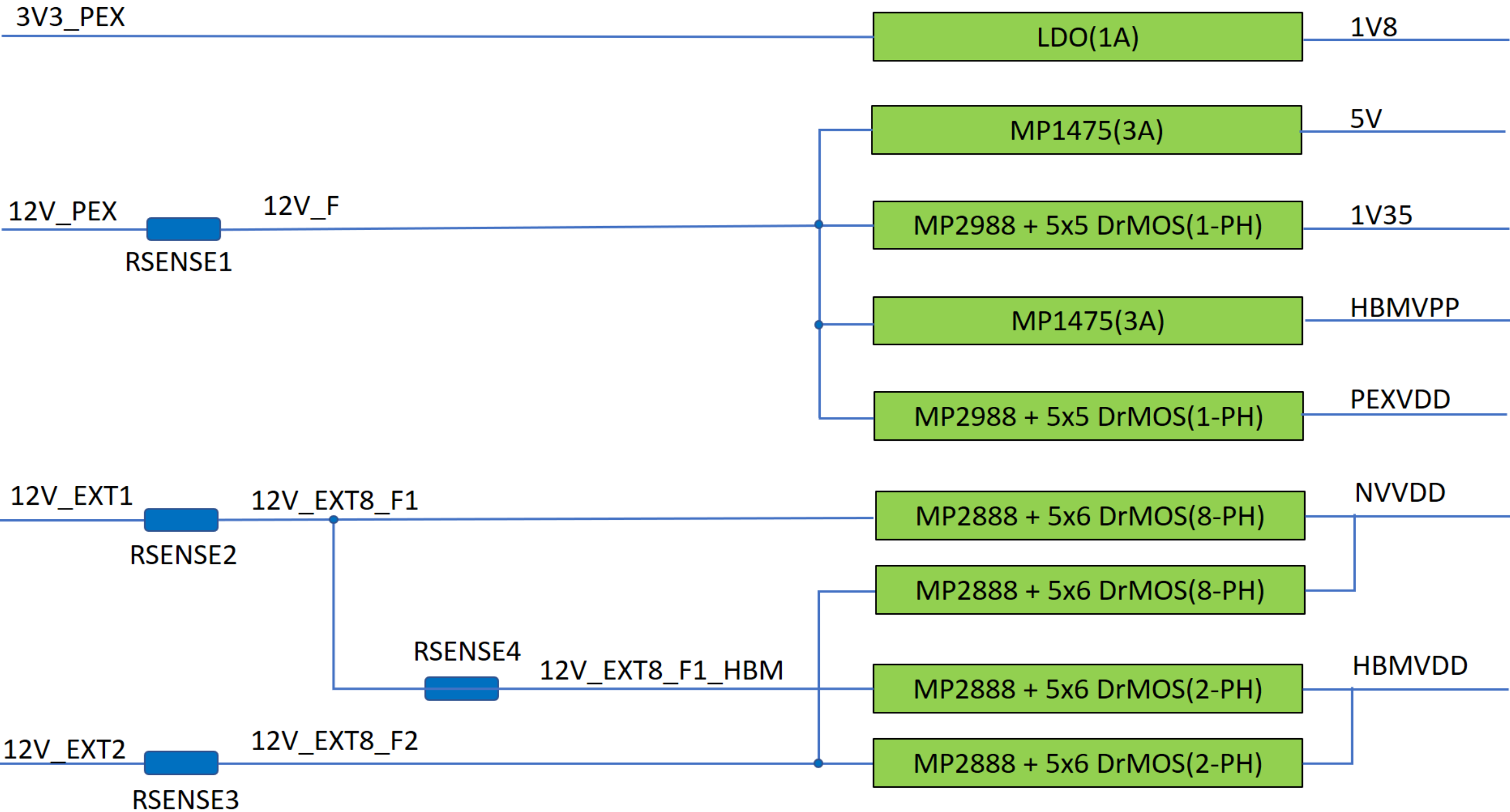
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Power Topology

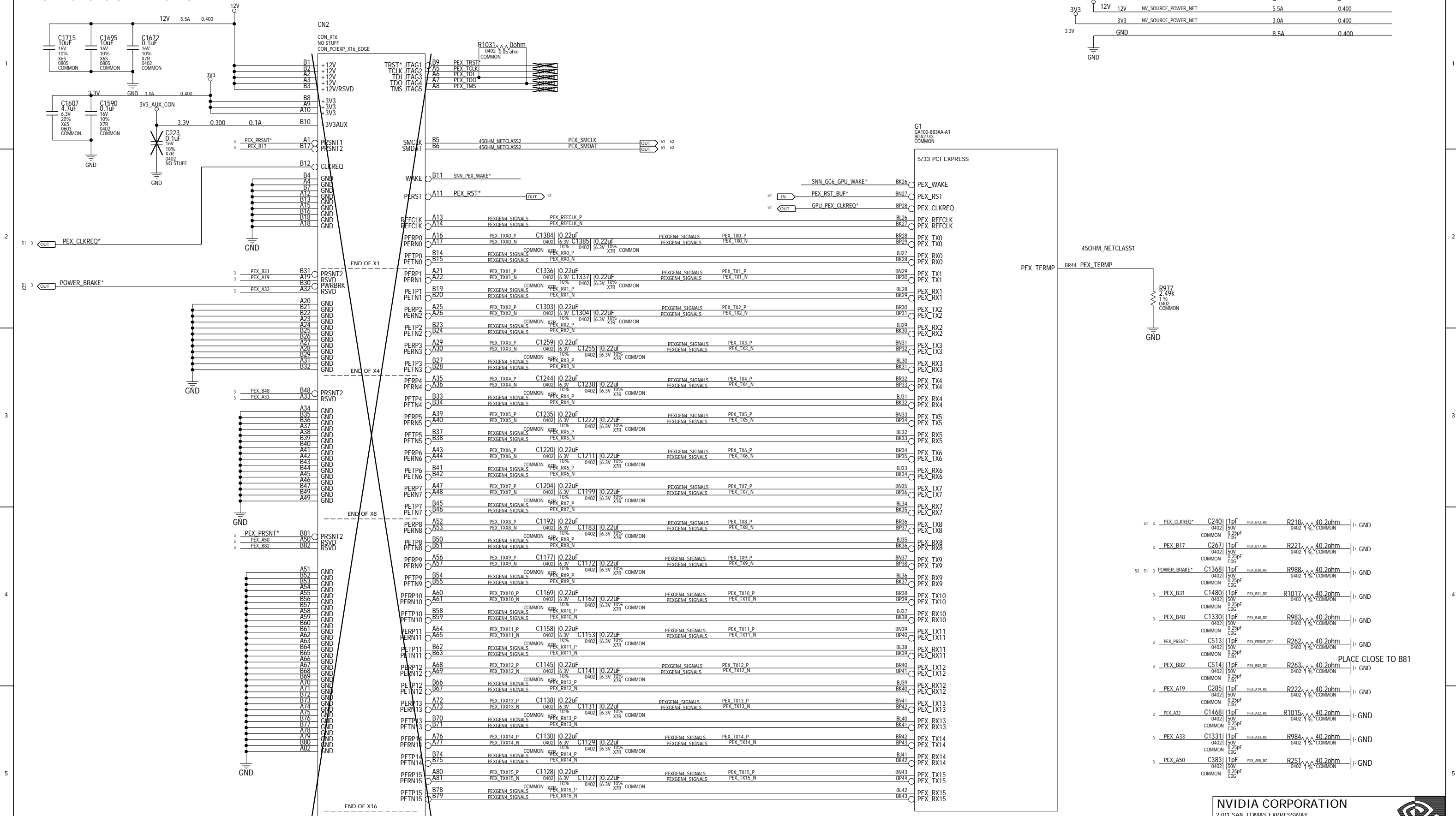


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ASSEMBLY	P1001 B01 SKU200 TESLA PASSIVE
PAGE DETAIL	Power Topology


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IO PCIe CONNECTOR



ASSEMBLY	P1001 B01 SKU200 TESLA PASSIVE
PAGE DETAIL	IO: PCIe CONNECTOR

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GPU NVHS 0,1,2 and 3

1

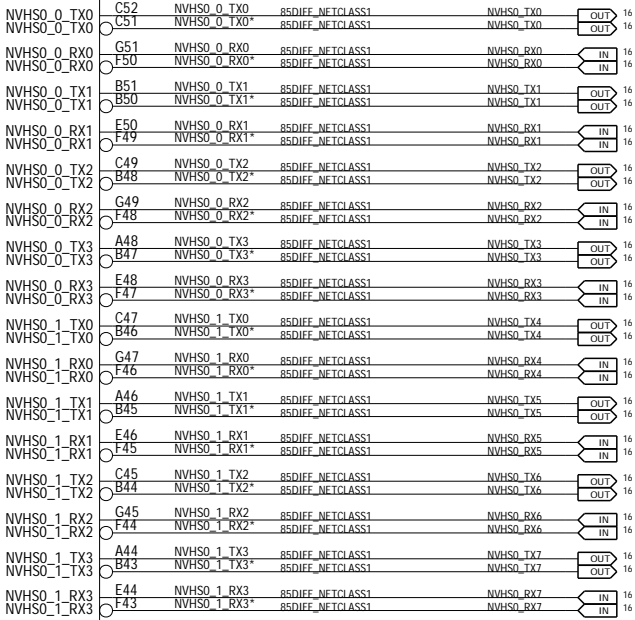
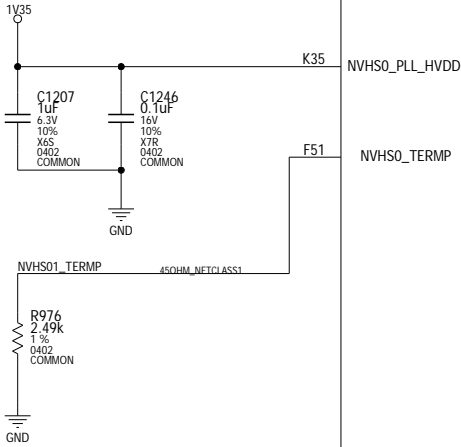
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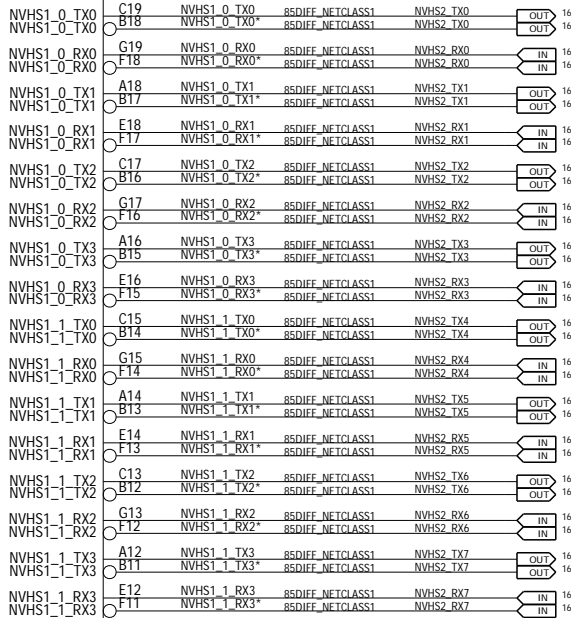
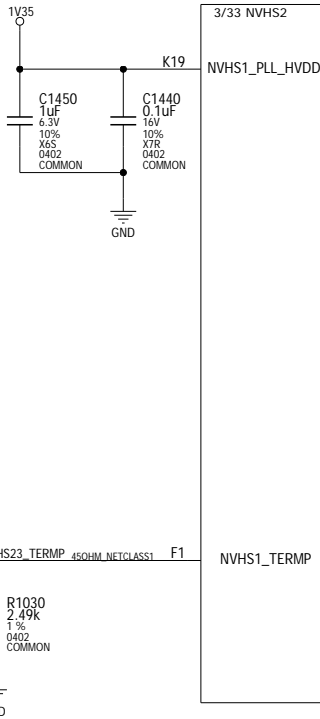
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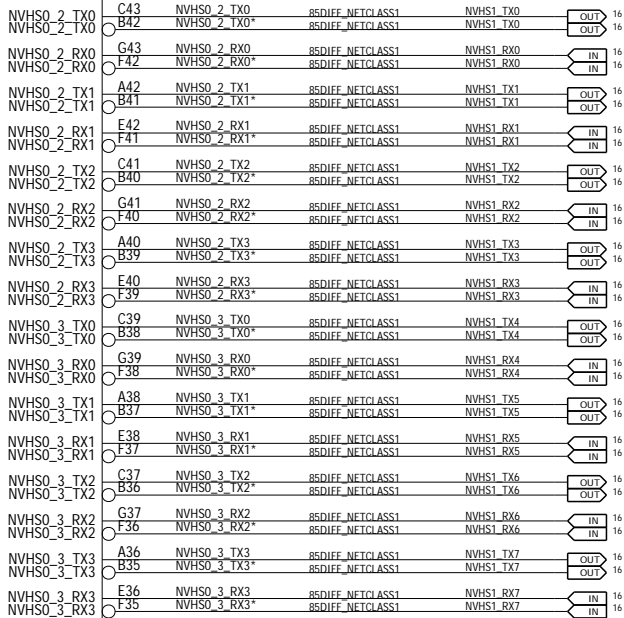
G1
GA100-883AA-A1
BGA2743
COMMON
1/33 NVHS0



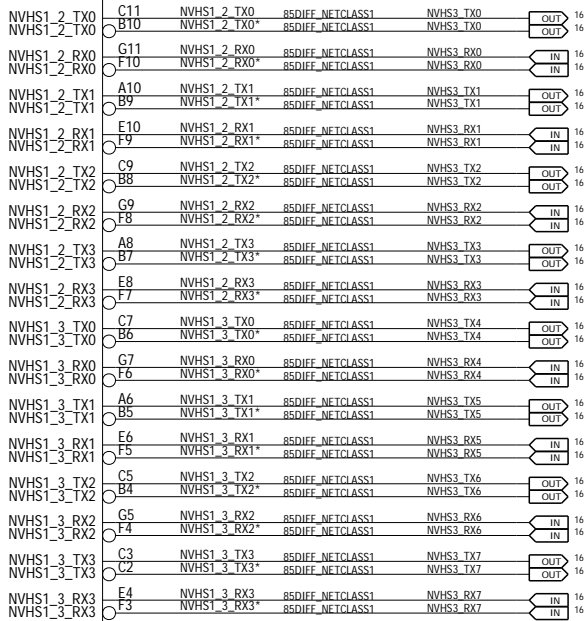
G1
GA100-883AA-A1
BGA2743
COMMON
3/33 NVHS2



G1
GA100-883AA-A1
BGA2743
COMMON
2/33 NVHS1



G1
GA100-883AA-A1
BGA2743
COMMON
4/33 NVHS3



1

2

3

4

5

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PAGE DETAIL	GPU: NVHS 0,1,2 & 3

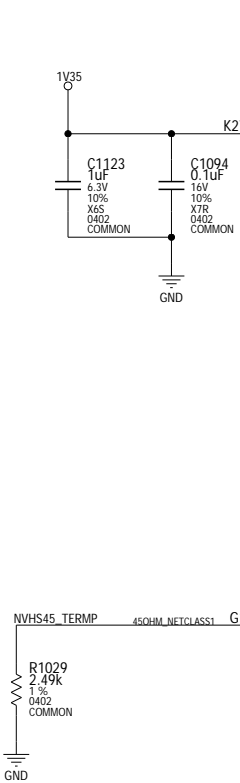
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GPU NVHS 4 and 5



G1
GA100-883AA-A1
BGA2743
COMMON

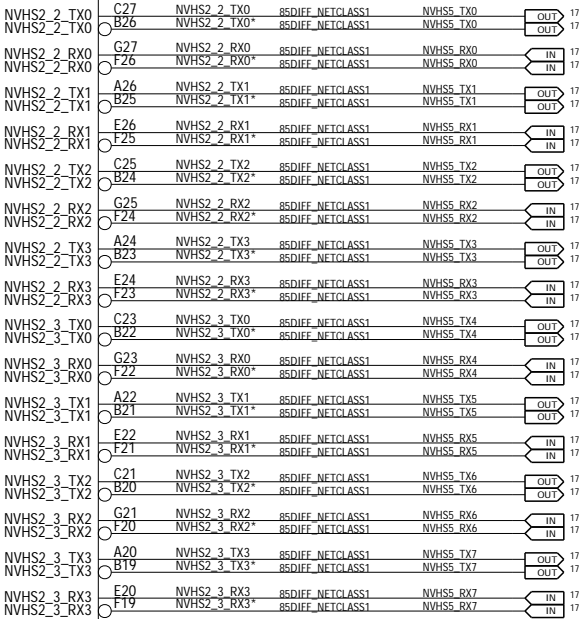
24/33 NVHS4

NVHS2_PLL_HVDD

NVHS2_TERM

G1
GA100-883AA-A1
BGA2743
COMMON

25/33 NVHS5



G1
GA100-883AA-A1
BGA2743
COMMON

21/33 NC

SNN GV100 NC00	B17	NC
SNN GV100 NC01	BN49	NC
SNN GV100 NC02	BN51	NC
SNN GV100 NC03	BP26	NC
SNN GV100 NC04	B11	NC
SNN GV100 NC05	B12	NC
SNN GV100 NC06	B13	NC
SNN GV100 NC07	B14	NC
SNN GV100 NC08	BK4	NC
SNN GV100 NC09	BK5	NC
SNN GV100 NC0A	BN6	NC
SNN GV100 NC0B	BK2	NC
SNN GV100 NC0C	BL2	NC
SNN GV100 NC0D	BK6	NC
SNN GV100 NC0E	B16	NC
SNN GV100 NC0F	BK7	NC
SNN GV100 NC10	BN7	NC
SNN GV100 NC11	BN45	NC
SNN GV100 NC12	BP49	NC
SNN GV100 NC13	BP50	NC
SNN GV100 NC14	BN47	NC
SNN GV100 NC15	BP51	NC
SNN GV100 NC16	BR26	NC
SNN GV100 NC17	BR46	NC
SNN GV100 NC18	BR48	NC
SNN GV100 NC19	BP27	NC
SNN GV100 NC1A	BP45	NC
SNN GV100 NC1B	BL3	NC
SNN GV100 NC1C	BL5	NC
SNN GV100 NC1D	BL6	NC
SNN GV100 NC1E	BN2	NC
SNN GV100 NC1F	BN3	NC
SNN GV100 NC20	BN4	NC
SNN GV100 NC21	BN2	NC
SNN GV100 NC22	BN3	NC
SNN GV100 NC23	BN4	NC
SNN GV100 NC24	BN5	NC
SNN GV100 NC25	BN6	NC
SNN GV100 NC26	BN18	NC
SNN GV100 NC27	BN22	NC
SNN GV100 NC28	BN26	NC
SNN GV100 NC29	BN5	NC
SNN GV100 NC2A	BP3	NC
SNN GV100 NC2B	BP4	NC
SNN GV100 NC2C	BP5	NC
SNN GV100 NC2D	BP46	NC
SNN GV100 NC2E	BP47	NC
SNN GV100 NC2F	BP48	NC

G1
GA100-883AA-A1
BGA2743
COMMON

31/33 TEST PINS

SNN TESTIO D0	B17	TESTIO_D0
SNN TESTIO D1	BK17	TESTIO_D1
SNN TESTIO D2	BN17	TESTIO_D2
SNN TESTIO D3	BP17	TESTIO_D3
SNN TESTIO D4	BR18	TESTIO_D4
SNN TESTIO D5	BP18	TESTIO_D5
SNN TESTIO D6	BL18	TESTIO_D6
SNN TESTIO D7	BK18	TESTIO_D7
SNN TESTIO D8	B19	TESTIO_D8
SNN TESTIO D9	BK19	TESTIO_D9
SNN TESTIO DA	BN19	TESTIO_D10
SNN TESTIO DB	BP19	TESTIO_D11

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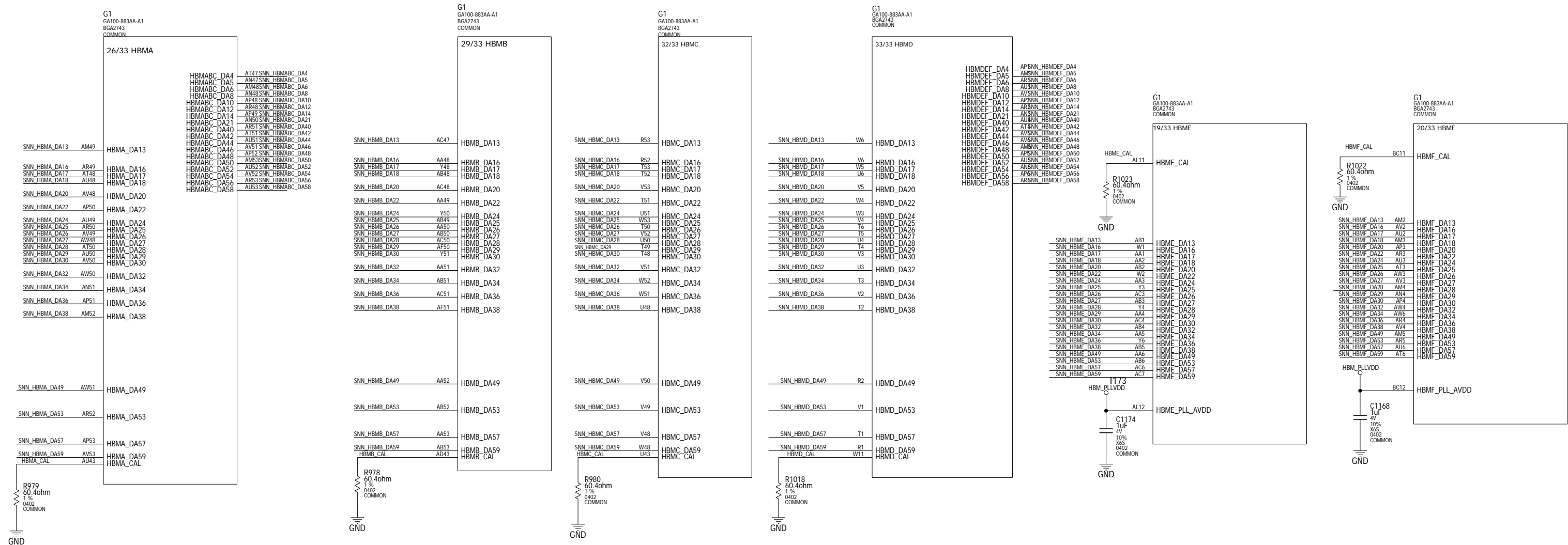
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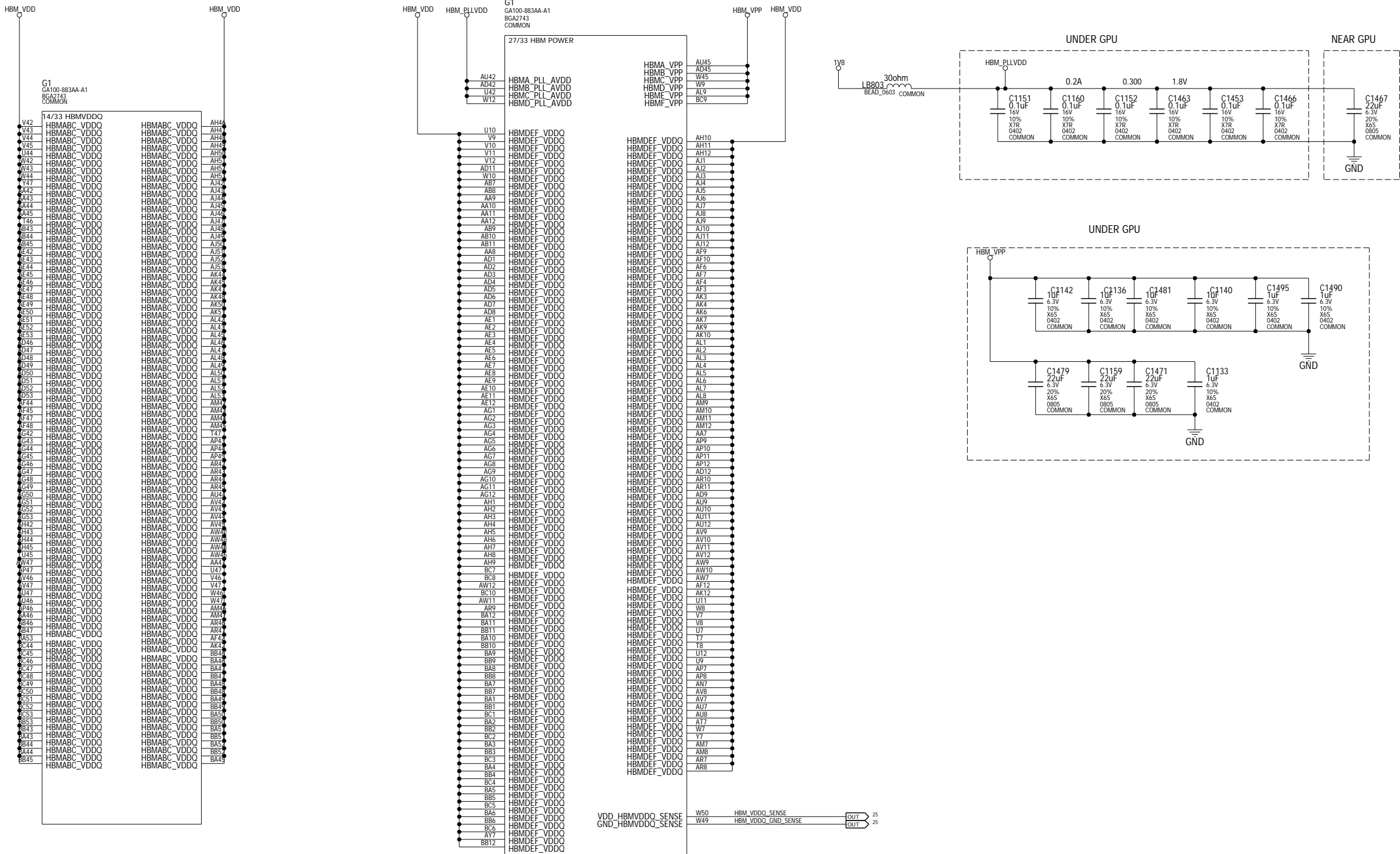
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PAGE DETAIL	GPU: NVHS 4 and 5

GPU HBM SIGNAL CONNECTIONS



GPU:HBM POWER CONNECTIONS



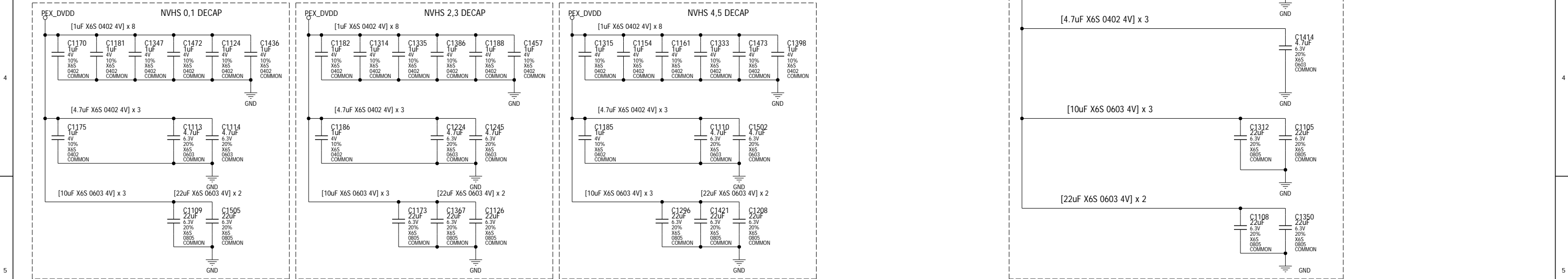
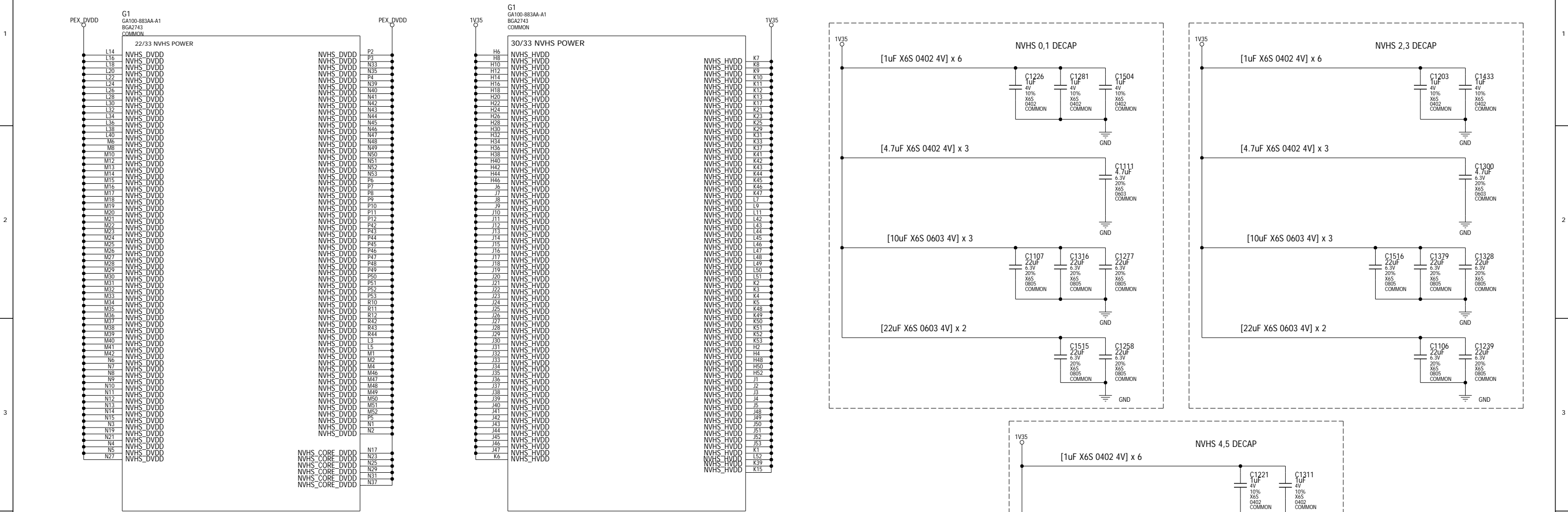
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[illegible]

A	B	C	D	E	F	G	H
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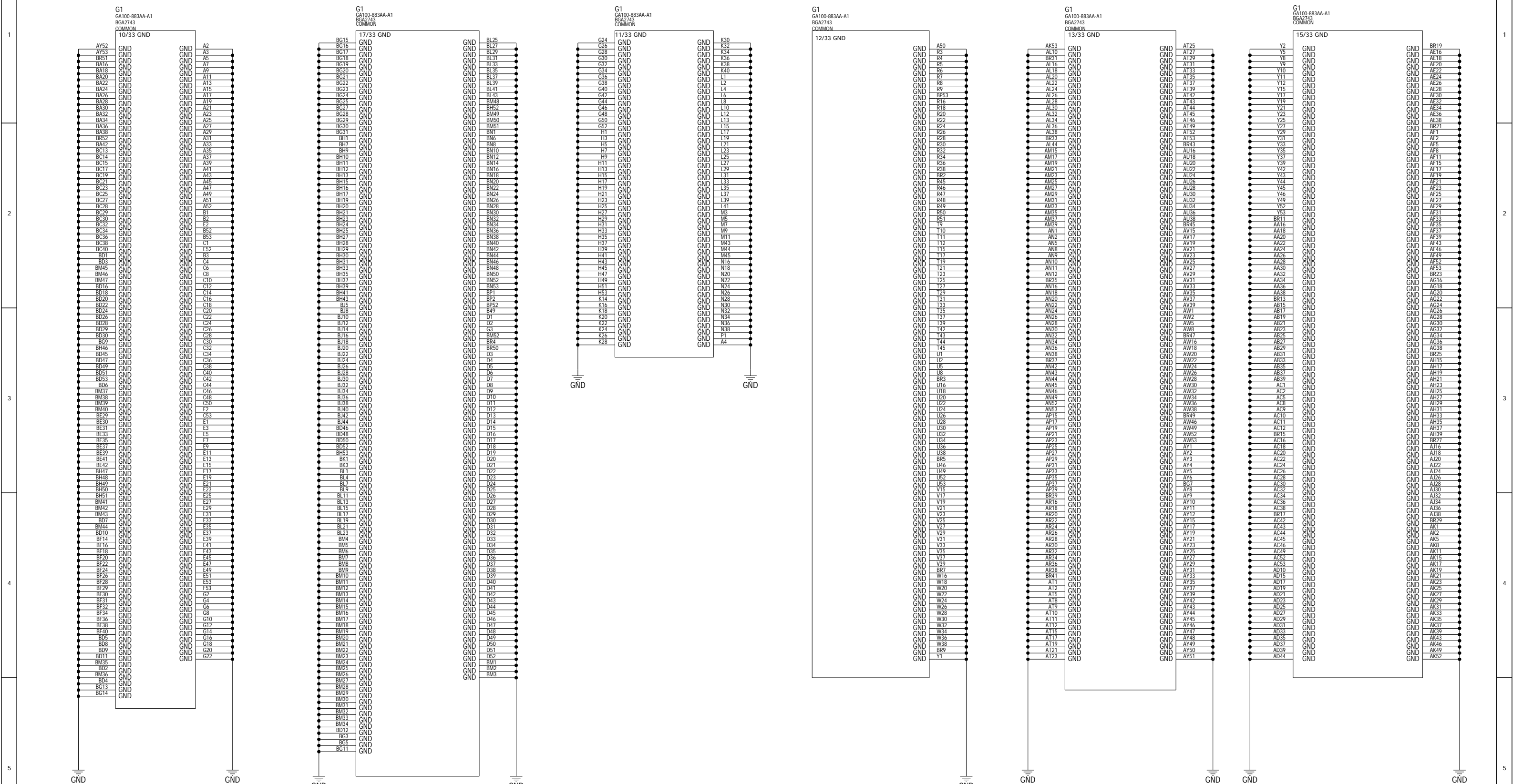
A	B	C	D	E	F	G	H
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GPU NVHS POWER



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GPU GND CONNECTIONS



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ALL IN	600 2100
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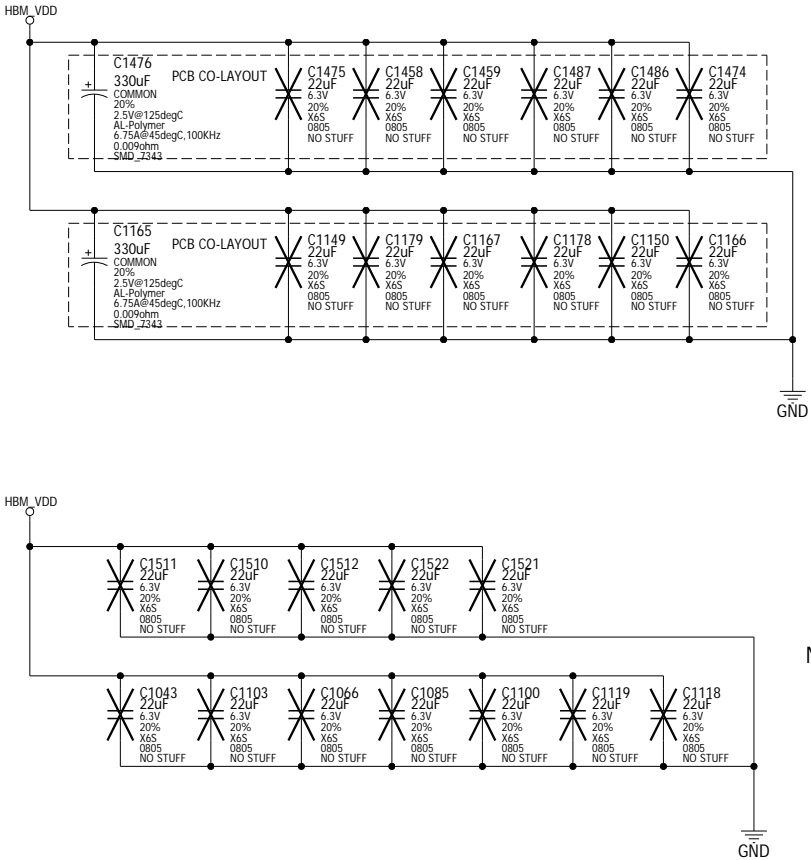
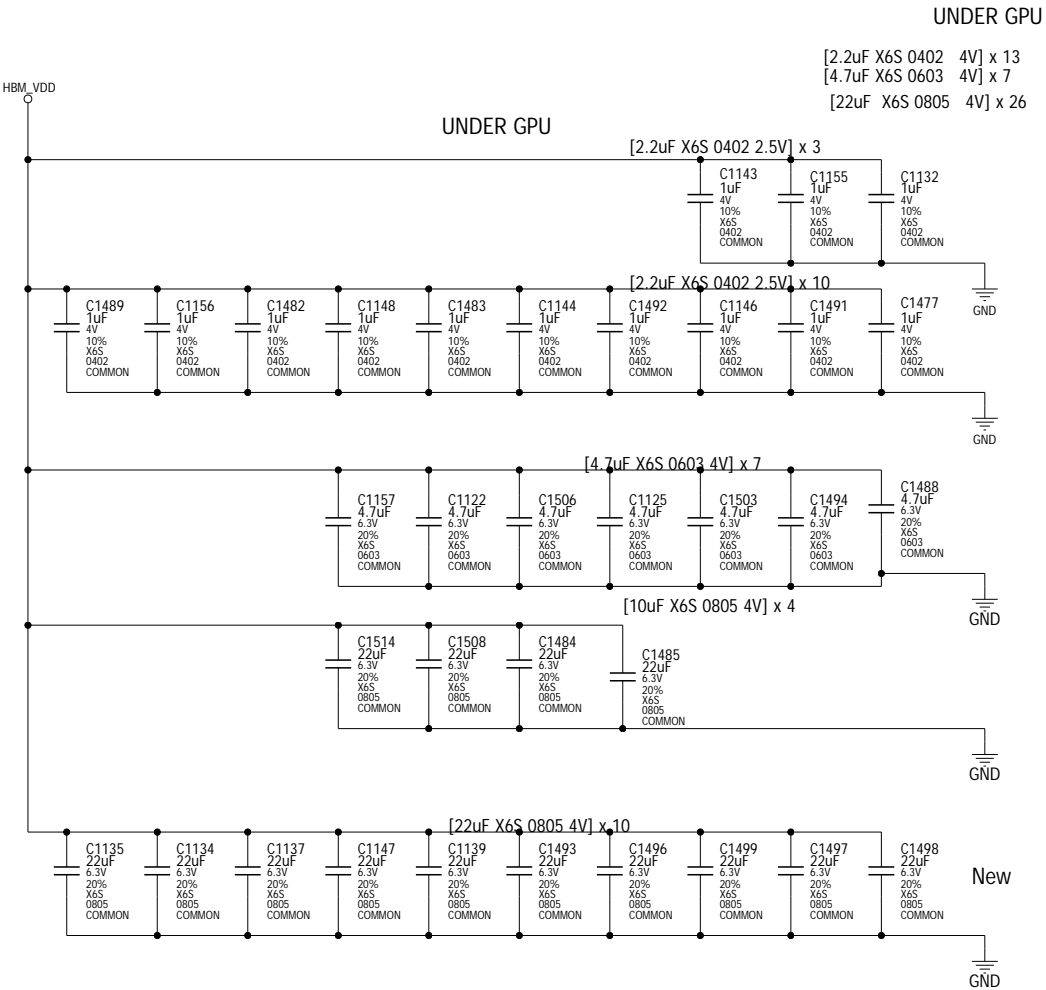
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[illegible]

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HBM DECAP



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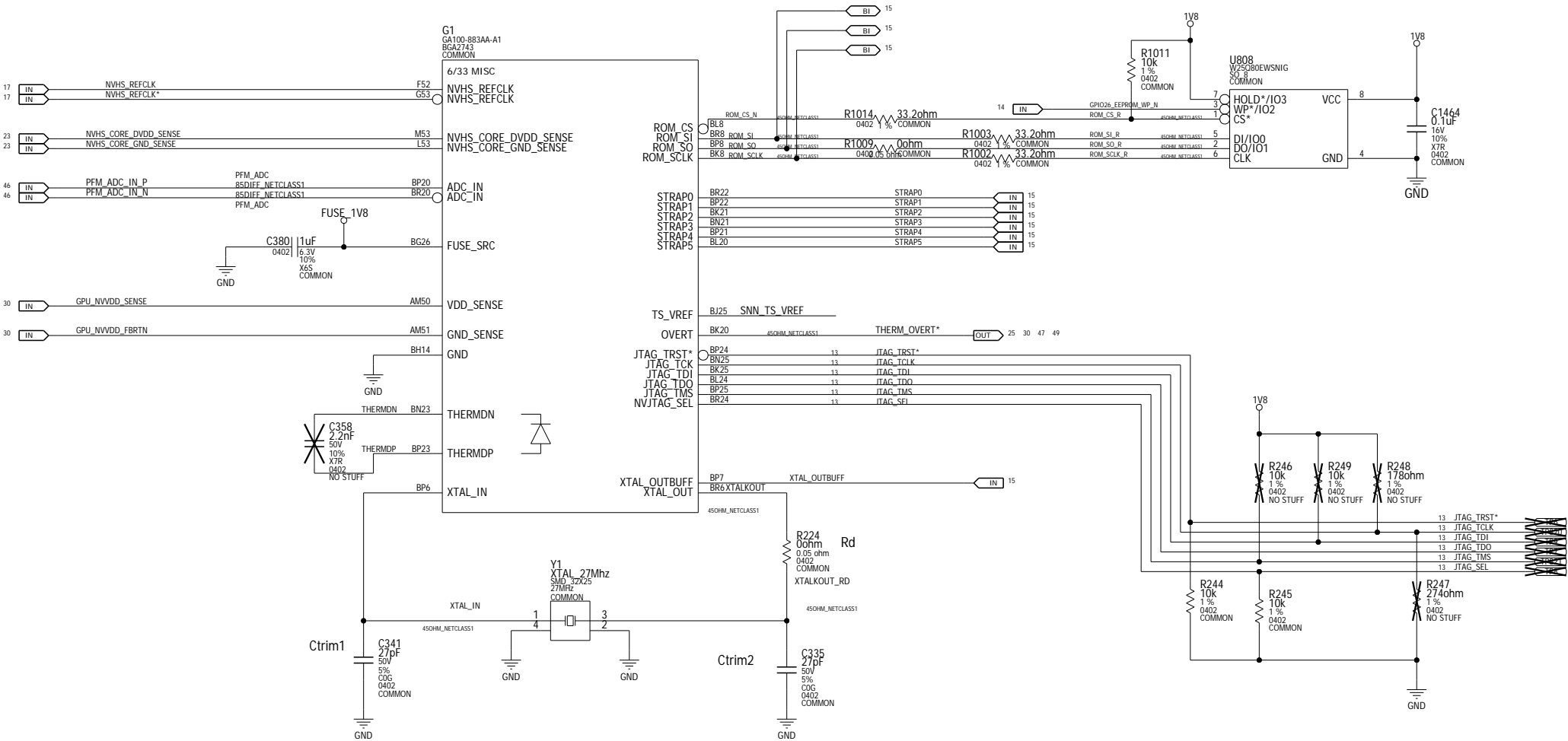
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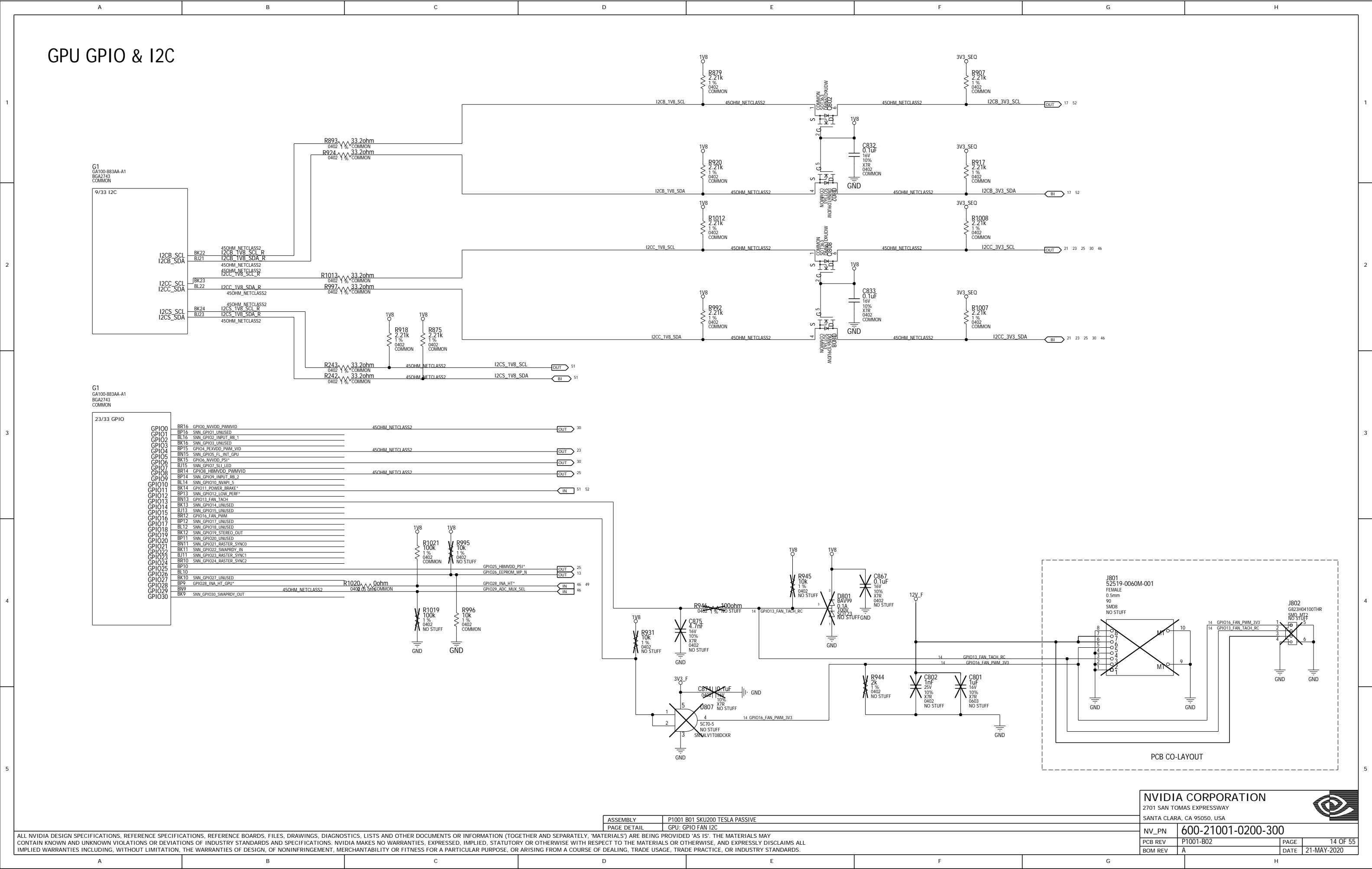
GPU ROM/JTAG



We are in the process of making Crystal's routing DG changes. I suggest to route XTAL In/Out nets with at least x3 spacing (see feedback from Paul Su)

Fom Paul Su:
4W or 5W spacing will have enough margin for 65mm.
If PCB spacing is not enough, 3W spacing should be within 20mm.

GPU GPIO & I2C



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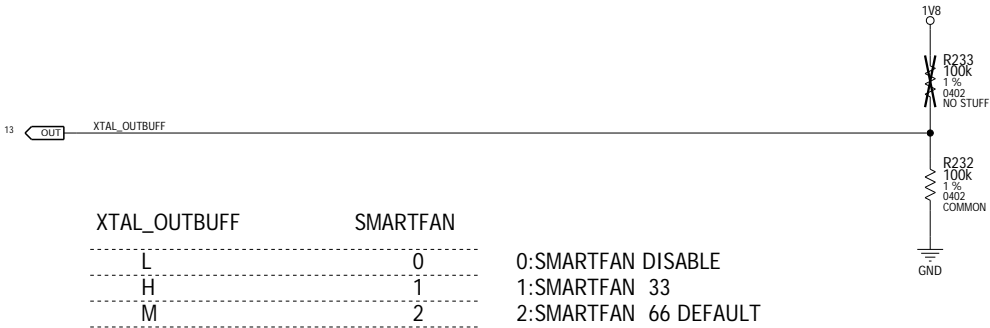
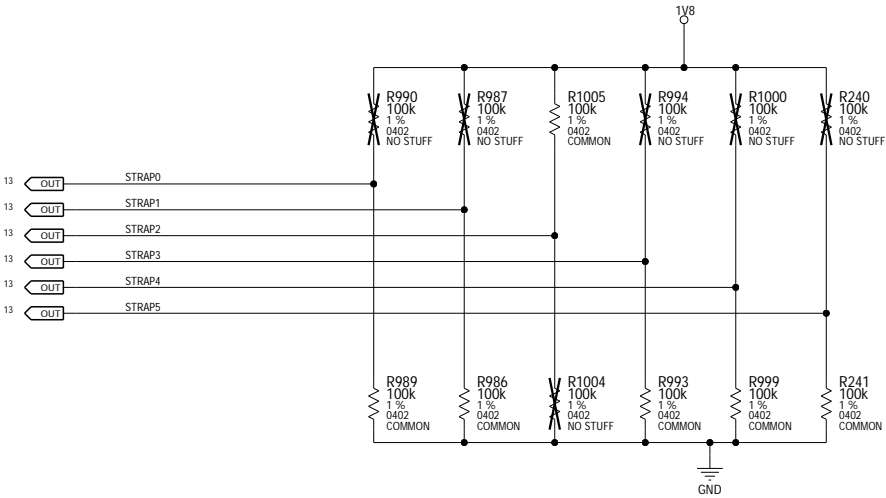
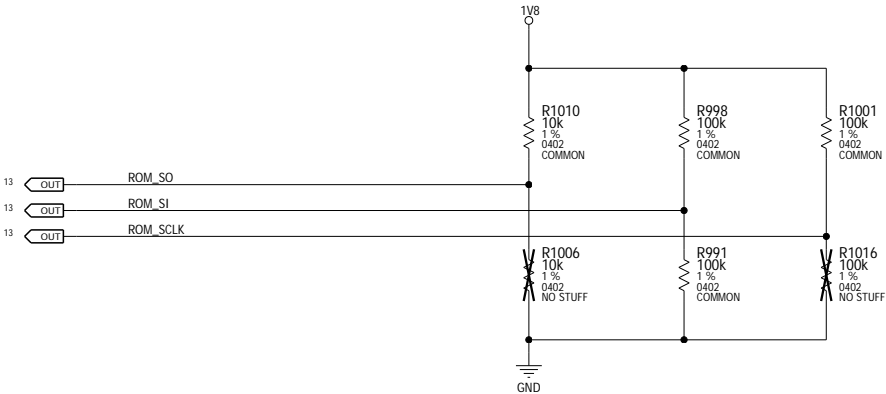
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GPU STRAP CONFIGURATION

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
H	L	L	00100	RAMCFG SAMSUNG HBM2 8Gb 8Hi
H	H	H	00111	RAMCFG HYNIX HBM2E 16Gb 8Hi
L	M	H	01010	RAMCFG MICRON HBM2E 16Gb 8Hi

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
H	M	H	0001	FS_OVERT ENABLE
H	H	M	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0



DEFAULT

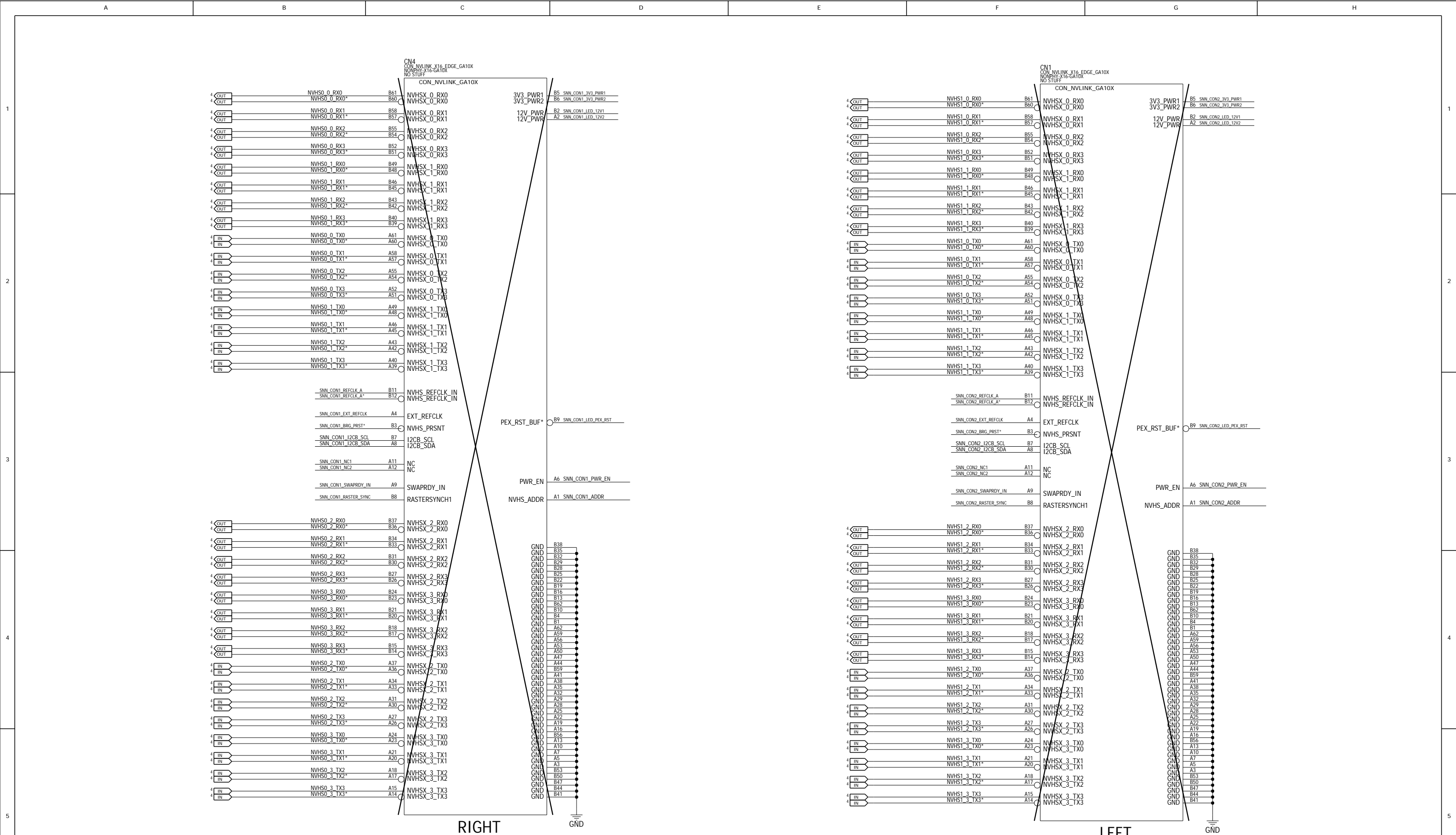
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default



RIGHT

LEFT

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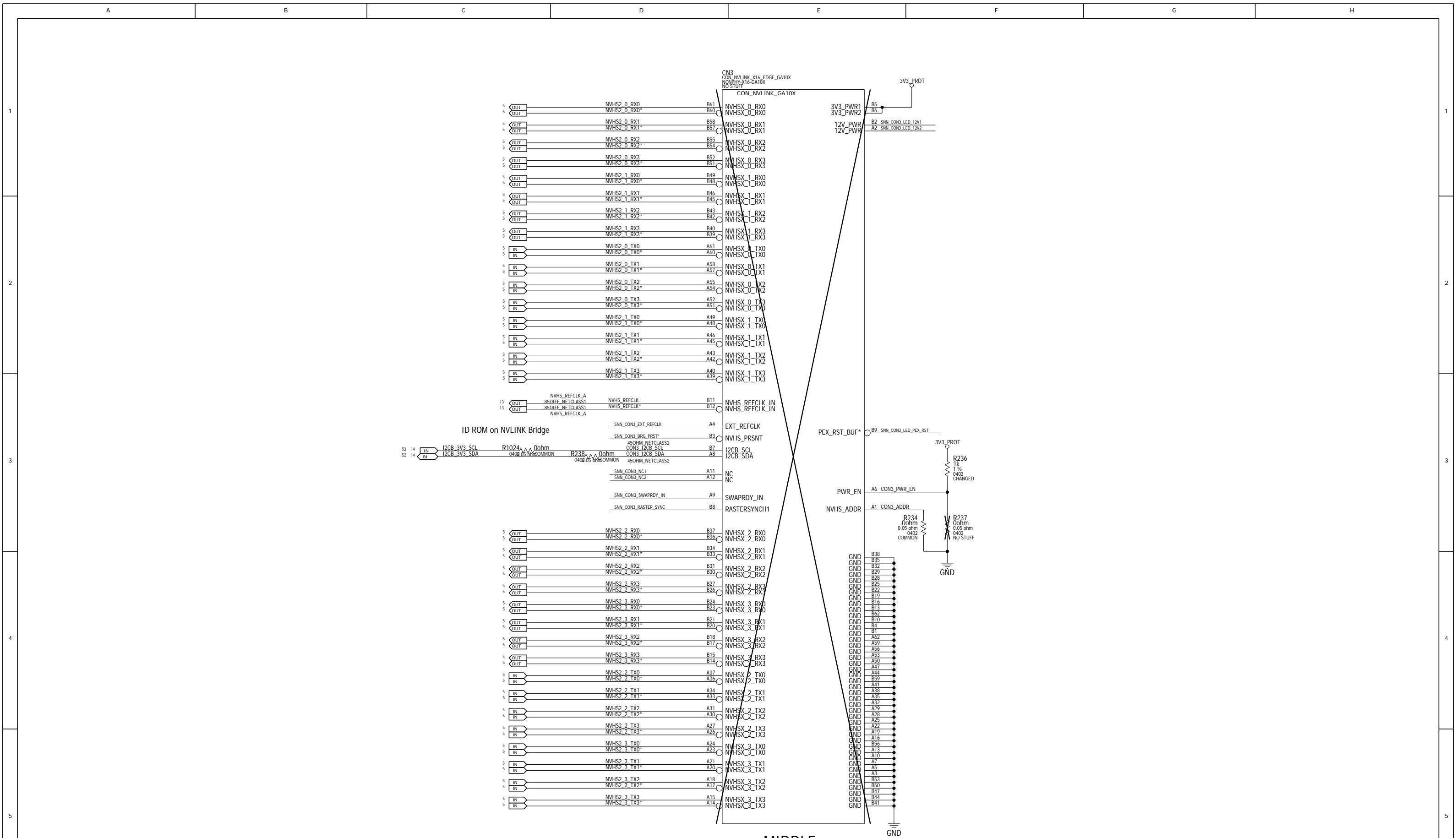
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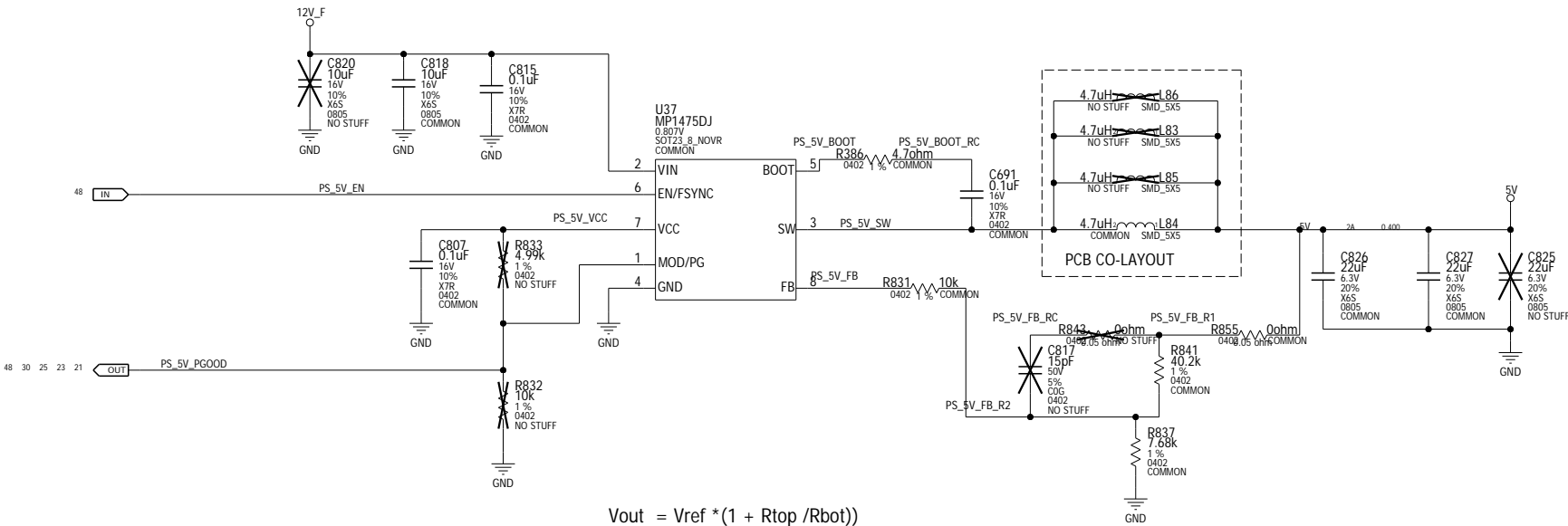
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PAGE DETAIL	IO:NVHS x16.CON1,2



PS: 5V



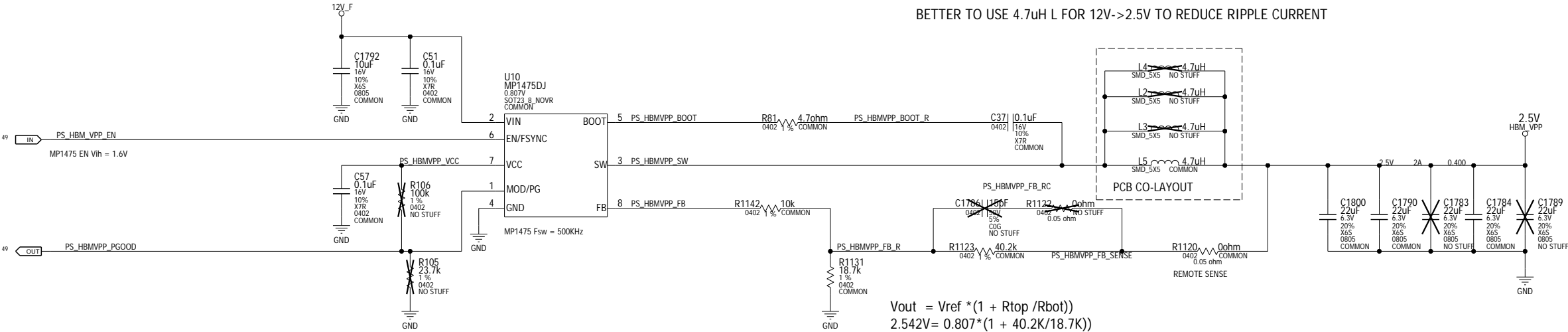
$$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$$
$$5.031V = 0.807 * (1 + 40.2K / 7.68K)$$

RIPPLE CURRENT=1.24A FOR 12V->5V 500KHz 4.7uH

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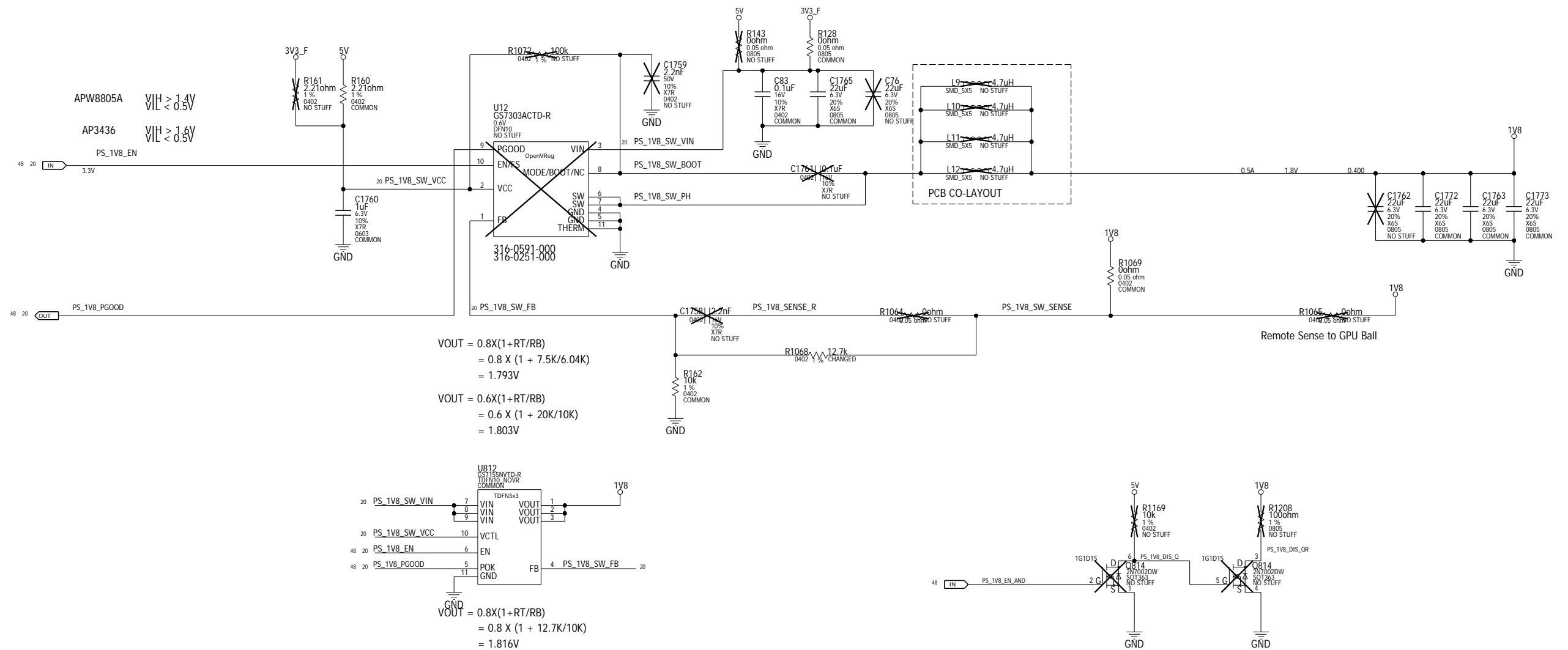
PS: HBM_VPP

HBMVPP = 2.5V



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PS 1V8



ASSEMBLY	P1001 B01 SKU200 TESLA PASSIVE
PAGE DETAIL	PS: 1V8

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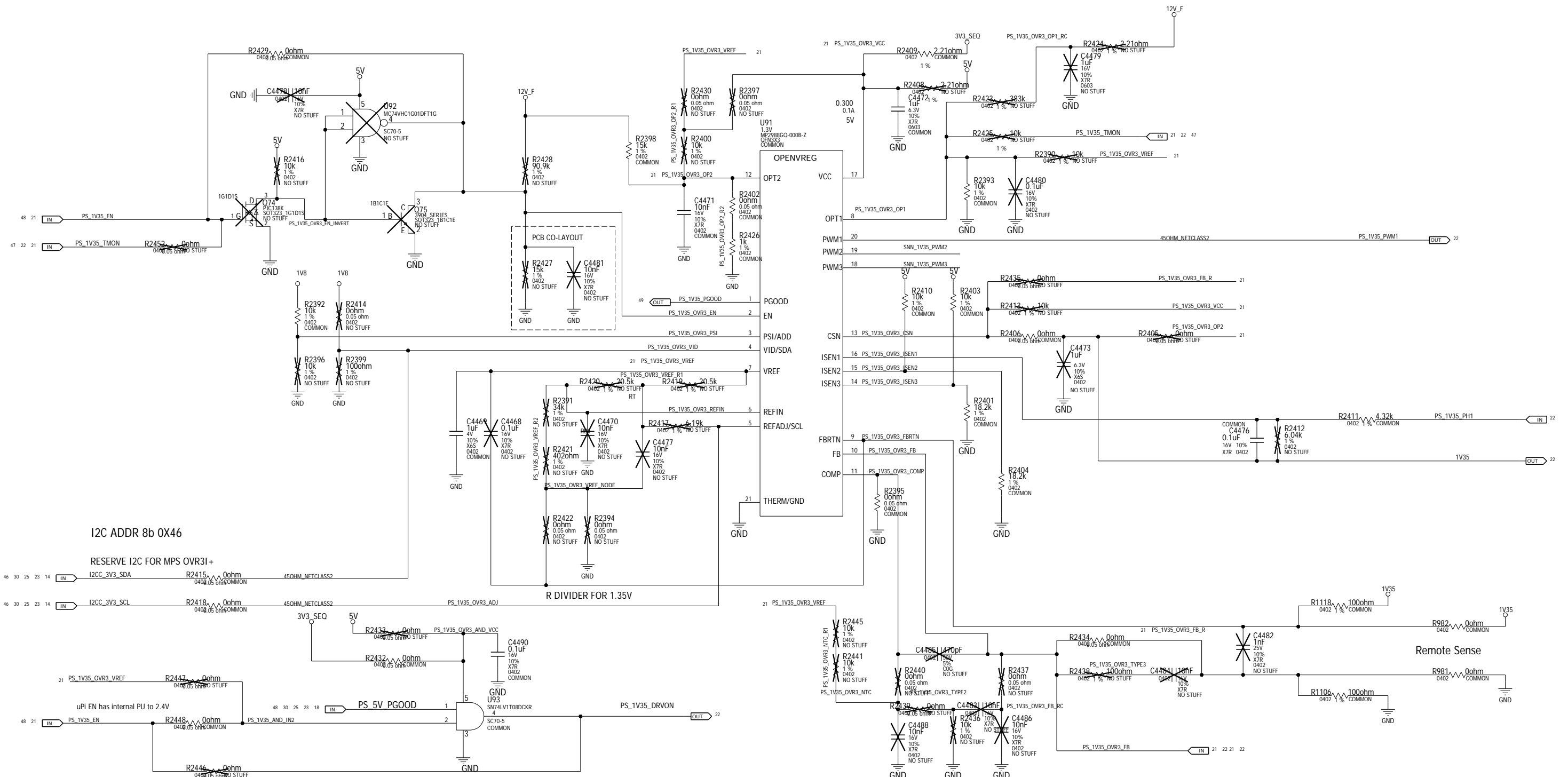
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PS IOVDD 1V35 Controller



ASSEMBLY	P1001 B01 SKU200 TESLA PASSIVE
PAGE DETAIL	PS: IOVDD 1V35 Controller

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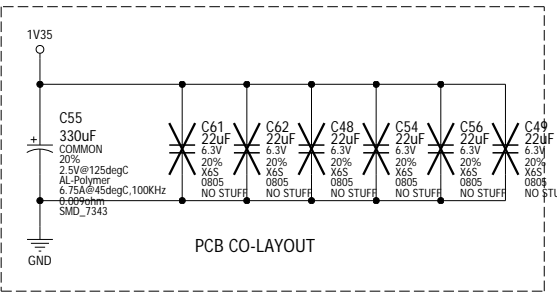
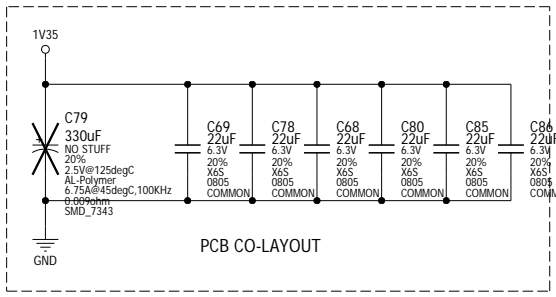
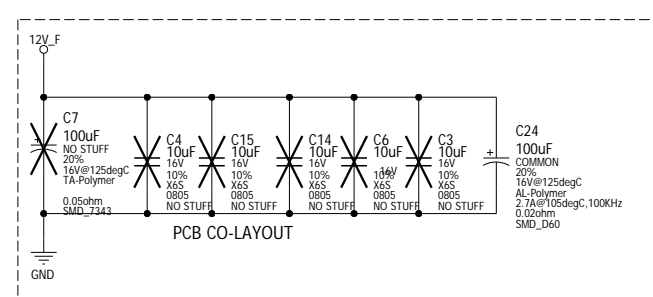
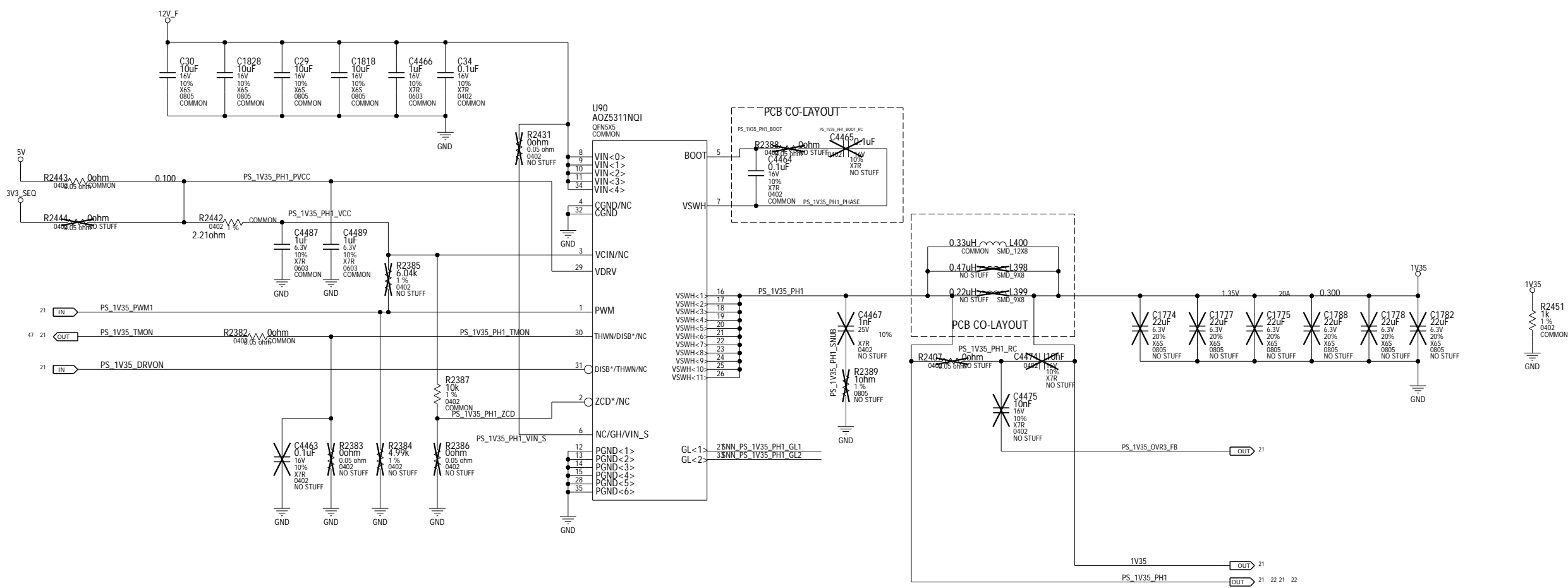
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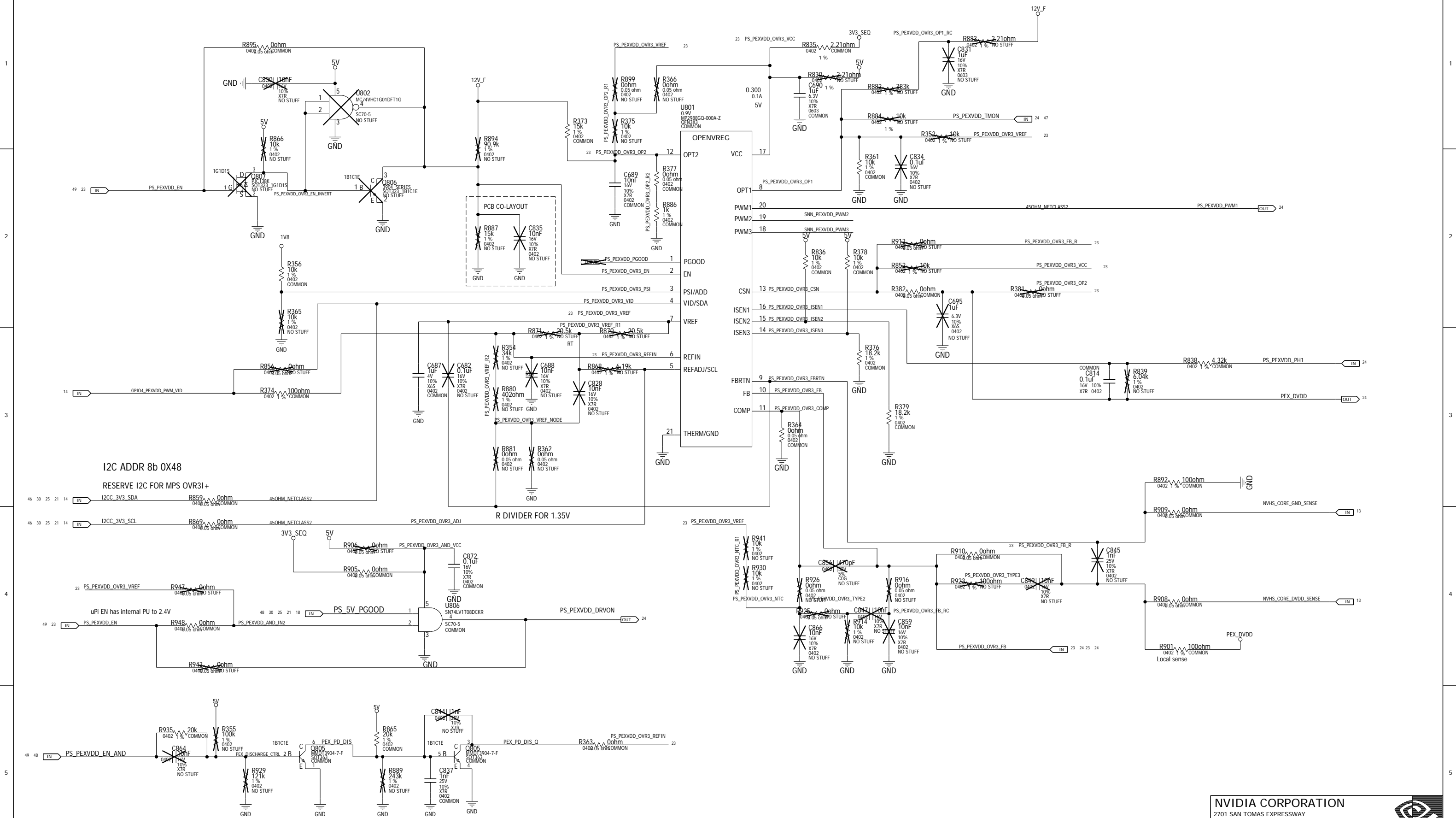


PS IOVDD 1V35 PHASE 1



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PS PEXVDD CONTROLLER



ASSEMBLY	P1001 B01 SKU200 TESLA PASSIVE
PAGE DETAIL	PS: PEXVDD Controller

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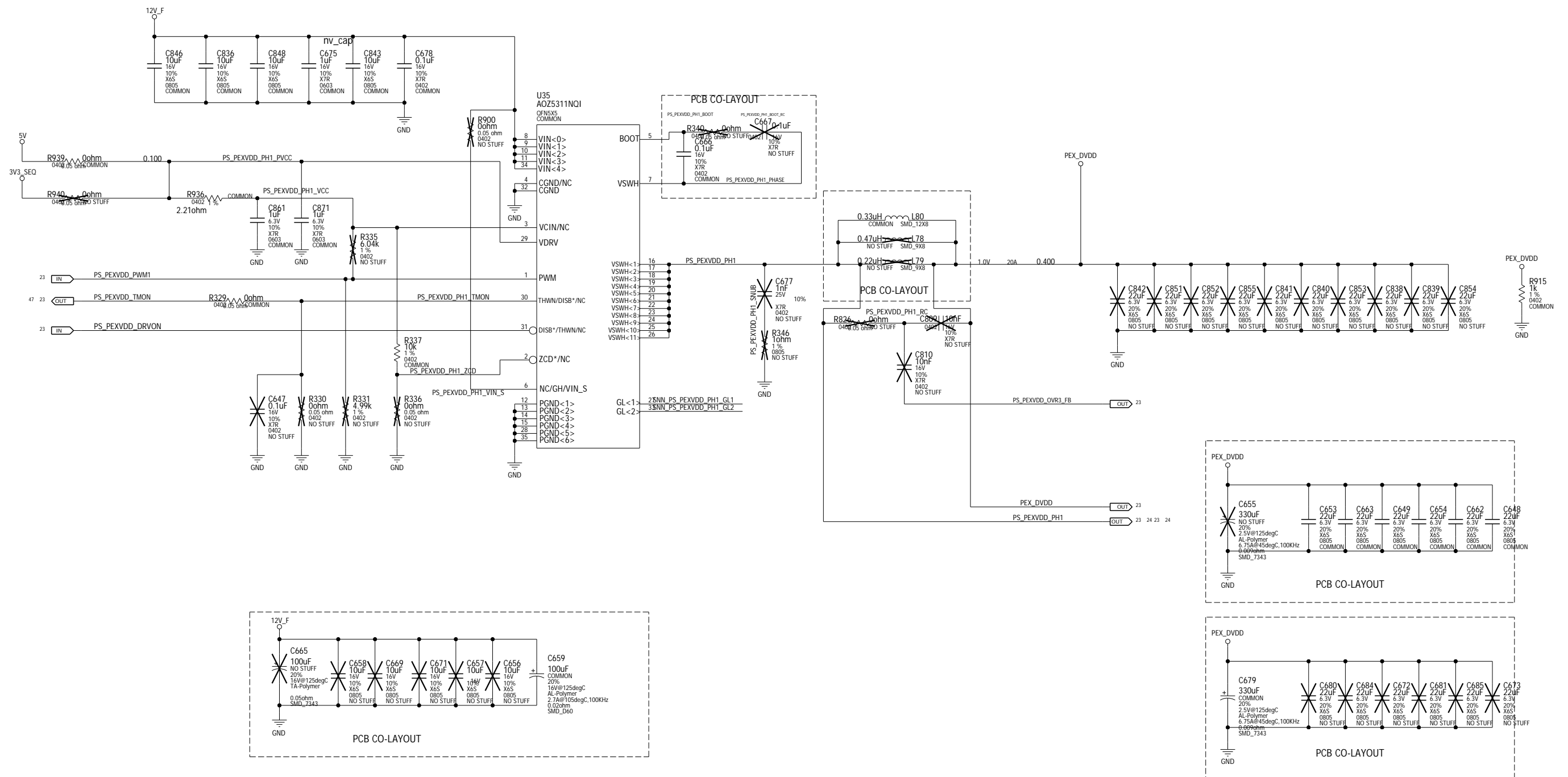
PCB REV	P1001-B02
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PS PEXVDD PHASE 1



ASSEMBLY	P1001 B01 SKU200 TESLA PASSIVE
PAGE DETAIL	PS: PEXVDD Phase1

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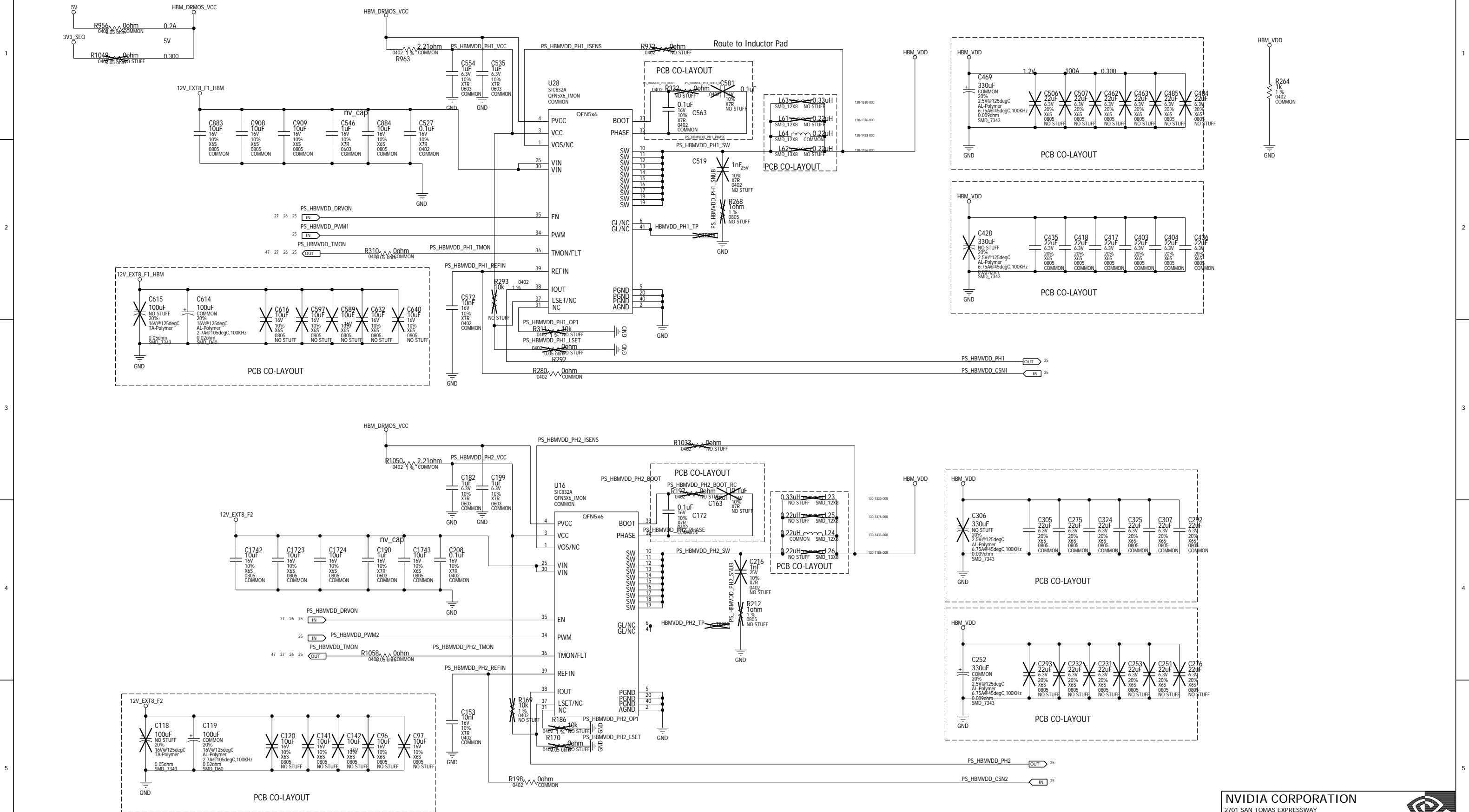
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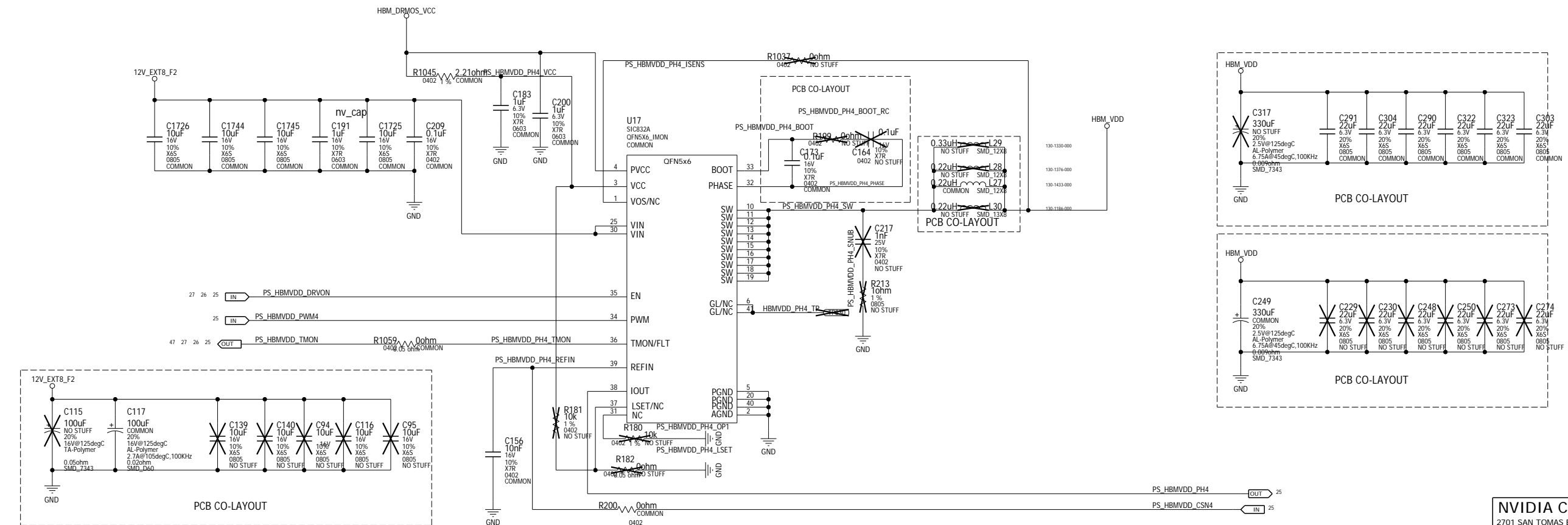
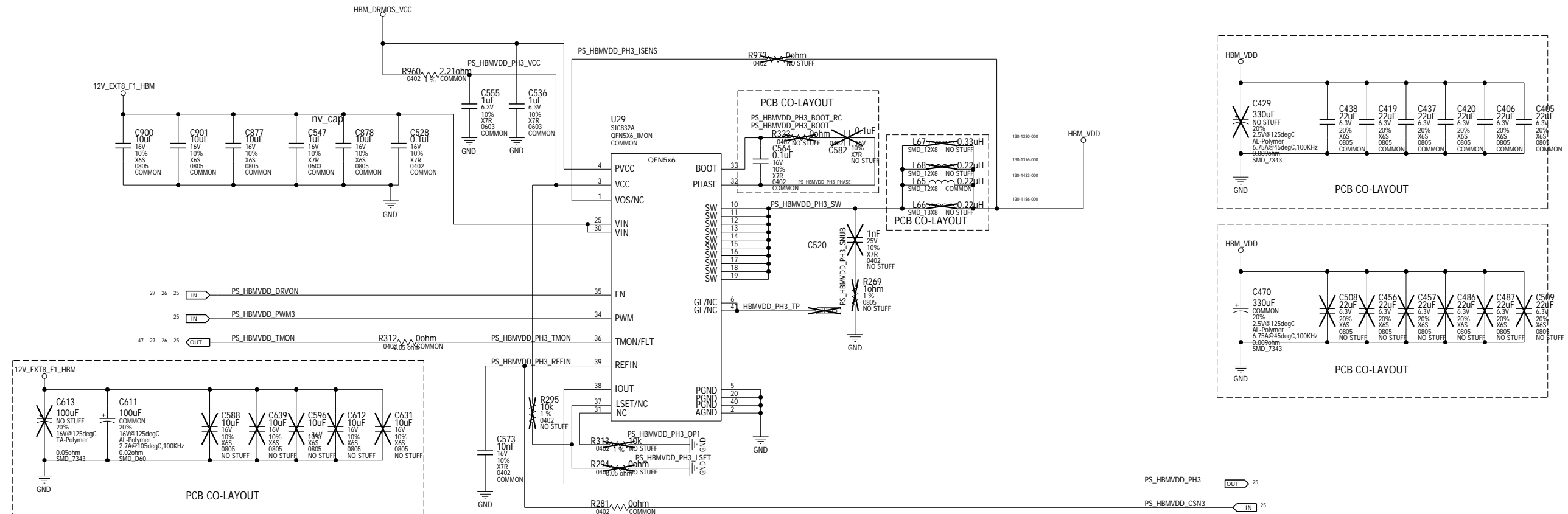
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PS HBMVDD PH1 PH2



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PS HBM_VDD PH3, PH4



ASSEMBLY	P1001 B01 SKU200 TESLA PASSIVE
PAGE DETAIL	PS: HBMVDD PH3 AND PH4

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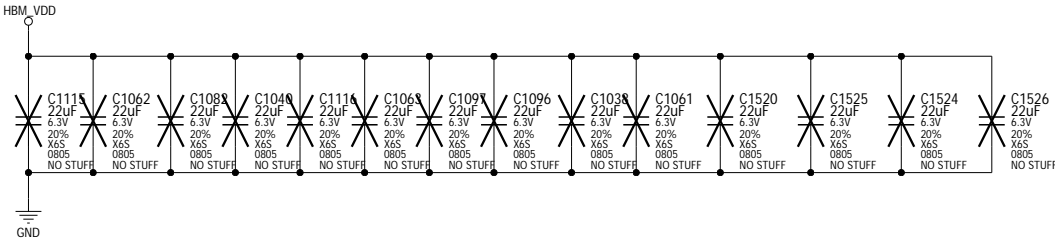
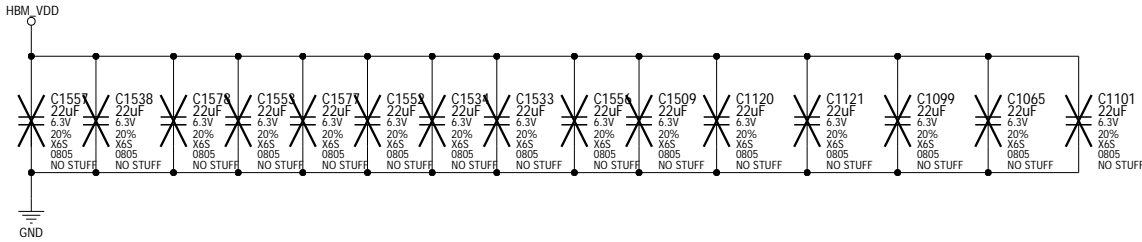
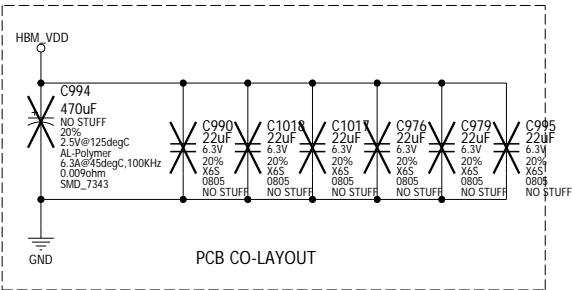
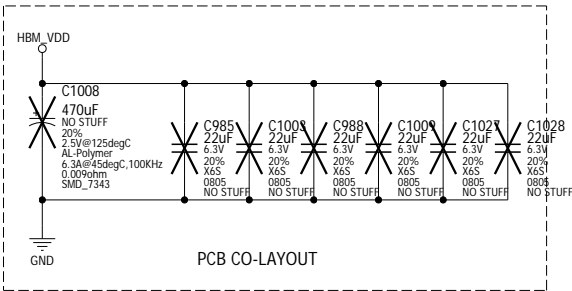
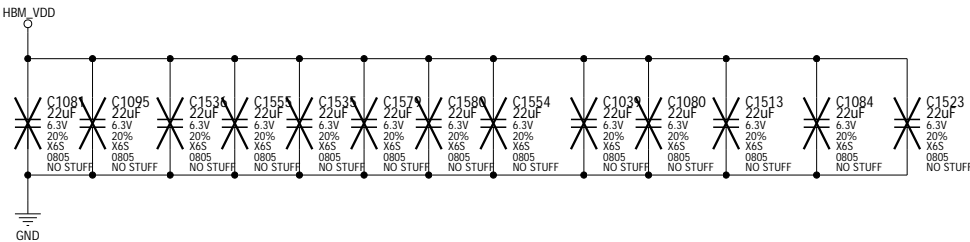
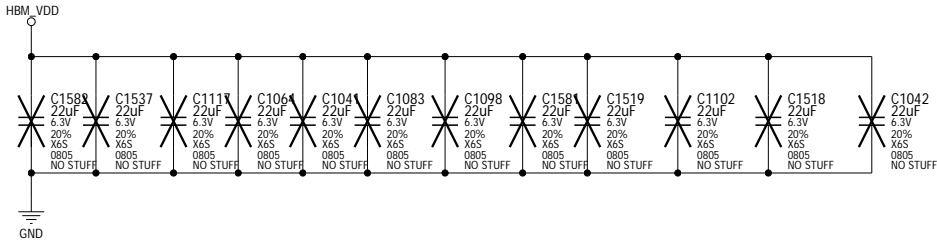
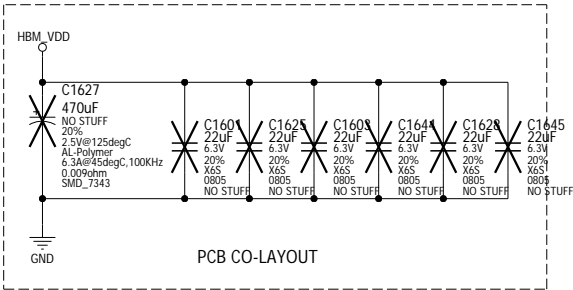
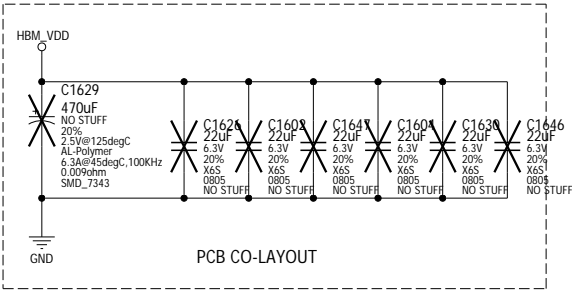
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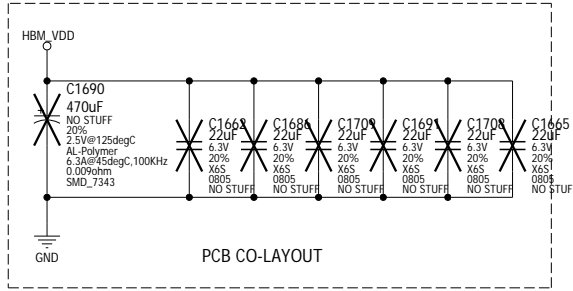
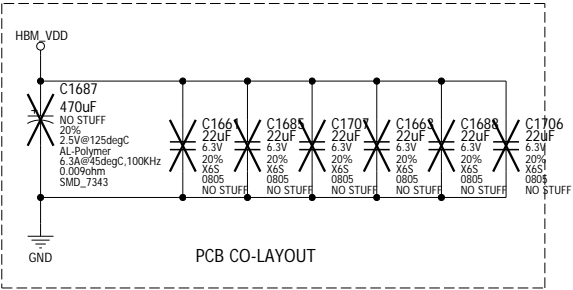
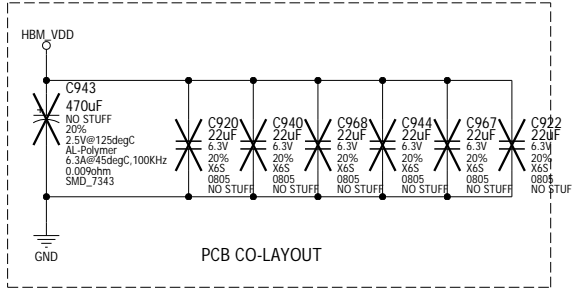
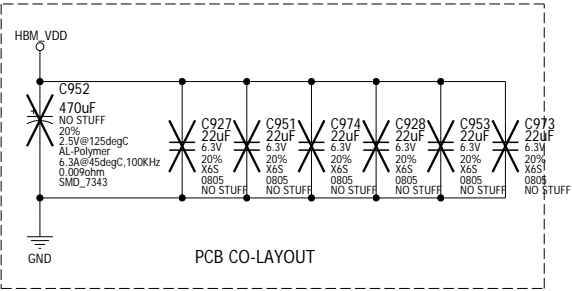
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PS HBMVDD OUTPUT MLCC 1



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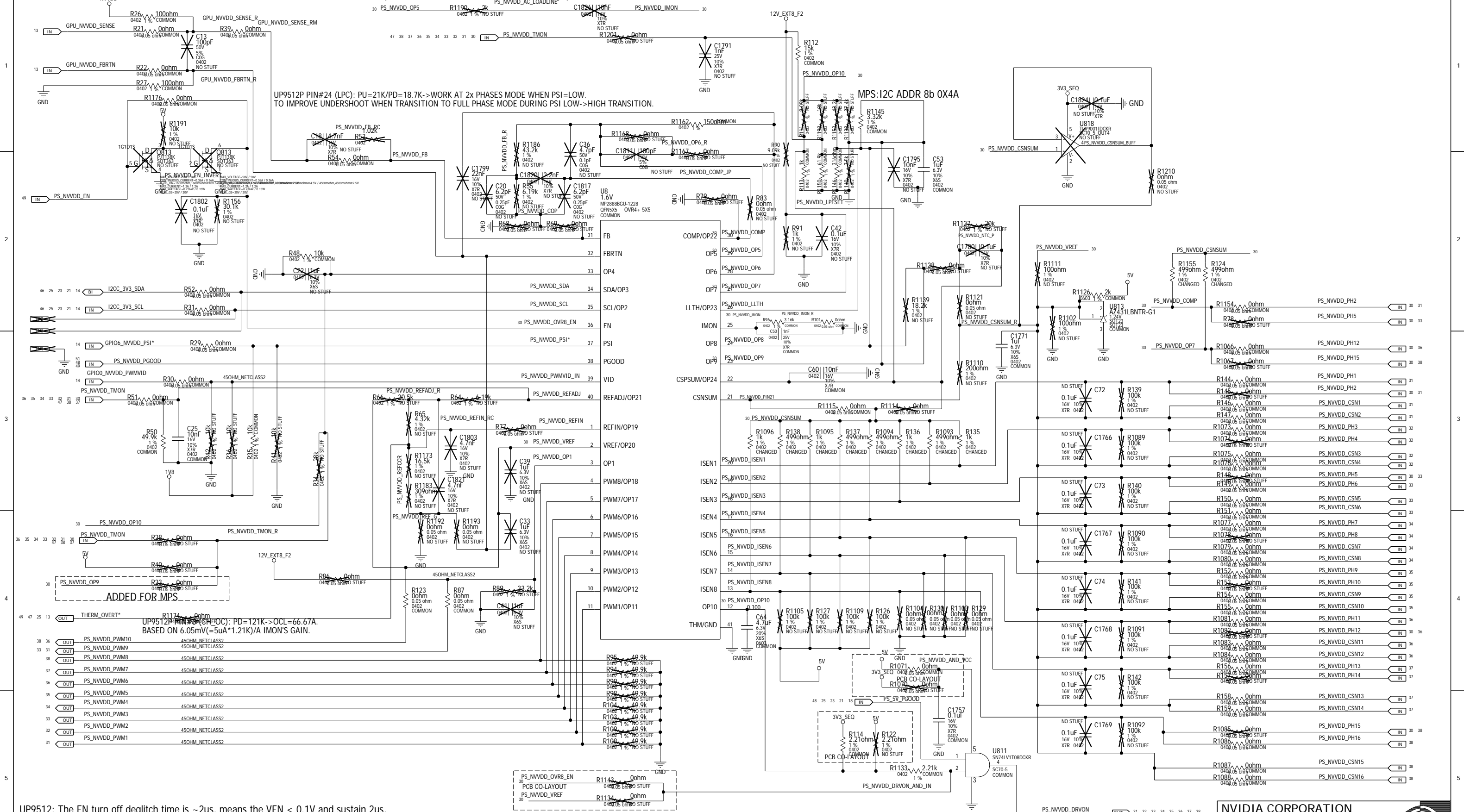
PS HBMVDD OUTPUT MLCC 2



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PS: NVVDD Controller_OVR4I

Reserve a RC BOM option for Onsemi controller to add AC loadline tuning option, if need tune Overshoot max



UP9512P: The EN turn off deglitch time is ~2us, means the VEN < 0.1V and sustain 2us, the controller will shut down (turn off both PWM outputs and internal logic circuit).

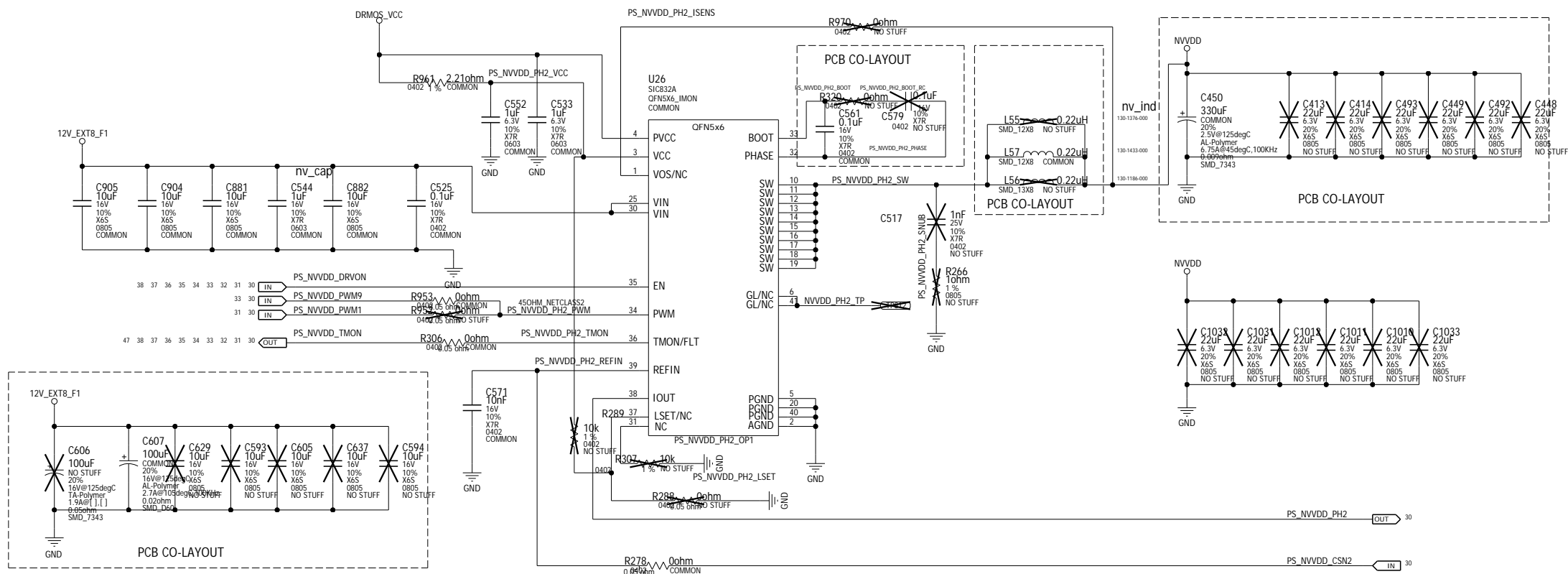
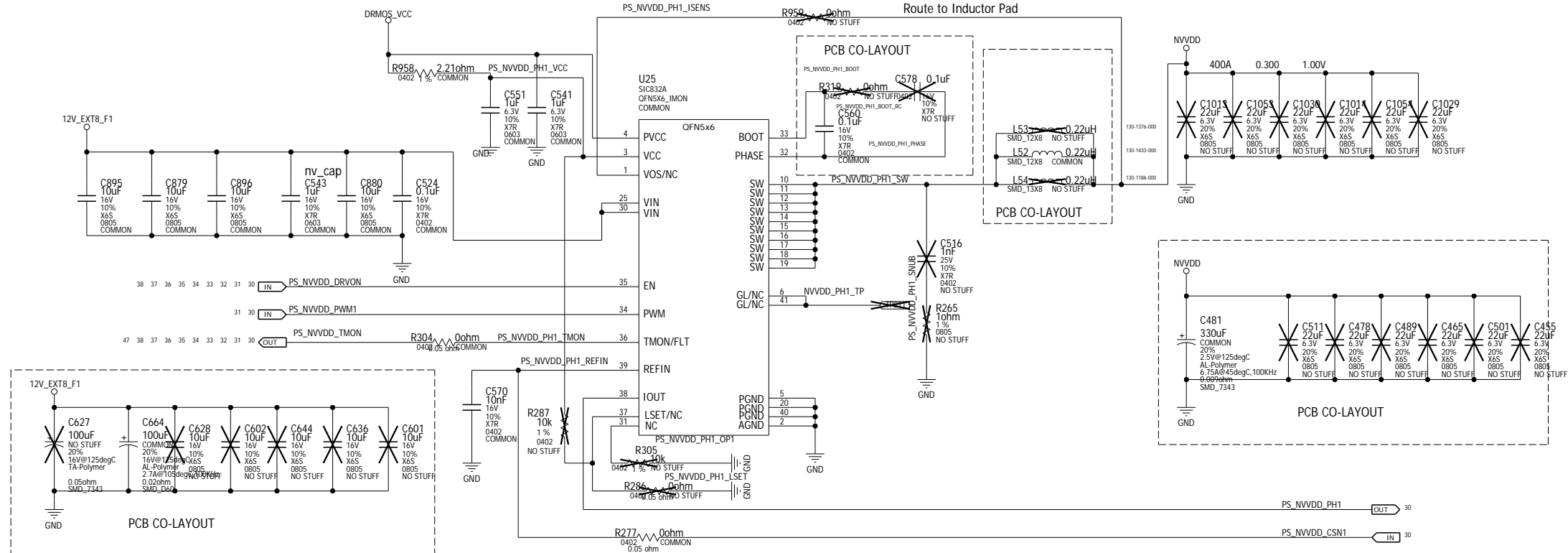
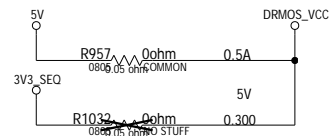
UP9512P: The maximum initialization time (Tinit) after EN toggling HIGH is 550us (max).

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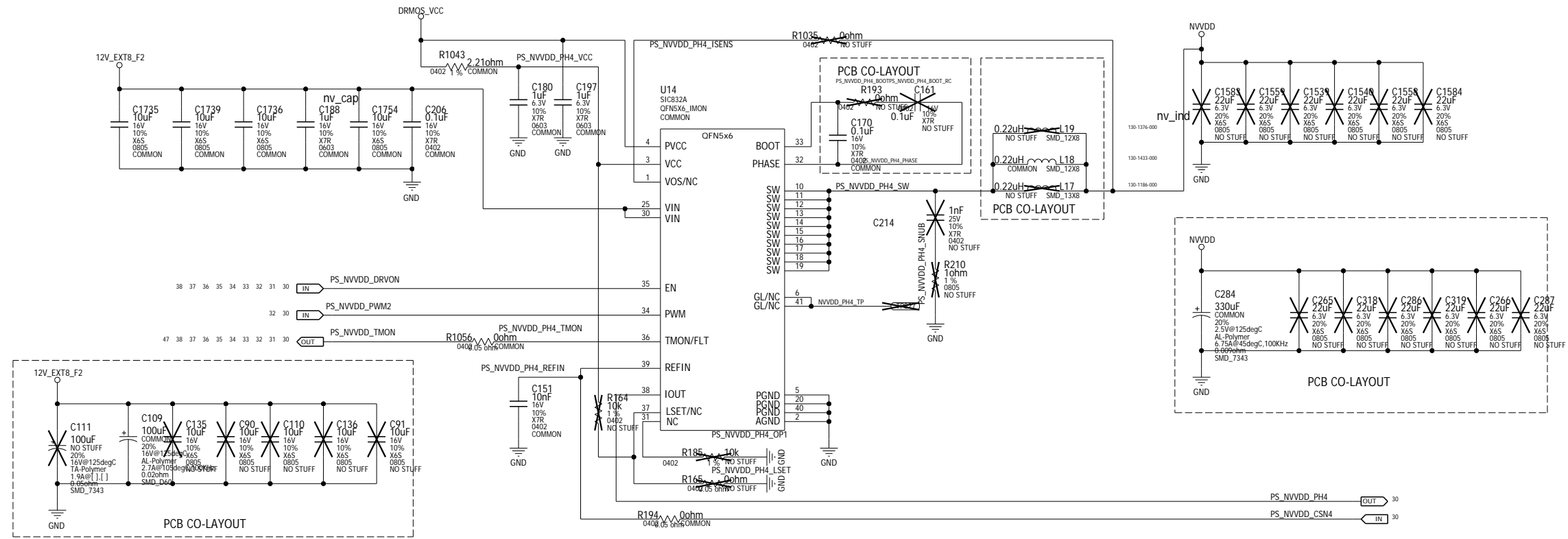
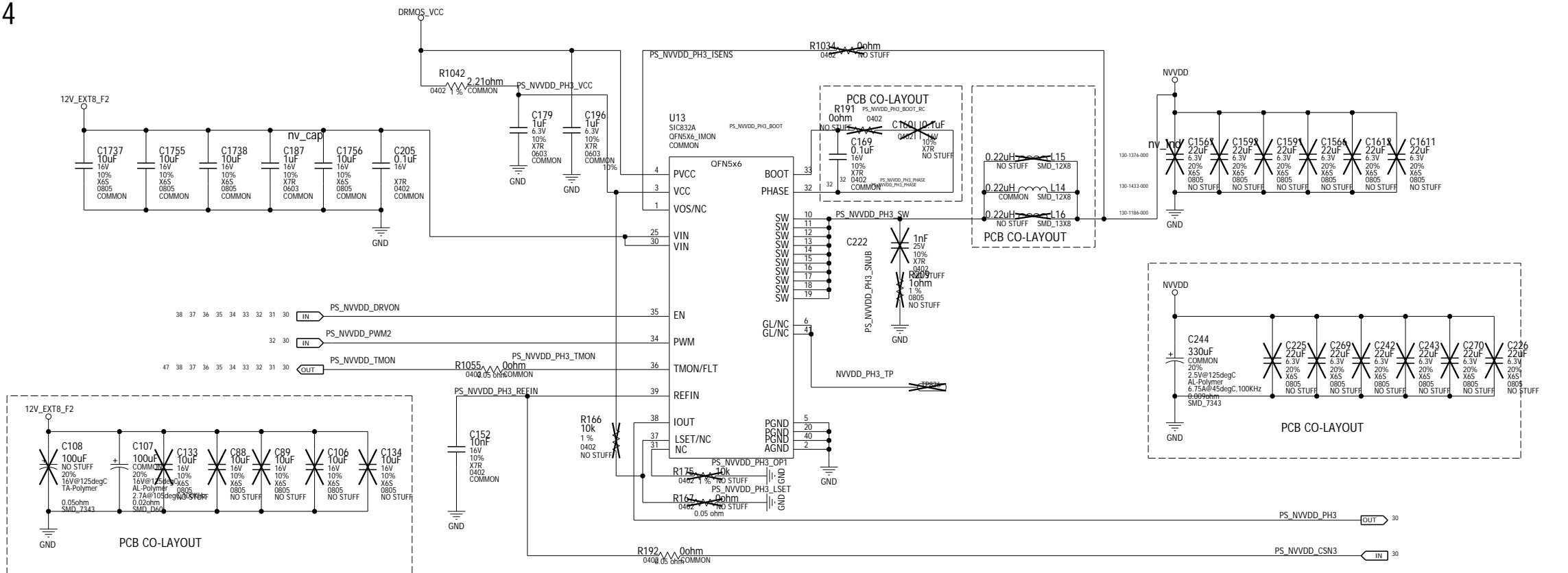
ASSEMBLY	P1001 B01 SKU200 TESLA PASSIVE
PAGE DETAIL	PS: NVVDD Controller_OVR4I

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PS NVVDD PH1 AND PH2



PS NVVDD PH3, PH4



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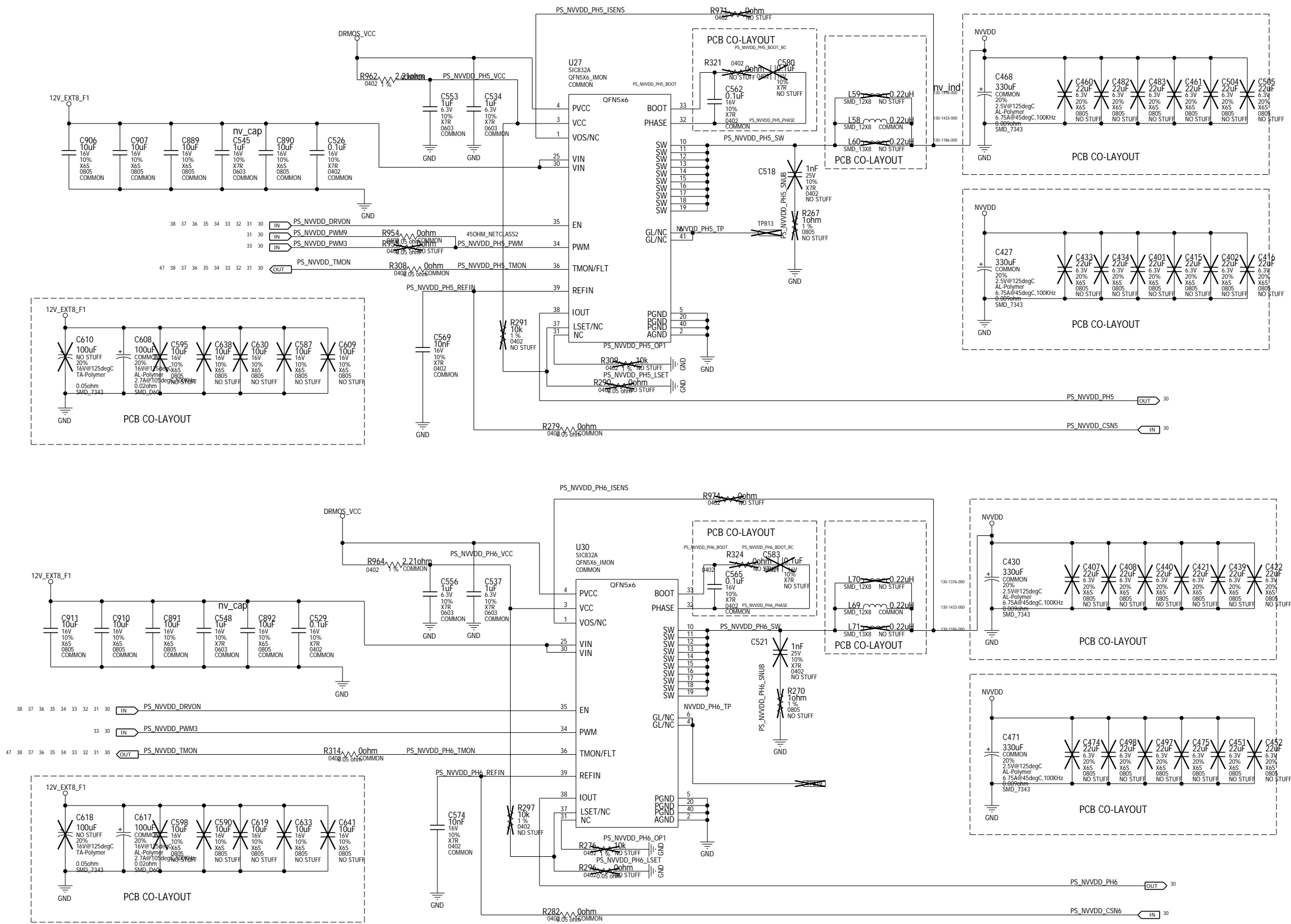


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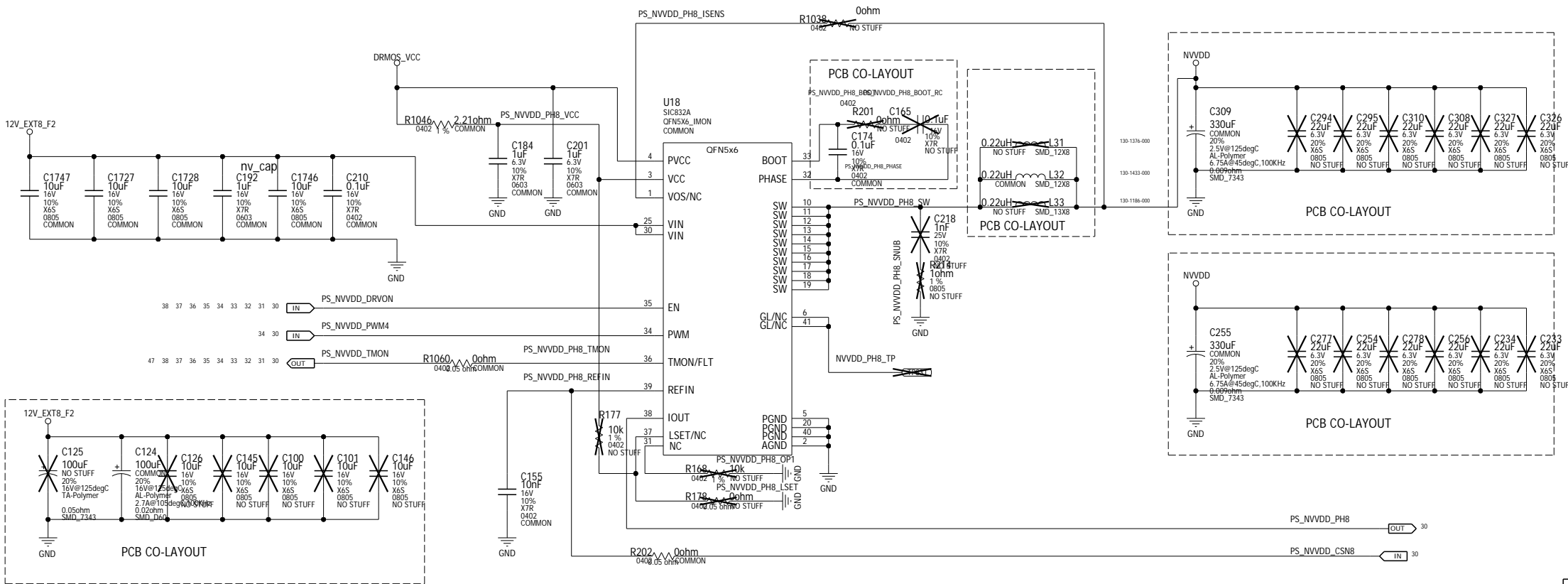
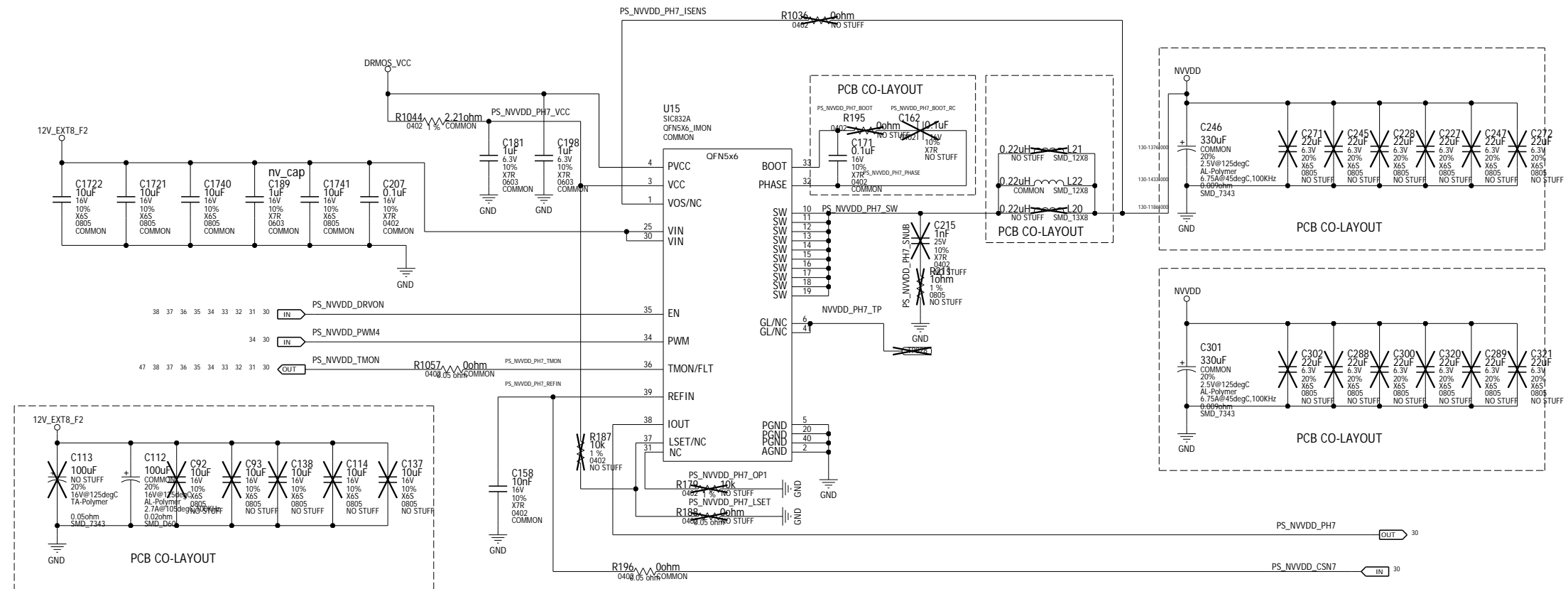
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PS NVVDD Phase 5,6



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PS NVVDD Phase 7,8



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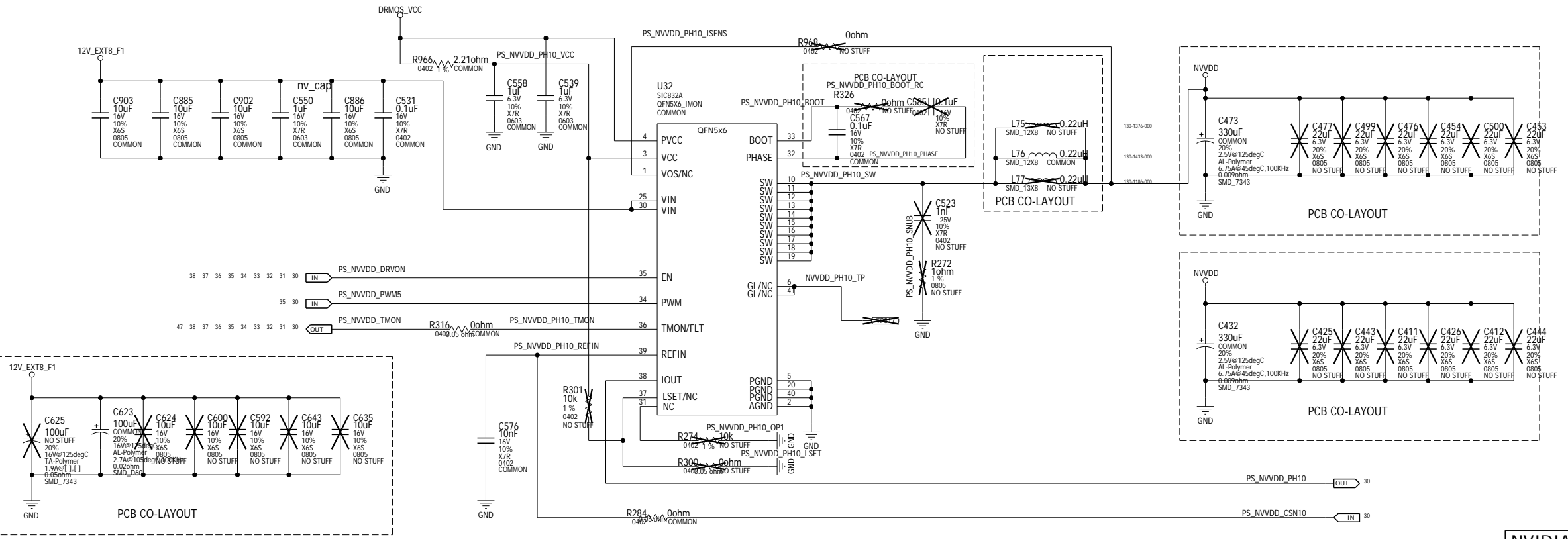
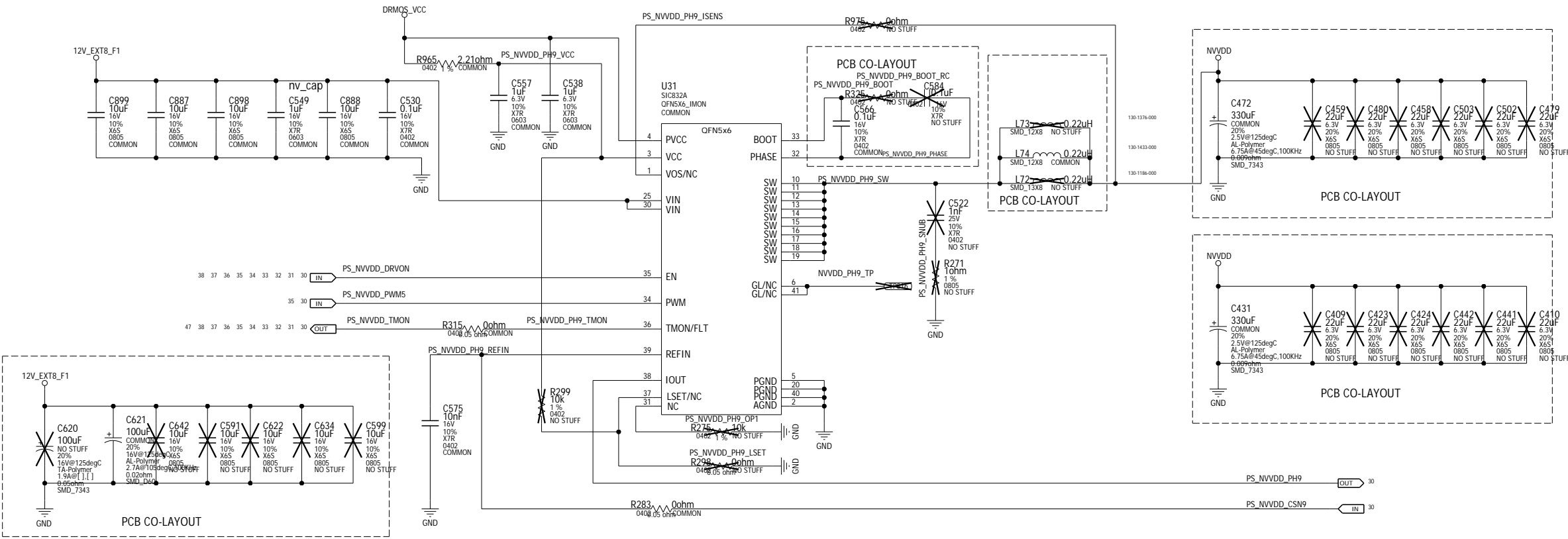
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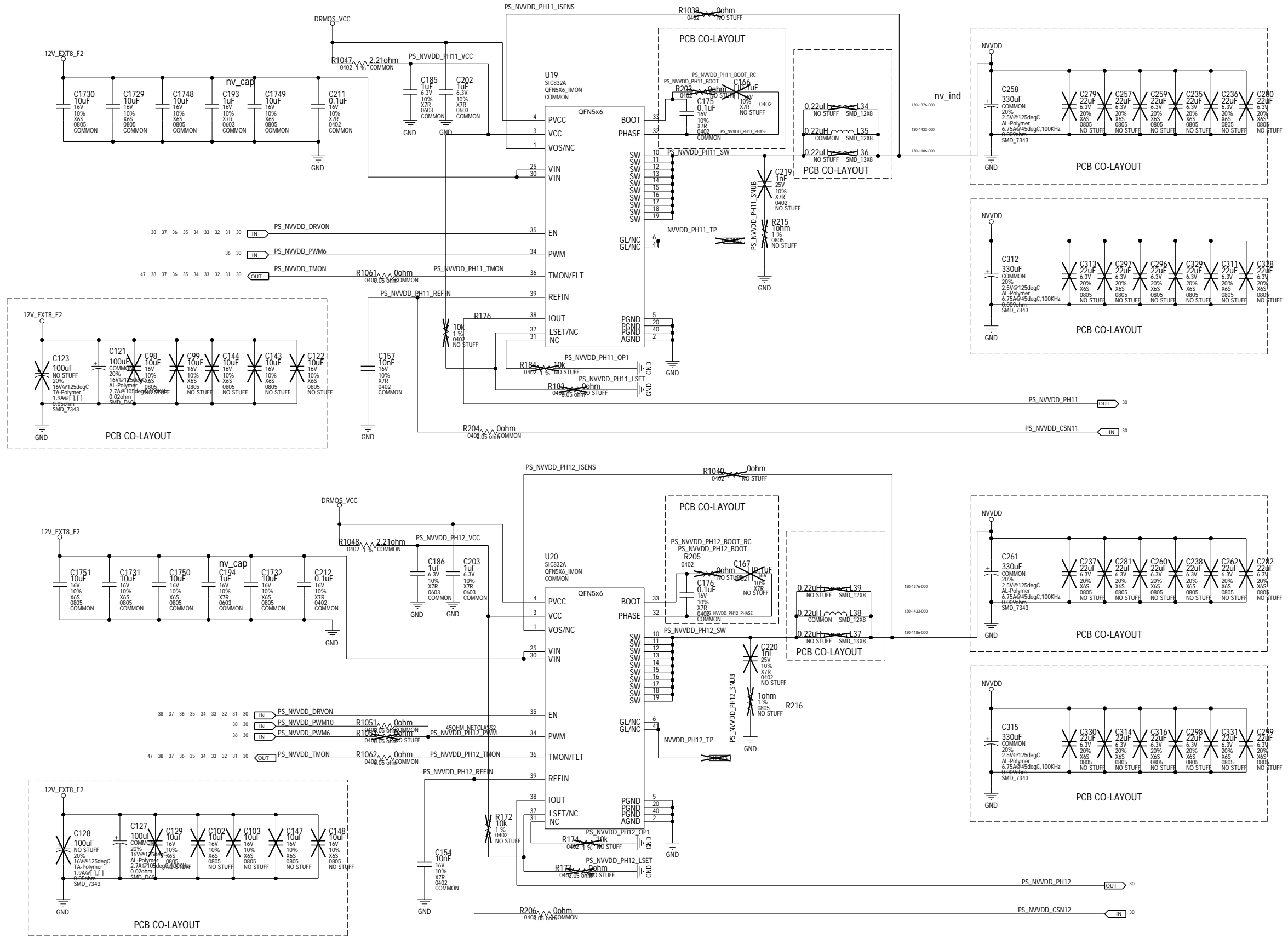


PS NVVDD PH 9,10



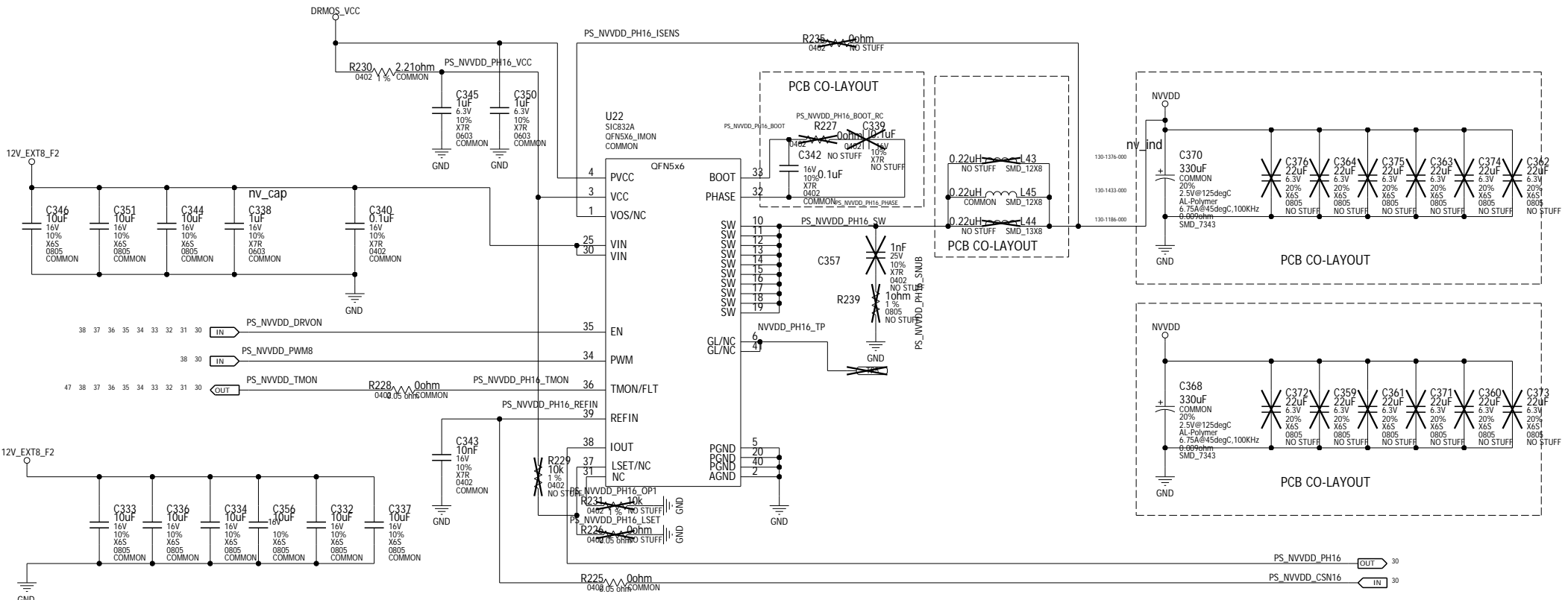
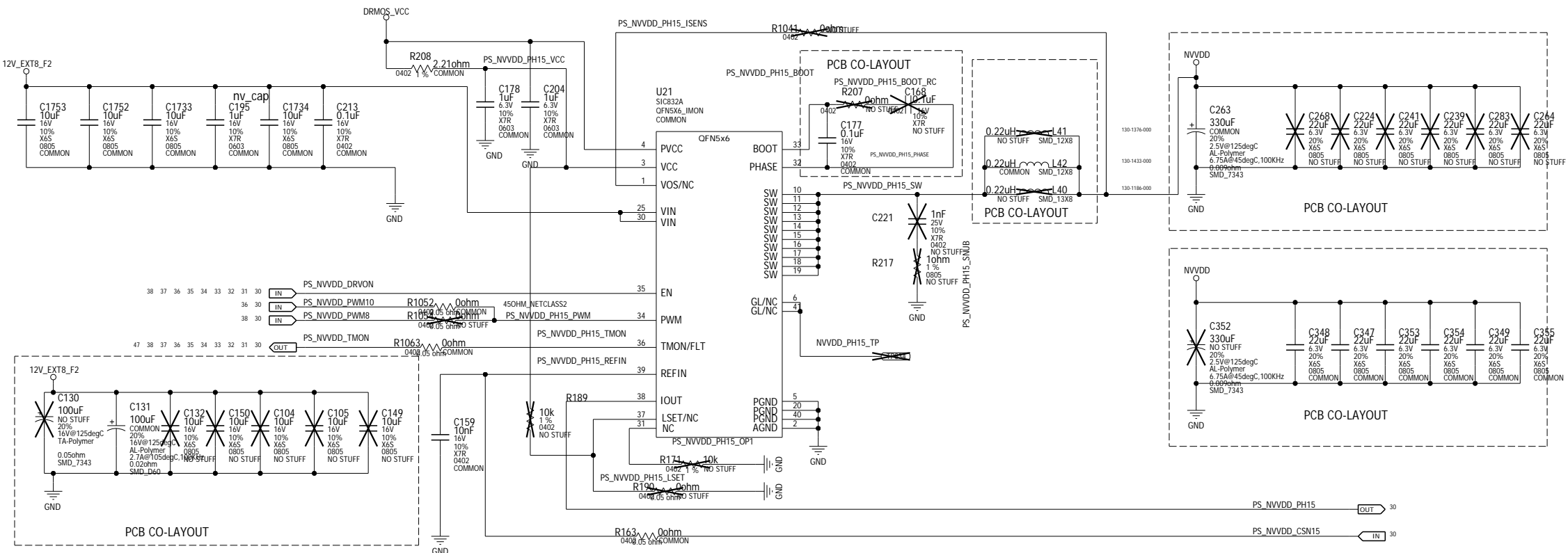
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PS NVVDD PH 11,12



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PS NVVDD PH 15,16



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PCB REV

P1001-B02

BOM REV

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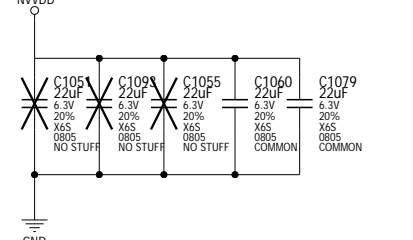
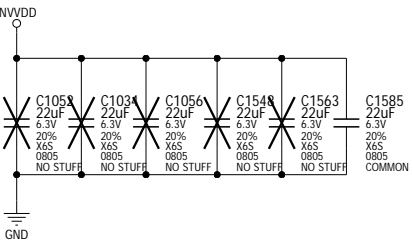
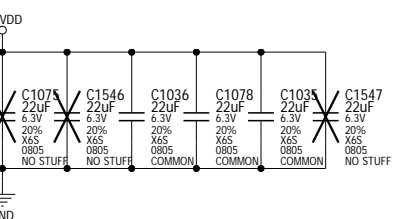
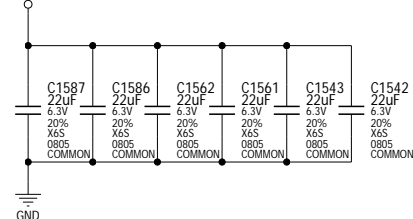
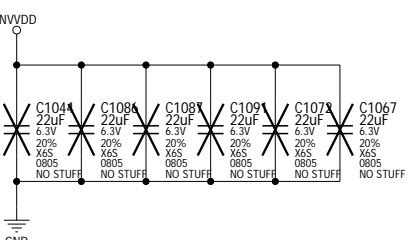
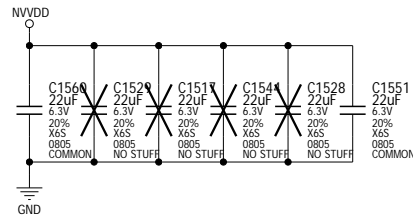
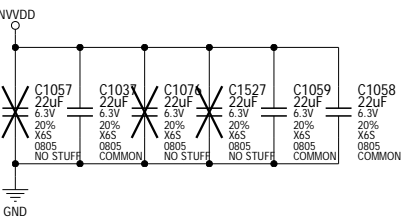
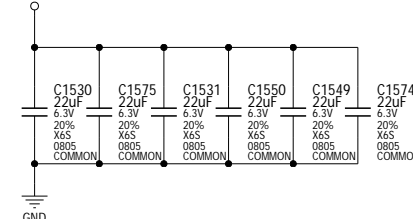
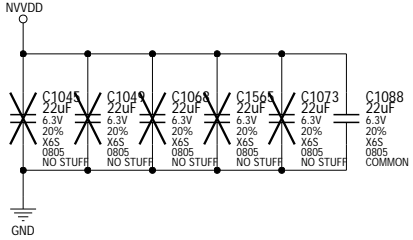
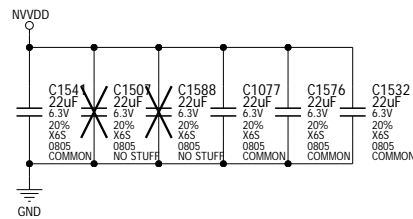
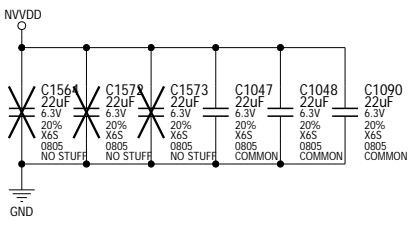
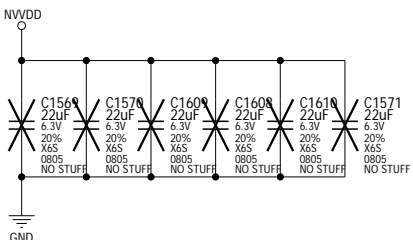
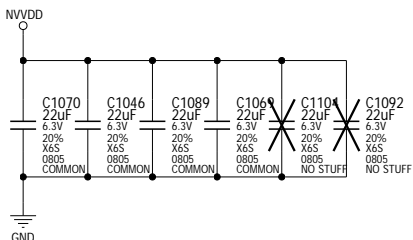
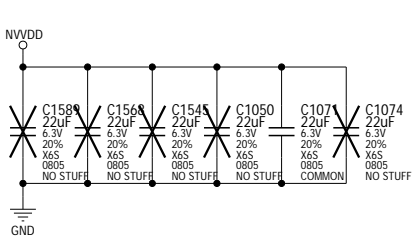
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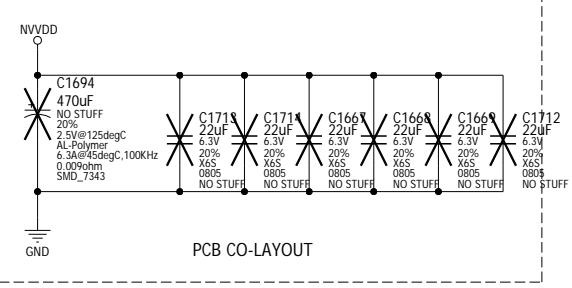
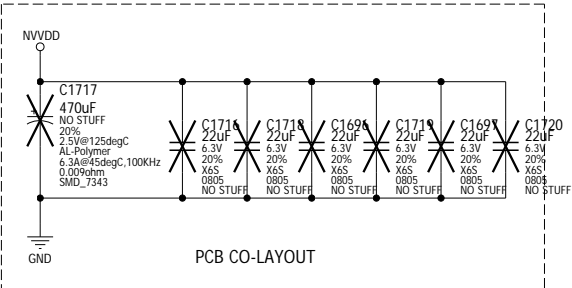
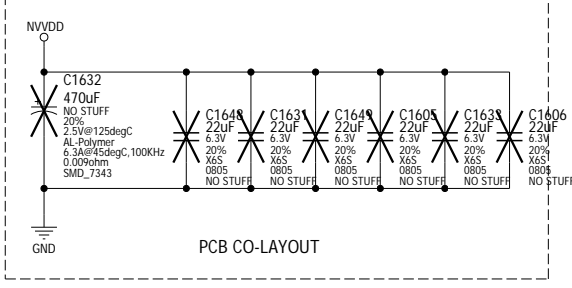
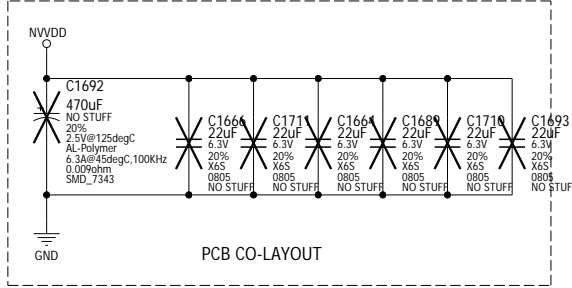
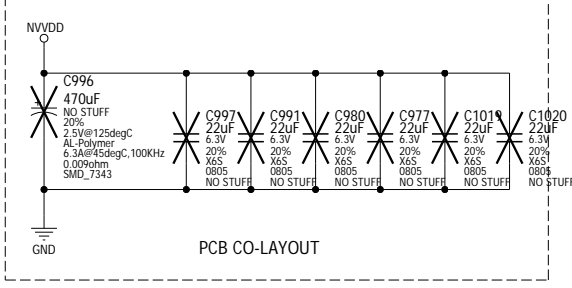
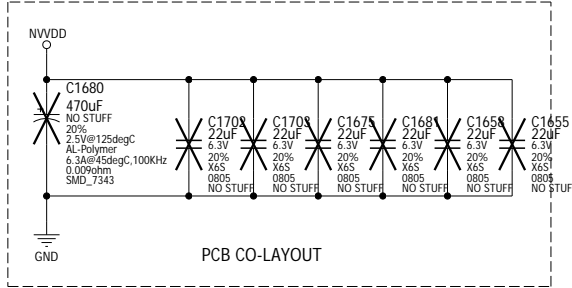
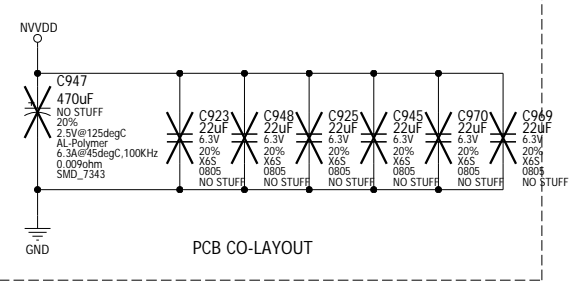
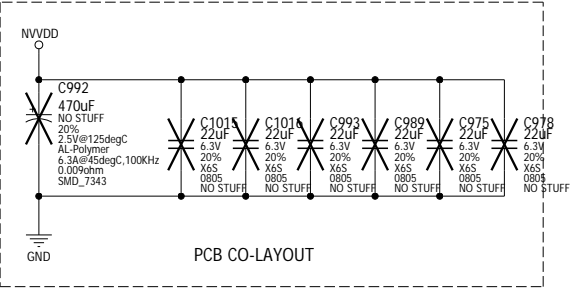
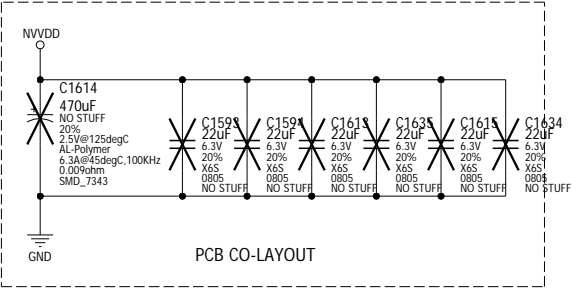
21-MAY-2020

PS NVVDD OUTPUT CAP



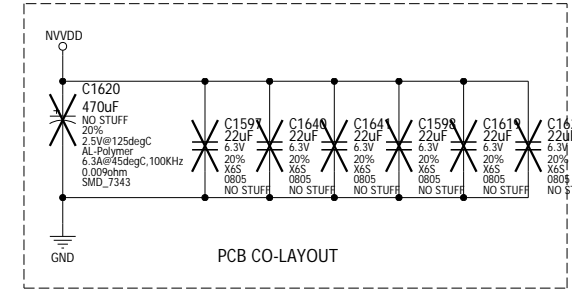
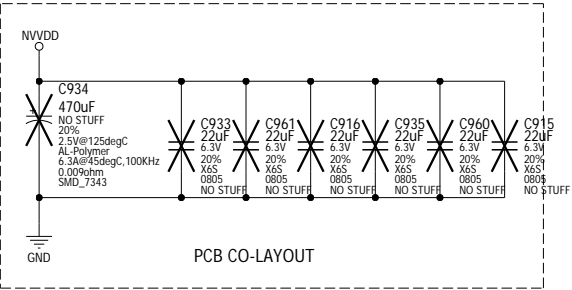
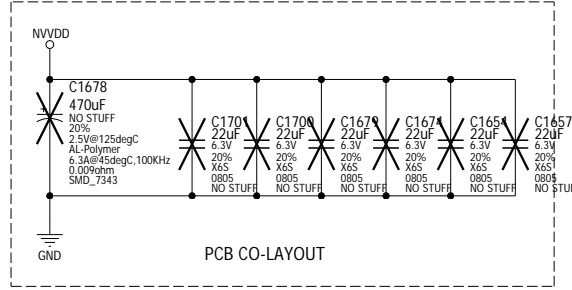
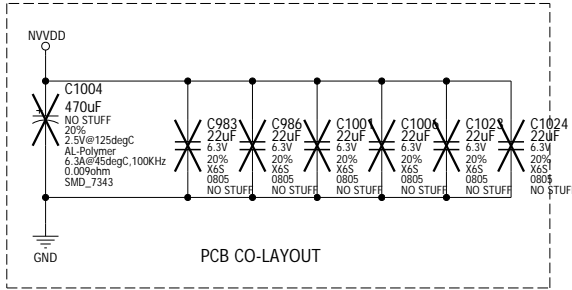
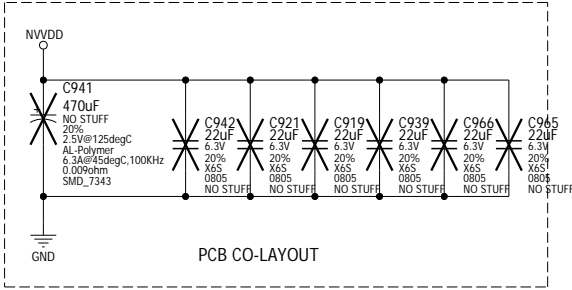
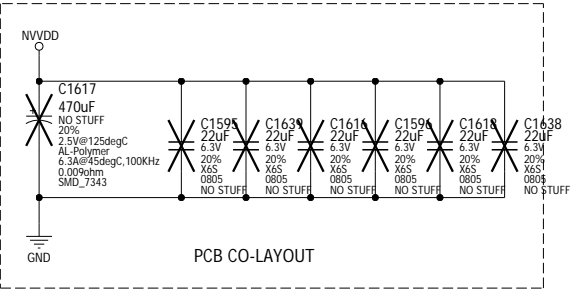
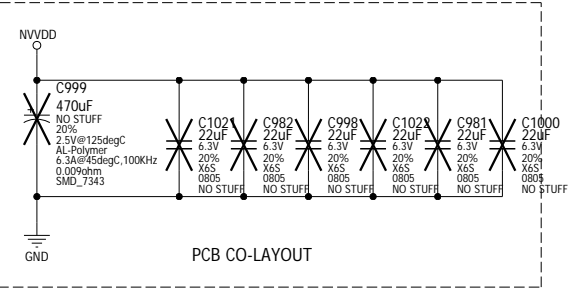
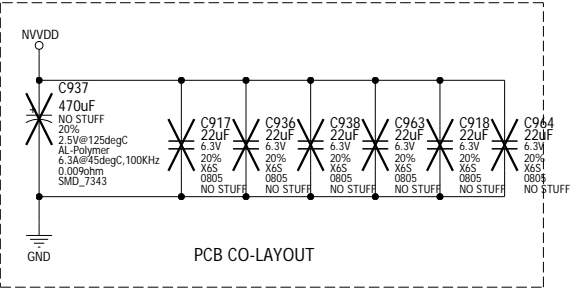
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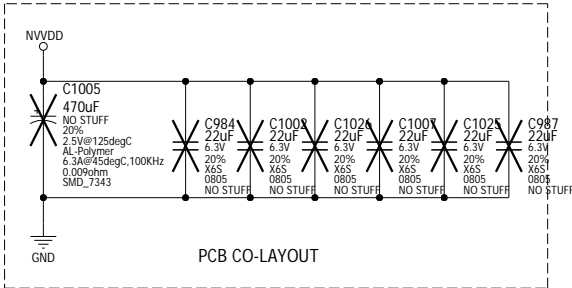
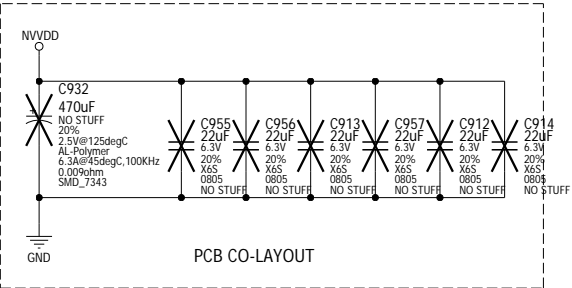
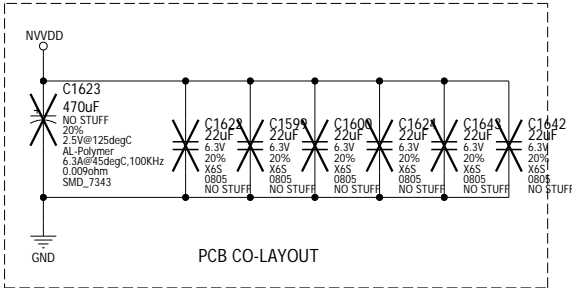
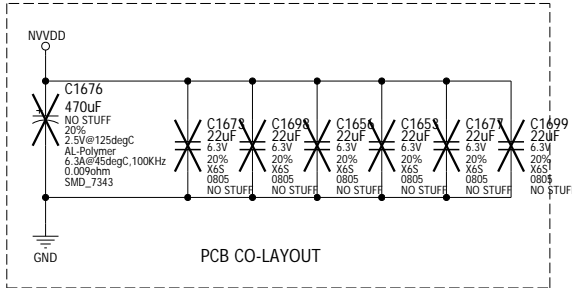
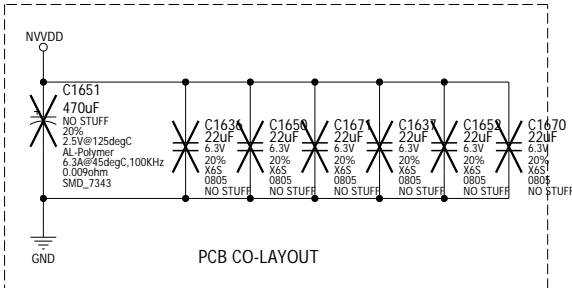
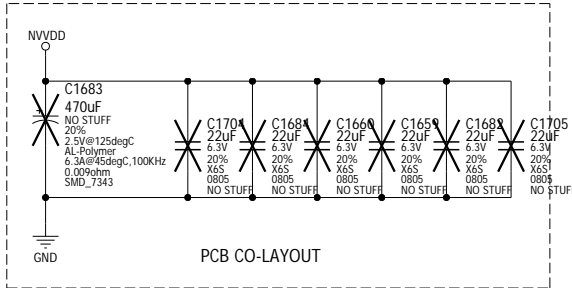
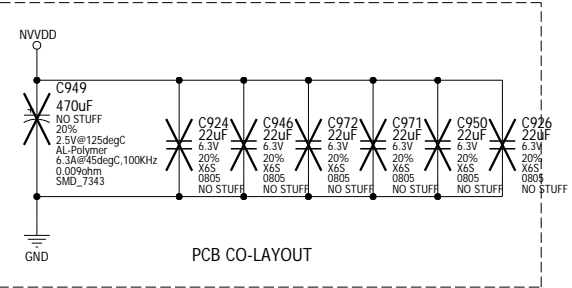
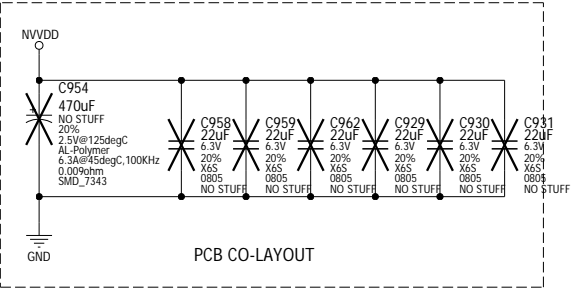
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BOM REV

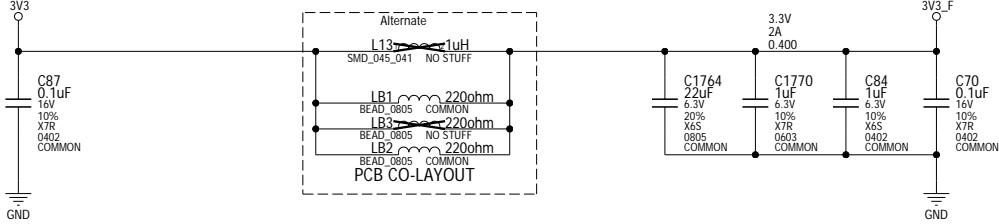
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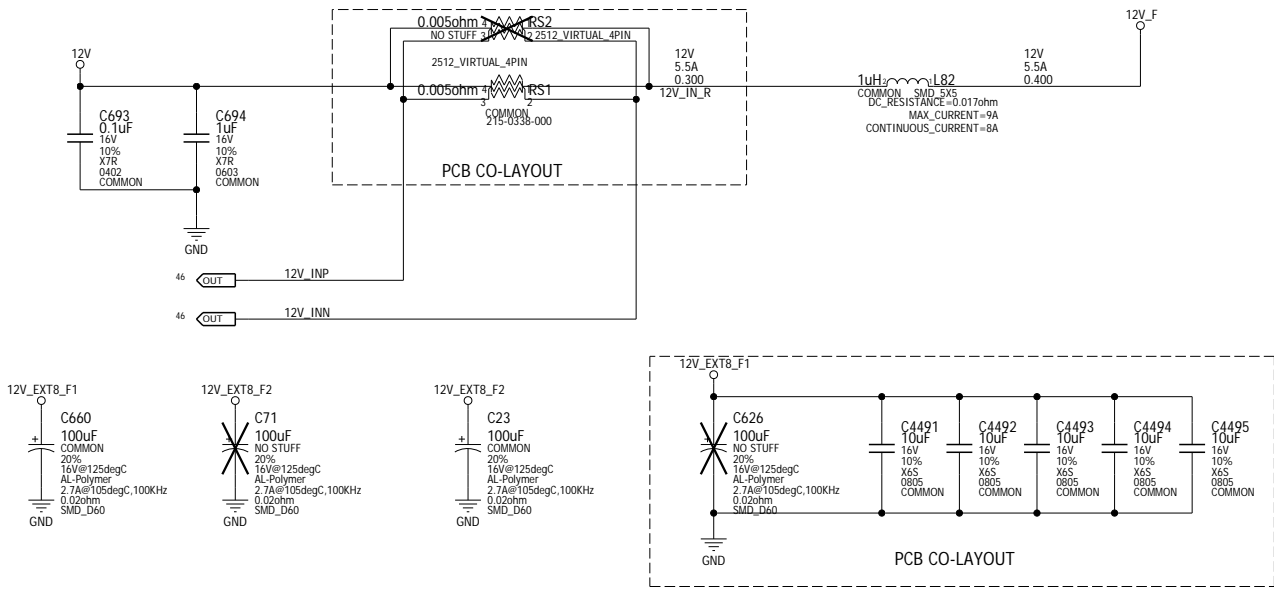
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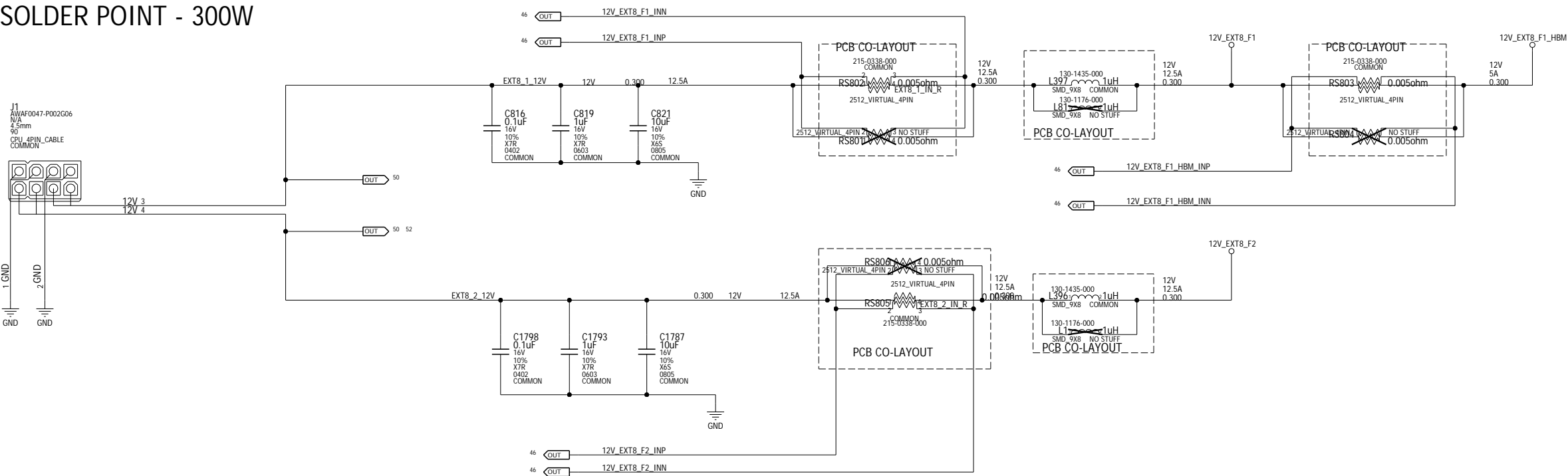
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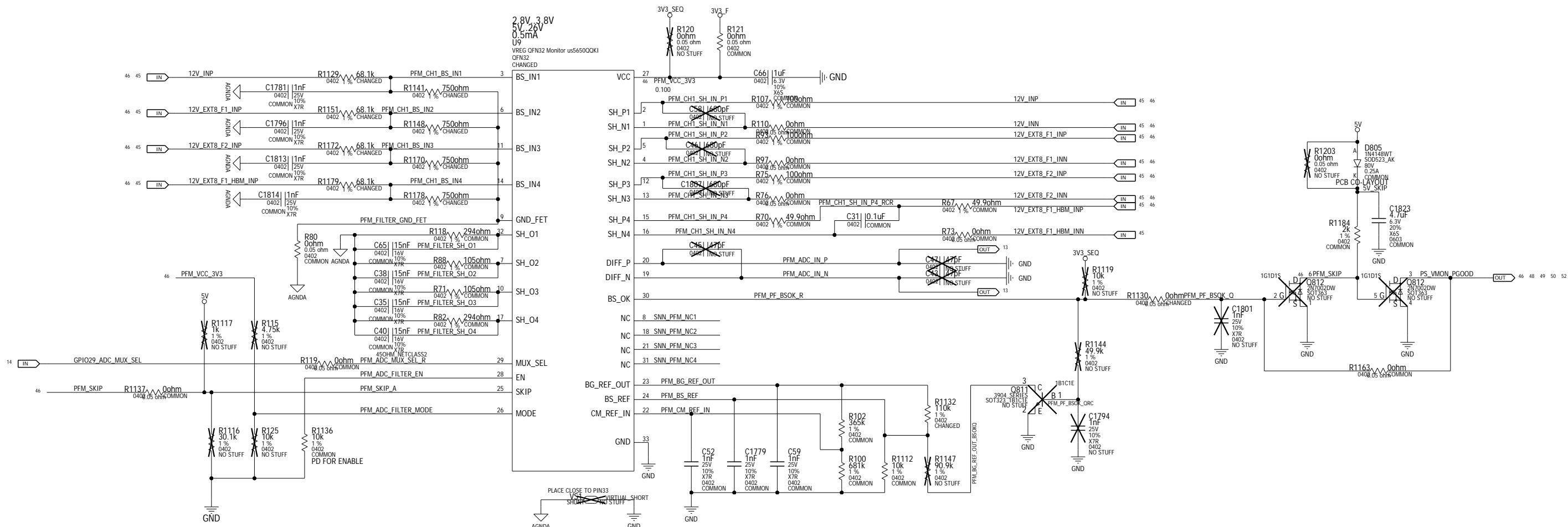
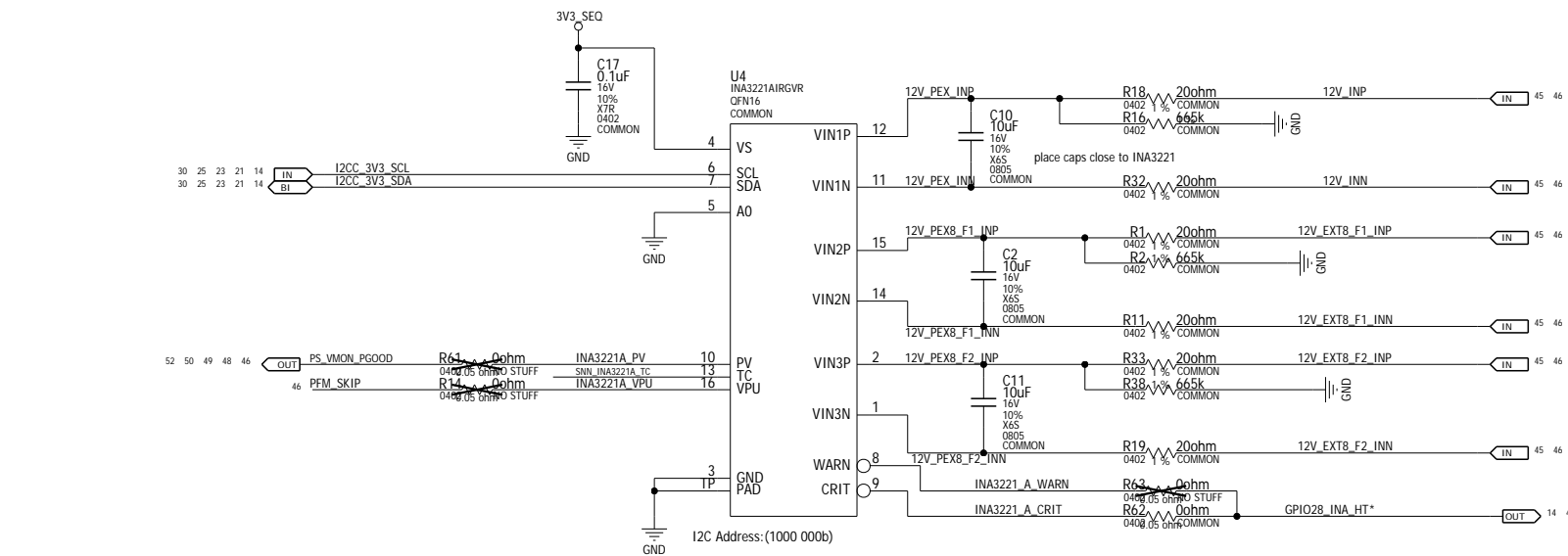


SINGLE CPU-8PIN PWR CONN SOLDER POINT - 300W




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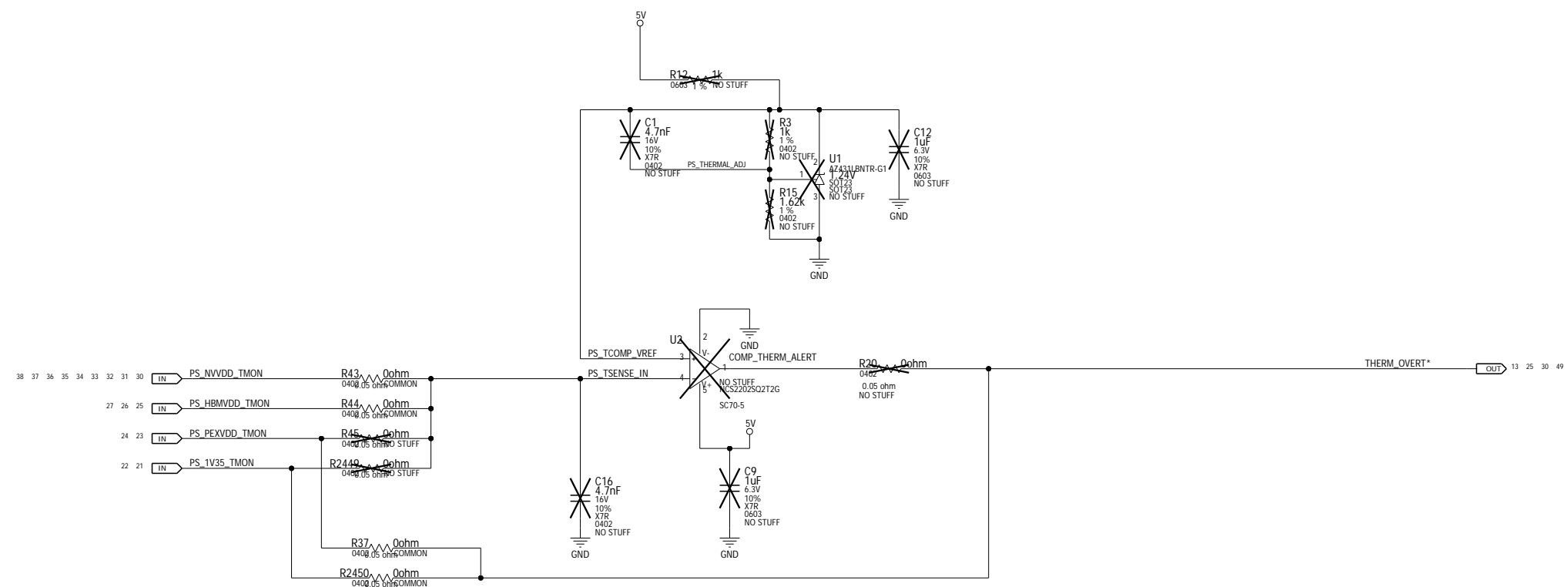


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PS THERMAL PROTECTION



ASSEMBLY	P1001 B01 SKU200 TESLA PASSIVE
PAGE DETAIL	PS: THERMAL PROTECTION

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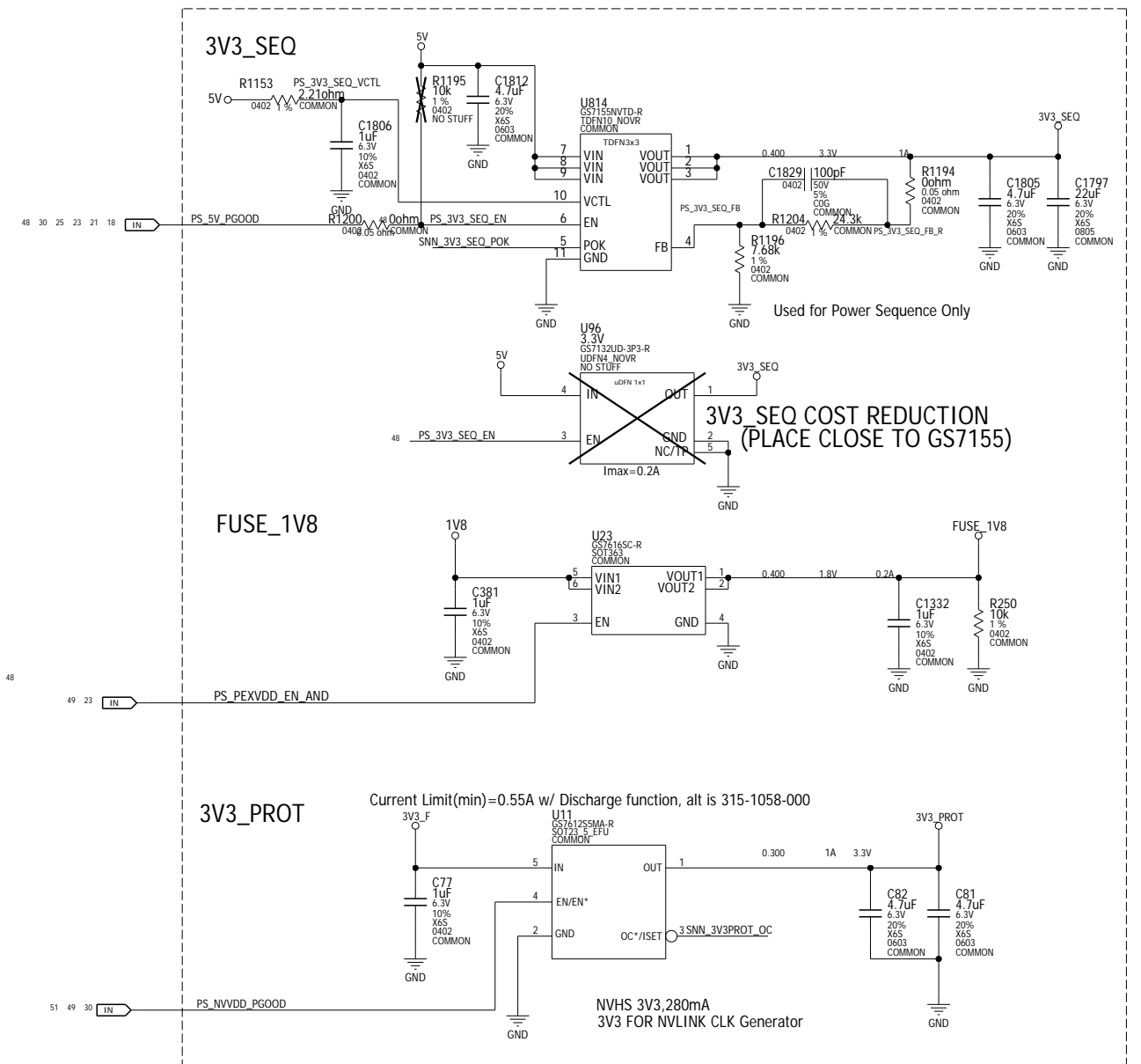
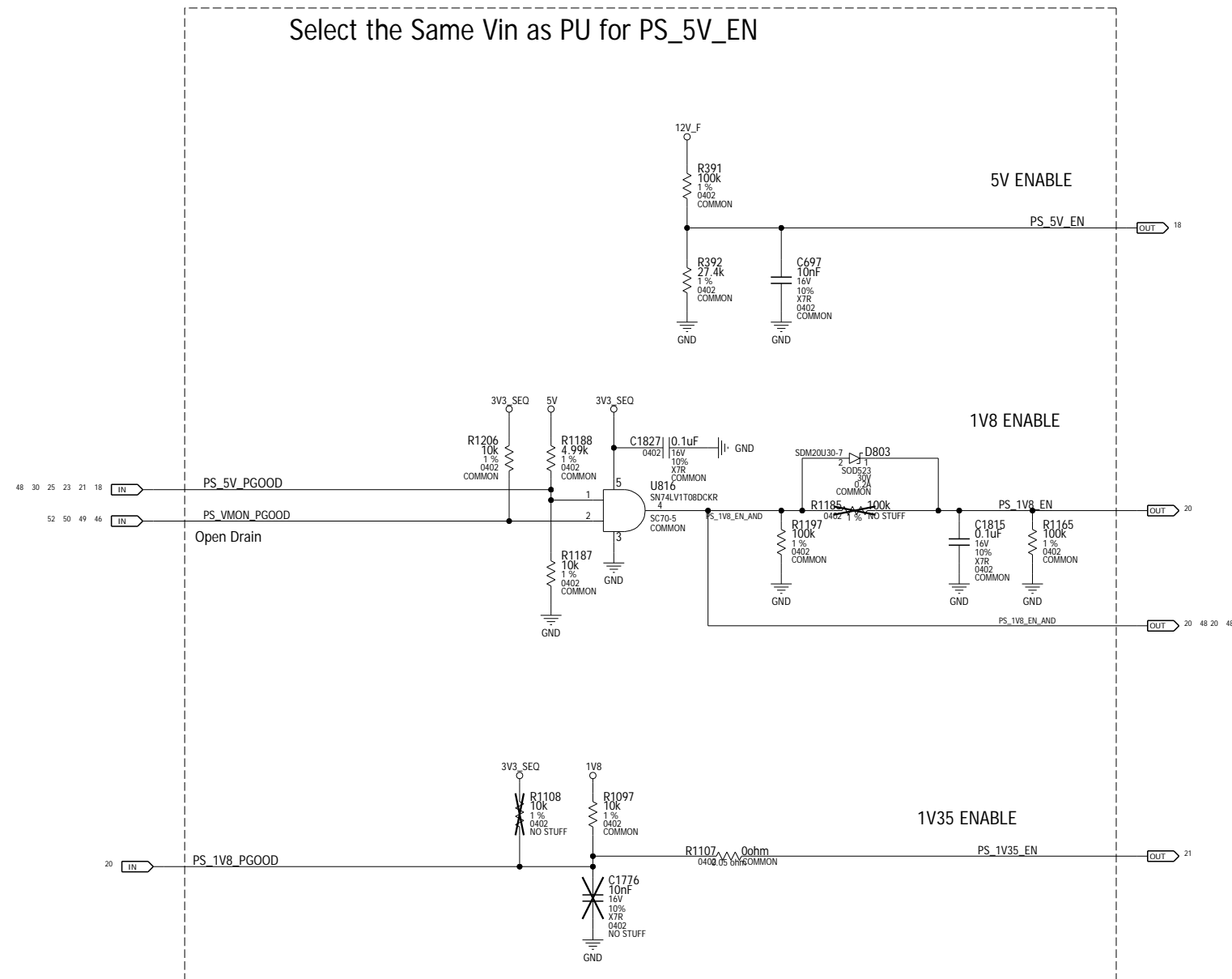
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BOM REV	A	DATE	21-MAY-2020

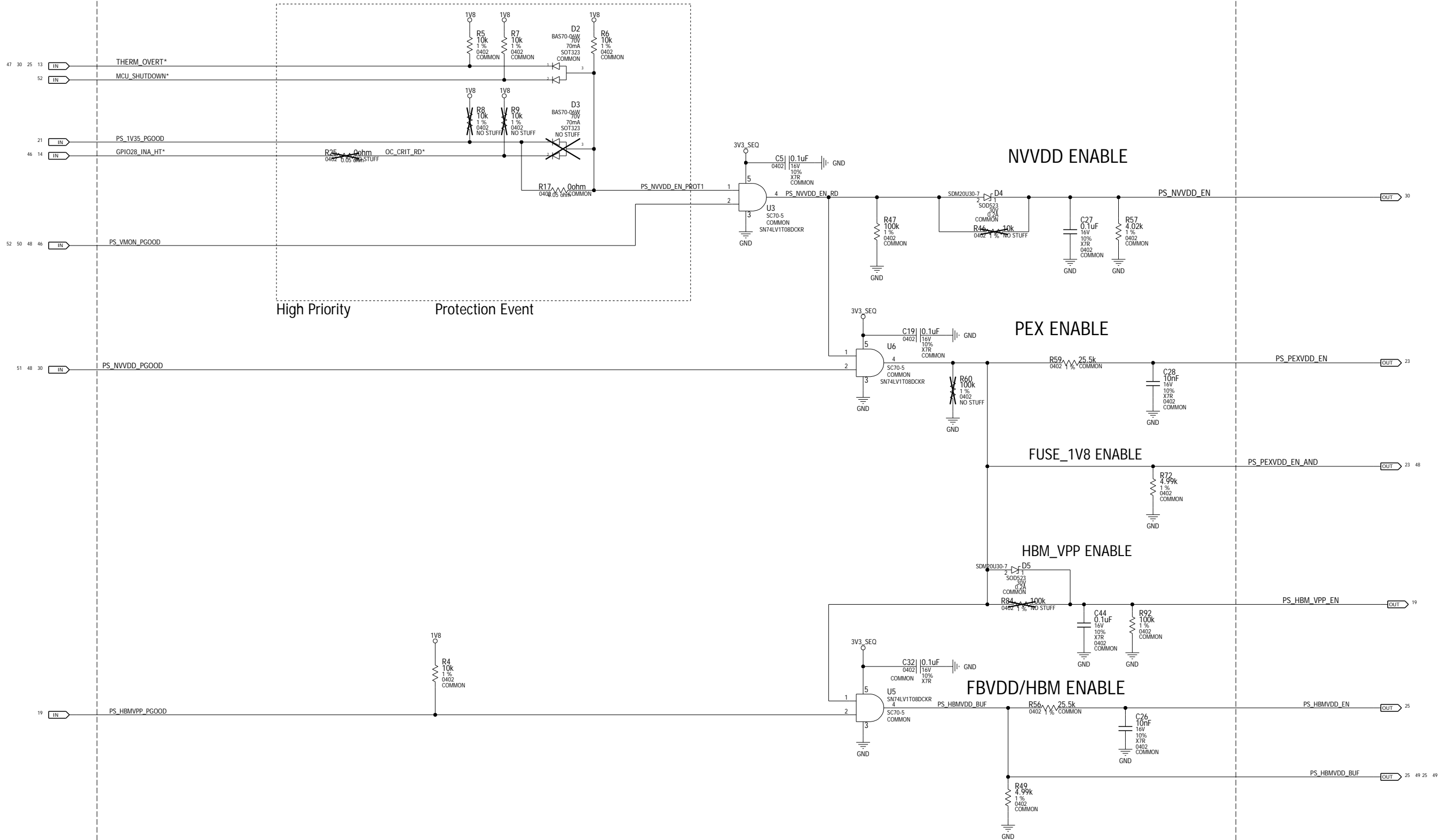
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ASSEMBLY	P1001 B01 SKU200 TESLA PASSIVE
PAGE DETAIL	SEQUENCE:5V,1V8, 1V35, 3V3_SEQ ENABLE

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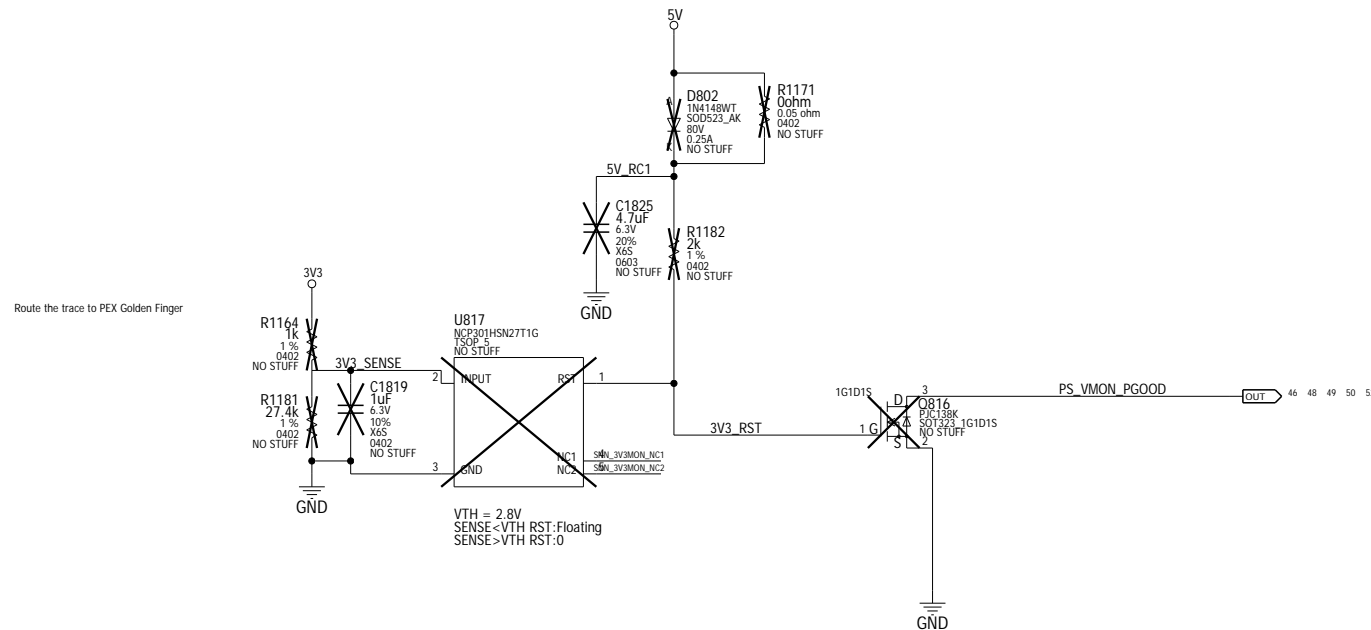
SEQUENCE NVVDD, PEX_DVDD, HBM_VDD ENABLE



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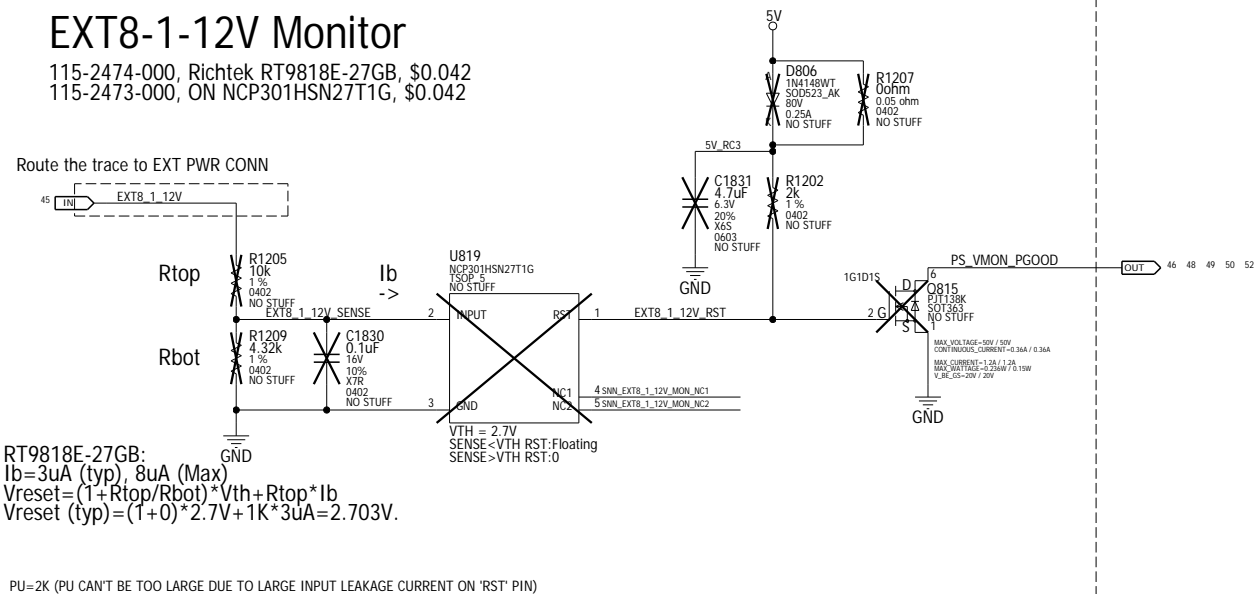
SEQUENCE PCIe MONITOR

PCIE Voltage Monitor



EXT8-1-12V Monitor

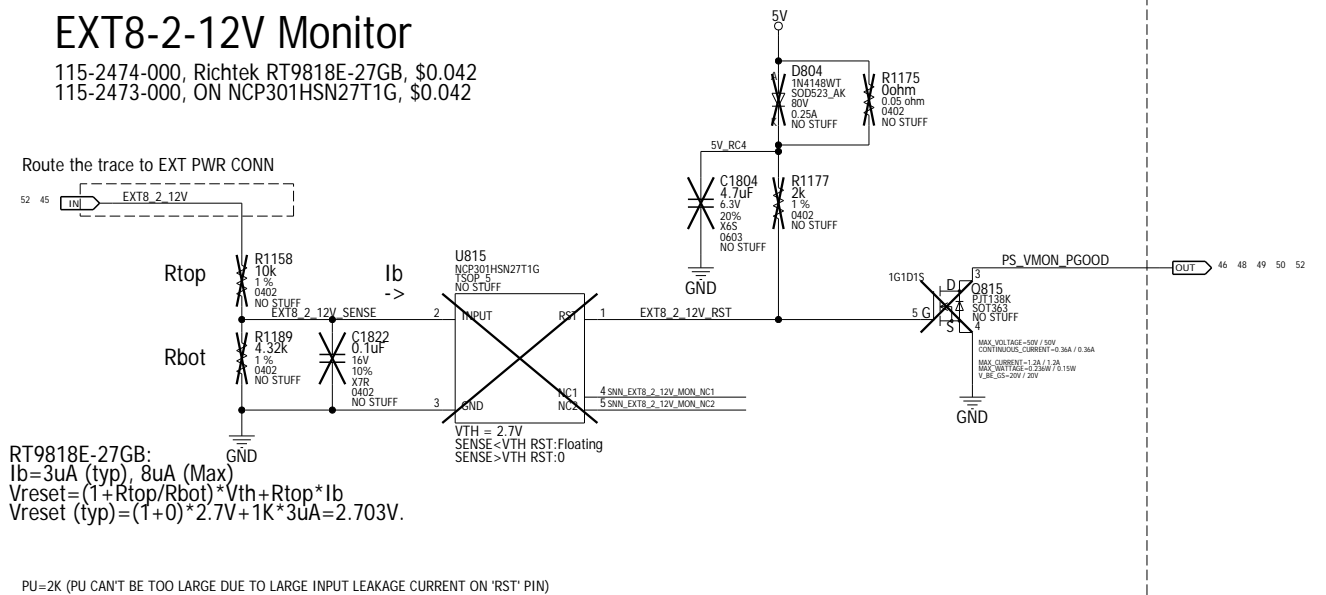
115-2474-000, Richtek RT9818E-27GB, \$0.042
115-2473-000, ON NCP301HSN27T1G, \$0.042



PU=2K (PU CAN'T BE TOO LARGE DUE TO LARGE INPUT LEAKAGE CURRENT ON 'RST' PIN)

EXT8-2-12V Monitor

115-2474-000, Richtek RT9818E-27GB, \$0.042
115-2473-000, ON NCP301HSN27T1G, \$0.042



PU=2K (PU CAN'T BE TOO LARGE DUE TO LARGE INPUT LEAKAGE CURRENT ON 'RST' PIN)

ASSEMBLY	P1001 B01 SKU200 TESLA PASSIVE
PAGE DETAIL	SEQUENCE: PCIe MONITOR

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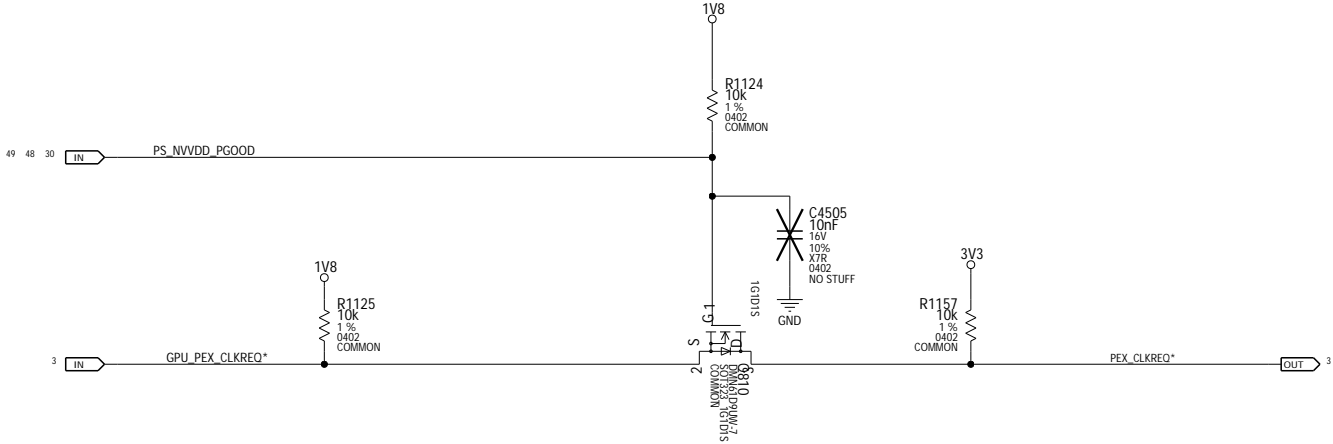
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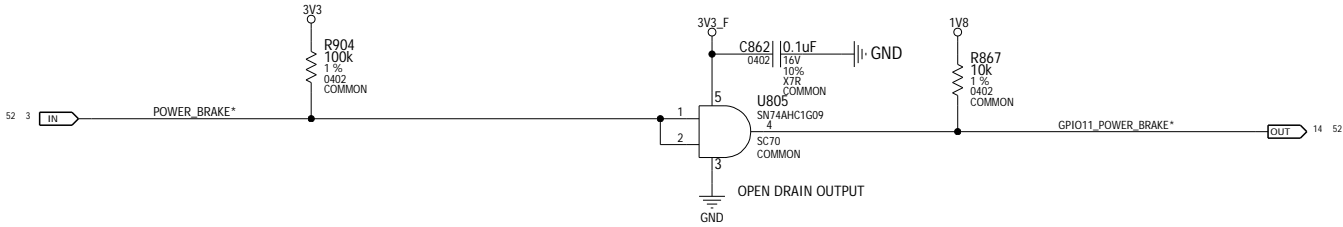
SEQUENCE MISC

PEX_CLKREQ*

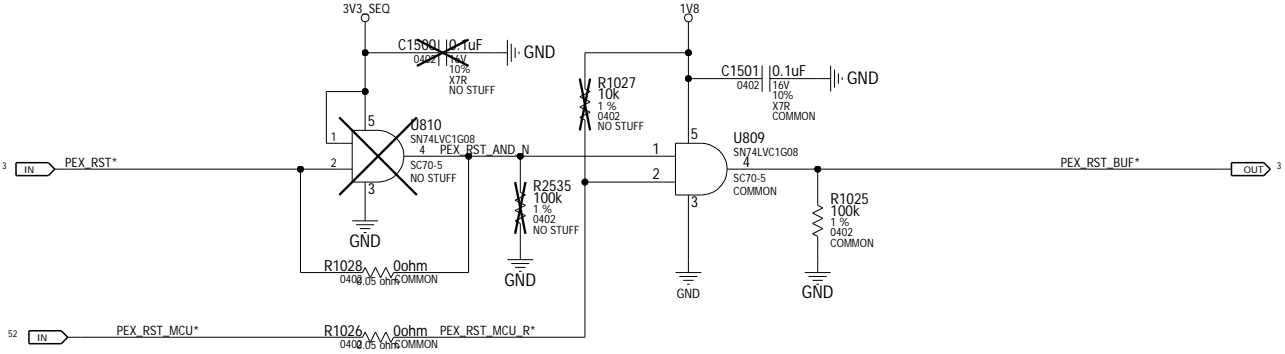


PEX_REFCLK Power Domain: HVDD(1.35V)

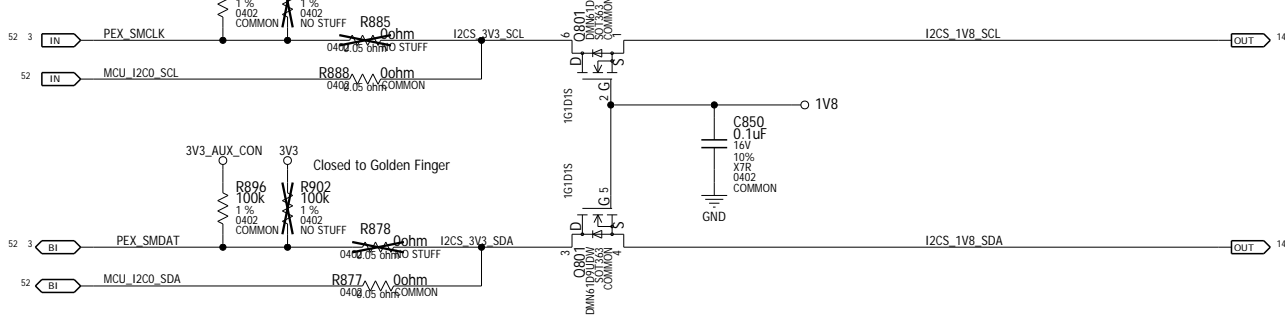
POWER BRAKE*



PEX_RST# LOGIC



SMBUS



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SEQUENCE ZERO POWER MCU

1

2

3

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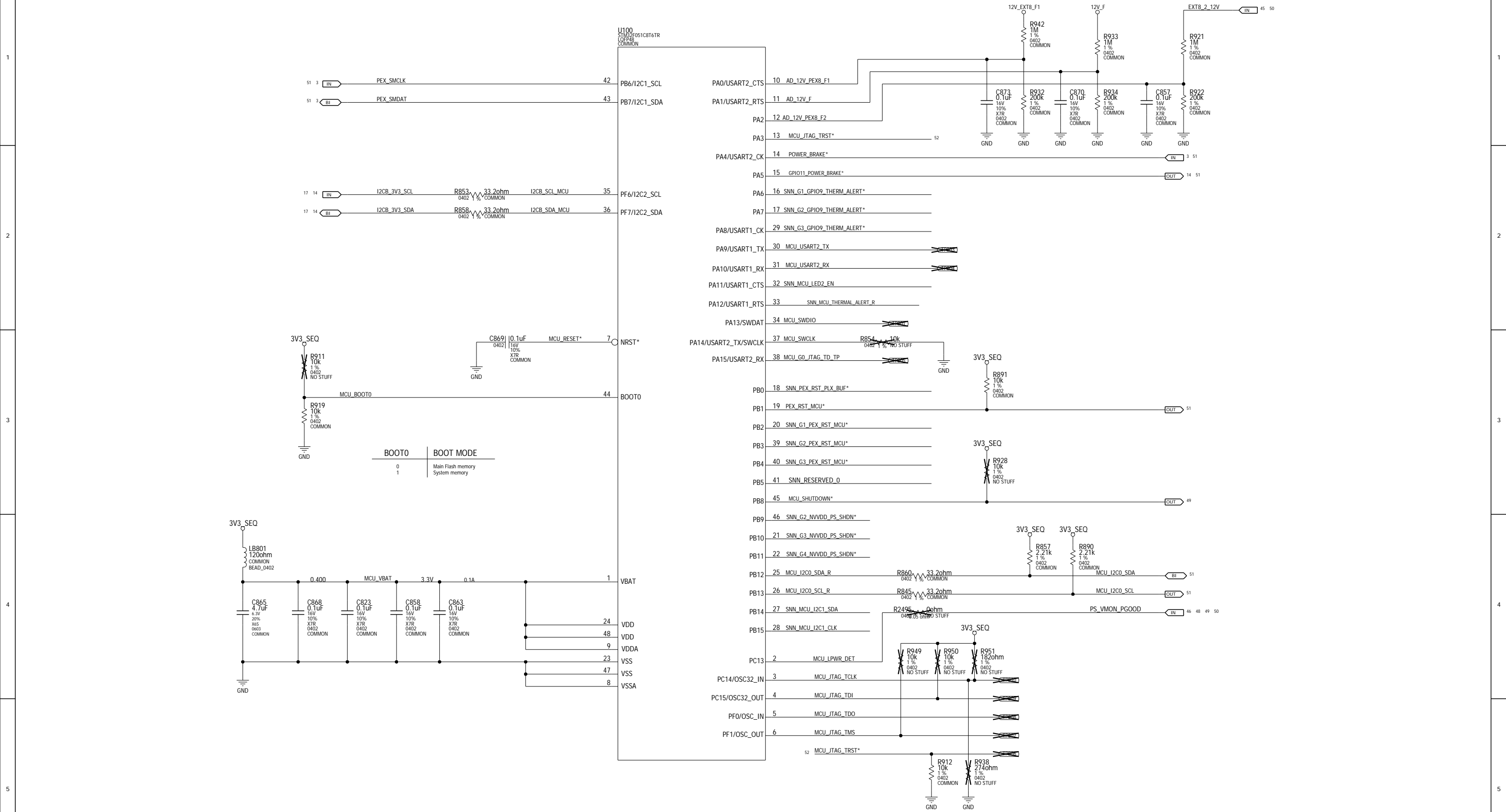
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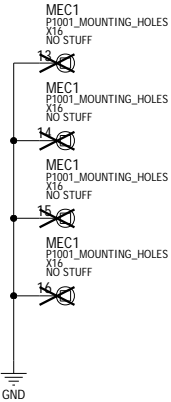
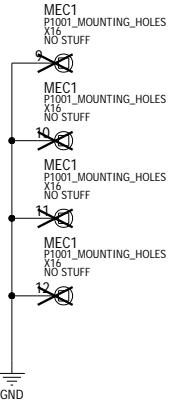
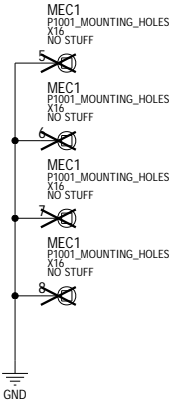
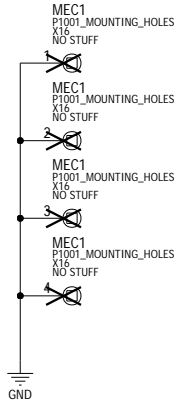
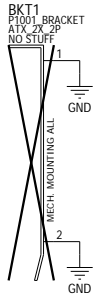
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