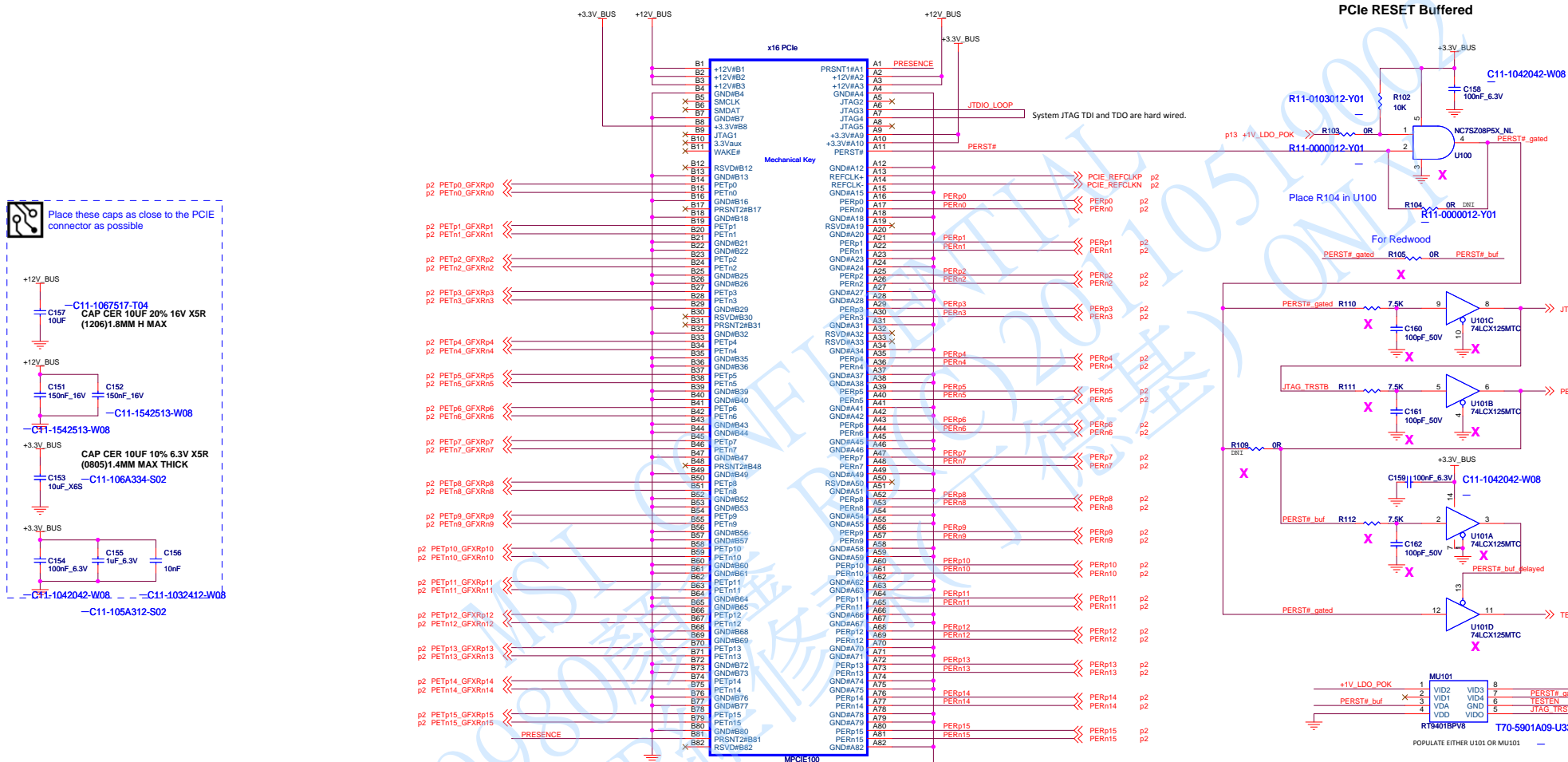


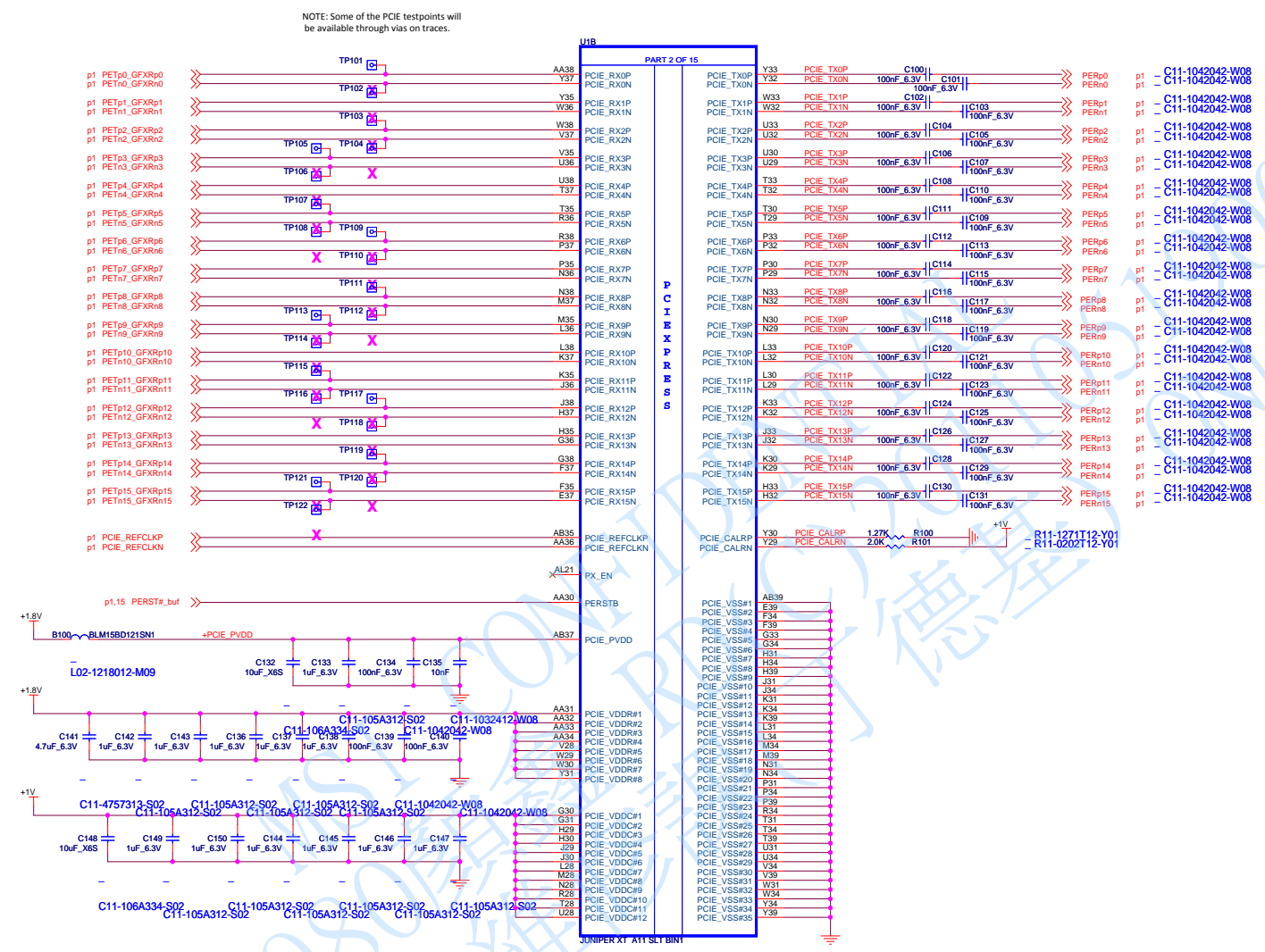


PCI-EXPRESS EDGE CONNECTOR



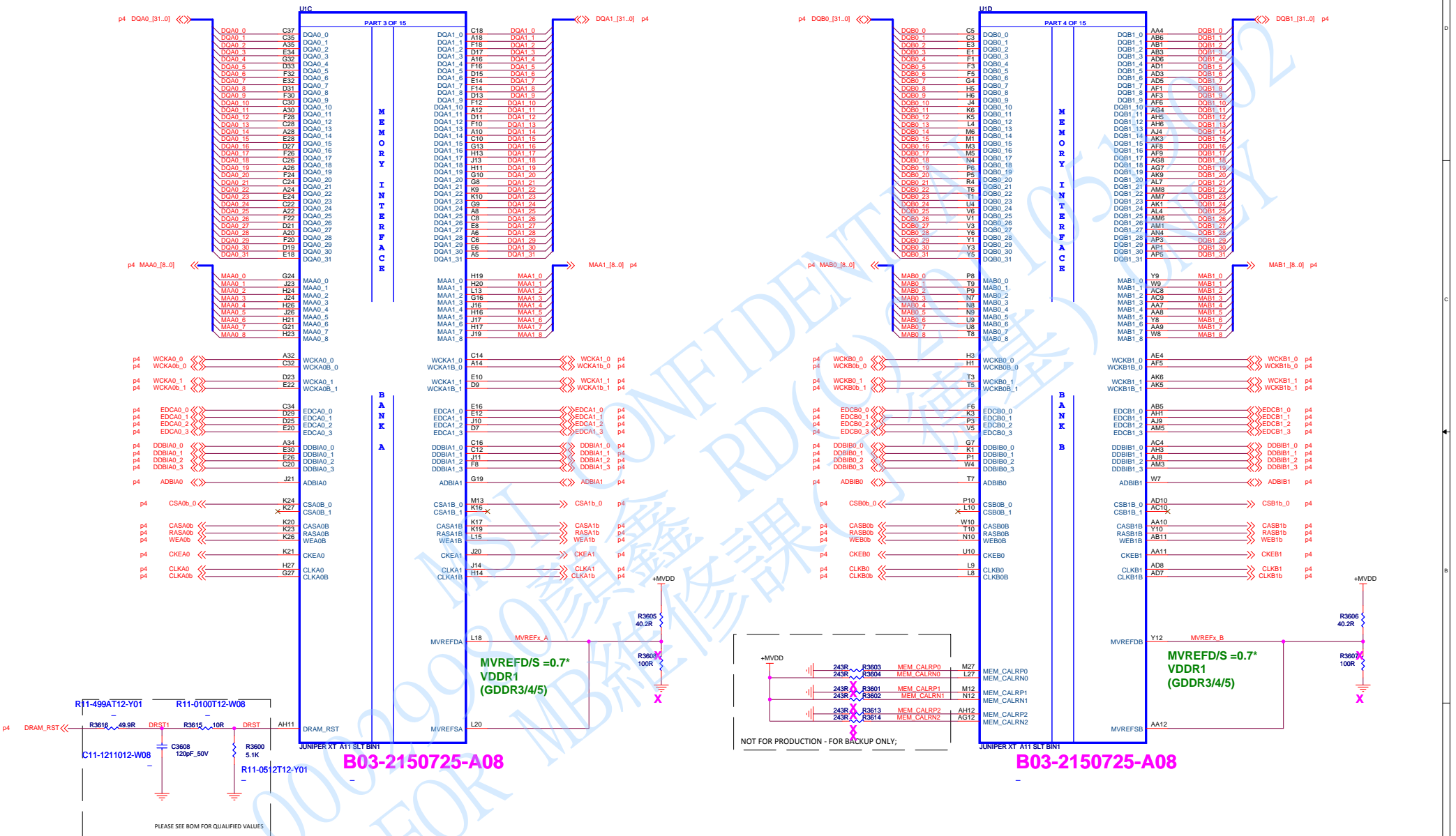
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

(2) M2 PCIe Interface

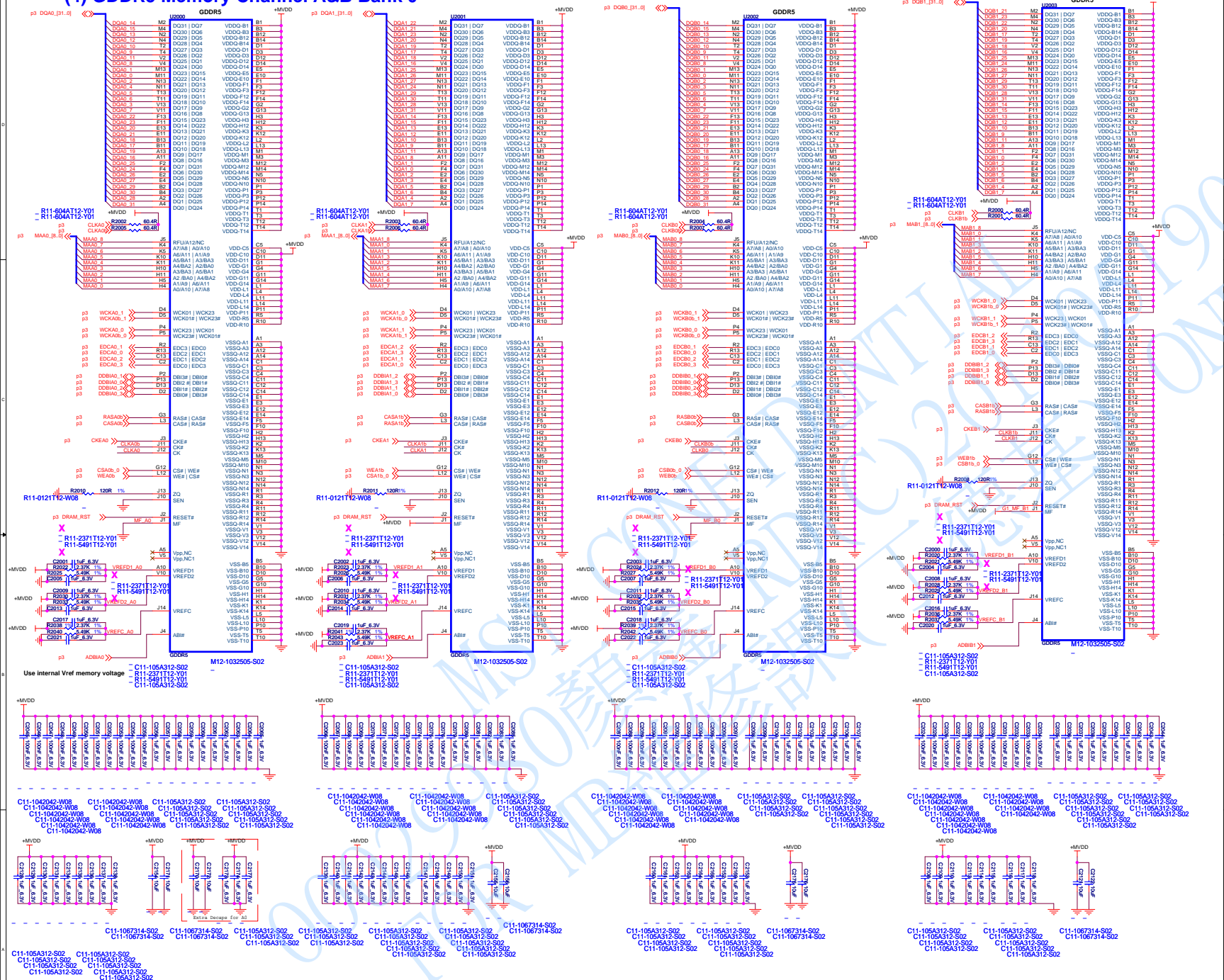


B03-2150725-A08

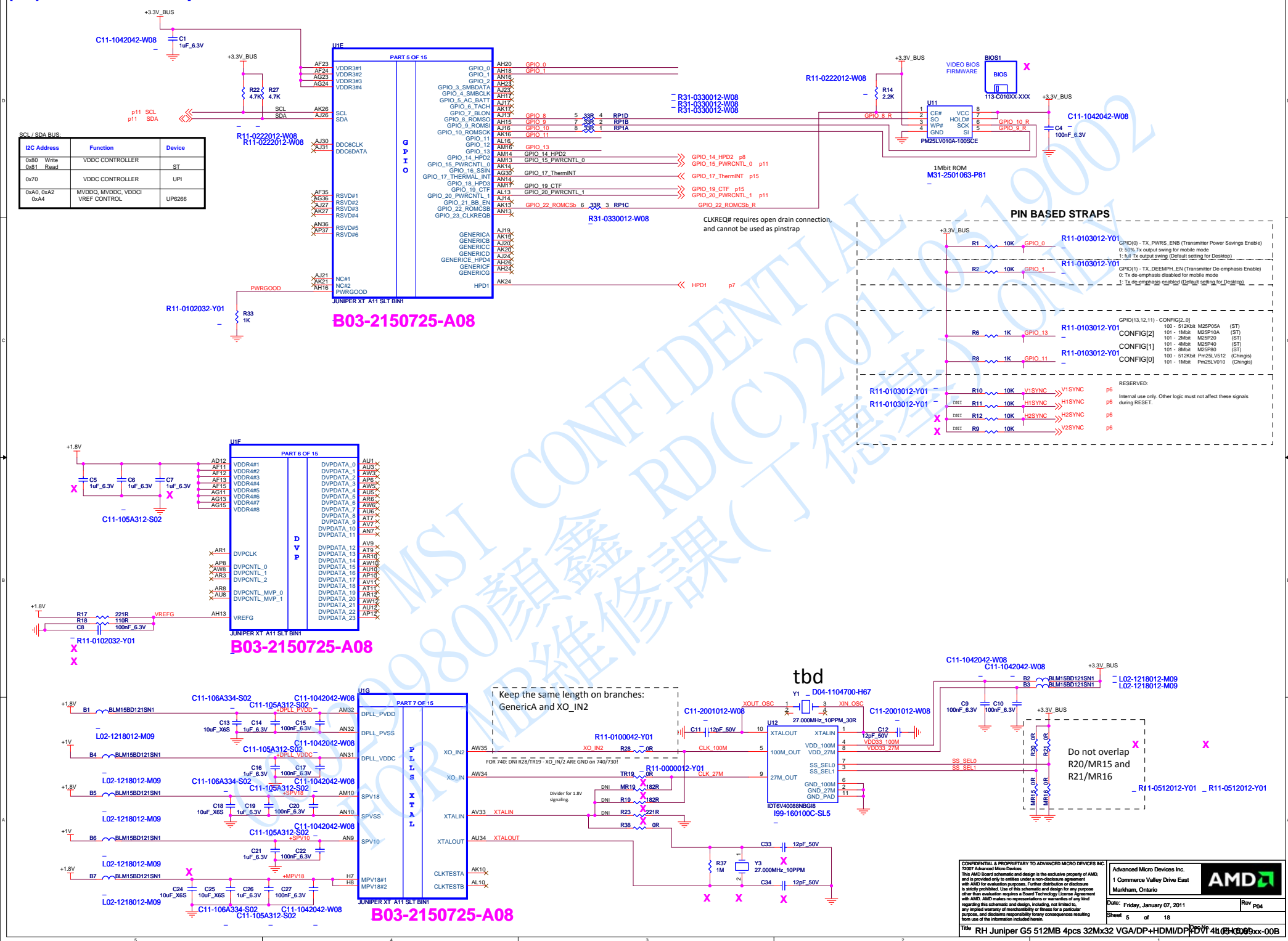
(3) M2 MEM Interface Ch A&B



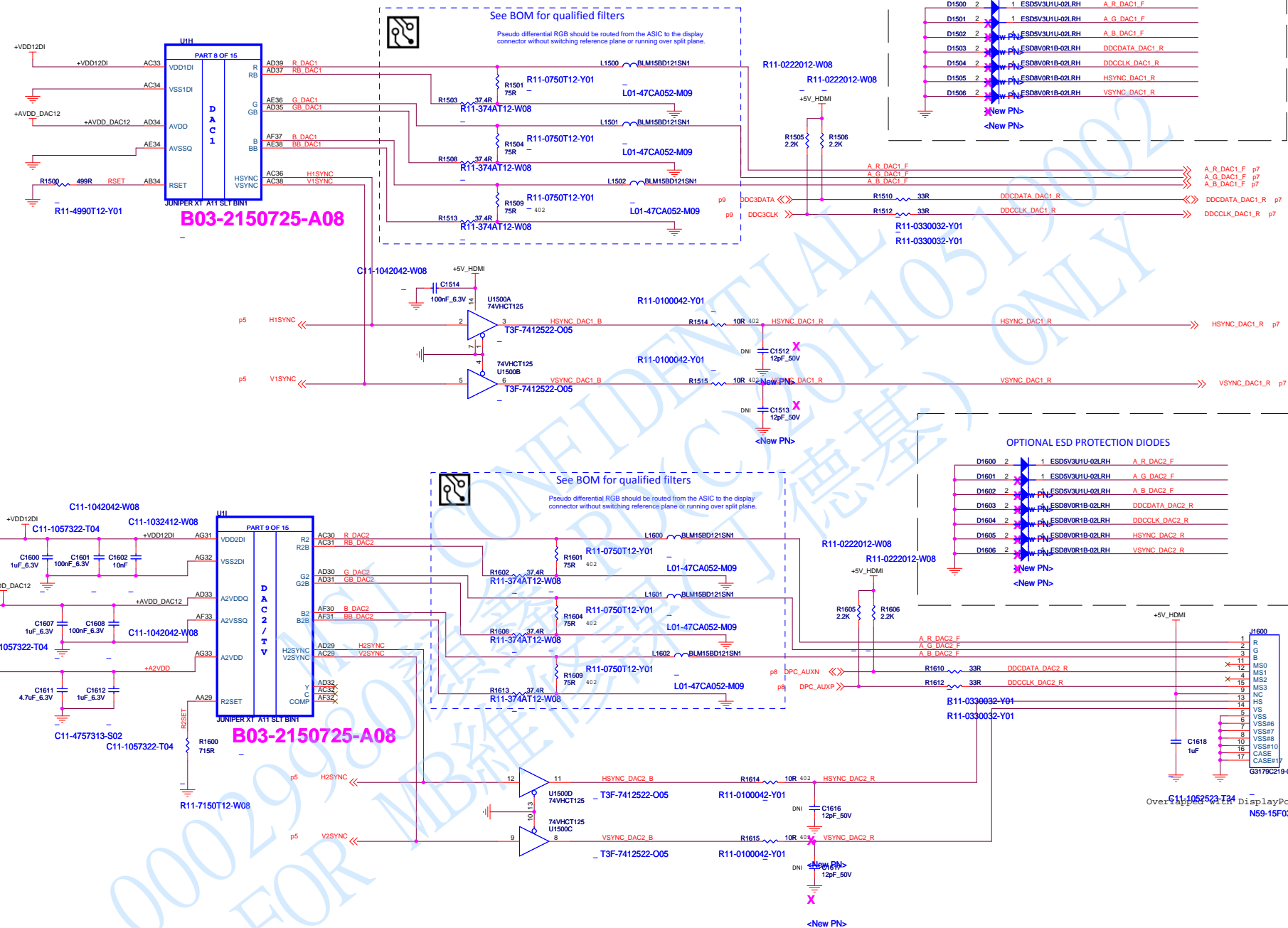
(4) GDDR5 Memory Channel A&B Bank 0



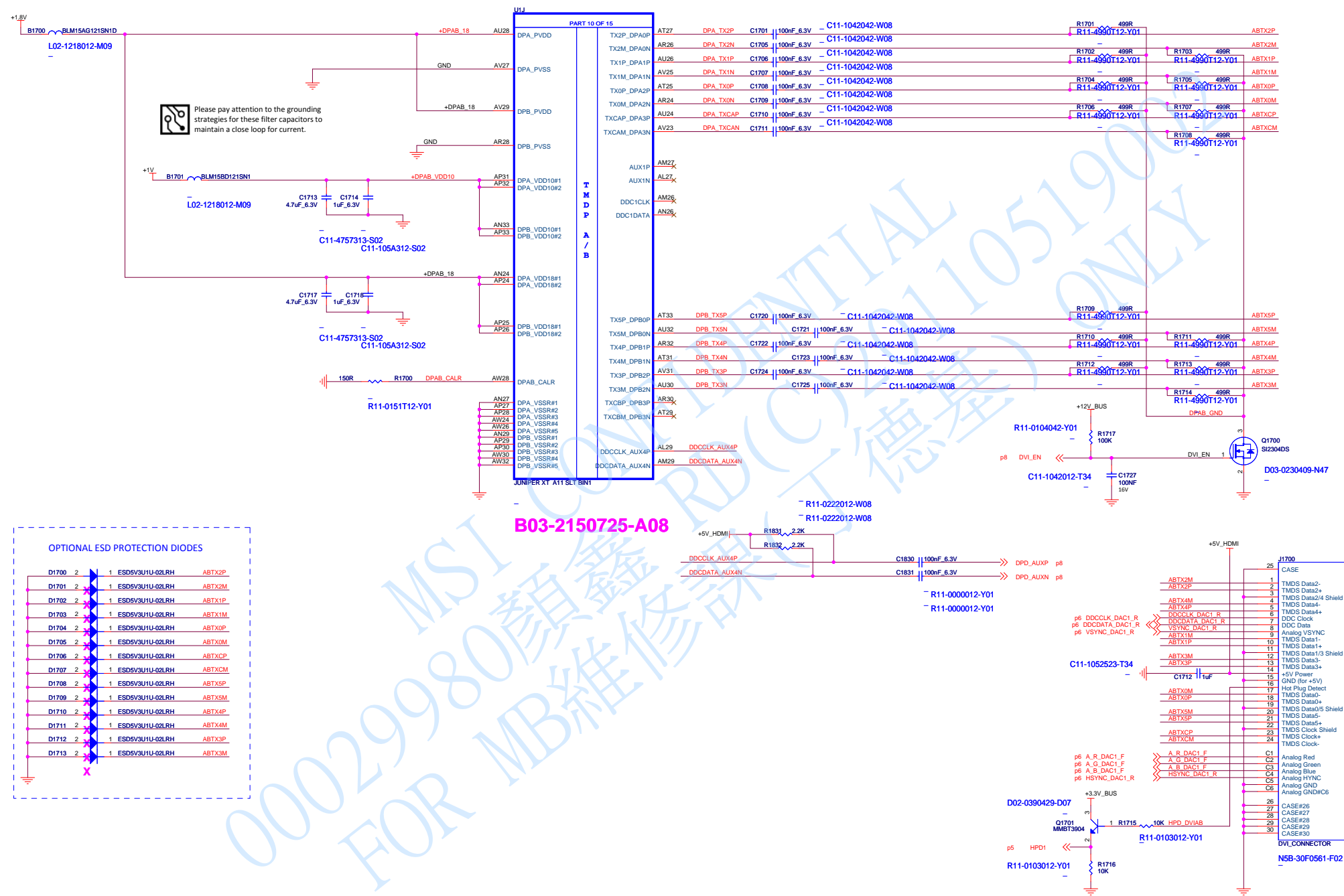
(06) M2 GPIOs Strap CF XTAL OSC



(07) M2 DAC1 and DAC2



(08) M2 TMDP A&B dDVI-I TOP



CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.
72007 Advanced Micro Devices

This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims any and all consequences resulting from use of the information contained herein.

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario



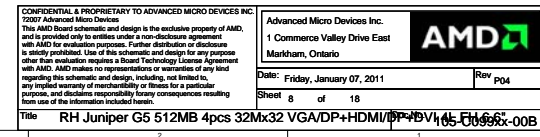
Date: Friday, January 07, 201

Sheet 7 of 18

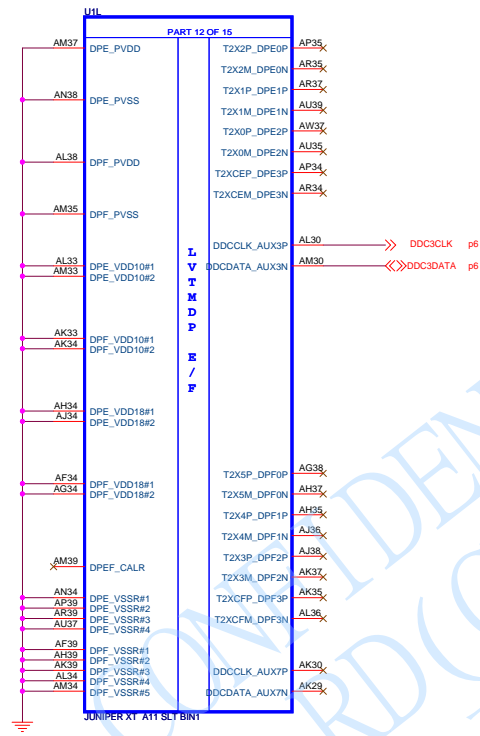
Rev P04

Title RH Juniper G5 512MB 4pcs 32Mx32 VGA/DP+HDMI/DP+DVI+4L FH 6.6" 105-2099xx-00B

removed Co-Lay DP port

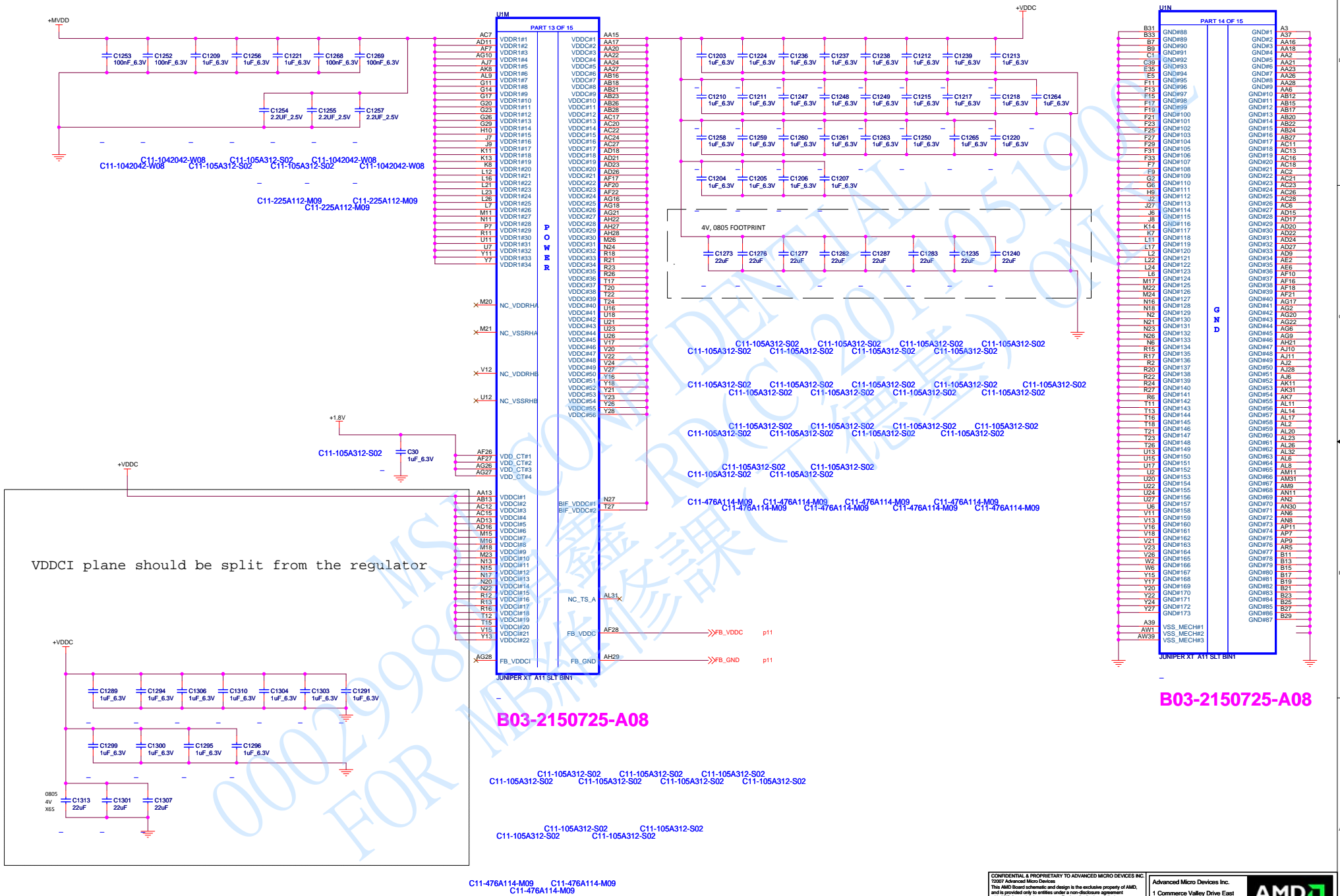


(10) M2 LVTMDP E&F



B03-2150725-A08

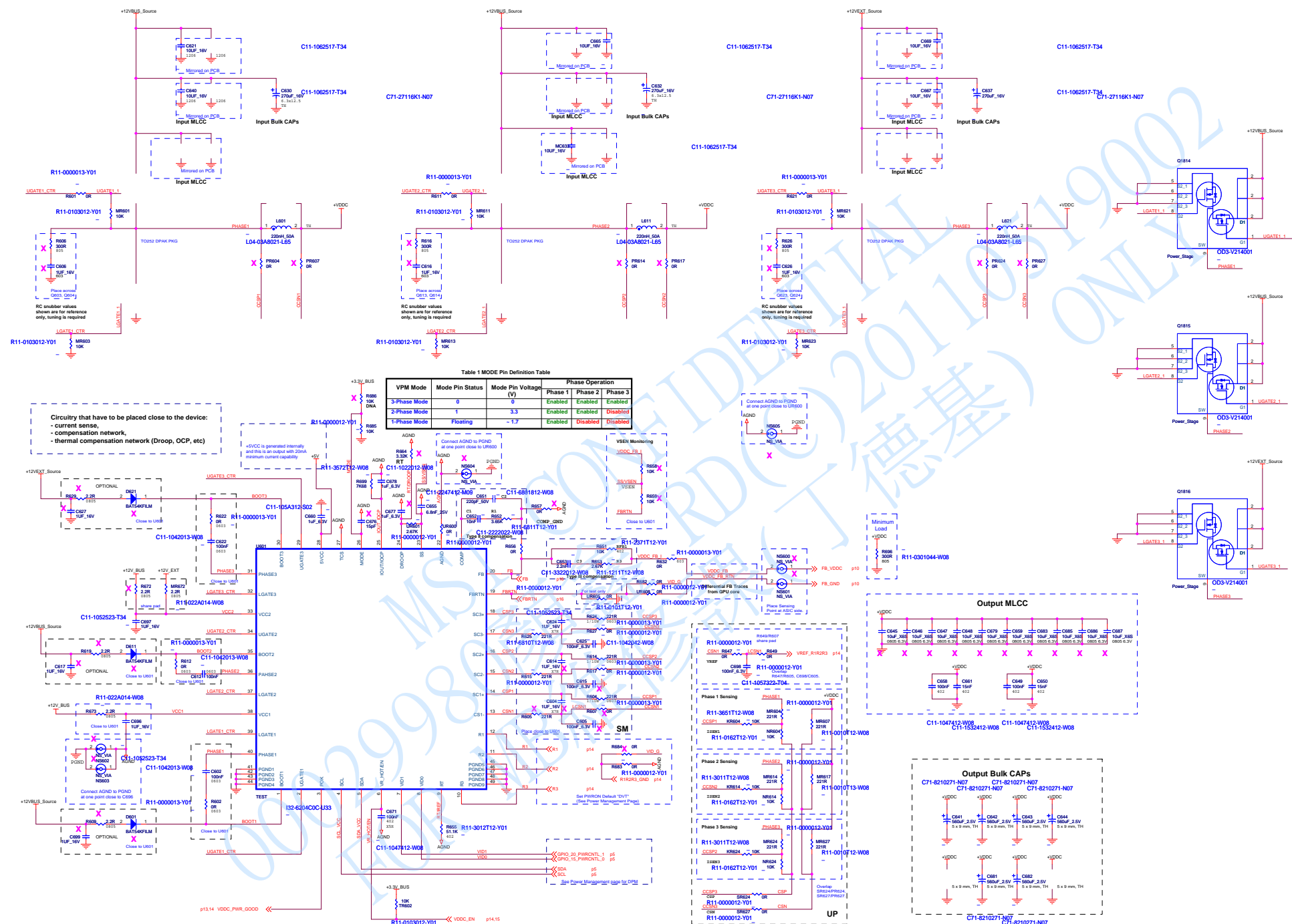
(11) M2 Power & GND



(11) VDDC

PHASE 1

PHASE 2



VPM Mode	Mode Pin Status	Mode Pin Voltage (V)	Phase Operation		
			Phase 1	Phase 2	Phase 3
3-Phase Mode	0	0	Enabled	Enabled	Enabled
2-Phase Mode	1	3.3	Enabled	Enabled	Disabled
1-Phase Mode	Floating	~ 1.7	Enabled	Disabled	Disabled

- current sense,
- compensation network,
- thermal compensation network (Droop, OCP, etc)


+5VCC is generated internally and this is an output with 20mA minimum current capability

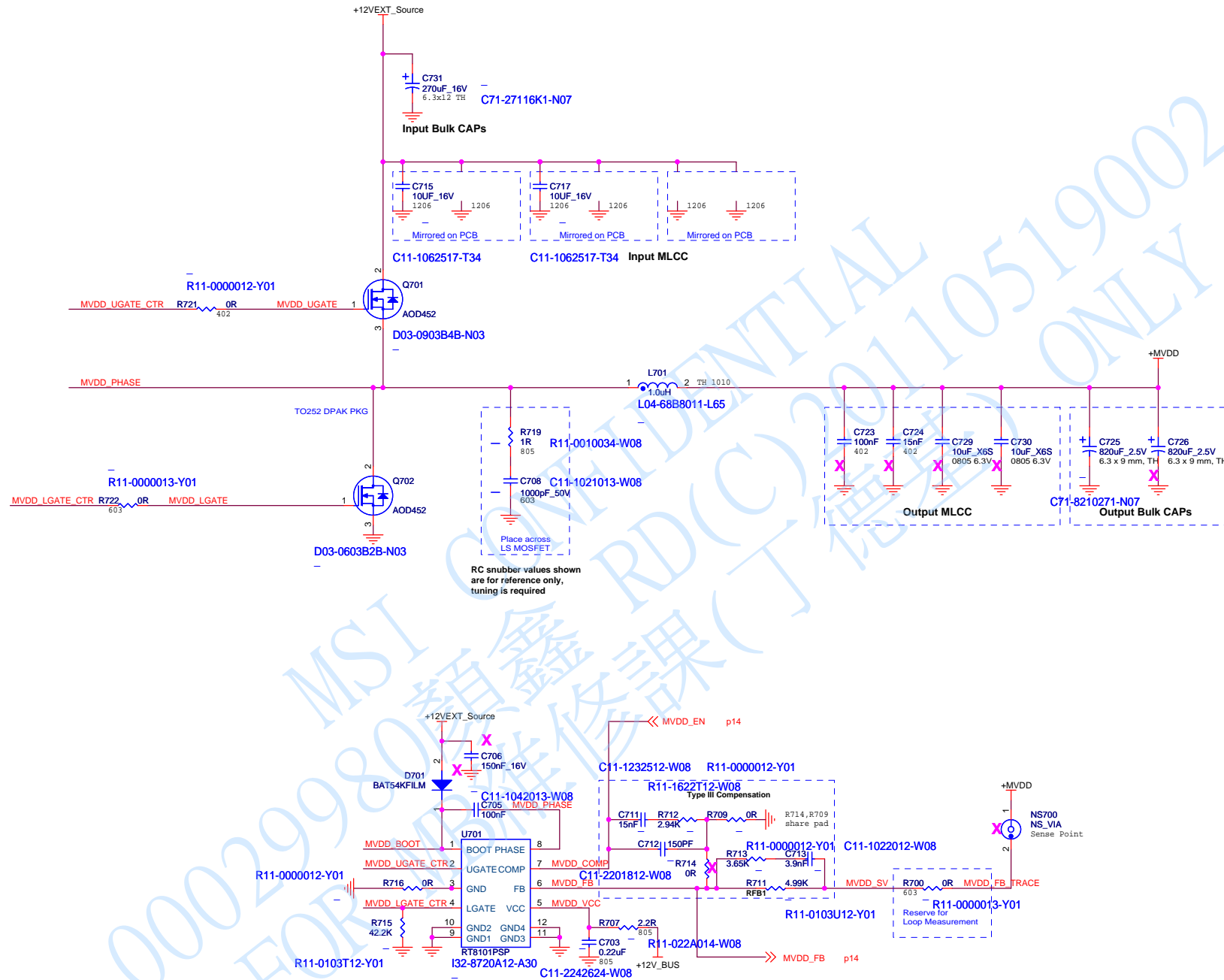
Connect AGND to PGND at one point close to UR600

Minimum Load
+VDDC

Output MLCC

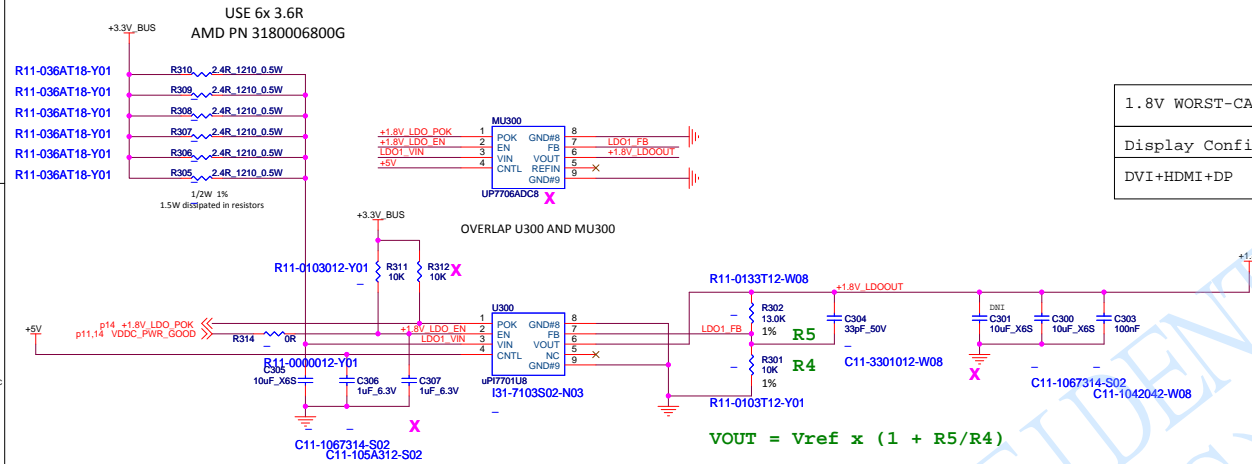
Output Bulk CAPs

CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC. 1997 Advanced Micro Devices This document contains information in the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement. It is not to be distributed outside the entity, nor is it to be reproduced, copied, or otherwise used in any manner without the express written permission of AMD. AMD makes no representation or warranty of any kind, either expressed or implied, regarding the design, manufacture, or suitability of any product described herein, or regarding the design, manufacture, or suitability of any implied warranty of merchantability or fitness for a particular purpose, or regarding the design, manufacture, or suitability of any product described herein, or regarding the design, manufacture, or suitability of any product described herein.		Advanced Micro Devices Inc. 1 Commerce Valley Drive East Mahanah, Ontario			
Date: <u>Friday, January 07, 2011</u>		Rev: <u>P04</u>			
Sheet: <u>11</u> of <u>18</u>					
Title: <u>RH Jupiter GS 512MB 4pcs 32m32c VGADP-P-HDMI/D-SubV1.4</u>					

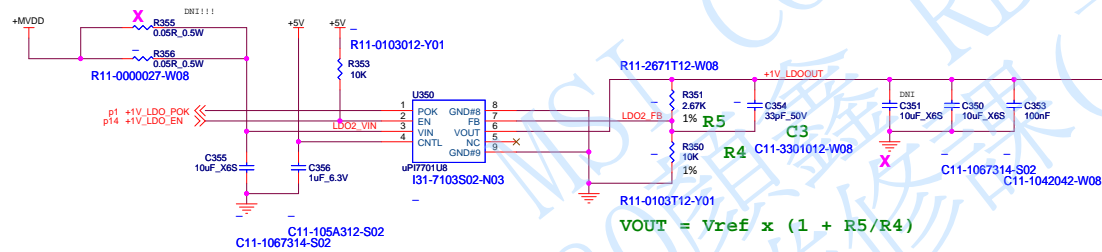


(15) Linear Regulators

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

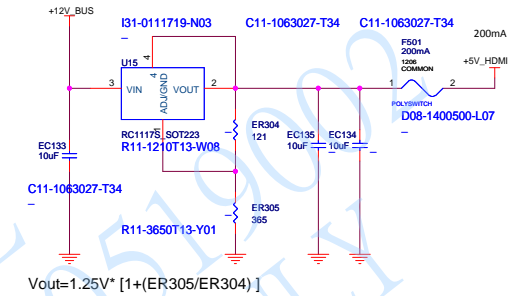


LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



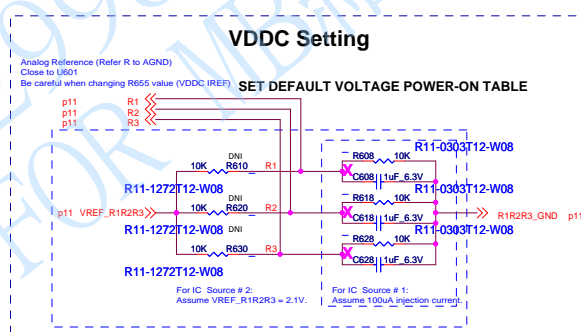
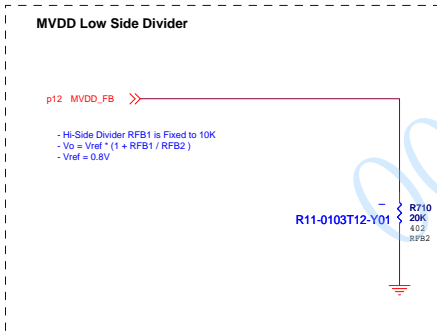
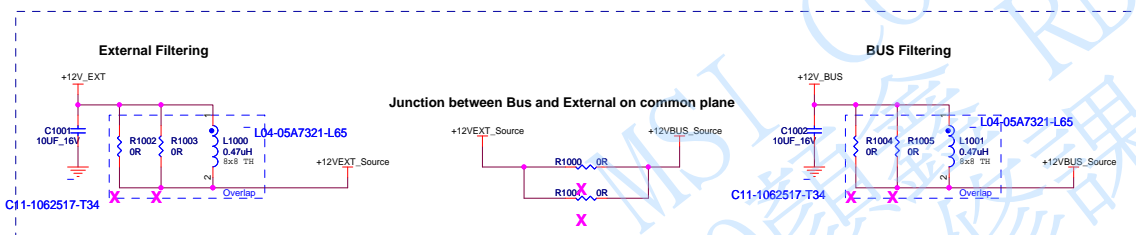
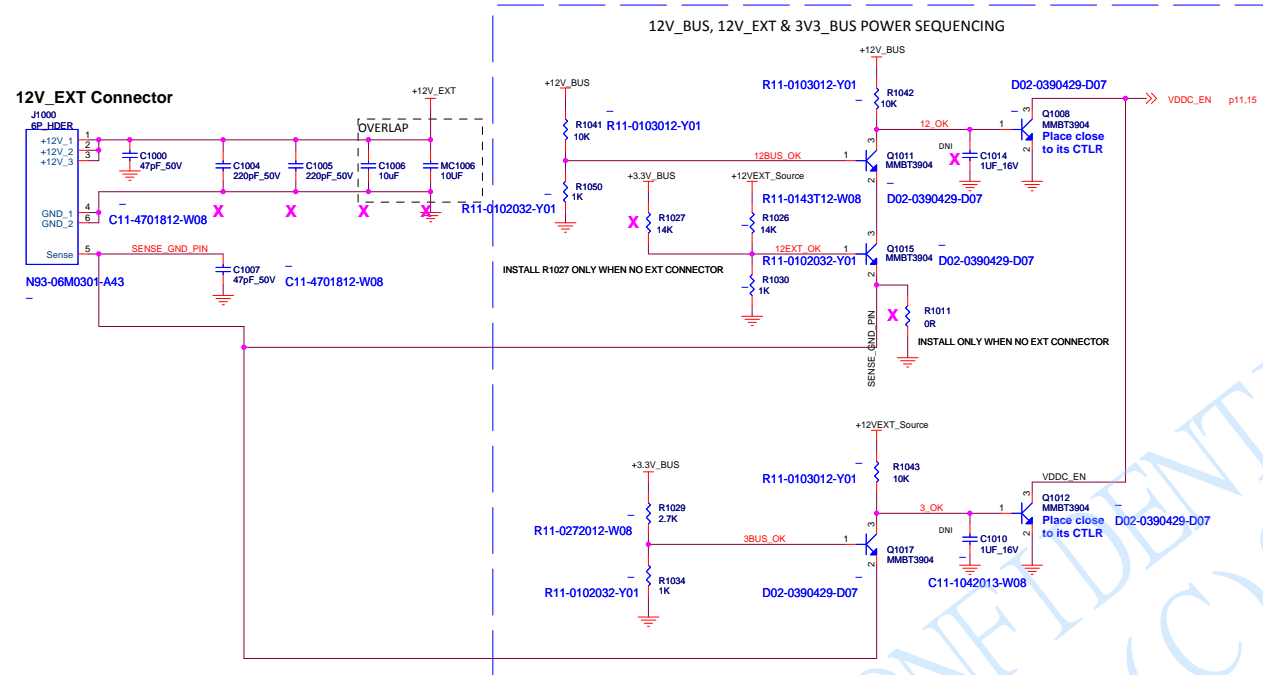
1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA

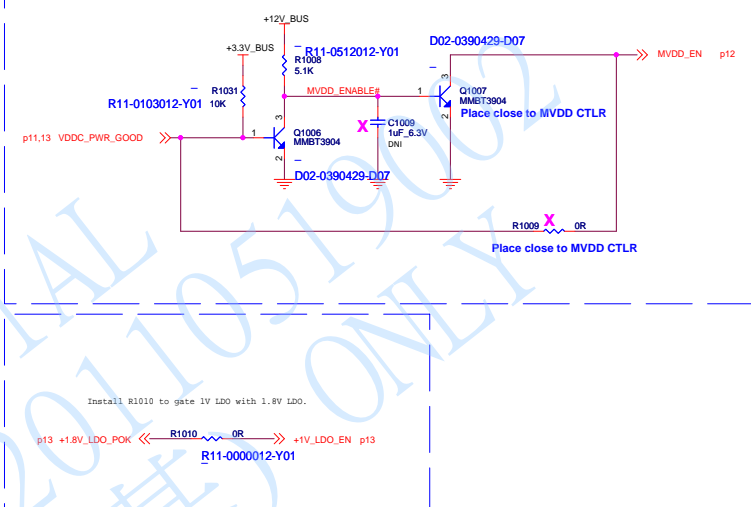


Change +5V REGULATOR to A1117
copy from MS-V208-5.0

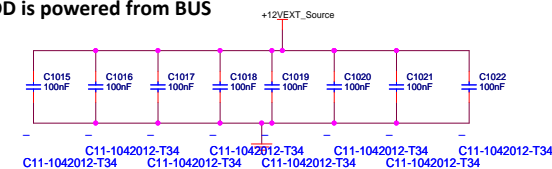
(16) Power Management - Power Gating and Dynamic Voltage Control



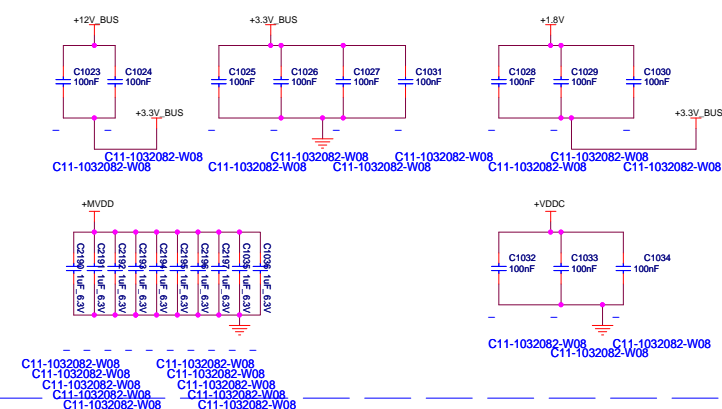
POWER SEQUENCING CIRCUIT



TO BE PLACED ALONG +12VEXT_Source between VDDC and MVDD ONLY when MVDD is powered from BUS




Stitching Caps:

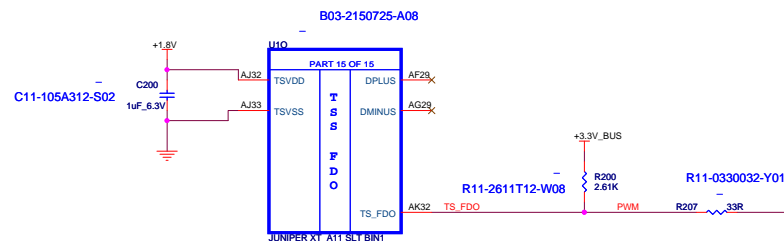


CONFIDENTIAL & PROPRIETARY TO ADVANCED MICRO DEVICES INC.
72007 Advanced Micro Devices

This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims any responsibility for any consequences resulting from use of the information included herein.

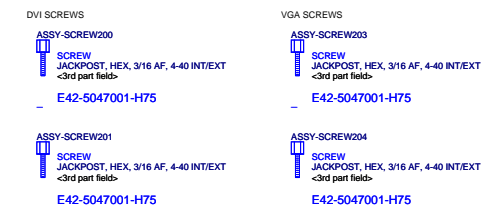
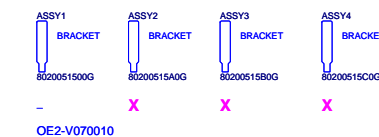
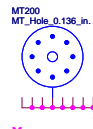
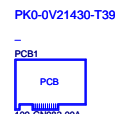
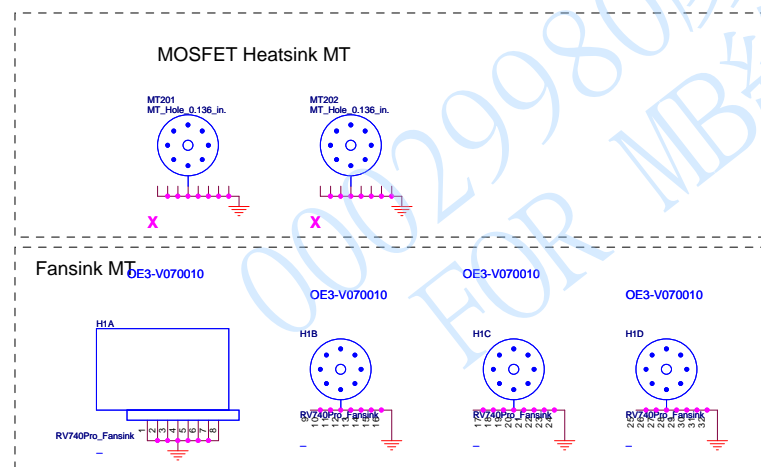
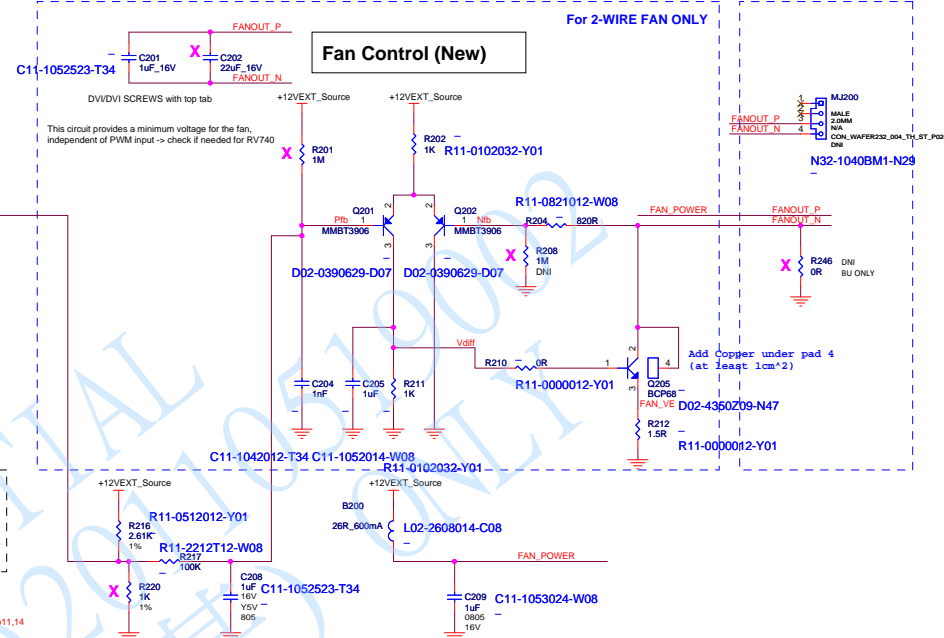
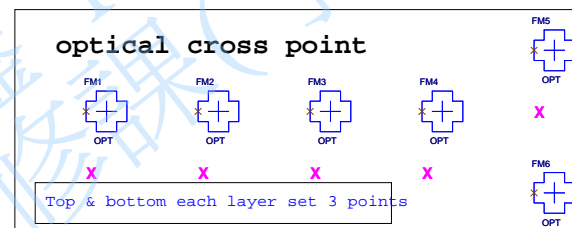
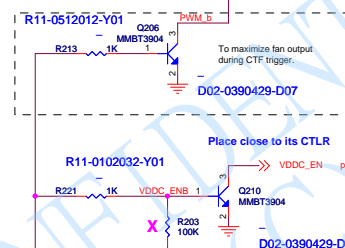
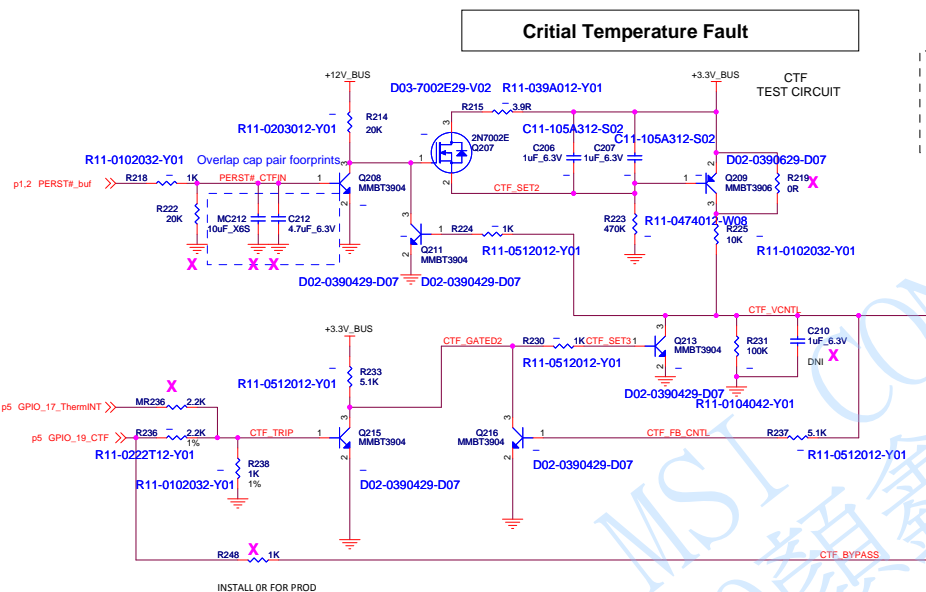
Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario			
Date: Friday, January 07, 2011		Rev P04	
Sheet 14 of 18			

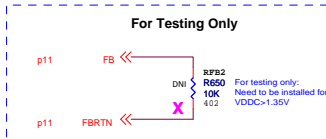
(19) Mechanical and Thermal Management

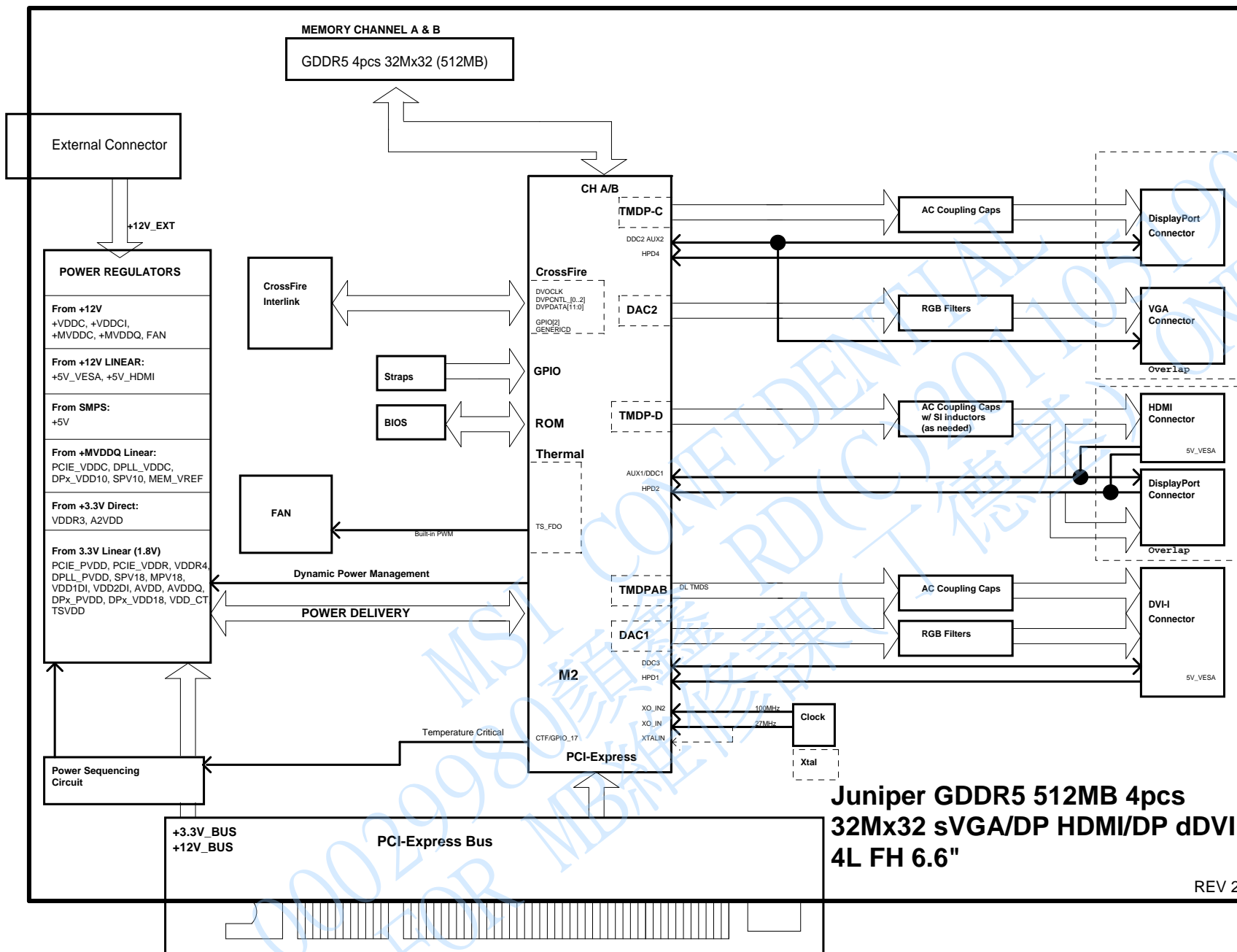


Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.







**Juniper GDDR5 512MB 4pcs
32Mx32 sVGA/DP HDMI/DP dDVI
4L FH 6.6"**

REV 2

<div>AMD</div>			Title		Schematic No.		Date:				
			RH Juniper G5 512MB 4pcs 32Mx32 VGA/DP+HDMI/DP+DVI 4L FH 6.6"		105-C099xx-00B		Friday, January 07, 2011				
			REVISION HISTORY					NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.		Rev P04	
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION								
00	00A	2009/12/12	RH Juniper G5 512MB 4pcs 32Mx32 VGA/DP+HDMI/DP+DVI 4L FH 6.6" sCF - based on B740 M2 4L								
MS-V214	3.0	2011/01/04	01. PAGE 05 removed U2 & relation for DP DNI 02. PAGE 06 stuff DAC2 03. PAGE 07 delete DUAL ANALOG SWITCH (U1802) 04. PAGE 08 delete Co-Lay DP port 05. PAGE 11 changed to Power Stage MOSFET 06. PAGE 11 removed Low-Side gate damping resistor 07. PAGE 11 removed co-lay choke & changed choke footprint 08. PAGE 11 changed 12V input CAP & removed partial 12V input MLCC 09. PAGE 11 changed Output CAP 10. PAGE 12 changed PWM IC to ANPEC/APW8720AKAE-TRG 11. PAGE 12 changed choke footprint 12. PAGE 12 stuff snuber 13. PAGE 12 changed MOFET to NIKO 0903 vs 0603 14. PAGE 12 changed 12V input CAP & removed partial 12V input MLCC 15. PAGE 12 changed Output CAP 16. PAGE 12 add R716 17. PAGE 13 changed LDO to I31-7103S02-N03 18. PAGE 13 combine +5V_HDMI & +5V_VESA use A1117 reg. 19. PAGE 14 change 12V input filter choke 20. PAGE 15 change FAN housing to 4pin 21. PAGE 15 add optical cross point & HDMI Fee symbol								
										