Advanced Micro Devices Inc.
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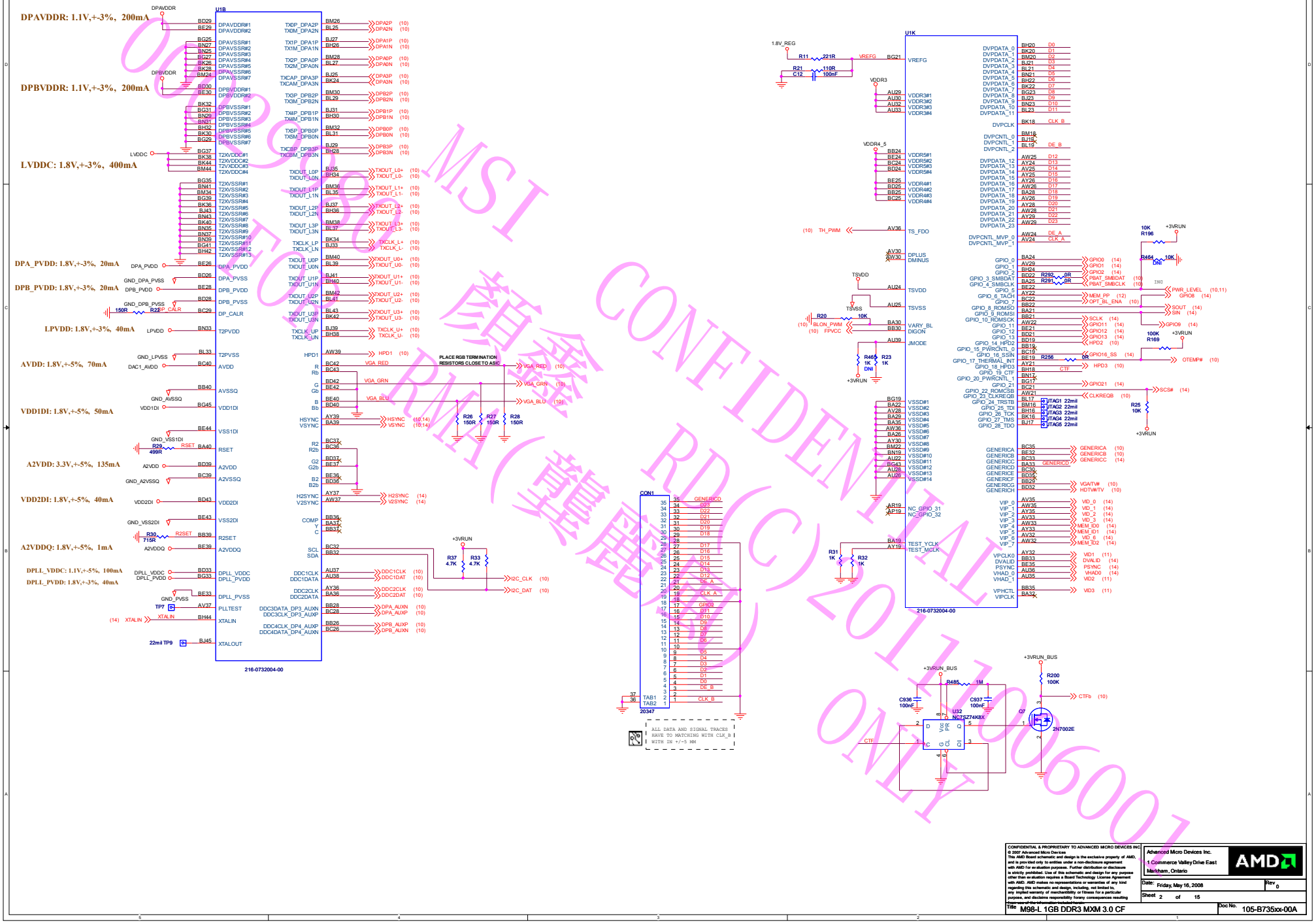
Markham, Ontario

Date:	Wednesday, May 14, 2008
Rev	0
Sheet	1 of 15
Title	M98-L 1GB DDR3 MXM 3.0 CF
Doc No.	105-B735xx-00A



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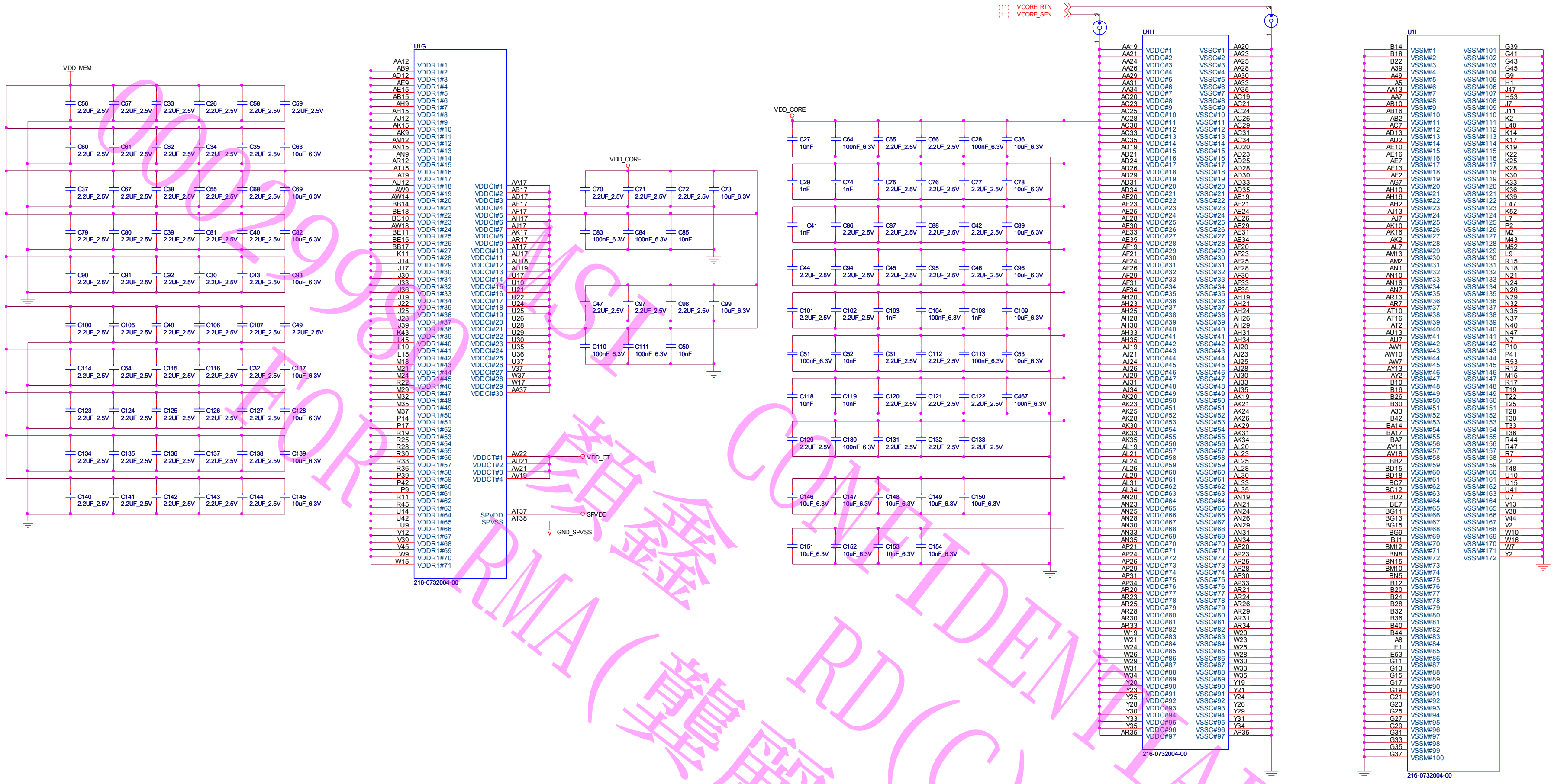

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Title: M98-L 1GB DDR3 MXM 3.0 CF

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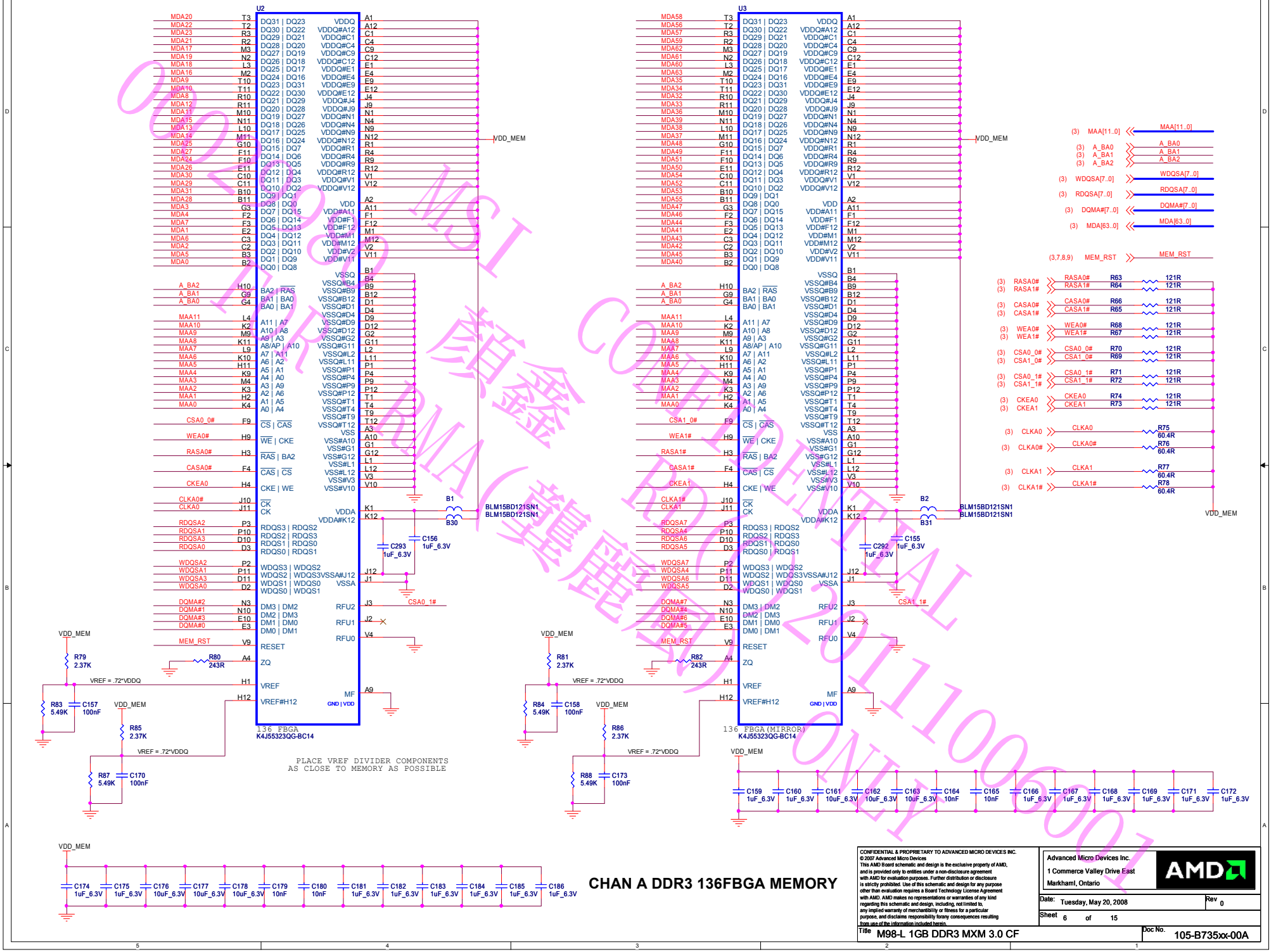

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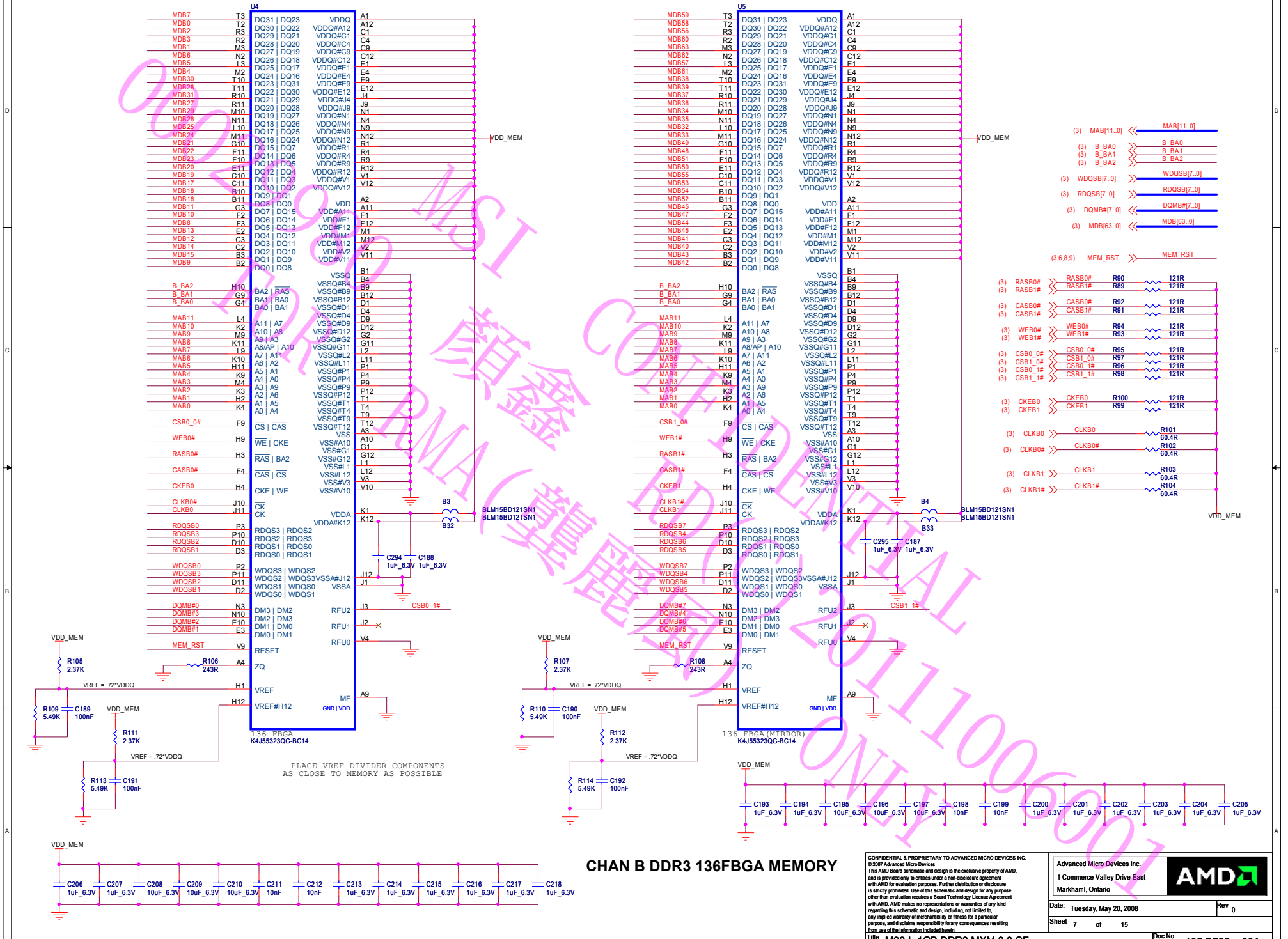

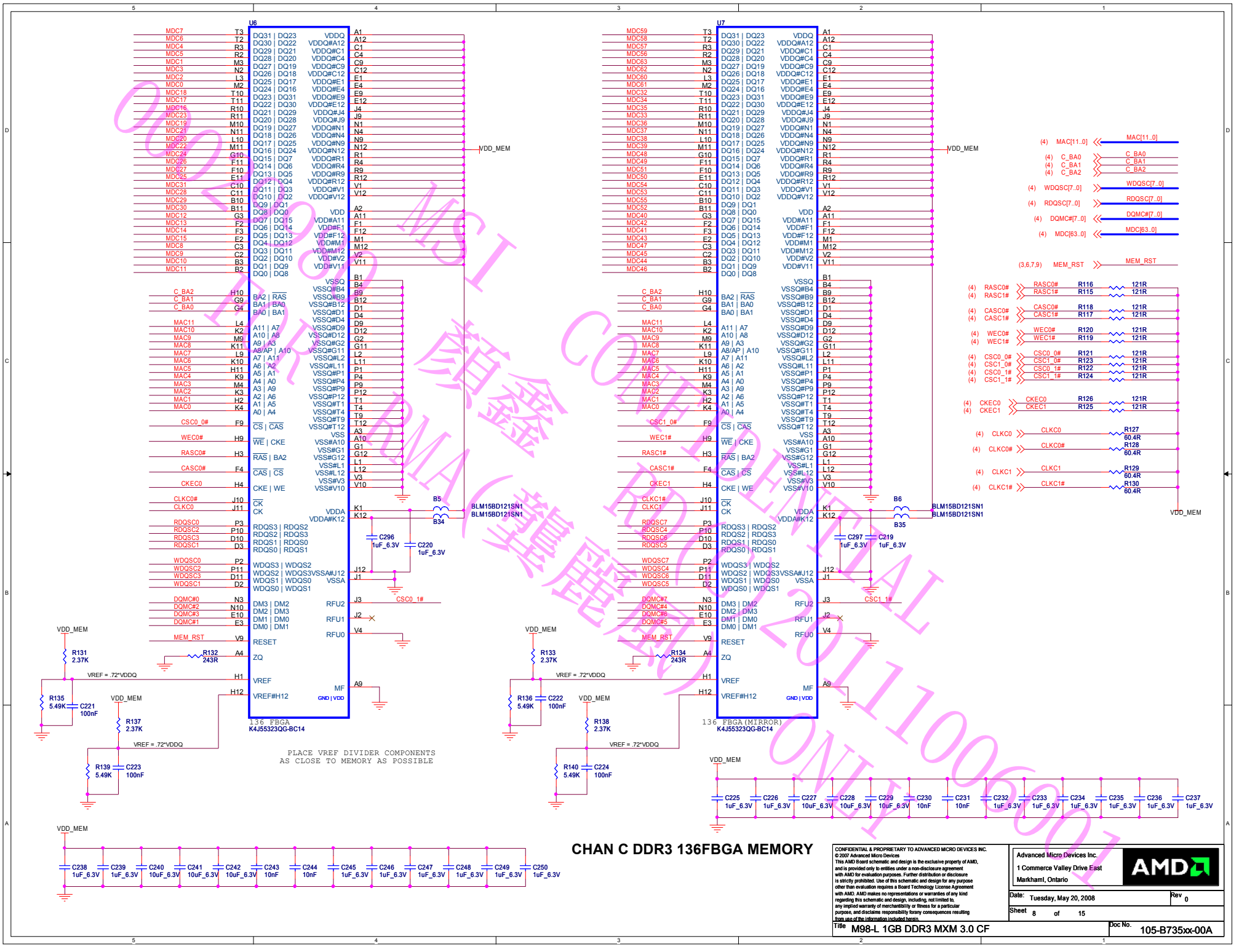
U6
U7
136 FBGA
K4J55323QG-BC14
136 FBGA (MIRROR)
K4J55323QG-BC14
VDD_MEM
PLACE VREF DIVIDER COMPONENTS
AS CLOSE TO MEMORY AS POSSIBLE
CHAN C DDR3 136FBGA MEMORY
M98-L 1GB DDR3 MXM 3.0 CF
105-B735xx-00A
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario
Date: Tuesday, May 20, 2008
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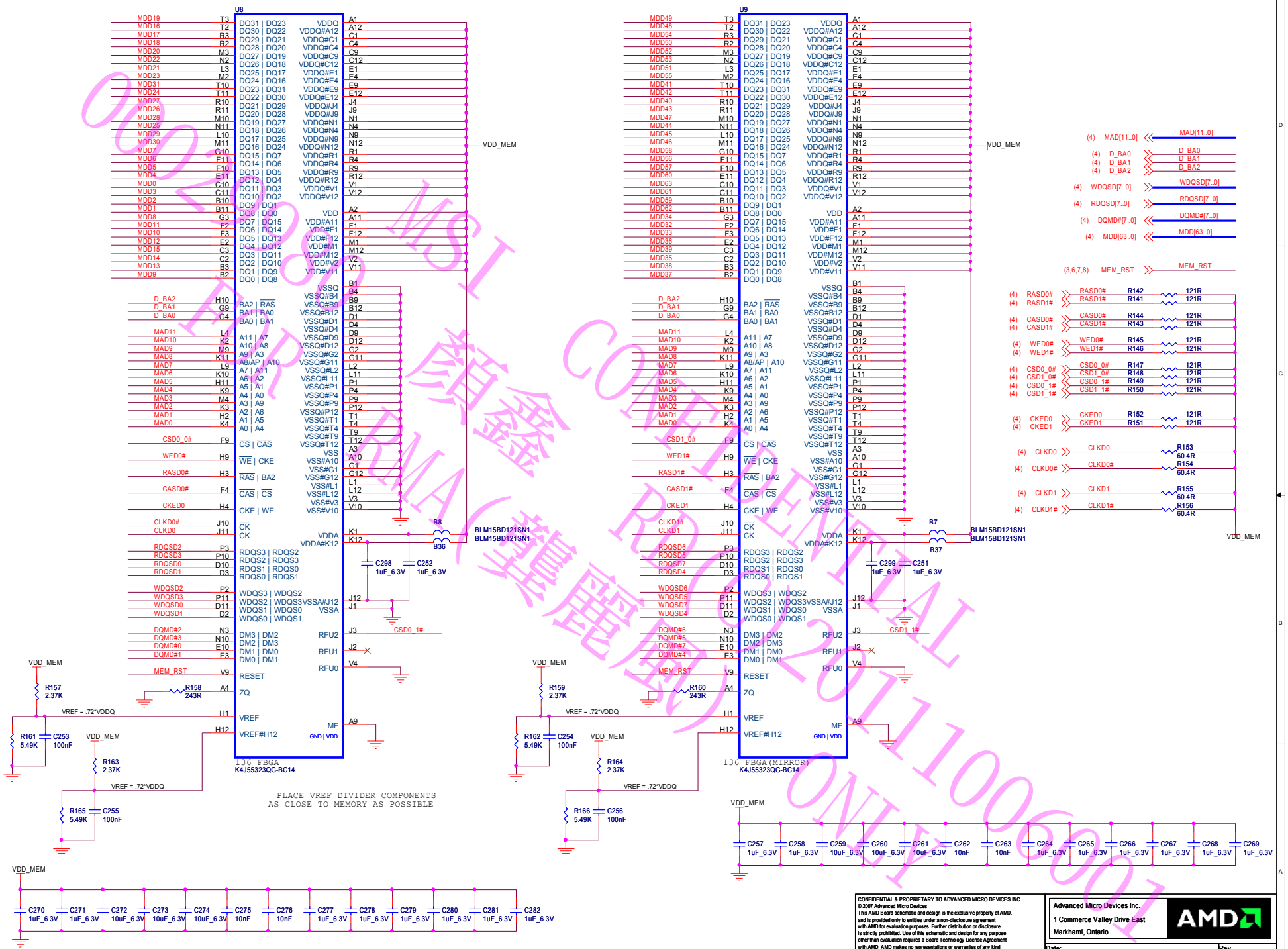

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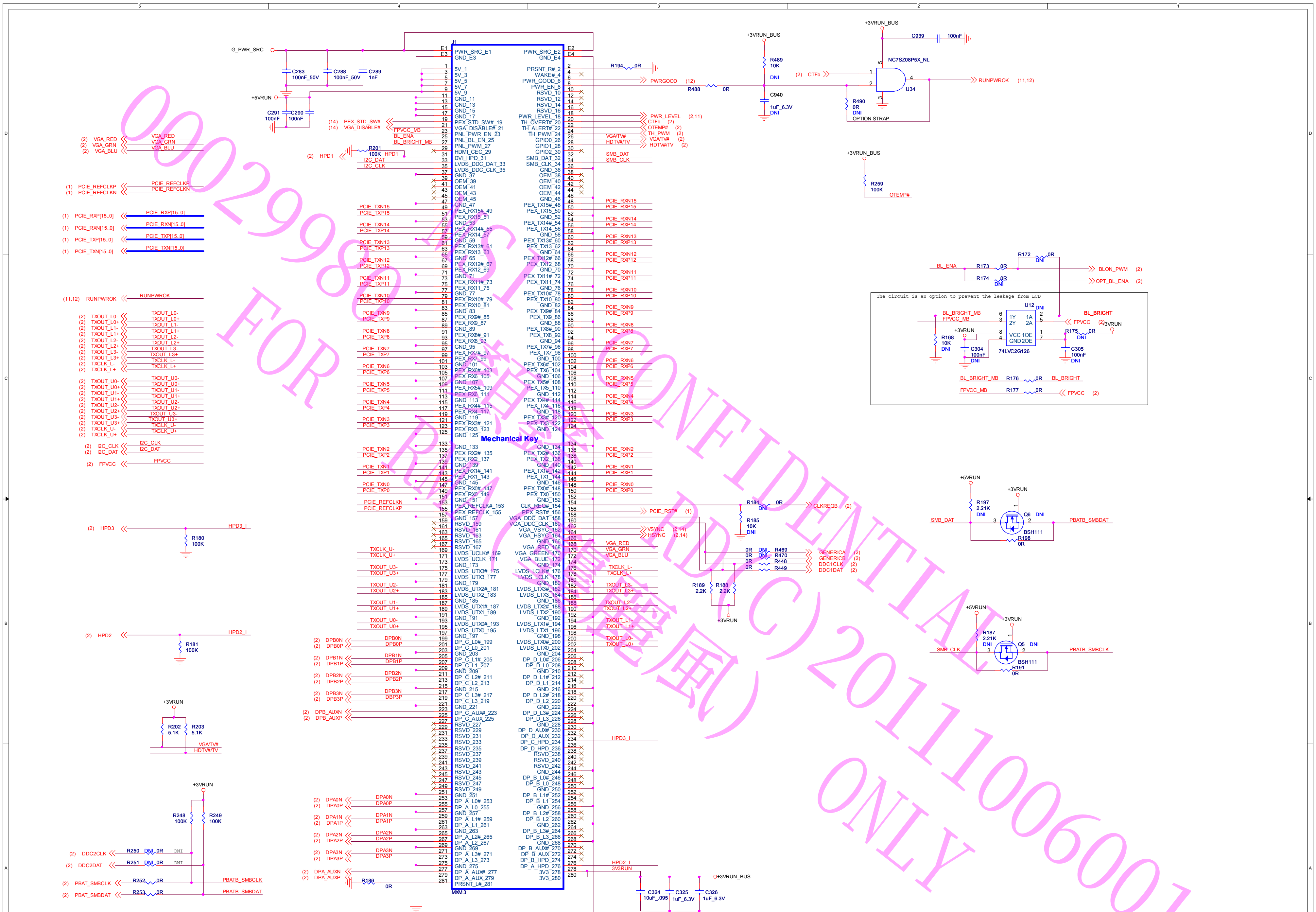
Doc No. 105-B735xx-00A



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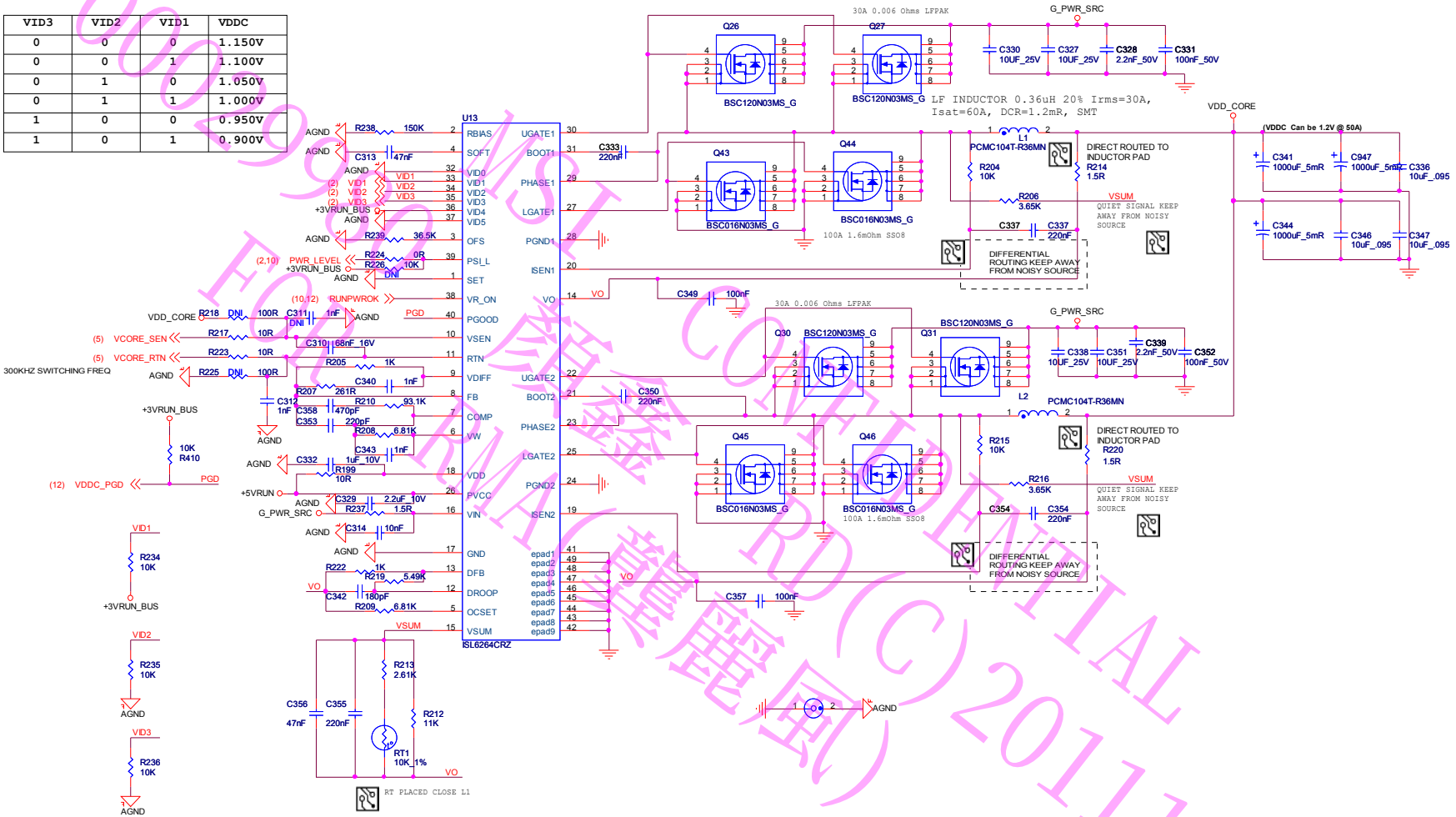
GPU1 CORE REG

CORE PWM TWO PHASE REGULATOR @ 50A

VID3	VID2	VID1	VDDC
0	0	0	1.150V
0	0	1	1.100V
0	1	0	1.050V
0	1	1	1.000V
1	0	0	0.950V
1	0	1	0.900V



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Title	M98-L 1GB DDR3 MXM 3.0 CF
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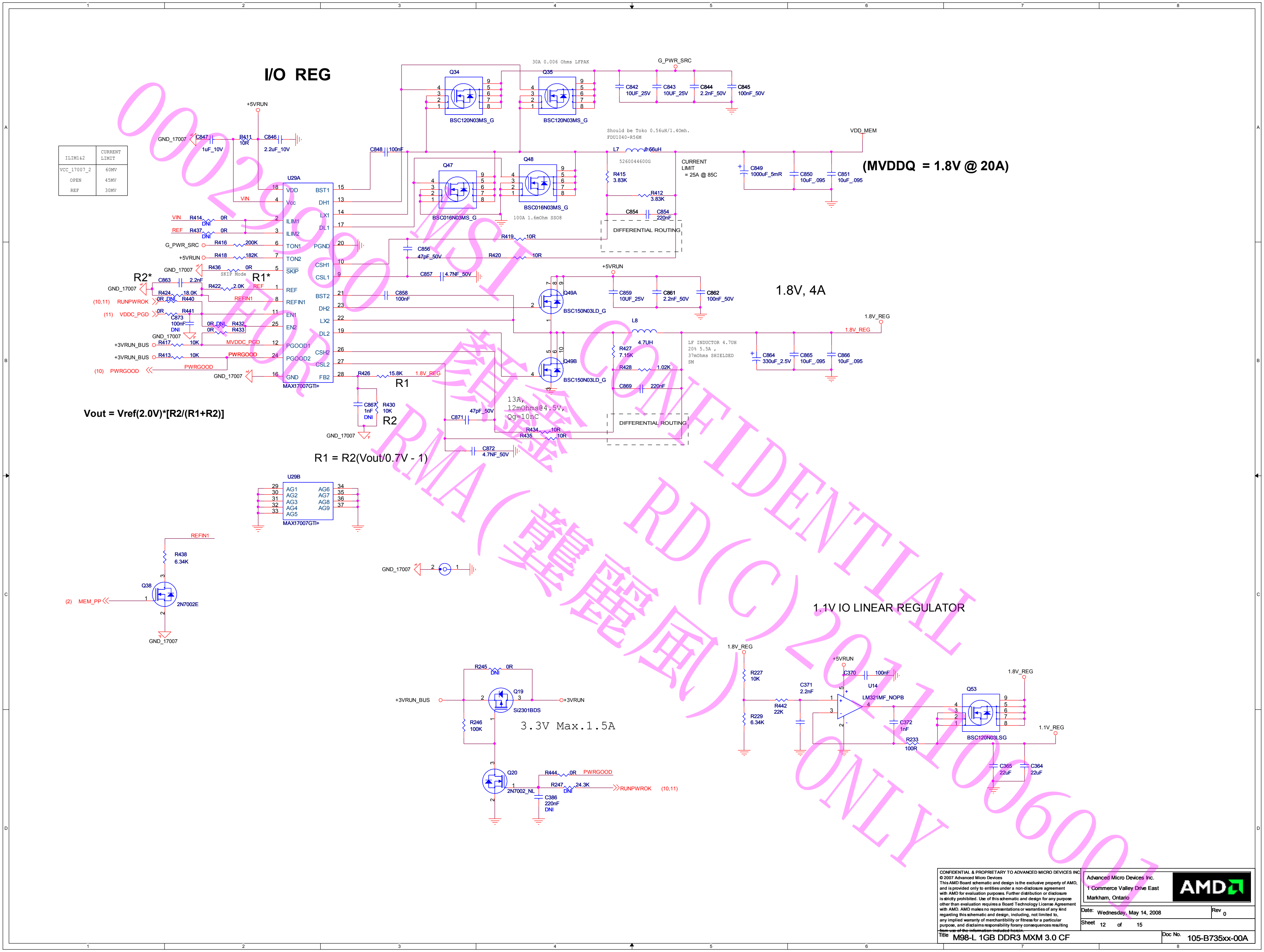
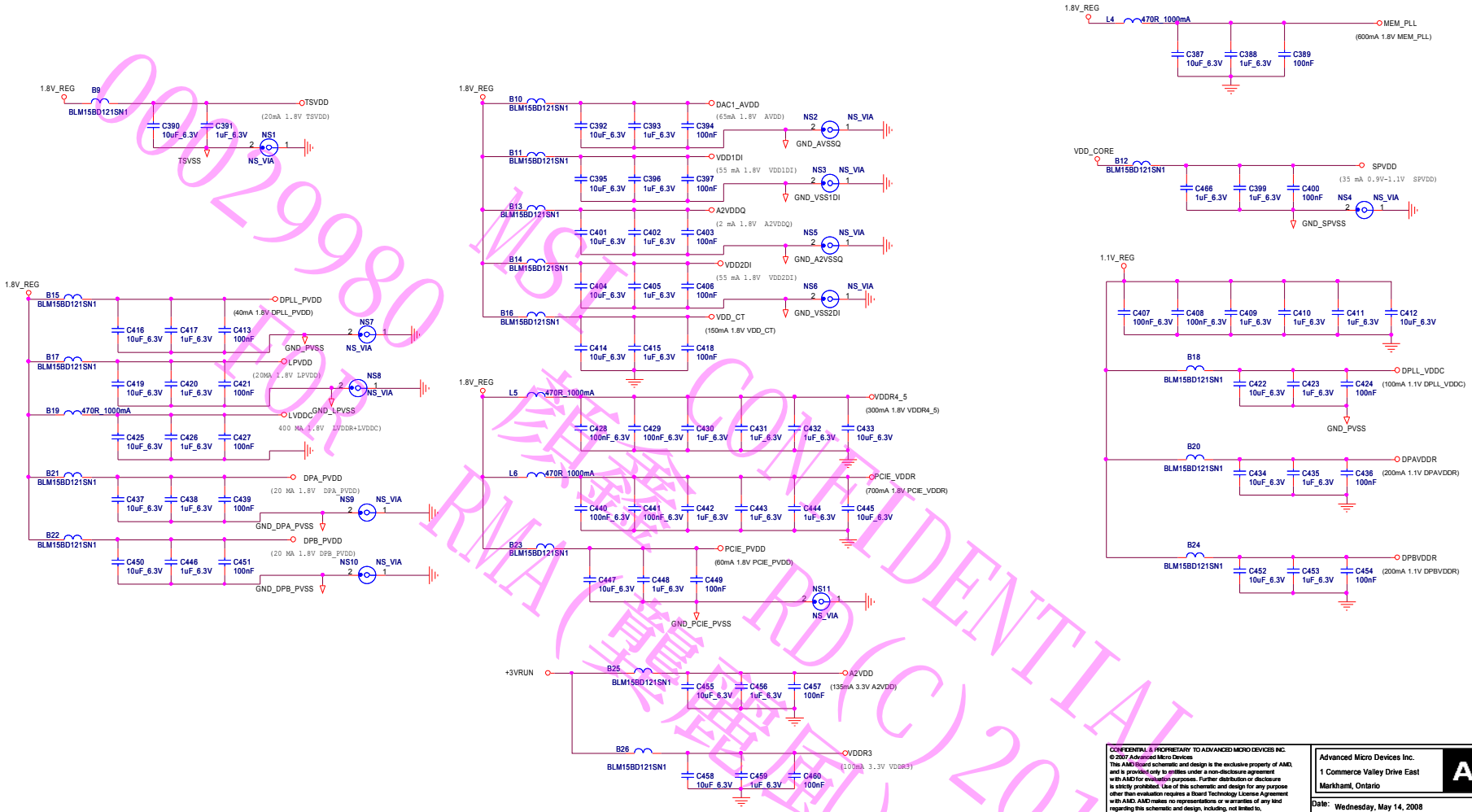
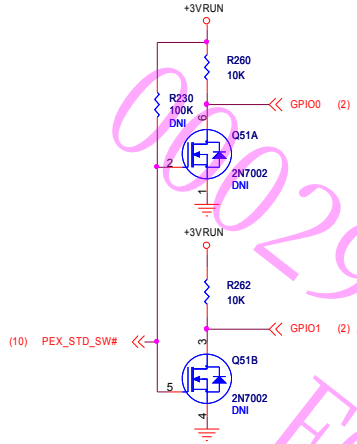
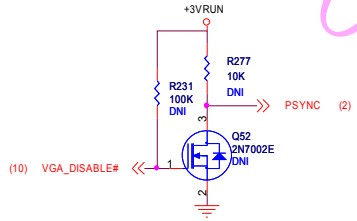
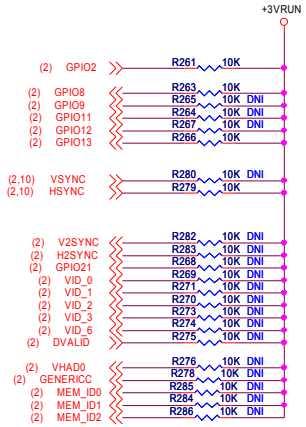
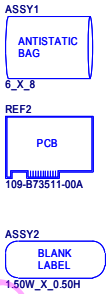








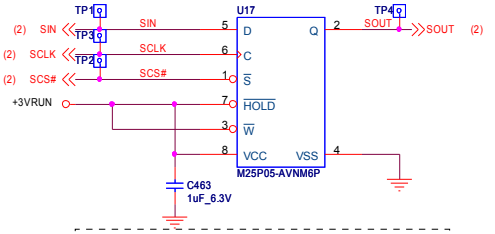




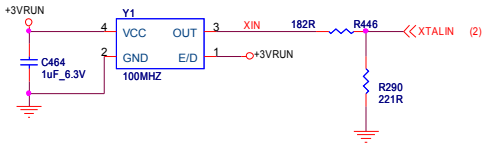
Pin Straps description

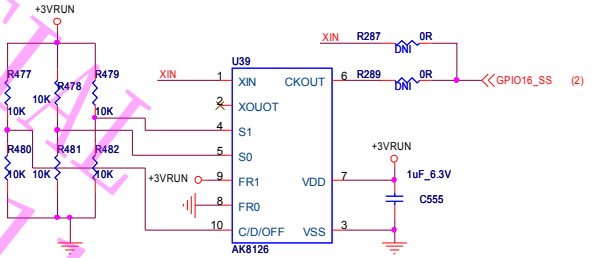
Strap Name			Default Value
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
DEBUG_ I2C_ENABLE	GPIO6	Internal use only. THIS PAD HAS AN INTERNALPULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except GND at reset.	0
MSI_DIS	VID_1	Disable Message Signaled Interrupt is both a ROM strap and a pin strap. The pin strap is only applicable if a BIOS ROM is not present.	0
AUDIO_EN	GPIO8	Enable HD Audio function in the PCI configuration space. 0 - Disable HD Audio 1 - Enable HD Audio	1
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11	GPIO9,13,12,11 (config 3,2,1,0): a> If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM Type: b> If BIOS_ROM_EN = 0, then Config[3:0] defines the Aperture size:Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 64MB 011 = 32MB 100 = 512MB 101 = 1GB 110 = 2GB 111 = 4GB	0100
BIF_CLK_PM_EN	DVALID	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
VIP_DEVICE_STRAP_EN	VSYNC	VSYNC - VIP_DEVICE_STRAP_EN 0: Driver would ignore the value sampled on VHAD_0 during reset. 1: Driver would use the sampled value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (0 indicates yes, 1 indicates no)	0
VIP_DEVICE	VHAD_0	If VIP_DEVICE_STRAP_EN is set to '1', then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to '0', then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
VGA_DIS	PSYNC	PSYNC - VGA DISABLE : 0 – VGA Controller capacity enabled 1 – The device will not be recognized as the system's VGA ontroller	0
HDMI_EN	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0 – No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
RX_PLL_CALIB_BYPASS	GPIO21		0
FORCE_COMPLIANCE_A	VID_3		

FLASH ROM



THEN APPLY ROM LESS DESIGN MUST KEEP TEST PONINTS AND TRACES OUT OF ASIC BALLS FOR DEBUG PURPOSE.





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Doc No. 105-B735xx-00A

5	4	3	2	1

AMD

Title

M98-L 1GB DDR3 MXM 3.0 CF

Schematic No. 105-B735xx-00A

Date: **Monday, May 05, 2008**

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	05/05/08	PROTOTYPE BASED ON B657

5	4	3	2	1