P1070-A01

GF108, 512MB 32Mx32 GDDR5
Desktop, 75W TGP, DL-DVI/VGA/HDMI

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18	Power Supply: NVVDD

2010/11/30 MS-V258-1.0 changed list

Page	Description
08	add a SP-CAP near GPU bottom add screw & HDMI fee & PCB & cross point & Fan changed BKT1 PCB footprint to shorter name
15	deleted 12V BOOST circuit & removed net 12V_FAN & 12V_F contact FAN 12V input directly & add R688 & modified fan control circuit & Fan housing changed to 4 pin & delete INFO ROM circuit & I2CC link to VDD adjust circuit & delete JTAG circuit & delete D501
16	removed net 12V_FAN & delete LDO Option & delete Switcher Option changed 12V Input choke footprint & delete co-lay resistor
17	changed FBVDDQ Output choke footprint & delete co-lay choke
18	changed NVVDD Output choke footprint & delete co-lay choke
17,18	changed Q2 Q3 Q4 Q5 Q6 Q8 Q9 Q10 PCB footprint to shorter name & remove co-lay SMD OS-CON CAP
19	add a new page for VDD adjust circuit

sku	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11070-BASE-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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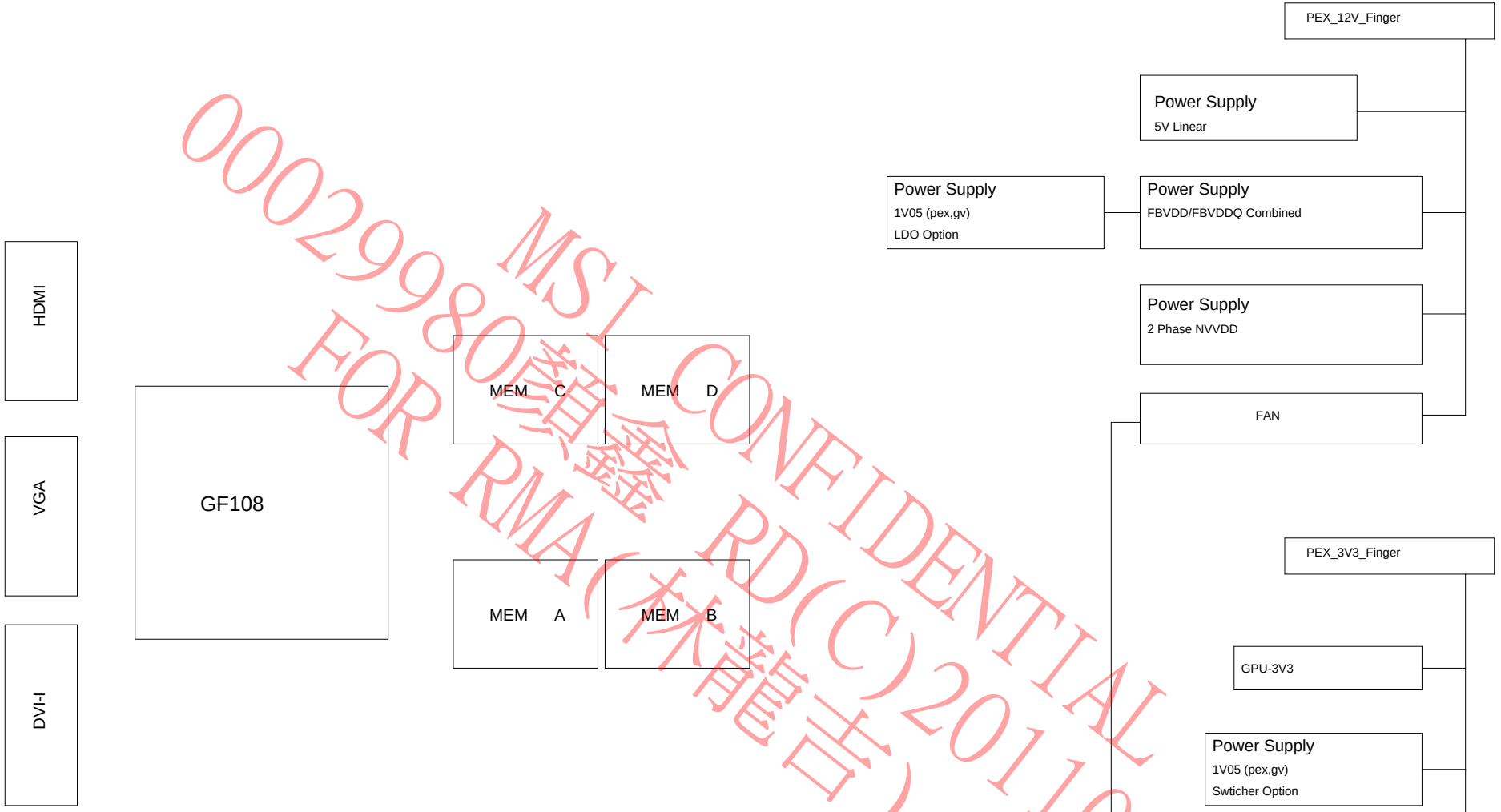
Block Diagram



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PAGE DETAIL	Block Diagram

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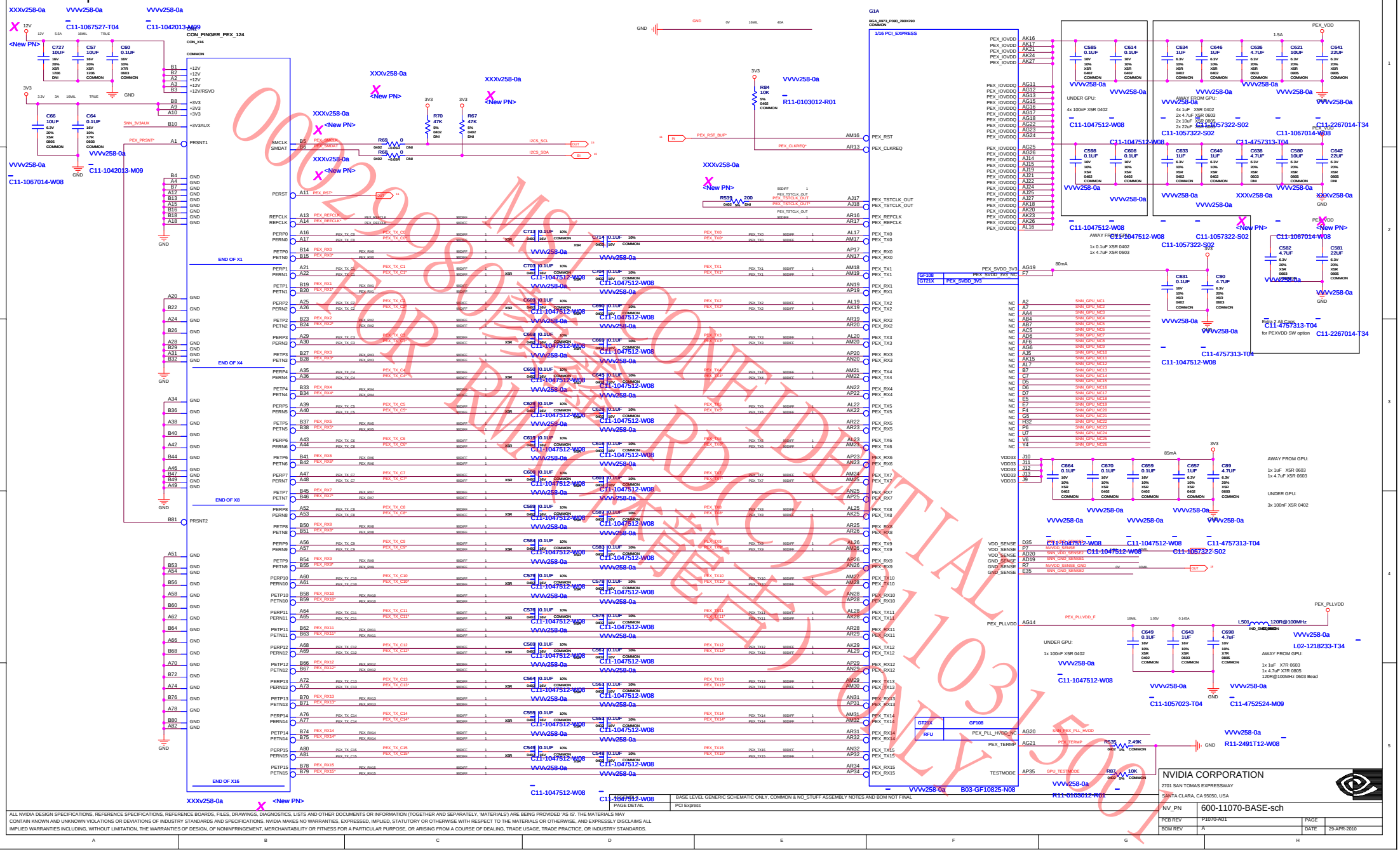

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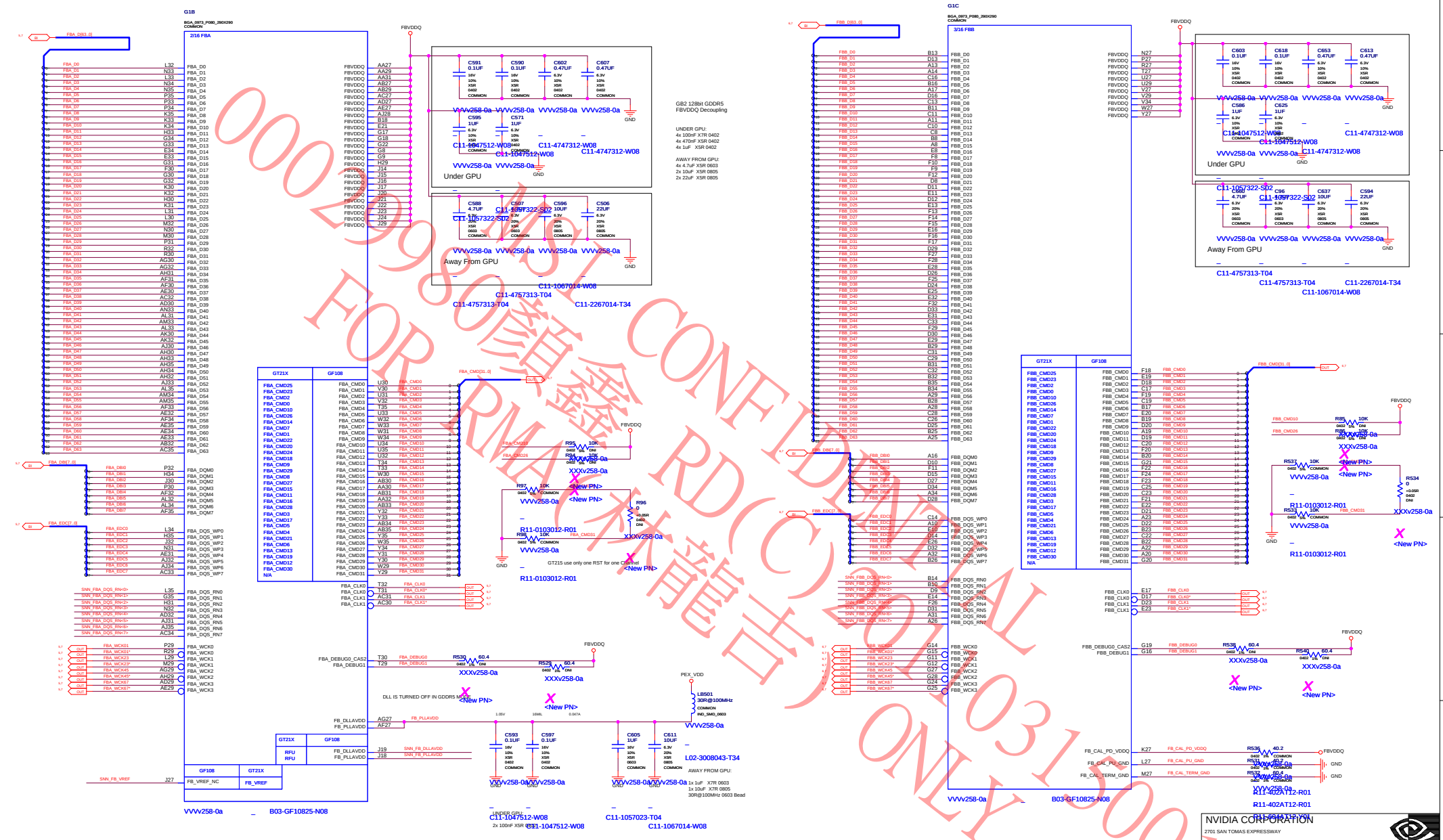
Framebuffer A/B: GPU Section



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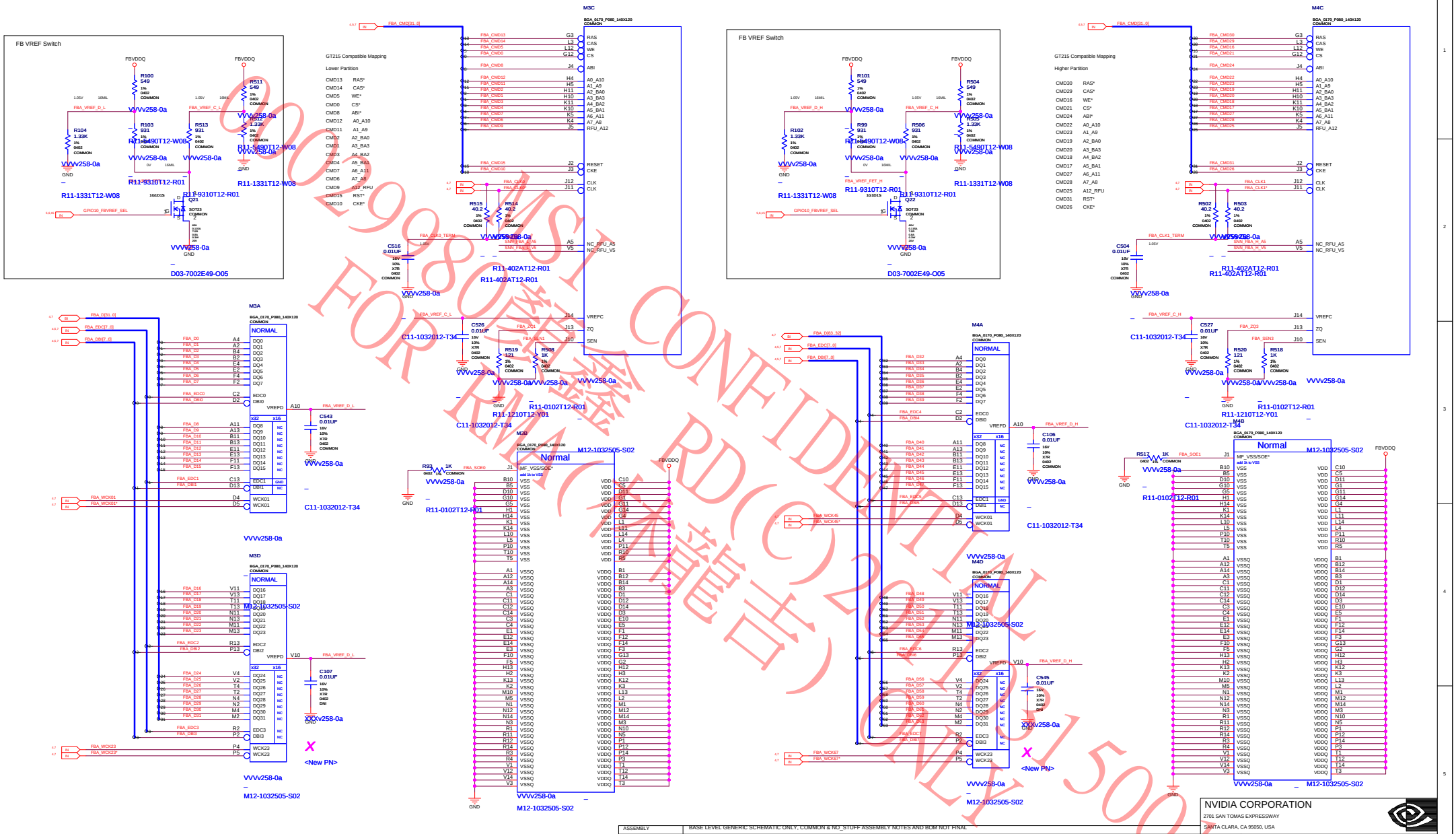
Framebuffer A: Memory Section



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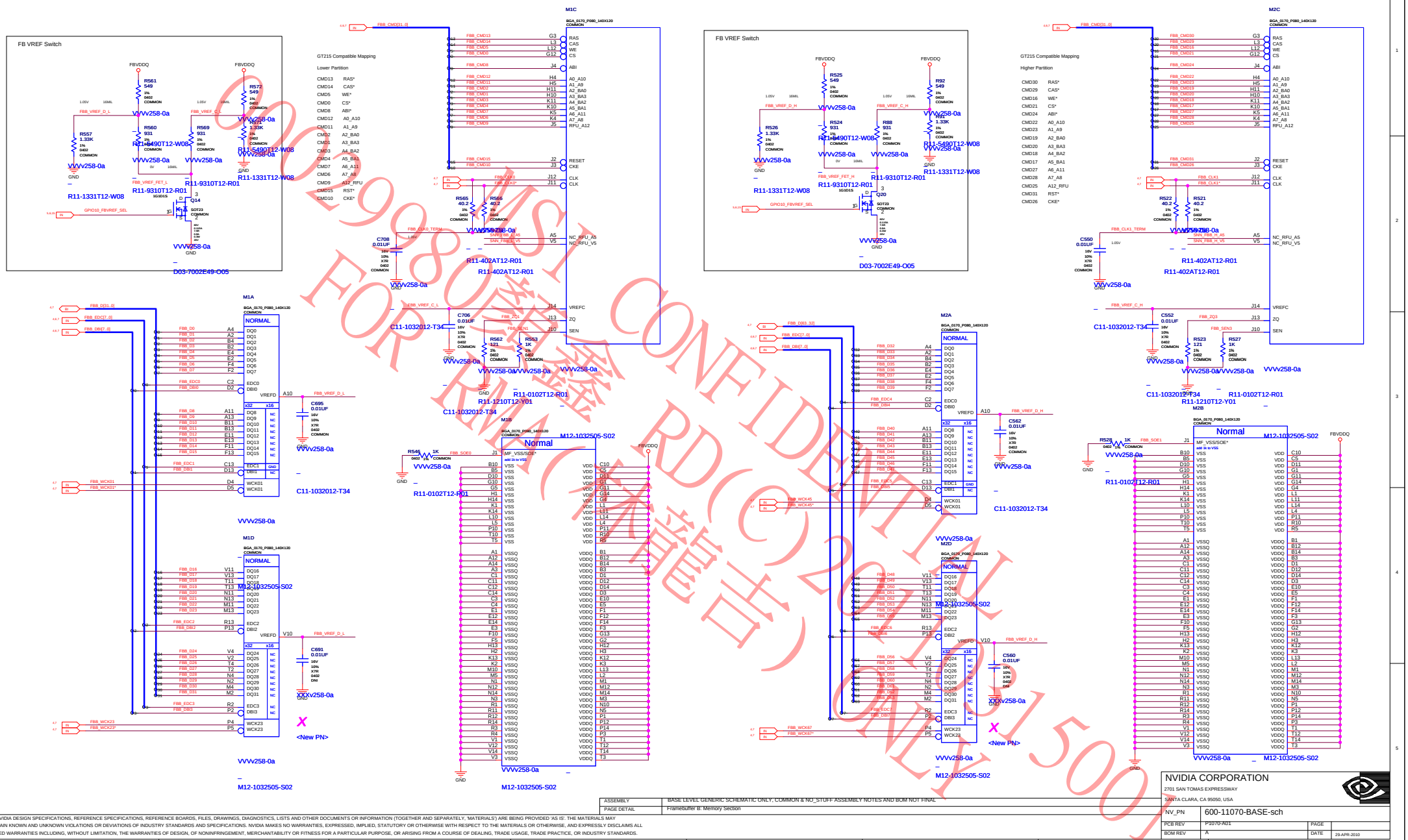
Framebuffer B: Memory Section



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Memory Decoupling, Net Rules

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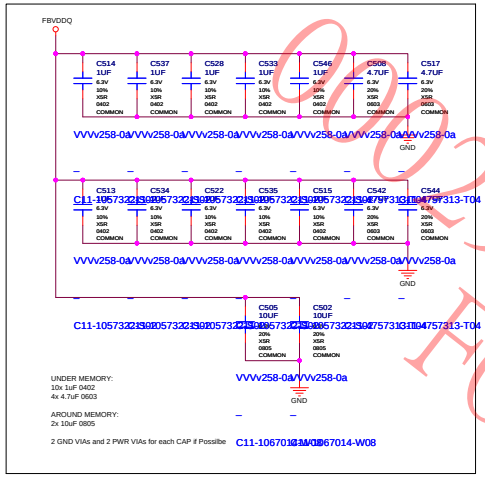

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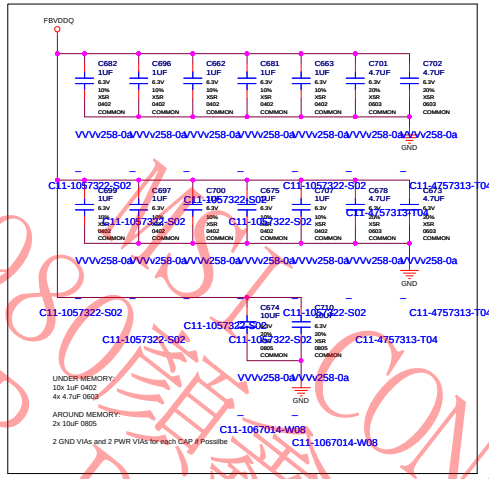

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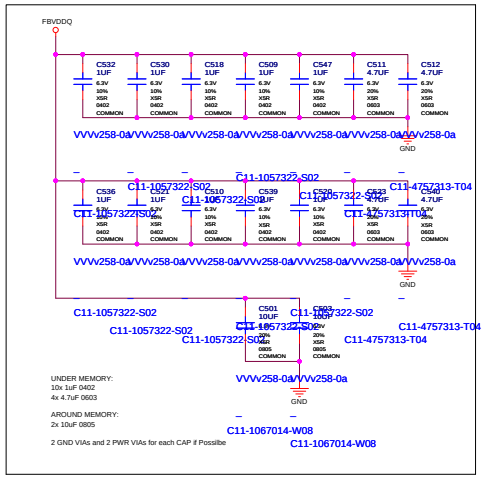

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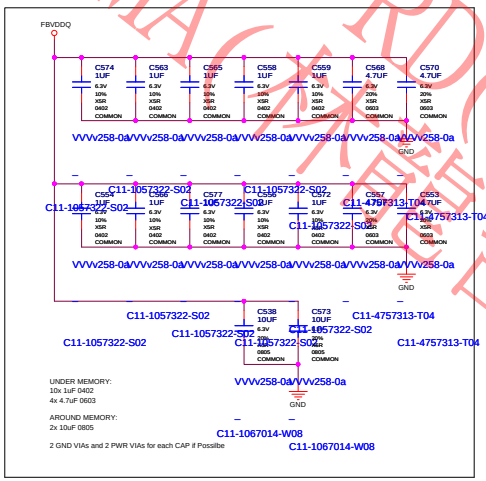
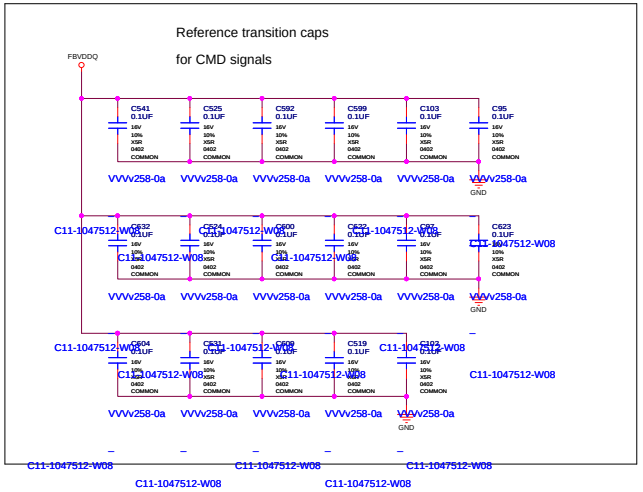
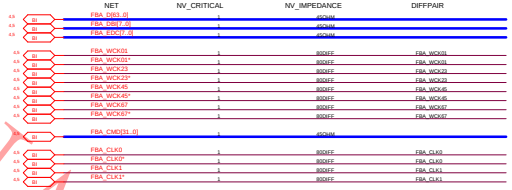


Reference transition caps for CMD signals

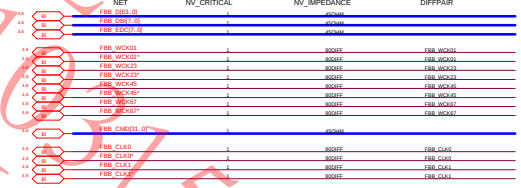


DATA, DBI, EDC, WCK, CMD/ADDR, CLK

NET RULES FOR PARTITION A



NET RULES FOR PARTITION B



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GPU Power and GND, NVVDD Decoupling, THERMAL/MECHANICAL

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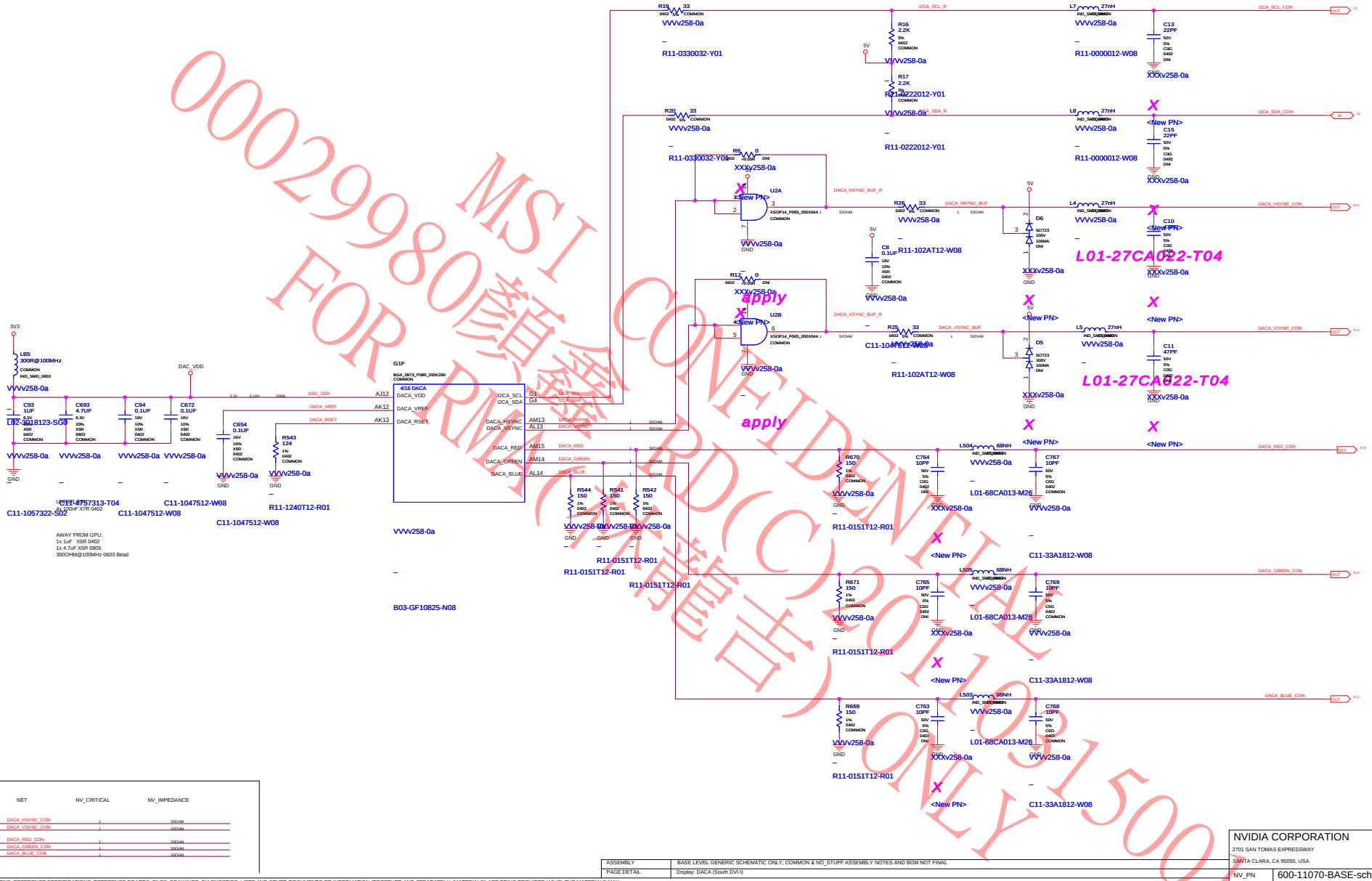
Display: DACA (South DVI-I)



NET	NV_CRITICAL	NV_IMPEDANCE
DACA_HSYNC_CON	1	50OHM
DACA_VSYNC_CON	1	50OHM
DACA_RED_CON	1	50OHM
DACA_GREEN_CON	1	50OHM
DACA_BLUE_CON	1	50OHM

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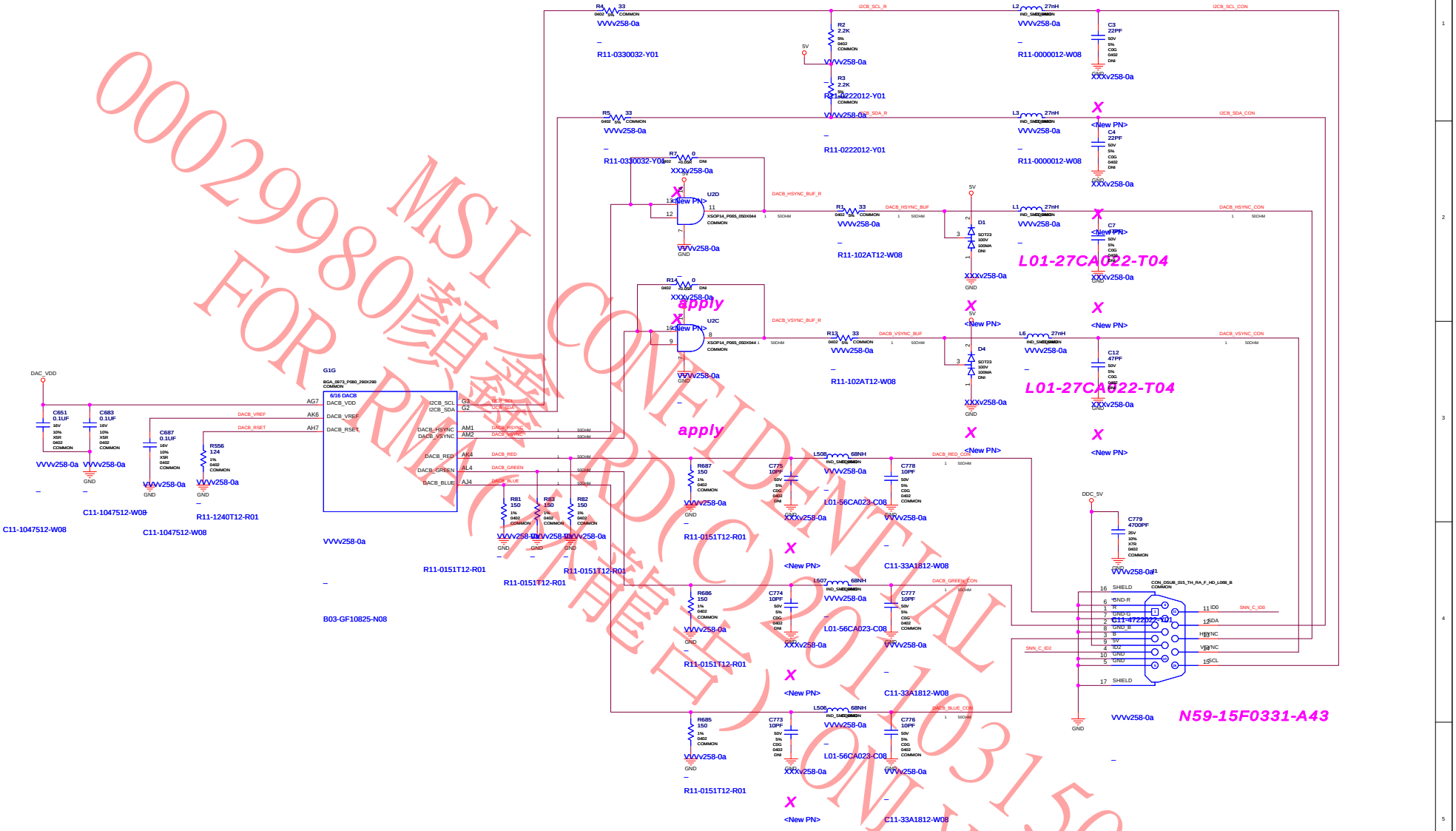

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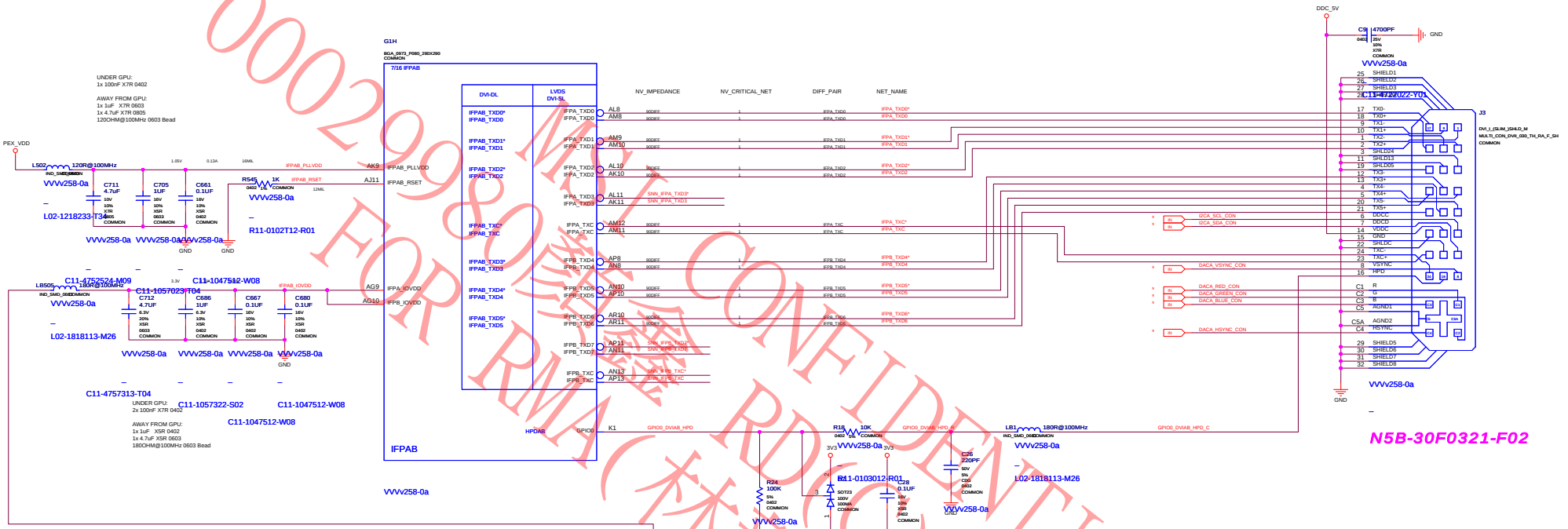
Display: LFPAB (South DVI-I)



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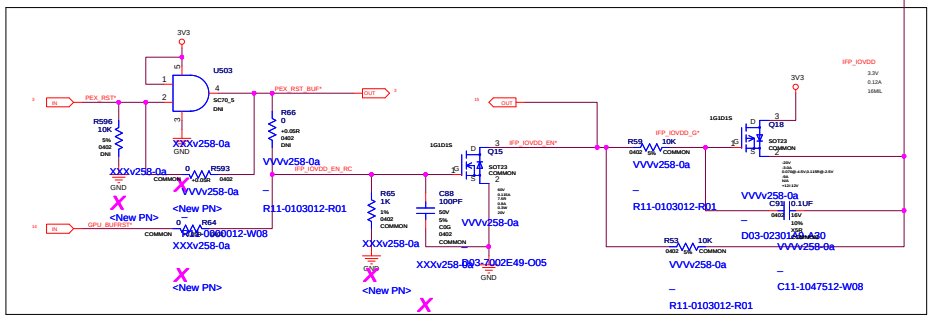

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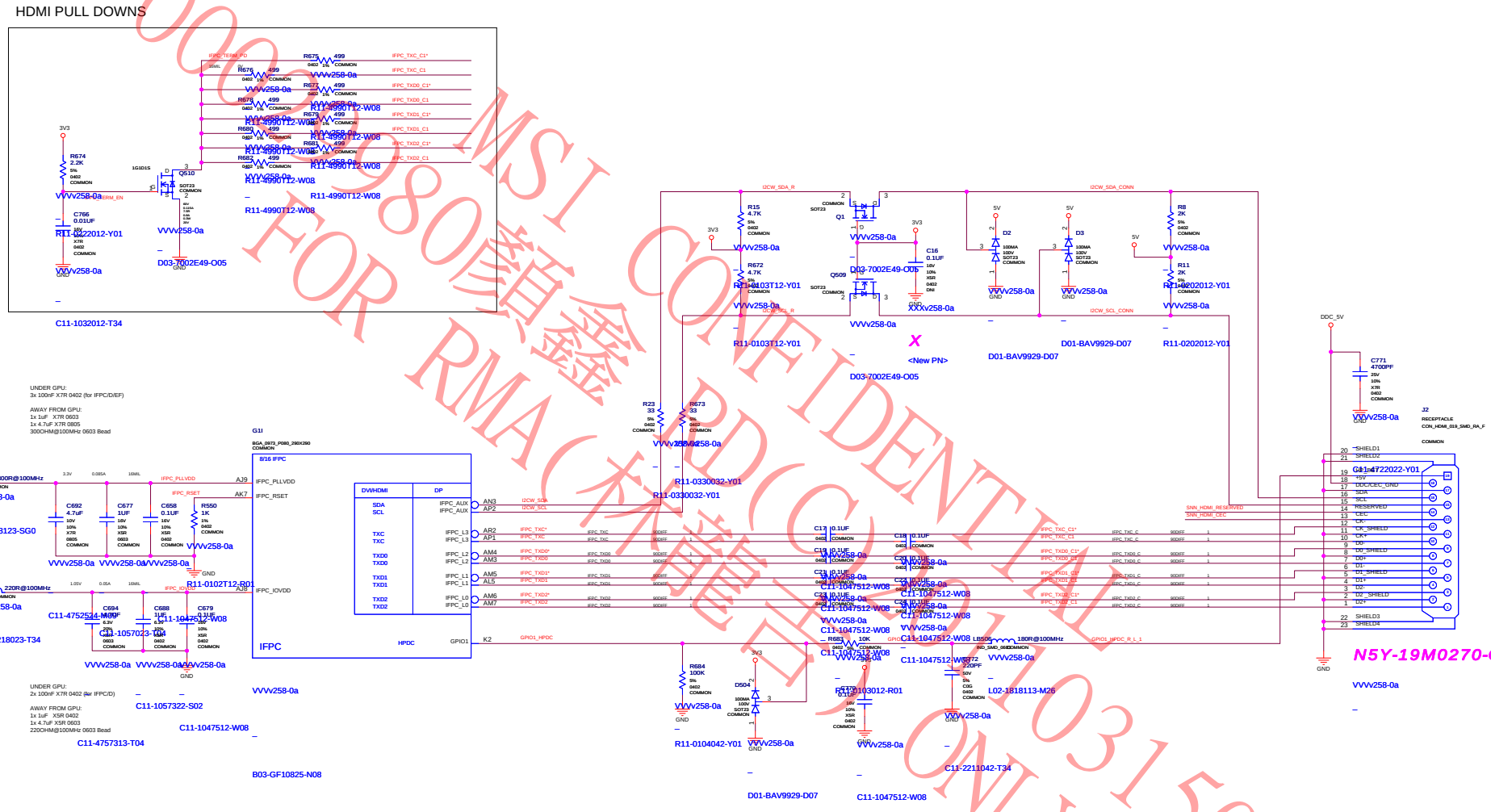
Display: LFPC (North HDMI)



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PAGE DETAIL	Display: LFPC (North HDMI)

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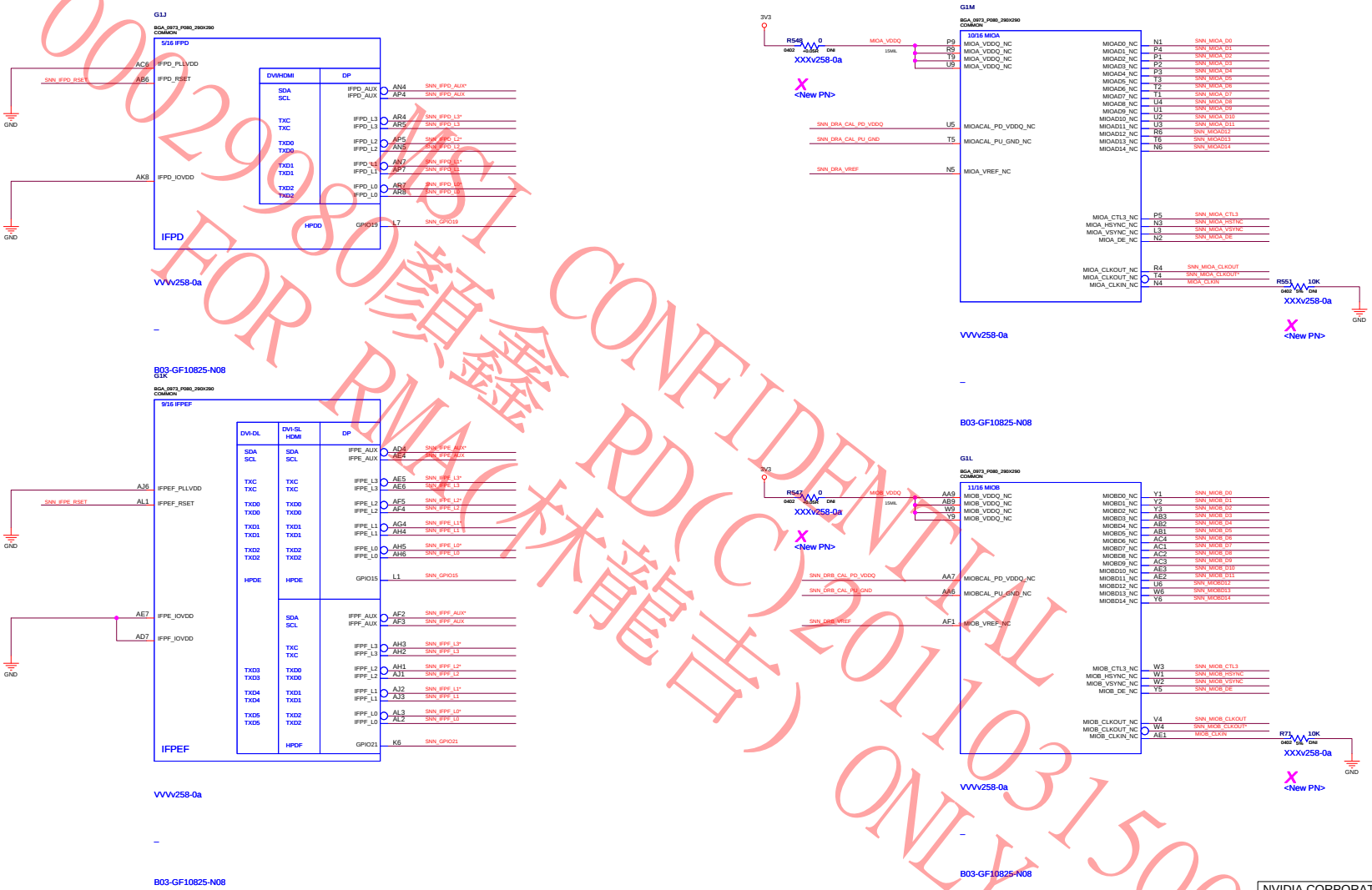
Unused: LFPD/EF, MIOA/B



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ASSEMBLY	
PAGE DETAIL	Unused: LFPD/EF, MIOA/B

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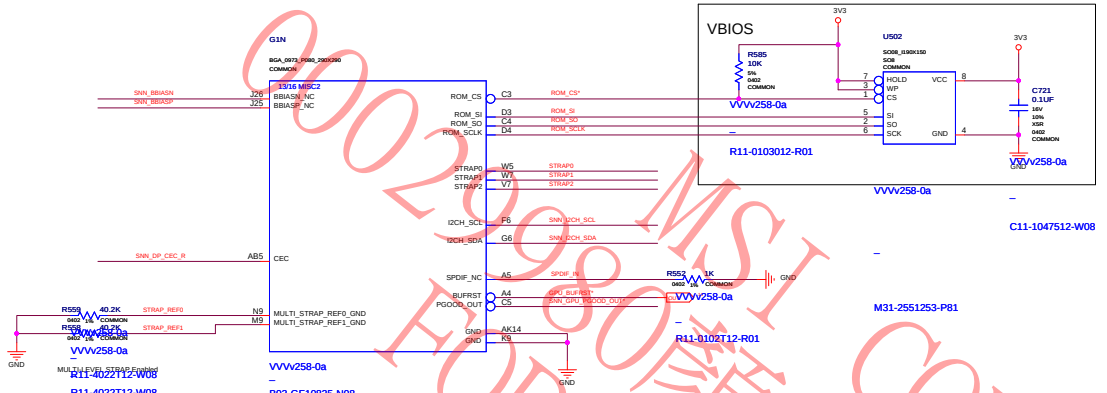
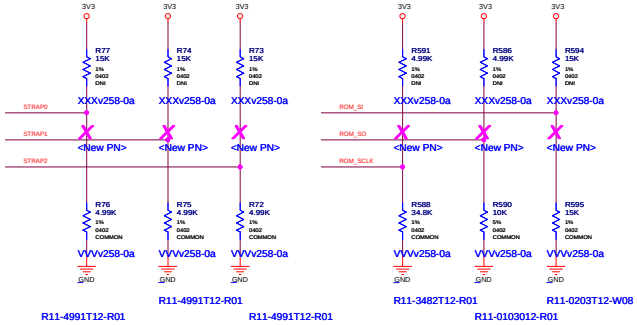
BOM REV	A	DATE	29-APR-2010

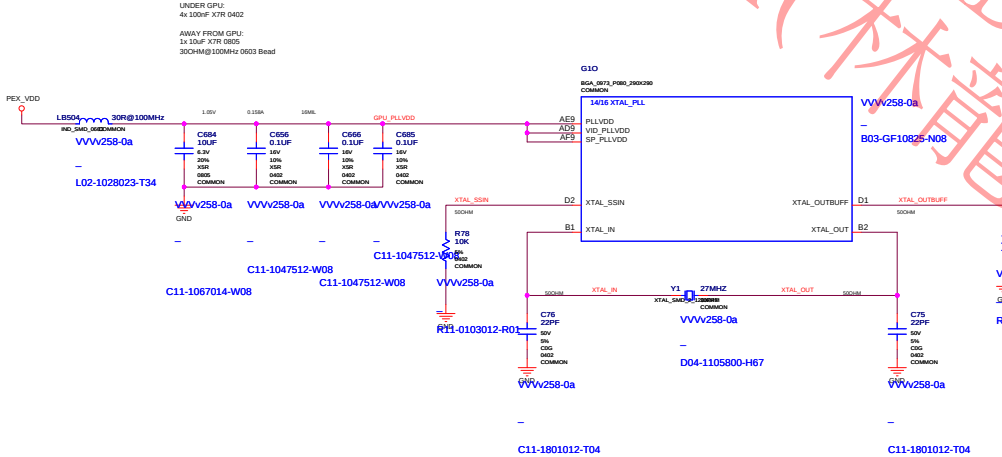
MISC: VBIOS, XTAL, STRAPS





ROM_SI	RAMCFG[3]	0001 32Mx32 128-bit Qimonda	
		0010 32Mx32 128-bit Hynix	=> 15K PD
	RAMCFG[2]	0011 32Mx32 128-bit Samsung	=> 20K PD
	RAMCFG[1]	0101 64Mx32 128-bit Qimonda	
		0110 64Mx32 128-bit Hynix	
	RAMCFG[0]	0111 64Mx32 128-bit Samsung	
ROM_SO	XCLK_417	0 277MHz (Default)	
	FB[0]_BAR_SIZE	0 256MB (Default)	10K PD
	SMB_ALT_ADDR	0 0x9E (Default)	
	VGA_DEVICE	1 VGA Device (Default)	
ROM_SCLK	PCI_DEVID_EXT	0 DID<4>=0	
	SUB_VENDOR	1 BIOS ROM Present	
	SLOT_CLK_CFG	1 Share Ref CLK	45K PD
	PEX_PLL_EN_TERM100	1 Enable	
STRAP0	USER_BIT [3..0]	0000 Default	5K PD
STRAP1	3GIO_PADCFG_LUT_ADR [3..0]	0000 Desktop	5K PD
STRAP2	PCI_DEVID [3:0]	0000 DID: 0x0DE0	5K PD

5k	GND	3V3
10k	0000	1000
15k	0001	1001
20k	0010	1010
25k	0011	1011
30k	0100	1100
35k	0101	1101
45k	0110	1110
	0111	1111



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: VBIOS, XTAL, STRAPS

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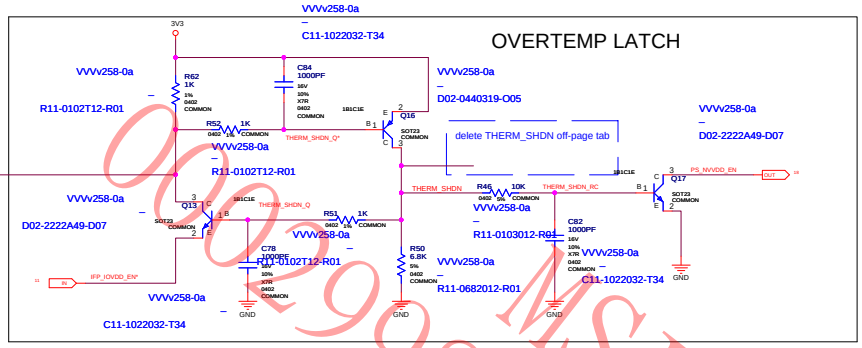
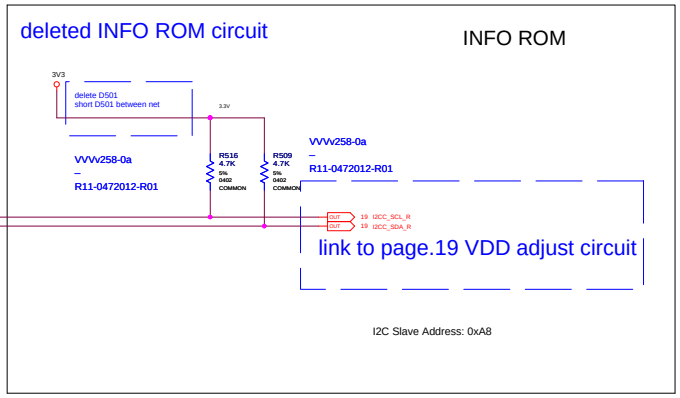
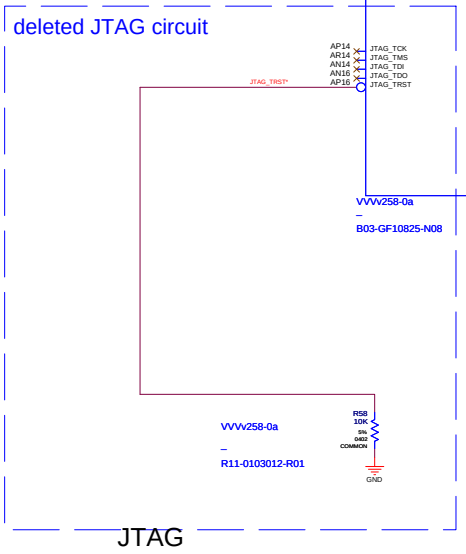
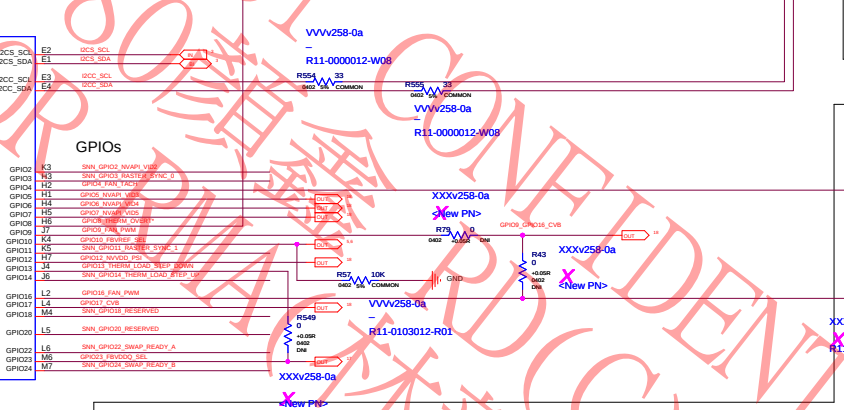
PCB REV	P1070-A01	PAGE	
BOM REV	A	DATE	29-APR-2010

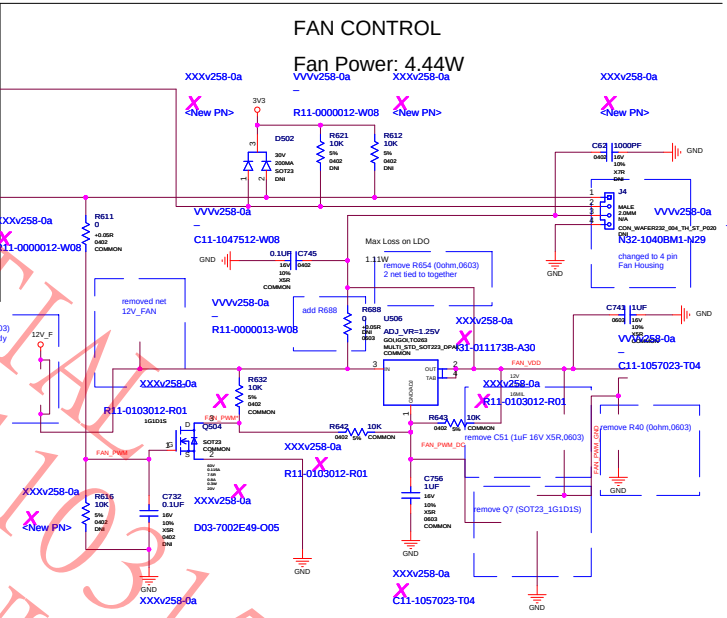
MISC:GPIO, JTAG, INFO ROM, THERMAL LATCH, FAN CONTROL

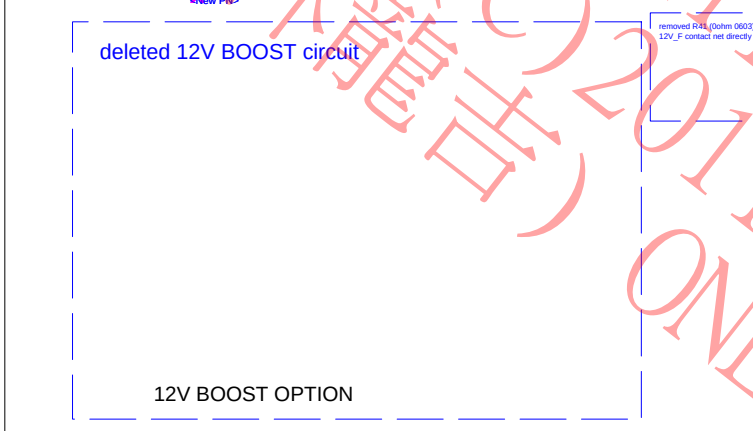












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ASSEMBLY	
PAGE DETAIL	MISC:GPIO, JTAG, INFO ROM, THERMAL LATCH, FAN CONTROL

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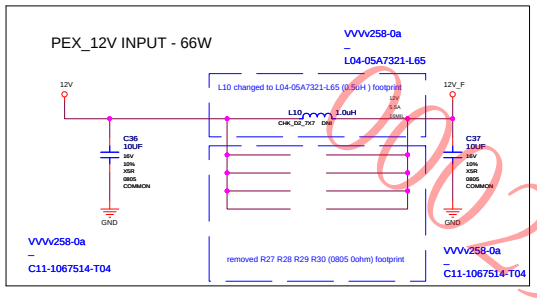
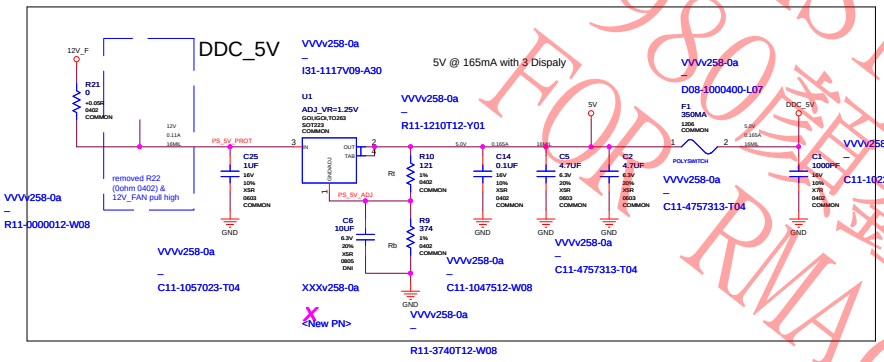
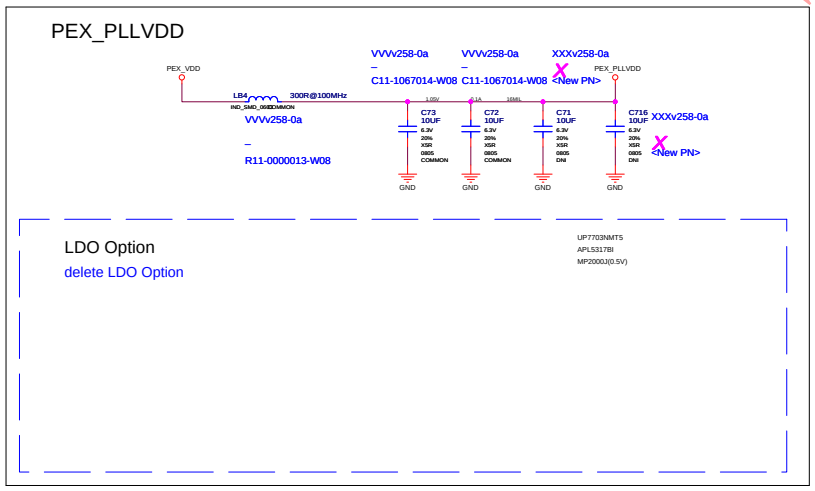
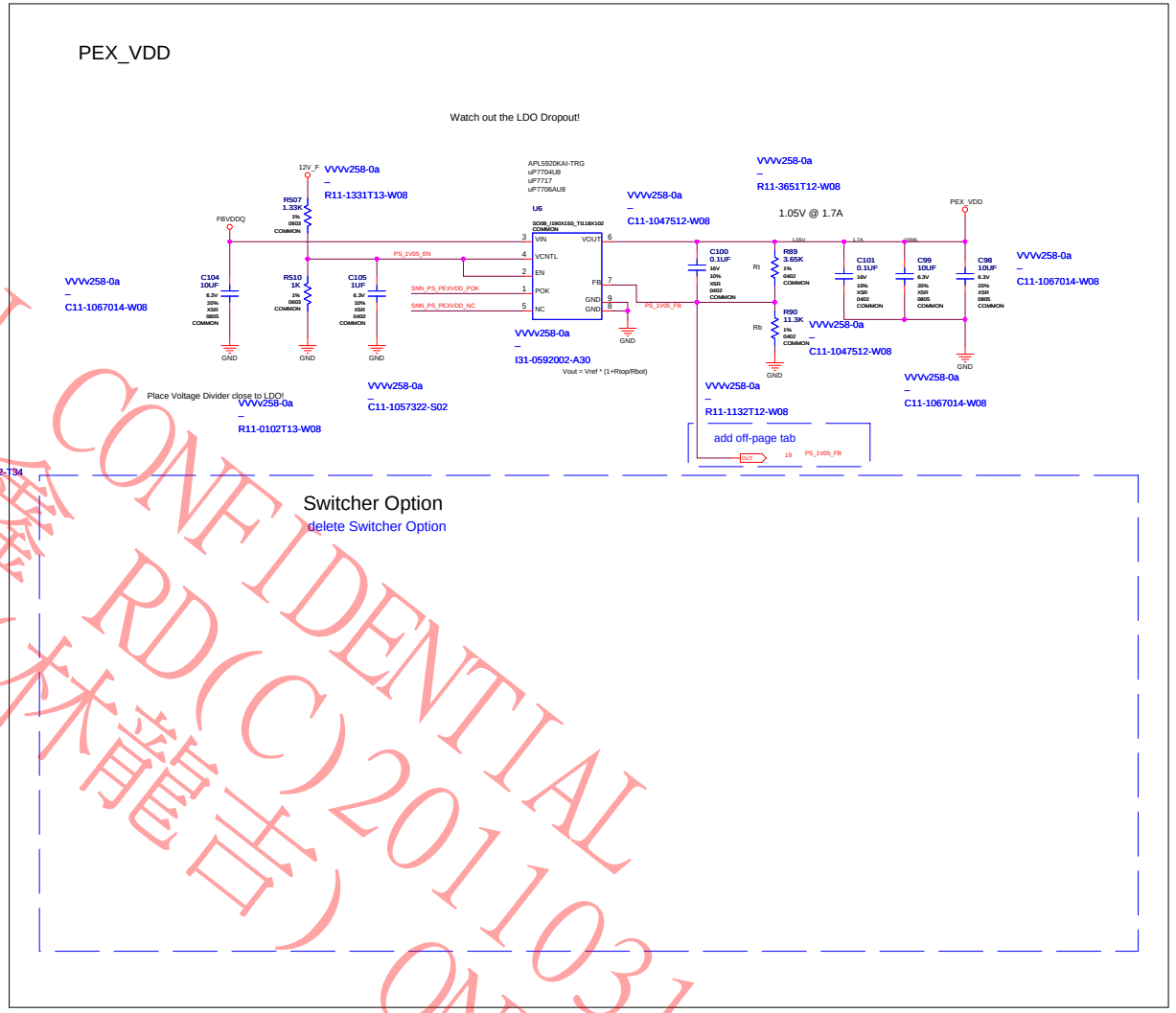
PCB REV	P1070-A01	PAGE	
BOM REV	A	DATE	29-APR-2010

Power Supply: 12V INPUT, DDC_5V, PEXVDD









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ASSEMBLY	
PAGE DETAIL	Power Supply: 12V INPUT, DDC_5V, PEXVDD

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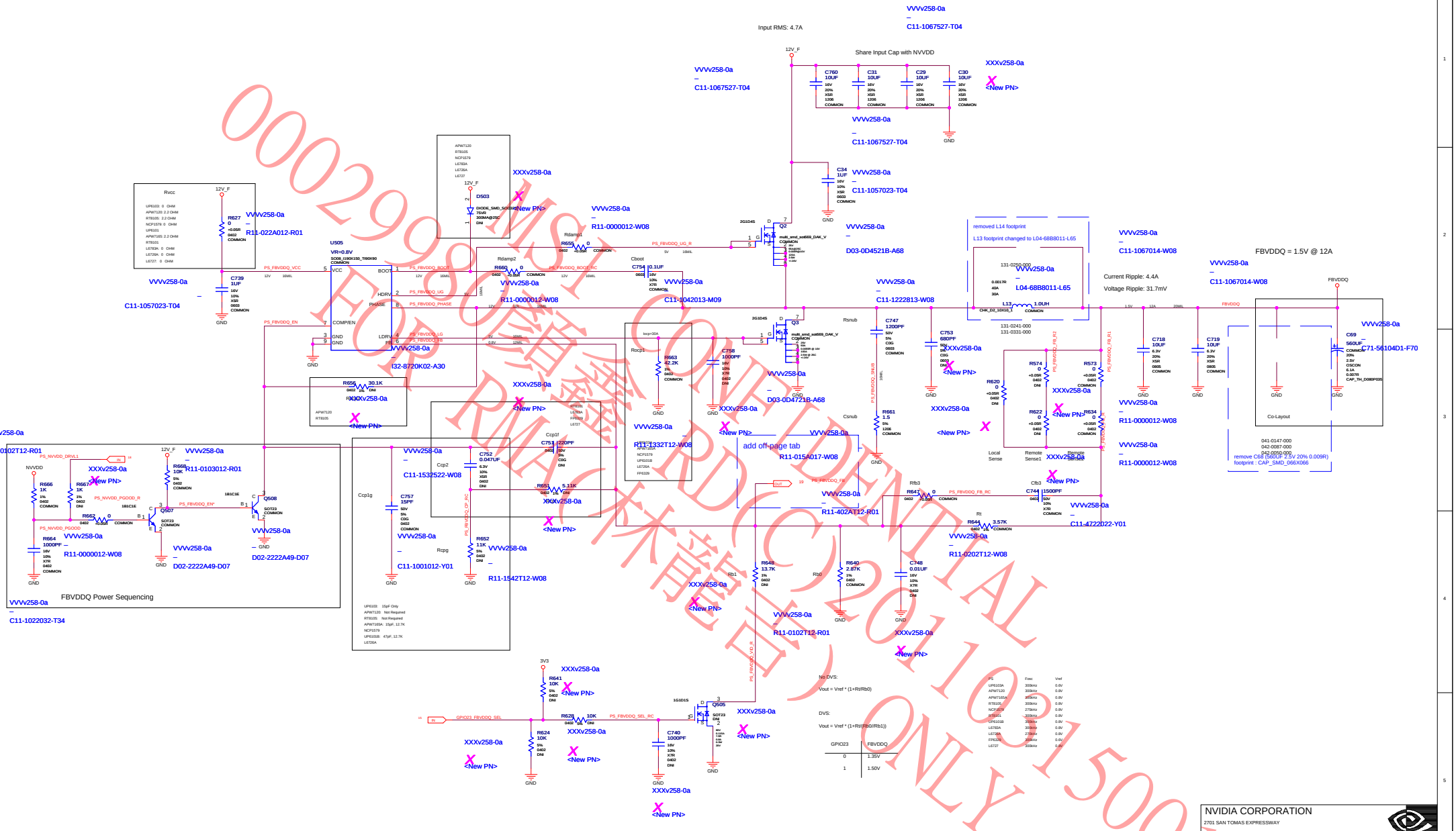
BOM REV	A	DATE	29-APR-2010

Power Supply: FBVDDQ



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PAGE DETAIL	Power Supply: FBVDDQ

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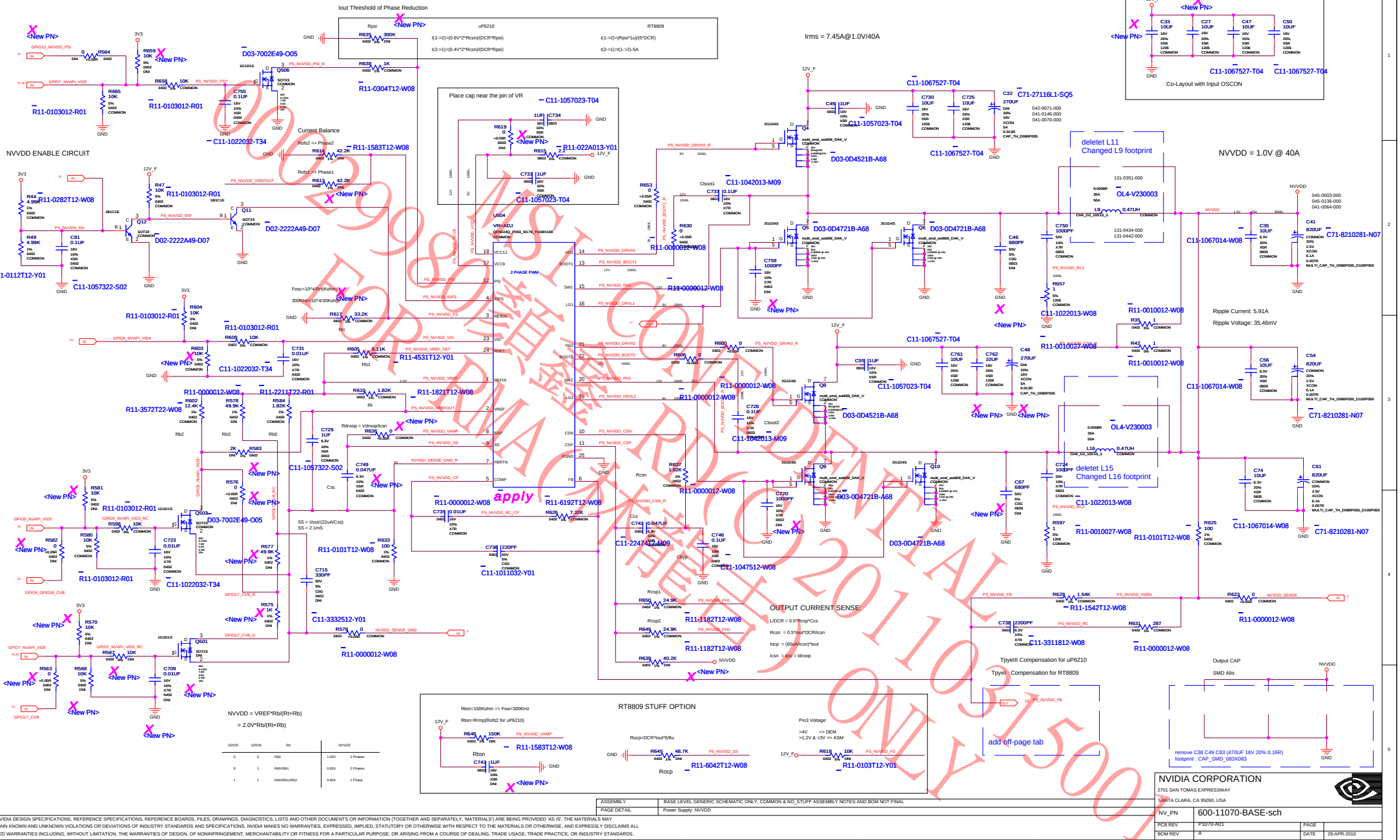
Power Supply: NVVDD



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PAGE DETAIL	Power Supply: NVVDD

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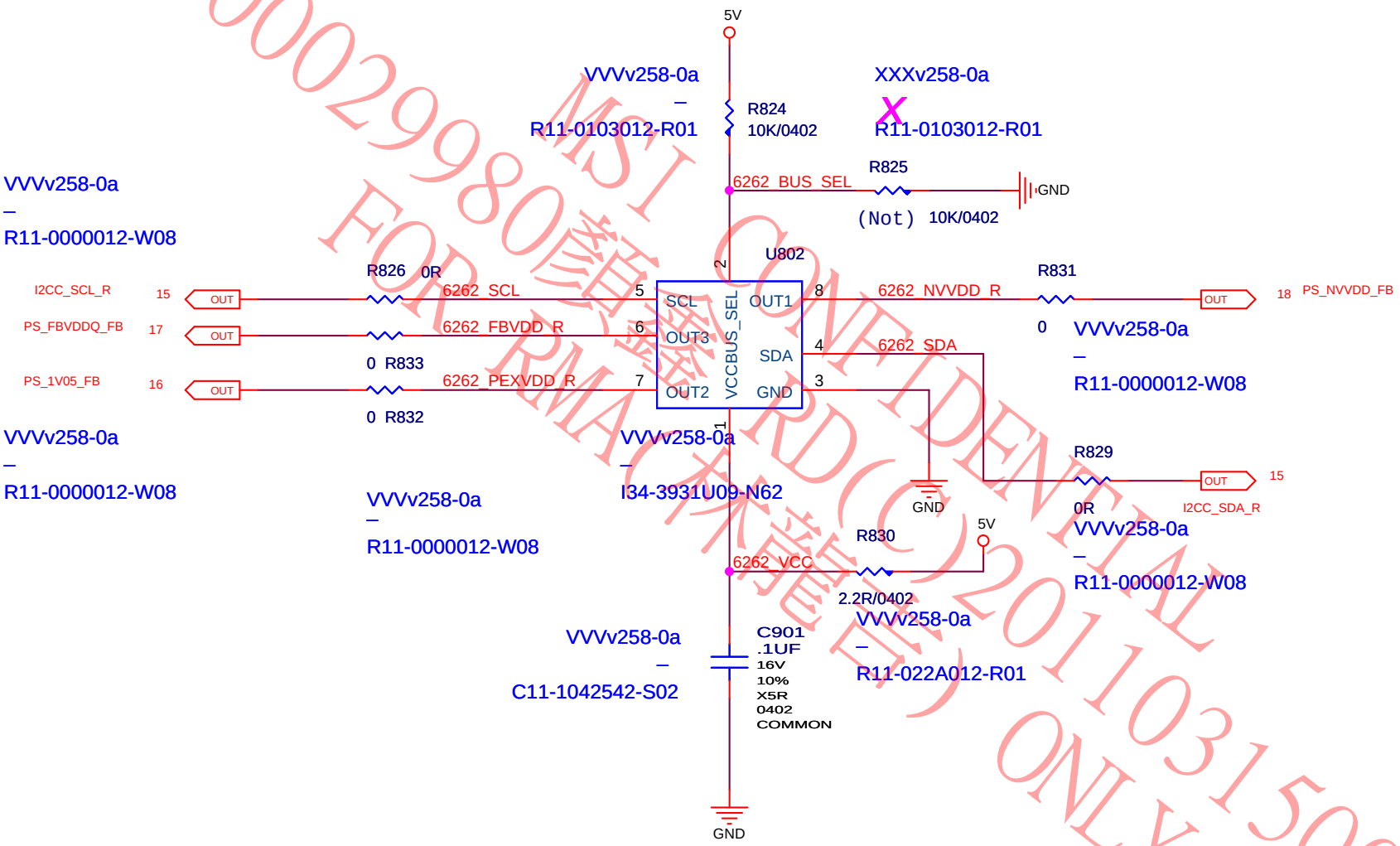
VDD adjust circuit

避免IC衝突，先預留0 OHm電阻



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Title: NVVDD adjust circuit		
Size: A	Document Number: 19	Rev: 1.0
Date: Friday, December 03, 2010	Sheet 19 of 19	