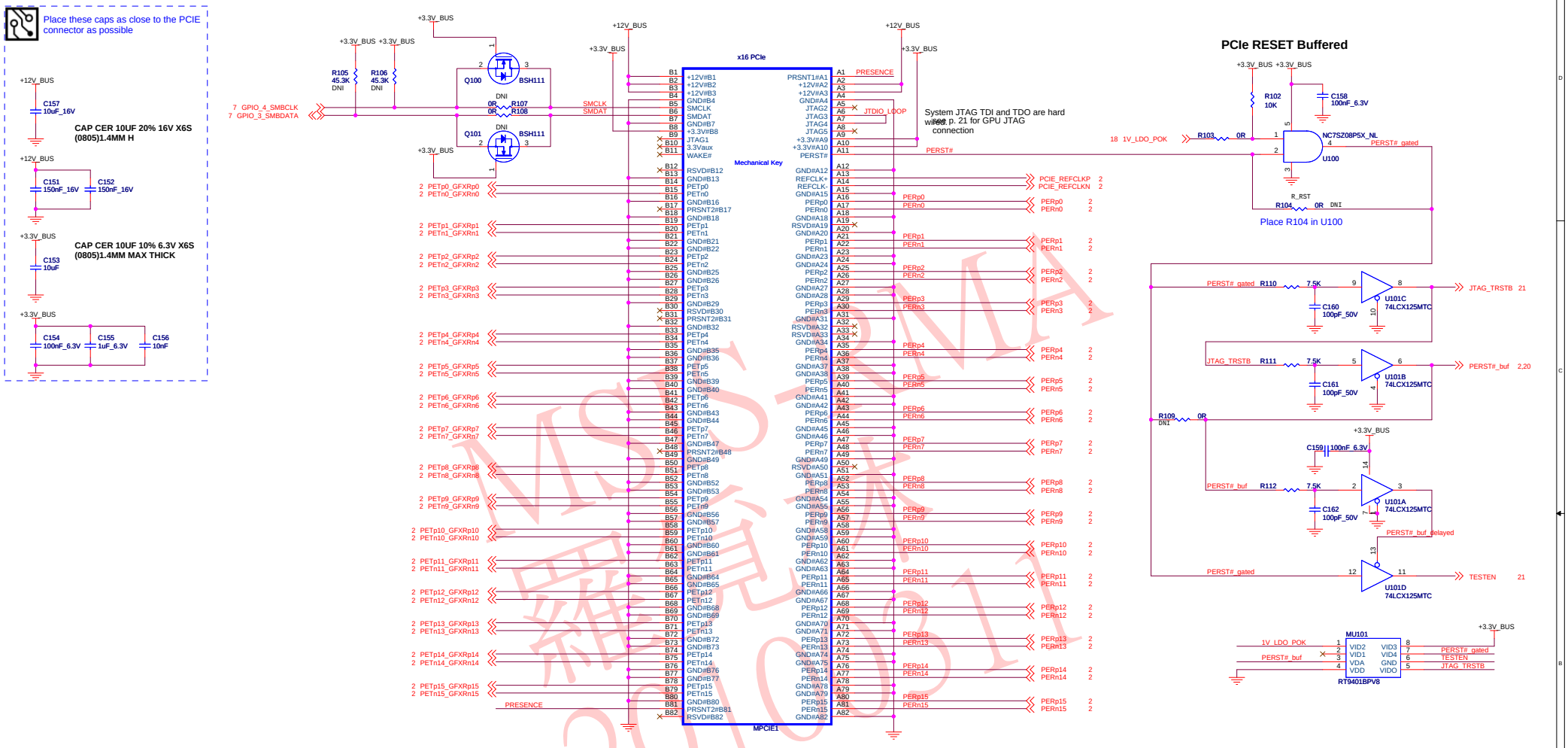
PCI-EXPRESS EDGE CONNECTOR



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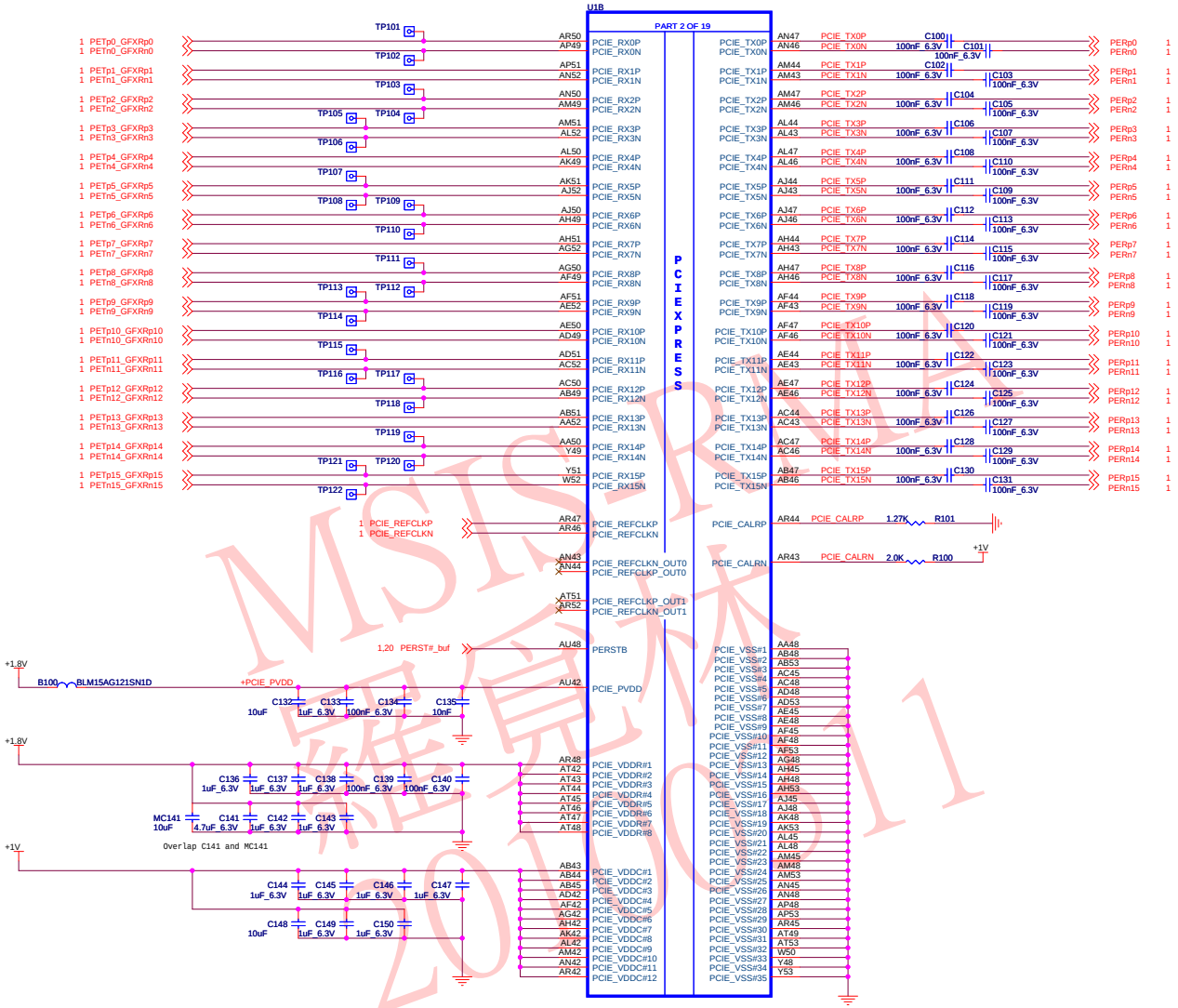
(2) CYPRESS PCIE Interface

NOTE: Some of the PCIE testpoints will
be available through vias on traces.



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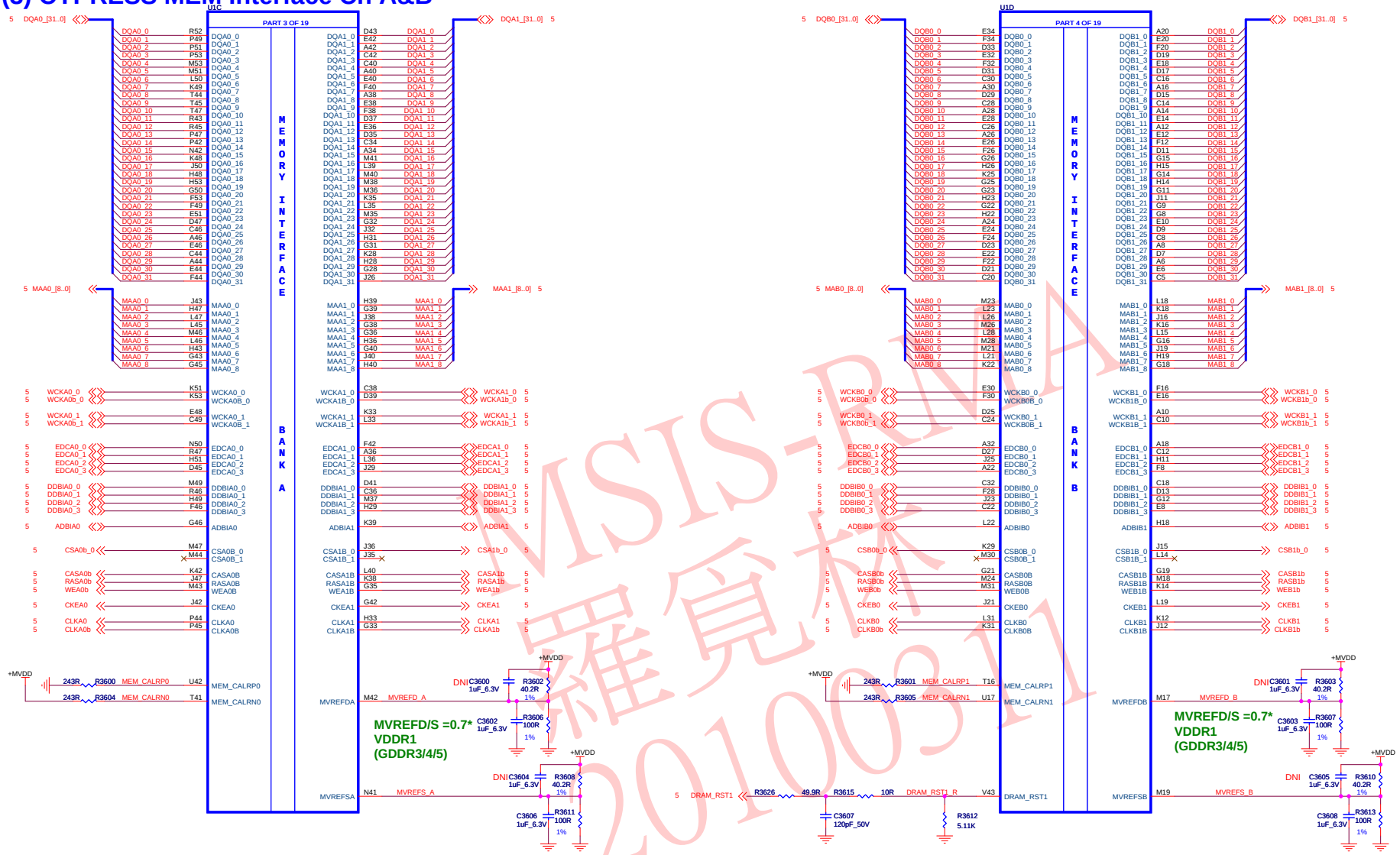
(3) CYPRESS MEM Interface Ch A&B



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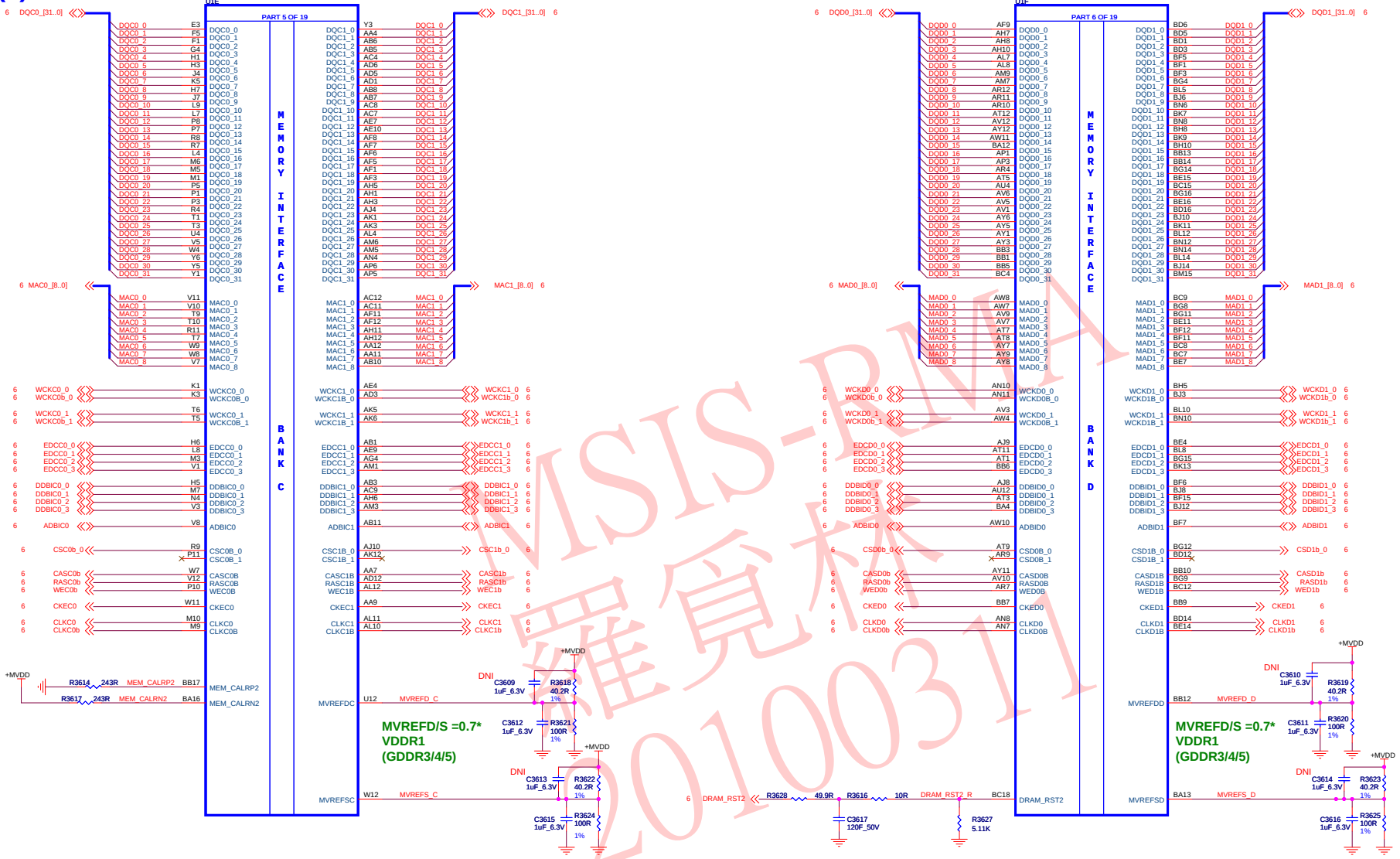
(4) CYPRESS MEM Interface Ch C&D



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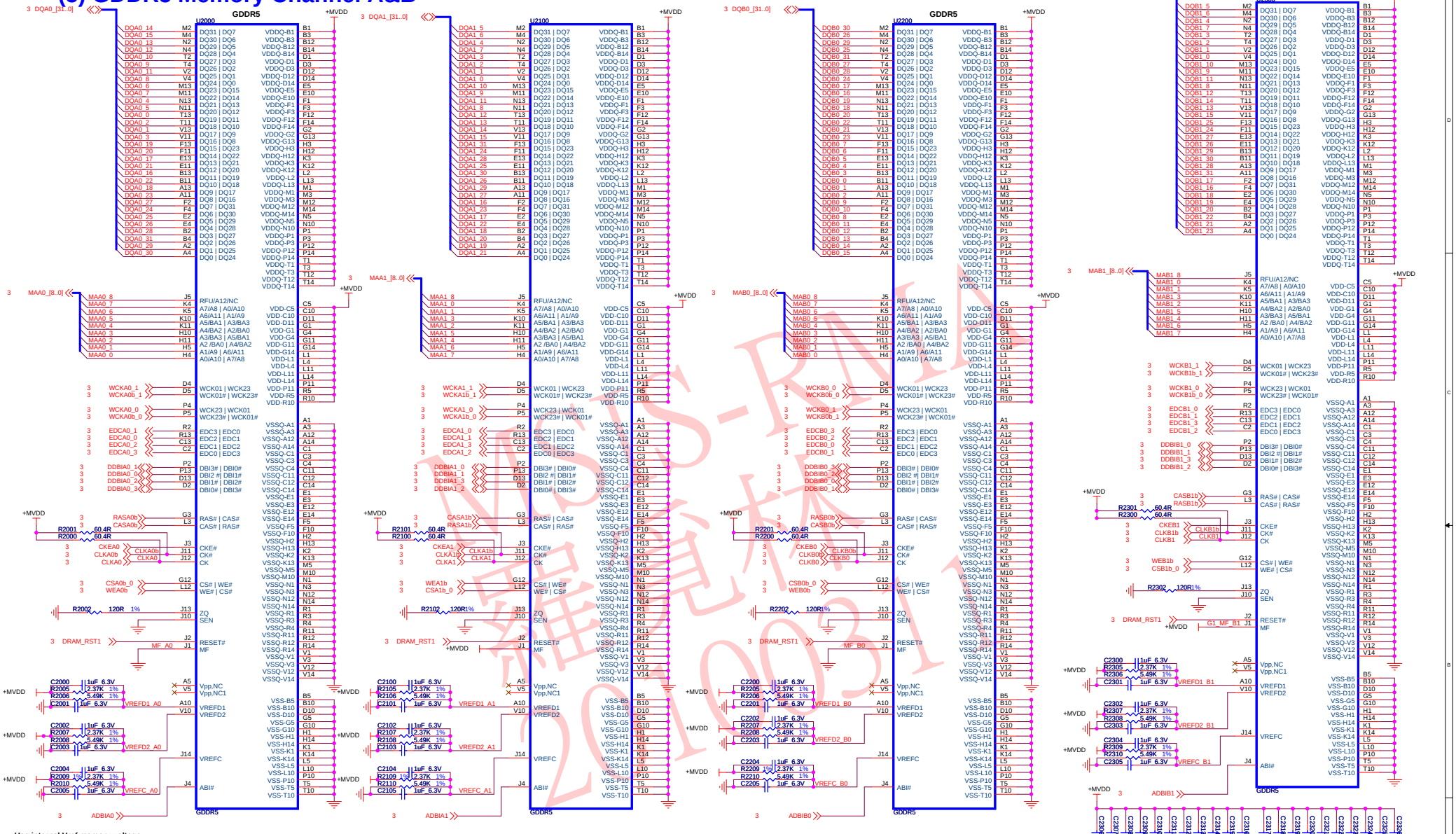
(5) GDDR5 Memory Channel A&B



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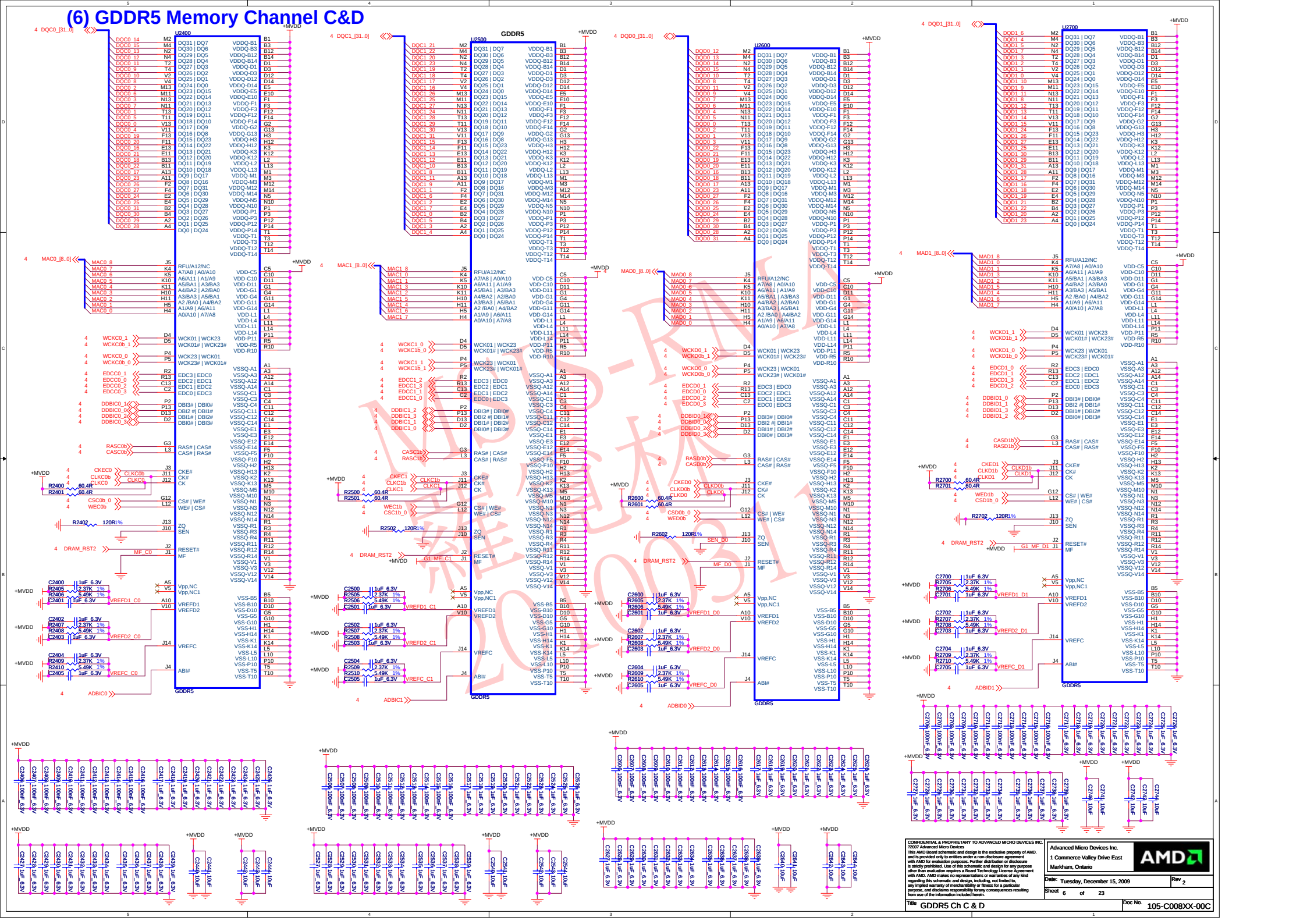
(6) GDDR5 Memory Channel C&D



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(07) Cypress GPIOs Strap CF XTAL OSC

PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO(13,12,11) - CONFIG[2..0]

CONFIG[2]	100 - 512Kbit	M25P05A	(ST)
	101 - 1Mbit	M25P10A	(ST)
CONFIG[1]	101 - 2Mbit	M25P20	(ST)
	101 - 4Mbit	M25P40	(ST)
CONFIG[0]	101 - 8Mbit	M25P80	(ST)
	100 - 512Kbit	Pm25LV512	(Chingis)
	101 - 1Mbit	Pm25LV010	(Chingis)

VIP_DEVICE_STRAP_DIS
0:VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

RESERVED:
Internal use only. Other logic must not affect these signals during RESET.

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability
TV OUT STANDARD 0 - PAL TVO 1 - NTSC TVO

RESERVED:
STRAP_BIOS_ROM_EN
CLKREQ# that requires open drain connection, and cannot be used as pinstrap
Don't set high at reset

Internal use only. Other logic must not affect these signals during RESET.

CrossFire Card-Edge

Upper Cable Card Edge

Lower Cable Card Edge

Place the crossfire testpoints near the ASIC and not the connector

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

Overlap pads

Change U2 SL16010DCT to Uc1008

Co-lay Uc1008 with U12 SL16010DCT

SCL / SDA BUS:

I2C Address	Function	Device
0xE0	VDDC REG	VT1165M
0xE2	VDDCI REG	VT1165M
0xA0	MVDDQ (debug)	UP6267
0xA2	MVDDC (debug)	UP6266

DDC6 BUS:

I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

PWRGOOD must be connected to GND for normal operation

Divider for 1.8V signaling.

route 50ohms single-ended/100ohms diff and keep short

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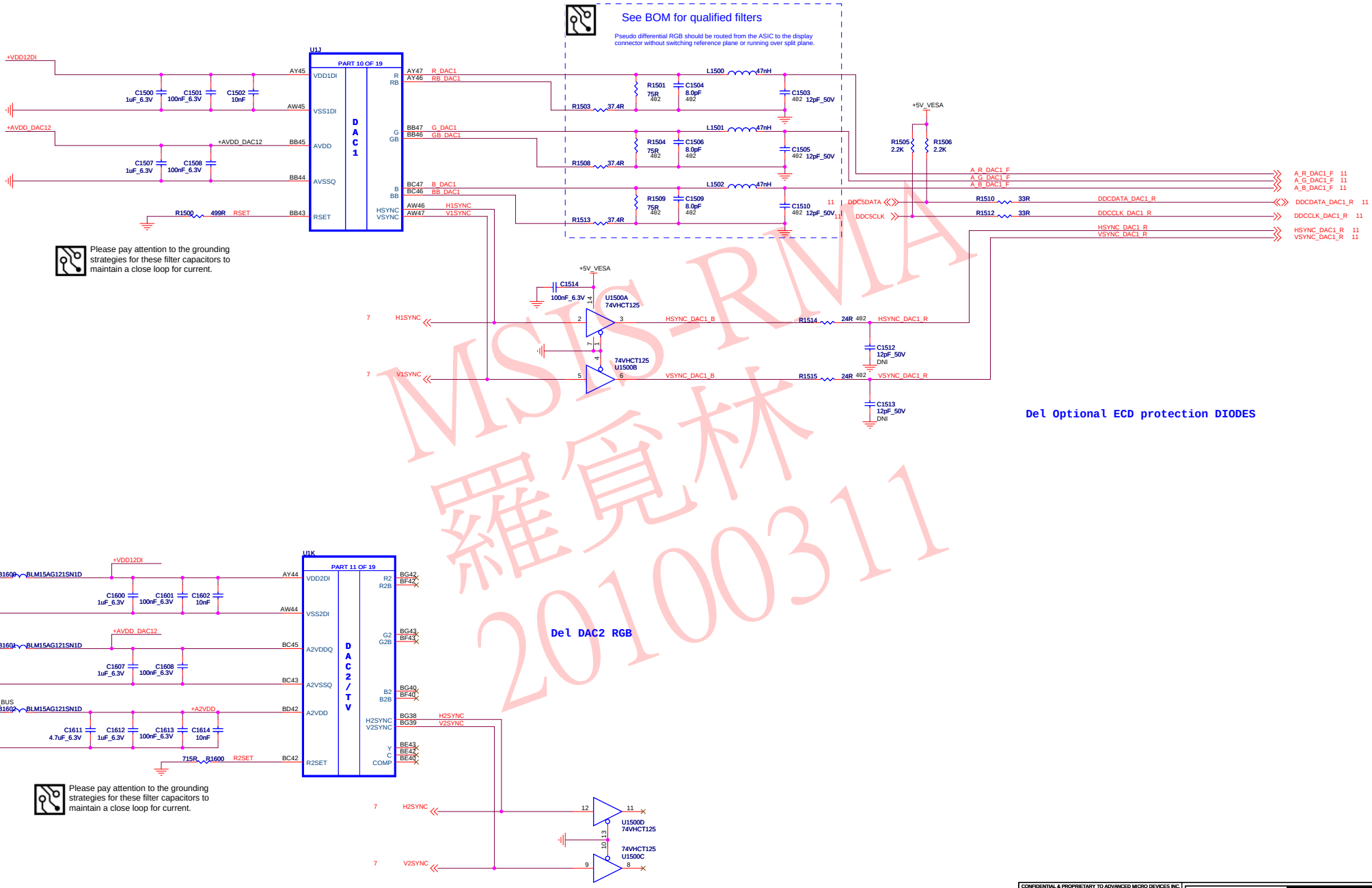
(08) CYPRESS DAC1 and DAC2

Del Optional ECD protection DIODES



Del Optional ECD protection DIODES

Del DAC2 RGB

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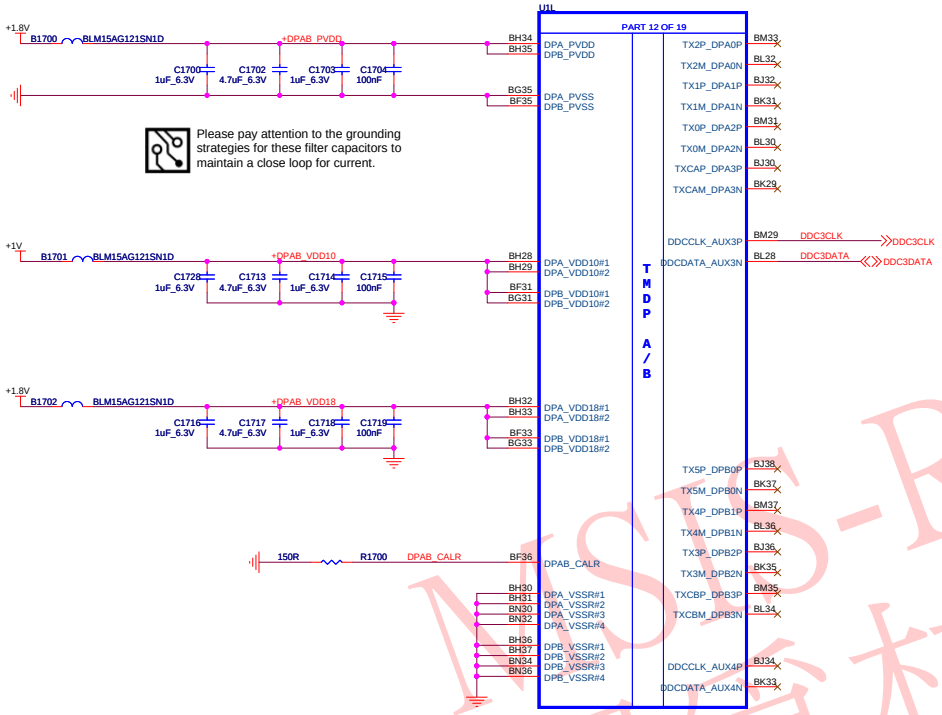
(09) CYPRESS TMDS A&B



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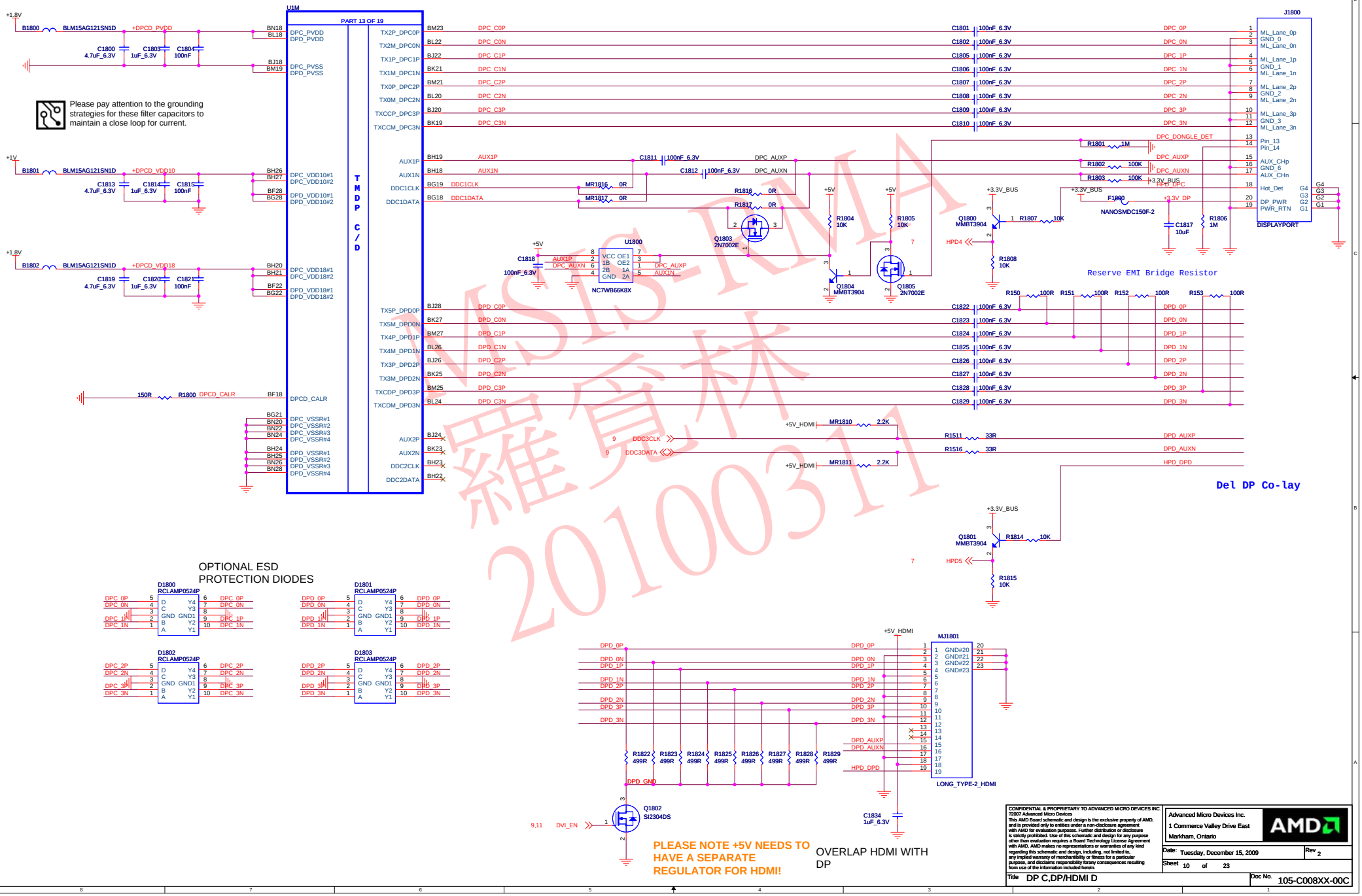
(10) CYPRESS Display Port/HDMI C&D



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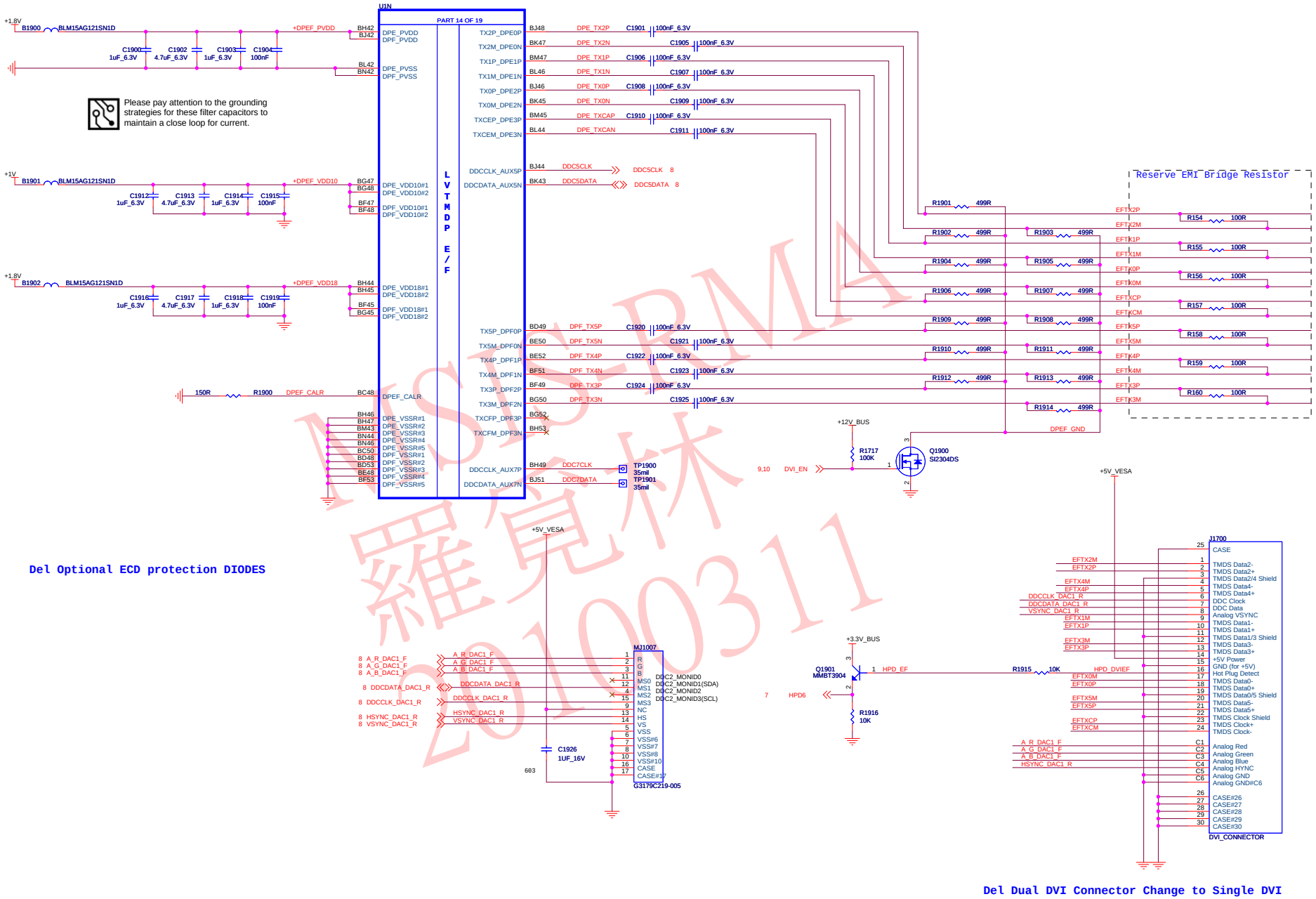
(11) CYPRESS LVTMDP E&F



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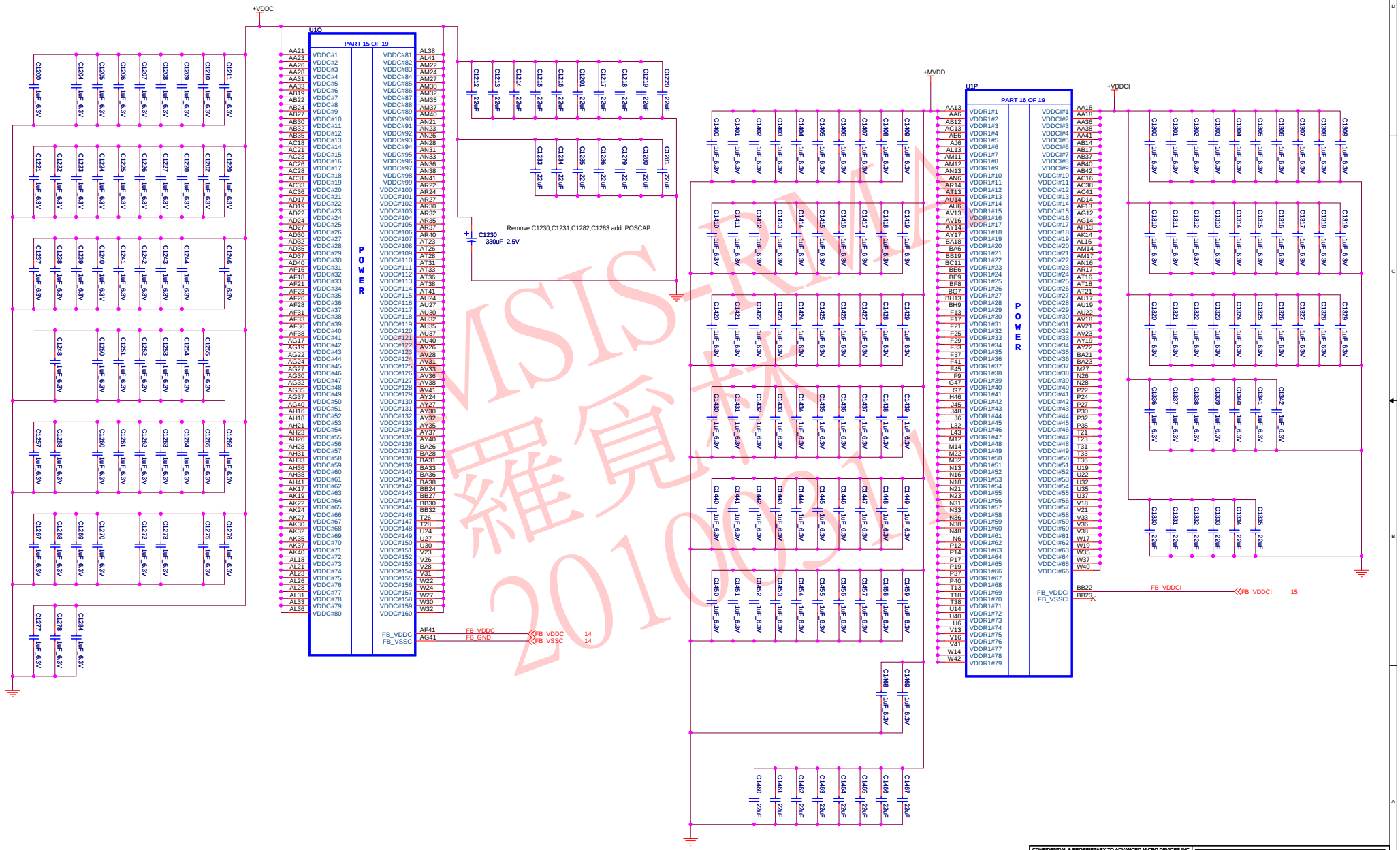
(12) CYPRESS Power



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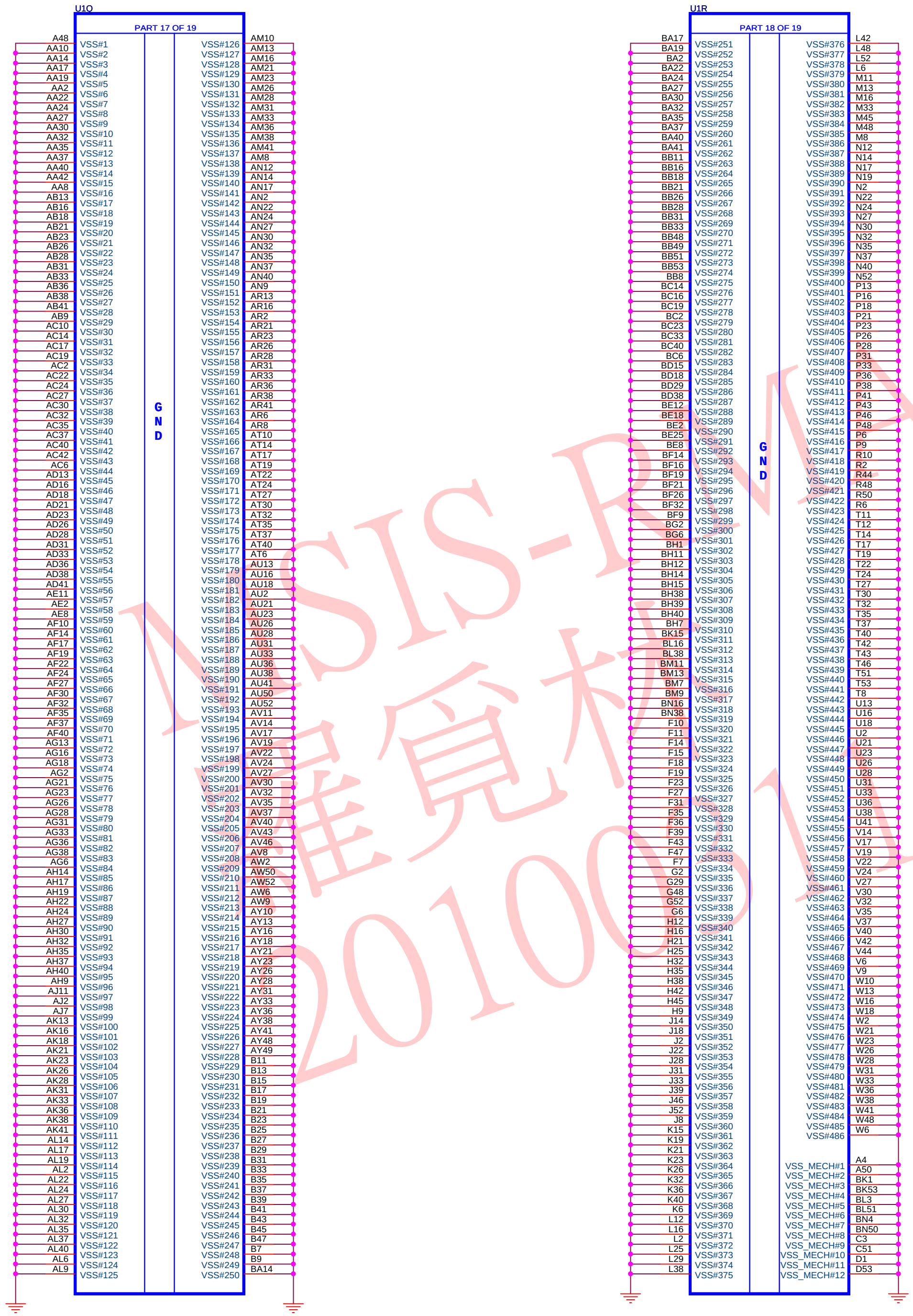
(13) CYPRESS GND



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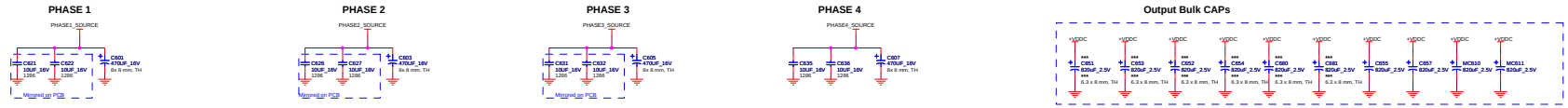
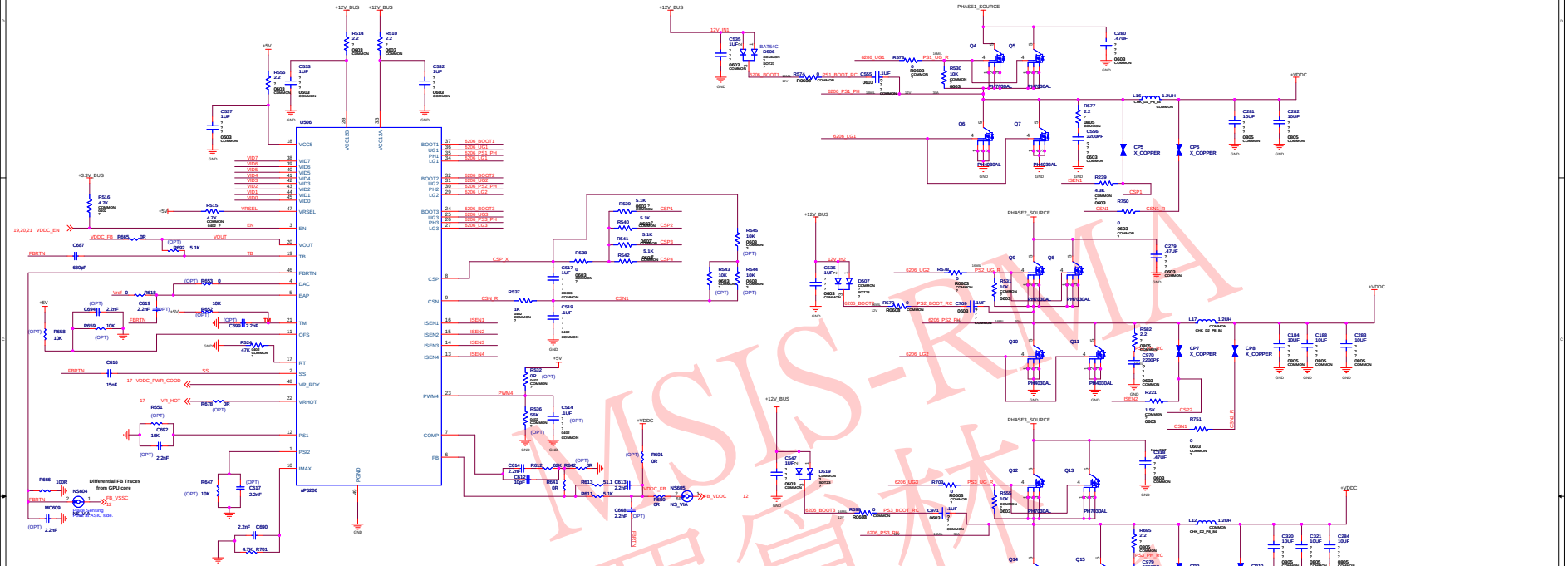
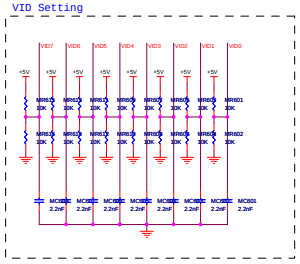
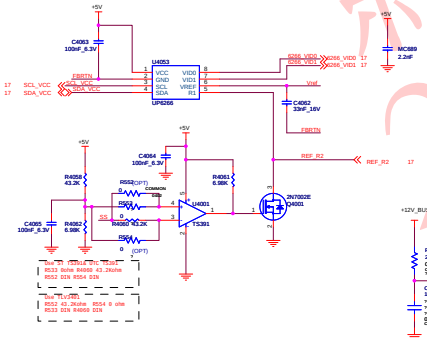
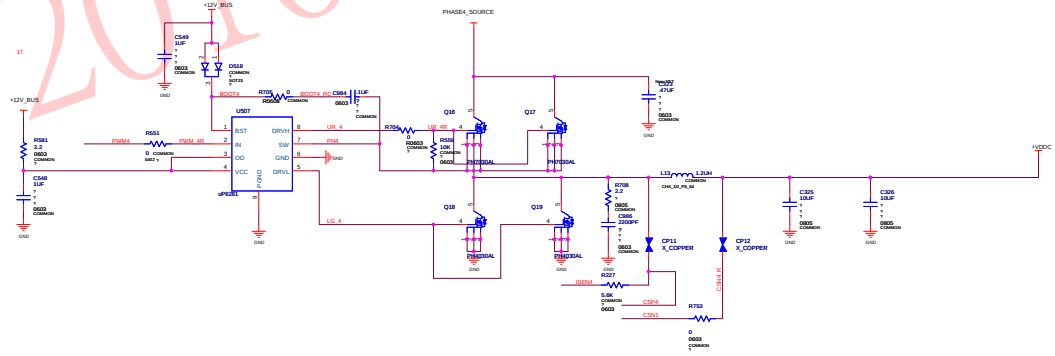
(14) VDDC











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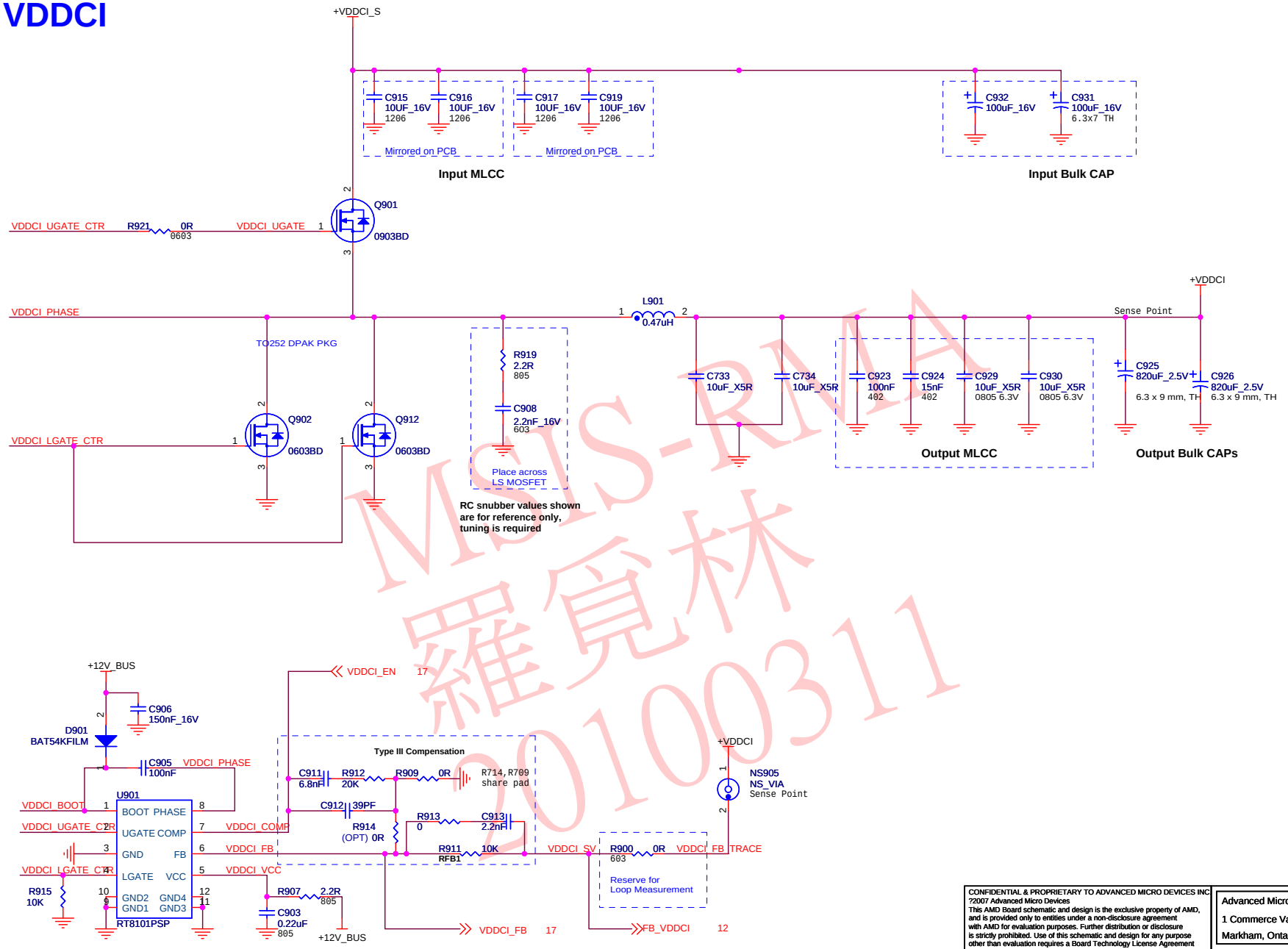
(15) VDDCI



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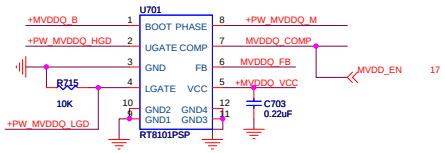
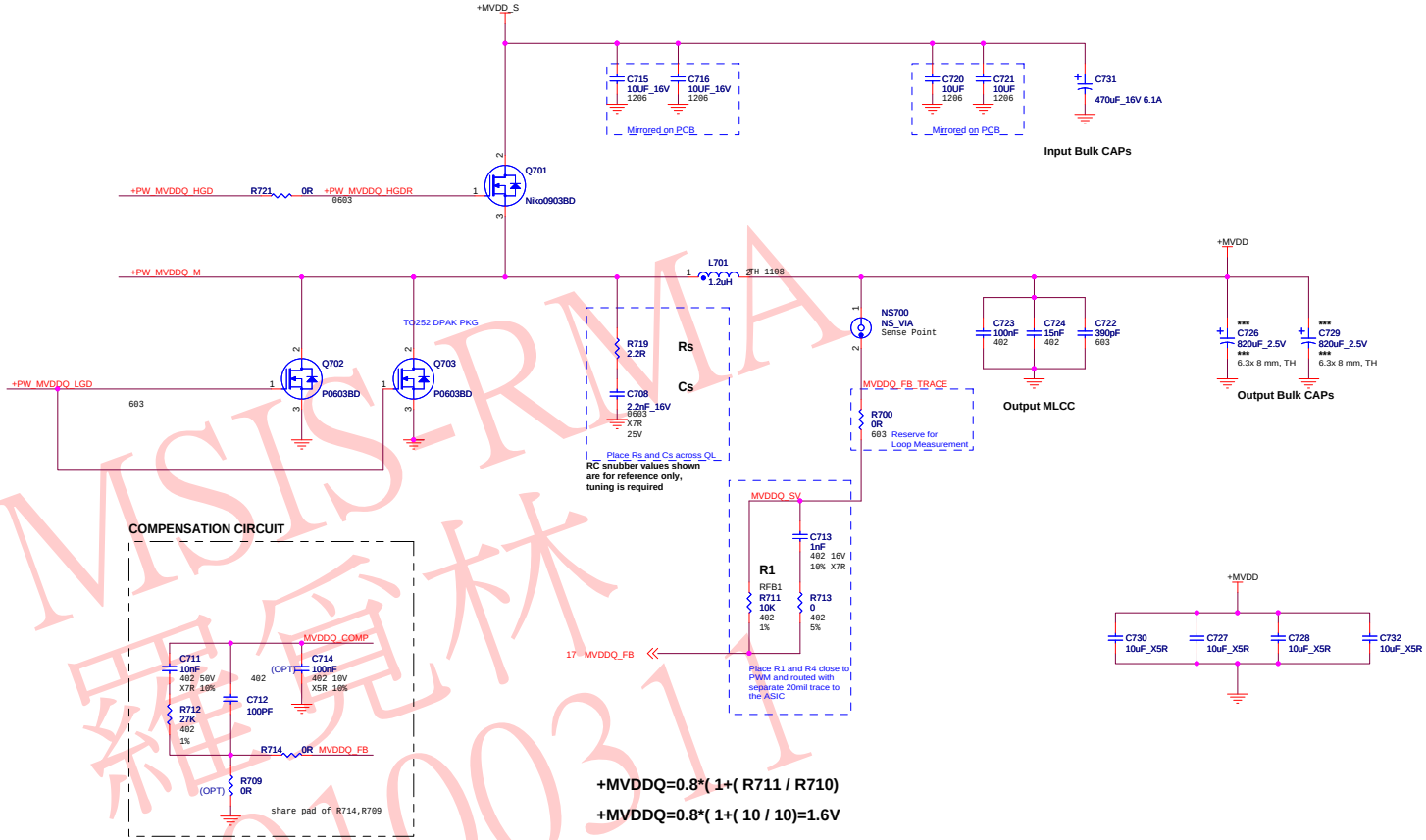
(16) MVDDQ



Layout guideline

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

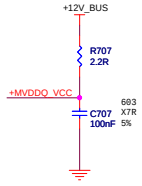


COMPENSATION CIRCUIT

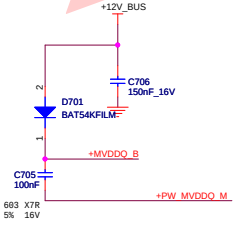
+MVDDQ=0.8*(1+(R711 / R710)

+MVDDQ=0.8*(1+(10 / 10)=1.6V

FILTERED SMPS VCC



BOOT CIRCUIT



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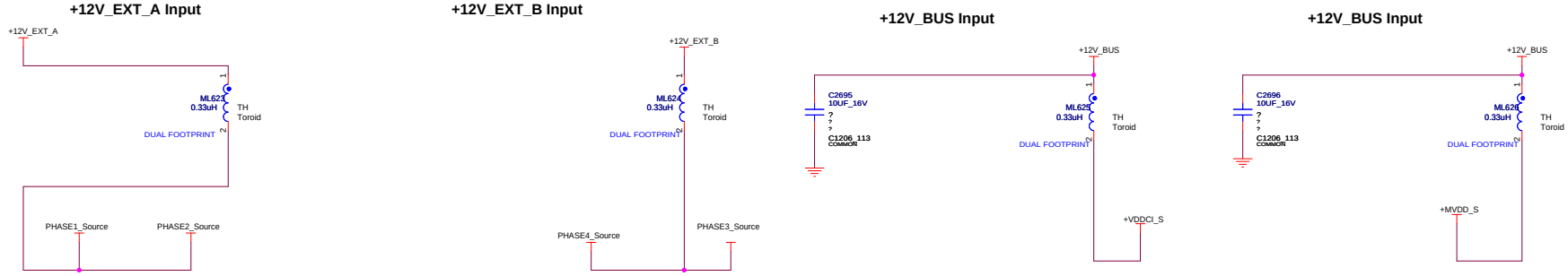
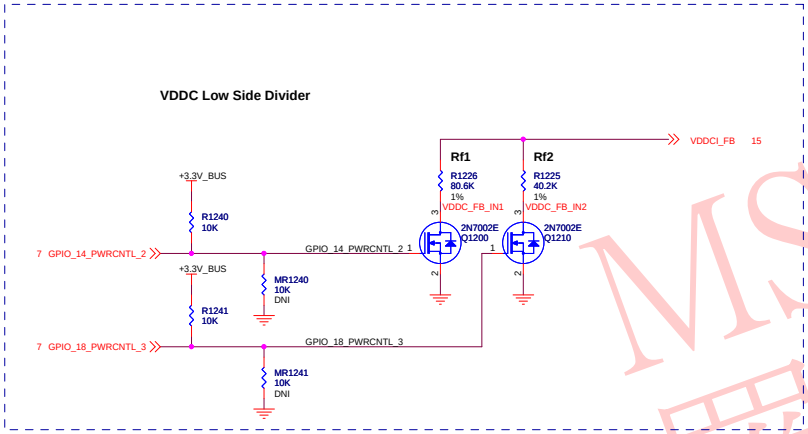
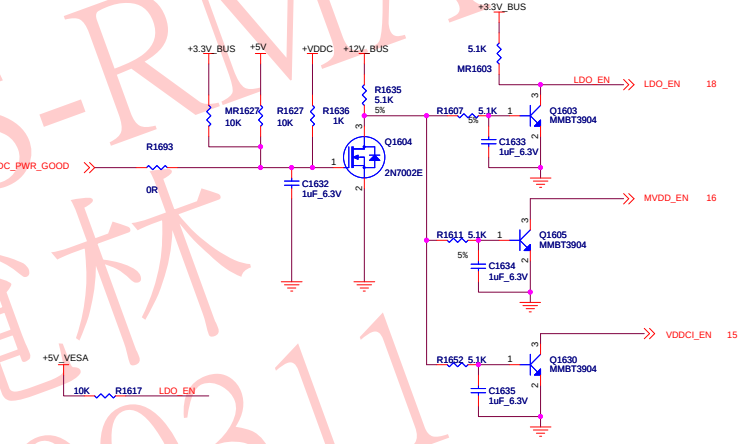
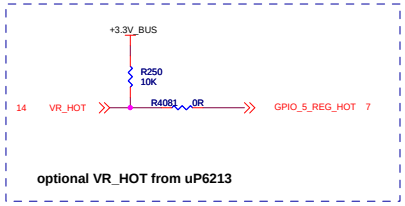
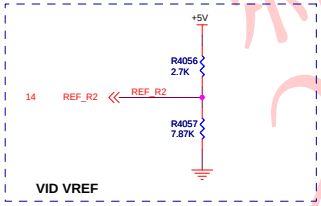
(17) CYPRESS VDDCI POWER PLAY



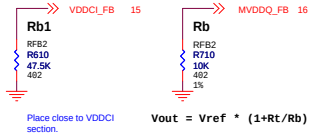








Resistors to set the output voltages for +VDDCI and +MVDD .



VDDC DPM through GPIOs (PVID)

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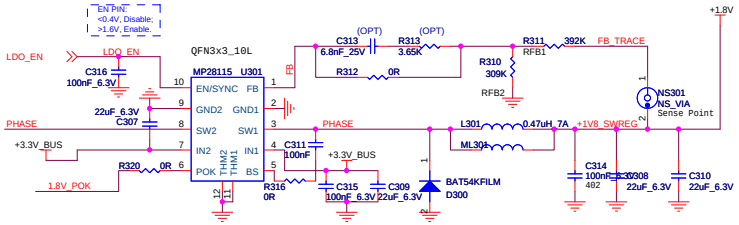
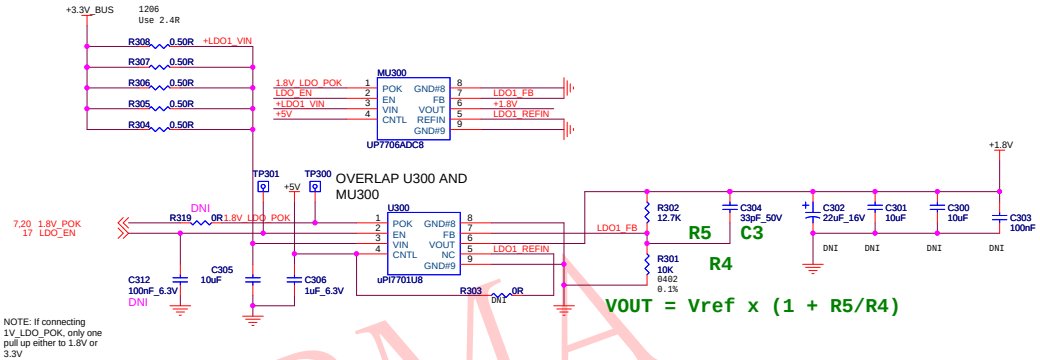
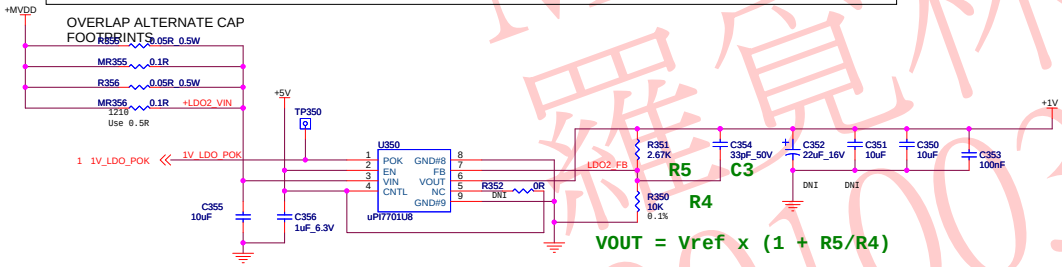
(18) CYPRESS Small Rail Regulators

LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

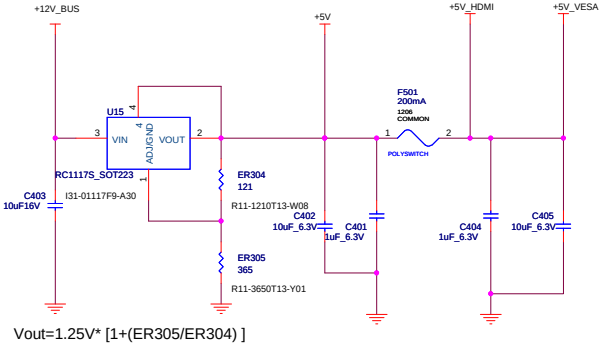




LDO #2: Vin = +1.35V to 1.8VMAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



optional 5V power for VDDC regulator;



Vout=1.25V* [1+(ER305/ER304)]

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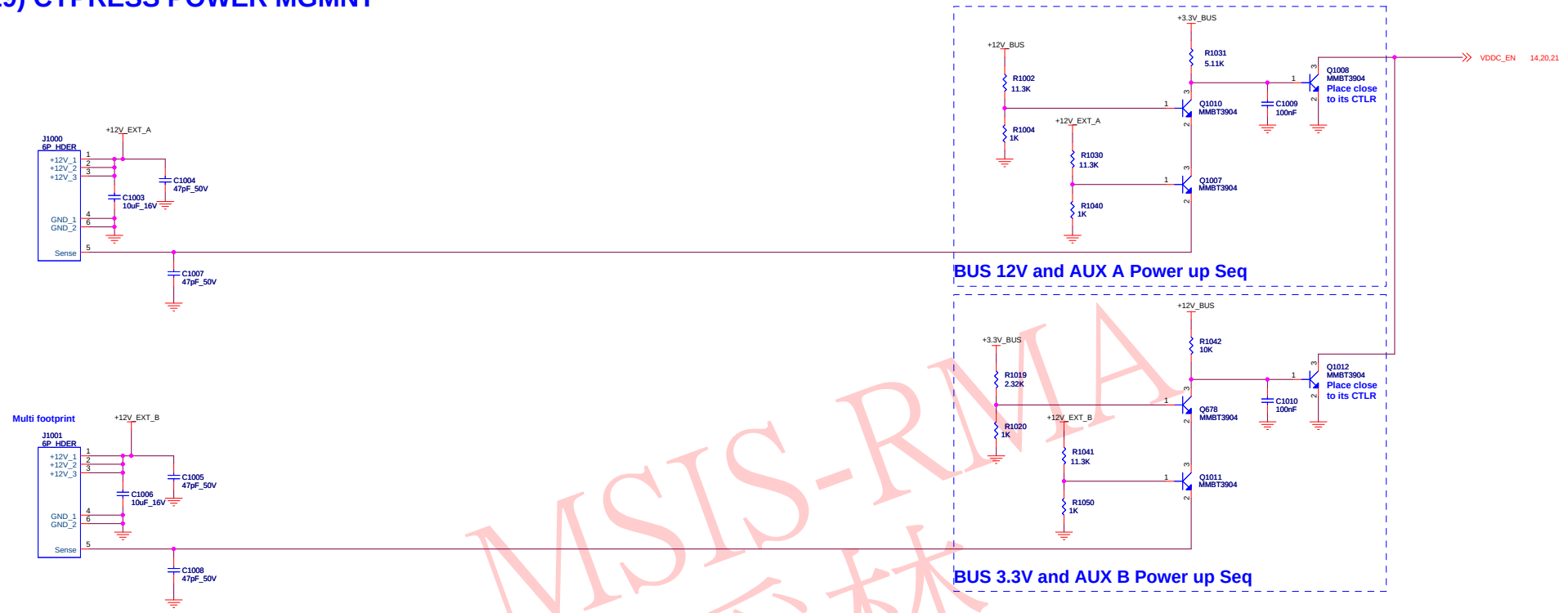
(19) CYPRESS POWER MGMNT



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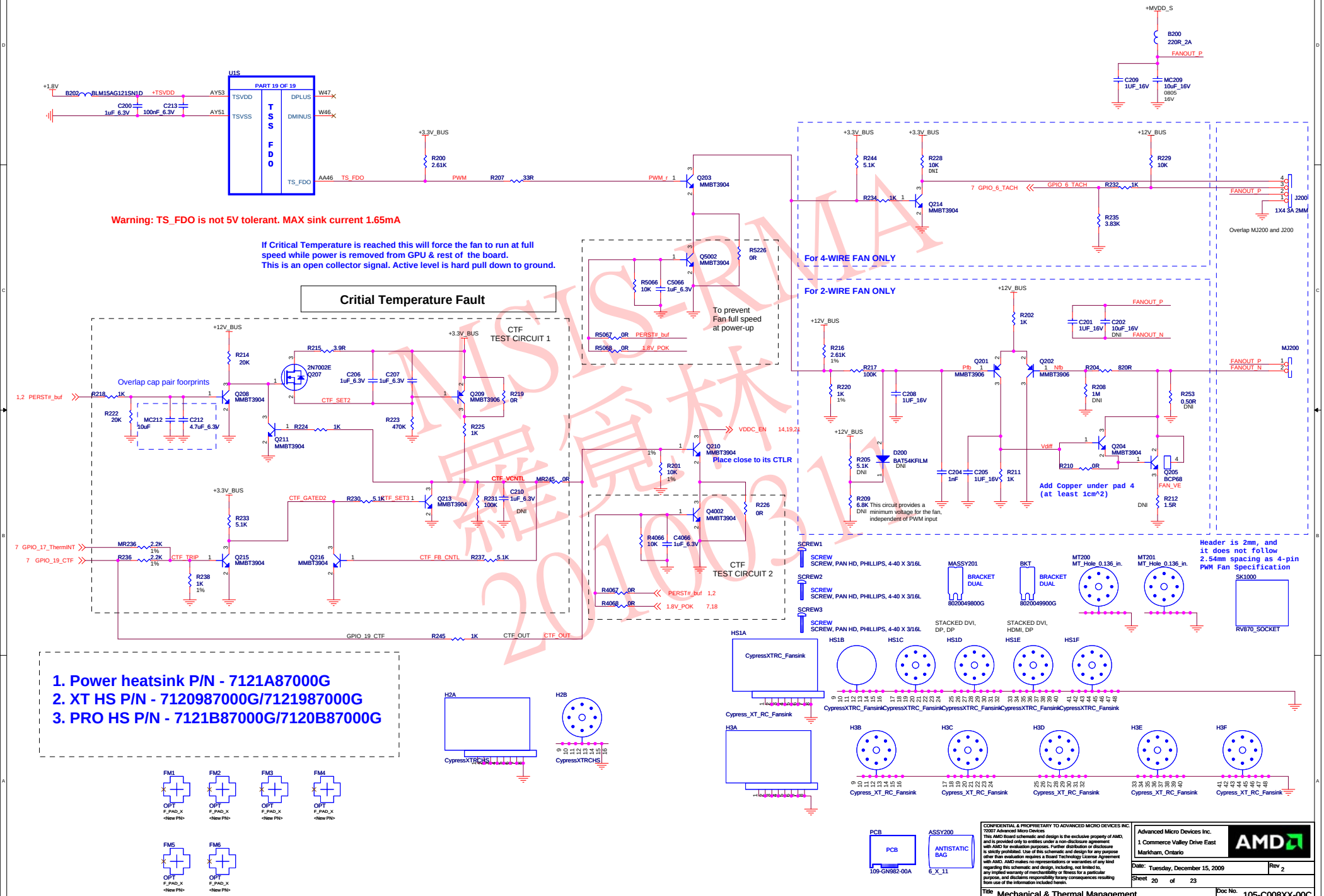
(20) CYPRESS Mechanical and Thermal Management



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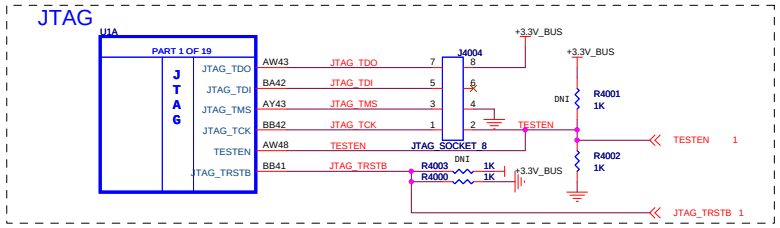
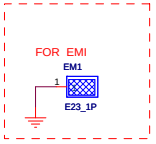
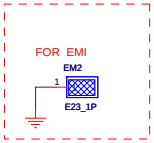
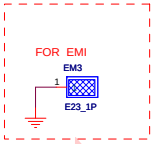
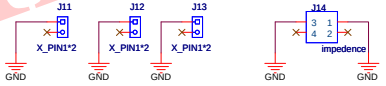
(21) CYPRESS Debug Circuits











Del PTC protect circuit.

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1 Commerce Valley Drive East
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Date: Tuesday, December 15, 2009 Rev 2

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Title Debug Circuits

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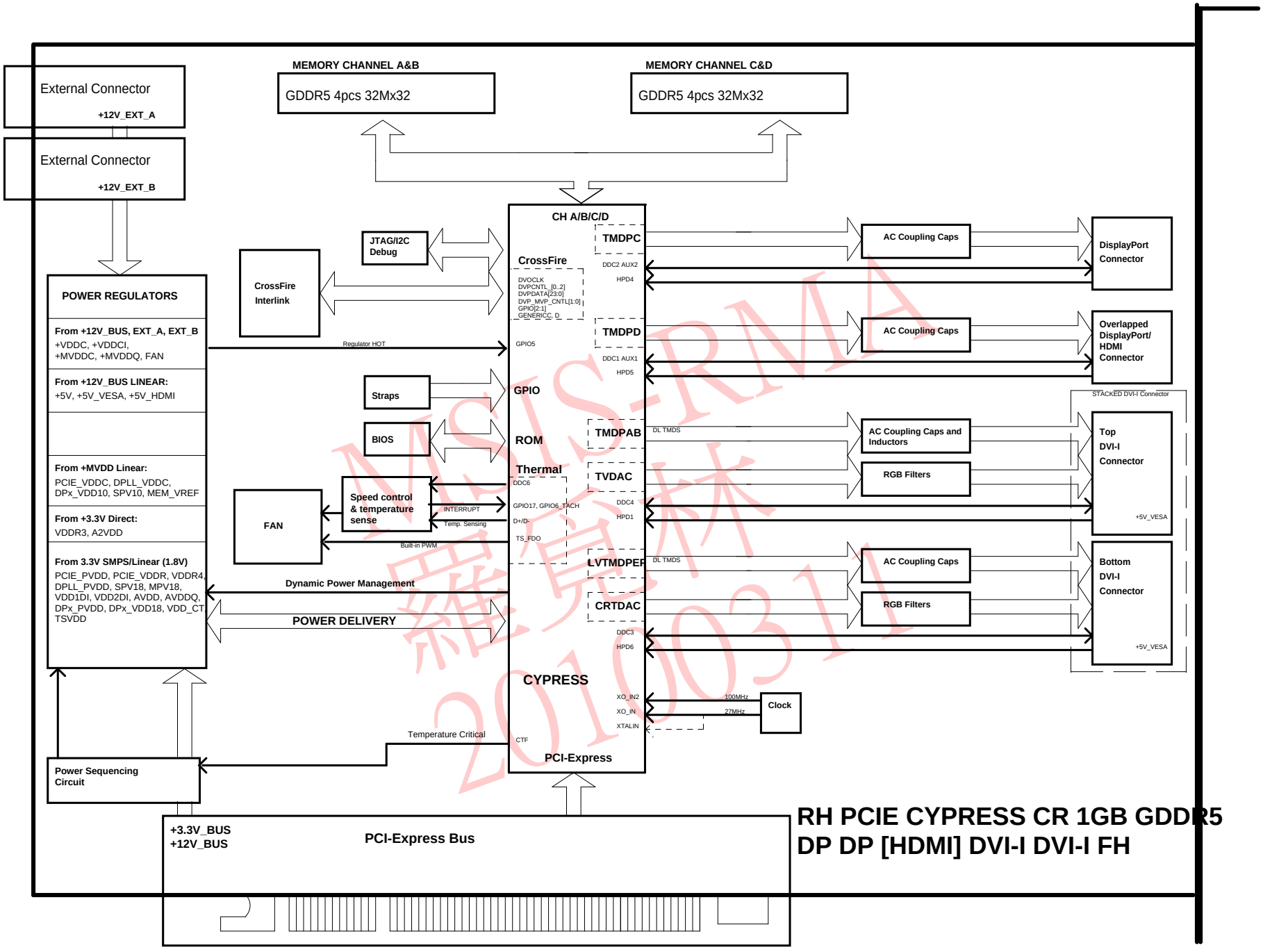

RH PCIE CYPRESS CR 1GB GDDR5
DP DP [HDMI] DVI-I DVI-I FH

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Title	Schematic No.	Date:
RH CYPRESS GDDR5 DP-HDMI-DVII-DVII	105-C008XX-00C	Tuesday, December 15, 2009

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	09/08/11	
1	00B	09/08/26	
2	00C	09/09/24	Initial release. Based on CYpress XT C001 00 PCB
	V209-0A	09/10/12	Based on CYpress XT C008 0C PCB 1. Page 7 Change U2 SL16010DCT to Uc1006 and Co-lay Uc1008 with U12 SL16010DCT 2.Page 8 Del DAC2 RGB 3.Page 9 Disable TMDP AB and disable DDC_AUX3,DDC_AUX4 4.Page 10 Del DP co-lay with HDMI 5.Page 11 Del Dual DVI Connector Change to Single DVI and Co-lay Silm D-Sub 6.Page 12 Remove C1230,C1231,C1282,C1283 add POSCAP 7.Page 14 Change VDDC PWM to Up6206 8.Page 18 Change +5V circuit. 9.Page 21 Del PTC protect circuit.
		09/11/2	10.Page3,4 changing the DRAM reset circuit 11.Page10 chang HDMI DDC to DDC3 12.Page 14 co-lay U4001 with TLV3401