

NV25, P80, DUAL DAC/TMDS, 128MB 4MX32 BGA DDR, TV IN/OUT, GOGGLES, AGP

P80-A00: Based on P53-A00.

A00-X00:
Populate R1034 with 0.01 Ohm
Populate 68R parallel terminations on FBCLK/CLK#

A00-X01:
Isolated GND, AGND and Chassis GND
Corrected Multichip Strap
Changed sync buffers inputs from pin 2 to pin 1 for easy probing.
Corrected PWRGD_FBVDD on memory PS

A00-X02:
Combined CX and SA power filters.
Connected memory PS bootstrap to 12V.
XOR Hotplugs to GPIO1.
Isolated PLL_VDD from 3.3VL to get rid of 350mV stray voltage.
Combined GND, AGND and Chassis GND

A00-X03
Changed both TMDS digital powers from 3.3V to 3.3VL.
Added a resistor to base transistor PLL_VDD sequencer.
Added 2nd fan connector.
Added various placement and routing notes.

P80-A01:

A02-X00
Fixed serial rom connections.
Added, again GND isolations.
Added testpoints to various (SAA7108) pins.
Changed DVO clocks series termination to 10R.

A02-X01
Moved VGA con and Bracket to new Sheet 3.2
Moved SROM to new Sheet 5.2
Moved SROM to new Sheet 5.2
Moved SEC-DVI Connector to Sheet 6.5
C1262, R1129 Changed to No stuff.
131-60102-0063-02 is SUB for 131-10102-0061-006
R1072 is changed to 2.2K from 1.5K, Put in BOM.
R1204(Nostuff), R1205-0R Added for FBVDDQ Power sequence after 3.3VL
R207 Changed from 118R to 105 Ohm
R927 Changed from 118R to 102 Ohm
C1405, C1406 Value changed to 330uf

A02-X02
Design file under Perforce Control.
Changed DACA IDUMP resistor to 0402pkg

A02-X03
Turned DACA SYN buffers into "analog" to ease the AGND antietch.
Added 5 caps on VDDDVO pins.
Changed R1116 to 0402 pkg.
Enabled AGP Fast Write.
Changed PS snubber's resistor to 2.2R (from 100R) per Semtech recommendation.

A02-X04
Combined FCCDDCPWRVGA and DDC+5V nets (del. L711 and C1116) for ease of routing.

A02-X05
Changed R1115 and R1116 back to SMD0603

A02-X06
Isolate SC1175 and SC1102 AGNDs per Semtech recommendations.
Removed 5V power option from SC1102.
Changed crystal loading caps to 10pF and have them reference to digital GND.

A02-X07
Changed snubber resistors to 0805 pkgs
Added RC to SC1102 VREF pin (NO_STUFF)
Removed extra X elements.

A02-X10
Added a 2A fuse on 12V input due to SC1102 current limit bug.

A02-X11
Added ICT to MCHIP_RST_ (GPU.AK5)
Removed SMD0805_SHORT symbols from PS pages (nets merged to GND)

P80-A03: Re-spin

A03-X00
Add two 5-3.0 VR for DVOA and B BUS power supply and change Flash Rom power to DVOA_PWR (3.0V) on Page 6
Change the decoupling cap. C1349,C1350,C1351,C1362,C907 connect to DVOA_PWR from 3.3V on page 5.1
Change the decoupling cap. C1443,C1444,C1445,C1446,C920 connect to DVOA_PWR from 3.3V on page 5.1
Change series P-ROM U505 power to DVOA_PWR (3.0V) on page 5.2
Change GPU pin AH1,AD1,AC7 connect to DVOA_PWR and change GPU pin AH15,AP8,AP12 connect to DVOB_PWR on Page 6.0.
Connection AGND to GND on page 3.1
Remove R1179,R1180,R1183,R1184,R1198,R1199,C1447
Change R1196,R1197 to "NO STUFF" on page 3.2

P80-A04: Schematics For P Release

A04-X00
Put NO_STUUF for C1123, C1126, C1129, C304, C307, C310
Replace C303, C306, C309, C1122, C1125, C1128 with CAP NPO 0603 15PF 16V 5% (035-20150-0006-000)
Replace L715, L717, L719, L300, L305, L309 with IND 0805 MTLR 5% 0.068UH (130-30680-0006-000)
Replace L716, L718, L720, L302, L306, L310 with IND 0603 MTLR 5% 0.068UH (130-20680-0006-000)

A04-X01
Change C29, C30 value from 33PF to 27PF to improve the color burst stability for conexent and philips TV chip
Change R23 to 12 Ohm from 1K Ohm

A04-X02
Clean up the page number

A04-X03
Clean up the Sch. part description mismatch with the BOM

COMMON -- ALL
NO_STUFF - NOT STUFFED
PRI_VGA - Primary VGA Support
PRI_DVI - Primary DVI-D (Digital) Support
PRI_DVI_I - Primary DVI-I - (Digital & Analog) Support
SEC_DVI_I - Secondary DVI-I (Digital & Analog) Support
PRI_PROT - Primary DVI-VGA protection diodes.
SEC_PROT - Secondary DVI-I protection diodes
MEM128 - 128MB EXTENDED MEMORY

NO_STUFF FOR FIRST BUILD
ROM_SER - Serial ROM used
ROM_PAR - Parallel ROM used.

STEREO - USED FOR STEREO GOGGLES
STEREOSYNC1 - USED FOR STEREO GOGGLES
STEREOSYNC2 - USED FOR STEREO GOGGLES
STEREOSYNCS - USED FOR STEREO SYNC BUFFERS
SAA8 - PHILIPS ENCODER/DECODER SAA7108
SAA2 - PHILIPS ENCODER SAA7102
CX - CONEXENT ENCODER CX25871


NO_STUFF FOR FIRST BUILD
EZ1586 - USED TO REGULATE FBVDDQ FROM FBVDD - LINEAR
SC1102 - USED TO REGULATE FBVDD FROM 12V - SWITCHER
SC1165 - USED TO REGULATE 3.3VL FROM 3.3V - LINEAR
SC1175 - USED TO REGULATE NVVDD FROM 3.3V AND 5V - SWITCHER

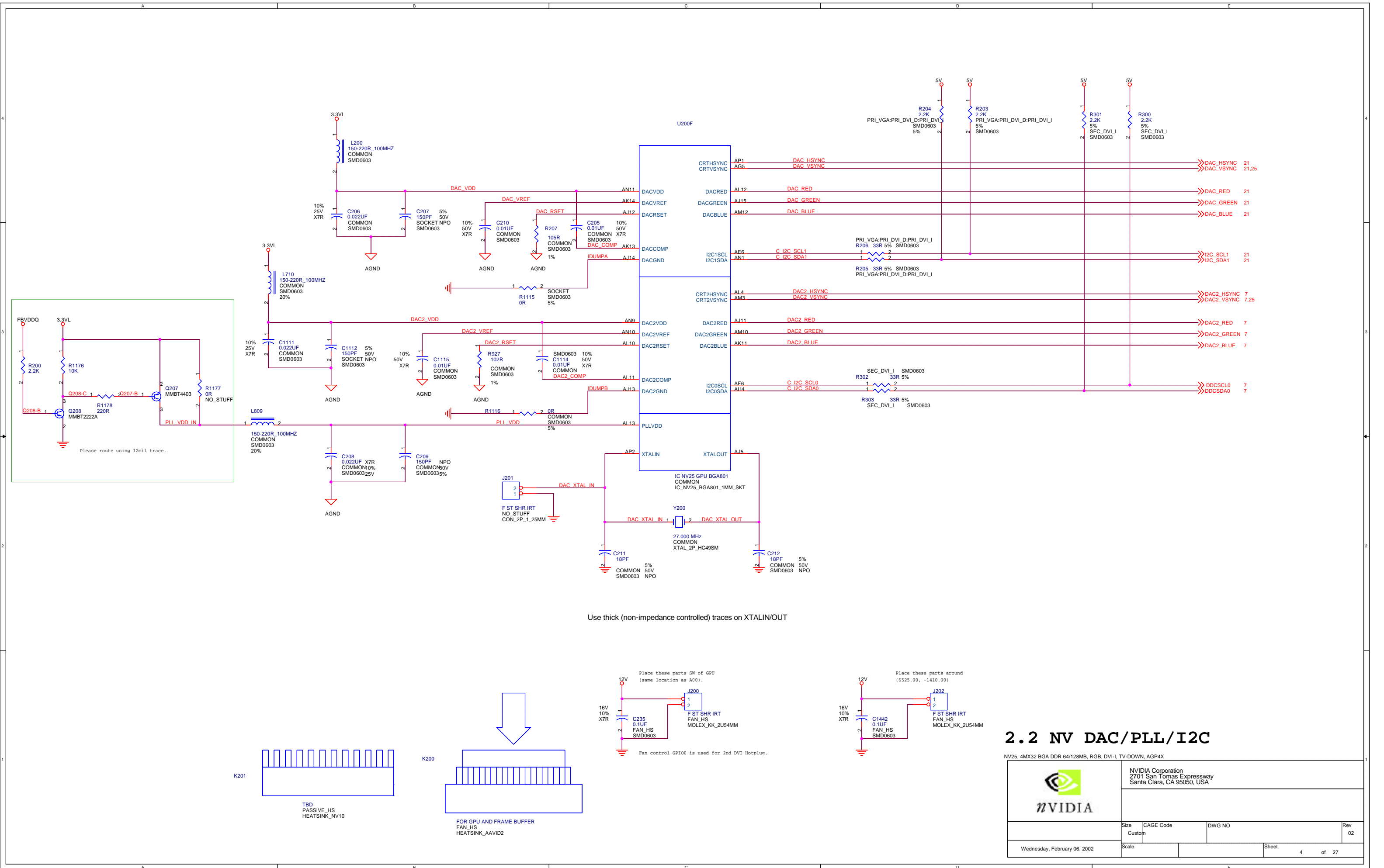
NO_STUFF FOR FIRST BUILD
PS_SEQ - USED FOR POWER SUPPLY SEQUENCE PROTECTION

VGA-TV-DVI - Used for Primary VGA / TV / Secondary DVI
VGA-DVI - Used for Primary VGA / Secodary DVI only
VGA-TV - Used for Primary VGA / TV
VGA - Used for Primary VGA only
DVI-TV-DVI - Used for Primary DVI / TV / Secondary DVI
DVI-DVI - Used for Primary DVI / Secondary DVI Only
DVI-TV - Used for Primary DVI / TV
DVI - Used for Secondary DVI
PASSIVE_HS - Used for Passive heat sink
FAN_HS - Used for Fan heat Sink
SOCKET - PARTS REMOVED WHEN USING A SOCKET

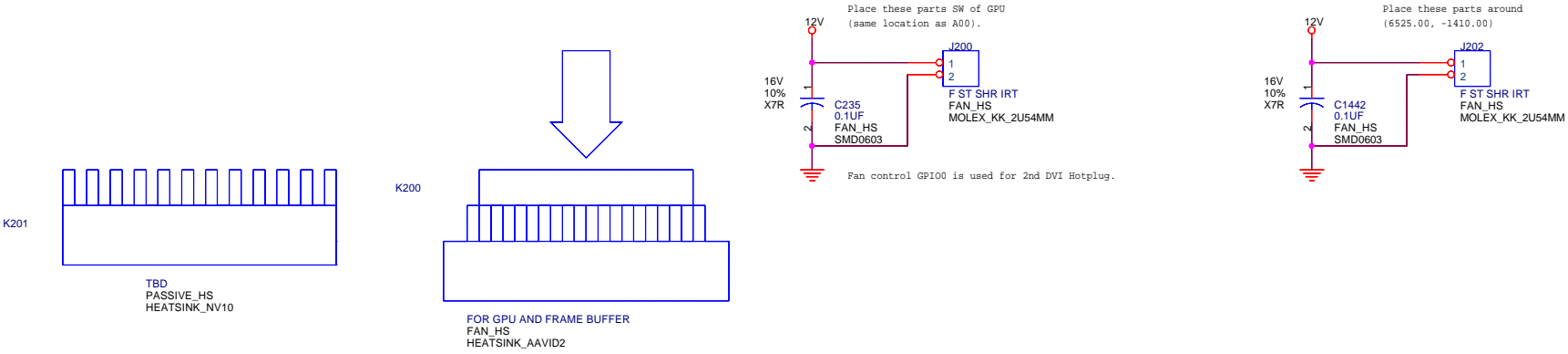
0. TOP PAGE

NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

 NVIDIA	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA			
	602-P0080-0000-A04			
	Size Custom	CAGE Code	DWG NO	Rev 02
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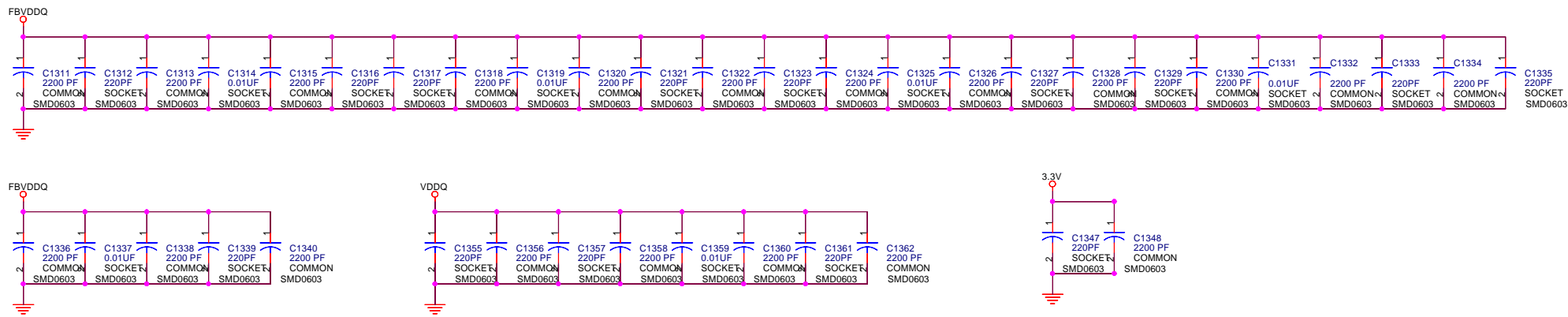


Use thick (non-impedance controlled) traces on XTALIN/OUT

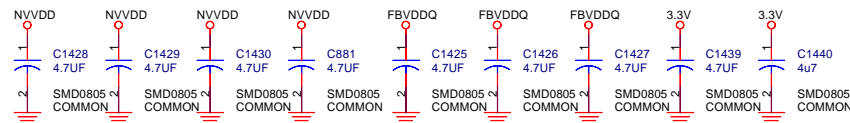


2.2 NV DAC/PLL/I2C

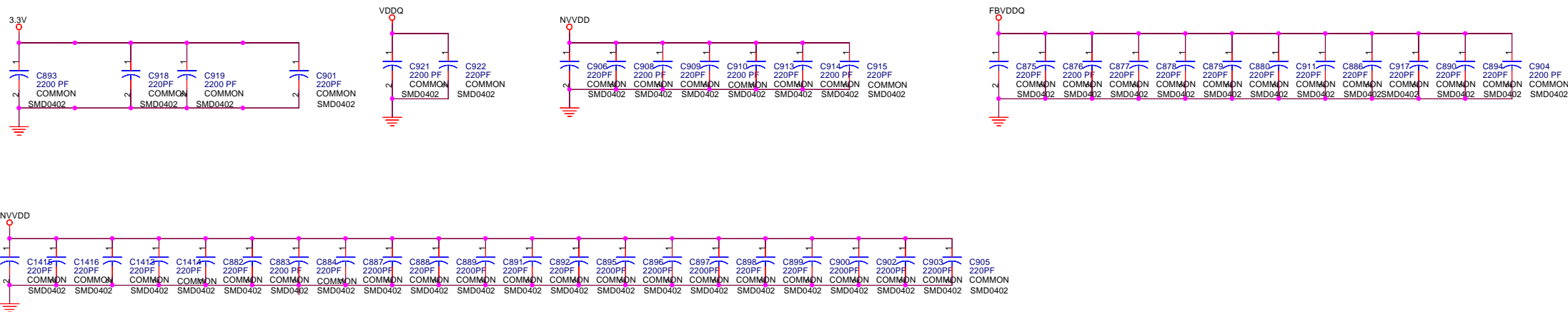
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TOP SIDE CAPS



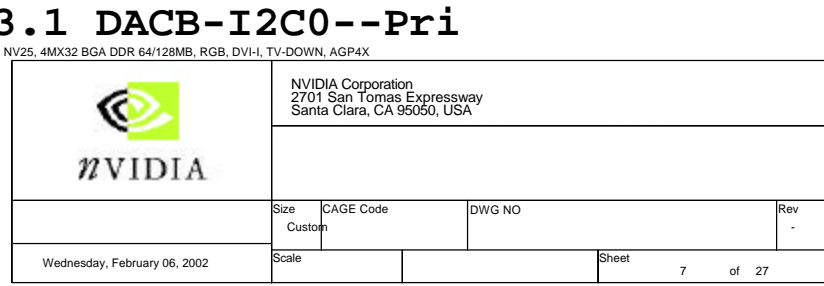
BOT SIDE CAPS



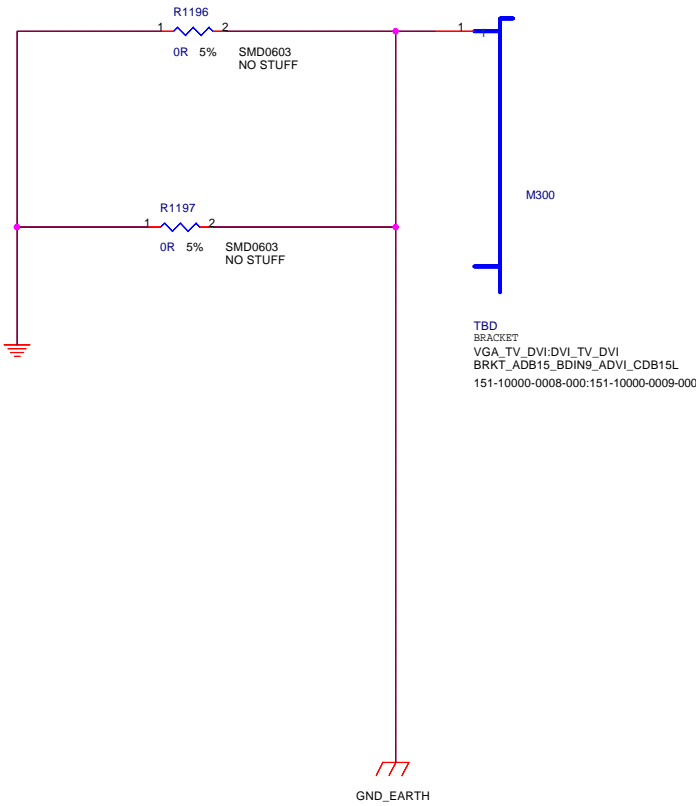
2.3 NV DECOUPLING

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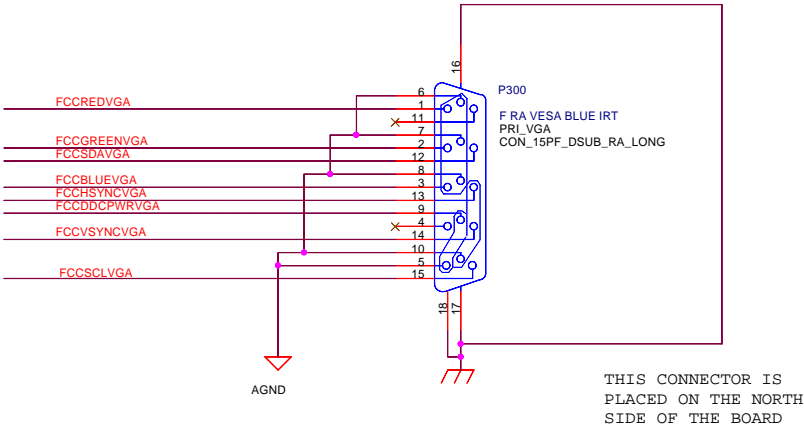
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Single point connection for digital and chassis GND.



VGA-TV-DVI - Used for Primary VGA / TV / Secondary DVI
DVI-TV-DVI - Used for Primary DVI / TV / Secondary DVI




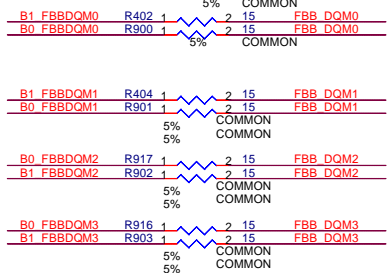
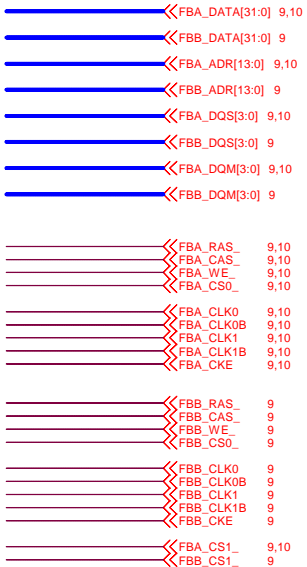
FCCDDCPWRVGA 7,19,21,22,25
FCCBLUEVGA 7,19
FCCGREENVGA 7,19
FCCREDVGA 7,19
FCCSCLVGA 7,19
FCCSDAVGA 7,19
FCCHSYNCSVGA 7,19
FCCVSYNCSVGA 7,19

3.2 VGA CON, BRACKET

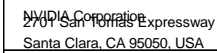
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NV25 4MX32 BGA DDR 64/128MB RGB DVI-I TV-DOWN AGP4X



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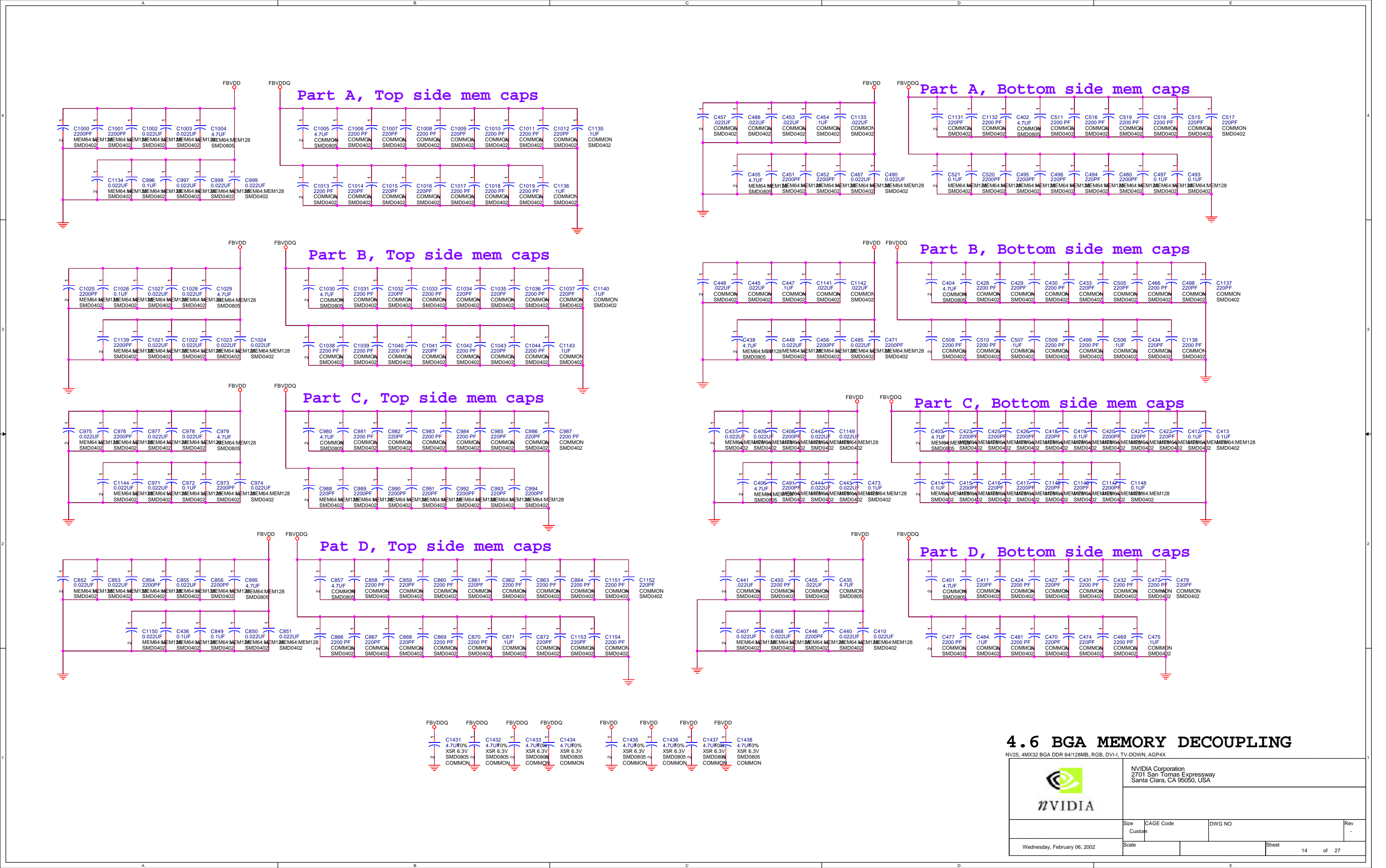
Part D, Bottom side memory

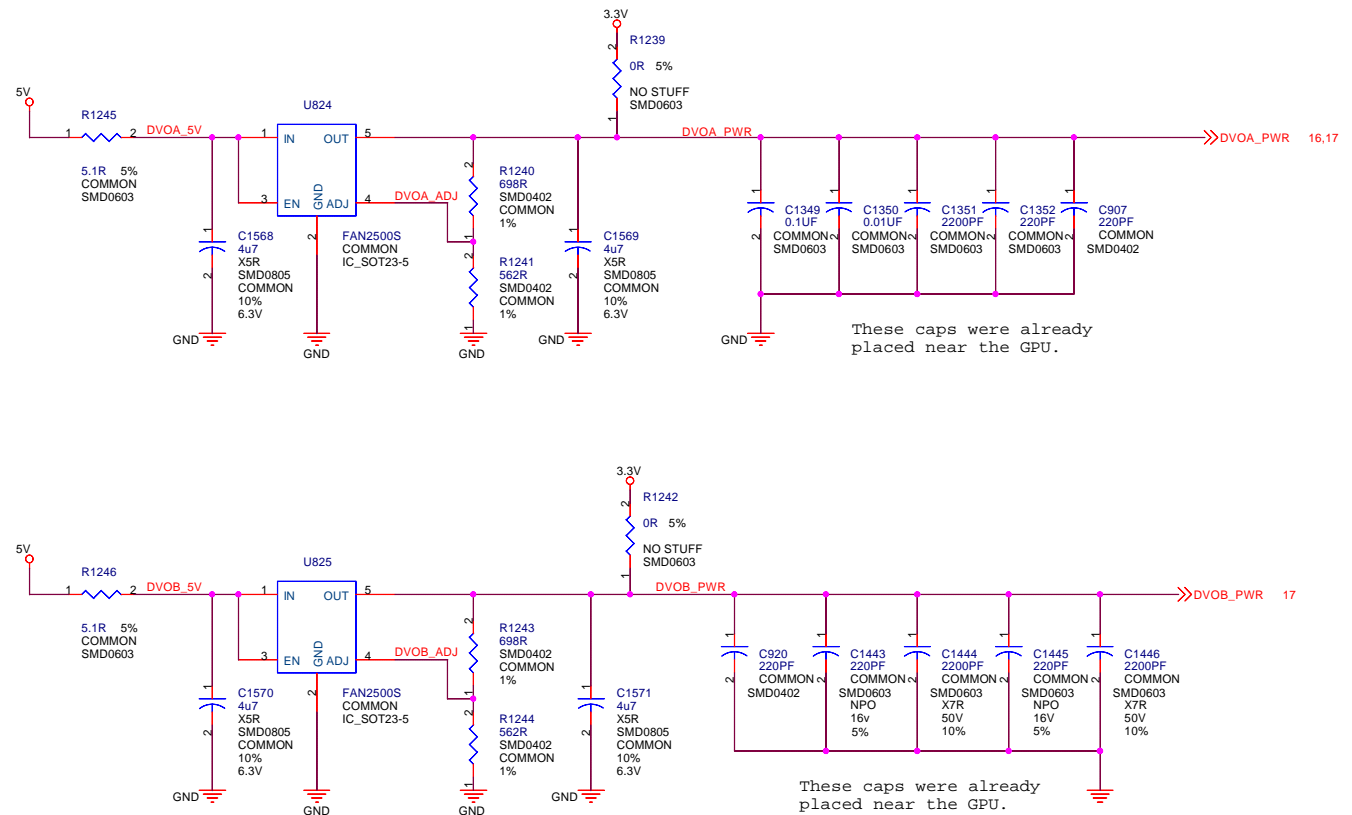


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5.2 S-ROM

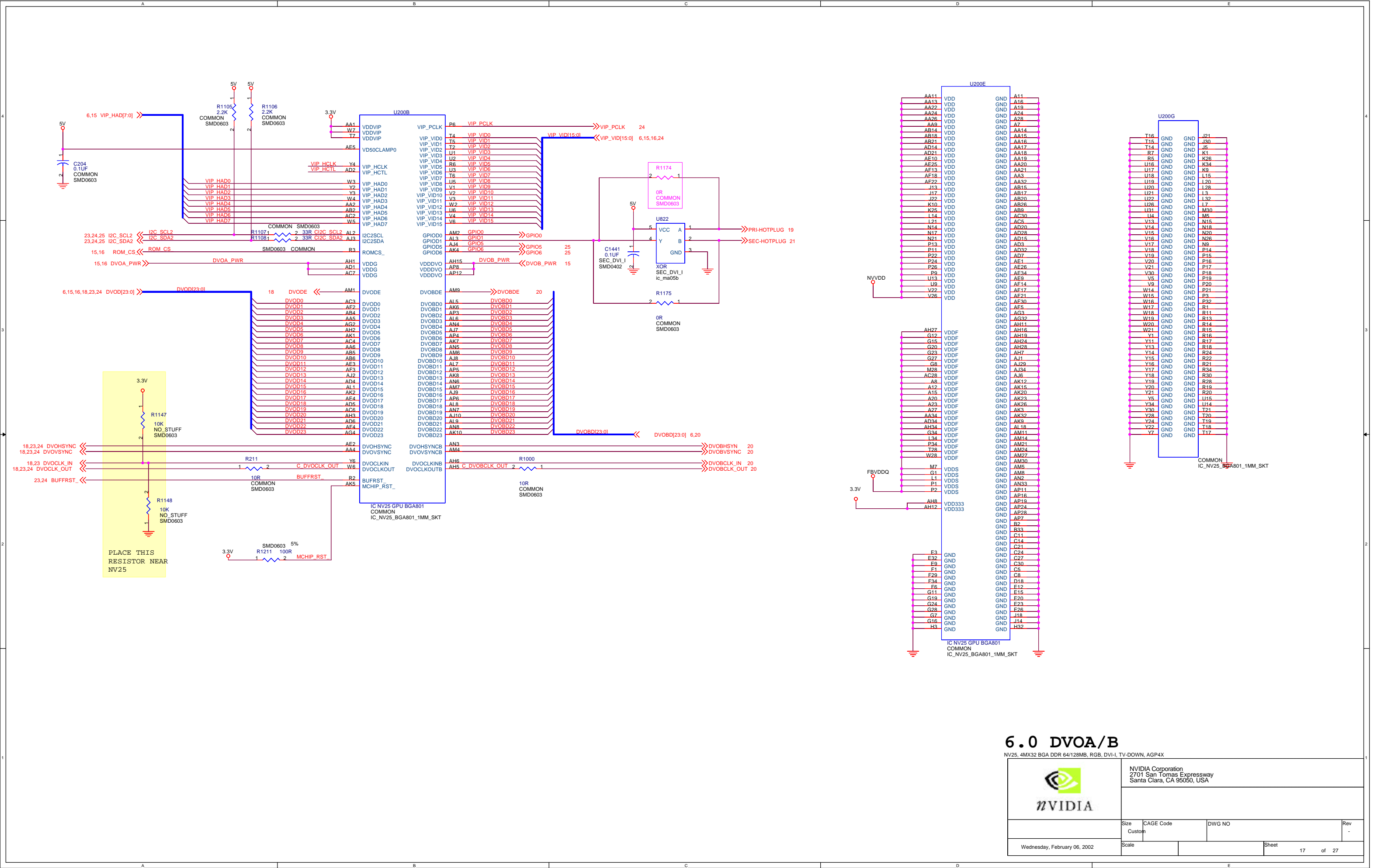
NV20, 4MX32 BGA DDR 32MB, RGB, DVI-I, TV-DOWN, TV I/F, AGP4X

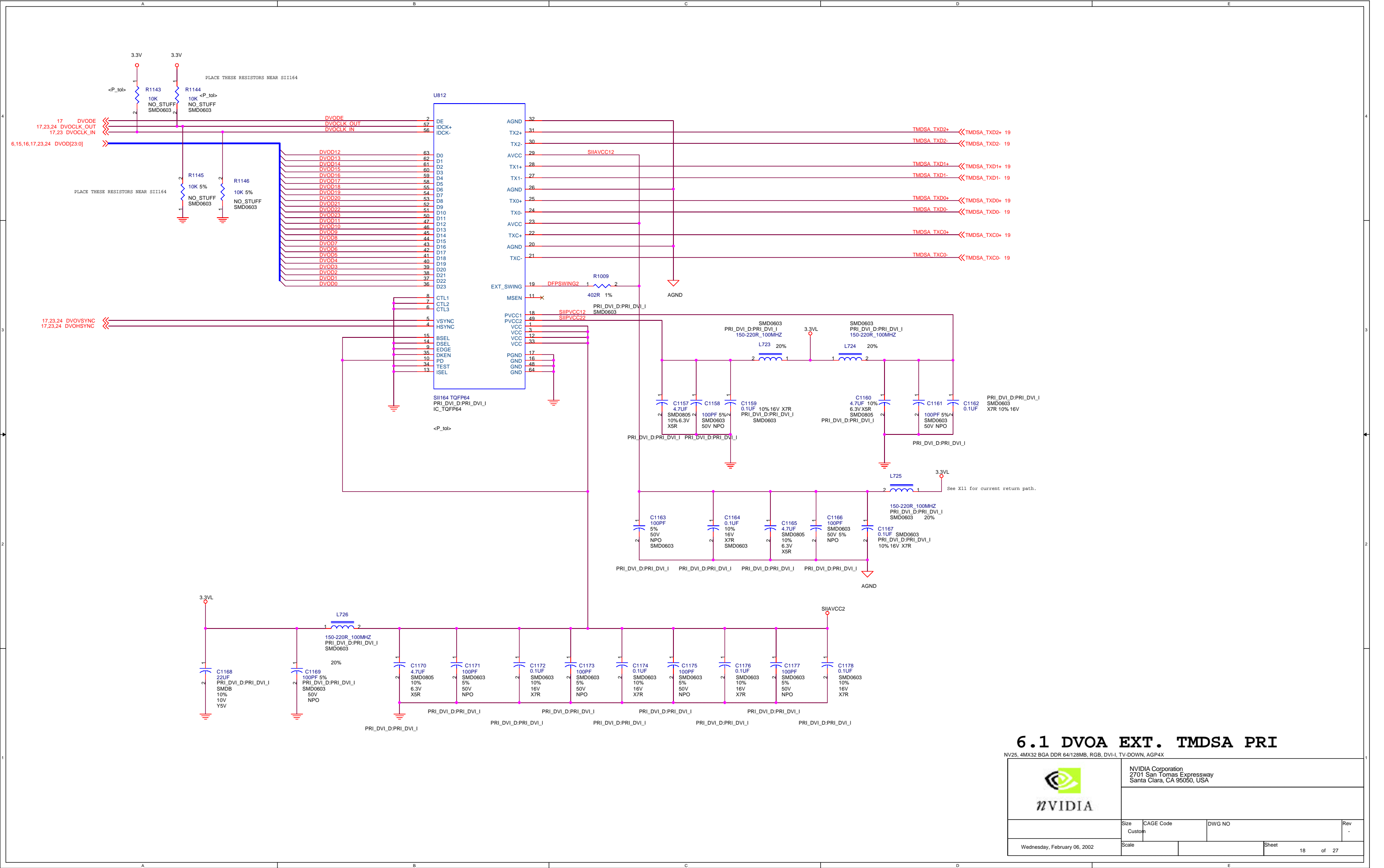


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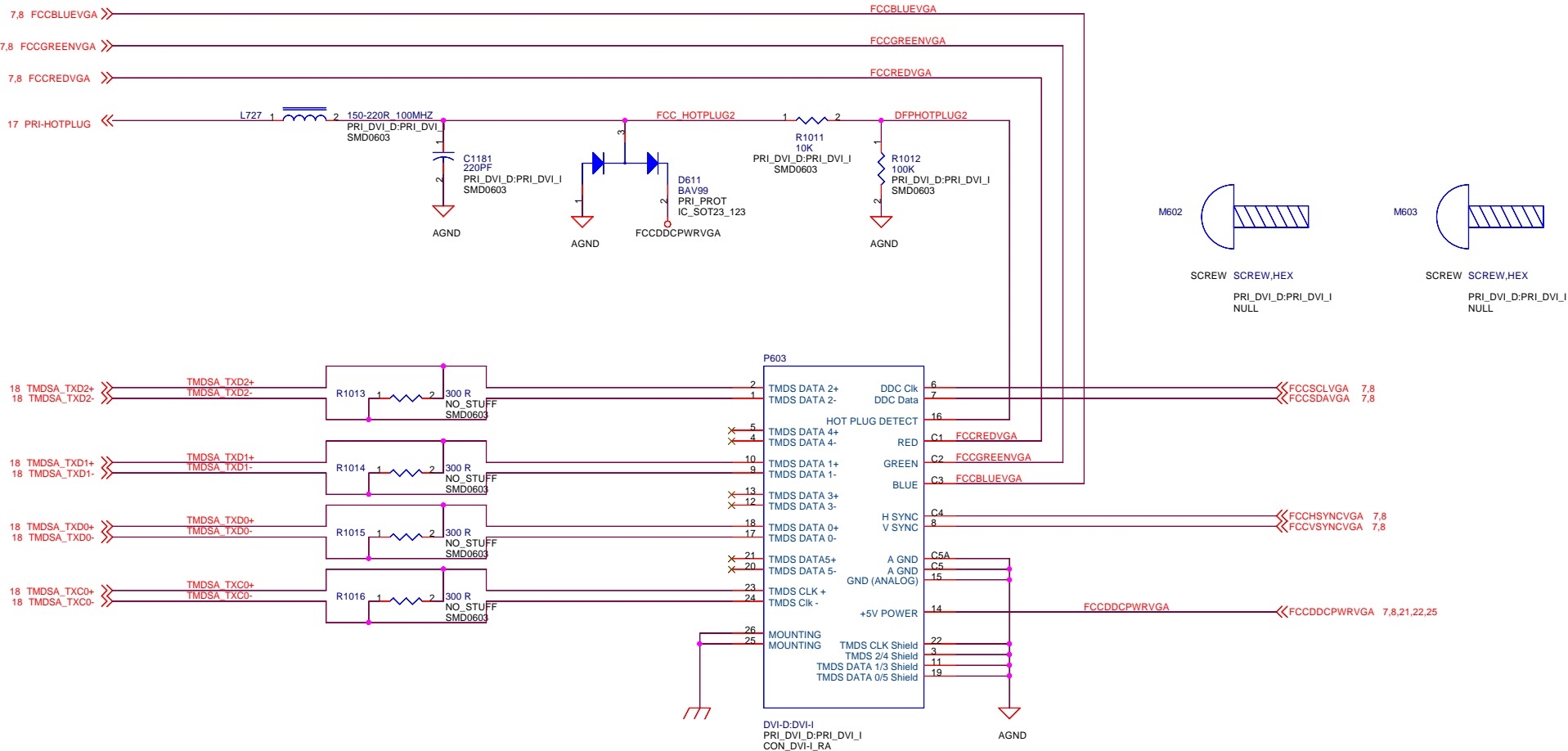




6.1 DVOA EXT. TMDSA PRI


NV25, 4MX32 BGA DDR 64/128MB, RGB, DVI-I, TV-DOWN, AGP4X

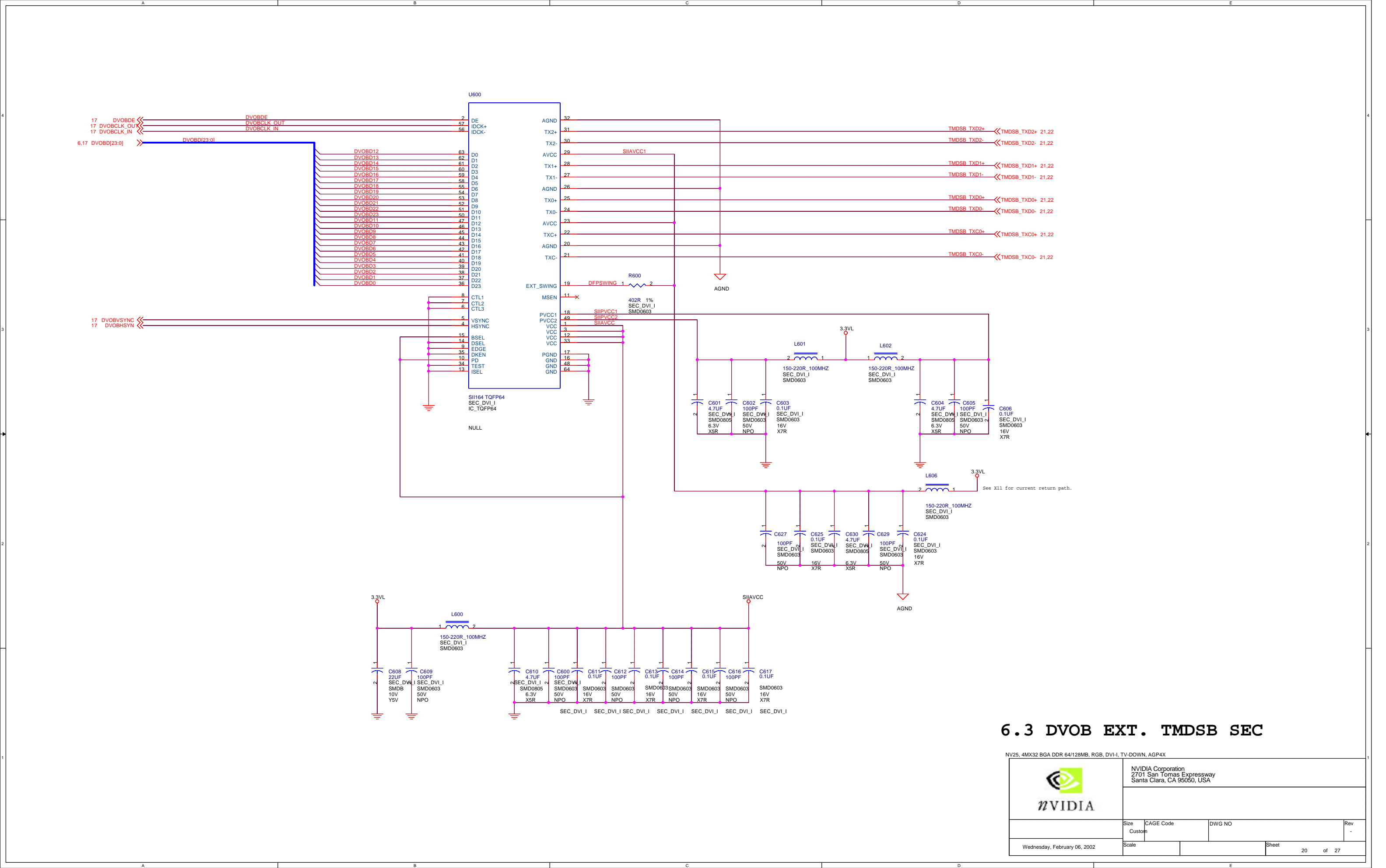
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6.2 DVOA EXT. TMDSA I/O PRI

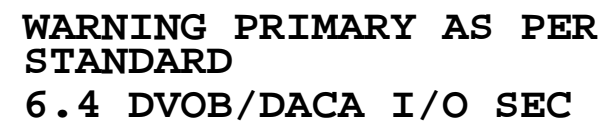
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6.3 DVOB EXT. TMDSB SEC

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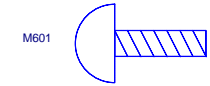
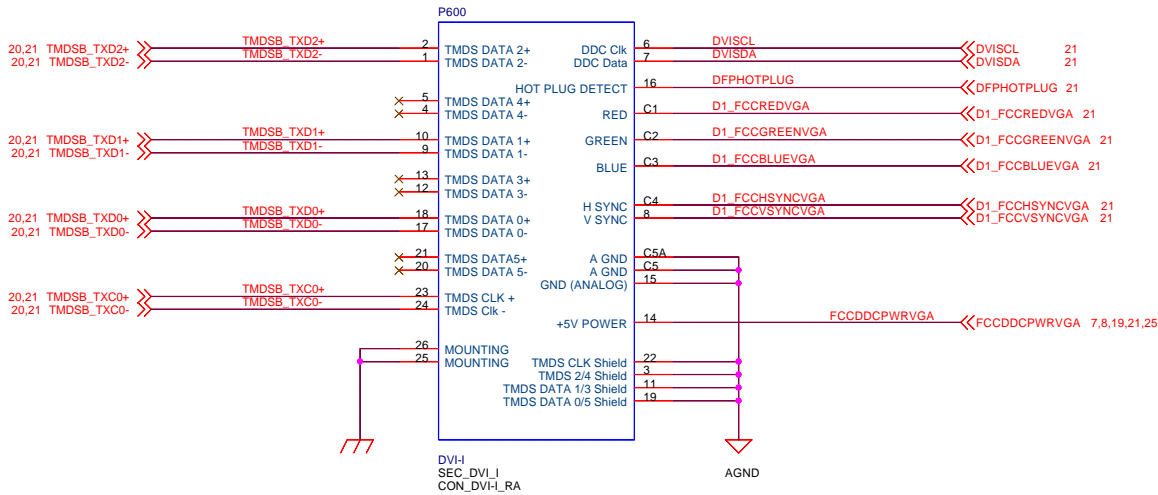


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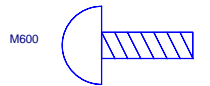


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SCREW SCREW,HEX
SEC_DVI_I
NULL

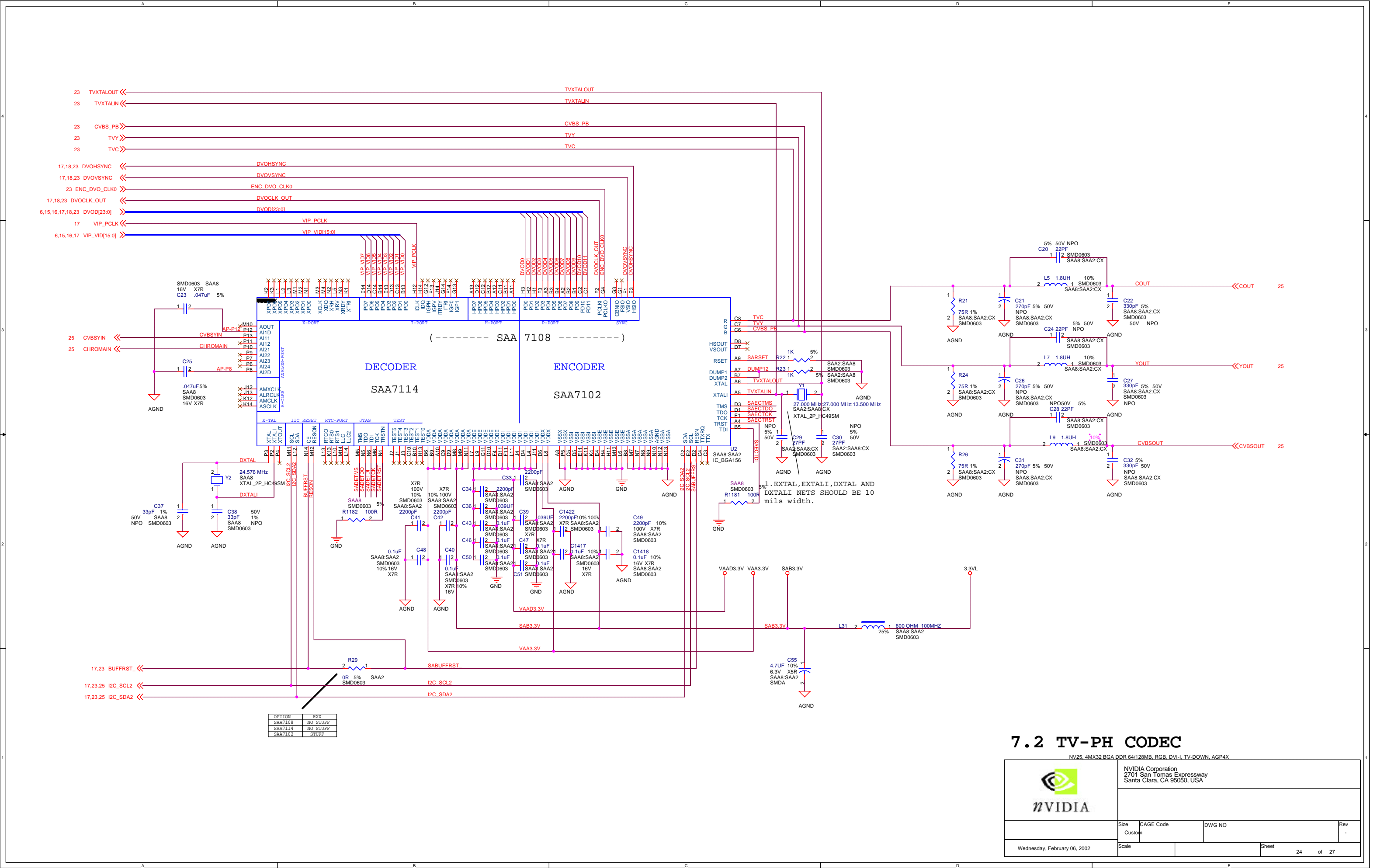


SCREW SCREW,HEX
SEC_DVI_I
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WARNING PRIMARY AS PER STANDARD 6.5 DVOB/DACA CONNECTOR

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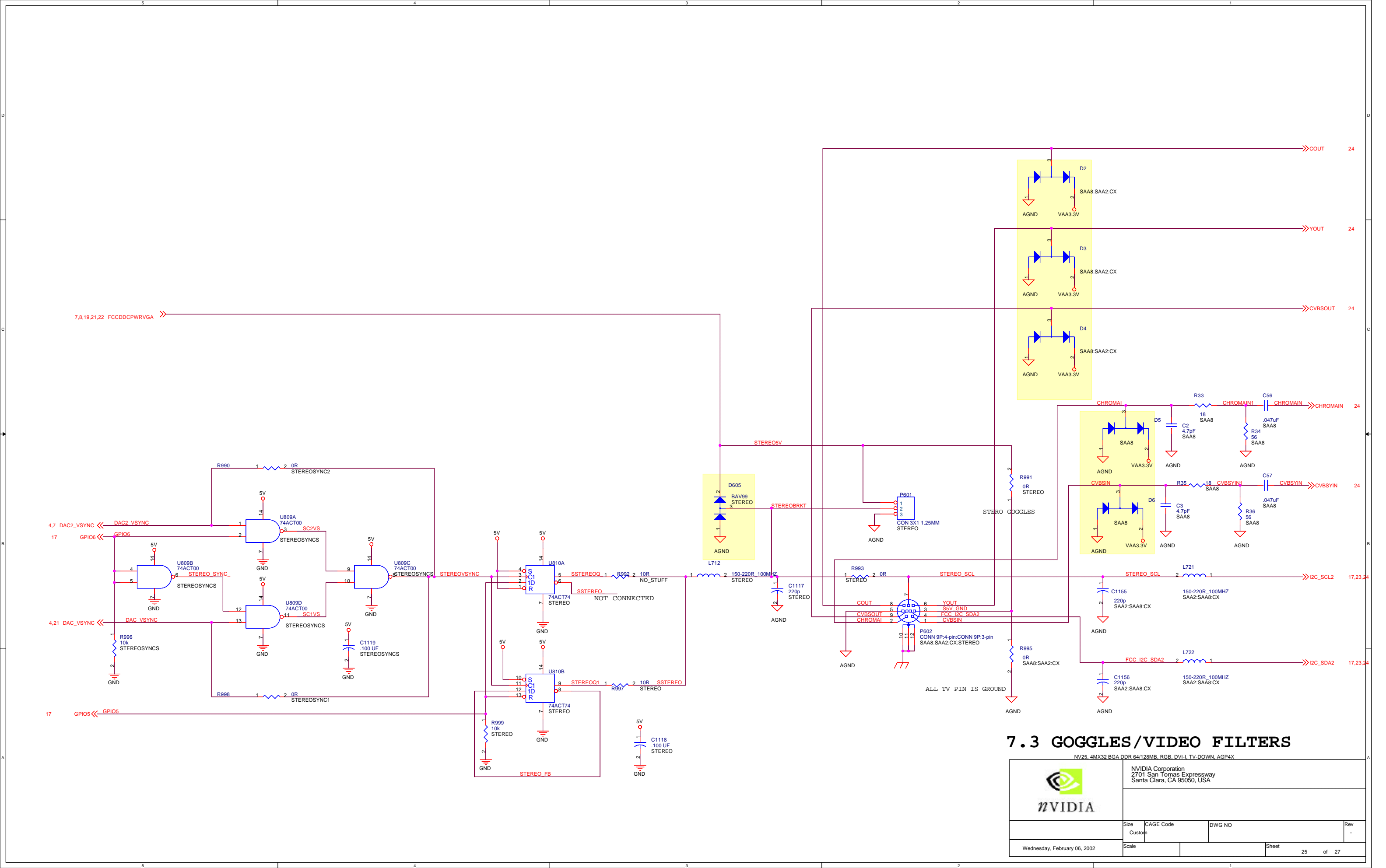
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7.2 TV-PH CODEC


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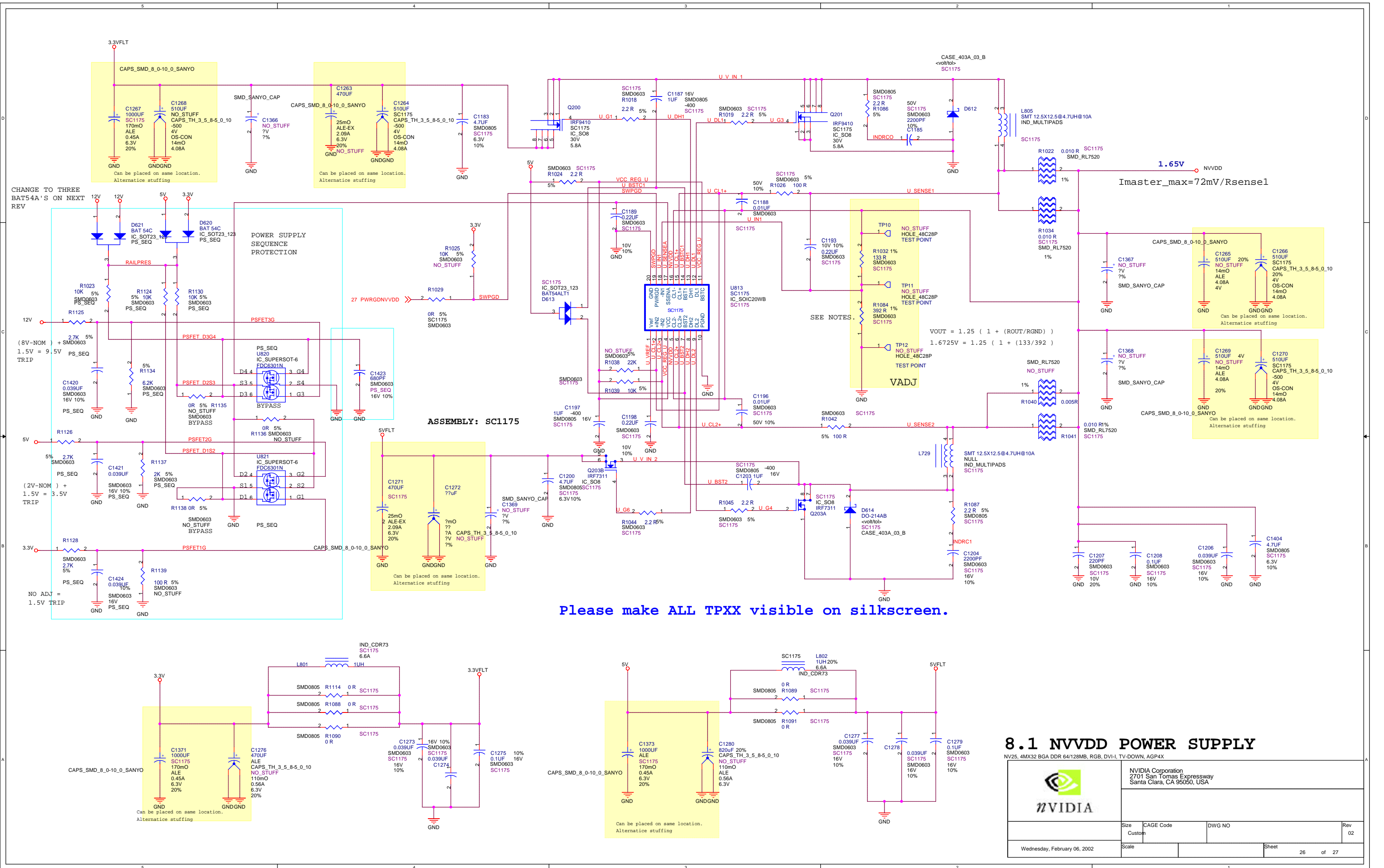
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7.3 GOGGLES/VIDEO FILTERS


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Please make ALL TPXX visible on silkscreen.

8.1 NVDD POWER SUPPLY

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