P654 - GT200/NVIO2

P654, GT200-100, 896MB/1792MB - GDDR3 BGA136 16M/32Mx32

DVI-I + DVI-I/DP + HD/SD/TVout, SPDIF, Dual SLI

Table of Contents

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10654-BASE-A03	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU00000	600-10654-0000-000	DT, GT200-100, 550/1350/1000, 896MB - 16Mx32 GDDR3, DVI-I + DVI-I + HDTV
2	SKU00001	600-10654-0001-000	DT, GT200-100, 550/1350/1000, 896MB - 16Mx32 GDDR3, DVI-I + DP + HDTV
3	SKU0051	600-10654-0051-300	DT, GT200B-103, 576/1242/1000, 896MB - 16MX32 GDDR3, DVI-I + DVI-I
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MS-V180 -0A

PAGE 21:VGS SLIM
PAGE-22 remove DACB HDTV Circuit
PAGE 24:DVI change HDMI
PAGE 25:DP modify DSDA/DSCL circuit
PAGE 28:ADD I2C0_SCL/SDA and GPIO 3 circuit,remove GPIO 12
PAGE 29:remove R112,R113 and GPIO8_FAN_TACH link to U21
PAGE 33:remove R671,R572
PAGE 35:remove RT8805CQVA change UPI6205 and UPI6262 circuit
PAGE 36:remove NCP5388MNR2G change UPI6208 circuit
PAGE 37/38 :remove NCP3418B change UPI6281 circuit
PAGE 39 :Add WL83L786G circuit

MS-V180 -10

1.PAGE 37,38 modify D15~D21 footprint
2..PAGE 37,38 add CAP

MS-V180 -20

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Title Page

Micro-Star International Co., LTD.

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Block Diagram

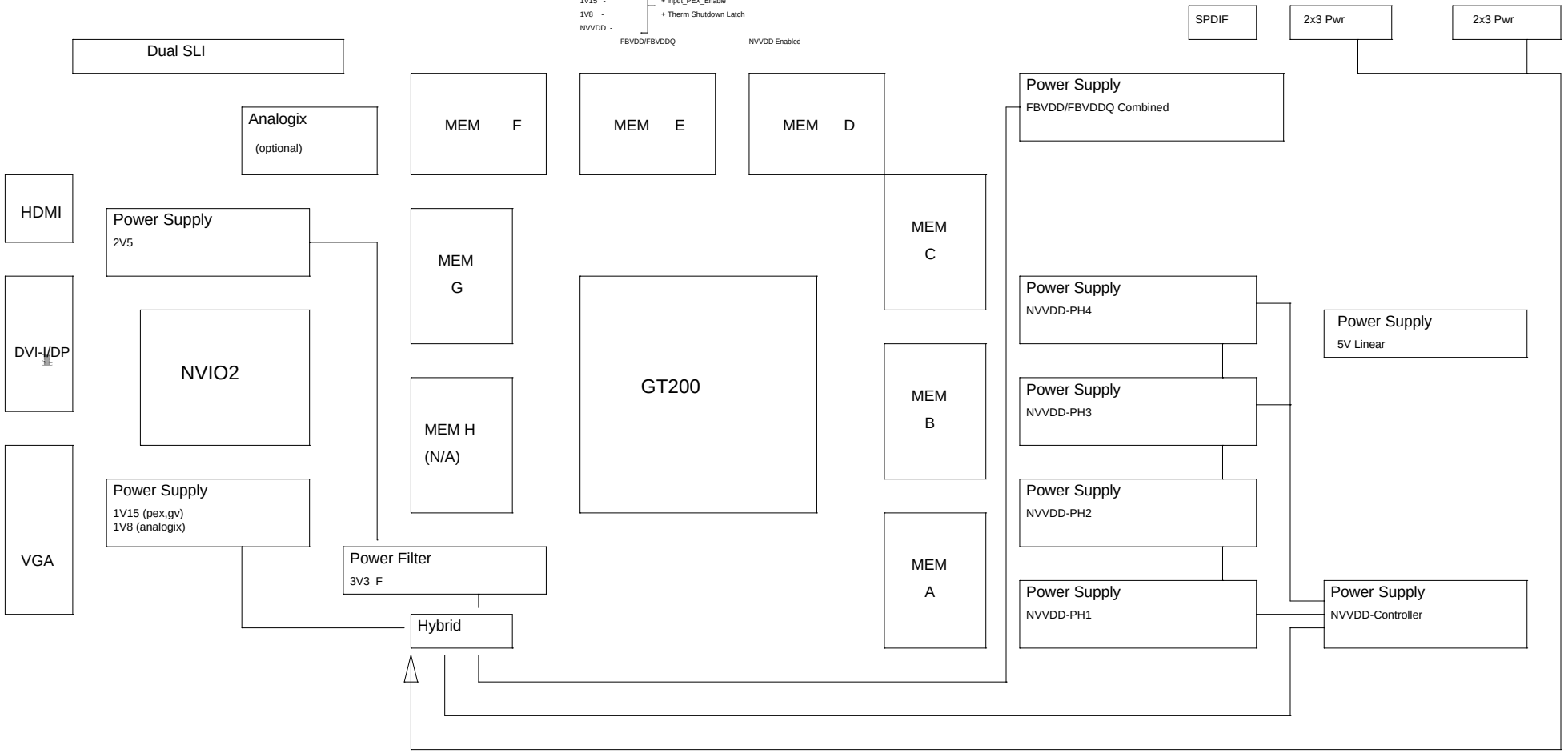
Power Sequence

5V - Always On
3V3 - Always On
12V_F - Always On
12V_PEX6_F1 - Always On
12V_PEX6_F2 - Always On
3V3_DP - Always On

3V3_F -
2V5 -
1V15 -
1V8 -
NVVDD -
FBVDD/FBVDDQ -

Hybrid Enable
+ Input_PEX_Enable
+ Therm Shutdown Latch

NVVDD Enabled



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PAGE DETAIL	Block Diagram

Micro-Star International Co., LTD.

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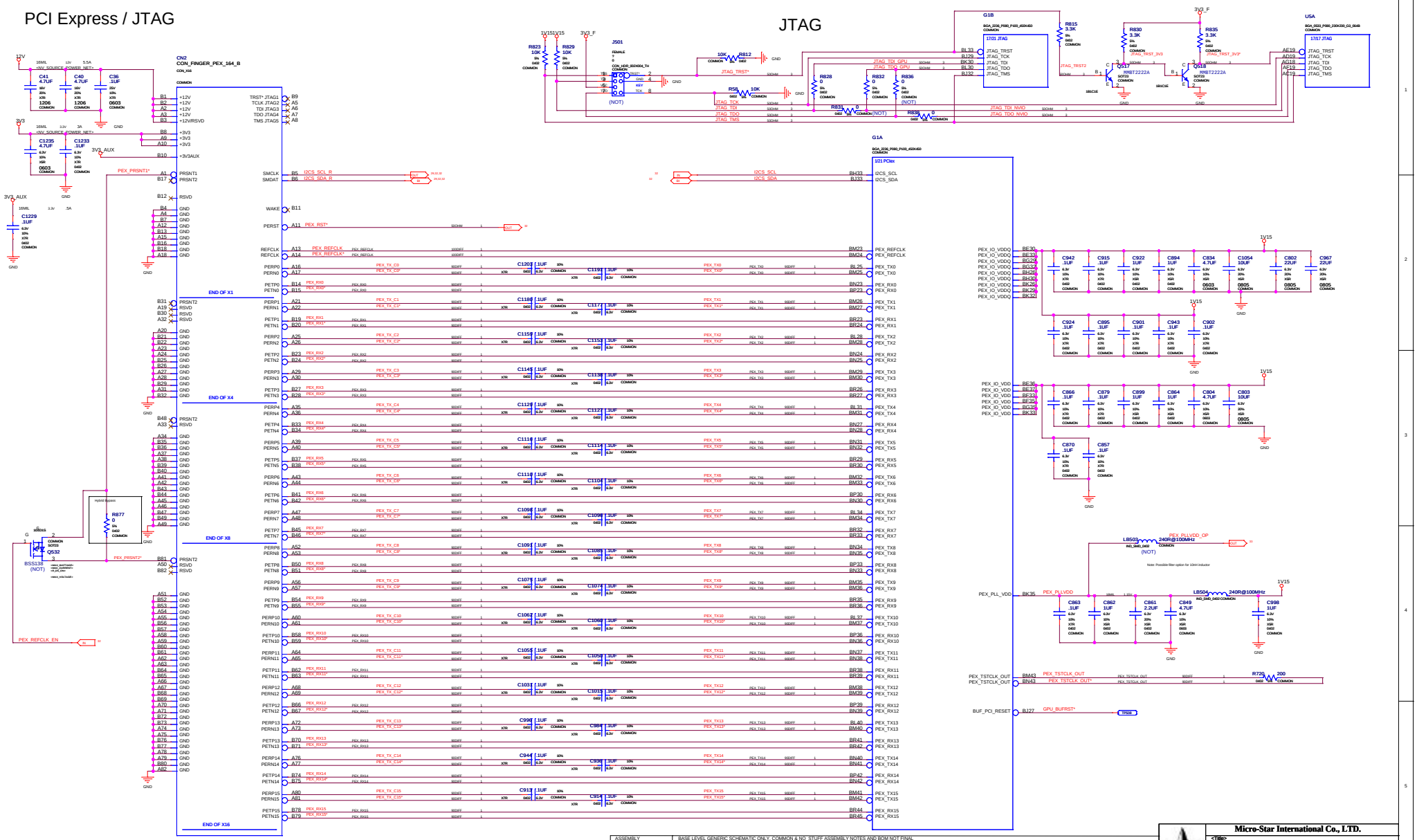
PCI Express / JTAG



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PAGE DETAIL	PCI Express / JTAG

Micro-Star International Co., LTD.

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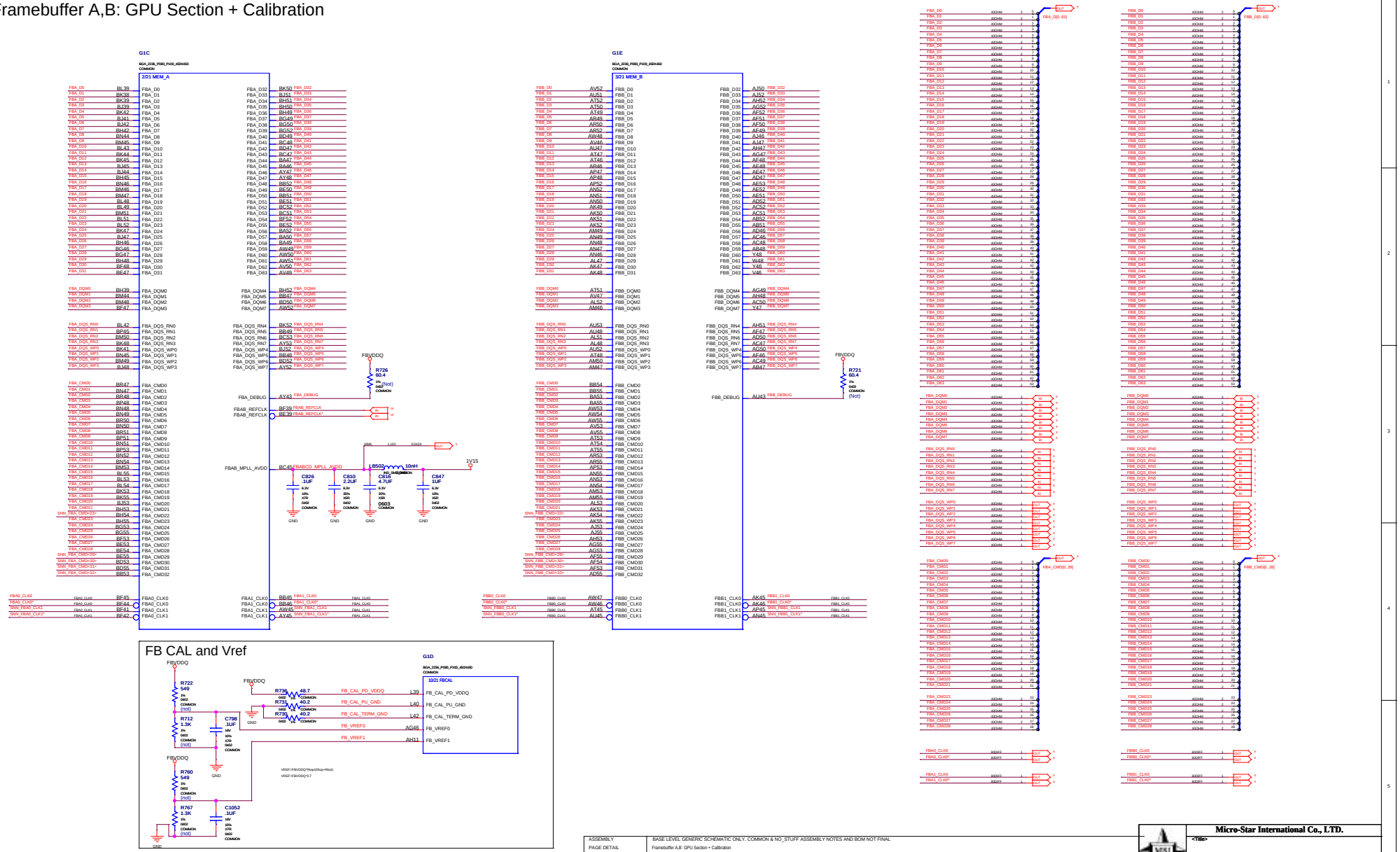
Framebuffer A,B: GPU Section + Calibration



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PAGE DETAIL	Framebuffer A,B: GPU Section + Calibration

Micro-Star International Co., LTD.	
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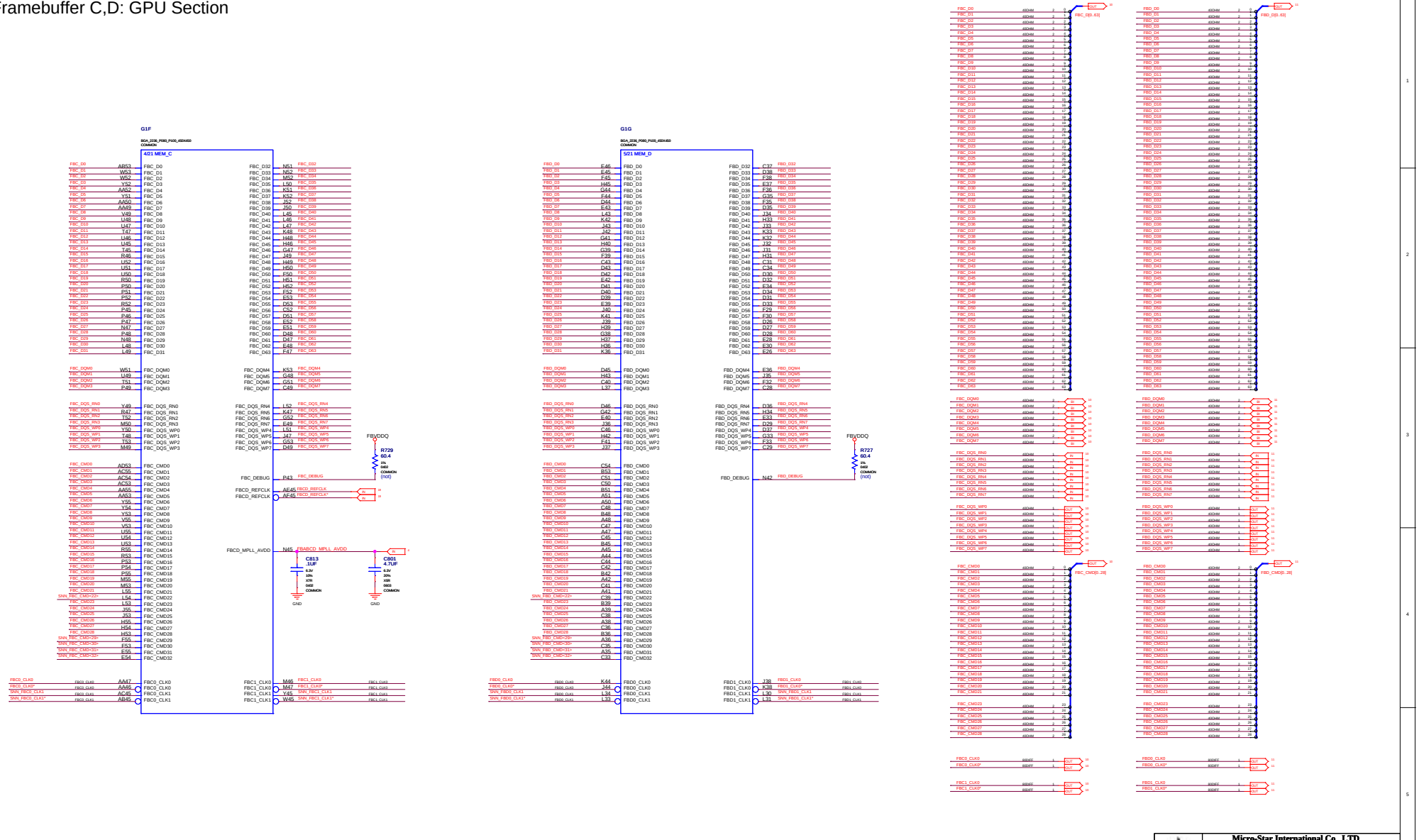
Framebuffer C,D: GPU Section



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PAGE DETAIL	Framebuffer C,D: GPU Section

Micro-Star International Co., LTD.

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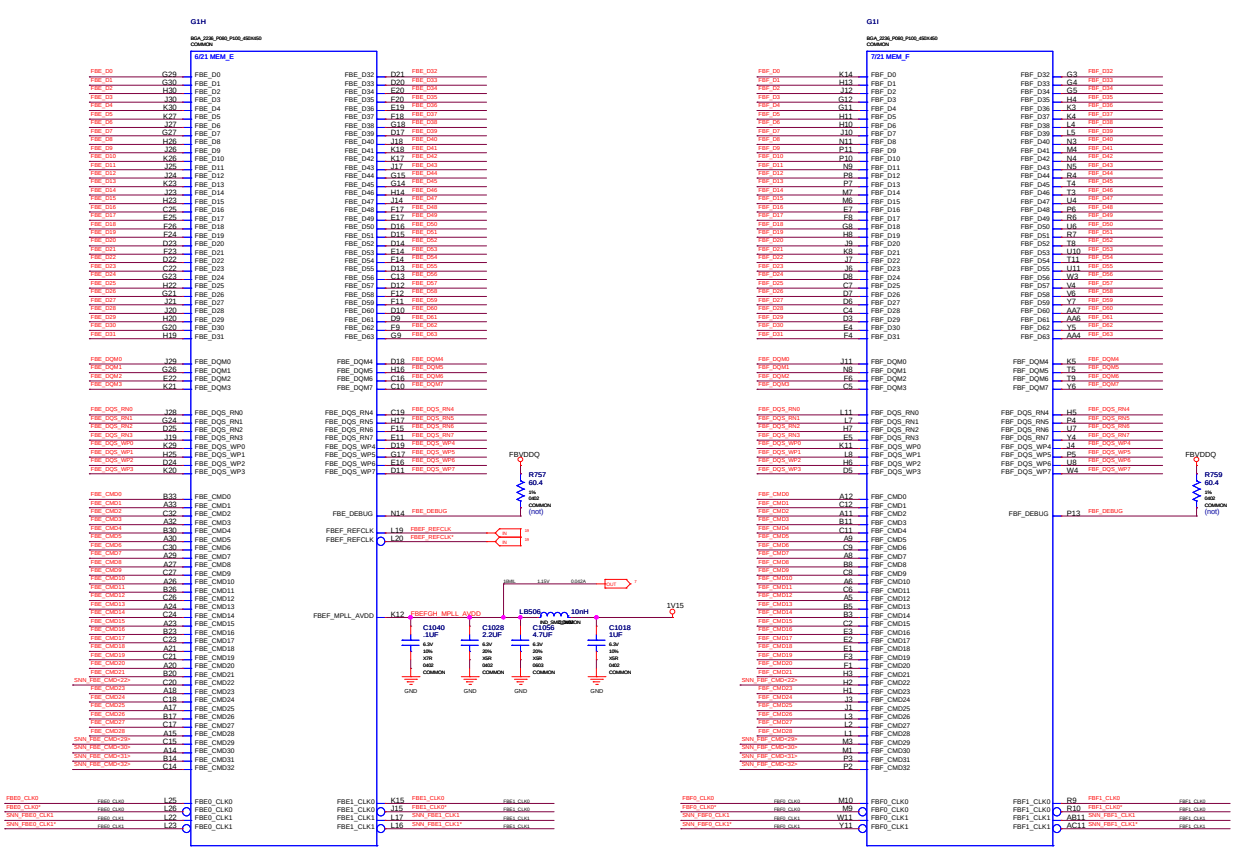
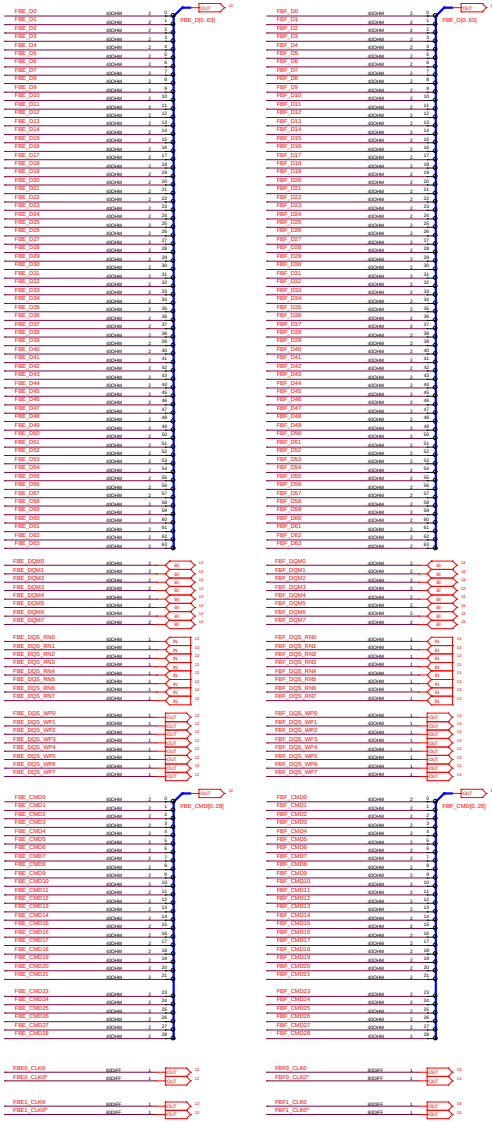
Framebuffer E,F: GPU Section





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PAGE DETAIL	Framebuffer E,F: GPU Section

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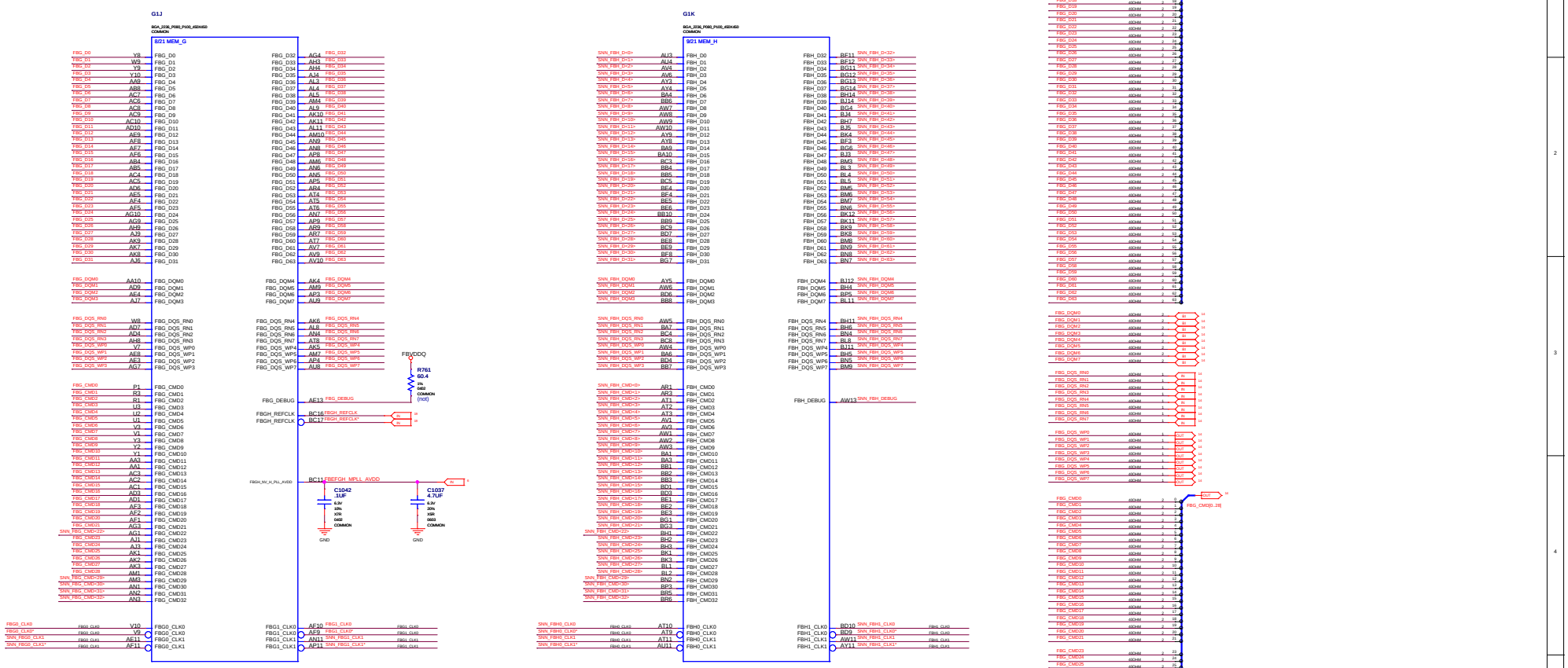
Framebuffer G,H: GPU Section



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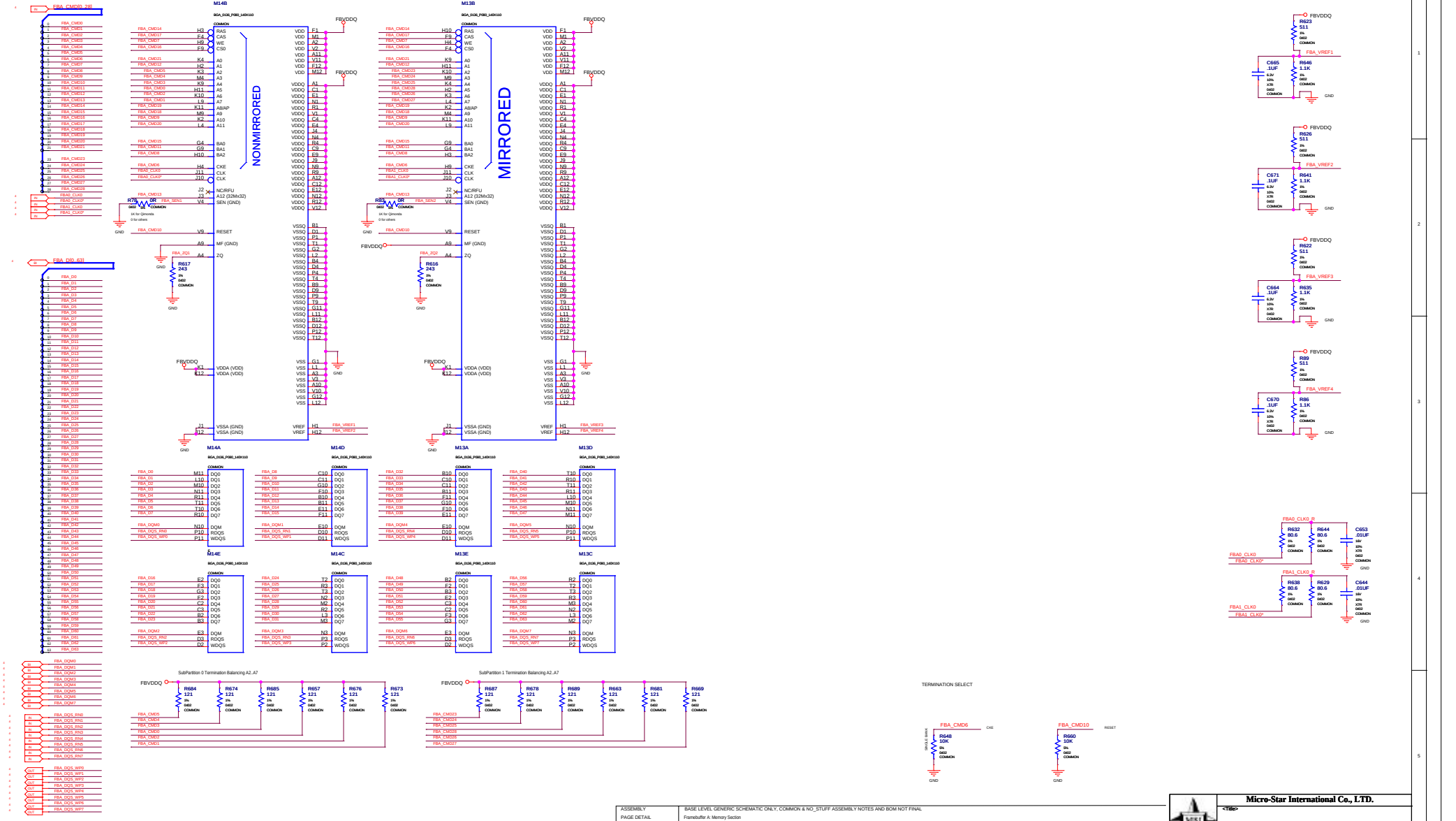
Framebuffer A: Memory Section



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Micro-Star International Co., LTD.

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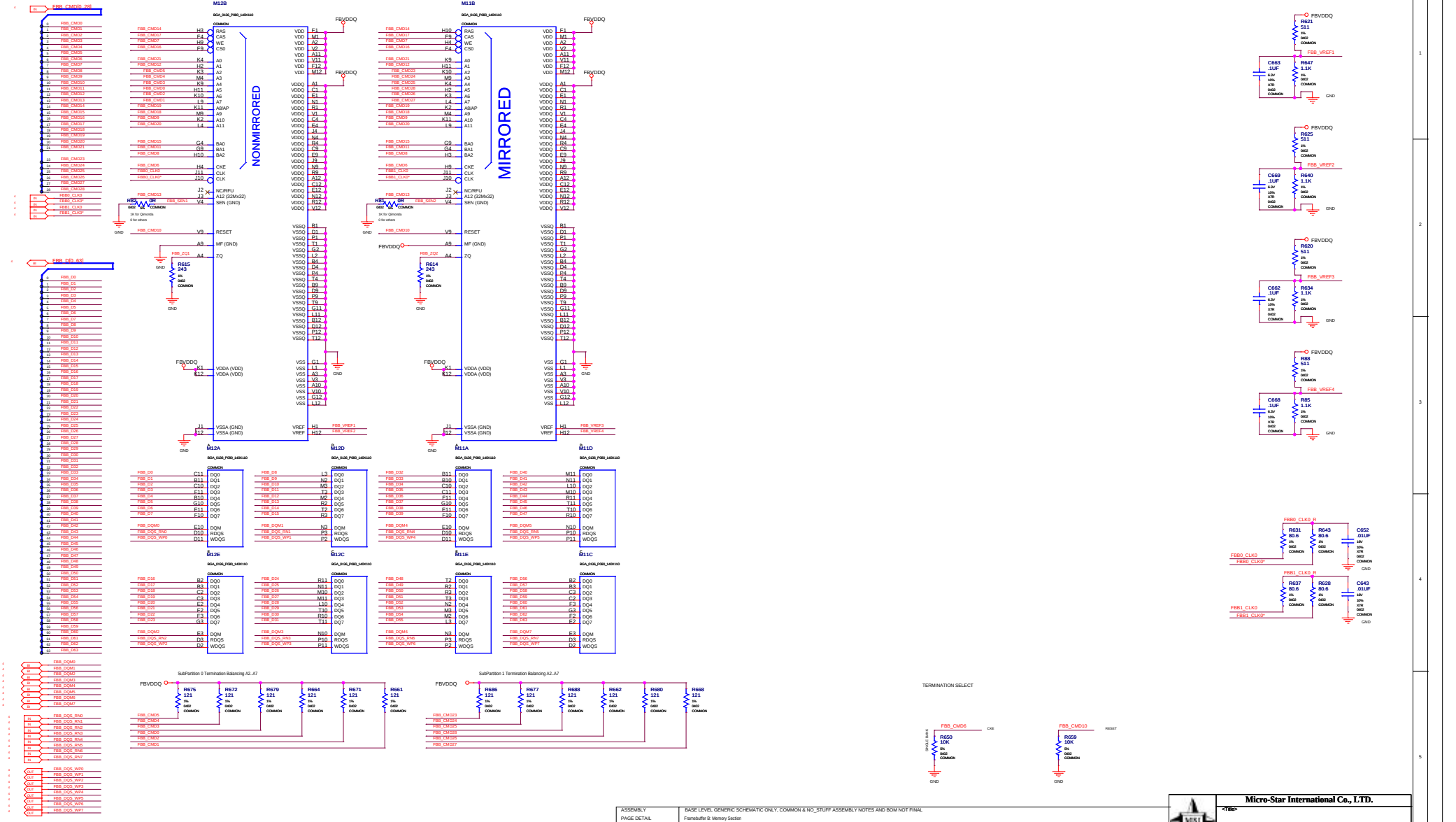
Framebuffer B: Memory Section



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Micro-Star International Co., LTD.

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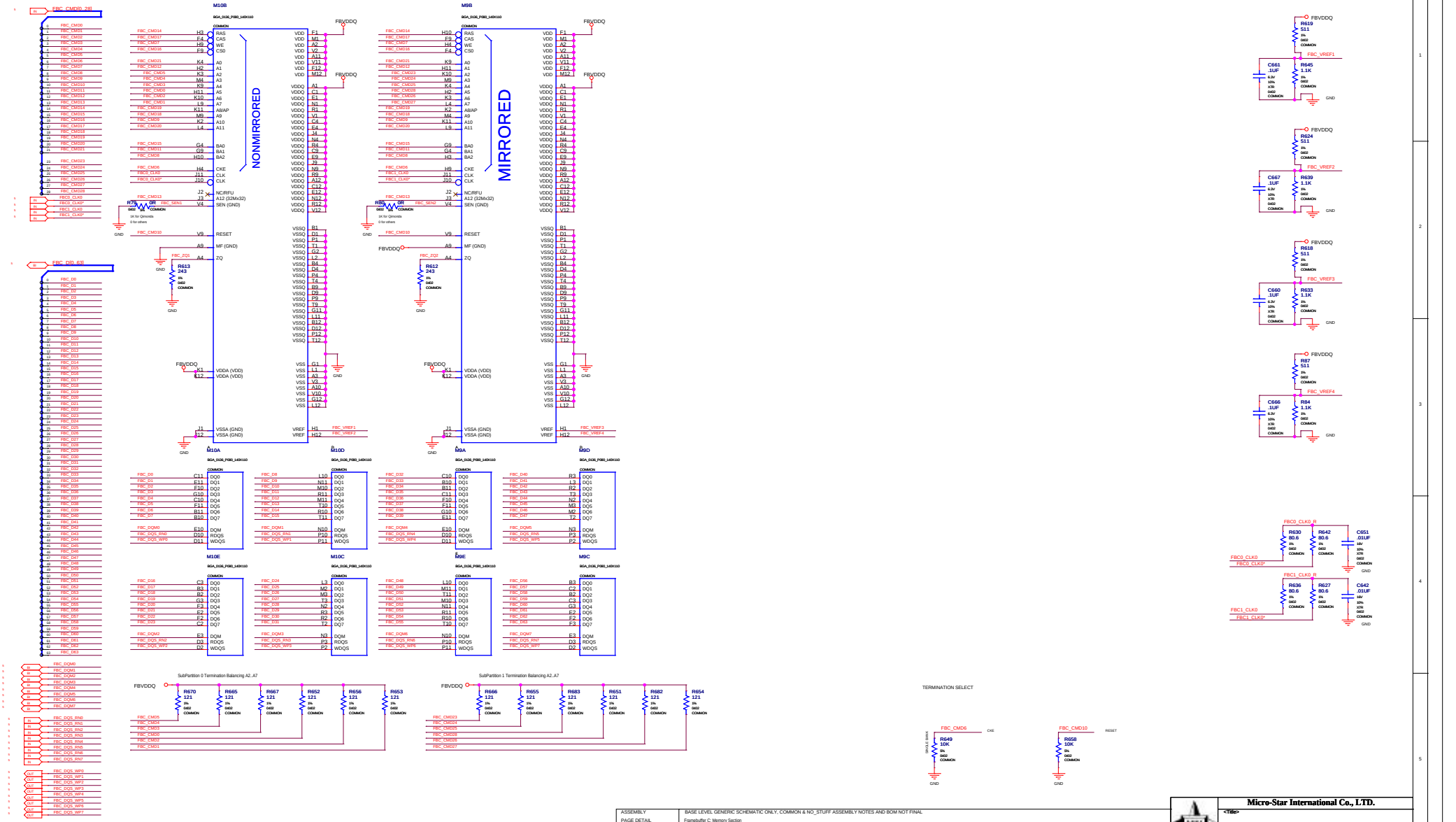
Framebuffer C: Memory Section



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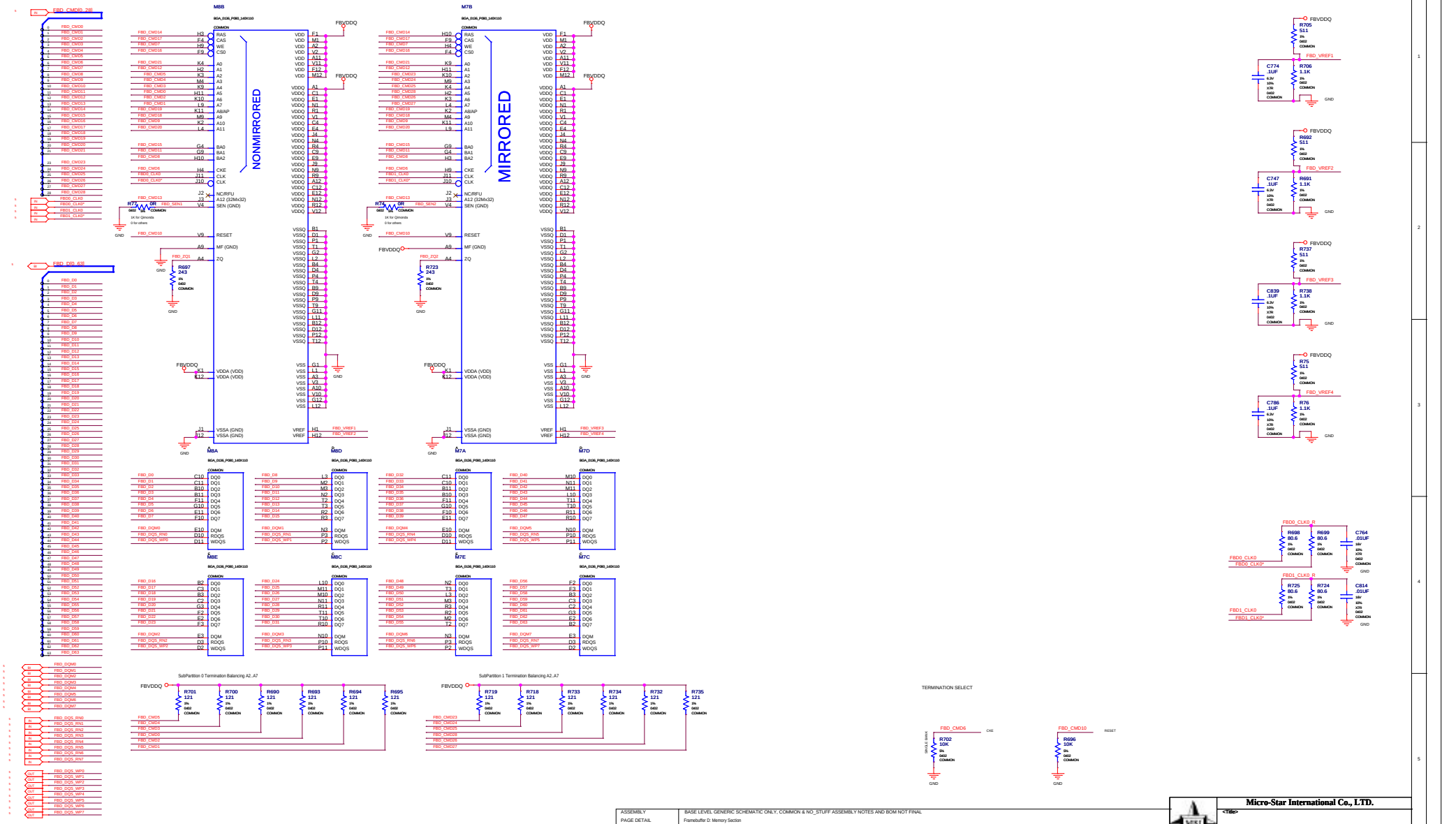
Framebuffer D: Memory Section



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PAGE DETAIL	Framebuffer D: Memory Section

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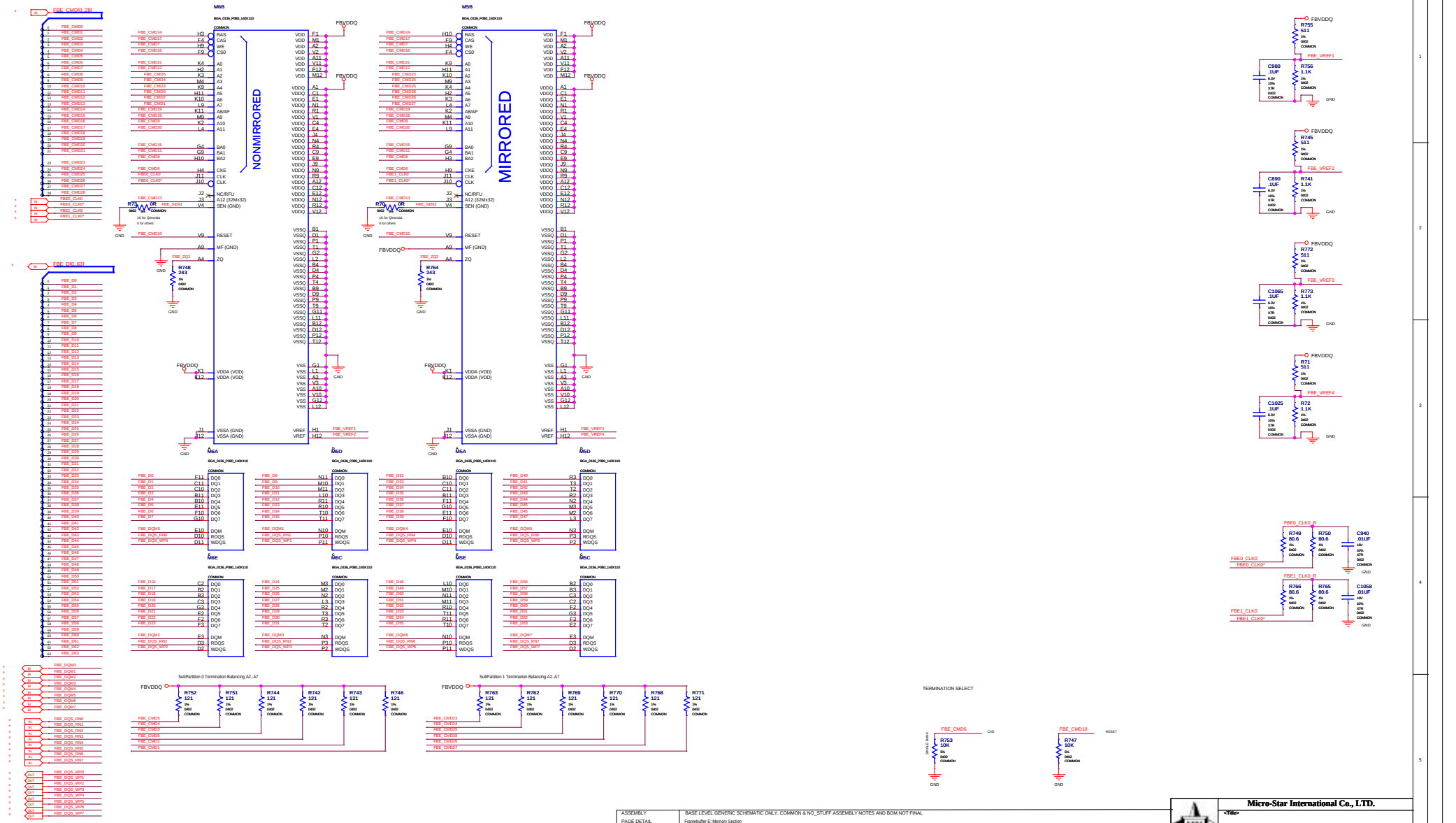
Framebuffer E: Memory Section



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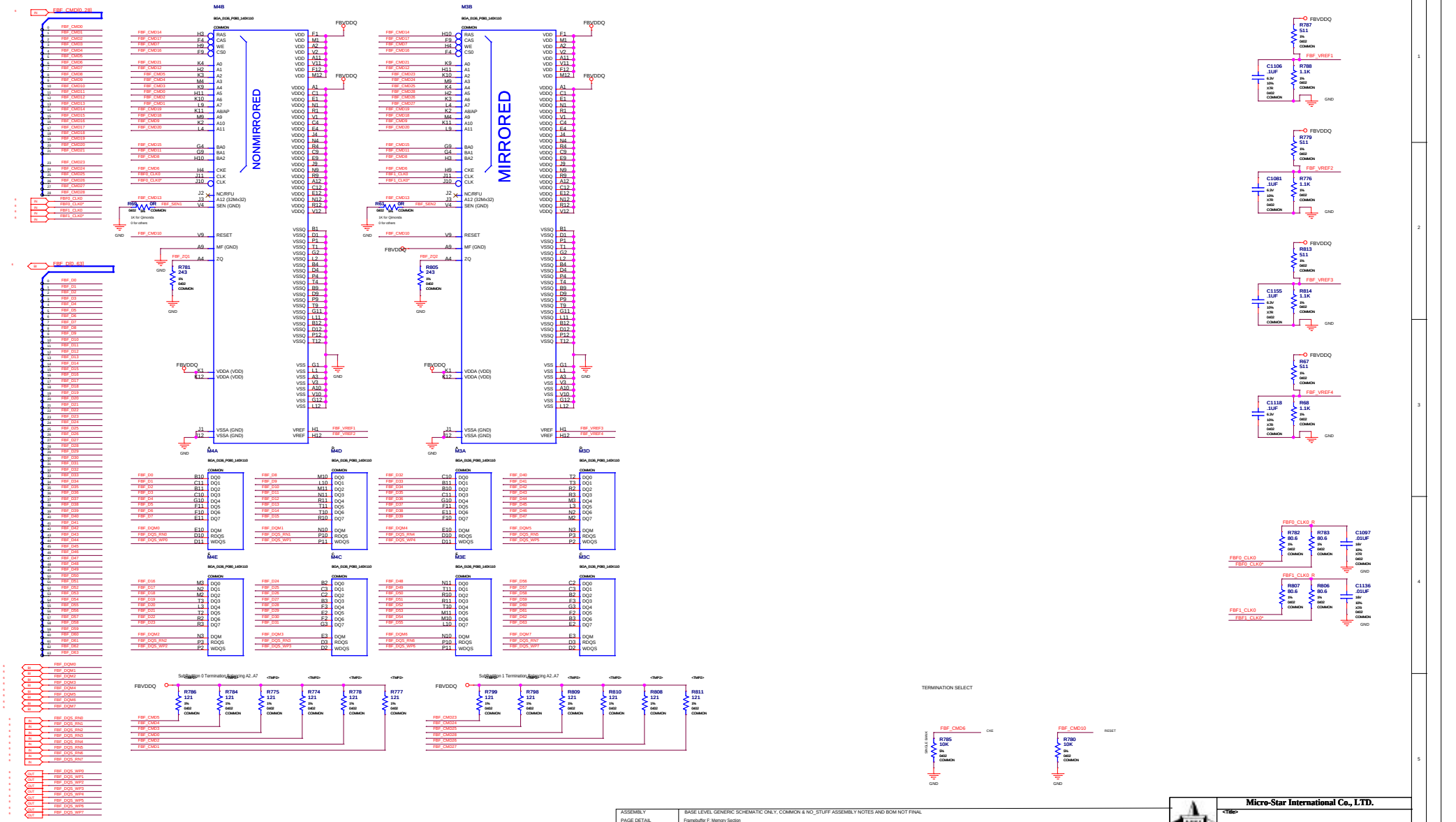
Framebuffer F: Memory Section



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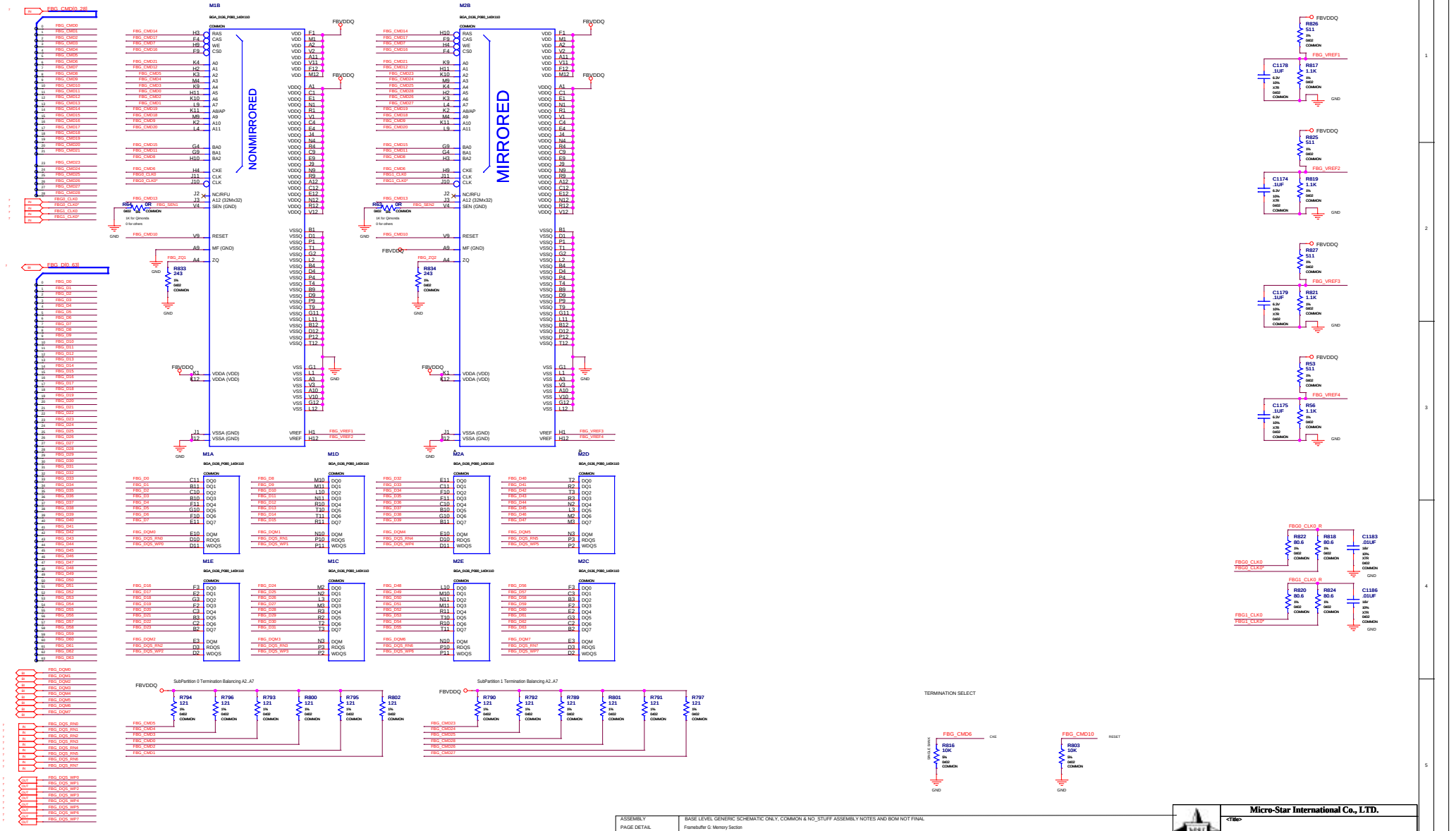
Framebuffer G: Memory Section



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Framebuffer H: N/A

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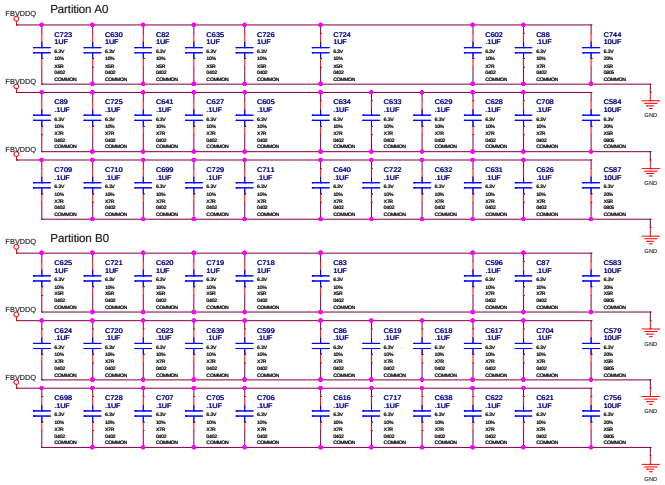
Decoupling: Memory Section A-D

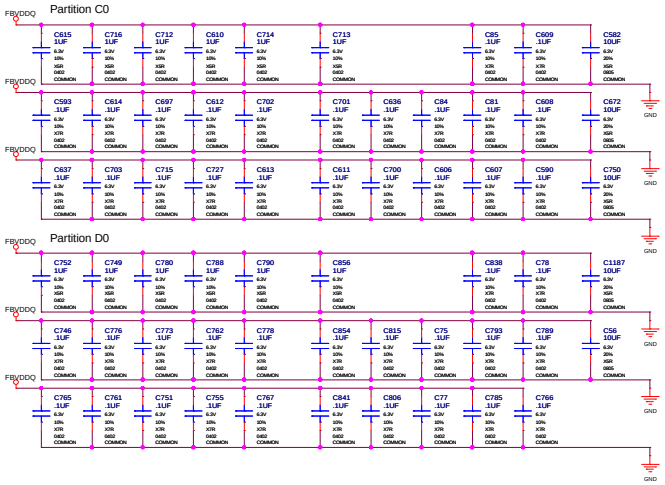
Banks A-D FBVDD/Q

Combined Distributed Capacitance

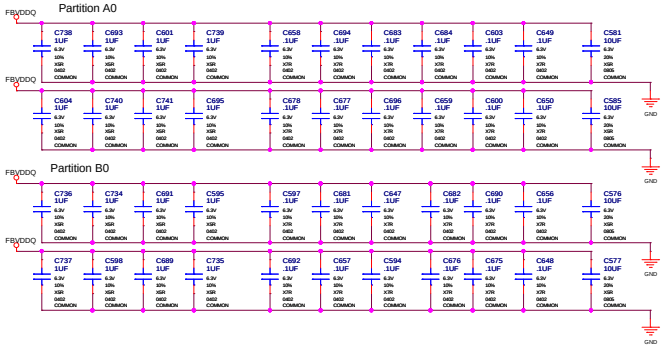
280 uF

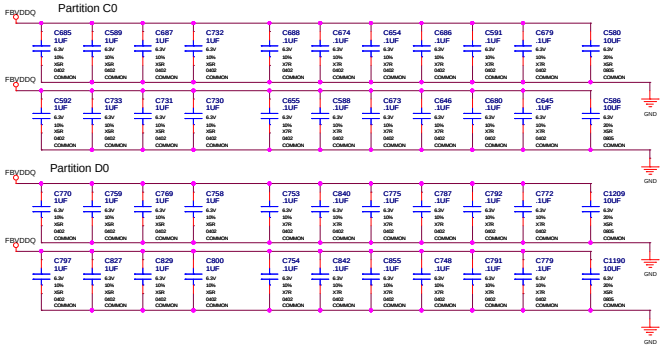
Decoupling for FBVDDQ





Decoupling for FBVDDQ





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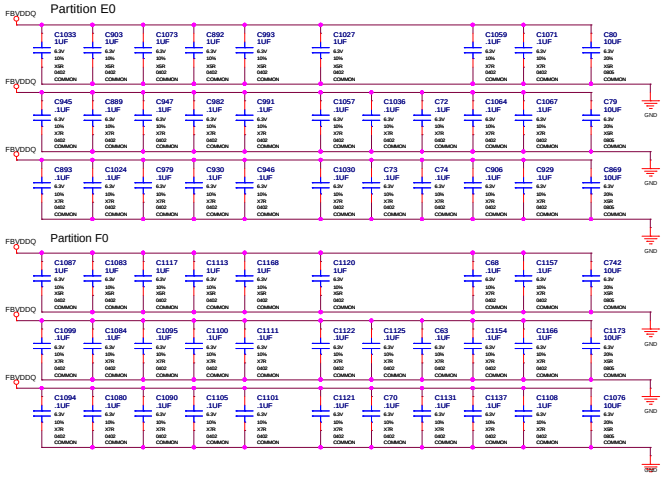
Decoupling: Memory Section E-G

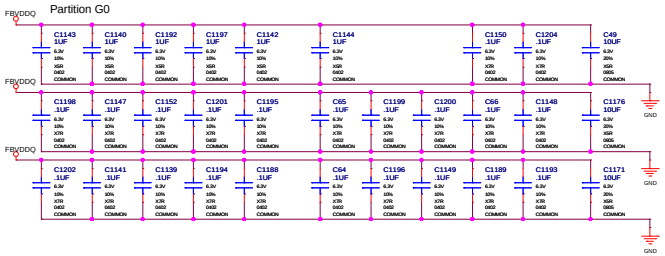
Banks E-G FBVDD/Q

Combined Distributed Capacitance

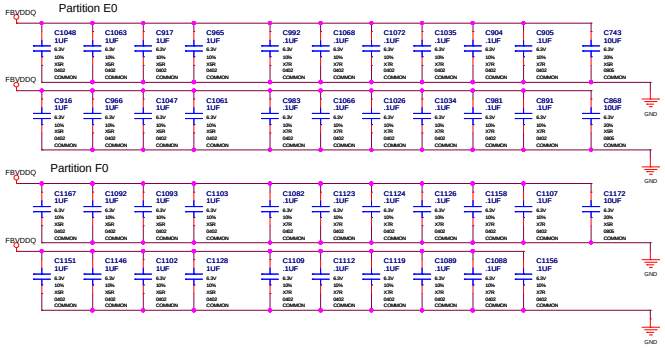
210 uF

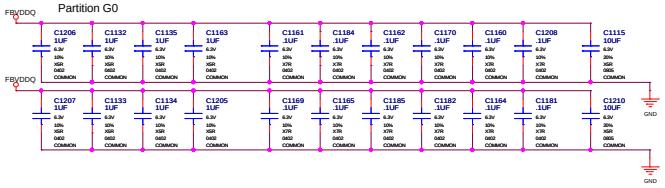
Decoupling for FBVDDQ





Decoupling for FBVDDQ





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PAGE DETAIL	Decoupling: Memory Section E-G

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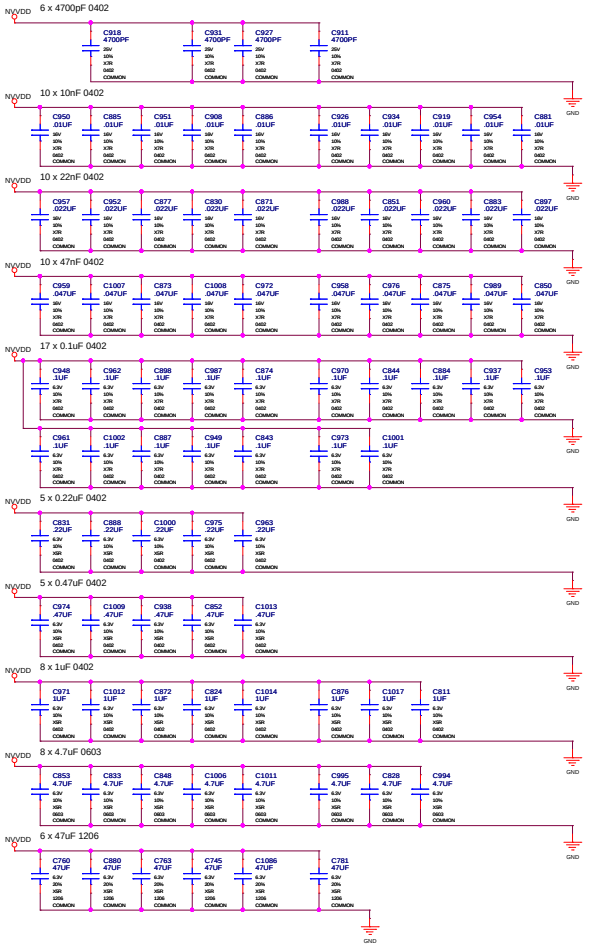
Decoupling: GPU (NVVDD, FBVDDQ)

Decoupling for NVVDD (under GPU)

GPU - NVVDD

Combined Distributed Capacitance

494 uF

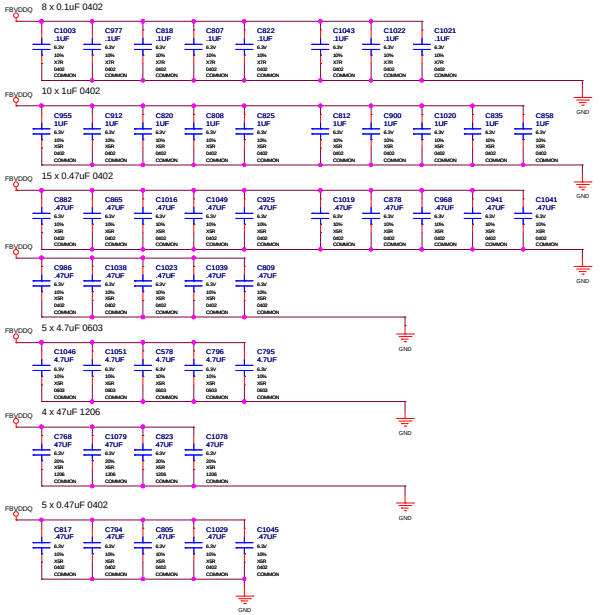


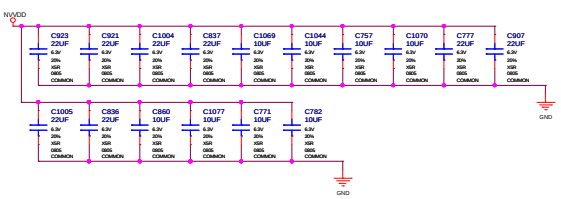
Decoupling for FBVDDQ (under GPU)

GPU - FBVDD/Q

Combined Distributed Capacitance

230 uF





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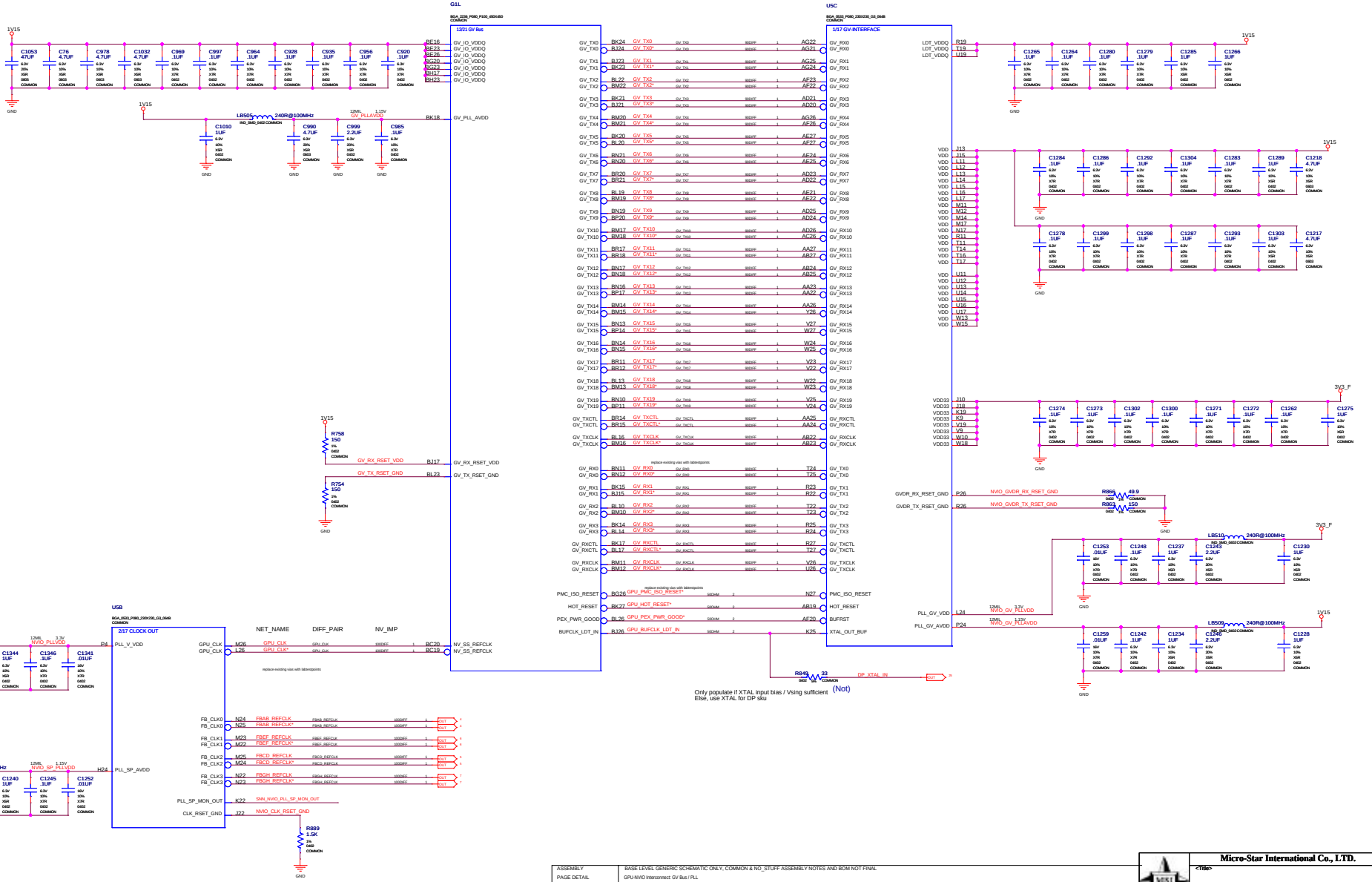
GPU-NVIO Interconnect: GV Bus / PLL



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PAGE DETAIL	GPU-NVIO Interconnect: GV Bus / PLL

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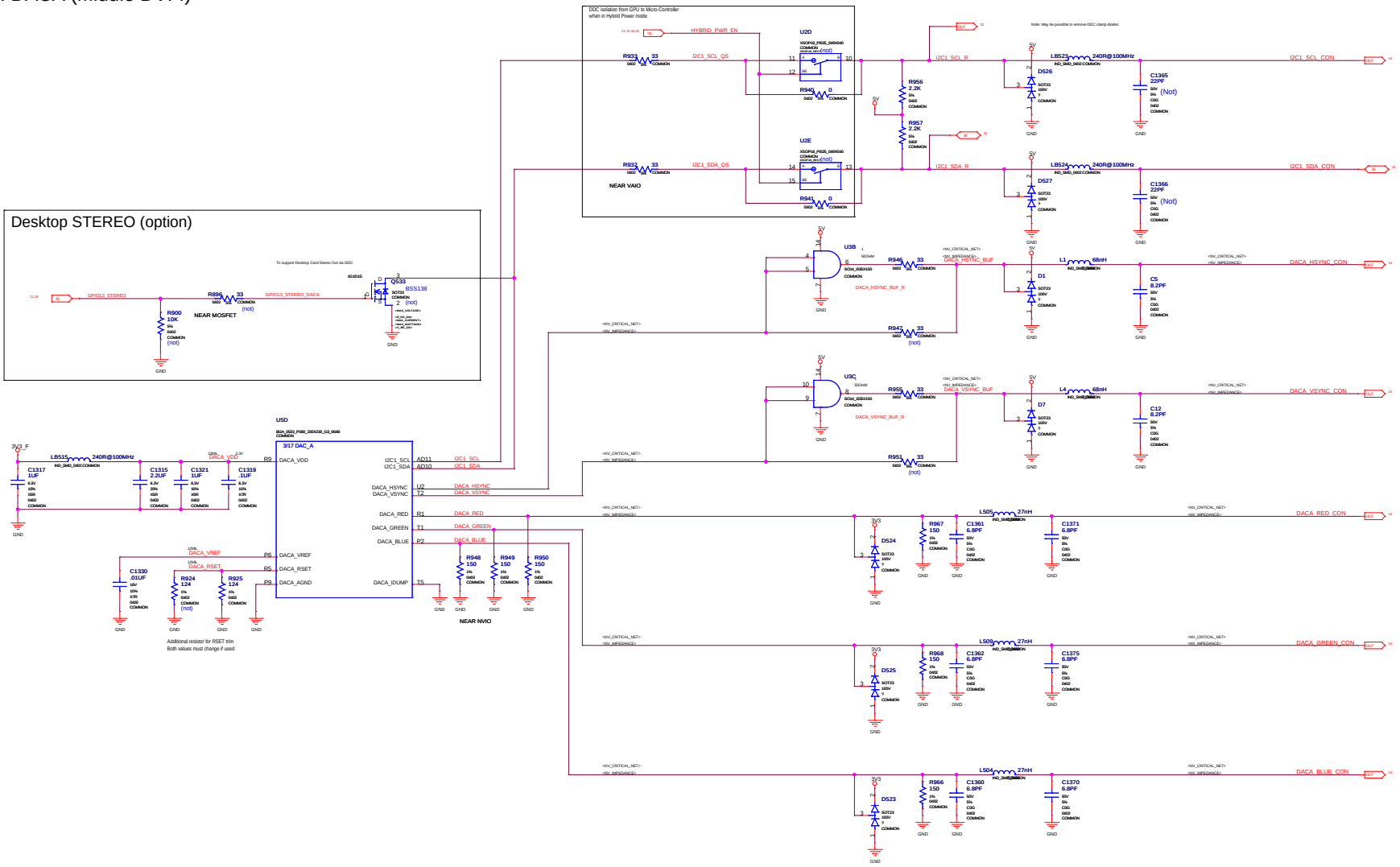

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PAGE DETAIL	Display: DACA (Middle DVI-I)

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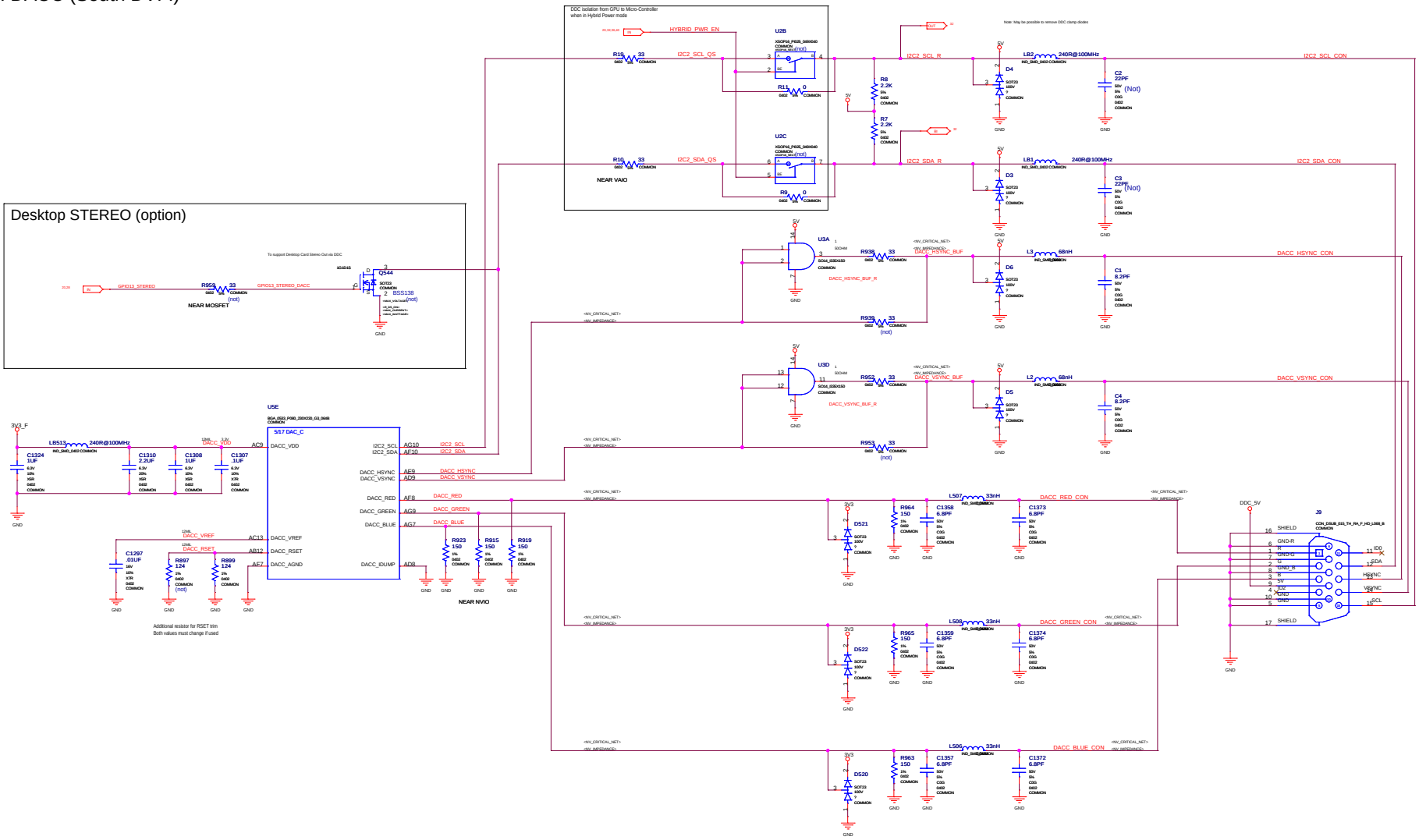
Display: DACC (South DVI-I)



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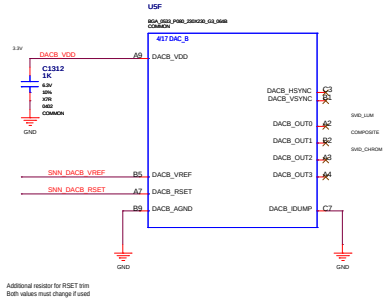
Display: DACB (North MiniDIN) SD/HDTV out

11/21 remove TV



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PAGE DETAIL	Display: DACB (North MiniDIN) SD/HDTV out

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Display: IFPAB for South DVI-I (with DACC)

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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Micro-Star International Co., LTD.

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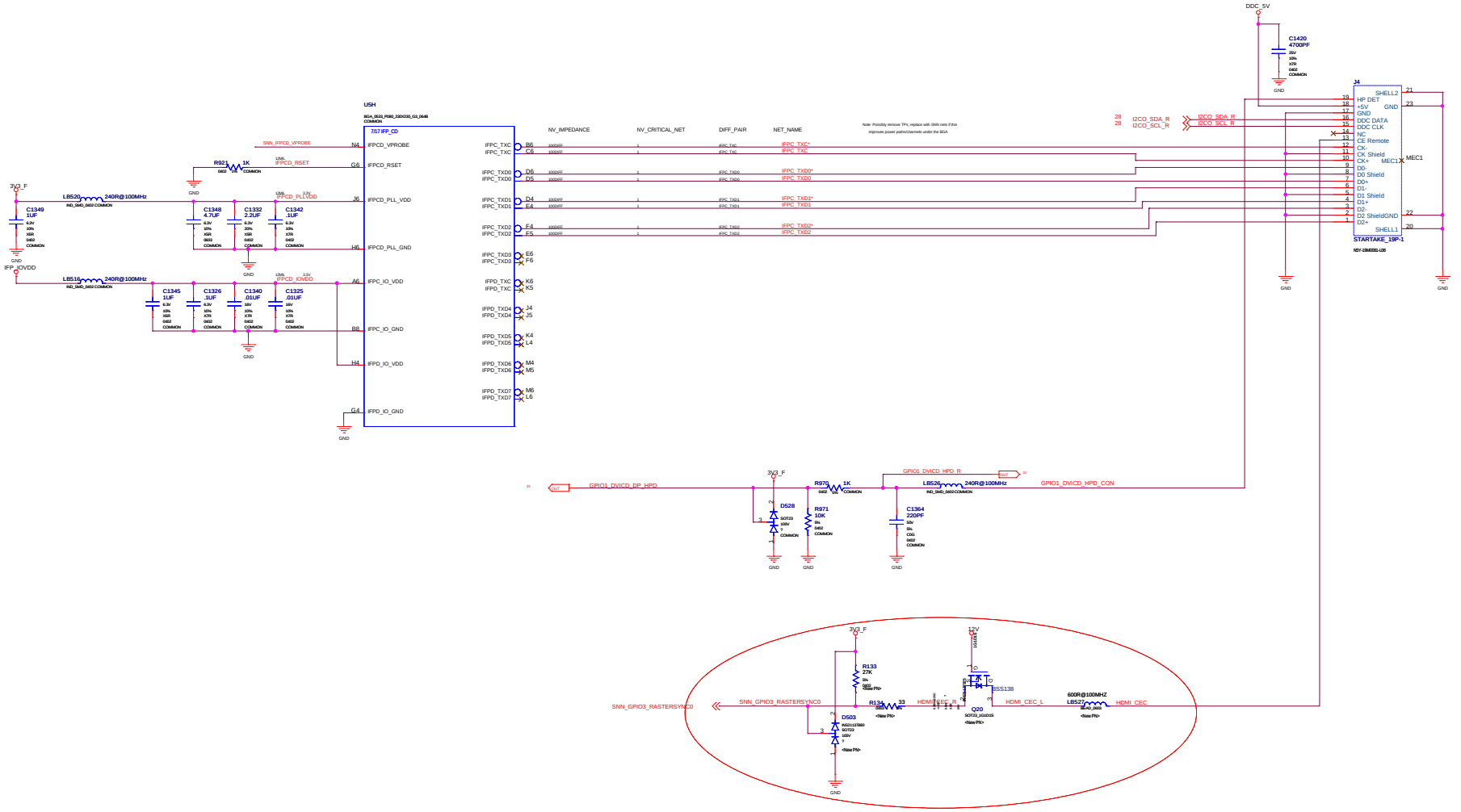
Display: IFPCD for middle DVI-I (with DACA)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: IFPCD for middle DVI-I (with DACA)

Micro-Star International Co., LTD.

<Title>

Size	Document Number	Rev
Custom	<Doc>	<RevCode>

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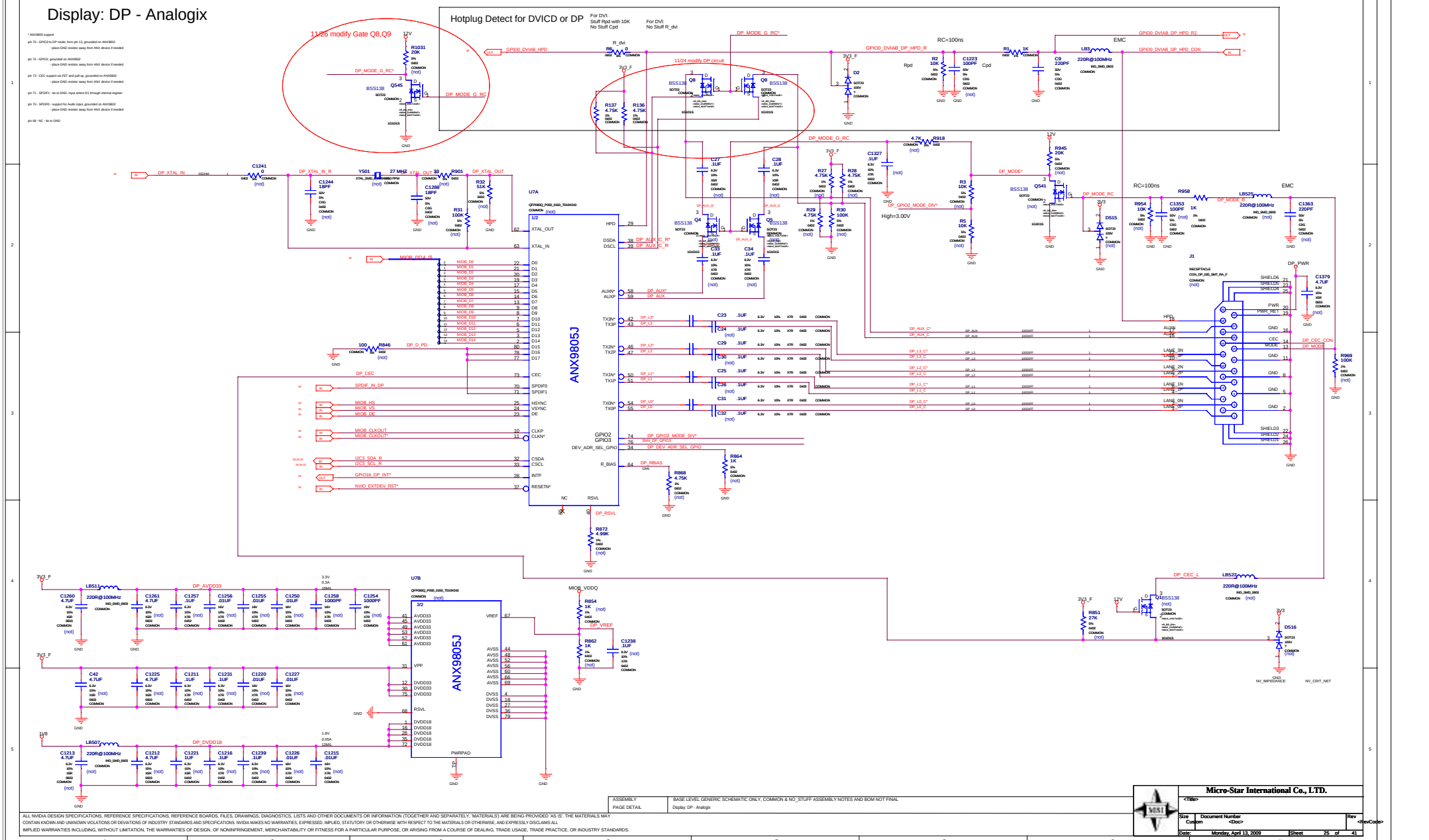
Display: DP - Analogix



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: DP - Analogix

Micro-Star International Co., LTD.

<Title>

Size	Document Number	Rev
Custom	<Doc>	<RevCode>

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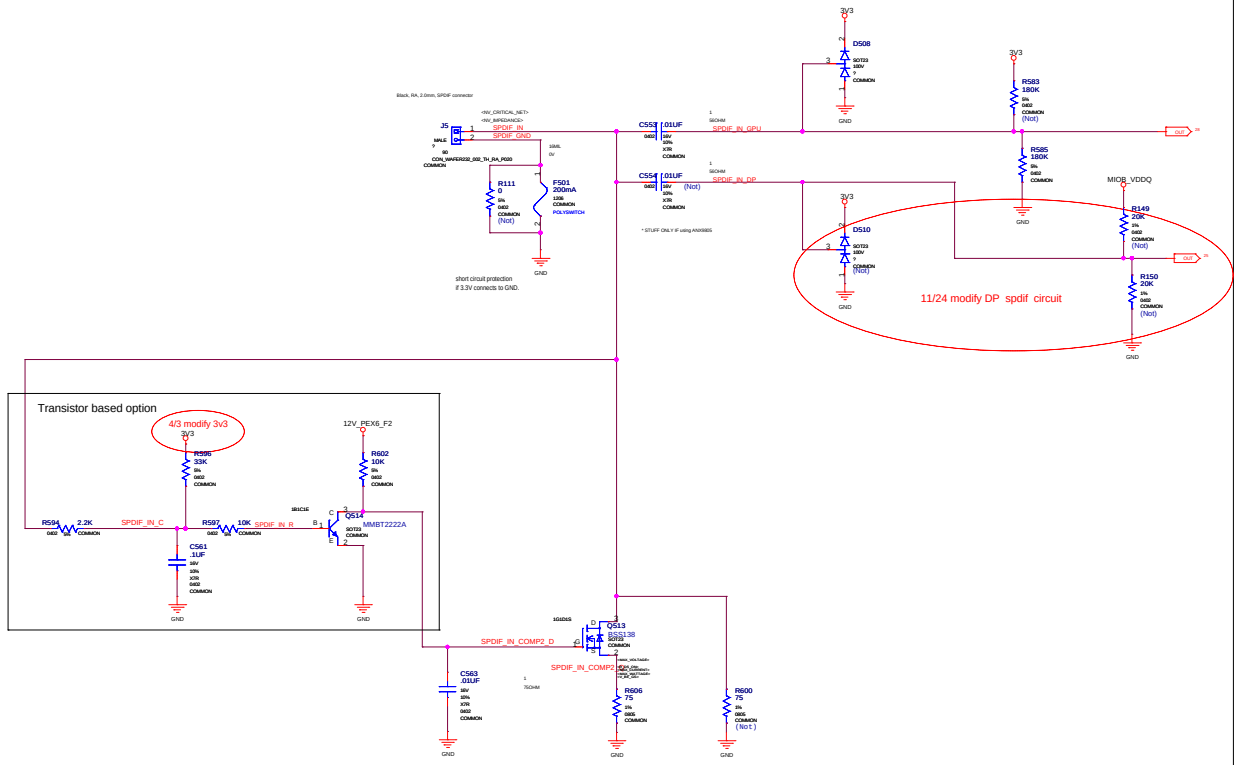
Connectors: SPDIF

SPDIF INPUT / Level Detection



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Connectors: SPDIF

Micro-Star International Co., LTD.			
<Title>			
Size: Custom	Document Number: <Doc>	Rev: <RevCode>	
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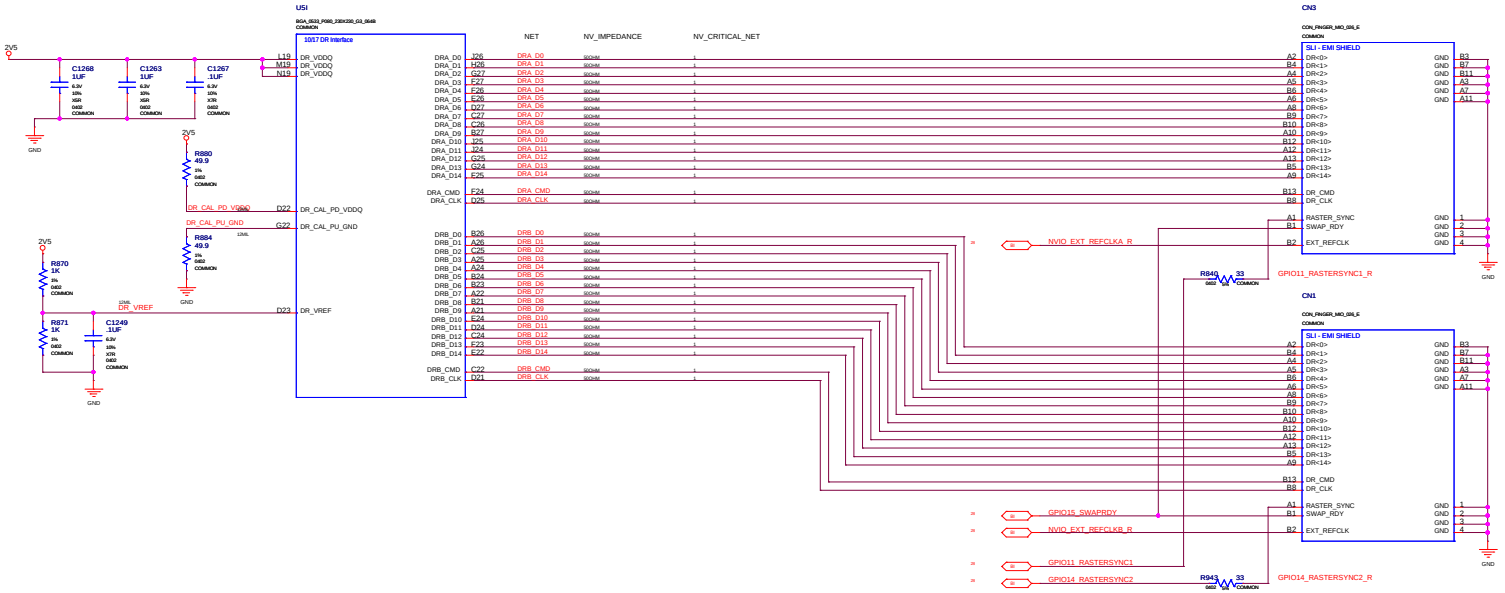
Connectors: DR Interface (Dual SLI)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Connectors: DR Interface (Dual SLI)

Micro-Star International Co., LTD.

<Title>

Size	Document Number	Rev
Custom	<Doc>	<RevCode>

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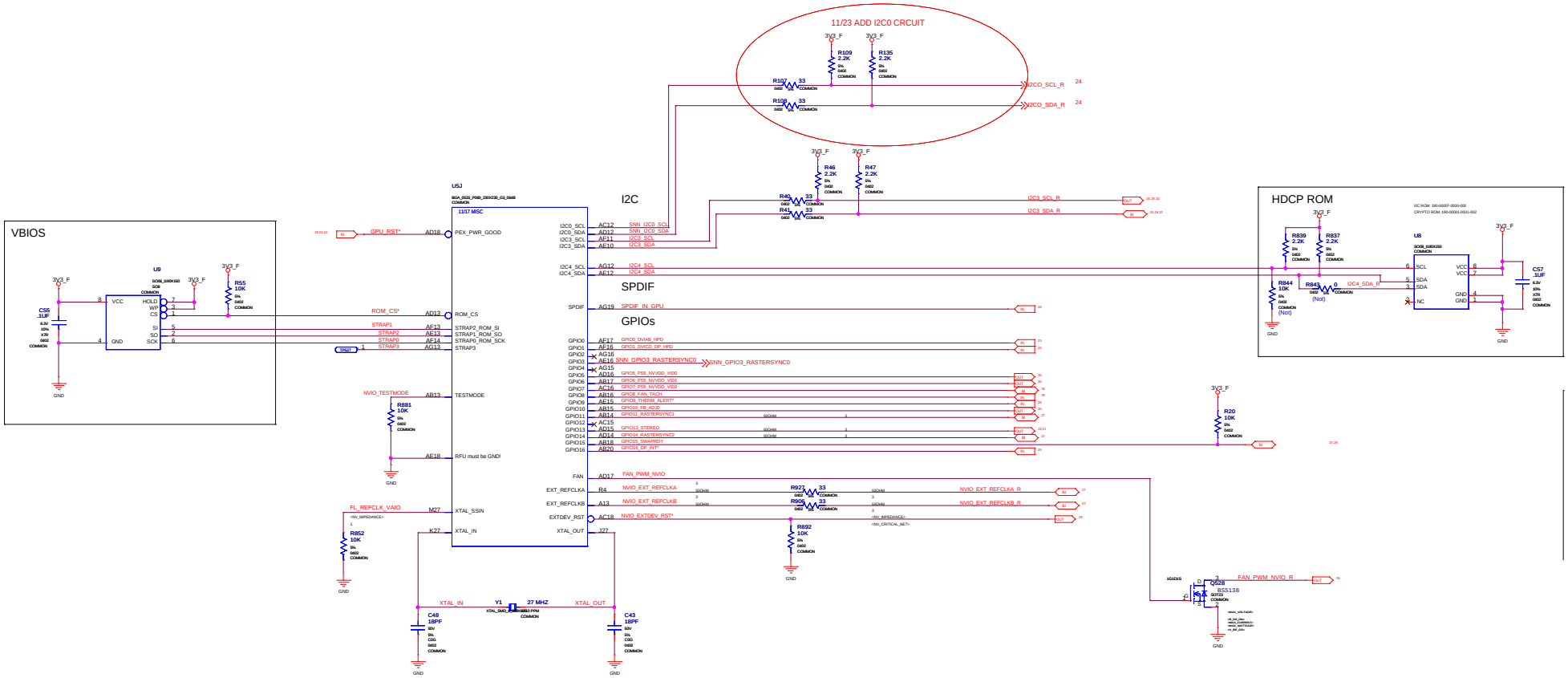
MISC: GPIO / XTAL / VBIOS / HDCP / I2C



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO / XTAL / VBIOS / HDCP / I2C

Micro-Star International Co., LTD.

<Title>

Size	Document Number	Rev
Custom	<Doc>	<RevCode>

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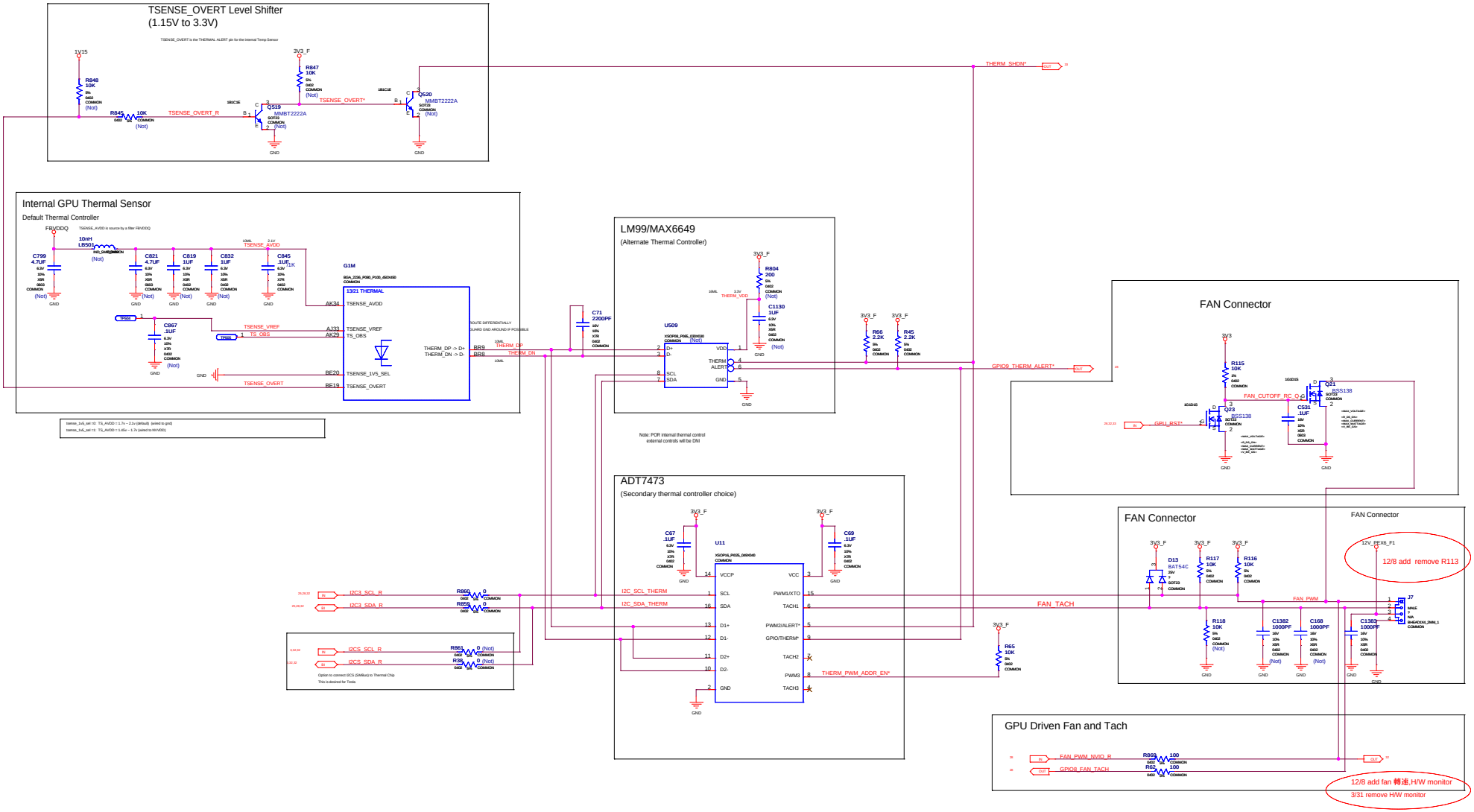
MISC: FAN / THERM



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: FAN / THERM

Micro-Star International Co., LTD.		
<Title>		
Size: Custom	Document Number: <Doc>	Rev: <RevCode>
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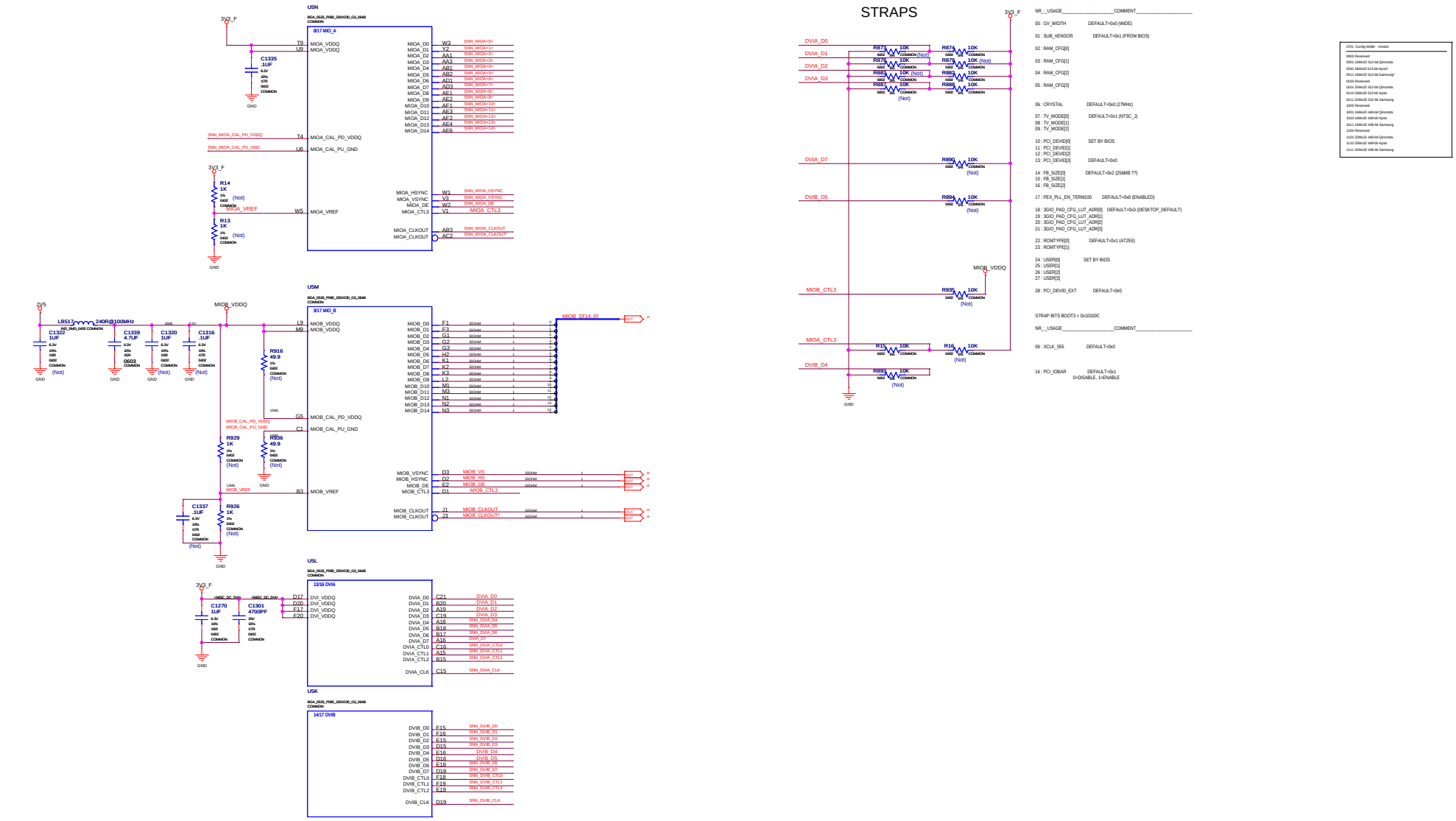
MISC: MIO / DVI / STRAPS



STRAP BITS BOOT0 = 0x101000

NR_:_USAGE_____COMMENT_____

00 : GV_WIDTH DEFAULT=0x0 (WIDE)

01 : SUB_VENDOR DEFAULT=0x1 (FROM BIOS)

02 : RAM_CFG[0]

03 : RAM_CFG[1]

04 : RAM_CFG[2]

05 : RAM_CFG[3]

06 : CRYSTAL DEFAULT=0x0 (27MHz)

07 : TV_MODE[0] DEFAULT=0x1 (NTSC_J)
08 : TV_MODE[1]
09 : TV_MODE[2]

10 : PCI_DEVID[0] SET BY BIOS
11 : PCI_DEVID[1]
12 : PCI_DEVID[2]
13 : PCI_DEVID[3] DEFAULT=0x0

14 : FB_SIZE[0] DEFAULT=0x2 (256MB ??)
15 : FB_SIZE[1]
16 : FB_SIZE[2]

17 :PEX_PLL_EN_TERM100 DEFAULT=0x0 (ENABLED)

18 : 3GIO_PAD_CFG_LUT_ADR[0] DEFAULT=0x3 (DESKTOP_DEFAULT)
19 : 3GIO_PAD_CFG_LUT_ADR[1]
20 : 3GIO_PAD_CFG_LUT_ADR[2]
21 : 3GIO_PAD_CFG_LUT_ADR[3]

22 : ROMTYPE[0] DEFAULT=0x1 (AT25S)
23 : ROMTYPE[1]

24 : USER[0] SET BY BIOS
25 : USER[1]
26 : USER[2]
27 : USER[3]

28 : PCI_DEVID_EXT DEFAULT=0x0

STRAP BITS BOOT3 = 0x10100C

NR_:_USAGE_____COMMENT_____

06 : XCLK_SS5 DEFAULT=0x0

16 : PCI_IOBAR DEFAULT=0x1
0=DISABLE, 1=ENABLE

CFG: Config Width Vendor

0000 Reserved
0001 16Mx32 S12-bit Qimonda
0010 16Mx32 S12-bit Hynix*
0011 16Mx32 S12-bit Samsung*
0100 Reserved
0101 32Mx32 S12-bit Qimonda
0110 32Mx32 S12-bit Hynix
0111 32Mx32 S12-bit Samsung
1000 Reserved
1001 16Mx32 s63-bit Qimonda
1010 16Mx32 s68-bit Hynix
1011 16Mx32 s68-bit Samsung
1100 Reserved
1101 32Mx32 s68-bit Qimonda
1110 32Mx32 s68-bit Hynix
1111 32Mx32 s68-bit Samsung

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: MIO / DVI / STRAPS

Micro-Star International Co., LTD.

<Title>

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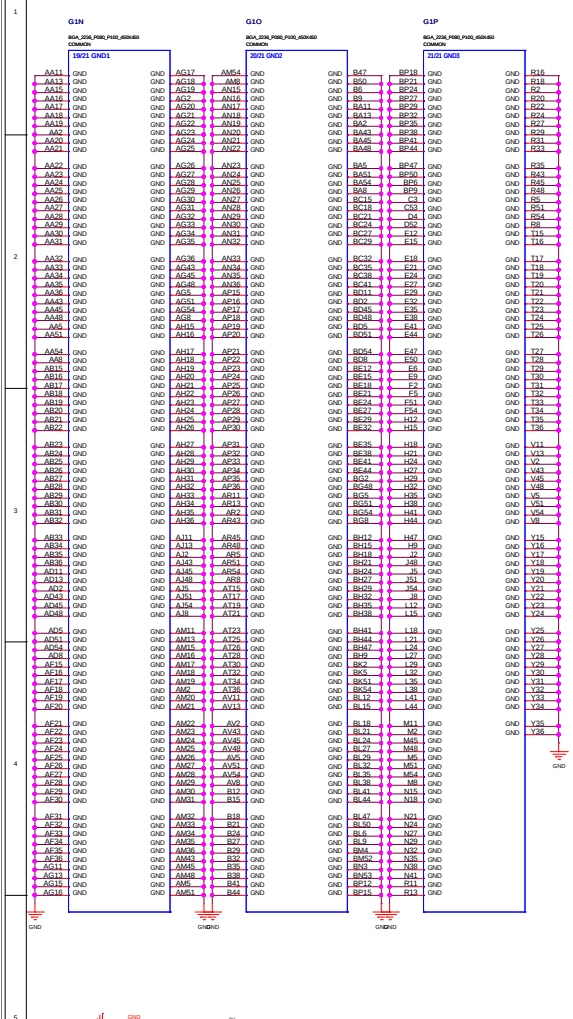
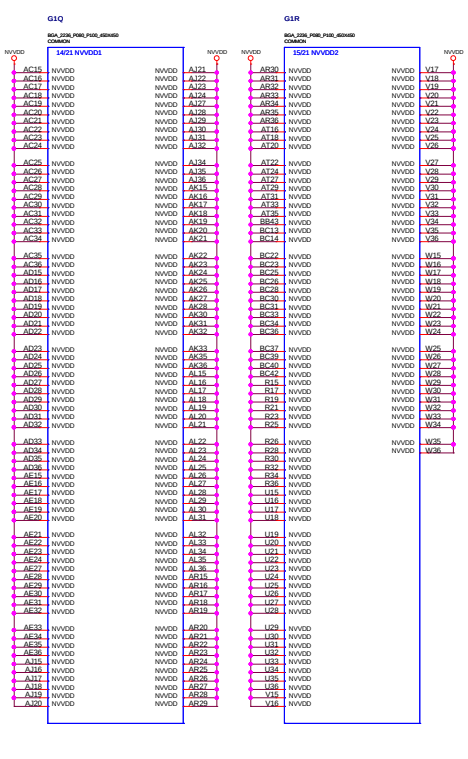
Power and GND (GPU and NVIOx)

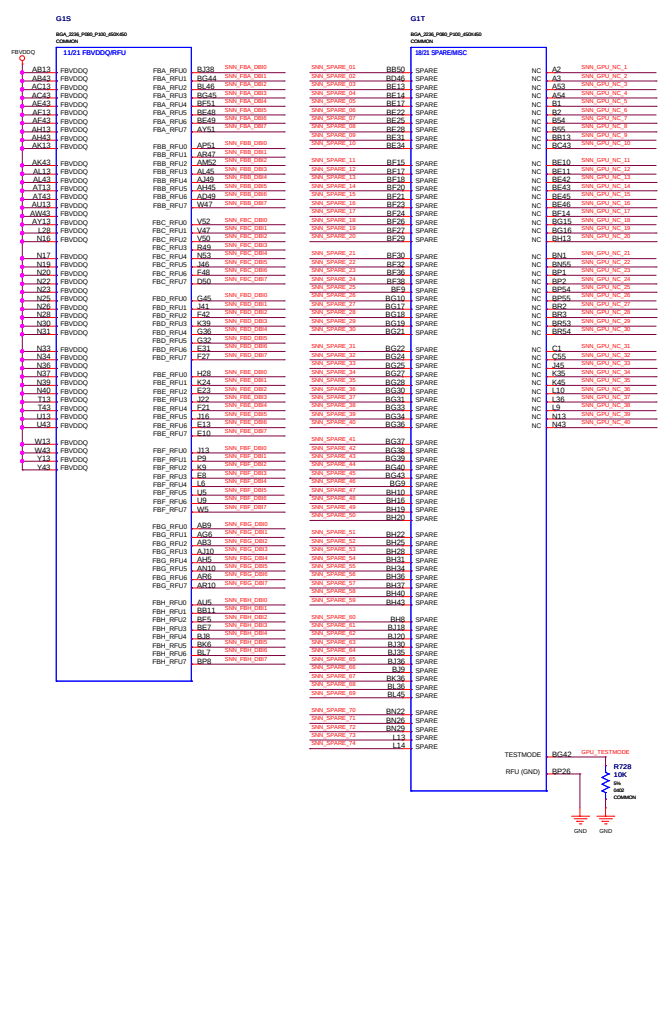
GPU SECTION GND



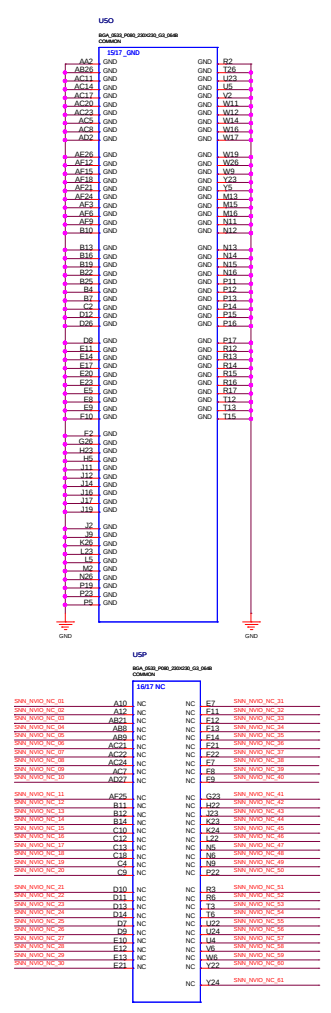
GPU SECTION POWER



GPU SECTION MISC



NVIOx SECTION GND



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power and GND (GPU and NVIOx)

Micro-Star International Co., LTD.

<Title>

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Custom	<Doc>	<RevCode>
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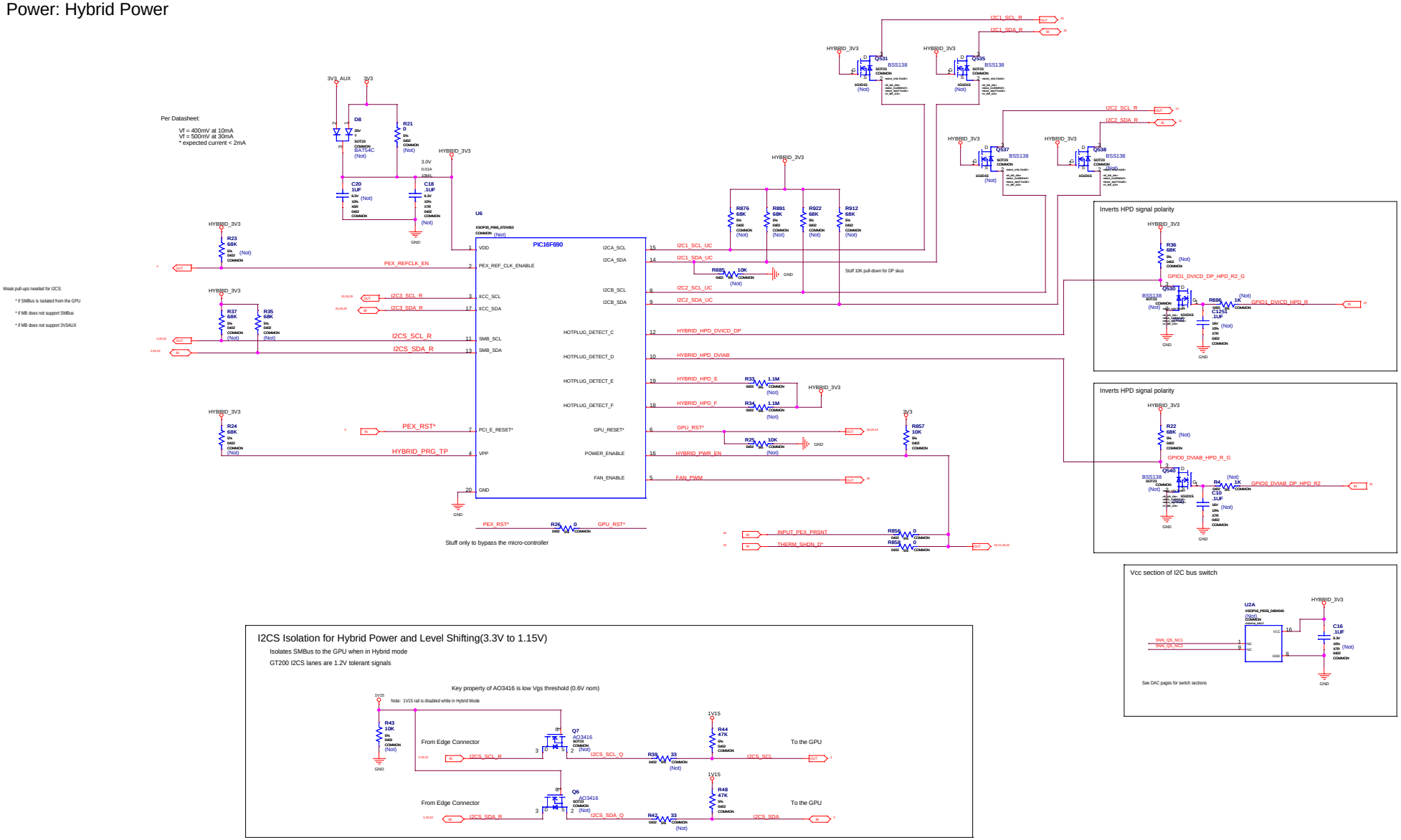
Power: Hybrid Power



I2CS Isolation for Hybrid Power and Level Shifting(3.3V to 1.15V)

Isolates SMBus to the GPU when in Hybrid mode

GT200 I2CS lanes are 1.2V tolerant signals

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power: Hybrid Power

Micro-Star International Co., LTD.			
<Title>			
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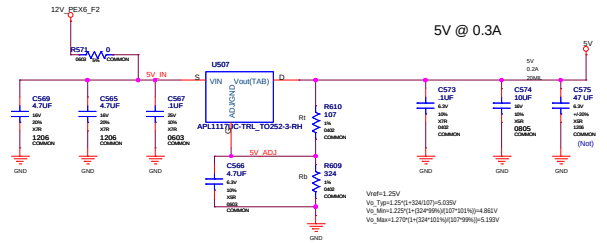
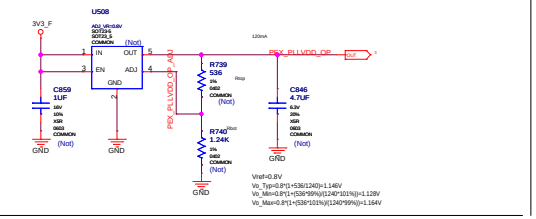
Power Supply: 5V LDO / 3V3_DP / THERM SHUTDOWN LATCH / IFP_IOVDD /PEX_PLVDD

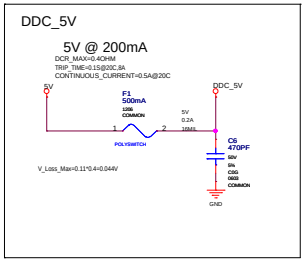
5V Linear



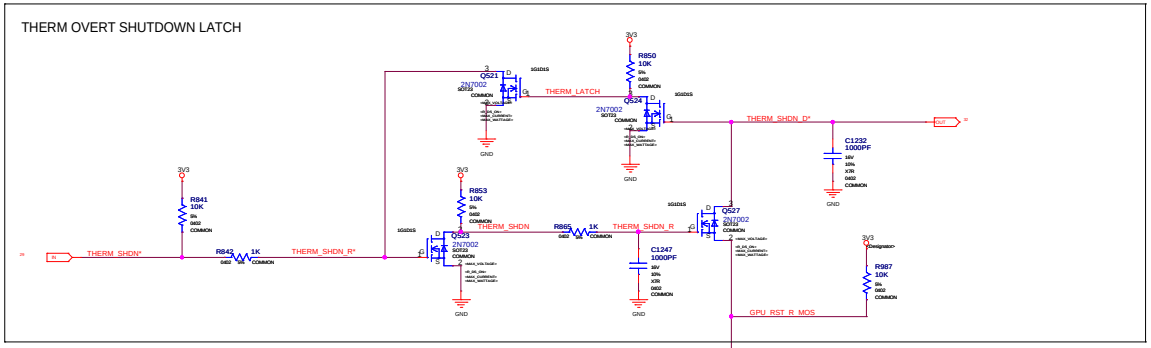
PEX PLLVDD optional Supply



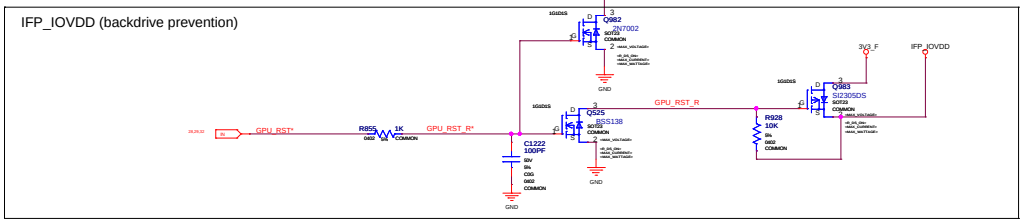
DDC_5V



THERM OVERT SHUTDOWN LATCH

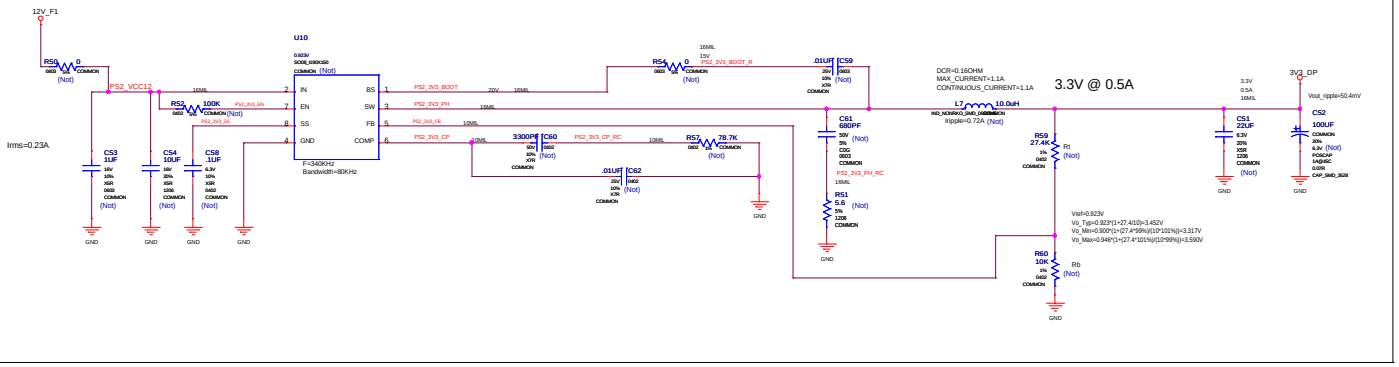


IFP_IOVDD (backdrive prevention)



3V3_DP SWITCHER

(Only required for DisplayPort SKU)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 5V + 5V Alt / SHDN LATCH / IFP_IOVDD

Micro-Star International Co., LTD.

<Title>

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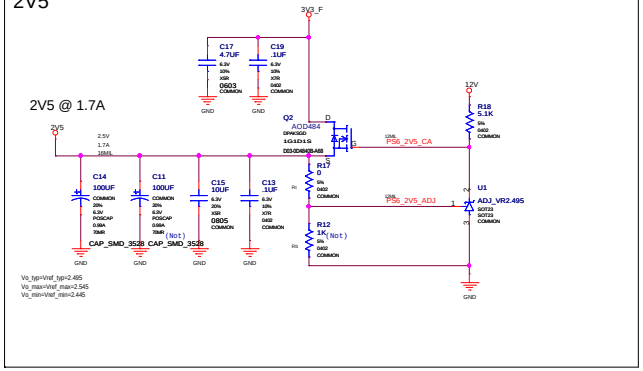
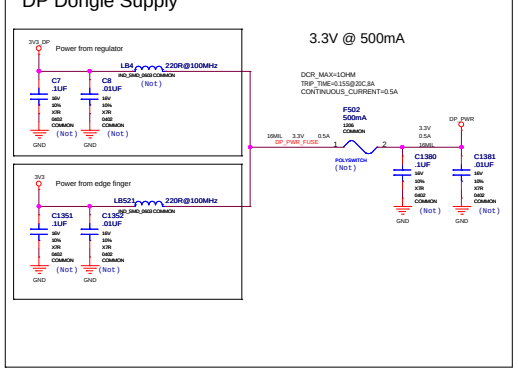
Power Supply: 2V5, DP_PWR, 8V5 1V15 (PEX_VDD, GV_VDD)

2V5



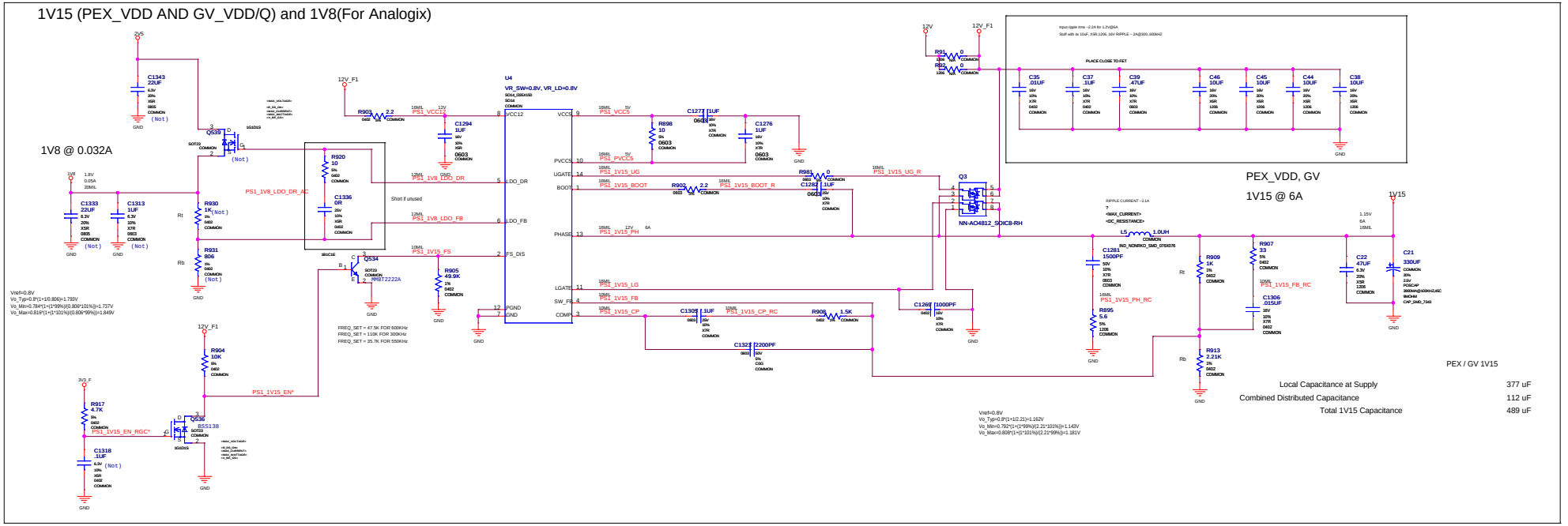
DP Dongle Supply



8V5

11/21:remove 8V5 circuit

1V15 (PEX_VDD AND GV_VDD/Q) and 1V8(For Analogix)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 2V5, DP_PWR, 1V15 (PEX_VDD, GV_VDD)

Micro-Star International Co., LTD.		
<Title>		
Size: Custom	Document Number: <Doc>	Rev: <RevCode>
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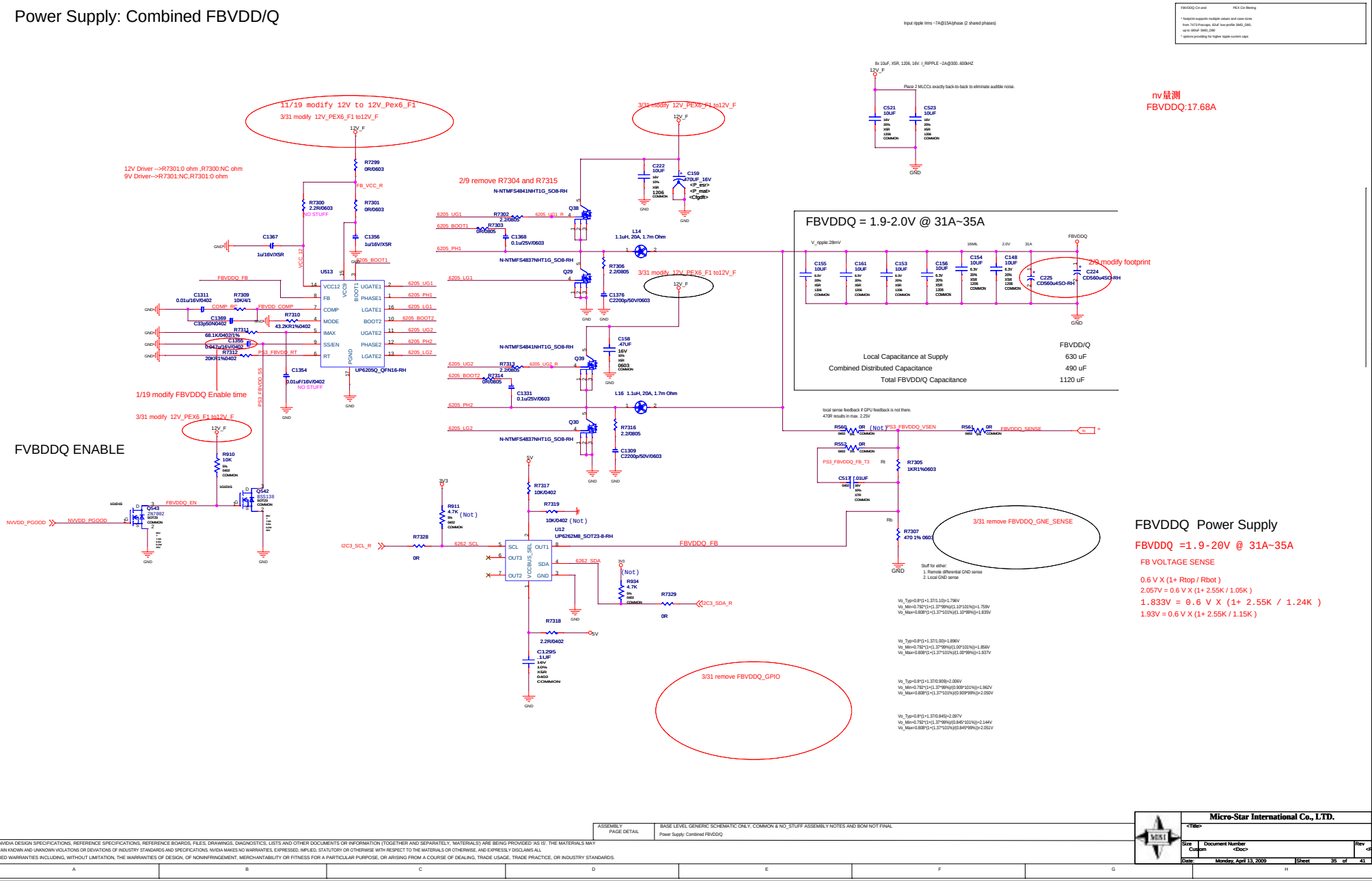
Power Supply: Combined FBVDD/Q



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: Combined FBVDD/Q

Micro-Star International Co., LTD.

<Title>

Size	Document Number	Rev
Custom	<Doc>	<RevCode>

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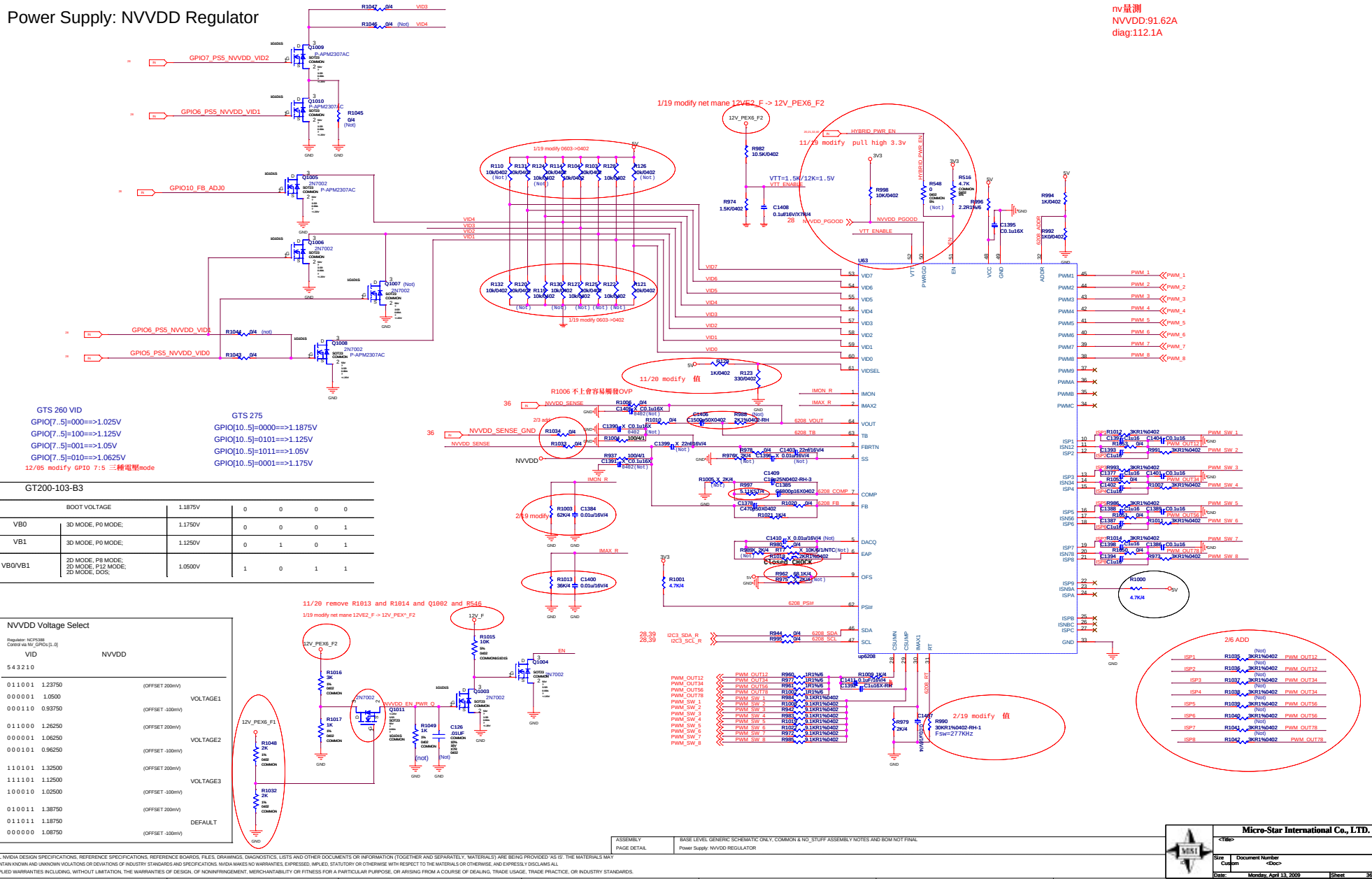
Power Supply: NVVDD Regulator



VID	NVVDD	
543210		
011001	1.23750	(OFFSET 200mV)
000001	1.0500	VOLTAGE1
000110	0.93750	(OFFSET -100mV)
011000	1.26250	(OFFSET 200mV)
000001	1.06250	VOLTAGE2
000101	0.96250	(OFFSET -100mV)
110101	1.32500	(OFFSET 200mV)
111101	1.12500	VOLTAGE3
100010	1.02500	(OFFSET -100mV)
010011	1.38750	(OFFSET 200mV)
011011	1.18750	DEFAULT
000000	1.08750	(OFFSET -100mV)

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD REGULATOR

Size: Custom	Document Number: <Doc>		Rev: <RevCode>
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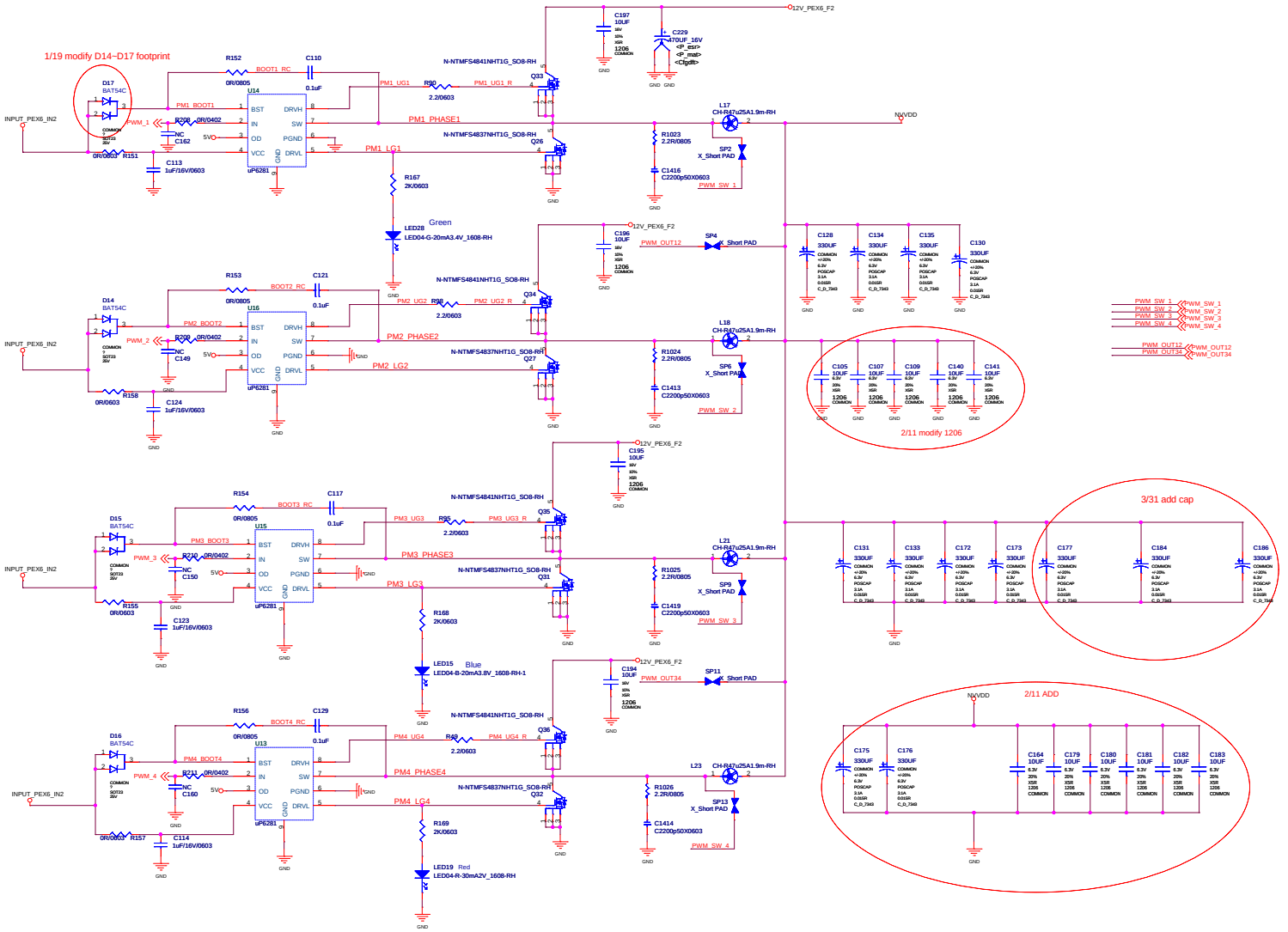
Power Supply: NVVDD Phase 1,2 powered from external PEX 6PIN



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 1-2 of 4

Size: Custom	Document Number: <Doc>	Rev: <RevCode>
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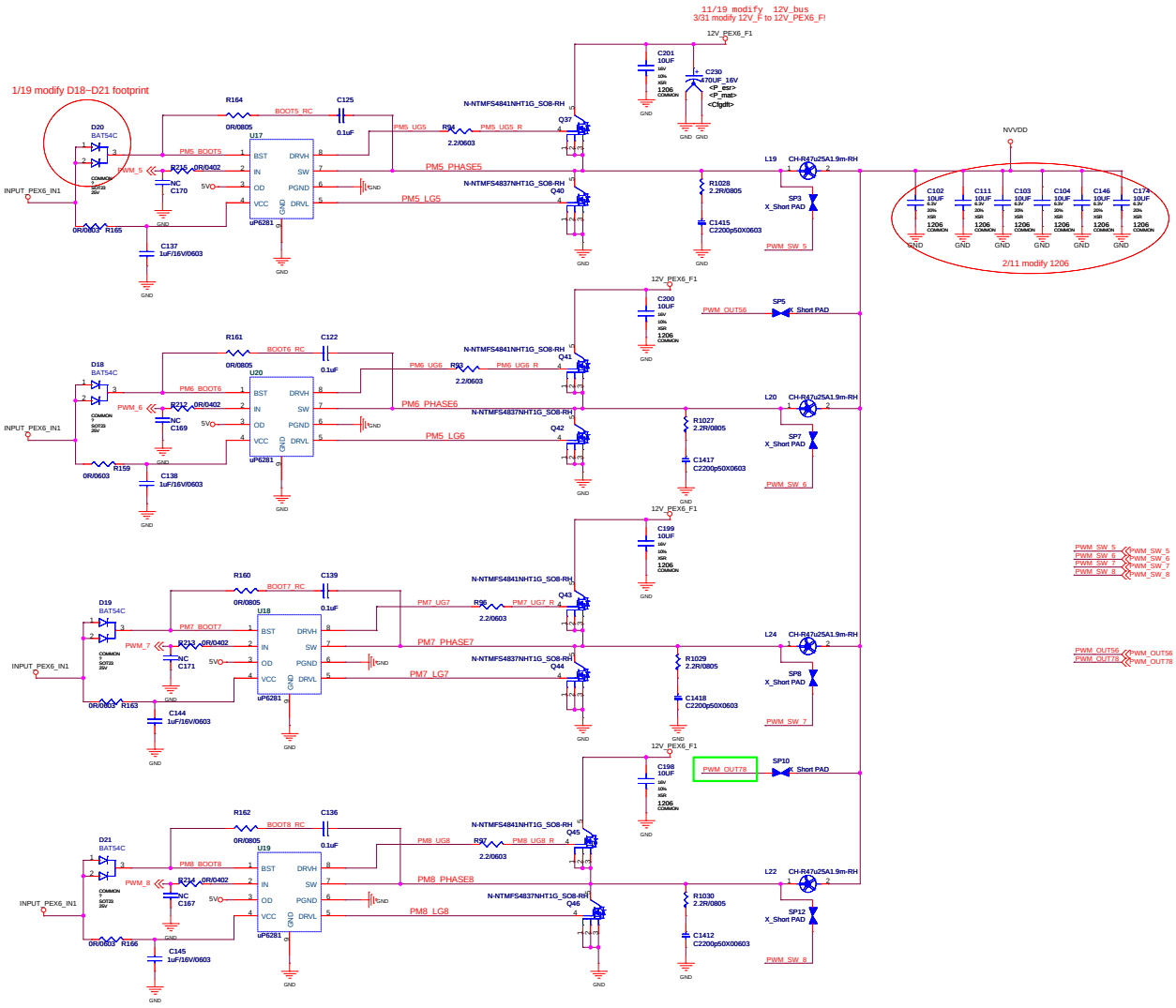
Power Supply: NVVDD Phase 5~8 powered from internal PEX edge connector



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 3-4 of 4

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<Title>			
Size: Custom	Document Number: <Doc>	Rev: <RevCode>	
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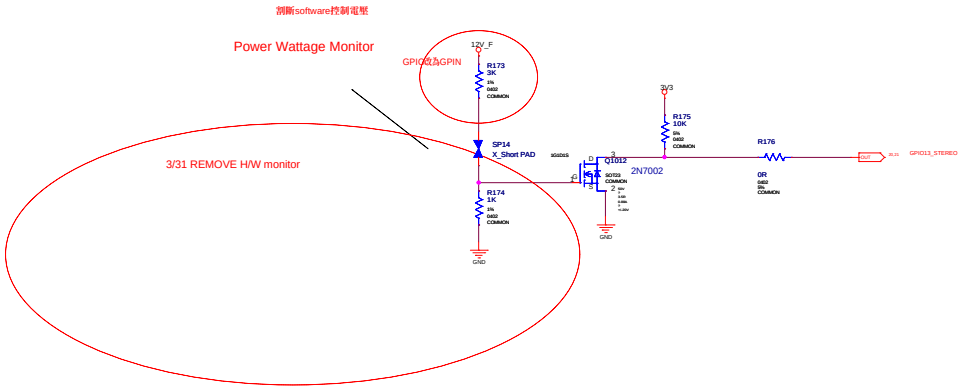
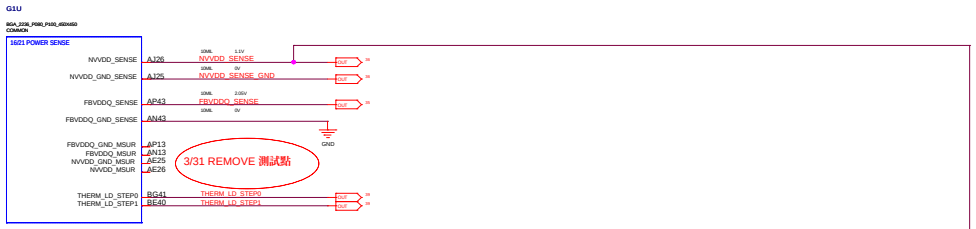
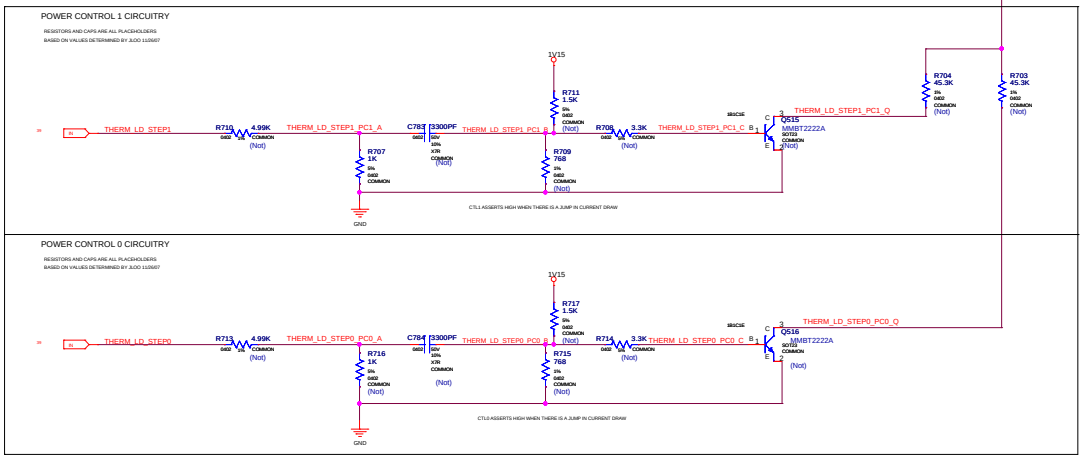
Power Supply: NVVDD power control



NVVDD & FBVDDQ SENSE/MSUR





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	NVVDD & FBVDDQ SENSE/MSUR

Micro-Star International Co., LTD.			
<Title>			
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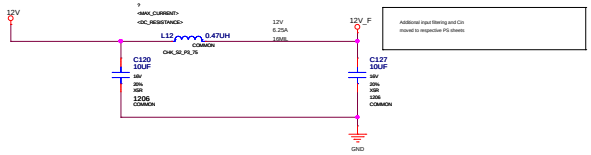
Power: Input Rail Filter and Detection Logic

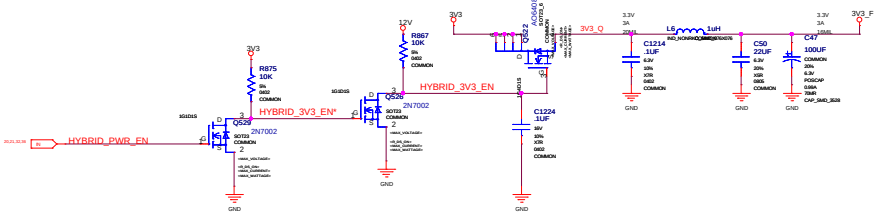
Connector Power State Table

2x3 Connector	2x3 Connector		Power	STATE
Connected	Connected		225W	Full Perf
Connected	Not Connected		150W	Board Off
Not Connected	Connected		150W	Board Off
Not Connected	Not Connected		75W	Board Off

PEX_12V INPUT - 66W

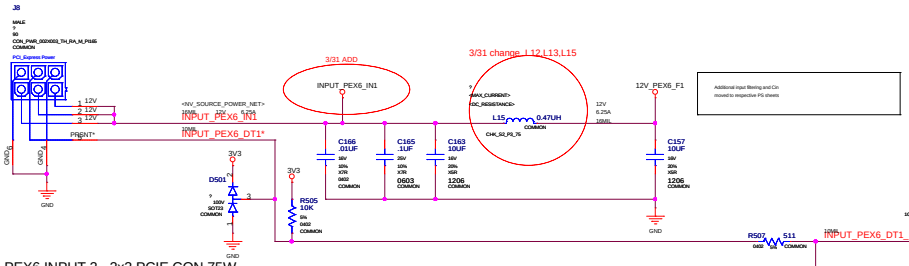


PEX 3V3 INPUT - 10W



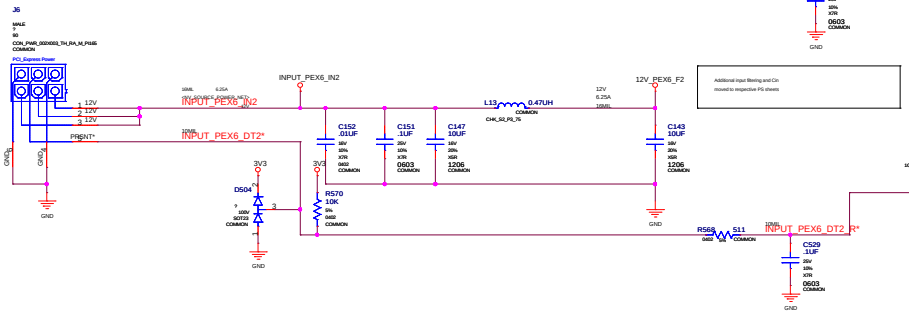
PEX6 INPUT 1 - 2x3 PCIE CON 75W

MUST BE ATTACHED AND POWERED TO START BOARD

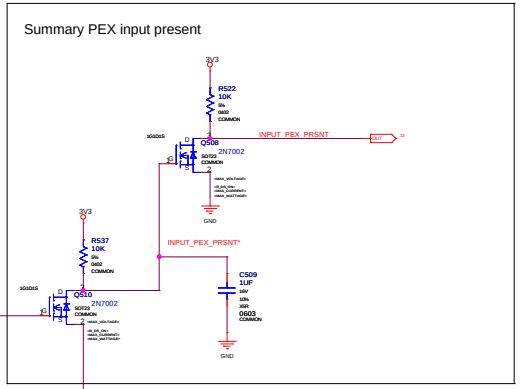


PEX6 INPUT 2 - 2x3 PCIE CON 75W

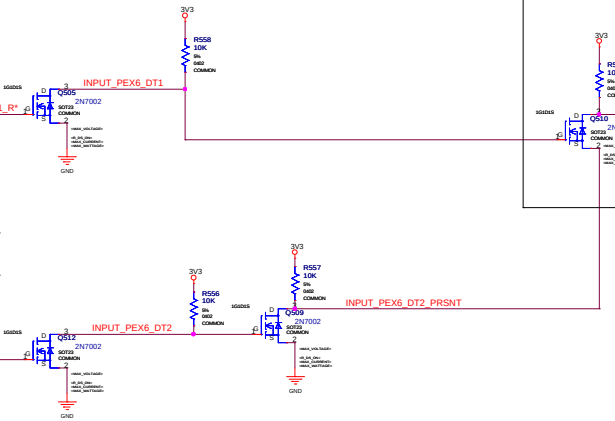
MUST BE ATTACHED AND POWERED TO START BOARD



Summary PEX input present



INPUT_PEX6_DT1 / INPUT_PEX6_DT2



ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: Power: Input Rail Filter and Detection Logic

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<Title>

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Thermal/Mechanical/ID

Bracket and Assembly

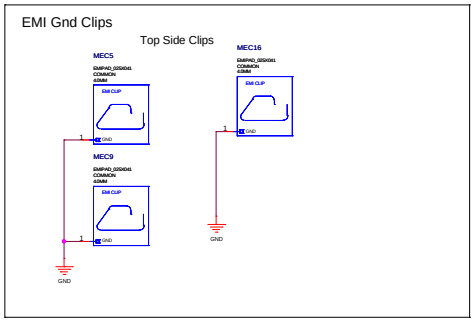
GPU Socket

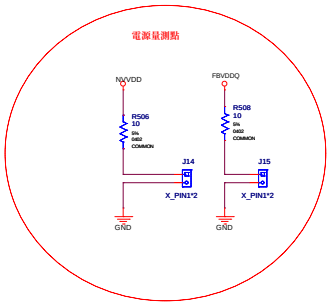
GPU Stiffener

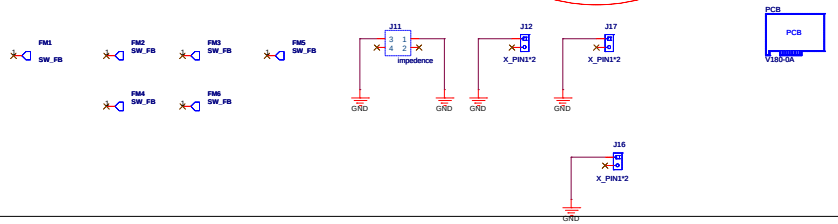
NVIOx Socket

Hockey Stick Retention Mechanism

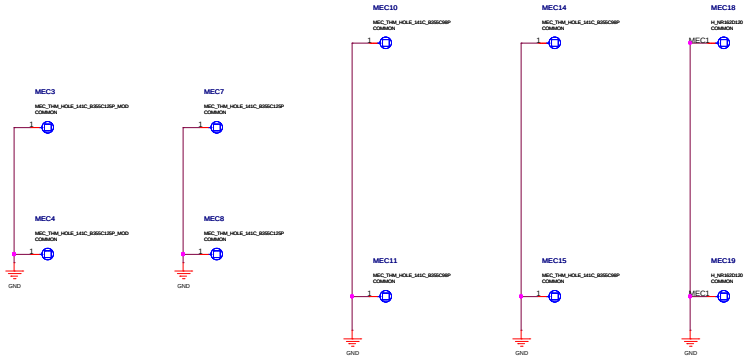
EMI Gnd Clips







THERMAL/MECHANICAL HOLES



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal/Mechanical

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