P691: G98/GT218, DDR2 MEMORY 64MX16/32MX16

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10691-BASE-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10691-0001-100	GT218-300, 550/1375/500, 256MB/64bit, 32Mx16 DDR2, DVI-DL+DP+VGA, DT
2	SKU0002	600-10691-0002-100	GT218-300, 550/1375/500, 512MB/64bit, 64Mx16 DDR2, DVI-DL+DP+VGA, DT
3	SKU0010	600-10691-0010-100	G98-400, 550/1375/500, 256MB/64bit, 32Mx16 DDR2, DVI-DL+DP+VGA, DT
4	SKU0011	600-10691-0011-100	G98-400, 550/1375/500, 512MB/64bit, 64Mx16 DDR2, DVI-DL+DP+VGA, DT
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P691 Overview

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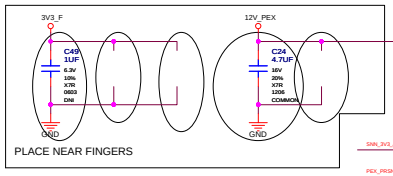
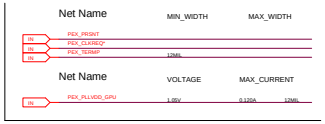
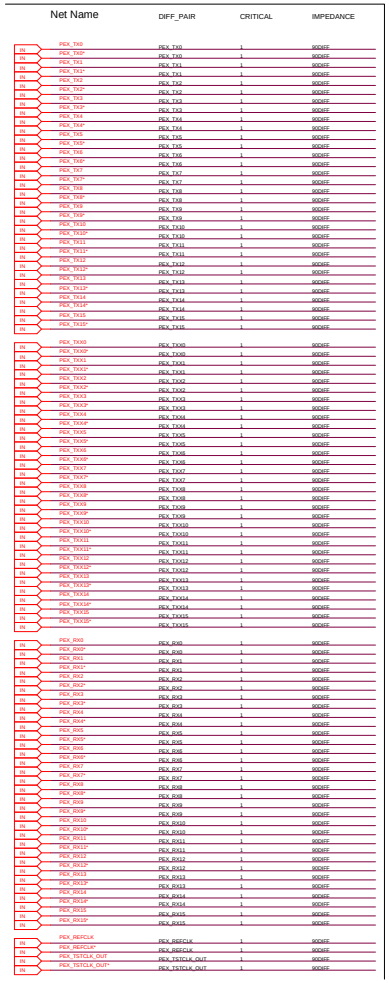
NAME		DATE	05-FEB-2009

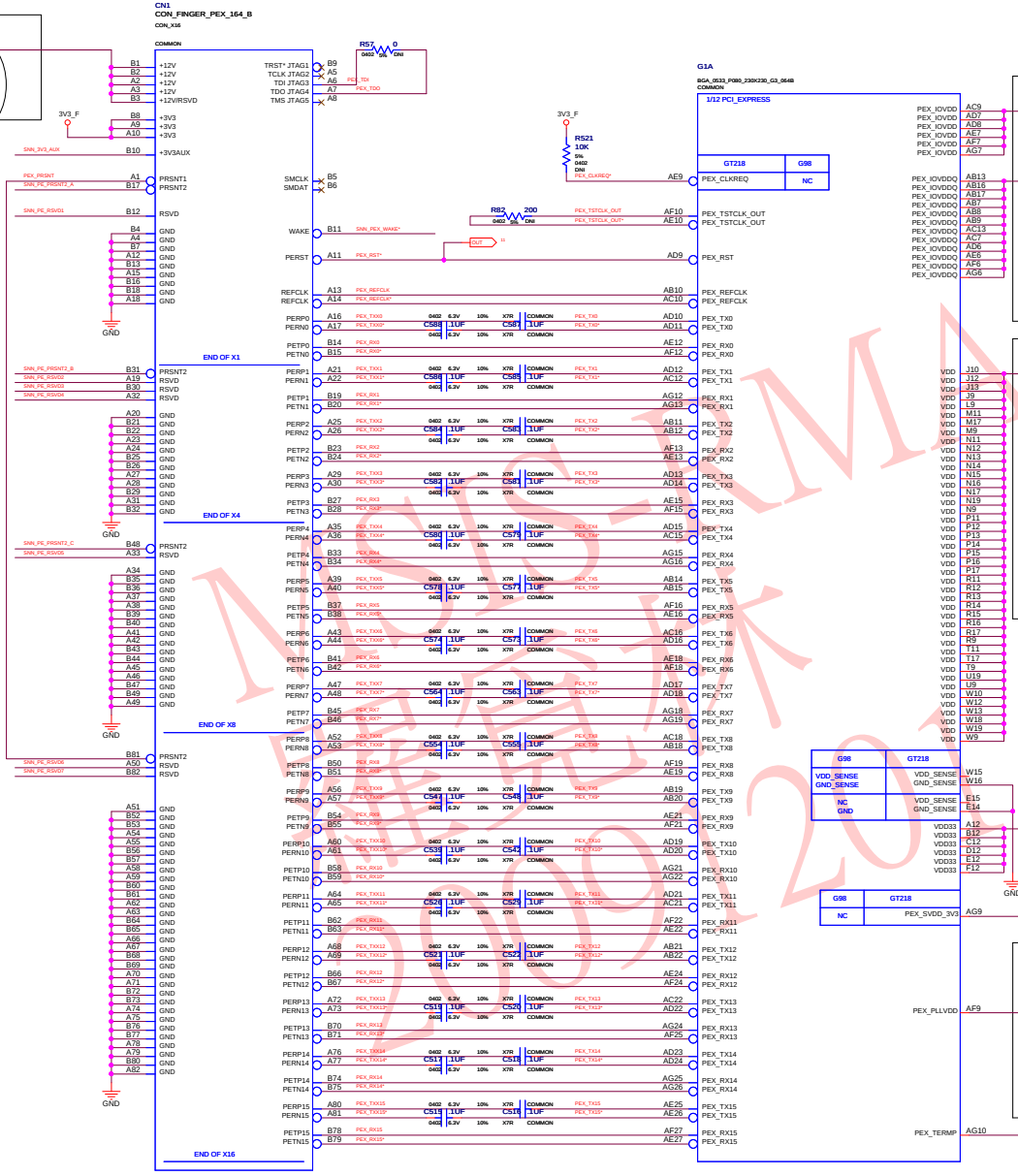
PCI Express Interface





9





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express Interface

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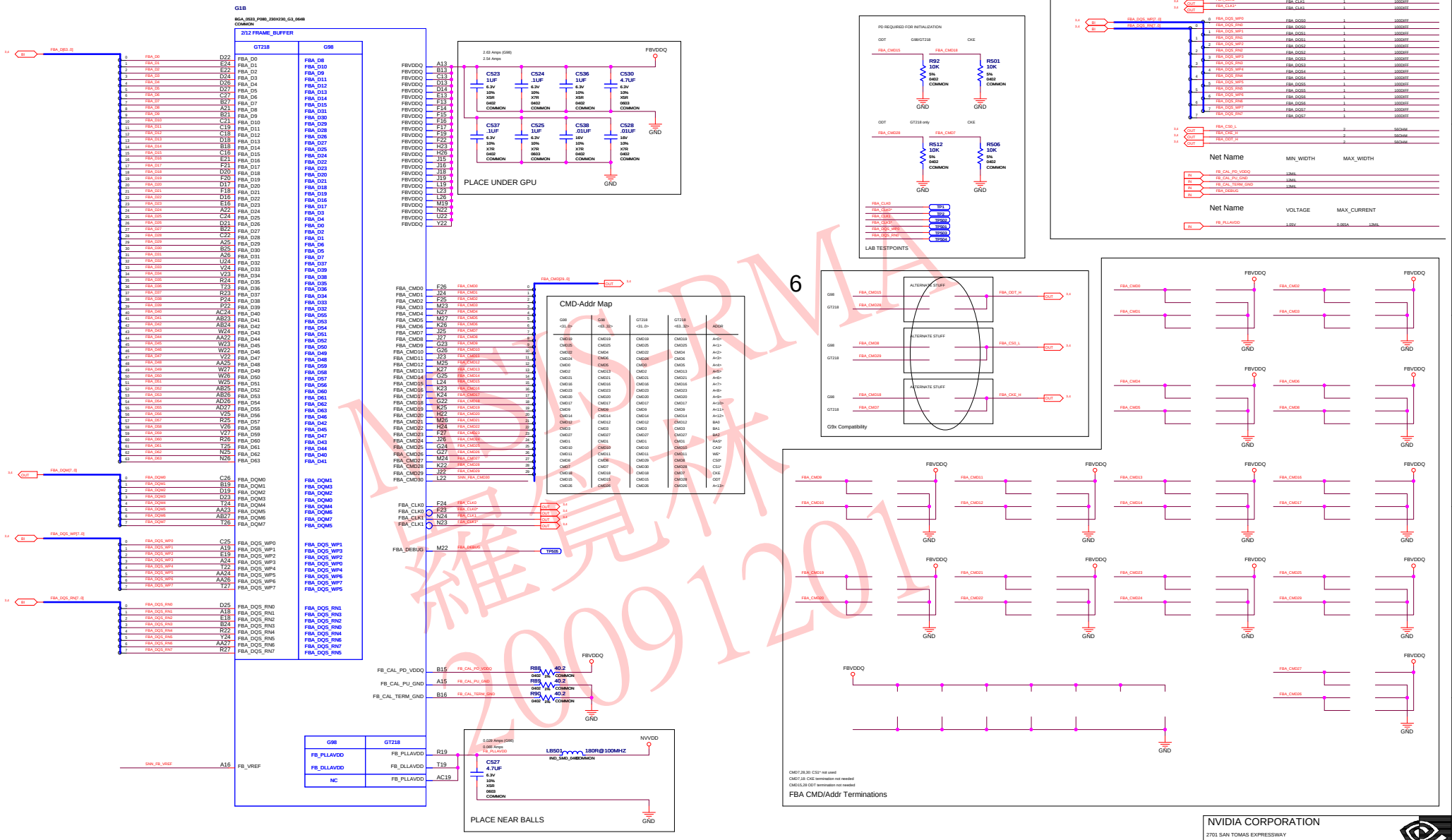
Frame Buffer Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Frame Buffer Interface

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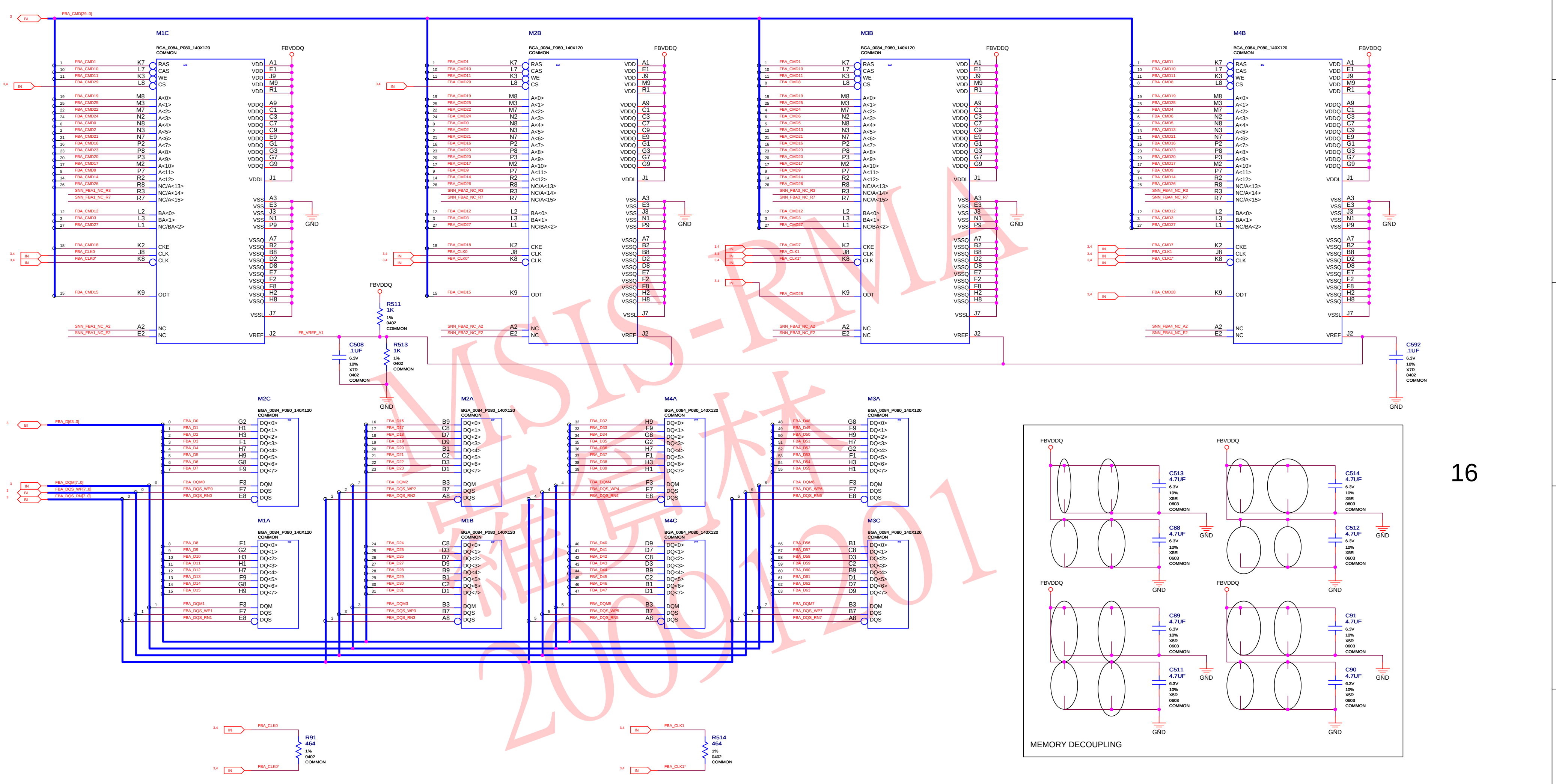
DDR2 Memories

Net Name	MIN_WIDTH	MAX_WIDTH
FB_VREF_A	12MIL	



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DDR2 Memories
NV_PN	600-10691-BASE-100 A
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DAC A Slim VGA

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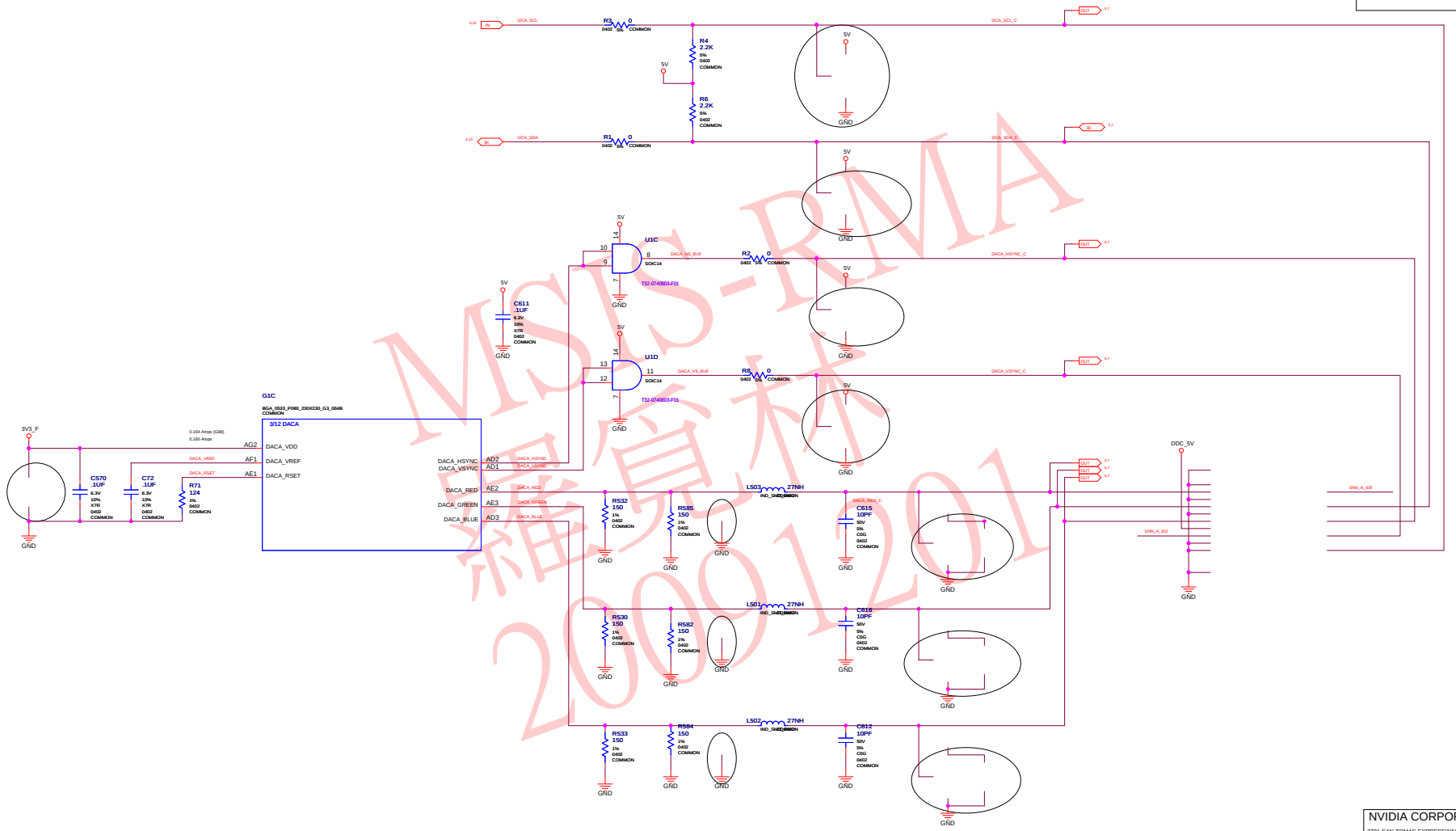
Net Name	CRITICAL	IMPEDANCE
DACA_RED	1	50OHM
DACA_GREEN	1	50OHM
DACA_BLUE	1	50OHM
DACA_RED_C	1	50OHM
DACA_GREEN_C	1	50OHM
DACA_BLUE_C	1	50OHM
DACA_HSYNC	2	50OHM
DACA_VSYNC	2	50OHM
DACA_HS_BUF	2	50OHM
DACA_VS_BUF	2	50OHM
DACA_HSYNC_C	2	50OHM
DACA_VSYNC_C	2	50OHM

Net Name	MIN_WIDTH	MAX_WIDTH
I2CA_SCL		
I2CA_SDA		
I2CA_SCL_C		
I2CA_SDA_C		
DACA_VREF	12MIL	
DACA_RSET	12MIL	



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DAC A Slim VGA

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DAC B VGA Header

Net Name	CRITICAL	IMPEDANCE
DACB_RED	1	50OHM
DACB_GREEN	1	50OHM
DACB_BLUE	1	50OHM
DACB_RED_C	1	50OHM
DACB_GREEN_C	1	50OHM
DACB_BLUE_C	1	50OHM
DACB_HSYNC	2	50OHM
DACB_VSYNC	2	50OHM
DACB_HSYNC_C	2	50OHM
DACB_VSYNC_C	2	50OHM
DACB_HS_BUF	2	50OHM
DACB_VS_BUF	2	50OHM

Net Name	MIN_WIDTH	MAX_WIDTH
I2CB_SCL		
I2CB_SDA		
I2CB_SCL_C		
I2CB_SDA_C		
DACB_VREF	12MIL	
DACB_RSET	12MIL	

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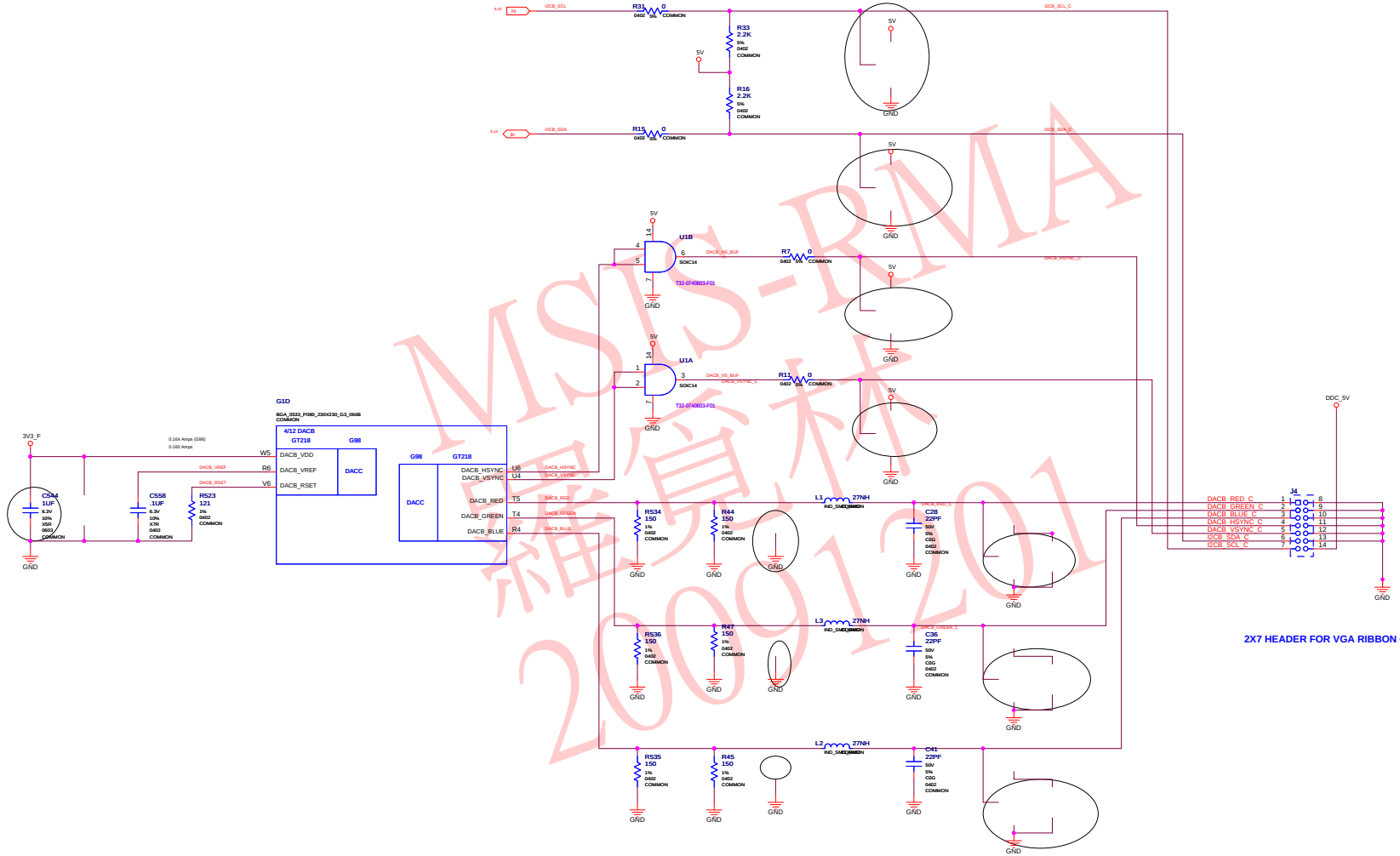

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DAC B VGA Header

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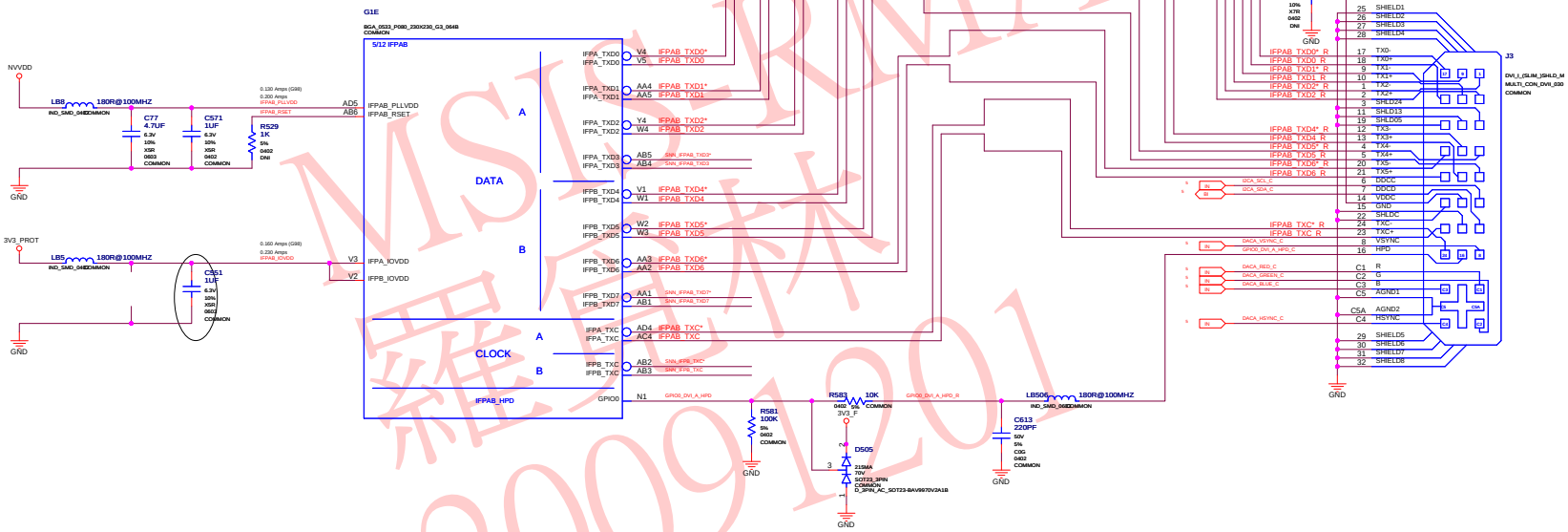
TMDS Interface



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Net Name	DIFF_PAIR	CRITICAL	IMPEDANCE
IFPAB_TXD0*	IFPAB_TXD0	1	90OHM
IFPAB_TXD0	IFPAB_TXD0	1	90OHM
IFPAB_TXD1*	IFPAB_TXD1	1	90OHM
IFPAB_TXD1	IFPAB_TXD1	1	90OHM
IFPAB_TXD2*	IFPAB_TXD2	1	90OHM
IFPAB_TXD2	IFPAB_TXD2	1	90OHM
IFPAB_TXD4*	IFPAB_TXD4	1	90OHM
IFPAB_TXD4	IFPAB_TXD4	1	90OHM
IFPAB_TXD5*	IFPAB_TXD5	1	90OHM
IFPAB_TXD5	IFPAB_TXD5	1	90OHM
IFPAB_TXD6*	IFPAB_TXD6	1	90OHM
IFPAB_TXD6	IFPAB_TXD6	1	90OHM
IFPAB_TXC*	IFPAB_TXC	1	90OHM
IFPAB_TXC	IFPAB_TXC	1	90OHM

Net Name	MIN_WIDTH	MAX_WIDTH
GPIO0_DVI_A_HPD		
GPIO0_DVI_A_HPD_R		
GPIO0_DVI_A_HPD_C		

Net Name	VOLTAGE	MAX_CURRENT		
IFPAB_PLLVDD	1.05V	0.200A	19MIL	
IFPAB_IOVDD	3.3V	0.230A	19MIL	
IFPAB_RSET			12MIL	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS Interface

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HDMI Connector

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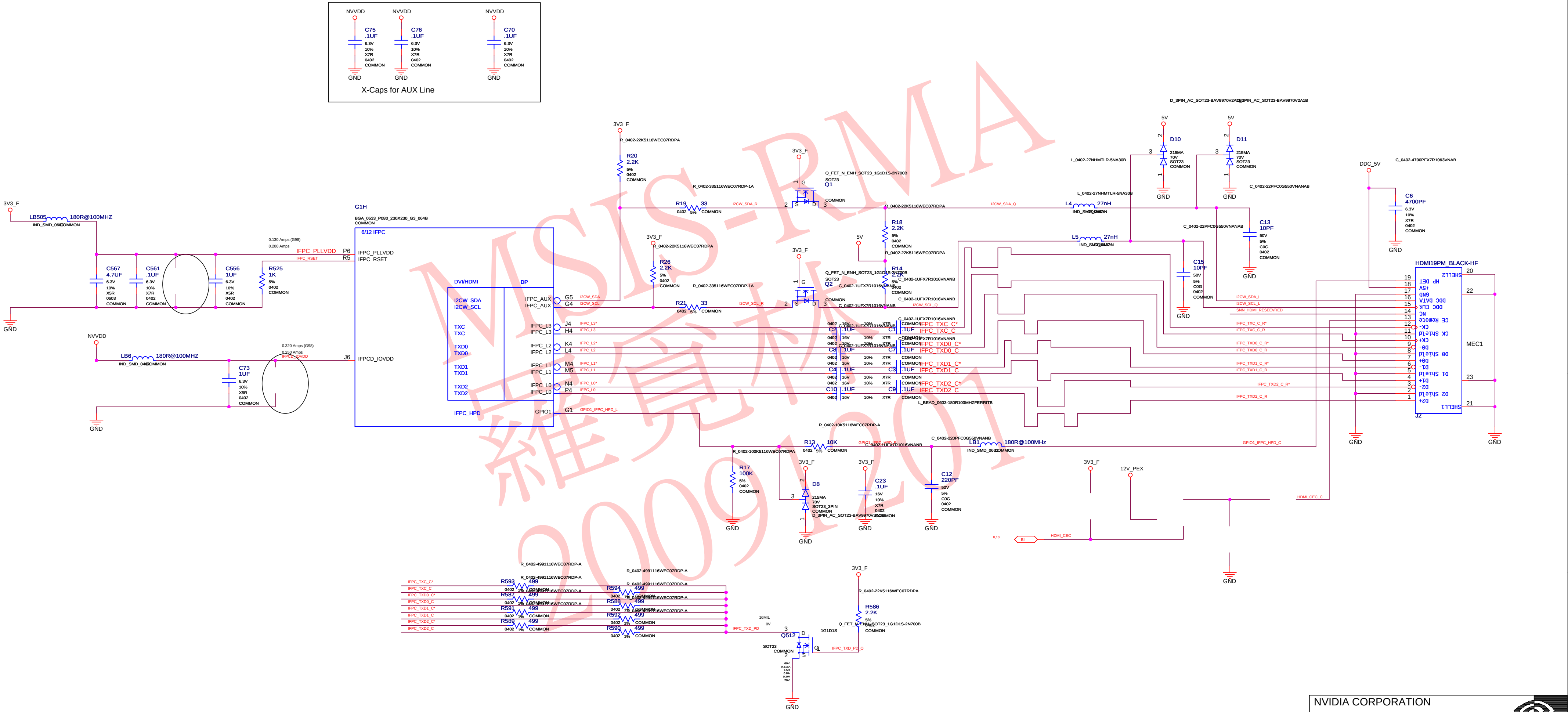
Net Name	MIN_WIDTH	MAX_WIDTH
GPIO_DP_HPD_C (IN)		
GPIO_DP_HPD_R (IN)		
GPIO_DP_HPD (IN)		
GPIO19_IFPD_HPD (IN)		
GPIO15_G98_IFPE_HPD (OUT, 8,9)		
IFPD_AUX_SEL (IN)		
DP_MODE* (IN)		
DP_MODE_C (IN)		
GPIO18_G98_DP_MODE (OUT, 8,10)		
I2CD_SDA (BI, 8,10)		
I2CD_SCL (IN, 8,10)		

Net Name	VOLTAGE	MAX_CURRENT	
IFPD_PLLVDD (IN)	3.3V	0.200A	16MIL
IFPD_RSET (IN)			12MIL

Net Name	DIFF_PAIR	CRITICAL	IMPEDANCE
IFPD_AUX*	IFPD_AUX	1	90DIFF
IFPD_AUX	IFPD_AUX	1	90DIFF
IFPD_AUX_RC*	IFPD_AUX_RC	1	90DIFF
IFPD_AUX_RC	IFPD_AUX_RC	1	90DIFF
IFPD_AUX_BYP*	IFPD_AUX_BYP	1	90DIFF
IFPD_AUX_BYP	IFPD_AUX_BYP	1	90DIFF
IFPD_AUX_C*	IFPD_AUX_C	1	90DIFF
IFPD_AUX_C	IFPD_AUX_C	1	90DIFF
IFPD_L3*	IFPD_L3	1	90DIFF
IFPD_L3	IFPD_L3	1	90DIFF
IFPD_L2*	IFPD_L2	1	90DIFF
IFPD_L2	IFPD_L2	1	90DIFF
IFPD_L1*	IFPD_L1	1	90DIFF
IFPD_L1	IFPD_L1	1	90DIFF
IFPD_L0*	IFPD_L0	1	90DIFF
IFPD_L0	IFPD_L0	1	90DIFF
IFPD_L3_C*	IFPD_L3_C	1	90DIFF
IFPD_L3_C	IFPD_L3_C	1	90DIFF
IFPD_L2_C*	IFPD_L2_C	1	90DIFF
IFPD_L2_C	IFPD_L2_C	1	90DIFF
IFPD_L1_C*	IFPD_L1_C	1	90DIFF
IFPD_L1_C	IFPD_L1_C	1	90DIFF
IFPD_L0_C*	IFPD_L0_C	1	90DIFF
IFPD_L0_C	IFPD_L0_C	1	90DIFF



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DisplayPort Connector
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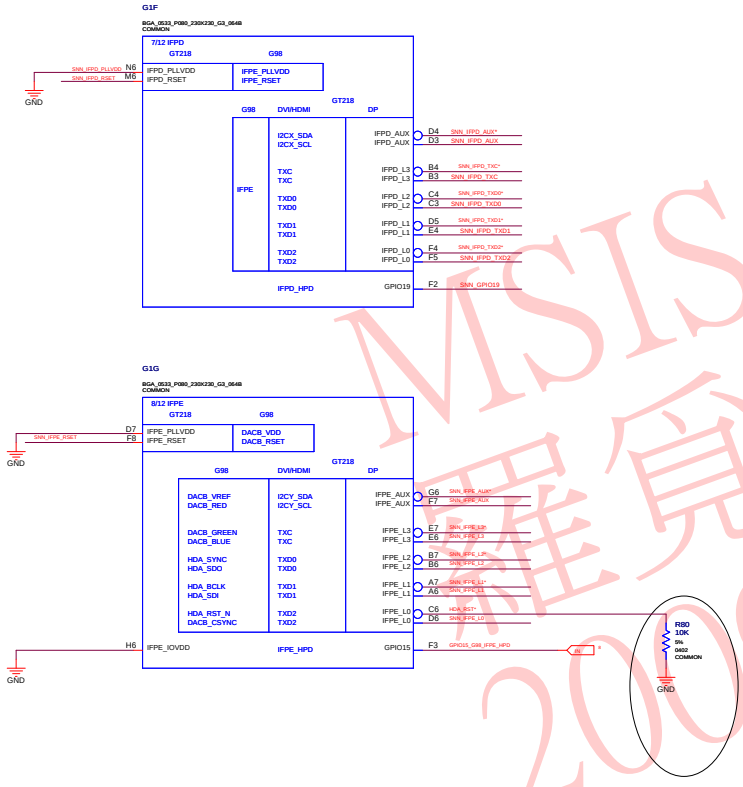
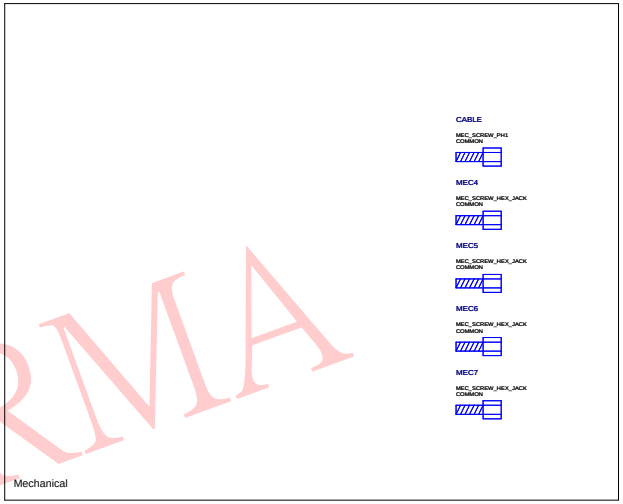
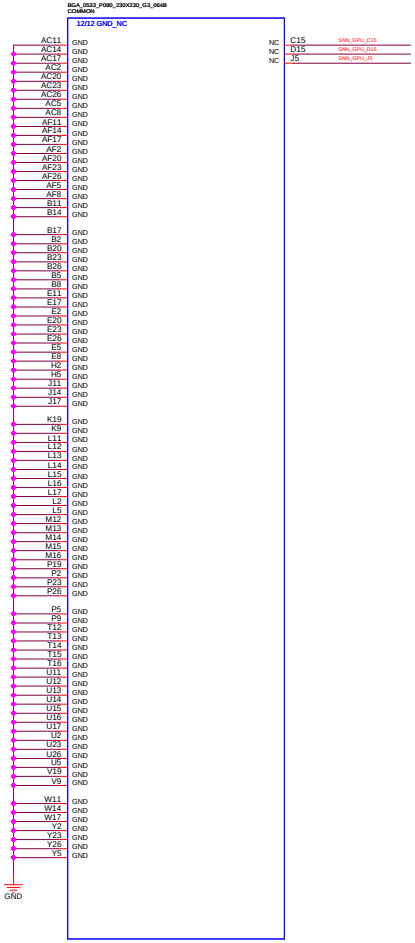
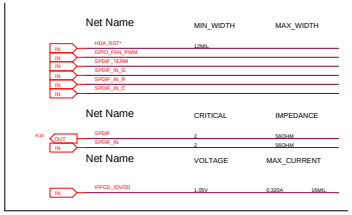
IFPC, IFPE Interface, Mechanical, SPDIF









ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPC, IFPE Interface, Mechanical, SPDIF

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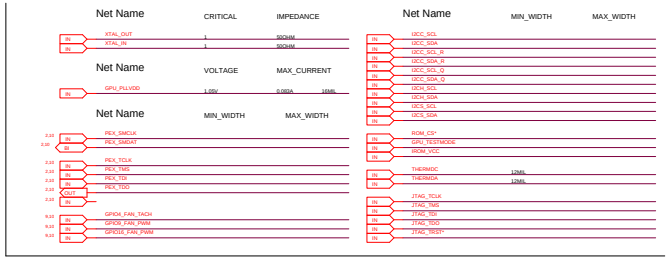
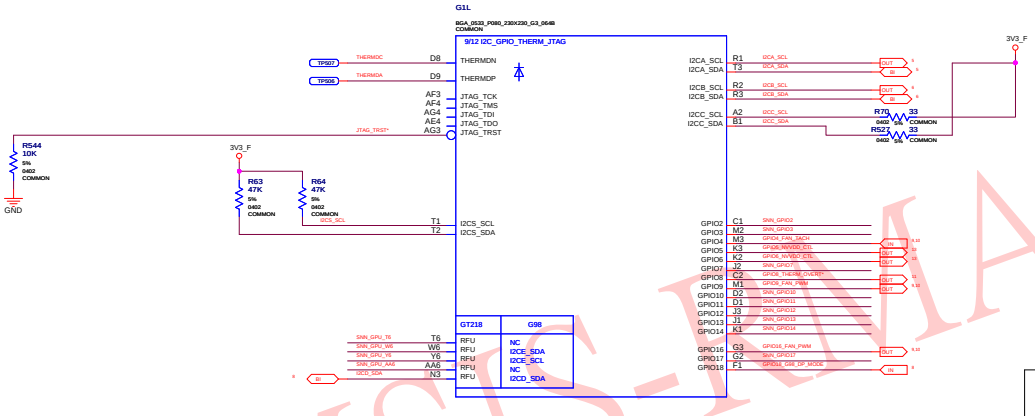
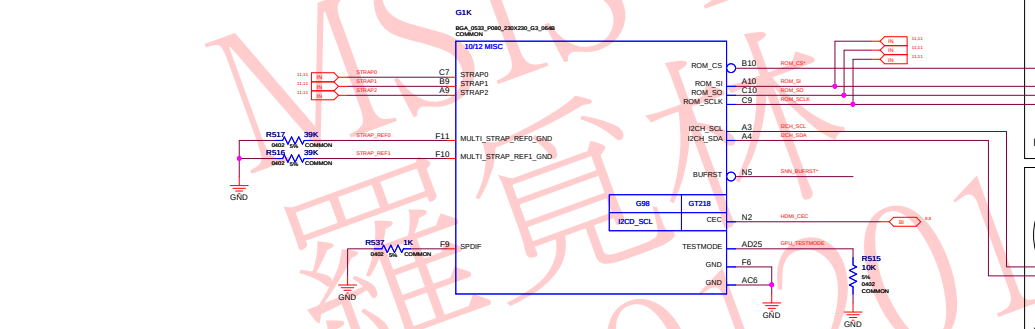
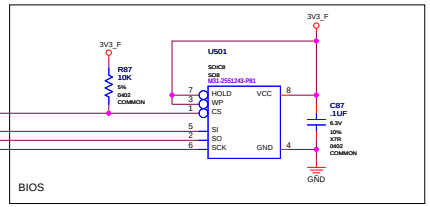
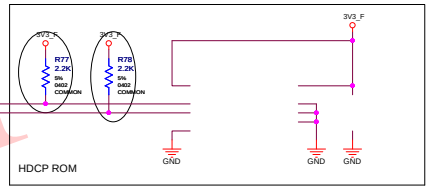
XTAL, ROM, JTAG

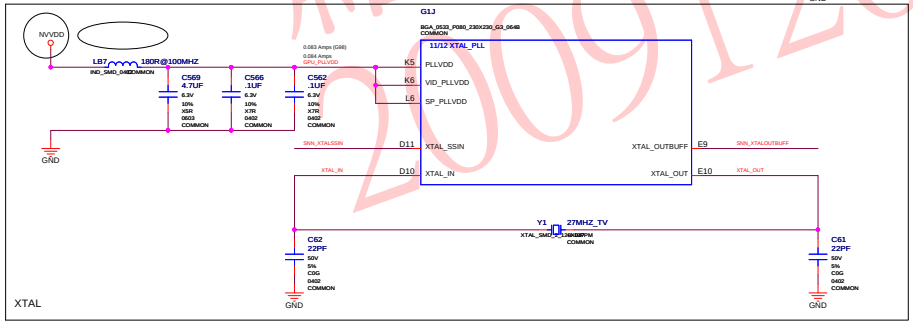












ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	XTAL, ROM, JTAG

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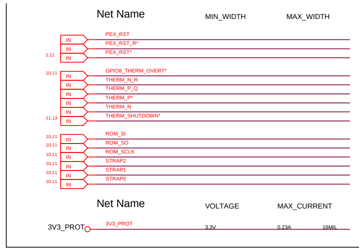
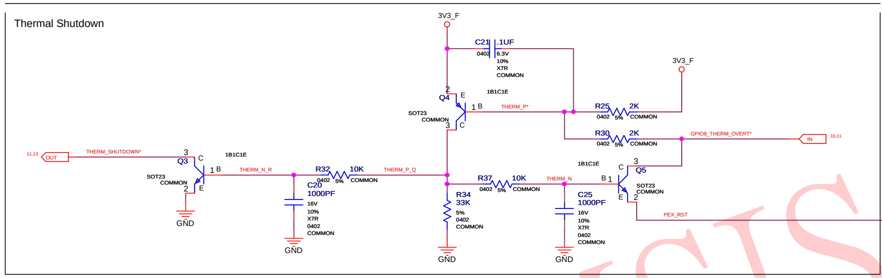
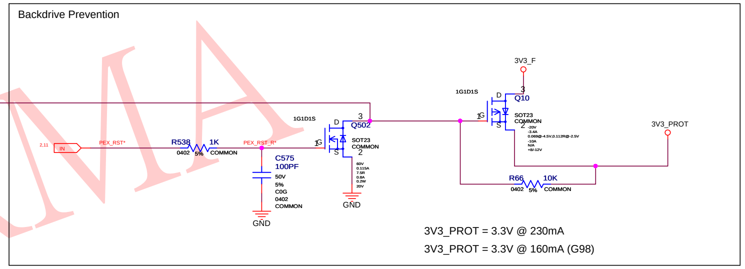
Thermal Protection, Protected 3V3, Straps







GT218 Straps MLS Mode

Bit	Signal	Values		Values	
03:	RAMCFG[3]	0000	Elpida		
		0001	Samsung, Micron		
02:	RAMCFG[2]	0010	Qimonda		
		0011	Hynix		
01:	RAMCFG[1]	0100	Nanya		
00:	RAMCFG[0]				
03:	XCLK_417	0	277 (Default)		
02:	FB[0]	0	256M (Default)		
01:	SMB_ALT_ADDR	0	0x9E		
		1	0x9C		
00:	VGA_DEVICE	0	Class code 302		
		1	Class code 300		
03:	PCI_DEVID_EXT	0	GT218-300-A1		
02:	SUB_VENDOR	0	No BIOS		
		1	BIOS		
01:	SLOT_CLK_CFG	0	Disable		
		1	Enable		
00:	PEX_PLL_EN_TERM100	0	Disable		
		1	Enable		
03:	PCI_DEVID[3]	0000	GT218-300-A1		
02:	PCI_DEVID[2]				
01:	PCI_DEVID[1]				
00:	PCI_DEVID[0]				
03:	3GIO_PADCFG_LUT_ADR[3]	0000	DSKTOP_DEFAULT	1000	DSKTOP_HTHRS
		0001	MOBILE_DEFAULT	1001	MOBILE_HTHRS_NAMP
02:	3GIO_PADCFG_LUT_ADR[2]	0010	MOBILE_NTHRS_LLAMP	1010	MOBILE_HTHRS_LLAMP
		0011	MOBILE_NTHRS_LAMP	1011	MOBILE_HTHRS_LAMP
01:	3GIO_PADCFG_LUT_ADR[1]	0100	MOBILE_NTHRS_HAMP	1100	MOBILE_HTHRS_HAMP
		0101	MOBILE_NTHRS_HHAMP	1101	MOBILE_HTHRS_HHAMP
00:	3GIO_PADCFG_LUT_ADR[0]	0110	MOBILE_NTHRS_HHHAMP	1110	MOBILE_HTHRS_HHHAMP
		0111	MOBILE_NTHRS_HHHHAMP	1111	MOBILE_HTHRS_HHHHAMP
03:	USER[3]	0000	Default		
02:	USER[2]				
01:	USER[1]				
00:	USER[0]				

Multilevel Straps

5K to GND	0000
10K to GND	0001
15K to GND	0010
20K to GND	0011
25K to GND	0100
30K to GND	0101
35K to GND	0110
45K to GND	0111
5K to VCC	1000
10K to VCC	1001
15K to VCC	1010
20K to VCC	1011
25K to VCC	1100
30K to VCC	1101
35K to VCC	1110
45K to VCC	1111

GT218 Straps BU Mode

Bit Signal	Values	
PCI_DEVID_EXT	0	GT218-300-A1
XCLK_417	0	277 (Default)
3GIO_PADCFG_LUT_ADR[3]	0000	DSKTOP_DEFAULT
	0001	MOBILE_DEFAULT
	0010	MOBILE_NTHRS_LLAMP
	0011	MOBILE_NTHRS_LAMP
	0100	MOBILE_NTHRS_HAMP
	0101	MOBILE_NTHRS_HHAMP
	0110	MOBILE_NTHRS_HHHAMP
	0111	MOBILE_NTHRS_HHHHAMP
	1000	DSKTOP_HTHRS
	1001	MOBILE_HTHRS_NAMP
	1010	MOBILE_HTHRS_LLAMP
	1011	MOBILE_HTHRS_LAMP
3GIO_PADCFG_LUT_ADR[2]	1100	MOBILE_HTHRS_HAMP
	1101	MOBILE_HTHRS_HHAMP
	1110	MOBILE_HTHRS_HHHAMP
	1111	MOBILE_HTHRS_HHHHAMP
3GIO_PADCFG_LUT_ADR[1]		
3GIO_PADCFG_LUT_ADR[0]		

GT218 Straps PM Mode

Bit Signal	Values	
PCI_DEVID_EXT	0	GT218-300-A1
XCLK_417	0	277/277 OR 417/417
PCI_DEVID[3]	0	GT218-300-A1
RAMCFG[2]	0000	Elpida
	0001	Samsung, Micron
	0010	Qimonda
	0011	Hynix
	0100	Nanya
RAMCFG[1]		
RAMCFG[0]		

Mode	REF0/REF1
MLS	Stuff
BU	No stuff
PM	Stuff one

G98 Straps MLS Mode

Bit	Signal	Values	
03:	RAMCFG[3]	0000	Elpida
		0100	Nanya
02:	RAMCFG[2]	0101	Samsung
		0110	Qimonda
01:	RAMCFG[1]	0111	Hynix
00:	RAMCFG[0]		
03:	XCLK_277	1	Enabled
02:	TVMODE[2]	001	NTSC_J
01:	TVMODE[1]		
00:	TVMODE[0]		
03:	PCI_DEVID_EXT	0	G98-409-U2
			G98-400-A2
			G98-400-U2
02:	SUB_VENDOR	1	BIOS
01:	SLOT_CLK_CFG	0	Disable
		1	Enable
00:	PEX_PLL_EN_TERM100	0	Disable
03:	PCI_DEVID[3]	0000	RFU
		0100	G98-409-U2
02:	PCI_DEVID[2]	0100	G98-400-A2
		0100	G98-400-U2
01:	PCI_DEVID[1]		
00:	PCI_DEVID[0]		
03:	3GIO_PADCFG_LUT_ADR[3]	0000	DSKTOP_DEFAULT
02:	3GIO_PADCFG_LUT_ADR[2]		
01:	3GIO_PADCFG_LUT_ADR[1]		
00:	3GIO_PADCFG_LUT_ADR[0]		
03:	USER[3]	0000	Default
02:	USER[2]		
01:	USER[1]		
00:	USER[0]		

Multilevel Straps

5K to GND	0000
10K to GND	0001
15K to GND	0010
20K to GND	0011
25K to GND	0100
30K to GND	0101
35K to GND	0110
45K to GND	0111
5K to VCC	1000
10K to VCC	1001
15K to VCC	1010
20K to VCC	1011
25K to VCC	1100
30K to VCC	1101
35K to VCC	1110
45K to VCC	1111

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Protection, Protected 3V3, Straps

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN 600-10691-BASE-100 A
ID | PAGE
NAME | DATE 05-FEB-2009

Power Supply I: FBVDD/Q, PEX_VDD, 5V, 3V3_F

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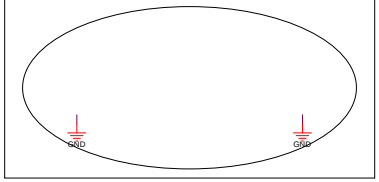
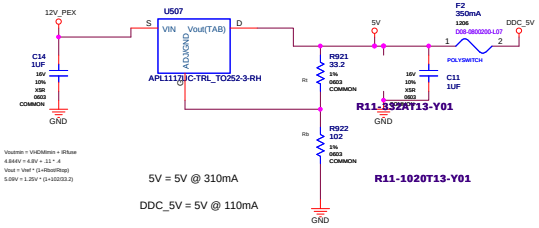
3V3_F = 3.3V @ 1.6A

3V3_F = 3.3V @ 1.2A (G98)



Net Name	MIN_WIDTH	MAX_WIDTH
PS_5V_ADJ		
PS_PEX_DR	16MIL	
PS_PEX_FB	12MIL	
PS_PEX_CP	12MIL	
PS_FBVDDQ_EN		
PS_FBVDDQ_EN*		
PS_FBVDDQ_FS	12MIL	
PS_FBVDDQ_VCC5	12MIL	
PS_FBVDDQ_VCC12	12MIL	
PS_FBVDDQ_PVCC5	12MIL	
PS_FBVDDQ_ROOT	12MIL	
PS_FBVDDQ_UG	16MIL	
PS_FBVDDQ_UG_R	16MIL	
PS_FBVDDQ_PHASE	16MIL	
PS_FBVDDQ_LG	16MIL	
PS_FBVDDQ_FB	12MIL	
PS_FBVDDQ_FB_RC	12MIL	
PS_FBVDDQ_CP	12MIL	
PS_FBVDDQ_CP_RC	12MIL	
PS_FBVDDQ_RC	16MIL	
PS_3V3_SS		
PS_3V3_SET		
PS_3V3_FAULT		

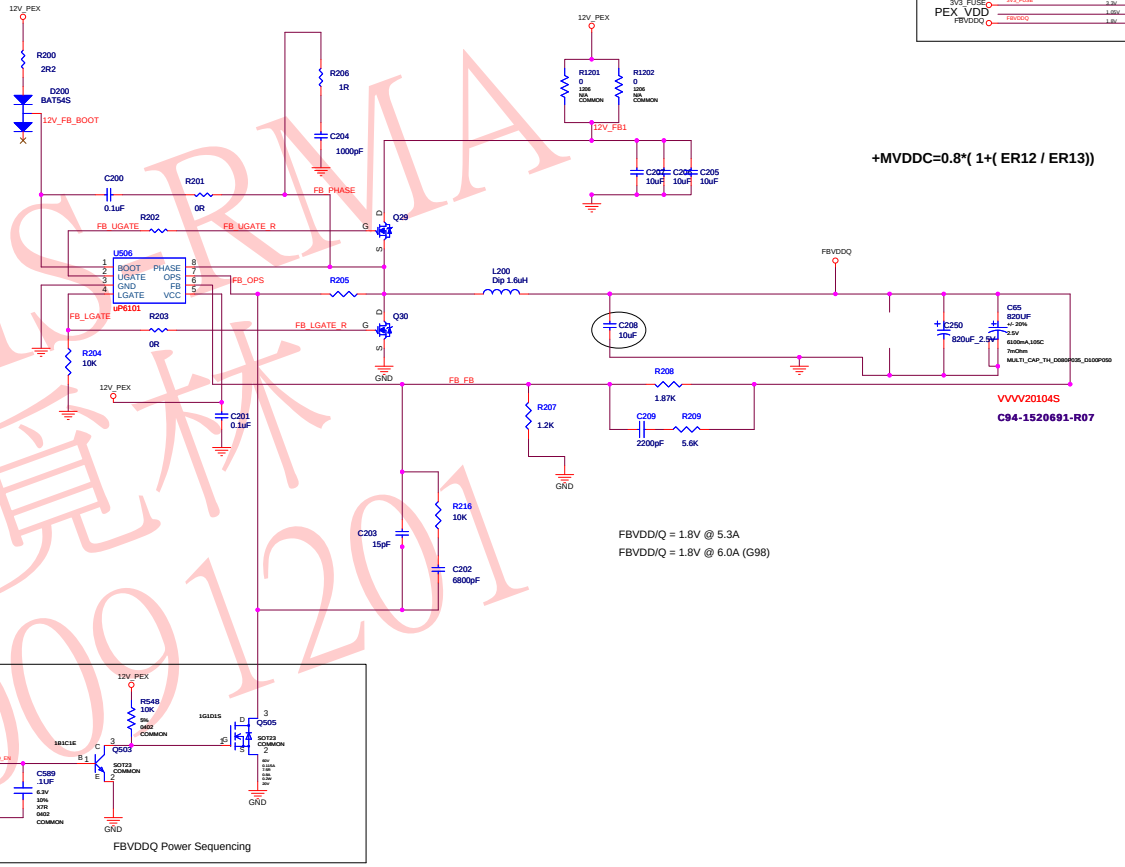
Net Name	VOLTAGE	MAX_CURRENT	
5V	5V	0.310A	12MIL
DDC_5V	5V	0.110A	12MIL
3V3_F	3.3V	1.6A	16MIL
3V3_FUSE	3.3V	0.500A	12MIL
PEX_VDD	1.05V	2.2A	24MIL
FBVDDQ	1.8V	6.0A	36MIL



5V = 5V @ 310mA

DDC_5V = 5V @ 110mA

R11-1020T13-Y01



+MVDDC=0.8*(1+(ER12 / ER13))

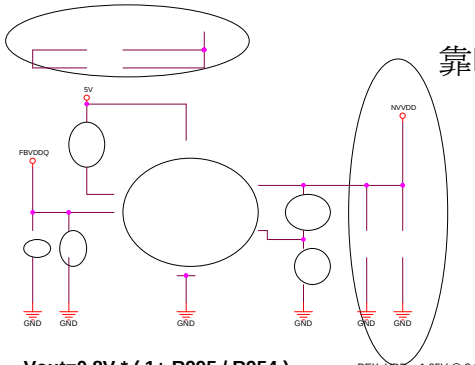
VVVV20104S

C94-1520691-R07

FBVDDQ/Q = 1.8V @ 5.3A

FBVDDQ/Q = 1.8V @ 6.0A (G98)

靠PEX_VDD



Vout=0.8V * (1+ R995 / R954)

PEX_VDD = 1.05V @ 2.2A

PEX_VDD = 1.05V @ 1.9A (G98)

FBVDDQ Power Sequencing

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply I: FBVDDQ, PEX_VDD, 5V, 3V3_F

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2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10691-BASE-100 A		
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Power Supply II: PEX_PLLVDD, NVVDD

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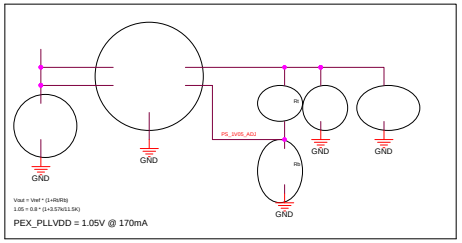

Net Name	MIN_WIDTH	MAX_WIDTH	CRITICAL
PS_NVVDD_FS	12MIL		
PS_NVVDD_EAT	12MIL		
PS_NVVDD_VCC12	12MIL		
PS_NVVDD_VCC5	12MIL		
PS_NVVDD_PVCC5	12MIL		
PS_NVVDD_BOOT	12MIL		
PS_NVVDD_BOOT_R	12MIL		
PS_NVVDD_LDO			
PS_NVVDD_UG	16MIL		
PS_NVVDD_UG_R	16MIL		
PS_NVVDD_PHASE	16MIL		
PS_NVVDD_LG	16MIL		
PS_NVVDD_LG_D	16MIL		
PS_NVVDD_LG_R	16MIL		
PS_NVVDD_RC	16MIL		
PS_NVVDD_FB	12MIL		
PS_NVVDD_FB_RC	12MIL		
PS_NVVDD_CF	12MIL		
PS_NVVDD_CF_RC	12MIL		
NVVDD_SENSE			
GPIO6_NVVDD_CTL			
GPIO6_NVVDD_CTL_Q	12MIL		
GPIO6_NVVDD_CTL			
GPIO6_NVVDD_CTL_Q	12MIL		
PS_1V05_ADJ			

Net Name	VOLTAGE	MAX_CURRENT	POWER_NET
12V_PEX	12V	5.5A	36MIL TRUE
3V3_PEX	3.3V	3.0A	16MIL TRUE
NVVDD	1.1V	11.7A	30MIL
PEX_PLLVDD	1.05V	0.17A	12MIL

NVVDD = 0.95V @ 14.5A

NVVDD Power Sequencing

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply II: PEX_PLLVDD, NVVDD

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10691-BASE-100 A		
ID		PAGE	
NAME		DATE	05-FEB-2009

Title: Basenet Report
Design: p691_a01
Date: Jan 27 23:02:52 2009

Base nets and synonyms for
p691_a01_lib.P691_A01(@p691_a01_lib.p691
_a01(sch_1))
Base Signal Location([Zone][dir])

3V3_F 12.2H
3V3_FUSE 12.2H
3V3_PEX 13.2G
3V3_PROT 11.1H
5V 12.2H
12V_PEX 13.2G
DACA_BLUE 5.1G< 5.4C
DACA_BLUE_C 5.1G> 5.4F> 7.3F<
DACA_GREEN 5.1G< 5.4C
DACA_GREEN_C 5.1G> 5.4F> 7.3F<
DACA_HSYNC 5.1G< 5.4C
DACA_HSYNC_C 5.1G> 5.3F> 7.4F<
DACA_HS_BUF 5.1G< 5.3D
DACA_RED 5.1G< 5.4C
DACA_RED_C 5.1G> 5.4F> 7.3F<
DACA_RSET 5.1G< 5.4B
DACA_VREF 5.1G< 5.4B
DACA_VSYNC 5.1G< 5.4C
DACA_VSYNC_C 5.1G> 5.3F> 7.3F<
DACA_VS_BUF 5.1G< 5.3D
DACB_BLUE 6.1G< 6.4C
DACB_BLUE_C 6.1G< 6.5E
DACB_GREEN 6.1G< 6.4C
DACB_GREEN_C 6.1G< 6.4E
DACB_HSYNC 6.1G< 6.4C
DACB_HSYNC_C 6.1G< 6.3E
DACB_HS_BUF 6.1G< 6.3D
DACB_RED 6.1G< 6.4C
DACB_RED_C 6.1G< 6.4E
DACB_RSET 6.1G< 6.4B
DACB_VREF 6.1G< 6.4B
DACB_VSYNC 6.1G< 6.4C
DACB_VSYNC_C 6.1G< 6.3E
DACB_VS_BUF 6.1G< 6.3D
DDC_5V 12.2H
DP_MODE* 8.1F< 8.2G
DP_MODE_C 8.1F< 8.3H
FBA_CKE_H 3.2G> 3.3F> 4.2D<
4.2F<
FBA_CLK0 3.1G> 3.2E 3.4D>
4.2A< 4.2C< 4.5B<
FBA_CLK0* 3.1G> 3.2E 3.4D>
4.2A< 4.2C< 4.5B<
FBA_CLK1 3.1G> 3.2E 3.4D>
4.2D< 4.2F< 4.5D<
FBA_CLK1* 3.1G> 3.2E 3.4D>
4.2D< 4.2F< 4.5D<
FBA_CMD<0> 3.2C 3.2G 4.2A 4.2C
FBA_CMD<29..0> 3.1G> 3.2D> 4.1A<>
FBA_CMD<1> 3.2C 3.2G 4.1A 4.1C
4.1E 4.1G
FBA_CMD<2> 3.2C 3.2H 4.2A 4.2C
FBA_CMD<3> 3.2C 3.2H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<4> 3.2C 3.3G 4.2E 4.2G
FBA_CMD<5> 3.3C 3.3G 4.2E 4.2G
FBA_CMD<6> 3.3C 3.3H 4.2E 4.2G
FBA_CMD<7> 3.2F 3.3C 3.3E
FBA_CMD<8> 3.3C 3.3E 3.3H 4.2E
4.2G
FBA_CMD<9> 3.3C 3.3E 4.2A 4.2C
4.2E 4.2G
FBA_CMD<10> 3.3C 3.3E 4.1A 4.1C
4.1E 4.1G
FBA_CMD<11> 3.3C 3.3F 4.1A 4.1C
4.1E 4.1G
FBA_CMD<12> 3.3C 3.3F 4.2A 4.2C
4.2E 4.2G
FBA_CMD<13> 3.3C 3.3G 4.2E 4.2G
FBA_CMD<14> 3.3C 3.3G 4.2A 4.2C
4.2E 4.2G
FBA_CMD<15> 3.1E 3.2E 3.3C 4.3A
4.3C
FBA_CMD<16> 3.3C 3.3H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<17> 3.3C 3.3H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<18> 3.1F 3.3C 3.3E 4.2A
4.2C
FBA_CMD<19> 3.3C 3.4E 4.2A 4.2C
4.2E 4.2G
FBA_CMD<20> 3.3C 3.4E 4.2A 4.2C
4.2E 4.2G
FBA_CMD<21> 3.3C 3.4F 4.2A 4.2C
4.2E 4.2G
FBA_CMD<22> 3.3C 3.4F 4.2A 4.2C
FBA_CMD<23> 3.3C 3.4G 4.2A 4.2C
4.2E 4.2G
FBA_CMD<24> 3.3C 3.4G 4.2A 4.2C
FBA_CMD<25> 3.3C 3.4H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<26> 3.3C 3.4H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<27> 3.3C 3.4H 4.2A 4.2C
4.2E 4.2G
FBA_CMD<28> 3.2E 3.2E 3.3C
FBA_CMD<29> 3.3C 3.3E 3.4H
FBA_CS0_L 3.2G> 3.3F> 4.2A<
4.2C<
FBA_D<0> 3.1B 4.3B
FBA_D<63..0> 3.1A<> 3.1G<> 4.3A<>
FBA_D<1> 3.1B 4.3B
FBA_D<2> 3.1B 4.3B
FBA_D<3> 3.1B 4.3B
FBA_D<4> 3.1B 4.3B
FBA_D<5> 3.1B 4.3B
FBA_D<6> 3.1B 4.3B
FBA_D<7> 3.1B 4.3B
FBA_D<8> 3.1B 4.4B
FBA_D<9> 3.1B 4.4B
FBA_D<10> 3.1B 4.4B
FBA_D<11> 3.2B 4.4B
FBA_D<12> 3.2B 4.4B
FBA_D<13> 3.2B 4.4B
FBA_D<14> 3.2B 4.4B
FBA_D<15> 3.2B 4.4B
FBA_D<16> 3.2B 4.3C
FBA_D<17> 3.2B 4.3C
FBA_D<18> 3.2B 4.3C
FBA_D<19> 3.2B 4.3C
FBA_D<20> 3.2B 4.3C
FBA_D<21> 3.2B 4.3C
FBA_D<22> 3.2B 4.3C
FBA_D<23> 3.2B 4.3C
FBA_D<24> 3.2B 4.4C
FBA_D<25> 3.2B 4.4C
FBA_D<26> 3.2B 4.4C
FBA_D<27> 3.2B 4.4C
FBA_D<28> 3.2B 4.4C
FBA_D<29> 3.2B 4.4C
FBA_D<30> 3.2B 4.4C
FBA_D<31> 3.2B 4.4C
FBA_D<32> 3.2B 4.3D
FBA_D<33> 3.2B 4.3D
FBA_D<34> 3.2B 4.3D
FBA_D<35> 3.2B 4.3D
FBA_D<36> 3.2B 4.3D
FBA_D<37> 3.2B 4.3D
FBA_D<38> 3.2B 4.3D
FBA_D<39> 3.2B 4.3D
FBA_D<40> 3.2B 4.4D
FBA_D<41> 3.3B 4.4D
FBA_D<42> 3.3B 4.4D
FBA_D<43> 3.3B 4.4D
FBA_D<44> 3.3B 4.4D
FBA_D<45> 3.3B 4.4D
FBA_D<46> 3.3B 4.4D
FBA_D<47> 3.3B 4.4D
FBA_D<48> 3.3B 4.3E
FBA_D<49> 3.3B 4.3E
FBA_D<50> 3.3B 4.3E
FBA_D<51> 3.3B 4.3E
FBA_D<52> 3.3B 4.3E
FBA_D<53> 3.3B 4.3E
FBA_D<54> 3.3B 4.3E
FBA_D<55> 3.3B 4.3E
FBA_D<56> 3.3B 4.4E
FBA_D<57> 3.3B 4.4E
FBA_D<58> 3.3B 4.4E
FBA_D<59> 3.3B 4.4E
FBA_D<60> 3.3B 4.4E
FBA_D<61> 3.3B 4.4E
FBA_D<62> 3.3B 4.4E
FBA_D<63> 3.3B 4.4E
FBA_DEBUG 3.2G< 3.4C
FBA_DQM<0> 3.3B 4.3B
FBA_DQM<7..0> 3.1G> 3.3A> 4.4A<
FBA_DQM<1> 3.3B 4.4B
FBA_DQM<2> 3.3B 4.3C
FBA_DQM<3> 3.3B 4.4C
FBA_DQM<4> 3.3B 4.3D
FBA_DQM<5> 3.4B 4.4D
FBA_DQM<6> 3.4B 4.3E
FBA_DQM<7> 3.4B 4.4E
FBA_DQS_RN<0> 3.1G 3.2E 3.4B 4.4B
FBA_DQS_RN<7..0> 3.1G<> 3.4A<> 4.4A<>
FBA_DQS_RN<1> 3.1G 3.4B 4.4B
FBA_DQS_RN<2> 3.1G 3.4B 4.4C
FBA_DQS_RN<3> 3.1G 3.4B 4.4C
FBA_DQS_RN<4> 3.1G 3.4B 4.4D
FBA_DQS_RN<5> 3.1G 3.4B 4.4D
FBA_DQS_RN<6> 3.1G 3.4B 4.4E
FBA_DQS_RN<7> 3.1G 3.4B 4.4E
FBA_DQS_WP<0> 3.1G 3.2E 3.4B 4.4B
FBA_DQS_WP<7..0> 3.1G<> 3.4A<> 4.4A<>
FBA_DQS_WP<1> 3.1G 3.4B 4.4B
FBA_DQS_WP<2> 3.1G 3.4B 4.4C
FBA_DQS_WP<3> 3.1G 3.4B 4.4C
FBA_DQS_WP<4> 3.1G 3.4B 4.4D
FBA_DQS_WP<5> 3.1G 3.4B 4.4D
FBA_DQS_WP<6> 3.1G 3.4B 4.4E
FBA_DQS_WP<7> 3.1G 3.4B 4.4E
FBA_ODT_H 3.2F> 3.2G> 4.3D<
4.3F<
FBVDDQ 12.2H
FB_CAL_PD_VDDQ 3.2G< 3.4C
FB_CAL_PU_GND 3.2G< 3.4C
FB_CAL_TERM_GND 3.2G< 3.4C
FB_PLLAVDD 3.2G< 3.5C
FB_VREF_A 4.1G< 4.3B
GPIO0_DVI_A_HPD 7.1G< 7.4D
GPIO0_DVI_A_HPD_C 7.1G< 7.3F
GPIO0_DVI_A_HPD_R 7.1G< 7.4E
GPIO4_FAN_TACH 9.5D> 10.1F< 10.2E<
GPIO5_NVDD_CTL 10.2E> 13.1G< 13.5D<
GPIO5_NVDD_CTL_Q 13.2G< 13.4E
GPIO6_NVDD_CTL 10.2E> 13.2G< 13.5G<
GPIO6_NVDD_CTL_Q 13.2G< 13.4F
GPIO8_THERM_OVERT* 10.2E> 11.1G< 11.2D<
GPIO9_FAN_PWM 9.5D< 10.1F< 10.2E>
GPIO15_G98_IFPE_HP 8.1F> 8.5C> 9.4D<
D
GPIO16_FAN_PWM 9.5D< 10.1F< 10.3E>
GPIO18_G98_DP_MODE 8.1F> 8.3G> 10.3E<
GPIO19_IFPD_HPD 8.1F< 8.5C
GPIO_DP_HPD 8.1F< 8.5D
GPIO_DP_HPD_C 8.1F< 8.4G
GPIO_DP_HPD_R 8.1F< 8.5E
GPIO_FAN_PWM 9.1G< 9.5E
GPU_PLLVDD 10.1F< 10.4C
GPU_TESTMODE 10.1G< 10.4E
HDA_RST* 9.1G< 9.4C
I2CA_SCL 5.1G< 5.2C< 10.2E>
I2CA_SCL_C 5.1F> 5.1G> 7.3F<
I2CA_SDA 5.1G<> 5.2C<> 10.2E<>
I2CA_SDA_C 5.1G<> 5.3F<> 7.3F<>
I2CB_SCL 6.1G< 6.2C< 10.2E>
I2CB_SCL_C 6.1G< 6.2E
I2CB_SDA 6.1G<> 6.2C<> 10.2E<>
I2CB_SDA_C 6.1G< 6.2E
I2CC_SCL 10.1G< 10.2E
I2CC_SCL_Q 10.1G< 10.2G
I2CC_SCL_R 10.1G< 10.2F
I2CC_SDA 10.1G< 10.2E
I2CC_SDA_Q 10.1G< 10.2G
I2CC_SDA_R 10.1G< 10.2F
I2CD_SCL 8.1F< 8.2G< 10.4E>
I2CD_SDA 8.1F<> 8.2G<> 10.3C<>
I2CH_SCL 10.1G< 10.3E
I2CH_SDA 10.1G< 10.3E
I2CS_SCL 10.1G< 10.2C
I2CS_SDA 10.1G< 10.2C
IFPAB_IOVDD 7.2G< 7.3C
IFPAB_PLLVDD 7.2G< 7.3C
IFPAB_RSET 7.2G< 7.3C
IFPAB_TXC 7.1G< 7.4D
IFPAB_TXC* 7.1G< 7.4D
IFPAB_TXD0 7.1G< 7.3D
IFPAB_TXD0* 7.1G< 7.3D
IFPAB_TXD1 7.1G< 7.3D
IFPAB_TXD1* 7.1G< 7.3D
IFPAB_TXD2 7.1G< 7.3D
IFPAB_TXD2* 7.1G< 7.3D
IFPAB_TXD4 7.1G< 7.3D
IFPAB_TXD4* 7.1G< 7.3D
IFPAB_TXD5 7.1G< 7.3D
IFPAB_TXD5* 7.1G< 7.3D
IFPAB_TXD6 7.1G< 7.3D
IFPAB_TXD6* 7.1G< 7.3D
IFPCD_IOVDD 9.1G< 9.3B
IFPD_AUX 8.1G< 8.4C
IFPD_AUX* 8.1G< 8.4C
IFPD_AUX_BYP 8.1G< 8.3D
IFPD_AUX_BYP* 8.1G< 8.2D
IFPD_AUX_C 8.1G< 8.4G
IFPD_AUX_C* 8.1G< 8.4G
IFPD_AUX_RC 8.1G< 8.3D
IFPD_AUX_RC* 8.1G< 8.2D
IFPD_AUX_SEL 8.1F< 8.3D
IFPD_L0 8.1G< 8.4C
IFPD_L0* 8.1G< 8.4C
IFPD_L0_C 8.1G< 8.4G
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JTAG_TDO 10.1G< 10.2C
JTAG_TMS 10.1G< 10.2C
JTAG_TRST* 10.1G< 10.2C
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PS_3V3_SS 12.1G< 12.3F
PS_5V_ADJ 12.1G< 12.2B
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SNN_A_ID2 5.4F
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SNN_IFPE_RSET 9.4B
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SNN_PE_PRSNT2_C 2.3B
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THERMDC 10.1G< 10.2C
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THERM_P* 11.1G< 11.2C
THERM_P_Q 11.1G< 11.2B
THERM_SHUTDOWN* 11.1G< 11.2A> 13.4A<
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XTAL_OUT 10.1F< 10.5E

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