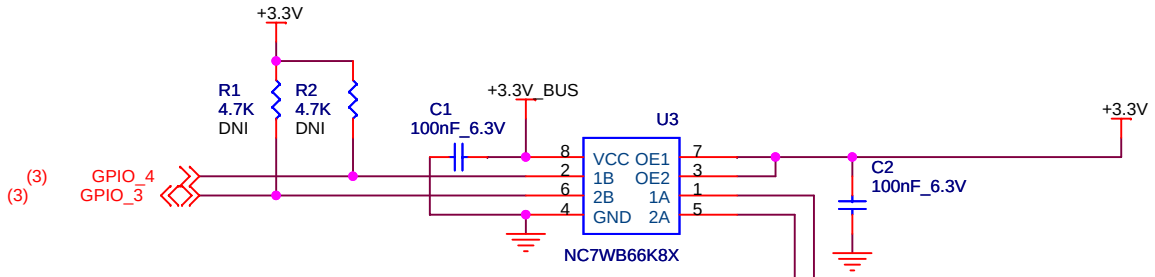
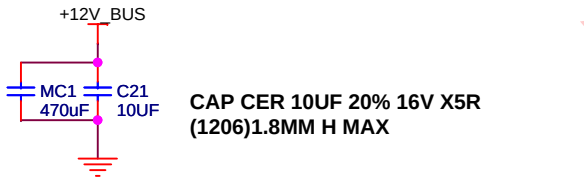
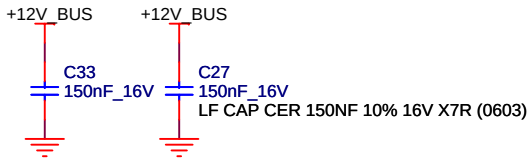
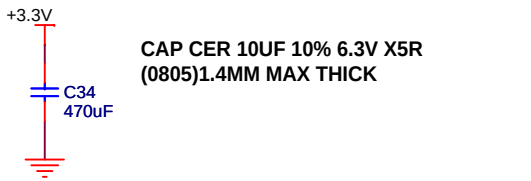
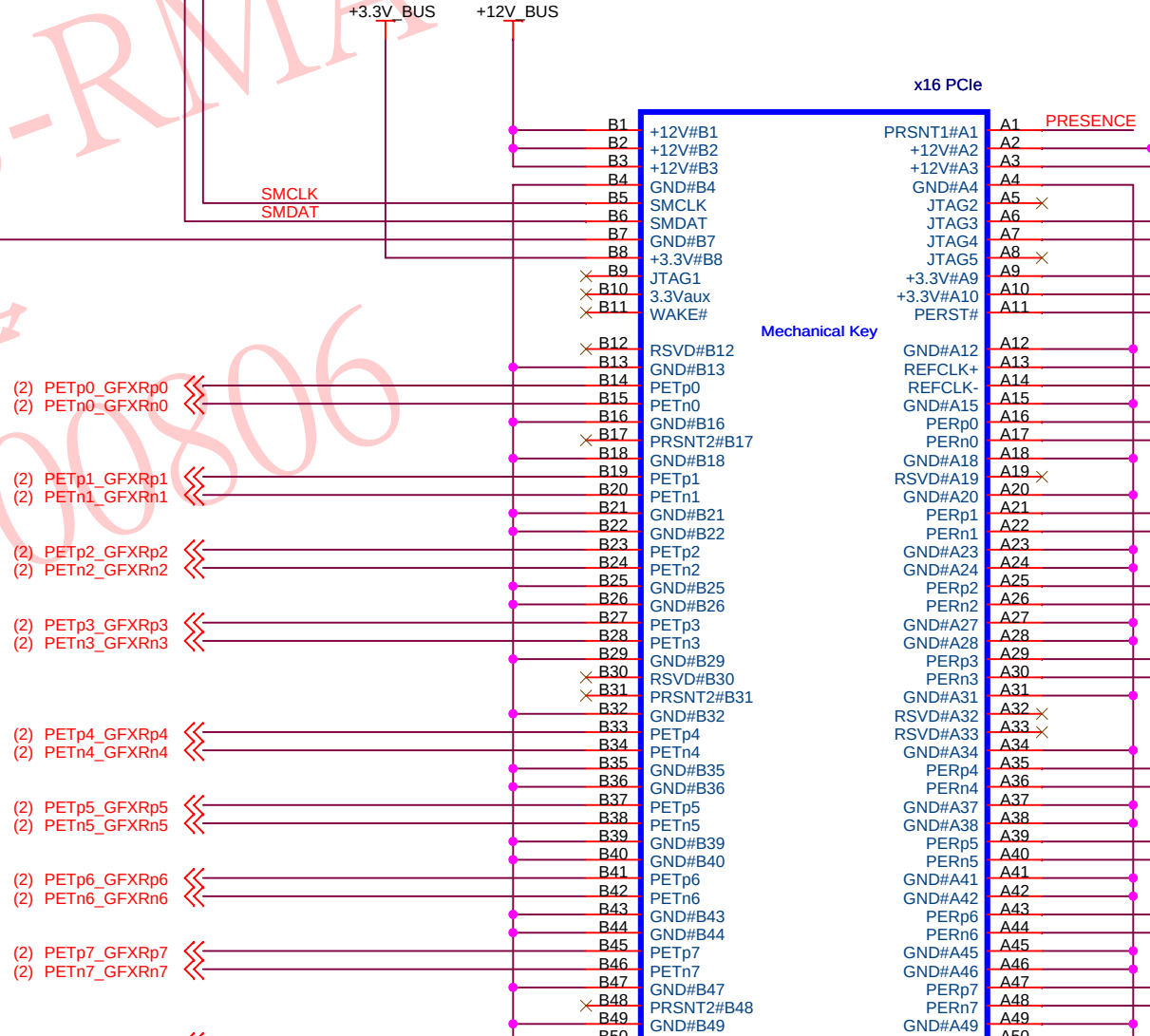
PCI-EXPRESS EDGE CONNE







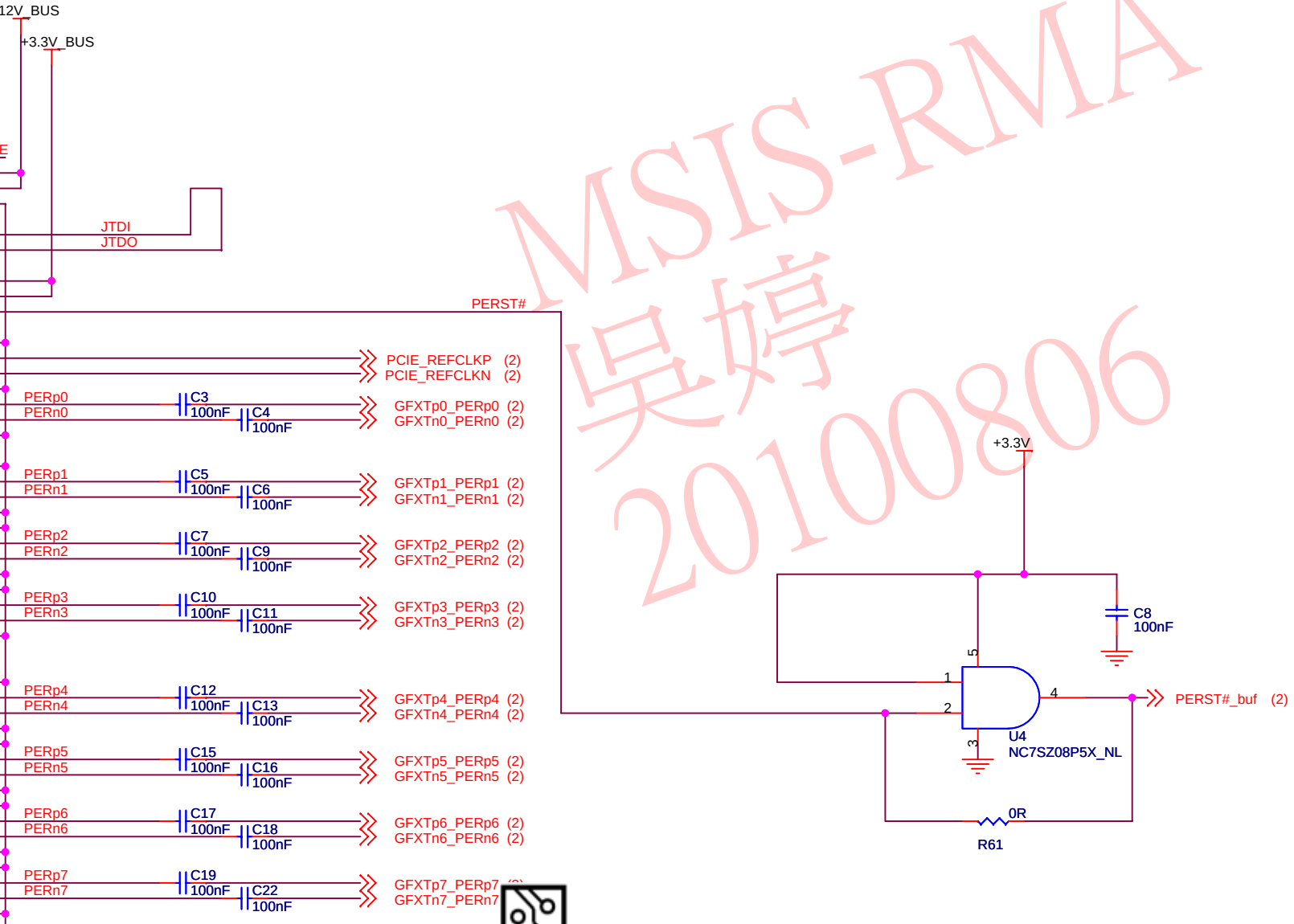


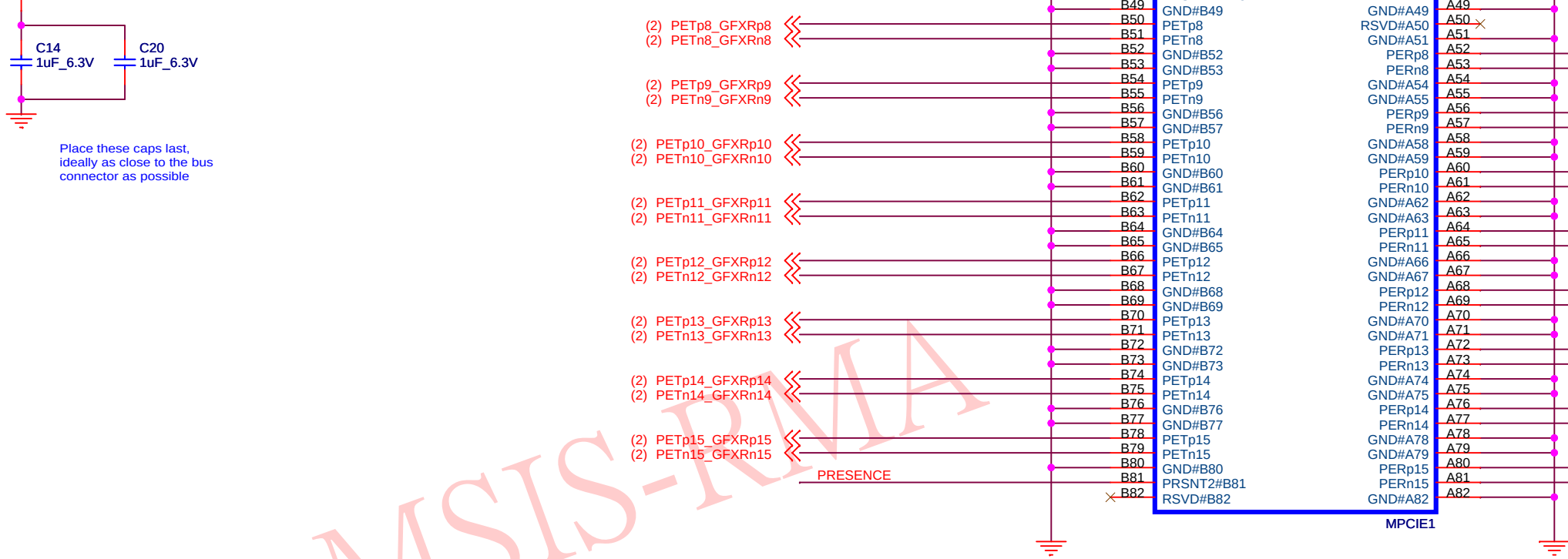


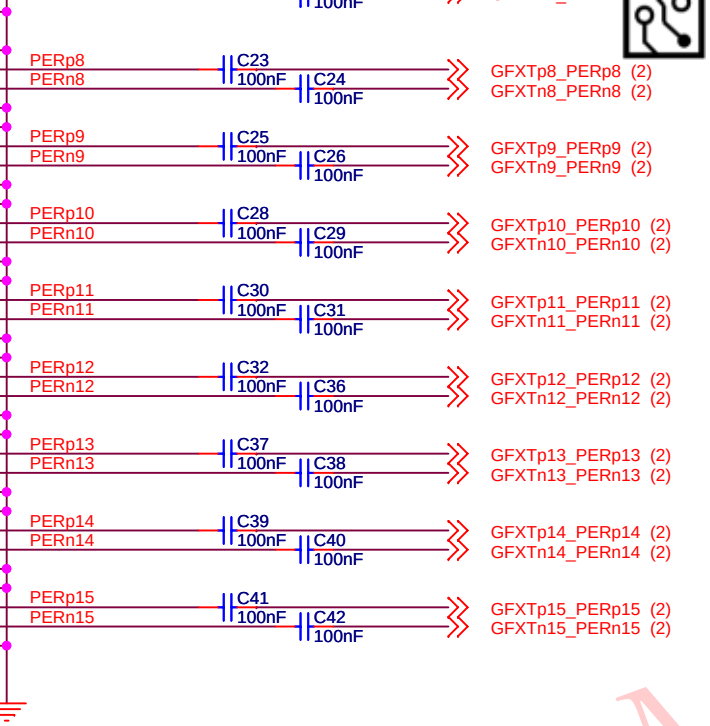
RV710 CUSTOM

VGA(header) + TVO + DVI

IECTOR







SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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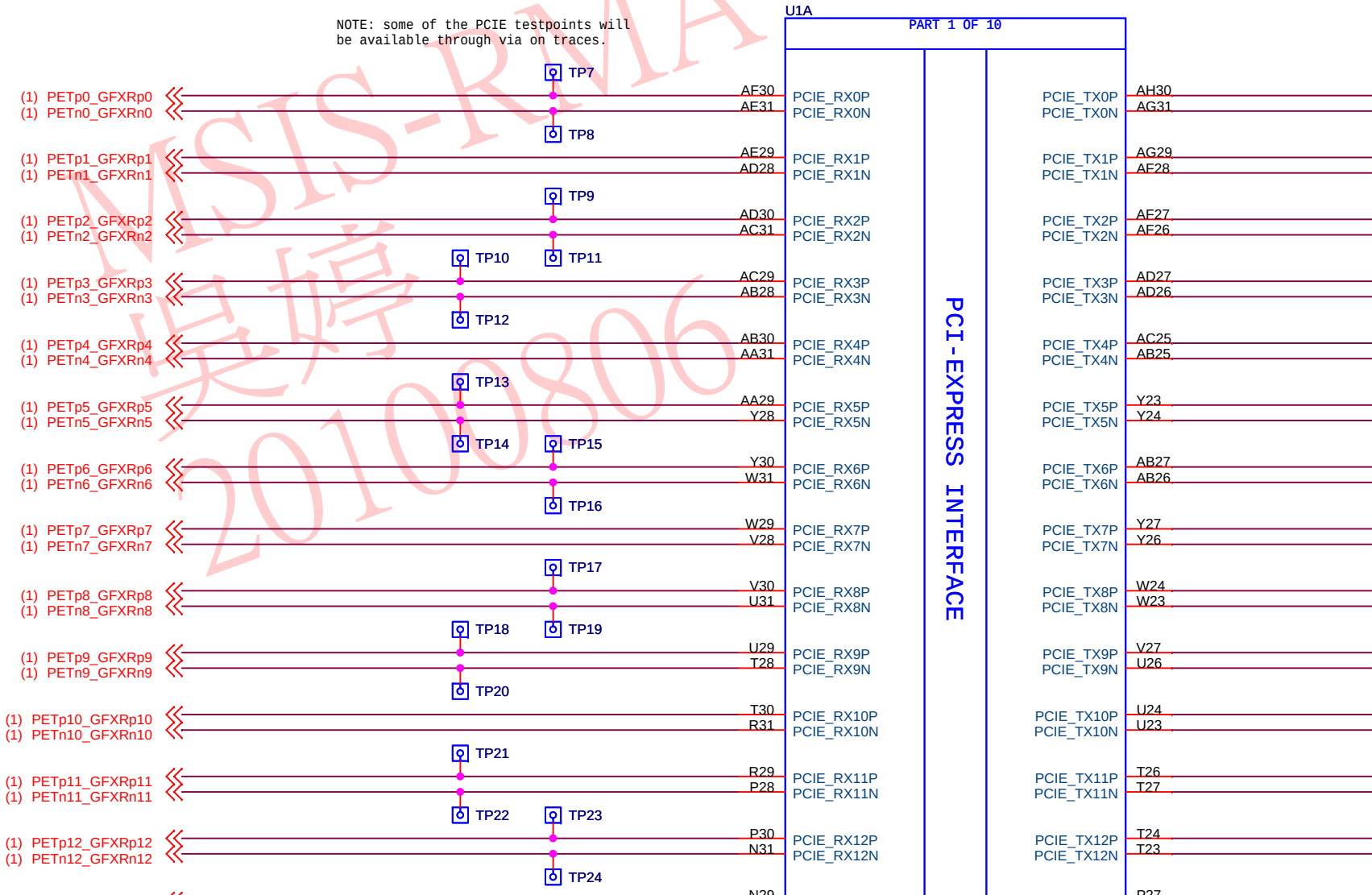
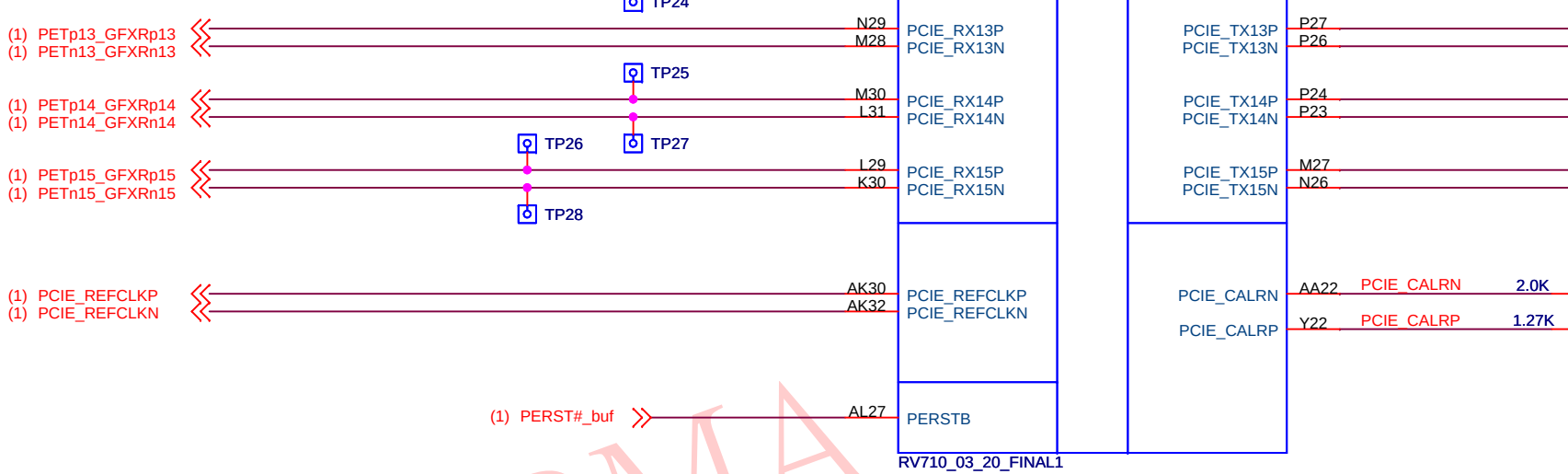
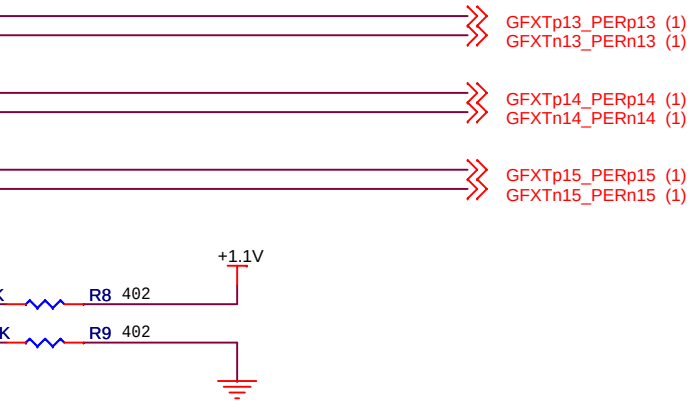
3 2 1







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Title: RH LP RV710 DDR2 VGA (header) TVO DVI

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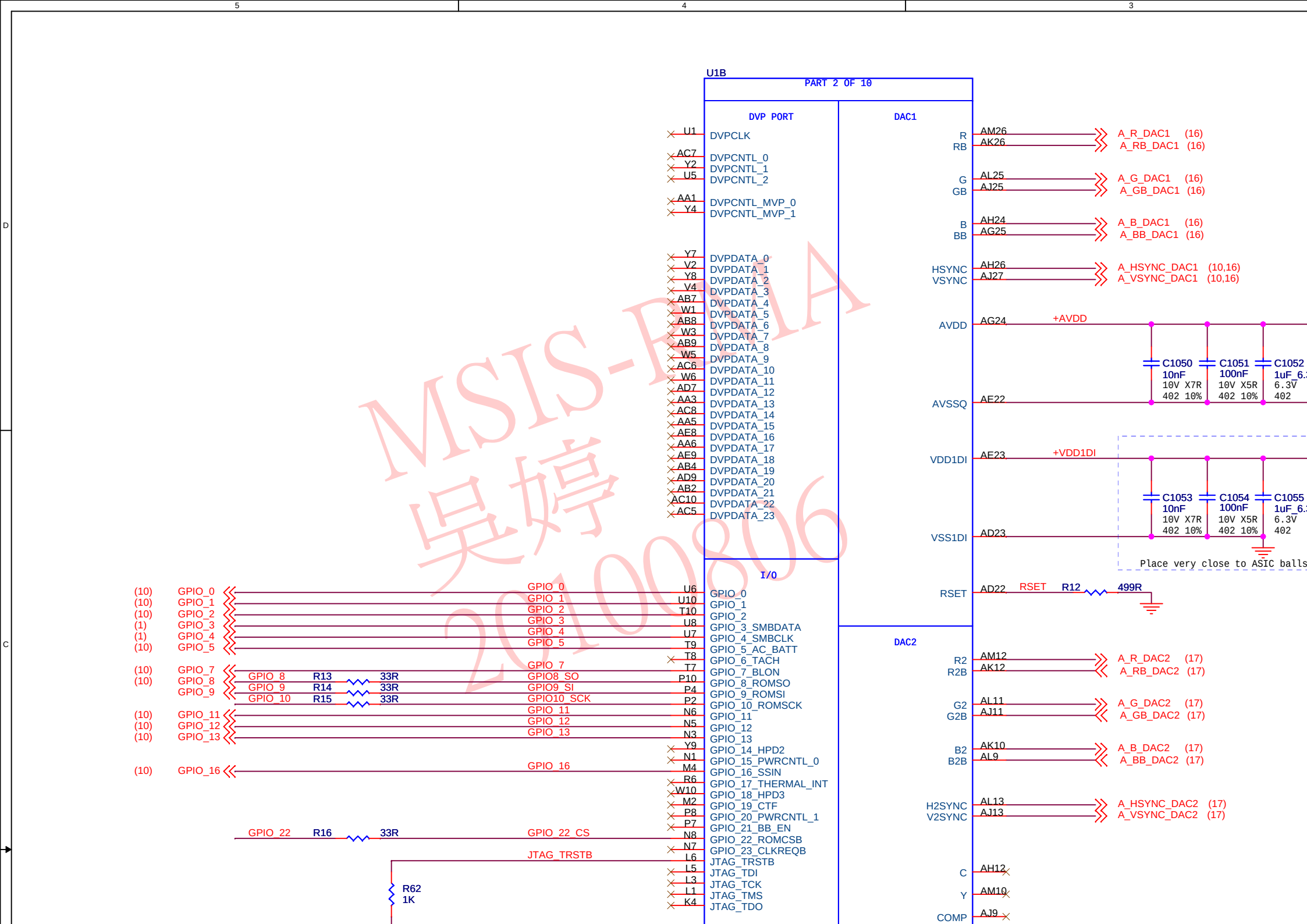
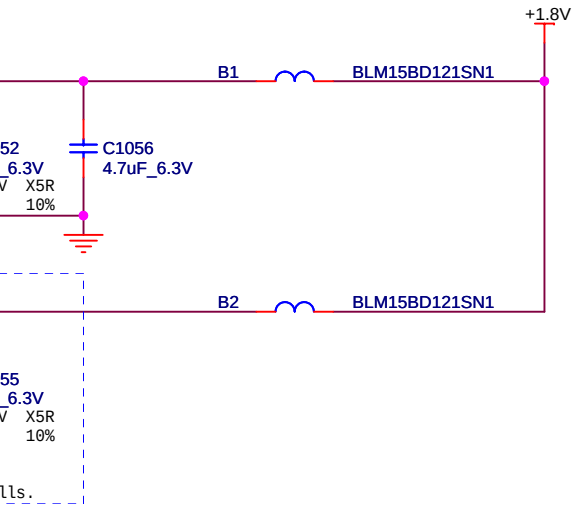
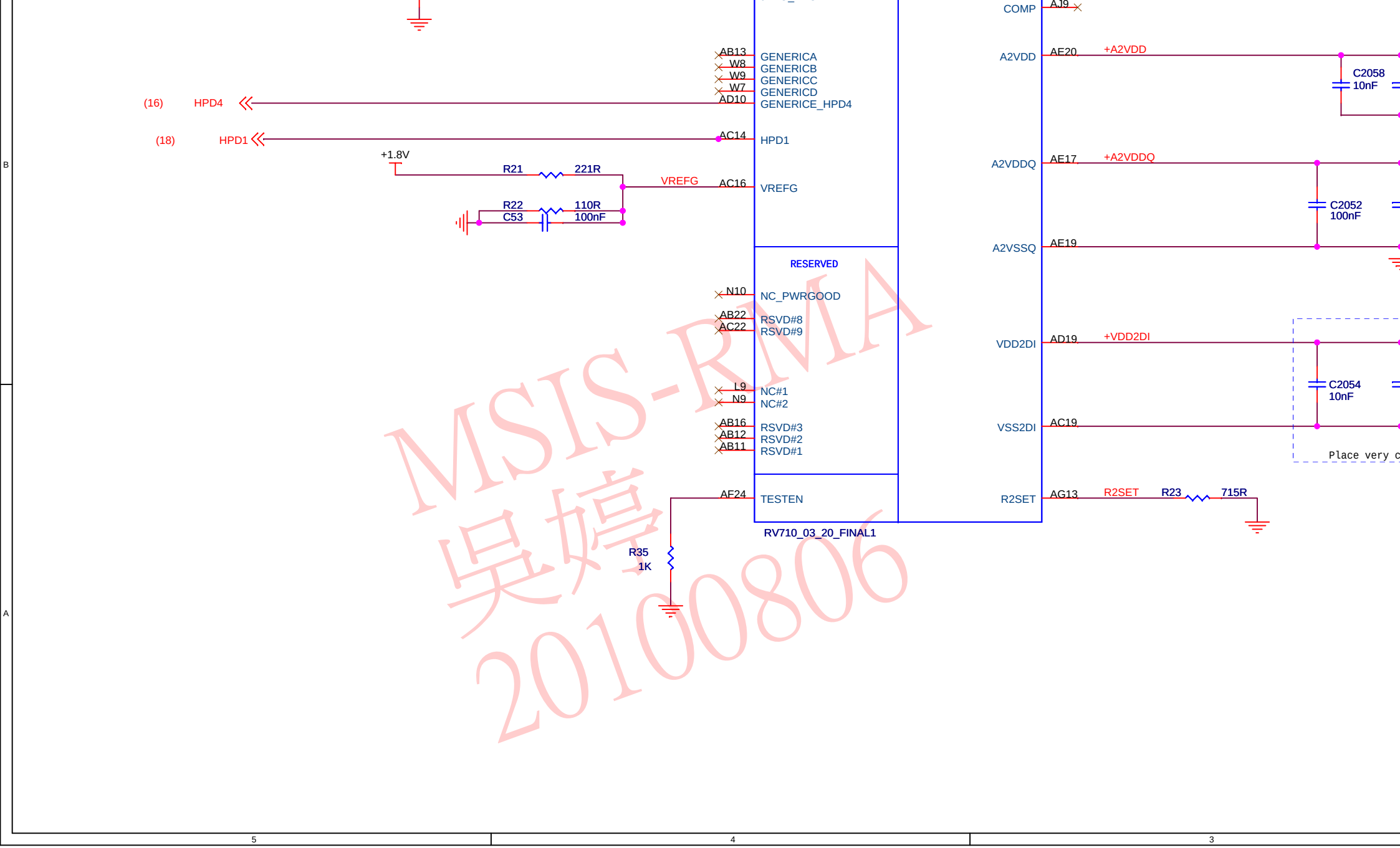
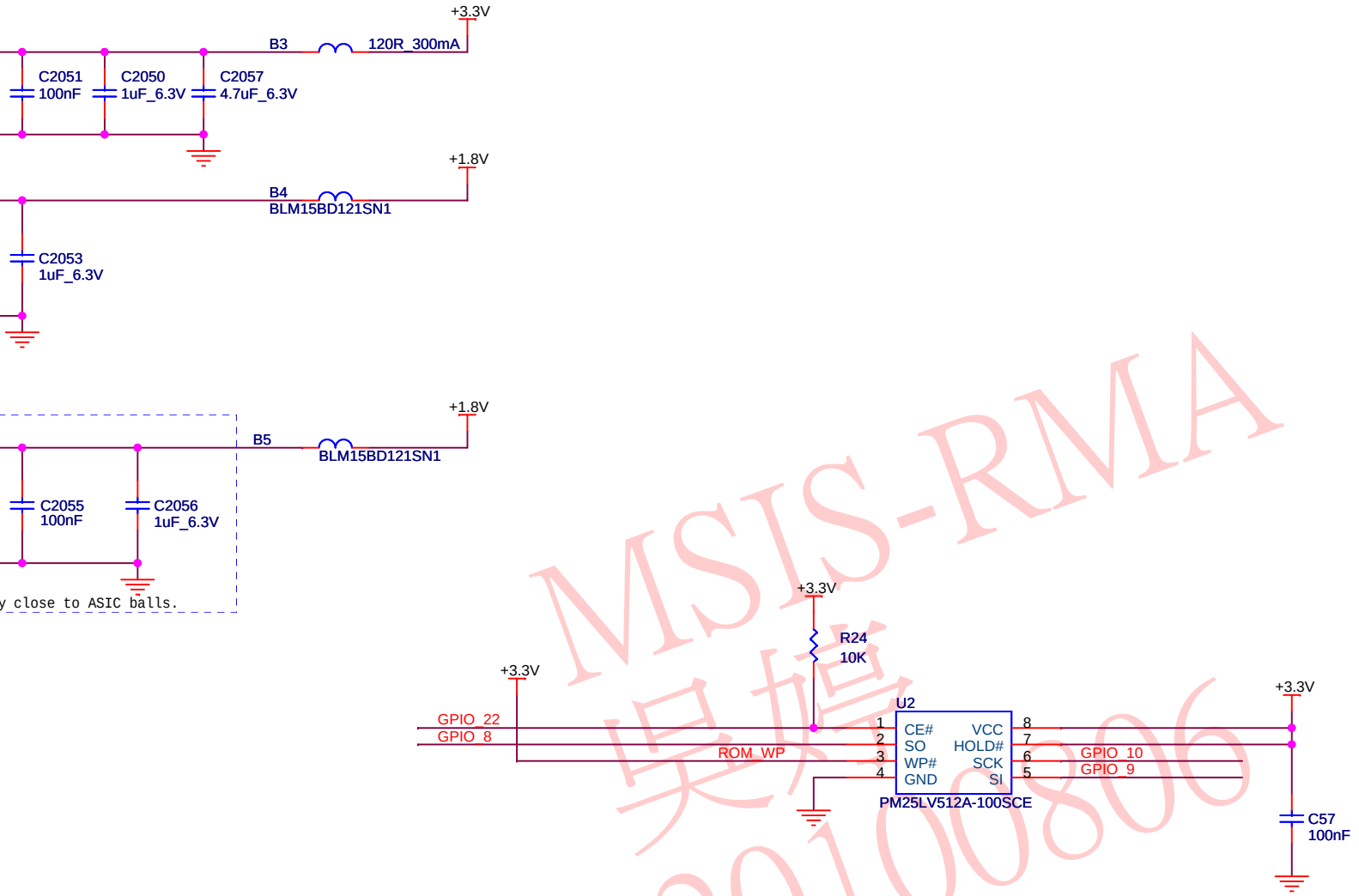





(16) HPD4
(18) HPD1
+1.8V
R21 221R
R22 110R
C53 100nF
VREFG
AB13 GENERICA
W8 GENERICB
W9 GENERICC
W7 GENERICD
AD10 GENERICE_HPD4
AC14 HPD1
AC16 VREFG
RESERVED
N10 NC_PWRGOOD
AB22 RSVD#8
AC22 RSVD#9
L9 NC#1
N9 NC#2
AB16 RSVD#3
AB12 RSVD#2
AB11 RSVD#1
AF24 TESTEN
R35 1K
RV710_03_20_FINAL1
COMP AJ9
A2VDD AE20 +A2VDD
C2058 10nF
A2VDDQ AE17 +A2VDDQ
C2052 100nF
A2VSSQ AE19
VDD2DI AD19 +VDD2DI
C2054 10nF
VSS2DI AC19
Place very c
R2SET AG13 R2SET R23 715R
MSIS-RMA
吳婷
20100806



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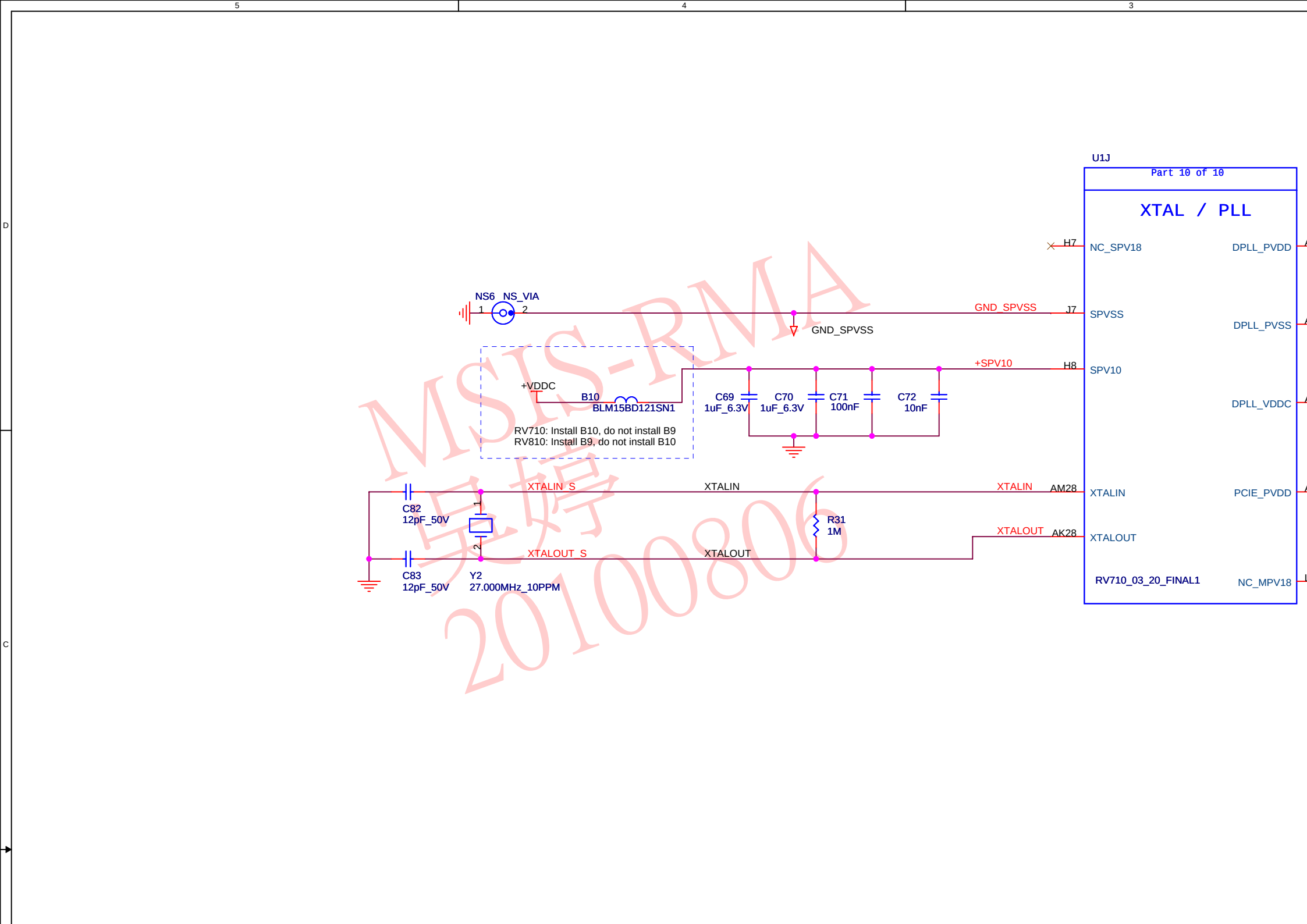
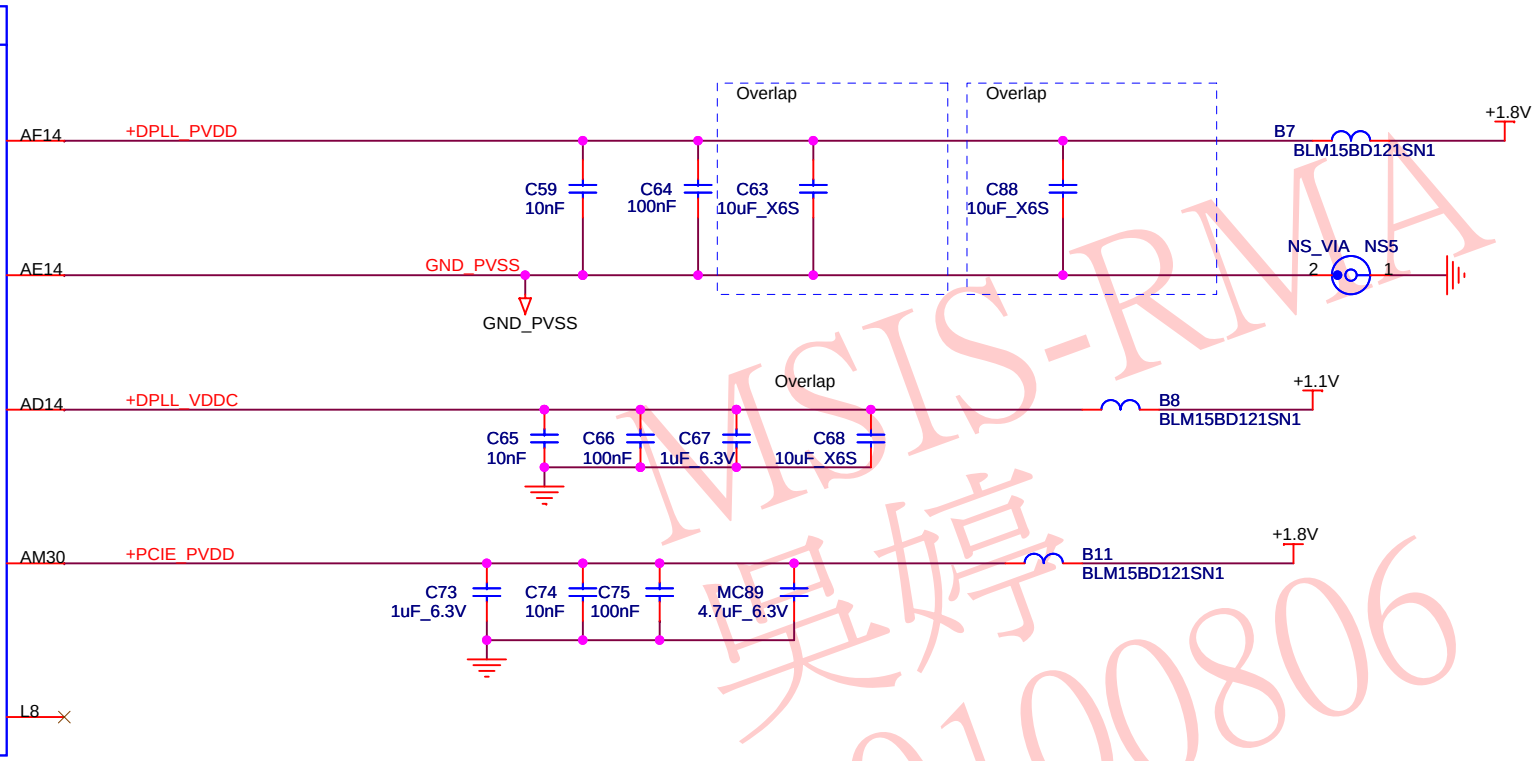
Title RH LP RV710 DDR2 VGA (header) TVO DVI	Doc No. 105-B750XX-00A


U1J
Part 10 of 10
XTAL / PLL
NC_SPV18
H7
DPLL_PVDD
SPVSS
J7
GND_SPVSS
DPLL_PVSS
SPV10
H8
+SPV10
DPLL_VDDC
XTALIN
AM28
PCIE_PVDD
XTALOUT
AK28
RV710_03_20_FINAL1
NC_MPV18
NS6 NS_VIA
+VDDC
B10
BLM15BD121SN1
C69
1uF_6.3V
C70
1uF_6.3V
C71
100nF
C72
10nF
RV710: Install B10, do not install B9
RV810: Install B9, do not install B10
XTALIN_S
XTALOUT_S
C82
12pF_50V
C83
12pF_50V
Y2
27.000MHz_10PPM
R31
1M
MSIS-RMA
20100806

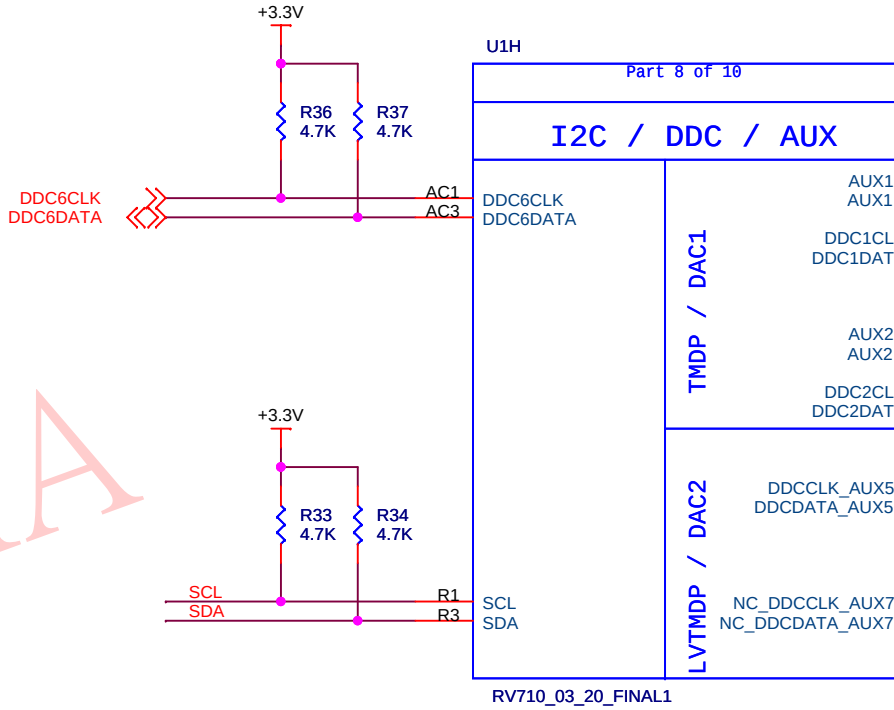


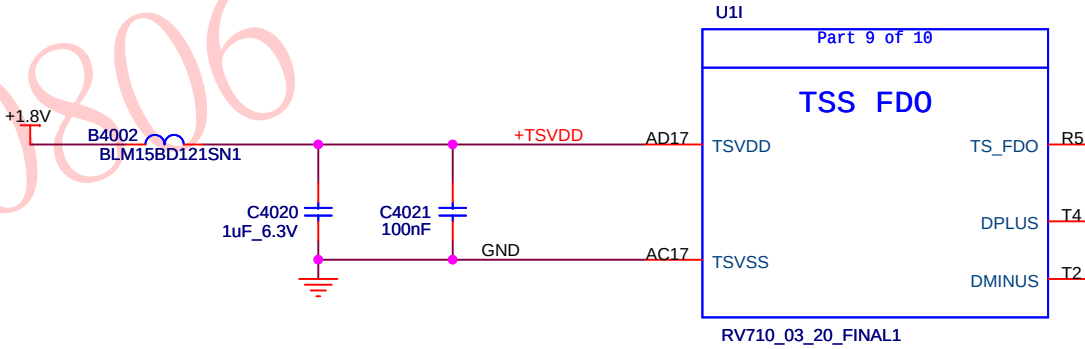
DDC6 BUS:

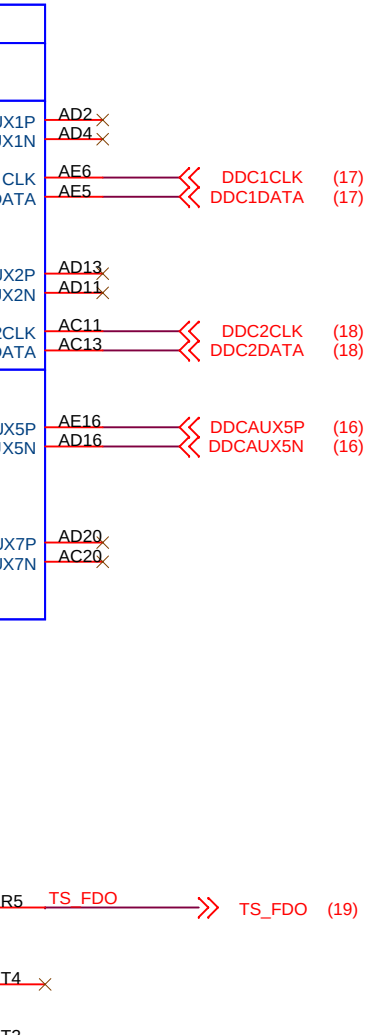
I2C Address	Function	Device
0x90	I2C VDDC Control	DS4402
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A







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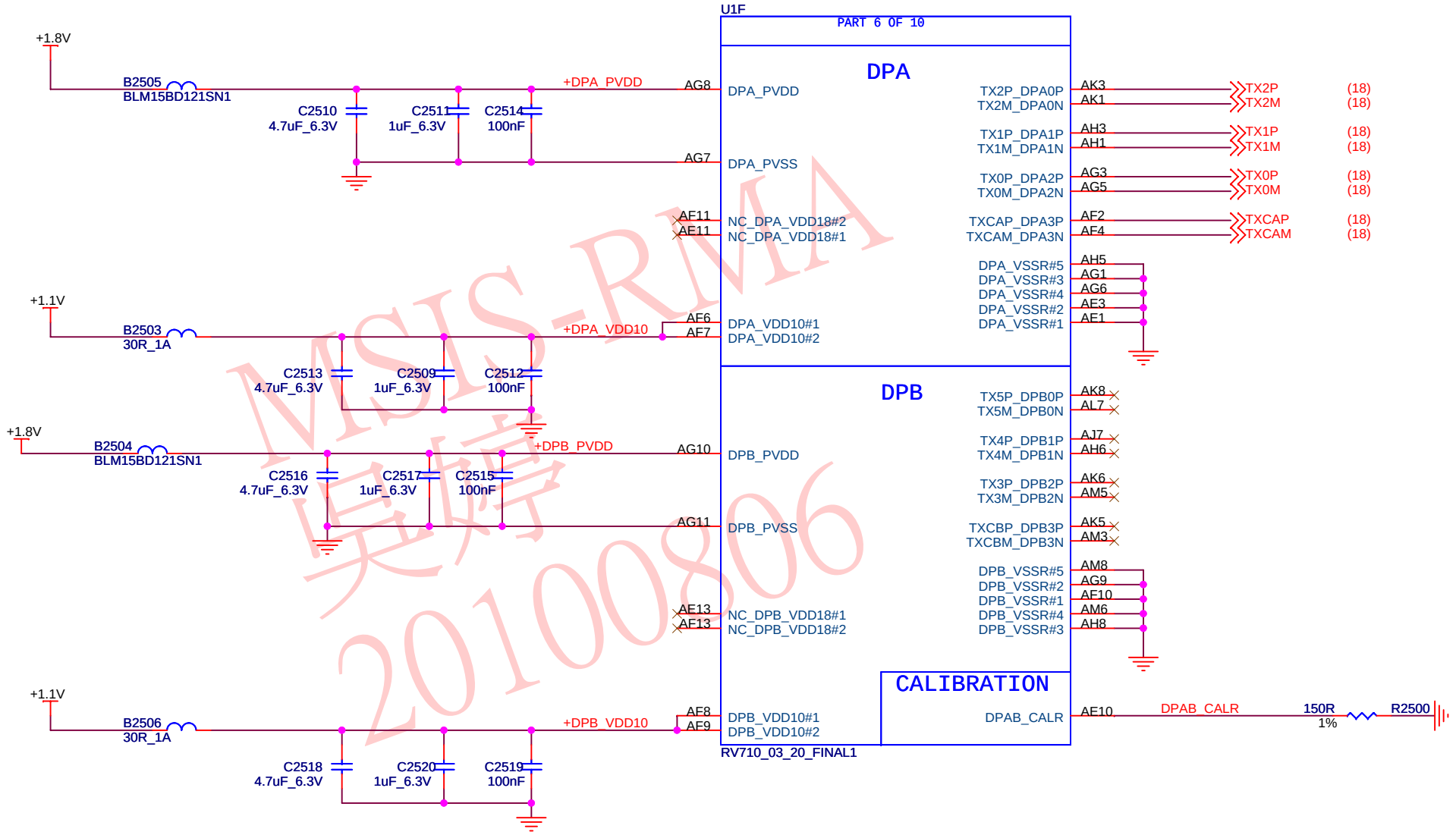
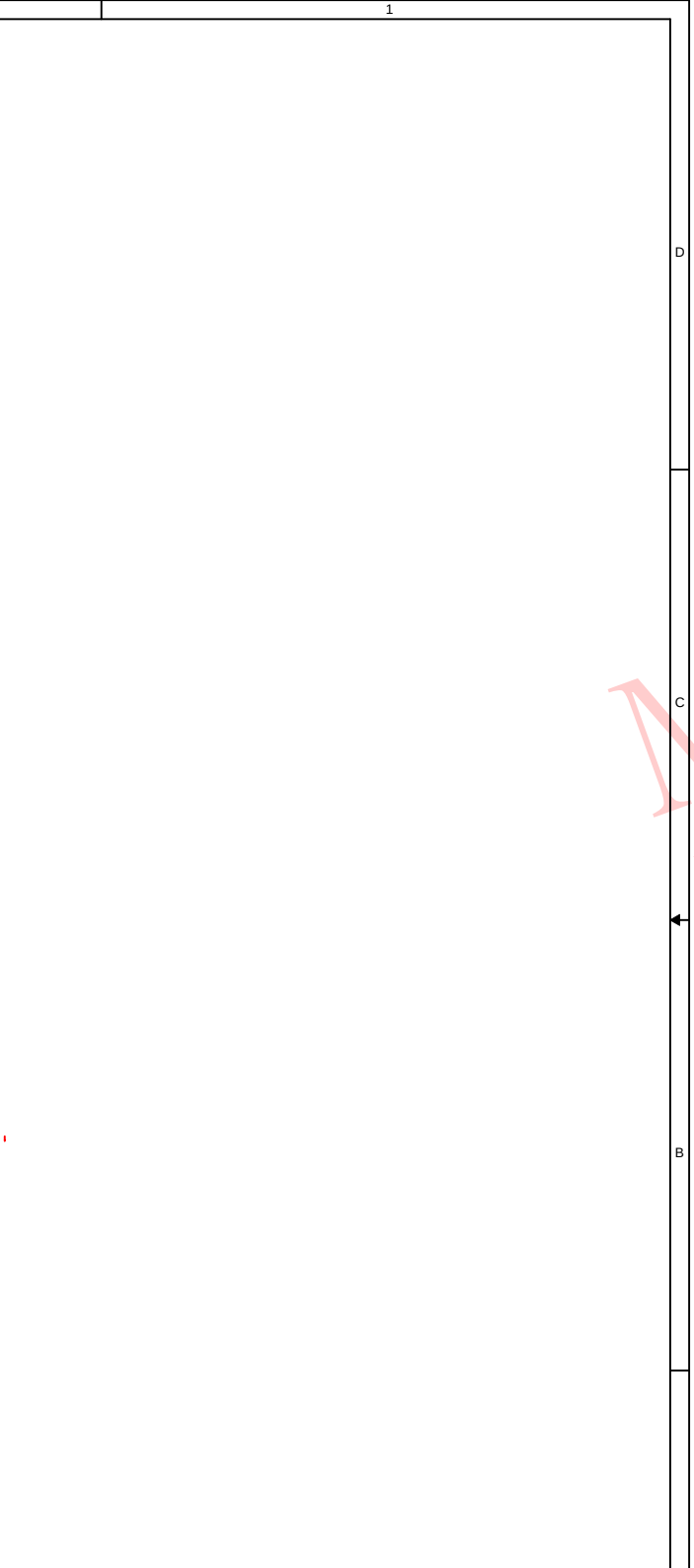
TMDP INTERFACE





Title RH LP RV710 DDR2 VC

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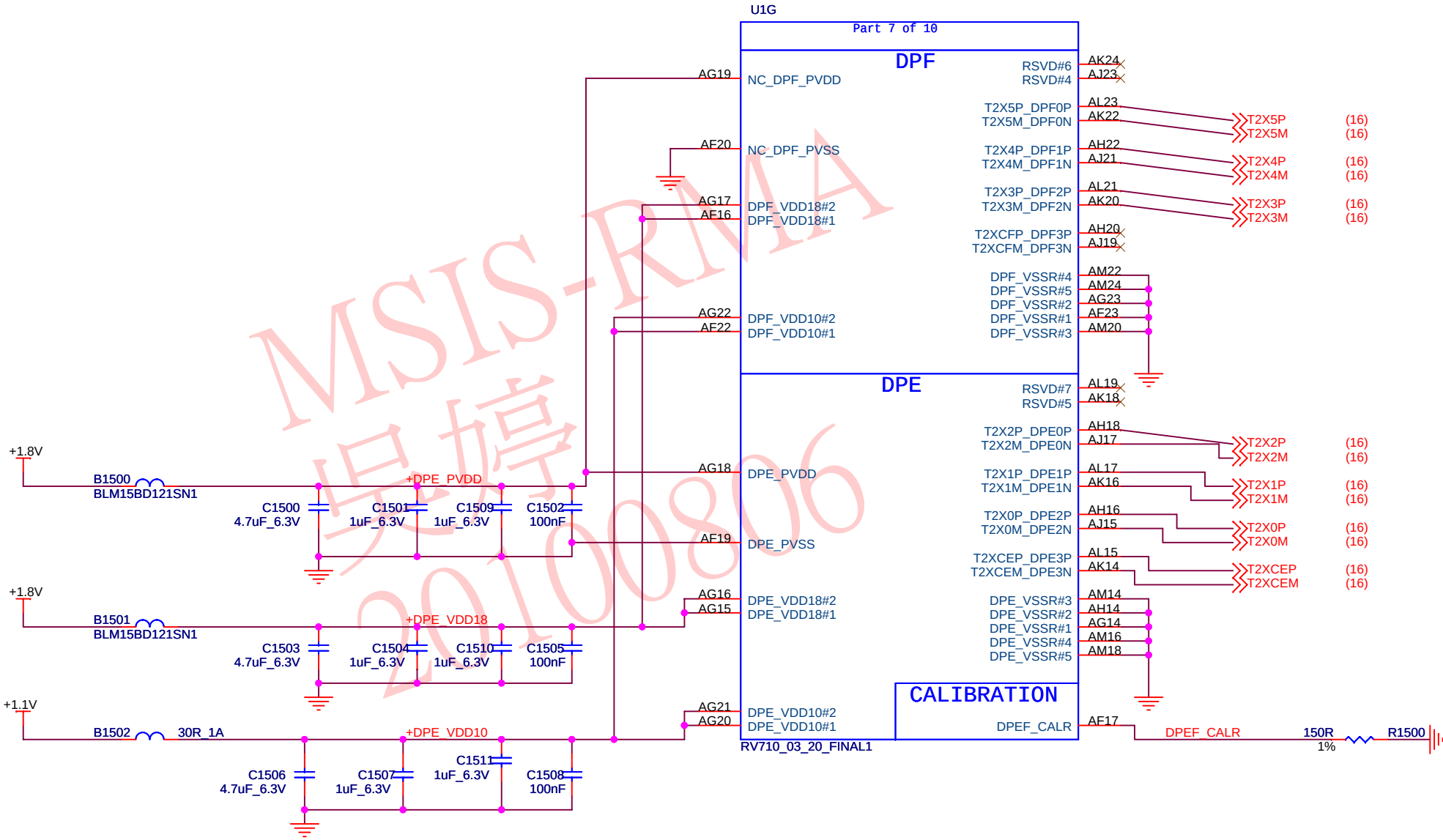
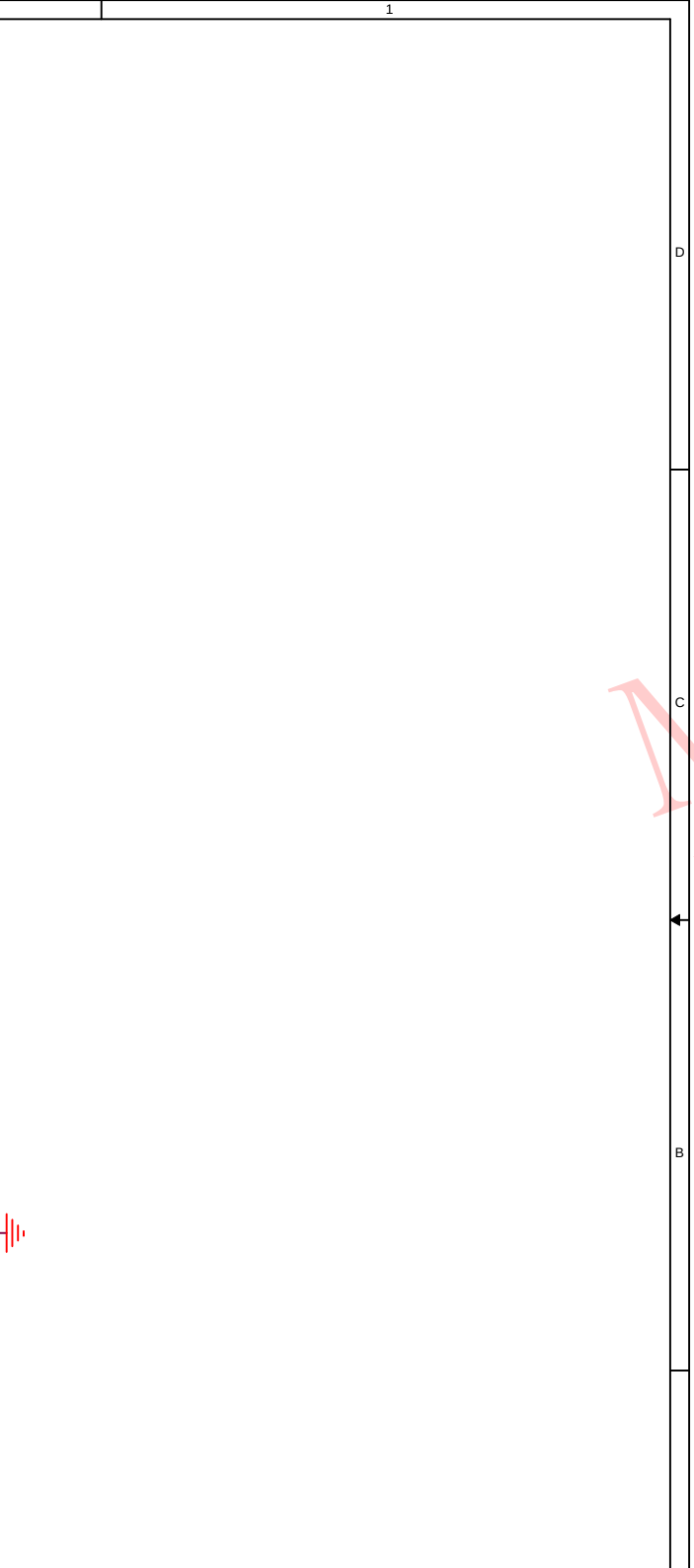
LVTMDP INTERFACE





Title RH LP RV710 DDR2 VC

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License Agreement
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quences resulting

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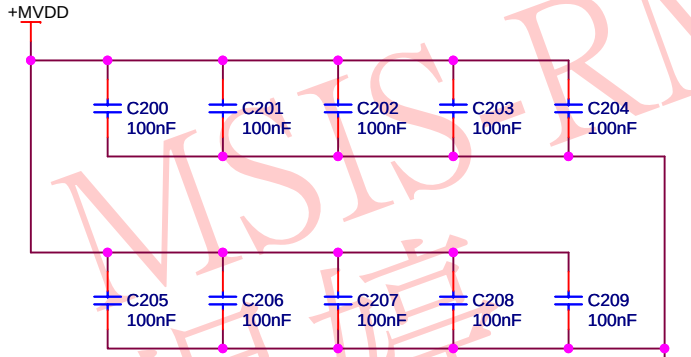
MEI

(15) M_MDA[63..0]

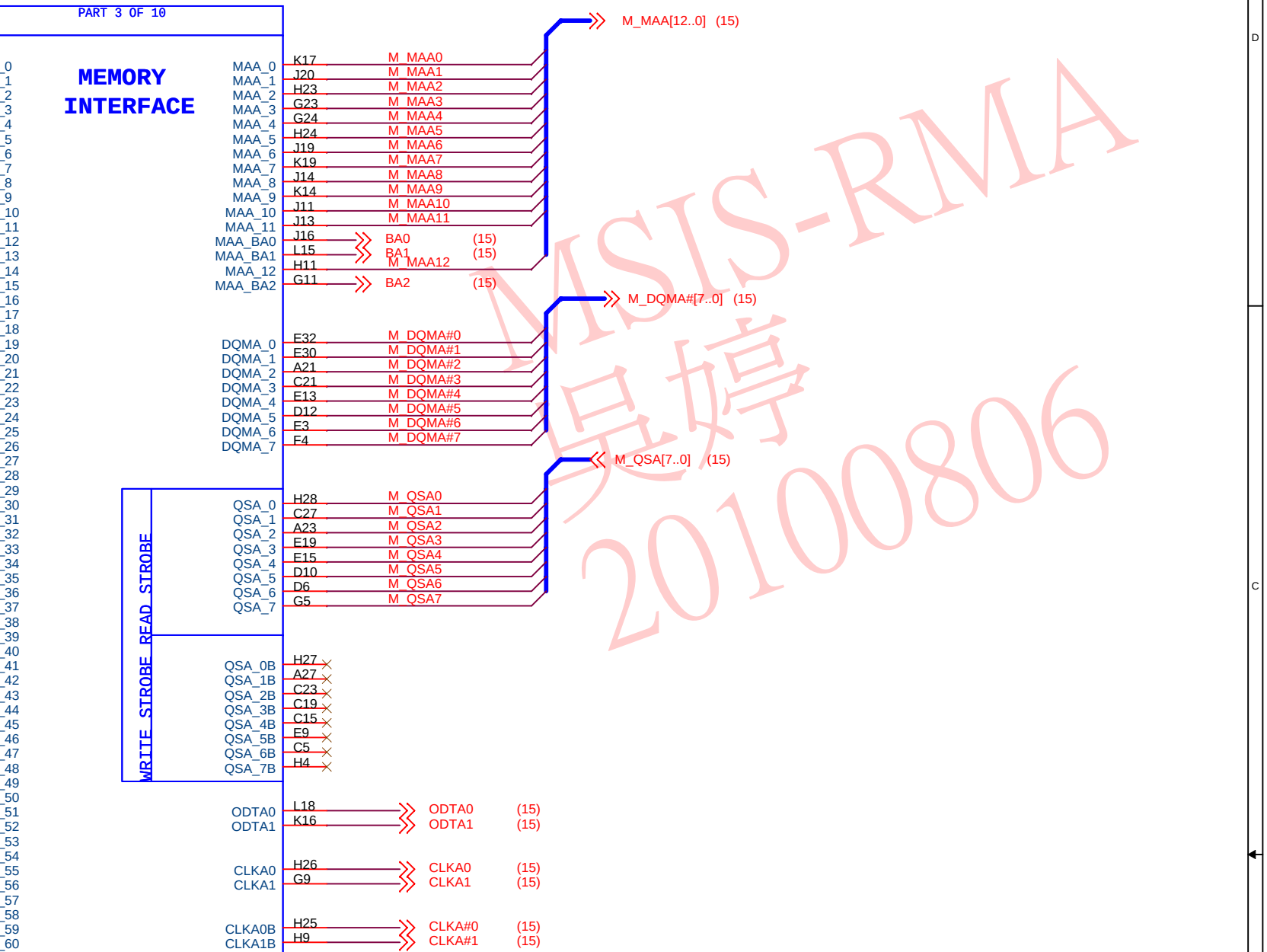
Stitching caps.
Place where memory transitions between L1 and L4.

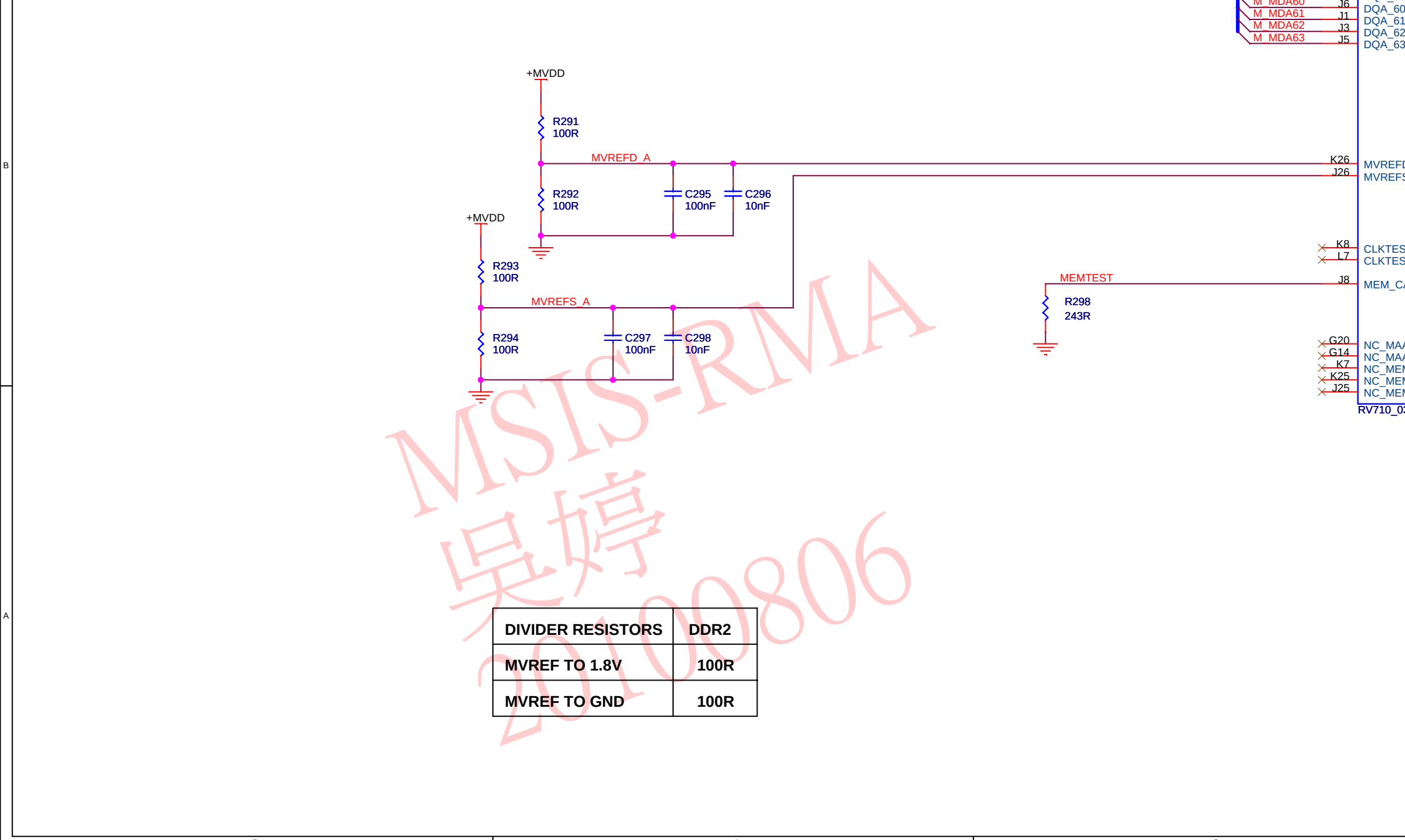


U1C

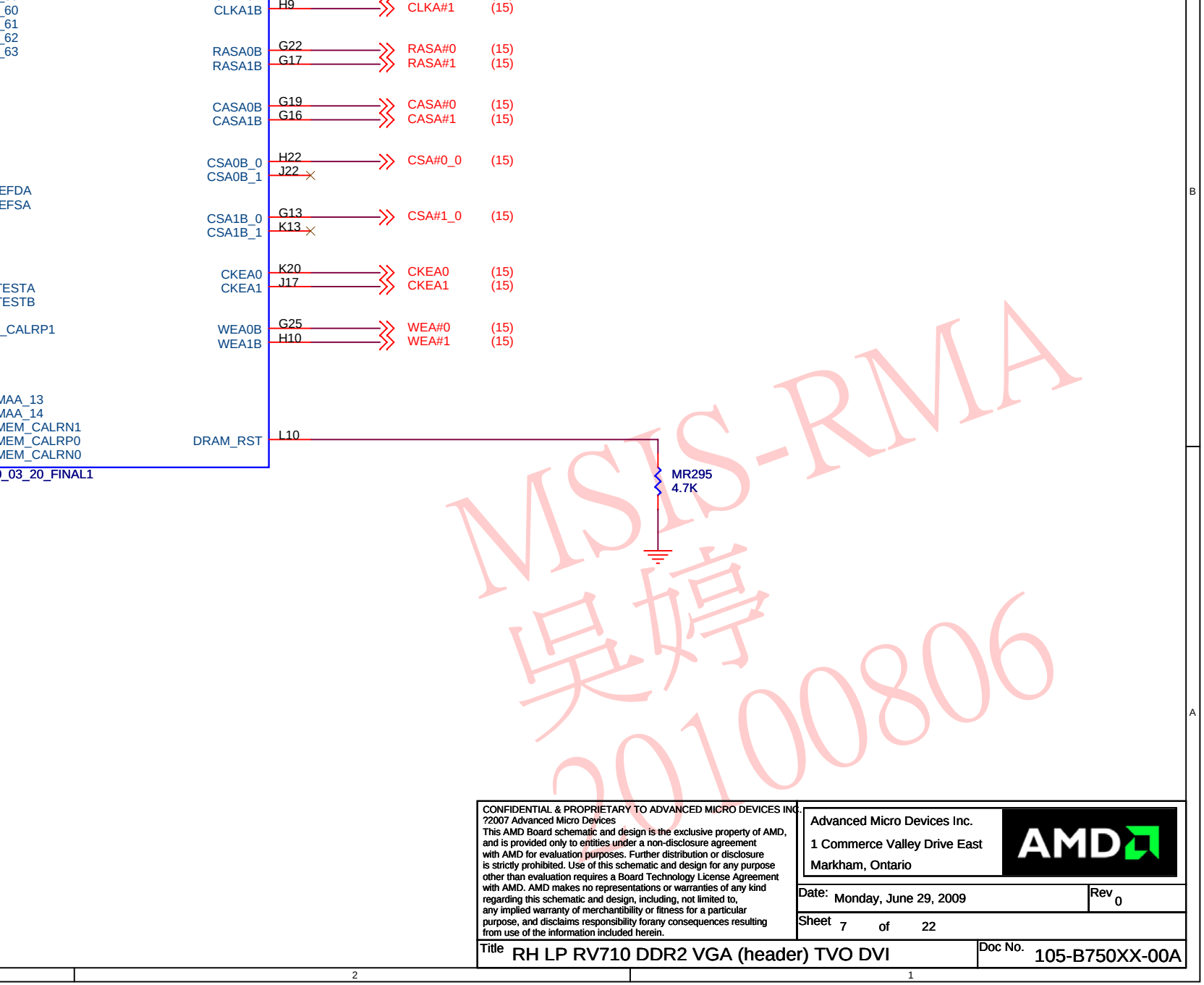
M_MDA0	K27	DQA_0
M_MDA1	J29	DQA_1
M_MDA2	H30	DQA_2
M_MDA3	H32	DQA_3
M_MDA4	G29	DQA_4
M_MDA5	F28	DQA_5
M_MDA6	F32	DQA_6
M_MDA7	F30	DQA_7
M_MDA8	C30	DQA_8
M_MDA9	F27	DQA_9
M_MDA10	A28	DQA_10
M_MDA11	C28	DQA_11
M_MDA12	E27	DQA_12
M_MDA13	G26	DQA_13
M_MDA14	D26	DQA_14
M_MDA15	F25	DQA_15
M_MDA16	A25	DQA_16
M_MDA17	C25	DQA_17
M_MDA18	E25	DQA_18
M_MDA19	D24	DQA_19
M_MDA20	E23	DQA_20
M_MDA21	F23	DQA_21
M_MDA22	D22	DQA_22
M_MDA23	F21	DQA_23
M_MDA24	E21	DQA_24
M_MDA25	D20	DQA_25
M_MDA26	F19	DQA_26
M_MDA27	A19	DQA_27
M_MDA28	D18	DQA_28
M_MDA29	F17	DQA_29
M_MDA30	A17	DQA_30
M_MDA31	C17	DQA_31
M_MDA32	E17	DQA_32
M_MDA33	D16	DQA_33
M_MDA34	F15	DQA_34
M_MDA35	A15	DQA_35
M_MDA36	D14	DQA_36
M_MDA37	F13	DQA_37
M_MDA38	A13	DQA_38
M_MDA39	C13	DQA_39
M_MDA40	E11	DQA_40
M_MDA41	A11	DQA_41
M_MDA42	C11	DQA_42
M_MDA43	F11	DQA_43
M_MDA44	A9	DQA_44
M_MDA45	C9	DQA_45
M_MDA46	F9	DQA_46
M_MDA47	D8	DQA_47
M_MDA48	E7	DQA_48
M_MDA49	A7	DQA_49
M_MDA50	C7	DQA_50
M_MDA51	E7	DQA_51
M_MDA52	A5	DQA_52
M_MDA53	E5	DQA_53
M_MDA54	C3	DQA_54
M_MDA55	E1	DQA_55
M_MDA56	G7	DQA_56
M_MDA57	G6	DQA_57
M_MDA58	G1	DQA_58
M_MDA59	G3	DQA_59
M_MDA60	J6	DQA_60
M_MDA61	J1	

EMORY INTERFACE





DIVIDER RESISTORS	DDR2
MVREF TO 1.8V	100R
MVREF TO GND	100R



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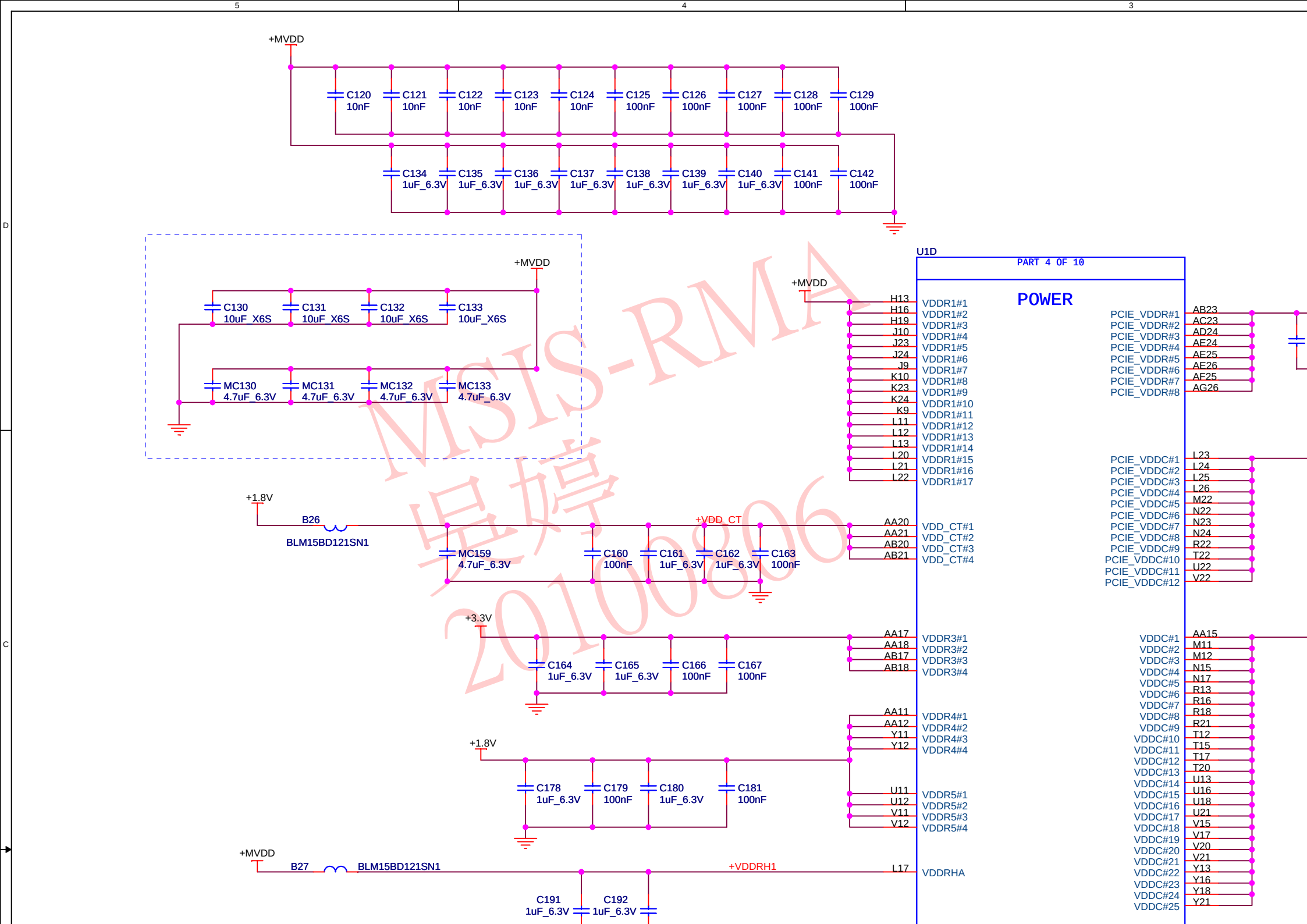

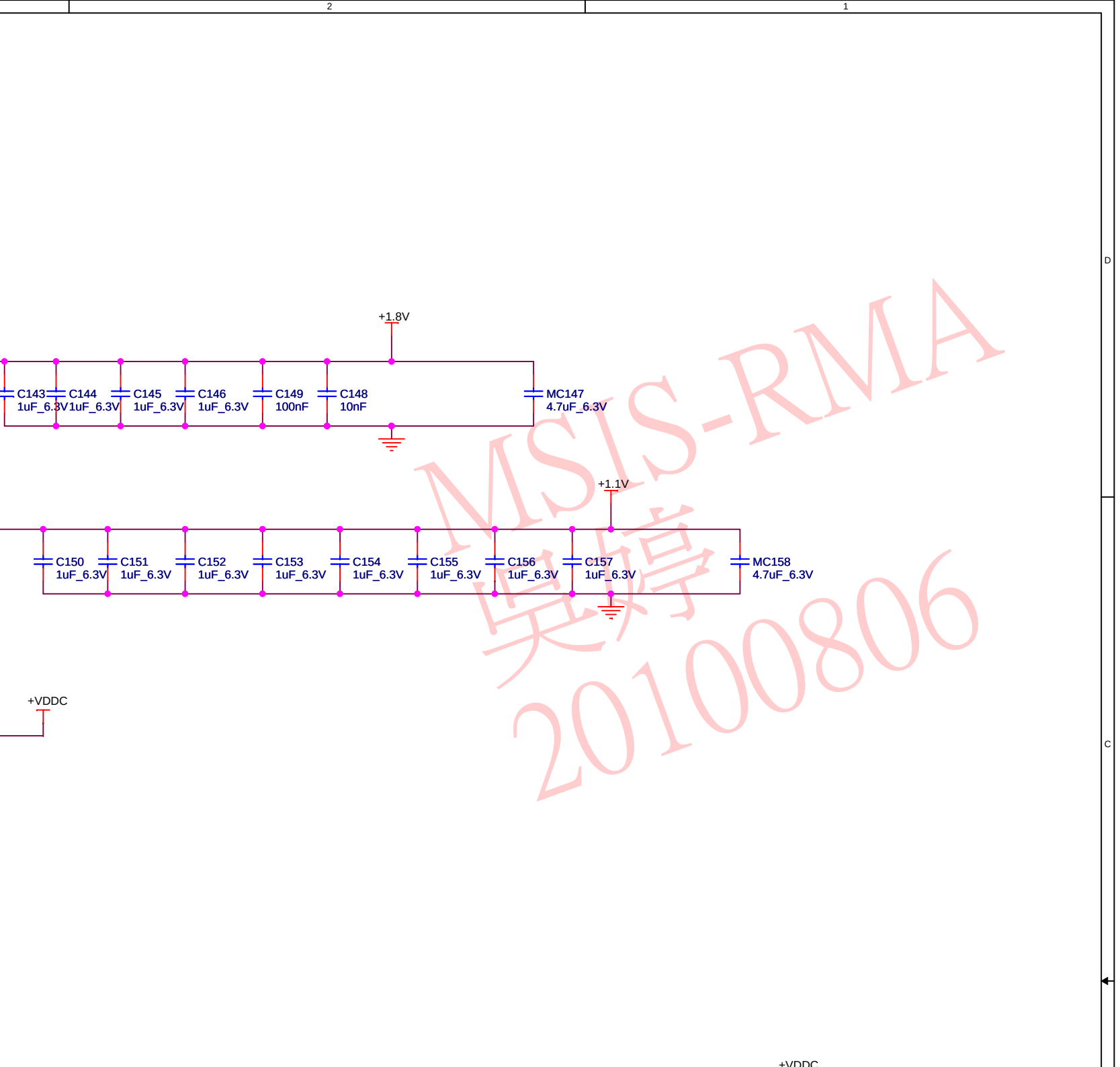

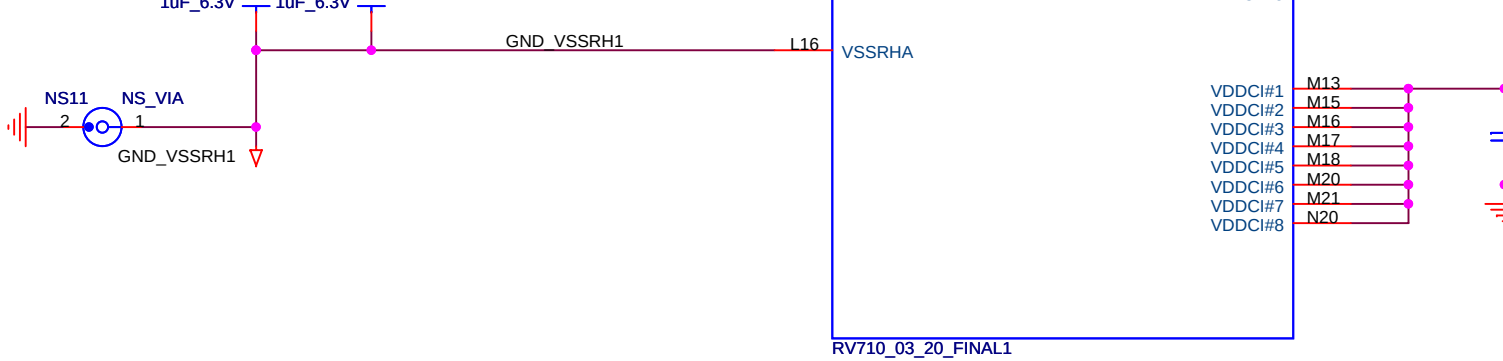

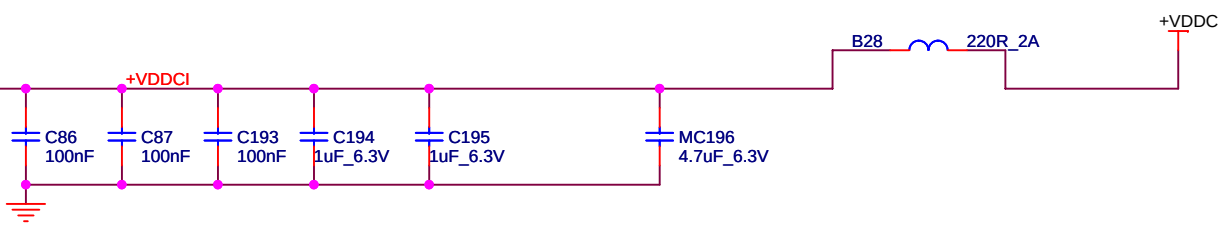

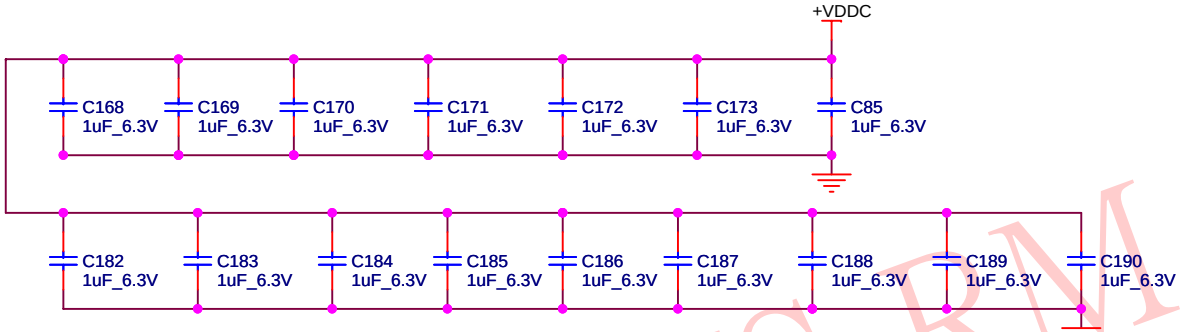

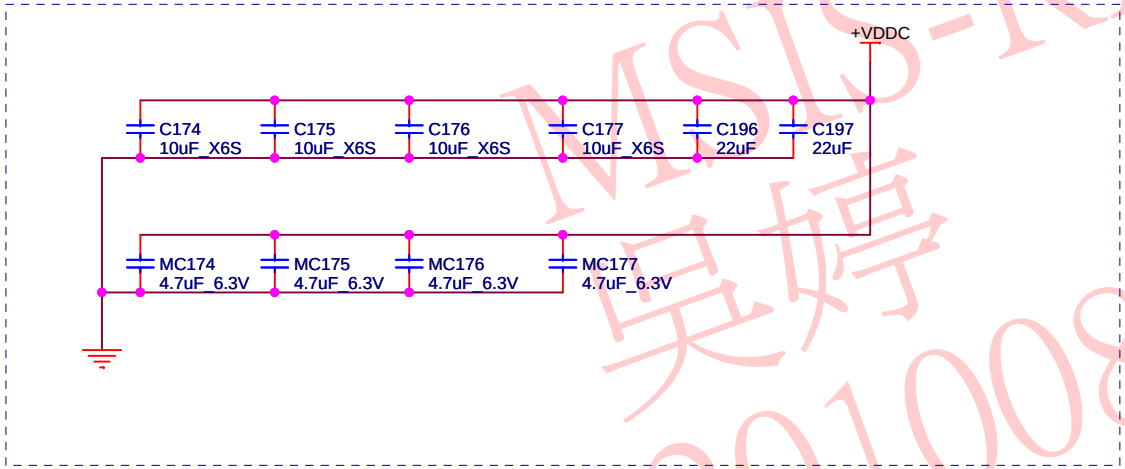

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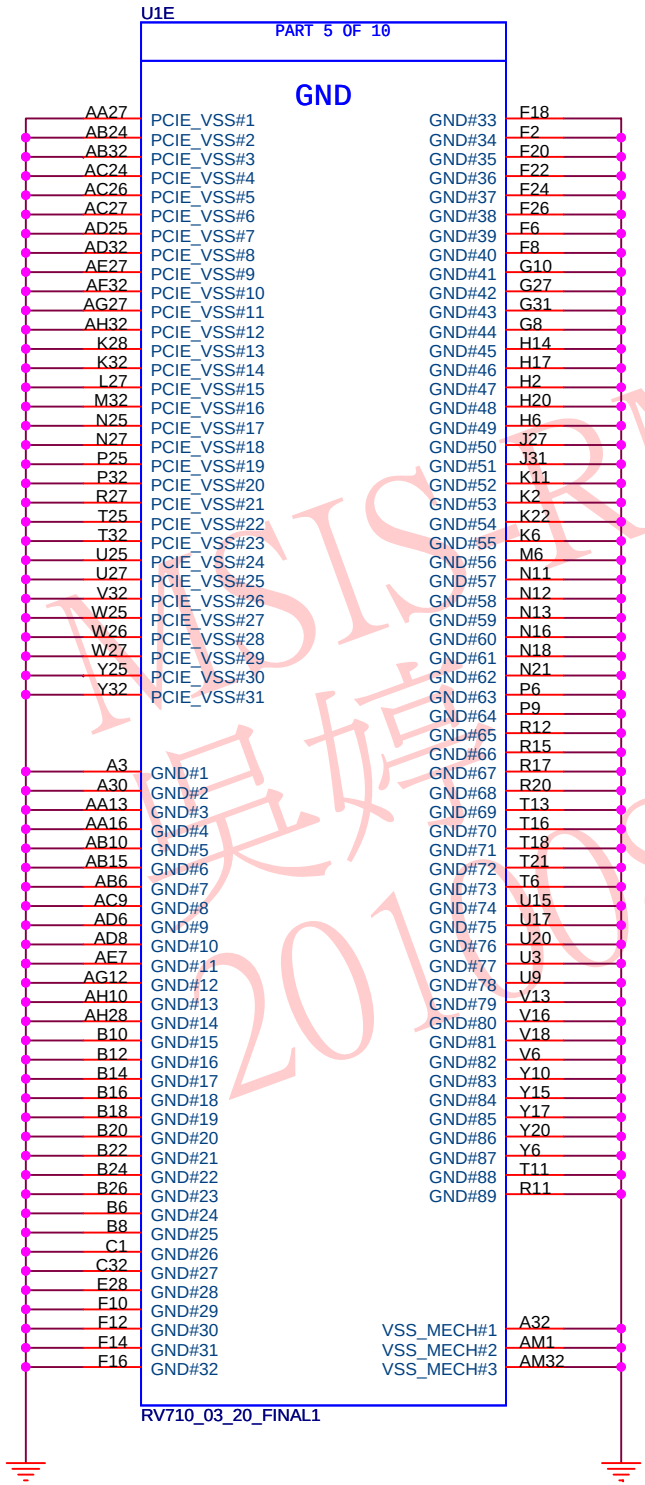
U1E
PART 5 OF 10
GND
PCIE_VSS#1
PCIE_VSS#2
PCIE_VSS#3
PCIE_VSS#4
PCIE_VSS#5
PCIE_VSS#6
PCIE_VSS#7
PCIE_VSS#8
PCIE_VSS#9
PCIE_VSS#10
PCIE_VSS#11
PCIE_VSS#12
PCIE_VSS#13
PCIE_VSS#14
PCIE_VSS#15
PCIE_VSS#16
PCIE_VSS#17
PCIE_VSS#18
PCIE_VSS#19
PCIE_VSS#20
PCIE_VSS#21
PCIE_VSS#22
PCIE_VSS#23
PCIE_VSS#24
PCIE_VSS#25
PCIE_VSS#26
PCIE_VSS#27
PCIE_VSS#28
PCIE_VSS#29
PCIE_VSS#30
PCIE_VSS#31
AA27
AB24
AB32
AC24
AC26
AC27
AD25
AD32
AE27
AE32
AG27
AH32
K28
K32
L27
M32
N25
N27
P25
P32
R27
T25
T32
U25
U27
V32
W25
W26
W27
Y25
Y32
GND#1
GND#2
GND#3
GND#4
GND#5
GND#6
GND#7
GND#8
GND#9
GND#10
GND#11
GND#12
GND#13
GND#14
GND#15
GND#16
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GND#27
GND#28
GND#29
GND#30
GND#31
GND#32
A3
A30
AA13
AA16
AB10
AB15
AB6
AC9
AD6
AD8
AE7
AG12
AH10
AH28
B10
B12
B14
B16
B18
B20
B22
B24
B26
B6
B8
C1
C32
E28
E10
F12
F14
F16
GND#33
GND#34
GND#35
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GND#47
GND#48
GND#49
GND#50
GND#51
GND#52
GND#53
GND#54
GND#55
GND#56
GND#57
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GND#70
GND#71
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GND#73
GND#74
GND#75
GND#76
GND#77
GND#78
GND#79
GND#80
GND#81
GND#82
GND#83
GND#84
GND#85
GND#86
GND#87
GND#88
GND#89
F18
F2
F20
F22
F24
F26
F6
F8
G10
G27
G31
G8
H14
H17
H2
H20
H6
J27
J31
K11
K2
K22
K6
M6
N11
N12
N13
N16
N18
N21
P6
P9
R12
R15
R17
R20
T13
T16
T18
T21
T6
U15
U17
U20
U3
U9
V13
V16
V18
V6
Y10
Y15
Y17
Y20
Y6
T11
R11
VSS_MECH#1
VSS_MECH#2
VSS_MECH#3
A32
AM1
AM32
RV710_03_20_FINAL1

Title RH LP RV710 DDR2 VC

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PIN BASED STRAPS

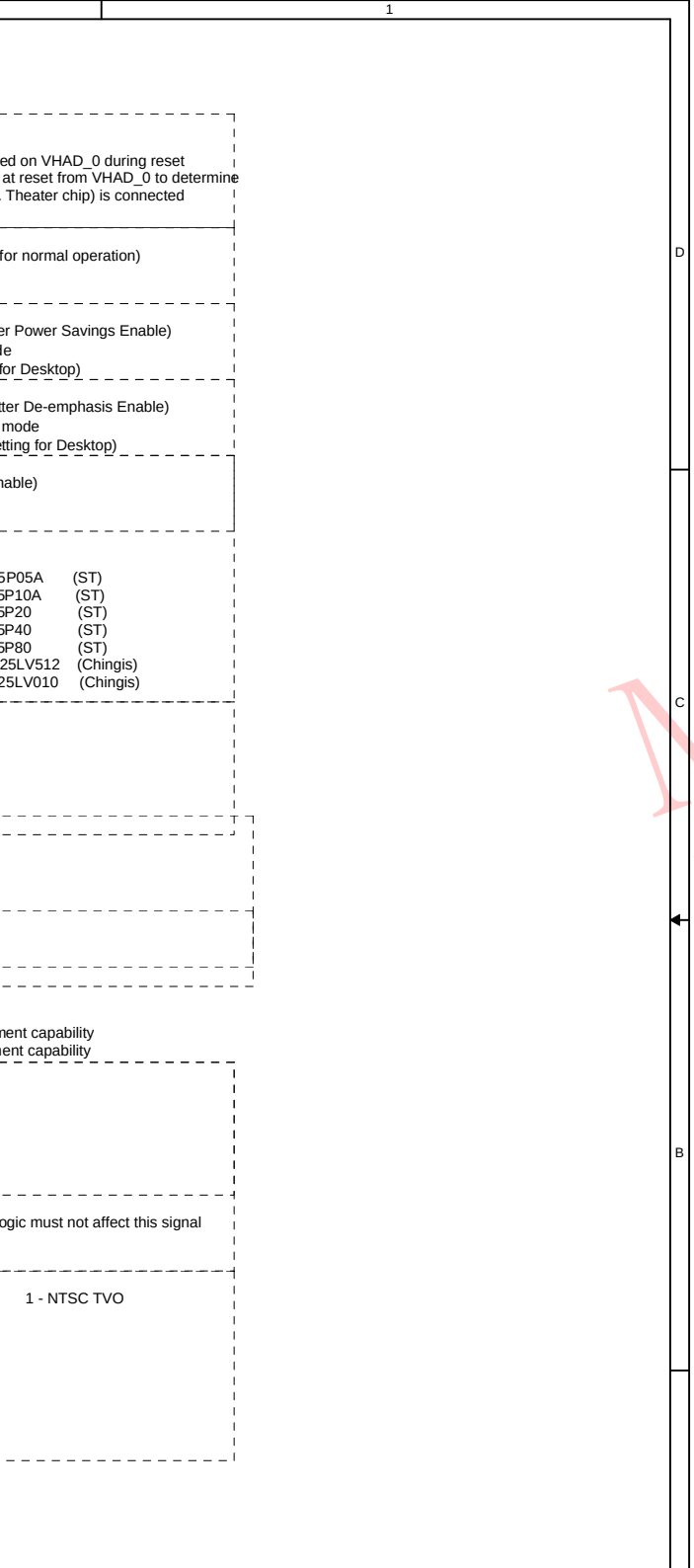
Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground — High logic voltage

Signal



Title RH LP RV710 DDR2 VC

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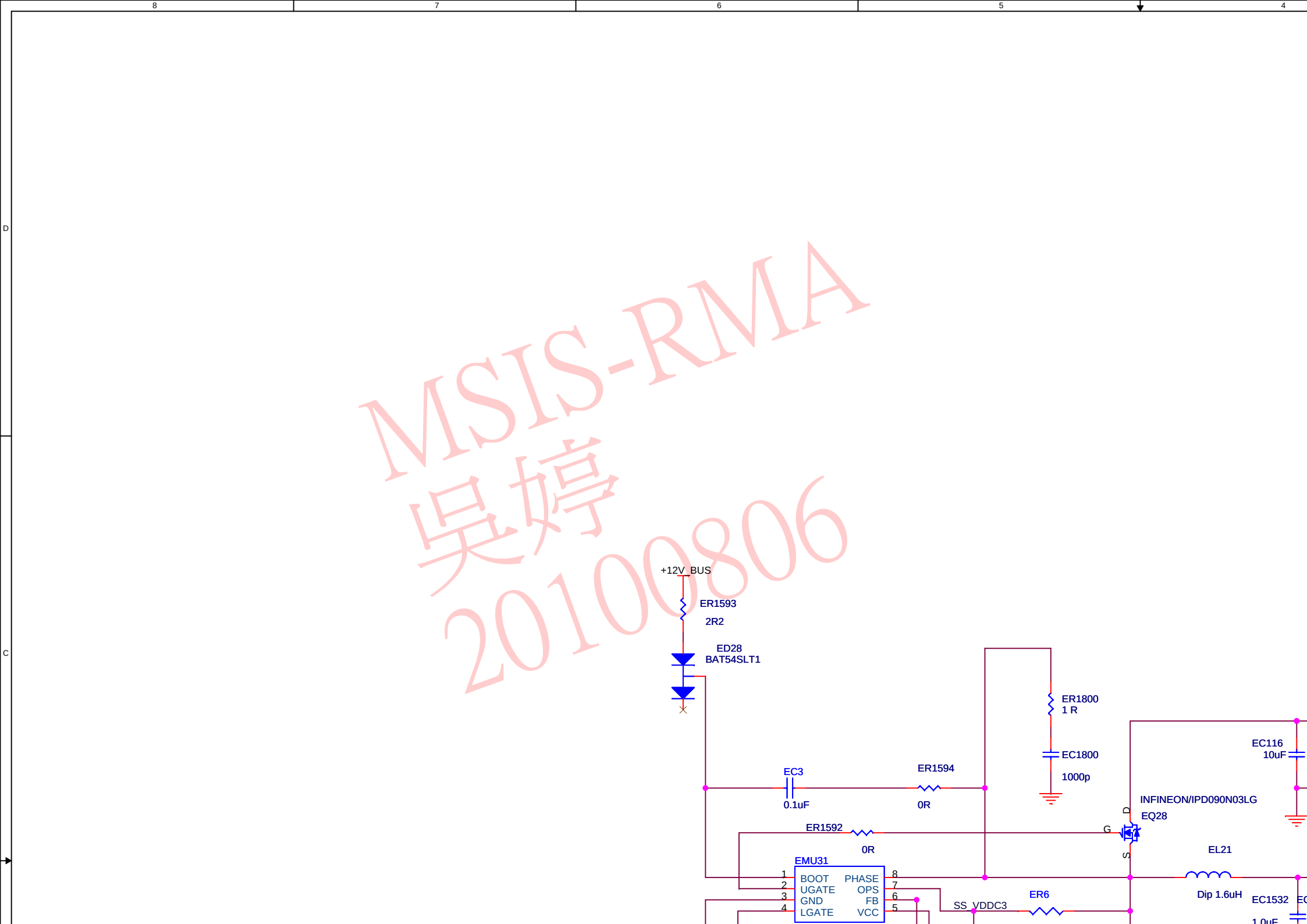
MSIS-RMA
吴婷
20100806
+12V_BUS
ER1593
2R2
ED28
BAT54SLT1
EC3
0.1uF
ER1594
0R
ER1592
0R
ER1800
1 R
EC1800
1000p
INFINEON/IPD090N03LG
EQ28
D
G
S
EC116
10uF
EL21
Dip 1.6uH
EC1532
EMU31
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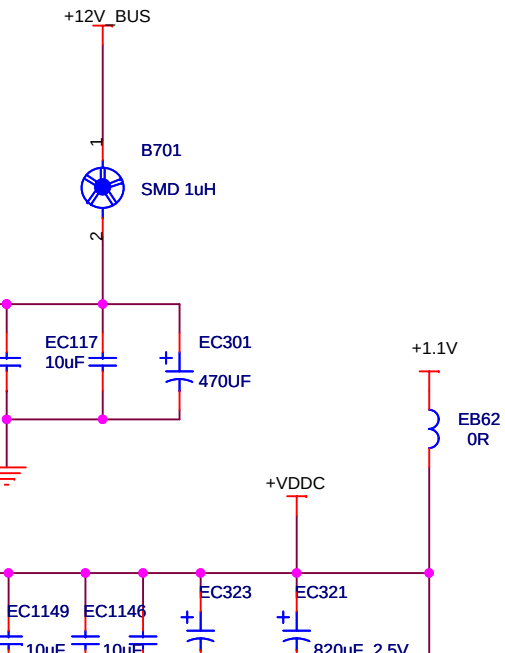
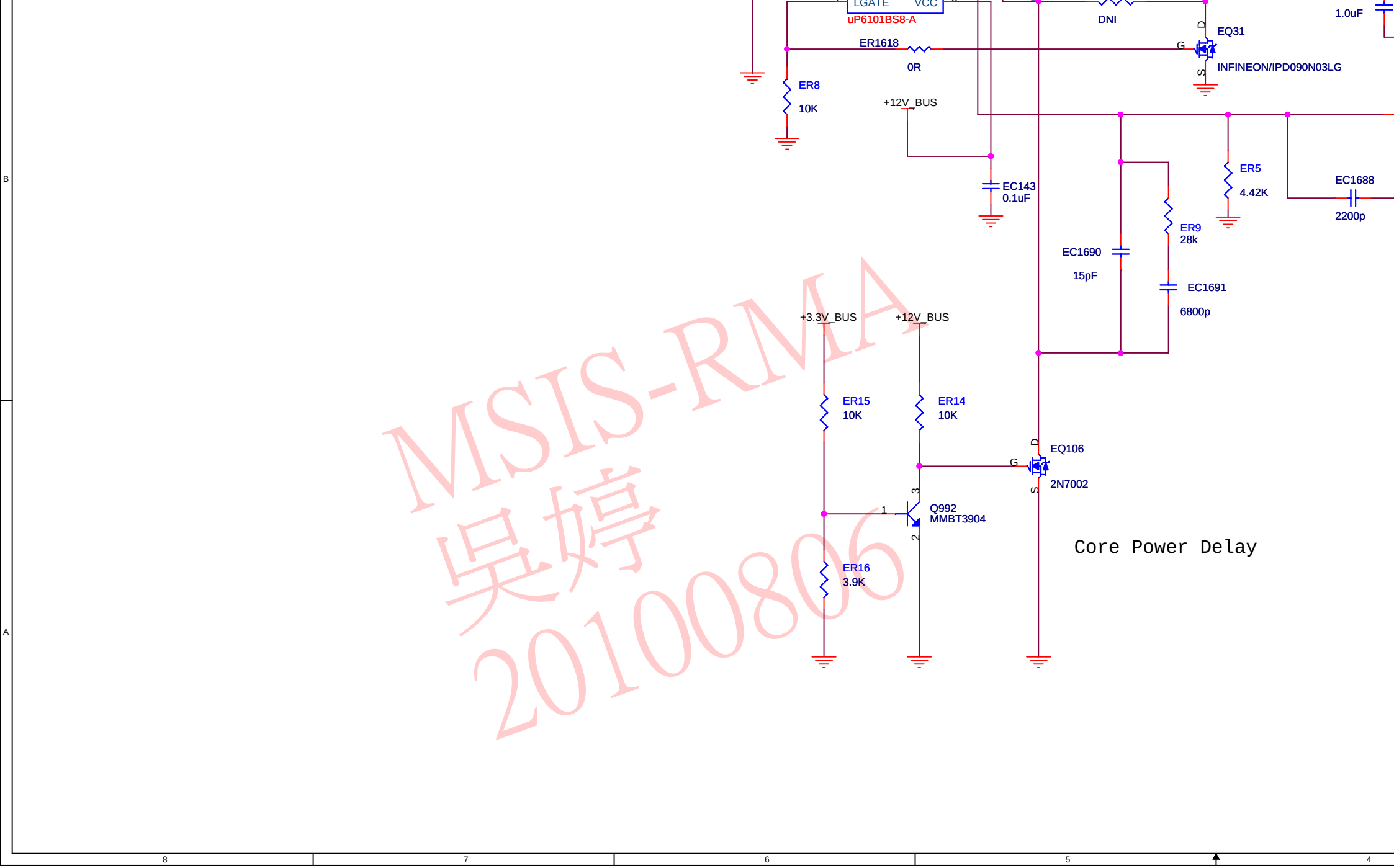
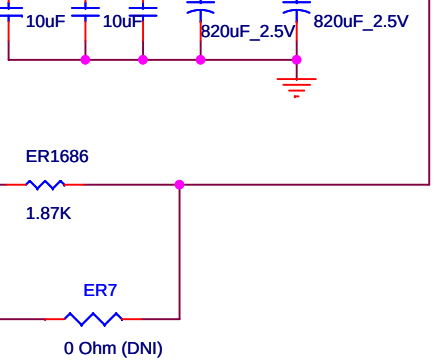
UGATE
GND
LGATE
PHASE
OPS
FB
VCC
SS_VDDC3
ER6







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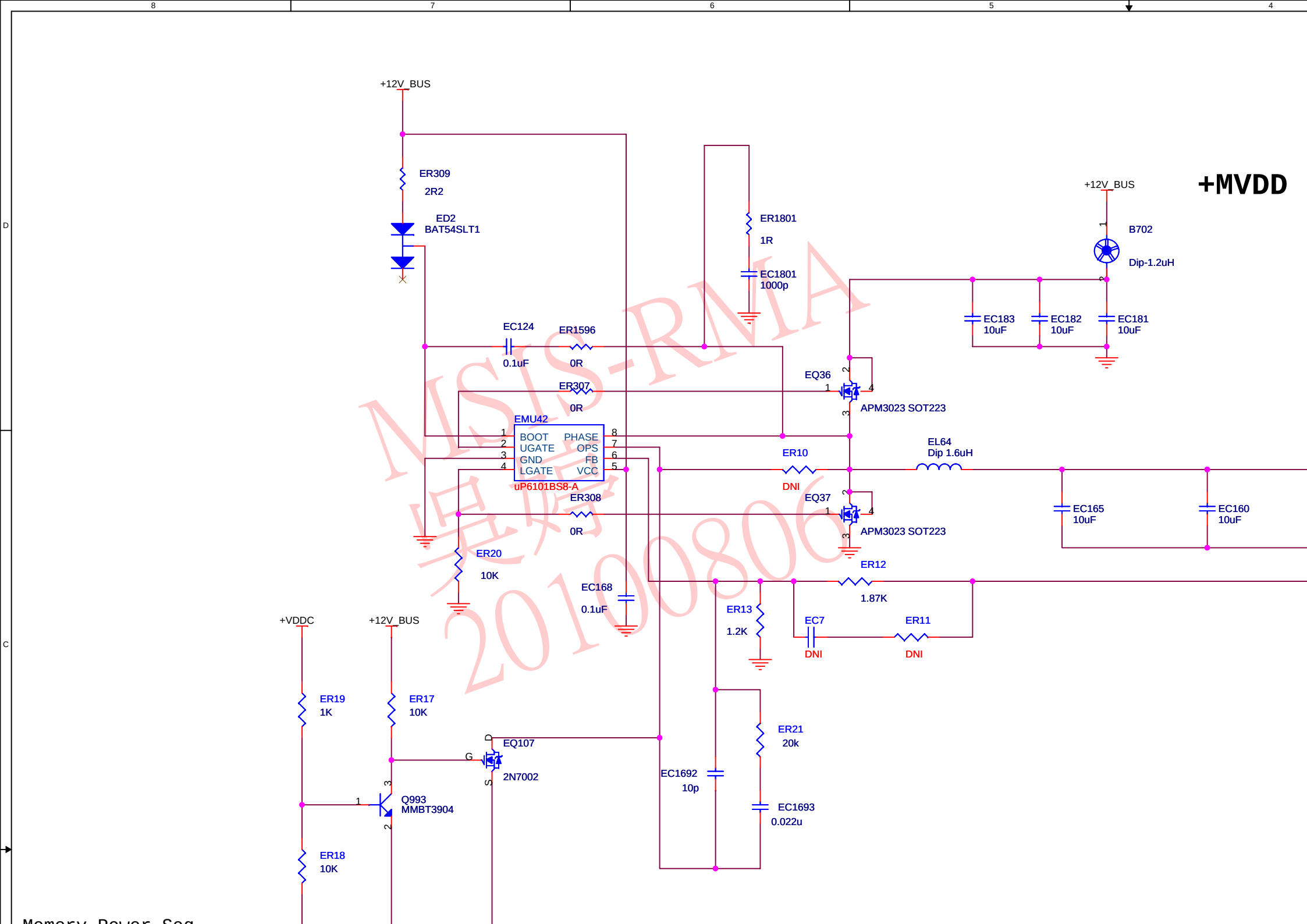
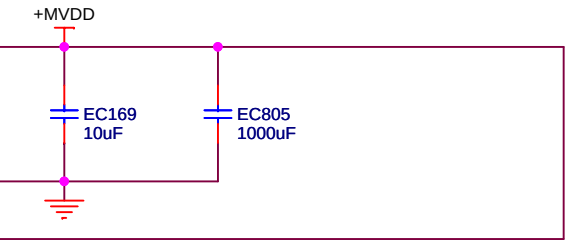
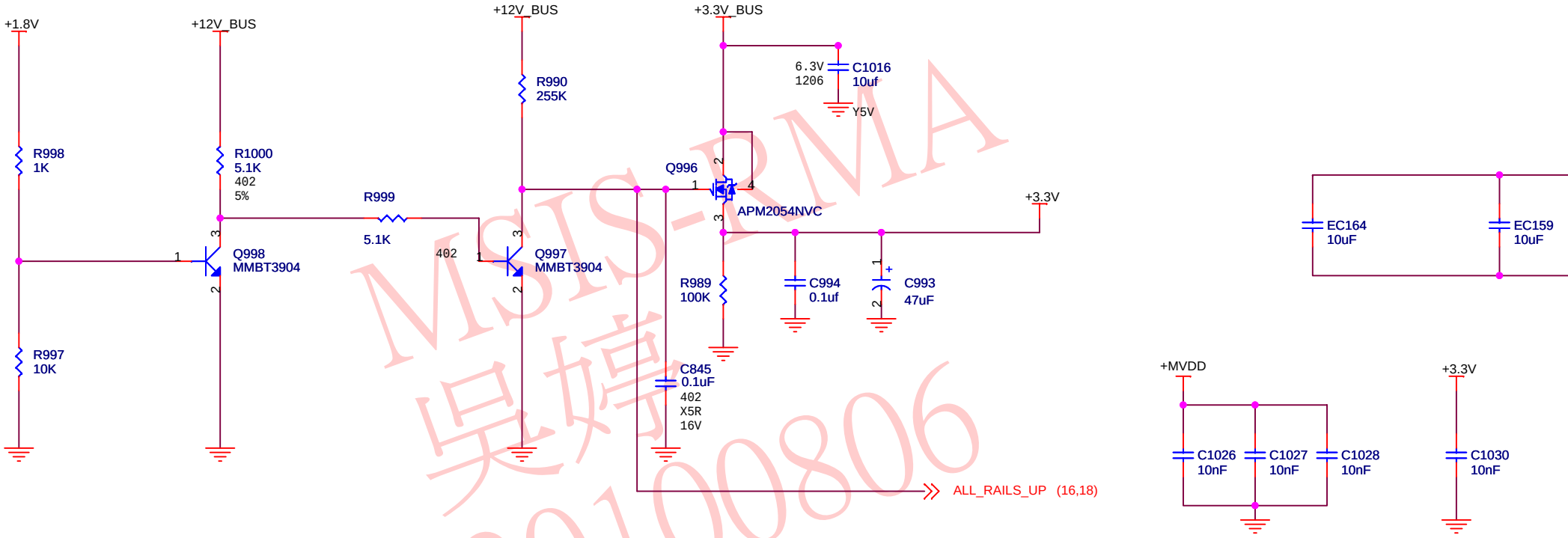
3 2 1

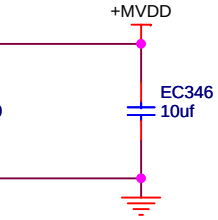


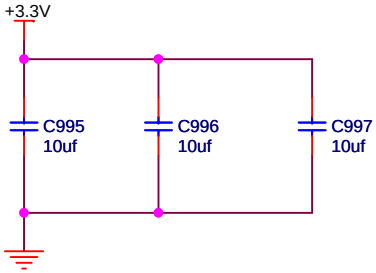
= 0.8 * (1+ (ER12 / ER13))

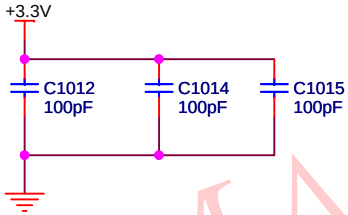


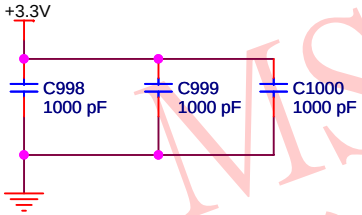
Memory Power Seq

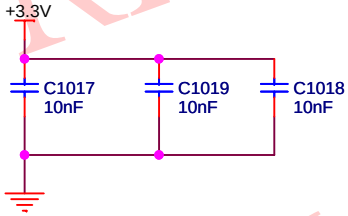












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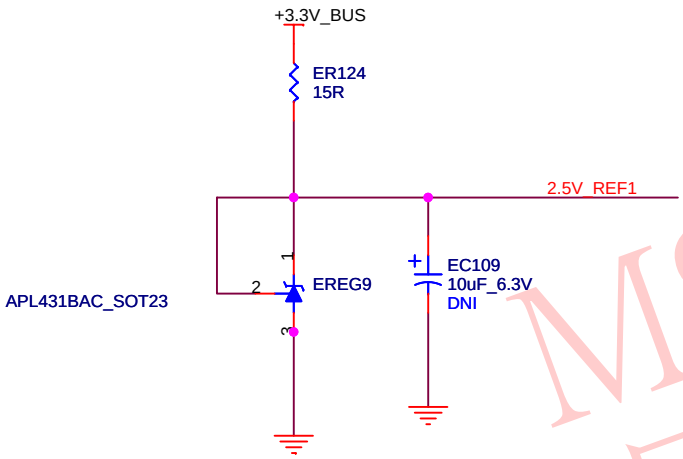
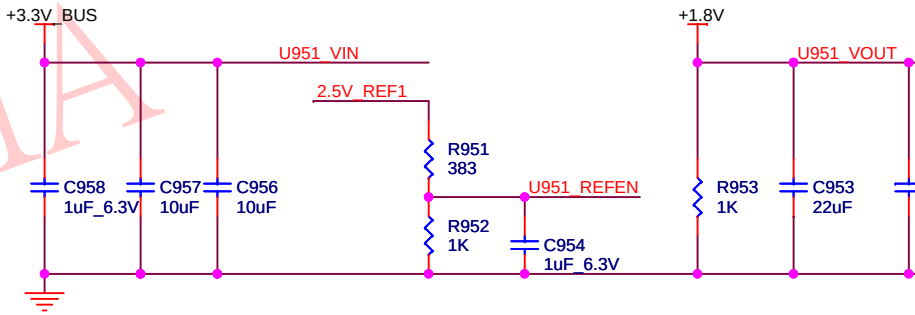
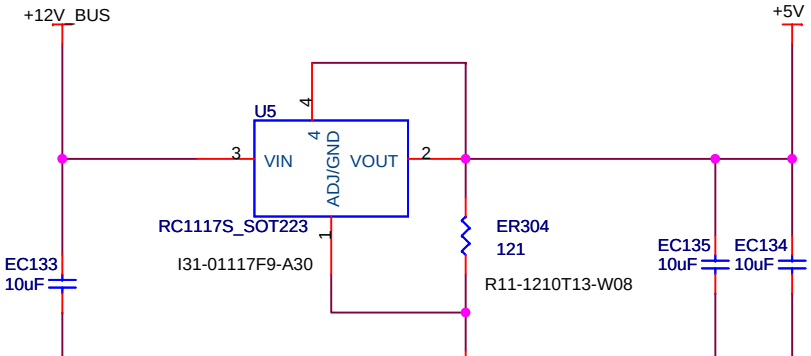
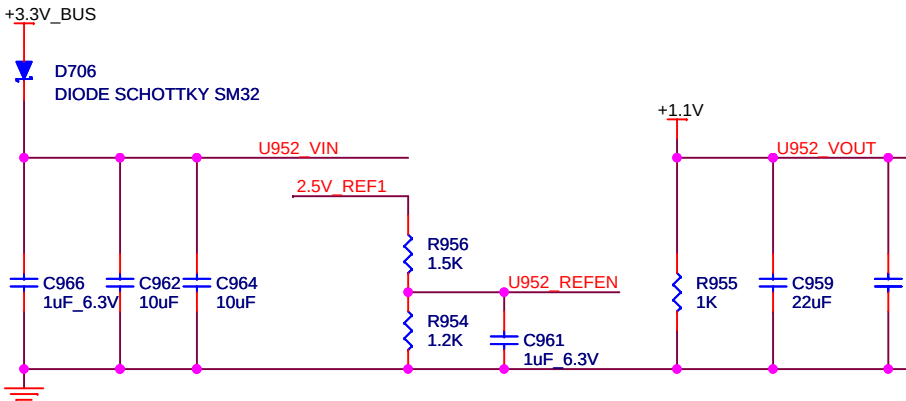
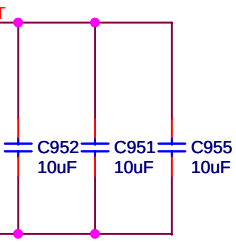
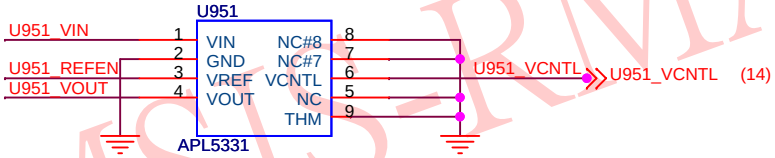


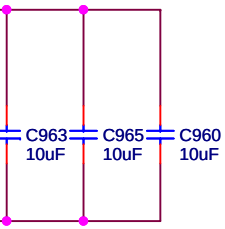


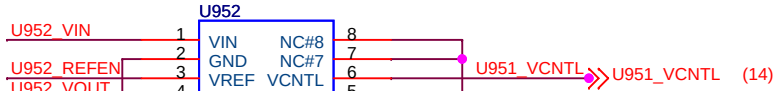


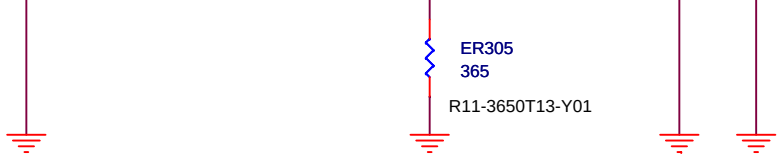




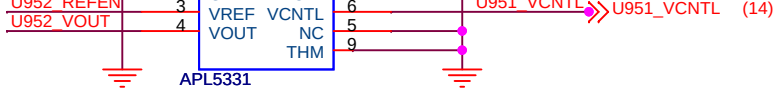








Vout=1.25V* [1+(ER305/ER304)]



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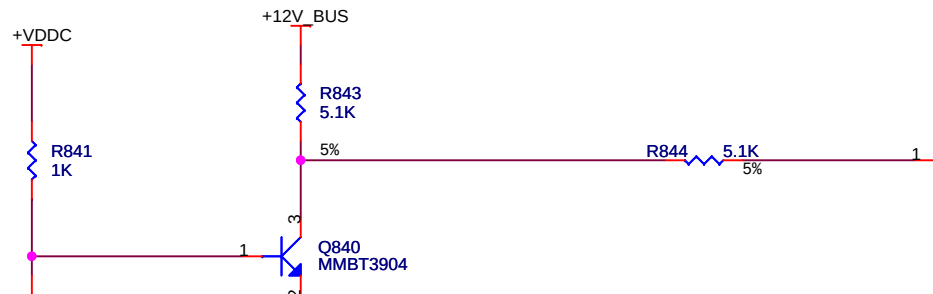

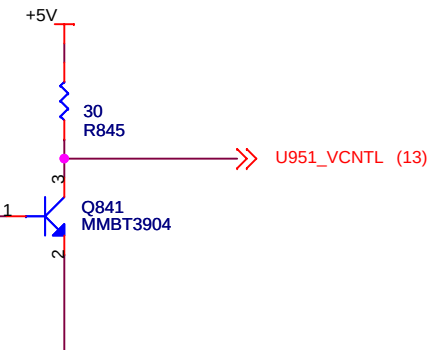

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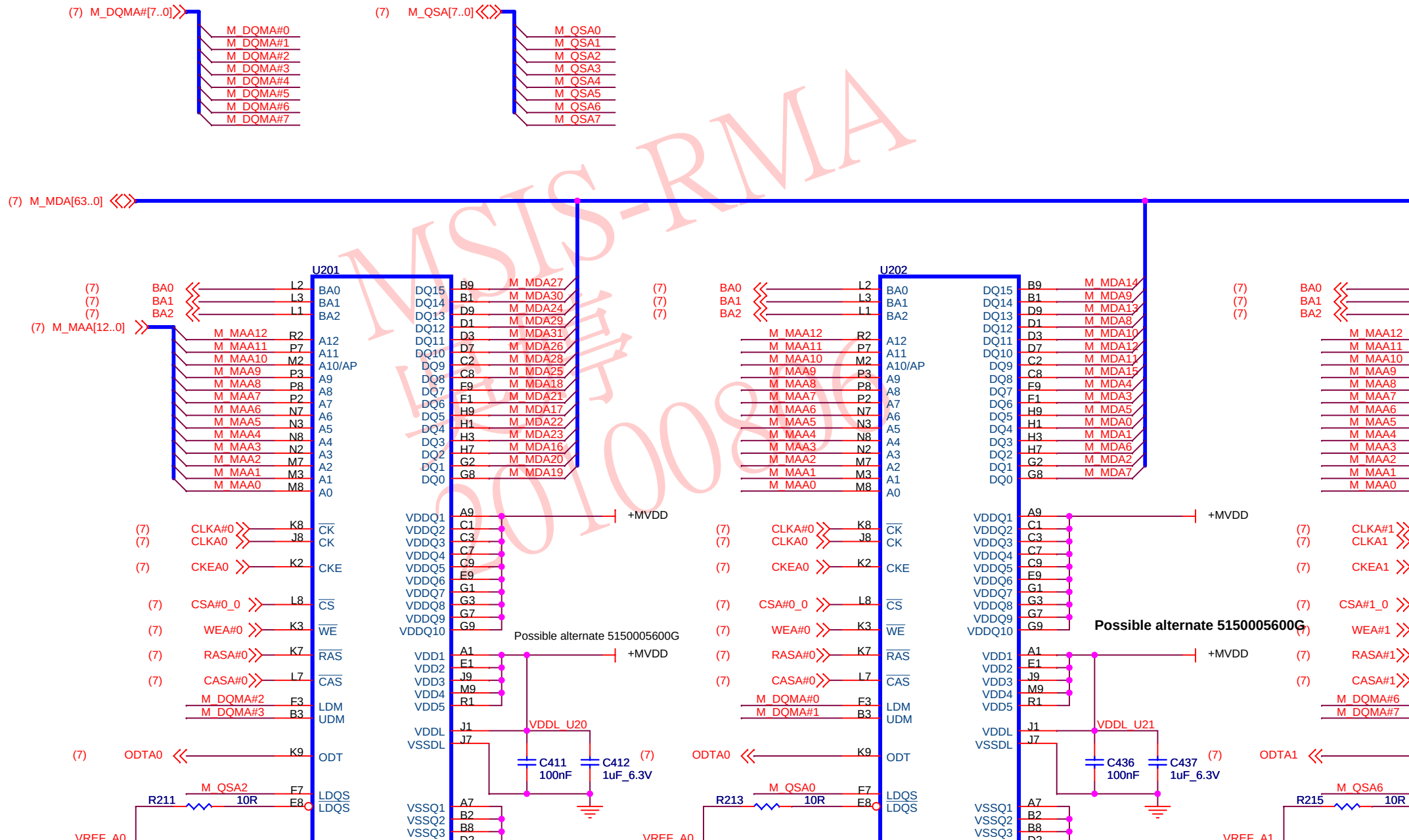
Title RH LP RV710 DDR2 VGA (header) TVO DVI

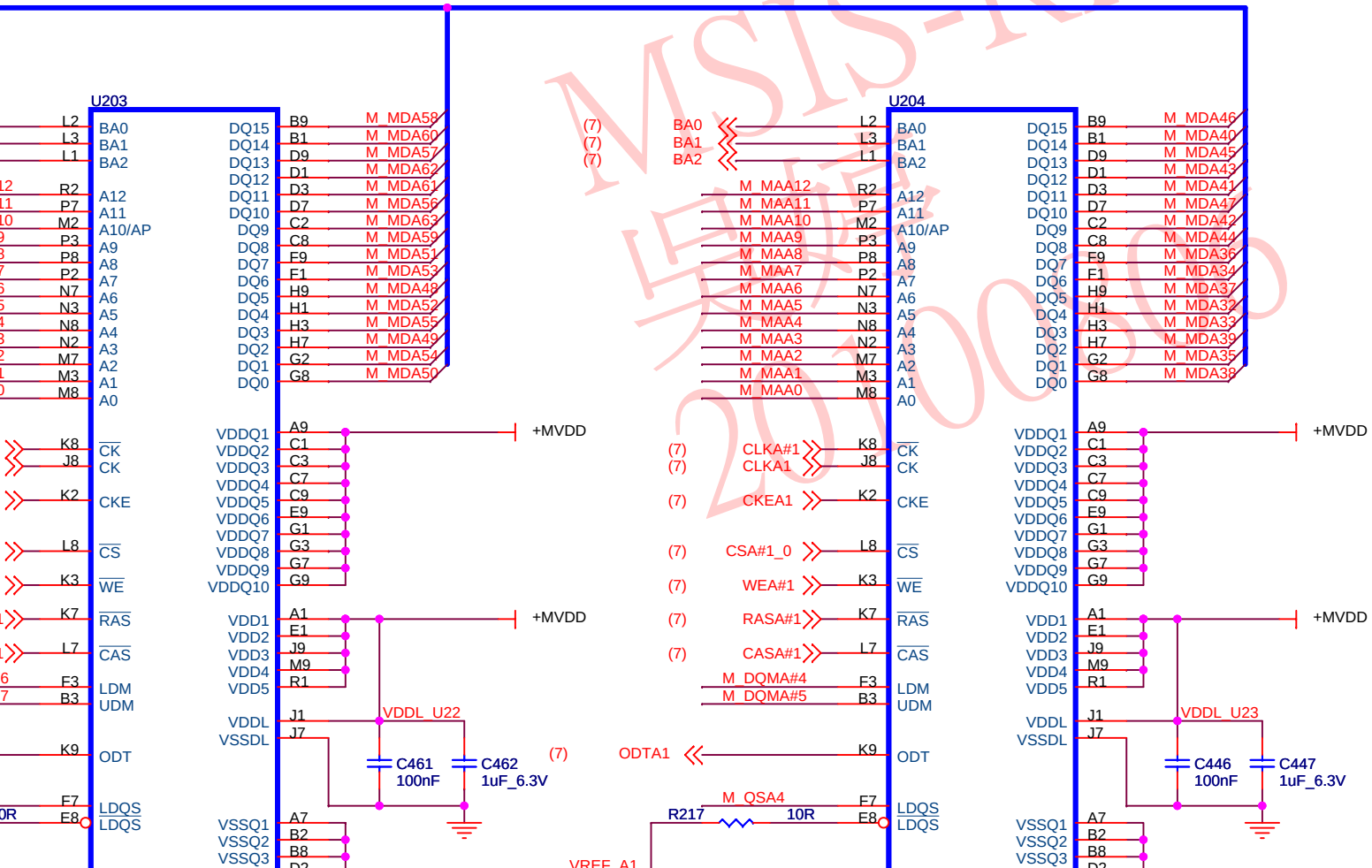
Doc No. 105-B750XX-00A

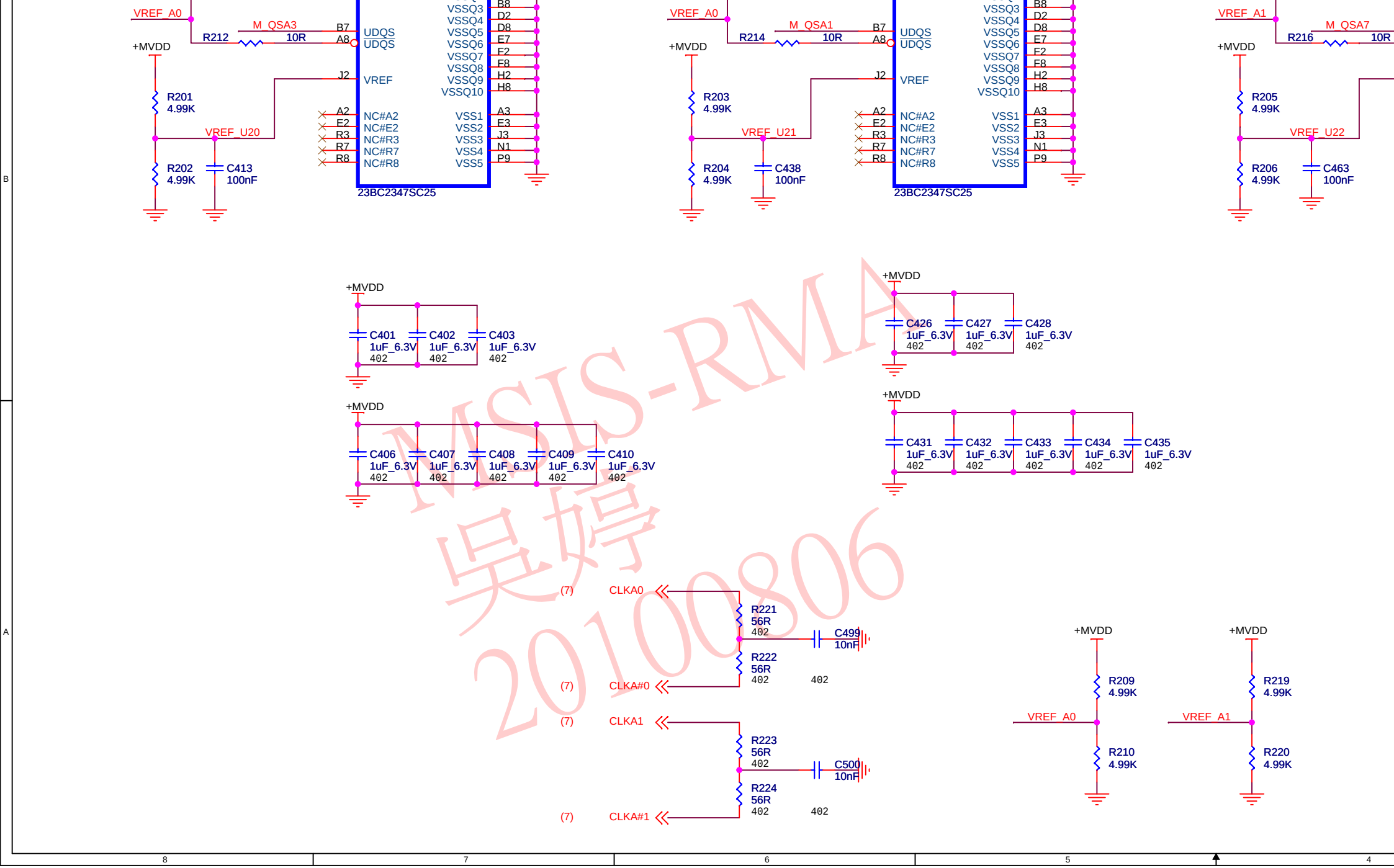
CHANNEL A: RANK 0 512MB DD

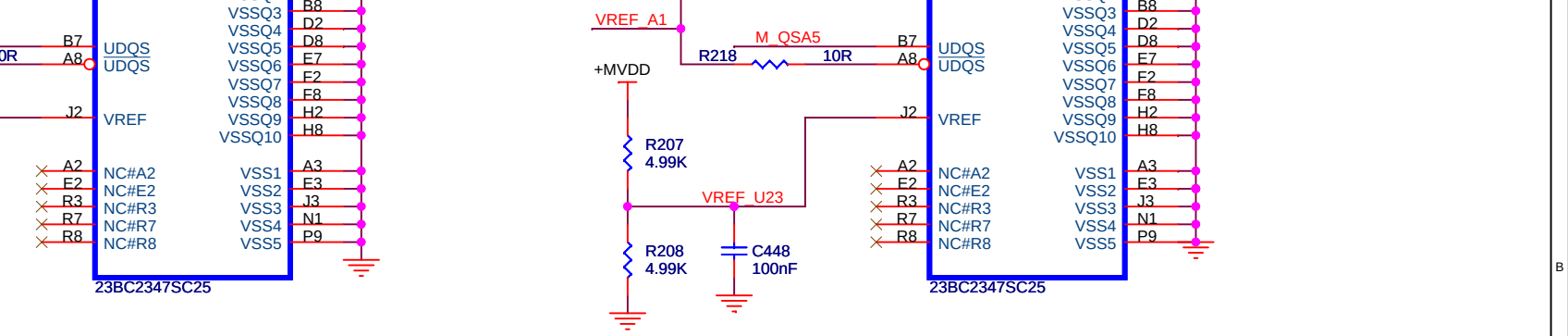
MAX DENSITY: 64Mx16

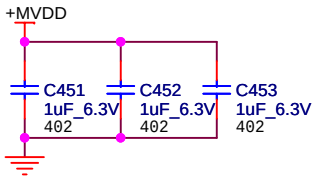


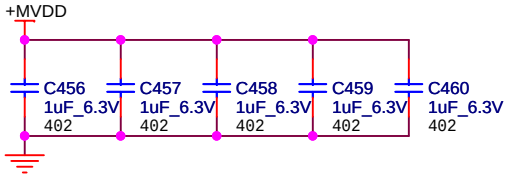
DR2

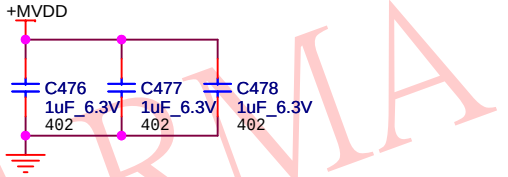


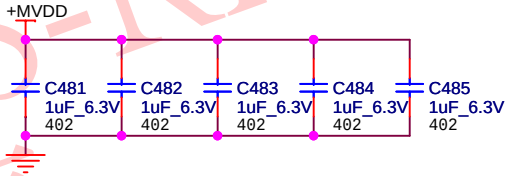












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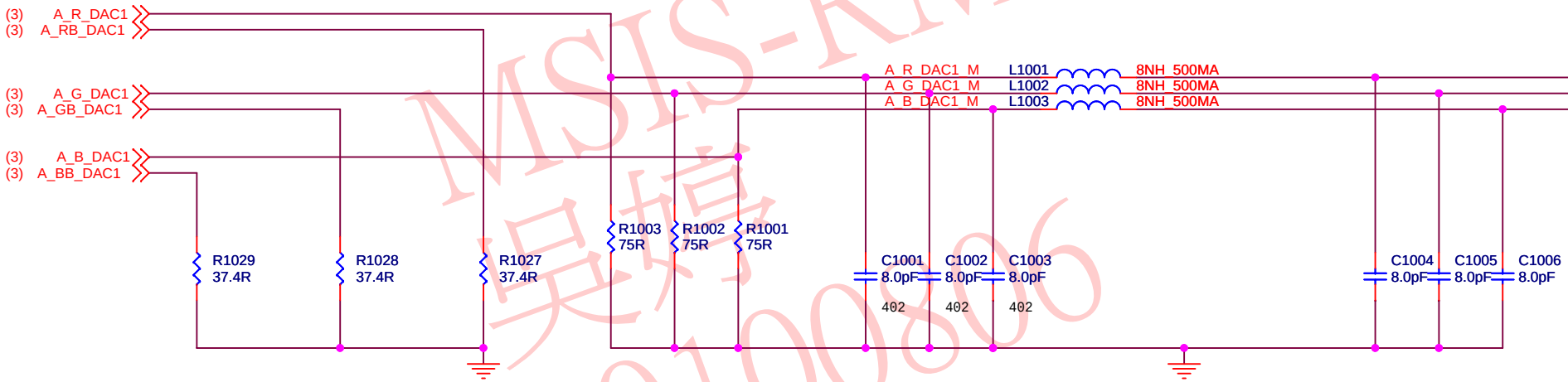
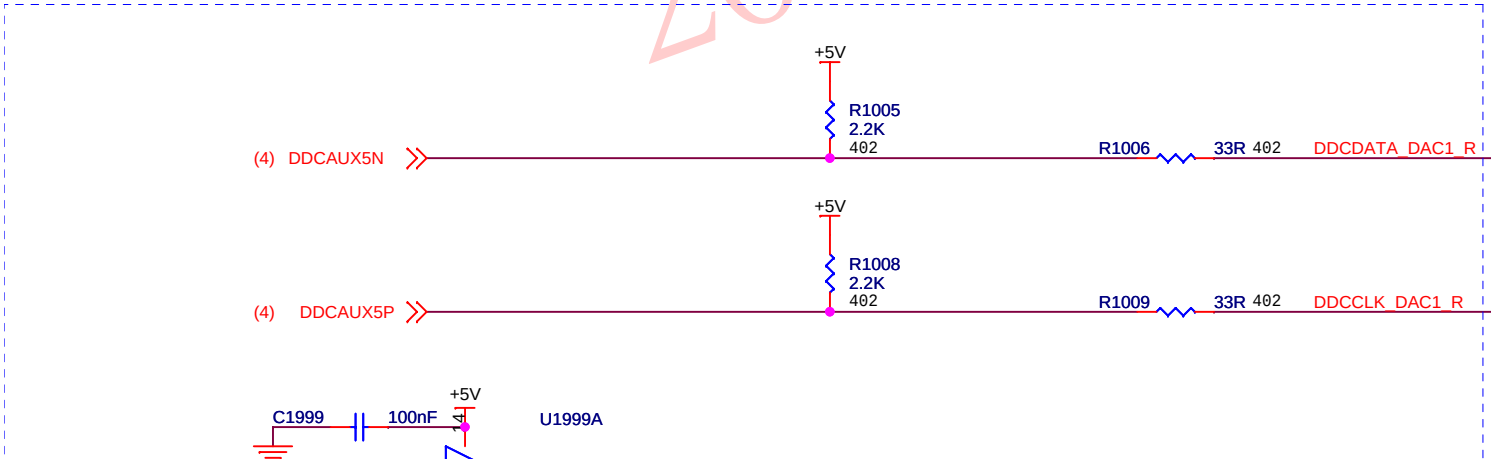
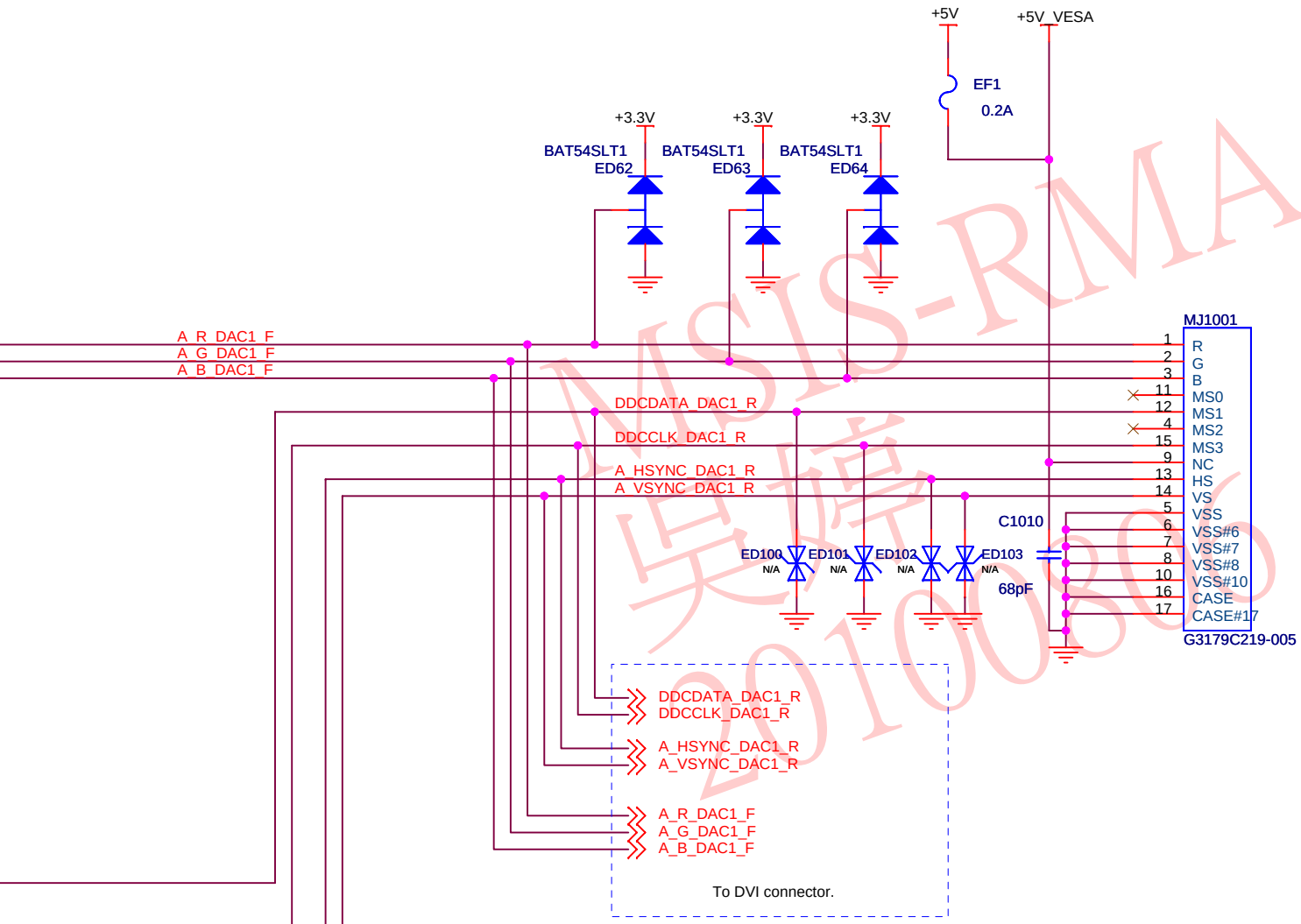
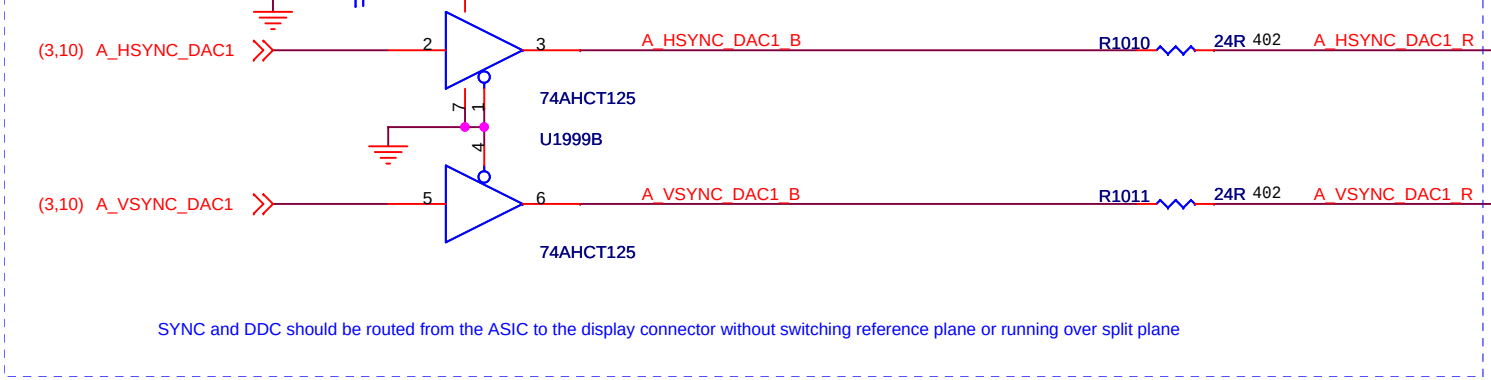
DAC 1 OUTPUT

Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)



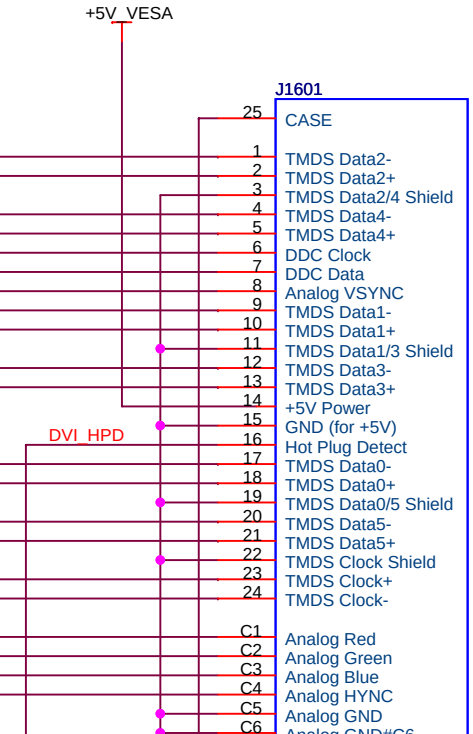


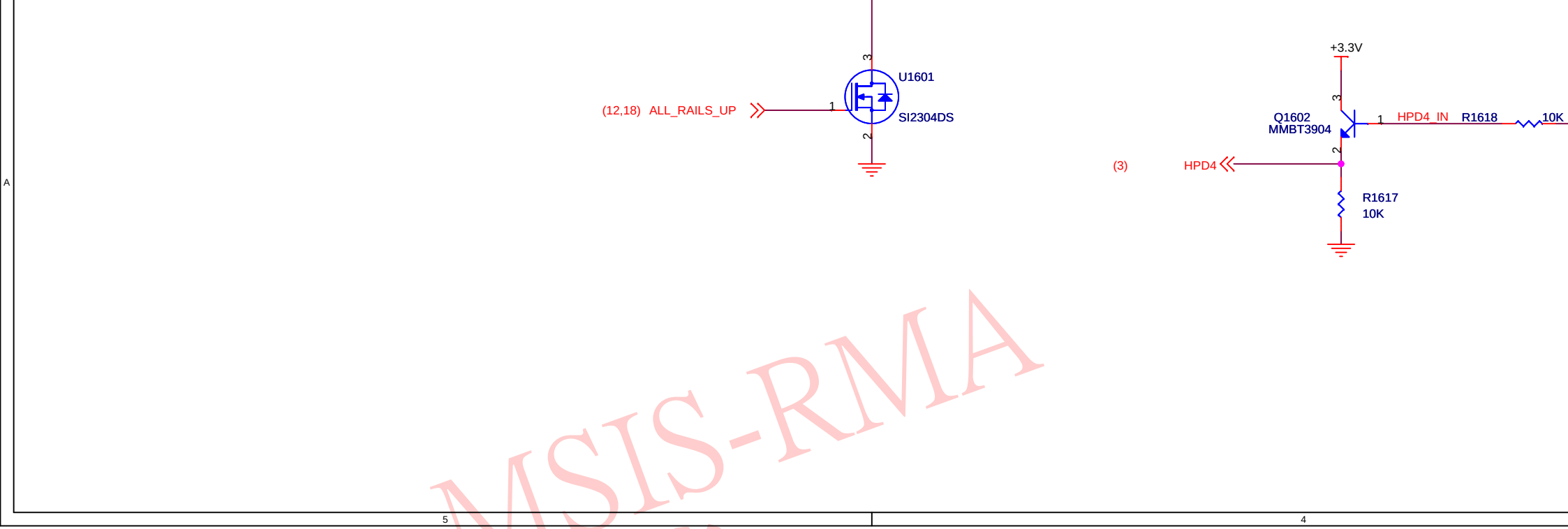


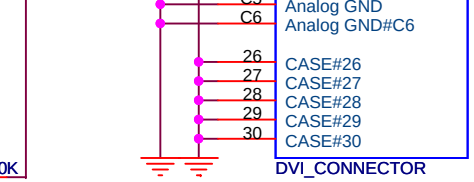


SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DPE / DPF OUTPUT







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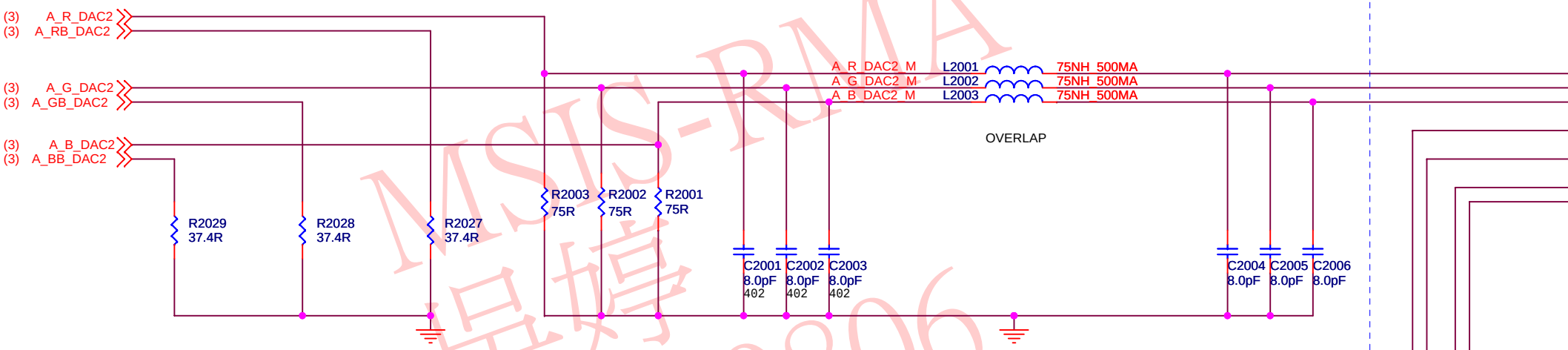
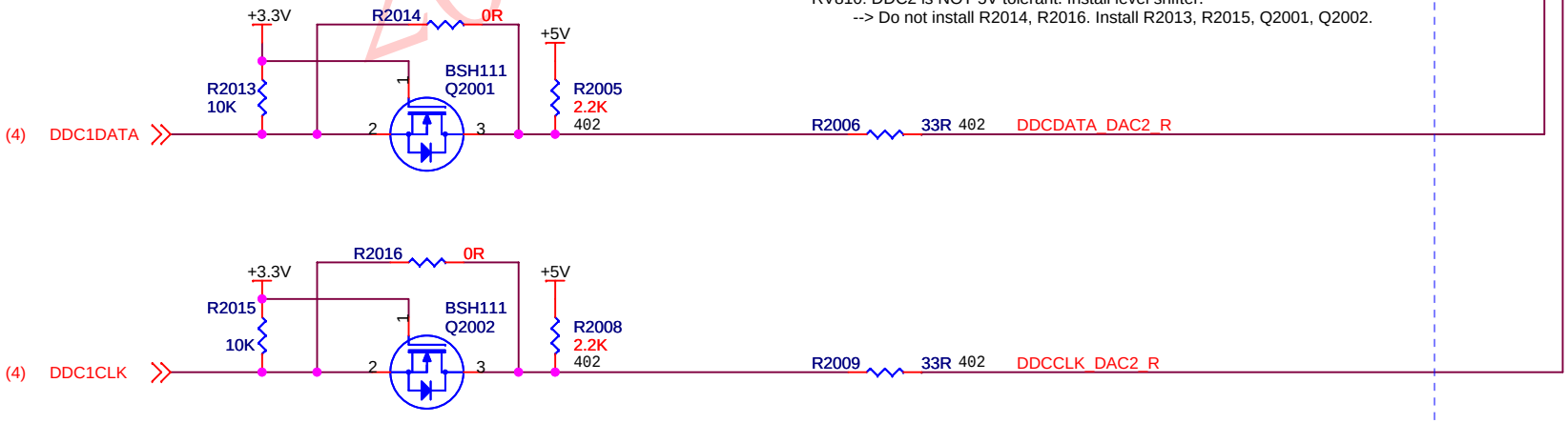
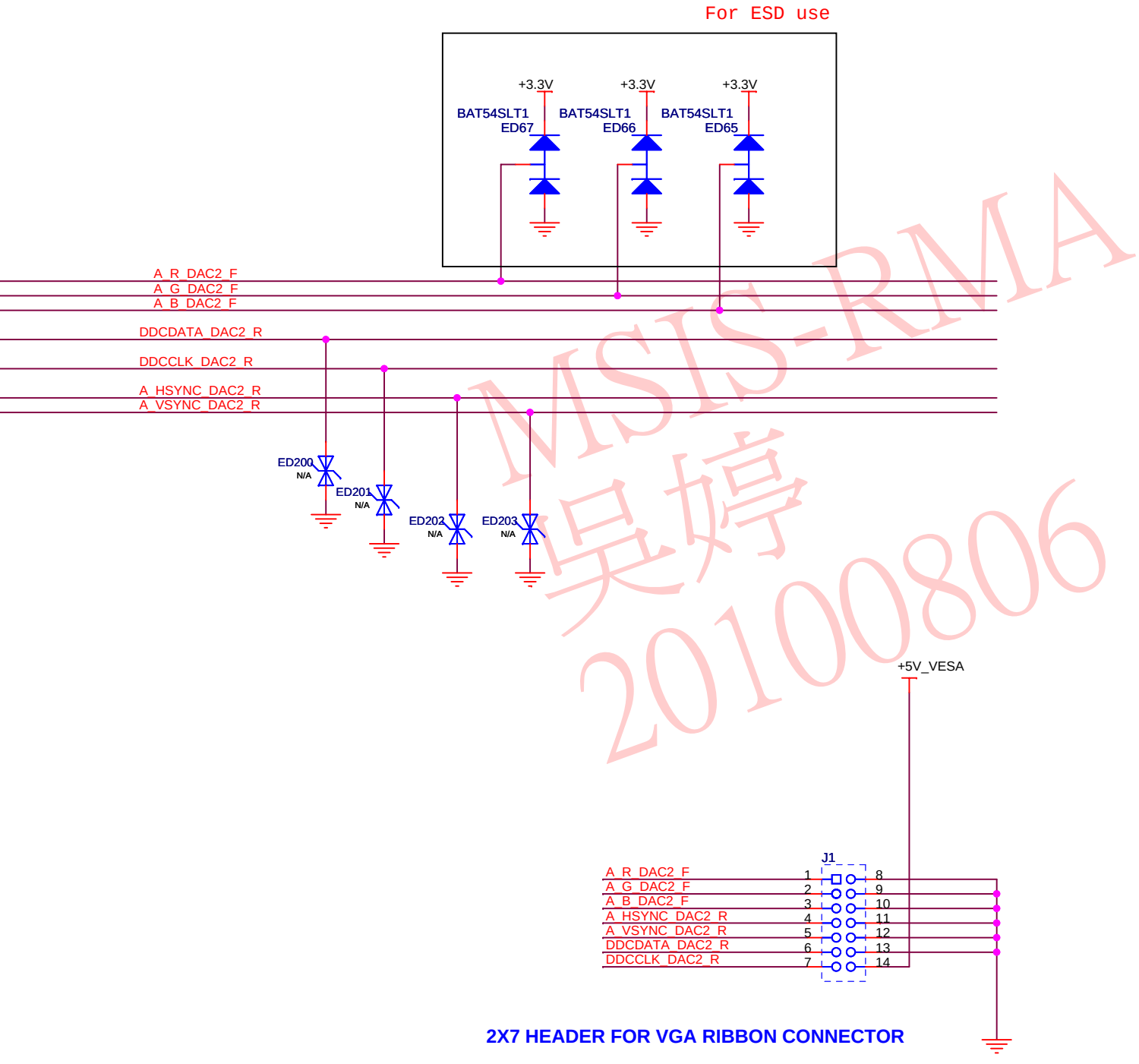
DAC 2 OUTPUT

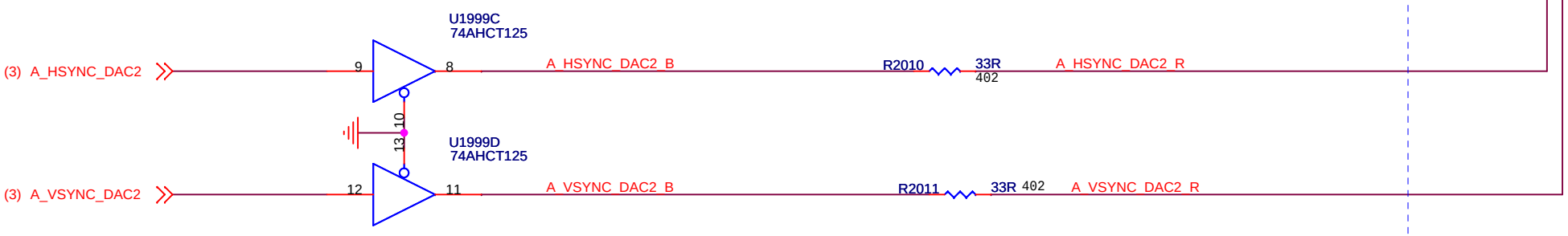
Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane



RV710: DDC2 is 5V tolerant. Do not install level shifter.
--> Do not install R2013, R2015, Q2001, Q2002. Install R2014, R2016.
RV810: DDC2 is NOT 5V tolerant. Install level shifter.
--> Do not install R2014, R2016. Install R2013, R2015, Q2001, Q2002.







SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

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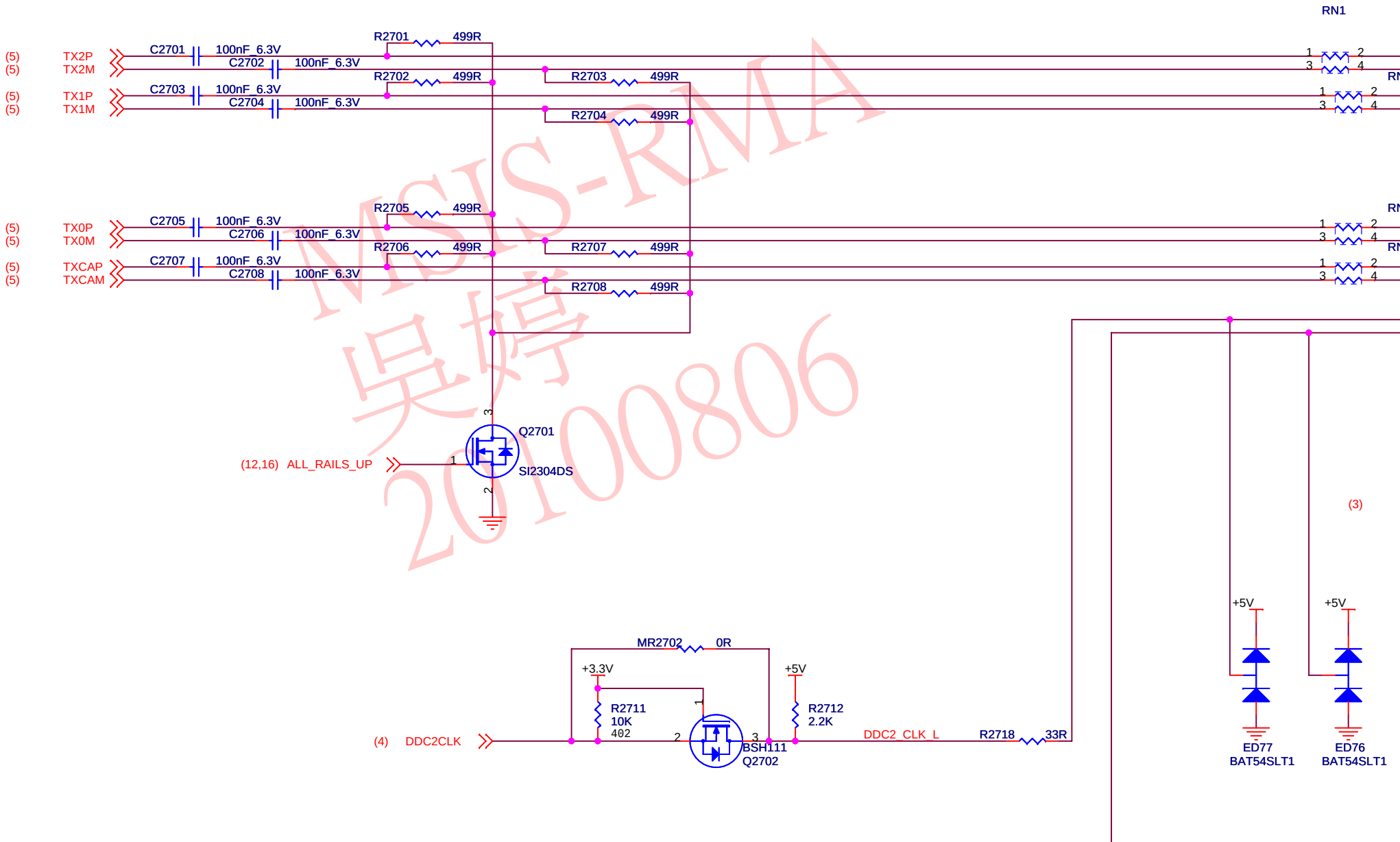
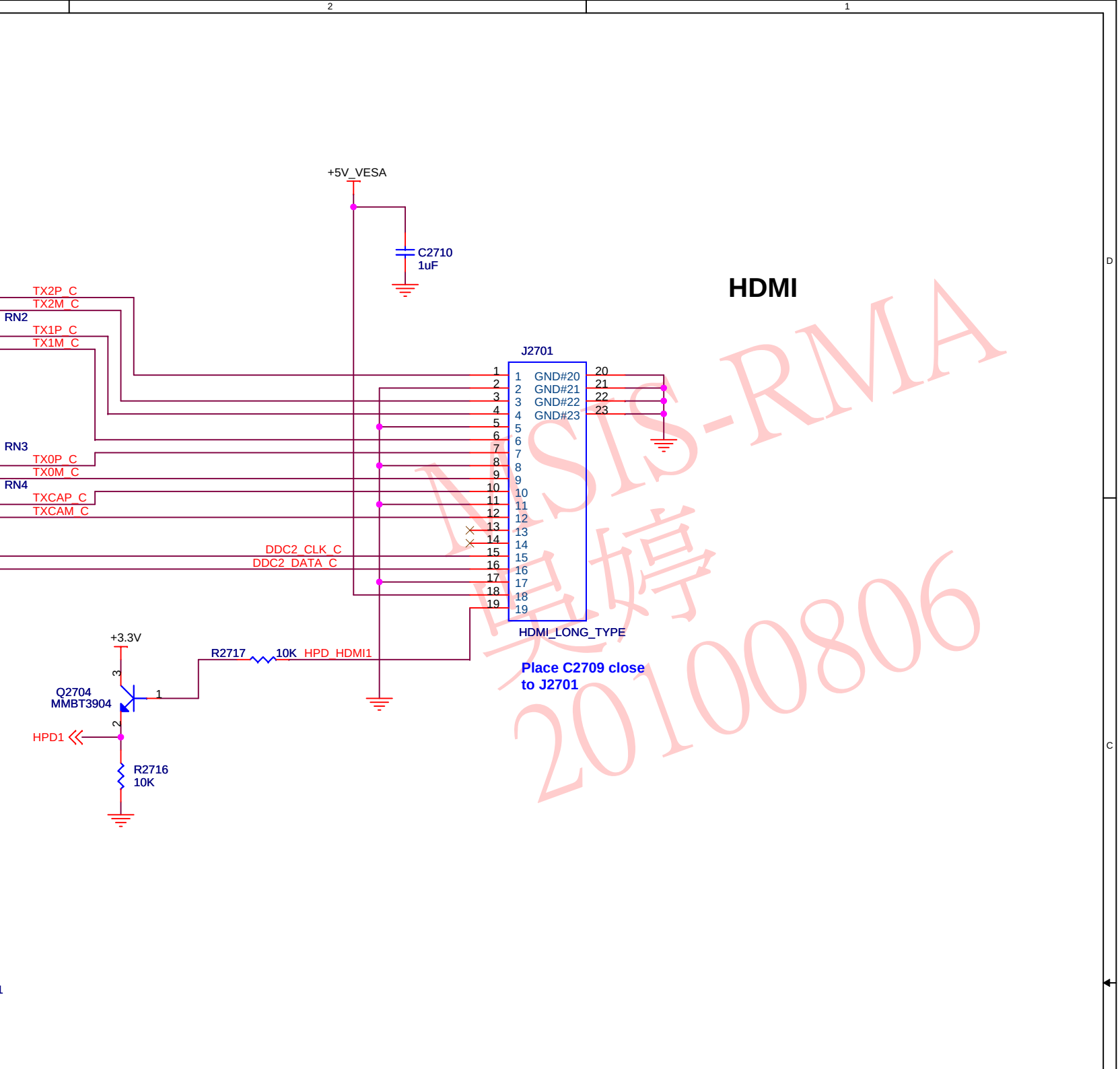
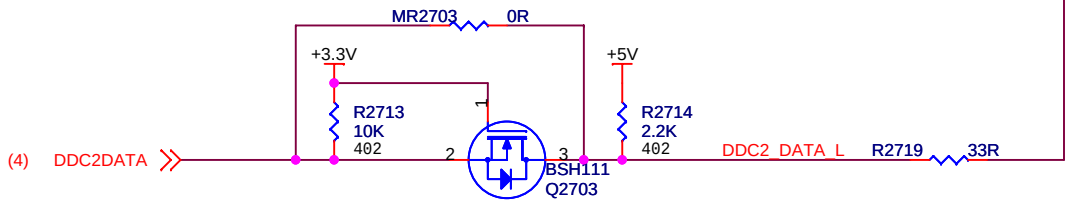
Doc No. 105-B750XX-00A




HDMI
+5V_VESA
C2710
1uF
TX2P_C
TX2M_C
RN2
TX1P_C
TX1M_C
RN3
TX0P_C
TX0M_C
RN4
TXCAP_C
TXCAM_C
DDC2_CLK_C
DDC2_DATA_C
J2701
1 GND#20
2 GND#21
3 GND#22
4 GND#23
HDMI_LONG_TYPE
Place C2709 close
to J2701
+3.3V
R2717
10K
HPD_HDMI1
Q2704
MMBT3904
HPD1
R2716
10K
ASIS-RMA
吳婷
20100806

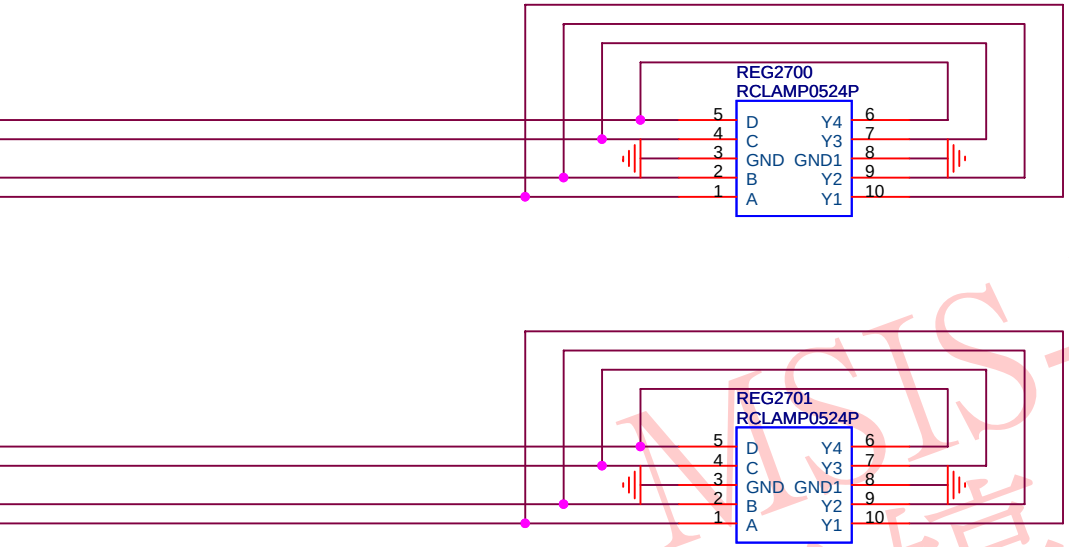


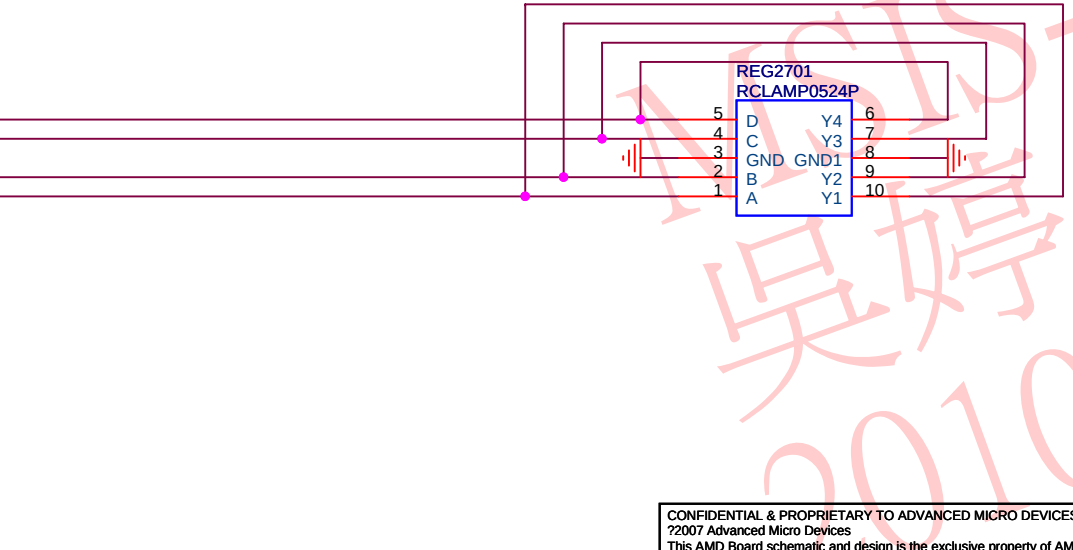
TX2P_C
TX2M_C
TX1P_C
TX1M_C

TX0P_C
TX0M_C
TXCAP_C
TXCAM_C

B
A
5
4
3

Optional ESD protection diodes





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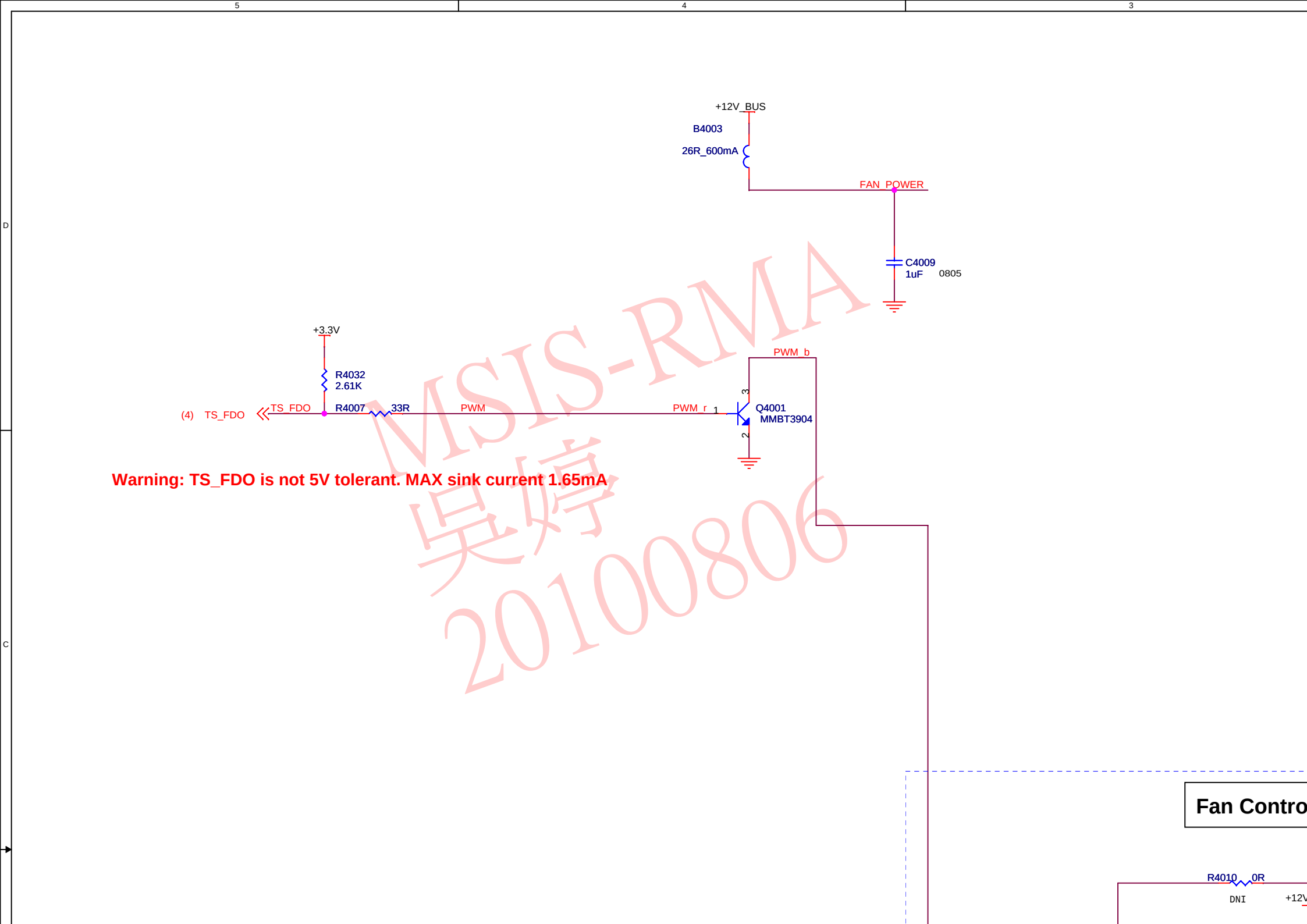
Title: RH LP RV710 DDR2 VGA (header) TVO DVI | Doc No. 105-B750XX-00A

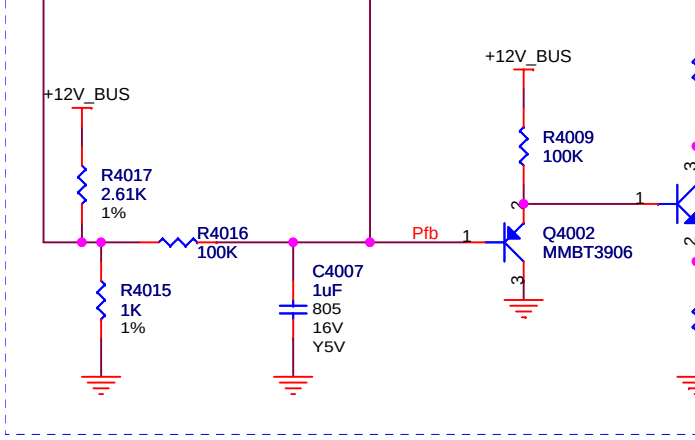


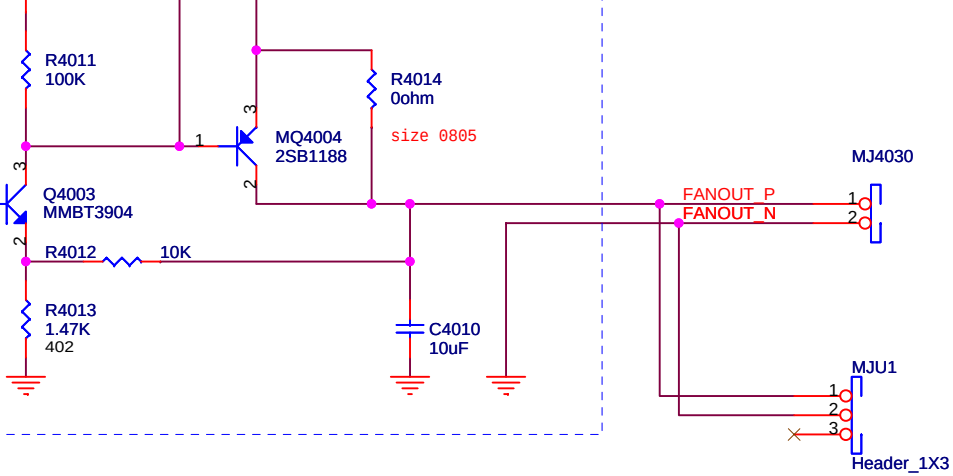
rol (Legacy)

For 2-WIRE FAN ONLY

FAN_POWER

12V_BUS





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Title: RH LP RV710 DDR2 VGA (header) TVO DVI

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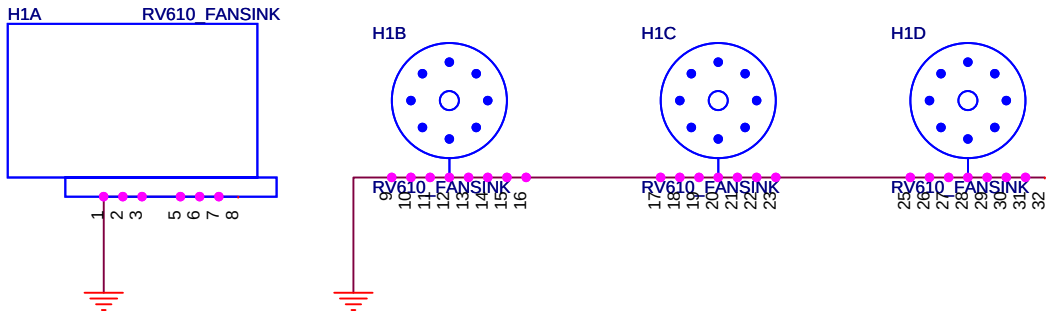

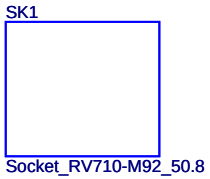

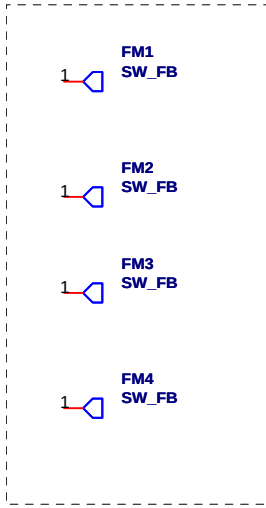

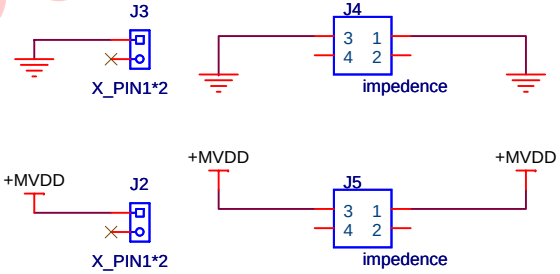

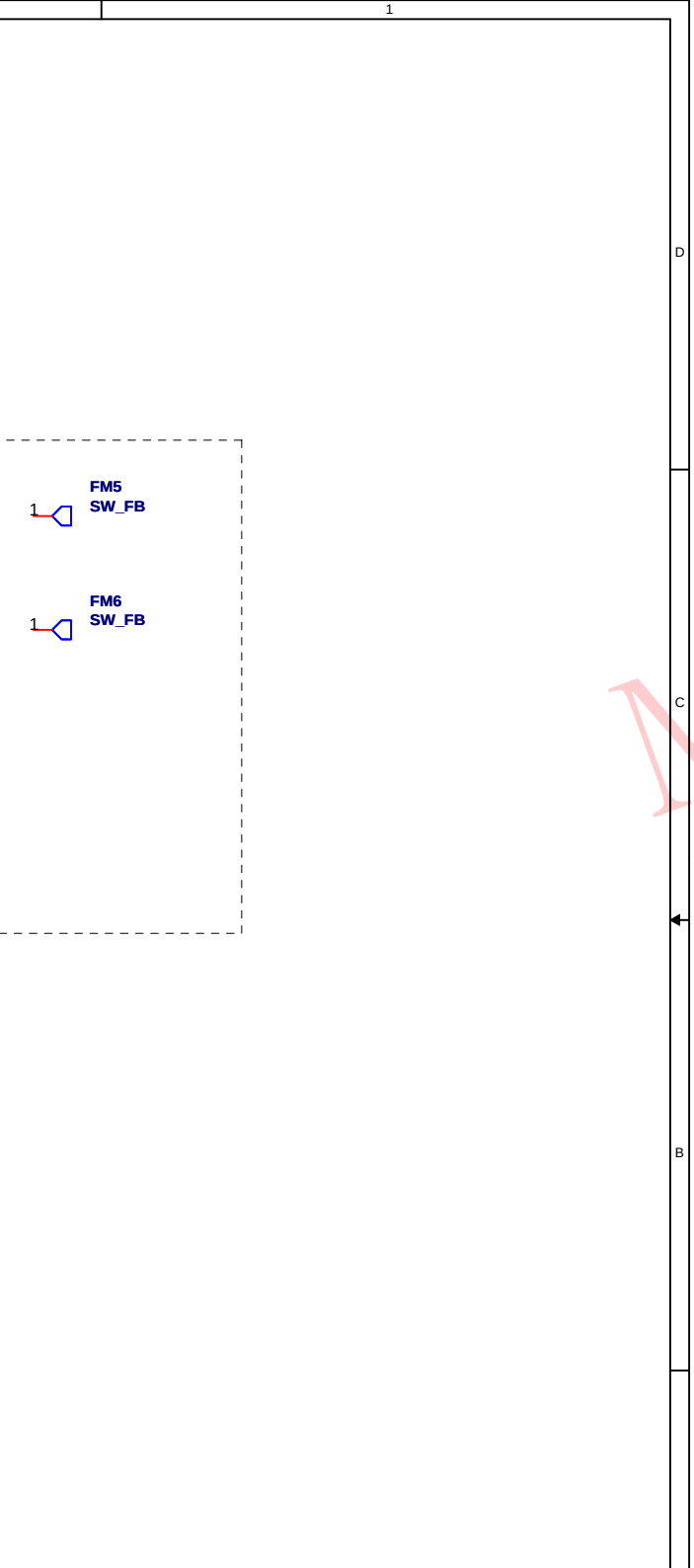

Title RH LP RV710 DDR2 VC

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VGA (header) TVO DVI

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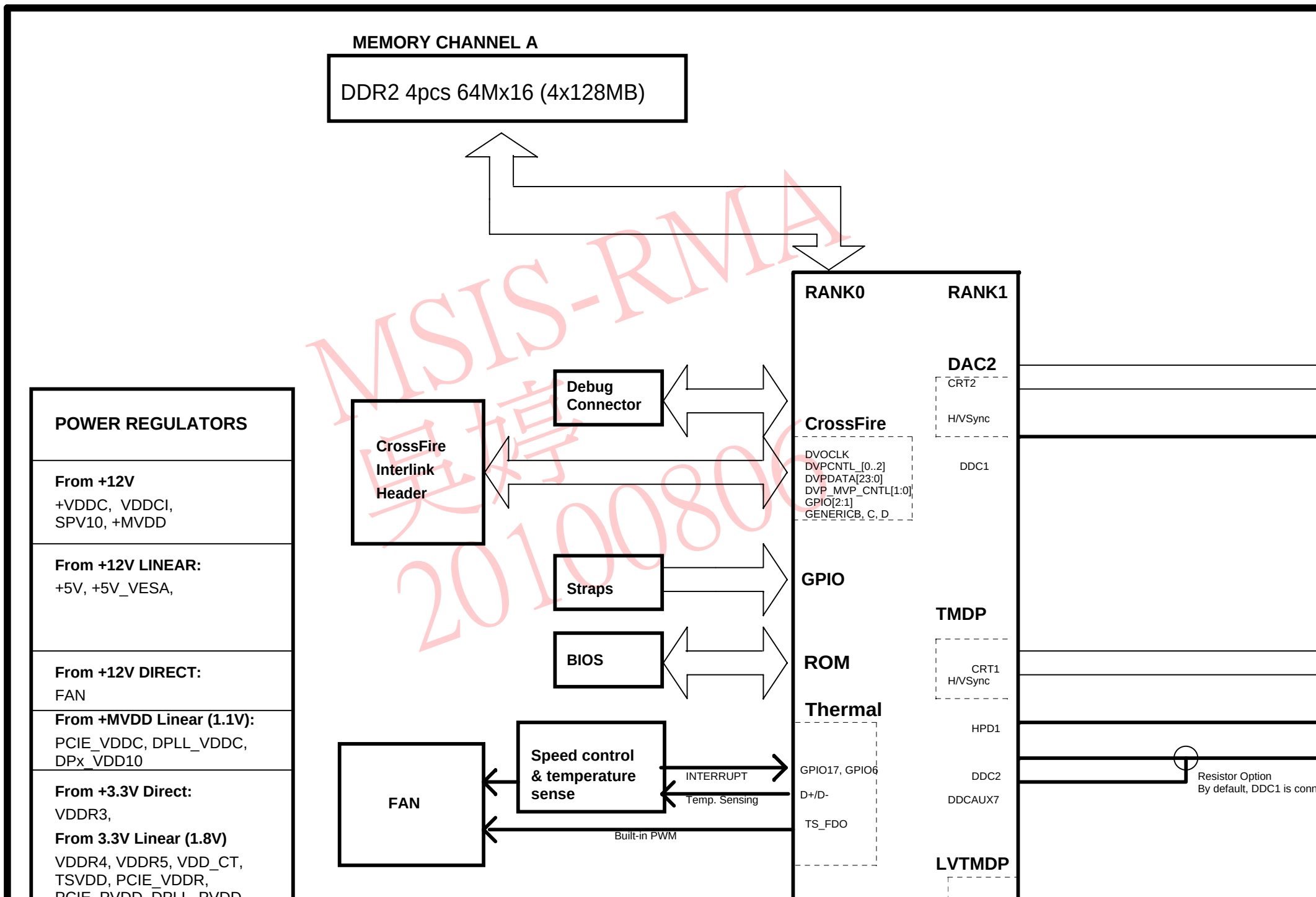
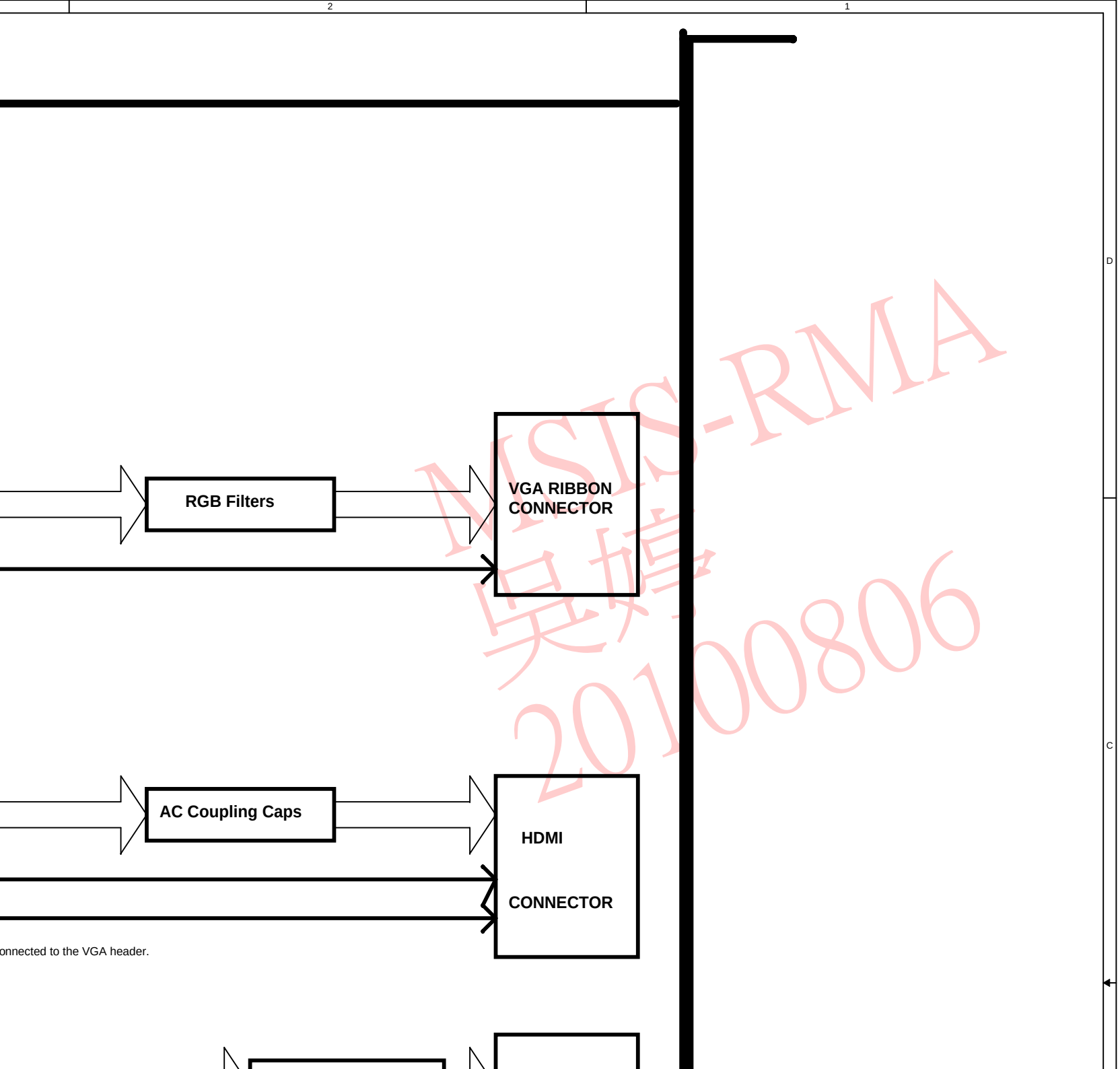
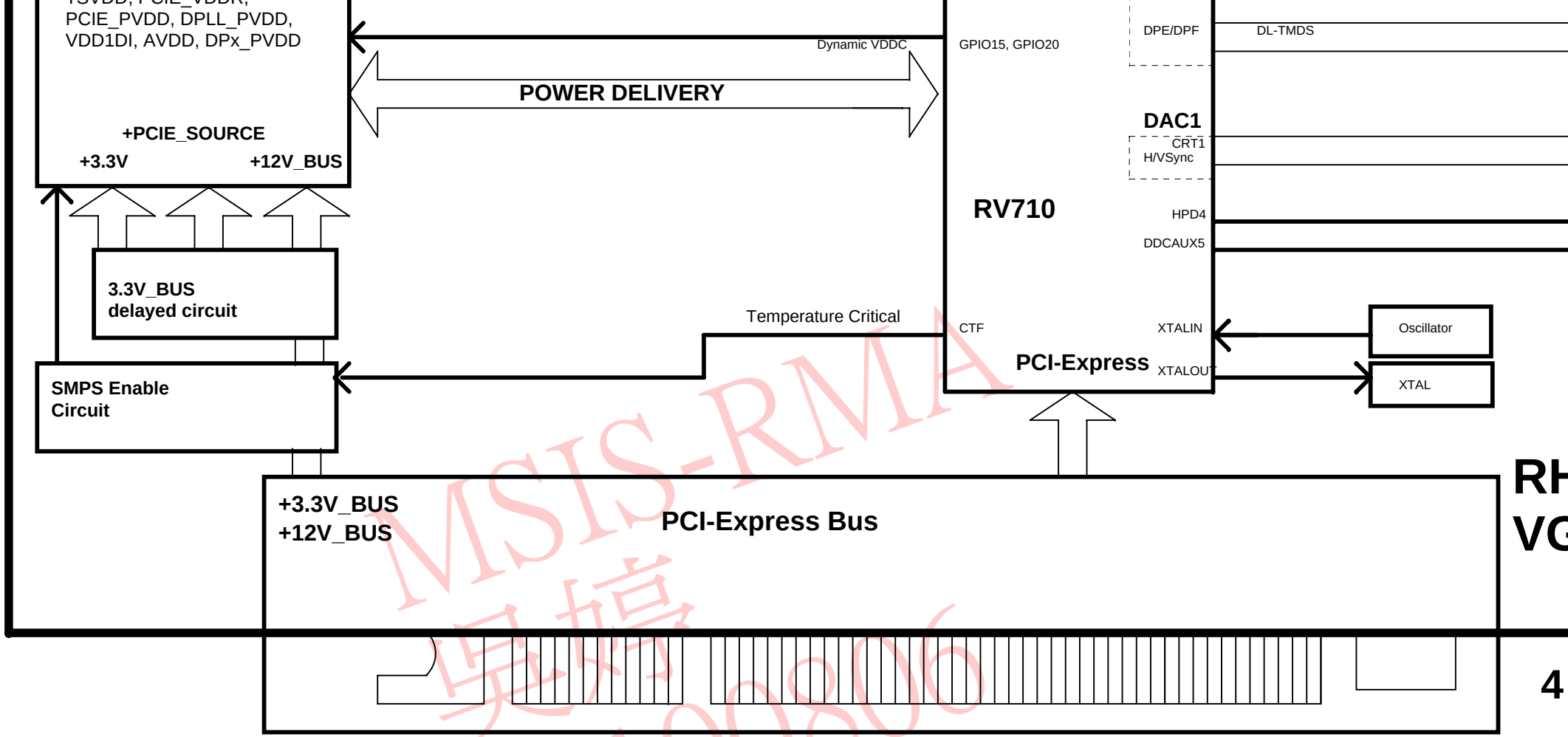
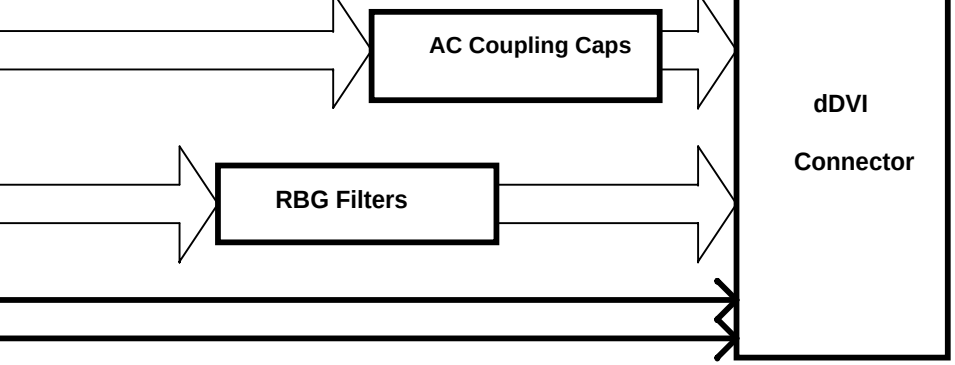

MEMORY CHANNEL A
DDR2 4pcs 64Mx16 (4x128MB)
POWER REGULATORS
From +12V
+VDDC, VDDCI,
SPV10, +MVDD
From +12V LINEAR:
+5V, +5V_VESA,
From +12V DIRECT:
FAN
From +MVDD Linear (1.1V):
PCIE_VDDC, DPLL_VDDC,
DPx_VDD10
From +3.3V Direct:
VDDR3,
From 3.3V Linear (1.8V)
VDDR4, VDDR5, VDD_CT,
TSVDD, PCIE_VDDR,
RANK0
RANK1
Debug Connector
CrossFire Interlink Header
CrossFire
DVOCLK
DVPCNTL_[0..2]
DVPDATA[23:0]
DVP_MVP_CNTL[1:0]
GPIO[2:1]
GENERICB, C, D
Straps
GPIO
BIOS
ROM
Thermal
FAN
Speed control & temperature sense
INTERRUPT
Temp. Sensing
Built-in PWM
GPIO17, GPIO6
D+/D-
TS_FDO
DAC2
CRT2
H/VSync
DDC1
TMDP
CRT1
H/VSync
HPD1
DDC2
DDCAUX7
LVTMDP
Resistor Option
By default, DDC1 is conn



onnected to the VGA header.





H PCIE RV710 DDR3
GA(header) + TVO + DVI

REV 1

4 Layer PCB

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Title	Schematic No.	Date:
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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 0

Sch Rev	PCB Rev	Date	RV710 ENGINEERING BOARD REVISION DESCRIPTION
01	00A	2008.04.02	INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.