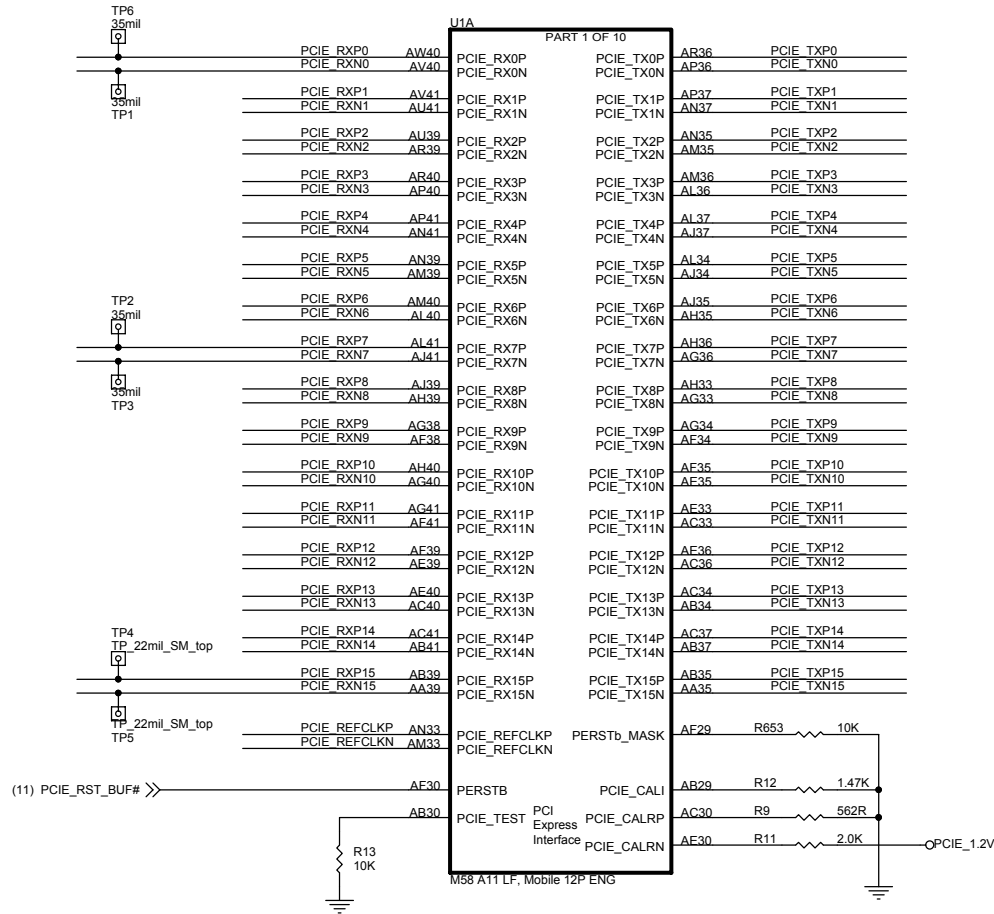


(11) PCIE\_REFCLKP << PCIE\_REFCLKP  
 (11) PCIE\_REFCLKN << PCIE\_REFCLKN

(11) PCIE\_RXP[15..0] << PCIE\_RXP[15..0]  
 (11) PCIE\_RXN[15..0] << PCIE\_RXN[15..0]  
 (11) PCIE\_TXP[15..0] << PCIE\_TXP[15..0]  
 (11) PCIE\_TXN[15..0] << PCIE\_TXN[15..0]



<Variant Name>



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Title		DELL "GREENLAND" M58P 512MB DDR3	
Size	B	Document Number	105-A70531-00A
Date:	Wednesday, October 05, 2005	Sheet	1 of 14
		Rev	0



(6) RASA0# >>> RASA0#  
(6) RASA1# >>> RASA1#  
(6) CASA0# >>> CASA0#  
(6) CASA1# >>> CASA1#  
(6) WEA0# >>> WEA0#  
(6) WEA1# >>> WEA1#  
(6) CSA0# >>> CSA0#  
(6) CSA1# >>> CSA1#  
(6) CKEA0 >>> CKEA0  
(6) CKEA1 >>> CKEA1  
(6) CLKA0 >>> CLKA0  
(6) CLKA0# >>> CLKA0#  
(6) CLKA1 >>> CLKA1  
(6) CLKA1# >>> CLKA1#  
(6) WDQSA[7..0] >>> WDQSA[7..0]  
(6) RDQSA[7..0] >>> RDQSA[7..0]  
(6) DQMA#[7..0] <<< DQMA#[7..0]  
(6) MDA[63..0] <<< MDA[63..0]  
(6) MAA[15..0] <<< MAA[15..0]

MDA0 Y37 DQA\_0  
MDA1 Y36 DQA\_1  
MDA2 Y34 DQA\_2  
MDA3 W36 DQA\_3  
MDA4 U34 DQA\_4  
MDA5 T35 DQA\_5  
MDA6 T37 DQA\_6  
MDA7 T34 DQA\_7  
MDA8 Y32 DQA\_8  
MDA9 Y31 DQA\_9  
MDA10 W32 DQA\_10  
MDA11 W30 DQA\_11  
MDA12 U33 DQA\_12  
MDA13 T32 DQA\_13  
MDA14 T31 DQA\_14  
MDA15 R30 DQA\_15  
MDA16 R36 DQA\_16  
MDA17 R35 DQA\_17  
MDA18 P37 DQA\_18  
MDA19 P36 DQA\_19  
MDA20 N35 DQA\_20  
MDA21 N34 DQA\_21  
MDA22 L35 DQA\_22  
MDA23 K34 DQA\_23  
MDA24 R33 DQA\_24  
MDA25 R32 DQA\_25  
MDA26 P33 DQA\_26  
MDA27 P30 DQA\_27  
MDA28 L33 DQA\_28  
MDA29 L35 DQA\_29  
MDA30 K33 DQA\_30  
MDA31 K31 DQA\_31  
MDA32 K37 DQA\_32  
MDA33 K36 DQA\_33  
MDA34 J37 DQA\_34  
MDA35 J36 DQA\_35  
MDA36 C36 DQA\_36  
MDA37 H35 DQA\_37  
MDA38 F35 DQA\_38  
MDA39 F34 DQA\_39  
MDA40 A39 DQA\_40  
MDA41 B39 DQA\_41  
MDA42 C38 DQA\_42  
MDA43 A38 DQA\_43  
MDA44 C37 DQA\_44  
MDA45 D37 DQA\_45  
MDA46 R35 DQA\_46  
MDA47 C35 DQA\_47  
MDA48 G34 DQA\_48  
MDA49 J34 DQA\_49  
MDA50 F33 DQA\_50  
MDA51 C33 DQA\_51  
MDA52 H32 DQA\_52  
MDA53 J32 DQA\_53  
MDA54 G31 DQA\_54  
MDA55 H31 DQA\_55  
MDA56 D34 DQA\_56  
MDA57 C33 DQA\_57  
MDA58 B34 DQA\_58  
MDA59 A34 DQA\_59  
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MDA61 F32 DQA\_61  
MDA62 B31 DQA\_62  
MDA63 D31 DQA\_63

U1C

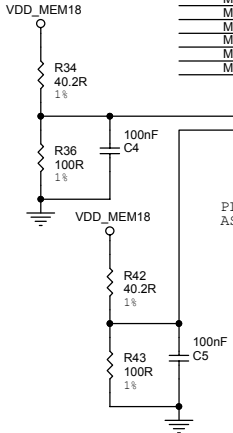
Part 3 of 10

Memory Channel A

MAA\_0 H39 MAA0  
MAA\_1 J40 MAA1  
MAA\_2 H41 MAA2  
MAA\_3 H38 MAA3  
MAA\_4 R39 MAA4  
MAA\_5 P39 MAA5  
MAA\_6 M41 MAA6  
MAA\_7 P40 MAA7  
MAA\_8 N40 MAA8  
MAA\_9 N38 MAA9  
MAA\_10 K39 MAA10  
MAA\_11 K40 MAA11  
MAA\_12 L41 MAA12  
MAA\_13 L39 MAA13  
MAA\_14 L38 MAA14  
MAA\_15 J38 MAA15  
DQMAb\_0 W35 DQMA#0  
DQMAb\_1 W33 DQMA#1  
DQMAb\_2 P34 DQMA#2  
DQMAb\_3 M31 DQMA#3  
DQMAb\_4 D38 DQMA#4  
DQMAb\_5 J33 DQMA#5  
DQMAb\_6 D33 DQMA#6  
DQMAb\_7 J36 WDQSA0  
QSA\_0B J30 WDQSA1  
QSA\_1B L36 WDQSA2  
QSA\_2B N32 WDQSA3  
QSA\_3B E37 WDQSA4  
QSA\_4B B38 WDQSA5  
QSA\_5B E31 WDQSA6  
QSA\_6B A33 WDQSA7  
QSA\_7B J37 RDQSA0  
QSA\_0 J31 RDQSA1  
QSA\_1 N37 RDQSA2  
QSA\_2 P31 RDQSA3  
QSA\_3 G37 RDQSA4  
QSA\_4 A37 RDQSA5  
QSA\_5 F32 RDQSA6  
QSA\_6 C32 RDQSA7  
RASA0b J40 RASA0#  
RASA1b D39 RASA1#  
CASA0b J39 CASA0#  
CASA1b C40 CASA1#  
WEA0b W41 WEA0#  
WEA1b E38 WEA1#  
CSA0b\_0 Y40 CSA0#  
CSA0b\_1 Y41 CSA1#  
CSA1b\_0 E40 CSA1#  
CSA1b\_1 E41 CSA1#  
CKEA0 W39 CKEA0  
CKEA1 D41 CKEA1  
CLKA0 R38 CLKA0#  
CLKA0b T38 CLKA0#  
CLKA1 G39 CLKA1#  
CLKA1b G40 CLKA1#

M58 A11 LF, Mobile 12P ENG

PLACE MVREF DIVIDER COMPONENTS AS CLOSE TO ASIC AS POSSIBLE



(7) RASB0# <<< RASB0#  
(7) RASB1# <<< RASB1#  
(7) CASB0# <<< CASB0#  
(7) CASB1# <<< CASB1#  
(7) WEB0# <<< WEB0#  
(7) WEB1# <<< WEB1#  
(7) CSB0# <<< CSB0#  
(7) CSB1# <<< CSB1#  
(7) CKEB0 <<< CKEB0  
(7) CKEB1 <<< CKEB1  
(7) CLKB0 <<< CLKB0  
(7) CLKB0# <<< CLKB0#  
(7) CLKB1 <<< CLKB1  
(7) CLKB1# <<< CLKB1#  
(7) WDQSB[7..0] <<< WDQSB[7..0]  
(7) RDQSB[7..0] <<< RDQSB[7..0]  
(7) DQMB#[7..0] <<< DQMB#[7..0]  
(7) MDB[63..0] <<< MDB[63..0]  
(7) MAB[15..0] <<< MAB[15..0]

U1D

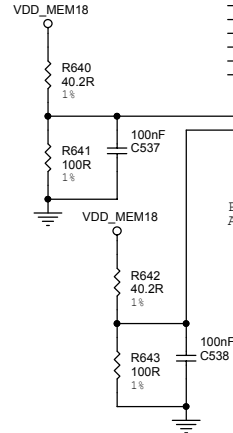
Part 4 of 10

Memory Channel B


MAB\_0 D0B\_0 MAB0  
MAB\_1 D0B\_1 MAB1  
MAB\_2 D0B\_2 MAB2  
MAB\_3 D0B\_3 MAB3  
MAB\_4 D0B\_4 MAB4  
MAB\_5 D0B\_5 MAB5  
MAB\_6 D0B\_6 MAB6  
MAB\_7 D0B\_7 MAB7  
MAB\_8 D0B\_8 MAB8  
MAB\_9 D0B\_9 MAB9  
MAB\_10 D0B\_10 MAB10  
MAB\_11 D0B\_11 MAB11  
MAB\_12 D0B\_12 MAB12  
MAB\_13 D0B\_13 MAB13  
MAB\_14 D0B\_14 MAB14  
MAB\_15 D0B\_15 MAB15  
DQMBb\_0 E28 DQMB#0  
DQMBb\_1 L28 DQMB#1  
DQMBb\_2 E23 DQMB#2  
DQMBb\_3 J22 DQMB#3  
DQMBb\_4 E17 DQMB#4  
DQMBb\_5 K19 DQMB#5  
DQMBb\_6 E11 DQMB#6  
DQMBb\_7 B9 DQMB#7  
QSB\_0B G27 WDQSB0  
QSB\_1B K27 WDQSB1  
QSB\_2B G22 WDQSB2  
QSB\_3B L22 WDQSB3  
QSB\_4B E17 WDQSB4  
QSB\_5B L17 WDQSB5  
QSB\_6B E13 WDQSB6  
QSB\_7B B10 WDQSB7  
E27 RDQSB0  
K26 RDQSB1  
E22 RDQSB2  
K23 RDQSB3  
E16 RDQSB4  
L17 RDQSB5  
D13 RDQSB6  
A8 RDQSB7  
RASB0b A27 RASB0#  
RASB1b C14 RASB1#  
CASB0b B27 CASB0#  
CASB1b B14 CASB1#  
WEB0b B28 WEB0#  
WEB1b C15 WEB1#  
CSB0b\_0 C29 CSB0#  
CSB0b\_1 A29 CSB1#  
CSB1b\_0 B16 CSB1#  
CSB1b\_1 C17 CSB1#  
CKEB0 C28 CKEB0  
CKEB1 C15 CKEB1  
CLKB0 D22 CLKB0#  
CLKB0b D23 CLKB0#  
CLKB1 D15 CLKB1#  
CLKB1b D16 CLKB1#

M58 A11 LF, Mobile 12P ENG

PLACE MVREF DIVIDER COMPONENTS AS CLOSE TO ASIC AS POSSIBLE



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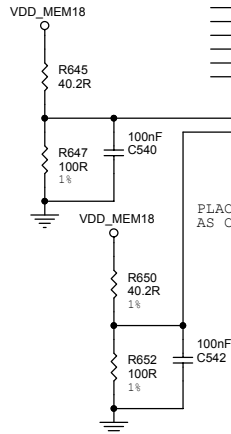
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Size	B	Document Number	105-A70531-00A
Date:	Wednesday, October 05, 2005	Sheet	3 of 14

(8) RASC0# >>> RASC0#  
(8) RASC1# >>> RASC1#  
(8) CASC0# >>> CASC0#  
(8) CASC1# >>> CASC1#  
(8) WEC0# >>> WEC0#  
(8) WEC1# >>> WEC1#  
(8) CSC0# >>> CSC0#  
(8) CSC1# >>> CSC1#  
(6,7,8,9) MEM\_RST >>> MEM\_RST  
(8) CKEC0 >>> CKEC0  
(8) CKEC1 >>> CKEC1  
(8) CLKC0 >>> CLKC0  
(8) CLKC0# >>> CLKC0#  
(8) CLKC1 >>> CLKC1  
(8) CLKC1# >>> CLKC1#  
(8) WQSC[7..0] >>> WQSC[7..0]  
(8) RDQSC[7..0] >>> RDQSC[7..0]  
(8) DQMC#[7..0] >>> DQMC#[7..0]  
(8) MDC[63..0] >>> MDC[63..0]  
(8) MAC[15..0] >>> MAC[15..0]

U1F			
Part 5 of 10			
MDC0 G9	DQC_0	MAC_0	T2 MAC0
MDC1 G6	DQC_1	MAC_1	R3 MAC1
MDC2 G5	DQC_2	MAC_2	R1 MAC2
MDC3 J8	DQC_3	MAC_3	U2 MAC3
MDC4 J5	DQC_4	MAC_4	H1 MAC4
MDC5 K6	DQC_5	MAC_5	K3 MAC5
MDC6 K5	DQC_6	MAC_6	K2 MAC6
MDC7 K5	DQC_7	MAC_7	J2 MAC7
MDC8 H14	DQC_8	MAC_8	L3 MAC8
MDC9 J14	DQC_9	MAC_9	L1 MAC9
MDC10 H13	DQC_10	MAC_10	P3 MAC10
MDC11 J11	DQC_11	MAC_11	P2 MAC11
MDC12 J10	DQC_12	MAC_12	N1 MAC12
MDC13 K9	DQC_13	MAC_13	N2 MAC13
MDC14 K11	DQC_14	MAC_14	B4 MAC14
MDC15 K13	DQC_15	MAC_15	T4 MAC15
MDC16 L13	DQC_16		
MDC17 L14	DQC_17		
MDC18 M14	DQC_18		
MDC19 M15	DQC_19		
MDC20 P11	DQC_20		
MDC21 P12	DQC_21		
MDC22 R10	DQC_22		
MDC23 R12	DQC_23		
MDC24 L7	DQC_24		
MDC25 L6	DQC_25		
MDC26 L9	DQC_26		
MDC27 N8	DQC_27		
MDC28 P5	DQC_28		
MDC29 P5	DQC_29		
MDC30 P9	DQC_30		
MDC31 R7	DQC_31		
MDC32 R6	DQC_32		
MDC33 T7	DQC_33		
MDC34 T8	DQC_34		
MDC35 W8	DQC_35		
MDC36 W7	DQC_36		
MDC37 Y5	DQC_37		
MDC38 Y7	DQC_38		
MDC39 Y7	DQC_39		
MDC40 R9	DQC_40		
MDC41 T10	DQC_41		
MDC42 T11	DQC_42		
MDC43 U12	DQC_43		
MDC44 W10	DQC_44		
MDC45 W12	DQC_45		
MDC46 Y10	DQC_46		
MDC47 Y11	DQC_47		
MDC48 AA9	DQC_48		
MDC49 AA11	DQC_49		
MDC50 AA12	DQC_50		
MDC51 AB12	DQC_51		
MDC52 AC11	DQC_52		
MDC53 AE9	DQC_53		
MDC54 AE11	DQC_54		
MDC55 AE12	DQC_55		
MDC56 Y8	DQC_56		
MDC57 AA5	DQC_57		
MDC58 AA8	DQC_58		
MDC59 AC7	DQC_59		
MDC60 AC7	DQC_60		
MDC61 AC8	DQC_61		
MDC62 AF6	DQC_62		
MDC63 AF8	DQC_63		

M58 A11 LF, Mobile 12P ENG

PLACE MVREF DIVIDER COMPONENTS  
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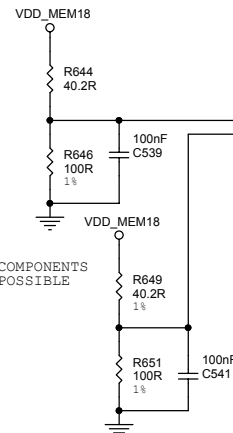


(9) RASD0# >>> RASD0#  
(9) RASD1# >>> RASD1#  
(9) CASD0# >>> CASD0#  
(9) CASD1# >>> CASD1#  
(9) WED0# >>> WED0#  
(9) WED1# >>> WED1#  
(9) CSD0# >>> CSD0#  
(9) CSD1# >>> CSD1#  
(9) CKED0 >>> CKED0  
(9) CKED1 >>> CKED1  
(9) CLKD0 >>> CLKD0  
(9) CLKD0# >>> CLKD0#  
(9) CLKD1 >>> CLKD1  
(9) CLKD1# >>> CLKD1#  
(9) WQSD[7..0] >>> WQSD[7..0]  
(9) RDQSD[7..0] >>> RDQSD[7..0]  
(9) DQMD#[7..0] >>> DQMD#[7..0]  
(9) MDD[63..0] >>> MDD[63..0]  
(9) MAD[15..0] >>> MAD[15..0]

U1F			
Part 6 of 10			
MDD0 AA3	DQD_0	MAD_0	AW8 MAD0
MDD1 AB1	DQD_1	MAD_1	AY7 MAD1
MDD2 AB3	DQD_2	MAD_2	AV8 MAD2
MDD3 AB4	DQD_3	MAD_3	BA8 MAD3
MDD4 AE3	DQD_4	MAD_4	AV3 MAD4
MDD5 AE1	DQD_5	MAD_5	AY3 MAD5
MDD6 AE1	DQD_6	MAD_6	AW2 MAD6
MDD7 AE4	DQD_7	MAD_7	AV5 MAD7
MDD8 AG1	DQD_8	MAD_8	AW4 MAD8
MDD9 AG2	DQD_9	MAD_9	AW7 MAD9
MDD10 AH2	DQD_10	MAD_10	BA5 MAD10
MDD11 AH3	DQD_11	MAD_11	BA4 MAD11
MDD12 AI4	DQD_12	MAD_12	AY5 MAD12
MDD13 AI4	DQD_13	MAD_13	AI10 MAD13
MDD14 AM2	DQD_14	MAD_14	AI9 MAD14
MDD15 AM2	DQD_15	MAD_15	AI9 MAD15
MDD16 AE5	DQD_16		
MDD17 AE6	DQD_17		
MDD18 AF7	DQD_18		
MDD19 AG8	DQD_19		
MDD20 AH8	DQD_20		
MDD21 AH8	DQD_21		
MDD22 AI8	DQD_22		
MDD23 AI7	DQD_23		
MDD24 AE9	DQD_24		
MDD25 AF10	DQD_25		
MDD26 AG10	DQD_26		
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MDD33 AR3	DQD_33		
MDD34 AN4	DQD_34		
MDD35 AP4	DQD_35		
MDD36 AL5	DQD_36		
MDD37 AM6	DQD_37		
MDD38 AN6	DQD_38		
MDD39 AR6	DQD_39		
MDD40 AI7	DQD_40		
MDD41 AL8	DQD_41		
MDD42 AN7	DQD_42		
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MDD45 AN10	DQD_45		
MDD46 AP10	DQD_46		
MDD47 AT10	DQD_47		
MDD48 AR11	DQD_48		
MDD49 AM11	DQD_49		
MDD50 AN11	DQD_50		
MDD51 AM13	DQD_51		
MDD52 AI14	DQD_52		
MDD53 AK14	DQD_53		
MDD54 AM15	DQD_54		
MDD55 AK15	DQD_55		
MDD56 AT11	DQD_56		
MDD57 AV11	DQD_57		
MDD58 AR13	DQD_58		
MDD59 AU13	DQD_59		
MDD60 AT14	DQD_60		
MDD61 AU14	DQD_61		
MDD62 AW14	DQD_62		
MDD63 AY14	DQD_63		

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MVREFS\_3  
MEMTEST  
TEST\_YCLK  
DRAM\_RST  
TEST\_MCLK

M58 A11 LF, Mobile 12P ENG



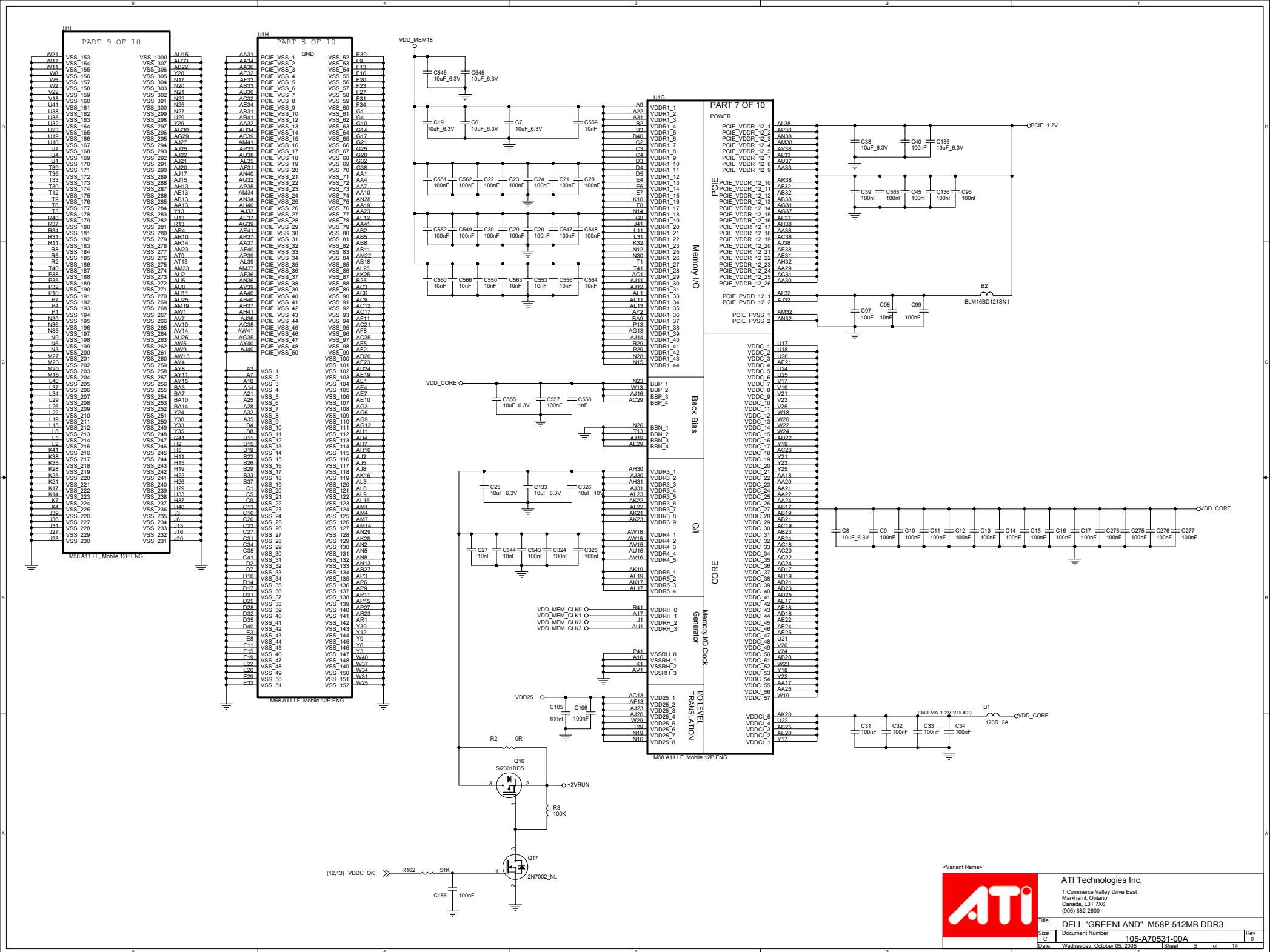
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AS CLOSE TO ASIC AS POSSIBLE

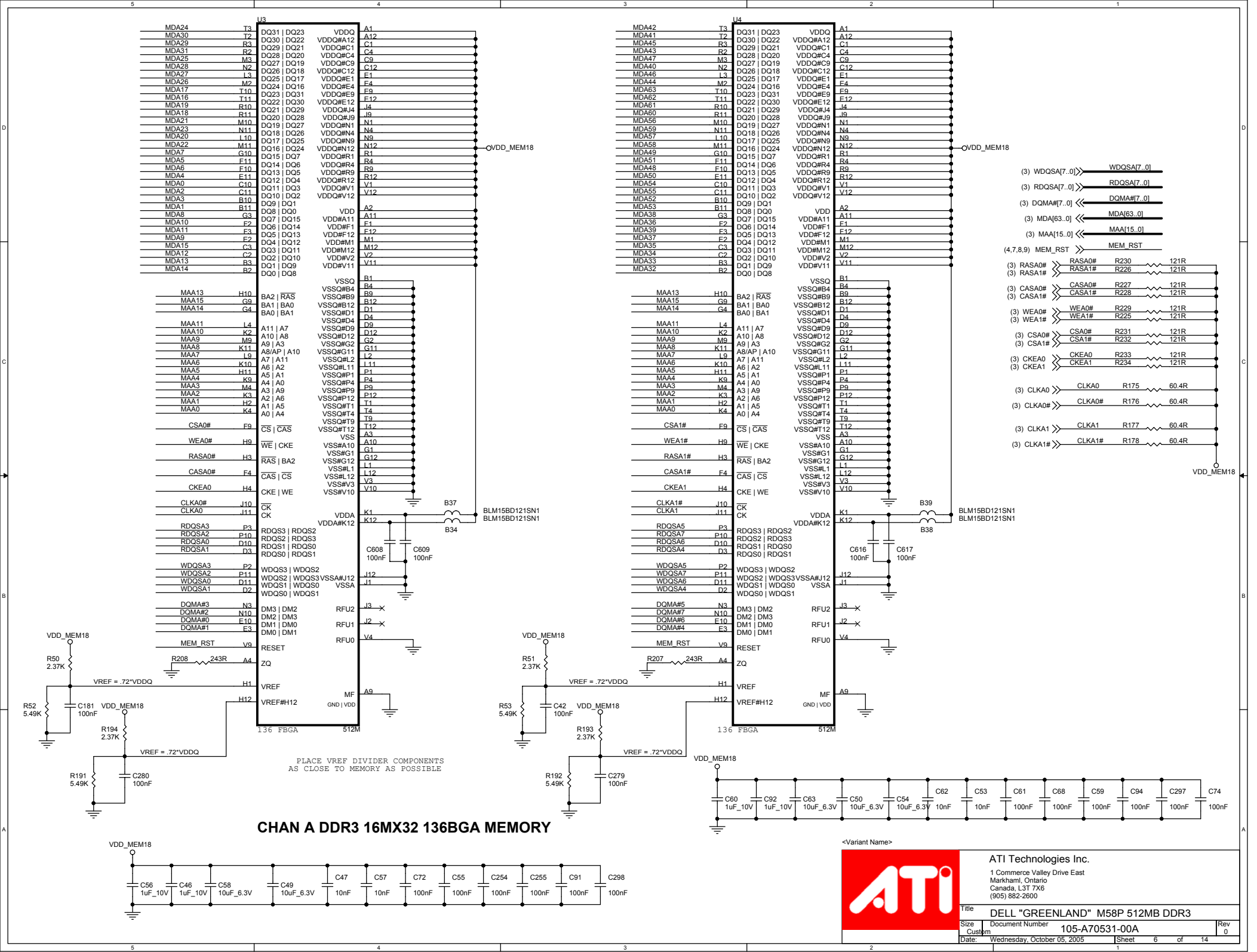


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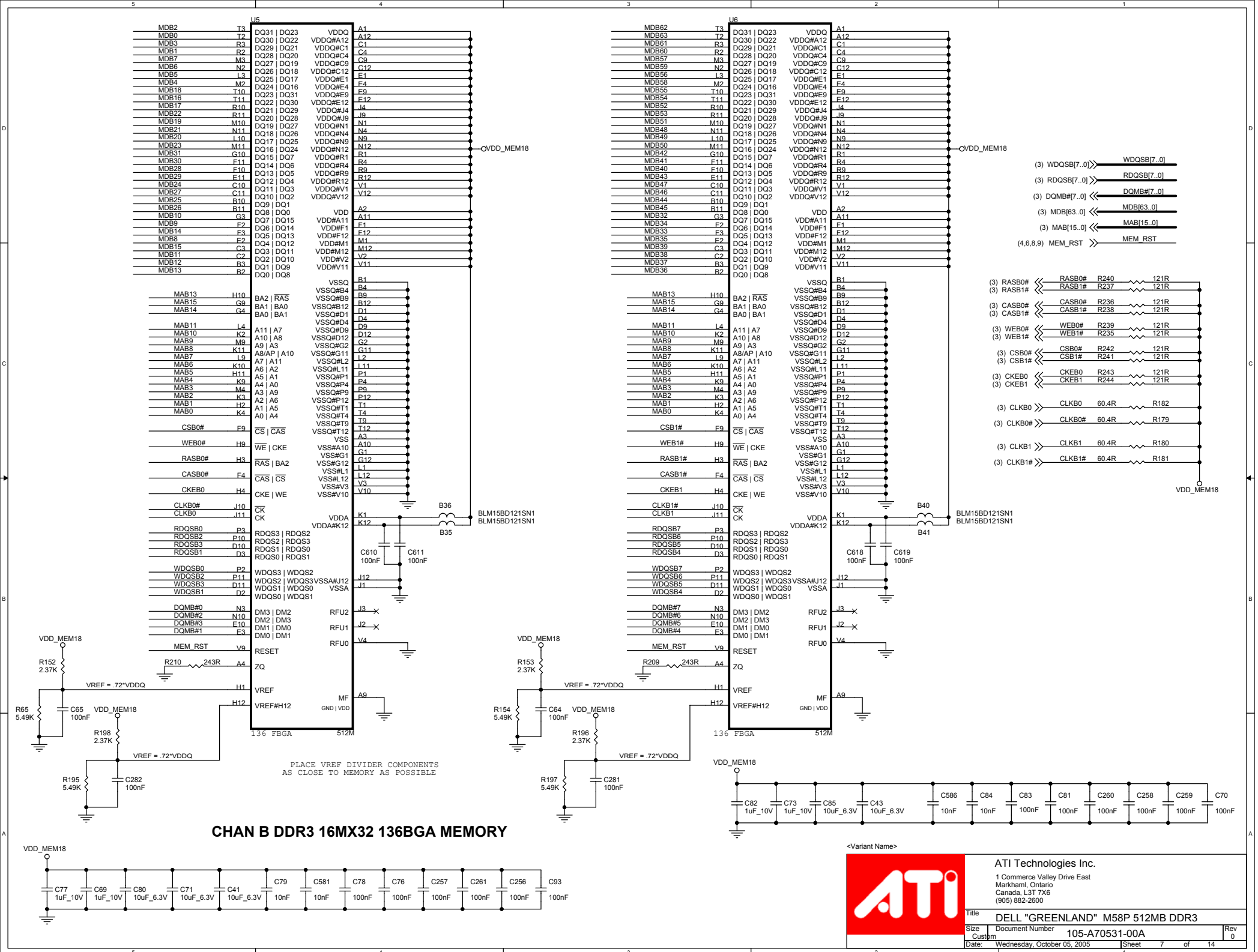
1 Commerce Valley Drive East  
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Canada, L3T 7X6  
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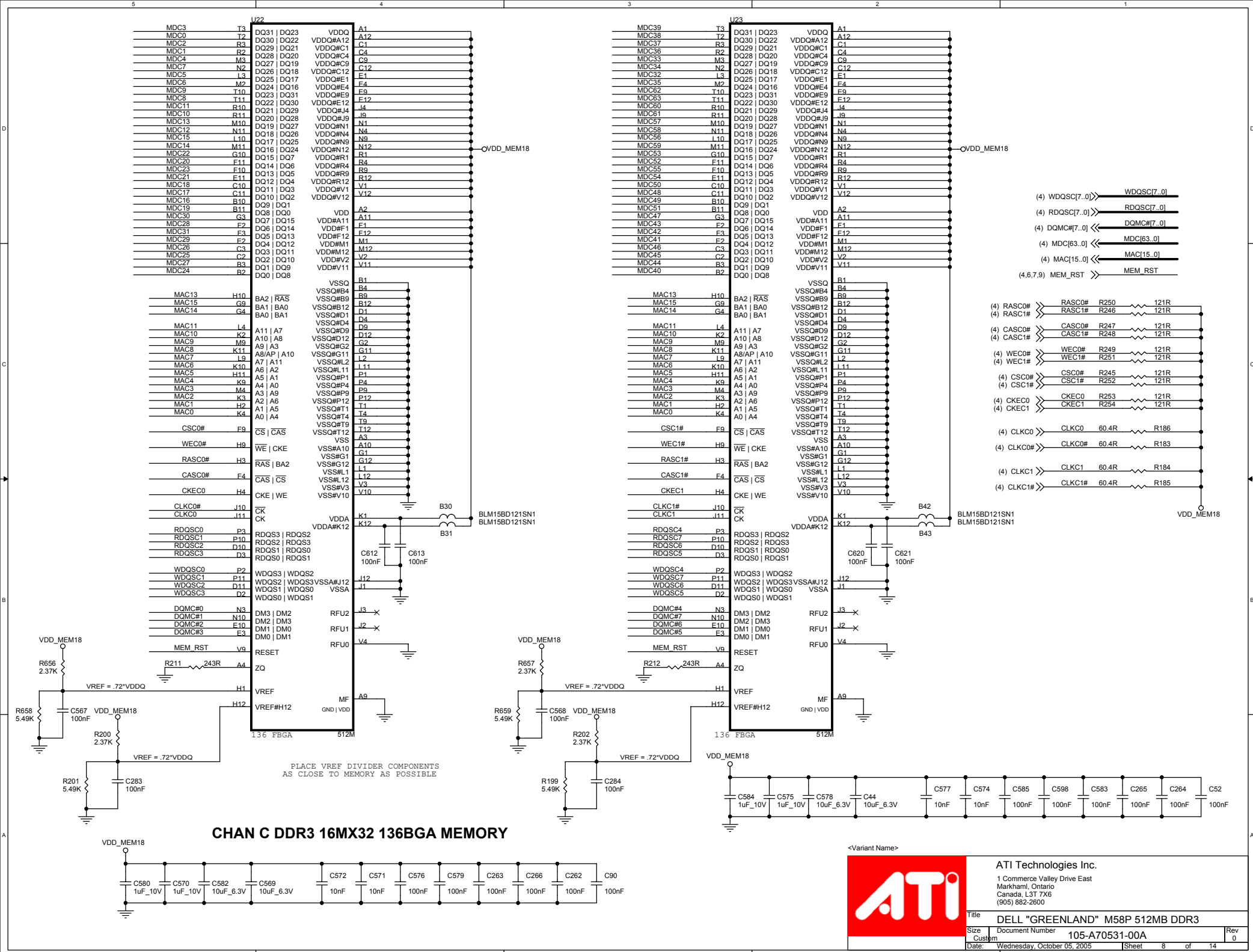
Title		DELL "GREENLAND" M58P 512MB DDR3	
Size	Document Number	105-A70531-00A	Rev 0
B	Date:	Wednesday, October 05, 2005	Sheet 4 of 14



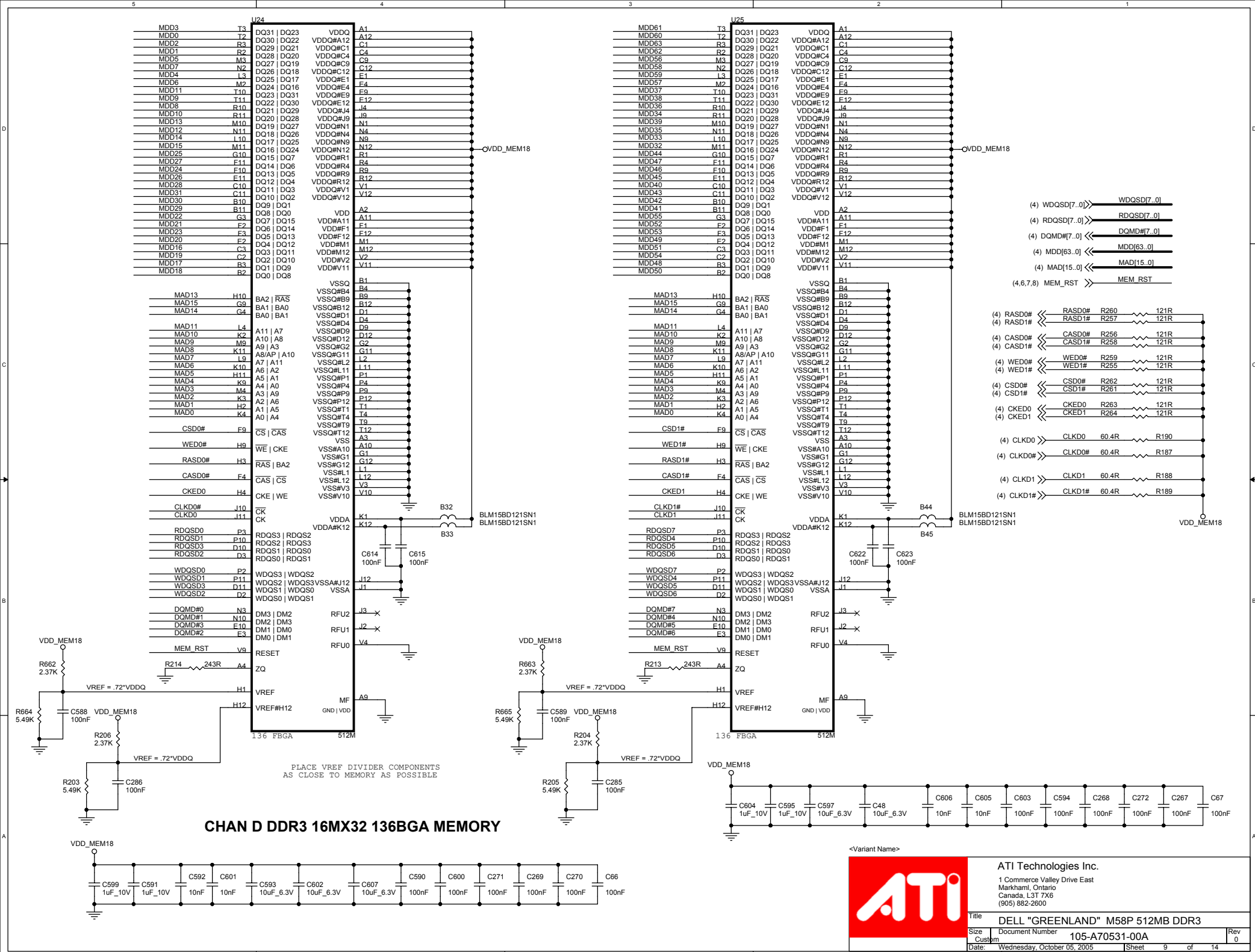












(2) YPrPb\_DET << YPrPb\_DET

(2) TV\_Y << TV\_Y

(2) TV\_C << TV\_C

(2) TV\_CVBS << TV\_CVBS

(2) VGA\_RED << VGA\_RED

(2) VGA\_GRN << VGA\_GRN

(2) VGA\_BLU << VGA\_BLU

(2) HSYNC << HSYNC

(2,15) VSYNC << VSYNC

(1) PCIE\_REFCLKP << PCIE\_REFCLKP

(1) PCIE\_REFCLKN << PCIE\_REFCLKN

(1) PCIE\_RXP[15..0] << PCIE\_RXP[15..0]

(1) PCIE\_RXN[15..0] << PCIE\_RXN[15..0]

(1) PCIE\_TXP[15..0] << PCIE\_TXP[15..0]

(1) PCIE\_TXN[15..0] << PCIE\_TXN[15..0]

(14,15) PBAT\_SMBCLK << PBAT\_SMBCLK

(14,15) PBAT\_SMBDAT << PBAT\_SMBDAT

(15) OTEMP# << OTEMP#

(12) RUNPWROK << RUNPWROK

(2) DVI\_TX0 << DVI\_TX0

(2) DVI\_TX0+ << DVI\_TX0+

(2) DVI\_TX1 << DVI\_TX1

(2) DVI\_TX1+ << DVI\_TX1+

(2) DVI\_TX2 << DVI\_TX2

(2) DVI\_TX2+ << DVI\_TX2+

(2) DVI\_CLK << DVI\_CLK

(2) DVI\_CLK+ << DVI\_CLK+

(2) DVI\_SCLK << DVI\_SCLK

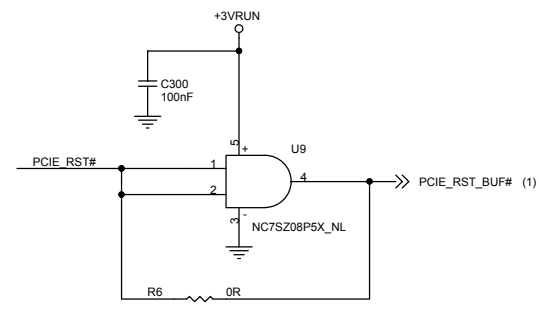
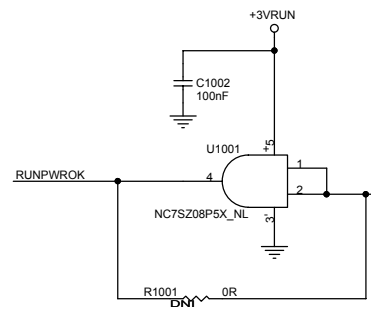
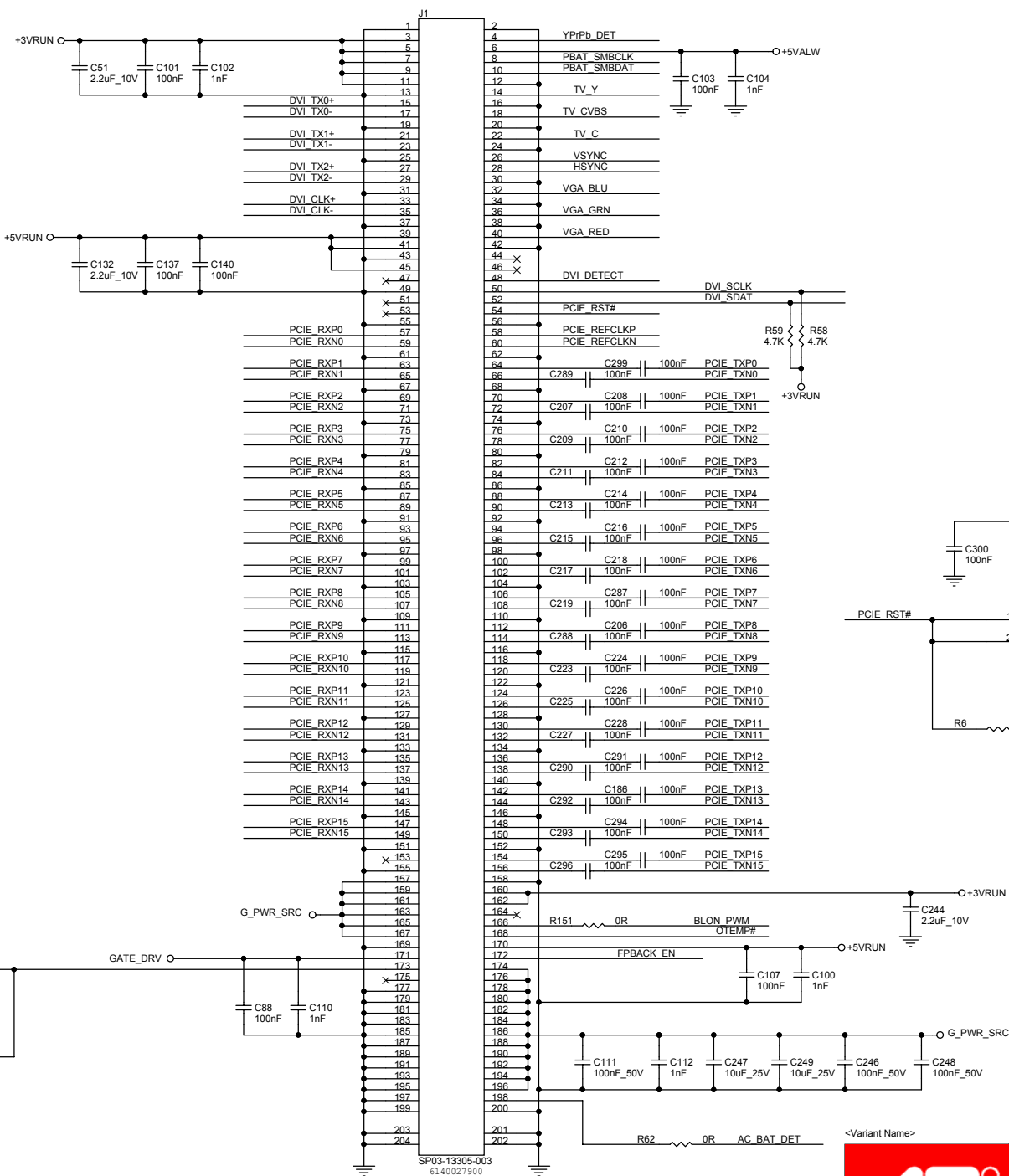
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(2) DVI\_DETECT << DVI\_DETECT

(2,14) BLON\_PWM << BLON\_PWM

(2) AC\_BAT\_DET << AC\_BAT\_DET

(14) FPCBACK\_EN << FPCBACK\_EN



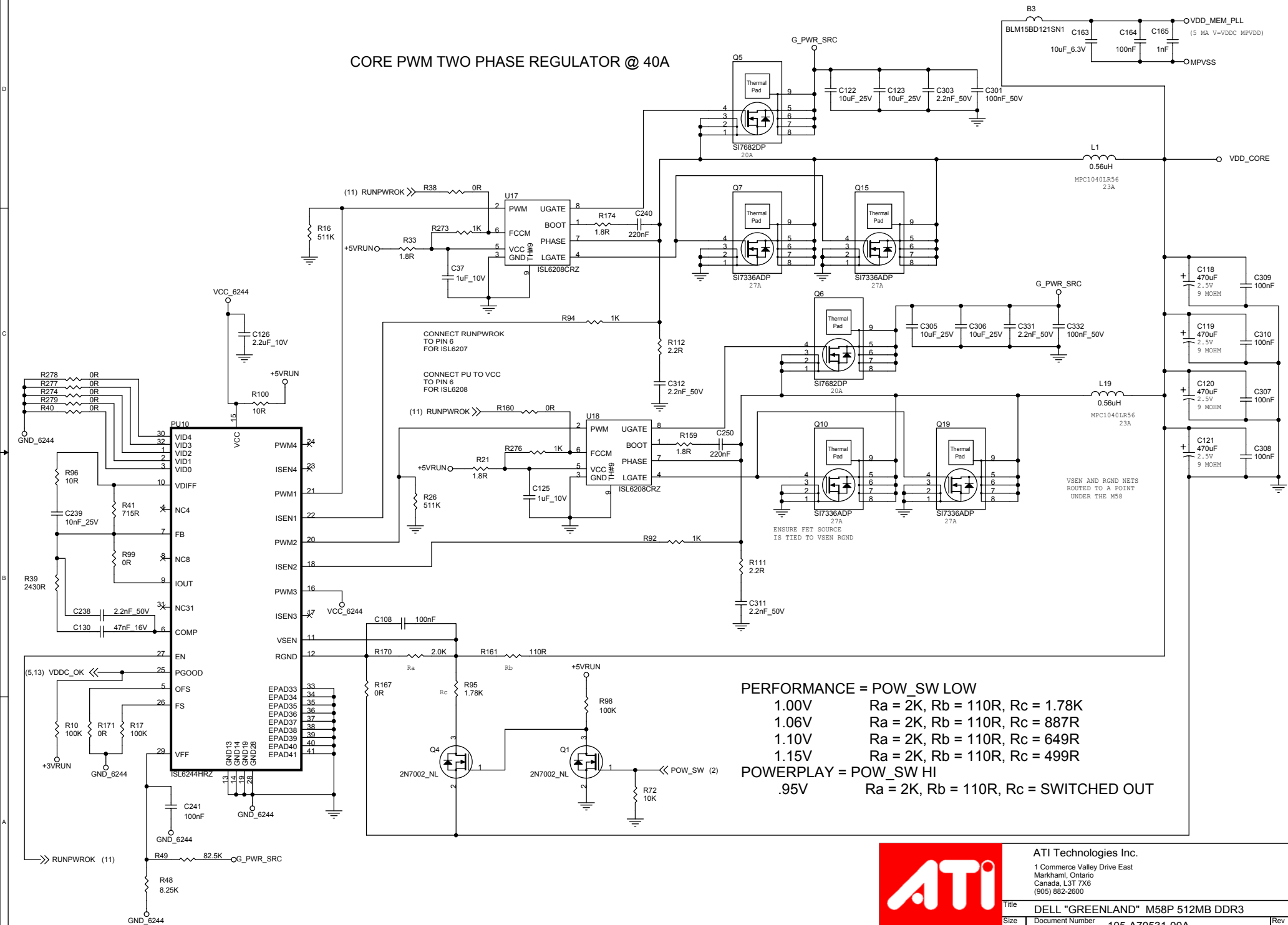
PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE



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Title	DELL "GREENLAND" M58P 512MB DDR3		
Size	Document Number	105-A70531-00A	Rev 0
Date:	Wednesday, October 05, 2005	Sheet 10	of 14

## CORE PWM TWO PHASE REGULATOR @ 40A



PERFORMANCE = POW\_SW LOW

1.00V       $R_a = 2K$ ,  $R_b = 110R$ ,  $R_c = 1.78K$

1.06V      Ra = 2K, Rb = 110R, Rc = 887R

1.10V Ra = 2K, Rb = 110R, Rc = 649R

1.15V Ra = 2K, Rb = 110R, Rc = 499R

POWERPLAY = POW SW HI

.95V      Ra = 2K, Rb = 110R, Rc = SWITCHED OUT



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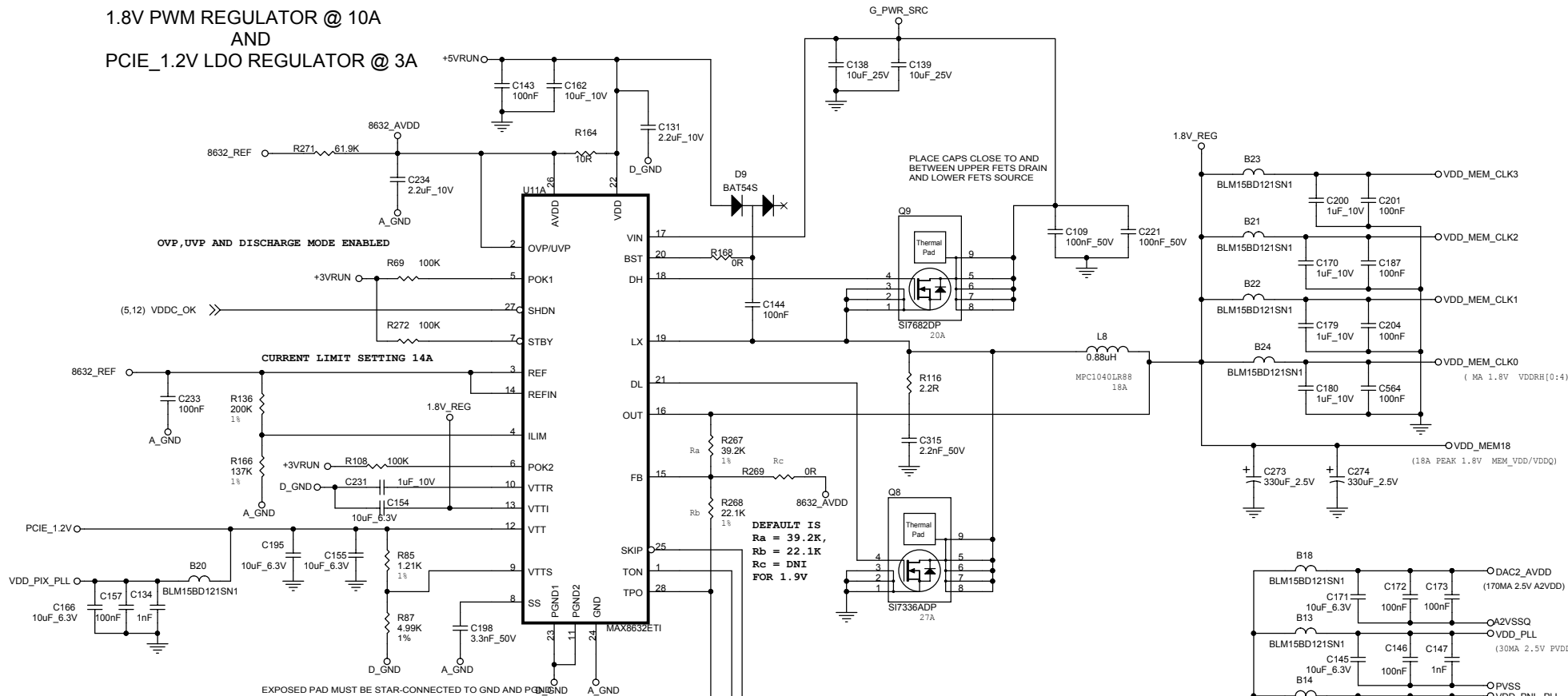
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Title	DELL "GREENLAND" M58P 512MB DDR3
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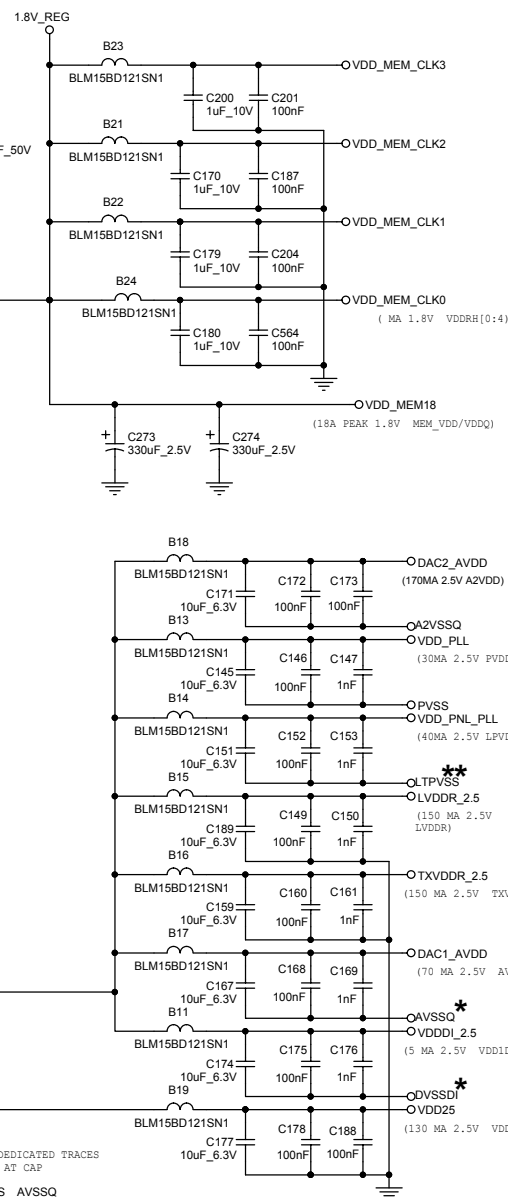
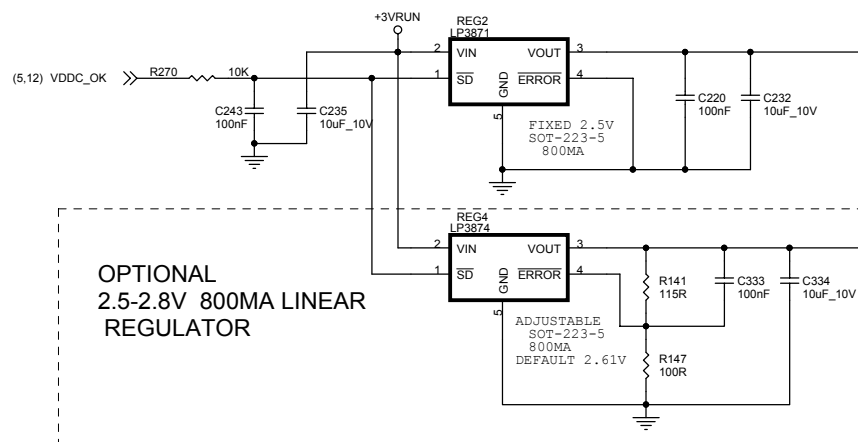
Size	Document Number	105-A70531-00A
Custom		

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# 1.8V PWM REGULATOR @ 10A AND PCIE\_1.2V LDO REGULATOR @ 3A



## 2.5V 800MA LINEAR REGULATOR

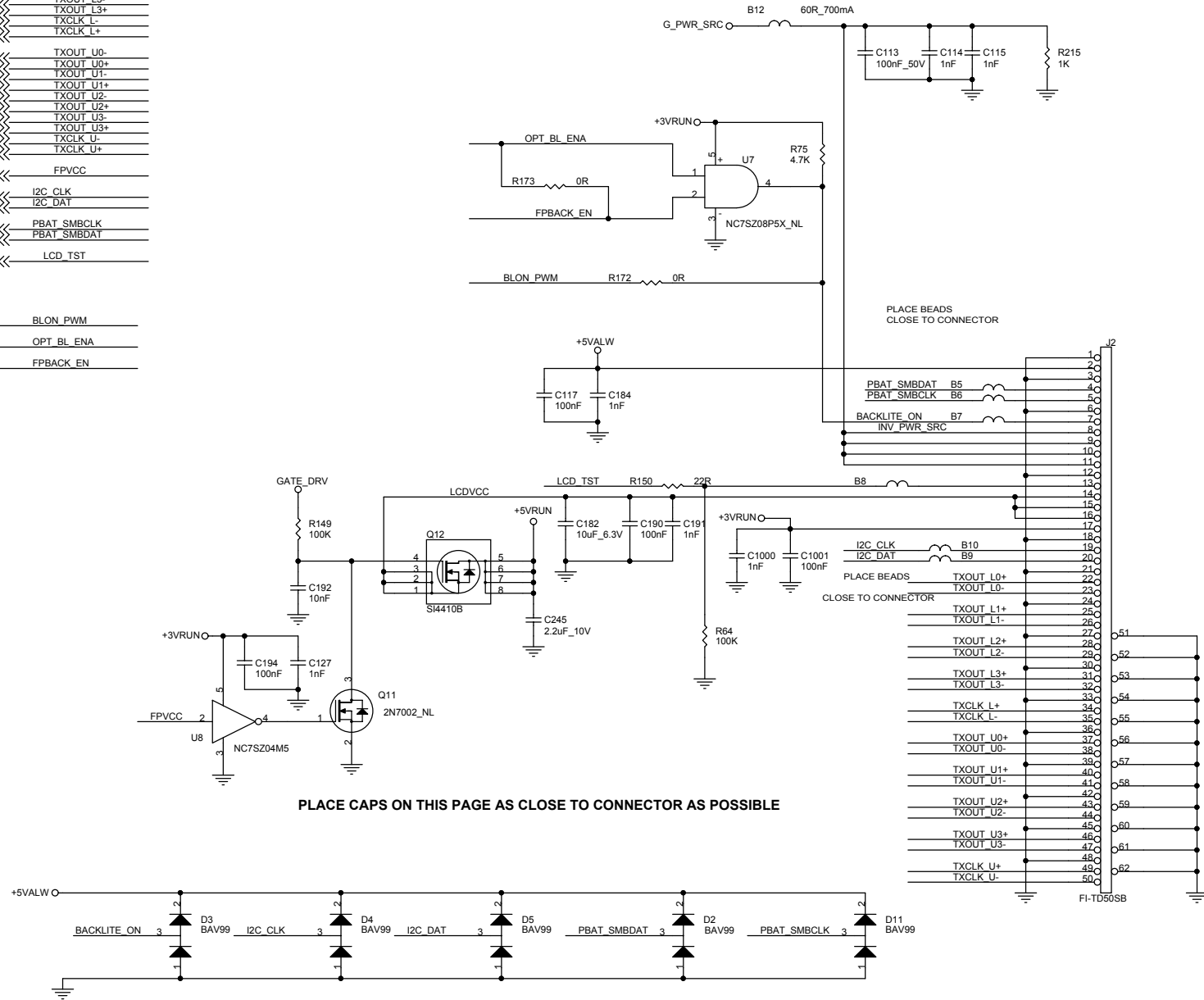


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(2) TXOUT\_L0- << TXOUT\_L0-  
 (2) TXOUT\_L0+ << TXOUT\_L0+  
 (2) TXOUT\_L1- << TXOUT\_L1-  
 (2) TXOUT\_L1+ << TXOUT\_L1+  
 (2) TXOUT\_L2- << TXOUT\_L2-  
 (2) TXOUT\_L2+ << TXOUT\_L2+  
 (2) TXOUT\_L3- << TXOUT\_L3-  
 (2) TXOUT\_L3+ << TXOUT\_L3+  
 (2) TXCLK\_L- << TXCLK\_L-  
 (2) TXCLK\_L+ << TXCLK\_L+  
 (2) TXOUT\_U0- << TXOUT\_U0-  
 (2) TXOUT\_U0+ << TXOUT\_U0+  
 (2) TXOUT\_U1- << TXOUT\_U1-  
 (2) TXOUT\_U1+ << TXOUT\_U1+  
 (2) TXOUT\_U2- << TXOUT\_U2-  
 (2) TXOUT\_U2+ << TXOUT\_U2+  
 (2) TXOUT\_U3- << TXOUT\_U3-  
 (2) TXOUT\_U3+ << TXOUT\_U3+  
 (2) TXCLK\_U- << TXCLK\_U-  
 (2) TXCLK\_U+ << TXCLK\_U+  
 (2) FPVCC << FPVCC  
 (2) I2C\_CLK << I2C\_CLK  
 (2) I2C\_DAT << I2C\_DAT  
 (11,15) PBAT\_SMBCLK << PBAT\_SMBCLK  
 (11,15) PBAT\_SMBDAT << PBAT\_SMBDAT  
 (2) LCD\_TST << LCD\_TST

(2,11) BLON\_PWM << BLON\_PWM  
 (2) OPT\_BL\_ENA << OPT\_BL\_ENA  
 (11) FBACK\_EN << FBACK\_EN



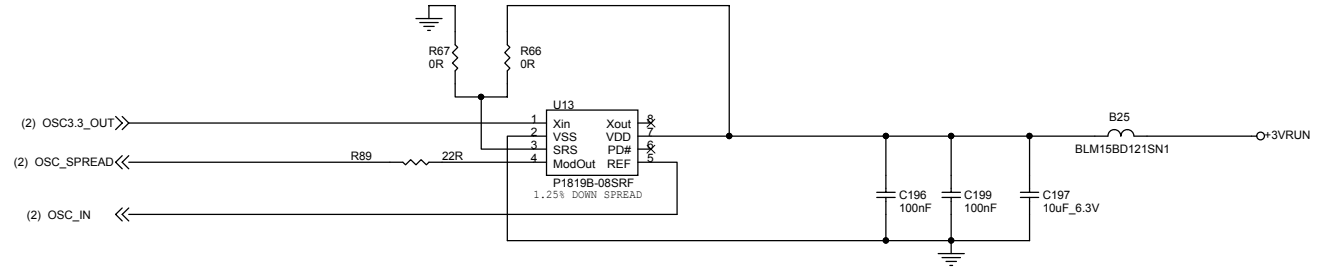
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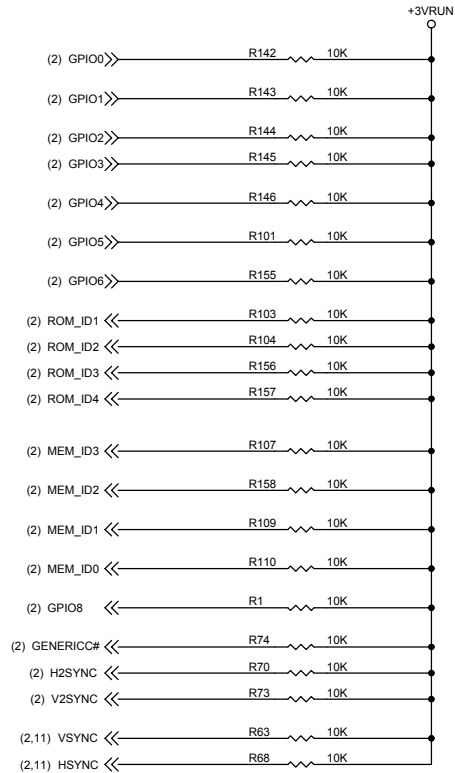
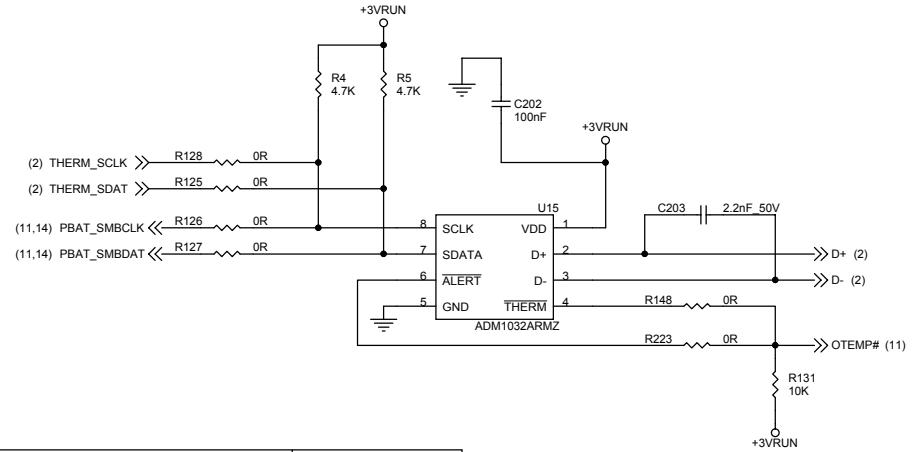
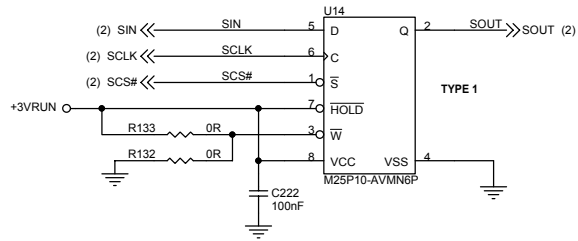
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Title	DELL "GREENLAND" M58P 512MB DDR3		
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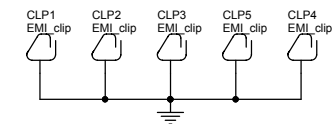
# MEMORY CLOCK SPREAD SPECTRUM



## FLASH ROM



STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
TX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
TX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE - TX DE-EMPHASIS DISABLED FOR MOBILE	INSTALL 10K RESISTOR
PCIE_MISC0/1	GPIO(3,2)	PCIE MISCELLANEOUS MODES - HALT IMPEDENCE CALCULATION BEFORE TX ENABLED AND ENABLE RX DETECT	DO NOT INSTALL 10K RESISTORS
DEBUG_ACCESS	GPIO4	- NORMAL MODE	DO NOT INSTALL 10K RESISTOR
PLL_BIAS_RD	GPIO(6,5)	REDUCE MIRROR BIAS SETTING FOR PHY PLL	01
ROMIDCFG(3:0)	ROMID (4:1)	SERIAL FLASH ROM TYPE SELECT - SERIAL M25P10 ROM	1011
MEM_TYPE	MEMID (3:0)	MEMORY TYPE AND SPEED SELECT - SAMSUNG GDDR3 256MB 8MX32	TBD
FORCE COMPLIANCE	GPIO8	DO NOT FORCE COMPLIANCE STATE QUICKLY	DO NOT INSTALL 10K RESISTOR
ATI FEATURE II	GENERICC H2SYNC V2SYNC	SET TO 000	DO NOT INSTALL 10K RESISTORS
VIP DEVICE	VSYN	NO SLAVE VIP DEVICE PRESENT AT RESET	INSTALL 10K RESISTOR
ATI FEATURE I	HSYN	SET TO 1	INSTALL 10K RESISTOR



<Variant Name>



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Title	Schematic No.	Date:
DELL "GREENLAND" M58P 512MB DDR3	105-A70531-00A	Wednesday, October 05, 2005

REVISION HISTORY	Rev 0
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Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/09/05	PROTOTYPE DESIGN BASED ON 105-A743-00B WITH FOLLOWING CHANGES: - CHANGE TO NEW LCD CONNECTOR AND PINOUT,ADD 24 BIT - CHANGES TO BOARD TO BOARD PINOUT TO ADD SOME +5VRUN PINS AND REMOVE RGB DDC, AND REMOVE INTERNAL TMDS DVI2
		13/09/05	- REMOVE EXTERNAL TMDS LOGIC AND CONNECT INTEGRATED TMDS - CHANGES TO CORE REGULATOR ISL6244/ISL6207 AND I/O REGULATOR MAX8632 AS PER DELL REVIEWS
		20/09/05	- CORRECT MEMORY U4,U6,U23,U25 CONTROL SIGNALS FOR NON MIRRORRED - ADD OPTIONAL PD/PU FOR NON HDCP/HDCP ON EEPROM WP PIN - ADD PU RESISTOR TO J2 BACKLITE_ON PIN - REMOVE DIODE D6 FROM IO REG LOWER FET Q8 - CHANGE TO ISL6208 SYMBOL
		28/09/05	- PULLUP I/O REG MAX8632 OVP/UEP PIN TO +5VRUN INSTEAD OF +5VALW
		04/10/05	- CORRECT MISSING GROUND ON +3VRUN CAPS AT MODULE CONNECTOR
		05/10/05	- CONNECT PIN 17 TO +3VRUN AT LVDS CONNECTOR AND ADD TWO CAPS