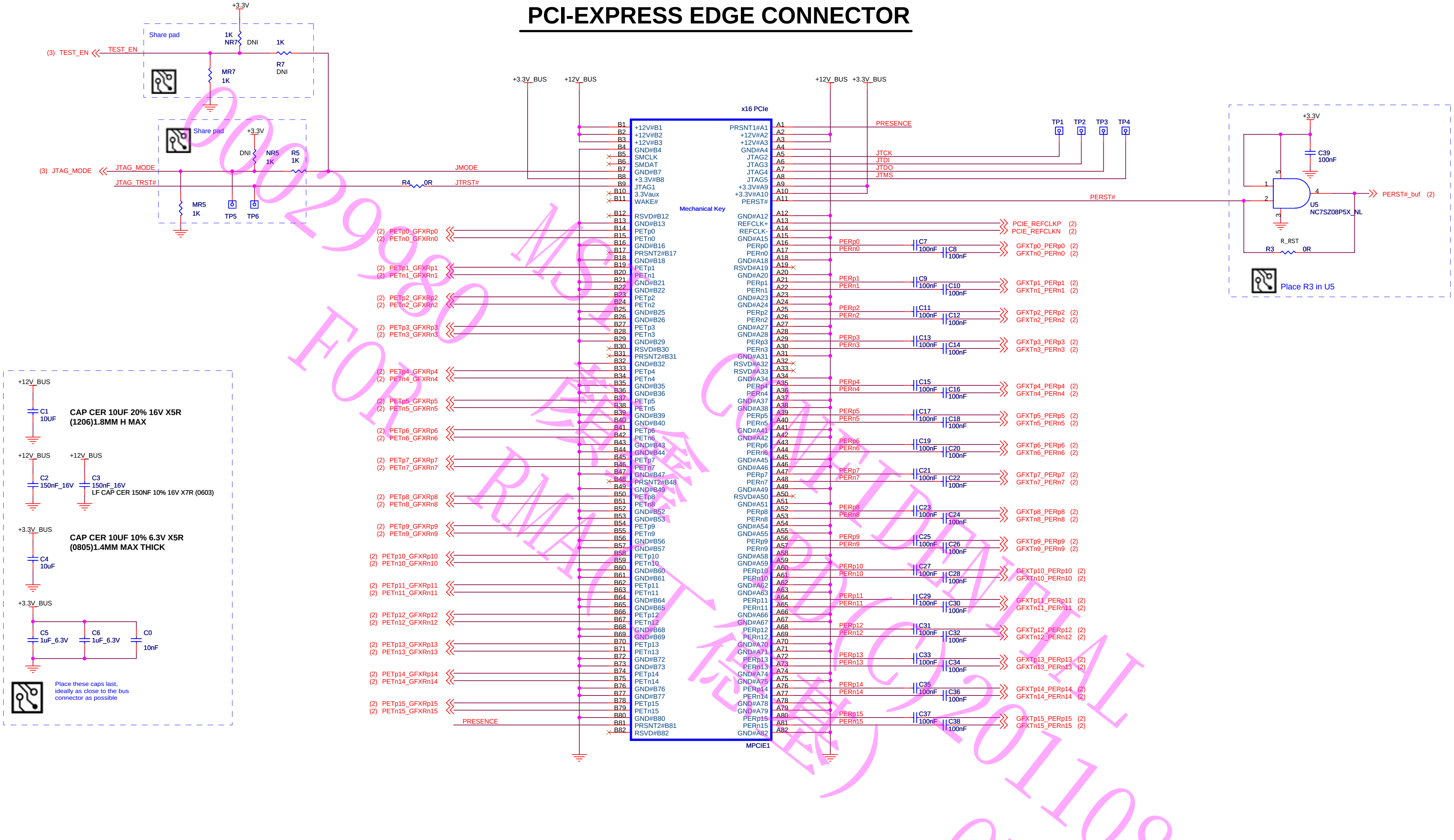
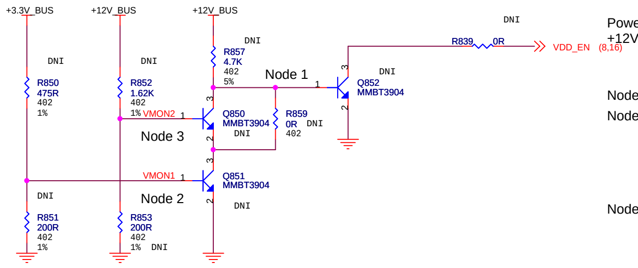
PCI-EXPRESS EDGE CONNECTOR





Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.

Node 1 When +12V_BUS ramps above min Vbe, SMPS_EN will be held low

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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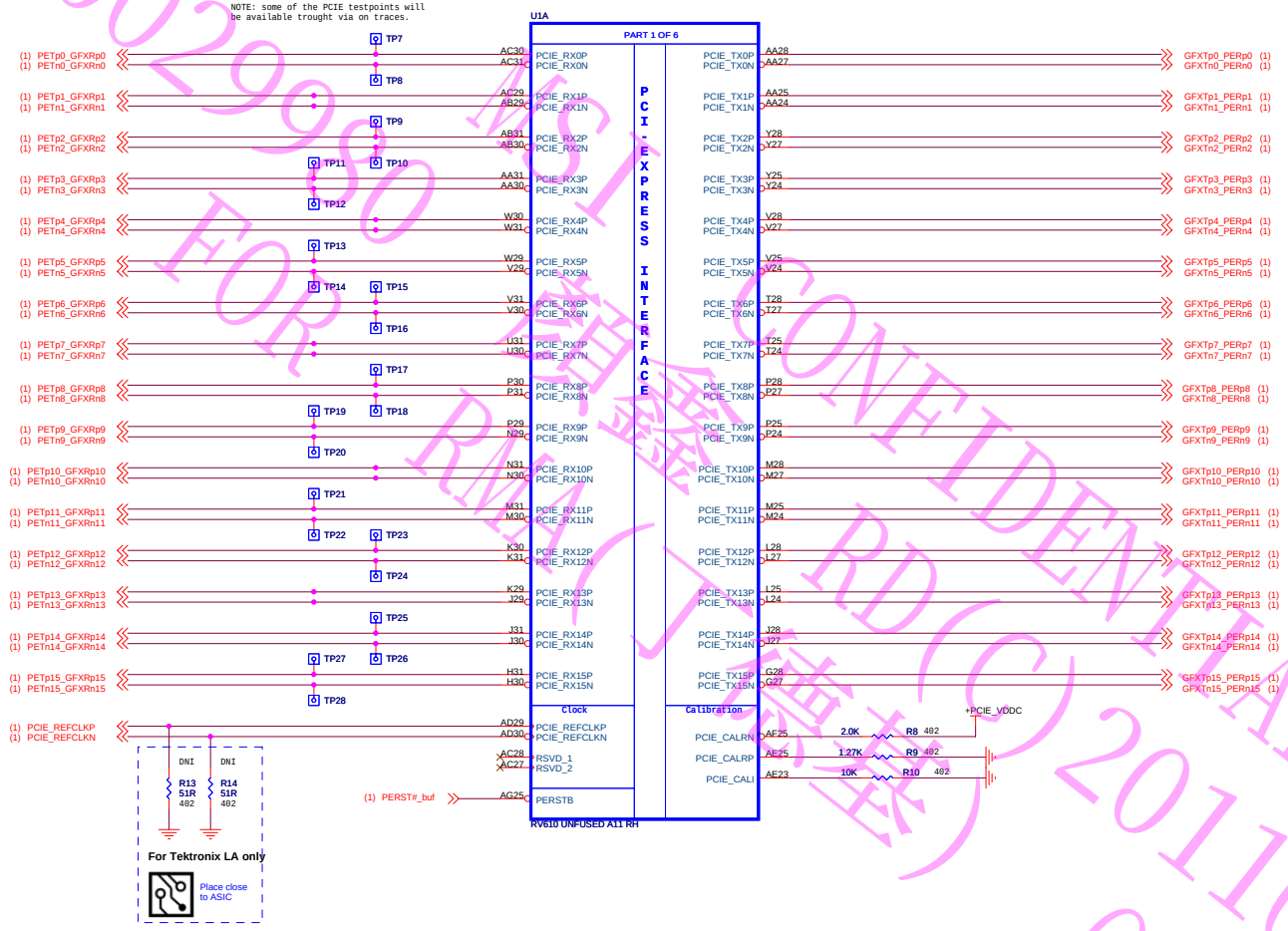

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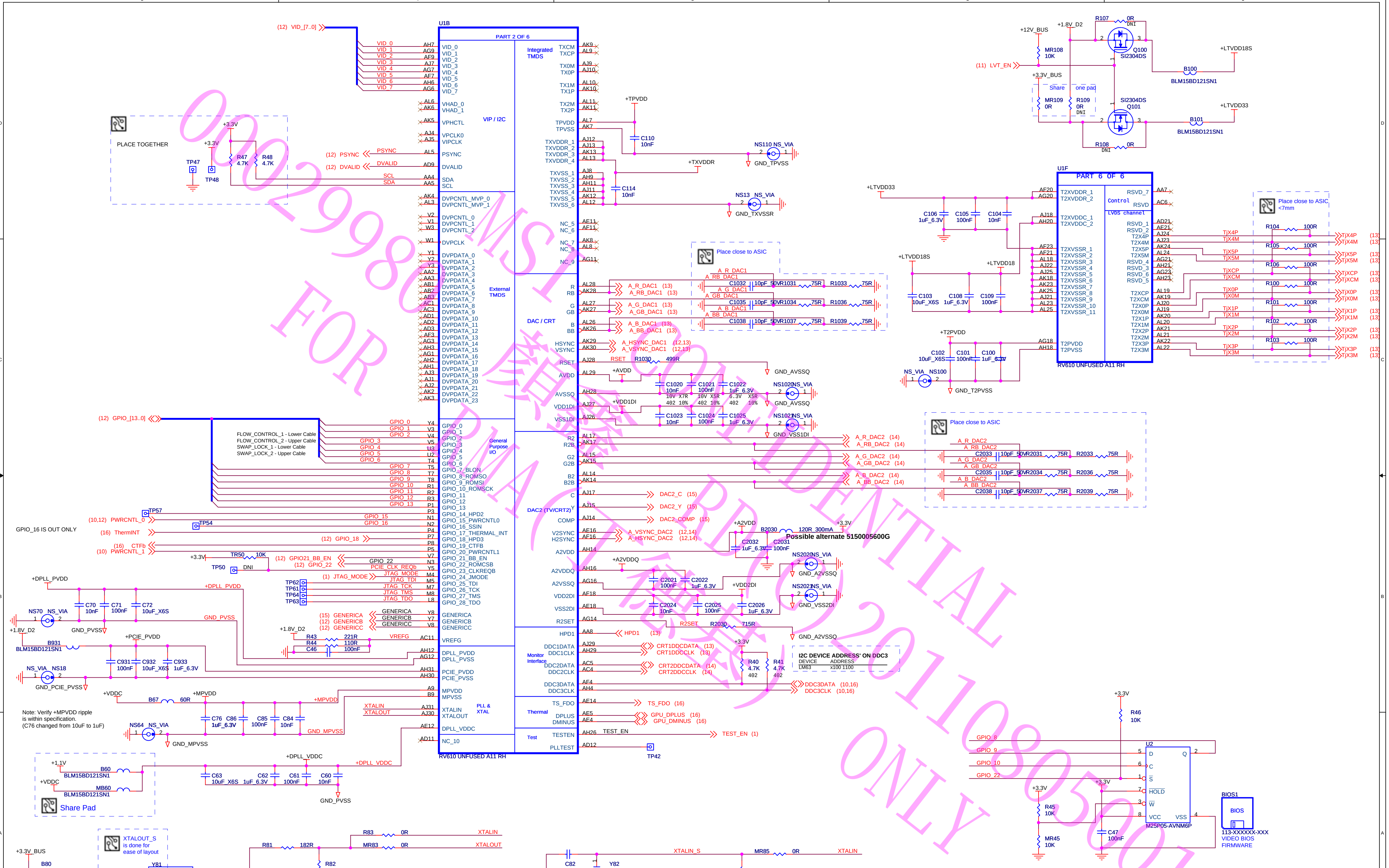
U1B
PART 2 OF 6
VIP / I2C
Integrated TMDS
External TMDS
DAC / CRT
General Purpose I/O
DAC2 (TV/CRT2)
Monitor Interface
PLL & XTAL
Thermal
Test
RV610 UNFUSED A11 RH
U1F
PART 6 OF 6
Control
LVDS channel
RV610 UNFUSED A11 RH
PLACE TOGETHER
Place close to ASIC
Place close to ASIC <7mm
Share one pad
Share Pad
XTALOUT_S is done for ease of layout
GPIO_16 IS OUT ONLY
FLOW_CONTROL_1 - Lower Cable
FLOW_CONTROL_2 - Upper Cable
SWAP_LOCK_1 - Lower Cable
SWAP_LOCK_2 - Upper Cable
Possible alternate 5150005600G
I2C DEVICE ADDRESS' ON DDC3
DEVICE ADDRESS
LM63 x100 1100
Note: Verify +MPVDD ripple is within specification. (C76 changed from 10uF to 1uF)
BIOS1
113-XXXXXX-XXX
VIDEO BIOS FIRMWARE
M25P05-AVNM6P
Y81 27.000MHz
Y82 27.000MHz_10PPM
Q100 SI2304DS
Q101 SI2304DS
BLM15BD121SN1

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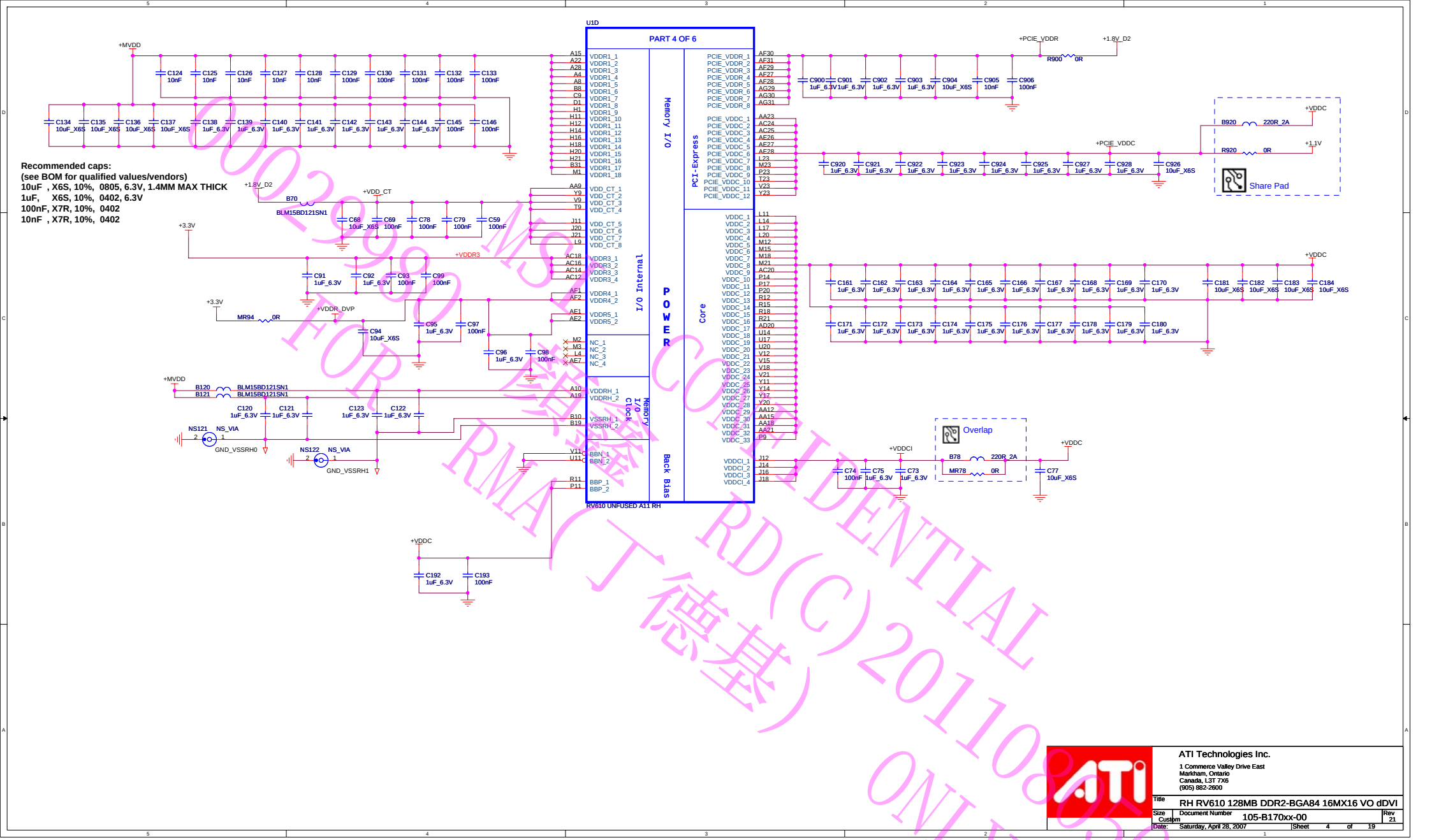

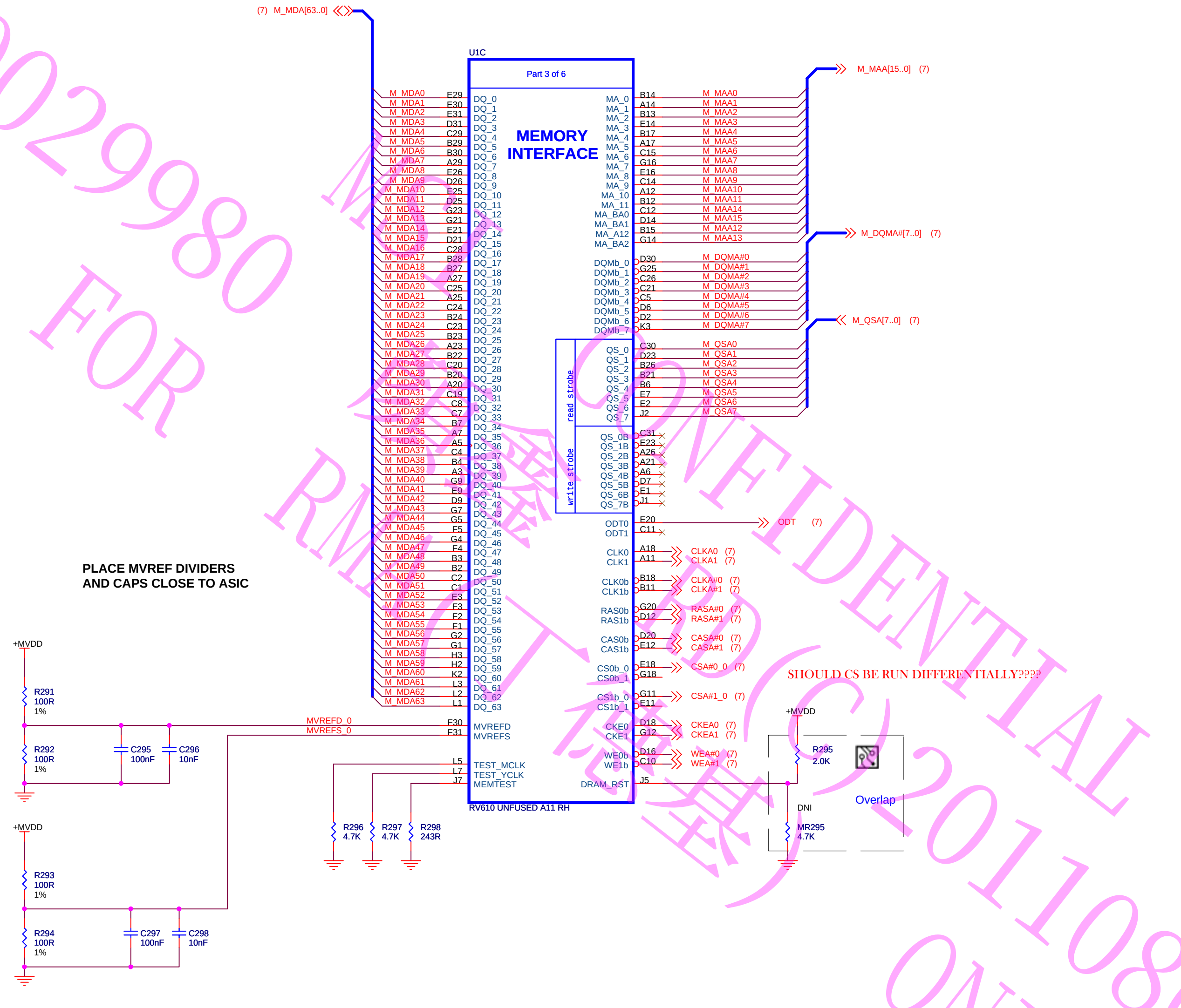

U1C
Part 3 of 6
MEMORY INTERFACE
RV610 UNFUSED A11 RH
(7) M_MDA[63..0]
M_MAA[15..0] (7)
M_DQMA#[7..0] (7)
M_QSA[7..0] (7)
read strobe
write strobe
ODT (7)
CLKA0 (7)
CLKA1 (7)
CLKA#0 (7)
CLKA#1 (7)
RASA#0 (7)
RASA#1 (7)
CASA#0 (7)
CASA#1 (7)
CSA#0_0 (7)
CSA#1_0 (7)
CKEA0 (7)
CKEA1 (7)
WEA#0 (7)
WEA#1 (7)
MVREFD
MVREFS
MVREFD_0
MVREFS_0
TEST_MCLK
TEST_YCLK
MEMTEST
DRAM_RST
SHOULD CS BE RUN DIFFERENTIALLY????
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC
+MVDD
R291 100R 1%
R292 100R 1%
R293 100R 1%
R294 100R 1%
C295 100nF
C296 10nF
C297 100nF
C298 10nF
R296 4.7K
R297 4.7K
R298 243R
R295 2.0K
DNI
MR295 4.7K
Overlap

DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

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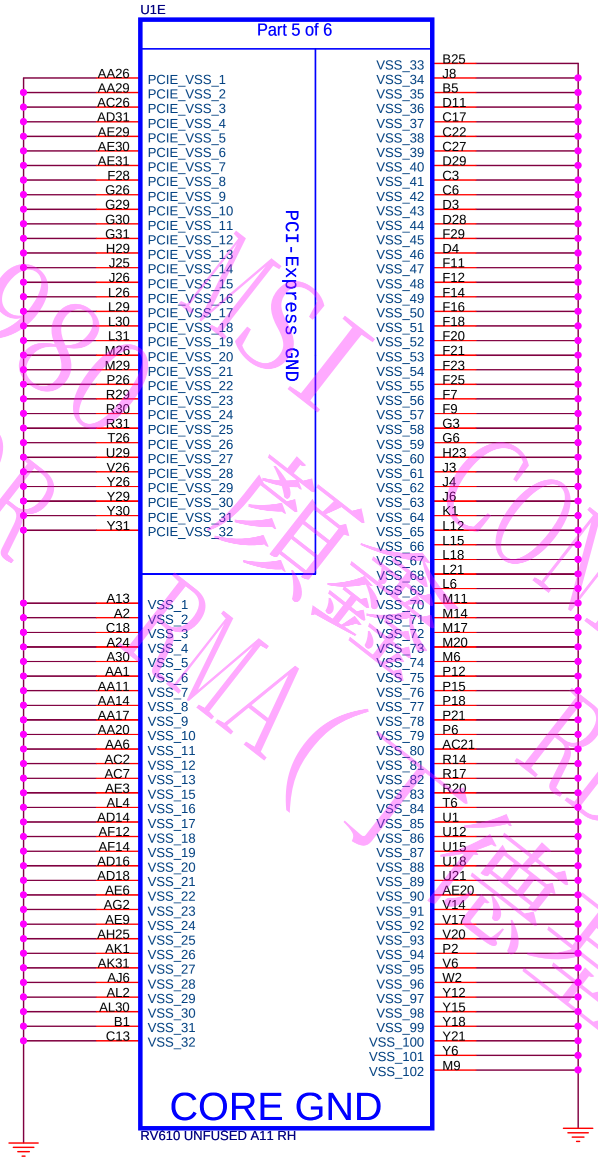
U1E
Part 5 of 6
PCI-Express GND
CORE GND
RV610 UNFUSED A11 RH
AA26 PCIE_VSS_1
AA29 PCIE_VSS_2
AC26 PCIE_VSS_3
AD31 PCIE_VSS_4
AE29 PCIE_VSS_5
AE30 PCIE_VSS_6
AE31 PCIE_VSS_7
F28 PCIE_VSS_8
G26 PCIE_VSS_9
G29 PCIE_VSS_10
G30 PCIE_VSS_11
G31 PCIE_VSS_12
H29 PCIE_VSS_13
J25 PCIE_VSS_14
J26 PCIE_VSS_15
L26 PCIE_VSS_16
L29 PCIE_VSS_17
L30 PCIE_VSS_18
L31 PCIE_VSS_19
M26 PCIE_VSS_20
M29 PCIE_VSS_21
P26 PCIE_VSS_22
R29 PCIE_VSS_23
R30 PCIE_VSS_24
R31 PCIE_VSS_25
T26 PCIE_VSS_26
U29 PCIE_VSS_27
V26 PCIE_VSS_28
Y26 PCIE_VSS_29
Y29 PCIE_VSS_30
Y30 PCIE_VSS_31
Y31 PCIE_VSS_32
A13 VSS_1
A2 VSS_2
C18 VSS_3
A24 VSS_4
A30 VSS_5
AA1 VSS_6
AA11 VSS_7
AA14 VSS_8
AA17 VSS_9
AA20 VSS_10
AA6 VSS_11
AC2 VSS_12
AC7 VSS_13
AE3 VSS_15
AL4 VSS_16
AD14 VSS_17
AF12 VSS_18
AF14 VSS_19
AD16 VSS_20
AD18 VSS_21
AE6 VSS_22
AG2 VSS_23
AF9 VSS_24
AH25 VSS_25
AK1 VSS_26
AK31 VSS_27
AJ6 VSS_28
AL2 VSS_29
AL30 VSS_30
B1 VSS_31
C13 VSS_32
VSS_33 B25
VSS_34 J8
VSS_35 B5
VSS_36 D11
VSS_37 C17
VSS_38 C22
VSS_39 C27
VSS_40 D29
VSS_41 C3
VSS_42 C6
VSS_43 D3
VSS_44 D28
VSS_45 F29
VSS_46 D4
VSS_47 F11
VSS_48 F12
VSS_49 F14
VSS_50 F16
VSS_51 F18
VSS_52 F20
VSS_53 F21
VSS_54 F23
VSS_55 F25
VSS_56 F7
VSS_57 F9
VSS_58 G3
VSS_59 G6
VSS_60 H23
VSS_61 J3
VSS_62 J4
VSS_63 J6
VSS_64 K1
VSS_65 L12
VSS_66 L15
VSS_67 L18
VSS_68 L21
VSS_69 L6
VSS_70 M11
VSS_71 M14
VSS_72 M17
VSS_73 M20
VSS_74 M6
VSS_75 P12
VSS_76 P15
VSS_77 P18
VSS_78 P21
VSS_79 P6
VSS_80 AC21
VSS_81 R14
VSS_82 R17
VSS_83 R20
VSS_84 T6
VSS_85 U1
VSS_86 U12
VSS_87 U15
VSS_88 U18
VSS_89 U21
VSS_90 AE20
VSS_91 V14
VSS_92 V17
VSS_93 V20
VSS_94 P2
VSS_95 V6
VSS_96 W2
VSS_97 Y12
VSS_98 Y15
VSS_99 Y18
VSS_100 Y21
VSS_101 Y6
VSS_102 M9

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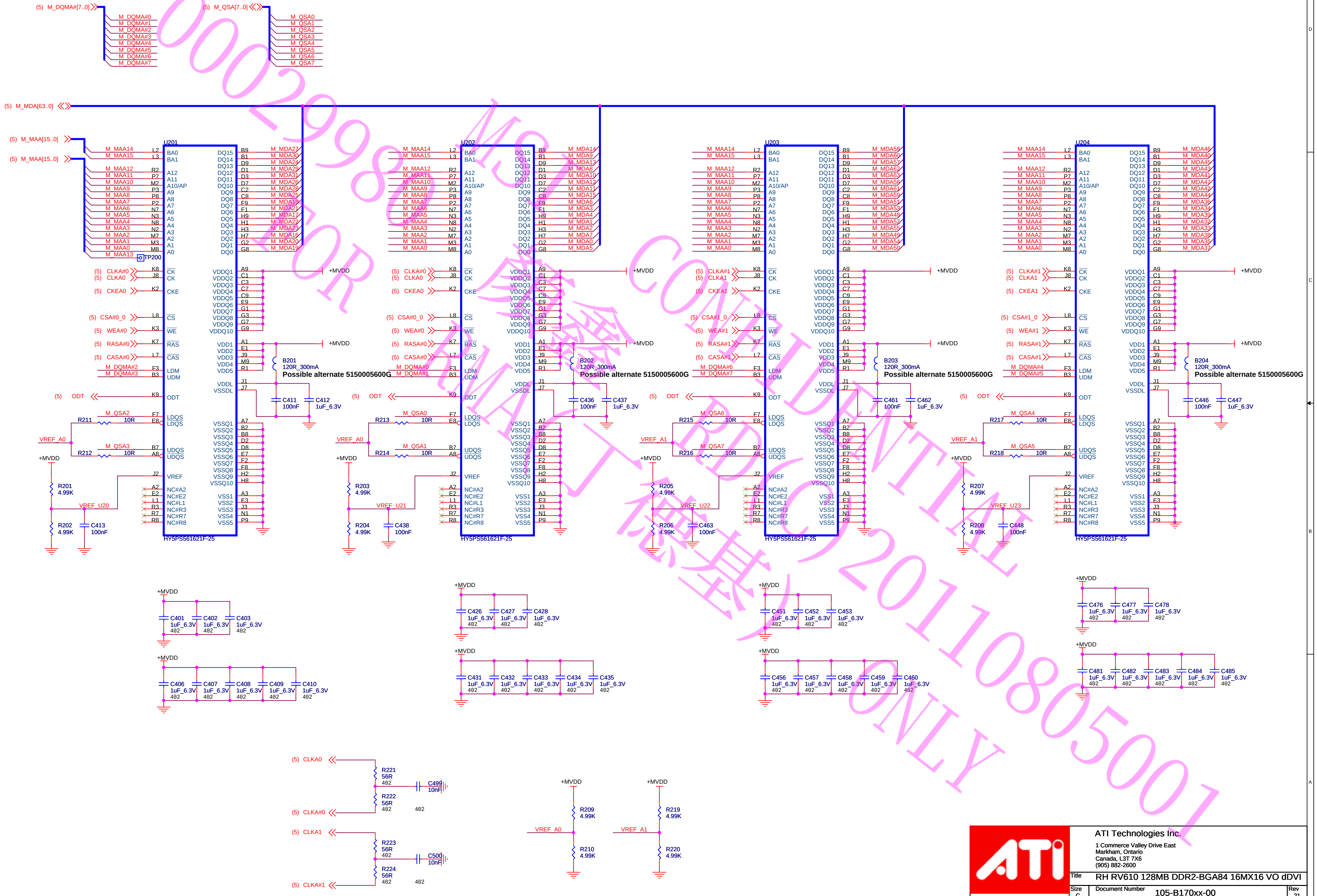
CHANNEL A: RANK 0 128MB DDR2



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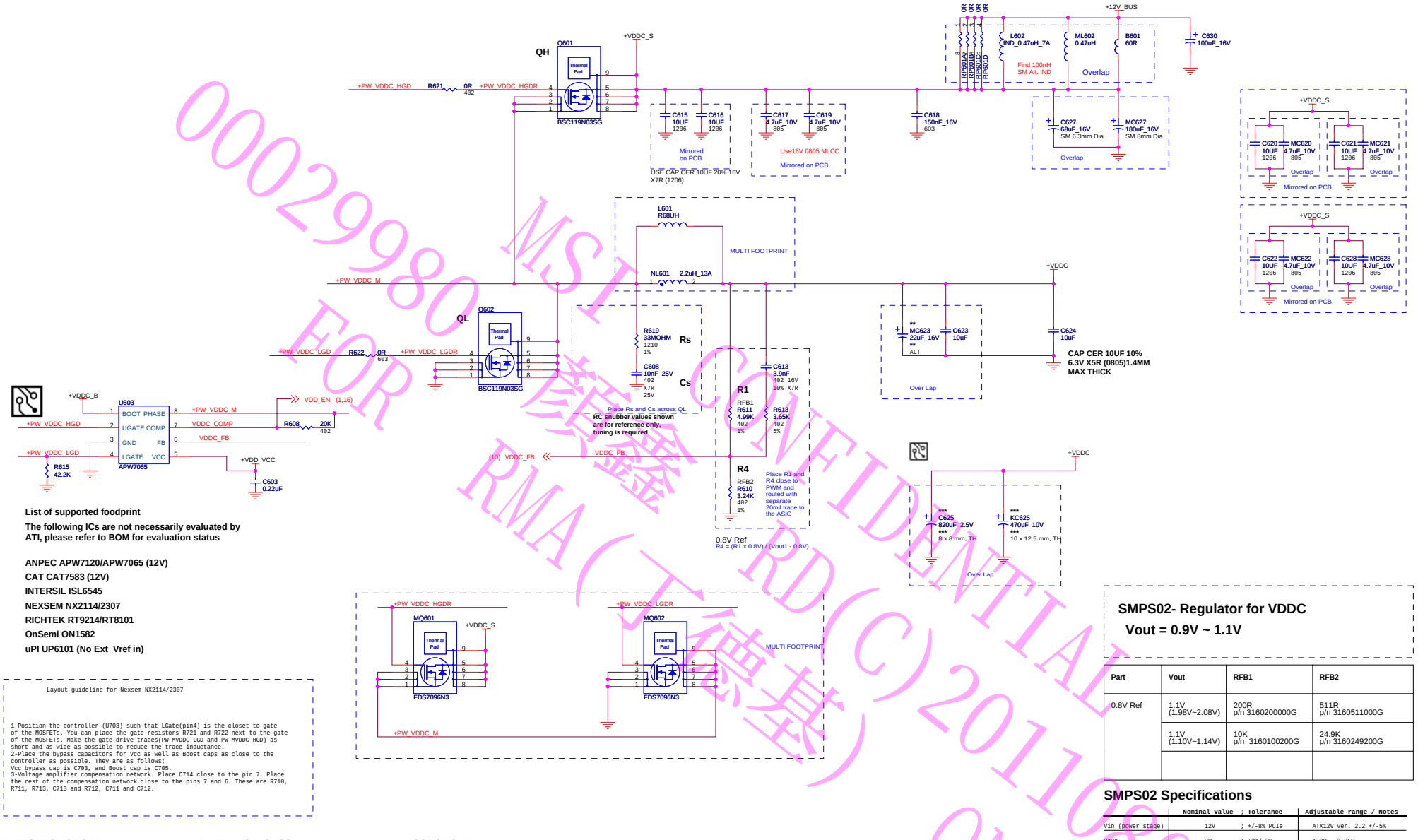


List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7120/APW7065 (12V)
CAT CAT7583 (12V)
INTERSIL ISL6545
NEXSEM NX2114/2307
RICHTEK RT9214/RT8101
OnSemi ON1582
uPI UP6101 (No Ext_Vref in)

Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

SMPS02- Regulator for VDDC

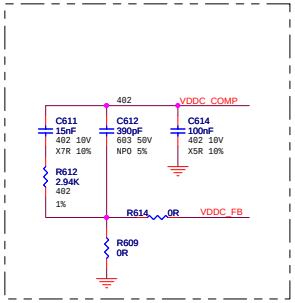
Vout = 0.9V ~ 1.1V

Part	Vout	RFB1	RFB2
0.8V Ref	1.1V (1.98V~2.08V)	200R p/n 3160200000G	511R p/n 3160511000G
	1.1V (1.10V~1.14V)	10K p/n 3160100200G	24.9K p/n 3160249200G

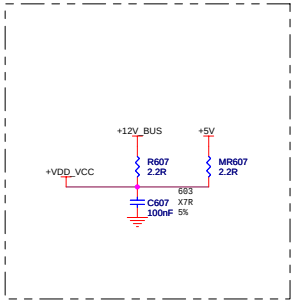
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

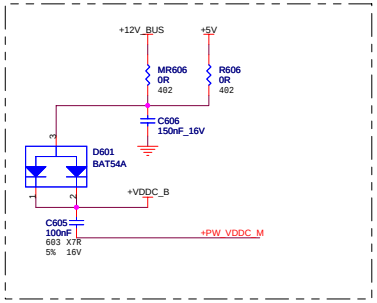
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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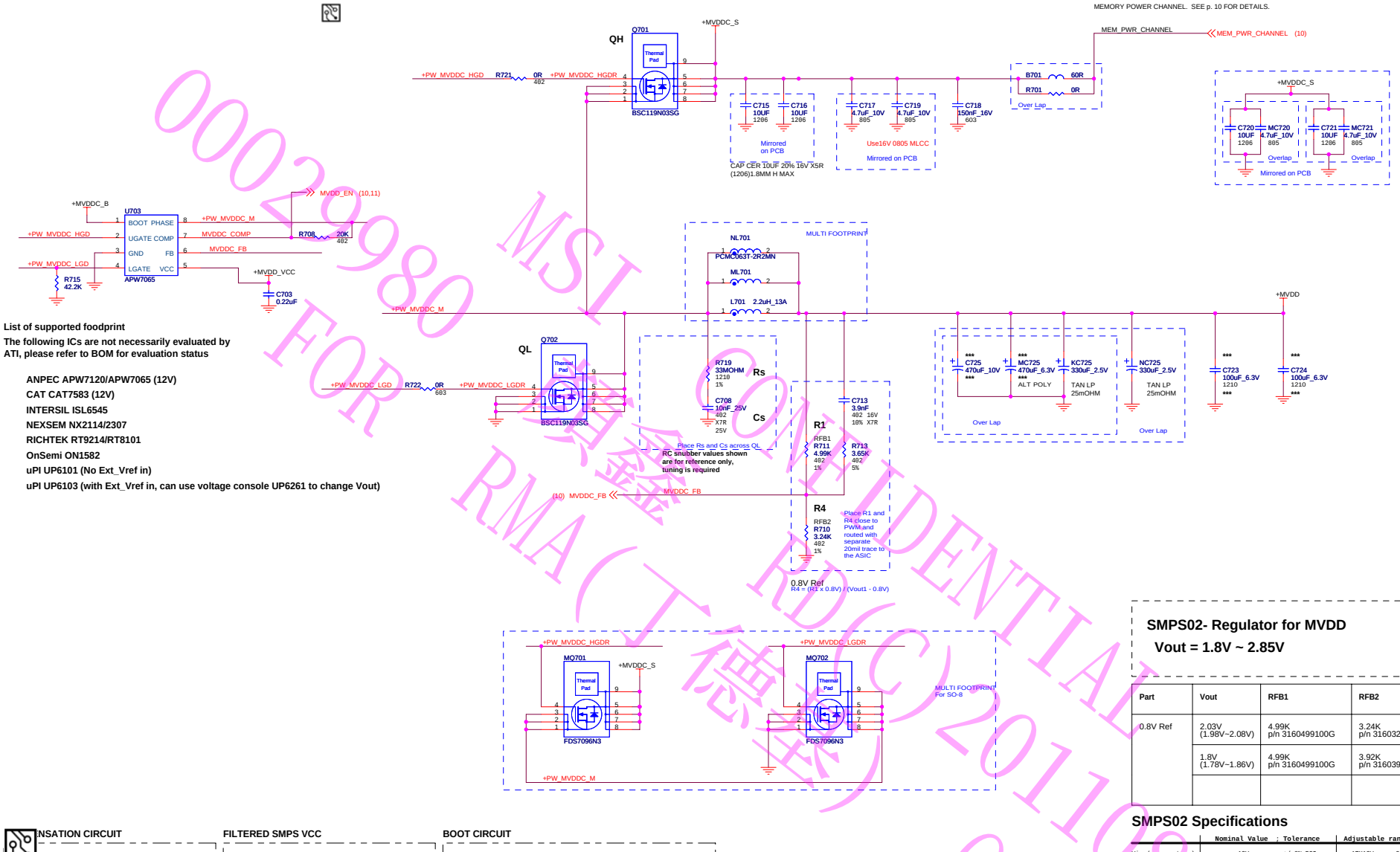

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- **INTERSIL ISL6545**
- **NEXSEM NX2114/2307**
- **RICHTEK RT9214/RT8101**
- **OnSemi ON1582**
- **uPI UP6101 (No Ext_Vref in)**
- **uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**

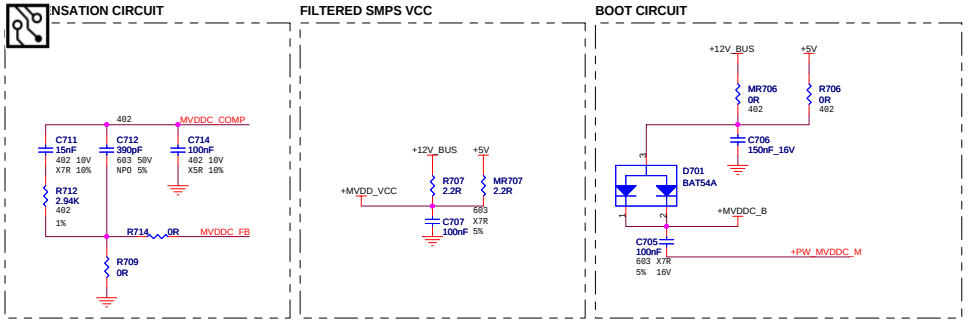
SMPS02- Regulator for MVDD

Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G
	1.8V (1.78V~1.86V)	4.99K p/n 3160499100G	3.92K p/n 3160392100G

SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		



Layout guideline for Nexsem NX2114/2307

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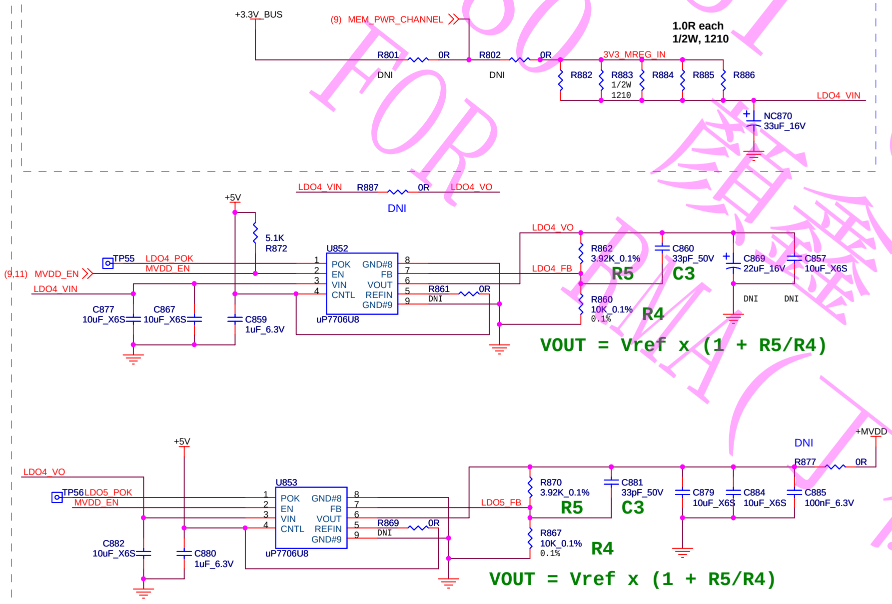
Linear Regulator for +MVDD
Vout = 1.8V ~ 2.1V
Iout = 2.75A MAX
P_REG = 1.35W
Tj(rise)max = 1.35Wx50C/W(50~70mm sq. Cu) = 67.5C

MEM PWR INPUT	INSTALL	DO NOT INSTALL
3.3V BUS (3V3_BUS_F)	R801 R802	R602 R701 or B701
12V (+VDDC_S)	R602 R701 or B701	R801 R802

Req = 1R/5 = 0.2R
P_Req = 0.2R * 2.75^2 = 1.5W
P_Reach = 1.5W/5 = 300mW < 500mW * 70%

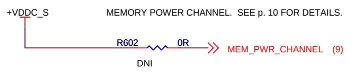
MEMORY POWER CHANNEL TO EASE LAYOUT CONGESTION OF LP BOARD. MEMORY POWER CHANNEL CAN BE USED TO DELIVER SOURCE VOLTAGE TO MVDD SMPS OR LINEAR REGULATORS (12V IN OR 3.3V IN)

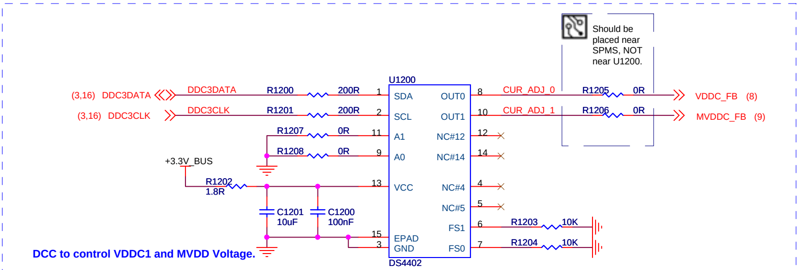


+3.3V_BUS
(9) MEM_PWR_CHANNEL
R801 0R DNI
R802 0R DNI
3V3_MREG_IN
1.0R each
1/2W, 1210
R882 R883 1/2W 1210 R884 R885 R886
LDO4_VIN
NC870 33uF_16V
LDO4_VIN R887 0R LDO4_VO
DNI
+5V
5.1K R872
TP55 LDO4_POK
(9,11) MVDD_EN
MVDD_EN
LDO4_VIN
U852
POK EN VIN CNTL GND#8 FB VOUT REFIN GND#9
uP7706U8
C877 10uF_X6S
C867 10uF_X6S
C859 1uF_6.3V
R861 0R DNI
LDO4_VO
LDO4_FB
R862 3.92K_0.1%
R5
C860 33pF_50V
C3
R860 10K_0.1%
R4
C869 22uF_16V
C857 10uF_X6S
DNI DNI
VOUT = Vref x (1 + R5/R4)
+5V
LDO4_VO
TP56 LDO5_POK
MVDD_EN
U853
POK EN VIN CNTL GND#8 FB VOUT REFIN GND#9
uP7706U8
C882 10uF_X6S
C880 1uF_6.3V
R869 0R DNI
LDO5_FB
R870 3.92K_0.1%
R5
C881 33pF_50V
C3
R867 10K_0.1%
R4
C879 10uF_X6S
C884 10uF_X6S
C885 100nF_6.3V
DNI
R877 0R
+MVDD
VOUT = Vref x (1 + R5/R4)

Memory Power Channel
Source Selection

MEMORY POWER CHANNEL. SEE p. 10 FOR DETAILS.





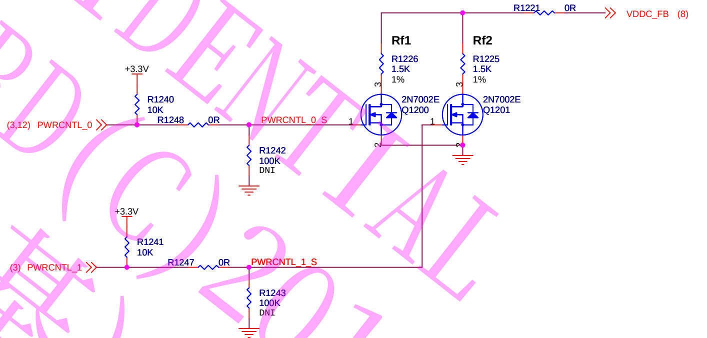
Should be placed near SPMS, NOT near U1200.
U1200
(3,16) DDC3DATA
DDC3DATA R1200 200R
(3,16) DDC3CLK
DDC3CLK R1201 200R
R1207 0R
R1208 0R
+3.3V_BUS
R1202 1.8R
C1201 10uF
C1200 100nF
SDA SCL A1 A0 VCC EPAD GND
OUT0 OUT1 NC#12 NC#14 NC#4 NC#5 FS1 FS0
DS4402
CUR_ADJ_0 R1205 0R VDDC_FB (8)
CUR_ADJ_1 R1206 0R MVDDC_FB (9)
R1203 10K
R1204 10K

DCC to control VDDC1 and MVDD Voltage.

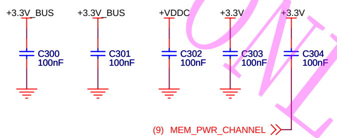
ASIC GPIO(x2) to control VDDC Voltage.

VDDC Voltage Settings Using GPIOs

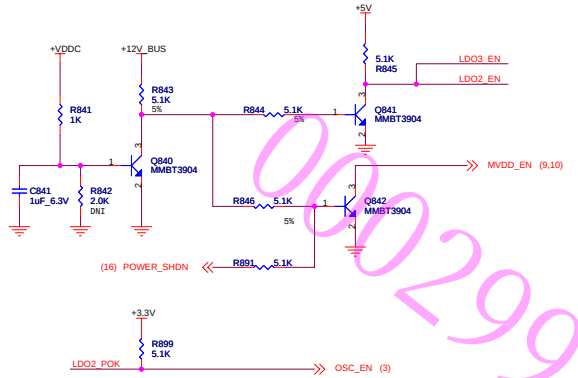
PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=		Rf1= Rf2=	Rf1= Rf2=	
0	0					
0	1					
1	0					
1	1	1	0	1		Power-up Default

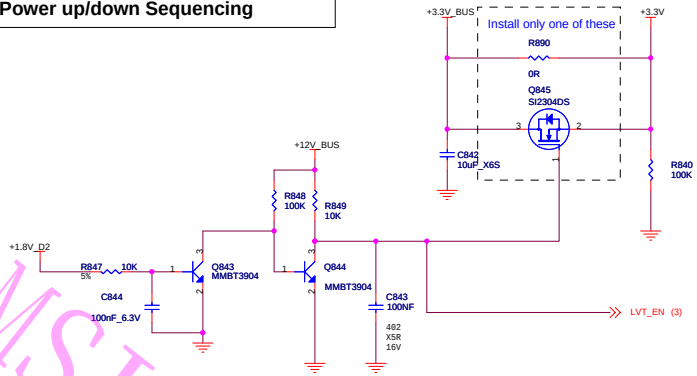


THESE ARE STITCHING CAPACITORS. THEIR PLACEMENT IS LAYOUT DEPENDANT.

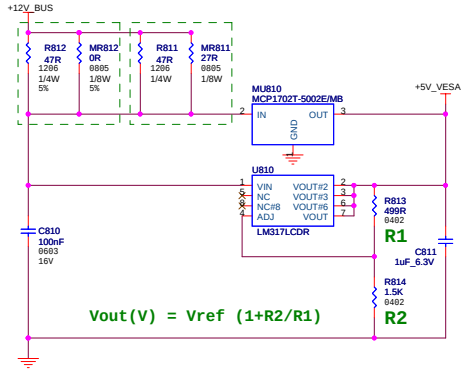


Power up/down Sequencing



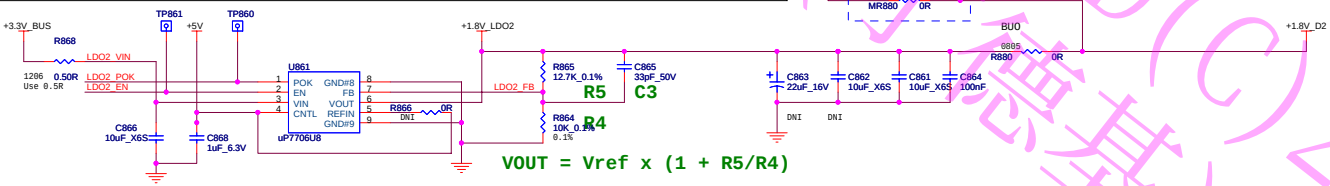


Regulators for +5V, +5V_VESA and +5V_VESA2



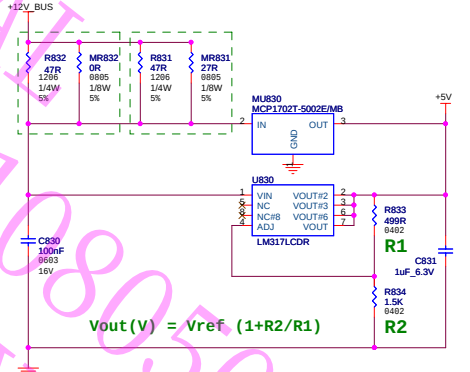
LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



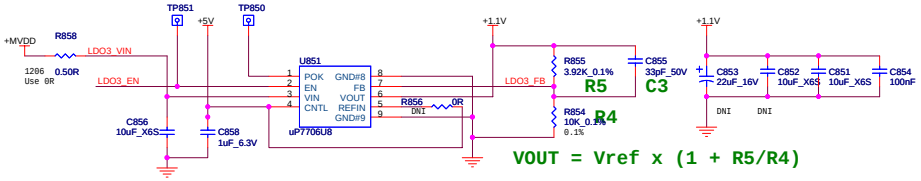
VOUT = Vref x (1 + R5/R4)

R868 (0.5R 1/2W or 0R 1206), R864, R865 & C865: To Be Verified



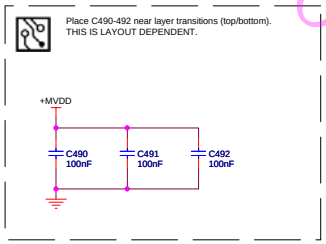
LDO #3: Vin = +1.45V to 2.1VMAX Vout = +1.1V +/- 2% Iout = 1.1A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

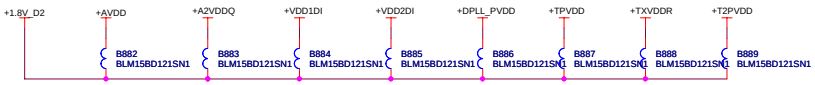


VOUT = Vref x (1 + R5/R4)

R854, R855 (3.92K) & C855: To Be Verified



Shared Power Rails



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PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - ATI Internal Use Only - Reserved (Default: 00)

GPIO(4) - DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

GPIO(5) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(6) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(7) - TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

GPIO(8) - ATI Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0] IF BIOS_ROM_EN=1 [default] (GPIO_22)
tmel - AT25F512A (512 kbit)0010
AT25F1024A (1 Mbit)0011
ST Microelectronics- M25P05A (512 kbit) 0100
M25P10A (1 Mbit) 0101
M25P20 (2 Mbit) 0101
Chingis (formerly PMC) -
Pm25LV512 (512 kbit) 0100
Pm25LV010 (1 Mbit) 0101

If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.
(Config 3 = don care).
x000 128MB
x001 256MB
x010 64MB
x011 32MB
x100 512MB
x101 1GB
x110 2GB
x111 4GB

GENERICC, GENERICB - ATI Internal Use Only - Reserved (Default: 0)

VSYNC - VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - ATI Internal Use Only - Reserved (Default 0)

PSYNC - VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO_21 - ATI Internal Use Only - Reserved (Default: 0)

VID_0 - ATI Internal Use Only - Reserved (Default: 0)

VID_1 - MSI_DIS (Default: 0)

VID_2 - ATI Internal Use Only - Reserved (Default: 0)

VID_3 - BIF_AUDIO_EN
0 - Disable HD Audio 1- Enable HD Audio

VID_4 - ATI Internal Use Only - Reserved (Default: 0)

VID_5 - 64BAR_EN_A (Default: 0)
Enable 64-bit BARS

VID_6:7 - ATI Internal Use Only - Reserved (Default: 00)

VSYNC - DDR2 VENDOR SELECT ATI Board Feature I
(see GPIO_18)

HSYNC2 - ATI Internal Use Only - Reserved (Default: 0)

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

GPIO_15 - FOR FUTURE EXPANSION

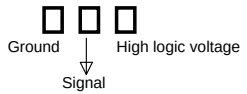
GPIO_22_ROMCSb - Enable external BIOS ROM device (Default 1)

GPIO_18 - DDR2 MEM VENDOR [V2SYNC:GPIO_18] ATI Board Feature I
QUIMONDA [0:0]
HYNIX [0:1]
SAMSUNG [1:0]

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout



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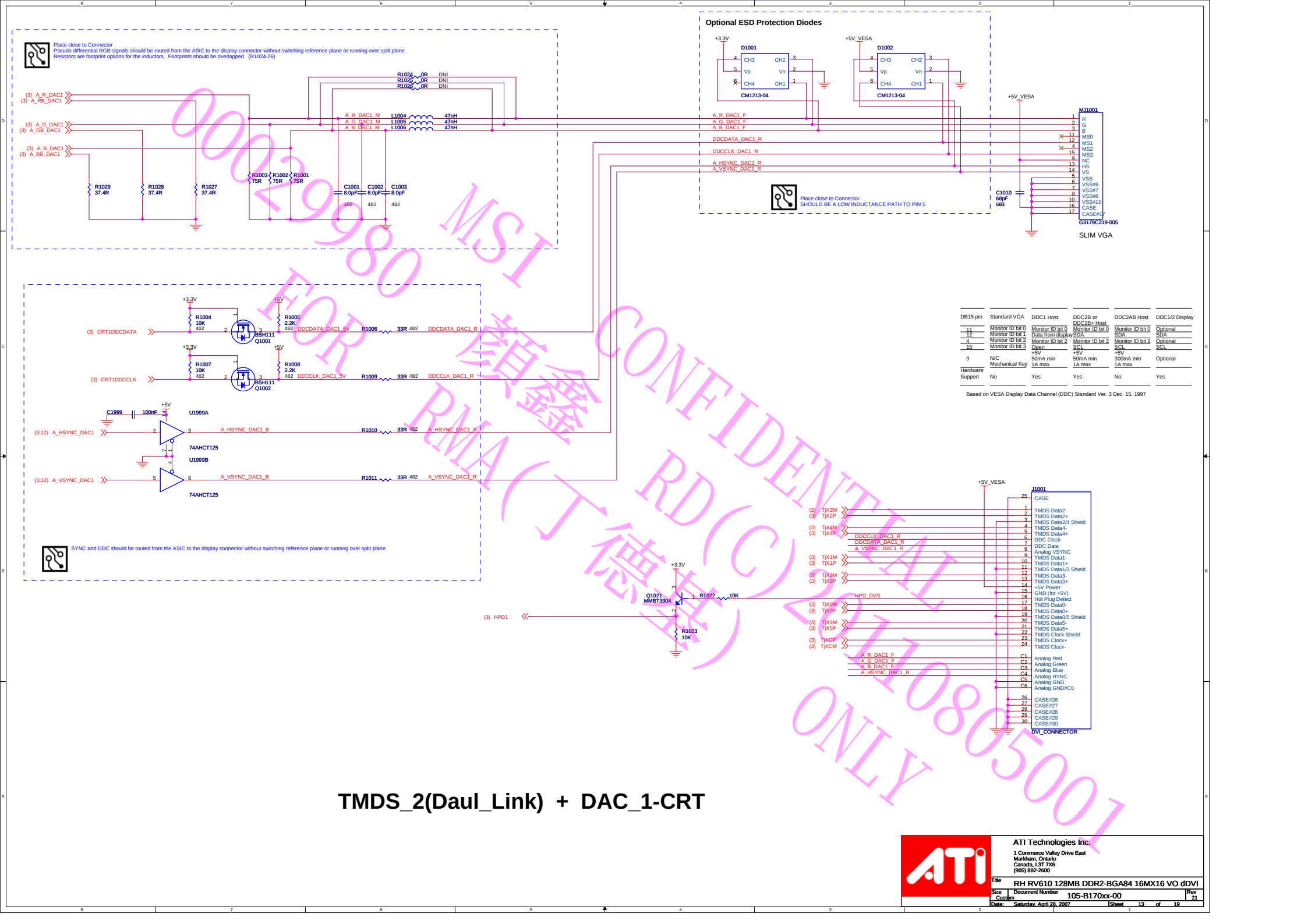

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

TMDS_2(Daul_Link) + DAC_1-CRT

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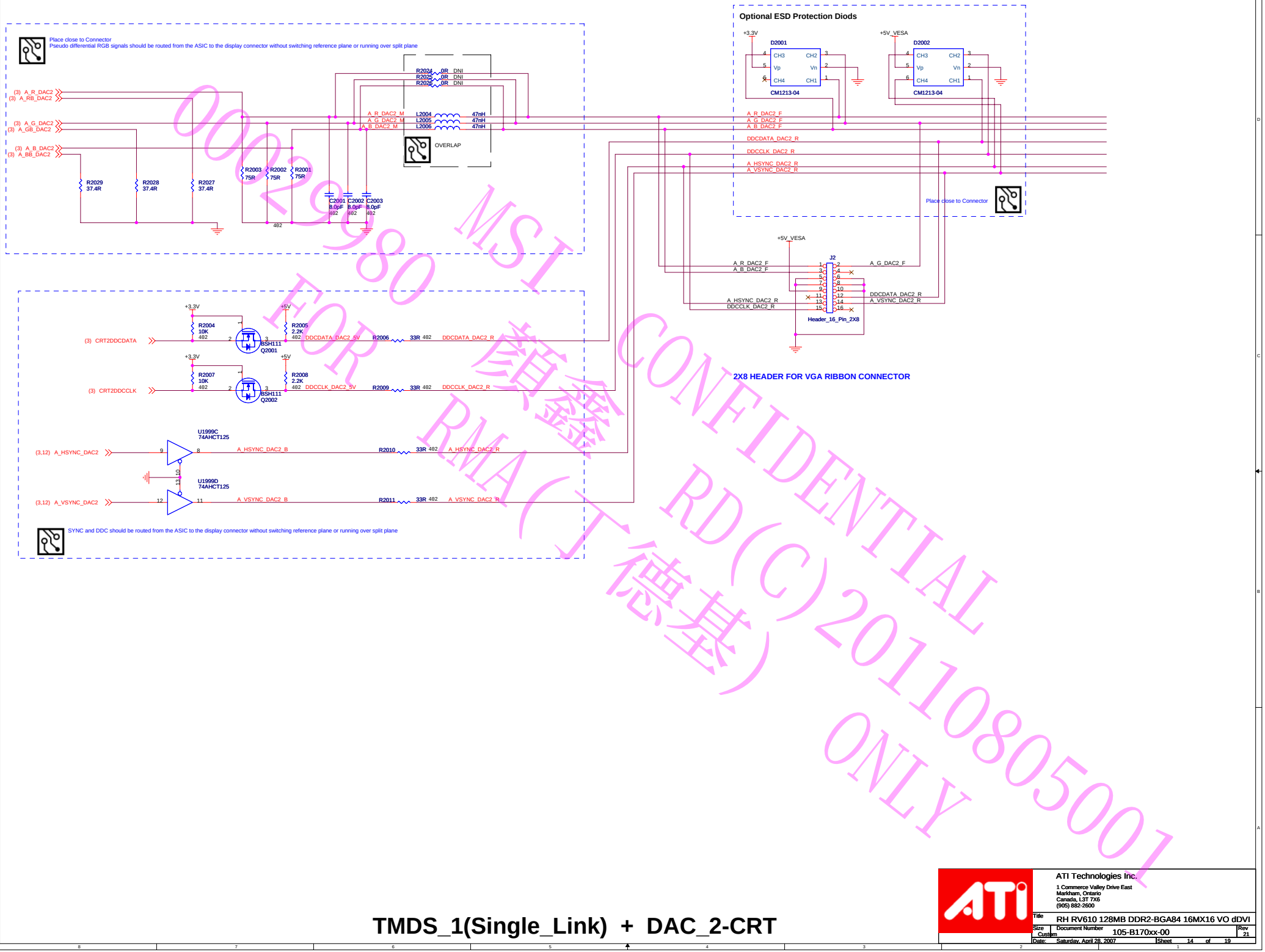

TMDS_1(Single_Link) + DAC_2-CRT

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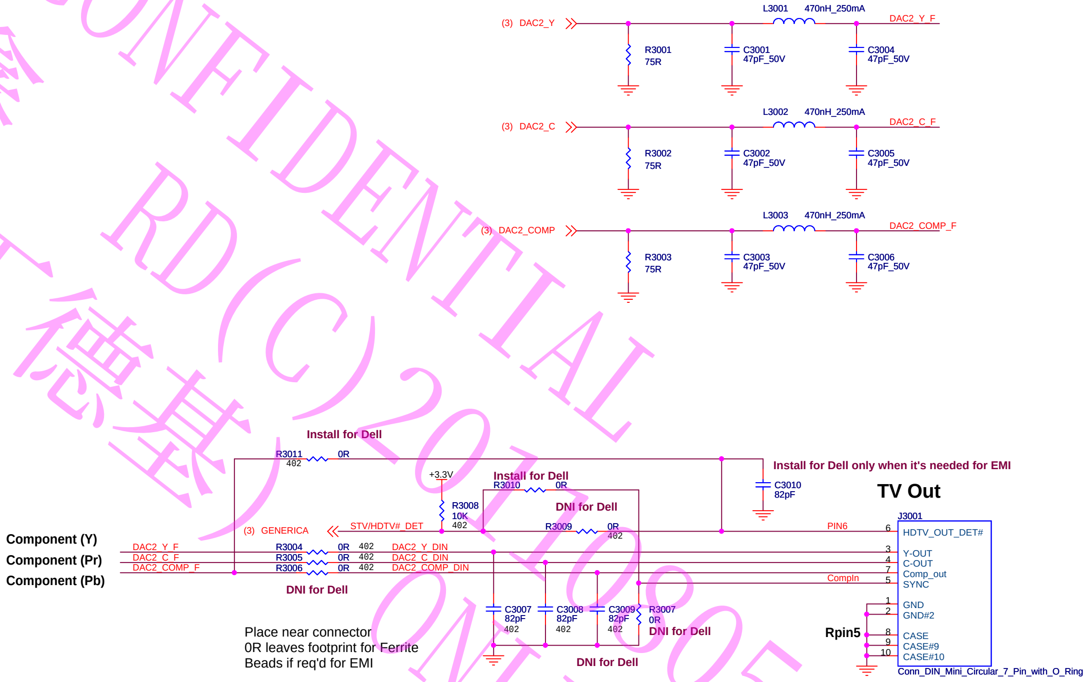
TV Out


(3) DAC2_Y
R3001 75R
C3001 47pF_50V
L3001 470nH_250mA
C3004 47pF_50V
DAC2_Y_F
(3) DAC2_C
R3002 75R
C3002 47pF_50V
L3002 470nH_250mA
C3005 47pF_50V
DAC2_C_F
(3) DAC2_COMP
R3003 75R
C3003 47pF_50V
L3003 470nH_250mA
C3006 47pF_50V
DAC2_COMP_F
Install for Dell
R3011 402 0R
+3.3V
R3008 10K 402
Install for Dell
R3010 0R
DNI for Dell
R3009 0R 402
Install for Dell only when it's needed for EMI
C3010 82pF
(3) GENERICA
STV/HDTV#_DET
PIN6
Component (Y)
Component (Pr)
Component (Pb)
DAC2_Y_F
DAC2_C_F
DAC2_COMP_F
R3004 0R 402
R3005 0R 402
R3006 0R 402
DAC2_Y_DIN
DAC2_C_DIN
DAC2_COMP_DIN
CompIn
DNI for Dell
C3007 82pF 402
C3008 82pF 402
C3009 82pF 402
R3007 0R
DNI for Dell
DNI for Dell
J3001
HDTV_OUT_DET#
Y-OUT
C-OUT
Comp_out
SYNC
GND
GND#2
CASE
CASE#9
CASE#10
Rpin5
Conn_DIN_Mini_Circular_7_Pin_with_O_Ring
Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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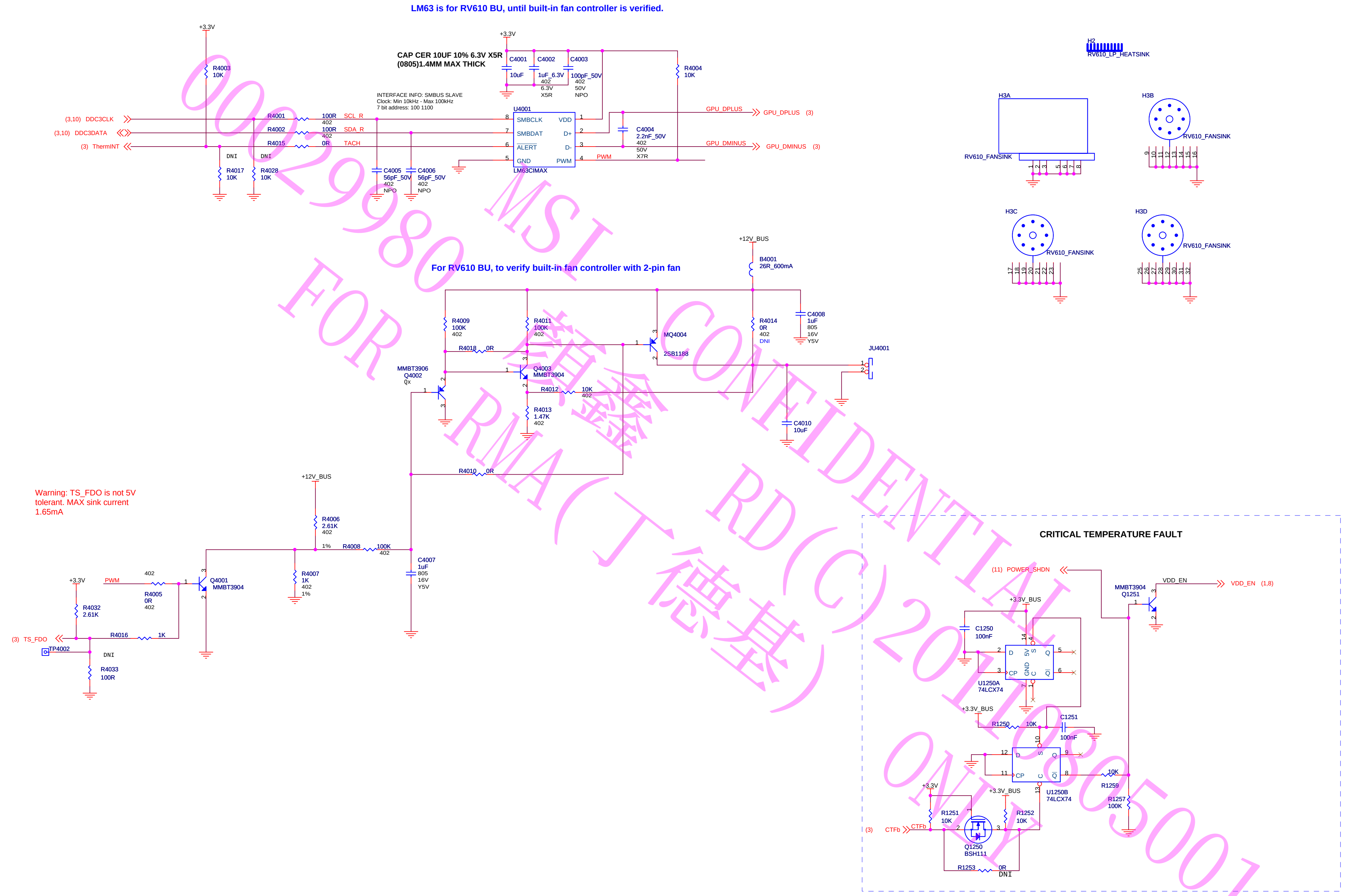

LM63 is for RV610 BU, until built-in fan controller is verified.
CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK
INTERFACE INFO: SMBUS SLAVE
Clock: Min 10kHz - Max 100kHz
7 bit address: 100 1100
+3.3V
R4003 10K
(3,10) DDC3CLK
(3,10) DDC3DATA
(3) ThermINT
R4001 100R SCL_R
R4002 100R SDA_R
R4015 0R TACH
R4017 10K DNI
R4028 10K DNI
C4005 56pF_50V 402 NPO
C4006 56pF_50V 402 NPO
C4001 10uF
C4002 1uF_6.3V 402 6.3V X5R
C4003 100pF_50V 402 50V NPO
U4001 LM63CIMAX
SMBCLK SMBDAT ALERT GND VDD D+ D- PWM
C4004 2.2nF_50V 402 50V X7R
R4004 10K
GPU_DPLUS (3)
GPU_DMINUS (3)
PWM
H2 RV610_LP_HEATSINK
H3A RV610_FANSINK
H3B RV610_FANSINK
H3C RV610_FANSINK
H3D RV610_FANSINK
For RV610 BU, to verify built-in fan controller with 2-pin fan
+12V_BUS
B4001 26R_600mA
R4009 100K 402
R4011 100K 402
R4018 0R
MMBT3906 Q4002 Qx
Q4003 MMBT3904
R4012 10K 402
R4013 1.47K 402
MQ4004 2SB1188
R4014 0R 402 DNI
C4008 1uF 805 16V Y5V
JU4001
C4010 10uF
R4010 0R
Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA
R4006 2.61K 402 1%
R4008 100K 402
C4007 1uF 805 16V Y5V
R4007 1K 402 1%
Q4001 MMBT3904
R4005 0R 402
R4032 2.61K
R4016 1K
(3) TS_FDO
TP4002
R4033 100R DNI
CRITICAL TEMPERATURE FAULT
(11) POWER_SHDN
MMBT3904 Q1251
VDD_EN
VDD_EN (1,8)
+3.3V_BUS
C1250 100nF
U1250A 74LCX74
R1250 10K
C1251 100nF
U1250B 74LCX74
R1259 10K
R1257 100K
R1251 10K
R1252 10K
(3) CTFb
Q1250 BSH111
R1253 0R DNI

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DVI/VGA SCREWS

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

MT1
MT_Hole_0.136_in.
DNI

MT2
MT_Hole_0.136_in_6VIA
DNI

ASSY1
BRACKET
8020040100G

ASSY2
BRACKET
LP
8020040400G

<Variant Name>

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<Variant Name>

Title

RH RV610 128MB DDR2-BGA84 16MX16 VO dDVI

Schematic No. 105-B170xx-00

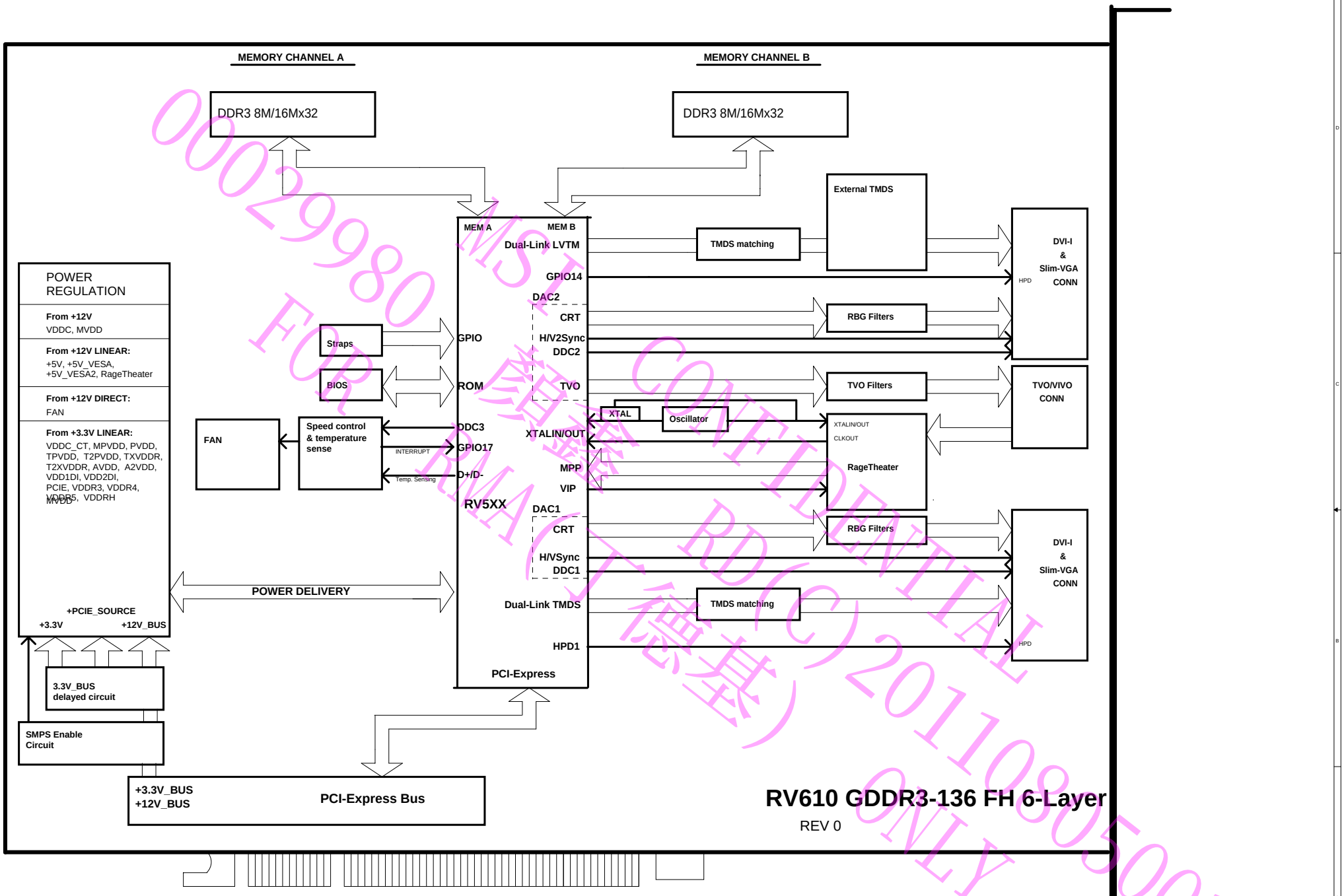
Date: Saturday, April 28, 2007

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.

Rev 21

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
014	00B	2007.02.22	RM C890/MC890, RM B801/L801/ML801
015	00B	2007.02.27	ADD R4010 FOR FAN CIRCUIT. ADD STITCHING CAPS C300, C301, C302, C303
016	00B	2007.02.28	CORRECT "300" TO C300; ADD C304, CHNG C301;
017	00B	2007.03.06	POWER SUPPLY CHANGES: ADD MC627, R615, R609, R715, R709, R714, R614; REMOVE MC630, MC624;
018	00B	2007.03.06	DUE TO LAYOUT CONSTRAINTS: RM ML601. CHANGE C627, MC627.
019	00C	2007.04.17	REMOVE R90, Q90 (A12+ ASIC REMOVES NEED FOR THESE PARTS); REMOVE C850 (IS NOT POPULATED ON ANY BOM - WILL CAUSE VDDC TO BE UNSTABLE); ADD C4010 (FOR FAN SPIN UP);
020	00C	2007.04.19	ADD C490, C491, C492 FOR POSSIBLE MEMORY SIGNAL INTEGRITY/EMI IMPROVEMENTS (PER EMI TEAM);
021	00	2007.04.25	NO NETLIST/LAYOUT CHANGES. SCHEMATIC UPDATE NOTES p.12 (V2SYNC/GPIO_18 CLARIFICATION)



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