PG161-A00

TU106 6GB GDDR6, 192b, X16
DVI-D/DP + DP + HDMI

TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	PCIE RC TERM
5	MEMORY: GPU FB_AB
6	MEMORY: FBA[31:0]
7	MEMORY: FBA[63:32]
8	MEMORY: FBB[31:0]
9	MEMORY: FBB[63:32]
10	MEMORY: GPU FB_CD
11	MEMORY: FBC[31:0]
12	MEMORY: FBC[63:32]
13	MEMORY: FBD[31:0]
14	MEMORY: FBD[63:32]
15	GPU PWR & GND
16	GPU Decoupling
17	GPU Decoupling2
18	IO: IFPAB DVI-D-DL
19	IO: IFPA DP
20	IO: IFPB DP
21	IO: IFPE & IFPF USBC NC
22	IO: IFPC HDMI
23	IO: IFPD DP
24	IO: NVHS Interface and Frame Lock
25	MISC1: Thermal, JTAG, GPIO,STEREO
26	MISC2: ROM, XTAL,STRAPS
27	PS: 1V8_AON
28	PS: 5V
29	PS: PEXVDD
30	PS: FBVDDQ
31	PS: FBVDDQ PH2
32	PS: NVVDD Controller
33	PS: NVVDD Controller OVR3i
34	PS: NVVDD Phase 6,4
35	PS: NVVDD Phase 3,5
36	PS: NVVDD Phase 2,1
37	PS: Input Power Balancing Switcher
38	PS: Input, Filtering, and Monitoring
39	PS: STEERING, UPB & HOT-UNPLUG
40	PS: Type-C BuckBoost
41	PD PPC
42	PS: 12V & 3V3_A SWITCHER
43	SEQ: 5V, 1V8, NV3V3 ENABLE
44	SEQ: NV, PEX, FB ENABLE
45	SEQ: VOLTAGE MONITOR
46	SEQ: DISCHARGE
47	SEQ: MISC
48	LOGO LED
49	LED DRIVER & BOOST
50	FAN
51	PS: Pre-filter
52	MECH
53	PTC

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Table of Contents

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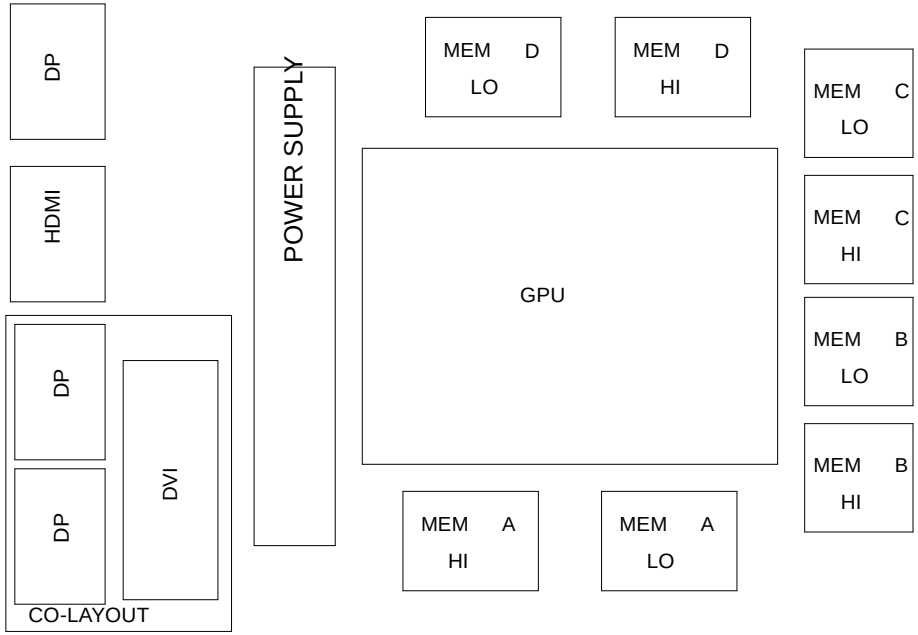
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 1 of 53

Page2: Block Diagram



Power Supply:

- Power Supply NVVDD-PH6
- Power Supply NVVDD-PH5
- Power Supply NVVDD-PH4
- Power Supply NVVDD-PH3
- Power Supply NVVDD-PH2
- Power Supply NVVDD-PH1
- Power Supply FBVDDQ-PH2
- Power Supply FBVDDQ-PH1
- Power Supply 5V
- PEX_VDD
- 1V8
- Fan
- DP_PWR

EXT_12V 2x4 PWR

PEX_12V Finger

3V3 Finger

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PAGE DETAIL	Block Diagram

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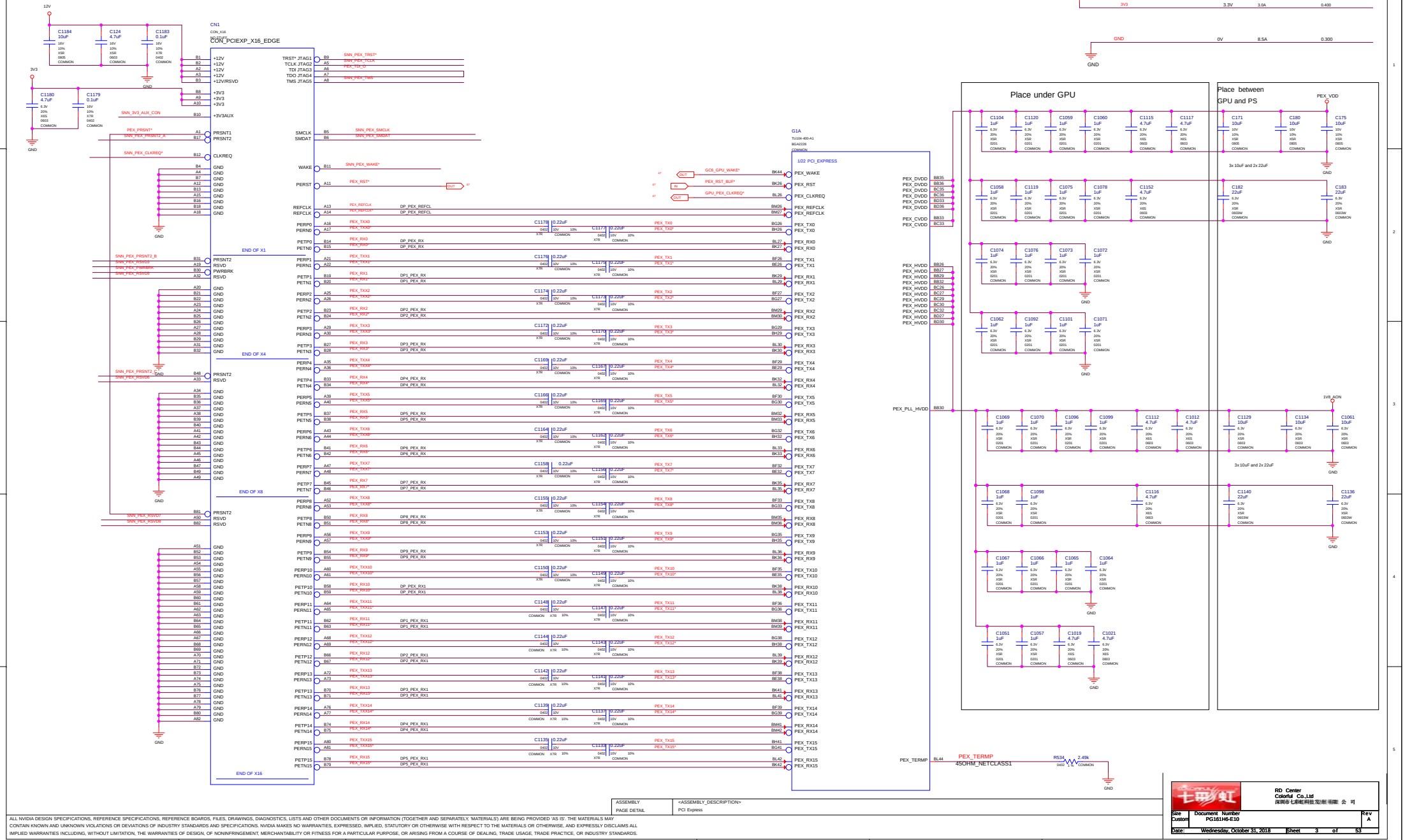
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 2 of 53

Page3: PCI Express



VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	5.5A	0.406
3.3V	3.0A	0.400
0V	8.5A	0.300

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI Express

Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 3 of 53

NO PEX GEN4 SUPPORT

DELETE RC TERMINATIONS

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCIE RC TERM

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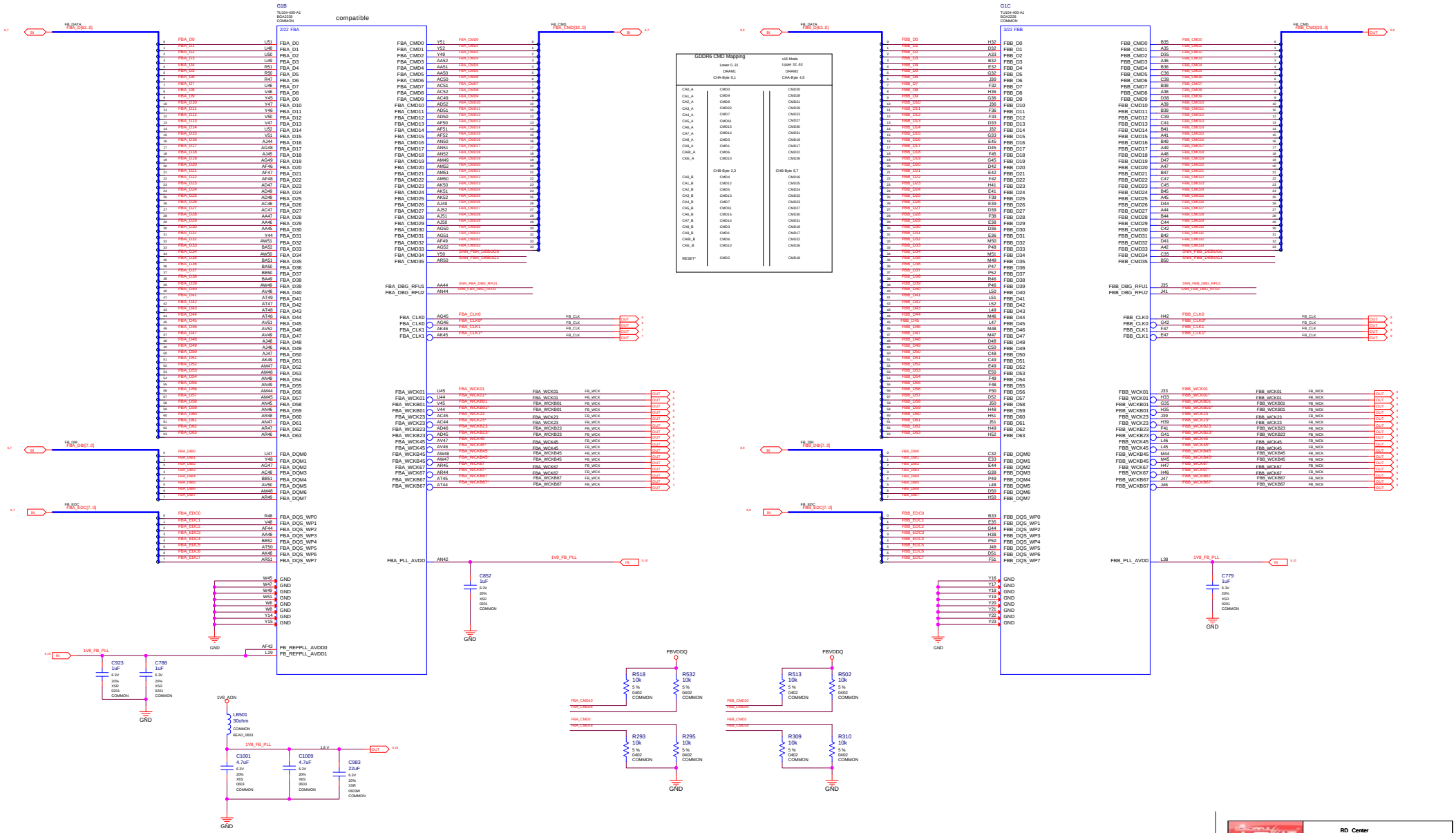
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 4 of 53

Page5: MEMORY: GPU Partition A/B



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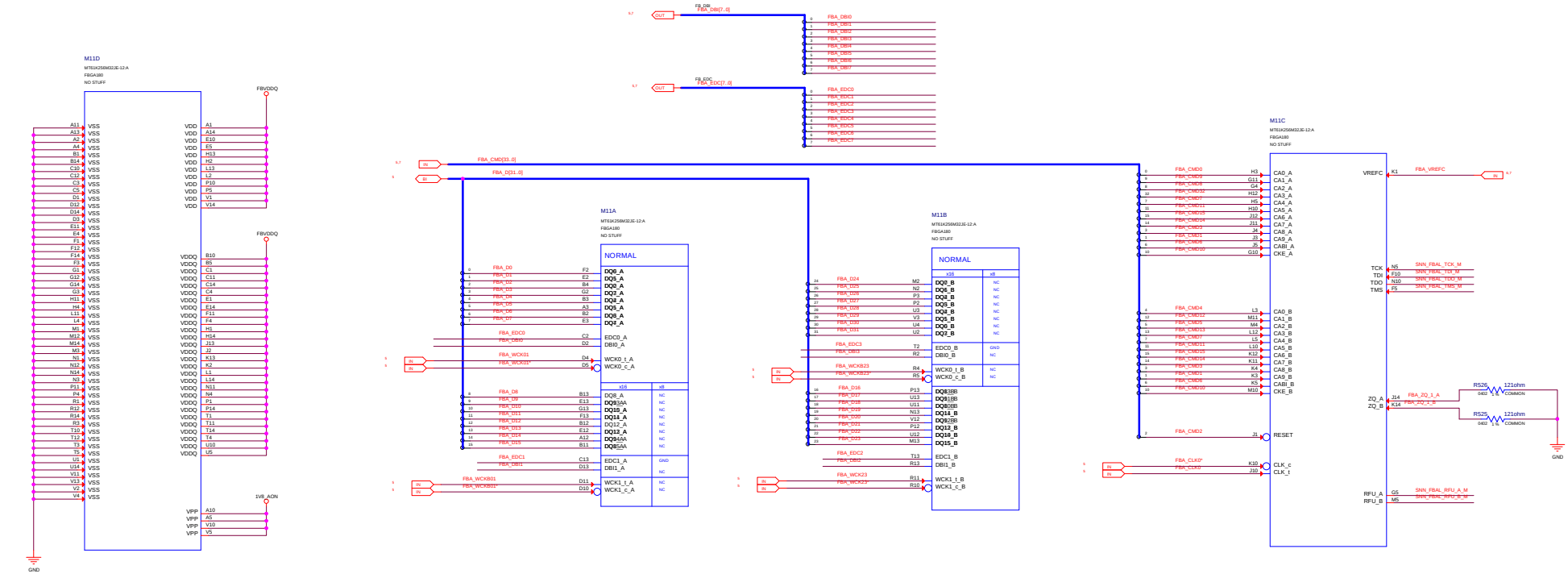
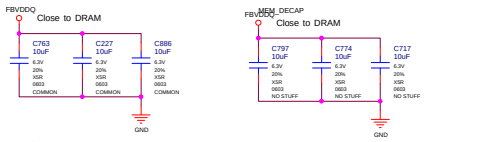
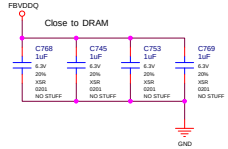
Size	Document Number	Rev
Custom	PG161H6-E10	A

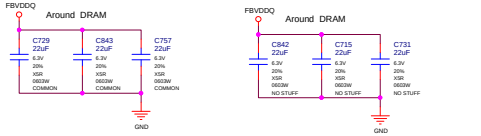
Date: Wednesday, October 31, 2018 Sheet 5 of 53

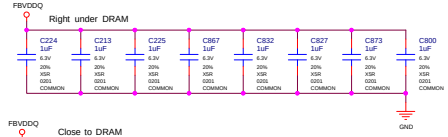
Page6: MEMORY: FBA Partition 31..0

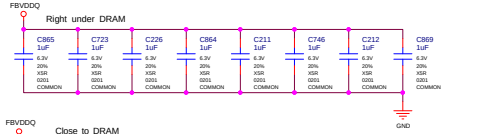


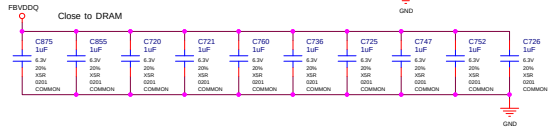


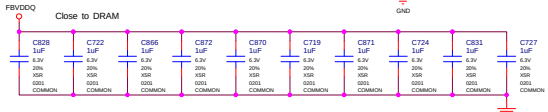




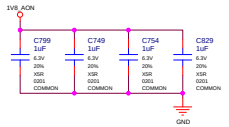








VREFC IS NOT USED IN x16 CONFIGURATION
1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R106



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Size	Document Number	Rev
Custom	PG161H6-E10	A
Date: Friday, November 02, 2018	Sheet 6 of 53	

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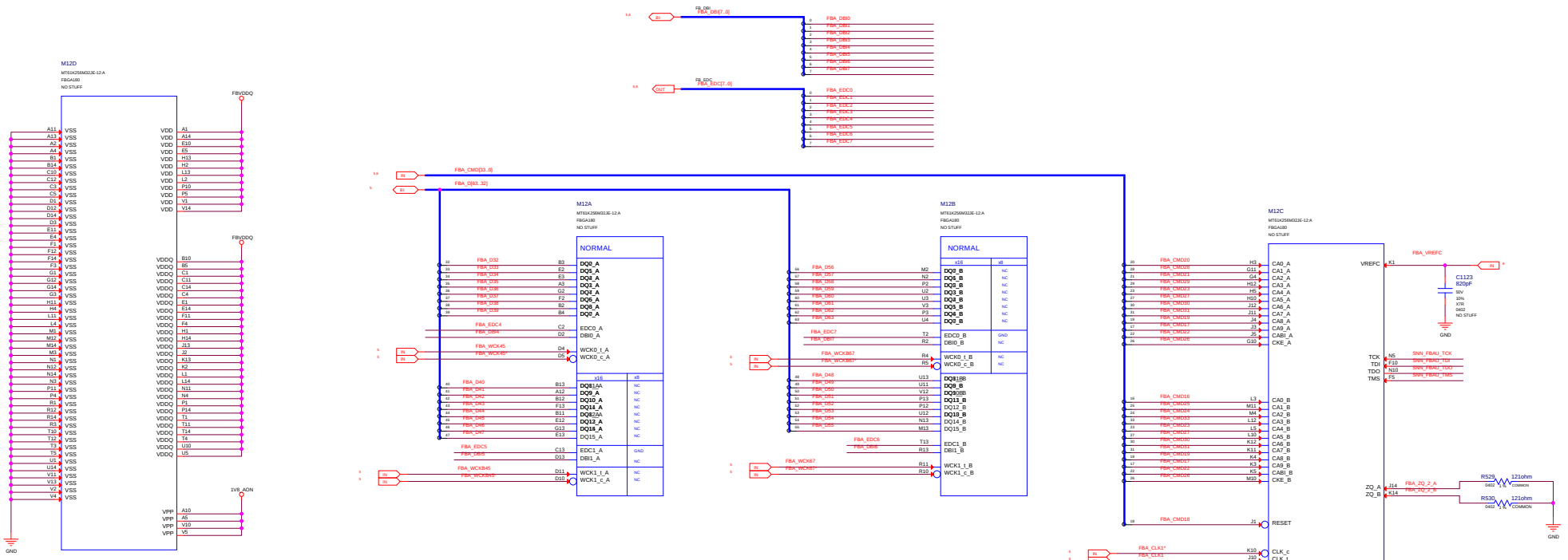
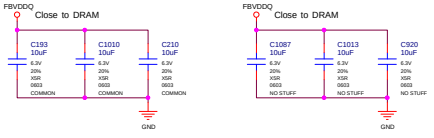
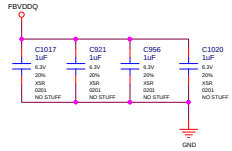
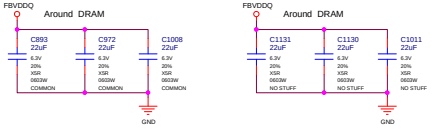
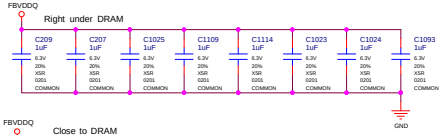
Page7: MEMORY: FBA Partition 63..32

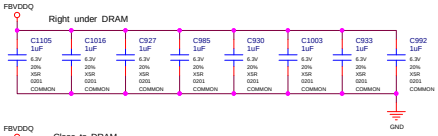


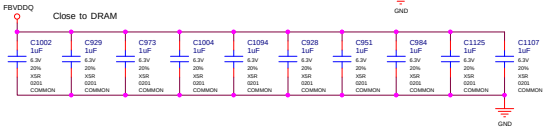


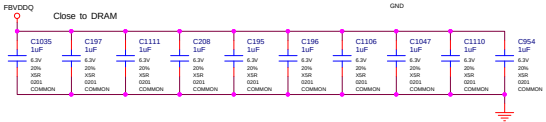


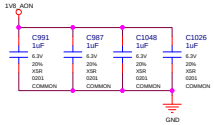












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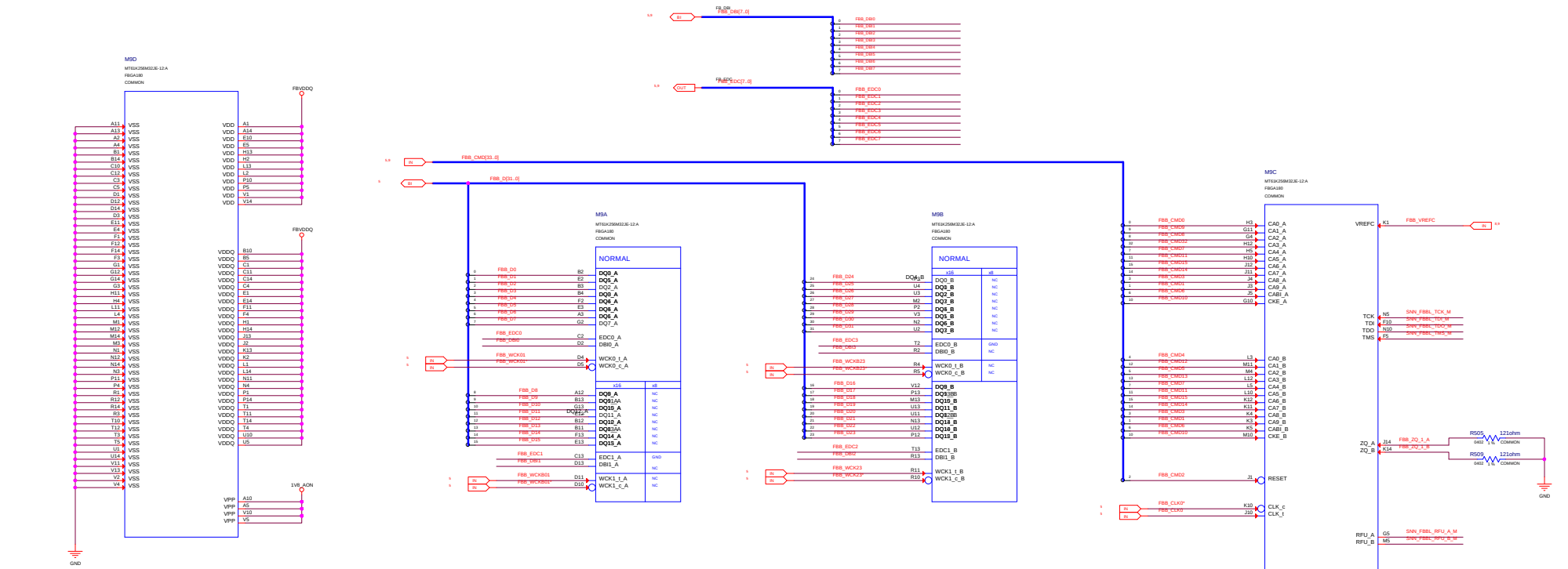
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Friday, November 02, 2018 Sheet 7 of 53

Page8: MEMORY: FBB Partition 31..0



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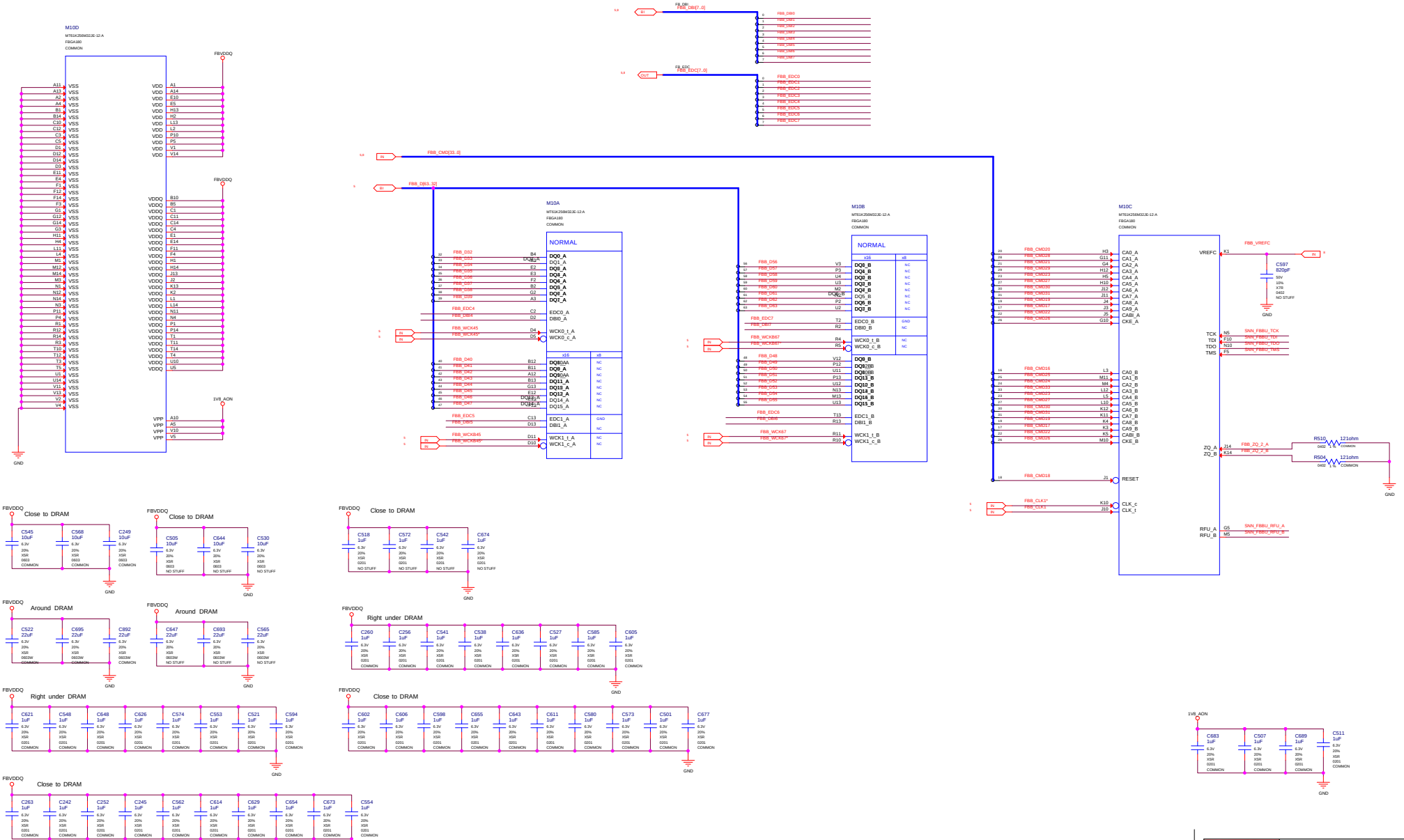
Page9: MEMORY: FBB Partition 63..32



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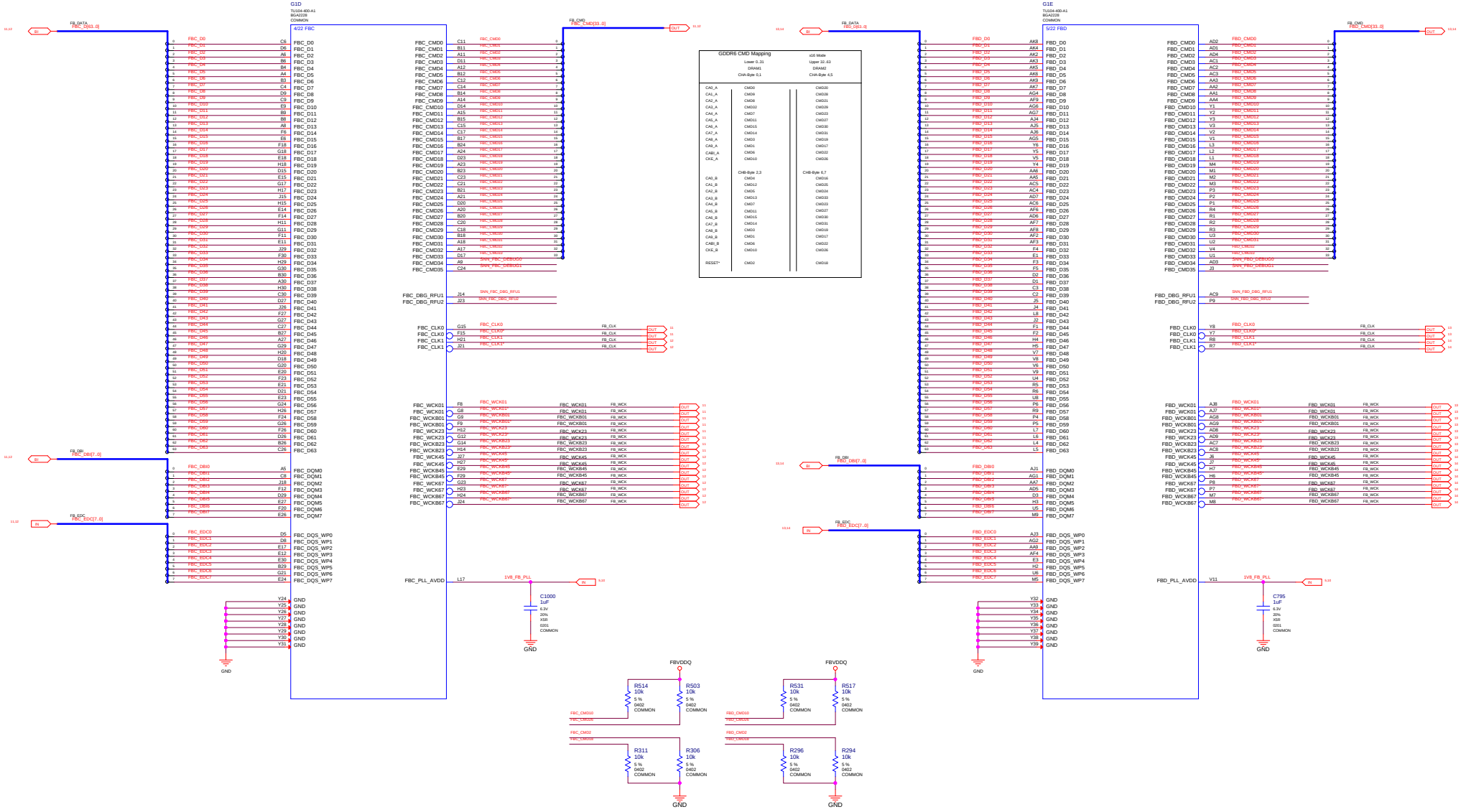
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 9 of 53

Page10: MEMORY: GPU Partition C/D



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PAGE DETAIL	MEMORY: GPU FB_CD

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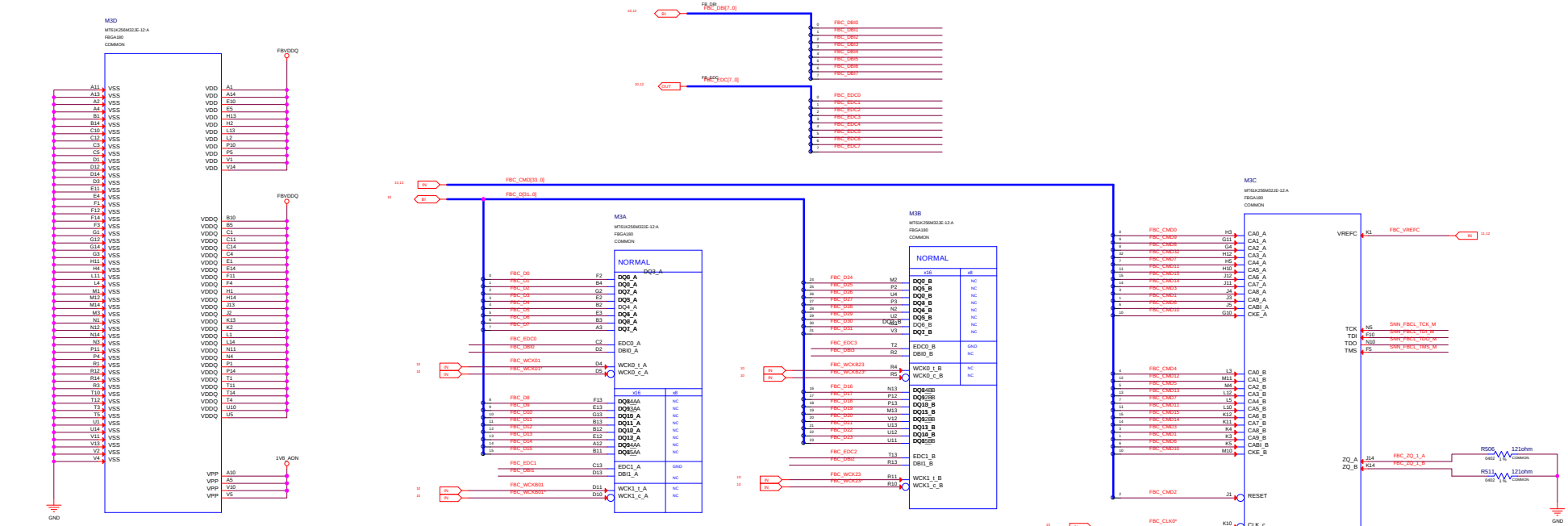
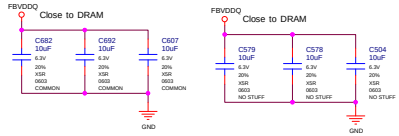
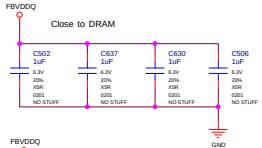
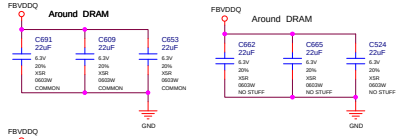
Size	Document Number	Rev
Custom	PG161H6-E10	A
Date: Wednesday, October 31, 2018	Sheet 10 of 53	

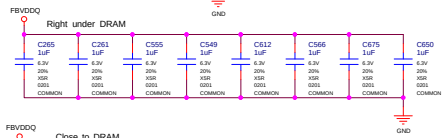
Page11: MEMORY: FBC Partition 31..0

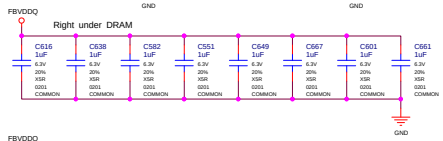


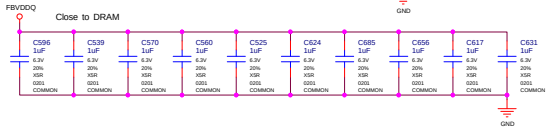


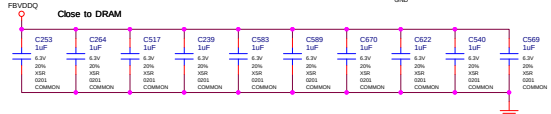




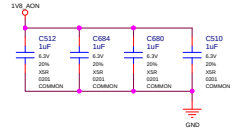








VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R75



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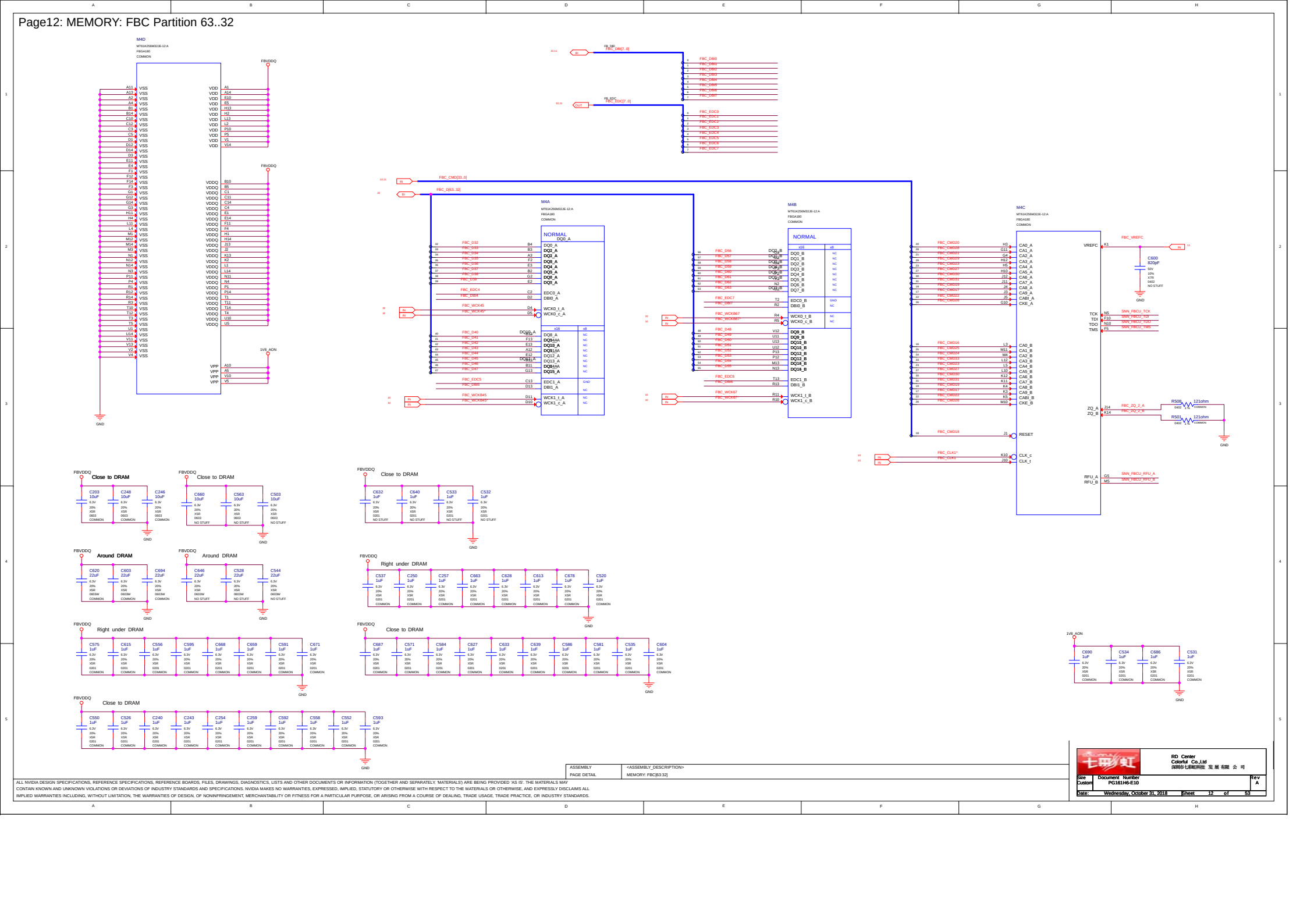
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 11 of 53

Page12: MEMORY: FBC Partition 63..32



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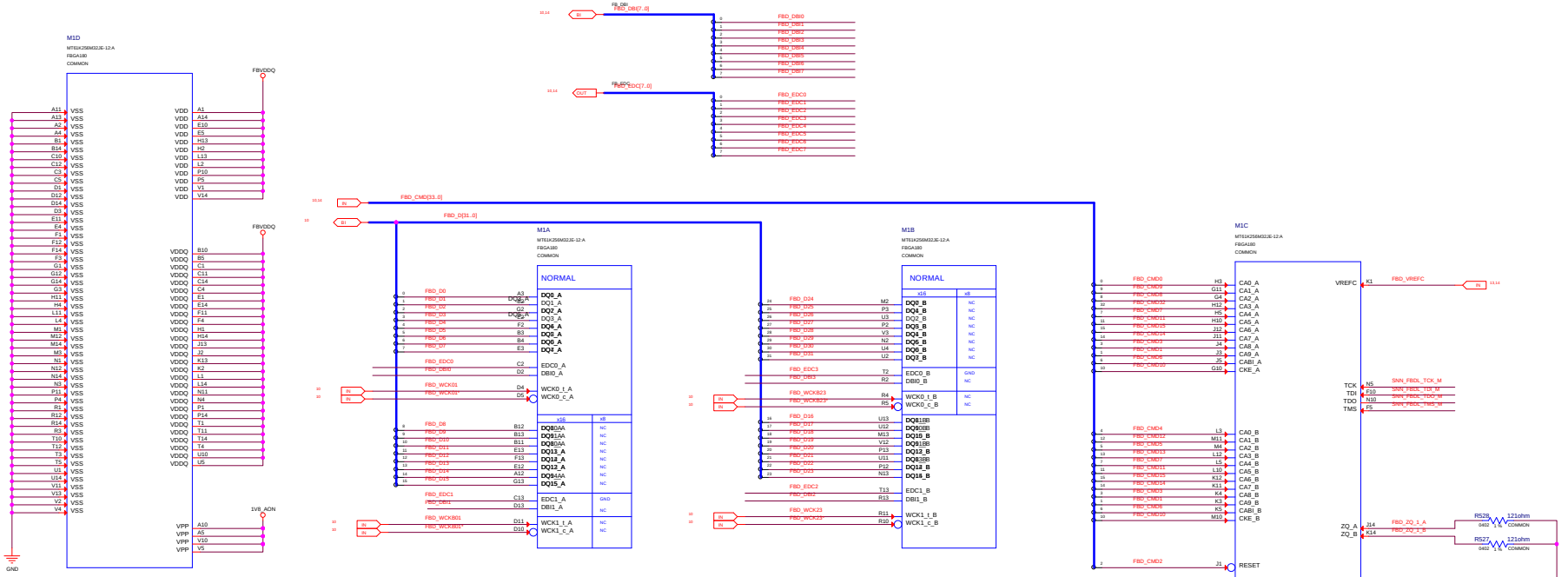
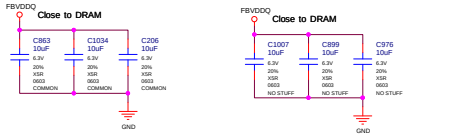
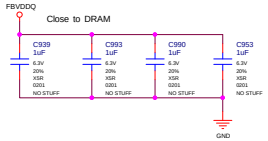
Size	Document Number	Rev
Custom	PG161H6-E10	A

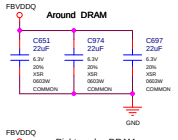
Date: Wednesday, October 31, 2018 | Sheet 12 of 53

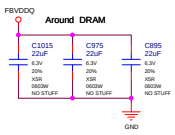
Page13: MEMORY: FBD Partition 31..0

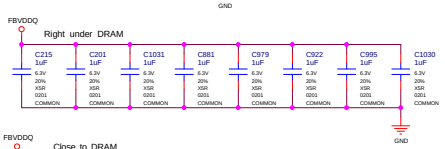


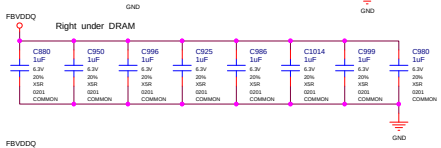


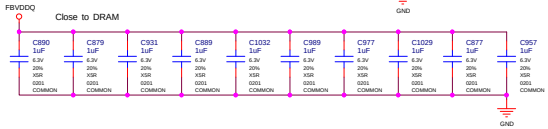


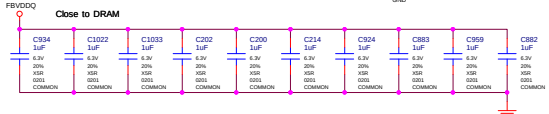




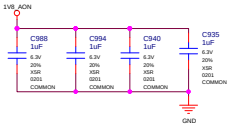








VREFC IS NOT USED IN x16 CONFIGURATION
1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R62



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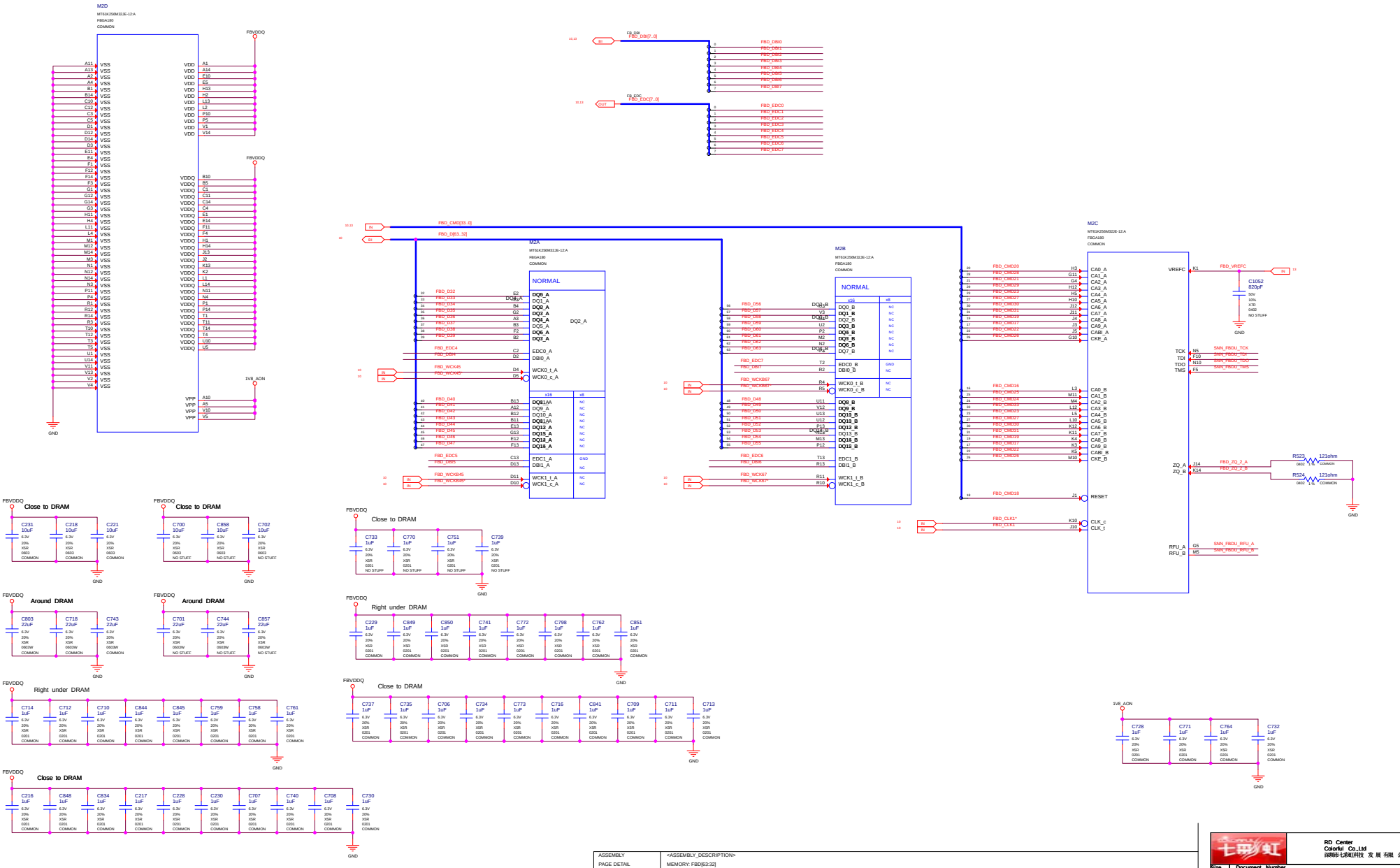
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 13 of 53

Page14: MEMORY: FBD Partition 63..32



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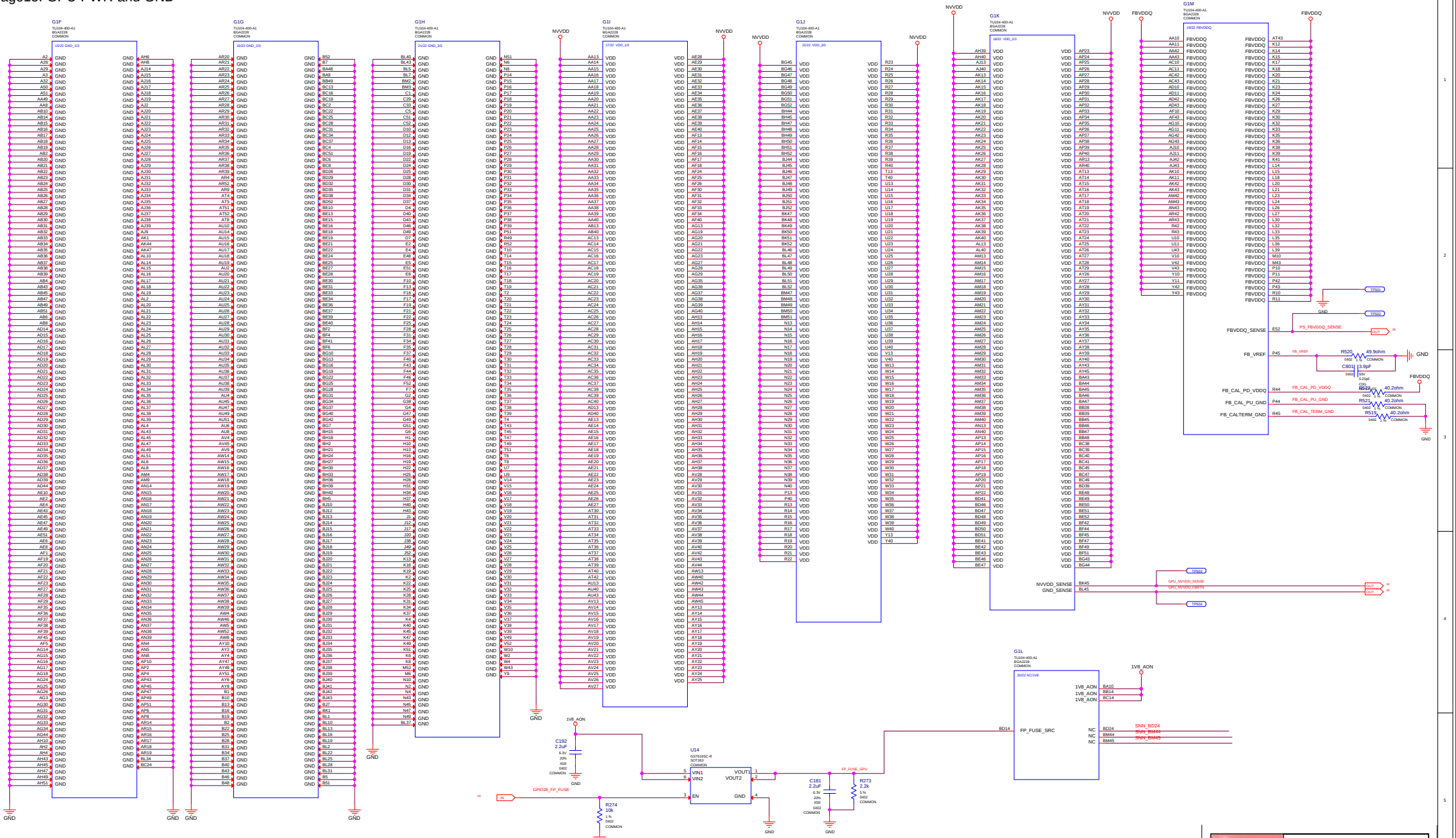
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 14 of 53

Page15: GPU PWR and GND



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PAGE DETAIL	GPU PWR & GND

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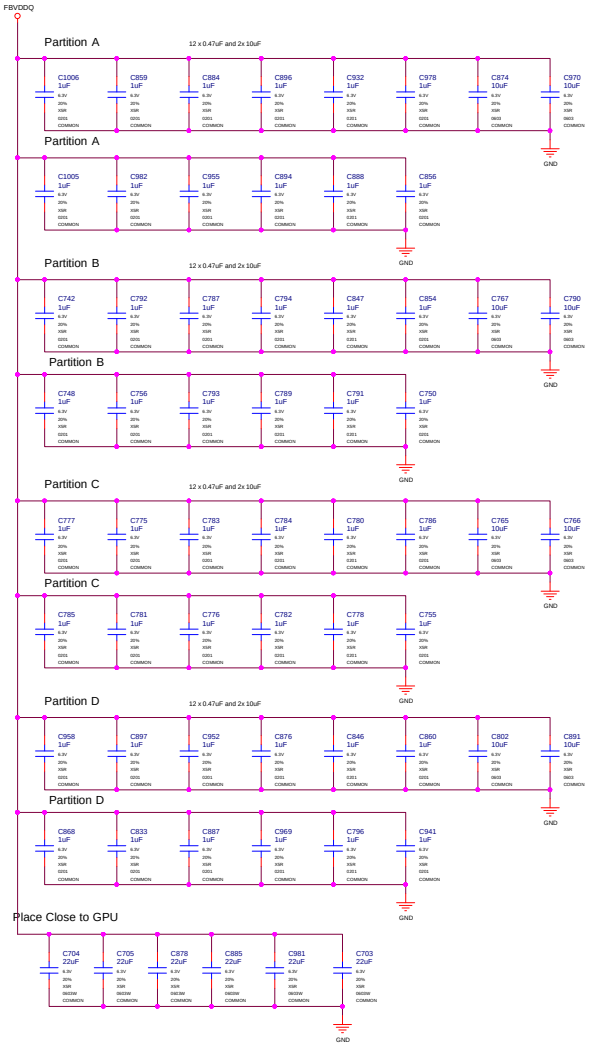
Size	Document Number	Rev
Custom	PG161H6-E10	A

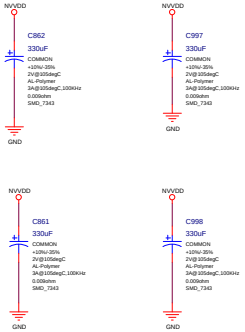
Date: Wednesday, October 31, 2018 Sheet 15 of 53

Page16: GPU Decoupling 1

FBVDDQ



NVVDD



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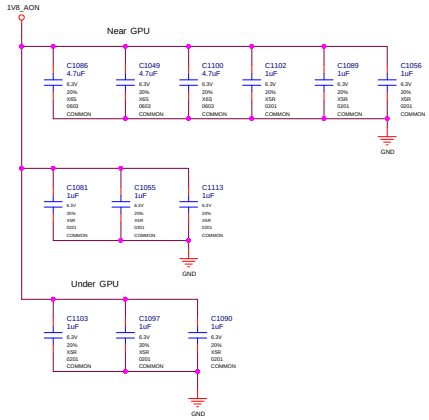

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PAGE DETAIL	GPU Decoupling

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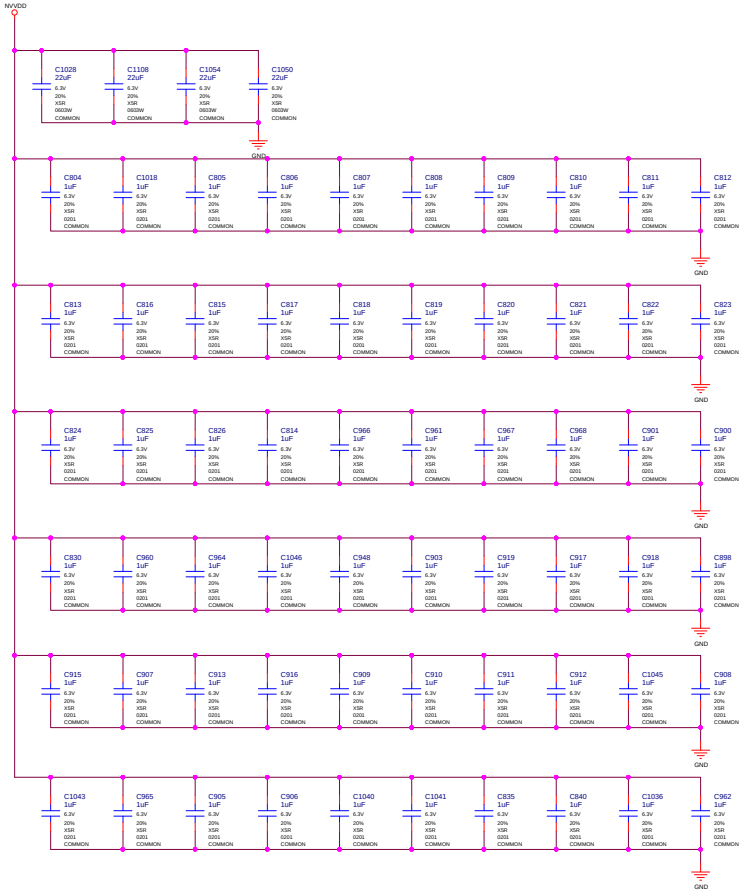
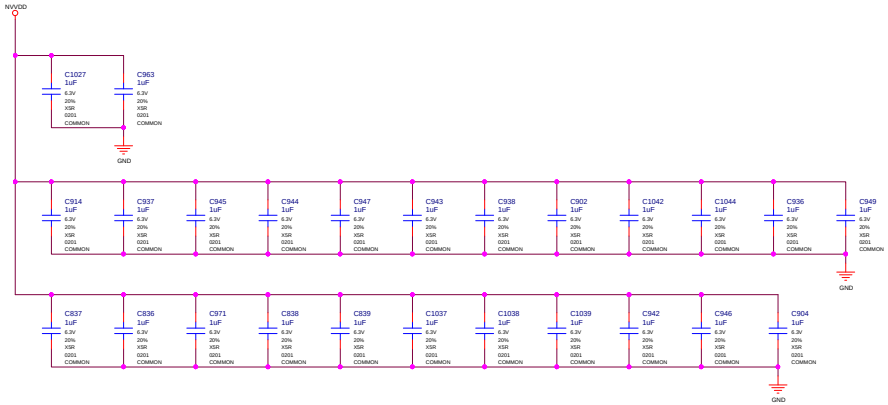
Size	Document Number	Rev
Custom	PG161H5-E10	A

Date: Wednesday, October 31, 2018 Sheet 16 of 53

Page17: GPU Decoupling 2

NVVDD





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PAGE DETAIL	GPU Decoupling2

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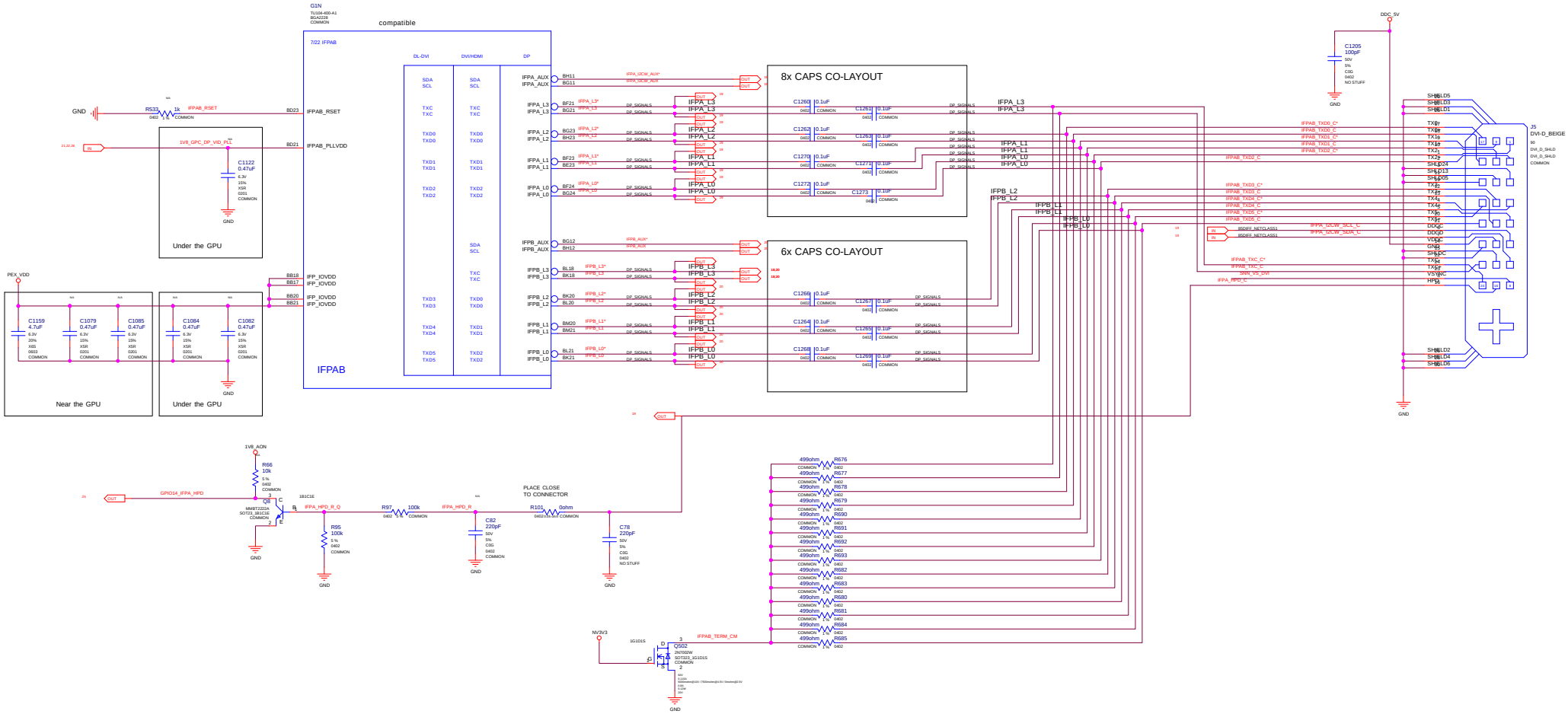
Size	Document Number	Rev
Custom	PG161H6-E10	A
Date: Wednesday, October 31, 2018	Sheet 17 of 53	

IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPAB DVI-D-DL

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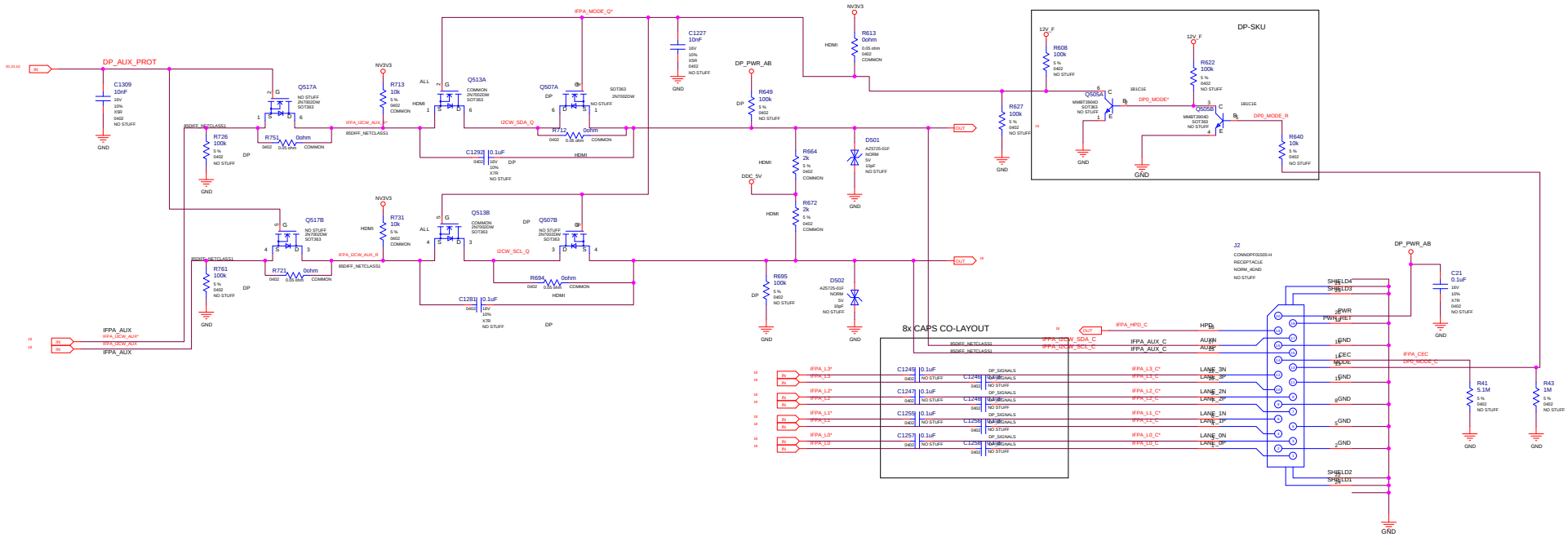
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 18 of 53



IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

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PAGE DETAIL	IO: IFPA DP

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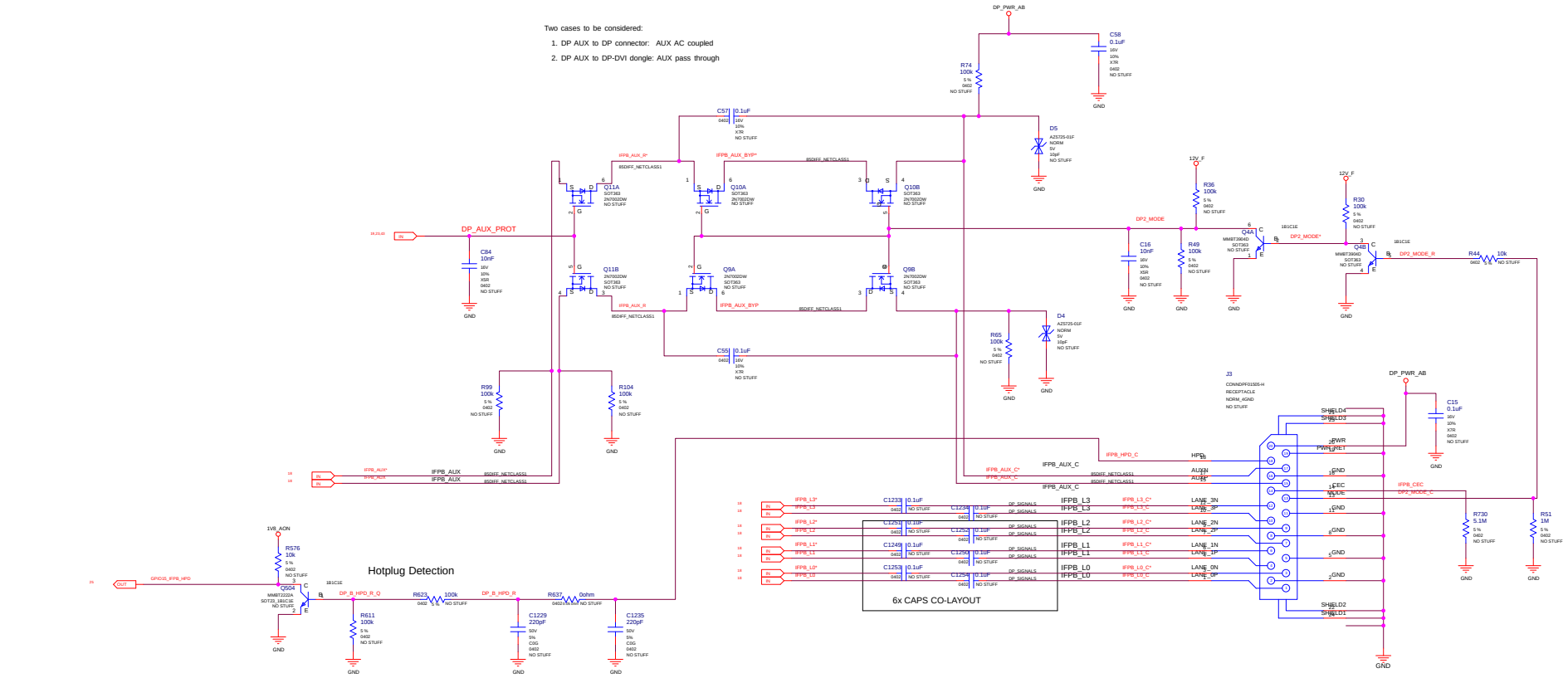
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 19 of 53

IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL



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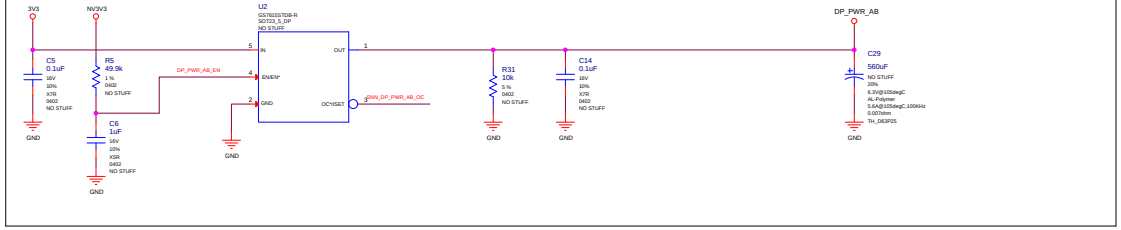

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PAGE DETAIL	IO: IFPB DP

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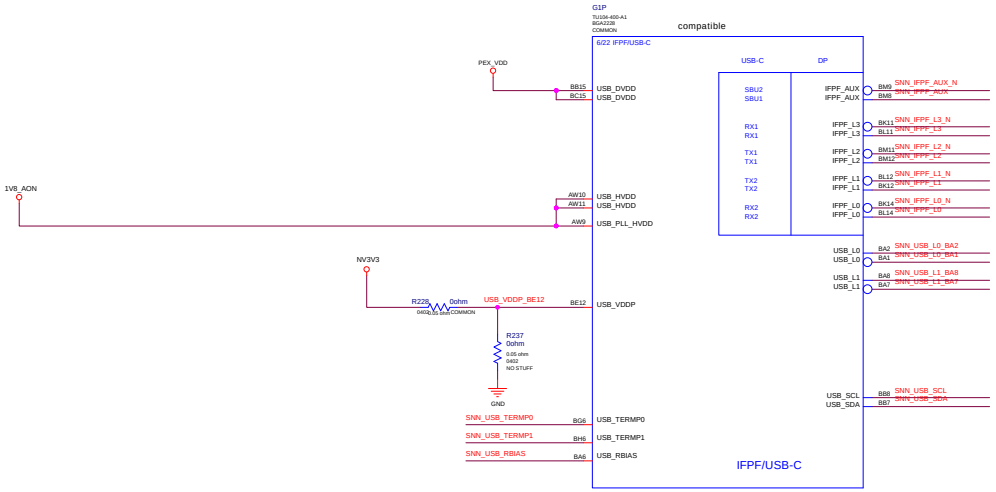
Size	Document Number	Rev
Custom	PG161H6-E10	A
Date: Wednesday, October 31, 2018	Sheet 20 of 53	



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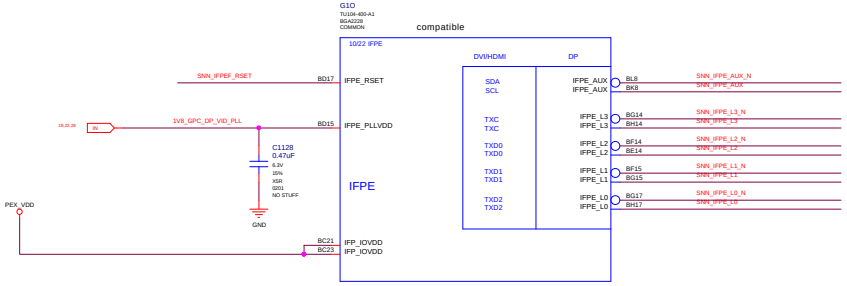

IFPE NC

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IO: IFPE & IFPF USBC NC

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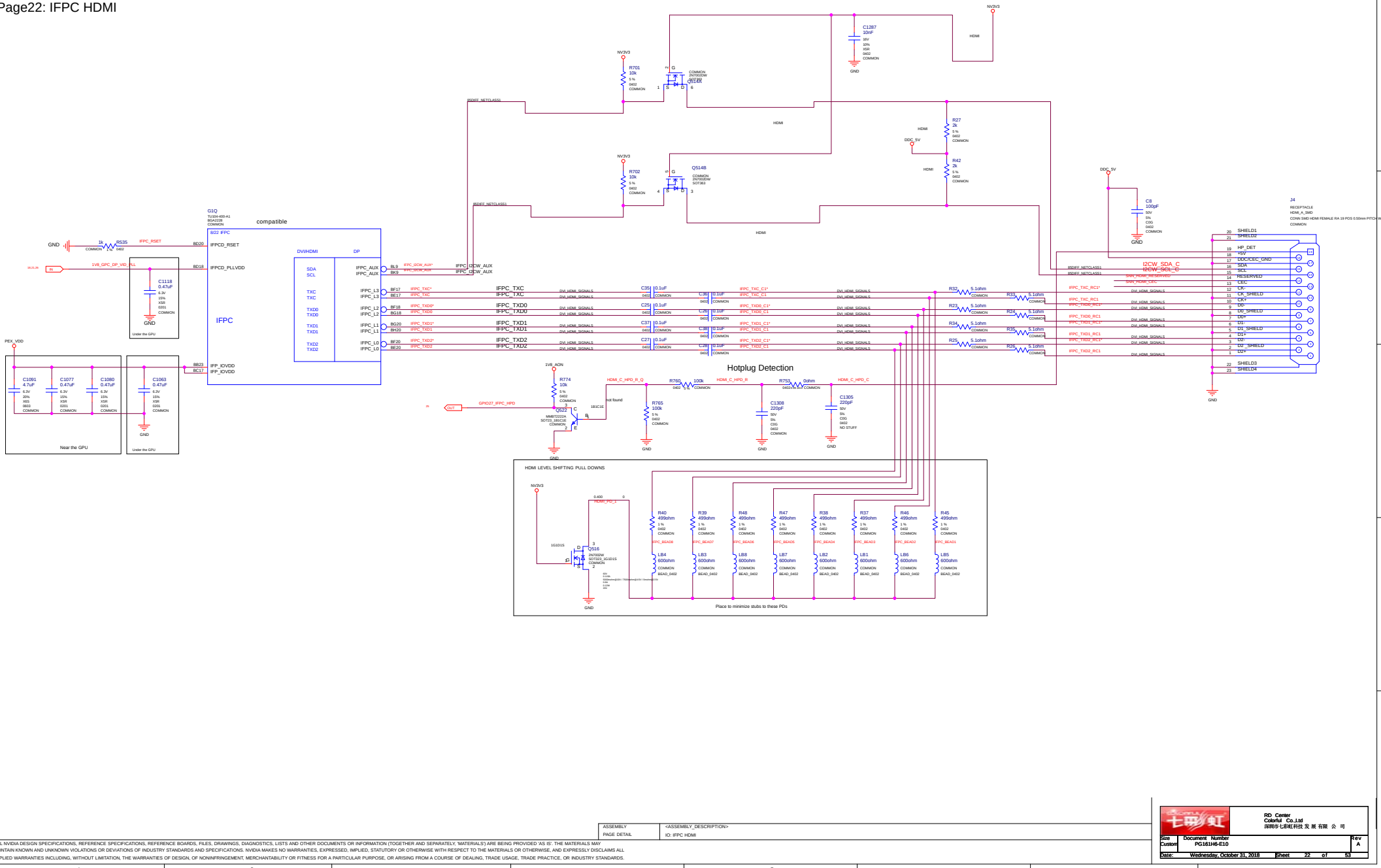
Size: Custom | Document Number: PG161H6-E10 | Rev: A
Date: Friday, November 09, 2018 | Sheet 21 of 53

21-OCT-2018

Page22: IFPC HDMI



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPC HDMI

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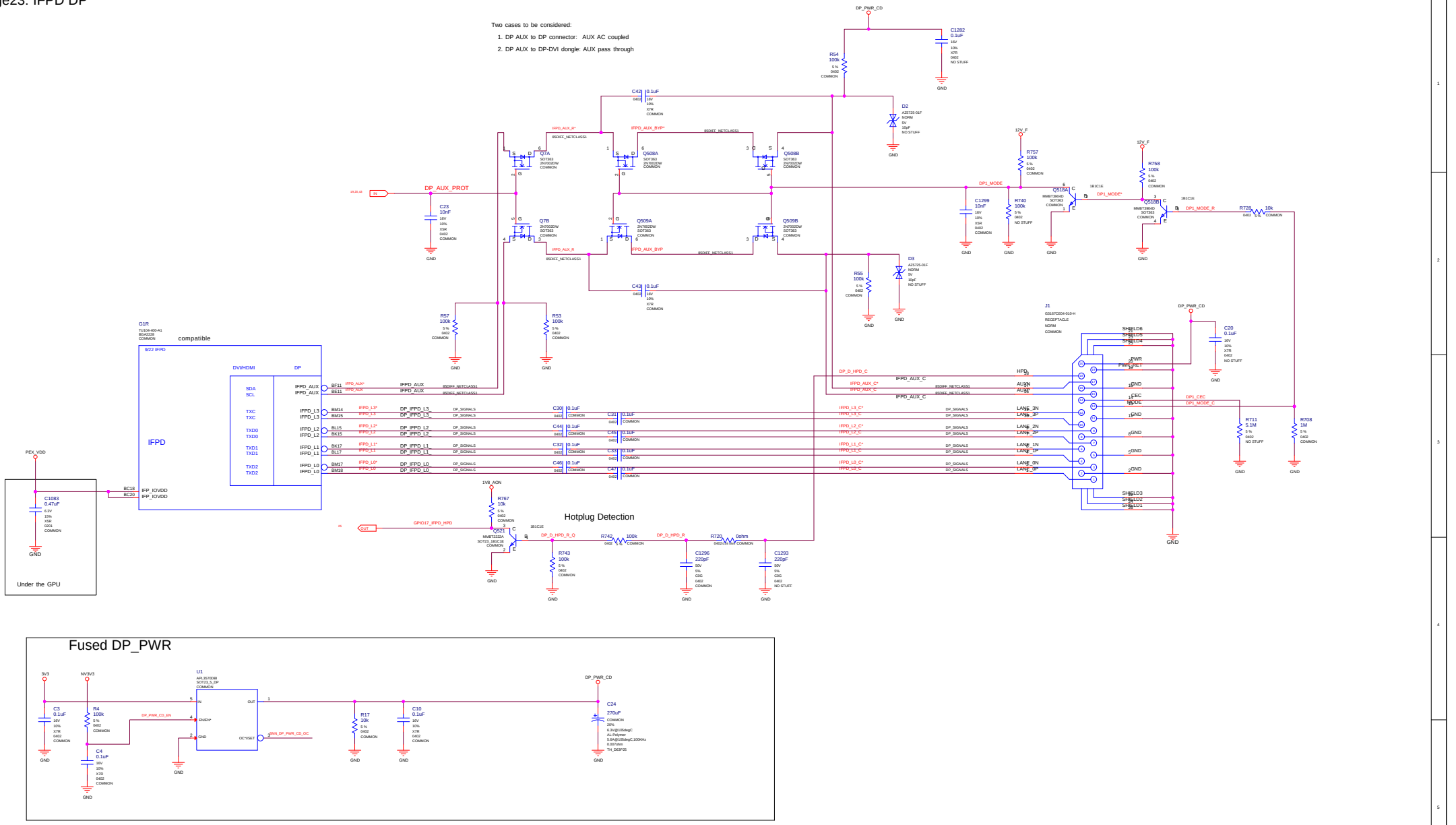
Size	Document Number	Rev
Custom	PG161H6-E10	A
Date:	Wednesday, October 31, 2018	Sheet 22 of 53

Page23: IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPD DP

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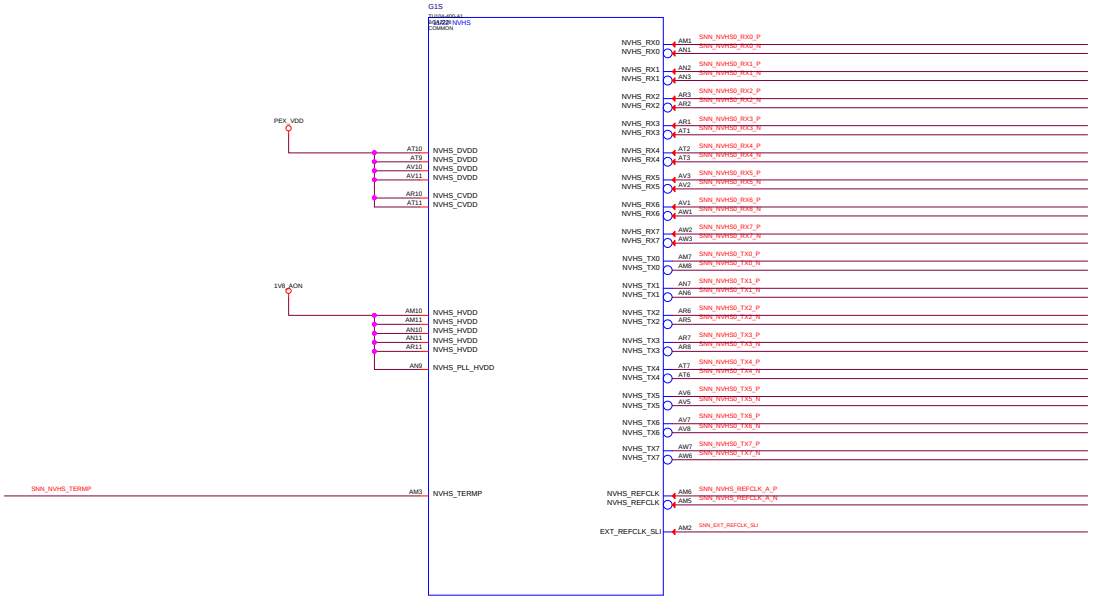
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 23 of 53

Page24: NVHS Interface and Frame Lock



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: NVHS Interface and Frame Lock

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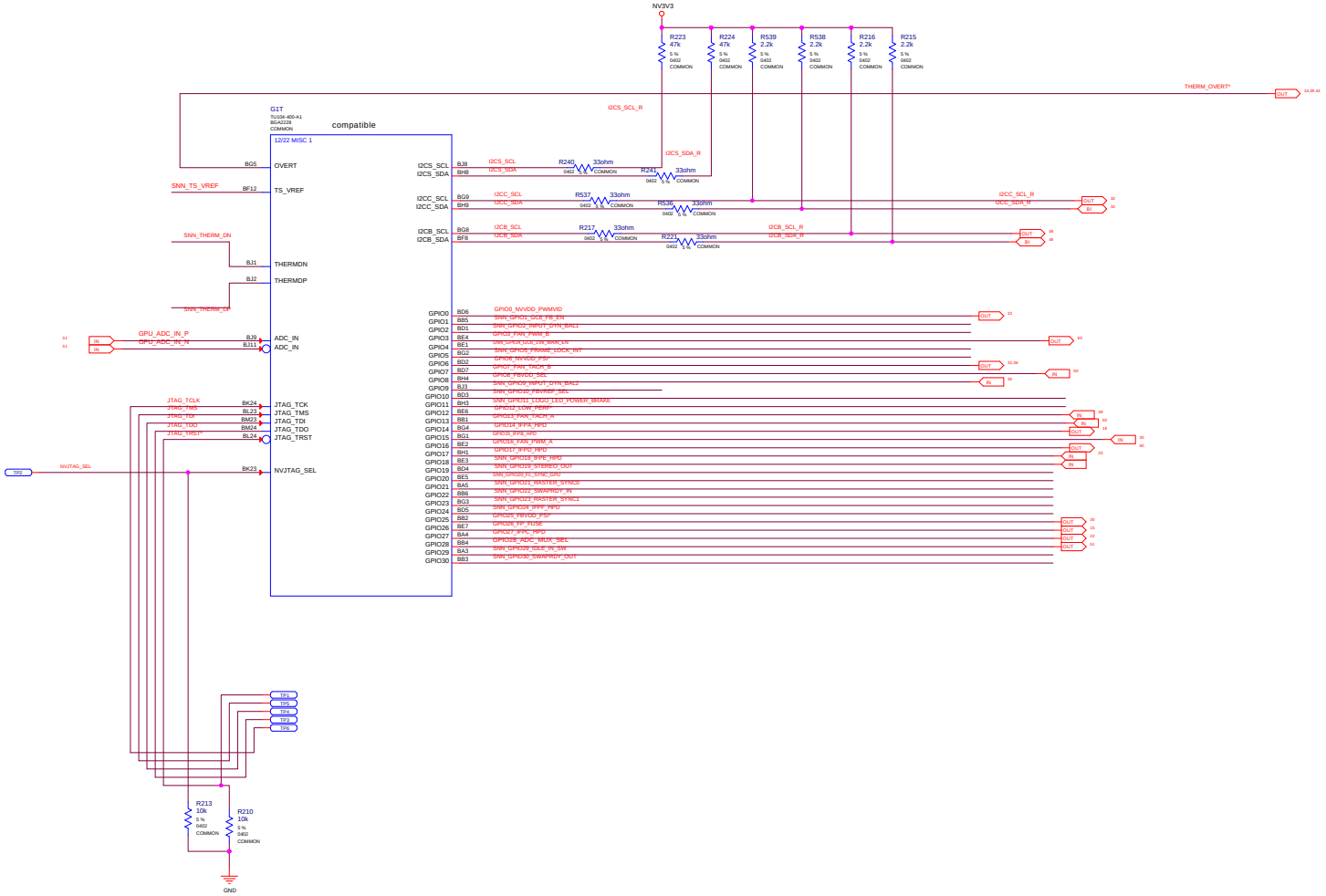
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 24 of 53

Page25: MISC1: Fan, Thermal, JTAG, GPIO



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: Thermal, JTAG, GPIO,STEREO

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Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 25 of 53

Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

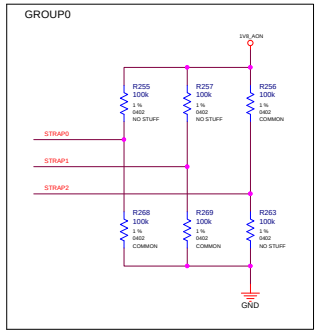
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

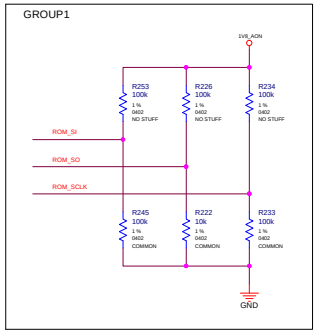
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

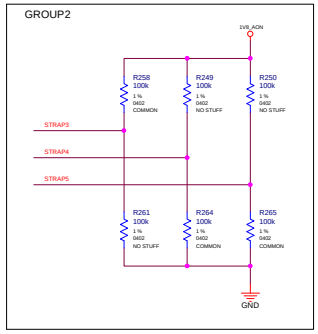
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

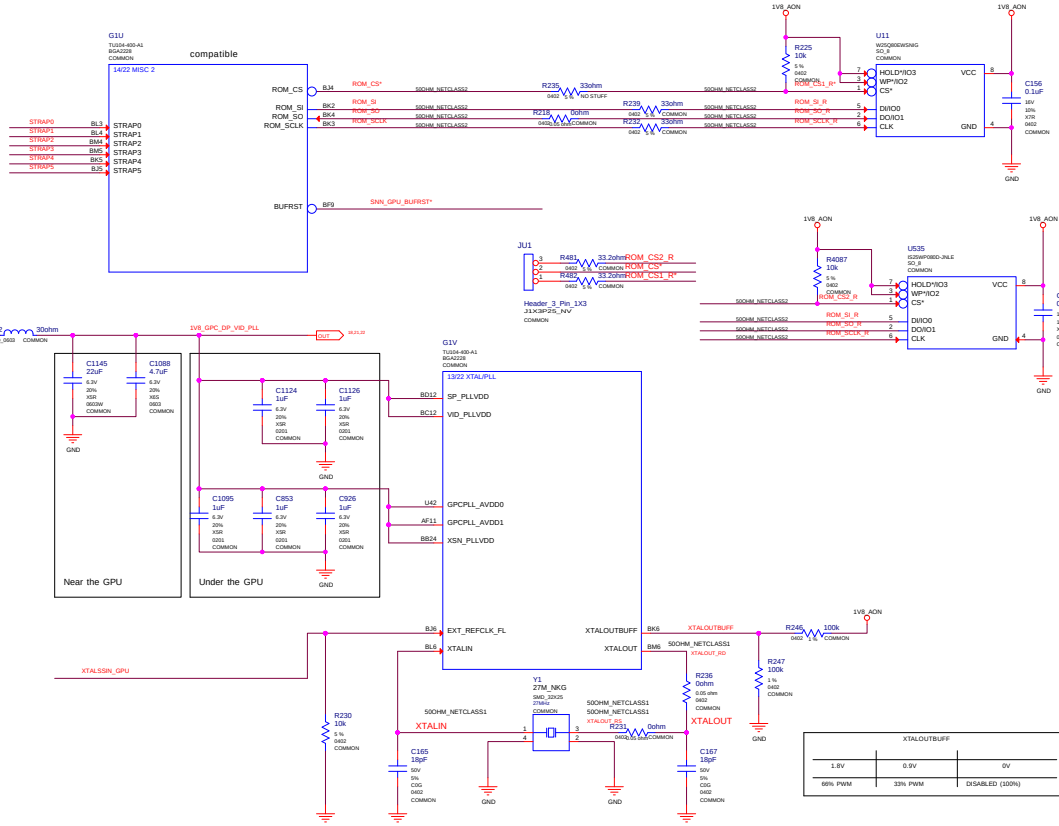
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE









ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL,STRAPS

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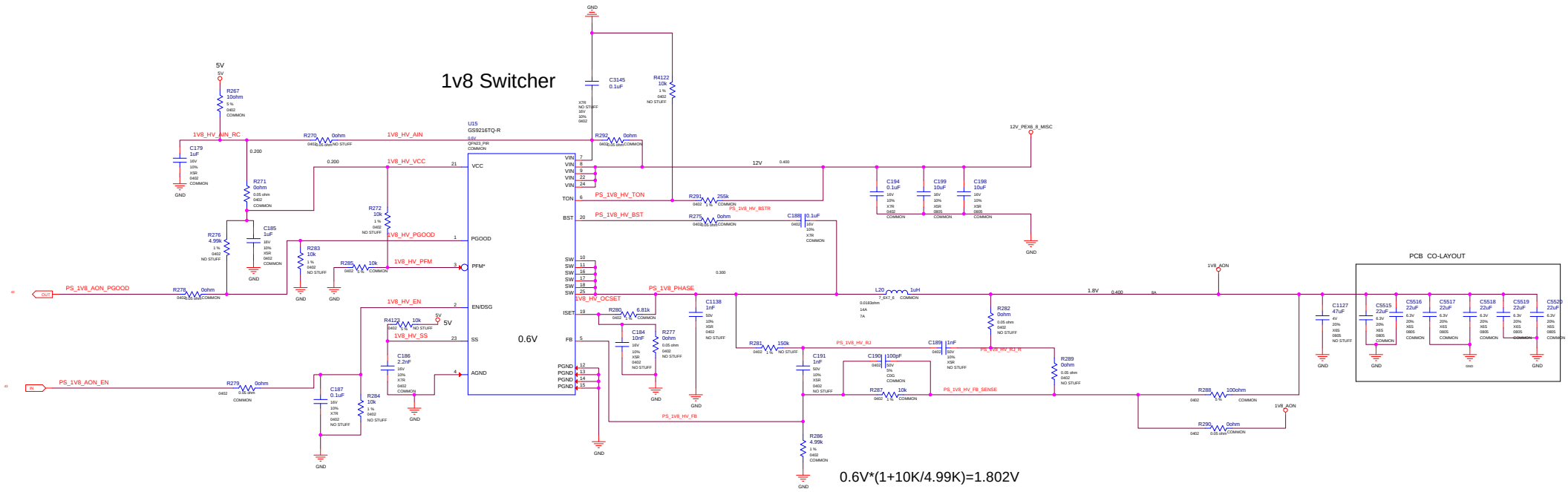
Size	Document Number	Rev
Custom	PG161H6-E10	A
Date: Wednesday, October 31, 2018	Sheet 26 of 53	

Page27: PS: 1V8_AON



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PAGE DETAIL	PS: 1V8_AON

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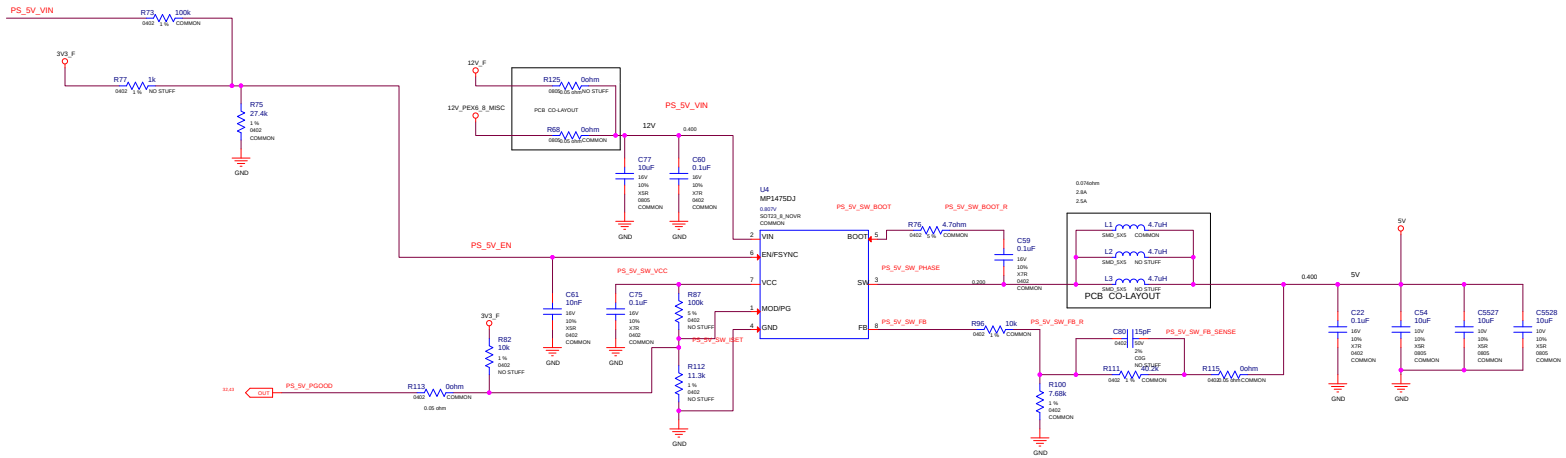
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Friday, November 09, 2018 Sheet 27 of 53



0.8V*(1+40.2K/7.68K)=4.9875V

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 5V

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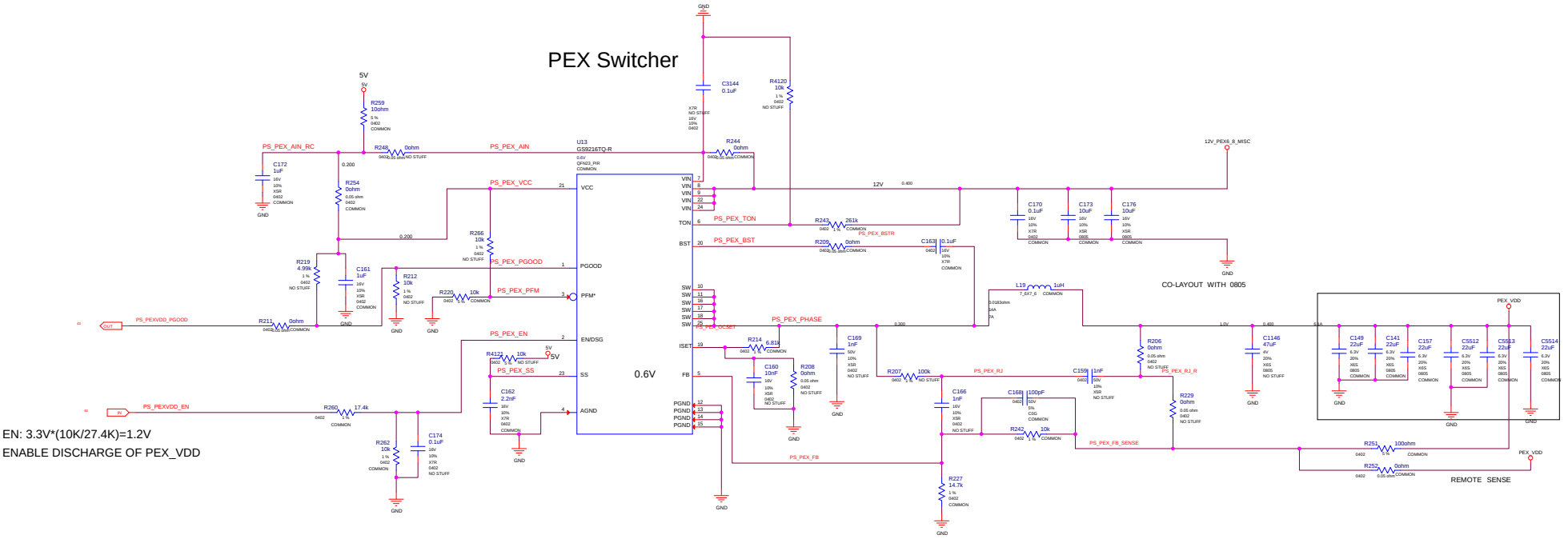
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Tuesday, November 06, 2018 Sheet 28 of 53

PEX Switcher



EN: 3.3V*(10K/27.4K)=1.2V

ENABLE DISCHARGE OF PEX_VDD

0.6V*(1+10K/14.7K)=1.008V

ASSEMBLY <ASSEMBLY_DESCRIPTION>

PAGE DETAIL PS: PEXVDD

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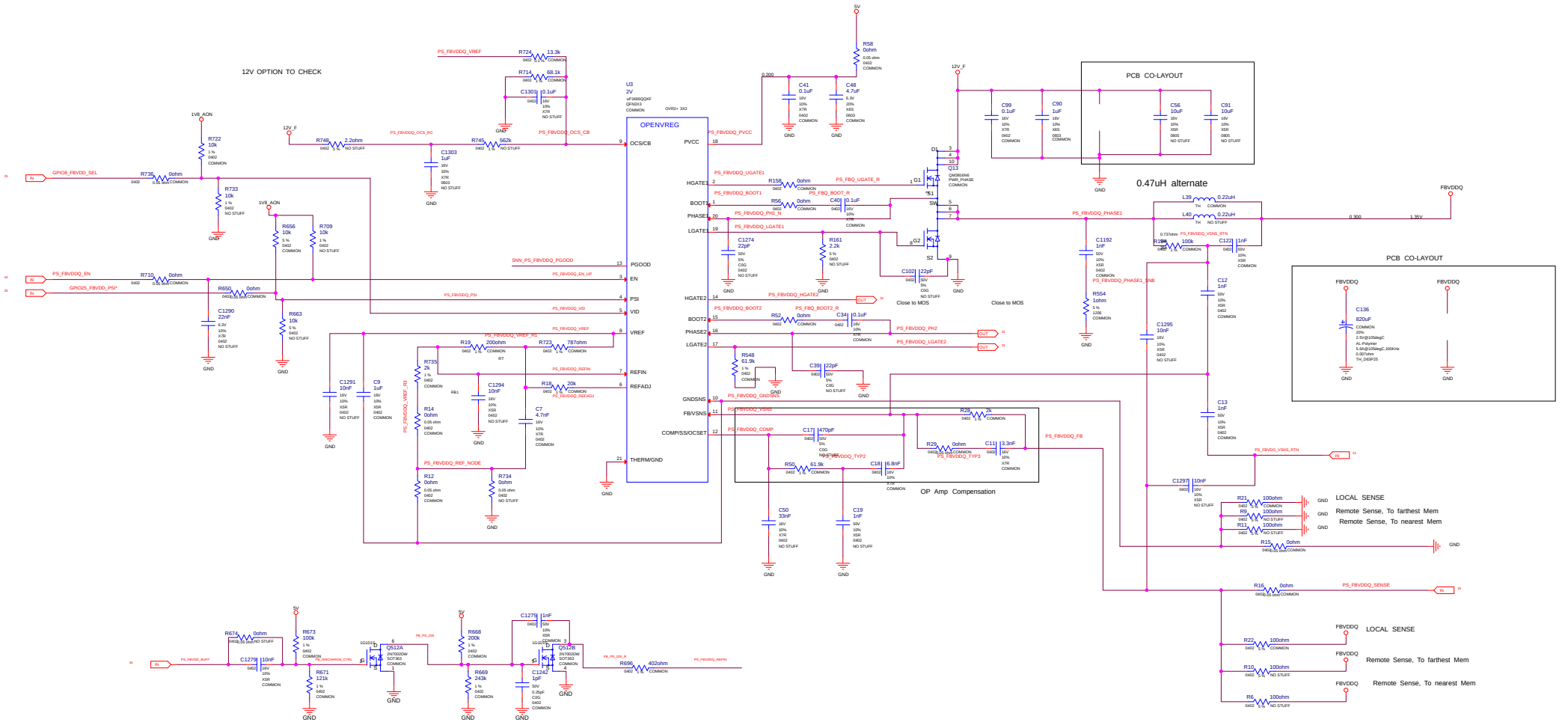
Size: Custom | Document Number: PG161H6-E10 | Rev: A

Date: Friday, November 09, 2018 | Sheet 29 of 53

Page30: PS: FBVDDQ



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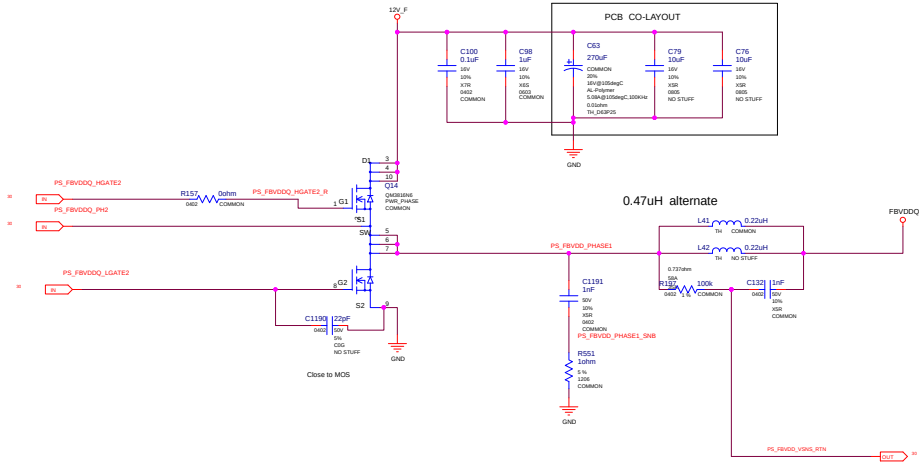
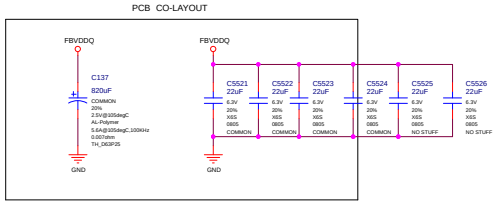
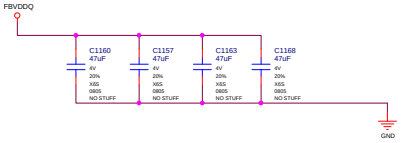
Size	Document Number	Rev
Custom	PG161H6-E10	A

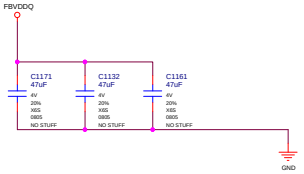
Date: Wednesday, October 31, 2018 Sheet 30 of 53

Page31: PS: FBVDDQ PH2









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PAGE DETAIL	PS: FBVDDQ PH2

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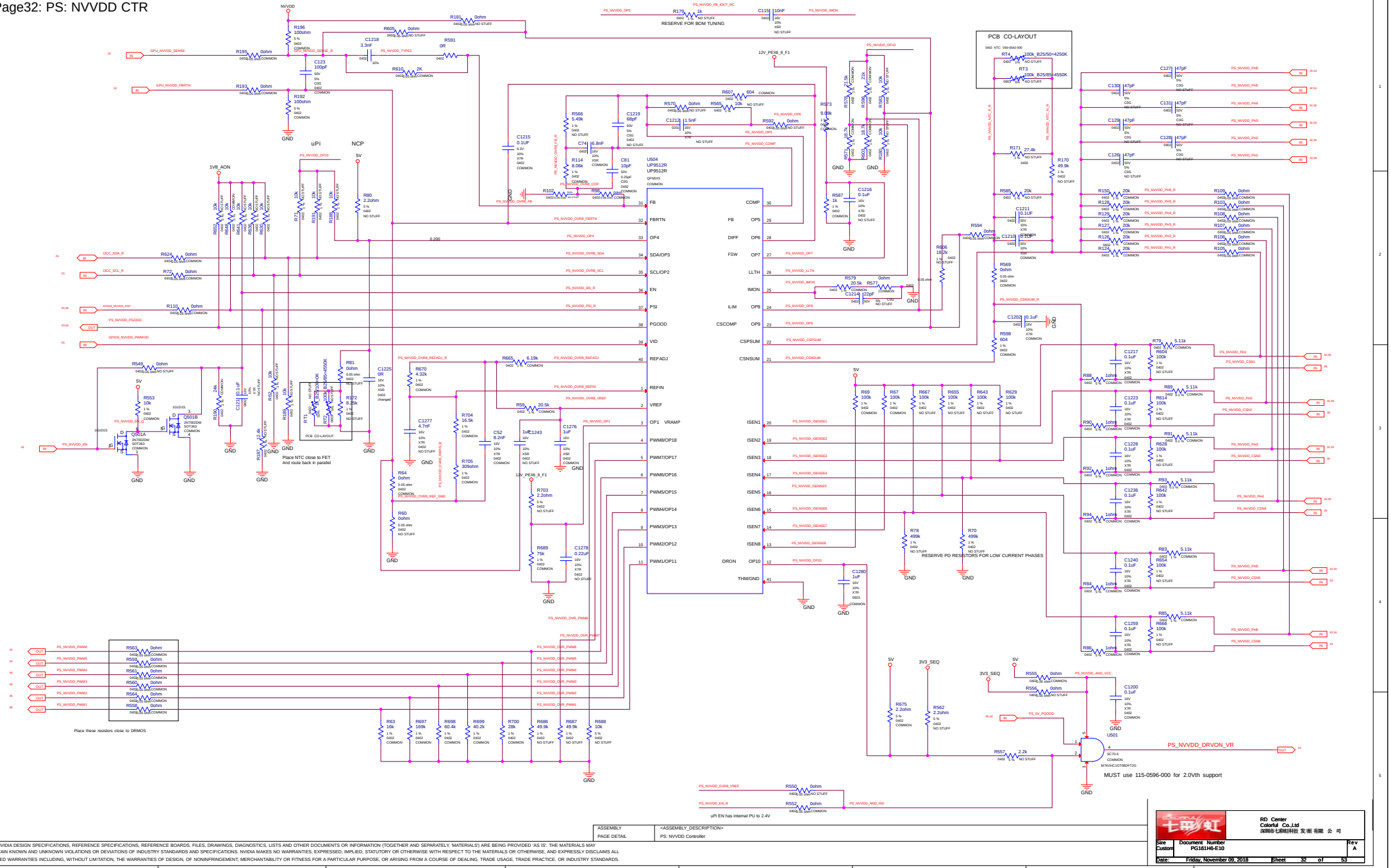
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 31 of 53

Page32: PS: NVVDD CTR



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Controller

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Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Friday, November 09, 2018 Sheet 32 of 53

DROP OVR3i SOLUTION

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Controller OVR3i

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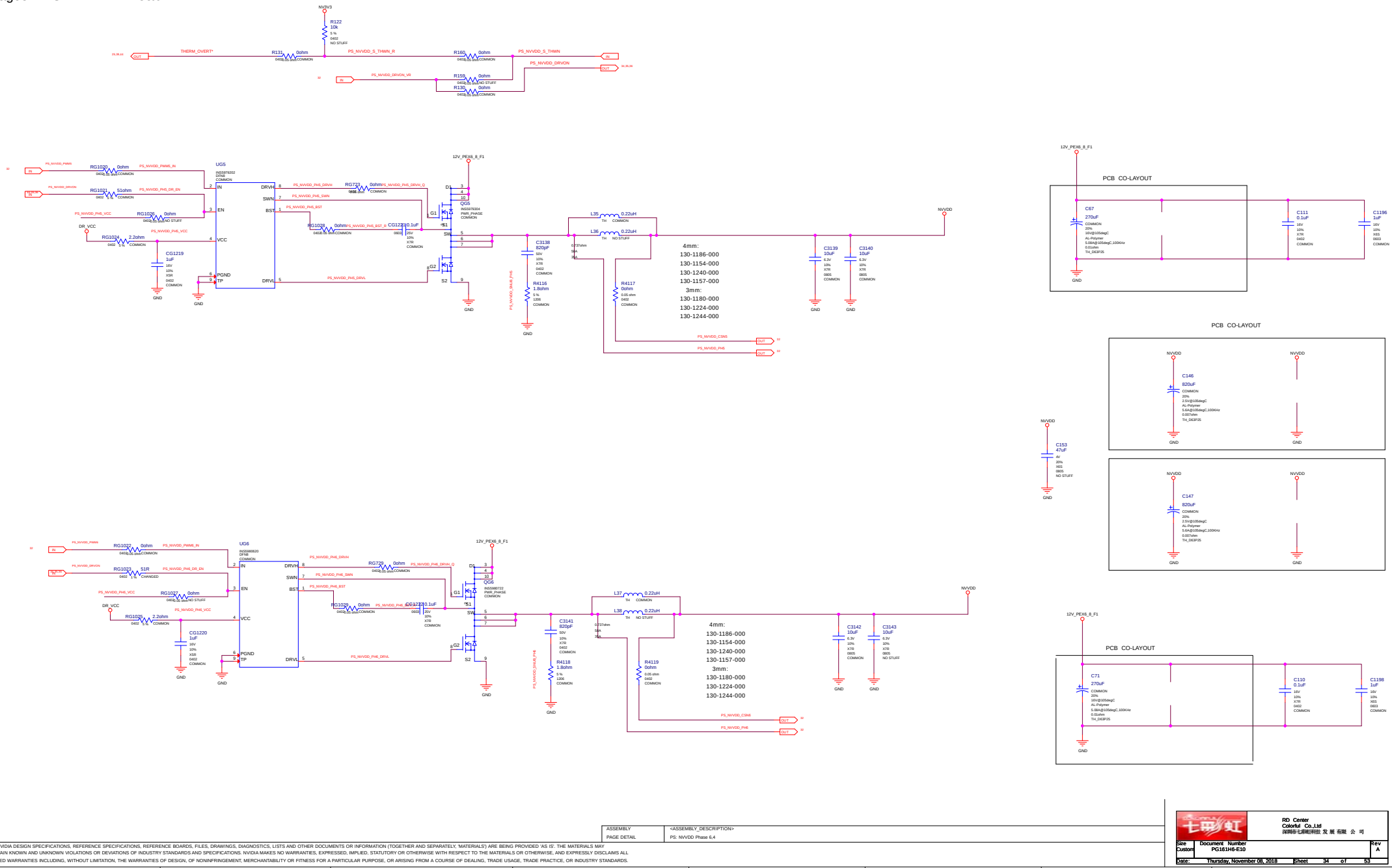
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 33 of 53

Page34: PS: NVVDD PH5&6



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 6,4

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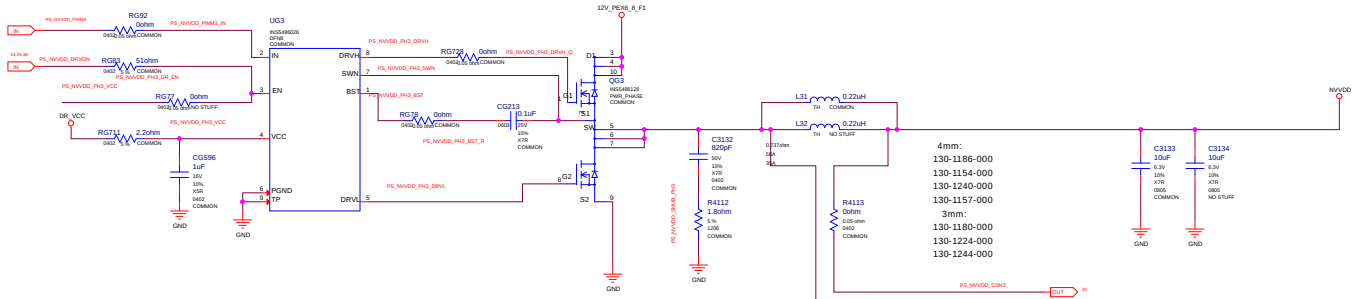
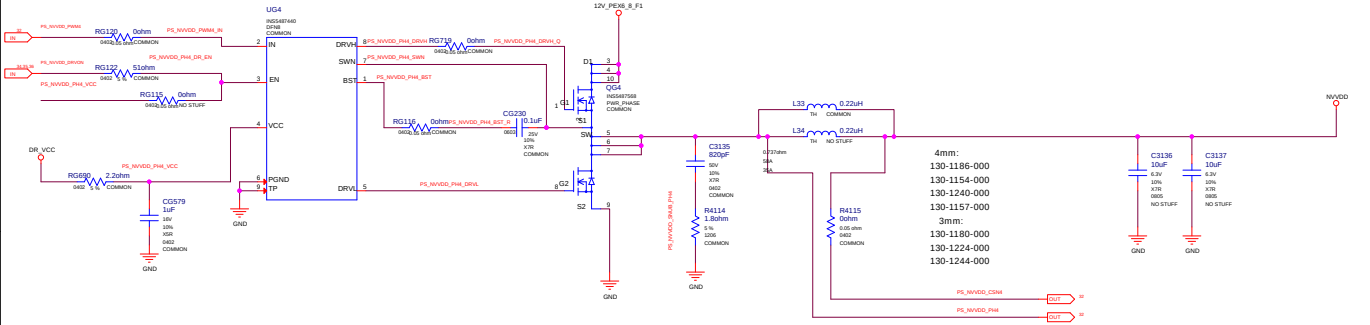
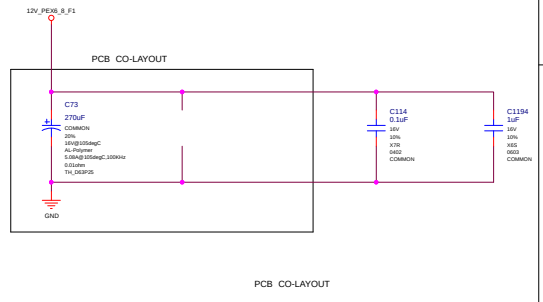
Size	Document Number	Rev
Custom	PG161H6-E10	A

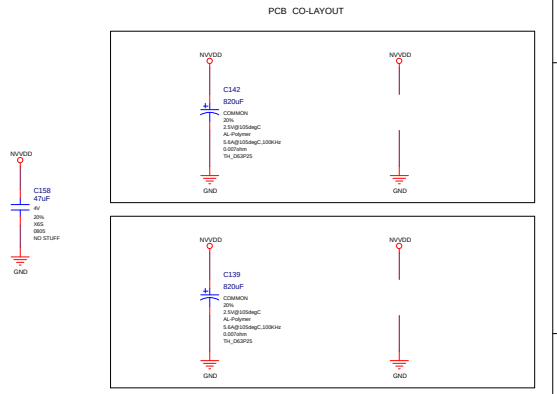
Date: Thursday, November 08, 2018 Sheet 34 of 53

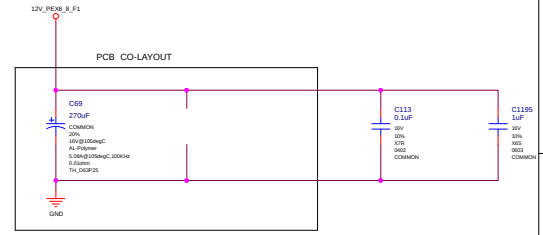
Page35: PS: NVVDD PH3&4











ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 3,5

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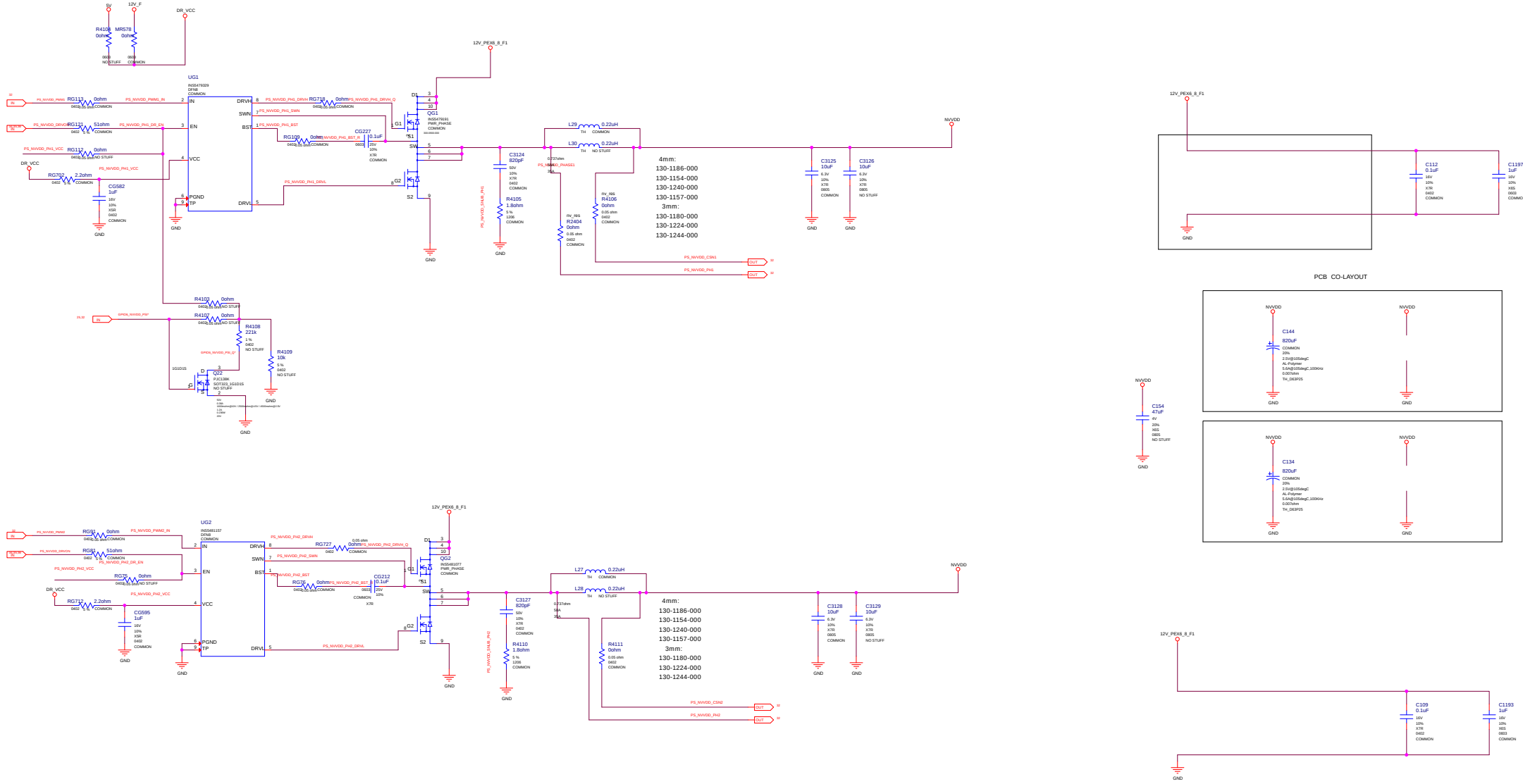
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 35 of 53

Page36: PS: NVVDD PH2&1



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PAGE DETAIL	PS: NVVDD Phase 2,1

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Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 36 of 53

DELETE RAIL BALANCE CIRCUIT

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Input Power Balancing Switcher

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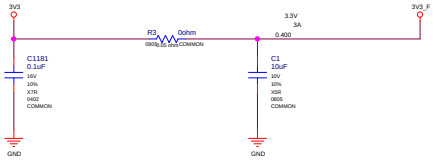
Size	Document Number	Rev
Custom	PG161H6-E10	A

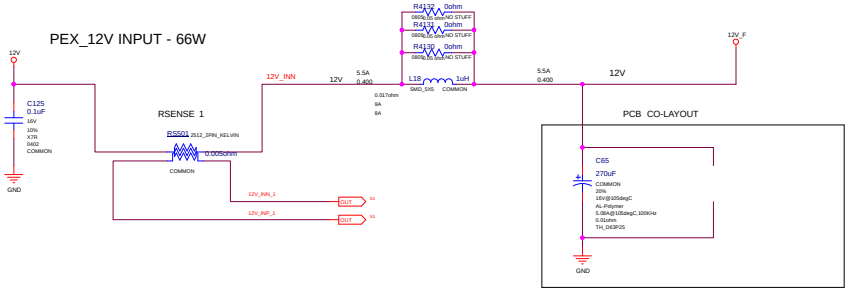
Date: Wednesday, October 31, 2018 Sheet 37 of 53

Page38: PS: Inputs, Filtering, and Monitoring

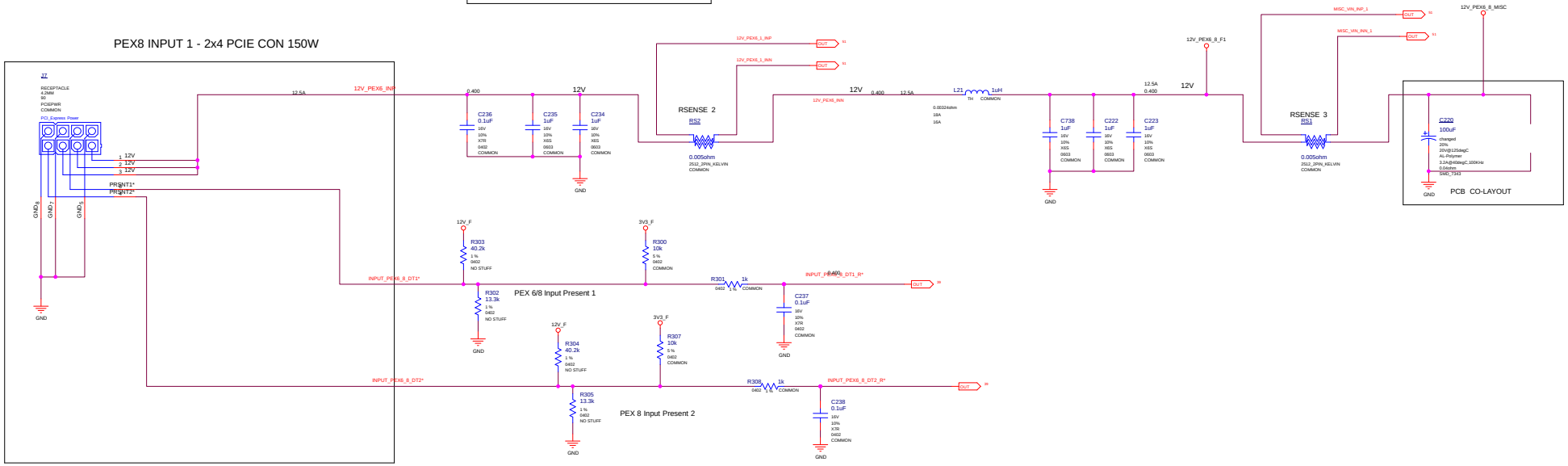
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Input, Filtering, and Monitoring

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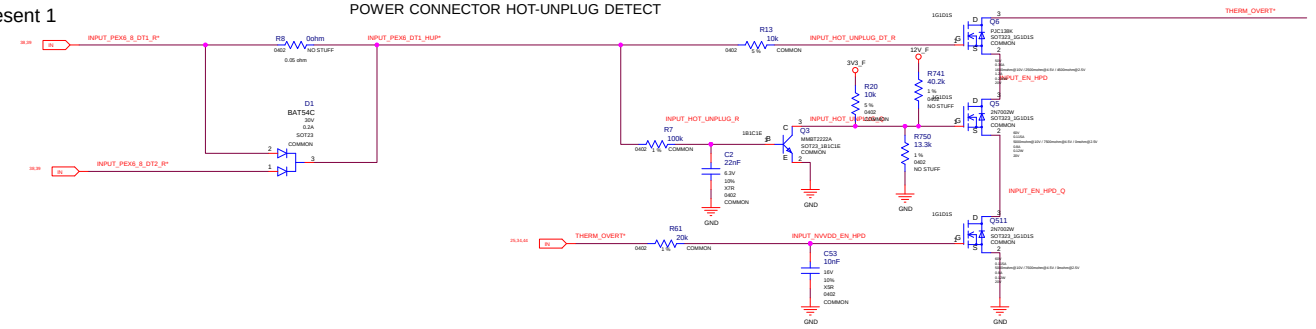
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Thursday, November 01, 2018 Sheet 38 of 53

Page39: PS: HOT-UNPLUG, UNDER POWER BOOT, CURRENT STEERING

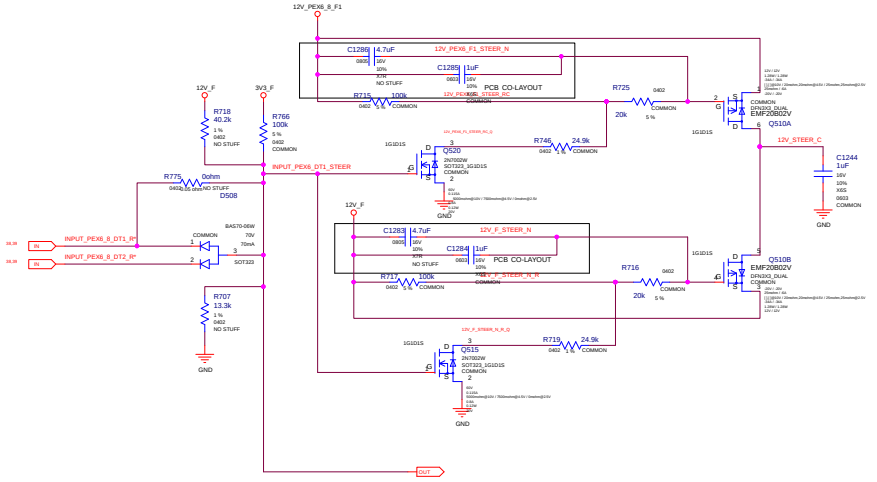
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

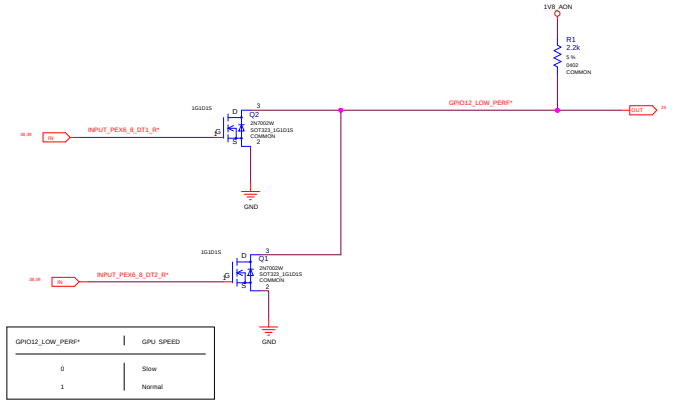


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: STEERING, UPB & HOT-UNPLUG

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Size: Custom | Document Number: PG161H6-E10 | Rev: A
Date: Thursday, November 08, 2018 | Sheet 39 of 53

Page40: BUCKBOOST

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Type-C BuckBoost

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Size: Custom	Document Number: PG161H6-E10	Rev: A
Date: Wednesday, October 31, 2018	Sheet 40 of 53	

Page41: PPC

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PD PPC

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Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 41 of 53

Page42: 12V & 3V3_A SWITCHER

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 12V & 3V3_A SWITCHER

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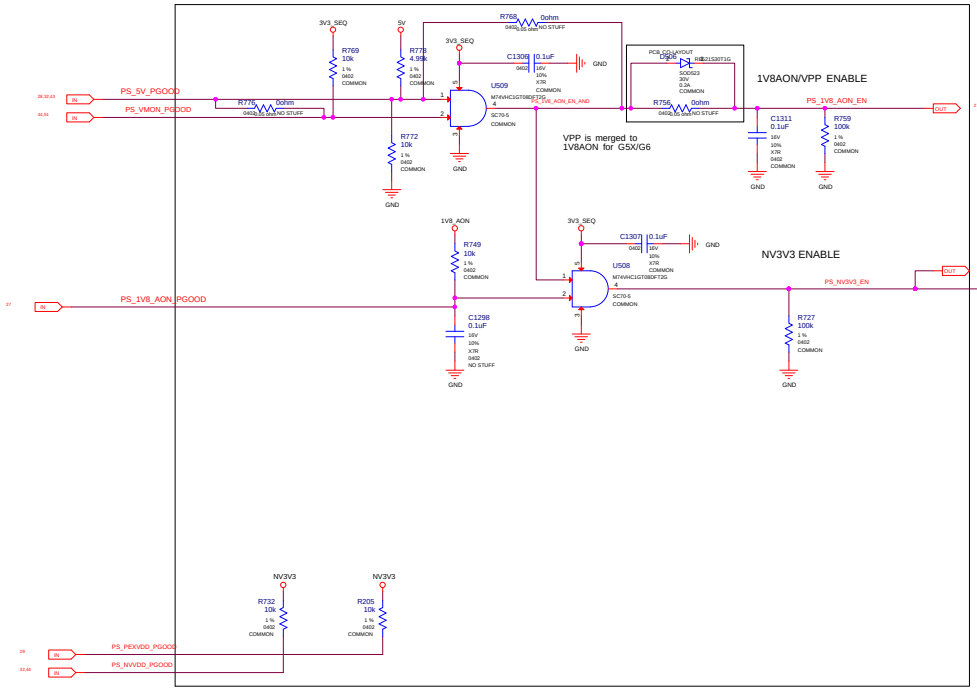
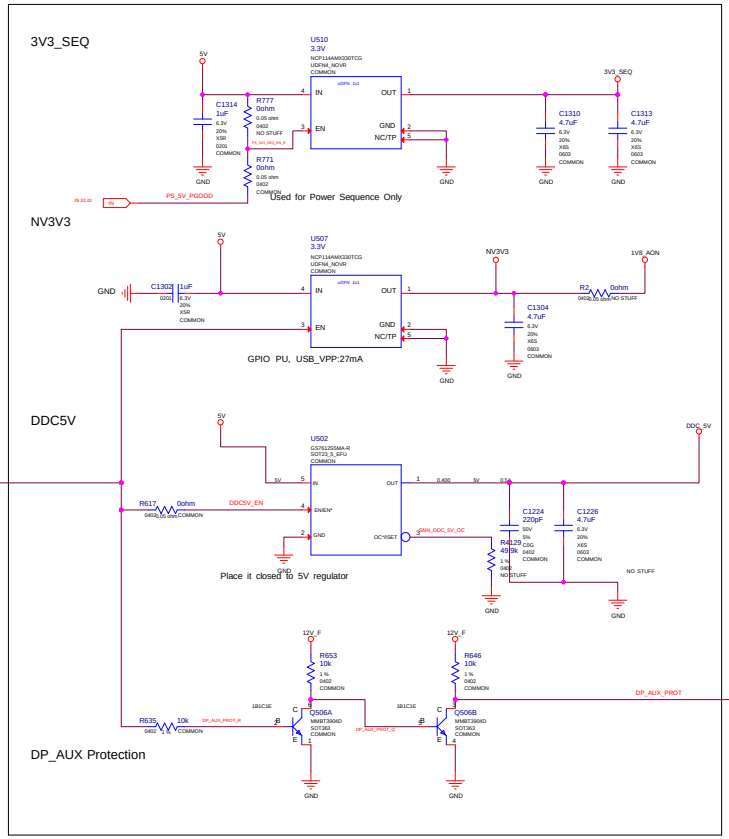
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 42 of 53

Page43: SEQ:5V,1V8,NV3V3 ENABLE





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PAGE DETAIL	SEQ: 5V, 1V8, NV3V3 ENABLE

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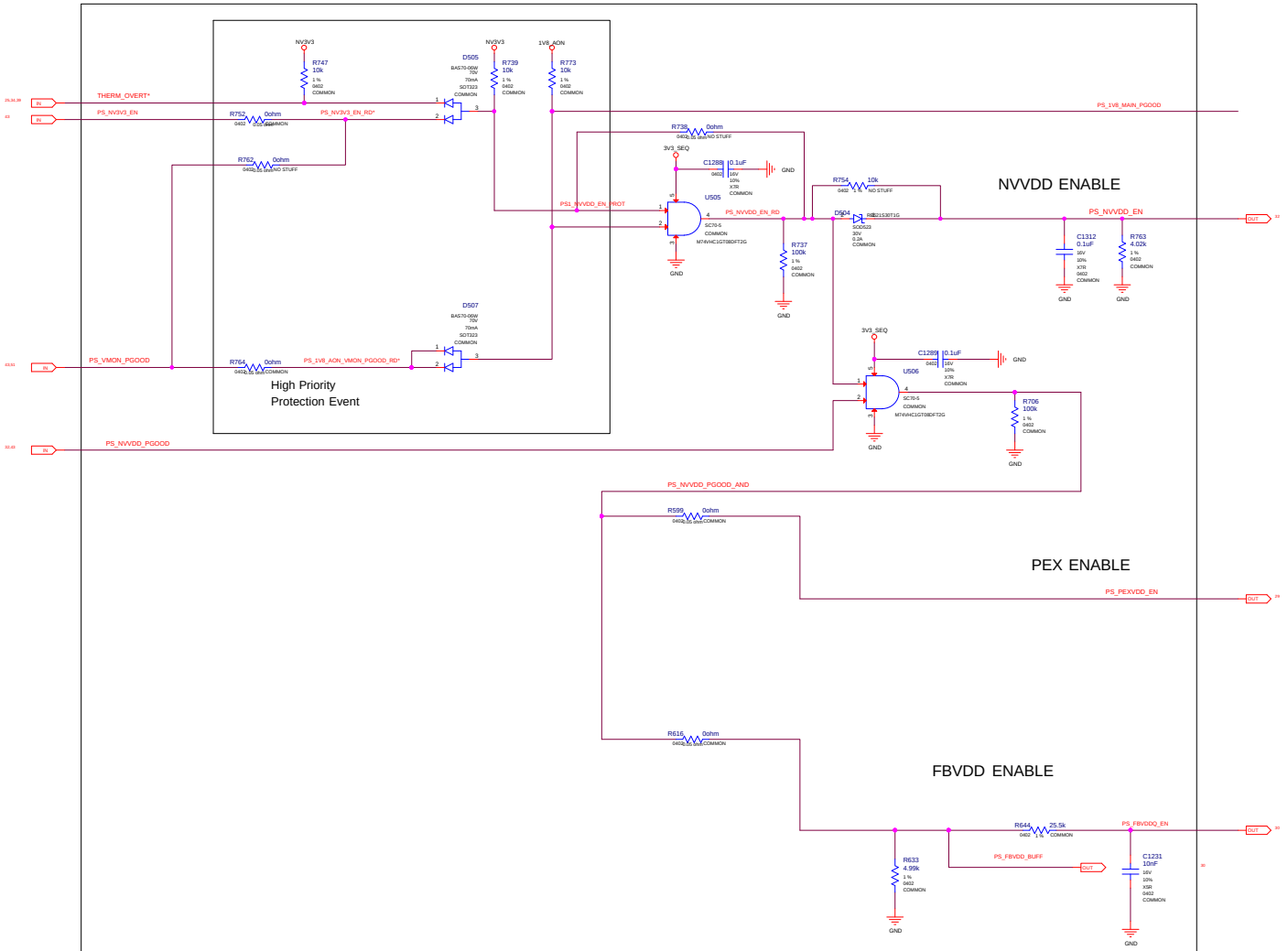
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 43 of 53

Page44: SEQ:NV,PEX,FB ENABLE



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PAGE DETAIL	SEQ: NV, PEX, FB ENABLE

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Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 44 of 53

Page45: SEQUENCE:Voltage Monitor

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: VOLTAGE MONITOR

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Size: Custom	Document Number: PG161H6-E10	Rev: A
Date: Wednesday, October 31, 2018	Sheet 45 of 53	

Page46: SEQUENCE:Discharge

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: DISCHARGE

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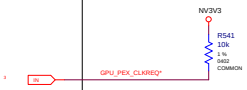
Size: Custom	Document Number: PG161H6-E10	Rev: A
Date: Wednesday, October 31, 2018	Sheet 46 of 53	

Page47: SEQUENCE:MISC

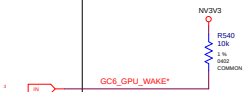
PEX_CLKREQ*



PU ON GPU SIDE

NC ON GOLD FINGER SIDE

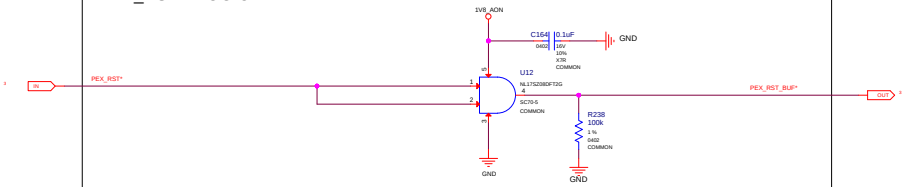
GPU_WAKE*



PU ON GPU SIDE

NC ON GOLD FINGER SIDE

PEX_RST# LOGIC



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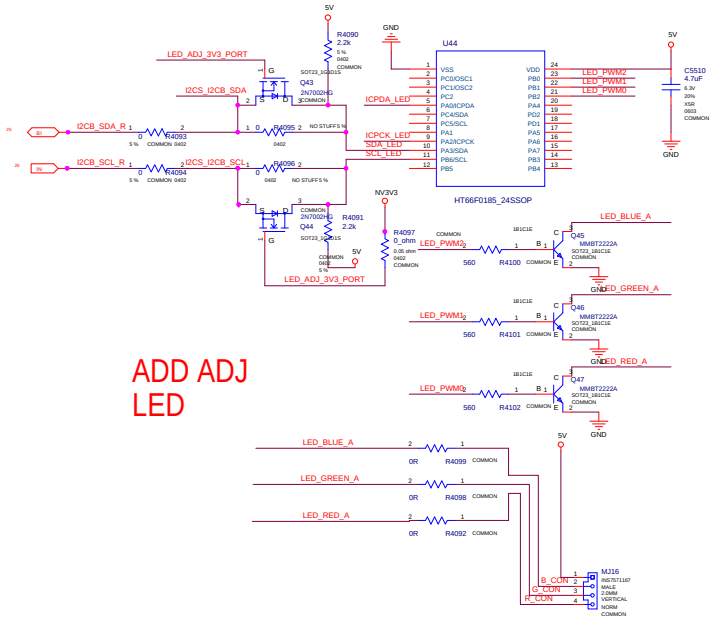
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 47 of 53



ADD ADJ LED

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	LOGO LED

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Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 48 of 53

Page49: LED DRIVER & Boost

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	LED DRIVER & BOOST

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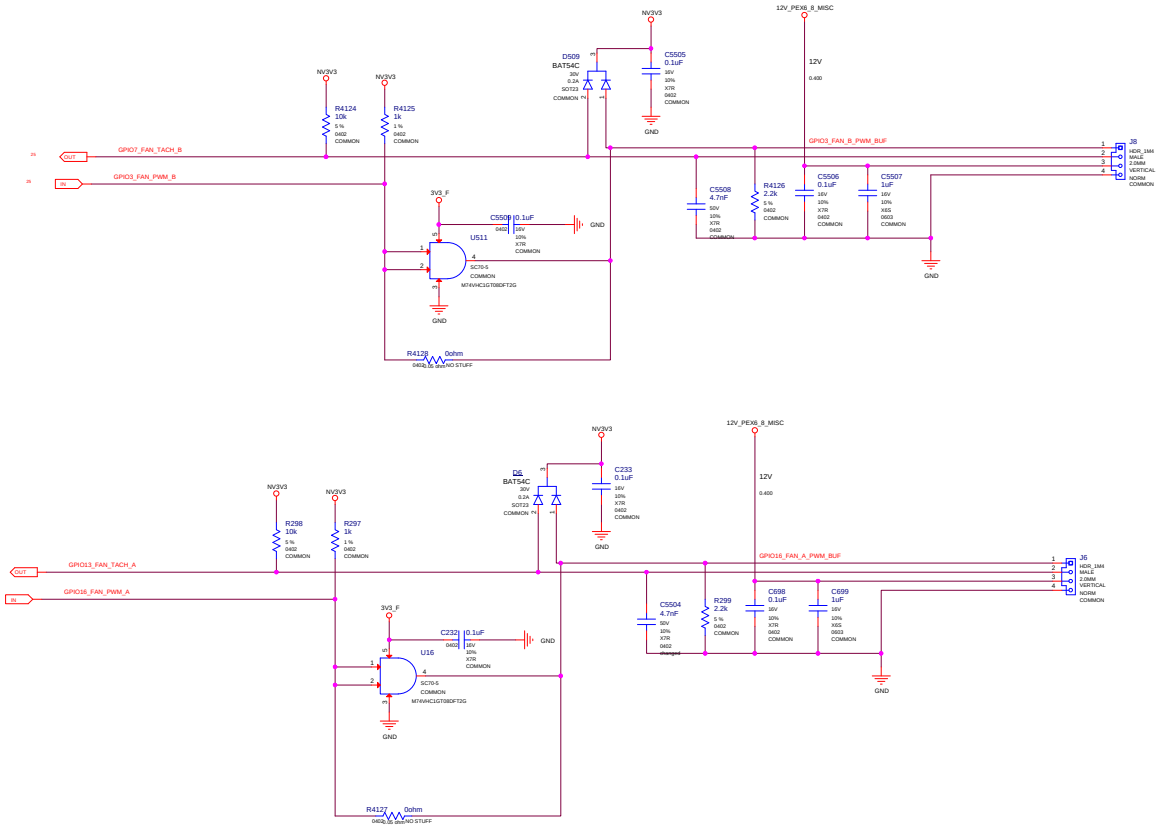
Size: Custom	Document Number: PG161H6-E10	Rev: A
Date: Wednesday, October 31, 2018	Sheet 49 of 53	

Page50: FAN



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	FAN

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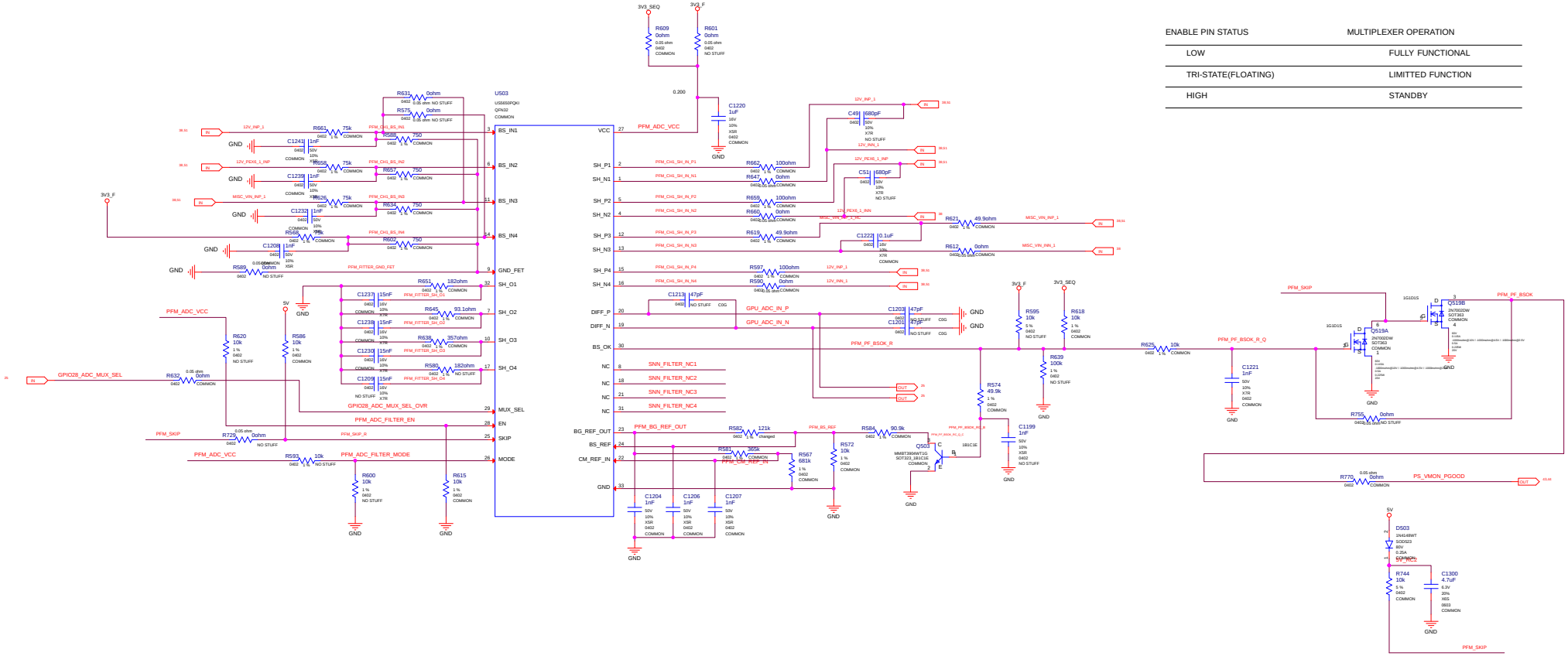
Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 50 of 53

Page51: PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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PAGE DETAIL	PS: Pre-filter

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Custom	PG161H6-E10	A

Date: Friday, November 09, 2018 Sheet 51 of 53

Page52: MECH

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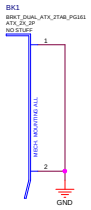

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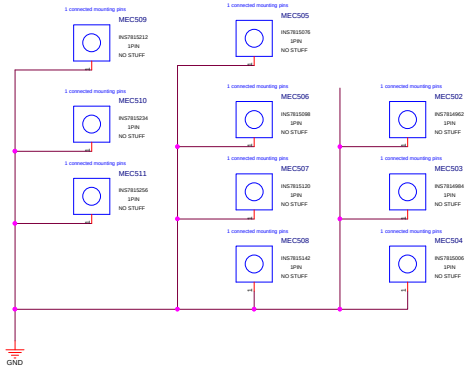

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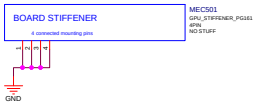

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Size	Document Number	Rev
Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 52 of 53

Page53: PTC

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Custom	PG161H6-E10	A

Date: Wednesday, October 31, 2018 Sheet 53 of 53