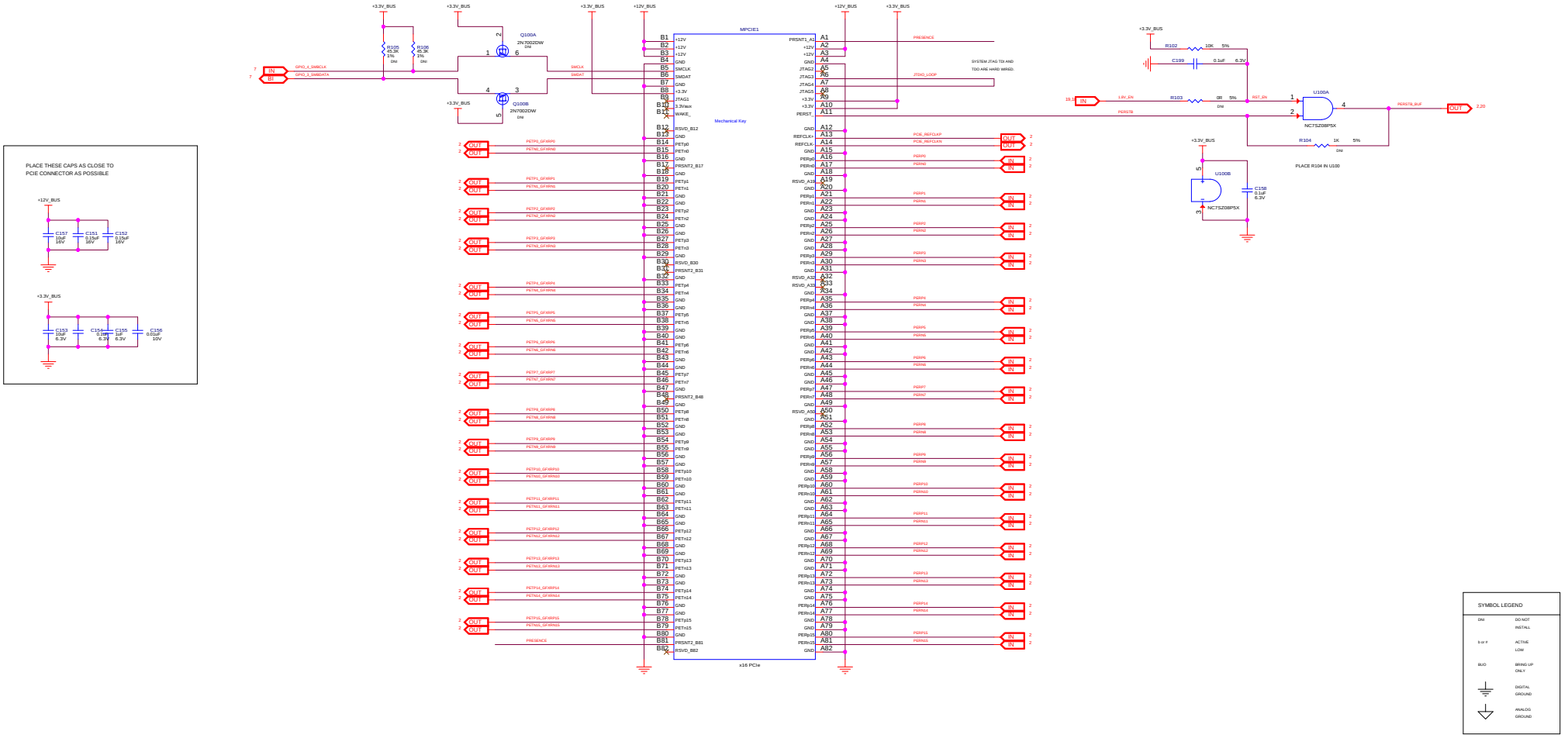
(1) PCI-EXPRESS EDGE CONNECTOR



MICRO-STAR INT'L CO.,LTD			
MS-V305			
Size: Custom	Document Description: 01 PCI-EXPRESS EDGE CONNECTOR		Rev: 10
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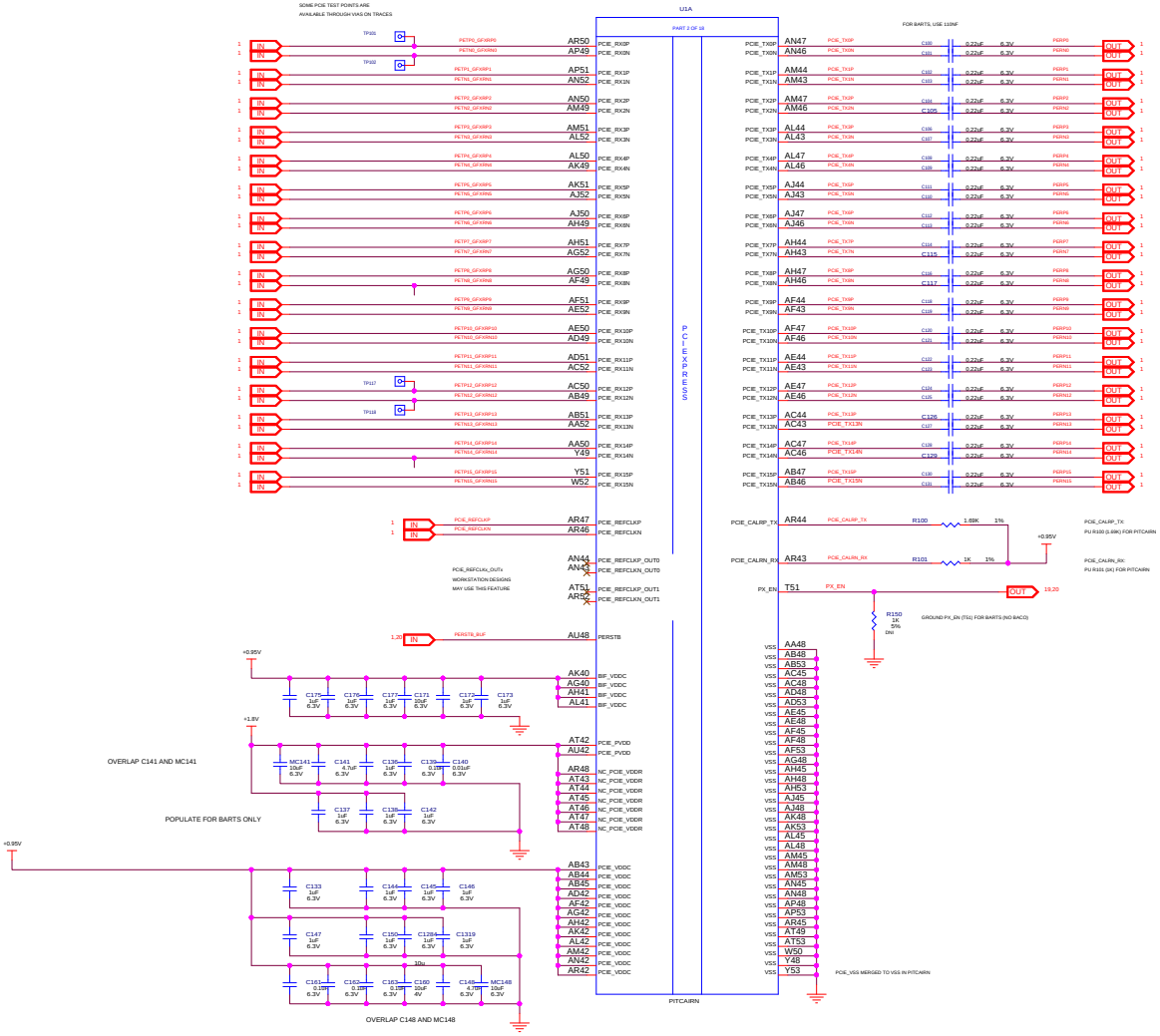
(2) CURACAO PCIE INTERFACE



MICRO-STAR INT'L CO.,LTD		
MS-V305		
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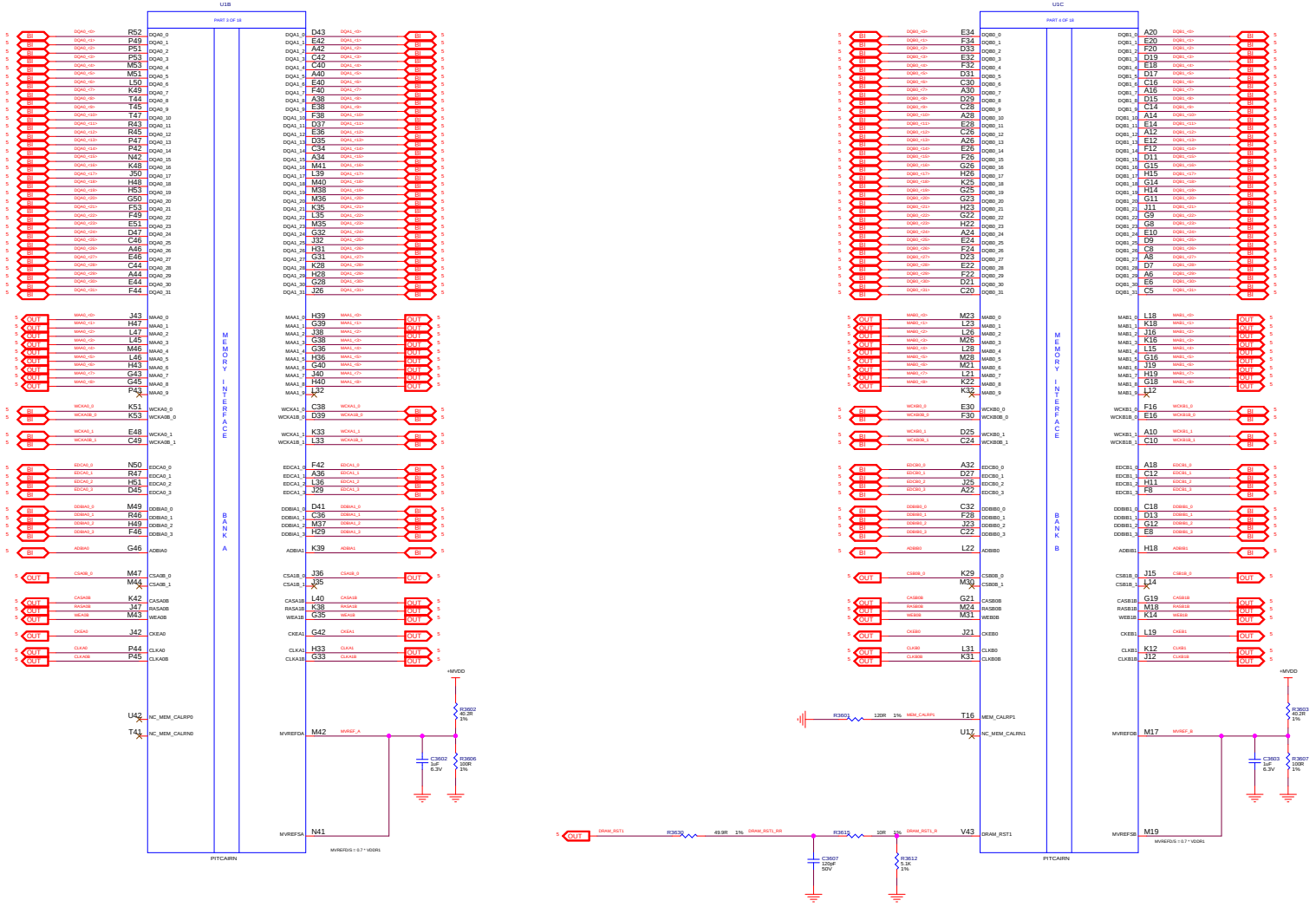
Date: Friday, August 16, 2013	Sheet 2 of 23	

(3) CURACAO MEM INTERFACE CH A/B



MICRO-STAR INT'L CO.,LTD			
MS-V305			
Size: Custom	Document Description: 03 CURACAO MEM CH AB		Rev: 10
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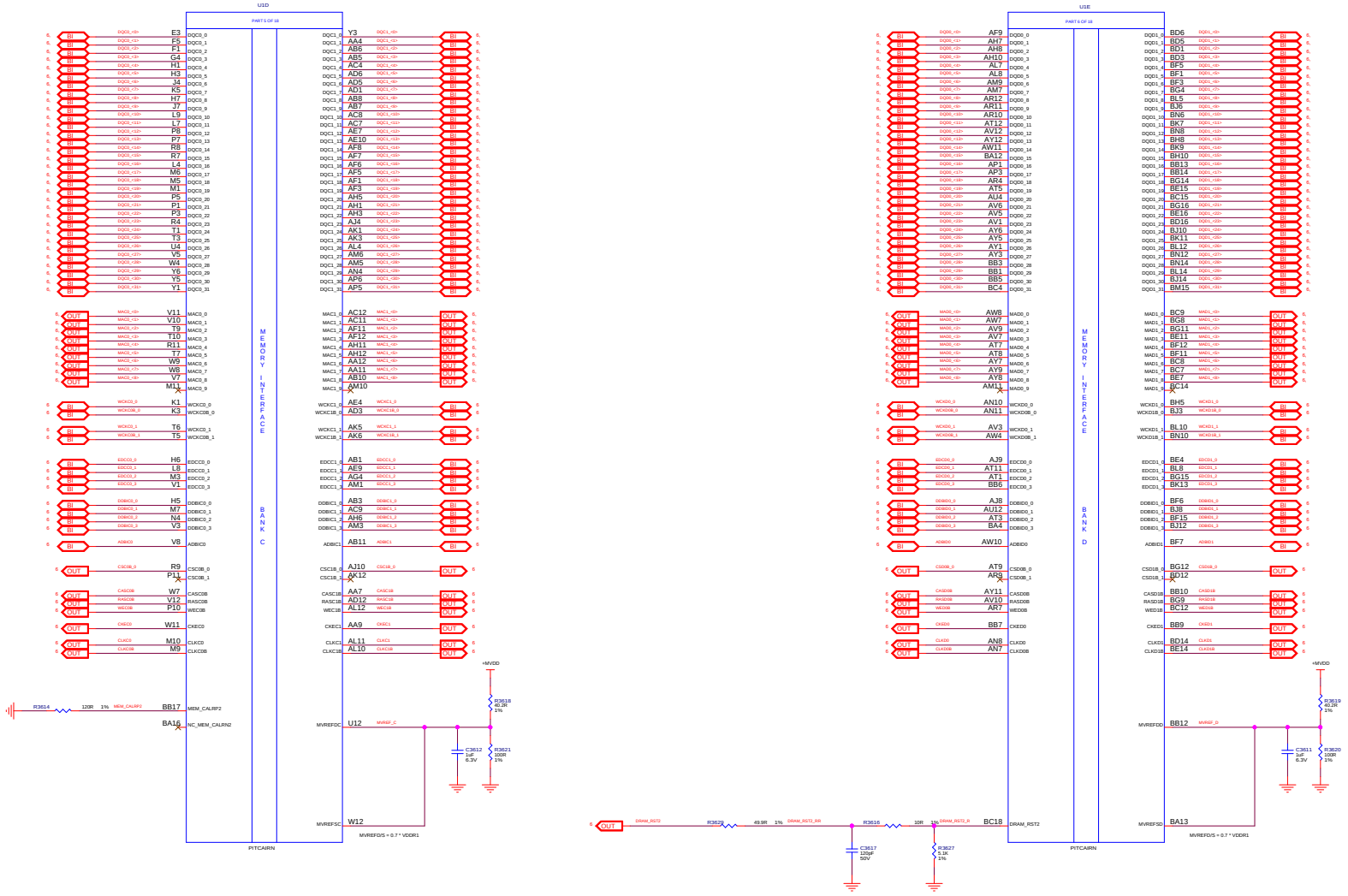
(4) CURACAO MEM INTERFACE CH C/D



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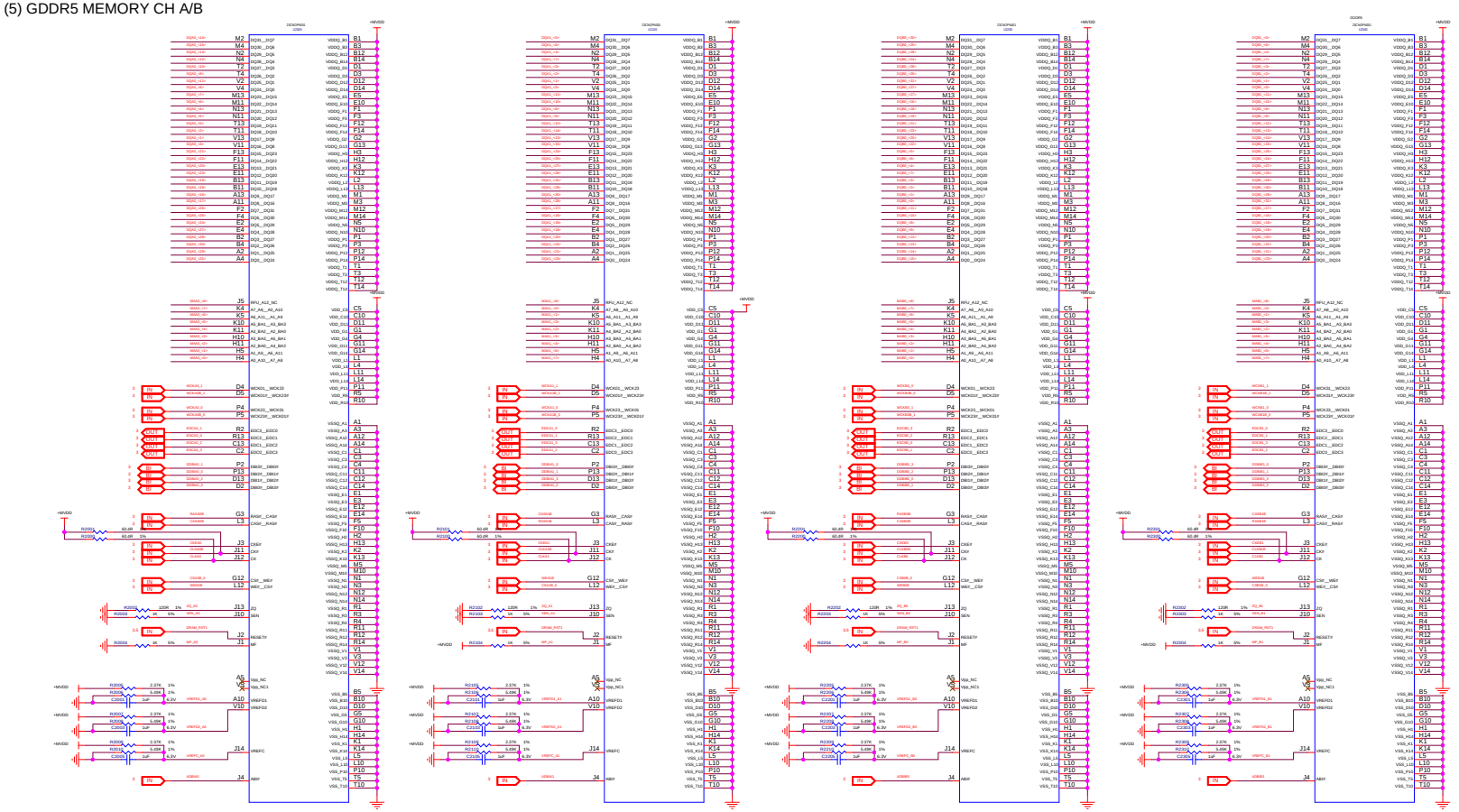
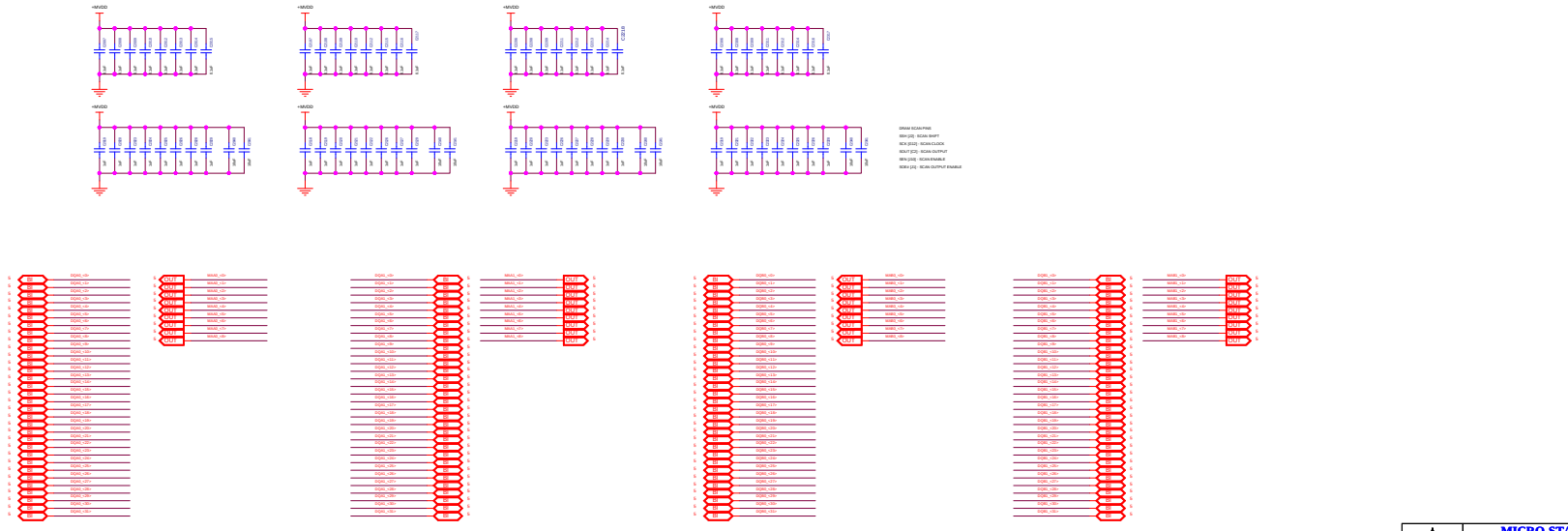
(5) GDDR5 MEMORY CH A/B





MICRO-STAR INT'L CO.,LTD		
MS-V305		
Size: Custom	Document Description: 05 GDDR5 MEM CH AB	Rev: 10
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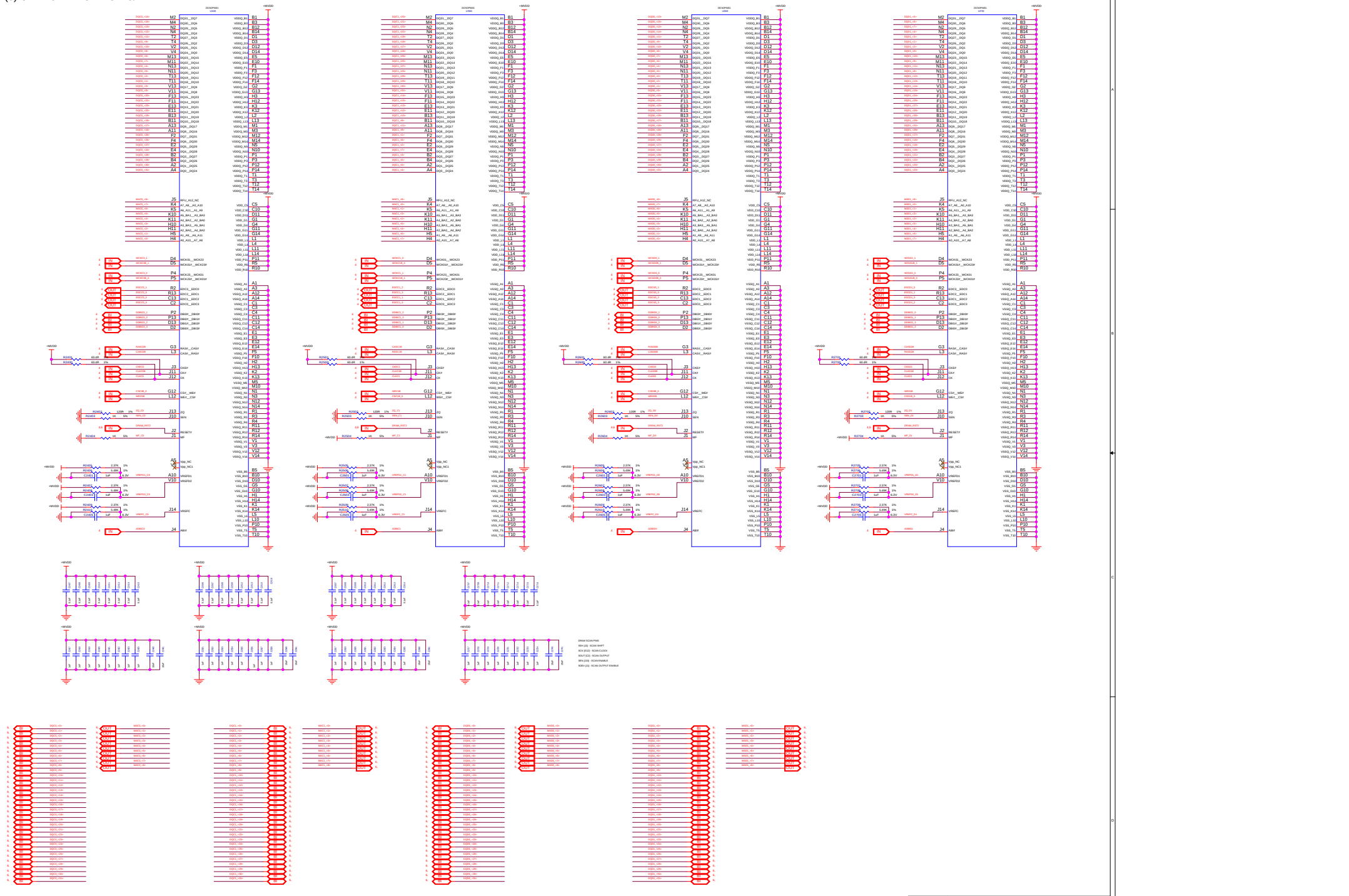
(6) GDDR5 MEMORY CH C/D



MICRO-STAR INT'L CO.,LTD			
MS-V305			
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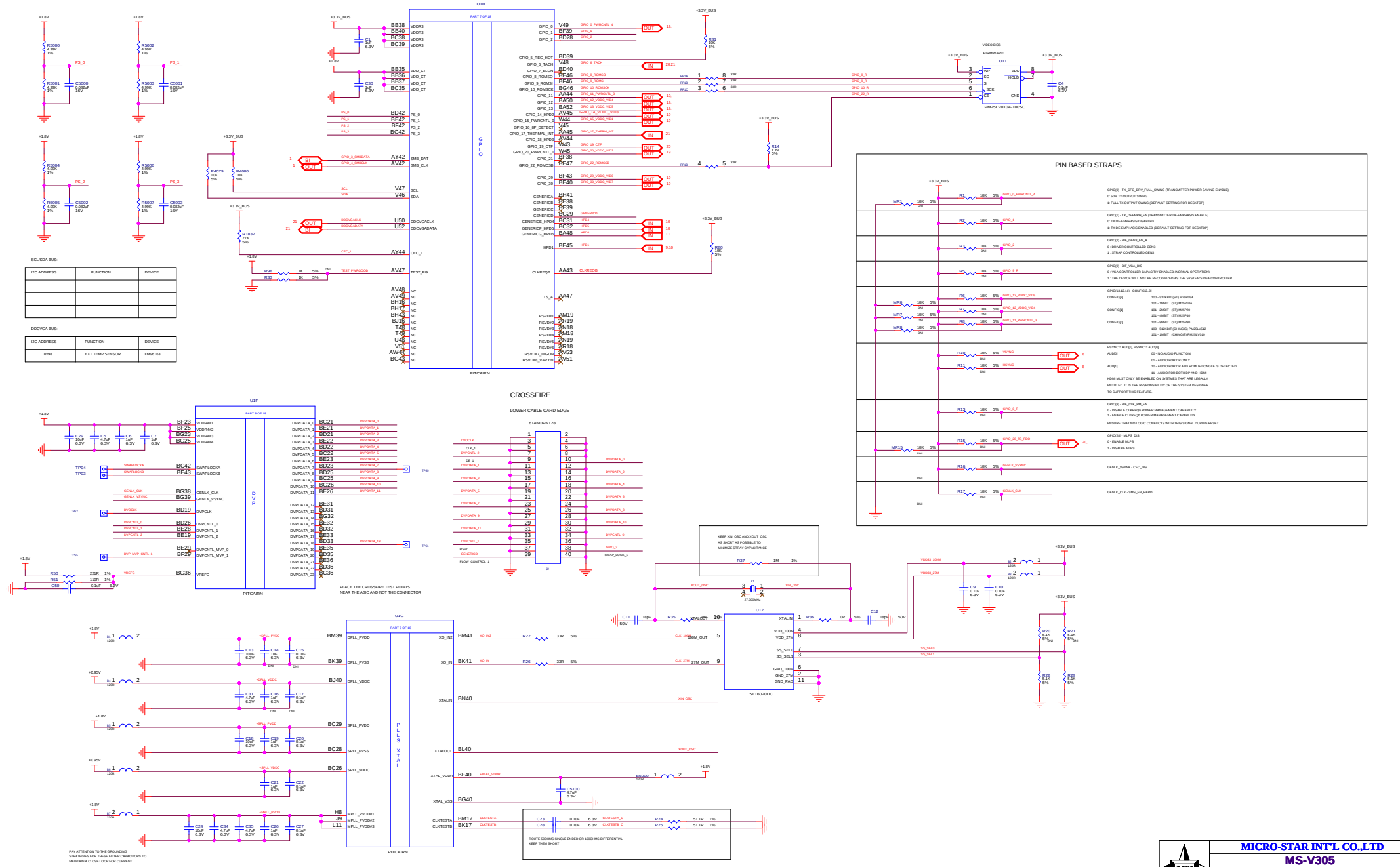
(7) CURACAO GPIO STRAP CF XTAL



MICRO-STAR INT'L CO.,LTD		
MS-V305		
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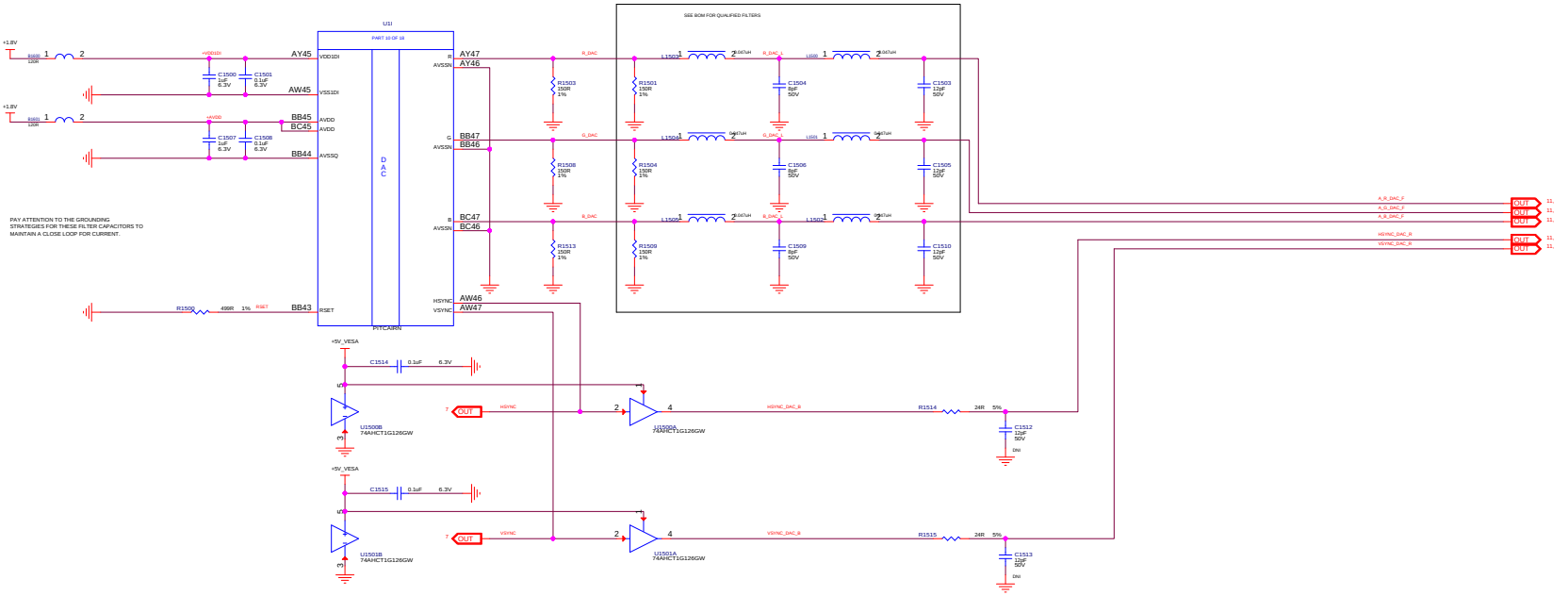
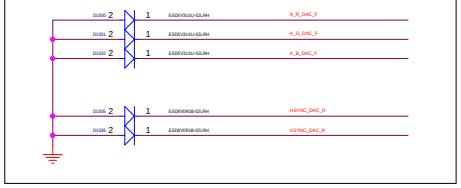
(8) CURACAO DAC1 LOCK



OPTIONAL ESD PROTECTION DIODES



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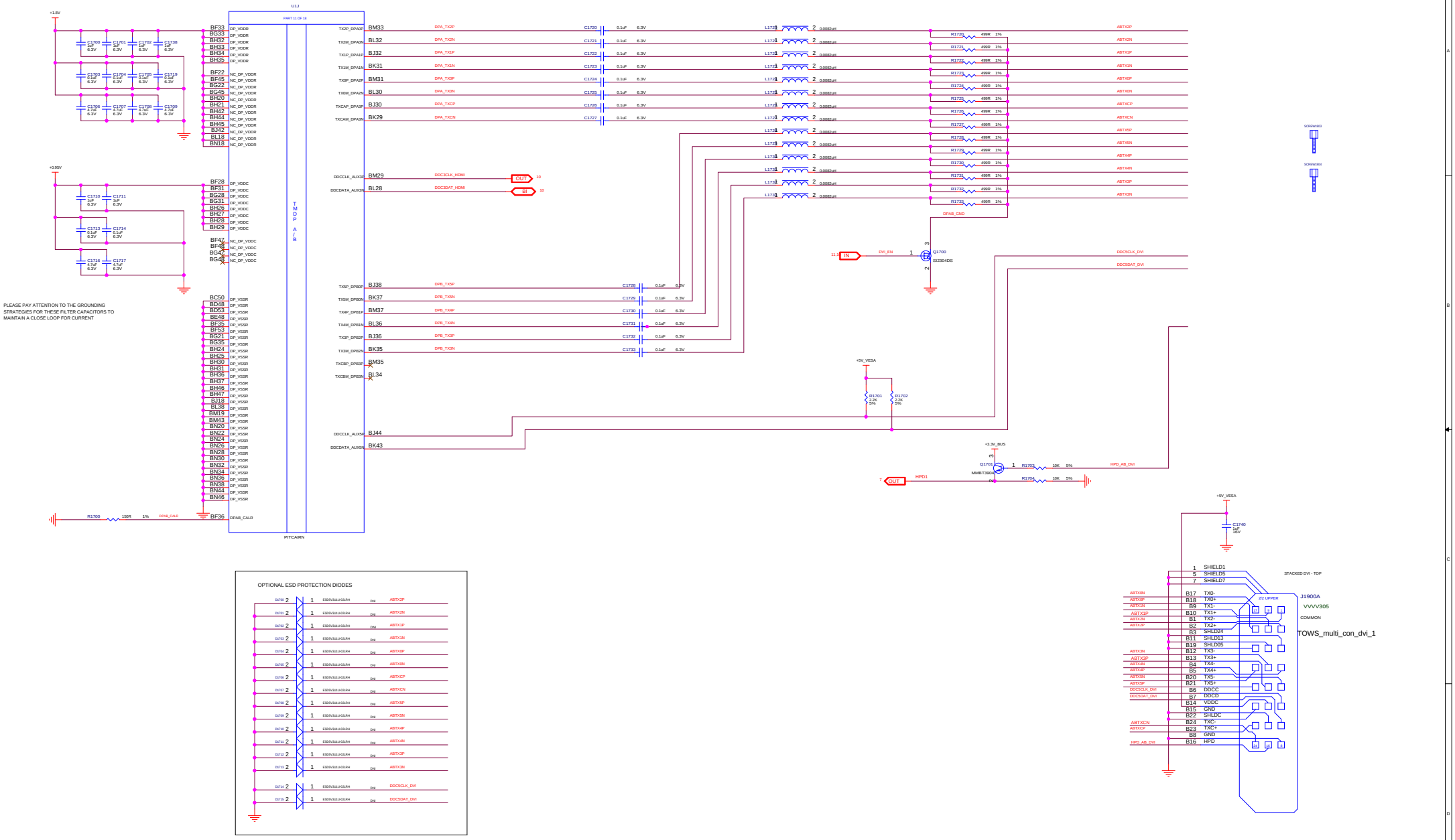
(9) CURACAO TMDP A/B



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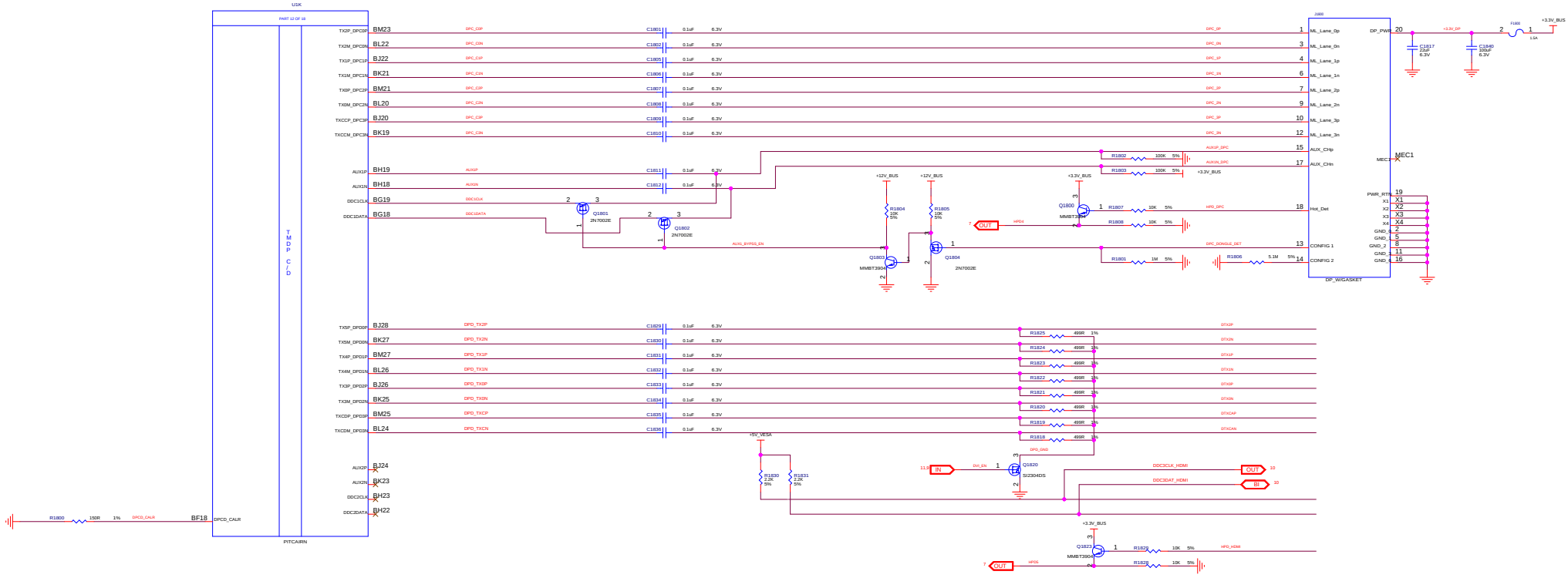
(10) CURACAO TMDP C/D



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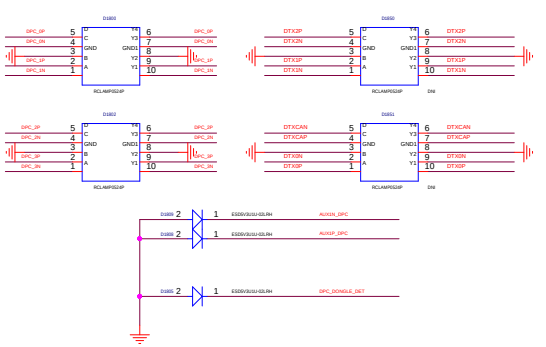

MICRO-STAR INT'L CO.,LTD
MS-V305
Size: Custom
Document Description: 10 CURACAO TMDPCD DP HDMI
Rev: 10
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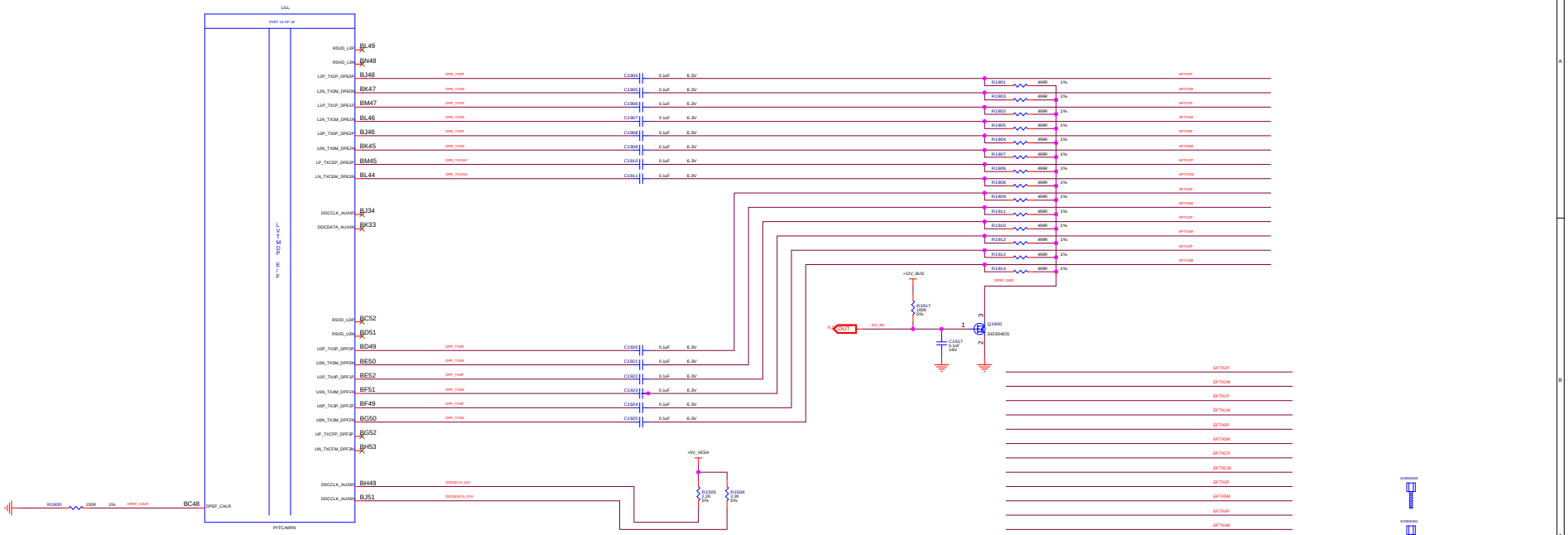
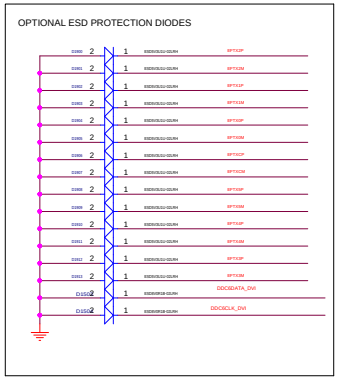
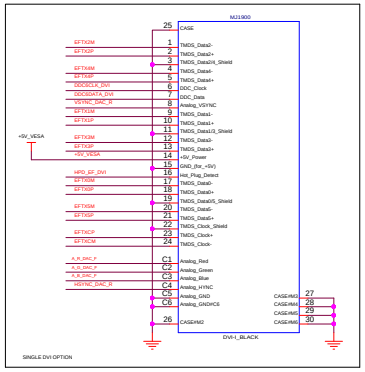
(11) CURACAO LVTMDP E/F







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Size: Custom	Document Description: 11 CURACAO LVTMDPEF dDVI Botto	Rev: 10	
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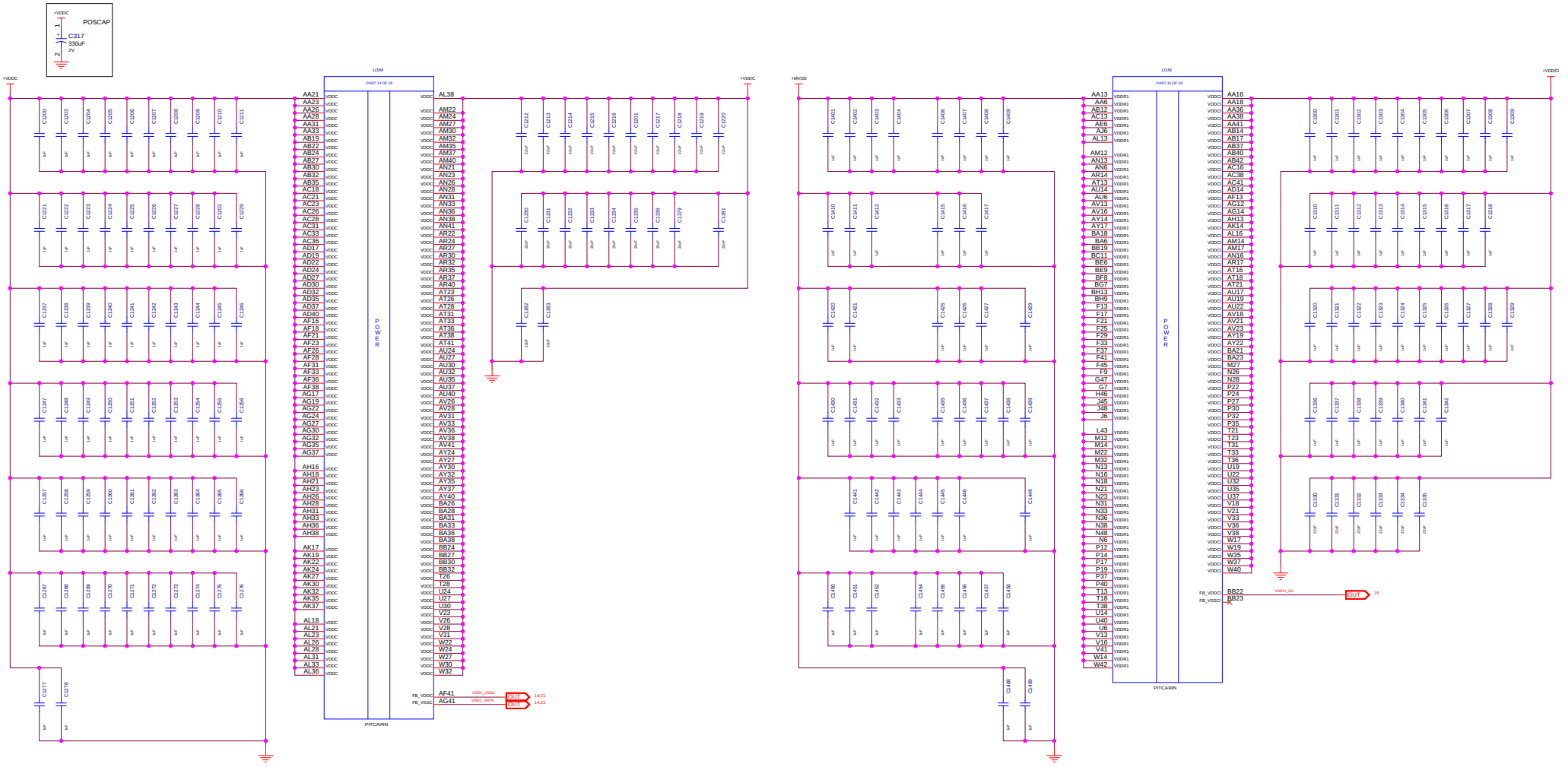
(12) CURACAO POWER



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Size: Custom	Document Description: 12 CURACAO POWER
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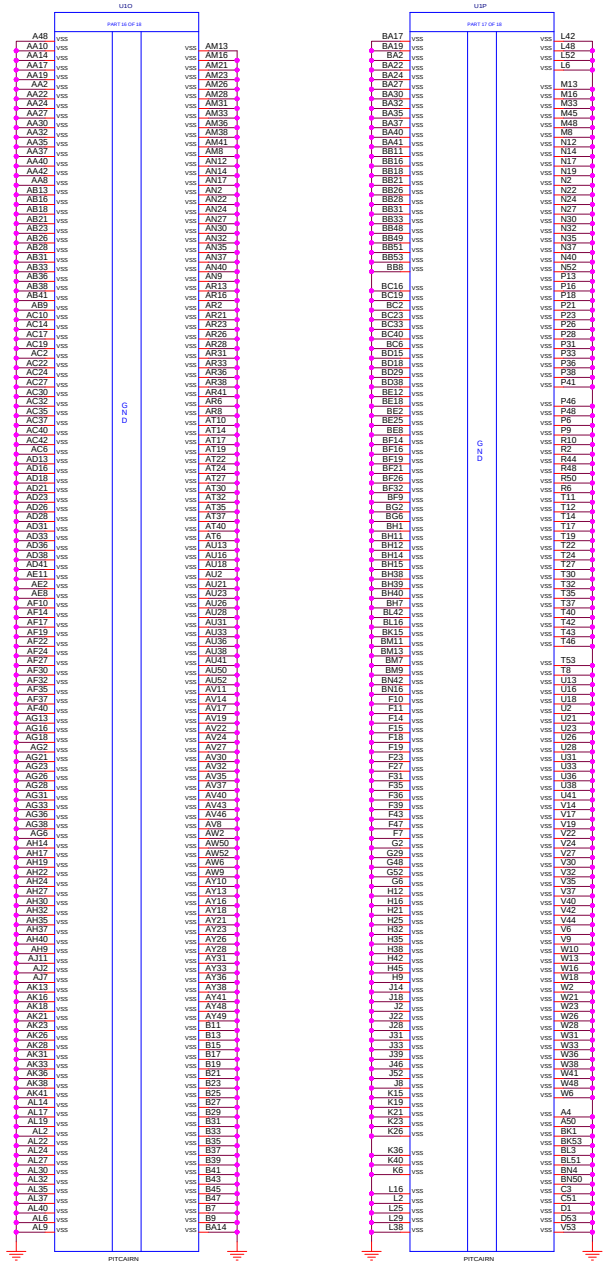
(13) CURACAO GROUND



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: 13 CURACAO GND	Rev: 10
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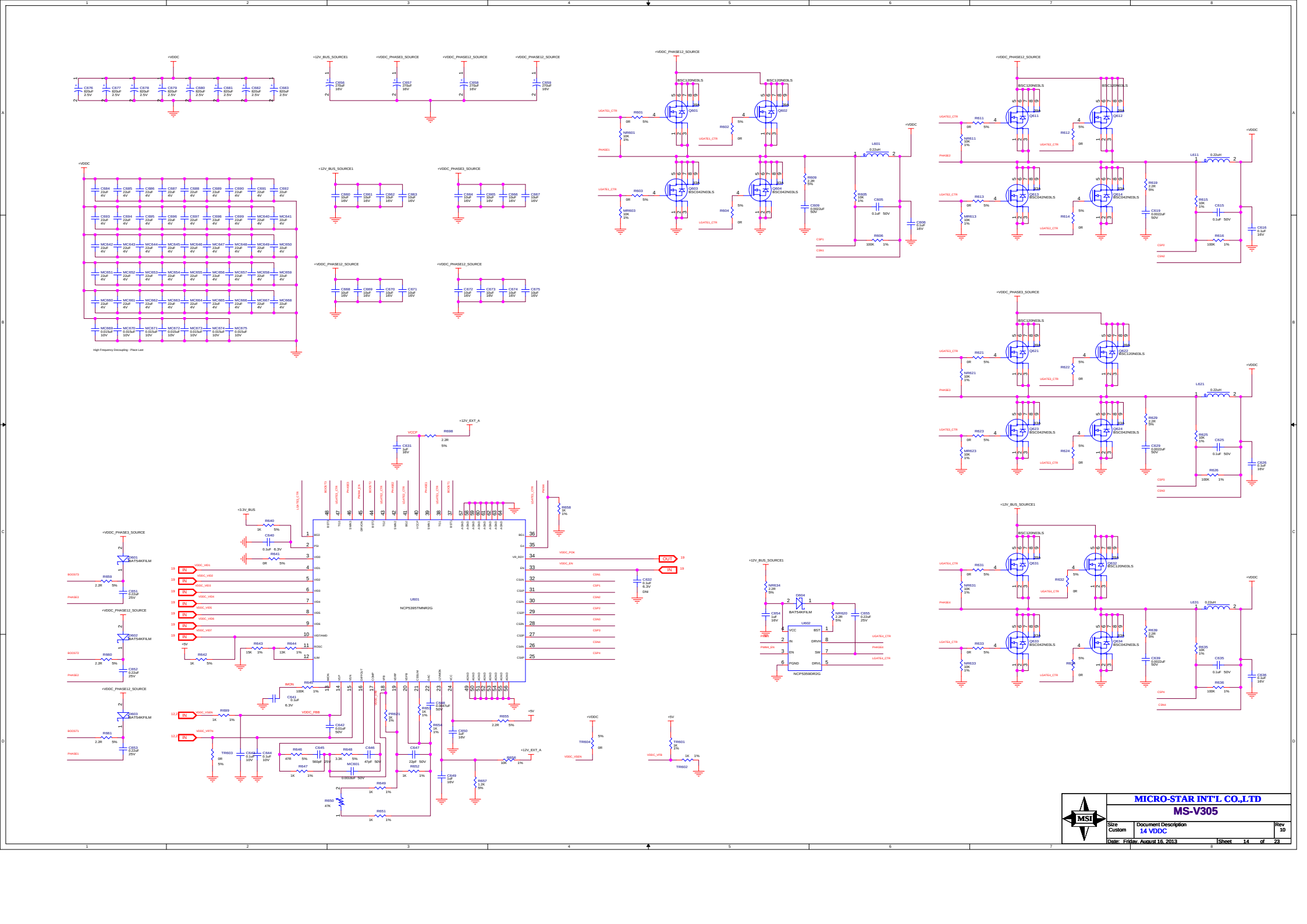
+VDDC
+12V_BUS_SOURCE1
+VDDC_PHASE3_SOURCE
+VDDC_PHASE12_SOURCE
High Frequency Decoupling - Place Last
U601
NCP5395TMNR2G
+12V_EXT_A
+3.3V_BUS
U602
NCP53590R2G
BAT54KFILM
BSC120N03LS
BSC042N03LS
MICRO-STAR INT'L CO.,LTD
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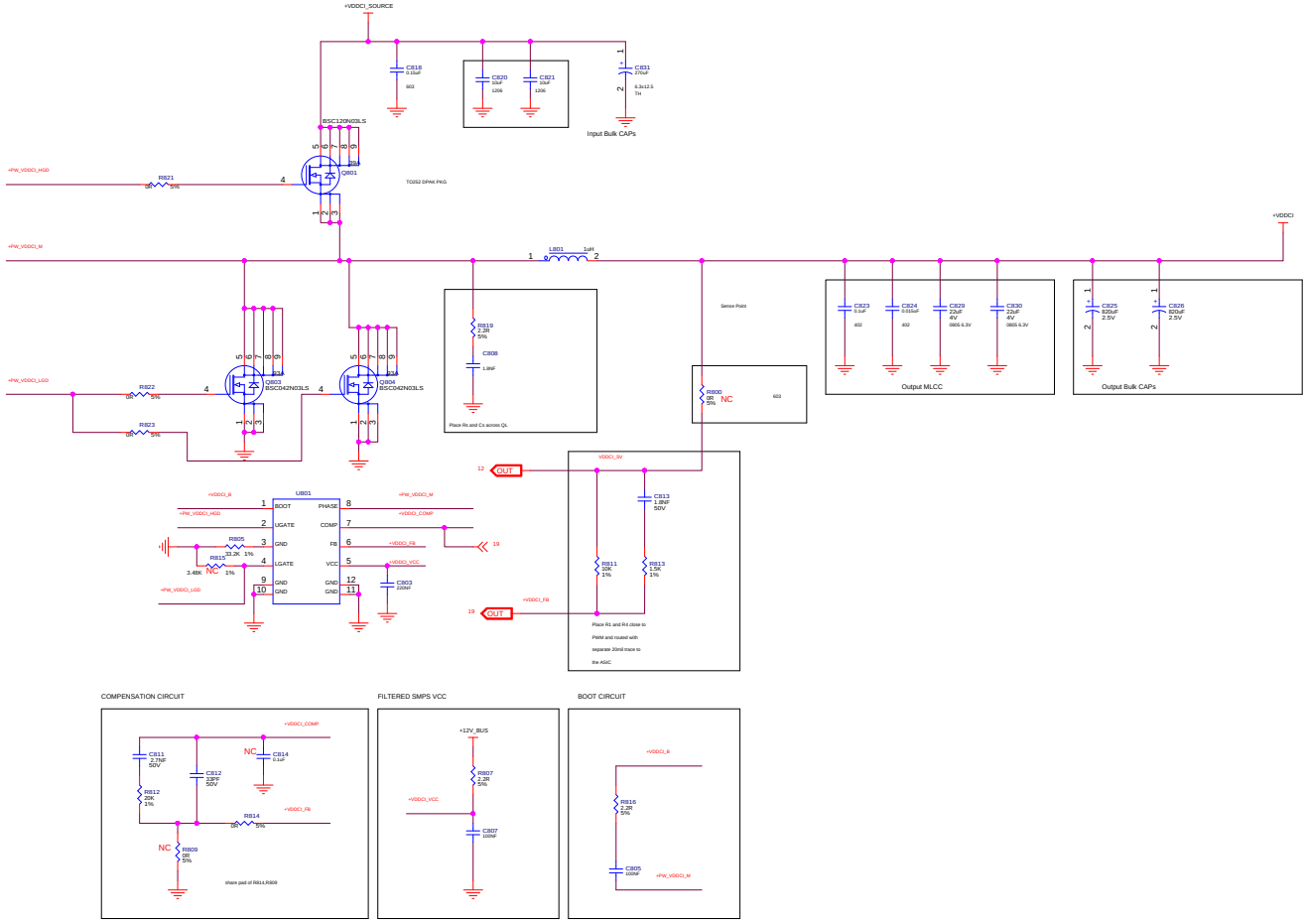
(15) VDDCI



MICRO-STAR INT'L CO.,LTD

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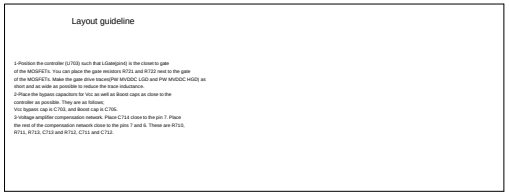
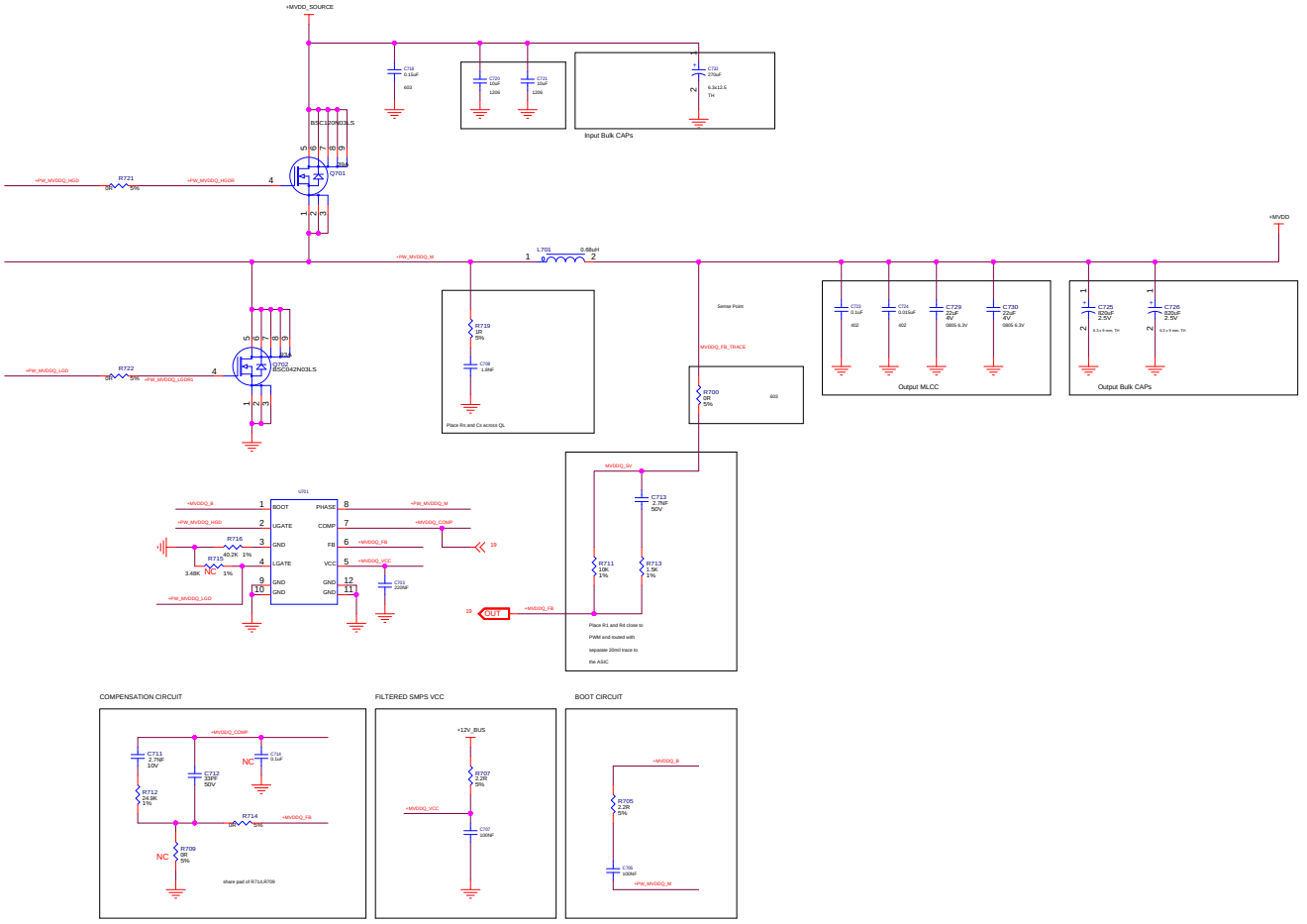
(16) MVDD





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Size: Custom	Document Description: 16 MVDD	Rev: 10
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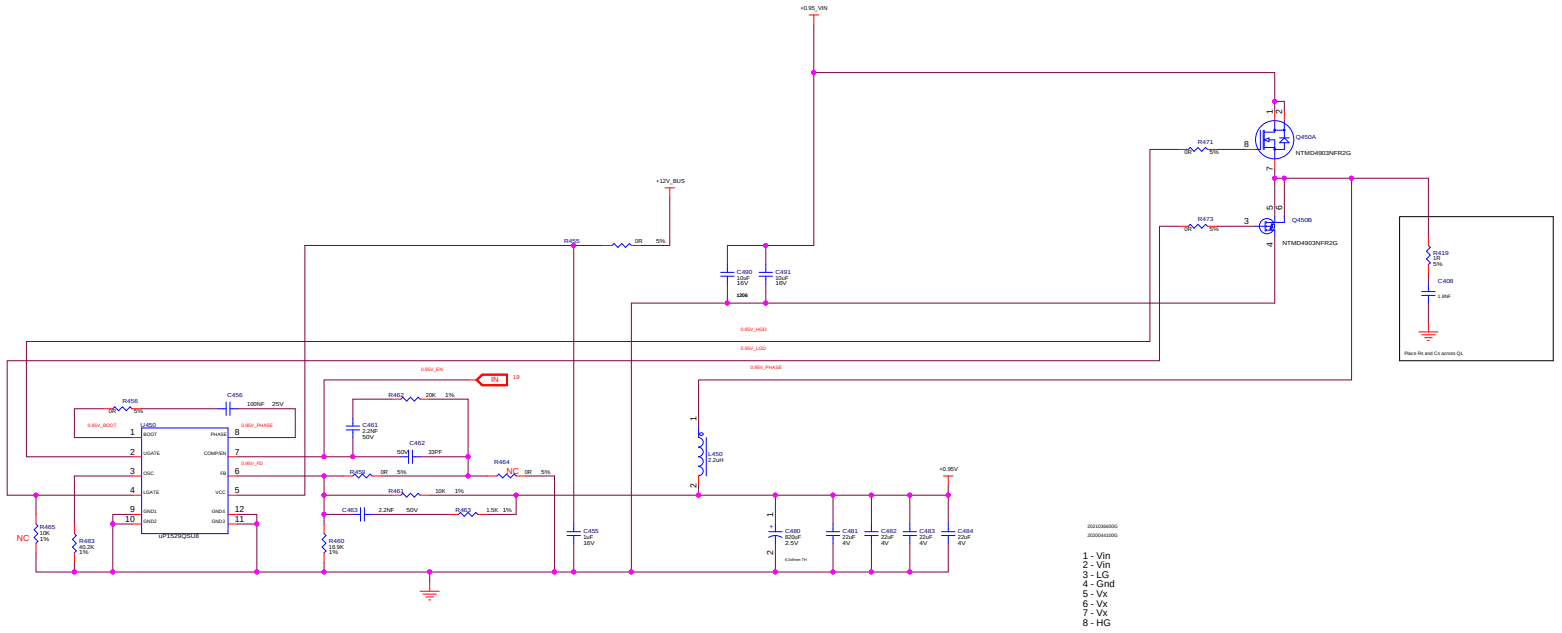
(17) 0.95V



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: 17 0.95V REG	Rev: 10
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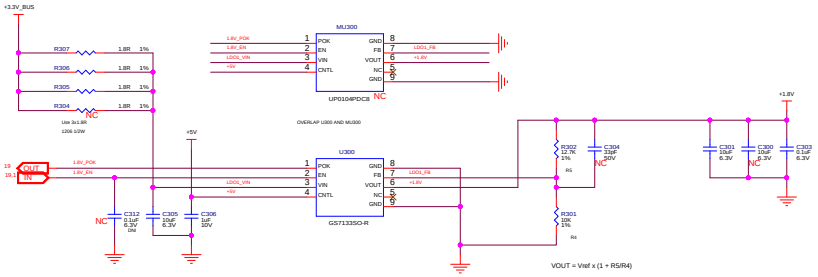
(18) SMALL RAIL REGULATORS

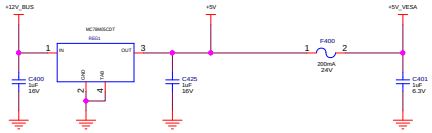
LDO #1: VIN = 3.0V TO 3.6V MAX VOUT = +1.8V +/- 2% IOUT = 1.3A RMS MAX

PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING



REGULATOR FOR +5V RAILS

IOUT MAX = 150mA



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MS-V305			
Size: Custom	Document Description: 18 SMALL RAIL REGULATORS		Rev: 10
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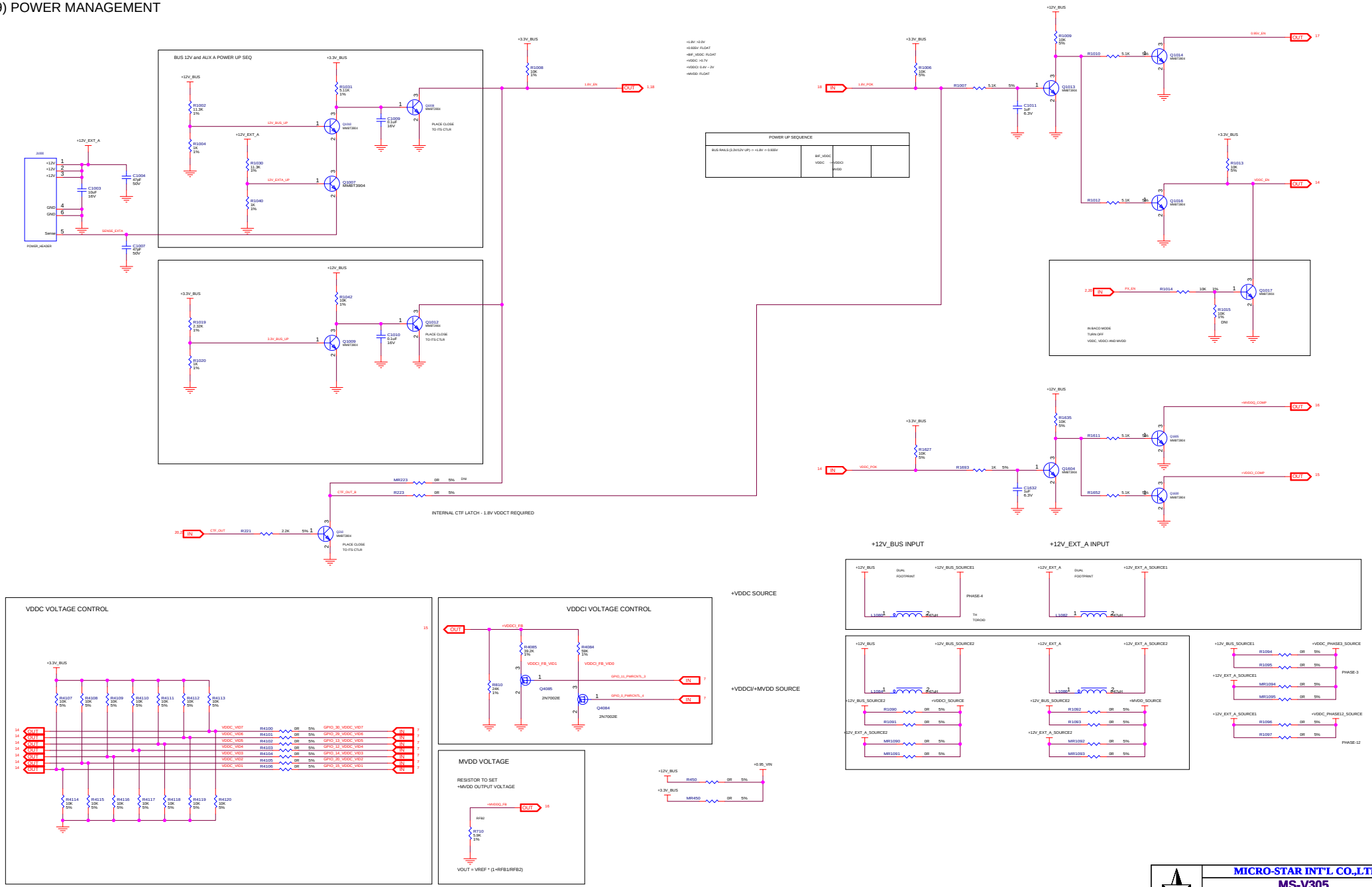
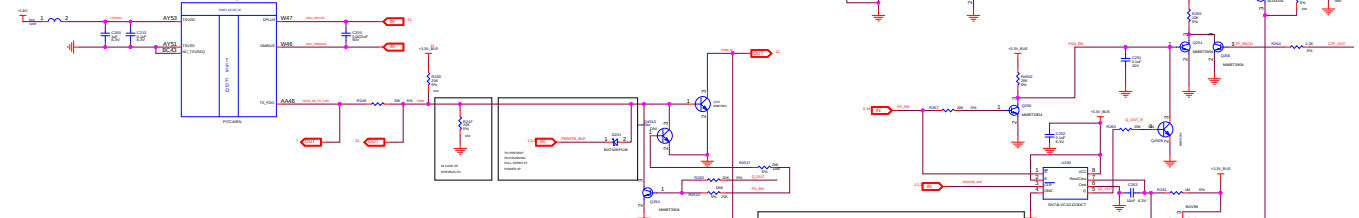
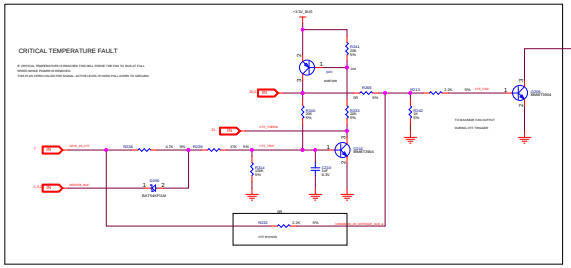
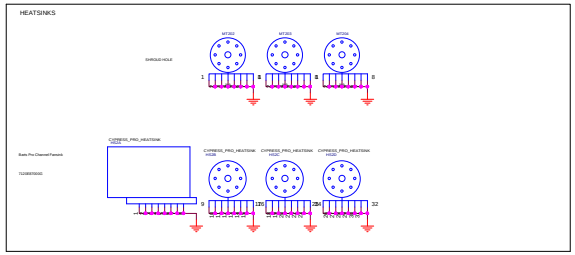
(19) POWER MANAGEMENT



(20) MECHANICAL AND THERMAL MANAGEMENT





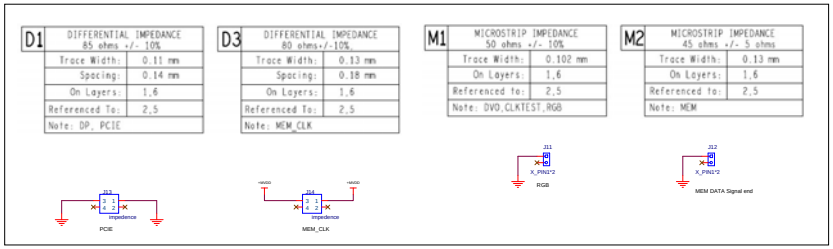


D1	DIFFERENTIAL IMPEDANCE 85 ohms +/- 10%	
	Trace Width:	0.11 mm
	Spacing:	0.14 mm
	On Layers:	1,6
	Referenced To:	2,5
	Note: DP, PCIE	

D3	DIFFERENTIAL IMPEDANCE 80 ohms +/- 10%	
	Trace Width:	0.13 mm
	Spacing:	0.18 mm
	On Layers:	1,6
	Referenced To:	2,5
	Note: MEM_CLK	

M1	MICROSTRIP IMPEDANCE 50 ohms +/- 10%	
	Trace Width:	0.102 mm
	On Layers:	1,6
	Referenced to:	2,5
	Note: DVO,CLKTEST,RGB	

M2	MICROSTRIP IMPEDANCE 45 ohms +/- 5 ohms	
	Trace Width:	0.13 mm
	On Layers:	1,6
	Referenced to:	2,5
	Note: MEM	



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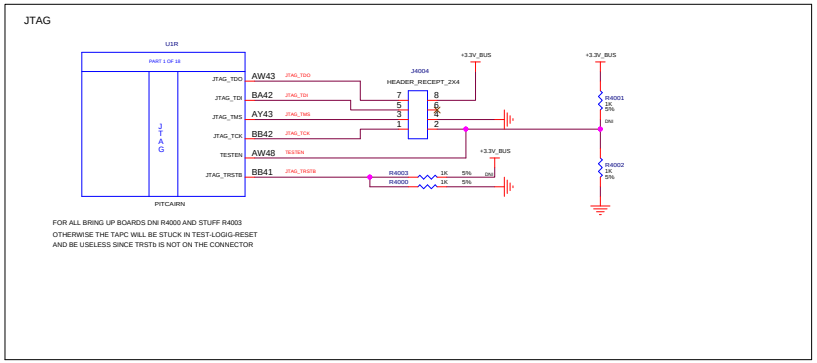
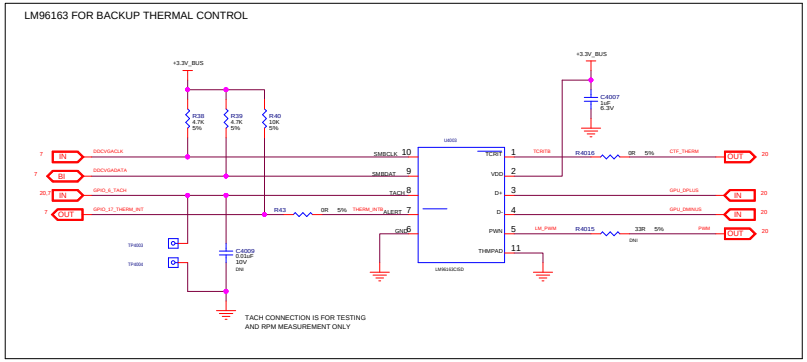
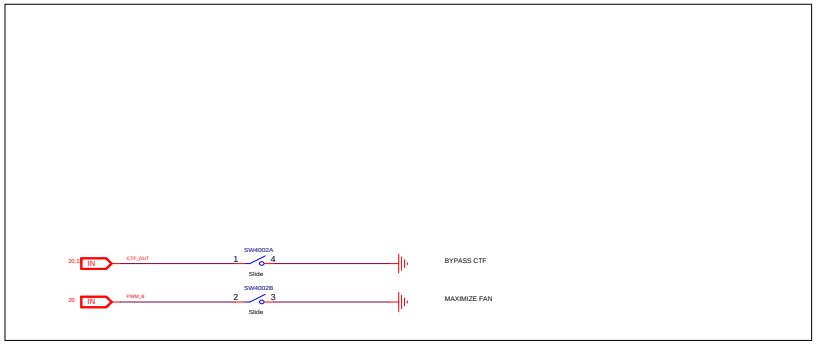
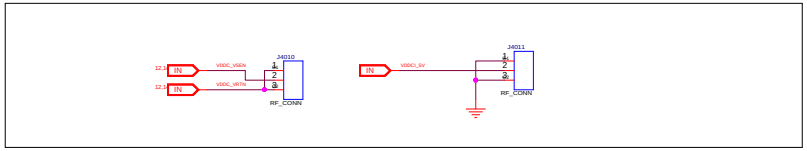
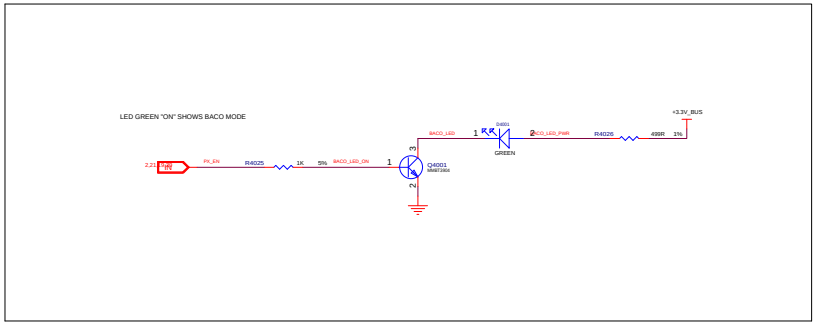
(21) DEBUG CIRCUITS











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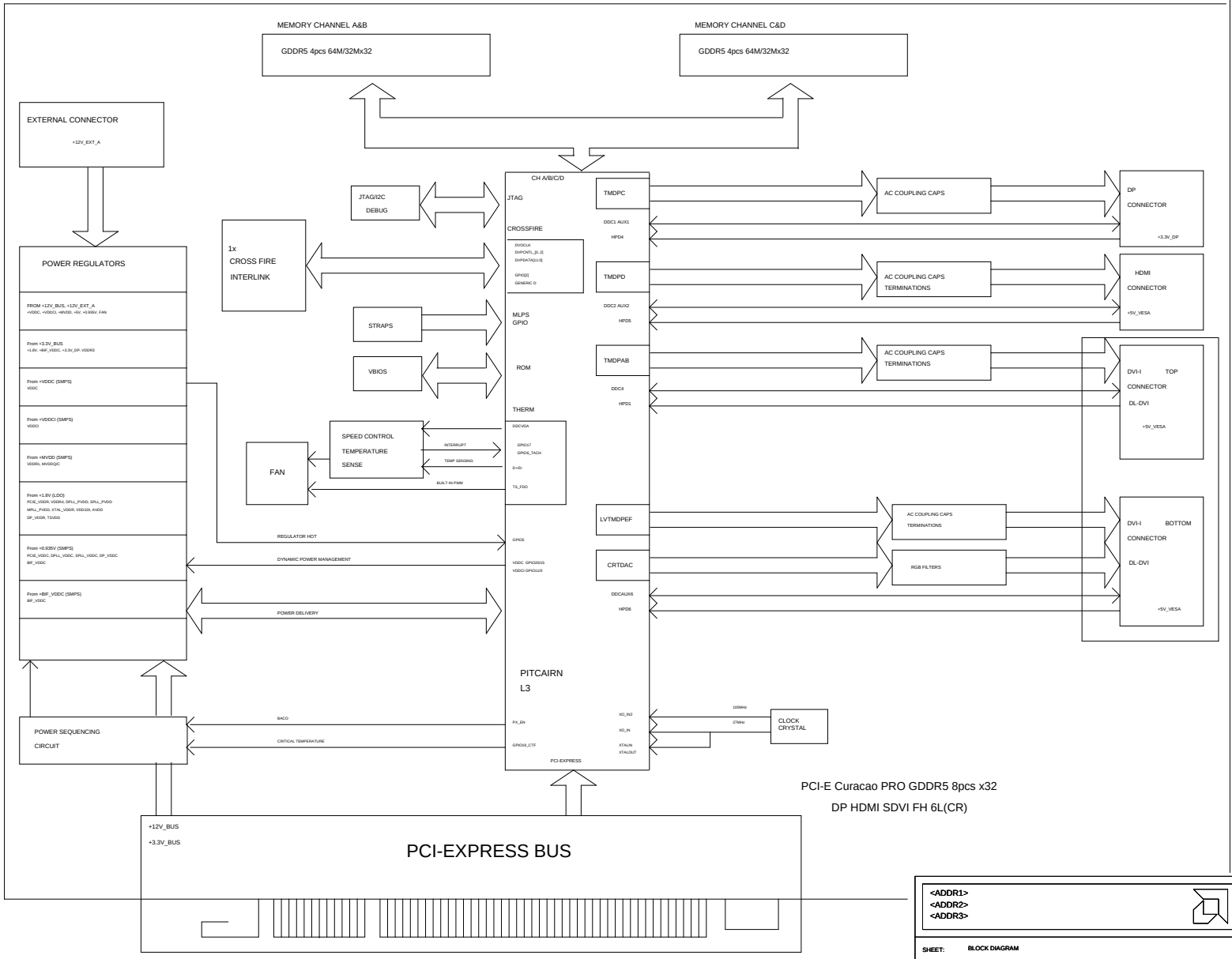
MS-V305			
Size: Custom	Document Description: 21 DEBUG CIRCUITS		Rev: 10
Date: Friday, August 16, 2013		Sheet 21 of 23	



PCI-E Curacao PRO GDDR5 8pcs x32

DP HDMI SDVI FH 6L(CR)

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DATE: Wed Jul 24 07:55:42 2013	REV: <REV>
SHEET NUMBER: 22 OF 23	
DOCUMENT NUMBER: 105_C630XX_01	

TITLE: <TITLE>

AMD

TITLE: <TITLE>

DOCUMENT NUMBER: 105_C630XX_01

DATE: Wed Jul 24 07:55:42 2013

SHEET NUMBER: 23 OF 23

REV: <REV>

REVISION HISTORY

ENGINEER: <ENGINEER>

NOTES: NOTE

<ADDR1>
<ADDR2>
<ADDR3>

SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
0	00A	01/07/2010	
1	00B	04/17/2012	No schematic change. Just add mouse bit hole on PCB
2	00	05/31/2013	No schematic change.