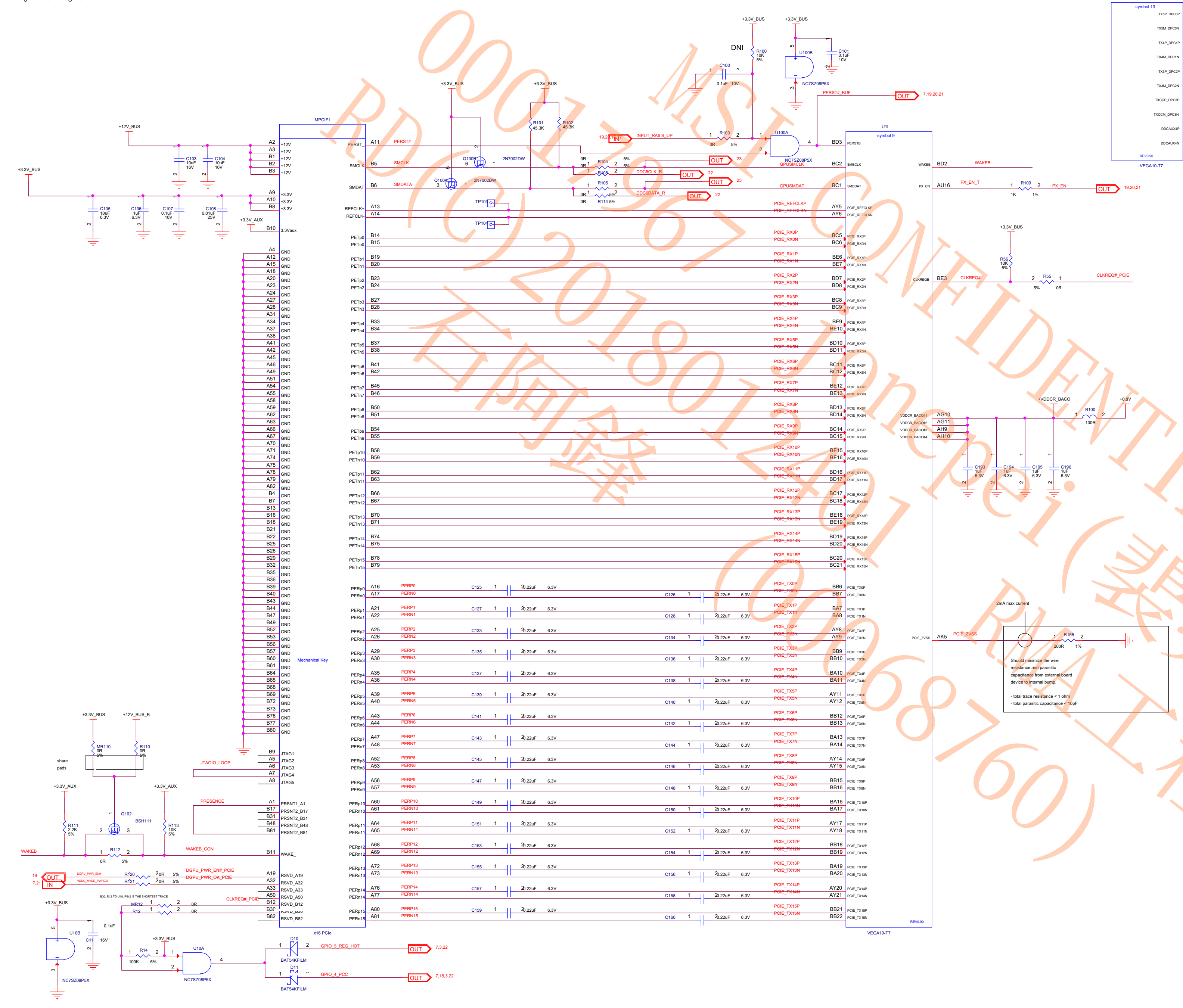
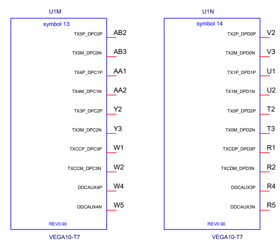
1. Vega10 PCIe Edge Connector





SYMBOL LEGEND

DNI	DO NOT INSTALL
X or #	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

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Custom	Vega10 - PCIe Interface	1.1
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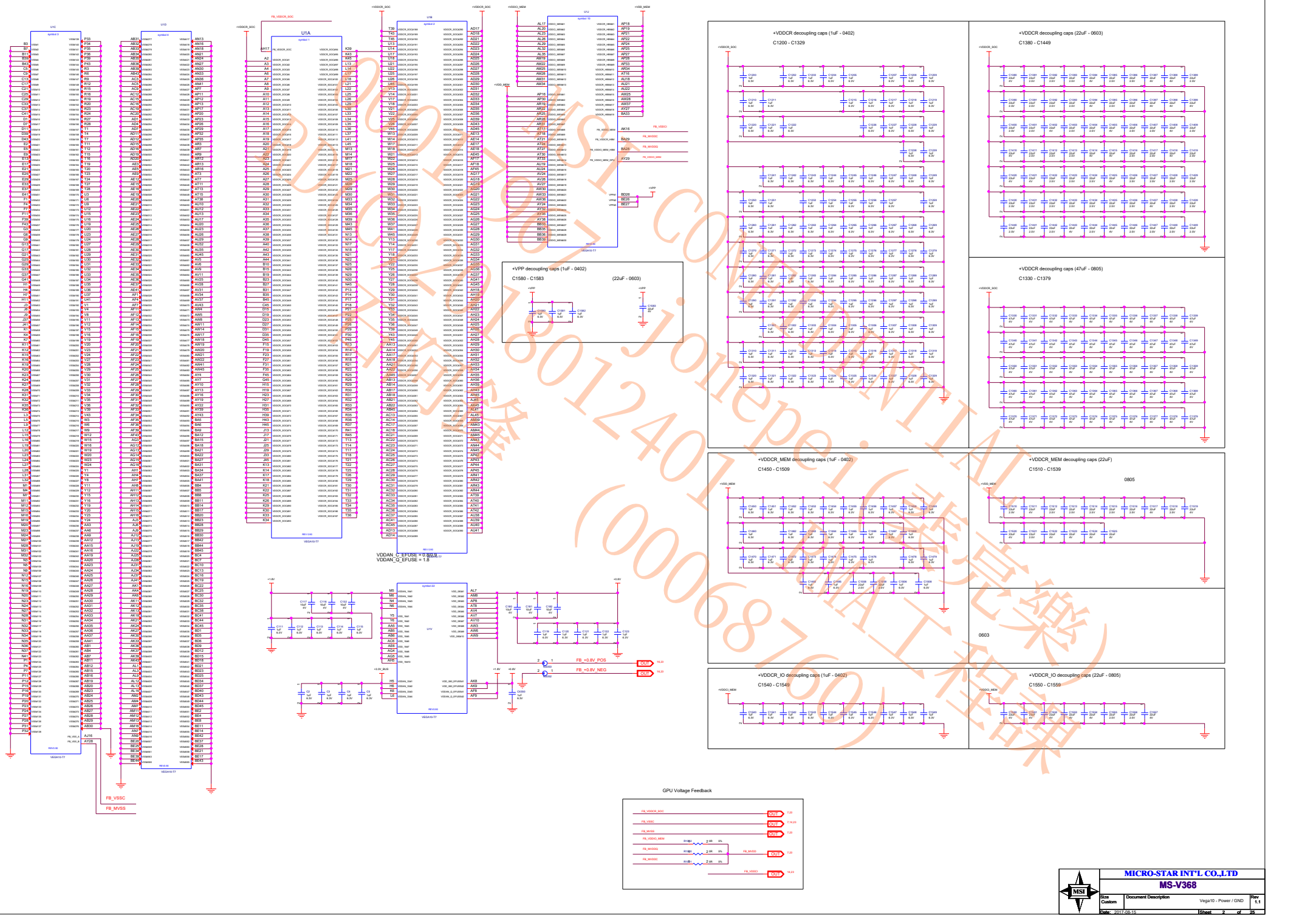
U1A
+VDDCR_SOC
+VDDCI_MEM
+VDD_MEM
+VPP decoupling caps (1uF - 0402)
C1580 - C1583
(22uF - 0603)
VDDAN_C_EFUSE = 0.9~1.8
VDDAN_Q_EFUSE = 1.8
+VDDCR decoupling caps (1uF - 0402)
C1200 - C1329
+VDDCR decoupling caps (22uF - 0603)
C1380 - C1449
+VDDCR decoupling caps (47uF - 0805)
C1330 - C1379
+VDDCR_MEM decoupling caps (1uF - 0402)
C1450 - C1509
+VDDCR_MEM decoupling caps (22uF)
C1510 - C1539
0805
0603
+VDDCR_IO decoupling caps (1uF - 0402)
C1540 - C1549
+VDDCR_IO decoupling caps (22uF - 0805)
C1550 - C1559
GPU Voltage Feedback
FB_VSSC
FB_MVSS
FB_+0.8V_POS
FB_+0.8V_NEG
MICRO-STAR INT'L CO.,LTD
MS-V368
Vega10 - Power / GND
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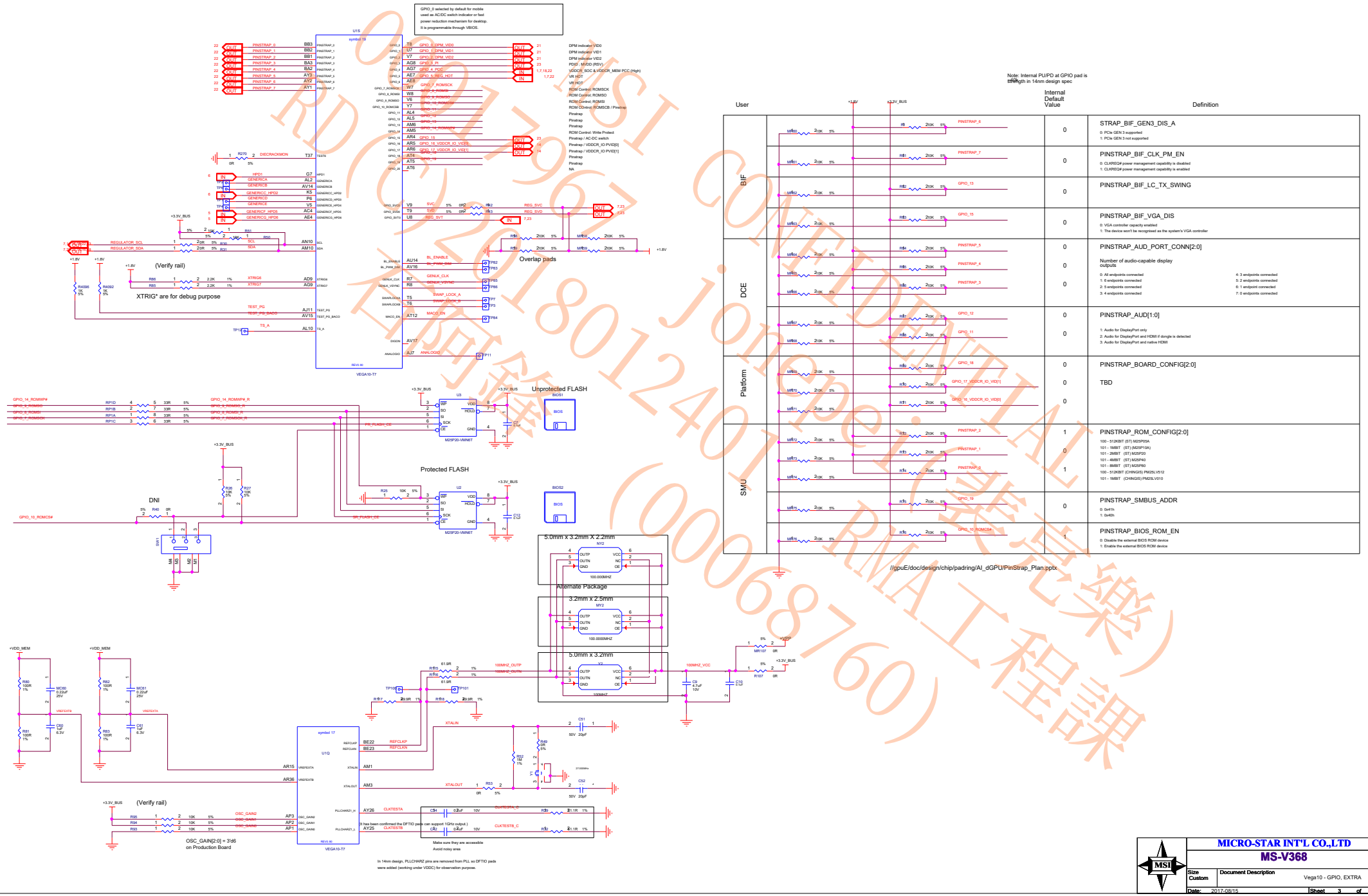
GPIO_0 selected by default for mobile used as AC/DC switch indicator or fast power reduction mechanism for desktop. It is programmable through VBIOS.
Note: Internal PU/PD at GPIO pad is strength in 14nm design spec
User
Internal Default Value
Definition
BIF
DCE
Platform
SMU
STRAP_BIF_GEN3_DIS_A
0: PCIe GEN 3 supported
1: PCIe GEN 3 not supported
PINSTRAP_BIF_CLK_PM_EN
0: CLKREQ# power management capability is disabled
1: CLKREQ# power management capability is enabled
PINSTRAP_BIF_LC_TX_SWING
PINSTRAP_BIF_VGA_DIS
0: VGA controller capacity enabled
1: The device won't be recognised as the system's VGA controller
PINSTRAP_AUD_PORT_CONN[2:0]
Number of audio-capable display outputs
0: All endpoints connected
1: 6 endpoints connected
2: 5 endpoints connected
3: 4 endpoints connected
4: 3 endpoints connected
5: 2 endpoints connected
6: 1 endpoint connected
7: 0 endpoints connected
PINSTRAP_AUD[1:0]
1: Audio for DisplayPort only
2: Audio for DisplayPort and HDMI if dongle is detected
3: Audio for DisplayPort and native HDMI
PINSTRAP_BOARD_CONFIG[2:0]
TBD
PINSTRAP_ROM_CONFIG[2:0]
100 - 512KBIT (ST) M25P05A
101 - 1MBIT (ST) (M25P10A)
101 - 2MBIT (ST) M25P20
101 - 4MBIT (ST) M25P40
101 - 8MBIT (ST) M25P80
100 - 512KBIT (CHINGIS) PM25LV512
101 - 1MBIT (CHINGIS) PM25LV010
PINSTRAP_SMBUS_ADDR
0: 0x41h
1: 0x40h
PINSTRAP_BIOS_ROM_EN
0: Disable the external BIOS ROM device
1: Enable the external BIOS ROM device
//gpuE/doc/design/chip/padring/AI_dGPU/PinStrap_Plan.pptx
(Verify rail)
XTRIG* are for debug purpose
Overlap pads
Unprotected FLASH
Protected FLASH
DNI
5.0mm x 3.2mm X 2.2mm
Alternate Package
3.2mm x 2.5mm
5.0mm x 3.2mm
OSC_GAIN[2:0] = 3'd6
on Production Board
It has been confirmed the DFTIO pads can support 1GHz output.)
Make sure they are accessible
Avoid noisy area
In 14nm design, PLLCHARZ pins are removed from PLL so DFTIO pads were added (working under VDDC) for observation purpose.
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Vega10 - GPIO, EXTRA
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Size: Custom	Document Description: Vega10 - TMDPAB 1xDP, 1xHDMI & +5V VESA	Rev: 1.1
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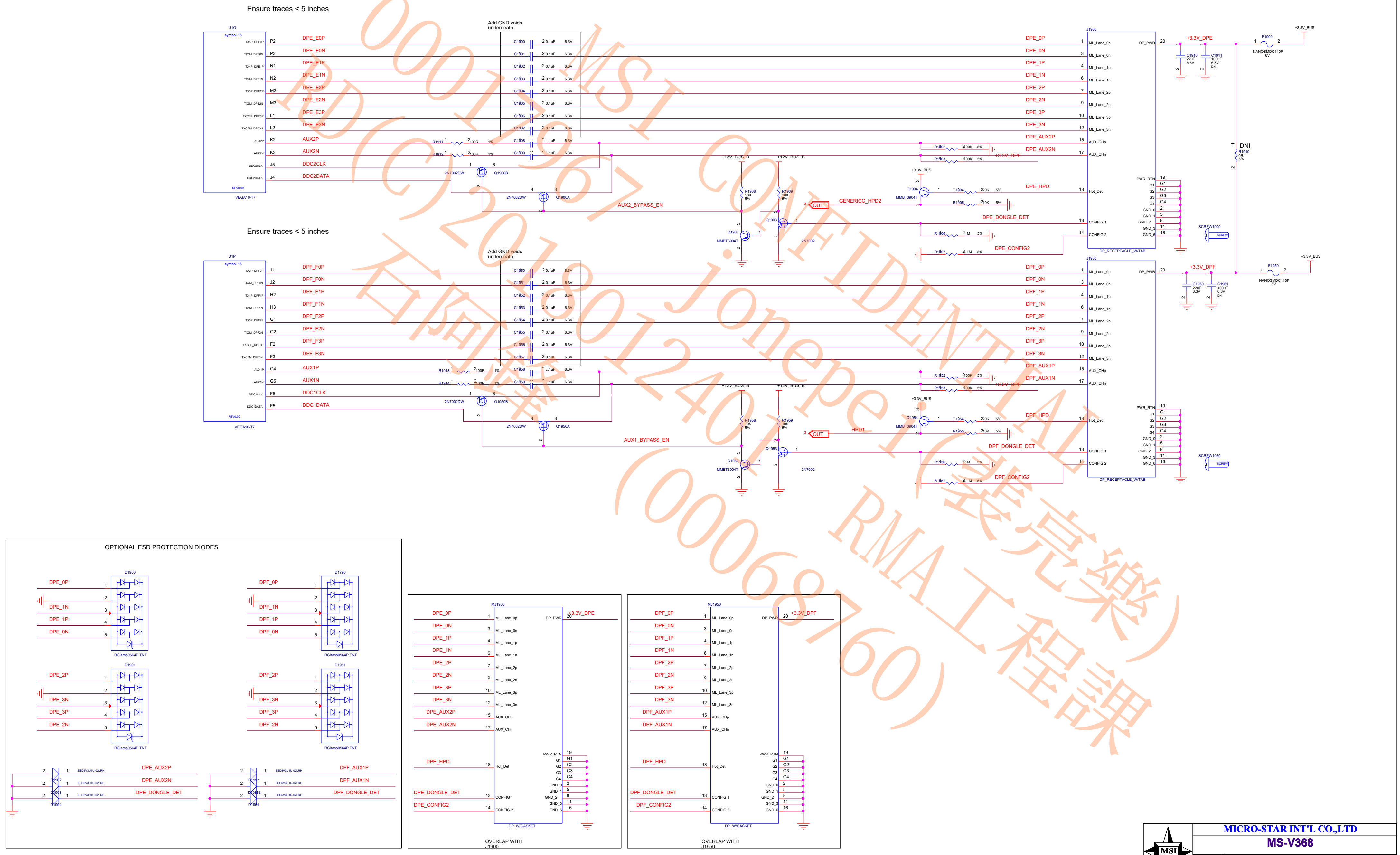

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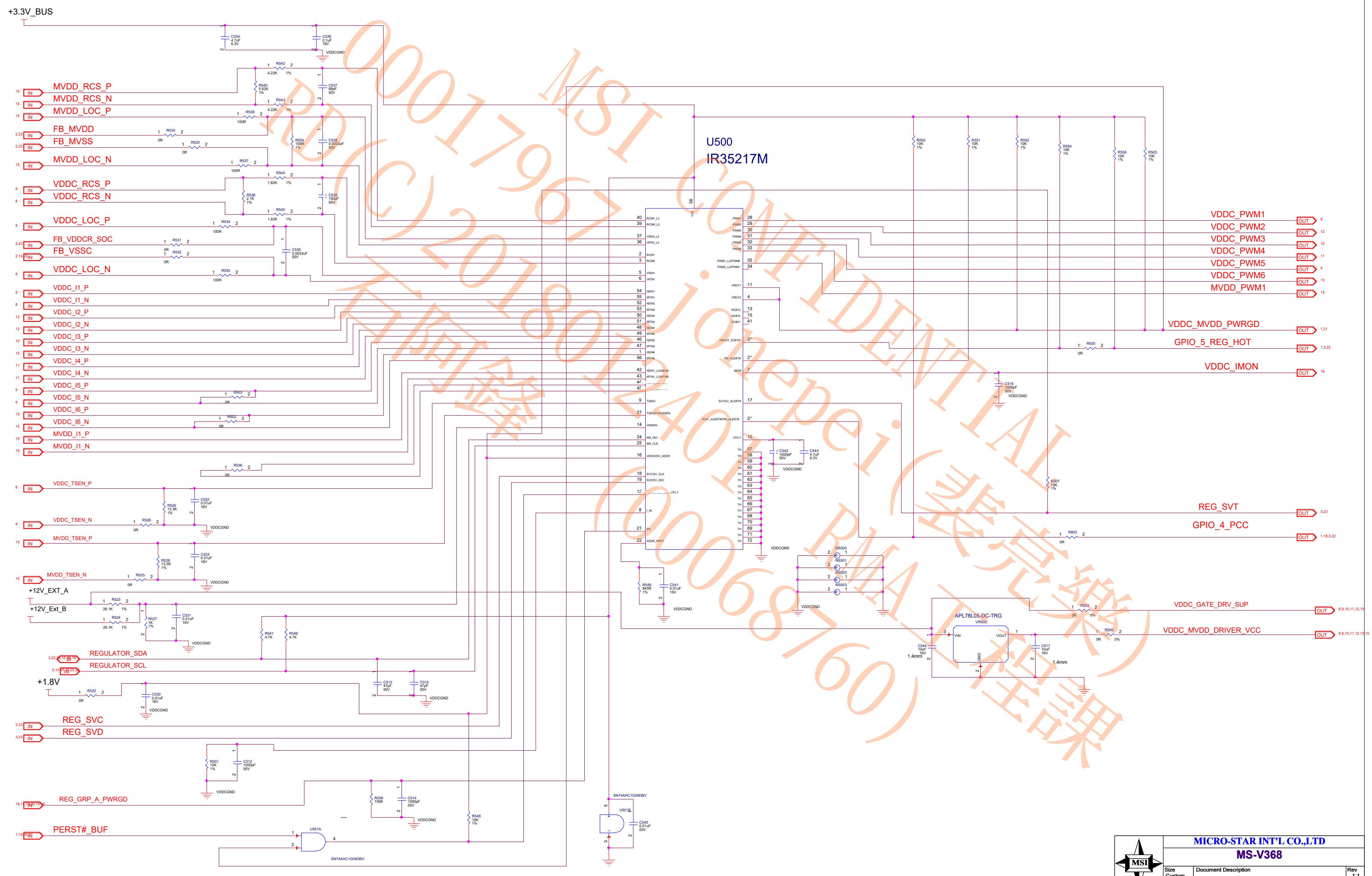

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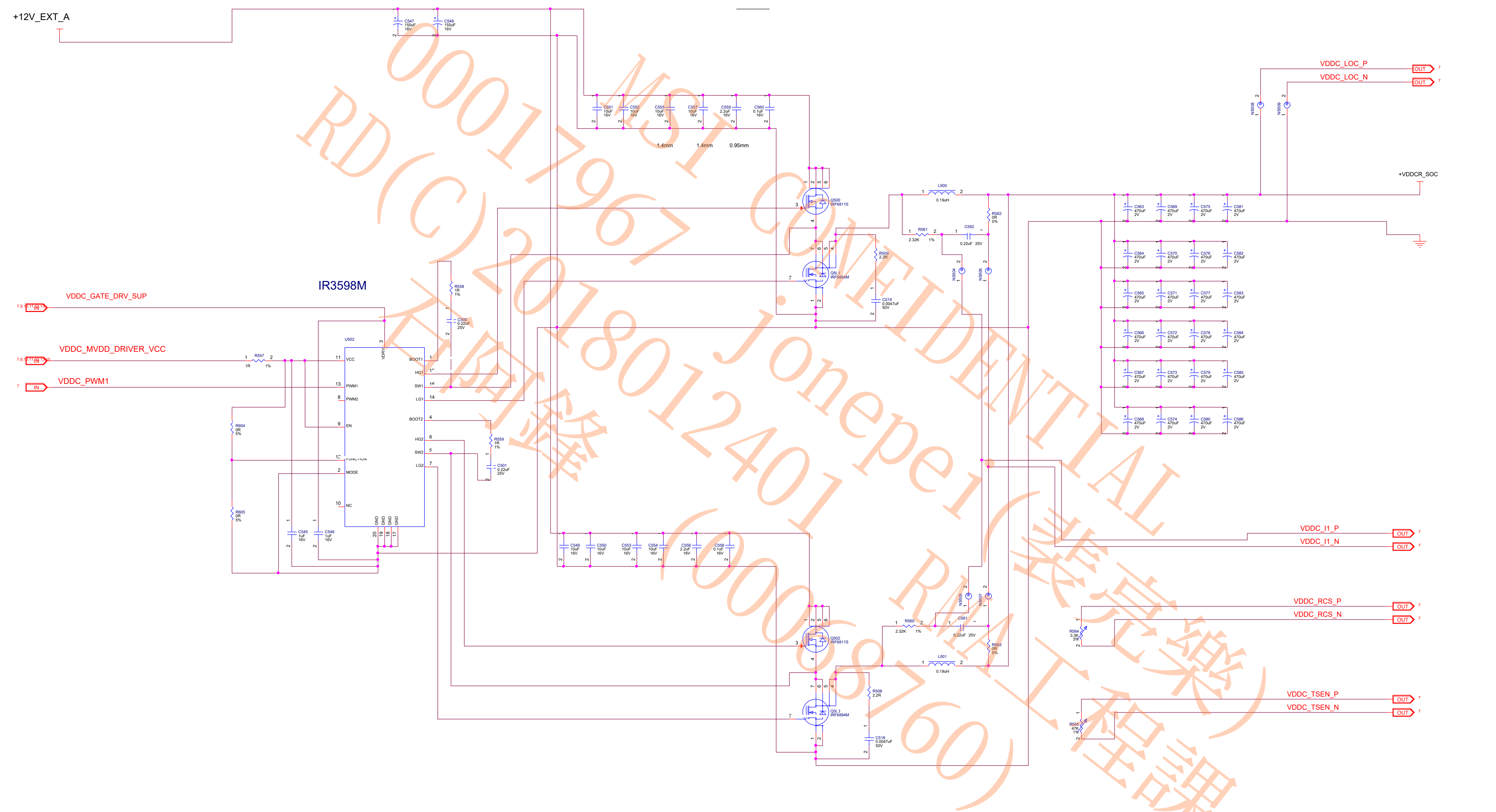

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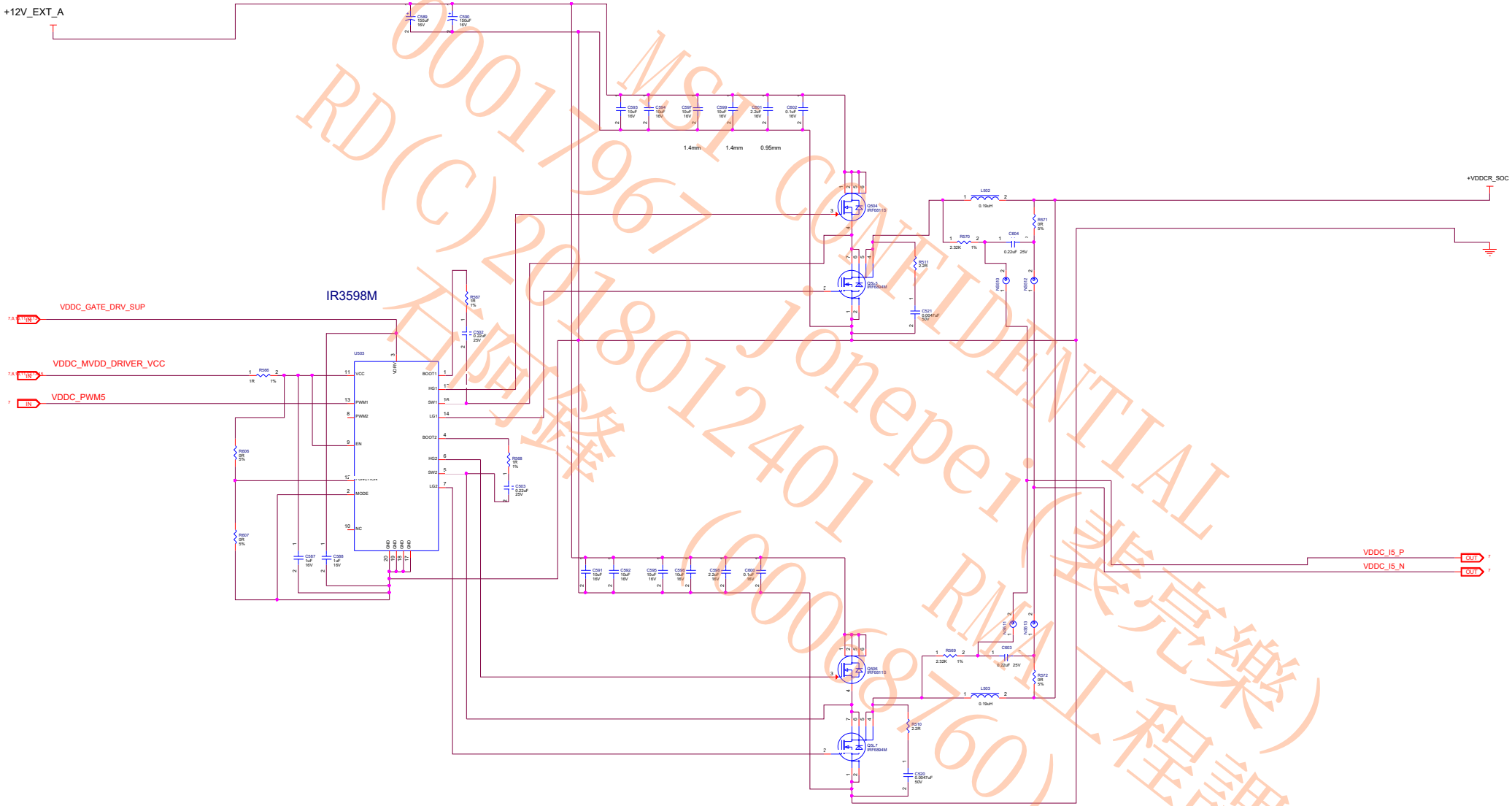

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Size: Custom	Document Description: Reg - VDDCR_SOC PHASES V and XI	Rev: 1.1
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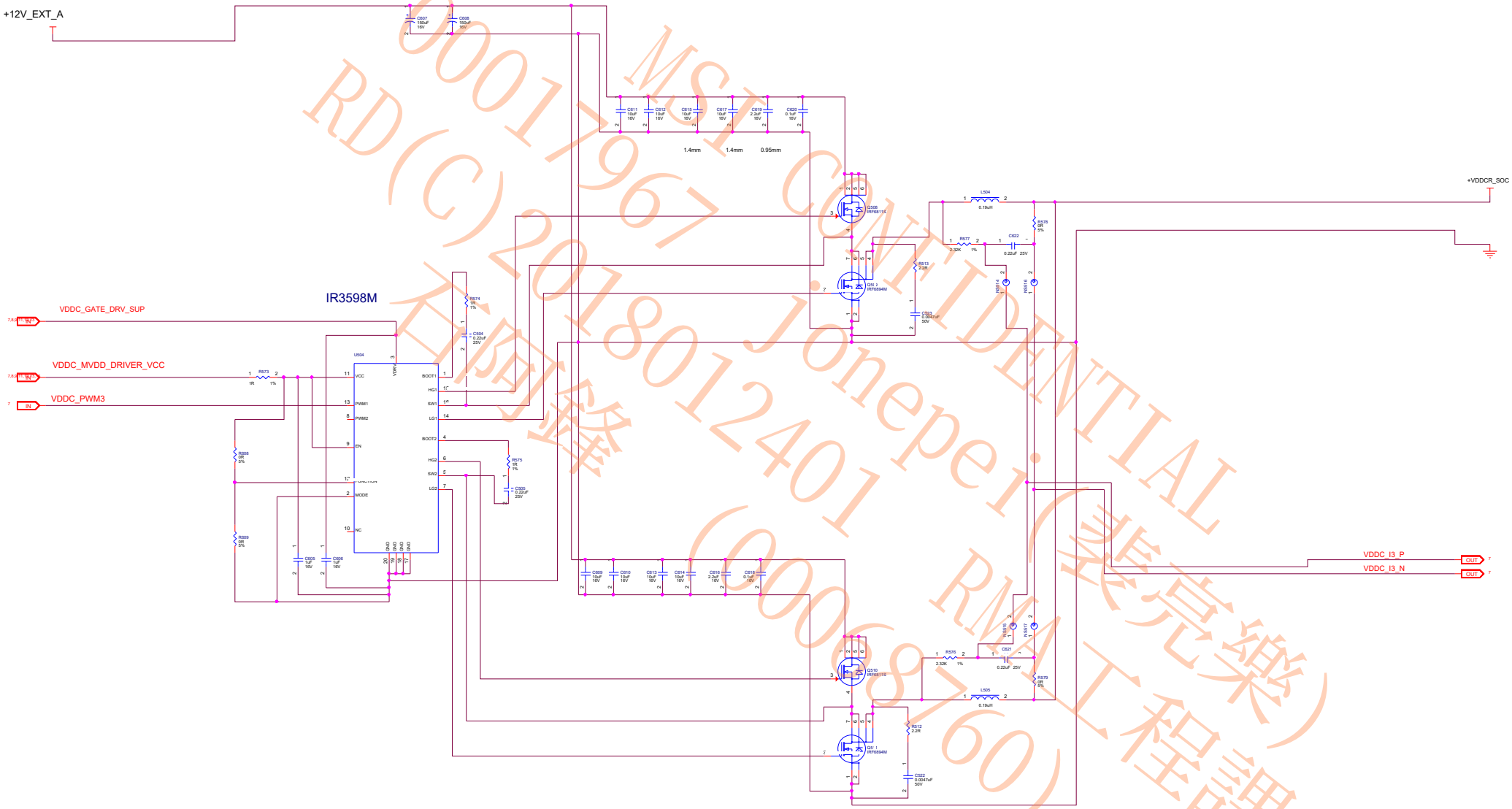

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Size: Custom	Document Description: Reg - VDDCR_SOC PHASES III and IX	Rev: 1.1
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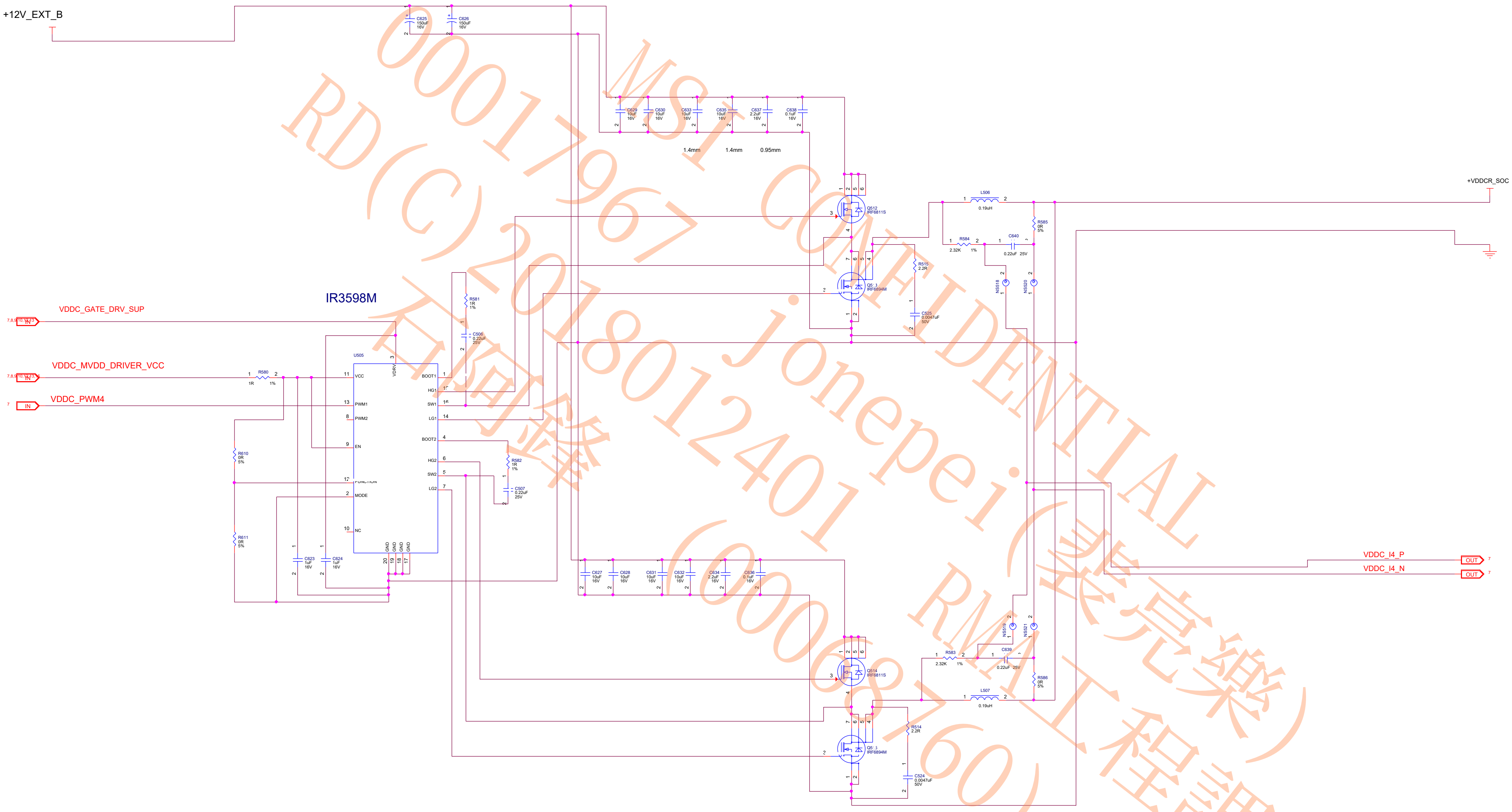

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Size	Document Description	Rev
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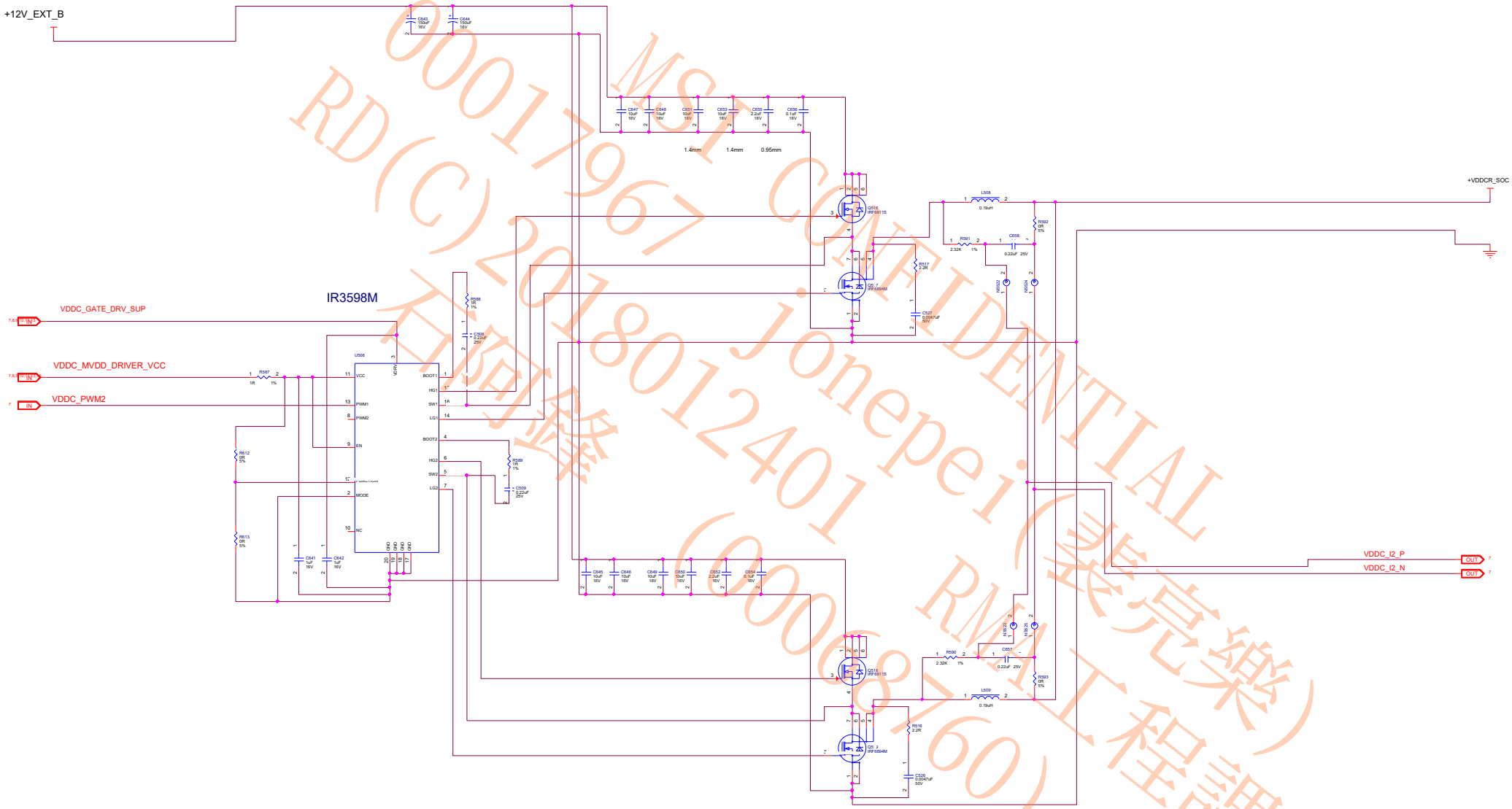

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Size: Custom	Document Description: Reg - VDDCR_SOC PHASES II and VIII	Rev: 1.1
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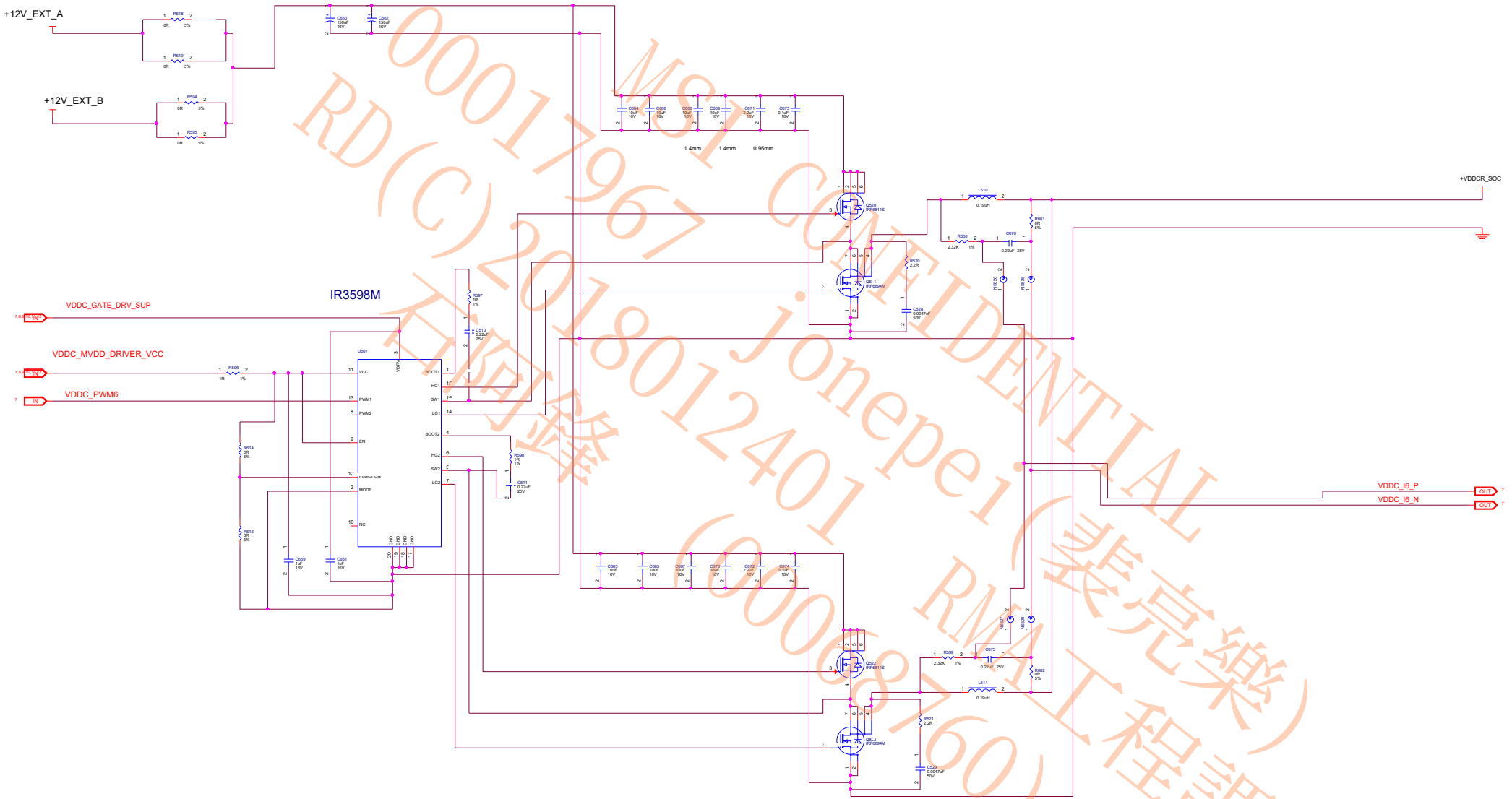

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Size: Custom	Document Description: Reg - VDDCR_SOC PHASES VI and XII	Rev: 1.1
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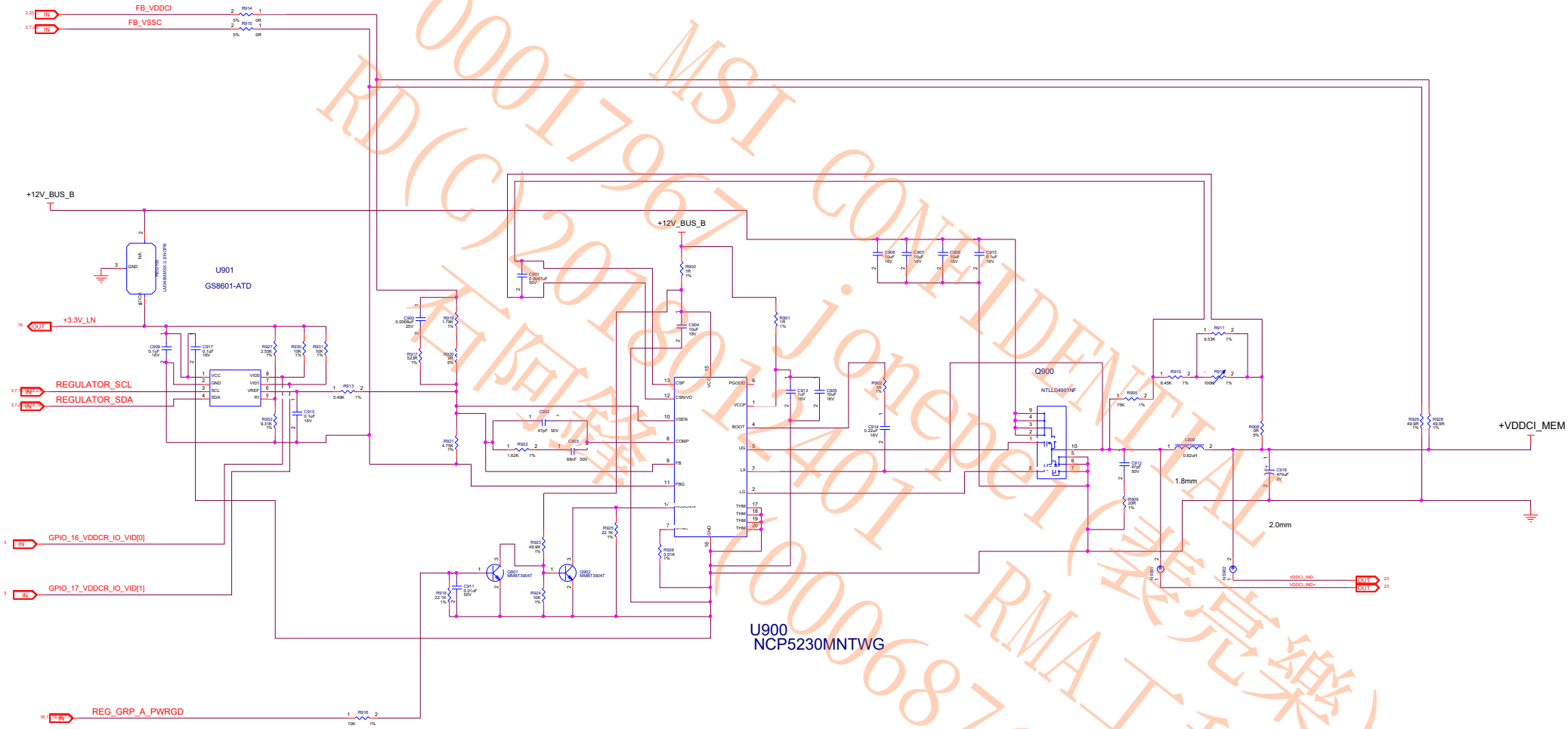

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Size: Custom	Document Description: Reg - VDDCR_IO	Rev: 1.1
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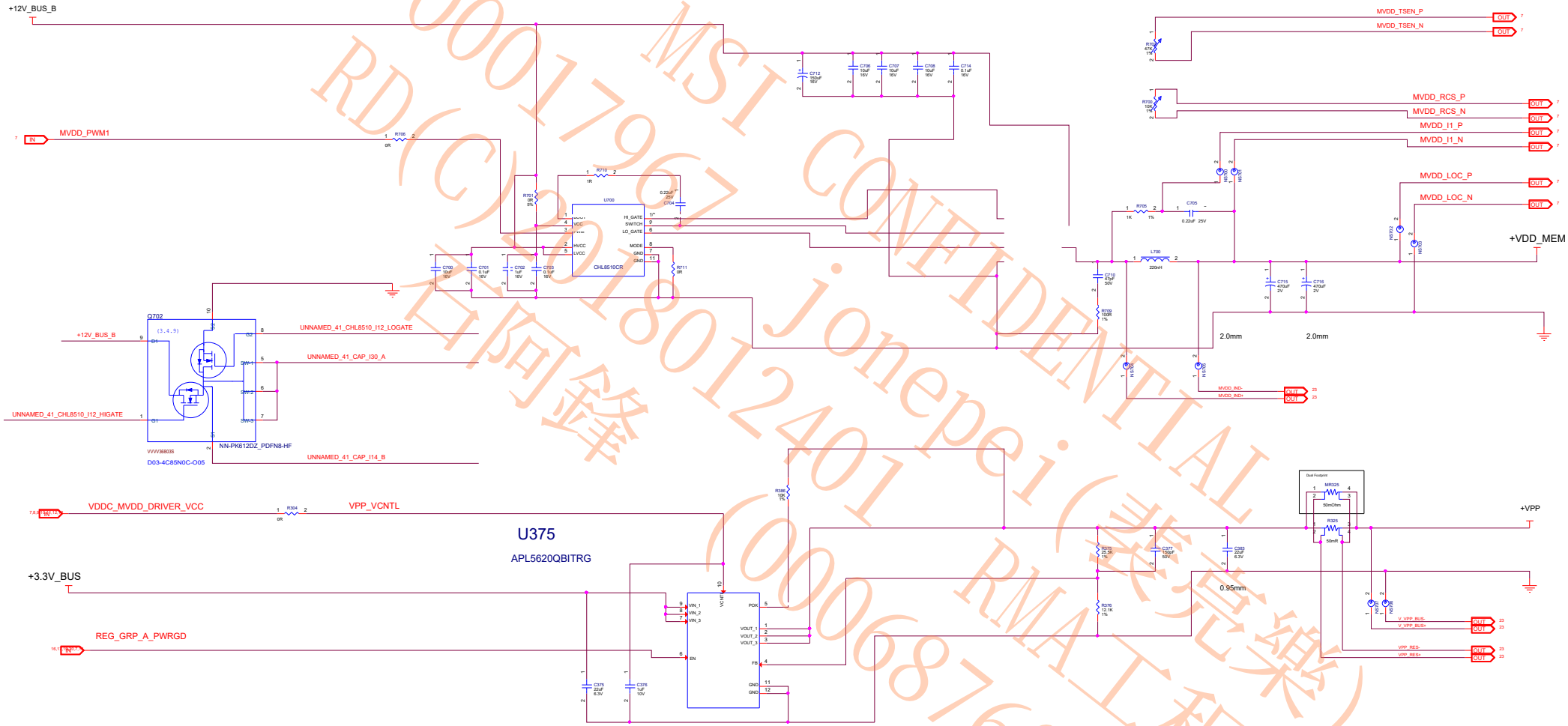

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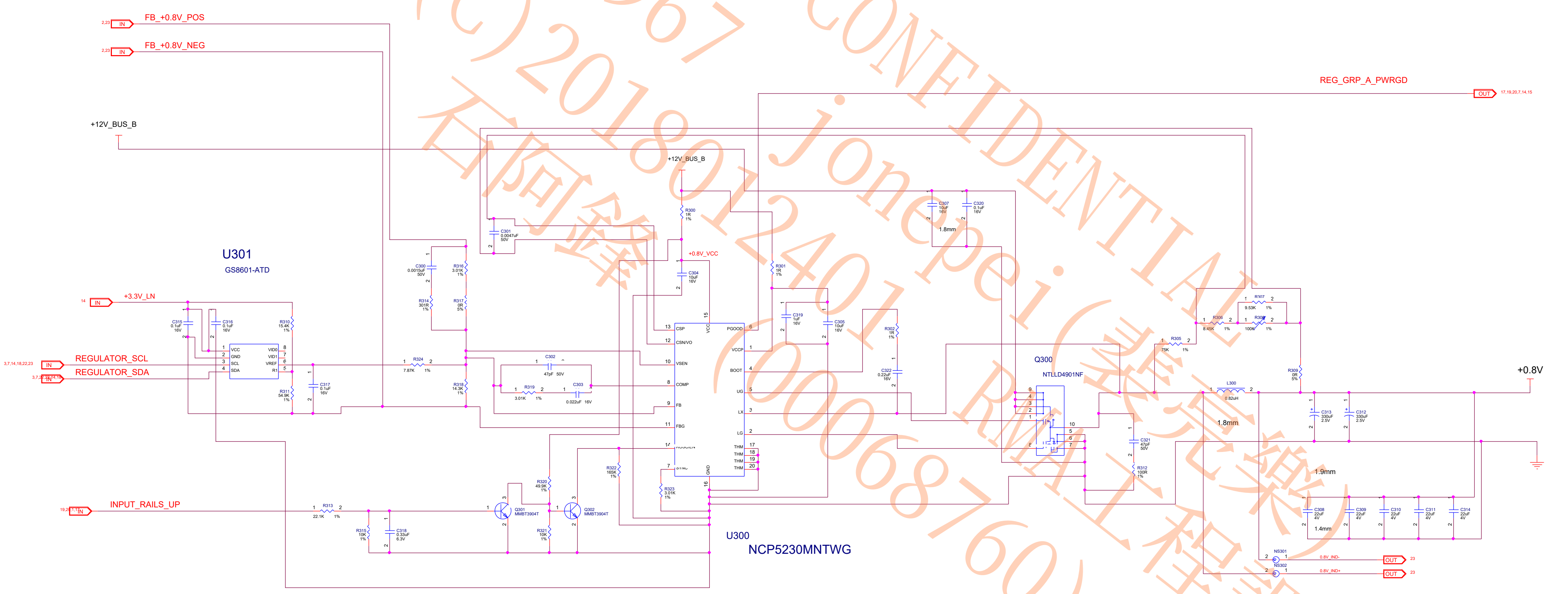

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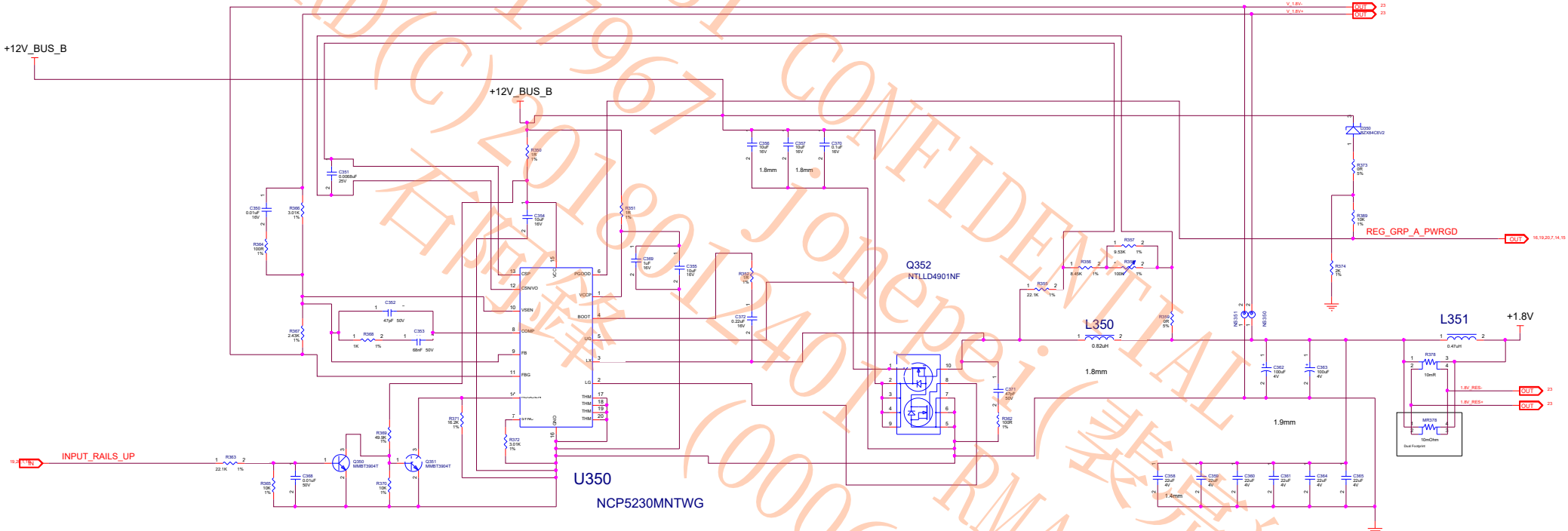

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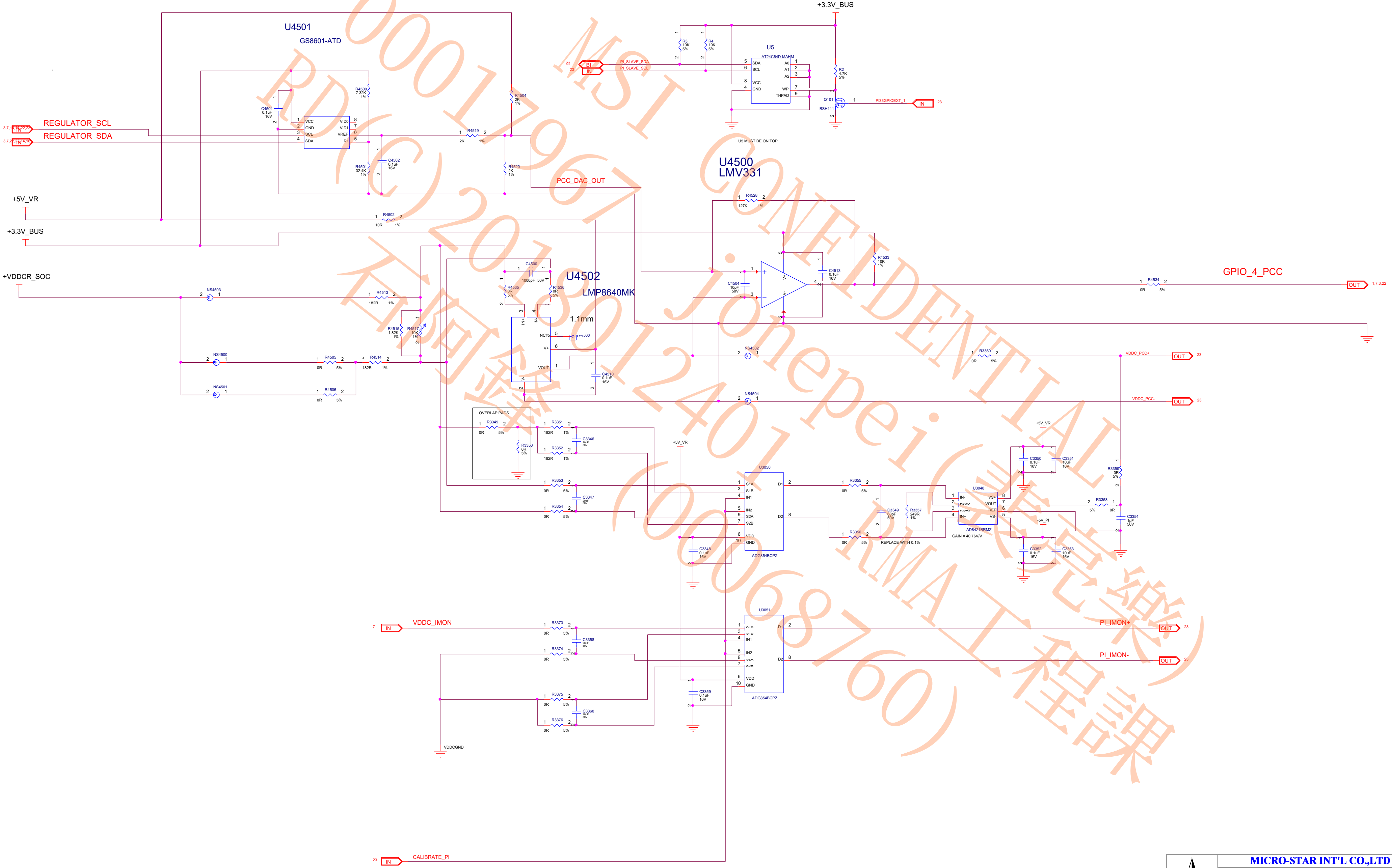

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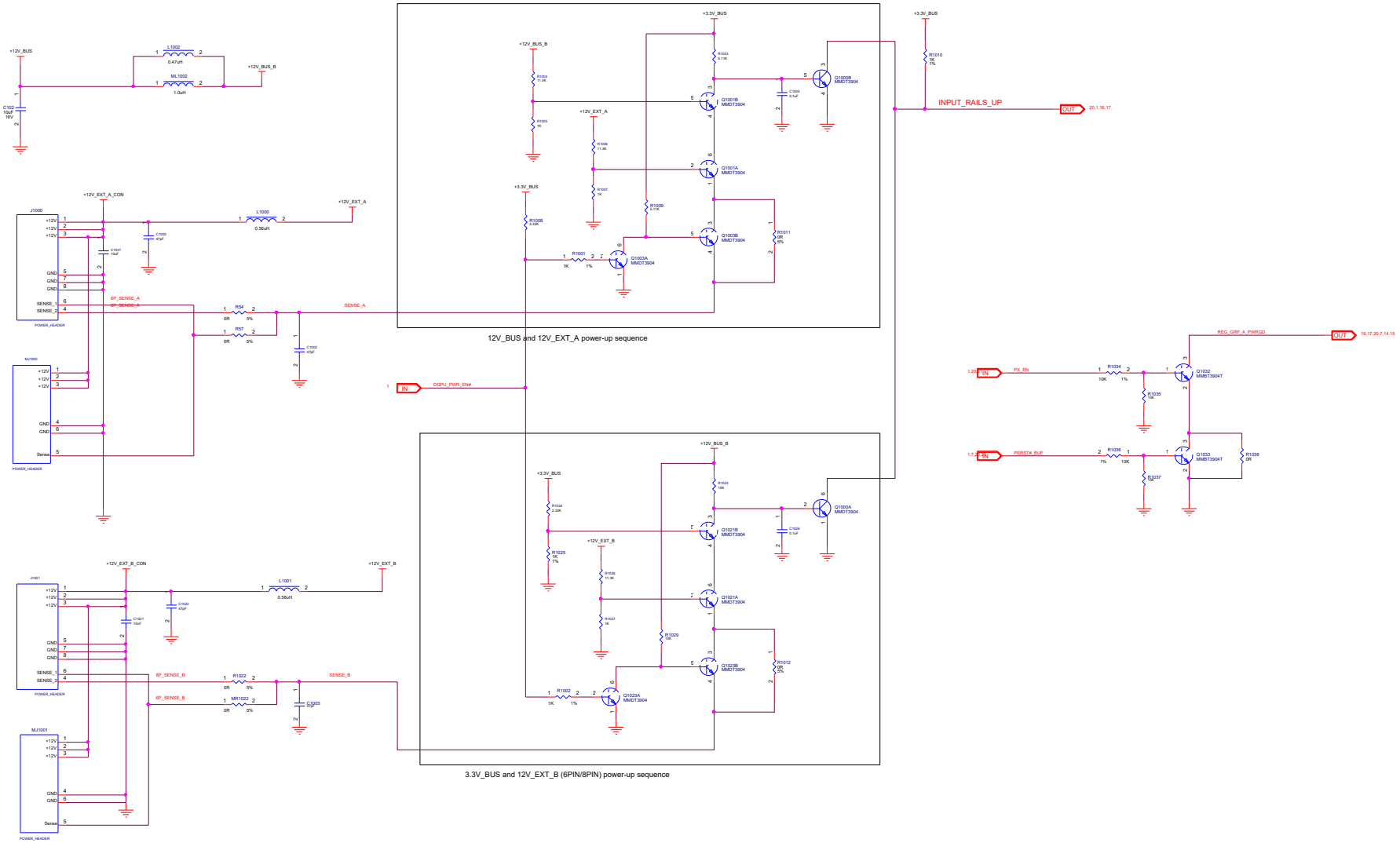

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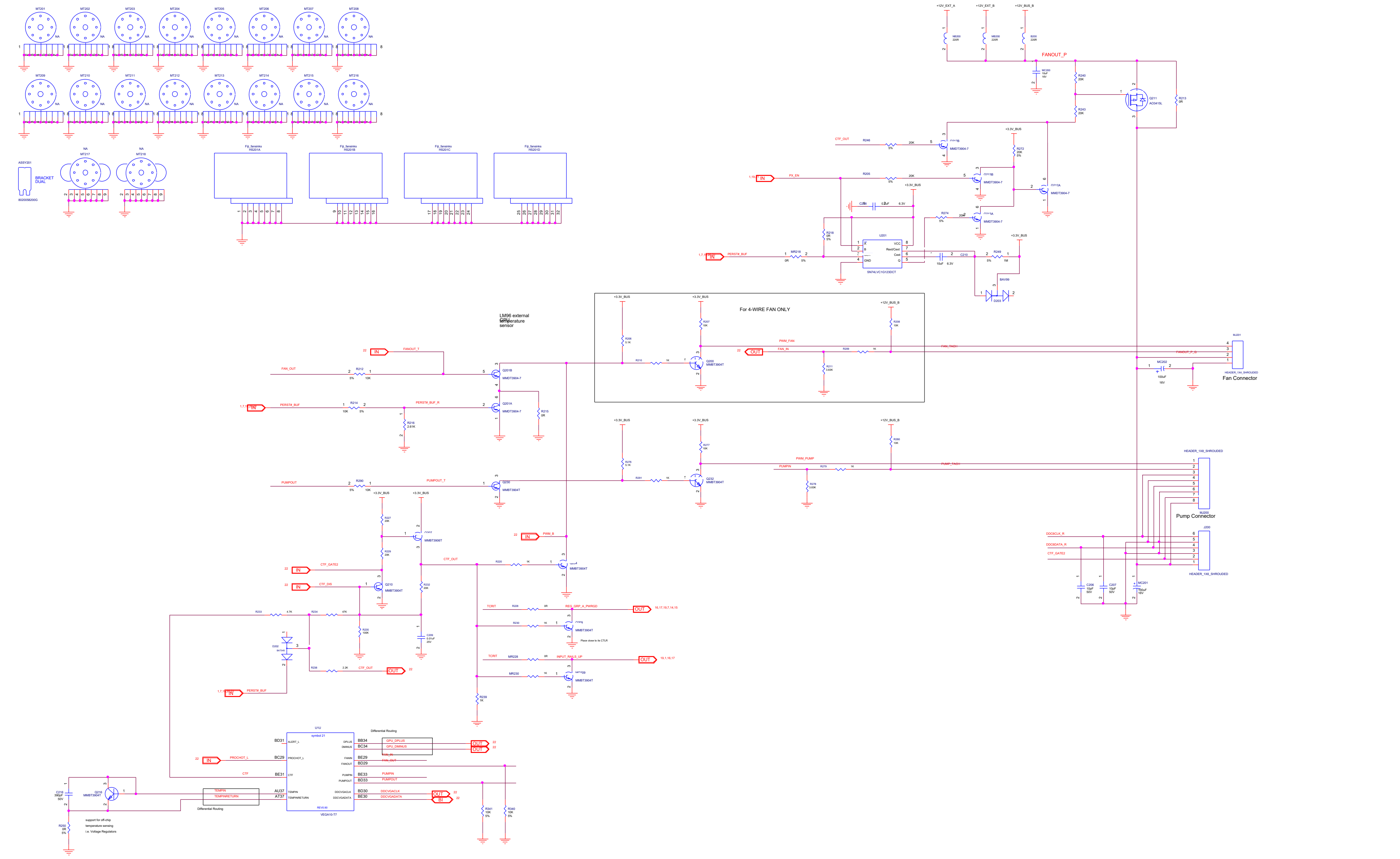

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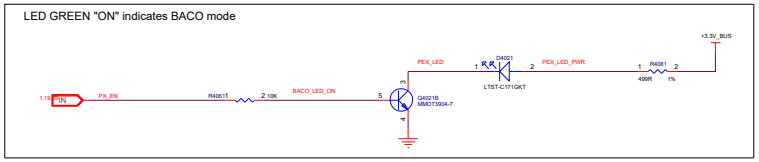

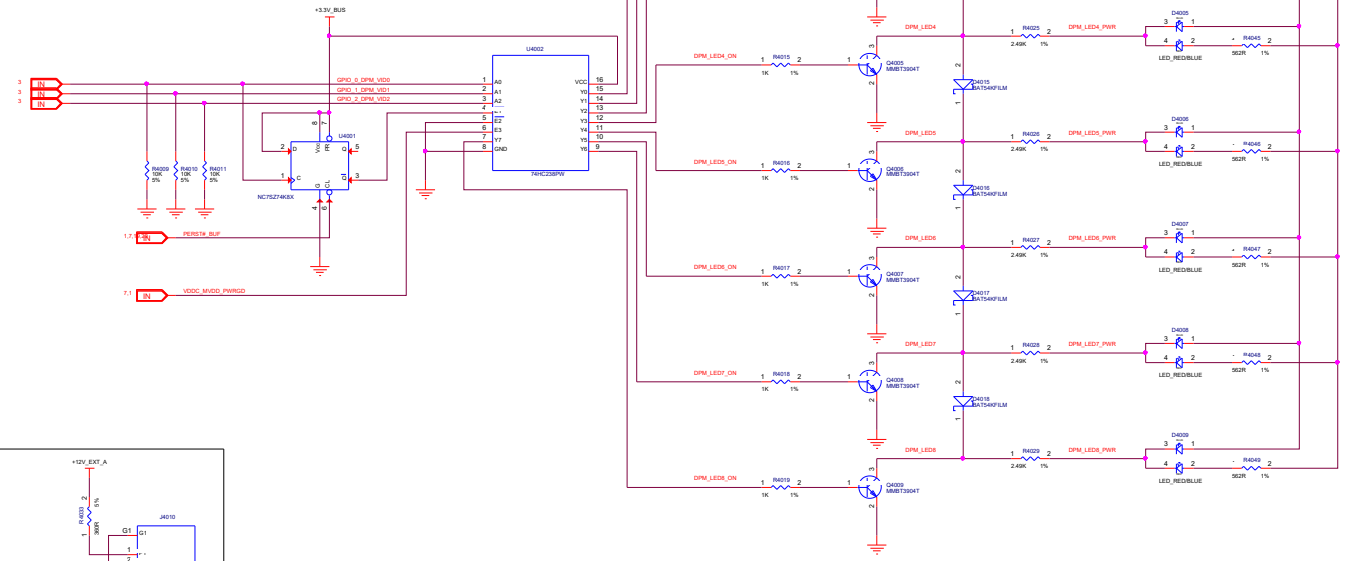

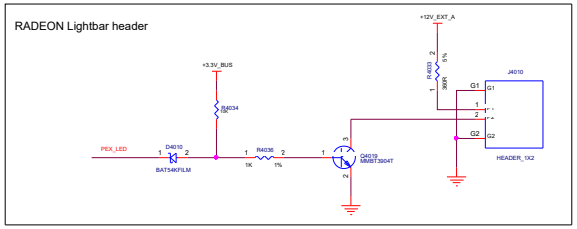

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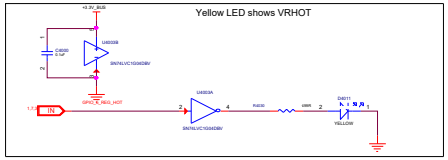

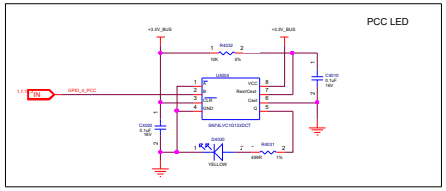

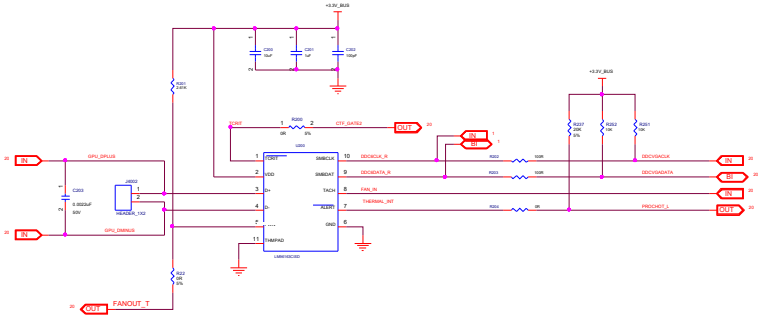

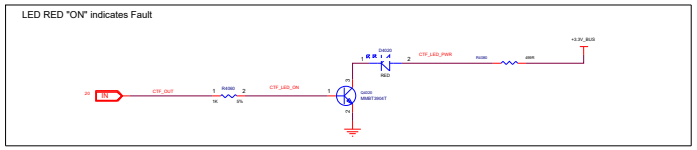

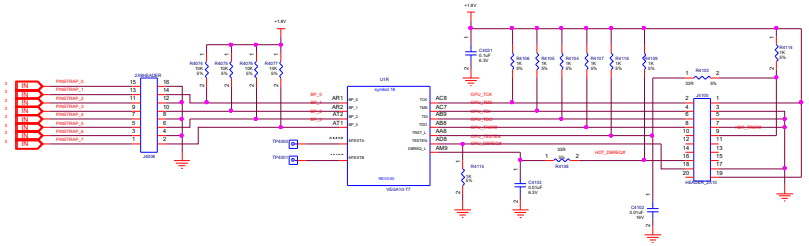

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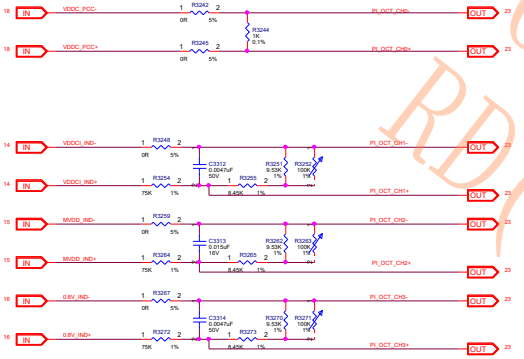
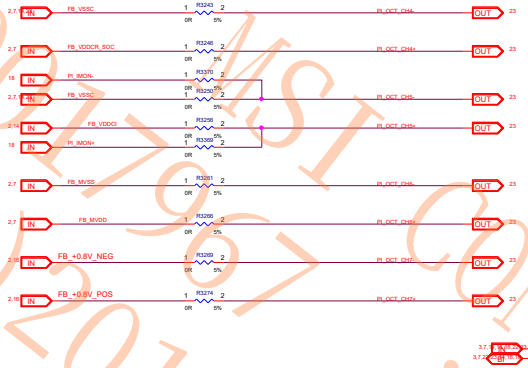
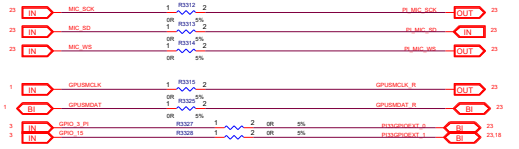
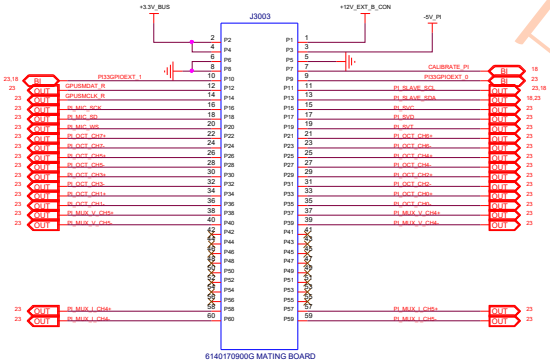
ALL COMPONENTS TO BE LOCATED NEXT TO SENSING ELEMENT (ON MAIN BOARD)
NETS IN GREEN SHOULD BE RE-NAMED

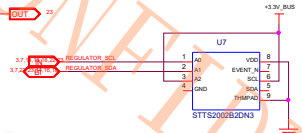




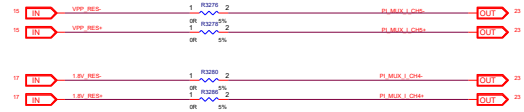


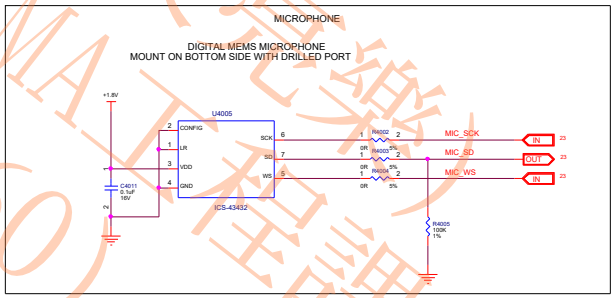
RESERVED FOR I2C_MASTER PINS





PLACE HOLDER FOR DS28C22
U7 MUST BE ON TOP





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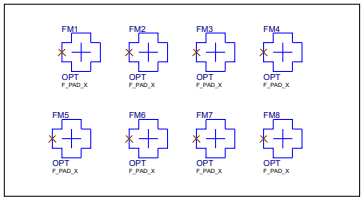

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A	10/9/15	Initial schematic creation
B	6/30/16	Many Changes on PI circuit , Minor Chnages on SMPS
C	9/30/16	Many Changes on PI circuit , ASIC SYMBOL UPDATED FOR FLASH ROM INTERFACE , flash ROM SI/SO swapped , RP1 added
D	11/29/16	Changes on PI circuit , 100MHz HCSL clock source replced (contact AMD for detailes)
E	01/05/17	PI circuit removed , 200R added to DP AUX (6 resistors)
F	02/02/17	1.8V/VPP Kelvin resistors dual footprinted , DP AUX (6 resistors changed to 100R) , Changed R4033 to 360R 1206 and moved to 12V_AUX , SMBUS Address note swap , J4001 removed , R115/R116 changed to 61.9R , R205 added
G	06/29/17	Re-Name to MSI Lable
H	08/15/17	Remove R1013,R1014,R1015,R106 and V_12V_BUS,V_12V_EXTA,V_12V_EXTB,V_3.3V_BUS, 12V_BUS_RES,12V_EXTA_RES,12V_EXTB_RES,3.3V_BUS_RES
I	08/16/17	Change J3003 footprint name from con_mating_samtec_fsi-130-03-x-d-m-ad to con_mating_samtec
I	08/17/17	Remove TP102/105/126/127/106/108/107/106/128/129/110/111/112/113/130/131/114/116/115/117/132/133/118/119/120/121/134/135/122/124/123/125. Change Q702 Footprint , Rename Page 24 to MECH and add 8 + light Point