

P1041-B01 GF104

GF104-300, 768MB/1536MB, GDDR5 192b 32M/64Mx32
DVI-I-DL, DVI-I-DL/DP, mHDMI

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變更記錄

- P3 , C55 change to 1206 10u
P4~P14 , add 跳頁&‘<>’符號
P14,刪除所有網絡線
P17 , add 6262 IC
P25,刪除原公版U2 & J501. 把I2CC接到6262IC
P27,接PS1_1V05_FB到6262,U4 foot_print 改為十字的
P28,改U8的FB接法 , 換L6為L04-22A8011-L65
P29 , core部份PWM換UP6213+6284 , OFS電壓開關抬50mV 。
頻率def400KHz , 開關抬到600KHz.
P30-31 , 加driver IC 6284 ; 去掉3顆input 電容 ; 同時增加6個
LED燈 , 增加CP1~CP12 ; 為精簡線路 , 刪除L mos端與
DRVL 0OHm電阻 , 刪除CSP , CSN 0Ω電阻 ; 更換MOS
& 電感 ; power前4相由PEX6_F1提供 , 后2相由PEX6_F2
提供 ; 電容部份保留公版。
P32,去除input 端12V 的LB電感
P33,加防彎條mec100 , 加6個十字光學點 , 加NVVDD , FBVDD
&pex_vdd的測試點, 增加阻抗條

REV	VARIANT	W/PN	ASSEMBLY
B	BASE	600-11041-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-11041-0000-300	P1041 GF104-300 768MB GDDR5 32Mx32 DVI-I+HDMI Frame Buffer
2	SKU0010	600-11041-0010-300	P1041 GF104-300 1536MB GDDR5 32Mx32 DVI-I+HDMI Frame Buffer
3	Q01	600-11041-0000-Q01	P1041 GF104-300 768MB GDDR5 32Mx32 Frame Buffer DVI-I+HDMI
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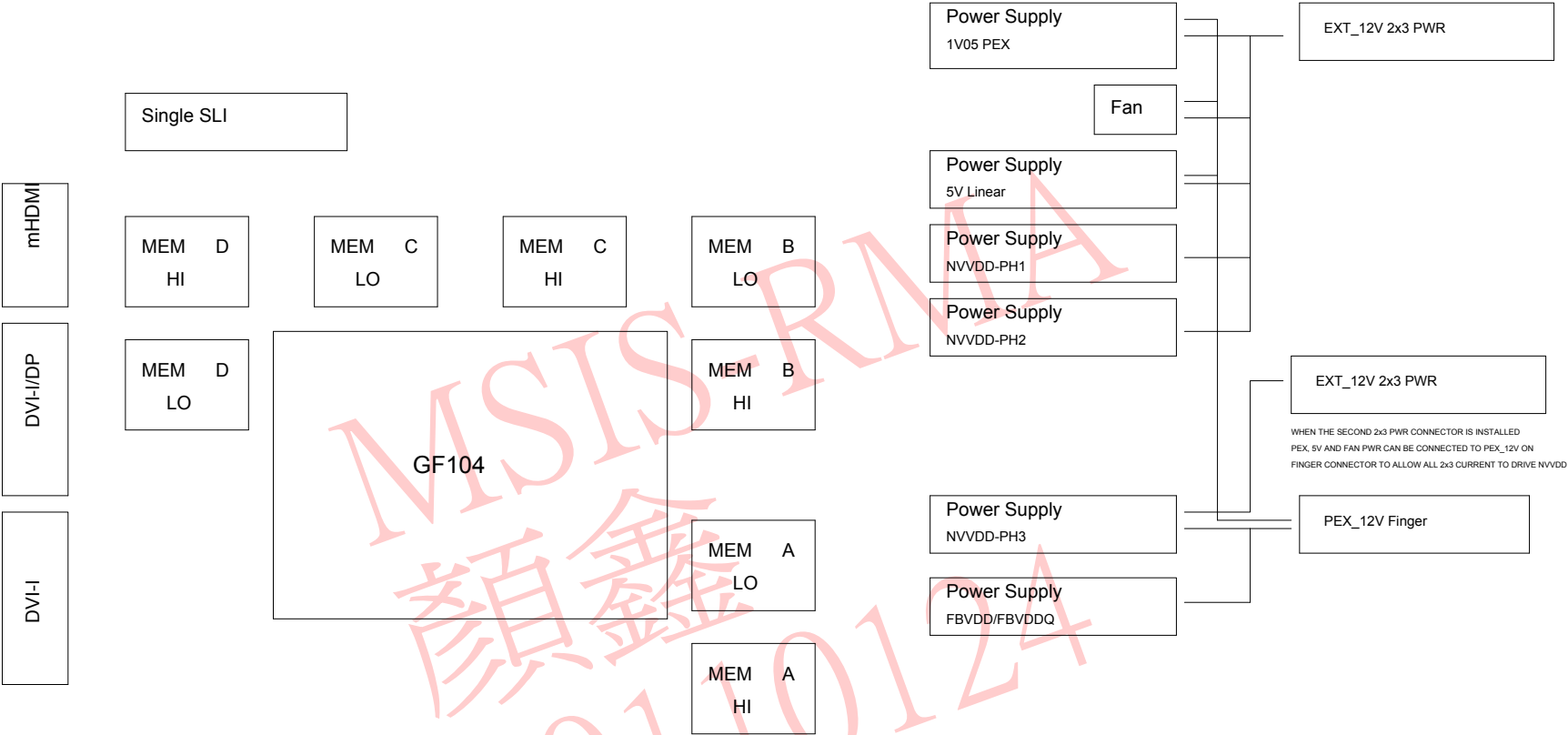
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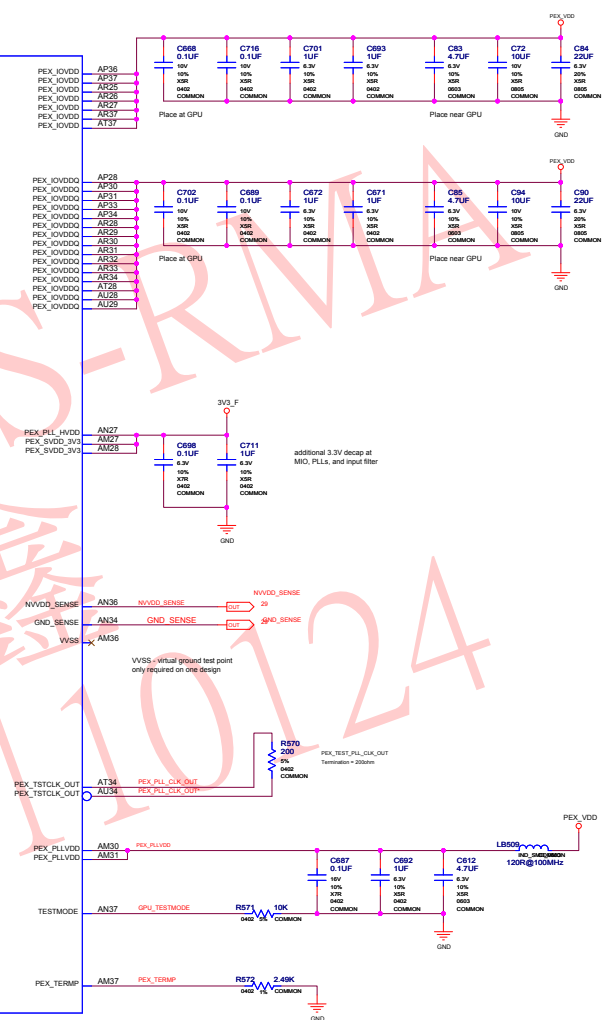
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ASSEMBLY	BASIC LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STORY ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Block Diagram

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NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
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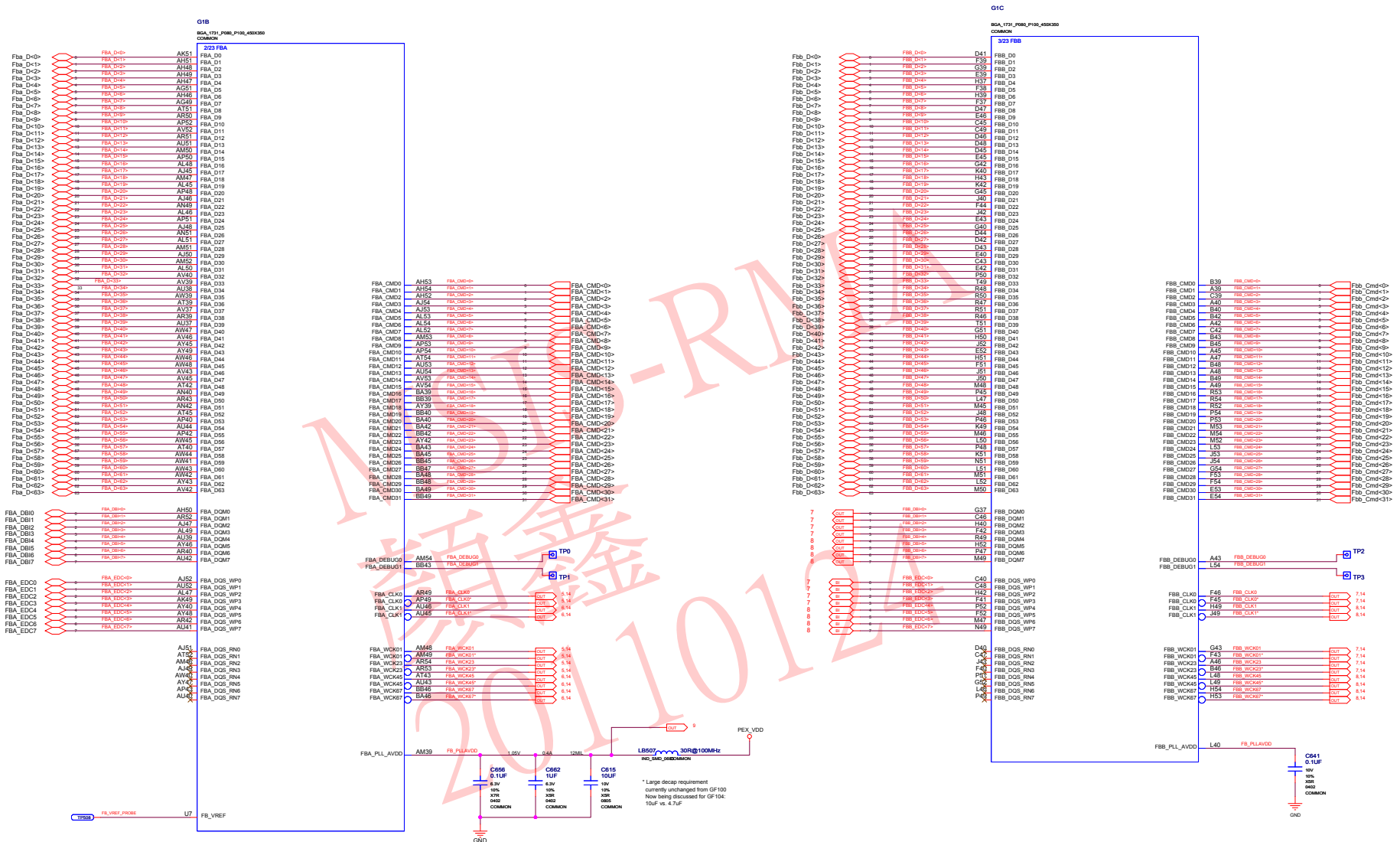
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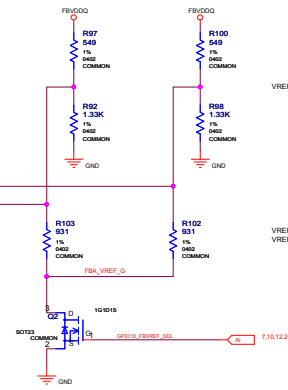
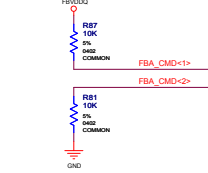
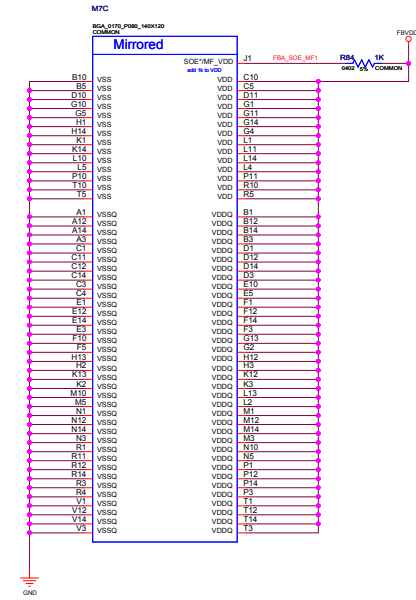
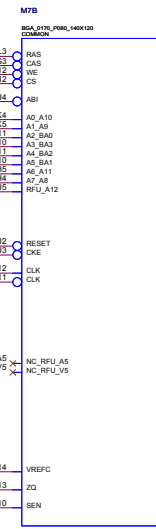
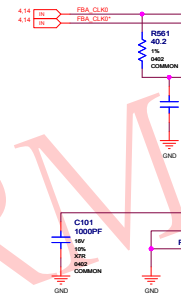
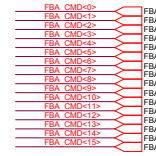
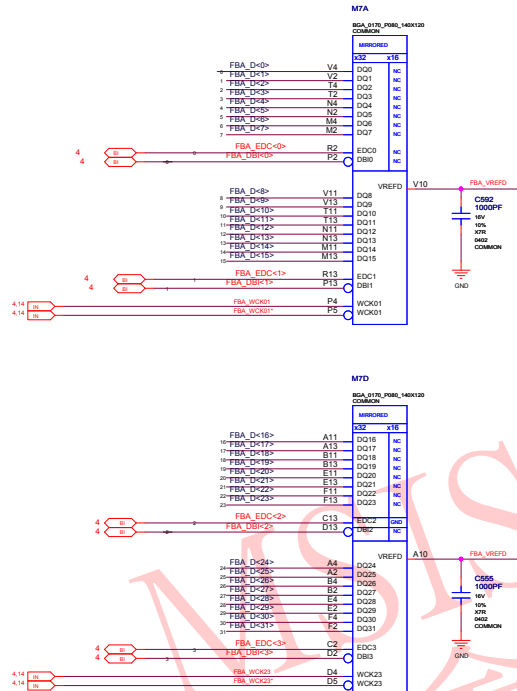
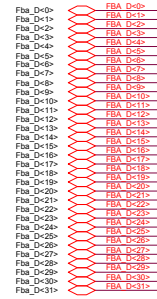
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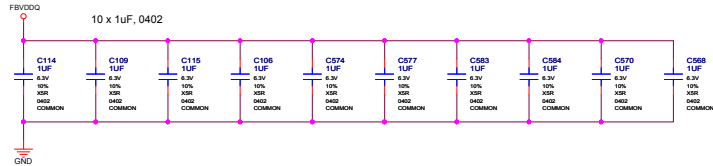
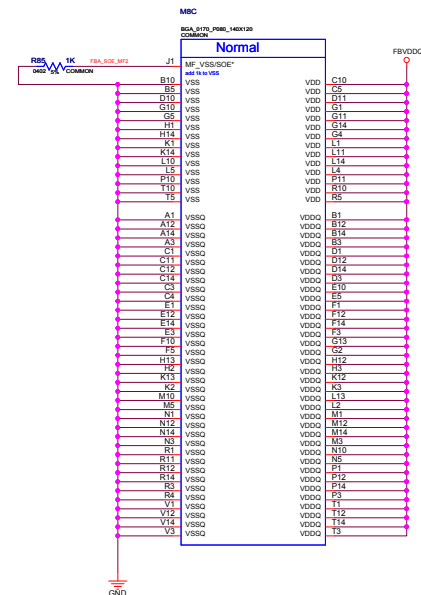
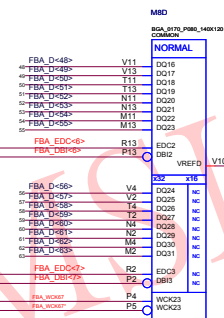
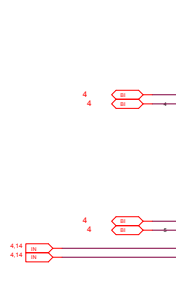

$$V_{REF} = 1.35 - [(542/542+549)] = 0.67V$$


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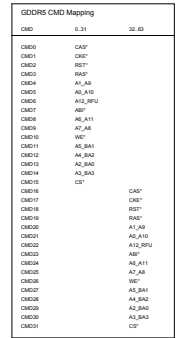
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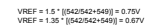
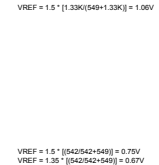
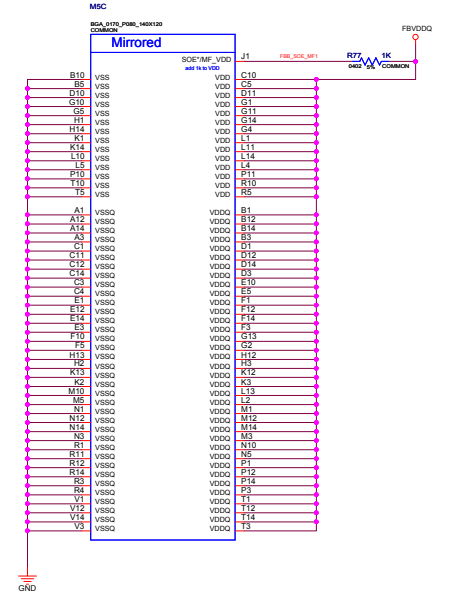
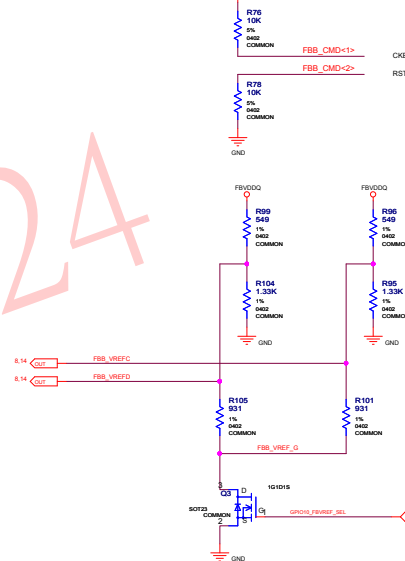
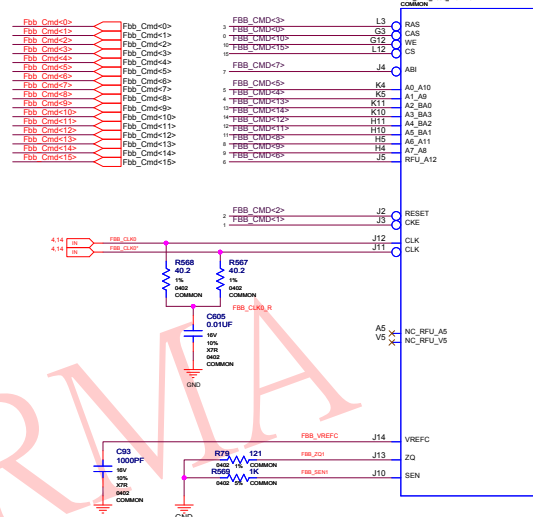
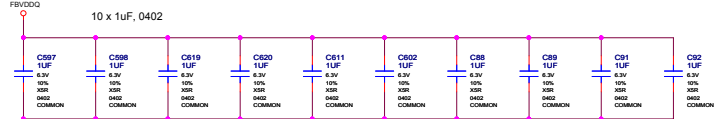
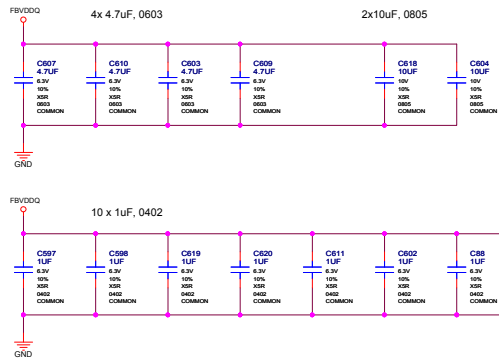
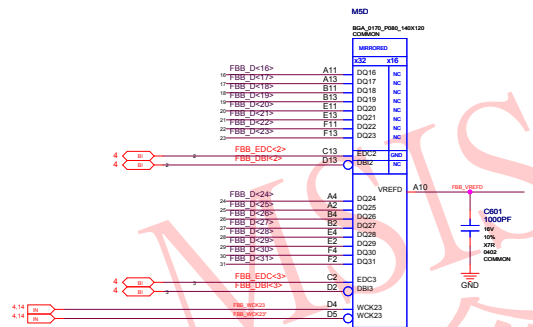
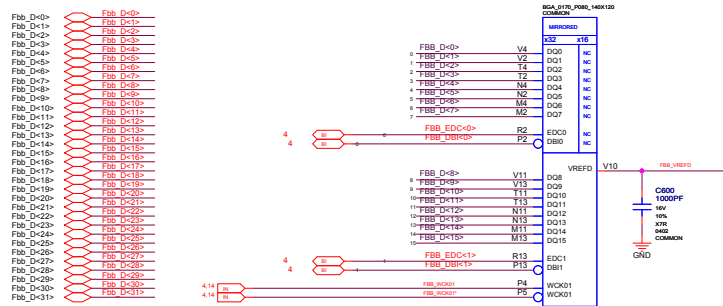
- internal Vref should be POR for VrefID
- potential for update



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- ** Vref switching options:
 - internal Vref should be POR for VrefID
 - potential for update



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PAGE DETAIL	FBB Part00 31..0

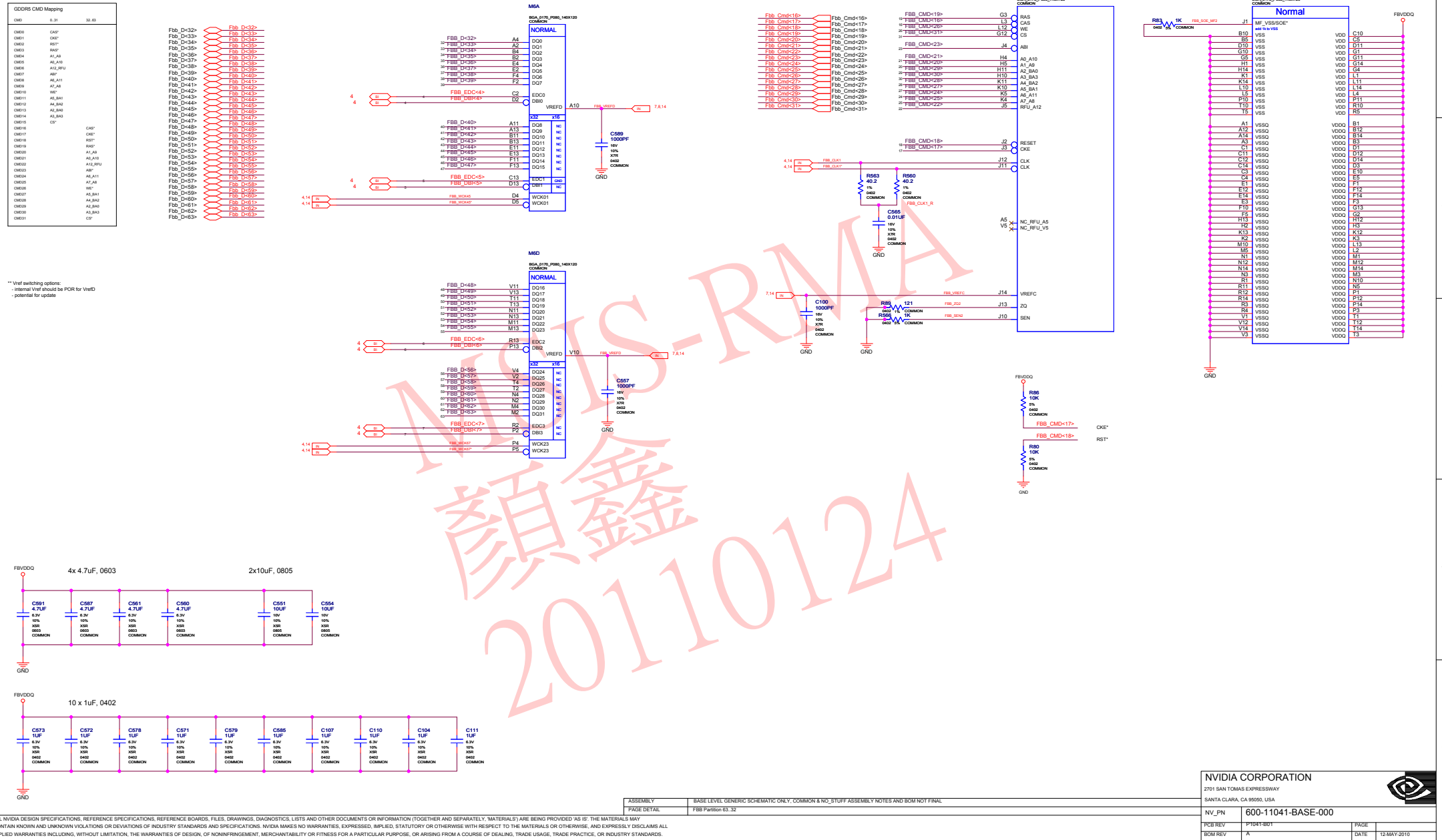
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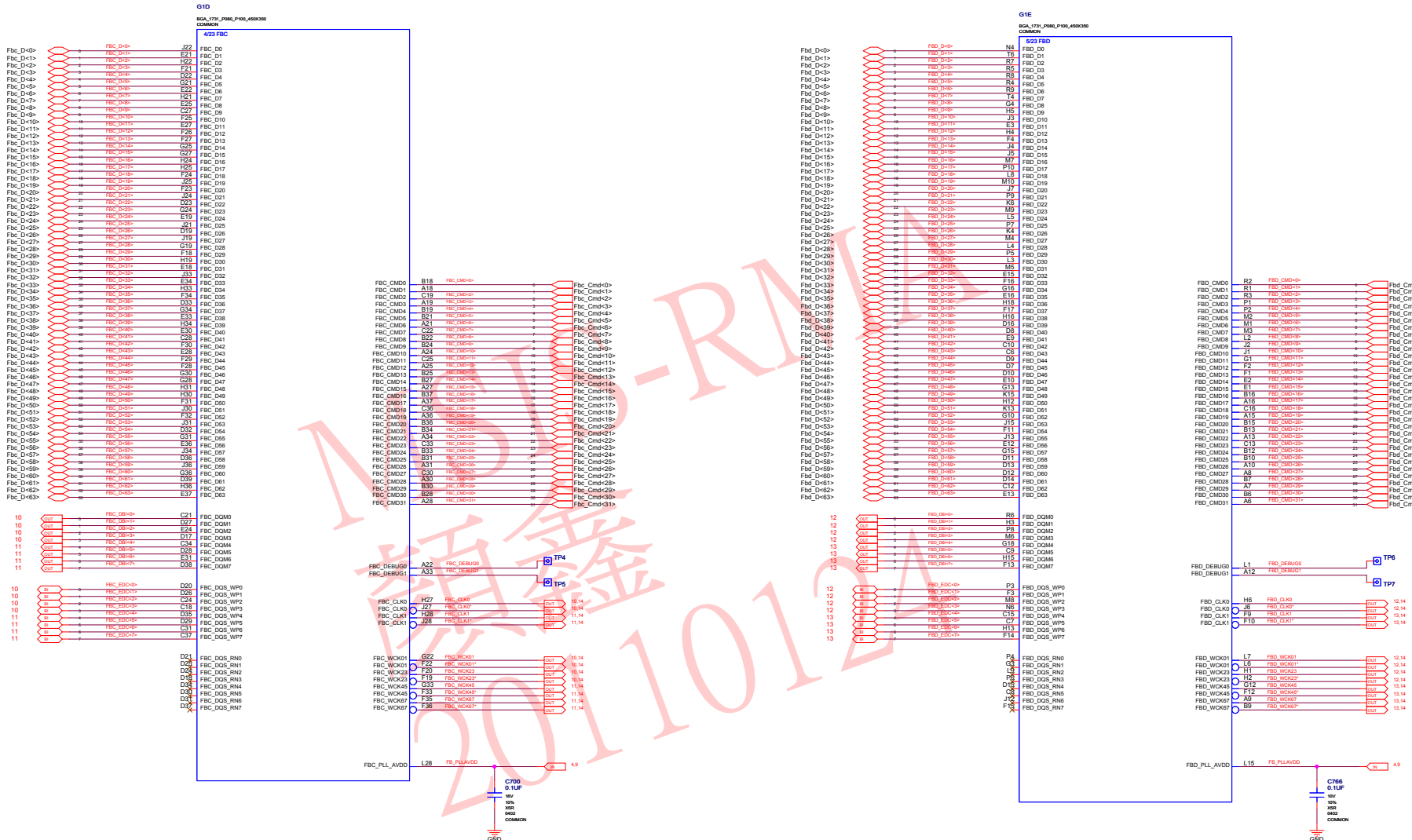
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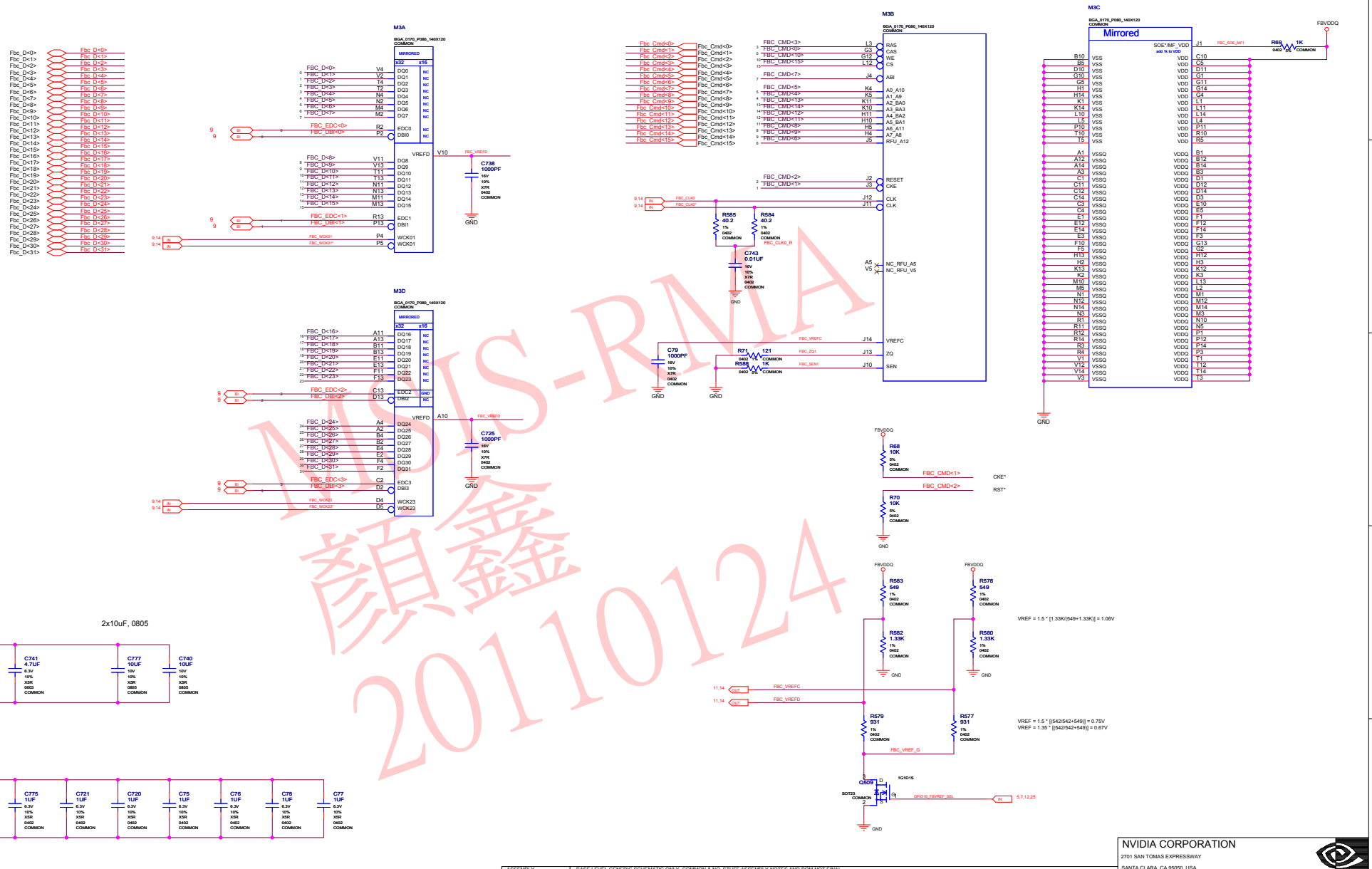
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GDDR5 CMD Mapping		
CMD	0..31	32..63
CM00	CAP	
CM01	CST	
CM02	RS*	
CM03	MAP	
CM04	AL_A0	
CM05	AL_A10	
CM06	AL_A20	
CM07	AB	
CM08	AL_A11	
CM09	AL_A8	
CM10	WE*	
CM11	AL_BA1	
CM12	AL_BA2	
CM13	AL_BA3	
CM14	AL_BA3	
CM15	CS*	
CM16		CAP*
CM17		CST*
CM18		RS*
CM19		MAP*
CM20		AL_A0
CM21		AL_A10
CM22		AL_A20
CM23		AB*
CM24		AL_A11
CM25		AL_A8
CM26		WE*
CM27		AL_BA1
CM28		AL_BA2
CM29		AL_BA3
CM30		AL_BA3
CM31		CS*

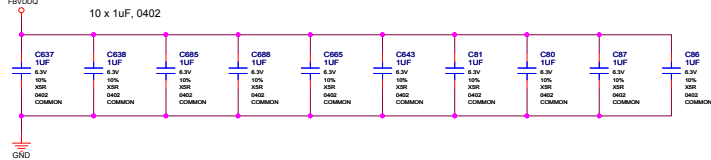
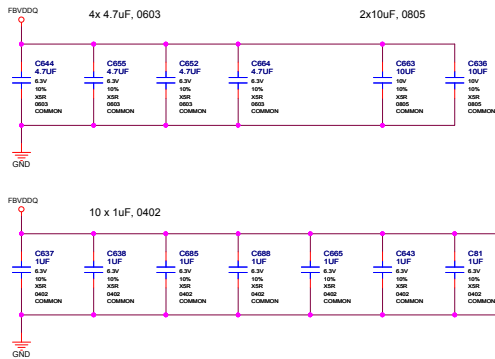
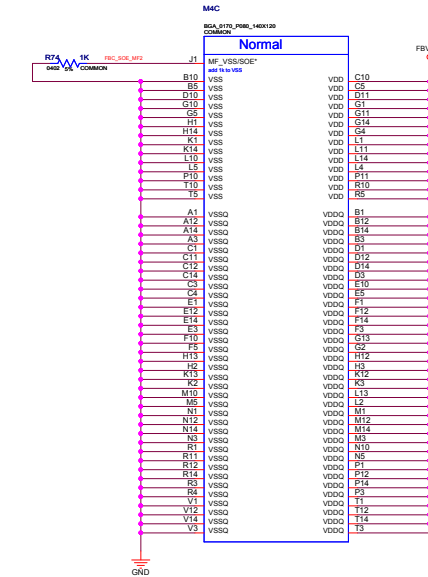
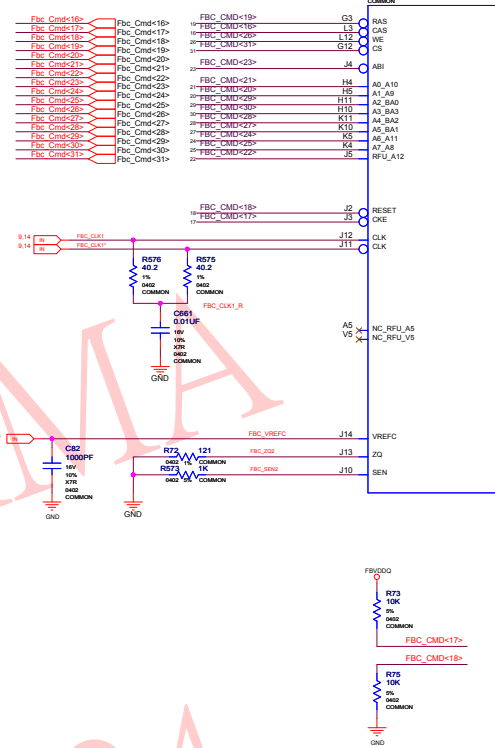
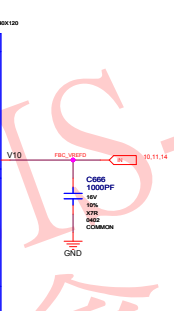
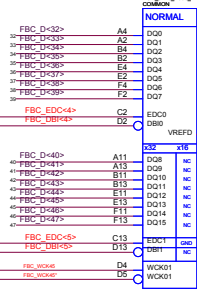
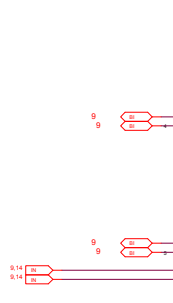
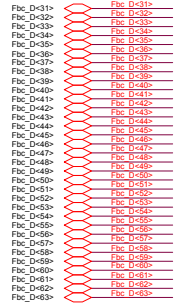
** Vref switching options:
external Vref should be POR for Vref0
potential for update



GDORS CMD Mapping

CMD	0..31	32..63
CMD0	CMD7	
CMD1	CMD8	
CMD2	RS7	
CMD3	RS0	
CMD4	AL_A0	
CMD5	AL_A10	
CMD6	AL_A10	
CMD7	AB7	
CMD8	AL_A11	
CMD9	AL_A8	
CMD10	AL_BA1	
CMD11	AL_BA2	
CMD12	AL_BA3	
CMD13	AL_BA3	
CMD14	AL_BA3	
CMD15	CS	
CMD16	CMD7	
CMD17	CMD7	
CMD18	RS7	
CMD19	RS0	
CMD20	AL_A0	
CMD21	AL_A10	
CMD22	AL_A10	
CMD23	AB7	
CMD24	AL_A11	
CMD25	AL_A8	
CMD26	AL_BA1	
CMD27	AL_BA2	
CMD28	AL_BA3	
CMD29	AL_BA3	
CMD30	AL_BA3	
CMD31	CS	

** Vref switching options:
- Internal Vref should be POR for VrefD
- potential for update



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC Partition 63..32

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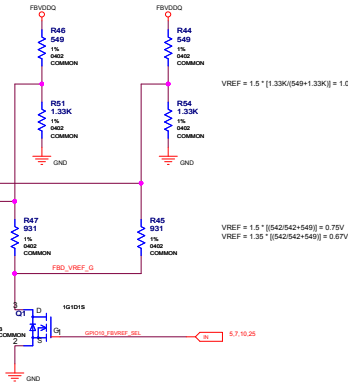
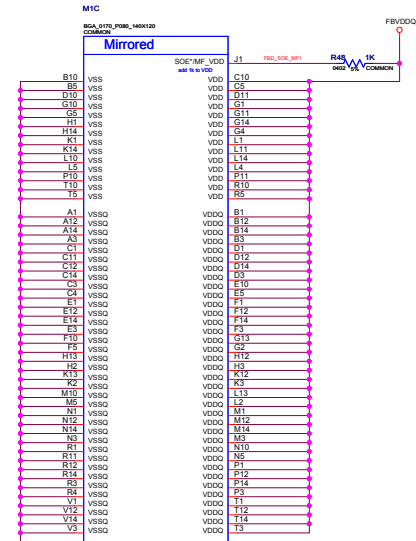



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- ** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update

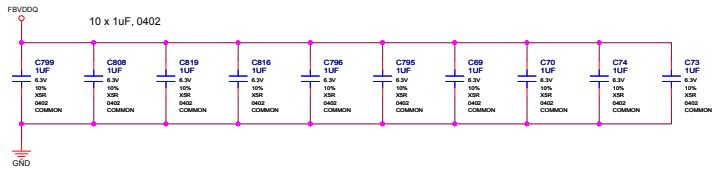
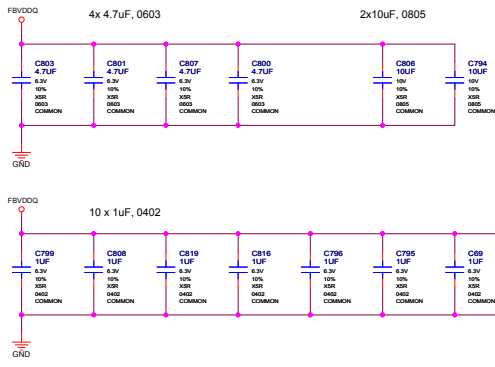
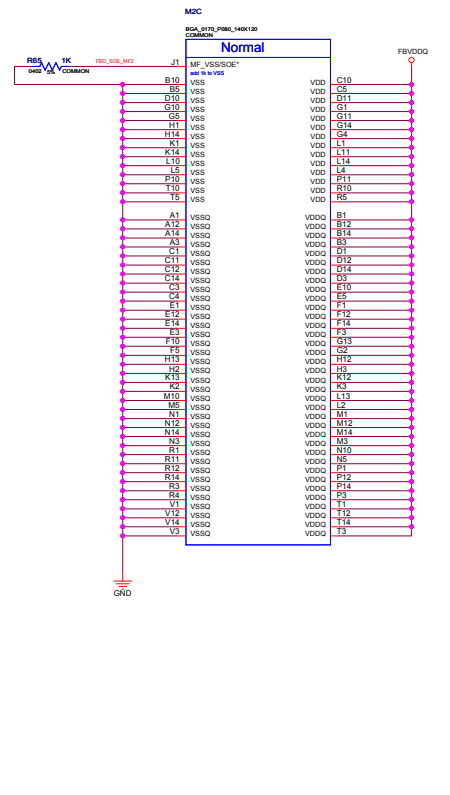
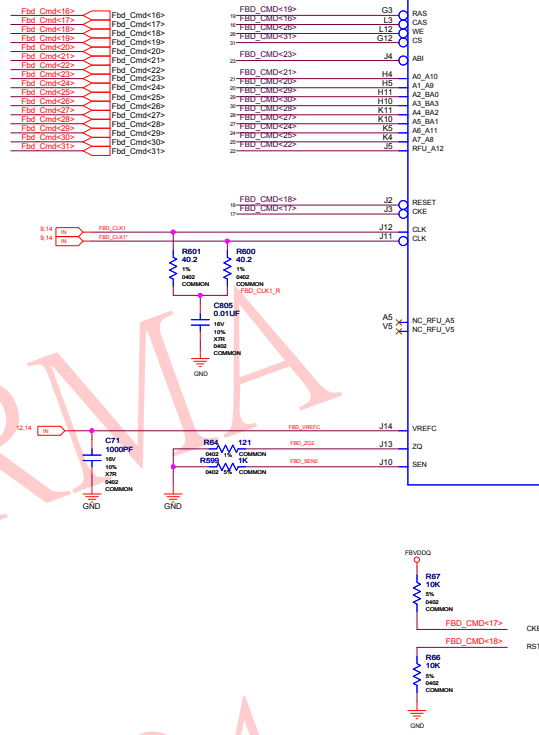
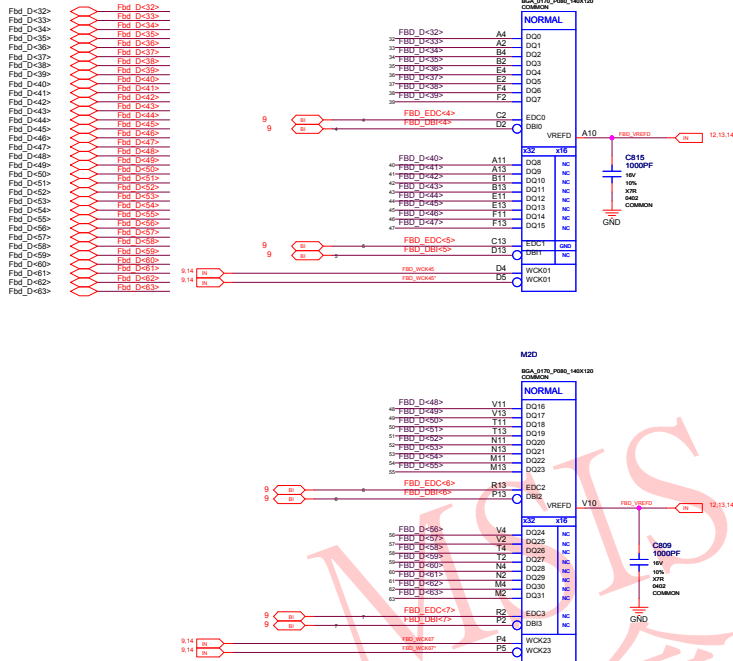


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GDORs CMD Mapping

GDOR	0..31	32..63
CM00	CAS*	
CM01	CAS*	
CM02	RST*	
CM03	RST*	
CM04	AL_A0	
CM05	AL_A10	
CM06	AL_A10	
CM07	AB*	
CM08	AL_A11	
CM09	AB*	
CM10	WE*	
CM11	AL_BA1	
CM12	AL_BA2	
CM13	AL_BA3	
CM14	AL_BA3	
CM15	CD*	
CM16	CD*	
CM17	CD*	
CM18	RST*	
CM19	RST*	
CM20	AL_A0	
CM21	AL_A10	
CM22	AL_A10	
CM23	AB*	
CM24	AL_A11	
CM25	AB*	
CM26	WE*	
CM27	AL_BA1	
CM28	AL_BA2	
CM29	AL_BA3	
CM30	AL_BA3	
CM31	CD*	

** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBD Partition 63..32


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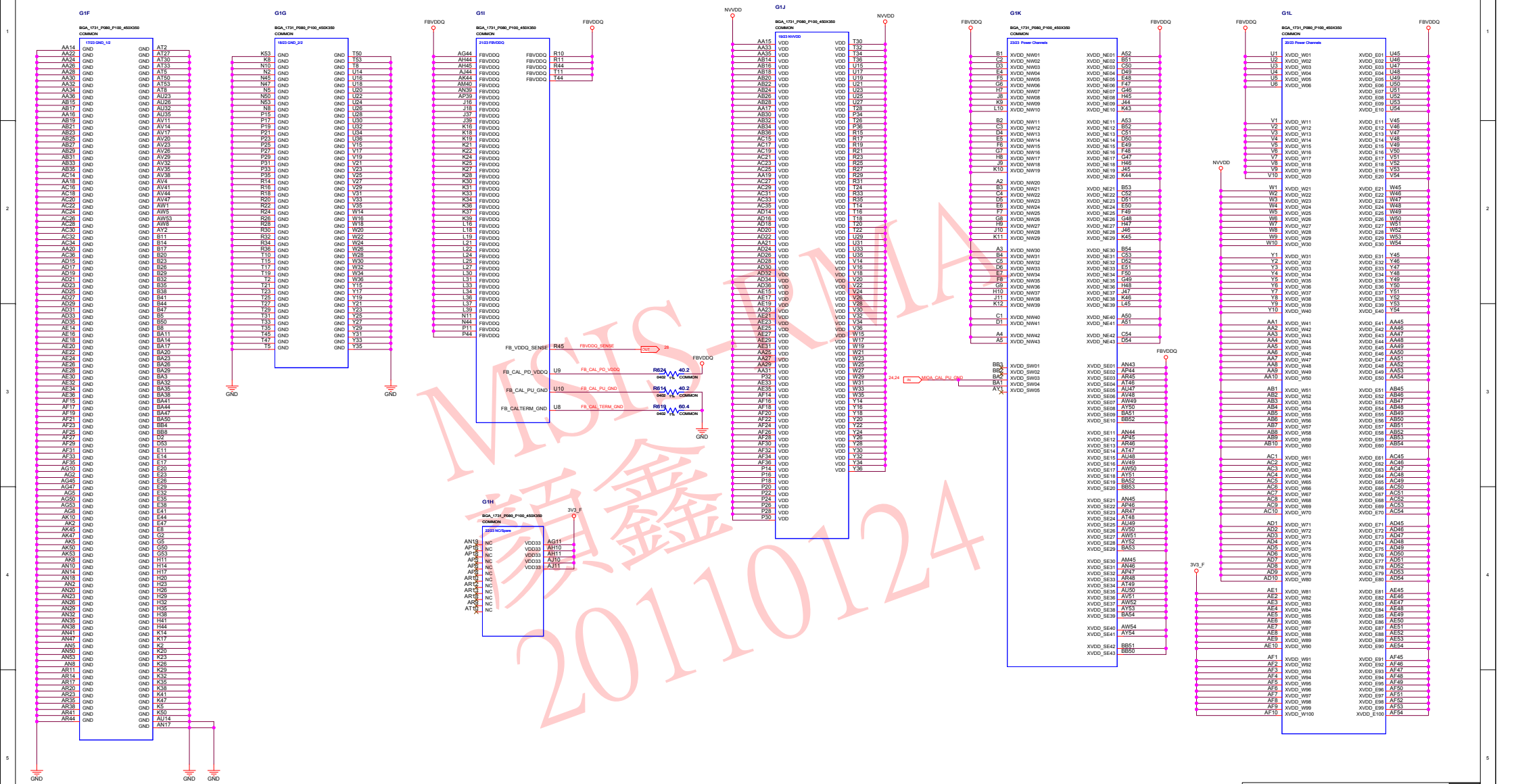
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PAGE DETAIL: FB Net Properties

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** Power channels are configurable.
XVDD_.* pins are not connected on the substrate.
Therefore, XVDD_.* pins can be assigned as needed.



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PAGE: DETAIL	GPU PWR and GND

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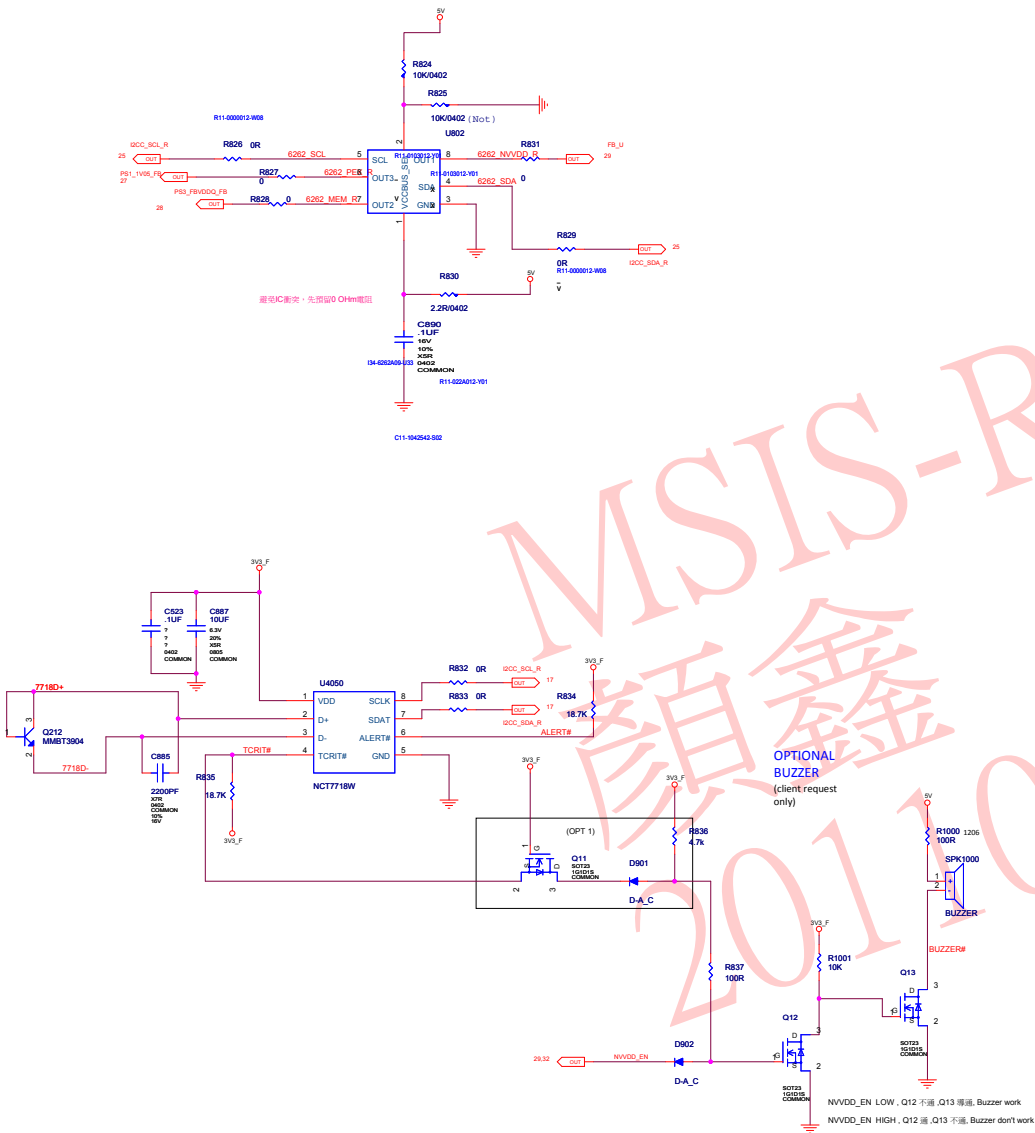
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BOM REV A

PAGE
DATE 12-MAY-2010

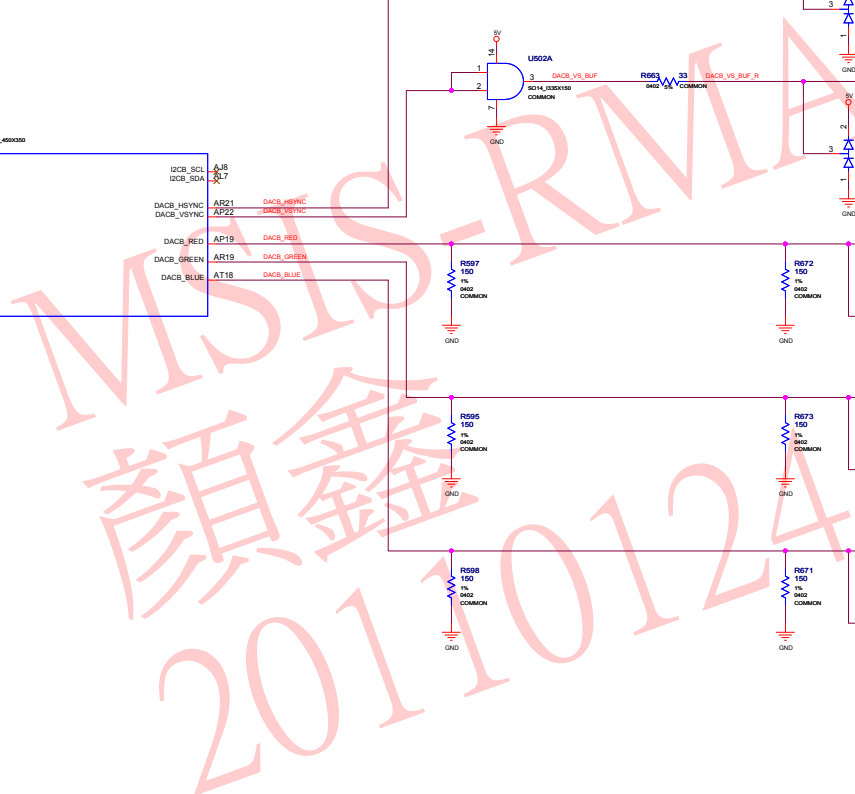
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PAGE DETAIL	GPU Decoupling



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NET	NV_CRITICAL	NV_IMPEDANCE
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19.21	IN	DACB HS DVI	2	500MB
19.21	IN	DACB VS DVI	2	500MB

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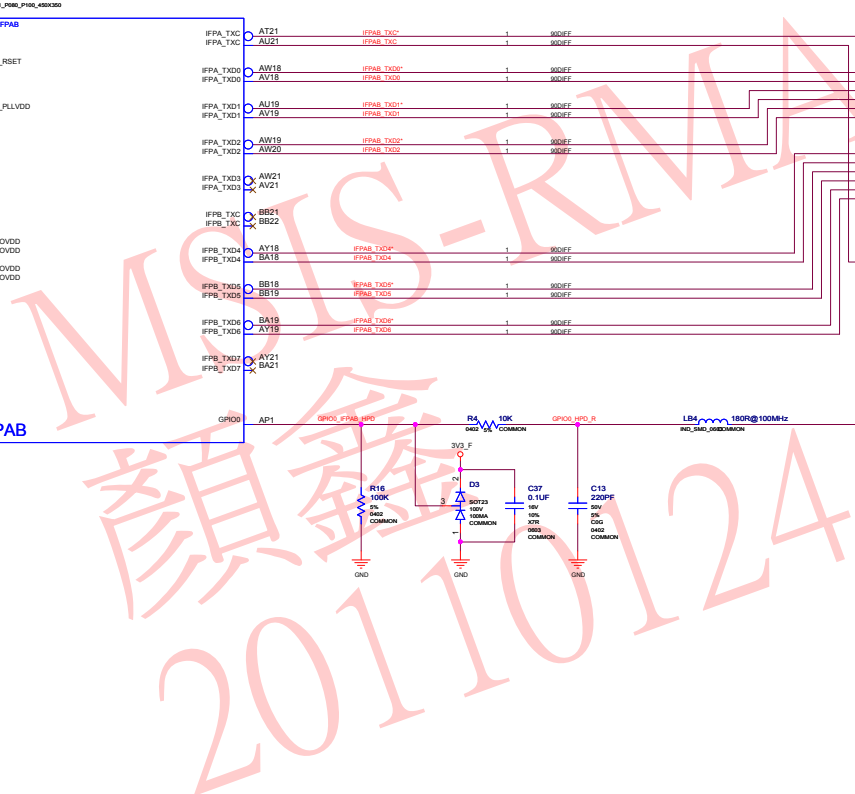
NV_PN	600-11041-BASE-000
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PCB REV	P1041-B01
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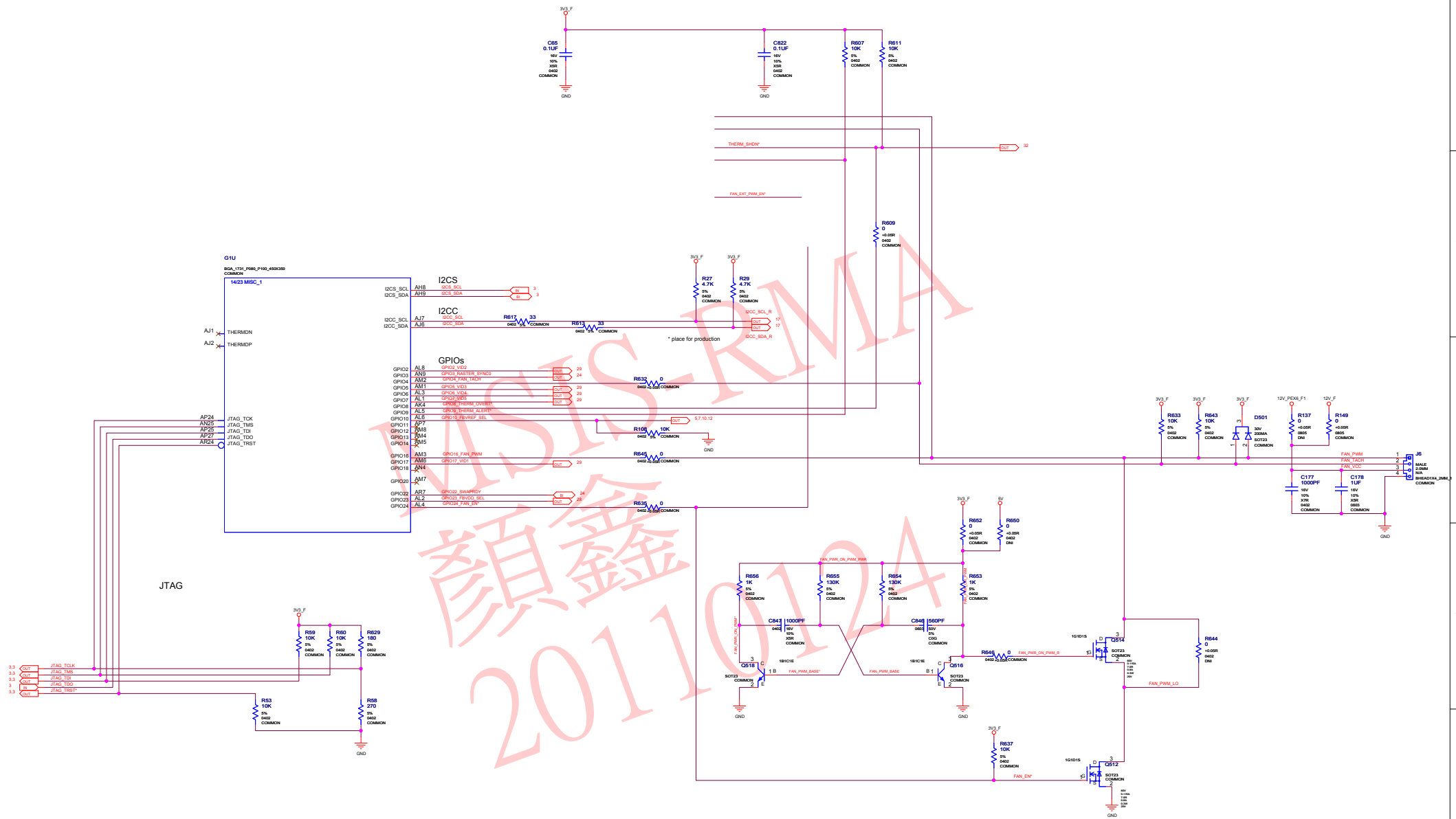
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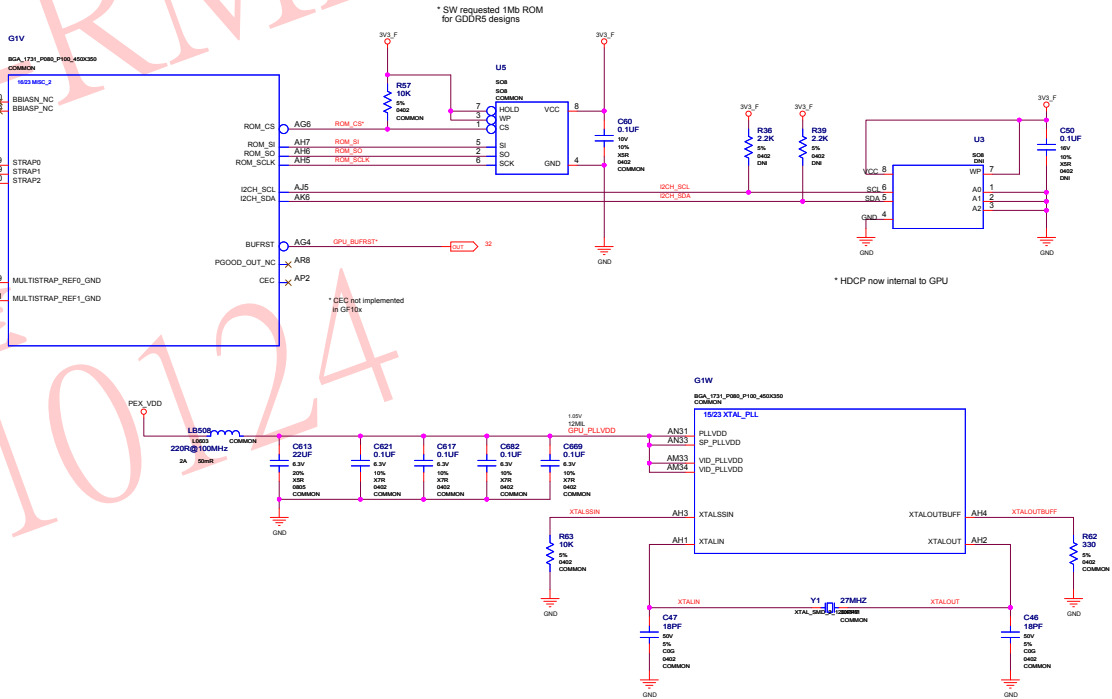





	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

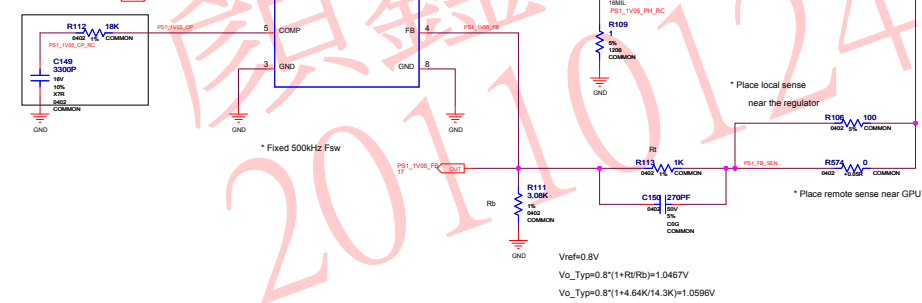
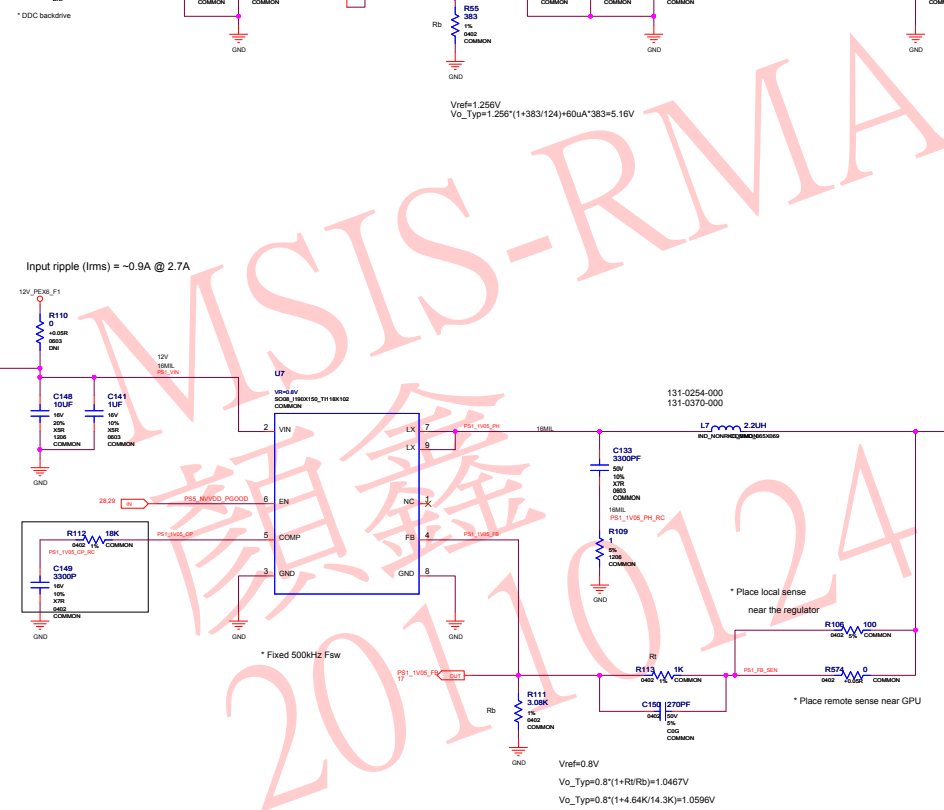
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0010	32Mx32	256-bit Hynix	
0011	32Mx32	256-bit Samsung	
0100	Reserved		
0101	64Mx32	256-bit Qimonda	
0110	64Mx32	256-bit Hynix	
0111	64Mx32	256-bit Samsung	
1000	Reserved		
1001	32Mx32	192-bit Qimonda	
1010	32Mx32	192-bit Hynix	
1011	32Mx32	192-bit Samsung	
1100	Reserved		
1101	64Mx32	192-bit Qimonda	
1110	64Mx32	192-bit Hynix	
1111	64Mx32	192-bit Samsung	

NET	NV_CRITICAL	NV_IMPEDANCE
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100	1	1




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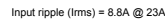
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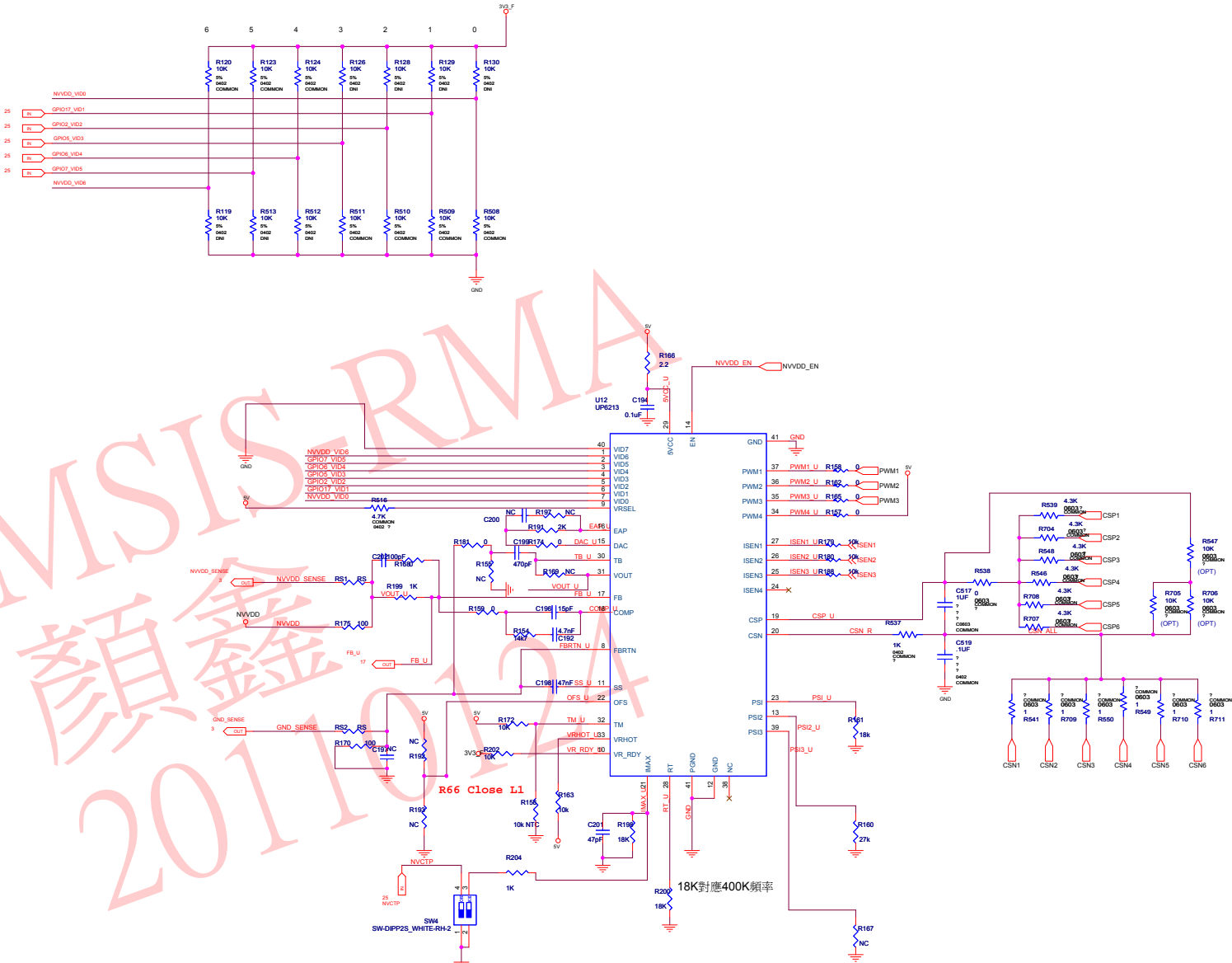


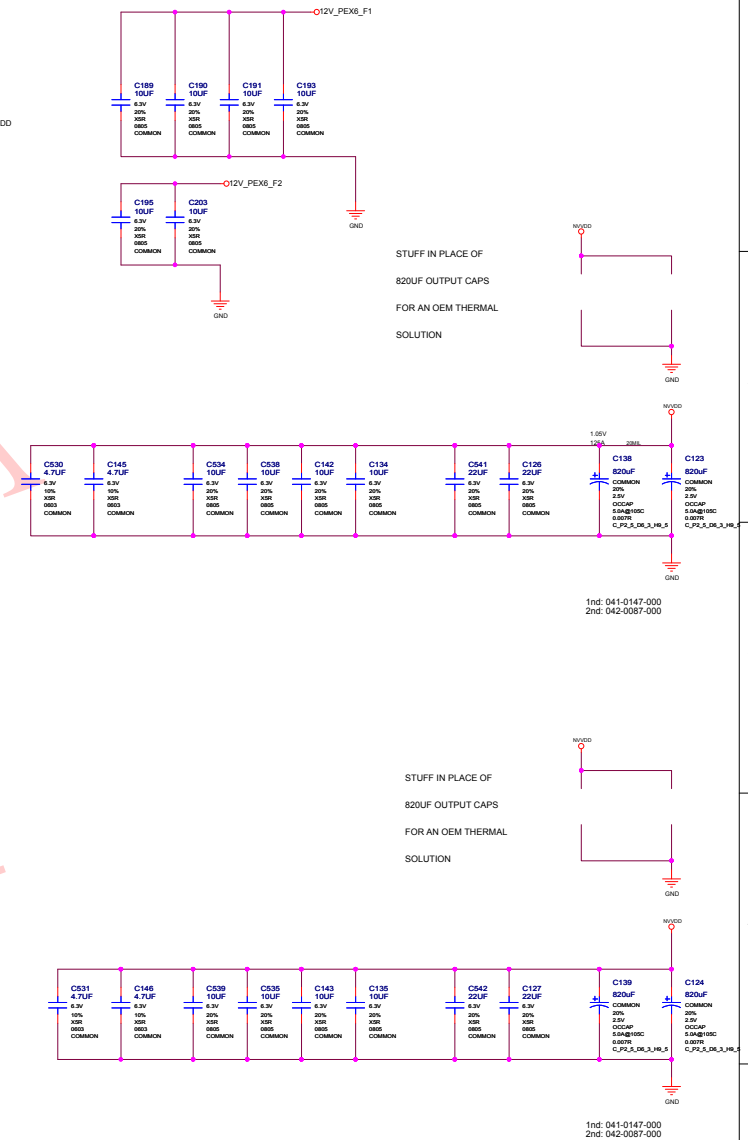
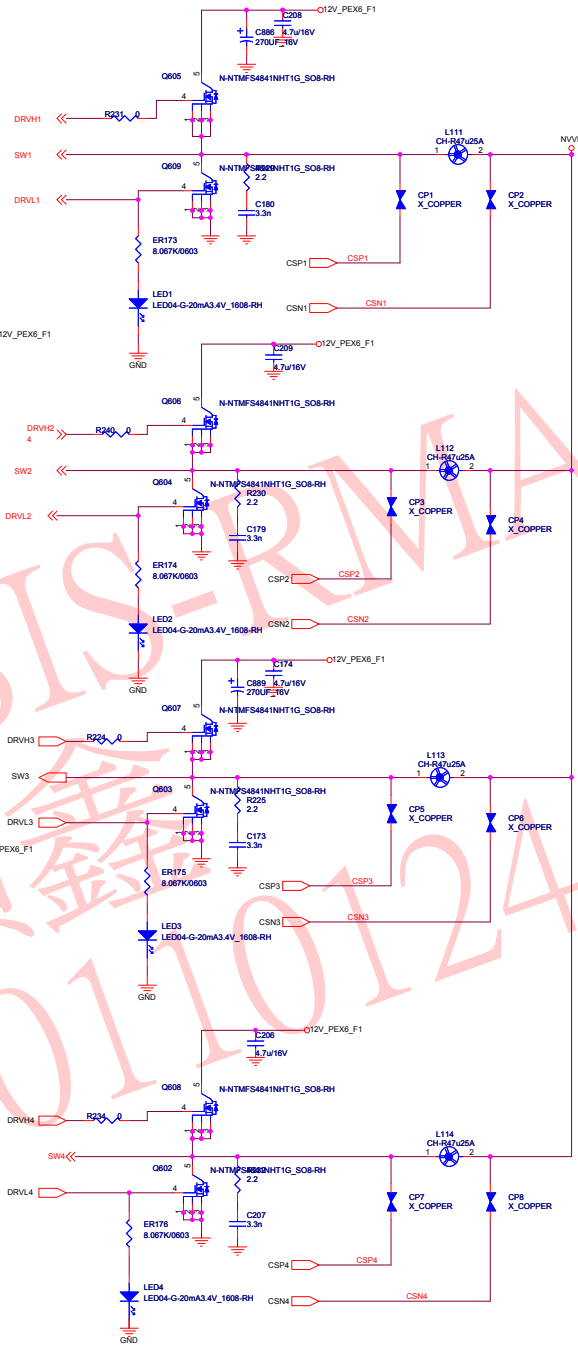
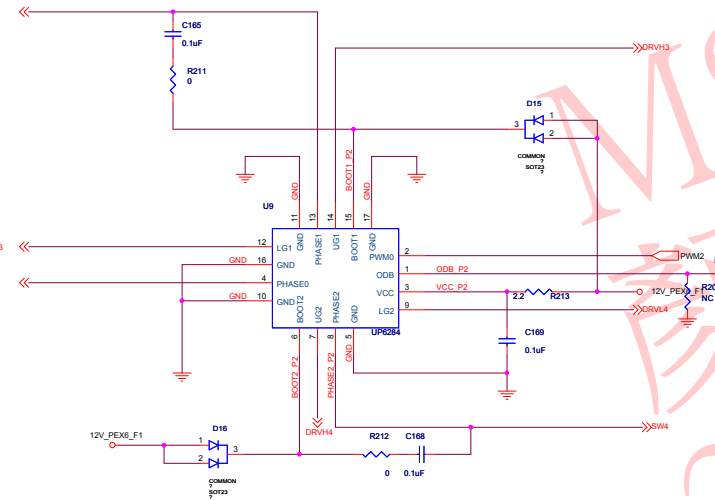
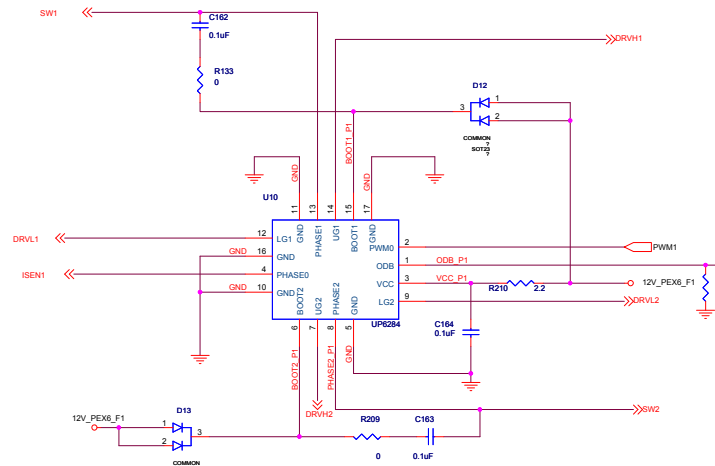
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1.5V	1

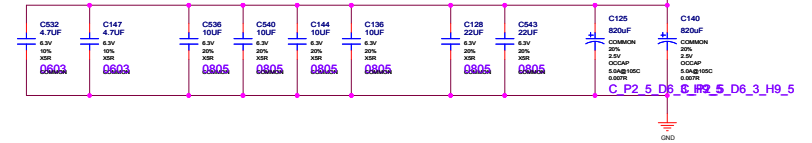
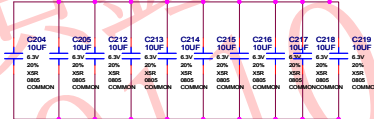
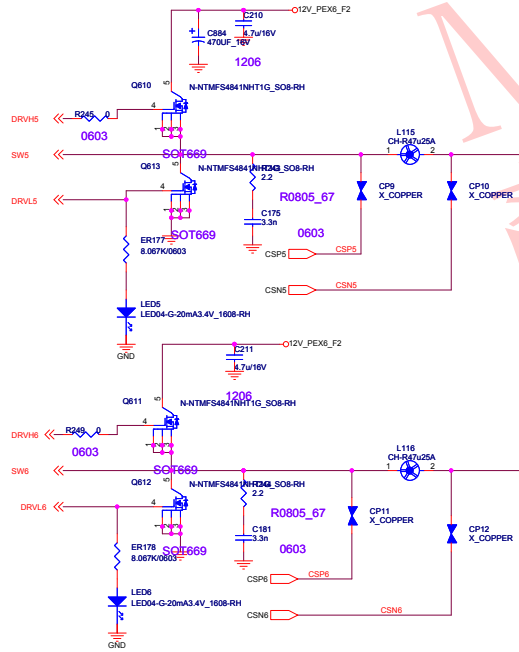
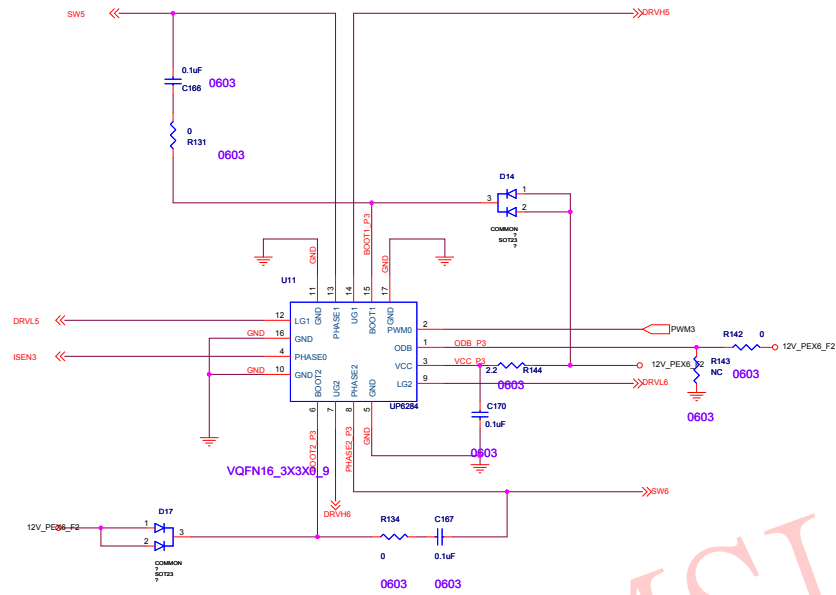
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VID Table					
GPIO7	GPIO6	GPIO5	GPIO2	GPIO17	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V







STUFF IN PLACE OF
820UF OUTPUT CAPS
FOR AN OEM THERMAL
SOLUTION

1nd: 041-0147-000
2nd: 042-0087-000



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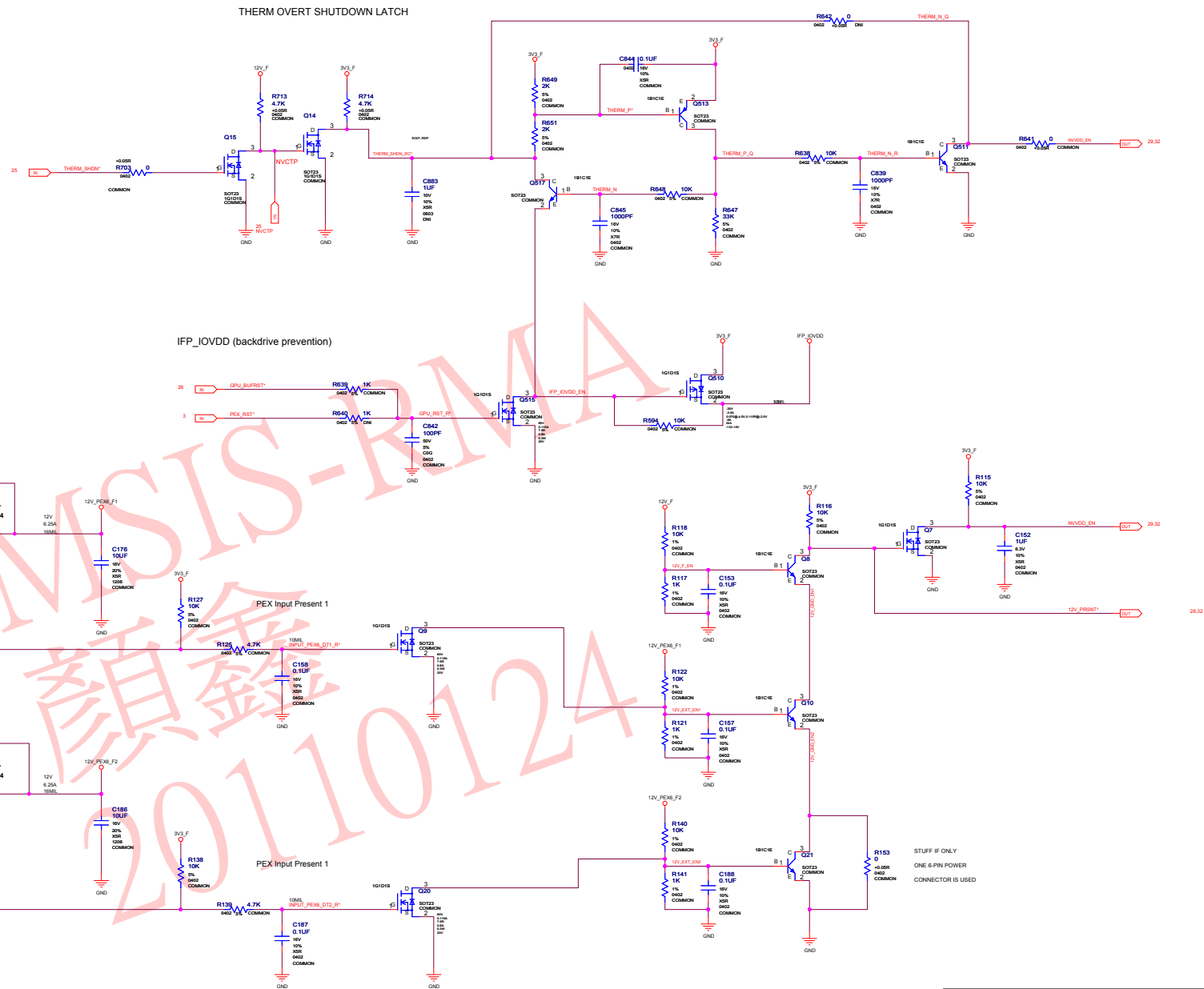
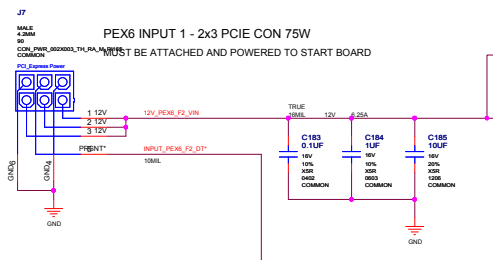
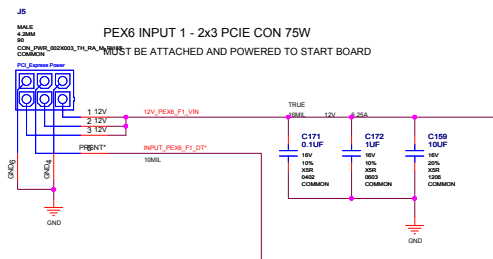
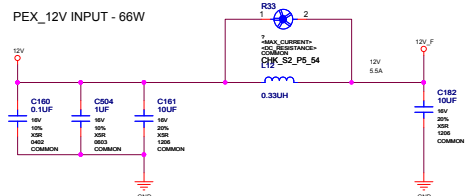
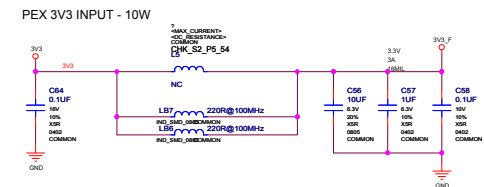
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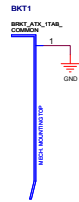
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STUFF IF ONLY
ONE 6-PIN POWER
CONNECTOR IS USED

Brackets:

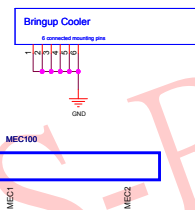
Bracket with DVI_DP_mHDMI : 151-10001-0355-071



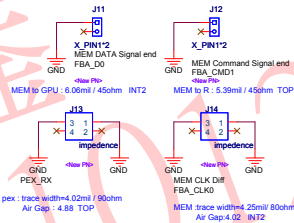
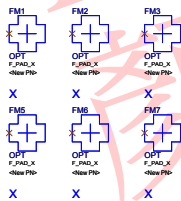
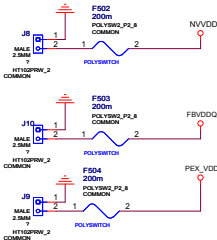
Bracket Screw



Cooler/GPU Stiffener



remove mec1



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PCB REV	P1041-B01	PAGE	
BOM REV	A	DATE	12-MAY-2010

