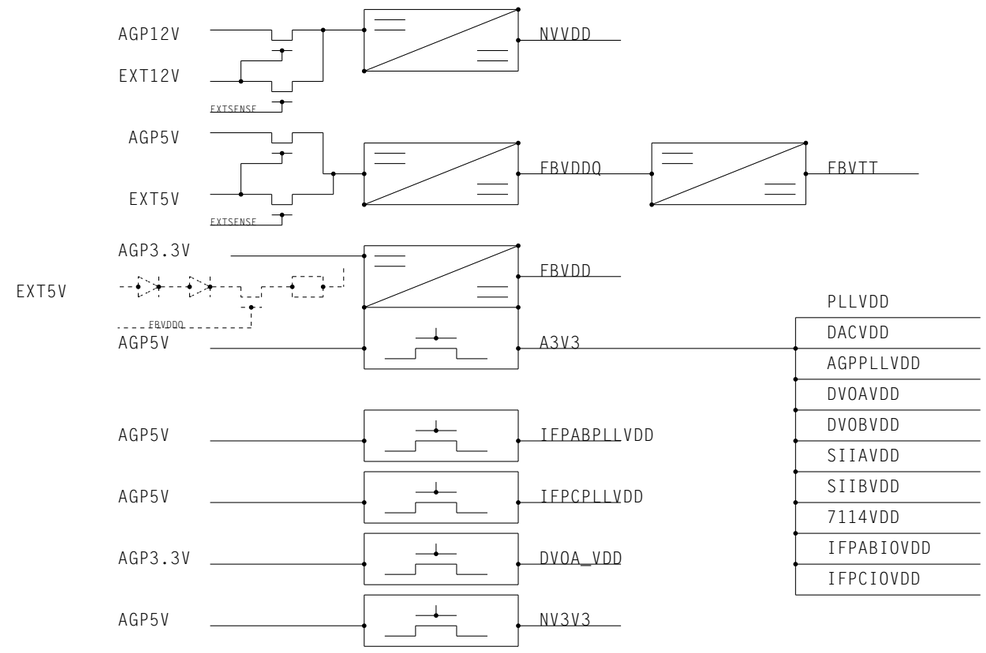
30P126 - NV30 Production Board

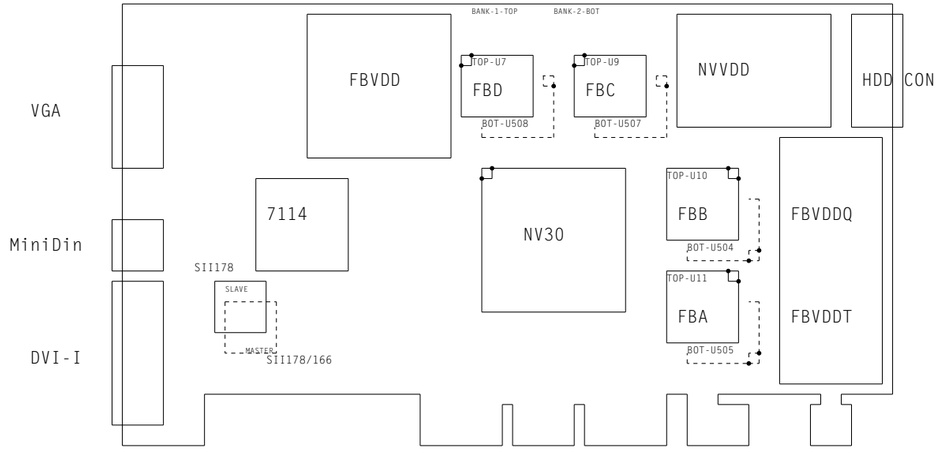
30P126_A05 - NV30 FC BGA, 128MB DDR2 (4Mx32), VGA, External TMDS(Dual-Link)

Internal TV,

Table of Contents:

Power Topology





Calibration Resistors

```
AGPCALPD_VDDQ   - 50 Ohm to AGPVDDQ (0.75v)
AGPCALPU_GND    - 50 Ohm to GND      (0.75v)
FB_CAL_PD_VDDQ  - 47.5 Ohm to FBVDDQ  (0.7v)
FB_CAL_PU_GND   - 47.5 Ohm to GND     (0.7v)
FB_CAL_CLK_GND  - 550 Ohm to GND    (1.2v)
FB_CAL_TERM_GND - 47.5 Ohm to GND     (0.7v) (or something close)
SAGPOCALPD_VDDQ - 50 Ohm to SAGPOVDDQ (0.75v)
SAGP1CALPD_VDDQ - 50 Ohm to SAGP1VDDQ (0.75v)
SAGPOCALPU_GND  - 50 Ohm to GND      (0.75v)
SAGP1CALPU_GND  - 50 Ohm to GND      (0.75v)
D1D2_CAL_PD_VDDQ- 50 Ohm to VDDQ
D1D2_CAL_PD_GND - 50 Ohm to GND
```

GPIO Assignments

GPIO	Type	Function
GPIO_0	IN	LOAD_TEST (Quickswitch)
GPIO_1	IN	Hot Plug/Unplug from DVI- Secondary -Bottom
GPIO_2	OUT	Fan PWM Control, LOW=FAN off, HIGH=FAN on
GPIO_3	OUT	Select NVVDD VSEL2
GPIO_4		Reserved
GPIO_5	OUT	Select NVVDD VSEL0
GPIO_6	OUT	Select NVVDD VSEL1
GPIO_7	OUT	SEL_2ND_DEV (Quickswitch)
GPIO_8	IN	GPU_SLOW_MODE#(THERM_ALERT# & EXTSENSE)
GPIO_9	IN	Reserved

FAN will RUN when GPIO_2 is tristated.

Connector I2C Assignments

Display Connector	NV30 Output	I2C Channel
VGA	DAC A	A
DVI-I (south)	DAC B+DVO A	B
DIN	DAC B	C

* * * NOTE:* * *

SKU SCH 602-10126-0003-005

SCH Ver:13

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

DETAIL	DRAWING DETAIL CONTINUED...		
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History:P126-A00

PLEASE REFER PREVIOUS VERSION SCHEMATICS(A04)

History:P126-A01

X01 10/08/02
1. Add pullup and pulldn for Master Sii178 to support Sii164/166 in the same location
2. Dual Mode Strap on Slave SII187 was tied to SIIA_AVCC(3.3V). now connected to SIIA_VCC(3.3V)

X02 10/09/02
1. Change AGP CAL PU/DN is changed from 56ohm to 50ohm prallel combination.

X03 10/10/02
1. Stuff AGVREFCG circuit and Change R594 from Nostuff 121K to stuff 158 K.Vref=350mV

X04 10/12/02
1. FBVTT cap values as per SI- C728, C729, C730, C731 from 1000pF to 2.2nF
   C749, C773, C597, C585, C560, C521. 0.01uF(10nF) to 0.022uF(22nF)
2. Add more clarity to block diagram.

History:P126-A02

X00 10/14/02
- Created New project from A01. Add min PCICLK length Constraint.

X01 10/15/02
1. Update netnames for E-Tools

X02 10/20/02
- Change TMDS Termination from No-Stuff to Stuff (NVPN 195-23000-0003-000)
- C87 - 1UF 0805 Cap on 12V AGP from 036-30105-0076-000 to 036-30105-0057-000

X03 10/24/02
1.Replaced varoious not for new design parts(147 error)
2.Connect un used PG chip input to 3.3V rail as per Intersil recomendation
- Add 12V pull up and pull down as per Intersil on power good chip o/p. To be used when no PG chip.
- Add series termination res to FRWR interface.

X04 10/25/02
1.Add anAdjustable LDO for DVOA_VDD rail to provide 3.0V from AGP3.3V rail
2.Add a decap for FB_CAL_CLK_GND, FB clock Bias pin.
3.Change R31 to 1K from 6.8K, R753 to 3.3K from 10K so the EXT_SENSE signal falls low quickly(< 650uS).
4.Add more notes for EXTSENSE and GPU_SLOW_MODE signals usuage for s/w.

X05 10/26/02
1.Change FB Vref voltage divider from using 120R to 1K.

X06 10/28/02
1.C658 was No stuff, change it to stuff, it is not under Heat sink.
2.Update Remote sense cap assy as per layout and bom.

History:P126-A03

X01 10/30/02
1.Change C737, C738, C783, C784 to 0603 from 0402
2. PCB A02 was not gerbered correct, corrected PCB is A03. Rolling SCH for A04

History:P126-A04

X00 11/04/02
1.Change U506 to 0.5% part

X01 11/05/02
1.Change NVVDD compensation to R608,R589,C598 to No stuff, C604 =0.1uF, R573 = 39K.
2.NVVDD, FBVDD Inductor of 3mohm type from 6mohm type.
3.Cange FAN circuit CAPs to 0805 from 0603.

X02 11/07/02
1.Do changes for Barry III, FBCAL-357ohm,Add 1pF cap for FBVREF.
2.No stuff CLK_Bias cap. DANGER.

X03 11/08/02
1. Add a diode in parallel to Q507, Cahnge R536, FBVDDQ OCset to 56.1k from 95.K

X04 11/12/02
1. IFPRSET changed from 1K to 1.5K.
2. CLK term at Memory cahnged to 226R,Zq for 128MB is 182R, 64MB is 90.9R, DAC Rest is 68R
3. FBVVDQ lower FET is chagned to higher current version.
4. FB I/O CAL is 20R, CLK Term is 40R, CLK CAL is 549R for 226ohm surce term, 357ohm for 100ohm CLK source term
5. DVOA Reg Rtop-976ohm, Rbot 698R for standard values instead of 180R 5% and 137R 5%

X05 11/21/02
1. Change Q511, for Idmax from 12A to 18A @ 25degC.

History:P126-A05

X00 11/22/02
1. Add pull down to TSTMODE_pin, Add pull up to 6225-0deg Phase, Replace FBVDD fets to 20V Vgs from 12 VGs
2. Remove cap for FB_CAL_CLK_GND, ADD cap for FBVREF to FBVDDQ, Add one more 1200uF CAP for FBVDD
3. ISL6569 and FET drivers on same power node, EXTSENSE moved to EXT_5V, Add EZ1117 Reg for GPU 3v3

X01 11/25/02
1. Remmove Firewire section. Change R804(10K) from 5% to 1%, R805 from 1.5K to 1.4K 1%. See notes.

X02 11/26/02
1. Remmove TAB bracket, Replace SlimVGA w/ standard VGA, Add pull down to hot plug ckt,
2. Move FBVDDQ to EXT_5V from EXT_12V. Add gating FETs instead of Diodes. Remove FRWRVDD, Inductor, 2caps
3. For NVVDD PS EXT_12V is through a gating FET instead of Diode/No diode.
4. Add discrete logic AND for EXTSENSE using Ext12V and Ext5V.
5. Remove Supplemental power connection resistors to FBVDD rail, No CGND2
6. Swapped LOAD_TEST, GPIO3_VSEL2 nets to GPU.
7. Set Higher threshold to disconnect AGP rails when EXT rail is used by using Voltage divider

X03 11/30/02
1. Move DVI_HPD pull down before series resitor, otherwise it was forming a voltage divider..
2. Delete Firewire enable strap(pull up)..
3. Add Placement note for signal: 3V3_6529 to be 330mOhm, it is already 330mohm..
4. Delete 8 nos, 0805 res on signal FB_3.3V - Suppemetal power ckt.
5. Add Zener threshold detector for 12V ext detect
6. Enable AGP-Rail FETs directly by EXT_Rails. Body diode helps Rail transistions

X04 12/02/02
1. C830 and C834 can not be connected to NV3V3, move to 3v3 as it was.

X05 12/03/02
1. Move following from 3V3 to A3V3 for layout: R55, R56, U12, C265, R720, R719, R678.
2. Move following from 3V3 to NV3V3 for layout: R608, R604, R605, R606.
3. Change FBVDDQ PS input cap from 80mm to 100mm cap with > 4.0A ripple current

X06 12/04/02
1. Update:Block diagram, Power topology, GPIO table, descriptions as per A05 baord
2. R702 changed to A3V3 from 3V3
3. The following changed from 3V3 to NV3V5: U8-D1D2 power pins, C701, R601, Q514
4. New NET AGP_12V_OFF and 0402 cap and a resistor.
5. New NET AGP_5V_OFF and 0402 cap and a resistor.

X07 12/05/02
-. Add GPIO control using FET, each fet controls only 3 VID pins

X08 12/05/02
1. R795, R796 changed to 0402 from 0603.Added a cap to CGND to STEREO_5V_C
2. Update BRKT1

X09 12/06/02
1. Updated GPIO Pages

X10 12/08/02
1. Resequenced RefDes

X10 12/09/02
1. Adjusted Resistor Values for External Sense Circuit
2. Changed Upper FET of 6225 to IRF7822
3. Removed 3 Resistors to bridge NV_S to 3V3_6529 (not required after removing option to strap power to 3V3)

X11 12/27/02
1. FAN circuit-Upper Cap changed to 0.01uF from 1uF, Lower caps No stuff, update variant for bracket.

X12 12/30/02 to 01/14/03
1. NVVDD Risen changed from 2.2K(13.5A/phase) to 2.32K 1%(13.8A/Phase) for better availability
2. Update DAC Rsets,Terminations. Update NVVDD default 1.2V, FBVDDQ=2.5V, MemCalib&Terms.
3. Update 470uF/16V,0.01uf/10V, 100pF/16V, Update Vairant as per latest BOM.

X12a 30/1/03
1. Add MEC5 extra screw for Fxflow bracket to keep 2nd slot open for air vent

X13 02/14/03
Add following items to SingleLink DVI BOM.
1. C905,C932,C939,C940- 4.7UF/0805
2. C906, C911,C912, C928, C934, C936, C937 - 100PF/0603
3. C907, C930, C933, C935, C938 - 036-20104-0056-000 -0.1UF/0603

FOR 128MB sku

NVVDD:0.8 to 1.5V Default 1.2V
NV3V3:3.5V
FBVDD:2.6V
FBVDDQ:2.5V
FBVTT:0.5*FBVDDQ
GPU Vref:0.5*FBVDDQ
MEM Vref:1.08V
CS Delay:5pF +/-0.25pF has 4.7pF as alternate.
Zq:200R 1%
CLK TermMEMory: 200R 1%
FB_CL_TERM_GND(R620): 47.5R 1%
FB_CAL_CLK(R628): 549R 1%
FB_CAL_PU/PD(R621/623):47.5 1%.

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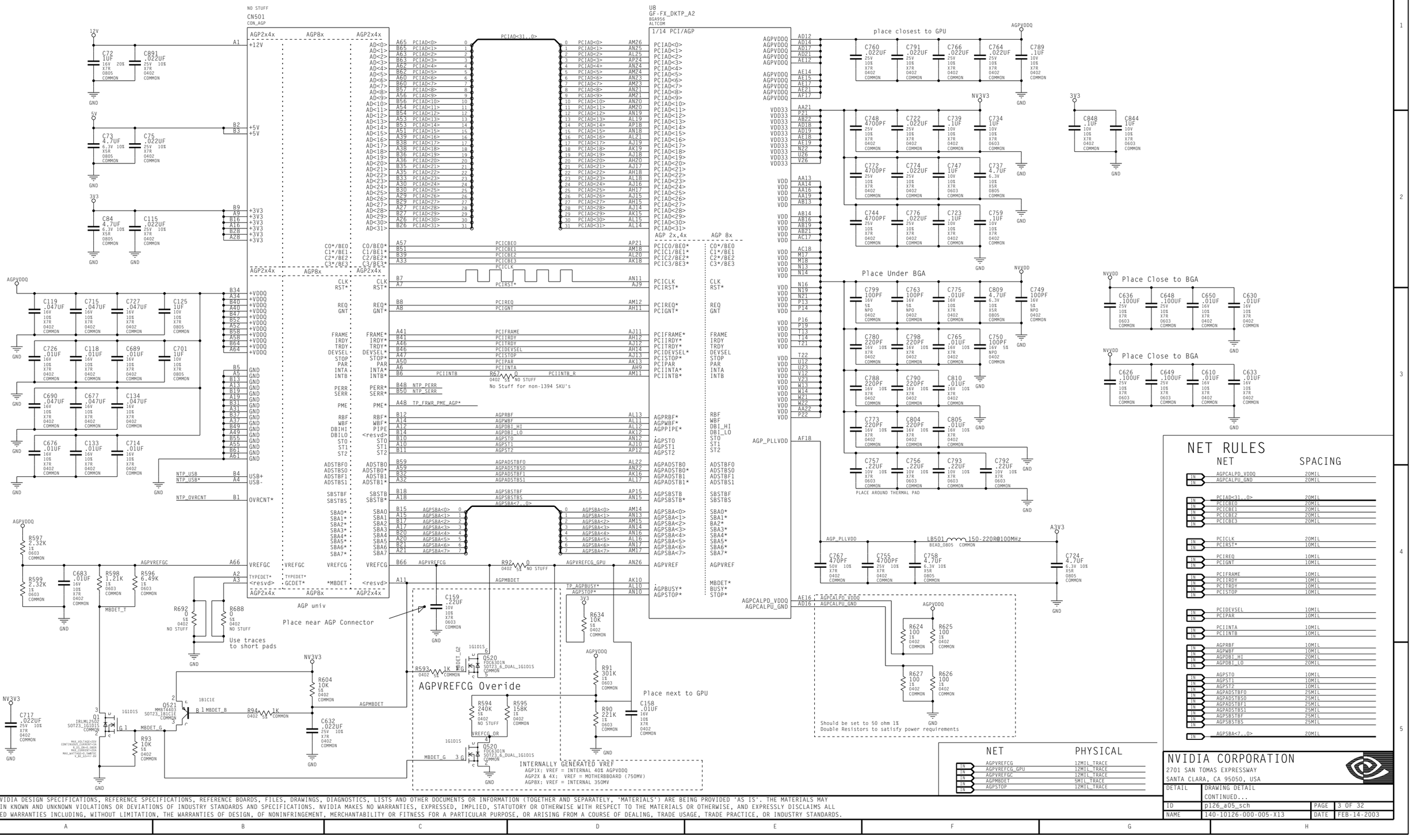
1.a. AGP 8X Interface



NET RULES

NET	SPACING
AGPCALPD_VDDQ	20MIL
AGPCALPU_GND	20MIL
PCIAD<31..0>	20MIL
PCICBE0	20MIL
PCICBE1	20MIL
PCICBE2	20MIL
PCICBE3	20MIL
PCICLK	20MIL
PCIRST*	10MIL
PCIREQ	10MIL
PCIGNT	10MIL
PCIFRAME	10MIL
PCIIRDY	10MIL
PCITRDY	10MIL
PCISTOP	10MIL
PCIDEVSEL	10MIL
PCIPAR	10MIL
PCIINTA	10MIL
PCIINTB	10MIL
AGPRBF	10MIL
AGPWBF	10MIL
AGPDBI_HI	20MIL
AGPDBI_LO	20MIL
AGPSTO	10MIL
AGPST1	10MIL
AGPST2	10MIL
AGPADSTBF0	25MIL
AGPADSTBS0	25MIL
AGPADSTBF1	25MIL
AGPADSTBS1	25MIL
AGPSBSTBF	25MIL
AGPSBSTBS	25MIL
AGPSBA<7..0>	20MIL

NET	PHYSICAL
AGPVREFCG	12MIL_TRACE
AGPVREFCG_GPU	12MIL_TRACE
AGPVREFGC	12MIL_TRACE
AGPMBDET	5MIL_TRACE
AGPSTOP	12MIL_TRACE

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2.a. Memory

U8
GF-FX_DKTP_A2
BGA956
ALTCOM
2/14 MEM_A_B

FBVDDQ

K24 K26 L15 L25 M25 P25 T25 U25 V25 W25

FBVDDQ

AA25 J25 J26 K11 K12 K14 K17 K18 K21 K23

Place near BGA

C731 4700PF 25V 10% X7R 0402 COMMON
C733 .022UF 25V 10% X7R 0402 COMMON
C603 .1UF 10V 10% X7R 0402 COMMON
C846 .1UF 10V 10% X7R 0402 COMMON
C786 4700PF 25V 10% X7R 0402 COMMON
C761 .022UF 25V 10% X7R 0402 COMMON
C615 .1UF 10V 10% X7R 0402 COMMON
C729 .1UF 10V 10% X7R 0402 COMMON
C732 4700PF 25V 10% X7R 0402 COMMON
C855 .022UF 25V 10% X7R 0402 COMMON
C870 .1UF 10V 10% X7R 0402 COMMON
C800 .1UF 10V 10% X7R 0402 COMMON
C651 4700PF 25V 10% X7R 0402 COMMON
C730 .022UF 25V 10% X7R 0402 COMMON
C666 .1UF 10V 10% X7R 0402 COMMON
C667 .1UF 10V 10% X7R 0402 COMMON
C728 1UF 10V 10% X7R 0603 COMMON
C692 1UF 10V 10% X7R 0603 COMMON
C696 1UF 10V 10% X7R 0603 COMMON
C738 4.7UF 6.3V 10% X5R 0805 COMMON

GND

7<> 5<> 4<> B1 FBAD<31..0>

0 FBAD<0>	T33	FBAD<0>
1 FBAD<1>	T31	FBAD<1>
2 FBAD<2>	U34	FBAD<2>
3 FBAD<3>	U33	FBAD<3>
4 FBAD<4>	W33	FBAD<4>
5 FBAD<5>	W31	FBAD<5>
6 FBAD<6>	Y34	FBAD<6>
7 FBAD<7>	Y33	FBAD<7>
8 FBAD<8>	T30	FBAD<8>
9 FBAD<9>	T29	FBAD<9>
10 FBAD<10>	R28	FBAD<10>
11 FBAD<11>	U29	FBAD<11>
12 FBAD<12>	U31	FBAD<12>
13 FBAD<13>	V31	FBAD<13>
14 FBAD<14>	W30	FBAD<14>
15 FBAD<15>	V28	FBAD<15>
16 FBAD<16>	AC31	FBAD<16>
17 FBAD<17>	AE30	FBAD<17>
18 FBAD<18>	AD31	FBAD<18>
19 FBAD<19>	AE29	FBAD<19>
20 FBAD<20>	AG28	FBAD<20>
21 FBAD<21>	AF31	FBAD<21>
22 FBAD<22>	AF30	FBAD<22>
23 FBAD<23>	AG31	FBAD<23>
24 FBAD<24>	AF34	FBAD<24>
25 FBAD<25>	AF33	FBAD<25>
26 FBAD<26>	AF32	FBAD<26>
27 FBAD<27>	AG33	FBAD<27>
28 FBAD<28>	AJ34	FBAD<28>
29 FBAD<29>	AJ33	FBAD<29>
30 FBAD<30>	AJ32	FBAD<30>
31 FBAD<31>	AK33	FBAD<31>

FBBD<31..0> B1 4<> 5<> 7<>

B31 FBBD<0>	0	FBBD<0>
A32 FBBD<1>	1	FBBD<1>
B32 FBBD<2>	2	FBBD<2>
A33 FBBD<3>	3	FBBD<3>
D33 FBBD<4>	4	FBBD<4>
E34 FBBD<5>	5	FBBD<5>
E33 FBBD<6>	6	FBBD<6>
E32 FBBD<7>	7	FBBD<7>
C31 FBBD<8>	8	FBBD<8>
D30 FBBD<9>	9	FBBD<9>
C32 FBBD<10>	10	FBBD<10>
E30 FBBD<11>	11	FBBD<11>
E29 FBBD<12>	12	FBBD<12>
F28 FBBD<13>	13	FBBD<13>
F29 FBBD<14>	14	FBBD<14>
G30 FBBD<15>	15	FBBD<15>
L31 FBBD<16>	16	FBBD<16>
M31 FBBD<17>	17	FBBD<17>
N30 FBBD<18>	18	FBBD<18>
N29 FBBD<19>	19	FBBD<19>
R29 FBBD<20>	20	FBBD<20>
P30 FBBD<21>	21	FBBD<21>
P31 FBBD<22>	22	FBBD<22>
R31 FBBD<23>	23	FBBD<23>
L33 FBBD<24>	24	FBBD<24>
L32 FBBD<25>	25	FBBD<25>
M33 FBBD<26>	26	FBBD<26>
M32 FBBD<27>	27	FBBD<27>
N31 FBBD<28>	28	FBBD<28>
P32 FBBD<29>	29	FBBD<29>
R33 FBBD<30>	30	FBBD<30>
R32 FBBD<31>	31	FBBD<31>

OUT FBAA<12..0> 4<> 5<> 7<>

0 FBAA<0>	AB30	FBAA<0>
1 FBAA<1>	AA28	FBAA<1>
2 FBAA<2>	AC29	FBAA<2>
3 FBAA<3>	AB29	FBAA<3>
4 FBAA<4>	Y31	FBAA<4>
5 FBAA<5>	AA29	FBAA<5>
6 FBAA<6>	Y30	FBAA<6>
7 FBAA<7>	AA31	FBAA<7>
8 FBAA<8>	Y32	FBAA<8>
9 FBAA<9>	AA33	FBAA<9>
10 FBAA<10>	AE31	FBAA<10>
11 FBAA<11>	AC28	FBAA<11>
12 FBAA<12>	AC32	FBAA<12>
TP_FBAA13	Y28	FBAA<13>

FBABA0 AE33 FBABANK<0>
FBABA1 AA32 FBABANK<1>

FBBA<12..0> OUT 4<> 5<> 7<>

K30 FBBA<0>	0	FBBA<0>
J28 FBBA<1>	1	FBBA<1>
L29 FBBA<2>	2	FBBA<2>
K29 FBBA<3>	3	FBBA<3>
H31 FBBA<4>	4	FBBA<4>
J29 FBBA<5>	5	FBBA<5>
H30 FBBA<6>	6	FBBA<6>
J31 FBBA<7>	7	FBBA<7>
F33 FBBA<8>	8	FBBA<8>
F32 FBBA<9>	9	FBBA<9>
L34 FBBA<10>	10	FBBA<10>
L28 FBBA<11>	11	FBBA<11>
J33 FBBA<12>	12	FBBA<12>
H28 TP_FBBA13		

K31 FBBBA0 4<> 5<> 7<> FBBBANK<0>
G33 FBBBA1 4<> 5<> 7<> FBBBANK<1>

FBCAS* AD33 FBBCAS* 4<> 5<> 7<>
FBWE* AB33 FBBWE* 4<> 5<> 7<>
FBCS0* AC33 FBBCS0* 4<> 5<> 7<>
FBCS1* AC34 FBBCS1* 4<> 5<> 7<>

FBCLK0 W29 FBBCLK0 4<> 5<> 7<>
FBCLK0* Y29 FBBCLK0* 4<> 5<> 7<>
FBCLK1 AC30 FBBCLK1 4<> 5<> 7<>
FBCLK1* AD29 FBBCLK1* 4<> 5<> 7<>

FBCKE AB31 FBBCKE H34 FBBCKE 4<> 5<> 7<>

FBVDDQ FBVREF J17 FBVREF
R615 1K 1% 0402 COMMON
C745 .1UF 10V 10% X7R 0402 COMMON
R616 1K 1% 0402 COMMON
C768 .1UF 10V 10% X7R 0402 COMMON
C771 2PF 50V +/-0.25PF C0G 0402 COMMON
GND
FB_DLLVDD J18 FB_DLLVDD
A01-02.8V, 1K/1K = 1.382/1.4/1.42V
A02-02.5V, 1K/1K = 1.212/1.252/1.294V

A3V3
150-220R@100MHz LB502 BEAD_0805 COMMON
C785 4.7UF 6.3V 10% X5R 0805 COMMON
C779 4700PF 25V 10% X7R 0402 COMMON
C778 470PF 50V 10% X7R 0402 COMMON
GND

CLK SOURCE TERM-BANK 1
Place Near GPU
FBACLK0 FBACLK0* R602 100 0402 1% NO STUFF
FBBCLK0 FBBCLK0* R603 100 0402 1% NO STUFF
FBCCLK0 FBCCLK0* R619 100 0402 1% NO STUFF
FBDCLK0 FBDCLK0* R630 100 0402 1% NO STUFF

NET RULES

NET	DIFFPAIR	SPACING
FBACLK0	FBACLK0	20MIL
FBACLK0*	FBACLK0	20MIL
FBACLK1	FBACLK1	20MIL
FBACLK1*	FBACLK1	20MIL
FBBCLK0	FBBCLK0	20MIL
FBBCLK0*	FBBCLK0	20MIL
FBBCLK1	FBBCLK1	20MIL
FBBCLK1*	FBBCLK1	20MIL
FBAD<31..0>		15MIL
FBBD<31..0>		15MIL
FBADQM0		15MIL
FBADQM1		15MIL
FBADQM2		15MIL
FBADQM3		15MIL
FBADQS0	FBADQS0	20MIL
FBADQS0*	FBADQS0	20MIL
FBADQS1	FBADQS1	20MIL
FBADQS1*	FBADQS1	20MIL
FBADQS2	FBADQS2	20MIL
FBADQS2*	FBADQS2	20MIL
FBADQS3	FBADQS3	20MIL
FBADQS3*	FBADQS3	20MIL
FBBDQS0	FBBDQS0	20MIL
FBBDQS0*	FBBDQS0	20MIL
FBBDQS1	FBBDQS1	20MIL
FBBDQS1*	FBBDQS1	20MIL
FBBDQS2	FBBDQS2	20MIL
FBBDQS2*	FBBDQS2	20MIL
FBBDQS3	FBBDQS3	20MIL
FBBDQS3*	FBBDQS3	20MIL
FBAA<12..0>		15MIL
FBBA<12..0>		15MIL
FBARAS*		15MIL
FBACAS*		15MIL
FBAWE*		15MIL
FBACS0*		15MIL
FBACS1*		15MIL
FBABA0		15MIL
FBABA1		15MIL
FBACKE		15MIL
FBBRAS*		15MIL
FBBCAS*		15MIL
FBBWE*		15MIL
FBBCS0*		15MIL
FBBCS1*		15MIL
FBBBA0		15MIL
FBBBA1		15MIL
FBBCKE		15MIL

NET RULES

NET	PHYSICAL	SPACING
FB_CAL_PD_VDDQ	12MIL_TRACE	20MIL
FB_CAL_PU_GND	12MIL_TRACE	20MIL
FB_CAL_CLK_GND	12MIL_TRACE	20MIL
FB_CAL_TERM_GND	12MIL_TRACE	20MIL

U8
GF-FX_DKTP_A2
BGA956
ALTCOM
3/14 MEM_C_D

FBVTT

L18 L21 L23 L24 M24 P24 T24 U24 V24 W24

FBVTT

AA24 AC24 J10 J9 K9 L10 L11 L12 L14 L17

Place near BGA

C602 .01UF 16V 10% X7R 0402 COMMON
C669 .001UF 50V 10% X7R 0402 COMMON
C704 .022UF 16V 10% X7R 0402 COMMON
C740 2200PF 10V 20% X7R 0402 COMMON
C525 .022UF 16V 10% X7R 0402 COMMON
C702 .1UF 10V 10% X7R 0402 COMMON
C526 .01UF 16V 10% X7R 0402 COMMON
C741 2200PF 10V 20% X7R 0402 COMMON
C705 .01UF 16V 10% X7R 0402 COMMON
C686 .001UF 50V 10% X7R 0402 COMMON
C707 .022UF 16V 10% X7R 0402 COMMON
C524 .1UF 10V 10% X7R 0402 COMMON
C703 .001UF 50V 10% X7R 0402 COMMON
C787 .022UF 16V 10% X7R 0402 COMMON
C742 2200PF 10V 20% X7R 0402 COMMON
C762 .022UF 16V 10% X7R 0402 COMMON
C743 2200PF 10V 20% X7R 0402 COMMON
C713 .001UF 50V 10% X7R 0402 COMMON
C716 .022UF 16V 10% X7R 0402 COMMON
C687 .001UF 50V 10% X7R 0402 COMMON
C600 .01UF 16V 10% X7R 0402 COMMON
C606 .001UF 50V 10% X7R 0402 COMMON
C712 4.7UF 6.3V 10% X5R 0805 COMMON

GND

8<> 6<> 4<> B1 FBCD<31..0>

0 FBCD<0>	B16	FBCD<0>
1 FBCD<1>	D16	FBCD<1>
2 FBCD<2>	A17	FBCD<2>
3 FBCD<3>	B17	FBCD<3>
4 FBCD<4>	B19	FBCD<4>
5 FBCD<5>	D19	FBCD<5>
6 FBCD<6>	A20	FBCD<6>
7 FBCD<7>	B20	FBCD<7>
8 FBCD<8>	G17	FBCD<8>
9 FBCD<9>	F18	FBCD<9>
10 FBCD<10>	E17	FBCD<10>
11 FBCD<11>	D17	FBCD<11>
12 FBCD<12>	G18	FBCD<12>
13 FBCD<13>	F20	FBCD<13>
14 FBCD<14>	G20	FBCD<14>
15 FBCD<15>	F21	FBCD<15>
16 FBCD<16>	G24	FBCD<16>
17 FBCD<17>	F26	FBCD<17>
18 FBCD<18>	G27	FBCD<18>
19 FBCD<19>	G26	FBCD<19>
20 FBCD<20>	D27	FBCD<20>
21 FBCD<21>	E28	FBCD<21>
22 FBCD<22>	D29	FBCD<22>
23 FBCD<23>	C30	FBCD<23>
24 FBCD<24>	A26	FBCD<24>
25 FBCD<25>	B26	FBCD<25>
26 FBCD<26>	C26	FBCD<26>
27 FBCD<27>	B27	FBCD<27>
28 FBCD<28>	A29	FBCD<28>
29 FBCD<29>	B29	FBCD<29>
30 FBCD<30>	C29	FBCD<30>
31 FBCD<31>	B30	FBCD<31>

FBDD<31..0> B1 8<> 4<> 6<>

D2 FBDD<0>	0	FBDD<0>
C1 FBDD<1>	1	FBDD<1>
C2 FBDD<2>	2	FBDD<2>
B1 FBDD<3>	3	FBDD<3>
B4 FBDD<4>	4	FBDD<4>
A5 FBDD<5>	5	FBDD<5>
B5 FBDD<6>	6	FBDD<6>
C5 FBDD<7>	7	FBDD<7>
D3 FBDD<8>	8	FBDD<8>
D5 FBDD<9>	9	FBDD<9>
C3 FBDD<10>	10	FBDD<10>
C4 FBDD<11>	11	FBDD<11>
F6 FBDD<12>	12	FBDD<12>
F8 FBDD<13>	13	FBDD<13>
G8 FBDD<14>	14	FBDD<14>
F9 FBDD<15>	15	FBDD<15>
G12 FBDD<16>	16	FBDD<16>
F14 FBDD<17>	17	FBDD<17>
G14 FBDD<18>	18	FBDD<18>
F15 FBDD<19>	19	FBDD<19>
E16 FBDD<20>	20	FBDD<20>
F16 FBDD<21>	21	FBDD<21>
G15 FBDD<22>	22	FBDD<22>
F17 FBDD<23>	23	FBDD<23>
B11 FBDD<24>	24	FBDD<24>
C11 FBDD<25>	25	FBDD<25>
B12 FBDD<26>	26	FBDD<26>
C12 FBDD<27>	27	FBDD<27>
D13 FBDD<28>	28	FBDD<28>
C14 FBDD<29>	29	FBDD<29>
B15 FBDD<30>	30	FBDD<30>
C15 FBDD<31>	31	FBDD<31>

OUT FBCA<12..0> 8<> 6<> 4<>

0 FBCA<0>	G23	FBCA<0>
1 FBCA<1>	E23	FBCA<1>
2 FBCA<2>	D23	FBCA<2>
3 FBCA<3>	F24	FBCA<3>
4 FBCA<4>	G21	FBCA<4>
5 FBCA<5>	E22	FBCA<5>
6 FBCA<6>	F22	FBCA<6>
7 FBCA<7>	F23	FBCA<7>
8 FBCA<8>	C20	FBCA<8>
9 FBCA<9>	B21	FBCA<9>
10 FBCA<10>	D25	FBCA<10>
11 FBCA<11>	F25	FBCA<11>
12 FBCA<12>	C23	FBCA<12>
TP_FBCA13	D21	FBCA<13>

FBCBA0 B25 FBCBANK<0>
FBCBA1 C21 FBCBANK<1>

FBCRAS* C24 FBCRAS
FBCCAS* B24 FBCCAS
FBCWE* B22 FBCWE
FBCCS0* B23 FBCCS0
FBCCS1* A23 FBCCS1

FBCCLK0 E20 FBCCLK0
FBCCLK0* D20 FBCCLK0
FBCCLK1 E25 FBCCLK1
FBCCLK1* D24 FBCCLK1

FBCCKE D22 FBCCKE

FBVDDQ
R623 47.5 1% 0402 COMMON
GND

FB_CAL_PD_VDDQ L16 FB_CAL_PD_VDDQ
FB_CAL_PU_GND L19 FB_CAL_PU_GND
FB_CAL_CLK_GND K16 FB_CAL_CLK_GND
FB_CAL_TERM_GND K19 FB_CAL_TERM_GND

R621 47.5 1% 0402 COMMON
R628 549 1% 0402 COMMON
R620 47.5 1% 0402 COMMON

FB_CAL_CLK_GND-A01, A02
549ohm for Target Termination of 200ohm
357ohm for Source Termination of 100ohm(Not used)
FBCALTERMGND-A01-40.2R, A02-47.5
FBCALPUGND-A01-20R, A02-47.5
FBCALPDVDDQ-A01-20R, A02-47.5

FBDA<12..0> OUT 4<> 6<> 8<>

0 FBDA<0>	G11	FBDA<0>
1 FBDA<1>	E11	FBDA<1>
2 FBDA<2>	D11	FBDA<2>
3 FBDA<3>	F12	FBDA<3>
4 FBDA<4>	G9	FBDA<4>
5 FBDA<5>	E10	FBDA<5>
6 FBDA<6>	F10	FBDA<6>
7 FBDA<7>	F11	FBDA<7>
8 FBDA<8>	B6	FBDA<8>
9 FBDA<9>	C6	FBDA<9>
10 FBDA<10>	A11	FBDA<10>
11 FBDA<11>	D12	FBDA<11>
12 FBDA<12>	B9	FBDA<12>
TP_FBDA13	D9	FBDA<13>

FBDBA0 D10 FBDBANK<0>
FBDBA1 B7 FBDBANK<1>

FBDRAS* B10 FBDRAS
FBDCAS* C9 FBDCAS
FBDWE* B7 FBDWE
FBDCS0* C8 FBDCS0
FBDCS1* B8 FBDCS1

FBDCLK0 E8 FBDCLK0
FBDCLK0* D8 FBDCLK0*
FBDCLK1 F13 FBDCLK1
FBDCLK1* E13 FBDCLK1*

FBDCKE A8 FBDCKE

FBDQM<0> A2 FBDDQM0
FBDQM<1> F7 FBDDQM1
FBDQM<2> E14 FBDDQM2
FBDQM<3> B13 FBDDQM3

FBDQS0 A3 FBDDQS0
FBDQS0* B3 FBDDQS0*
FBDQS1 E7 FBDDQS1
FBDQS1* D6 FBDDQS1*
FBDQS2 D14 FBDDQS2
FBDQS2* D15 FBDDQS2*
FBDQS3 A14 FBDDQS3
FBDQS3* B14 FBDDQS3*

Place near BGA

C601 .01UF 16V 10% X7R 0402 COMMON
C668 .001UF 50V 10% X7R 0402 COMMON
C703 .022UF 16V 10% X7R 0402 COMMON
C739 2200PF 10V 20% X7R 0402 COMMON
C524 .022UF 16V 10% X7R 0402 COMMON
C701 .1UF 10V 10% X7R 0402 COMMON
C525 .01UF 16V 10% X7R 0402 COMMON
C740 2200PF 10V 20% X7R 0402 COMMON
C704 .022UF 16V 10% X7R 0402 COMMON
C667 .001UF 50V 10% X7R 0402 COMMON
C706 .022UF 16V 10% X7R 0402 COMMON
C523 .1UF 10V 10% X7R 0402 COMMON
C522 .01UF 16V 10% X7R 0402 COMMON
C741 2200PF 10V 20% X7R 0402 COMMON
C705 .01UF 16V 10% X7R 0402 COMMON
C686 .001UF 50V 10% X7R 0402 COMMON
C707 .022UF 16V 10% X7R 0402 COMMON
C524 .1UF 10V 10% X7R 0402 COMMON
C712 .001UF 50V 10% X7R 0402 COMMON
C742 2200PF 10V 20% X7R 0402 COMMON
C762 .022UF 16V 10% X7R 0402 COMMON
C743 2200PF 10V 20% X7R 0402 COMMON
C711 .001UF 50V 10% X7R 0402 COMMON
C716 .022UF 16V 10% X7R 0402 COMMON
C687 .001UF 50V 10% X7R 0402 COMMON
C600 .01UF 16V 10% X7R 0402 COMMON
C606 .001UF 50V 10% X7R 0402 COMMON
C712 4.7UF 6.3V 10% X5R 0805 COMMON

GND

FBDA<12..0> OUT 4<> 6<> 8<>

CLK SOURCE TERM-BANK 2
Place Near GPU
FBACLK1 FBACLK1* R602 100 0402 1% NO STUFF
FBBCLK1 FBBCLK1* R603 100 0402 1% NO STUFF
FBCCLK1 FBCCLK1* R614 100 0402 1% NO STUFF
FBDCLK1 FBDCLK1* R629 100 0402 1% NO STUFF

NET RULES

NET	DIFFPAIR	SPACING
FBCCLK0	FBCCLK0	20MIL
FBCCLK0*	FBCCLK0	20MIL
FBCCLK1	FBCCLK1	20MIL
FBCCLK1*	FBCCLK1	20MIL
FBDCLK0	FBDCLK0	20MIL
FBDCLK0*	FBDCLK0	20MIL
FBDCLK1	FBDCLK1	20MIL
FBDCLK1*	FBDCLK1	20MIL
FBCD<31..0>		15MIL
FBDD<31..0>		15MIL
FBCDQM0		15MIL
FBCDQM1		15MIL
FBCDQM2		15MIL
FBCDQM3		15MIL
FBDDQM0		15MIL
FBDDQM1		15MIL
FBDDQM2		15MIL
FBDDQM3		15MIL
FBCDQS0	FBCDQS0	20MIL
FBCDQS0*	FBCDQS0	20MIL
FBCDQS1	FBCDQS1	20MIL
FBCDQS1*	FBCDQS1	20MIL
FBCDQS2	FBCDQS2	20MIL
FBCDQS2*	FBCDQS2	20MIL
FBCDQS3	FBCDQS3	20MIL
FBCDQS3*	FBCDQS3	20MIL
FBDDQS0	FBDDQS0	20MIL
FBDDQS0*	FBDDQS0	20MIL
FBDDQS1	FBDDQS1	20MIL
FBDDQS1*	FBDDQS1	20MIL
FBDDQS2	FBDDQS2	20MIL
FBDDQS2*	FBDDQS2	20MIL
FBDDQS3	FBDDQS3	20MIL
FBDDQS3*	FBDDQS3	20MIL
FBCA<12..0>		15MIL
FBDA<12..0>		15MIL
FBCRAS*		15MIL
FBCCAS*		15MIL
FBCWE*		15MIL
FBCCS0*		15MIL
FBCCS1*		15MIL
FBCBA0		15MIL
FBCBA1		15MIL
FBCCKE		15MIL
FBDRAS*		15MIL
FBDCAS*		15MIL
FBDWE*		15MIL
FBDCS0*		15MIL
FBDCS1*		15MIL
FBDBA0		15MIL
FBDBA1		15MIL
FBDCKE		15MIL

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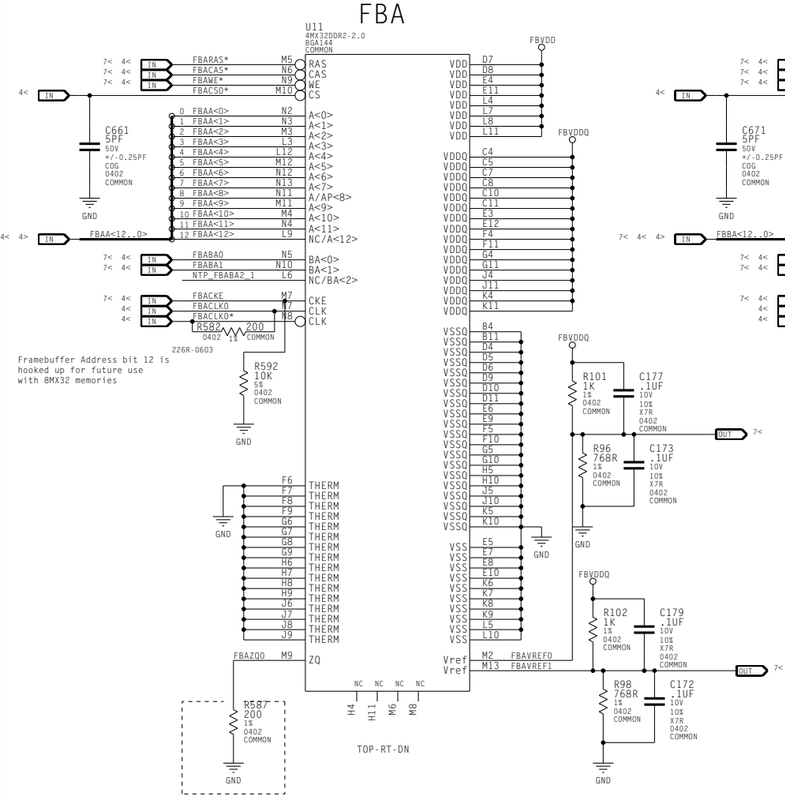
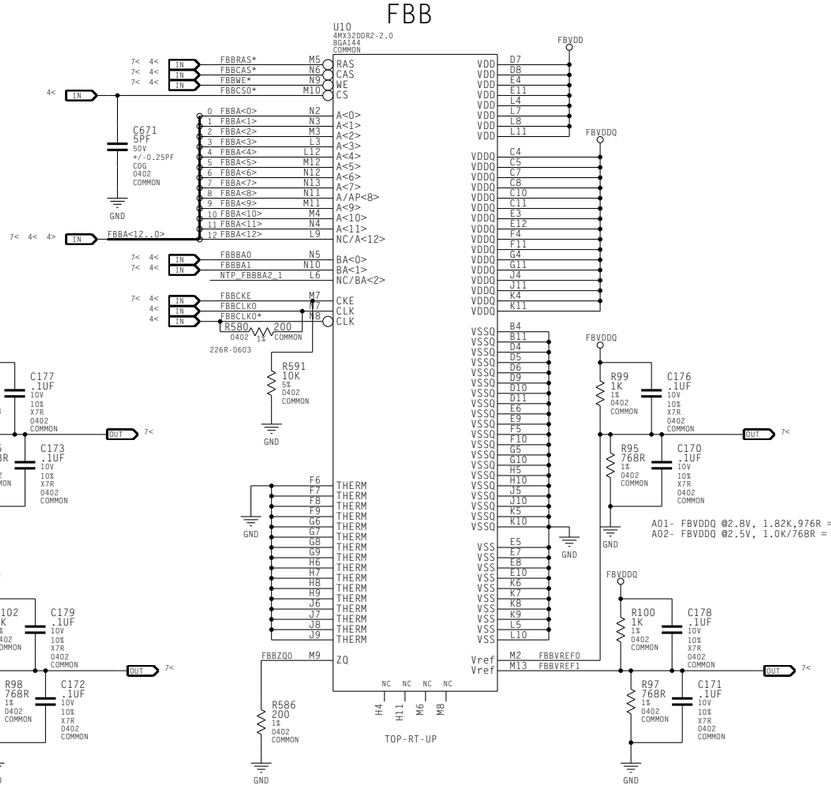
DETAIL	DRAWING DETAIL CONTINUED...		
ID	p126_a05_sch	PAGE	4 OF 32
NAME	140-10126-000-005-X13	DATE	FEB-14-2003

2.b. Memory: Bank1: FBA & FBB

FBA



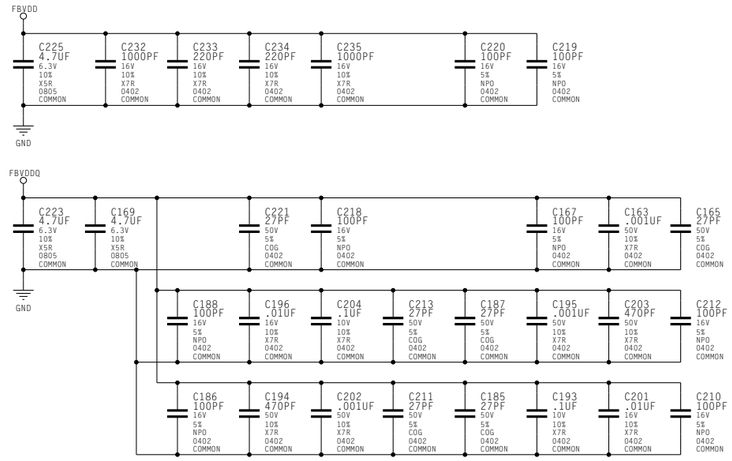
FBB



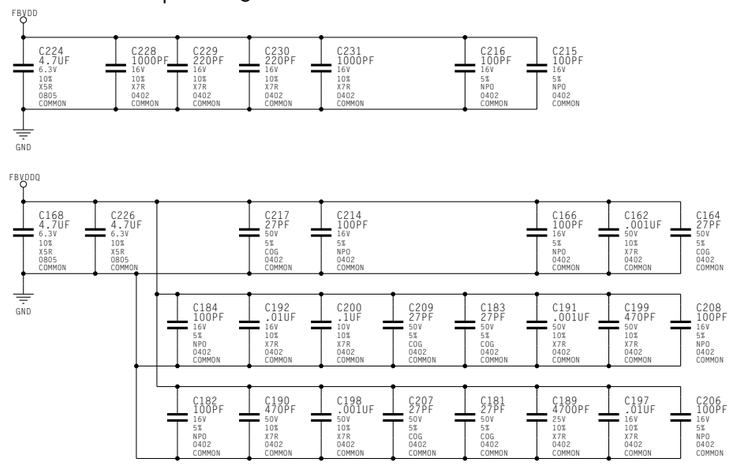
A01- FBVDDQ @2.8V, 1.82K,976R = 0.968/0.978/0.988V
A02- FBVDDQ @2.5V, 1.0K/768R = 1.0513/1.0879/1.126V

A01- ZQ is 90ohm(?) with One Load and 200ohm with two loads

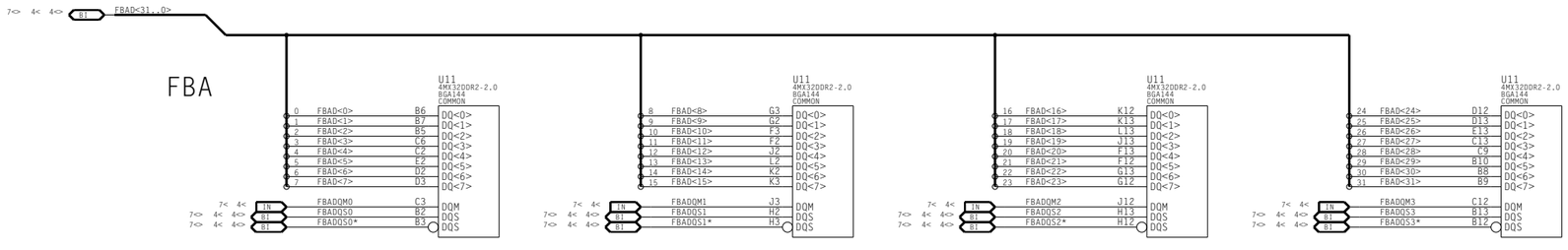
Decoupling for FBA



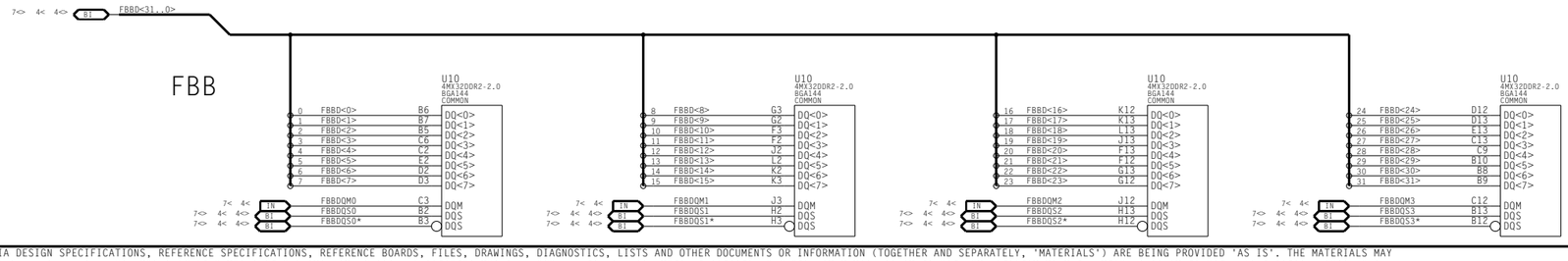
Decoupling for FBB



FBA



FBB



NET RULES

NET	PHYSICAL
FBAZQ0	12MIL_TRACE
FBBZQ0	12MIL_TRACE

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DETAIL	Memory Page 1 CONTINUED...		
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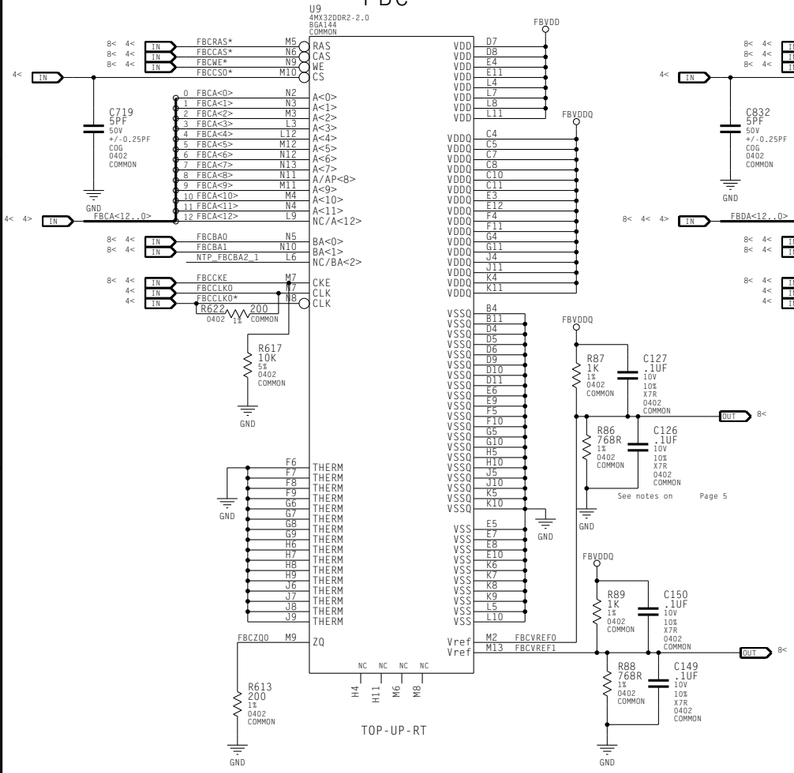
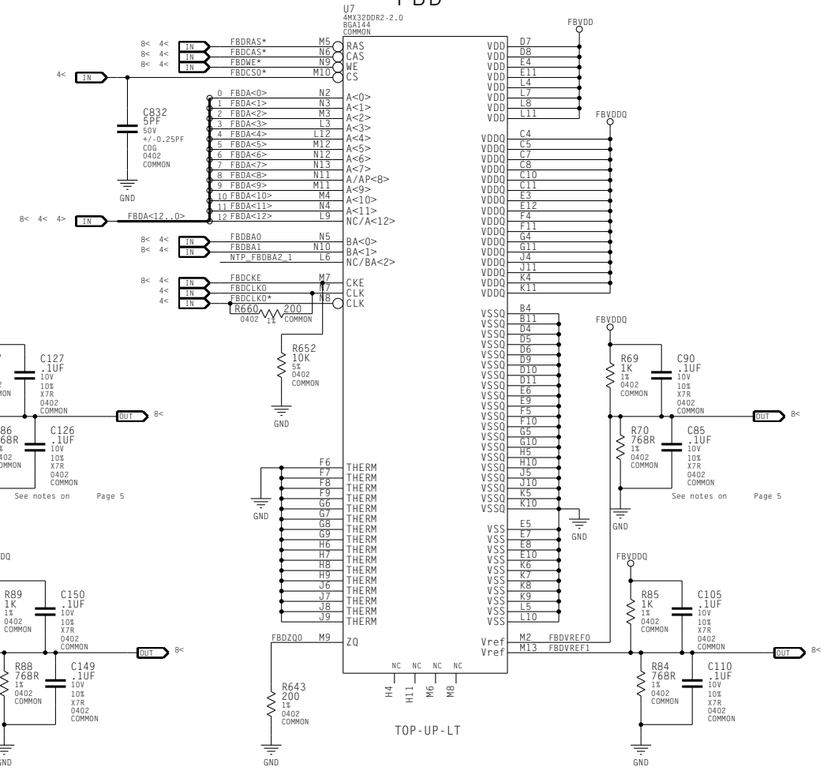
2.c. Memory: Bank1: FBC & FBD

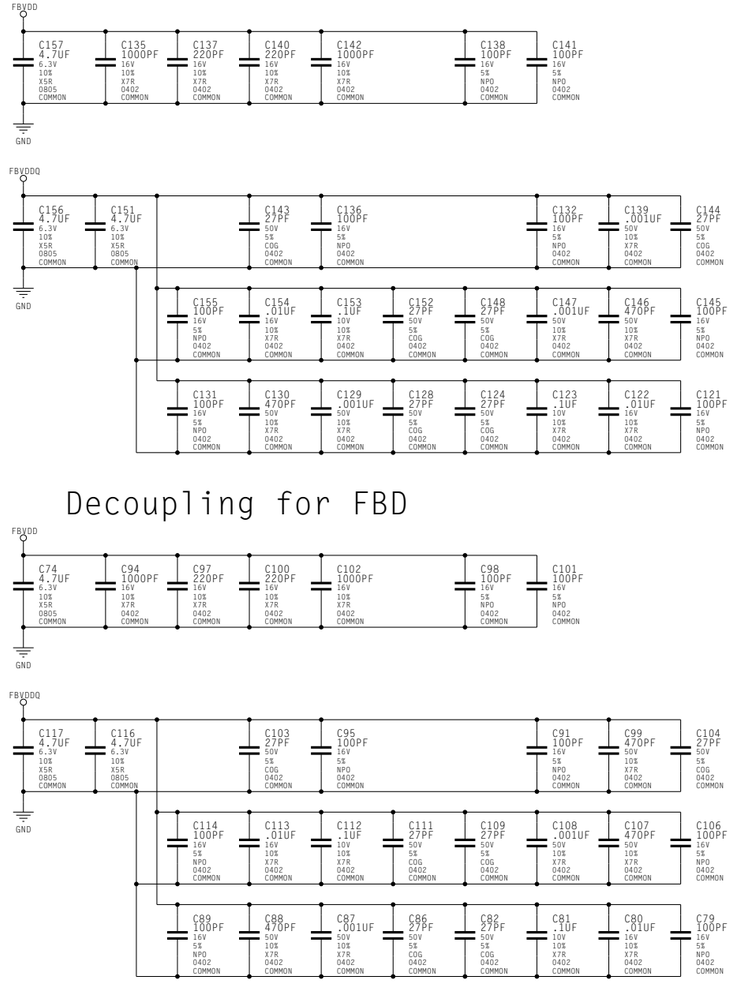
FBC



FBD



Decoupling for FBC



Decoupling for FBD

NET RULES

NET	PHYSICAL
FBCZQ0	12MIL_TRACE
FBDZQ0	12MIL_TRACE

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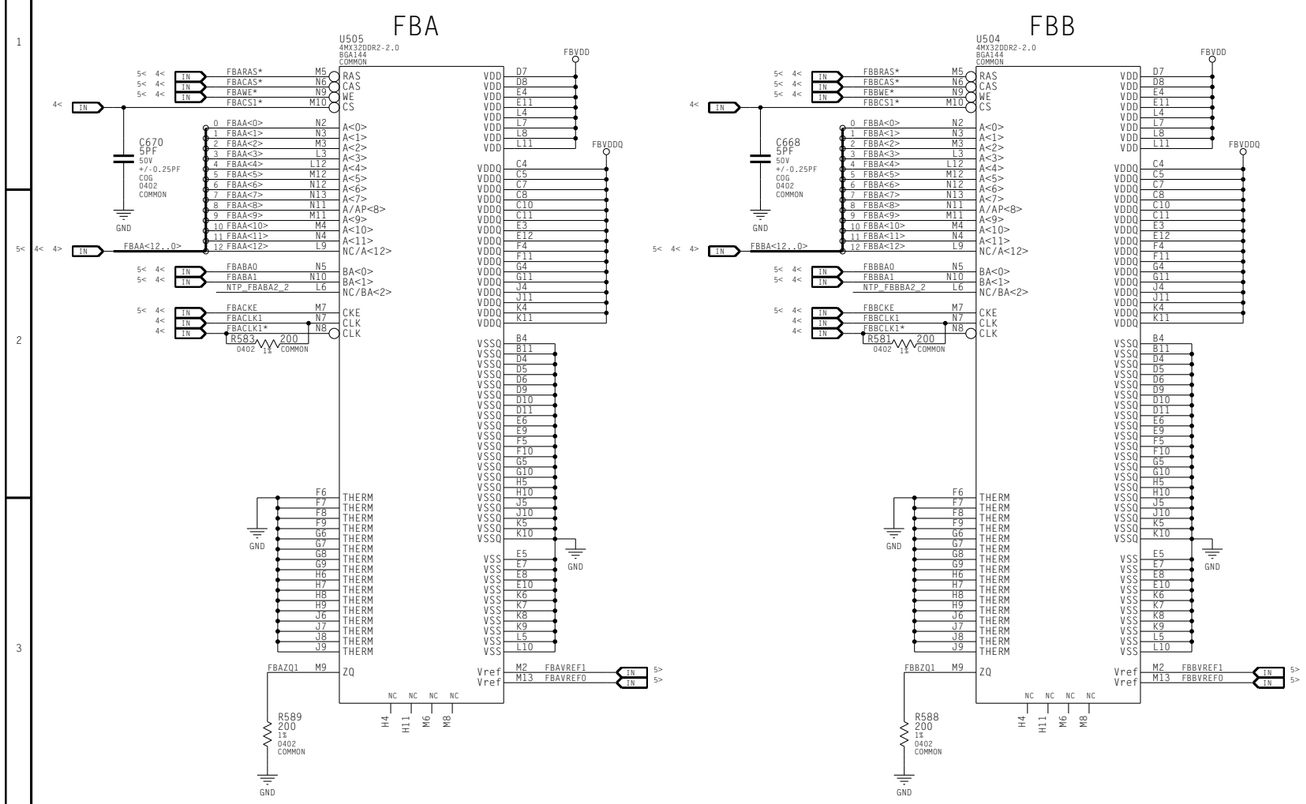
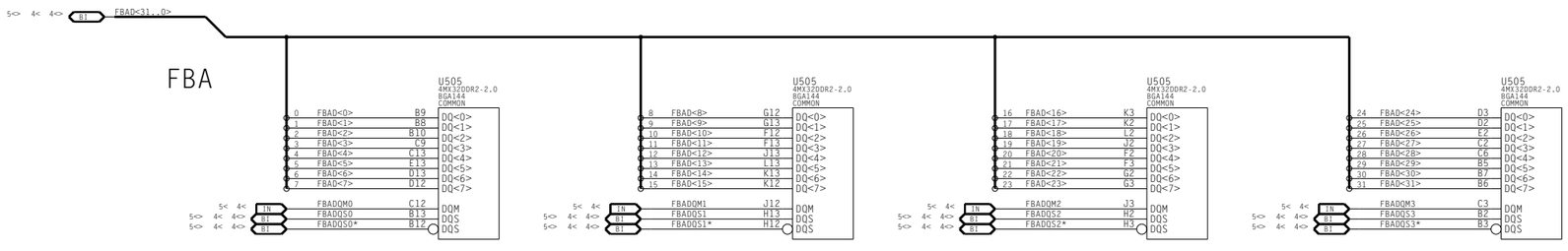
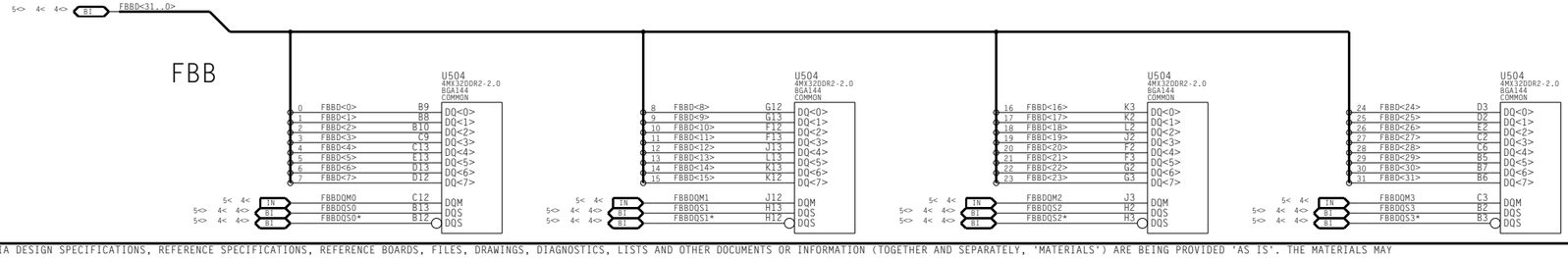
SANTA CLARA, CA 95050, USA

DETAIL	Memory Page 2 CONTINUED...		
ID	p126_a05_sch	PAGE	6 OF 32
NAME	140-10126-000-005-X13	DATE	FEB-14-2003

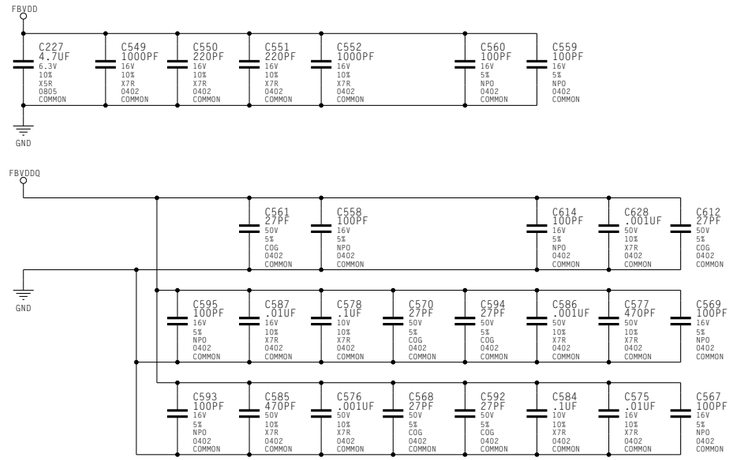
2.d. Memory: Bank2: FBA & FBB



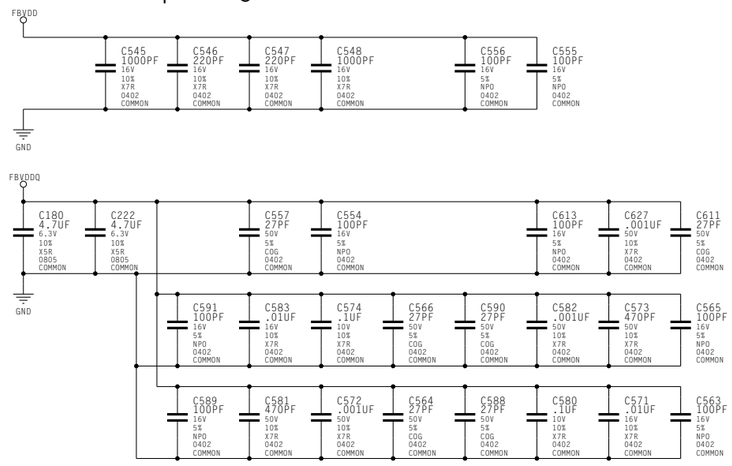




Decoupling for FBA



Decoupling for FBB



NET RULES

NET		PHYSICAL
IN	FBAZQ1	12MIL_TRACE
IN	FBBZQ1	12MIL_TRACE

NVIDIA CORPORATION
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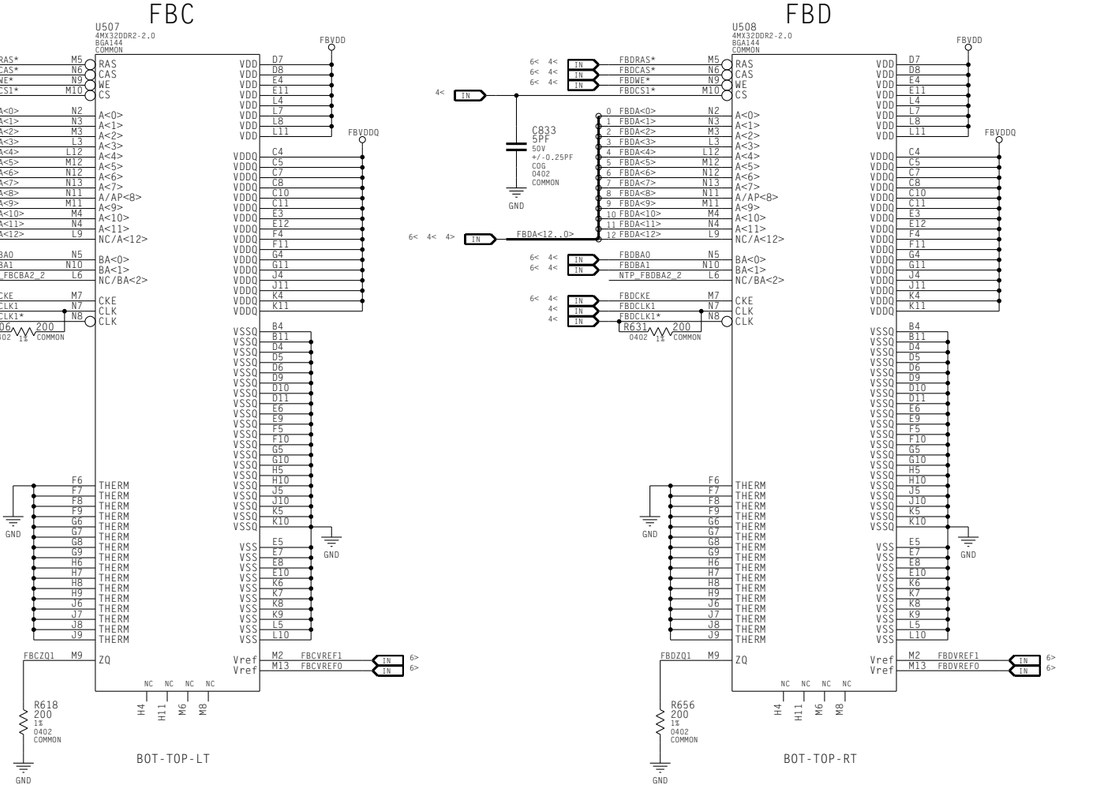
SANTA CLARA, CA 95050, USA

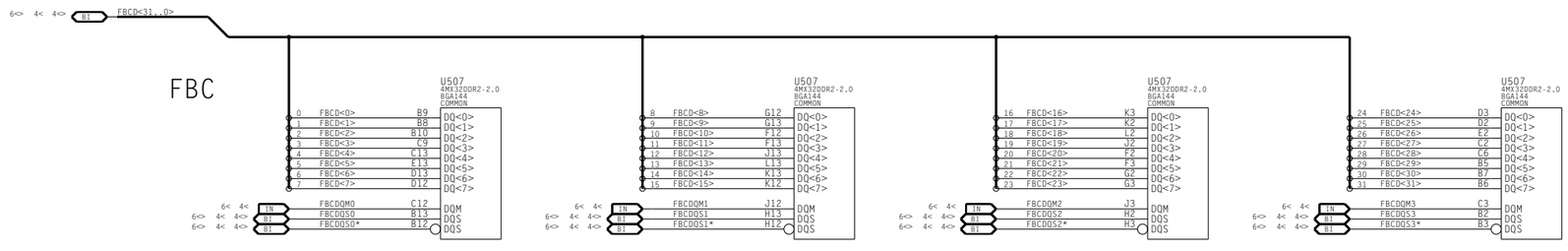
DETAIL	DRAWING DETAIL CONTINUED...		
ID	p126_a05_sch	PAGE	7 OF 32
NAME	140-10126-000-005-X13	DATE	FEB-14-2003

2.e. Memory: Bank2: FBC & FBD

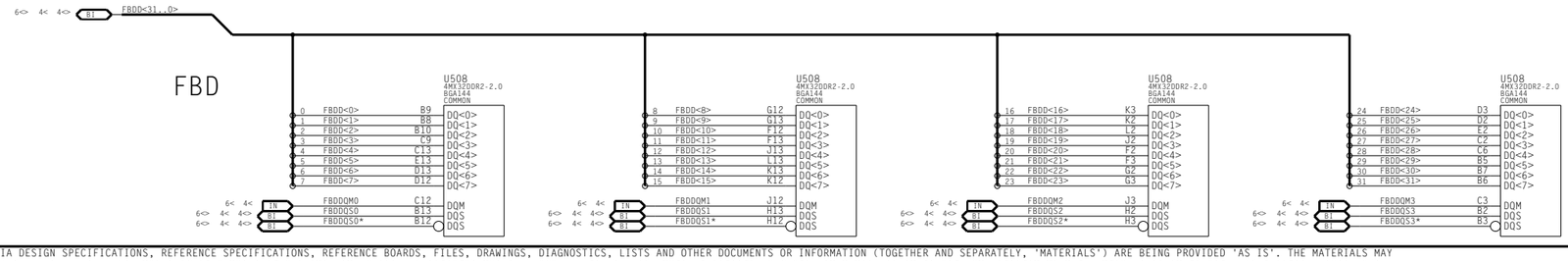
FBC



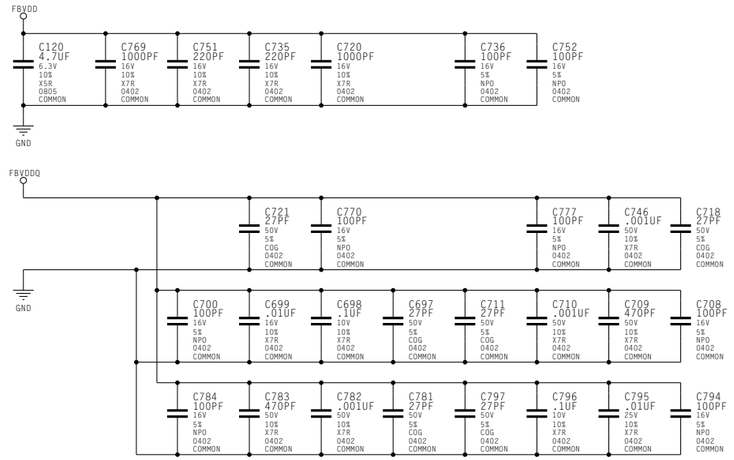
FBC



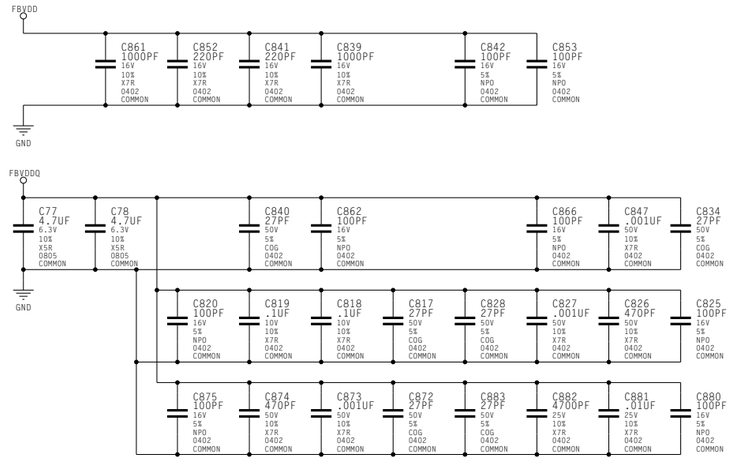
FBD



Decoupling for FBC



Decoupling for FBD



NET RULES

NET	PHYSICAL
FBCZQ1	12MIL_TRACE
FBDZQ1	12MIL_TRACE

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DETAIL	DRAWING DETAIL CONTINUED...		
ID	p126_a05_sch	PAGE	8 OF 32
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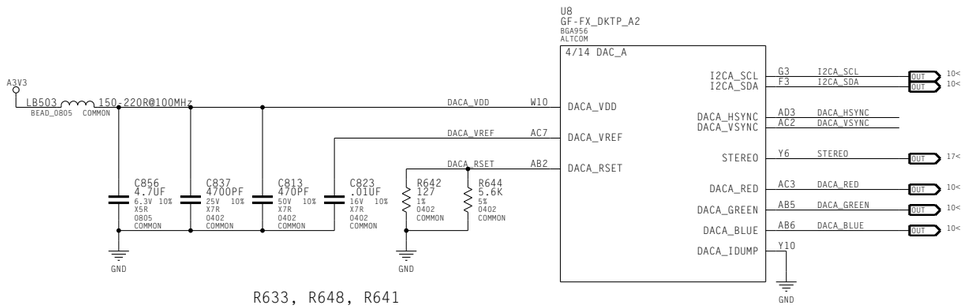
3.a. DAC and PLL

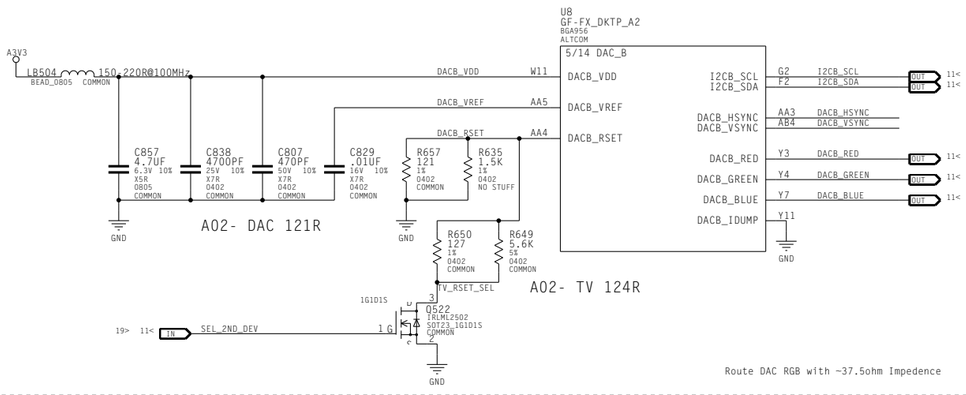
DACA



R633, R648, R641
A01-68R
A02- 124R

Route DAC RGB with ~37.5ohm Impedence

DACB



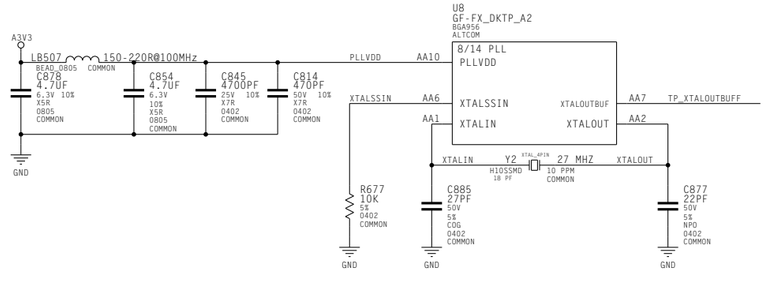
A02- DAC 121R

A02- TV 124R

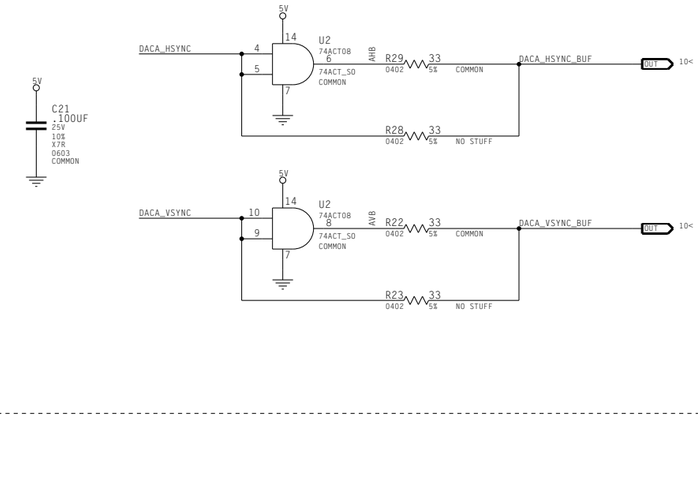
To QuickSwitch

Route DAC RGB with ~37.5ohm Impedence

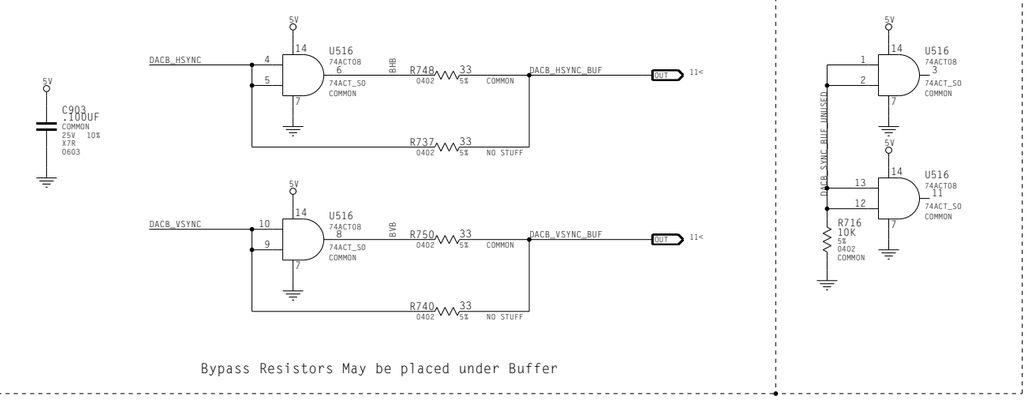
XTAL/PLLVDD



DAC Sync Buffer



Unused Buffers



Bypass Resistors May be placed under Buffer

NET RULES

NET	PHYSICAL	VOLTAGE
XTALIN	18MIL_TRACE	
XTALOUT	18MIL_TRACE	
DACA_VDD	12MIL_TRACE	3.3V
DACA_VREF	5MIL_TRACE	
DACA_RSET	5MIL_TRACE	
DACB_VDD	12MIL_TRACE	3.3V
DACB_VREF	5MIL_TRACE	
DACB_RSET	5MIL_TRACE	
TV_RSET_SEL	5MIL_TRACE	
PLLVDD	12MIL_TRACE	3.3V

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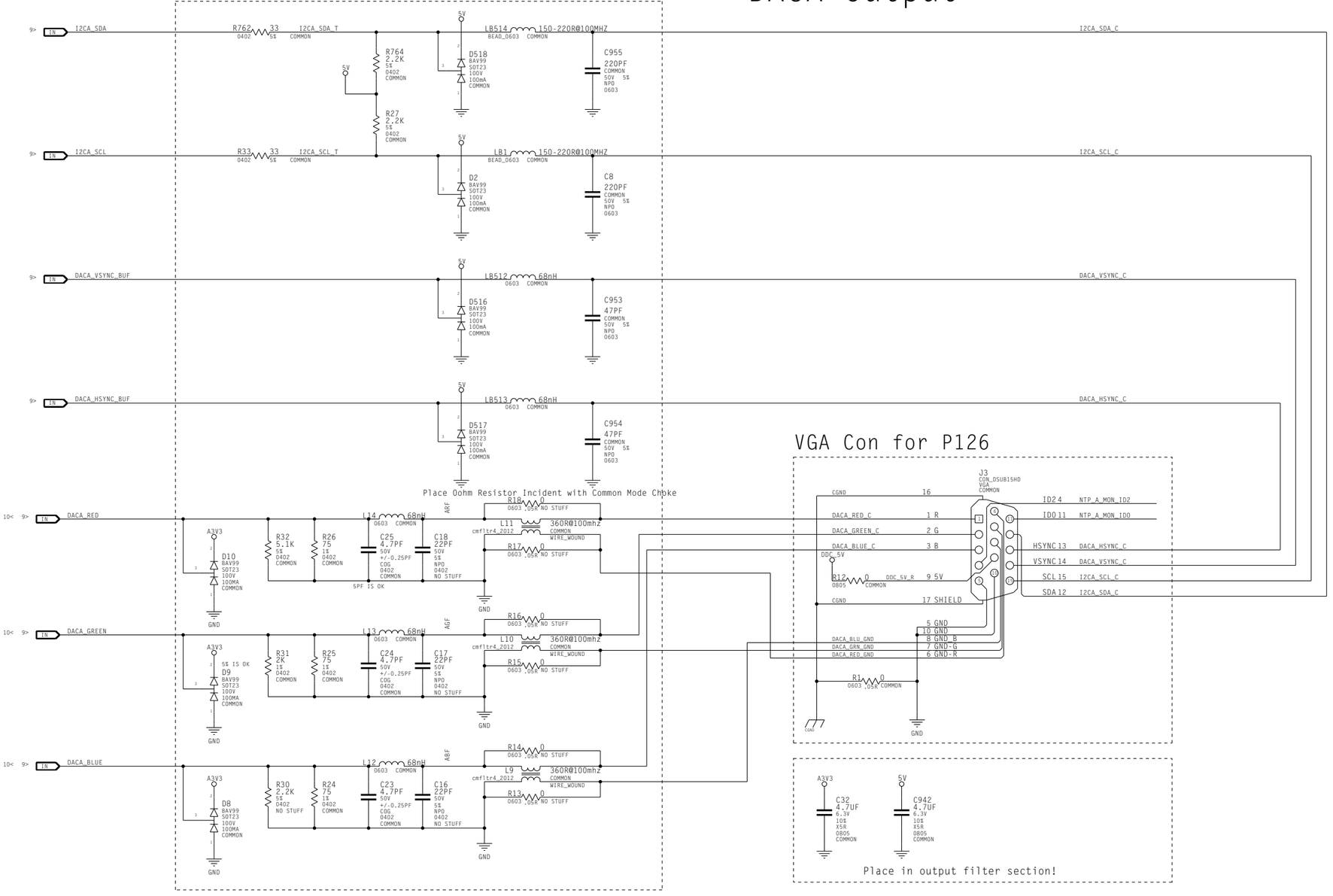
3.b. DACA Output

RGB-FILTER

DACA output



NET RULES

	NET	SPACING
10< 9> IN	DACA_RED	20MIL
10< 9> IN	DACA_GREEN	20MIL
10< 9> IN	DACA_BLUE	20MIL
IN	DACA_RED_C	20MIL
IN	DACA_GREEN_C	20MIL
IN	DACA_BLUE_C	20MIL

	NET	PHYSICAL
IN	DACA_RED_GND	12MIL_TRACE
IN	DACA_GRN_GND	12MIL_TRACE
IN	DACA_BLU_GND	12MIL_TRACE

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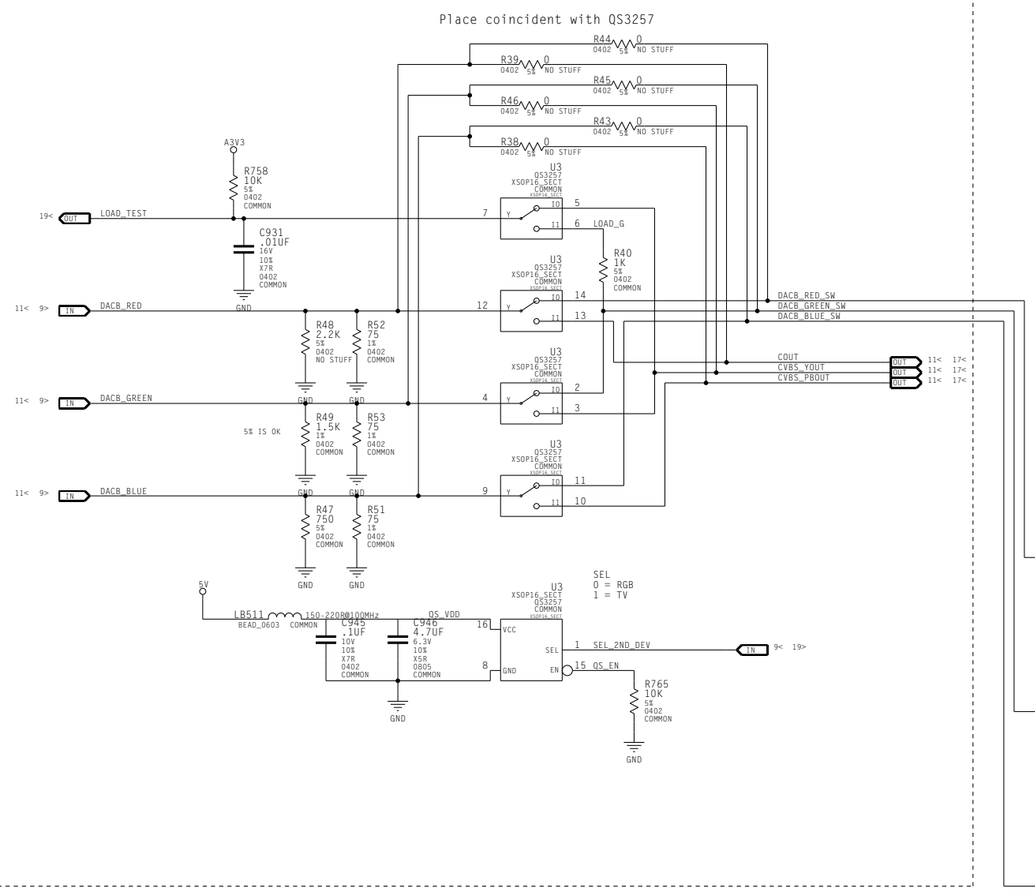
3.c. DACB Output

Quickswitch for DACB

Place Quickswitch near DACB filter

Place coincident with QS3257



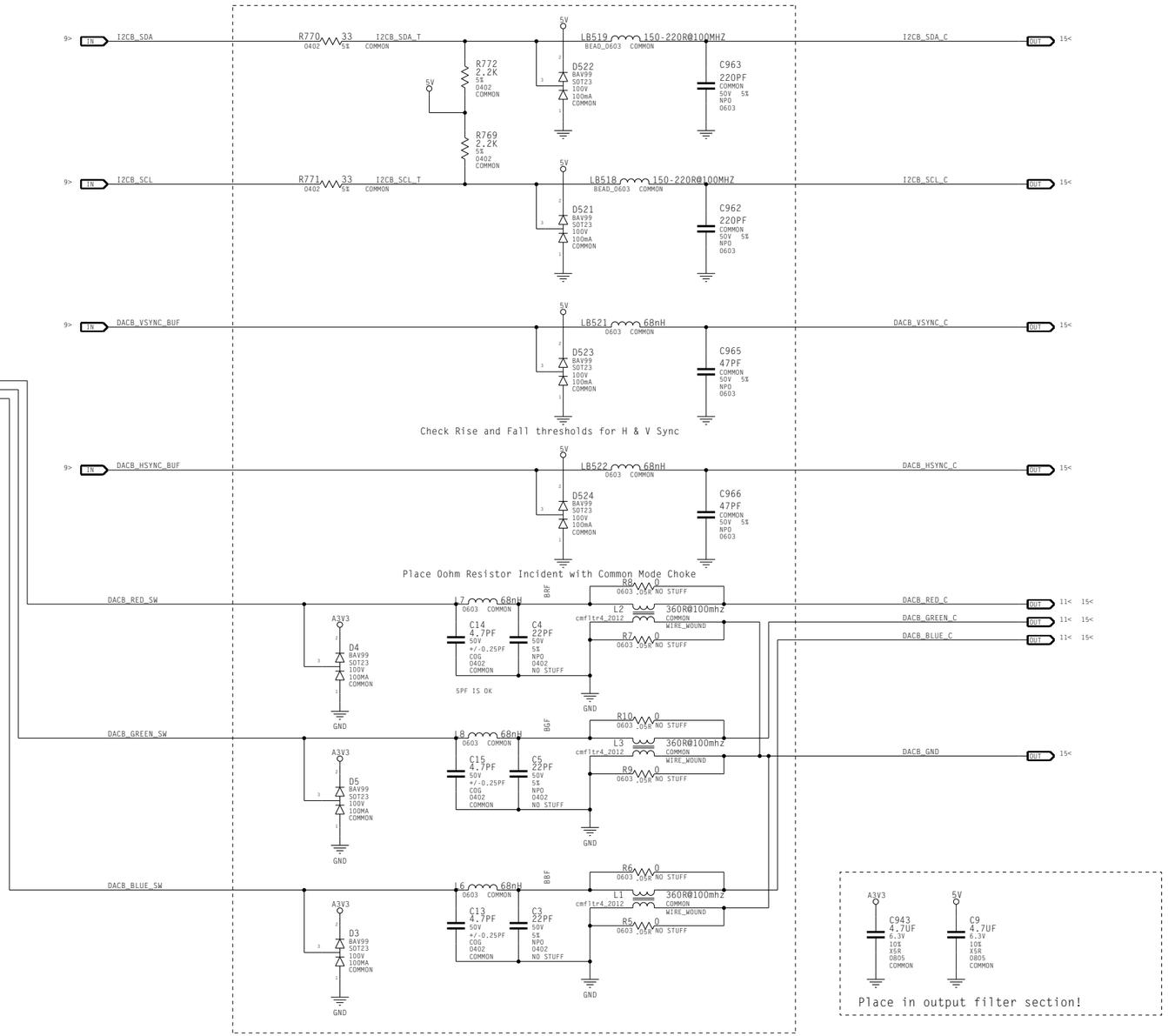
NET RULES

		NET	SPACING
11< 9>	IN	DACB_RED	20MIL
11< 9>	IN	DACB_GREEN	20MIL
11< 9>	IN	DACB_BLUE	20MIL
	IN	DACB_RED_SW	20MIL
	IN	DACB_GREEN_SW	20MIL
	IN	DACB_BLUE_SW	20MIL
15< 11>	IN	DACB_RED_C	20MIL
15< 11>	IN	DACB_GREEN_C	20MIL
15< 11>	IN	DACB_BLUE_C	20MIL
17< 11>	IN	COUT	20MIL
17< 11>	IN	CVBS_YOUT	20MIL
17< 11>	IN	CVBS_PBOUT	20MIL

	NET	PHYSICAL	VOLTAGE
IN	QS_VDD	12MIL_TRACE	5V

RGB-FILTER

DACB output



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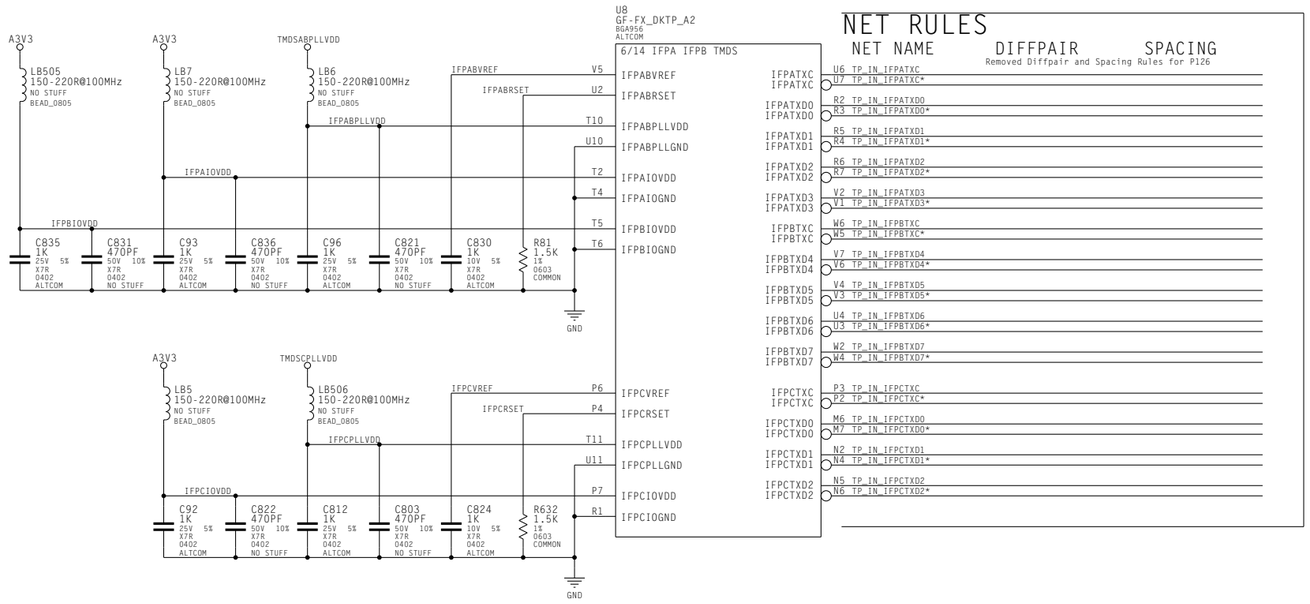
4.a. Internal TMDS



NET RULES

Removed Diffpair and Spacing Rules for P126

NET NAME	DIFFPAIR	SPACING

IFP Power should have alternate pull-down to GND when not used

NET RULES

	NET	PHYSICAL	VOLTAGE
IN	IFPABPLLVDD	12MIL_TRACE	3.3V
IN	IFPAIOVDD	12MIL_TRACE	3.3V
IN	IFPBIOVDD	12MIL_TRACE	3.3V
IN	IFPABVREF	10MIL_TRACE	3.3V
IN	IFPABRSET	10MIL_TRACE	3.3V
IN	IFPCPLLVDD	12MIL_TRACE	3.3V
IN	IFPCIOVDD	12MIL_TRACE	3.3V
IN	IFPCVREF	10MIL_TRACE	3.3V
IN	IFPCRSET	10MIL_TRACE	3.3V

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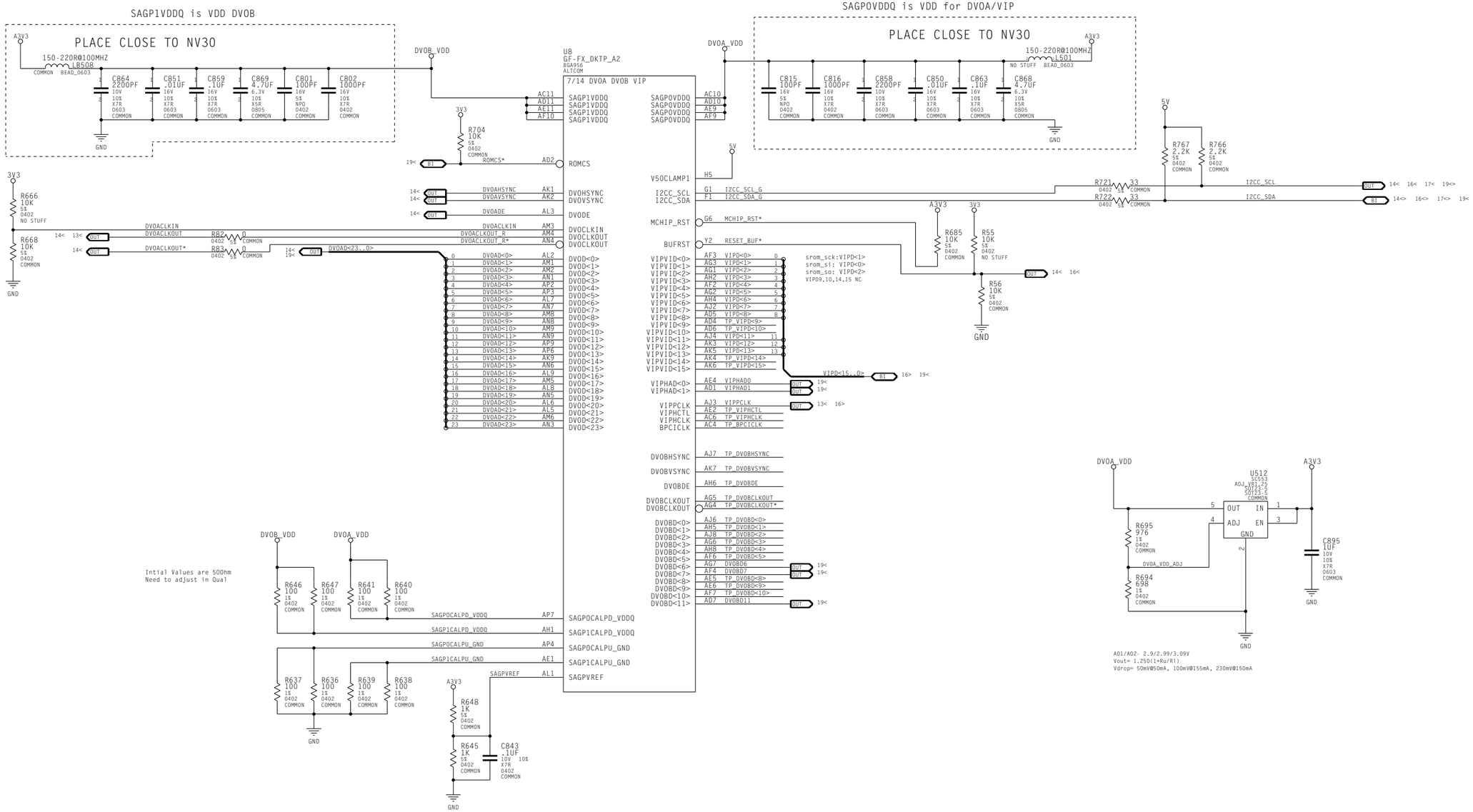
4.b. DVO/VIP Interface

NET RULES

	NET	PHYSICAL	SPACING
IN	SAGPOCALPD_VDDQ	12MIL_TRACE	20MIL
IN	SAGP1CALPD_VDDQ	12MIL_TRACE	20MIL
IN	SAGPOCALPU_GND	12MIL_TRACE	20MIL
IN	SAGP1CALPU_GND	12MIL_TRACE	20MIL
13> IN	DVOACLKOUT		20MIL
14< IN	DVOACLKOUT_R		20MIL
13> IN	VIPPCLK		20MIL
16>			



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4.c. DVOA: External Dual-Link Transmitter

Multi-Use PinMapping

DVOAD<0>	FP_DATA<23>
DVOAD<1>	FP_DATA<22>
DVOAD<2>	FP_DATA<21>
DVOAD<3>	FP_DATA<20>
DVOAD<4>	FP_DATA<19>
DVOAD<5>	FP_DATA<18>
DVOAD<6>	FP_DATA<17>
DVOAD<7>	FP_DATA<16>
DVOAD<8>	FP_DATA<15>
DVOAD<9>	FP_DATA<14>
DVOAD<10>	FP_DATA<13>
DVOAD<11>	FP_DATA<12>
DVOAD<12>	FP_DATA<0>
DVOAD<13>	FP_DATA<1>
DVOAD<14>	FP_DATA<2>
DVOAD<15>	FP_DATA<3>
DVOAD<16>	FP_DATA<4>
DVOAD<17>	FP_DATA<5>
DVOAD<18>	FP_DATA<6>
DVOAD<19>	FP_DATA<7>
DVOAD<20>	FP_DATA<8>
DVOAD<21>	FP_DATA<9>
DVOAD<22>	FP_DATA<10>
DVOAD<23>	FP_DATA<11>

Note a:
STUFFING OPTION:
Rdual for Dual-Link
Rsing for Single-Link

U4
SII178
78_TQFP64
NO STUFF

SII1xx (combi_sym)
SLAVE
TOP

NET SPACING RULES

NET NAME	DIFFPAIR	NET_SPACING_RULE
SIIA_TXD3	SIIA_TXD3	20MIL
SIIA_TXD3*	SIIA_TXD3	20MIL
SIIA_TXD4	SIIA_TXD4	20MIL
SIIA_TXD4*	SIIA_TXD4	20MIL
SIIA_TXD5	SIIA_TXD5	20MIL
SIIA_TXD5*	SIIA_TXD5	20MIL

U517
SII164
64_TQFP64
ALTCOM

SII1xx (combi_sym)
MASTER
BOTTOM

NET SPACING RULES

NET NAME	DIFFPAIR	NET_SPACING_RULE
SIIA_TXD0	SIIA_TXD0	20MIL
SIIA_TXD0*	SIIA_TXD0	20MIL
SIIA_TXD1	SIIA_TXD1	20MIL
SIIA_TXD1*	SIIA_TXD1	20MIL
SIIA_TXD2	SIIA_TXD2	20MIL
SIIA_TXD2*	SIIA_TXD2	20MIL
SIIA_TXC	SIIA_TXC	20MIL
SIIA_TXC*	SIIA_TXC	20MIL

For Single Link SIL164/168 is used

STUFF OPTION
Rx for SII164/166
Ry for SII178

Sil178 Dual-Link TMDS

ISEL/RST - I2C Interface Select.
HIGH - active (config programmed by I2C)

When ISEL/RST = HIGH
BSEL/SCL - I2C CLK
DSEL/SDA - I2C DATA

MASTER
I2C Address is 70h and is based on MAST and DUAL pins.

SLAVE
I2C Address is 72h

Notes:
Make sure Software knows and programs this correctly.
1. Detect Dual-Link Capable
2. Detect Master and Slave
3. Both Master and Slave transmitters must set bit 2 (BSEL) at register addr 0x0B to 0 for 12-biot mode
4. For frequencies less than or equal to 165Mhz, bit 0 (PD) at register addr 0x0B of Slave must be set to 0. For frequencies greater than 165Mhz, bit 0 (PD) at register addr 0x0B of Slave must be set to 1.
5. Skew beween Master and Slave can be controlled by DCTL[2:0] register
6. Both Single-Link and Dual-Link mode will be configured via I2CC

*May want to created a tool to read the I2C registers.

NET RULES

NET	PHYSICAL
SIIA_VCC	12MIL_TRACE
SIIA_AVCC	12MIL_TRACE
SIIA_PVCC1	12MIL_TRACE
SIIA_PVCC2	12MIL_TRACE

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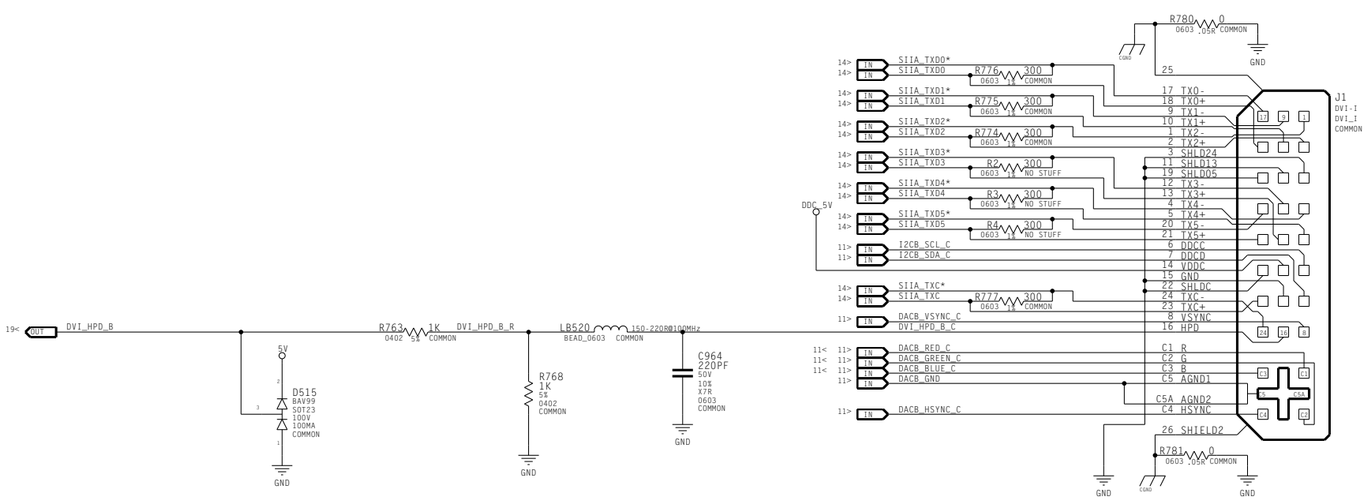
4.e. DVI-I (TMDS) Connector

(South)



NV30 GPIO's are 5V Tolerant

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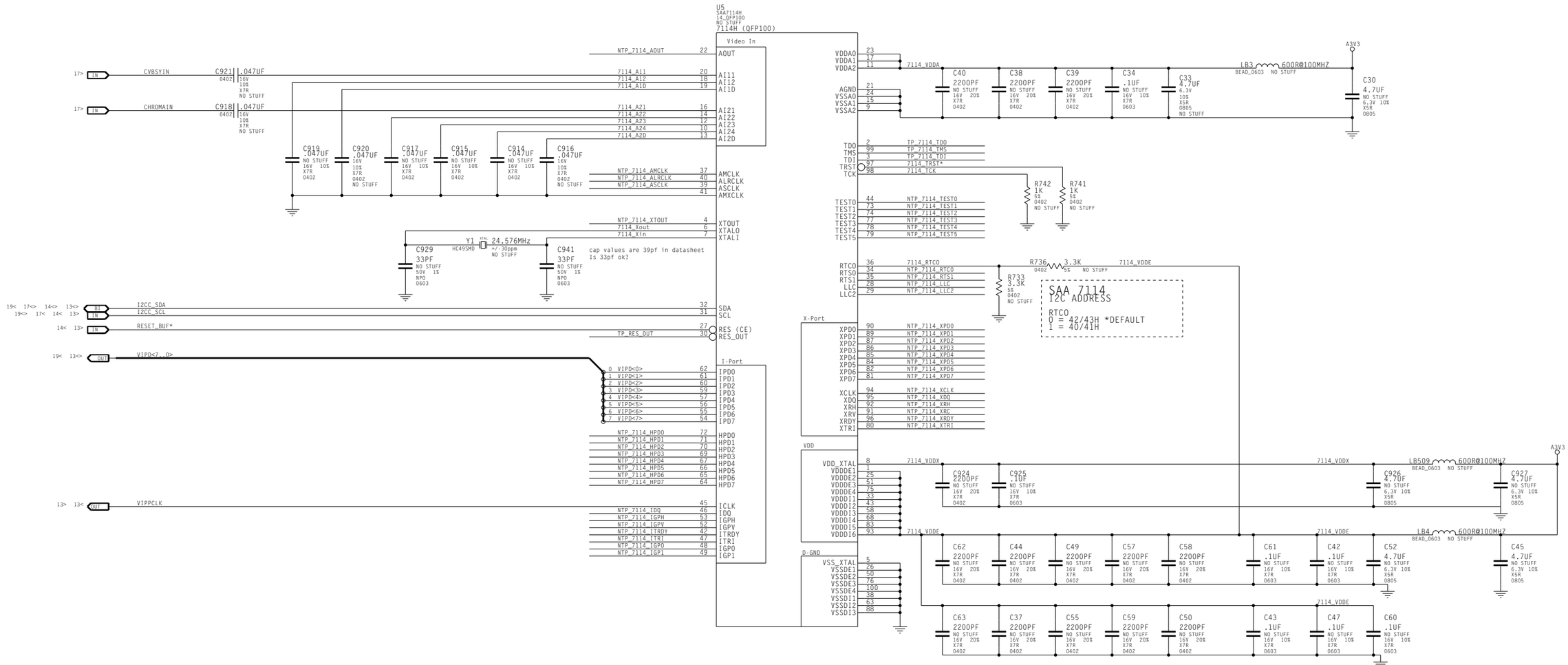
5.a. Video Capture

NET RULES

NET	PHYSICAL	VOLTAGE
7114_VDDA	12MIL_TRACE	3.3V
7114_VDDX	12MIL_TRACE	2.8V
7114_VDDE	12MIL_TRACE	3.3V

VIDEO CAPTURE



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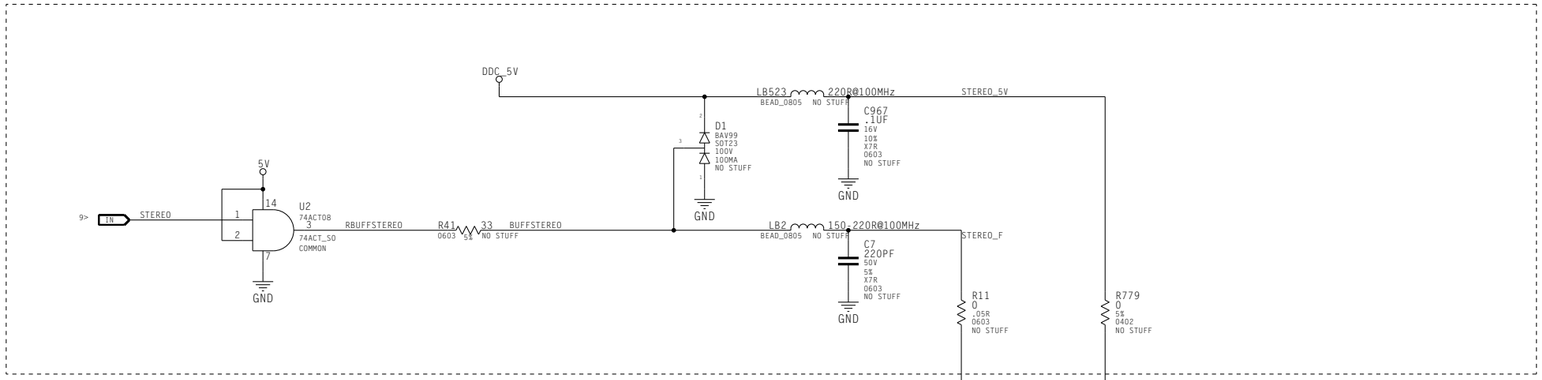
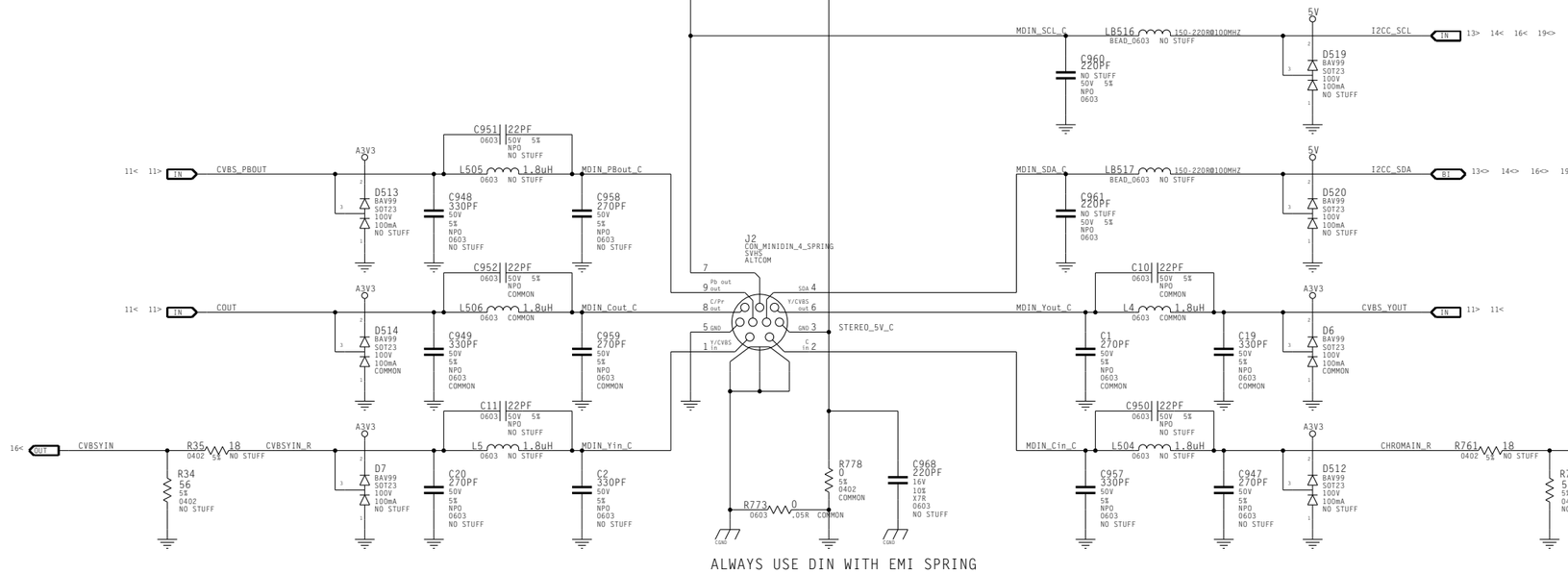
5.b. DIN Connector (TV , VIVO, STEREO)

STEREO 3D





ALWAYS USE DIN WITH EMI SPRING

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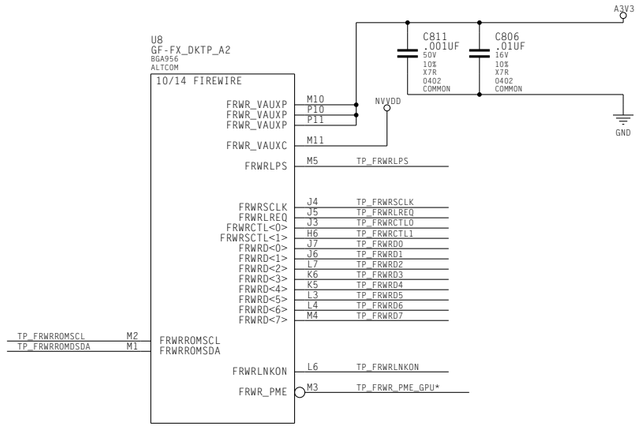
6.a. Firewire



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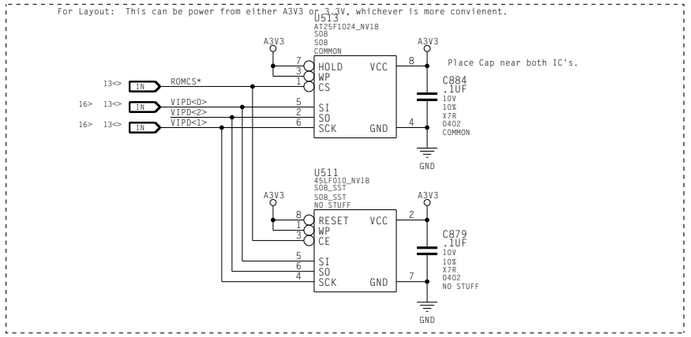
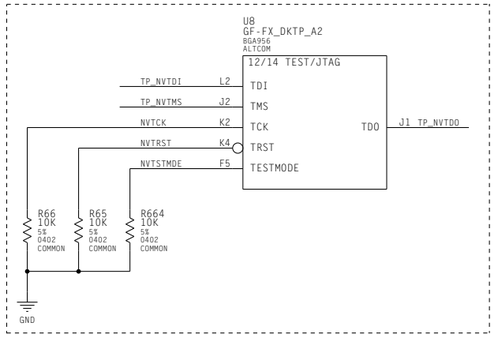
7.a. BIOS, Straps, Misc

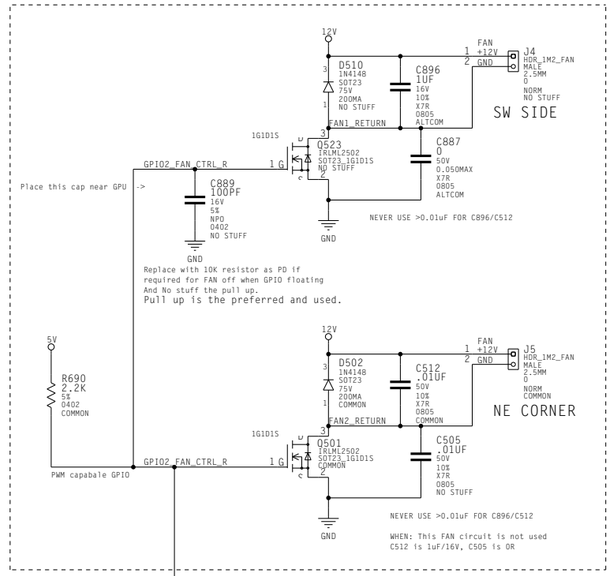
BIOS (serial)



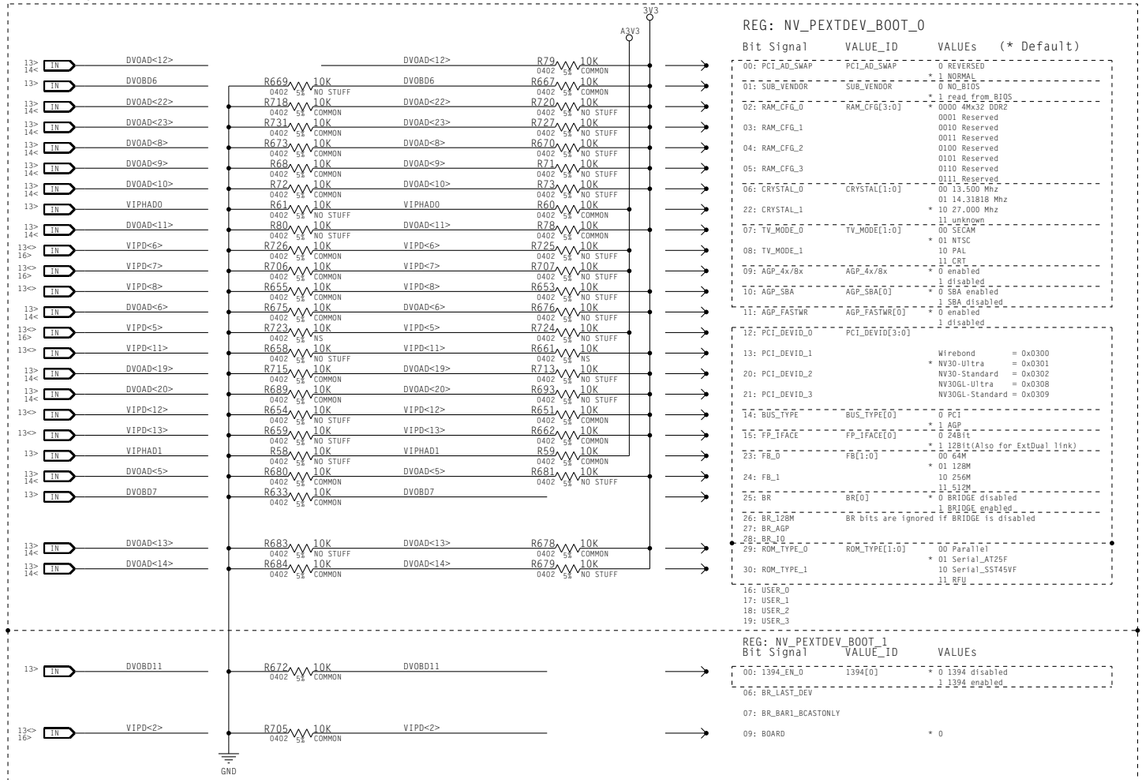
Test/JTAG



Fan1/Fan2



Straps



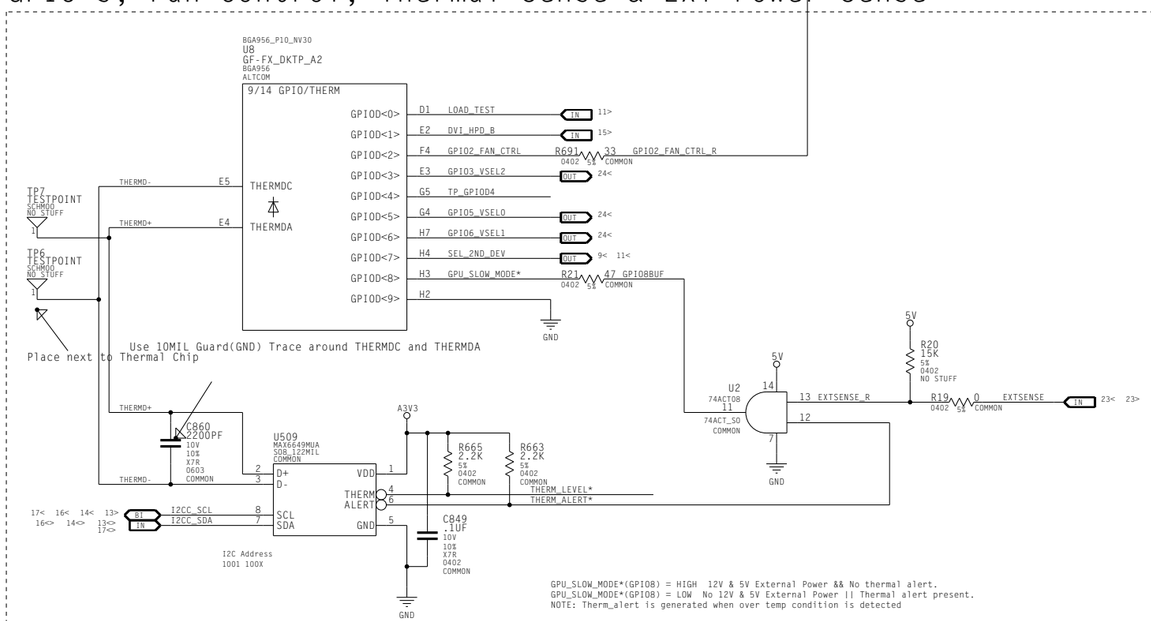
REG: NV_PEXTDEV_BOOT_0

Bit	Signal	VALUE_ID	VALUEs (* Default)
00:	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED * 1 NORMAL
01:	SUB_VENDOR	SUB_VENDOR	0 NO_BIOS * 1 read from BIOS
02:	RAM_CFG_0	RAM_CFG[3:0]	* 0000 4Mx32 DDR2 0001 Reserved 0010 Reserved 0011 Reserved
03:	RAM_CFG_1		0100 Reserved 0101 Reserved 0110 Reserved 0111 Reserved
04:	RAM_CFG_2		
05:	RAM_CFG_3		
06:	CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz 01 14.31818 Mhz * 10 27.000 Mhz 11 unknown
07:	TV_MODE_0	TV_MODE[1:0]	00 SECAM * 01 NTSC 10 PAL 11 CRT
08:	TV_MODE_1		
09:	AGP_4x/8x	AGP_4x/8x	* 0 enabled 1 disabled
10:	AGP_SBA	AGP_SBA[0]	* 0 SBA enabled 1 SBA disabled
11:	AGP_FASTWR	AGP_FASTWR[0]	* 0 enabled 1 disabled
12:	PCI_DEVID_0	PCI_DEVID[3:0]	
13:	PCI_DEVID_1		Wirebond = 0x0300 * NV30-Ultra = 0x0301
20:	PCI_DEVID_2		NV30-Standard = 0x0302 NV30GL-Ultra = 0x0308
21:	PCI_DEVID_3		NV30GL-Standard = 0x0309
14:	BUS_TYPE	BUS_TYPE[0]	0 PCI * 1 AGP
15:	FP_IFACE	FP_IFACE[0]	0 24Bit * 1 12Bit(Also for ExtDual link)
23:	FB_0	FB[1:0]	00 64M * 01 128M 10 256M 11 512M
24:	FB_1		
25:	BR	BR[0]	* 0 BRIDGE disabled 1 BRIDGE enabled
26:	BR_128M	BR bits are ignored if BRIDGE is disabled	
27:	BR_AGP		
28:	BR_IO		
29:	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel * 01 Serial_AT25F 10 Serial_SST45VF 11 RFU
30:	ROM_TYPE_1		
16:	USER_0		
17:	USER_1		
18:	USER_2		
19:	USER_3		

REG: NV_PEXTDEV_BOOT_1

Bit	Signal	VALUE_ID	VALUEs
00:	1394_EN_0	1394[0]	* 0 1394 disabled 1 1394 enabled
06:	BR_LAST_DEV		
07:	BR_BAR1_BCASTONLY		
09:	BOARD		* 0

GPIO's, Fan Control, Thermal Sense & EXT Power Sense



NET RULES

NET	PHYSICAL
THERMDC	10MIL_TRACE
THERMDA	10MIL_TRACE
FAN1_RETURN	16MIL_TRACE
FAN2_RETURN	16MIL_TRACE

NET	SPACING
GPIO2_FAN_CTRL	20MIL
GPIO2_FAN_CTRL_R	20MIL

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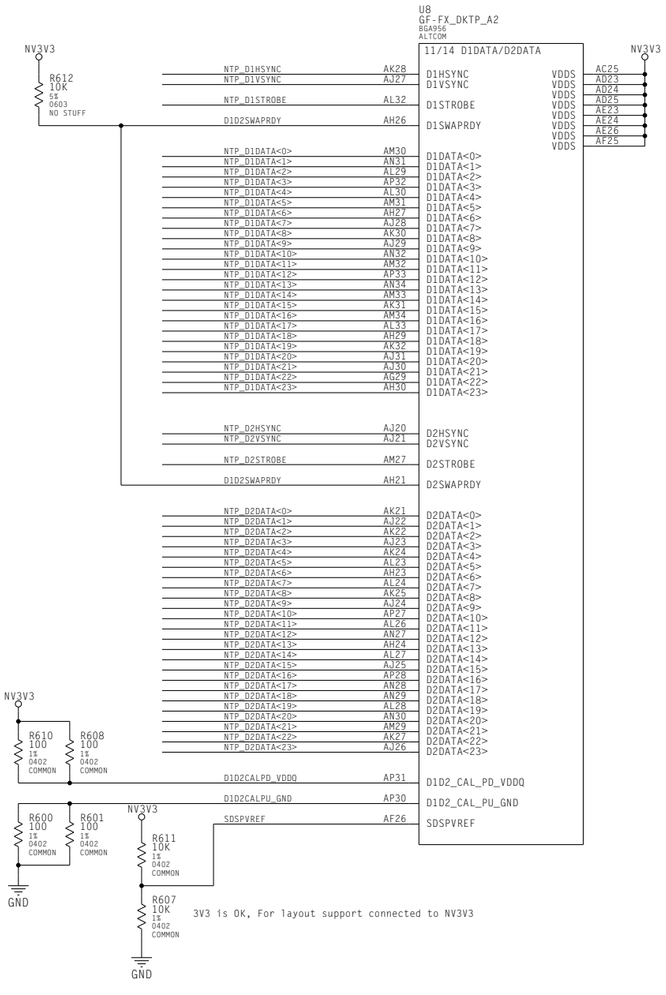
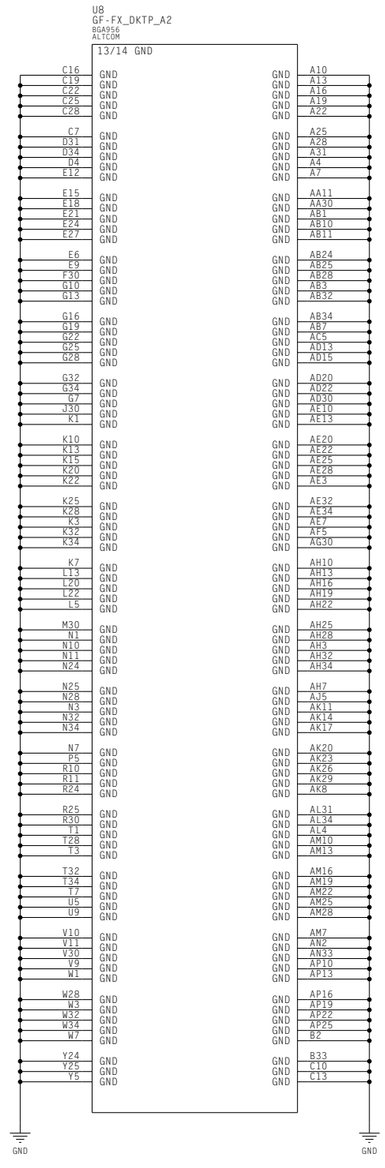
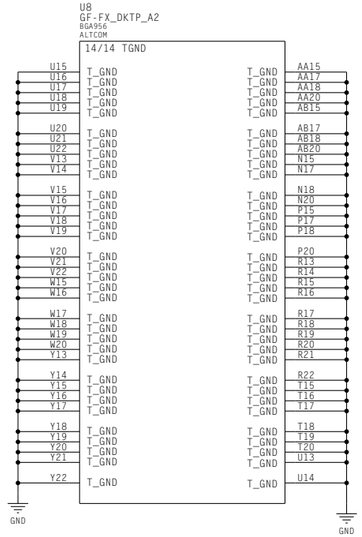
8.a. GND, Thermal GND and Misc...







NET RULES

	NET	PHYSICAL	SPACING
IN	D1D2CALPD_VDDQ	12MIL_TRACE	20MIL
IN	D1D2CALPU_GND	12MIL_TRACE	20MIL

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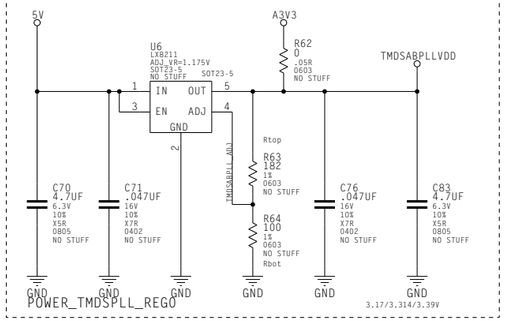
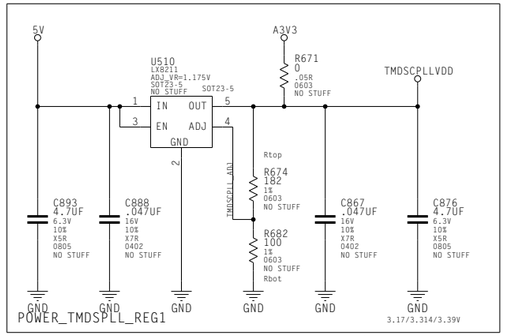
9.a. Power Supply I: TMDS/A3V3/FBVDD

TMDS AB PLL Supply



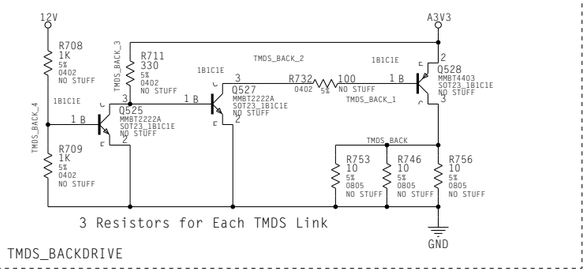
Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+(100/182))

TMDS C PLL Supply

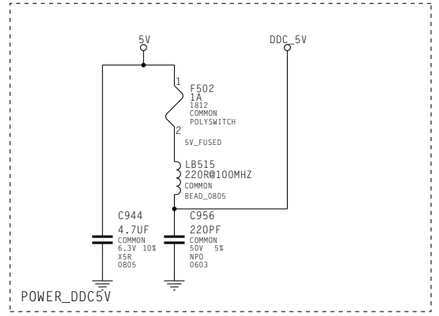


Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+(100/182))

TMDS backdrive prevention



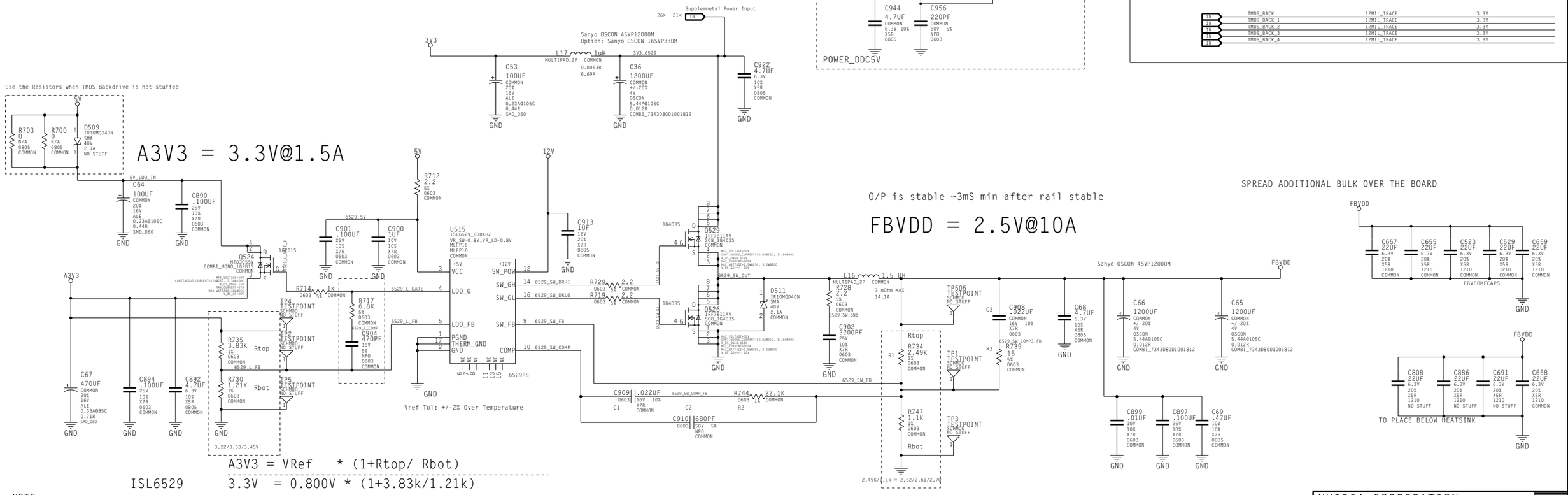
DDC 5V



NET RULES

NET	PHYSICAL	VOLTAGE
A3V3	12MIL_TRACE	3.3V
FBVTT	12MIL_TRACE	0.9V
FBVDDQ	12MIL_TRACE	1.8V
FBVDD	12MIL_TRACE	2.5V
NVVDD	12MIL_TRACE	1.2V
5V	12MIL_TRACE	5V
12V	12MIL_TRACE	12V
3V3	12MIL_TRACE	3.3V
AGPVDDQ	12MIL_TRACE	3.3V
GND	12MIL_TRACE	0V
DDC_5V	12MIL_TRACE	5V
5V_FUSED	12MIL_TRACE	5V
TMDSABPLLVDD	12MIL_TRACE	2.8V
TMDSCPLLVDD	12MIL_TRACE	2.8V
TMDSABPLL_ADJ	10MIL_TRACE	3.3V
TMDSCPLL_ADJ	10MIL_TRACE	3.3V
6529_SW_12V	10MIL_TRACE	12V
6529_5V	12MIL_TRACE	5V
3V3_6529	16MIL_TRACE	3.3V
6529_SW_OUT	16MIL_TRACE	3.3V
6529_SW_COMP	10MIL_TRACE	3.3V
6529_SW_COMP_FB	24MIL_TRACE	3.3V
6529_SW_FB	10MIL_TRACE	2.5V
6529_SW_COMP3_FB	10MIL_TRACE	3.3V
6529_SW_SNB	12MIL_TRACE	3.3V
6529_SW_DRHI	24MIL_TRACE	12V
6529_SW_DRLO	24MIL_TRACE	12V
6529_SW_GH	24MIL_TRACE	12V
6529_SW_GL	24MIL_TRACE	12V
6529_L_GATE	16MIL_TRACE	5V
6529_L_GATE_R	16MIL_TRACE	5V
6529_VDD_FB	10MIL_TRACE	2.5V
6529_GND_FB	10MIL_TRACE	3.3V
5V_LDO_IN	16MIL_TRACE	5V
6529_L_COMP	10MIL_TRACE	3.3V
6529_L_FB	10MIL_TRACE	3.3V
TMDS_BACK	12MIL_TRACE	3.3V
TMDS_BACK_1	12MIL_TRACE	3.3V
TMDS_BACK_2	12MIL_TRACE	3.3V
TMDS_BACK_3	12MIL_TRACE	3.3V
TMDS_BACK_4	12MIL_TRACE	3.3V

FBVDD-SWITCHER / A3V3-LDO CONTROLER ISL6529



NOTE

5V external Supplemental power to 3.3V is for FBVDD,See other page
For voltage Shmoo, the Rtop reistor value should not be changed more than 10%
Please contact design team to check the compensation circuit analysis

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9.b. Power Supply II: FBVDDQ/FBVTT

NET RULES

NET	PHYSICAL	VOLTAGE
6225_VCC	12MIL_TRACE	5V
6225_PHASE1	12MIL_TRACE	5V
6225_PHASE2	12MIL_TRACE	5V
6225_UGATE1	12MIL_TRACE	5V
6225_UGATE2	12MIL_TRACE	5V
6225_LGATE1	12MIL_TRACE	3.3V
6225_LGATE2	12MIL_TRACE	3.3V
VDDQ_VSEN	10MIL_TRACE	3.3V
6225_BOOT1	10MIL_TRACE	3.3V
6225_BOOT2	10MIL_TRACE	3.3V
6225_ISEN1	10MIL_TRACE	3.3V
6225_ISEN2	10MIL_TRACE	3.3V
VDDQ_OCSET	10MIL_TRACE	3.3V
VTTREF_IN	10MIL_TRACE	3.3V
VTT_SNB	10MIL_TRACE	0.9V
FBVDDQ_SNB	10MIL_TRACE	1.8V

NOTE:
For 5V(AGP) operation the MCLK is limited to 5V AGP i/p current.
With 5V_Ext(HDD Con): The MCLK is limited to PS output current and board thermal capabilities

NOTE: No FUSE protection for AGP5V

Turnoff: ~40nS for Vth of 1V.min

Vth= 1V/1.8/3.0V

Sanyo OSCON 6SVPB2OM for 10A o/p Ct.
042-50827-0037-014

FBVDDQmax = 2.5V@10A

FBVDDQ
Vout1 = VRef * (1+Rtop/Rbot)
1.8V = 0.9V * (1+(10K/10K))

MLCC 039-70107-0037-000

O/P is stable ~180mS min after rail stable

Falco SDQIE1007-477
131-10472-0011-000

2.05K/1.15K = 2.448/2.504/2.562

Hys Mode

CCM Mode(Default)

Set VTT Voltage in DDR Mode

EXTERNAL VTT REF OPTION (Default)

FBVTT
Vout2 = Vout1/2
0.9V = 1.8V/2

FBVTT = 0.9V@4A

Sanyo OSCON 2R5SVP15000M

PLACE NEAR GPU AREA

Vref Tol: +/-1% Over Temperature

Place close to pin 18

INTERNAL VTT REF OPTION
(TO BE TESTED)

NO_STUFF for No power sequencing

NOTE

For Shmoo to change the o/p voltage adjust the FBVDDQ and VTT levels independently

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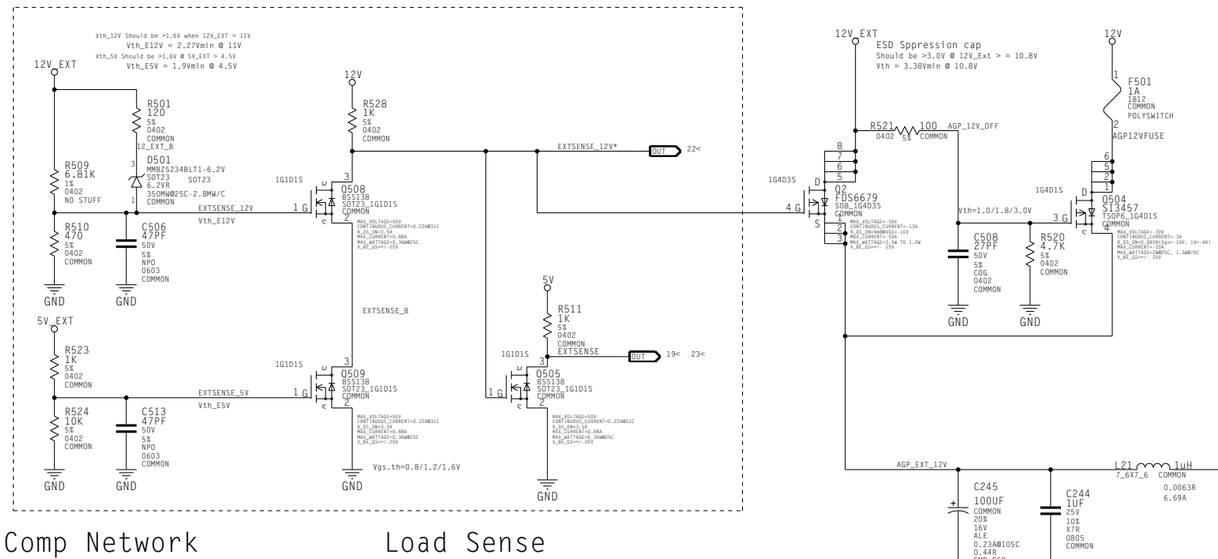
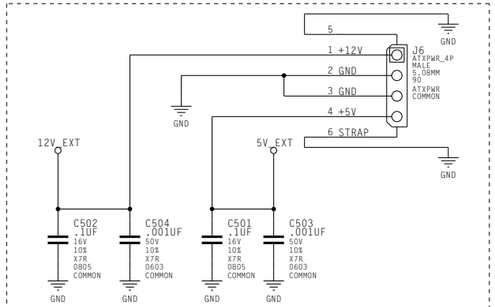
9.c. Power Supply III: NVVDD

For 12V(AGP) operation the NVCLK is limited to 12V AGP i/p current.
With 12V_Ext(HDD Con): The NVCLK is limited PS output current and board thermal capabilities

External Power Sense



External Power Connector

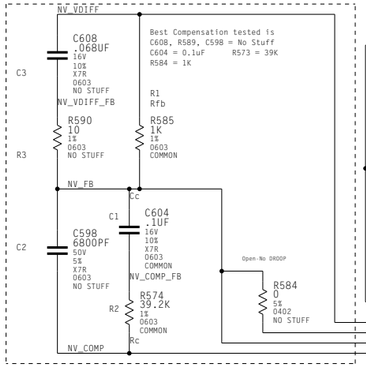


NET RULES

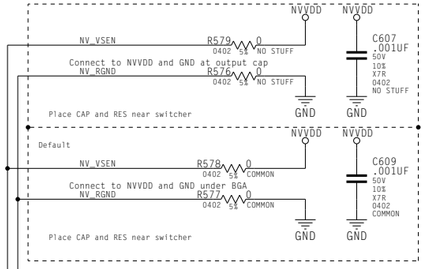
	NET	PHYSICAL	VOLTAGE
5V_EXT	5V_EXT	60MIL_TRACE	5V
12V_EXT	12V_EXT	60MIL_TRACE	12V
IN	NV_12V_IN	30MIL_TRACE	12V
IN	AGP12VFUSE	20MIL_TRACE	12V
23> 19< IN	EXTSENSE	5MIL_TRACE	3.3V
IN	NV_PHASE1	12MIL_TRACE	1.2V
IN	NV_PHASE2	12MIL_TRACE	1.2V
IN	NV_VCC	12MIL_TRACE	5V
IN	NV_BOOT1	10MIL_TRACE	3.3V
IN	NV_BOOT2	10MIL_TRACE	3.3V
IN	NV_COMP	10MIL_TRACE	3.3V
IN	NV_COMP_FB	10MIL_TRACE	3.3V
IN	NV_FB	10MIL_TRACE	3.3V
IN	NV_PWM1	10MIL_TRACE	3.3V
IN	NV_PWM2	10MIL_TRACE	3.3V
IN	NV_VDIFF	10MIL_TRACE	3.3V
24> 23< IN	NV_OFS	10MIL_TRACE	3.3V
IN	NV_ISEN1	10MIL_TRACE	3.3V
IN	NV_ISEN2	10MIL_TRACE	3.3V
IN	PH1_SNB	10MIL_TRACE	1.2V
IN	PH2_SNB	10MIL_TRACE	1.2V
IN	NV_UGATE1	24MIL_TRACE	12V
IN	NV_UGATE2	24MIL_TRACE	12V
IN	NV_UGATE1_R	24MIL_TRACE	12V
IN	NV_UGATE2_R	24MIL_TRACE	12V
IN	NV_LGATE1	24MIL_TRACE	12V
IN	NV_LGATE2	24MIL_TRACE	12V
IN	NV_LGATE1_R	24MIL_TRACE	12V
IN	NV_LGATE2_R	24MIL_TRACE	12V

	NET	DIFFPAIR	PHYSICAL
IN	NV_VSEN	NV_REM_SENSE	10MIL_TRACE
IN	NV_RGND	NV_REM_SENSE	10MIL_TRACE

Comp Network



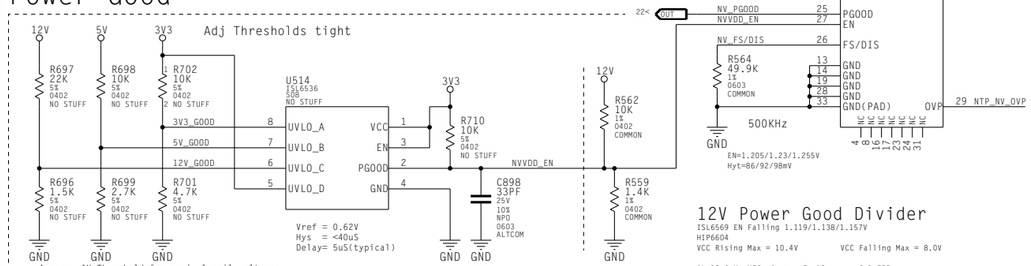
Load Sense



NVVDD Voltage Select

Vref Tol: +/-1% over Temperature
Dynamic VID o/p rate = 25mV/(2 * 1/Freq)
SoftStart-stable o/p Delay = 2048/Freq

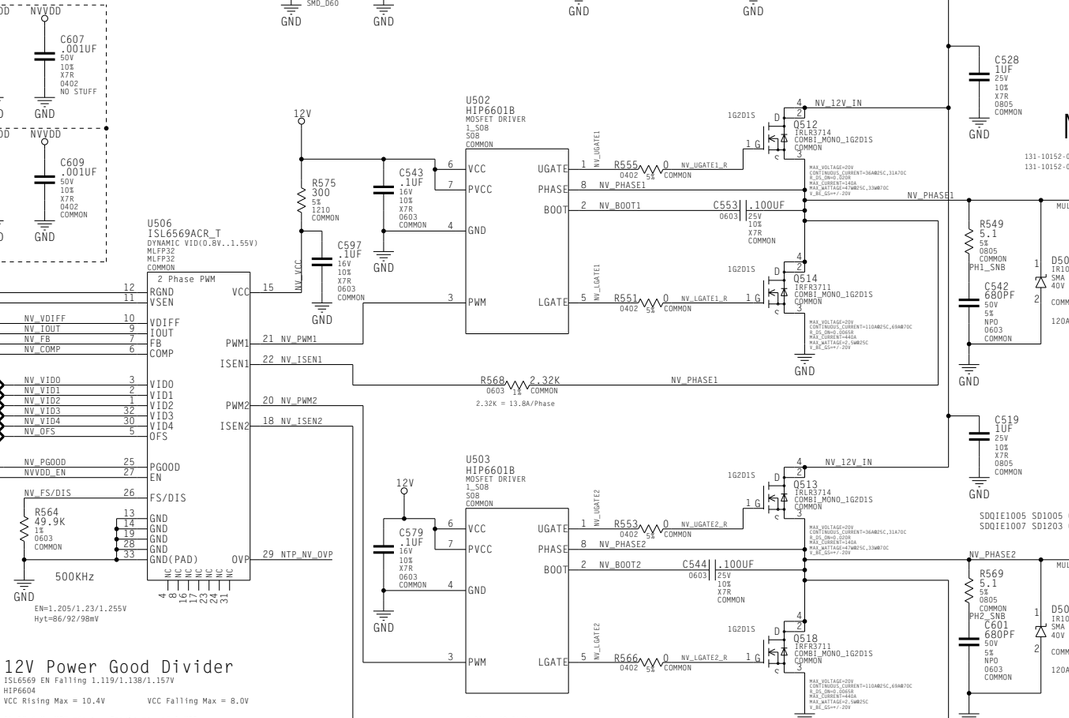
Power Good



12V Power Good Divider

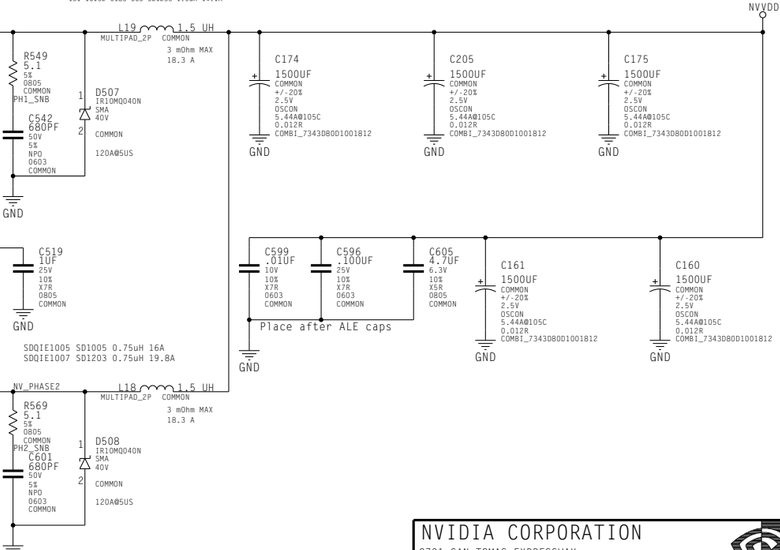
ISL6569 EN Falling 1.119/1.138/1.157V
HIP6604
VCC Rising Max = 10.4V VCC Falling Max = 8.0V

At 10.4 V, VR2.min > = Enable max of 1.255
At 8.0V VR2.max < Minimum of Enable falling threshold 1.119
The AGP12V rail of 10.4V is arrived by
12V - 5% - 500mV Noise - 500mV Guard



NVVDD = 0.8V..1.50V (25A)

131-10152-0153-006 SD1207 1.5uH 14.6A-Default
131-10152-0183-003 SD1233 1.5uH 14.1A



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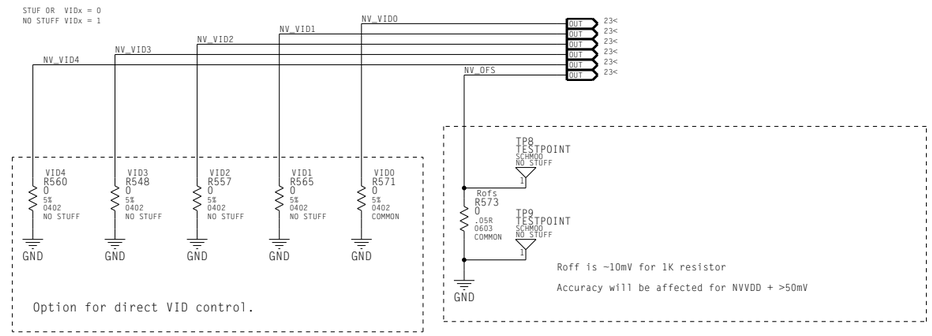
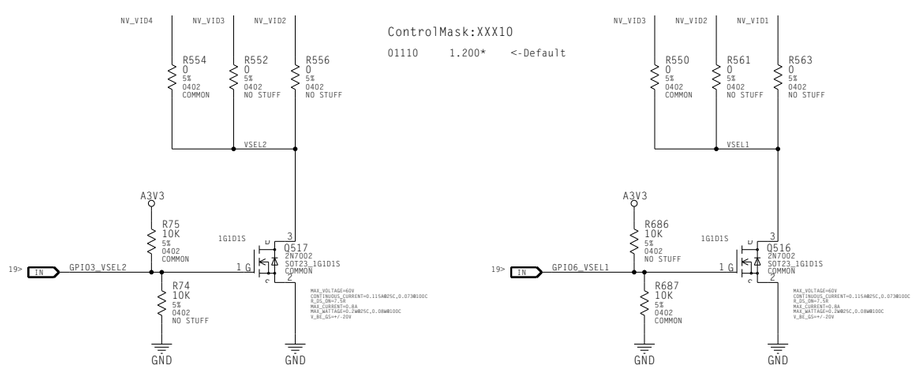
9.d. Power Supply III: NVVDD Voltage Select Options

ISL6569
5-Bit VID Table

	VID[4:0]	VOLTAGE	VID[4:0]	VOLTAGE
	00000	1.550	10000	1.150
	00001	1.525	10001	1.125
	00010	1.500*	10010	1.100*
	00011	1.475	10011	1.075
	00100	1.450	10100	1.050
	00101	1.425	10101	1.025
	00110	1.400*	10110	1.000*
	00111	1.375	10111	0.975
	01000	1.350	11000	0.950
	01001	1.325	11001	0.925
	01010	1.300*	11010	0.900*
	01011	1.275	11011	0.875
	01100	1.250	11100	0.850
	01101	1.225	11101	0.825
Default->	01110	1.200*	11110	0.800*
	01111	1.175	11111	Shutdown

Table is with Roffset= OR
* SELECTABLE





Pullup not necessary to be A3V3, Can be AGP3V3.

*NOTE: GPIO usages changes on P126-A05 and onward due to added N-CH MOSFETs

Tri State ALL GPIOs When default voltage is required.

When GPIO = 1 then VID = 0
When GPIO = 0 then VID = 1

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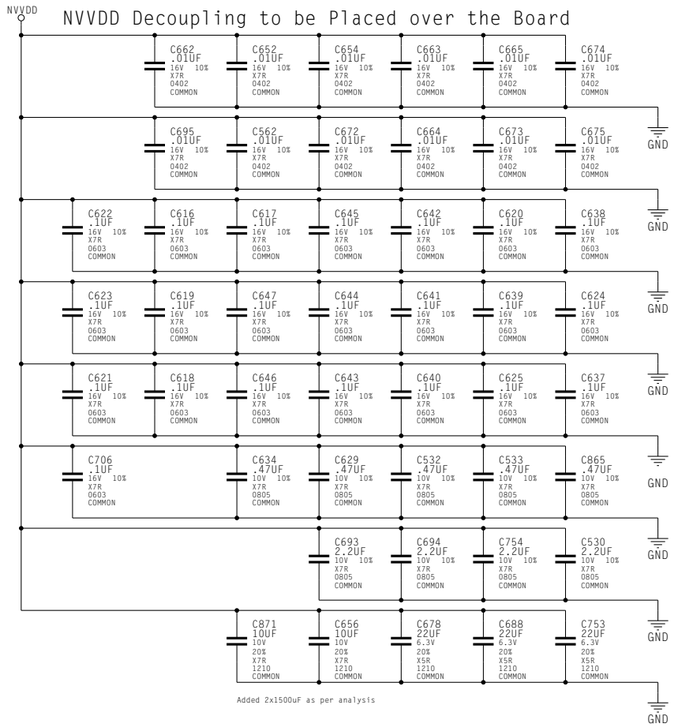
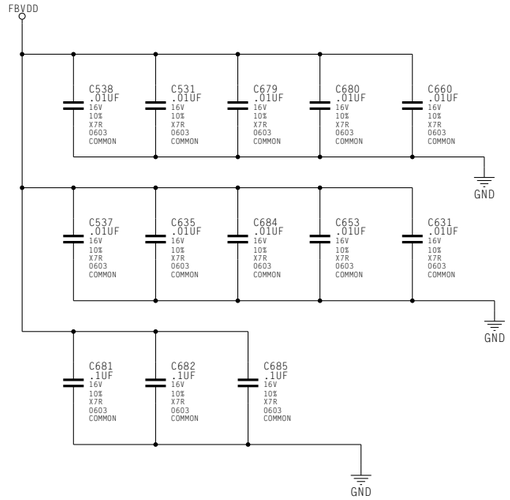
9.E. Additional Decoupling





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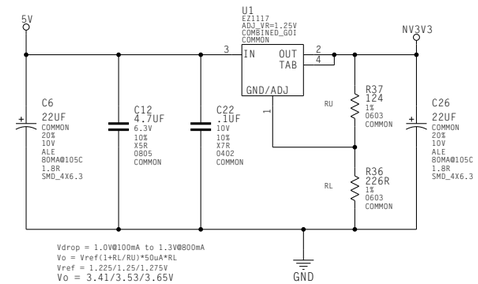
9.f.FBVDD Current Supplement & NV3V3

GPU 3.3V REGULATOR

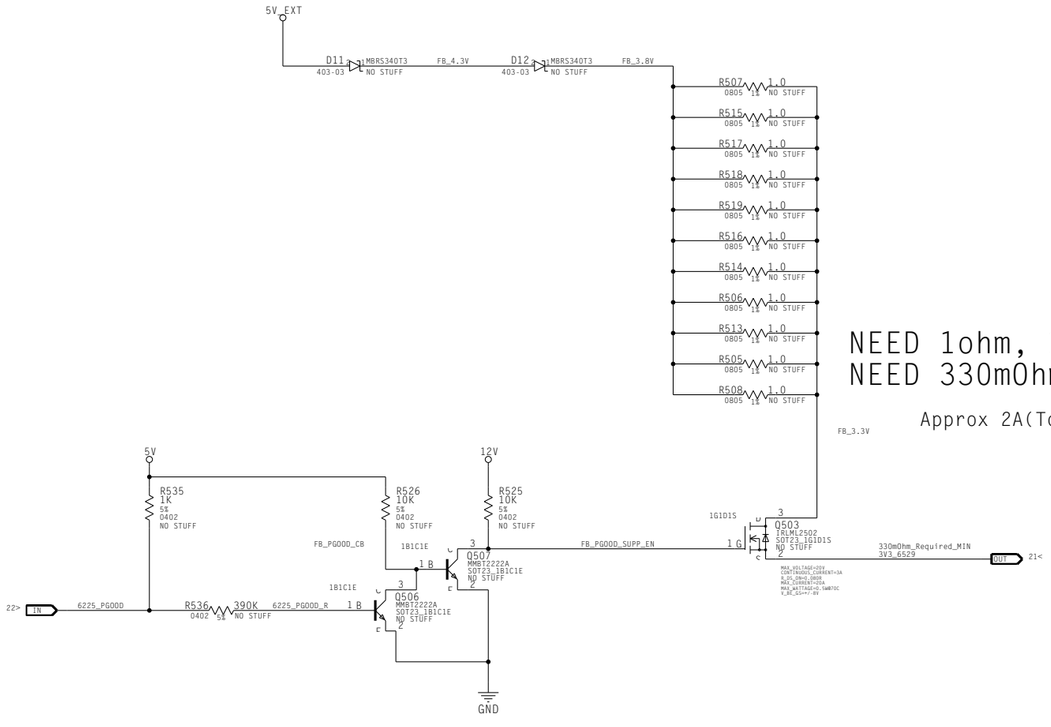
For Better Drive Bias to Frame Buffer

3.5V, 500mA



Vdrop = 1.0V@100mA to 1.3V@800mA
Vo = Vref(1+RL/RU)*50uA*RL
Vref = 1.225/1.25/1.275V
Vo = 3.41/3.53/3.65V

NEVER USE THIS CIRCUIT



NEED 1ohm, 10nos/0805
NEED 330mOhm trace resistance

Approx 2A(To be decied)

This circuit will be enabed after 180mS minimum after NVVDD

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10.a.Mechanical

151-10000-0021-000-STDVGA-DIN-DVI
151-10000-5004-000-DualWide-VGA-DIN-DVI

BKT1
DS15HD, MDIN, DVI, NO TAB
ATX_1X_NO
NO STUFF
BRKT_ADVI_BDIN9_CDB15

FootPrint:BRKT_ADVI_BDIN9_CDB15

FX FLOW(NVTM2) FANSINK ASSY KIT

095-20000-0001-000

MEC1
HEX_JACK_SCREW
STD
COMMON

MEC2
HEX_JACK_SCREW
STD
COMMON

2 for VGA

MEC3
HEX_JACK_SCREW
STD
COMMON

MEC4
HEX_JACK_SCREW
STD
COMMON

2 for DVI-I

SCREW PARTS- 155-00003-0000-000
or 155-00005-0000-000

MEC5
HEX_JACK_SCREW
STD
NO STUFF

1 for 2nd Slot open

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*** Signal Cross-Reference for the entire design ***

3V3_6529	21< 26>
5V_FUSED	21<
5V_LDO_IN	21<
6225_BOOT1	22<
6225_BOOT2	22<
6225_ISEN1	22<
6225_ISEN2	22<
6225_LGATE1	22<
6225_LGATE2	22<
6225_PGOOD	22> 26<
6225_PHASE1	22<
6225_PHASE2	22<
6225_UGATE1	22<
6225_UGATE2	22<
6225_VCC	22<
6529_5V	21<
6529_GND_FB	21<
6529_L_COMP	21<
6529_L_FB	21<
6529_L_GATE	21<
6529_L_GATE_R	21<
6529_SW_12V	21<
6529_SW_COMP	21<
6529_SW_COMP3_FB	21<
6529_SW_COMP_FB	21<
6529_SW_DRHI	21<
6529_SW_DRLO	21<
6529_SW_FB	21<
6529_SW_GH	21<
6529_SW_GL	21<
6529_SW_OUT	21<
6529_SW_SNB	21<
6529_VDD_FB	21<
7114_VDDA	16<
7114_VDDE	16<
7114_VDDX	16<
AGP12VFUSE	23<
AGPADSTBF0	3<
AGPADSTBF1	3<
AGPADSTBS0	3<
AGPADSTBS1	3<
AGPCALPD_VDDQ	3<
AGPCALPU_GND	3<
AGPDBI_HI	3<
AGPDBI_LO	3<
AGPMBDET	3<
AGPRBF	3<
AGPSBA<0>	3<
AGPSBA<7..0>	3<
AGPSBA<1>	3<
AGPSBA<2>	3<
AGPSBA<3>	3<
AGPSBA<4>	3<
AGPSBA<5>	3<
AGPSBA<6>	3<
AGPSBA<7>	3<
AGPSBSTBF	3<
AGPSBSTBS	3<
AGPSTO	3<
AGPST1	3<
AGPST2	3<
AGPSTOP	3<
AGPVREFCG	3<
AGPVREFCG_GPU	3<
AGPVREFGC	3<
AGPWBF	3<
CHROMAIN	16< 17>
COUT	11> 11< 17<
CVBSYIN	16< 17>
CVBS_PBOUT	11> 11< 17<
CVBS_YOUT	11> 11< 17<
D1DZCALPD_VDDQ	20<
D1DZCALPU_GND	20<
DACA_BLUE	9> 10<
DACA_BLUE_C	10<
DACA_BLU_GND	10<
DACA_GREEN	9> 10<
DACA_GREEN_C	10<
DACA_GRN_GND	10<
DACA_HSYNC_BUF	9> 10<
DACA_RED	9> 10<
DACA_RED_C	10<
DACA_RED_GND	10<
DACA_RSET	9<
DACA_VDD	9<
DACA_VREF	9<
DACA_VSYNC_BUF	9> 10<
DACB_BLUE	9> 11<
DACB_BLUE_C	11> 11< 15<
DACB_BLUE_SW	11<
DACB_GND	11> 15<
DACB_GREEN	9> 11<
DACB_GREEN_C	11> 11< 15<
DACB_GREEN_SW	11<
DACB_HSYNC_BUF	9> 11<
DACB_HSYNC_C	11> 15<
DACB_RED	9> 11<
DACB_RED_C	11> 11< 15<
DACB_RED_SW	11<
DACB_RSET	9<
DACB_VDD	9<
DACB_VREF	9<
DACB_VSYNC_BUF	9> 11<
DACB_VSYNC_C	11> 15<
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DVOACLKOUT	13< 13> 14<
DVOACLKOUT*	13> 14<
DVOACLKOUT_R	13<
DVOAD<0>	13> 14<
DVOAD<11..0>	13> 14< 19<
DVOAD<23..0>	13> 14< 19<

DVOAD<1>	13> 14<
DVOAD<2>	13> 14<
DVOAD<3>	13> 14<
DVOAD<4>	13> 14<
DVOAD<5>	13> 14< 19<
DVOAD<6>	13> 14< 19<
DVOAD<7>	13> 14<
DVOAD<8>	13> 14< 19<
DVOAD<9>	13> 14< 19<
DVOAD<10>	13> 14< 19<
DVOAD<11>	13> 14< 19<
DVOAD<12>	13> 14< 19<
DVOAD<23..12>	13> 14< 19<
DVOAD<13>	13> 14< 19<
DVOAD<14>	13> 14< 19<
DVOAD<15>	13> 14<
DVOAD<16>	13> 14<
DVOAD<17>	13> 14<
DVOAD<18>	13> 14<
DVOAD<19>	13> 14< 19<
DVOAD<20>	13> 14< 19<
DVOAD<21>	13> 14<
DVOAD<22>	13> 14< 19<
DVOAD<23>	13> 14< 19<
DVOADE	13> 14<
DVOAHSYNC	13> 14<
DVOAVSYNC	13> 14<
DVOBD6	13> 19<
DVOBD7	13> 19<
DVOBDI1	13> 19<
EXTSENSE	19< 23< 23>
EXTSENSE_12V*	22< 23>
FAN1_RETURN	19<
FAN2_RETURN	19<
FBAA<0>	4> 4< 5< 7<
FBAA<12..0>	4> 4< 5< 7<
FBAA<1>	4> 4< 5< 7<
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DETAIL	DRAWING DETAIL CONTINUED...		
ID	p126_a05_sch	PAGE	28 OF 32
NAME	140-10126-000-005-X13	DATE	FEB-14-2003

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DETAIL	DRAWING DETAIL CONTINUED...		
ID	p126_a05_sch	PAGE	29 OF 32
NAME	140-10126-000-005-X13	DATE	FEB-14-2003

*** Part Cross-Reference for the entire design ***

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R694	R	13
R695	R	13
R696	R	23
R697	R	23
R698	R	23
R699	R	23
R700	R	21
R701	R	23
R702	R	23
R703	R	21
R704	R	13
R705	R	19
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R710	R	23
R711	R	21
R712	R	21
R713	R	19
R714	R	21
R715	R	19
R716	R	9
R717	R	21
R718	R	19
R719	R	21
R720	R	19
R721	R	13
R722	R	13
R723	R	19
R724	R	19
R725	R	19
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R728	R	21
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R731	R	19
R732	R	21
R733	R	16
R734	R	21
R735	R	21
R736	R	16
R737	R	9
R738	R	14
R739	R	21
R740	R	9
R741	R	16
R742	R	16
R743	R	14
R744	R	21
R745	R	14
R746	R	21
R747	R	21
R748	R	9
R749	R	14
R750	R	9
R751	R	14
R752	R	14
R753	R	21
R754	R	14
R755	R	14
R756	R	21
R757	R	14
R758	R	11
R759	R	14
R760	R	17
R761	R	17
R762	R	10
R763	R	15
R764	R	10
R765	R	11
R766	R	13
R767	R	13
R768	R	15
R769	R	11
R770	R	11
R771	R	11
R772	R	11
R773	R	17
R774	R	15
R775	R	15
R776	R	15
R777	R	15
R778	R	17
R779	R	17
R780	R	15
R781	R	15
TP1	TESTPOINT	21
TP2	TESTPOINT	21
TP3	TESTPOINT	21
TP4	TESTPOINT	21
TP5	TESTPOINT	21

TP6	TESTPOINT 19
TP7	TESTPOINT 19
TP8	TESTPOINT 24
TP9	TESTPOINT 24
TP501	TESTPOINT 22
TP502	TESTPOINT 22
TP503	TESTPOINT 22
TP504	TESTPOINT 22
TP505	TESTPOINT 21
U1	U_VREG_3PIN 26
U2	U_AND_2IN 9 17 19
U3	U_SW_ANA_3257 11
U4	U_PNLNK_SI11XX 14
U5	U_VDEC_SAA71XX 16
U6	U_VREG_5PIN 21
U7	U_MEM_SD_DDR2_4MX32 6
U8	U_GPU_NV3O 3 4 9 12 13 18 19 20
U9	U_MEM_SD_DDR2_4MX32 6
U10	U_MEM_SD_DDR2_4MX32 5
U11	U_MEM_SD_DDR2_4MX32 5
U501	U_SWREG_ISL6225 22
U502	U_SWREG_HIP66OX 23
U503	U_SWREG_HIP66OX 23
U504	U_MEM_SD_DDR2_4MX32 7
U505	U_MEM_SD_DDR2_4MX32 7
U506	U_SWREG_ISL6569 23
U507	U_MEM_SD_DDR2_4MX32 8
U508	U_MEM_SD_DDR2_4MX32 8
U509	U_TEMP_AD1032 19
U510	U_VREG_5PIN 21
U511	U_MEM_FL_SER_128KX8 19
U512	U_VREG_5PIN 13
U513	U_MEM_FL_SER_128KX8 19
U514	U_PGOOD_ISL6536 23
U515	U_SWREG_ISL6529 21
U516	U_AND_2IN 9
U517	U_PNLNK_SI11XX 14
Y1	XTAL 16
Y2	XTAL_4PIN 9

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