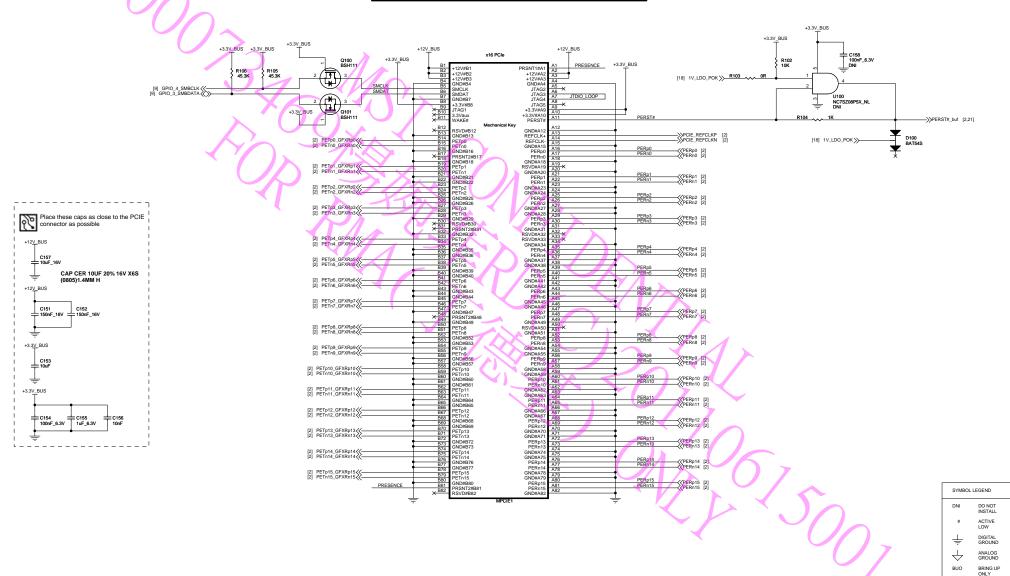
PCI-EXPRESS EDGE CONNECTOR

PCIe RESET Buffered



CONFIDENTIAL & PROPRIETANY TO ADVANCED MCRD DEACES INC.

1 Death Advanced from Deaker

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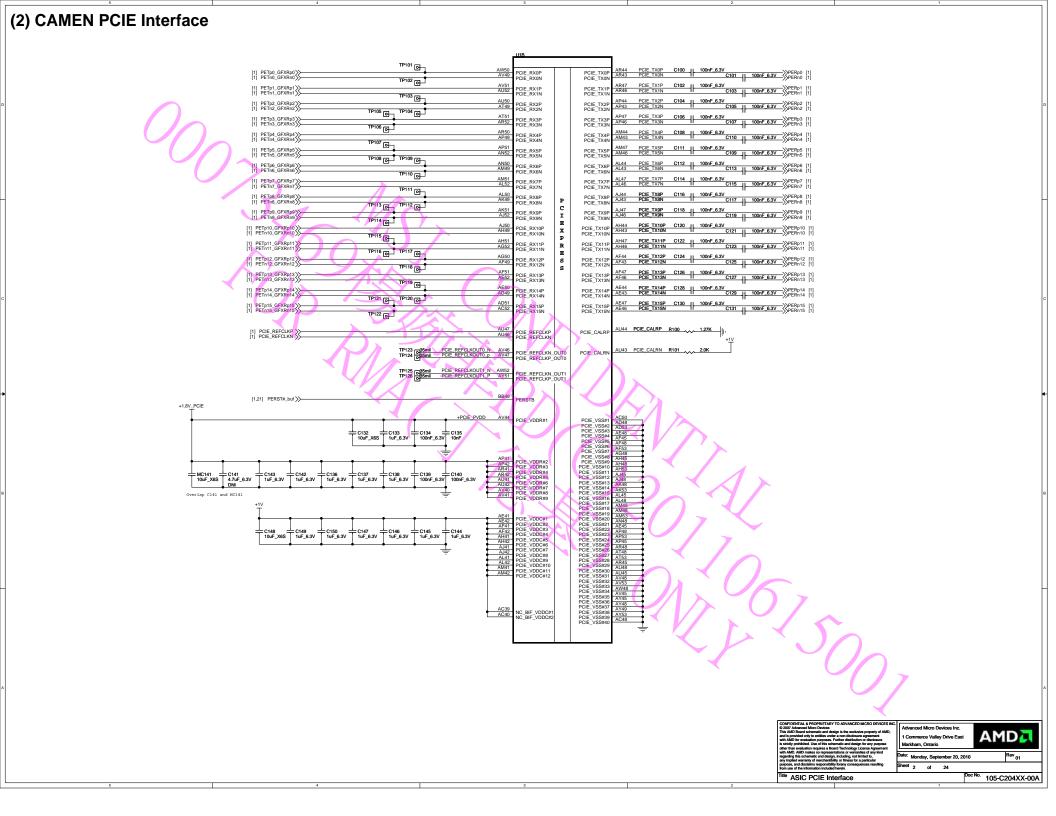
with ARID Several Internet in an office of Internet in Advanced Micro Devices Inc.

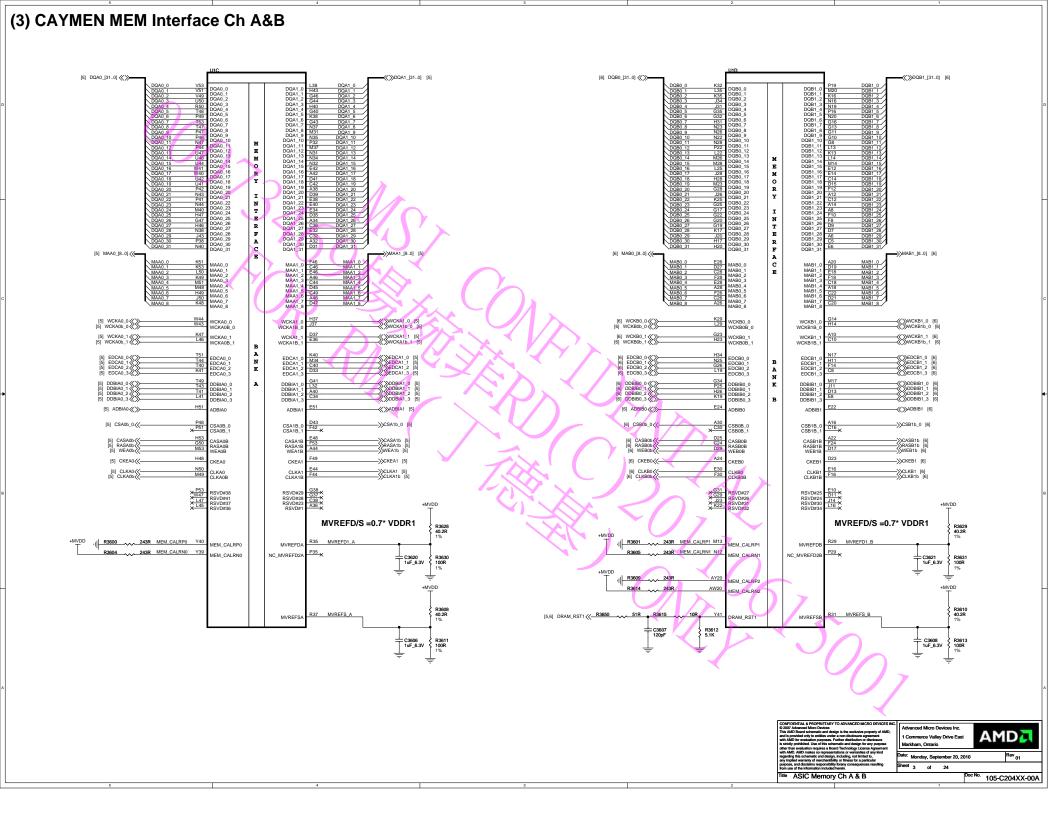
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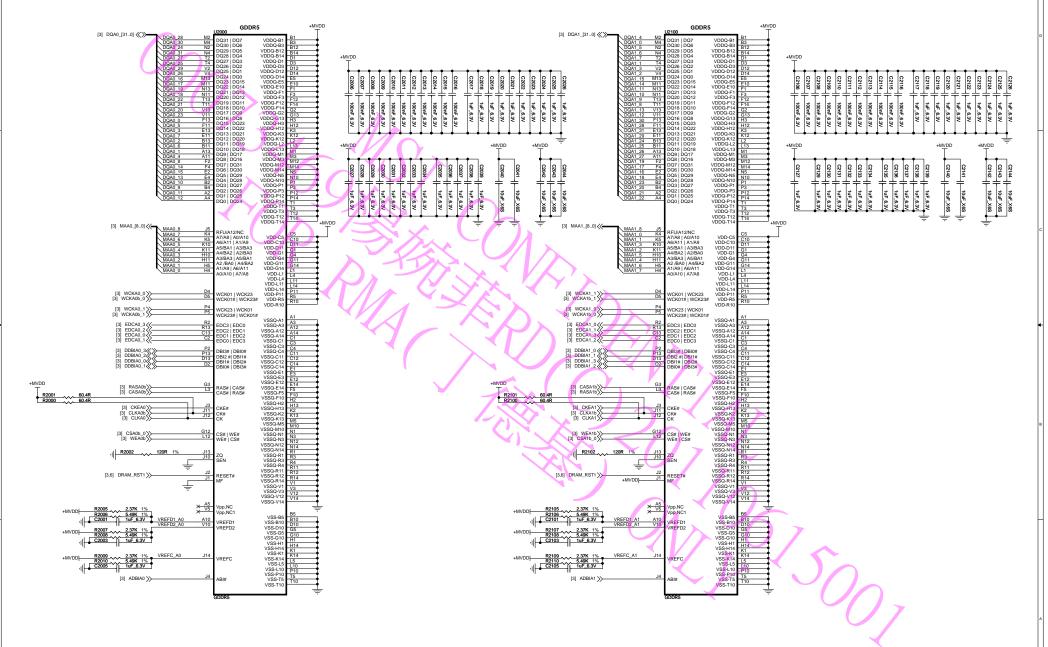
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(4) CAYMEN MEM Interface Ch C&D [7] DQC0_[31..0] 《>>= DQC1_[31..0] [7] [8] DQD0_[31..0] 《>>-✓ >>DQD1_[31..0] [8] DQD0_0 DQD0_1 DQD0_2 DQD0_3 DQD0_4 DQD0_5 DQD0_6 DQD0_7 DQD0_8 DQD0_8 DQD0_10 DQD0_110 DQD0_12 DQD0_13 DQD0_14 DQD0_15 DQD0_15 DQD0_17 DQD0_18 M O R Y M E M O R OQC0 12 I N T E R DQD0_19 DQD0_20 DQD0_21 DQD0_22 DQD0_23 DQD0_25 DQD0_25 DQD0_27 DQD0_28 DQD0_27 DQD0_28 DQD0_29 DQD0_31 DQC0 19 DQC0 20 DQC0 21 DQC0 23 DQC0 24 DQC0 25 DQC0 25 DQC0 27 DQC0 27 DQC0 28 DQC0 29 N T E R F A C A C E DQC0_31 DQD1_3 [7] MACO_[8..0] <<= [8] MAD0_[8..0] <<= MAD0_0 MAD0_1 MAD0_2 MAD0_3 MAD0_4 MAD0_5 MAD0_6 MAD0_7 MAD0_8 MAD1_0 MAD1_1 MAD1_2 MAD1_3 MAD1_4 MAD1_5 MACO_0 MACO_1 MACO_2 MACO_3 MACO_4 MACO_5 MACO_6 MACO_7 MACO_8 MAD1 [8] WCKD0_0 WCKC1_0 [7] WCKC1b_0 [7] WCKC1_ WCKC1B_ A N K EDCC0 0 EDCD0 0 EDCC0_1 EDCC0_2 EDCC0_3 EDCD0_1 EDCD0_2 EDCD0_3 c [7] DDBIC0_0 [7] DDBIC0_1 [7] DDBIC0_2 [7] DDBIC0_3 DDBIC1_0 [7] DDBIC1_1 [7] DDBIC1_2 [7] DDBIC1_3 [7] [8] DDBID0_0 [8] DDBID0_1 [8] DDBID0_2 [8] DDBID0_3 DDBID1_0 [8] DDBID1_1 [8] DDBID1_2 [8] DDBID1_3 [8] DDBICO_0 DDBICO_1 DDBICO_3 DDBICO_3 DDBIDO_0 DDBIDO_1 DDBIDO_3 DDBIDO_3 [7] ADBIC0 ≪≫ -≪≫ADBIC1 [7] [8] ADBID0 << >> ADBID0 √ ADBID1 [8] ADBIC0 ADBIC ADBID CSC0B_0 CSC0B_1 ->>CSC1b_0 [7] CSD0B_0 CSD0B_1 ->>CSD1b_0 [8] CSC1B_ CSC1B_ [7] CASC0b ([7] RASC0b ([7] WEC0b (CASCOB RASCOB WECOB ->>CASC1b [7] ->>RASC1b [7] ->>WEC1b [7] ->>CASD1b [8] ->>RASD1b [8] ->>WED1b [8] [7] CKEC0 << ->>CKEC1 [7] [8] CKED0 << ->>CKED1 [8] CKECO CKEC CKEDO CKED CLKC0 CLKC0B CLKD0 CLKD0B XAT1 XAV3 XAU7 XAU7 XAV7 RSVD#11 RSVD#11 RSVD#13 MVREFD/S =0.7* VDDR1 R3632 40.2R 1% MVREFD/S =0.7* VDDR1 MVREFDC MVREFDD NC MVREFD20 NC MVREFD2 = C3624 1uF_6.3V C3625 1uF_6.3V +MVDD R3622 40.2R AL15 MVREFS C [7,8] DRAM_RST2 MVREFS D MVREFSO DRAM_RST2 MVREFSE R3627 5.1K C3617 120pF **AMD** Jarkham Ontario Monday, September 20, 2010 ASIC Memory Ch C & D No. 105-C204XX-00A

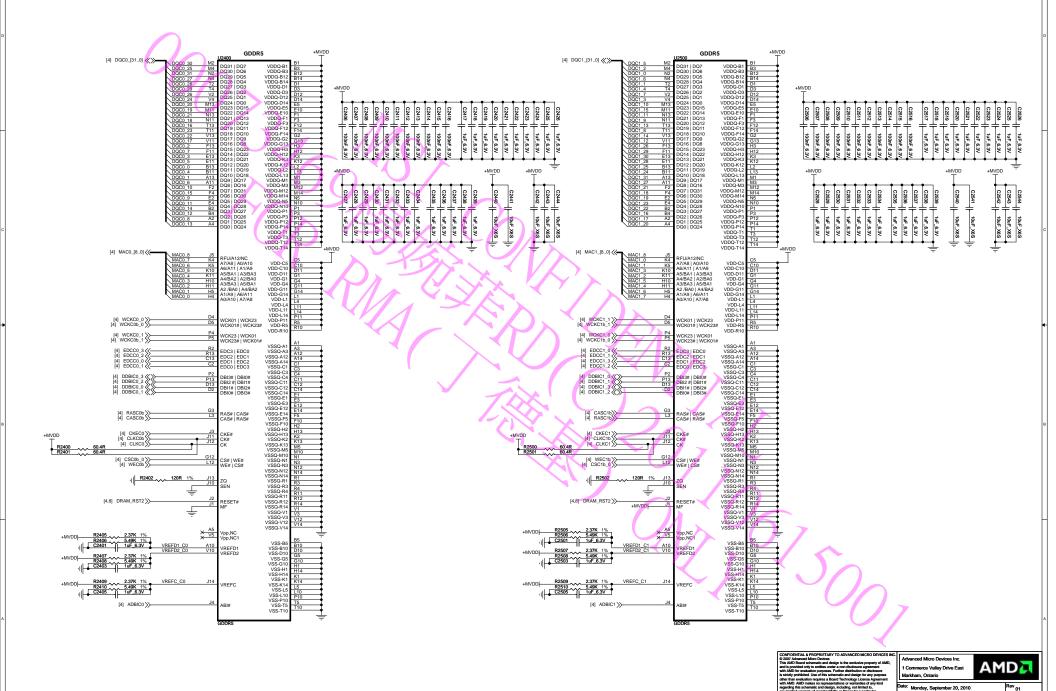
(5) GDDR5 Memory Channel A



CONTINUENTLY A TO ADMINISTRAT TO ADMINISTRAT TO ADMINISTRATE T

(6) GDDR5 Memory Channel B GDDR5 [3] DQB0_[31..0] 《>> [3] DQB1_[31..0] 《>> (931 | DO7 (930 | DO5 VDQ-B: VDQ-B: VDQ-B: VDQ-B: VDQ-B: VDQ-B: VDQ-D: VDQ-D: VDQ-D: VDQ-E: VDQ-F: VDQ-F: VDQ-F: VDQ-F: VDQ-F: VDQ-B: VD VDDQ-B VDDQ-B VDDQ-B VDDQ-B VDDQ-D VDDQ-D VDDQ-D VDDQ-D VDDQ-B VDDQ-F VDQ-F VDQ-T VDDQ-T 100nF_6.3V 100nF_6.3V 100nF_6.3V 100nF_6.3V 100nF_6.3V 100nF_6.3V 100nF_6.3V 1uF_6.3V 1uF_6.3V 1uF_6.3V 10F_6.3V 10F_6.3V 10F_6.3V 10F_6.3V 10F_6.3V C2344 10uF_X6S C2343 10uF_X6S 10uF_X6S C2238 | 1uF_6.3V C2238 | 1uF_6.3V C2237 | 1uF_6.3V C2236 | 1uF_6.3V C2340 | 10uF_X6S | C2241 | 10uF_X6S | C2341 | 10uF_X6S ||-1 10F_6.3V 2 10F_6.3V 1 10F_6.3V 1 10F_6.3V 1 10F_6.3V 1 10F_6.3V 1 10F_6.3V 10uF_X6S 1uF_6.3V 10F_6.3V 10F_6.3V 10F_6.3V 10F_6.3V 10F_6.3V 10uF_X6S [3] MABO_[8..0] <<-[3] MAB1_[8..0] (RFU/A12/NC A7/A8 | A0/A10 A6/A11 | A1/A9 A5/BA1 | A3/BA3 A4/BA2 | A2/BA0 A3/BA3 | A5/BA1 A2 /BA0 | A4/BA2 A1/A9 | A6/A11 A0/A10 | A7/A8 RFU/A12/NC A7/A8 | A0/A10 A6/A11 | A1/A9 A5/BA1 | A3/BA3 A4/BA2 | A2/BA0 A3/BA3 | A5/BA1 A2 /BA0 | A4/BA2 A1/A9 | A6/A11 A0/A10 | A7/A8 VDD-C1 VDD-D1 VDD-G1 VDD-G4 VDD-C1 VDD-C1 VDD-G1 VDD-G1 VDD-G1 VDD-L1 VDD-L1 VDD-L1 VDD-P1 VDD-R1 VDD-G1 VDD-G14 VDD-L1 VDD-L4 VDD-L11 VDD-L14 VDD-P11 VDD-R5 WCK23 | WCK01 WCK23# | WCK01# WCK23 | WCK01 WCK23# | WCK01# VSSQ-A VSSQ-A1 VSSQ-A1 VSSQ-A1 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-E1 VSSQ-B1 VSSQ-A1 VSSQ-A3 VSSQ-A12 VSSQ-A14 VSSQ-C1 VSSQ-C1 VSSQ-C1 VSSQ-C14 [3] EDCB0_1 [3] EDCB0_0 [3] EDCB0_2 [3] EDCB0_3 DC3 | EDC0 DC2 | EDC1 DC1 | EDC2 DC0 | EDC3 EDC3 | EDC0 EDC2 | EDC1 EDC1 | EDC2 EDC0 | EDC3 DBI3# | DBI0# DBI2 #| DBI1# DBI1# | DBI2# DBI0# | DBI3# DBI3# | DBI0# DBI2 #| DBI1# DBI1# | DBI2# DBI0# | DBI3# [3] RASB0b>> [3] CASB0b>> [3] CASB1b [3] CKEB0 [3] CLKB0b [3] CKEB1 [3] CLKB1b [3] CLKB1 CS# | WE# WE# | CS# [3,5] DRAM_RST1 >> [3,5] DRAM_RST1 >> VSS-B5 VSS-B10 VSS-D10 VSS-G5 VSS-G10 VSS-H1 VSS-H14 VSS-K14 VSS-L5 VSS-L10 VSS-P10 VSS-T5 VSS-T10 VSS-B: VSS-B1: VSS-G: VSS-G: VSS-H1: VSS-H: VSS-L: VSS-L: VSS-L: VSS-P1: VSS-T1: [3] ADBIB0 > **AMD** larkham Ontario Monday, September 20, 2010 GDDR5 Ch B No. 105-C204XX-00A

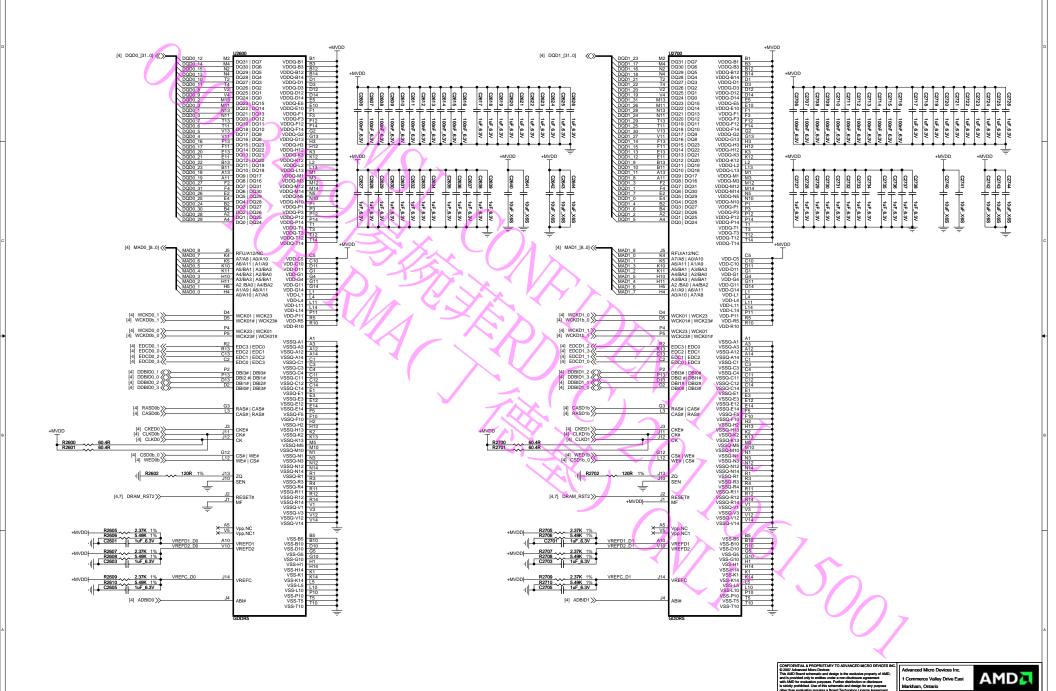
(7) GDDR5 Memory Channel C



GDDR5 Ch C

No. 105-C204XX-00A

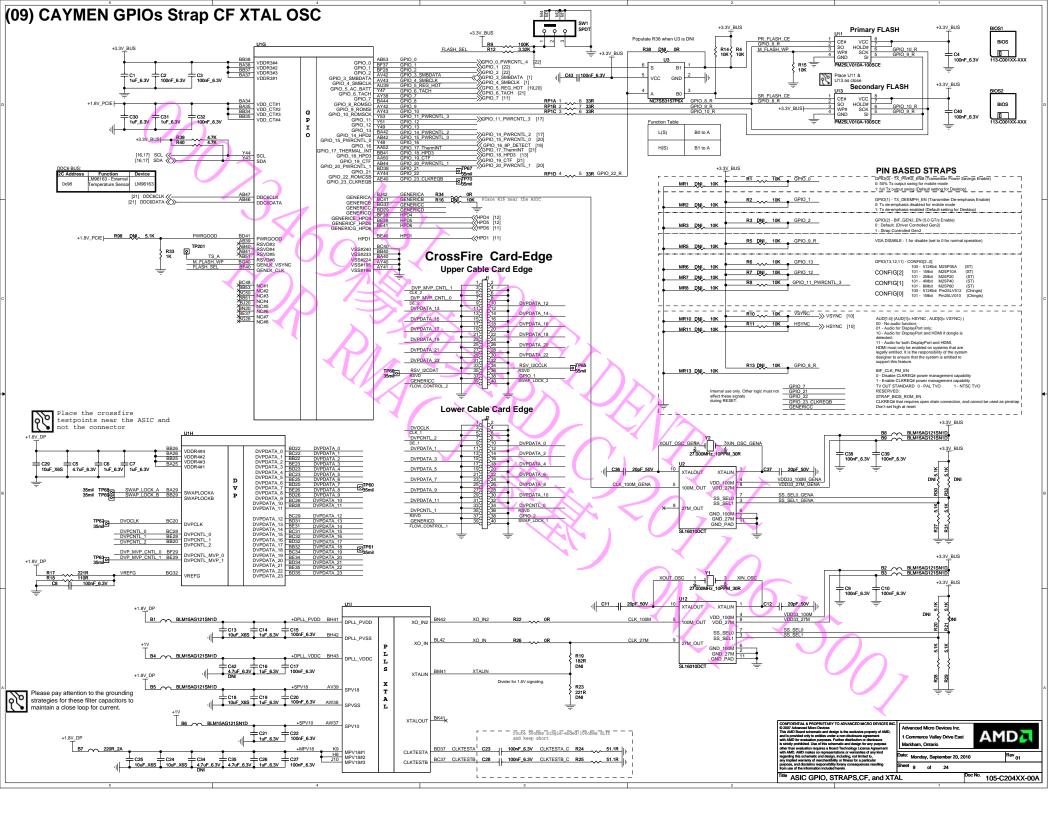
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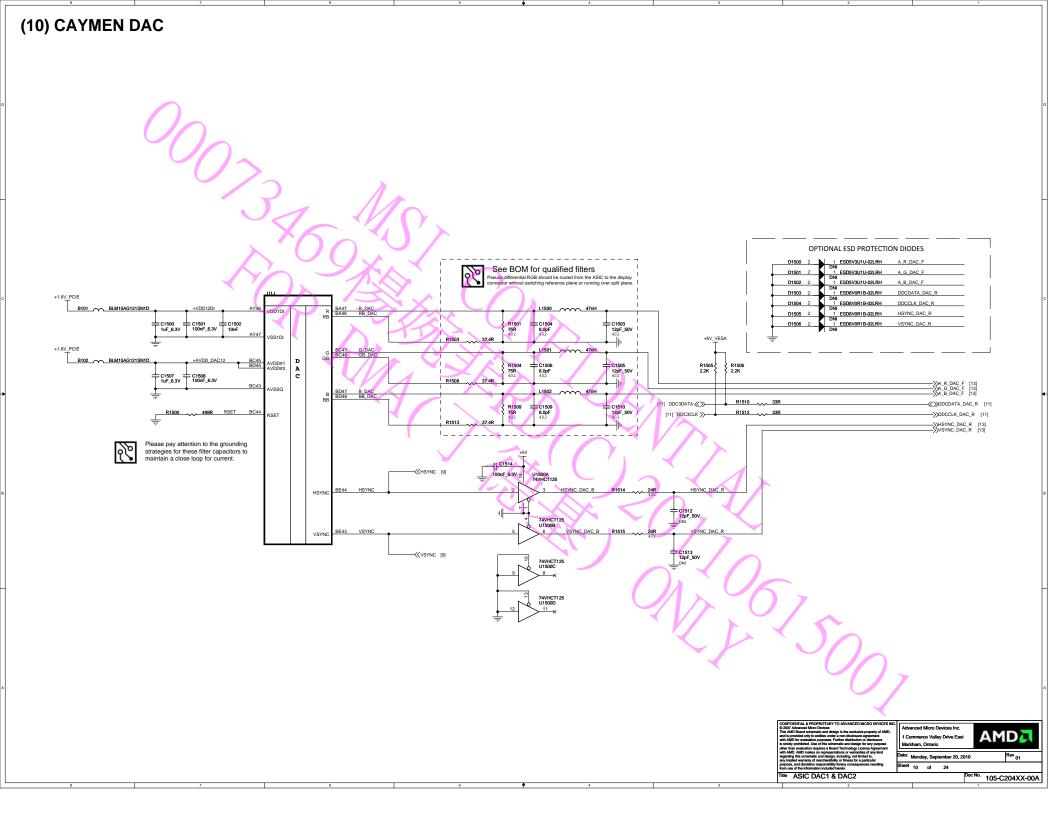


Monday, September 20, 2010

No. 105-C204XX-00A

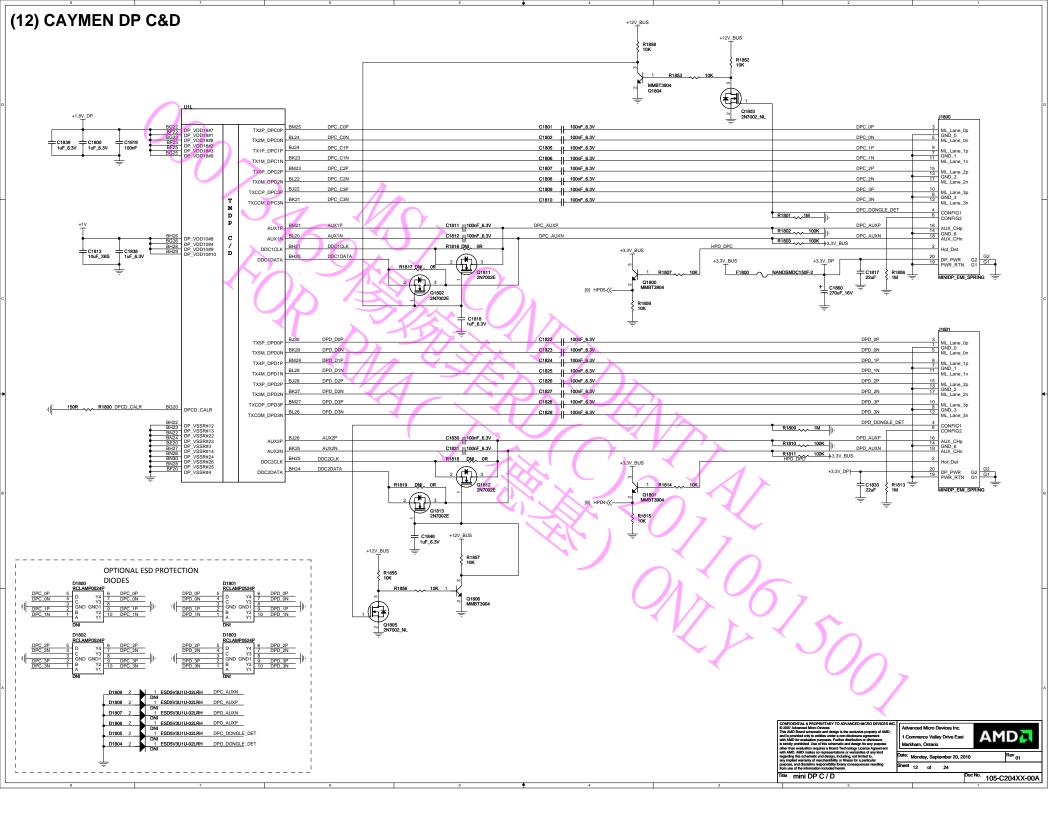
GDDR5 Ch D

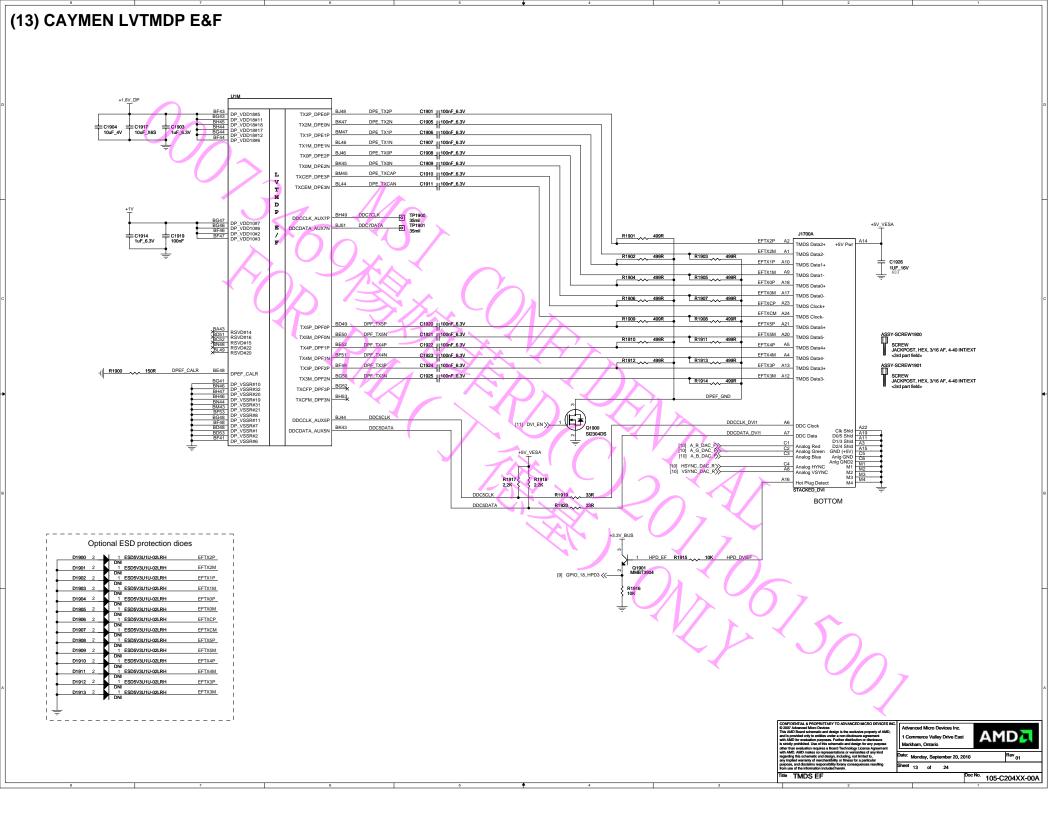


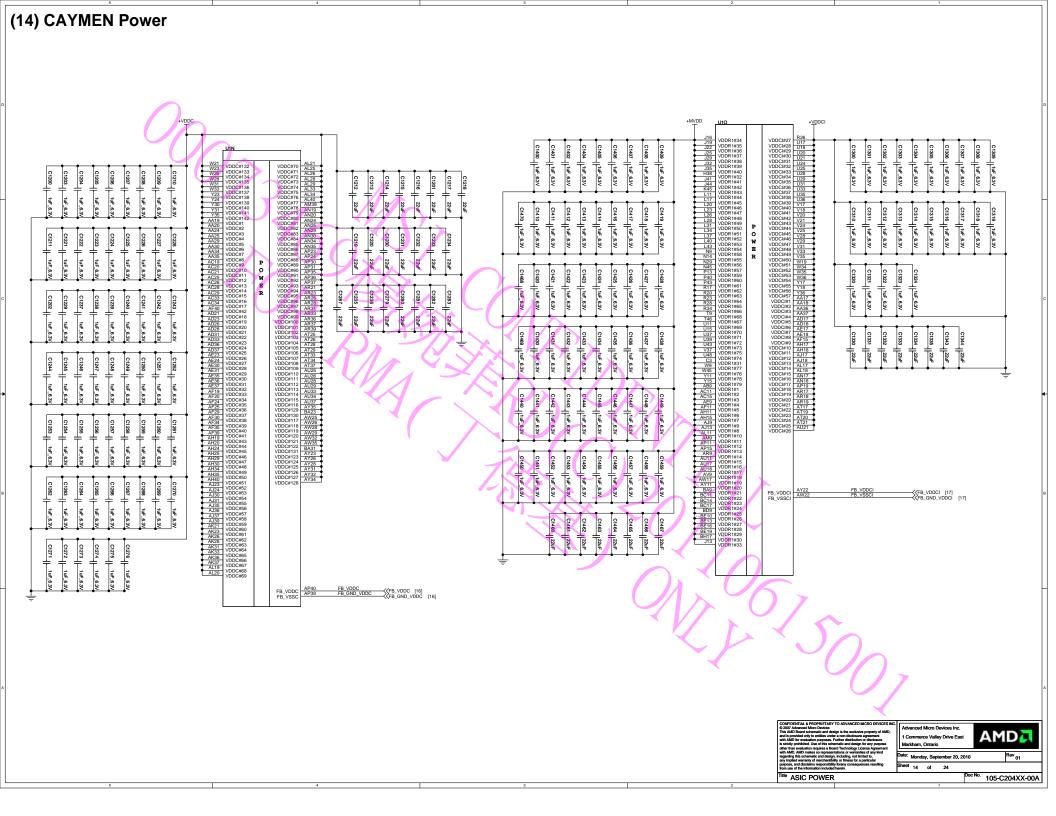


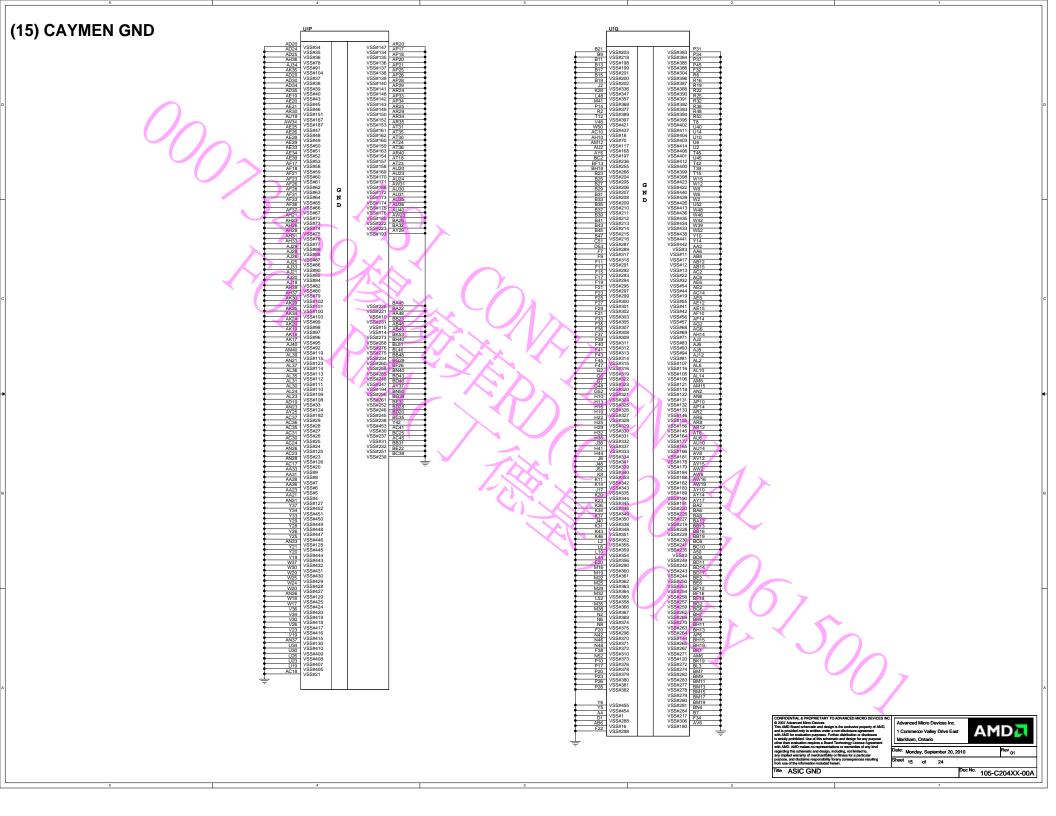
Q1702 SI2304DS 499R 2 499R 3 499R 2 49 1131 DVI EN >>-R1733 C1729 100nF_6.3V +1.8V_DP TX2P DPAG VDD18#15 VDD18#16 VDD18#14 VDD18#10 VDD18#4 VDD18#13 DPA_TX2N TX2M_DPA0 C1736 | 100nF_6.3V DPA TX1N DDC4CLK DDC4DATA TX1M_DPA1 DPA TXOP TX0P DPA2 +5V_VESA Please pay attention to the grounding DPA TX0N HPD_DPA strategies for these filter capacitors to maintain a close loop for current. TX0M DPA2 R1730 2.2K R1731 2.2K DPA_TXCAP TXCAP_DPA3 TXCAM_DPA3 Q1703 MMBT3904 [9] HPD6 <<-->> DDC3CLK [10] DDCCLK AUX3 R1728 10K DCDATA_AUX3N -≪≫DDC3DATA [10] +5V VESA +1.8V_PCIE J1700B C1701 100nF_6.3V TMDS_Data2+ +5V_Pwr C1705 100nF_6.3V C1712 1UF_16V R1701 499R R1703 C1706 100nF_6.3V TMDS Data1+ C1707 100nF_6.3V ABTX1M B9 TMDS Data1-R1702 499R R1705 C1708 100nF_6.3V TMDS_Data0+ C1709 100nF_6.3V TMDS_Data0-R1704 _____ 499R R1707 _____ 499R C1710 100nF_6.3V C1711 100nF_6.3V R1706 499R R1708 499R C1720 | 100nF_6.3V TMDS Data54 BL38 DPB_TX5N C1721 100nF_6.3V ABTX5M B20 TMDS Data5-TX5M DPB0 R1709 _____ 499R R1711 C1722 100nF_6.3V C1723 100nF_6.3V R1710 499R R1713 ABTX3P B13 C1724 | 100nF_6.3V TMDS_Data3+ R1700 N 150R DPAB_CALR BF32 DPAB_CALR C1725 100nF_6.3V ABTX3M B12 TX3M_DPB2N TMDS_Data3-R1712 499R R1714 +12V BUS TXCBP_DPB3P DP_VSSR#16 DP_VSSR#28 DP_VSSR#29 DP_VSSR#27 DP_VSSR#5 DP_VSSR#17 DP_VSSR#18 DP_VSSR#30 DP_VSSR#39 DP_VSSR#9 BK35 TXCBM_DPB3N BM31 DDC4CLK [13] DVI_EN <<--[10] DDCCLK_DAC_R>> Clk_Shid D0/5_Shid D1/3_Shid D2/4_Shid BI 30 DDC4DATA [10] DDCDATA_DAC_R(()) DCDATA_AUX4N DDC_Data C1727 100nF Analog Red Analog_Green GND_(+5V) Analog_Blue Anlg_GND +3.3V_BUS R1715 10K HPD_DVIAB B16 Hot_Plug_Detect Q1701 MMBT390 Optional ESD protection dioes TOP 1 ESD5V3U1U-02LRH DNI ASSY-SCREW1700 SCREW JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT <3rd part field> ESD5V3U1U-02LRH 1 ESD5V3U1U-02LRH DNI 1 ESD5V3U1U-02LRH DNI ASSY-SCREW1701 ABTX0P SCREW JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT <3rd part field> 1 ESD5V3U1U-02LRH DNI 1 ESD5V3U1U-02LRH ABTX5P 1 ESD5V3U1U-02LRH ABTX5M 1 ESD5V3U1U-02LRH DNI ABTX4P 1 ESD5V3U1U-02LRH 1 ESD5V3U1U-02LRH D1713 2 ABTX3M **AMD** Markham, Ontario Monday, September 20, 2010 No. 105-C204XX-00A

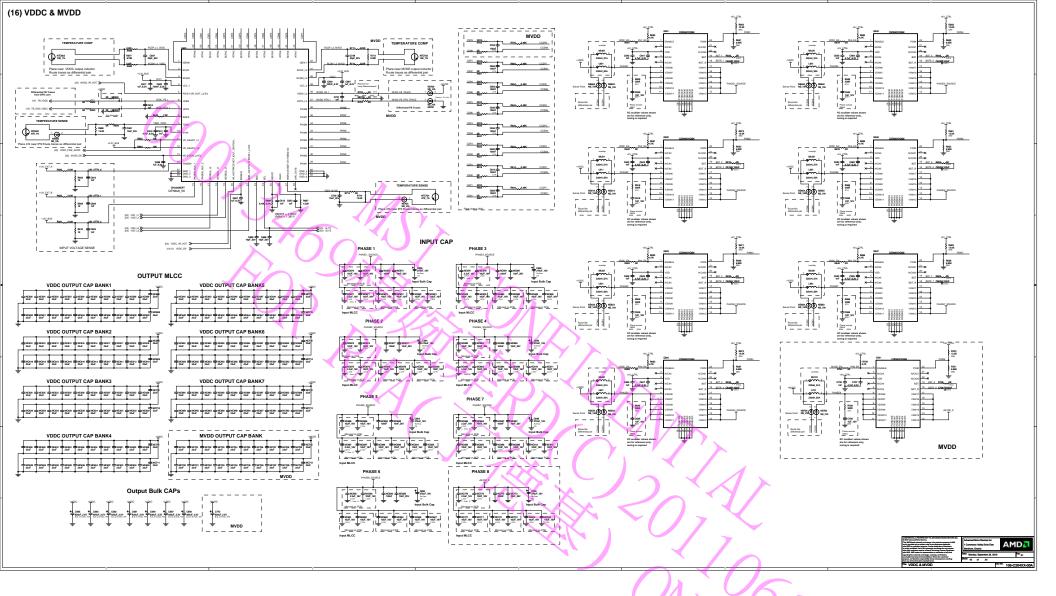
(11) CAYMEN TMDS A&B

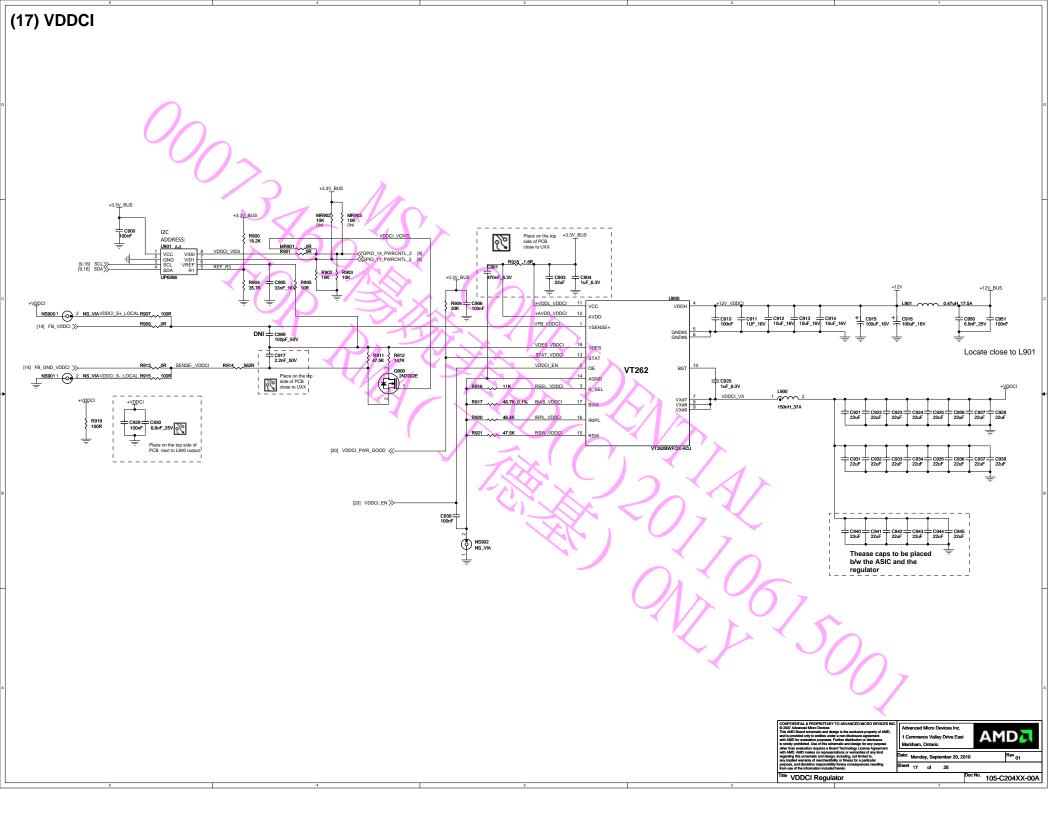






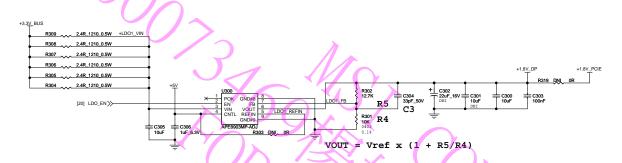


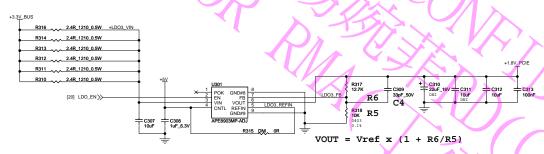




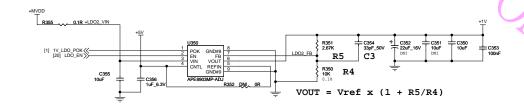
(18) CAYMEN Small Rail Regulators

LDO #1: Vin = 2.3V to 3.6V MAX Vout = +1.8V +/- 2% lout = 2.0A (TBV) RMS MAX PCB: 50 to 70mm sq. copper area for cooling





LDO #2: Vin = \pm 1.40V to 1.8VMAX Vout = \pm 1V \pm 2% lout = 1.5A (TBV) RMS MAX PCB: 50 to 70mm sq. copper area for cooling



Regulators for +5V, +5V_VESA and +5V_HDMI lout max = 150mA (DVI+HDMI)

