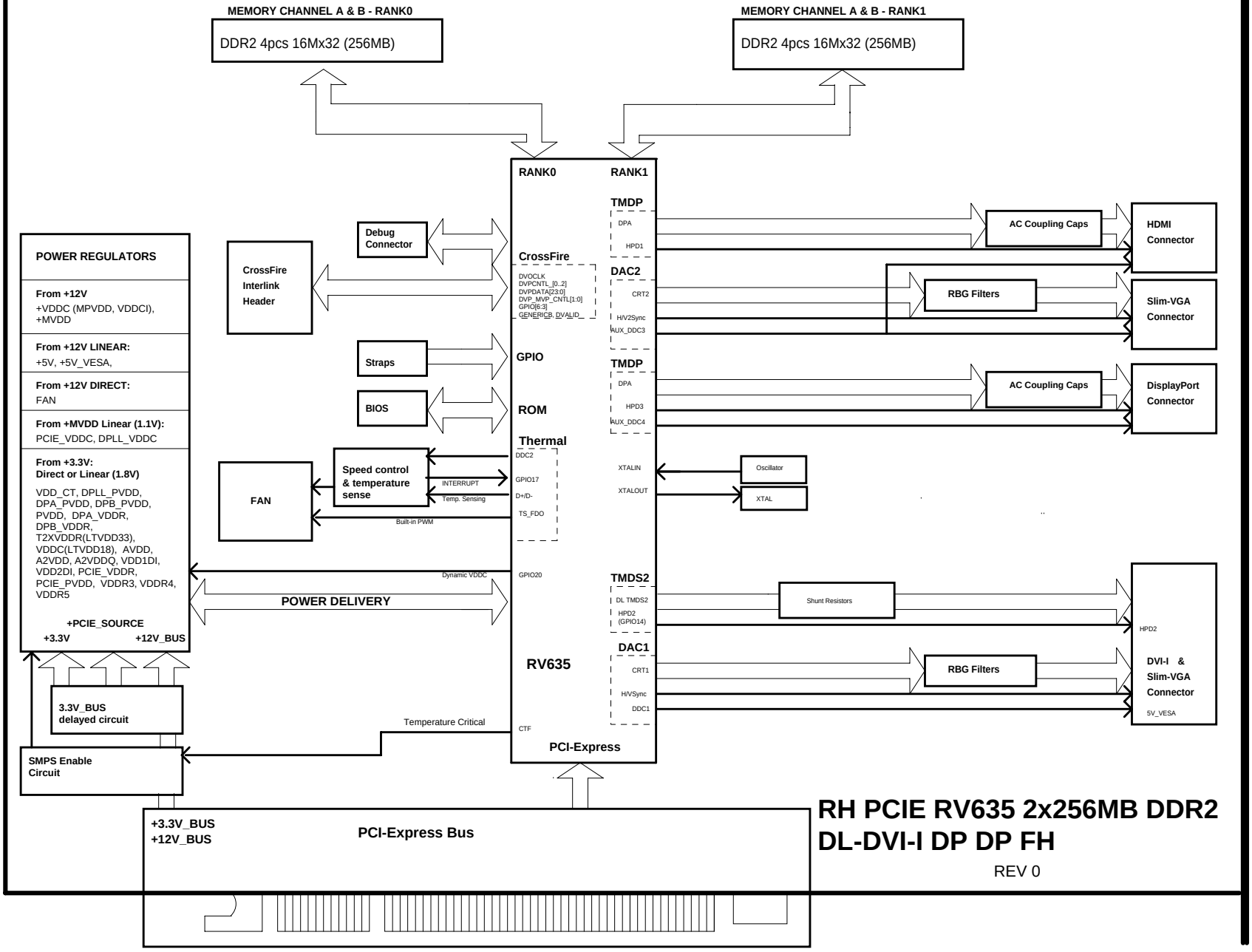
| Title | Schematic No. | Date: |
|---|---|---|
| RH PCIE RV635 2x256MB DDR2 DUAL DL-DVI-I DL-DVI-I VO FH | 105-B382xx-10 | Wednesday, January 09, 2008 |

# REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
**For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.**
**Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 2

| Sch Rev | PCB Rev | Date | REVISION DESCRIPTION |
|---|---|---|---|
| 0 | 00A | 16/10/07 | Initial design for RV635 GDDR3 |
| 1 | 00 | 20/12/07 | Release to Production |
| 2 | 10 | 04/01/08 | HDMI J2001 connector changed from 61400515G to 6140024800G |




# RH PCIE RV635 2x256MB DDR2
# DL-DVI-I DP DP FH

REV 0



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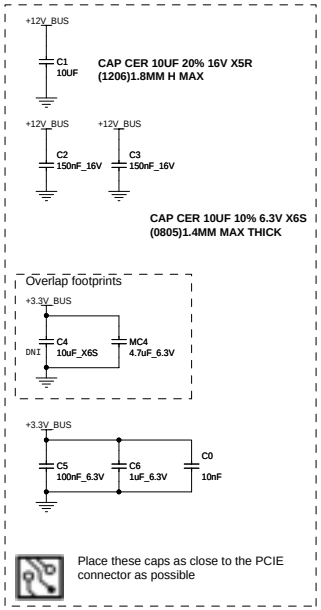
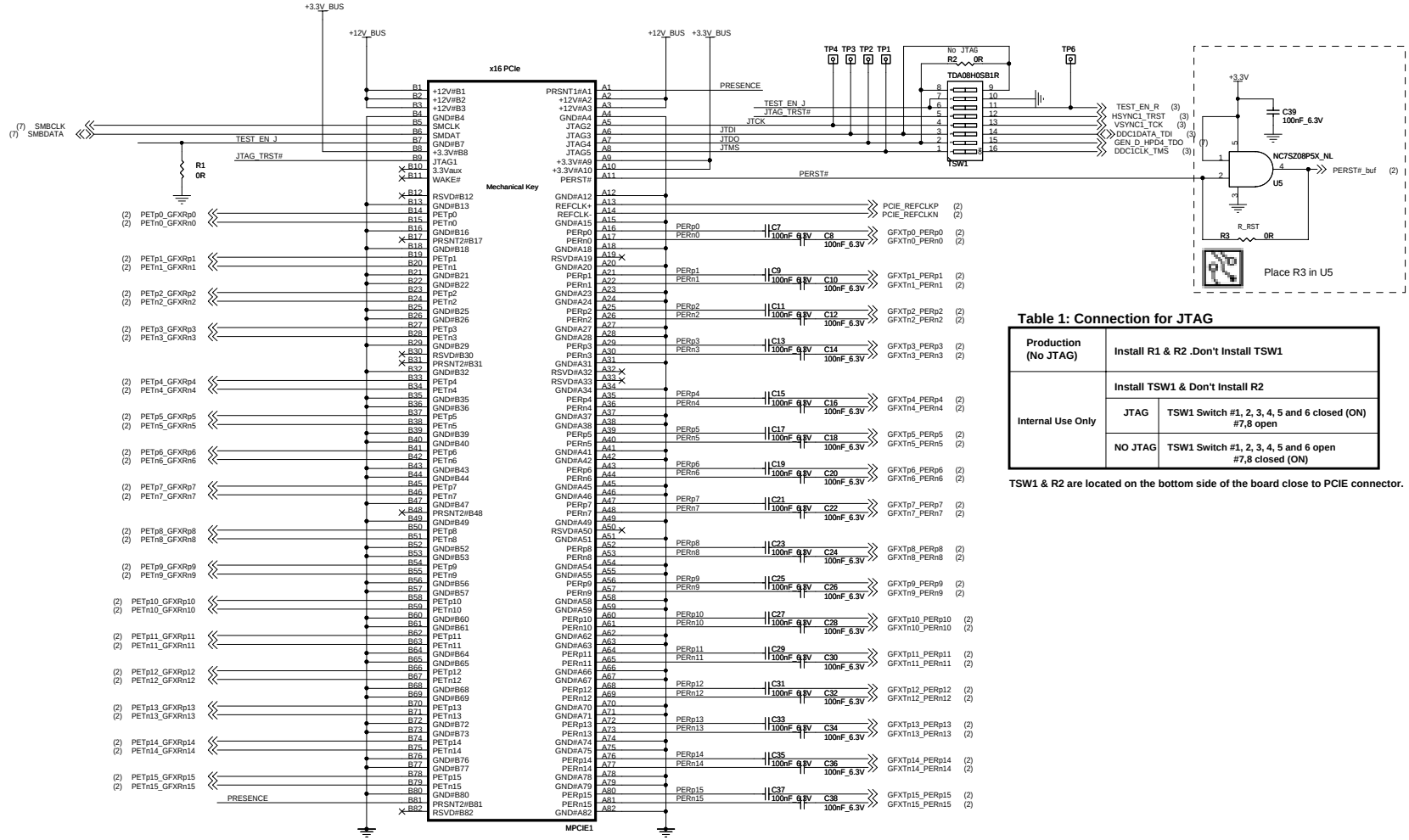
| Title | RV635 DDR2 - BLOCK DIAGRAM |
| Doc No. | 105-B382xx-10 |

# PCI-EXPRESS EDGE CONNECTOR




## Table 1: Connection for JTAG

| | | |
|---|---|---|
| **Production (No JTAG)** | **Install R1 & R2 .Don't Install TSW1** | |
| **Internal Use Only** | **Install TSW1 & Don't Install R2** | |
| | **JTAG** | **TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #7,8 open** |
| | **NO JTAG** | **TSW1 Switch #1, 2, 3, 4, 5 and 6 open #7,8 closed (ON)** |

**TSW1 & R2 are located on the bottom side of the board close to PCIE connector.**

| SYMBOL LEGEND | |
|---|---|
| DNI | DO NOT INSTALL |
| # | ACTIVE LOW |
| | DIGITAL GROUND |
| | ANALOG GROUND |
| BUO | BRING UP ONLY |



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| Title | RV635 DDR2 - PCI-E Edge Connector |
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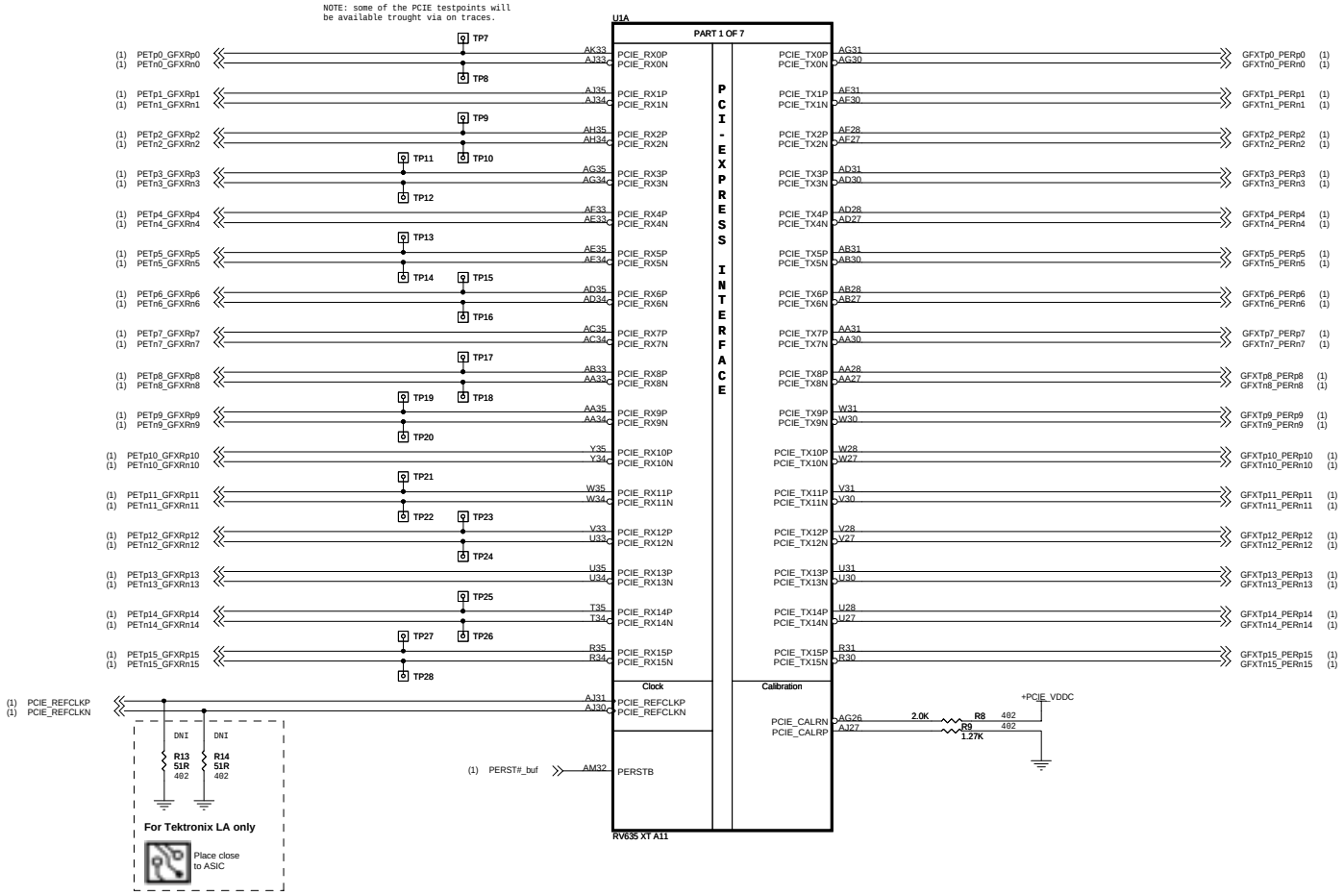




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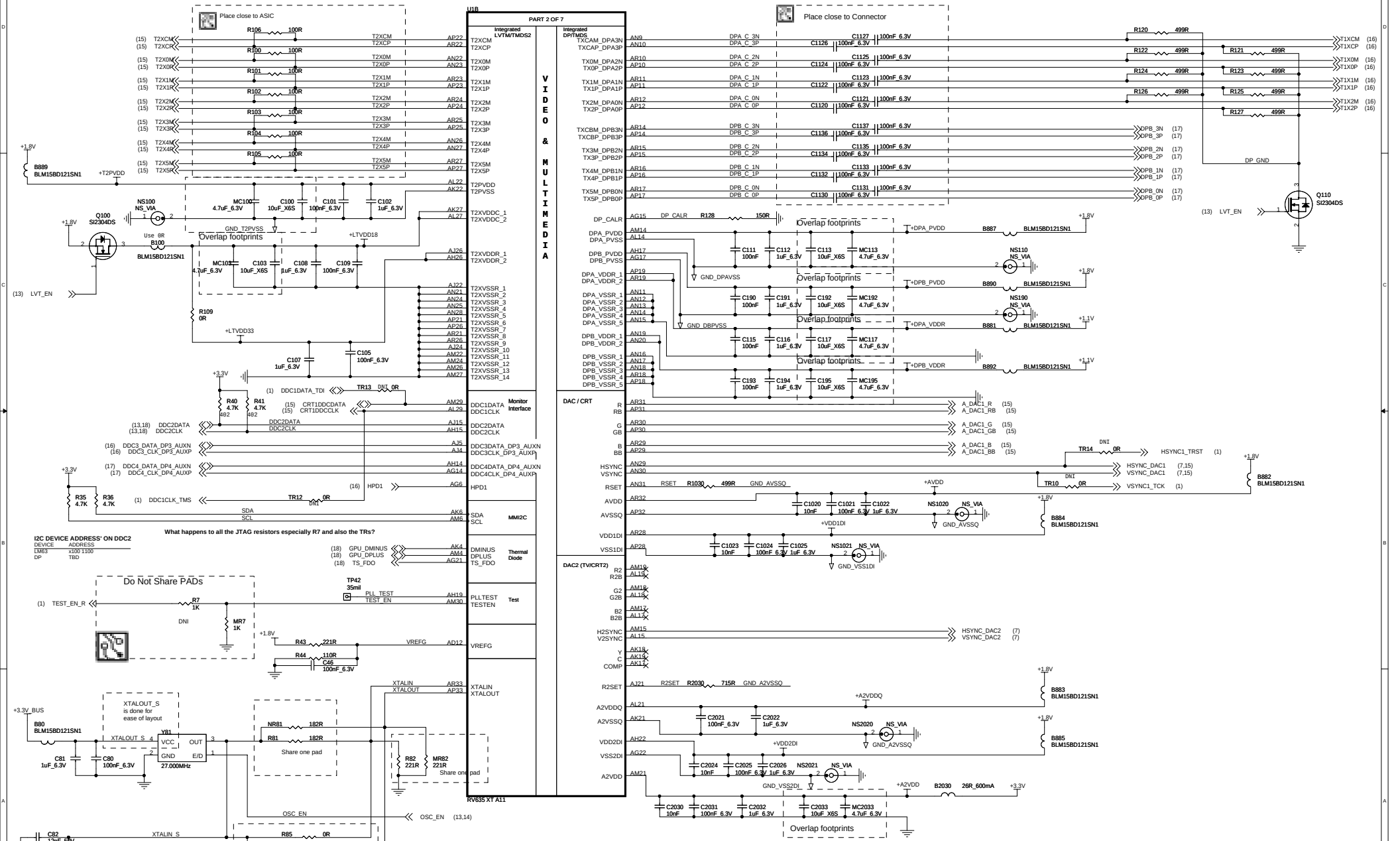
Title RV635 DDR2 - ASIC PCIE_Interface

Doc No. 105-B382xx-10

**Recommended caps:**
**(see BOM for qualified values/vendors)**
**10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK**
**1uF, X6S, 0402, 6.3V**
**100nF, X7R, 0402**
**10nF , X7R, 0402**







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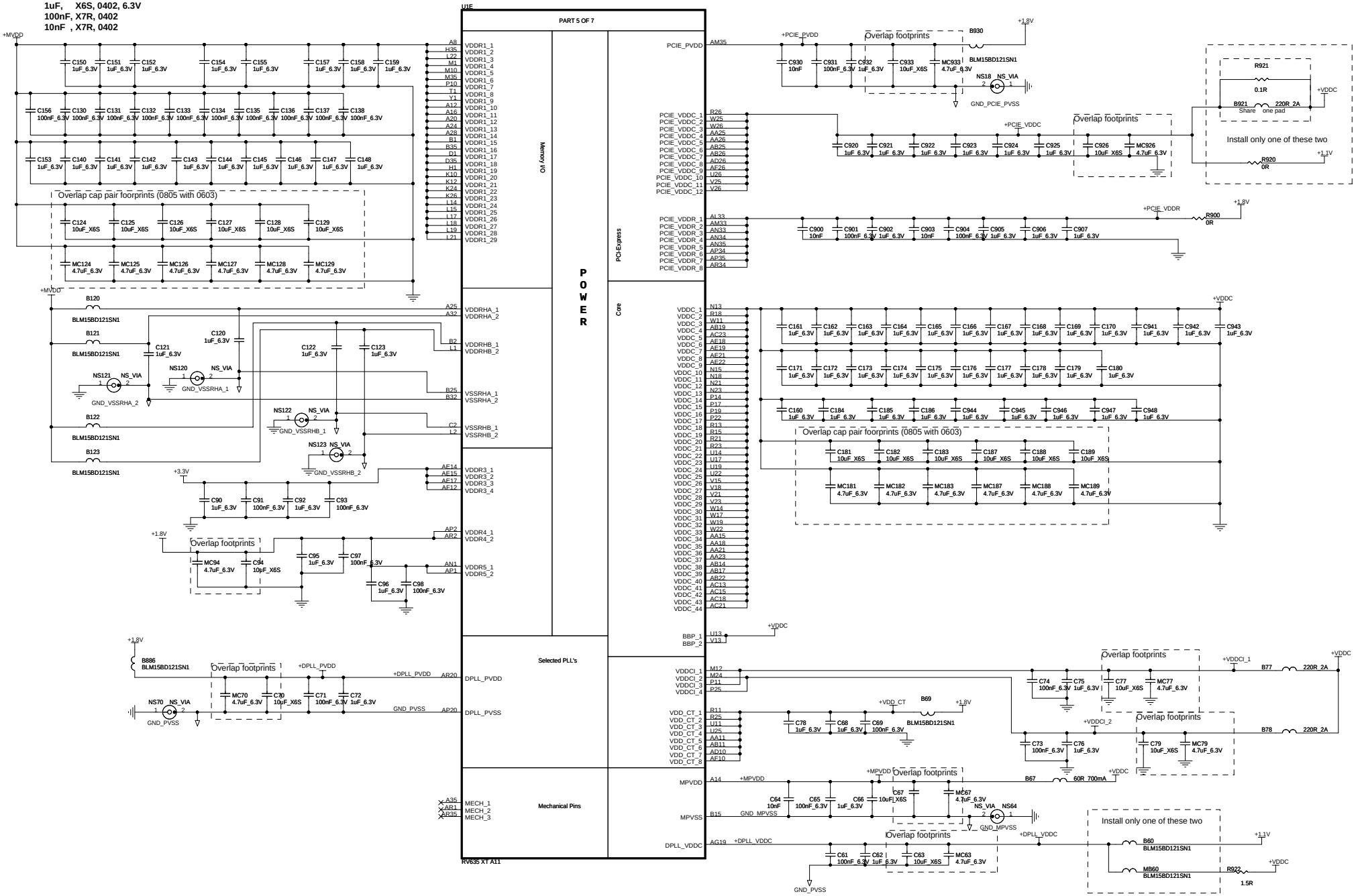
| Title | RV635 DDR2 - ASIC MAIN |
| Doc No. | 105-B382xx-10 |

**Recommended caps:**
**(see BOM for qualified values/vendors)**
**10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK**
**1uF, X6S, 0402, 6.3V**
**100nF, X7R, 0402**
**10nF , X7R, 0402**



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| | |
|---|---|
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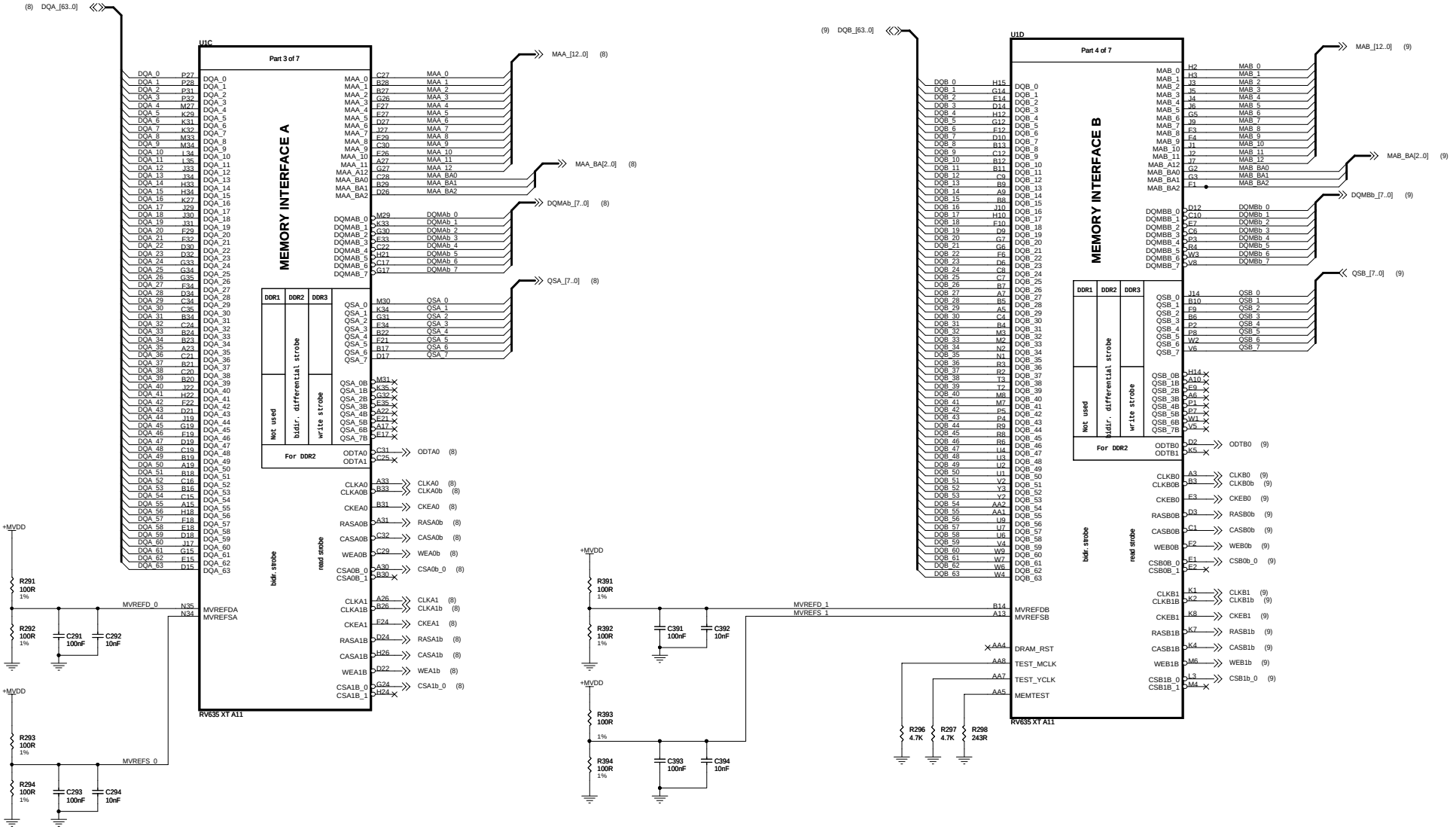
| Title | RV635 DDR2 - ASIC Power |
| Doc No. | 105-B382xx-10 |



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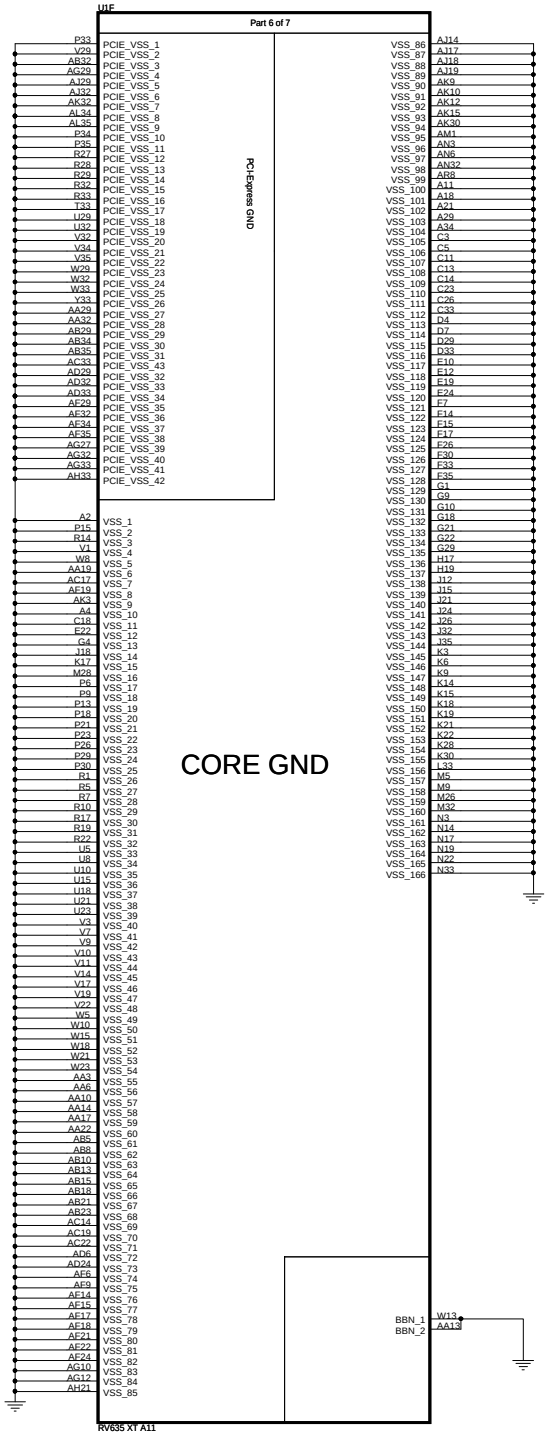
Title RV635 DDR2 - ASIC Memory Interface (Channel A & B) Doc No. 105-B382xx-10



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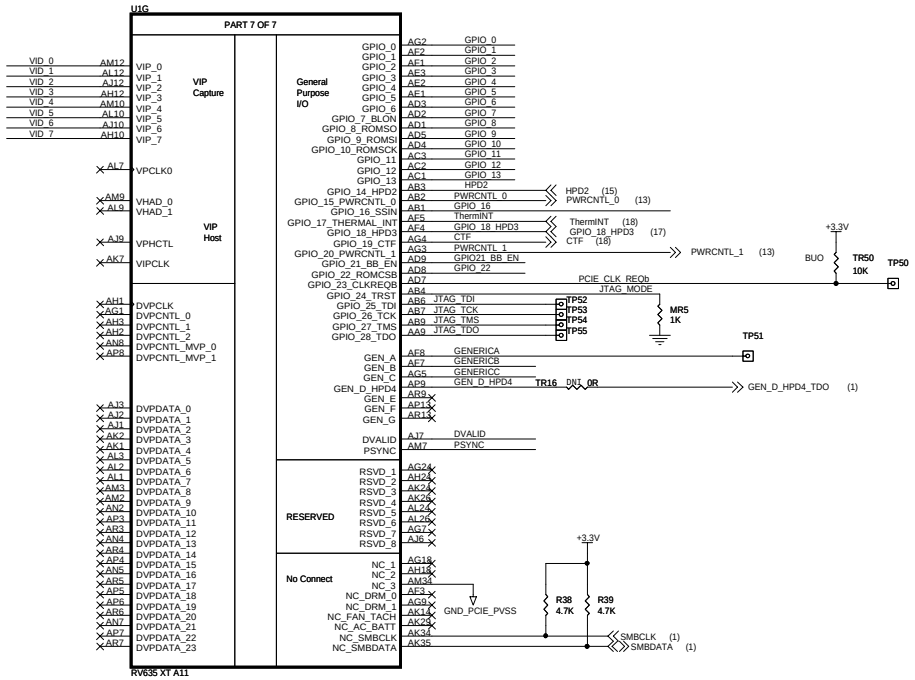
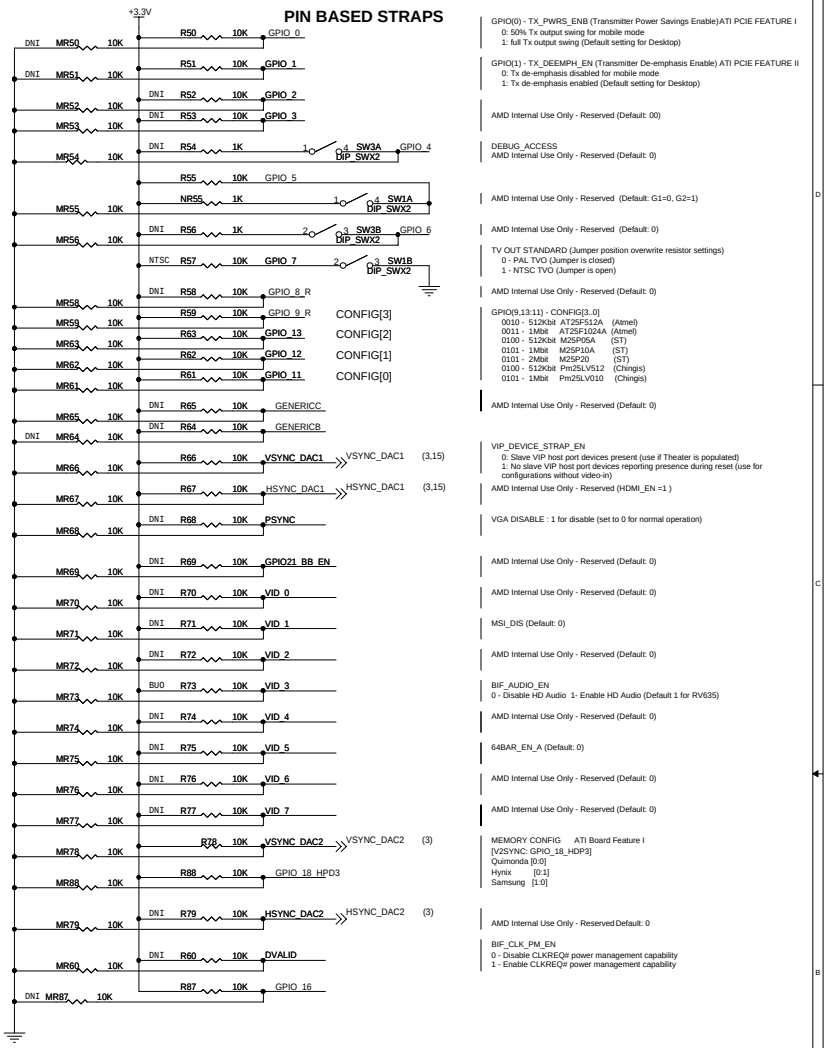
Title RV635 DDR2 - ASIC Grounds

Doc No. 105-B382xx-10




## PIN BASED STRAPS




GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

AMD Internal Use Only - Reserved (Default: 00)

DEBUG_ACCESS
AMD Internal Use Only - Reserved (Default: 0)

AMD Internal Use Only - Reserved (Default: G1=0, G2=1)

AMD Internal Use Only - Reserved (Default: 0)

TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

AMD Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0]
0010 - 512Kbit AT25F512A (Atmel)
0011 - 1Mbit AT25F1024A (Atmel)
0100 - 512Kbit M25P05A (ST)
0101 - 1Mbit M25P10A (ST)
0101 - 2Mbit M25P20 (ST)
0100 - 512Kbit Pm25LV512 (Chingis)
0101 - 1Mbit Pm25LV010 (Chingis)

AMD Internal Use Only - Reserved (Default: 0)

VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

AMD Internal Use Only - Reserved (HDMI_EN =1 )

VGA DISABLE : 1 for disable (set to 0 for normal operation)

AMD Internal Use Only - Reserved (Default: 0)

AMD Internal Use Only - Reserved (Default: 0)

MSI_DIS (Default: 0)

AMD Internal Use Only - Reserved (Default: 0)

BIF_AUDIO_EN
0 - Disable HD Audio 1- Enable HD Audio (Default 1 for RV635)

AMD Internal Use Only - Reserved (Default: 0)

64BAR_EN_A (Default: 0)

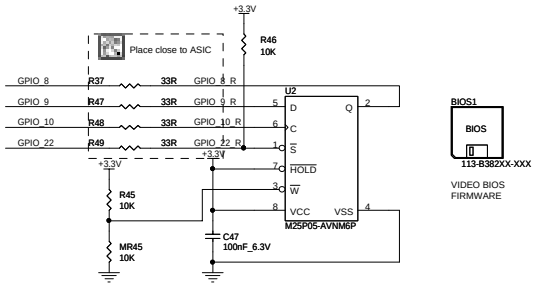
AMD Internal Use Only - Reserved (Default: 0)

AMD Internal Use Only - Reserved (Default: 0)

MEMORY CONFIG ATI Board Feature I
[V2SYNC: GPIO_18_HDP3]
Quimonda [0:0]
Hynix [0:1]
Samsung [1:0]

AMD Internal Use Only - Reserved Default: 0

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability



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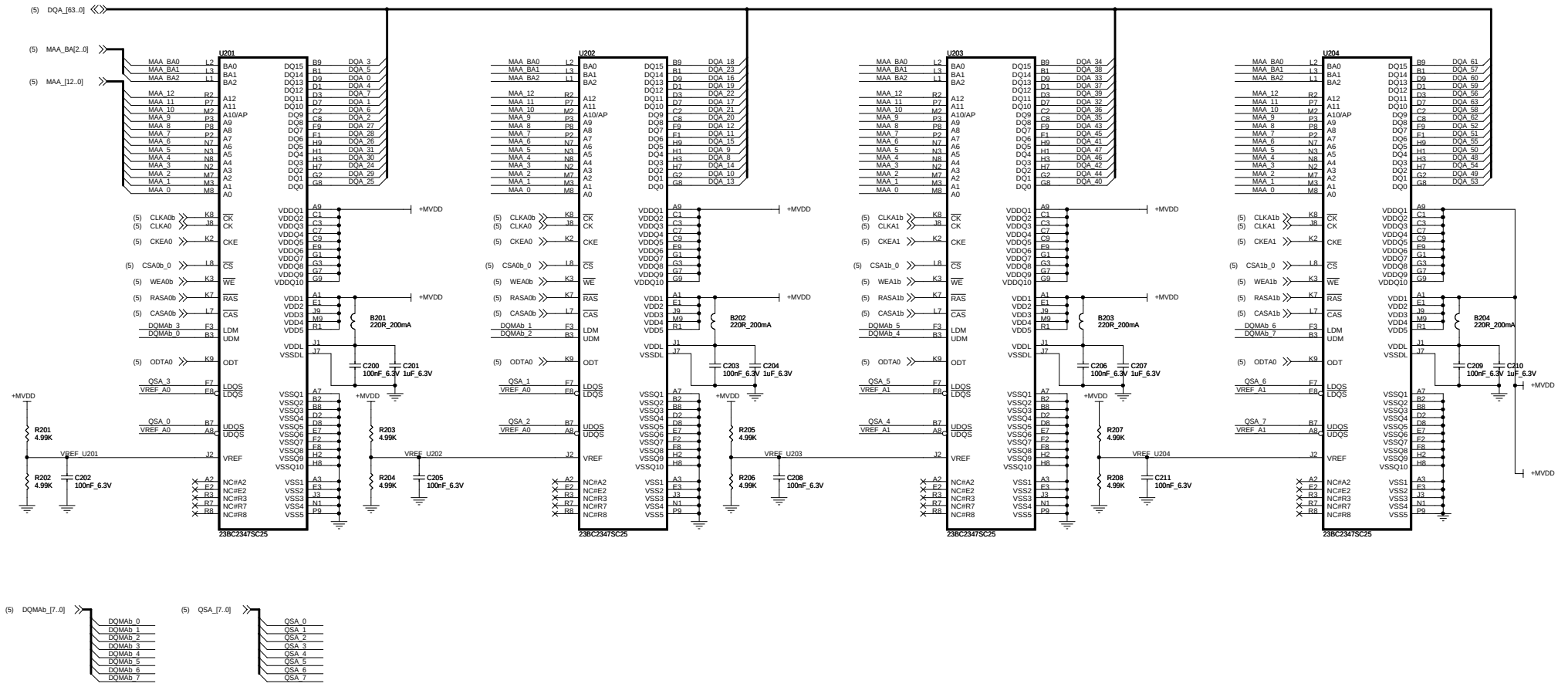
Title RV635 DDR2 - ASIC DVO & GPIOs

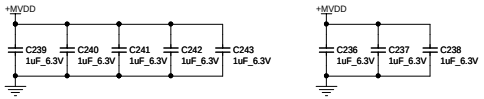
Doc No. 105-B382xx-10

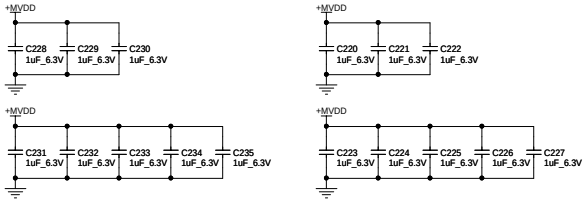
# CHANNEL A: 128MB/256MB DDR2

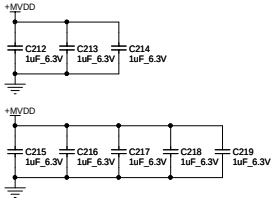


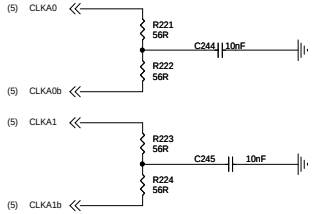


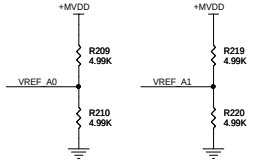




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Title RV635 DDR2 - MEM CH A

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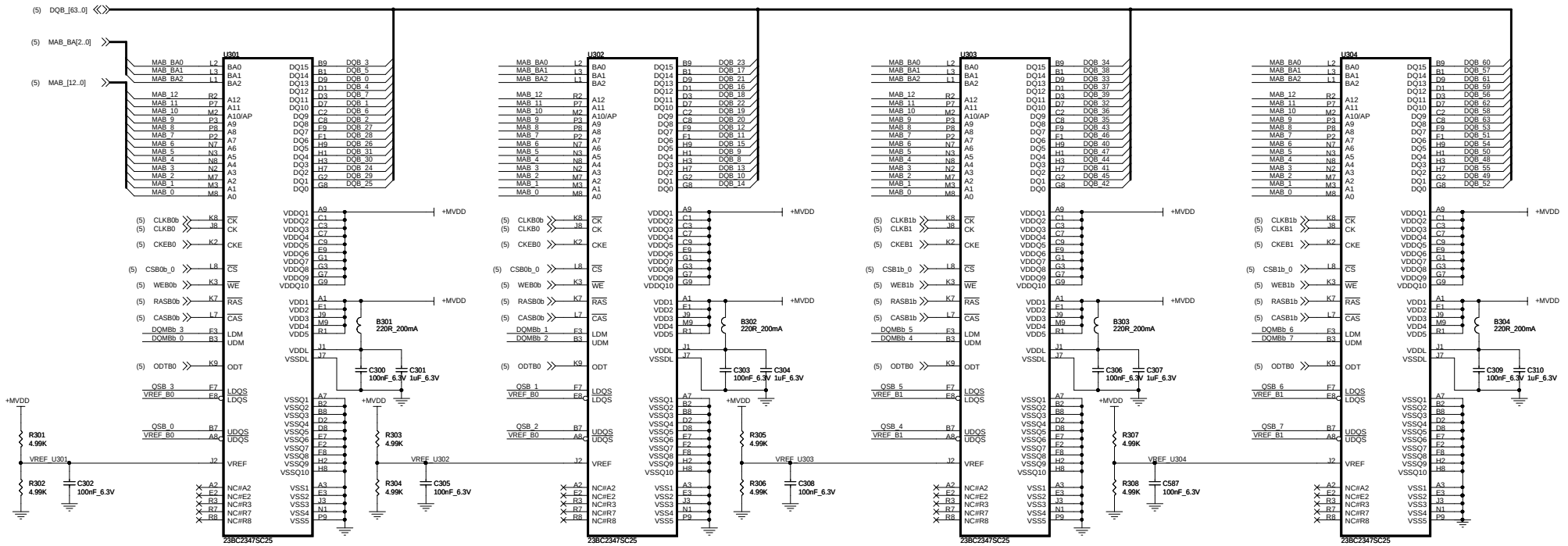
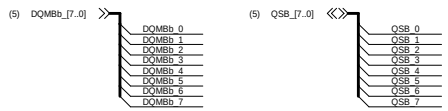
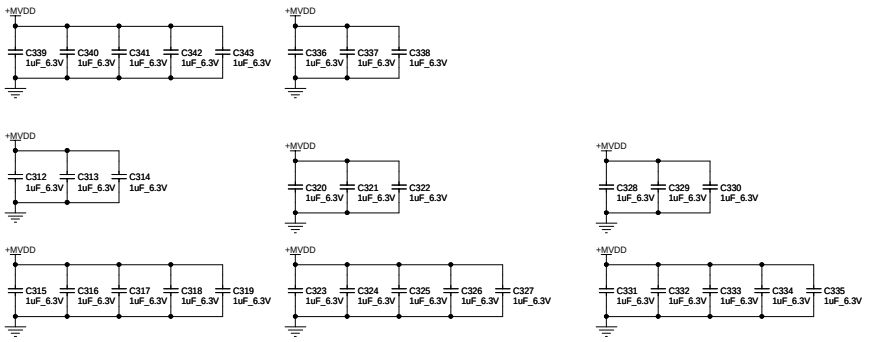
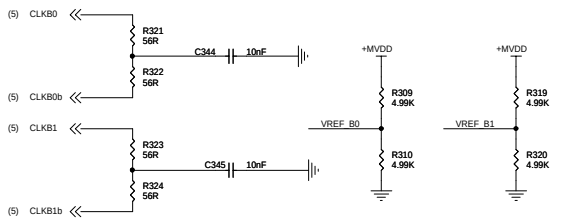
# CHANNEL B: 128MB/256MB DDR2



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| Title | RV635 DDR2 - MEM CH B |
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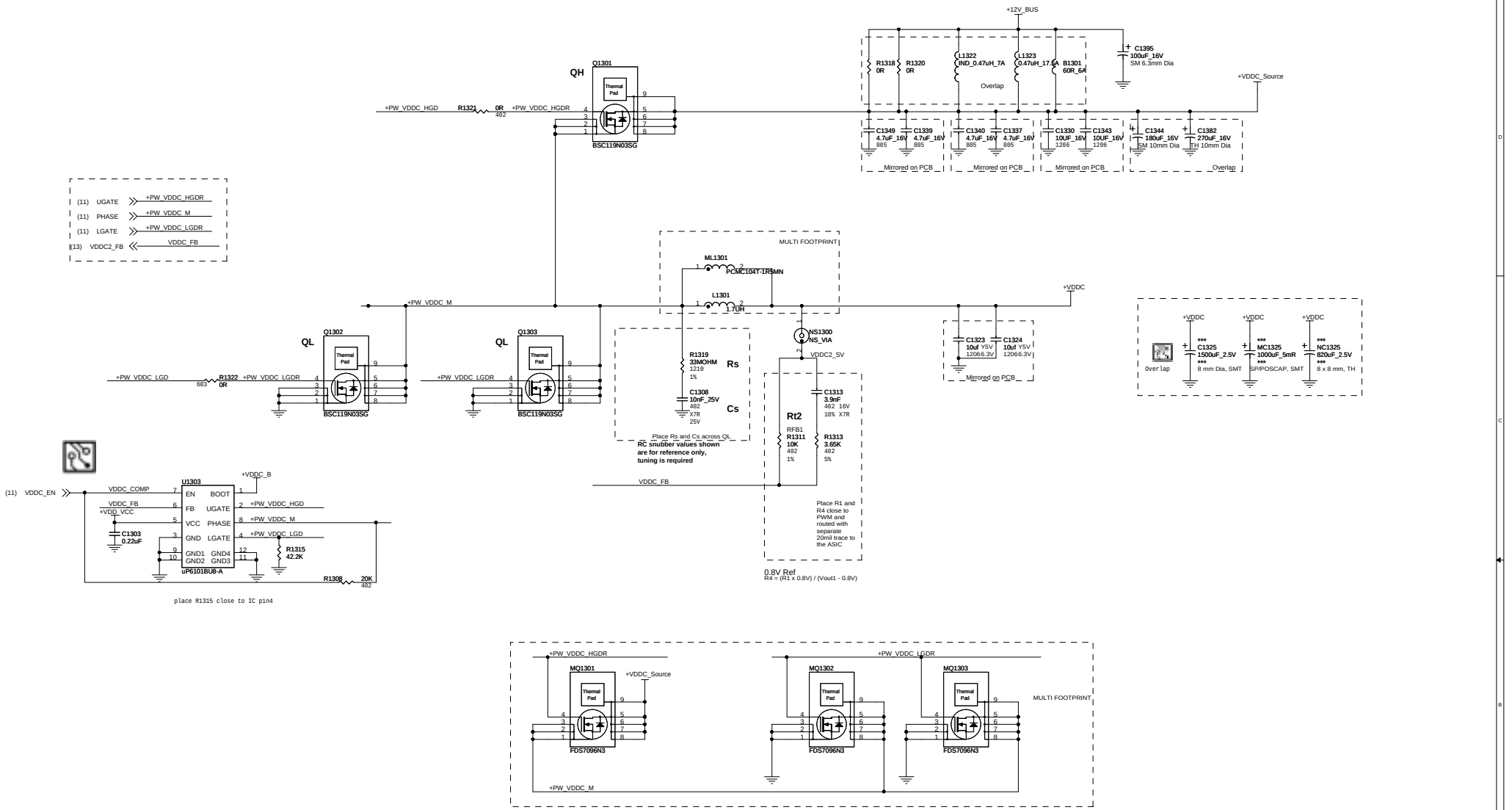
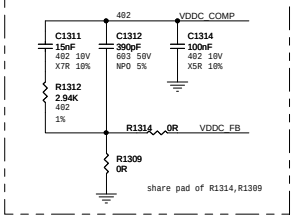
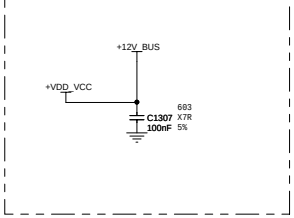


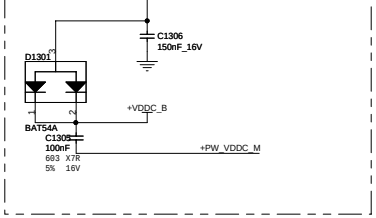

## COMPENSATION CIRCUIT




## FILTERED SMPS VCC




## BOOT CIRCUIT



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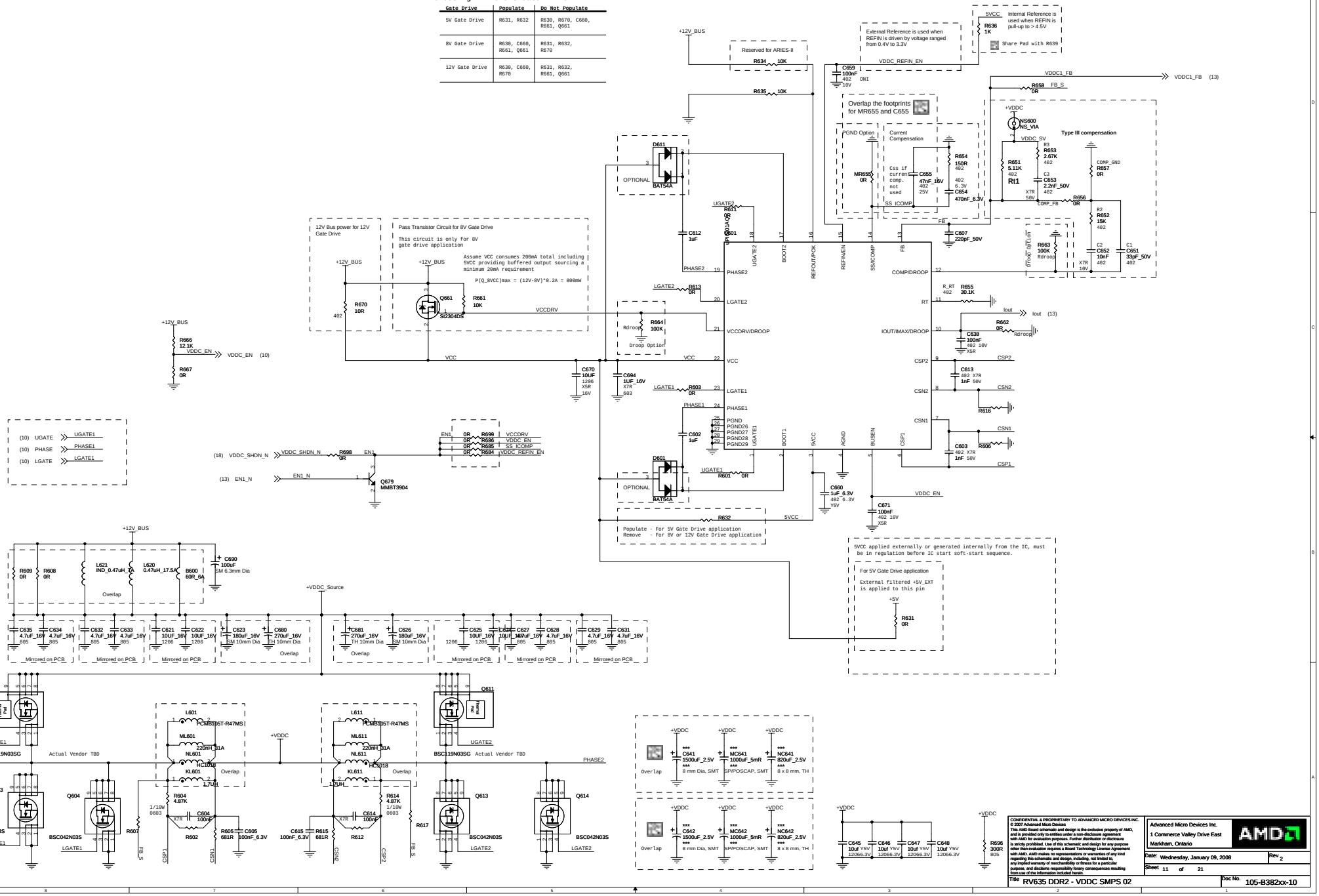
Title RV635 DDR2 - VDDC SMPS 01

Doc No. 105-B382xx-10

## Choosing Different Gate Drive

| Gate Drive | Populate | Do Not Populate |
|---|---|---|
| 5V Gate Drive | R631, R632 | R630, R670, C660, R661, Q661 |
| 8V Gate Drive | R630, C660, R661, Q661 | R631, R632, R670 |
| 12V Gate Drive | R630, C660, R670 | R631, R632, R661, Q661 |



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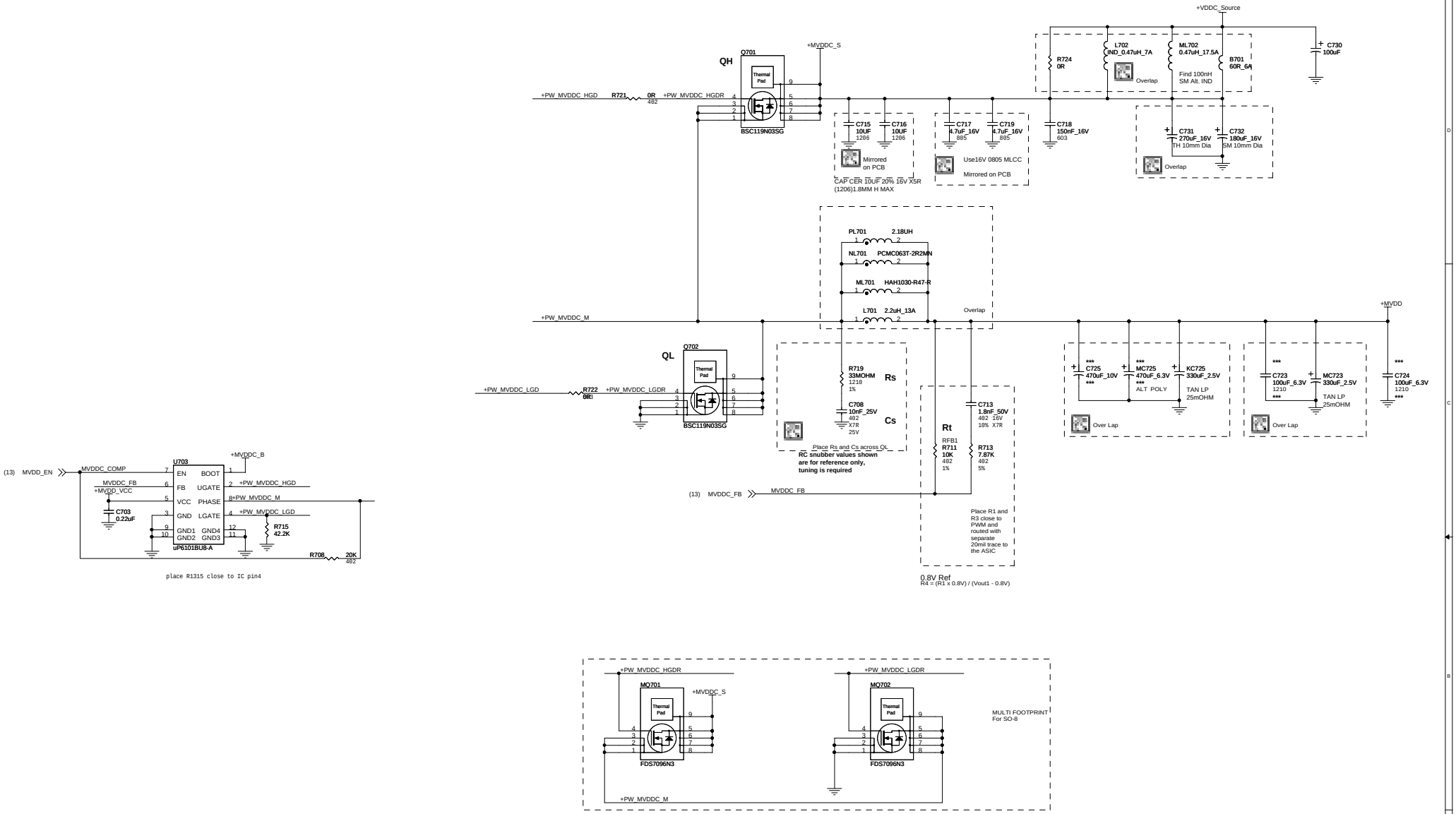
Title: RV635 DDR2 - VDDC SMPS 02

Doc No. 105-B382xx-10



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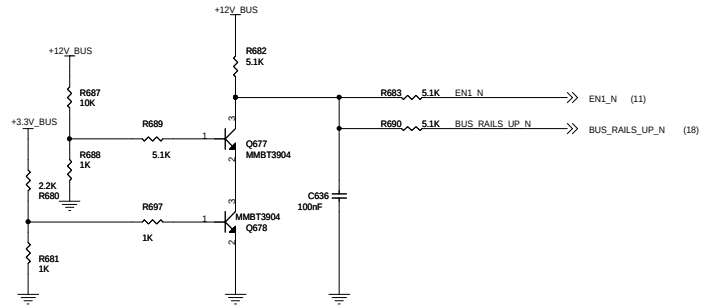
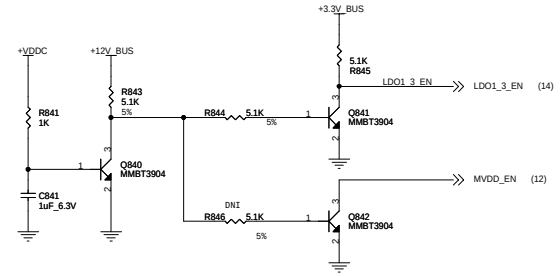
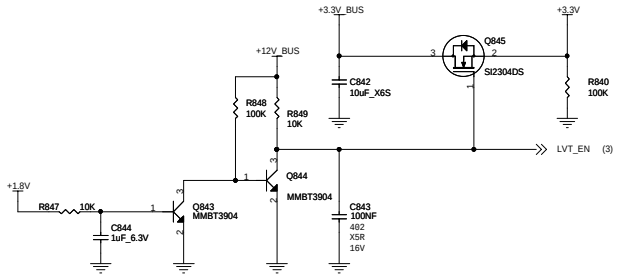
| Title | RV635 DDR2 - MVDD SMPS 01 |
| Doc No. | 105-B382xx-10 |

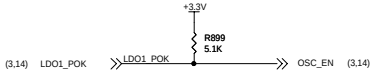
## Power up Sequencing



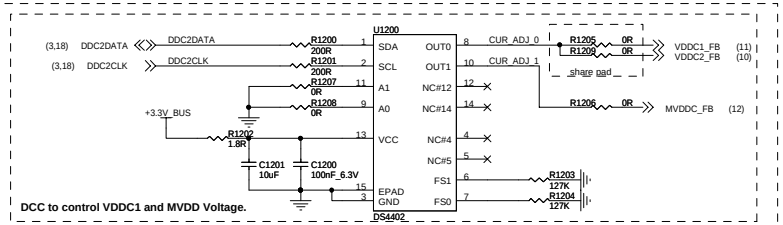

### VDDC Enable Circuit



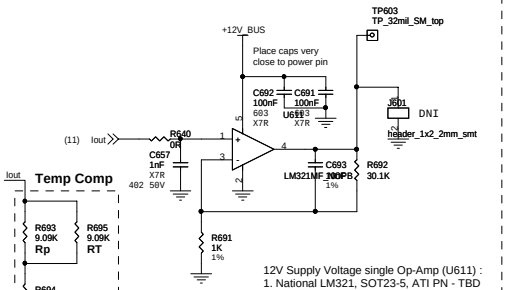




**Resistors to set the output voltages for +VDDC and +MVDDC**




DCC to control VDDC1 and MVDD Voltage.

### Buffered VDDC Output Current Monitoring



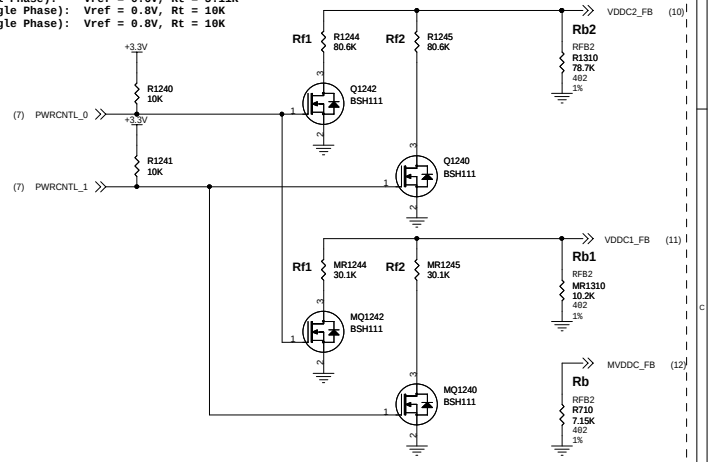

12V Supply Voltage single Op-Amp (U611) :
1. National LM321, SOT23-5, ATI PN - TBD
2. TI alternate? ATI PN - TBD

## Power Play

**VDDC Voltage Settings Using GPIOs (for VDDC1 Dual Phase)**

| PWRCNTL_1 GPIO_20 | PWRCNTL_0 GPIO_15 | Output Voltage (V) Rf1= Rf2= | Rf1= Rf2= | Rf1= Rf2= | |
|---|---|---|---|---|---|
| 0 | 0 | 0.90V | | | |
| 0 | 1 | 1.00V | | | |
| 1 | 0 | 1.00V | | | |
| 1 | 1 | 1.10 | | | Power-up Default |

Vout = Vref * (1+Rt/Rb)
VDDC1 (Dual Phase): Vref = 0.6V, Rt = 5.11K
VDDC2 (Single Phase): Vref = 0.8V, Rt = 10K
MVDDC (Single Phase): Vref = 0.8V, Rt = 10K



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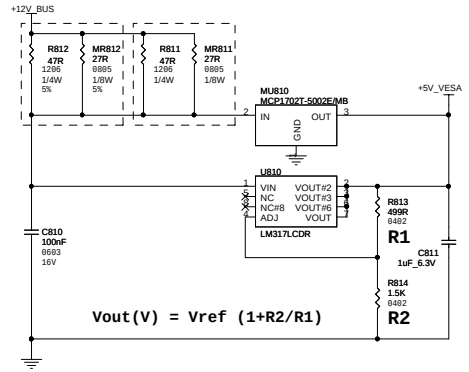
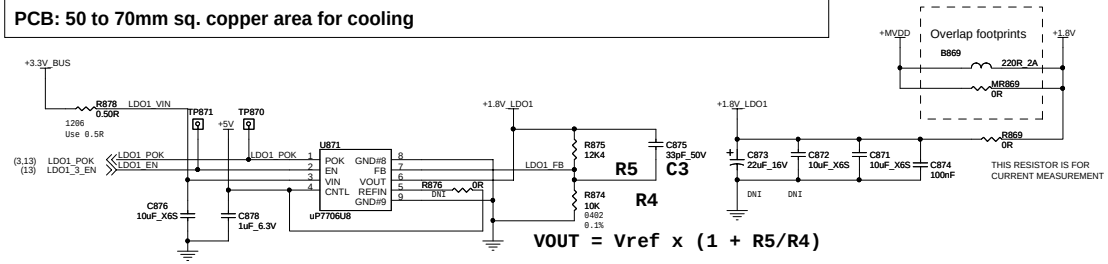
132-
For Testing purposes only

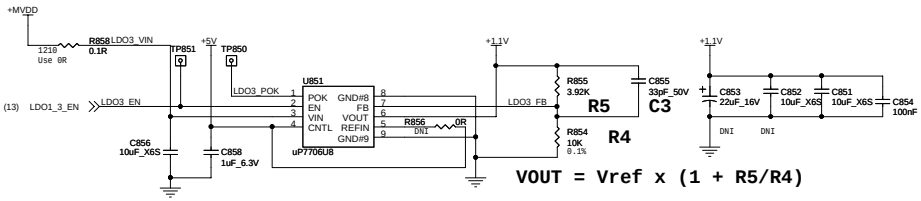
# Regulators for +5V, +5V_VESA and +5V_VESA2

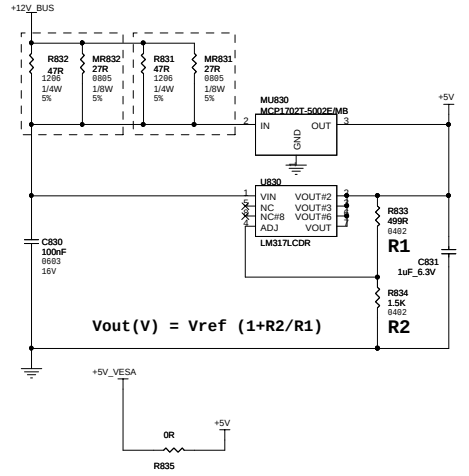



**LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX**
**PCB: 50 to 70mm sq. copper area for cooling**




**LDO #3: Vin = +1.45V to 2.0VMAX Vout = +1.1V +/- 2% Iout = 1.4A (TBV) RMS MAX**
**PCB: 50 to 70mm sq. copper area for cooling**



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See BOM for qualified filters

(3) A_DAC1_R — R1001 75R — C1004 8.0pF — L1001 47nH — R1024 0R — A_R_DAC1_M — C1001 12pF_50V — L1004 36NH

(3) A_DAC1_RB — R1027 37.4R

(3) A_DAC1_G — R1002 75R — C1005 8.0pF — L1002 47nH — R1025 0R — A_G_DAC1_M — C1002 12pF_50V — L1005 36NH

(3) A_DAC1_GB — R1028 37.4R

(3) A_DAC1_B — R1003 75R — C1006 8.0pF — L1003 47nH — R1026 0R — A_B_DAC1_M — C1003 12pF_50V — L1006 36NH

(3) A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

For ESD Protection

+3.3V — D1001 CM1213-04 — +5V_VESA — D1002 CM1213-04

+5V_VESA — B1012 30R_3A — R1012 0R — +5V_DAC1_VESA

Overlap pads

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

MJ1001

| | |
|---|---|
| 1 | R |
| 2 | G |
| 3 | B |
| 11 | MS0 — DDC2_MONID0 |
| 12 | MS1 — DDC2_MONID1(SDA) |
| 4 | MS2 — DDC2_MONID2 |
| 15 | MS3 — DDC2_MONID3(SCL) |
| 9 | NC |
| 13 | HS |
| 14 | VS |
| 5 | VSS |
| 6 | VSS#6 |
| 7 | VSS#7 |
| 8 | VSS#8 |
| 10 | VSS#10 |
| 16 | CASE |
| 17 | CASE#17 |

C1010 68pF 603

G3179C219-005

(3) CRT1DDCDATA — +3.3V — R1004 10K — +5V — R1005 2.2K — Q1001 BSH111 — DDCDATA_DAC1_5V — R1006 33R — DDCDATA_DAC1_R

(3) CRT1DDCCLK — +3.3V — R1007 10K — +5V — R1008 2.2K — Q1002 BSH111 — DDCCLK_DAC1_5V — R1009 33R — DDCCLK_DAC1_R

| DB15 pin | Standard VGA | DDC1 Host | DDC2B or DDC2B+ Host | DDC2AB Host | DDC1/2 Display |
|---|---|---|---|---|---|
| 11 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Optional |
| 12 | Monitor ID bit 1 | Data from display | SDA | SDA | SDA |
| 4 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Optional |
| 15 | Monitor ID bit 3 | Open | SCL | SCL | SCL |
| | | +5V | +5V | +5V | |
| 9 | N/C | 50mA min | 50mA min | 300mA min | Optional |
| Hardware | Mechanical Key | 1A max | 1A max | 1A max | |
| Support | No | Yes | Yes | No | Yes |

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

U1999A — C1999 100nF_6.3V — +5V

(3,7) HSYNC_DAC1 — HSYNC_DAC1_B — R1010 10R — HSYNC_DAC1_R — C1007 12pF_50V

U1999B

(3,7) VSYNC_DAC1 — VSYNC_DAC1_B — R1011 10R — VSYNC_DAC1_R — C1008 12pF_50V

74VHC125

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

U1999C — U1999D — 74VHC125

(7) HPD2 — Q1021 MMBT3904 — +3.3V — R1022 10K — HPD_DVI2 — R1023 10K

+5V_DAC1_VESA

(3) T2X2M — TMDS Data2-
(3) T2X2P — TMDS Data2+
TMDS Data2/4 Shield
(3) T2X4M — TMDS Data4-
(3) T2X4P — TMDS Data4+
DDCCLK_DAC1_R — DDC Clock
DDCDATA_DAC1_R — DDC Data
VSYNC_DAC1_R — Analog VSYNC
(3) T2X1M — TMDS Data1-
(3) T2X1P — TMDS Data1+
TMDS Data1/3 Shield
(3) T2X3M — TMDS Data3-
(3) T2X3P — TMDS Data3+
+5V Power
GND (for +5V)
Hot Plug Detect
(3) T2X0M — TMDS Data0-
(3) T2X0P — TMDS Data0+
TMDS Data0/5 Shield
(3) T2X5M — TMDS Data5-
(3) T2X5P — TMDS Data5+
TMDS Clock Shield
(3) T2XCP — TMDS Clock+
(3) T2XCM — TMDS Clock-
A_R_DAC1_F — Analog Red
A_G_DAC1_F — Analog Green
A_B_DAC1_F — Analog Blue
HSYNC_DAC1_R — Analog HYNC
Analog GND
Analog GND#C6
CASE#26
CASE#27
CASE#28
CASE#29
CASE#30

J1001 — CASE — DVI_CONNECTOR



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Title: RV635 DDR2 - DAC1&TMDS2

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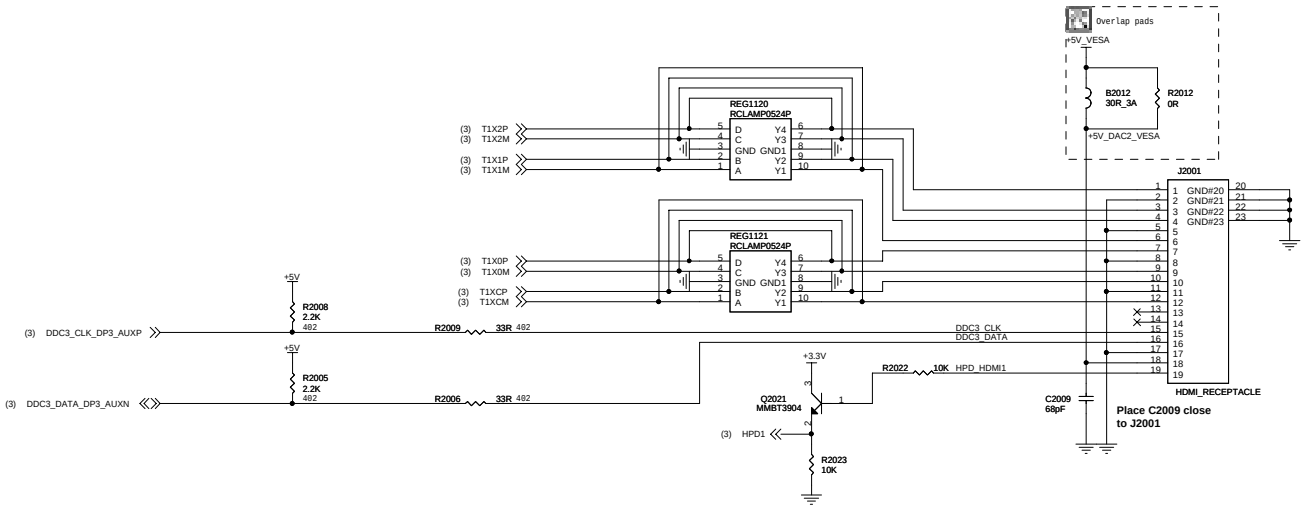




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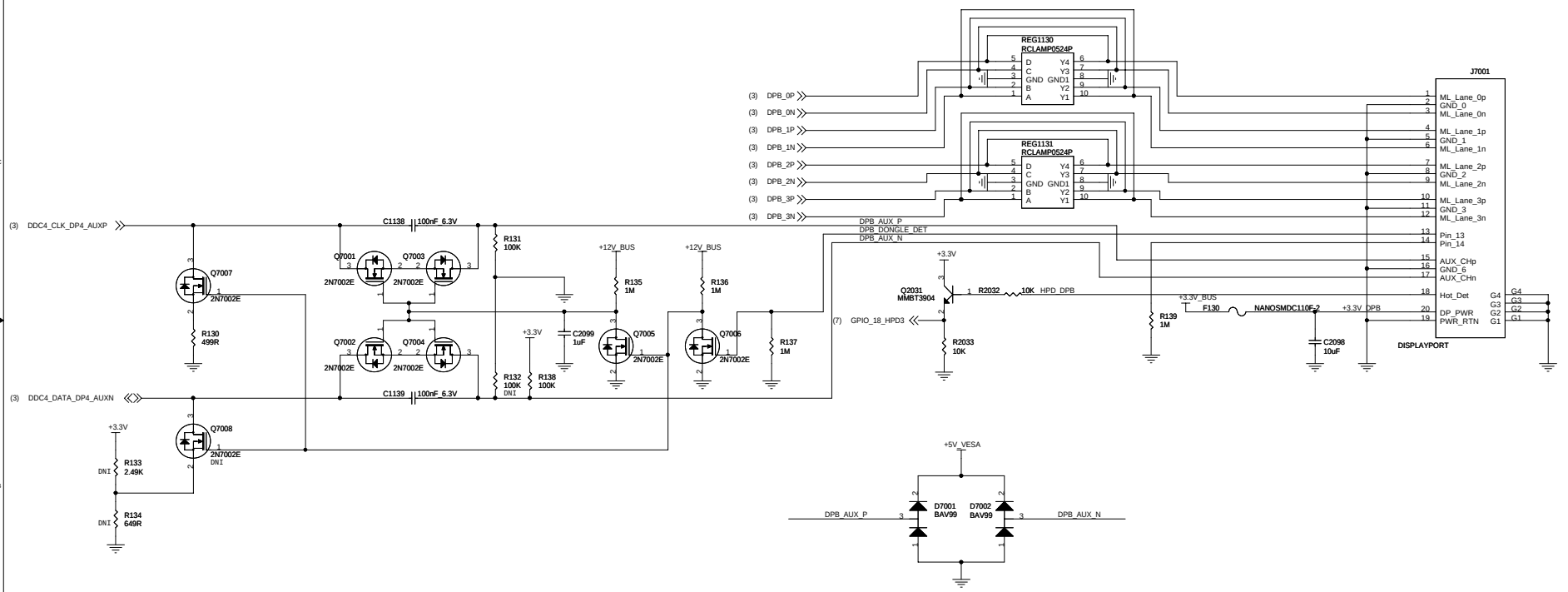
Title RV635 DDR2 - HDMI1

Doc No. 105-B382xx-10



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LM63 is for BU only, until built-in fan controller is verified.

Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

Not intended for production
LED off shows the fault

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board.

Bypass Switch
(not for production)

For 2-WIRE FAN ONLY

For 4-WIRE FAN ONLY

Header is 2mm, and it does not follow 2.54mm spacing as 4-pin PWM Fan Specification

Overlap MJ4030 and J4030

DNI (bypass for fan with 3.3V PWM)

For testing purposes only

See BOM for qualified option.

USE FANSINK FOR RV635 DDR2, p/n 7120036100G or (7122035100G)



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Title RV635 DDR2 - Thermal Management

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DVI/DVI SCREWS with top tab

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

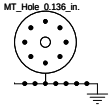
ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET
8020046100G

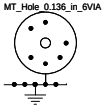
**Need New Bracket**

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

MT1
MT_Hole_0.136_in.



MT2
MT_Hole_0.136_in_6VIA



DNI

SK1
SOCKET_880

**RV635 Socket**

PCB1
PCB
109-GN982-00A



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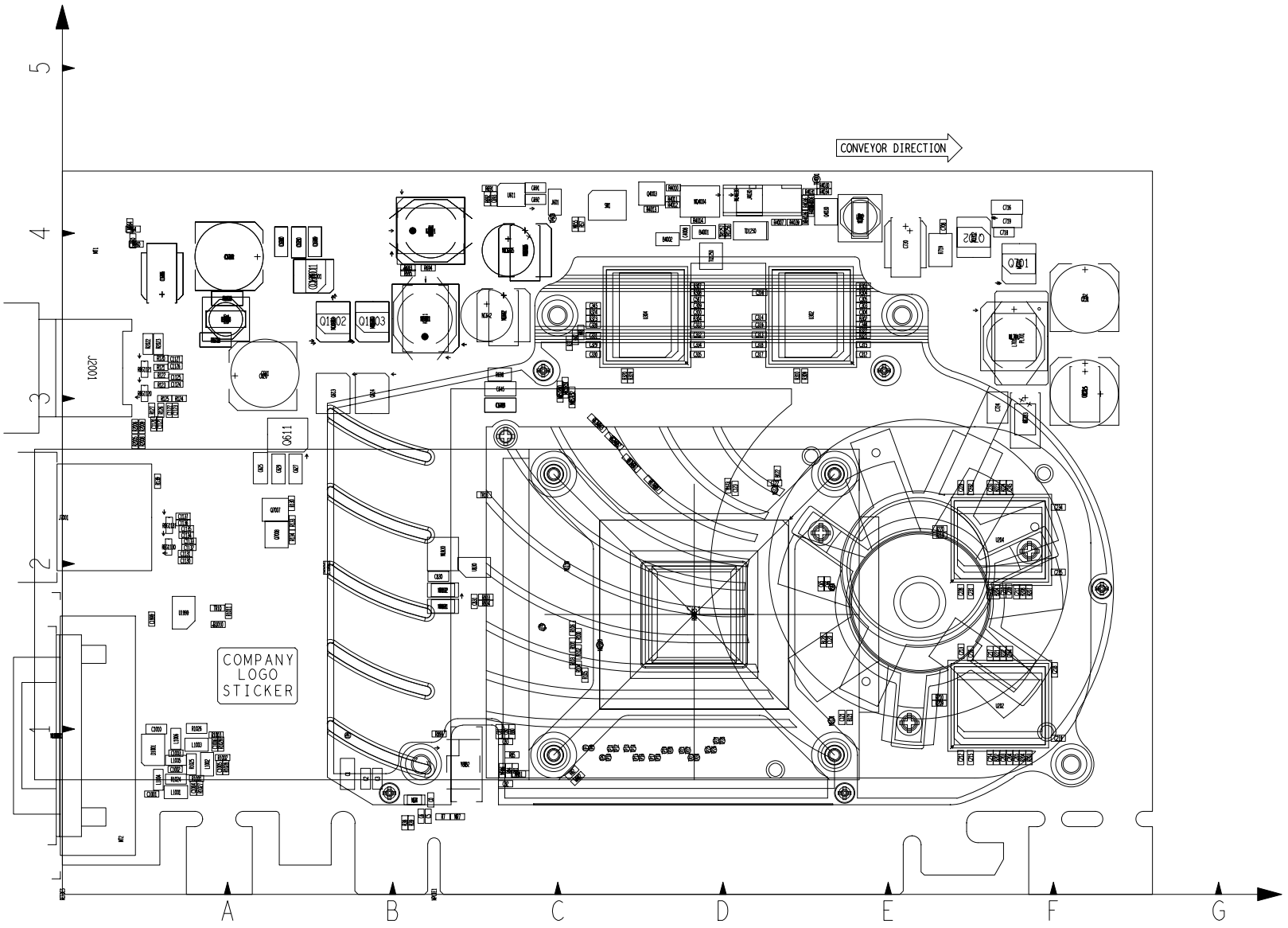


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|---|---|
| AMD<br>ADVANCED MICRO DEVICES<br>PCBCAD GROUP | RH RV635 512MB DDR2 DL-DVI DP HDMI FH 6<br><br>P/N 109-B38231-10<br>JANUARY 7, 2008 ASSEMBLY TOP<br>DORINA ABRAMOVICI SHEET 1 OF 2 |

| | |
|---|---|
| ADVANCED MICRO DEVICES<br>PCBCAD GROUP | RH RV635 512MB DDR2 DL-DVI DP HDMI FH 6<br><br>P/N 109-B38231-10<br>JANUARY 7, 2008<br>DORINA ABRAMOVICI |