

P141-A03, NV31/NV34/NV18B
4(8,16)Mx16, 64(128,256)MB, VIDEO IN/OUT, DVI-I, VGA

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HISTORY:

A00

- X00: INITIAL VERSION
- X01: First Review
 - Replaced series resistors in sync lines with 33ohms
 - Moved clamping diodes next to GPU
 - Added parallel caps to EMI filter DACB
 - Removed not needed strap on SAA7114
 - Connected RESET and WP of SST ROM to ROMVCC
 - Added parallel ROM and Strapps
 - Added FBVDD regulator
 - Added STEREO glasses circuit
 - Removed Decoupling CAPs on VIP VDD, covered by Caps on page 2
 - Added ROM_VCC for cleaner planes
 - Changed used TMDS lines of IFPA and IFPB to TP from NTP
 - Changed Resistor for AGP Vref circuit to 158k
- X02: Final Review
 - Added clock termination resistors
 - Added net name for FBxALxxx
 - Added cap on filter input for FB_DLLVDD, DACA_VDD & DACB_VDD
 - Changed netnames for SAA7114 NTPs to NTP_xxx
 - Added 1uF cap parallel to fan connector
 - Changed all xxCALxx resistors to 50 Ohms
 - Changed all FBxDQS*-<x> to NTP_FBxDQS*-<x> with NO_TEST property

A01

- X00: Fixed pin swap on parallel ROM A12 & A13
 - Added charge pump for SC2612
 - Added resistors to swap GPIO for DACB loadtest
 - Added resistors for I2C on internal Video IN connector
- X01: Updated variant information for new Sbom structure

A02

- X00: Added sw adjust for NVVDD
 - Exchanged TMDSIOVDD regulator to lower the voltage drop
 - Changed TMDSPLLVDD regulator bypass to A3V3
 - Addrd 1k series resistor in DACB load detection circuit

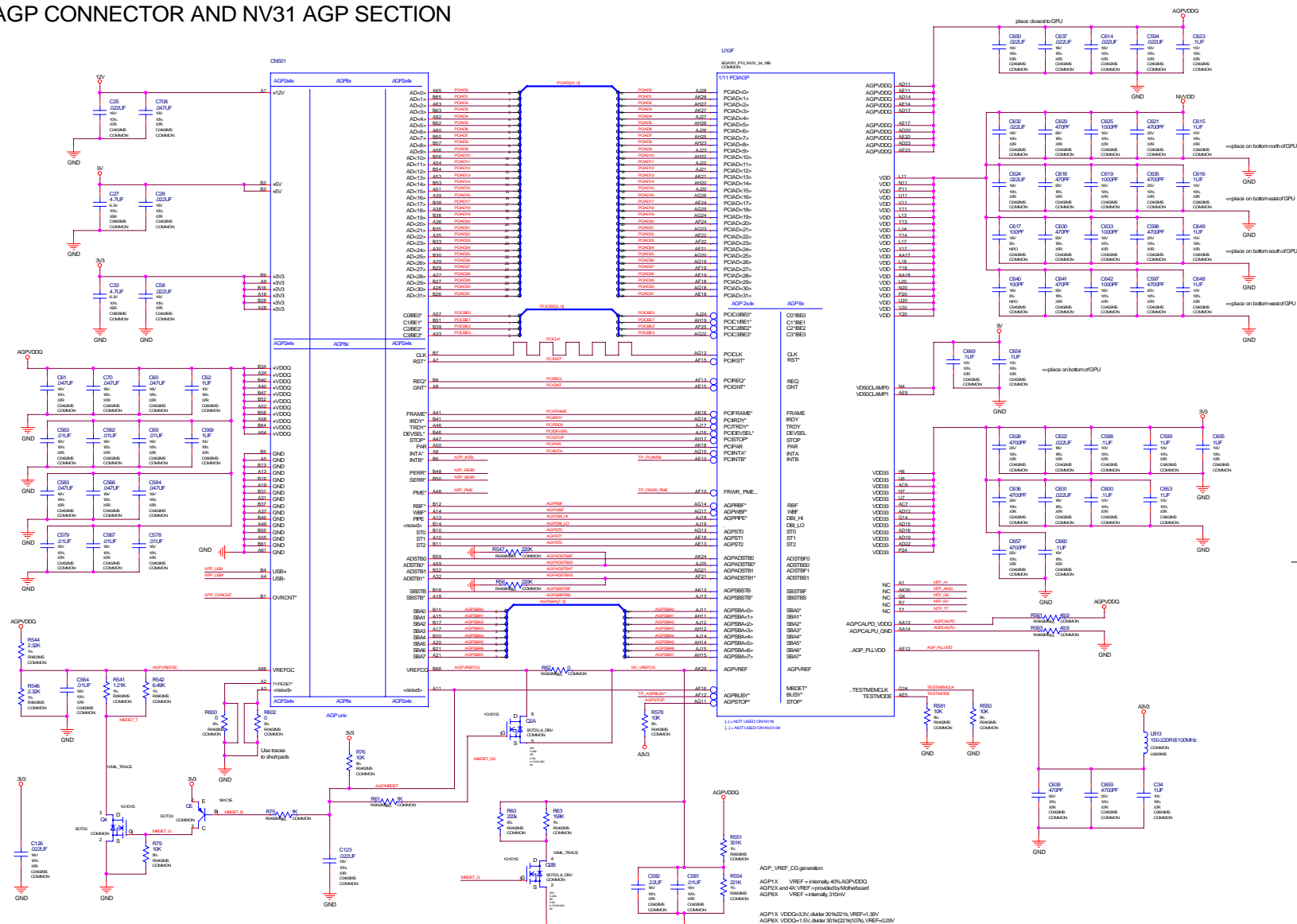
A03

- X00: Removed GPIO5 from NVVDD adjust
 - Fixed values for DAC Rset resitors
 - Removed Sync Buffer bypass
 - Removed 2nd voltage selection fet
 - Changed to new internal video connector
 - Added snubber to NVVDD and FBVDD regulator

8912 version 00B base on P141-A03 Modify.
1.Remove Page 13 MiniDim and Add AV-out connector.
2.Change all R,C,L parts to MSI footprint.

602-10141-0000-000 Base Schematic

AGP CONNECTOR AND NV31 AGP SECTION

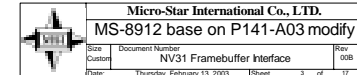
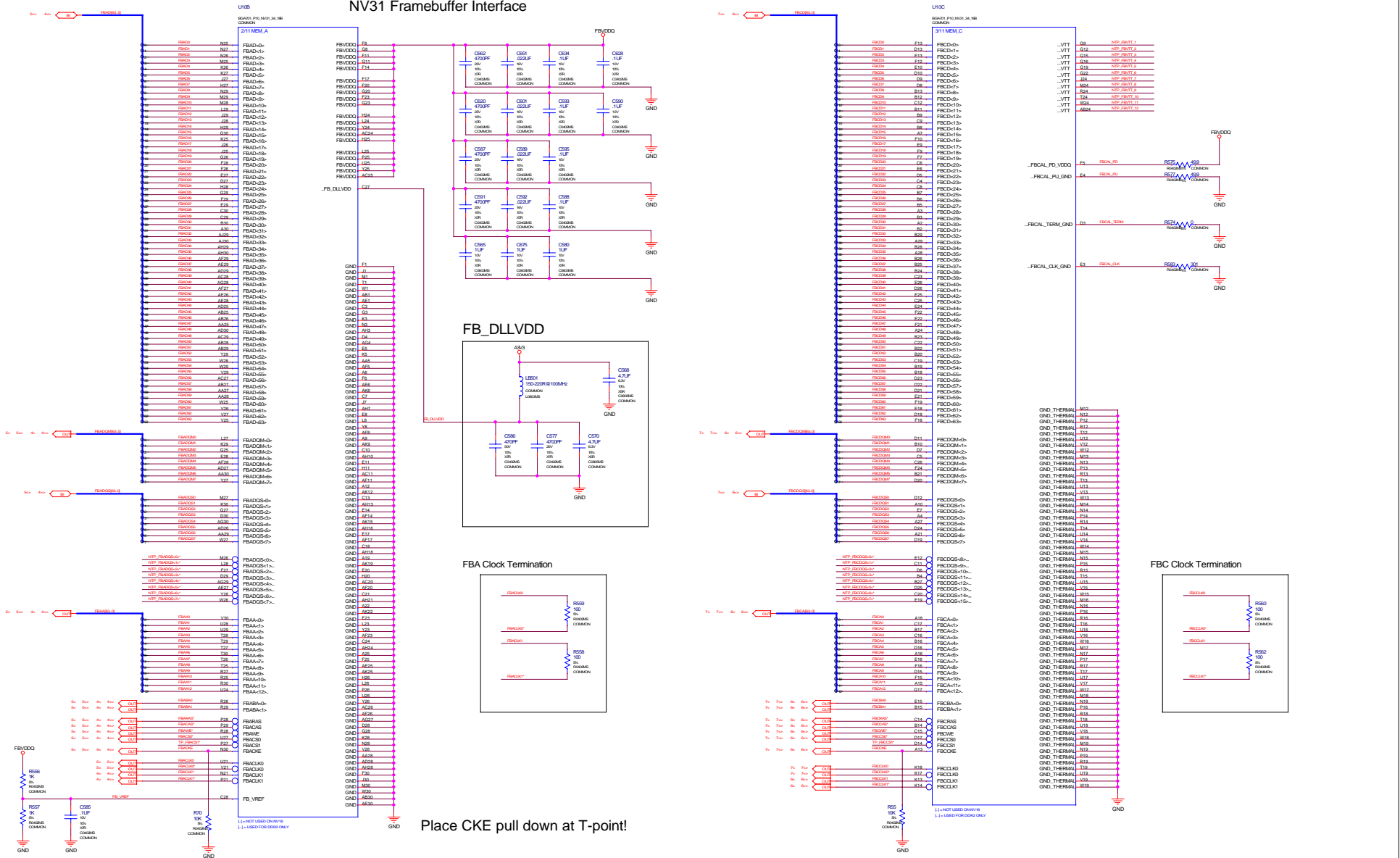


AGP rules

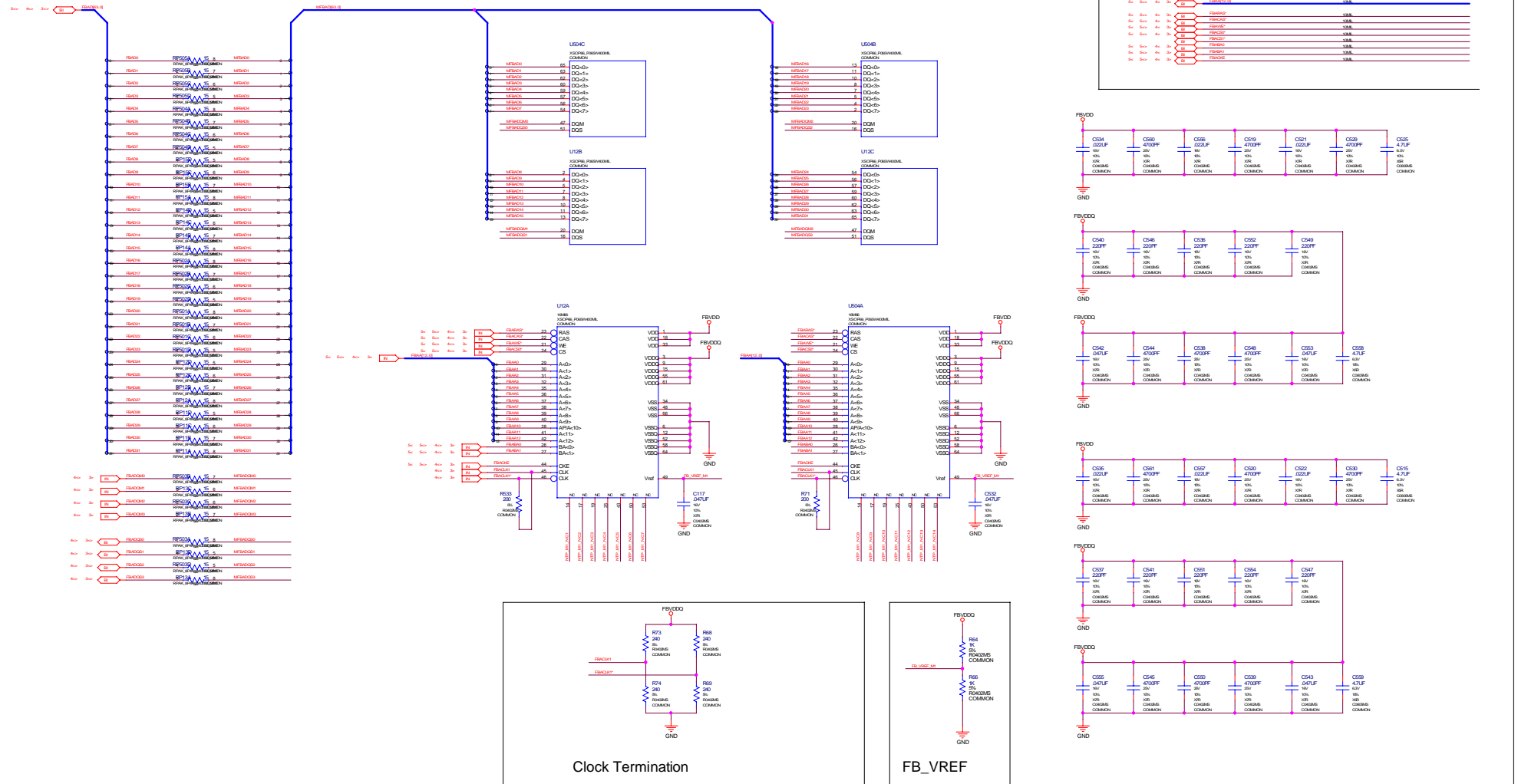
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Micro-Star International Co., LTD.			
MS-8912 base on P141-A03 modify			
Size	Document Number		Rev
Custom	AGP CONNECTOR AND NV31 AGP SECTION		00B
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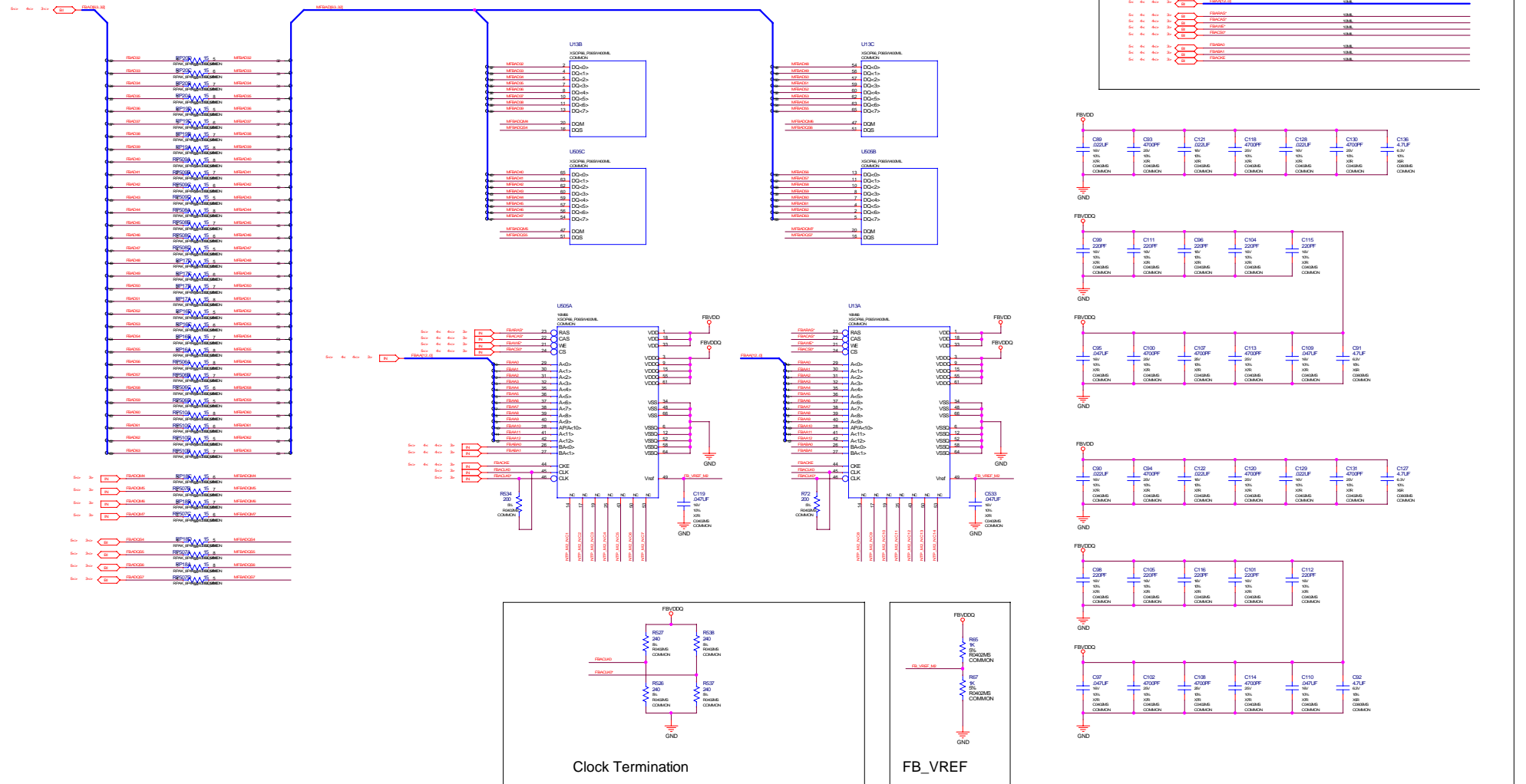
NV31 Framebuffer Interface



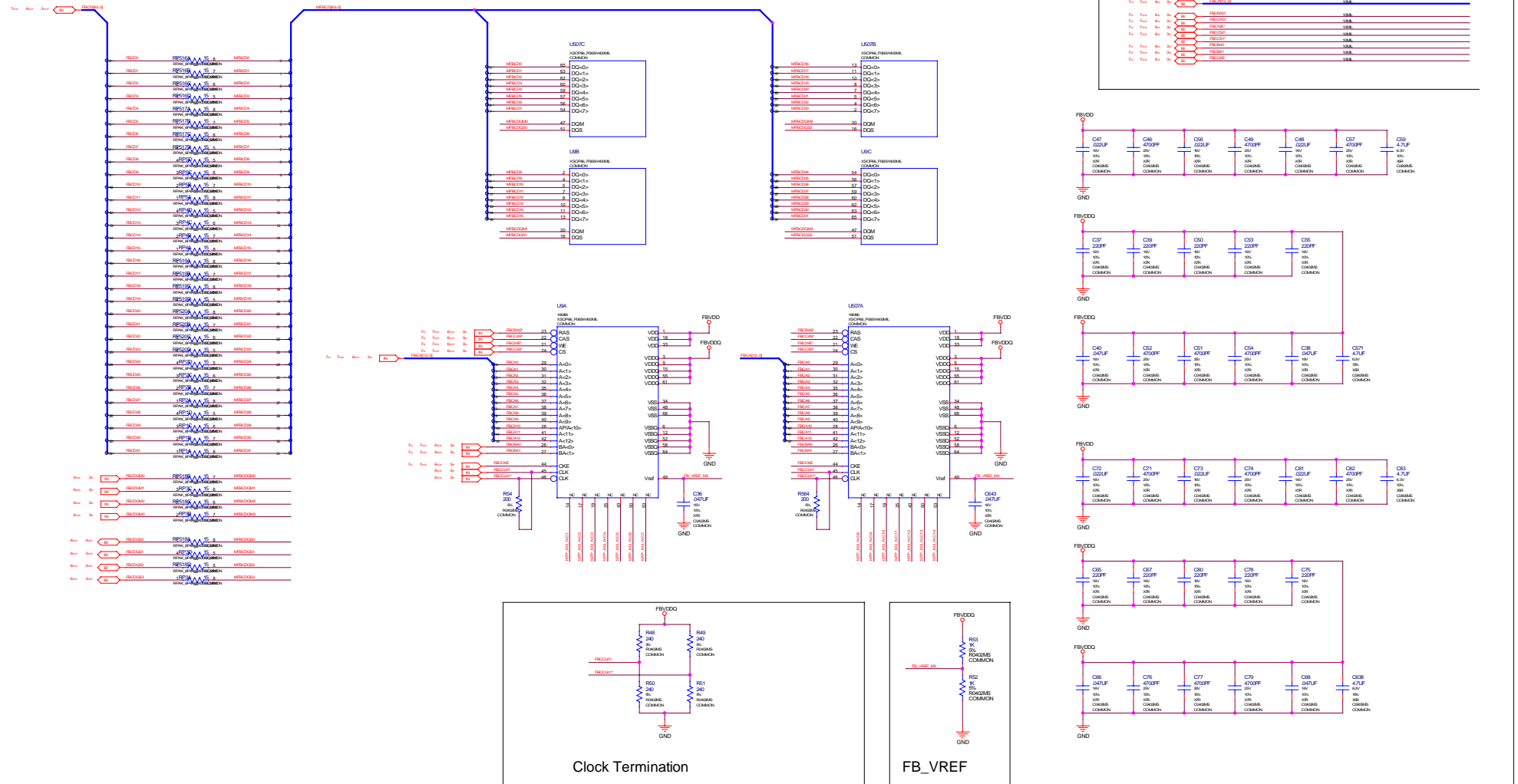
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



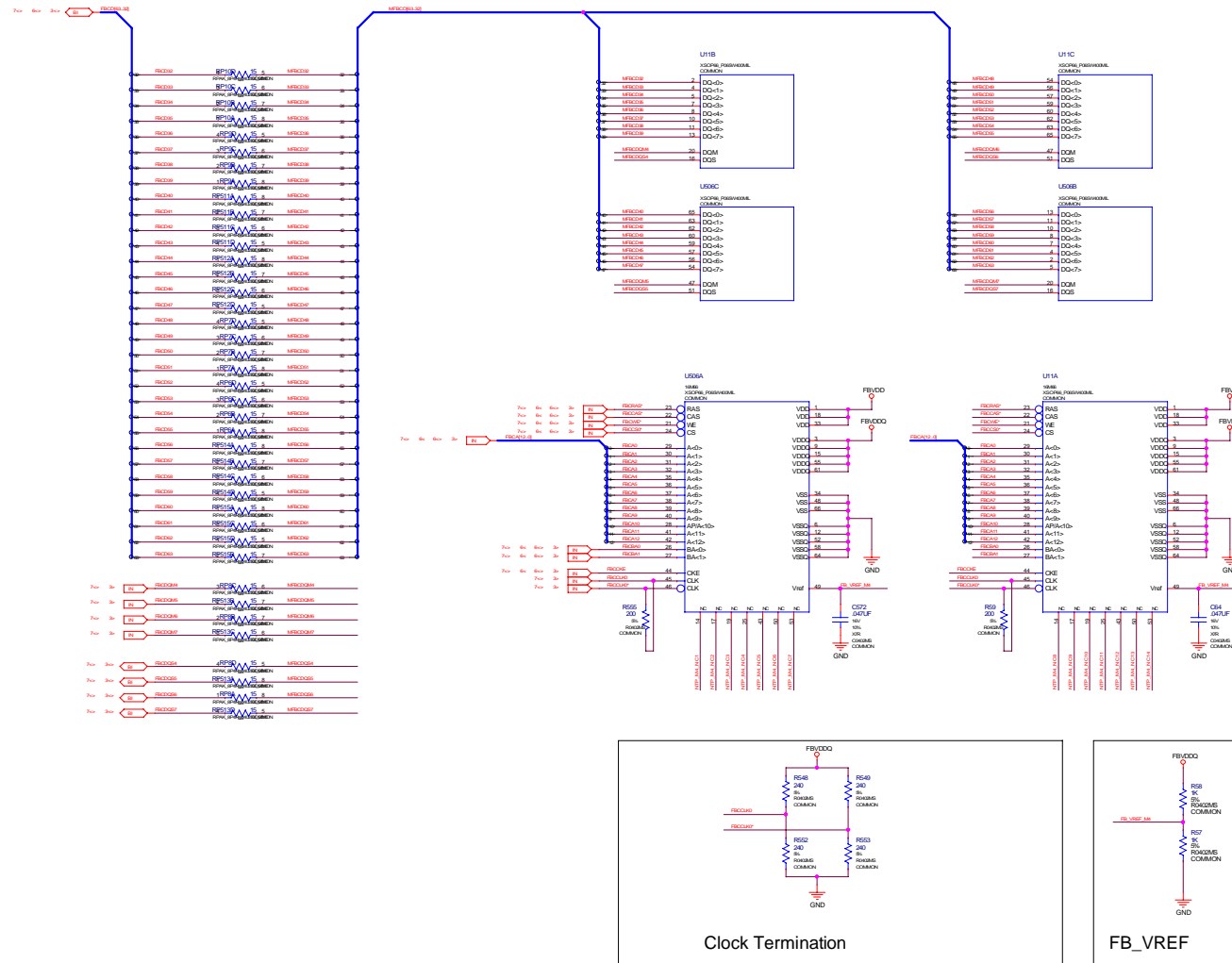
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

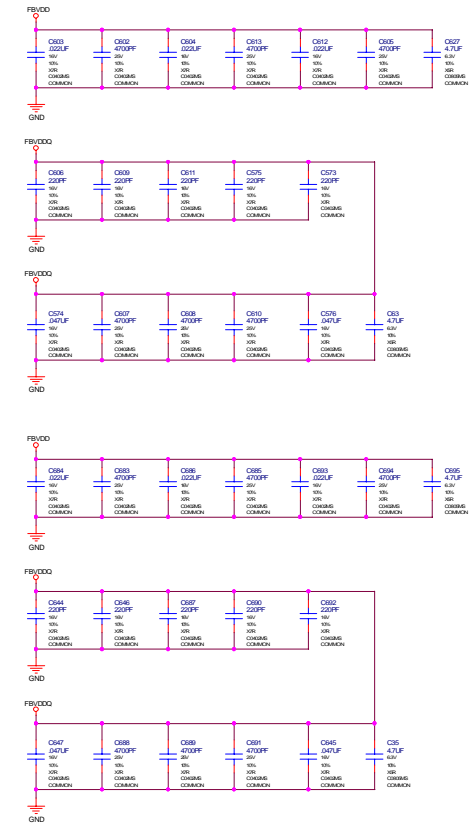
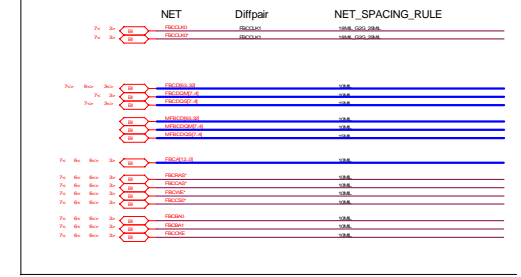


PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



Clock Termination

FB_VREF



Micro-Star International Co., LTD.

MS-8912 base on P141-A03 modify

Size Document Number

Custom MEMORY 8(16)Mx16DDR Partition C , Bits 32..63

Date Thursday, February 13, 2003 Sheet 7 of 17

[illegible]

The schematic diagram illustrates the DAC section of the AD9434 evaluation board. It features a 100MHz oscillator (L6688) driving a chain of dividers (CD74, CD75, CD80, CD79, CD86) to generate clocks for DACs 0-3. DACs 0-2 are configured as 10-bit DACs, while DAC 3 is a 12-bit DAC. The DAC outputs are connected to a 10-bit DAC core (DAC0-3) and a 12-bit DAC core (DAC0-3). The DAC outputs are connected to a 10-bit DAC core (DAC0-3) and a 12-bit DAC core (DAC0-3). The DAC outputs are connected to a 10-bit DAC core (DAC0-3) and a 12-bit DAC core (DAC0-3).

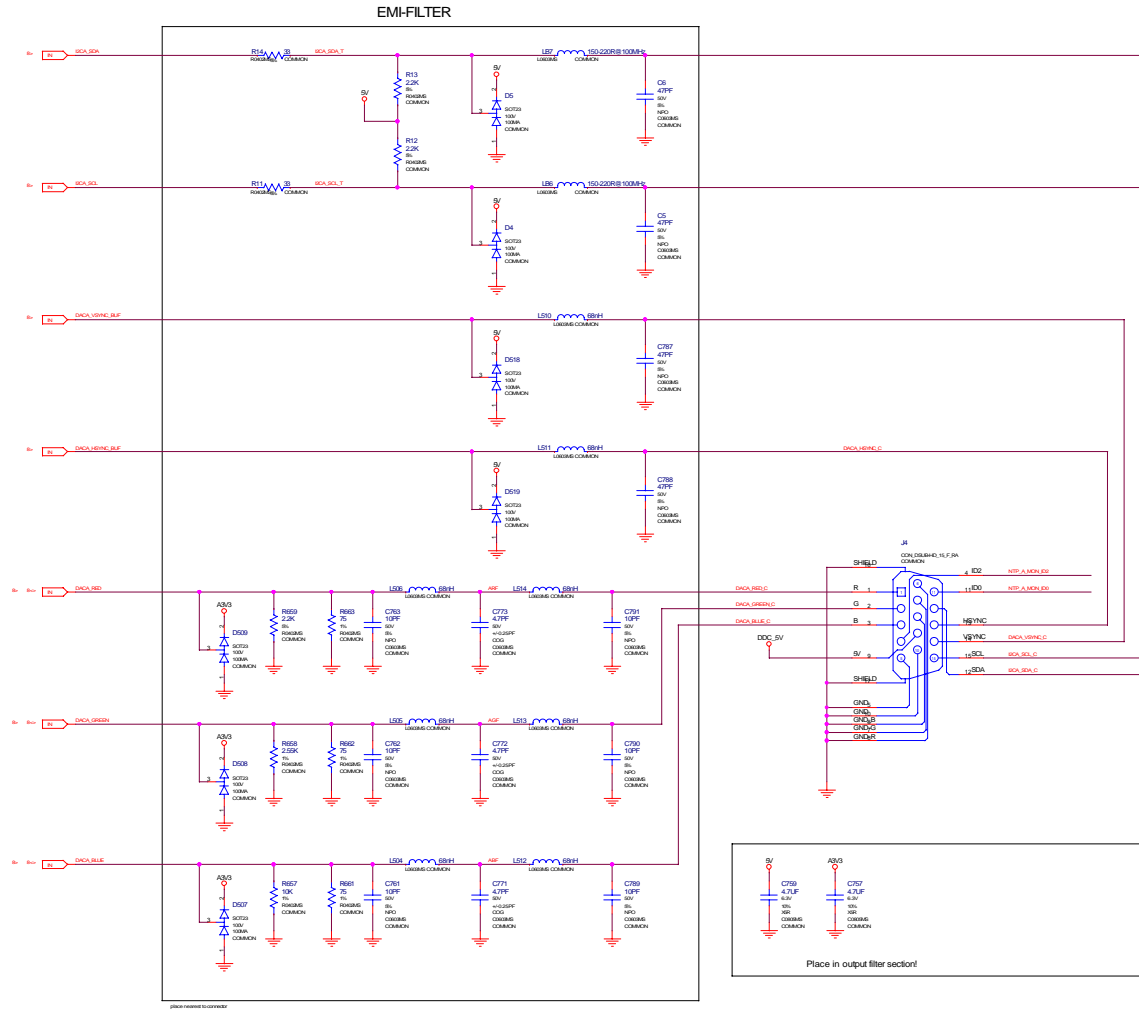
The diagram shows four 74181 ALUs connected in parallel to perform a 4-bit addition. Each ALU is configured with inputs A and B as 1s and 0s, and carry-in as 0. The outputs are summed to produce a 4-bit result.

- ALU1:** Inputs A=1, B=0, Carry-in=0. Output is 101.
- ALU2:** Inputs A=1, B=0, Carry-in=0. Output is 101.
- ALU3:** Inputs A=1, B=0, Carry-in=0. Output is 101.
- ALU4:** Inputs A=1, B=0, Carry-in=0. Output is 101.

The final 4-bit result is 1011.

Primary Display (DACA), DB15 only!

NET	NET_SPACING_RULE
ASF	200R_GGG_X3R
ASF	200R_GGG_X3R
ASF	200R_GGG_X3R
ENCA RED (C)	200R_GGG_X3R
ENCA GREEN (C)	200R_GGG_X3R
ENCA BLUE (C)	200R_GGG_X3R



Place all filter components
on the side nearest to the
reference GND plane!

Route all signals only on
layers referenced to GND!

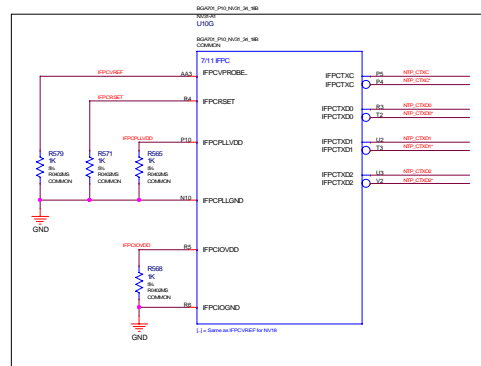
Don't split the reference
GND plane beneath
a RGB signal!

Place all filter components
on the side nearest to the
reference GND plane!

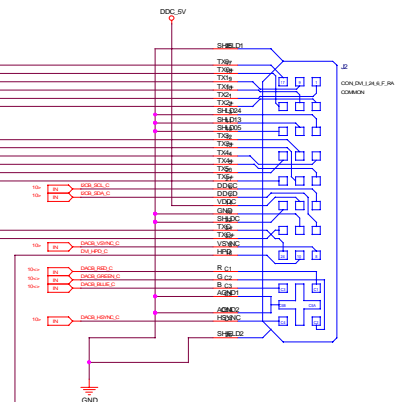
Don't split the reference
GND plane beneath
a RGB signal!

Pin	Signal	Function
1	CS	Chip Select
2	CS	Chip Select
3	CS	Chip Select
4	CS	Chip Select
5	CS	Chip Select
6	CS	Chip Select
7	CS	Chip Select
8	CS	Chip Select
9	CS	Chip Select
10	CS	Chip Select
11	CS	Chip Select
12	CS	Chip Select
13	CS	Chip Select
14	CS	Chip Select
15	CS	Chip Select
16	CS	Chip Select
17	CS	Chip Select
18	CS	Chip Select
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22	CS	Chip Select
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134	CS	Chip Select
1		

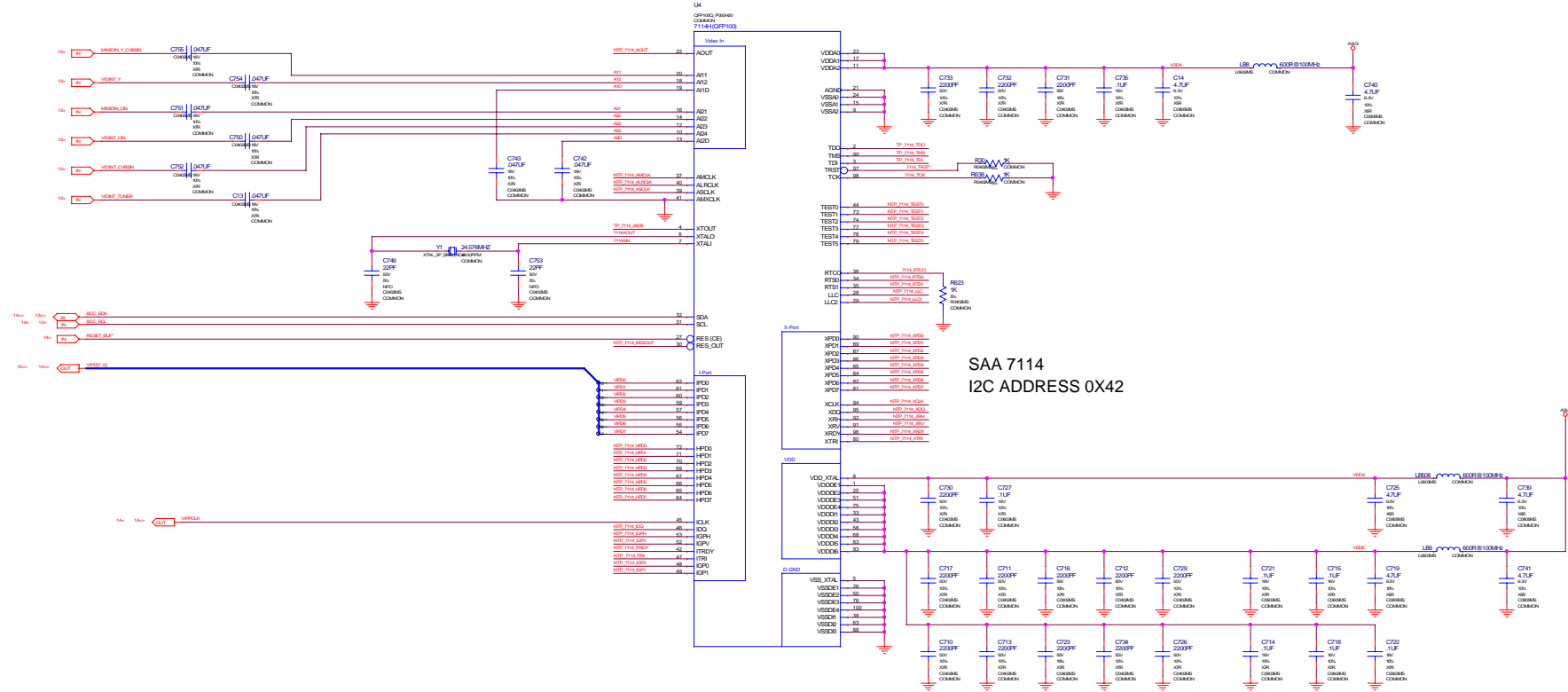
Unused Transmitter



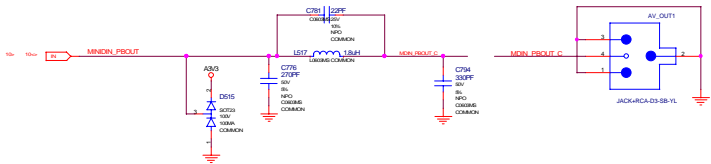
	NET	NET_PHYSICAL_TYPE	VOLTAGE
	STPM402	1.8K_20K	1.8V
	STPM403	1.8K_20K	1.8V
	STPM404	1.8K_20K	1.8V
	STPM405	1.8K_20K	1.8V
	STPM406	1.8K_20K	1.8V
	STPM407	1.8K_20K	1.8V
	STPM408	1.8K_20K	1.8V
	STPM409	1.8K_20K	1.8V
	STPM410	1.8K_20K	1.8V
	STPM411	1.8K_20K	1.8V
	STPM412	1.8K_20K	1.8V
	STPM413	1.8K_20K	1.8V
	STPM414	1.8K_20K	1.8V
	STPM415	1.8K_20K	1.8V
	STPM416	1.8K_20K	1.8V
	STPM417	1.8K_20K	1.8V
	STPM418	1.8K_20K	1.8V
	STPM419	1.8K_20K	1.8V
	STPM420	1.8K_20K	1.8V
	STPM421	1.8K_20K	1.8V
	STPM422	1.8K_20K	1.8V
	STPM423	1.8K_20K	1.8V
	STPM424	1.8K_20K	1.8V
	STPM425	1.8K_20K	1.8V
	STPM426	1.8K_20K	1.8V
	STPM427	1.8K_20K	1.8V
	STPM428	1.8K_20K	1.8V
	STPM429	1.8K_20K	1.8V
	STPM430	1.8K_20K	1.8V
	STPM431	1.8K_20K	1.8V
	STPM432	1.8K_20K	1.8V
	STPM433	1.8K_20K	1.8V
	STPM434	1.8K_20K	1.8V
	STPM435	1.8K_20K	1.8V
	STPM436	1.8K_20K	1.8V
	STPM437	1.8K_20K	1.8V
	STPM438	1.8K_20K	1.8V
	STPM439	1.8K_20K	1.8V
	STPM440	1.8K_20K	1.8V
	STPM441	1.8K_20K	1.8V
	STPM442	1.8K_20K	1.8V
	STPM443	1.8K_20K	1.8V
	STPM444	1.8K_20K	1.8V
	STPM445	1.8K_20K	1.8V
	STPM446	1.8K_20K	1.8V
	STPM447	1.8K_20K	1.8V
	STPM448	1.8K_20K	1.8V
	STPM449	1.8K_20K	1.8V
	STPM450	1.8K_20K	1.8V
	STPM451	1.8K_20K	1.8V
	STPM452	1.8K_20K	1.8V
	STPM453	1.8K_20K	1.8V
	STPM454	1.8K_20K	1.8V
	STPM455	1.8K_20K	1.8V
	STPM456	1.8K_20K	1.8V
	STPM457	1.8K_20K	1.8V
	STPM458	1.8K_20K	1.8V
	STPM459	1.8K_20K	1.8V
	STPM460	1.8K_20K	1.8V
	STPM461	1.8K_20K	1.8V
	STPM462	1.8K_20K	1.8V
	STPM463	1.8K_20K	1.8V
	STPM464	1.8K_20K	1.8V
	STPM465	1.8K_20K	1.8V
	STPM466	1.8K_20K	1.8V
	STPM467	1.8K_20K	1.8V
	STPM468	1.8K_20K	1.8V
	STPM469	1.8K_20K	1.8V
	STPM470	1.8K_20K	1.8V
	STPM471	1.8K_20K	1.8V
	STPM472	1.8K_20K	1.8V
	STPM473	1.8K_20K	1.8V
	STPM474	1.8K_20K	1.8V
	STPM475	1.8K_20K	1.8V
	STPM476	1.8K_20K	1.8V
	STPM477	1.8K_20K	1.8V
	STPM478	1.8K_20K	1.8V
	STPM479	1.8K_20K	1.8V
	STPM480	1.8K_20K	1.8V
	STPM481	1.8K_20K	1.8V
	STPM482	1.8K_20K	1.8V
	STPM483	1.8K_20K	1.8V
	STPM484	1.8K_20K	1.8V
	STPM485	1.8K_20K	1.8V
	STPM486	1.8K_20K	1.8V
	STPM487	1.8K_20K	1.8V

[illegible]

VIDEO CAPTURE

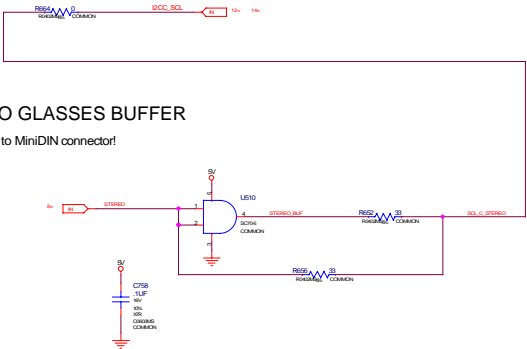


VIDEO IN/OUT CONNECTOR /STEREO GLASSES

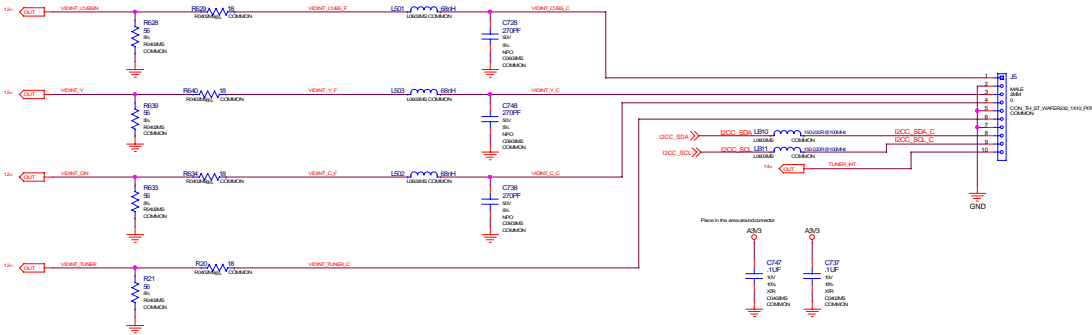


STEREO GLASSES BUFFER

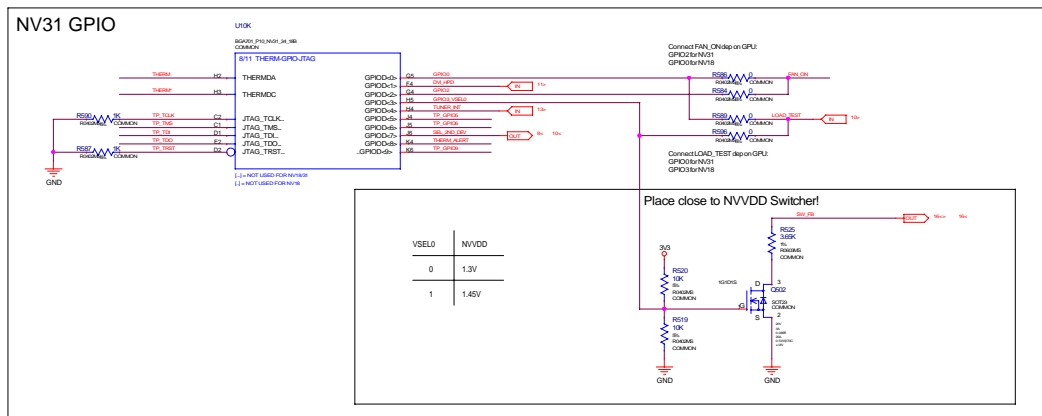
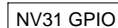
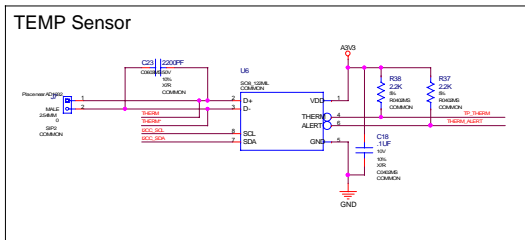
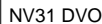
Place close to MiniDIN connector!



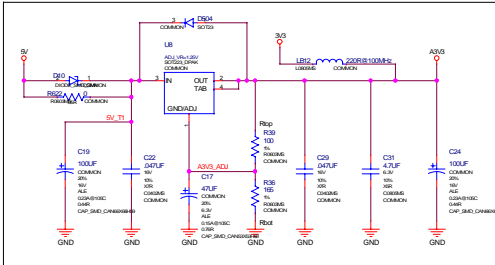
INTERNAL VIDEO IN CONNECTOR



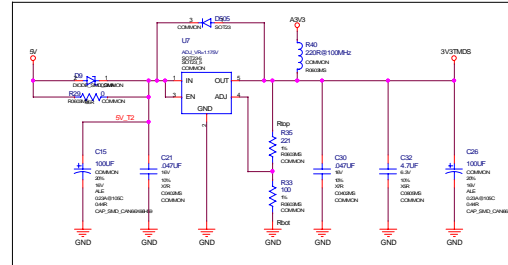
NV31 VIP



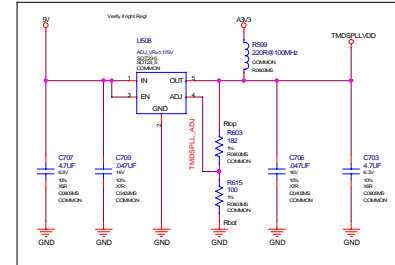
ANALOG 3V3




TMDS 3V3 Supply



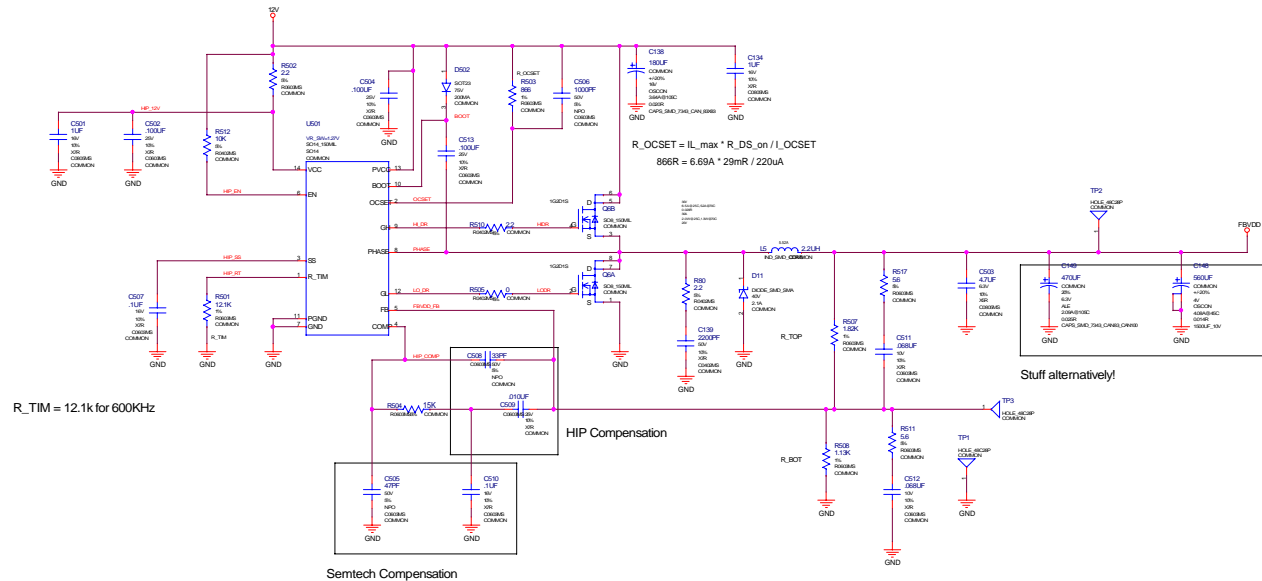
TMDS PLL Supply



[illegible]

	Micro-Star International Co., LTD.		
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FBVDD Switcher (3.3V out of 12V Rail)



$$FBVDD = V_{Ref} * (1 + R_{top} / R_{bot})$$

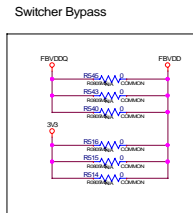
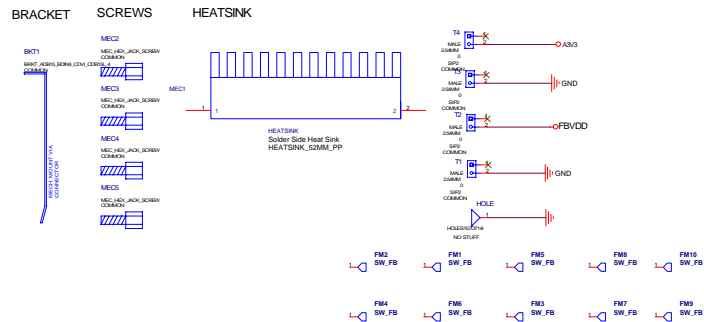
$$3.29V = 1.270V * (1 + 1.82K / 1.13K)$$

$$2.5V = 1.270V * (1 + 1K / 1.02k)$$

$$3.34V = 0.8V * (1 + 3.32K / 1.07K)$$

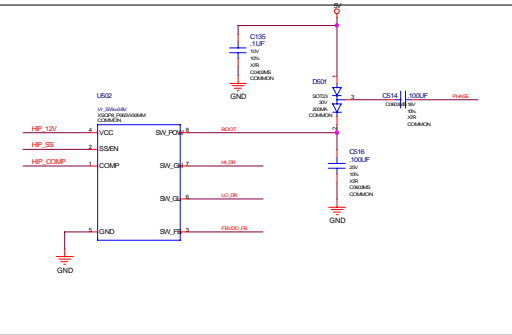
$$2.5V = 0.8V * (1 + 2.37K / 1.02K)$$

MECHANICAL COMPONENTS



NET		NET_PHYSICAL_TYPE
EN	14.120	10MR_TRACK
EN	15.120	10MR_TRACK
EN	16.120	10MR_TRACK
EN	17.120	10MR_TRACK
EN	18.120	10MR_TRACK
EN	19.120	10MR_TRACK
EN	20.120	10MR_TRACK
EN	21.120	10MR_TRACK
EN	22.120	10MR_TRACK
EN	23.120	10MR_TRACK
EN	24.120	10MR_TRACK
EN	25.120	10MR_TRACK
EN	26.120	10MR_TRACK
EN	27.120	10MR_TRACK
EN	28.120	10MR_TRACK
EN	29.120	10MR_TRACK
EN	30.120	10MR_TRACK
EN	31.120	10MR_TRACK

Semtech Sc2612
Stuff alternatively to ISL & HIP!



DDC 5V

