8988-00A(C277) DESIGN

PAGE SUMMARY:

8981 Ver : 00A modify P229-B01 Summary

Page 11. Add Video in connect to mini-din 10 pin & remove J5.

Page 12. Add DVI-I common choke.

Page 13. Connect net MIOBD 2 , MIOBD 6 & MIOBD 7 to BUS.

Page 15. Modify Power ,PWM change to ISL6549.

Page 16. Add Video function.

8988 Ver : 00A modify 8981-100 Summary

Page 02. Delete PCI-E connector

Page 15. Change 5V power supply to BR02VDD & Add sequence

Page 17,18,19,20. Add BR02 bradge circuit

8988 Ver : 00A BOM

SKU000:MSI 602-8988-A10 MS-8988 00A NV43/VGA/DVI-I/VHT-10/256M DDR (Hynix 16*16-4)

SKU001:MSI 602-8988-A20 MS-8988 00A OPT:A NV43/VGA/DVI-I/VHT-10/128M DDR(Samsung 8*16-3.6)

REVISION HISTORY:

X1 Initial Release

sku	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10229-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	nv43dvivgatv128m16x	600-10229-0002-101	P229-B01 NV43 GEN DVI-IVGAS-VIDEO 128MB 16Mx16 TSOP
2	nv43dvivgatv128m8x	600-10229-0003-101	P229-B01 NV43 GEN DVI-IVGAHDTV 128MB 8Mx16 TSOP
3	43gldvivgatv128m8x	600-50229-0001-101	P229-B01 NV43-GL GEN DVI-IVGAHDTV 128MB 8Mx16 TSOP
4	nv43dvivgatv256m16x	600-10229-0004-101	P229-B01 NV43 GEN DVI-IVGAHDTV 256MB 16Mx16 TSOP
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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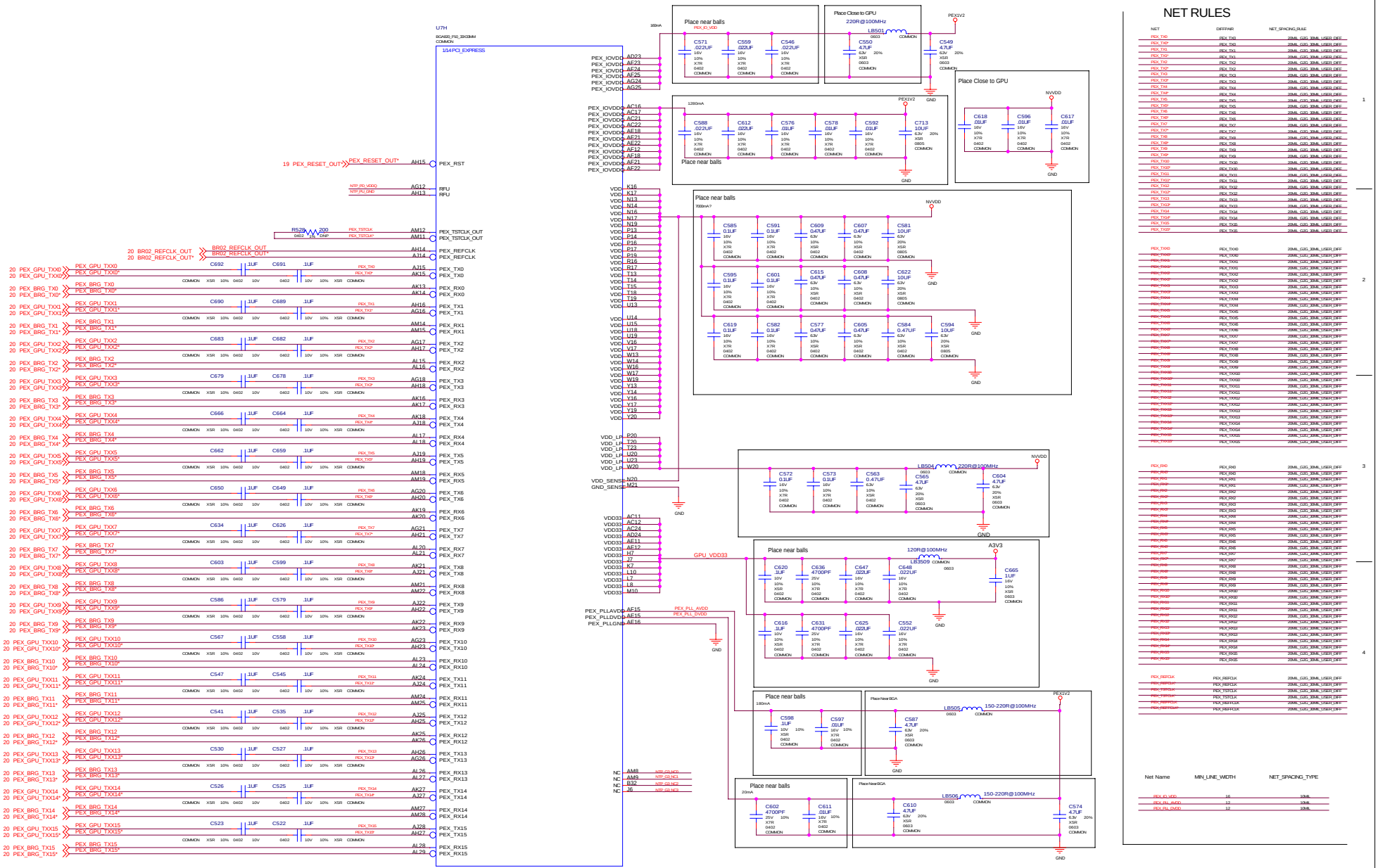

NET RULES

NET	DIFFPAIR	NET_SPACING_RULE
PEX_TX0	PEX_TX0	20MIL_GSG_30MIL_USER_DIFF
PEX_TX0*	PEX_TX0	20MIL_GSG_30MIL_USER_DIFF
PEX_TX1	PEX_TX1	20MIL_GSG_30MIL_USER_DIFF
PEX_TX1*	PEX_TX1	20MIL_GSG_30MIL_USER_DIFF
PEX_TX2	PEX_TX2	20MIL_GSG_30MIL_USER_DIFF
PEX_TX2*	PEX_TX2	20MIL_GSG_30MIL_USER_DIFF
PEX_TX3	PEX_TX3	20MIL_GSG_30MIL_USER_DIFF
PEX_TX3*	PEX_TX3	20MIL_GSG_30MIL_USER_DIFF
PEX_TX4	PEX_TX4	20MIL_GSG_30MIL_USER_DIFF
PEX_TX4*	PEX_TX4	20MIL_GSG_30MIL_USER_DIFF
PEX_TX5	PEX_TX5	20MIL_GSG_30MIL_USER_DIFF
PEX_TX5*	PEX_TX5	20MIL_GSG_30MIL_USER_DIFF
PEX_TX6	PEX_TX6	20MIL_GSG_30MIL_USER_DIFF
PEX_TX6*	PEX_TX6	20MIL_GSG_30MIL_USER_DIFF
PEX_TX7	PEX_TX7	20MIL_GSG_30MIL_USER_DIFF
PEX_TX7*	PEX_TX7	20MIL_GSG_30MIL_USER_DIFF
PEX_TX8	PEX_TX8	20MIL_GSG_30MIL_USER_DIFF
PEX_TX8*	PEX_TX8	20MIL_GSG_30MIL_USER_DIFF
PEX_TX9	PEX_TX9	20MIL_GSG_30MIL_USER_DIFF
PEX_TX9*	PEX_TX9	20MIL_GSG_30MIL_USER_DIFF
PEX_TX10	PEX_TX10	20MIL_GSG_30MIL_USER_DIFF
PEX_TX10*	PEX_TX10	20MIL_GSG_30MIL_USER_DIFF
PEX_TX11	PEX_TX11	20MIL_GSG_30MIL_USER_DIFF
PEX_TX11*	PEX_TX11	20MIL_GSG_30MIL_USER_DIFF
PEX_TX12	PEX_TX12	20MIL_GSG_30MIL_USER_DIFF
PEX_TX12*	PEX_TX12	20MIL_GSG_30MIL_USER_DIFF
PEX_TX13	PEX_TX13	20MIL_GSG_30MIL_USER_DIFF
PEX_TX13*	PEX_TX13	20MIL_GSG_30MIL_USER_DIFF
PEX_TX14	PEX_TX14	20MIL_GSG_30MIL_USER_DIFF
PEX_TX14*	PEX_TX14	20MIL_GSG_30MIL_USER_DIFF
PEX_TX15	PEX_TX15	20MIL_GSG_30MIL_USER_DIFF
PEX_TX15*	PEX_TX15	20MIL_GSG_30MIL_USER_DIFF

Net Name	MIN_LINE_WIDTH	NET_SPACING_TYPE
PEX_IO_VDD	16	10MIL
PEX_PLL_AVDD	12	10MIL
PEX_PLL_DVDD	12	10MIL

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Size	Document Number	Rev
Custom	PCI Express Interface	00A

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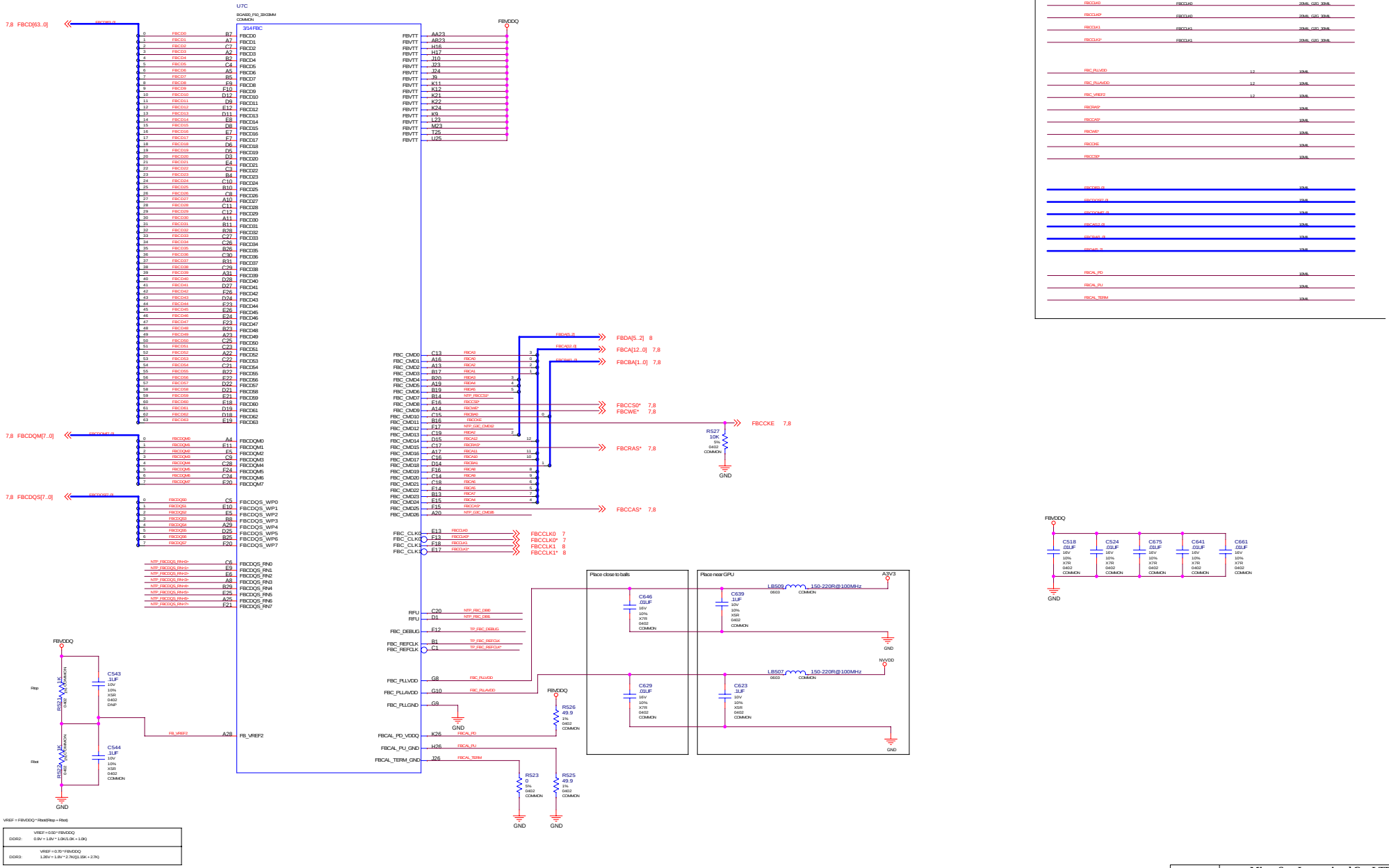
FB BANK A

U7B
2/14 FBA
FBVDDQ
PLACE BELOW GPU
GND
FBA_PLLVDD
FBA_PLLAVDD
FB_VREF1
FB_DLLVDD
PLACE close to balls
PLACE near GPU
A3V3
NVVDD
ON NV3x version's of G3
FB_DLLVDD will be routed on FB_PLLVDD

FB BANK C



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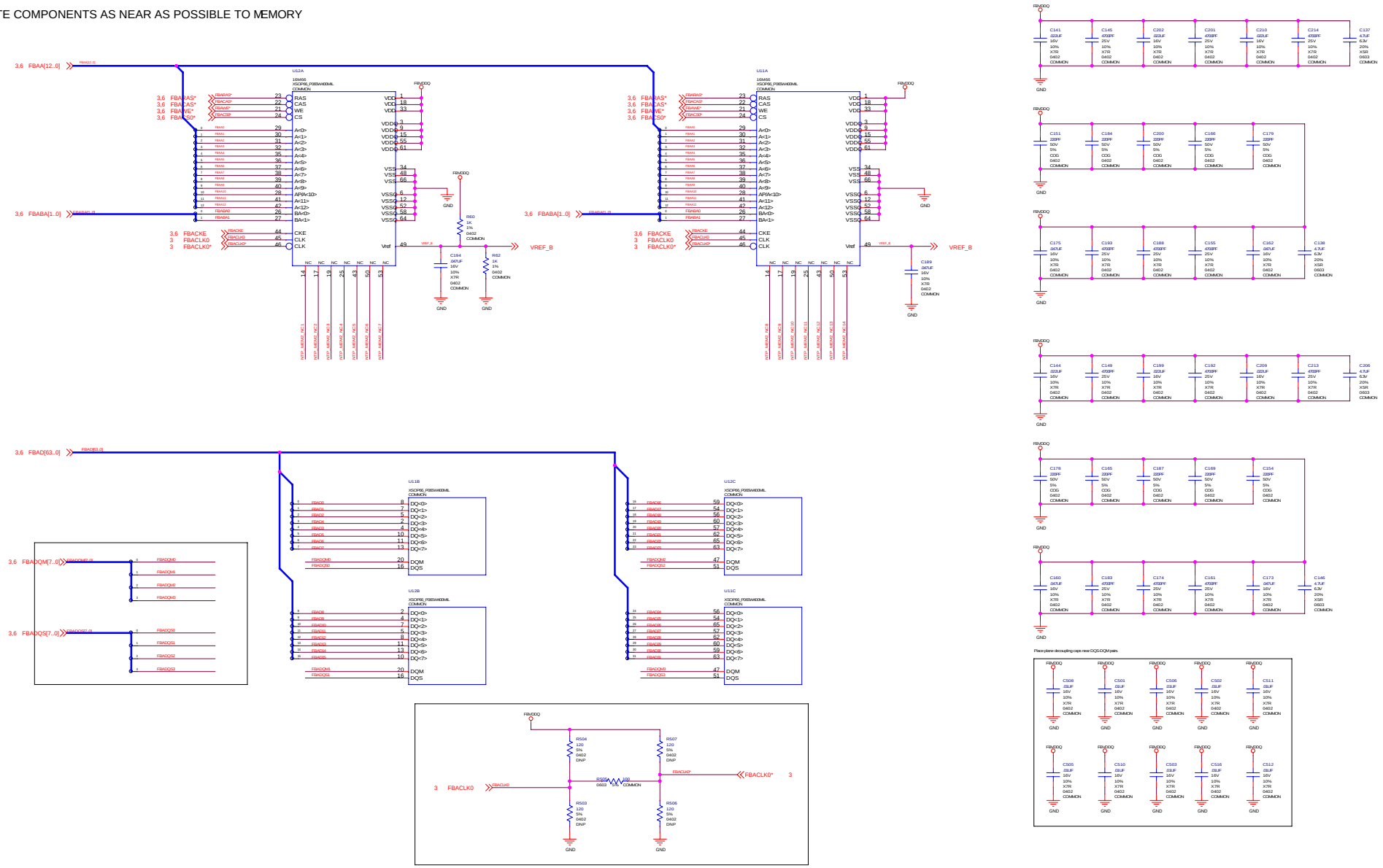
MS-8988		
Size: Custom	Document Number: FB BANK C	Rev: 00A
Date: Tuesday, November 16, 2004	Sheet 4 of 20	

MEMORY 1st bank
0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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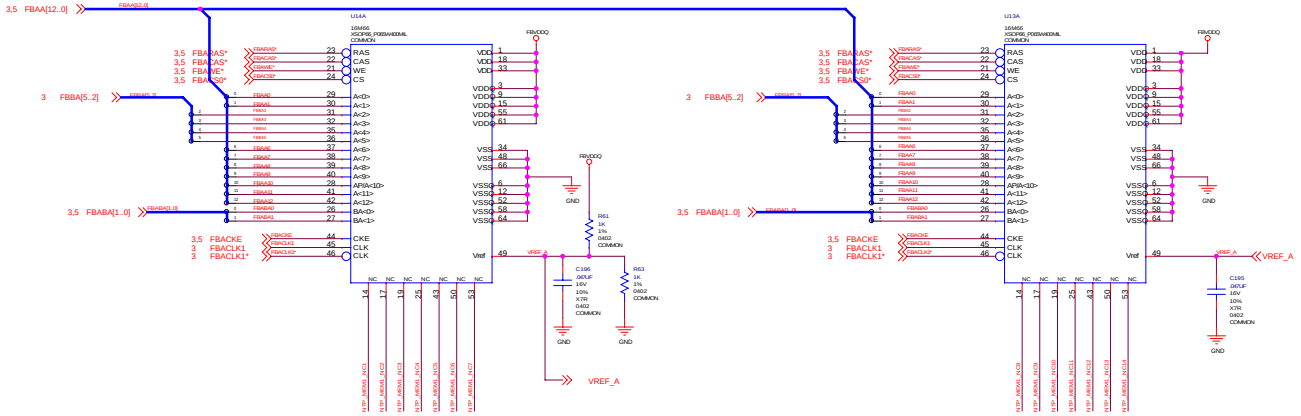
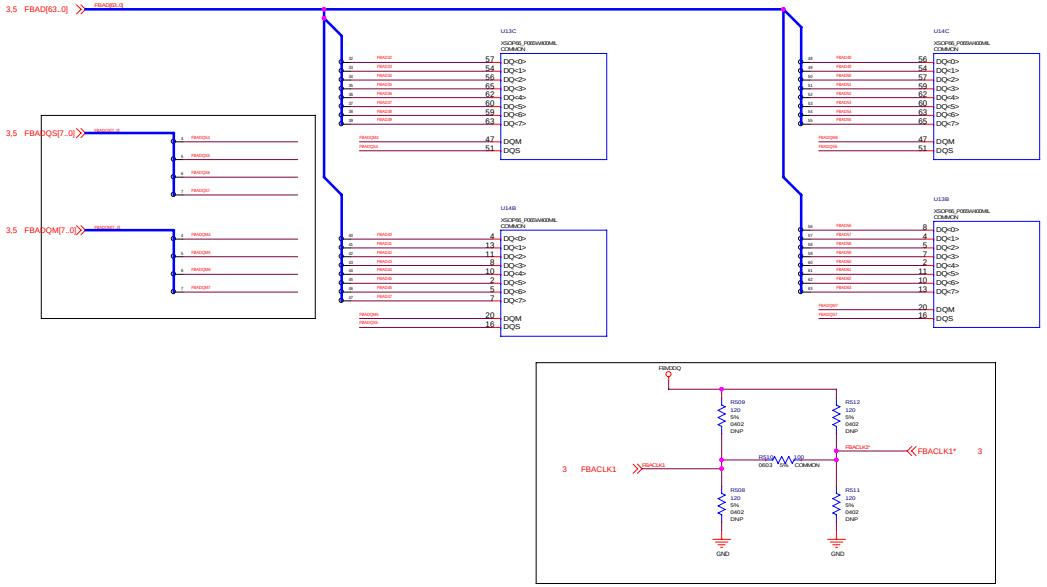
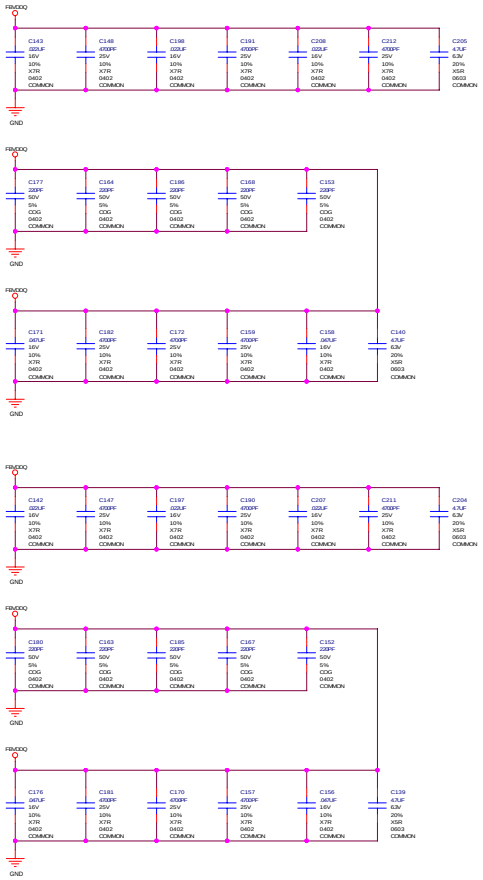
MS-8988	
Size: Custom	Document Number: Memory 1st bank 0..31
Rev: 00A	
Date: Tuesday, November 16, 2004	Sheet 5 of 20

MEMORY 1st bank
32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY







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Size: Custom	Document Number: Memory 1st 32..63
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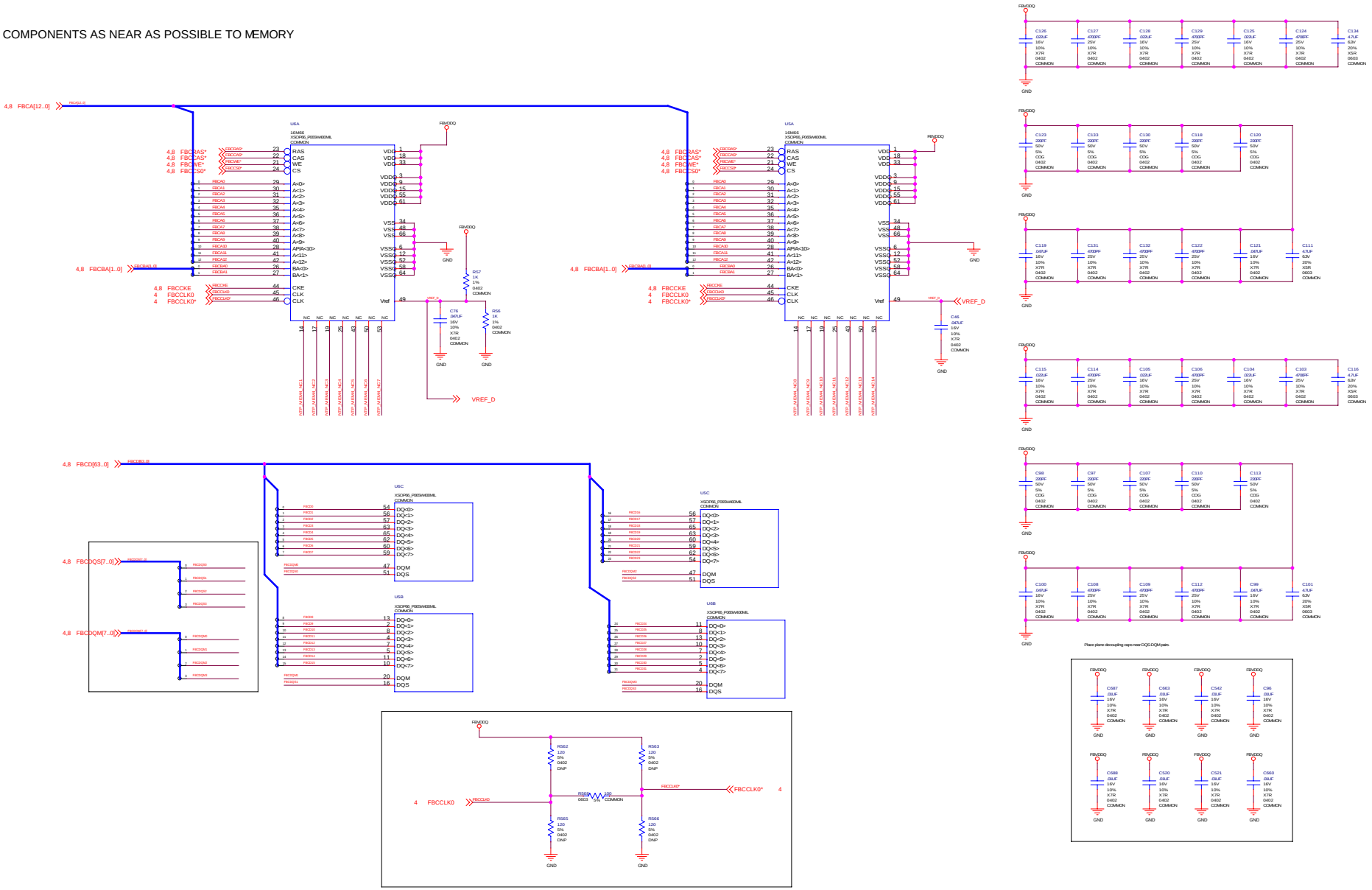
MEMORY 2nd bank
0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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MS-8988		
Size: Custom	Document Number: Memory 2nd bank 0..31	Rev: 00A
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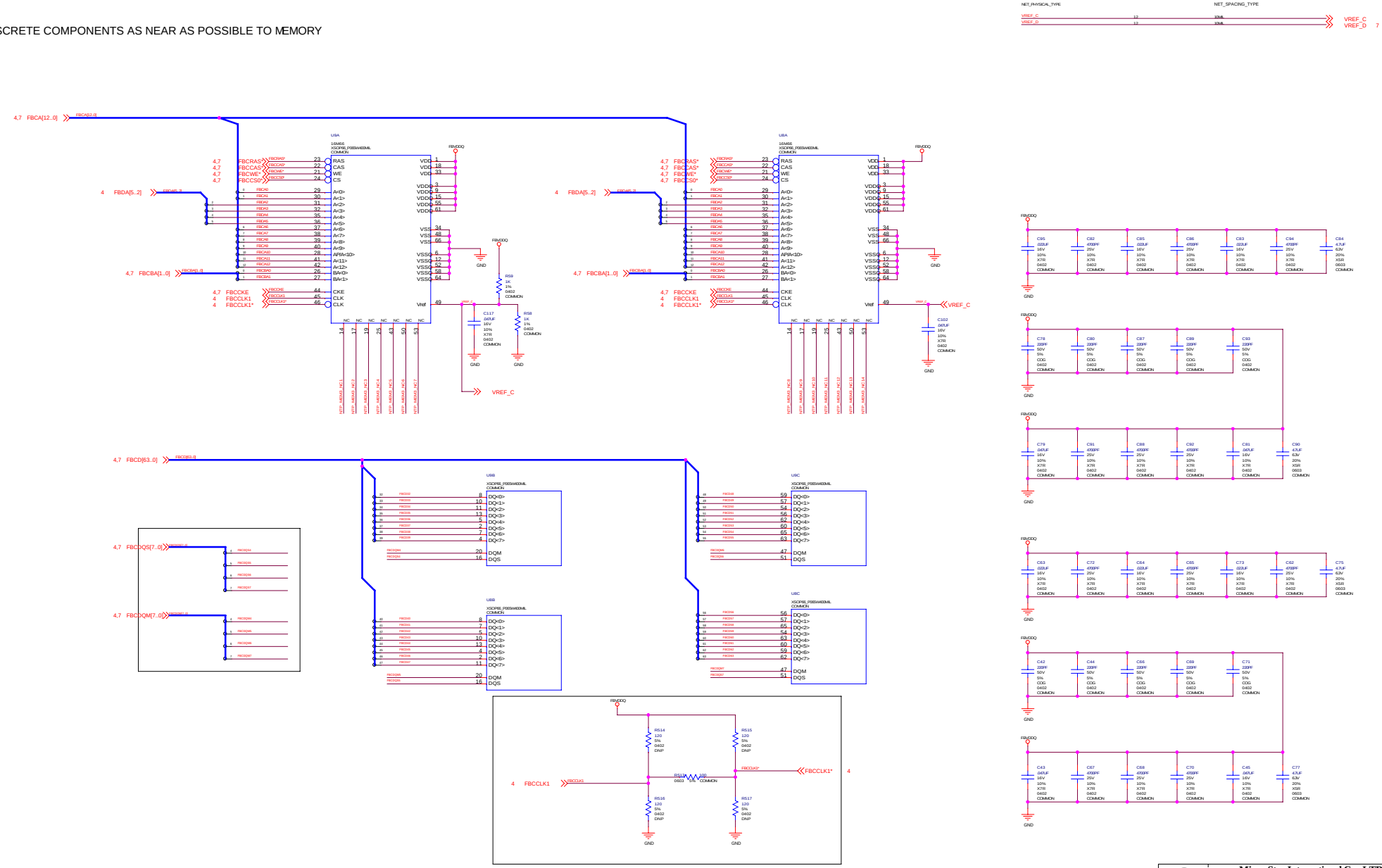
MEMORY 2nd bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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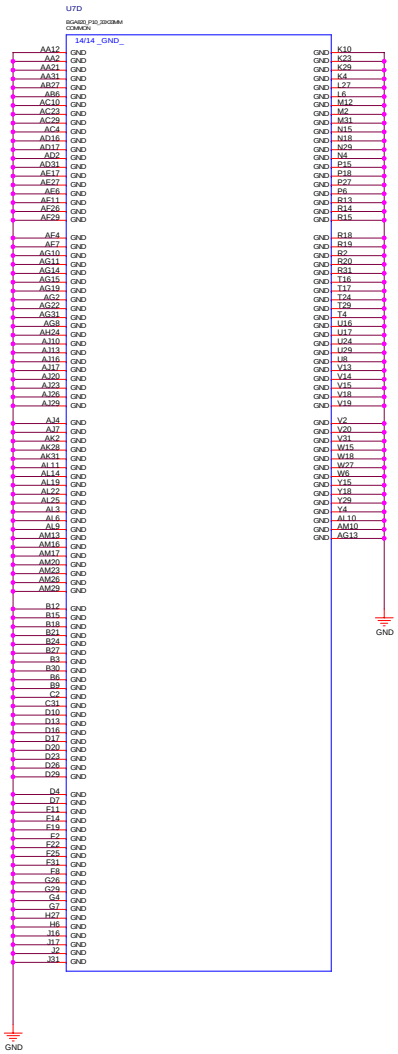
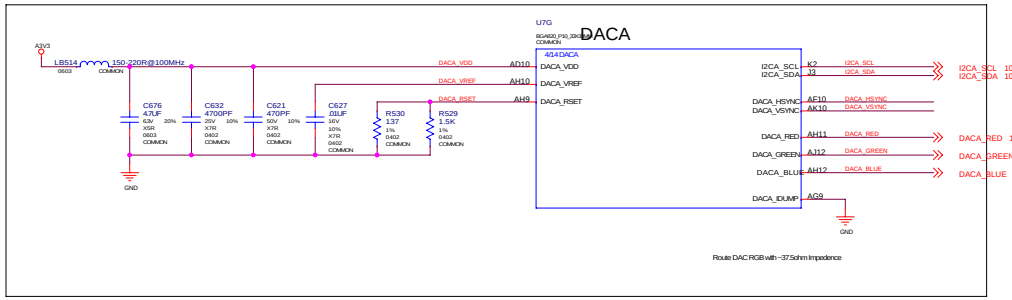
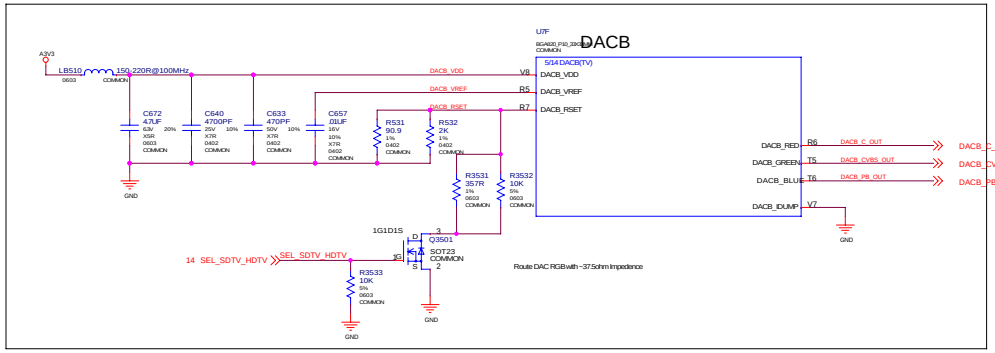
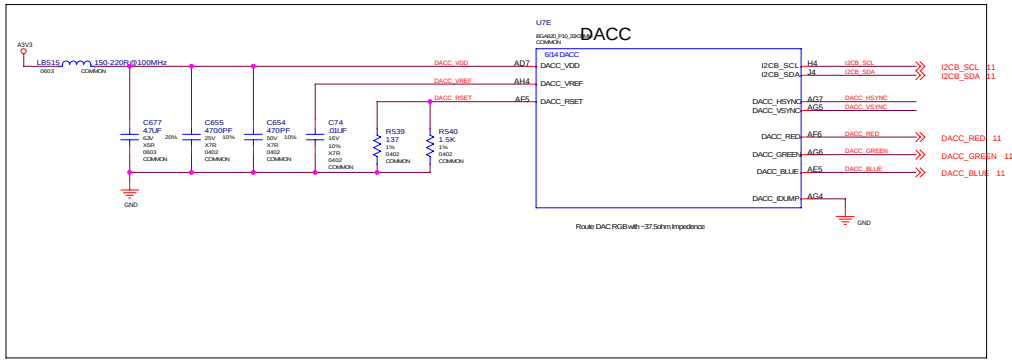
GND,DACA,DACB,DACC





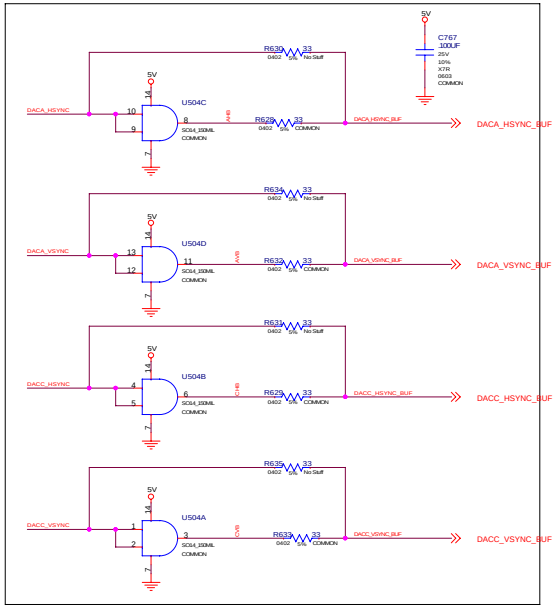




NET RULES

NET_NAME	MIN_LINE_WIDTH	NET_SPACING_RULE	IMPEDANCE
I2CA_SCL		30MIL	
I2CA_SDA		30MIL	
DACA_HSYNC		30MIL	
DACA_VSYNC		30MIL	
DACA_RED		30MIL	USA411:RR7:137:50:OHM:2%
DACA_GREEN		30MIL	USA312:RR6:137:50:OHM:2%
DACA_BLUE		30MIL	USA412:RR5:137:50:OHM:2%
DACA_VDD	12	30MIL	
DACA_VREF	12	30MIL	
DACA_RSET	12	30MIL	
DACB_C_OUT		30MIL	USB5:RR41:37:50:OHM:2%
DACB_CVBS_OUT		30MIL	UB75:RR28:137:50:OHM:2%
DACB_PB_OUT		30MIL	UB75:RR21:137:50:OHM:2%
DACB_VDD	12	30MIL	
DACB_VREF	12	30MIL	
DACB_RSET	12	30MIL	
DACC_HSYNC		30MIL	
DACC_VSYNC		30MIL	
DACC_RED		30MIL	USAG5:RR23:137:50:OHM:2%
DACC_GREEN		30MIL	USAG5:RR27:137:50:OHM:2%
DACC_BLUE		30MIL	USAG5:RR20:137:50:OHM:2%
DACC_VDD	12	30MIL	
DACC_VREF	12	30MIL	
DACC_RSET	12	30MIL	
TV_RSET_SEL	12	30MIL	
I2CB_SDA		30MIL	
I2CB_SCL		30MIL	
SEL_2ND_DEV		30MIL	
AHB		30MIL	
AVB		30MIL	
DACA_HSYNC_BUF		30MIL	
DACA_VSYNC_BUF		30MIL	
CHB		30MIL	
CVB		30MIL	
DACC_HSYNC_BUF		30MIL	
DACC_VSYNC_BUF		30MIL	

DACA & DACC Sync Buffers



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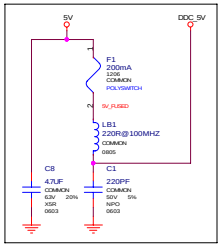
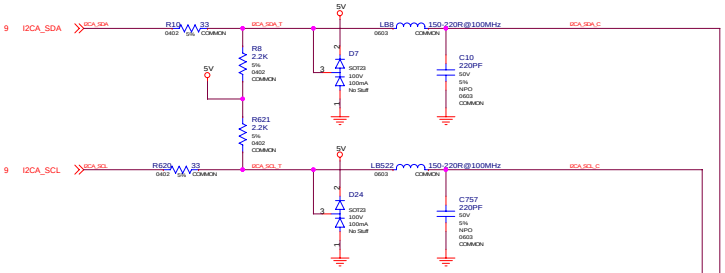
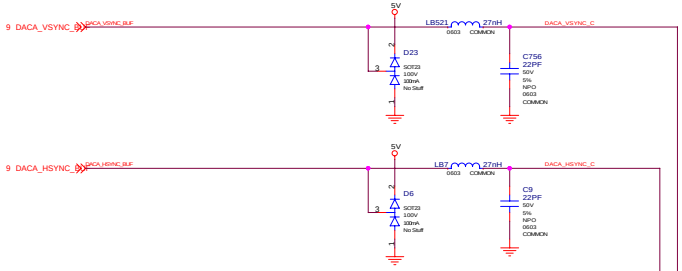
VGA
DACA

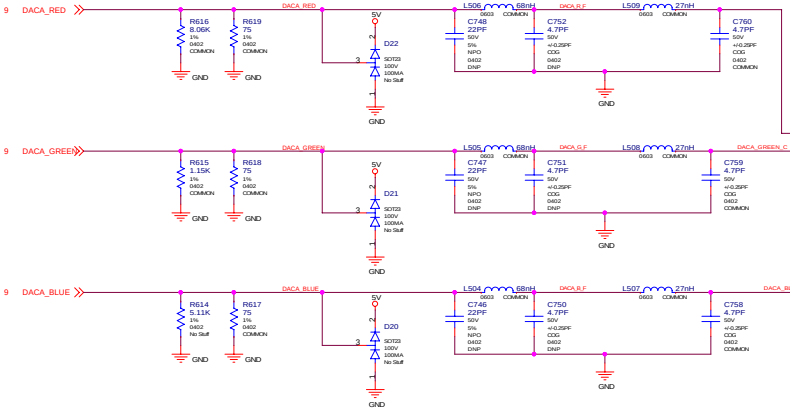
DDC
5V

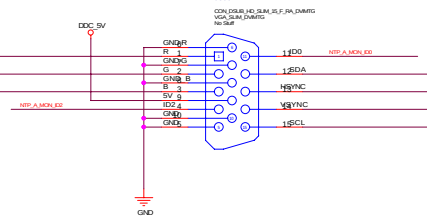


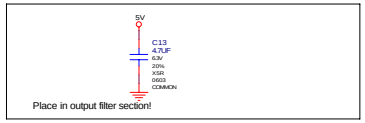
Changed the FUSE to 200mA



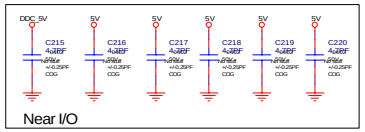


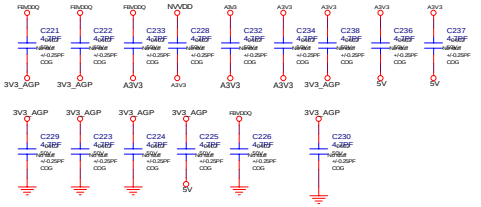


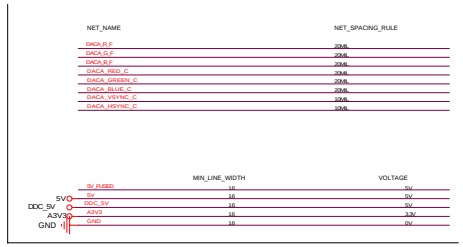




EMI Reserve Cap.







12 I2CA_SDA_C >> I2CA_SDA_C
12 I2CA_SCL_C >> I2CA_SCL_C
12 DACA_VSYNC_C >> DACA_VSYNC_C
12 DACA_HSYNC_C >> DACA_HSYNC_C
12 DACA_RED_C >> DACA_RED_C
12 DACA_GREEN_C >> DACA_GREEN_C
12 DACA_BLUE_C >> DACA_BLUE_C

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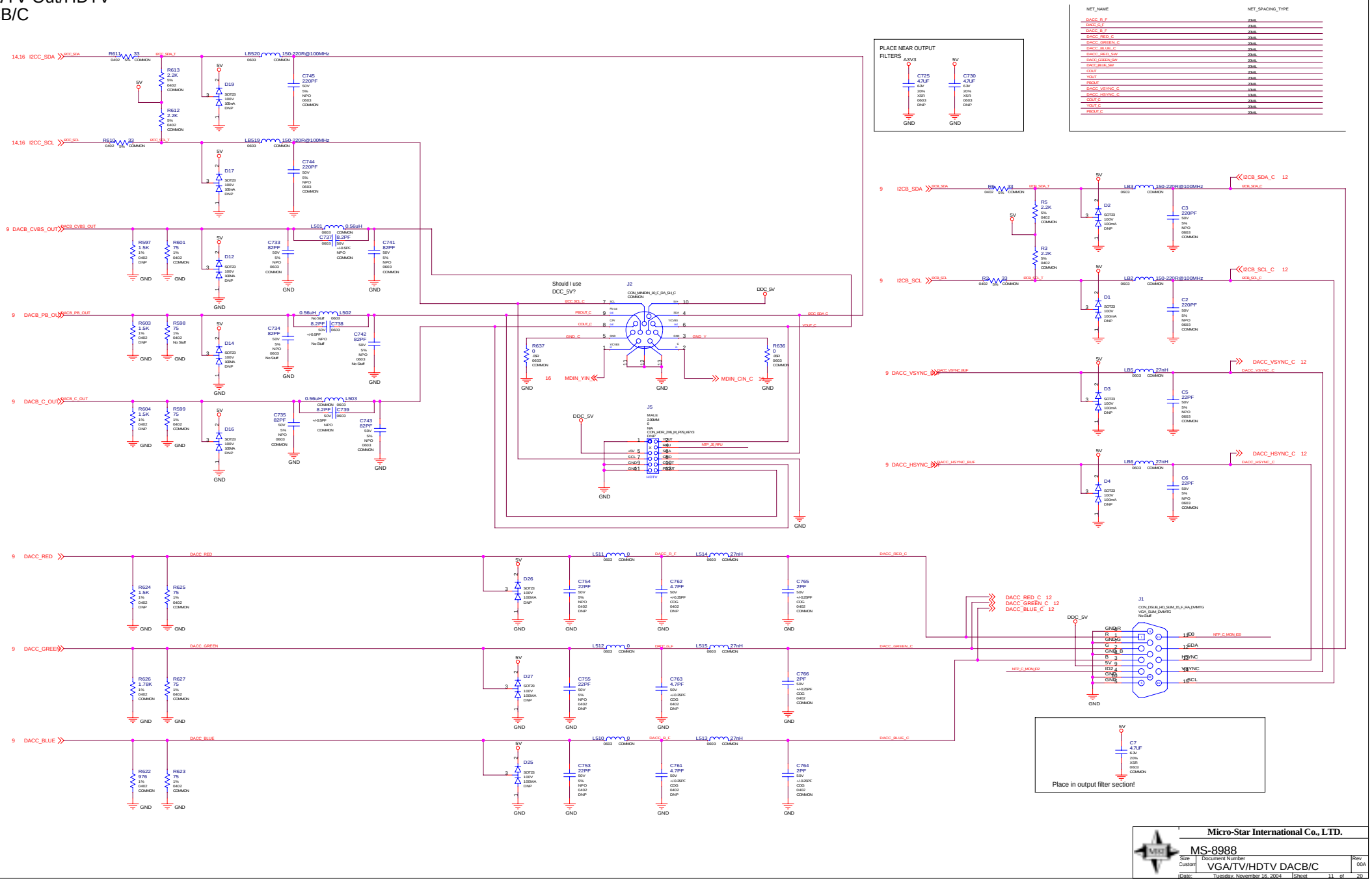
VGA/TV Out/HDTV
DACB/C



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Size: Custom	Document Number: VGA/TV/HDTV DACB/C		Rev: 00A
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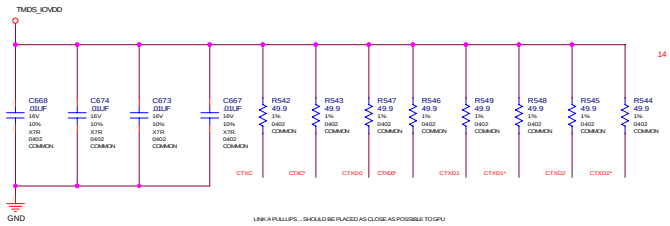
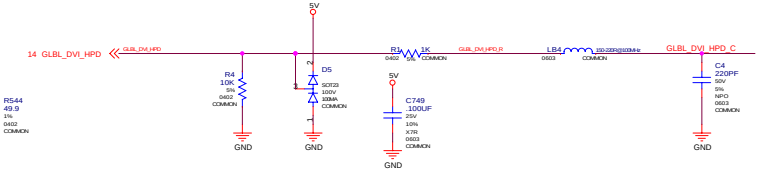
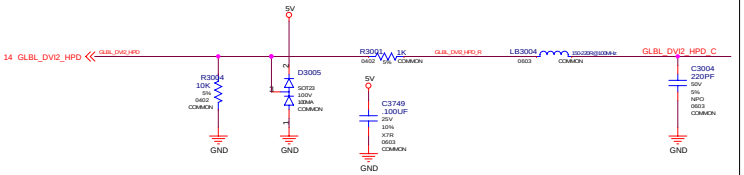
INTERNAL TMDS



Hotplug Detection

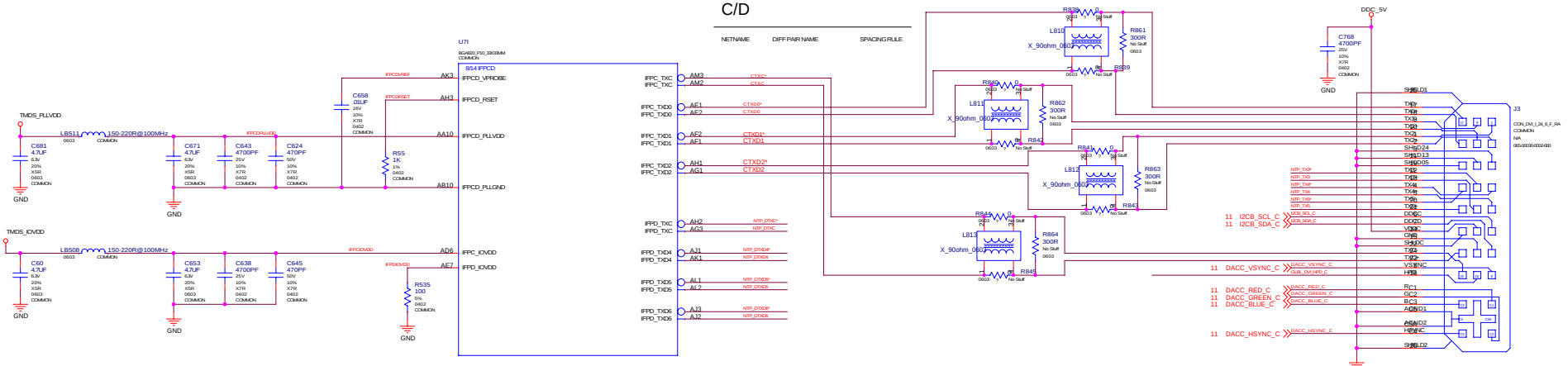


Hotplug Detection2

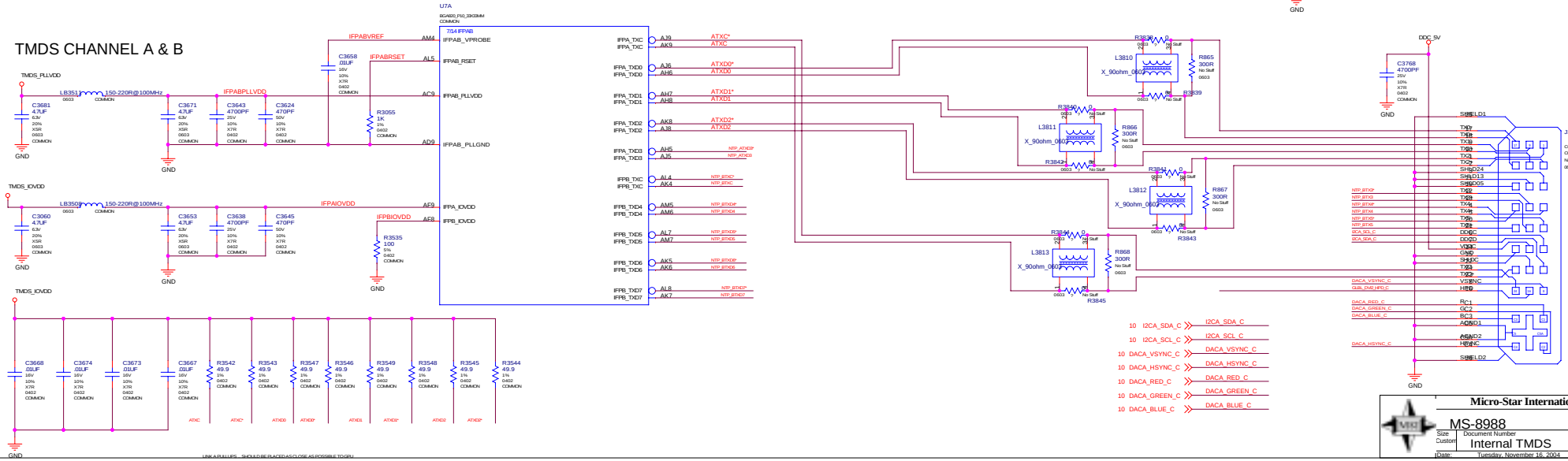


INTERNAL TMDS ..LINK C/D

NETNAME	DIFF PAIR NAME	SPACING RULE



TMDS CHANNEL A & B



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Size: Custom	Document Number: Internal TMDS
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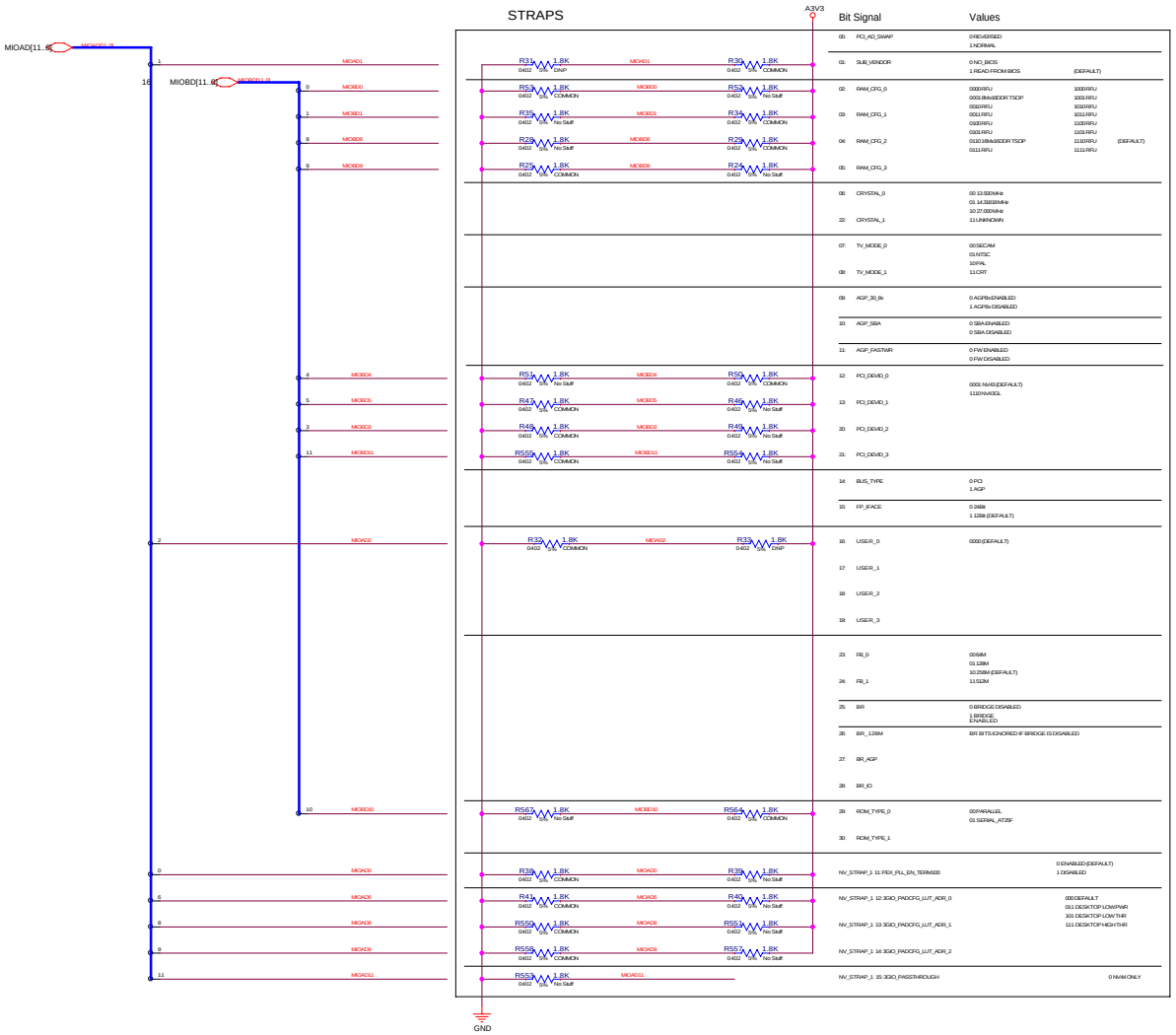
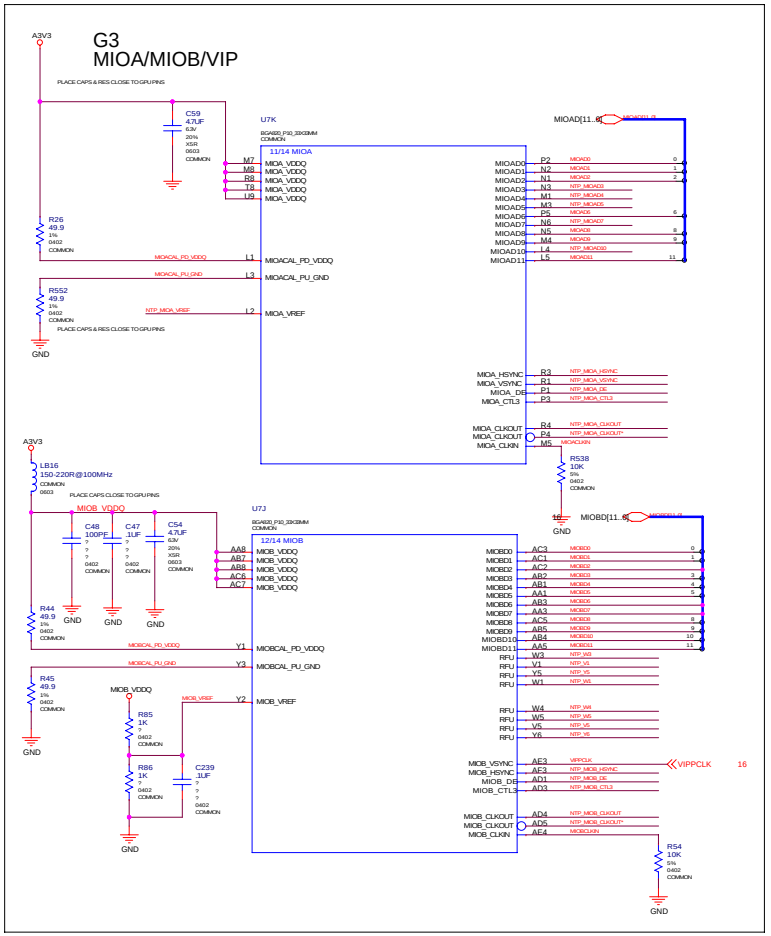
STRAPS, MIOA/MIOB

STRAPS



MIOs



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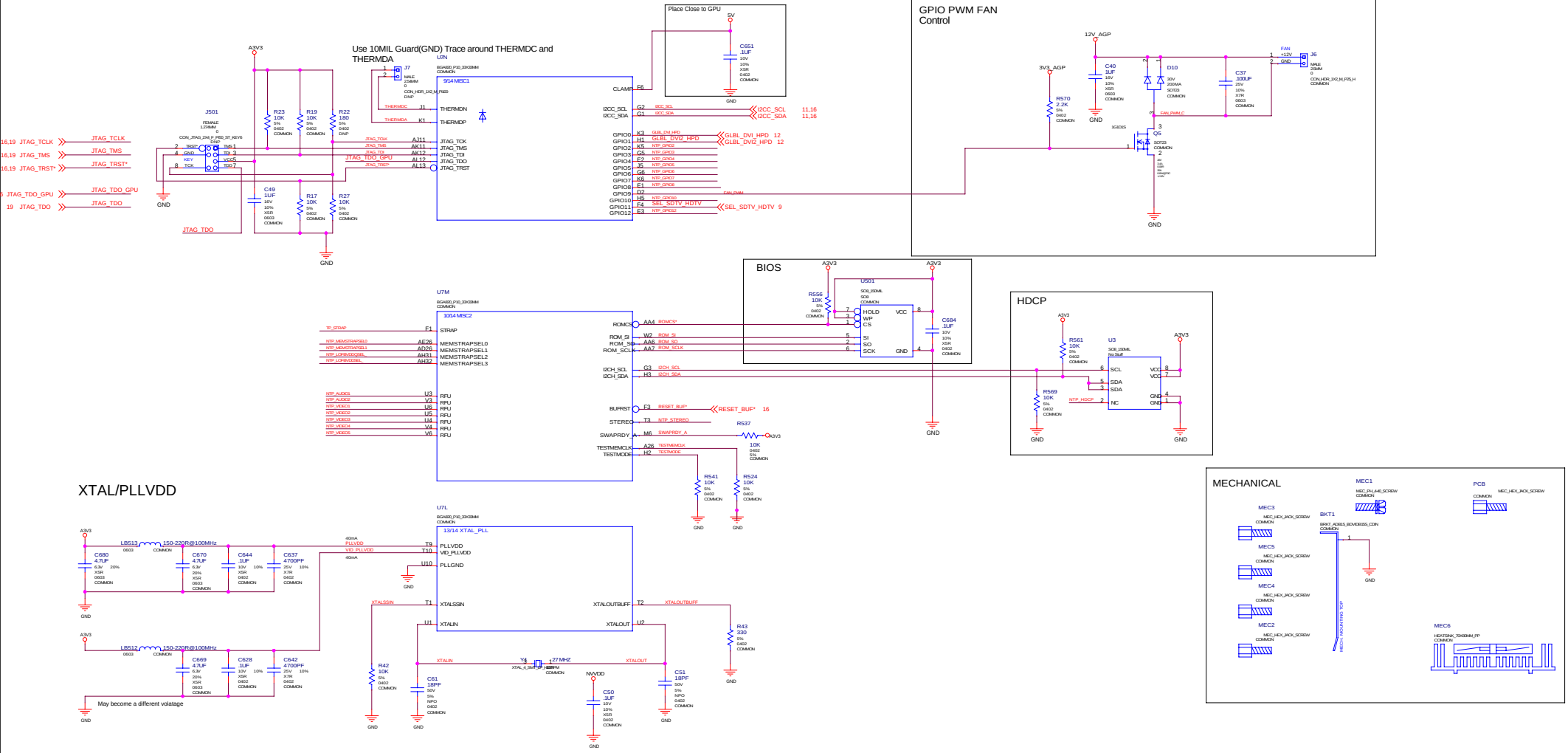
MS-8988
Size: Custom | Document Number: Straps, MIOA/MIOB | Rev: 00A
Date: Tuesday, November 16, 2004 | Sheet 13 of 20

XTAL, GPIO, ROM

NET	MIN_LIN_WIDTH	NET_SPACING_RULE
XTALIN		10MIL
XTALOUT		10MIL
PLLVDD	12	10MIL
VID_PLLVDD	12	10MIL
FAN_PWM		20MIL
FAN_PWM_B		20MIL
FAN_PWM_C		20MIL
THERMDC	10	
THERMDA	10	



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Size	Document Number	Rev
Custom	XTAL,GPIO,ROM,FAN,MEC	00A
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Power Supply II (ISL6549)

1V2 NVVDD
bypass

PEX1V2 = 1.2V @ 3A

1V2 = 0.8V * (1+Rt/Rb)

NVVDD & PEX1V2

NVVDD = 1.35V @ upto 24A

1.2V~1.4V/24A(ambient)

NVVDD = 0.8V * (1+Rt/Rb)

NVVDD = 0.8V*(1+1.13k/1.8k)=1.302V

5V & 3V3

BR02VDD = 1.3V @ upto 3A

V(BR02VDD)=V(fb)*(1+Rtop/Rbom)

1.302V=1.24*(1+100/2000)

V(3V3)=V(fb)*(1+Rtop/Rbom)

3.333V=2.5*(1+1000/3000)

Net Name	MIN_LINE_WIDTH		VOLTAGE
5V	16	2A	5V
NVVDD	16	2A	1.35V
PEX1V2	20	4	12V
12V_PEX_FLTRD	20	6	12V

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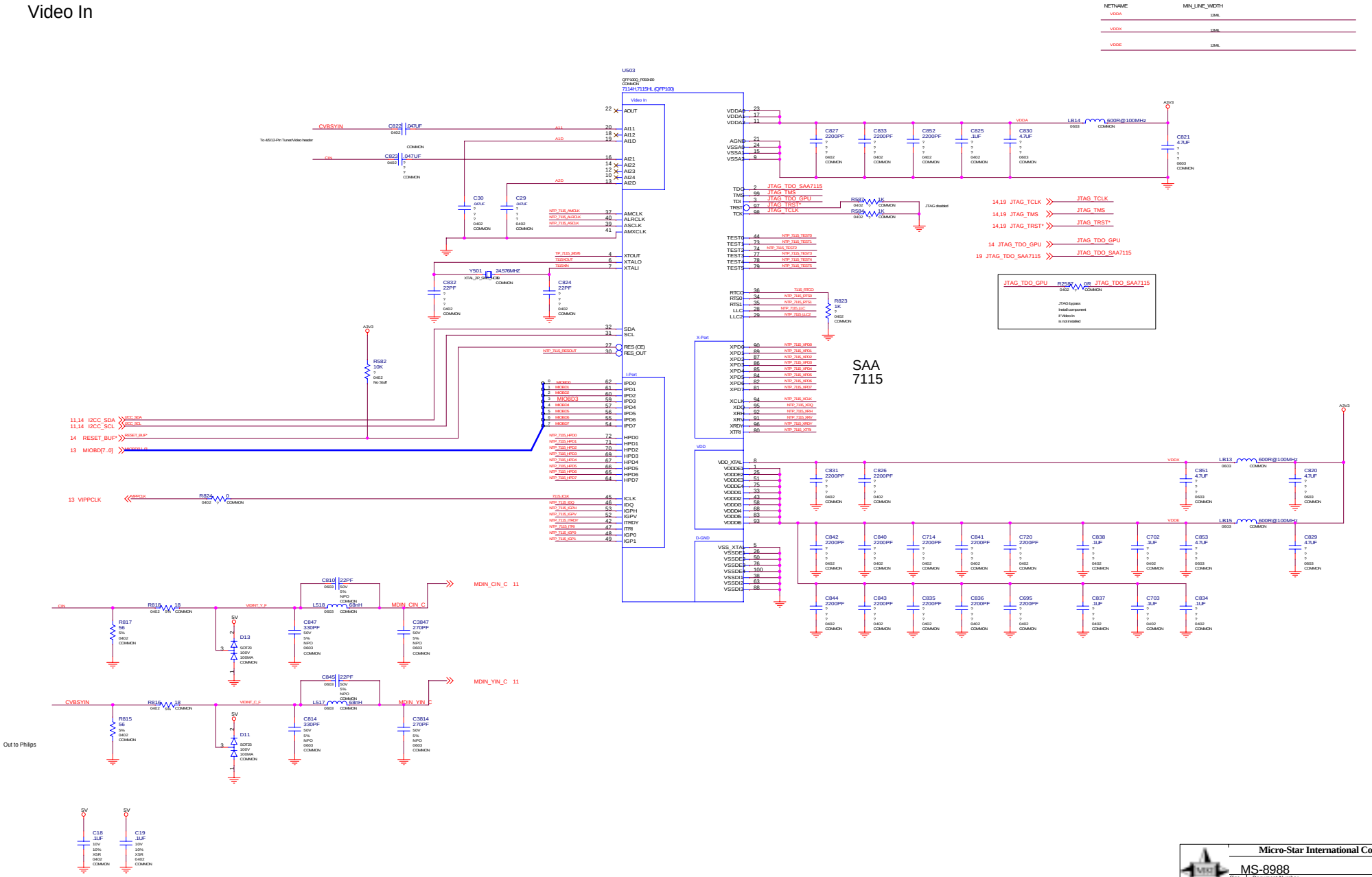
Video In


NETNAME
MIN_LINE_WIDTH
VDDA
VDDX
VDDE
U503
SAA 7115
Video In
I-Port
X-Port
VDD
D-GND
A3V3
5V
CVBSYIN
CIN
MDIN_CIN_C
MDIN_YIN_C
VIDINT_V_F
VIDINT_C_F
JTAG_TDO_SAA7115
JTAG_TMS
JTAG_TDO_GPU
JTAG_TRST*
JTAG_TCLK
JTAG disabled
JTAG_TDO_GPU R258 0R JTAG_TDO_SAA7115
JTAG bypass
Install component
if Video-in
is not installed
11,14 I2CC_SDA
11,14 I2CC_SCL
14 RESET_BUF*
13 MIOBD[7..0]
13 VIPPCLK
Out to Philips
Micro-Star International Co., LTD.
MS-8988
Video In
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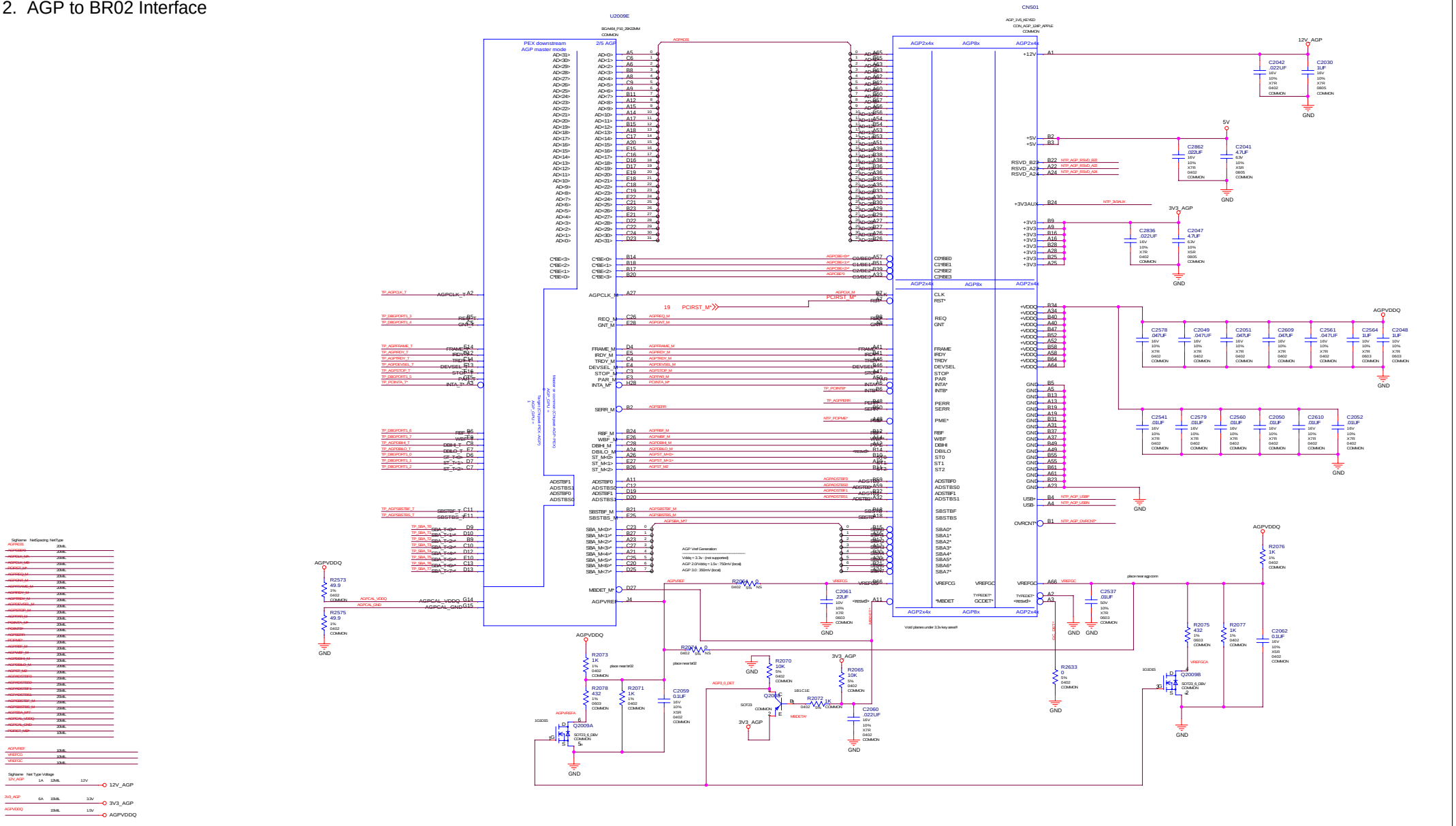
2. AGP to BR02 Interface



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
AGP to BR02 Interface

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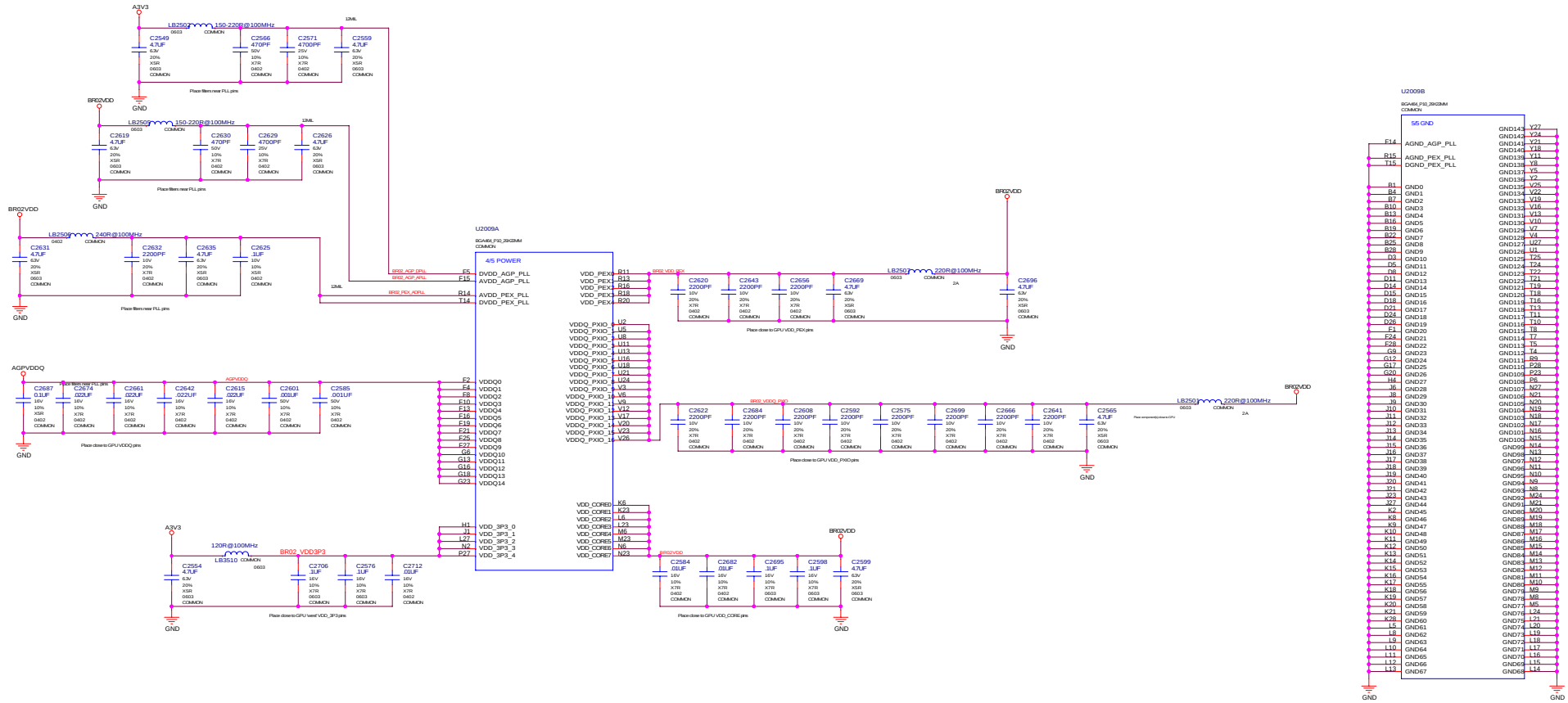
3. BR02 PWR/GND/De-Coupling



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BR02 PWR/GND/De-Coupling

Micro-Star International Co., LTD.			
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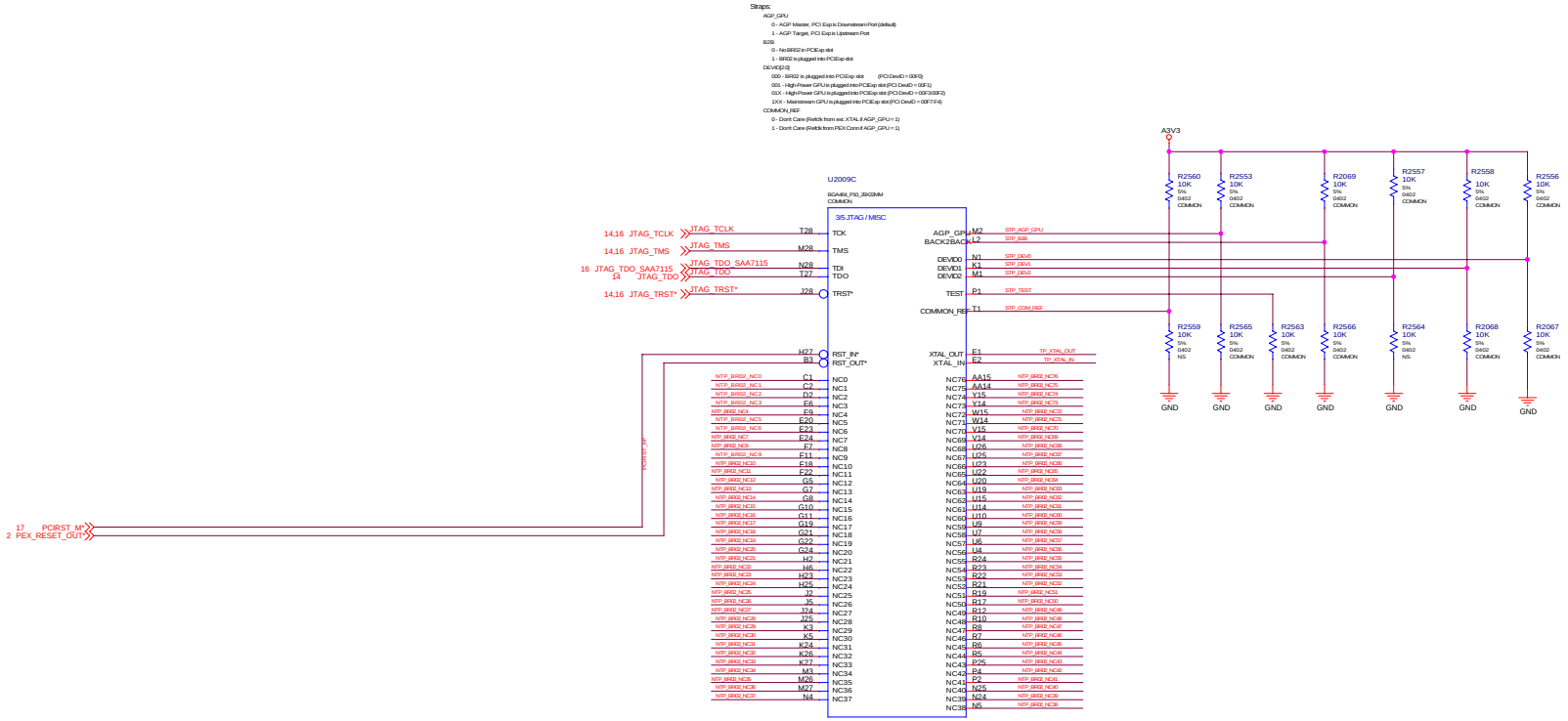
4. BR02 JTAG / Straps / Misc.



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
BR02 JTAG / Straps / Misc.

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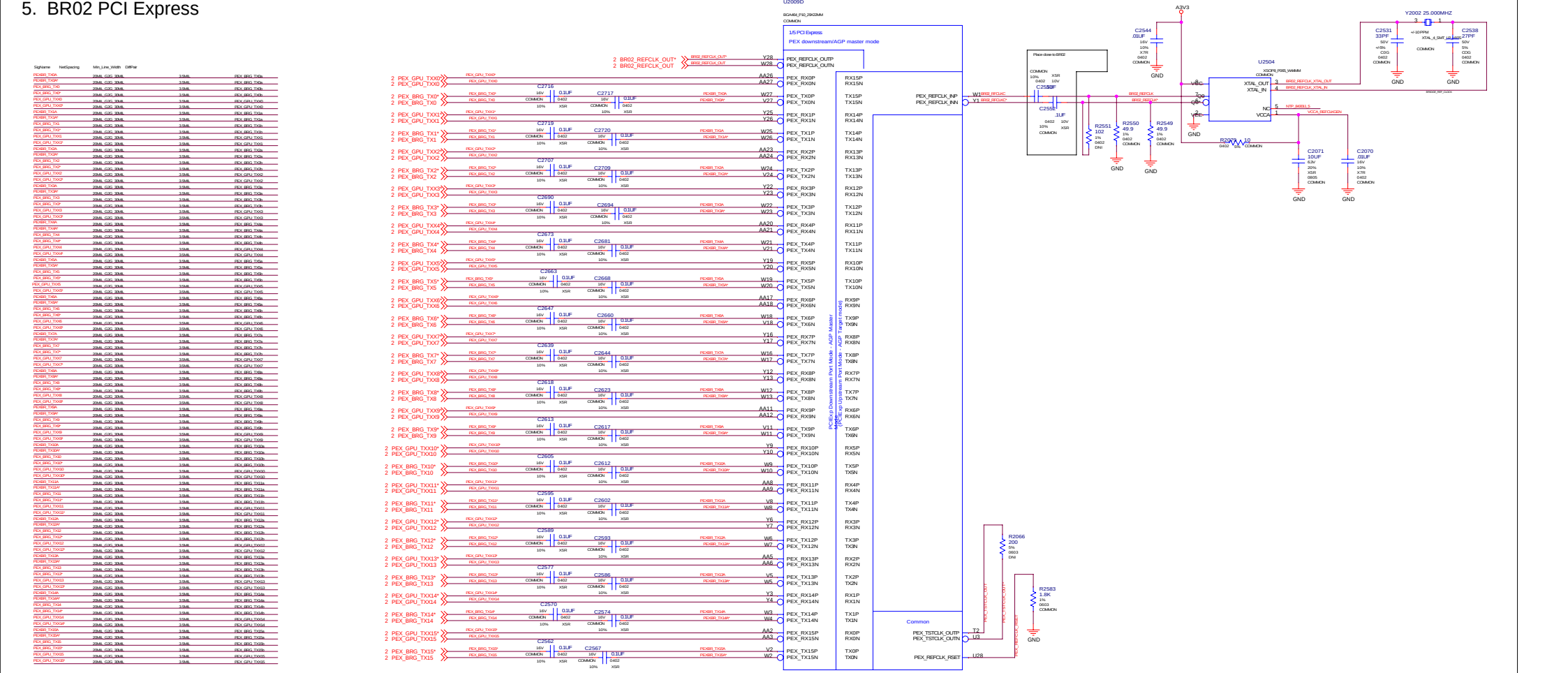
5. BR02 PCI Express



SigName	NetSpacing	Min_Line_Width	DiffPair	
PEXBR_TX0A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX0a
PEXBR_TX0A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX0a
PEX_BRG_TX0		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX0b
PEX_BRG_TX0*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX0b
PEX_GPU_TX0D		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEX_GPU_TX0D*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEXBR_TX1A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX1a
PEXBR_TX1A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX1a
PEX_BRG_TX1		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX1
PEX_BRG_TX1*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX1b
PEX_GPU_TX0C		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX01
PEX_GPU_TX0C*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX01
PEXBR_TX2A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX2a
PEXBR_TX2A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX2a
PEX_BRG_TX2		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX2b
PEX_BRG_TX2*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX2b
PEX_GPU_TX02		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX02
PEX_GPU_TX02*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX02
PEXBR_TX3A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX3a
PEXBR_TX3A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX3a
PEX_BRG_TX3		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX3b
PEX_BRG_TX3*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX3b
PEX_GPU_TX03		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX03
PEX_GPU_TX03*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX03
PEXBR_TX4A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX4a
PEXBR_TX4A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX4a
PEX_BRG_TX4		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX4b
PEX_BRG_TX4*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX4b
PEX_GPU_TX04		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX04
PEX_GPU_TX04*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX04
PEXBR_TX5A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX5a
PEXBR_TX5A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX5a
PEX_BRG_TX5		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX5b
PEX_BRG_TX5*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX5b
PEX_GPU_TX05		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX05
PEX_GPU_TX05*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX05
PEXBR_TX6A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX6a
PEXBR_TX6A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX6a
PEX_BRG_TX6		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX6b
PEX_BRG_TX6*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX6b
PEX_GPU_TX06		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX06
PEX_GPU_TX06*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX06
PEXBR_TX7A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX7a
PEXBR_TX7A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX7a
PEX_BRG_TX7		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX7b
PEX_BRG_TX7*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX7b
PEX_GPU_TX07		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX07
PEX_GPU_TX07*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX07
PEXBR_TX8A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX8a
PEXBR_TX8A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX8a
PEX_BRG_TX8		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX8b
PEX_BRG_TX8*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX8b
PEX_GPU_TX08		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX08
PEX_GPU_TX08*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX08
PEXBR_TX9A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX9a
PEXBR_TX9A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX9a
PEX_BRG_TX9		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX9b
PEX_BRG_TX9*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX9b
PEX_GPU_TX09		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX09
PEX_GPU_TX09*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX09
PEXBR_TX10A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX10a
PEXBR_TX10A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX10a
PEX_BRG_TX10		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX10b
PEX_BRG_TX10*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX10b
PEX_GPU_TX0D		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEX_GPU_TX0D*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEXBR_TX11A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX11a
PEXBR_TX11A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX11a
PEX_BRG_TX11		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX11b
PEX_BRG_TX11*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX11b
PEX_GPU_TX0D		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEX_GPU_TX0D*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEXBR_TX12A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX12a
PEXBR_TX12A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX12a
PEX_BRG_TX12		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX12b
PEX_BRG_TX12*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX12b
PEX_GPU_TX0D		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEX_GPU_TX0D*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEXBR_TX13A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX13a
PEXBR_TX13A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX13a
PEX_BRG_TX13		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX13b
PEX_BRG_TX13*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX13b
PEX_GPU_TX0D		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEX_GPU_TX0D*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEXBR_TX14A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX14a
PEXBR_TX14A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX14a
PEX_BRG_TX14		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX14b
PEX_BRG_TX14*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX14b
PEX_GPU_TX0D		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEX_GPU_TX0D*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEXBR_TX15A		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX15a
PEXBR_TX15A*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX15a
PEX_BRG_TX15		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX15b
PEX_BRG_TX15*		20MIL G2G 30MIL	3.5MIL	PEX_BRG_TX15b
PEX_GPU_TX0D		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D
PEX_GPU_TX0D*		20MIL G2G 30MIL	3.5MIL	PEX_GPU_TX0D

BR02_REFCLK_OUT	20MIL G2G 30MIL	3.5MIL	BR02_REFCLK_OUT
BR02_REFCLK_OUT*	20MIL G2G 30MIL	3.5MIL	BR02_REFCLK_OUT
BR02_REFCLK	20MIL G2G 30MIL	3.5MIL	BR02_REFCLK
BR02_REFCLK*	20MIL G2G 30MIL	3.5MIL	BR02_REFCLK
BR02_REFCLKC	20MIL G2G 30MIL	3.5MIL	BR02_REFCLKC
BR02_REFCLKC*	20MIL G2G 30MIL	3.5MIL	BR02_REFCLKC

PEX_REFCLK_RSET		3.5MIL	
PEX_TSTCLK_OUT	20MIL G2G 30MIL	3.5MIL	PEX_TSTCLK_OUT
PEX_TSTCLK_OUT*	20MIL G2G 30MIL	3.5MIL	PEX_TSTCLK_OUT
BR02_REFCLK_OUT	20MIL G2G 30MIL	3.5MIL	BR02_REFCLK_OUT
BR02_REFCLK_OUT*	20MIL G2G 30MIL	3.5MIL	BR02_REFCLK_OUT

ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
BR02 PCI Express

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