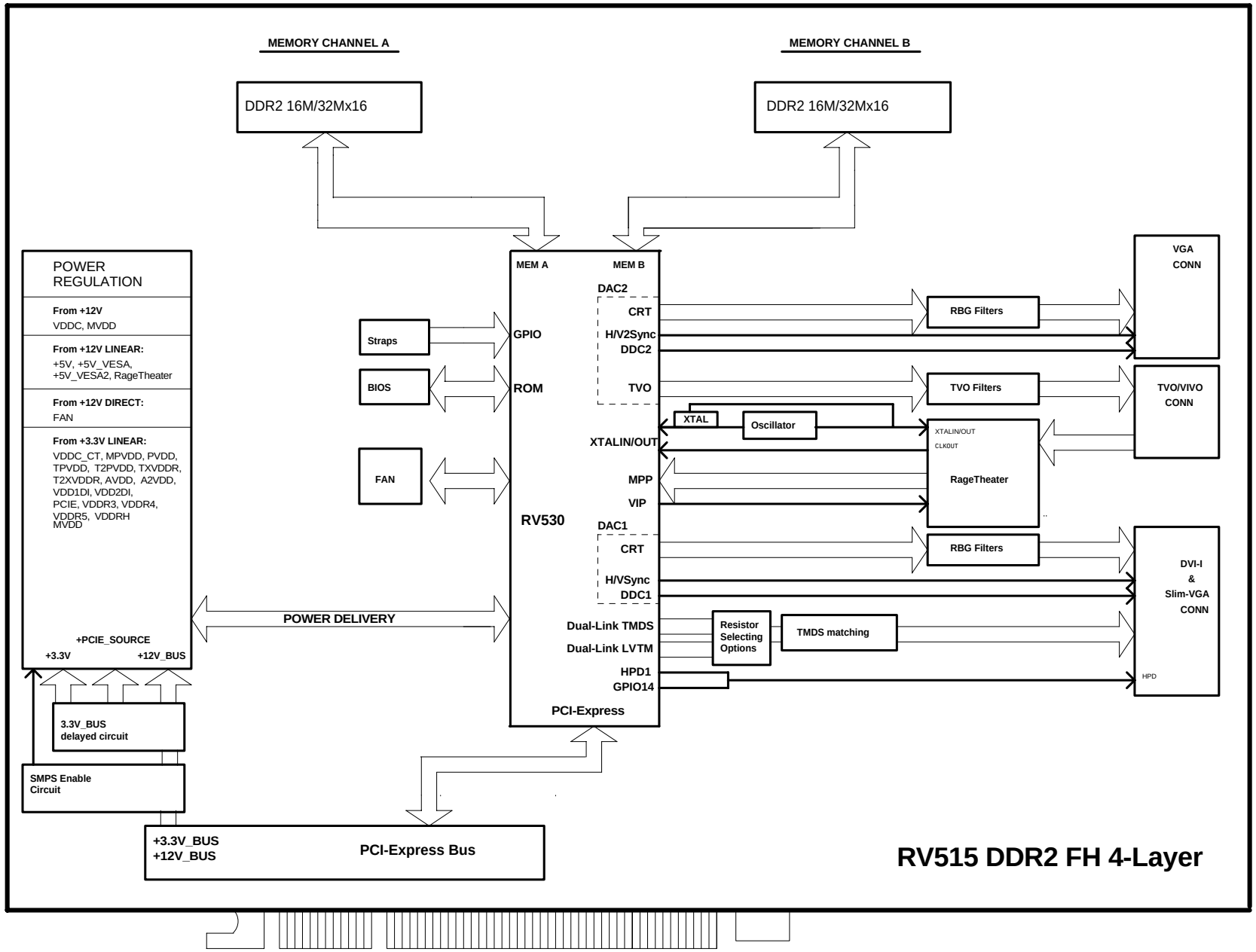

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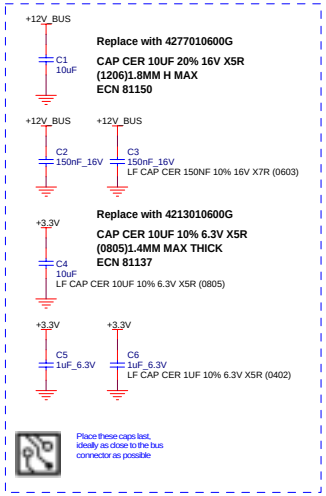
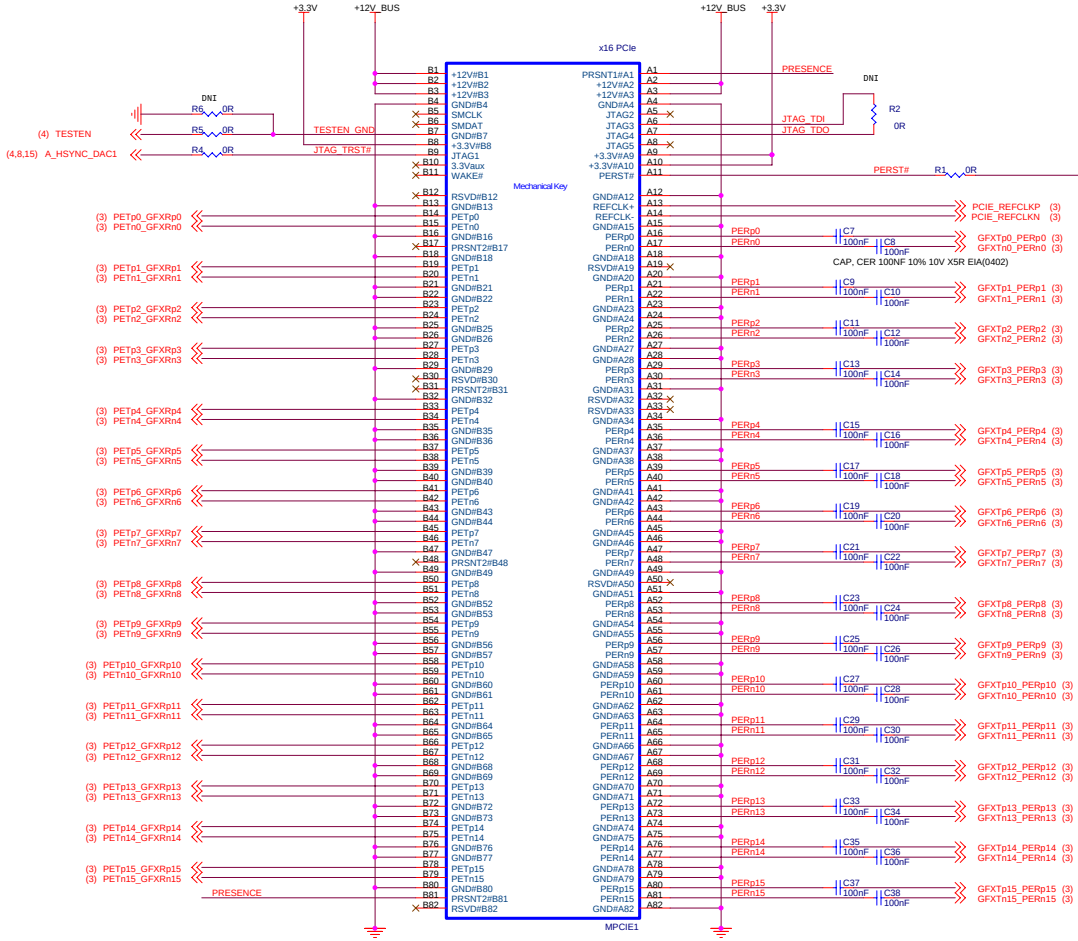
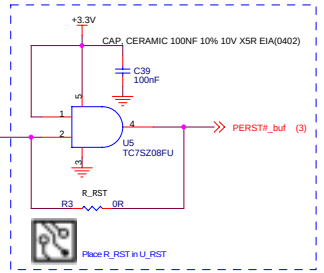
PCI-EXPRESS EDGE CONNECTOR







Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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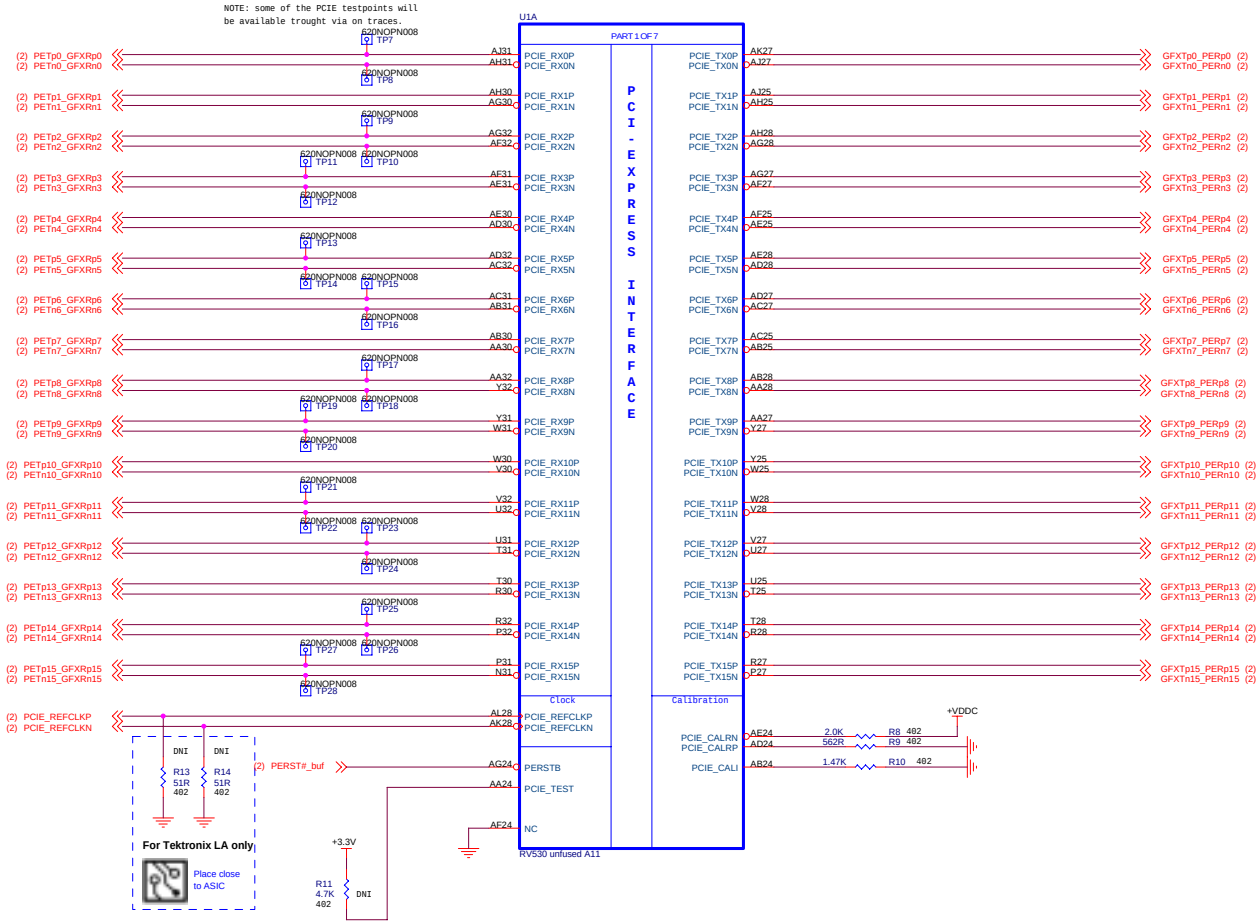

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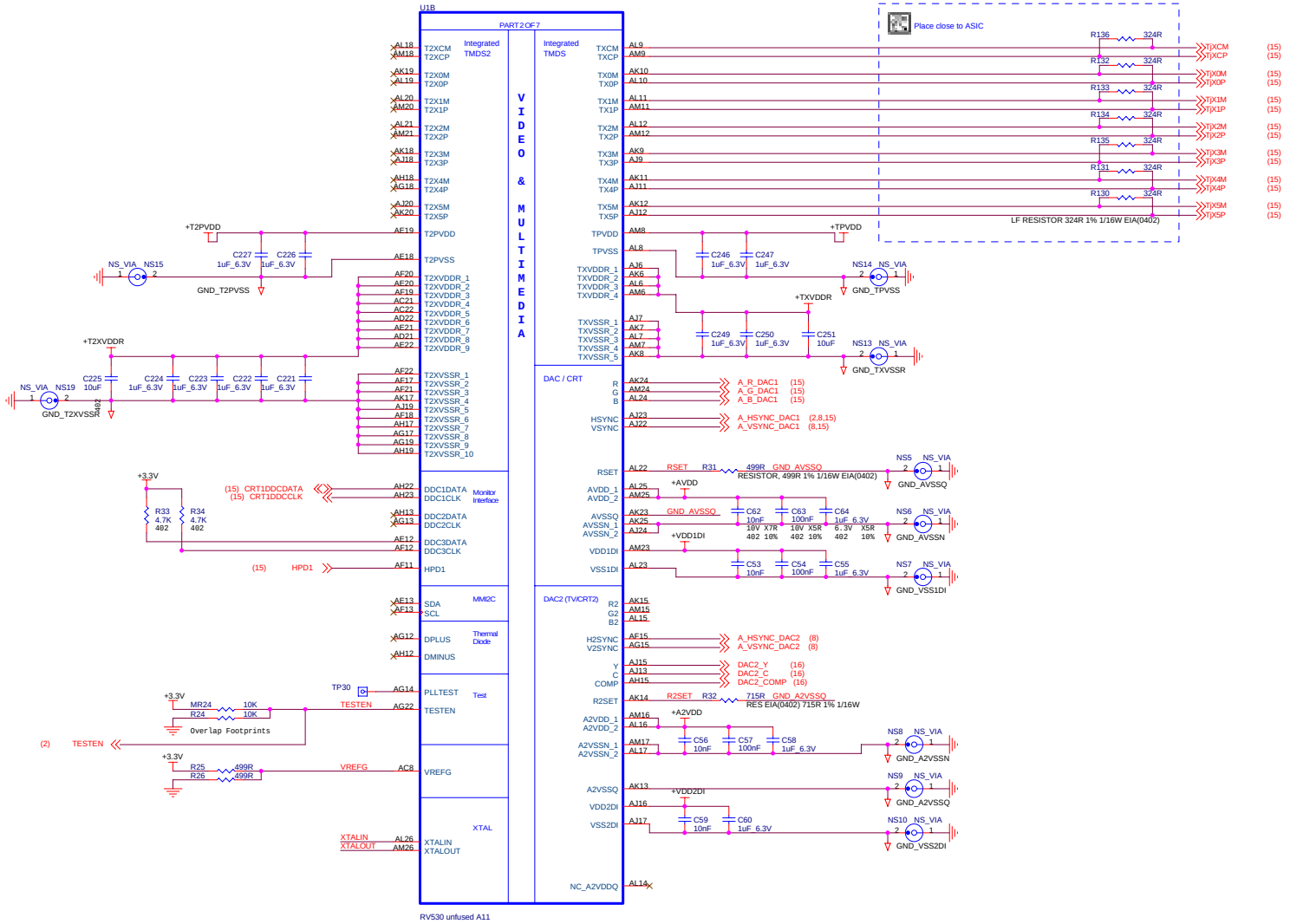

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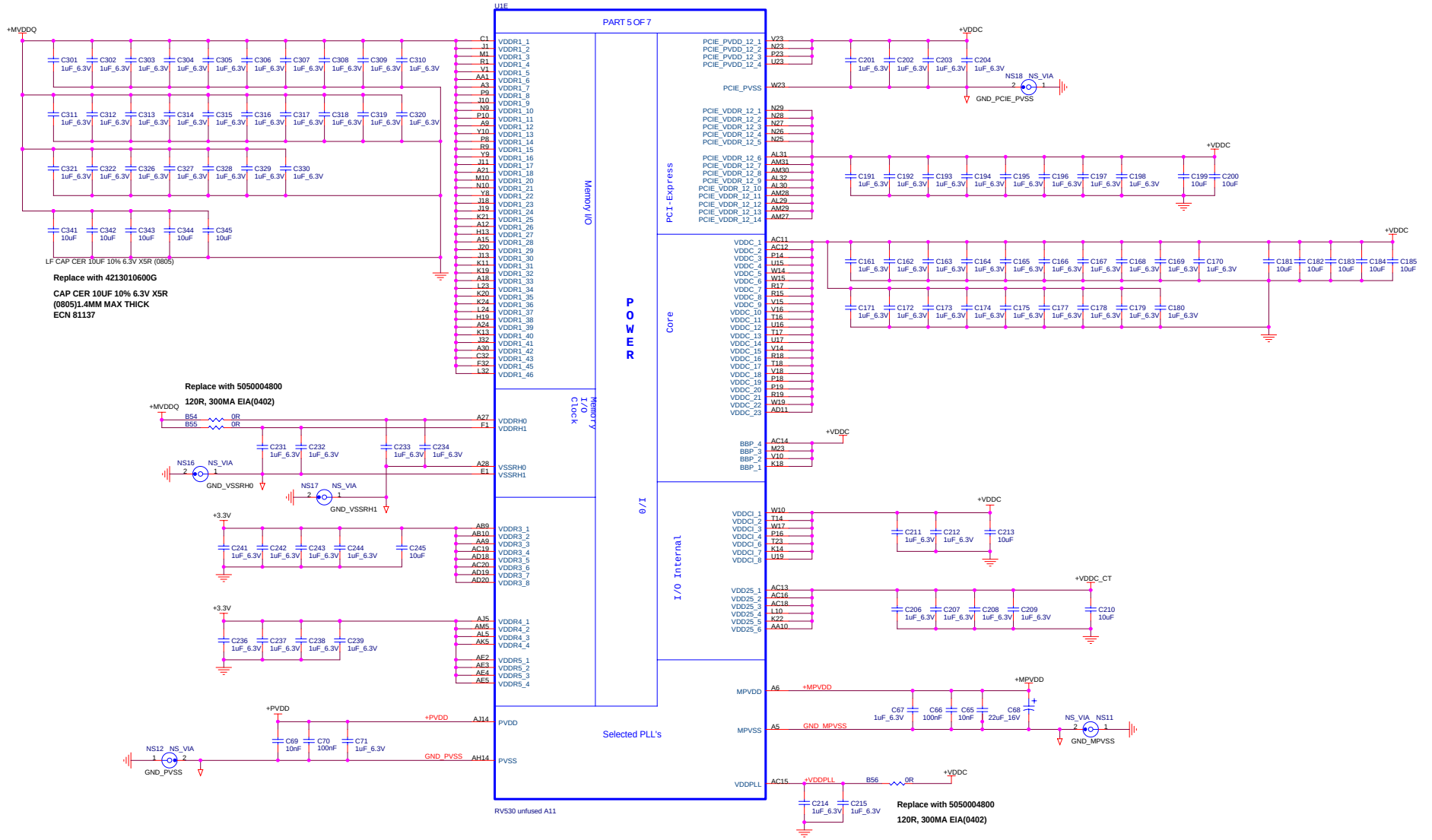
U1E
PART 5 OF 7
POWER
Memory I/O
PCI-Express
Core
I/O Internal
Memory CLOCK I/O
Selected PLL's
RV530 unfused A11
+MVDDQ
LF CAP CER 10UF 10% 6.3V X5R (0805)
Replace with 4213010600G
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK
ECN 81137
Replace with 5050004800
120R, 300MA EIA(0402)
+VDDC
GND_PCIE_PVSS
GND_VSSRH0
GND_VSSRH1
+3.3V
+PVDD
GND_PVSS
+MPVDD
GND_MPVSS
+VDDC_CT
+VDDPLL
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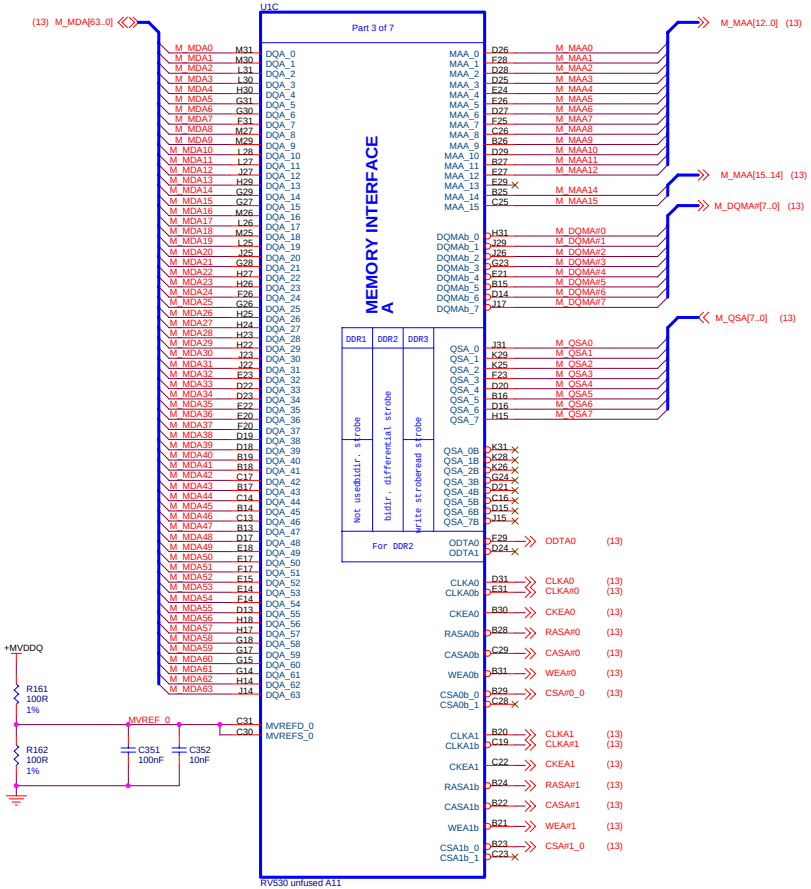
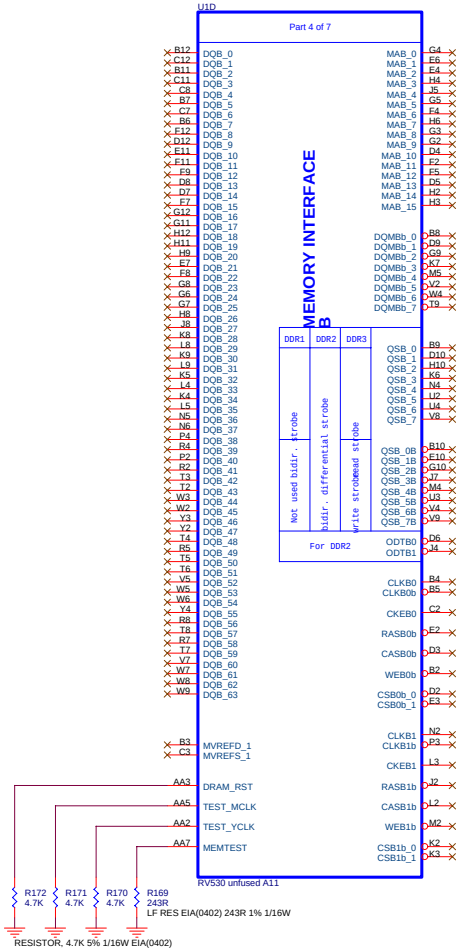
RV530 MEMORY CHANNELS A and B

Channel A



Channel B



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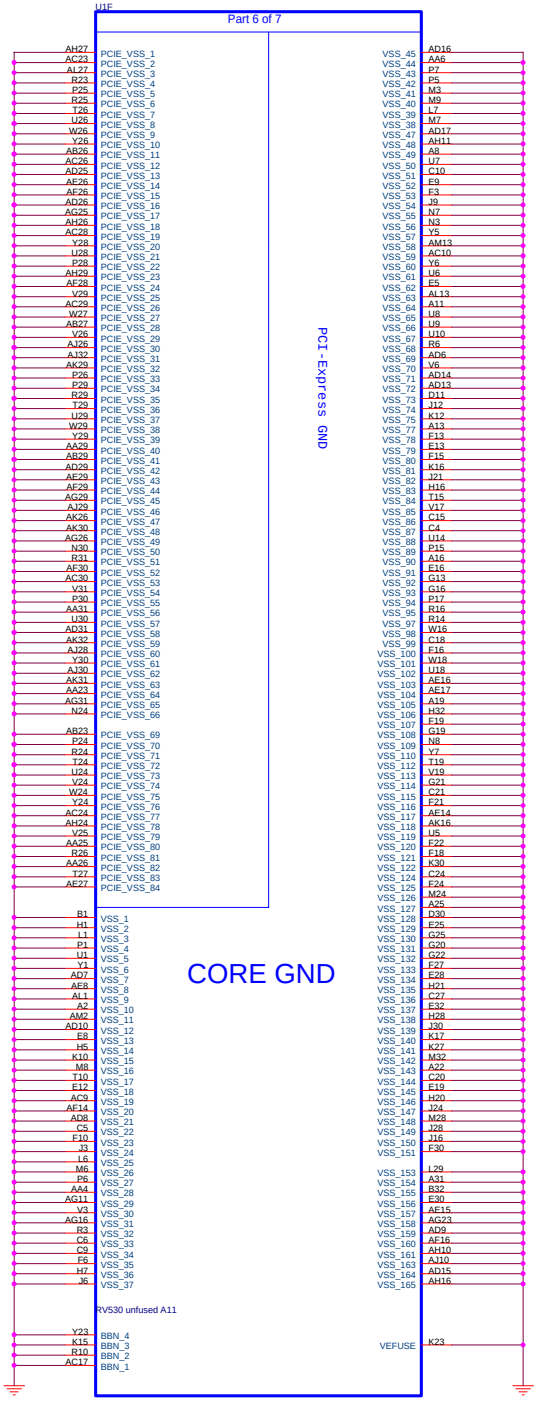

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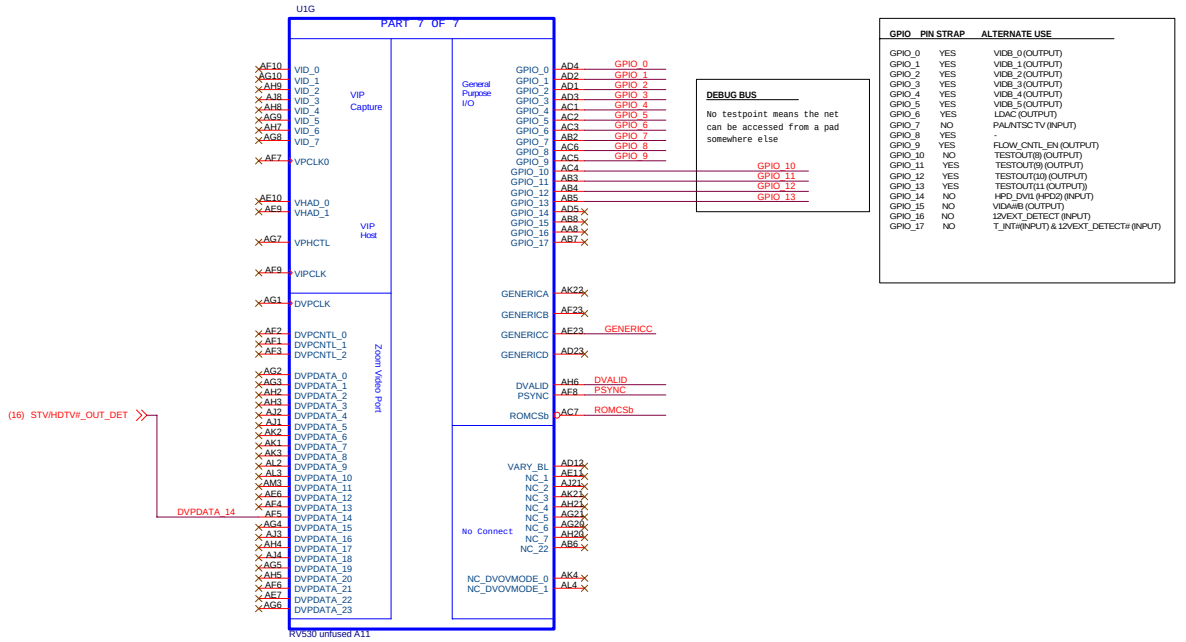
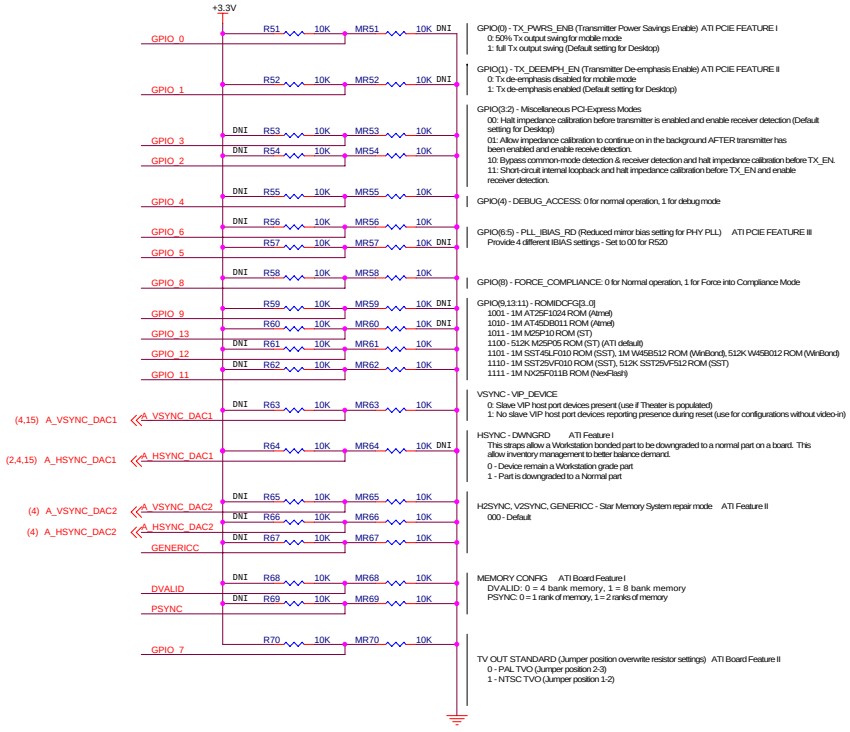
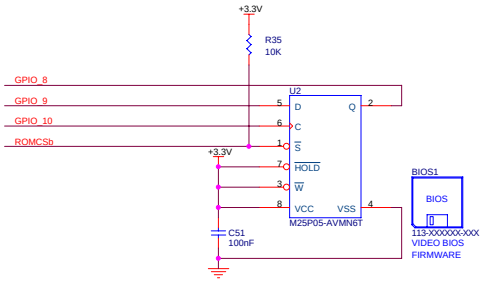


GPIO	PIN STRAP	ALTERNATE USE
GPIO_0	YES	VIDB_0 (OUTPUT)
GPIO_1	YES	VIDB_1 (OUTPUT)
GPIO_2	YES	VIDB_2 (OUTPUT)
GPIO_3	YES	VIDB_3 (OUTPUT)
GPIO_4	YES	VIDB_4 (OUTPUT)
GPIO_5	YES	VIDB_5 (OUTPUT)
GPIO_6	YES	LDAC (OUTPUT)
GPIO_7	NO	PAL/NTSC TV (INPUT)
GPIO_8	YES	-
GPIO_9	YES	FLOW_CNTL_EN (OUTPUT)
GPIO_10	NO	TESTOUT(8) (OUTPUT)
GPIO_11	YES	TESTOUT(9) (OUTPUT)
GPIO_12	YES	TESTOUT(10) (OUTPUT)
GPIO_13	YES	TESTOUT(11 (OUTPUT))
GPIO_14	NO	HPD_DVI1 (HPD2) (INPUT)
GPIO_15	NO	VIDAal/B (OUTPUT)
GPIO_16	NO	12VEXT_DETECT (INPUT)
GPIO_17	NO	T_INT#(INPUT) & 12VEXT_DETECT# (INPUT)

PIN BASED STRAPS





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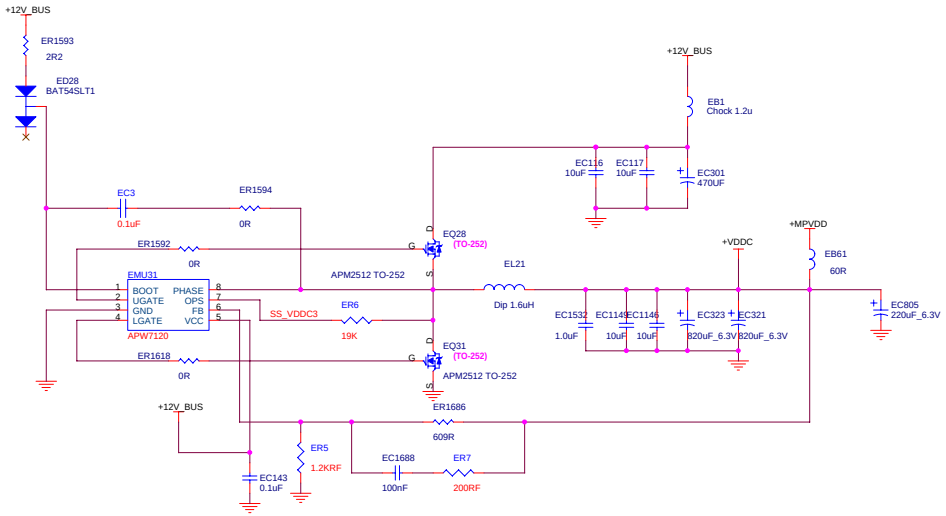
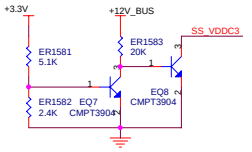
CORE REGULATOR +VDDC



+VDDC=1.2V



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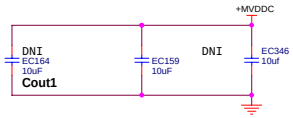

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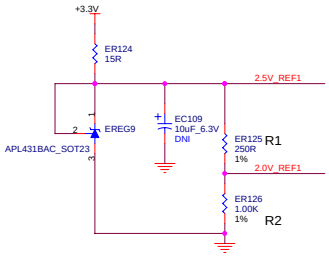

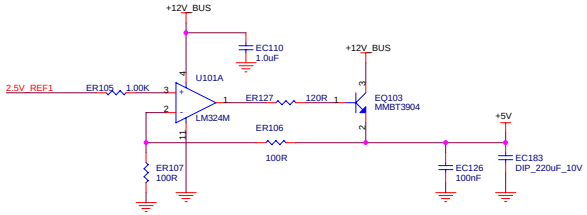

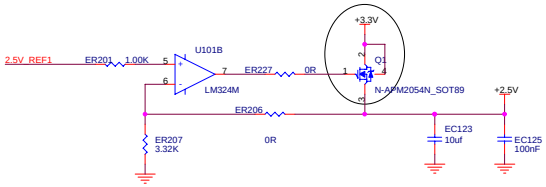

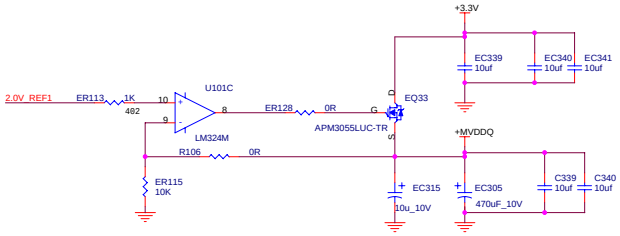

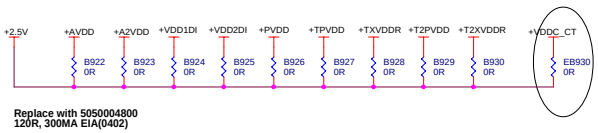

Replace with 5050004800
120R, 300MA EIA(0402)

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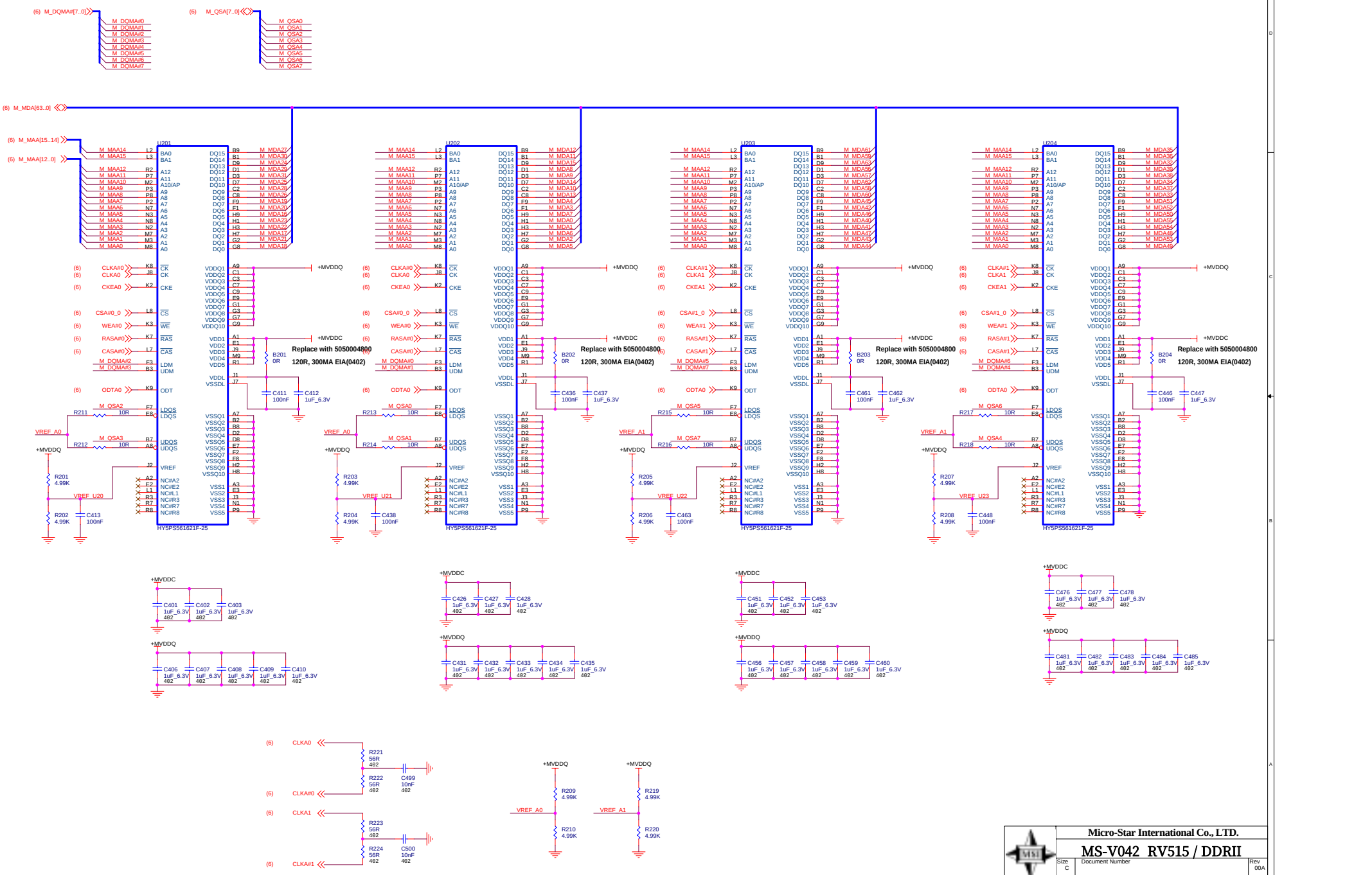
CHANNEL A: RANK 0 128MB DDR2



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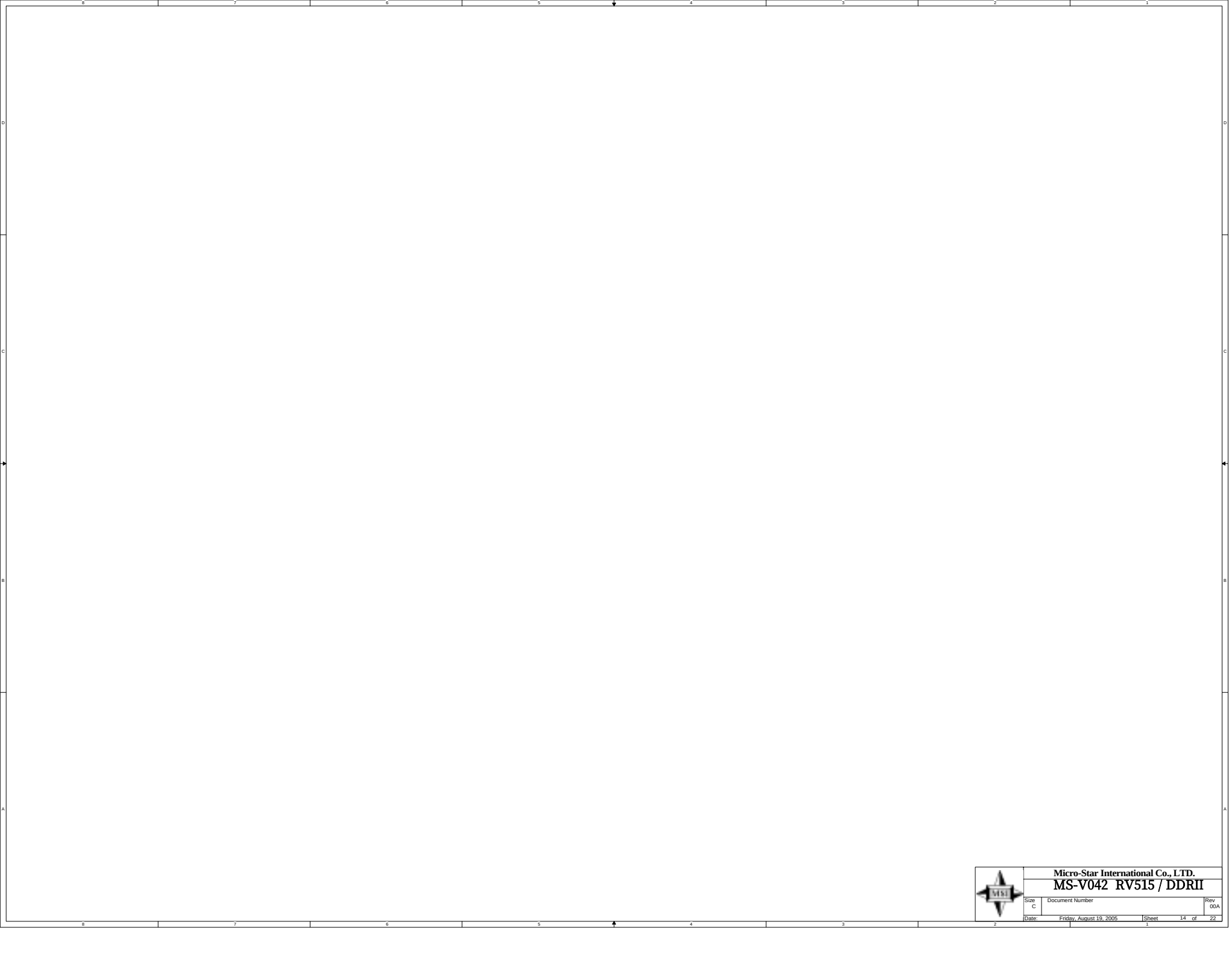

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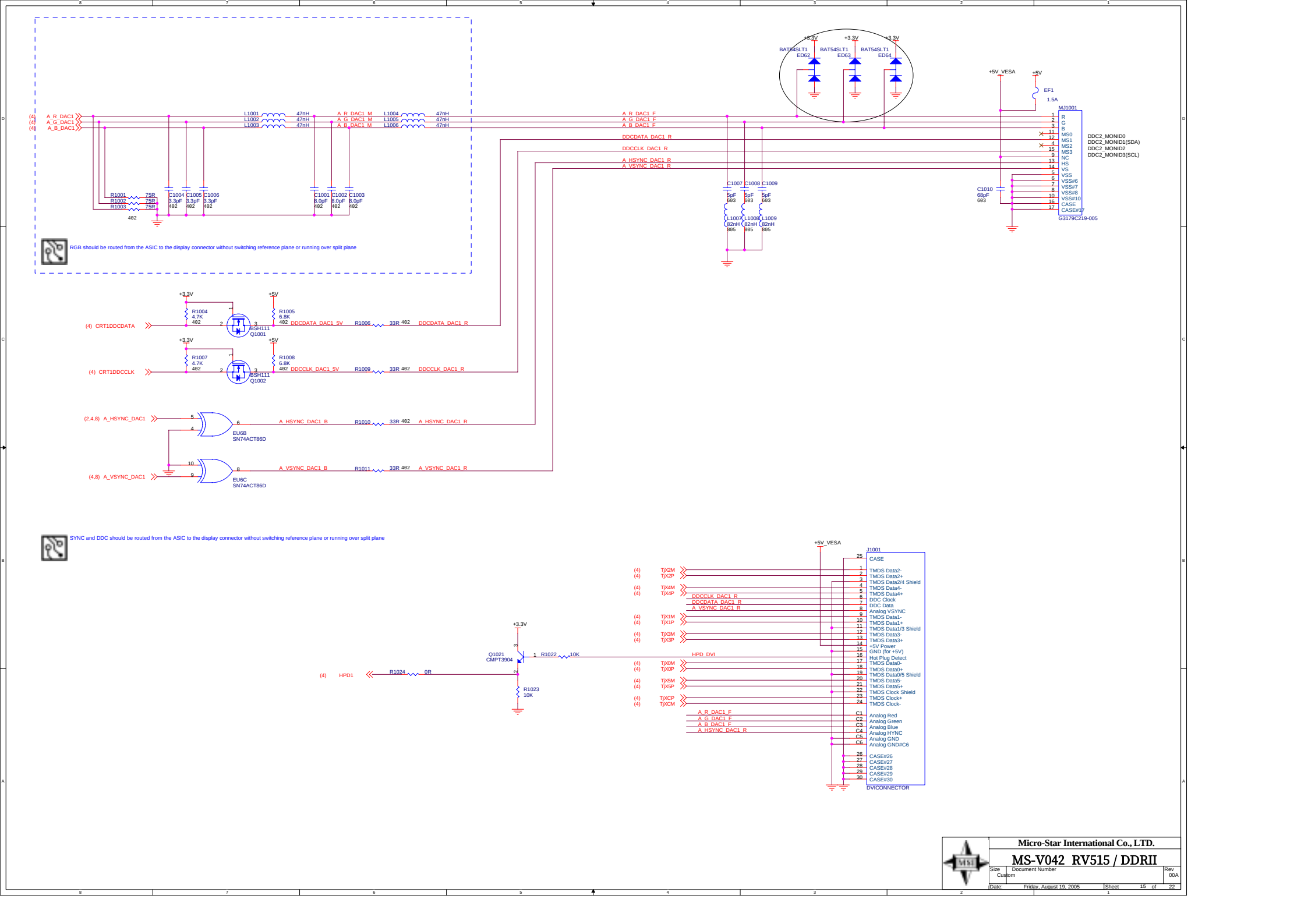
RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane
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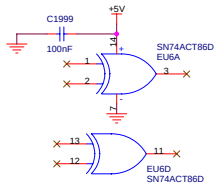

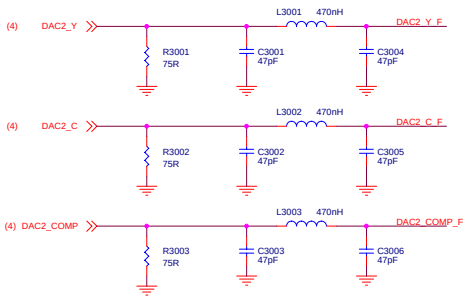

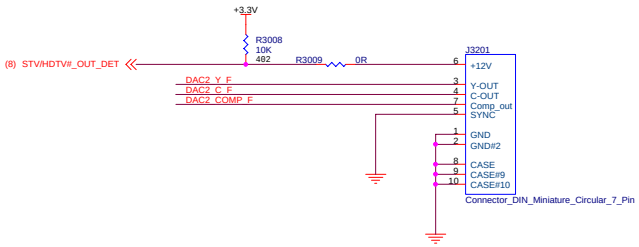

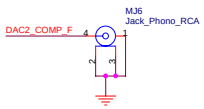

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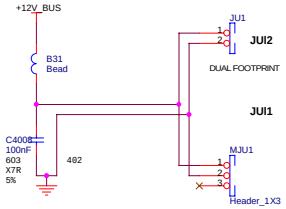

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DVI/VGA SCREWS

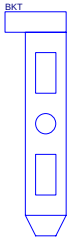
SCREW1

SCREW
JACKSCREW
ASSY
7020000800

SCREW2

SCREW
JACKSCREW
ASSY
7020000800

BKT



PCB

H2

LOW PROFILE HS

FM1
SW_FB

FM2
SW_FB

FM3
SW_FB

FM4
SW_FB

FM5
SW_FB

FM6
SW_FB

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