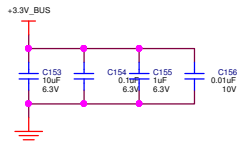
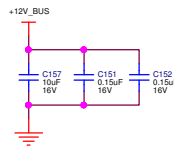
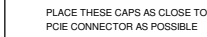
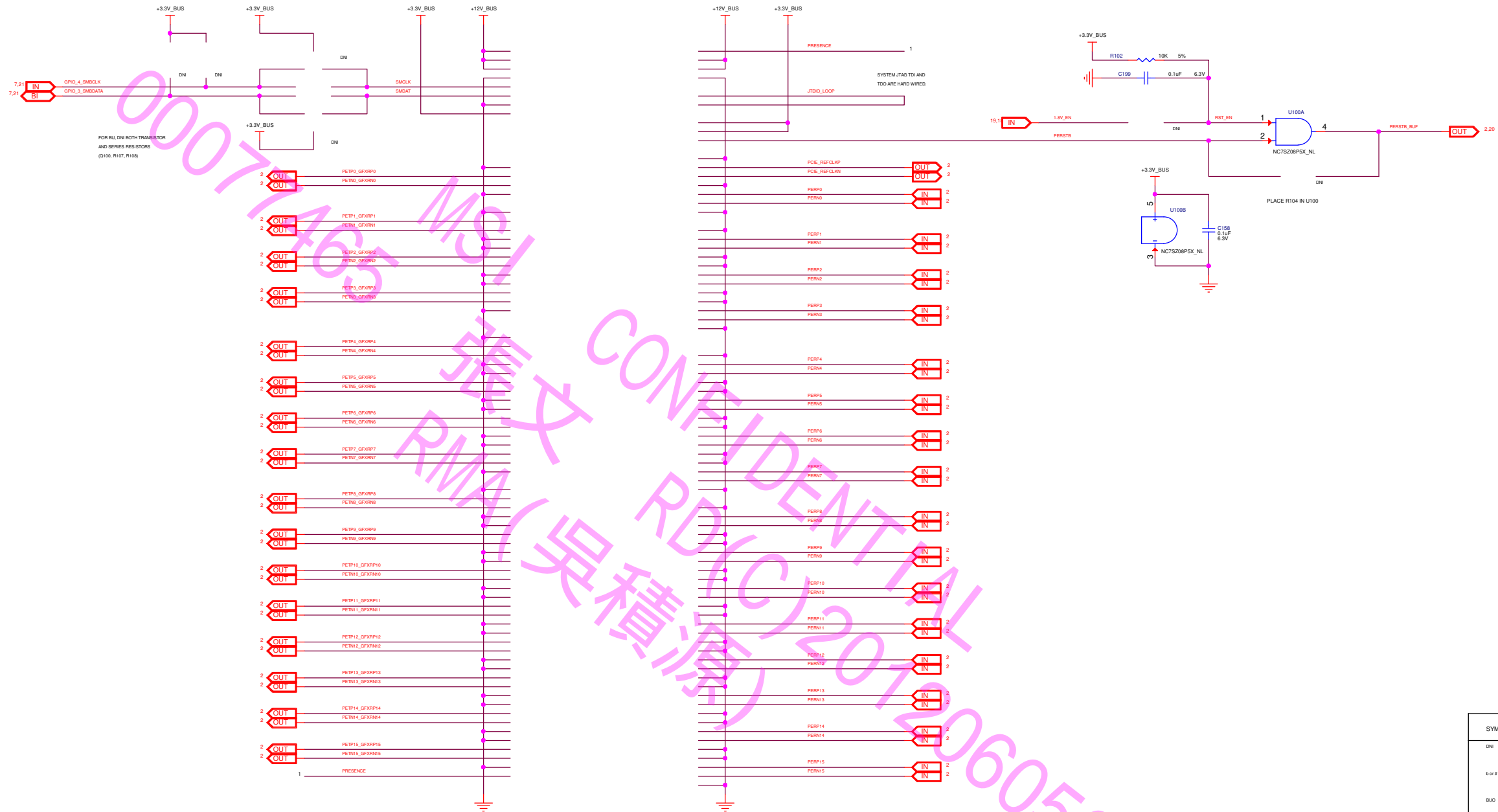




(1) PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
b or #	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

AMD - GRAPHICS
1 COMMERCE VALLEY
MARKHAM, ONTARIO, L3T 7X6


SHEET:

DATE: PCT/EURO/2015/04011

SHEET NUMBER: 1 OF 23

DOCUMENT NUMBER: 102-C40304-00

NOTES: NOTE



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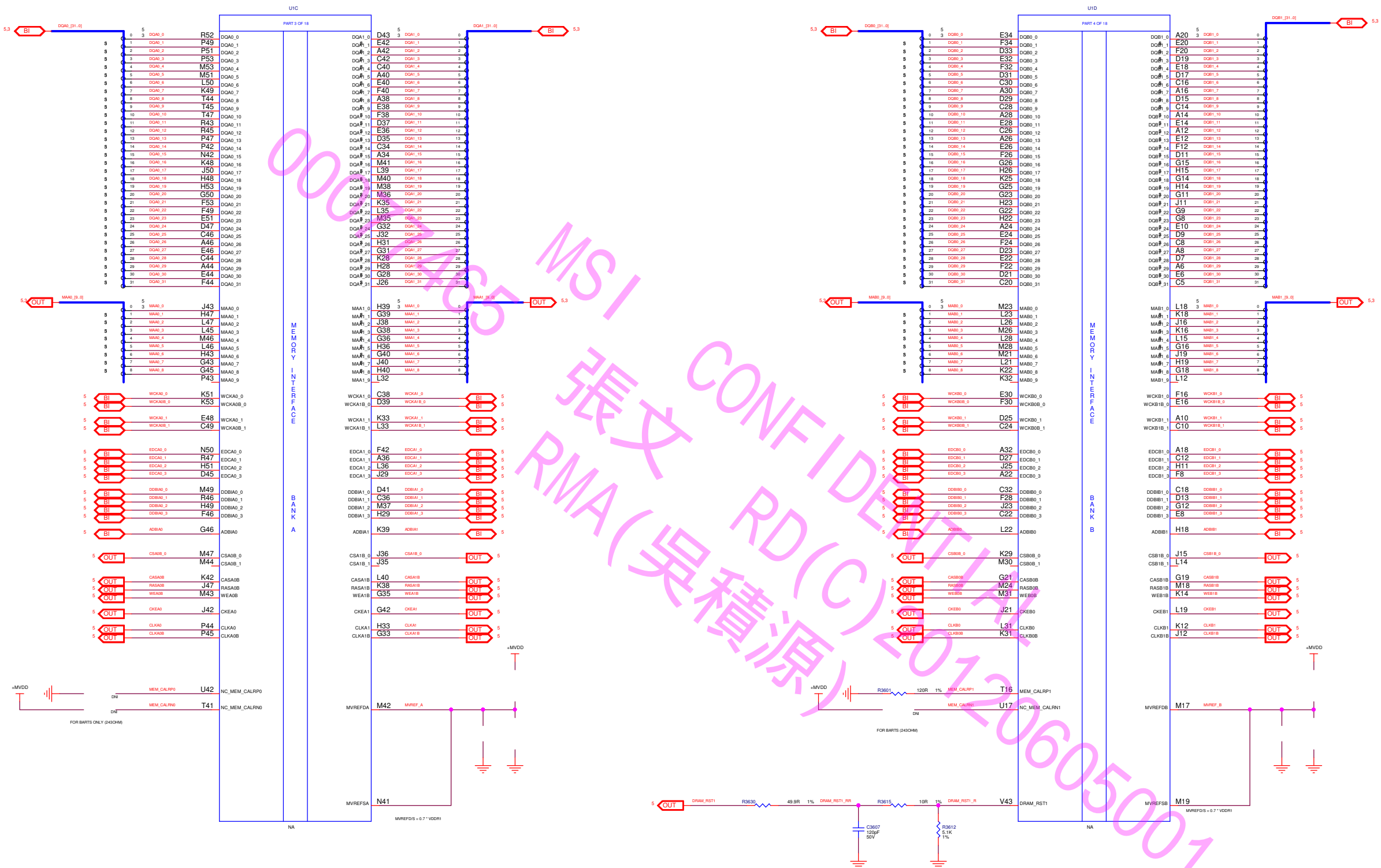
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TITLE:	TITLE
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(3) PITCAIRN MEM INTERFACE CH A/B



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SHEET:

DATE: 2016-08-25-AR2011

REV: 08

SHEET NUMBER: 3 OF 23

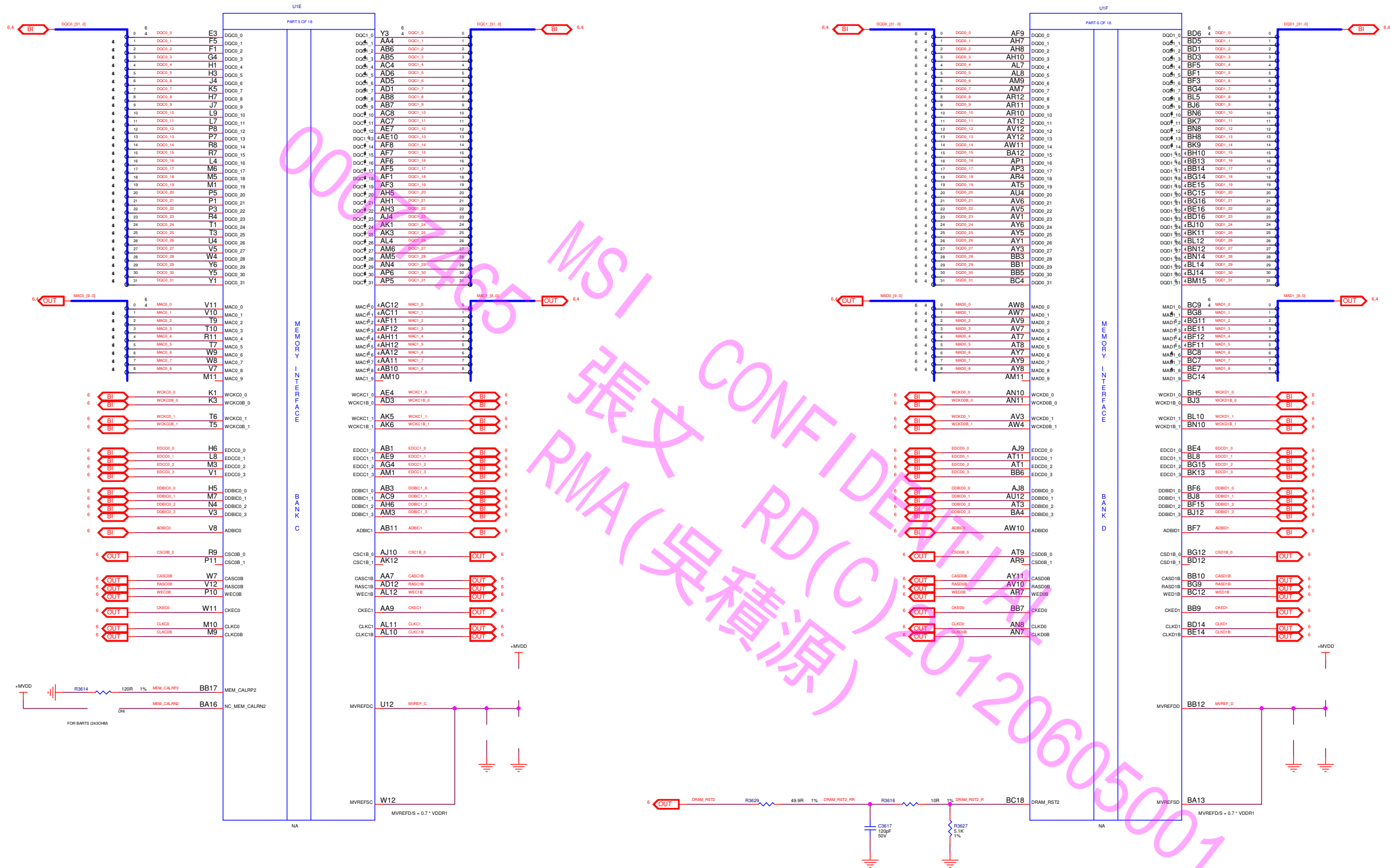
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TITLE:

(4) PITCAIRN MEM INTERFACE CH C/D



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MARKHAM, ONTARIO, L3T 7X6

SHEET:

DATE: 2011-03-08

SHEET NUMBER: 4 OF 23

DOCUMENT NUMBER: 102-C40304-00

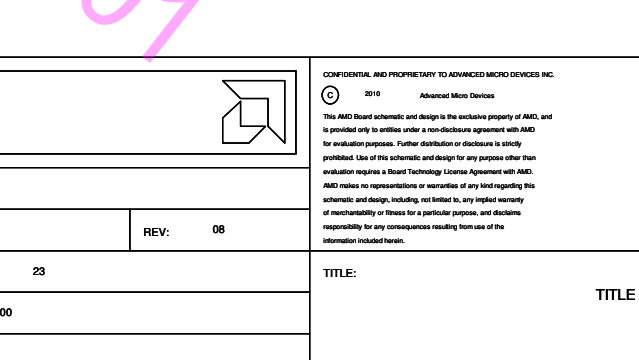
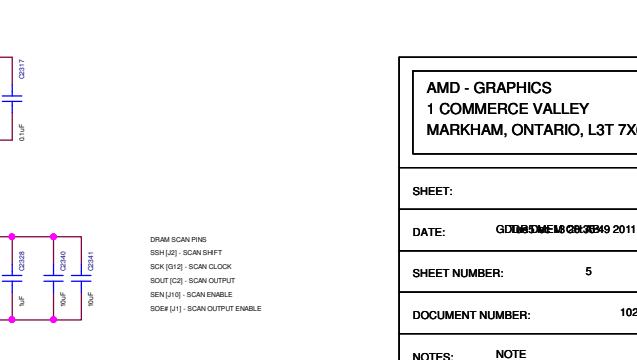
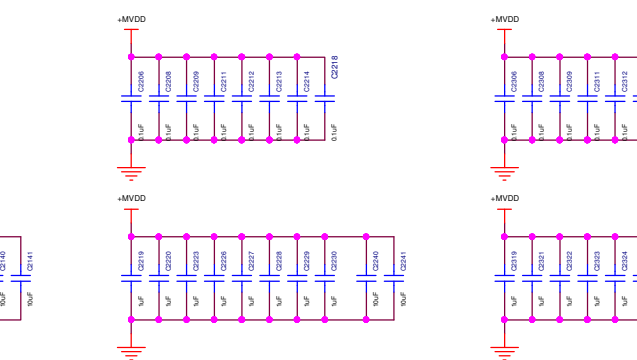
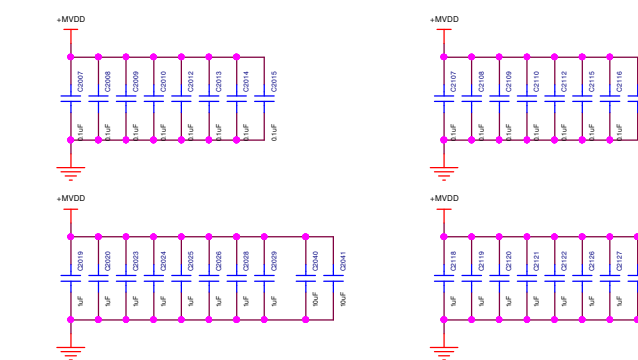
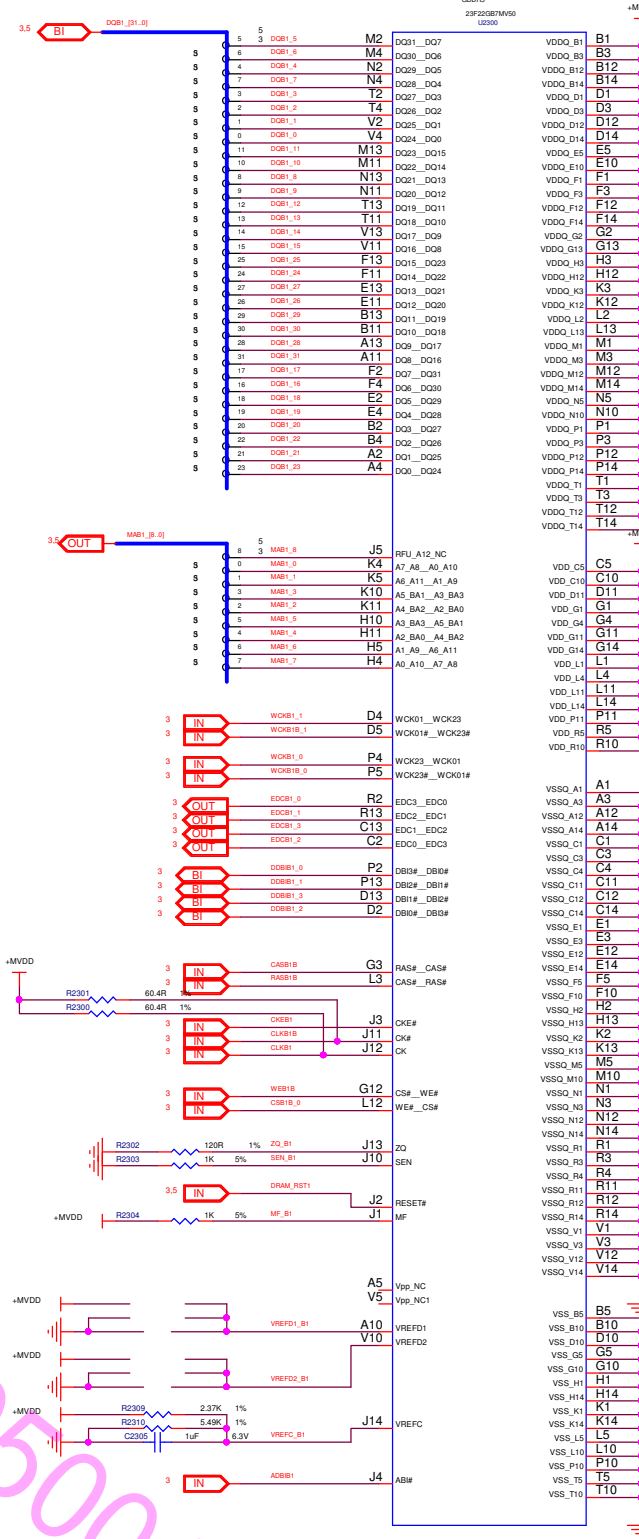
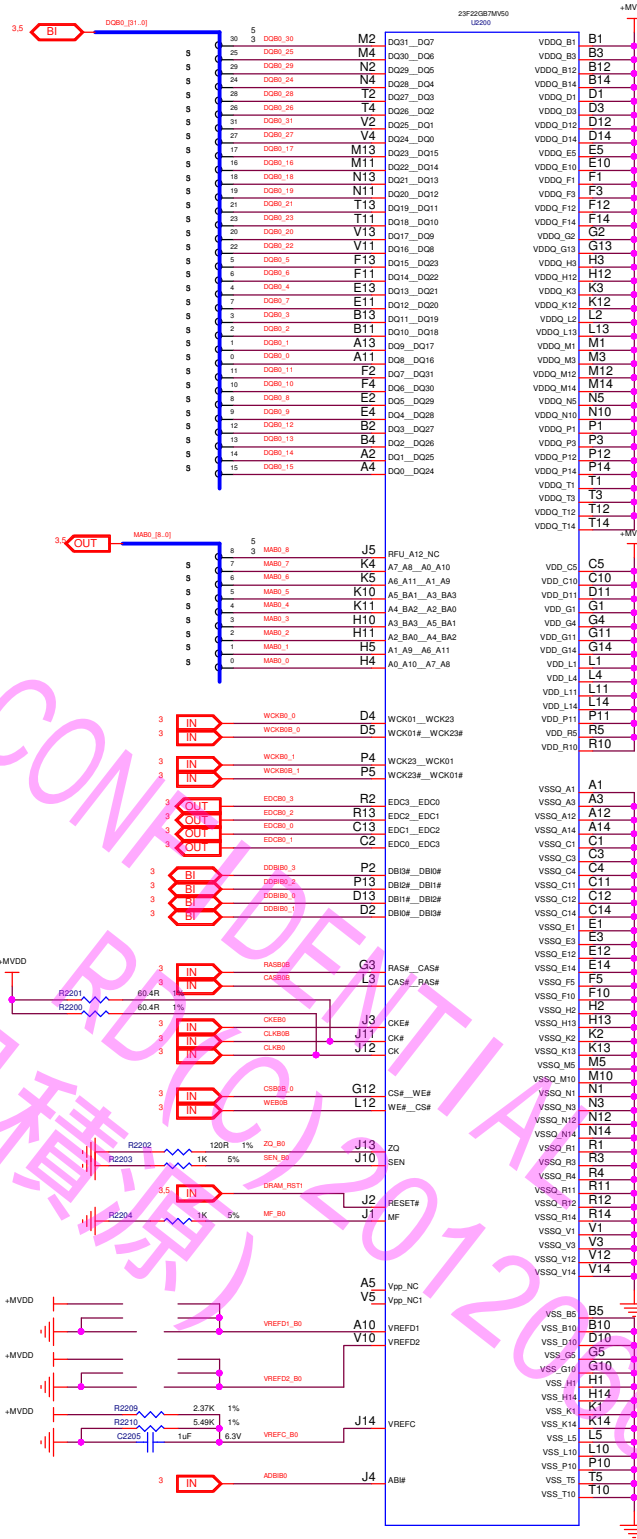
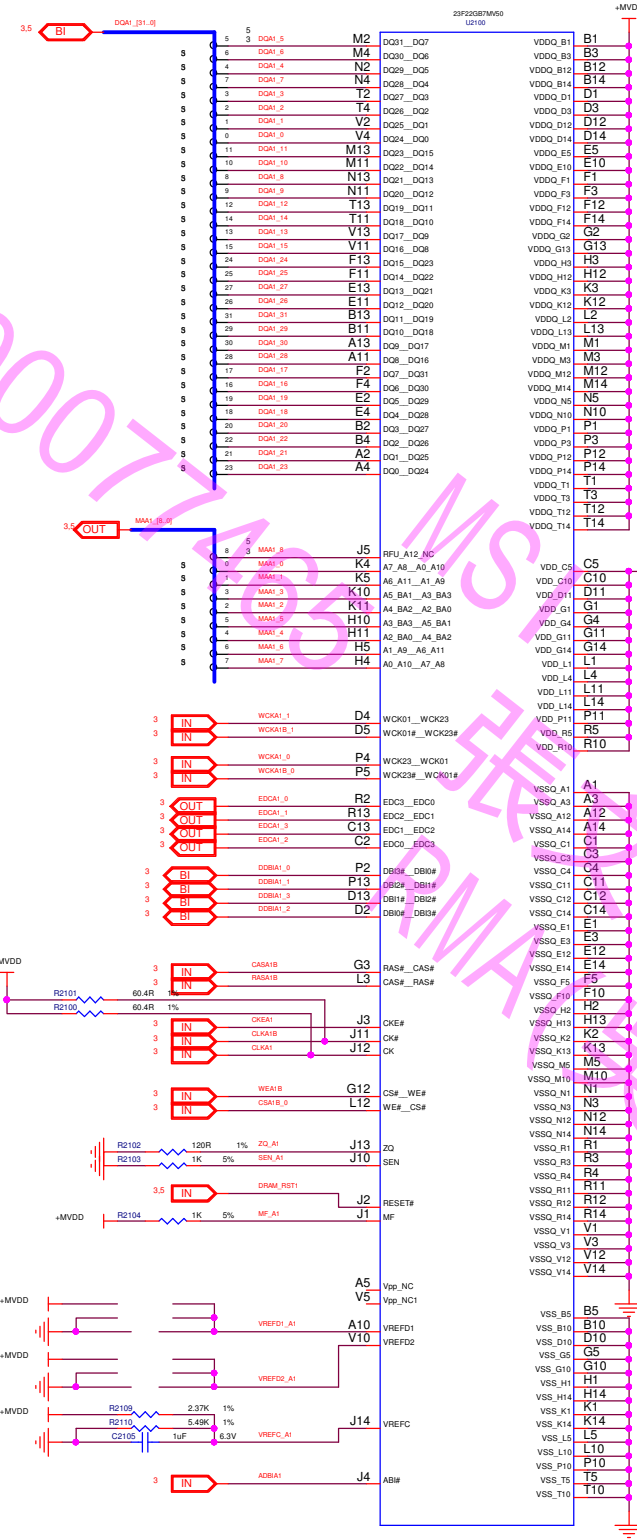
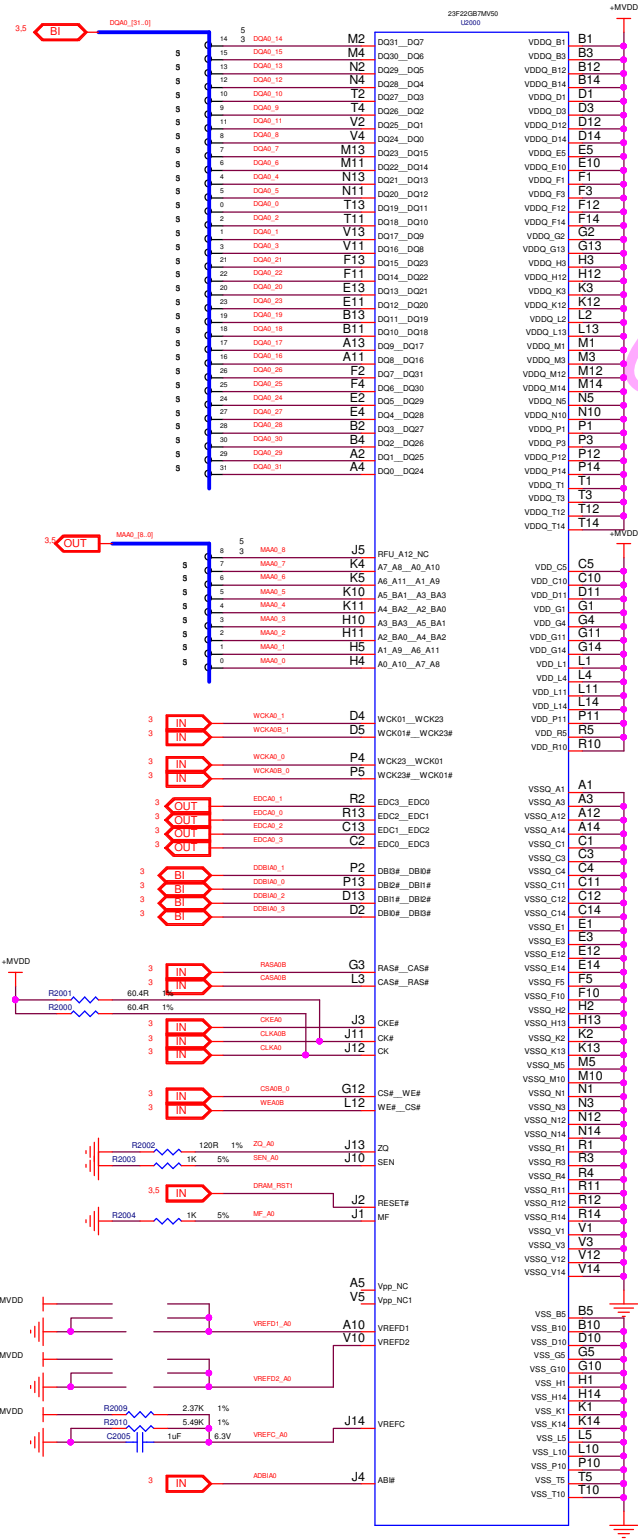
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REV: 08

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(5) GDDR5 MEMORY CH A/B



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SHEET:

DATE: 2011-08-08

REV: 08

SHEET NUMBER: 5 OF 23

DOCUMENT NUMBER: 102-C40304-00

NOTES: NOTE

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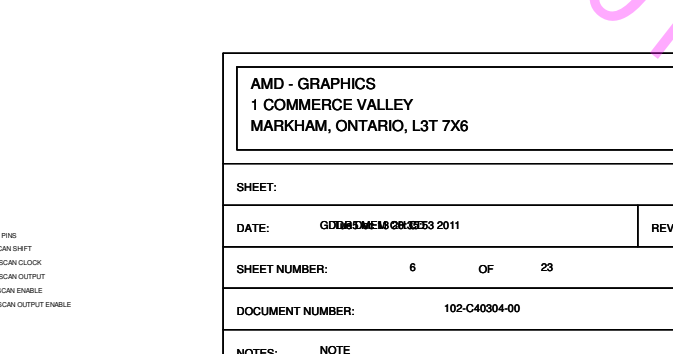
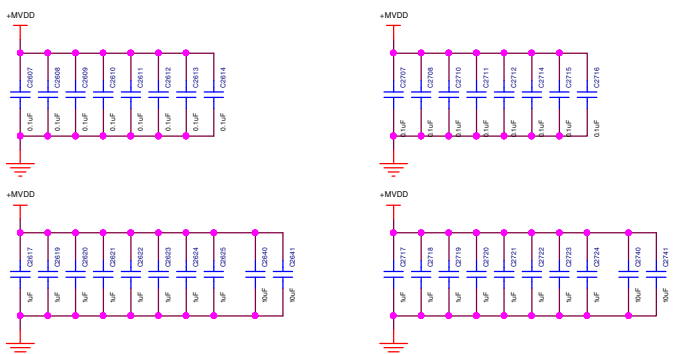
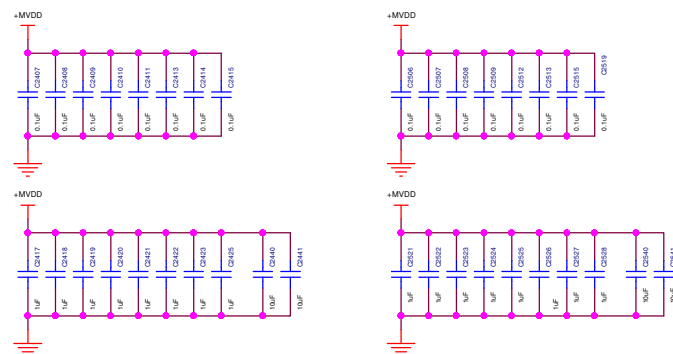
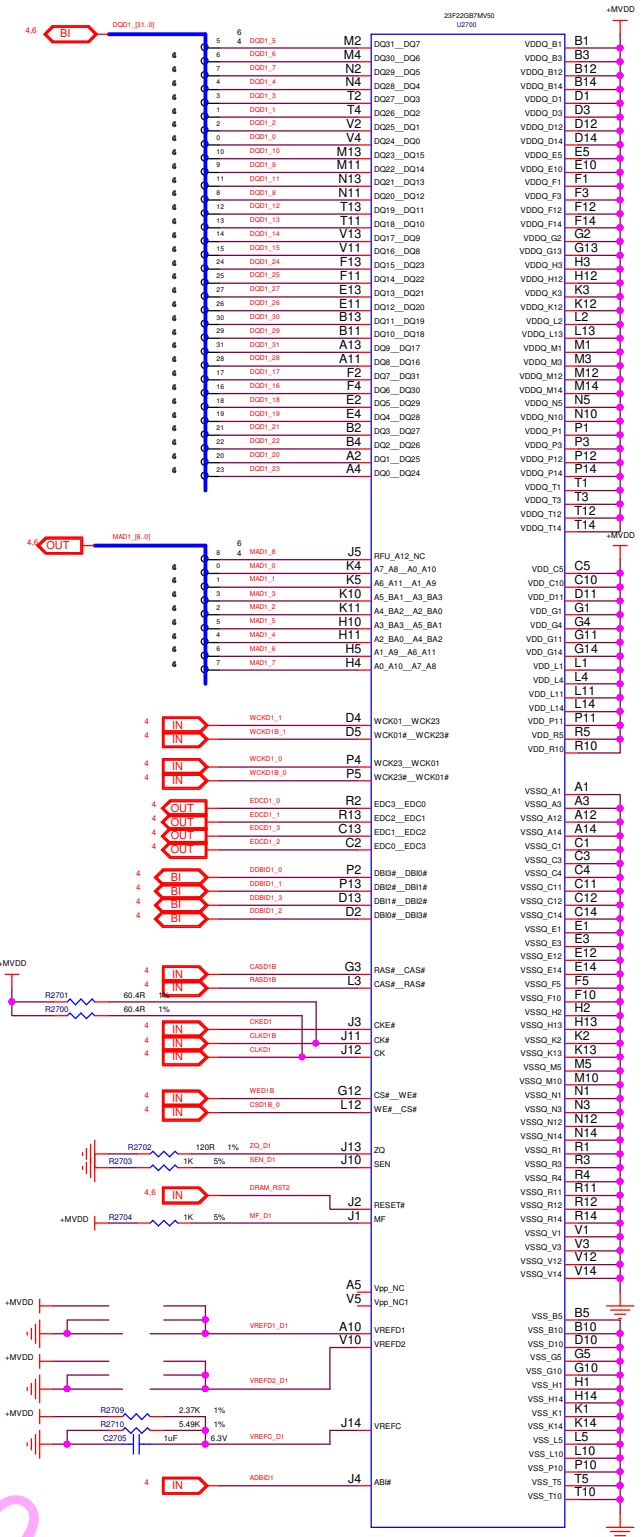
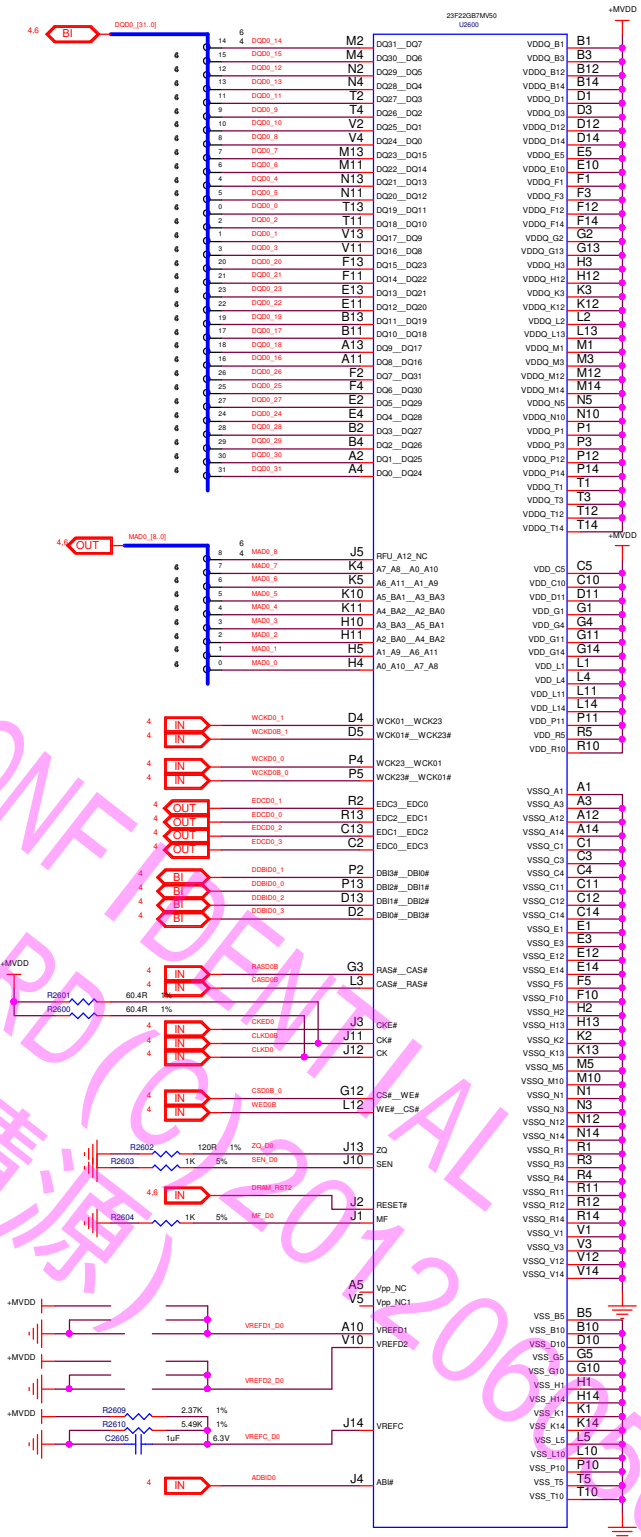
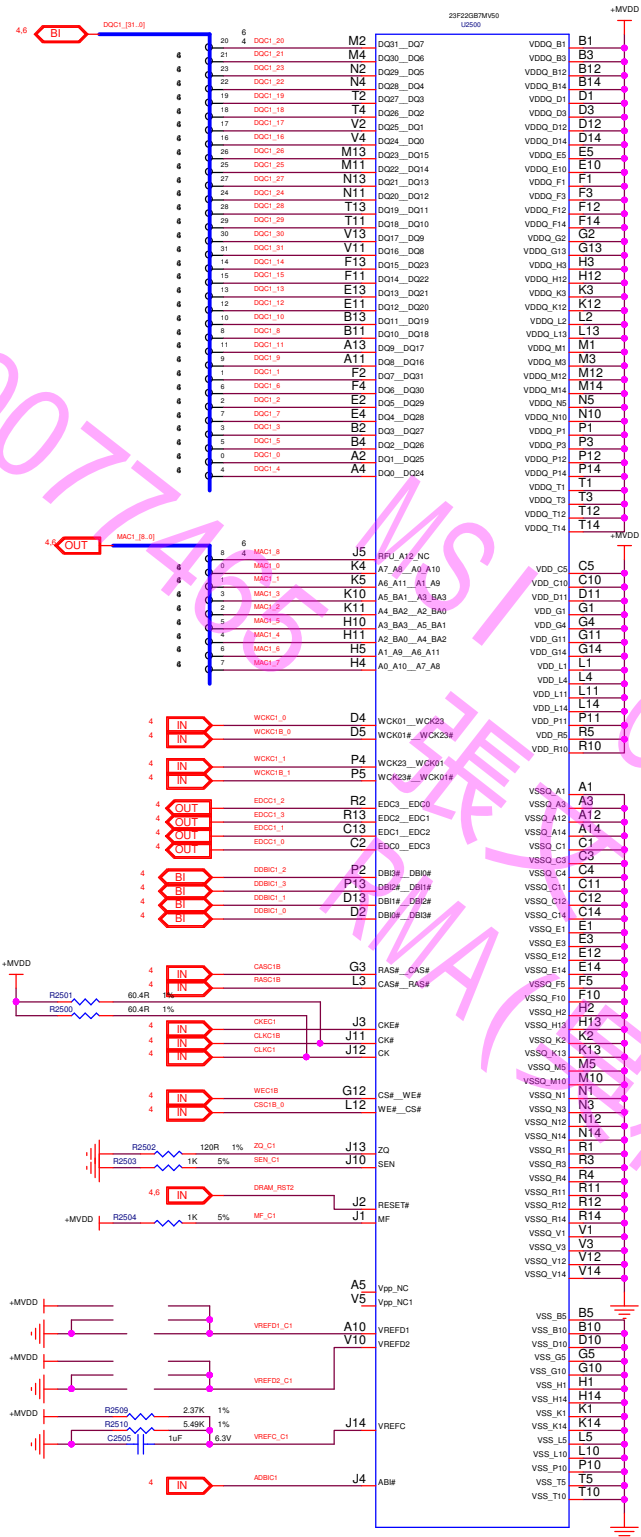
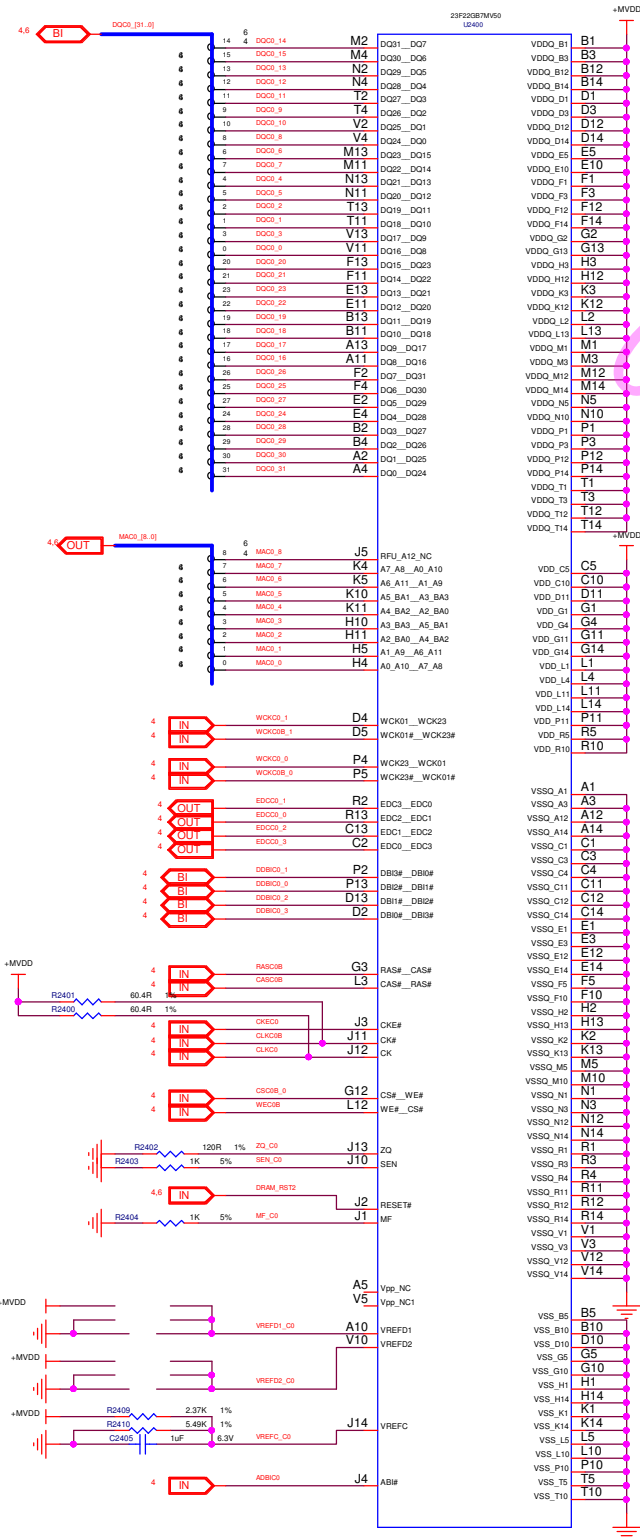
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(6) GDDR5 MEMORY CH C/D



AMD - GRAPHICS 1 COMMERCE VALLEY MARKHAM, ONTARIO, L3T 7X6		
SHEET:		
DATE: 2008-05-23 2011		REV: 06
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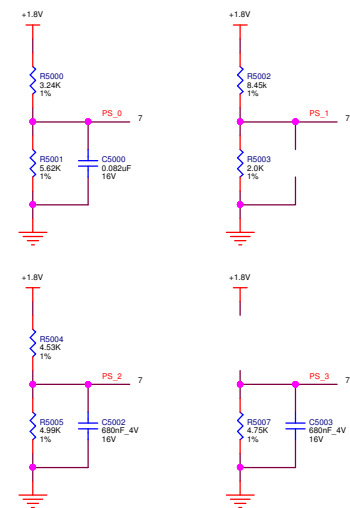
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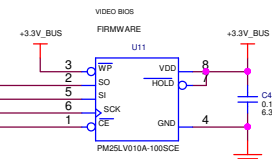
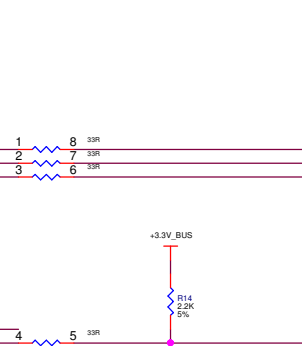
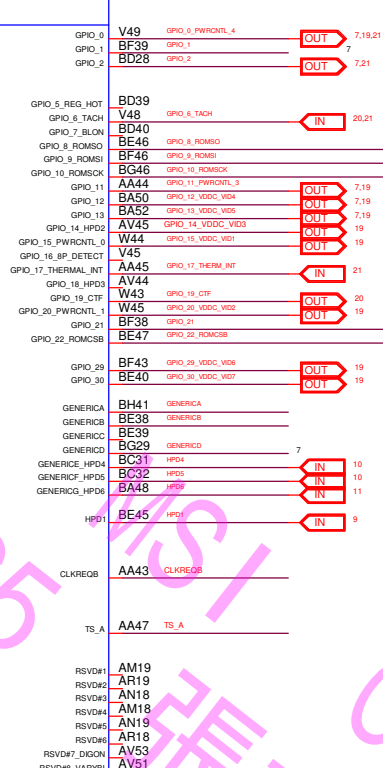
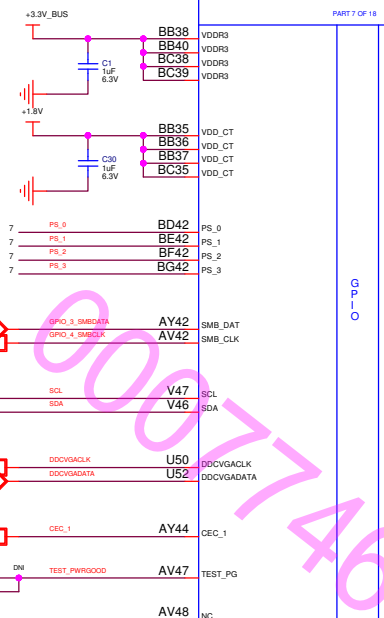
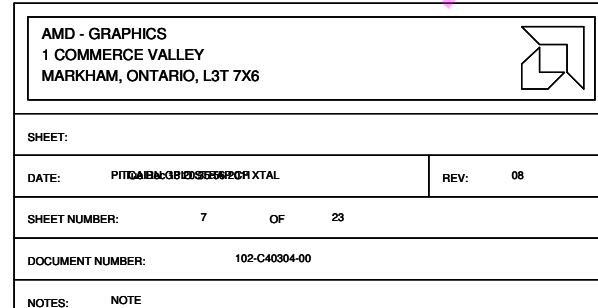
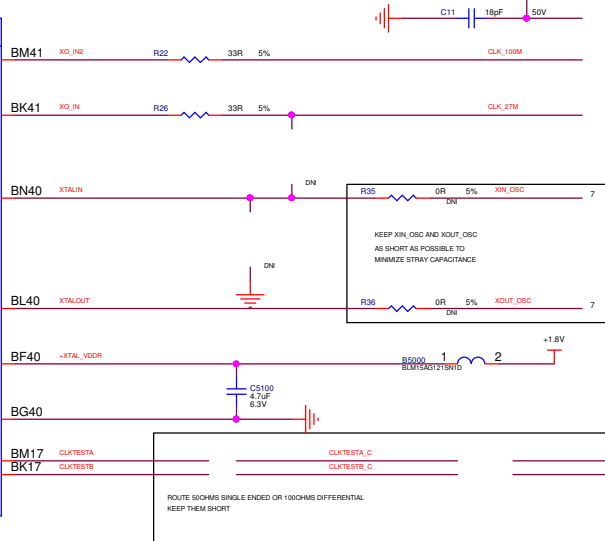
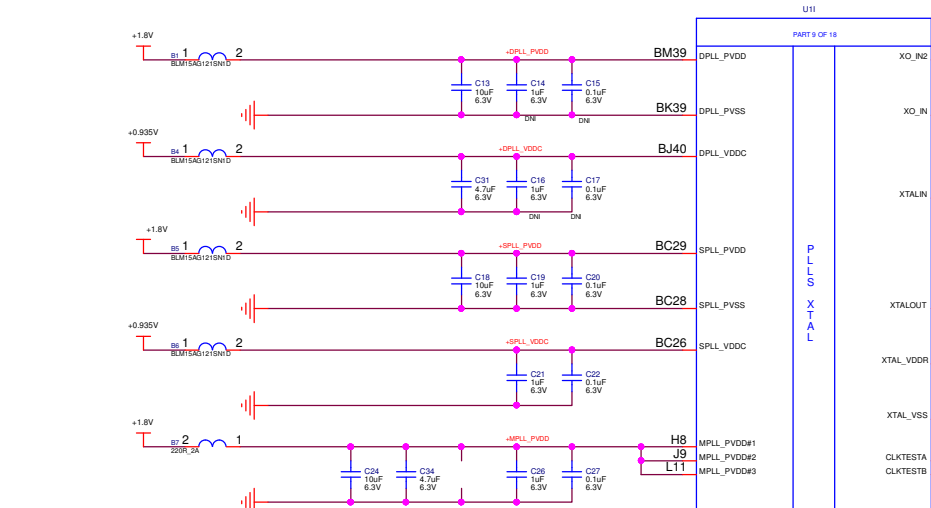
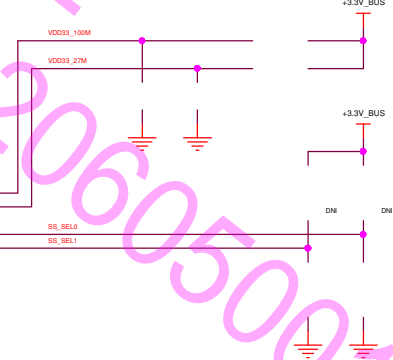
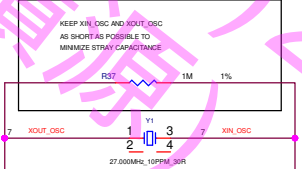
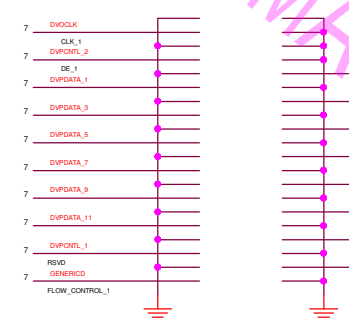
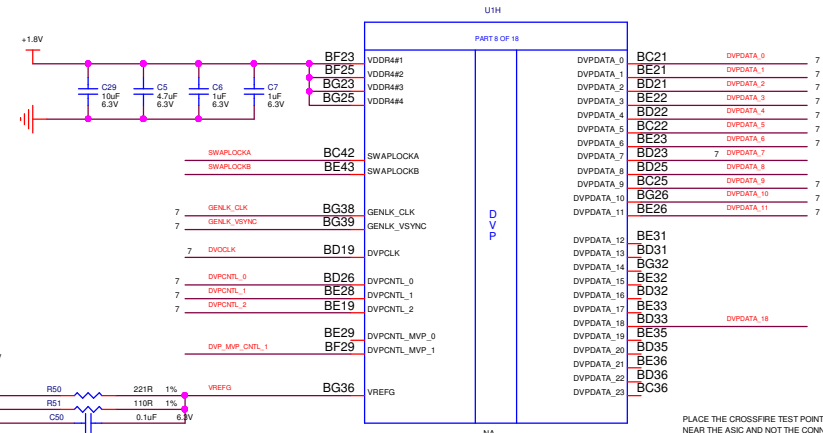
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(7) PITCAIRN GPIO STRAP CF XTAL



I2C ADDRESS	FUNCTION	DEVICE

I2C ADDRESS	FUNCTION	DEVICE
0x98	EXT TEMP SENSOR	LM96163

[illegible]

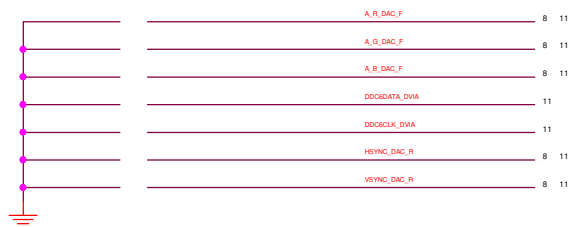
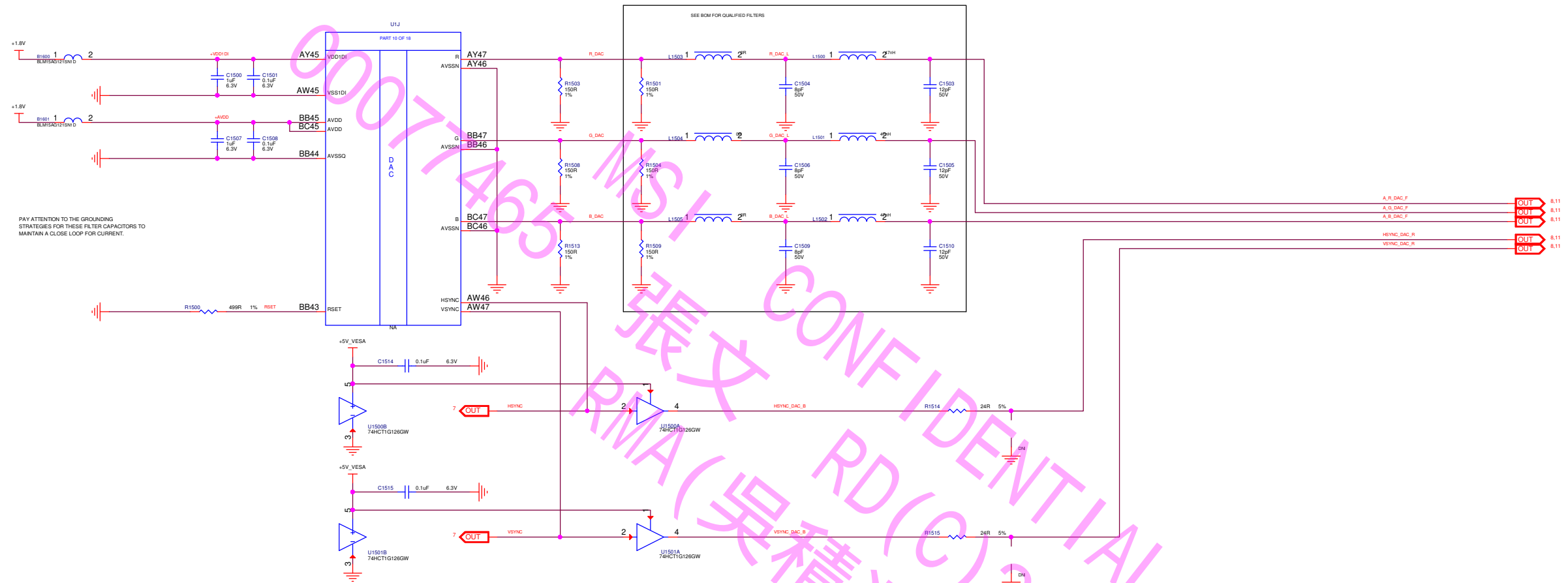
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TITLE:	TITLE
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(8) PITCAIRN DAC1 LOCK



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DATE: Tue Dec 13 20:36:00 2011

REV: 08

SHEET NUMBER: 8 OF 23

DOCUMENT NUMBER: 102-C40304-00

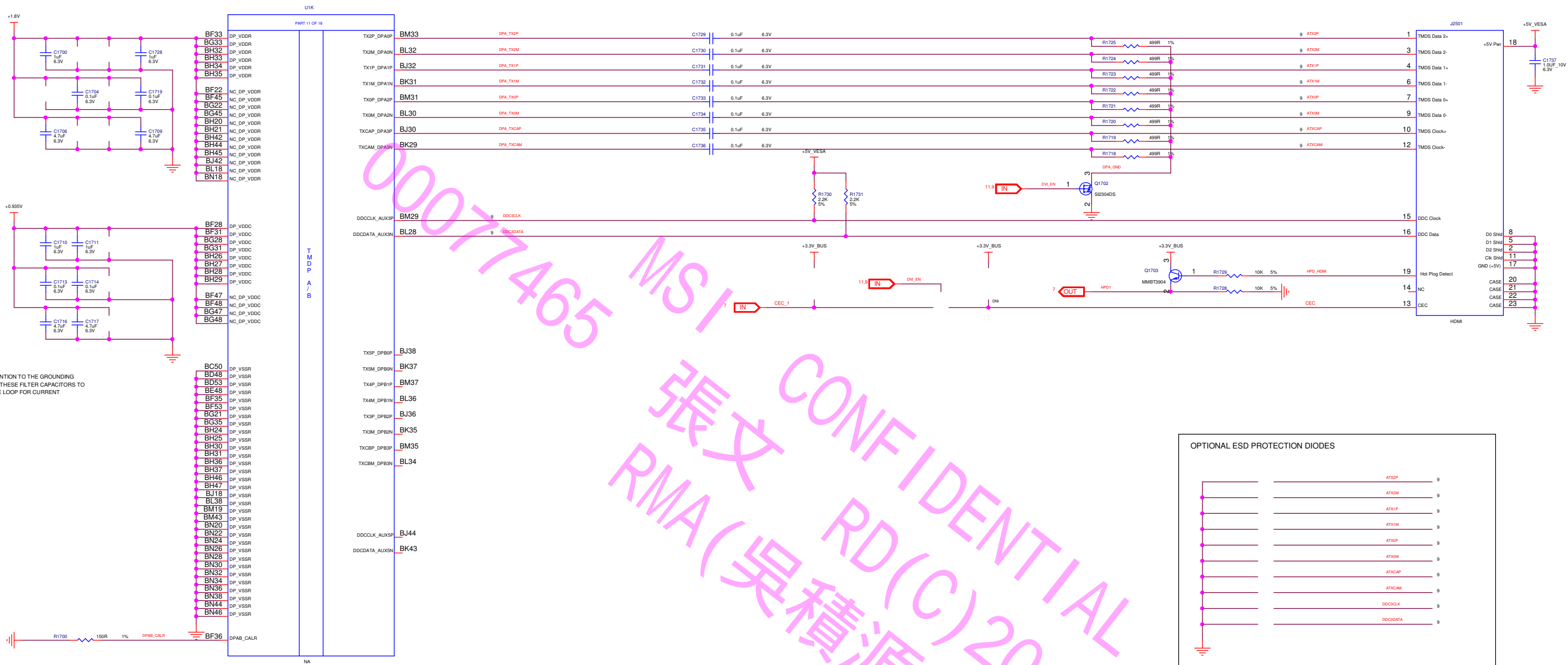
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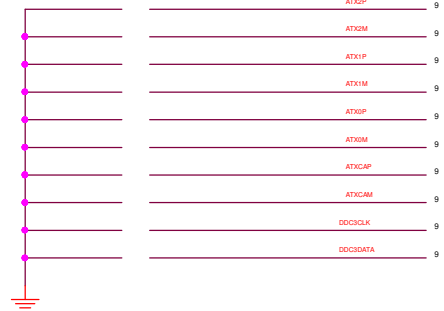
TITLE:

TITLE

(9) PITCAIRN TMDP A/B



OPTIONAL ESD PROTECTION DIODES



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SHEET NUMBER

DOCUMENT NUMBER:

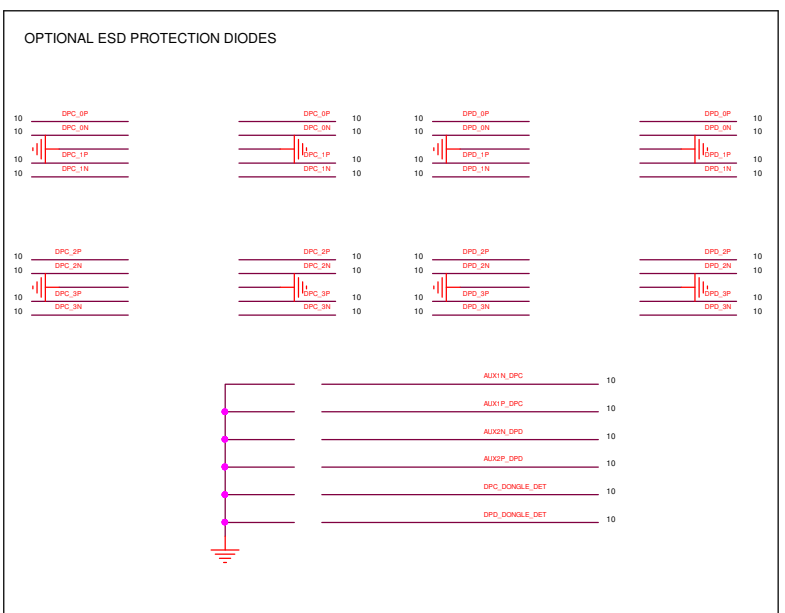
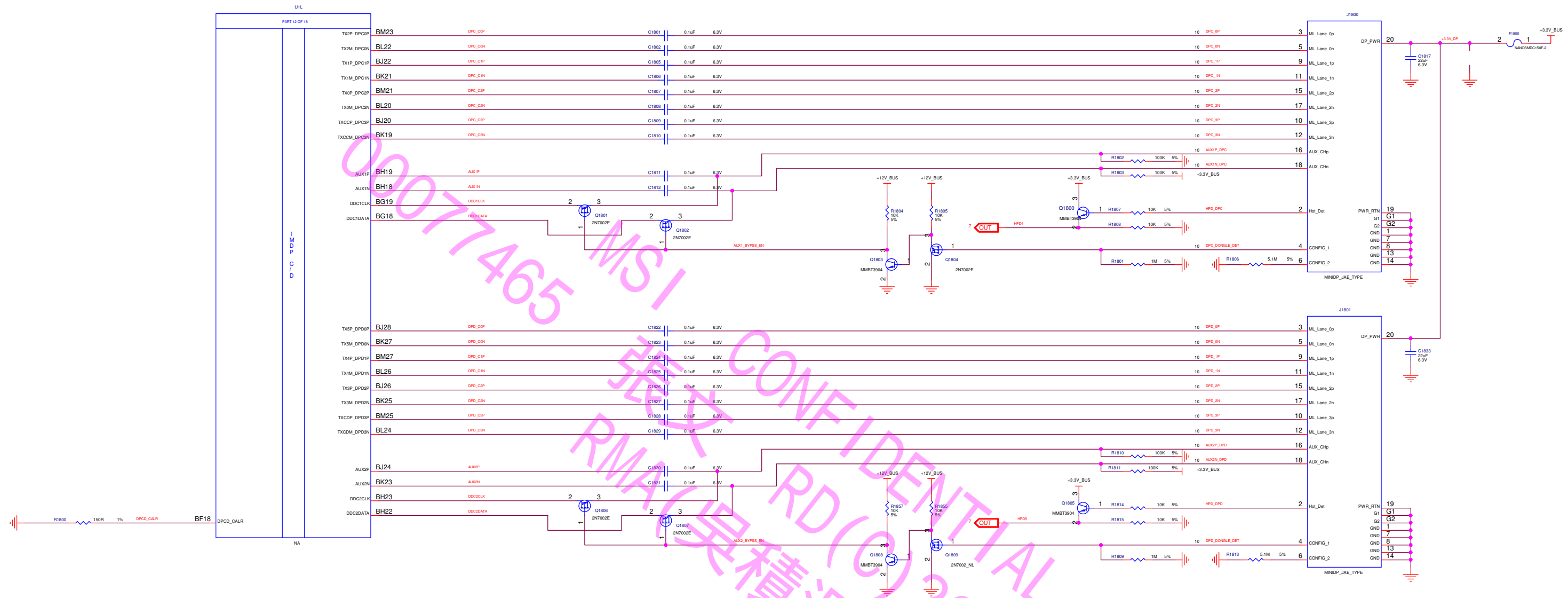
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REV: 08

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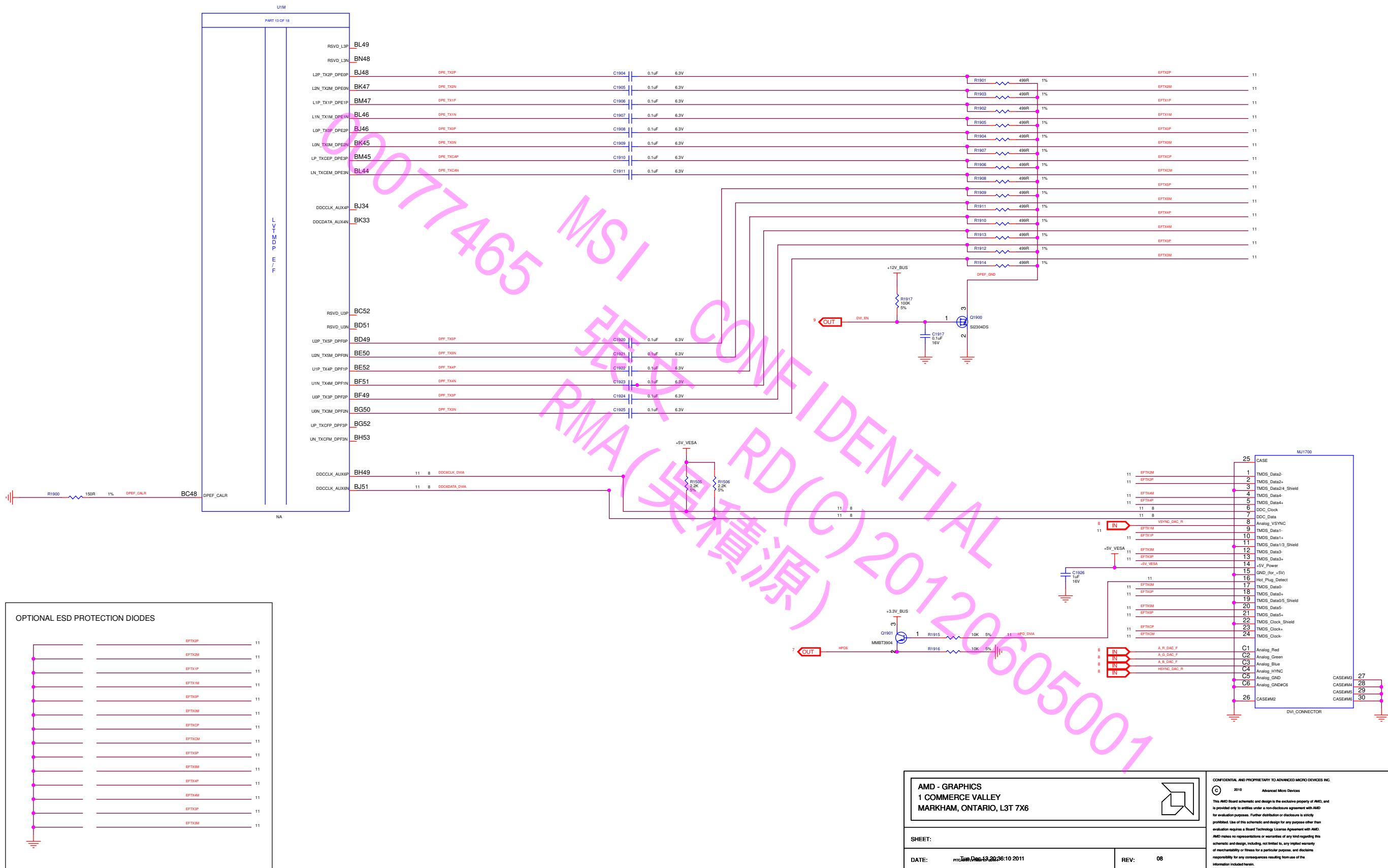
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(10) PITCAIRN TMDP C/D



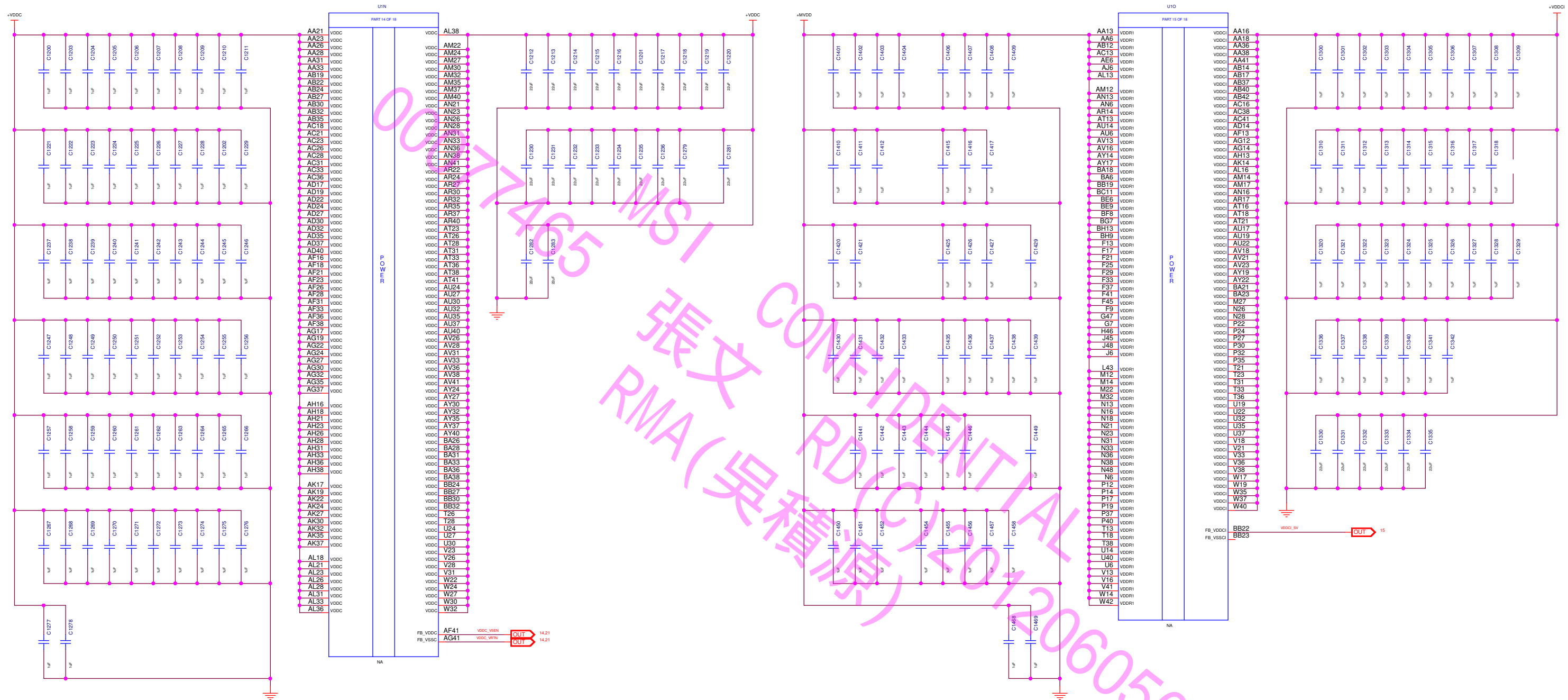
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SHEET:					
DATE:	JUN 06 2010 JUN 06 2010	REV:	08		
SHEET NUMBER:	10	OF	23	TITLE:	
DOCUMENT NUMBER:	102-C40304-00			TITLE	
NOTES:	NOTE				

(11) PITCAIRN LVTMDP E/F



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DATE: 2010-09-20 10:10:11	REV: 06	
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DOCUMENT NUMBER: 102-C40304-00		
NOTES: NOTE		TITLE:

(12) PITCAIRN POWER



1 COMMERCE VALLEY
AMBIKAMPONARIO, L3T 7X6

SHEET:

DATE: 2013 20:36:14 2011

REV: 08

SHEET NUMBER: 12 OF 23

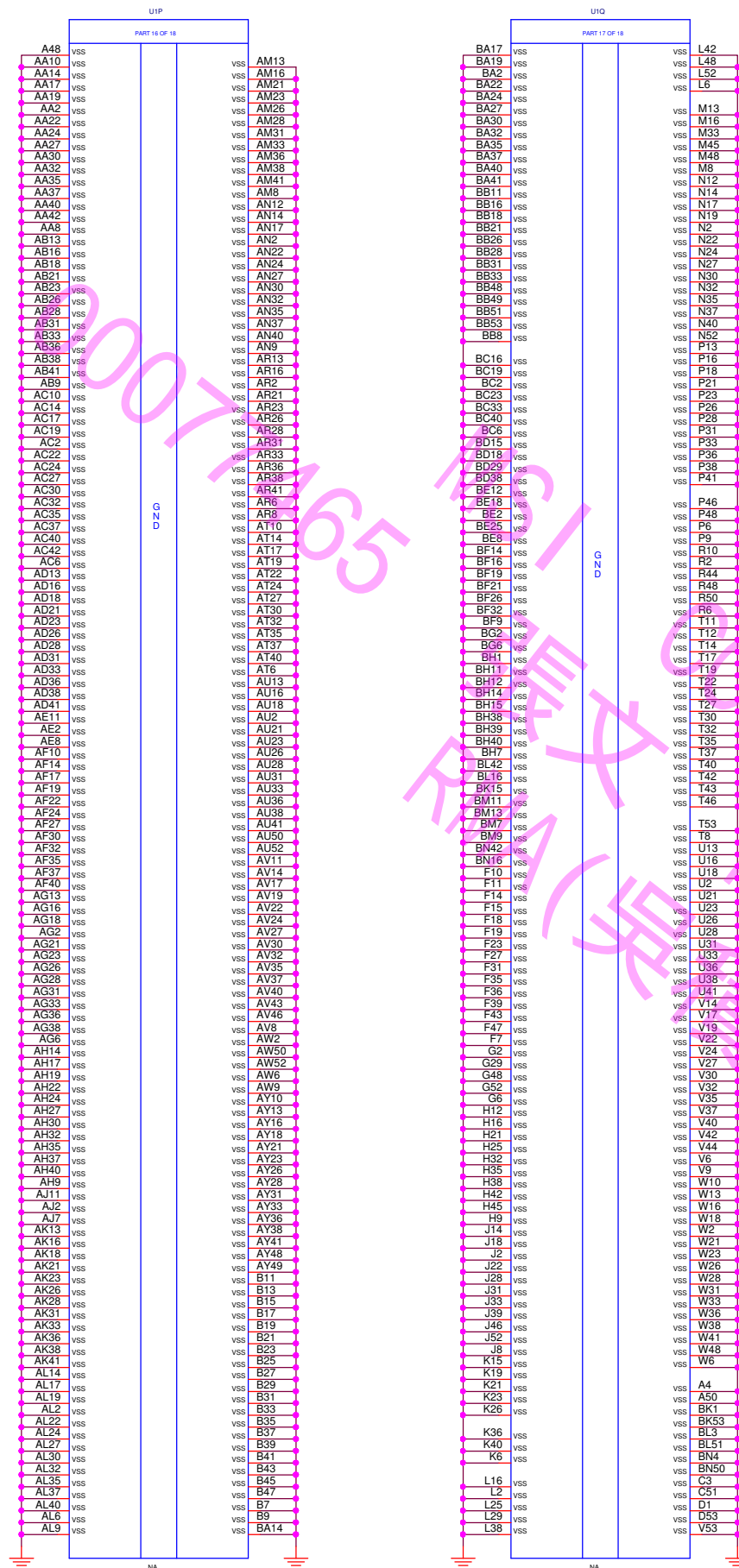
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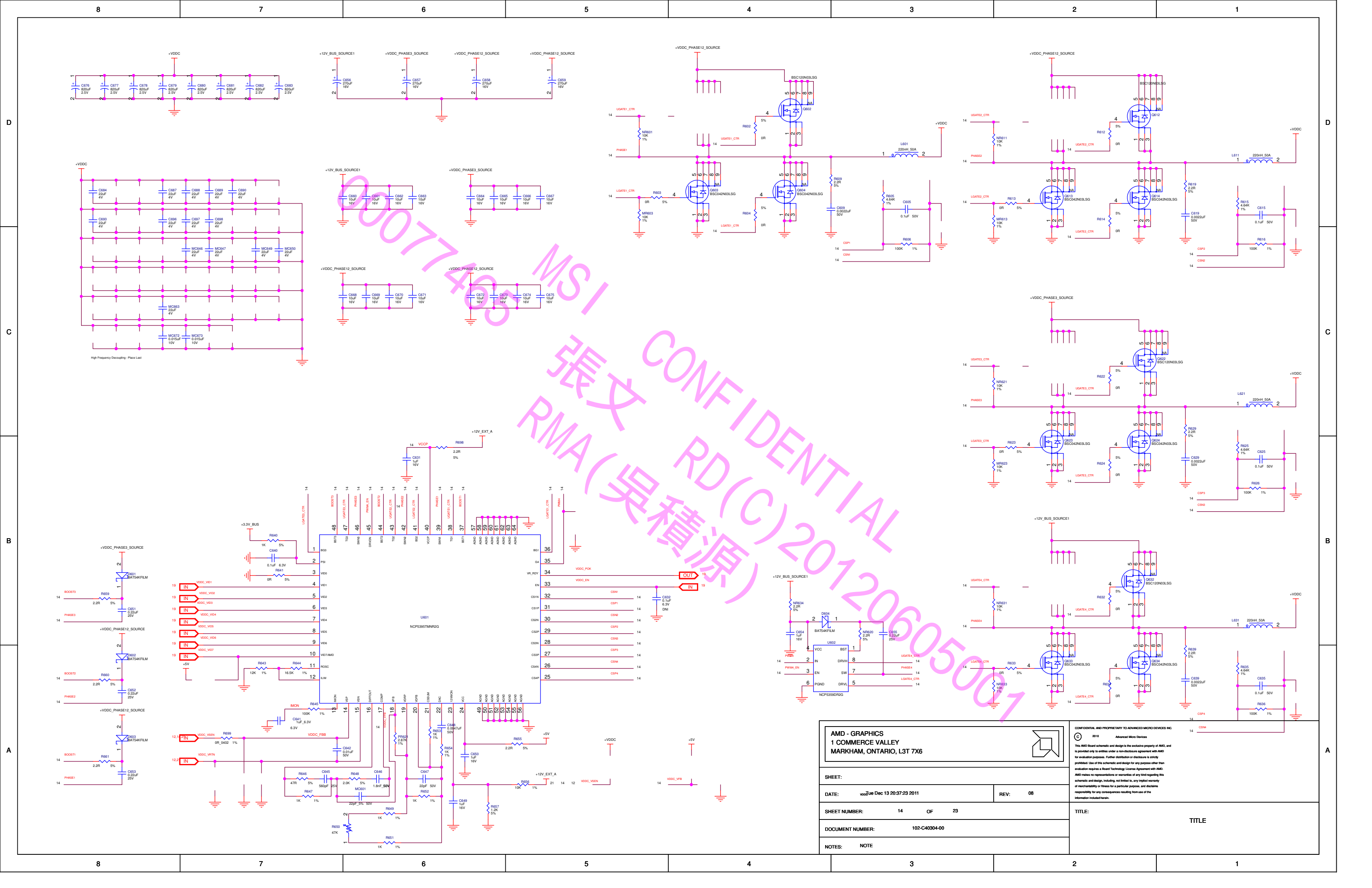
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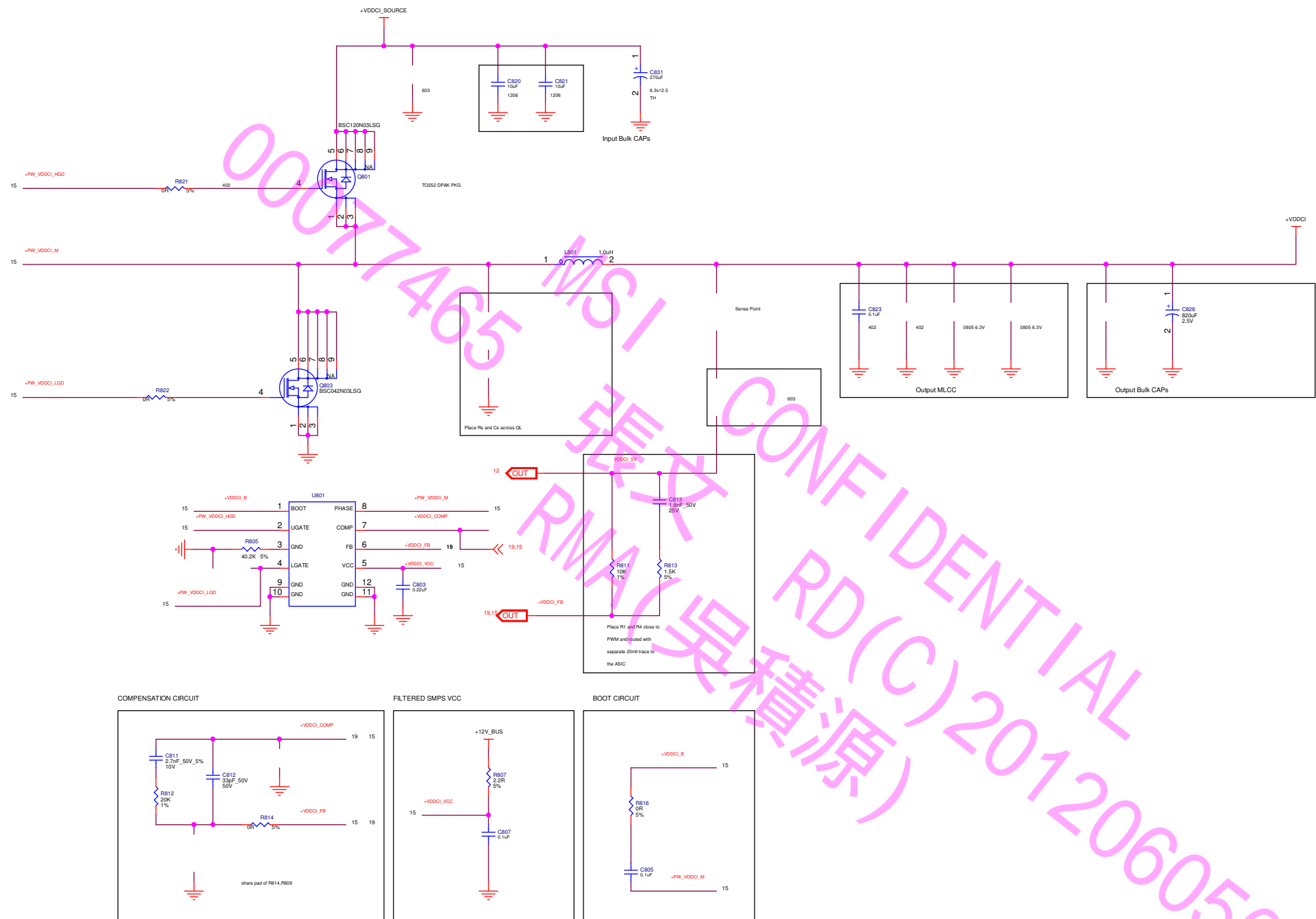
(13) PITCAIRN GROUND



<div> <div> AMD - GRAPHICS 1 COMMERCE VALLEY MARKHAM, ONTARIO, L3T 7X6 </div> <div>  </div> </div>		<div> CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. 2010 Advanced Micro Devices </div> <div> This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein. </div>	
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DOCUMENT NUMBER:	102-C40304-00		
NOTES:	NOTE		



(15) VDDCI



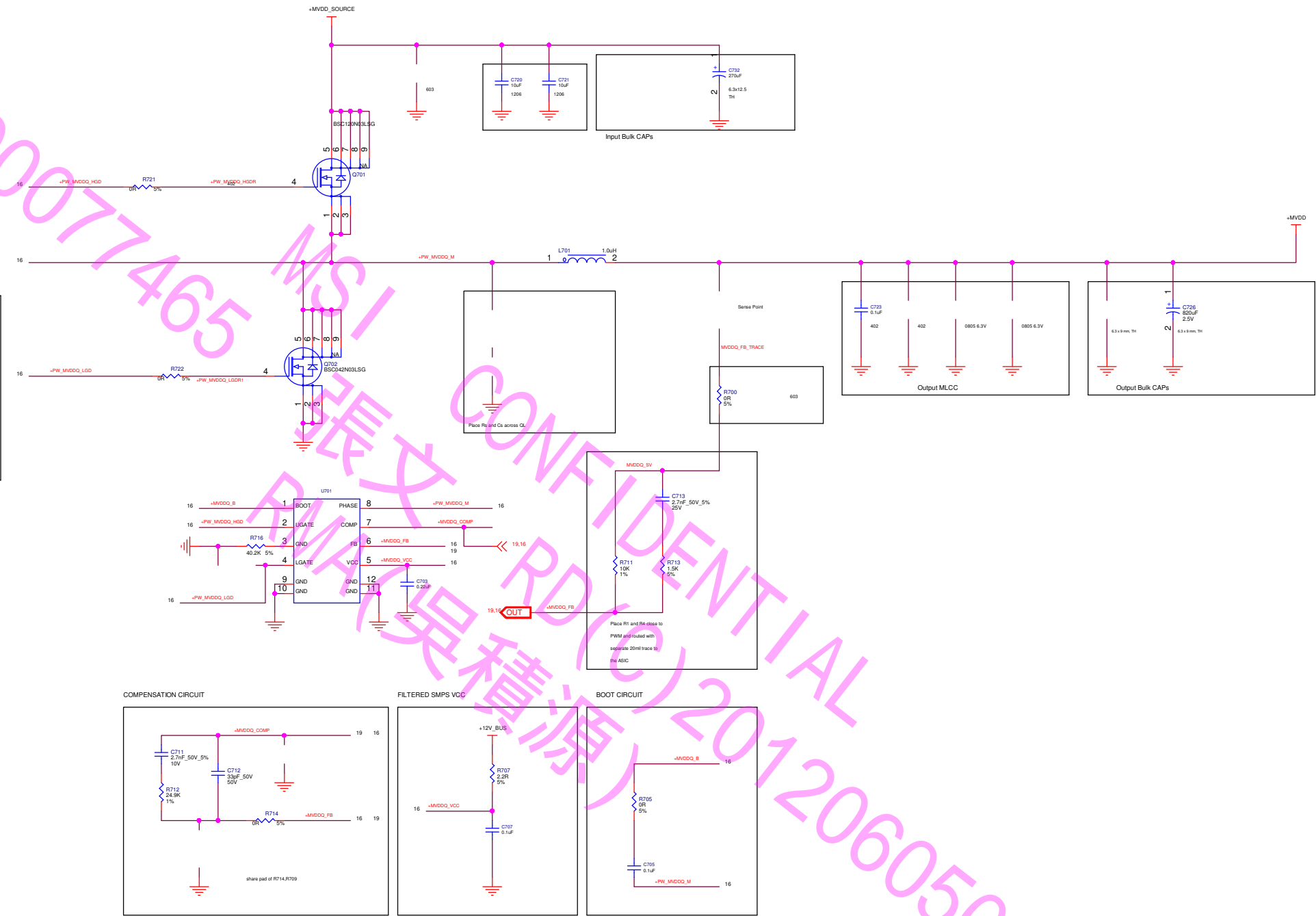
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SHEET: VDDCI		REV: 08	
SHEET NUMBER: Tue Dec 13 20:37:29 2011		OF 08	
DOCUMENT NUMBER: 15		23	
NOTES: NOTE		102-C40304-00	
		TITLE:	


Layout guideline

1-Position the controller (U703) such that L.Gate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW_MVDDQ_LSD and PW_MVDDQ_HSD) as short and as wide as possible to reduce the trace inductance.

2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows:
Vcc-bypass cap is C705, and Boost cap is C705.

3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 5. These are R710, R711, R712, C713 and R713, C711 and C712.

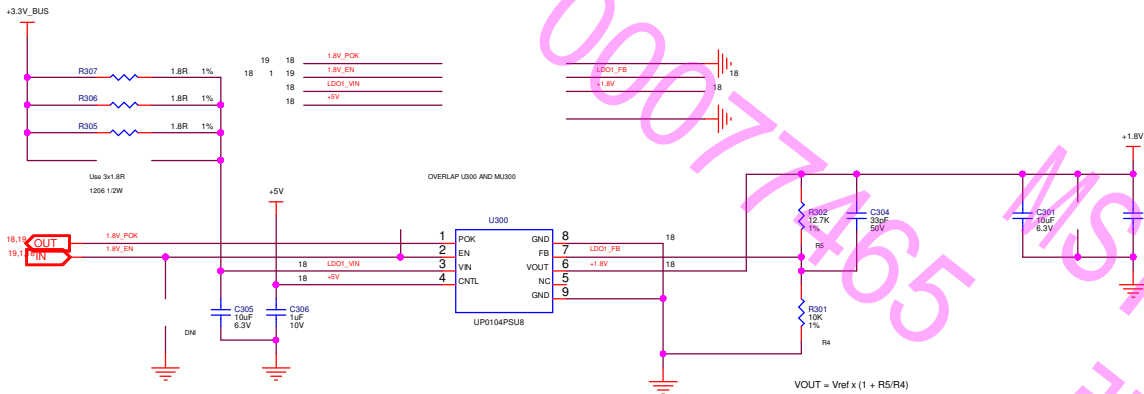


<div>AMD - GRAPHICS 1 COMMERCE VALLEY MARKHAM, ONTARIO, L3T 7X6</div> <div></div>		<div>CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. © 2010 Advanced Micro Devices</div> <div>This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.</div>	
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SHEET NUMBER: 16 OF 23		TITLE	
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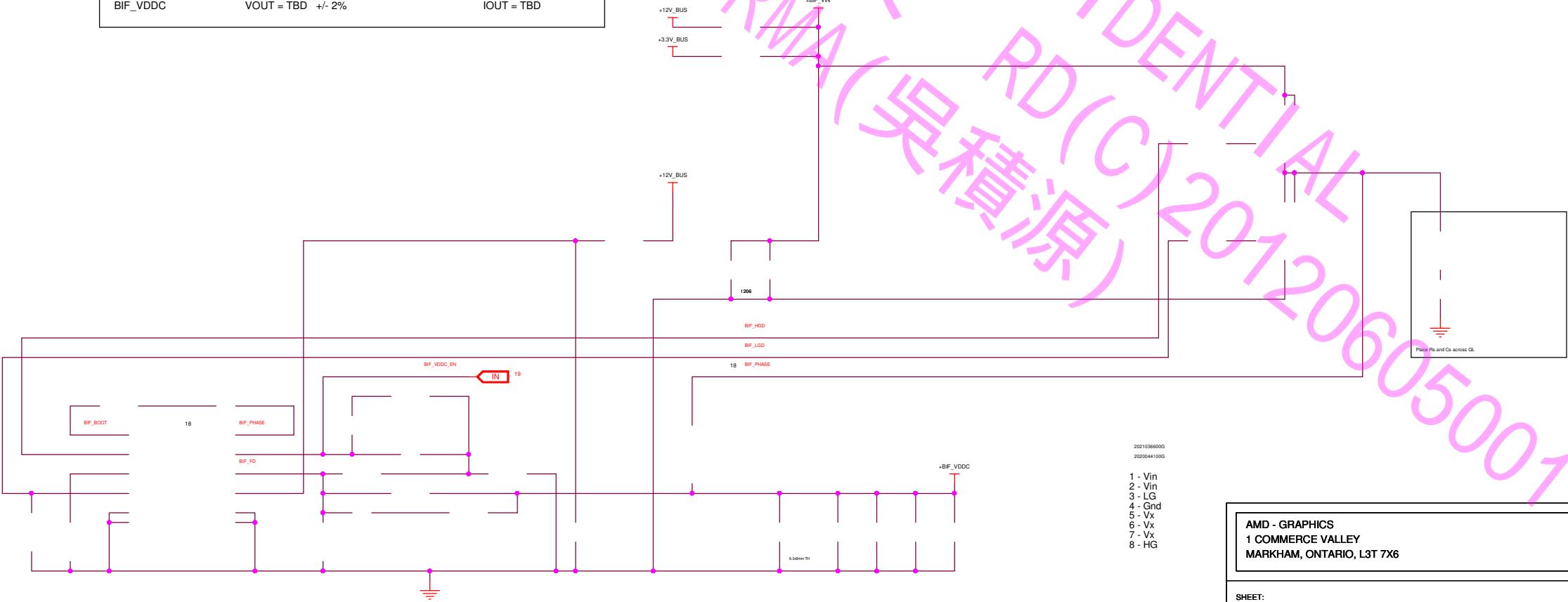
(17) 0.935V

(18) SMALL RAIL REGULATORS

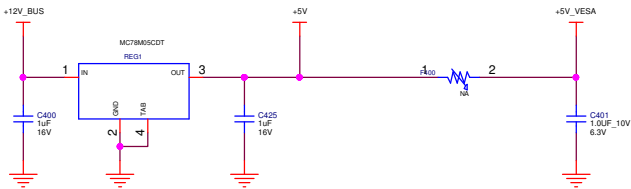
LDO #1: VIN = 3.0V TO 3.6V MAX VOUT = +1.8V +/- 2% IOU = 1.3A RMS MAX
PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING



BIF_VDDC VOUT = TBD +/- 2% IOU = TBD



REGULATOR FOR +5V RAILS
IOU MAX = 150mA



2010366003
20200411003

- 1 - Vin
- 2 - Vin
- 3 - LG
- 4 - Gnd
- 5 - Vx
- 6 - Vx
- 7 - Vx
- 8 - HG

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DATE: 2010.11.18 11:18 2011

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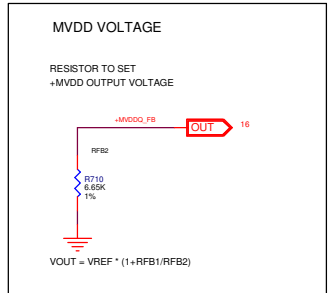
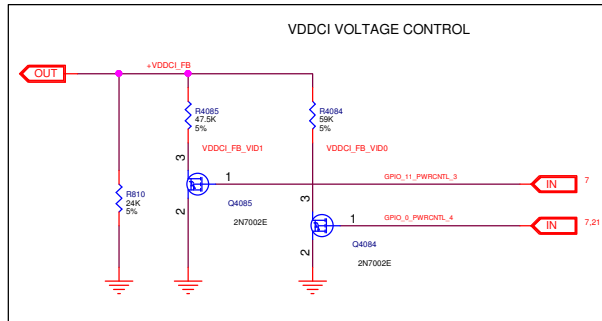
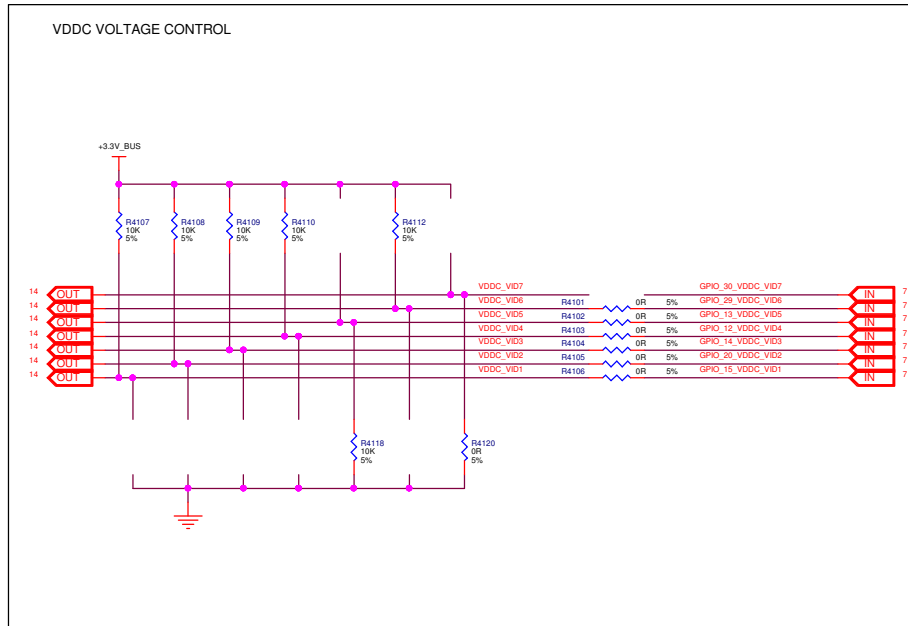
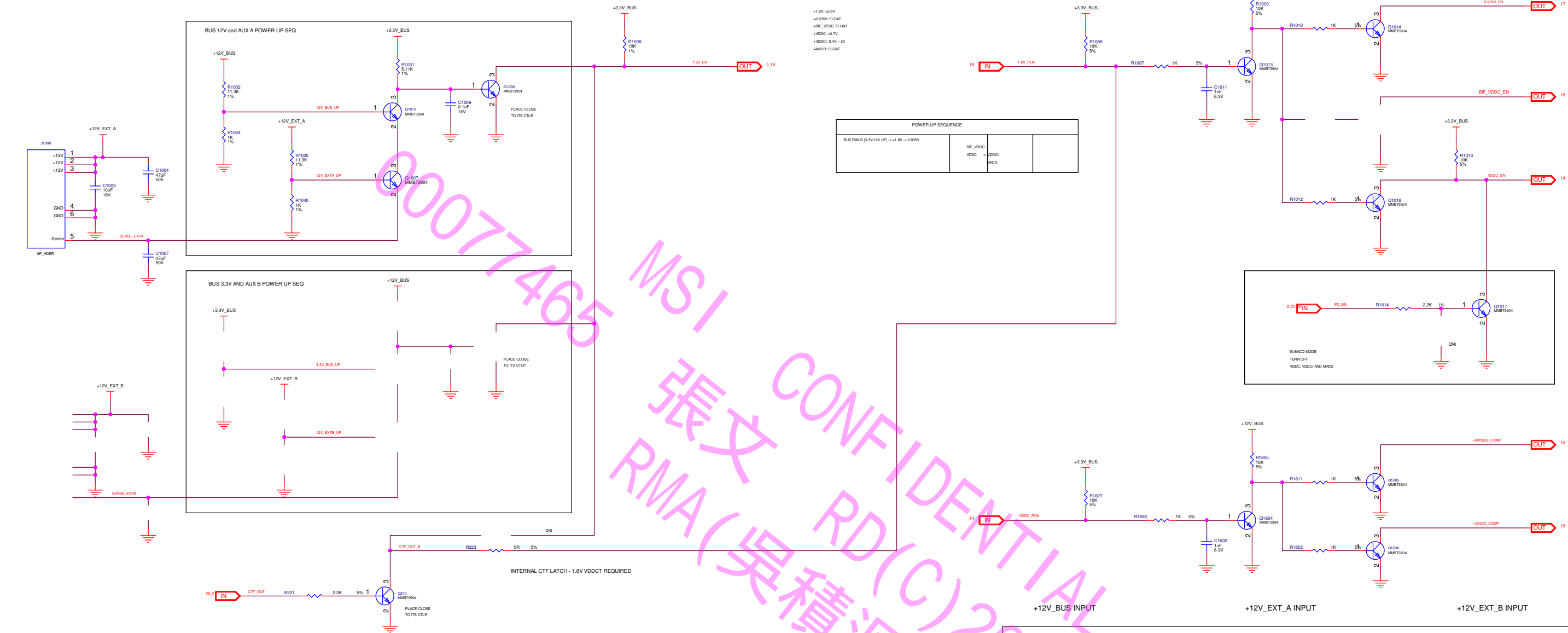
SHEET NUMBER: 18 OF 23

DOCUMENT NUMBER: 102-C40304-00

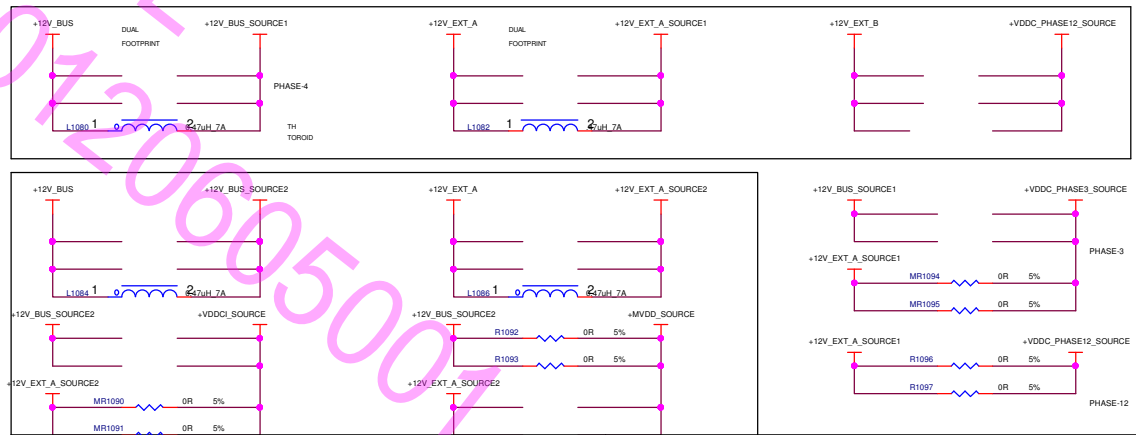
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(19) POWER MANAGEMENT

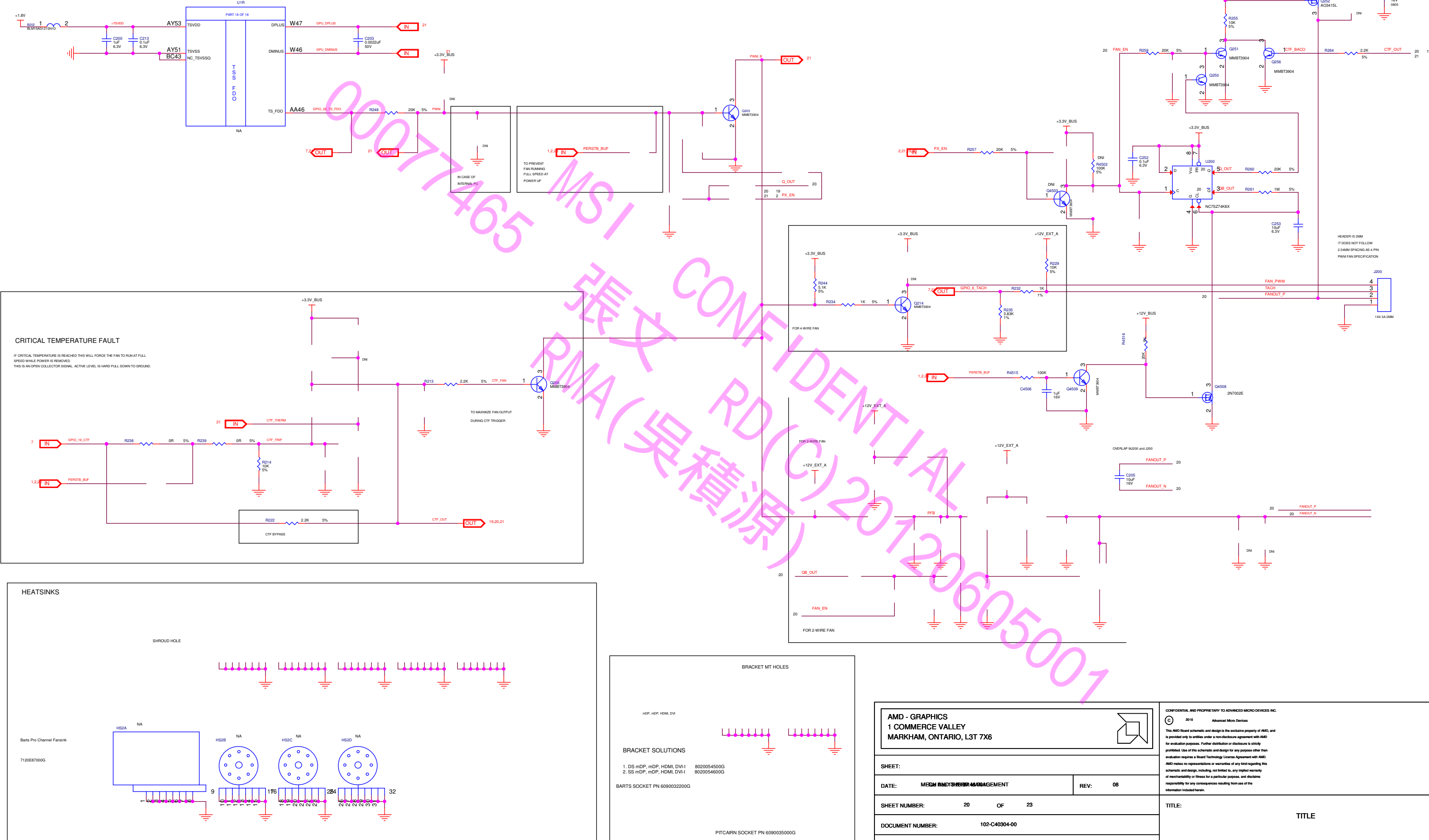


OPTIONAL VR_HOT FROM UP6213

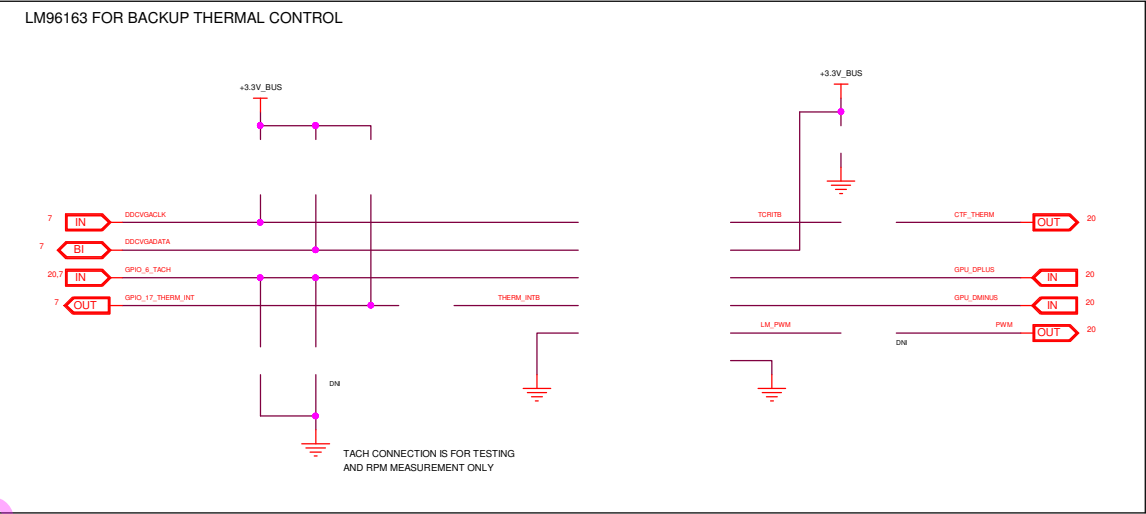
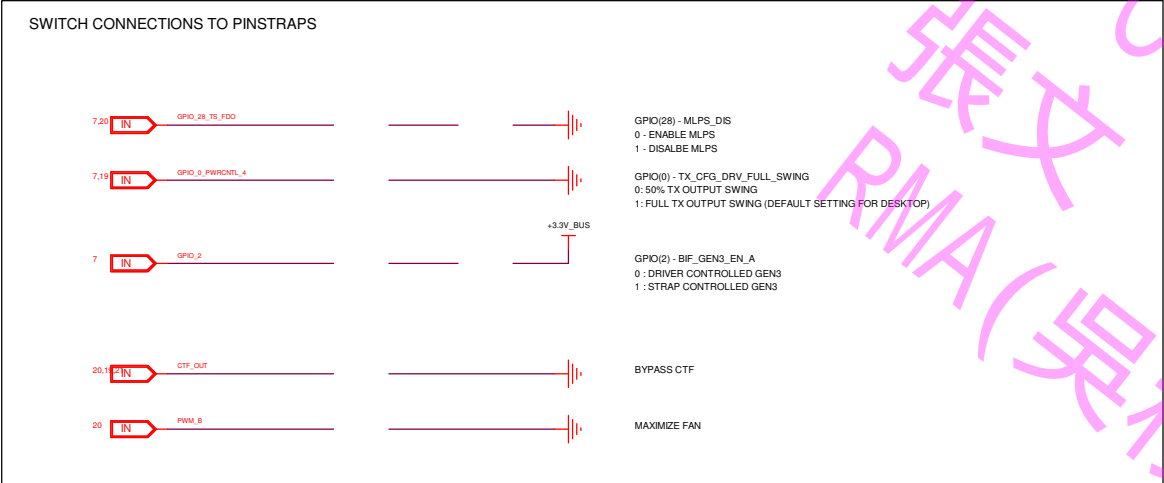
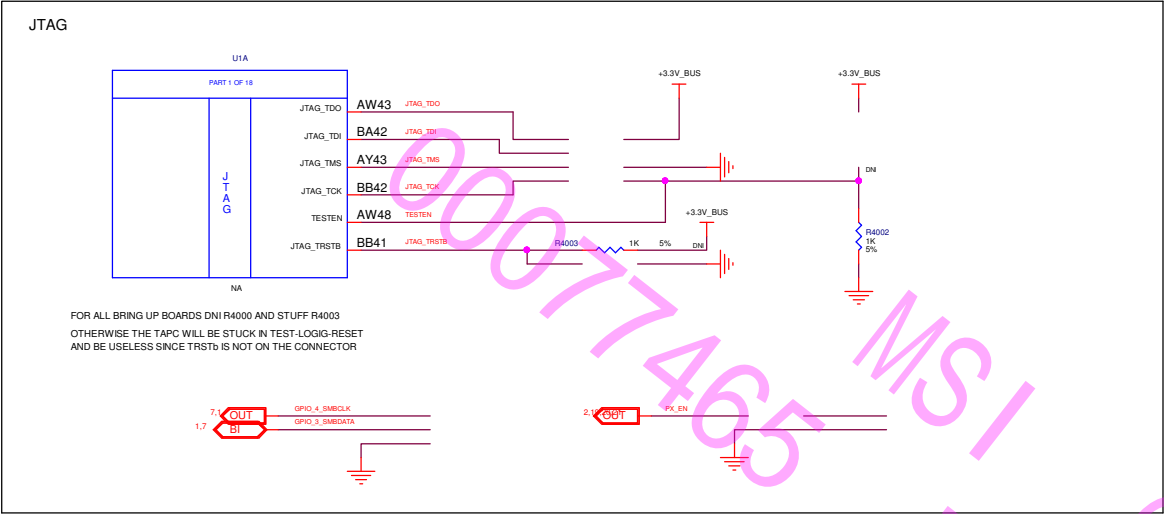


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SHEET: 19 OF 23		
DATE: 2013-07-20 13:37:42 2011	REV: 08	
DOCUMENT NUMBER: 102-C40304-00		
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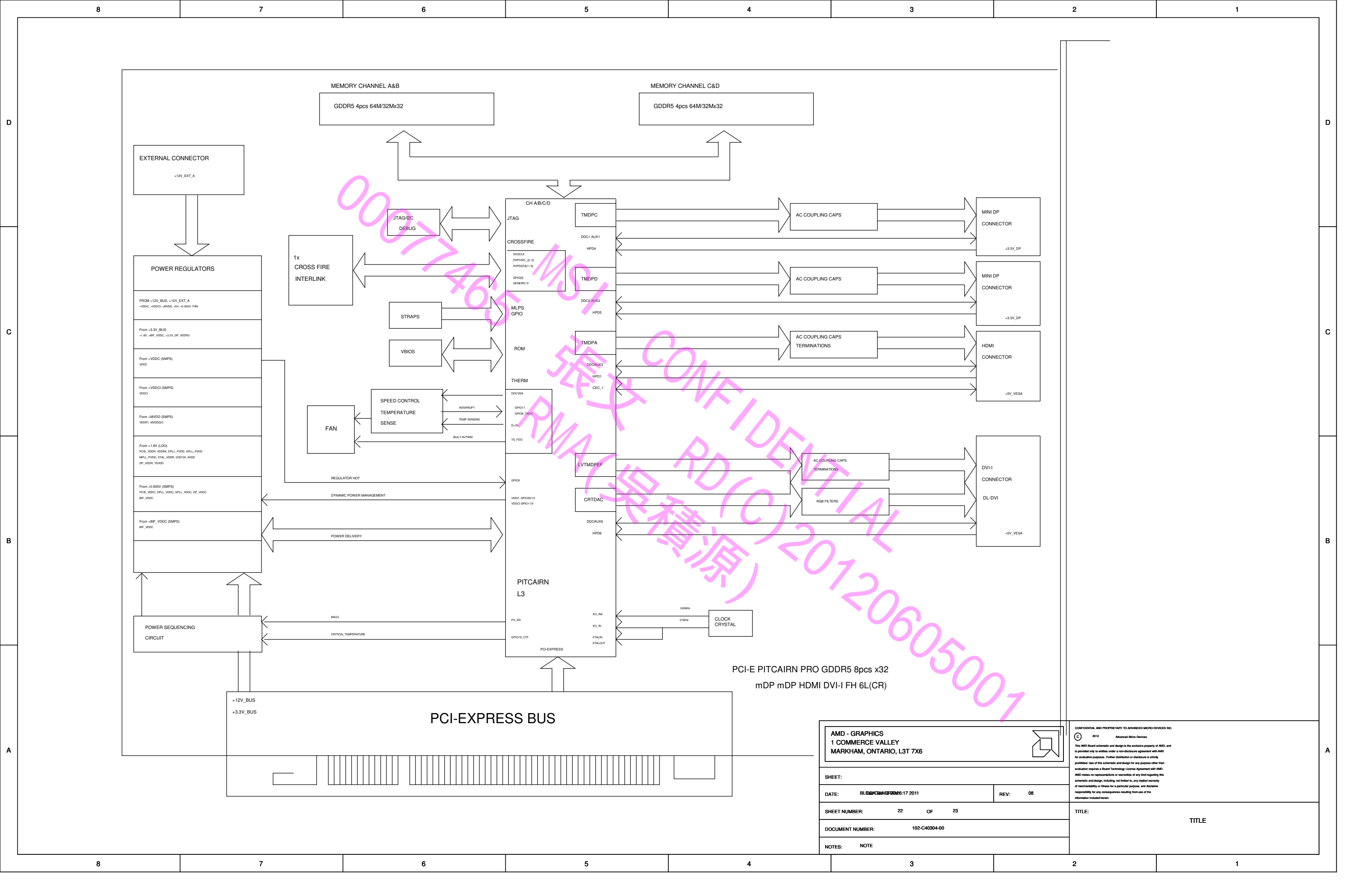
(20) MECHANICAL AND THERMAL MANAGEMENT



(21) DEBUG CIRCUITS




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SHEET:		DATE: 06/06/2011 13:20:37:49 2011		REV: 08	
SHEET NUMBER: 21 OF 23		DOCUMENT NUMBER: 102-C40304-00		TITLE:	
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SHEET:	
DATE: 2011-07-17	REV: 08
SHEET NUMBER: 22 OF 23	
DOCUMENT NUMBER: 102-C40304-00	
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AMD				TITLE:		DOCUMENT NUMBER: 102-C40304-00		DATE: Tue Dec 13 20:26:17 2011		SHEET NUMBER: 23 OF 23		REV: 08			
REVISION HISTORY				ENGINEER: XXX		NOTES: NOTE		<div>CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.</div>				AMD - GRAPHICS 1 COMMERCE VALLEY MARKHAM, ONTARIO, L3T 7X6			
SCH Rev		PCB Rev		Date		REVISION DESCRIPTION									
0		00A		01/07/2010		PITCARN PRO GR DESIGN									
0		00B		2011/05/11		Update Baco delay circuitry for 2 pin fan									

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