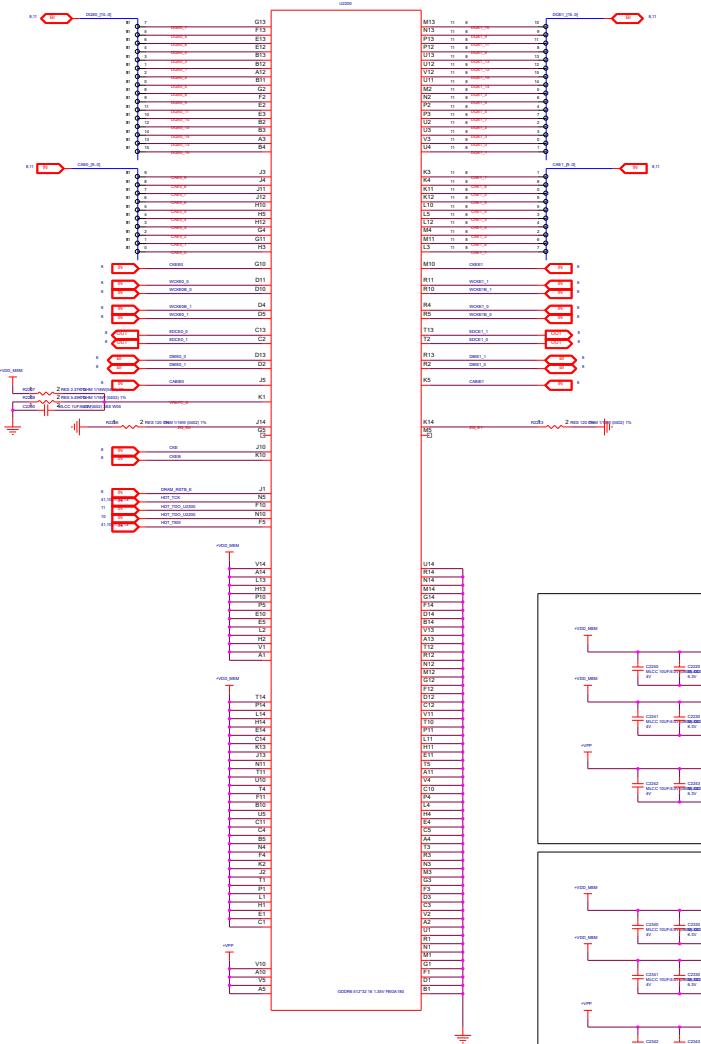
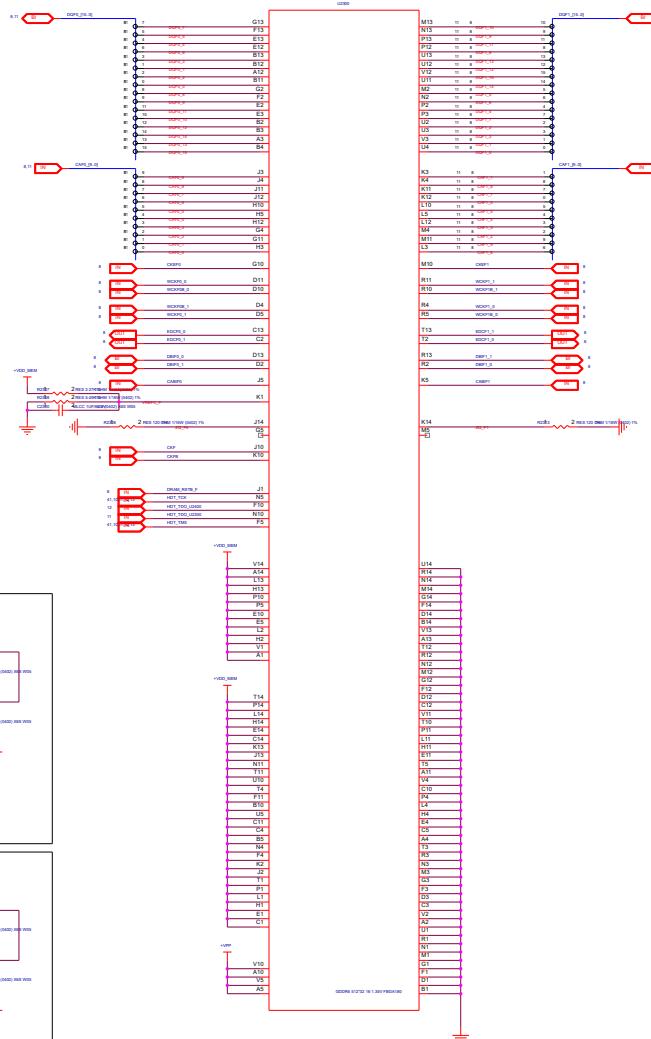


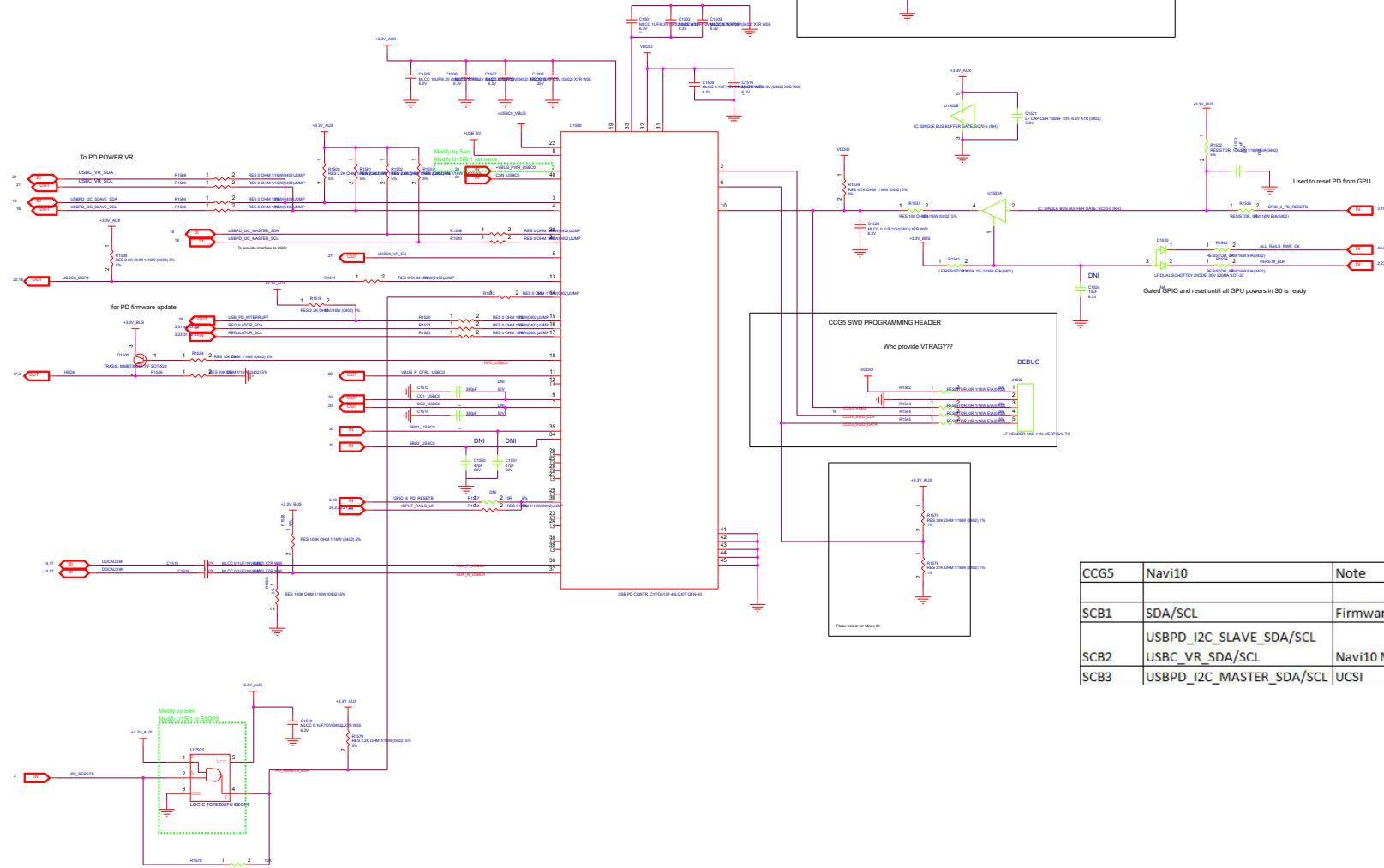
ASIC CH0 → MEM CHA  
ASIC CH1 → MEM CHB



ASIC CH0 -> MEM C  
ASIC CH1 -> MEM C

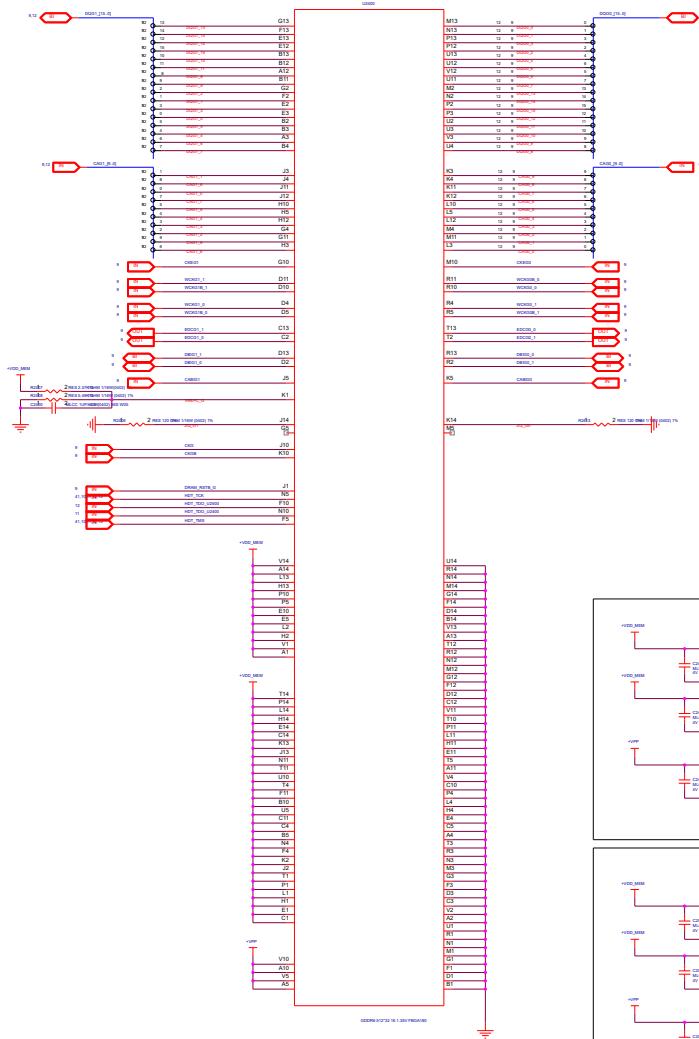


for GPU DP/USB COMPHY

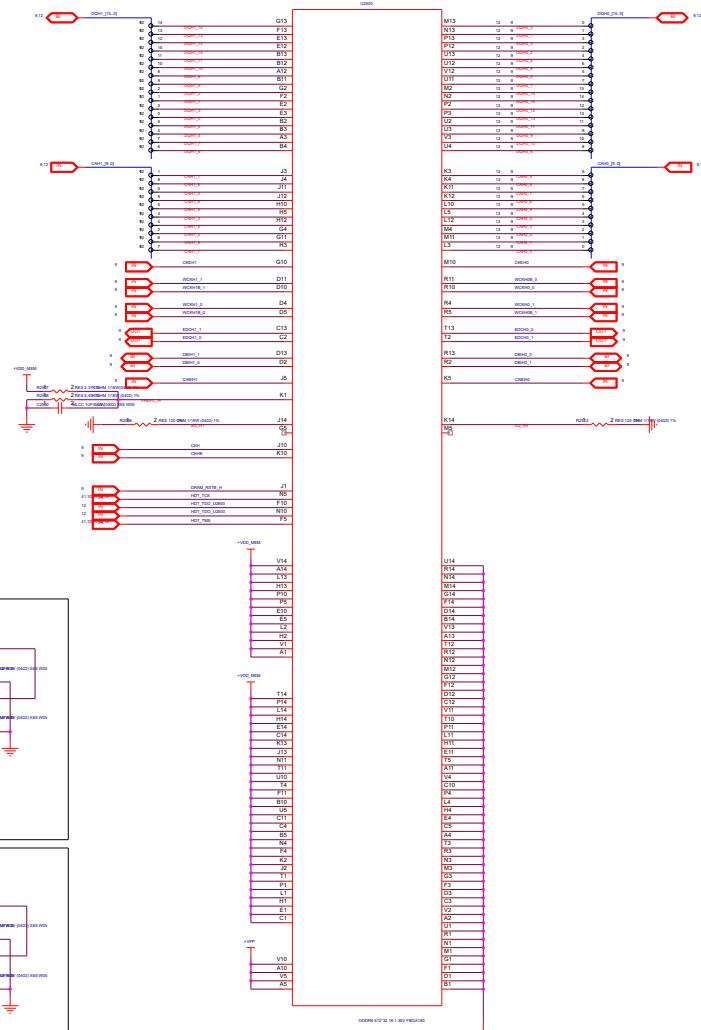


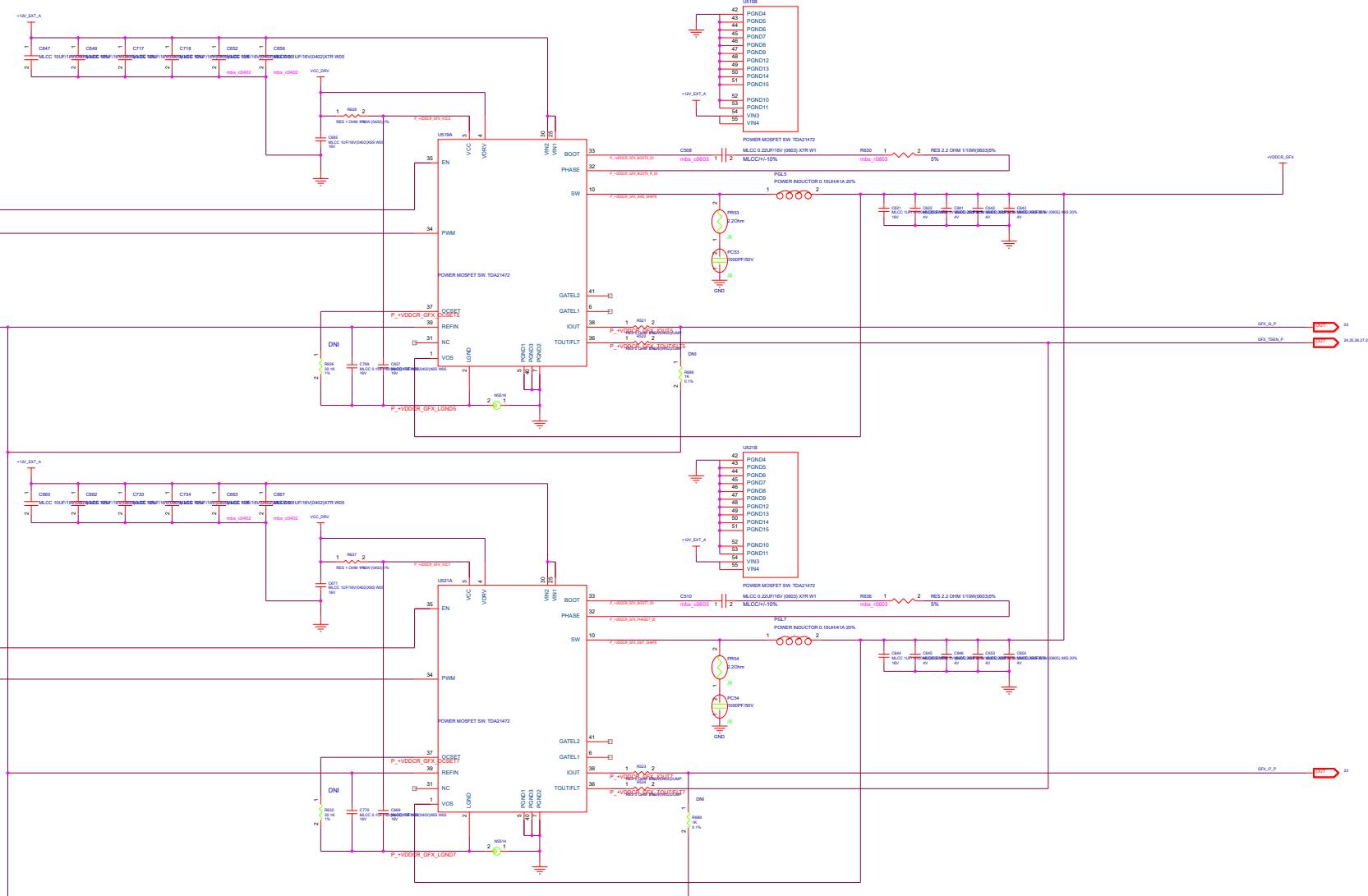
CC5	Navi10	Note
SCB1	SDA/SCL	Firmware update/SMU
SCB2	USBPD_I2C_SLAVE_SDA/SCL	Navi10 MUX/PD_Regulator/re-driver
SCB3	USBPD_I2C_MASTER_SDA/SCL	UCSI

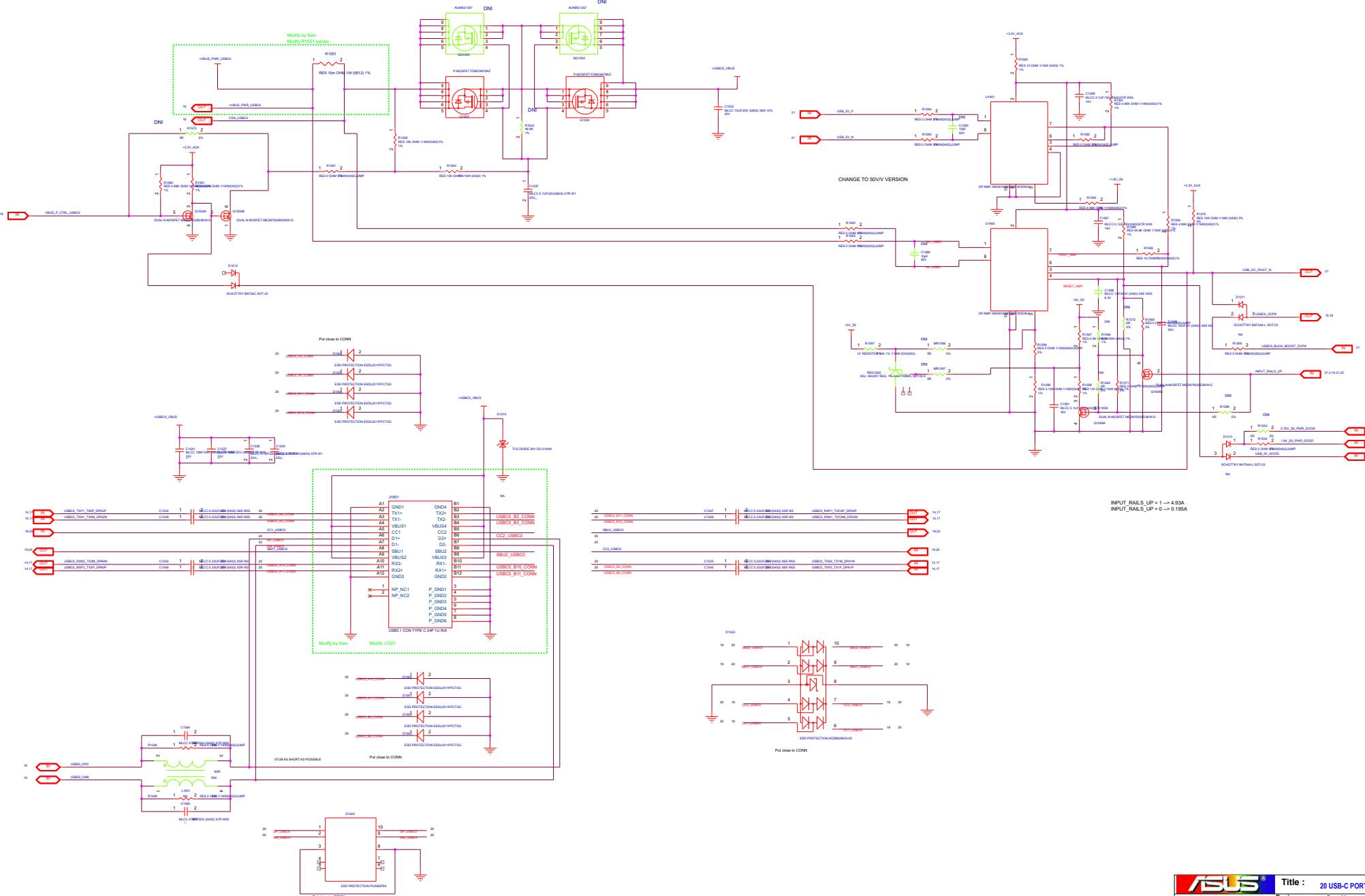
ASIC CH0 -> MEM CHB  
ASIC CH1 -> MEM CHA



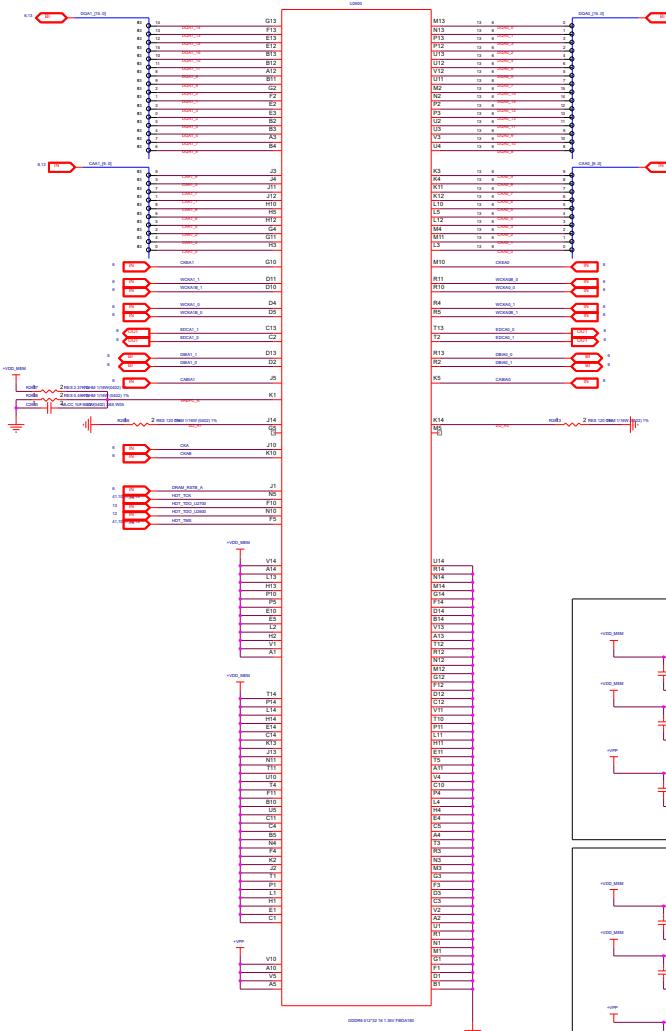
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ASIC CH1 -> MEM CHA



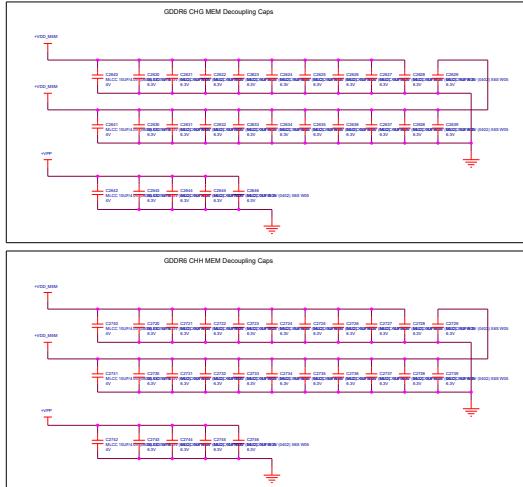
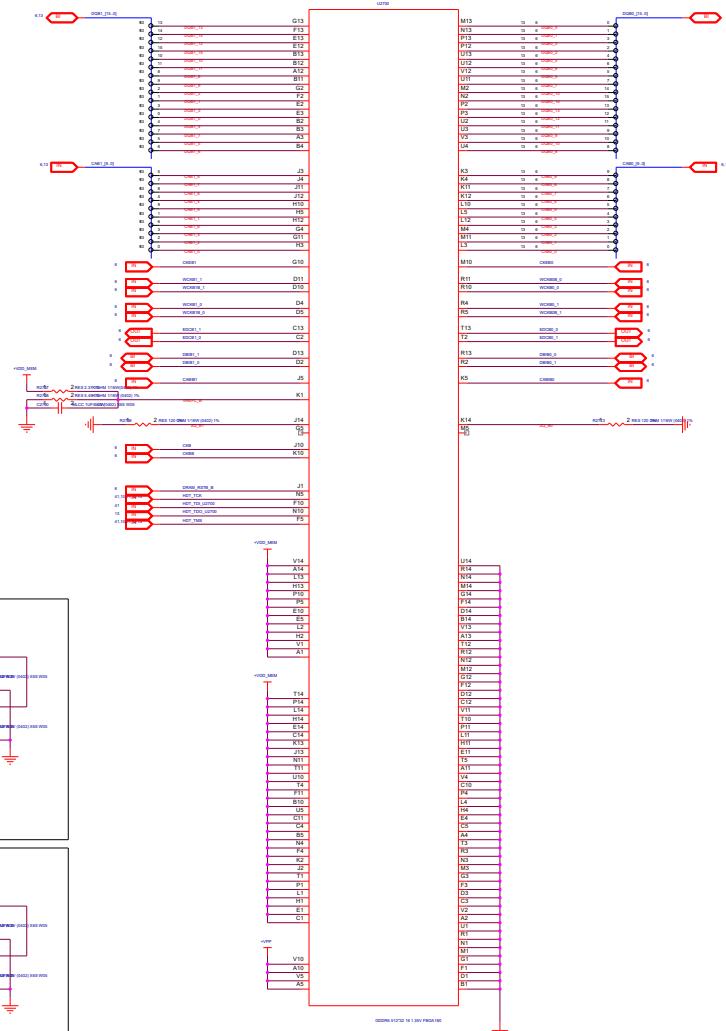


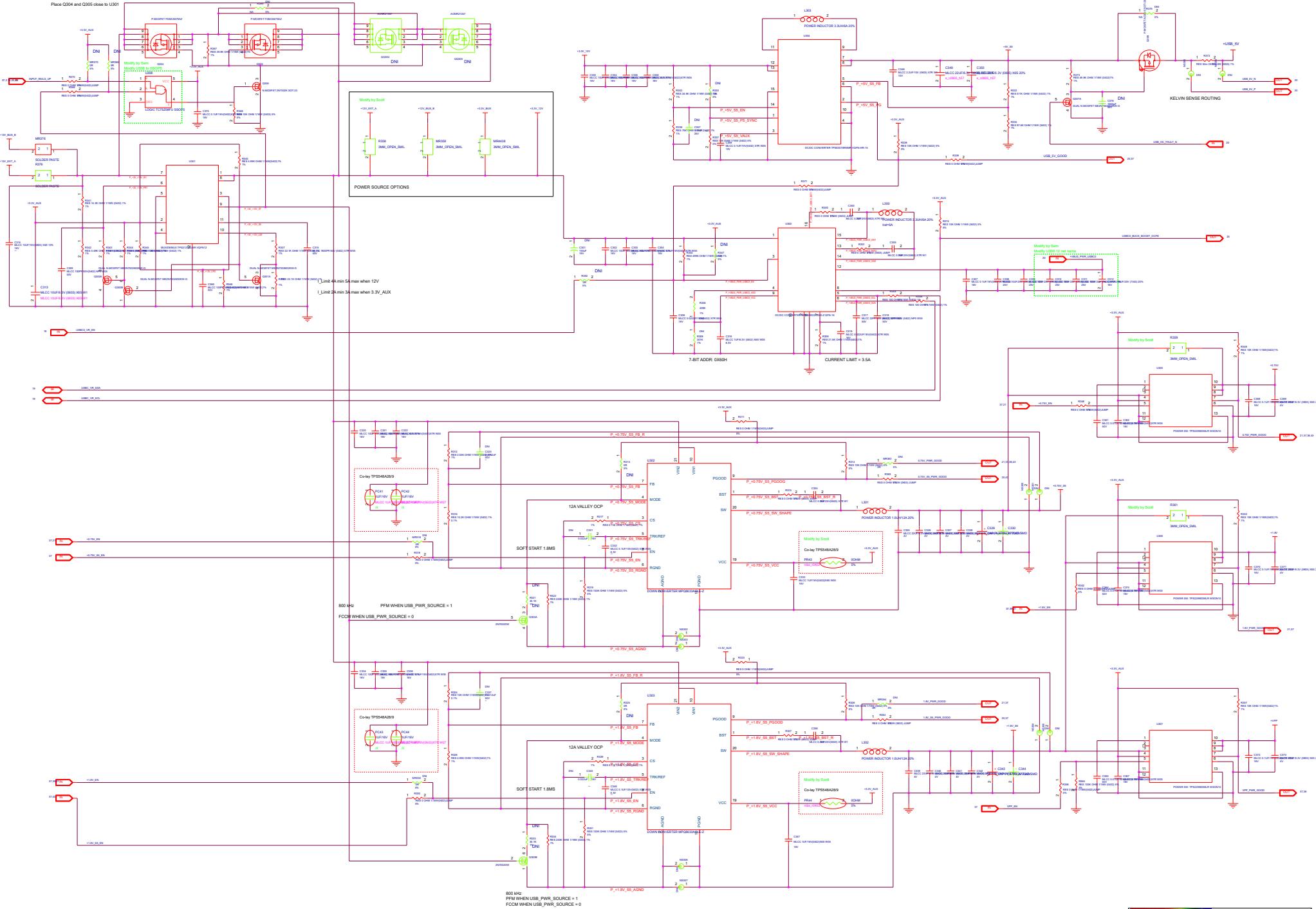


ASIC CH0 → MEM CHB  
ASIC CH1 → MEM CHA

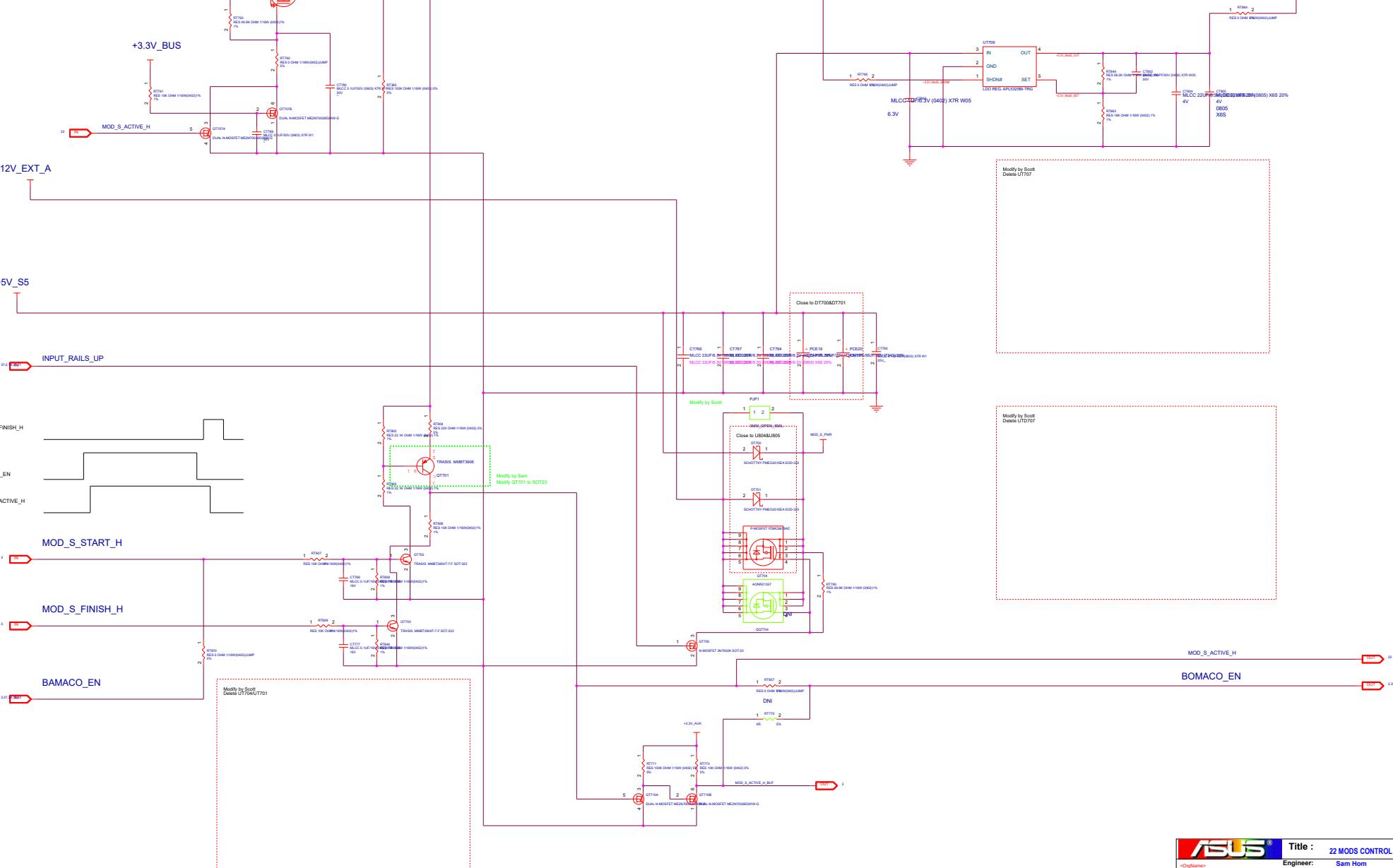


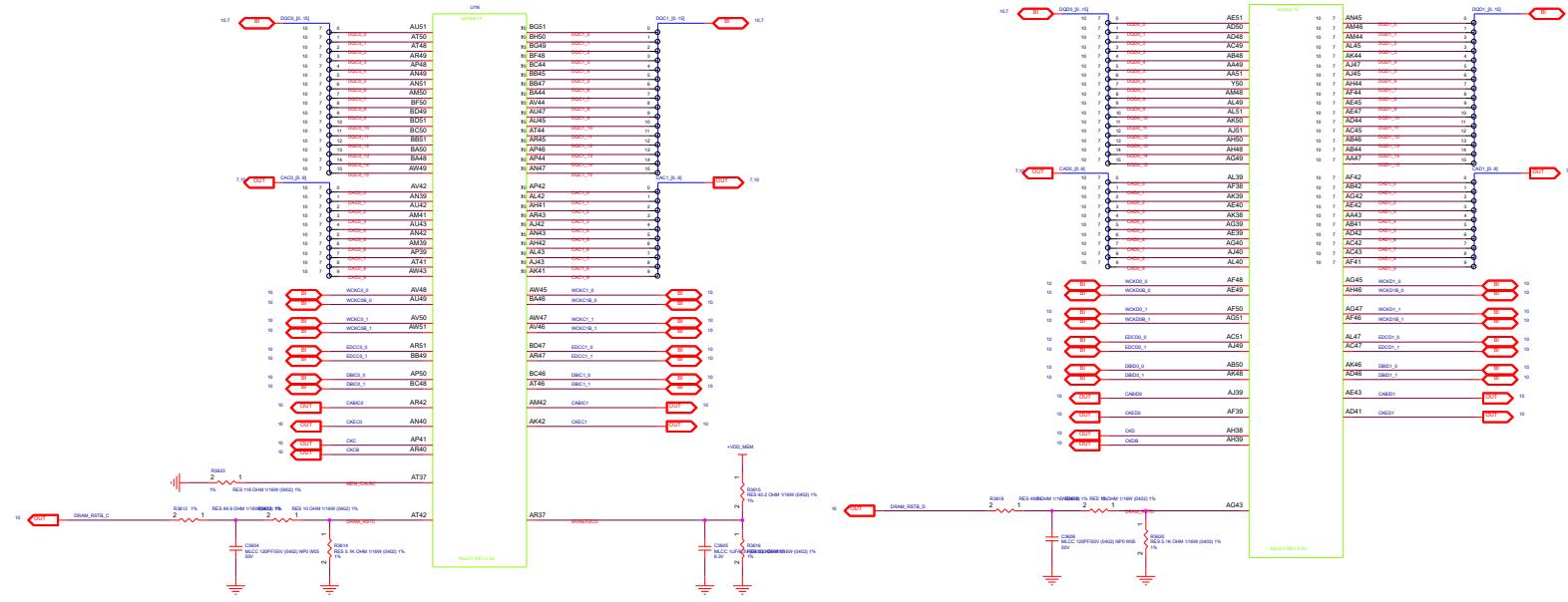
ASIC CH0 → MEM CHB  
ASIC CH1 → MEM CHA

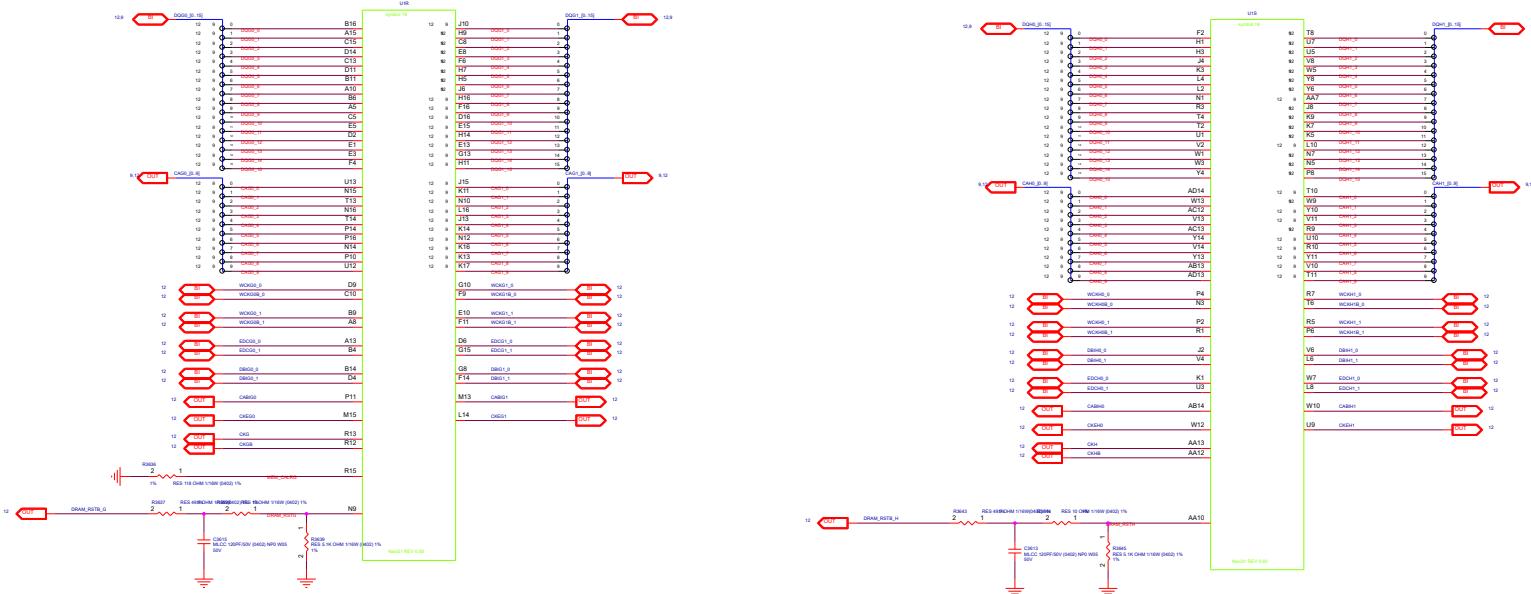




+3.3V\_AUX

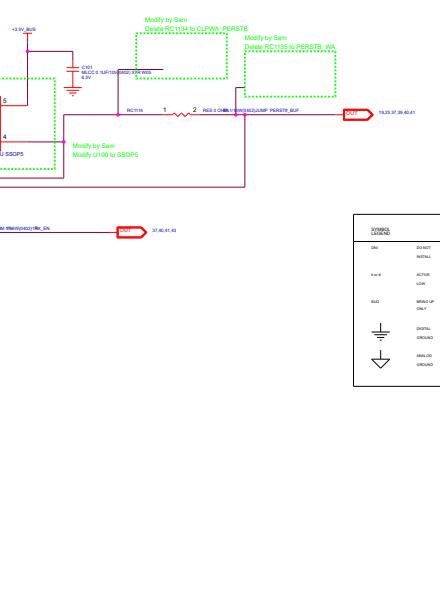
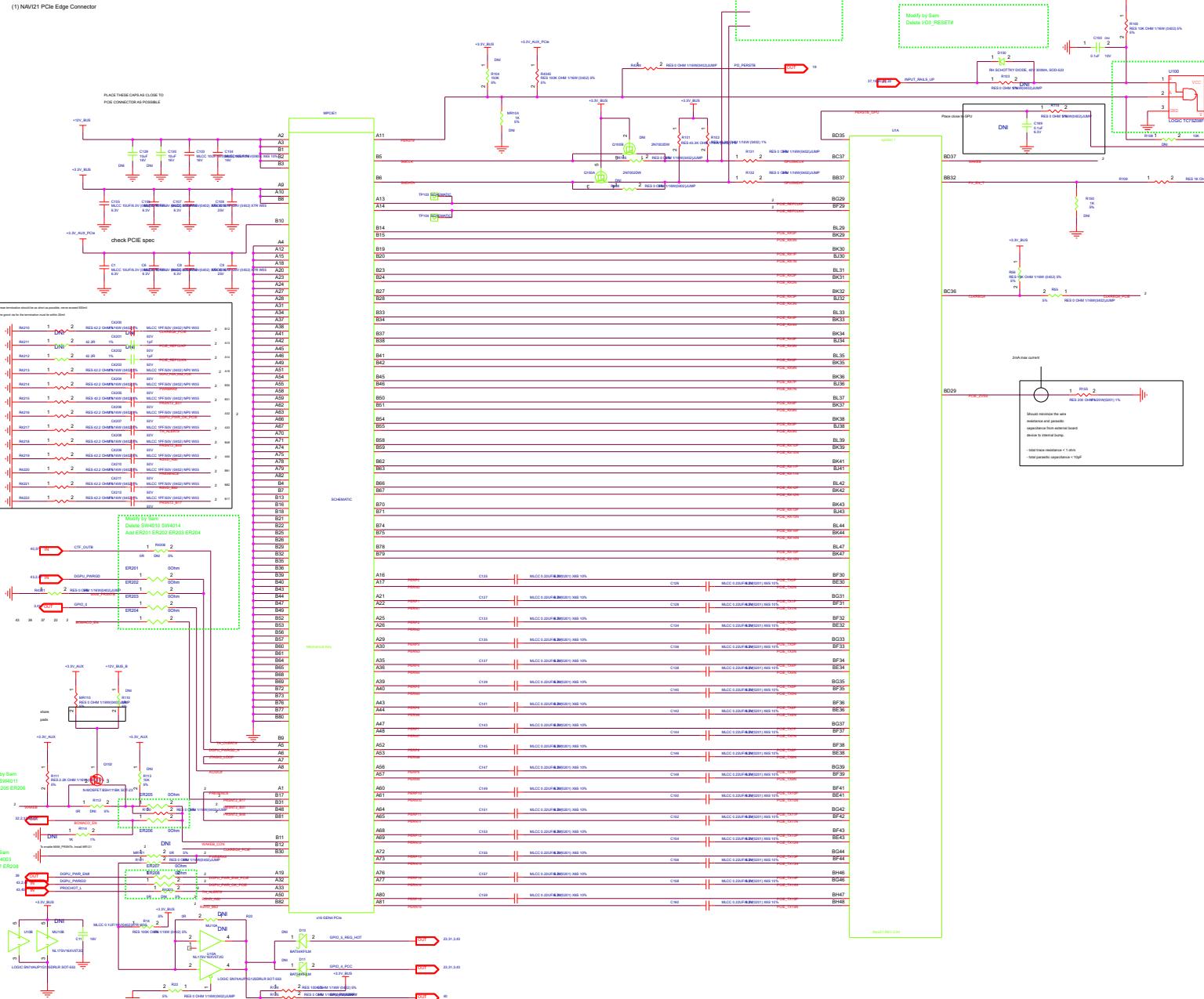




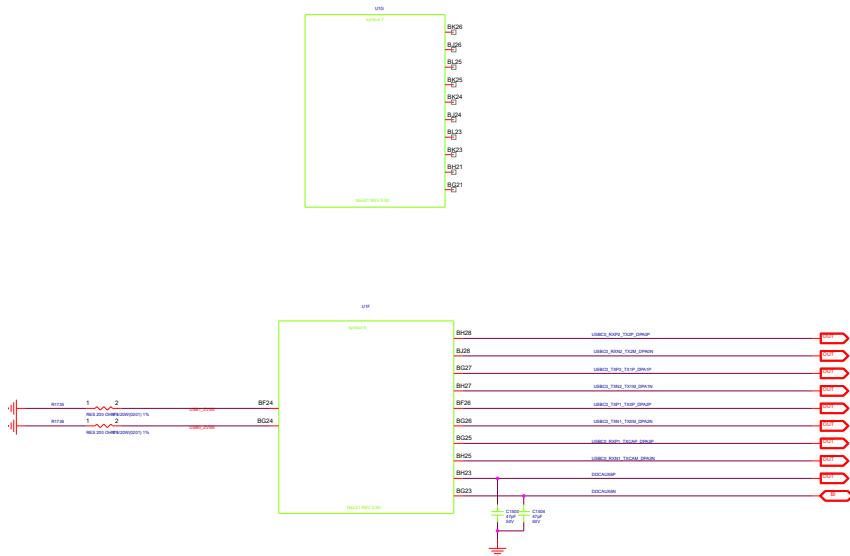


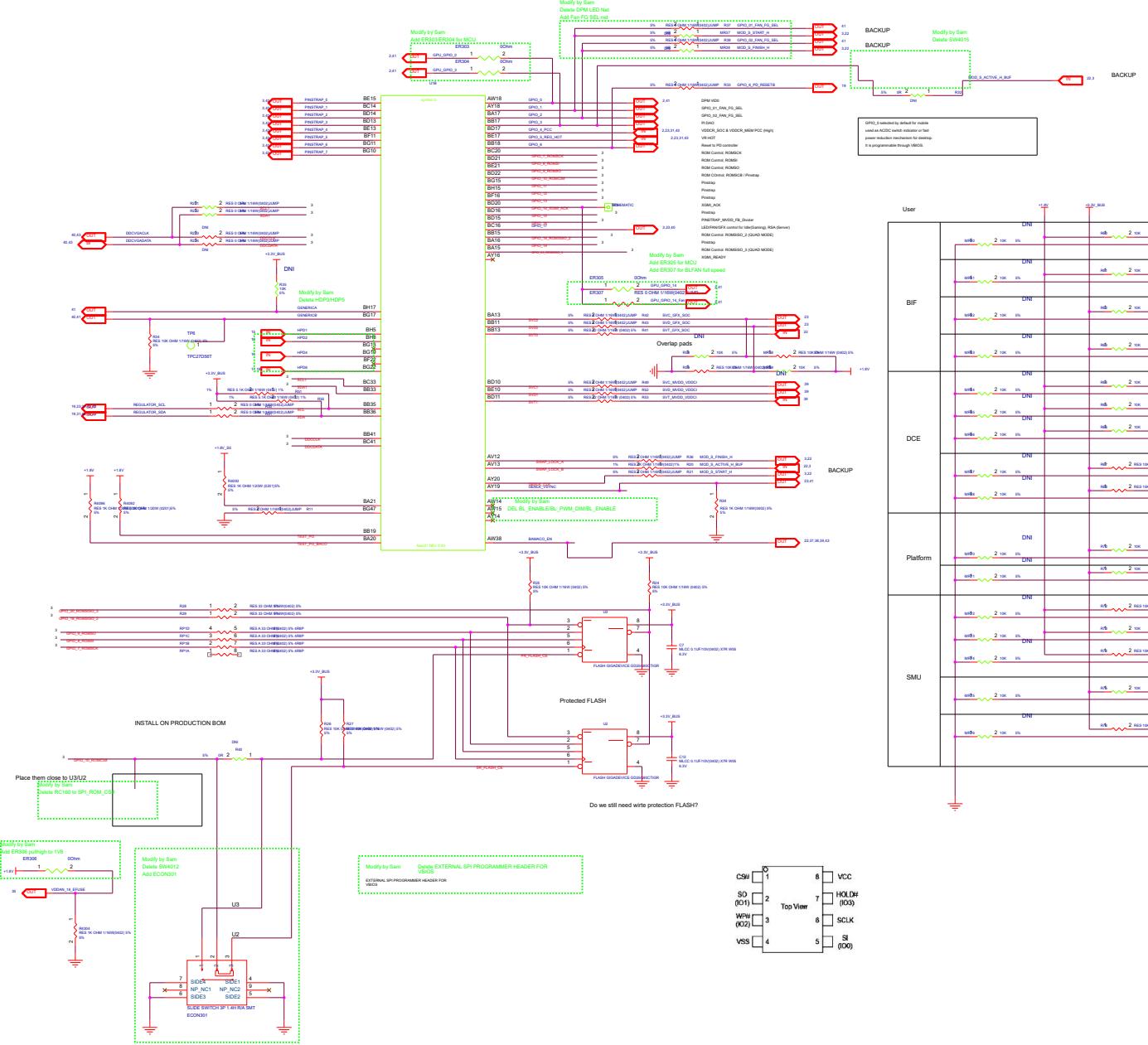
# TABLE OF CONTENTS

SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	GFX PHASES 8&9
2	NAVI 21 - PCIe Interface	27	GFX PHASES 11
3	NAVI 21 - GPIOs	28	GFX PHASES 5&7
4	NAVI 21 XTAL	29	GFX PHASES 3&10
5	XGMI	30	SOC PHASE 1&2
6	NAVI 21 MEM CH AB	31	VDD_MEM & VDDCI CONTROLLER
7	NAVI 21 MEM CH CD	32	VDD_MEM PHASES 1&2
8	NAVI 21 MEM CH EF	33	VDDCI_MEM PHASE 1
9	NAVI 21 MEM CH GH	34	NAVI 21 DECAPS
10	GDDR6 MEM CH CD	35	NAVI 21 POWER
11	GDDR6 MEM CH EF	36	NAVI 21_POWER and GND
12	GDDR6 MEM CH GH	37	POWER_MANAGEMENT
13	GDDR6 MEM CH AB	38	ClampWA
14	NAV121 TMDDPA - USB-C	39	SVI2 & BxMACO
15	NAV121 TMDDPF - HDMI	40	THERMAL
16	NAV121 TMDDPC&E - DP	41	DPM_Status_LED & GDDR6_JTAG
17	NAV121 TMDDPA	42	Pi Debug
18	NAV121 USB	43	DEBUG
19	PD Controller	44	History
20	USB-C PORT 1		
21	USB_5V_1.8V_0.75V		
22	MODS CONTROL & POWER		
23	GFX & SOC CONTROLLER		
24	GFX PHASES 1&2		
25	GFX PHASES 4&6		

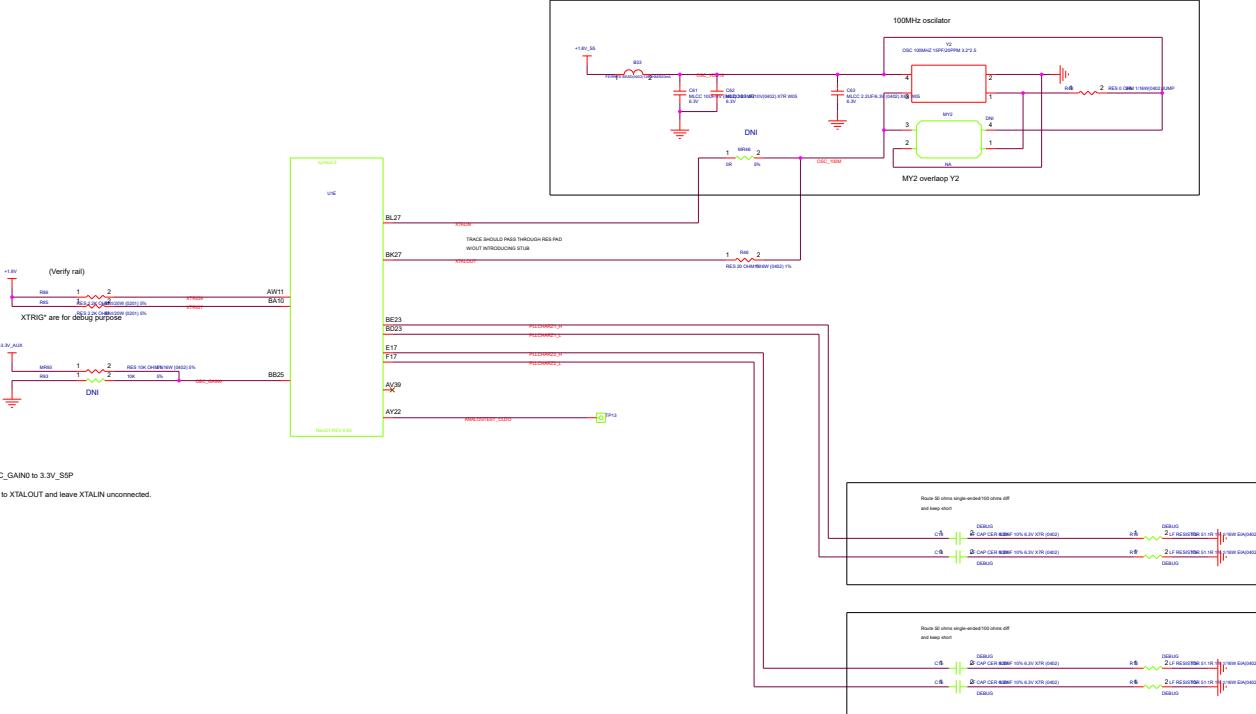


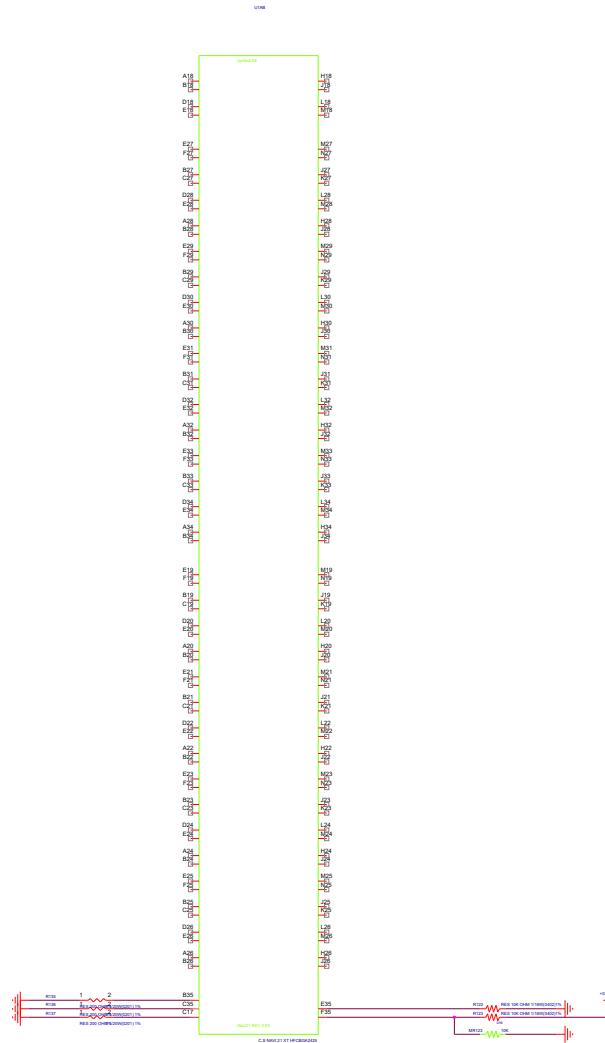
SYMBOL LEGEND	
DM	DO NOT INSTALL
IC or IC	ACTIVE LOW
BUZ	BURST UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

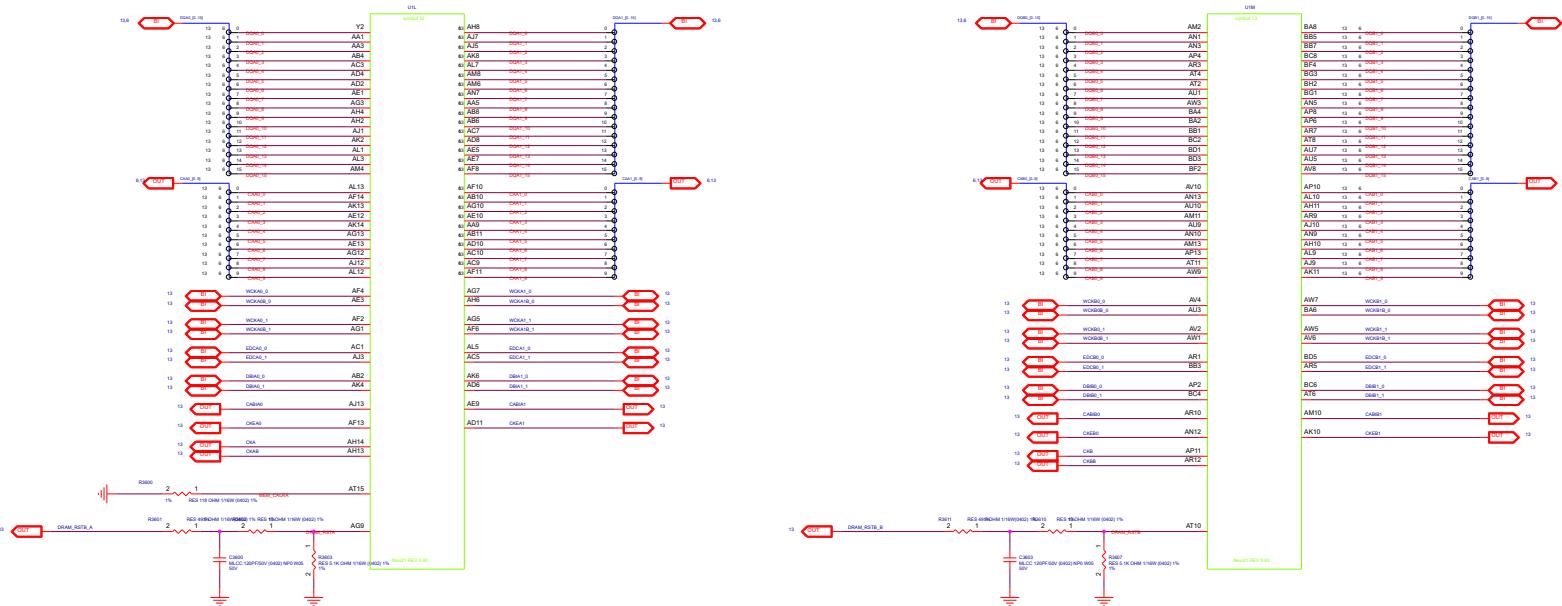


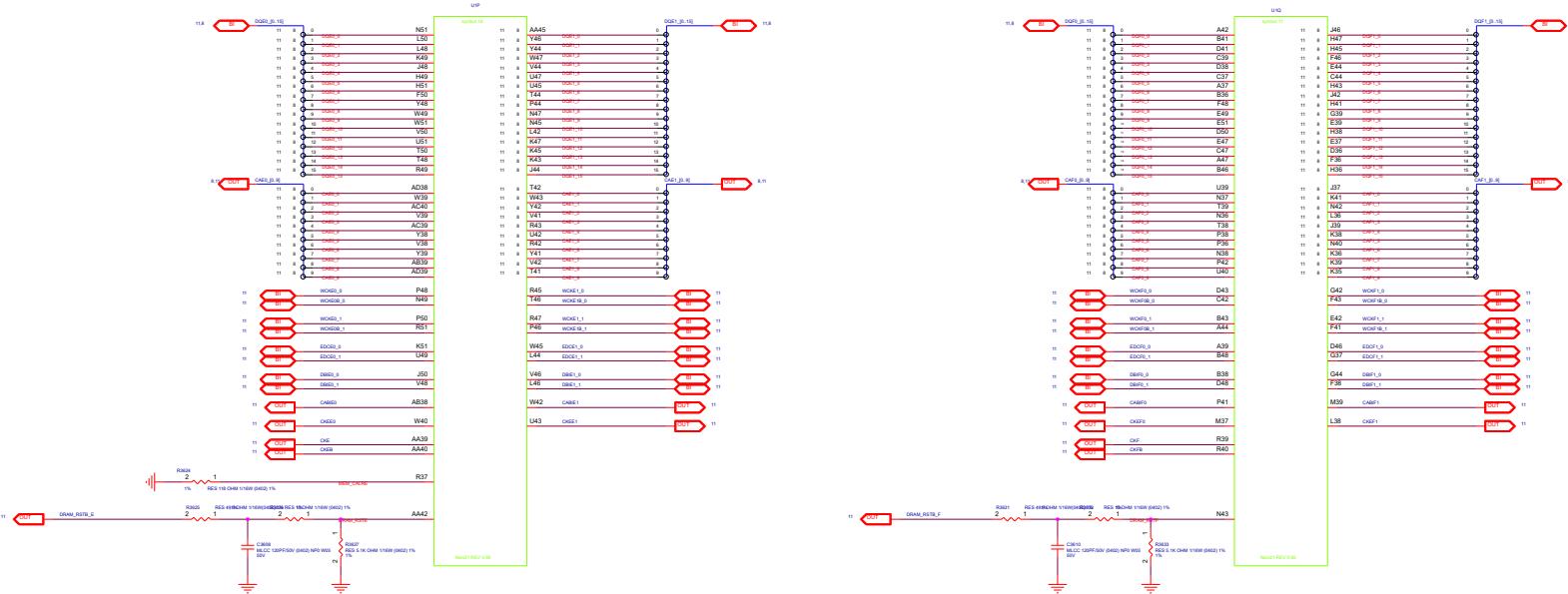


User		DNI	Note: Internal PULLUP at GPIO pad is strong in 14nm design spec	Internal Default Value	Definition
BiF		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
DCE		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
Platform		wk/s 2 tce sh DNI	sb 2 tce sh	3 40	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 40	TBD
		wk/s 2 tce sh DNI	sb 2 tce sh	3 40	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 40	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 40	0
SMU		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	1
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	1
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	0
		wk/s 2 tce sh DNI	sb 2 tce sh	3 43	1

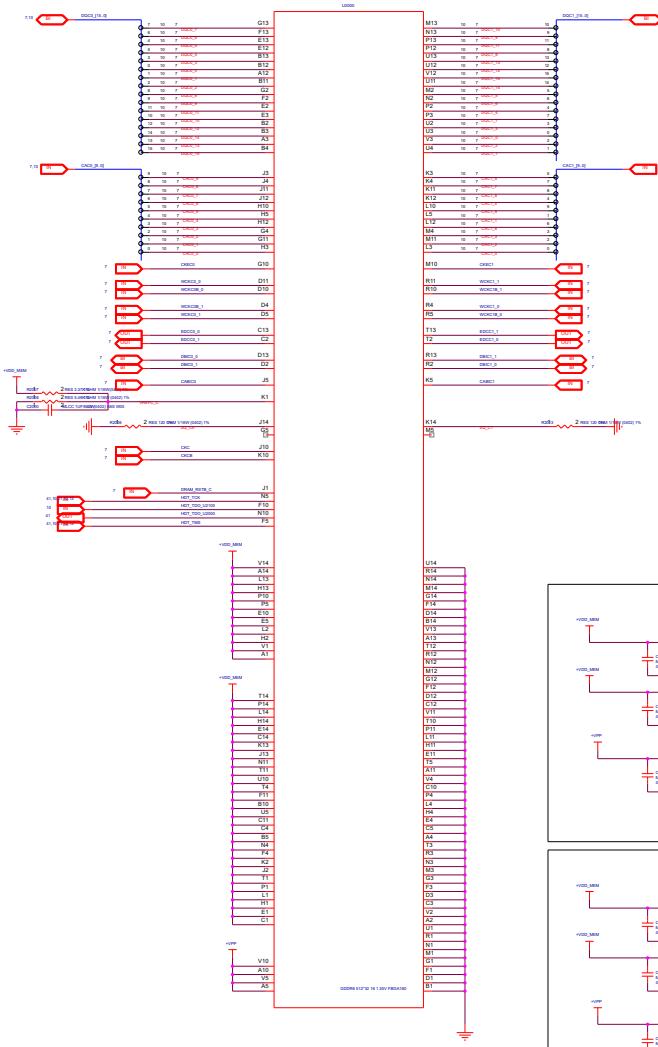




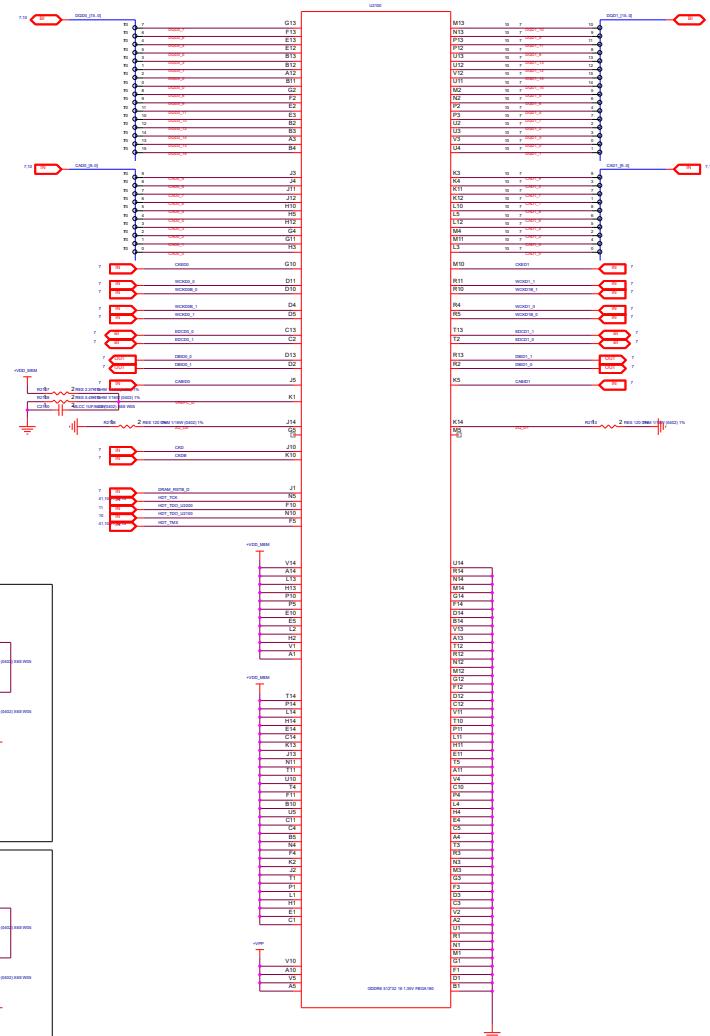


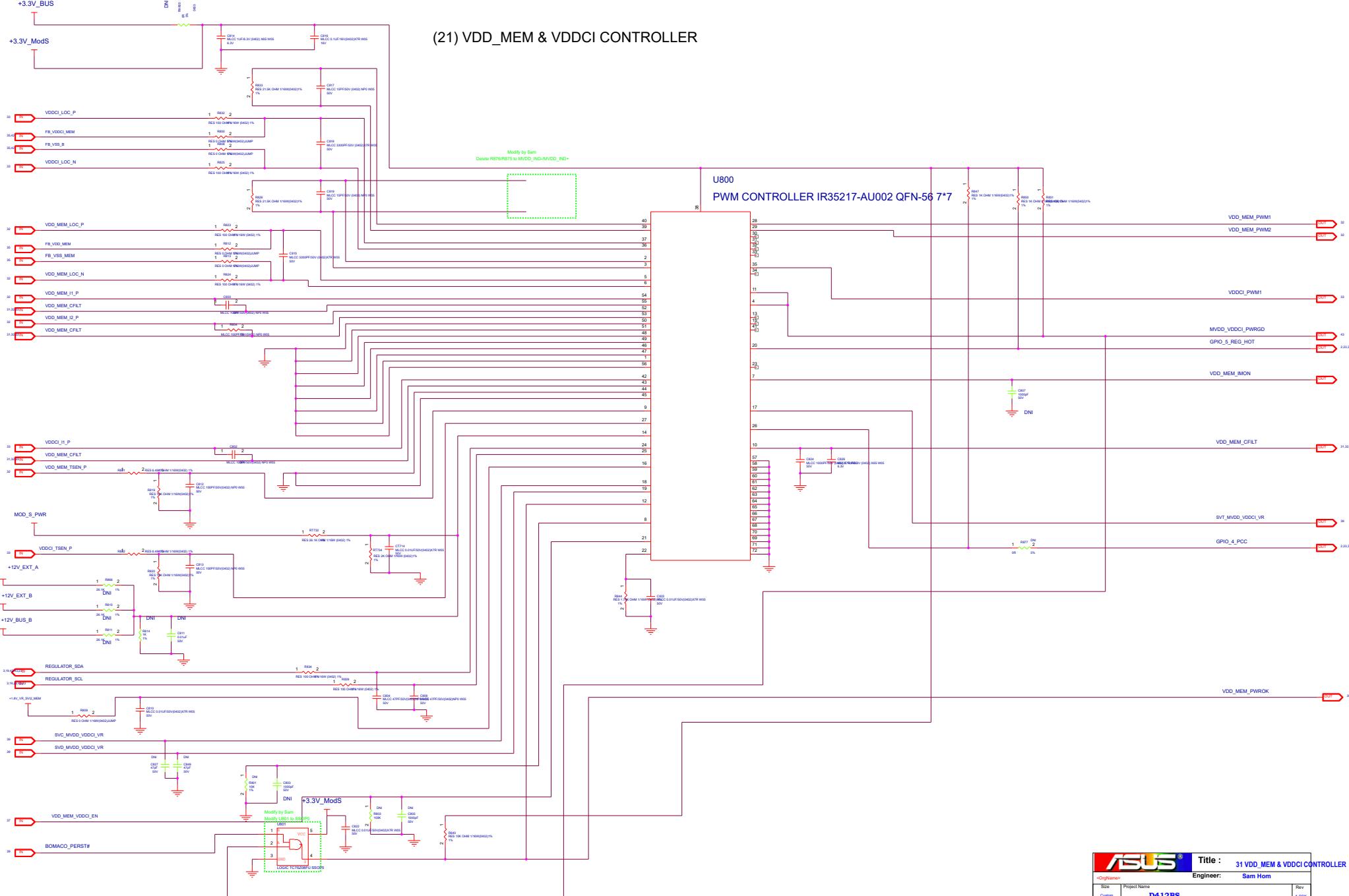


ASIC CH0 -> MEM CHA  
ASIC CH1 -> MEM CHB

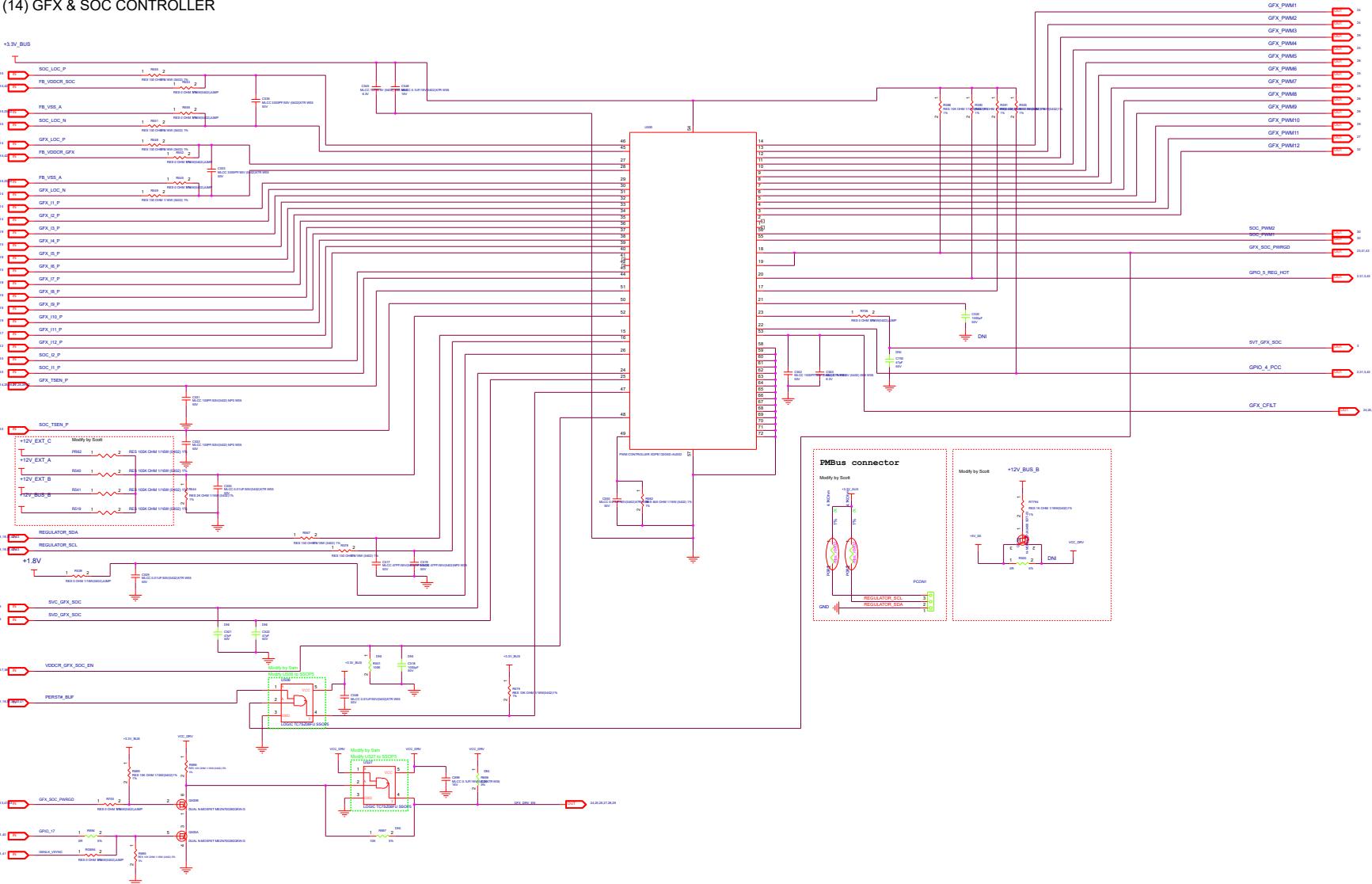


ASIC CH0 -> MEM C

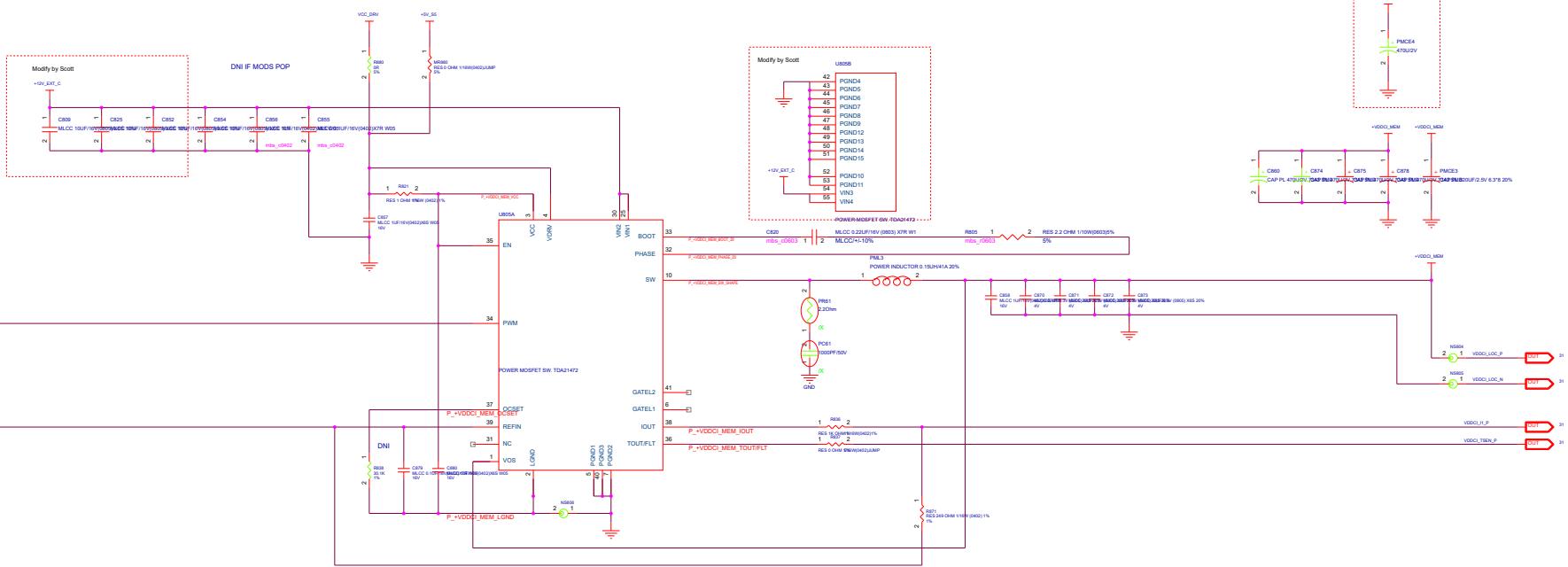


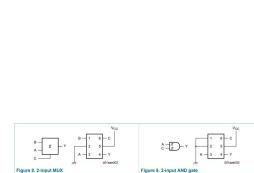
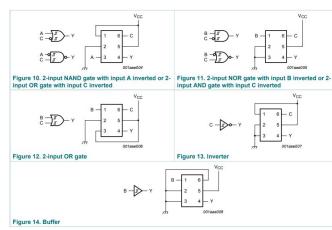


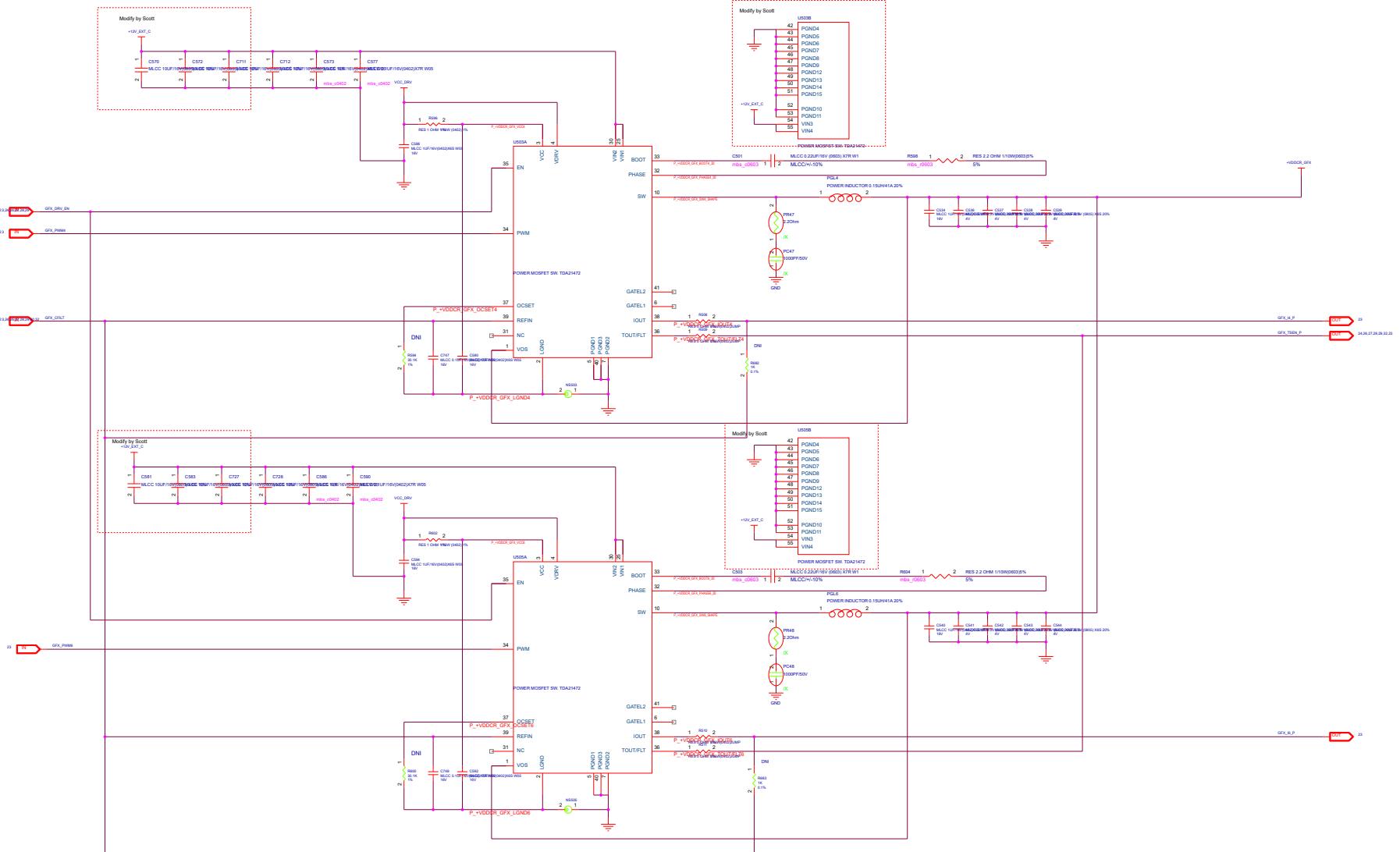
## (14) GFX & SOC CONTROLLER

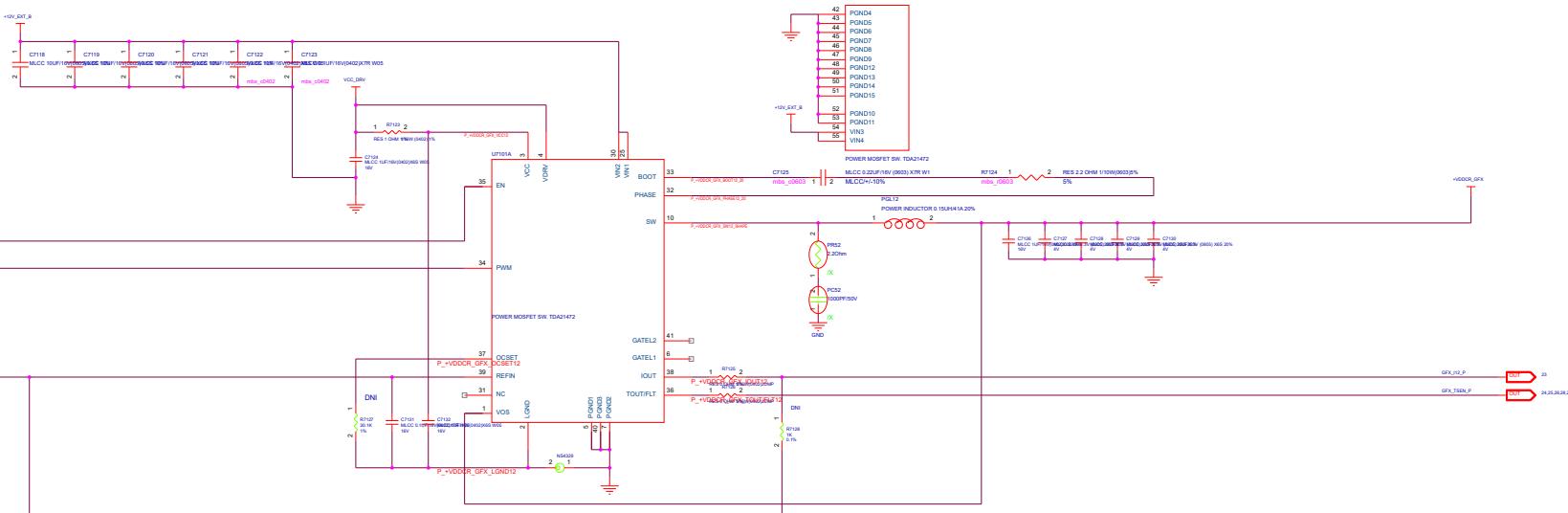
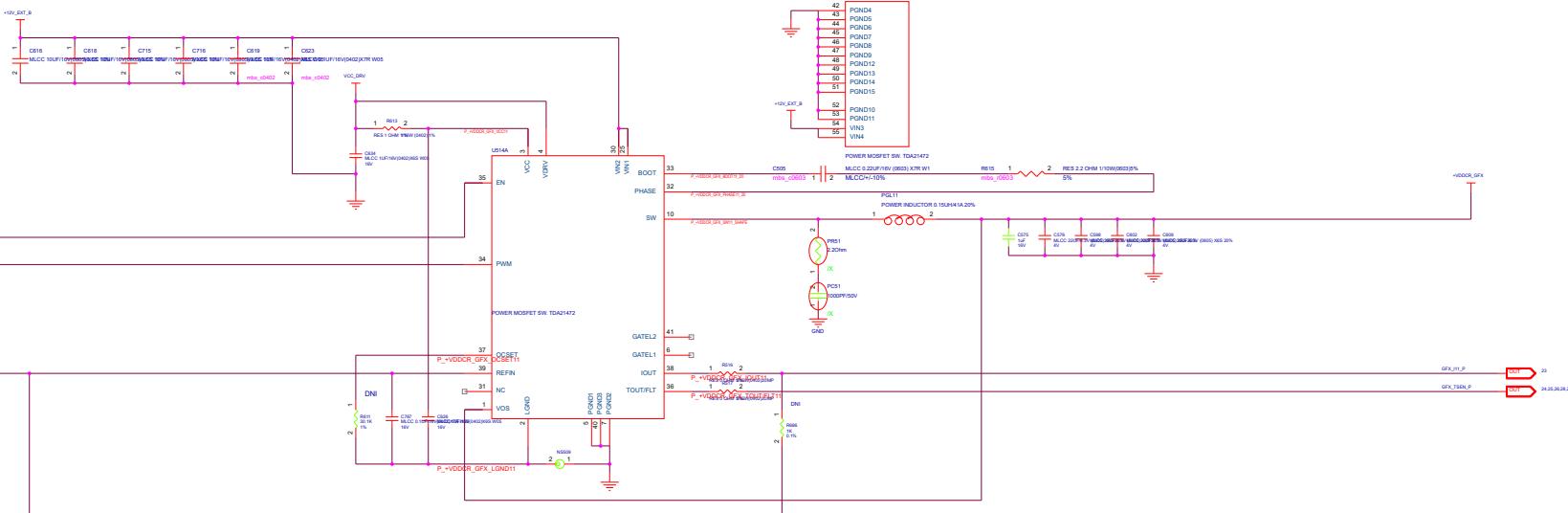


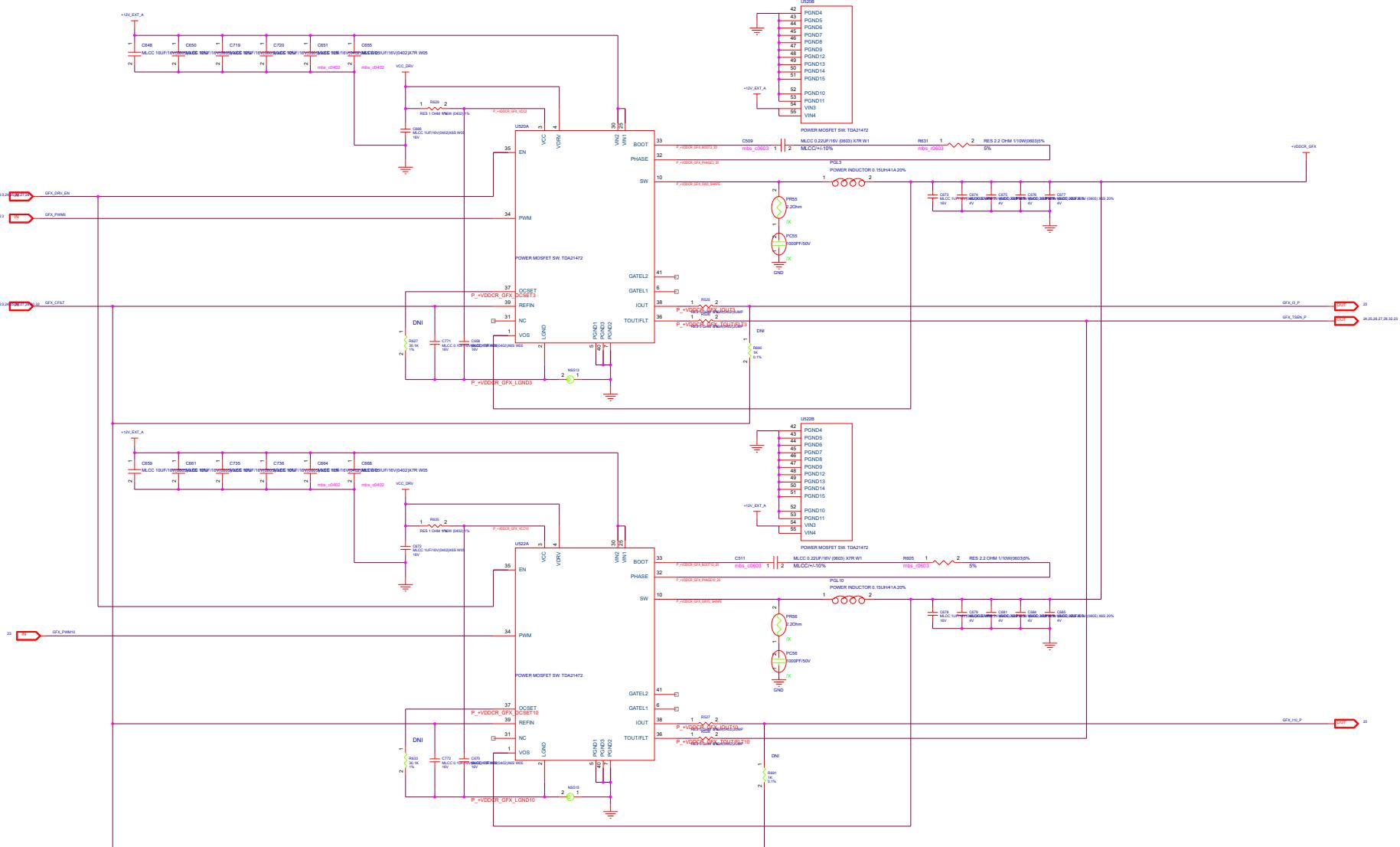
	Title : 23 GFX & SOC CONTROLLER	
Engineer: Sam Hom		
<OrgName>		
Size Custom	Project Name <b>D412BS</b>	Rev 1.00X
Date: September 15, 2010		Sheet 03 of 03

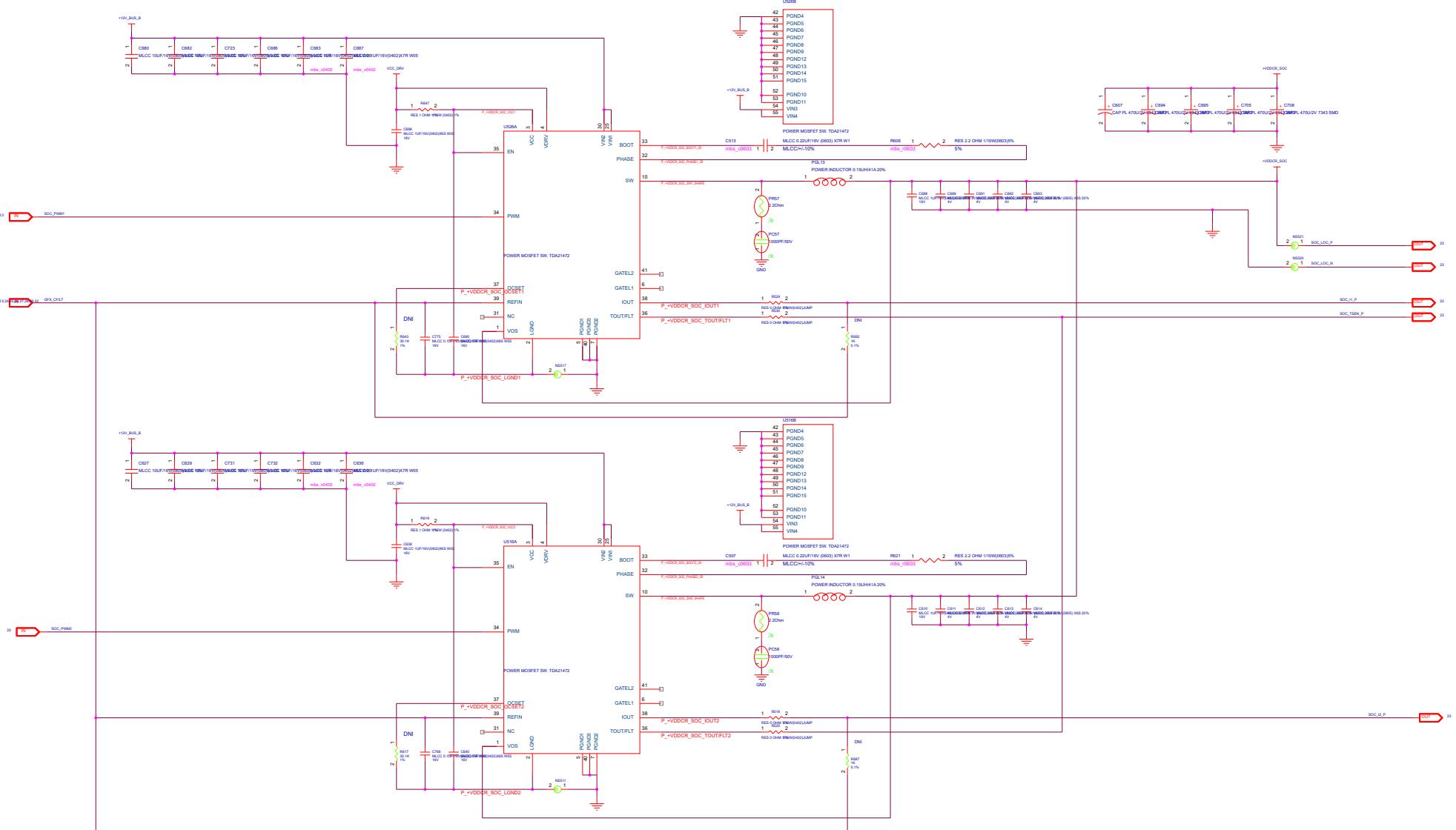


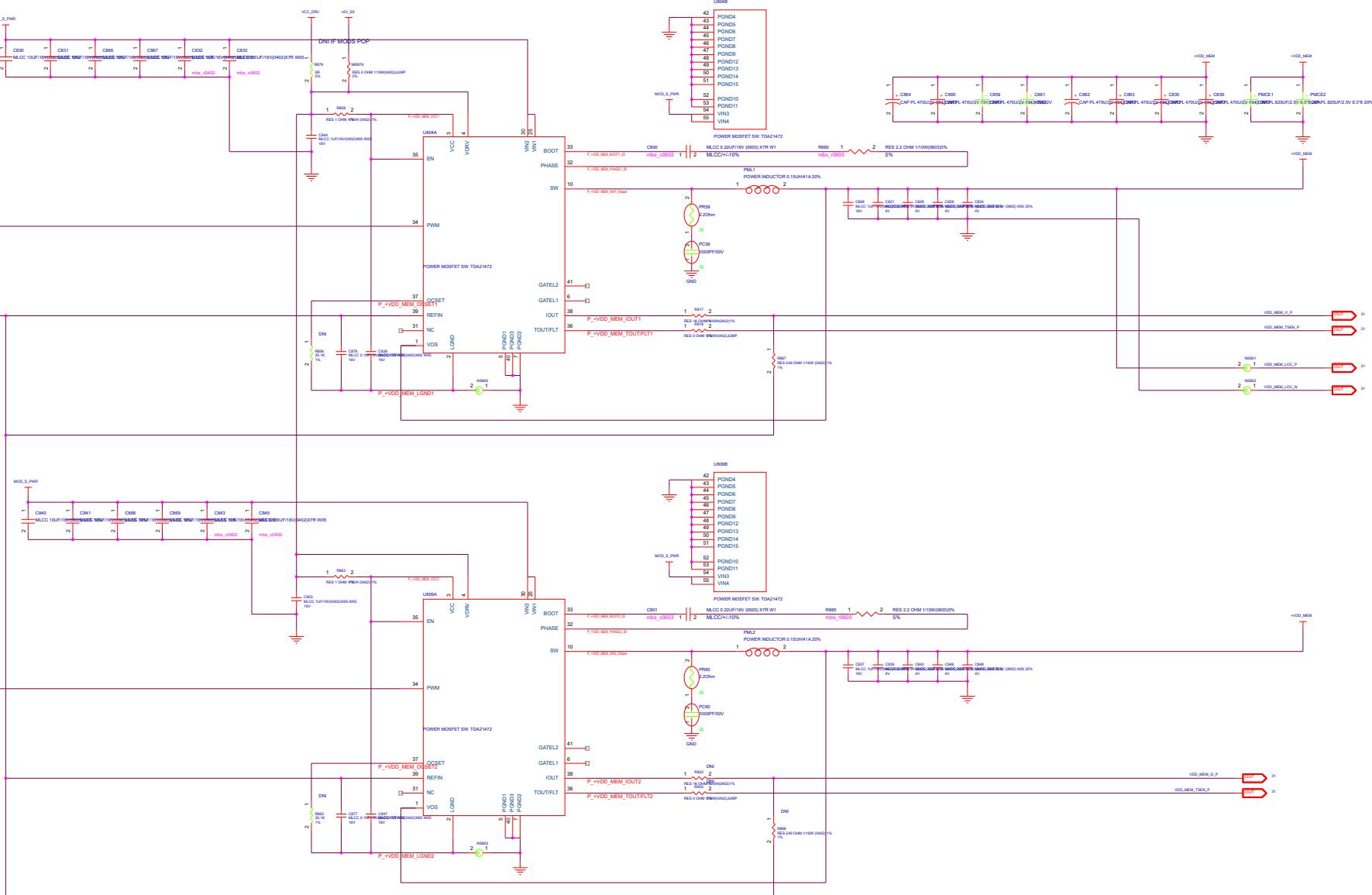




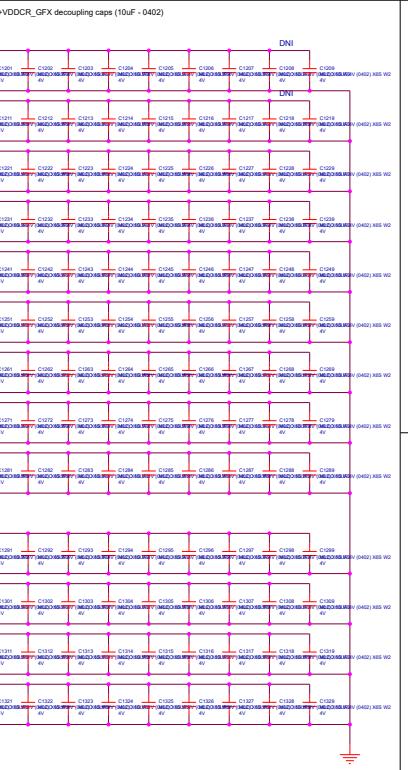




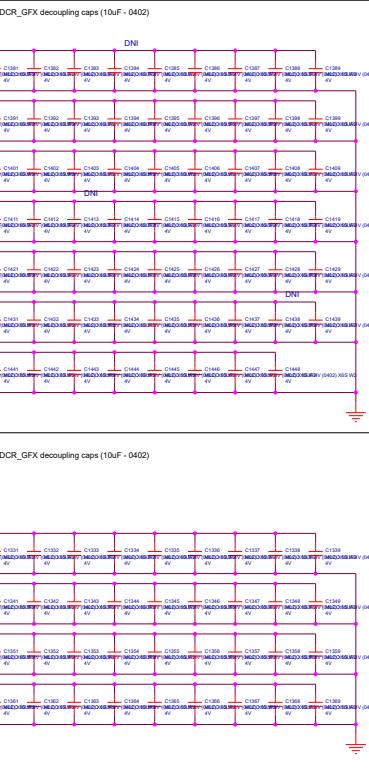




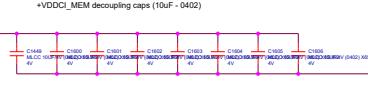
+VDDCR\_GFX



+VDDCR\_GFX



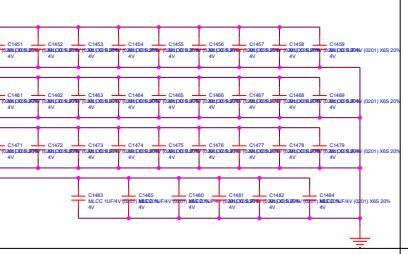
+VDDCI\_MEM



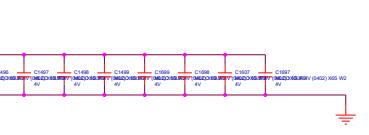
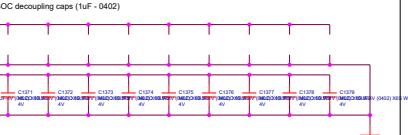
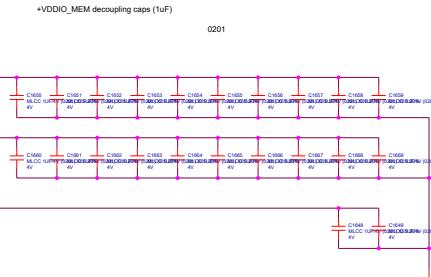
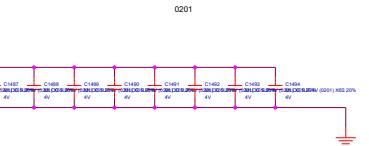
DNI these six caps to match SLT board and keep the design consistent across SKUs

C1218  
C1208  
C1200  
C1438  
C1413  
C1384

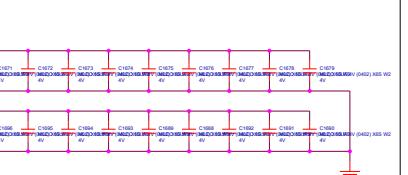
+VDDIO\_MEM decoupling caps (1uF - 0201)



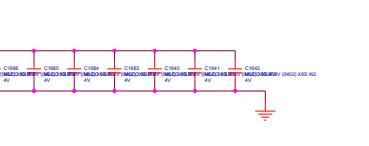
VDDCR\_SOC decoupling caps (1uF)

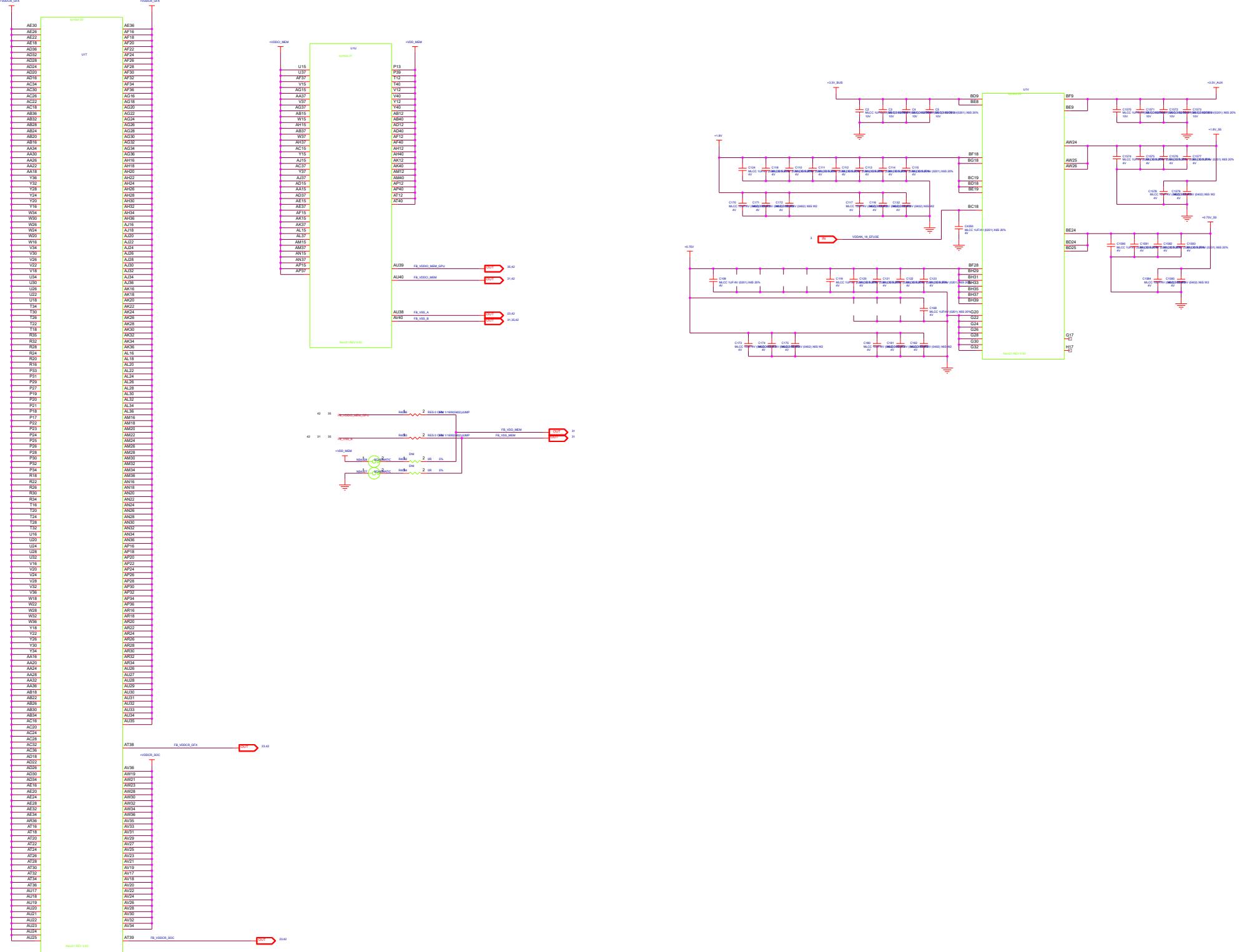


+VDDCI\_MEM decoupling caps (10uF - 0402)

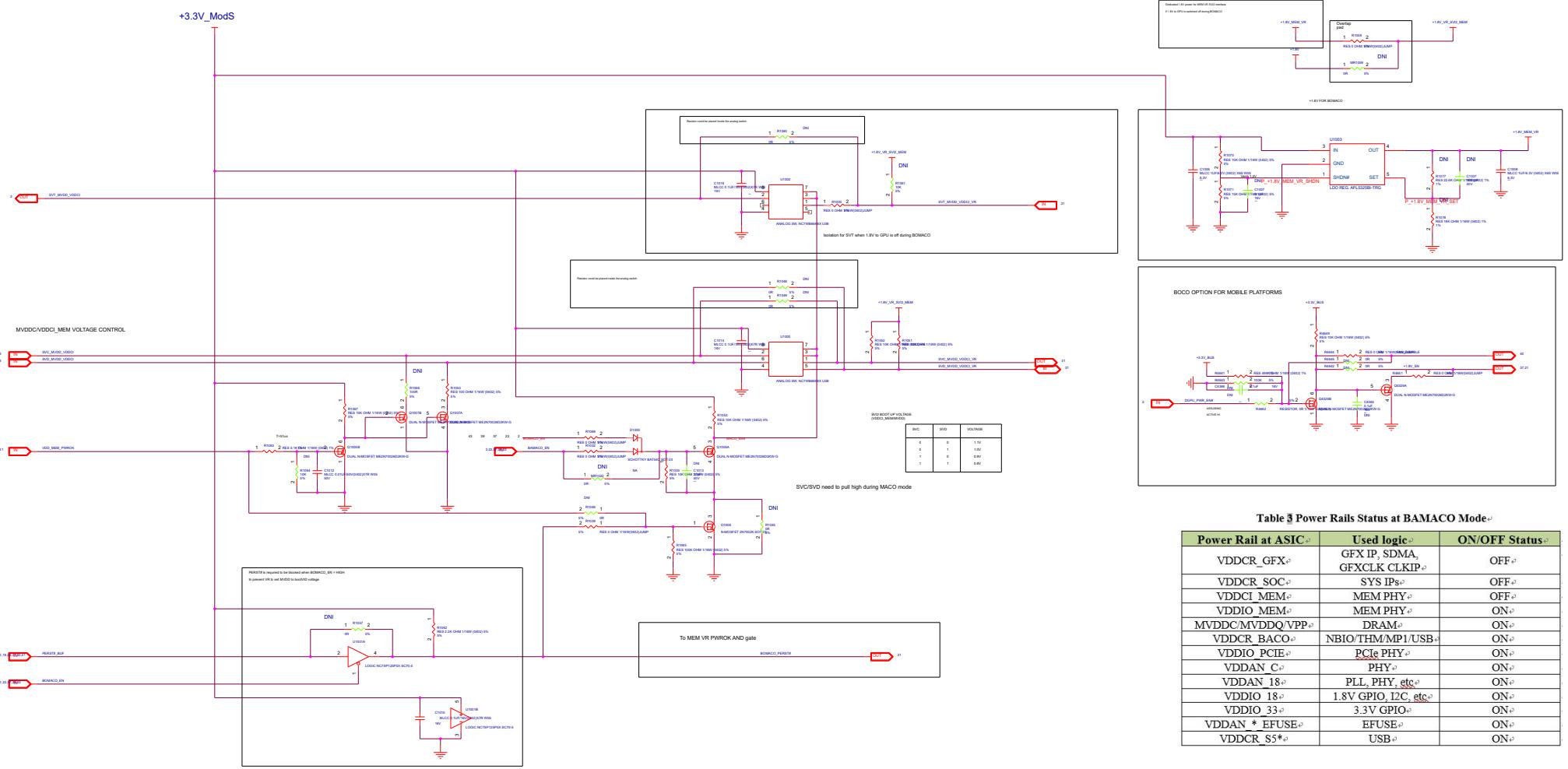


+VDDCR\_MEM decoupling caps (10uF - 0402)





FOR PI DAUGHTER CARD  
Modify by Sam  
Date 12/05/14 08:03 AM 2012



**Table 3** Power Rails Status at BAMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status
VDDCR_GF0	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BAC0	NBIO/THM/MP1/USB	ON
VDDIO_PCIE	PCIe PHY	ON
VDDAN_C0	PHY	ON
VDDAN_18	PLL, PHY, etc	ON
VDDIO_18	1.8V GPIO, I2C, etc	ON
VDDIO_33	3.3V GPIO	ON
VDDAN_*_EFUSE	EFUSE	ON
VDDCR_S5*	USB	ON

**Table 3 Power Rails Status at BOMACO Mode**

Power Rail at ASIC <sup>o</sup>	Used logic <sup>o</sup>	ON/OFF Status for BOMACO-A <sup>o</sup>
VDDCR_GFX <sup>o</sup>	GFX IP, SDMA, GFXCLK CLKIP <sup>o</sup>	OFF <sup>o</sup>
VDDCR_SOC <sup>o</sup>	SYS IPS <sup>o</sup>	OFF <sup>o</sup>
VDDCI_MEM <sup>o</sup>	MEM PHY <sup>o</sup>	OFF <sup>o</sup>
VDDIO_MEM <sup>o</sup>	MEM PHY <sup>o</sup>	ON <sup>o</sup>
MVDDC/MVDDQ/VPP <sup>o</sup>	DRAM <sup>o</sup>	ON <sup>o</sup>
VDDCR_BACO <sup>o</sup>	NBIO/THM/MP1/USB <sup>o</sup>	OFF <sup>o</sup>
VDDIO_PCIE <sup>o</sup>	PCIe PHY <sup>o</sup>	OFF <sup>o</sup>
VDDAN_C <sup>o</sup>	PHY <sup>o</sup>	OFF <sup>o</sup>
VDDAN_18 <sup>o</sup>	PLL, PHY, etc. <sup>o</sup>	OFF <sup>o</sup>
VDDIO_18 <sup>o</sup>	1.8V GPIO, I <sub>C</sub> , etc. <sup>o</sup>	OFF <sup>o</sup>
VDDIO_33 <sup>o</sup>	3.3V GPIO <sup>o</sup>	OFF <sup>o</sup>
VDDAN_EFUSE <sup>o</sup>	EFUSE <sup>o</sup>	OFF <sup>o</sup>
VDDCR_SS <sup>o</sup>	USB <sup>o</sup>	ON <sup>o</sup>

**Table 4 Key Signals at Different PM Modes**

Signals	Default	BOCO	BOMACO
PX EN <sup>a</sup>	LOW <sup>a</sup>	N/A <sup>a</sup>	N/A <sup>a</sup>
MACO EN <sup>a</sup>	N/A <sup>a</sup>	N/A <sup>a</sup>	N/A <sup>a</sup>
PERSTB <sup>b</sup>	HIGH <sup>c</sup>	1>0>1 <sup>c</sup>	1>0>1 <sup>c</sup>
PWR EN <sup>a</sup>	HIGH <sup>a</sup>	LOW <sup>a</sup>	LOW <sup>a</sup>
BOMACO EN <sup>a</sup>	LOW <sup>a</sup>	LOW <sup>a</sup>	HIGH <sup>a</sup>

**Table 5 Platform to Support BOMACO+**

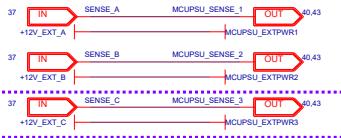
BOMACO EN	SVC PU/PD	SVD PU/PD
HIGH <sup>o</sup>	PU <sup>o</sup>	PU <sup>o</sup>
LOW <sup>o</sup>	bootVID <sup>o</sup>	bootVID <sup>o</sup>

## Power



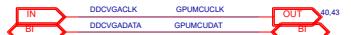
From 12V (for 外接式風扇使用, 任一組12V皆可)  
 From PCIE 3V3\_AUX (for ITE)  
 From BUS 3V3 (for ITE logic判斷)  
 For 12V to 5V ARGB PWR

## PSU DETECT INPUT



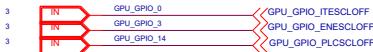
From EXT 0 (外部電源第一組)  
 From EXT1 (外部電源第二組)  
 From EXT2 (外部電源第三組)

## I2C



GPU I2CB Master (for ITE / ENE)

## GPU\_GPIO



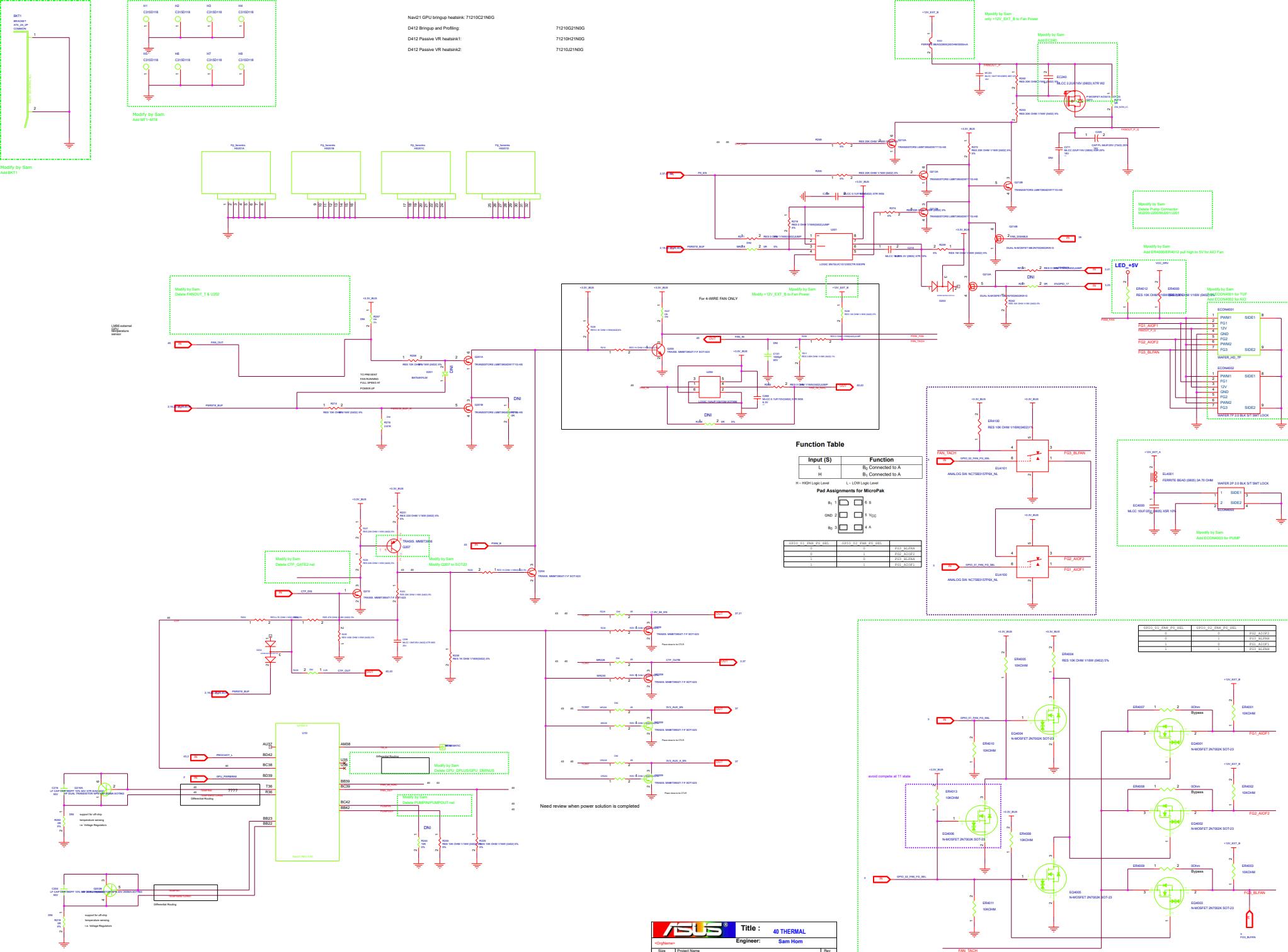
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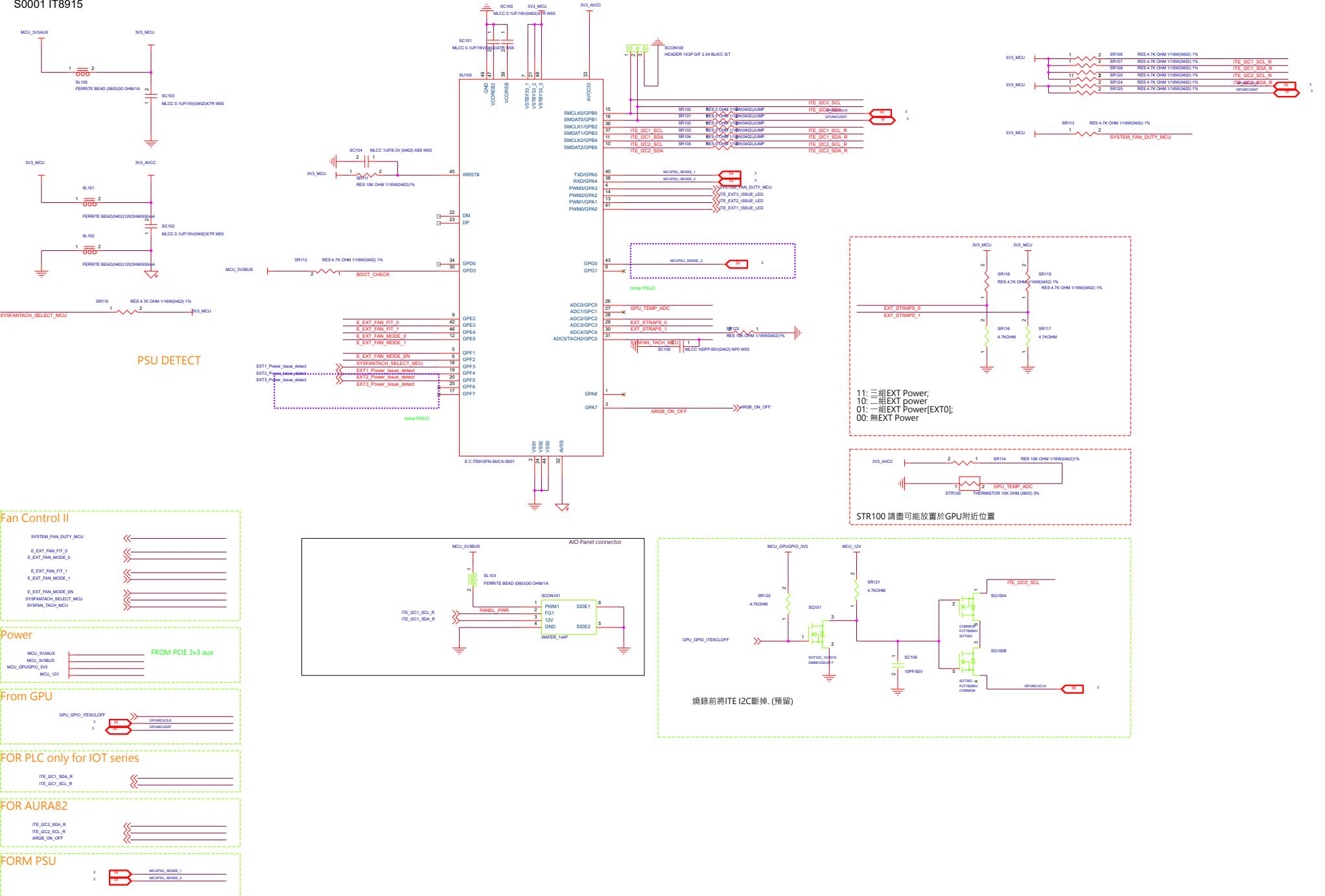
Engineer: Sam Horn

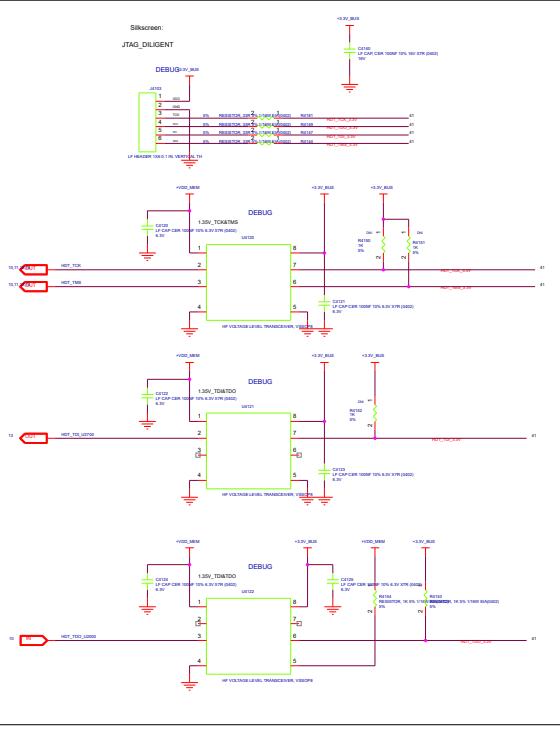
Size	Project Name	Rev
B	D412BS	1.00X

Date: Tuesday, November 10, 2020

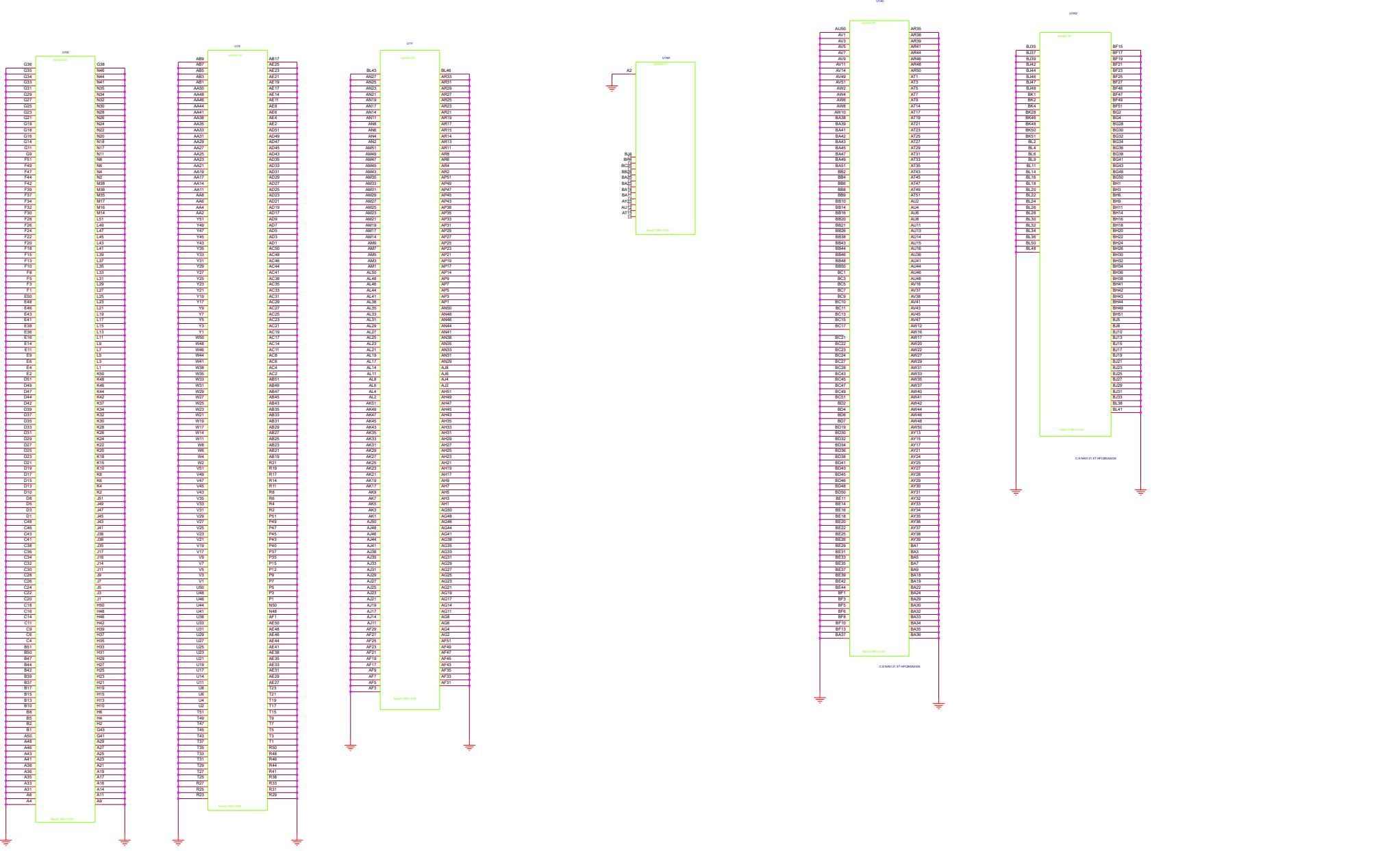
Sheet 46 of 51







Modify by Sam  
Delete RGB LED header  
Delete RADEON Lightbar



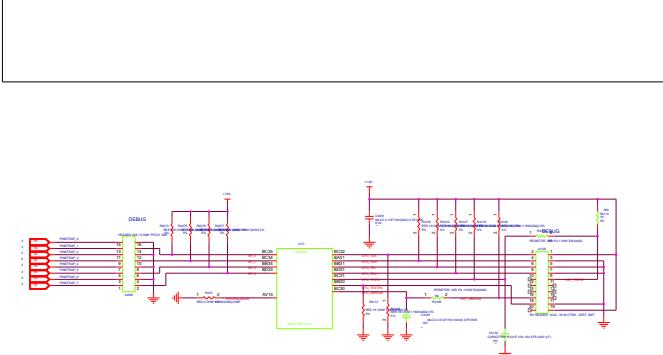
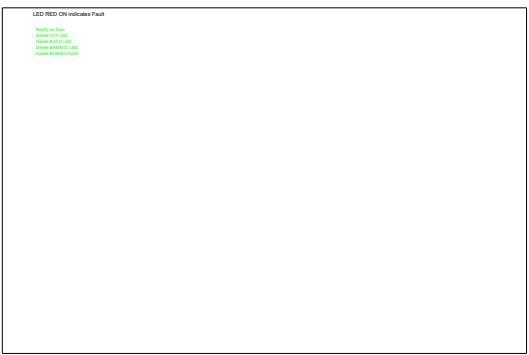
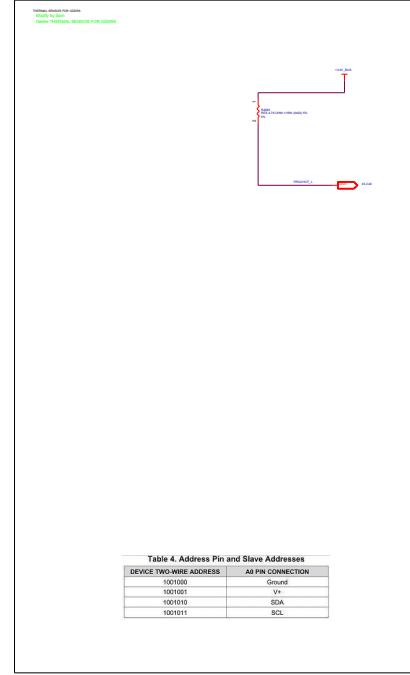
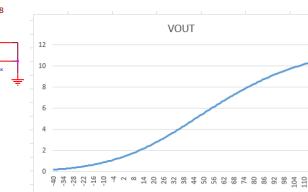
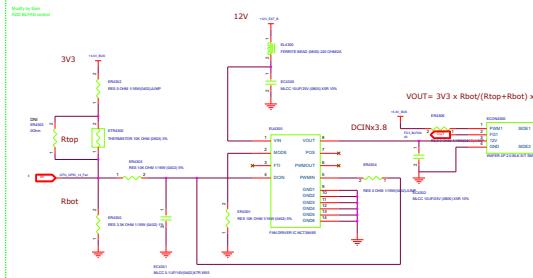
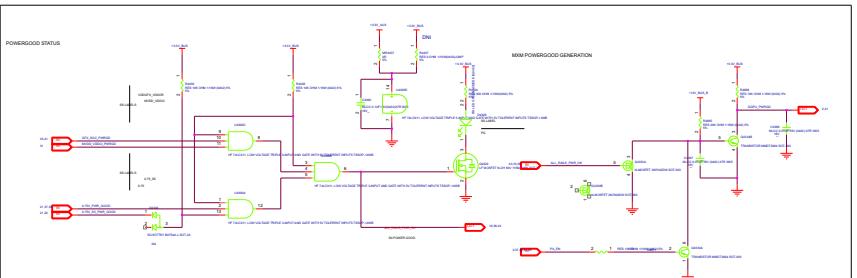
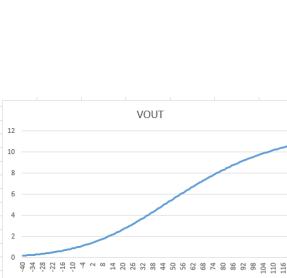
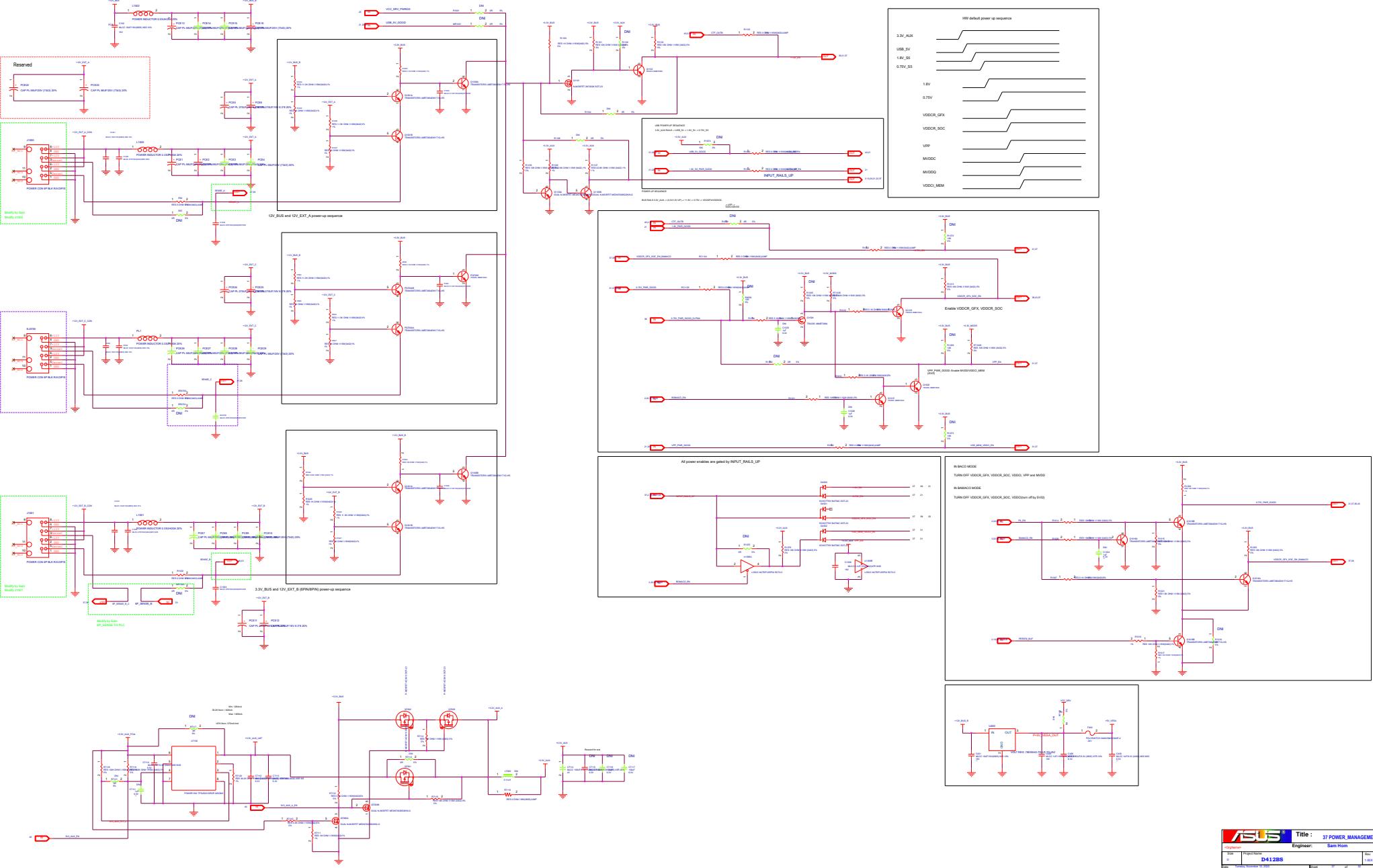


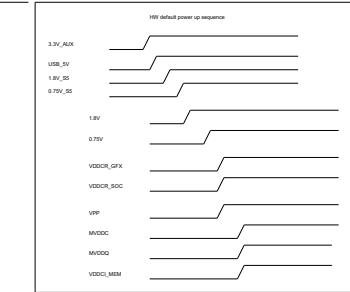
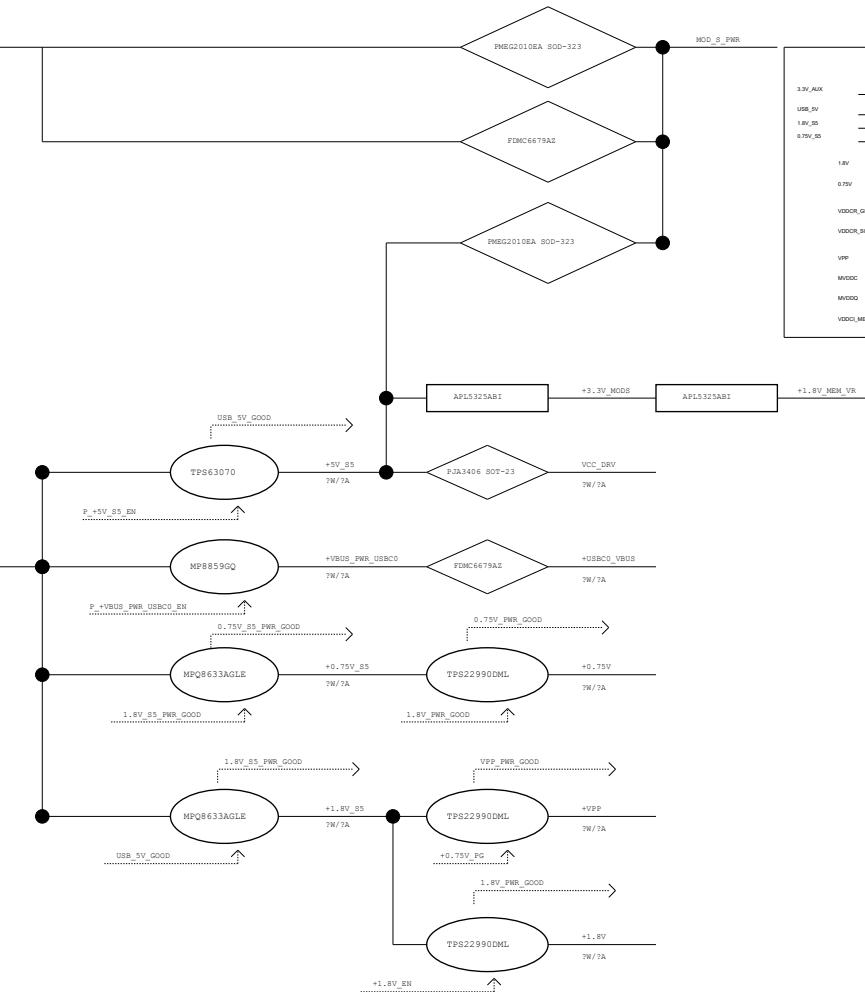
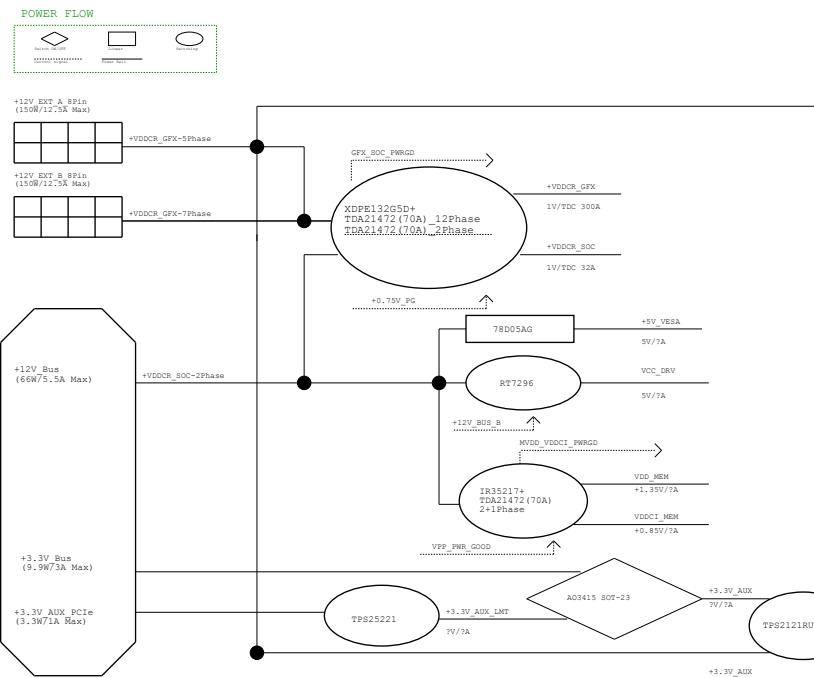
Table 4. Address Pin and Slave Addresses	
DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL

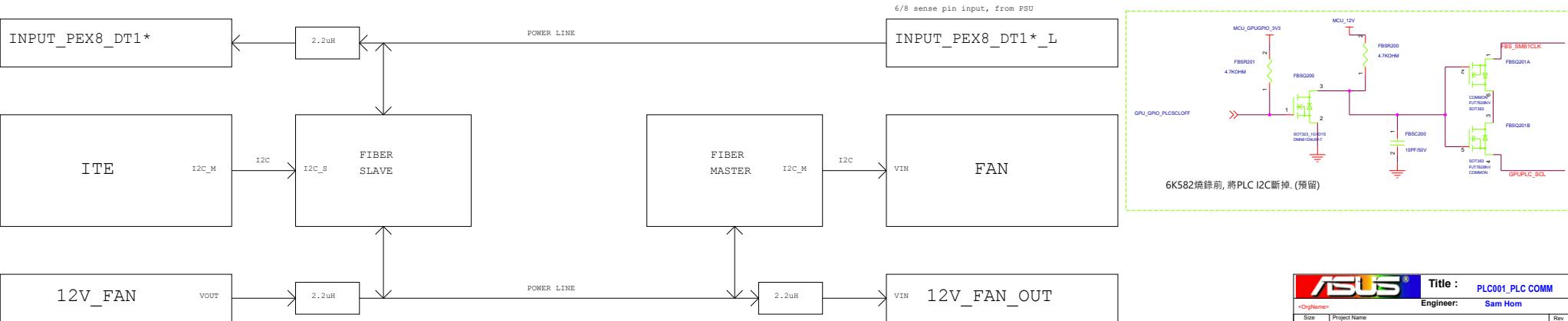
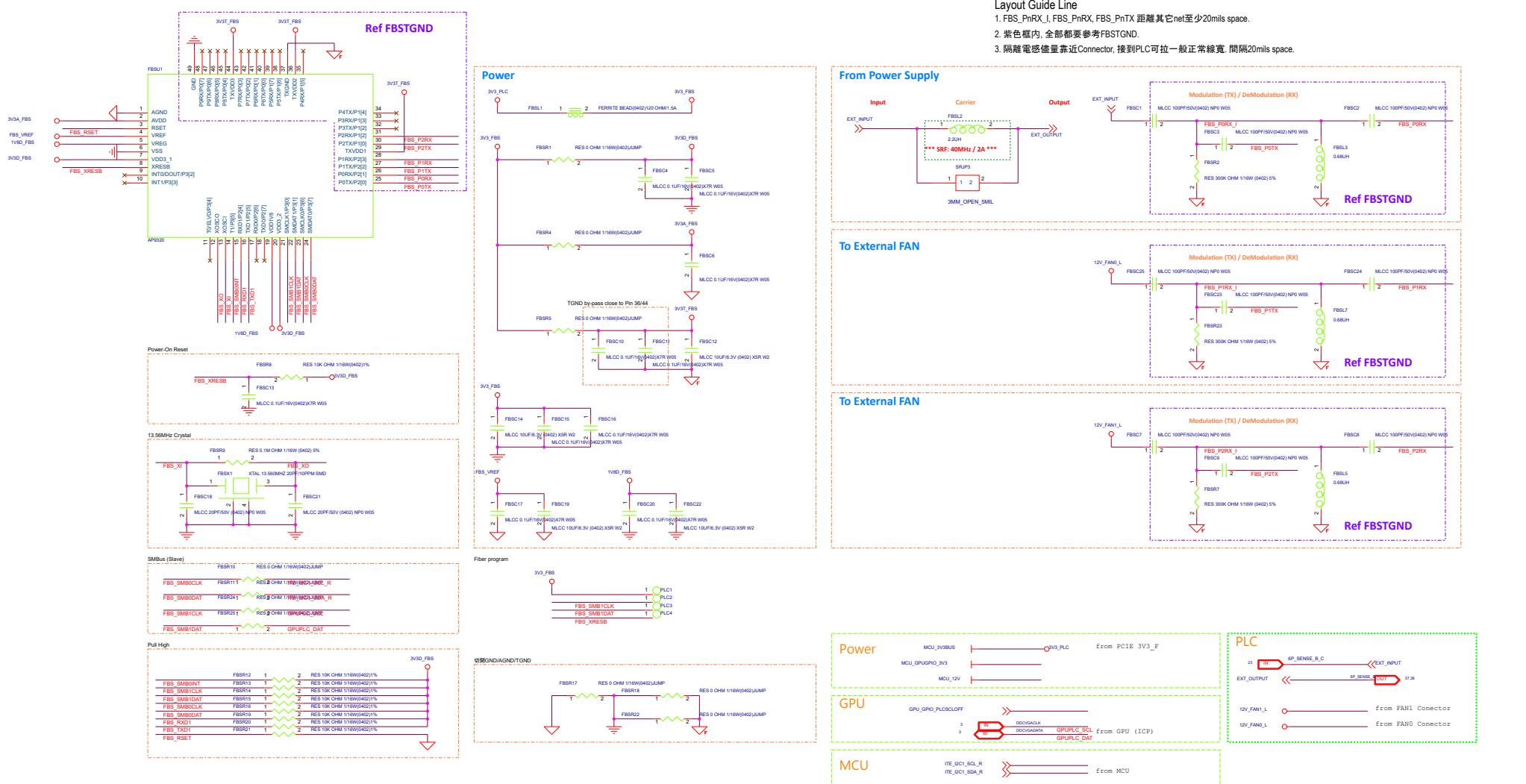


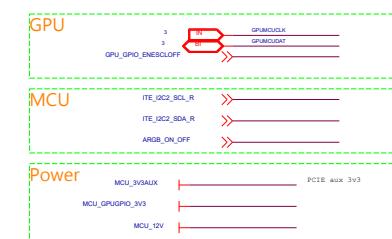
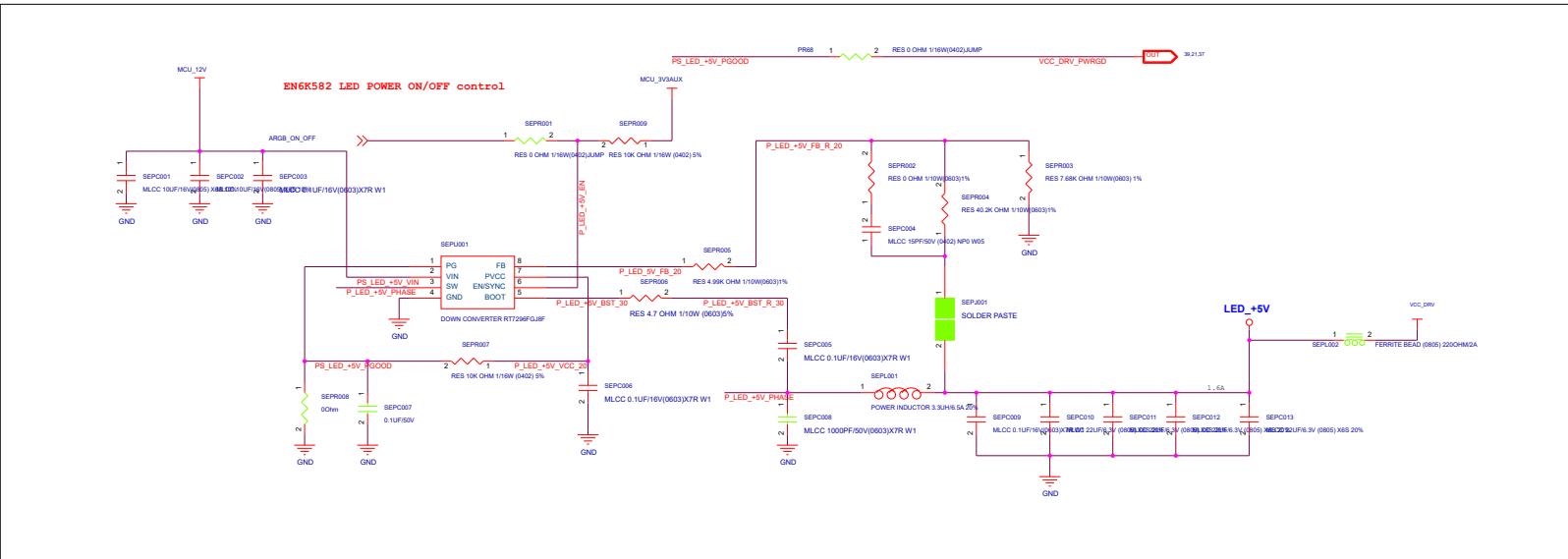
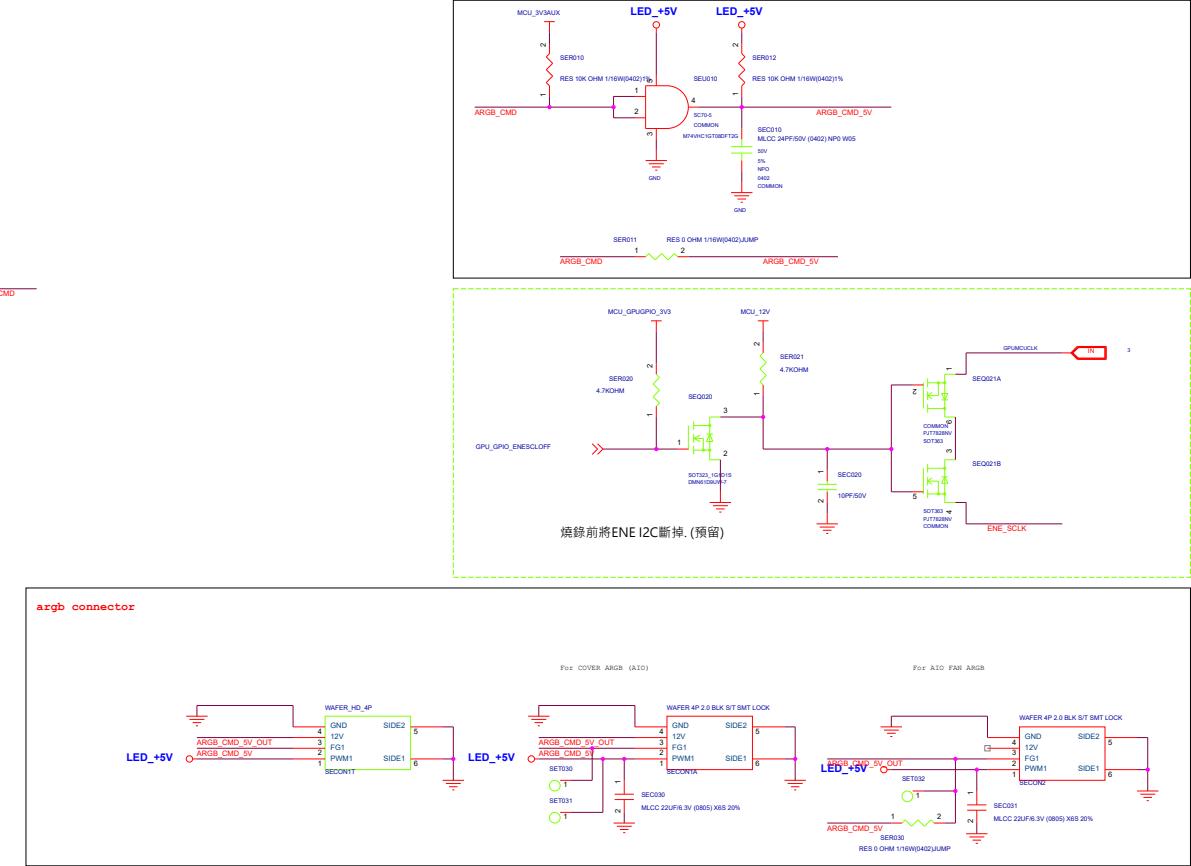
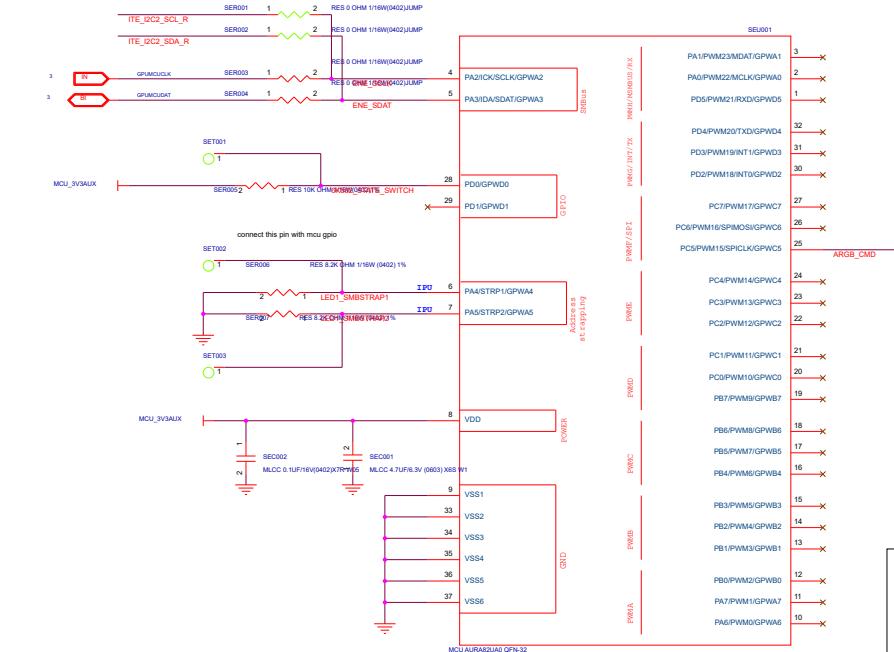


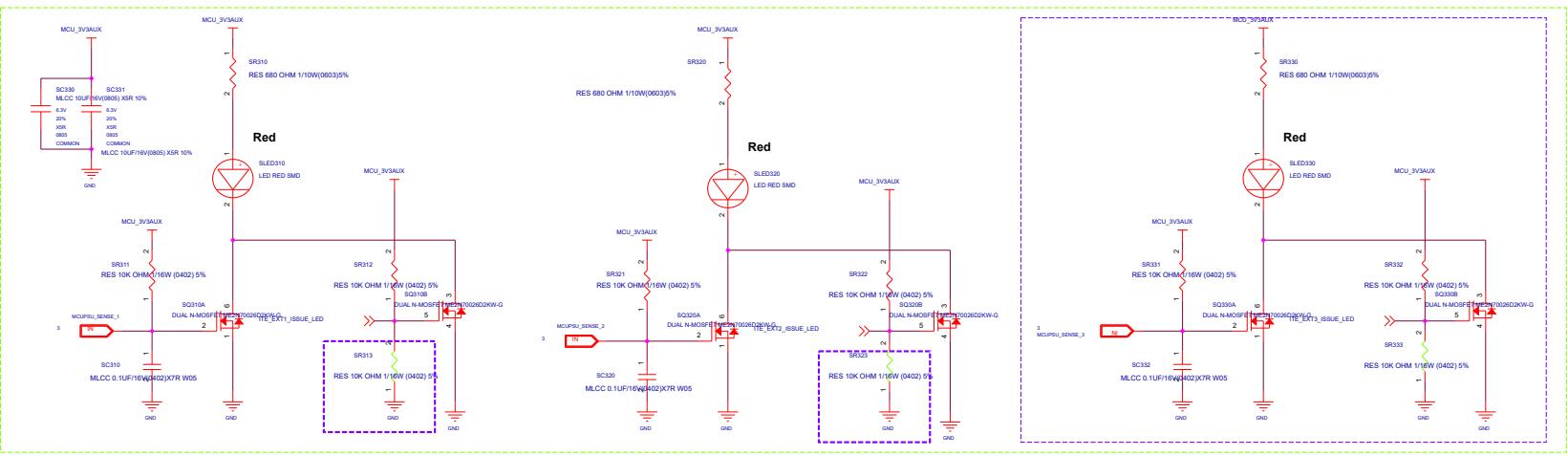
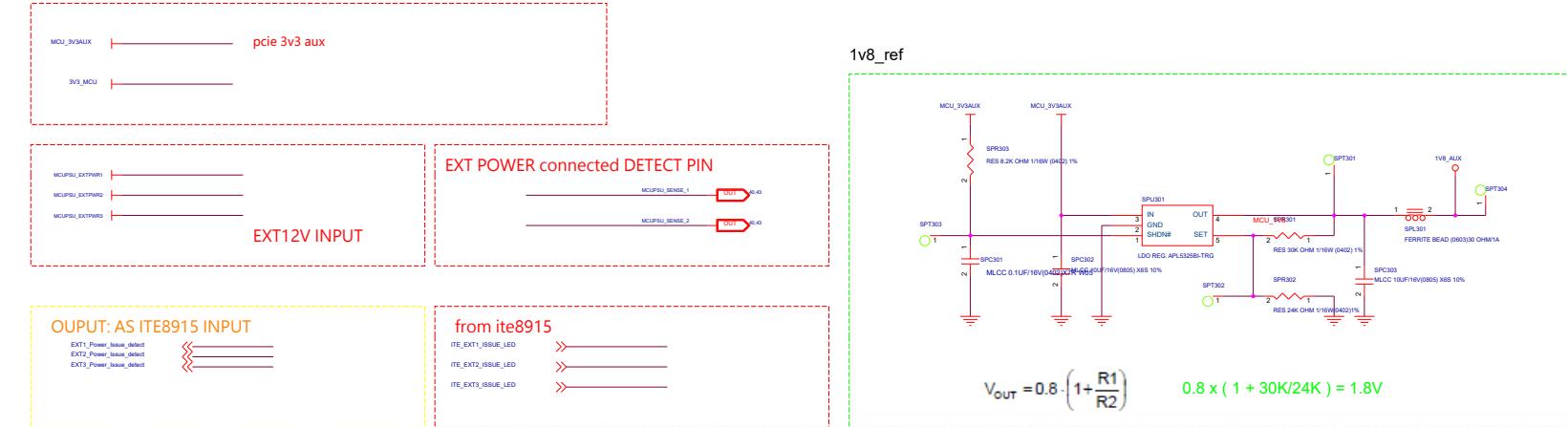
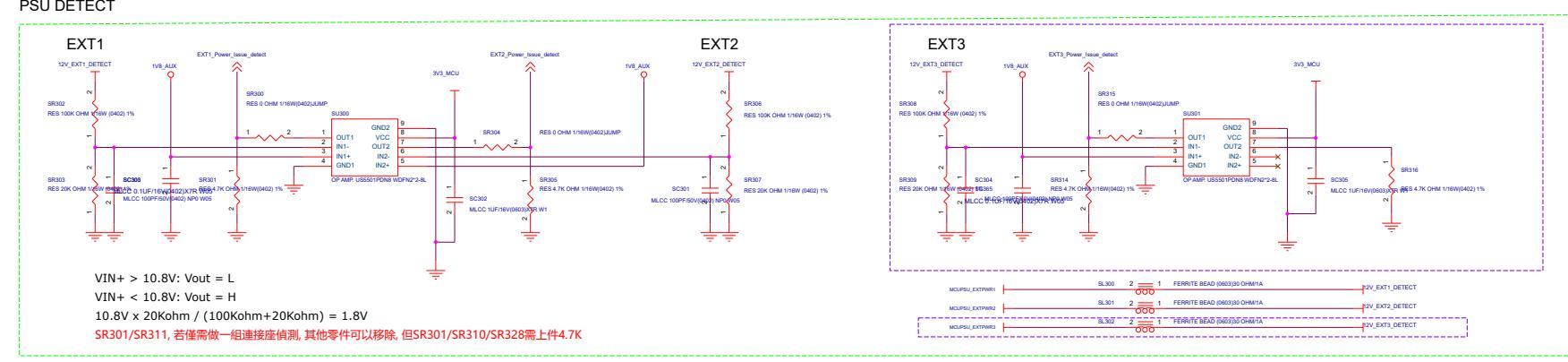
1 -00B  
Nov 11  
2018  
Added MODS circuit

1 -00C  
Jan 19  
2018  
Connected +12V\_50 to OSC\_VDD18  
Gated +VBUS\_PWR\_USB03 by  
USB4C\_D007 Power protection  
control

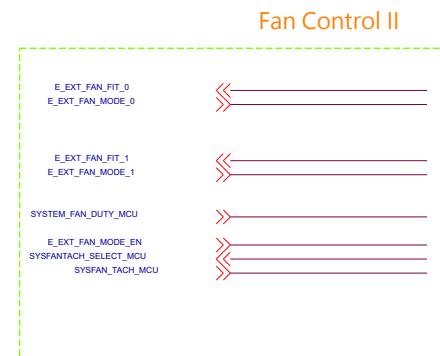
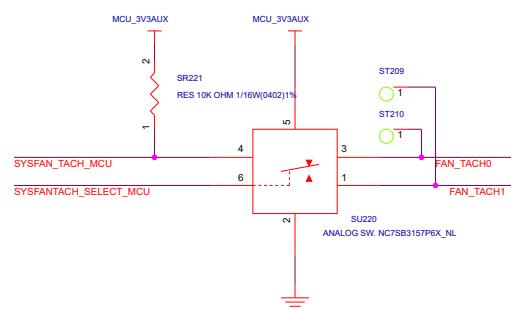
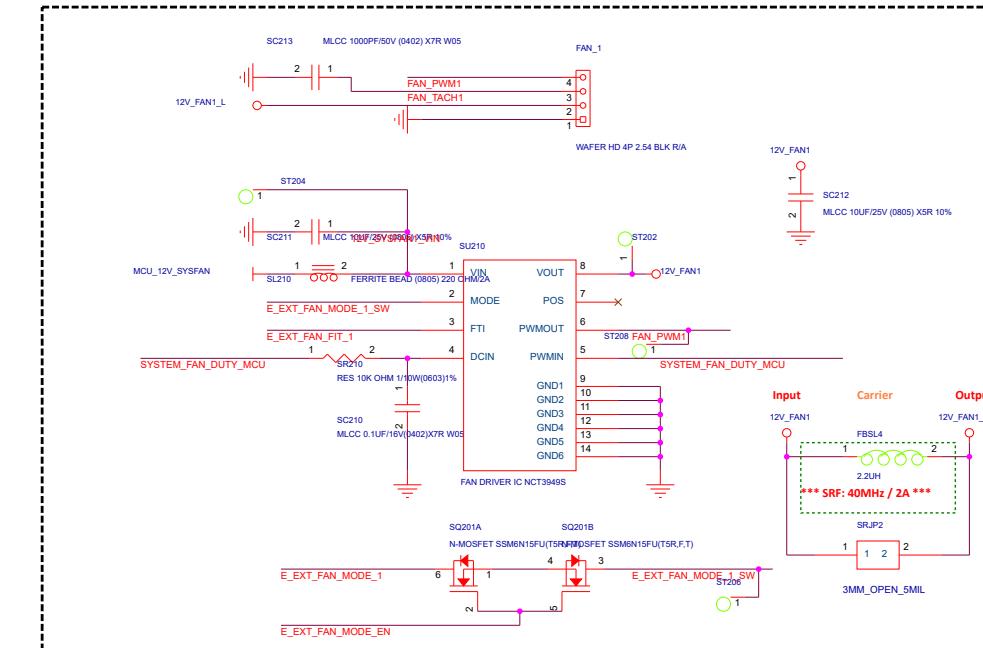
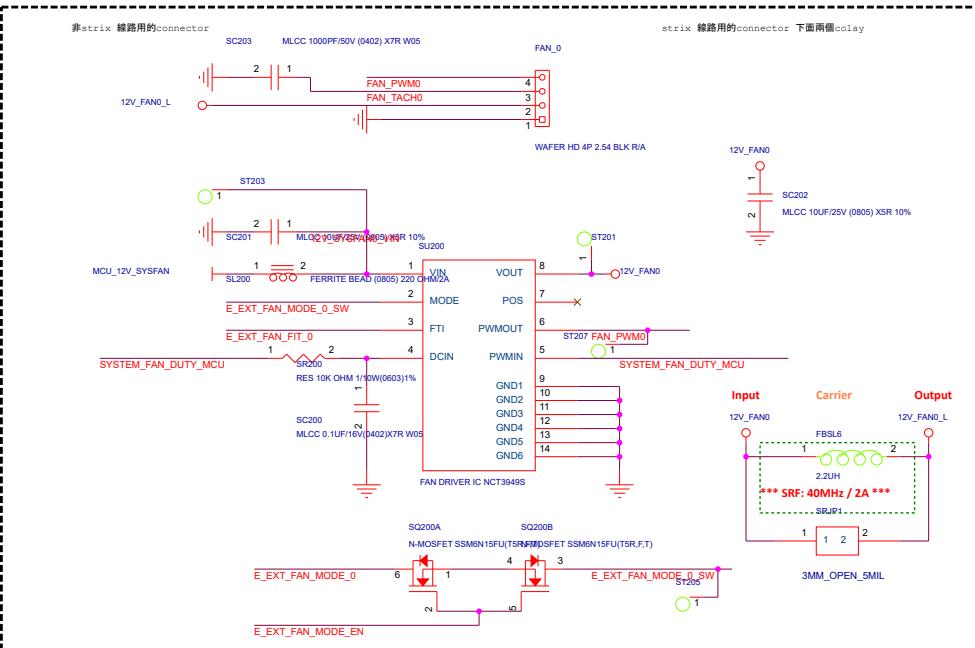








- 1.EXT power is not connected, the led is always on
- 2.EXT power is connected EXT 12V is over 10.8V, the led turns off EXT 12v is below 10.8v.the led blink



Title : STRIX004\_SYSTEM FAN CONTROL

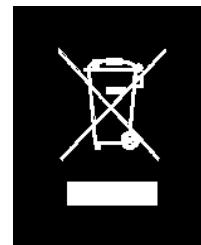
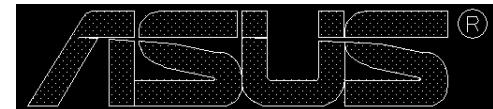
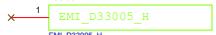
Engineer: Sam Hom

Size	Project Name	Rev
B	D412BS	1.00X
Date:	Tuesday, November 10, 2020	
Sheet	50	of 51

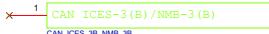
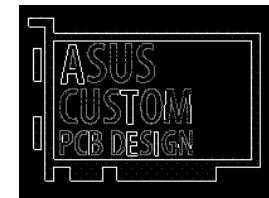
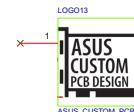
# ASUS VGA PCB Logo



PCB MADE IN CHINA



ASUS Re-design logo  
Do not place this on reference board



CAN ICES-3 (B)/NMB-3(B)

