

PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

TABLE OF CONTENTS

Page Description

Page Description

Page Description

1	Table of Contents
2	Block Diagram
3	PCI Express
4	PCI Termination
5	MEMORY: GPU Partition A/B
6	MEMORY: FBA Partition 31..0
7	MEMORY: FBA Partition 63..32
8	MEMORY: FBB Partition 31..0
9	MEMORY: FBB Partition 63..32
10	MEMORY: GPU Partition C/D
11	MEMORY: FBC Partition 31..0
12	MEMORY: FBC Partition 63..32
13	MEMORY: FBD Partition 31..0
14	MEMORY: FBD Partition 63..32
15	GPU PWR and GND
16	GPU Decoupling
17	GPU DECOUPLING
18	IFPAB TALL-DP
19	IFPE DP
20	IFPF USBC
21	IFPC HDMI 2.0/DP
22	IFPD DP
23	NVHS INTERFACE
24	MISC: FAN,THERMAL,JTAG,GPIO,STEREO
25	MISC3: ROM, STRAPS

26	MISC: XTAL, PLL
27	MISC: USB PPC
28	PS: USB VR
29	PS: 5V, 5V BACKUP
30	PS: PEXVDD, 1V8
31	PS: FBVDD CONTROLLER
32	PS: FBVDD CONTROLLER OVR3
33	PS: FBVDD PHASE 1, 2
34	PS: NVVDD CONTROLLER OVR8
35	PS: NVVDD Phase 1, 2
36	PS: NVVDD Phase 3, 4
37	PS: NVVDD Phase 5, 6
38	PS: NVVDD Phase 7, 8
39	PS: INPUT SWITCH RTD3
40	PS: INPUT SWITCH RTD3 USB
41	PS: INPUT SWITCH RAIL BALANCE
42	PS: 12V CURRENT STEERING
43	PS: VR THERMAL PROTECTION
44	PS: INPUTS, FILTERING AND MONITORING
45	PS: CURRENT STEERING,HOT UNPLUG DETECT
46	PS: PRE-FILTER
47	SEQUENCE: 5V, 1V8, NV3V3 ENABLE
48	SEQUENCE: NV, PEX, FB ENABLE
49	SEQUENCE: PCIE VOLTAGE MONITOR
50	SEQUENCE: DISCHARGE

51	SEQUENCE: MISC
52	LED & FAN HEADERS
53	LED 2
54	Mechanical: Bracket/Thermal Solution

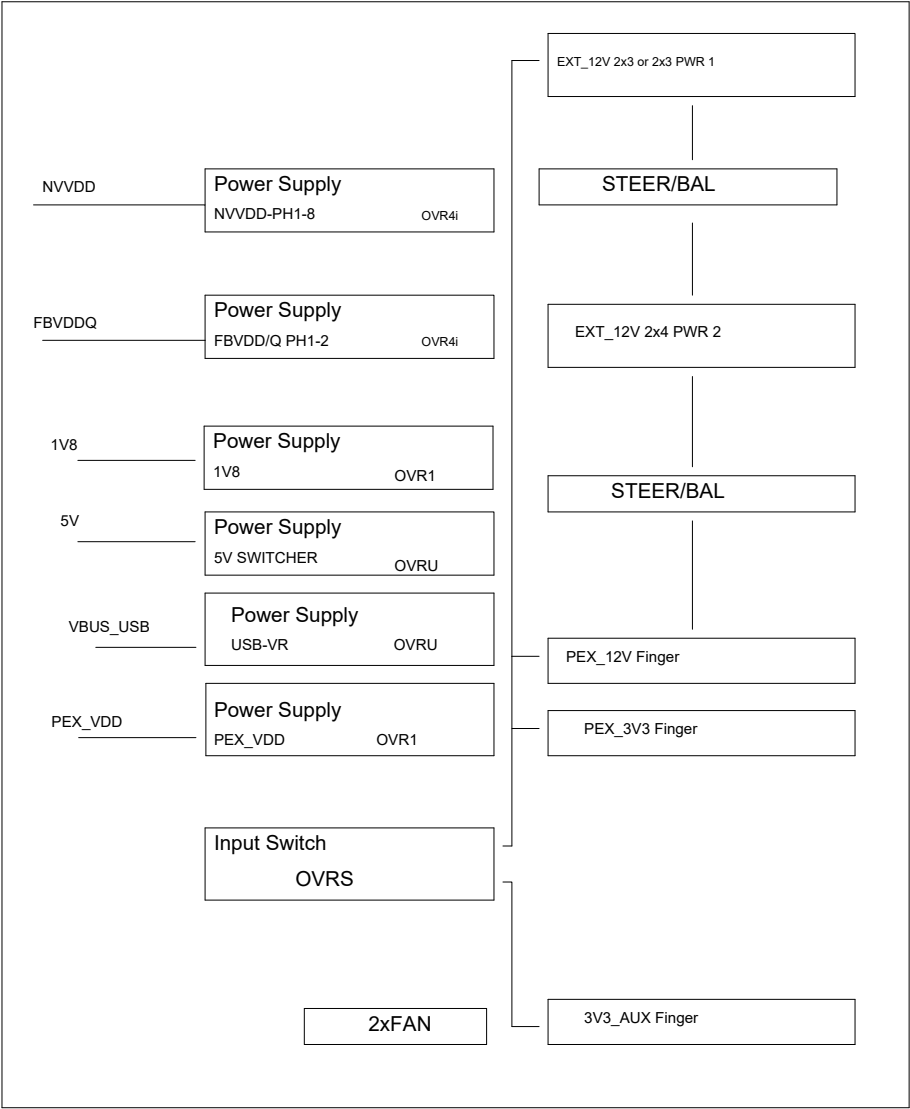
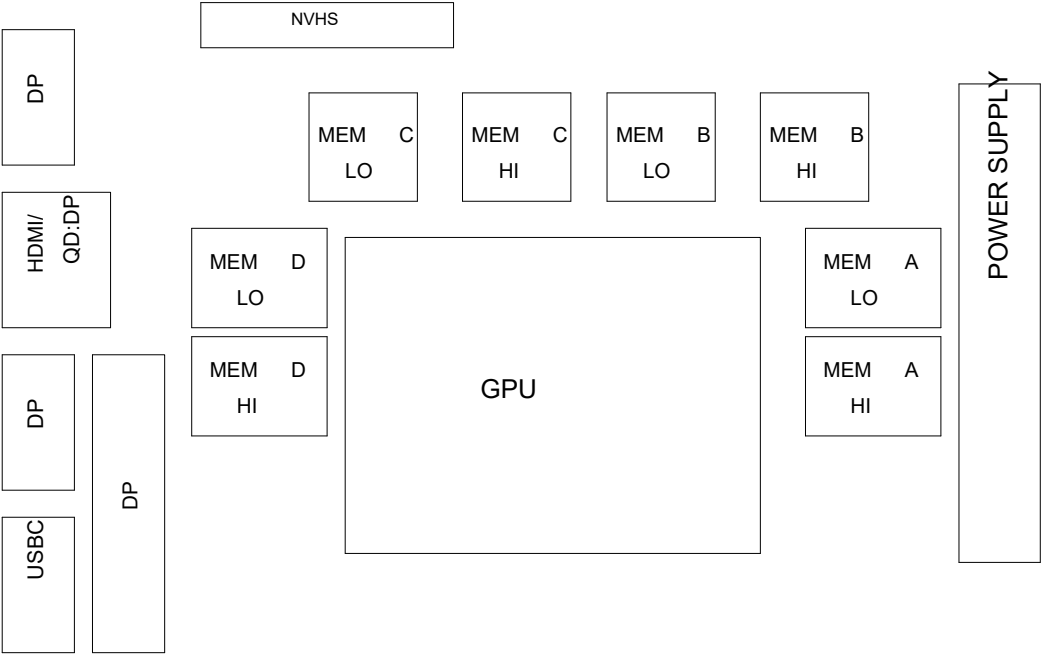
base on V372-02S change for D18 Z
 1. P.23 remove SLI & BRIDGE_LED_VDD & SLI_BRG_PRST*
 2. P.52 remove LED change FAN connector
 3. P.53 remove LED
 4. P.38/44 add FUSE
 5. P.5~14 mem add <>
 6. P.53 LED use V336-0D
 7. P.32 remove
 8. P.35~38 dual MOS
 9. P.33 change dual MOS
 10. P.43 remove
 11. P.31 change to UP1666
 12. P.21 remove colay DP

0727:

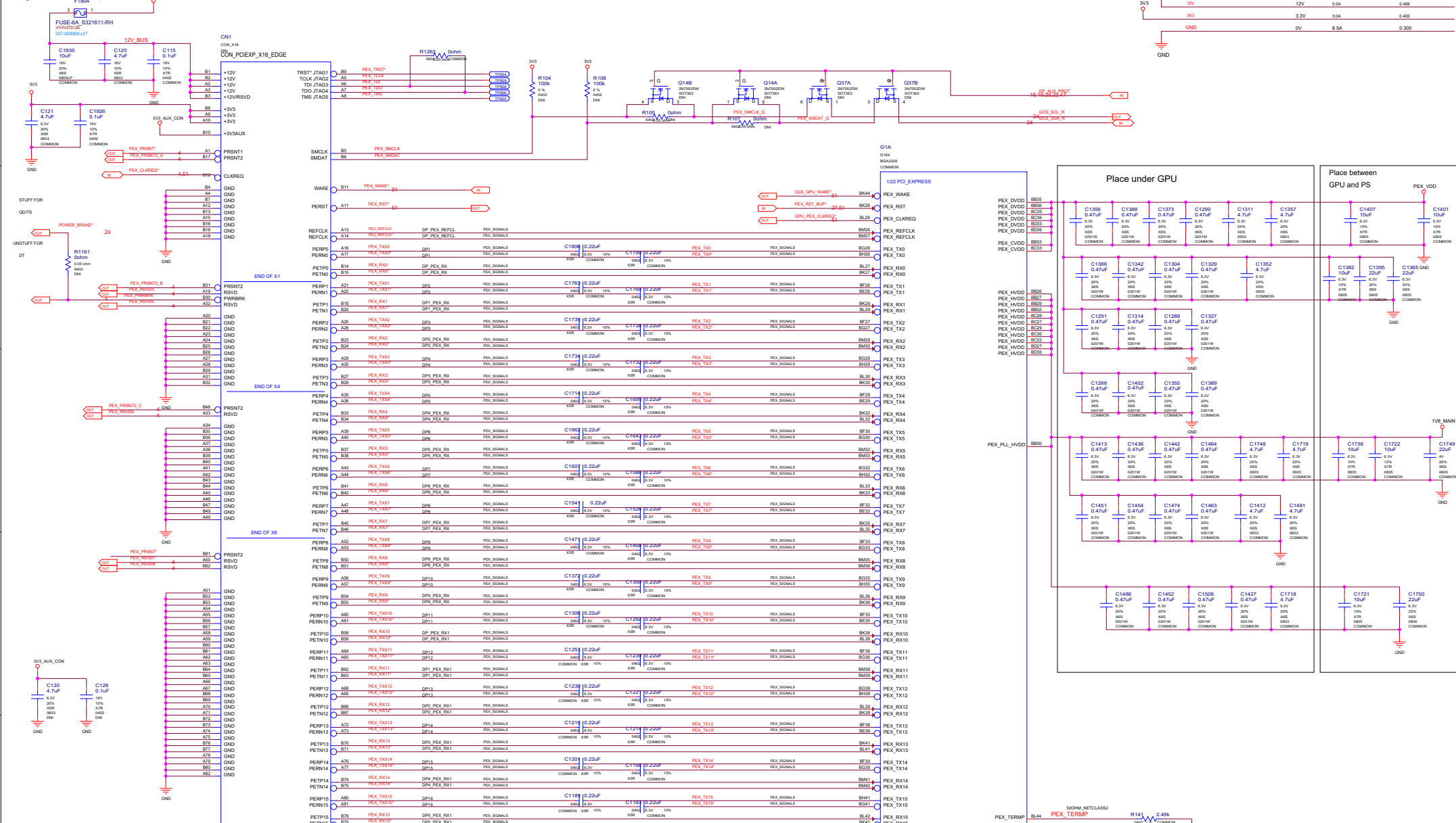
page 24: REMOVE GPIO29_IDLE_IN_SW
 remove GPIO9_INPUT_DYN_BAL2
 page 29: 12V_F RTD3 change to 12V_F
 page 30: 12V_F RTD3 change to 12V_F
 page 33: 12V_F RTD3 change to 12V_F
 移除保護線路
 page 39: remove INPUT SWITCH RTD3
 page 40: remove INPUT SWITCH RTD3 USB
 page 44: remove INA3221

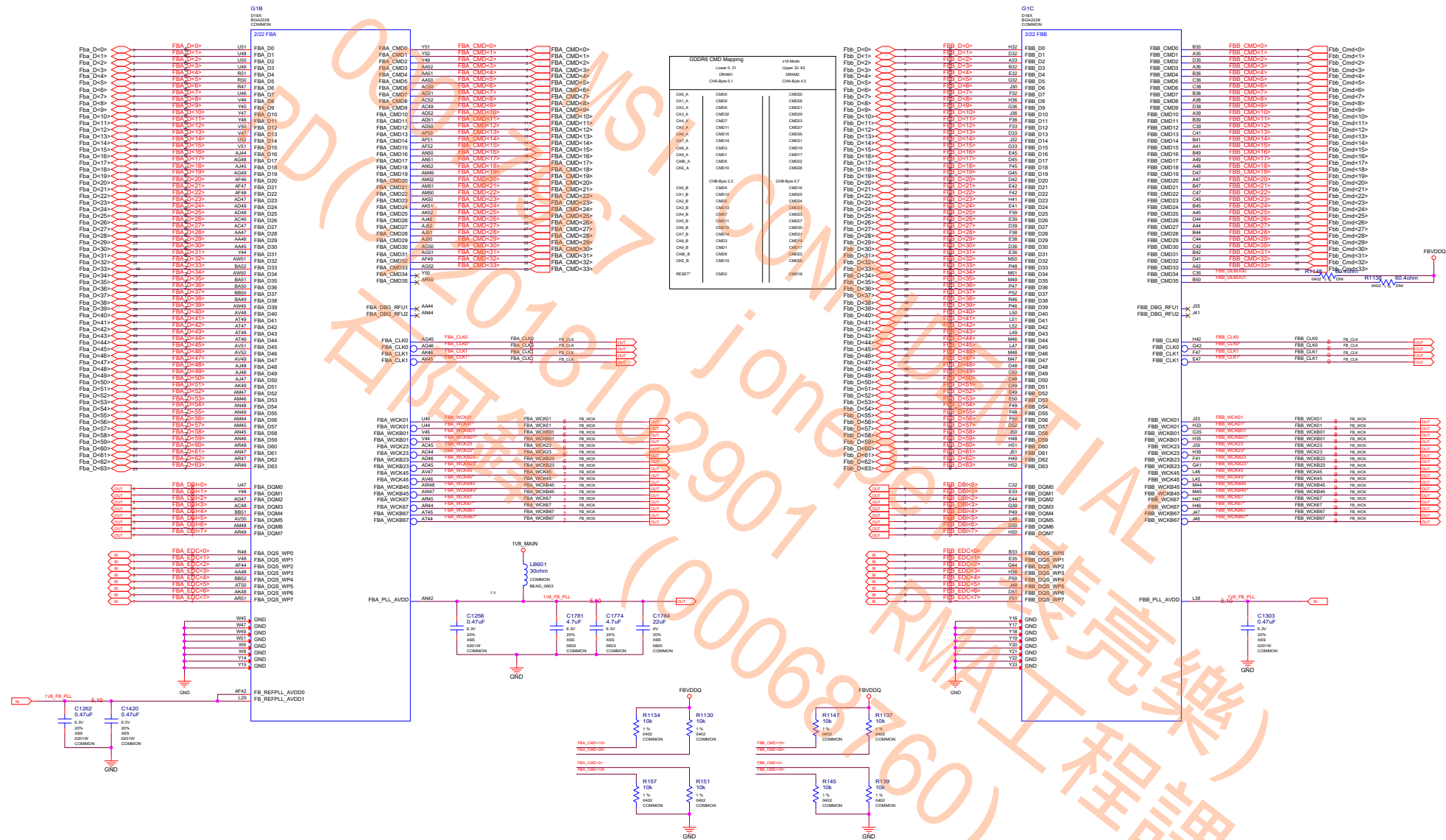
page 46: remove PFM_SKIP net
 remove PS_RTD3_12V_SW net
 page 47: remove PS_VMON_PGOOD net
 12V_F RTD3 change to 12V_F
 remove 3V3_PORT
 remove 3V3_RTD3 change to nv3v3
 page 48: remove OC_CRIT* NET from ina3221
 remove PS_VMON_PGOOD net
 page 49: PCIE Voltage Monitor1
 page 52: REMOVE VIN =>12V_PEX6_8_IN_OVRS

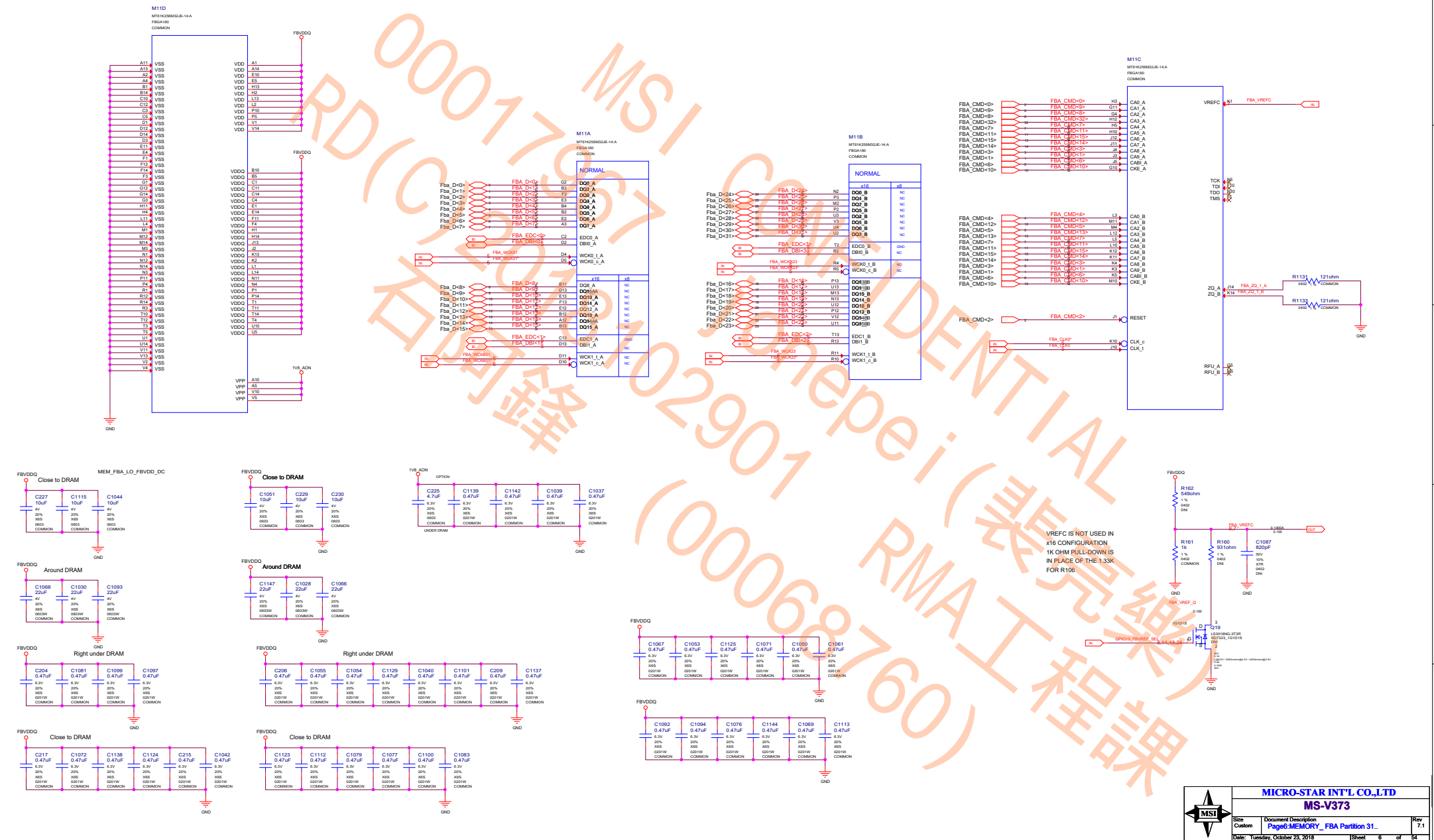
page 54: change GPU scrow holes to small size

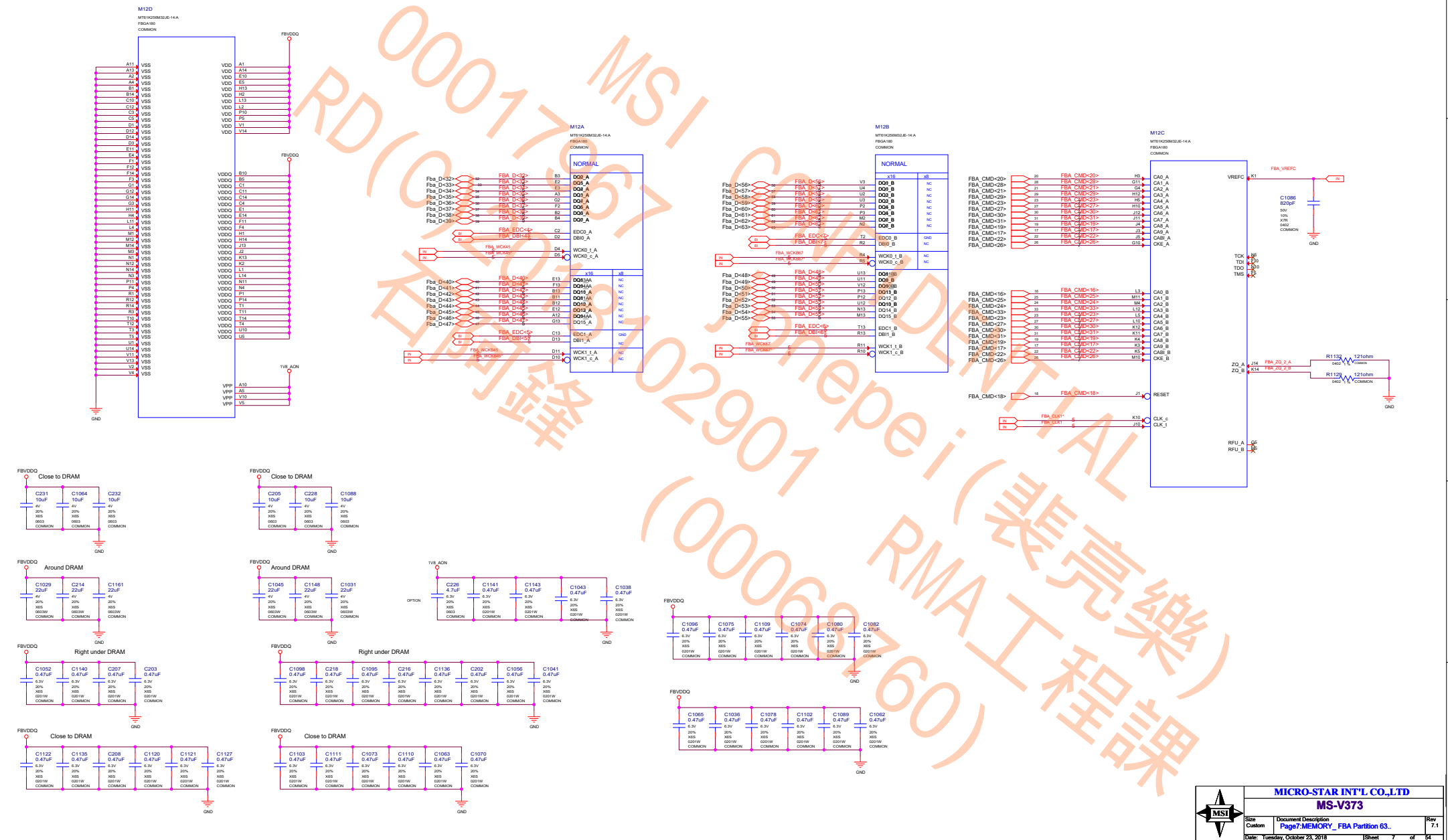


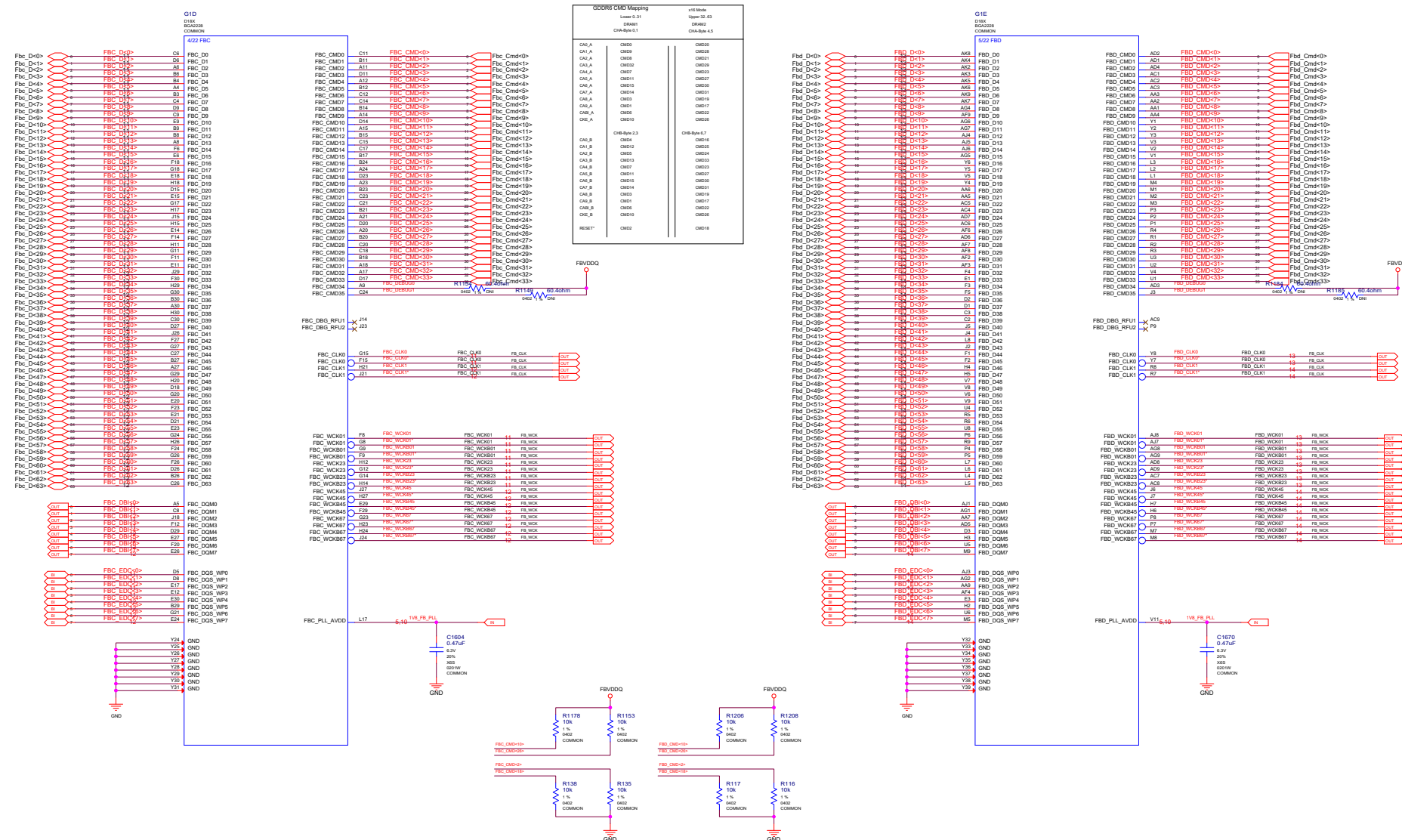
	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.406
3V3	3.3V	3.0A	0.400
GND	0V	8.5A	0.300

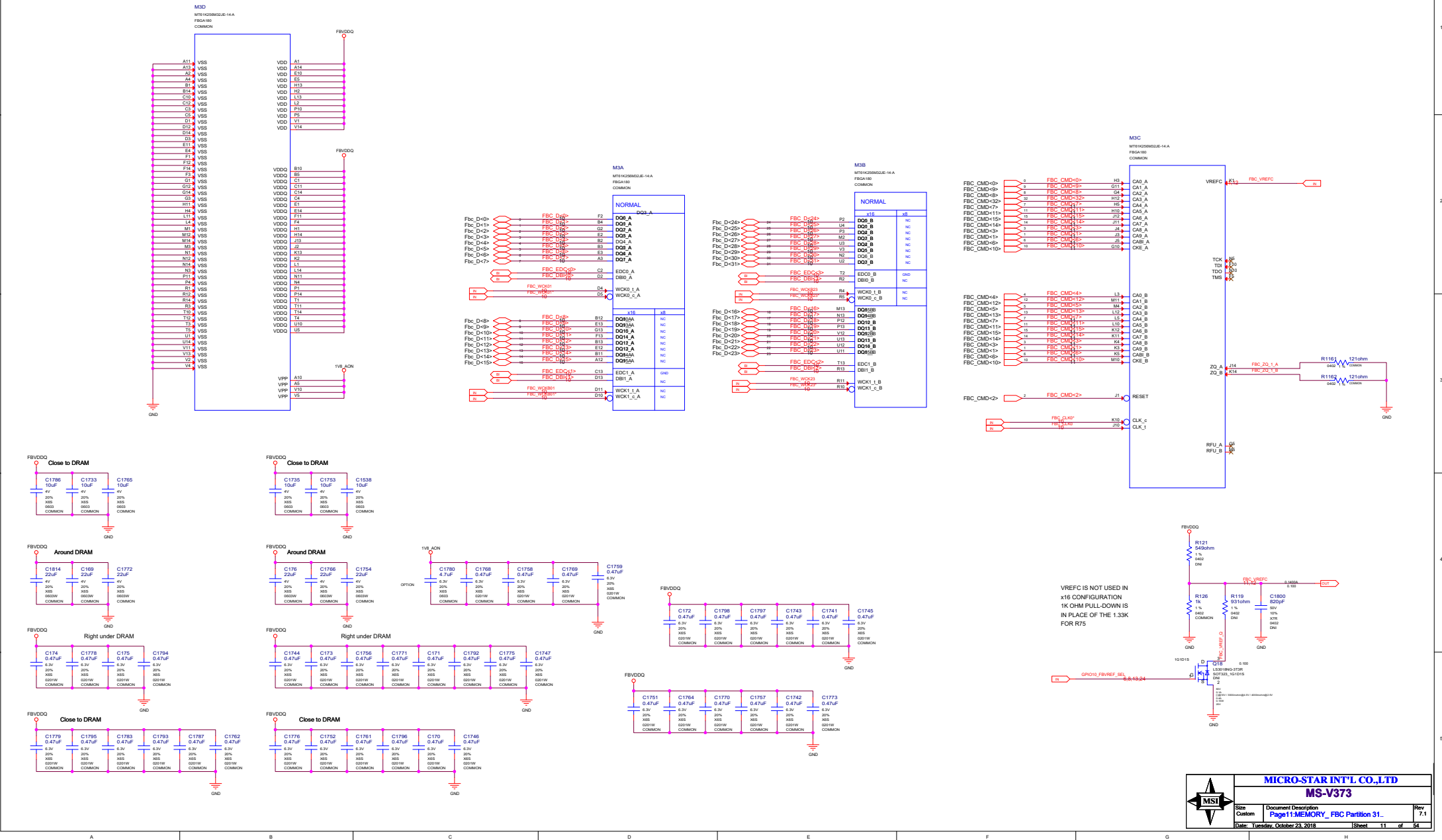


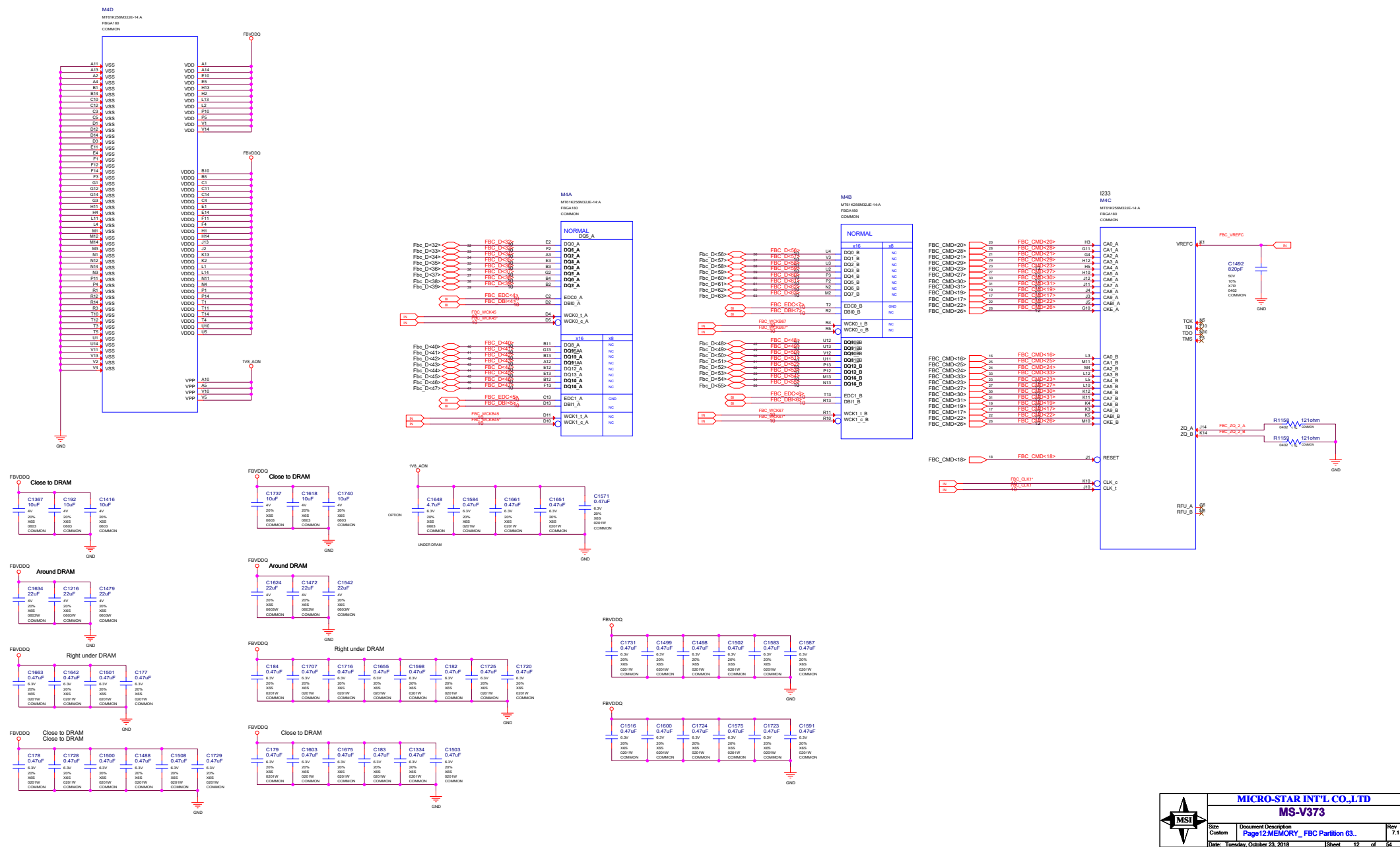


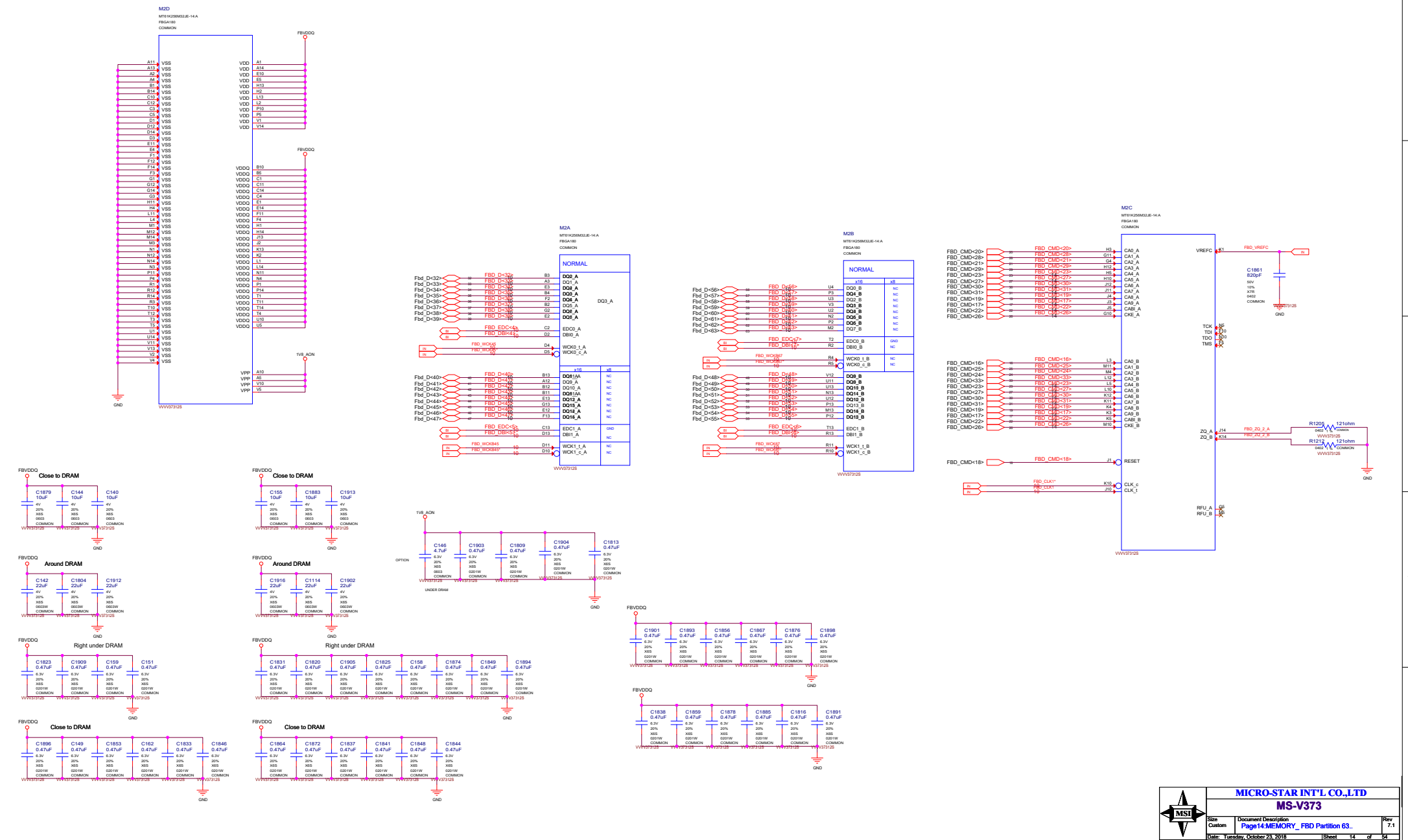


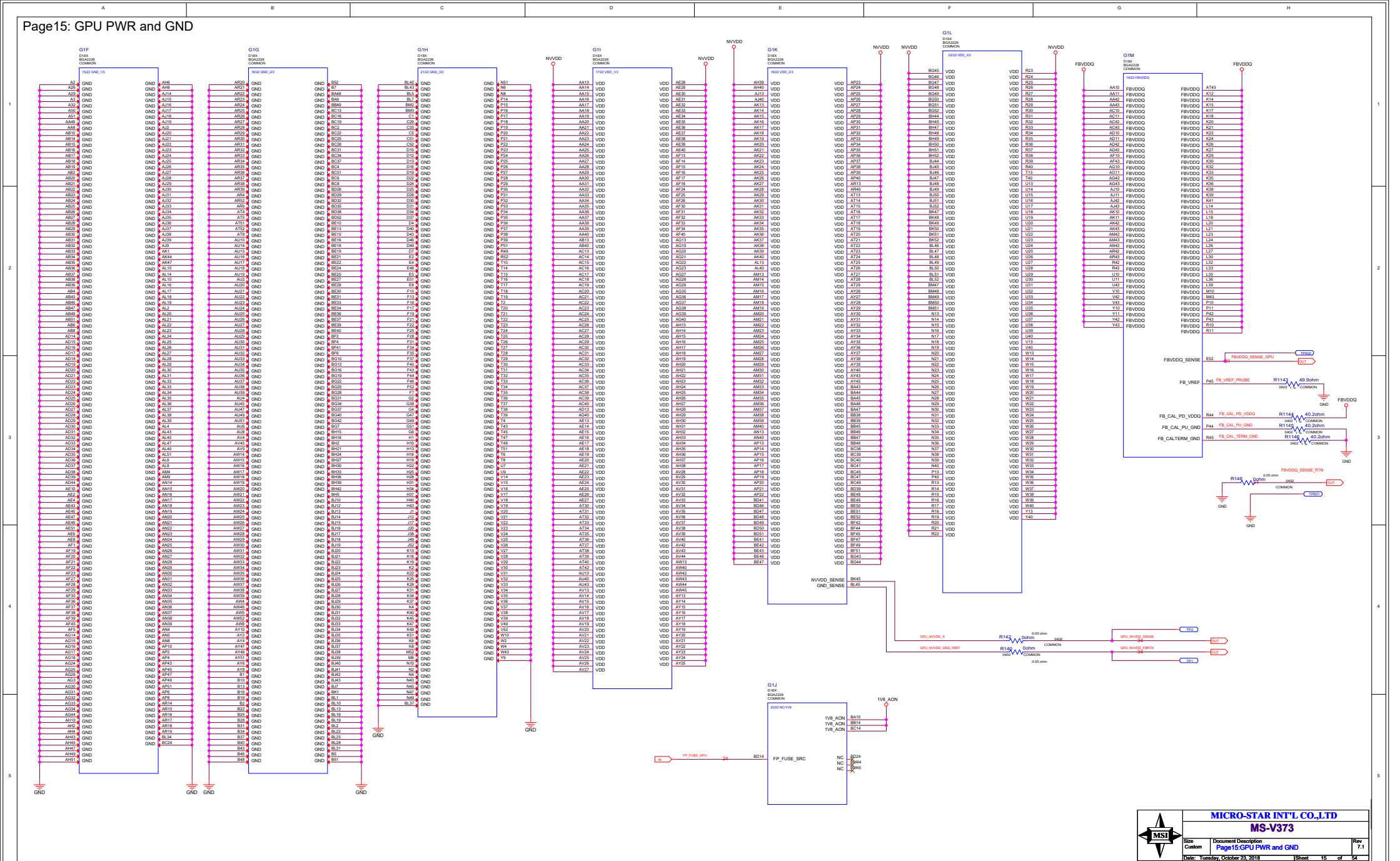


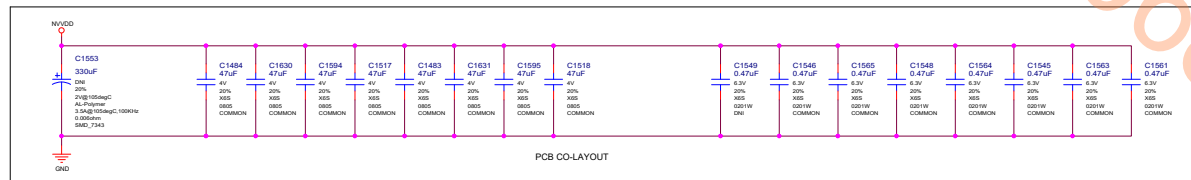
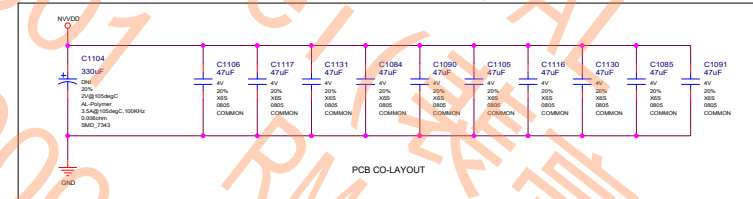
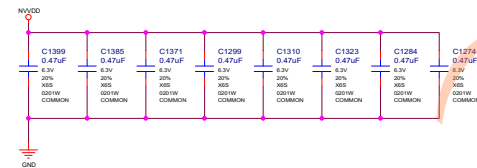
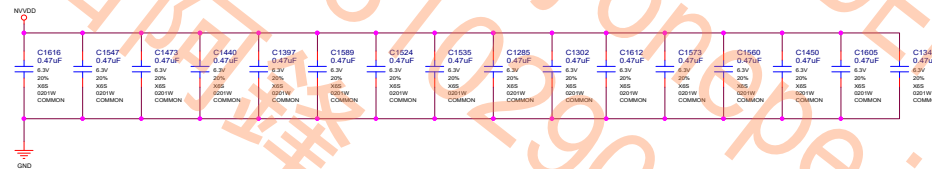
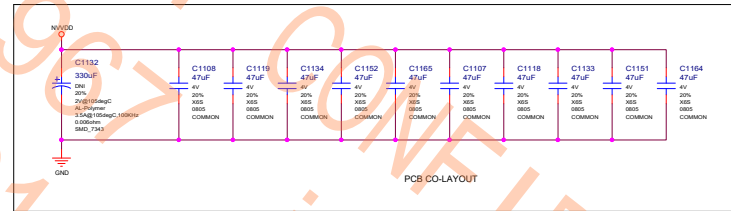
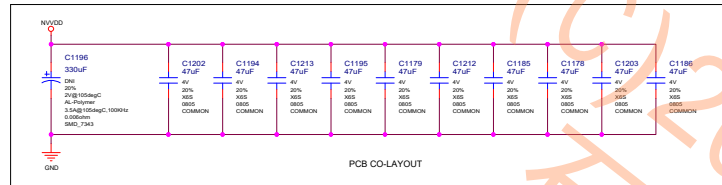
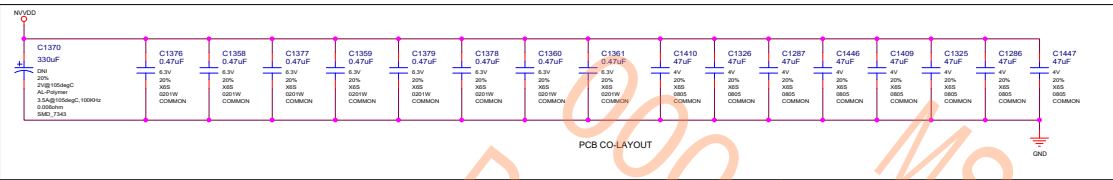


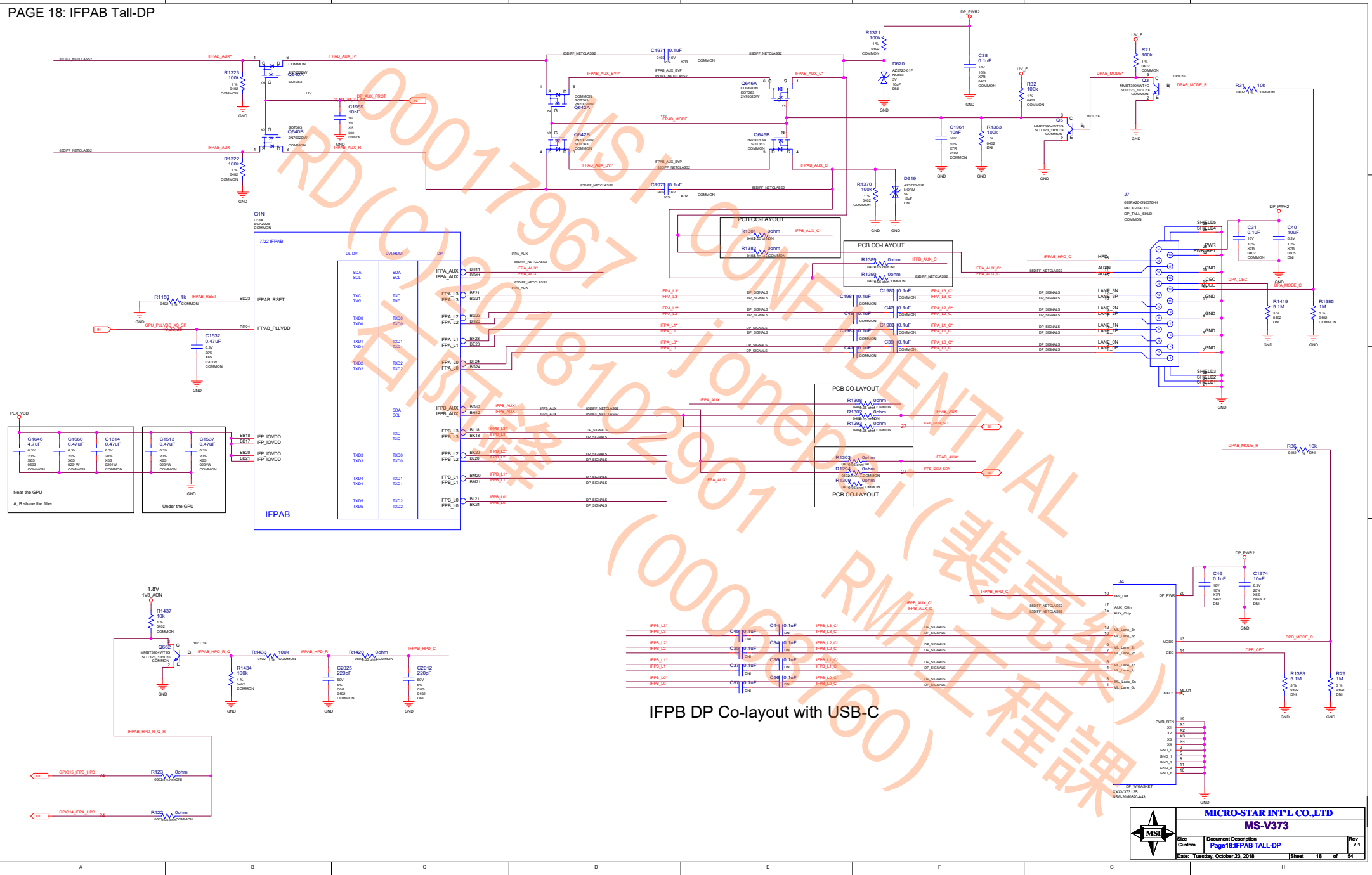


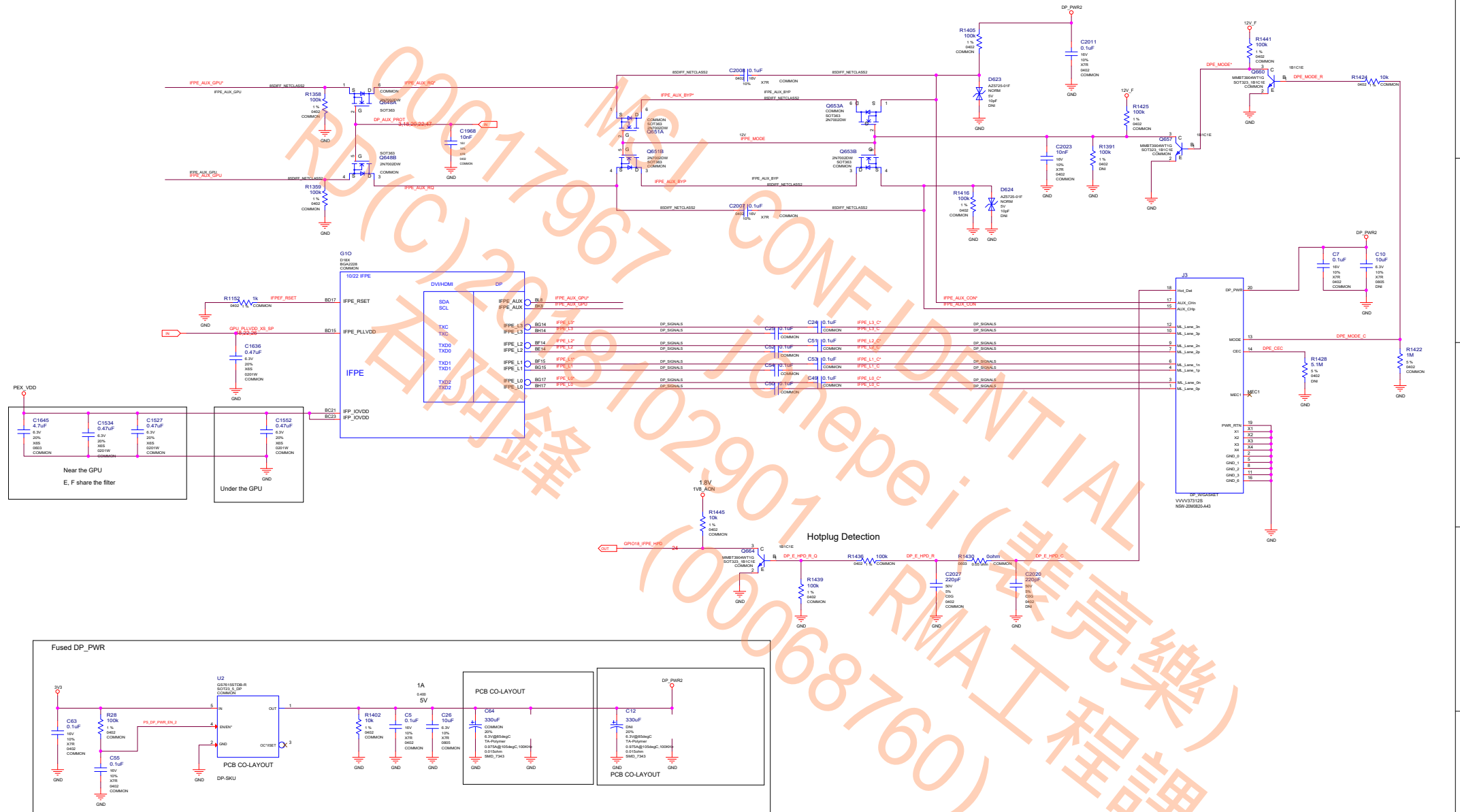




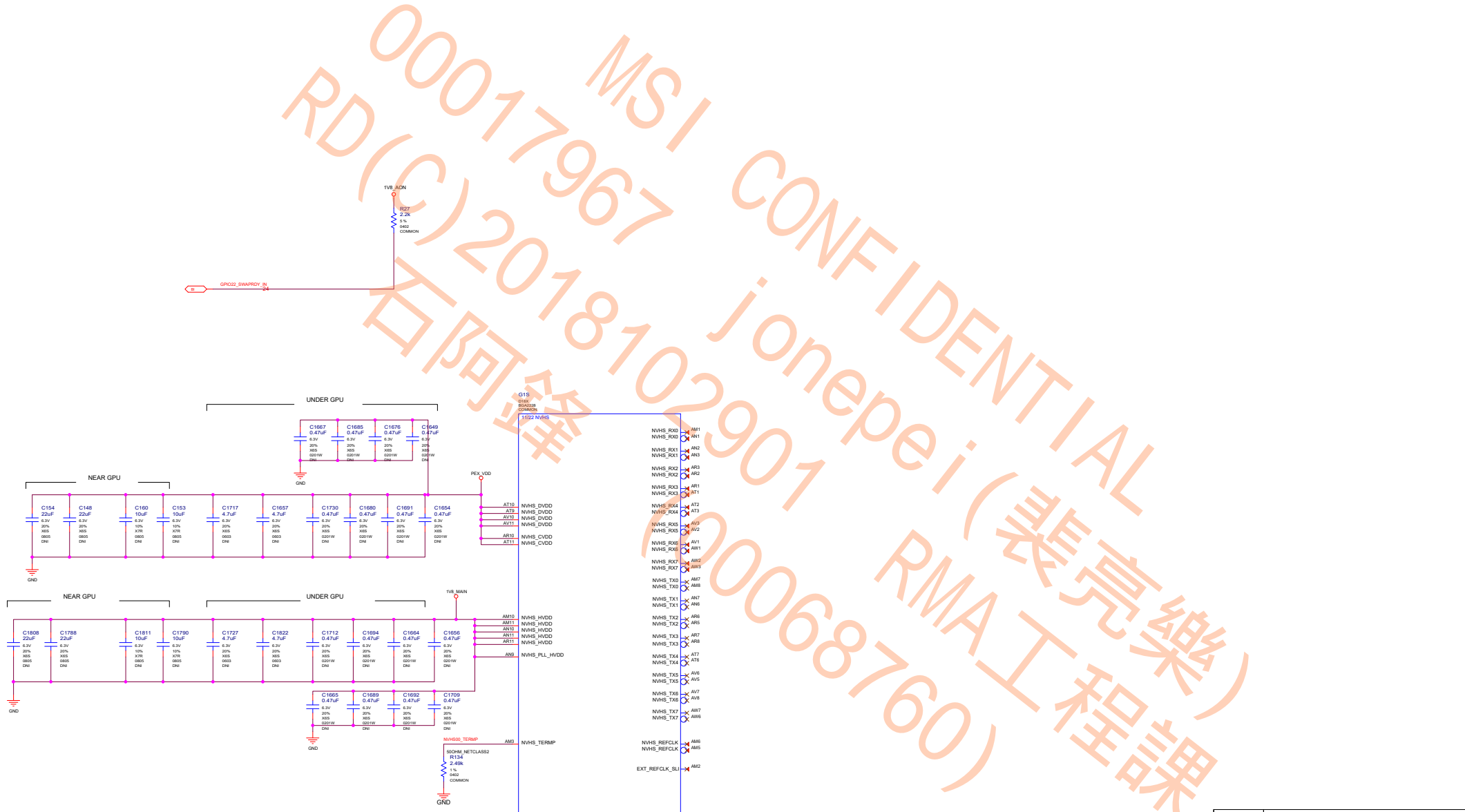


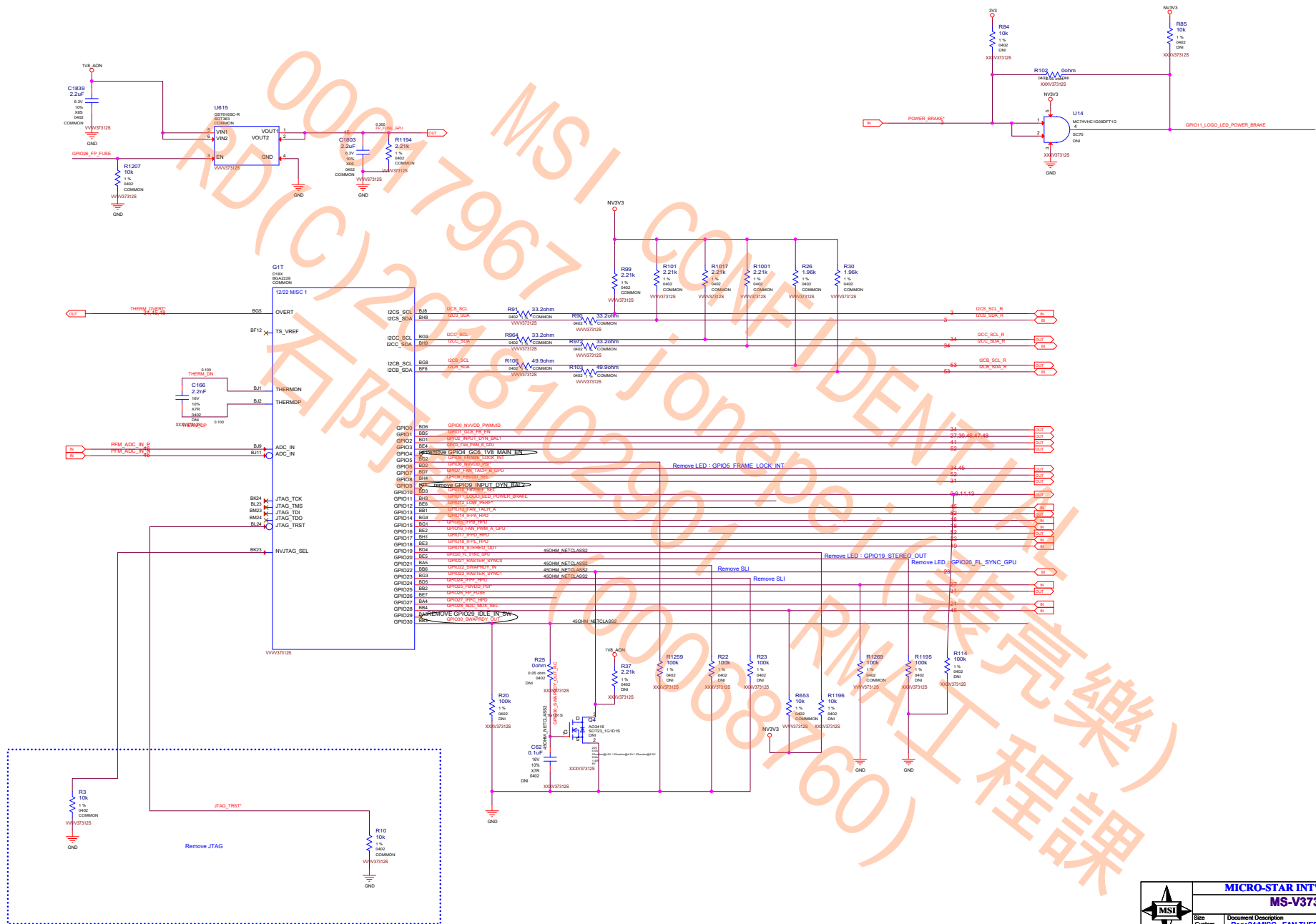












RAMCFG[4:0]			
00000	RAMCFG TBD		
00001	RAMCFG TBD		DEFAULT
00010	RAMCFG TBD		
00011	RAMCFG TBD		
00110	RAMCFG TBD		
00111	RAMCFG TBD		

DUMMY[2:0].FS_OVERT			
	1:ENABLE 0:DISABLE		
XXX1	FS_OVERT ENABLE		DEFAULT
XXX0	FS_OVERT DISABLE		

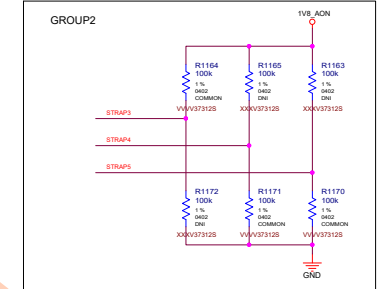
SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
1	1	1	1	
1	1	1	0	1:SMB_ALT_ADDR ENABLE 0:SMB_ALT_ADDR DISABLE
1	1	0	1	
1	1	0	0	1:DEVID_SEL REBRAND 0:DEVID_SEL ORIGINAL
1	0	1	1	1:PCIE_CFG LOW POWER 0:PCIE_CFG HIGH POWER
1	0	0	1	1:VGA_DEVICE ENABLE 0:VGA_DEVICE DISABLE
1	0	0	0	
0	1	1	1	
0	1	1	0	
0	1	0	1	
0	1	0	0	
0	0	1	1	
0	0	1	0	
0	0	0	1	
0	0	0	0	

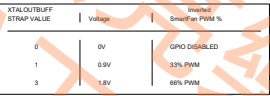
RAMCFG[4:0]		DENSITY	WIDTH	VENDOR
00000		8Gb	256-bit	Samsung
00001		8Gb	256-bit	Micron
00010		8Gb	256-bit	Hynix
00110		16Gb	256-bit	Samsung
00111		16Gb	256-bit	Samsung

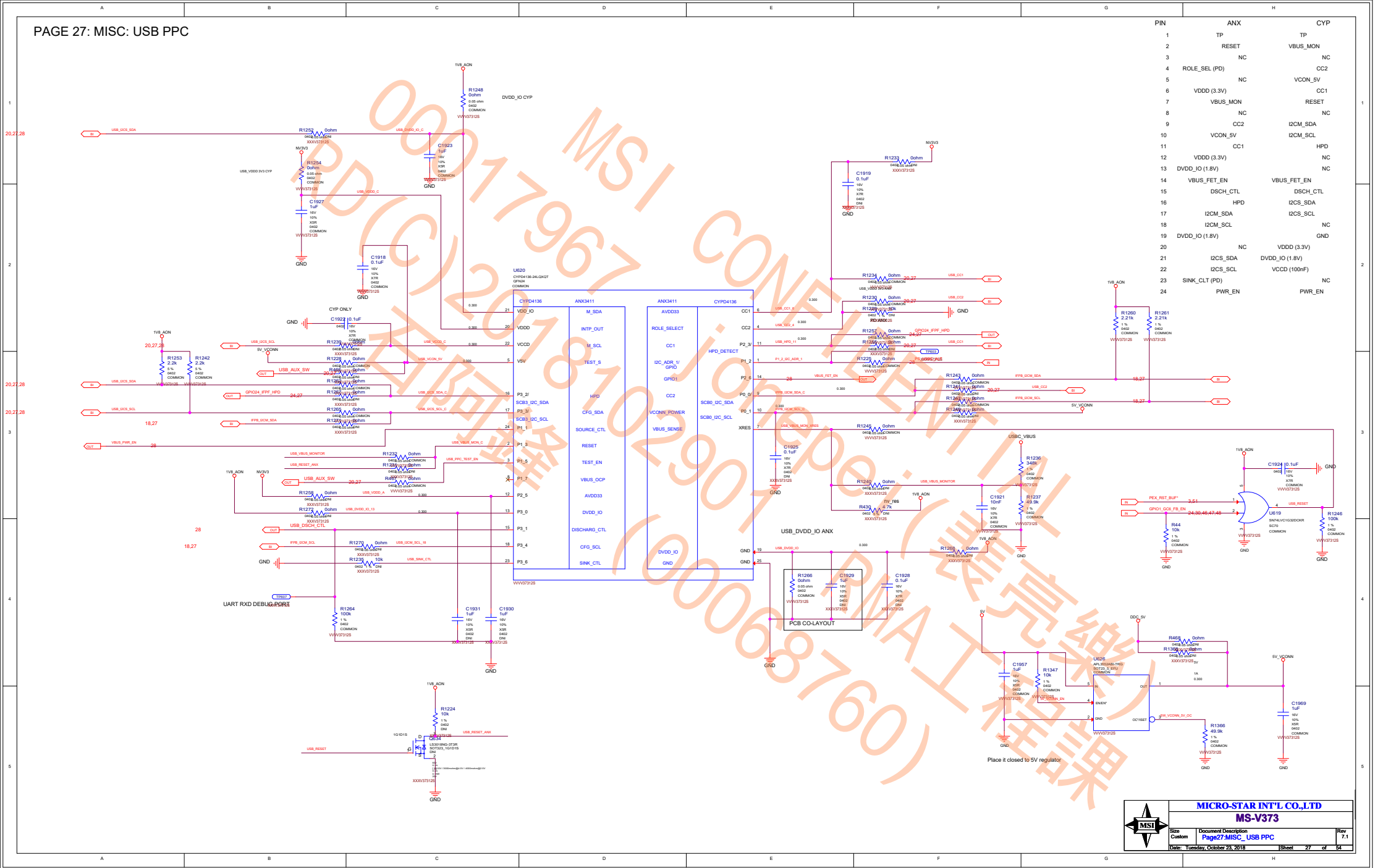
SMB_ALT_ADDR		DEVID_SEL	PCIE_CFG	VGA_DEVICE	
1	1	1	1	1	
1	1	1	0	0	1:SMB_ALT_ADDR ENABLE 0:SMB_ALT_ADDR DISABLE
1	1	0	1	1	
1	1	0	0	0	1:DEVID_SEL REBRAND 0:DEVID_SEL ORIGINAL
1	0	1	1	1	1:PCIE_CFG LOW POWER 0:PCIE_CFG HIGH POWER
1	0	0	1	1	1:VGA_DEVICE ENABLE 0:VGA_DEVICE DISABLE
1	0	0	0	0	
0	1	1	1	1	
0	1	1	0	0	
0	1	0	1	1	
0	1	0	0	0	
0	0	1	1	1	
0	0	1	0	0	
0	0	0	1	1	
0	0	0	0	0	

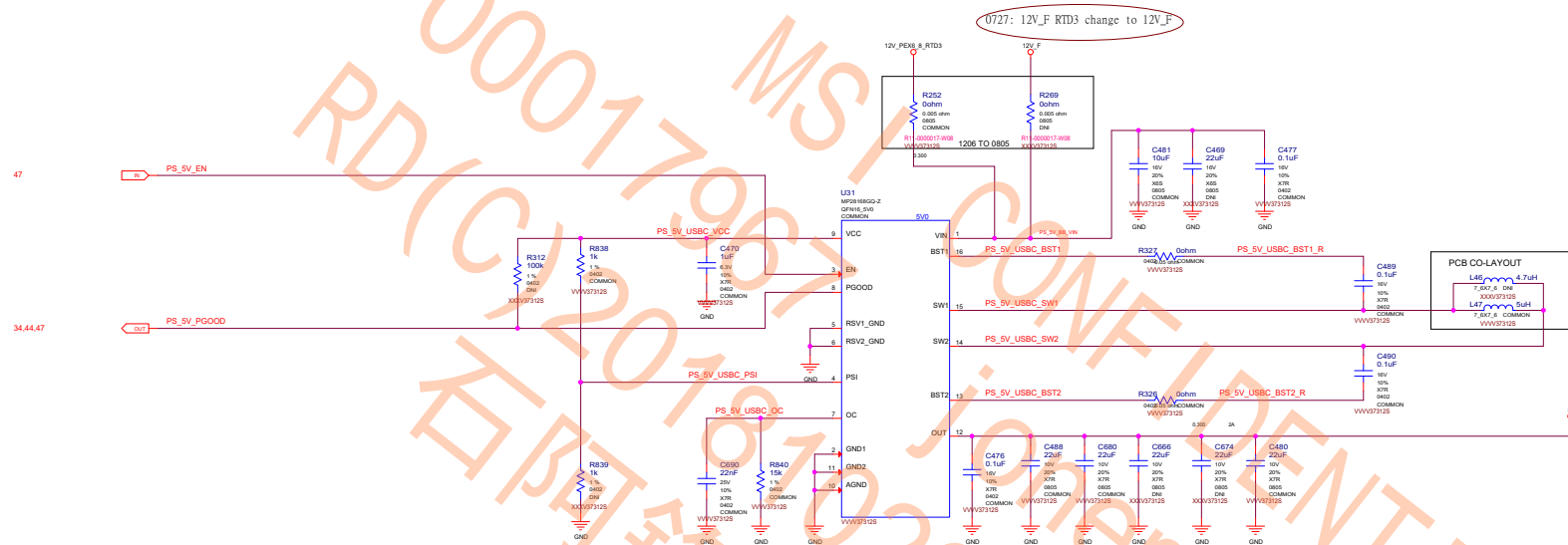
SMB_ALT_ADDR		DEVID_SEL	PCIE_CFG	VGA_DEVICE	
1	1	1	1	1	
1	1	1	0	0	1:SMB_ALT_ADDR ENABLE 0:SMB_ALT_ADDR DISABLE
1	1	0	1	1	
1	1	0	0	0	1:DEVID_SEL REBRAND 0:DEVID_SEL ORIGINAL
1	0	1	1	1	1:PCIE_CFG LOW POWER 0:PCIE_CFG HIGH POWER
1	0	0	1	1	1:VGA_DEVICE ENABLE 0:VGA_DEVICE DISABLE
1	0	0	0	0	
0	1	1	1	1	
0	1	1	0	0	
0	1	0	1	1	
0	1	0	0	0	
0	0	1	1	1	
0	0	1	0	0	
0	0	0	1	1	
0	0	0	0	0	

SMB_ALT_ADDR		DEVID_SEL	PCIE_CFG	VGA_DEVICE	
1	1	1	1	1	
1	1	1	0	0	1:SMB_ALT_ADDR ENABLE 0:SMB_ALT_ADDR DISABLE
1	1	0	1	1	
1	1	0	0	0	1:DEVID_SEL REBRAND 0:DEVID_SEL ORIGINAL
1	0	1	1	1	1:PCIE_CFG LOW POWER 0:PCIE_CFG HIGH POWER
1	0	0	1	1	1:VGA_DEVICE ENABLE 0:VGA_DEVICE DISABLE
1	0	0	0	0	
0	1	1	1	1	
0	1	1	0	0	
0	1	0	1	1	
0	1	0	0	0	
0	0	1	1	1	
0	0	1	0	0	
0	0	0	1	1	
0	0	0	0	0	









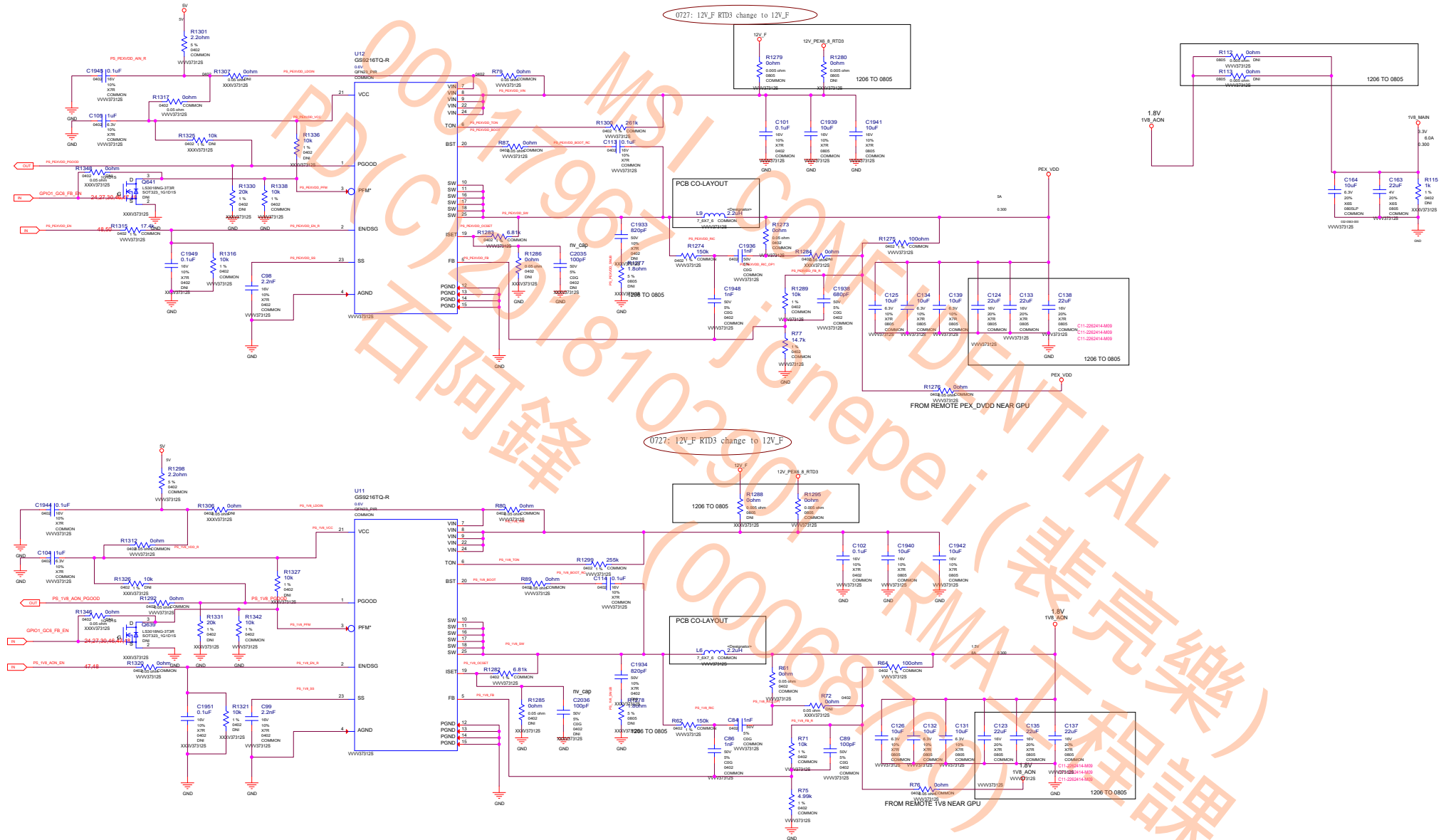
remove



MICRO-STAR INT'L CO.,LTD

MS-V373


Size Custom	Document Description Page29:PS_5V, 5V BACKUP	Rev 7.1
Date: Tuesday, October 23, 2018		Sheet 29 of 54



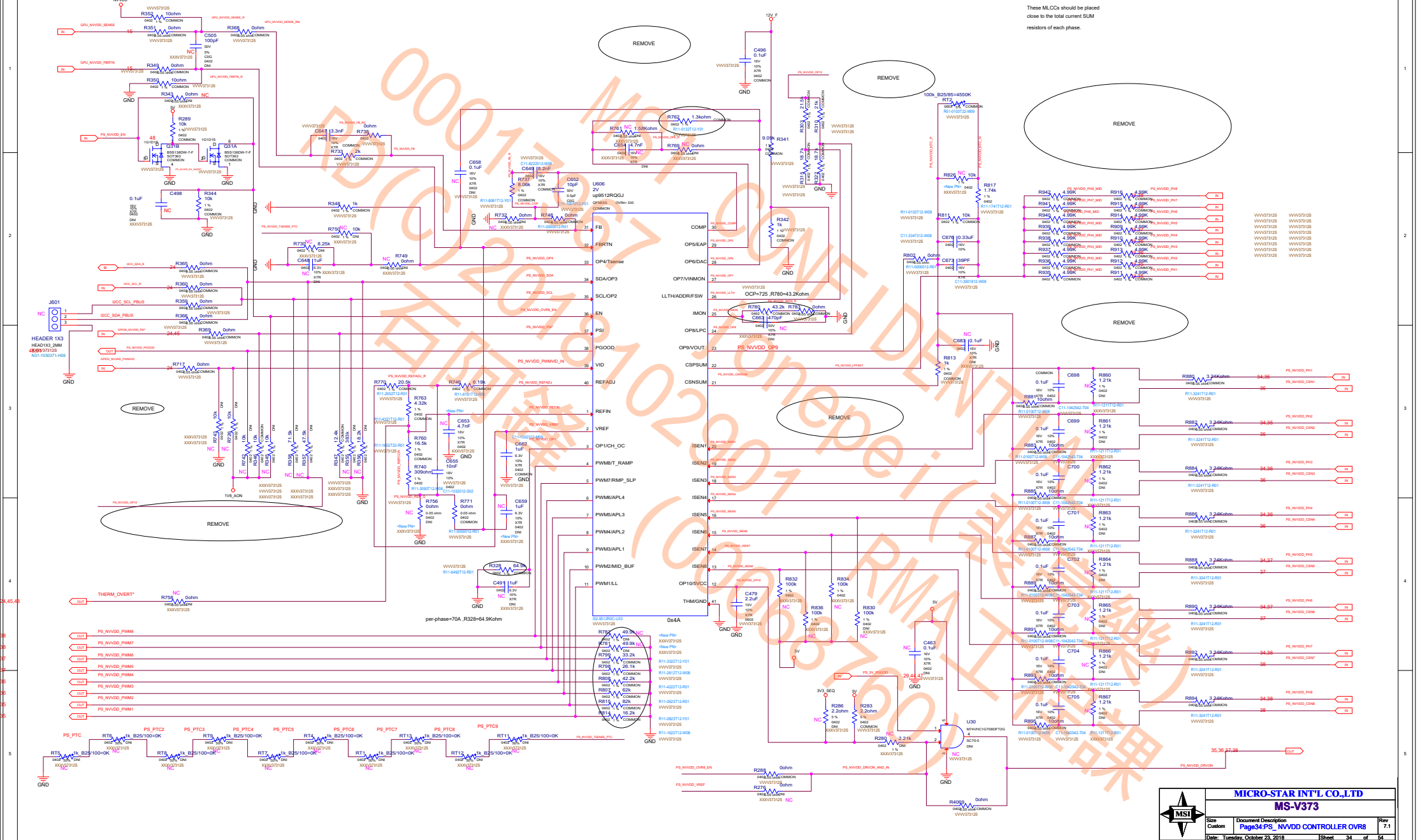
MICRO-STAR INT'L CO.,LTD
MS-V373

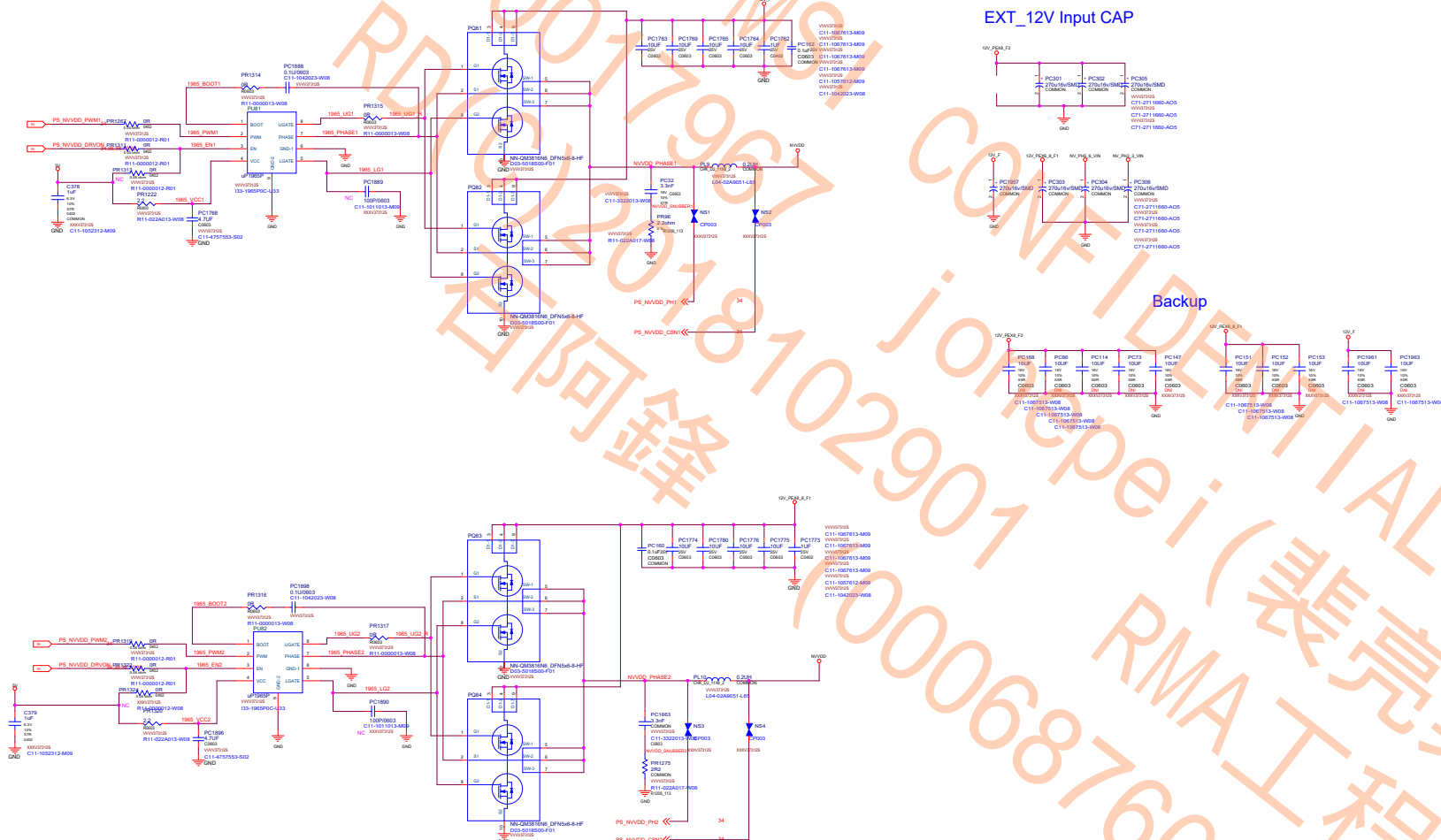
Size Custom	Document Description Page30:PS_PEXVDD, 1V8	Rev 7.1
Date: Tuesday, October 23, 2018		Sheet 30 of 54

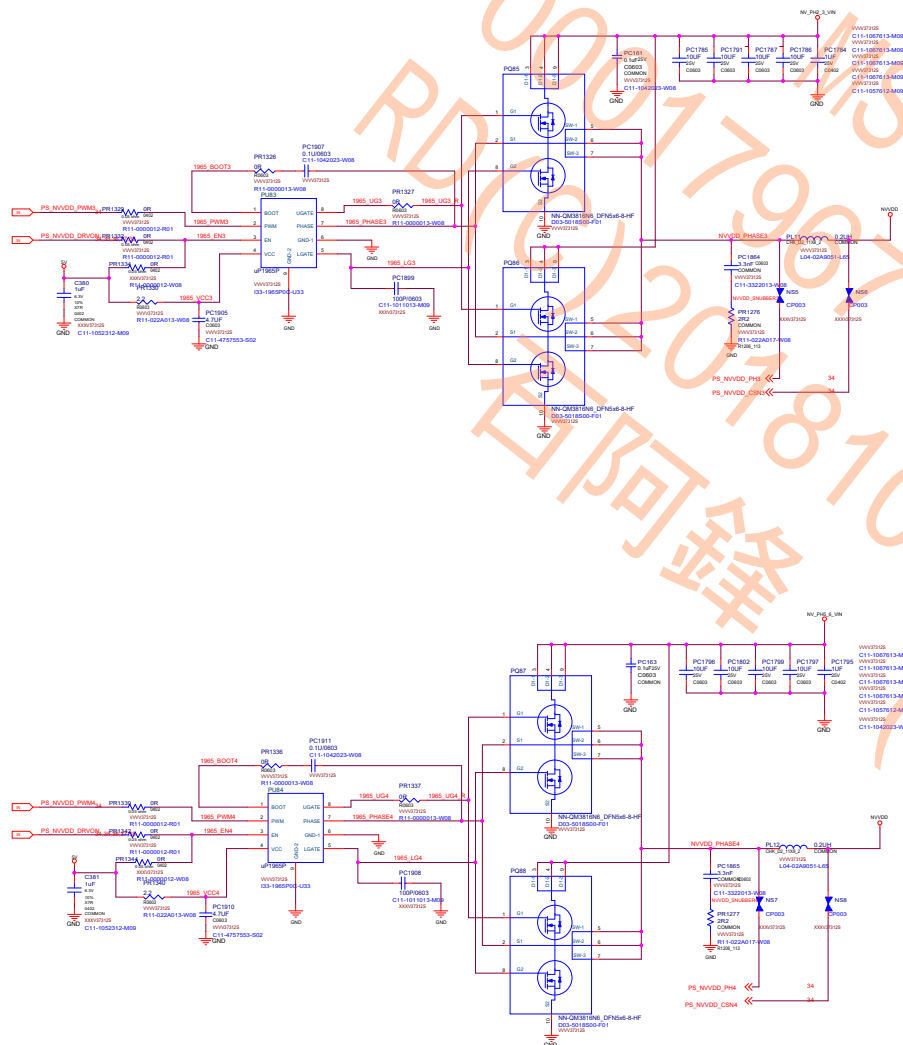
MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2018102901 RMA工程課
石阿鋒 (00068760)

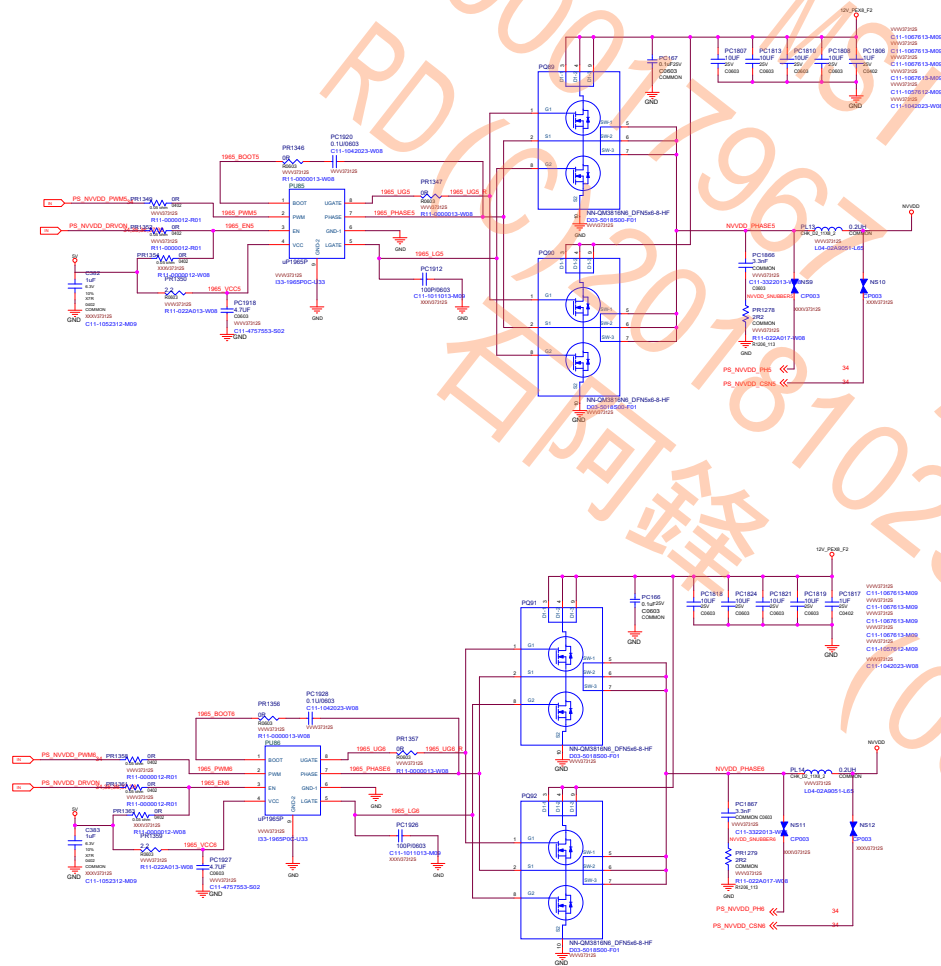
	MICRO-STAR INT'L CO.,LTD		
	MS-V373		
	Size	Document Description	Rev
	Custom	Page32:PS_FBVD Controller OVR3	7.1
Date: Tuesday, October 23, 2018		Sheet 32 of 54	

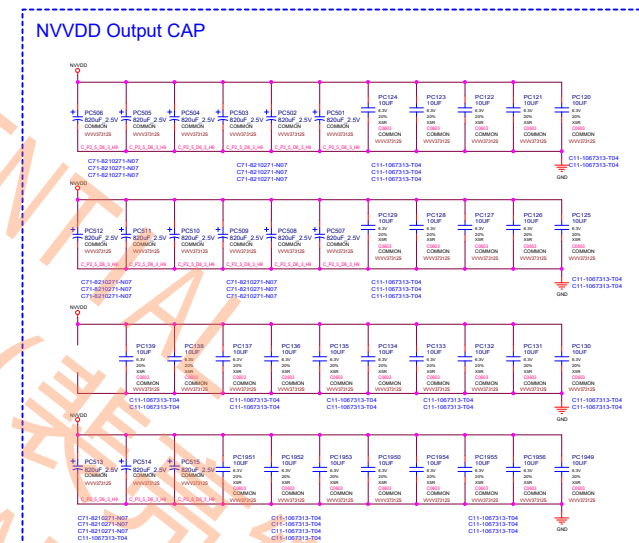
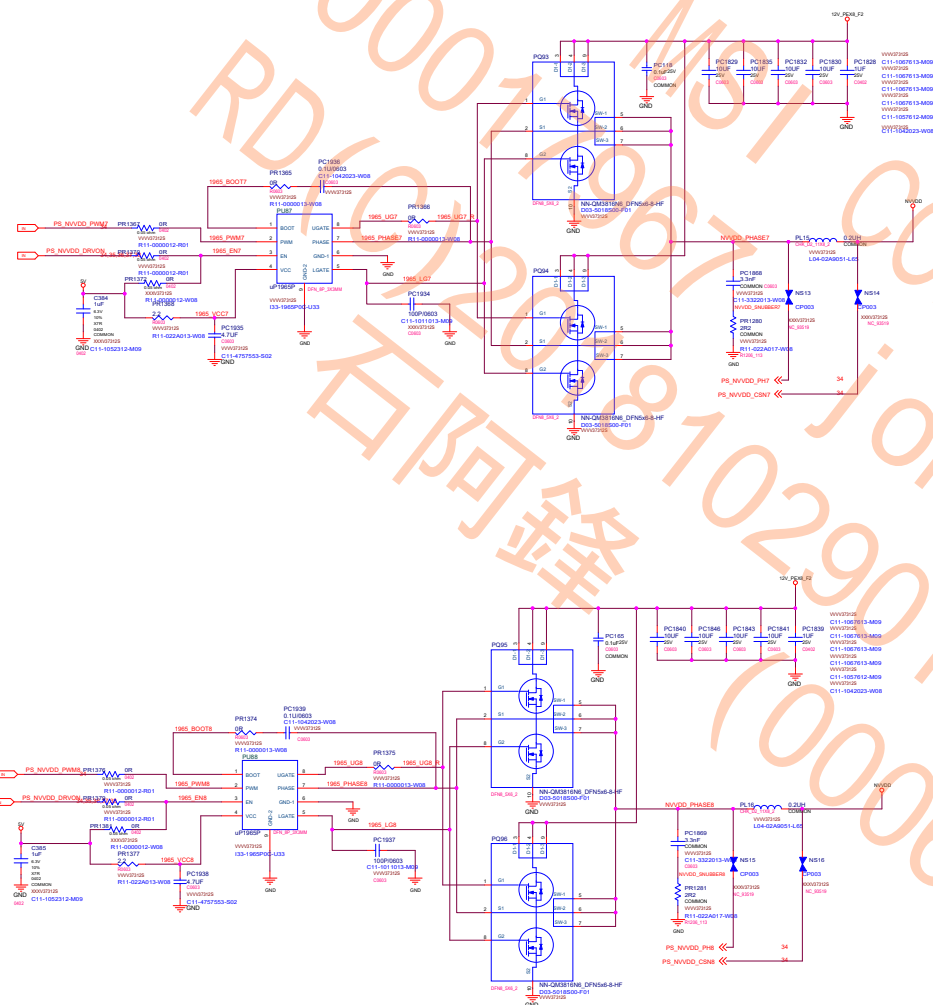








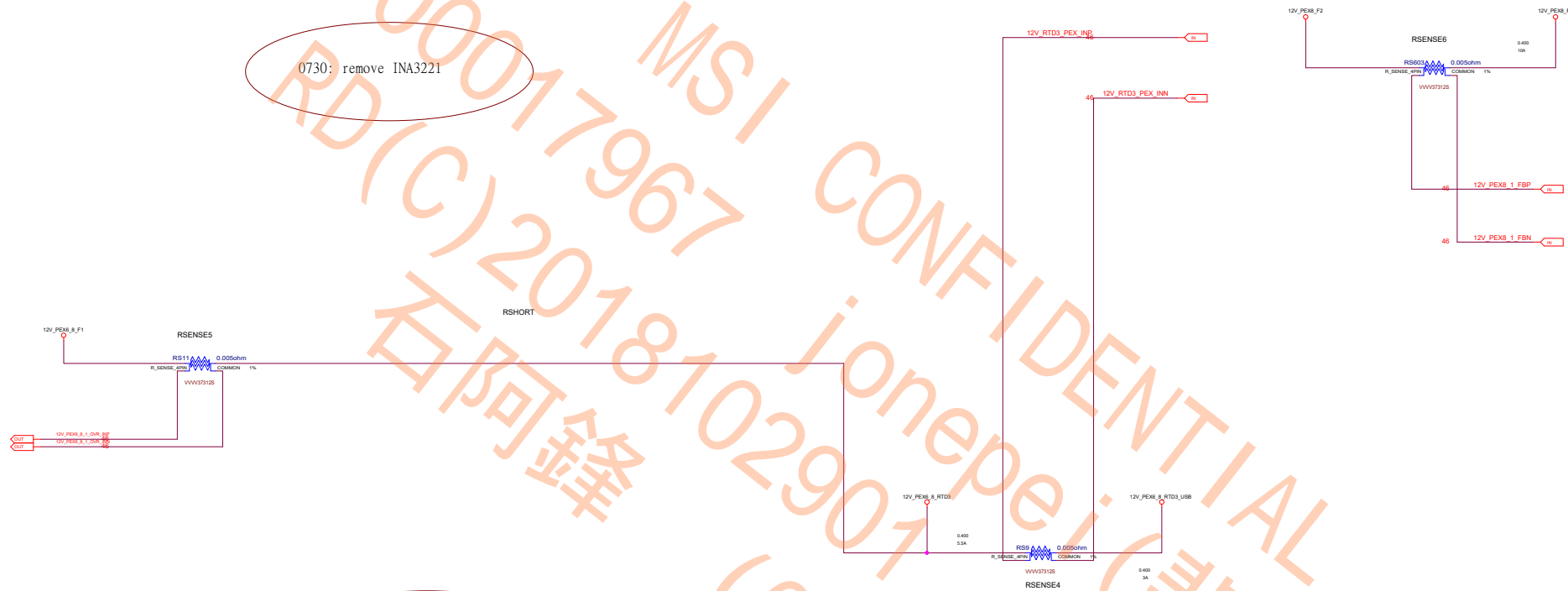




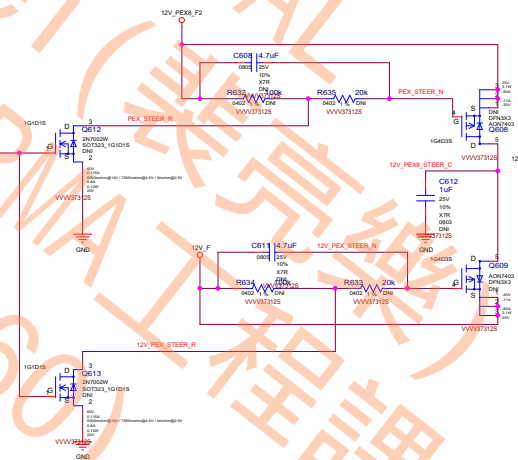
AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

0727: remove



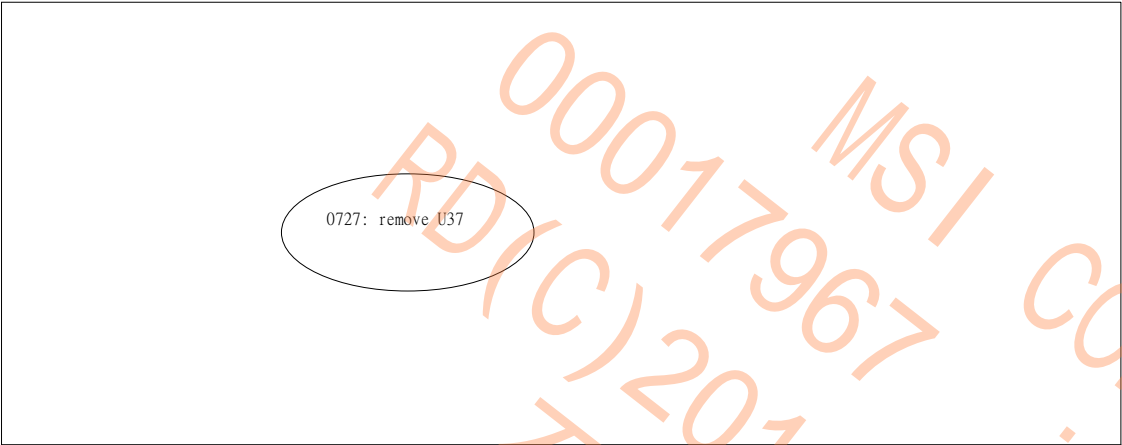




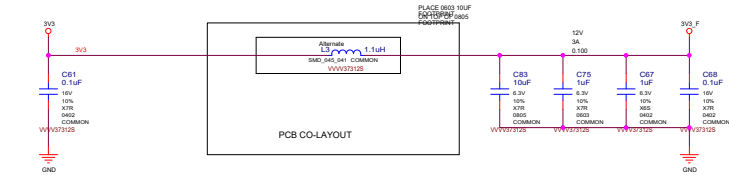
MICRO-STAR INT'L CO.,LTD			
MS-V373			
Size Custom	Document Description Page42:PS_12V CURRENT STEERING		Rev 7.1
Date: Tuesday, October 23, 2018		Sheet 42 of	54

MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2018102901 RMA工程課
石阿鋒 (00068760)

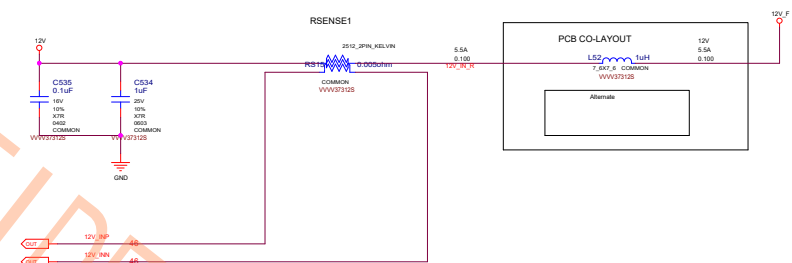
MICRO-STAR INT'L CO.,LTD		
MS-V373		
Size	Document Description	Rev
Custom	Page43.PS_VR THERMAL PROTECTION	7.1
Date: Tuesday, October 23, 2018		Sheet 43 of 54



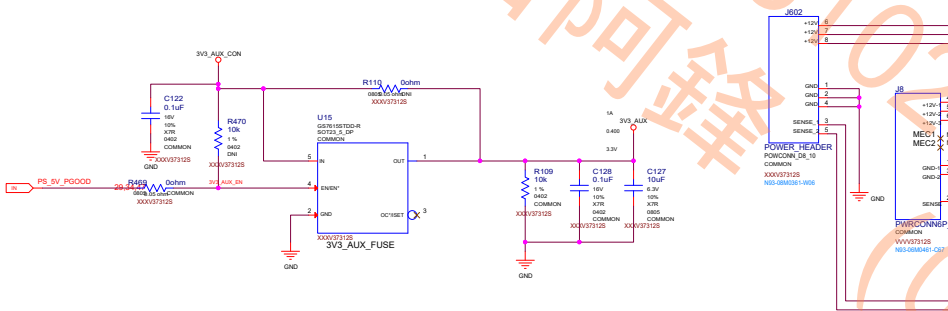
PEX 3V3 INPUT - 10W



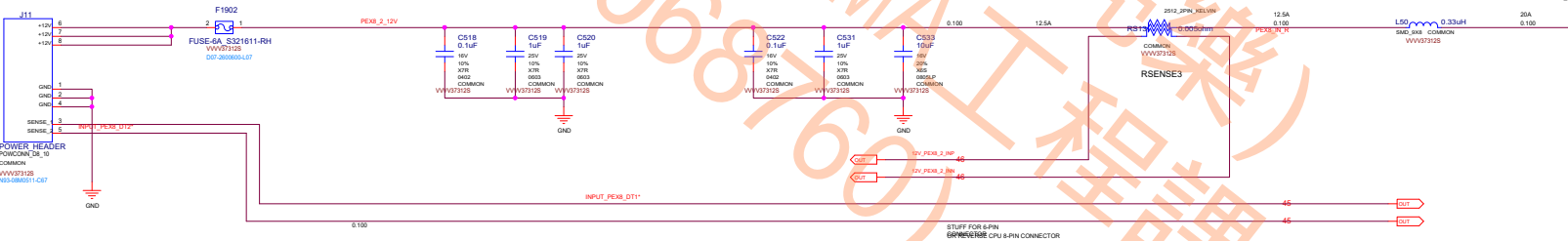
PEX_12V INPUT - 66W

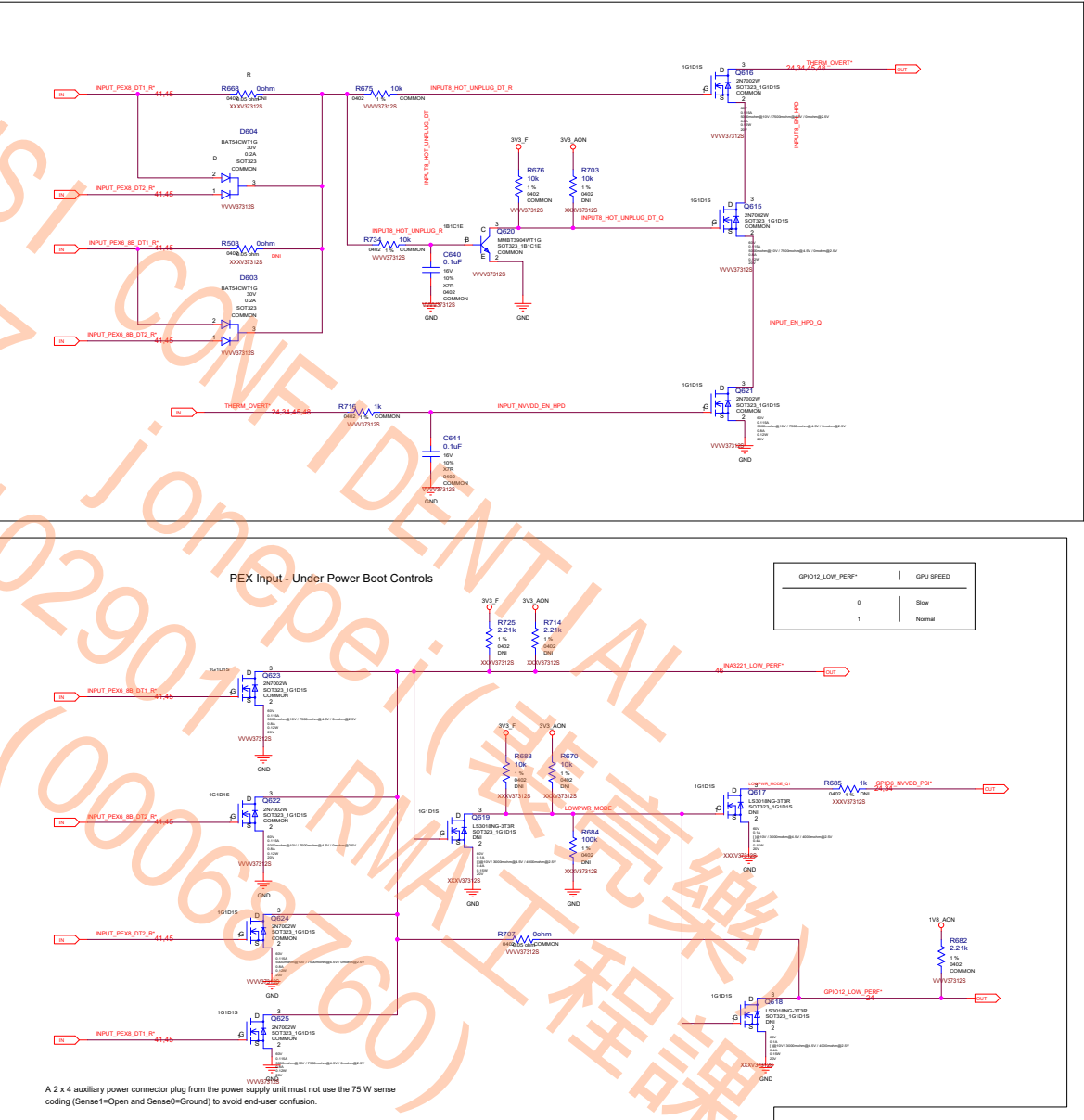
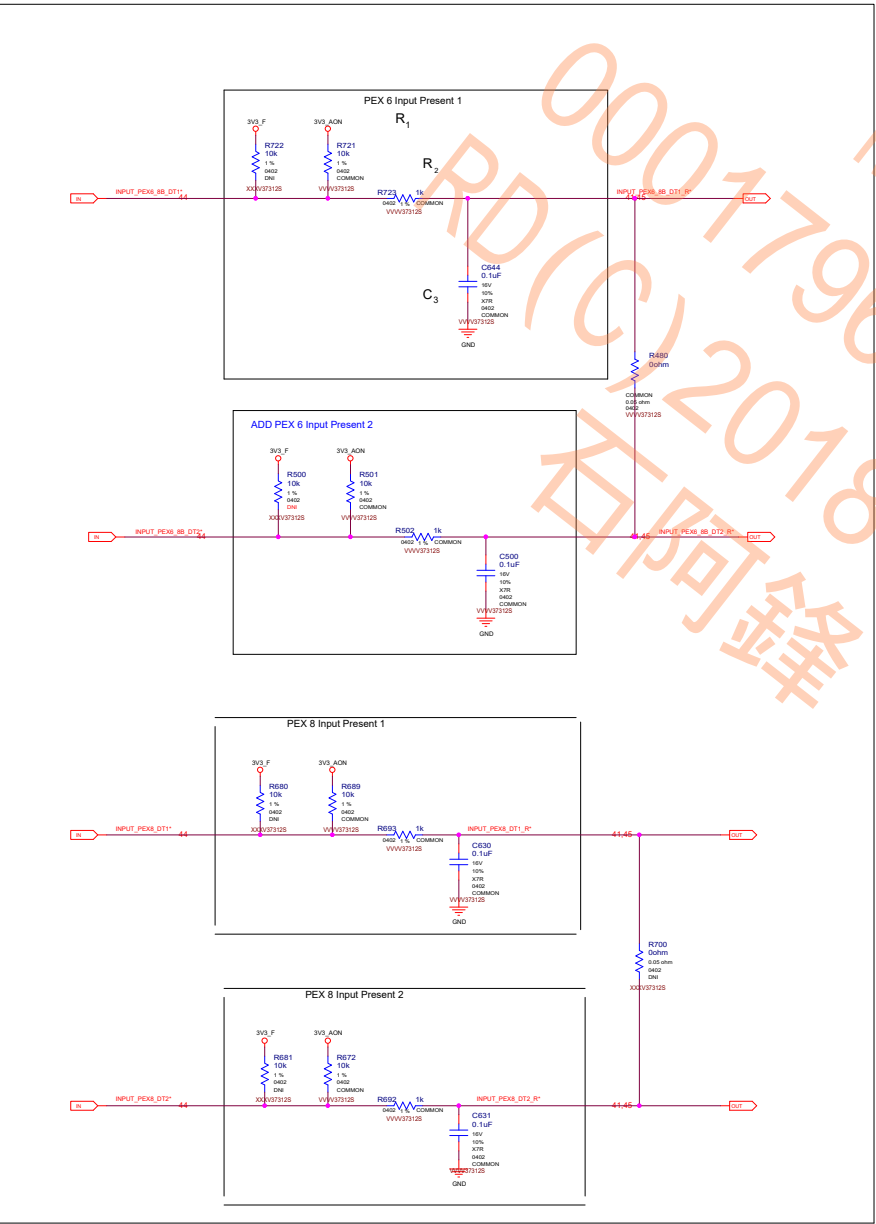


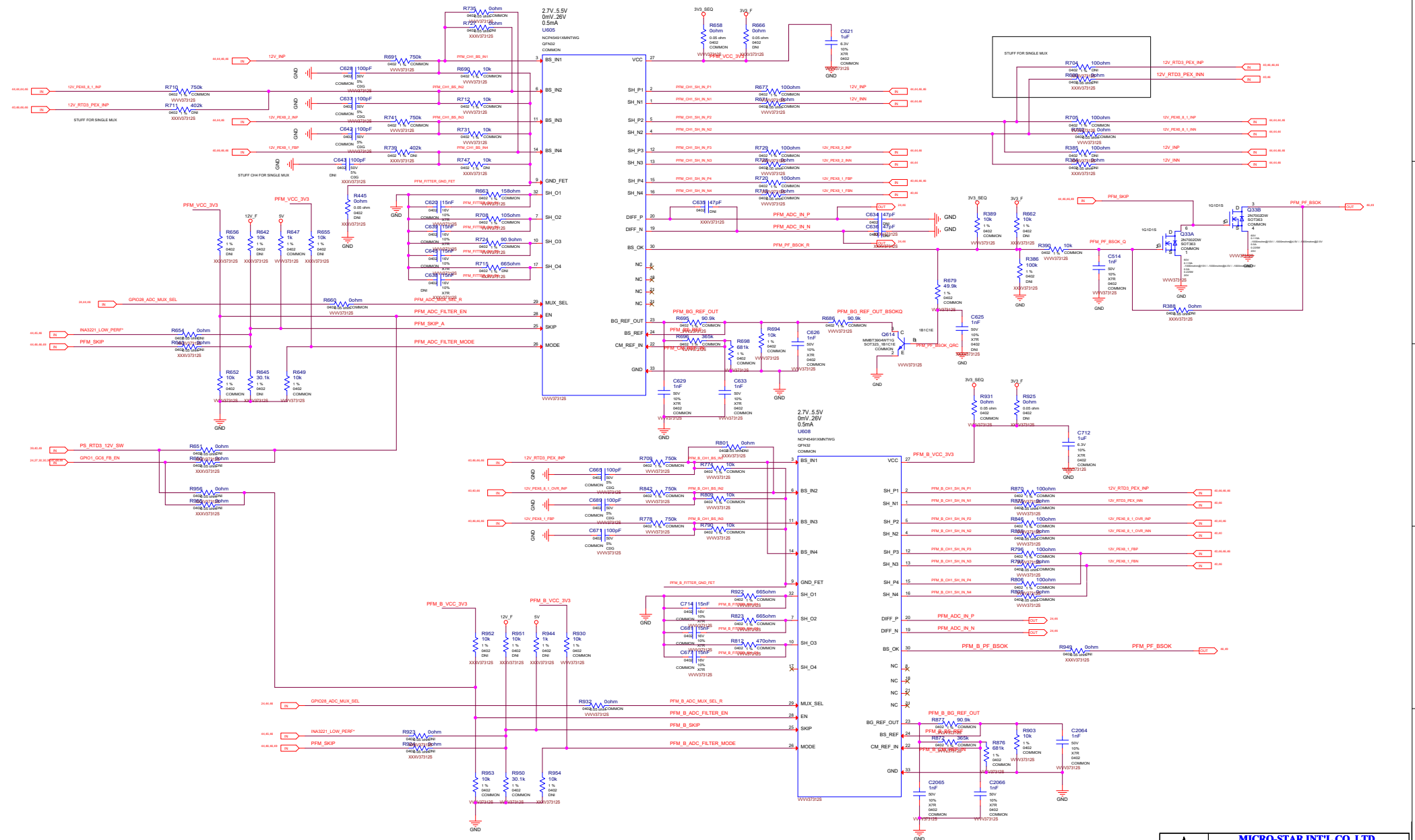
PEX6 INPUT 1 - 2x3 PCIe CON 75W

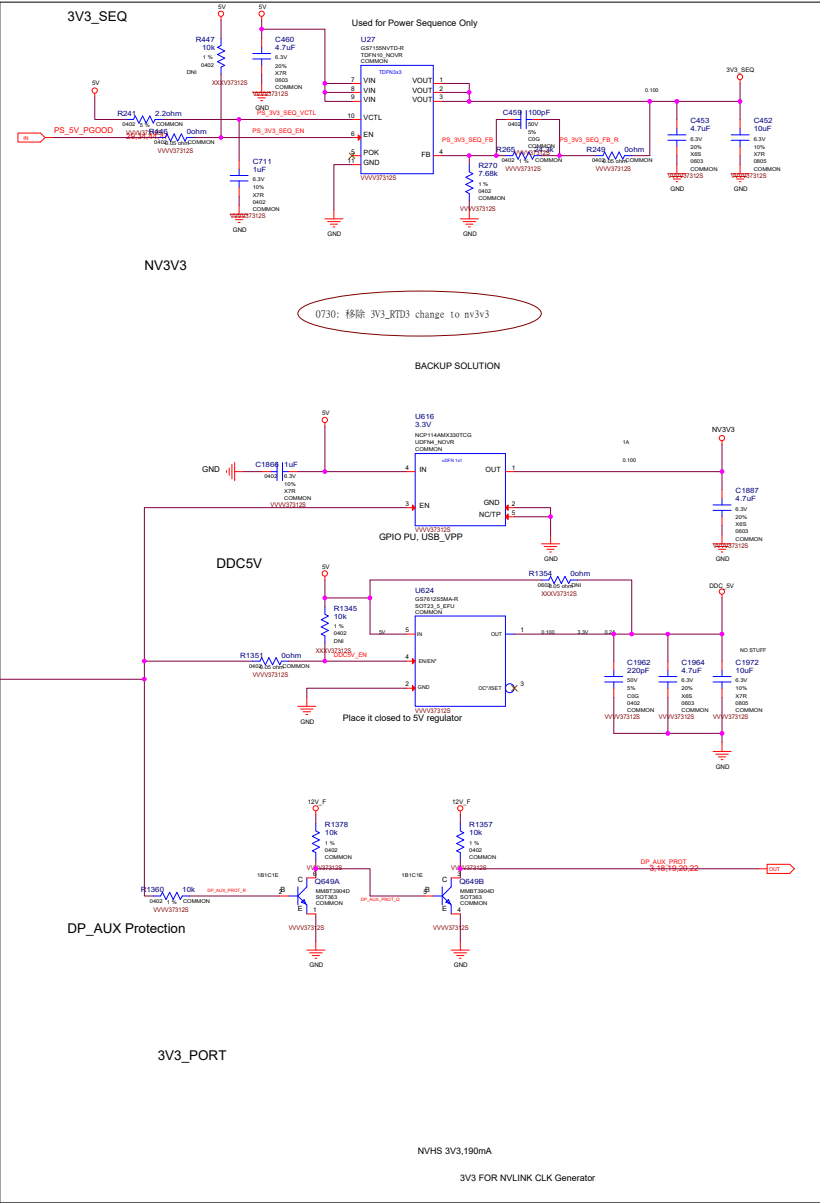
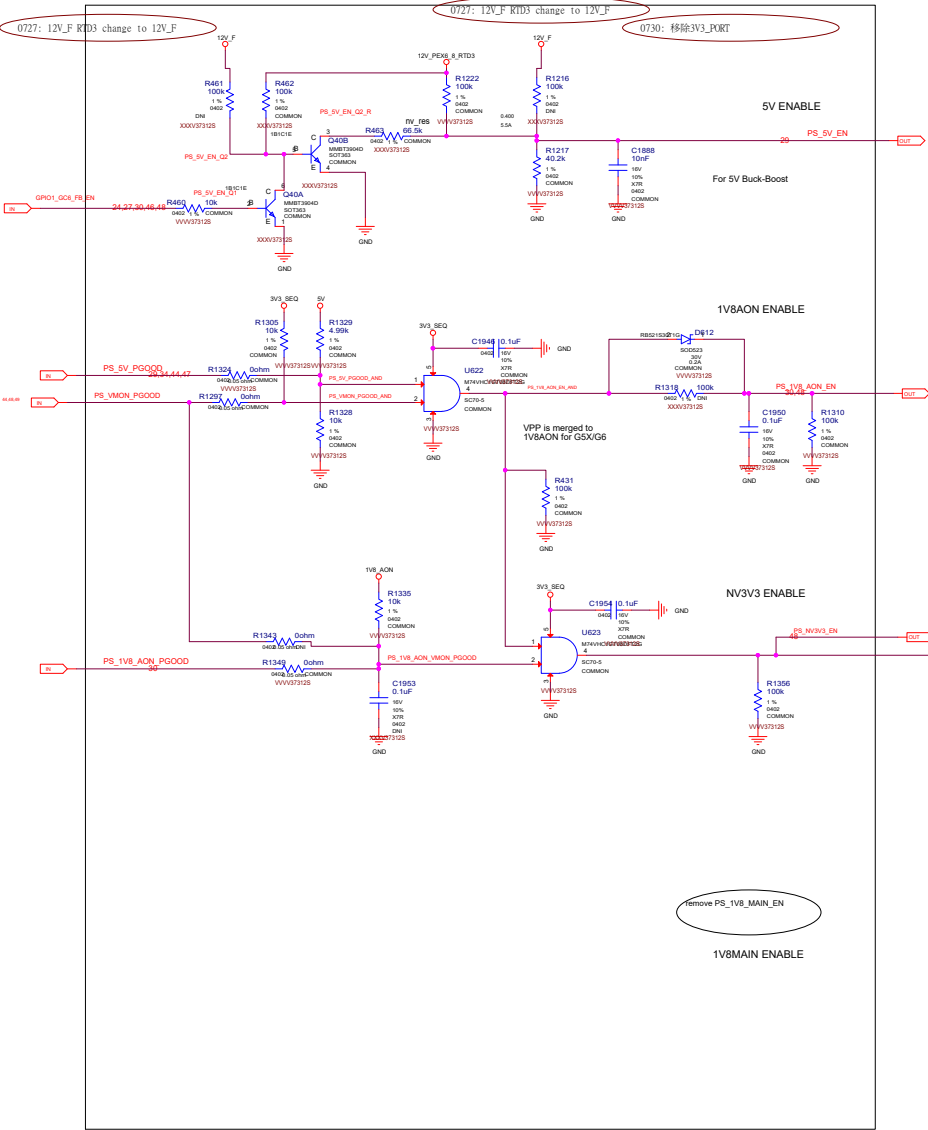


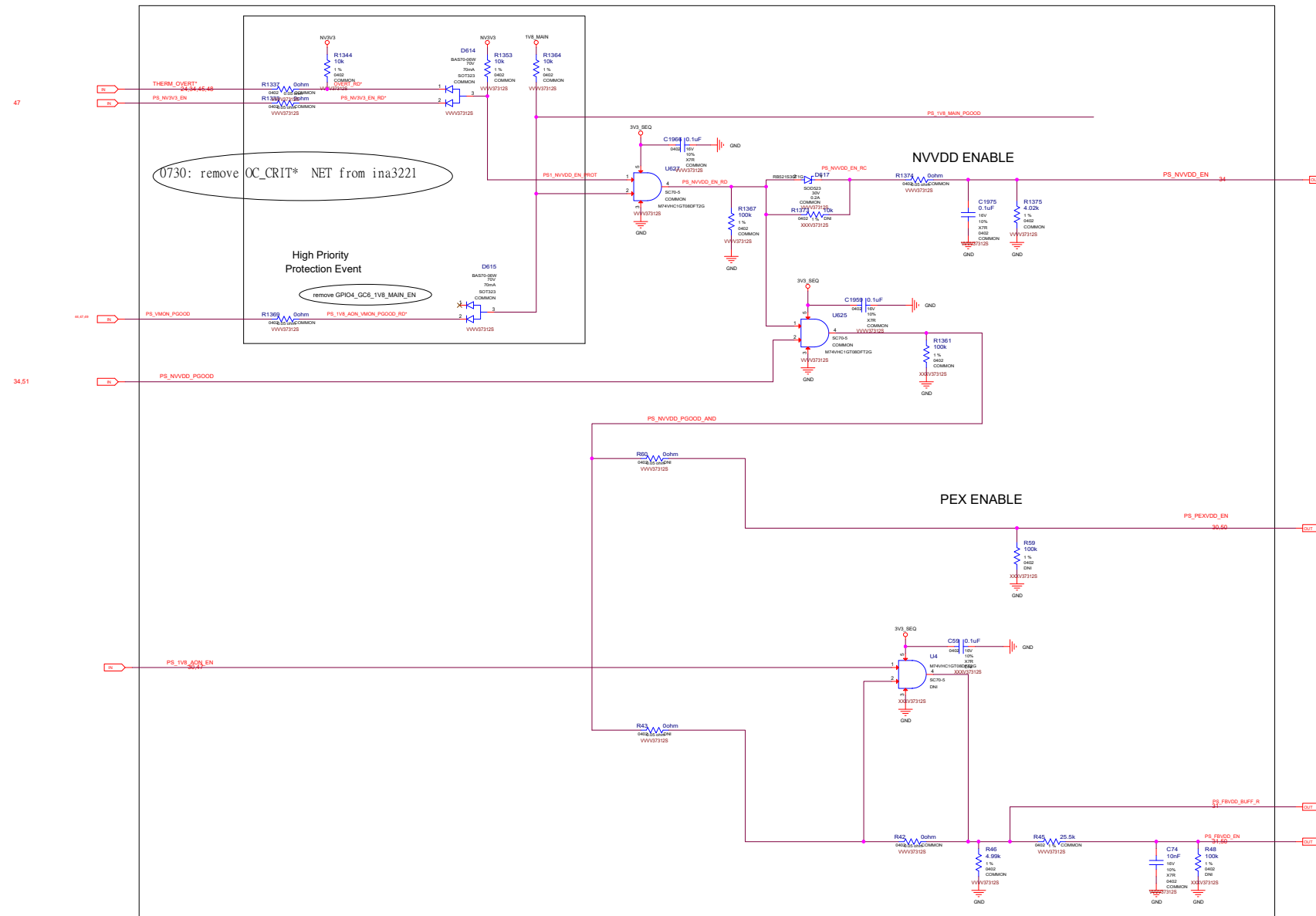
PEX8 INPUT 2 - 2x4 PCIe CON 150W







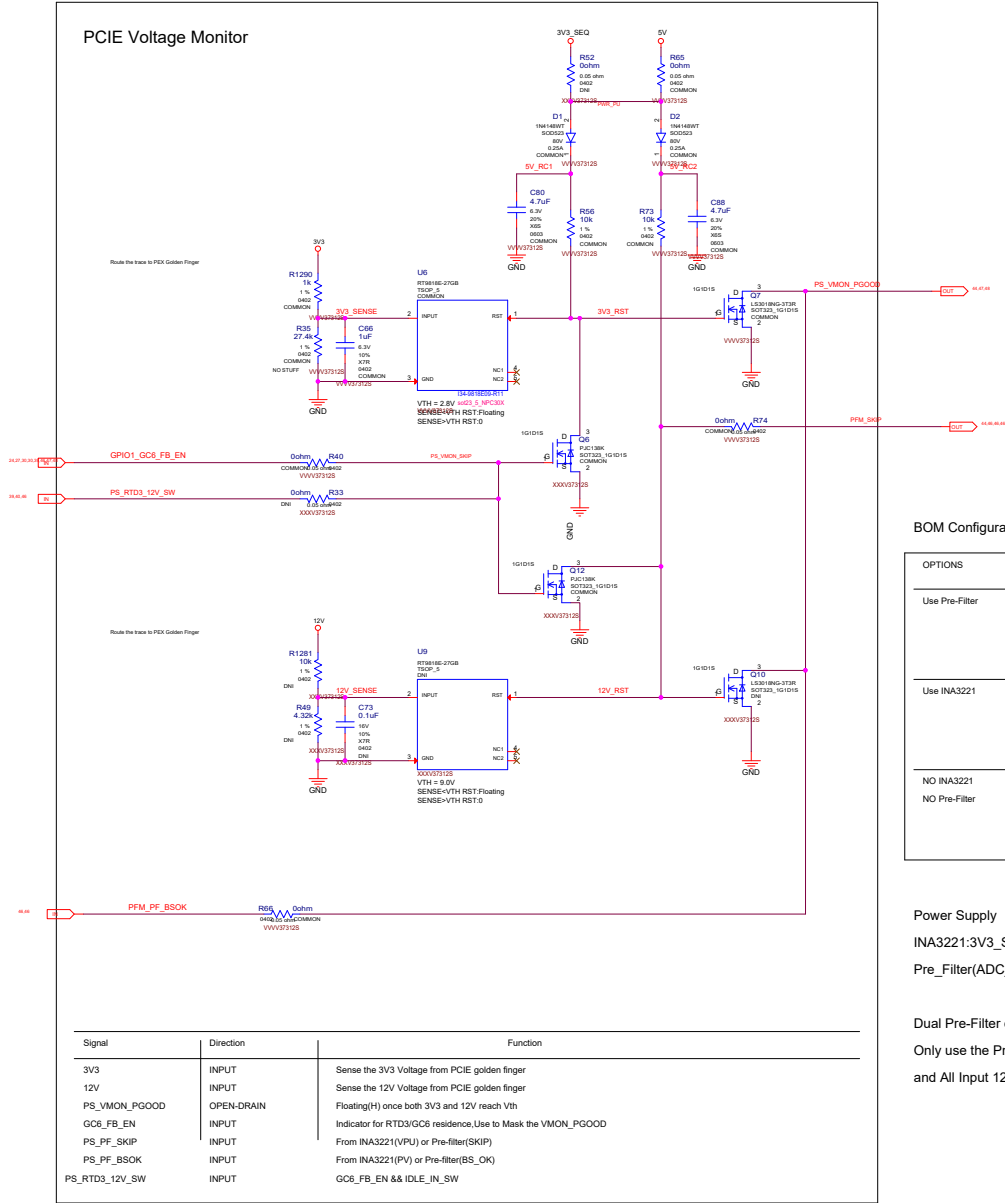




MICRO-STAR INT'L CO.,LTD

MS-V373

Size Custom	Document Description Page48:SEQUENCE_ NV, PEX, FB ENAB
Date: Tuesday, October 23, 2018	Sheet 48



BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ
Pre_Filter(ADC_MUX):3V3(PEX)

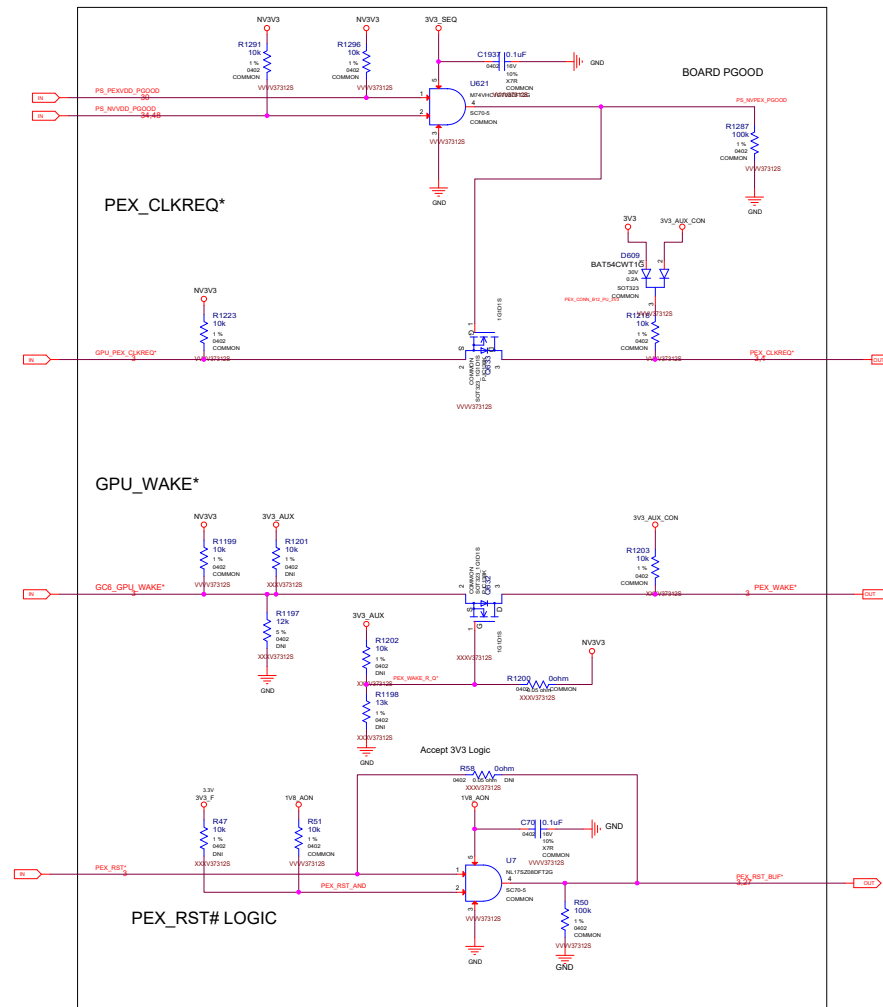
Dual Pre-Filter case:

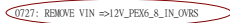
Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

31.48

31.48

30.48

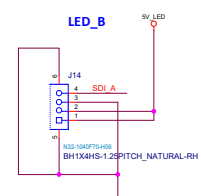
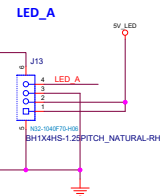
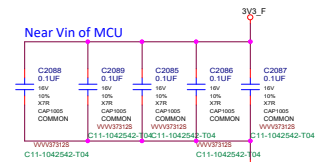
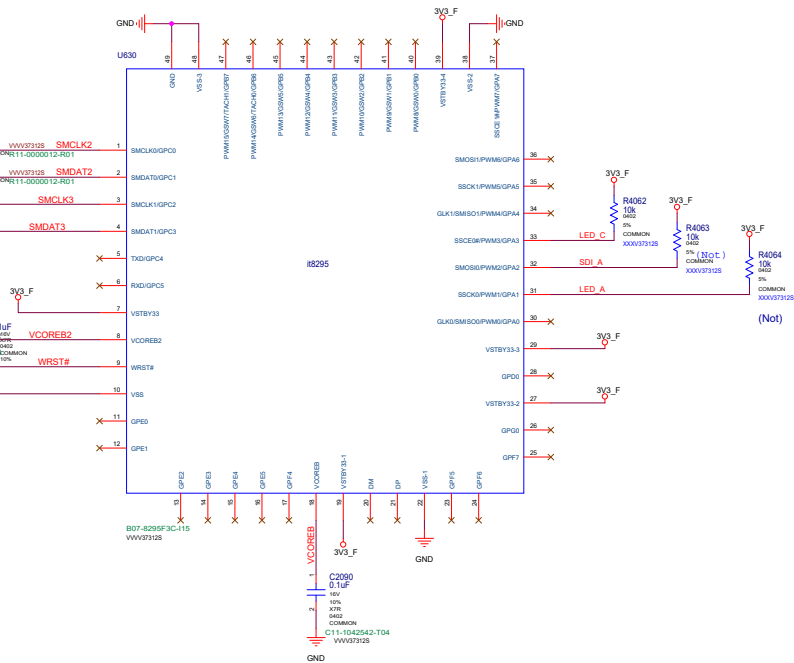
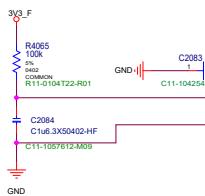
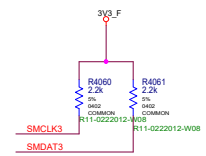
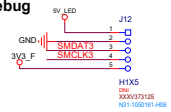




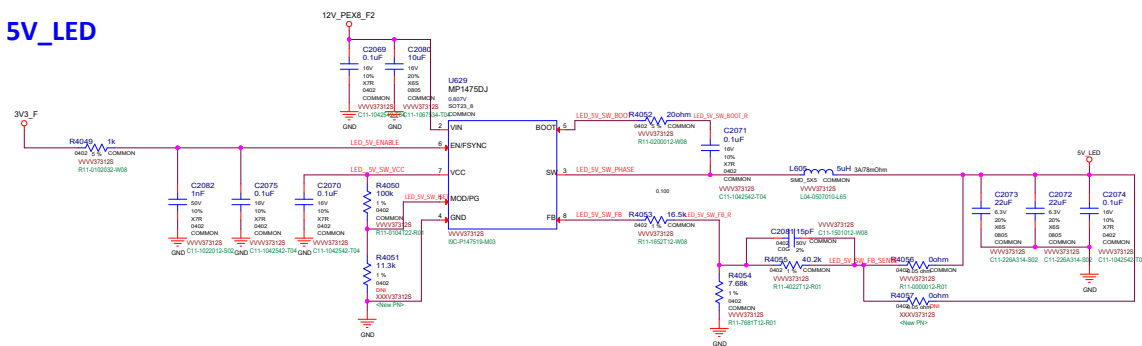
Size Custom	Document Description Page52:LED & FAN HEADERS	Rev 7.1
Date: Tuesday, October 23, 2018	Sheet 52 of 54	

Firmware Programming

Debug



5V_LED

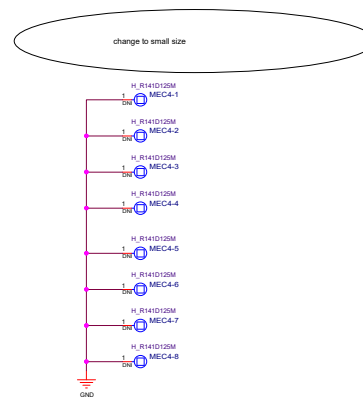
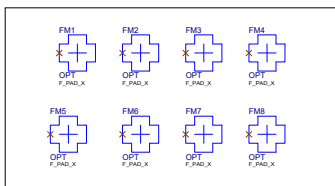
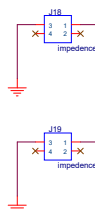
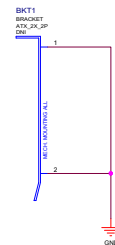




Screw



Brackets:



STIFFENER

Mechanical Holes Symbol

