

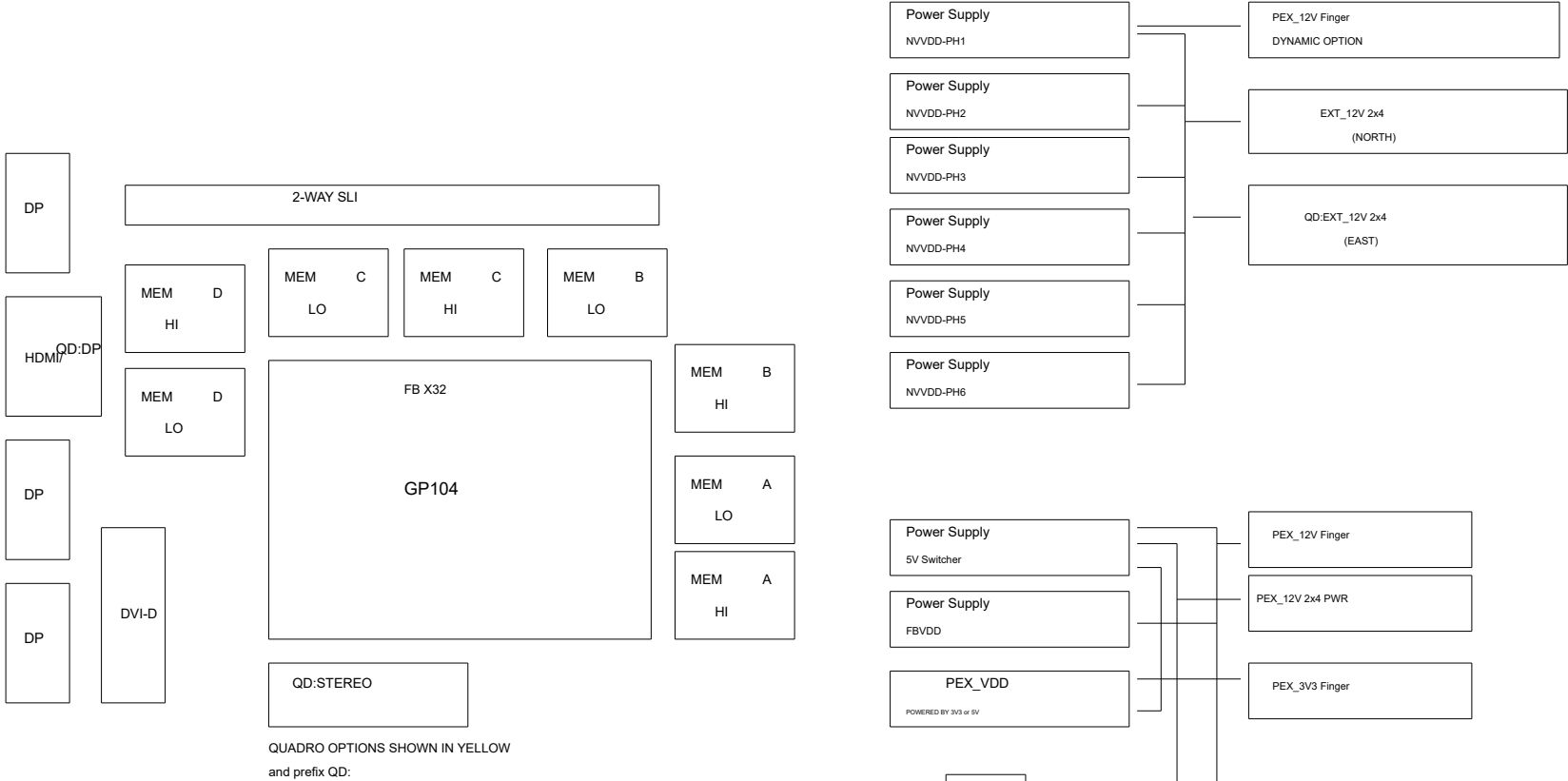
PG411 A01

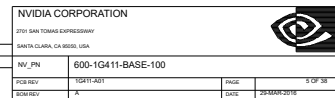
GP104 - 8GB GDDR5, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

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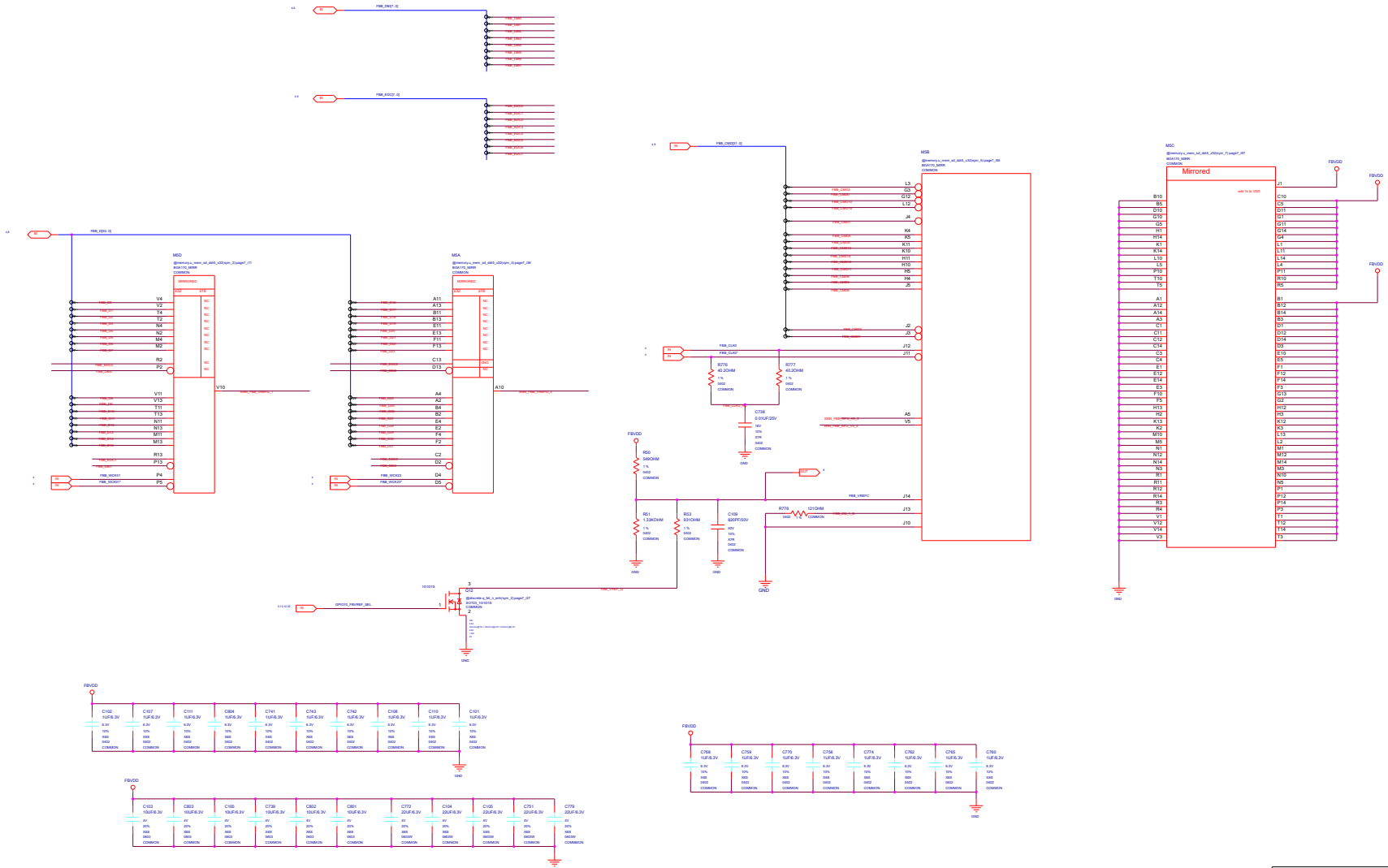
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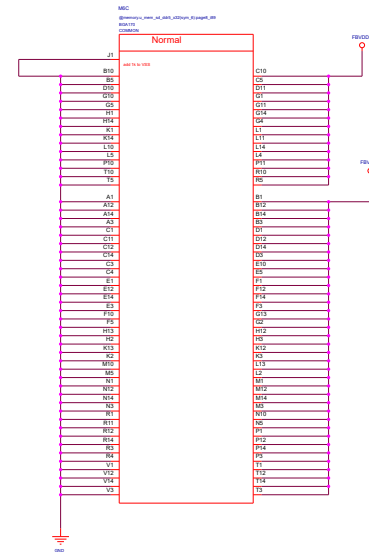
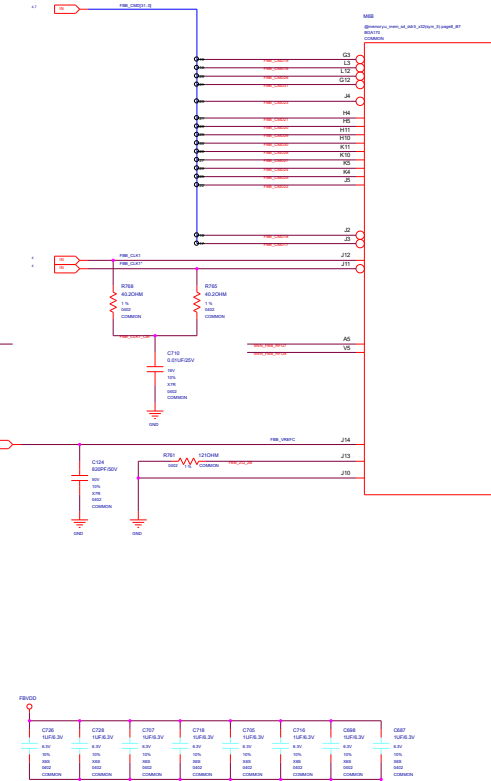


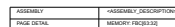


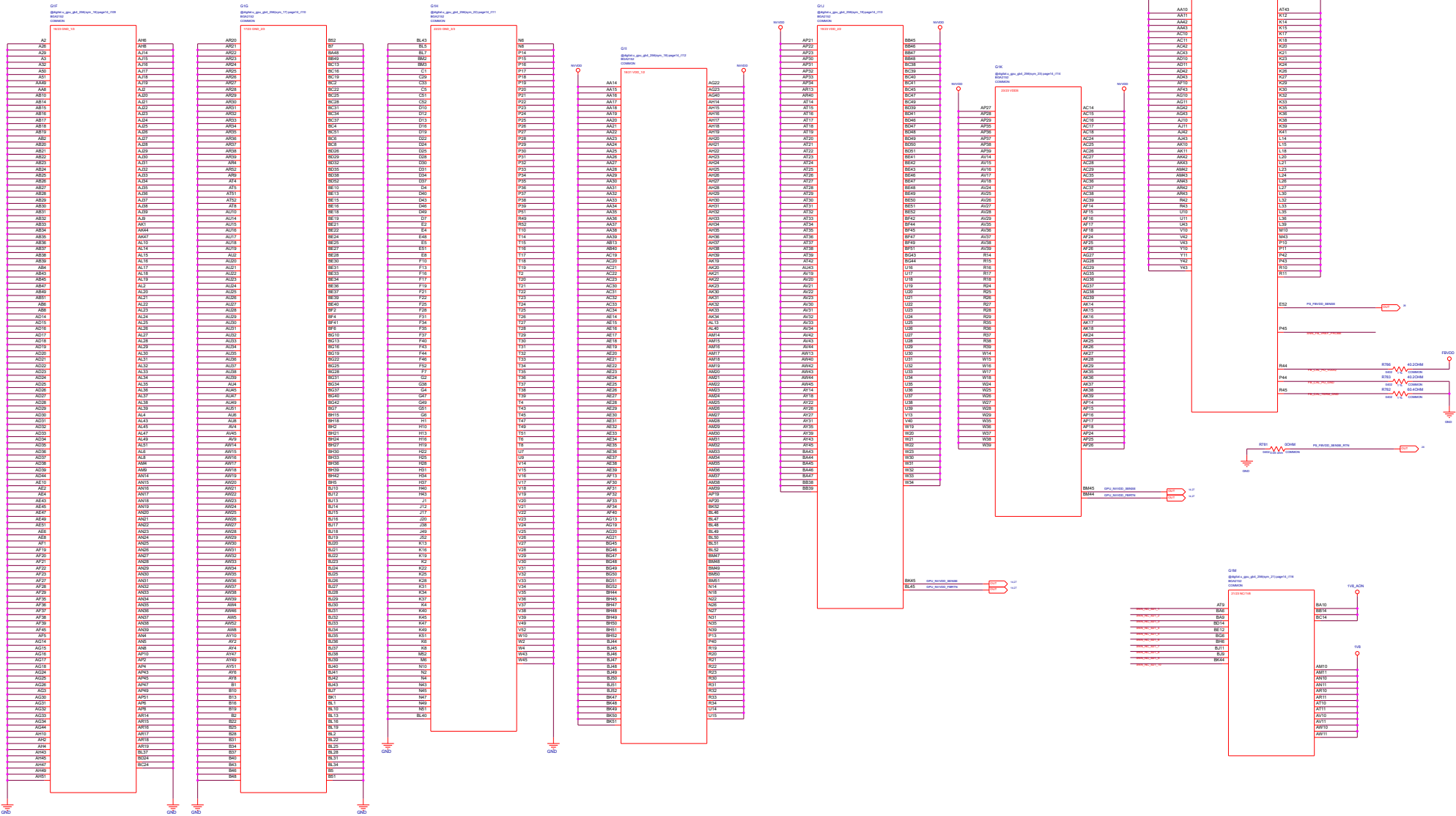


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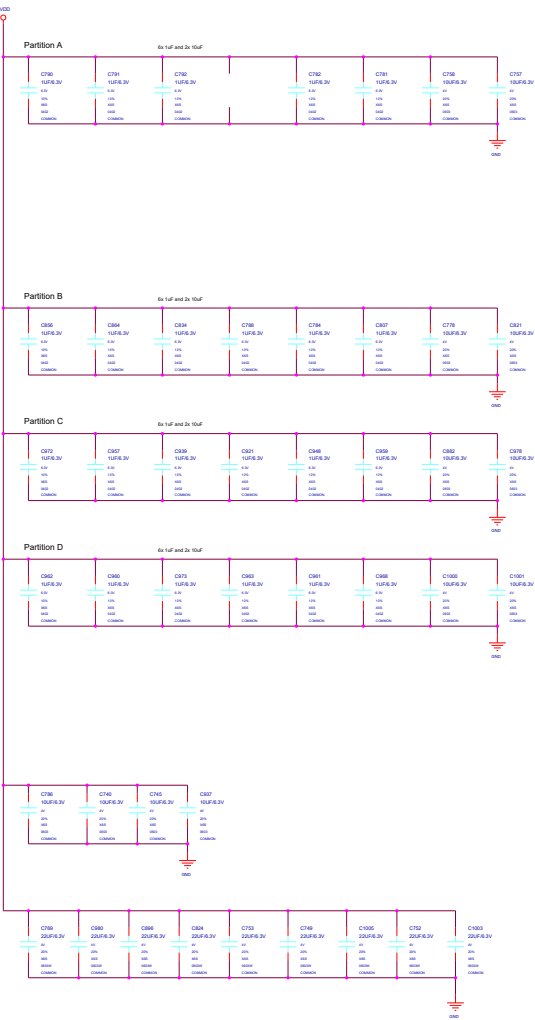




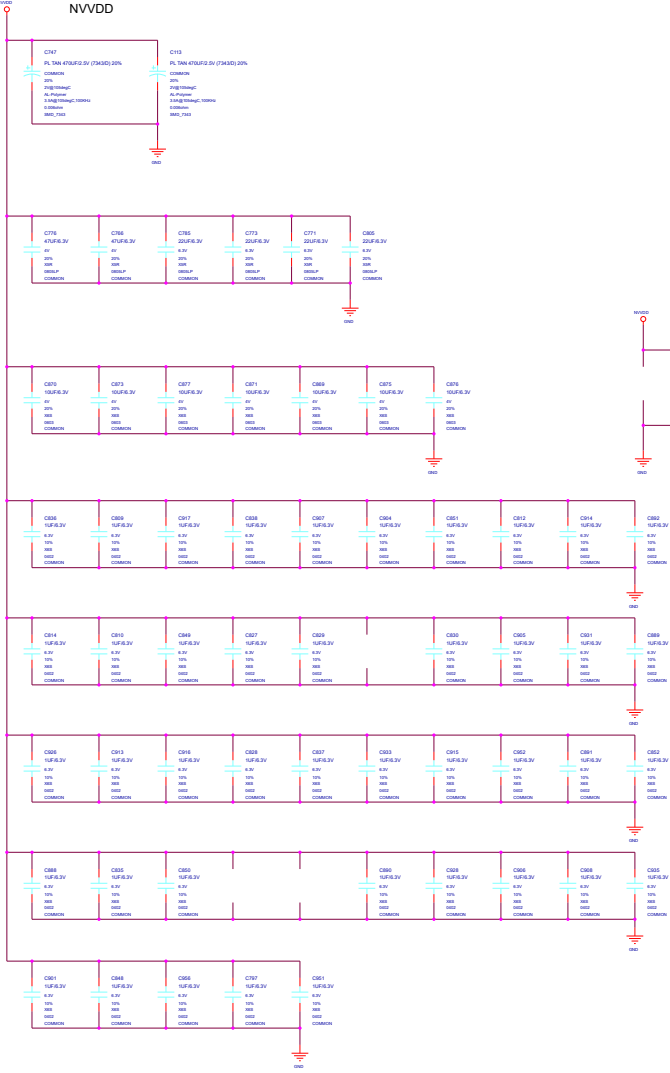




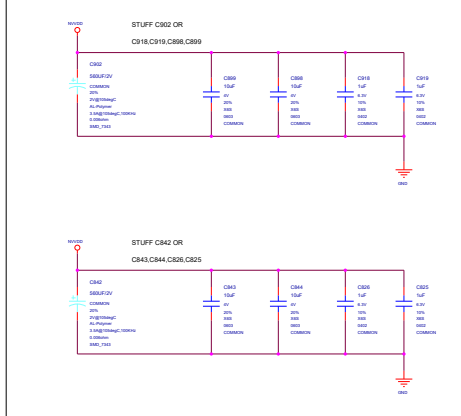
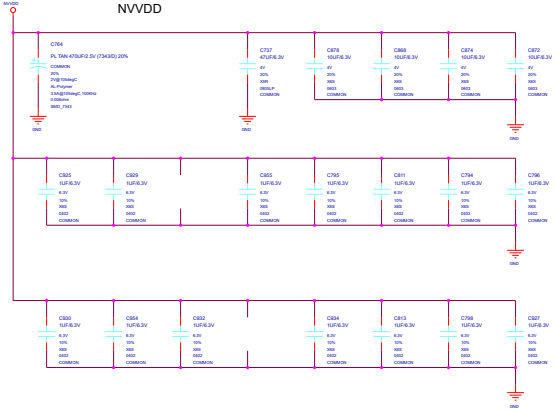
FBVDD



NVDD

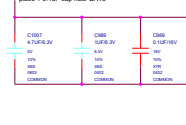


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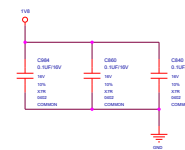


1V8_AON

place 1.0 uF cap near BA10

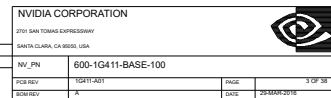


VDD18

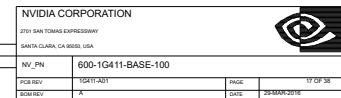


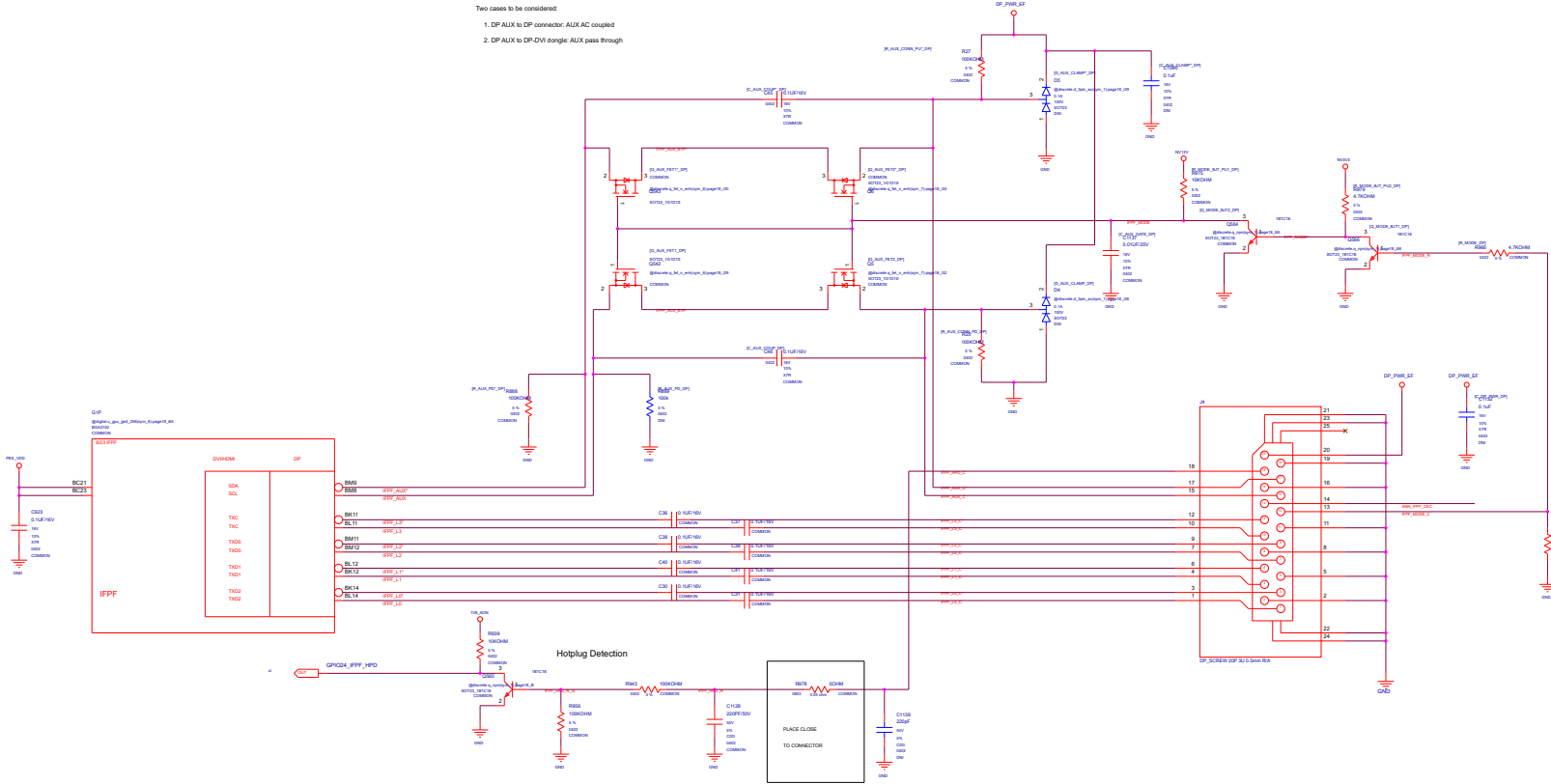
place 1.0 uF cap for BB14 and BC14 to share

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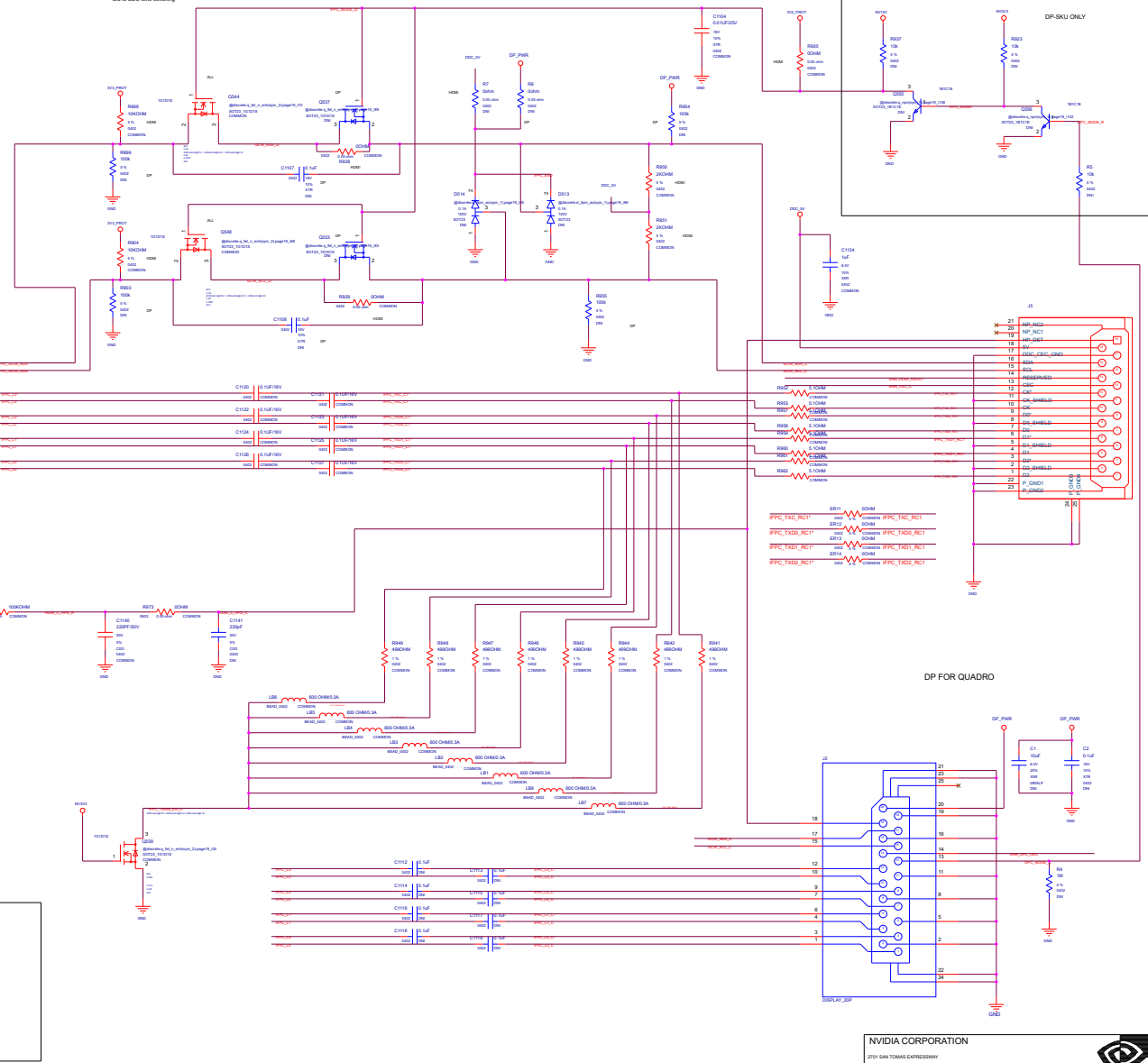
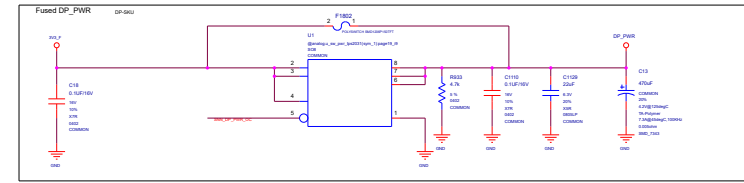
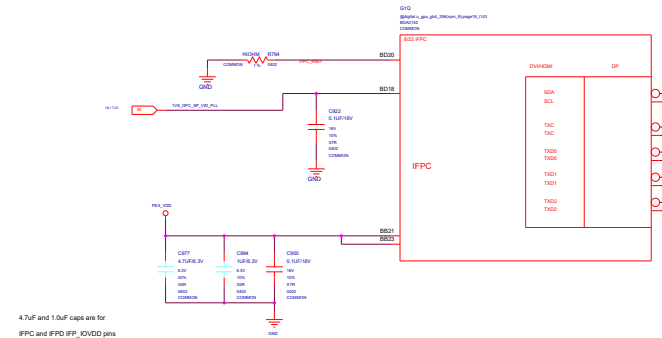
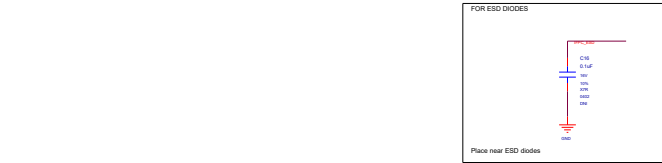


1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

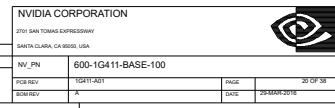


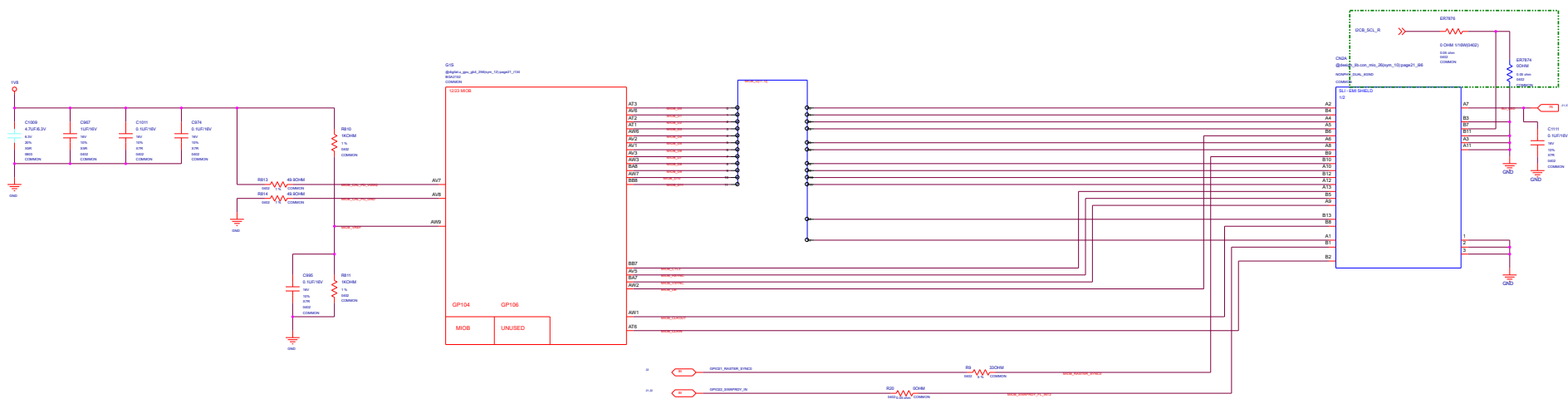



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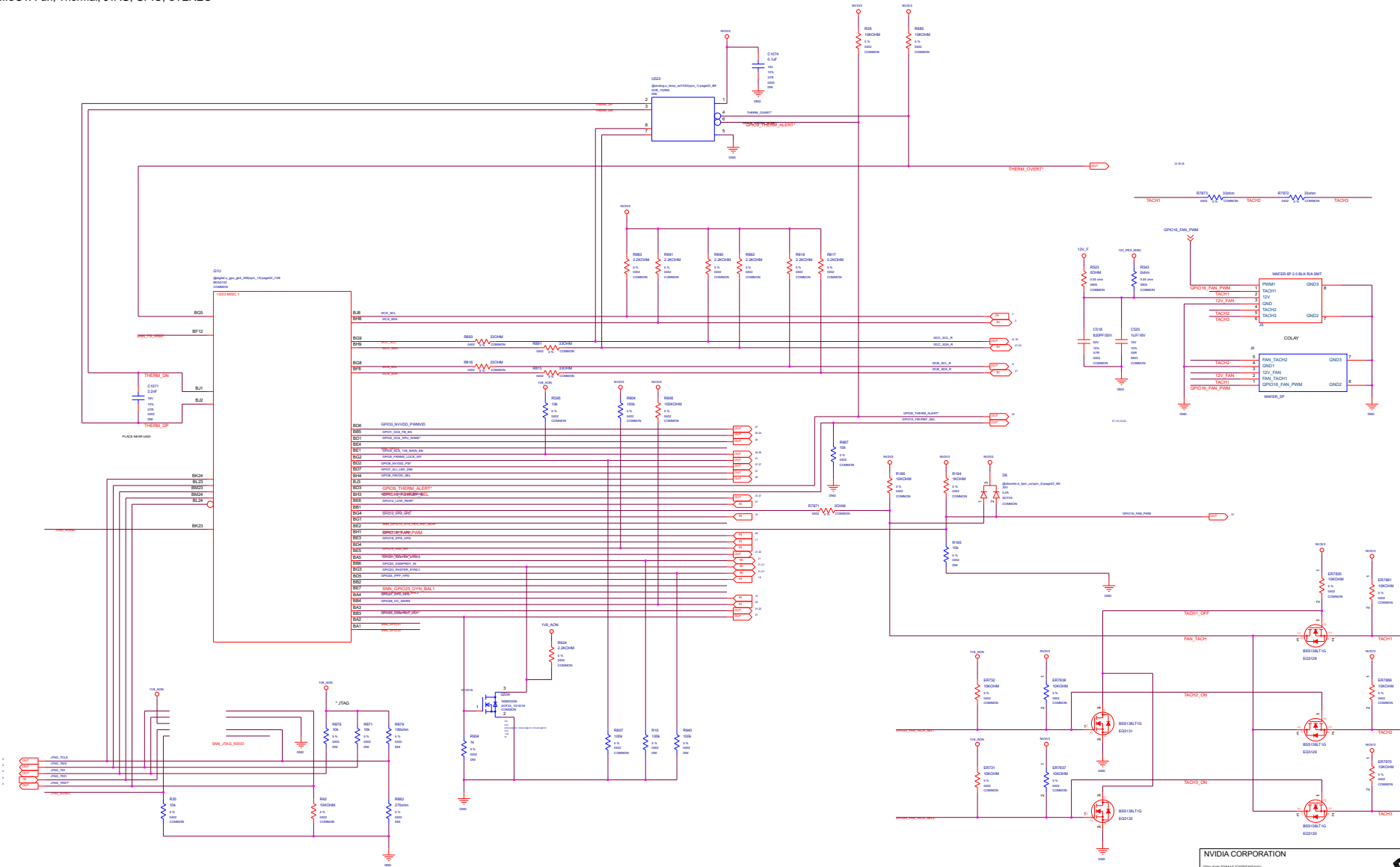
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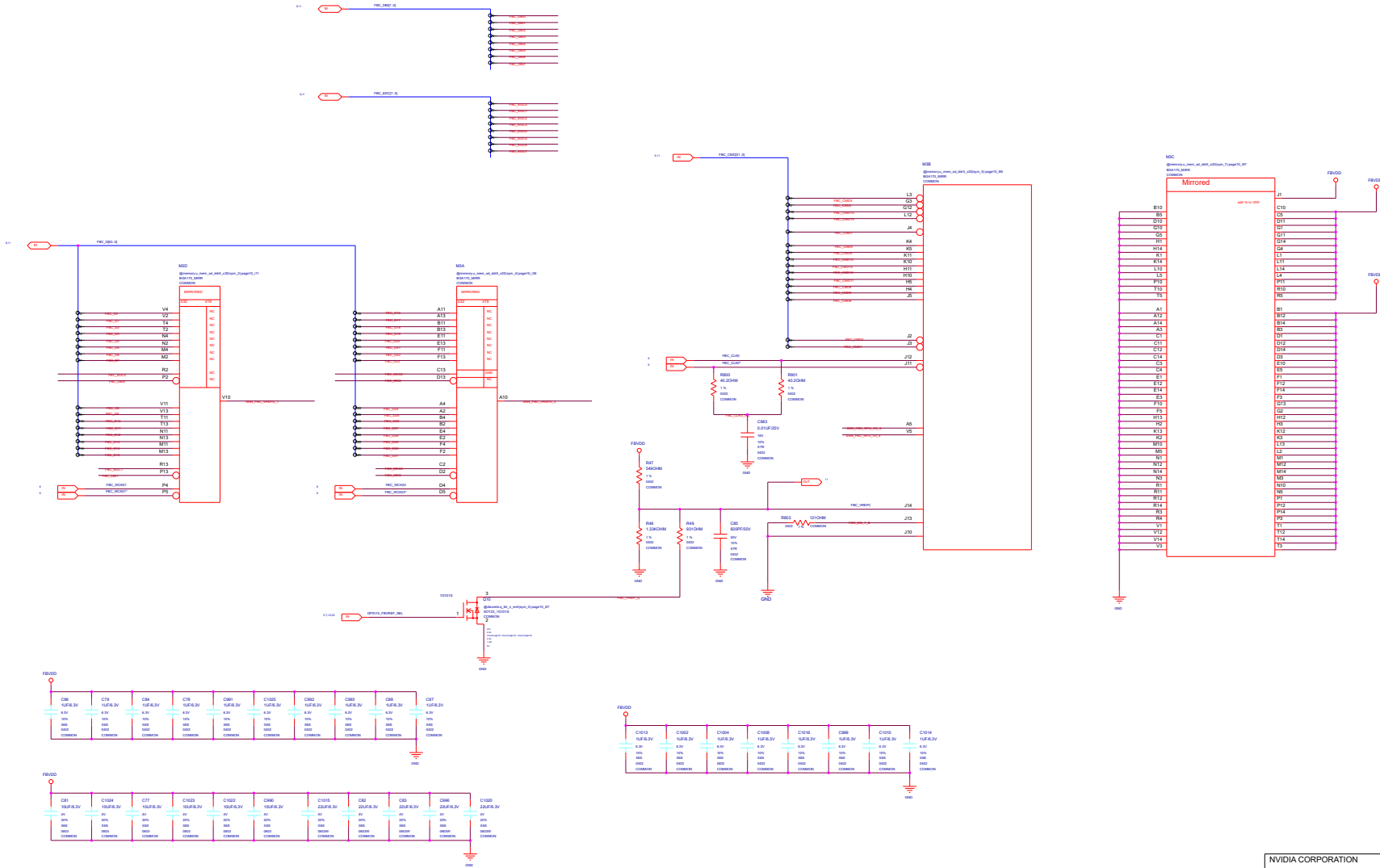


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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DESIGN	MISC1 Fan, Thermal, JTAG, GPIO, Stereo

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
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NV_PN	600-10411-BASE-100		
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ASSEMBLY		ASSEMBLY DESCRIPTION	
FBC PART 31..0		MEMORY FBC(31)0	
NV_PN		600-10411-BASE-100	
FBC REV		10411-001	
BOARD REV		A	
		PAGE 10 OF 38	
		DATE 201809-2018	

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
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NV_PN	600-10411-BASE-100
FBC REV	10411-001
BOARD REV	A

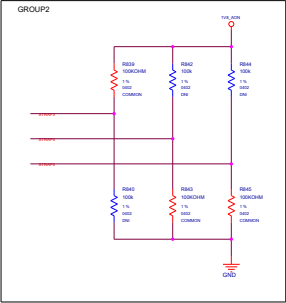
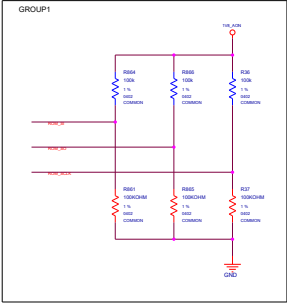
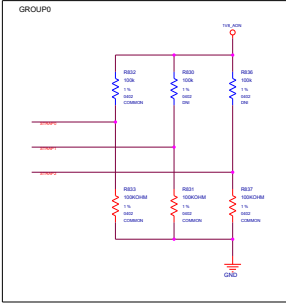
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L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1-ENABLE 0-DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High-Tied to 1.8V
M=Middle-Tied to 0.9V
L=Low-Tied to 0V

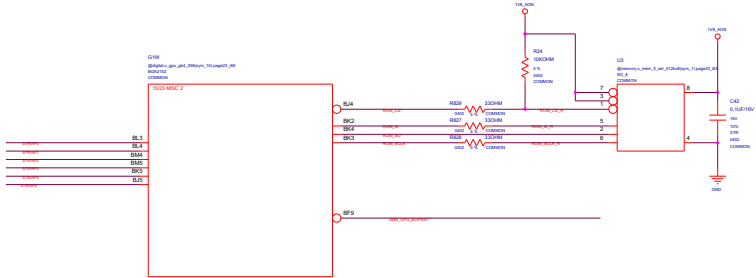
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

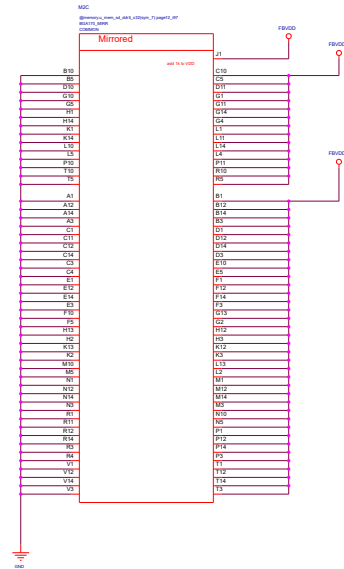
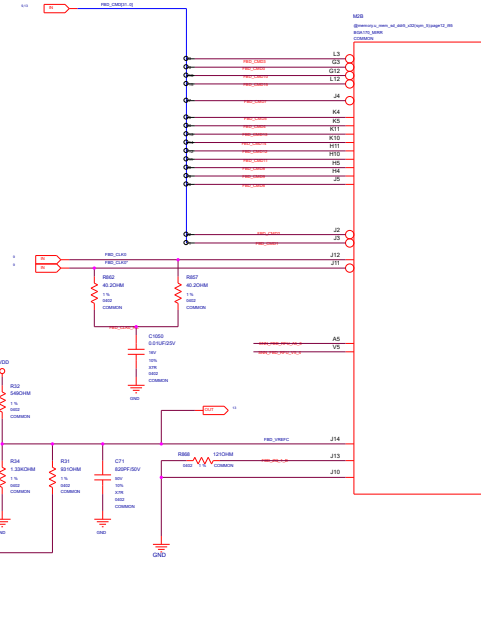
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

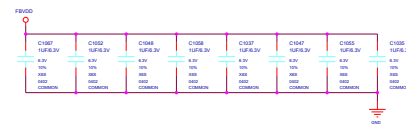
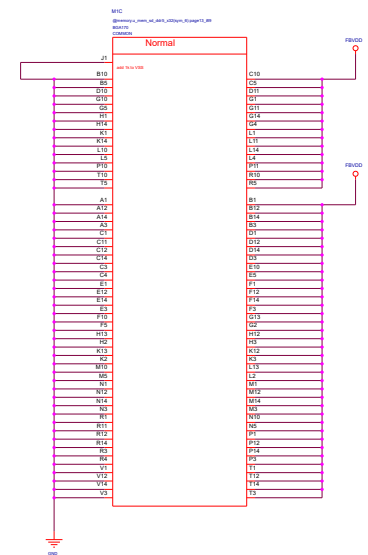


CFDP[0] Config With Vendor

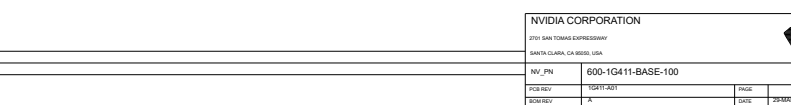
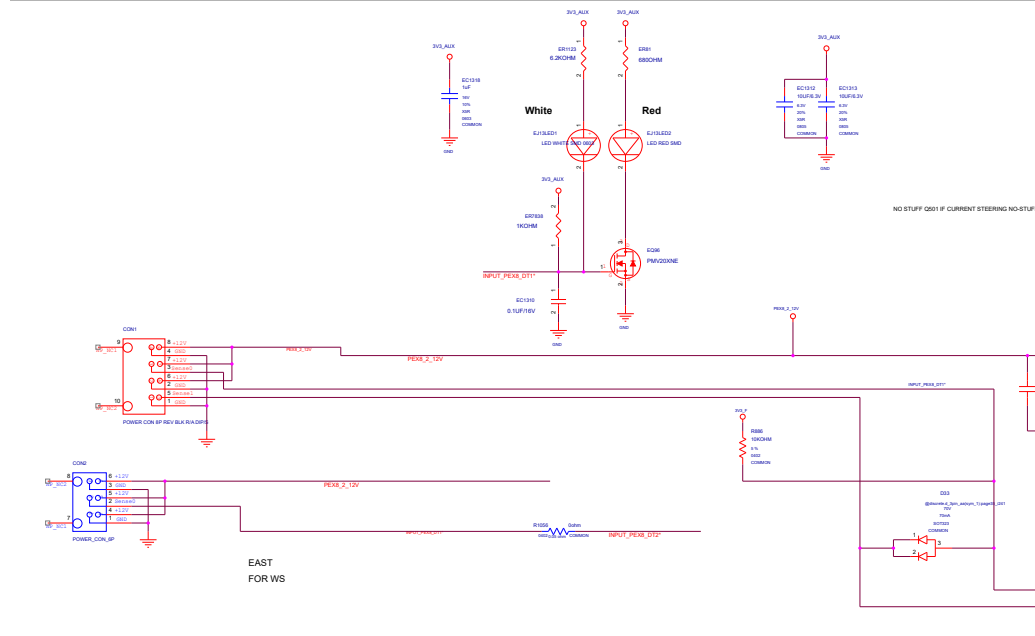
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0001 256MA32 256-44t Micron
0010 256MA32 256-44t Hynix
0011 Reserved
0100 Reserved
0101 Reserved
0110 Reserved
0111 Reserved




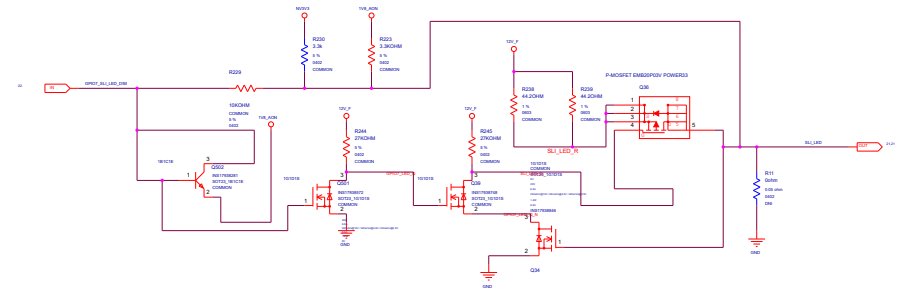
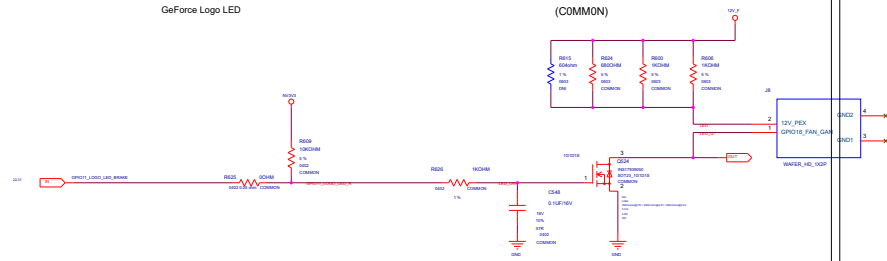




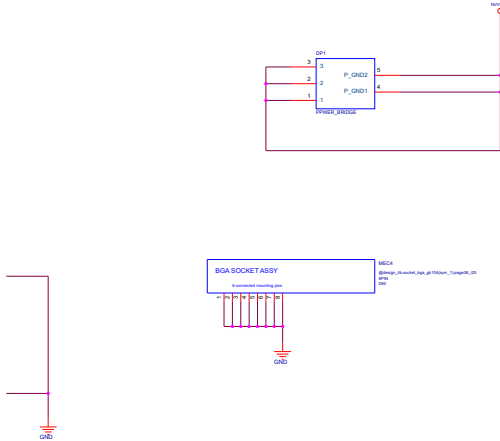
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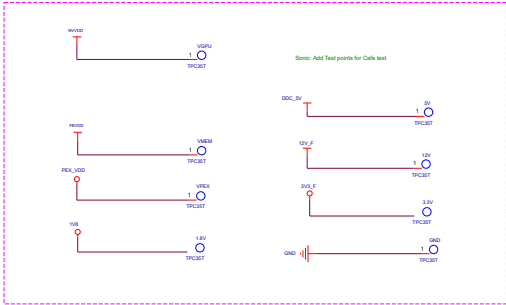
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NV_PN	600-1G411-BASE-100			
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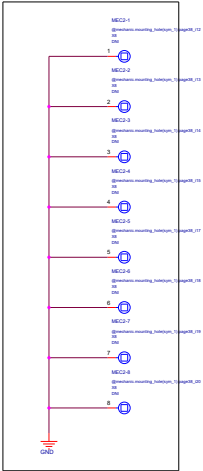
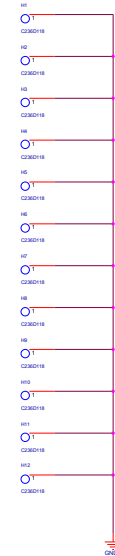
Brackets:

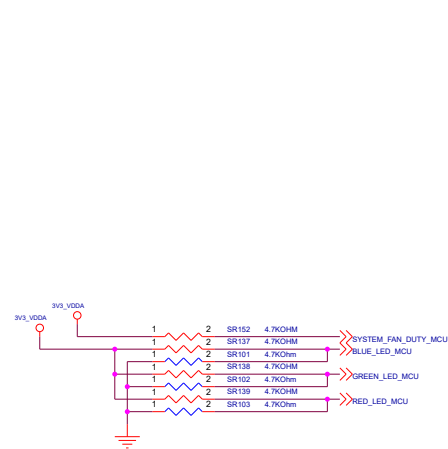
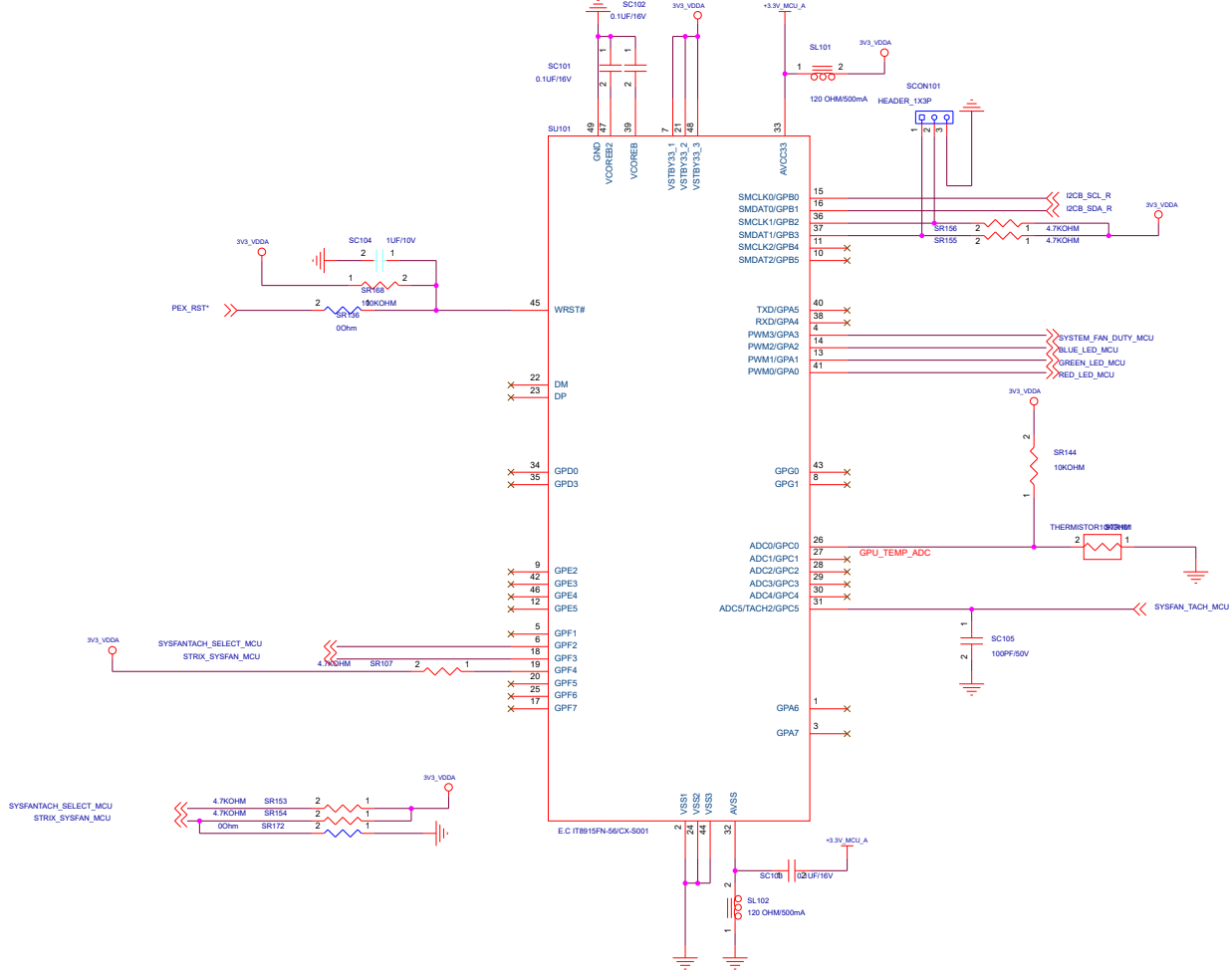


GPU Stiffener



Mechanical Holes Symbol





STRIX_101 請盡可能放置於GPU位置 (在不影響Layout的前提下)

SCL SDA TO GPU MASTER I2C

PERST# TO PCIE

3V3_VDDA TO Power (under 10mA)

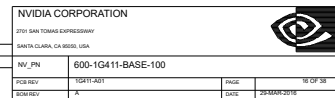
SYSFAN_TACH_MCU SYSFANTACH_SELECT_MCU STRIX_SYSFAN_MCU SYSTEM_FAN_DUTY_MCU TO S0002 SYSTEM FAN CONTROL

BLUE_LED_MCU GREEN_LED_MCU RED_LED_MCU TO S0003 RGB LED

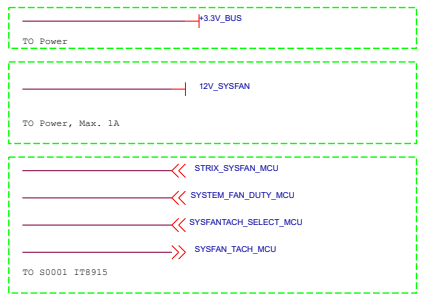
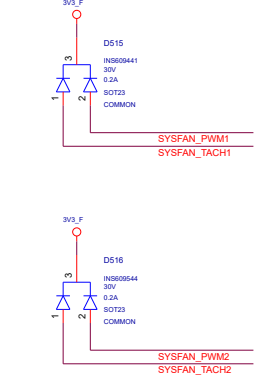
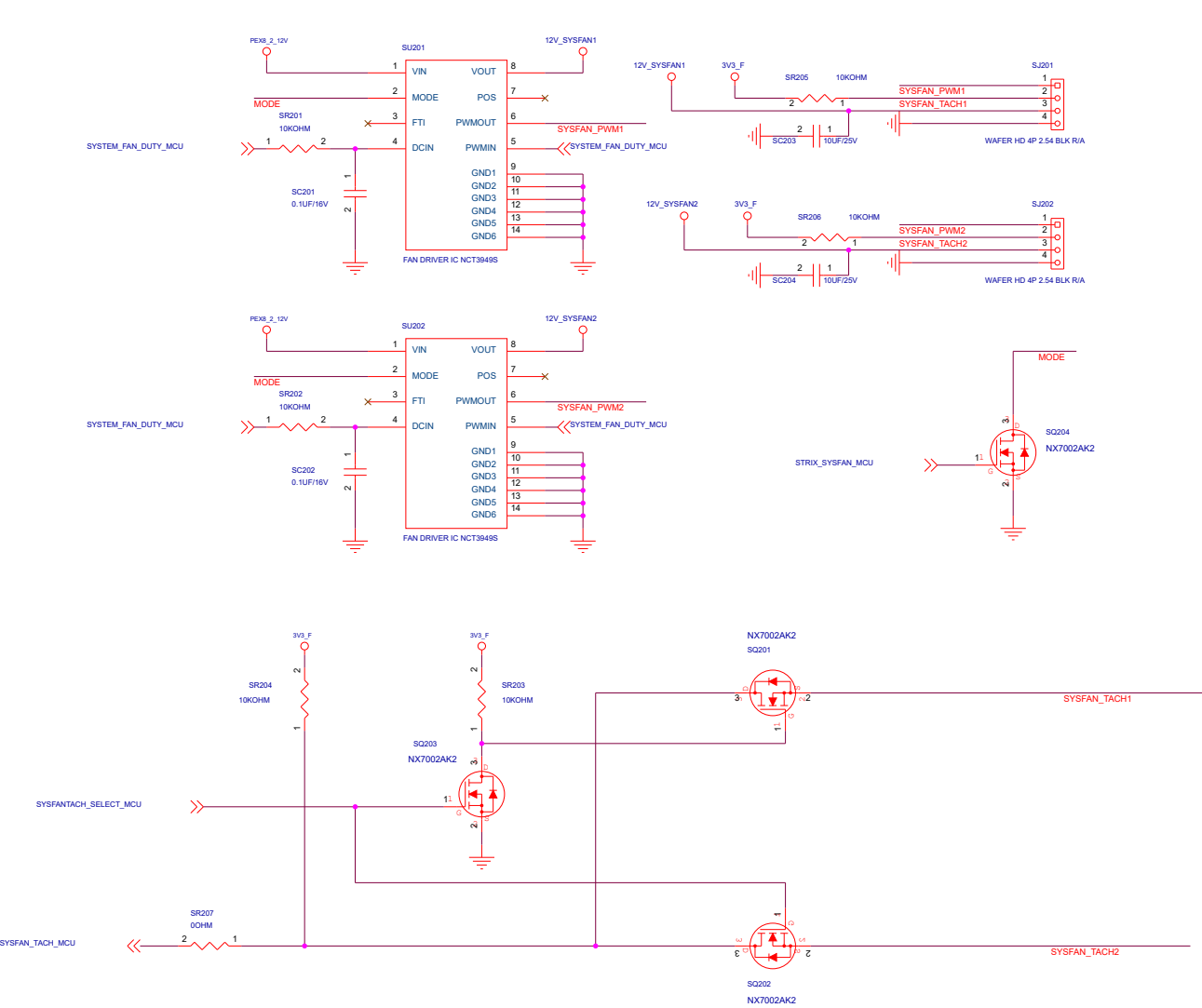
STRIX_SYSFAN_MCU	Mode
L	NORMAL
H (Default)	STRIX

SYSFANTACH_SELECT_MCU	Mode
L	SYSFAN_TACH1
H (Default)	SYSFAN_TACH2

Title		
<Title>		
Size	Document Number	
A3	<Doc>	
Date:	Wednesday, December 28, 2016	Rev <RevCode>
Sheet	1	of 1

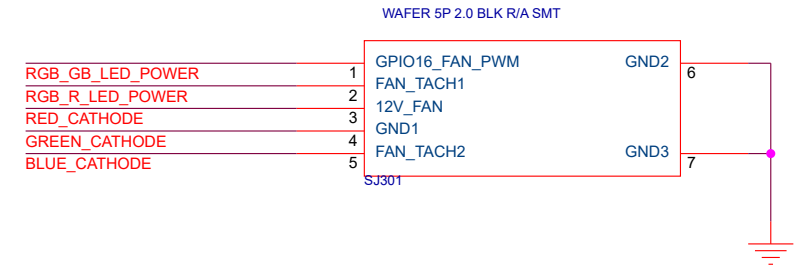
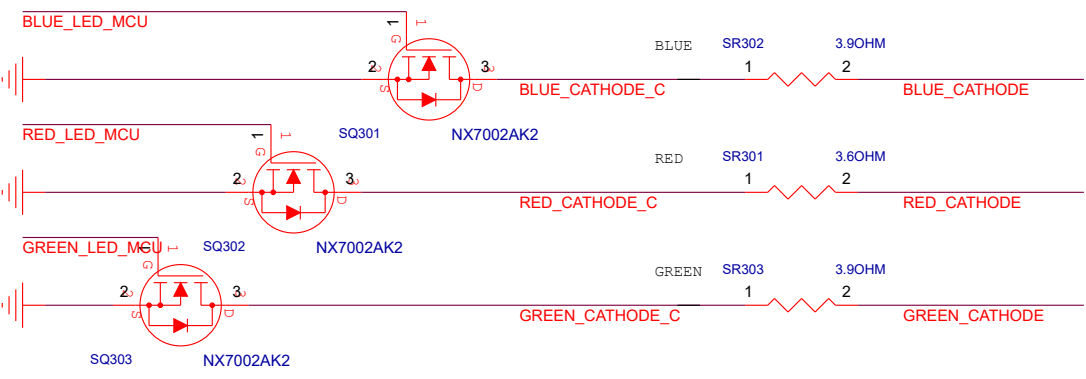
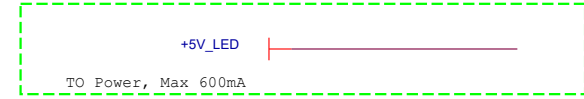
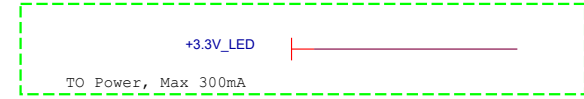
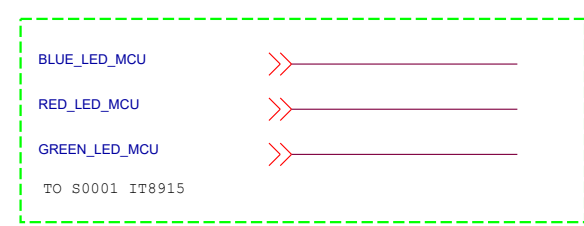
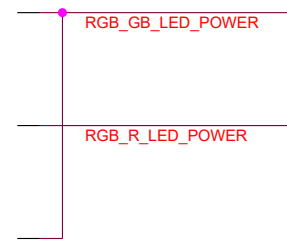
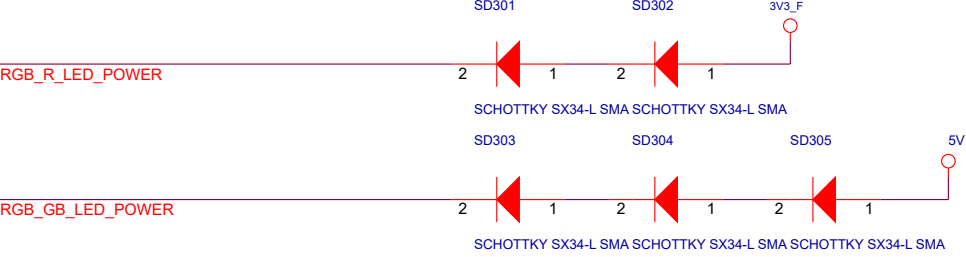


ASSEMBLY	=ASSEMBLY_DESCRIPTION
PAGE DETAIL	IFPAB DIV D-CL

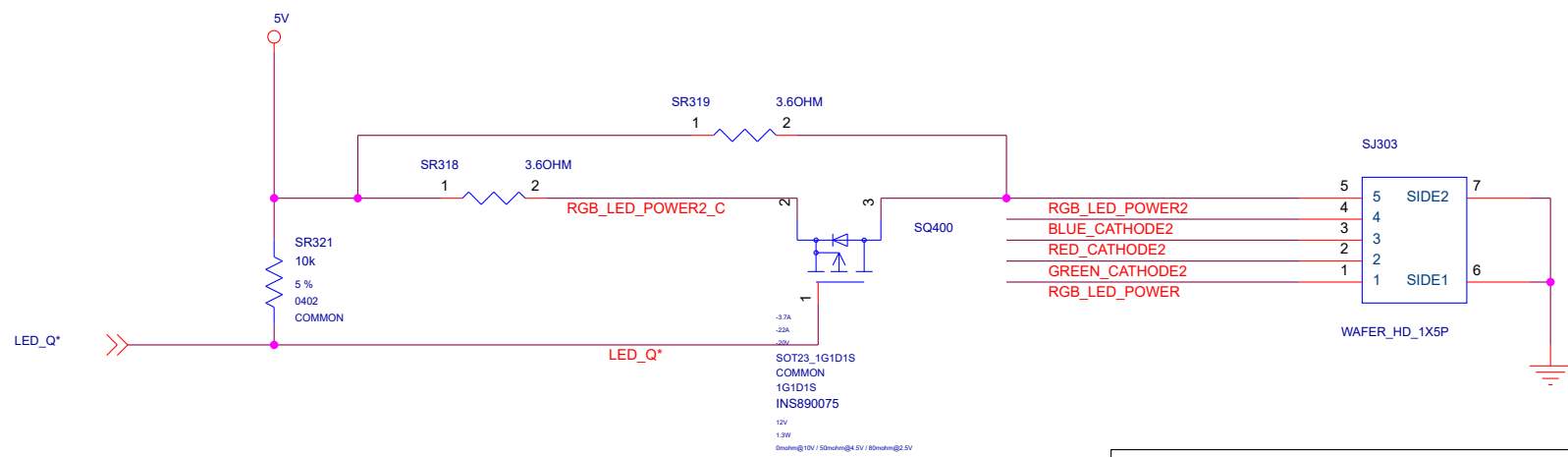
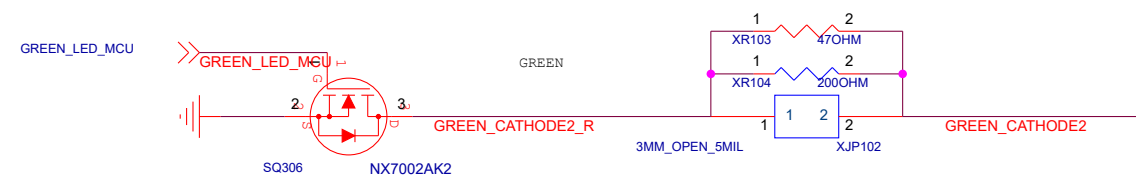
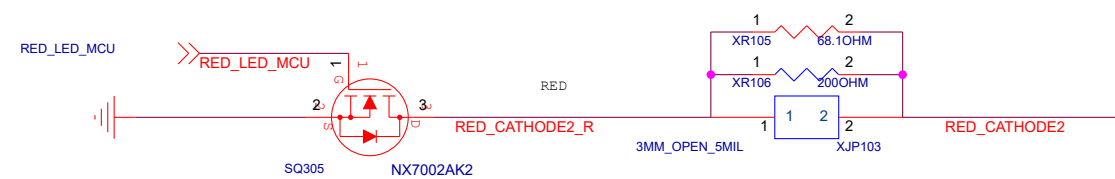
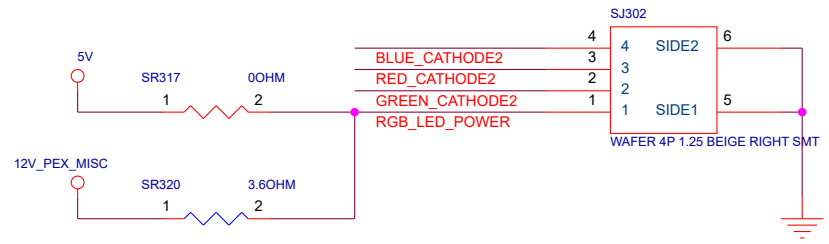
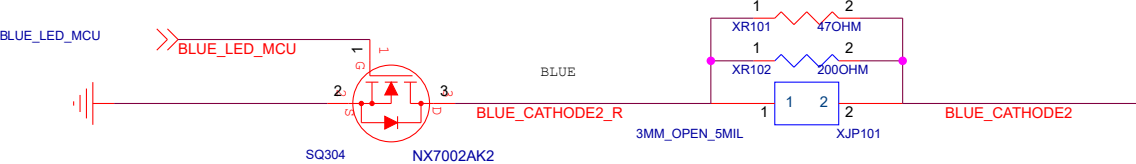


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H (Default)	STRIX

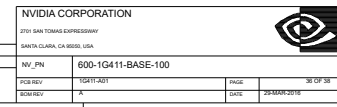
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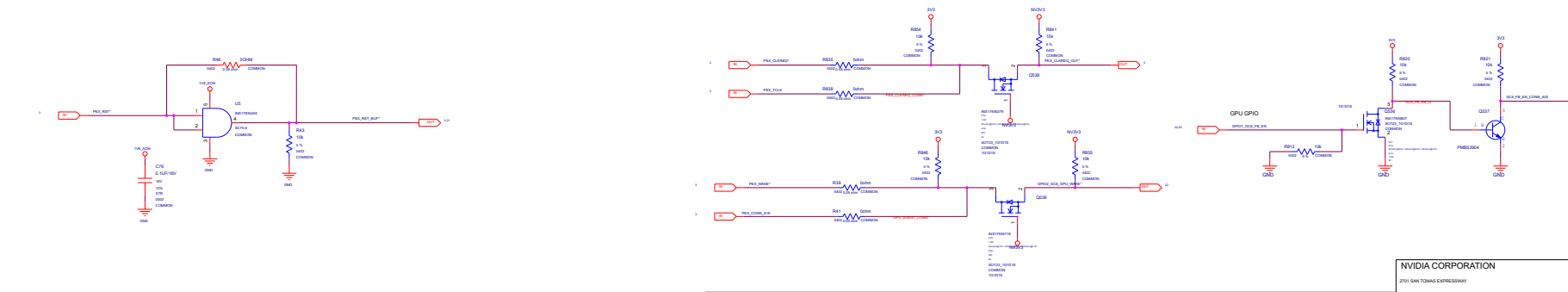
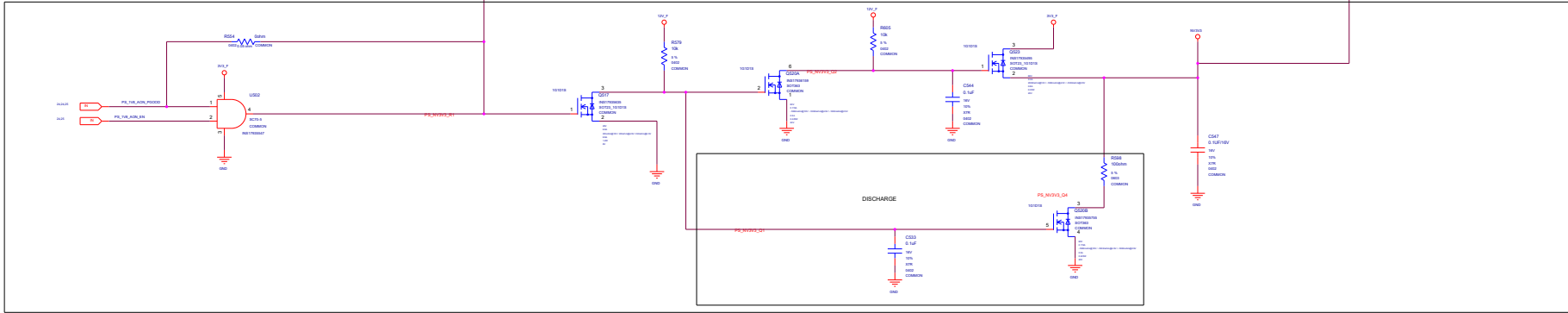
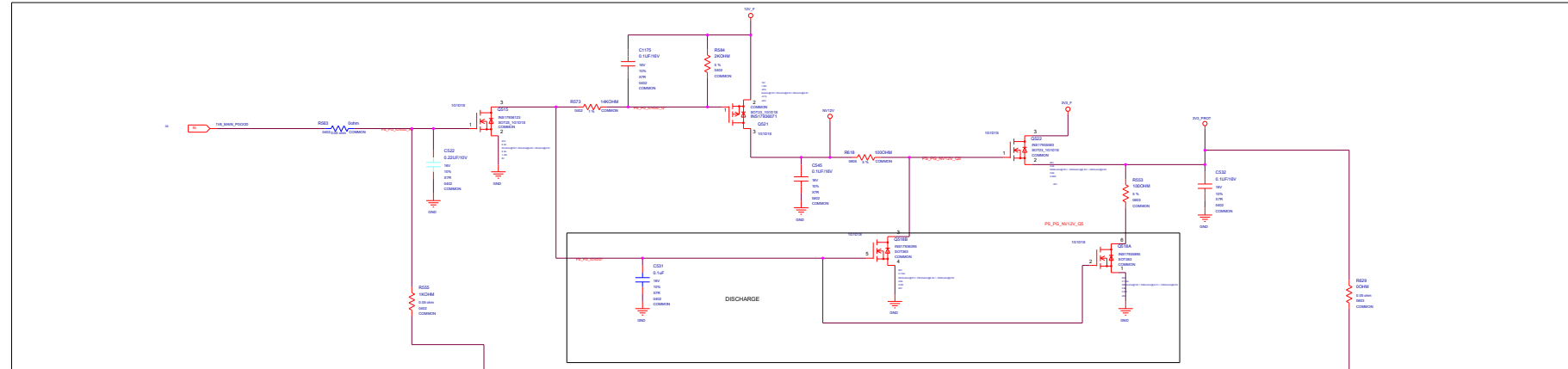


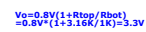
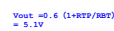
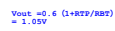
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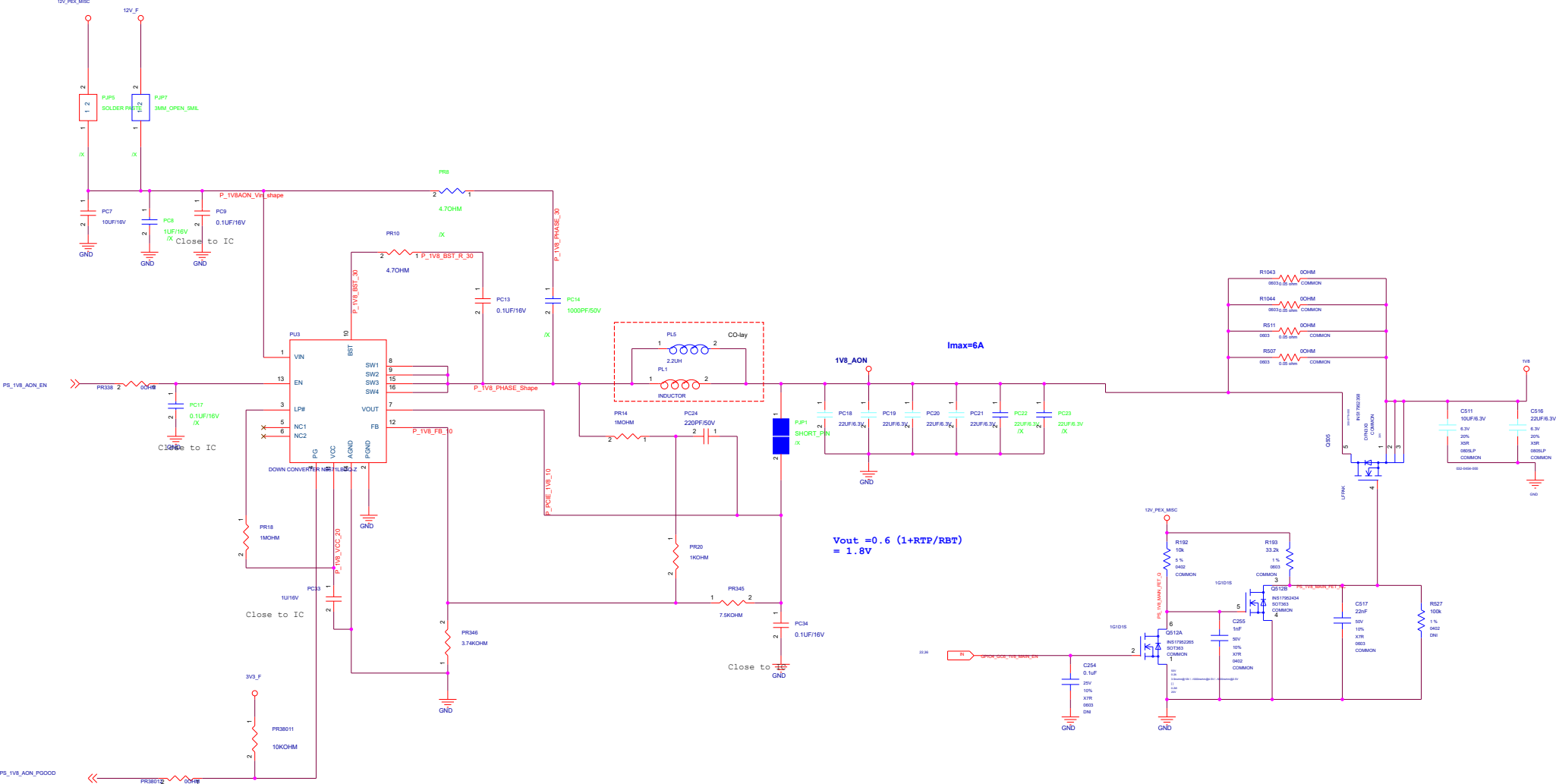


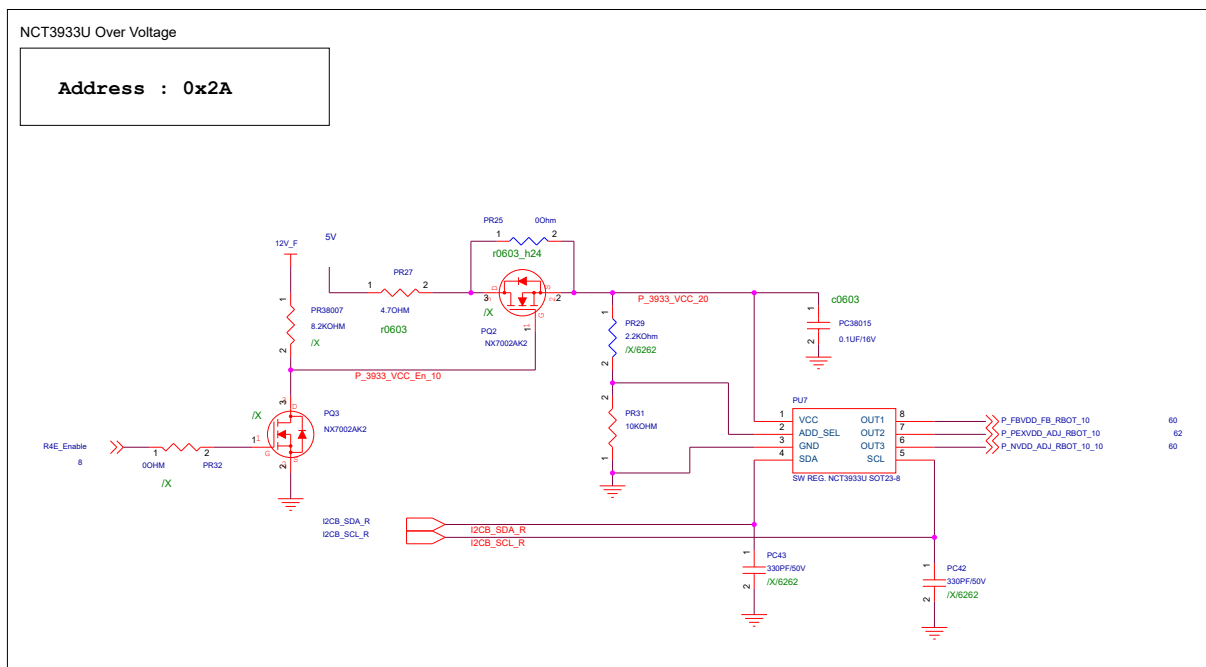
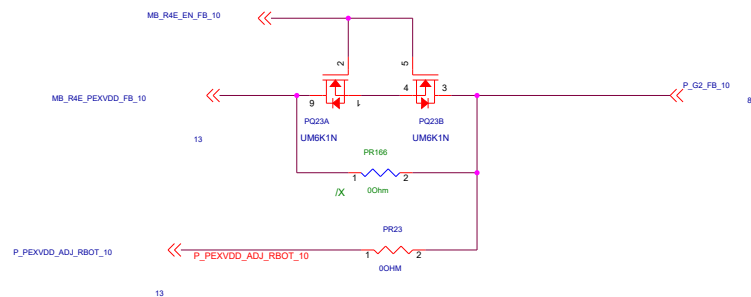
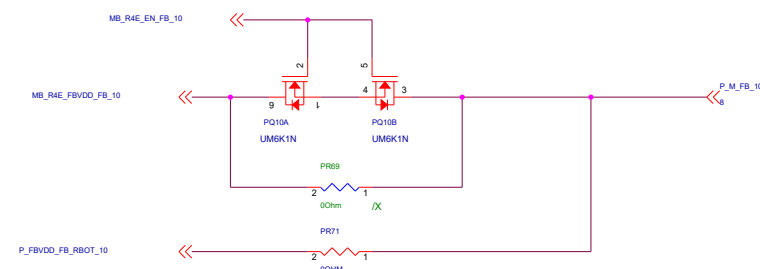
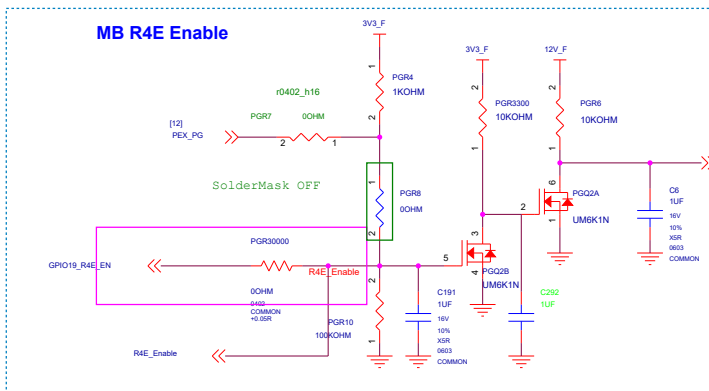
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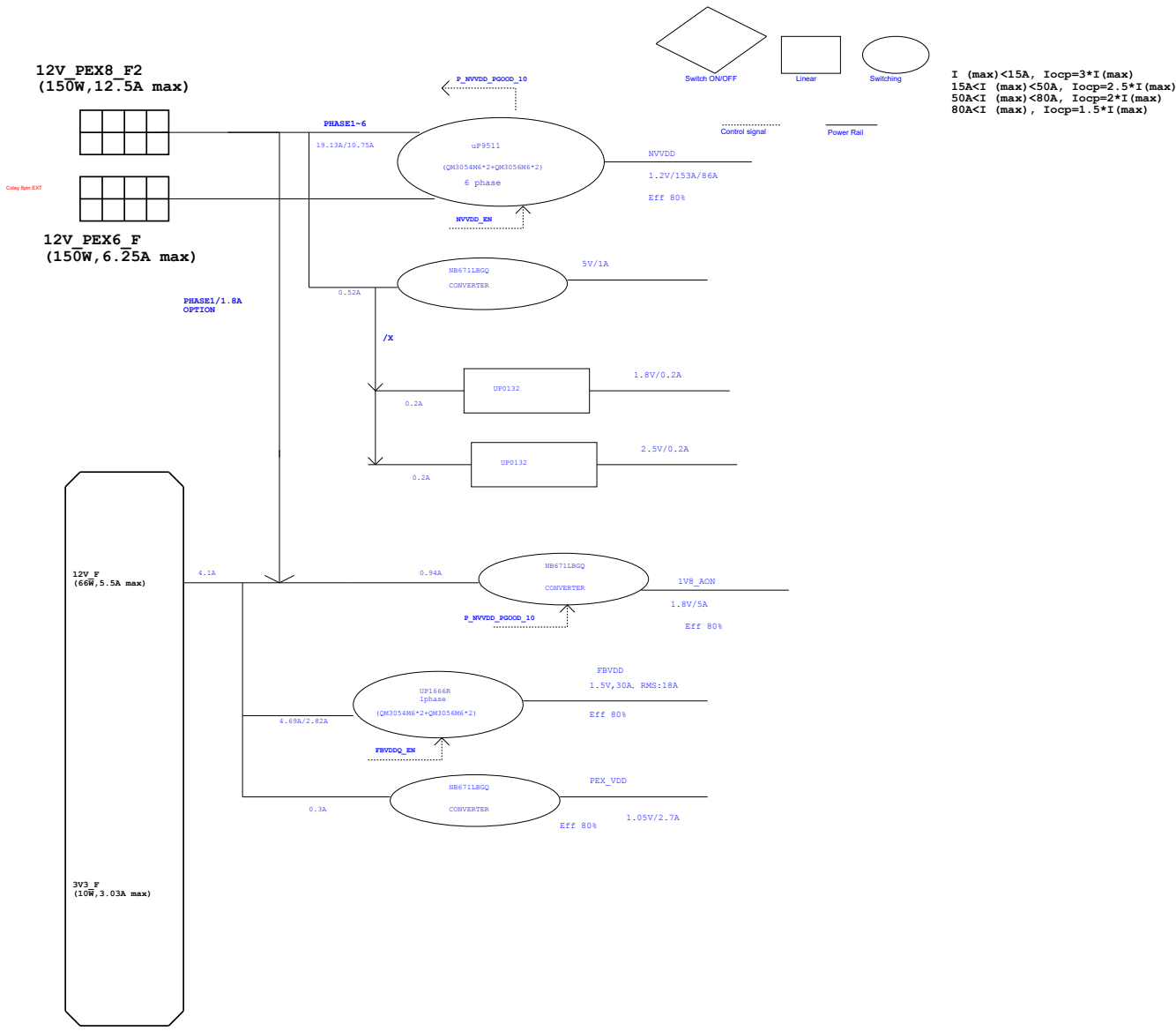


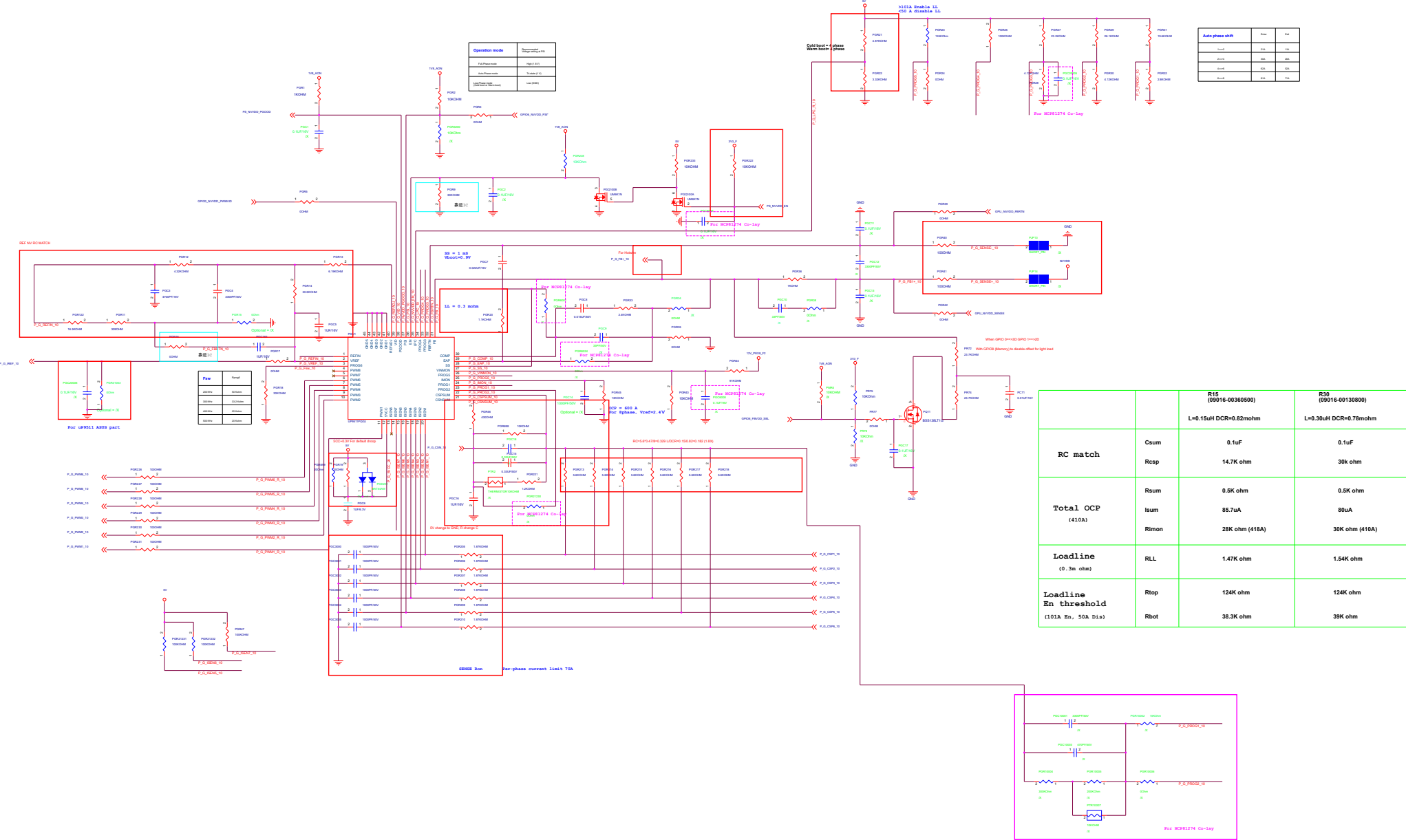


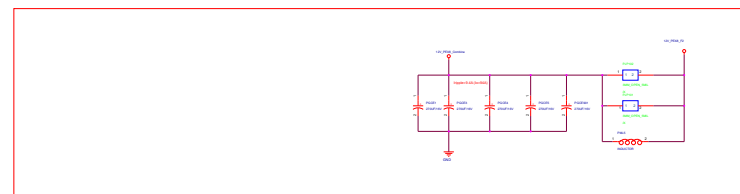
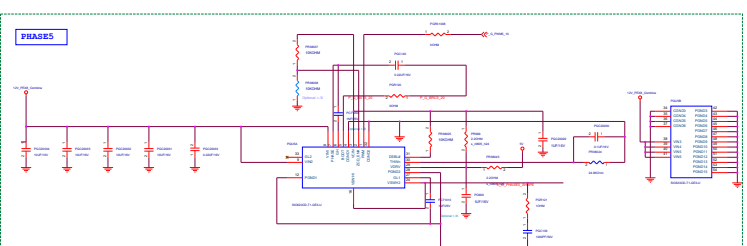


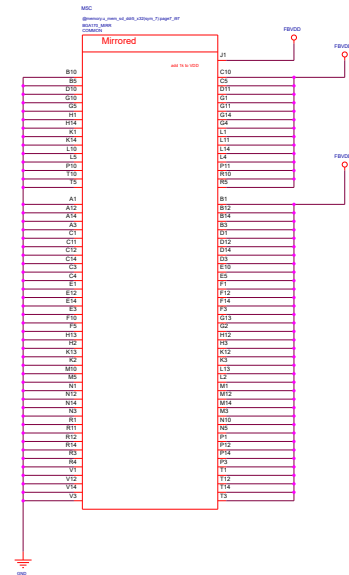
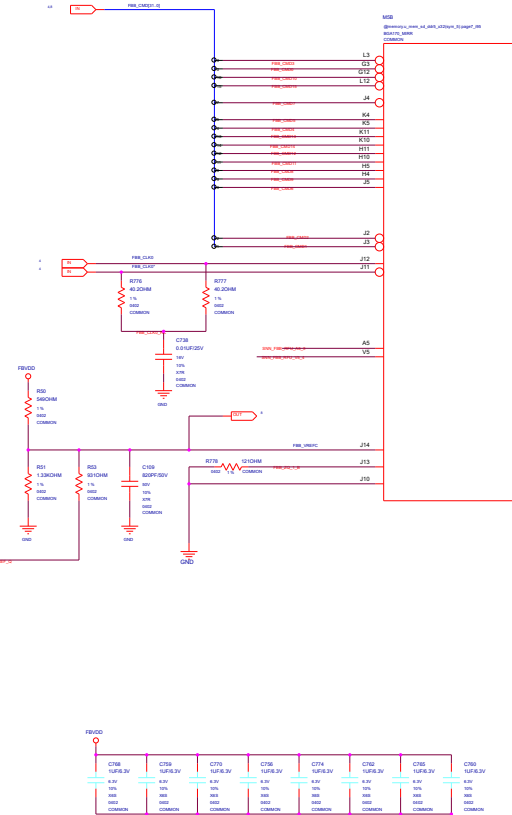













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