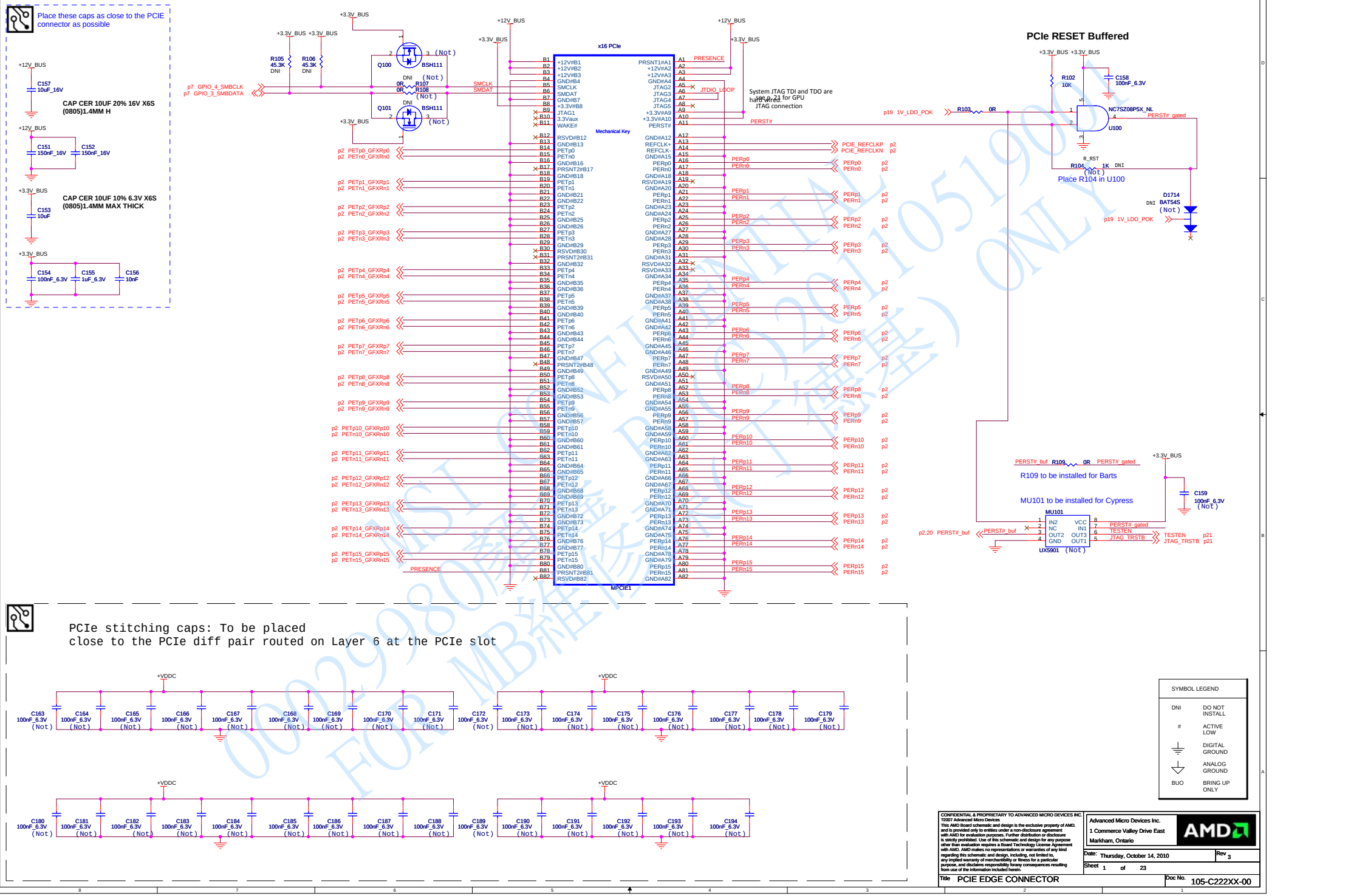
PCI-EXPRESS EDGE CONNECTOR



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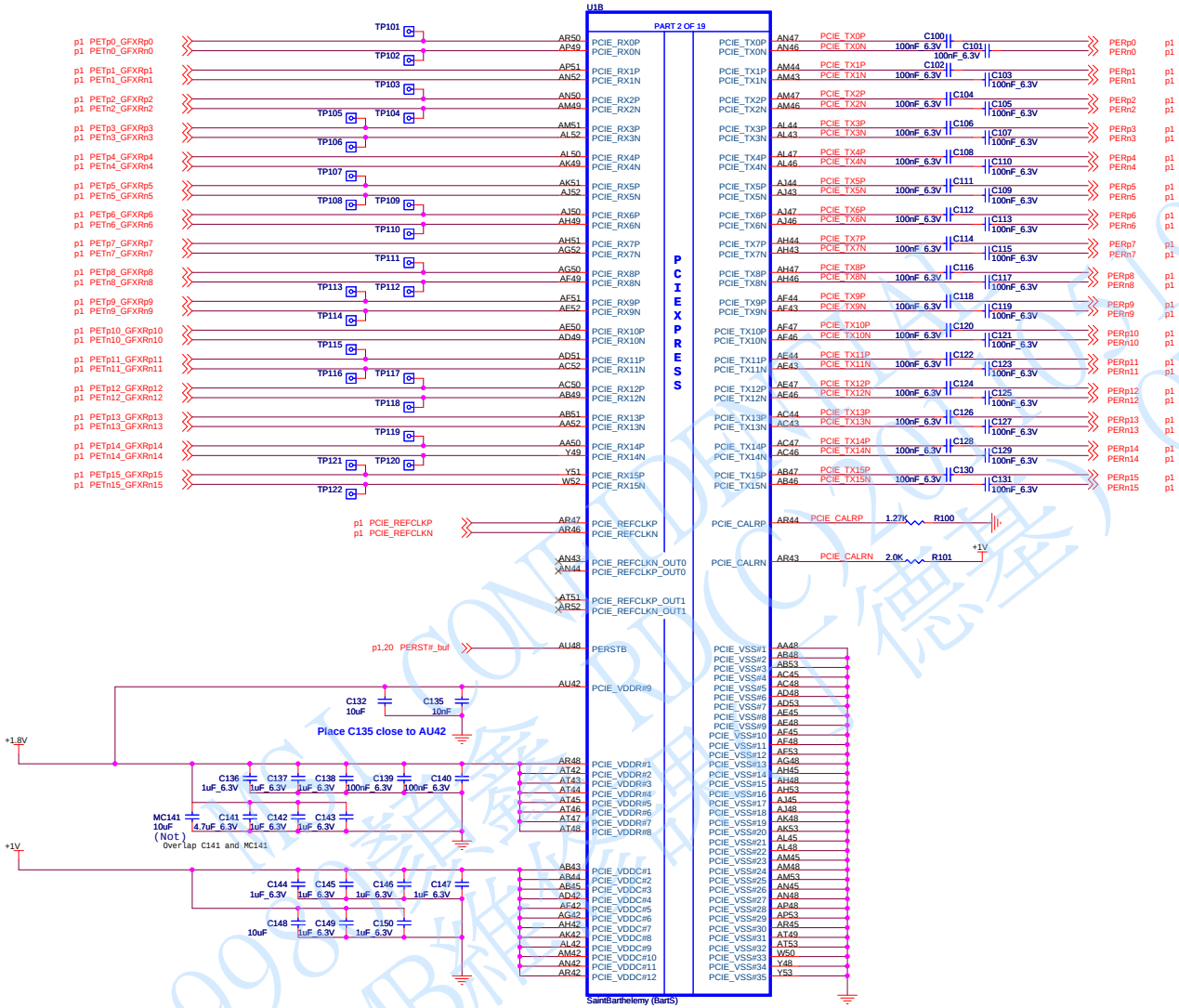
Date:	Thursday, October 14, 2010
Rev	3
Sheet	1 of 23
Title	PCIE EDGE CONNECTOR
Doc No.	105-C222XX-00

(2) BARTS/ CYPRESS PCIE Interface

NOTE: Some of the PCIE testpoints will be available through vias on traces.



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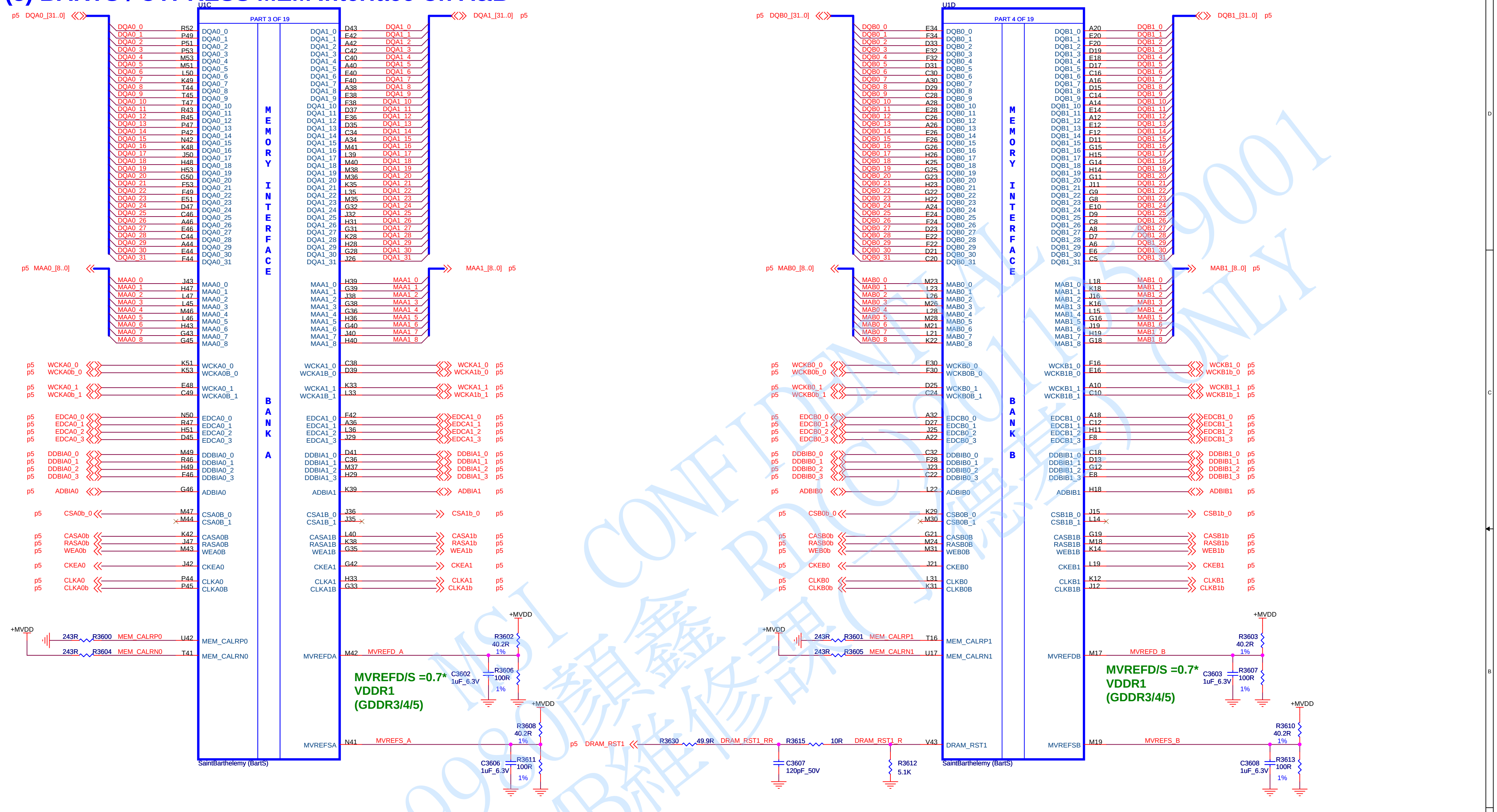
Date:	Thursday, October 14, 2010
Rev	1
Sheet	2 of 23
Title	ASIC PCIE Interface
Doc No.	105-C222XX-00B

(3) BARTS / CYPRESS MEM Interface Ch A&B



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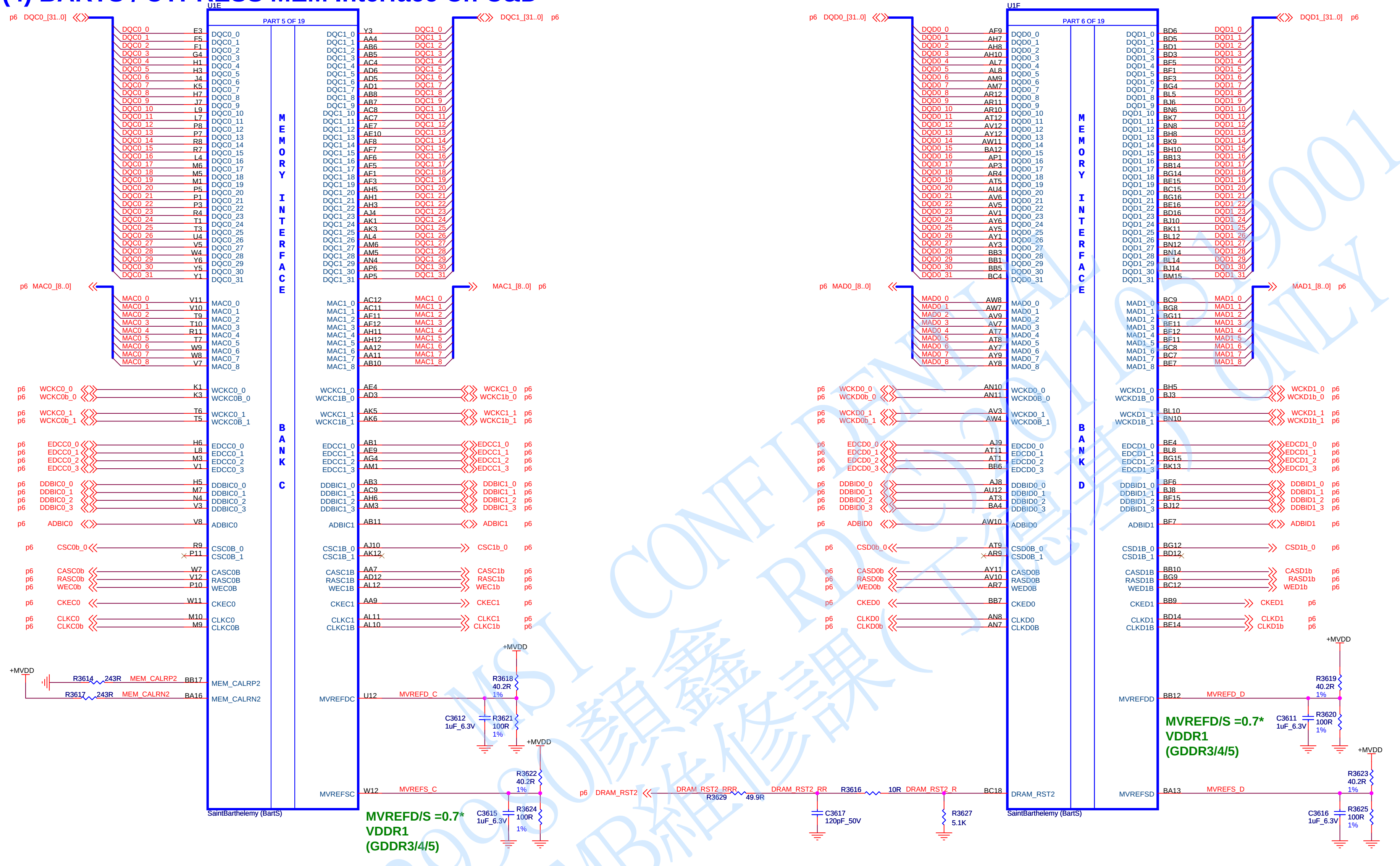
Date:	Thursday, October 14, 2010
Rev	1
Sheet	3 of 23
Title	ASIC Memory Ch A & B
Doc No.	105-C222XX-00B

(4) BARTS / CYPRESS MEM Interface Ch C&D



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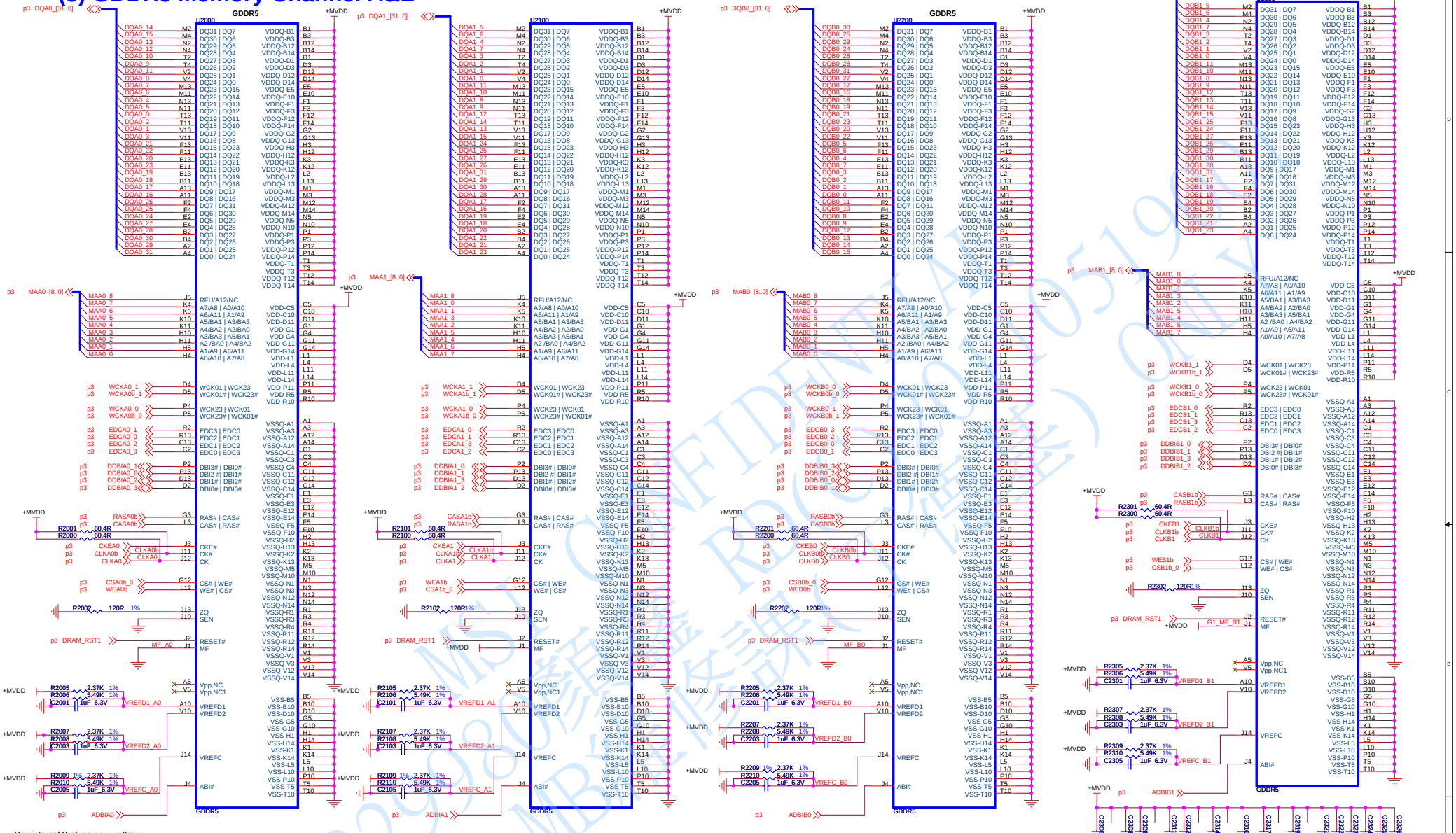
Date: Thursday, October 14, 2010	Rev 1
Sheet 4 of 23	
Title ASIC Memory Ch C & D	Doc No. 105-C222XX-00B

(5) GDDR5 Memory Channel A&B



Use internal Vref memory voltage

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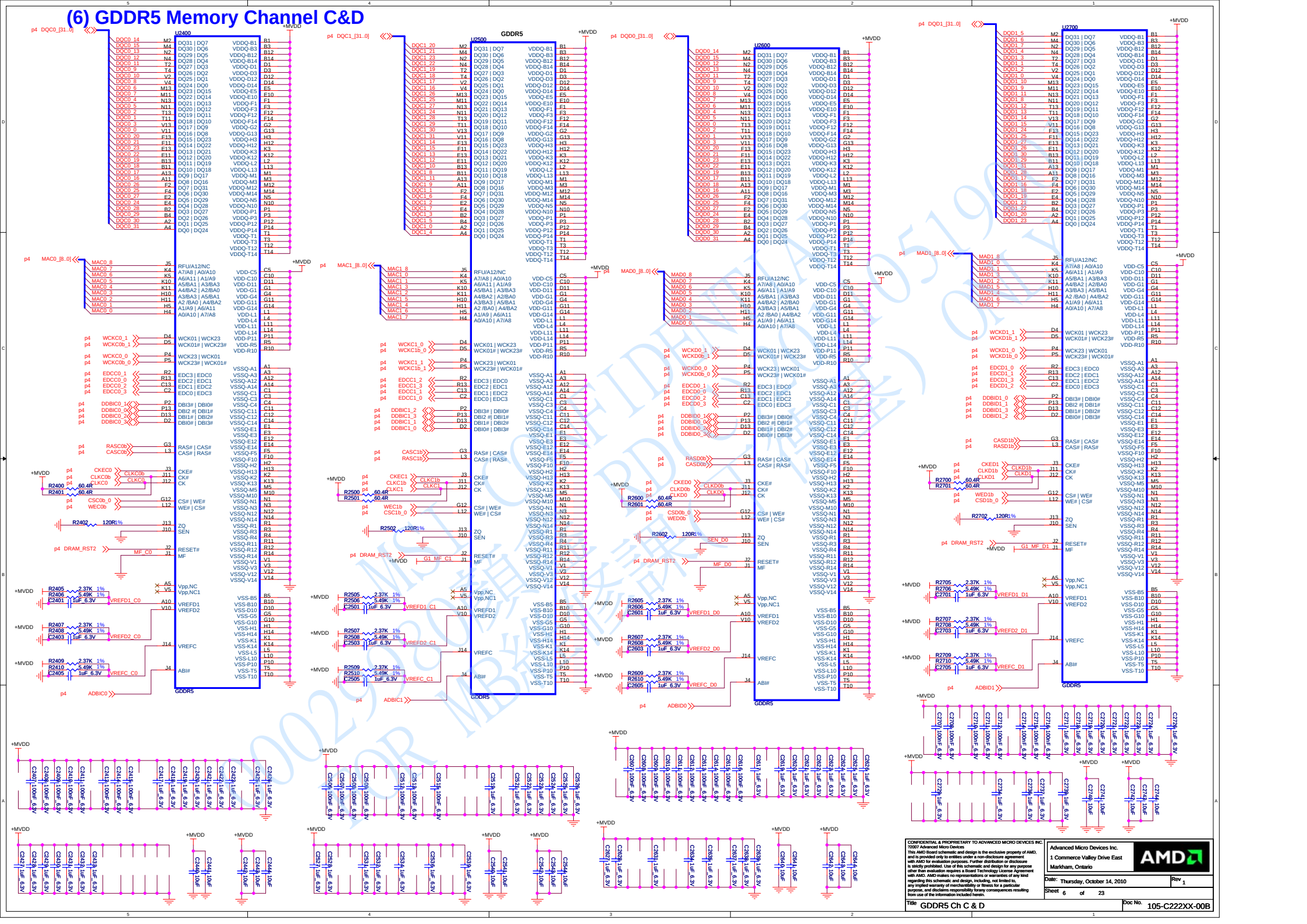
Date:	Thursday, October 14, 2010
Rev	1
Sheet	5 of 23
Title	GDDR5 Ch A & B
Doc No.	105-C222XX-00B

(6) GDDR5 Memory Channel C&D



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Date:	Thursday, October 14, 2010
Rev	1
Sheet	6 of 23
Title	GDDR5 Ch C & D
Doc No.	105-C222XX-00B

(07) BARTS / Cypress GPIOs Strap CF XTAL OSC

PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

9/16:add_ dual VBIOS _circuit

SCL / SDA BUS:

I2C Address	Function	Device
0x60	Chil VDDC REG	

DDC6 BUS:

I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

PWRGOOD must be connected to GND for normal operation

PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO(13,12,11) - CONFIG[2..0]

CONFIG[2]	100 - 512Kbit	M25P05A	(ST)
	101 - 1Mbit	M25P10A	(ST)
CONFIG[1]	101 - 2Mbit	M25P20	(ST)
	101 - 4Mbit	M25P40	(ST)
CONFIG[0]	101 - 8Mbit	M25P80	(ST)
	100 - 512Kbit	Pm25LV512	(Chingis)
	101 - 1Mbit	Pm25LV010	(Chingis)

RESERVED:
Internal use only. Other logic must not affect these signals during RESET.

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

RESERVED:
STRAP_BIOS_ROM_EN
CLKREQ# that requires open drain connection, and cannot be used as pinstrap
Don't set high at reset

CrossFire Card-Edge

Lower Cable Card Edge

Place the crossfire testpoints near the ASIC and not the connector

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

9/15: copy layout

Keep XIN_OSC and XOUT_OSC as short as possible to minimize stray capacitance

Share pad R26 and R19

Divider for 1.8V signaling.

route 50ohms single-ended/100ohms diff and keep short

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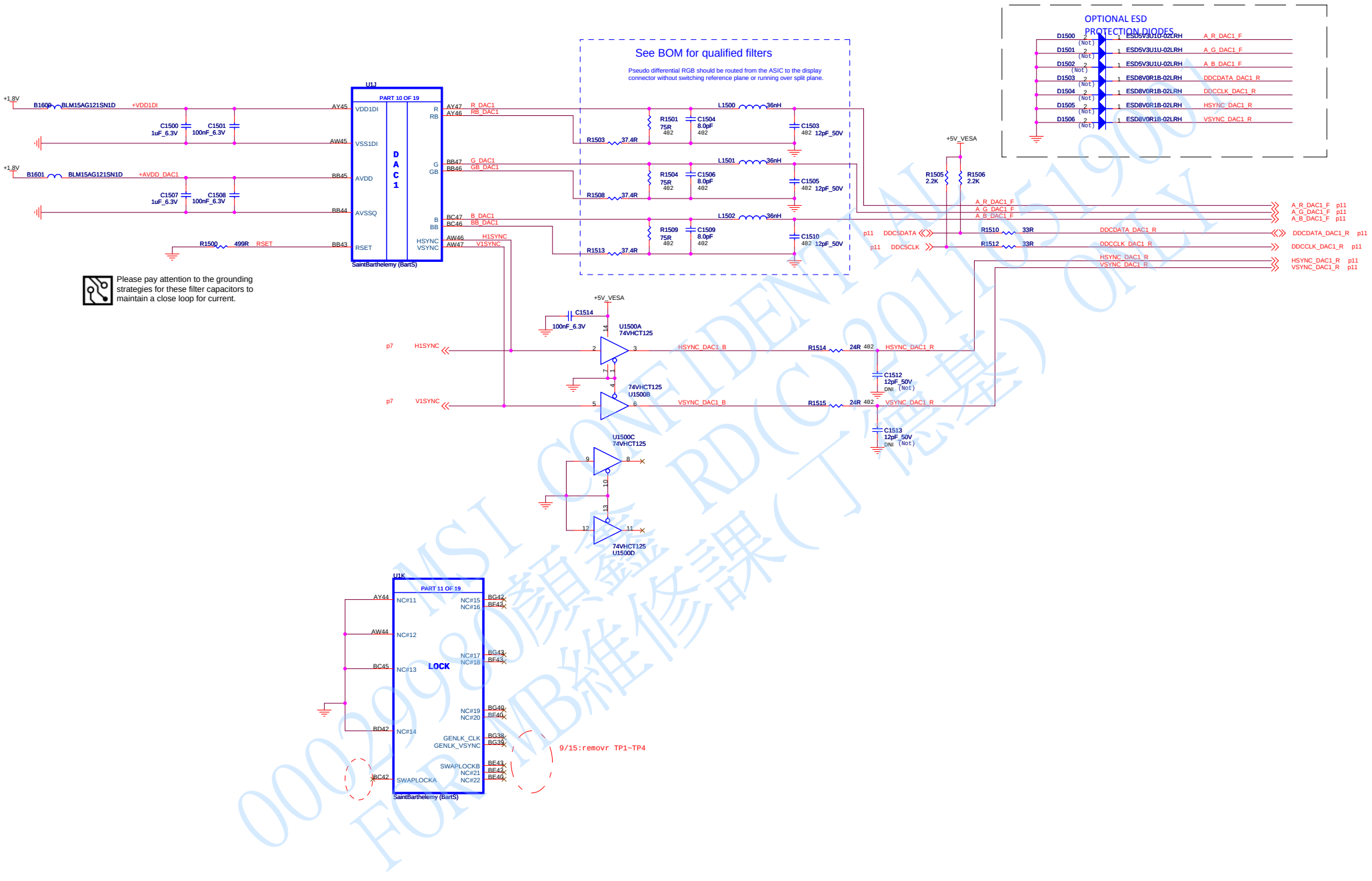
Date:	Thursday, October 14, 2010
Rev	1
Sheet	7 of 23
Title	ASIC GPIO, STRAPS,CF, and XTAL
Doc No.	105-C222XX-00B

(08) BARTS / CYPRESS DAC1



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Date:	Thursday, October 14, 2010
Rev	1
Sheet	8 of 23
Title	Power Management
Doc No.	105-C222XX-00B

(09) BARTS / CYPRESS TMDS A&B

HDMI/DVI MUX:
0.1uF cap to be used, placed close to VDD power pins
Place 1x to top and 1x to bottom of the package
Use 5 ground vias for the ground pad: 1 via at each corner of the ground pad and 1 in the center of the ground pad
TDFN package to be used: 2600009800G
SEL is 1.8V only

Disp. Out	DVI	HDMI
SEL	0	1

PLEASE NOTE +5V NEEDS TO HAVE A SEPARATE REGULATOR FOR HDMI!

OVERLAP HDMI WITH DP

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

Optional ESD protection dioes

TOP

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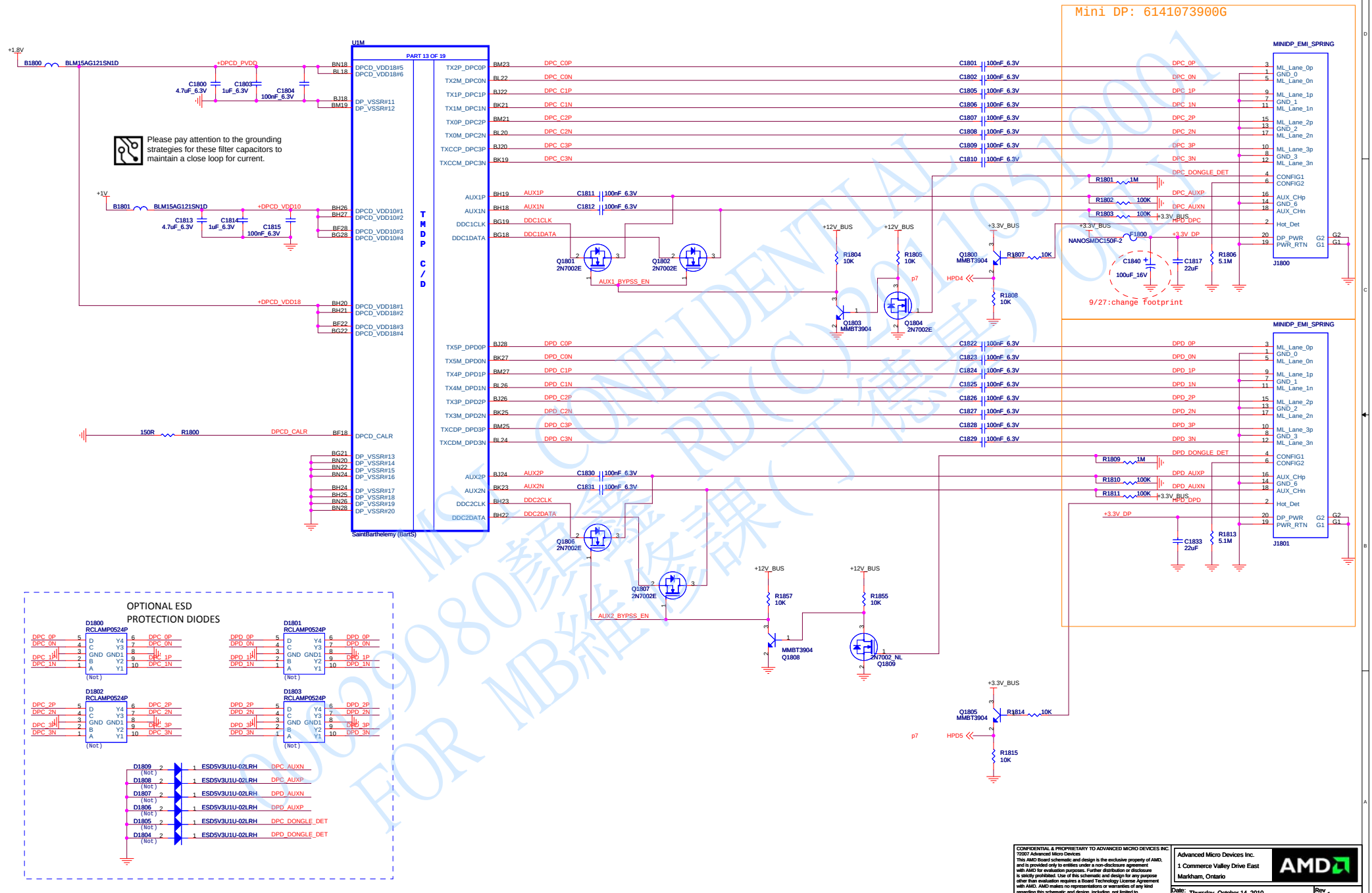
Date: Thursday, October 14, 2010 Rev 1
Sheet 9 of 23
Title ASIC TMDS AB
Doc No. 105-C222XX-00B

(10) BARTS / CYPRESS Display Port/HDMI C&D



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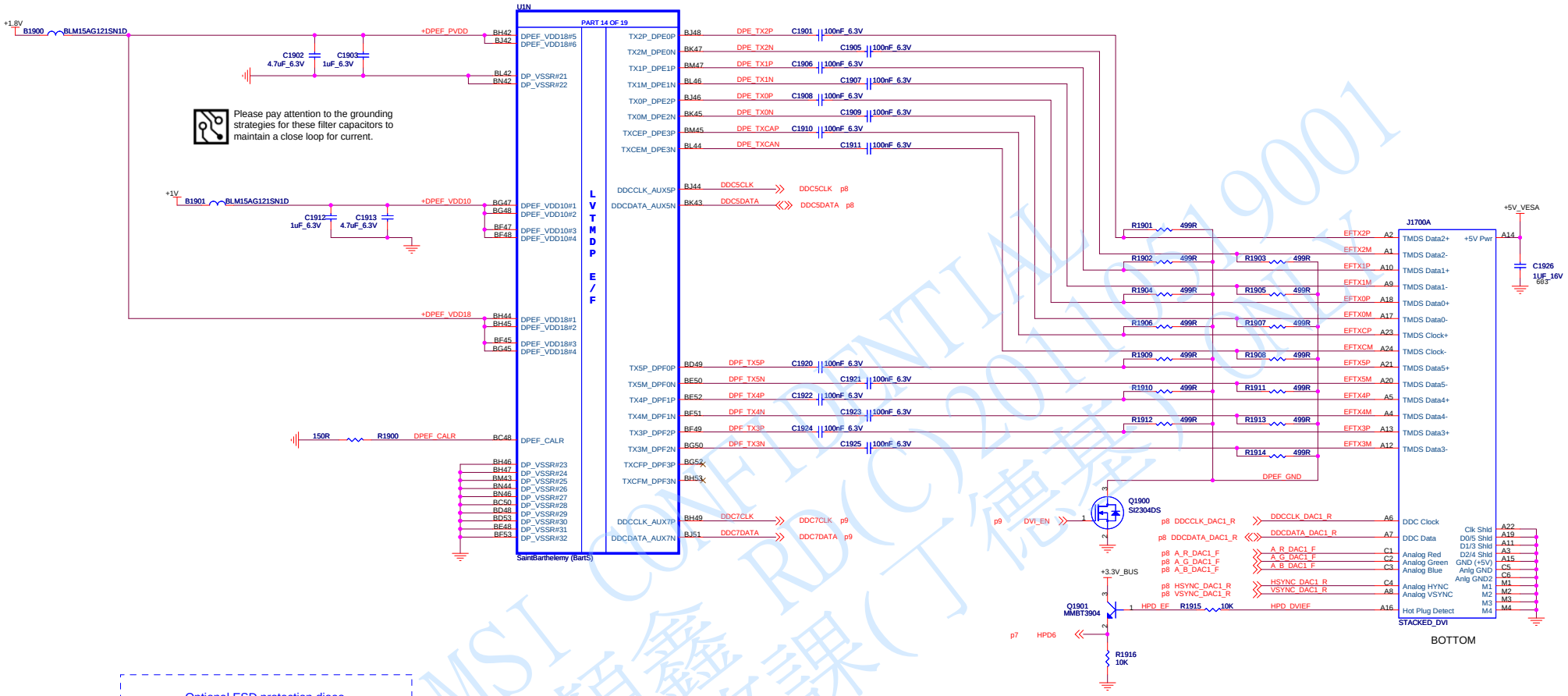
Date:	Thursday, October 14, 2010
Rev	1
Sheet	10 of 23
Title	ASIC DP C,D
Doc No.	105-C222XX-00B

(11) BARTS / CYPRESS LVTMDP E&F



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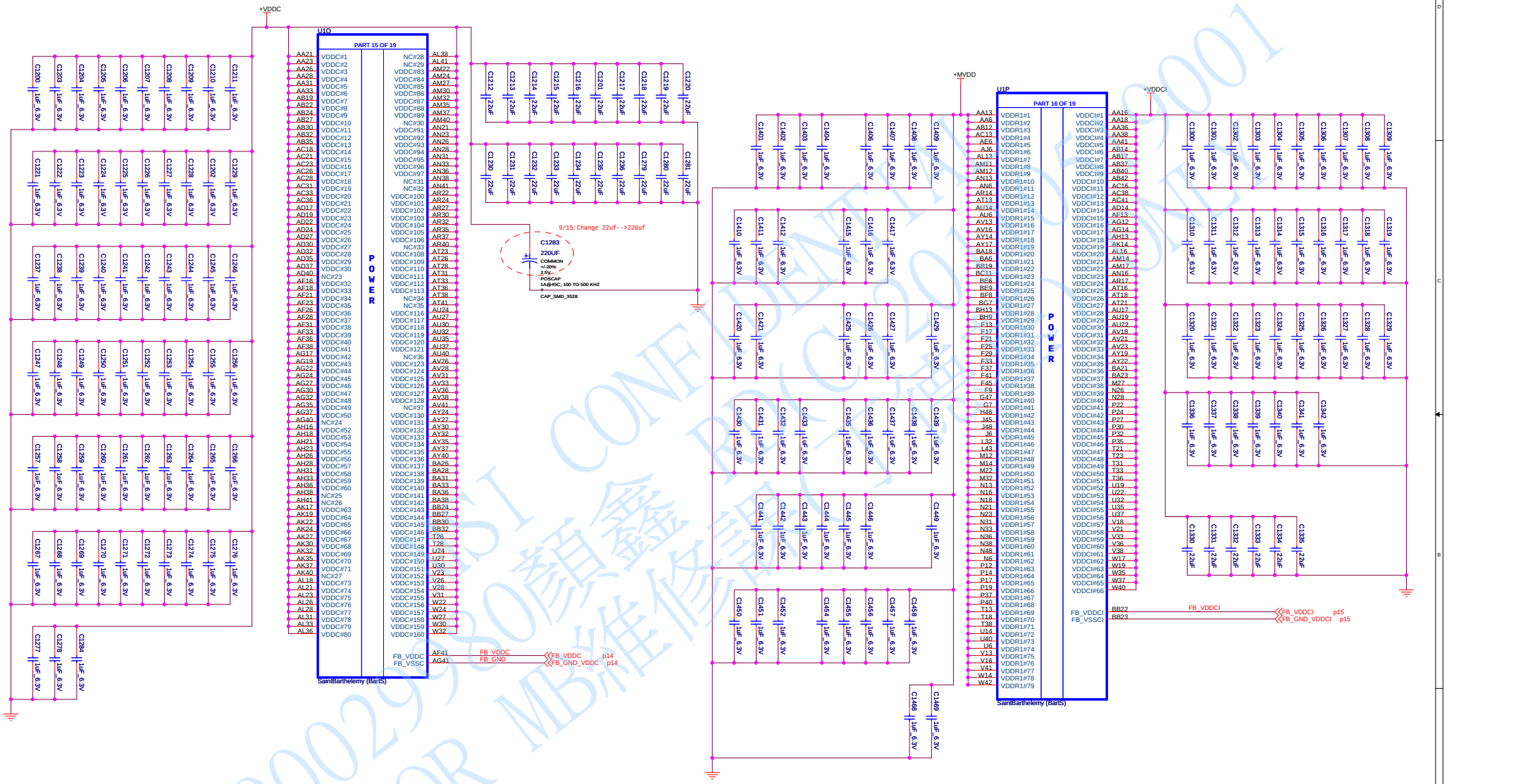
Date:	Thursday, October 14, 2010
Rev	1
Sheet	11 of 23
Title	ASIC TMDS EF
Doc No.	105-C222XX-00B

(12) BARTS / CYPRESS Power



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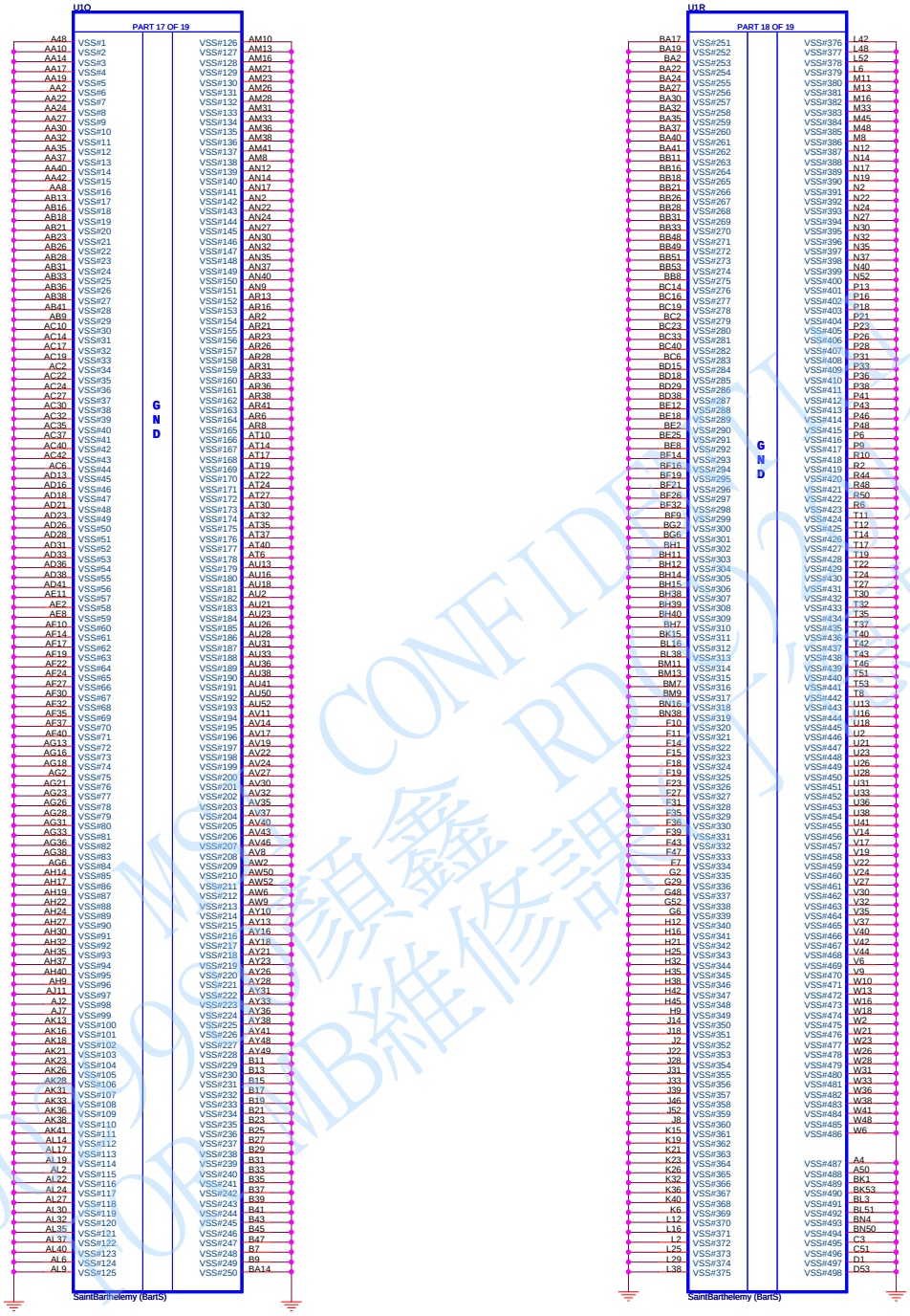
Date:	Thursday, October 14, 2010
Rev	1
Sheet	12 of 23
Title	ASIC POWER
Doc No.	105-C222XX-00B

(13) BARTS / CYPRESS GND



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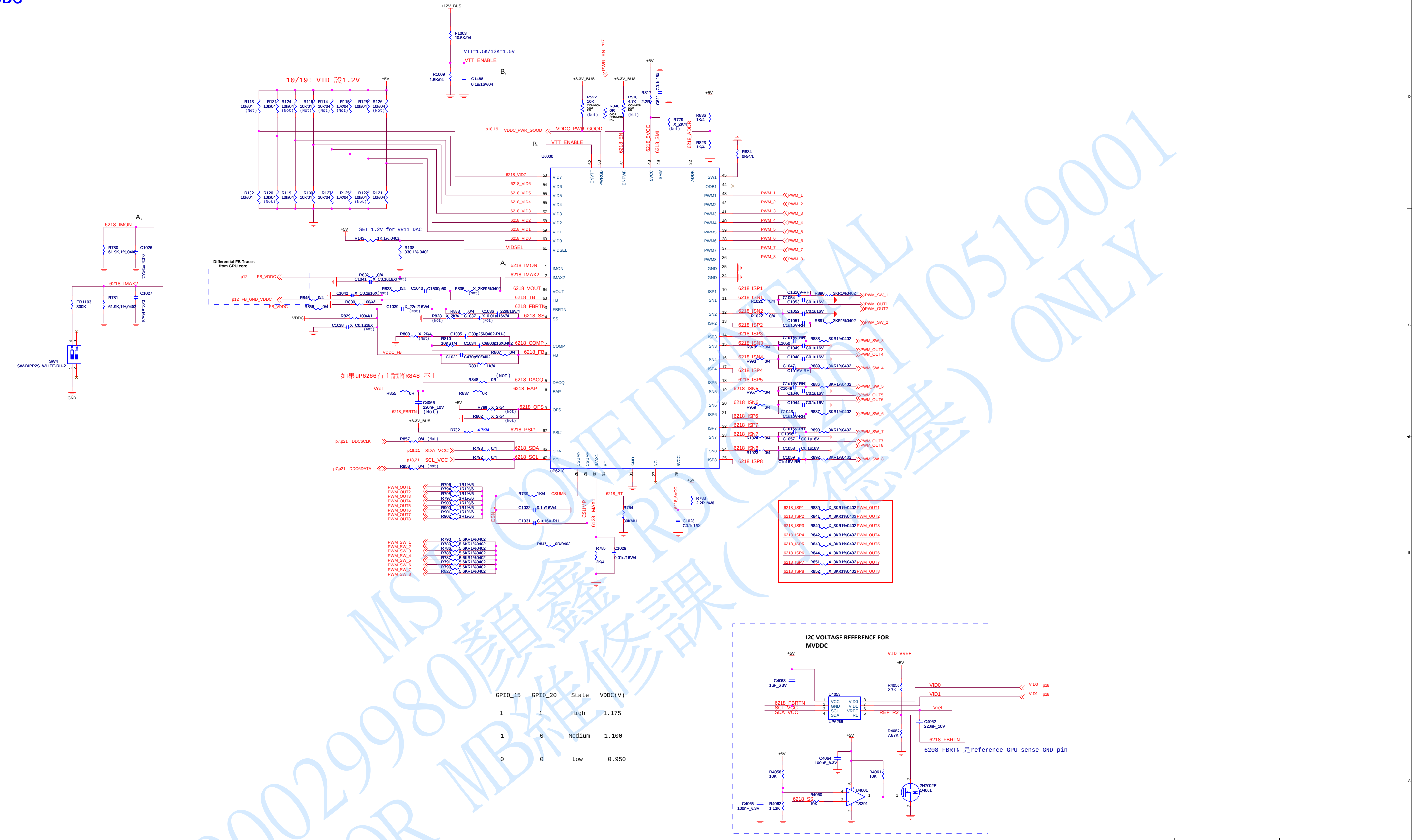
Date:	Thursday, October 14, 2010
Rev	1
Sheet	13 of 23
Title	ASIC GND
Doc No.	105-C222XX-00B

(14) VDDC



GPIO_15	GPIO_20	State	VDDC(V)
1	1	High	1.175
1	0	Medium	1.100
0	0	Low	0.950

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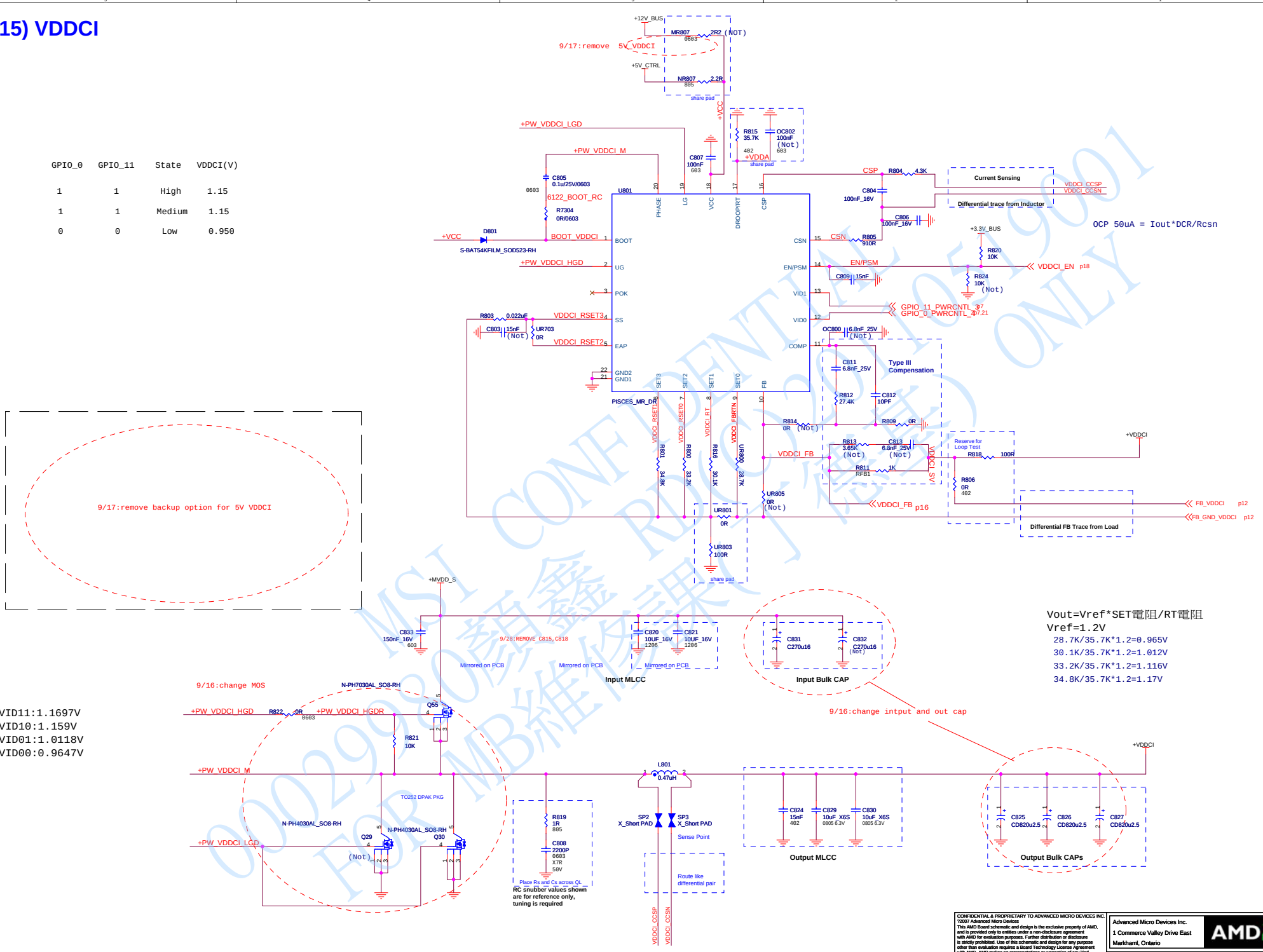
Date: Friday, November 26, 2010
Rev 1
Sheet 14 of 23
Title VDDC
Doc No. 105-C222XX-00B

(15) VDDCI

GPIO_0	GPIO_11	State	VDDCI(V)
1	1	High	1.15
1	1	Medium	1.15
0	0	Low	0.950



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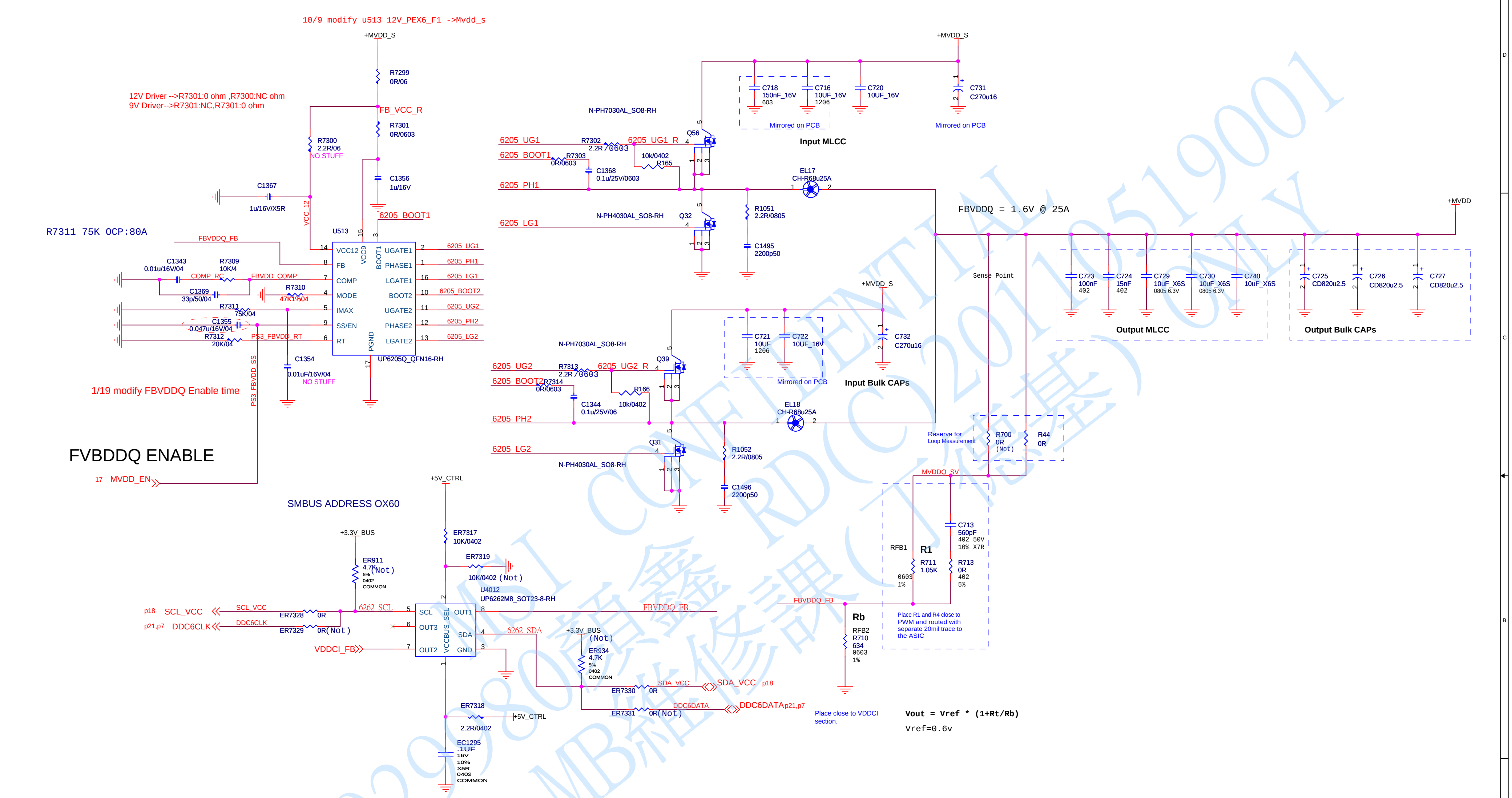
Date: Friday, November 26, 2010 Rev 1
Sheet 15 of 23
Title VDDCI Doc No. 105-C222XX-00B

(16) MVDD



Layout guideline

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

Resistors to set the output voltages for +VDDCI and +MVDD .

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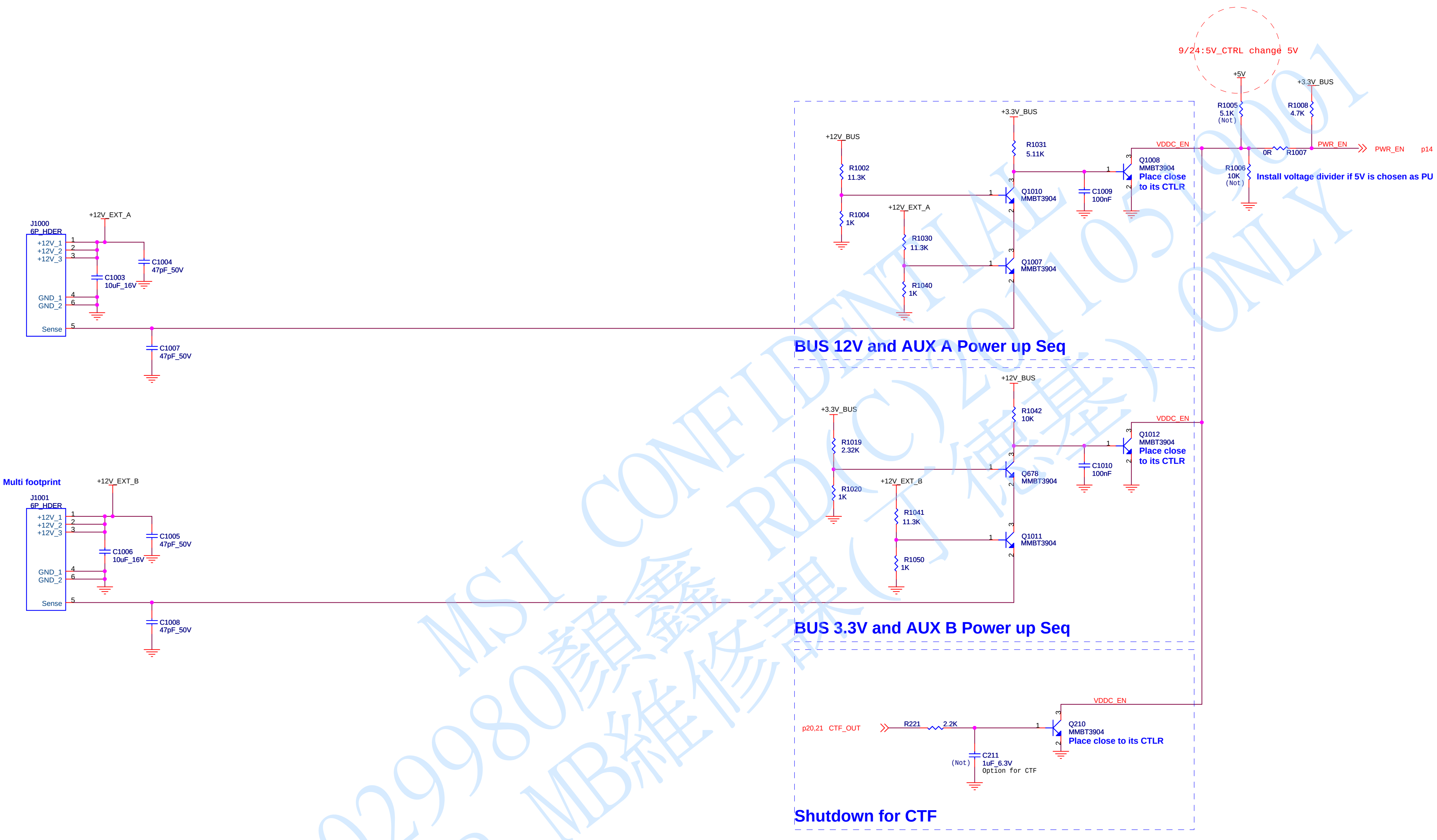
Date:	Monday, October 18, 2010
Rev	1
Sheet	16 of 23
Title	MVDD
Doc No.	105-C222XX-00B

(19) BARTS / CYPRESS POWER MGMNT



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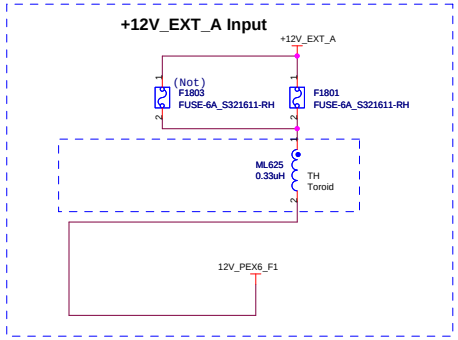
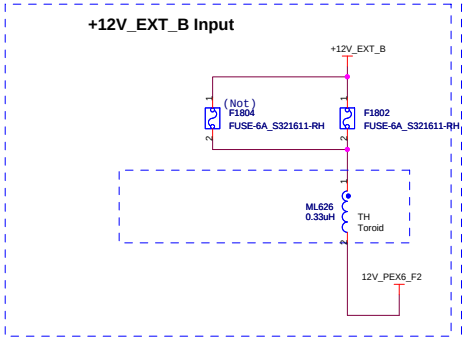
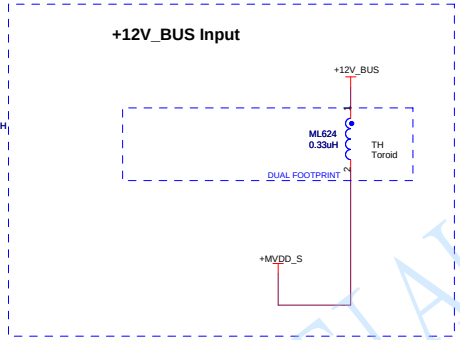
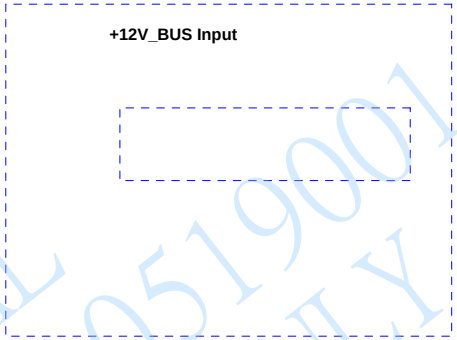
Date: Thursday, October 14, 2010		Rev 1
Sheet 17 of 23		
Title Power Management		Doc No. 105-C222XX-00B

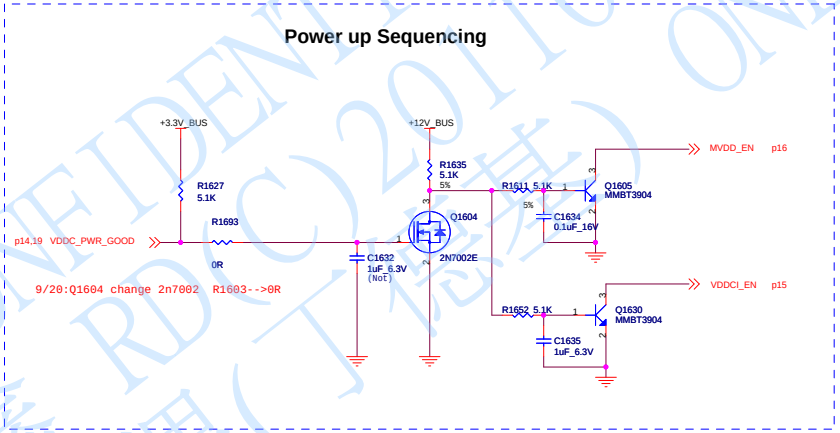
(17) BARTS / CYPRESS VDDCI POWER PLAY

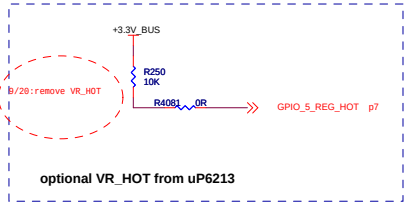


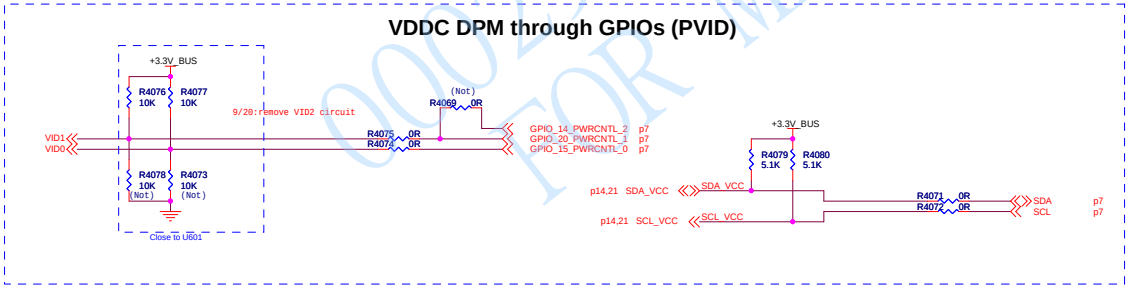












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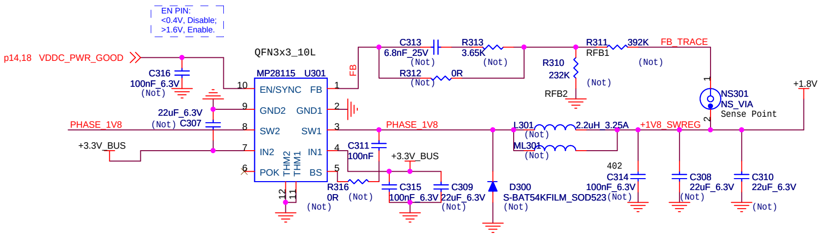
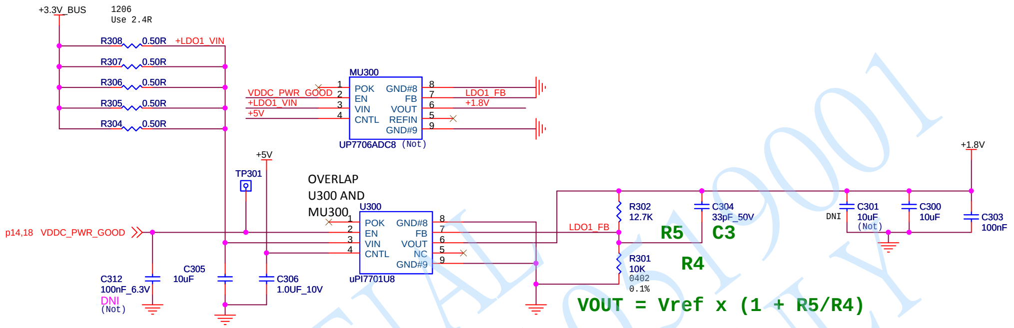
Date:	Thursday, October 14, 2010
Rev	1
Sheet	18 of 23
Title	Power Management 2
Doc No.	105-C222XX-00B

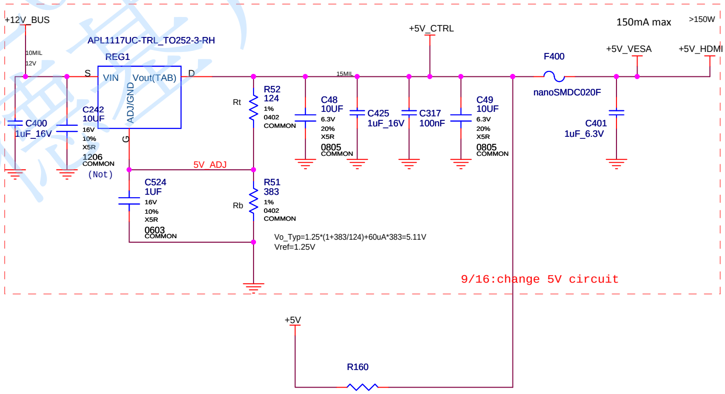
(18) BARTS / CYPRESS Small Rail Regulators

LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

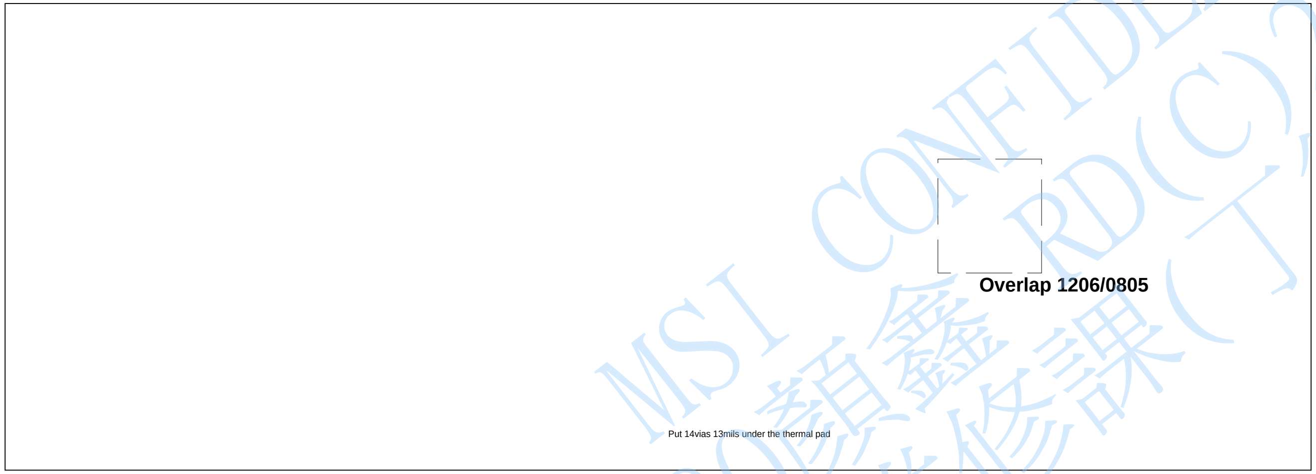




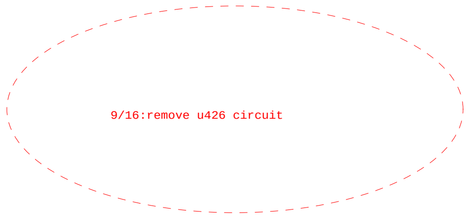
Regulators for +5V, +5V_VESA and +5V_HDMI
Iout max = 150mA (DVI+HDMI)



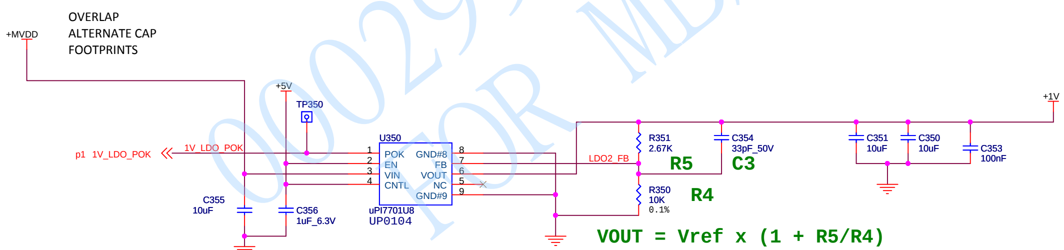
Other cheaper solution at 5MHz switching for 1.8V



optional 5V power for VDDC regulator;



LDO #2: Vin = +1.35V to 1.8VMAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



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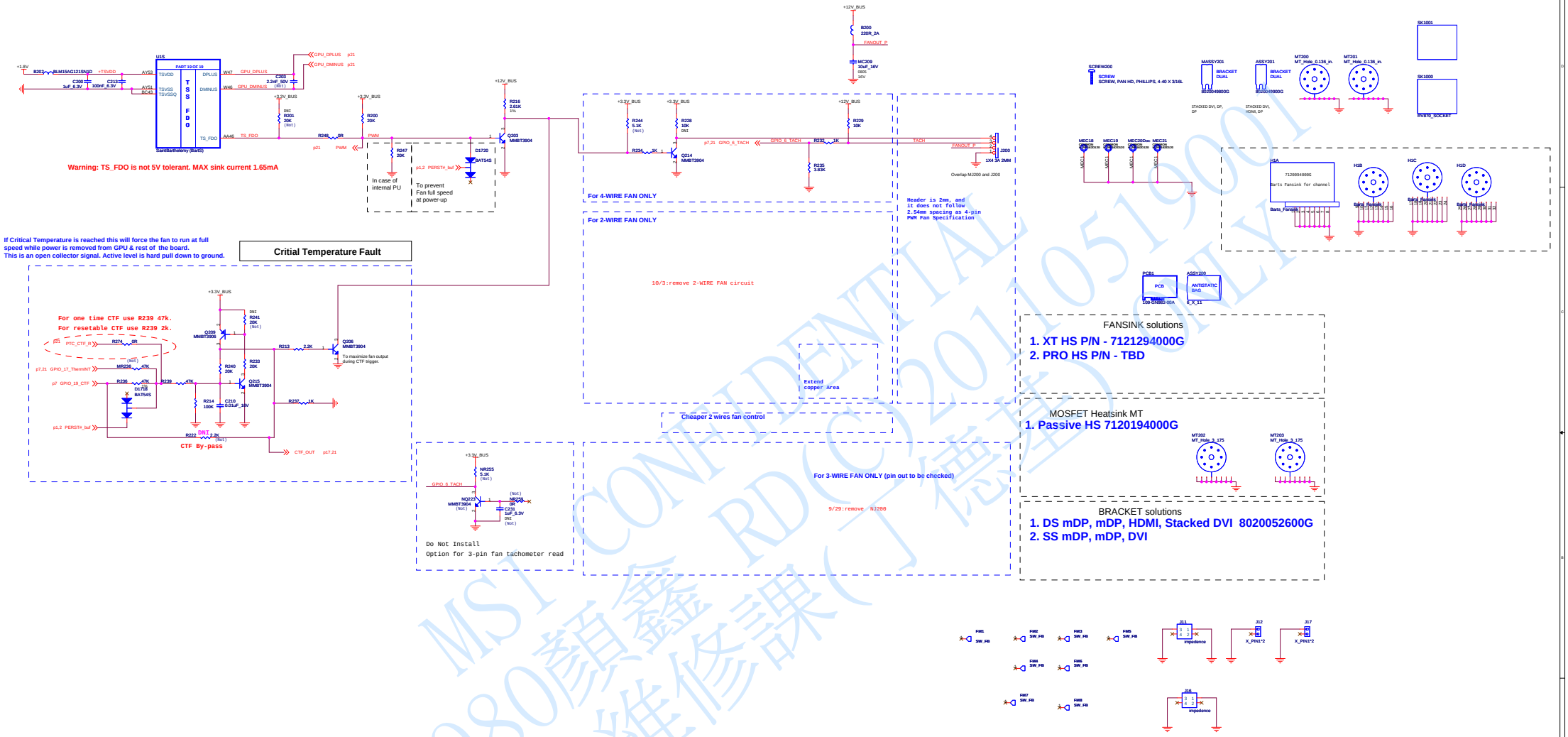
Date: Thursday, October 14, 2010		Rev 1	
Sheet 19 of 23			
Title Small Rail Regulators		Doc No. 105-C222XX-00B	

(20) BARTS / CYPRESS Mechanical and Thermal Management



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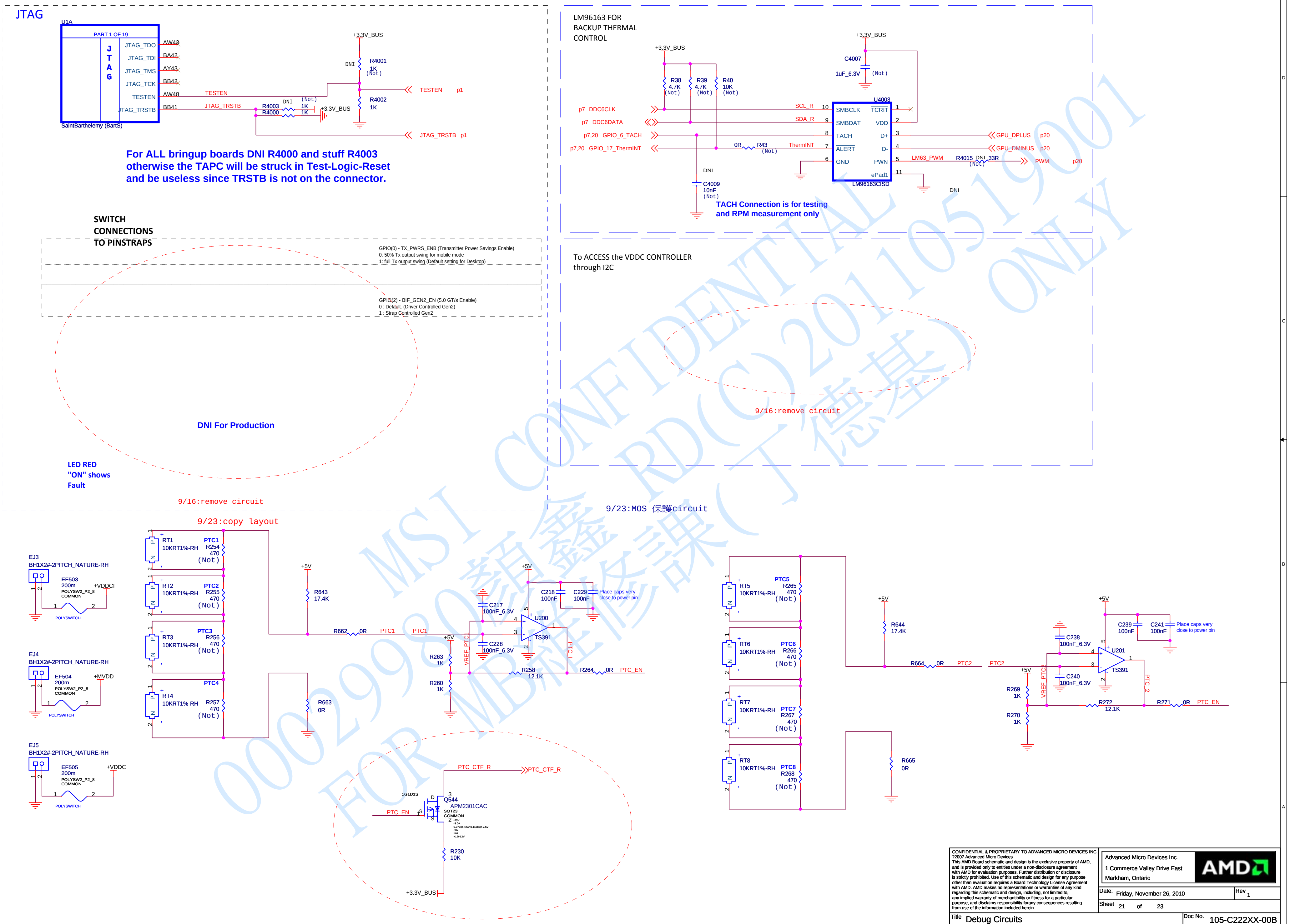
Date: Tuesday, November 30, 2010 Rev: 1
Sheet 20 of 23
Title: Mechanical & Thermal Management
Doc No. 105-C222XX-00B

(21) CYPRESS Debug Circuits



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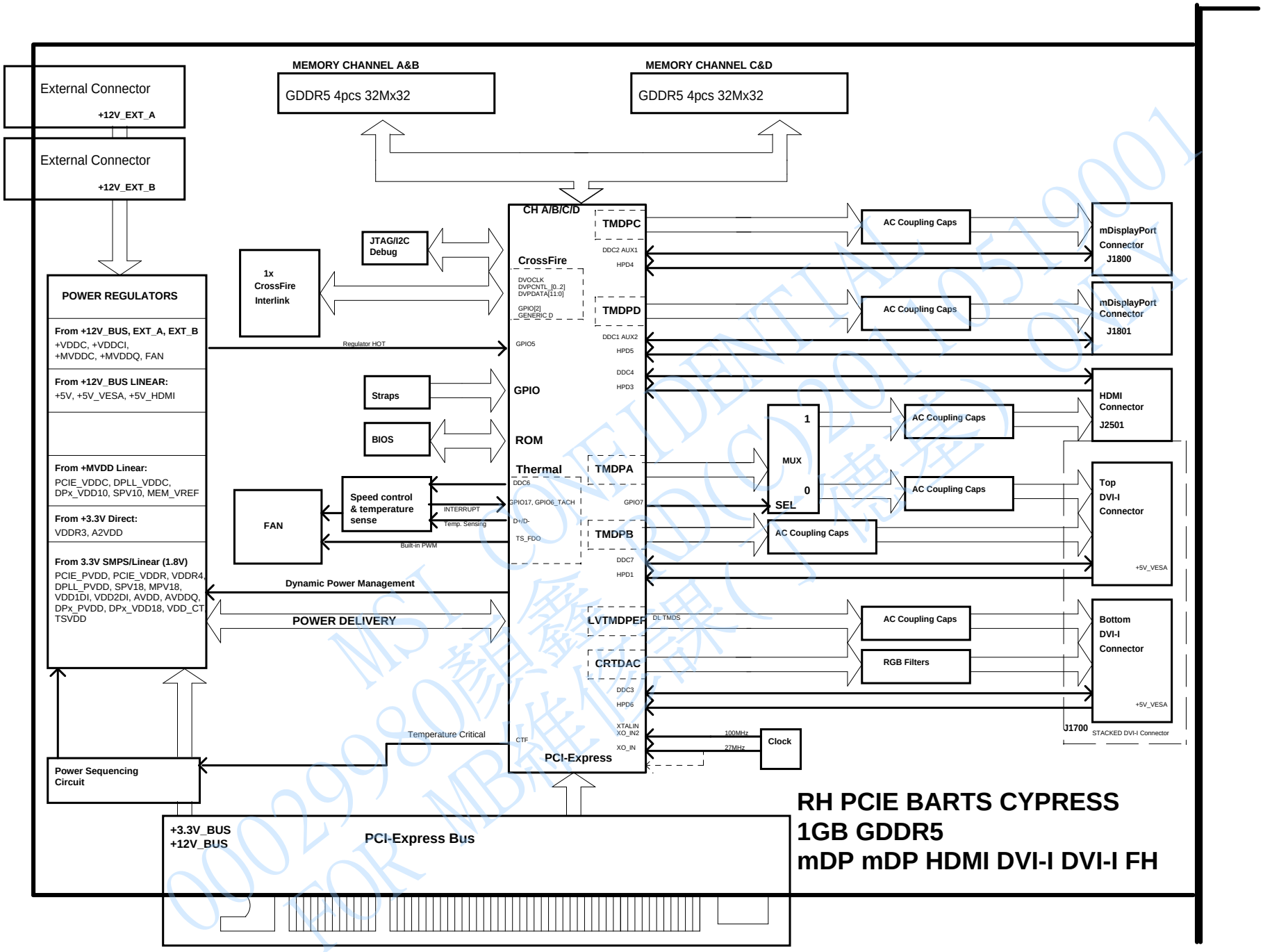
Date: Friday, November 26, 2010	Rev 1
Sheet 21 of 23	
Title Debug Circuits	Doc No. 105-C222XX-00B



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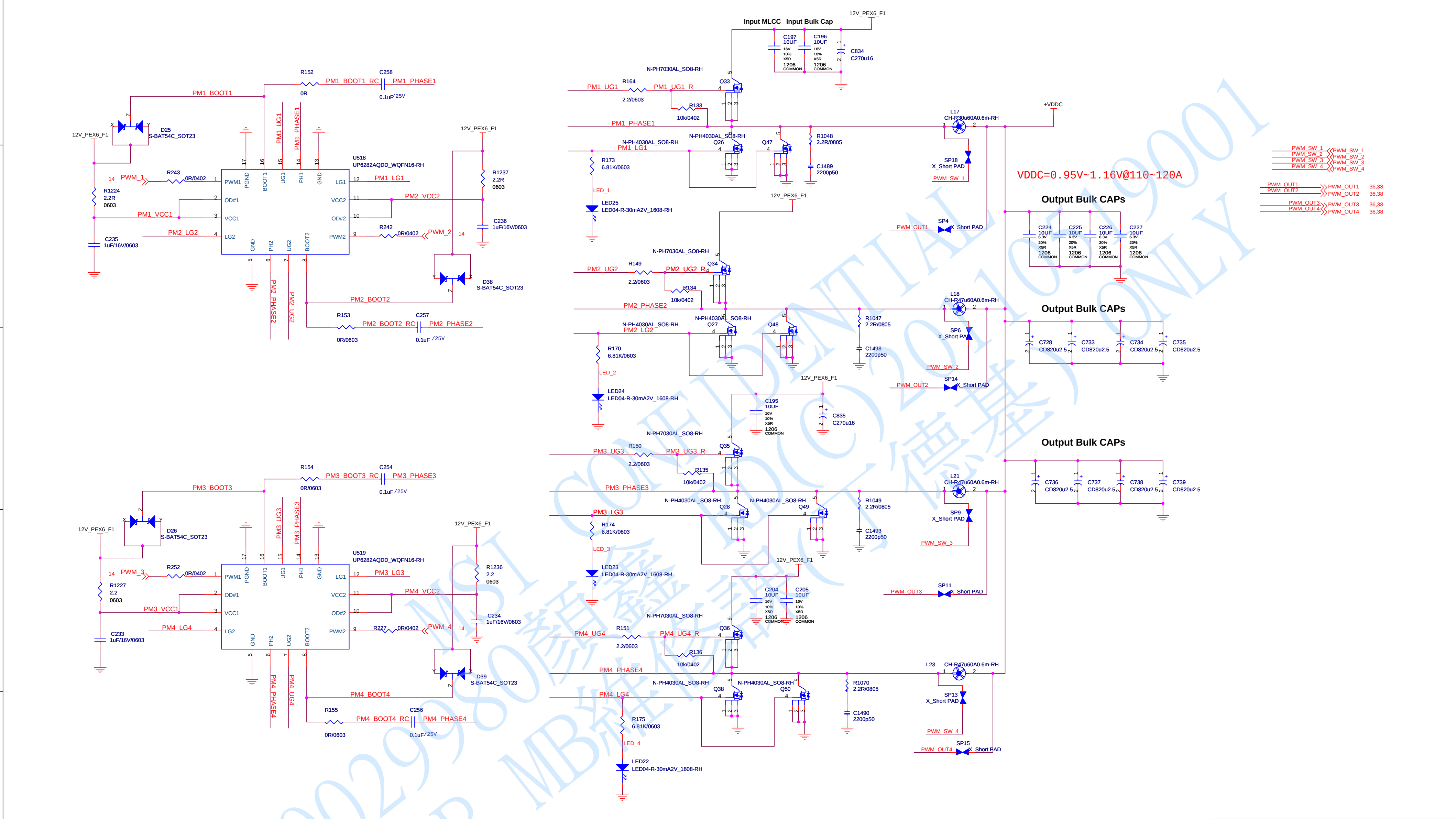
Date:	Thursday, October 14, 2010
Rev	1
Sheet	22 of 23
Title	Block Diagram
Doc No.	105-C222XX-00B

Power Supply: VDDC 1~4 Phase powered from external PEX 8PIN



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 1-2 of 4

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<Title>		
Size: Custom	Document Number: <Doc>	Rev: <RevCode>
Date: Thursday, October 14, 2010	Sheet 22 of 25	

Title	Schematic No.	Date:
RH BARTS CYPRESS GDDR5 mDP-mDP-HDMI-DVII-DVII	105-C222XX-00B	Tuesday, November 30, 2010

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	19/04/2010	Initial release. Based on C220
1	00B	09/08/2010	Page01: Added direct connection from Pull-Up for MU101 for Cypress Page09: remove the inductor for top DVI line Page14: update Q601,Q602,Q603,Q604 symbol Page17: add C211 Page20: add R201, R237, R241. Page18: add optional 3-pin fan tach circuitry; Page50: update block diagram

V251-0A bason C222

Page 07: add dual VBIOS circuit

Page 12: add SP-CAP

page14: change up6218 power circuit

page15:modify up6122 circuit and change choke

page16:change up6205 power circuit

page17: pwr_en power sequency change 3.3V_BUS

page18:change input choke

page19:change 5V and remove u330

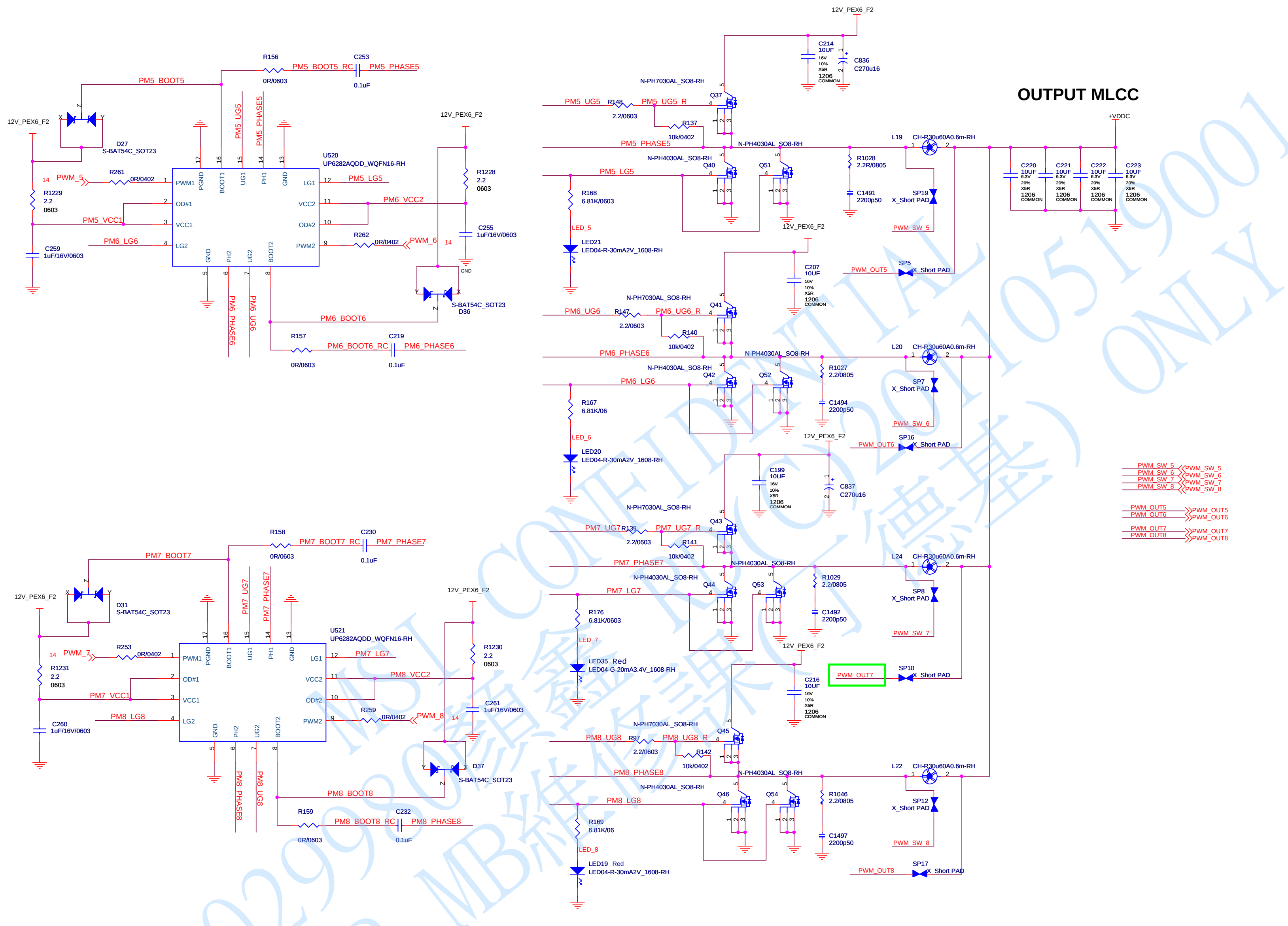
page21:remove LED circuit and switch and j404, add thermal diode for MOS protection

page22/23:add VDDC up6128 driver ciruit

V251-10 bason V251-0A

page21:modify thermal diode for MOS protection

Power Supply: NVVDD Phase 5~8 powered from internal PEX edge connector



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 3-4 of 4

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<Title>		
Size: Custom	Document Number: <Doc>	Rev: <RevCode>
Date: Thursday, October 14, 2010	Sheet 23 of 25	