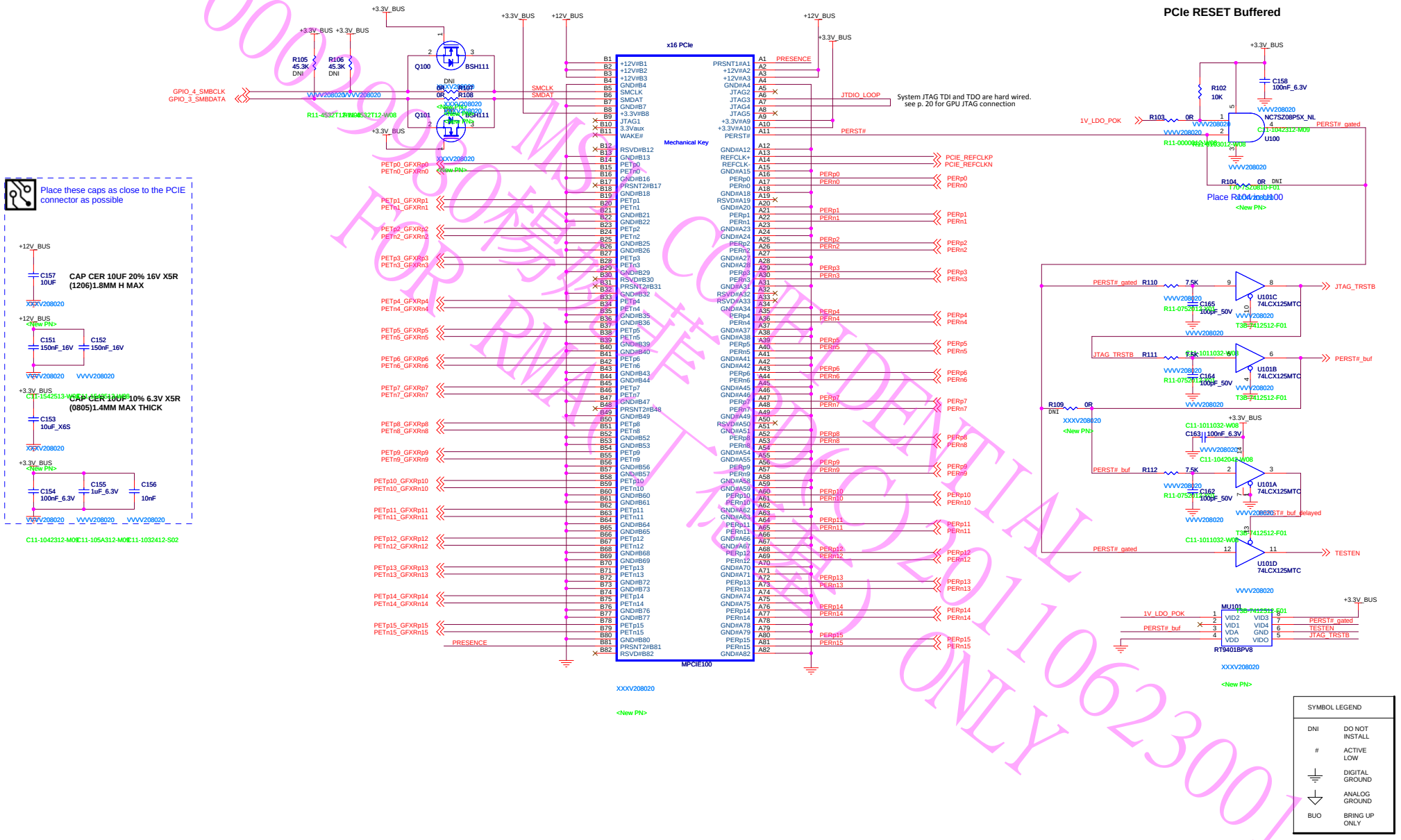
PCI-EXPRESS EDGE CONNECTOR

CORVETTE

1.Add PCIe Reset Buffered Circuit U101,MU101



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(2) JUNIPER PCIe Interface

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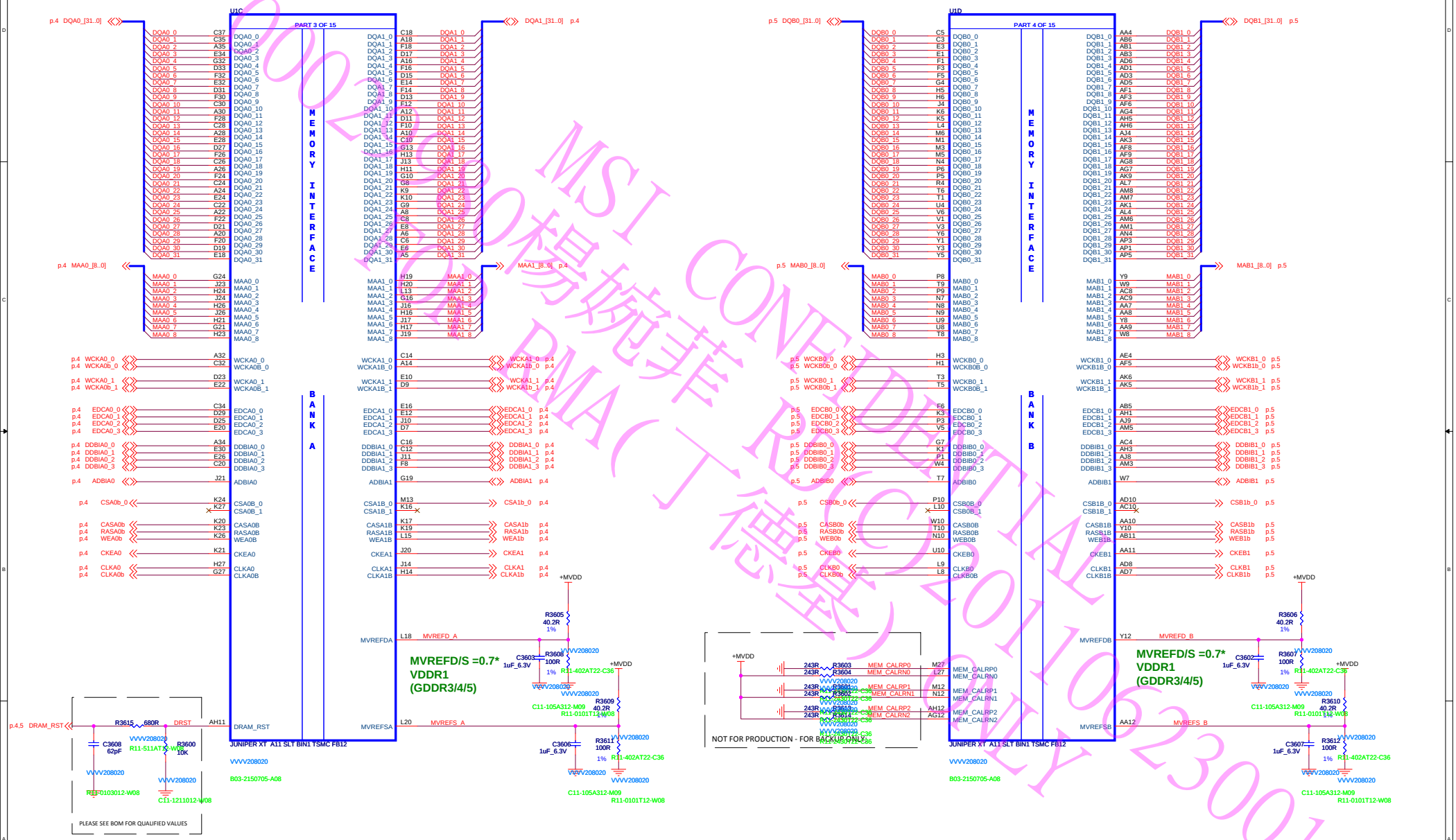
(3) JUNIPER MEM Interface Ch A&B



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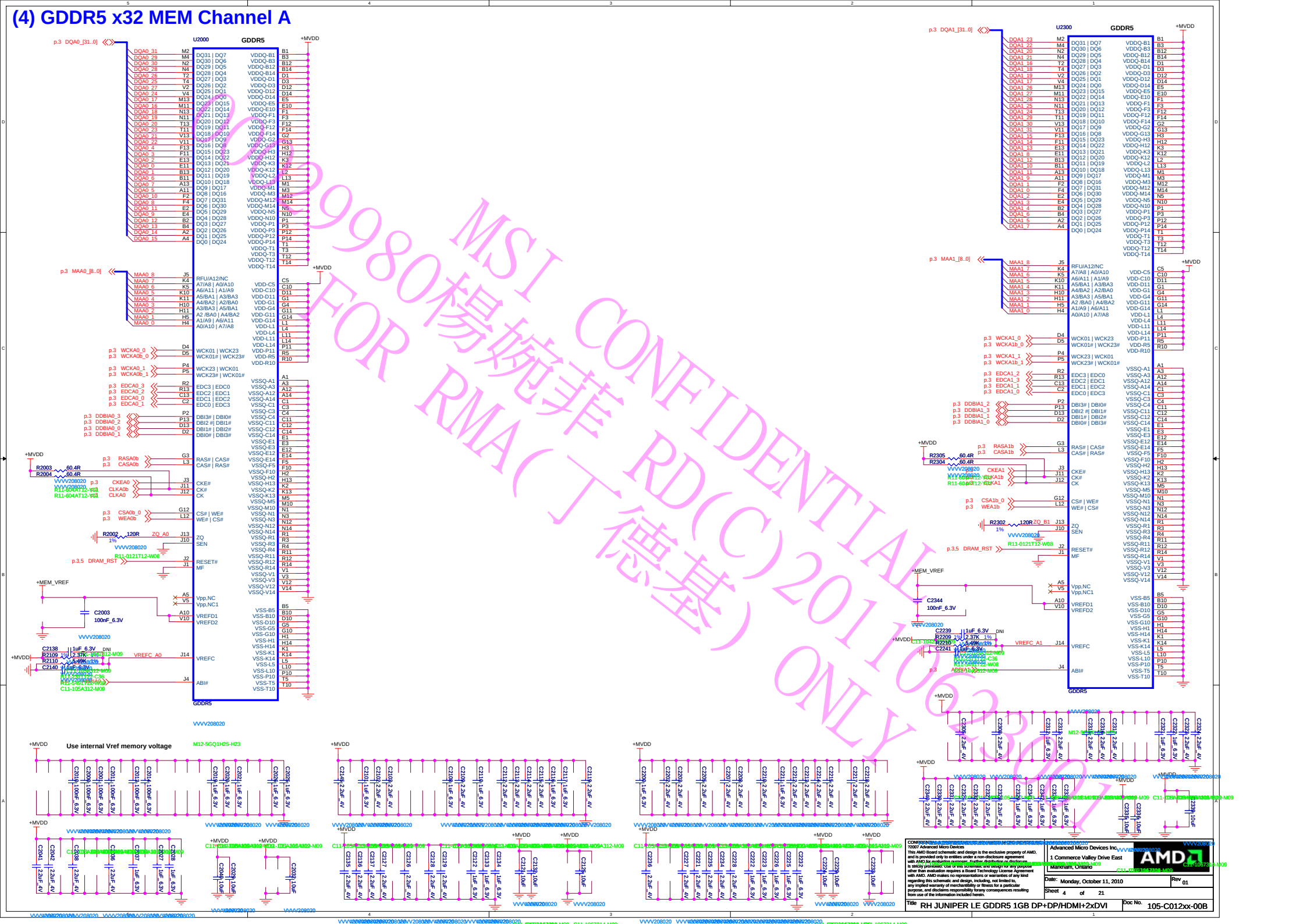
(4) GDDR5 x32 MEM Channel A



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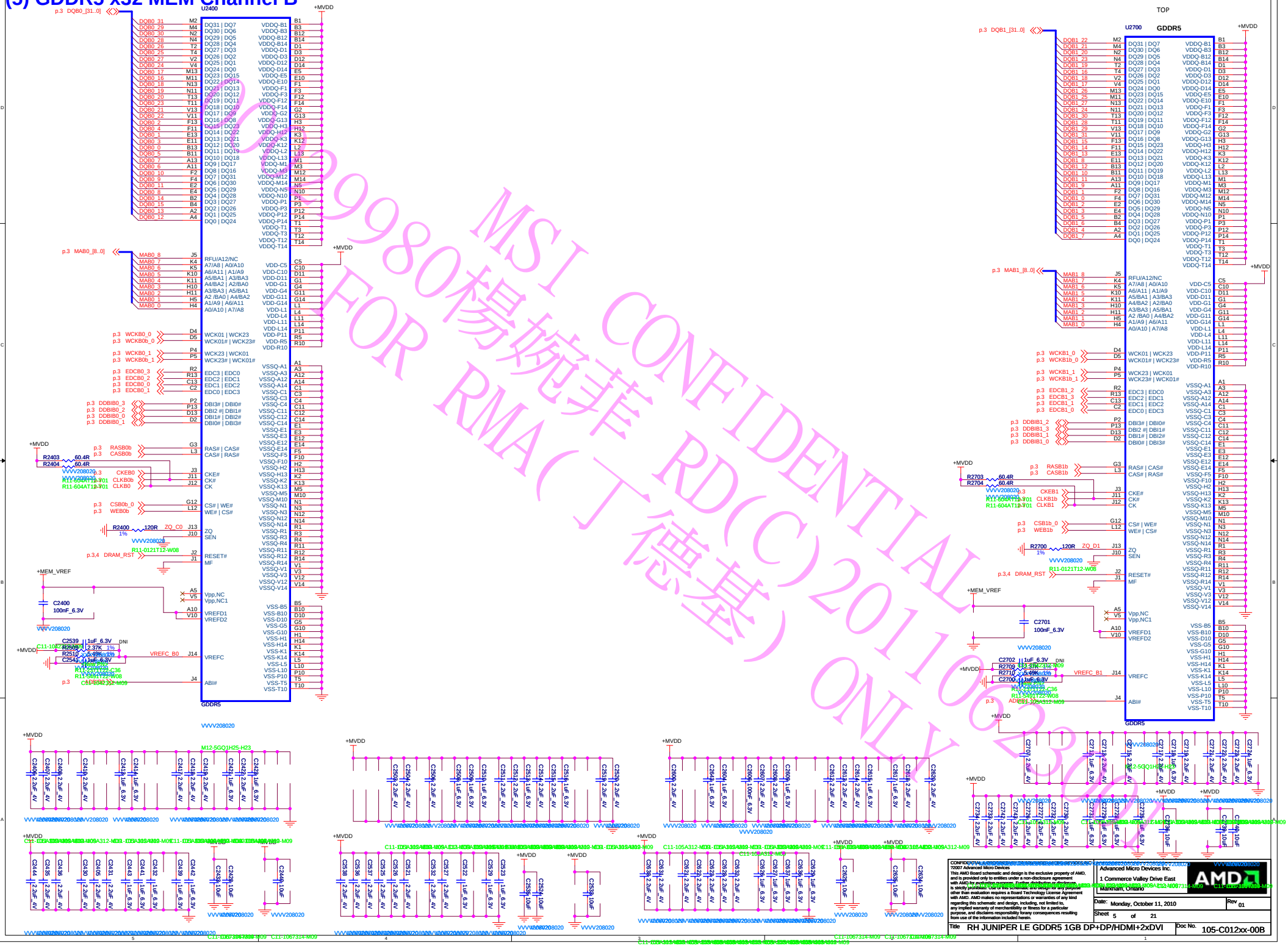
(5) GDDR5 x32 MEM Channel B



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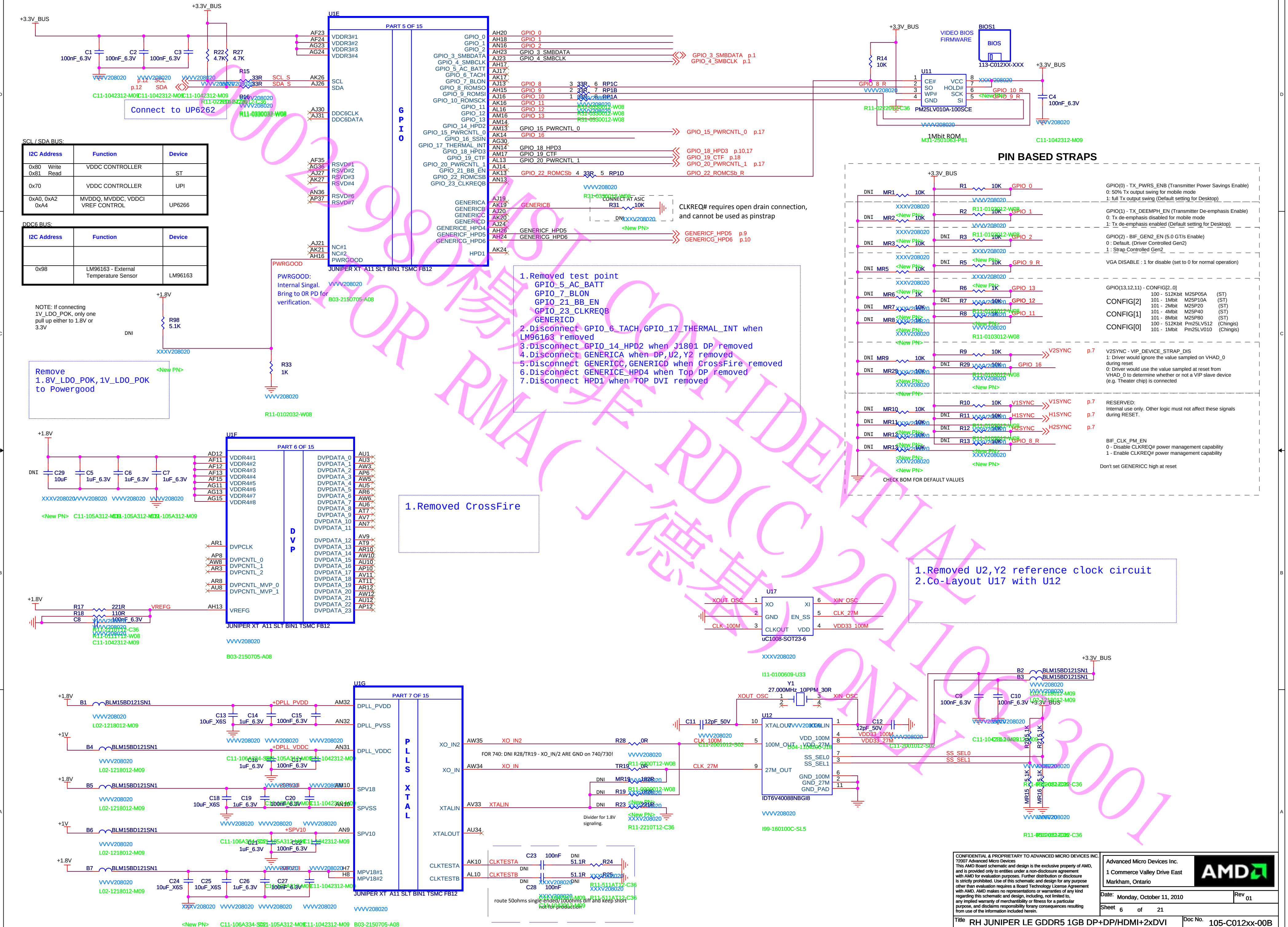
(06) JUNIPER GPIOs Strap CF XTAL OSC



SCL / SDA BUS:

I2C Address	Function	Device
0x80 Write 0x81 Read	VDDC CONTROLLER	ST
0x70	VDDC CONTROLLER	UPI
0xA0, 0xA2 0xA4	MVDDQ, MVDDC, VDDCI VREF CONTROL	UP6266

DDC6 BUS:

I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

Remove
1.8V_LDO_POK,1V_LDO_POK
to Powergood

1.Removed test point
GPIO_5_AC_BATT
GPIO_7_BLON
GPIO_21_BB_EN
GPIO_23_CLKREQB
GENERICD
2.Disconnect GPIO_6_TACH,GPIO_17_THERMAL_INT when LM96163 removed
3.Disconnect GPIO_14_HPD2 when J1801 DP removed
4.Disconnect GENERICA when DP,U2,Y2 removed
5.Disconnect GENERICC,GENERICD when CrossFire removed
6.Disconnect GENERIC_HPD4 when Top DP removed
7.Disconnect HPD1 when TOP DVI removed

1.Removed CrossFire

1.Removed U2,Y2 reference clock circuit
2.Co-Layout U17 with U12

PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO(13,12,11) - CONFIG[2..0]

CONFIG[2]	100 - 512Kbit	M25P05A	(ST)
	101 - 1Mbit	M25P10A	(ST)
CONFIG[1]	101 - 2Mbit	M25P20	(ST)
	101 - 4Mbit	M25P40	(ST)
CONFIG[0]	101 - 8Mbit	M25P80	(ST)
	100 - 512Kbit	Pm25LV512	(Chingis)
	101 - 1Mbit	Pm25LV010	(Chingis)

V2SYNC - VIP_DEVICE_STRAP_DIS
1: Driver would ignore the value sampled on VHAD_0 during reset
0: Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected

RESERVED:
Internal use only. Other logic must not affect these signals during RESET.

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

Don't set GENERICC high at reset

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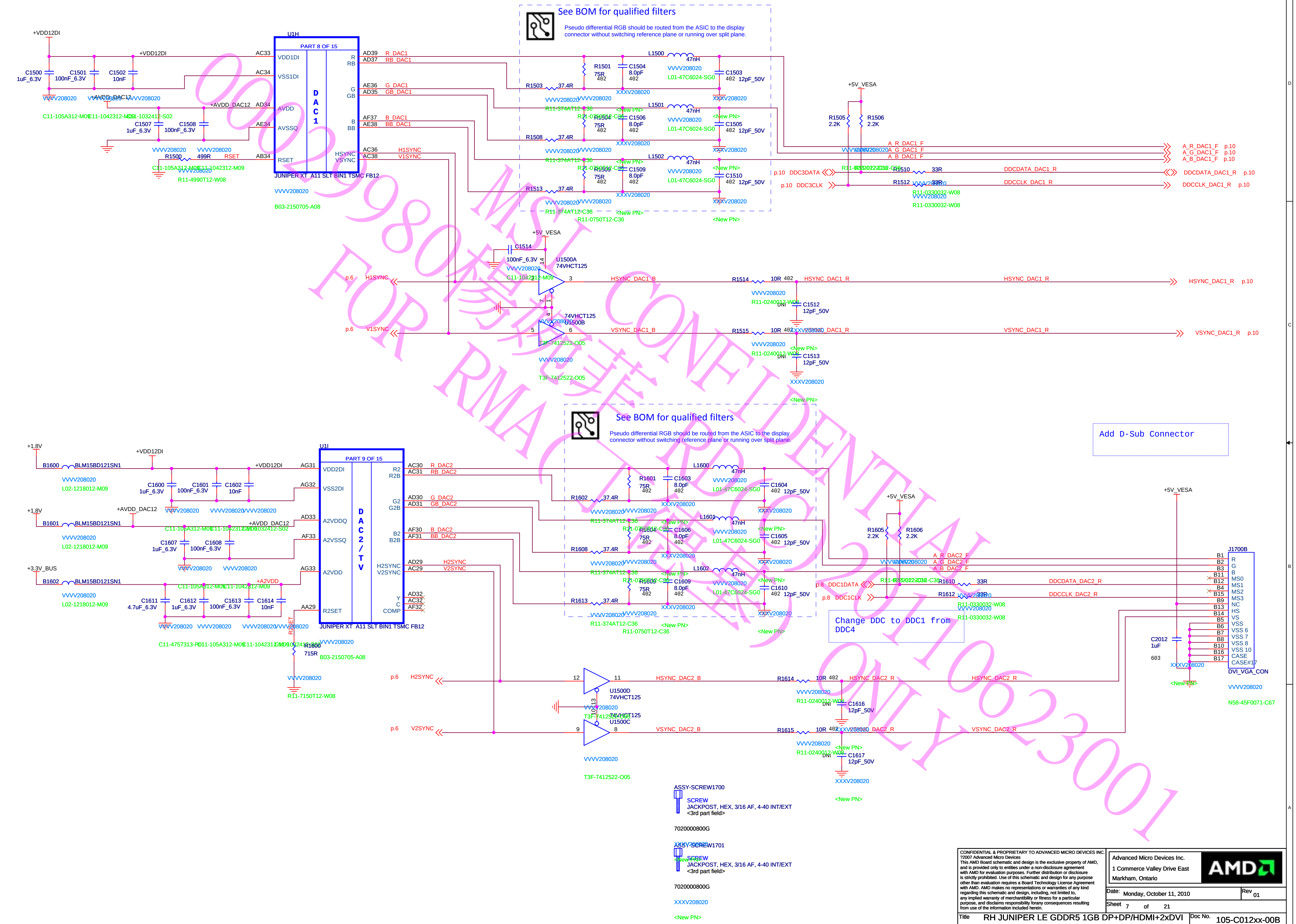
(07) JUNIPER DAC1 and DAC2



See BOM for qualified filters
Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.
U1H
PART 8 OF 15
VDD1DI
VSS1DI
AVDD
AVSSQ
RSET
DAC1
R
RB
G
GB
B
BB
HSYNC
VSYNC
JUNIPER XT A11 SLT BIN1 TSMC FB12
B03-2150705-A08
+VDD12DI
+AVDD_DAC12
C1500 1uF_6.3V
C1501 100nF_6.3V
C1502 10nF
C1507 1uF_6.3V
C1508 100nF_6.3V
R1500 499R
RSET
R_DAC1
RB_DAC1
G_DAC1
GB_DAC1
B_DAC1
BB_DAC1
H1SYNC
V1SYNC
L1500 47nH
L1501 47nH
L1502 47nH
R1501 75R
R1503 37.4R
R1508 37.4R
R1513 37.4R
C1504 8.0pF
C1503 12pF_50V
C1505 12pF_50V
C1510 12pF_50V
+5V_VESA
R1505 2.2K
R1506 2.2K
A_R_DAC1_F p.10
A_G_DAC1_F p.10
A_B_DAC1_F p.10
DDCDATA_DAC1_R p.10
DDCCLK_DAC1_R p.10
R1510 33R
R1512 33R
C1514 100nF_6.3V
U1500A 74VHCT125
U1500B 74VHCT125
HSYNC_DAC1_B
VSYNC_DAC1_B
R1514 10R
R1515 10R
HSYNC_DAC1_R p.10
VSYNC_DAC1_R p.10
C1512 12pF_50V
C1513 12pF_50V
Add D-Sub Connector
U1I
PART 9 OF 15
VDD2DI
VSS2DI
A2VDDQ
A2VSSQ
A2VDD
R2SET
DAC2/TV
R2
R2B
G2
G2B
B2
B2B
H2SYNC
V2SYNC
Y
C
COMP
JUNIPER XT A11 SLT BIN1 TSMC FB12
B1600 BLM15BD121SN1
B1601 BLM15BD121SN1
B1602 BLM15BD121SN1
+1.8V
+3.3V_BUS
+A2VDD
R1600 715R
R_DAC2
G_DAC2
B_DAC2
H2SYNC
V2SYNC
L1600 47nH
L1601 47nH
L1602 47nH
R1602 37.4R
R1608 37.4R
R1613 37.4R
R1605 2.2K
R1606 2.2K
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
Change DDC to DDC1 from DDC4
J1700B
DVI_VGA_CON
N58-45F0071-C67
U1500D 74VHCT125
U1500C 74VHCT125
HSYNC_DAC2_B
VSYNC_DAC2_B
R1614 10R
R1615 10R
HSYNC_DAC2_R
VSYNC_DAC2_R
C1616 12pF_50V
C1617 12pF_50V
ASSY-SCREW1700
SCREW JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT <3rd part field>
7020000800G
ASSY-SCREW1701
SCREW JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT <3rd part field>
7020000800G

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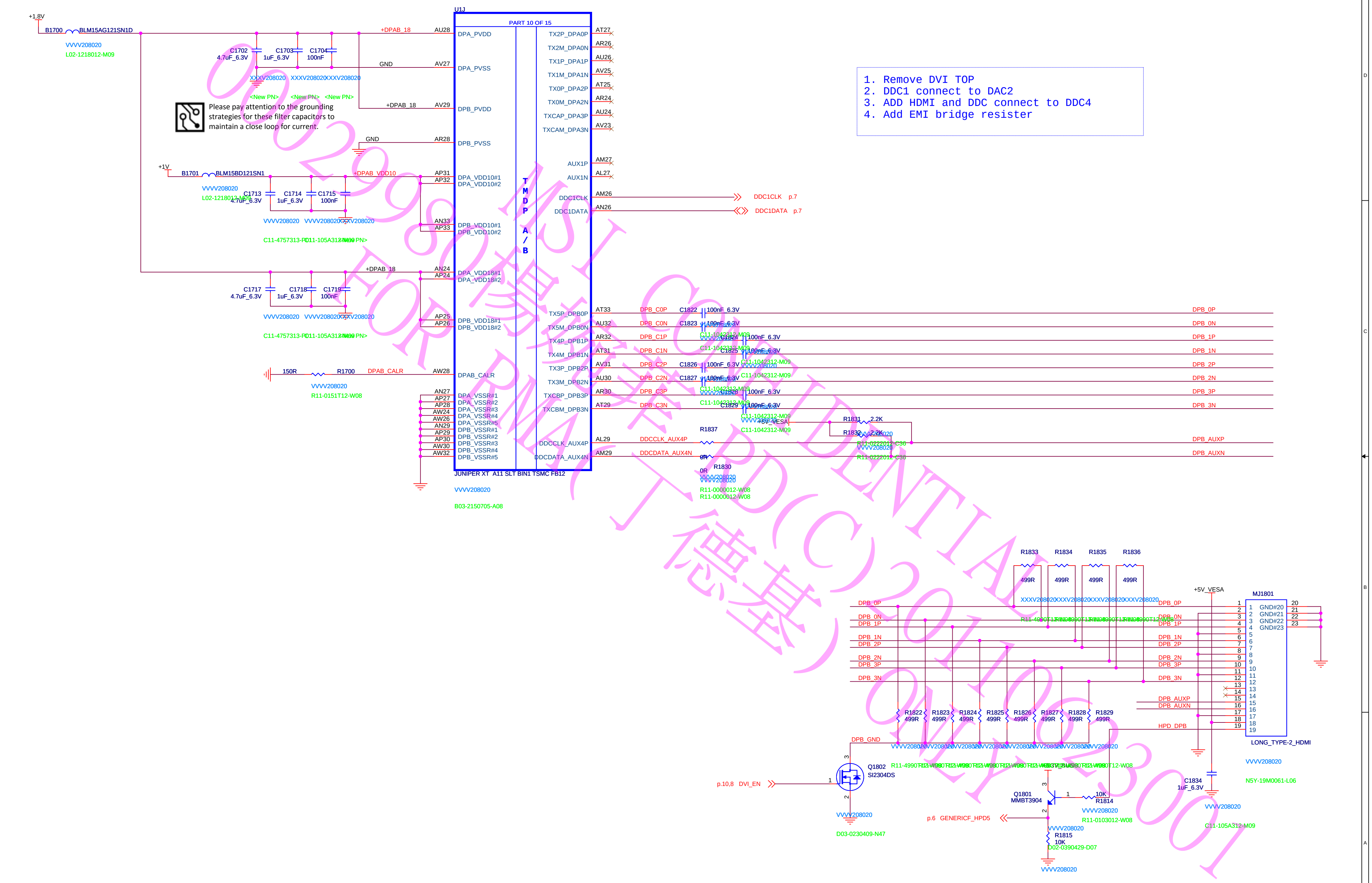
(08) JUNIPER TMDP A&B dDVI-I TOP



U1J
PART 10 OF 15
JUNIPER XT A11 SLT BIN1 TSMC FB12
TMDP A/B
DPA_PVDD
DPA_PVSS
DPB_PVDD
DPB_PVSS
DPA_VDD10#1
DPA_VDD10#2
DPB_VDD10#1
DPB_VDD10#2
DPA_VDD18#1
DPA_VDD18#2
DPB_VDD18#1
DPB_VDD18#2
DPAB_CALR
TX2P_DPA0P
TX2M_DPA0N
TX1P_DPA1P
TX1M_DPA1N
TX0P_DPA2P
TX0M_DPA2N
TXCAP_DPA3P
TXCAM_DPA3N
AUX1P
AUX1N
DDC1CLK
DDC1DATA
TX5P_DPB0P
TX5M_DPB0N
TX4P_DPB1P
TX4M_DPB1N
TX3P_DPB2P
TX3M_DPB2N
TXCBP_DPB3P
TXCBM_DPB3N
DDCCLK_AUX4P
DDCDATA_AUX4N
+1.8V
B1700 BLM15AG121SN1D
+1V
B1701 BLM15BD121SN1
+DPAB_18
+DPAB_VDD10
Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.
DDC1CLK p.7
DDC1DATA p.7
R1700 150R DPAB_CALR
+5V_VESA
R1831 2.2K
R1832 2.2K
R1837
R1830 0R
DPB_0P
DPB_0N
DPB_1P
DPB_1N
DPB_2P
DPB_2N
DPB_3P
DPB_3N
DPB_AUXP
DPB_AUXN
HPD_DPB
DPB_GND
MJ1801
LONG_TYPE-2_HDMI
Q1802 SI2304DS
p.10,8 DVI_EN
Q1801 MMBT3904
p.6 GENERIC_HPD5
R1814 10K
R1815 10K
C1834 1uF_6.3V

1. Remove DVI TOP
2. DDC1 connect to DAC2
3. ADD HDMI and DDC connect to DDC4
4. Add EMI bridge resister

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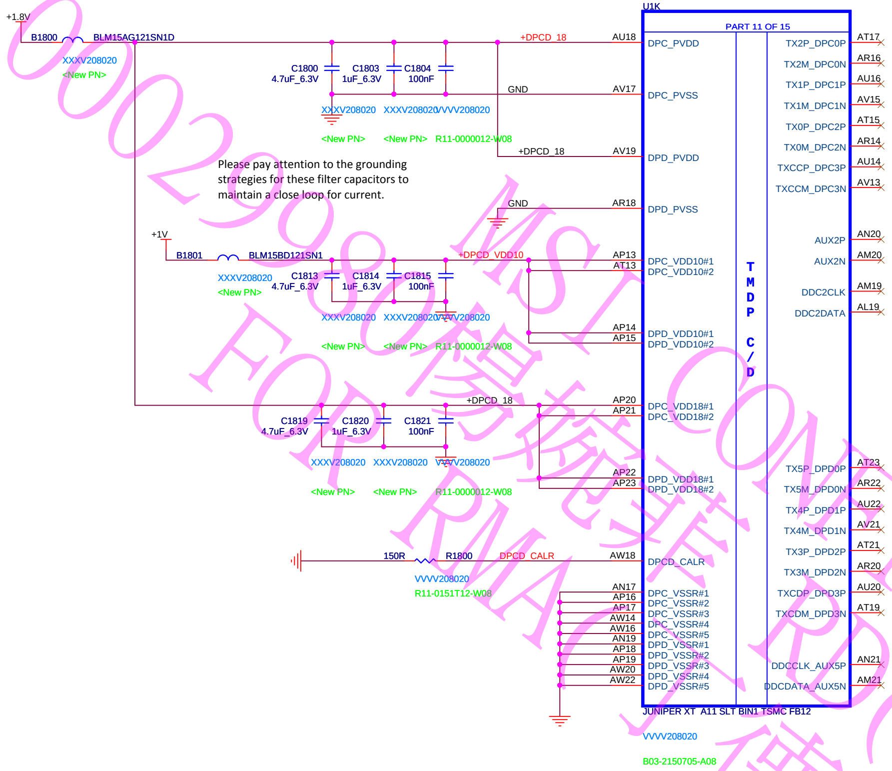
(09) JUNIPER Display Port C & Display Port/HDMI D



+1.8V
B1800 BLM15AG121SN1D
XXXV208020
<New PN>
+DPCD_18
C1800 4.7uF_6.3V
C1803 1uF_6.3V
C1804 100nF
GND
XXXV208020 XXXV208020 VVVV208020
<New PN> <New PN> R11-0000012-W08
Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.
+1V
B1801 BLM15BD121SN1
+DPCD_VDD10
C1813 4.7uF_6.3V
C1814 1uF_6.3V
C1815 100nF
C1819 4.7uF_6.3V
C1820 1uF_6.3V
C1821 100nF
150R R1800 DPCD_CALR
VVVV208020
R11-0151T12-W08
U1K
PART 11 OF 15
DPC_PVDD
DPC_PVSS
DPD_PVDD
DPD_PVSS
DPC_VDD10#1
DPC_VDD10#2
DPD_VDD10#1
DPD_VDD10#2
DPC_VDD18#1
DPC_VDD18#2
DPD_VDD18#1
DPD_VDD18#2
DPCD_CALR
DPC_VSSR#1
DPC_VSSR#2
DPC_VSSR#3
DPC_VSSR#4
DPC_VSSR#5
DPD_VSSR#1
DPD_VSSR#2
DPD_VSSR#3
DPD_VSSR#4
DPD_VSSR#5
TMDP C/D
TX2P_DPC0P
TX2M_DPC0N
TX1P_DPC1P
TX1M_DPC1N
TX0P_DPC2P
TX0M_DPC2N
TXCCP_DPC3P
TXCCM_DPC3N
AUX2P
AUX2N
DDC2CLK
DDC2DATA
TX5P_DPD0P
TX5M_DPD0N
TX4P_DPD1P
TX4M_DPD1N
TX3P_DPD2P
TX3M_DPD2N
TXCDP_DPD3P
TXCDM_DPD3N
DDCCLK_AUX5P
DDCDATA_AUX5N
JUNIPER XT A11 SLT BIN1 TSMC FB12
VVVV208020
B03-2150705-A08

1.Removed DP,HDMI Circuit

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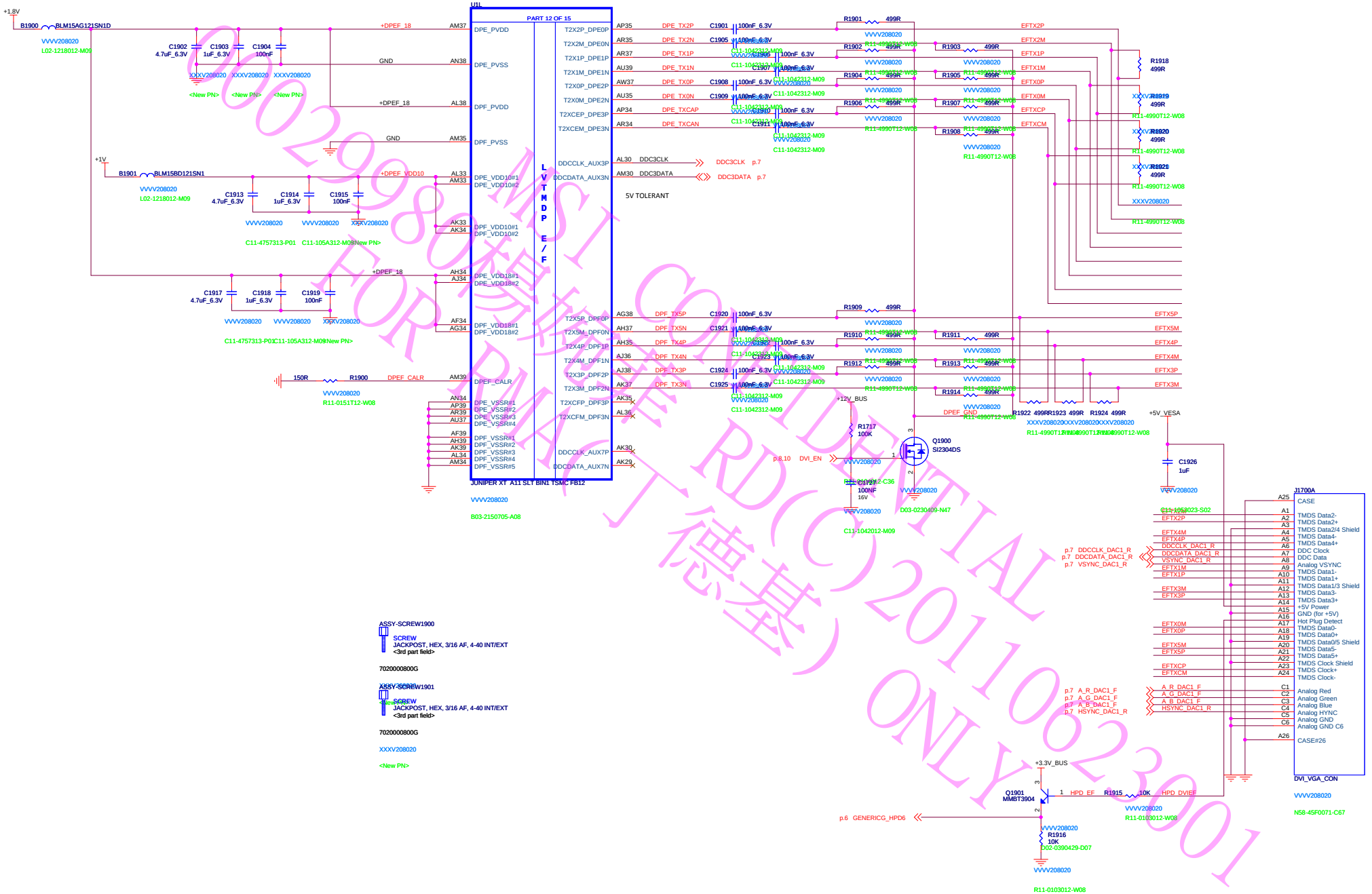
(10) JUNIPER LVTMDP E&F dDVI-I BOTTOM



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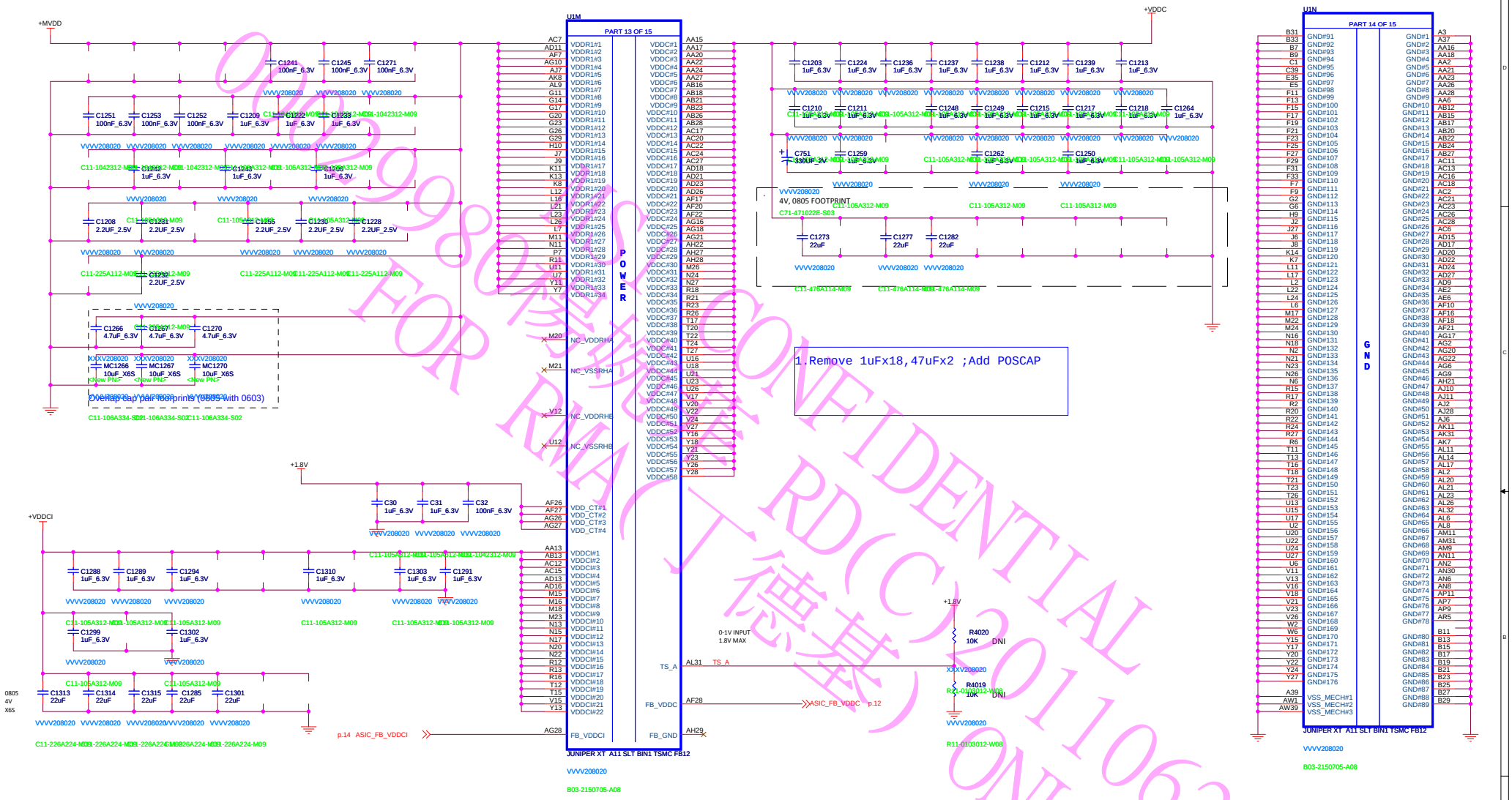
(11) JUNIPER Power & GND



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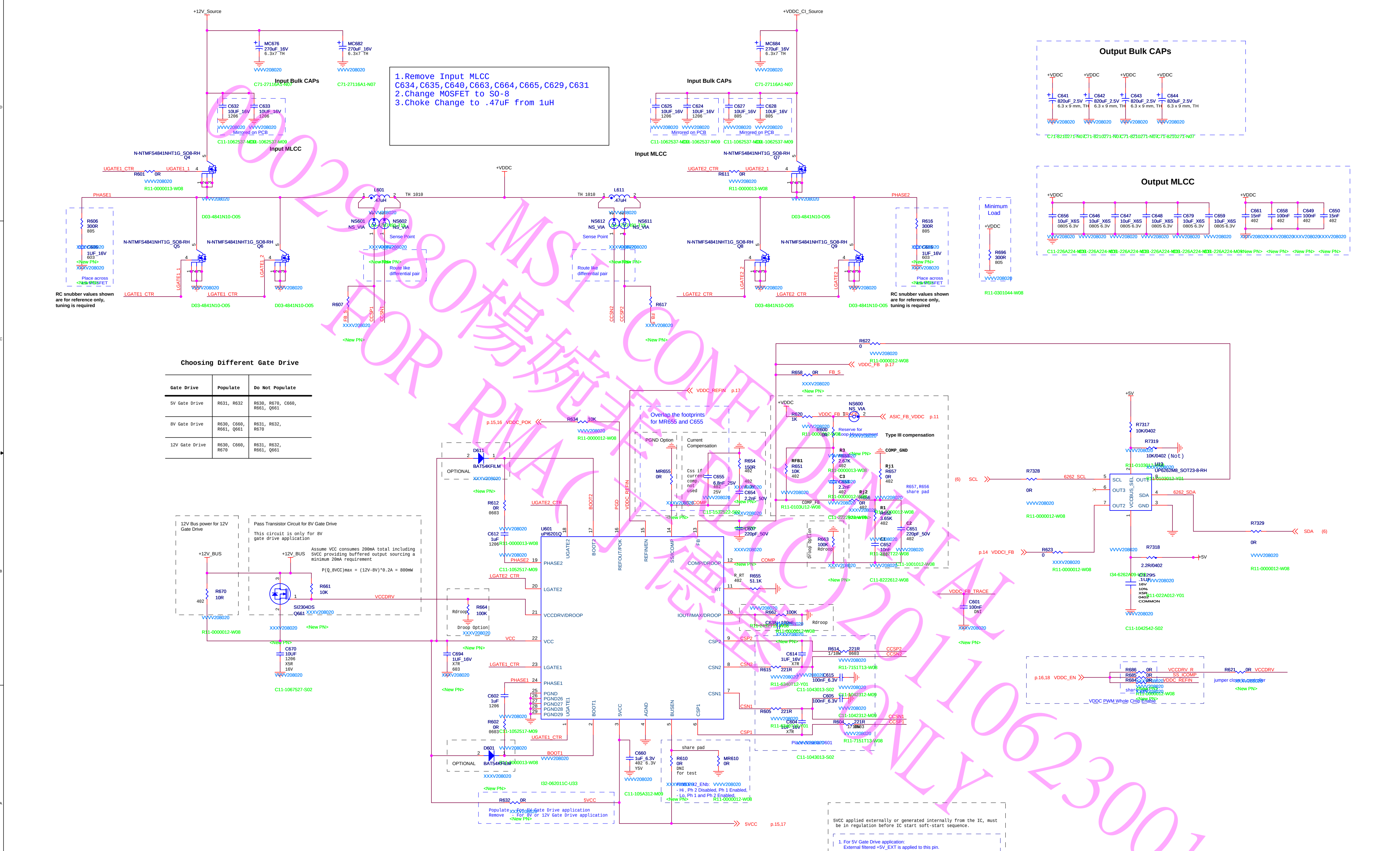

1.Remove Input MLCC
C634,C635,C640,C663,C664,C665,C629,C631
2.Change MOSFET to SO-8
3.Choke Change to .47uF from 1uH
+12V_Source
+VDDC_CI_Source
Input Bulk CAPs
Input MLCC
Output Bulk CAPs
Output MLCC
Minimum Load
PHASE1
PHASE2
UGATE1_CTR
UGATE2_CTR
LGATE1_CTR
LGATE2_CTR
N-NTMFS4841NHT1G_SO8-RH
L601 .47uH
L611 .47uH
Sense Point
Route like differential pair
RC snubber values shown are for reference only, tuning is required
Place across HS MOSFET
12V Bus power for 12V Gate Drive
Pass Transistor Circuit for 8V Gate Drive
This circuit is only for 8V gate drive application
Assume VCC consumes 200mA total including 5VCC providing buffered output sourcing a minimum 20mA requirement
P(Q_8VCC)max = (12V-8V)*0.2A = 800mW
U601 uP6201Q
Overlap the footprints for MR655 and C655
PGND Option
Current Compensation
Type III compensation
Reserve for Loop Measurement
Droop Option
OPTIONAL
share pad
Populate - For 5V Gate Drive application
Remove - For 8V or 12V Gate Drive application
VDDC PWM Whole Chip Enable
jumper close to controller
U13 UP6262M8_SOT23-8-RH
5VCC applied externally or generated internally from the IC, must be in regulation before IC start soft-start sequence.
1. For 5V Gate Drive application: External filtered +5V_EXT is applied to this pin.
2. For 8V or 12V Gate Drive application: +5VCC is generated internally and this is an output with 20mA minimum current capability

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661

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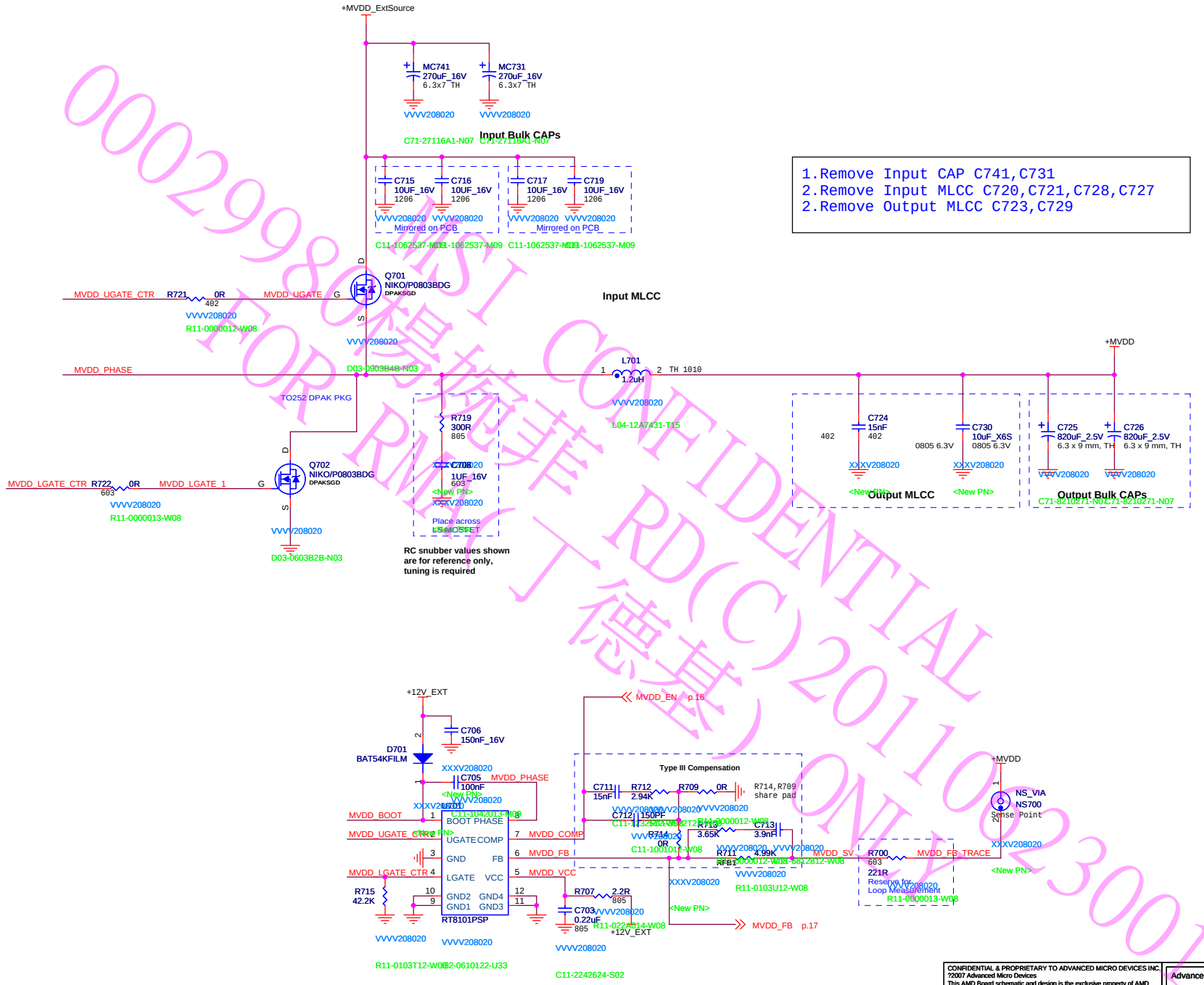

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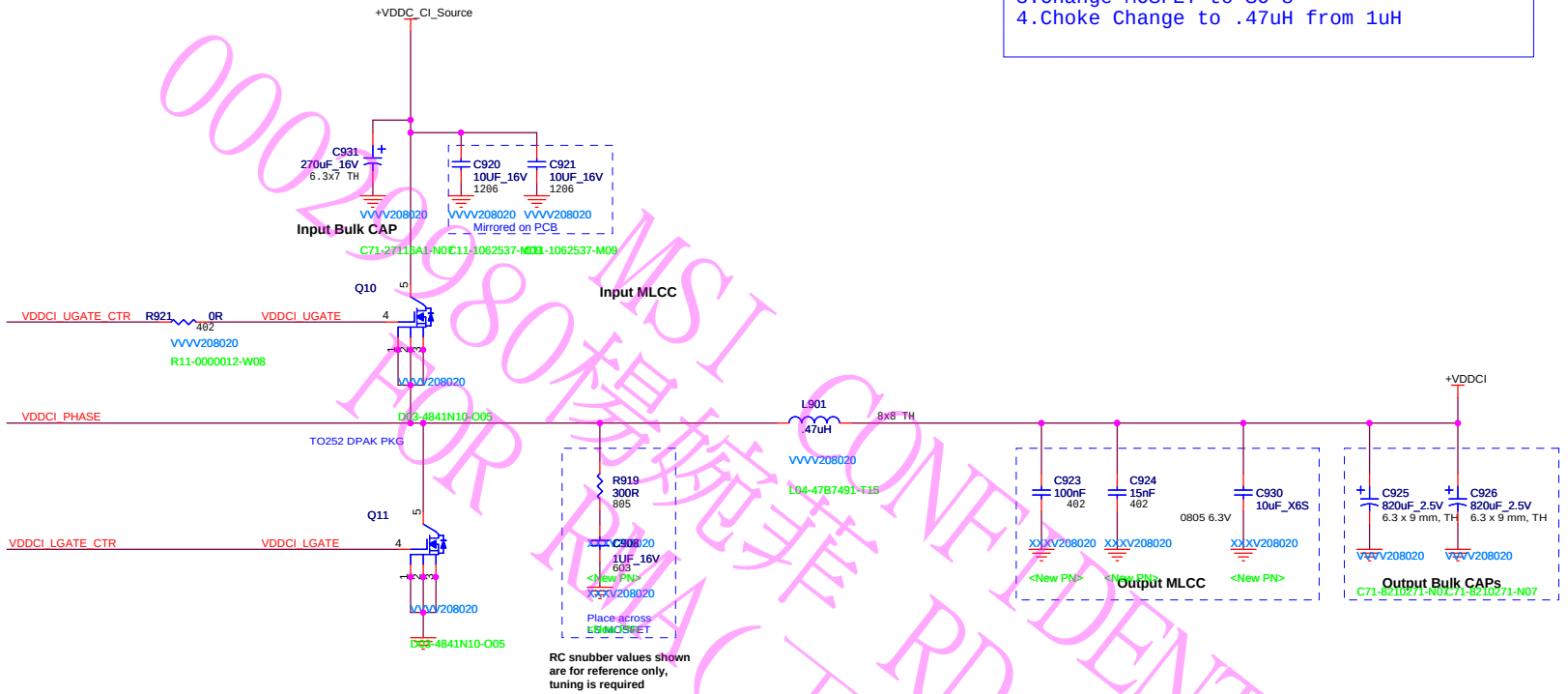
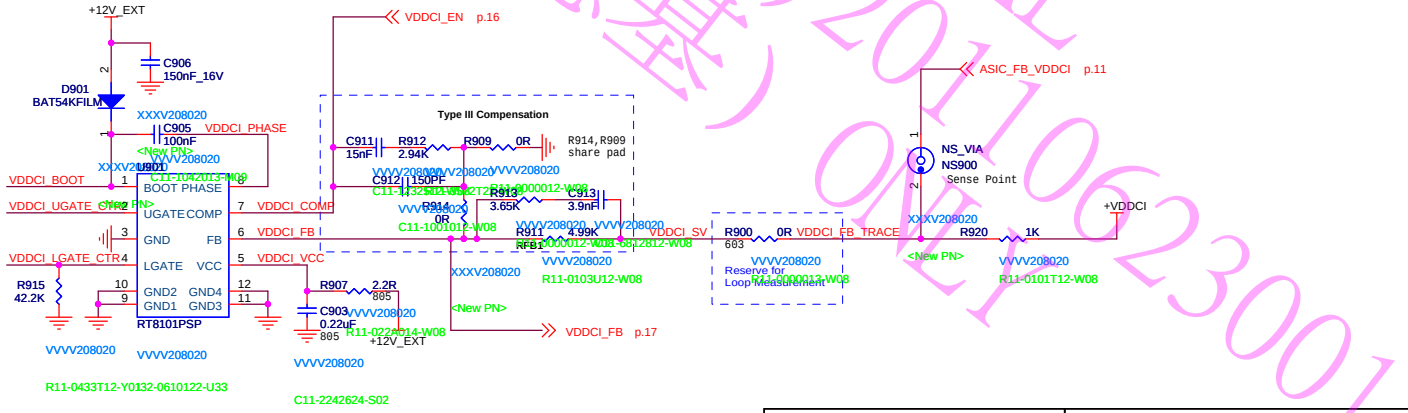
1.Remove Input MLCC C915,C916,C917,C919
2.Remove Output MLCC C923,C929
3.Change MOSFET to SO-8
4.Choke Change to .47uH from 1uH





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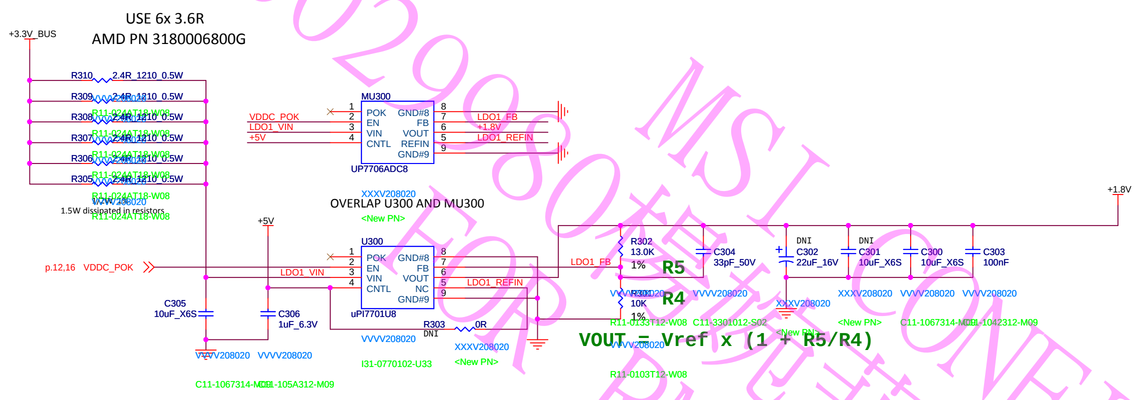
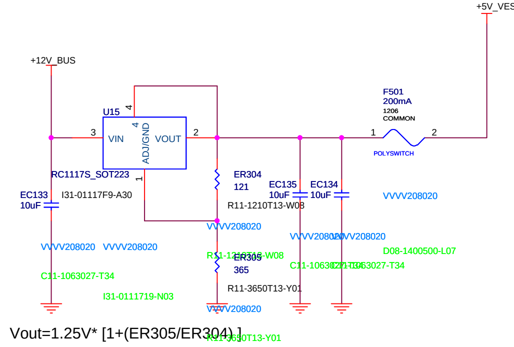
(15) Linear Regulators

Regulators for +5V, +5V_VESA and +5V_HDMI

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

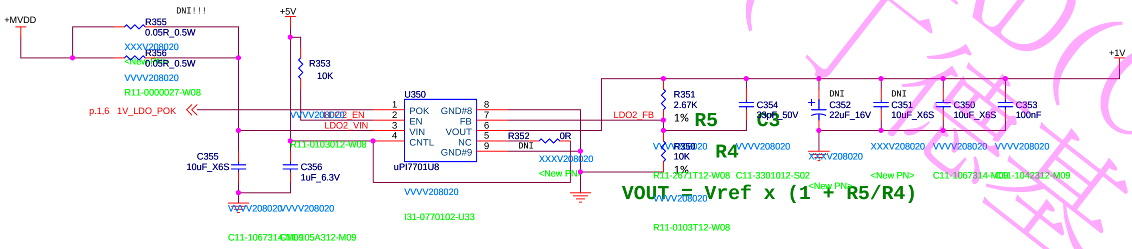


USE 6x 3.6R
AMD PN 3180006800G
+3.3V_BUS
R310 2.4R_1210_0.5W
R309 2.4R_1210_0.5W
R308 2.4R_1210_0.5W
R307 2.4R_1210_0.5W
R306 2.4R_1210_0.5W
R305 2.4R_1210_0.5W
1.5W dissipated in resistors
MU300
UP7706ADC8
OVERLAP U300 AND MU300
U300
uPI7701U8
VDDC_POK
LDO1_VIN
LDO1_FB
LDO1_REFIN
p.12,16 VDDC_POK
+5V
+1.8V
C305 10uF_X6S
C306 1uF_6.3V
R303 0R DNI
R302 13.0K 1%
R301 10K 1%
R5
R4
C304 33pF_50V
C302 22uF_16V
C301 10uF_X6S
C300 10uF_X6S
C303 100nF
VOUT = Vref x (1 + R5/R4)

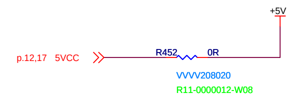


1.Change +5V REGULATOR to A1117

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

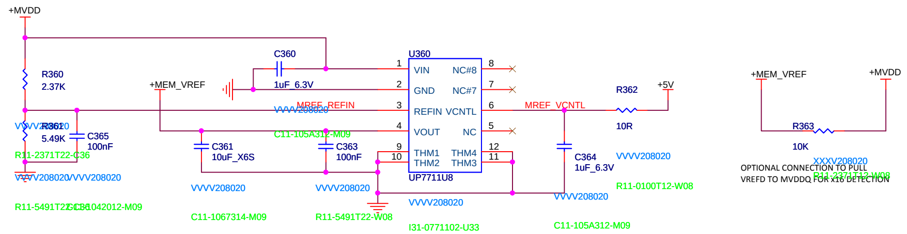


+MVDD
DNI!!!
R355 0.05R_0.5W
R356 0.05R_0.5W
+5V
R353 10K
U350
uPI7701U8
p.1,6 1V_LDO_POK
LDO2_EN
LDO2_VIN
LDO2_FB
C355 10uF_X6S
C356 1uF_6.3V
R352 0R DNI
R351 2.67K 1%
R350 10K 1%
R5
R4
C3
+1V
C354 33pF_50V
C352 22uF_16V
C351 10uF_X6S
C350 10uF_X6S
C353 100nF
VOUT = Vref x (1 + R5/R4)



1.Removed BACKUP OPTION FOR +5V REGULATOR

Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ



There must be one 100nF at each VREF pin
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices

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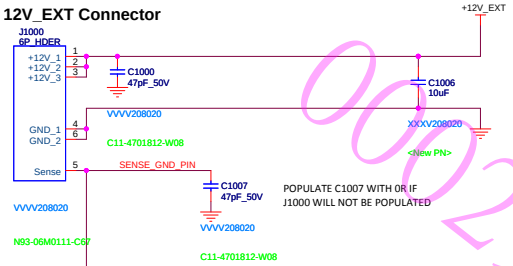
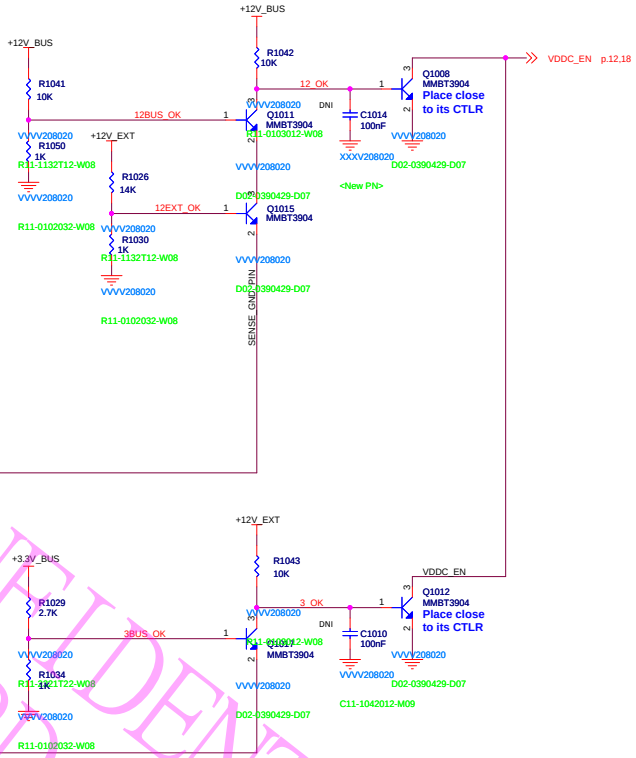
(16) Power Management - Power Gating and External Power Detect

12V_EXT Connector



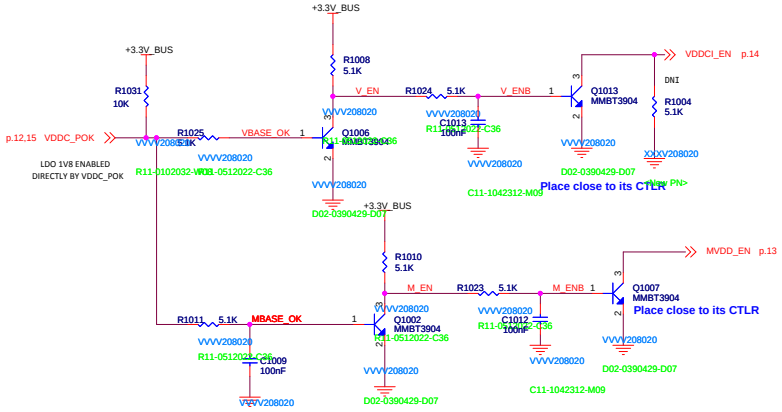
1.Remove option LED

12V_BUS, 12V_EXT & 3V3_BUS POWER SEQUENCING



POWER SEQUENCING CIRCUIT

FOR MVDD & VDDCI
(ENABLES CANNOT BE SHARED SINCE IT IS ALSO THE COMPENSATION PIN OF THE SMPS REGULATOR)



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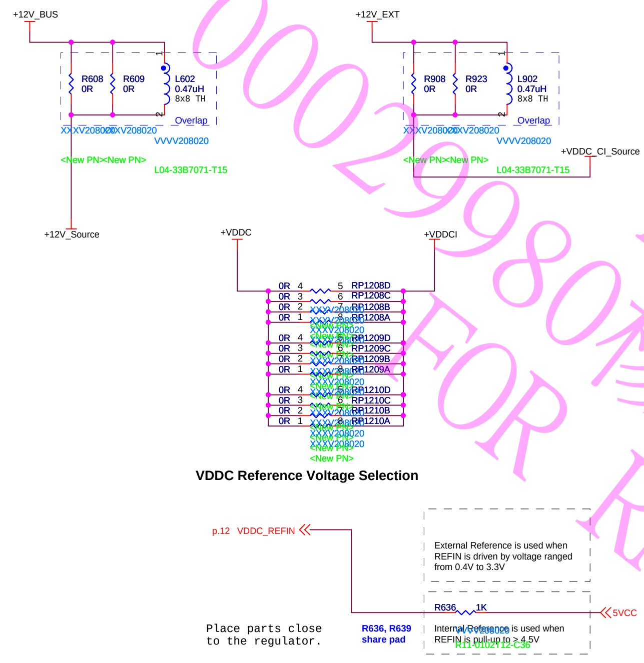
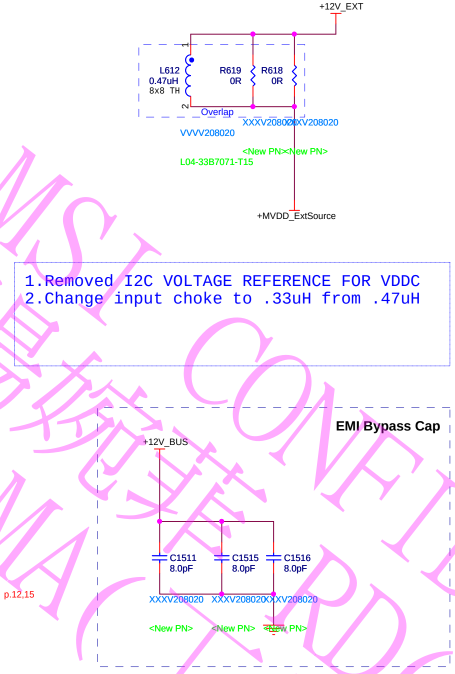
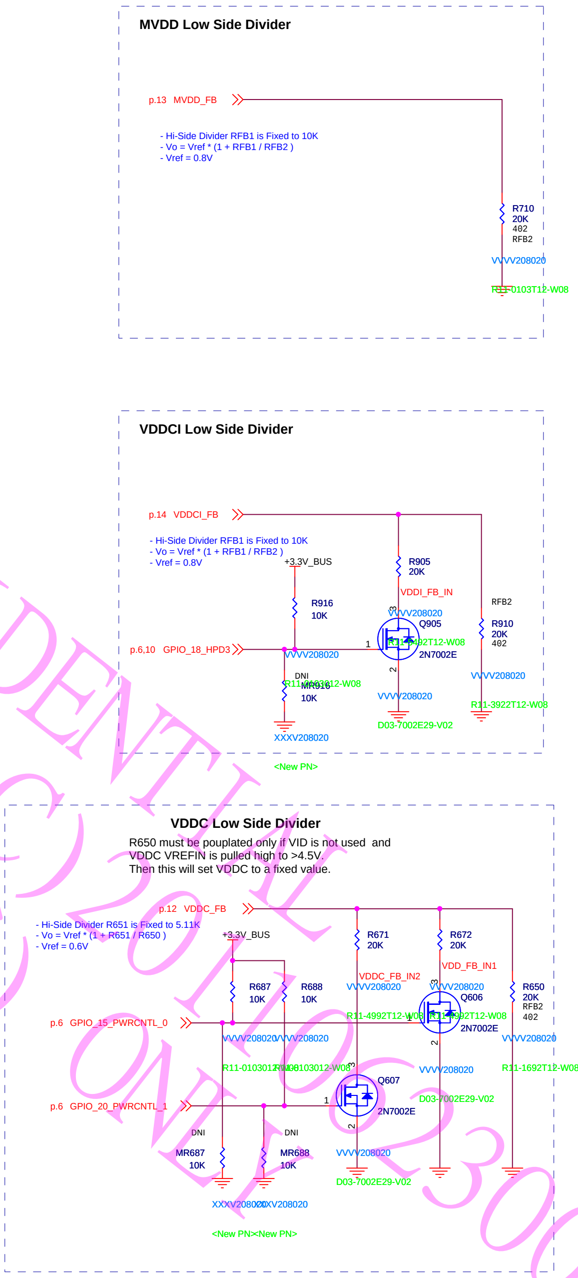
(18) Power Management 2



+12V_BUS
R608 0R
R609 0R
L602 0.47uH 8x8 TH
_Overlap
VVVV208020
<New PN><New PN>
L04-33B7071-T15
+12V_Source
+12V_EXT
R908 0R
R923 0R
L902 0.47uH 8x8 TH
+VDDC_CI_Source
+VDDC
+VDDCI
RP1208D
RP1208C
RP1208B
RP1208A
RP1209D
RP1209C
RP1209B
RP1209A
RP1210D
RP1210C
RP1210B
RP1210A
VDDC Reference Voltage Selection
p.12 VDDC_REFIN
External Reference is used when REFIN is driven by voltage ranged from 0.4V to 3.3V
R636 1K
Internal Reference is used when REFIN is pull-up to > 4.5V
5VCC
p.12,15
Place parts close to the regulator.
R636, R639 share pad





MVDD Low Side Divider
p.13 MVDD_FB
- Hi-Side Divider RFB1 is Fixed to 10K
- Vo = Vref * (1 + RFB1 / RFB2)
- Vref = 0.8V
R710 20K 402 RFB2
VDDCI Low Side Divider
p.14 VDDCI_FB
- Hi-Side Divider RFB1 is Fixed to 10K
- Vo = Vref * (1 + RFB1 / RFB2)
- Vref = 0.8V
+3.3V_BUS
R905 20K
VDDI_FB_IN
R916 10K
Q905 2N7002E
R910 20K 402
RFB2
p.6,10 GPIO_18_HPD3
MR916 10K
DNI
VDDC Low Side Divider
R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V.
Then this will set VDDC to a fixed value.
p.12 VDDC_FB
- Hi-Side Divider R651 is Fixed to 5.11K
- Vo = Vref * (1 + R651 / R650)
- Vref = 0.6V
+3.3V_BUS
R671 20K
R672 20K
VDD_FB_IN1
VDDC_FB_IN2
R687 10K
R688 10K
R650 20K RFB2 402
Q606 2N7002E
p.6 GPIO_15_PWRCNTL_0
Q607 2N7002E
p.6 GPIO_20_PWRCNTL_1
MR687 10K
MR688 10K
DNI

VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

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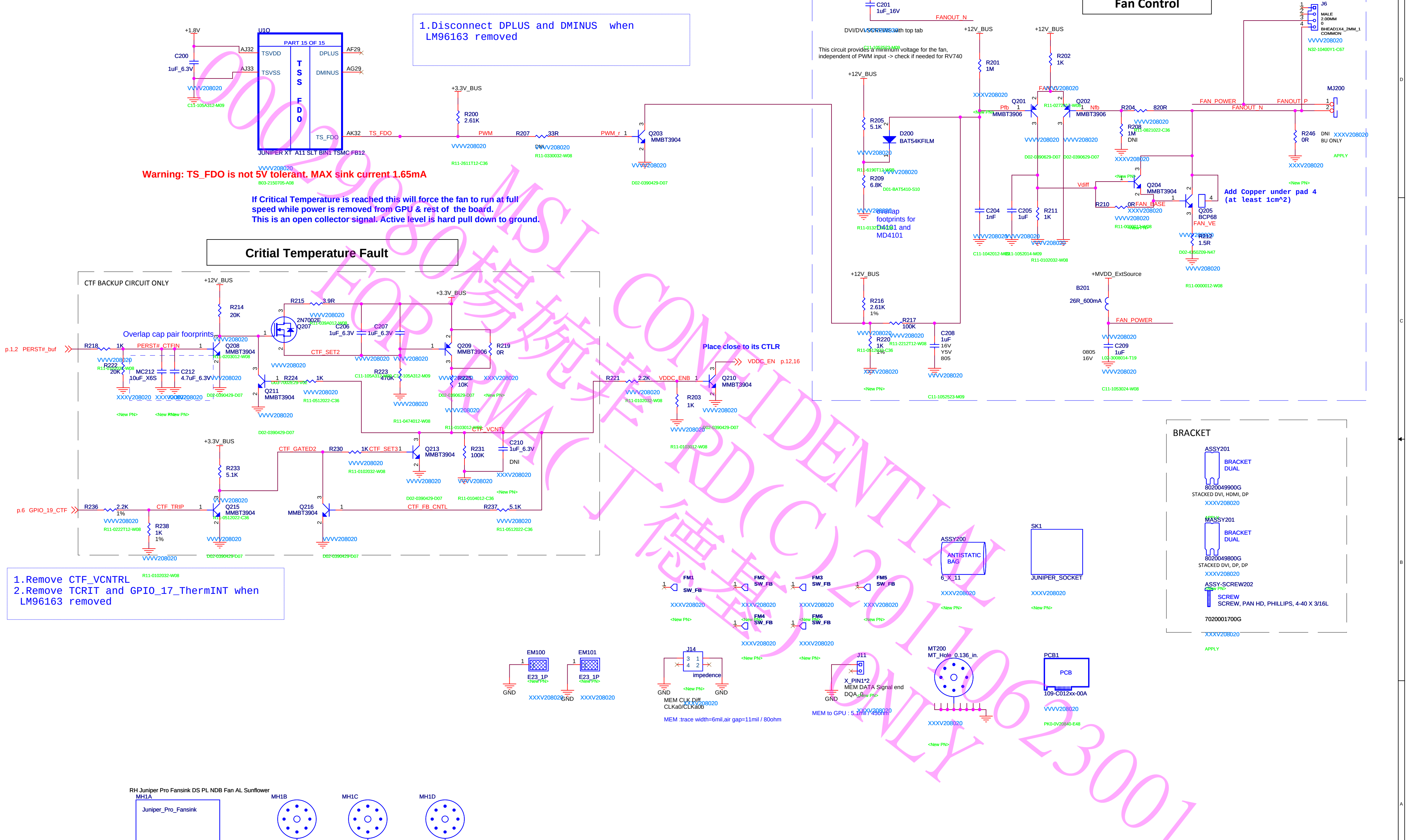
(19) Mechanical and Thermal Management



1.Disconnect DPLUS and DMINUS when LM96163 removed
U1O
PART 15 OF 15
TSVDD
TSVSS
DPLUS
DMINUS
TS_FDO
JUNIPER XT A11 SLT BIN1 TSMC FB12
Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA
If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board.
This is an open collector signal. Active level is hard pull down to ground.
Critial Temperature Fault
CTF BACKUP CIRCUIT ONLY
Overlap cap pair foorprints
p.1,2 PERST#_buf
p.6 GPIO_19_CTF
Place close to its CTLR
VDDC_EN p.12,16
1.Remove CTF_VCNTRL
2.Remove TCRIT and GPIO_17_ThermINT when LM96163 removed
For 2-WIRE FAN
Fan Control
This circuit provides a minimum voltage for the fan, independent of PWM input -> check if needed for RV740
Overlap footprints for D4101 and MD4101
Add Copper under pad 4 (at least 1cm^2)
BRACKET
ASSY201
BRACKET DUAL
80200499900G
STACKED DVI, HDMI, DP
ASSY201
BRACKET DUAL
80200498800G
STACKED DVI, DP, DP
ASSY-SCREW202
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L
70200001700G
ANTISTATIC BAG
JUNIPER_SOCKET
MEM :trace width=6mil,air gap=11mil / 80ohm
MEM to GPU : 5.1mil / 450mil
RH Juniper Pro Fansink DS PL NDB Fan AL Sunflower
Juniper_Pro_Fansink
1.Remove VDDC Thermal Protection

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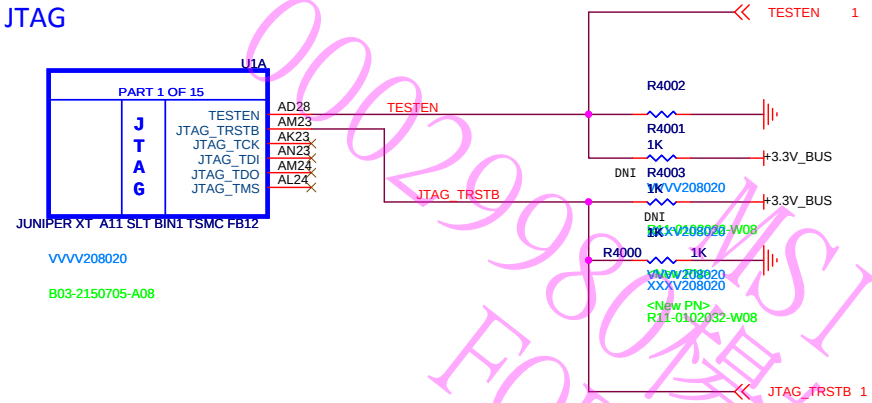
(19) Debug Circuits



1.Remove LED RED "ON" shows Fault circuit
2.Remove JTAG and re-connect to PCIe RESET Buffered
3.Remove SWITCH CONNECTIONS TO PINSTRAPS
4.Remove LM96163

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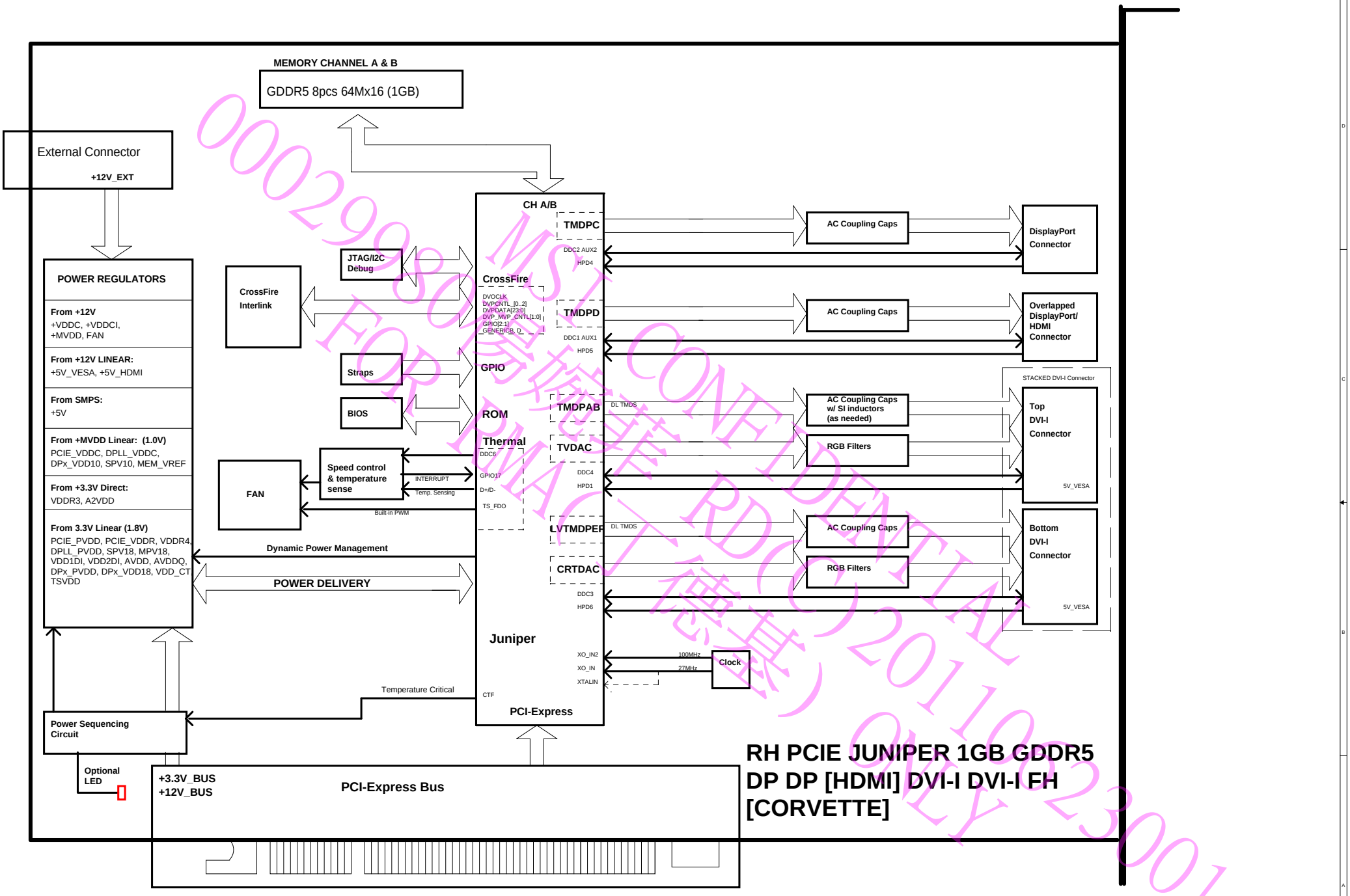

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Title	Schematic No.	Date:
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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 01

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/03/23	JUNIPER LE GDDR5 1GB - BASED ON C010 REV43;
01	00B	2009/07/13	p. 16 - ADD R1010-1, Q1002: MVDD WAS NOT DELAYED ENOUGH WRT VDDCI, ADD EXTRA TRANSISTOR CONNECTION TO CHANGE DELAY; p. 18 - REMOVE R247, R245, CHANGE NET NAME FROM CTF_BYPASS TO CTF_VCNTRL, CHANGE SW4003 CONNECTION TO PRODUCTION-READY CONFIG; p. 6 - ADD 2ND OSCILLATOR CLOCK SOLUTION TO MITIGATE ANY POSSIBLE CONCERNS SHARING GENERICA WITH XO_IN2, AND ALSO TO ALLOW FOR DIFFERENT SPREAD-SPECTRUM SETTINGS FOR DISPLAY AND MEMC TO MITIGATE ANY POSSIBLE EMI PROBLEMS; p.15 - REMOVE R300, R357: 0R WERE THERE FOR BU AND PRE-PRODUCTION DEVELOPMENT, REMOVE FOR PRODUCTION; p. 17 - ADD R687-8, MR687-8, R916, MR916: ADD OPTION OF PU/PD, SO DEFAULT VDDC/VDDCI ON POWER-UP CAN BE CONTROLLED IN BOM; P.8/10 - UPDATE TO DVI FOOTPRINT THAT ALLOWS FOR SINGLE-DVI OVERLAP; p. 15 - ADD R363 - OPTIONAL CONNECTION TO PULL VREFD TO MVDDQ FOR x16 DETECTION BY MEM DEVICES (CERTAIN MEM DEVICES HAVE A BUG THAT CANNOT DETECT x16/x32 WITHOUT PU/PD ON VREFD); p. 17 - ADD R1072-3, R1075-6: THESE ARE FOOTPRINTS TO BE USE FOR FERRITE BEADS IF EMI IS FAILING;
		2010/10/11	Base on V208-4.0 to modify p.4 1.Change to 32Mx32bit ,remove U2100,U2200 p.5 1.Change to 32Mx32bit ,remove U2500,U2600