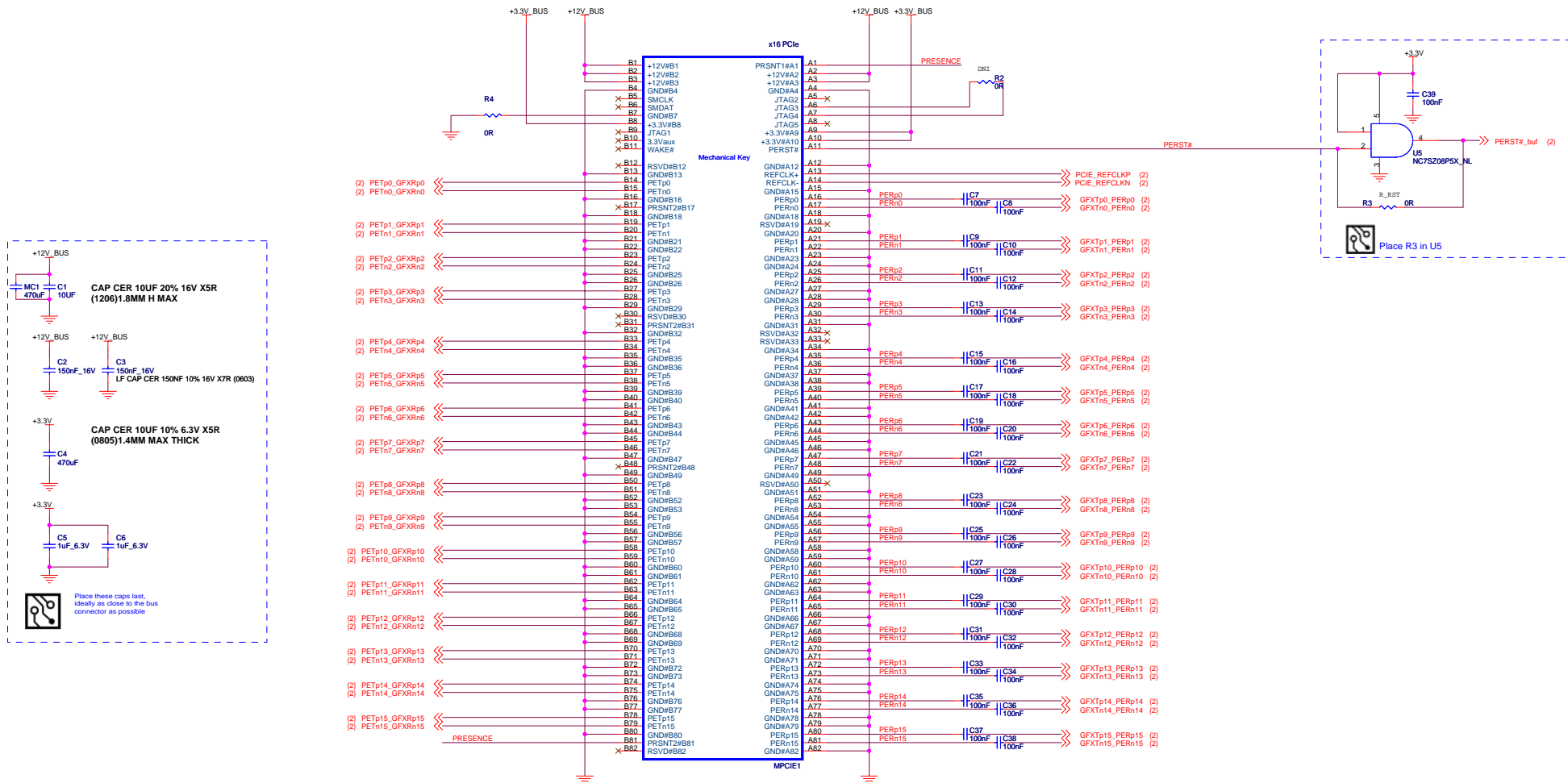


PCI-EXPRESS EDGE CONNECTOR

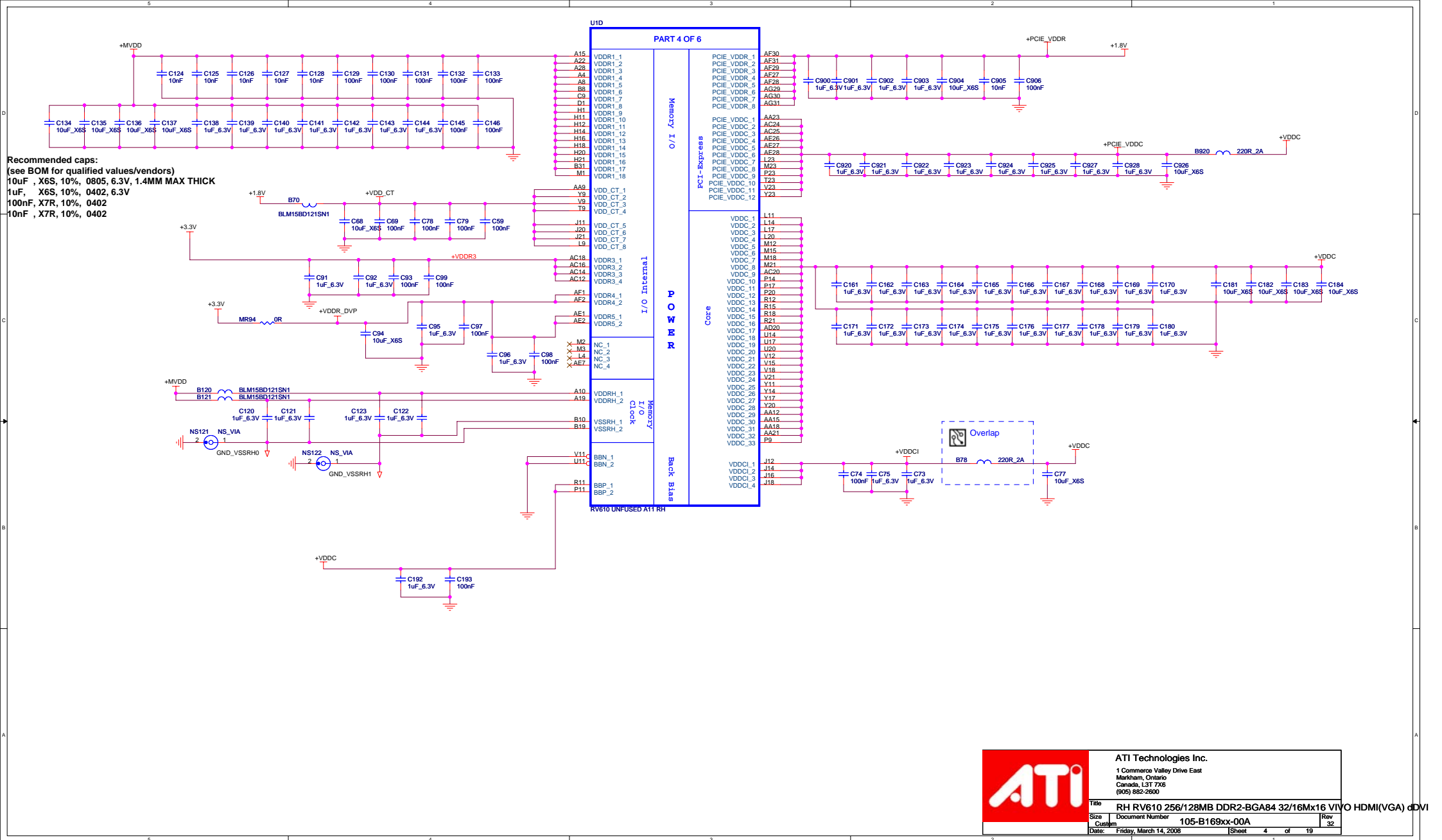


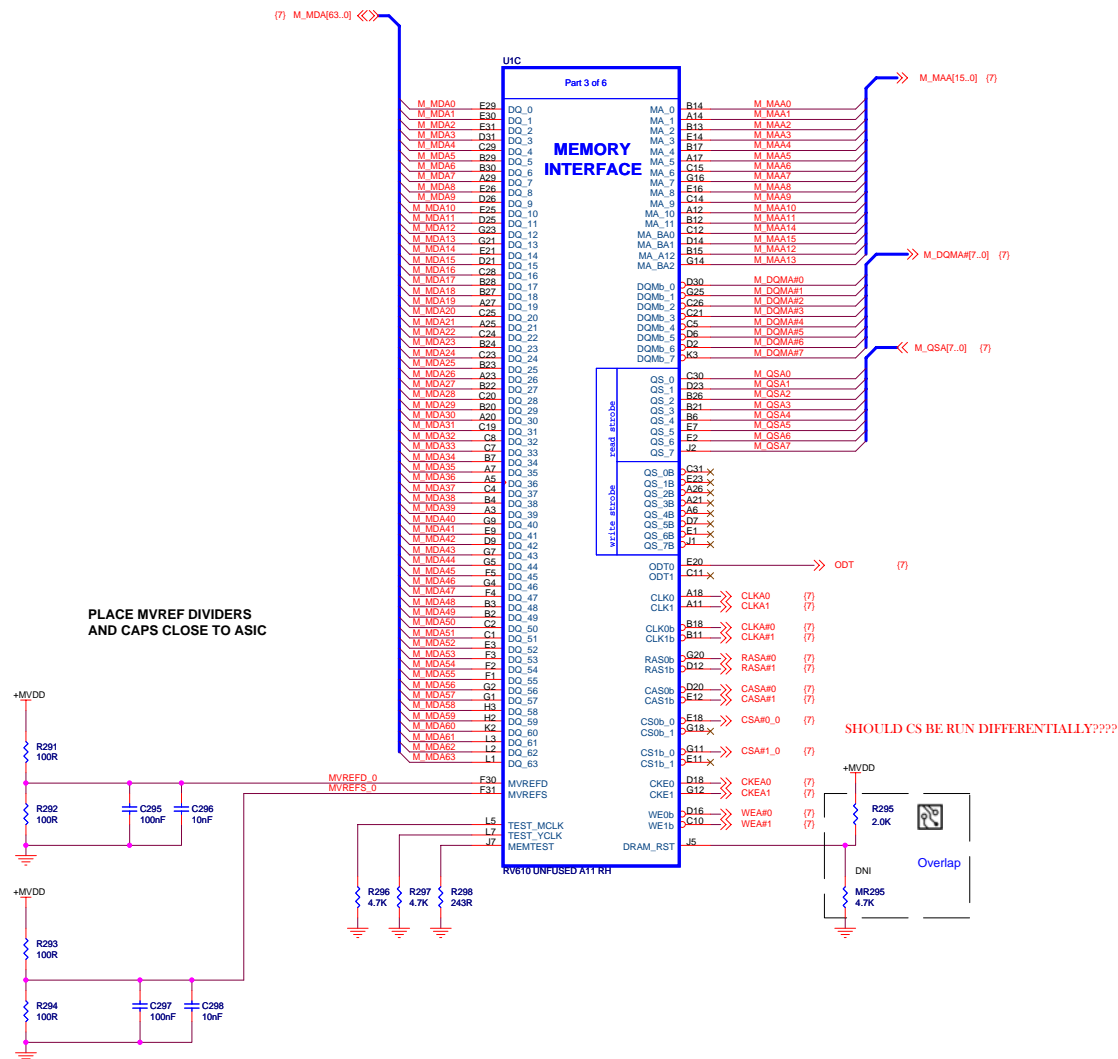
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND



ATI Technologies Inc.		
1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7Y6 (905) 882-2600		
Title	RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HD(M) (VGA) dDVI	
Size	Document Number	105-B169xx-00A
C		Rev 32
Date	Friday, March 14, 2008	Sheet 1 of 19





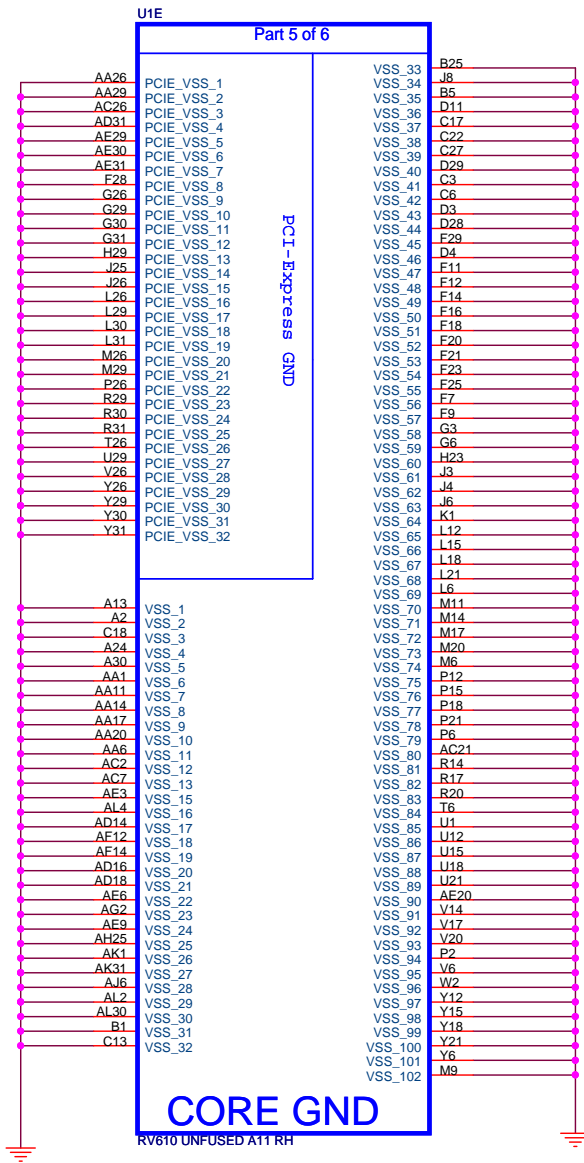


DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada L3T 7X6
(905) 882-2600

Title	RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI		
Size	Document Number	105-B169xx-00A	Rev 32
Date	Friday, March 14, 2008	Sheet 5	of 19

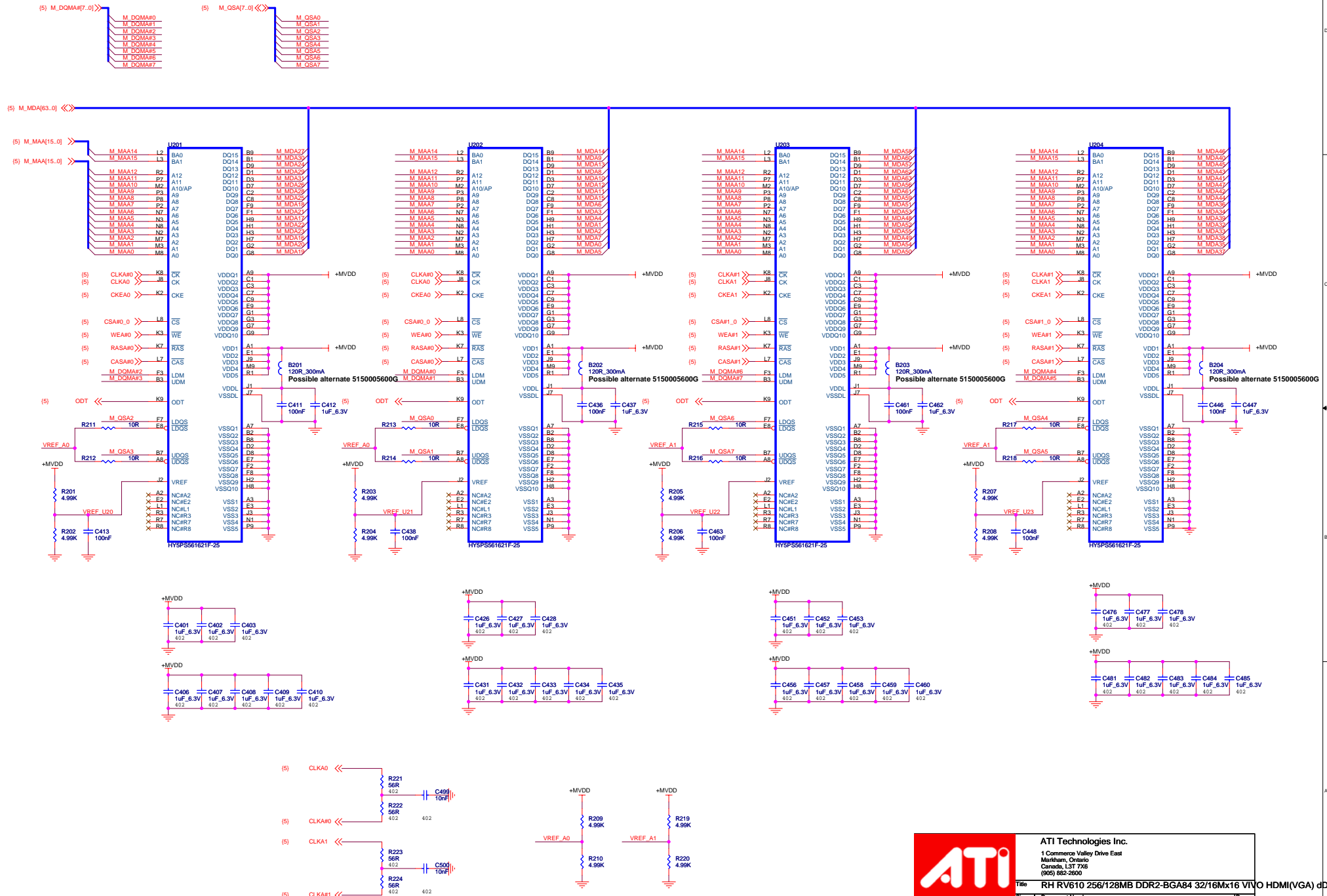


ATI Technologies Inc.

1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title		RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI	
Size	Document Number	105-B169xx-00A	Rev
B			32
Date:	Friday, March 14, 2008	Sheet	6 of 19

CHANNEL A: RANK 0 128MB DDR2

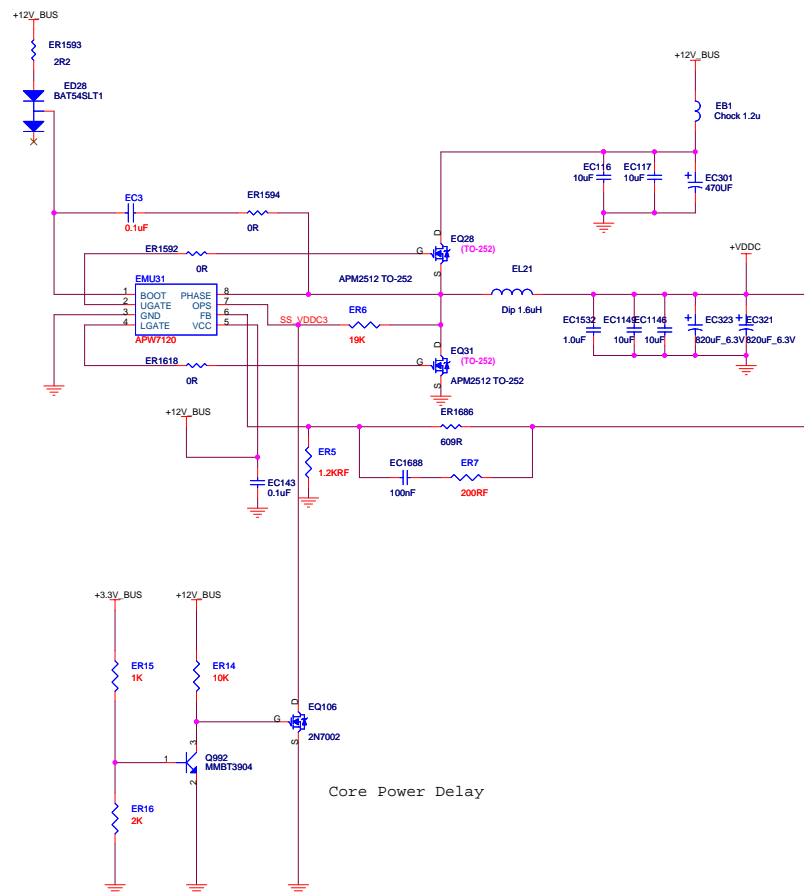


ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2650

RR RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI

Document Number	105-B169xx-00A	Rev	32
Friday, March 14, 2008	[Sheet	7	of 19

CORE REGULATOR +VDDC



ATI Technologies Inc.

1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

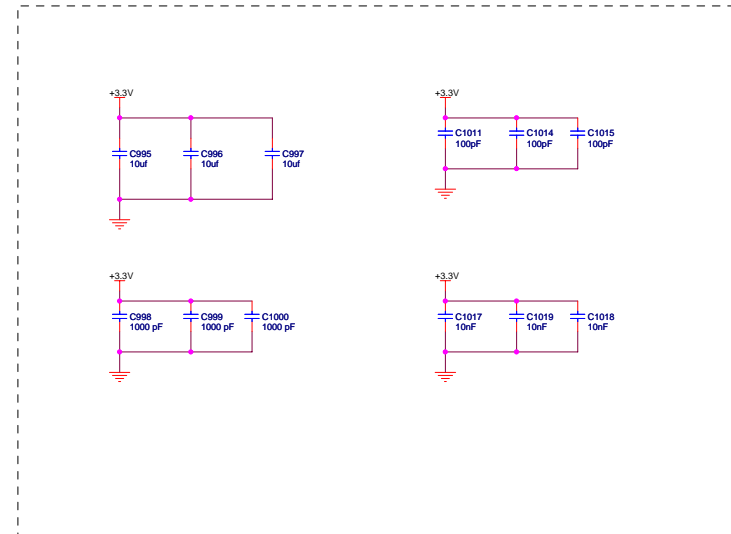
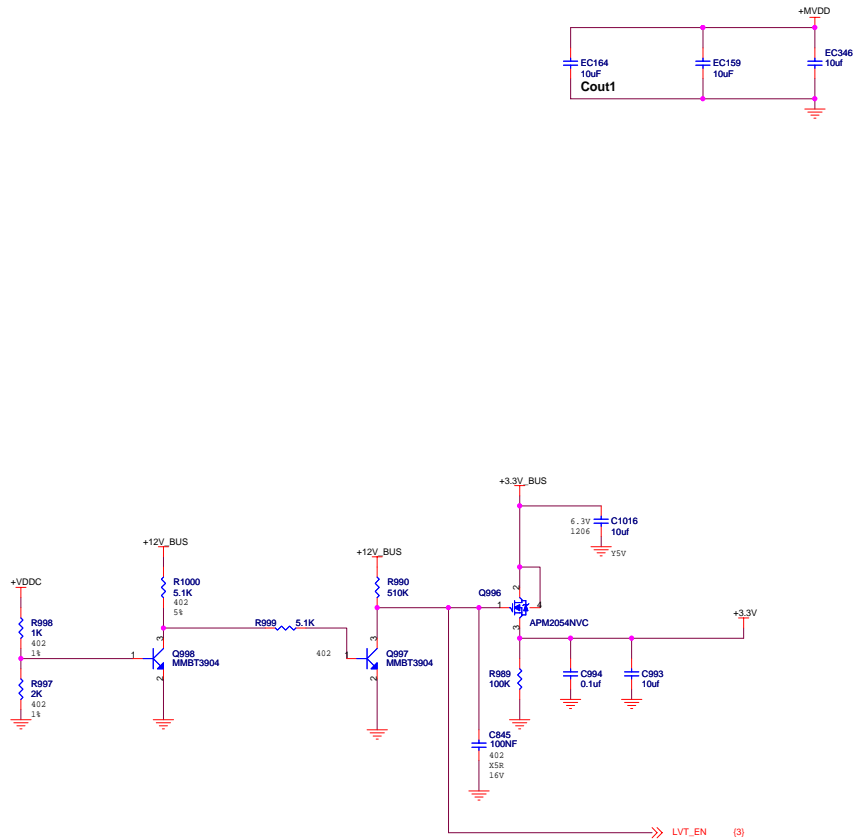
Title TR RV630 - MVDD SMPS02

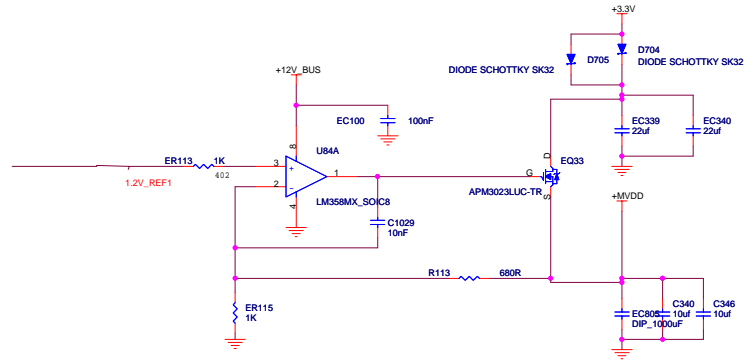
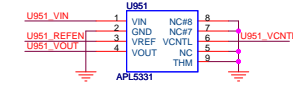
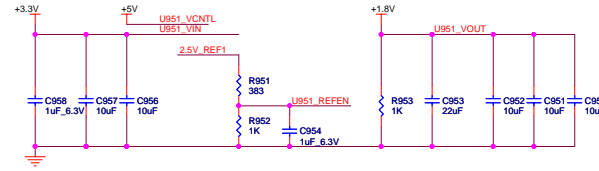
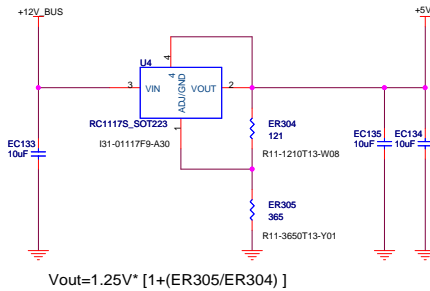
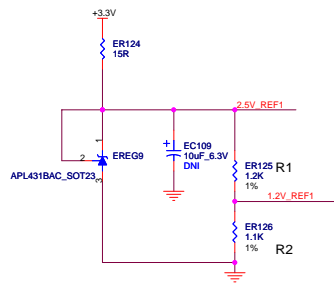
Size Customer Document Number 105-DB047-00A

Date Friday, March 14, 2008

Sheet 8 of 21

Rev 7





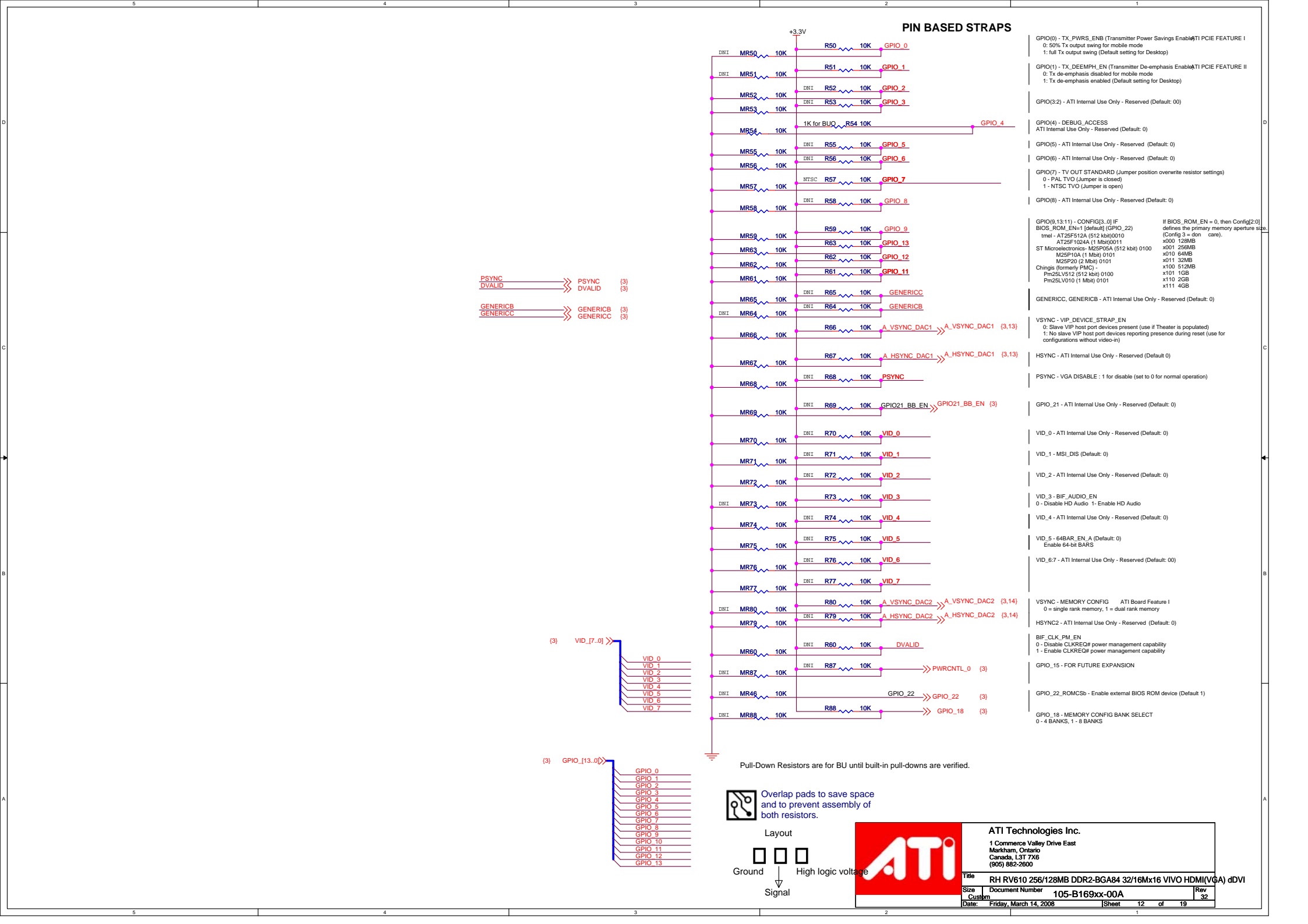
Shared Power Rails



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada L3T 7X6
(905) 882-2800

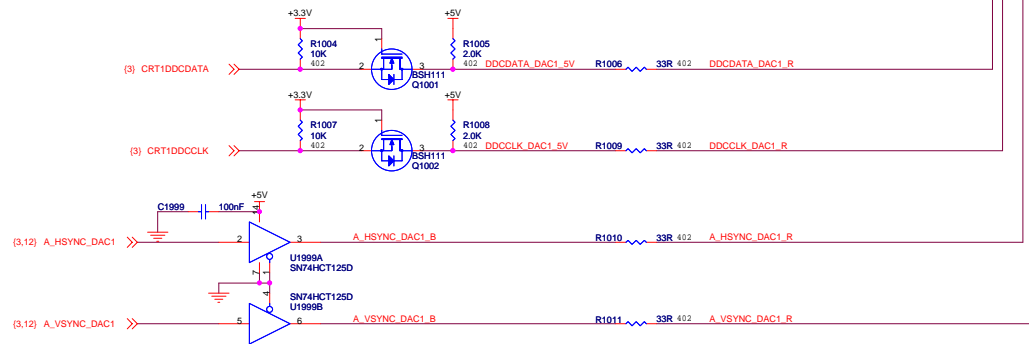
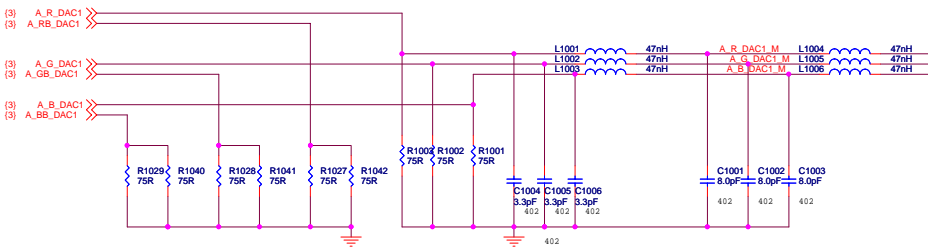
Title RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI

Size C Document Number 105-B169xx-00A Rev 32
Date: Friday, March 14, 2008 Sheet 11 of 19





Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)

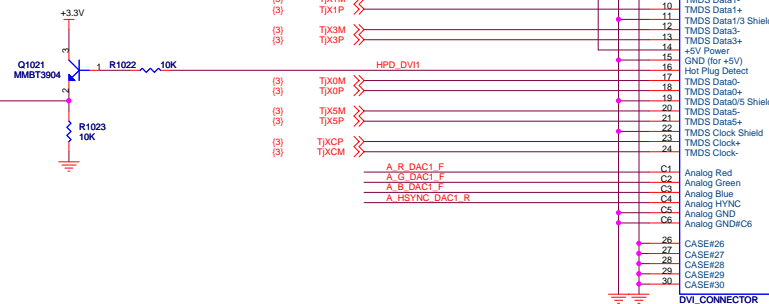


SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional
13	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
14	Monitor ID bit 3	Monitor ID bit 3	Monitor ID bit 3	Monitor ID bit 3	Optional
15	Open	Open	Open	Open	Optional
9	N/C	N/C	N/C	N/C	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

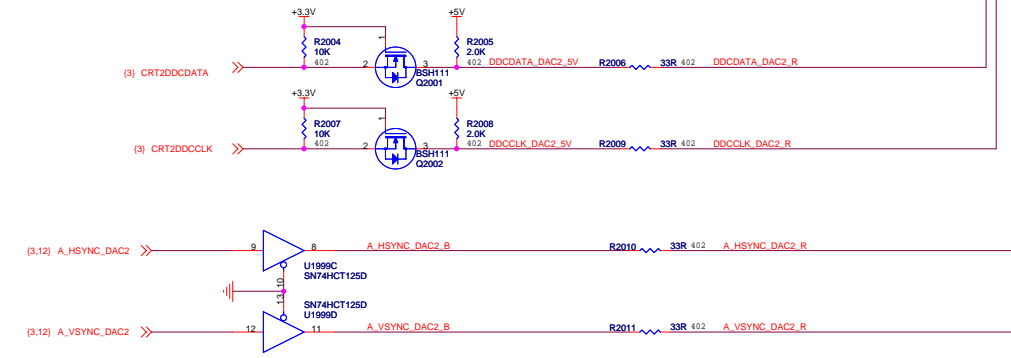
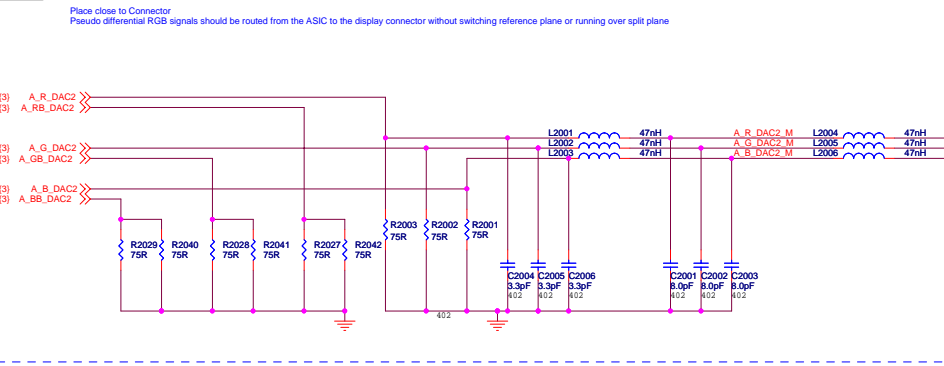
TMDS_2(Daul_Link) + DAC_1-CRT



ATI Technologies Inc.

1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 862-2600

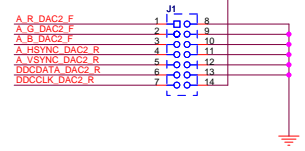
Title RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI
Size Document Number 105-B169xx-00A Rev 32
Date Friday, March 14, 2008 Sheet 13 of 18



SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

Very important to meet HDMI compliance requirements
Capacitance of SDADDC_HDMI & SCLDDC_HDMI nets to Power/GND planes must be less than 50pF (try to make it lower)

55mA current limited +5V rail



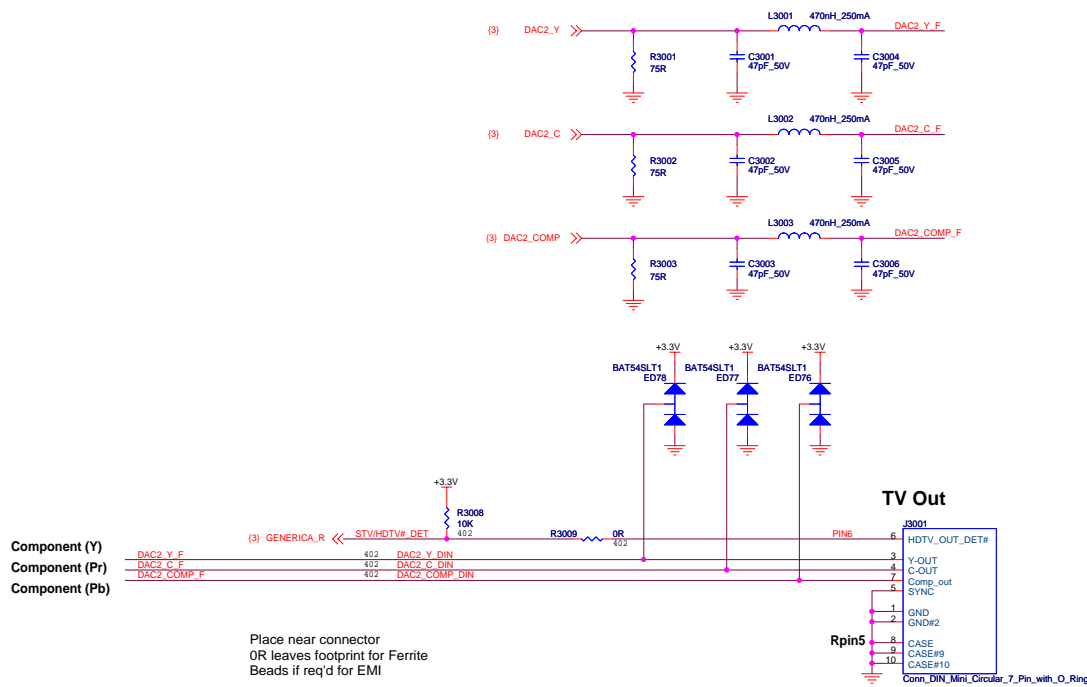
DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	Optional
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	Optional
9	N/C	+5V	+5V	+5V	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

TMD5_1(Single_Link) + DAC_2-CRT



ATI Technologies Inc.			
1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 862-2600			
Title	RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI		Rev
Size	Document Number	105-B169xx-00A	32
Customer			
Date	Friday, March 14, 2008	Sheet	14 of 18



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
 - 7-pin Svideo/Composite MiniDIN P/N 6071001500G
 - 4-pin Svideo MiniDIN P/N 6070001000G

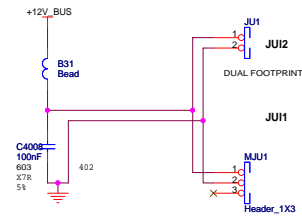
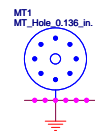
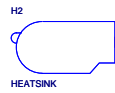


ATI Technologies Inc.

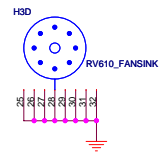
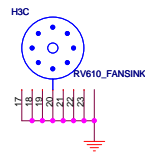
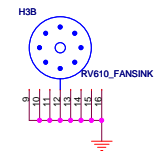
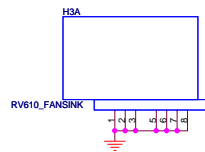
1 Commerce Valley Drive East
 Markham, Ontario
 Canada L3T 7X6
 (905) 882-2600

File RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDV

Size	Document Number	Rev
C	105-B169xc-00A	32
Date:	Friday, March 14, 2008	Sheet 15 of 19



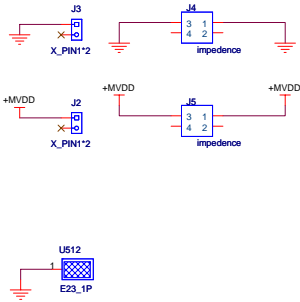
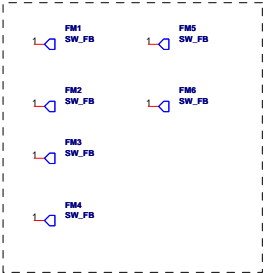
80200439A0G (DVI+HDMI+DIN)



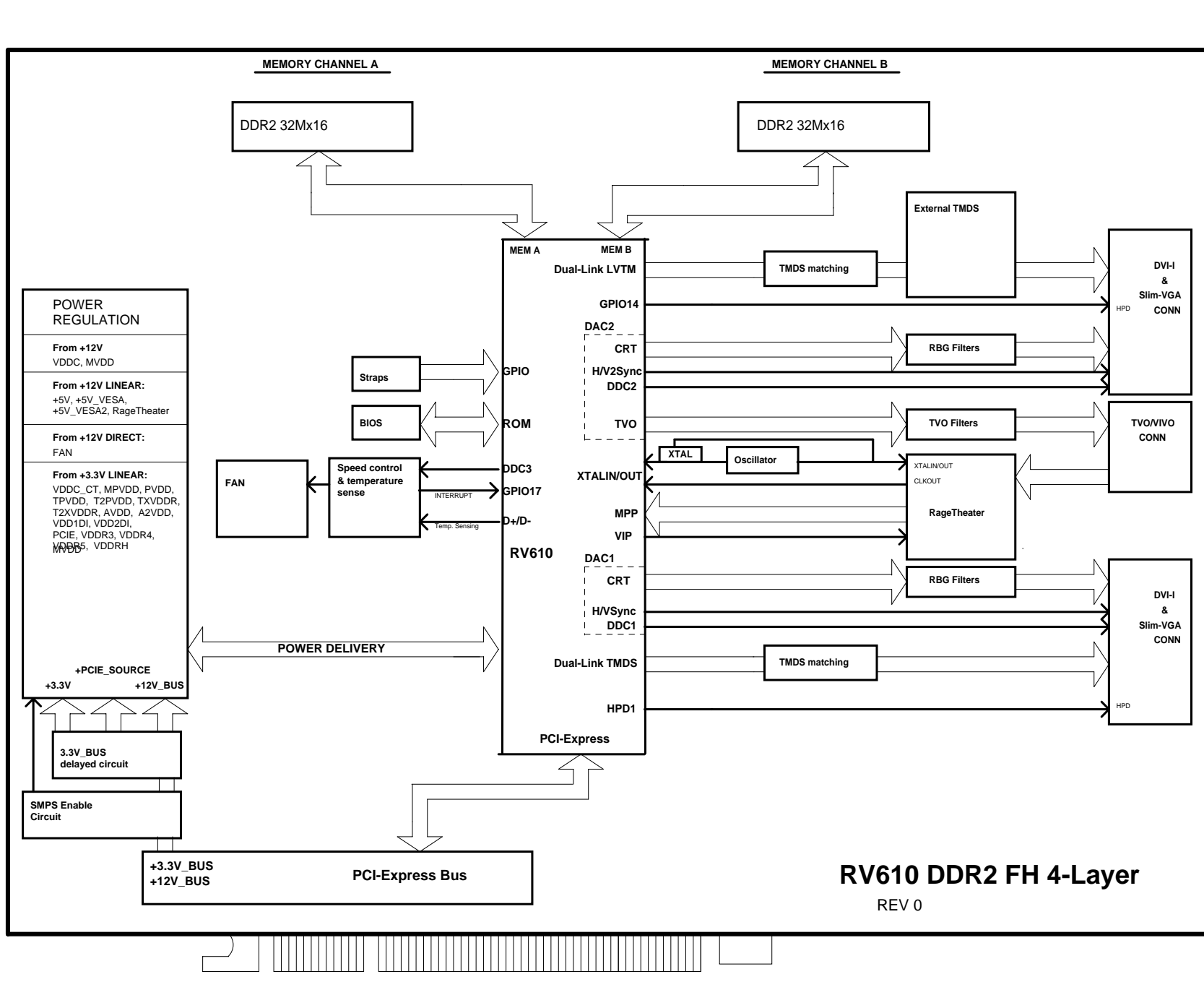
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title		RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI	
Size	Document Number	105-B169xx-00A	Rev
Date:		Friday, March 14, 2008	Sheet 16 of 19

ASSY3
BRACKET
8020040100G



<div><Variant Name></div> <div>ATI</div>			Title		Schematic No.		Date:		
			RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI (VGA) 5-DM9xx-00A				Friday, March 14, 2008		
REVISION HISTORY			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact ATI representative to obtain latest BOM closest to the application desired.				Rev 32		
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION						
		2006.12.01	UPDATE SCHEM. BOM MANAGEMENT.						
		2006.12.14	UPDATE SCHEMATIC TO NETLIST WITH NO ERRORS						
		2006.12.18	DORINA UPDATE MEM SWAP						
		2006.12.19	REMOVE TP ON MEM - TO BE REPLCED BY 0.8MM PADS ON ALL LINES						
		2006.12.20	CHANGED B67 to PN 5260014800G AND C76 to PN 4172010500G						
0	00A	2006.12.21	J2 REMOVED						
		2007.01.15	NC626 removed (VDDC output cap). LDO output resistor (R879, R880) moved closer to LDO. MVDD LDO input resistors changed to 1R. Debug header changed to include Gen1/2 switch. HDMI caps removed. Added thermal shutdown option to power sequencing.						
		2007.01.16	REMOVE BACK BIAS, REMOVE MC624						
		2007.01.17	REMOVE R5515, R5516, R5521, R5524 REMOVE R94						
		2007.01.22	ADDED H3, H4, H5						
		2007.01.22	DECAP CHANGES ON PAGE 3						
		2007.01.23	HEATSINK GROUNDING ADJUSTED						
		2007.01.23	DORINA - HEATSINK GNDING PINS ADJUSTED						
		2007.01.24	RM JTAG + SMA CLOCK CONNECTIONS TO EASE LAYOUT CONGESTION						
		2007.01.24	ADDED C300, C301, C302 (STITCHING CAPS) TO IMPROVE DDC LINES						
		2007.01.24	FIXED ORCAD NETLIST PROBLEM; NO EFFECTIVE CHANGE.						
		2007.01.24	ADD Q102 TO SOLVE A11 VDDR3 LEAKAGE PROBLEM.						
1	00B	2007.01.25	CHNG REF DES OF VDDR3 LEAKAGE BLOCK TO Q/R-90						
2	00C	2007.02.09	PCB mechanical updates only. No Schematic changes.						



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDMI(VGA) dDVI		
Size	Document Number	105-B169xx-00A	Rev 32
C	Date:	Friday, March 14, 2008	Sheet 19 of 19