

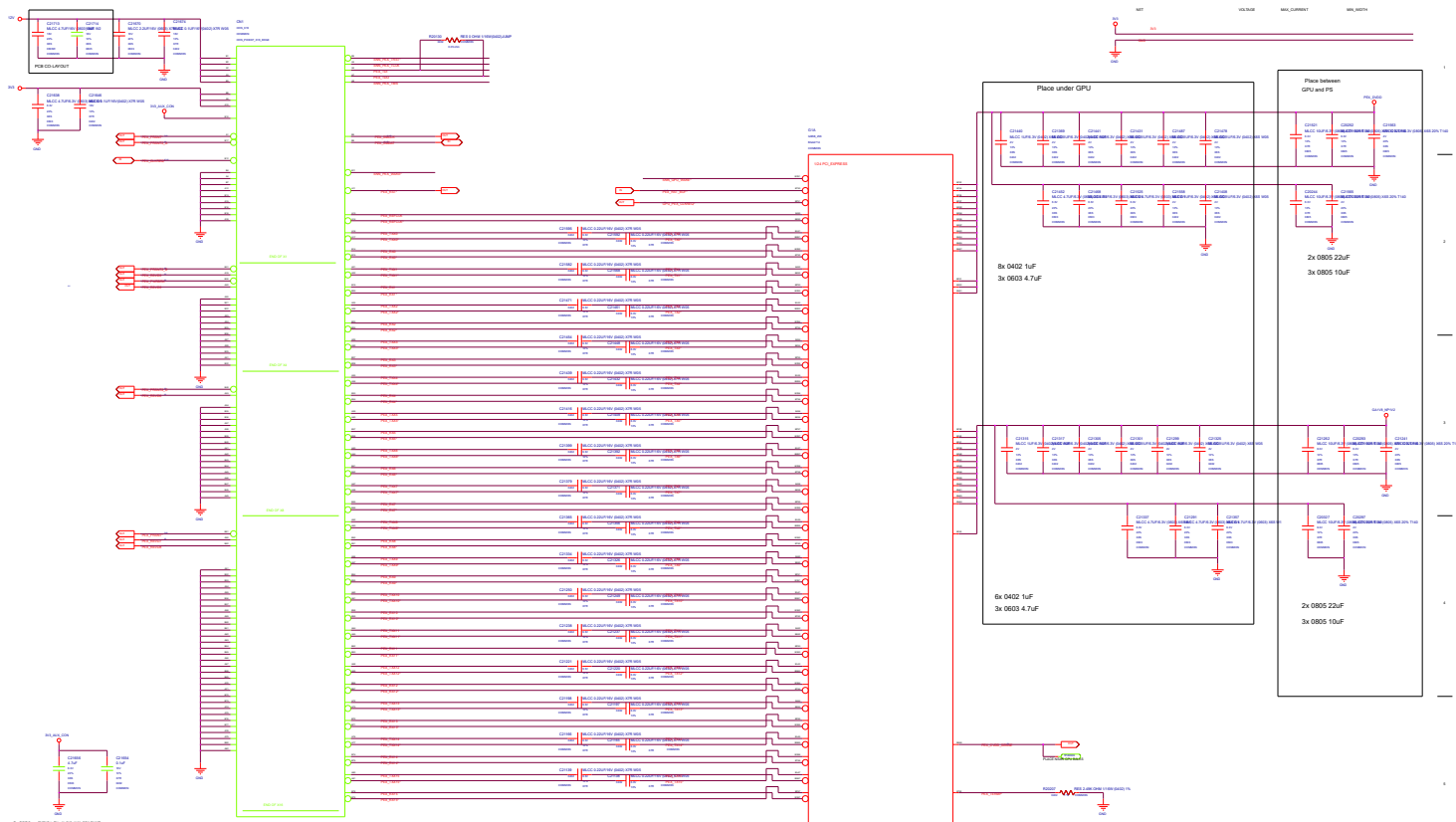
DP + DP + DP + HDMI/DP

Page	Description
1	Table of Contents
2	BLOCK DIAGRAM
3	PCI EXPRESS
4	MEMORY: GPU PARTITION A/B
5	MEMORY: FBA PARTITION(3:1.0)
6	MEMORY: FBA PARTITION(8:3.32)
7	MEMORY: FBB PARTITION(3:1.0)
8	MEMORY: FBB PARTITION(8:3.31)
9	MEMORY: GPU PARTITION C/D
10	MEMORY: FBC PARTITION(3:1.0)
11	MEMORY: FBC PARTITION(8:3.32)
12	MEMORY: FBD PARTITION(3:1.0)
13	MEMORY: FBD PARTITION(8:3.32)
14	- BLANK -
15	- BLANK -
16	- BLANK -
17	- BLANK -
18	- BLANK -
19	MEMORY DECOUPLING
20	GPU: GND, NC
21	GPU: GPU POWER
22	GPU: NVDDO DECOUPLING(1/2)
23	GPU: NVDDO DECOUPLING(2/2)
24	GPU: FBVDDO DECOUPLING
25	- BLANK -

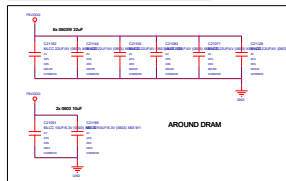
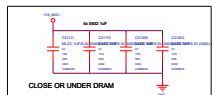
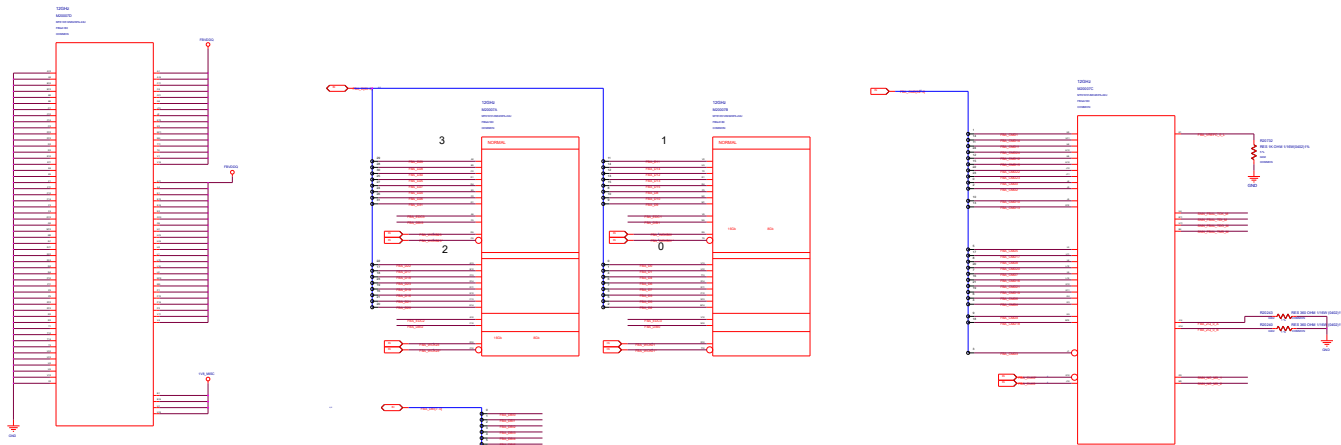
Page	Description
26	GPU, GPIO, THERMAL, JTAG
27	IPFAM, IPFB, UNUSED, NP, IPFE
28	IFPC, HDMIOP, NP, IPFA
29	IFPD, DP, NP, IPFB
30	IPFE, DP, NP, IFPC
31	IPFF, DP, NP, IPFD
32	MISC, ROM, STRAPS
33	MISC, XTAL, PLL
34	PS, 5V
35	PS: PEX_DVDD, GAT1V8, NP1V2
36	PS: NP1V8(NP ONLY), 1V8_MISC
37	PS: FBVDDQ_OV/R3
38	PS: FBVDD_PH2 (PWM2)
39	PS: FBVDD_PH3 (PWM3) and PH4 (PWM1)
40	PS: FBVDD_OUTPUT_CAP_NEAR_VR
41	PS: FBVDD_OUTPUT_CAP_NEAR_MEMORY
42	PS: NVDD Controller
43	PS: NVDD Controller Sense
44	PS: NVDD PH1A, PH1B
45	PS: NVDD PH1C, PH2A
46	PS: NVDD PH2B, PH2C
47	PS: NVDD PH3A, PH3B
48	PS: NVDD PH3C, PH4A
49	PS: NVDD PH4B, PH4C
50	PS: NVDD PH5A, PH5B

Page	Description
51	PS: NVDD PH5C, PH6A
52	PS: NVDD PH6B, PH6C
53	PS: NVDD PH7A, PH7B
54	PS: NVDD PH7C, PH8A
55	PS: NVDD PH8B, PH8C
56	PS: INPUT CAP
57	PS: NVDD OUTPUT CAP
58	-BLANK-
59	-BLANK-
60	SP_FLLVDD LDO_LOADSWITCH
61	-BLANK-
62	PS: INPUTS, FILTERING, MONITORING
63	PS: PREFILTER
64	BLANK
65	SEQ: 5V, GA1V8, NP1V2 EN, 3V3_SEQ, 3V3_PROT
66	SEQ: NV, PEX, FB EN
67	SEQ: MISC, PEX3V3 MONITOR
68	FAN & NORTH LOGO LED
69	XV LEDs
70	MECH & VR THERMAL PROTECTION
71	PCIe TERM
72	KICKER









FBIWDOO DECAP per diamsell pair

Close to DRAM:

18x 10uF 0402

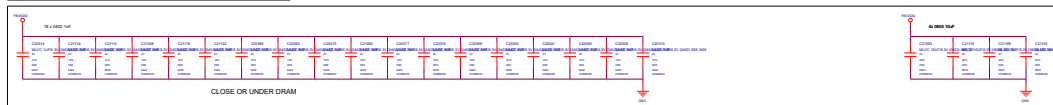
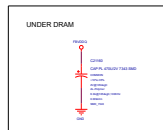
4x 10uF 0603

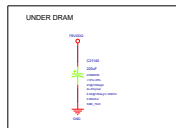
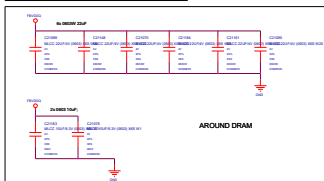
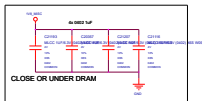
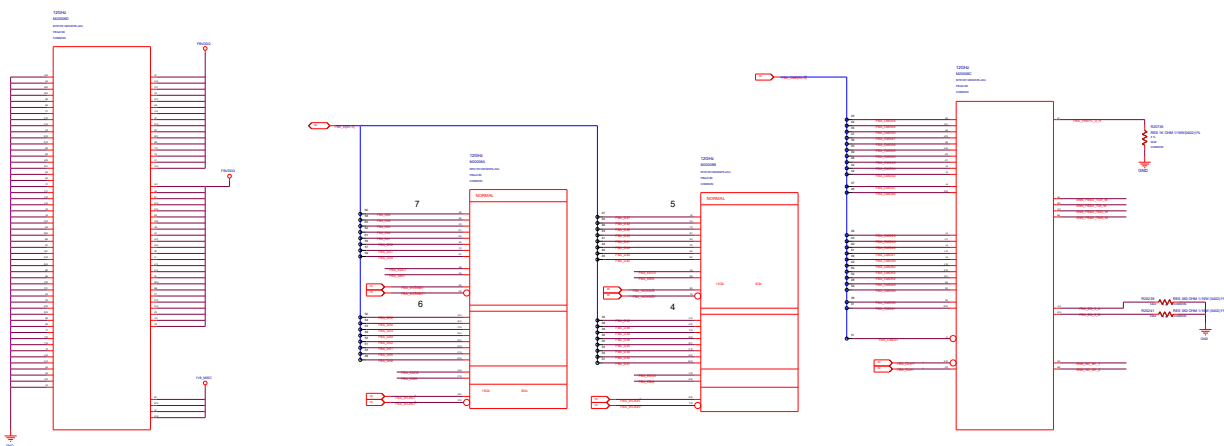
Need at least 2 gnd and 2 pwr vias per DECAP

Around DRAM:

2x 10uF 0603

6x 22uF 0603W





FBVDDQ DECAP per clamshell pair:

Close to DRAM:

18x 1uF 0402

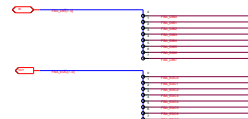
4x 10µF 0603

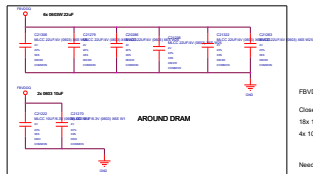
Around DRAM:

2x 10 μ F 0603

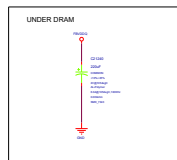
6x 22 μ F 0503W

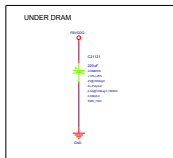
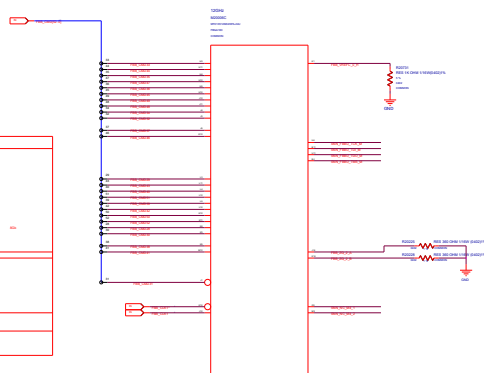
Need at least 2 gnd and 2 pwr vias per DECAP





Need at least 2 gnd and 2 pwr vias per DECAP



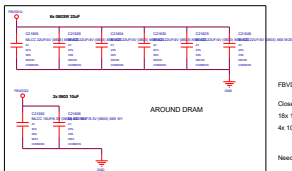
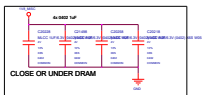
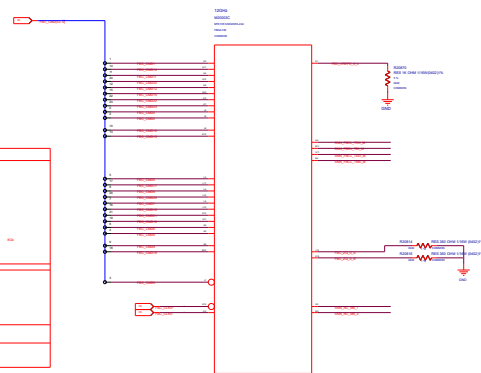
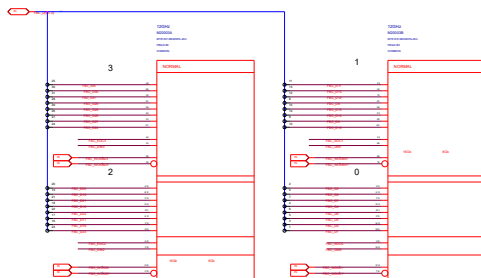
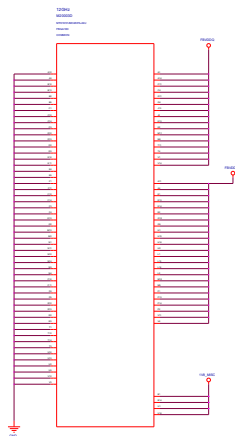


Around DRAM:
2x 10uF 0603
6x 22uF 0603W

CLOSE OR UNDER DRAM







FBC/ODD DECAP per damshell pair

Close to DRAM:

15x 10uF 6002

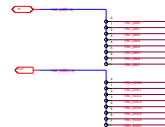
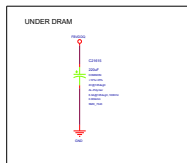
4x 10uF 6003

Around DRAM:

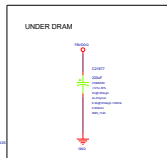
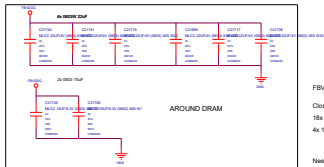
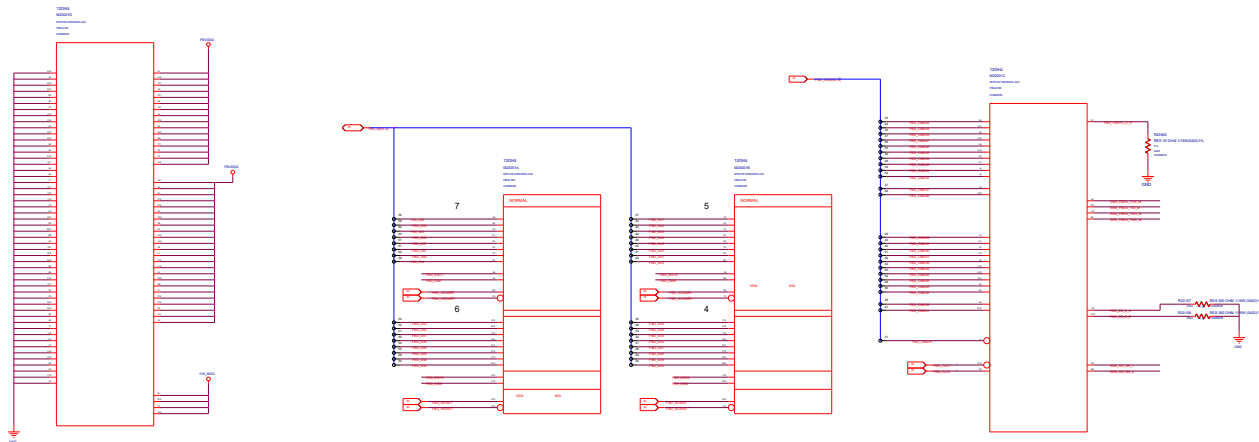
2x 10uF 6005

6x 22uF 9600W

Need at least 2 grid and 2 per vias per DECAP





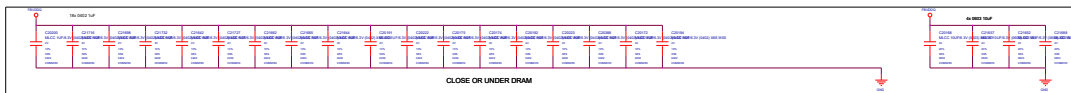


FBDVDDQ DECAP per clammshell pair:

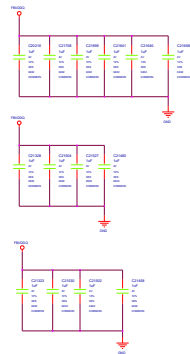
Close to DRAM:
18x 1uF 0402
4x 10uF 0603

Around DRAM:
2x 1uF 0402
6x 22uF 0603W

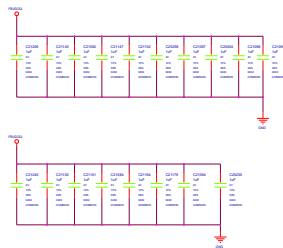
Need at least 2 gnd and 2 pwr vias per DECAP



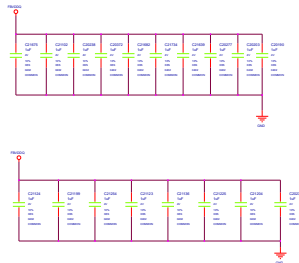
PLACE AROUND EAST DRAM



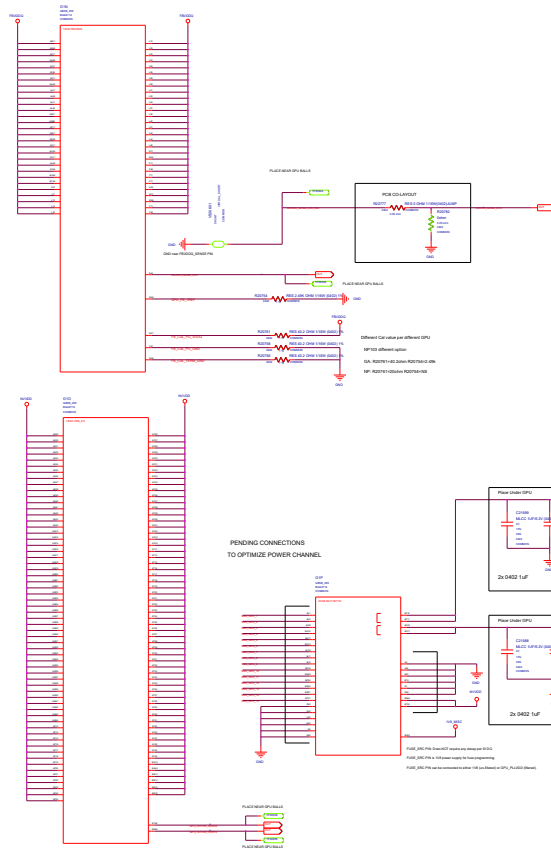
PLACE AROUND WEST DRAM



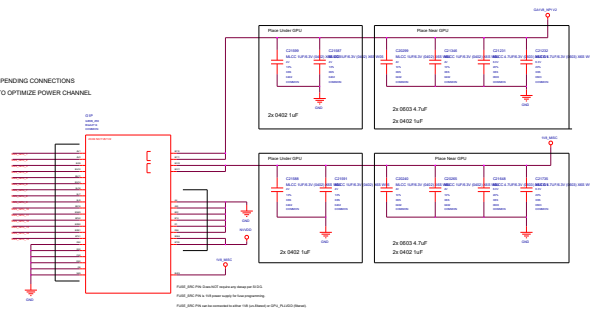
PLACE NORTH DRAM





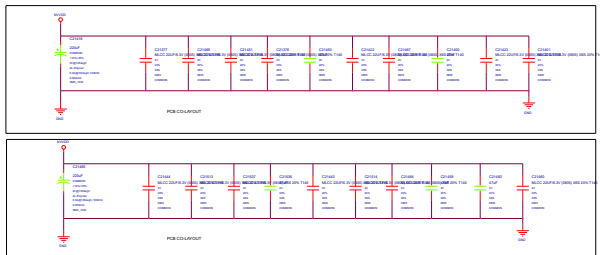


PENDING CONNECTIONS
TO OPTIMIZE POWER CHANNEL



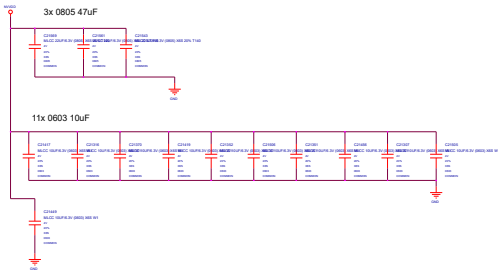
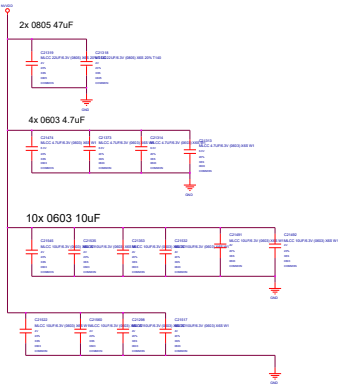
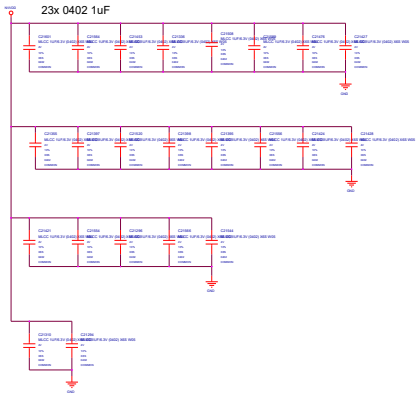
NVVDD

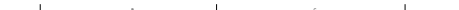
UNDER GPU



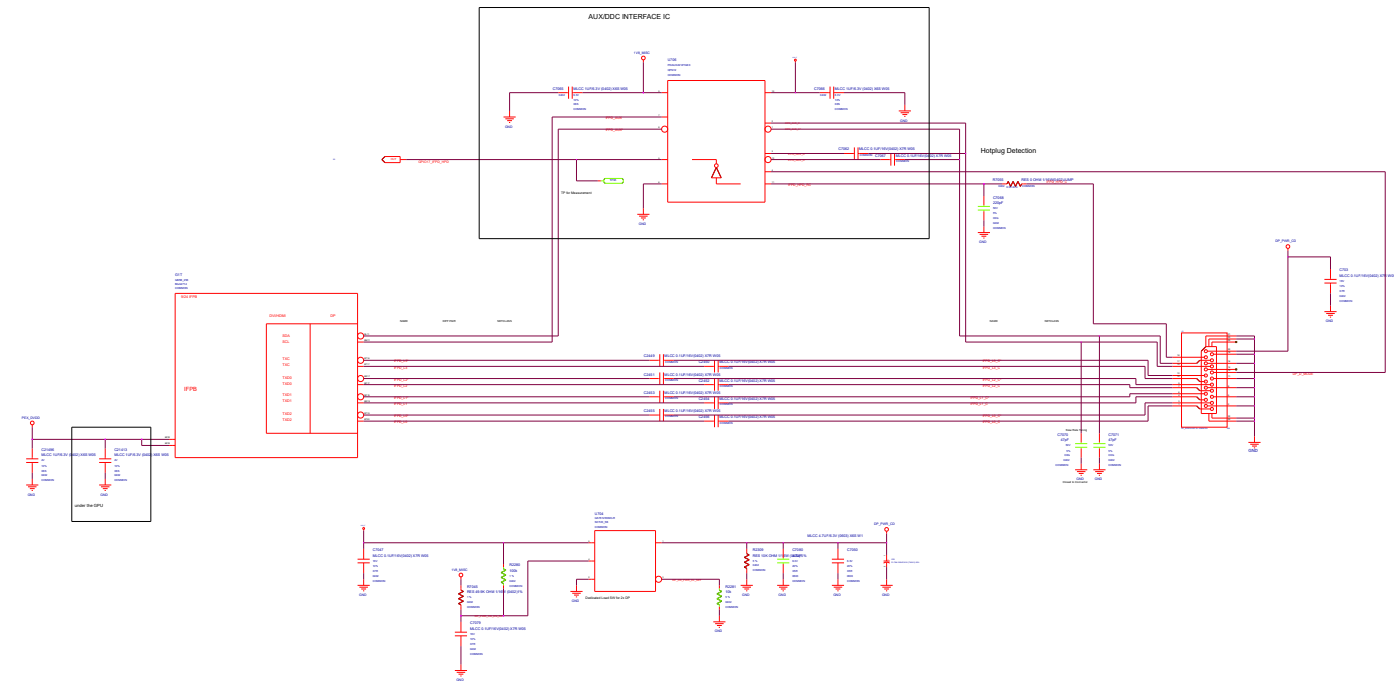
UNDER GPU

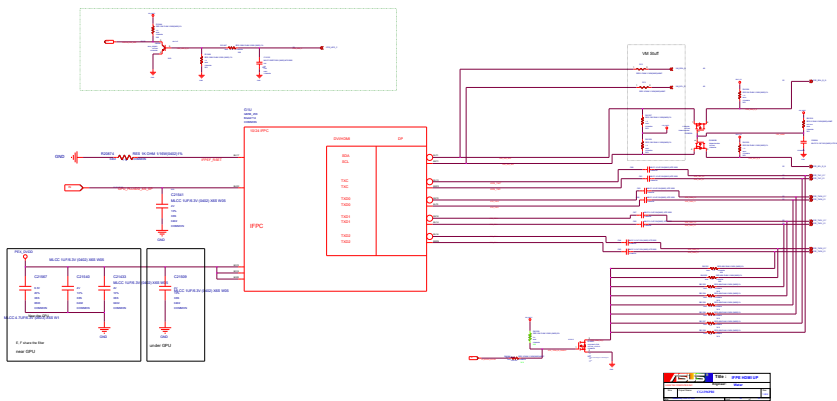
NVVDD

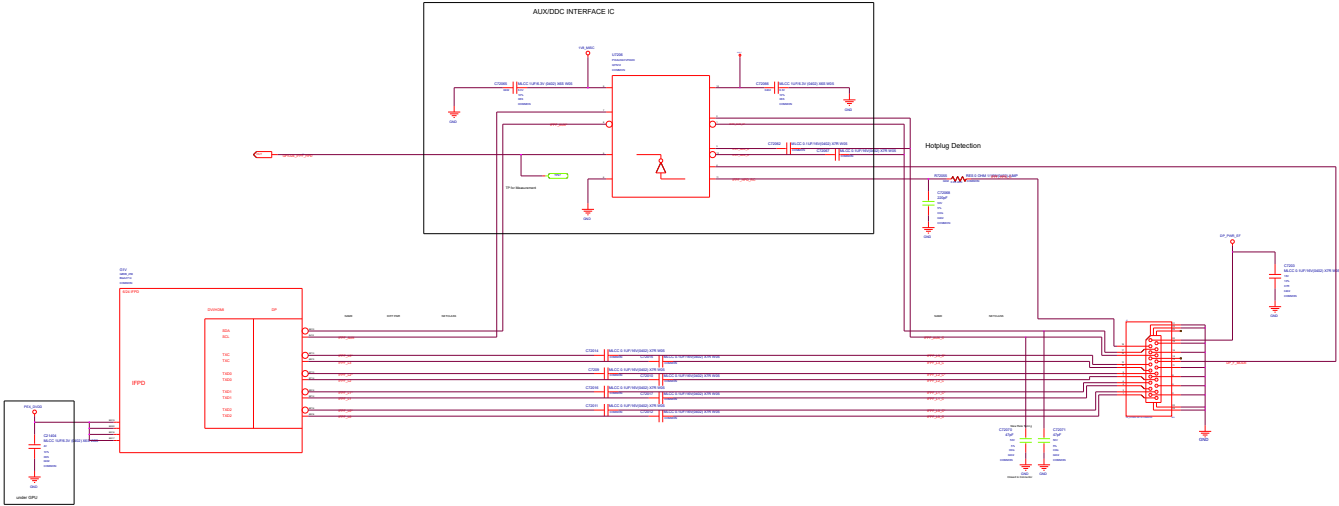












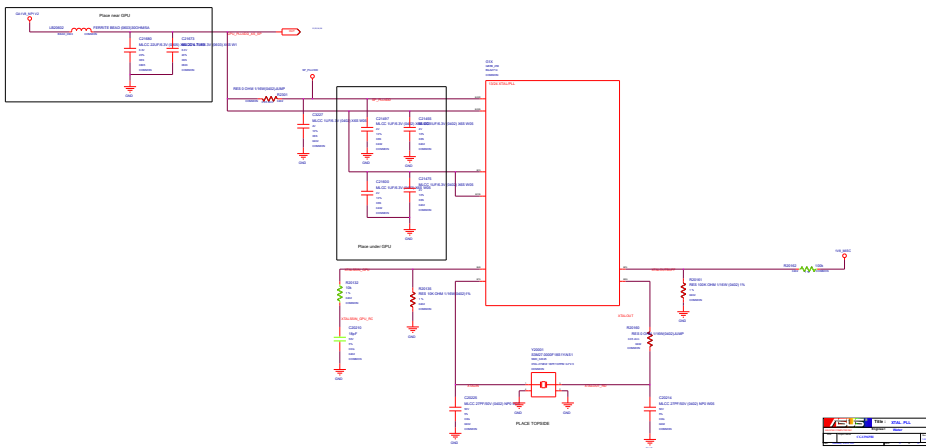
GROUP2

ROM_S0	ROM_S1	ROM_SCLK	SMARTFAN2-S1FS_OVERT	1:ENABLE 0:DISABLE
L	M	L	1001	FAN2[1]=33%~32%, FS_OVERT ENABLE

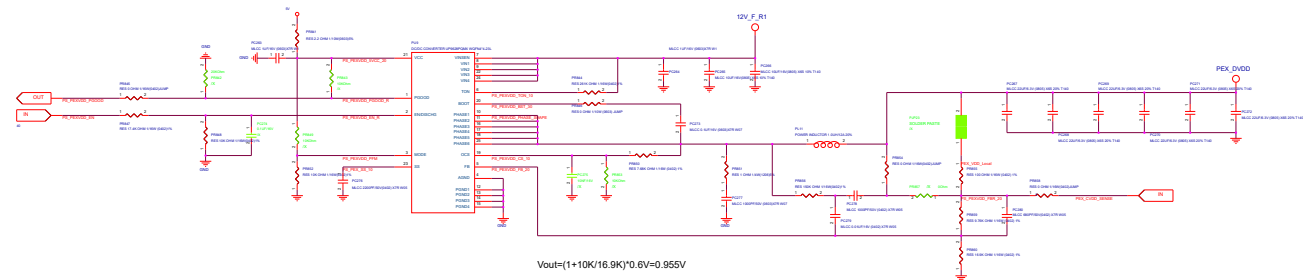
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

←-DEFAULT

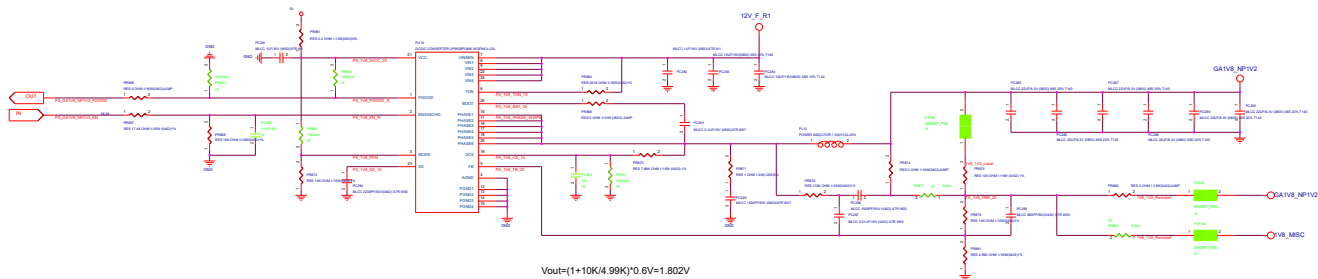




PEX_DVDD

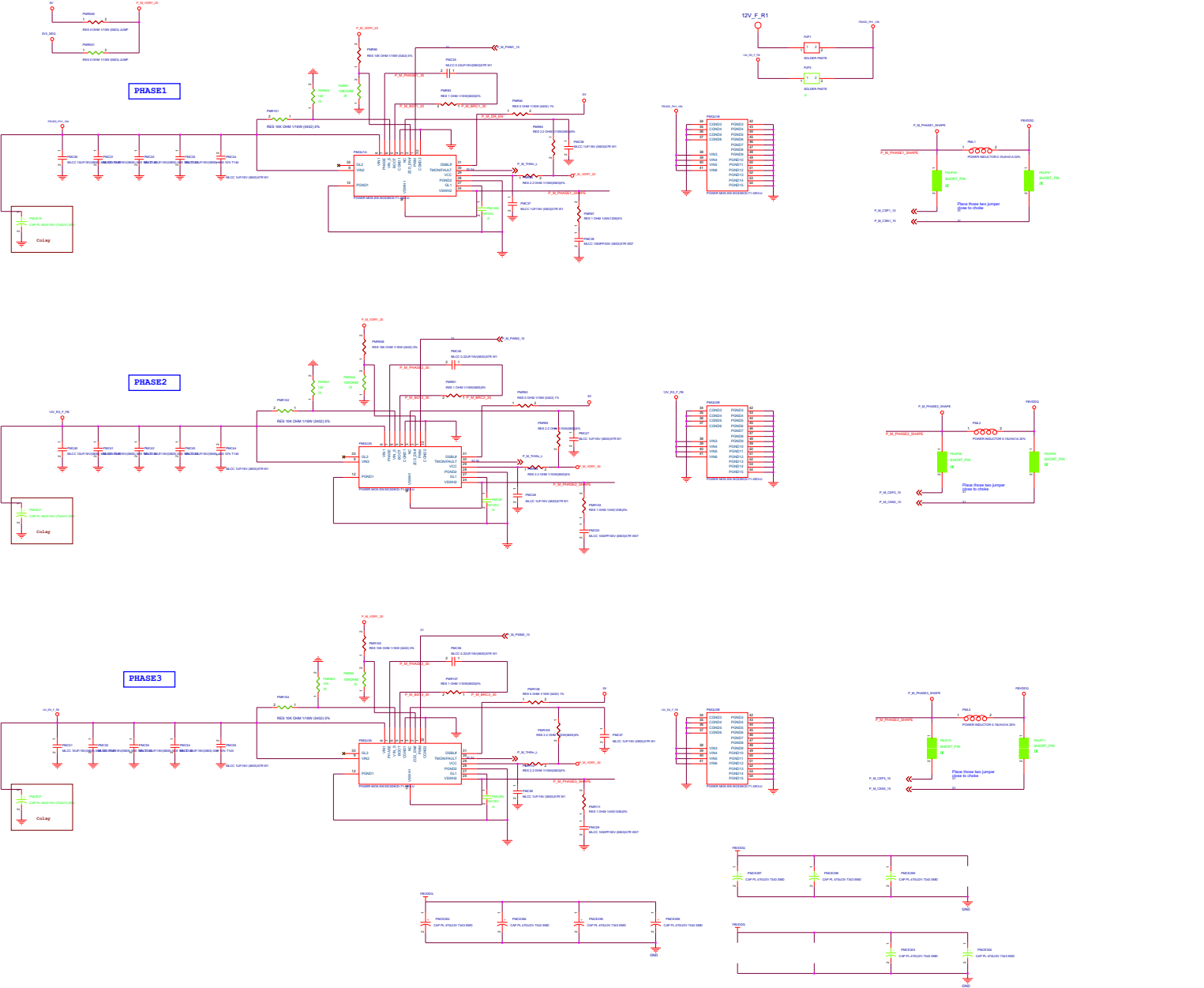


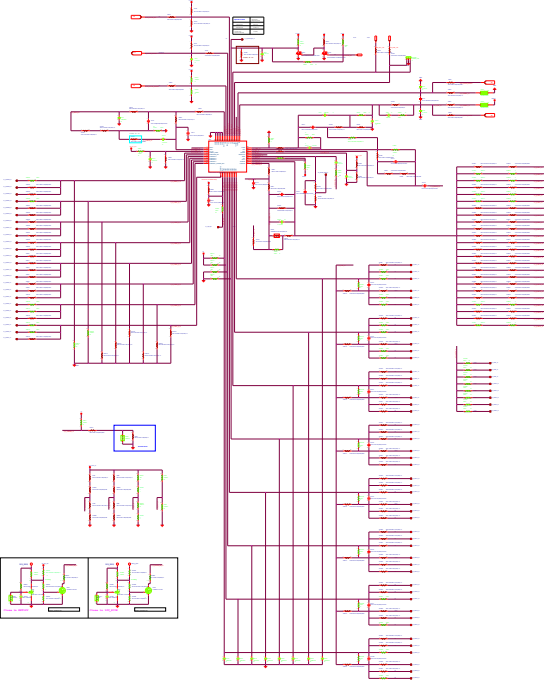
1V8(1V2 for NP; 1V8 for GA102)

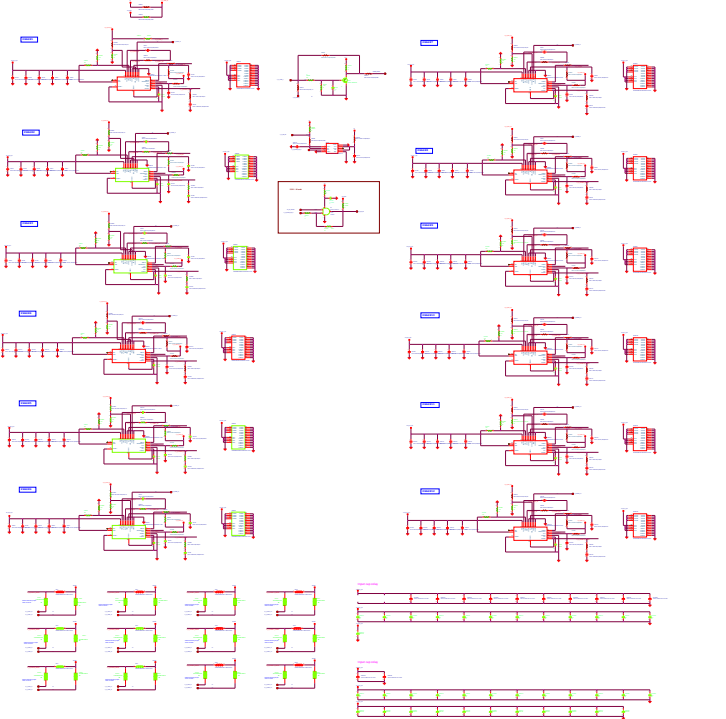


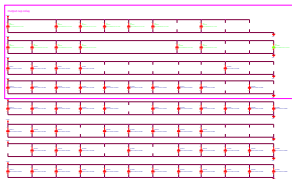
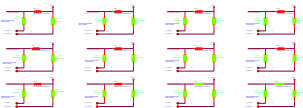
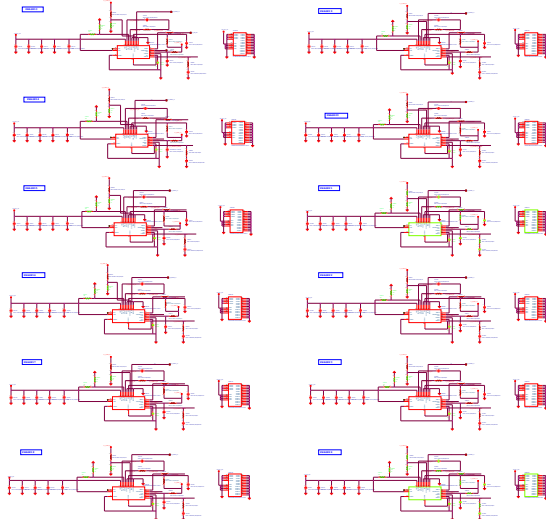


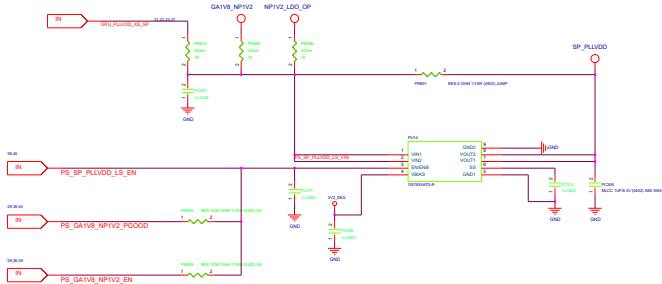
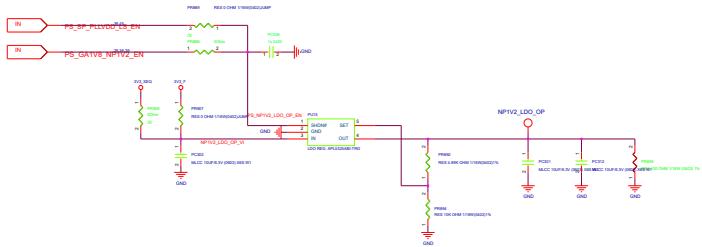


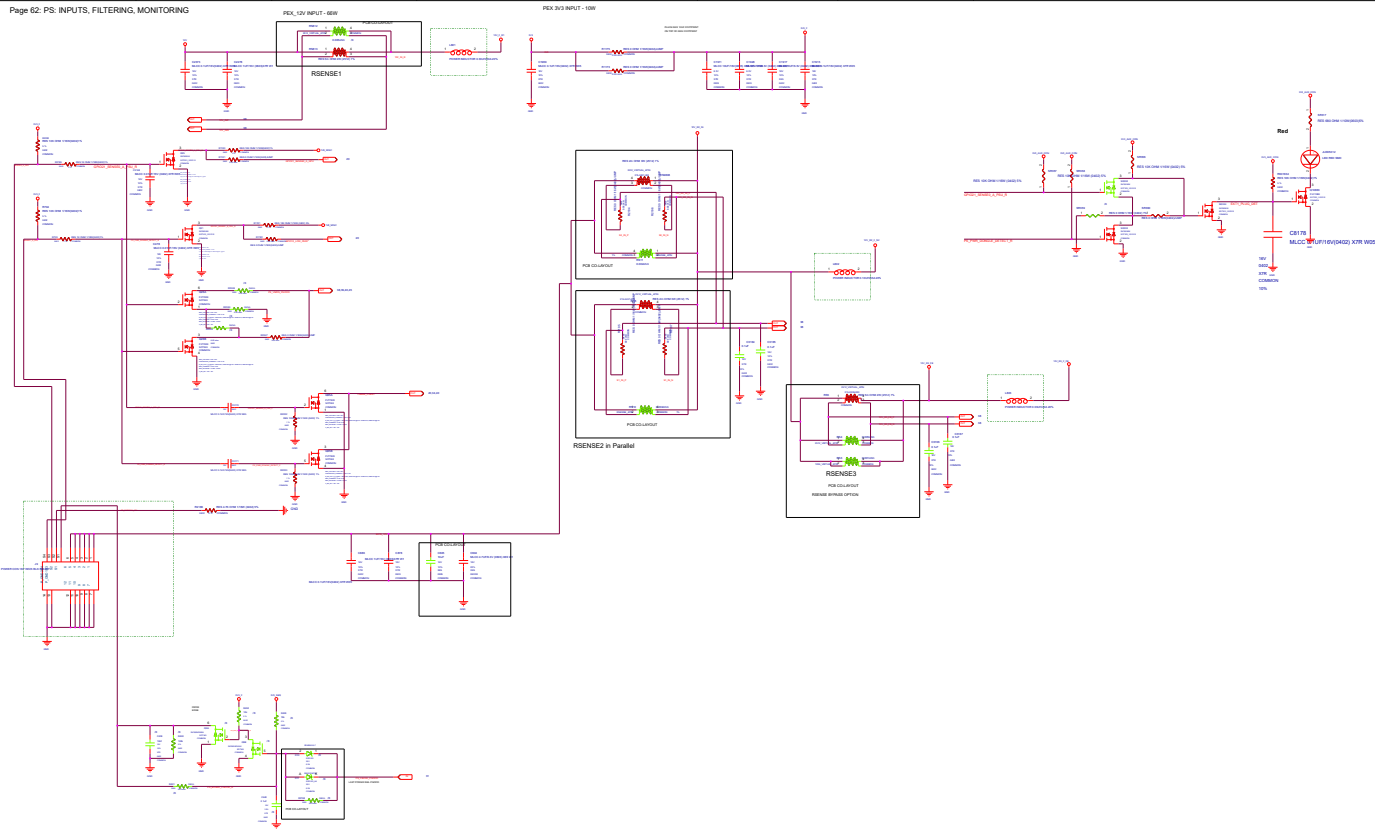


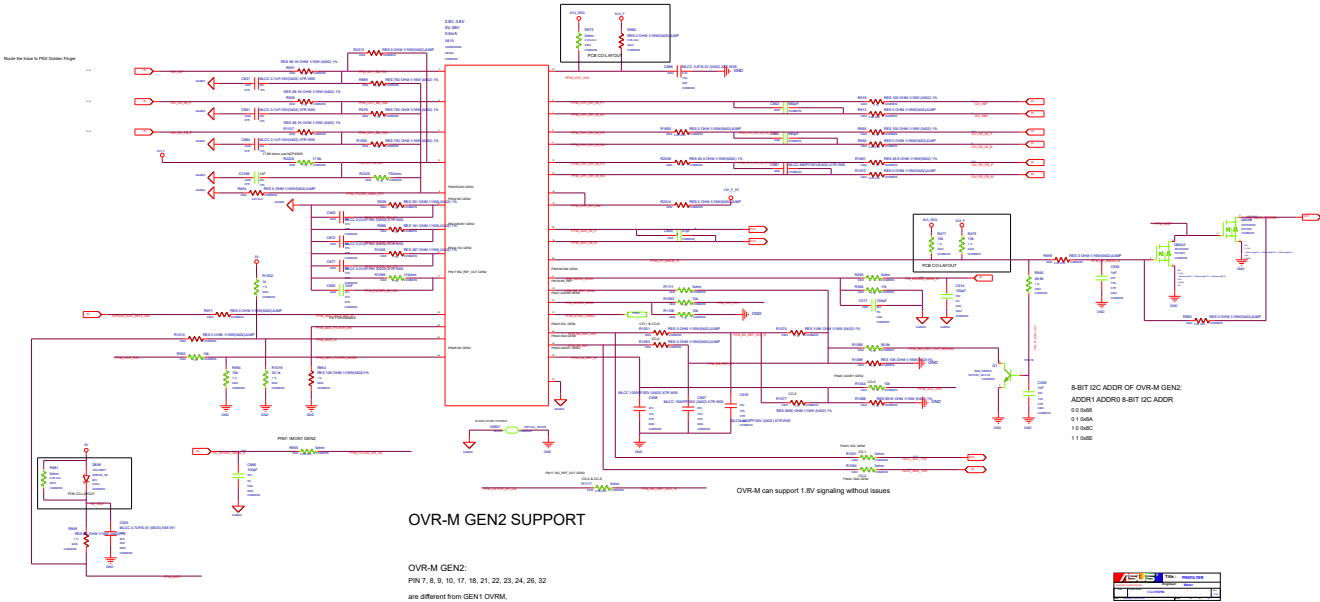


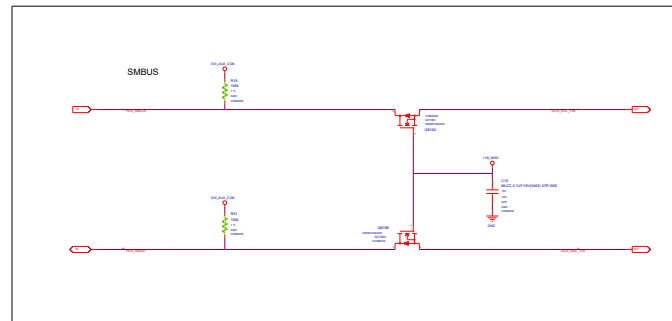
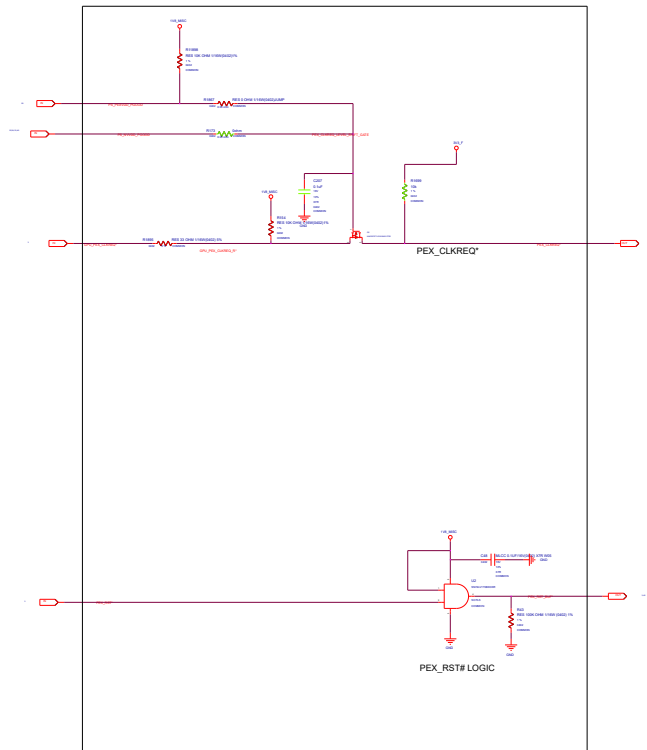






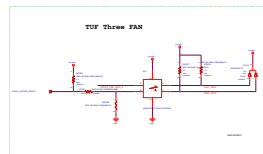
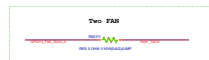
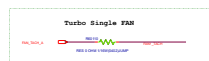
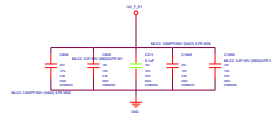
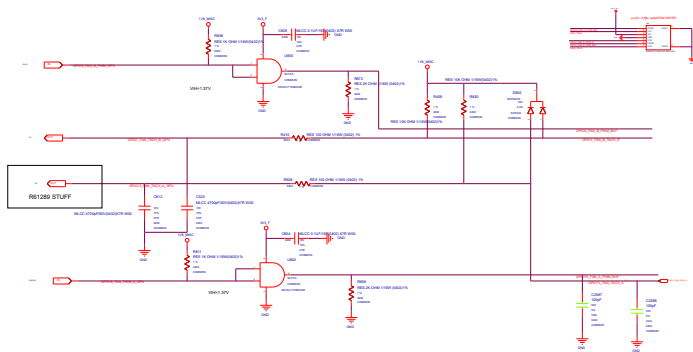




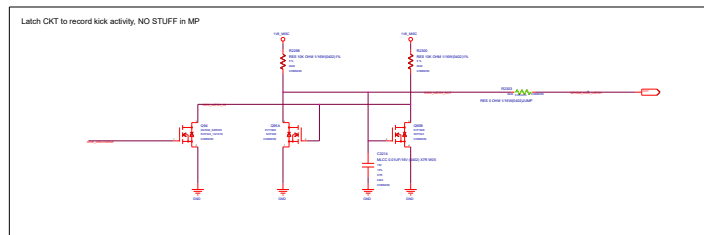
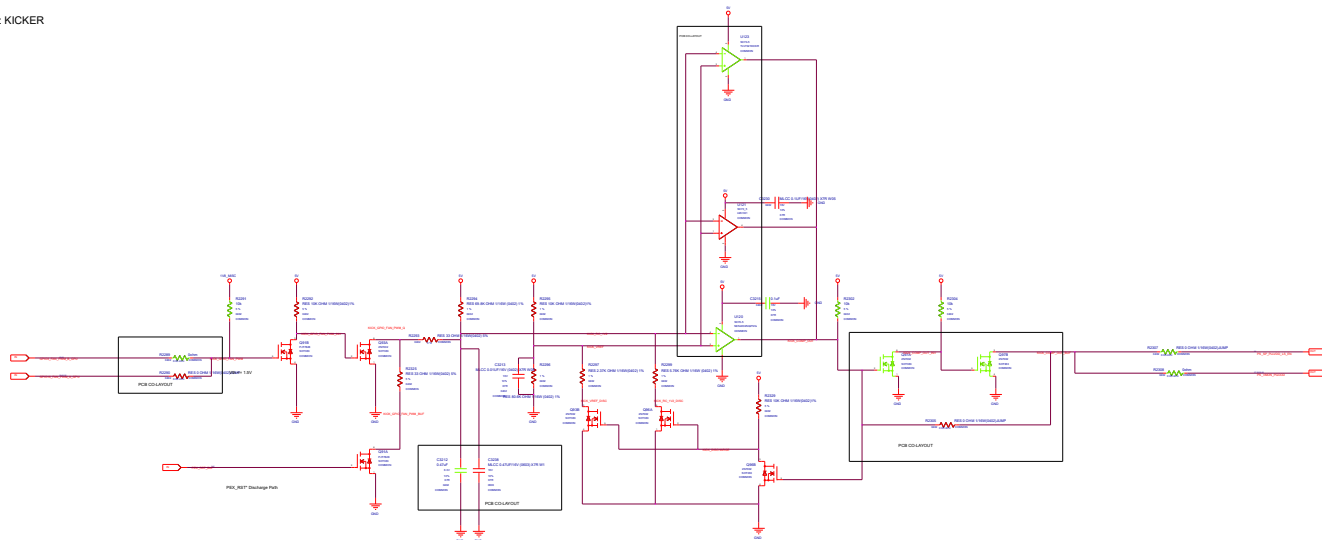


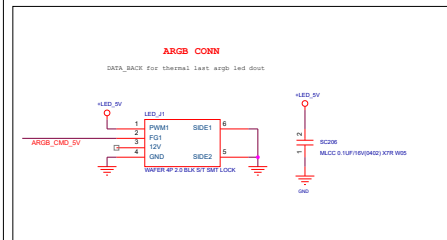
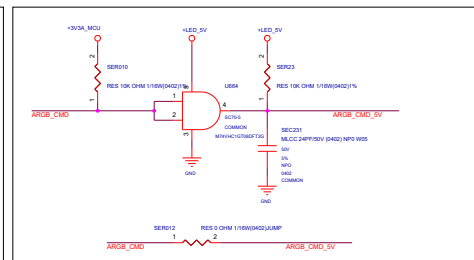
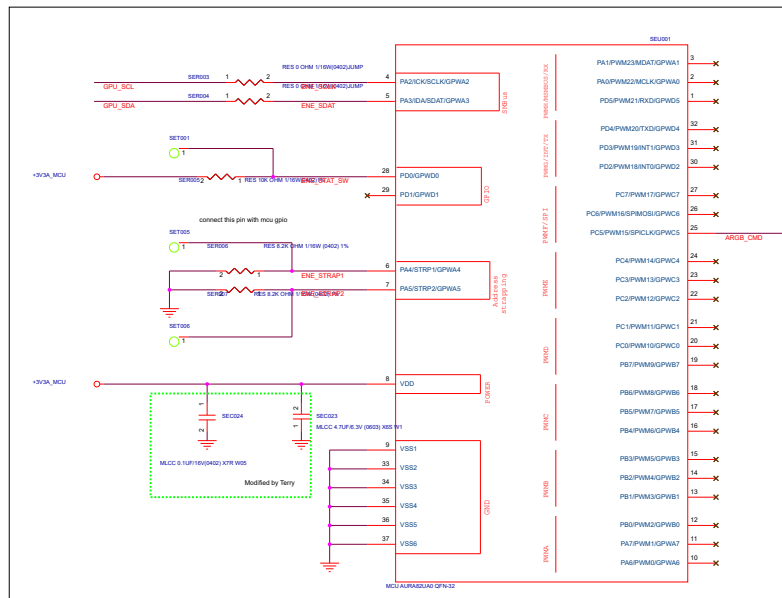
REMOVE PEX3V3 MONITOR





ASUS		Title: PSA	
Source: Newspaper/Periodical		Keywords: Water	
Date:	CICL 04/09/2002		





Power



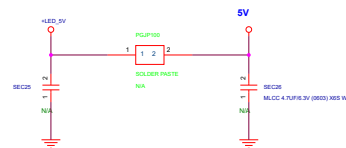
PCIe bus 3.3V AUX (for ITE)

I2C



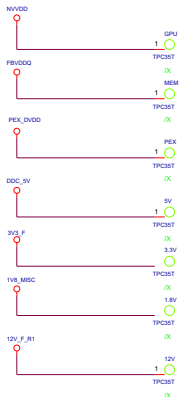
GPU I2CB Master (to ITE)

MLCC 4.7uF/5.3V (0603) XES W1



ASUS VGA Screws and PCB Holes

Power_test_point



X-clip Holes for GPU Thermal Module

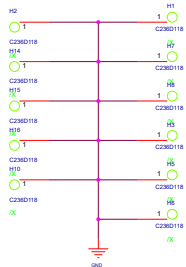
Drill: 3.8mm
Top Circle: 6mm
Bottom Circle: 10mm



Note: If you need to use Spring screws for Thermal Module, DON'T use these parts!
Please discuss this with your ME RD.

Screws for Back Plate
Screw P/N: 13050-72805045

Drill: 3mm
Top Circle: 6mm
Bottom Circle: 6mm



Note: Please change the hole quantity according to actual requirement.

NP1V2_LDO_OP











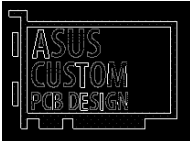






SP_PLLVDD

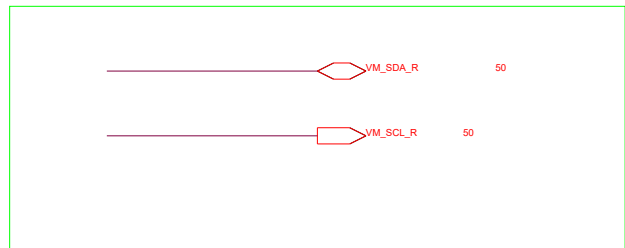
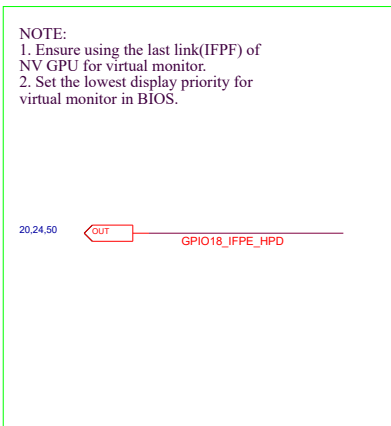
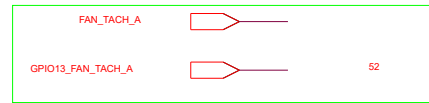
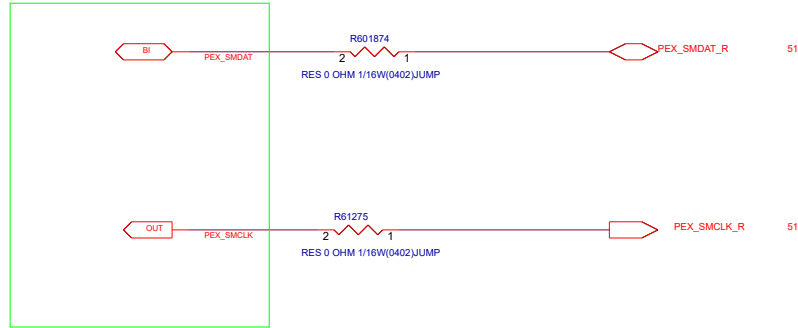
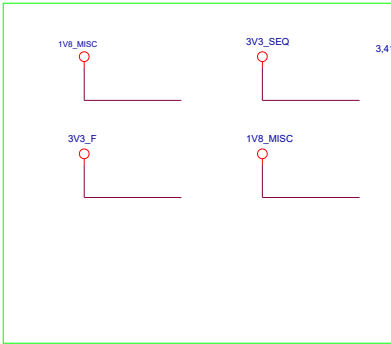


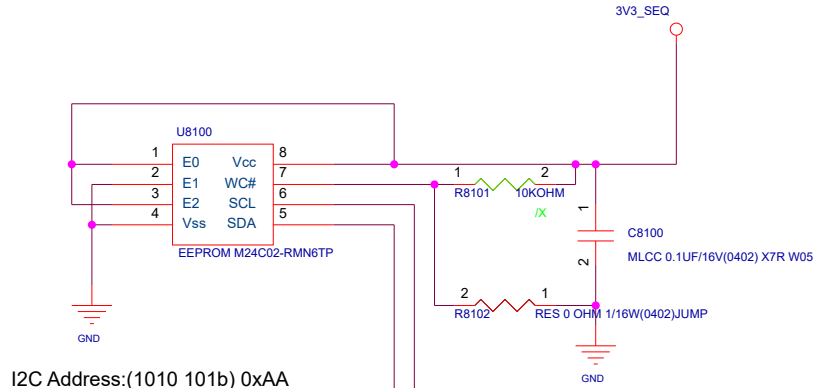
GND



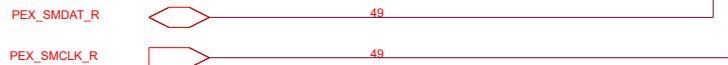
ASUS VGA PCB Logo


<div><div>LOG001</div><div><div>1</div><div>CE</div><div>JK</div></div></div> <div></div>	<div><div>LOG008</div><div><div>1</div><div>ROHS</div><div>ROHS</div><div>JK</div></div></div> <div></div>																
<div><div>LOG002</div><div><div>1</div><div>VCCI</div><div>JK</div></div></div> <div></div>	<div><div>LOG009</div><div><div>1</div><div>PCB MADE IN CHINA</div><div>PCB_MADE_IN_CHINA</div><div>JK</div></div></div> <div><div>PCB MADE IN CHINA</div></div>																
<div><div>LOG003</div><div><div>1</div><div>EMI_D33005_H</div><div>EMI_D33005_H</div><div>JK</div></div></div> <div></div>	<div><div>LOG009</div><div><div>1</div><div>MARK_1</div><div>MARK_1</div><div>JK</div></div></div> <div></div>																
<div><div>LOG004</div><div><div>1</div><div>FCC</div><div>JK</div></div></div> <div></div>	<div><div>LOG001</div><div><div>1</div><div>WEEE_LOGO</div><div>WEEE_LOGO</div><div>JK</div></div></div> <div></div> <div><div>ASUS Re-design logo</div><div>Do not place this on reference board</div></div>																
<div><div>LOG005</div><div><div>1</div><div>FCM</div><div>FCM</div><div>JK</div></div></div> <div></div>	<div><div>LOG003</div><div><div>1</div><div>ASUS CUSTOM PCB DESIGN</div><div>ASUS_CUSTOM_PCB</div><div>JK</div></div></div> <div></div>																
<div><div>LOG006</div><div><div>1</div><div>CAN ICES-003(B)/NMB-003(B)</div><div>CAN_ICES_003_NMB_003</div><div>JK</div></div></div> <div><div>CAN ICES-003(B)/NMB-003(B)</div></div>	<div><div>LOG009</div><div><div>1</div><div>SFIS</div><div>SFIS</div><div>JK</div></div></div> <div></div> <div>place two SFIS outlines on each side of PCB</div>																
<div><div>LOG007</div><div><div>1</div><div>RoHS</div><div>RoHS</div><div>JK</div></div></div> <div></div>	<div><div>LOG009</div><div><div>1</div><div>UKCA</div><div>UKCA_0000</div><div>JK</div></div></div> <div></div> <div><table><tr><td colspan="2"></td><td colspan="2">Title : PCB Logo</td></tr><tr><td colspan="2">ASUSTEK COMPUTER INC.</td><td colspan="2">Engineer: Alex Luo</td></tr><tr><td>Size</td><td>Project Name</td><td>CG1396PBI</td><td>Rev 1.00X</td></tr><tr><td colspan="2">Date: Wednesday, June 01, 2022</td><td>Printed</td><td>08 08 07</td></tr></table></div>			Title : PCB Logo		ASUSTEK COMPUTER INC.		Engineer: Alex Luo		Size	Project Name	CG1396PBI	Rev 1.00X	Date: Wednesday, June 01, 2022		Printed	08 08 07
		Title : PCB Logo															
ASUSTEK COMPUTER INC.		Engineer: Alex Luo															
Size	Project Name	CG1396PBI	Rev 1.00X														
Date: Wednesday, June 01, 2022		Printed	08 08 07														





Change to I2CS(1V8) add R8103



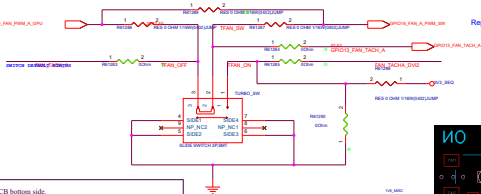
		Title : FRU	
ASUSTEK COMPUTER INC		Engineer: Water	
Size	Project Name CG1396PBI		Rev 1.00X
Date: Wednesday, June 29, 2022	Sheet	51	of 52

NOTE:

1. Disconnect fan tach signal between FAN CON and GPU GPIO PIN, and add off-page symbol on each side.
 2. Connect the fan tach off-page symbol from FAN CON to U10831 pin1.
 3. Connect the fan tach off-page symbol from GPU GPIO to CQ99 pin2.
 4. Mount R61272/unmount R61271 if FAN TURBO function was needed.
- Otherwise, unmount all parts in this page except R61271 to restore original fan tach route: FAN CON—GPU.

FROM GPU GPIO16

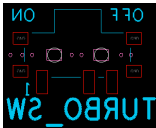
GPIO16_FAN_PWM_A_SPU



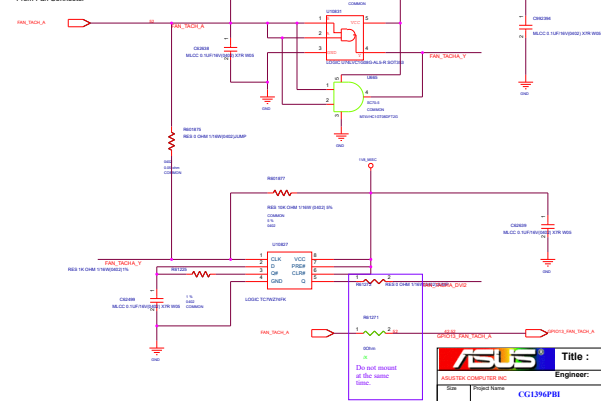
Replace FAN PWM BUFF INPUT

Go to GPU GPIO13

Put TURBO_SW symbol onto PCB bottom side.
Put ON and OFF text righty on the each side of SW symbol.



From Fan Connector



		Title : TURBO_FAN					
		Engineer: Water					
Size	Project Name	CG1396PBH					
Date	Versioning	Rev 05 2023	<table border="1"> <tr> <td>Drawn</td> <td>EC</td> <td>CF</td> <td>EC</td> </tr> </table>	Drawn	EC	CF	EC
Drawn	EC	CF	EC				