


SYNC MASTER=J85 MLB B		SYNC DATE=04/02/2013	
PAGE TITLE			
BLOCK DIAGRAM: SYSTEM			
 Apple Inc.		DRAWING NUMBER	051-0886
		SIZE	D
		REVISION	A.0.0
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87654321

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

BOM OPTIONS
COMMON
ALTERNATE
16GB_PROD
32GB_PROD
64GB_PROD
128GB_PROD
DEVELOPMENT_JTAG_TAP
JTAG_DAP
MLB (WDOG TO PMU)

WIFI BOM OPTIONS
ANDGATE_TI
FERRITE_TV
FERRITE_IDK

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0207	1	H6P + 1GB ELPIDA	U0652	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0208	339S0207		U0652	HYNIX DDR

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0656	1	1C, PMU, ANYA, D2089A1, OTPXX, FCCSP342	U8100	CRITICAL	

FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0921	1	TOS, 19NM, PPN1.5, C, DDP, 16GB	U1400	16GB
335S0922	1	TOS, 19NM, PPN1.5, C, QDP, 32GB	U1400	32GB
335S0923	1	TOS, 19NM, PPN1.5, C, ODP, 64GB	U1400	64GB
335S0929	1	TOS, 19NM, PPN1.5, C, 12DP, 64GB	U1400	96GB
335S0924	1	TOS, 19NM, PPN1.5, C, 16DP, 128GB	U1400	128GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0930	335S0921	16GB	U1400	HYNIX 20NM PPN1.5 16GB
335S0931	335S0922	32GB	U1400	HYNIX 20NM PPN1.5 32GB
335S0932	335S0923	64GB	U1400	HYNIX 20NM PPN1.5 64GB

U2200

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S4272	1	1C, SIGMA142IV, PMU, SW, GREENFET3, AA, TQFN	U2200	

NOTE: FOLLOWING J72, U2200 USES 353S3672 FOOTPRINT (353S4272 HAS SMALLER PADS DUE TO NEW DFM RULES)

4.3UF CAP

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657		C1009, C1015...	RDAR #13988471

WIFI

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0223	339S0213		U5800	

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-6207	1	FENCE, TALL, MLB, X221	PD_FENCE_MLB	CRITICAL	
806-7613	1	FENCE, RADIO, MLB, C BRD, X221	PD_CAN_RADIO	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	EEEE FOR 639-5393 (X200C1 GOOD)	FNJD	CRITICAL	EEEE_X200C_GOOD
825-7639	1	EEEE FOR 639-5394 (X200C1 BETTER)	FNJ5	CRITICAL	EEEE_X200C_BETTER
825-7639	1	EEEE FOR 639-5385 (X200C1 BEST)	FNJ9	CRITICAL	EEEE_X200C_BEST
825-7639	1	EEEE FOR 639-5386 (X200C1 BEST+)	FNJH	CRITICAL	EEEE_X200C_BEST+
825-7639	1	EEEE FOR 639-5387 (X200C1 ULTIMATE)	FNJ6	CRITICAL	EEEE_X200C_ULTIMATE
825-7639	1	EEEE FOR 639-5388 (X200C1 GOOD IVS)	FNJ8	CRITICAL	EEEE_X200C_GOOD_IVS
825-7639	1	EEEE FOR 639-5389 (X200C1 BETTER IVS)	FNJF	CRITICAL	EEEE_X200C_BETTER_IVS
825-7639	1	EEEE FOR 639-5390 (X200C1 BEST IVS)	FNJC	CRITICAL	EEEE_X200C_BEST_IVS
825-7639	1	EEEE FOR 639-5391 (X200C1 BEST+ IVS)	FNJ7	CRITICAL	EEEE_X200C_BEST+_IVS
825-7639	1	EEEE FOR 639-5392 (X200C1 ULTIMATE IVS)	FNJG	CRITICAL	EEEE_X200C_ULTIMATE_IVS

GYRO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1192	1	GYRO, ST MICRO	U2720	CRITICAL	GYRO_STMICRO
338S1218	1	GYRO, INVENSENSE	U2720	CRITICAL	GYRO_INVENSENSE
132S0391	1	CAP 0.01UF 25V 0201	C2726	CRITICAL	GYRO_STMICRO
132S0288	1	CAP 0.1UF 16V 0201	C2726	CRITICAL	GYRO_INVENSENSE

338S1158 OLD GYRO - ST MICRO
OLDER INVENSENSE P/N 338S1135
OLD INVENSENSE P/N 338S1200 (3/22/13)

ACCEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1163	1	1C, ACCEL, 3-AXIS, DIG, BMA282, LGA14	U2700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

338S1233 ST MICRO - DISQUAL'ED
338S1114 OLD ACCEL - ST MICRO
338S1191 OLD ACCEL - ST MICRO

SYNC MASTER=J72 MLB C SYNC DATE=11/26/2012

BOM TABLES

Apple Inc.

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DRAWING NUMBER
051-0886

REVISION
A.0.0

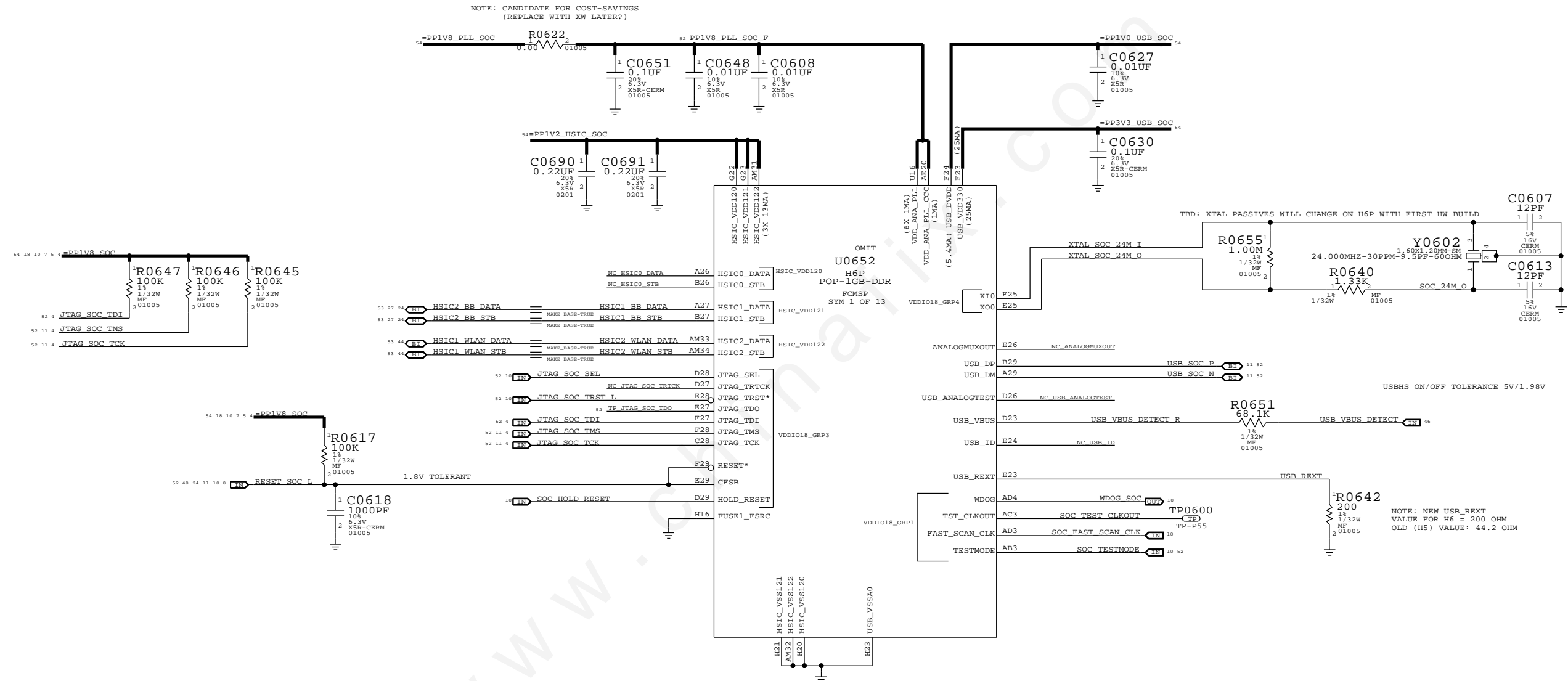
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PAGE
4 OF 121

SHEET
3 OF 54

SIZE
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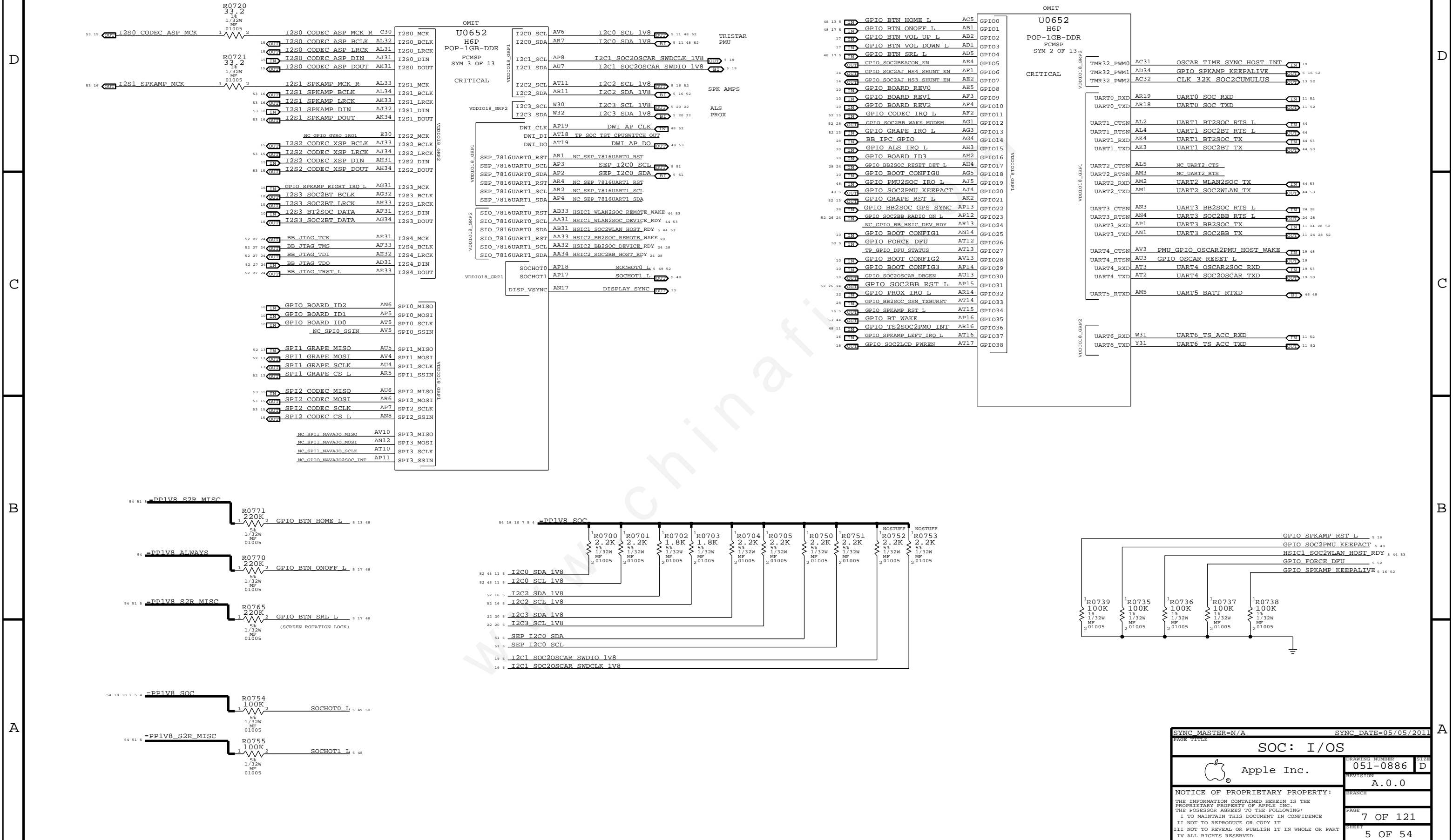
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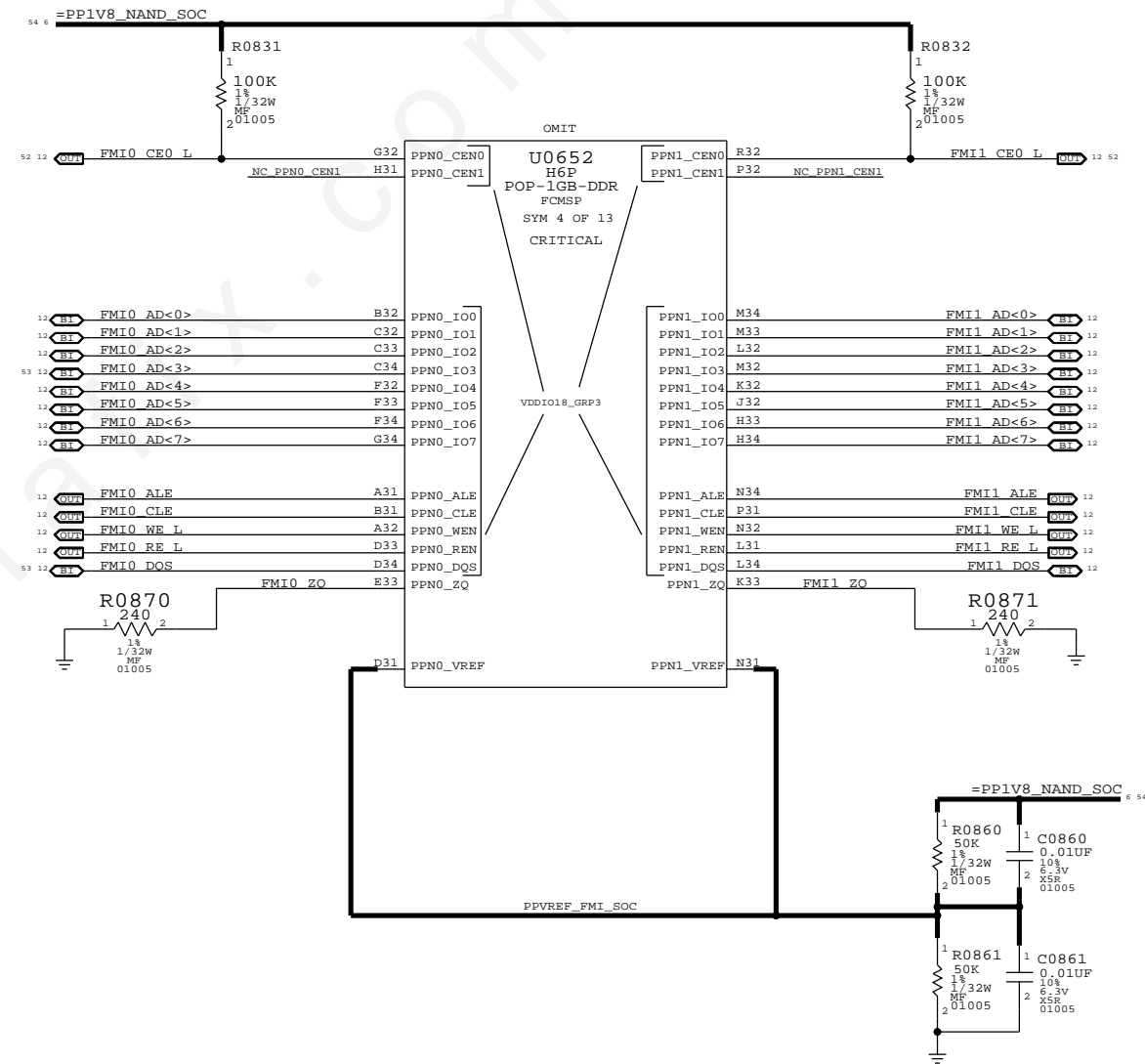
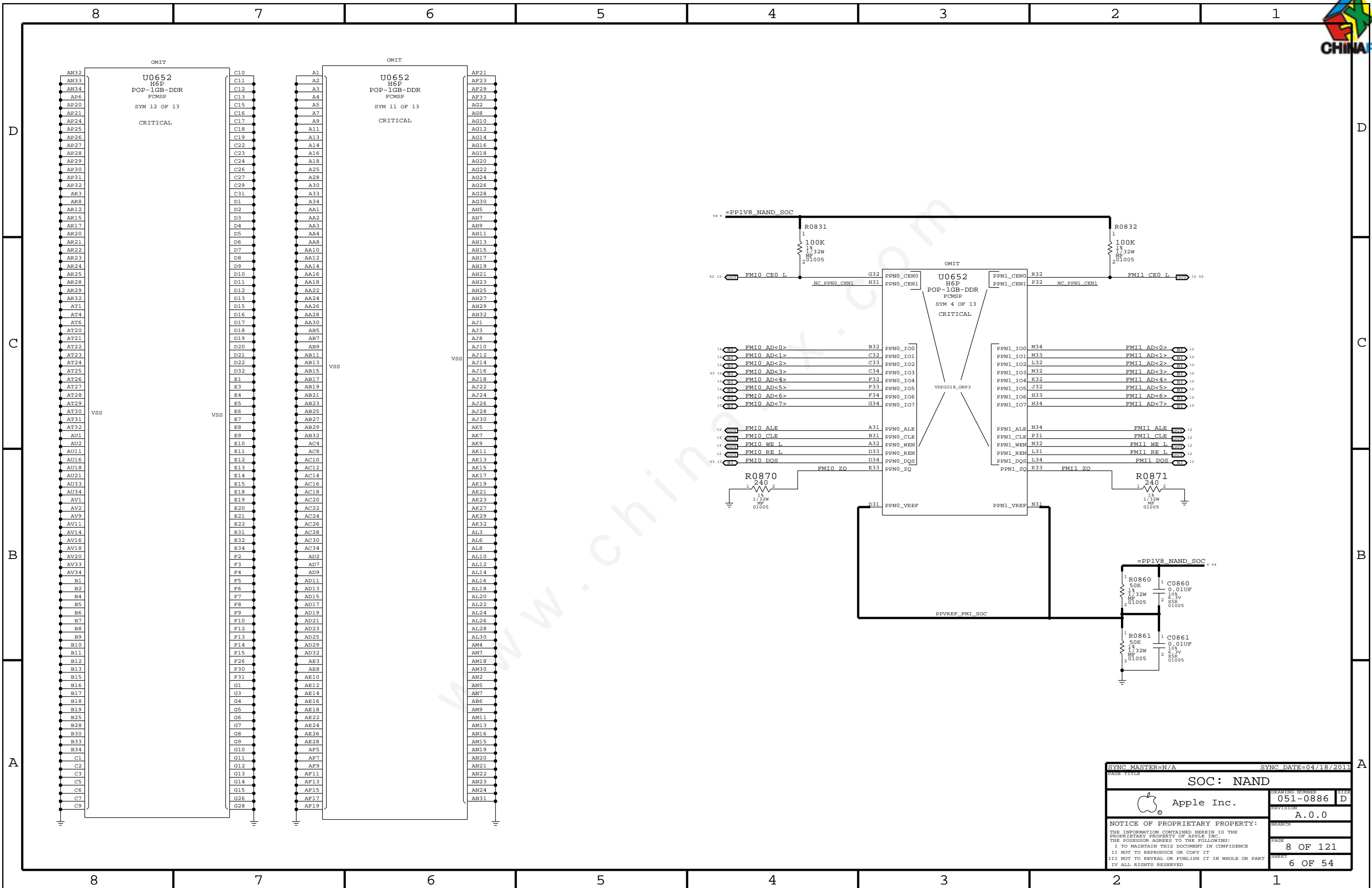



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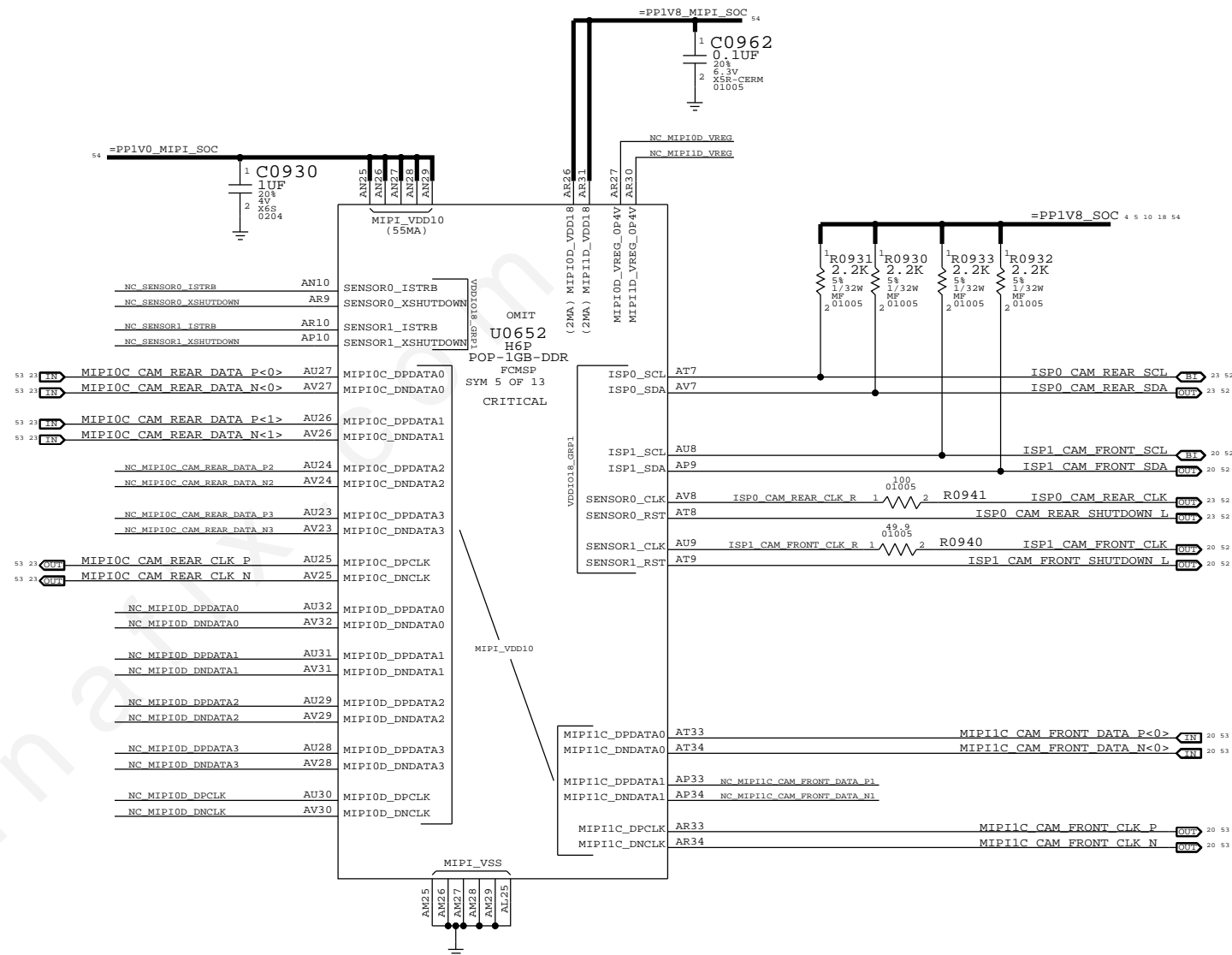
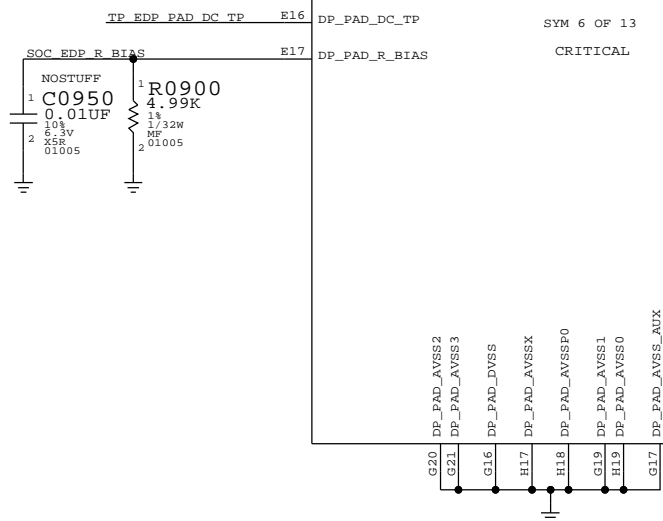
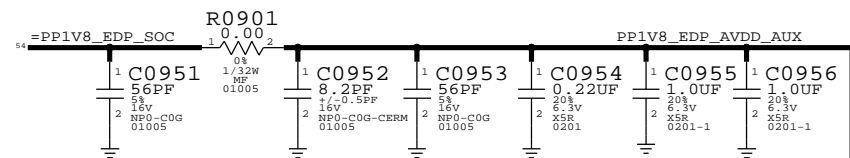
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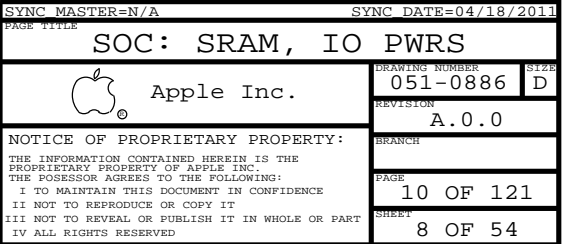


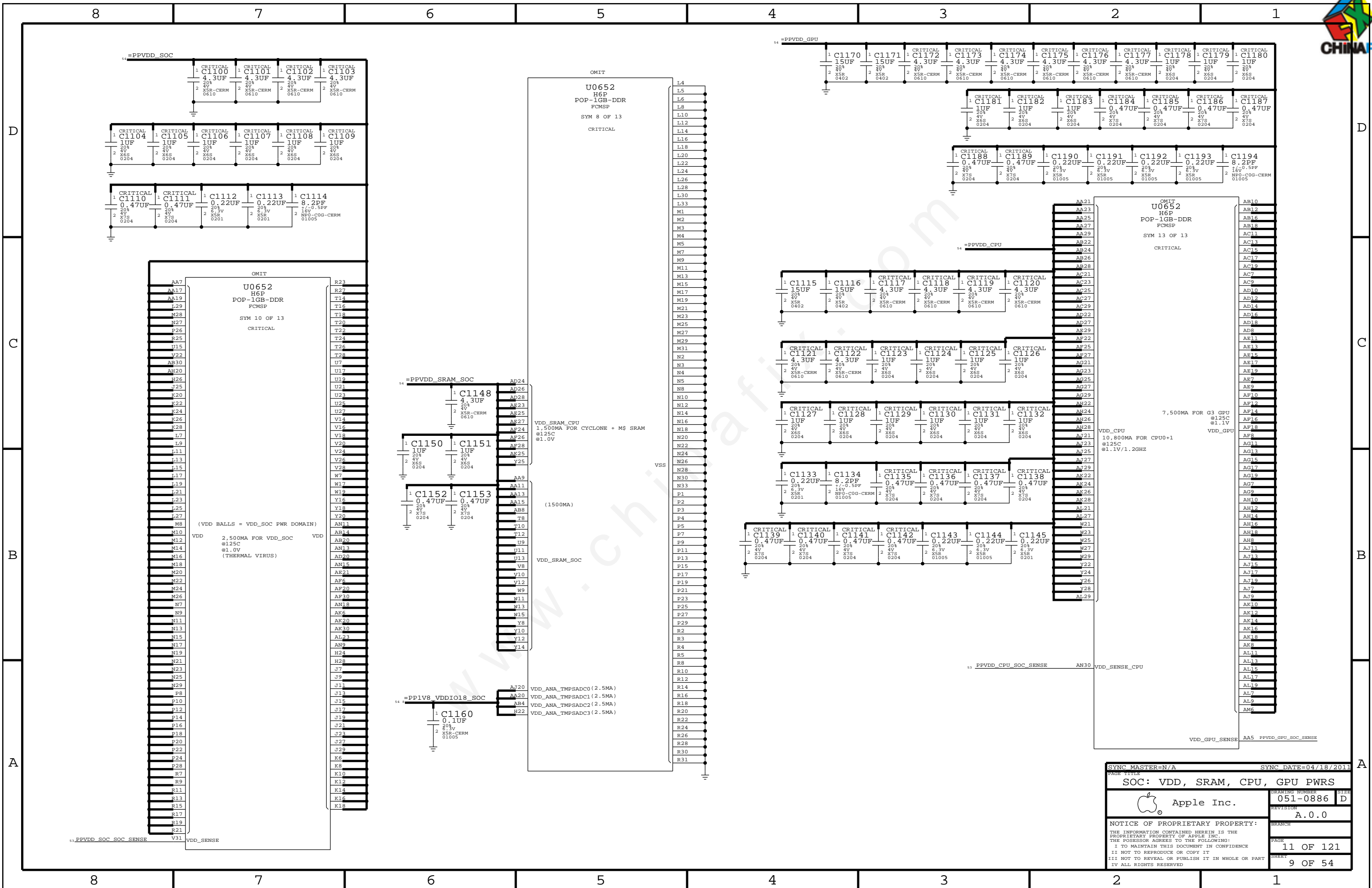


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		SHEET 6 OF 54	

DISPLAYPORT

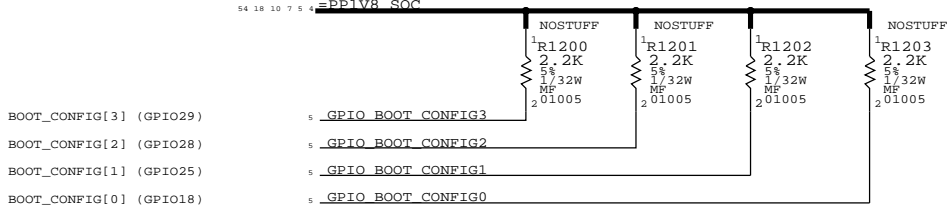






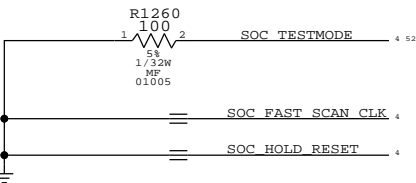
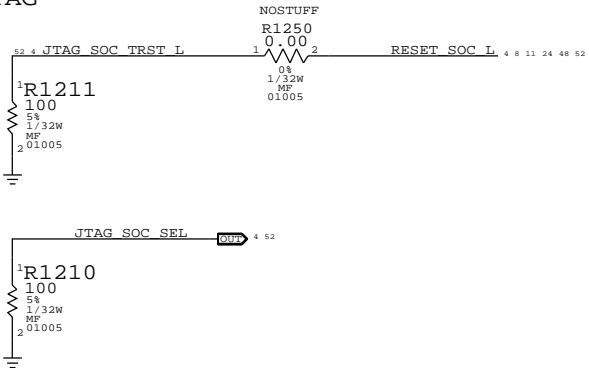


BOOT CONFIG ID



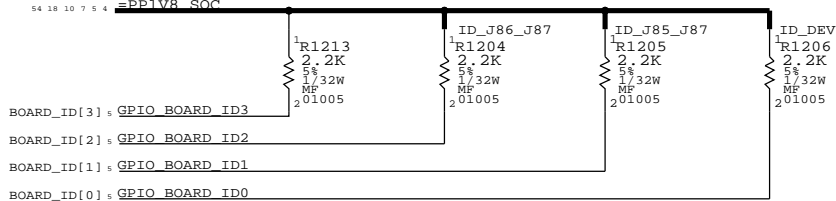
BOOT_CONFIG[3-0]		S/W READ FLOW
0000	SPI0	1. SET GPIO AS INPUT
0001	SPI0 TEST MODE	2. DISABLE PU AND ENABLE PD
0010	NAND	3. READ
0011	NAND TEST MODE	

JTAG



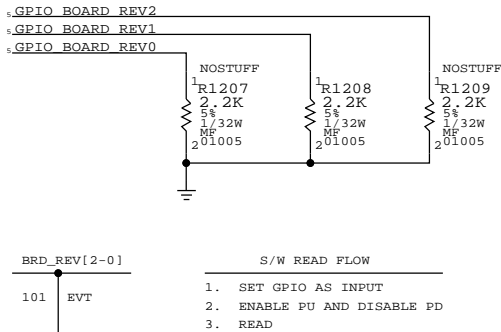
I2S3 SOC2BT BCLK	I2S4 SOC2BT BCLK	44
I2S3 SOC2BT LRCK	I2S4 SOC2BT LRCK	44
I2S3 BT2SOC DATA	I2S4 BT2SOC DATA	44
I2S3 SOC2BT DATA	I2S4 SOC2BT DATA	44
WDOG_SOC	WDOG_SOC2PMU RESET_IN	48

BOARD ID

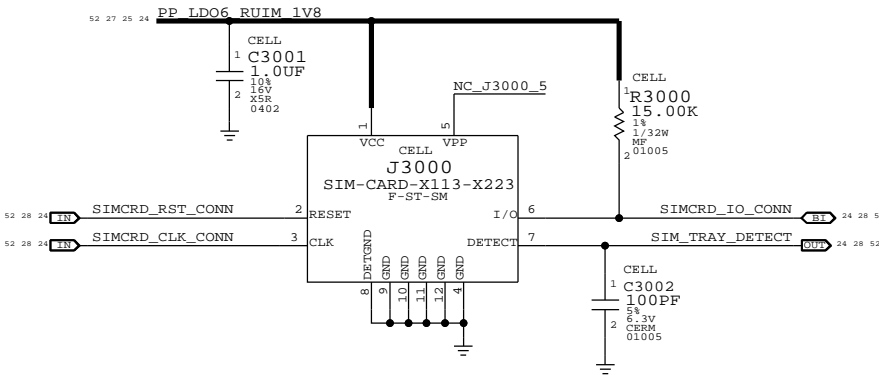


ID[3-0]	SYSTEM	S/W READ FLOW
1010	J85 AP	1. SET GPIO AS INPUT
1011	J85 DEV	2. DISABLE PU AND ENABLE PD
1100	J86 AP	3. READ
1101	J86 DEV	
1110	J87 AP	
1111	J87 DEV	


BOARD REVISION




SIM CARD

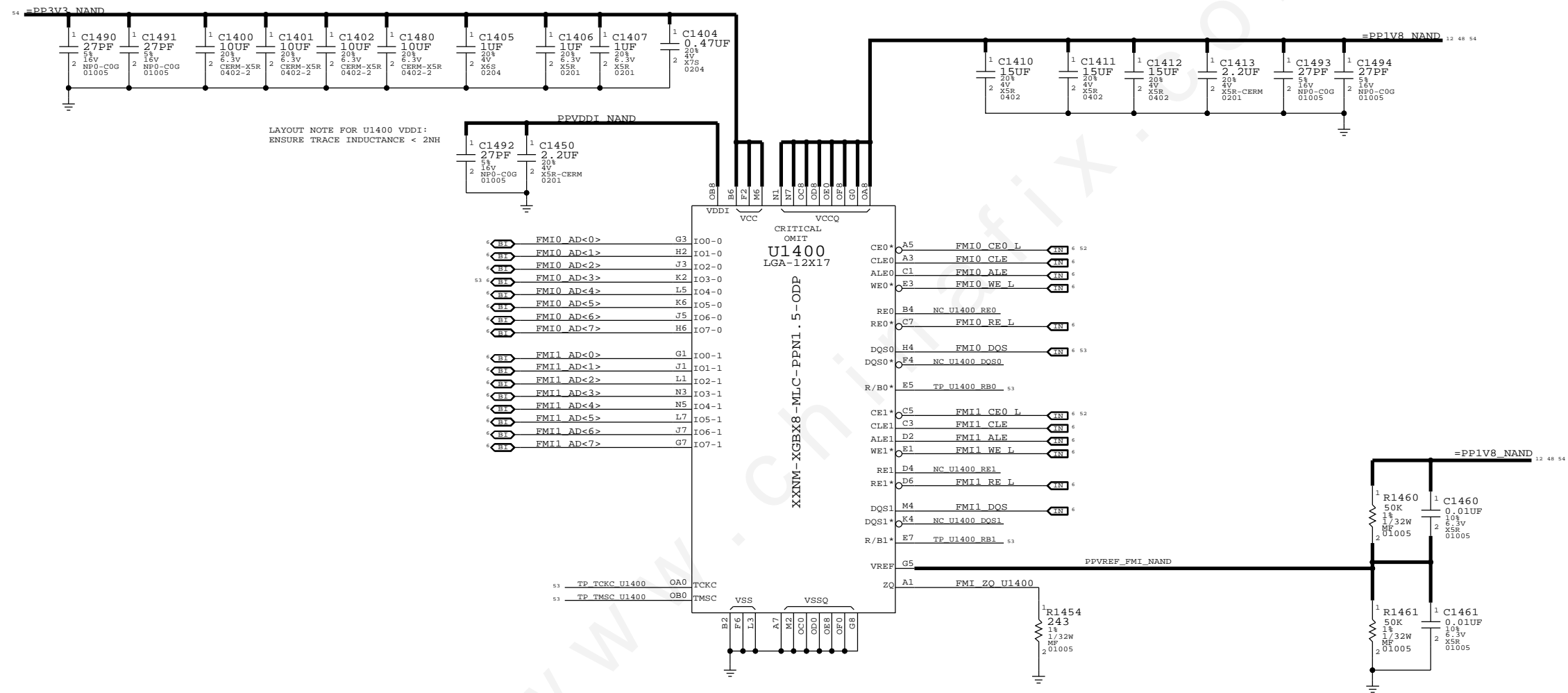


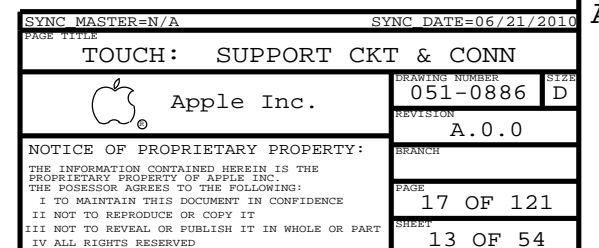
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SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

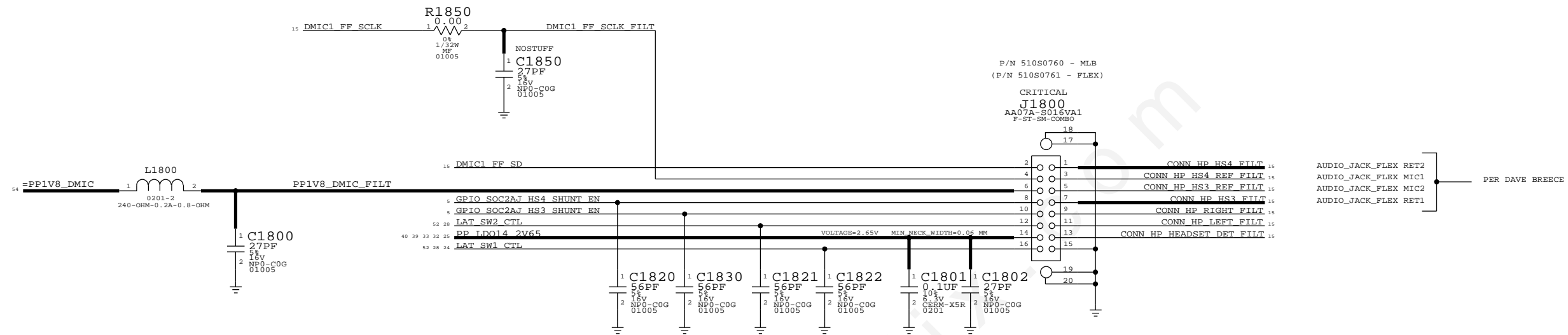
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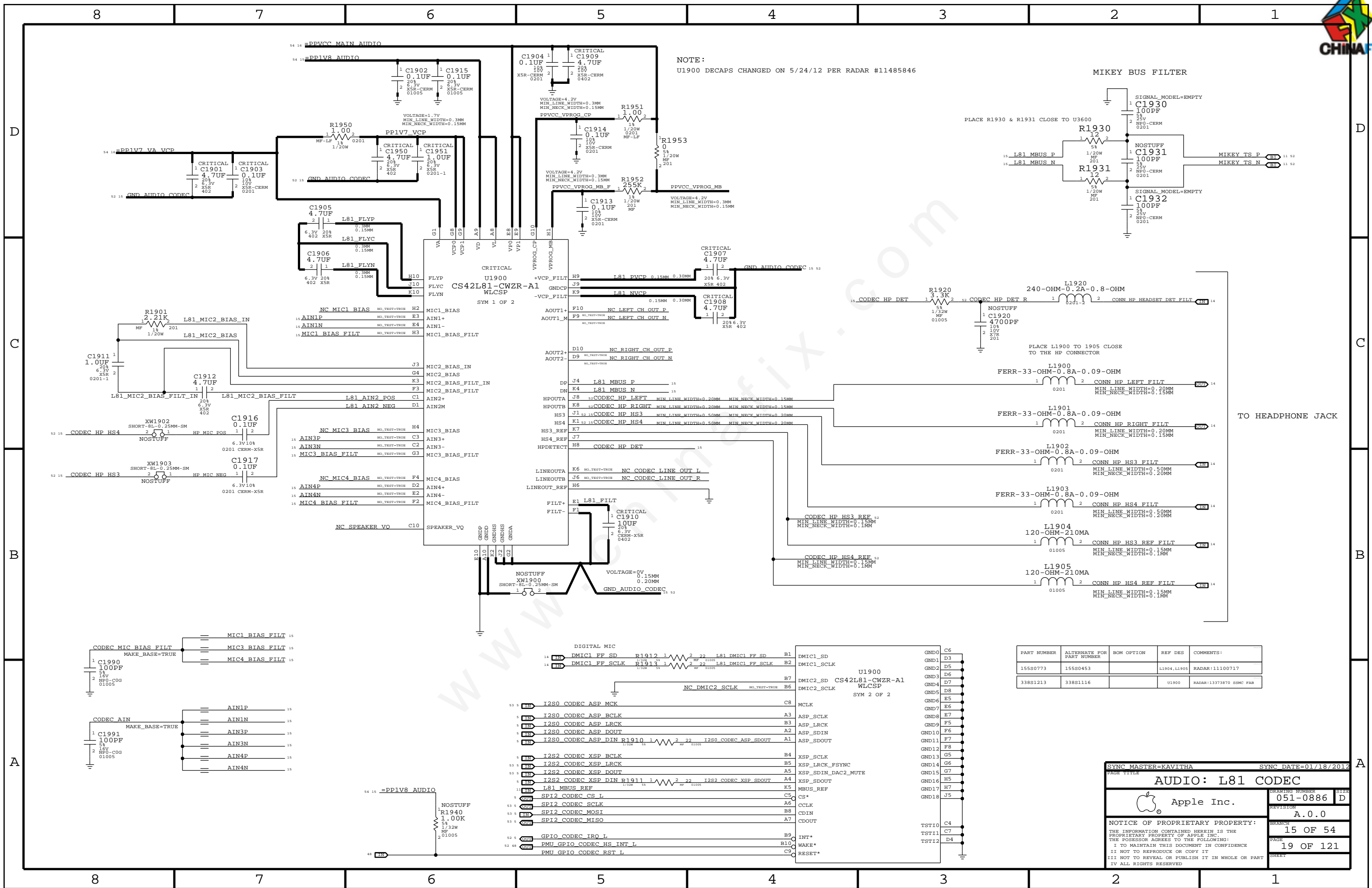
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		SHEET 11 OF 54	








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	14 OF 54		
	PAGE		
18 OF 121			
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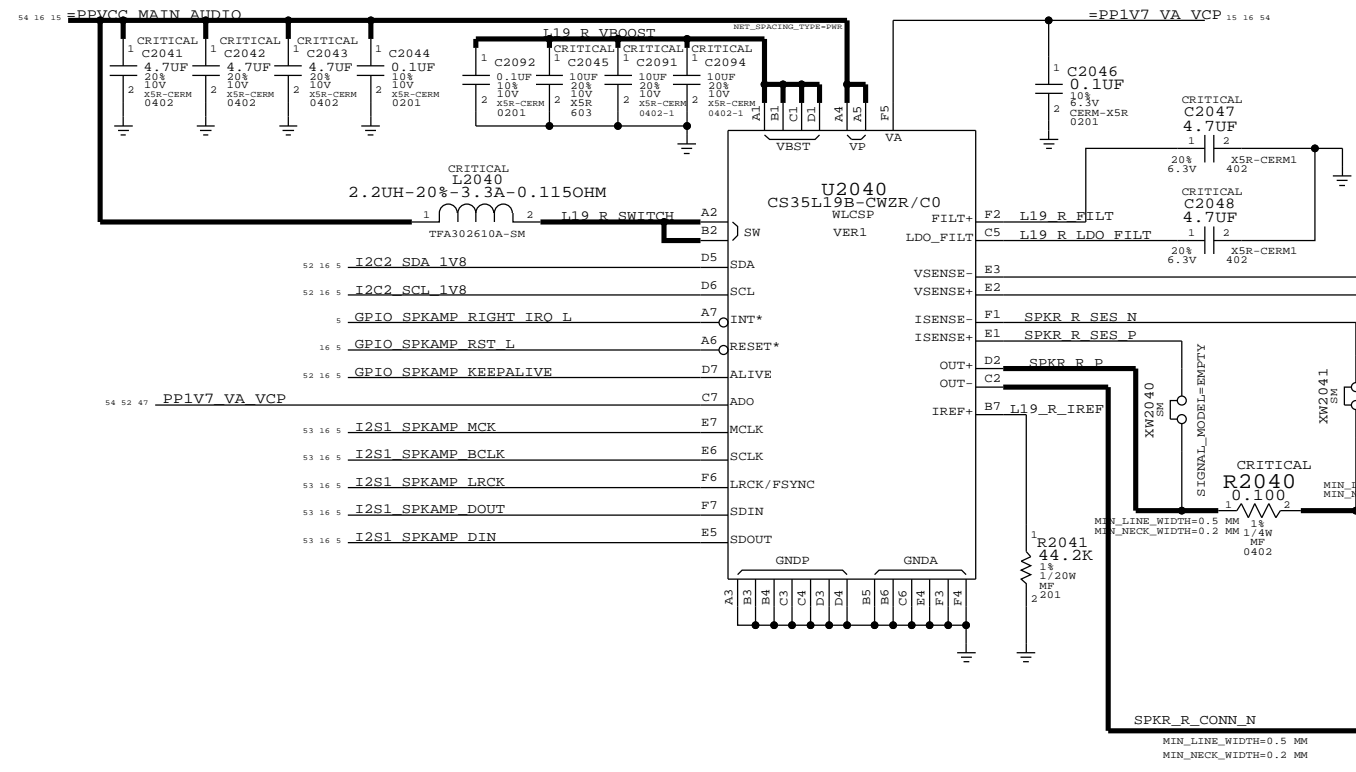


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RIGHT SPEAKER AMP

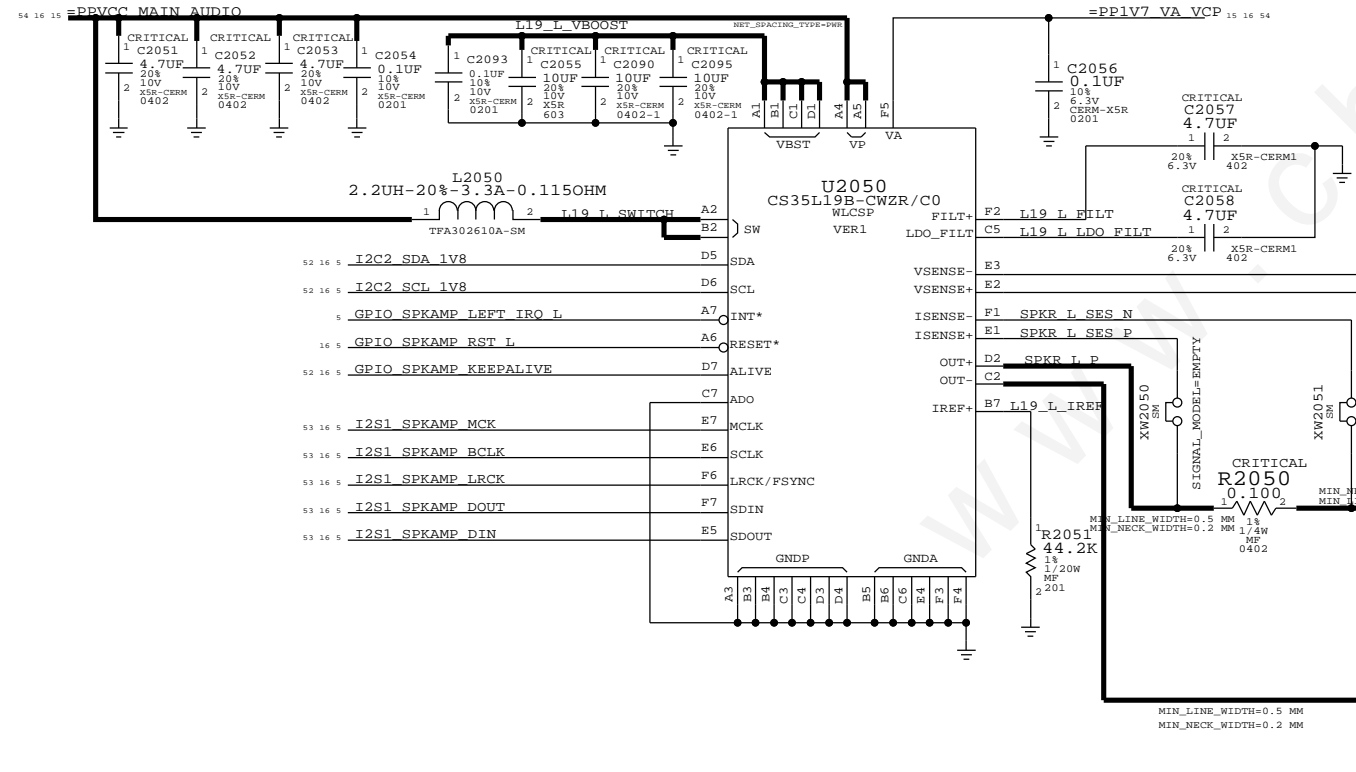
I2C ADDRESS: 1000001X



SPEAKER CONNECTOR


LEFT SPEAKER AMP

I2C ADDRESS: 1000000X




UPDATED: DEC 13

1. ALL THE EMI/DESENSE FILTER COMPONENTS HAVE BEEN REMOVED BASED ON PERFORMANCE ON J65
2. THE CURRENT VERSION OF L19 IS B0 AND WILL CHANGE TO C0 BY MARCH 2013. C0 FIXES PROCESS ISSUES.

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		SHEET	16 OF 34



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		SHEET 17 OF 54	



C

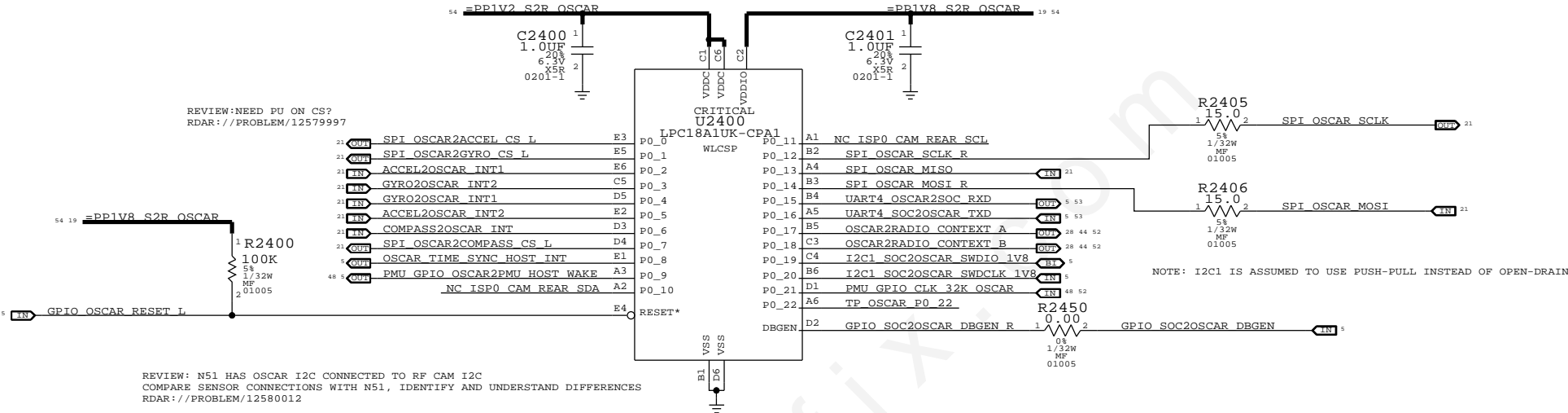
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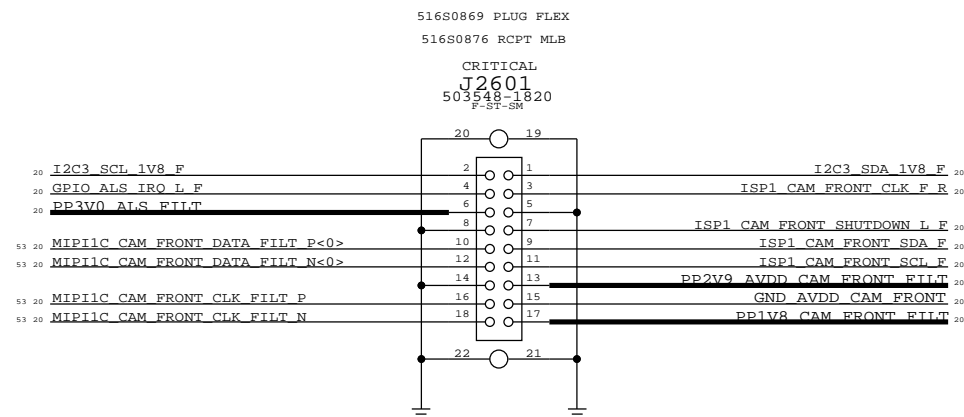
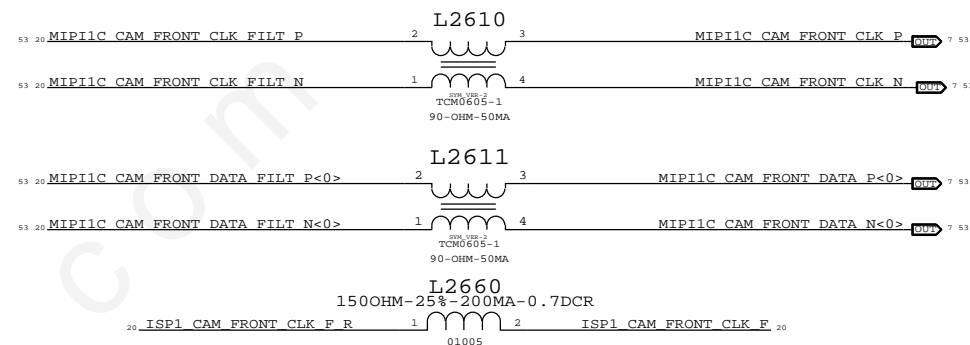
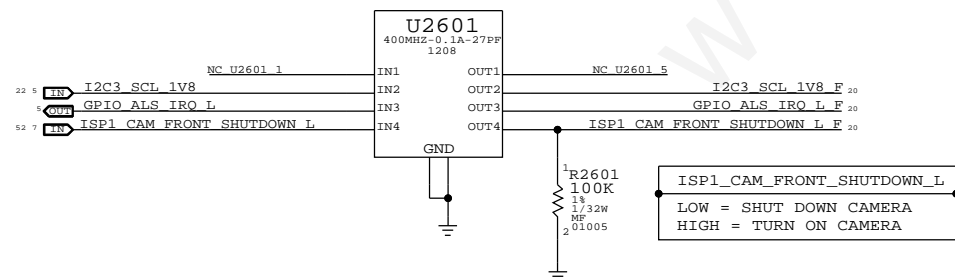
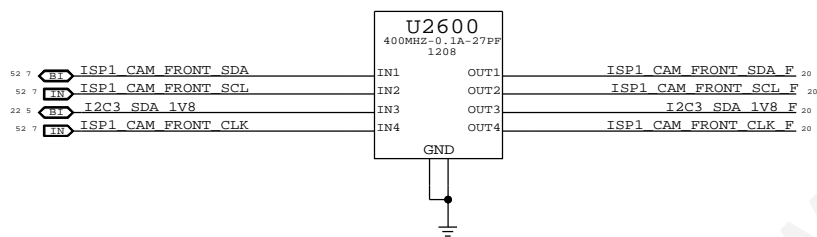
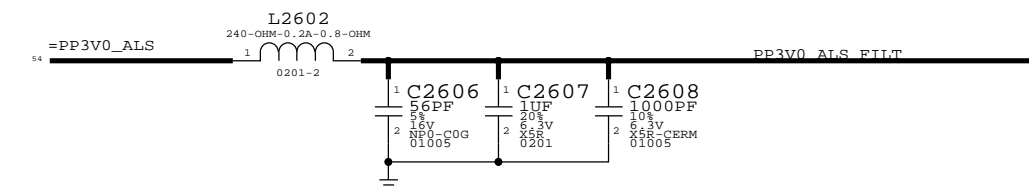
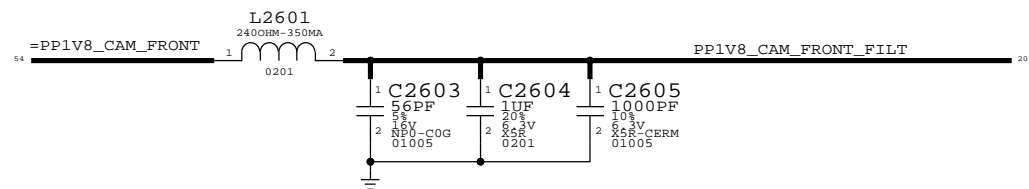
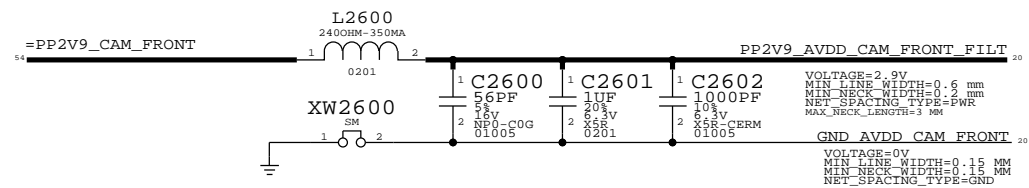
OSCAR

APN 337S4416

OSCAR VDDIO = 1.8V HIBERNATE (NEED TO WAKE HOST)
OSCAR CORE = 1.2V HIBERNATE (NEED TO RUN IN S2R)



VGA FRONT CAMERA CONNECTOR



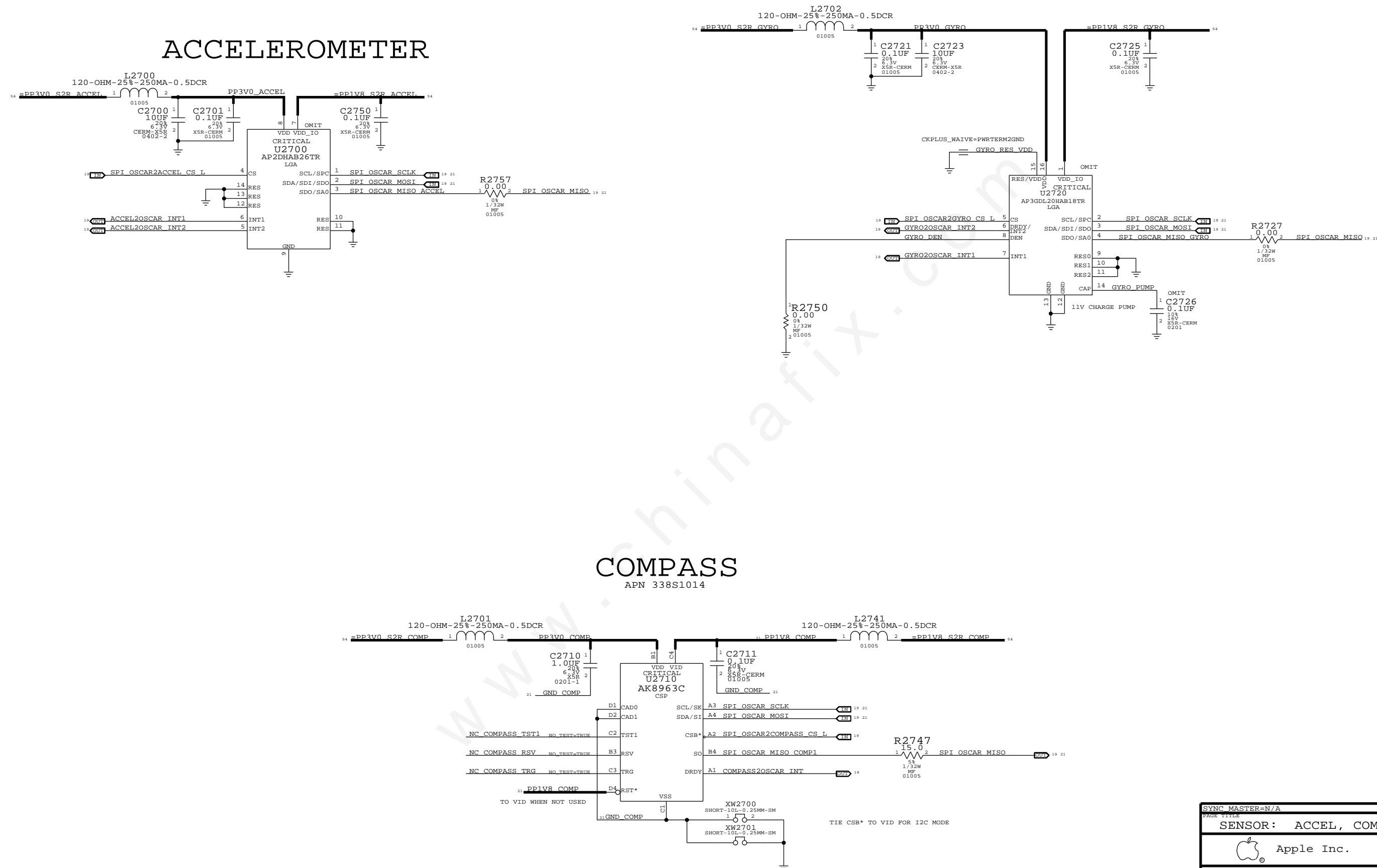
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GYRO

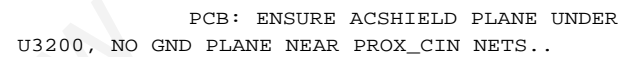
ACCELEROMETER


COMPASS

APN 338S1014



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NOTICE OF PROPRIETARY PROPERTY:		27 OF 121	
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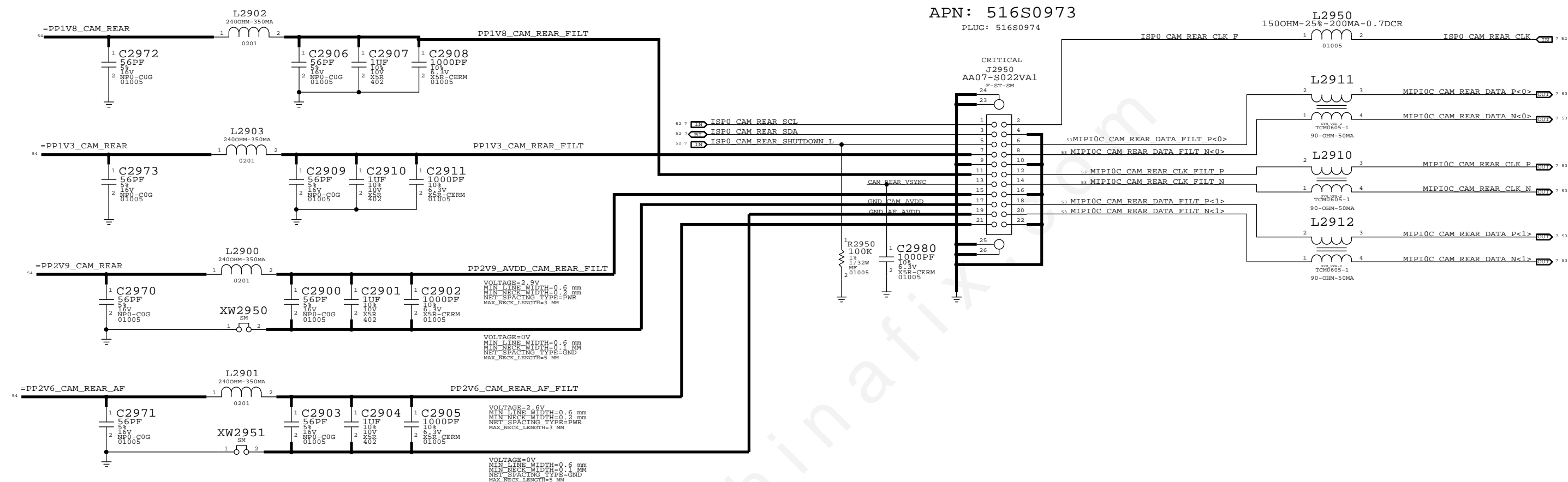


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REAR CAMERA CONNECTOR

APN: 516S0973

PLUG: 516S0974



CAMERA: REAR CONN & FILTERS		DRAWING NUMBER		SIZE	
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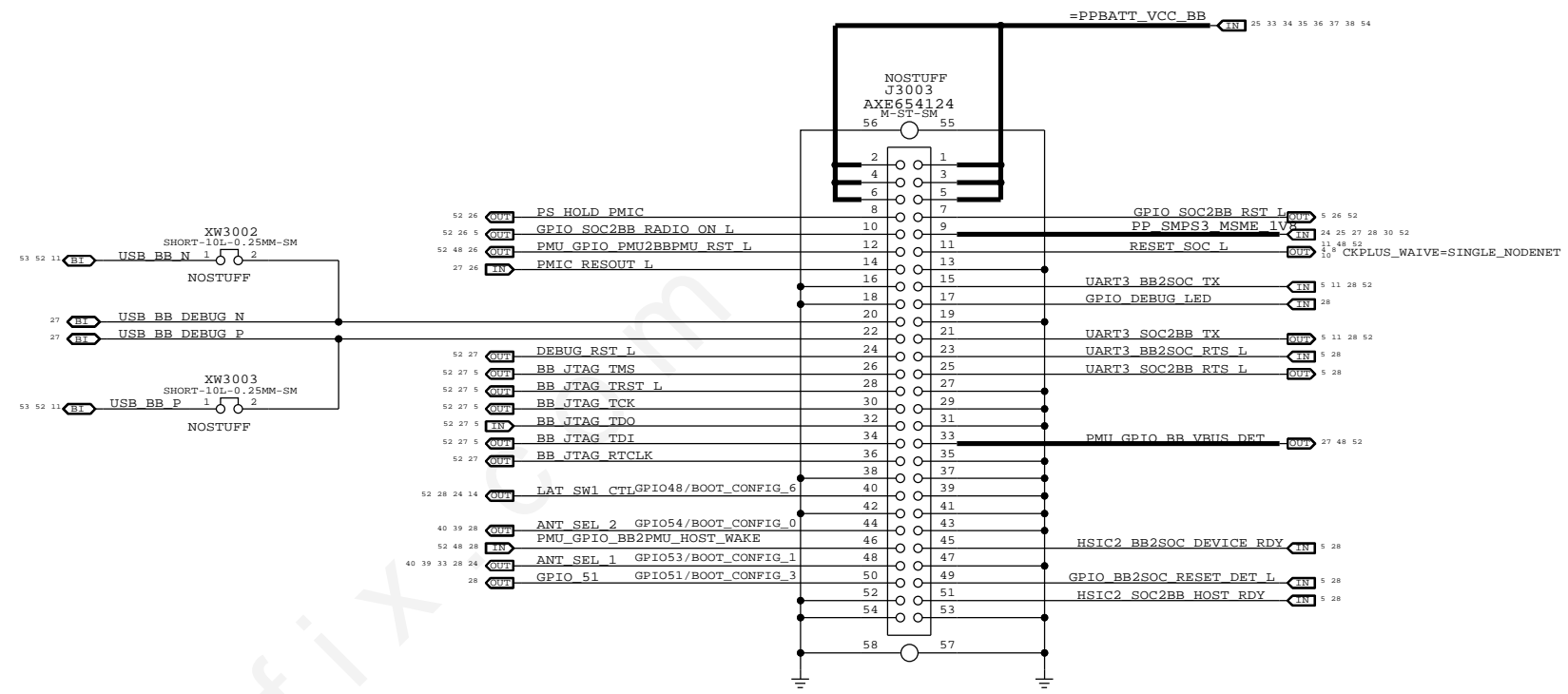


AP INTERFACE & DEBUG CONNECTORS

PROBE POINTS

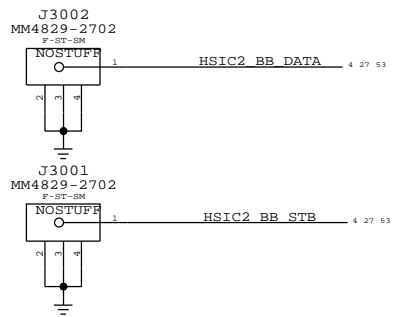
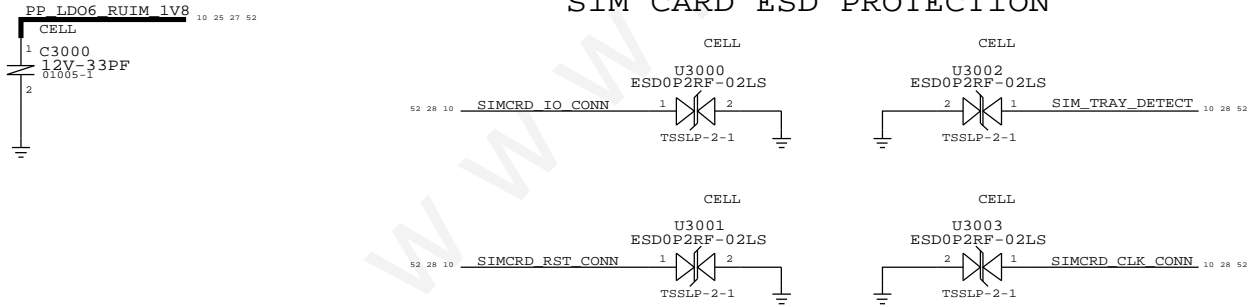
- PP3000
P4MM
1 BB_ERROR_FLAG 28
- PP3001
P4MM
1 SLEEP_CLK_32K 26 27
- PP3002
P4MM
1 PMIC_SSBI 26 27
- PP3003
P4MM
1 19P2M_MDM 26 27
- PP3008
P4MM
1 WTR_SSBI_TX_GPS 28 29
- PP3009
P4MM
1 WTR_SSBI_PRX_DRX 28 29
- PP3010
P4MM
1 WTR_RX_ON 28 29
- PP3011
P4MM
1 WTR_RF_ON 28 29
- PP3012
P4MM
1 UART_WLAN2BB_LTE_COEX 28 44
- PP3013
P4MM
1 UART_BB2WLAN_LTE_COEX 28 44

DEBUG CONNECTOR



BOOT OPTIONS	BOOT_CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION							
		6	5	4	3	2	1	0	
BOOT_DEFAULT_OPTION	0x00	X	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0x01	X	1	0	0	0	0	0	1
BOOT_HSIC_OPTION	0x02	X	1	0	0	0	0	1	0
BOOT_USB_OPTION	0x03	X	1	0	0	0	0	1	1
ENABLE SAHARA PROTOCOL	0x08	X	1	0	0	1	0	X	X

SIM CARD ESD PROTECTION



CELL:AP INTERFACE & DEBUG CONNECTORS

Apple Inc.

051-0886

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PAGE

30 OF 121

SHEET

24 OF 54



PMU (1 OF 2)

D

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C

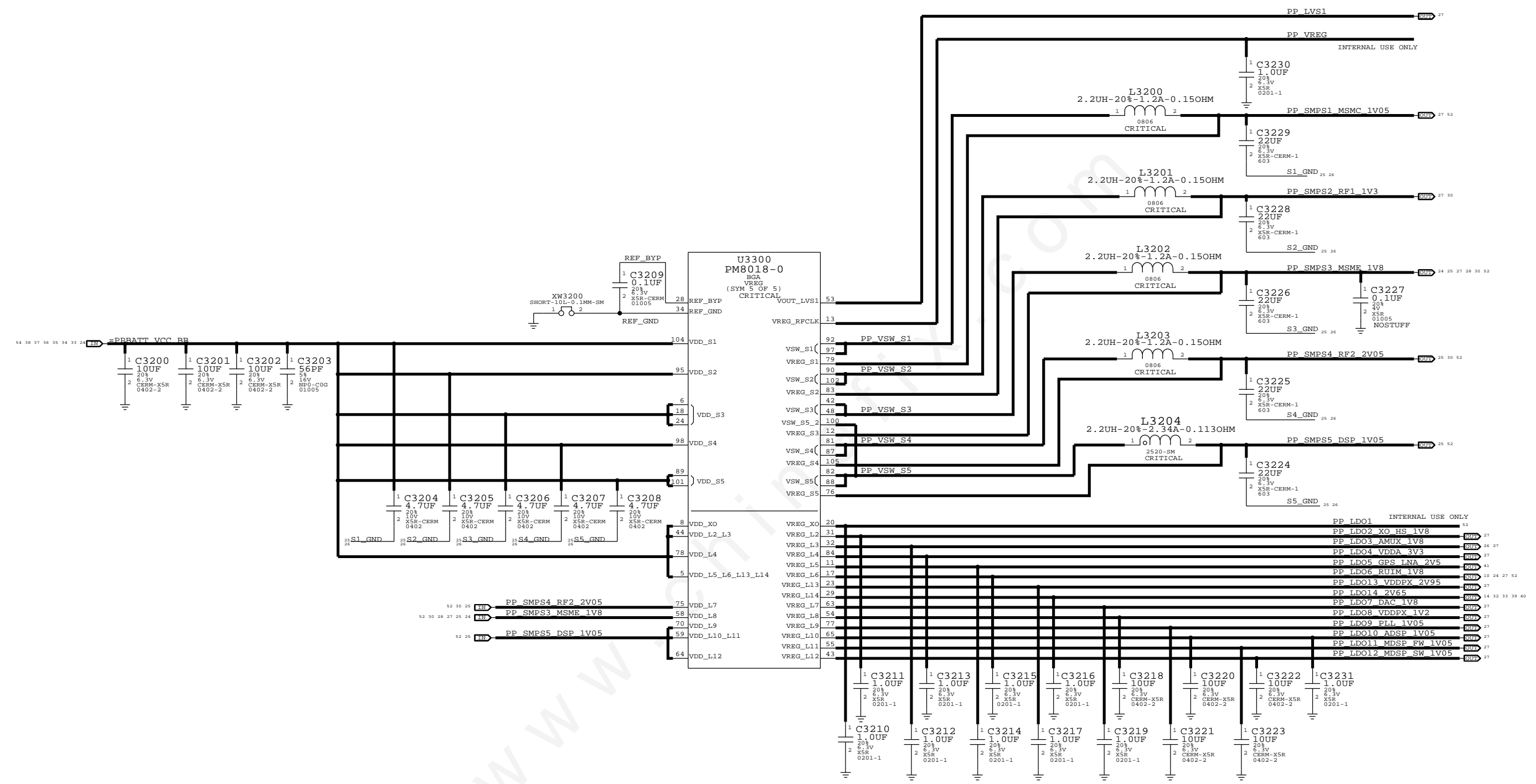
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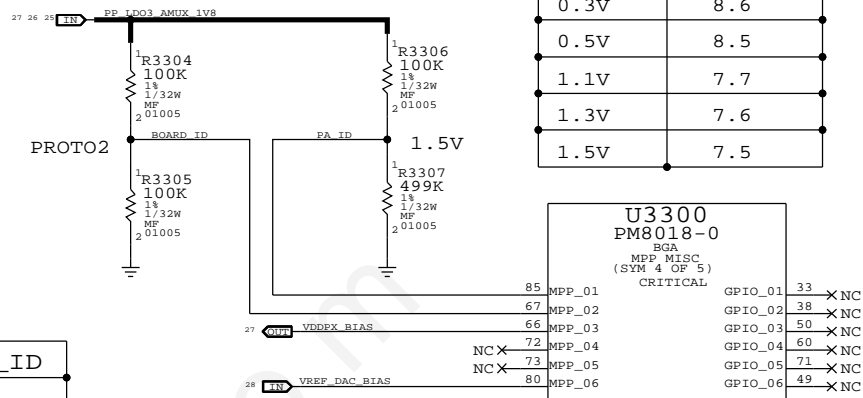
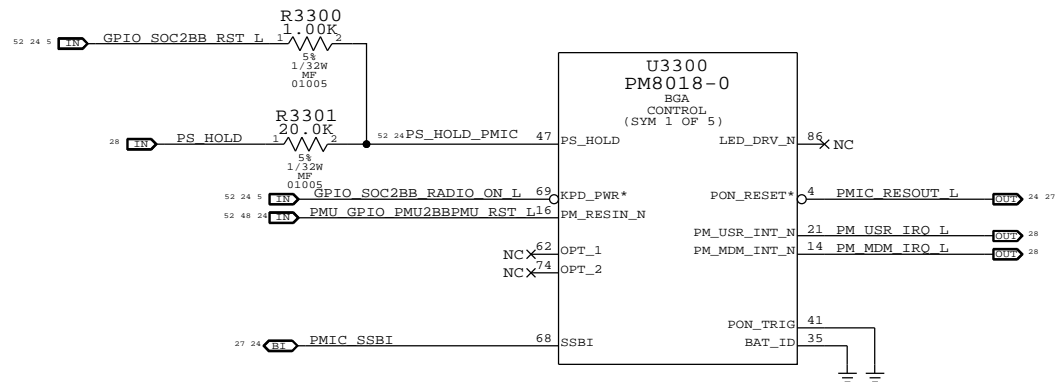


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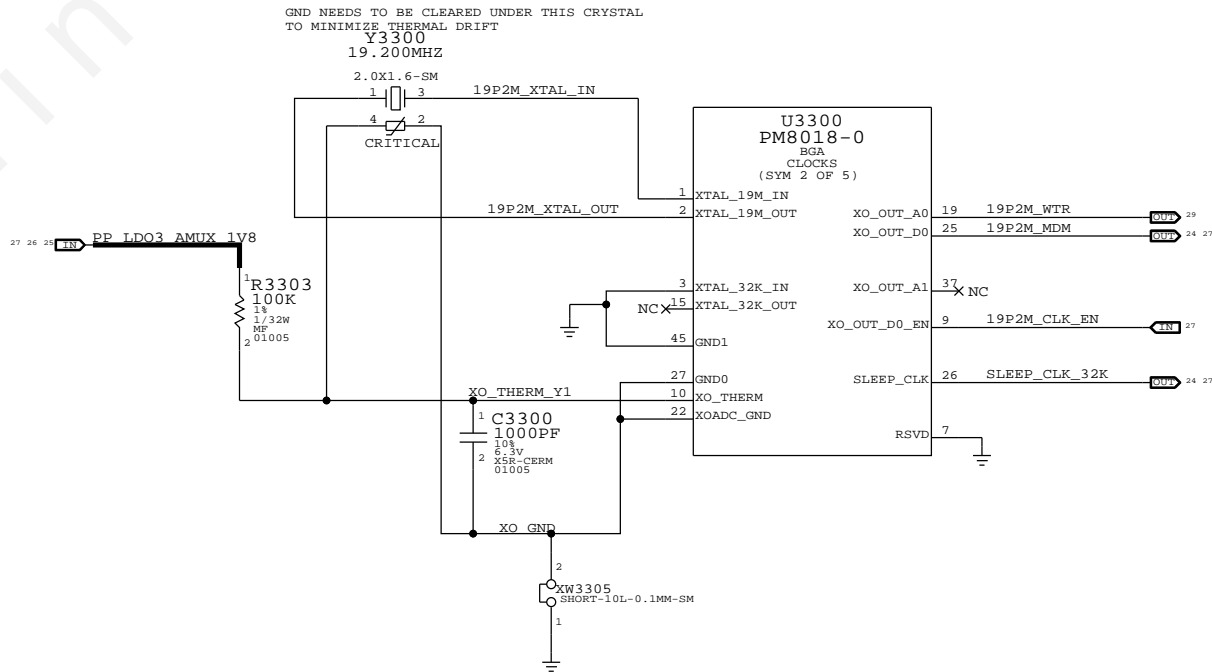
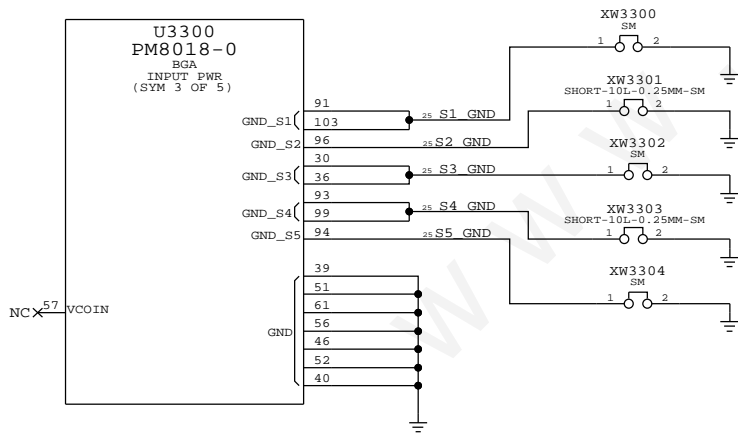
BOARD_ID	REVISION
0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT


BB GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX

PA_ID	MAV VER
0.1V	8.7
0.3V	8.6
0.5V	8.5
1.1V	7.7
1.3V	7.6
1.5V	7.5



AP SECTION NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.



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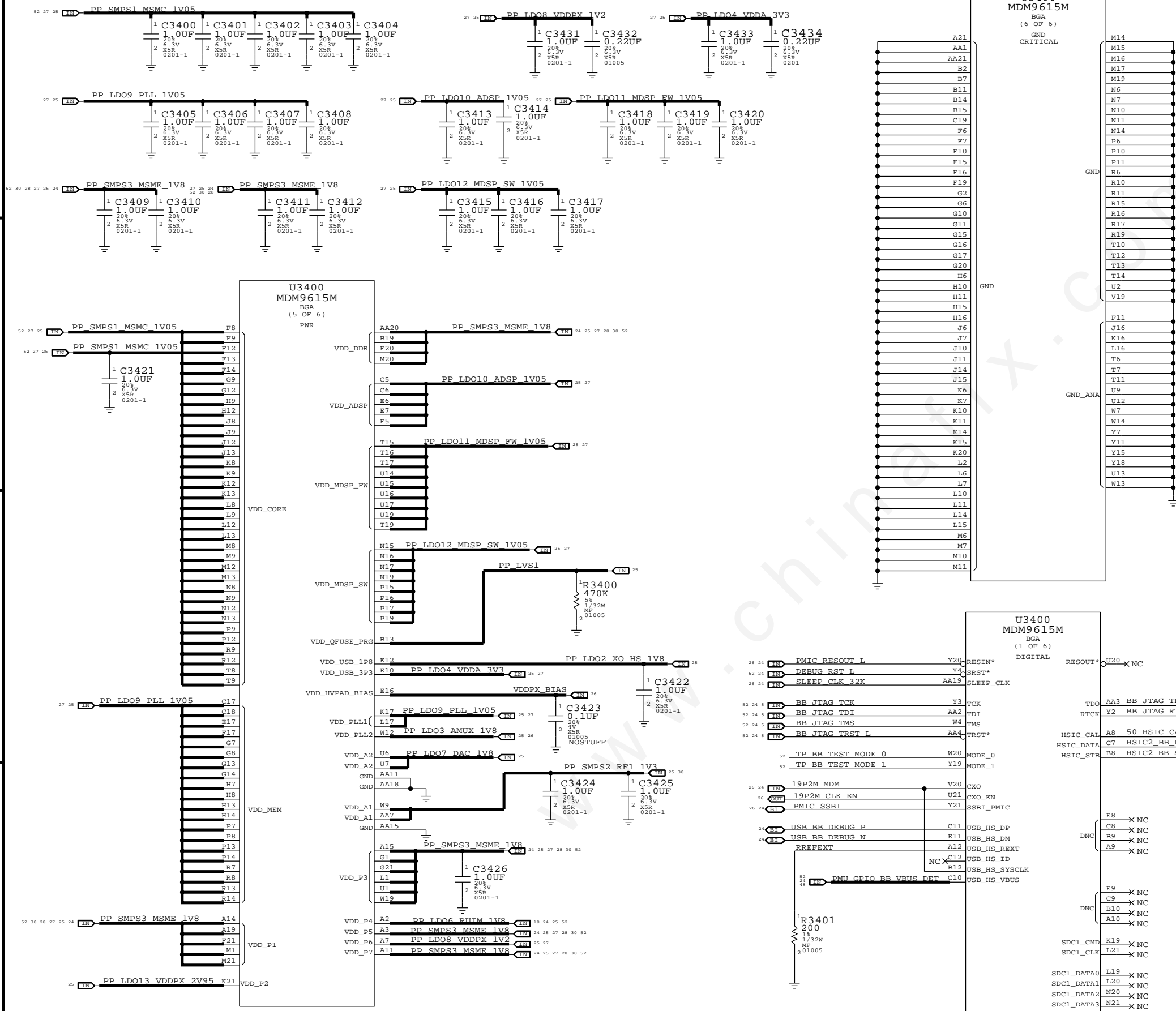
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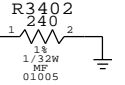
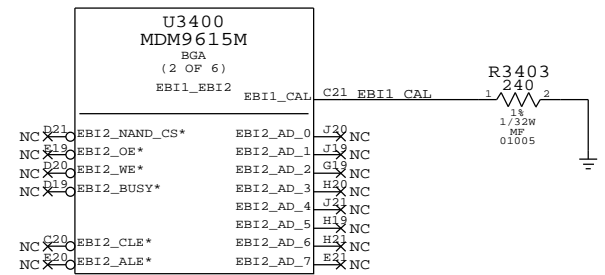
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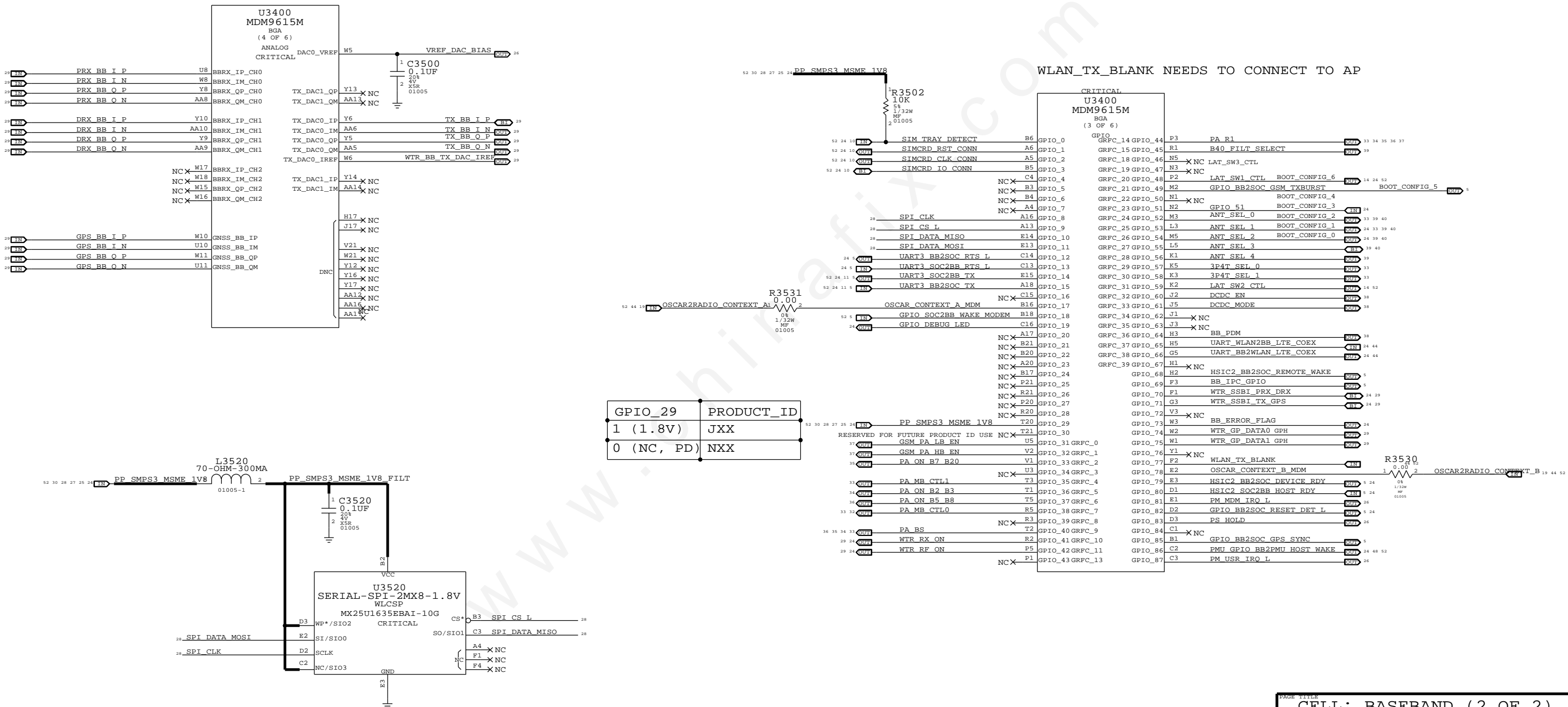


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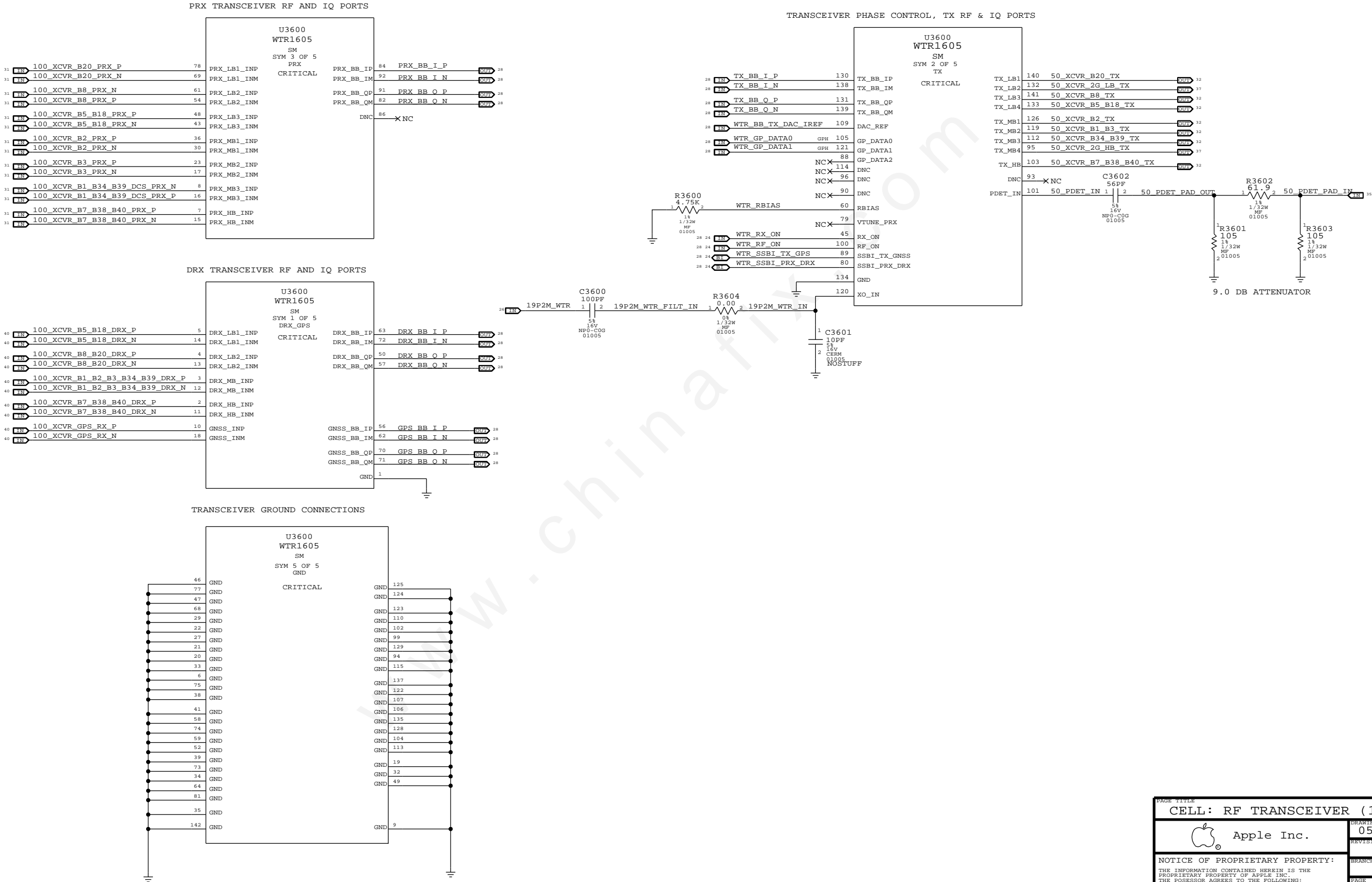
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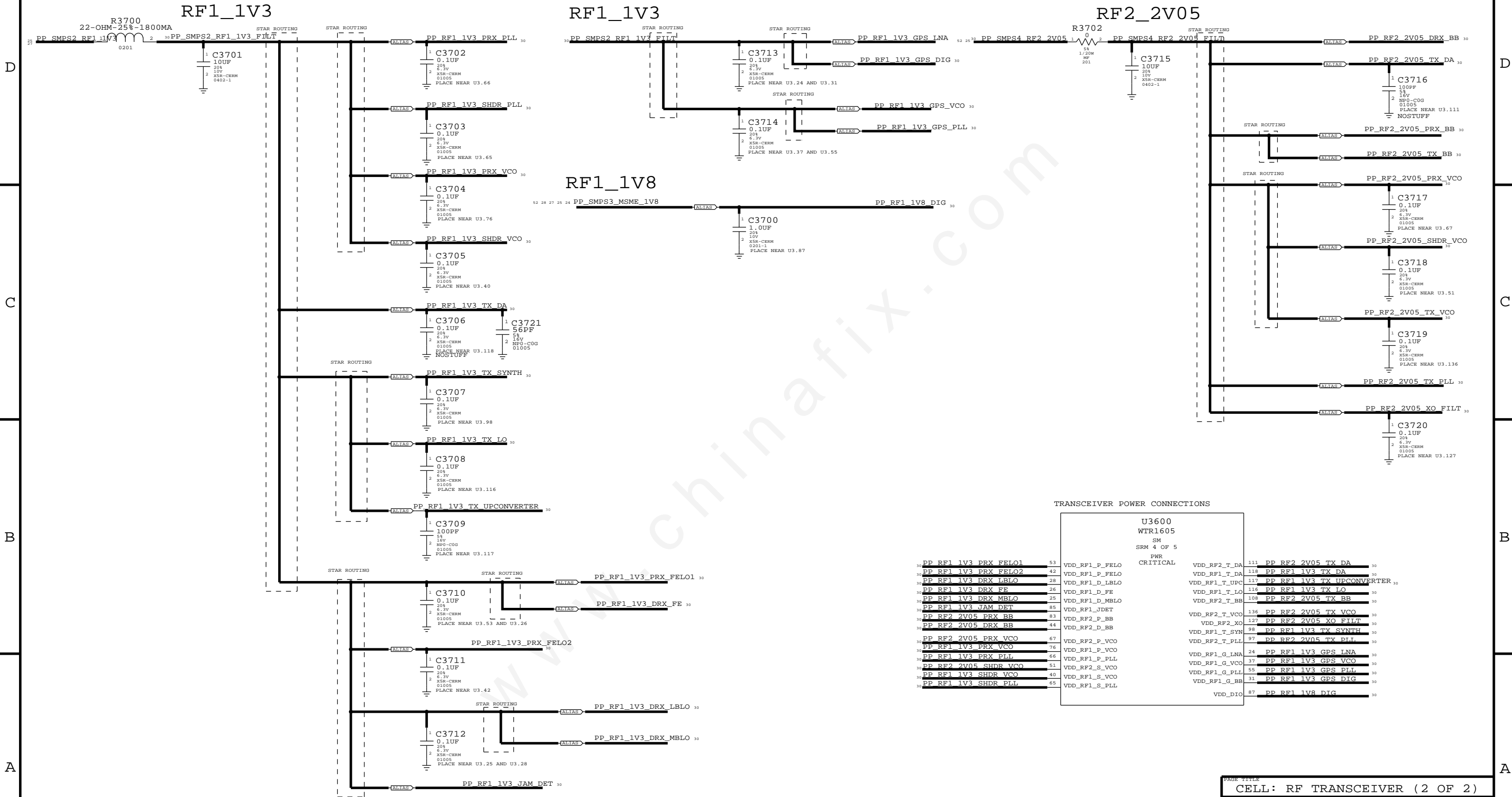


RF TRANSCEIVER (1 OF 2)





RF TRANSCEIVER (2 OF 2)

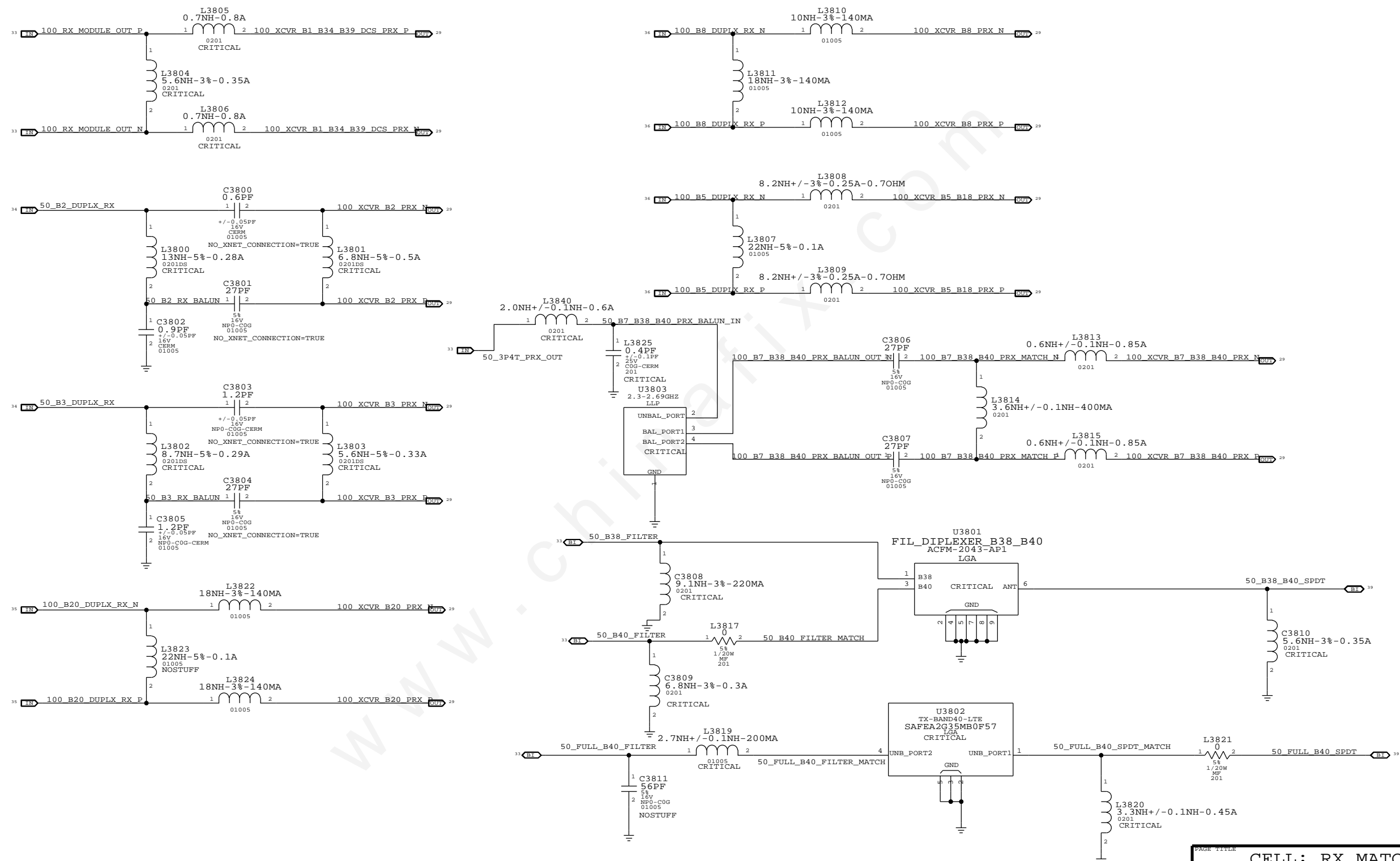



TRANSCEIVER POWER CONNECTIONS

U3600			WTR1605		
SM			SRM 4 OF 5		
PWR			CRITICAL		
PP RF1 1V3 PRX FELO1	53	VDD_RF1_P_FELO	VDD_RF2_T_DA	111	PP RF2 2V05 TX DA
PP RF1 1V3 PRX FELO2	42	VDD_RF1_P_FELO	VDD_RF1_T_DA	118	PP RF1 1V3 TX DA
PP RF1 1V3 DRX LBLO	28	VDD_RF1_D_LBLO	VDD_RF1_T_UPC	117	PP RF1 1V3 TX UPCONVERTER
PP RF1 1V3 DRX FE	26	VDD_RF1_D_FE	VDD_RF1_T_LO	116	PP RF1 1V3 TX LO
PP RF1 1V3 DRX MBLO	25	VDD_RF1_D_MBLO	VDD_RF2_T_BB	108	PP RF2 2V05 TX BB
PP RF1 1V3 JAM DET	85	VDD_RF1_JDET	VDD_RF2_T_VCO	136	PP RF2 2V05 TX VCO
PP RF2 2V05 PRX BB	83	VDD_RF2_P_BB	VDD_RF2_XO	127	PP RF2 2V05 XO FILT
PP RF2 2V05 DRX BB	44	VDD_RF2_D_BB	VDD_RF1_T_SYN	98	PP RF1 1V3 TX SYNTH
PP RF2 2V05 PRX VCO	67	VDD_RF2_P_VCO	VDD_RF2_T_PLL	97	PP RF2 2V05 TX PLL
PP RF1 1V3 PRX VCO	76	VDD_RF1_P_VCO	VDD_RF1_G_LNA	24	PP RF1 1V3 GPS LNA
PP RF1 1V3 PRX PLL	66	VDD_RF1_P_PLL	VDD_RF1_G_VCO	37	PP RF1 1V3 GPS VCO
PP RF2 2V05 SHDR VCO	51	VDD_RF2_S_VCO	VDD_RF1_G_PLL	55	PP RF1 1V3 GPS PLL
PP RF1 1V3 SHDR VCO	40	VDD_RF1_S_VCO	VDD_RF1_G_BB	31	PP RF1 1V3 GPS DIG
PP RF1 1V3 SHDR PLL	55	VDD_RF1_S_PLL	VDD_DIO	87	PP RF1 1V8 DIG

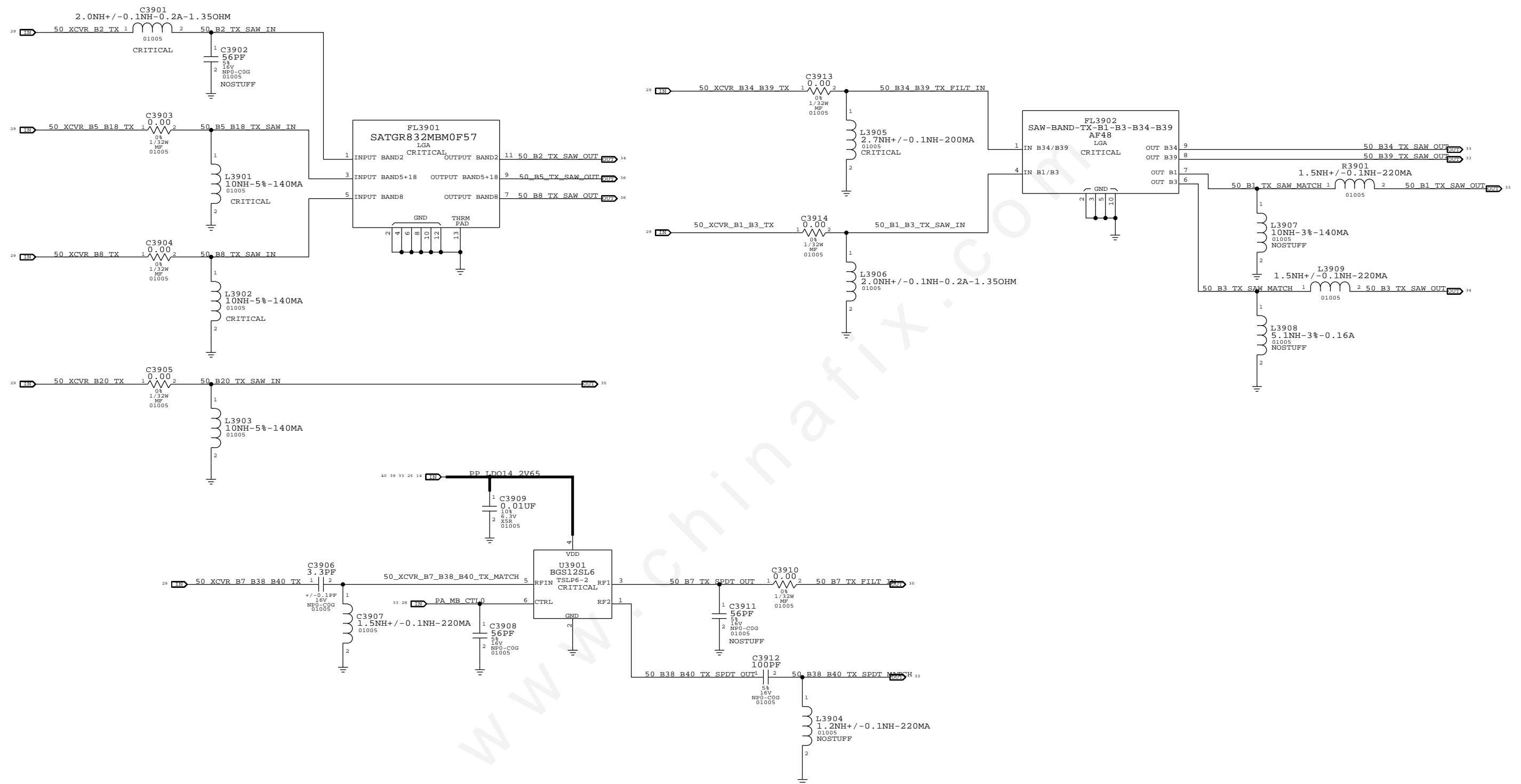
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RX MATCHING



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TX INTERSTAGE FILTERS



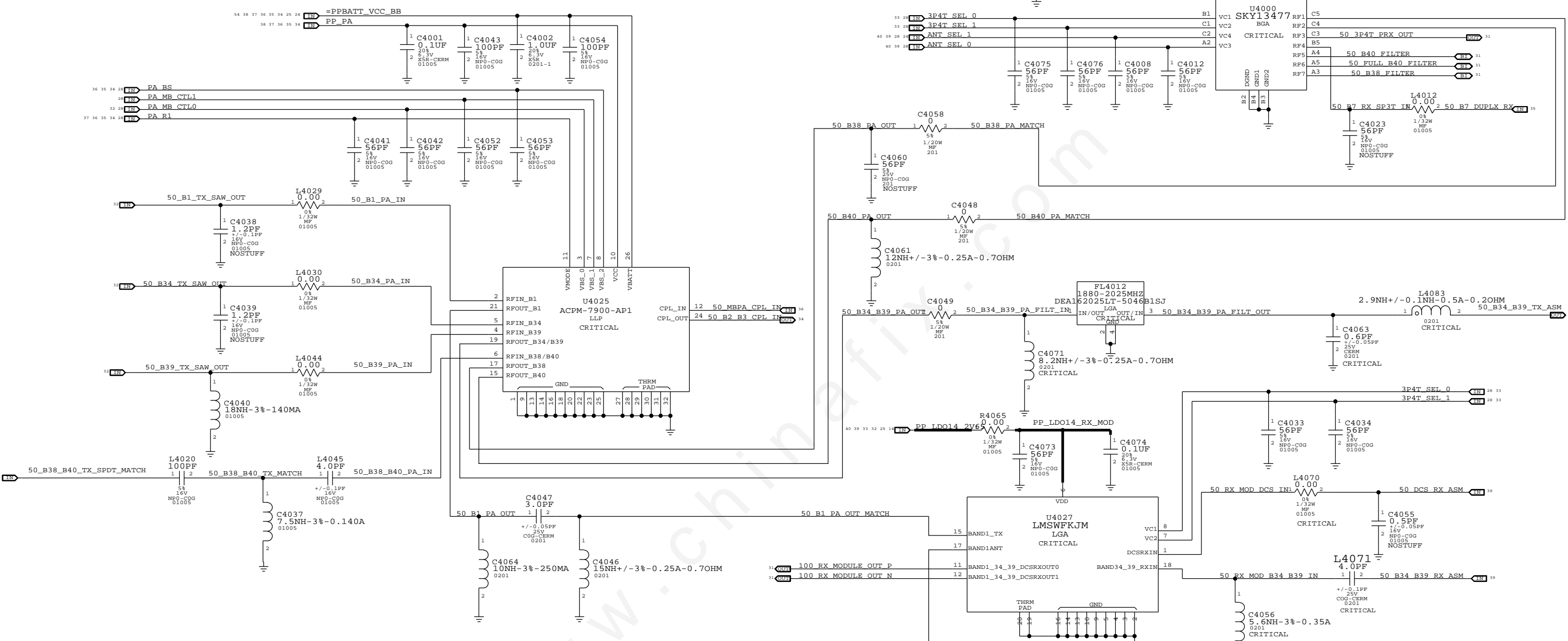
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	PAGE	39 OF 121
	SHEET	32 OF 54



BAND 1/34/39/38/40 TX

D
C
B
A

D
C
B
A



BAND	PA POWER MODE	PA_BS	PA_CTL1	PA_CTL0	PA_R1
OFF	X	X	0	0	0
B1	HPM	X	1	0	0
B1	LPM	X	1	0	1
B34	HPM	1	0	1	0
B34	LPM	1	0	1	1
B39	HPM	0	0	1	0
B39	LPM	0	0	1	1
B38	HPM	1	1	1	0
B38	LPM	1	1	1	1
B40	HPM	0	1	1	0
B40	LPM	0	1	1	1

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40 OF 121

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33 OF 54

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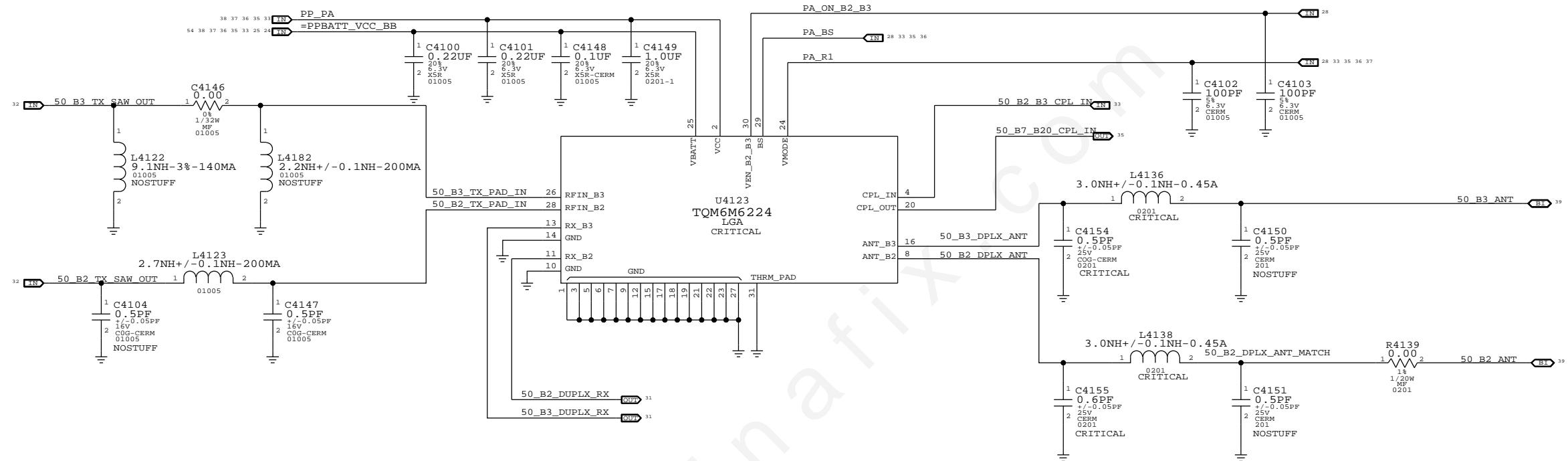
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BAND 2 / 3 PAD

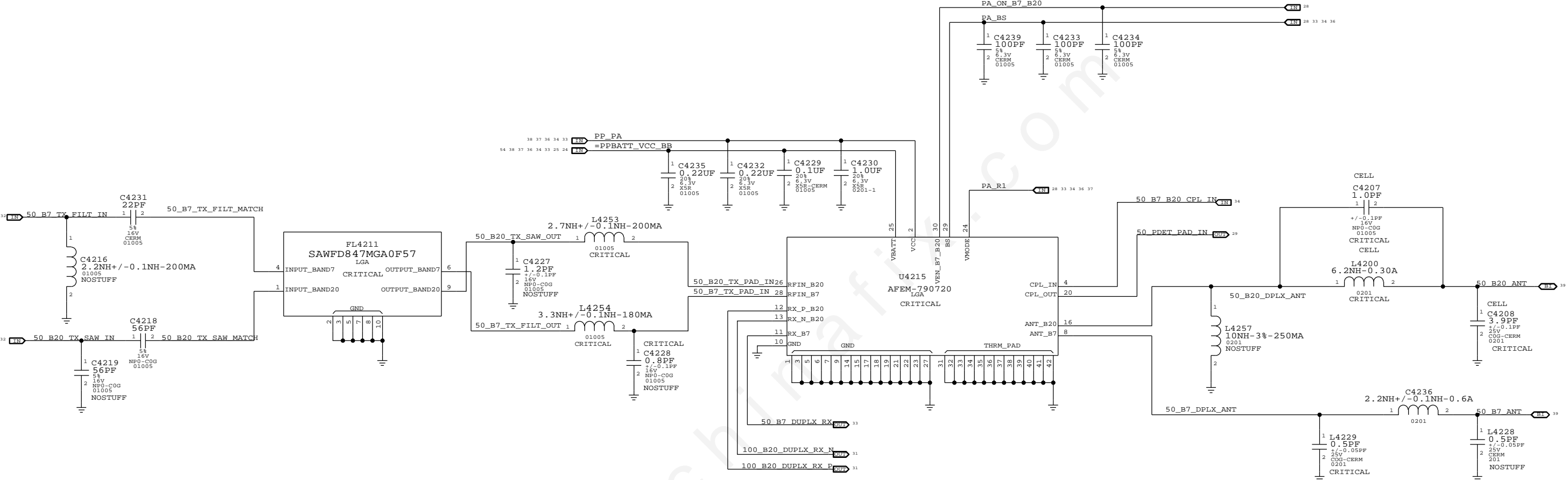


BAND	PA	POWER	MODE	PA_BS	PA_ON_B2_B3	PA_R1
=====	=====	=====	=====	=====	=====	=====
OFF		X		X	0	X
B3		HPM		0	1	0
B3		LPM		0	1	1
B2		HPM		1	1	0
B2		LPM		1	1	1


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BAND 20/7 PAD

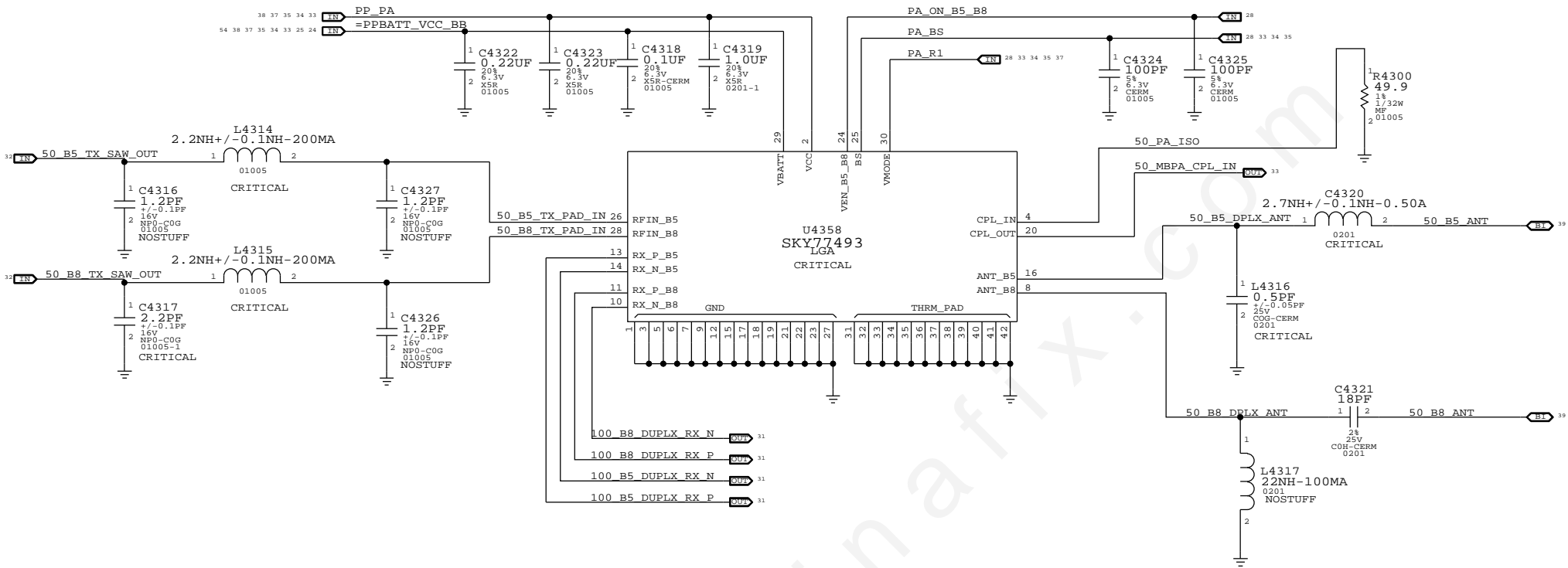


BAND	PA	POWER	MODE	PA_BS	PA_ON_B20_B7	PA_R1
=====	=====	=====	=====	=====	=====	=====
OFF		X		X	0	X
B20		HPM		0	1	0
B20		LPM		0	1	1
B7		HPM		1	1	0
B7		LPM		1	1	1

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BAND 5 / 8 PAD



BAND	PA	POWER	MODE	PA_BS	PA_ON_B5_B8	PA_R1
=====	=====	=====	=====	=====	=====	=====
OFF		X		X	0	X
B5		HPM		0	1	0
B5		LPM		0	1	1
B8		HPM		1	1	0
B8		LPM		1	1	1

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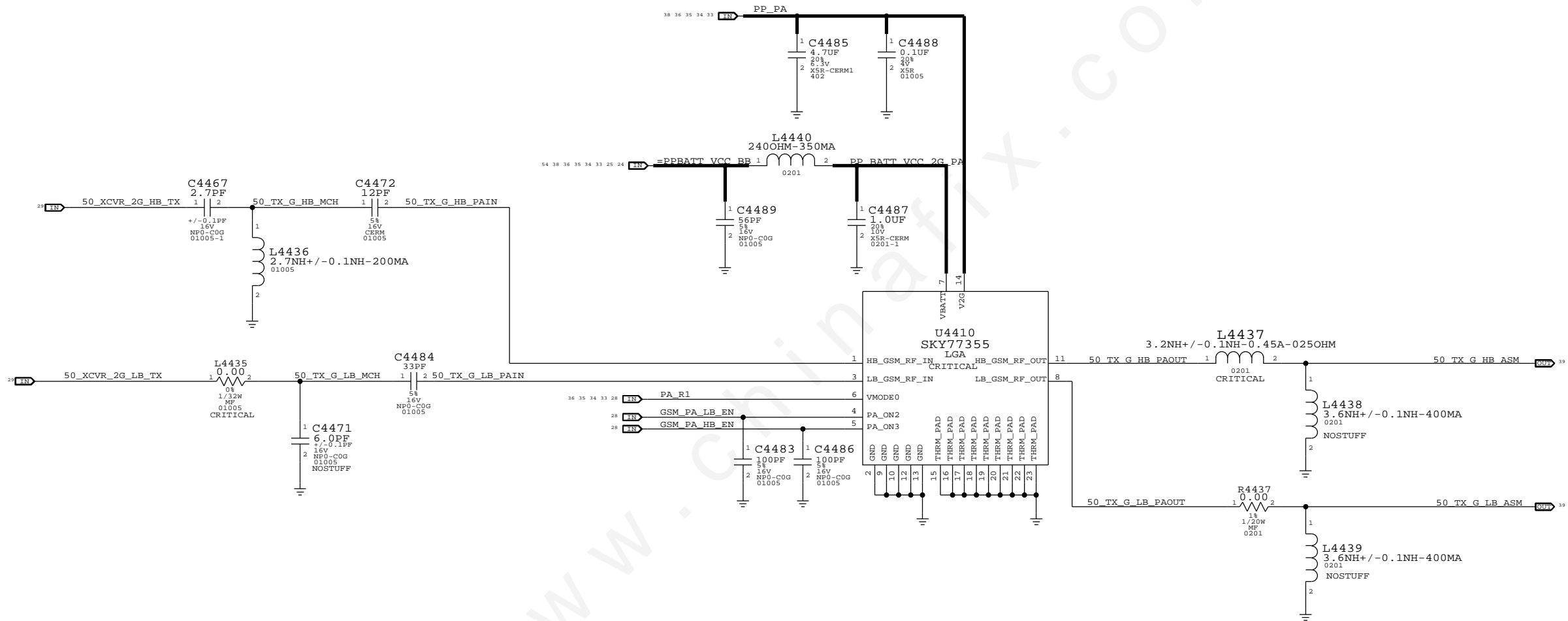


2G PA


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2G PA GAIN MODES

BAND	MODE	GAIN MODE	PA_R1	PCL RANGE
LOW BAND	GSM	ULTRA LOW	HIGH	16 TO 19
LOW BAND	GSM	LOW	HIGH	14 TO 15
LOW BAND	GSM	MEDIUM	LOW	7 TO 13
LOW BAND	GSM	HIGH	LOW	5 TO 6
HIGH BAND	GSM	ULTRA LOW	HIGH	10 TO 15
HIGH BAND	GSM	LOW	HIGH	7 TO 9
HIGH BAND	GSM	HIGH	LOW	0 TO 6
LOW BAND	EDGE	LOW	HIGH	15 TO 19
LOW BAND	EDGE	MEDIUM	LOW	10 TO 14
LOW BAND	EDGE	HIGH	LOW	8 TO 9
HIGH BAND	EDGE	LOW	HIGH	9 TO 15
HIGH BAND	EDGE	HIGH	LOW	2 TO 8

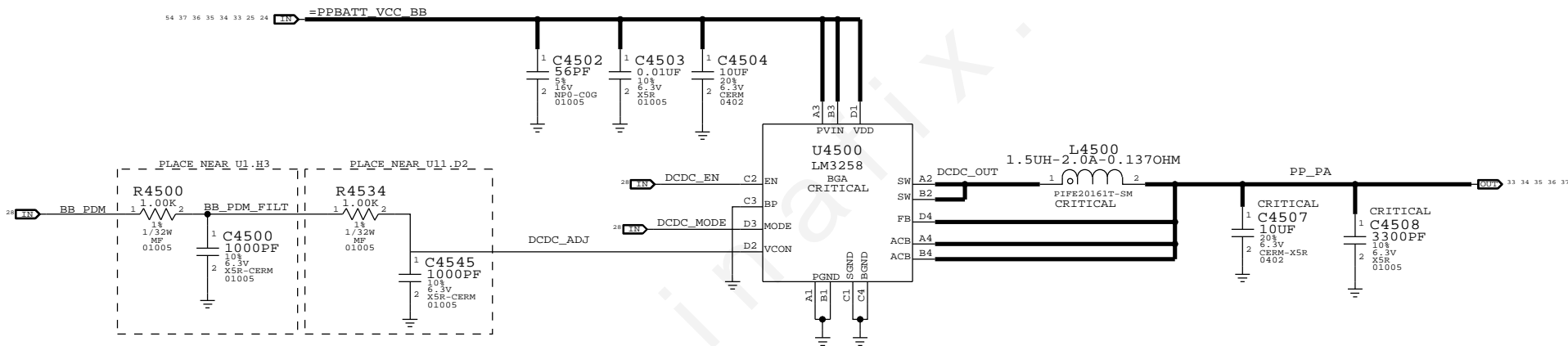



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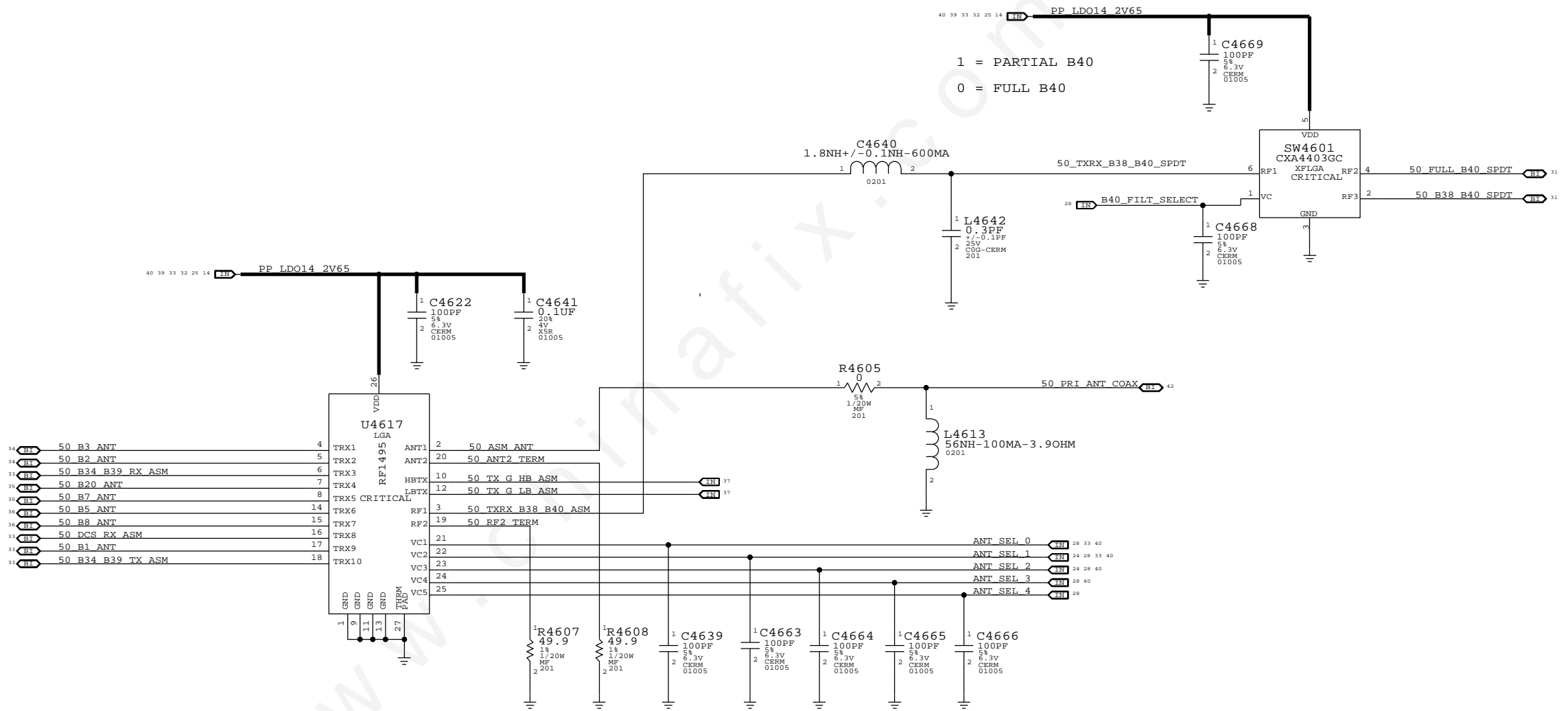
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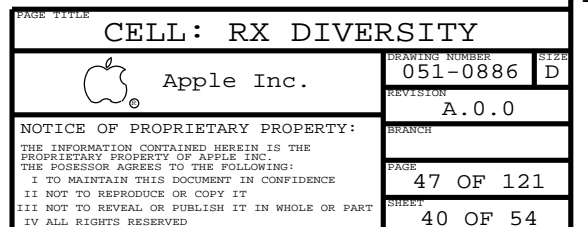
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	PAGE	45 OF 121
	SHEET	38 OF 54



PRIMARY ASM



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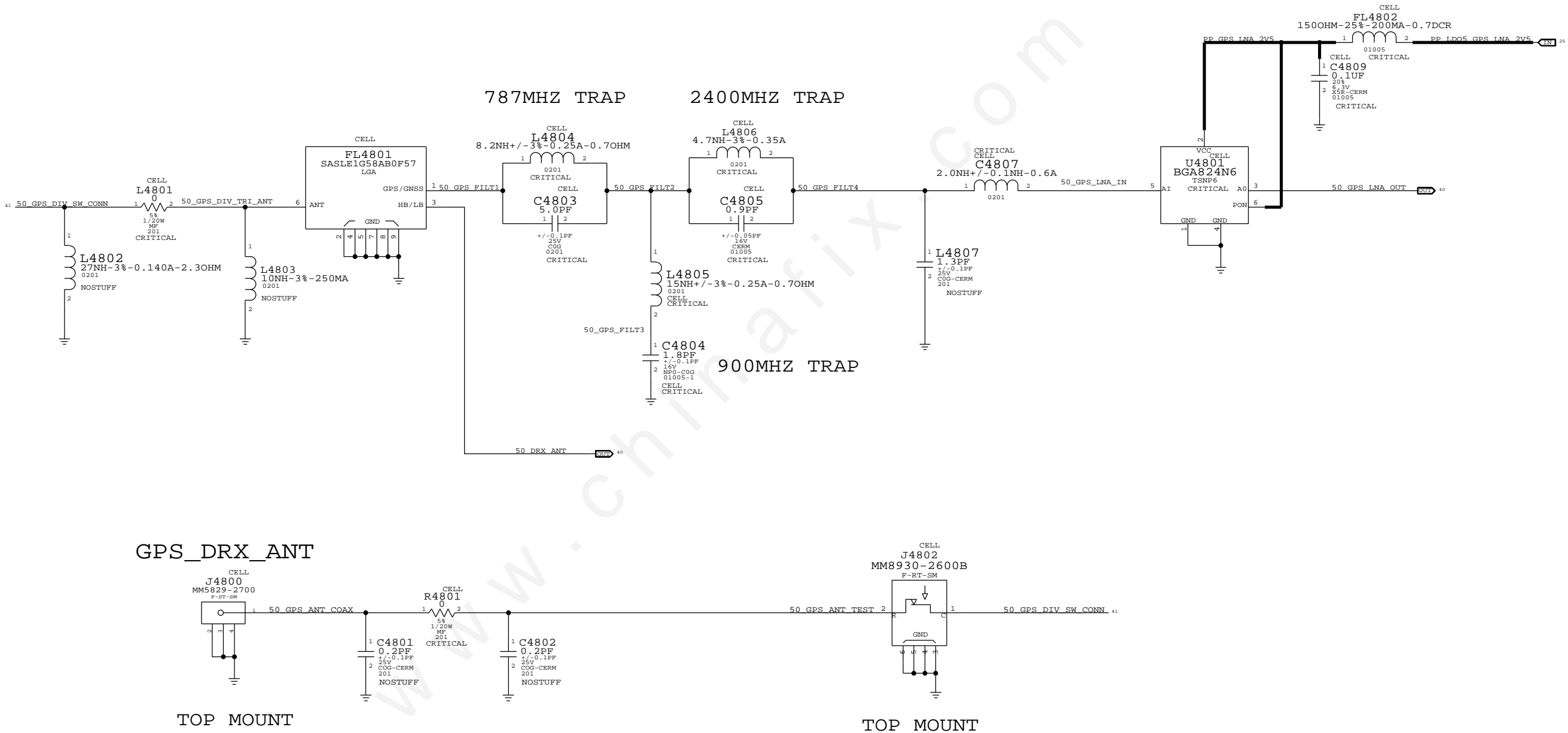



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GPS

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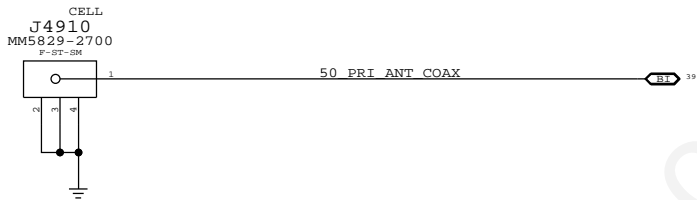



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		SHEET	41 OF 54

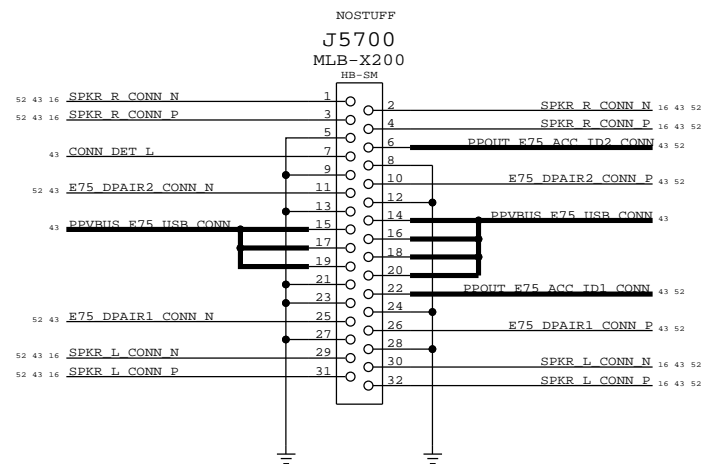


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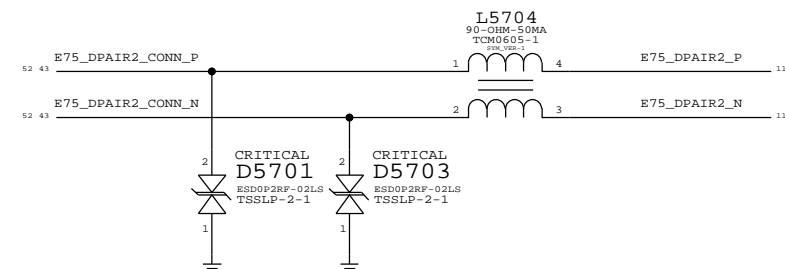
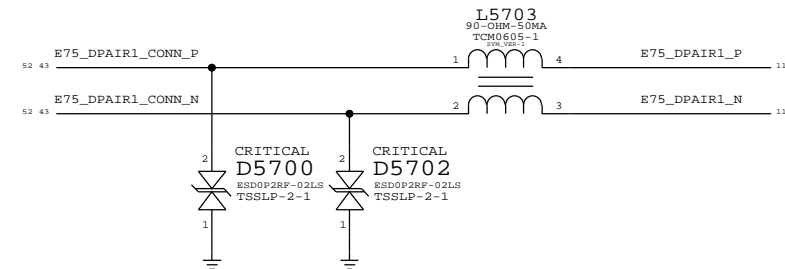
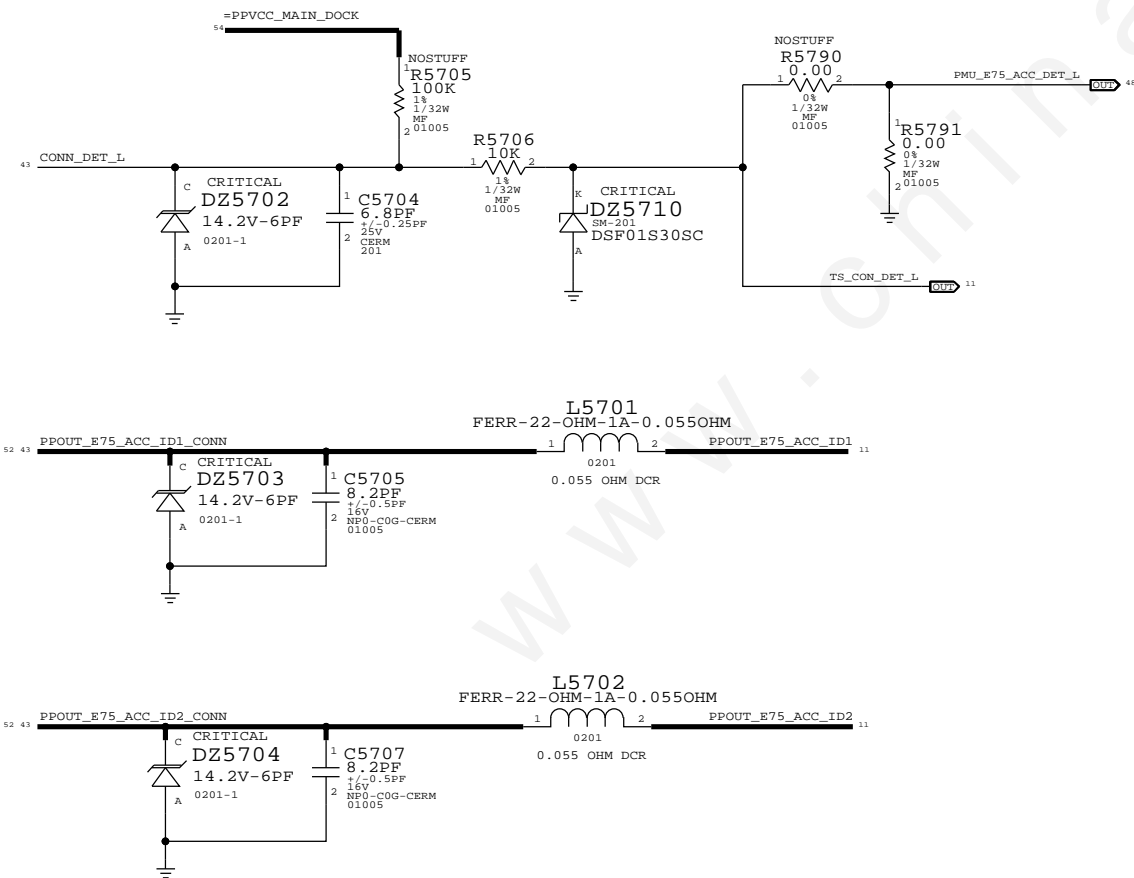
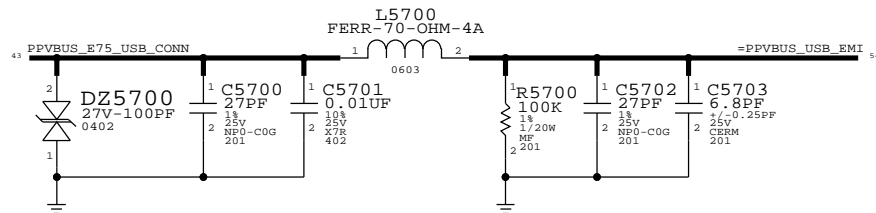
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		PAGE	49 OF 121
		SHEET	42 OF 54



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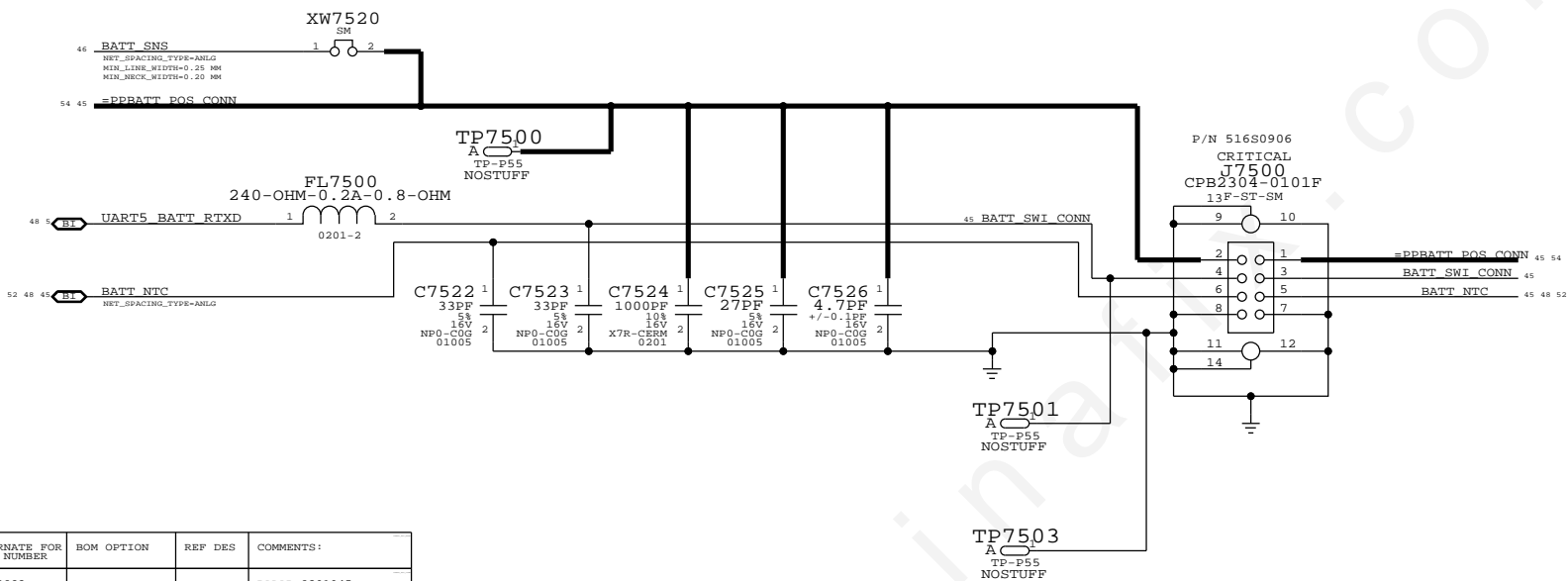



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		PAGE	57 OF 121
		SHEET	43 OF 54

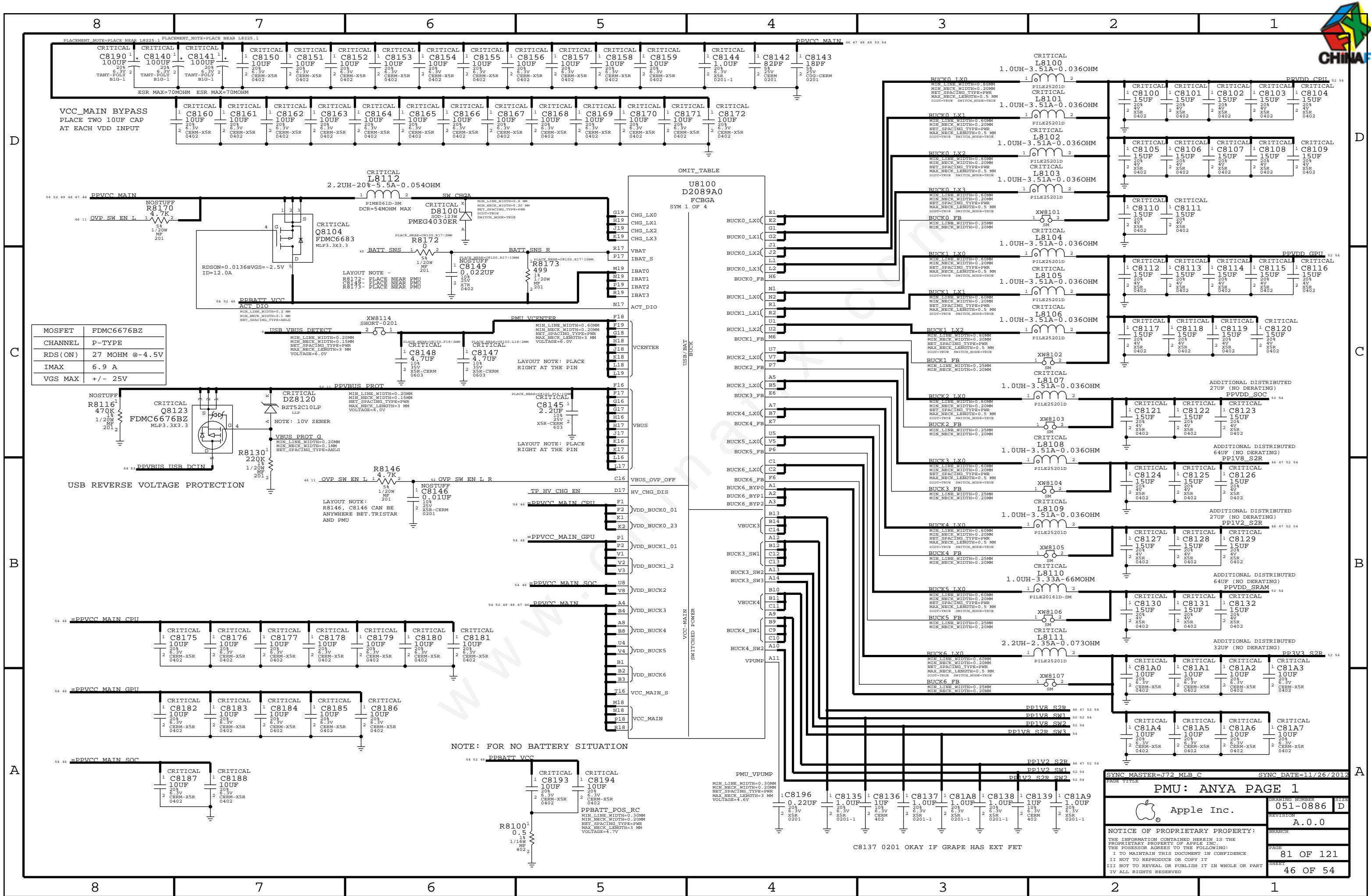


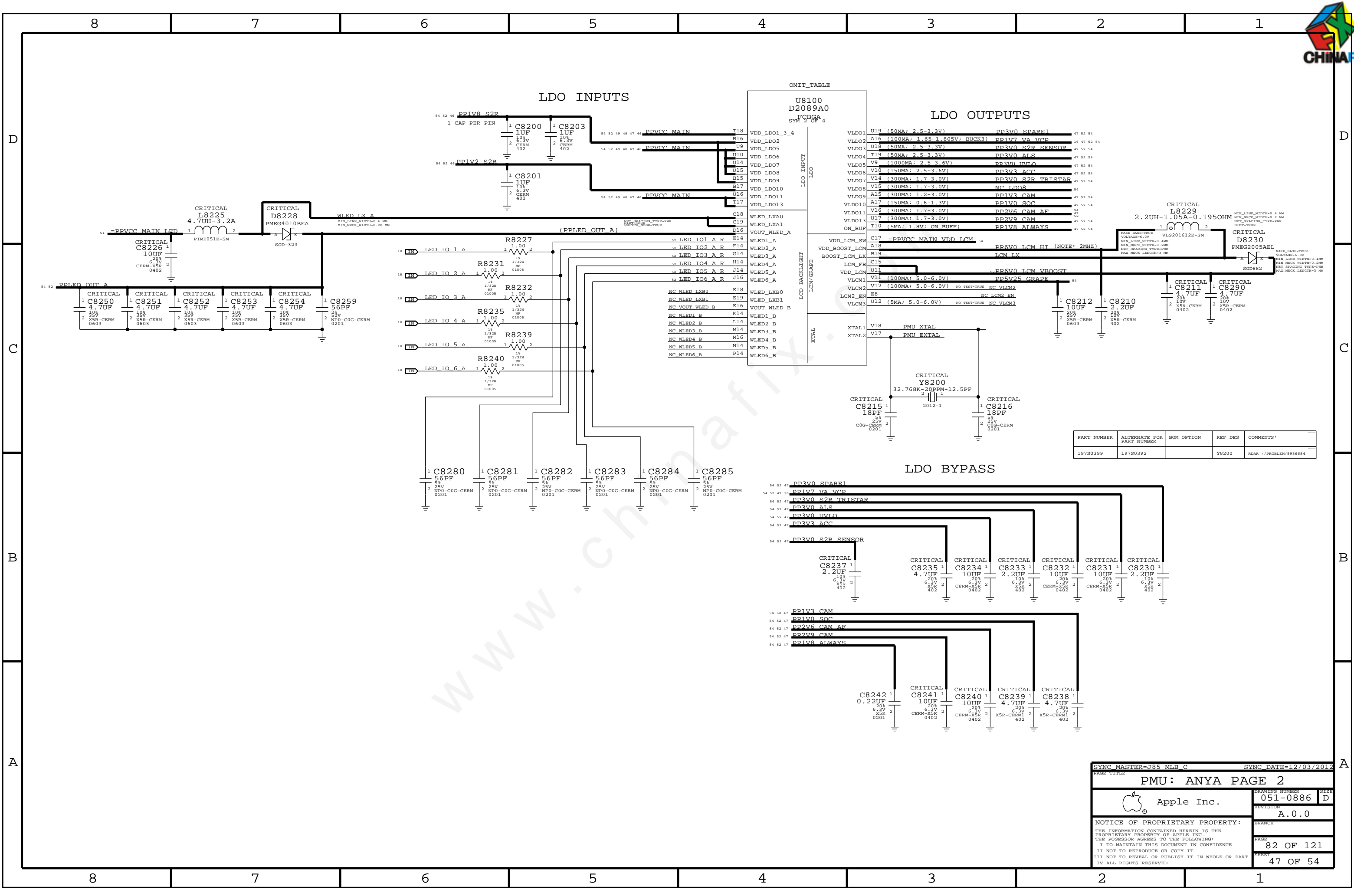
C





SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
POWER: BATTERY CONNECTOR			
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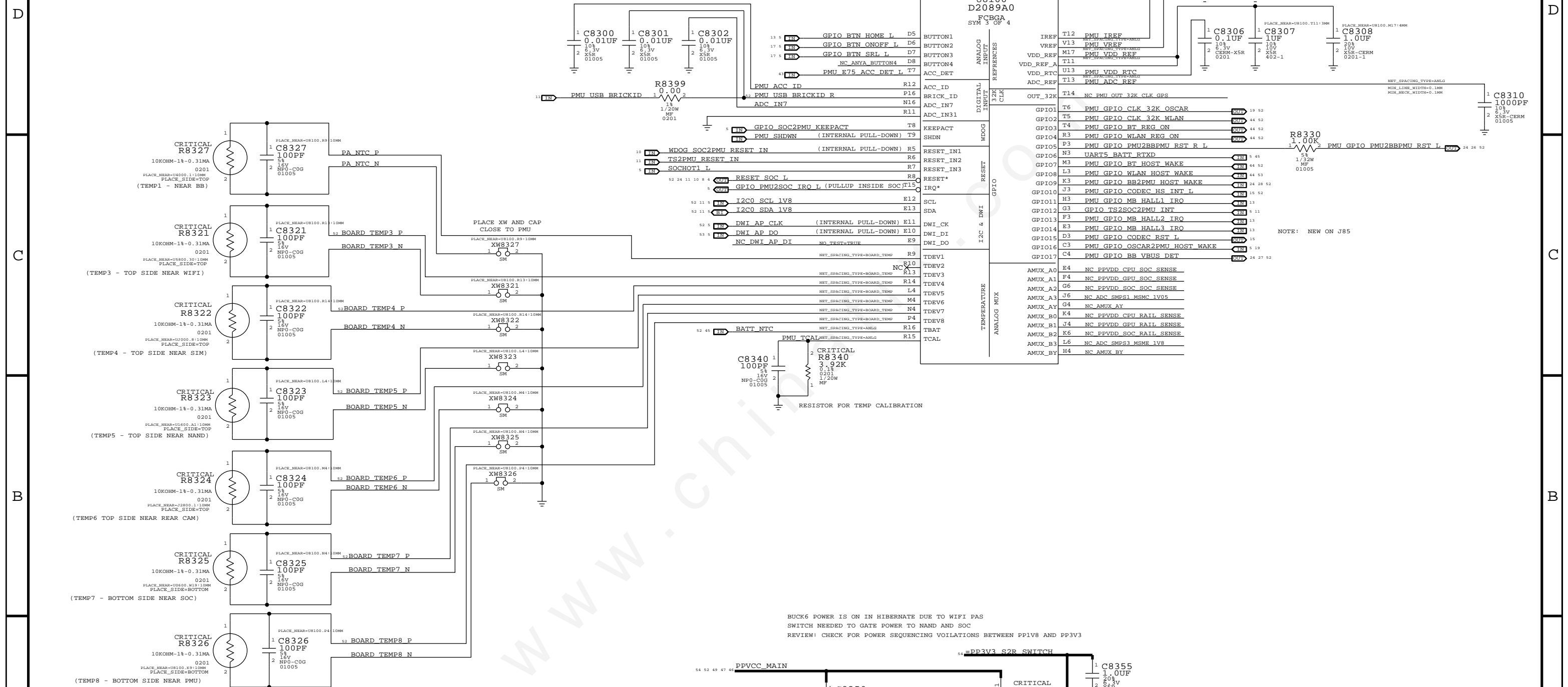




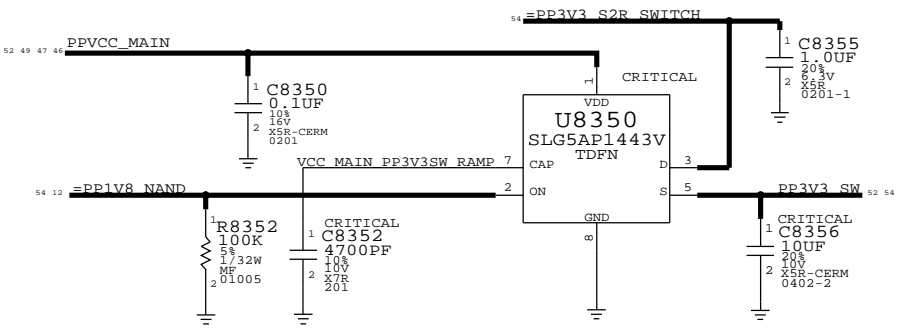
REVIEW: VERIFY NC ON TDEV2 IS OK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0739	138S0706		C8308	

I2C ADDRESS: 0111100X (0X78)

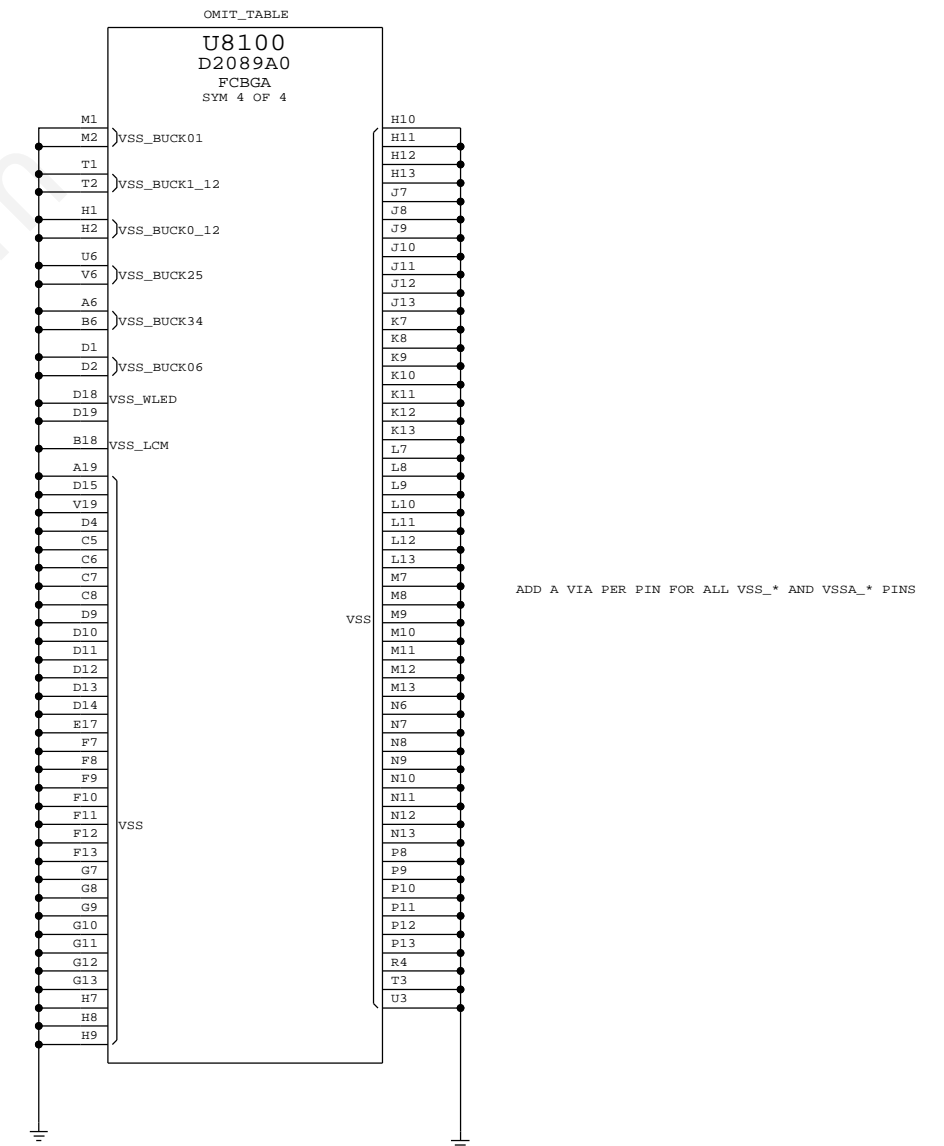
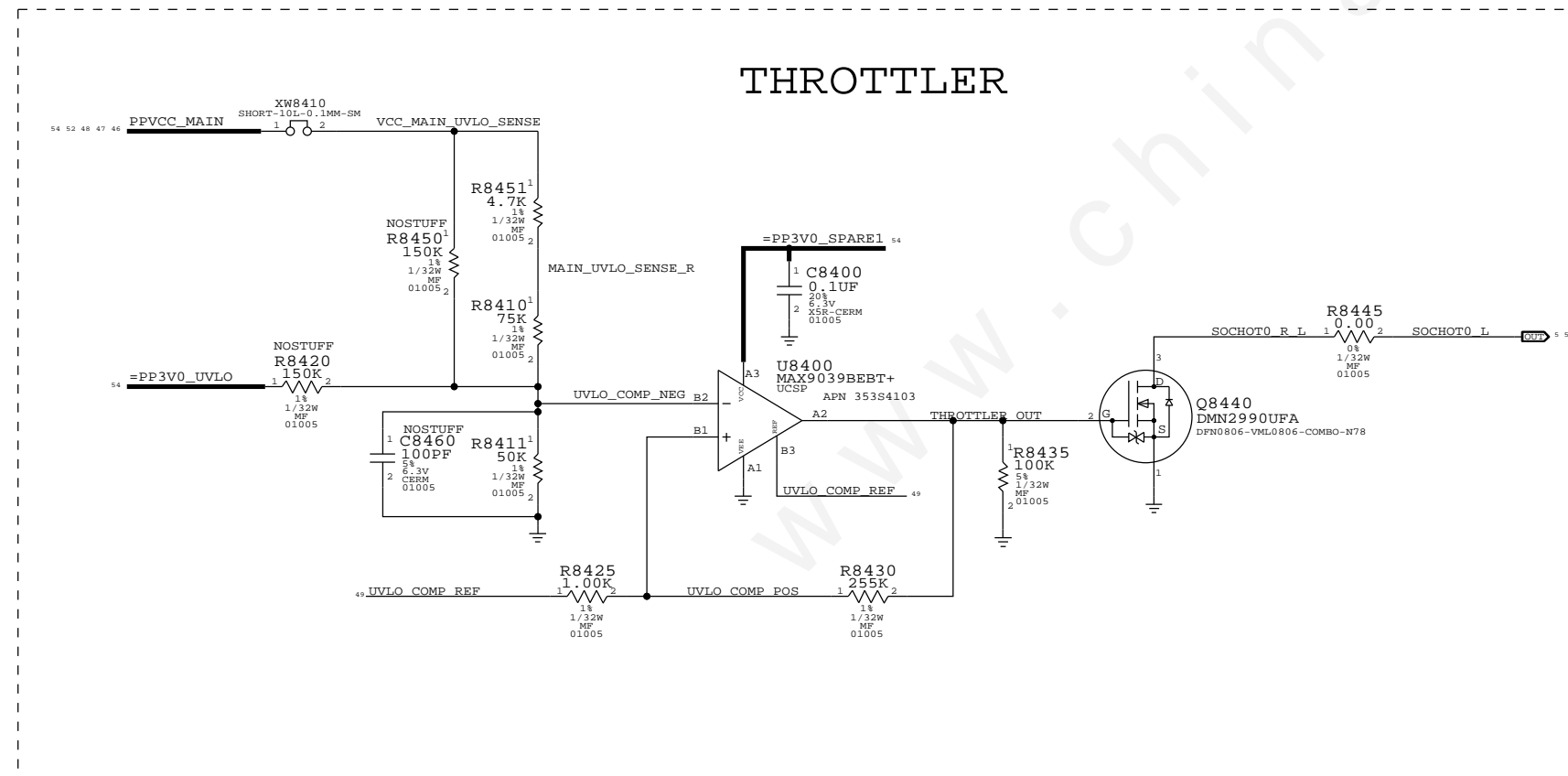


BUCK6 POWER IS ON IN HIBERNATE DUE TO WIFI PAS
SWITCH NEEDED TO GATE POWER TO NAND AND SOC
REVIEW: CHECK FOR POWER SEQUENCING VIOLATIONS BETWEEN PP1V8 AND PP3V3



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	R8321, R8322	R8323, R8324	RDAR: // PROBLEM/8380167
118S0764	118S0717		R8340	RDAR: // PROBLEM/8380167

PAGE TITLE		SYNC DATE=11/26/2012	
PMU: ANYA PAGE 3			
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[illegible]



D

C

B

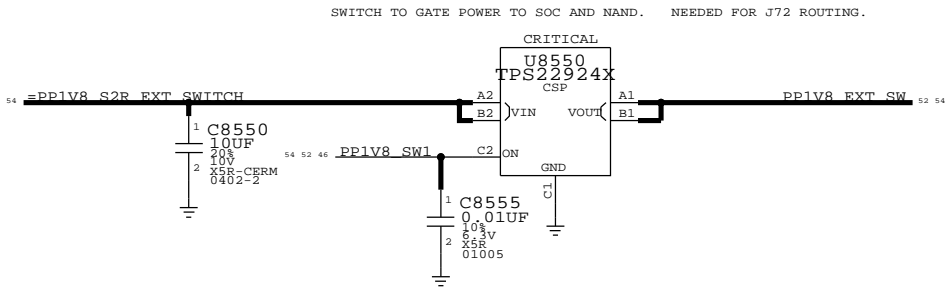
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A



SYNC MASTER=J85 MLB C		SYNC DATE=11/26/2012	
PAGE TITLE			
POWER: PP1V8_SW			
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		SHEET	50 OF 54

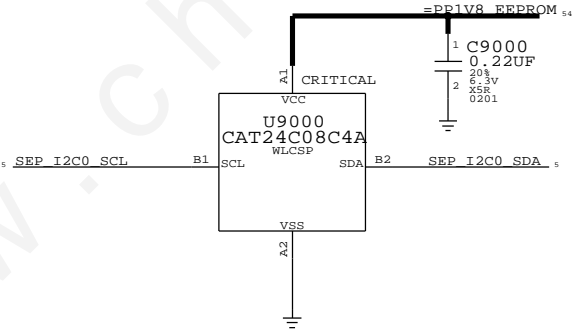



DEBUG

54 5 =PP1V8 S2R MISC TF9002
C A
TP-P55

SEP EEPROM

UNPROGRAMMED P/N: 335S0894




SYNC MASTER=J72 MLB C		SYNC DATE=11/26/2012	
PAGE TITLE			
SEP: EEPROM & SOC DEBUG			
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8	7	6	5	4	3	2	1
<div>TP9300 GPIO CODEC IRO L 5 15</div> <div>TP9304 PMU GPIO CODEC HS INT L 15 48</div> <div>TP9303 BATT NTC 45 48</div> <div>TP9305 PPLED OUT A 47 54</div> <div>TP9396 PP3V0 UVLO 47 54</div> <div>TP9397 PP3V0 SPARE1 47 54</div> <div>TP9398 SOCHOT0 L 5 49</div> <div>TP9312 BOARD TEMP3 P 48</div> <div>TP9313 BOARD TEMP4 P 48</div> <div>TP9314 BOARD TEMP5 P 48</div> <div>TP9315 BOARD TEMP6 P 48</div> <div>TP9316 BOARD TEMP7 P 48</div> <div>TP9317 BOARD TEMP8 P 48</div> <div>TP9318 CLK 32K SOC2CUMULUS 5 13</div> <div>TP9320 CODEC HP DET R 15</div> <div>TP9321 CODEC HP HS3 15</div> <div>TP9322 CODEC HP HS3 REF 15</div> <div>TP9323 CODEC HP HS4 15</div> <div>TP9324 CODEC HP HS4 REF 15</div> <div>TP9325 CODEC HP LEFT 15</div> <div>TP9326 CODEC HP RIGHT 15</div> <div>TP9328 DISPLAY SYNC R 13</div> <div>TP9329 DWI AP CLK 5 48</div> <div>TP9330 E75 DPAIR1 CONN N 43</div> <div>TP9331 E75 DPAIR1 CONN P 43</div> <div>TP9332 E75 DPAIR2 CONN N 43</div> <div>TP9333 E75 DPAIR2 CONN P 43</div> <div>TP9334 FMIO CE0 L 6 12</div> <div>TP9335 FMI1 CE0 L 6 12</div> <div>TP9336 GND</div> <div>TP9337 GND AUDIO CODEC 15</div> <div>TP9338 GPIO BTN HOME FILT L 13</div> <div>TP9339 GPIO BTN ONOFF L FILT 17</div> <div>TP9340 GPIO BTN SRL L FILT 17</div> <div>TP9341 GPIO BTN VOL DOWN L FILT 17</div> <div>TP9342 GPIO BTN VOL UP L FILT 17</div> <div>TP9343 GPIO FORCE DFU 5</div> <div>TP9344 GPIO GRAPE IRO L 5 13</div> <div>TP9345 GPIO GRAPE RST L 5 13</div> <div>TP9346 GPIO SOC2BB WAKE MODEM 5 28</div> <div>TP9347 GPIO SPKAMP KEEPALIVE 5 16</div> <div>TP9348 I2C0_SCL_1V8 5 11 48</div> <div>TP9349 I2C0_SDA_1V8 5 11 48</div> <div>TP9350 I2C2_SCL_1V8 5 16</div> <div>TP9351 I2C2_SDA_1V8 5 16</div> <div>TP9352 ISP0_CAM_REAR_CLK 7 23</div> <div>TP9353 ISP0_CAM_REAR_SCL 7 23</div> <div>TP9354 ISP0_CAM_REAR_SDA 7 23</div> <div>TP9355 ISP0_CAM_REAR_SHUTDOWN L 7 23</div> <div>TP9356 ISP1_CAM_FRONT_CLK 7 20</div> <div>TP9357 ISP1_CAM_FRONT_SCL 7 20</div> <div>TP9358 ISP1_CAM_FRONT_SDA 7 20</div> <div>TP9359 ISP1_CAM_FRONT_SHUTDOWN L 7 20</div> <div>TP9360 JTAG SOC SEL 4 10</div> <div>TP9361 JTAG SOC TCK 4 11</div> <div>TP9362 JTAG SOC TDI 4</div> <div>TP9363 JTAG SOC TMS 4 11</div> <div>TP9364 JTAG SOC TRST L 4 10</div> <div>TP9365 JTAG WLAN SEL 44</div> <div>TP9366 OSCAR2RADIO_CONTEXT A 19 28 44</div> <div>TP9367 OSCAR2RADIO_CONTEXT B 19 28 44</div> <div>TP9368 WLAN_TX BLANK 28 44</div> <div>TP9369 LAT_SW1_CTL 14 24 28</div> <div>TP9370 LAT_SW2_CTL 14 28</div> <div>TP9371</div> <div>TP9372 LED IO1 A R 47</div> <div>TP9373 LED IO2 A R 47</div> <div>TP9374 LED IO3 A R 47</div> <div>TP9375 LED IO4 A R 47</div> <div>TP9376 LED IO5 A R 47</div> <div>TP9377 LED IO6 A R 47</div> <div>TP9378 MIKEY TS N 11 15</div> <div>TP9379 MIKEY TS P 11 15</div> <div>TP9380 OVP_SW_EN_L_R 46</div> <div>TP9382 PMU GPIO BT_HOST_WAKE 44 48</div> <div>TP9383 PMU GPIO BT_REG_ON 44 48</div> <div>TP9384 PMU GPIO_CLK_32K_OSCAR 19 48</div> <div>TP9385 PMU GPIO_CLK_32K_WLAN 44 48</div> <div>TP9387 PMU_USB_BRICKID_R 48</div> <div>TP9388 PP1V0_SOC 47 54</div> <div>TP9389 PP1V2_S2R 46 47 54</div> <div>TP9390 PP1V2_S2R_SW2 46 54</div> <div>TP9391 PP1V2_SW1 46 54</div> <div>TP9393 PP1V7_VA_VCP 16 47 54</div> <div>TP9395 PP1V8_ALWAYS 47 54</div> <div>TP93A0 PP1V8_EXT_SW 50 54</div> <div>TP93A1 PP1V8_GRAPE_FILT 13</div> <div>TP93A2 PP1V8_GRAPE_SW 13</div> <div>TP93A3 PP1V8_PLL_SOC_F 4</div> <div>TP93A4 PP1V8_S2R 46 47 54</div> <div>TP93A6 PP1V8_S2R_SW3_COMP 54</div> <div>TP93A7 PP1V8_SW1 46 50 54</div> <div>TP93A8 PP1V8_SW2 46 54</div> <div>TP93A9 PP1V8_XTAL 8</div> <div>TP93B0 PP2V6_CAM_AF 47 54</div> <div>TP93B8 PP3V0_S2R_HALL_FILT 13</div> <div>TP93C0 PP3V0_S2R_SENSOR 47 54</div> <div>TP93C1 PP3V0_S2R_TRISTAR 47 54</div> <div>TP93C3 PP3V3_ACC 47 54</div> <div>TP93C4 PP3V3_S2R 46 54</div> <div>TP93C5 PP3V3_SW 48 54</div> <div>TP93C6 PP5V25_GRAPE_FILT 13</div> <div>TP93C8 PP6V0_LCM_VBOOST 47</div> <div>TP93C9 PPBATT_VCC 46 54</div> <div>TP93D0 PPLED_BACK_REG_A 18</div> <div>TP93D1 PPOUT_E75_ACC_ID1_CONN 43</div> <div>TP93D2 PPOUT_E75_ACC_ID2_CONN 43</div> <div>TP93D3 PPVBUS_PROT 11 46</div> <div>TP93D4 PPVBUS_USB_DCIN 46 54</div> <div>TP93D5 PPVCC_MAIN 46 47 48 49 54</div> <div>TP93D6 PPVCC_MAIN_LCD_SW_CONN 18</div> <div>TP93D7 PPVDD_CPU 46 54</div> <div>TP93D8 PPVDD_GPU 46 54</div> <div>TP93D9 PPVDD_SOC 46 54</div> <div>TP93E0 PPVDD_SRAM 46 54</div> <div>TP93G4 PP_SMPS4_RF2_2V05 25 30</div> <div>TP93G9 SOC_TESTMODE 4 10</div> <div>TP93H1 SPI1_GRAPE_CS_L 5 13</div> <div>TP93H2 SPI1_GRAPE_MISO 5 13</div> <div>TP93H3 SPI1_GRAPE_MOSI 5 13</div> <div>TP93H4 SPI1_GRAPE_SCLK_R 13</div> <div>TP93H5 SPKR_L_CONN_N 16 43</div> <div>TP93H6 SPKR_L_CONN_P 16 43</div> <div>TP93H7 SPKR_R_CONN_N 16 43</div> <div>TP93H8 SPKR_R_CONN_P 16 43</div> <div>TP93I1 TP_JTAG_SOC_TDO 4</div> <div>TP93I2 TP_JTAG_WLAN_TCK 44</div> <div>TP93I3 TP_JTAG_WLAN_TRST_L 44</div> <div>TP93I4 UART0_SOC_RXD 5 11</div> <div>TP93I5 UART0_SOC_TXD 5 11</div> <div>TP93I6 UART3_BB2SOC_TX 5 11 24 28</div> <div>TP93I7 UART3_SOC2BB_TX 5 11 24 28</div> <div>TP93I8 UART6_TS_ACC_RXD 5 11</div> <div>TP93I9 UART6_TS_ACC_TXD 5 11</div> <div>TP93J0 USB_SOC_N 4 11</div> <div>TP93J1 USB_SOC_P 4 11</div> <div>TP93J9 PP3V0_ALS 47 54</div> <div>TP93JA PP2V9_CAM 47 54</div> <div>TP93JB PP1V3_CAM 47 54</div> <div>TP93JC PMU_GPIO_WLAN_REG_ON 44 48</div> <div>RF TEST POINTS</div> <div>TP93G1 PP_SMPS1_MSMC_1V05 25 27</div> <div>TP93G2 PP_SMPS3_MSME_1V8 24 25 27 28 30</div> <div>TP93G5 PP_SMPS5_DSP_1V05 25</div> <div>TP93H1 PP_LDO1 25</div> <div>TP93H5 TP_BB_TEST_MODE_0 27</div> <div>TP93I0 TP_BB_TEST_MODE_1 27</div> <div>TP93J0 SIMCRD_RST_CONN 10 24 28</div> <div>TP93J5 SIMCRD_CLK_CONN 10 24 28</div> <div>TP93J7 SIMCRD_IO_CONN 10 24 28</div> <div>TP93J8 SIM_TRAY_DETECT 10 24 28</div> <div>TP93J9 PP_LDO6_RUIM_1V8 10 24 25 27</div> <div>TP93J2 GPIO_SOC2BB_RADIO_ON_L 5 24 26</div> <div>TP93J3 GPIO_SOC2BB_RST_L 5 24 26</div> <div>TP93J4 PMU_GPIO_PMU2BBPMU_RST_L 24 26 48</div> <div>TP93J5 PMU_GPIO_BB2PMU_HOST_WAKE 24 28 48</div> <div>TP93J6 PS_HOLD_PMIC 24 26</div> <div>TP93J7 DEBUG_RST_L 24 27</div> <div>TP93J8 BB_JTAG_RTCLK 24 27</div> <div>TP93J9 BB_JTAG_TCK 5 24 27</div> <div>TP93J0 BB_JTAG_TDI 5 24 27</div> <div>TP93J1 BB_JTAG_TDO 5 24 27</div> <div>TP93J2 BB_JTAG_TMS 5 24 27</div> <div>TP93J3 BB_JTAG_TRST_L 5 24 27</div> <div>TP93J4 USB_BB_N 11 24 53</div> <div>TP93J5 USB_BB_P 11 24 53</div> <div>TP93J6 RESET_SOC_L 4 8 10 11 24 48</div> <div>TP93J7 PMU_GPIO_BB_VBUS_DET 24 27 48</div> <div>STANDOFFS: P/N 860-1657</div> <div>STD9300</div> <div>STDOFF-3.3X1.8R1.28H-SM</div> <div>STD9301</div> <div>STDOFF-3.3X1.8R1.28H-SM</div> <div>STANDOFF: P/N 860-1683</div> <div>STD9302</div> <div>STDOFF-3.3X2.2R1.35H-SM-1</div> <div>PLATED THROUGH HOLES</div> <div>DRILL SIZE: 1.1MM X 0.4MM</div> <div>PLATING SIZE: 1.4MM X 0.7MM</div> <div>SL9300</div> <div>TH-NSP</div> <div>SL-1.1X0.4-1.4X0.7</div> <div>SL9303</div> <div>TH-NSP</div> <div>SL-1.1X0.4-1.4X0.7</div> <div>SL9304</div> <div>TH-NSP</div> <div>SL-1.1X0.4-1.4X0.7</div> <div>SL9305</div> <div>TH-NSP</div> <div>SL-1.1X0.4-1.4X0.7</div> <div>MH9300</div> <div>3P25R2P5</div> <div>860-1688</div> <div>MH9302</div> <div>WASHER-BTN-MLB-X221</div> <div>TH</div> <div>NEAR BUTTON FLEX CONN</div>							

SYNC MASTER=J85 MLB C		SYNC DATE=12/03/12	
PAGE TITLE			
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87654321

EE CHARACTERIZATION TP

FOR FRANK (SEG)

PP9450 1 PPVDD SOC SOC SENSE PLACE_NEAR=U0652.V31:1MM
PP9451 1 PPVDD CPU SOC SENSE PLACE_NEAR=U0652.AN30:1MM

NAND

PP9401 1 FMI0_DQS PLACE_SIDE=BOTTOM PLACE_NEAR=U0652.D34:2MM
PP9402 1 FMI0_AD<3> PLACE_SIDE=BOTTOM PLACE_NEAR=U0652.C34:2MM
PP9403 1 FMI0_DQS PLACE_NEAR=U0652.D34:2MM
PP9410 1 TP_TCKC_U1400
PP9411 1 TP_TM5C_U1400
PP9412 1 TP_U1400_RB0
PP9413 1 TP_U1400_RB1

DWI

PP9405 1 DWI_AP_DO PLACE_SIDE=BOTTOM PLACE_NEAR=U8100:2MM

AUDIO

PP9406 1 I2S0_CODEC_ASP_MCK PLACE_NEAR=U1900:2MM

PP9416 1 I2S2_CODEC_XSP_LRCK PLACE_NEAR=U1900:2MM
PP9417 1 I2S2_CODEC_XSP_DOUT PLACE_NEAR=U1900:2MM

PP9419 1 I2S1_SPKAMP_MCK PLACE_NEAR=U2040:2MM
PP9420 1 I2S1_SPKAMP_BCLK PLACE_NEAR=U2040:2MM
PP9421 1 I2S1_SPKAMP_LRCK PLACE_NEAR=U2040:2MM
PP9422 1 I2S1_SPKAMP_DOUT PLACE_NEAR=U2040:2MM
PP9423 1 I2S1_SPKAMP_DIN PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM

PP9424 1 SPI2_CODEC_SCLK PLACE_NEAR=U1900:2MM
PP9425 1 SPI2_CODEC_MOSI PLACE_NEAR=U1900:2MM
PP9426 1 SPI2_CODEC_MISO PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM

GRAPE

OSCAR

PP9428 1 UART4_SOC2OSCAR_TXD PLACE_SIDE=BOTTOM PLACE_NEAR=U2400:2MM
PP9429 1 UART4_OSCAR2SOC_RXD PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM

UART5

CAMERA

PP9440 1 MIPI1C_CAM_FRONT_CLK_P PLACE_NEAR=U0652.AR33:3MM
PP9441 1 MIPI1C_CAM_FRONT_CLK_N PLACE_NEAR=U0652.AR34:3MM
PP9442 1 MIPI1C_CAM_FRONT_DATA_P<0> PLACE_NEAR=U0652.AT33:3MM
PP9443 1 MIPI1C_CAM_FRONT_DATA_N<0> PLACE_NEAR=U0652.AT34:3MM
PP9444 1 MIPI0C_CAM_REAR_CLK_P PLACE_NEAR=U0652.AU25:3MM
PP9445 1 MIPI0C_CAM_REAR_CLK_N PLACE_NEAR=U0652.AV25:3MM
PP9446 1 MIPI0C_CAM_REAR_DATA_P<0> PLACE_NEAR=U0652.AU27:3MM
PP9447 1 MIPI0C_CAM_REAR_DATA_N<0> PLACE_NEAR=U0652.AV27:3MM

HIGH SPEED, NO TEST

MIPI0C_CAM_REAR_CLK_P NO_TEST=TRUE
MIPI0C_CAM_REAR_CLK_N NO_TEST=TRUE
MIPI0C_CAM_REAR_DATA_P<0..3> NO_TEST=TRUE
MIPI0C_CAM_REAR_DATA_N<0..3> NO_TEST=TRUE
MIPI0C_CAM_REAR_CLK_FILT_P NO_TEST=TRUE
MIPI0C_CAM_REAR_CLK_FILT_N NO_TEST=TRUE
MIPI0C_CAM_REAR_DATA_FILT_P<0..3> NO_TEST=TRUE
MIPI0C_CAM_REAR_DATA_FILT_N<0..3> NO_TEST=TRUE
MIPI1C_CAM_FRONT_CLK_P NO_TEST=TRUE
MIPI1C_CAM_FRONT_CLK_N NO_TEST=TRUE
MIPI1C_CAM_FRONT_DATA_P<0> NO_TEST=TRUE
MIPI1C_CAM_FRONT_DATA_N<0> NO_TEST=TRUE
MIPI1C_CAM_FRONT_CLK_FILT_P NO_TEST=TRUE
MIPI1C_CAM_FRONT_CLK_FILT_N NO_TEST=TRUE
MIPI1C_CAM_FRONT_DATA_FILT_P<0> NO_TEST=TRUE
MIPI1C_CAM_FRONT_DATA_FILT_N<0> NO_TEST=TRUE
EDP_DATA_P<0..3> NO_TEST=TRUE
EDP_DATA_EMI_P<0..3> NO_TEST=TRUE
EDP_DATA_EMI_N<0..3> NO_TEST=TRUE
EDP_DATA_EMI_CONN_P<0..3> NO_TEST=TRUE
EDP_DATA_EMI_CONN_N<0..3> NO_TEST=TRUE

WIFI

PP9480 1 HSIC1_WLAN2SOC_DEVICE_RDY
PP9481 1 HSIC1_WLAN2SOC_REMOTE_WAKE
PP9482 1 PMU_GPIO_WLAN_HOST_WAKE
PP9483 1 HSIC1_SOC2WLAN_HOST_RDY

GPIO_BT_WAKE FUNC_TEST=TRUE

FOR HSIC CHARACTERIZATION

PP9460 1 HSIC1_WLAN_DATA PLACE_NEAR=U0652.AN33:3MM

PP9462 1 HSIC1_WLAN_DATA PLACE_NEAR=U5800.13:3MM
PP9463 1 HSIC1_WLAN_STB PLACE_NEAR=U5800.14:3MM

PP9468 1 UART1_BT2SOC_TX PLACE_NEAR=U0652:3MM
PP9469 1 UART1_SOC2BT_TX PLACE_NEAR=U5800:3MM

PP9471 1 UART2_WLAN2SOC_TX PLACE_NEAR=U0652:3MM
PP9472 1 UART2_SOC2WLAN_TX PLACE_NEAR=U5800:3MM


BASEBAND

USB_BB_P FUNC_TEST=TRUE
USB_BB_N FUNC_TEST=TRUE

FOR HSIC CHARACTERIZATION

PP9465 1 HSIC2_BB_STB PLACE_NEAR=U0652.B27:3MM
PP9466 1 HSIC2_BB_DATA PLACE_NEAR=U3400.C7:3MM

PROX

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TEST: EE TP/PP				DRAWING NUMBER	051-0886
 Apple Inc.				REVISION	A.0.0
				BRANCH	
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				SHEET	53 OF 54



POWER CONNECTIONS

BUCK0

52 46 PPVDD_CPU == =PPVDD_CPU 9
MAKE_BASE=TRUE

BUCK1

52 46 PPVDD_GPU == =PPVDD_GPU 9
MAKE_BASE=TRUE

BUCK2

52 46 PPVDD_SOC == =PPVDD_SOC 9
MAKE_BASE=TRUE

BUCK3

52 47 46 PP1V8_S2R == =PP1V8_S2R_MISC 5 51
MAKE_BASE=TRUE == =PP1V8_S2R_VDDIO_WLAN_BT 44
== =PP1V8_S2R_TRISTAR 11
== =PP1V8_S2R_DDR 8
== =PP1V8_S2R_GRAPE 13
== =PP1V8_S2R_EXT_SWITCH 50
== =PP1V8_S2R_REAR_CAMERA
== =PP1V8_S2R_MESA
== =PP1V8_S2R_VDD_CORE_GPS
== =PP1V8_S2R_VDD_IO_GPS

BUCK3_SW

52 50 46 PP1V8_SW1 == =PP1V8_AUDIO 15
MAKE_BASE=TRUE == =PP1V8_DMIC 14
== =PP1V8_CAM_FRONT 20
== =PP1V8_CAM_REAR 23
== =PP1V8_PROX 22

PP1V8_EXT SW

52 50 46 PP1V8_EXT SW == =PP1V8_VDDIO18_SOC 8 9
MAKE_BASE=TRUE == =PP1V8_SOC 4 5 7 10 18
== =PP1V8_MIPI_SOC 7
== =PP1V8_EDP_SOC 7
== =PP1V8_NAND_SOC 6
== =PP1V8_NAND 12 48
== =PP1V8_PLL_SOC 4
== =PP1V8_SPKRAMP
== =PP1V8_EEPROM 51
== =PP1V8_BEACON

PP1V8_SW2

52 46 PP1V8_SW2 == =PP1V8_GRAPE 13
MAKE_BASE=TRUE

PP1V8_S2R_SW3

46 PP1V8_S2R_SW3 == =PP1V8_S2R_GYRO 21
MAKE_BASE=TRUE == =PP1V8_S2R_ACCEL 21
== =PP1V8_S2R OSCAR 19

PP1V8_S2R_SW3 COMP

54 52 PP1V8_S2R_SW3 COMP == =PP1V8_S2R COMP 21
MAKE_BASE=TRUE

PP1V8_S2R_SW3 SHOULD BE ON IN HIBERNATE
CURRENTLY POWERS OSCAR AND 1.8V RAIL ON SENSOR

BUCK4

52 47 46 PP1V2_S2R == =PP1V2_S2R_DDR 8
MAKE_BASE=TRUE == =PP1V2_S2R_DDR_SOC 8
== =PP1V2_S2R_CAM_REAR

BUCK4_SW

52 46 PP1V2_SW1 == =PP1V2_VDDO_DDR 8
MAKE_BASE=TRUE == =PP1V2_VDDIOD_SOC 8
== =PP1V2_HSIC_SOC 4

PP1V2_S2R_SW2

52 46 PP1V2_S2R_SW2 == =PP1V2_S2R OSCAR 19
MAKE_BASE=TRUE
PP1V2_S2R_SW2 SHOULD BE ON IN HIBERNATE
PROVIDE 1.2V TO OSCAR

BUCK5

52 46 PPVDD_SRAM == =PPVDD_SRAM_CPU
MAKE_BASE=TRUE == =PPVDD_SRAM_SOC 9

BUCK6

52 46 PP3V3_S2R == =PP3V3_S2R_SWITCH 48
MAKE_BASE=TRUE == =PP3V3_S2R_WIFI_PA 44

PP3V3_SW

52 48 PP3V3_SW == =PP3V3_EDP_PU
MAKE_BASE=TRUE == =PP3V3_NAND 12
== =PP3V3_USB_SOC 4

LDO1

52 47 PP3V0_SPARE1 == =PP3V0_SPARE1 49
MAKE_BASE=TRUE

LDO2

52 47 16 PP1V7_VA_VCP == =PP1V7_VA_VCP 15 16
MAKE_BASE=TRUE

LDO3

LDO3 SHOULD BE ON IN HIBERNATE
COMPASS, ACCEL, GYRO, PROX ARE ON OSCAR
HALL EFFECT NEEDS TO BE ON IN HIBERNATE
52 47 PP3V0_S2R_SENSOR == =PP3V0_S2R_HALL 13
MAKE_BASE=TRUE == =PP3V0_S2R_GYRO 21
== =PP3V0_S2R_ACCEL 21
== =PP3V0_S2R_COMP 21

LDO4

52 47 PP3V0_ALS == =PP3V0_ALS 20
MAKE_BASE=TRUE == =PP3V0_PROX 22
== =PP3V0_HP_ALS
== =PP3V0_IO_ALS
SHOULD IO ALS POWER HERE?

LDO5

52 47 PP3V0_UVLO == =PP3V0_UVLO 49
MAKE_BASE=TRUE

LDO6

52 47 PP3V3_ACC == =PP3V3_ACC 11
MAKE_BASE=TRUE

LDO7

LDO7 SHOULD BE ON IN HIBERNATE
52 47 PP3V0_S2R_TRISTAR == =PP3V0_S2R_TRISTAR 11
MAKE_BASE=TRUE

LDO8

47 NC_LDO8 NO_TEST=TRUE == =NC_LDO8
MAKE_BASE=TRUE

LDO9

BACKUP RAIL. CAN BE BOOSTED TO MEET
1.1V MIN ON CAMERA IF NEEDED.
52 47 PP1V3_CAM == =PP1V3_CAM_FRONT
MAKE_BASE=TRUE == =PP1V3_CAM_REAR 23

LDO10

52 47 PP1V0_SOC == =PP1V0_USB_SOC 4
MAKE_BASE=TRUE == =PP1V0_MIPI_SOC 7
== =PP1V0_EDP_PAD_DVDD_SOC 7

LDO11

52 47 PP2V6_CAM_AF == =PP2V6_CAM_REAR_AF 23
MAKE_BASE=TRUE

LDO13

52 47 PP2V9_CAM == =PP2V9_CAM_FRONT 20
MAKE_BASE=TRUE == =PP2V9_CAM_REAR 23

VLCM1

47 PP5V25_GRAPE == =PP5V25_GRAPE 13
MAKE_BASE=TRUE

CHARGER MAIN

52 49 48 47 46 PPVCC_MAIN == =PPVCC_MAIN_AUDIO 15 16
MAKE_BASE=TRUE == =PPVCC_MAIN_LED 47
== =PPVCC_MAIN_DOCK 43
== =PPVCC_MAIN_DEV
== =PPVCC_MAIN_CPU 46
== =PPVCC_MAIN_GPU 46
== =PPVCC_MAIN_SOC 46
== =PPVCC_MAIN_GRAPE 13
== =PPVCC_MAIN_LCD 18
== =PPVCC_MAIN_NAVAJO 47
== =PPVCC_MAIN_VDD_LCM 44
== =PPVCC_MAIN_WLAN
== =PPVCC_MAIN_GPS

BATTERY

52 46 PPBATT_VCC == =PPBATT_POS_CONN 45
MAKE_BASE=TRUE == =PPBATT_VCC_BB 24 25 33 34 35 36 37 38
== =PPBATT_AUDIO

USB POWER INPUT


52 46 PPVBUS_USB_DCIN == =PPVBUS_USB_EMI 43
MAKE_BASE=TRUE

ON_BUF

52 47 PP1V8_ALWAYS == =PP1V8_ALWAYS 5
MAKE_BASE=TRUE

BACKLIGHT BOOST

52 47 PPLED_OUT_A == =PPLED_REG_A 18
MAKE_BASE=TRUE

SYNC MASTER=J72 MLB C		SYNC DATE=11/26/2012	
PAGE TITLE			
POWER: ALIASES			
	Apple Inc.	DRAWING NUMBER	SIZE
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		121 OF 121	
		SHEET	
		54 OF 54	