<Variant Name>

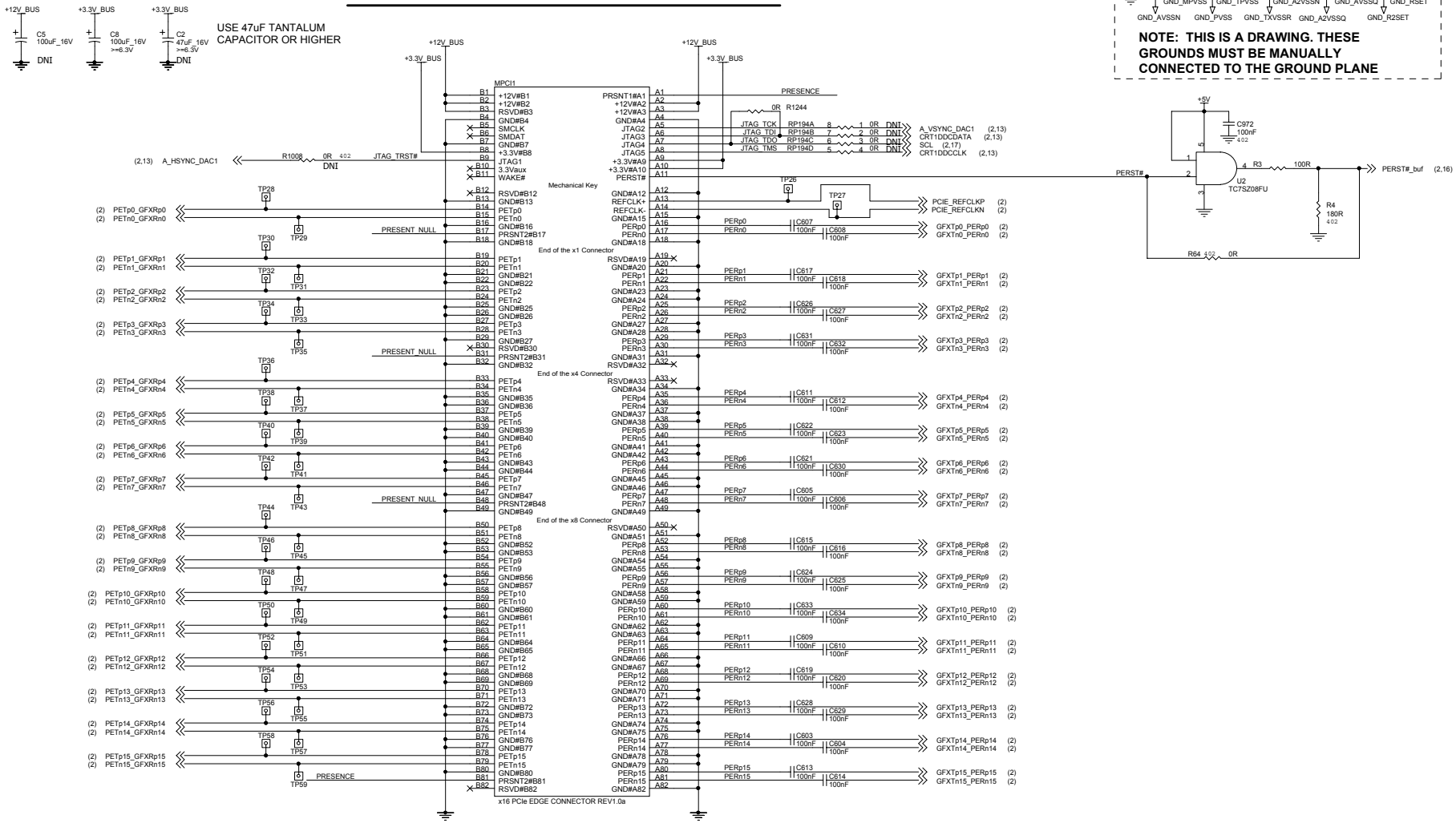
Title	Schematic No.	Date:
PCI-E RV380/370 256M pterm TSOP V-VV-DI	105-A334xx-00C	**Tuesday, March 16, 2004**

REVISION HISTORY

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
		11-24-03	PRELIMINARY BASED ON 105-A297xx-00A 03-11-24 - (pg 02) Swap DVI DDC clock and data lines
1	00B	12-29-03	- (pg 07) Add R1043 for power dissipation - (Layout) Move C284, blocking Grantsdale PCIE connector latch
2	00C	03-09-04	- (Layout) Move fan connector to shorten fan power wire - (Layout) Correct C151 overlap - (pg02) Fix pull-up +VDD_DVO to +VDDR4 - (pg04) Remove CP2, 3, 4, 5, 6 and 8 for dual footprint manufacturing issues (Capacitor packs sharing with 402 footprints) - (pg05) Remove dual-package FET for VDDC - (pg06) Remove C986, C987, C988, C989, C990, C991, C992 and C993) - (pg06) Change R297 to 1206 footprint - (pg07) Add MC917 as multi-footprint for C917, remove L3 (redundant option) - (pg13, 15) +5V supply with current limiting for VESA DDC spec, remove F1, B21

PCI-EXPRESS EDGE CONNECTOR



NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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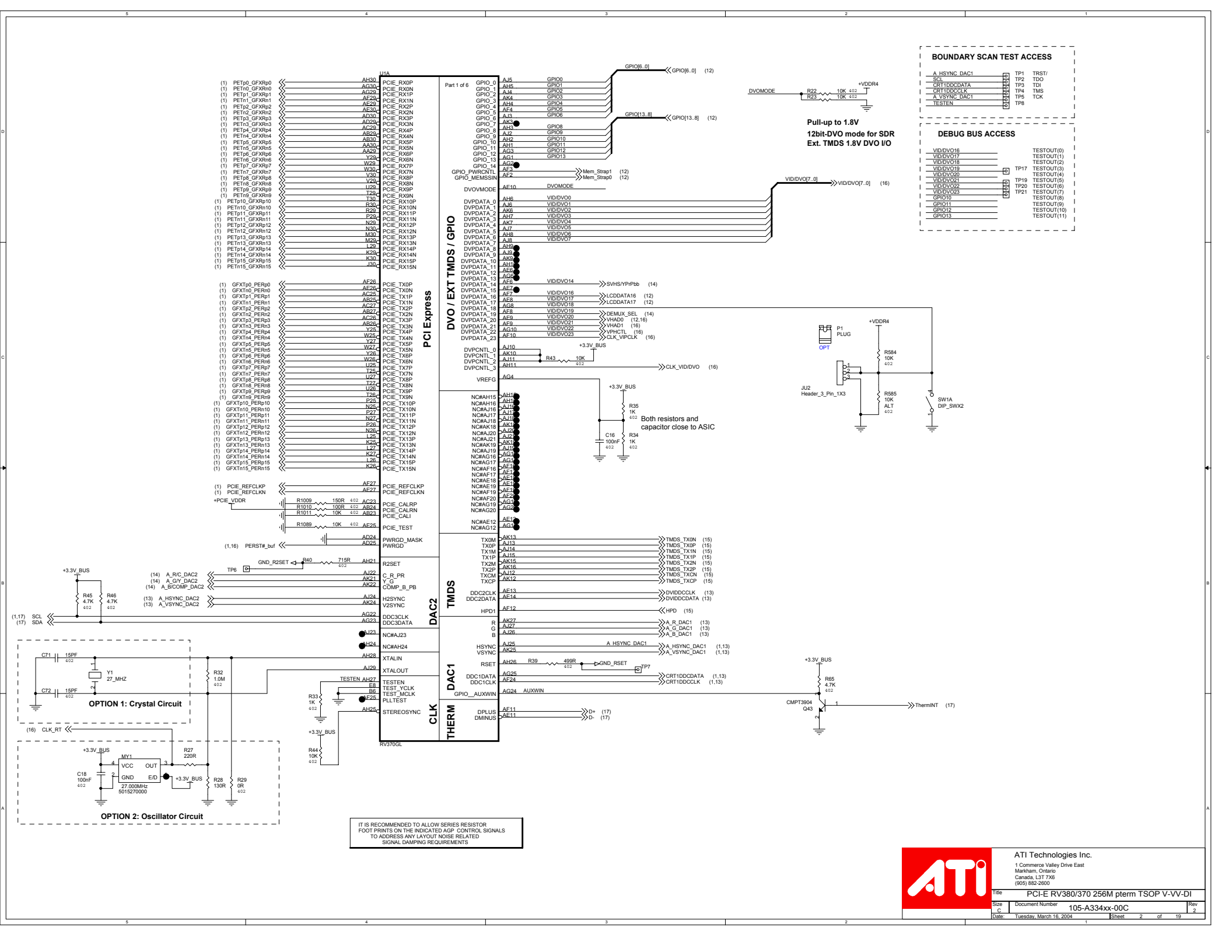
U1A
Part 1 of 6
PCI Express
DVO / EXT TMDS / GPIO
TMDS
DAC2
DAC1
CLK
THERM
RV370GL
BOUNDARY SCAN TEST ACCESS
DEBUG BUS ACCESS
Pull-up to 1.8V
12bit-DVO mode for SDR
Ext. TMDS 1.8V DVO I/O
Both resistors and capacitor close to ASIC
OPTION 1: Crystal Circuit
OPTION 2: Oscillator Circuit
IT IS RECOMMENDED TO ALLOW SERIES RESISTOR FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS TO ADDRESS ANY LAYOUT NOISE RELATED SIGNAL DAMPING REQUIREMENTS
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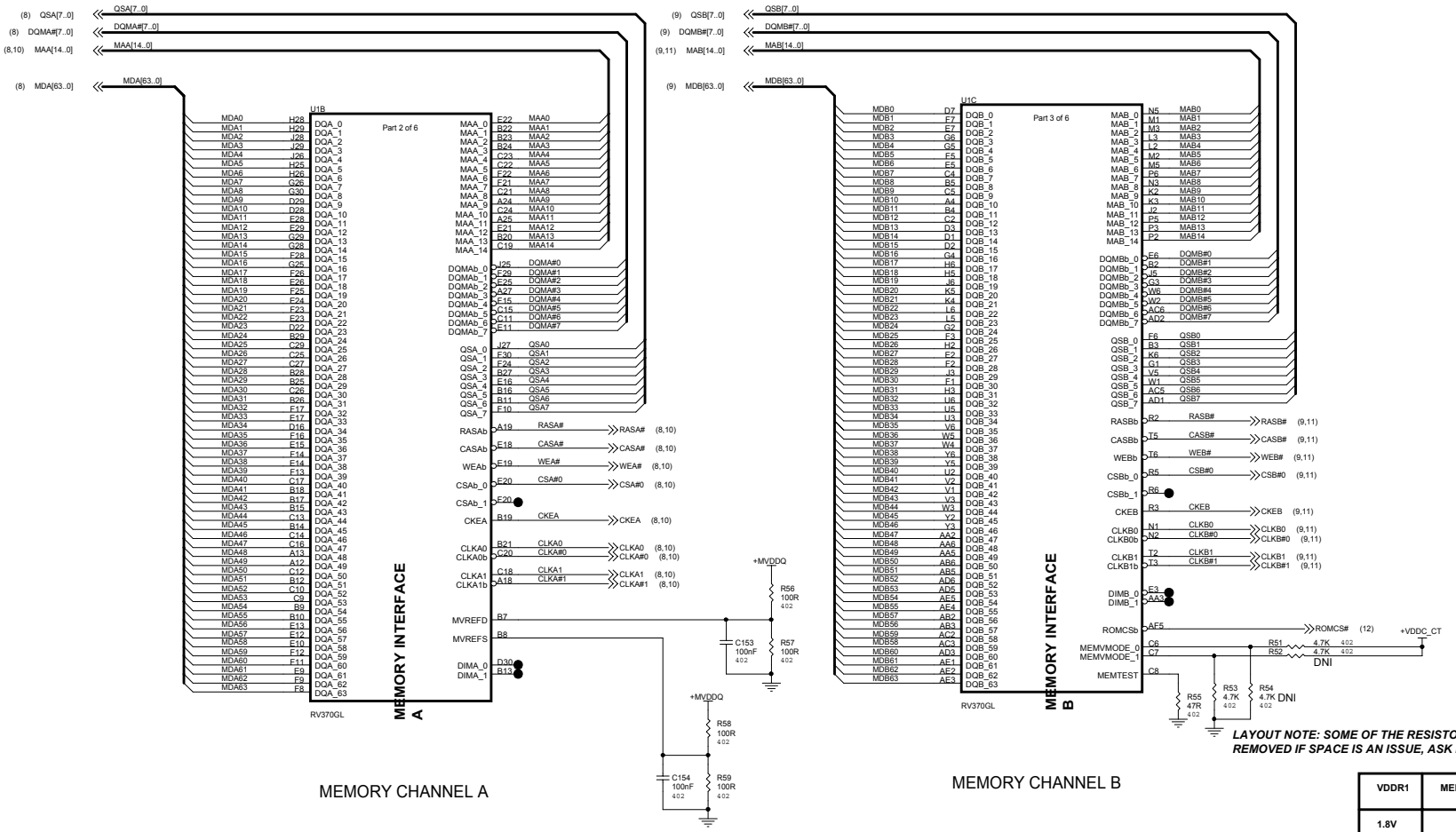

MEMORY CHANNEL A

MEMORY CHANNEL B

PLACE C351/152 VERY CLOSE TO ASIC
R56/57/58/59 CLOSE TO ASIC AS WELL

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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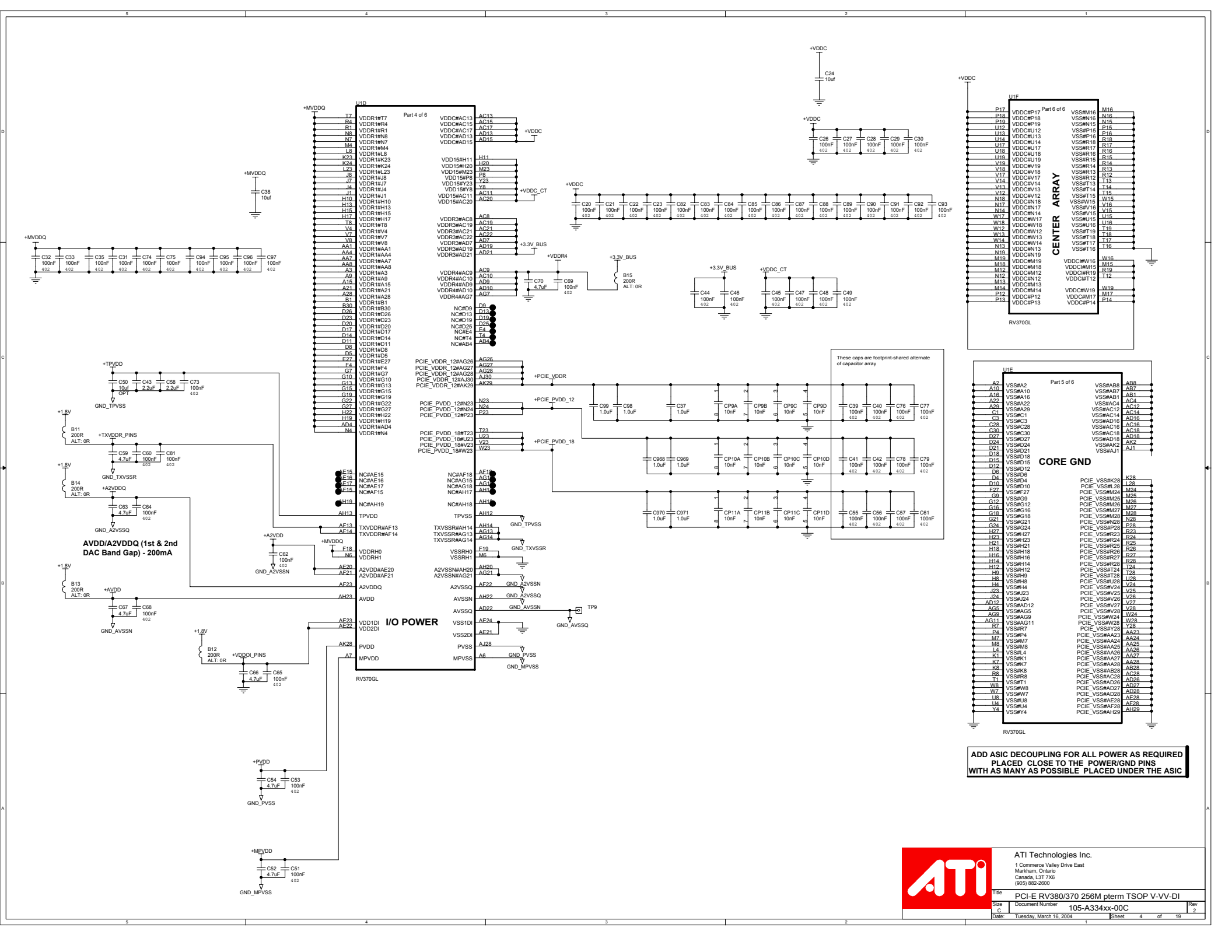
U1D
Part 4 of 6
I/O POWER
RV370GL
U1F
Part 6 of 6
CENTER ARRAY
RV370GL
U1E
Part 5 of 6
CORE GND
RV370GL
These caps are footprint-shared alternate of capacitor array
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED PLACED CLOSE TO THE POWER/GND PINS WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
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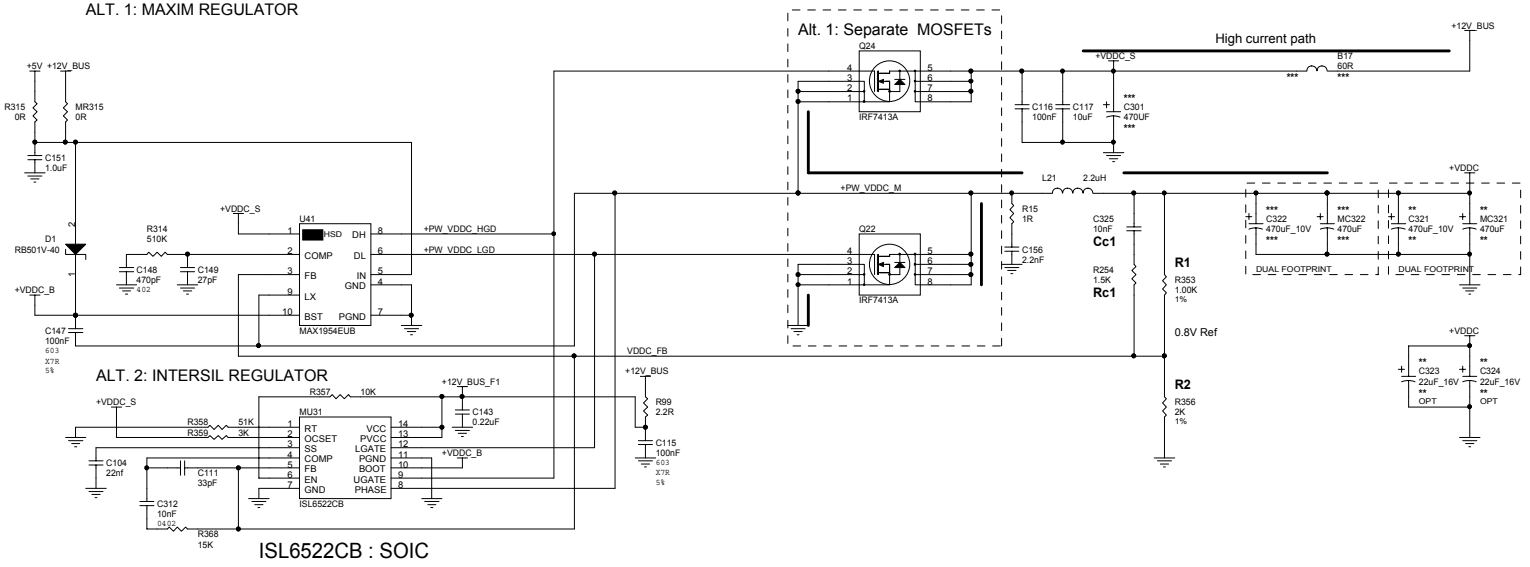
Regulator for VDDC (ASIC Core)

Vout = 1.2V ~ 1.3V

ALT. 1: MAXIM REGULATOR

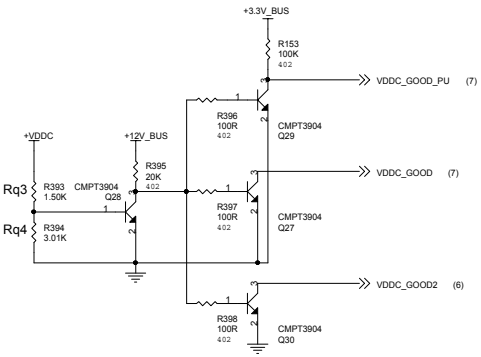


ALT. 2: INTERSIL REGULATOR

ISL6522CB : SOIC

Part	NOTES
MAX1954	Do not install Cc1, Rc1
ISL6522	Install Cc1, Rc1

Part	Vout	R1	R2
MAX1954 ISL6522	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
0.8V Ref	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100



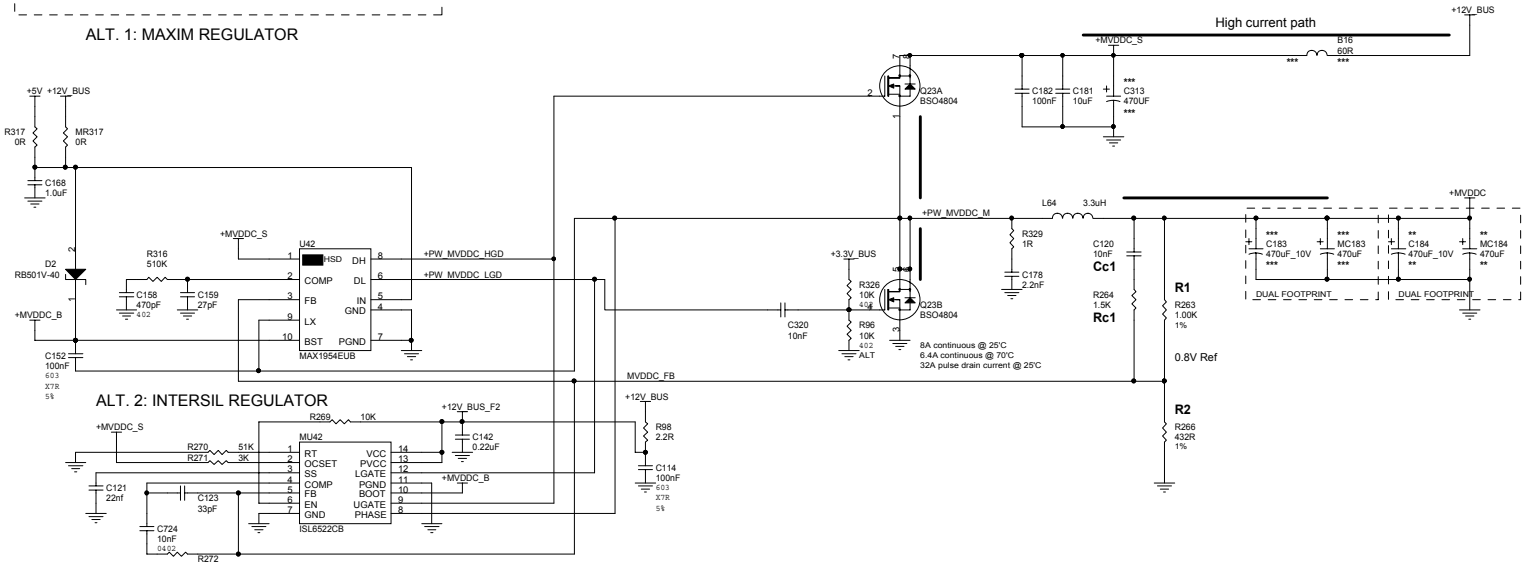
+VDDC	Rq3	Rq4
+1.3V	1.5K	2.4K
+1.2V	1.5K	3K

Circuit to hold PCI-E voltage low and wait for +VDDC for proper power sequence

Regulator for MVDDC (Memory Core)

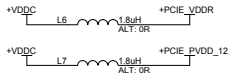
Vout = 2.5V ~ 3.3V

ALT. 1: MAXIM REGULATOR



ALT. 2: INTERSIL REGULATOR

ISL6522CB : SOIC



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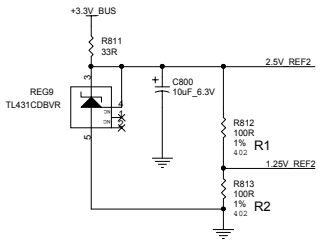
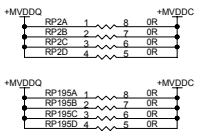
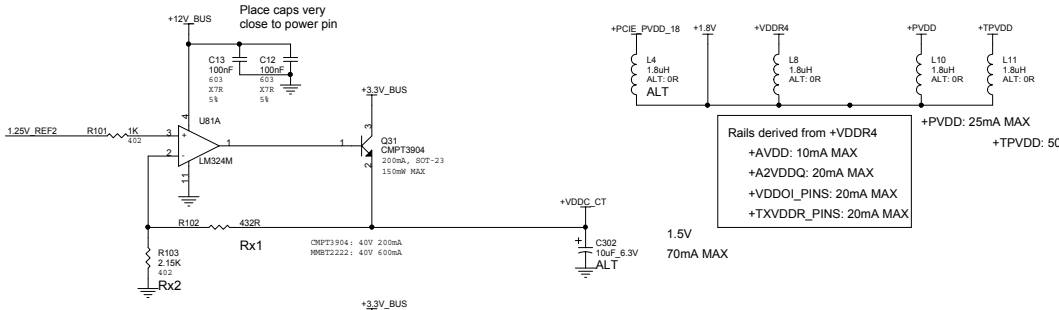


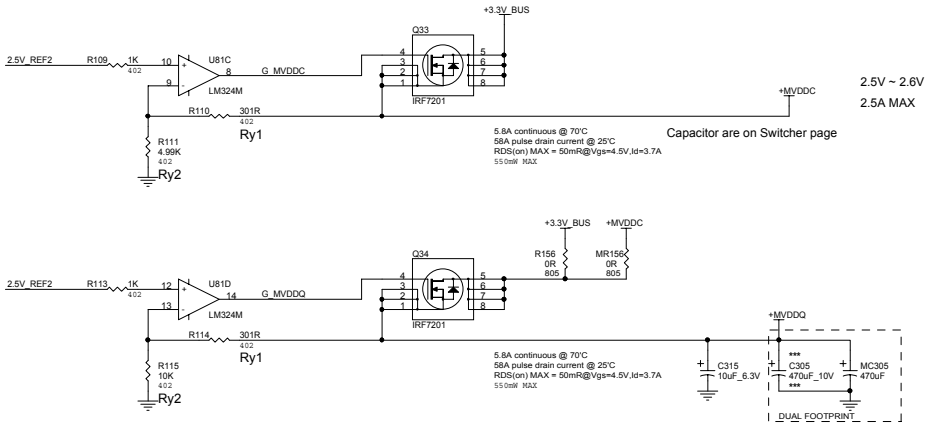
Voltage Req.	R1	R2
0.8V	150R P/N 3160150000 402	71.5R P/N 324075R500
1.25V	100R P/N 3160100000 402	100R P/N 3160100000 402
1.5V	100R P/N 3160100000 402	150R P/N 3160150000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240015200

Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.5V	0R P/N 3230000000 603 P/N 3150000000 402	DNI

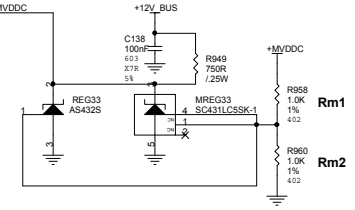






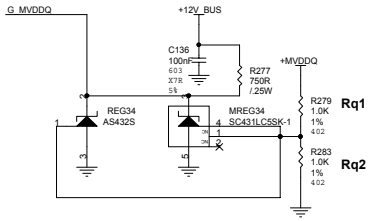
Alt. regulator for +MVDDC
Vout = 2.5V ~ 2.6V
Iout = 500mA MAX

Voltage Req.	Rm1	Rm2
3.34V [-0.04V/+0.04V]	4.32K	2.55K
3.45V [-0.04V/+0.04V]	4.32K	2.43K
2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100



Alt regulator for +MVDDQ
Vout = 2.5V ~ 2.6V
Iout = 200mA MAX

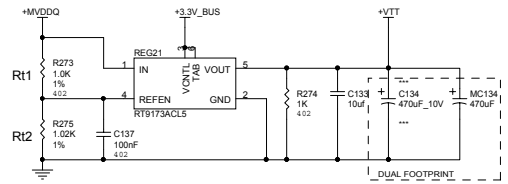
Voltage Req.	Rq1	Rq2
1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
2.5V	1K 3240100100	1K 3240100100
2.6V	4.75K 3240475100	4.32K 3240432100



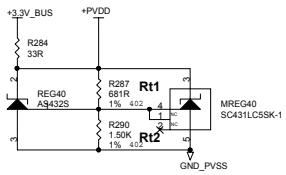
	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100

Regulator for +VTT (Termination)
Vout = 1.25V ~ 1.3V with +2.5V +MVDDQ
Iout = 1000mA MAX

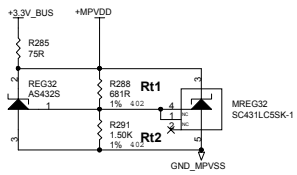
+MVDDQ = +2.5V	Rt1	Rt2
1.25V	1K 3240100100	1K 3240100100
1.3V	1.0K 3240100100 603 3160100100 402	1.02K 3240102100



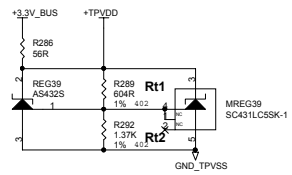
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



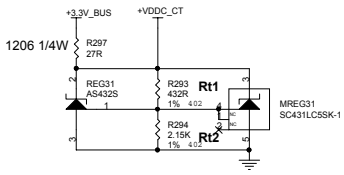
Alt regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX



Alt. regulator for +TPVDD
Vout = 1.65V ~ 1.85V
Iout = 20mA MAX



Alt regulator for +VDDC_CT
Vout = 1.5V
Iout = 70mA MAX



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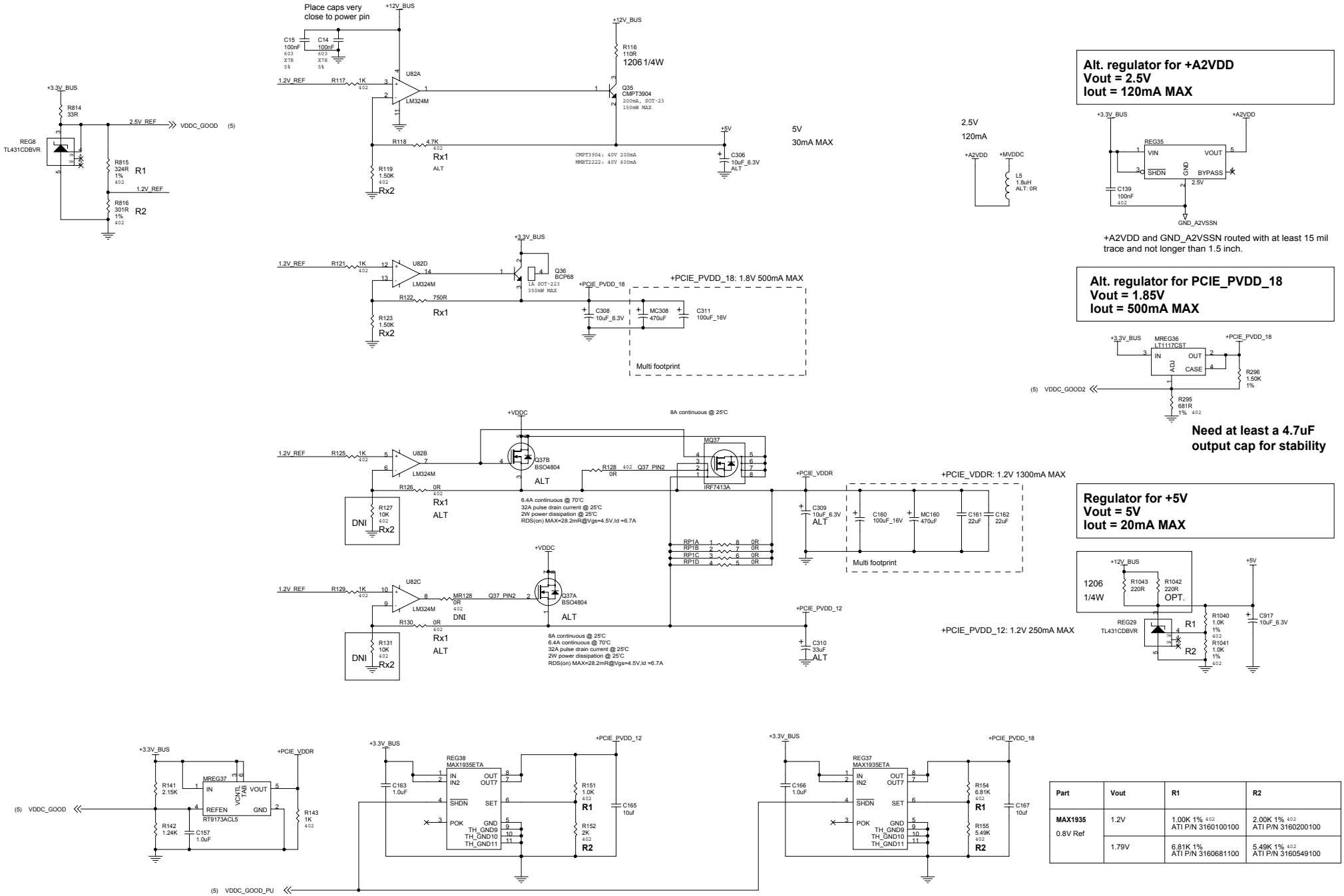

Part	Vout	R1	R2
MAX1935 0.8V Ref	1.2V	1.00K 1% 402 ATI P/N 3160100100	2.00K 1% 402 ATI P/N 3160200100
	1.79V	6.81K 1% ATI P/N 3160681100	5.49K 1% 402 ATI P/N 3160549100

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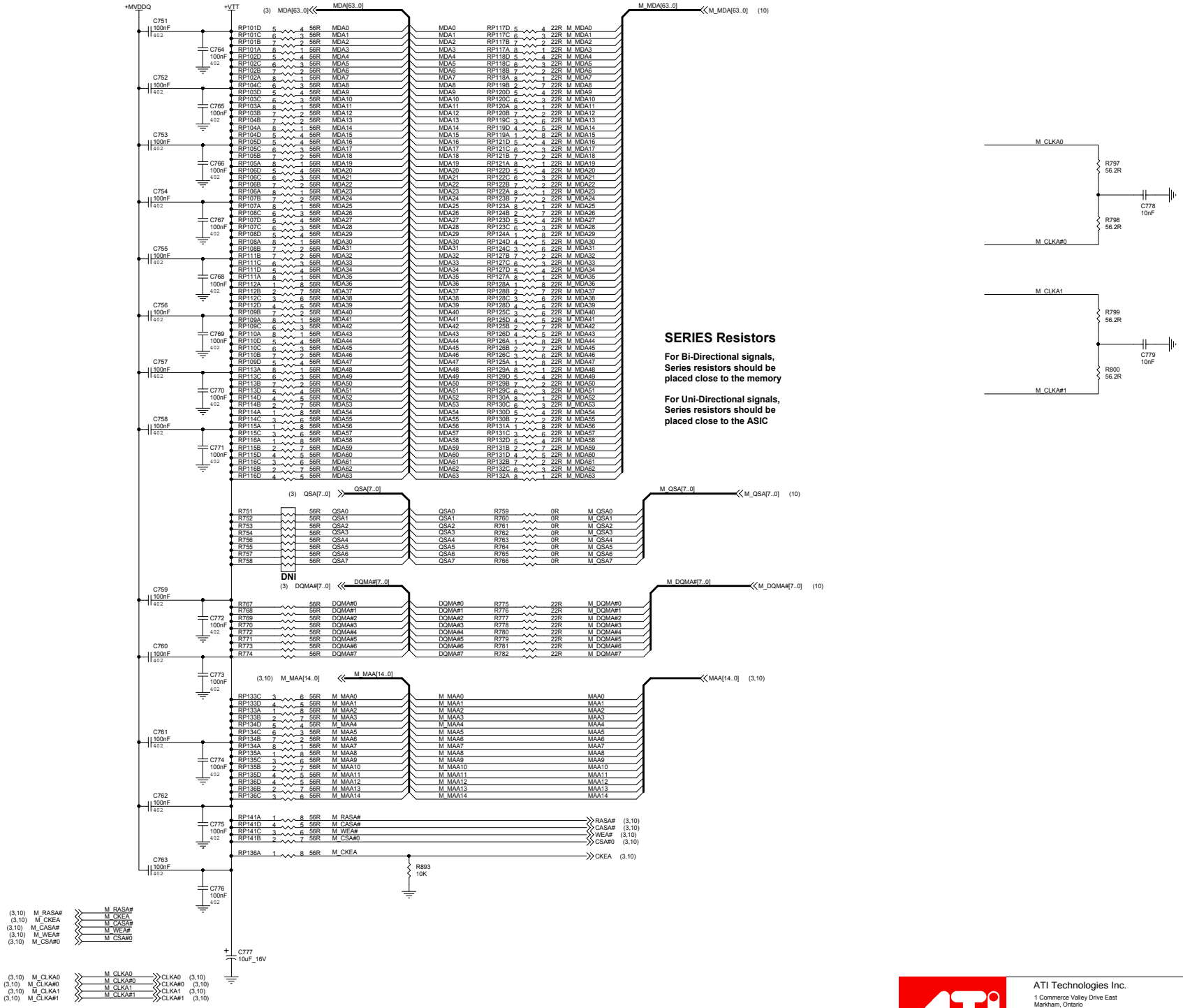

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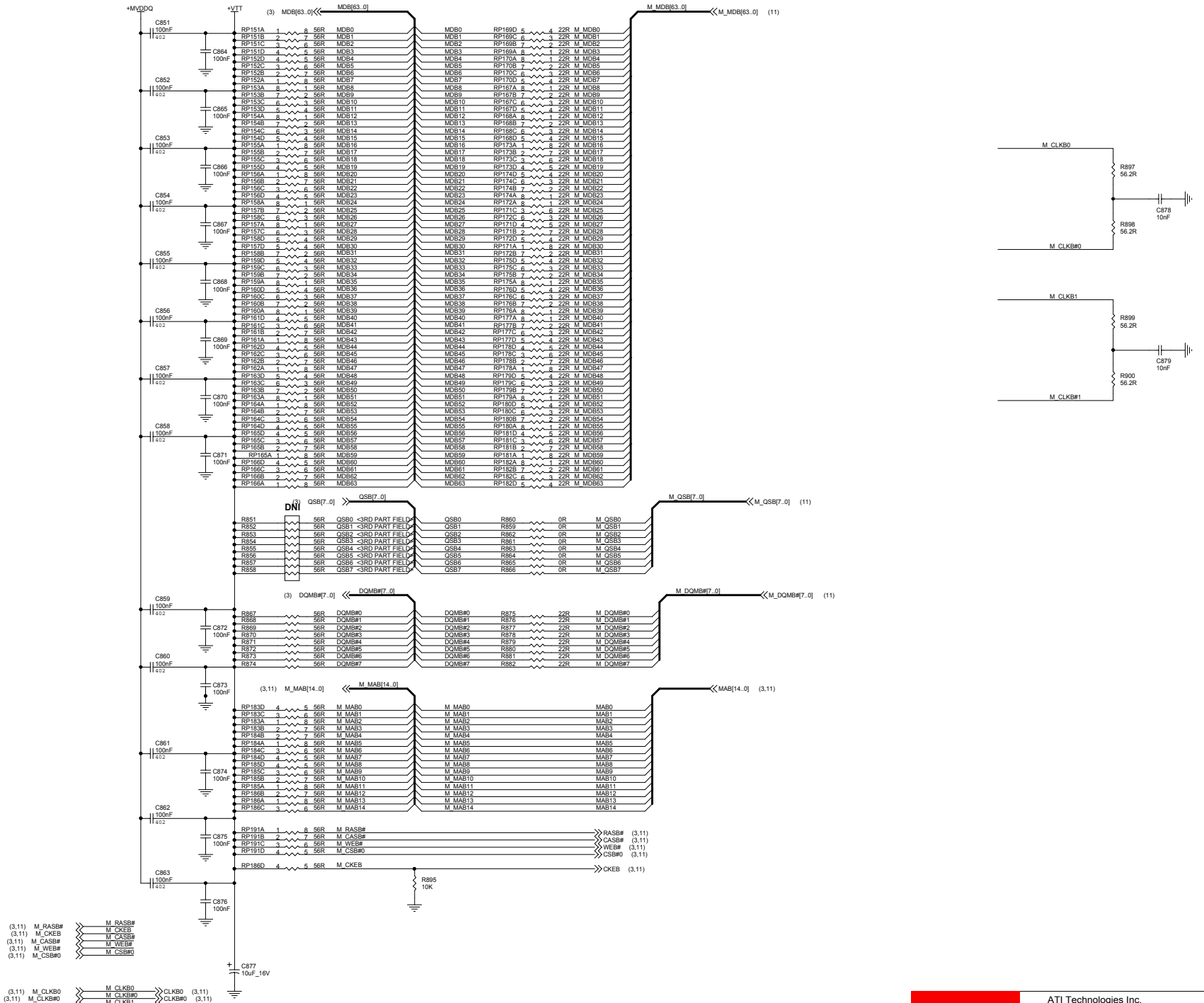

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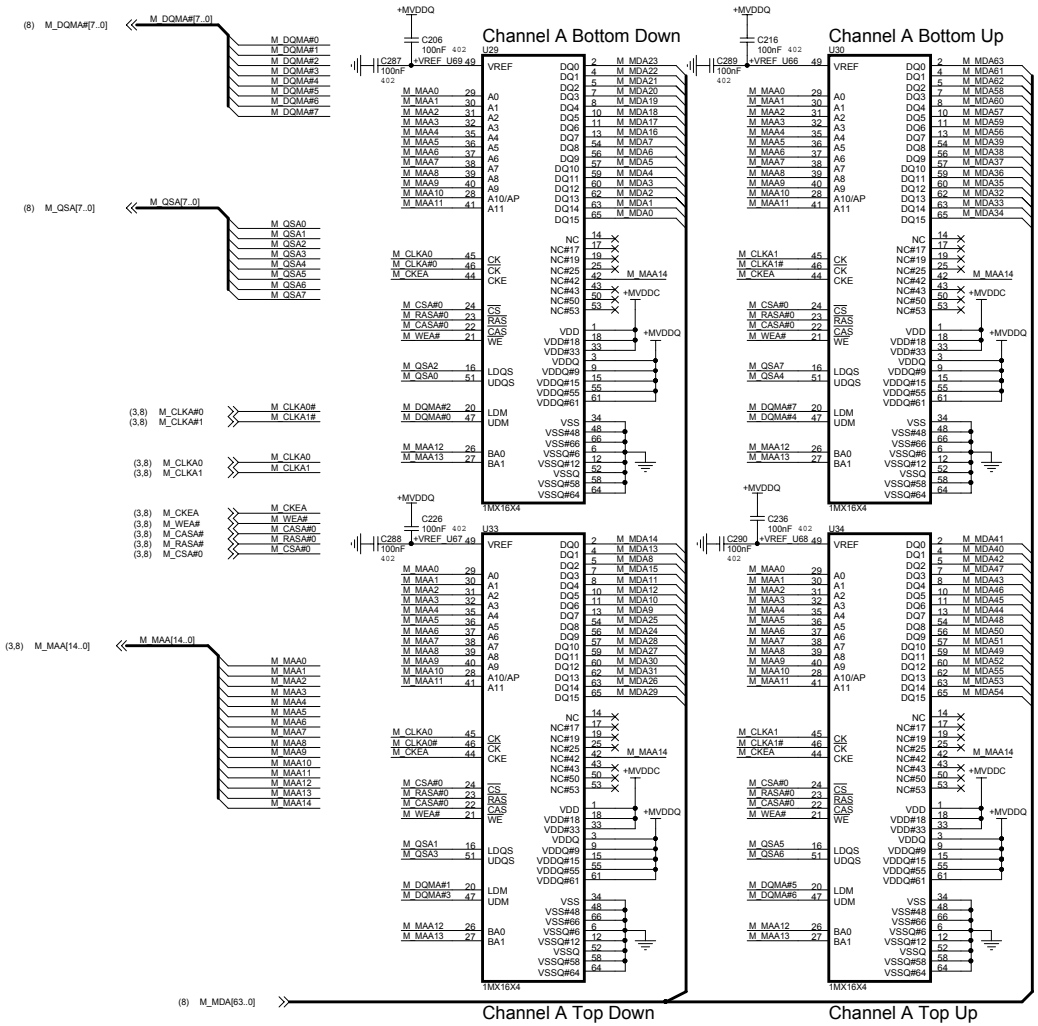
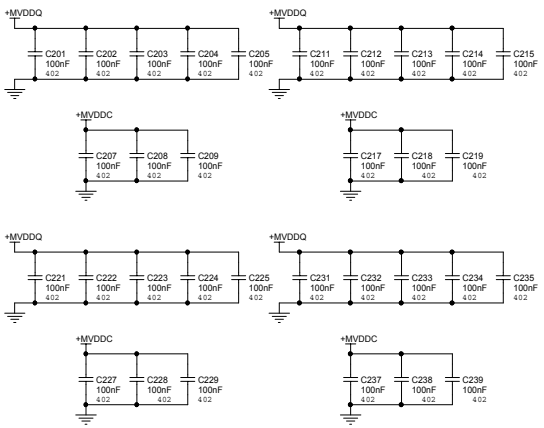
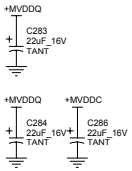
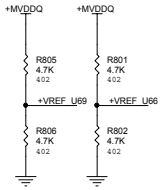
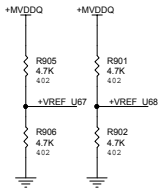


Put 1 1uF cap per power pin of memory









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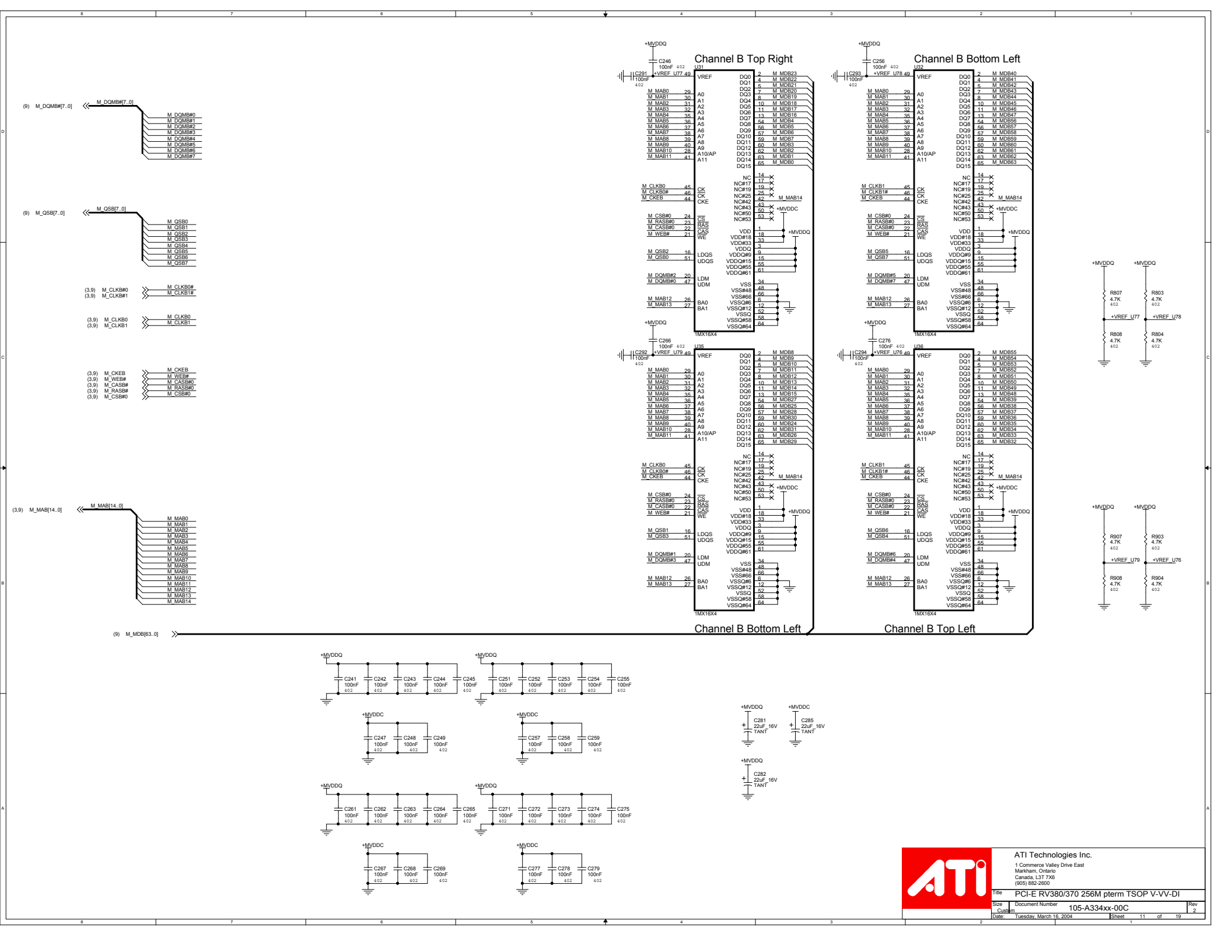
Channel B Top Right
Channel B Bottom Left
Channel B Top Left
Channel B Bottom Right
M_DQMB#[7..0]
M_QSB[7..0]
M_CLKB#0
M_CLKB#1
M_CLKB0
M_CLKB1
M_CKEB
M_WEB#
M_CASB#
M_RASB#
M_CSB#0
M_MAB[14..0]
M_MDB[63..0]
+MVDDQ
+MVDDC
+VREF_U77
+VREF_U78
+VREF_U79
+VREF_U76
1MX16X4
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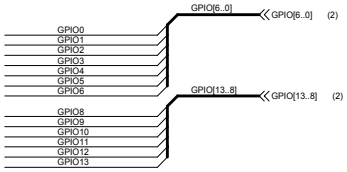
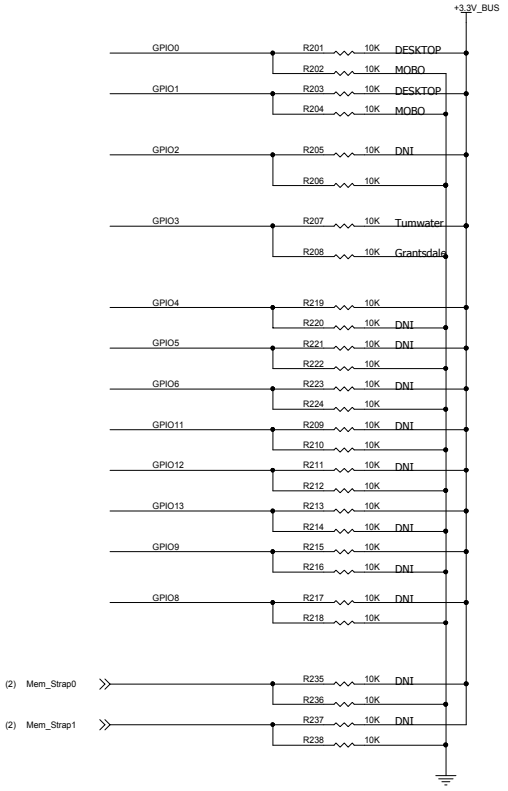
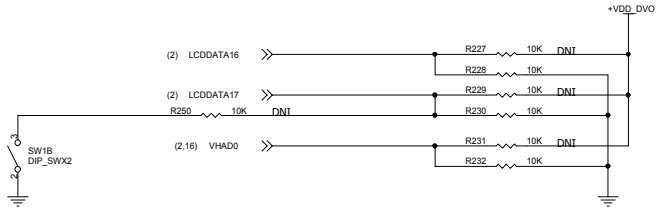
OPTION STRAPS





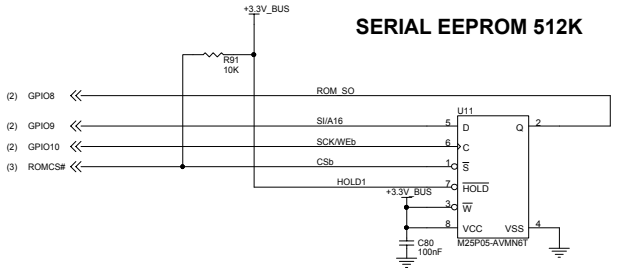


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K



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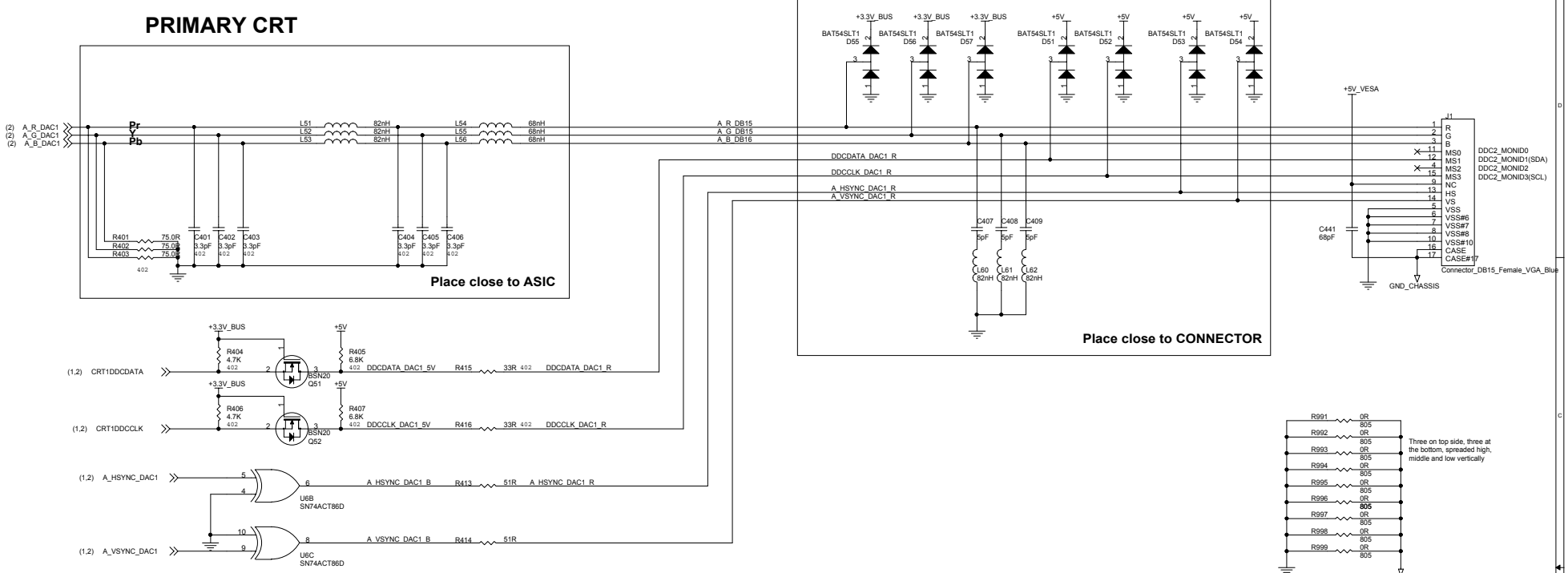
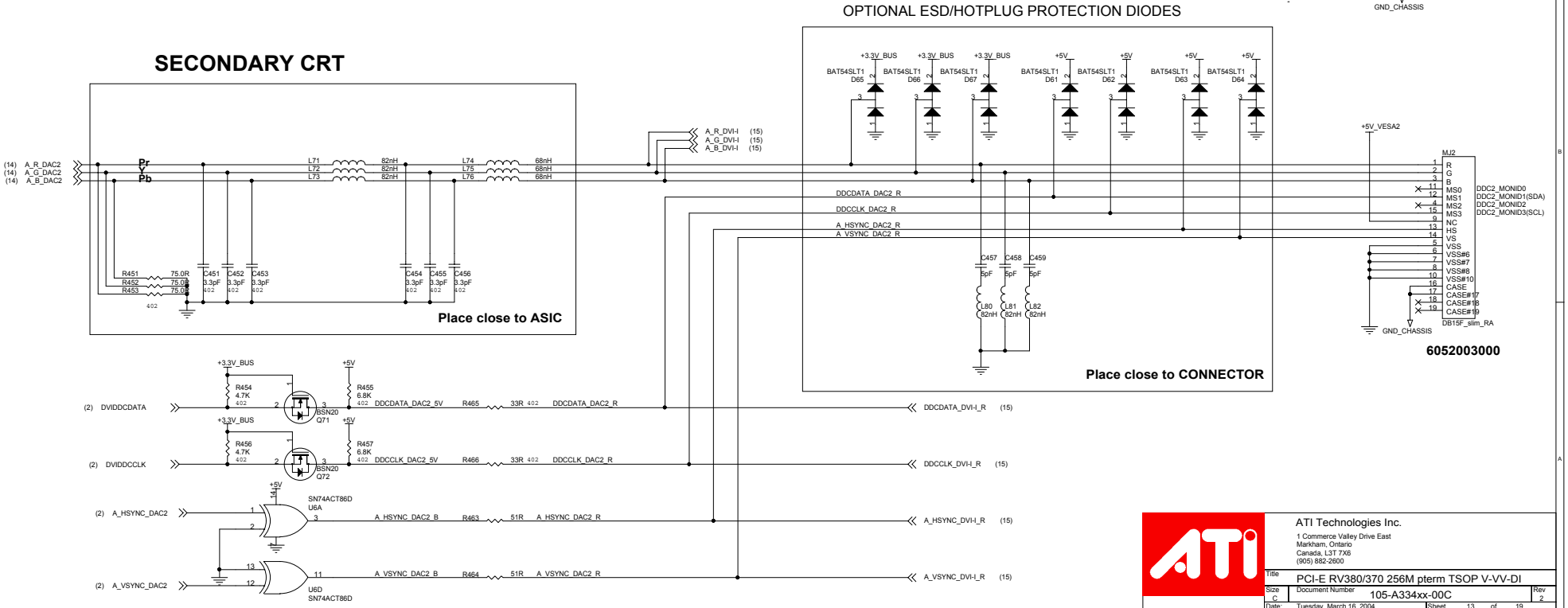
PRIMARY CRT



SECONDARY CRT



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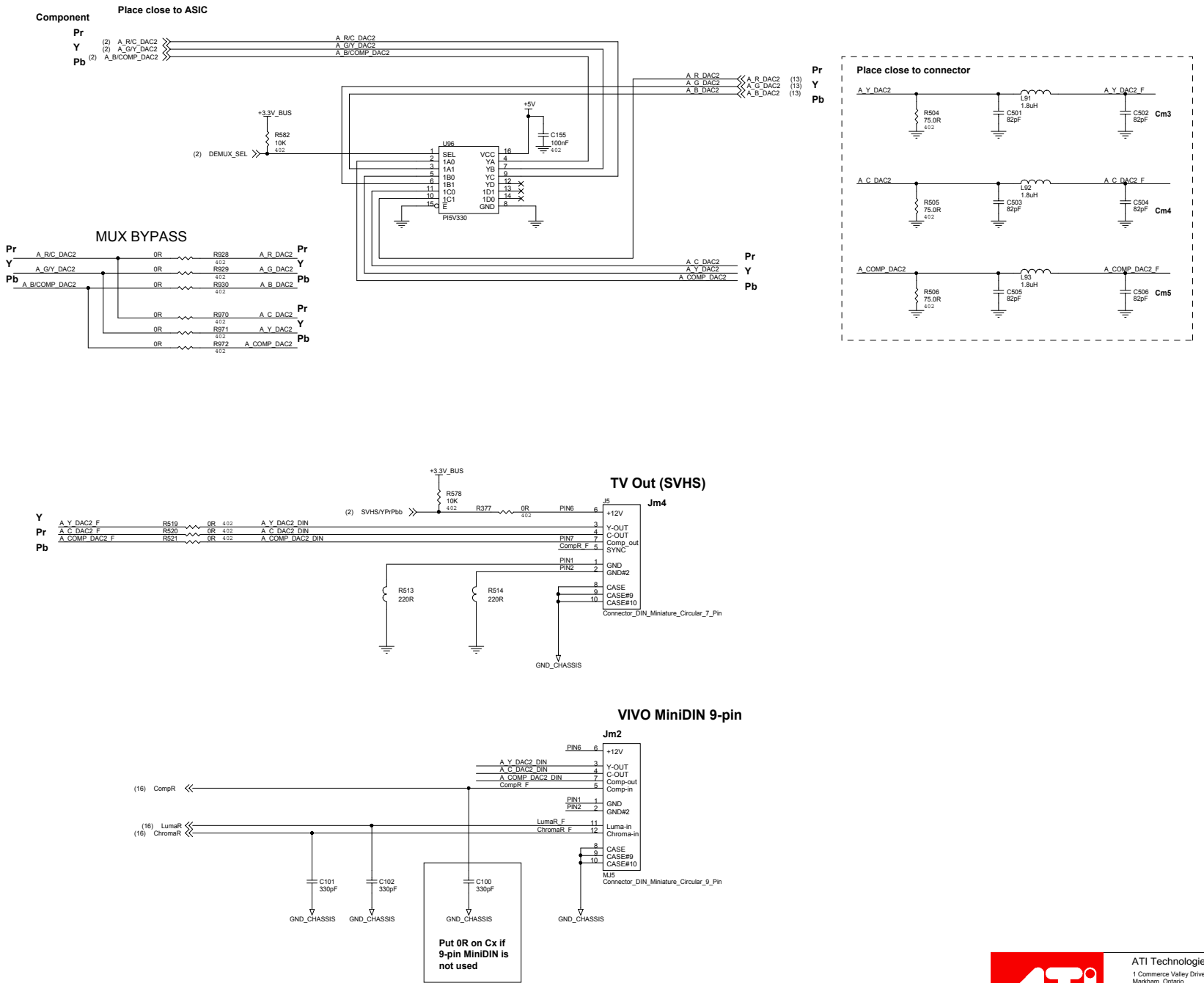

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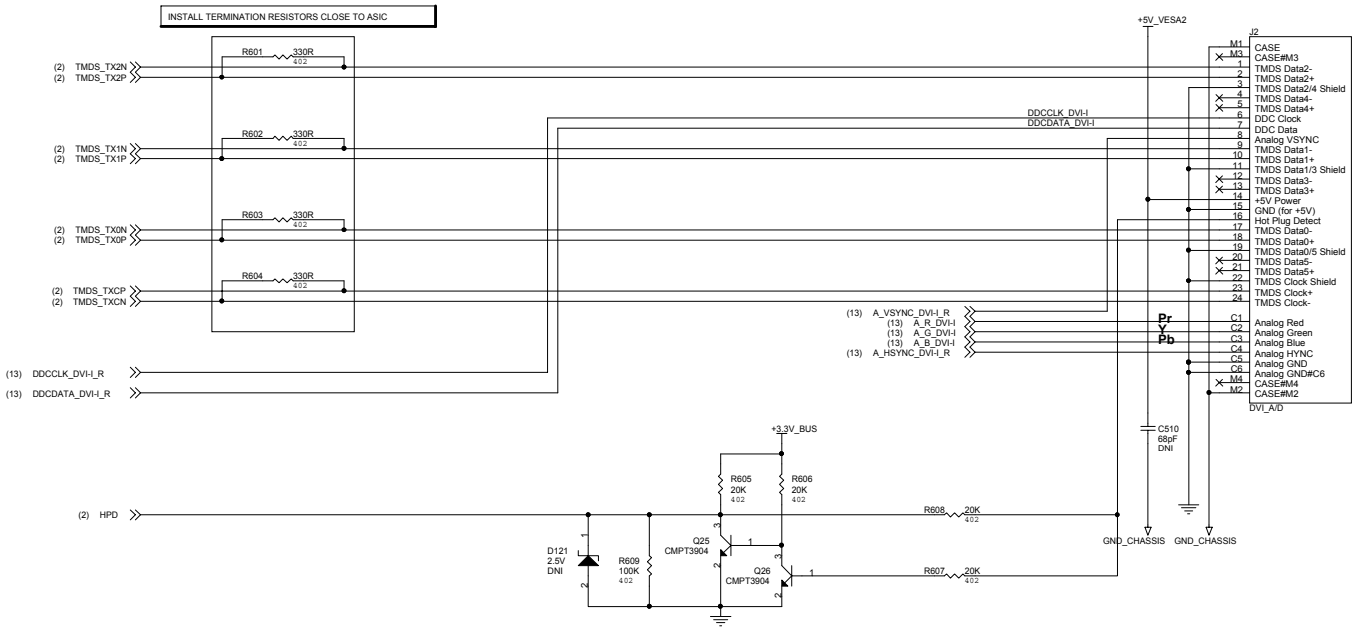
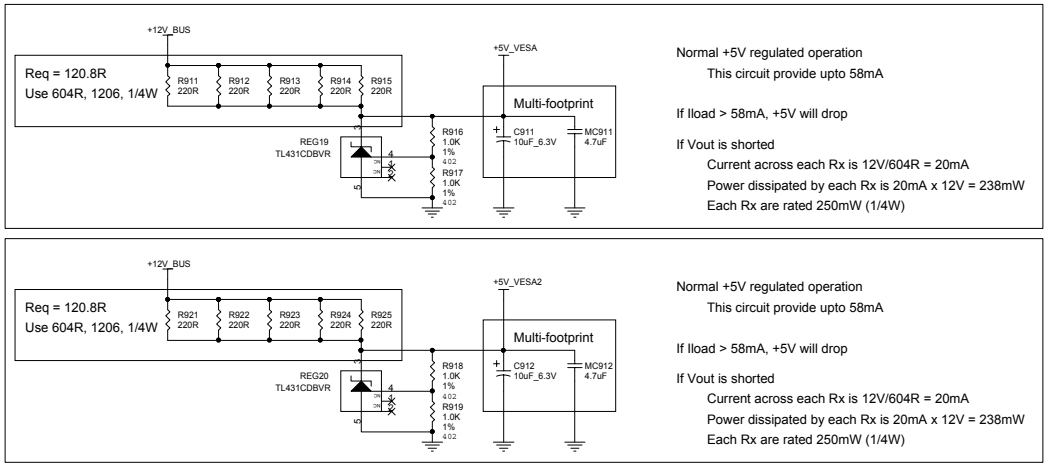
PRIMARY DVI-I CONNECTOR





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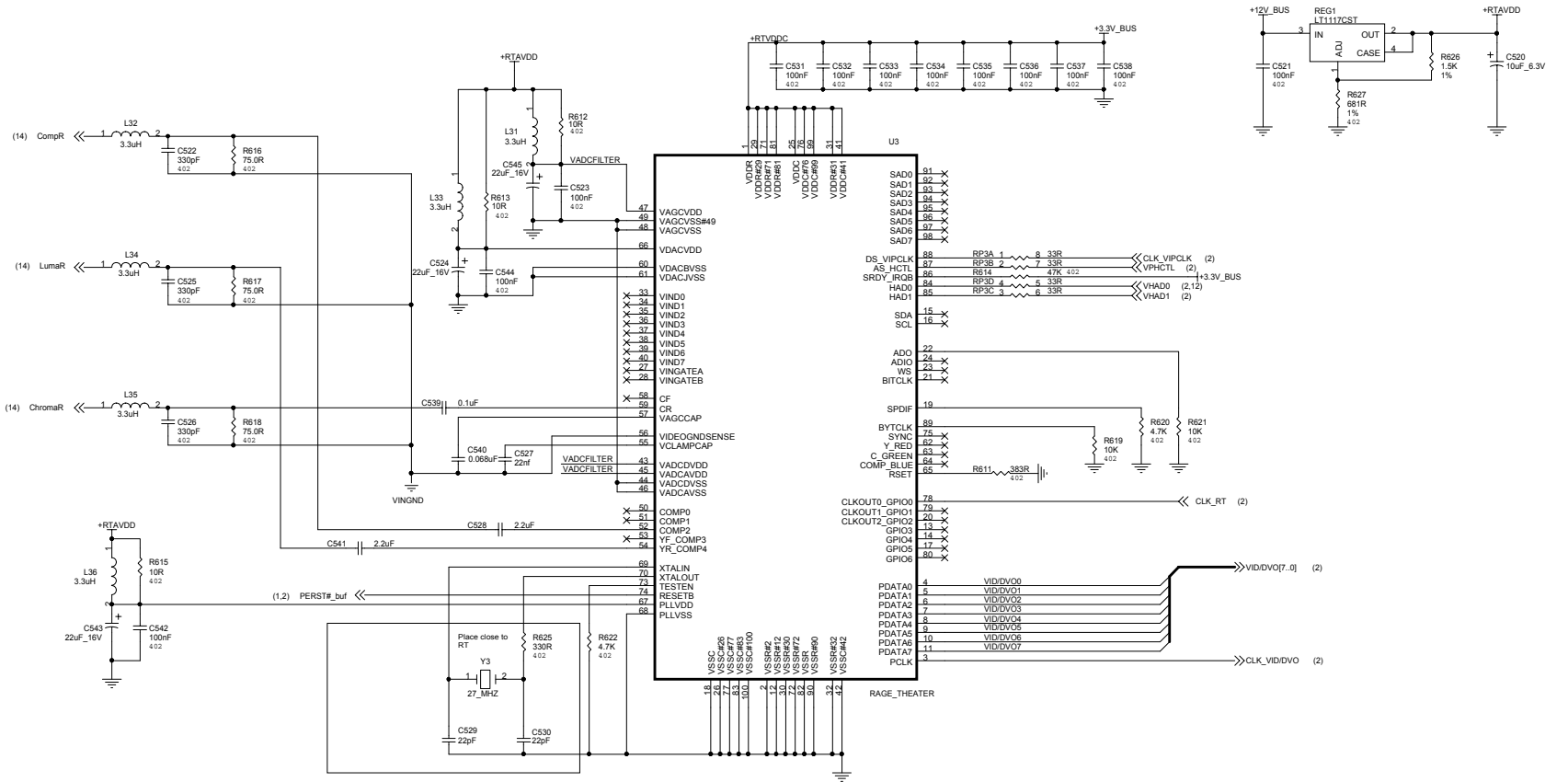
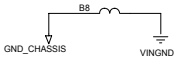
+RTAVDD
Vout = 3.3V
Iout = 125mA MAX, 80mA RMS



Footprint can be replaced with zero ohm or other.



IMPORTANT

Put 2D line as close as possible to pin 56 of Rage Theater

Layout Guide line of THEATER

#1 : C27 and C28 have to be placed as close as possible to the respective pins of Rage THEATER

#2 : VINGND should be seperated from Digital or Chassis Ground and have no loops

#3 : VINGND should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

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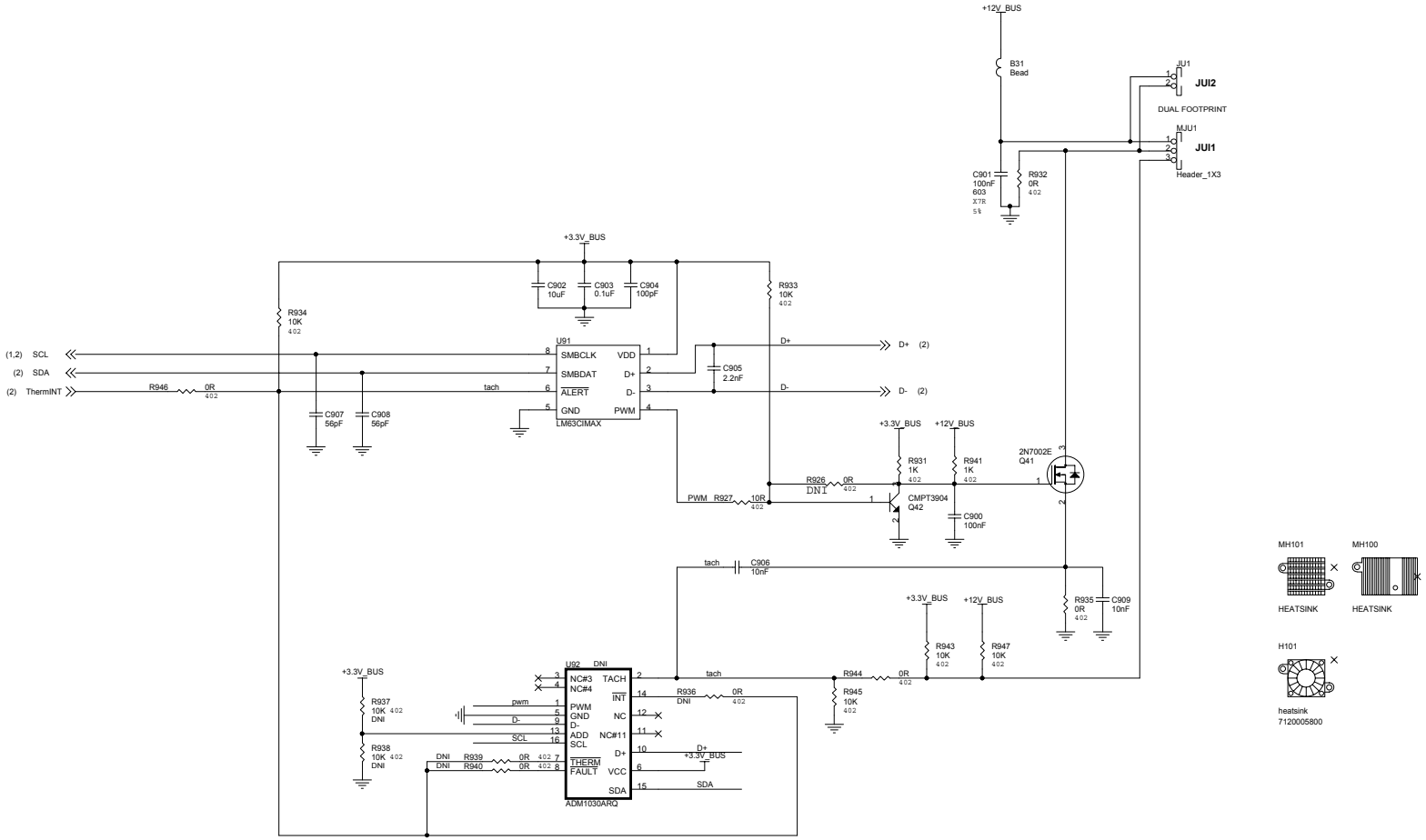
TEMPERATURE SENSE AND SPEED CONTROLLED FAN



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ASSY1
SCREW
JACKSCREW

ASSY2
SCREW
JACKSCREW

ASSY3
SCREW
JACKSCREW

ASSY4
SCREW
JACKSCREW

MISC. BOARD PARTS

ASSY7
ANTISTATIC
BAG
6_X_11

REF5
ATI LOGO
LABEL
ATI_LOGO_LABEL

ASSY8
BLANK
LABEL

ASSY10
BRACKET
DVI, DIN, VGA

ASSY12
BRACKET
8020037100
SV-VO-V
Slim VGA, DIN, VGA, 347
8020034700

ASSY11
BRACKET
80200370A0
DI-V
DVI, DIN, VGA

ASSY13
BRACKET
80200371A0
SV-V
Slim VGA, DIN, VGA, 347

MT1
MT_Hole_0.136_in.
GND_CHASSIS

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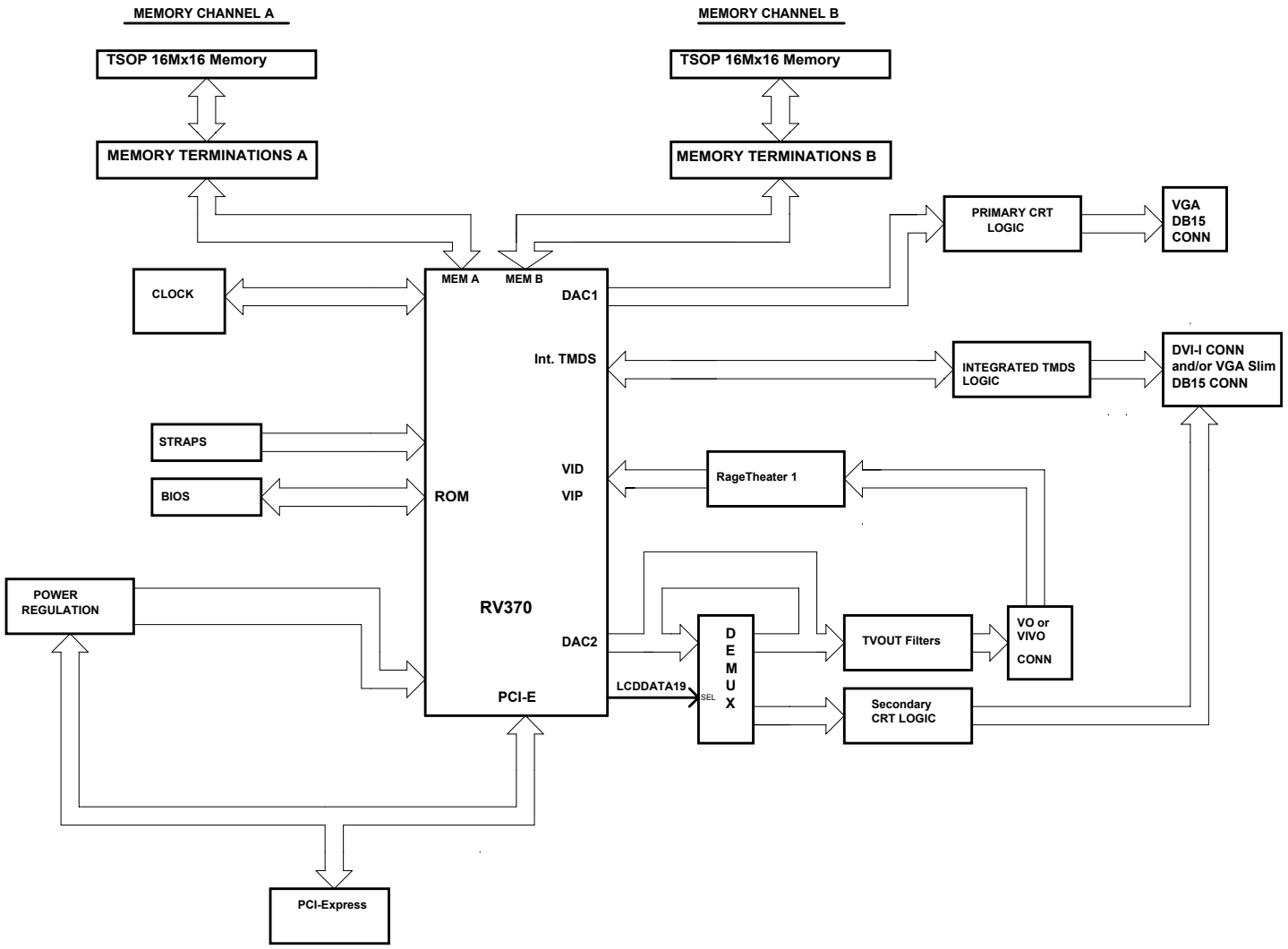

REFERENCE DESIGN

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