P78, NV17, 4Mx32 DDR, 64MB, RGB, TV-out, AGP4X

PCI DEVICE ID = 0X171 FOR NV17-128D.

PRIMARY ** VGA1 DAC A ** LFH1 TMDS A I2C_A
SECONDARY ** S-VIDEO/TV-OUT DAC B ** LFH2 VGA2 TMDS B I2C_B
VIDCAP ** VIP 7113 I2C_C.
9pin DIN ** RGB2 I2C_C.

X01: P78-A00
New file Created P71-X39+memory of P75 and new Mem PS

X02: P78-A00
Memory Address bus termination removed

X03: P78-A00
Cleanup- Design Review updates

X04: P78-A00
Mem Data/DQM bus Swapped on 11/14/01

X05: P78-A00
IFP PLLVDD REGULATOR ADDED
FBBCLK0 and 1 interchanged

X06: P78-A00
Memory U201/U203
Mem clock Pullups not required-R243 to R250 removed.
MVREF res package changed from 0603 to 0402 for R219,R220 to R222, R239 to R242
U201- nets FBD19,20,21 swapped

X07: P78-A00
For I2C-2 Pull up/Protection
R1033 to 1036(4 pcs), 0603 addeded
L602, L603 (2pcs), 0805 added.
C883,C884 (2pcs), 0603 added
D505, D506 (2pcs), sot23 added.

X08: P78-A00
Changed the power for GPU Frame buffer decaps. Should be FBVDDQ/FBVDD.
Deleted C868, C846 - TH part no space.
L602, L603- Package changed from 0805 to 0603.
GPU VDDDVO, C529, C530 AND DVOVREF TO 3.3V instead of A3.3V

X09: P78-A00
ADDED ONE MORE REGULATOR FOR IFP PLLVDD
C885, C886 -0805 ADDED
R1038,R1039-0402 ADDED
U825 ADDED
R1028, R1029, R1031, R1032 PACKAGE CHANGED TO 0402.

X10: P78-A00-Final Review
C419, C886 removed.-Not required

X11: P78-A00
R1040 Pull Down for Hotswap input added

X12: P78-A00
R616 added in series to Core switcher 12V input

X13: P78-A00
R201 AND C293 to be on FBVDD/Q instead of 3.3V

X14: P78-A00-PCB X-Released
Moved C618 CAP from 12V to 12V_IN

X15: P78-A00 -SCH X-Released
Memory Power R69 to support 2.8V or 2.5V Sku.
R69 CHANGED TO 154R FROM 150R FOR 2.8V
Bracket component added to SCH

NVVDD more comments added in PS sheet
Mem PScomments edited in PS sheet

X17: P78-A00
Y300 Should be 18pF XTAL
C320,C321- New tuned values are 18pF
New Discrete VGA filter component values changed to 10pF-68nH-No cap- 68nH-10pF.
NO_STUFF Integrated filter components.

U511 memory regulator o/p current spec lowerd to 2.0A and Added new NVPN for 2.5V.
C145 No_stuff
U701-More substitute added
P300-DB15 and Bracket replaced with new PN.

X18: P78-A00
VGA Filter 10pF to be stuffed, missed in X17

X19: P78-A00
Add note in SCH that SAA7113 is not supported in this design
Heat sink M2 changed from 45x45mm to 53x64mm

X20: P78-A00
PCI Device ID bit labels were reversed, Corrected.
FOR LFH we need 15pF caps for C335, C329, C332, C341, C344, C338 in VGA Filter
R1031, R1032, R1038, R1039, resistor values corrected.

P78-A01-X01
Add D-FF buffer to PCIRST_ signal. Added U101.
Add R325, series termination res to XTALBUFF signal
Add R111, C146 smoothing ckt to PCIRST.
Add R112 to by pass D-FF ckt.
Replaced pkg IND_SMD0805_FLT with SMD0805 for L316-L318, L305, L307, L308
ADD SS Control circuit for 3.3V rail coming delayed (No problem observed in P78 but in other Pxx)
Added Q2, Q3, D25, R618-R620
AGPSTOP pulled to 3.3V from AGPVDDQ

P78-A01-X02
Add R113 & R114 to D-FF ckt and Asynchronously Reset the o/p D-FF using PCIRST_

P78-A02:
1) Added TMDS driveback circuit to block and isolate GPU 5VCLAMP, VDD33 and A3.3V when power is off (workaround for BugID=47136).
2) Changed L307, L305, L308, L317, L318 and L316 footprint back to 0805 pkg which was mistakenly done on A01.
3) Changed netname DP2_HPD to DP2_HPD_XOR at the XOR gate input.
4) Removed R1037, the option to use one regulator for both IFPP0LLVDD and IFP1PLLVDD rails.

Stuff Option	Meaning
COMMON	Common to all assemblies
NO STUFF	Not present in any assembly
VIDCAP	Video In - Video Out, or Video Capture
LFH	LFH BOTH CHANNELS, NO TV, NO VIDCAP
TV	Second DAC channel goes to Svideo connector as TV Out
TVO	4pin DIN for TV Only
VGA1	Filter cap for VGA SKU
1117	Fixed 1117 linear regulator for A3.3V
1117_ADJ	Adjustable 1117 linear regulator for A3.3V
NO_1117	Connect A3.3V to 3.3V. No 1117 regulator.
IFPREG0	2.8V FOR IFP0PLLVD FOR LFH
IFPREG1	2.8V FOR IFP1PLLVD FOR LFH
IFPREG3V	IFP PLLVDD REGULATORS INPUT 3.3V
IFPREG5V	IFP PLLVDD REGULATORS INPUT 5V
ONE_IFPREG	COMMON 2.8V REGULATOR FOR IFP0PLLVD AND IFP1PLLVDD
IFP03V	A3.3V FOR IFP0PLLVD, DON'T USE IFPREG0, FOR TV
IFP13V	A3.3V FOR IFP1PLLVD, DON'T USE IFPREG1, FOR TV
NV17-128D	STRAP OPTION 0X171
CLAMP1	VGA1 Sync/I2C Clamping diodes
RGB_PROT	RGB Protection diodes on primary DAC outputs
CLAMP2	VGA2 Sync/I2C Clamping diodes
RGB2_PROT	RGB Protection diodes on secondary DAC outputs
CLAMP3	VIDCAP I2C/Video In Clamping diodes
TVCLAMP	TV Red/Green Clamping diodes
GPU	GPU ONLY
NV17-128D	IDSTRAP OPTION-171H
MEMORY	Memory only
M2-8V	Memory & PS output 2.8V
M2-5V	Memory & PS output 2.5V
BUF_RESET	PCIRST through D-FF circuit

PAGE OVERVIEW

VIDEO CAPTURE USING SAA7113 IS NOT SUPPORTED IN P78

REFER BOM FOR CORRECT NVPNs

140-10078-0000-A02
602-10078-0000-A02

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P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X

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{Item}\t{Quantity}\t{Reference}\t{Value}\t{Assembly}\t{MAIN}\t{NVPN}\t{Source Package}\t{AVL1}\t{AVL2}\t{AVL3}\t{AVL4}\t{AVL5}
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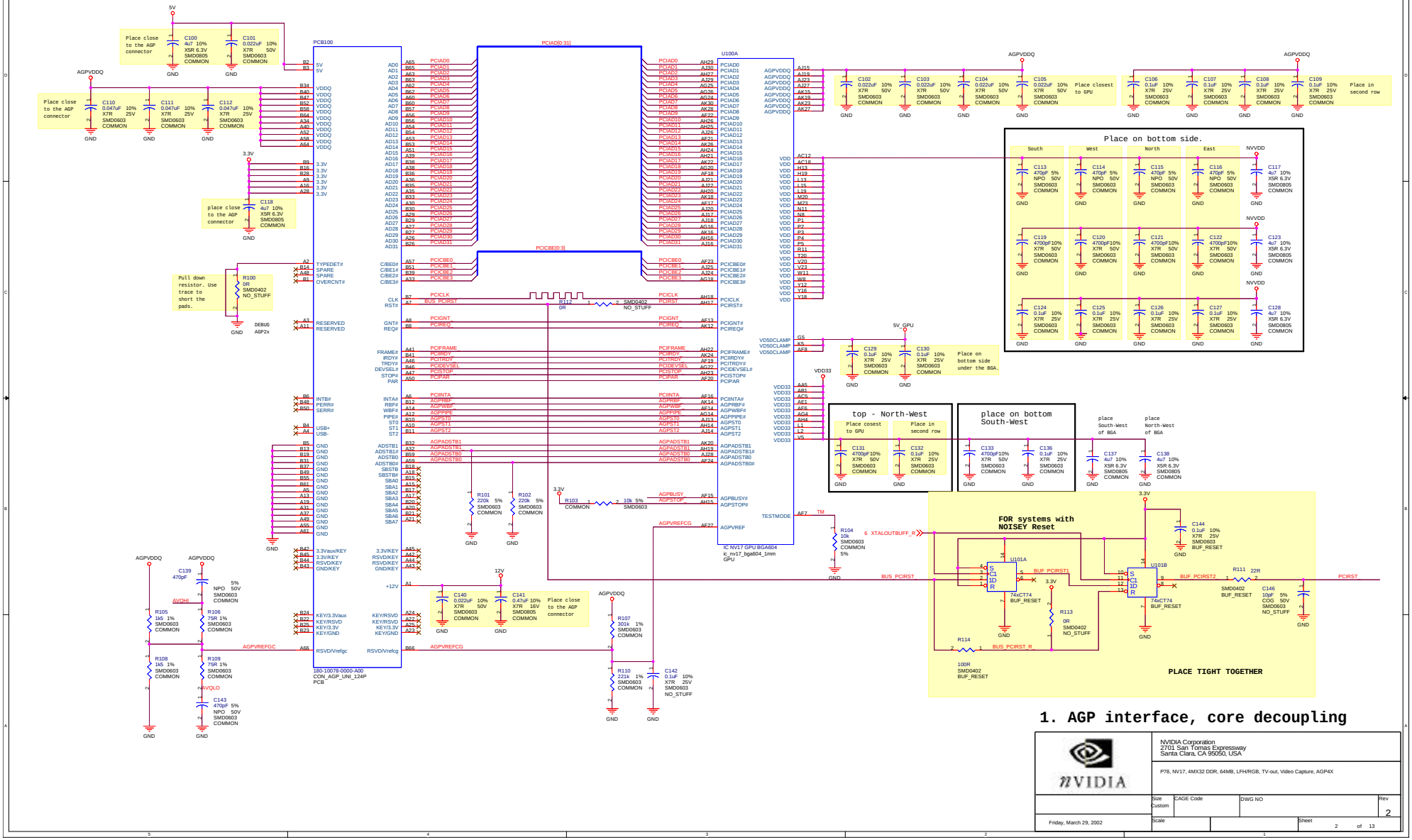

1. AGP interface, core decoupling

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Size	CAGE Code	DWG NO	Rev
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Scale		Sheet	2 of 13

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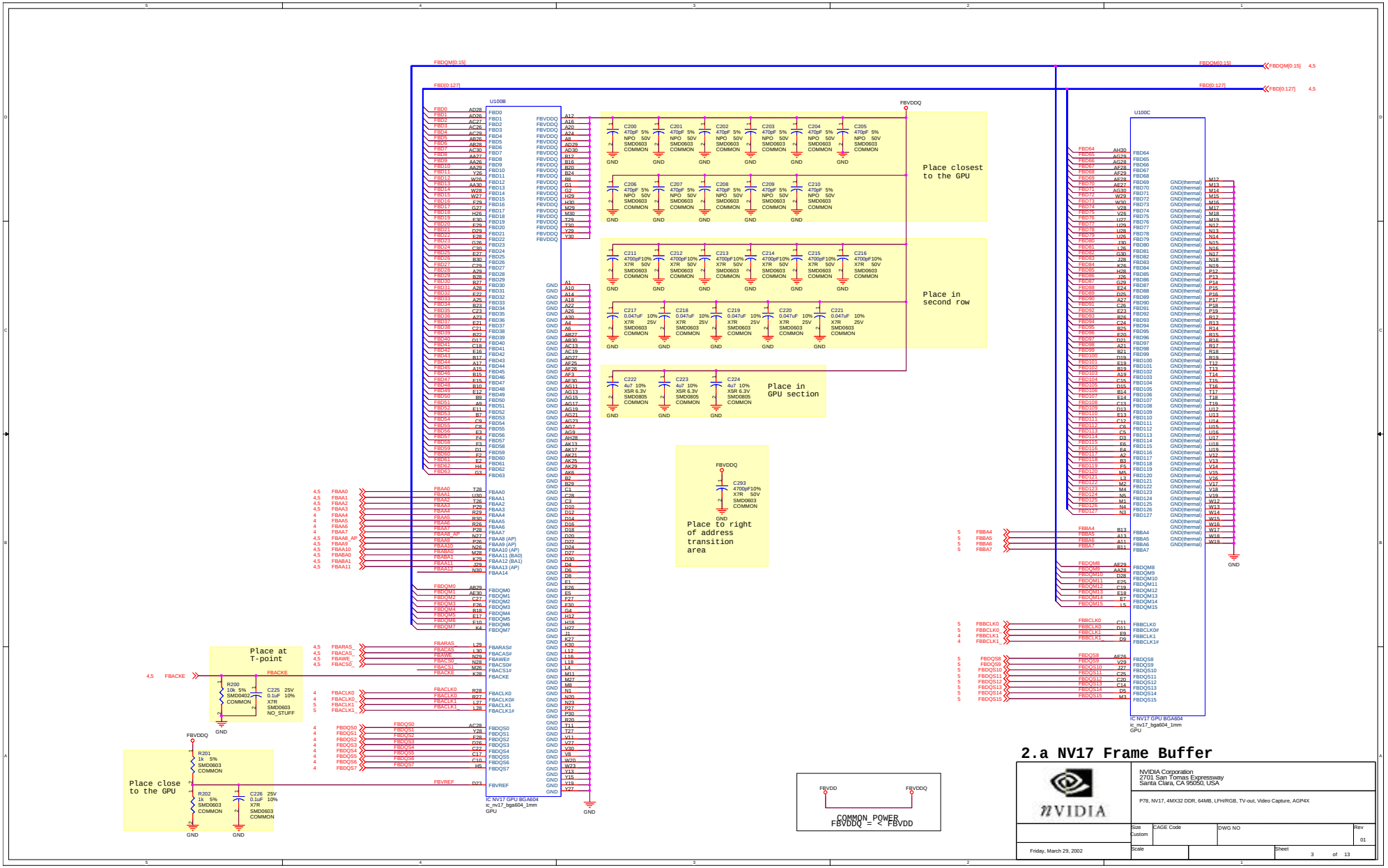

2.a NV17 Frame Buffer

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Size	CAGE Code	DWG NO	Rev
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Scale			Sheet 3 of 13

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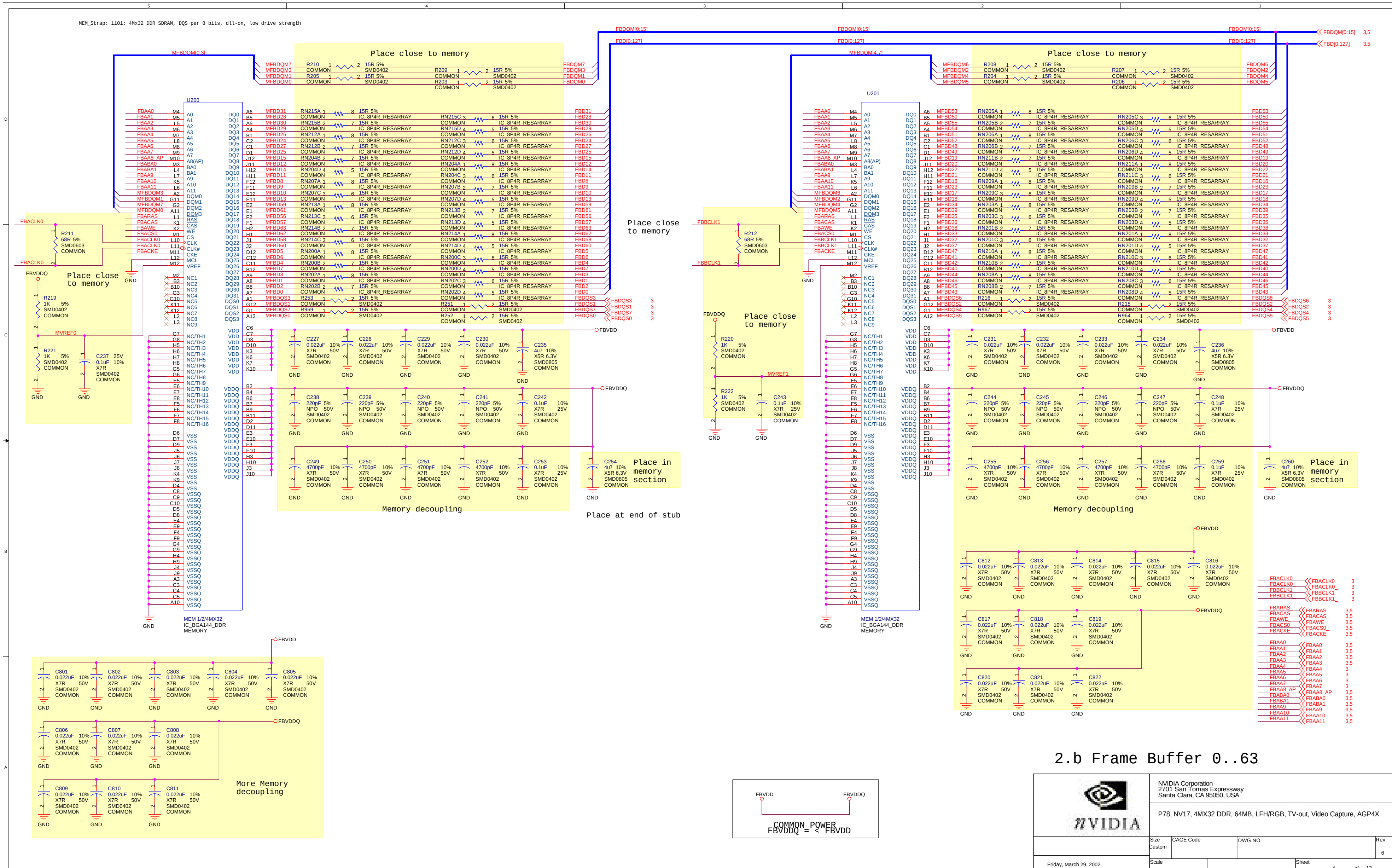

2.b Frame Buffer 0..63

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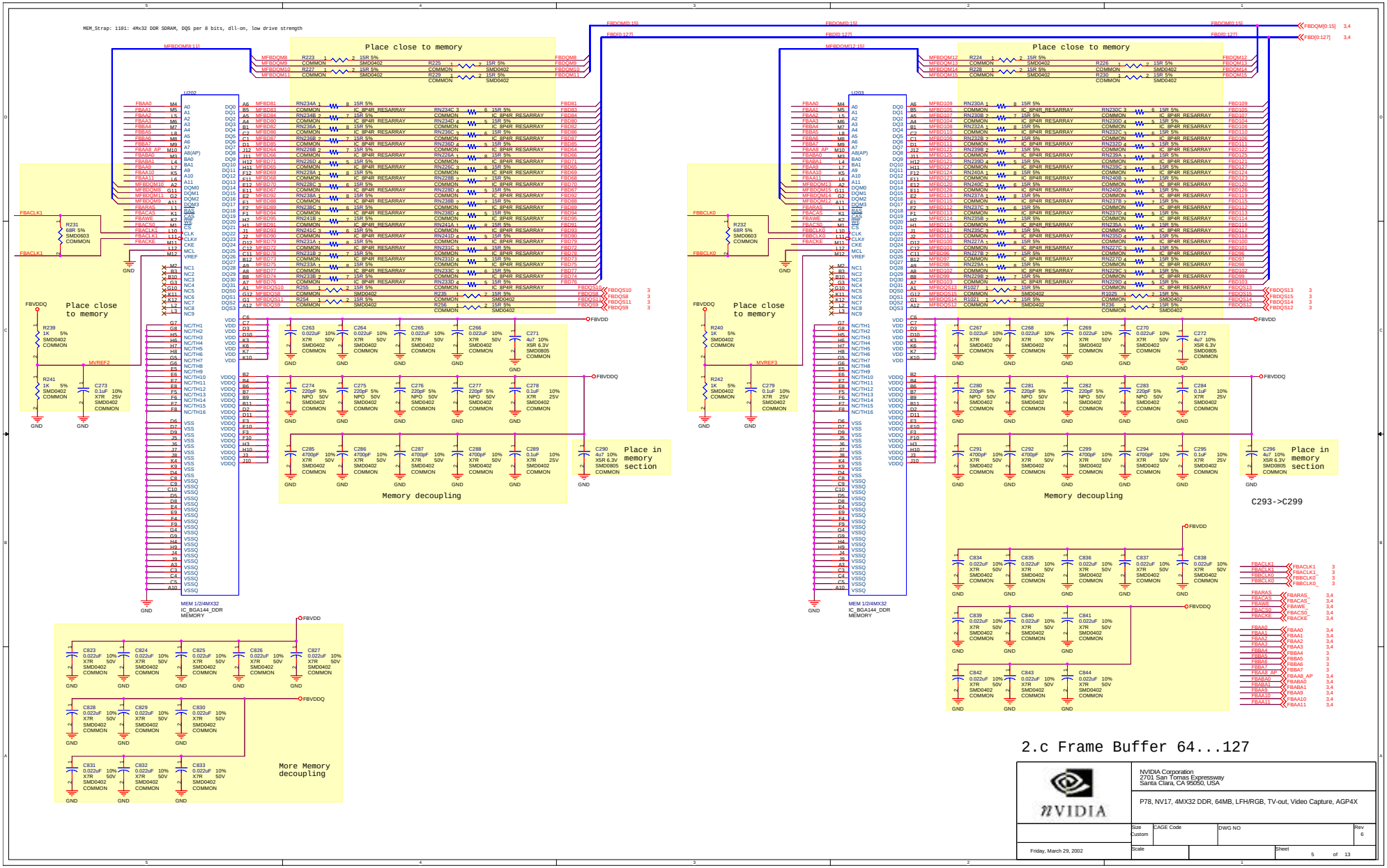
Size	CAGE Code	DWG NO	Rev
Custom			6

Friday, March 29, 2002 — Scale — Sheet 4 of 13


MEM_Strap: 1181: 4Mx32 DDR SDRAM, DQS per 8 bits, dll-on, low drive strength
Place close to memory
Place close to memory
Place close to memory
Place close to memory
Place in memory section
Place in memory section
Memory decoupling
Memory decoupling
More Memory decoupling
C293->C299
MEM 1/2/4MX32 IC_BGA144_DDR MEMORY
MEM 1/2/4MX32 IC_BGA144_DDR MEMORY
2.c Frame Buffer 64...127
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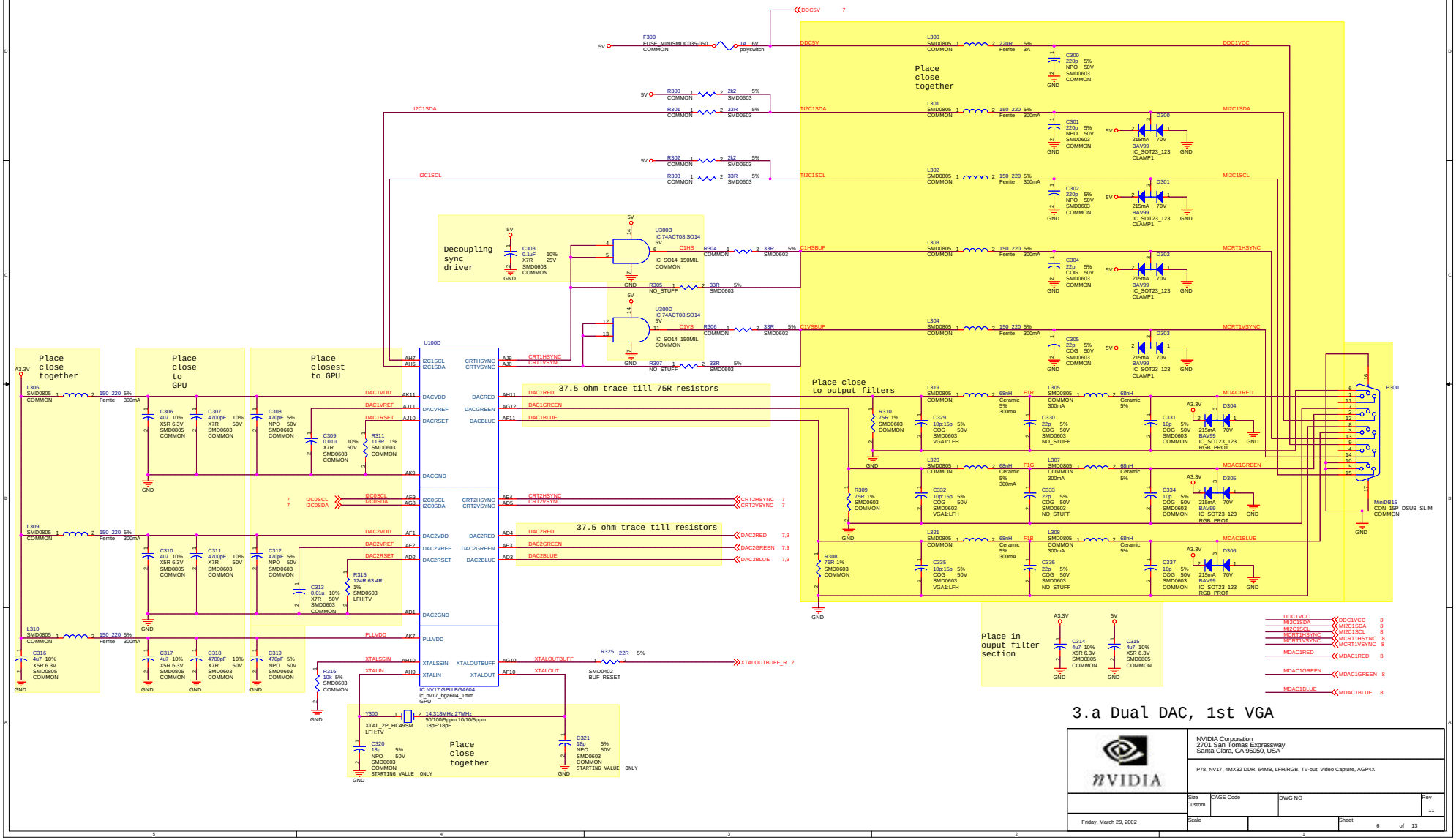
Decoupling sync driver
Place close together
Place close to output filters
Place close to GPU
Place closest to GPU
37.5 ohm trace till 75R resistors
37.5 ohm trace till resistors
Place in ouput filter section
IC NV17 GPU BGA604
P300
MiniDB15
3.a Dual DAC, 1st VGA
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Friday, March 29, 2002
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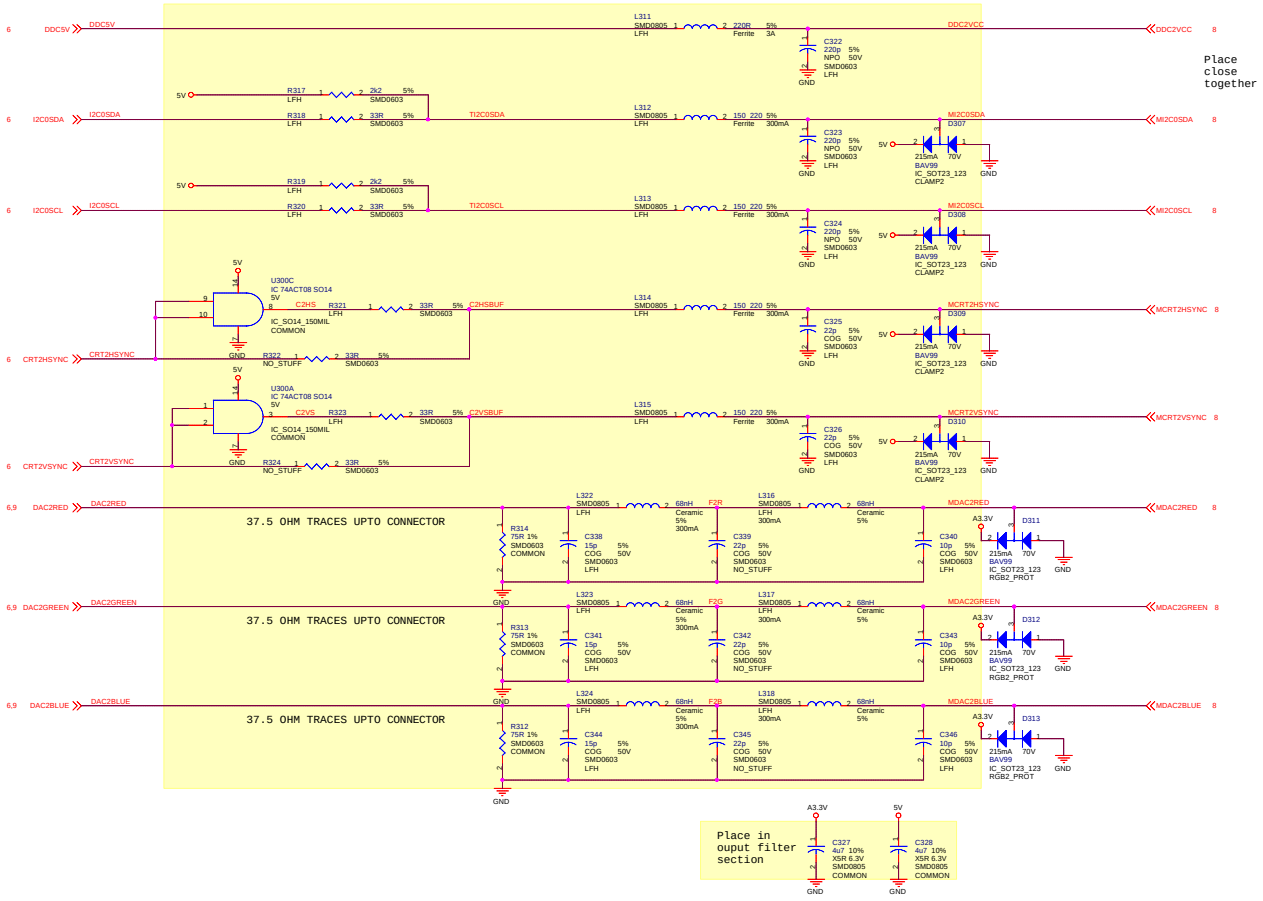

VERIFY SKU FOR PROTECTION DIODES

3.b Dual DAC, 2nd LFH

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Custom			11
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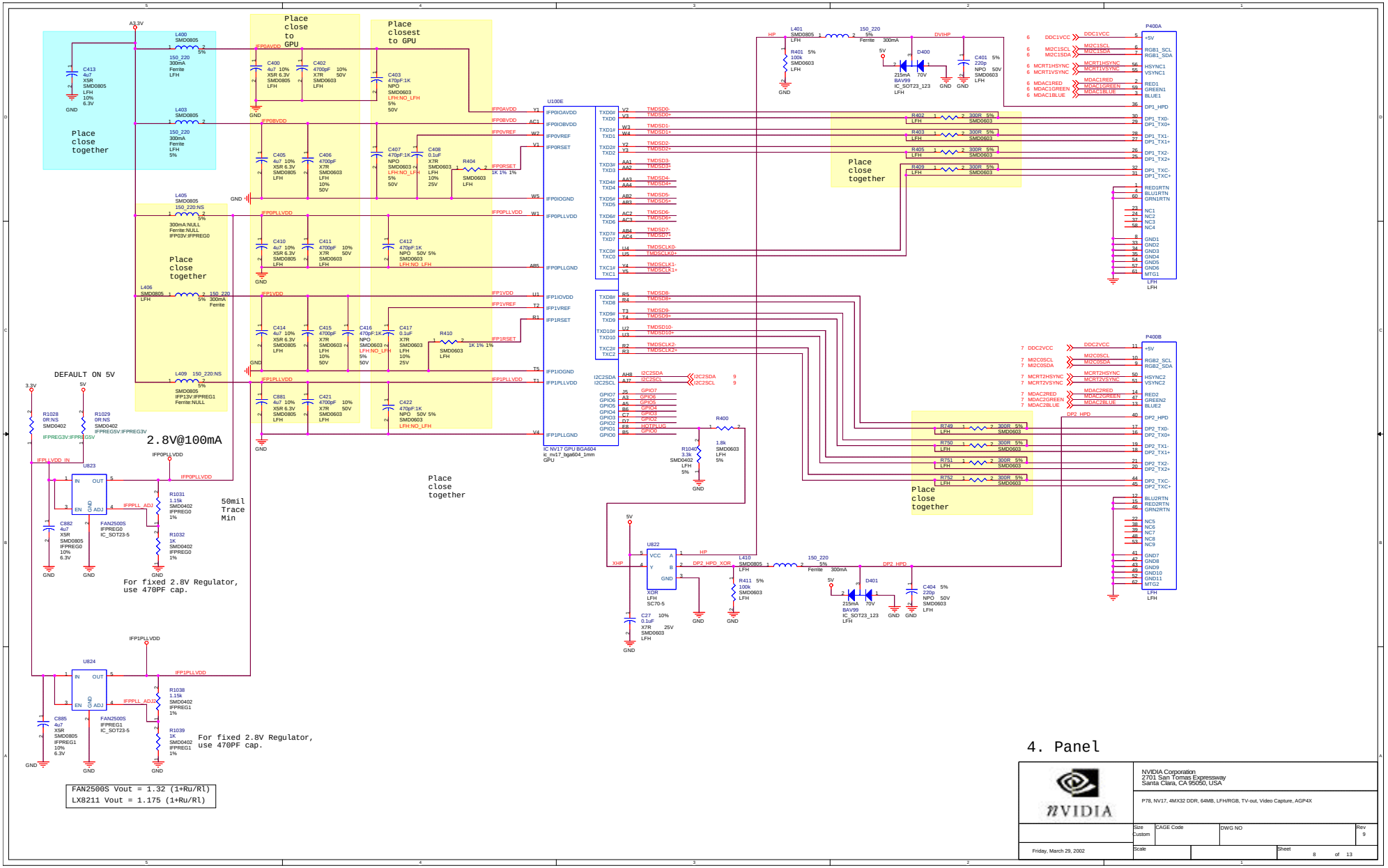

4. Panel

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Size	CAGE Code	DWG NO	Rev
Custom			9

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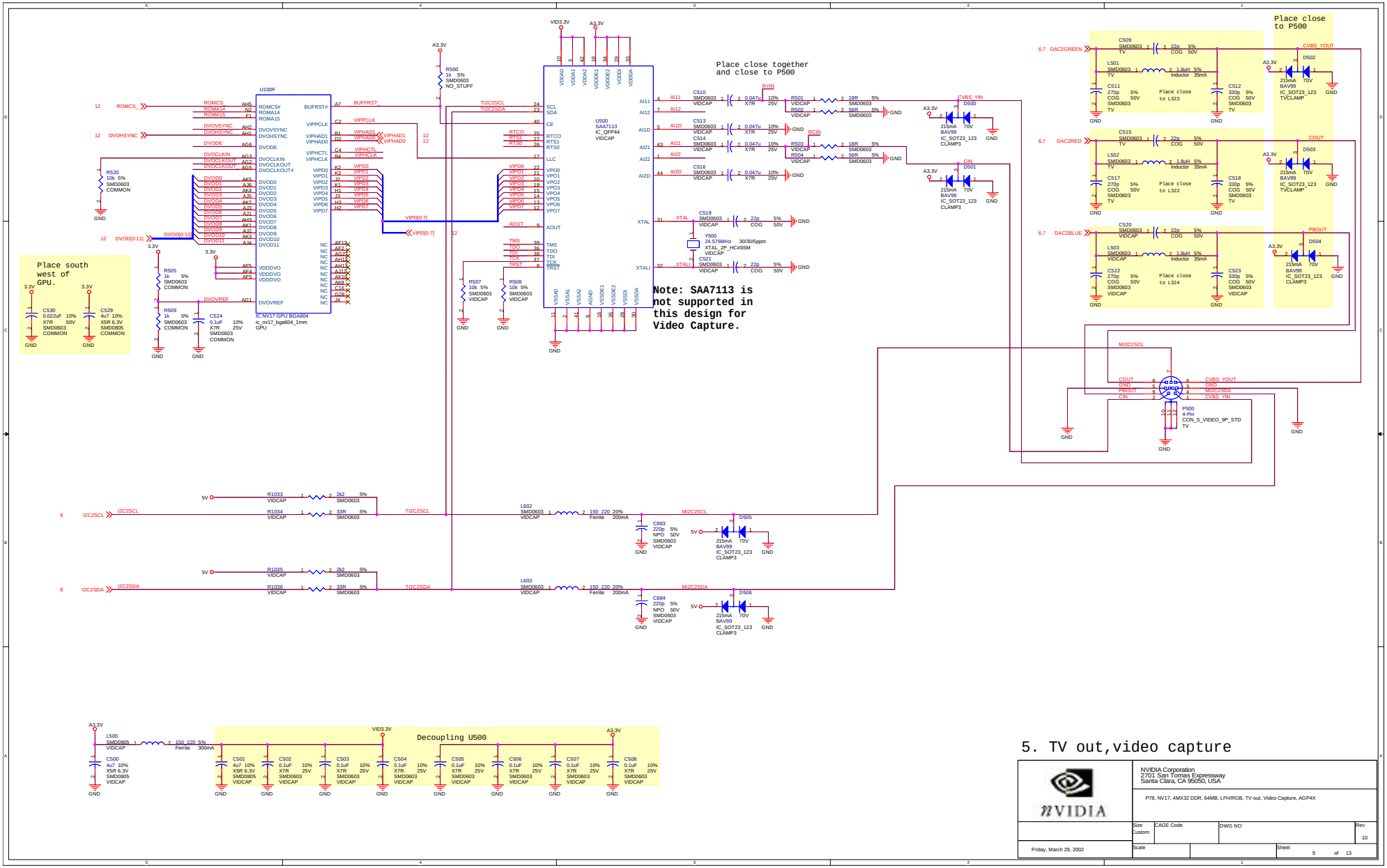
Place close to P500
Place close together and close to P500
Place south west of GPU.
Note: SAA7113 is not supported in this design for Video Capture.
Decoupling U500
U100F
U500
SAA7113
IC_QFP44
VIDCAP
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
GPU
P500
4-Pin
CON_S_VIDEO_9P_STD
TV
CVBS_YOUT
COUT
PBOUT
CVBS_YIN
MI2C2SCL
MI2C2SDA
I2C2SCL
I2C2SDA
TI2C2SCL
TI2C2SDA
VIPD[0:7]
DVOD[0:11]
ROMCS_
DVOHSYNC
DAC2GREEN
DAC2RED
DAC2BLUE
A3.3V
VID3.3V
5V
GND
Inductor 35mA
Place close to L323
Place close to L322
Place close to L324
TVCLAMP
CLAMP3
5. TV out,video capture
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P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X
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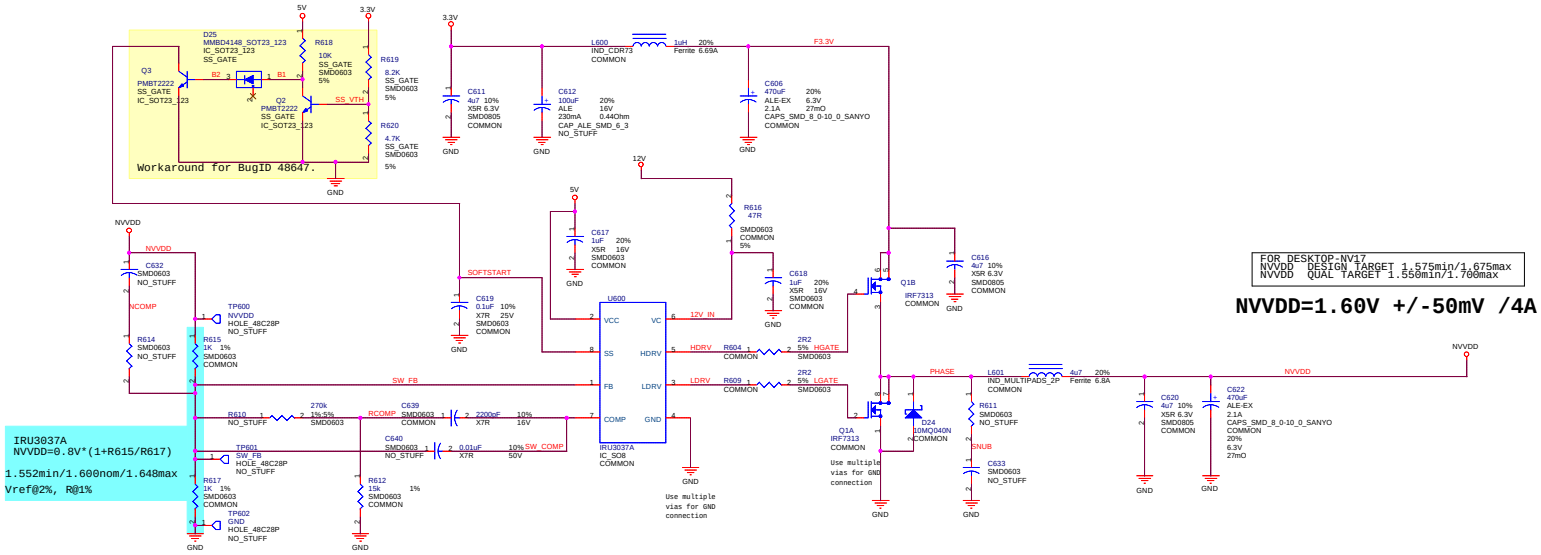
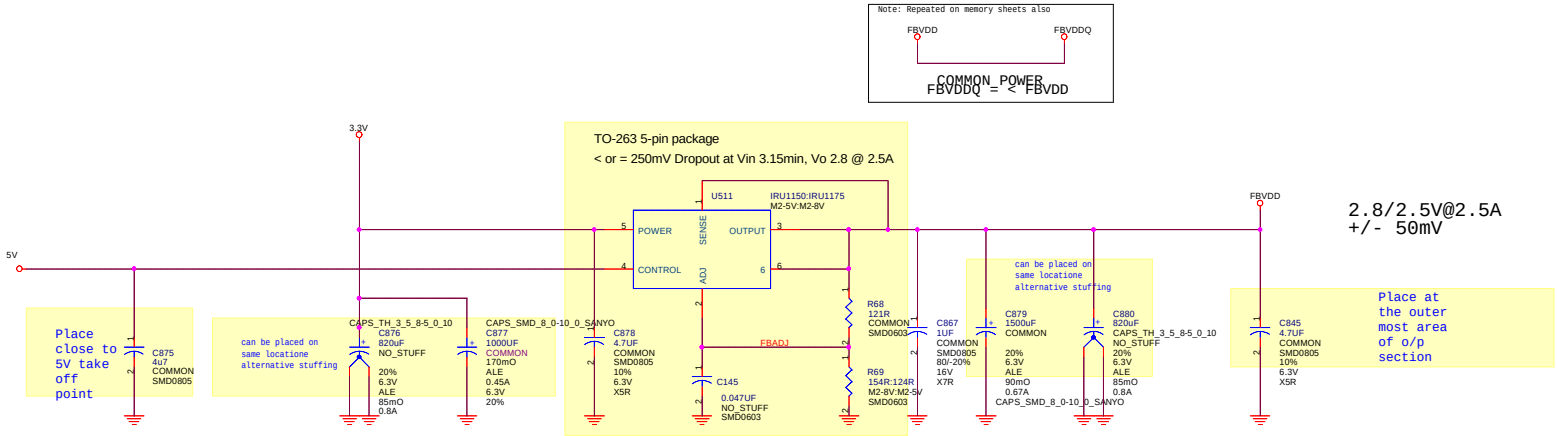


6. Power supply

NVIDIA	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA
	P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X
Friday, March 29, 2002	Size: Custom; CAGE Code; DWG NO; Rev: 16; Scale; Sheet: 10 of 13




```
Vo = 1.25 * ( 1+ R69/R68) + Iadj * R69
 Iadj = 50uA
 M2-8V = 2.512/2.54/2.563- Mem Limit 2.66 to 2.94
 M2-5V = 2.817/2.85/2.881- Mem Limit 2.375 to 2.625
```

6.a MEMORY power supply

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Size	CAGE Code	DWG NO	Rev
C			16

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Scale

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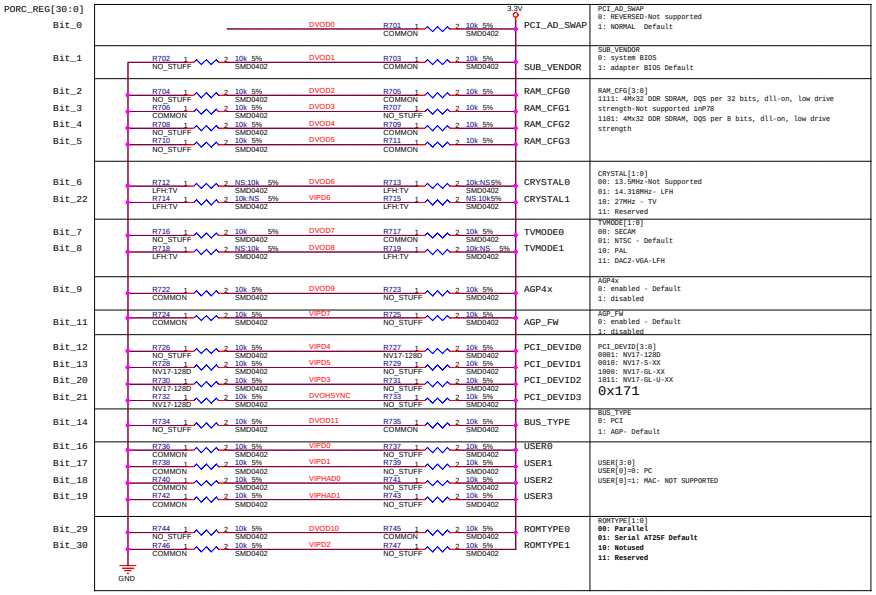
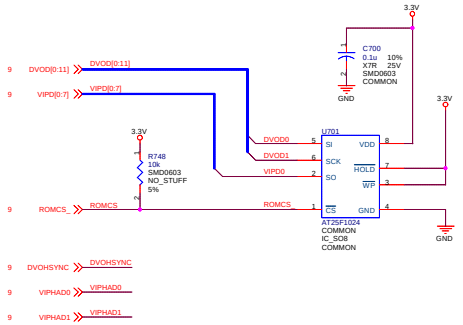
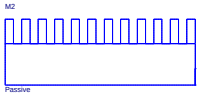
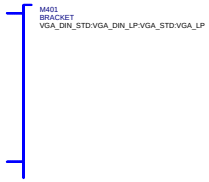






COMMON
110-00018-0000-000
HEATSINK, PASSIVE, MECH HOLD DOWN, 53mm X 64mm



7. BIOS, Strapping

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Custom			17

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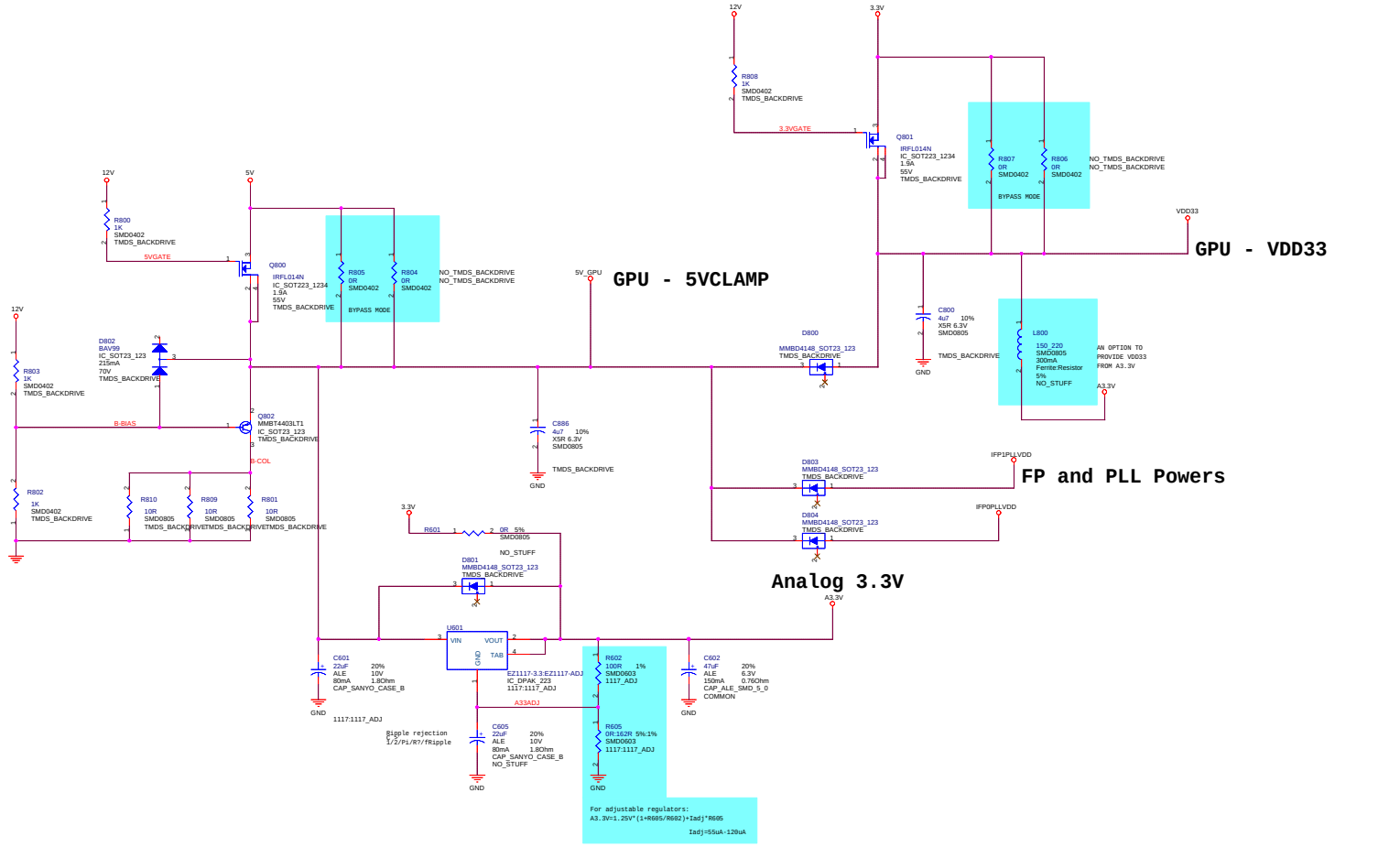
GPU - VDD33
GPU - 5VCLAMP
FP and PLL Powers
Analog 3.3V
8. Linear Power Supplies
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P78, NV17, 4MX32 DDR, 64MB, LFH/RGB, TV-out, Video Capture, AGP4X
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