P2002

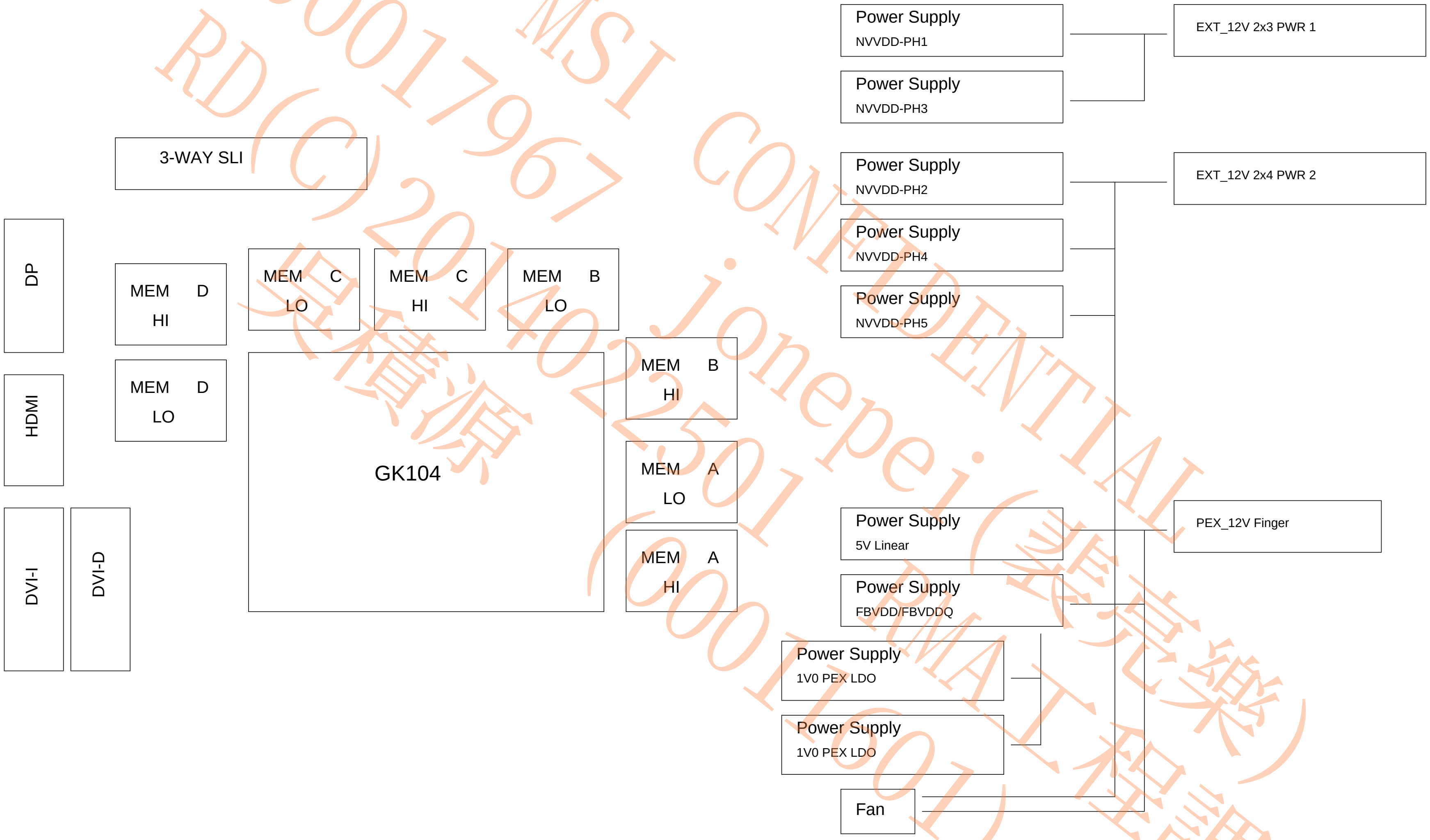
2GB GDDR5, 256b, 64Mx32

Stacked DVI-I/DVI-D + HDMI + DP

TABLE OF CONTENTS

Base on V282-1.0
P17/P18 add dvi emi circuit
P23 add I2C B
P25 CHANGE NVVDD POK & MEM OUTPUT CHOKE
P26/P27 CHANGE NVVDD POWER CIRCUIT
P30 CHANGE INPUT CHOKE/ 6pin 8pin connect colay

Page2: Block Diagram



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Custom	2: Block Diagram	40

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Page3: PCI Express

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	24MIL
3V3	3.3V	3.0A	20MIL
GND	0V	8.5A	16MIL

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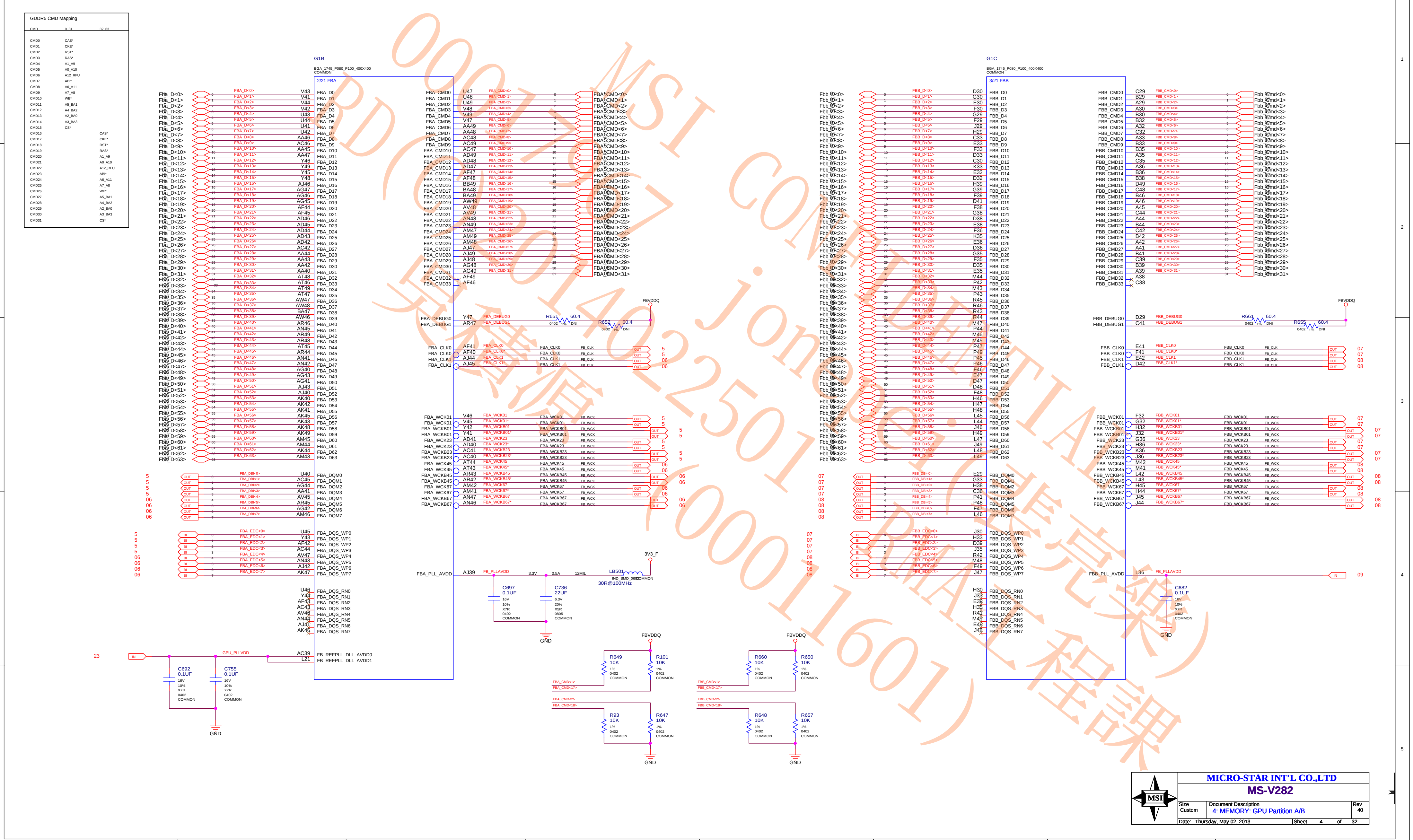
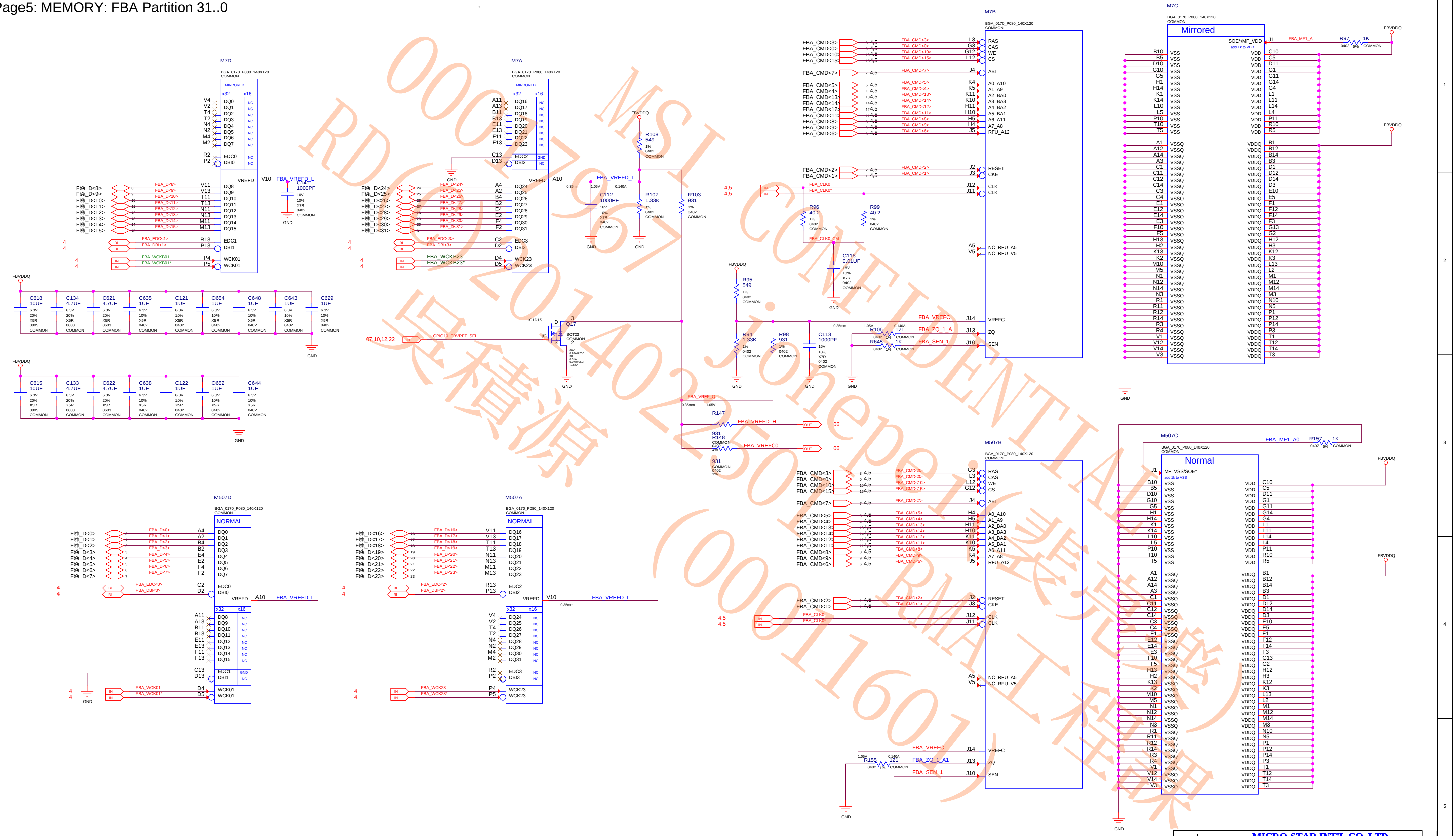
Page4: MEMORY: GPU Partition A/B



Page5: MEMORY: FBA Partition 31..0


M7D
M7A
M7B
M7C
M507D
M507A
M507B
M507C
BGA_0170_P080_140X120
Mirrored
Normal
FBA_VREFD_L
FBA_VREFC
FBA_VREFD_H
FBA_VREFC0
FBA_ZQ_1_A
FBA_SEN_1
FBA_MF1_A0
FBVDDQ
GND
GPIO10_FBVREF_SEL
Q17
SOT23
R108 549
R107 1.33K
R103 931
R96 40.2
R99 40.2
R95 549
R94 1.33K
R98 931
R106 121
R645 1K
R147 931
R148 931
R155 121
R97 1K
R157 1K
C141 1000PF
C112 1000PF
C113 1000PF
C118 0.01UF
C618 10UF
C134 4.7UF
C621 4.7UF
C635 1UF
C121 1UF
C654 1UF
C648 1UF
C643 1UF
C629 1UF
C615 10UF
C133 4.7UF
C622 4.7UF
C638 1UF
C122 1UF
C652 1UF
C644 1UF

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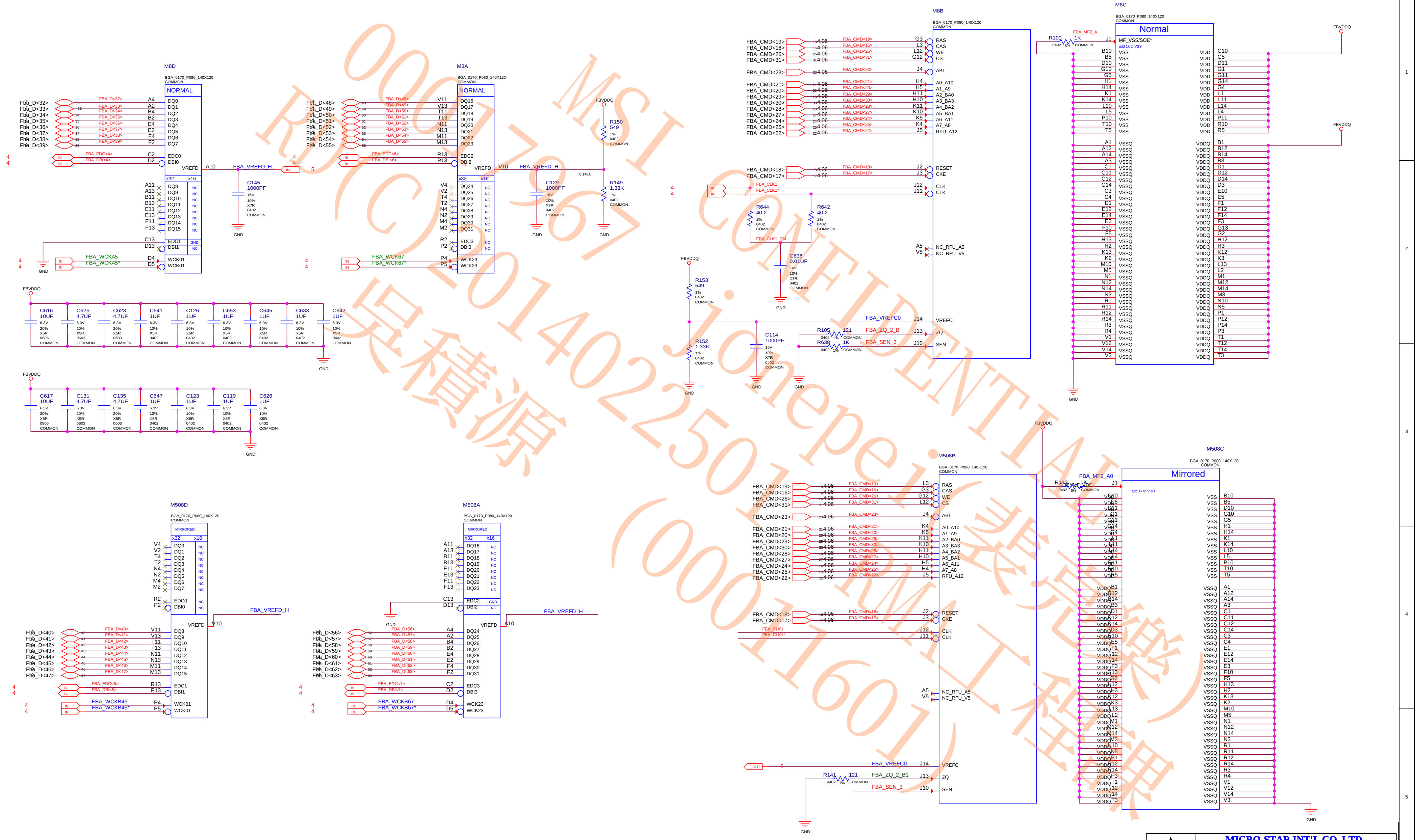
Page6: MEMORY: FBA Partition 63..32



M8D
M8A
M8B
M8C
M508D
M508A
M508B
M508C
BGA_0170_P080_140X120
NORMAL
Normal
MIRRORED
Mirrored
FBA_VREFD_H
FBA_VREFC0
FBA_WCK45
FBA_WCK67
FBA_WCKB45
FBA_WCKB67
FBA_ZQ_2_B
FBA_ZQ_2_B1
FBA_SEN_3
FBA_CLK1
FBA_CLK1*
FBA_MF2_A
FBA_MF2_A0
FBVDDQ
GND
R150 549
R149 1.33K
R153 549
R152 1.33K
R644 40.2
R642 40.2
R105 121
R638 1K
R141 121
R100 1K
C145 1000PF
C129 1000PF
C114 1000PF
C636 0.01UF
C616 10UF
C625 4.7UF
C623 4.7UF
C641 1UF
C126 1UF
C653 1UF
C645 1UF
C633 1UF
C642 1UF
C617 10UF
C131 4.7UF
C135 4.7UF
C647 1UF
C123 1UF
C119 1UF
C626 1UF

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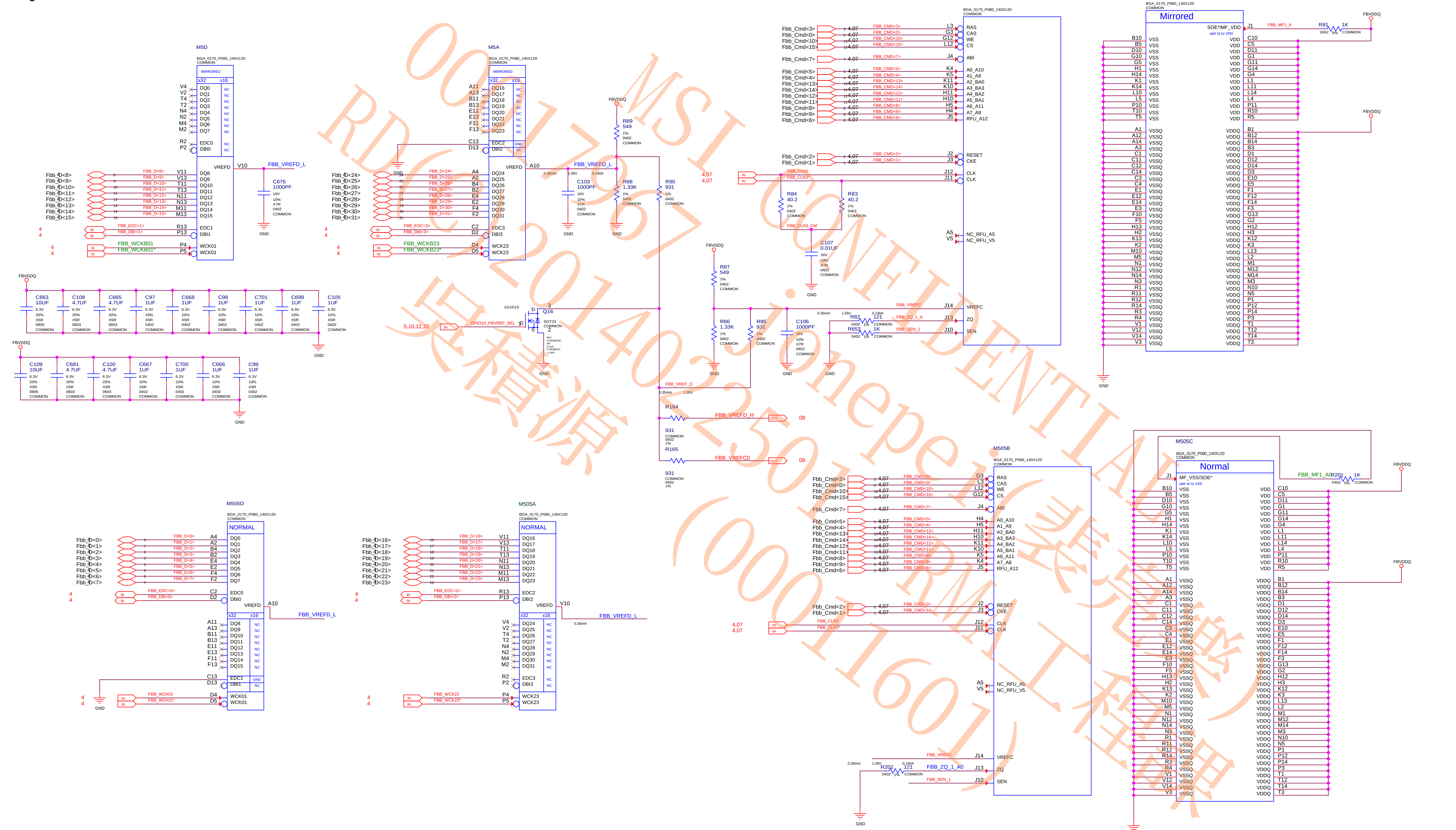
Page7: MEMORY: FBB Partition 31..0



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Custom	7: MEMORY: FBB Partition 31..0	40

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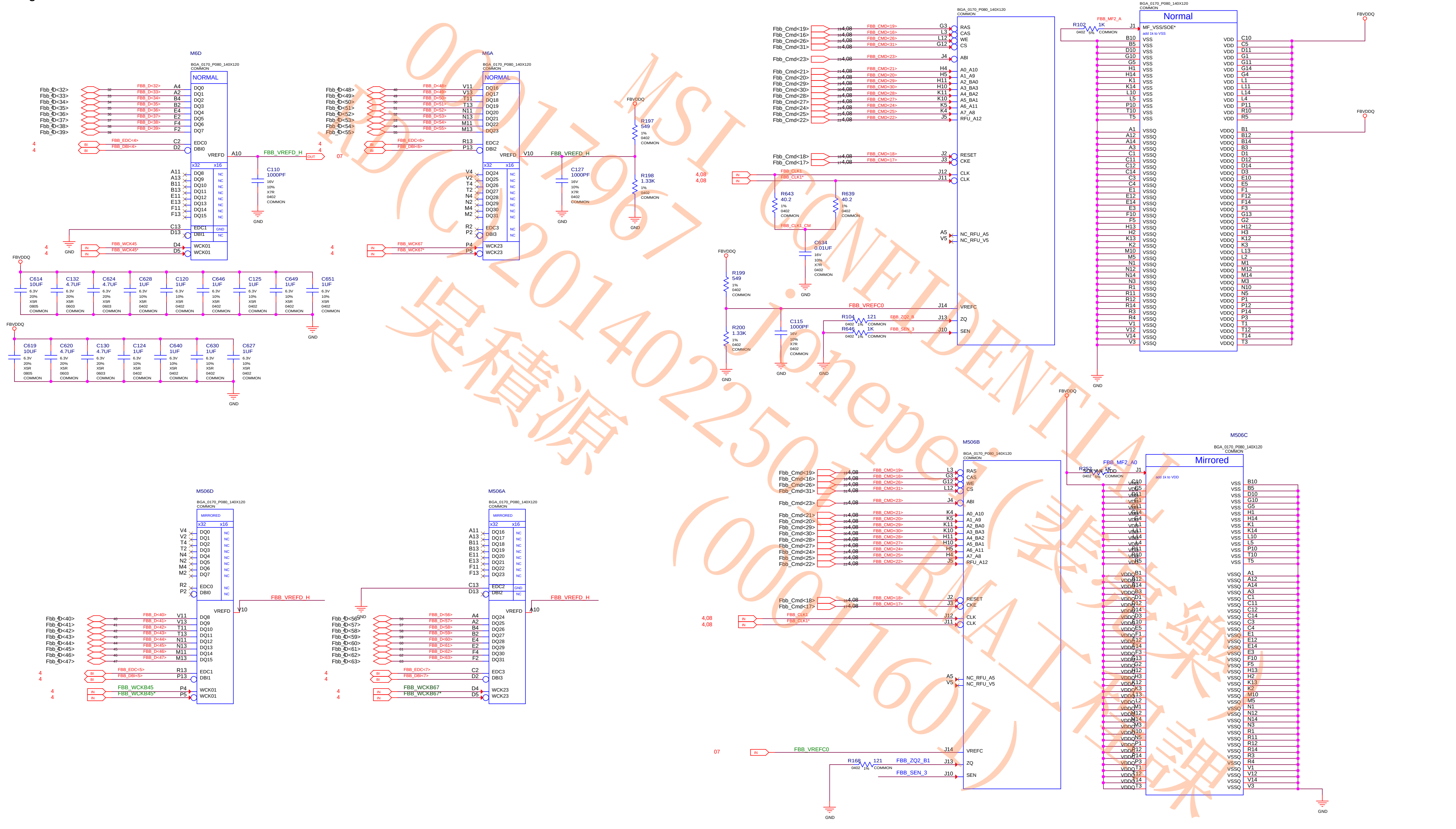
Page8: MEMORY: FBB Partition 63..32



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Custom	8: MEMORY: FBB Partition 63..32	40

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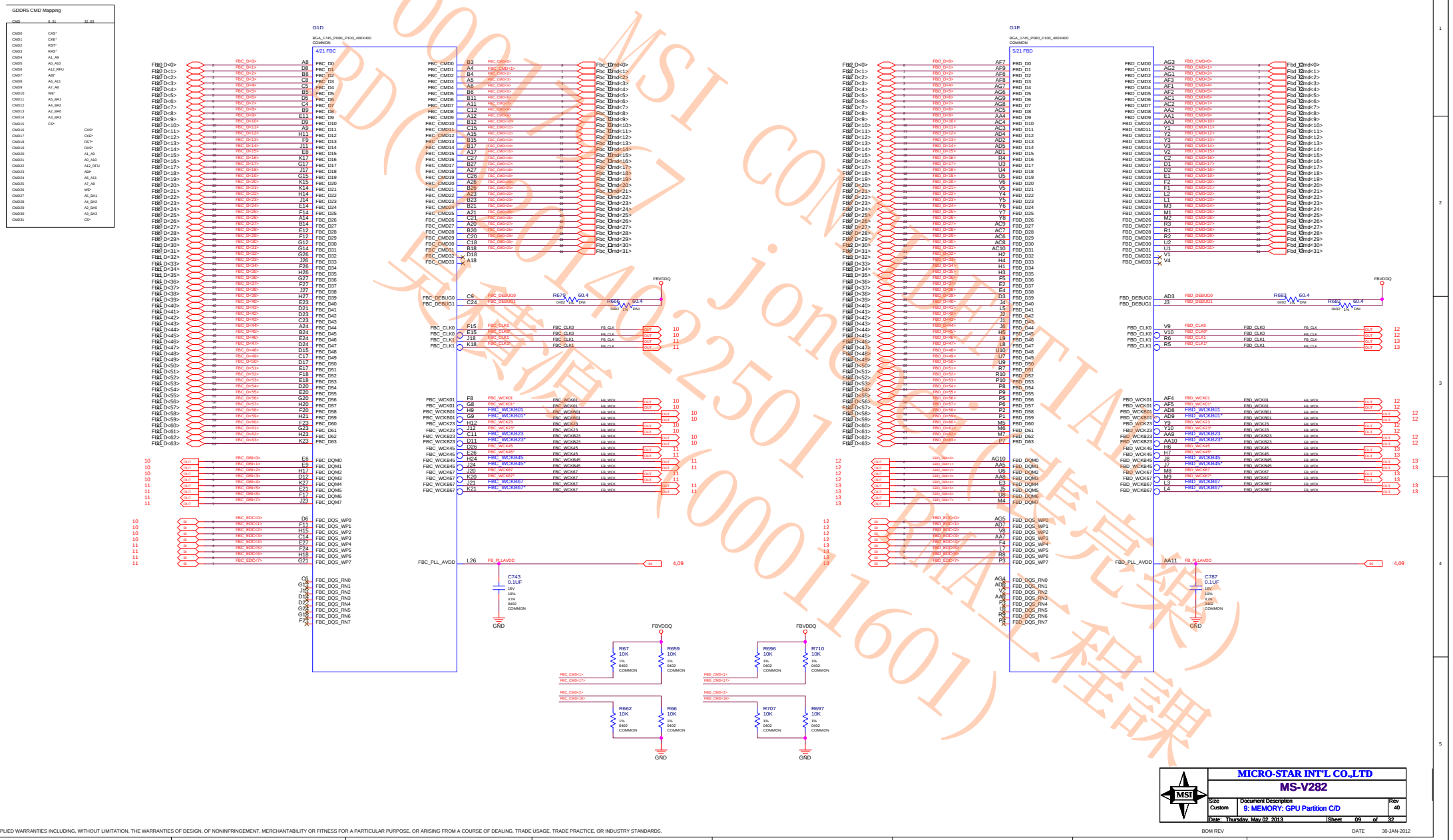
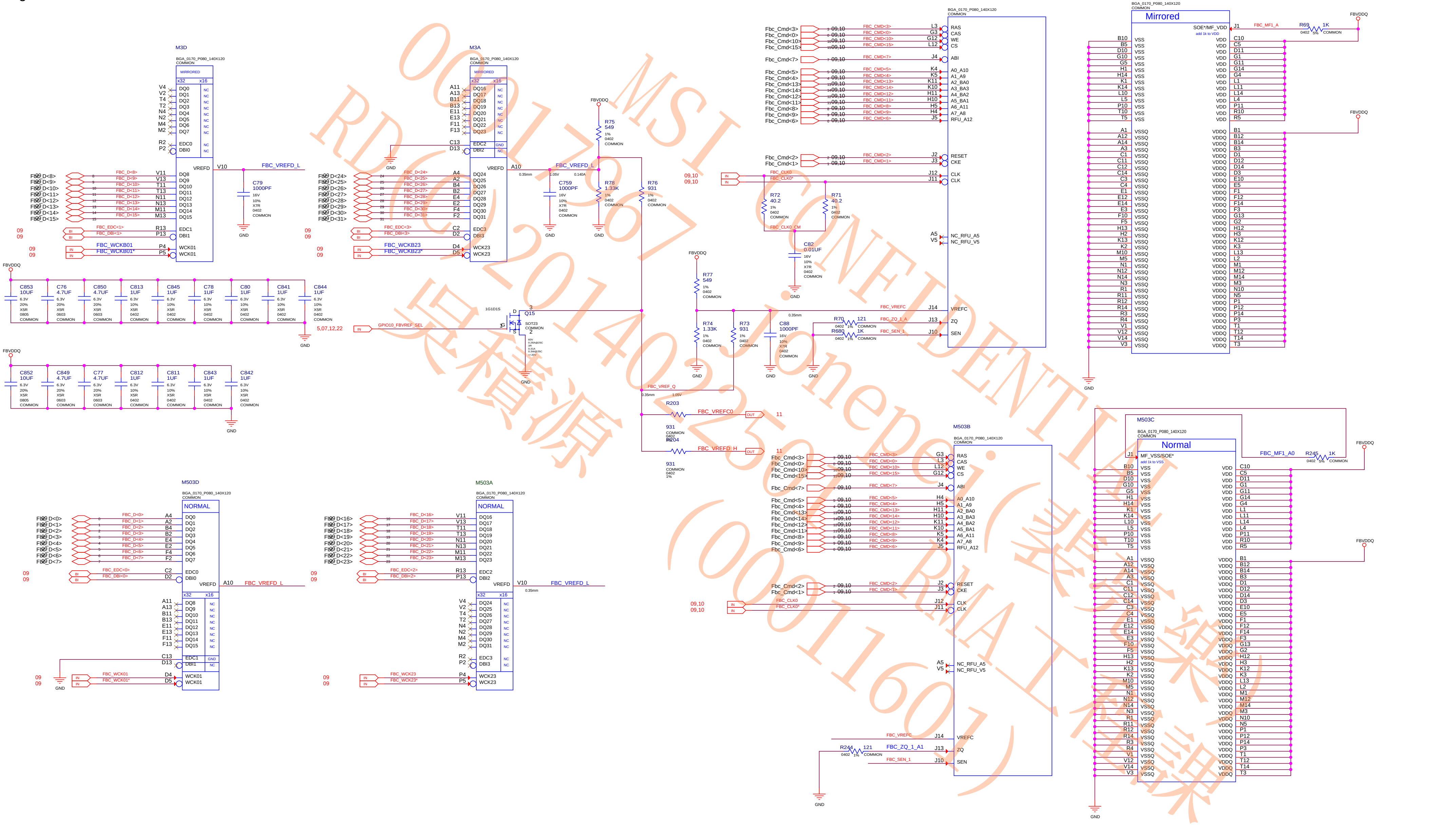
Page9: MEMORY: GPU Partition C/D



Page10: MEMORY: FBC Partition 31..0


M3D
BGA_0170_P080_140X120
MIRRORED
M3A
M3B
M3C
Mirrored
M503D
M503A
NORMAL
M503B
M503C
Normal
FBC_VREFD_L
FBC_VREFC
FBC_VREFC0
FBC_VREFD_H
FBC_VREF_Q
FBC_ZQ_1_A
FBC_ZQ_1_A1
FBC_SEN_1
FBC_MF1_A
FBC_MF1_A0
FBC_CLK0
FBC_CLK0*
FBC_CLK0_CM
FBC_WCKB01
FBC_WCKB01*
FBC_WCKB23
FBC_WCKB23*
FBC_WCK01
FBC_WCK01*
FBC_WCK23
FBC_WCK23*
GPIO10_FBVREF_SEL
FBVDDQ
GND
Q15
SOT23
R75 549
R78 1.33K
R76 931
R77 549
R74 1.33K
R73 931
R72 40.2
R71 40.2
R70 121
R680 1K
R69 1K
R245 1K
R244 121
R203 931
R204 931
C79 1000PF
C759 1000PF
C88 1000PF
C82 0.01UF
C853 10UF
C76 4.7UF
C850 4.7UF
C813 1UF
C845 1UF
C78 1UF
C80 1UF
C841 1UF
C844 1UF
C852 10UF
C849 4.7UF
C77 4.7UF
C812 1UF
C811 1UF
C843 1UF
C842 1UF

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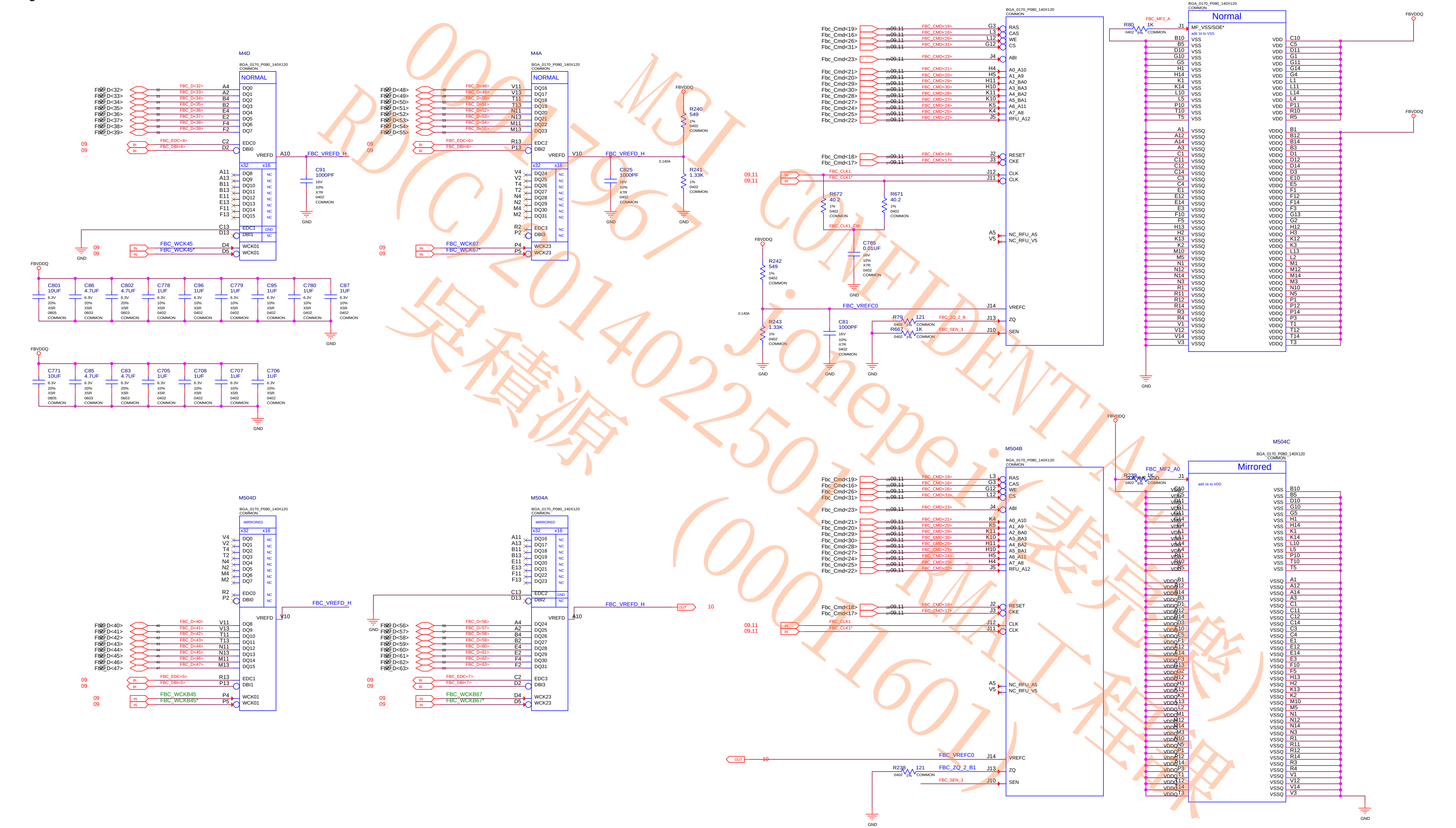
Page11: MEMORY: FBC Partition 63..32



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Size: Custom	Document Description: 11: MEMORY: FBC Partition 63..32	Rev: 40
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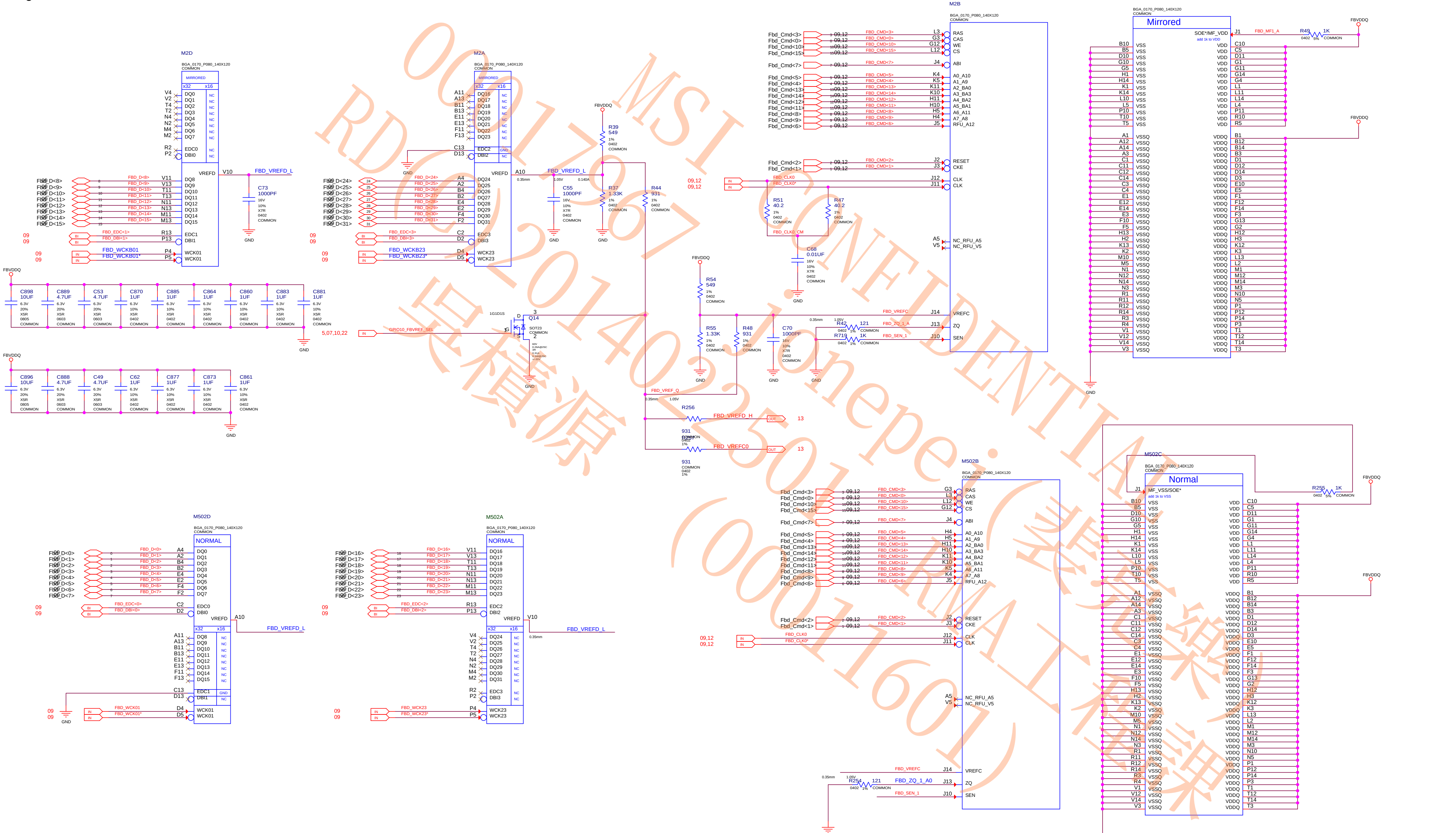
Page12: MEMORY: FBD Partition 31..0



M2D
BGA_0170_P080_140X120
MIRRORED
M2A
M2B
M2C
Mirrored
M502D
M502A
NORMAL
M502B
M502C
Normal
FBD_VREFD_L
FBD_VREFD_H
FBD_VREFC0
FBD_WCKB01
FBD_WCKB23
FBD_ZQ_1_A0
GPIO10_FBVREF_SEL
5,07,10,22
FBVDDQ
GND
Q14
SOT23
C73 1000PF
C55 1000PF
C70 1000PF
C68 0.01UF
R39 549
R37 1.33K
R44 931
R51 40.2
R47 40.2
R54 549
R55 1.33K
R48 931
R42 121
R719 1K
R49 1K
R256
R254 121
R255 1K
C898 10UF
C889 4.7UF
C53 4.7UF
C870 1UF
C885 1UF
C864 1UF
C860 1UF
C883 1UF
C881 1UF
C896 10UF
C888 4.7UF
C49 4.7UF
C62 1UF
C877 1UF
C873 1UF
C861 1UF

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Custom	12: MEMORY: FBD Partition 31..0	40

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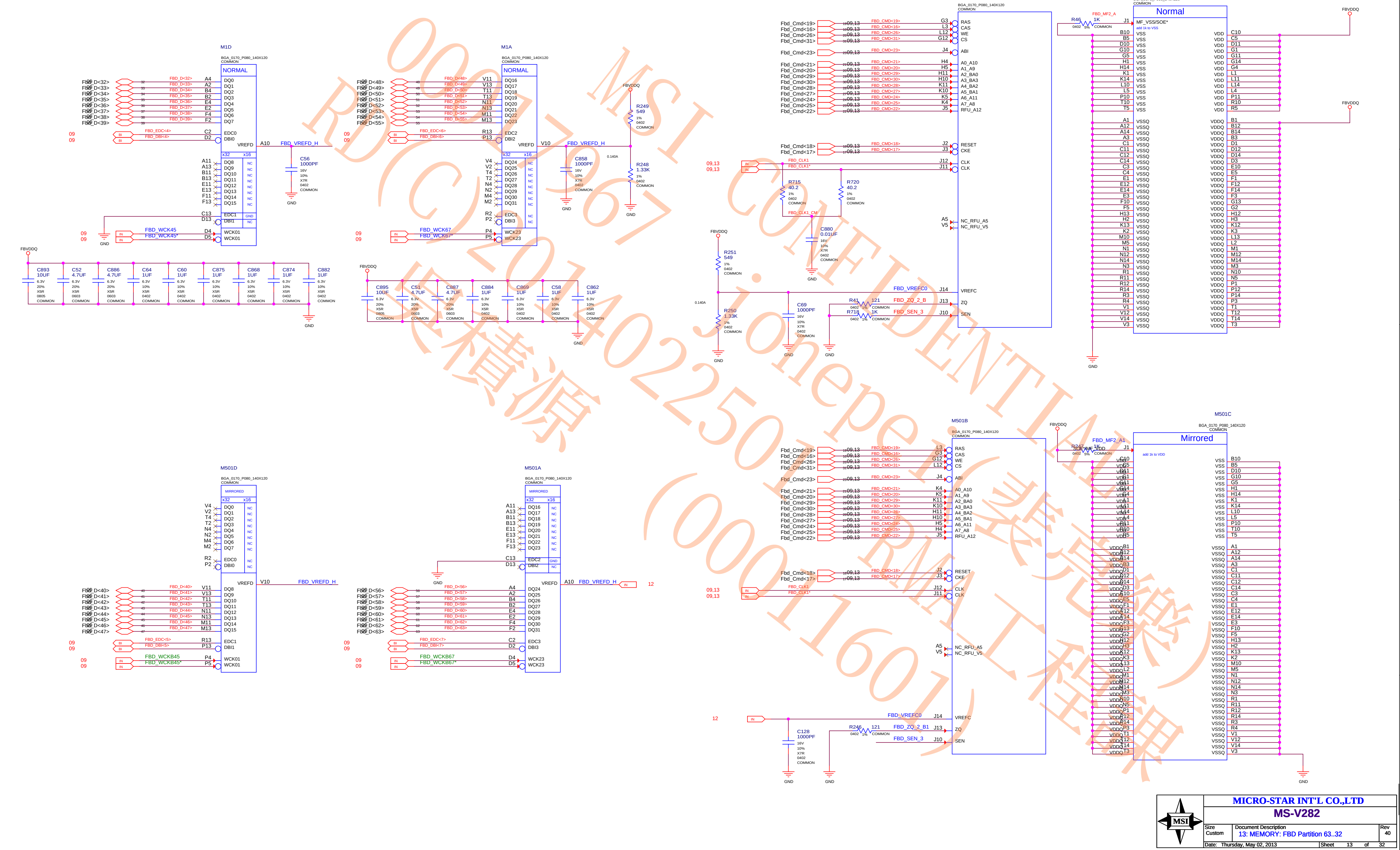
Page13: MEMORY: FBD Partition 63..32



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Custom	13: MEMORY: FBD Partition 63..32	40

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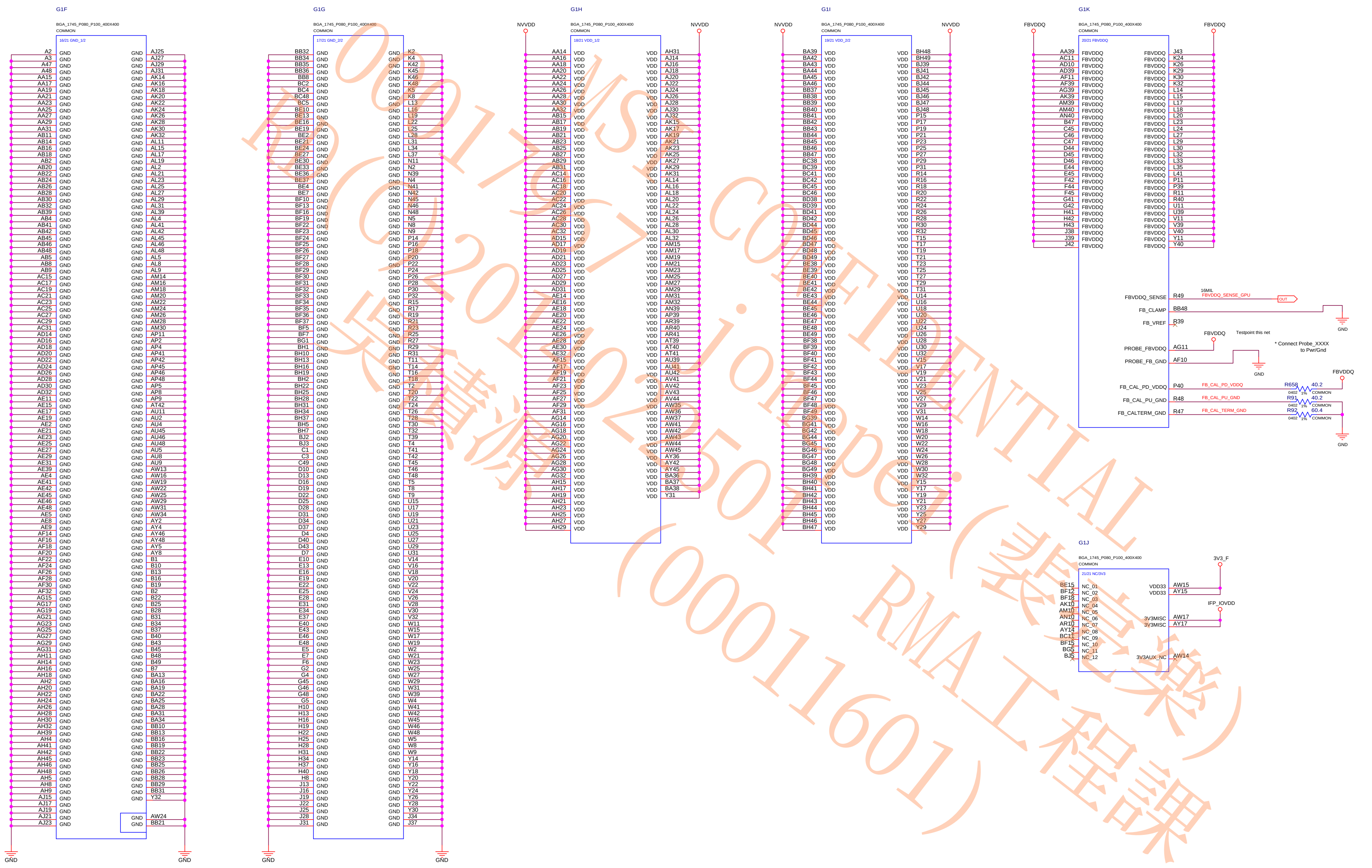
Page14: GPU PWR and GND



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Custom	14: GPU PWR and GND	40

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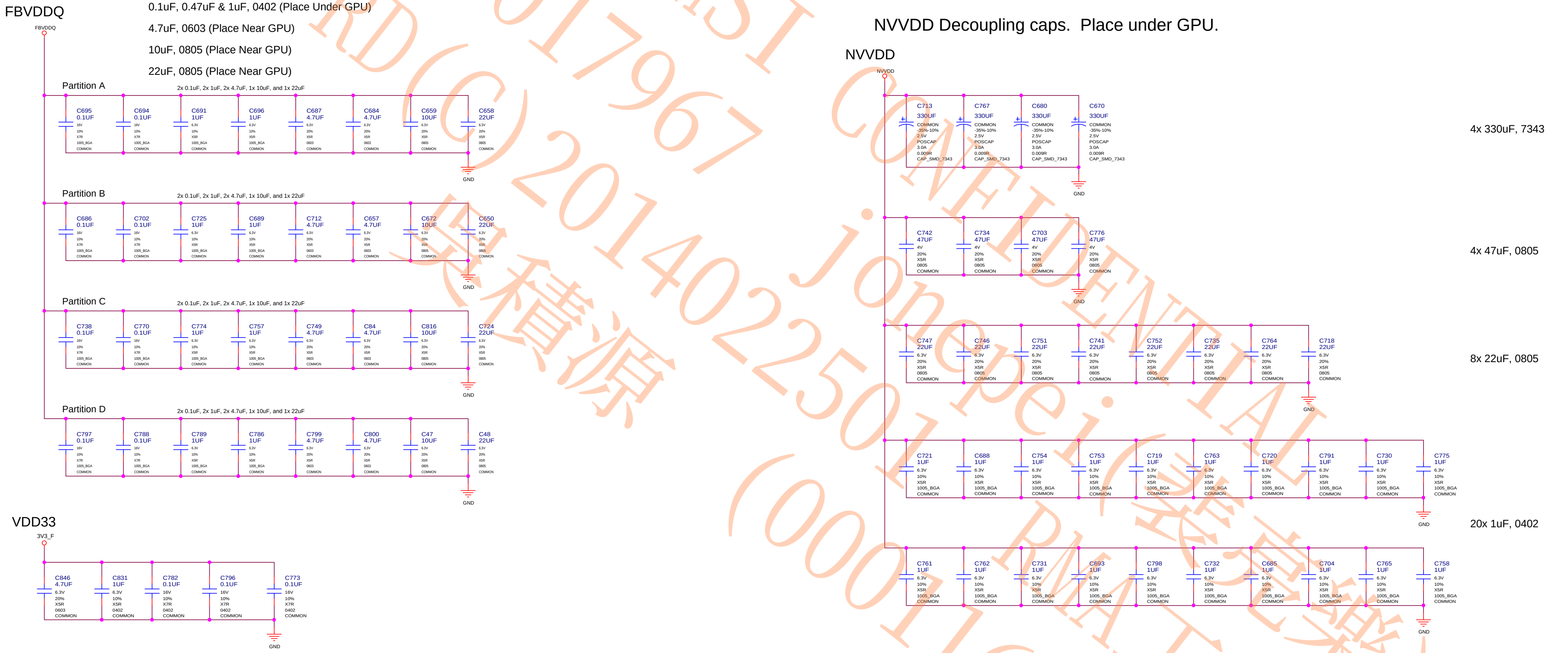
Page15: GPU Decoupling

Based on GB2-X GDDR5 FBVDDQ Decap Guideline



FBVDDQ
0.1uF, 0.47uF & 1uF, 0402 (Place Under GPU)
4.7uF, 0603 (Place Near GPU)
10uF, 0805 (Place Near GPU)
22uF, 0805 (Place Near GPU)
Partition A
2x 0.1uF, 2x 1uF, 2x 4.7uF, 1x 10uF, and 1x 22uF
C695 0.1UF
C694 0.1UF
C691 1UF
C696 1UF
C687 4.7UF
C684 4.7UF
C659 10UF
C658 22UF
Partition B
2x 0.1uF, 2x 1uF, 2x 4.7uF, 1x 10uF, and 1x 22uF
C686 0.1UF
C702 0.1UF
C725 1UF
C689 1UF
C712 4.7UF
C657 4.7UF
C672 10UF
C650 22UF
Partition C
2x 0.1uF, 2x 1uF, 2x 4.7uF, 1x 10uF, and 1x 22uF
C738 0.1UF
C770 0.1UF
C774 1UF
C757 1UF
C749 4.7UF
C84 4.7UF
C816 10UF
C724 22UF
Partition D
2x 0.1uF, 2x 1uF, 2x 4.7uF, 1x 10uF, and 1x 22uF
C797 0.1UF
C788 0.1UF
C789 1UF
C786 1UF
C799 4.7UF
C800 4.7UF
C47 10UF
C48 22UF
GND
VDD33
3V3_F
C846 4.7UF 6.3V 20% X5R 0603 COMMON
C831 1UF 6.3V 10% X5R 0402 COMMON
C782 0.1UF 16V 10% X7R 0402 COMMON
C796 0.1UF 16V 10% X7R 0402 COMMON
C773 0.1UF 16V 10% X7R 0402 COMMON
NVVDD Decoupling caps. Place under GPU.
NVVDD
C713 330UF
C767 330UF
C680 330UF
C670 330UF
COMMON -35%-10% 2.5V POSCAP 3.0A 0.009R CAP_SMD_7343
4x 330uF, 7343
C742 47UF
C734 47UF
C703 47UF
C776 47UF
4V 20% X5R 0805 COMMON
4x 47uF, 0805
C747 22UF
C746 22UF
C751 22UF
C741 22UF
C752 22UF
C735 22UF
C764 22UF
C718 22UF
6.3V 20% X5R 0805 COMMON
8x 22uF, 0805
C721 1UF
C688 1UF
C754 1UF
C753 1UF
C719 1UF
C763 1UF
C720 1UF
C791 1UF
C730 1UF
C775 1UF
C761 1UF
C762 1UF
C731 1UF
C693 1UF
C798 1UF
C732 1UF
C685 1UF
C704 1UF
C765 1UF
C758 1UF
6.3V 10% X5R 1005_BGA COMMON
20x 1uF, 0402

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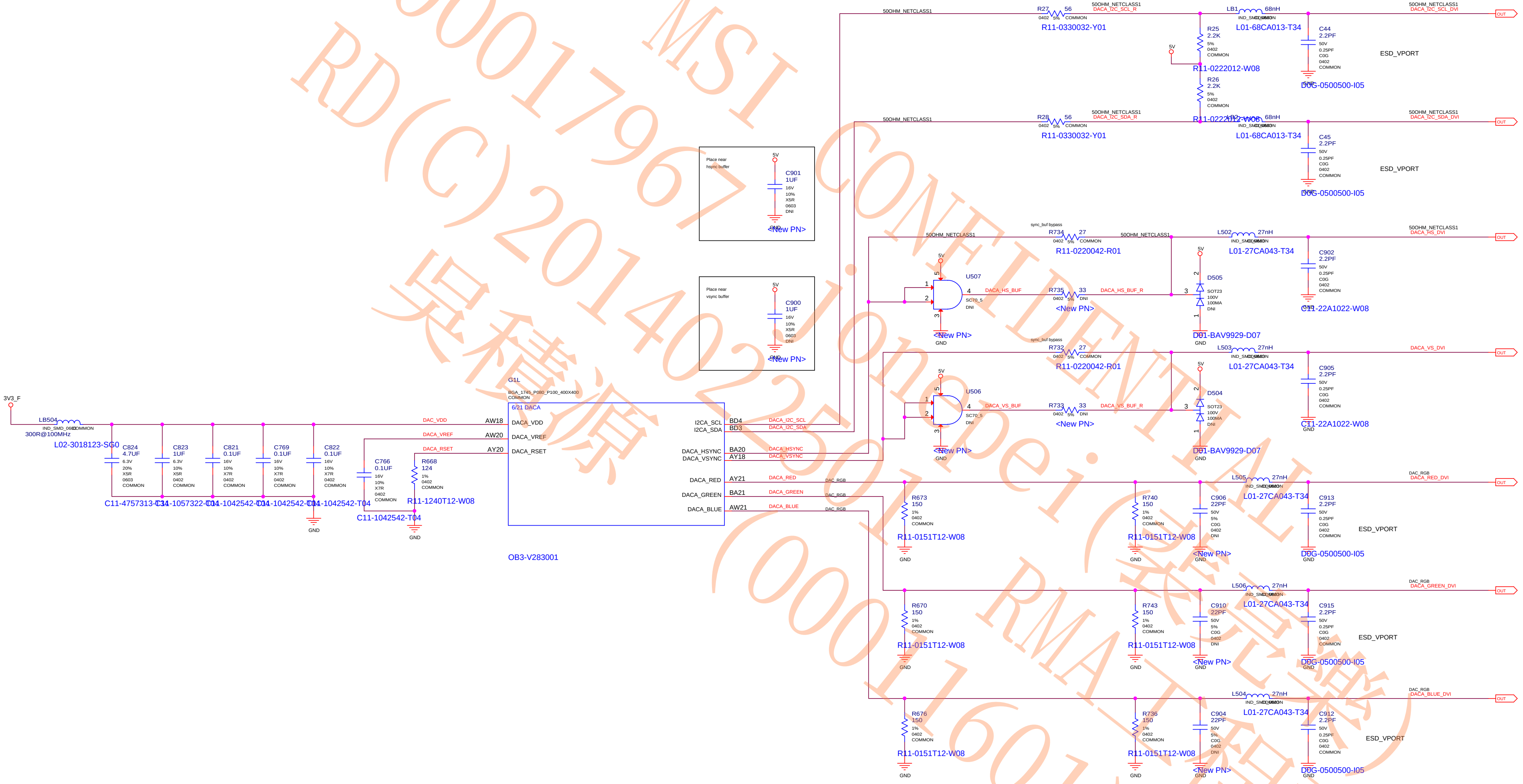
Page16: DACA Interface



3V3_F
LB504
300R@100MHz
L02-3018123-SG0
C824 4.7UF
C823 1UF
C821 0.1UF
C769 0.1UF
C822 0.1UF
C766 0.1UF
C11-4757313-T34
C11-1057322-T04
C11-1042542-T04
C11-1042542-T04
C11-1042542-T04
C11-1042542-T04
R668 124
R11-1240T12-W08
GND
DAC_VDD
DACA_VREF
DACA_RSET
G1L
6/21 DACA
AW18 DACA_VDD
AW20 DACA_VREF
AY20 DACA_RSET
I2CA_SCL BD4
I2CA_SDA BD3
DACA_HSYNC BA20
DACA_VSYNC AY18
DACA_RED AY21
DACA_GREEN BA21
DACA_BLUE AW21
OB3-V283001
Place near hsync buffer
C901 1UF
Place near vsync buffer
C900 1UF
<New PN>
50OHM_NETCLASS1
R27 56
R11-0330032-Y01
R28 56
R11-0330032-Y01
R25 2.2K
R11-0222012-W08
R26 2.2K
R11-0222012-W08
5V
LB1 68nH
L01-68CA013-T34
LB2 68nH
L01-68CA013-T34
C44 2.2PF
C45 2.2PF
D0G-0500500-I05
ESD_VPORT
DACA_I2C_SCL_DVI
DACA_I2C_SDA_DVI
sync_buf bypass
R734 27
R11-0220042-R01
R732 27
R11-0220042-R01
U507
U506
DACA_HS_BUF
DACA_VS_BUF
R735 33
R733 33
DACA_HS_BUF_R
DACA_VS_BUF_R
D505
D504
D01-BAV9929-D07
L502 27nH
L503 27nH
L01-27CA043-T34
C902 2.2PF
C905 2.2PF
C11-22A1022-W08
DACA_HS_DVI
DACA_VS_DVI
L505 27nH
L506 27nH
L504 27nH
R673 150
R670 150
R676 150
R740 150
R743 150
R736 150
R11-0151T12-W08
C906 22PF
C910 22PF
C904 22PF
C913 2.2PF
C915 2.2PF
C912 2.2PF
DAC_RGB
DACA_RED_DVI
DACA_GREEN_DVI
DACA_BLUE_DVI
OUT

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DAC_VDD	3.3V	0.25A	16MIL

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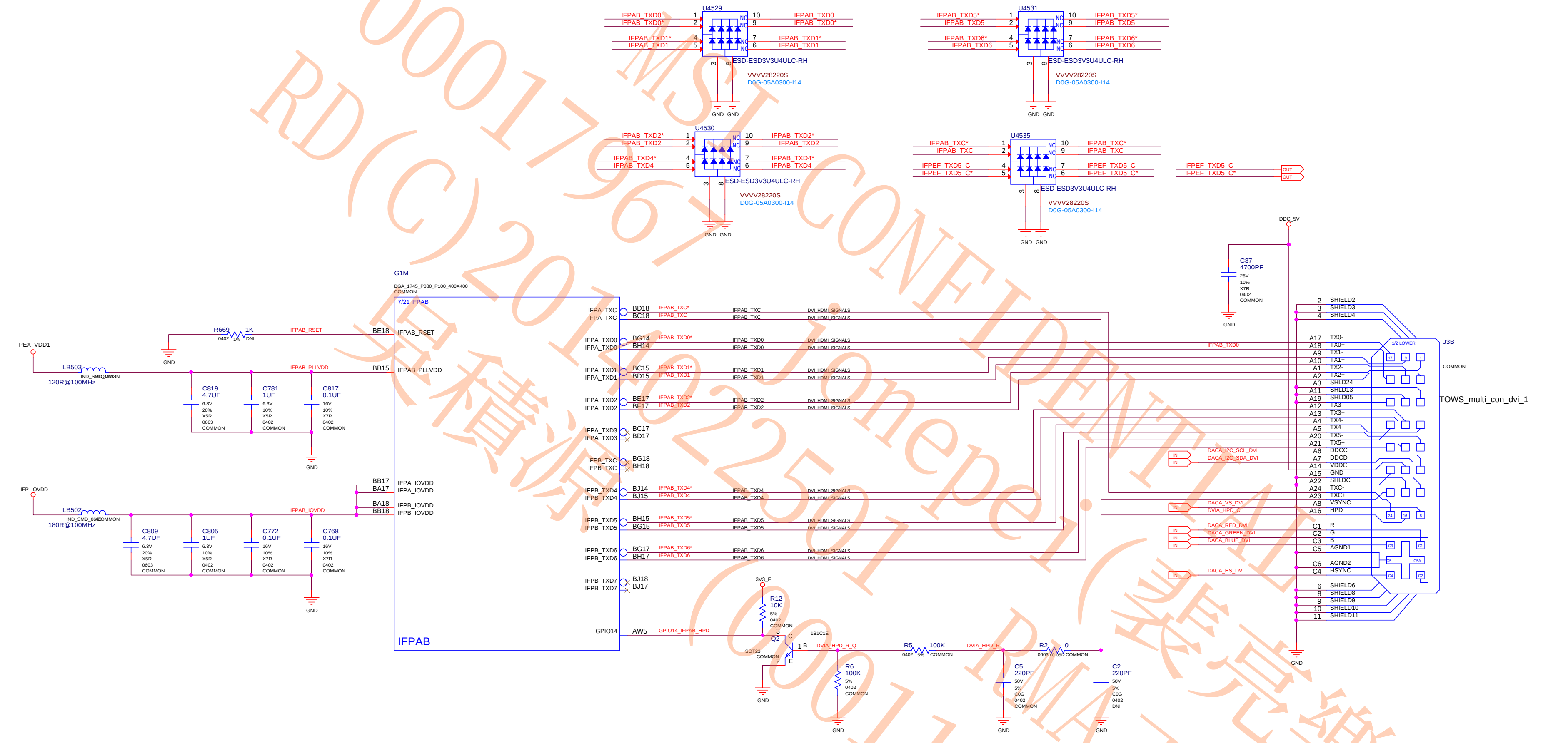
Page17: IFPAB DVI-I-DL


U4529
U4530
U4531
U4535
ESD-ESD3V3U4ULC-RH
VVVV28220S
D0G-05A0300-I14
IFPAB_TXD0
IFPAB_TXD0*
IFPAB_TXD1
IFPAB_TXD1*
IFPAB_TXD2
IFPAB_TXD2*
IFPAB_TXD4
IFPAB_TXD4*
IFPAB_TXD5
IFPAB_TXD5*
IFPAB_TXD6
IFPAB_TXD6*
IFPAB_TXC
IFPAB_TXC*
IFPEF_TXD5_C
IFPEF_TXD5_C*
GND
G1M
BGA_1745_P080_P100_400X400
7/21 IFPAB
IFPAB_RSET
IFPAB_PLLVDD
IFPA_IOVDD
IFPB_IOVDD
GPIO14
IFPAB
PEX_VDD1
IFP_IOVDD
R669 1K
LB503 120R@100MHz
LB502 180R@100MHz
C819 4.7UF
C781 1UF
C817 0.1UF
C809 4.7UF
C805 1UF
C772 0.1UF
C768 0.1UF
C37 4700PF
DDC_5V
3V3_F
R12 10K
Q2
R6 100K
R5 100K
R2 0
C5 220PF
C2 220PF
GPIO14_IFPAB_HPD
DVIA_HPD_R_Q
DVIA_HPD_R
DVI_HDMI_SIGNALS
DACA_I2C_SCL_DVI
DACA_I2C_SDA_DVI
DACA_VS_DVI
DVIA_HPD_C
DACA_RED_DVI
DACA_GREEN_DVI
DACA_BLUE_DVI
DACA_HS_DVI
J3B
TOWS_multi_con_dvi_1

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Size: Custom	Document Description: 17: IFPAB DVI-I-DL		Rev: 40
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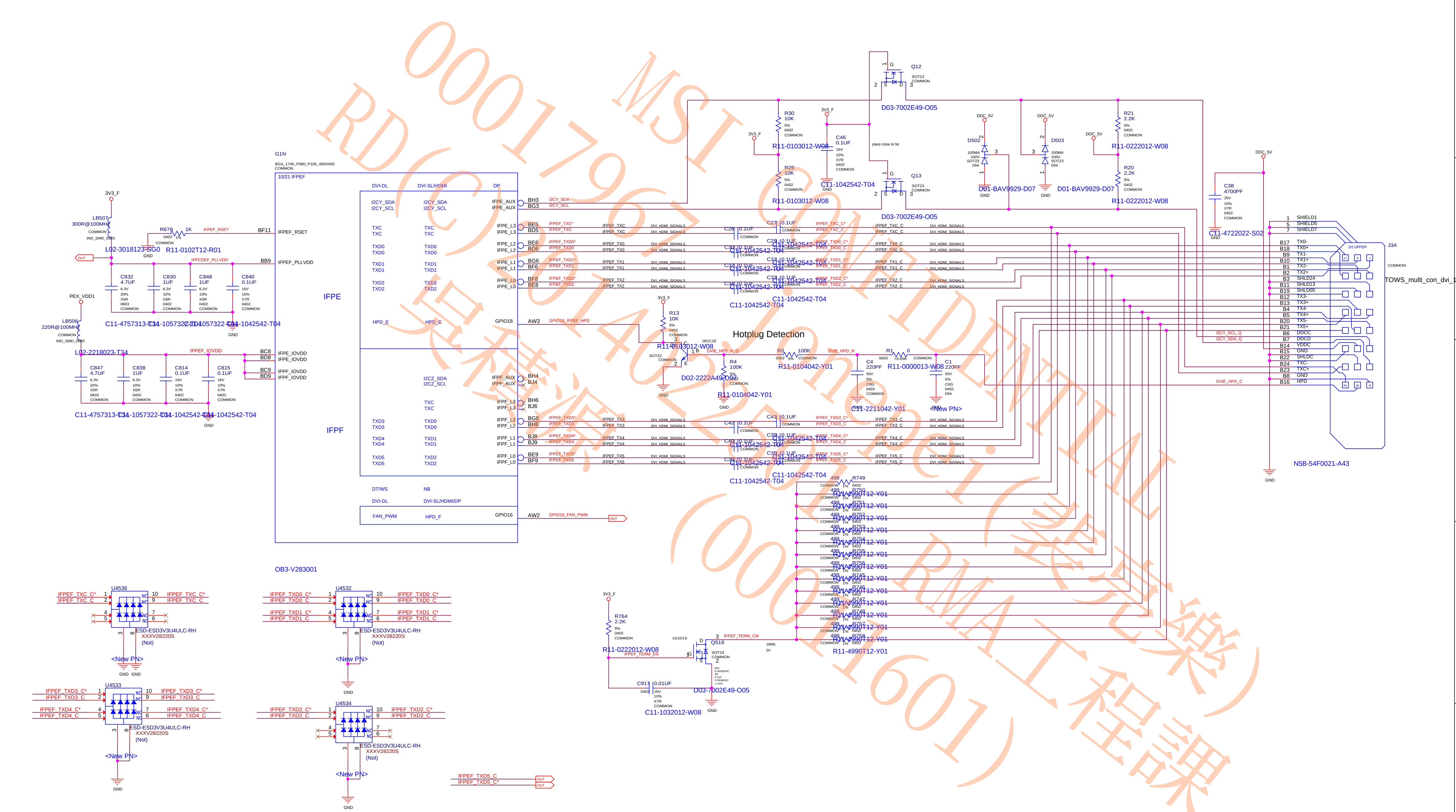
Page18: IFPEF DVI-D-DL



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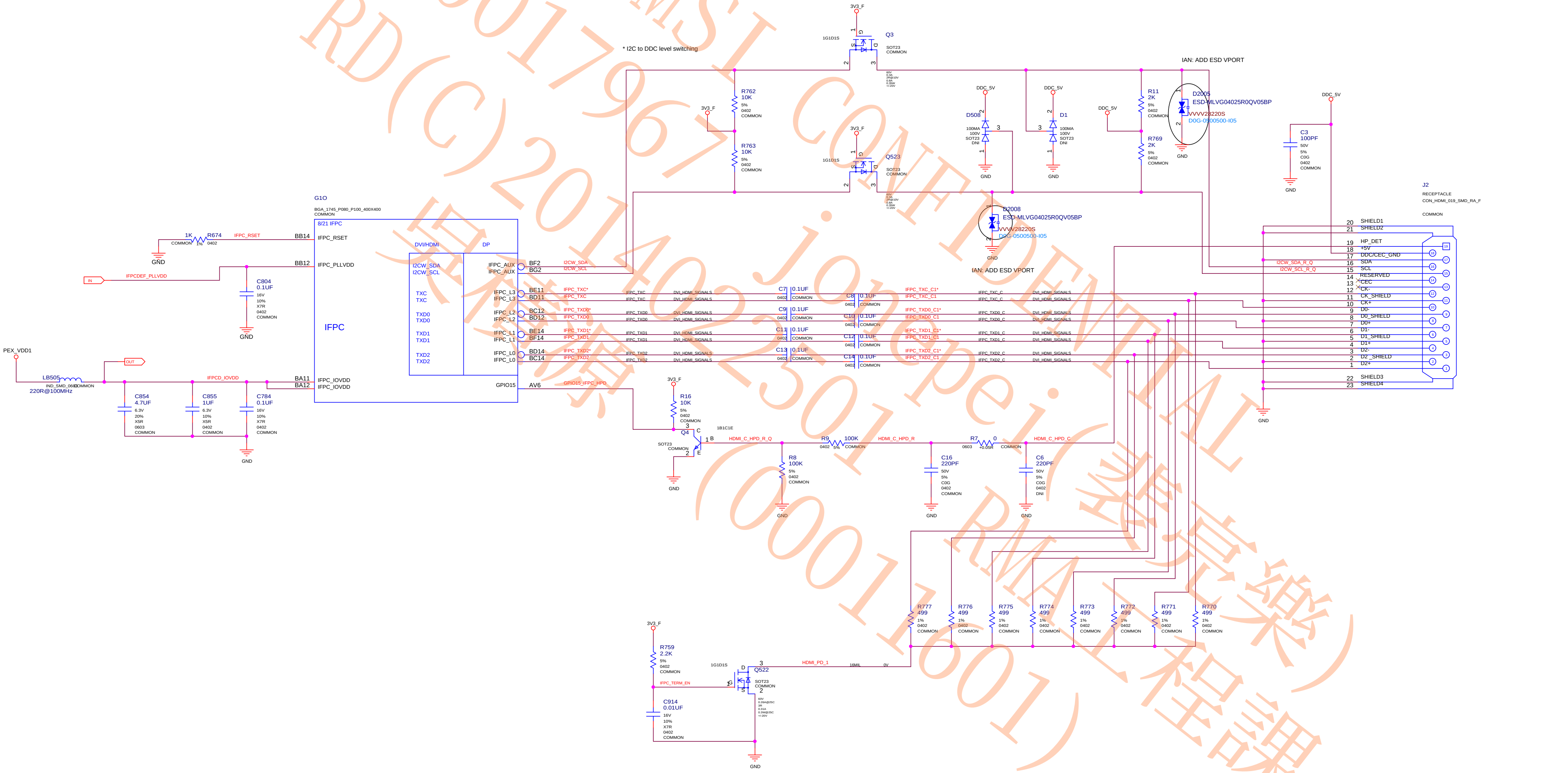
Page19: IFPC HDMI



* I2C to DDC level switching
IAN: ADD ESD VPORT
G1O
BGA_1745_P080_P100_400X400
COMMON
8/21 IFPC
IFPC
IFPC_RSET
IFPC_PLLVDD
IFPC_IOVDD
DVI/HDMI
DP
I2CW_SDA
I2CW_SCL
IFPC_AUX
TXC
TXD0
TXD1
TXD2
IFPC_L3
IFPC_L2
IFPC_L1
IFPC_L0
GPIO15
AV6
PEX_VDD1
LB505
220R@100MHz
IFPCDEF_PLLVDD
IFPCD_IOVDD
C854 4.7UF
C855 1UF
C784 0.1UF
C804 0.1UF
R674 1K
Q3
Q523
Q4
Q522
R762 10K
R763 10K
R11 2K
R769 2K
R16 10K
R8 100K
R9 100K
R7 0
R759 2.2K
C914 0.01UF
C16 220PF
C6 220PF
C3 100PF
D508
D1
D2005
D2008
ESD-MLVG04025R0QV05BP
D0G-0500500-I05
R777 499
R776 499
R775 499
R774 499
R773 499
R772 499
R771 499
R770 499
HDMI_C_HPD_R_Q
HDMI_C_HPD_R
HDMI_C_HPD_C
HDMI_PD_1
IFPC_TERM_EN
J2
RECEPTACLE
CON_HDMI_019_SMD_RA_F
SHIELD1
SHIELD2
HP_DET
+5V
DDC/CEC_GND
SDA
SCL
RESERVED
CEC
CK-
CK_SHIELD
CK+
D0-
D0_SHIELD
D0+
D1-
D1_SHIELD
D1+
D2-
D2_SHIELD
D2+
SHIELD3
SHIELD4
3V3_F
DDC_5V
GND

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Size: Custom	Document Description: 19: IFPC HDMI	Rev: 40
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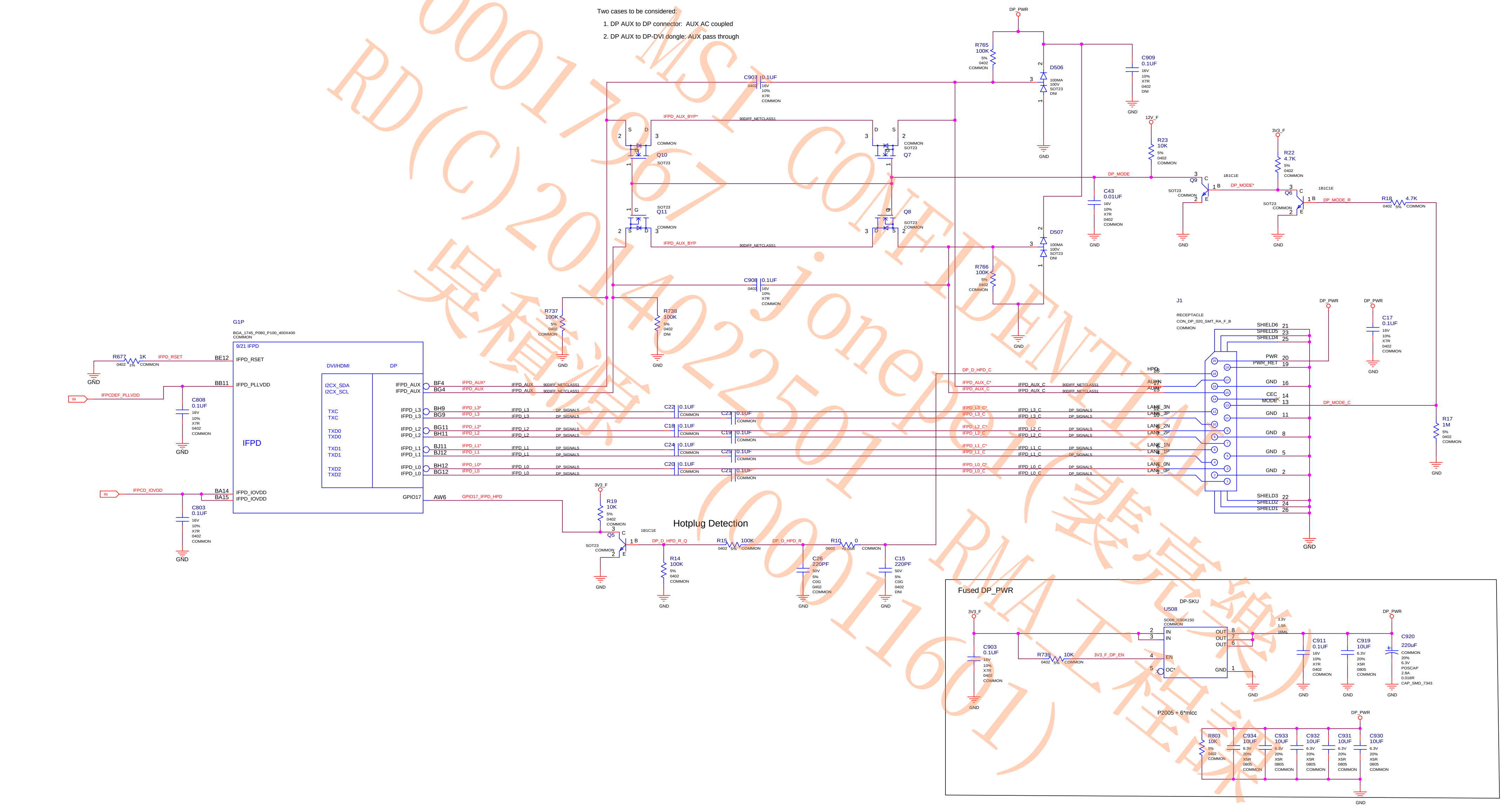
Page20: IFPD DP



Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through
G1P
BGA_1745_P080_P100_400X400
9/21 IFPD
IFPD
IFPD_RSET
IFPD_PLLVDD
IFPD_IOVDD
DVI/HDMI
DP
I2CX_SDA
I2CX_SCL
TXC
TXD0
TXD1
TXD2
IFPD_AUX
IFPD_L3
IFPD_L2
IFPD_L1
IFPD_L0
GPIO17
IFPCDEF_PLLVDD
IFPCD_IOVDD
IFPD_AUX_BYP*
IFPD_AUX_BYP
90DIFF_NETCLASS1
DP_SIGNALS
DP_PWR
DP_MODE
DP_MODE*
DP_MODE_R
DP_MODE_C
DP_D_HPD_C
IFPD_AUX_C
GPIO17_IFPD_HPD
Hotplug Detection
J1
RECEPTACLE
CON_DP_020_SMT_RA_F_B
HPD
AUXN
AUXP
CEC
MODE
PWR
PWR_RET
Fused DP_PWR
DP-SKU
U508
3V3_F_DP_EN
P2005 + 6*mlcc
12V_F
3V3_F
GND

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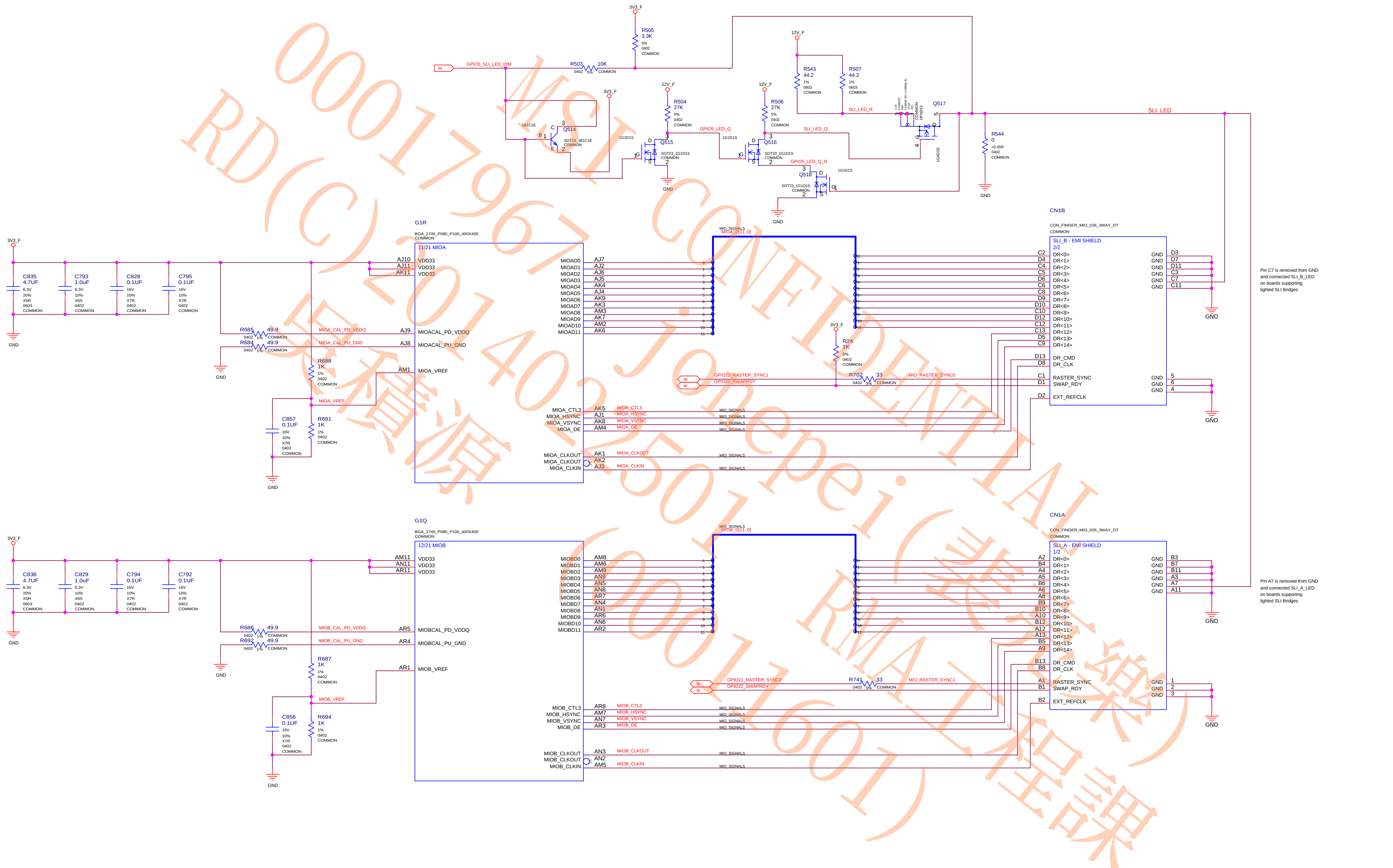
Page21: MIOA/B Interface



SLI LED (GEFORCE ONLY)
3V3_F
R505 3.3K 5% 0402 COMMON
GPIO5_SLI_LED_DIM
R503 10K
12V_F
R543 44.2 1% 0603 COMMON
R507 44.2 1% 0603 COMMON
SLI_LED_R
Q517
SLI_LED
R544 0
Q514
R504 27K 5% 0402 COMMON
GPIO5_LED_Q
Q515
R506 27K 5% 0402 COMMON
SLI_LED_Q
Q516
GPIO5_LED_Q_N
Q518
GND
G1R
BGA_1745_P080_P100_400X400 COMMON
11/21 MIOA
VDD33
MIOACAL_PD_VDDQ
MIOACAL_PU_GND
MIOA_VREF
MIOAD0
MIOAD1
MIOAD2
MIOAD3
MIOAD4
MIOAD5
MIOAD6
MIOAD7
MIOAD8
MIOAD9
MIOAD10
MIOAD11
MIOA_CTL3
MIOA_HSYNC
MIOA_VSYNC
MIOA_DE
MIOA_CLKOUT
MIOA_CLKOUT
MIOA_CLKIN
C835 4.7UF
C793 1.0uF
C828 0.1UF
C795 0.1UF
R685 49.9
R684 49.9
R688 1K
C857 0.1UF
R691 1K
MIOA_CAL_PD_VDDQ
MIOA_CAL_PU_GND
MIOA_VREF
MIO_SIGNALS
MIOA_D[11..0]
CN1B
CON_FINGER_MIO_026_3WAY_DT COMMON
SLI_B - EMI SHIELD 2/2
DR<0>
DR<1>
DR<2>
DR<3>
DR<4>
DR<5>
DR<6>
DR<7>
DR<8>
DR<9>
DR<10>
DR<11>
DR<12>
DR<13>
DR<14>
DR_CMD
DR_CLK
RASTER_SYNC
SWAP_RDY
EXT_REFCLK
R24 1K
GPIO23_RASTER_SYNC1
GPIO22_SWAPRDY
R702 33
MIO_RASTER_SYNC0
Pin C7 is removed from GND and connected SLI_B_LED on boards supporting lighted SLI Bridges
G1Q
BGA_1745_P080_P100_400X400 COMMON
12/21 MIOB
MIOBCAL_PD_VDDQ
MIOBCAL_PU_GND
MIOB_VREF
MIOBD0
MIOBD1
MIOBD2
MIOBD3
MIOBD4
MIOBD5
MIOBD6
MIOBD7
MIOBD8
MIOBD9
MIOBD10
MIOBD11
MIOB_CTL3
MIOB_HSYNC
MIOB_VSYNC
MIOB_DE
MIOB_CLKOUT
MIOB_CLKOUT
MIOB_CLKIN
C836 4.7UF
C829 1.0uF
C794 0.1UF
C792 0.1UF
R686 49.9
R692 49.9
R687 1K
C856 0.1UF
R694 1K
MIOB_CAL_PD_VDDQ
MIOB_CAL_PU_GND
MIOB_VREF
MIOB_D[11..0]
CN1A
CON_FINGER_MIO_026_3WAY_DT COMMON
SLI_A - EMI SHIELD 1/2
GPIO21_RASTER_SYNC0
GPIO22_SWAPRDY
R741 33
MIO_RASTER_SYNC1
Pin A7 is removed from GND and connected SLI_A_LED on boards supporting lighted SLI Bridges

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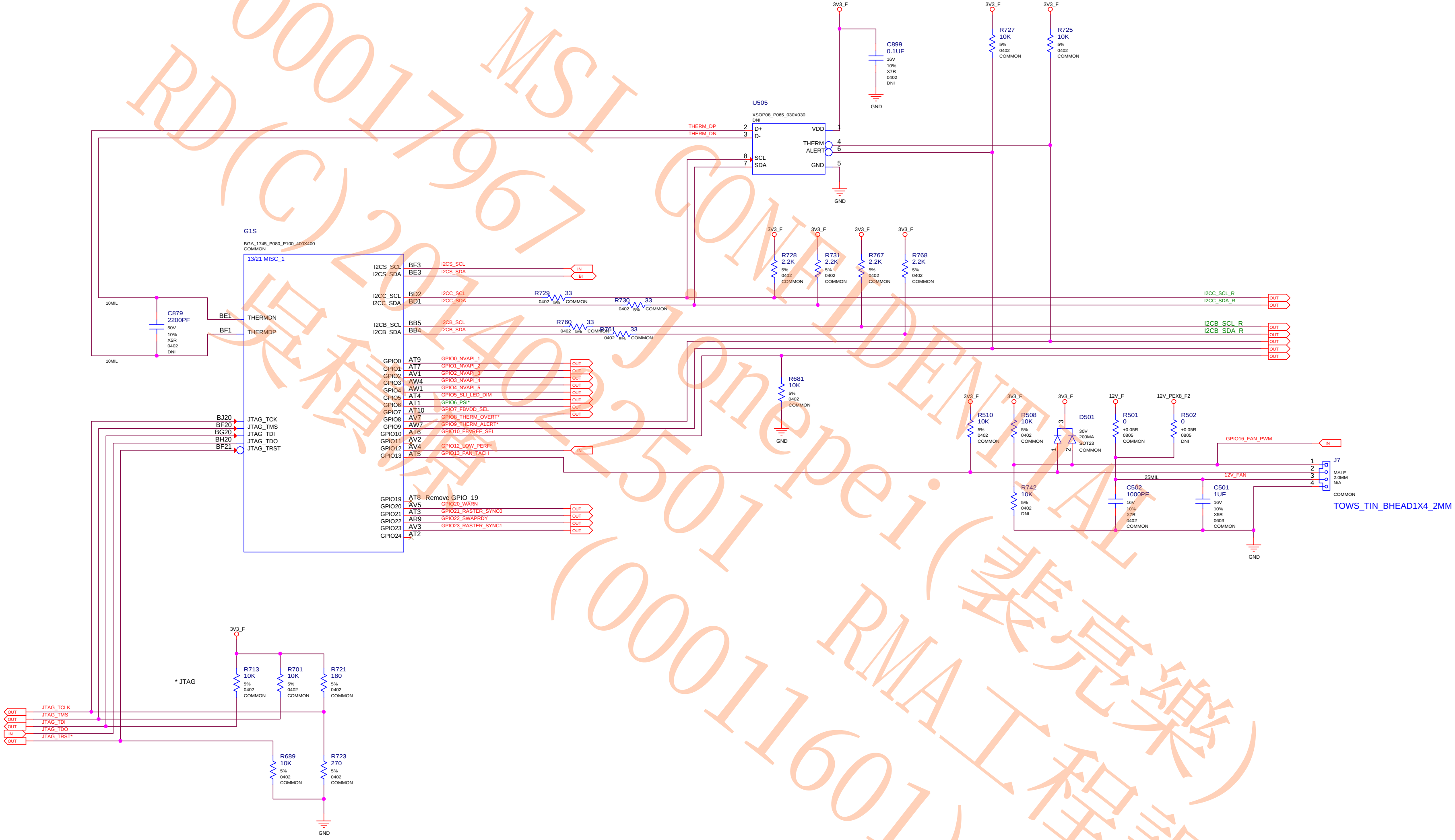
Page22: MISC1: Fan, Thermal, JTAG, GPIO



U505
XSOP08_P065_030X030
DNI
THERM_DP
THERM_DN
D+
D-
VDD
THERM
ALERT
SCL
SDA
GND
3V3_F
C899
0.1UF
R727
10K
R725
10K
G1S
BGA_1745_P080_P100_400X400
COMMON
13/21 MISC_1
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
THERMDN
THERMDP
C879
2200PF
R729
33
R730
33
R760
33
R761
33
R728
2.2K
R731
2.2K
R767
2.2K
R768
2.2K
I2CC_SCL_R
I2CC_SDA_R
I2CB_SCL_R
I2CB_SDA_R
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST
GPIO0_NVAPI_1
GPIO1_NVAPI_2
GPIO2_NVAPI_3
GPIO3_NVAPI_4
GPIO4_NVAPI_5
GPIO5_SLI_LED_DIM
GPIO6_PSI*
GPIO7_FBVDD_SEL
GPIO8_THERM_OVERT*
GPIO9_THERM_ALERT*
GPIO10_FBVREF_SEL
GPIO12_LOW_PERF*
GPIO13_FAN_TACH
Remove GPIO_19
GPIO20_WARN
GPIO21_RASTER_SYNC0
GPIO22_SWAPRDY
GPIO23_RASTER_SYNC1
R681
10K
R510
10K
R508
10K
D501
R501
0
R502
0
12V_F
12V_PEX8_F2
GPIO16_FAN_PWM
R742
10K
C502
1000PF
C501
1UF
12V_FAN
J7
TOWS_TIN_BHEAD1X4_2MM
GND
* JTAG
JTAG_TCLK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST*
R713
10K
R701
10K
R721
180
R689
10K
R723
270

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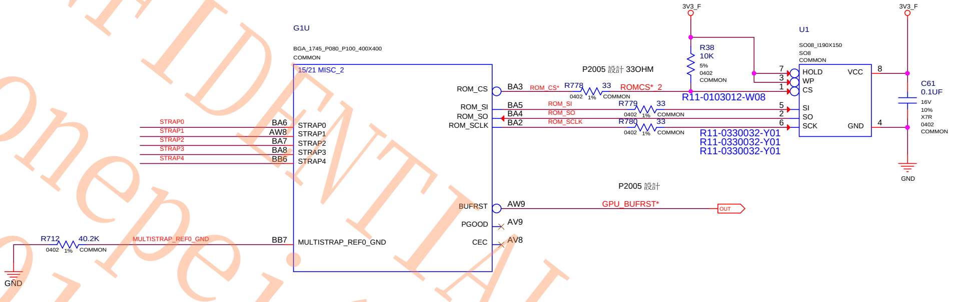
Page23: MISC2: ROM, XTAL, Straps

Strap	Function	Value	Note	Pull
STRAP0	USER_BIT [3:0]*	0000*		5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*		5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0000 - (0x1180)*		5K PD -400 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*		45K PU*
STRAP4	DP_PLL_VDD_33V*	1*	FOR 3_3V*	45K PD*
	PEX_MAX_SPEED*	1*	FOR GEN2/3*	
	PEX_SPD_CHANGE_GEN3*	1*	ENABLED*	
	*			
ROM_SI	RAMCFG[0]*	0*		35K PD* (0110 for 64Mx32 256 bit Hynix for SKU 0 primary memory)
	RAMCFG[1]*	1*		
	RAMCFG[2]*	1*		
	RAMCFG[3]*	0*		
ROM_SO	VGA_DEVICE*	1*		10k PU*
	SMB_ALT_ADDR*	0*		
	FB[0]_APERTURE_SIZE*	0*	For 256MB*	
	FB[1]_APERTURE_SIZE*	1*	For 256MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0*	DISABLED*	25K PD*
	PCI_DEVID_EXT[5]*	0*	For 0x1180*	
	SUB_VENDOR*	1*	Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0*	For 0x1180*	

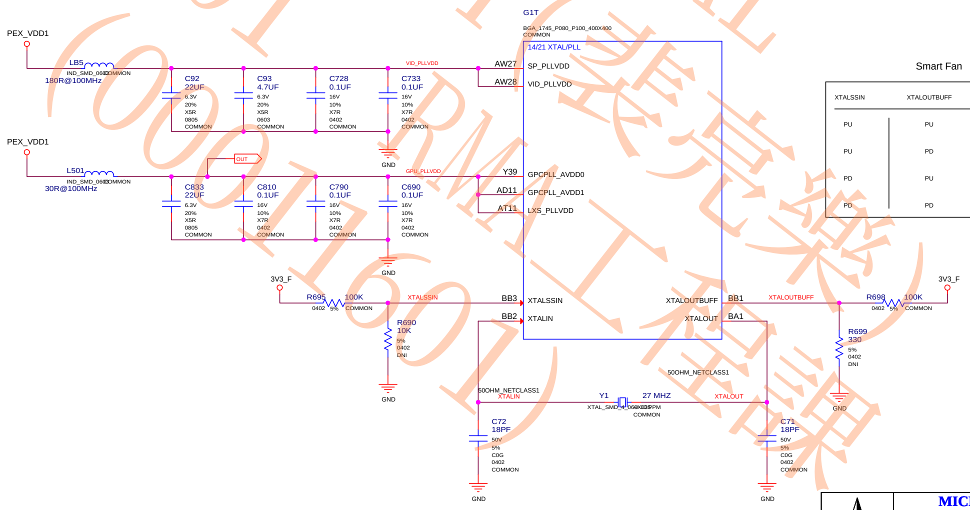
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0]	Config Width Vendor
0000	Reserved
0001	32Mx32 256-bit Elpida
0010	32Mx32 256-bit Hynix
0011	32Mx32 256-bit Samsung
0100	Reserved
0101	64Mx32 256-bit Elpida
0110	64Mx32 256-bit Hynix
0111	64Mx32 256-bit Samsung
1000	Reserved
1001	32Mx32 192-bit Elpida
1010	32Mx32 192-bit Hynix
1011	32Mx32 192-bit Samsung
1100	Reserved
1101	64Mx32 192-bit Elpida
1110	64Mx32 192-bit Hynix
1111	64Mx32 192-bit Samsung

Remove Dual Bios

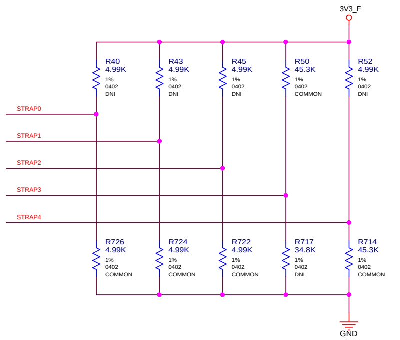


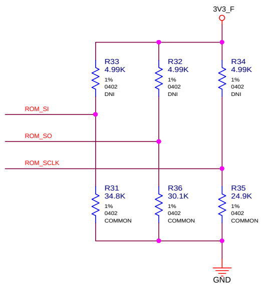
	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND



Smart Fan

XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)





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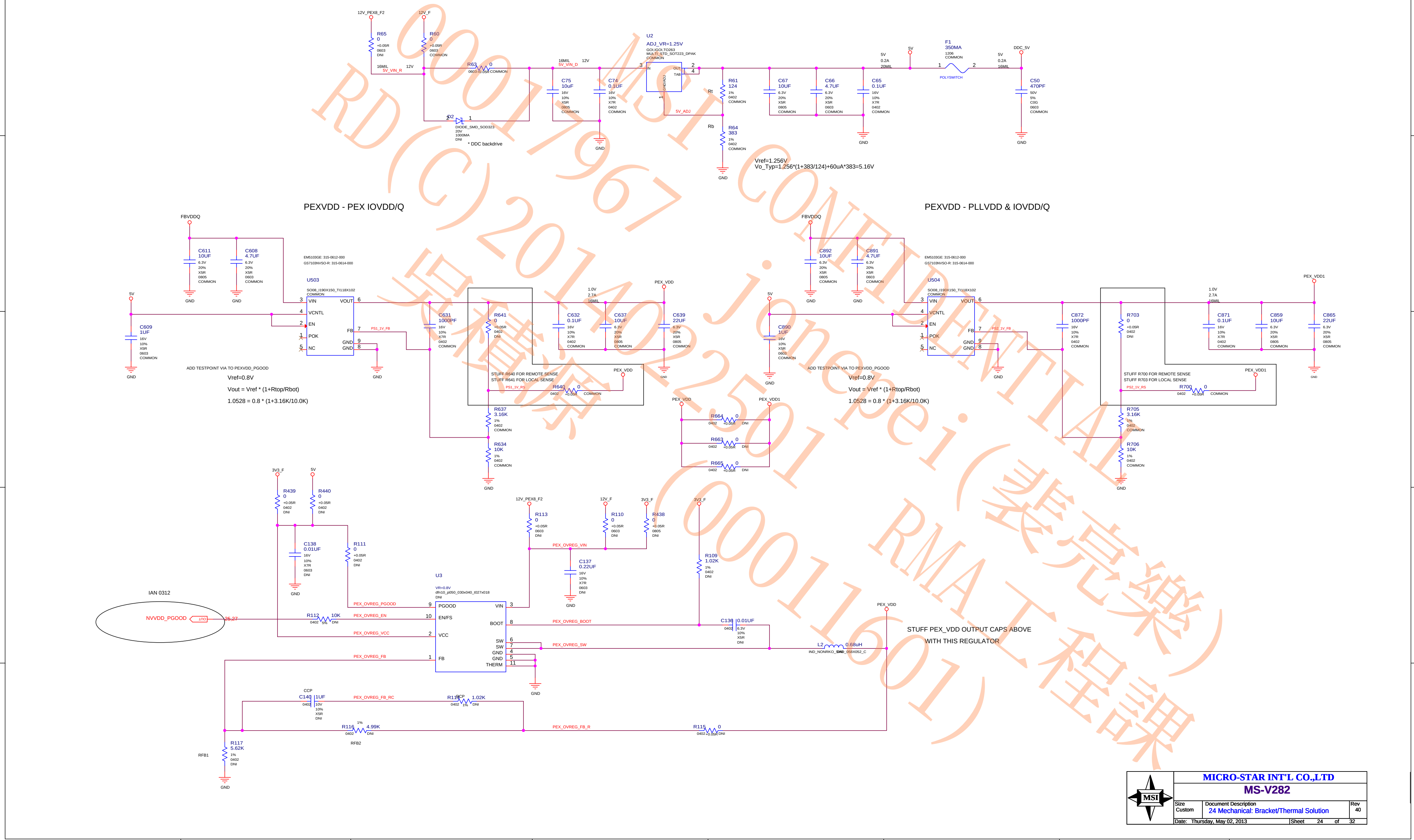
Page24: PS: 5V, PEX_VDD



12V_PEX8_F2
12V_F
R65 0
R60 0
R63 0
5V_VIN_R
5V_VIN_D
D2
DIODE_SMD_SOD323
* DDC backdrive
C75 10uF
C74 0.1UF
U2
ADJ_VR=1.25V
Rt
Rb
5V_ADJ
R61 124
R64 383
C67 10UF
C66 4.7UF
C65 0.1UF
F1 350MA
POLYSWITCH
DDC_5V
C50 470PF
Vref=1.256V
Vo_Typ=1.256*(1+383/124)+60uA*383=5.16V
PEXVDD - PEX IOVDD/Q
PEXVDD - PLLVDD & IOVDD/Q
FBVDDQ
C611 10UF
C608 4.7UF
U503
VIN
VOUT
VCNTL
EN
POK
NC
FB
GND
C609 1UF
C631 1000PF
R641 0
C632 0.1UF
C637 10UF
C639 22UF
PEX_VDD
ADD TESTPOINT VIA TO PEXVDD_PGOOD
Vref=0.8V
Vout = Vref * (1+Rtop/Rbot)
1.0528 = 0.8 * (1+3.16K/10.0K)
STUFF R640 FOR REMOTE SENSE
STUFF R641 FOR LOCAL SENSE
R640 0
R637 3.16K
R634 10K
R664 0
R663 0
R665 0
PEX_VDD1
U504
C892 10UF
C891 4.7UF
C890 1UF
C872 1000PF
R703 0
C871 0.1UF
C859 10UF
C865 22UF
STUFF R700 FOR REMOTE SENSE
STUFF R703 FOR LOCAL SENSE
R700 0
R705 3.16K
R706 10K
3V3_F
R439 0
R440 0
C138 0.01UF
R111 0
R113 0
R110 0
R438 0
PEX_OVREG_VIN
C137 0.22UF
R109 1.02K
IAN 0312
NVVDD_PGOOD
U3
PGOOD
EN/FS
VCC
FB
VIN
BOOT
SW
THERM
PEX_OVREG_PGOOD
PEX_OVREG_EN
PEX_OVREG_VCC
PEX_OVREG_FB
PEX_OVREG_BOOT
PEX_OVREG_SW
R112 10K
C139 0.01UF
L2 0.68uH
STUFF PEX_VDD OUTPUT CAPS ABOVE
WITH THIS REGULATOR
C140 1UF
PEX_OVREG_FB_RC
R114 1.02K
R116 4.99K
PEX_OVREG_FB_R
R115 0
R117 5.62K
RFB1
RFB2
GND
MICRO-STAR INT'L CO.,LTD
MS-V282
Size Custom
Document Description
24 Mechanical: Bracket/Thermal Solution
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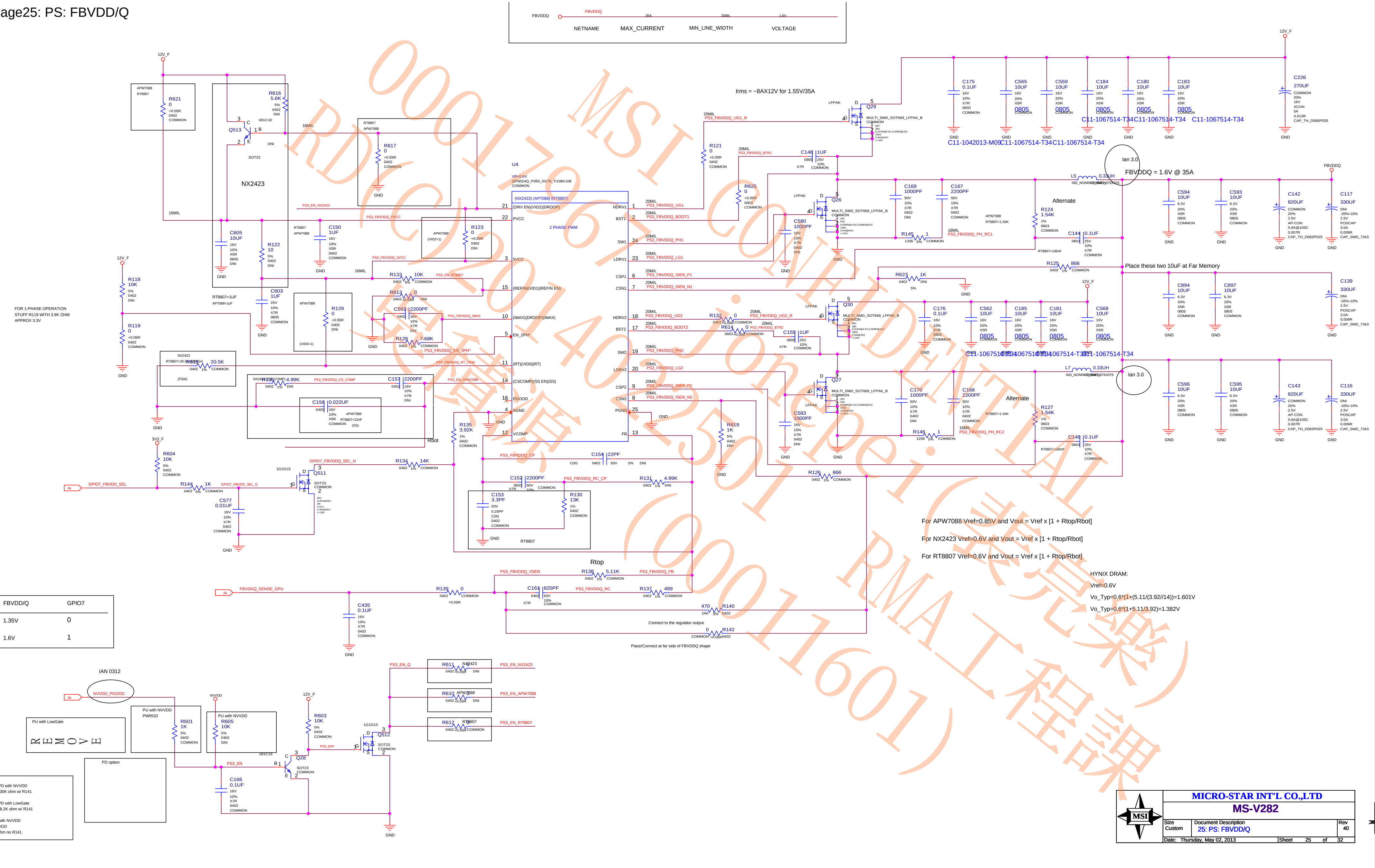
Page25: PS: FBVDD/Q



FBVDDQ
NETNAME
MAX_CURRENT
MIN_LINE_WIDTH
VOLTAGE
35A
20MIL
1.6V
12V_F
3V3_F
FBVDDQ = 1.6V @ 35A
Place these two 10uF at Far Memory
U4
NX2423
APW7088
RT8807
Q513
Q511
Q512
Q28
Q29
Q26
Q30
Q27
L5
L7
Alternate
Rtop
Rbot
GPIO7_FBVDD_SEL
FBVDDQ_SENSE_GPU
NVVDD_PGOOD
Connect to the regulator output
Place/Connect at far side of FBVDDQ shape
PU with LowGate
PU with NVVDD PWRGD
PU with NVVDD
PD option
IAN 0312
REMOVE
PU/PD with NVVDD 10K/30K ohm w/ R141
PU/PD with LowGate 30K/8.2K ohm w/ R141
PU with NVVDD PWRGD 1K ohm no R141
FOR 1-PHASE OPERATION STUFF R119 WITH 3.9K OHM APPROX 3.3V

Irms = ~8AX12V for 1.55V/35A

FBVDD/Q	GPIO7
1.35V	0
1.6V	1

For APW7088 Vref=0.85V and Vout = Vref x [1 + Rtop/Rbot]

For NX2423 Vref=0.6V and Vout = Vref x [1 + Rtop/Rbot]

For RT8807 Vref=0.6V and Vout = Vref x [1 + Rtop/Rbot]

HYNIX DRAM:

Vref=0.6V

Vo_Typ=0.6*(1+(5.11/(3.92//14))=1.601V

Vo_Typ=0.6*(1+5.11/3.92)=1.382V

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Page26: PS: NVVDD Controller

VID Table

GPIO7	GPIO6	GPIO5	GPIO2	GPIO17	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

PSI intended for lower power states
switching from 5 phases down to 1 or 2 phases
PSI DRVON enabled for either 3 or 4 phases

*NTC resistor 1s a placeholder

REMOVE V282-1.0 NVVDD PWM

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V282	
Size: Custom	Document Description: Page26: PS: NVVDD Controller	Rev: 40
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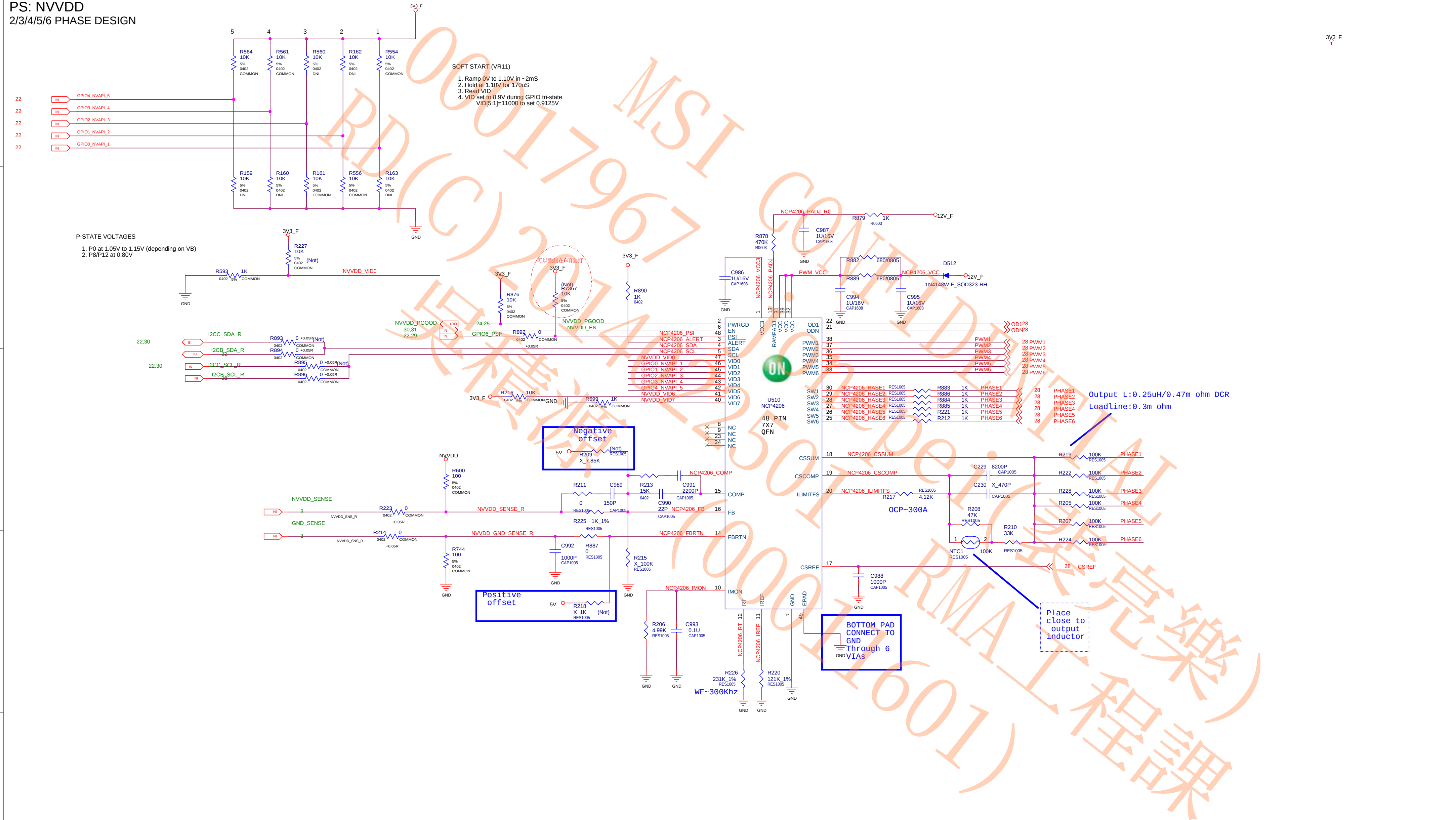
PS: NVVDD

2/3/4/5/6 PHASE DESIGN



SOFT START (VR11)
1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPIO tri-state
VID[5:1]=11000 to set 0.9125V
P-STATE VOLTAGES
1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V
GPIO4_NVAPI_5
GPIO3_NVAPI_4
GPIO2_NVAPI_3
GPIO1_NVAPI_2
GPIO0_NVAPI_1
NVVDD_VID0
NVVDD_PGOOD
NVVDD_EN
I2CC_SDA_R
I2CB_SDA_R
I2CC_SCL_R
I2CB_SCL_R
GPIO6_PSI*
U510
NCP4206
48 PIN
7X7
QFN
Negative offset
Positive offset
NVVDD_SENSE
GND_SENSE
NVVDD_SENSE_R
NVVDD_GND_SENSE_R
Output L:0.25uH/0.47m ohm DCR
Loadline:0.3m ohm
OCP~300A
WF~300Khz
BOTTOM PAD CONNECT TO GND Through 6 VIAs
Place close to output inductor
D512
1N4148W-F_SOD323-RH
12V_F
3V3_F
PHASE1
PHASE2
PHASE3
PHASE4
PHASE5
PHASE6
PWM1
PWM2
PWM3
PWM4
PWM5
PWM6
CSREF

MICRO-STAR INT'L CO.,LTD

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Custom	25_PS_ NVVDD Supply	40

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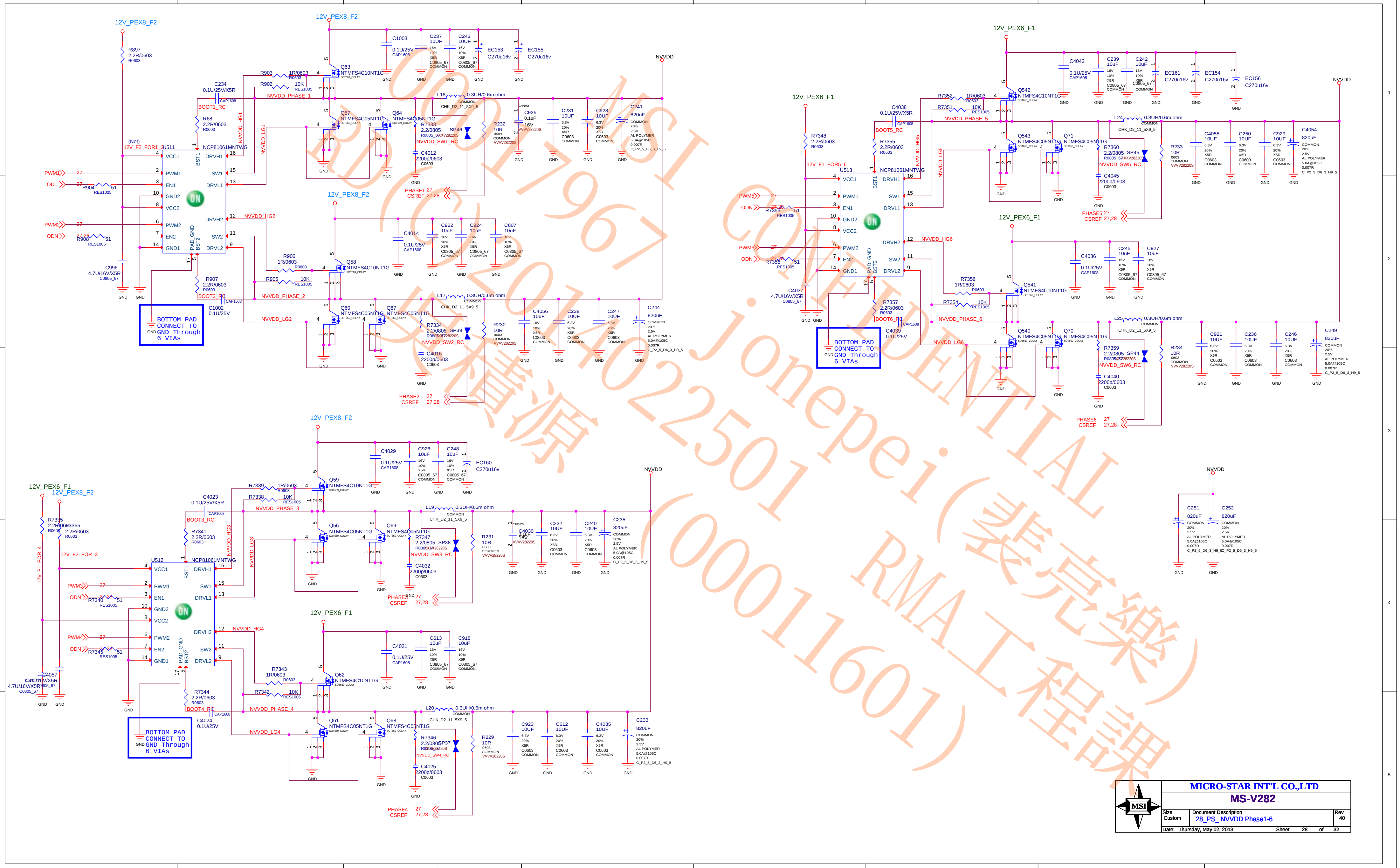
12V_PEX8_F2
12V_PEX6_F1
NVVDD
NCP81061MNTWG
U511
U512
U513
VCC1
PWM1
EN1
GND2
VCC2
PWM2
EN2
GND1
BST1
DRVH1
SW1
DRVL1
DRVH2
SW2
DRVL2
PAD_GND
BST2
BOTTOM PAD CONNECT TO GND Through 6 VIAs
NTMFS4C10NT1G
NTMFS4C05NT1G
NVVDD_PHASE_1
NVVDD_PHASE_2
NVVDD_PHASE_3
NVVDD_PHASE_4
NVVDD_PHASE_5
NVVDD_PHASE_6
NVVDD_HG1
NVVDD_LG1
NVVDD_HG2
NVVDD_LG2
NVVDD_HG3
NVVDD_LG3
NVVDD_HG4
NVVDD_LG4
NVVDD_HG5
NVVDD_LG5
NVVDD_HG6
NVVDD_LG6
NVVDD_SW1_RC
NVVDD_SW2_RC
NVVDD_SW3_RC
NVVDD_SW4_RC
NVVDD_SW5_RC
NVVDD_SW6_RC
0.3UH/0.6m ohm
CHK_D2_11_5X9_5
PHASE1 27
PHASE2 27
PHASE3 27
PHASE4 27
PHASE5 27
PHASE6 27
CSREF 27,28
PWM1
PWM2
PWM3
PWM4
PWM5
PWM6
OD1
ODN
GND
820uF
C270u16v
12V_F2_FOR1_1
12V_F2_FOR_3
12V_F1_FOR_4
12V_F1_FOR5_6
MICRO-STAR INT'L CO.,LTD
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Document Description 28_PS_NVVDD Phase1-6
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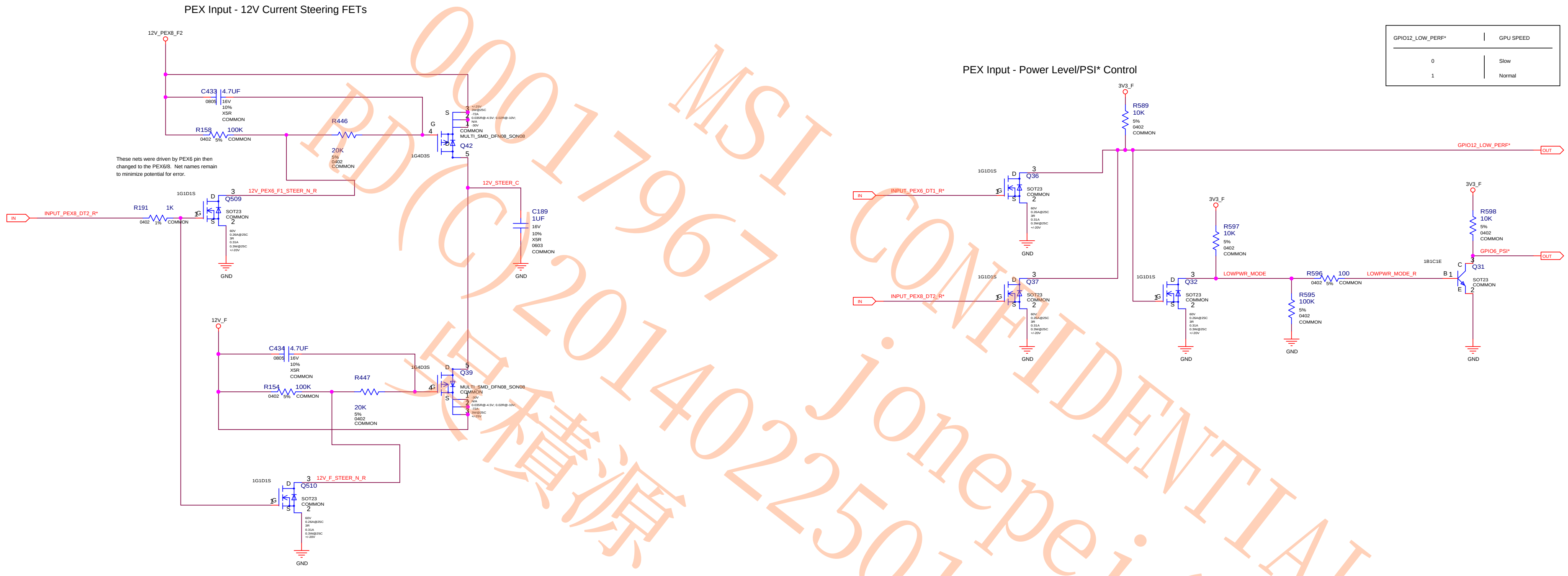
Page29: PS: 12V Current Steering, PSI Control, and LED

GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal



PEX Input - 12V Current Steering FETs
12V_PEX8_F2
C433 4.7UF 0805 16V 10% X5R COMMON
R158 100K 0402 5% COMMON
R446 20K 5% 0402 COMMON
Q42 MULTI_SMD_DFN08_SON08 COMMON
1G4D3S
These nets were driven by PEX6 pin then changed to the PEX6/8. Net names remain to minimize potential for error.
12V_PEX6_F1_STEER_N_R
INPUT_PEX8_DT2_R*
R191 1K 0402 1% COMMON
Q509 SOT23 COMMON
1G1D1S
GND
12V_STEER_C
C189 1UF 16V 10% X5R 0603 COMMON
12V_F
C434 4.7UF 0805 16V 10% X5R COMMON
R154 100K 0402 5% COMMON
R447 20K 5% 0402 COMMON
Q39 MULTI_SMD_DFN08_SON08 COMMON
12V_F_STEER_N_R
Q510 SOT23 COMMON
PEX Input - Power Level/PSI* Control
3V3_F
R589 10K 5% 0402 COMMON
GPIO12_LOW_PERF*
INPUT_PEX6_DT1_R*
Q36 SOT23 COMMON
INPUT_PEX8_DT2_R*
Q37 SOT23 COMMON
R597 10K 5% 0402 COMMON
Q32 SOT23 COMMON
LOWPWR_MODE
R596 100 0402 5% COMMON
LOWPWR_MODE_R
R595 100K 5% 0402 COMMON
R598 10K 5% 0402 COMMON
GPIO6_PSI*
Q31 SOT23 COMMON
1B1C1E
IN
OUT

REMOVE GeForce Logo LED

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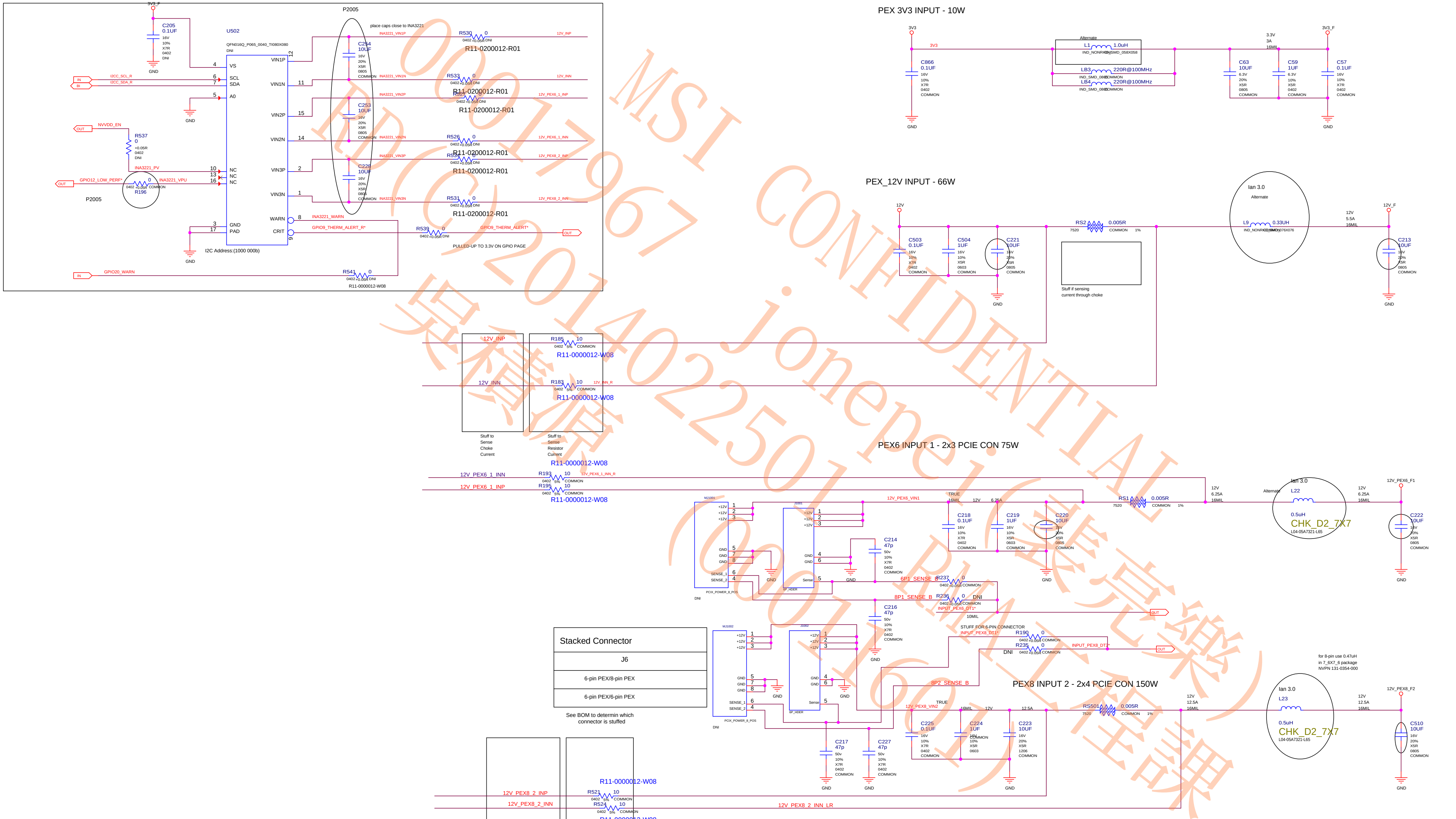

P2005
U502
QFN016Q_P065_0040_TI080X080
DNI
place caps close to INA3221
VS
SCL
SDA
A0
VIN1P
VIN1N
VIN2P
VIN2N
VIN3P
VIN3N
NC
GND
PAD
WARN
CRIT
C205
0.1UF
C254
10UF
C253
10UF
C228
10UF
R530
R533
R526
R531
R537
R196
R539
R541
R11-0200012-R01
R11-0000012-W08
INA3221_WARN
GPIO9_THERM_ALERT_R*
GPIO9_THERM_ALERT*
GPIO20_WARN
GPIO12_LOW_PERF*
INA3221_VPU
NVVDD_EN
INA3221_PV
I2C Address:(1000 000b)
PULLED-UP TO 3.3V ON GPIO PAGE
PEX 3V3 INPUT - 10W
3V3
3V3_F
C866
0.1UF
L1
1.0uH
LB3
220R@100MHz
LB4
220R@100MHz
Alternate
C63
10UF
C59
1UF
C57
0.1UF
PEX_12V INPUT - 66W
12V
12V_F
RS2
0.005R
C503
0.1UF
C504
1UF
C221
10UF
L9
0.33UH
Ian 3.0
C213
10UF
Stuff if sensing
current through choke
12V_INP
12V_INN
R185
R183
12V_INN_R
Stuff to
Sense
Choke
Current
Stuff to
Sense
Resistor
Current
PEX6 INPUT 1 - 2x3 PCIE CON 75W
12V_PEX6_1_INN
12V_PEX6_1_INP
R193
R195
12V_PEX6_VIN1
RS1
0.005R
C218
0.1UF
C219
1UF
C220
10UF
L22
0.5uH
CHK_D2_7X7
L04-05A7321-L65
12V_PEX6_F1
C222
10UF
C214
47p
C216
47p
6P1_SENSE_B
8P1_SENSE_B
R237
R236
INPUT_PEX6_DT1*
STUFF FOR 6-PIN CONNECTOR
INPUT_PEX8_DT1*
R190
R235
INPUT_PEX8_DT2
Stacked Connector
J6
6-pin PEX/8-pin PEX
6-pin PEX/6-pin PEX
See BOM to determin which
connector is stuffed
PEX8 INPUT 2 - 2x4 PCIE CON 150W
8P2_SENSE_B
12V_PEX8_VIN2
RS501
0.005R
C225
0.1UF
C224
1UF
C223
10UF
C217
47p
C227
47p
L23
0.5uH
CHK_D2_7X7
L04-05A7321-L65
12V_PEX8_F2
C510
10UF
for 8-pin use 0.47uH
in 7_6X7_6 package
NVPN 131-0354-000
12V_PEX8_2_INP
12V_PEX8_2_INN
R521
R524
12V_PEX8_2_INN_LR

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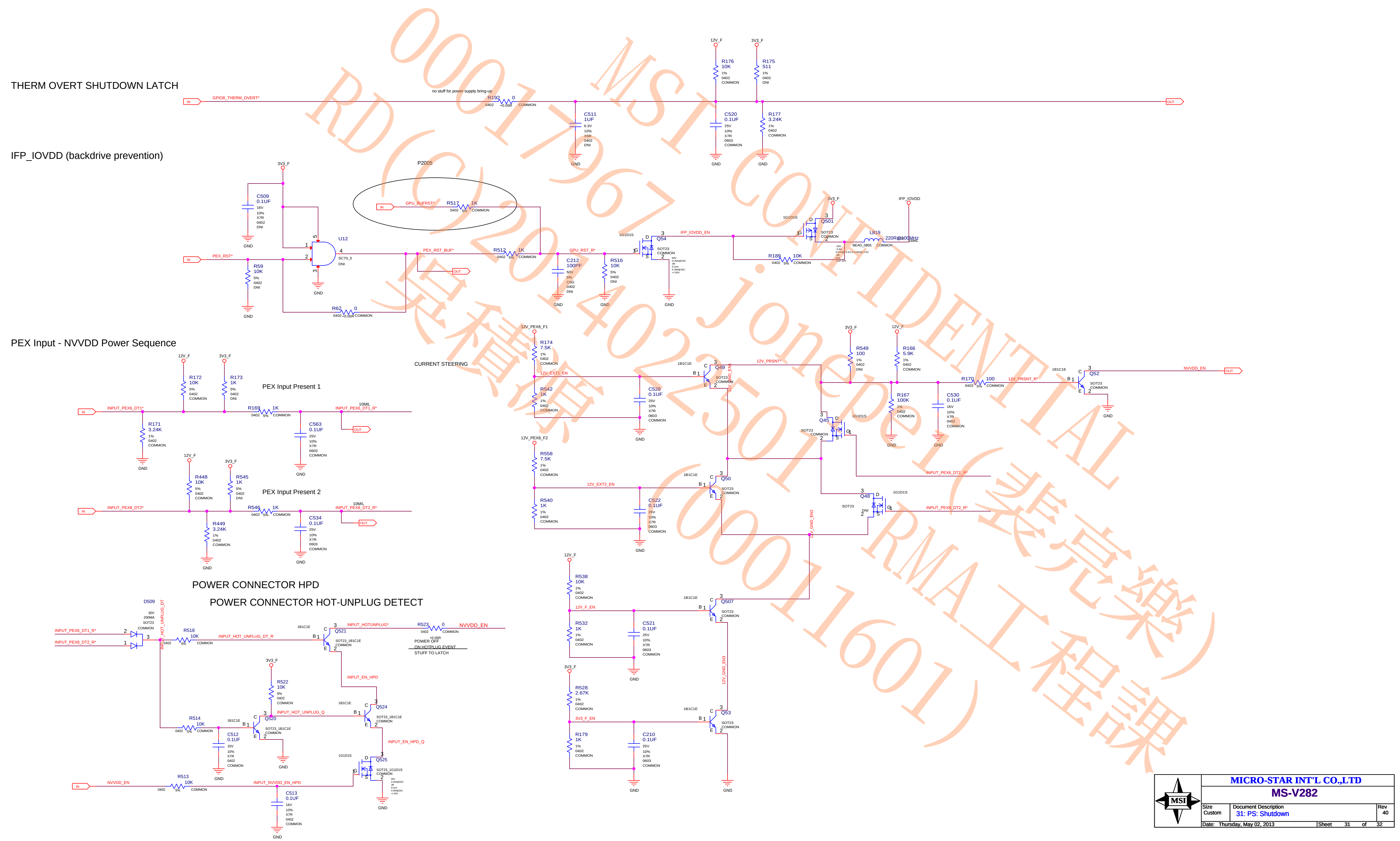
Page31: PS: Shutdown


STUFF for TMP411
THERM OVERT SHUTDOWN LATCH
GPIO8_THERM_OVERT*
no stuff for power supply bring-up
R192 0
C511 1UF
R176 10K
R175 511
C520 0.1UF
R177 3.24K
IFP_IOVDD (backdrive prevention)
P2005
GPU_BUFRST*
R517 1K
C509 0.1UF
U12
SC70_5
PEX_RST*
R59 10K
R62 0
PEX_RST_BUF*
R512 1K
GPU_RST_R*
C212 100PF
R516 10K
Q54
IFP_IOVDD_EN
Q501
IFP_IOVDD
LB19
R189 10K
PEX Input - NVVDD Power Sequence
CURRENT STEERING
R174 7.5K
12V_EXT1_EN
R542 1K
C528 0.1UF
Q49
12V_PRSNT*
R549 100
R166 5.9K
R170 100
Q52
NVVDD_EN
R167 100K
C530 0.1UF
Q45
PEX Input Present 1
INPUT_PEX6_DT1*
R172 10K
R173 1K
R169 1K
INPUT_PEX6_DT1_R*
R171 3.24K
C563 0.1UF
PEX Input Present 2
INPUT_PEX8_DT2*
R448 10K
R545 1K
R546 1K
INPUT_PEX8_DT2_R*
R449 3.24K
C534 0.1UF
R558 7.5K
12V_EXT2_EN
R540 1K
C522 0.1UF
Q50
Q48
POWER CONNECTOR HPD
POWER CONNECTOR HOT-UNPLUG DETECT
D509
R518 10K
INPUT_HOT_UNPLUG_DT_R
Q521
INPUT_HOTUNPLUG*
R523 0
POWER OFF
ON HOTPLUG EVENT
STUFF TO LATCH
R522 10K
INPUT_EN_HPD
Q524
R514 10K
C512 0.1UF
Q520
INPUT_HOT_UNPLUG_Q
INPUT_EN_HPD_Q
Q525
NVVDD_EN
R513 10K
INPUT_NVVDD_EN_HPD
C513 0.1UF
R538 10K
12V_F_EN
R532 1K
C521 0.1UF
Q507
R528 2.67K
3V3_F_EN
R179 1K
C210 0.1UF
Q53
GND

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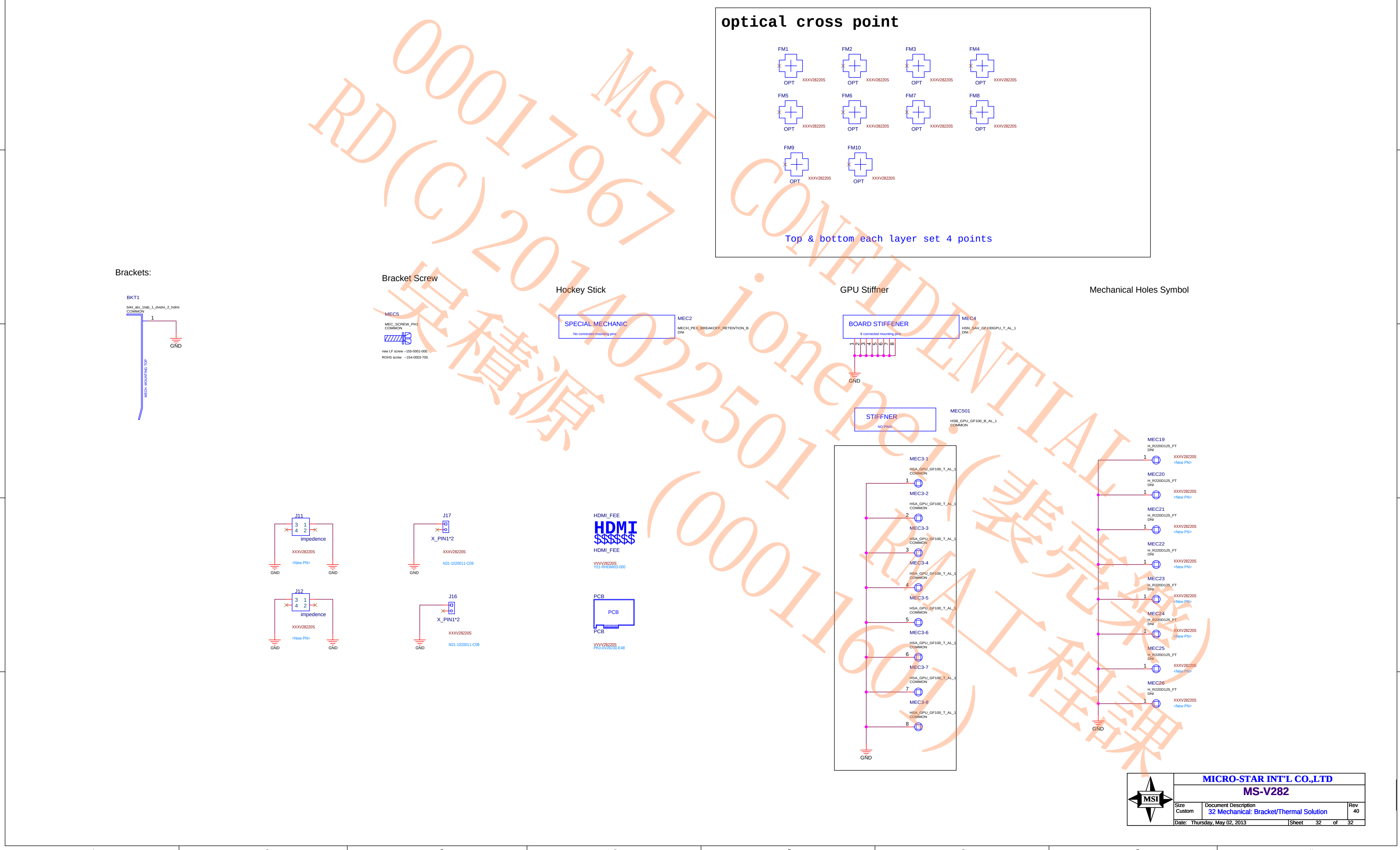
Page32: Mechanical: Bracket/Thermal Solution



optical cross point
FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8 FM9 FM10
OPT
XXXV28220S
Top & bottom each layer set 4 points
Brackets:
BKT1
brkt_atx_1tab_1_dvidvi_2_hdmi
COMMON
MECH. MOUNTING TOP
GND
Bracket Screw
MEC5
MEC_SCREW_PH1
COMMON
new LF screw --155-0001-000
ROHS screw --154-0003-700.
Hockey Stick
SPECIAL MECHANIC
No connected mounting pins
MEC2
MECH_PEX_BREAKOFF_RETENTION_B
DNI
GPU Stiffner
BOARD STIFFENER
8 connected mounting pins
MEC4
HSN_SAV_GF100GPU_T_AL_1
DNI
STIFFNER
NO PINS
MEC501
HSB_GPU_GF100_B_AL_1
COMMON
MEC3-1 MEC3-2 MEC3-3 MEC3-4 MEC3-5 MEC3-6 MEC3-7 MEC3-8
HSA_GPU_GF100_T_AL_1
COMMON
Mechanical Holes Symbol
MEC19 MEC20 MEC21 MEC22 MEC23 MEC24 MEC25 MEC26
H_R220D125_FT
DNI
XXXV28220S
<New PN>
J11
J12
impedence
J17
J16
X_PIN1*2
N31-1020011-C09
HDMI_FEE
HDMI
$$$$$$
VVVV28220S
Y01-RHDMI03-000
PCB
PK0-0V28230-E48
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MS-V282
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Custom
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