

P727-A01: G96, GB1-128, GDDR3, DL-DVI, DL-DVI/VGA, SD/HDTV

V129-121

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- Page 24: POWER SUPPLY: NVVDD DUAL PHASE SWITCHER
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REV 1.2 HISTORY

04/01

PAGE 12.Remove J1 Slim-DSUB connector

PAGE 15.Add R761 and R762 to reserve pull down DP AUX
Change F503 and F504 footprint to 1812 size
Remove DP J8 Pin25,Pin26

PAGE 18.Change U514~U517 to EM1~EM6

PAGE 19.Add 2pin Fan control circuit

PAGE 23.Add C120,C149 10uF 1206 footprint to reserve PEX_VDD power

04/08

PAGE 22. Add R92 0805 0ohm Resistor for 3V3 bypass to 2V5 power

REV 1.21 HISTORY

06/04

PAGE 20.Add R774 10K pull down resistor for HDA issue

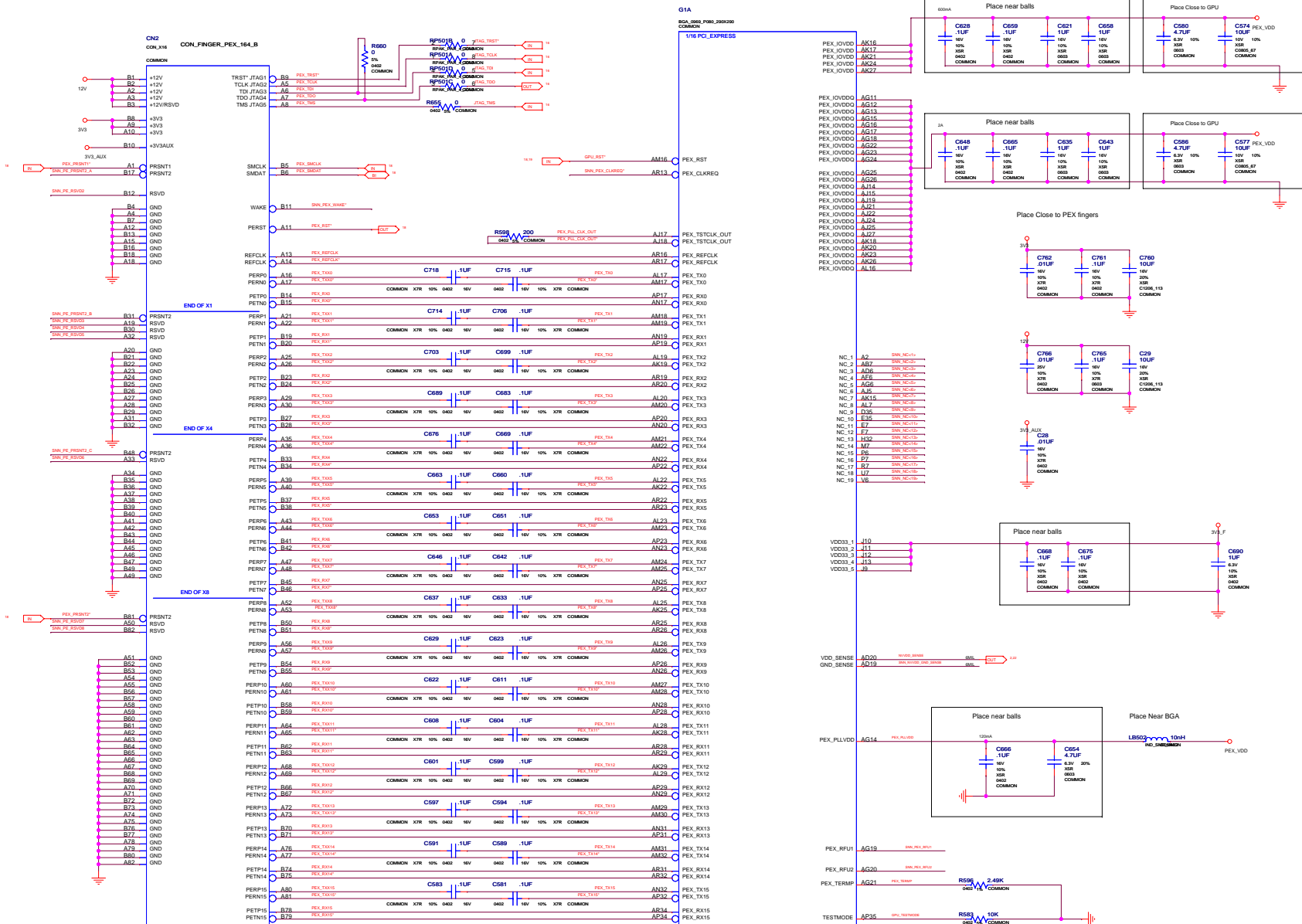
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1	SKJ0000	600-10727-0000-100	G96-400, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
2	SKJ0001	600-10727-0001-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
3	SKJ0002	600-10727-0002-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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G1A



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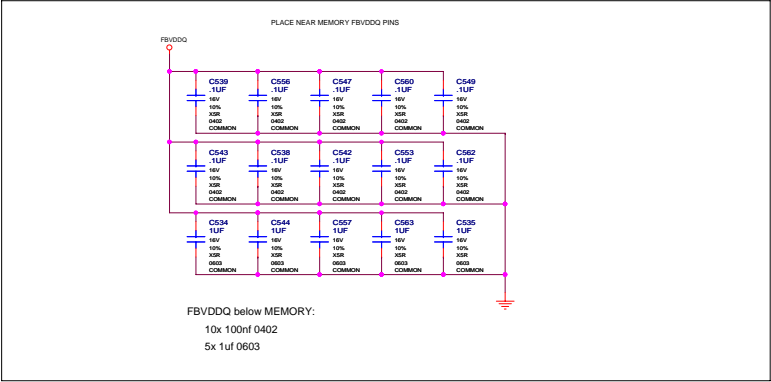
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS

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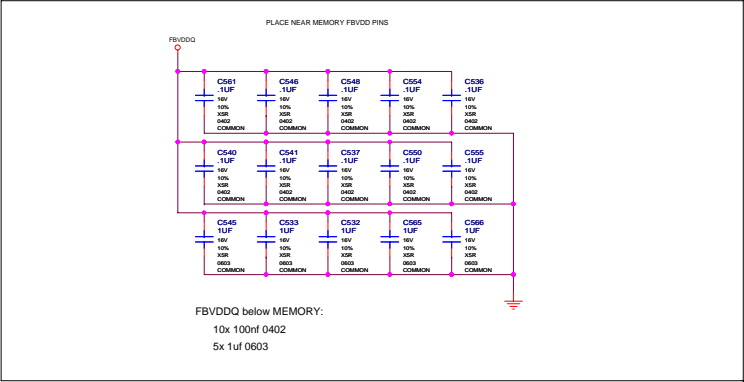


FRAME BUFFER: PARTITION A DECOUPLING

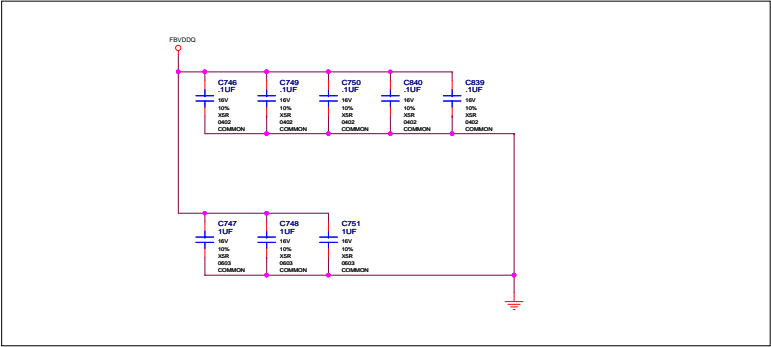
Decoupling for FBA 0..31



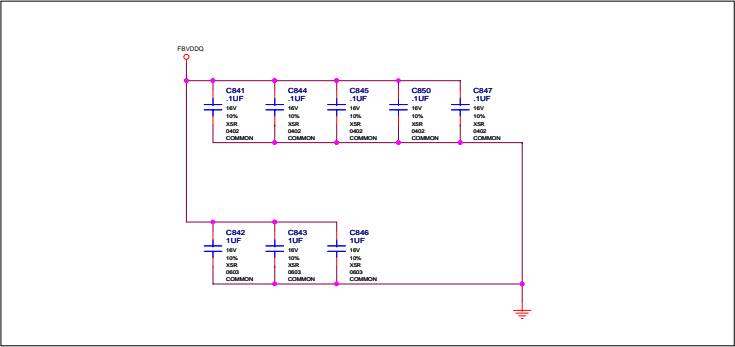
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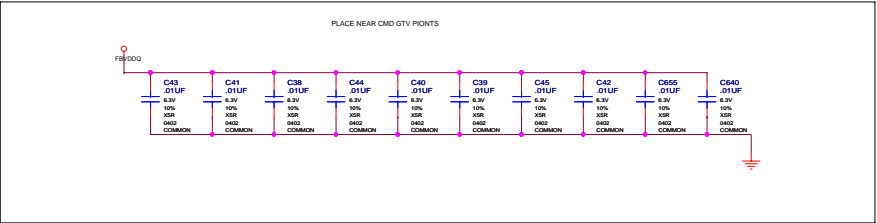
Decoupling for FBA A1 0..31



Decoupling for FBA A1 0..31



Return path coupling GND/FBVDDQ for FBA

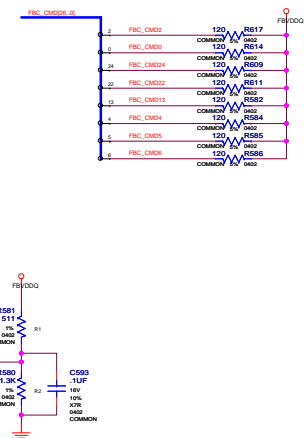
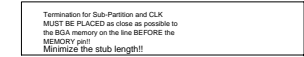
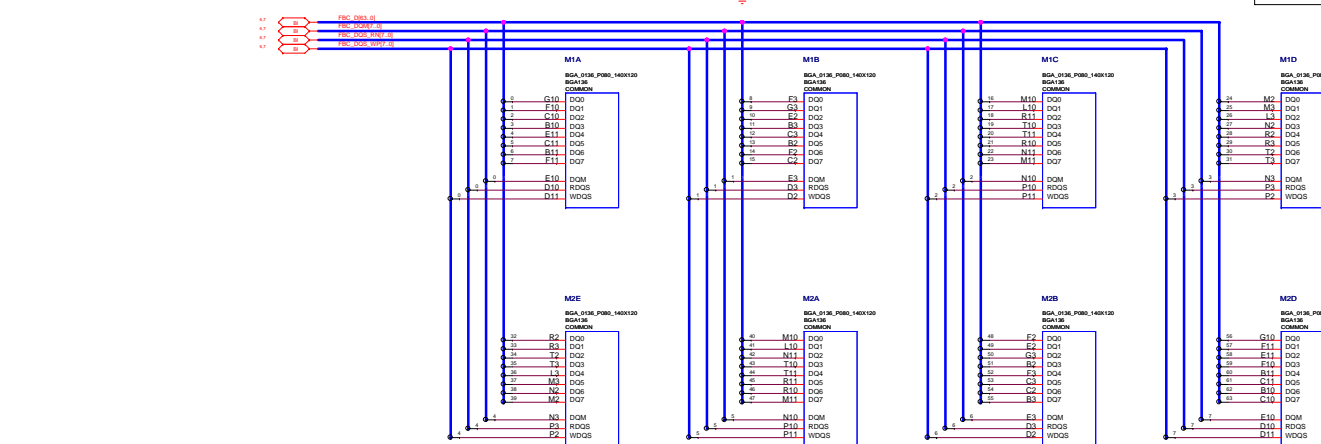



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ASSEMBLY	BASIC LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 1000 ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

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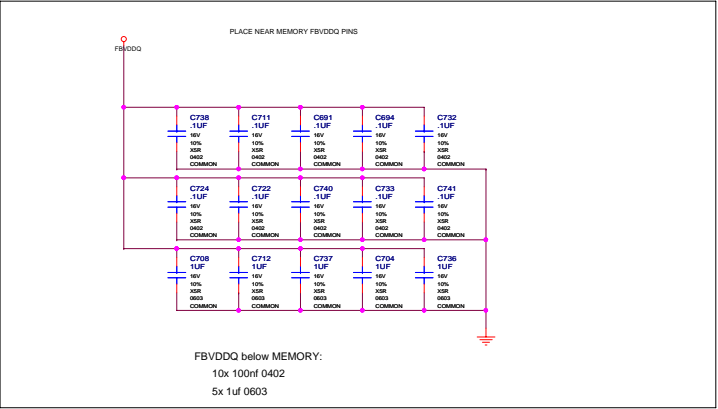
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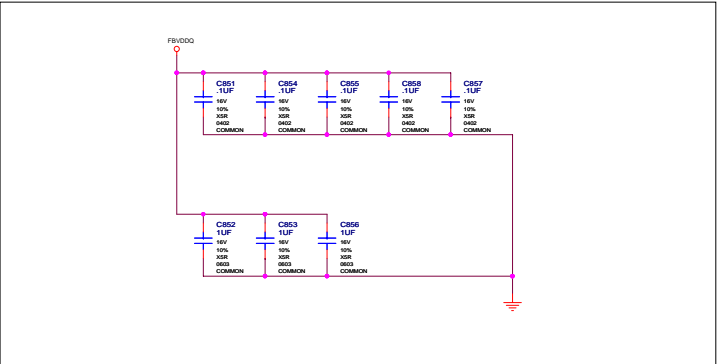
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FRAMEBUFFER: PARTITION C DECOUPLING

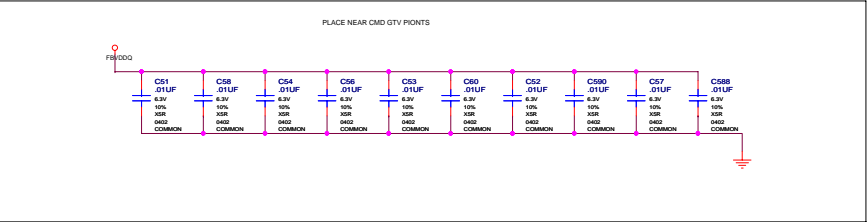
Decoupling for FBC 0..31



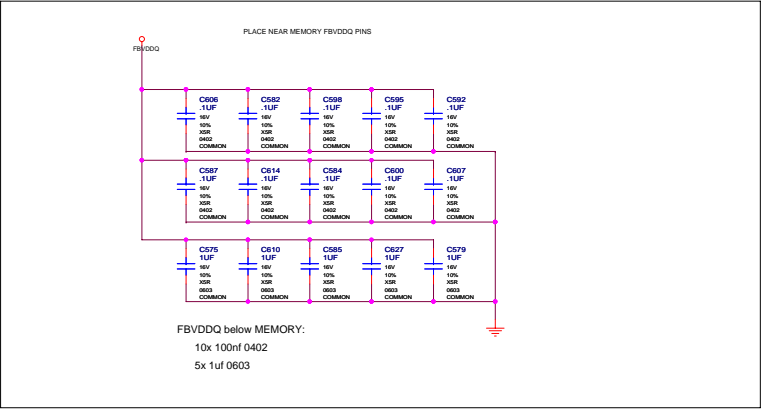
Decoupling for FBC C1 0..31



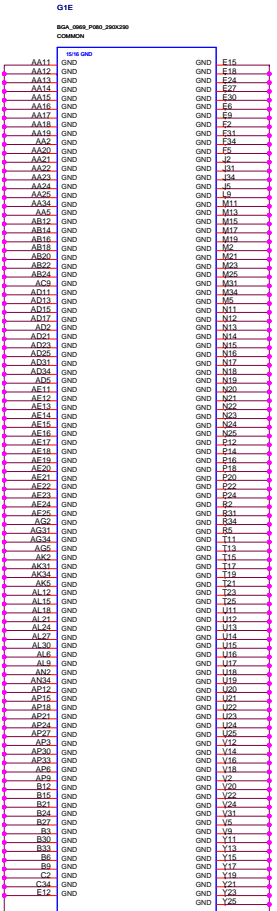
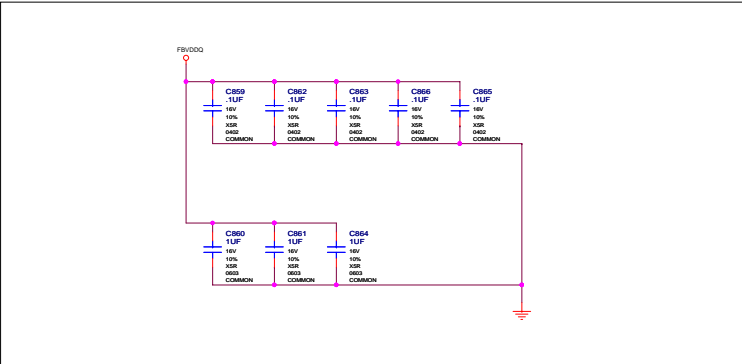
Return path coupling GND/FBVDDQ for FBC



Decoupling for FBC 32..63



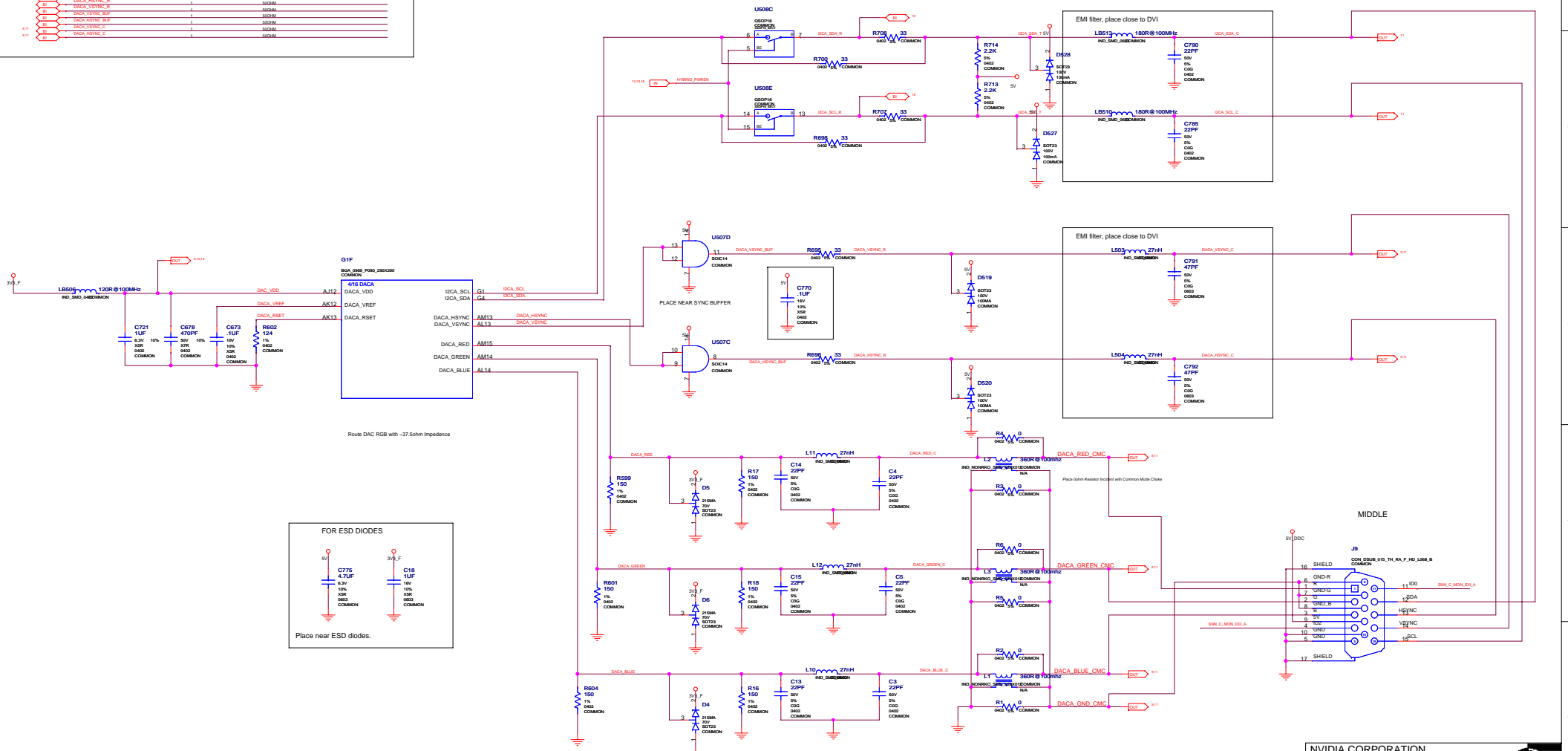
Decoupling for FBC C1 32..63



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IN	DATA_VREF			120M
IN	DATA_VBIAS			120M
	DATA_RSD	1	75OHM	
IN	DATA_GREEN	1	75OHM	
IN	DATA_BLUE	1	75OHM	
	DATA_RSD_C	1	75OHM	
IN	DATA_GREEN_C	1	75OHM	
IN	DATA_BLUE_C	1	75OHM	
6.3.1.5	DATA_GND_CMIC			0V 120M
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6.3.1	DATA_BLUE_CMIC	1	75OHM	
6.3.1	DATA_VBIAS_CMIC	1	75OHM	
	DATA_VBIAS	1	50OHM	
	DATA_VREF	1	50OHM	
	DATA_VREF_B	1	50OHM	
	DATA_VREF_R	1	50OHM	
	DATA_VREF_BUF	1	50OHM	
	DATA_VREF_BUF	1	50OHM	
6.3.1	DATA_VREF_C	1	50OHM	
	DATA_VREF_C	1	50OHM	

Primary Display (DACA), DVI-I

DACA RGB-FILTER



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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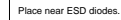


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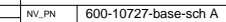
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10.12	DACC_VSYN2_C	1	SDCHM
10.12	DACC_HSYN2_C	1	SDCHM



PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MI
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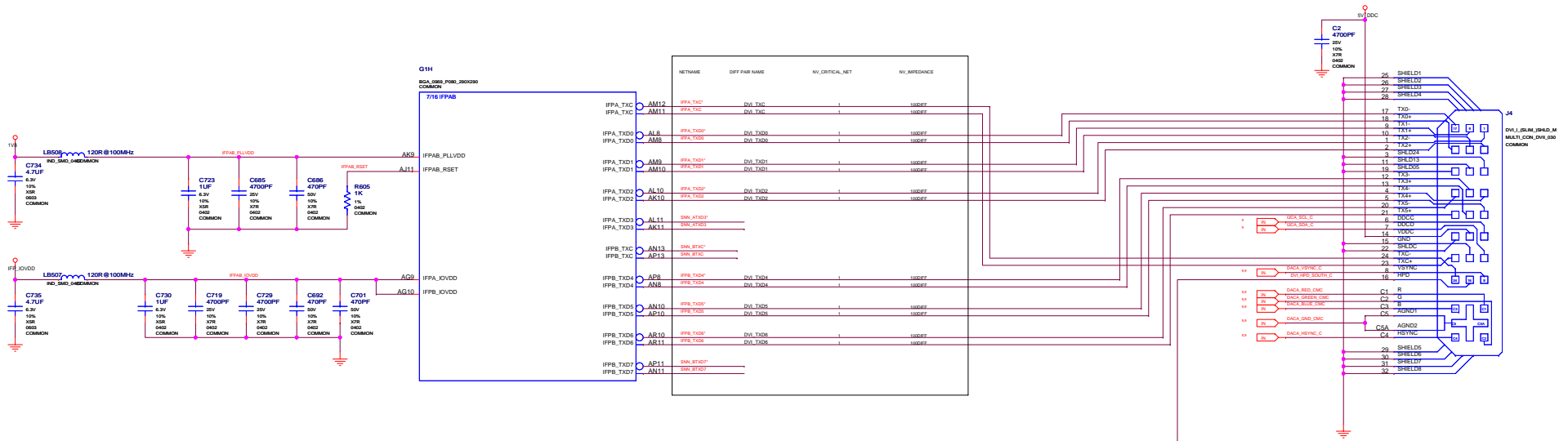
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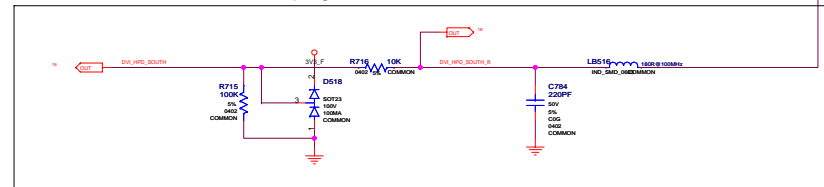


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TMDS LINK: A & B



Hotplug Detection



NETNAME	MIN. LINE WIDTH	VOLTAGE
#FAB_PLVDD	120M	1.8V
#FAB_I0VDD	120M	3.3V
#FABRESET	120M	

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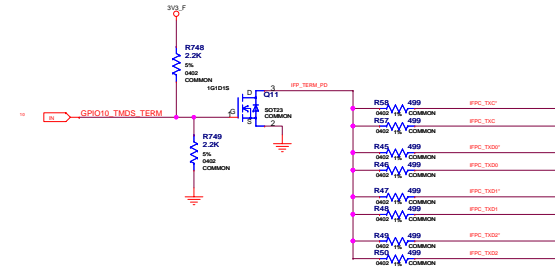


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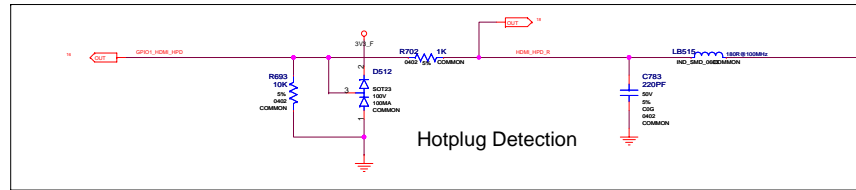
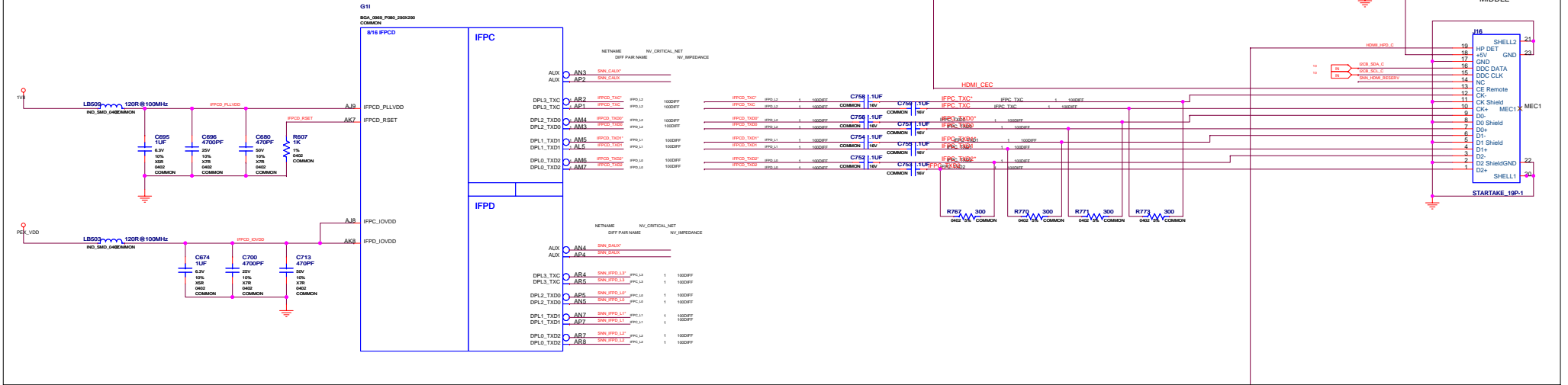
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TMD5 LINK: C & D



TMD5 C : HDMI



NETNAME	MIN_LENGTH	VOLTAGE
IFPCD_FLVDD	1.2MIL	1.8V
IFPCD_OVDD	1.2MIL	2.5V
IFPCD_TERM_PD	0.001	1.8V

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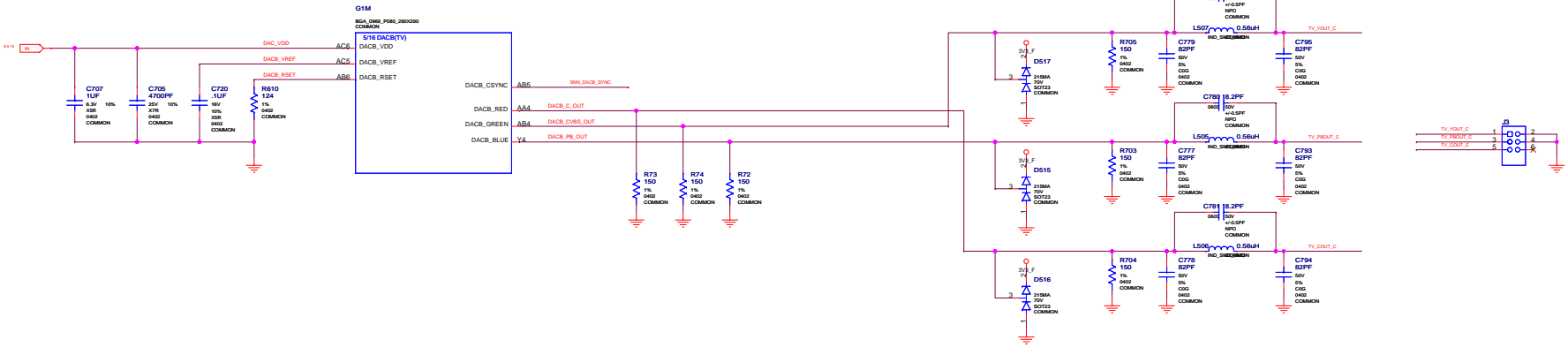
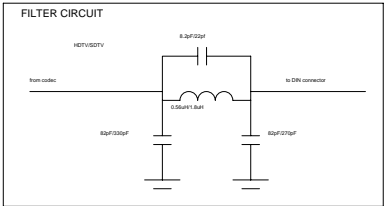
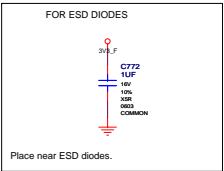
ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 5100FF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: TMD5 LINK C/D, AC COUPLING, PD, DVI CONNECTOR MID

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DACB: SD/HD VIDEO OUT CONNECTOR

NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
DACB_C_OUT		75OHM	1
DACB_CVBS_OUT		75OHM	1
DACB_PB_OUT		75OHM	1
TV_PROUT_C		75OHM	1
TV_PROUT_S		75OHM	1
TV_PROUT_E		75OHM	1
DACB_VREF	100M		
DACB_RESET	100M		



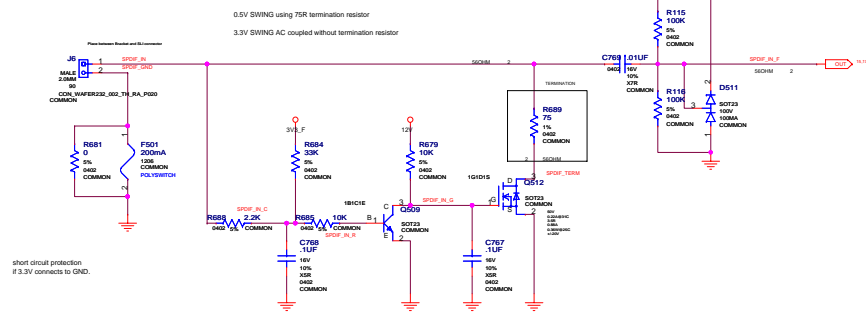
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 100FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTER, MINOR CONNECTOR NORTH, SD/HD VIDEO OUTPUT CONNECTOR

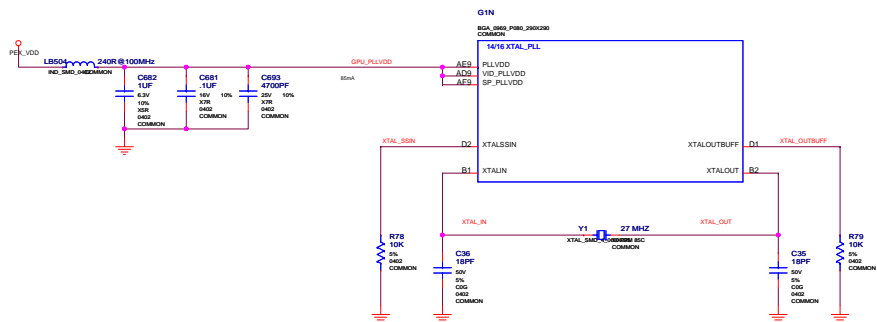
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NAME			

XTAL/PLLVD/SPDIF IN

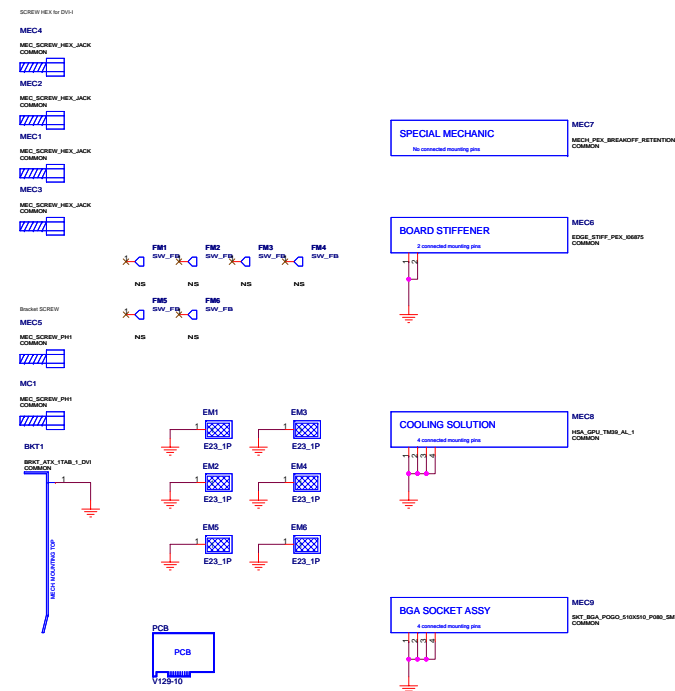
SPDIF IN



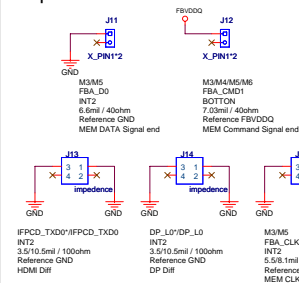
XTAL/GPU_PLLVDD



MECHANICALS & THERMALS



Impedance control line



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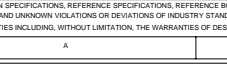
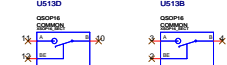
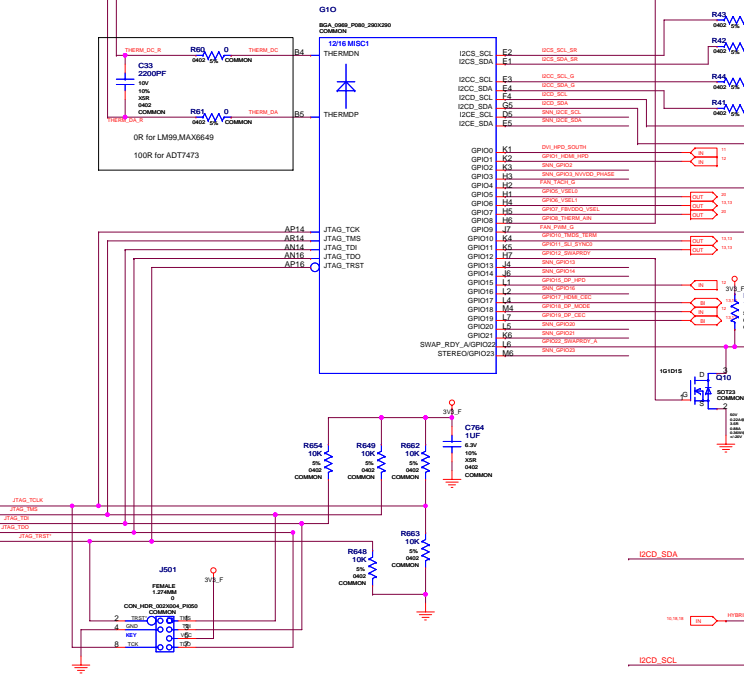
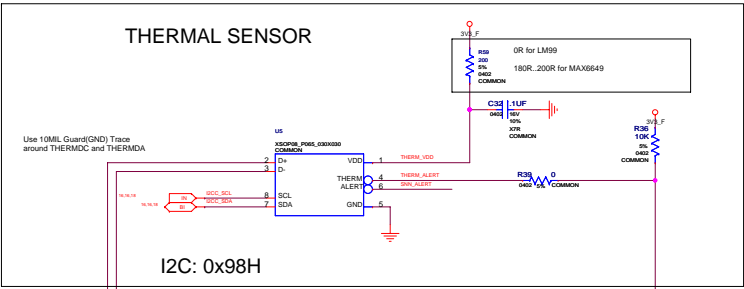
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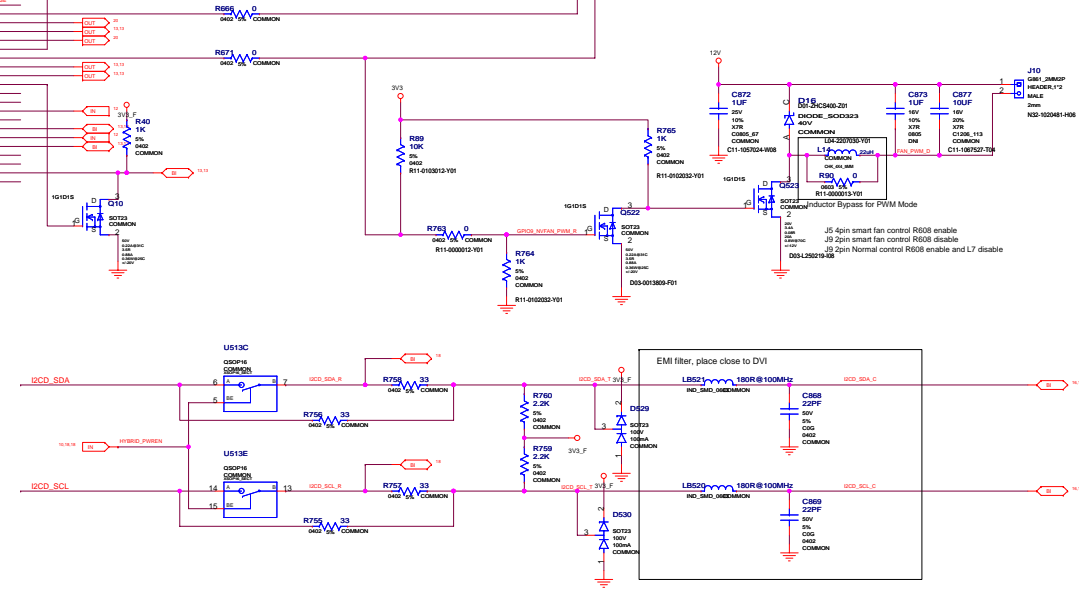
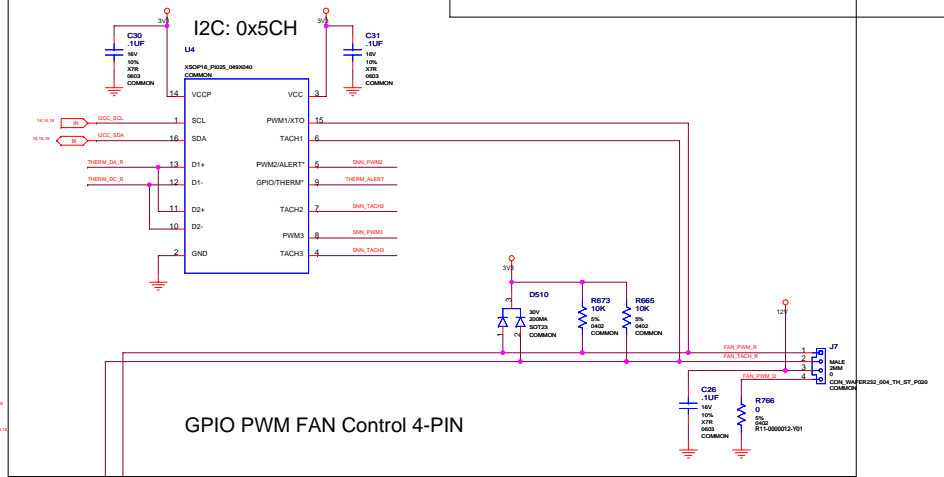
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF-IN, XTAL, MECHANICALS, THERMALS



GPIO & JTAG

THERMAL SENSOR, FAN CONTROLLER
uses 3V3: always on.



NETNAME	MIN_LINE_WIDTH	VOLTAGE
THERM_DC	10MIL	3V3
THERM_SDA	10MIL	3V3
THERM_SCL	10MIL	3V3
THERM_ALERT	10MIL	3V3
THERM_ALERT_N	10MIL	3V3
THERM_DC	10MIL	3V3

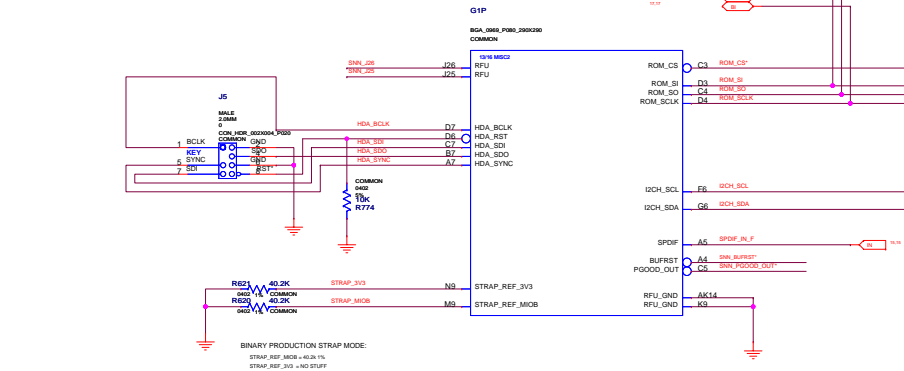
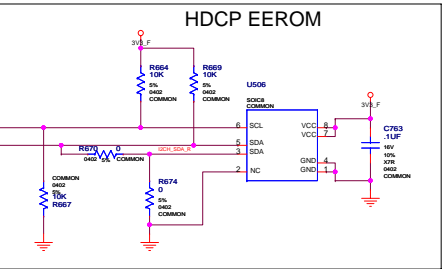
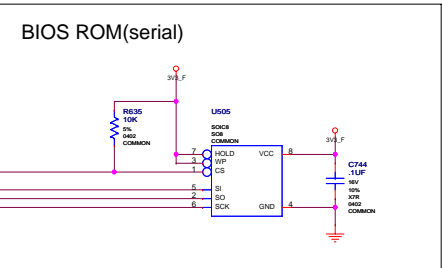
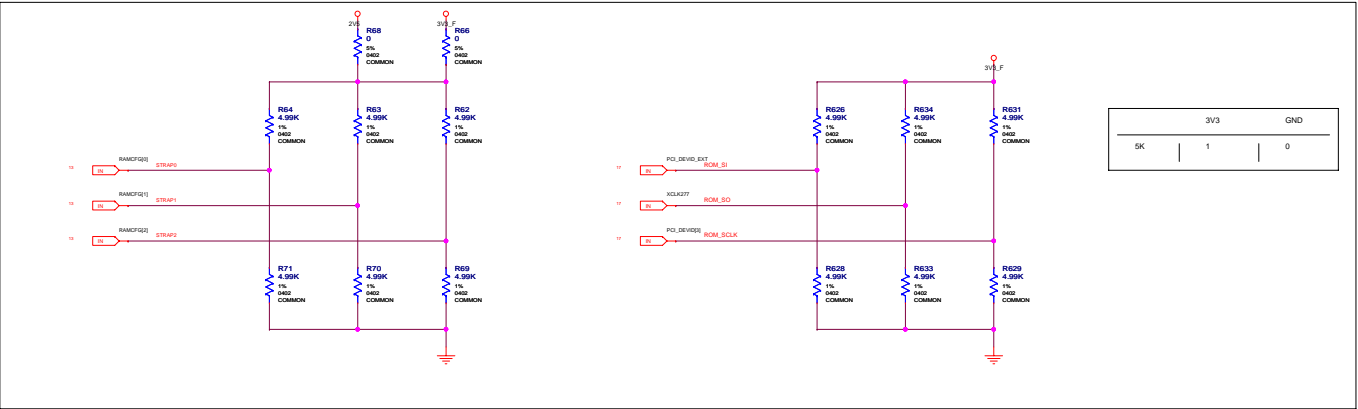
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 310FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	EXTERNAL THERMAL SENSOR, 4PIN FAN CONTROL, GPIO

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STRAPPING OPTIONS

Assembly: BIOS



NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
HDA_BCLK		50ohm	
HDA_RST		50ohm	
HDA_SDI		50ohm	
HDA_SDO		50ohm	
HDA_SYNC		50ohm	

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STRAP ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

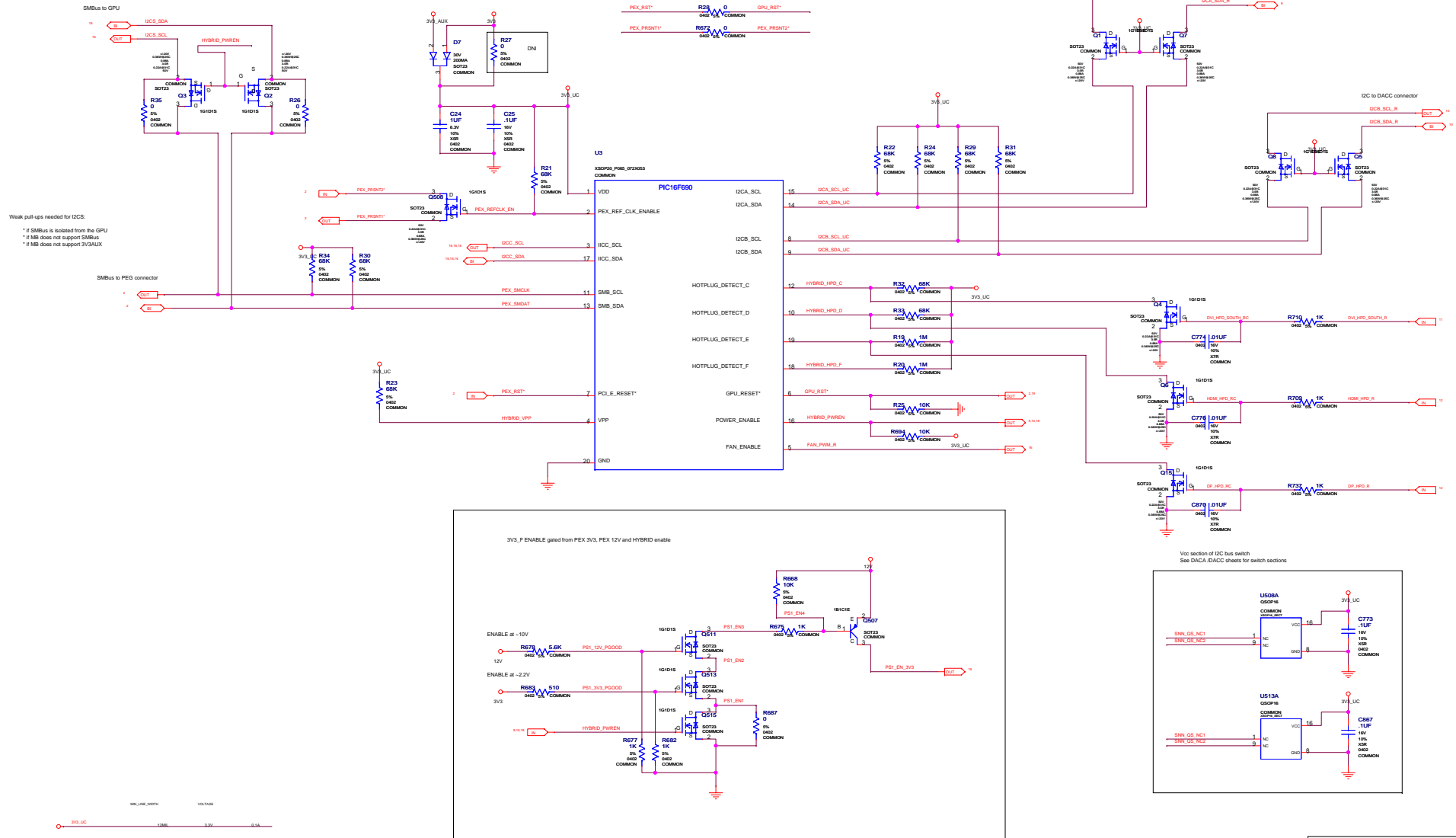
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HYBRID POWER

Per Datasheet:

Vf = 400mV at 10mA
* expected current < 2

Stuff only to bypass the micro-controller



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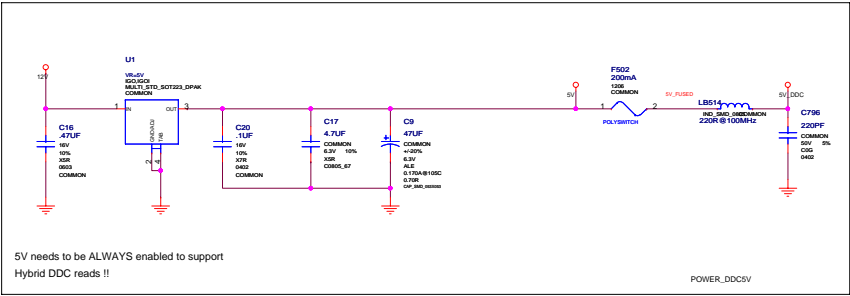
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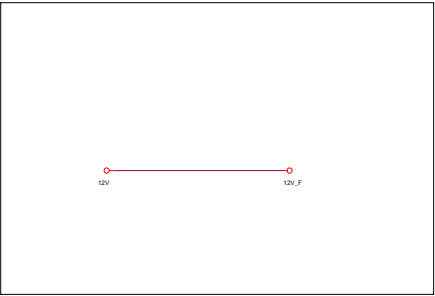
Power Supply: 5V, 5V_DDC, TMD5, MIOA_VDDQ

5V REGULATOR

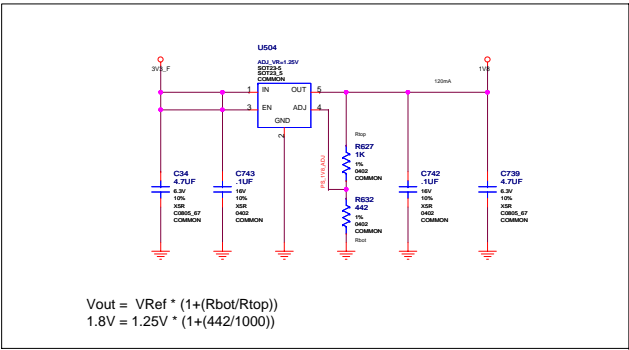


5V DDC

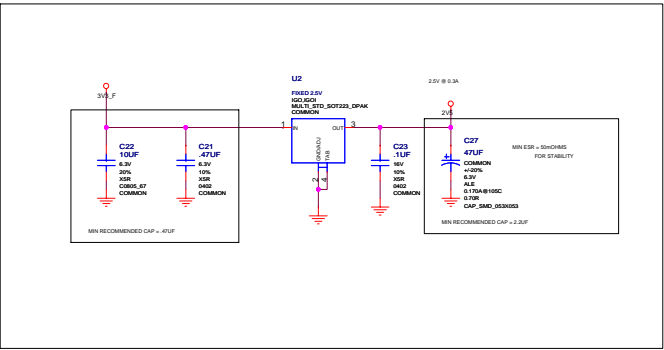
12V filter



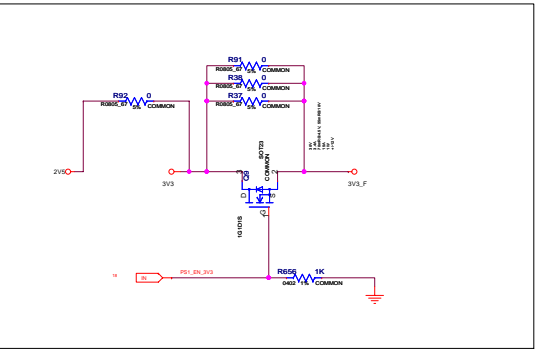
IFP PLL Supply 1.8V



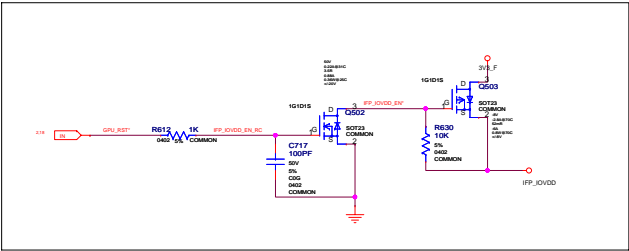
MIO_VDD 2.5V



3V3 switch



IFP_IOVDD BACKDRIVE PREVENTION



NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	0.1A	120M	5V
5V_DDC	0.1A	120M	5V
5V	0.1A	120M	5V
PL1_V16_AD3	0.1A	120M	1.8V
1V8	0.1A	120M	1.8V
2V5	0.1A	120M	2.5V
2V5	0.1A	120M	2V
2V5_F	0.1A	120M	2.5V
12V_F	0.1A	120M	12V

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 3100FF ASSEMBLY NOTES AND BOARD NOT FINAL
PAGE DETAIL	POWER SUPPLY LINEARS: 5V, DDC5V, IFPPLLVD, IFP10VDD, MIO_VDD, 3V3 FILTER, 12V FILTER

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FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3

1

2

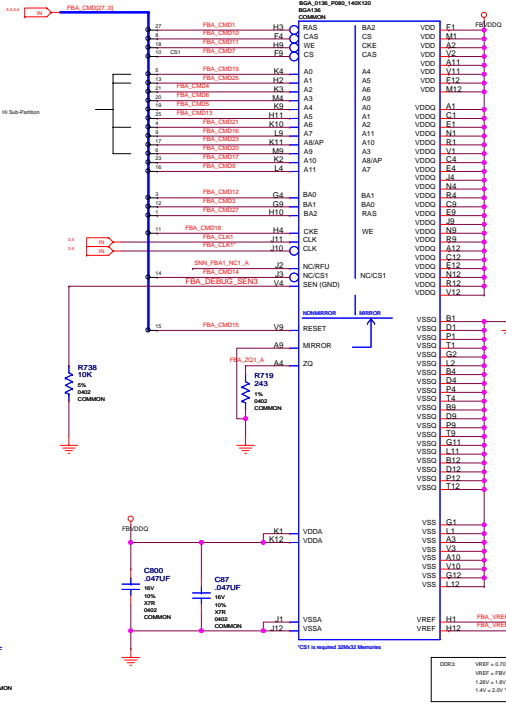
3

4

5

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FBA Partition	
136BGA CMD Mapping	
CMD	ADDR
CM01	BA0*
CM02	BA1*
CM03	BA2*
CM04	BA3*
CM05	BA4*
CM06	BA5*
CM07	BA6*
CM08	BA7*
CM09	BA8*
CM10	BA9*
CM11	BA10*
CM12	BA11*
CM13	BA12*
CM14	BA13*
CM15	BA14*
CM16	BA15*
CM17	BA16*
CM18	BA17*
CM19	BA18*
CM20	BA19*
CM21	BA20*
CM22	BA21*
CM23	BA22*
CM24	BA23*
CM25	BA24*
CM26	BA25*
CM27	BA26*



NET		DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
FBA_CMD07	FBA_CMD08	FBA_CMD09	800PT	1
FBA_CMD09	FBA_CMD10	FBA_CMD11	800PT	1
FBA_CMD11	FBA_CMD12	FBA_CMD13	800PT	1
FBA_CMD13	FBA_CMD14	FBA_CMD15	800PT	1
FBA_CMD15	FBA_CMD16	FBA_CMD17	800PT	1
FBA_CMD17	FBA_CMD18	FBA_CMD19	800PT	1
FBA_CMD19	FBA_CMD20	FBA_CMD21	800PT	1
FBA_CMD21	FBA_CMD22	FBA_CMD23	800PT	1
FBA_CMD23	FBA_CMD24	FBA_CMD25	800PT	1
FBA_CMD25	FBA_CMD26	FBA_CMD27	800PT	1

Termination for Sub-Partition and CLK MUST BE PLACED as close as possible to the BGA memory on the line BEFORE the MEMORY pin! Minimize the stub length!

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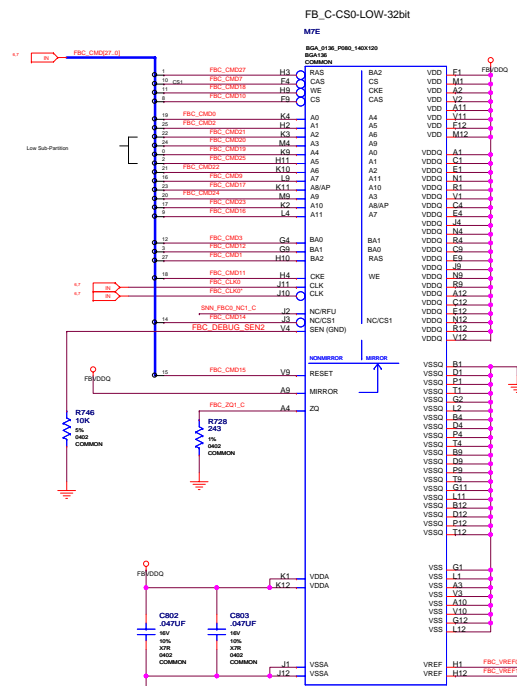
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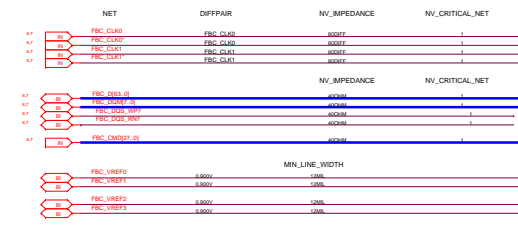
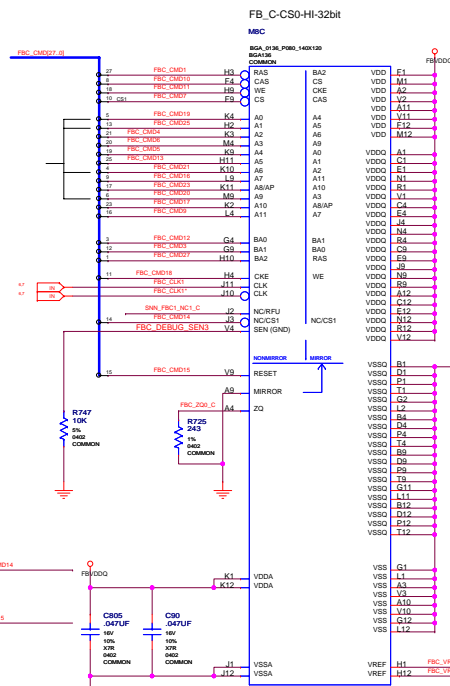
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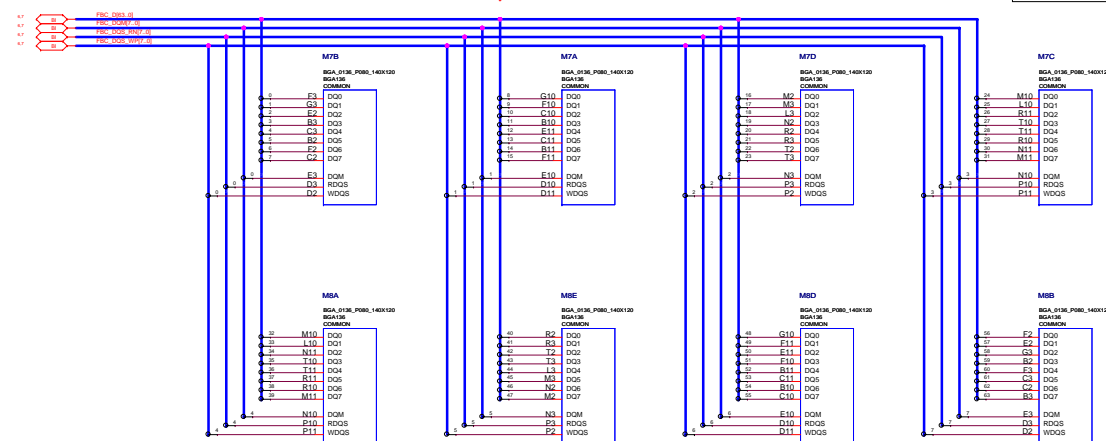
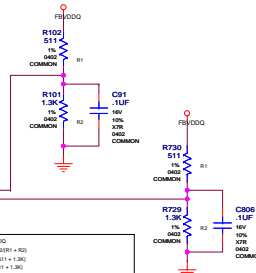
FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3



FBC Partition			CSD
CMD	ADDR		
CMD01	R40*		
CMD02	C40*		
CMD11	WE*		
CMD18	CKE		
CMD19	RESET/ODT		
CMD6	CS0*		
CMD19	A0-0		
CMD05	A0-1		
CMD04	A0-2	} Low Sub-Partition	
CMD04	A0-3		
CMD03	A0-4		
CMD3	A0-5		
CMD4	A0-6	} H Sub-Partition	
CMD6	A0-6		
CMD6	A0-6		
CMD5	A0-6		
CMD13	A0-6		
CMD21	A0-6		
CMD16	A0-7		
CMD23	A0-8		
CMD20	A0-9		
CMD17	A0-10		
CMD9	A0-11		
CMD14	A0-12		
CMD12	BA0		
CMD3	BA1		
CMD27	BA2		



Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!

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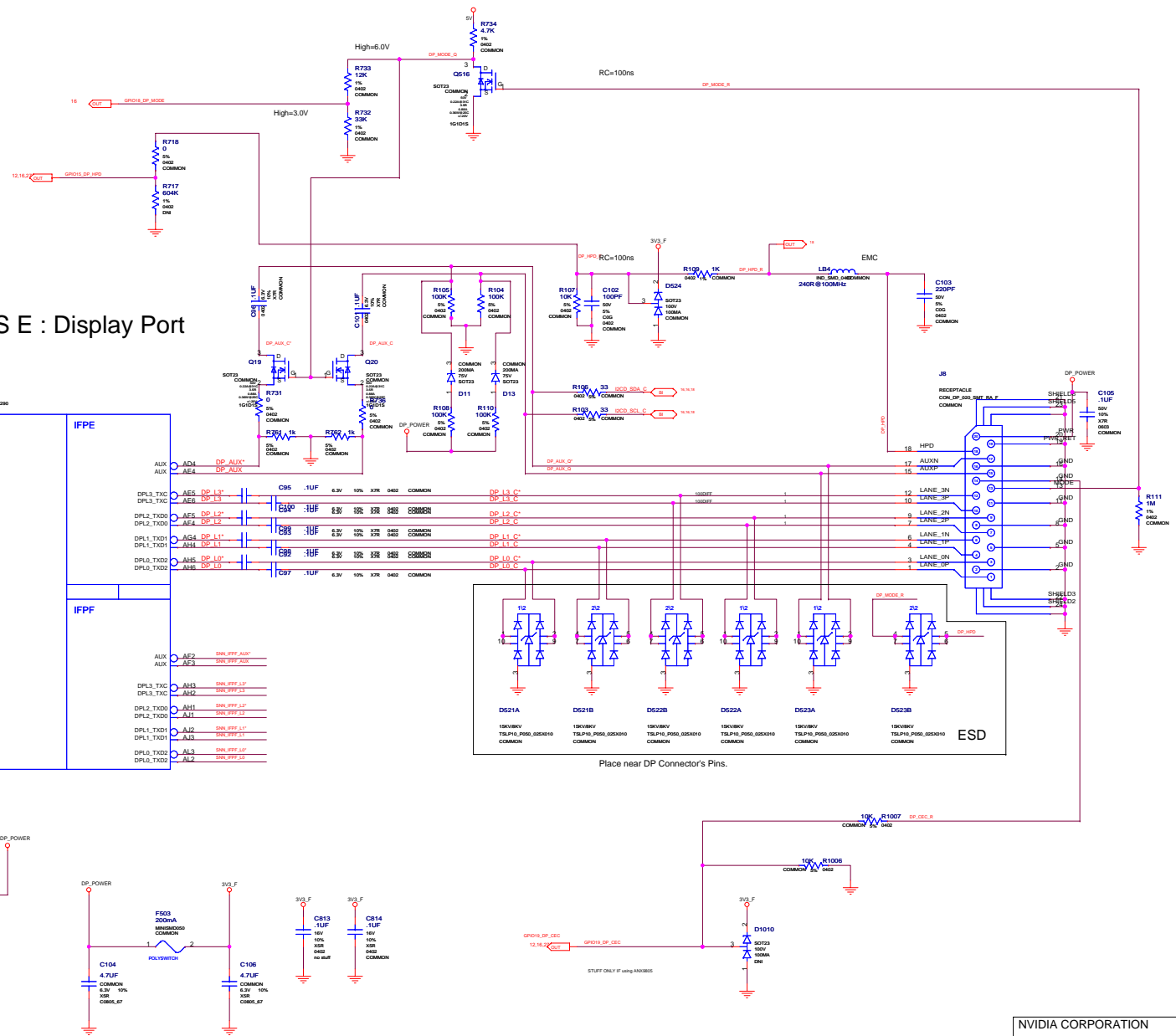
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TMDS LINK: E & F

TMDS E : Display Port



Place near DP Connector's Pins.

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



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