


PG174-A01

TU117, 128b GDDR5 x32, 75W
DVI-D DL/DUAL DP + HDMI

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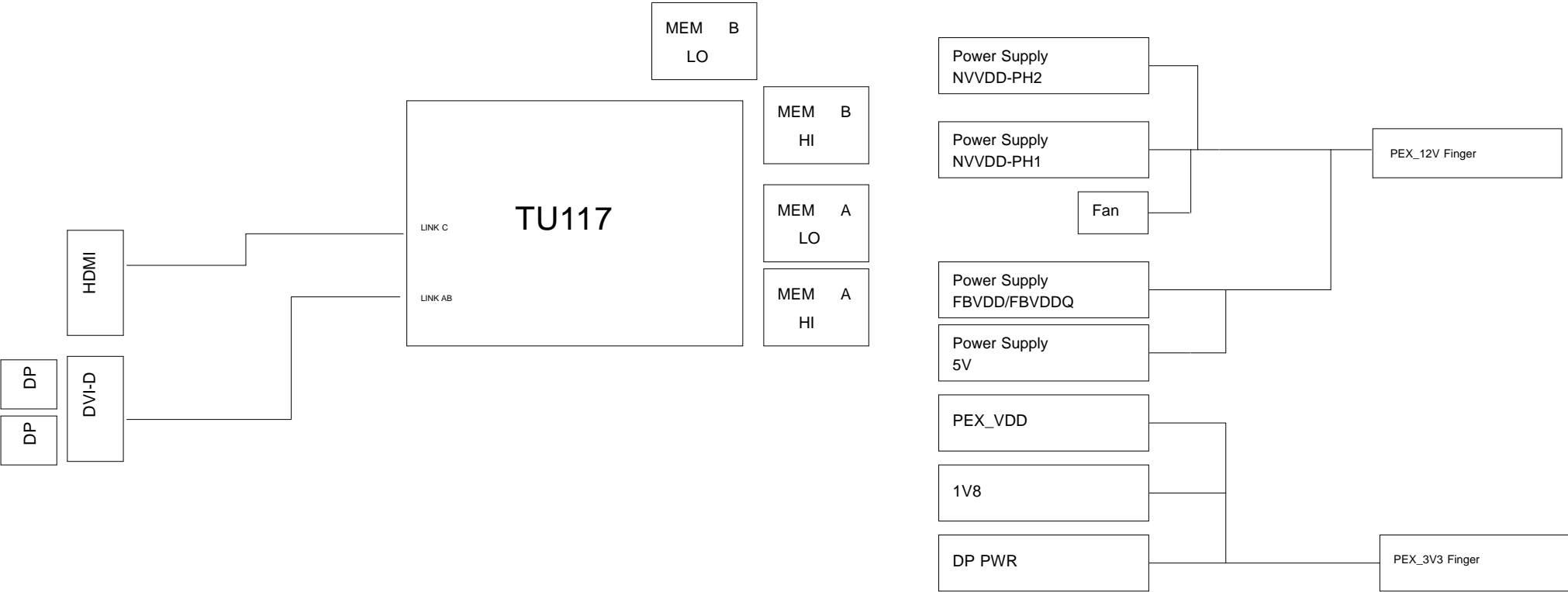
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Block Diagram

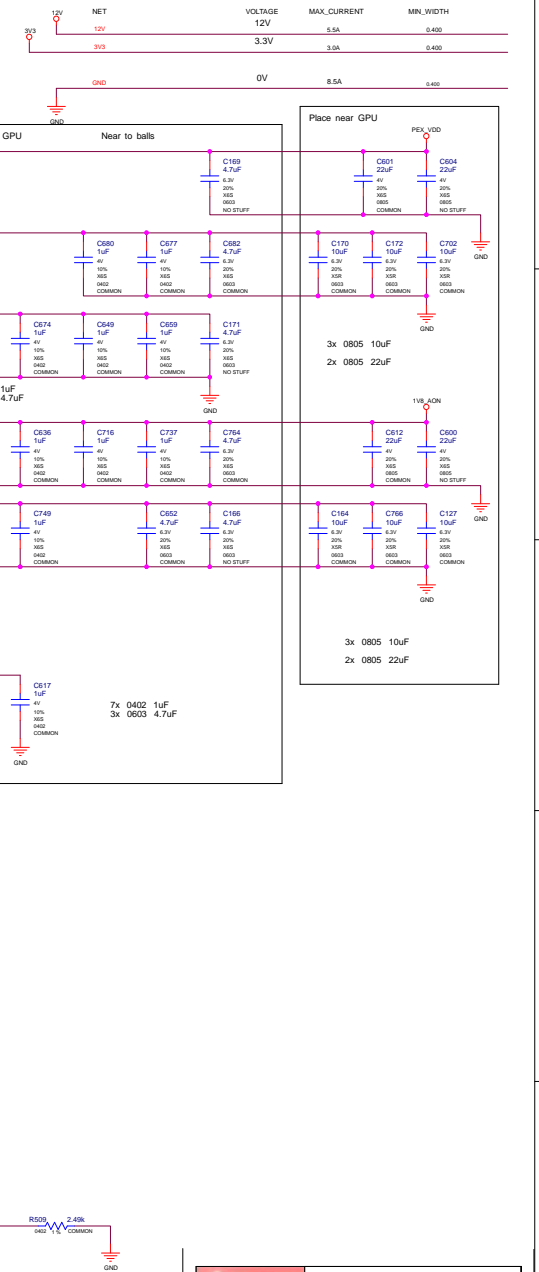
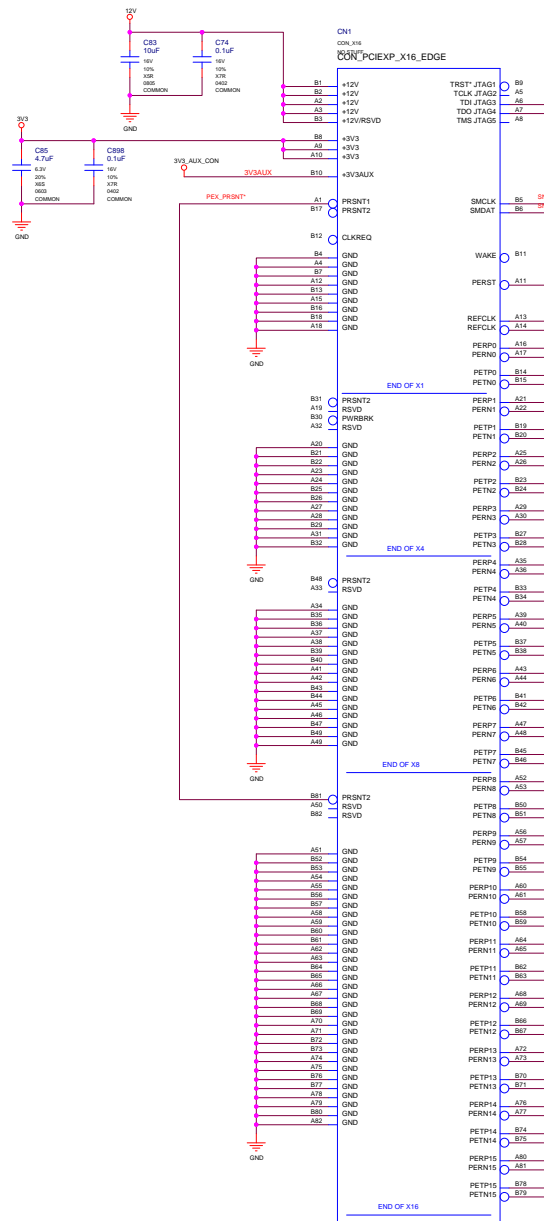


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PAGE DETAIL	Block Diagram


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PCI Express

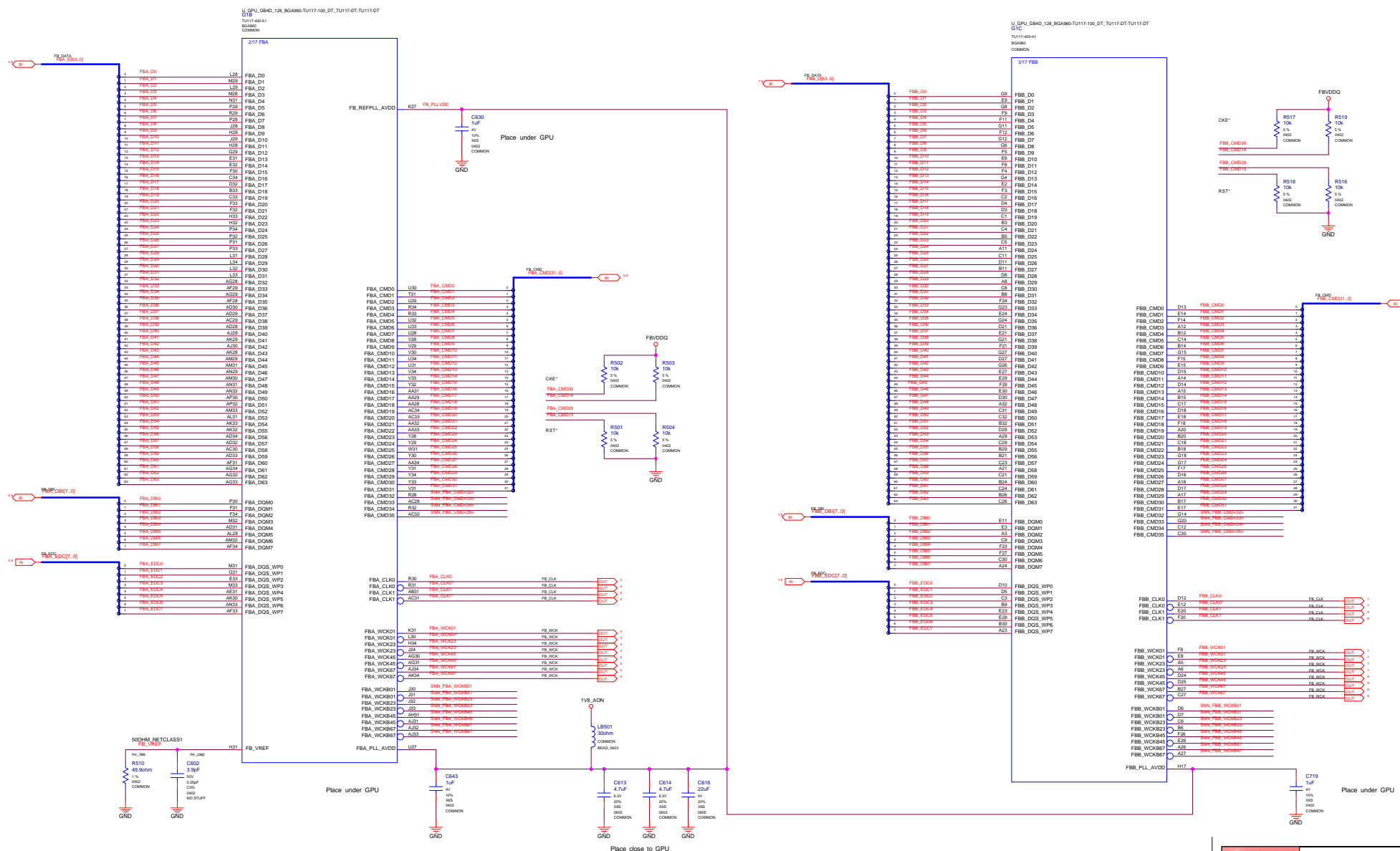


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MEMORY: GPU Partition A/B

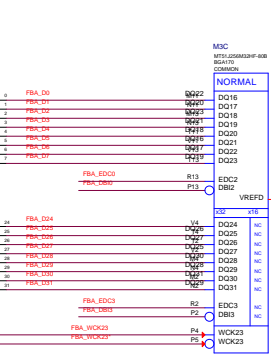
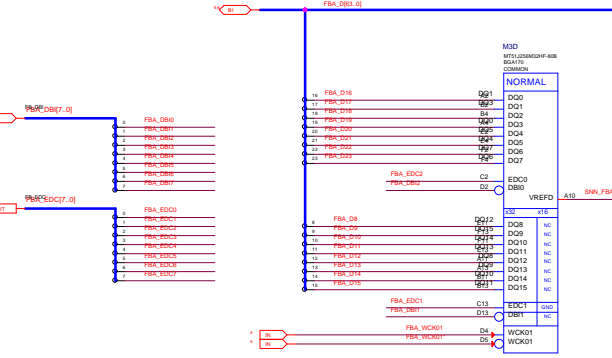
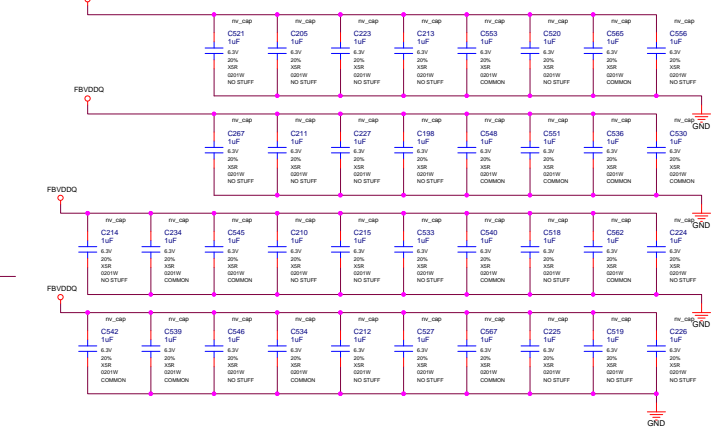
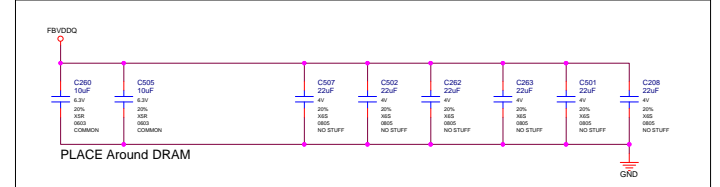
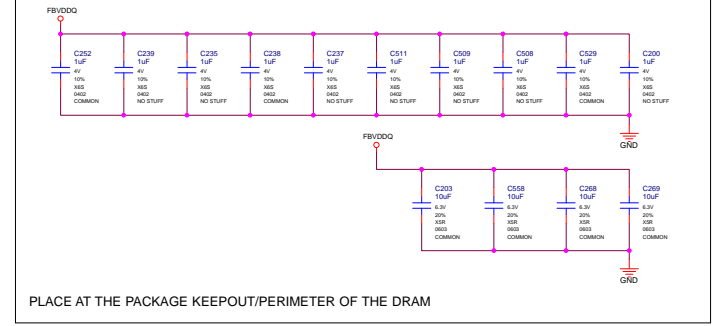
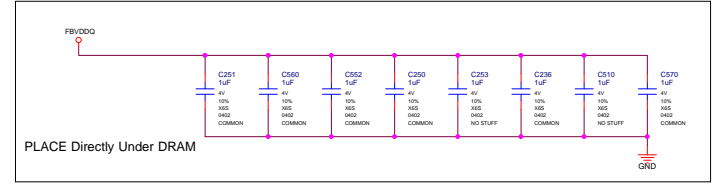
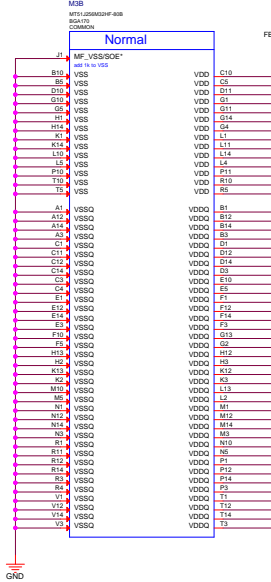
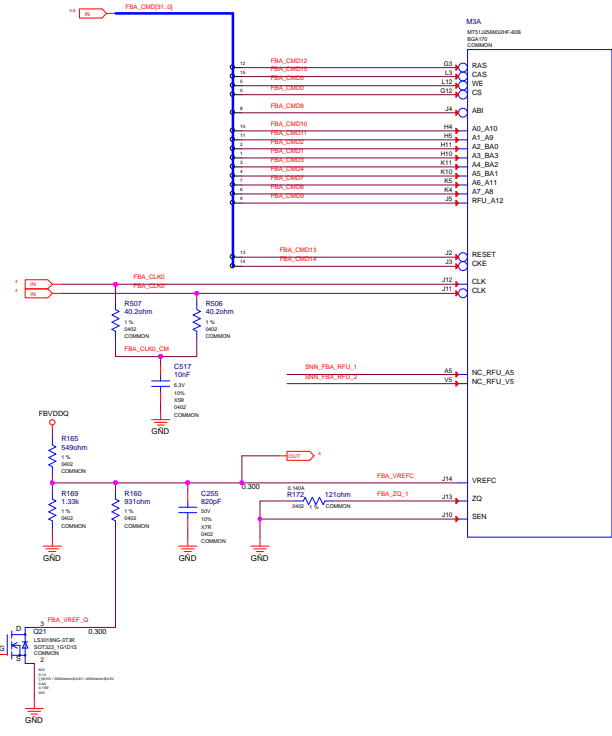


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MEMORY: FBA Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3,BA3	
CMD2	A2,BA2	
CMD3	A4,BA2	
CMD4	AS,BA1	
CMD5	WE*	
CMD6	A7,A8	
CMD7	AB,A11	
CMD8	AB*	
CMD9	A12,RFU	
CMD10	A0,A10	
CMD11	A1,A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17	A3,BA3	
CMD18	A2,BA2	
CMD19	A4,BA2	
CMD20	AS,BA1	
CMD21	WE*	
CMD22	A7,A8	
CMD23	AB,A11	
CMD24	AB*	
CMD25	A12,RFU	
CMD26	A0,A10	
CMD27	A1,A9	
CMD28	RAS*	
CMD29	RST*	
CMD30	CKE*	
CMD31	CAS*	



ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	MEMORY: FBA(31..0)

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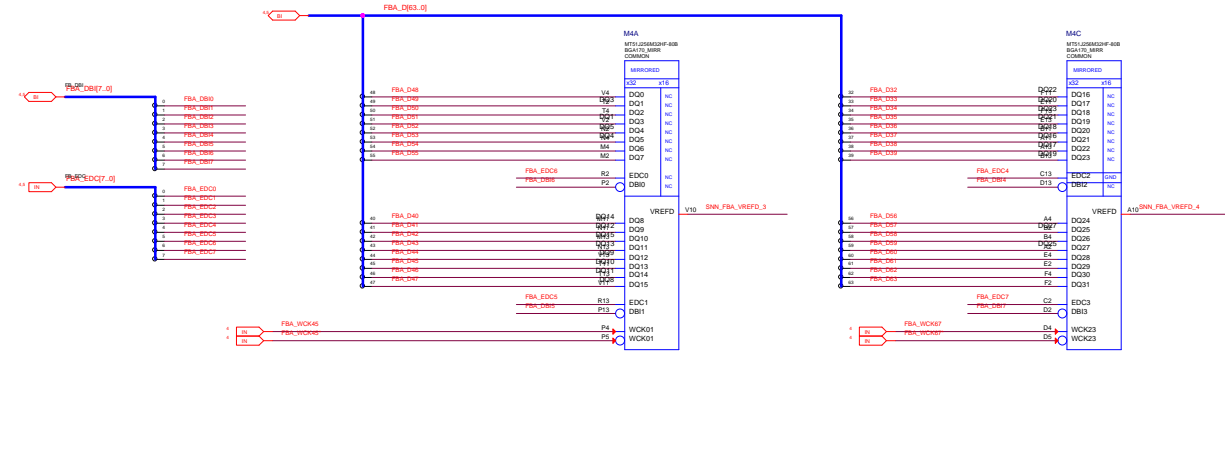
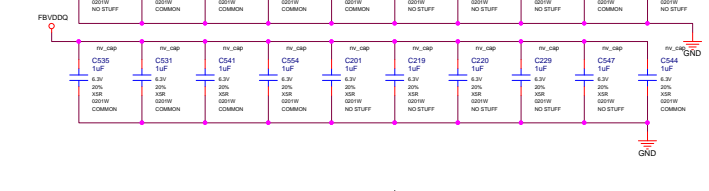
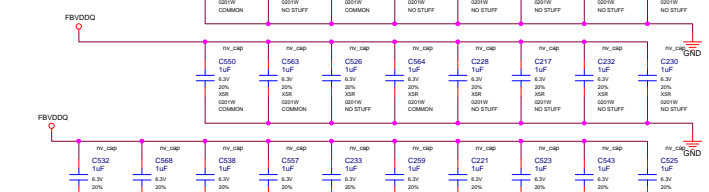
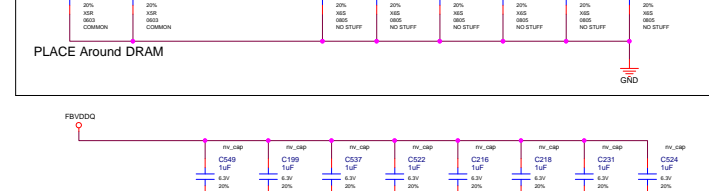
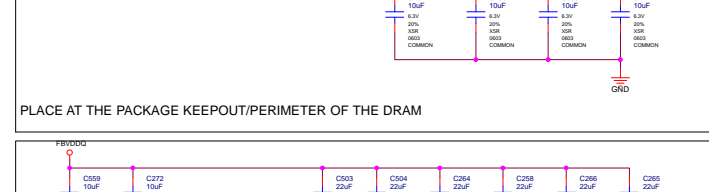
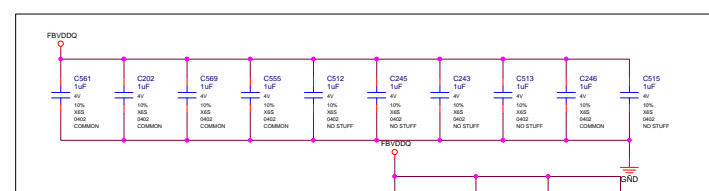
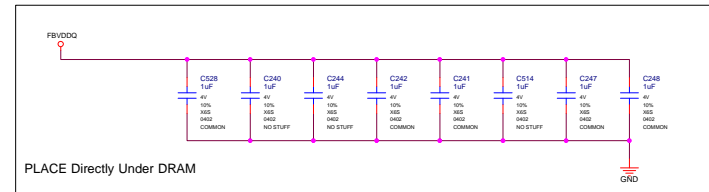
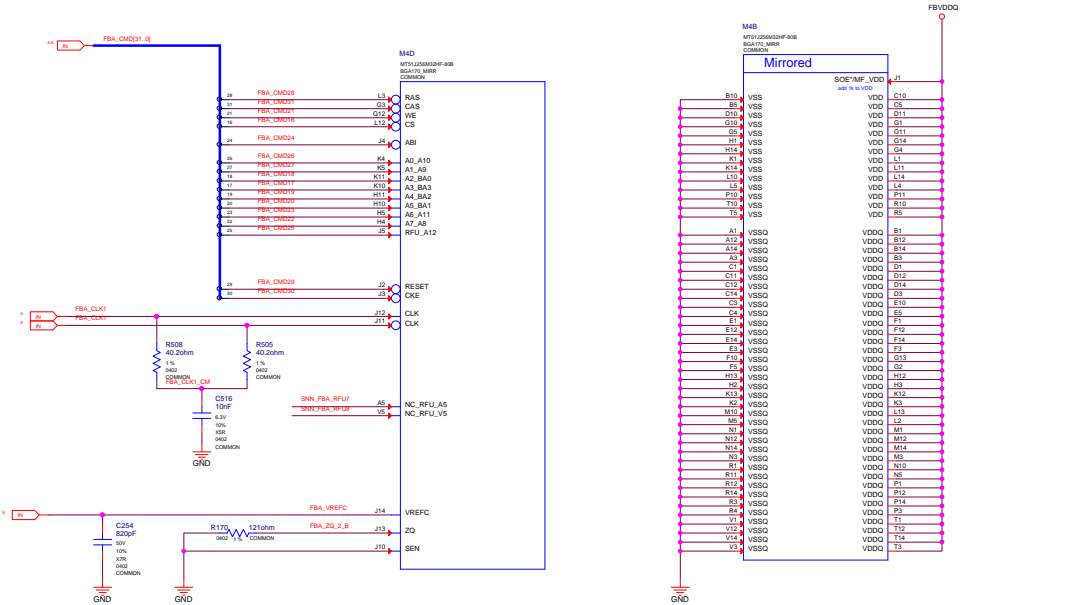
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MEMORY: FBA Partition 63..32

CMD	0..31	32..63
CMD0	C0*	
CMD1	A0_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A6_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	AB_A11	
CMD8	AB*	
CMD9	A12_RFU	
CMD10	AL_A10	
CMD11	A1_A9	C0*
CMD12	RA0*	A0_BA3
CMD13	R0*	A2_BA0
CMD14	RA0*	A4_BA2
CMD15	RA0*	A6_BA1
CMD16	RA0*	WE*
CMD17	RA0*	A7_A8
CMD18	RA0*	AB_A11
CMD19	RA0*	AB*
CMD20	RA0*	A12_RFU
CMD21	RA0*	AL_A10
CMD22	RA0*	A1_A9
CMD23	RA0*	RA0*
CMD24	RA0*	R0*
CMD25	RA0*	RA0*
CMD26	RA0*	RA0*
CMD27	RA0*	RA0*
CMD28	RA0*	RA0*
CMD29	RA0*	RA0*
CMD30	RA0*	RA0*
CMD31	RA0*	RA0*



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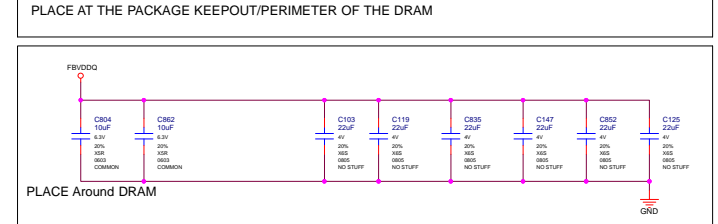
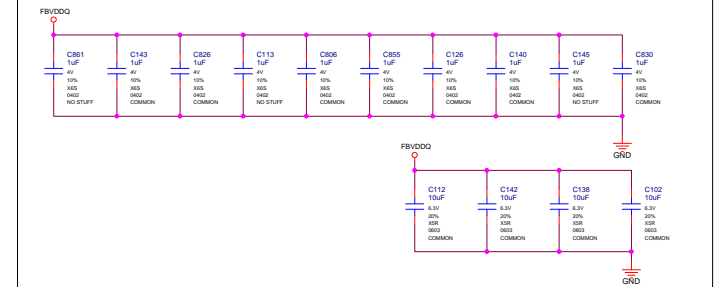
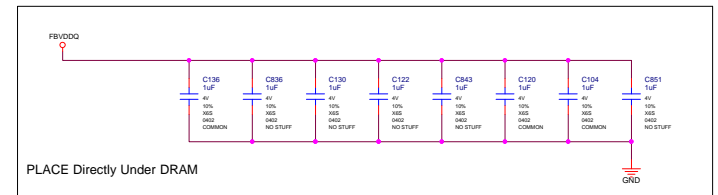
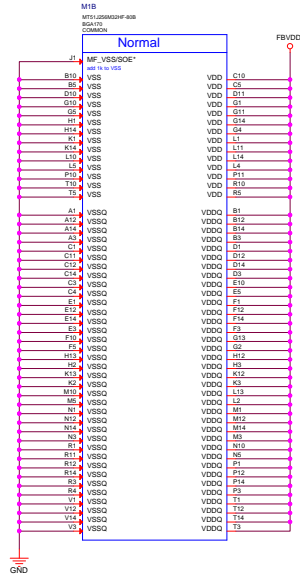
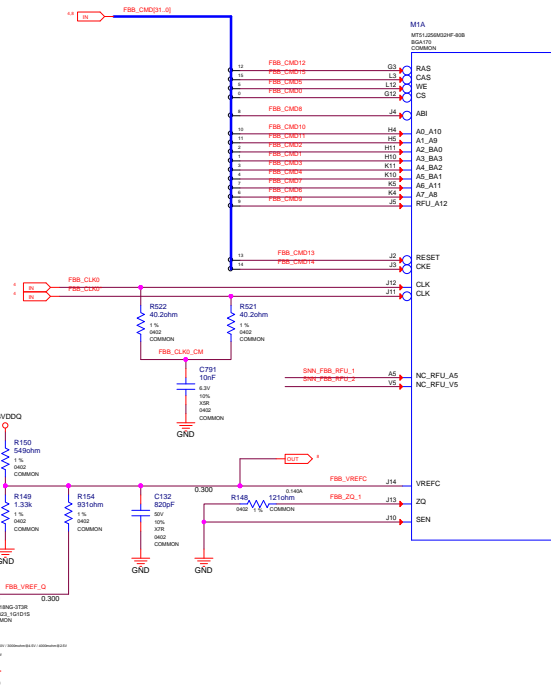
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MEMORY: FBB Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3..BA3	
CMD2	A2..BA2	
CMD3	A4..BA4	
CMD4	A6..BA1	
CMD5	WE*	
CMD6	A7..A8	
CMD7	A6..A11	
CMD8	AB*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A9	
CMD12	RA*	
CMD13	RS*	
CMD14	CK*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3..BA3
CMD18		A2..BA2
CMD19		A4..BA4
CMD20		A6..BA1
CMD21		WE
CMD22		A7..A8
CMD23		A6..A11
CMD24		AB*
CMD25		A12..RFU
CMD26		A0..A10
CMD27		A1..A9
CMD28		RA*
CMD29		RS*
CMD30		CK*
CMD31		CAS*

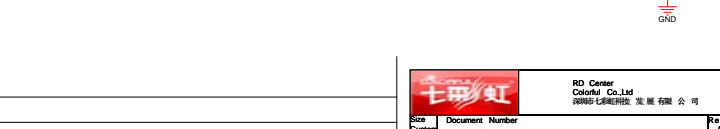
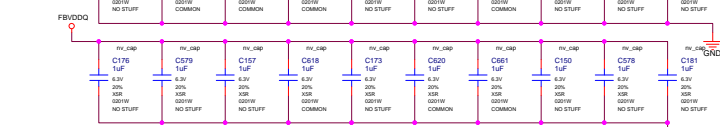
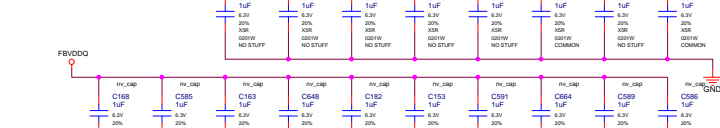
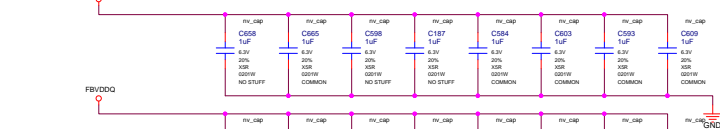
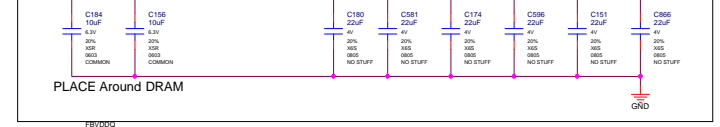
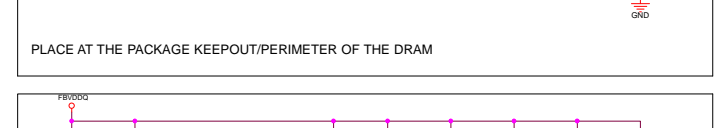
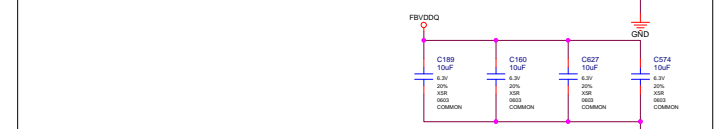
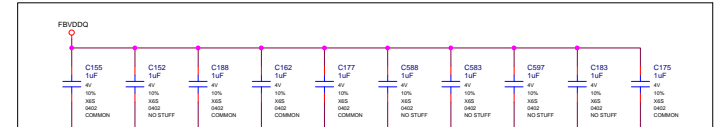
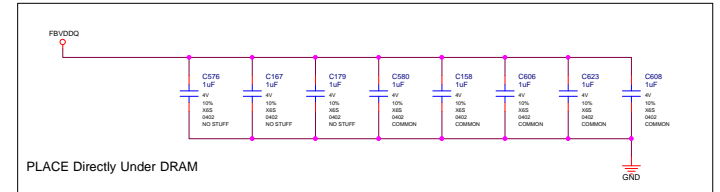
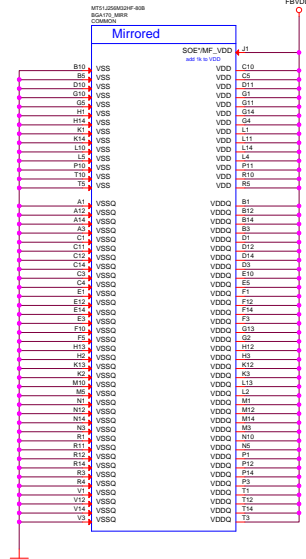
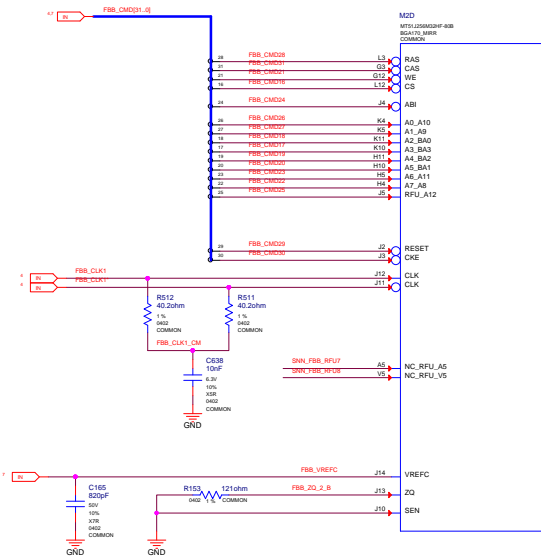


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MEMORY: FBB Partition 63..32

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA2	
CMD3	A4_BA2	
CMD4	A3_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	ALL_A11	
CMD8	AB*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A8	
CMD12	RAS*	
CMD13	RST*	
CMD14	CHE*	
CMD15	CAS*	
CMD16		
CMD17		
CMD18		
CMD19		
CMD20		
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CMD26		
CMD27		
CMD28		
CMD29		
CMD30		
CMD31		



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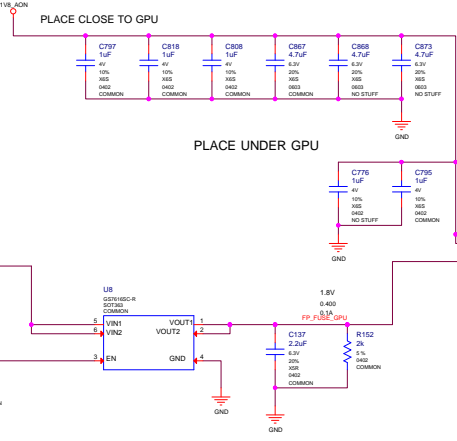
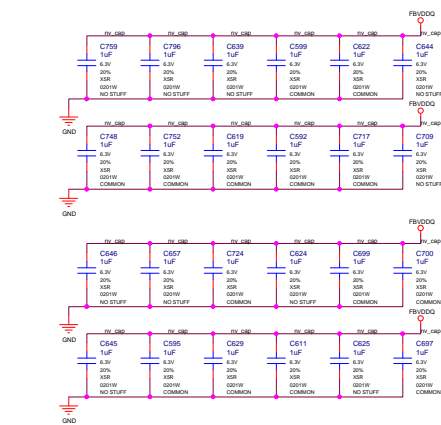
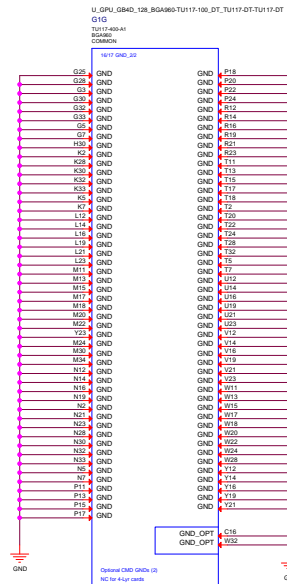
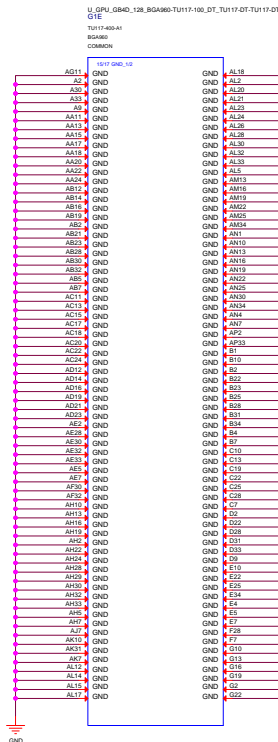
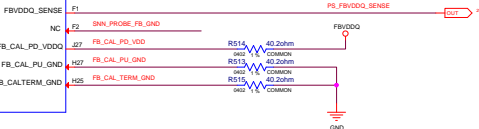
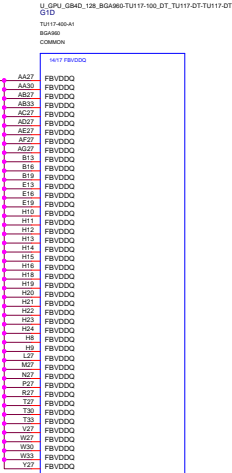
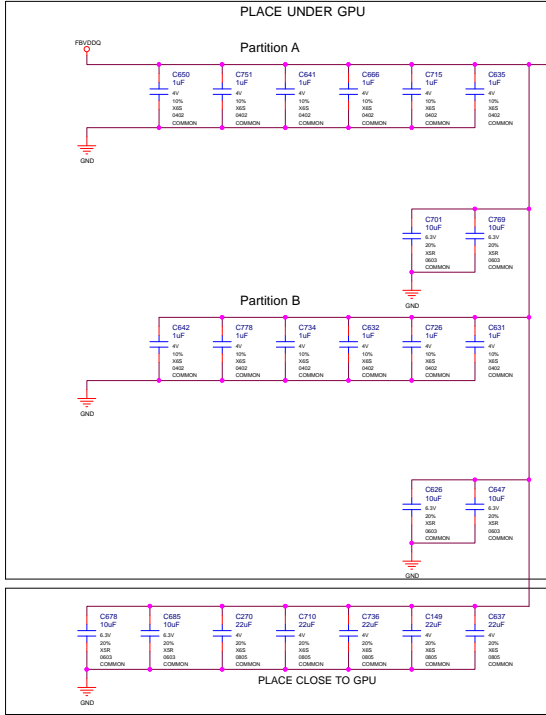
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GPU FBVDDQ & 1V8 Decoupling



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ASSEMBLY	-ASSEMBLY DESCRIPTION-
PAGE DETAIL	GPU FBVDDQ & 1V8 Decoupling

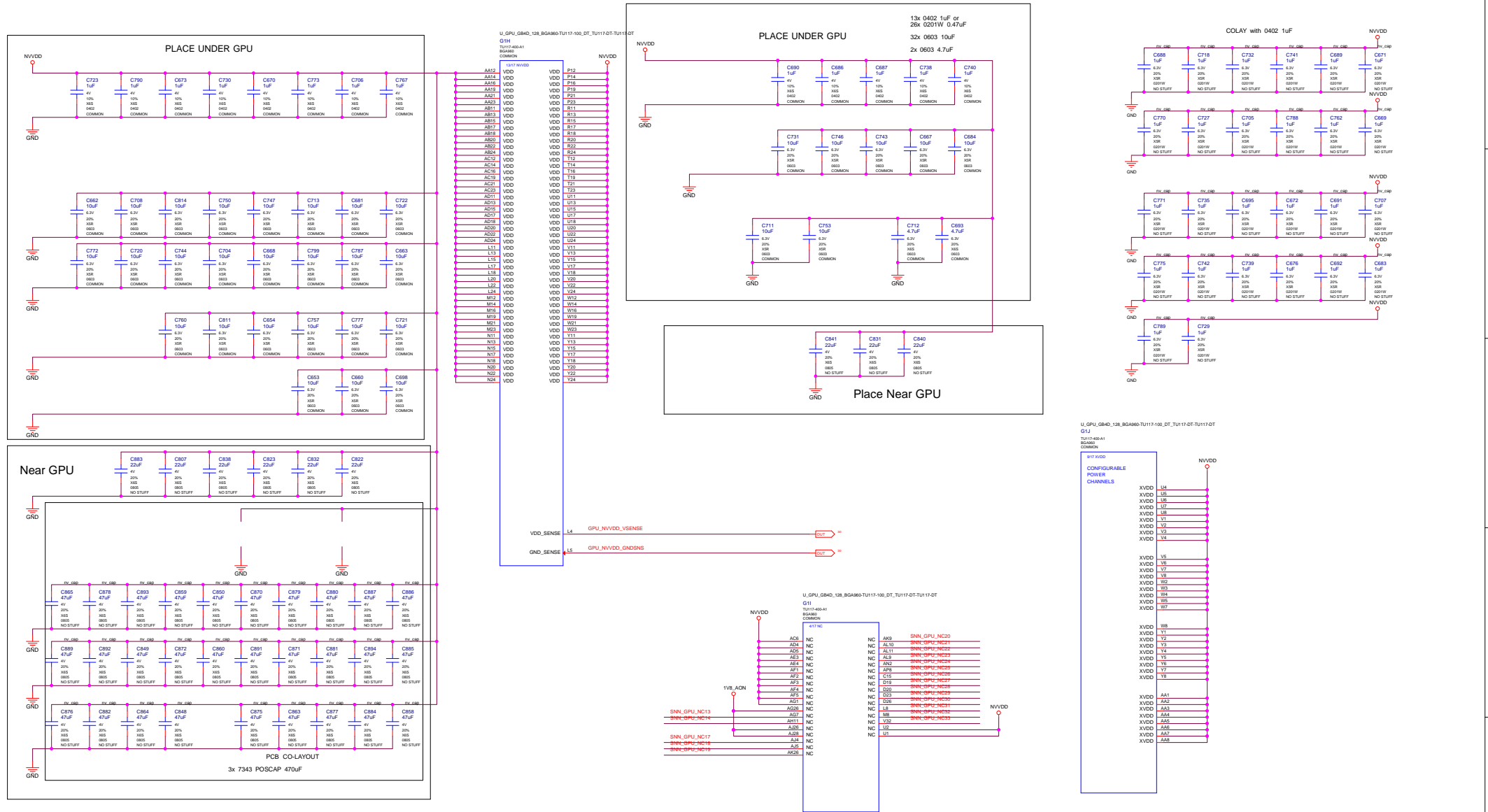


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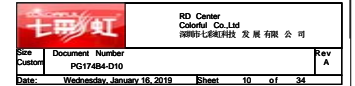
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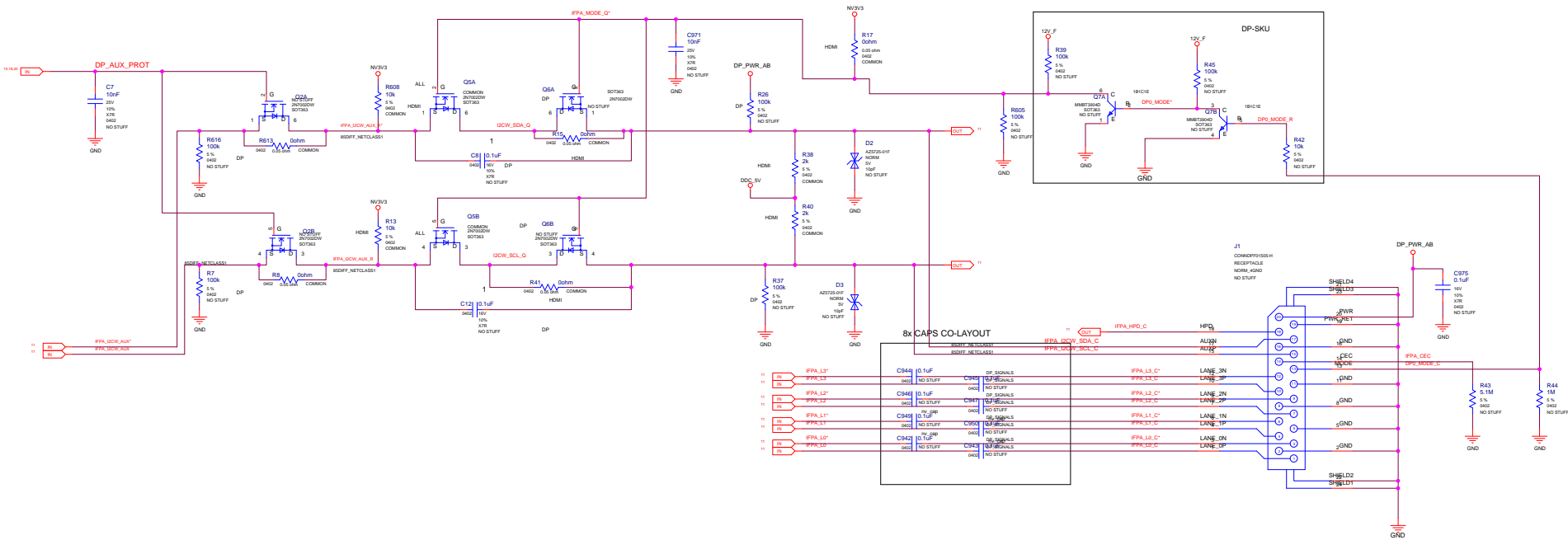
GPU NVVDD Decoupling



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU NVVDD DECOUPLING



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IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	IFPA DP

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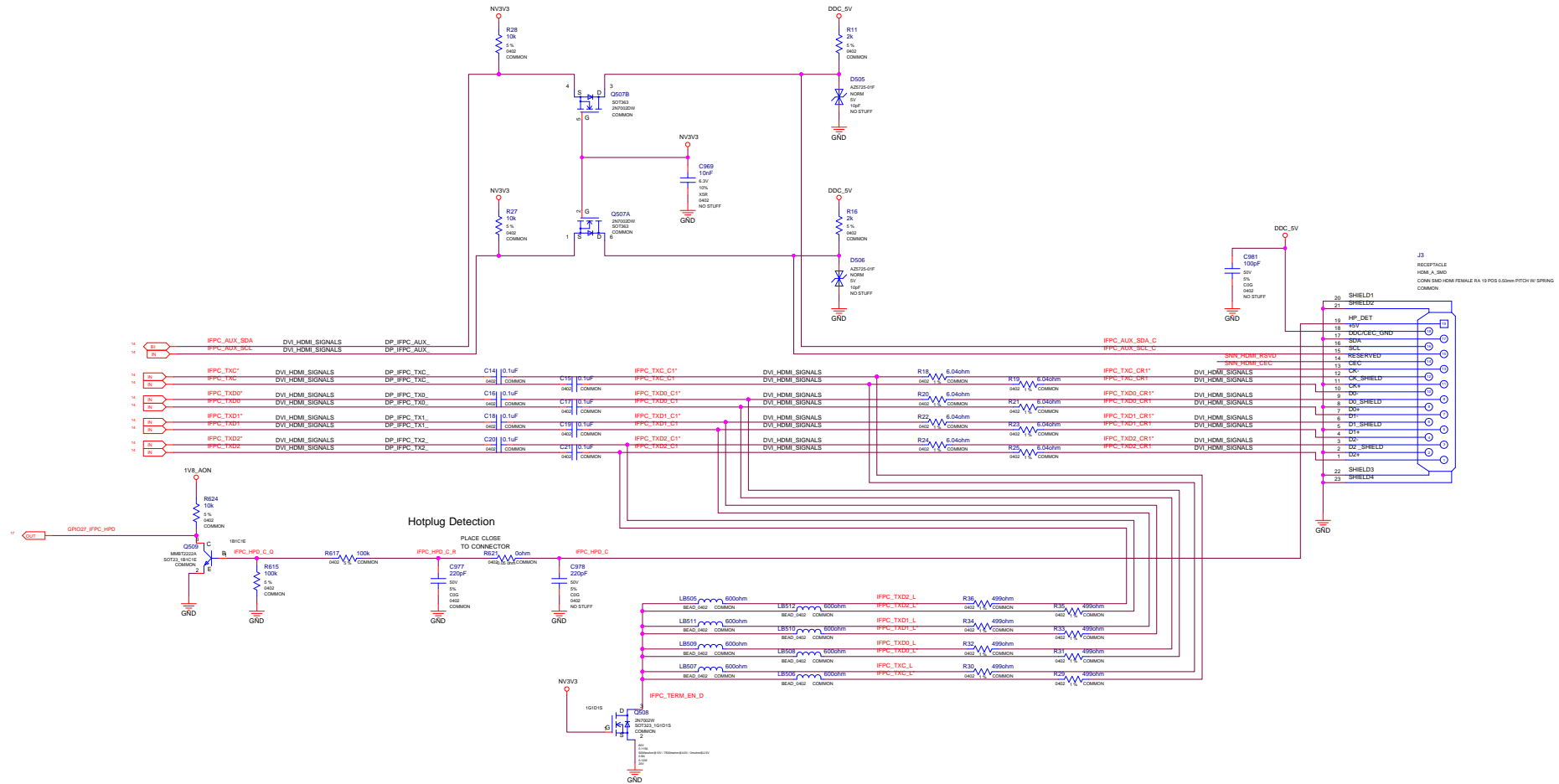


ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	IFPC


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IFPC HDMI

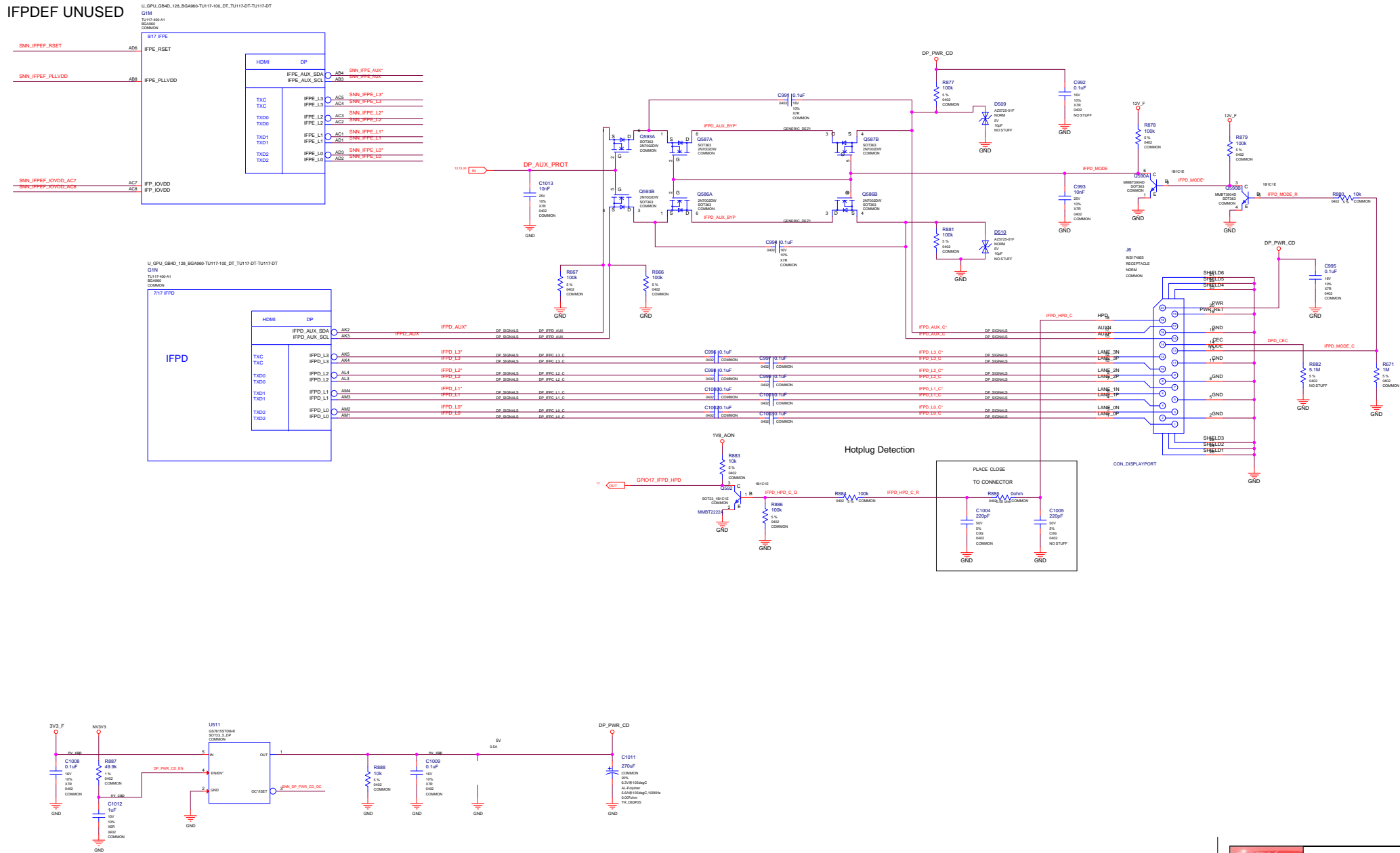


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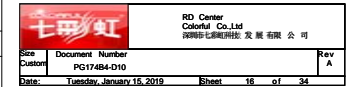
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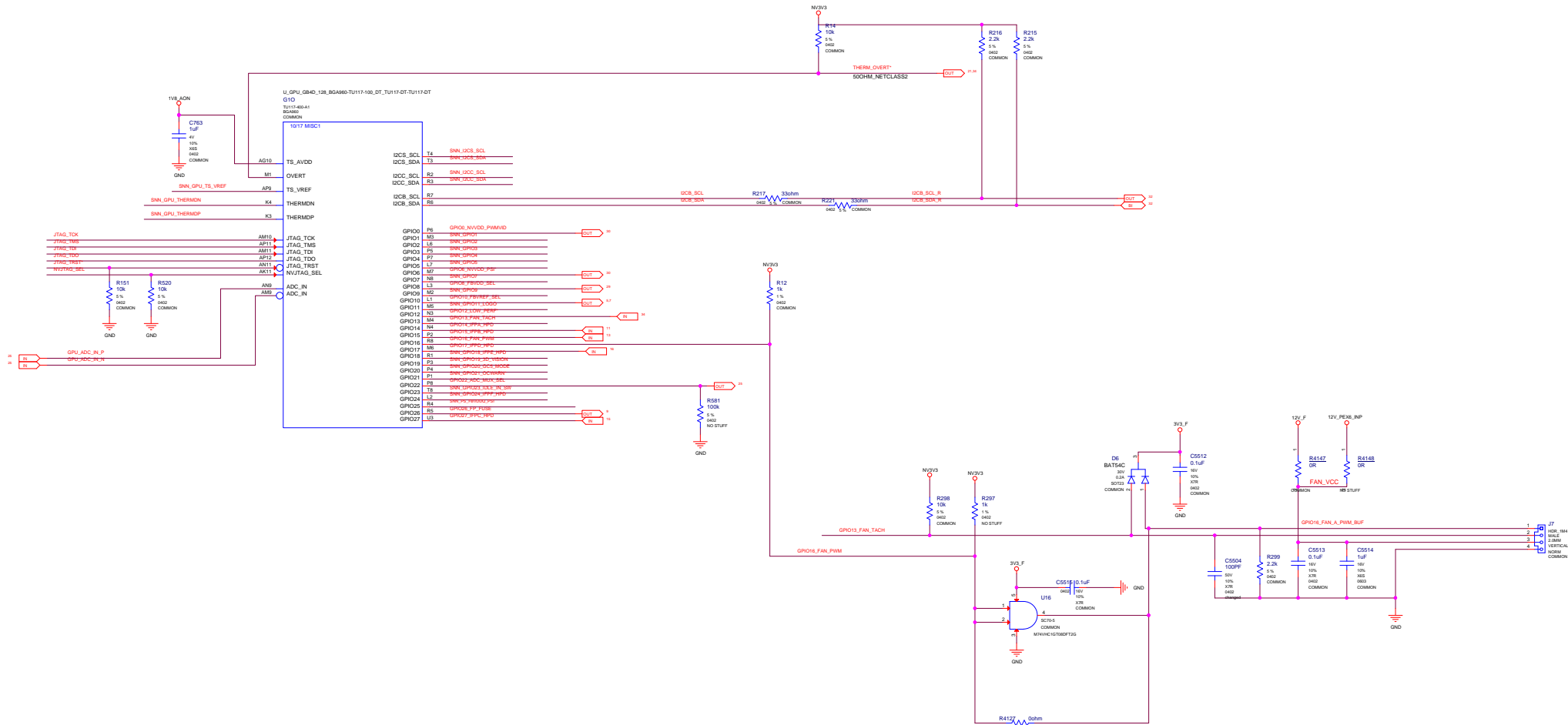


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MISC1: GPIO, Fan, Thermal, JTAG



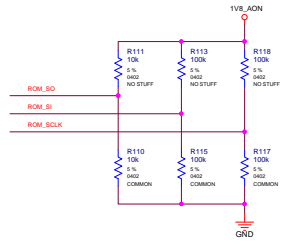
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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO

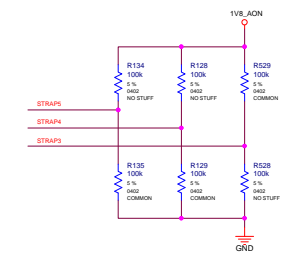
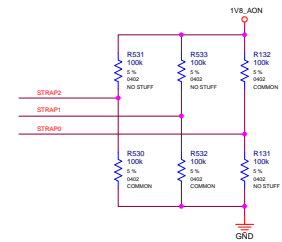
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MISC2: ROM, XTAL, Straps

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0].FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	xxx1	FS_OVERT ENABLE	Default
L	L	M	xxx0	FS_OVERT DISABLE	



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

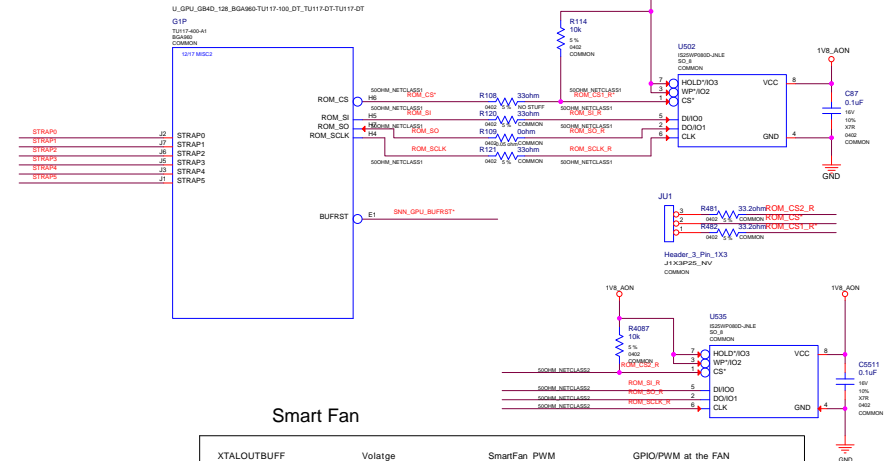


```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

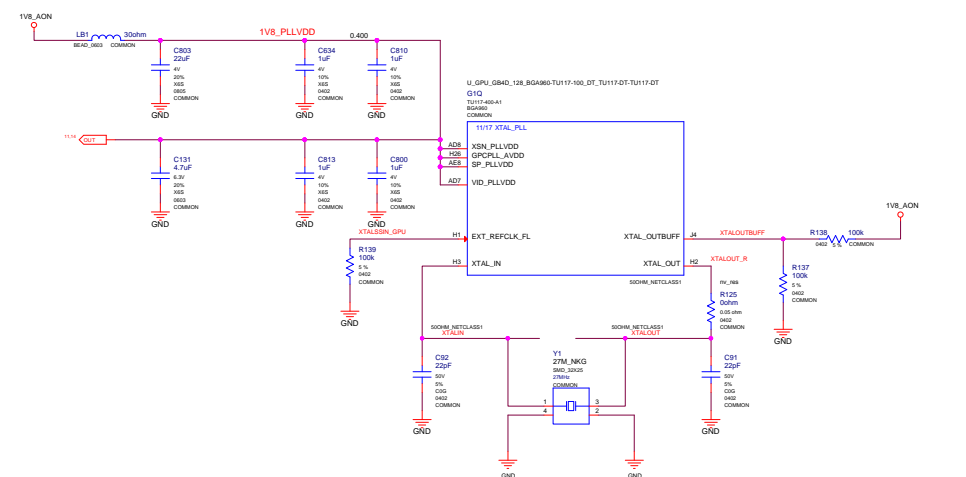
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```



Smart Fan

XTALOUTBUFF	Voltage	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



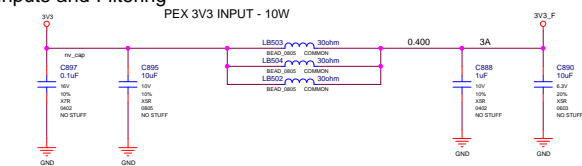
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

ASSEMBLY	«ASSEMBLY_DESCRIPTION
PAGE DETAIL	MISC2: ROM, XTAL, Straps

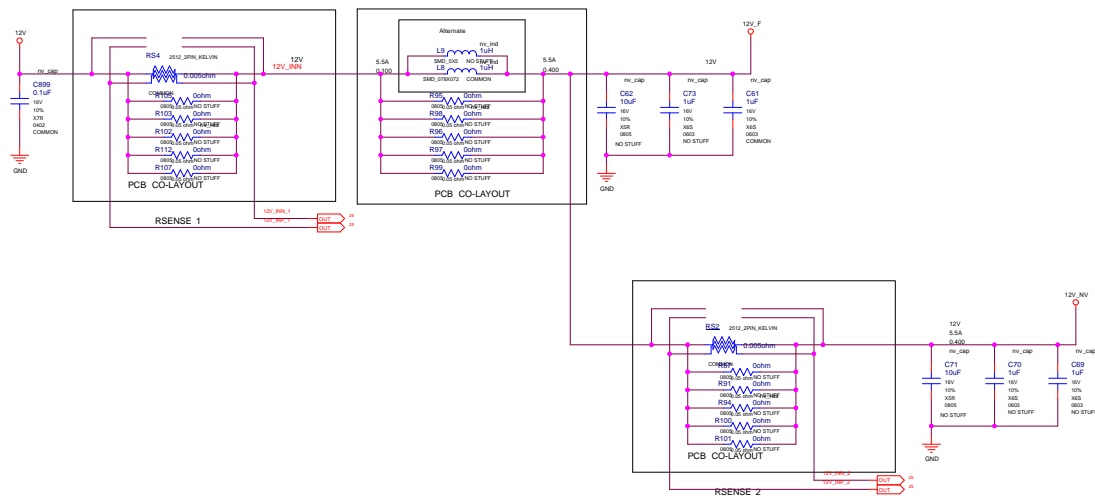
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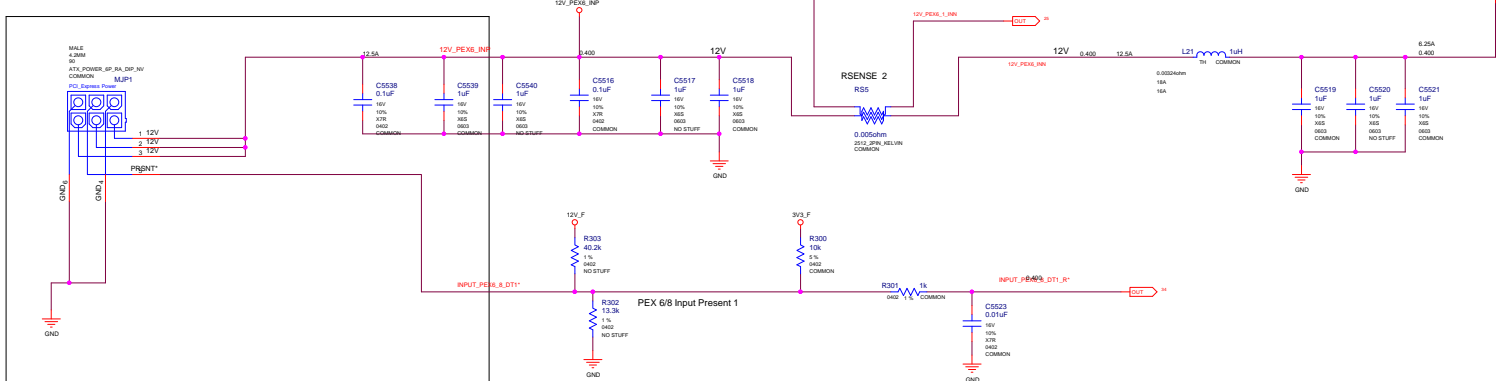
Power Inputs and Filtering



PEX_12V INPUT - 66W



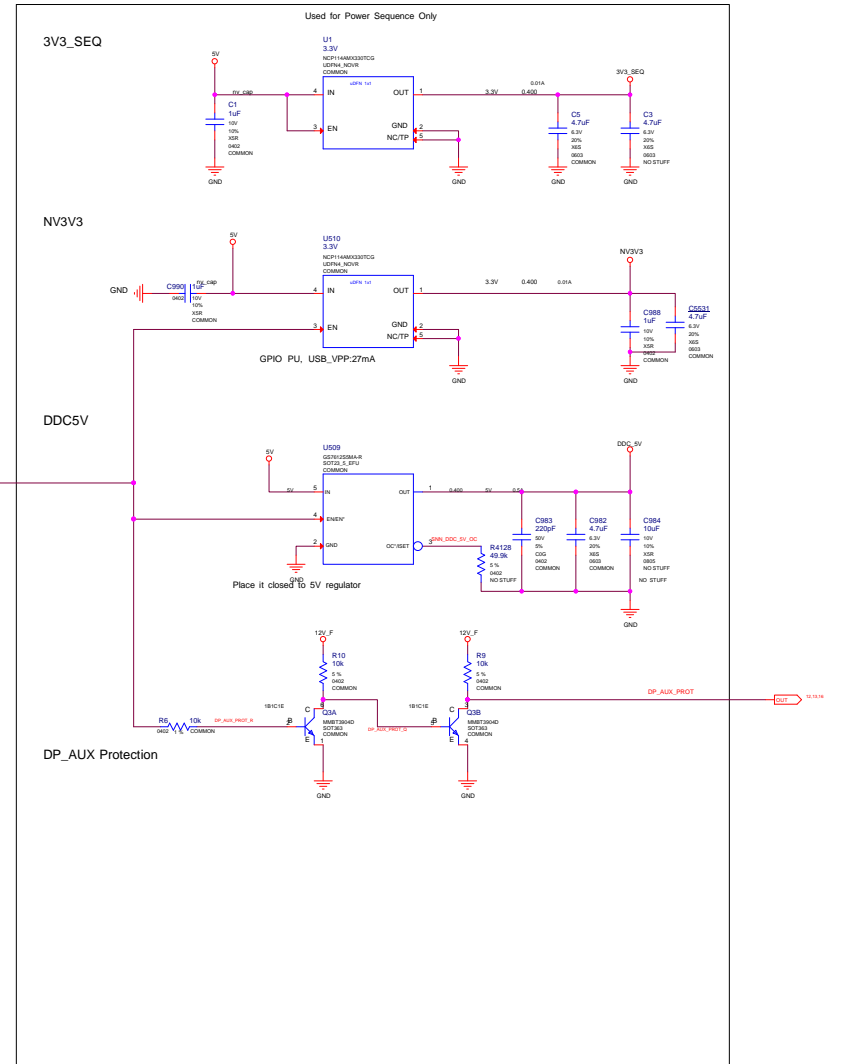
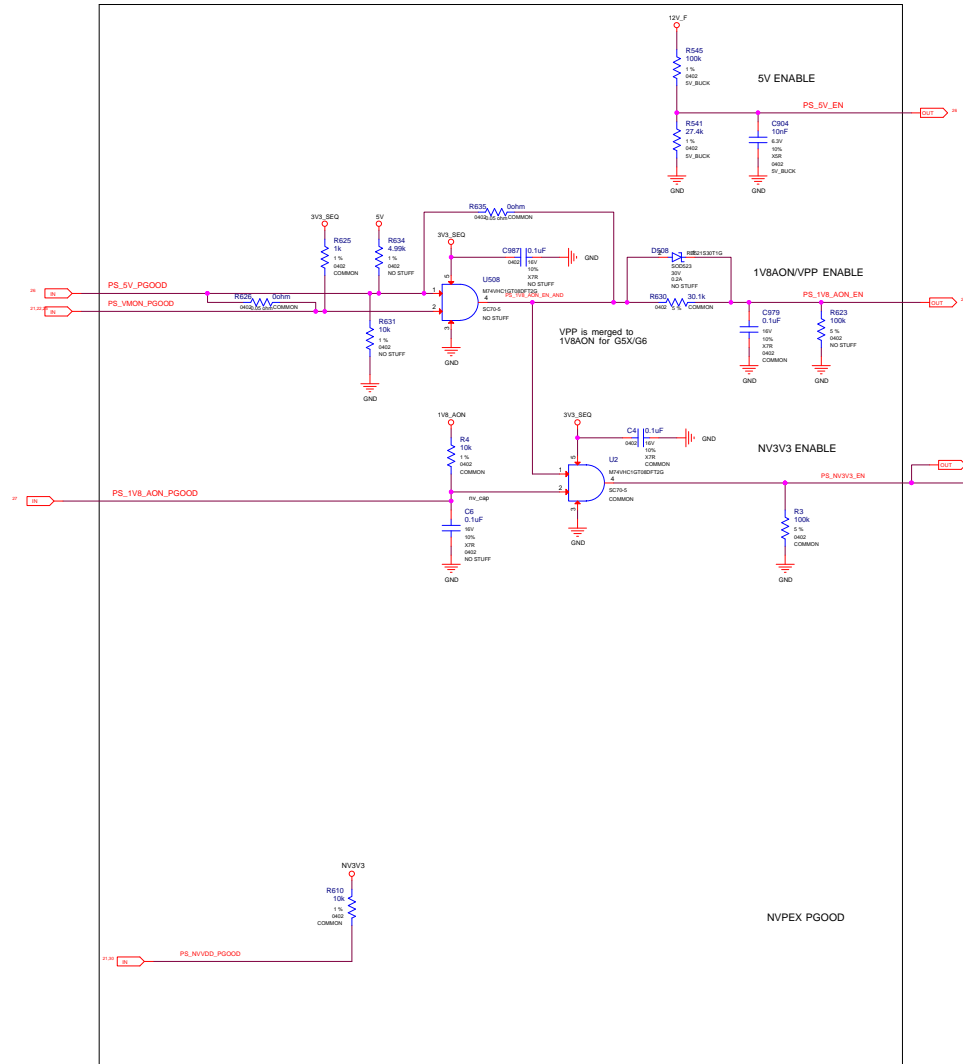
PEX6 INPUT 1 - 2x3 PCIE CON 75W



ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	Power Inputs and Filtering

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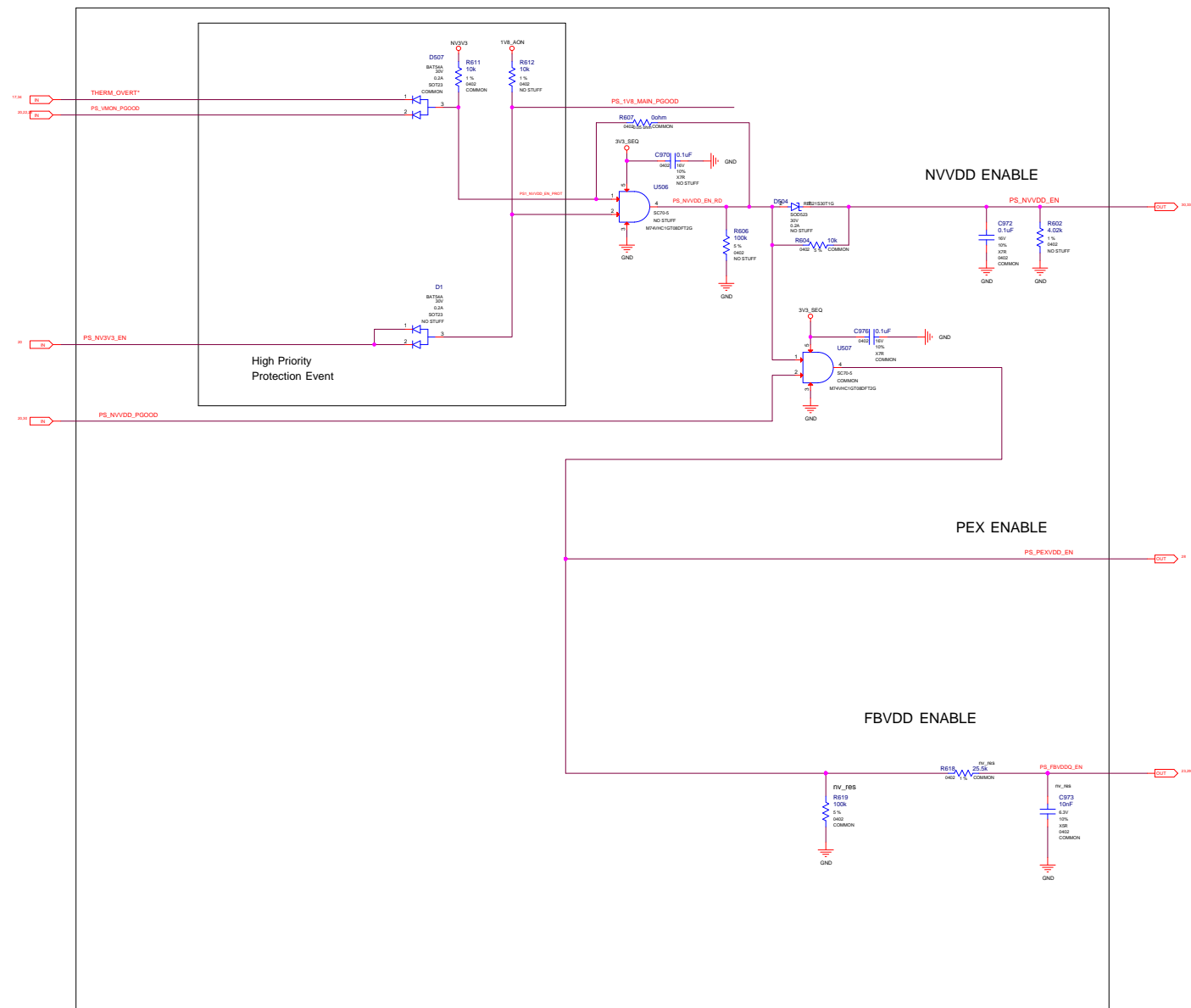
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SEQ:NV,PEX,FB ENABLE

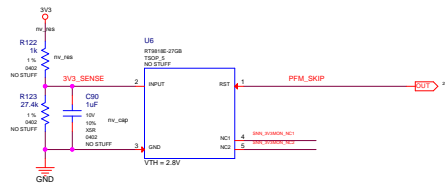
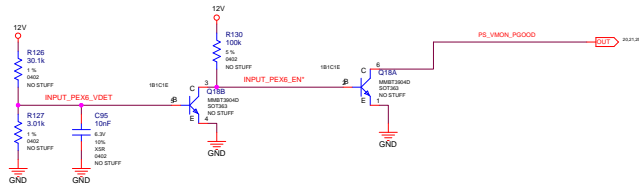


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PAGE DETAIL	SEQ: NV, PEX, FB ENABLE

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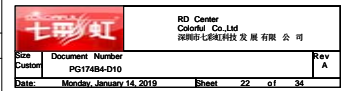
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SEQUENCE:Voltage Monitor

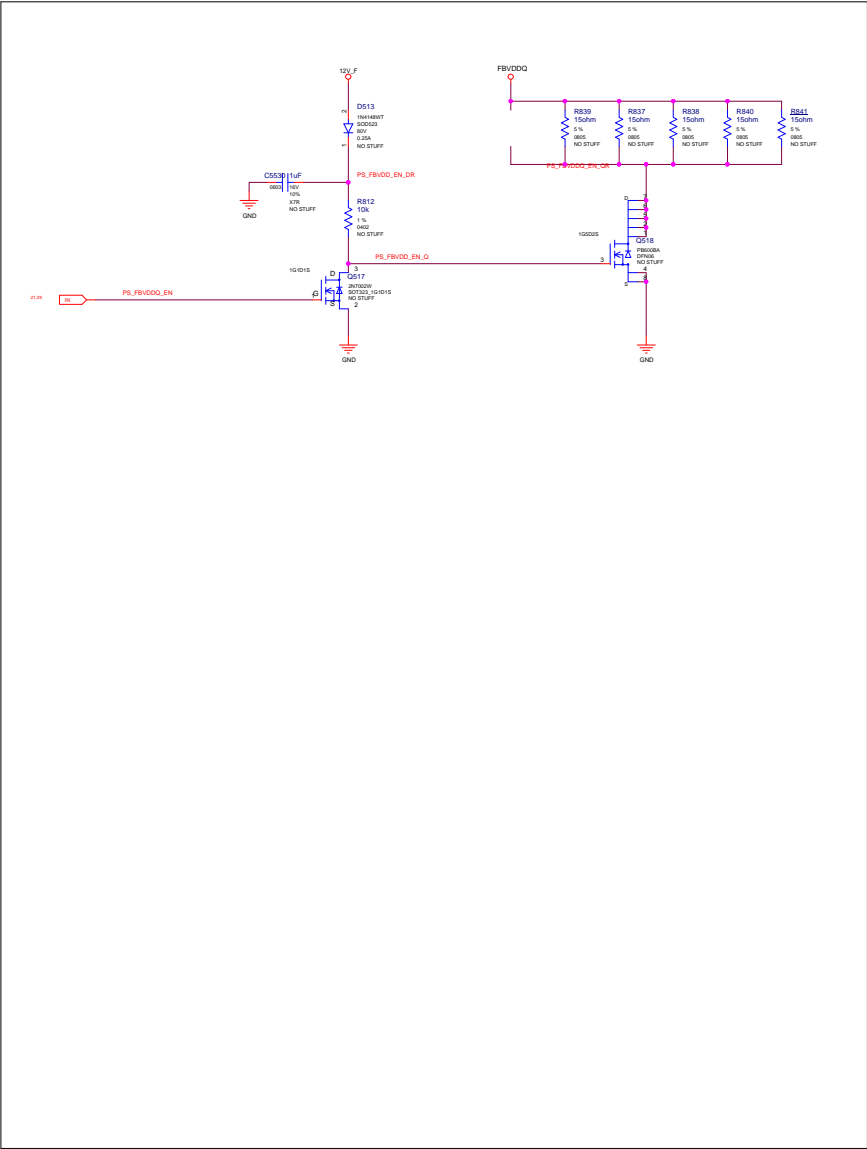


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PAGE DETAIL	SEQ: VOLTAGE MONITOR

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SEQUENCE:Discharge

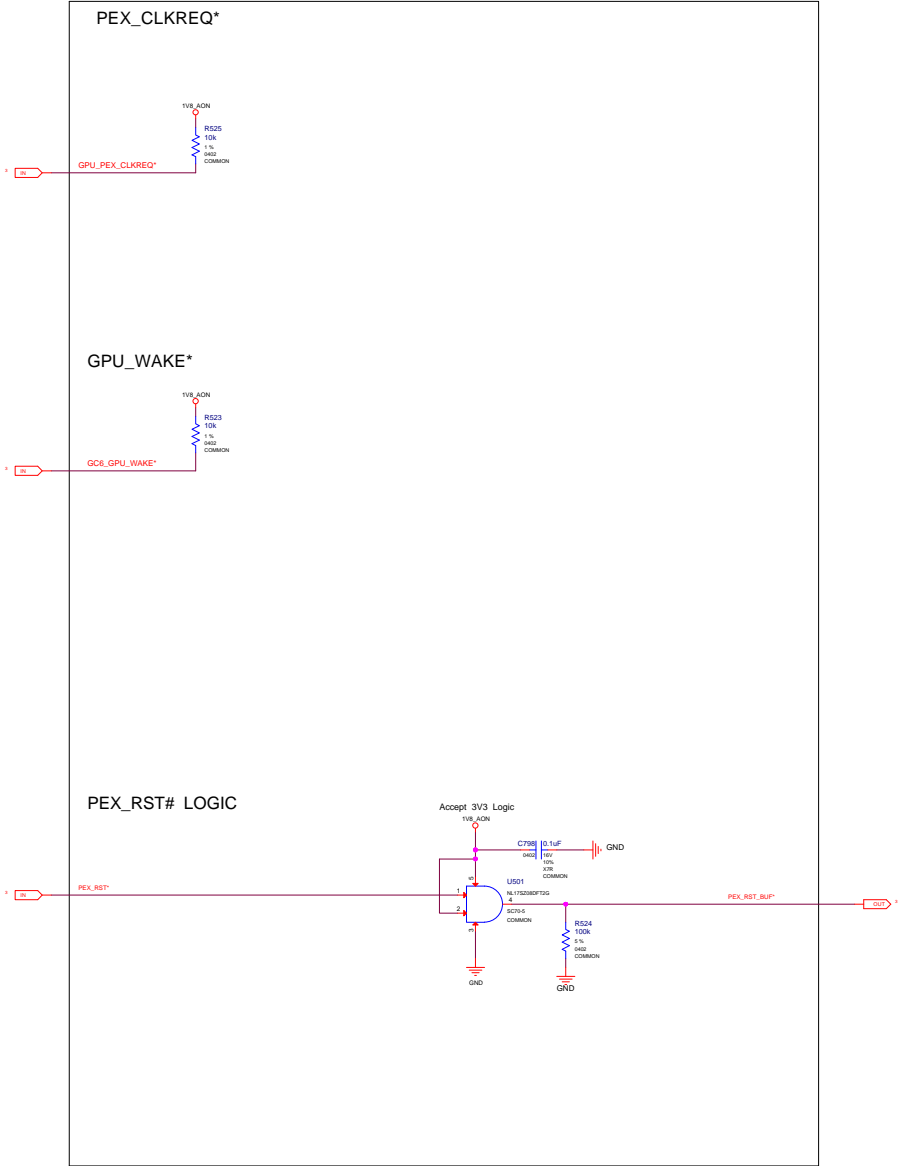


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ASSEMBLY	<ASSEMBLY DESCRIPTION>
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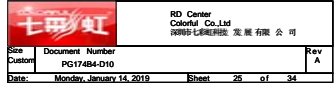
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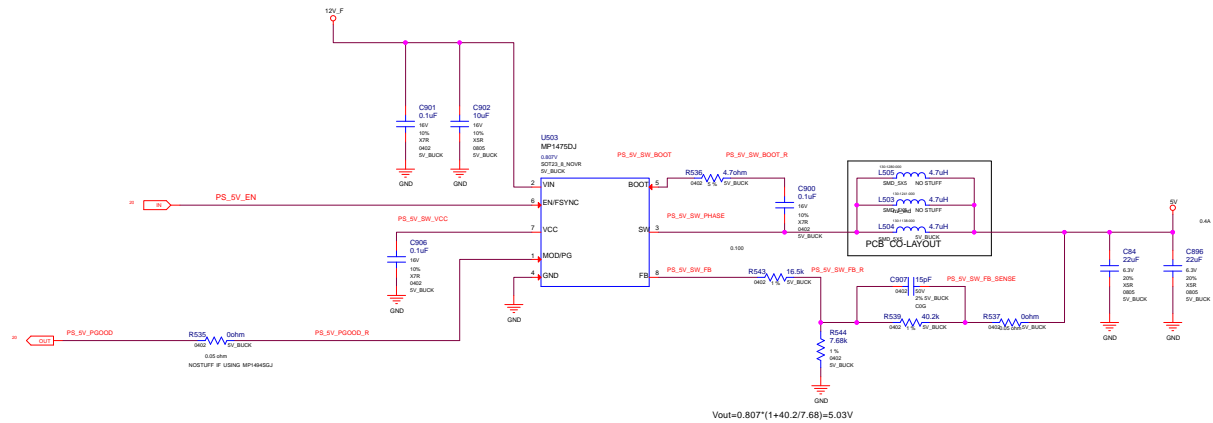
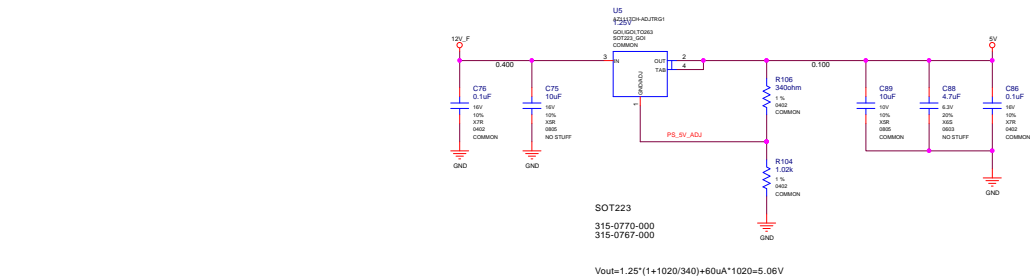
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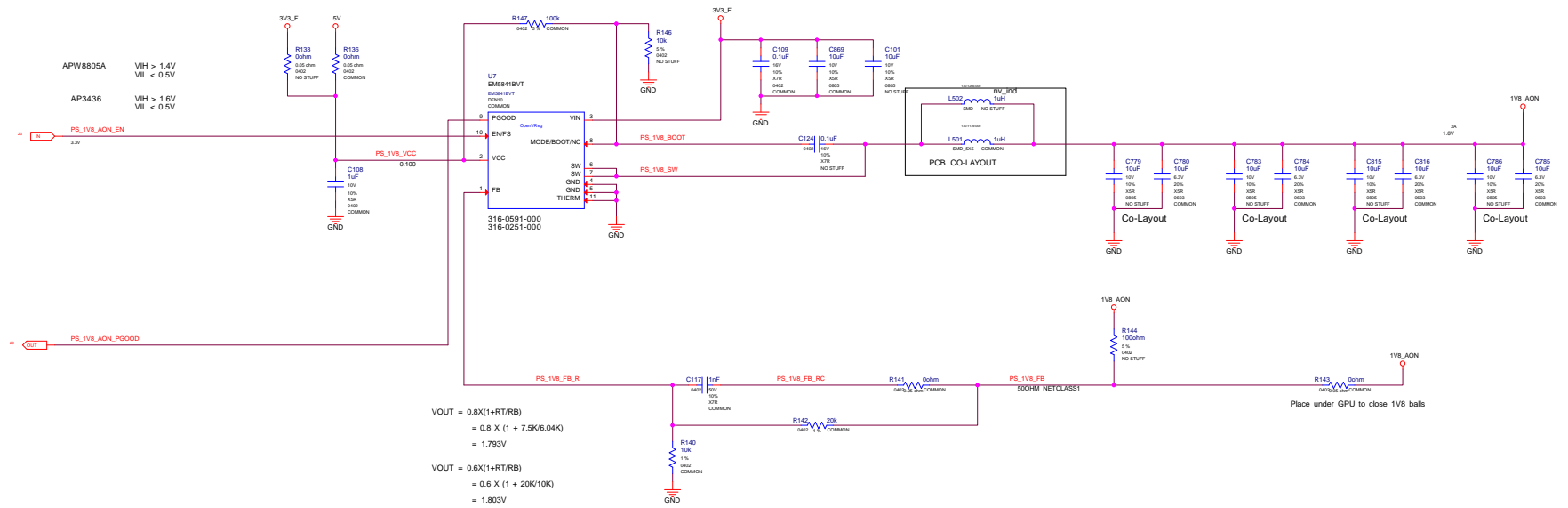
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ASSEMBLY	ASSEMBLY DESCRIPTION
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PS: 1V8

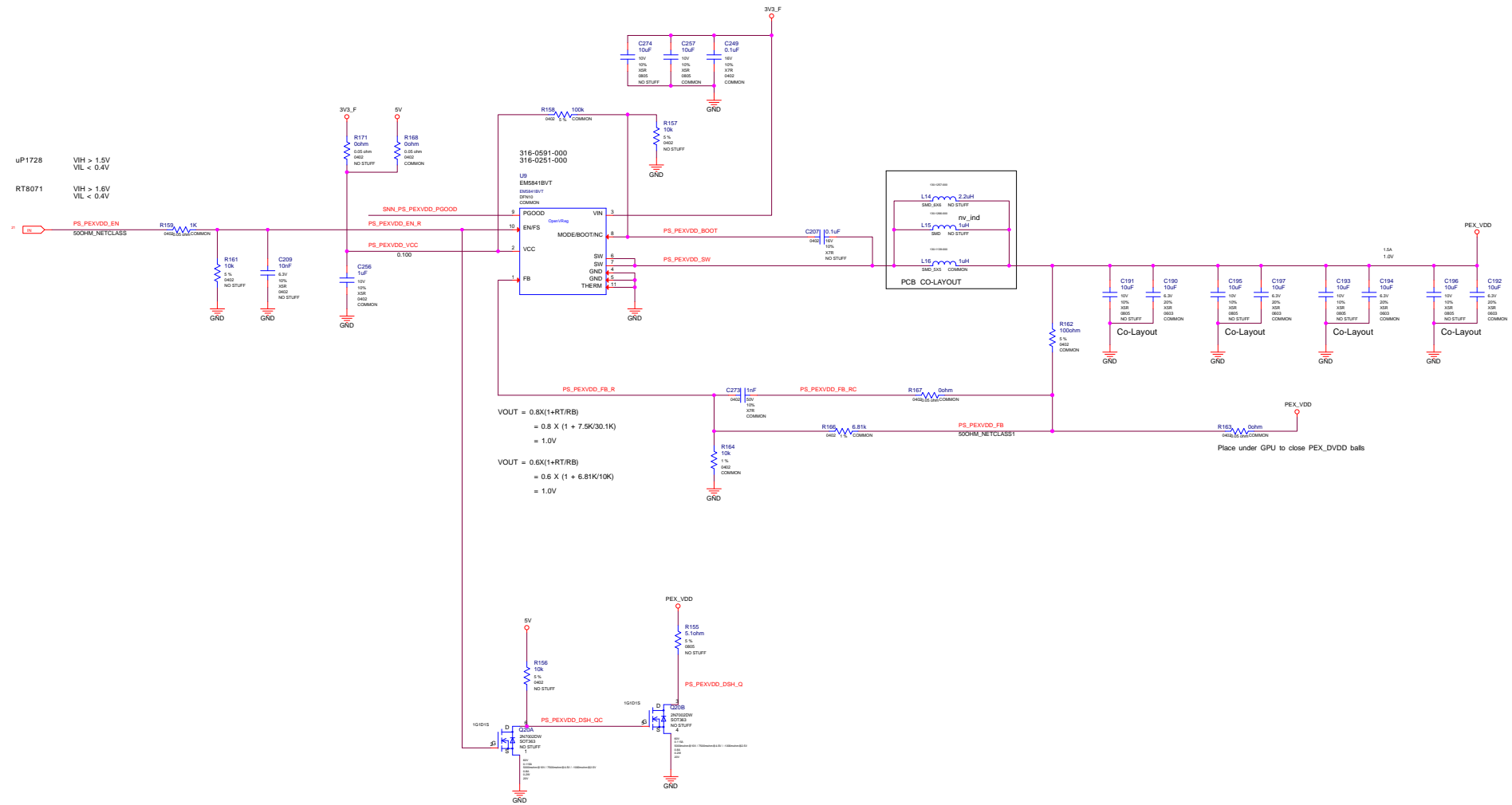


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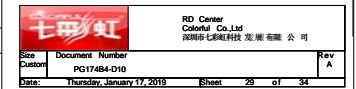
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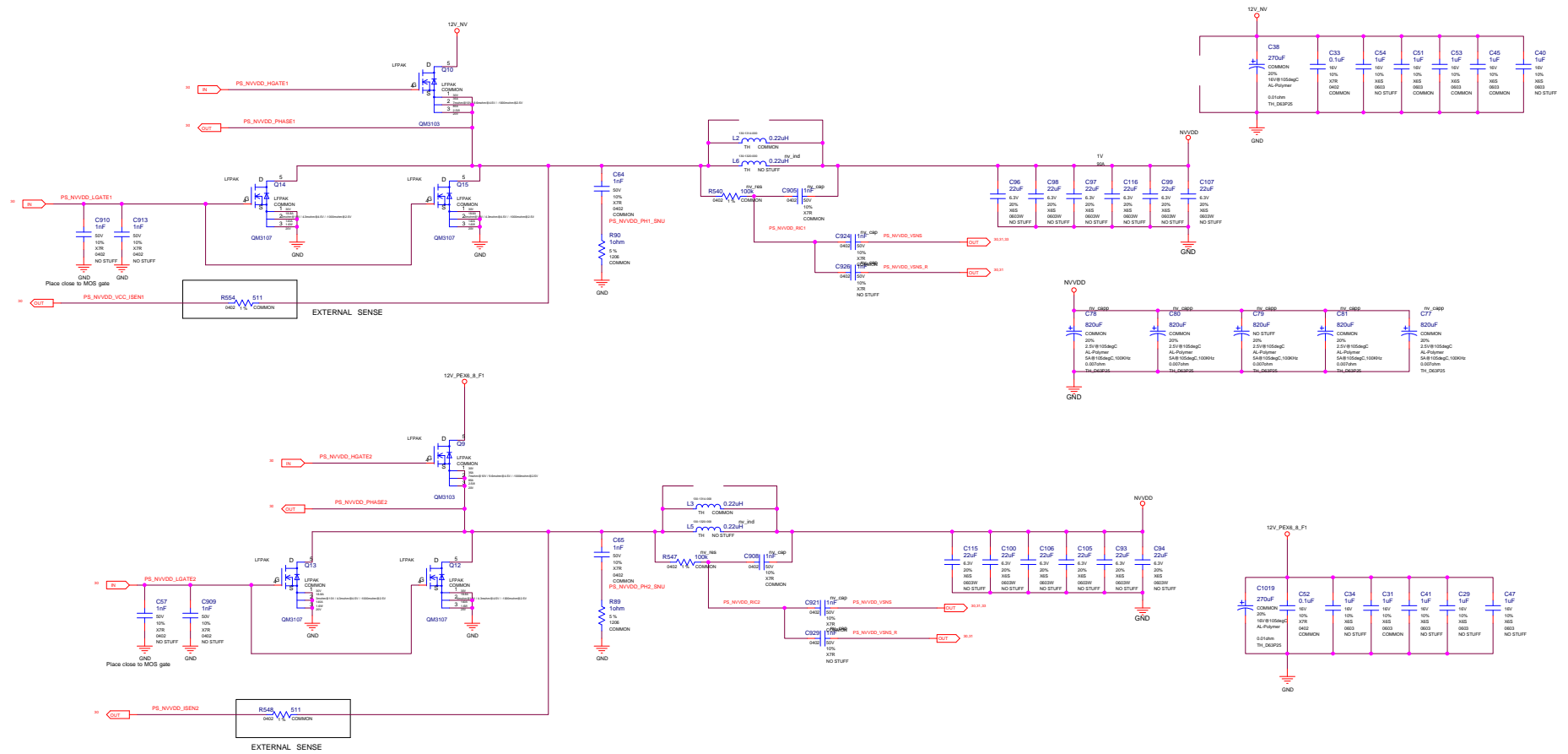
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PS: NVVDD Phase 1,2



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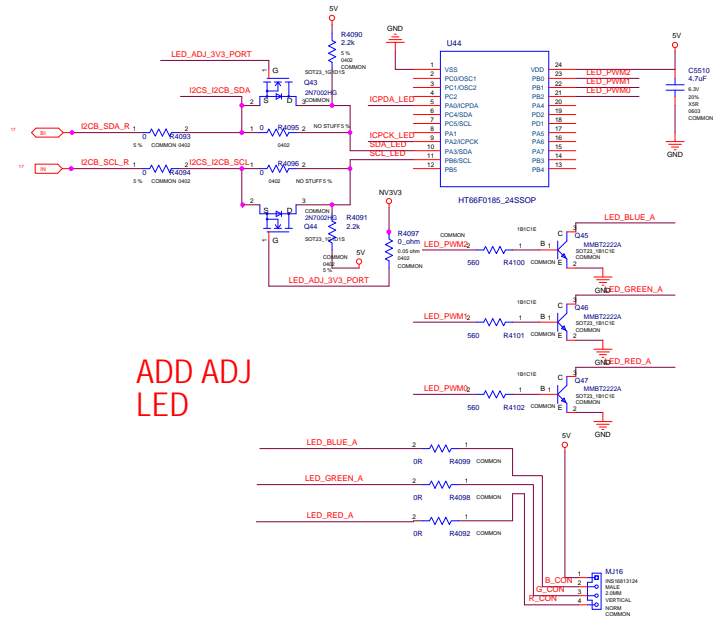
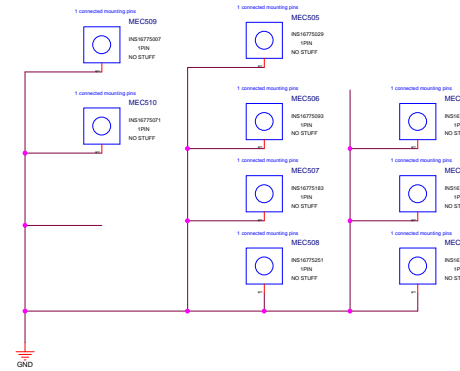
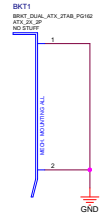


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Mechanical: Bracket/Thermal Solution

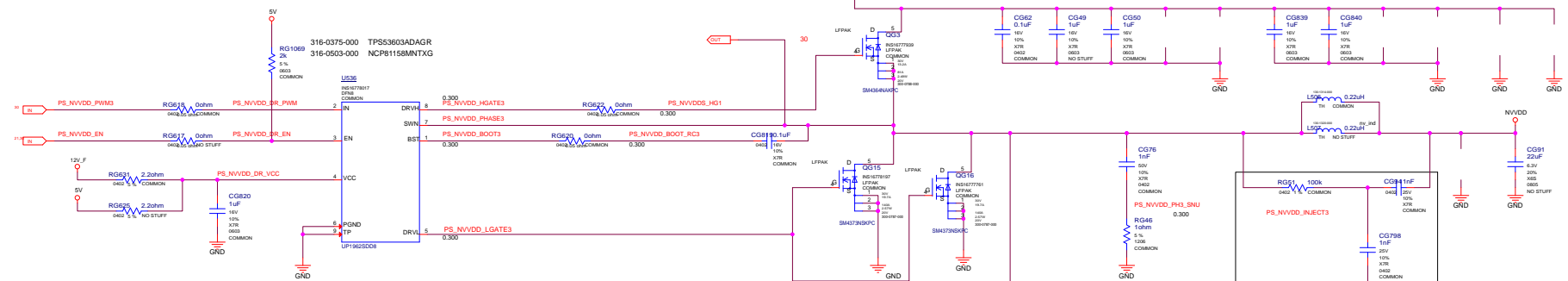
Brackets:



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PAGE DETAIL	MECH: Bracket/Thermal

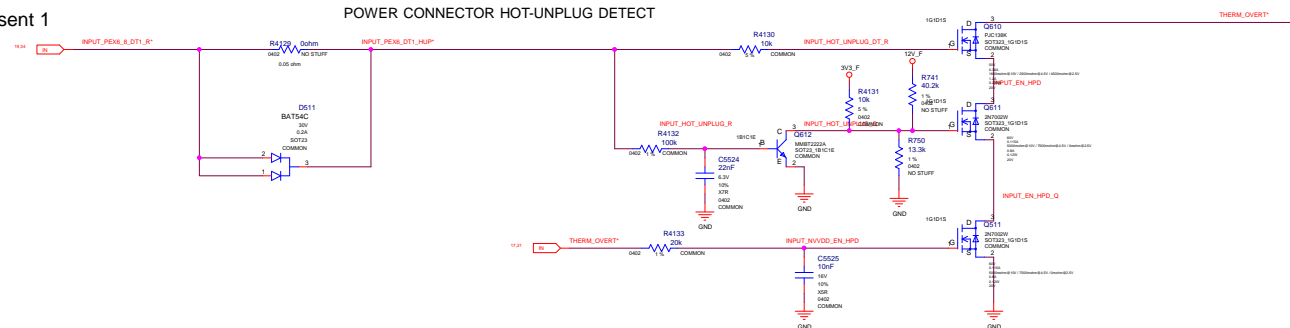
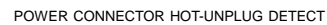
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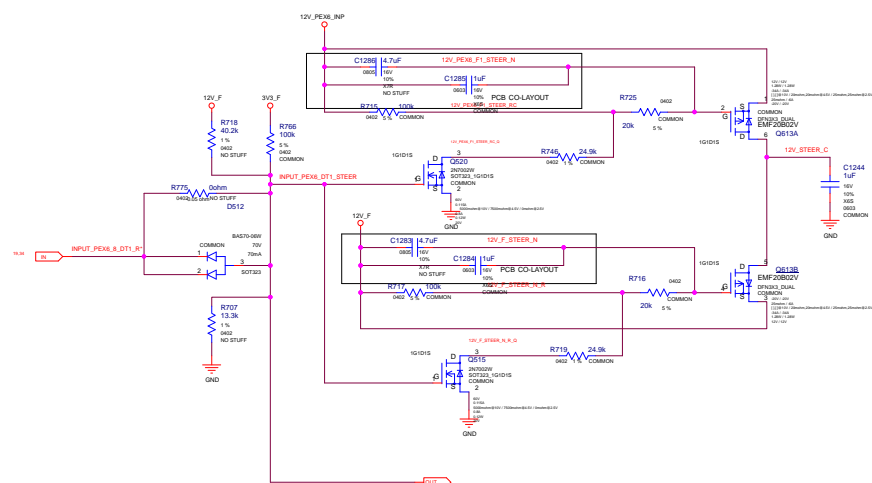


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GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



GPI012_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: STEERING, UPB & HOT-UNPLUG

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