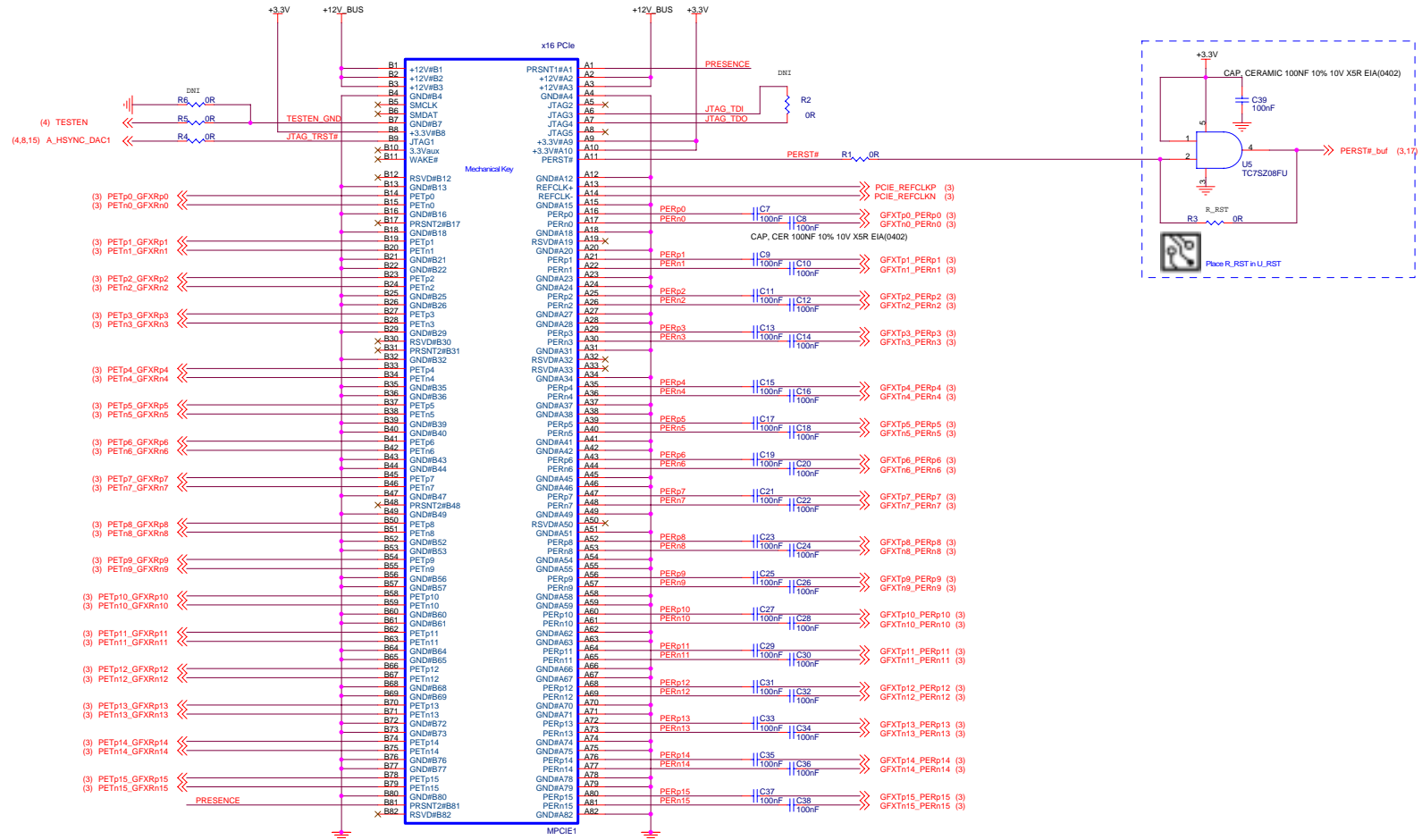
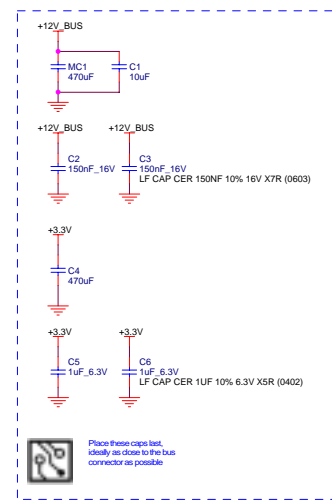


# PCI-EXPRESS EDGE CONNECTOR



Power Sequence Circuit to ensure SMPS\_EN is released after +12V\_BUS and +3.3V\_BUS are both in regulation. Pull-up may or may not be required on SMPS\_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS\_EN will be held low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS\_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS\_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

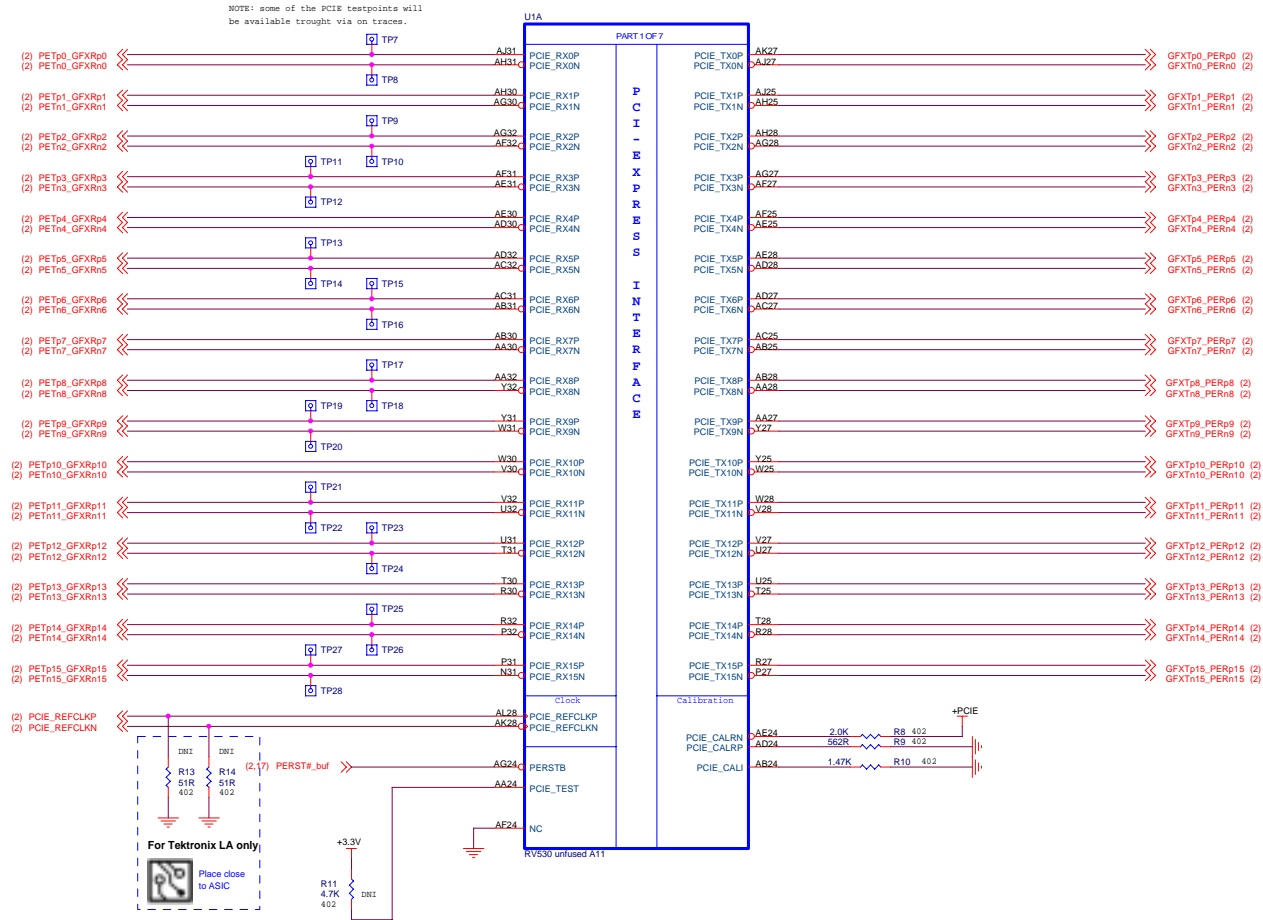
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND



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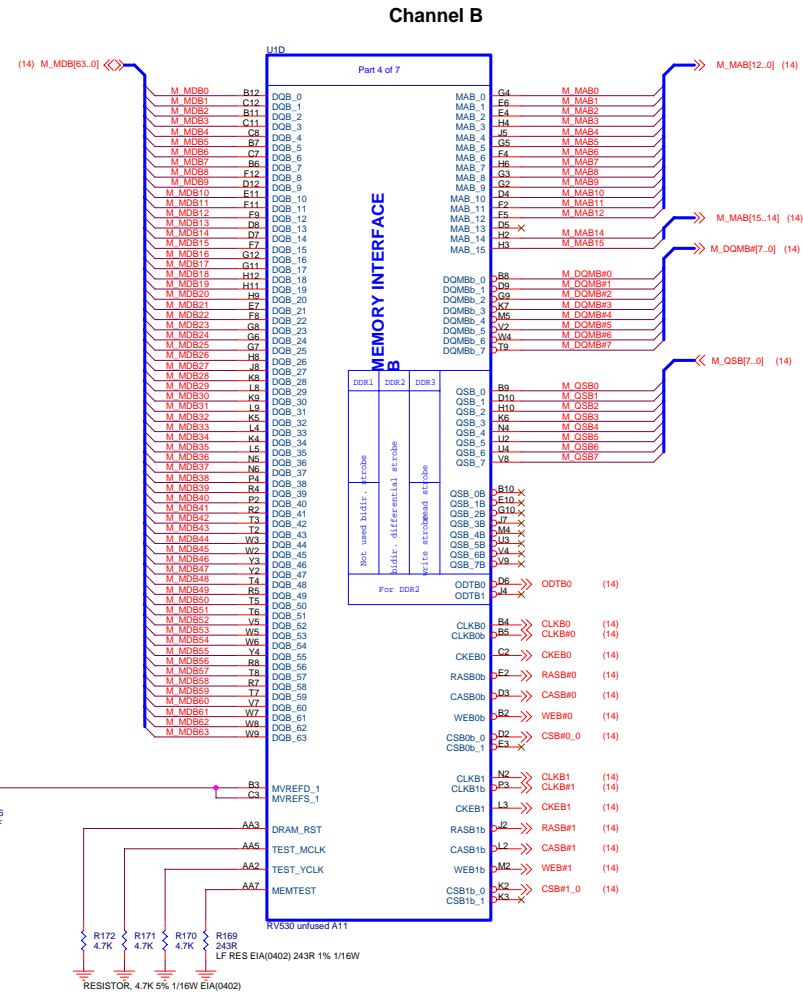
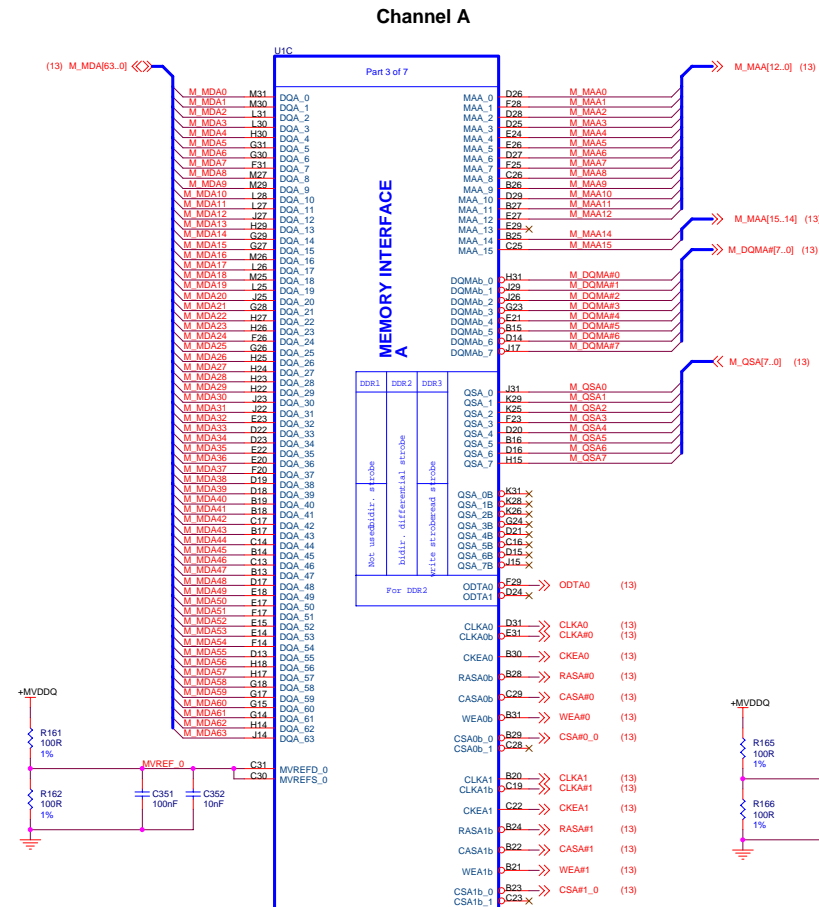
MS-V040 RV530/DDRII

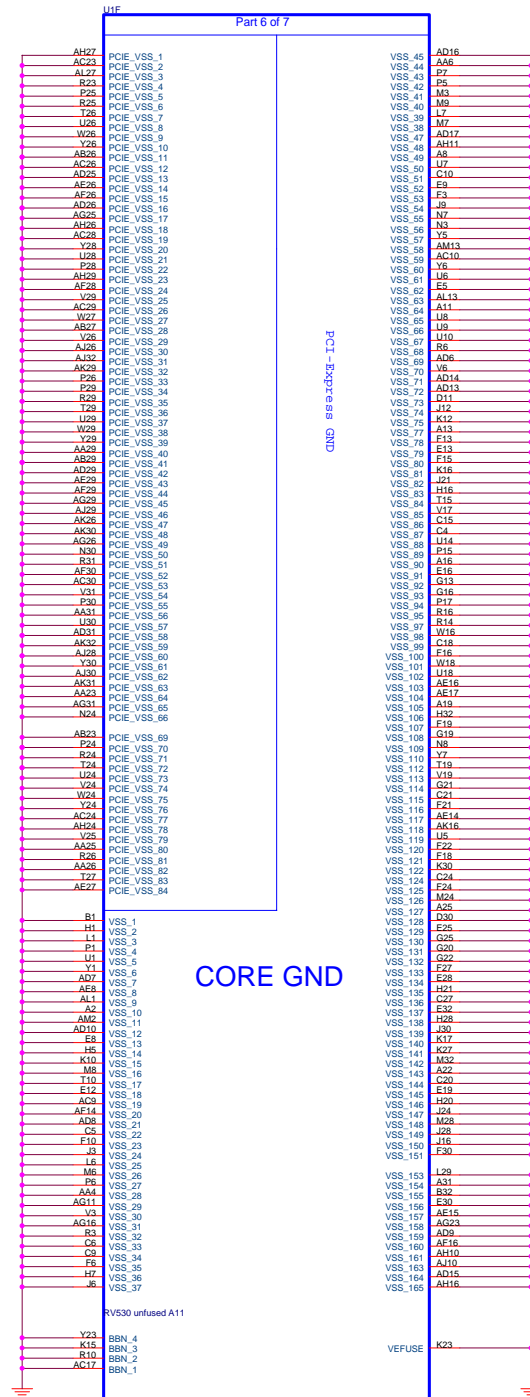
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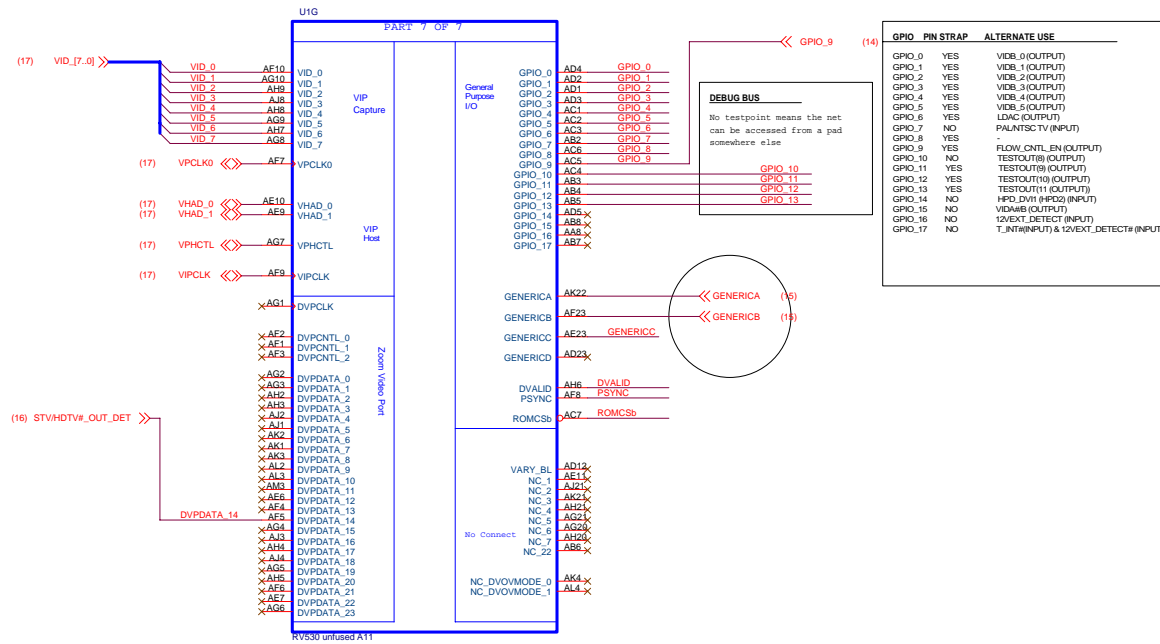




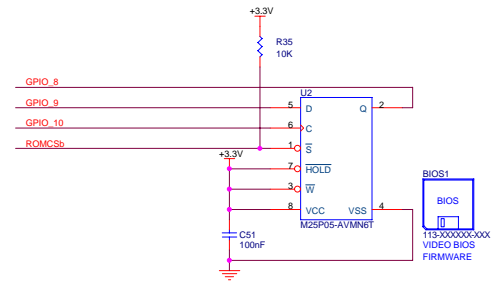
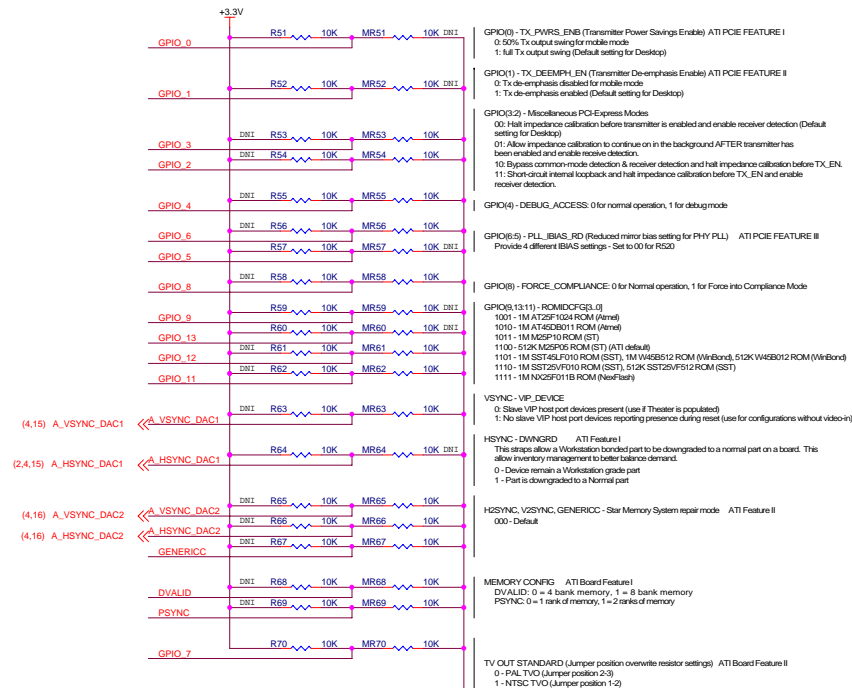






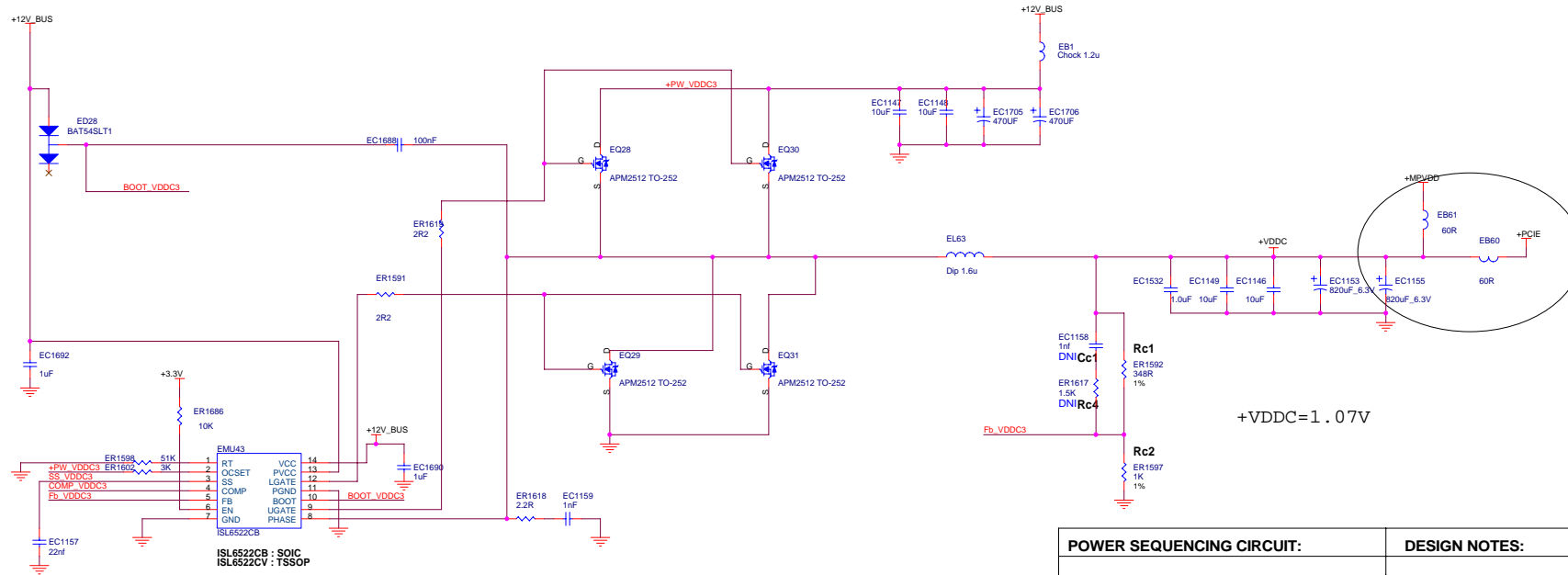


## PIN BASED STRAPS



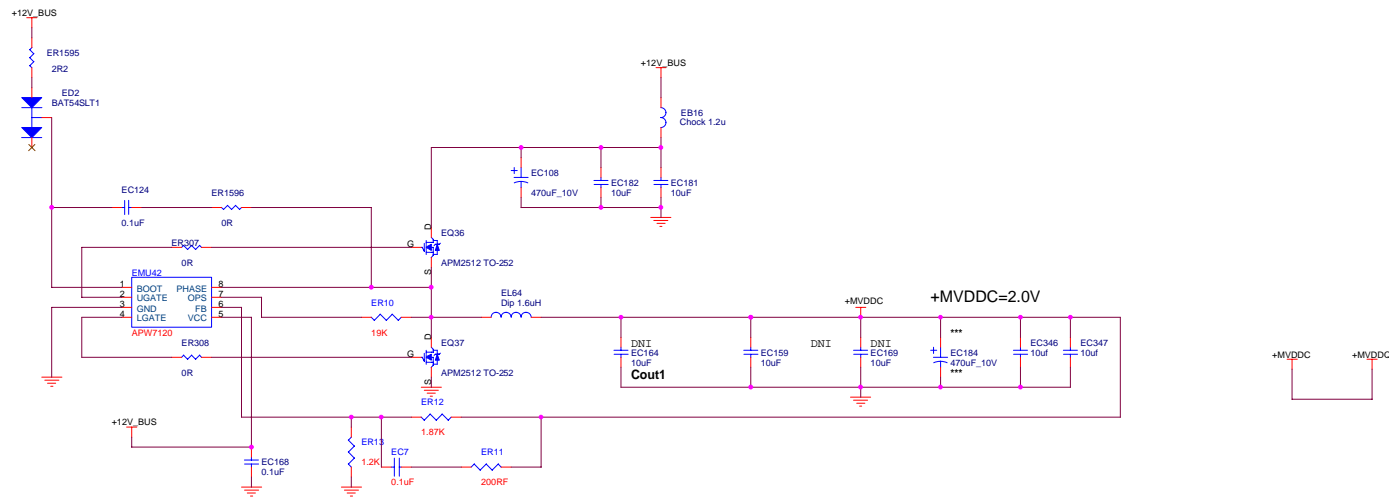


# CORE REGULATOR VDDC



Lower MOSFET should be surrounded by a lot of copper for heat dissipation

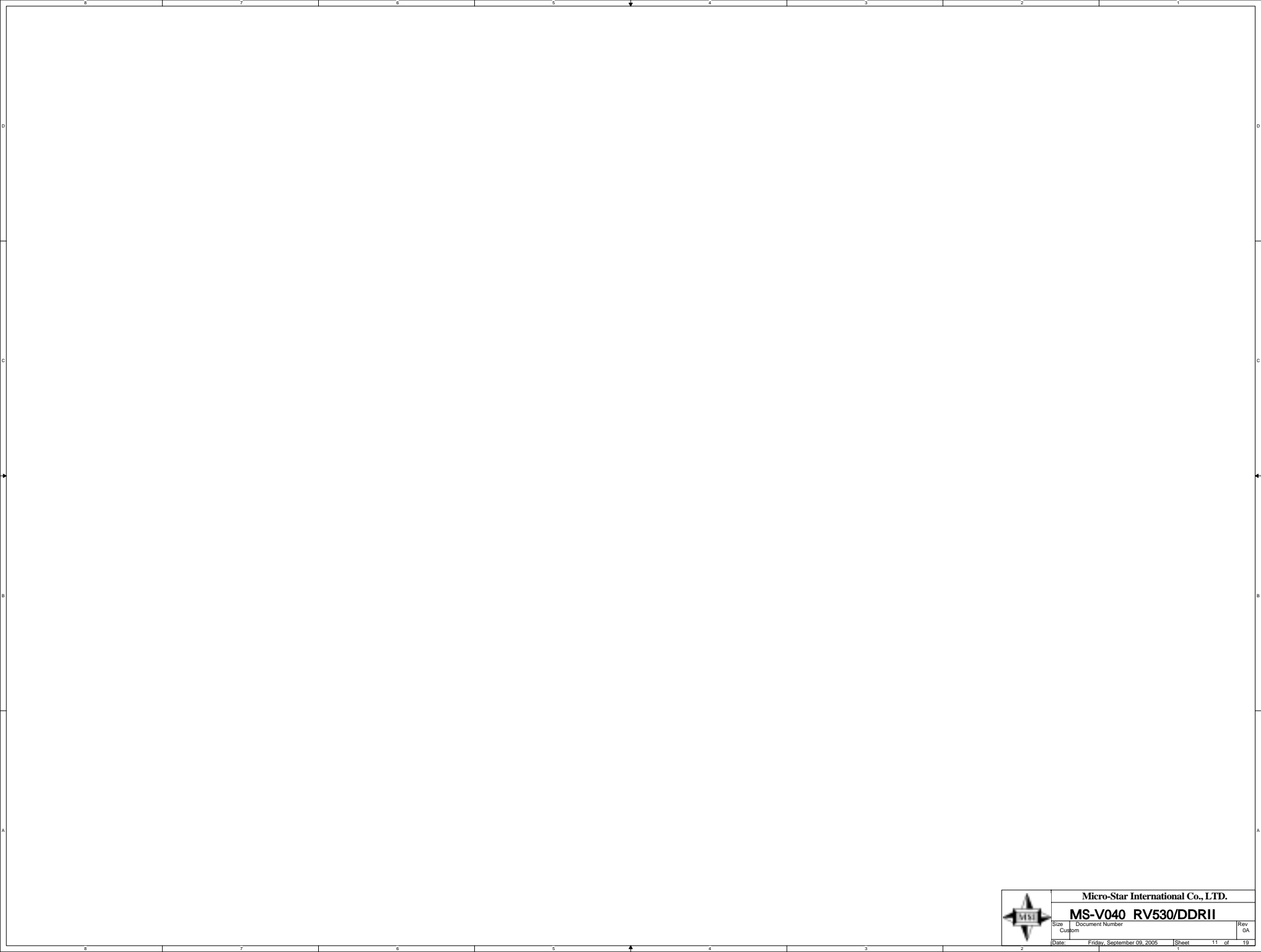
POWER SEQUENCING CIRCUIT:	DESIGN NOTES:
	<p><b>Compensation Circuit</b></p>
<p><b>FOR ALTERNATE #1</b></p> <p>Remove R374, R375, R371, C168 and U32</p> <p>Install R370, R112, R954, R305-R308, C168, C159 and MU32</p>	<p><b>FOR ALTERNATE #2</b></p> <p>Change C157 for 10 uF and C121 for 1 uF</p> <p>Replace C764 by 0 Ohm resistor</p> <p>Remove R314 with a bead</p> <p>Remove R954, R370, R305-R308, C159, R112, C160 and MU32</p> <p>Install R374, R375, R371, C168 and U32</p> <p><b>Compensation circuit</b></p> <p>Rc1 = 10K, Rc2 = 8.06K</p> <p>R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF</p>



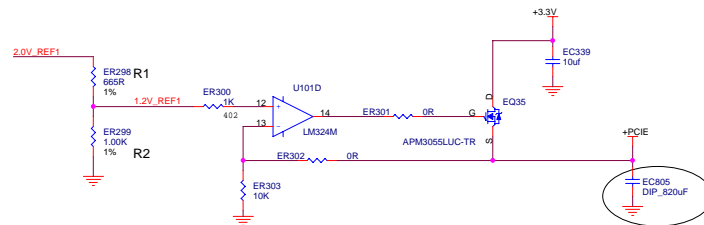
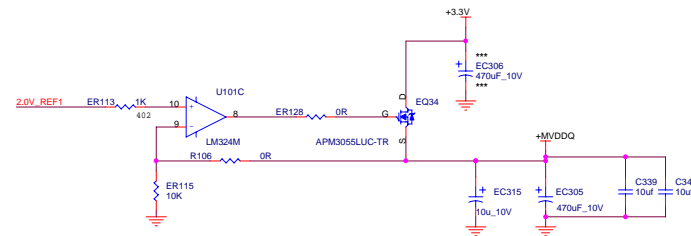
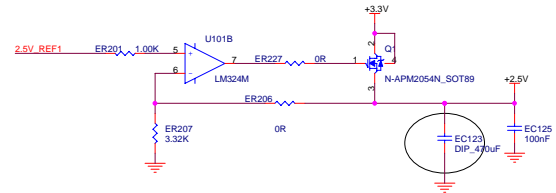
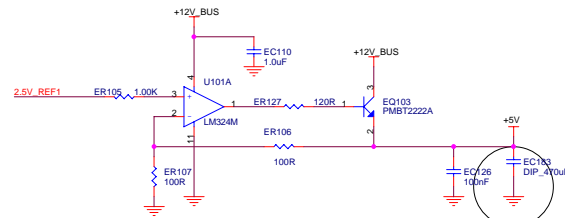
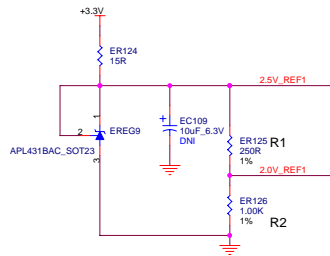
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Replace with 5050004800  
120R, 300MA EIA(0402)

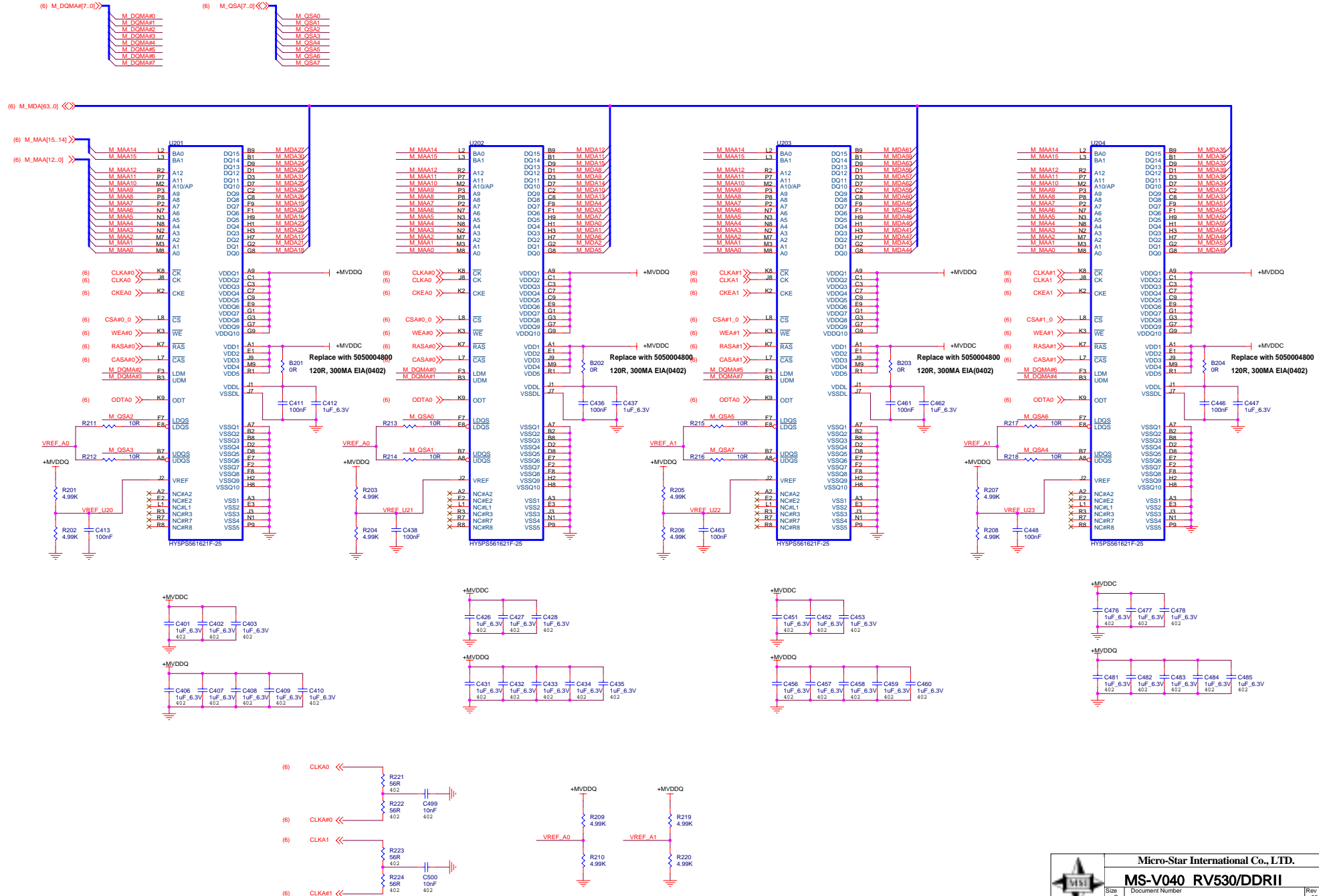


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# CHANNEL A: RANK 0 128MB DDR2

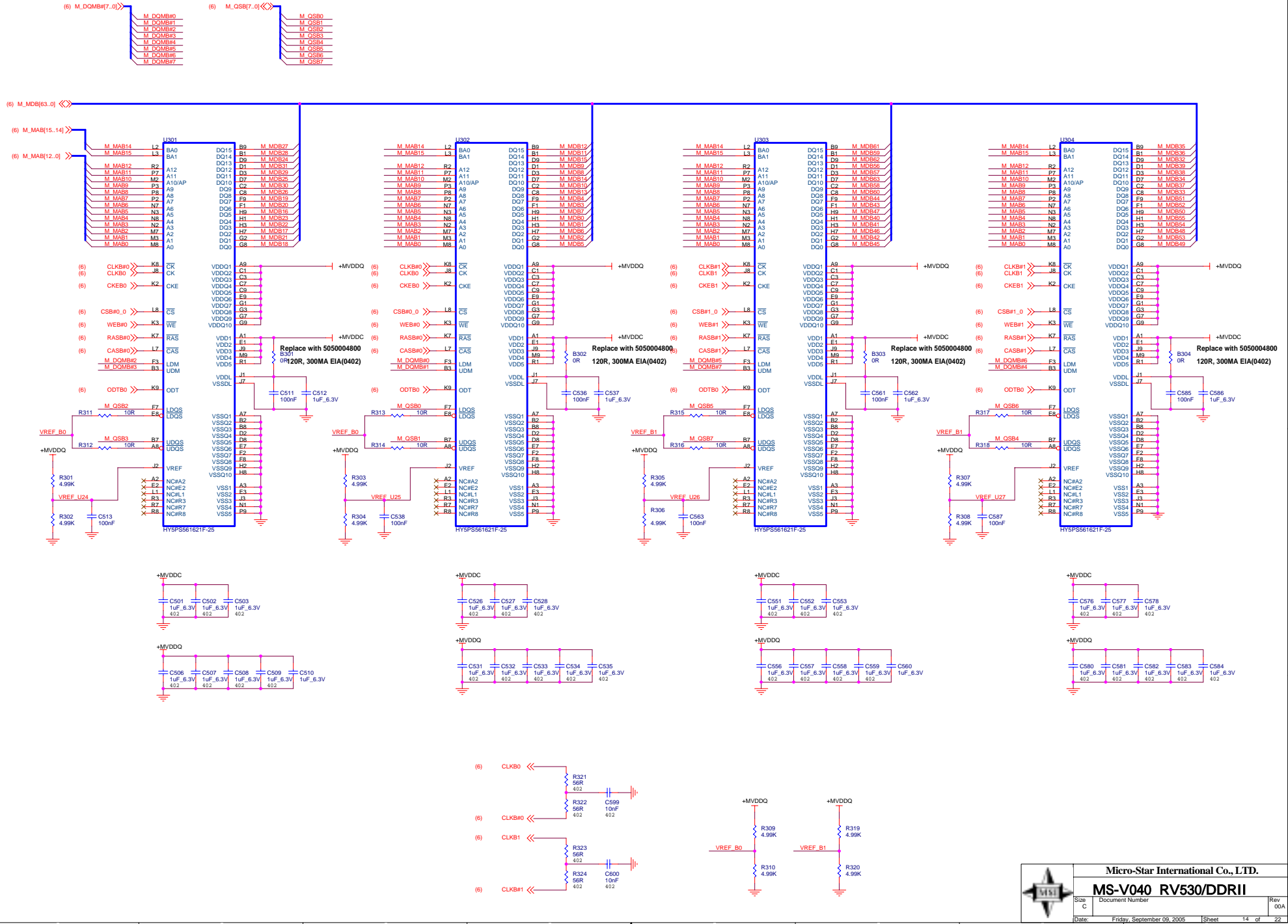


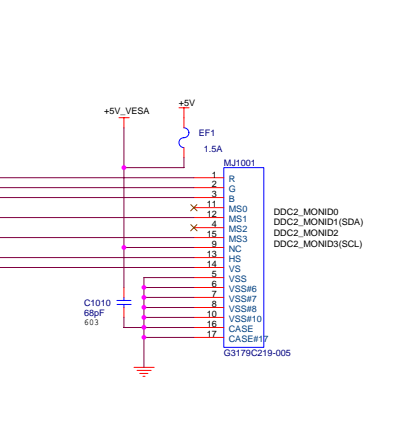
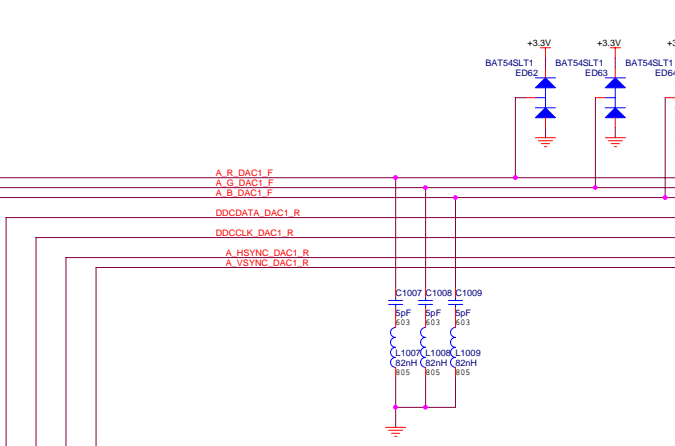
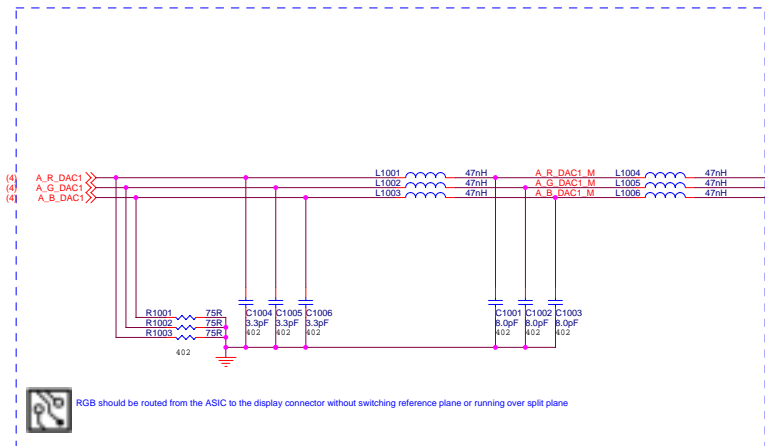
Micro-Star International Co., LTD.

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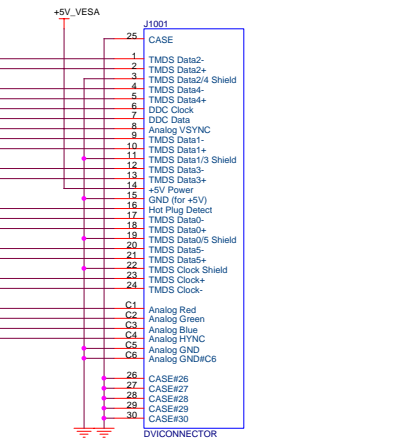
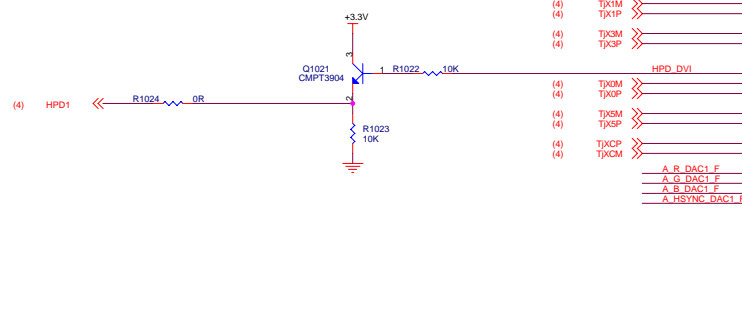
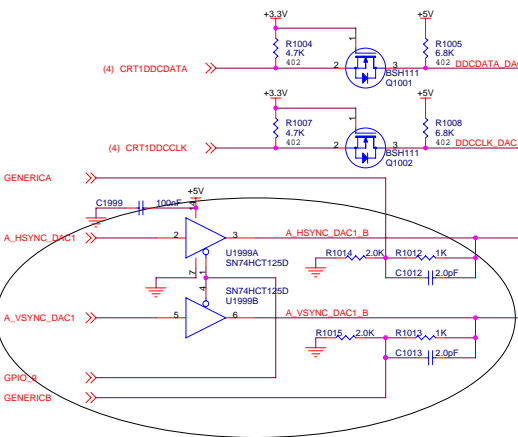
**CHANNEL B: RANK 0 128MB DDR2**

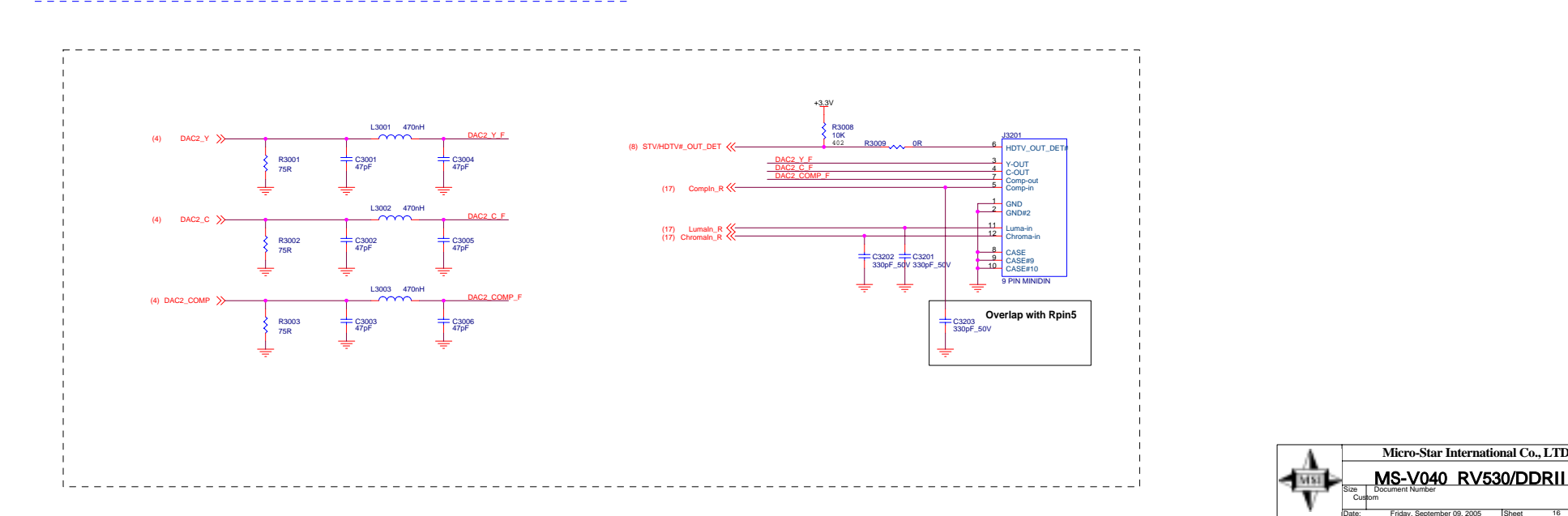
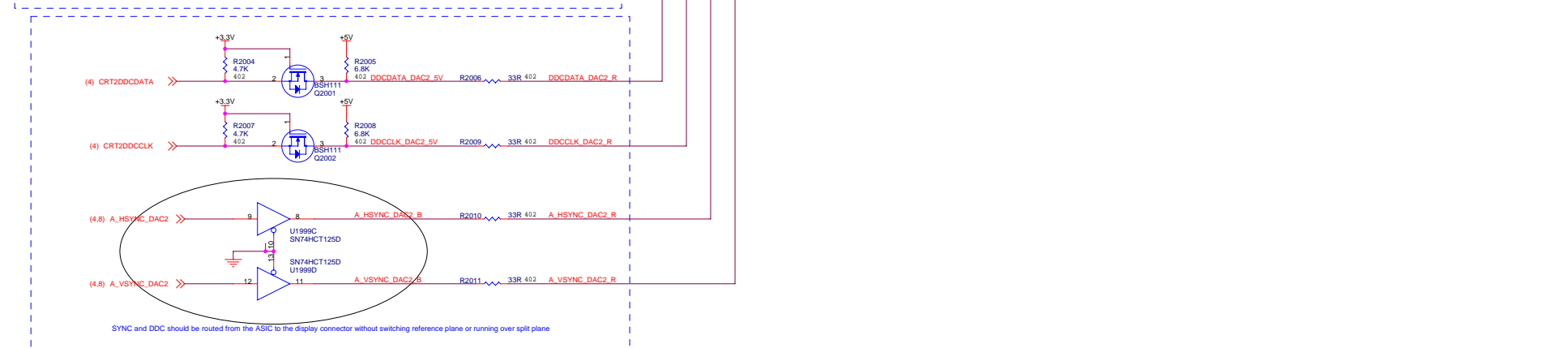
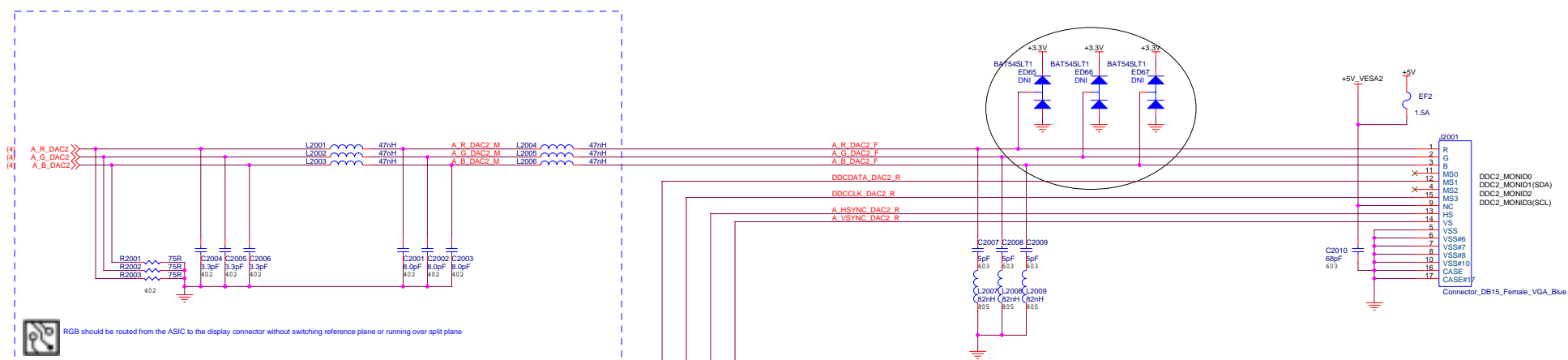




DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional SDA
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional SDA
15	Monitor ID bit 3	Open	Open	Open	Optional SDA
9	N/C	+5V	+5V	+5V	Optional
Hardware Support	No	Yes	Yes	No	Yes

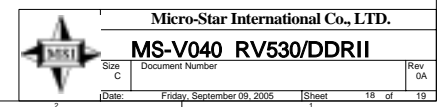
Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997











DVI/VGA SCREWS

- SCREW1  
SCREW  
JACKSCREW  
ASSY  
7020000800

SCREW2  
SCREW  
JACKSCREW  
ASSY  
7020000800

SCREW3  
SCREW  
JACKSCREW  
ASSY  
7020000800

SCREW4  
SCREW  
JACKSCREW  
ASSY  
7020000800

