

## MS-V041 VER 10

NV43-PCIE NV43 256MB/128bit, BGA 16MX16 DDR2,VGA,DVI-I,TV-OUT(HT-10)

**P295-A00 DESIGN NV43 300/267MHZ 128MB/256MB/512MB DDR2 84-FBGA**

PAGE SUMMARY:

## DDR2 84-FBGA Clock setting 350MHZ

Page1: P295 Overview

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Page19: Other Powers - A3V3, DDC\_5, TMDSPLL, TMD SIO, FBVTT and 5V-3V3 POWER SEQUENCING

REV  
HISTORY

## A00

-08/04/2005:

1. Page 18: change power solution to RT9218 for NVVDD & FBVDDQ

## 10S

-08/04/2005:

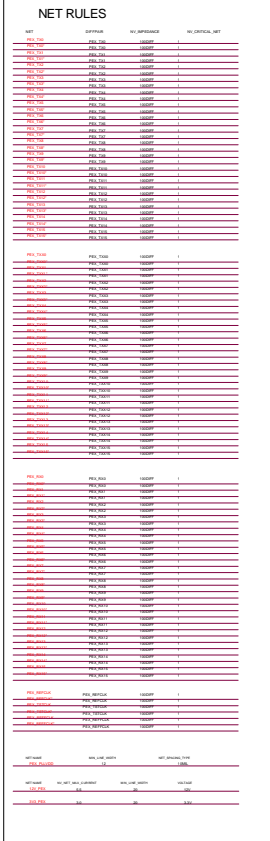
1. Page 18: Move C913~C916 out form C910, C911 & Move C930, C931 out form C929

2. Page 19: Add C940 near C36

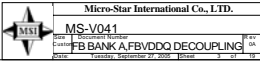
3. Page 19: Remove C16, C35, C55

[illegible]

	<b>Micro-Star International Co., LTD.</b>			
	<b>MS-V041</b>			
	Site Customer	Document Number <b>P295 Overview</b>		Rev QA
	Date <b>Monday, September 26, 2005</b>	Sheet <b>1</b>		of <b>10</b>

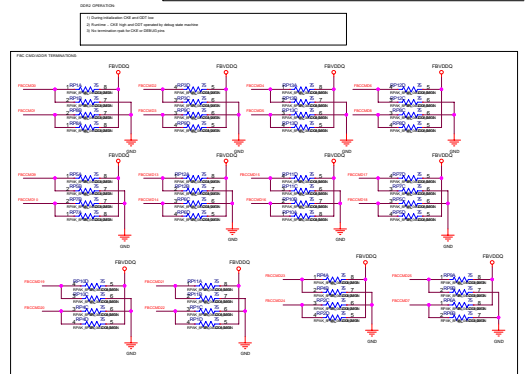
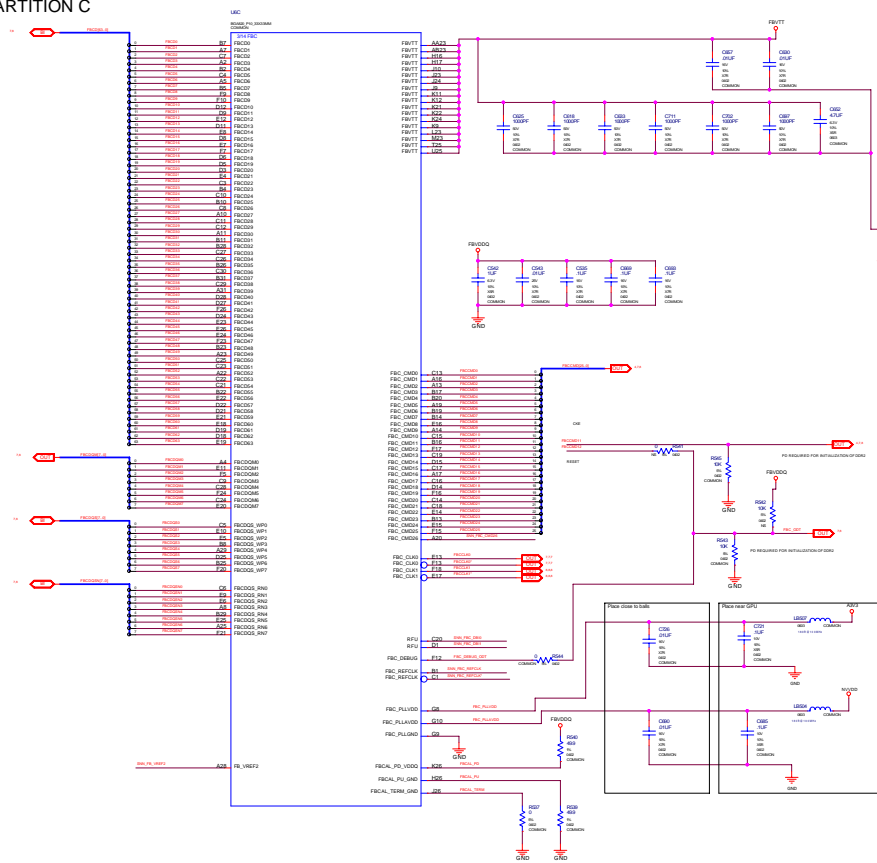


## FB PARTITION A

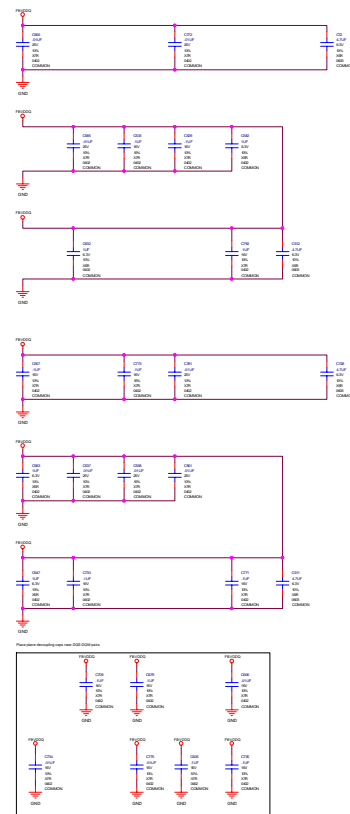
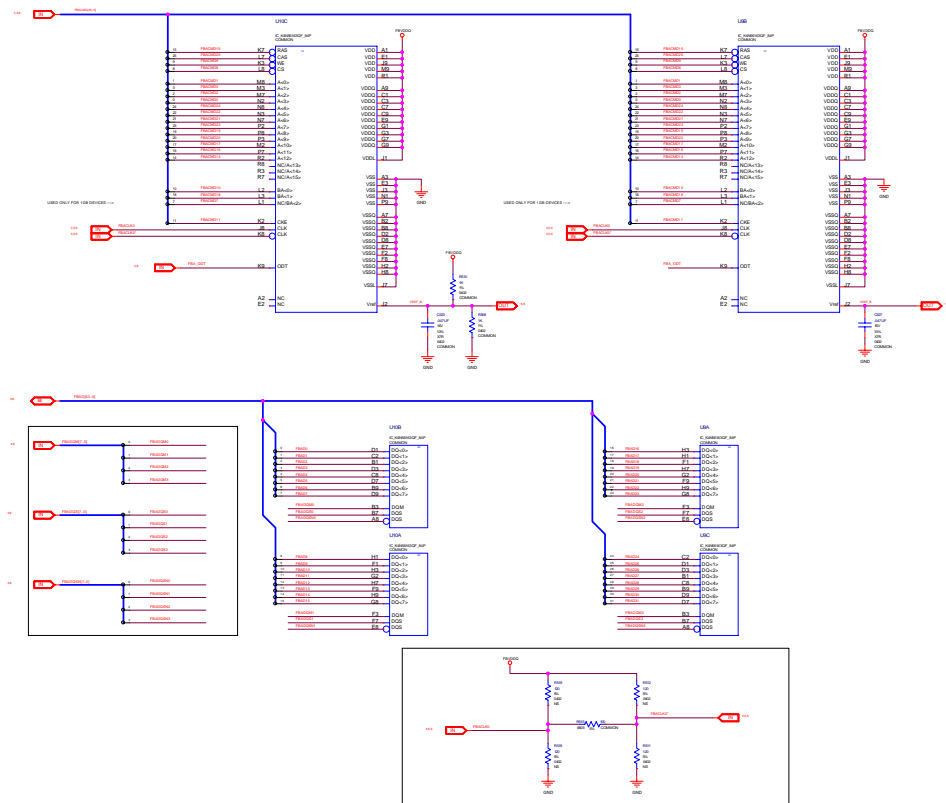


# 04 FB BANK C, FBVTT TERMINATIONS

## FB PARTITION C

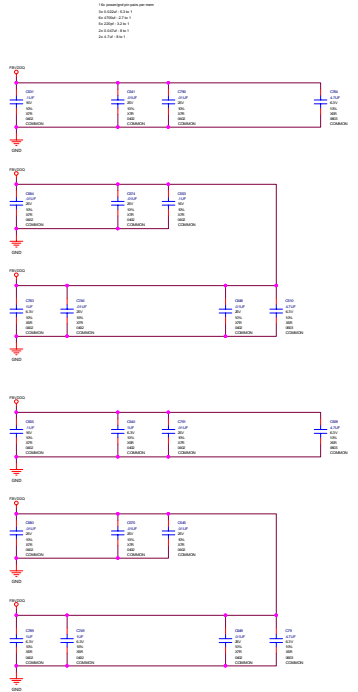
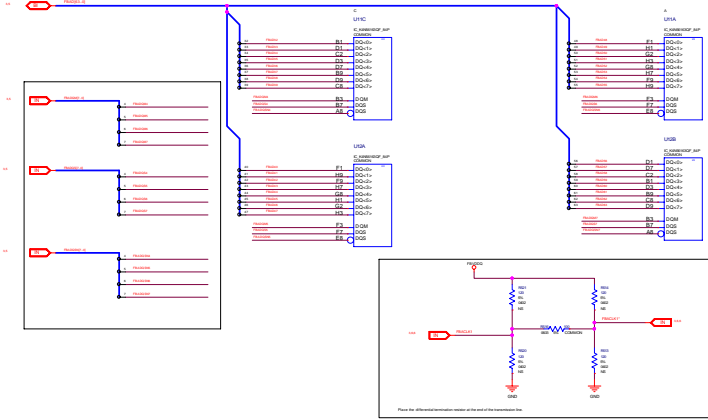
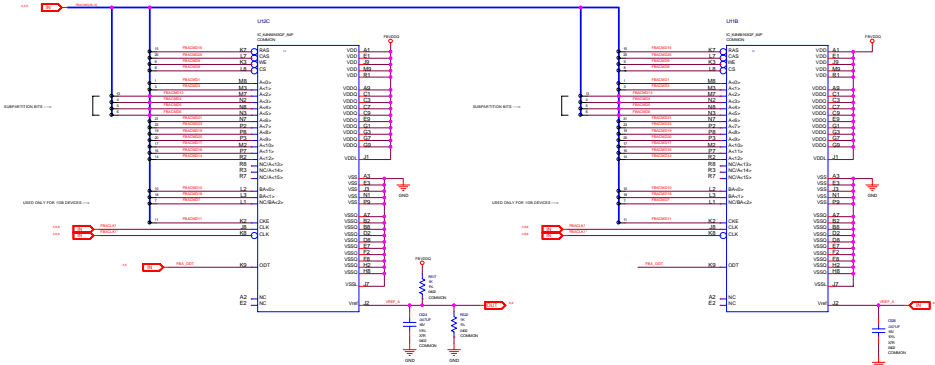


PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



06 MEMORY PARTITION A 32..63

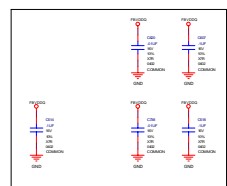
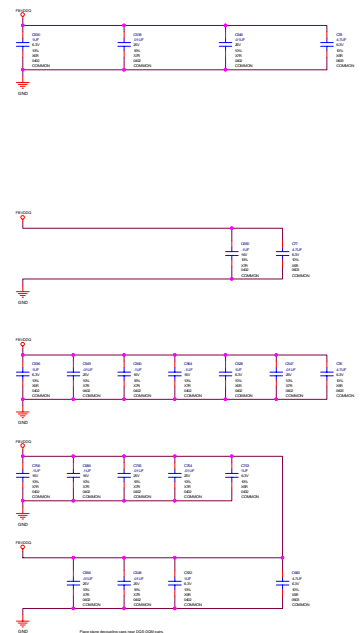
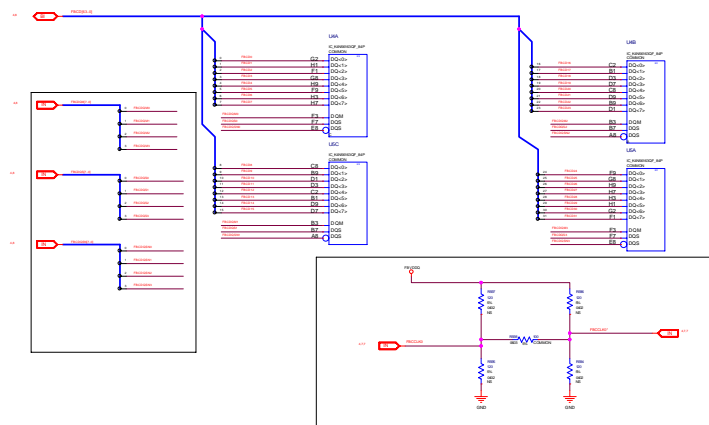
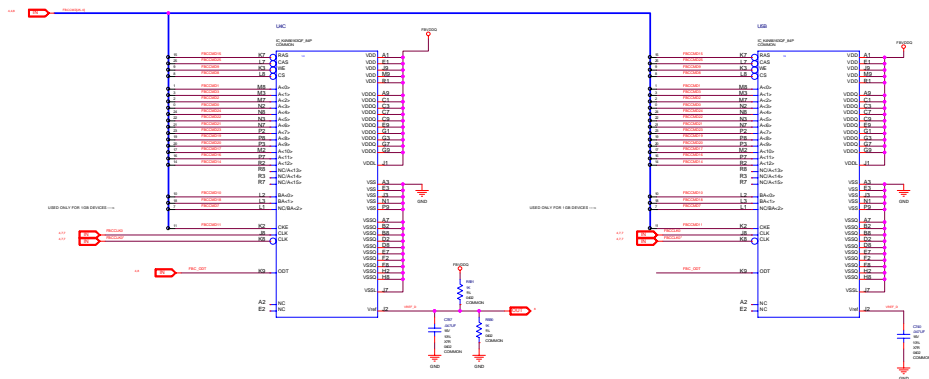
FBA MEMORY 1st bank 32..63  
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



## 07 MEMORY PARTITION C 0..31

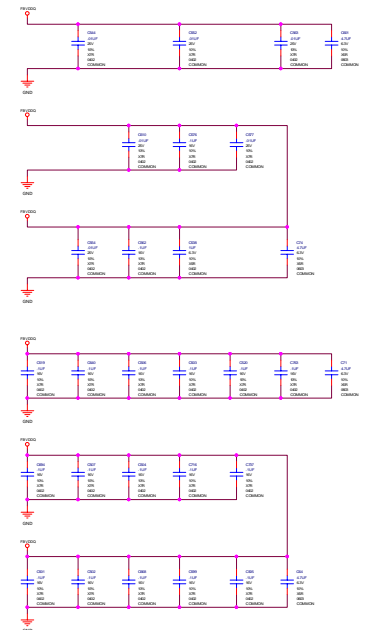
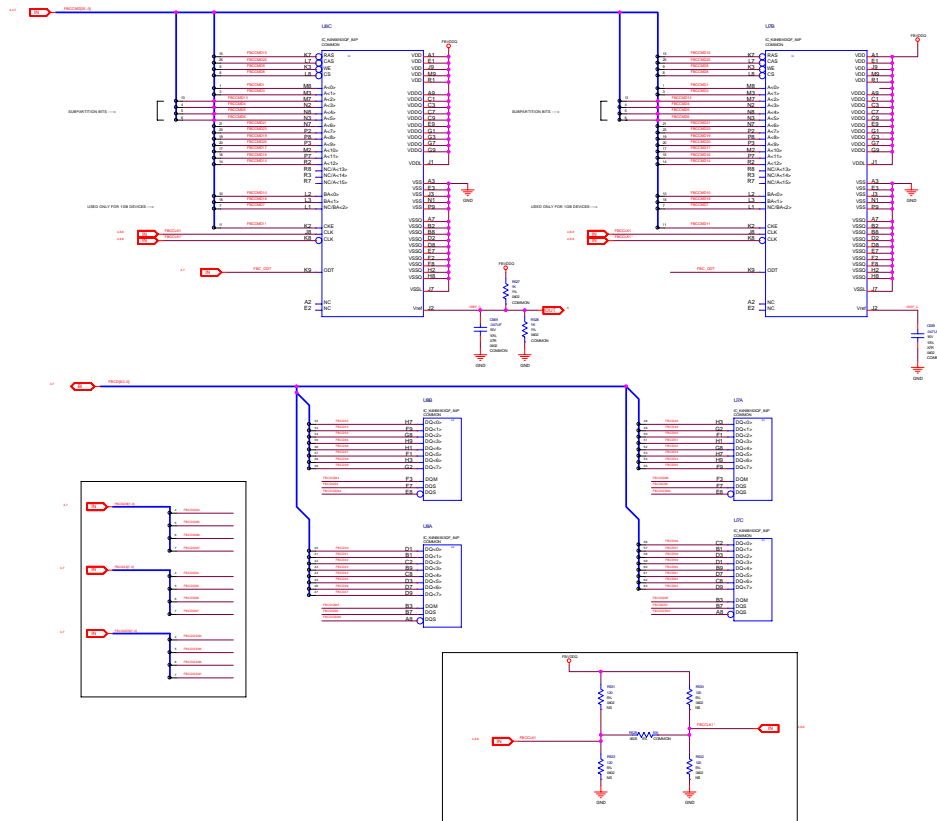
## FBC MEMORY 2nd bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



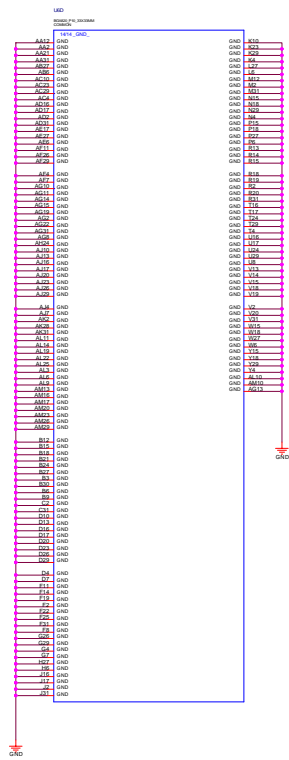
## FBC MEMORY 2nd bank 32..63

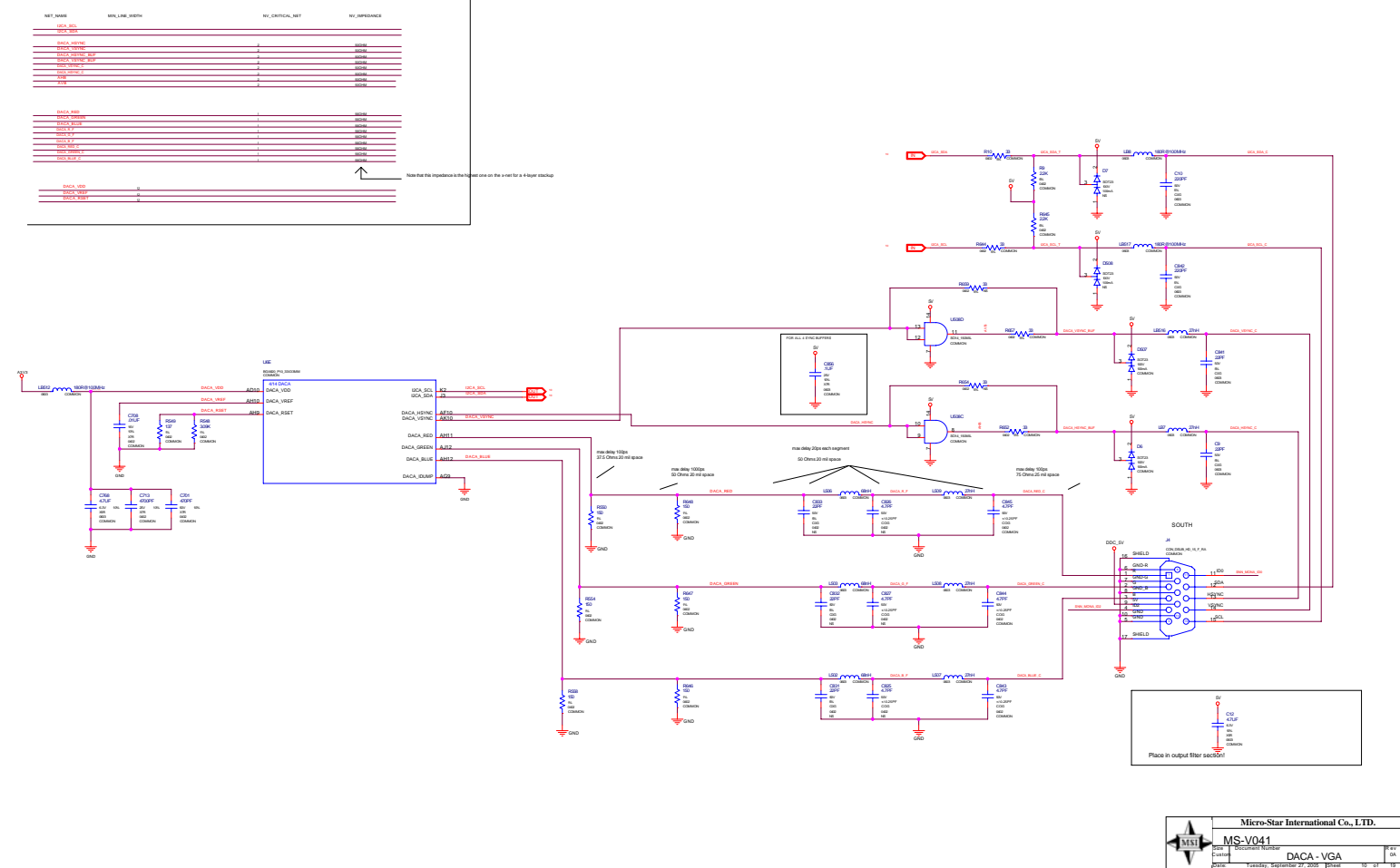
NAME	MIN_LINE_WIDTH
USER_C	32
USER_D	32



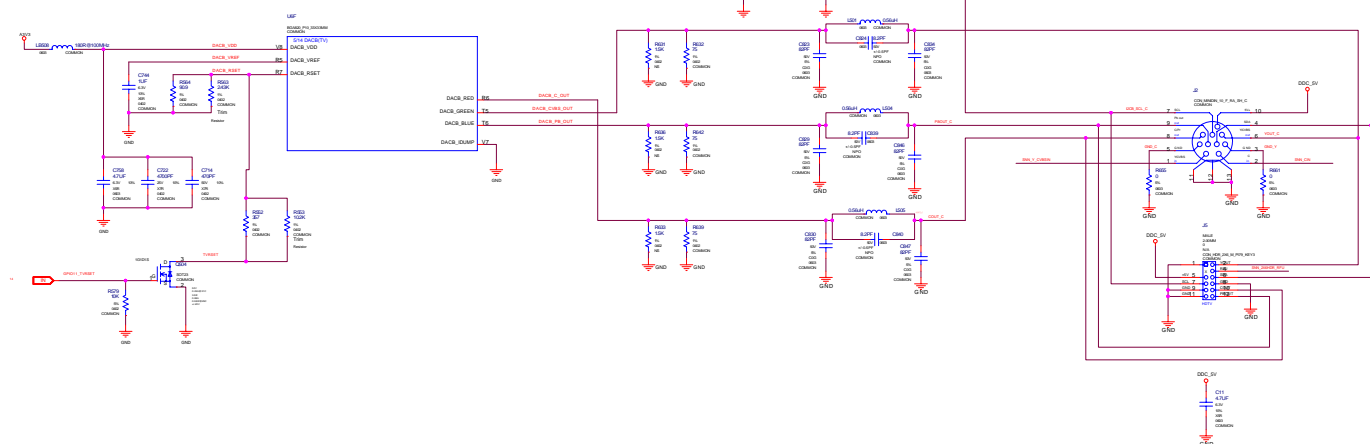
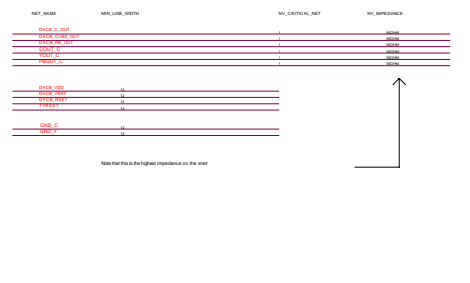


## 09 GPU GND



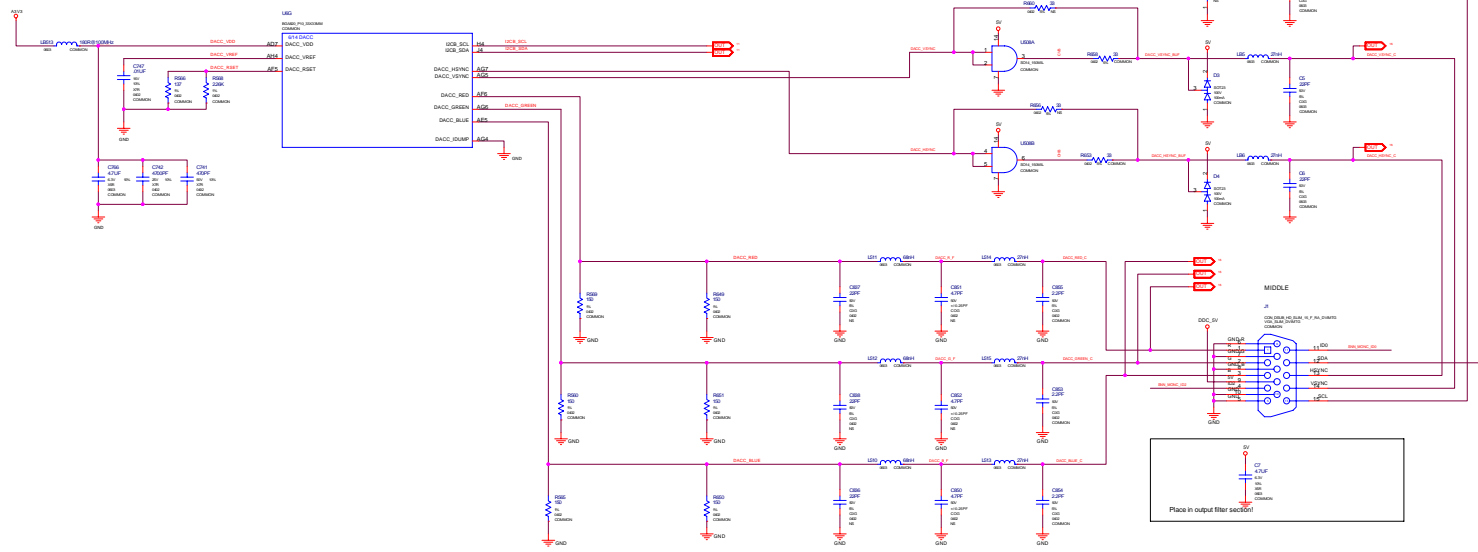


## 11 DACB - TVOUT, VIDEO IN



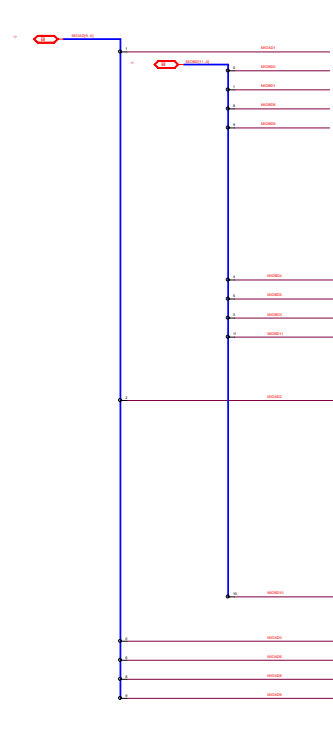
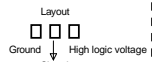
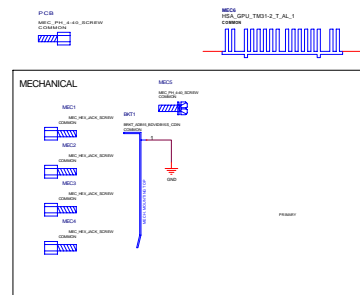
# 12 DACC - VGA

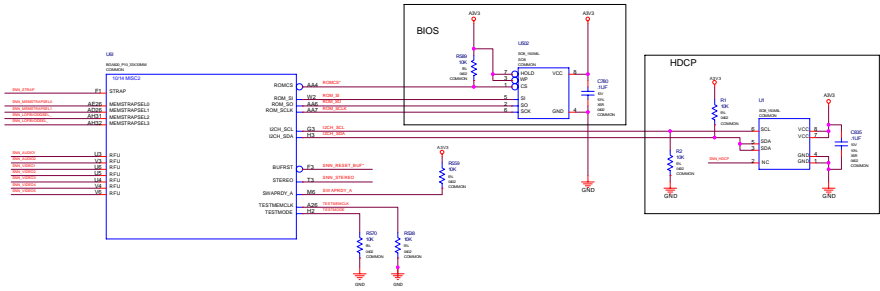
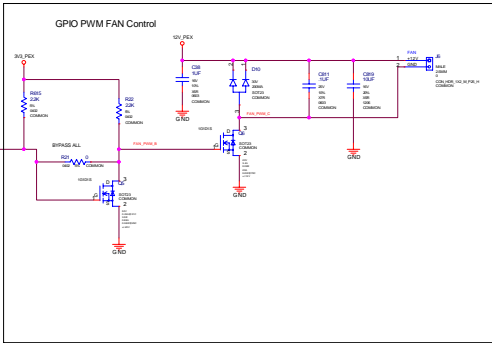
NET_NAME	SUBLINE_SHORT	NET_SYMBOLIC_NAME	NET_CRITICAL_NAME	NET_REFERENCE
DACC_VDD				
DACC_VSS				
DACC_VDDNC				
DACC_VSSNC				
DACC_VDDREF				
DACC_VSSREF				
DACC_VDD1				
DACC_VSS1				
DACC_VDD2				
DACC_VSS2				
DACC_VDD3				
DACC_VSS3				
DACC_VDD4				
DACC_VSS4				
DACC_VDD5				
DACC_VSS5				
DACC_VDD6				
DACC_VSS6				
DACC_VDD7				
DACC_VSS7				
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DACC_VSS8				
DACC_VDD9				
DACC_VSS9				
DACC_VDD10				
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DACC_VDD98				
DACC_VSS98				
DACC_VDD99				
DACC_VSS99				
DACC_VDD100				
DACC_VSS100				



### 13 STRAPS, FANSINK, MECHANICALS

Overlap pads to save space  
and to prevent assembly of  
both resistors.

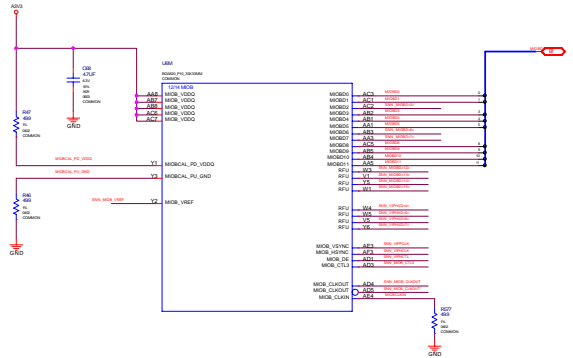
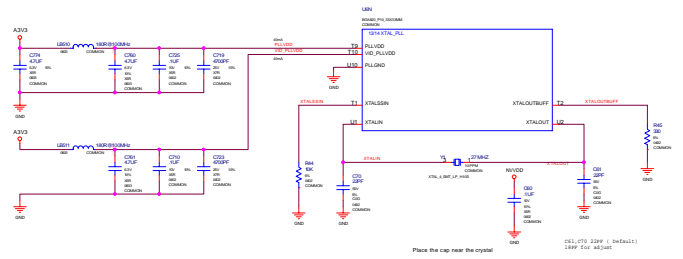
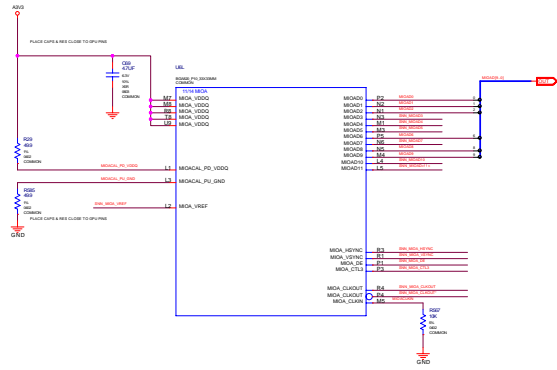
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VDD\_PLL1000

XTALIN

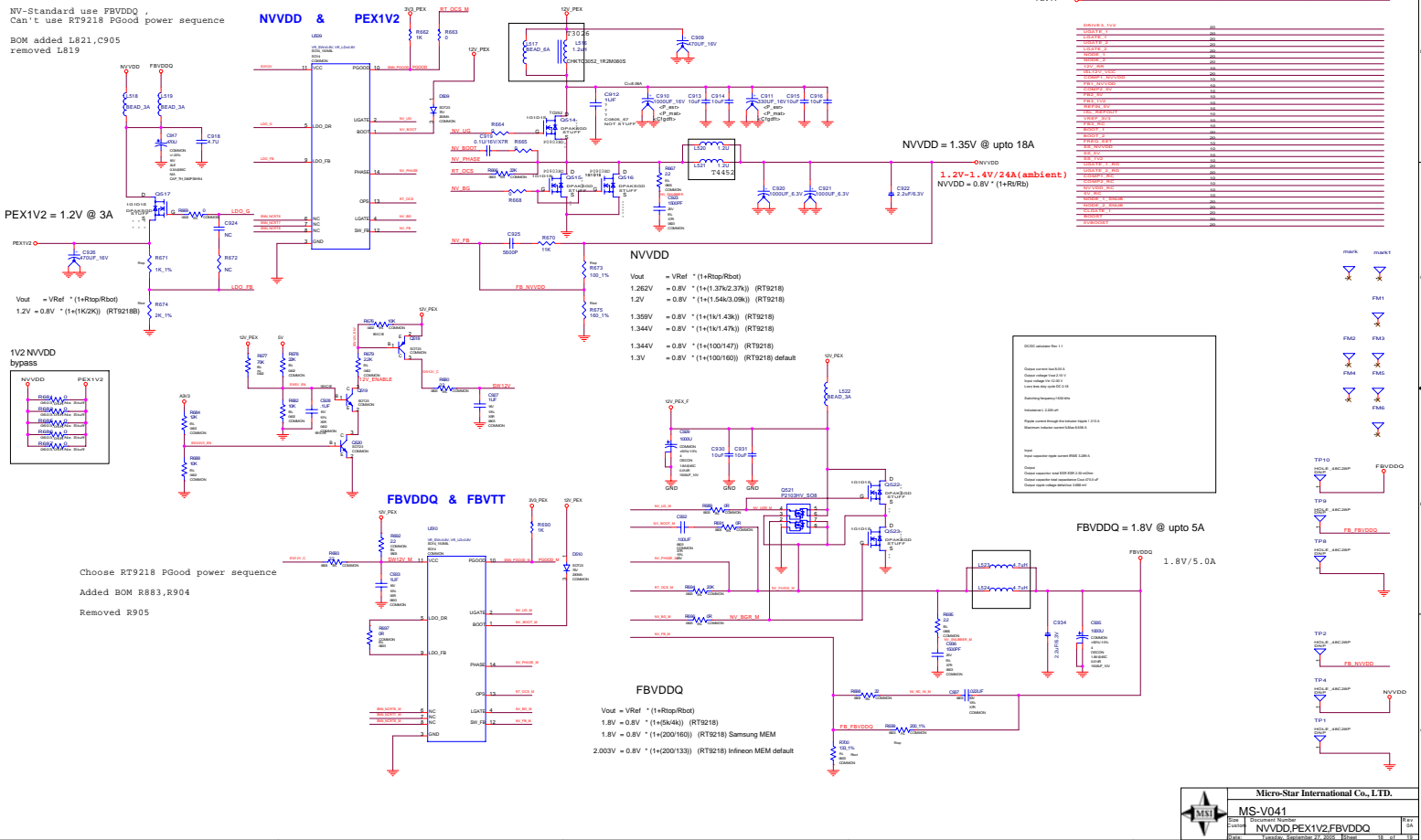
XTALOUT

PLL1000

18 Power Supply (RT9218)  
NVVDD, PEX1V2, FBVDDQ

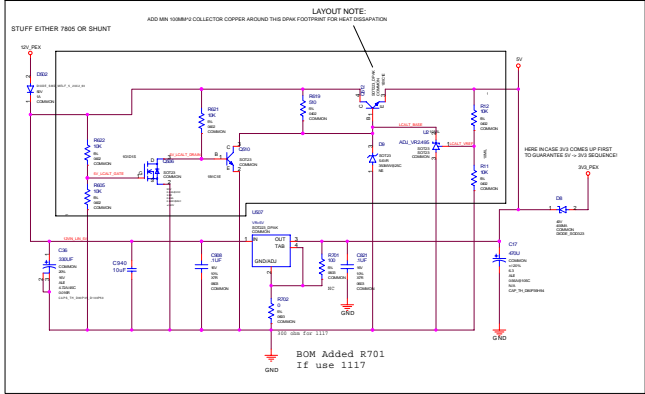
```
NV-Standard use FBVDDQ ,
Can't use RT9218 PGood power sequence

BOM added L821,C905
removed L819
```

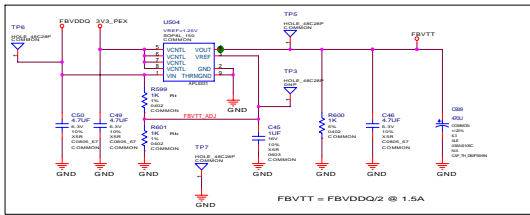


19 Others Power Supply (Linears)  
5V,FBVDDQ,A3V3,3V3,TMDS\_PLLVDD,TMDS\_IOVDD,FBVTT

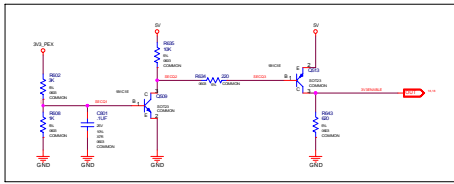
5V LOW COST REGULATOR



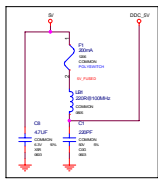
FBVTT TERMINATION



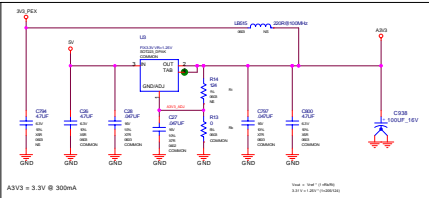
Power Sequencing



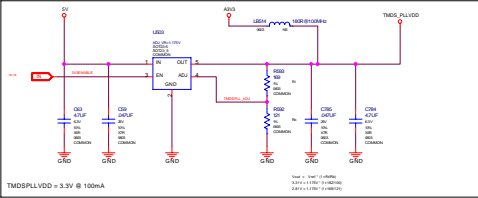
DDC 5V



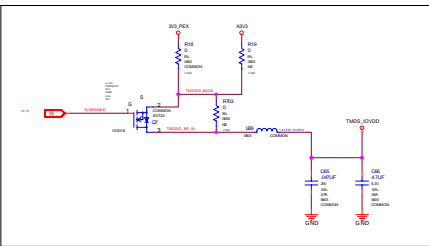
A3V3 Power Supply



TMDS PLL Supply



TMDS IO SUPPLY WITH BACKDRIVE PROTECTION



NET NAME	MIN	MAX	WIDTH	IN	NET	MAX	CURRENT	VOLTAGE
3V3_PEX	0	100	100	0	0	0	0	0
FBVDDQ	0	100	100	0	0	0	0	0
A3V3	0	100	100	0	0	0	0	0
TMDS_PLLVDQ	0	100	100	0	0	0	0	0
TMDS_IOVDD	0	100	100	0	0	0	0	0
5V	0	100	100	0	0	0	0	0
PEK3V3	0	100	100	0	0	0	0	0
DDC_5V	0	100	100	0	0	0	0	0
GND	0	100	100	0	0	0	0	0
FBVTT	0	100	100	0	0	0	0	0
5V	0	100	100	0	0	0	0	0