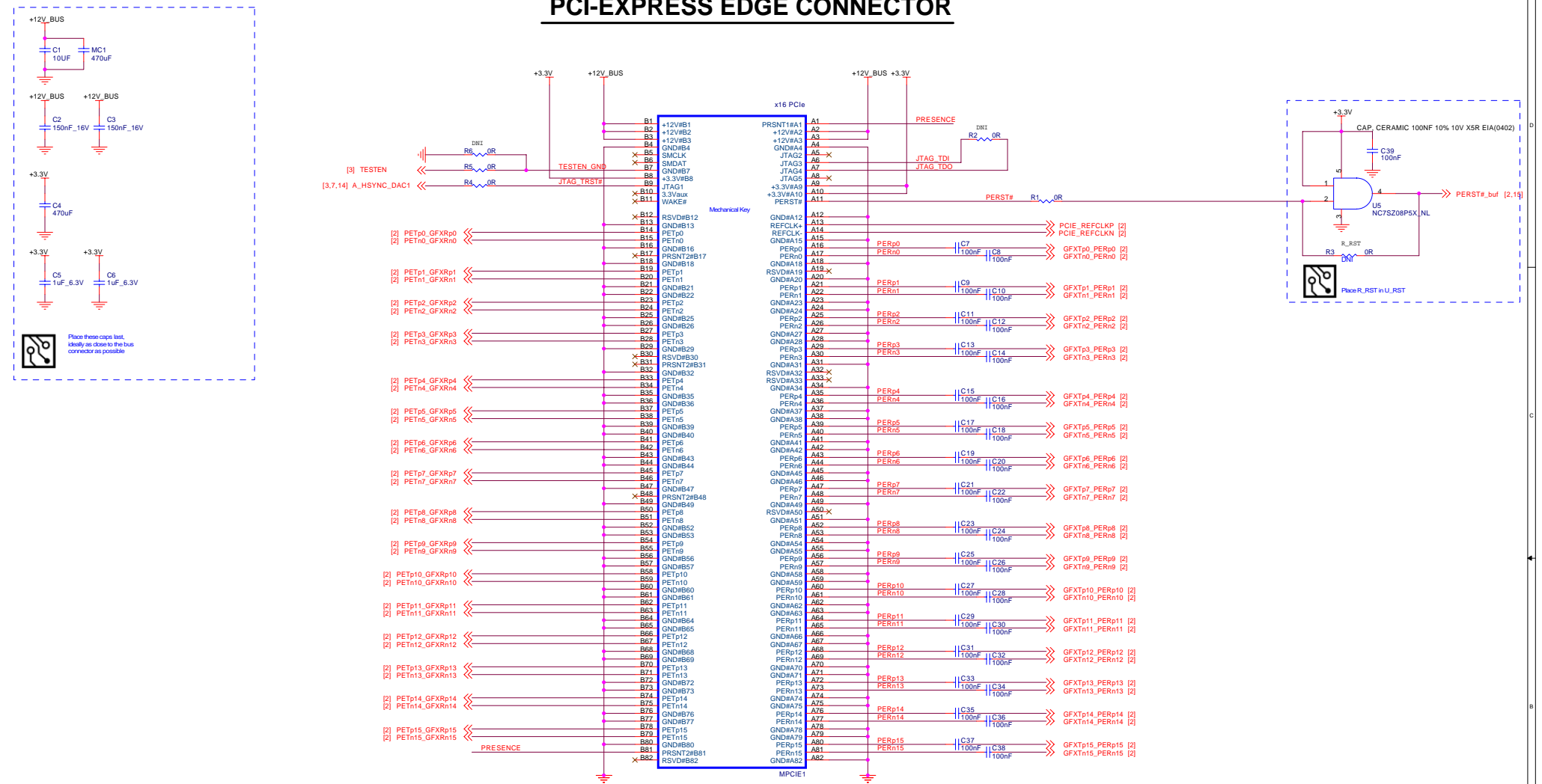


# PCI-EXPRESS EDGE CONNECTOR



Power Sequence Circuit to ensure SMPS\_EN is released after +12V\_BUS and +3.3V\_BUS are both in regulation. Pull-up may or may not be required on SMPS\_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS\_EN will be held low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS\_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)  
Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS\_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)  
Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

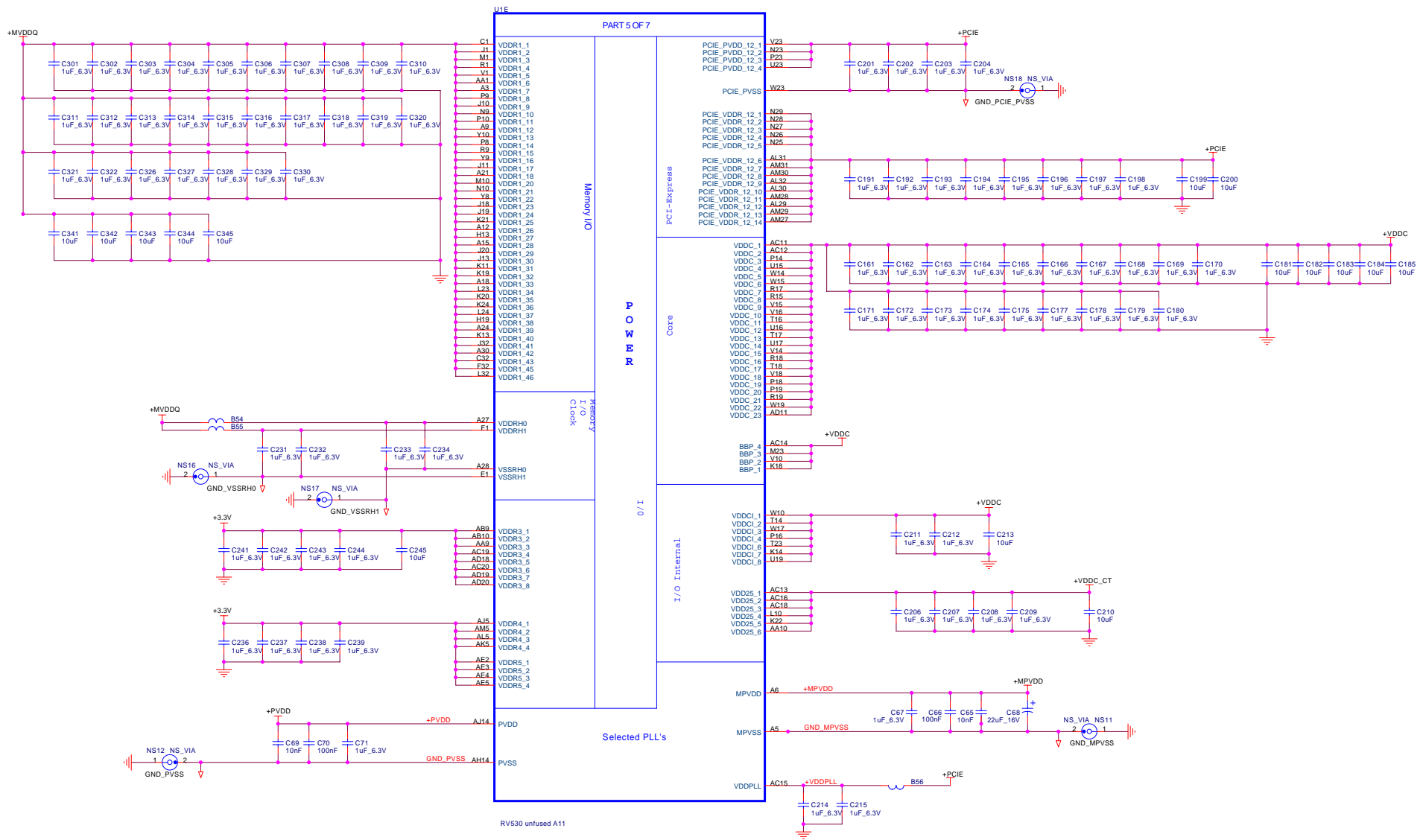


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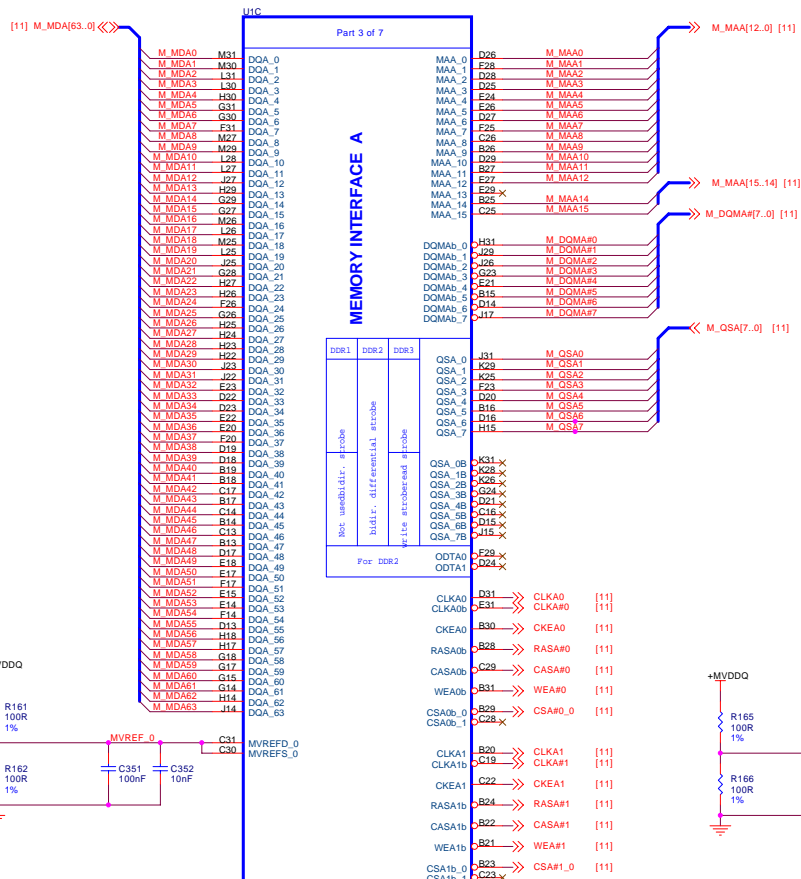


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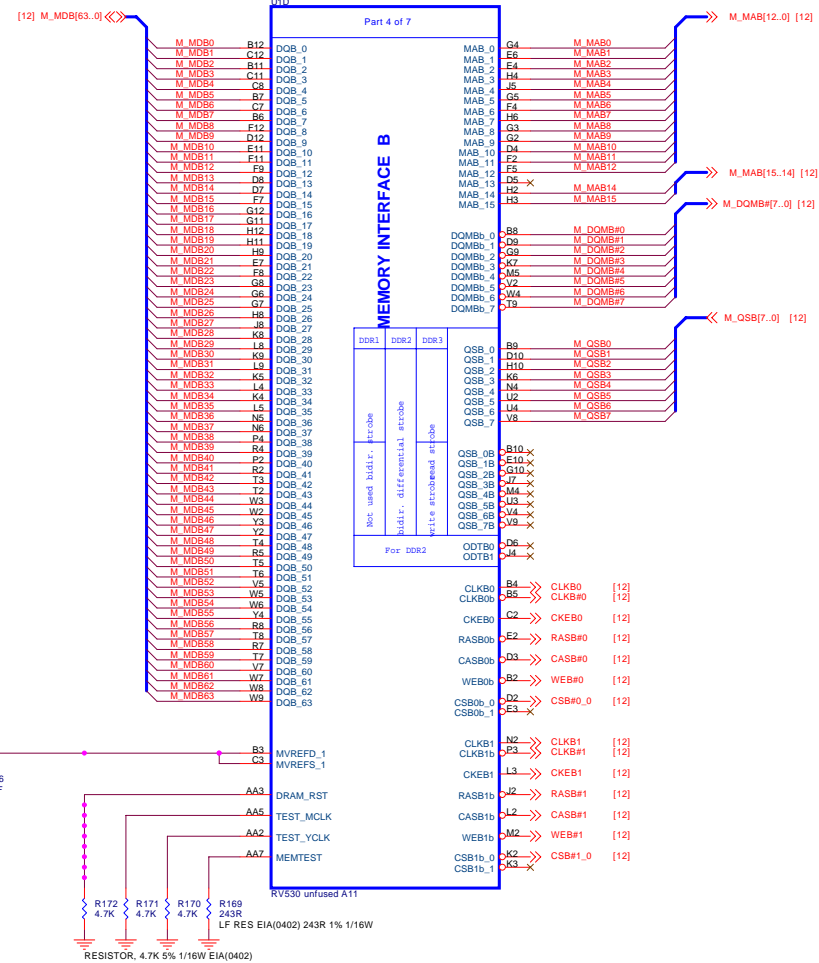
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## RV530 MEMORY CHANNELS A and B

Channel A



Channel B



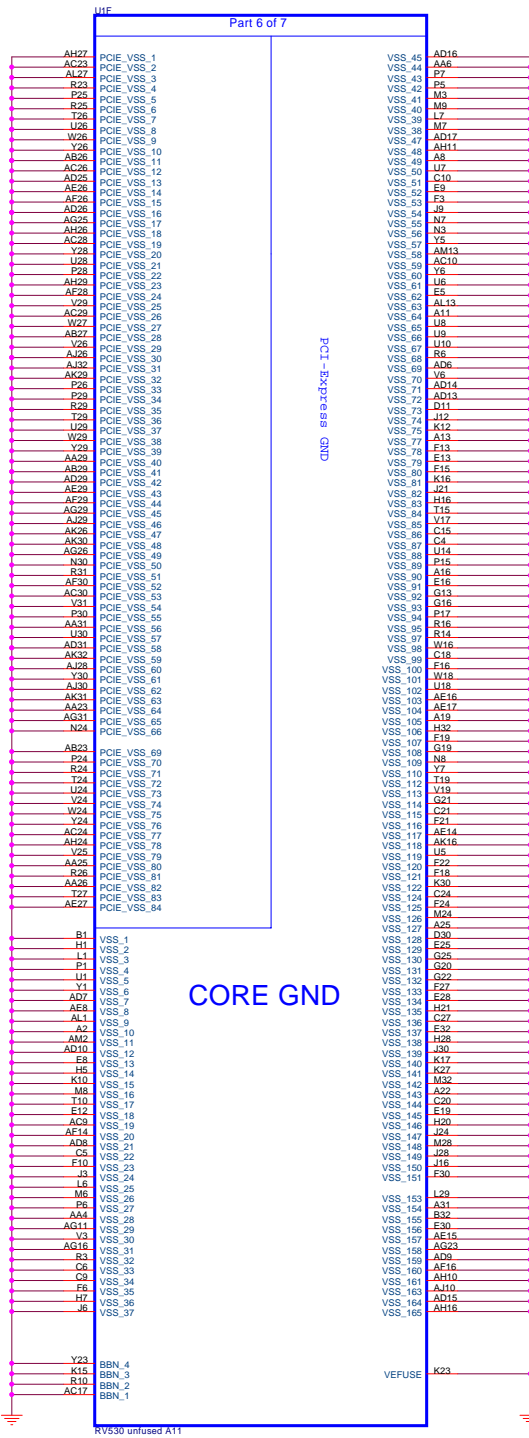
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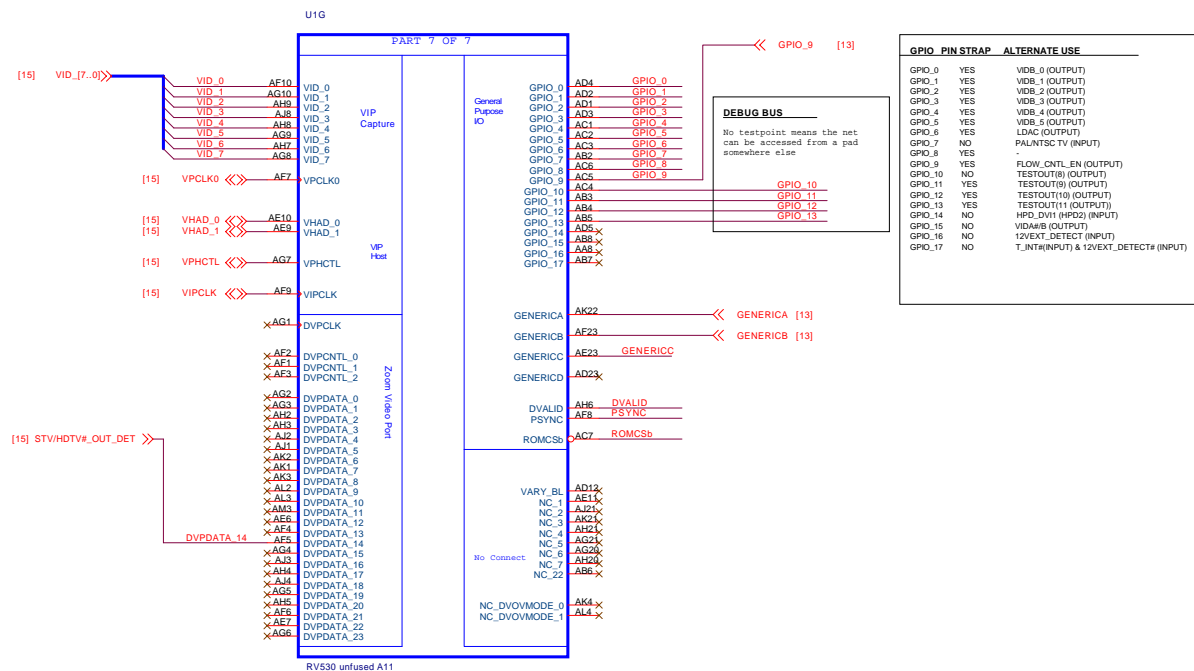
Size C Document Number 105-A67700-00A

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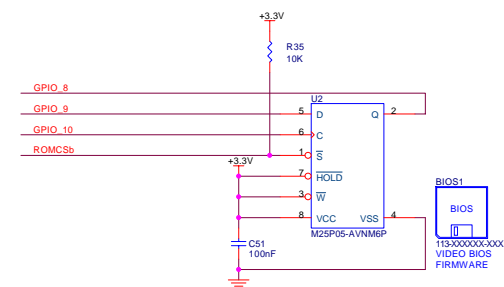
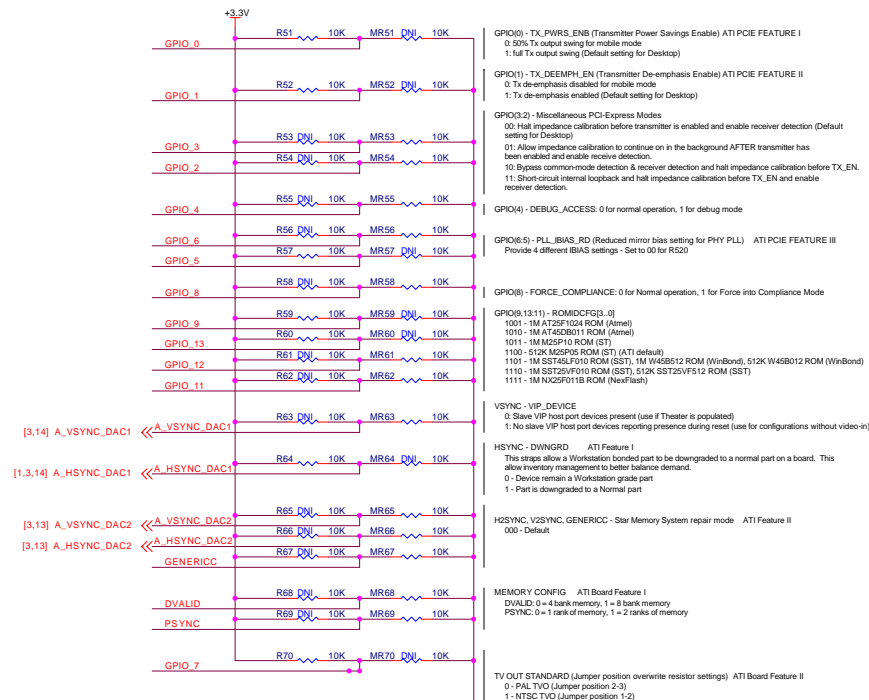


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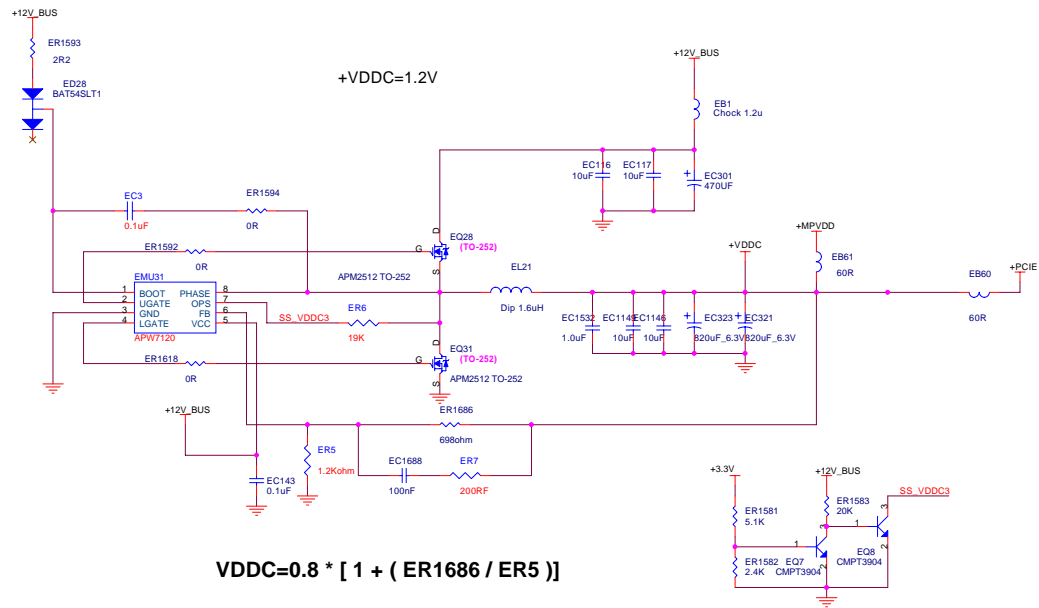
## PIN BASED STRAPS



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## CORE REGULATOR +VDDC



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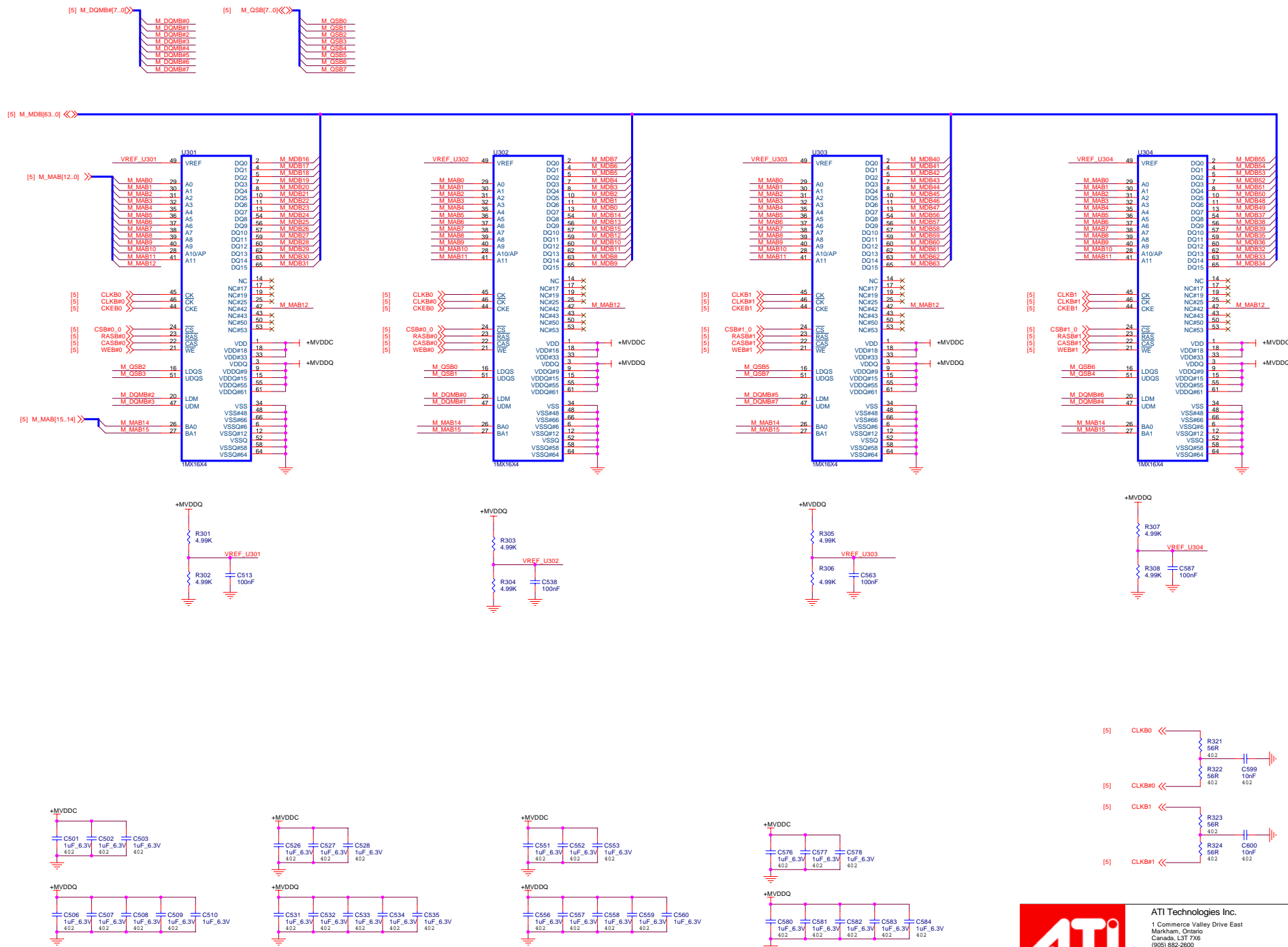






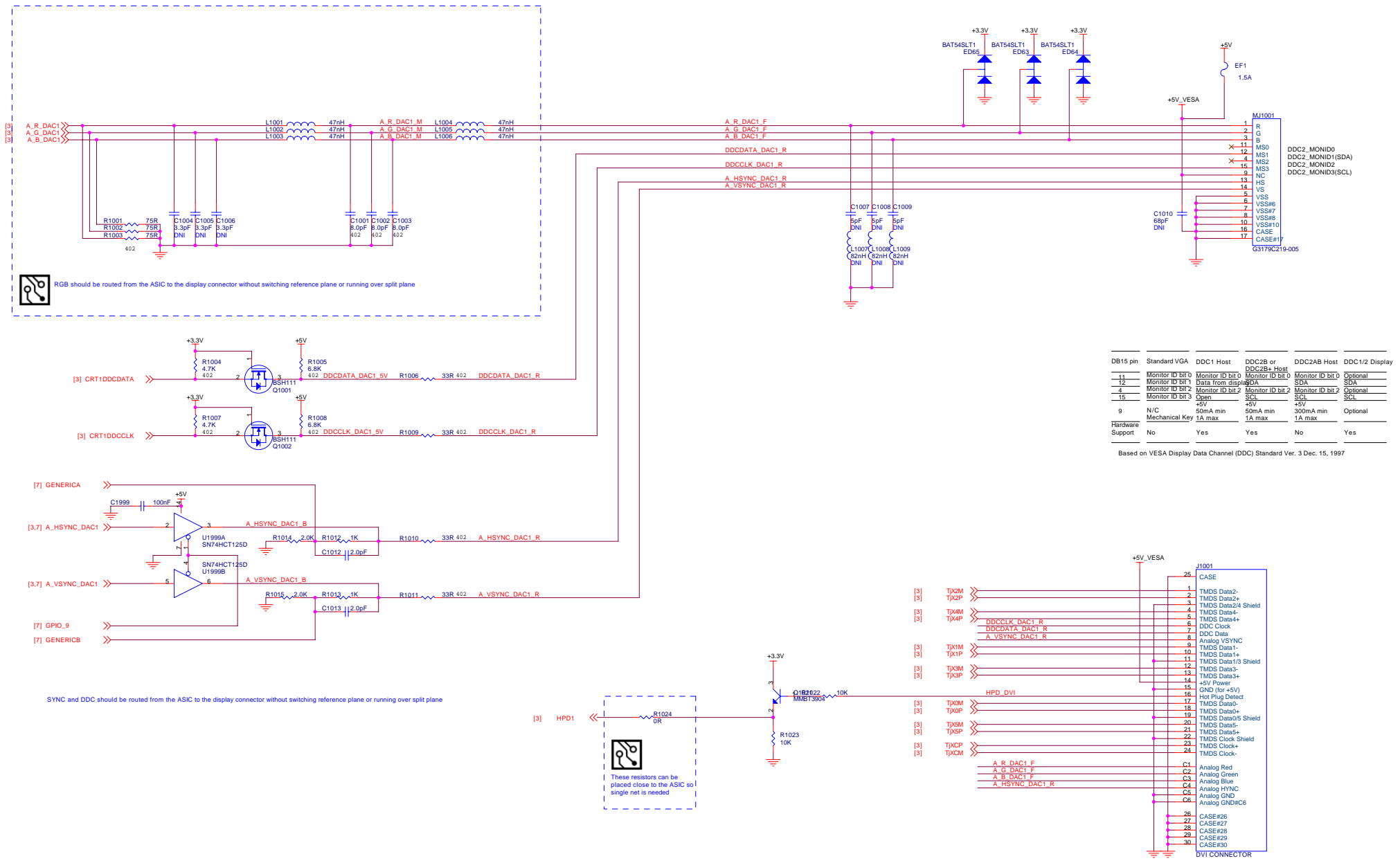


**CHANNEL B: RANK 0 128/256MB DDR1**



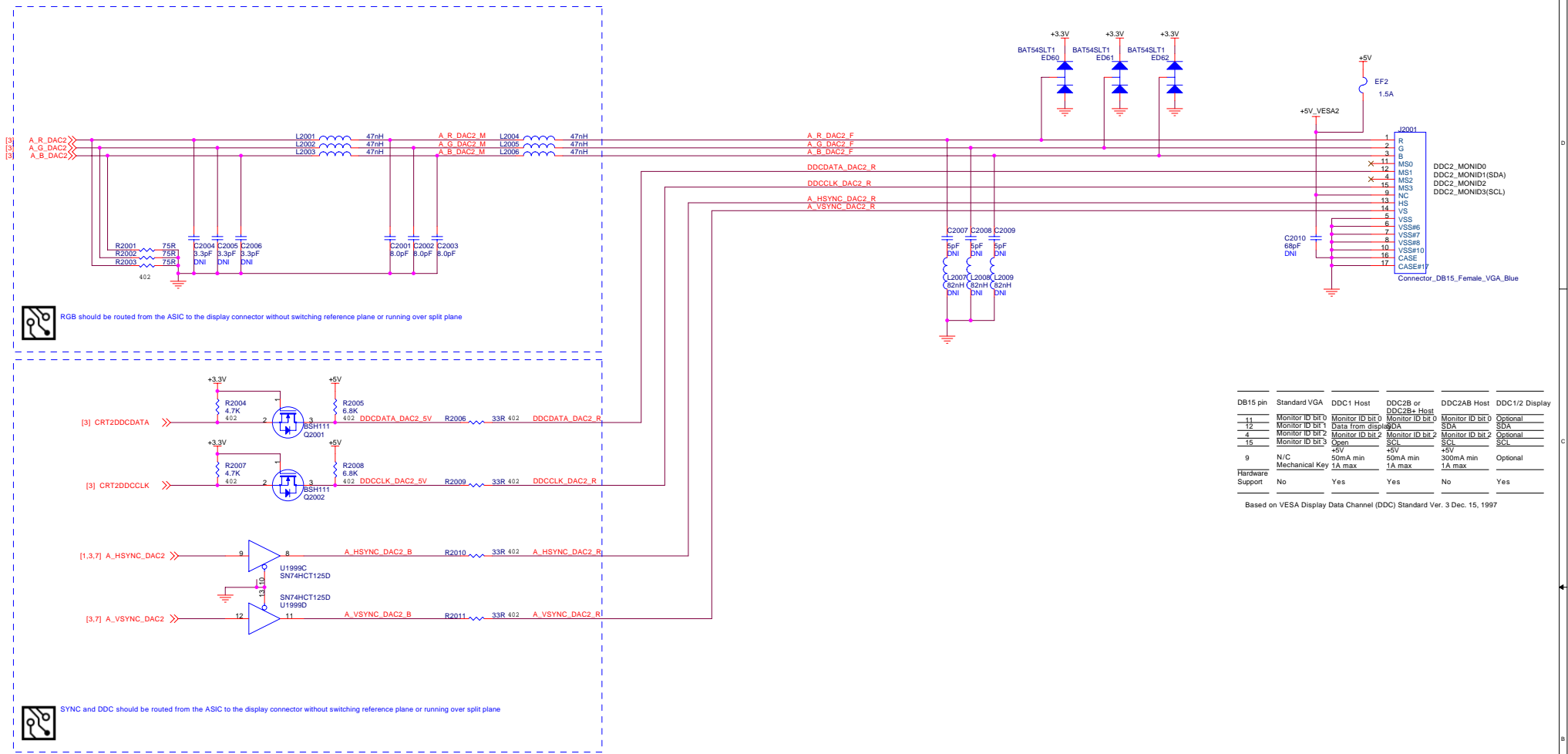
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DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional	Optional
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional	Optional
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional	Optional
15	Monitor ID bit 3	Open	Monitor ID bit 3	Optional	Optional
9	N/C	+5V	+5V	+5V	Optional
Hardware Support	No	Yes	Yes	No	Yes

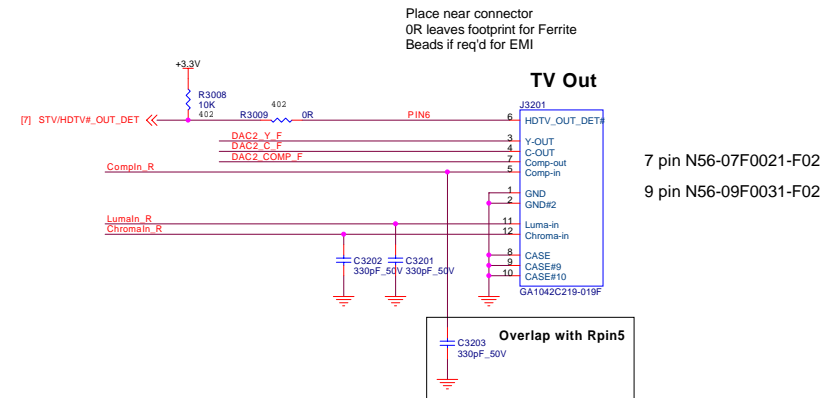
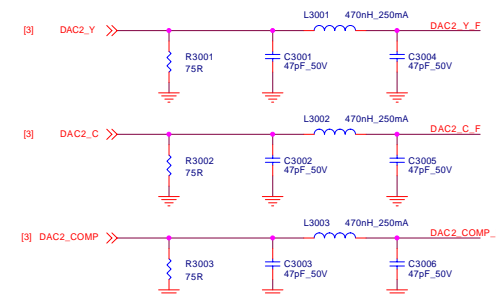
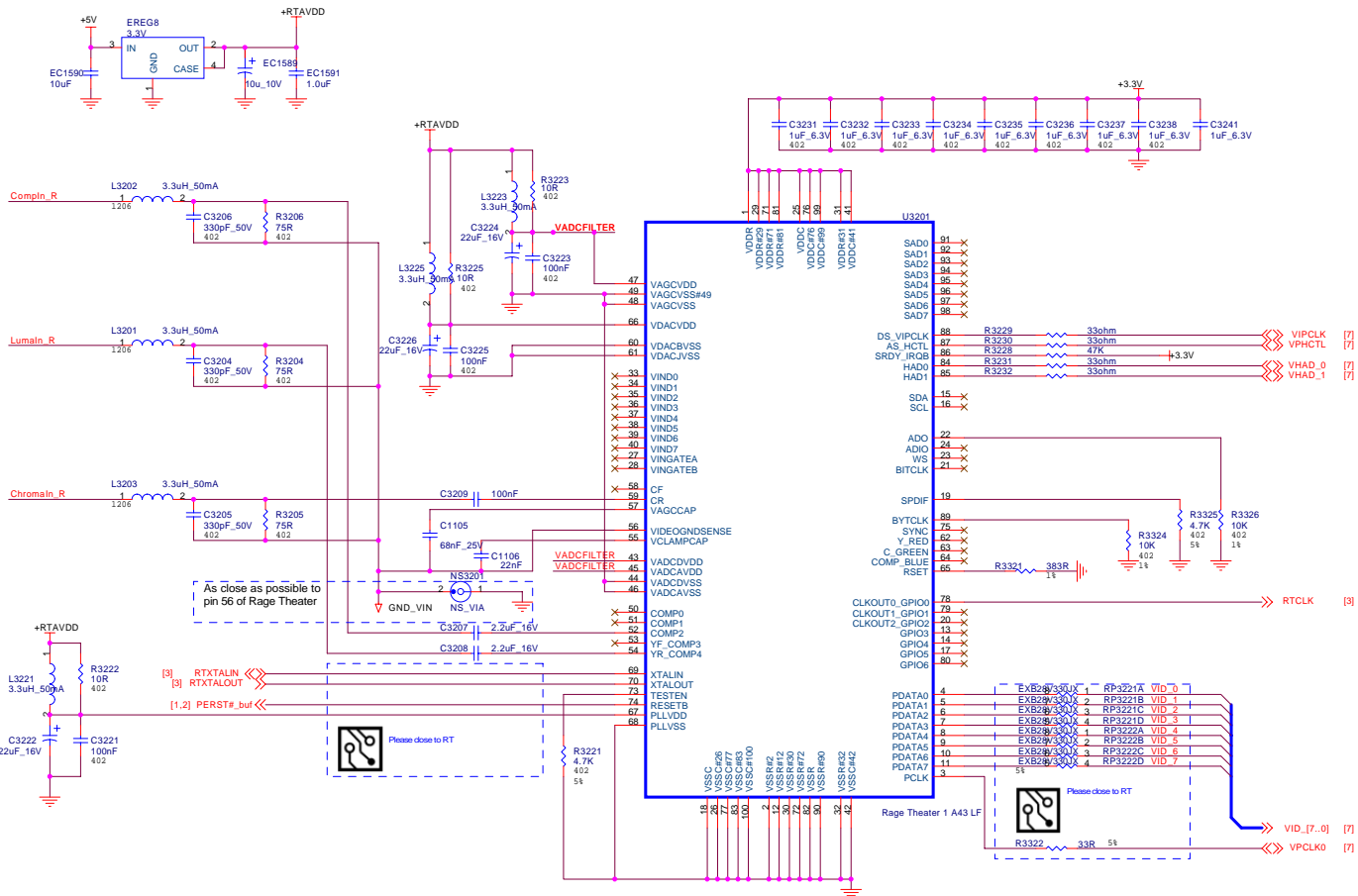
Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



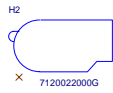
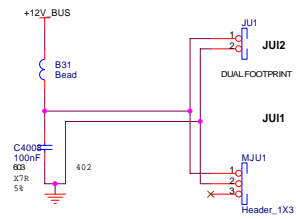
DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	Open	Open	Optional
9	N/C	+5V	+5V	+5V	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	1A max

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

**+RTAVDD**  
**Vout = 3.3V**  
**Iout = 125mA MAX, 80mA RMS**



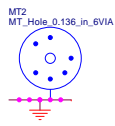
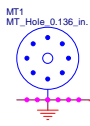
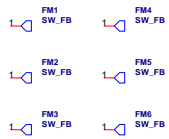
The 7-pin MiniDIN footprint allows one of the two MiniDINs:  
 - 7-pin Svideo/Composite MiniDIN P/N 6071001500G  
 - 4-pin Svideo MiniDIN P/N 6070001000G



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<Variant Name>



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TitleRV515/530 ATX VGA DVI VIVO 256/512MB TSOP

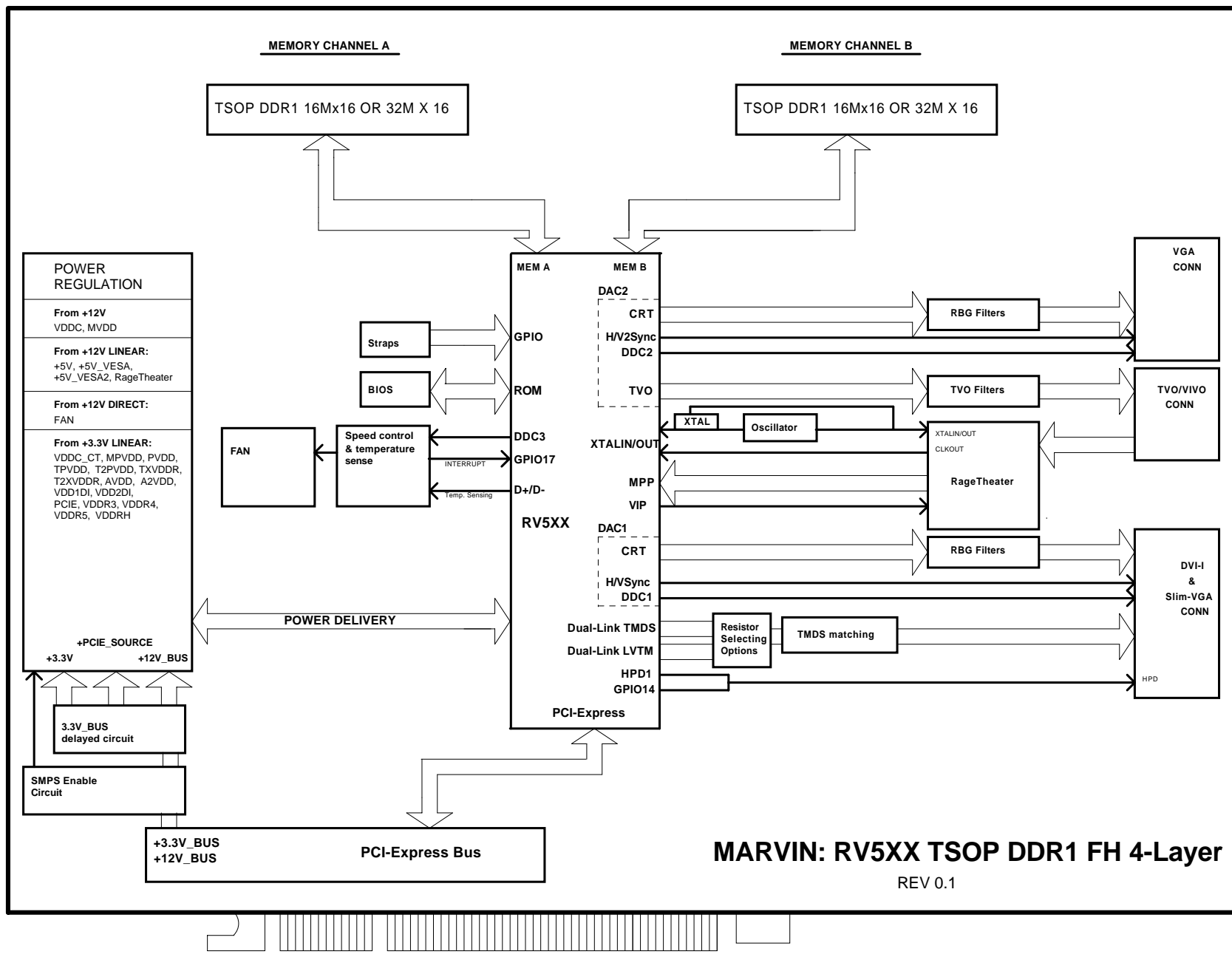
Schematic No.105-A67700-00A

Date:Wednesday, October 05, 2005

REVISION HISTORY

Rev1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/29/05	DERIVE FROM A666
		07/27/05	(pg 01) Correct clock circuitry to support RT (pg 08) Swap R603 and R604 to match layout for documentation purposes (pg 09) Swap R703 and R704 to match layout for documentation purposes (pg 10) Add MVDD linear regulator option (pg 11) Add R986, R987, R988; replace redundant power sequence circuit with +5V_EN and MVDD_EN (pg 11) Add MR911, R918 for +MPVDD for no-tracking option (pg 16) Change C3103 to 603 footprint, change RT to power from 3.3V_BUS to avoid leakage, remove redundant RT clock resistors



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