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P15	1. Change DVI Footprint
	2. Add ESD ROTECTION DIODES
P16	Change DVI Footprint
P17	1. Add ESD ROTECTION DIODES in I2CW
	2. Add POSCAP in DP_PWR
P22	Add Dual BIOS Circuit
P24	Change L802/L803 Footprint
P25	Del C211
P26	1. Change EL4/EL7 Footprint
	2. Change C837/C839/C844/C845/C950 Footprint
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P28	Change EL9 Footprint
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P17	Remove POSCAP and Add 5pcs 22uF MLCC in DP_PWR
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P21	Add GPIO5_SLI_LED_DIM
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P29	1. Add GPIO12_PWR_LVL in U502
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P30	Add SLI LED circuit

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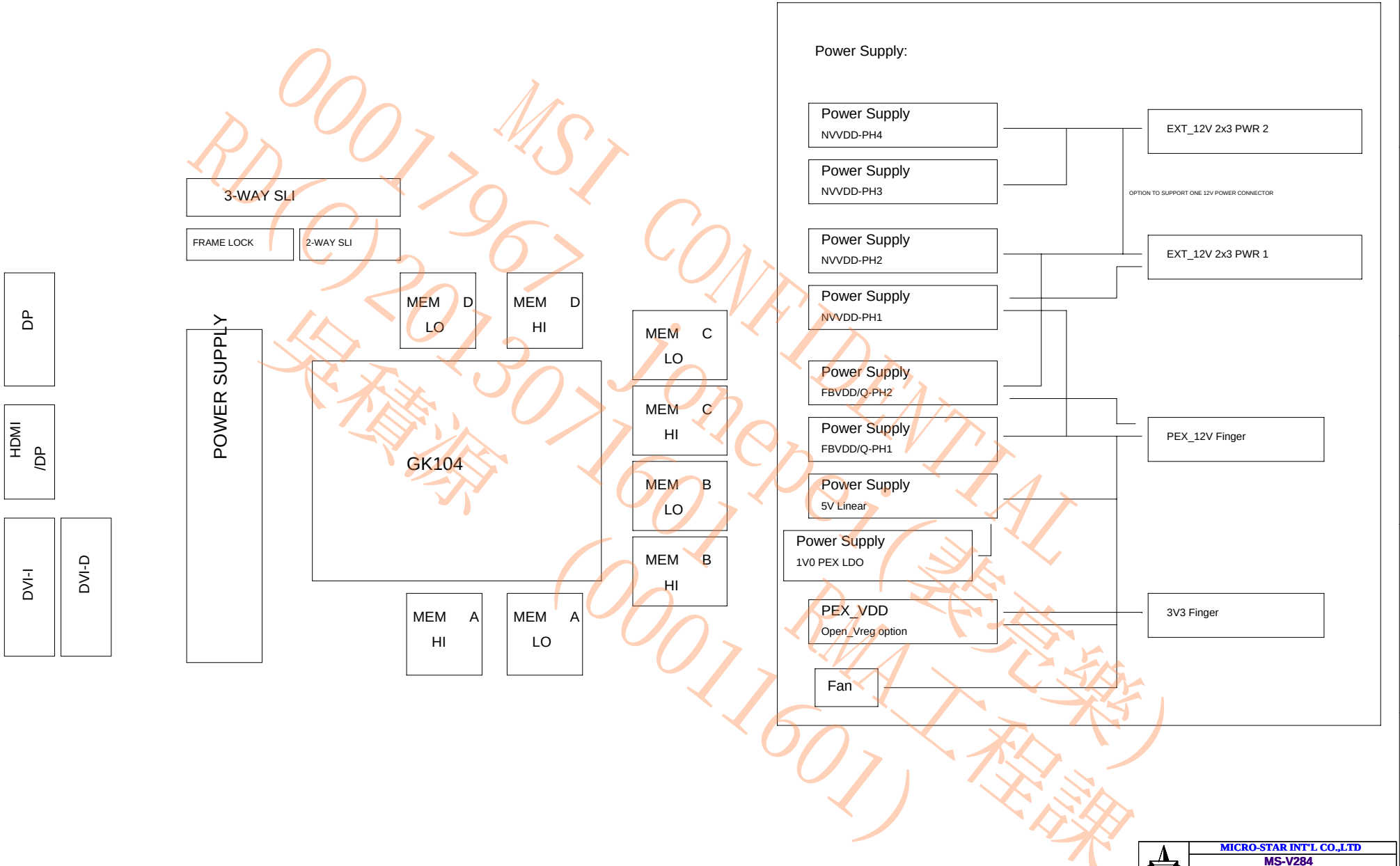
Page2: Block Diagram



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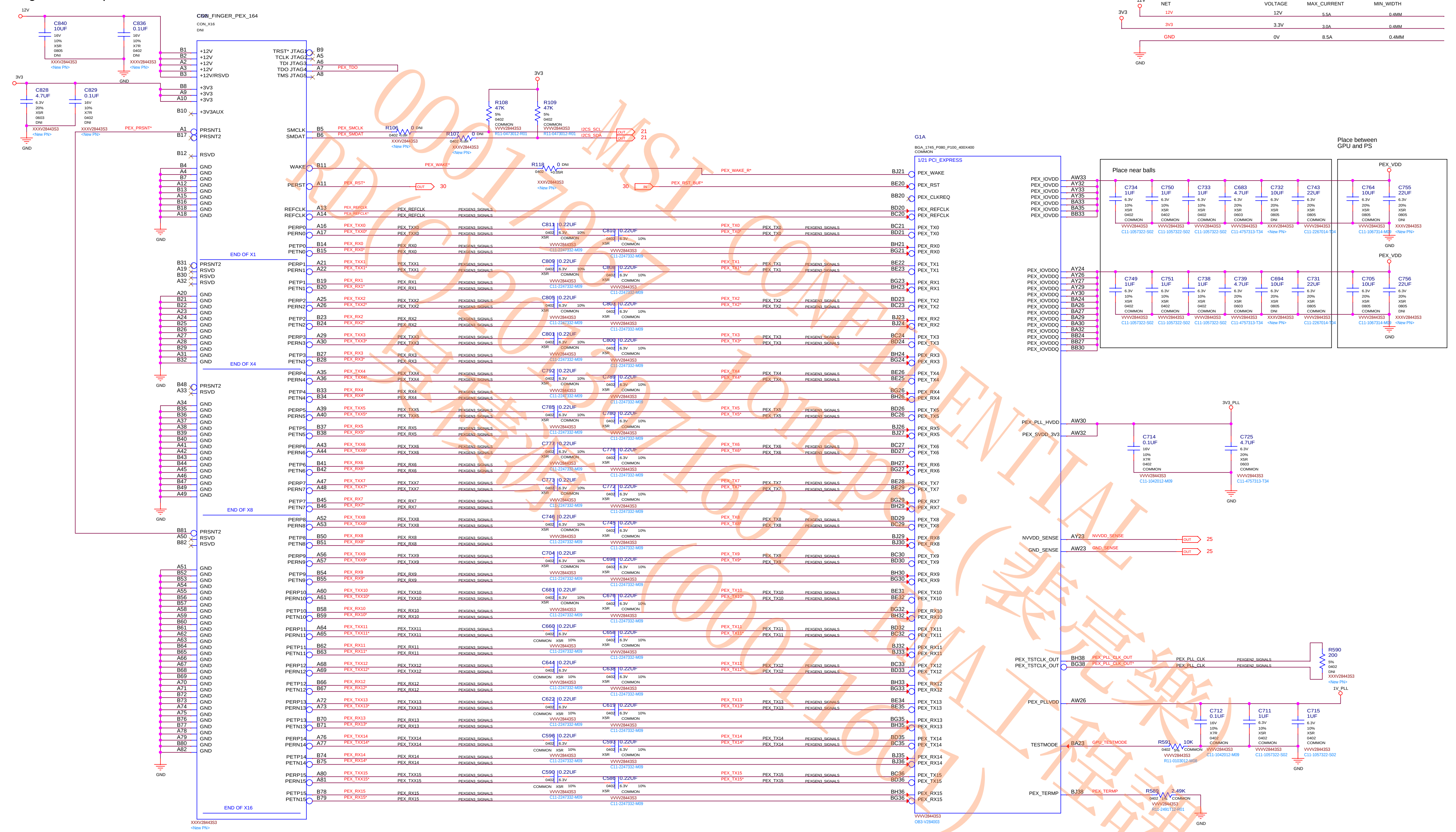
Page3: PCI Express



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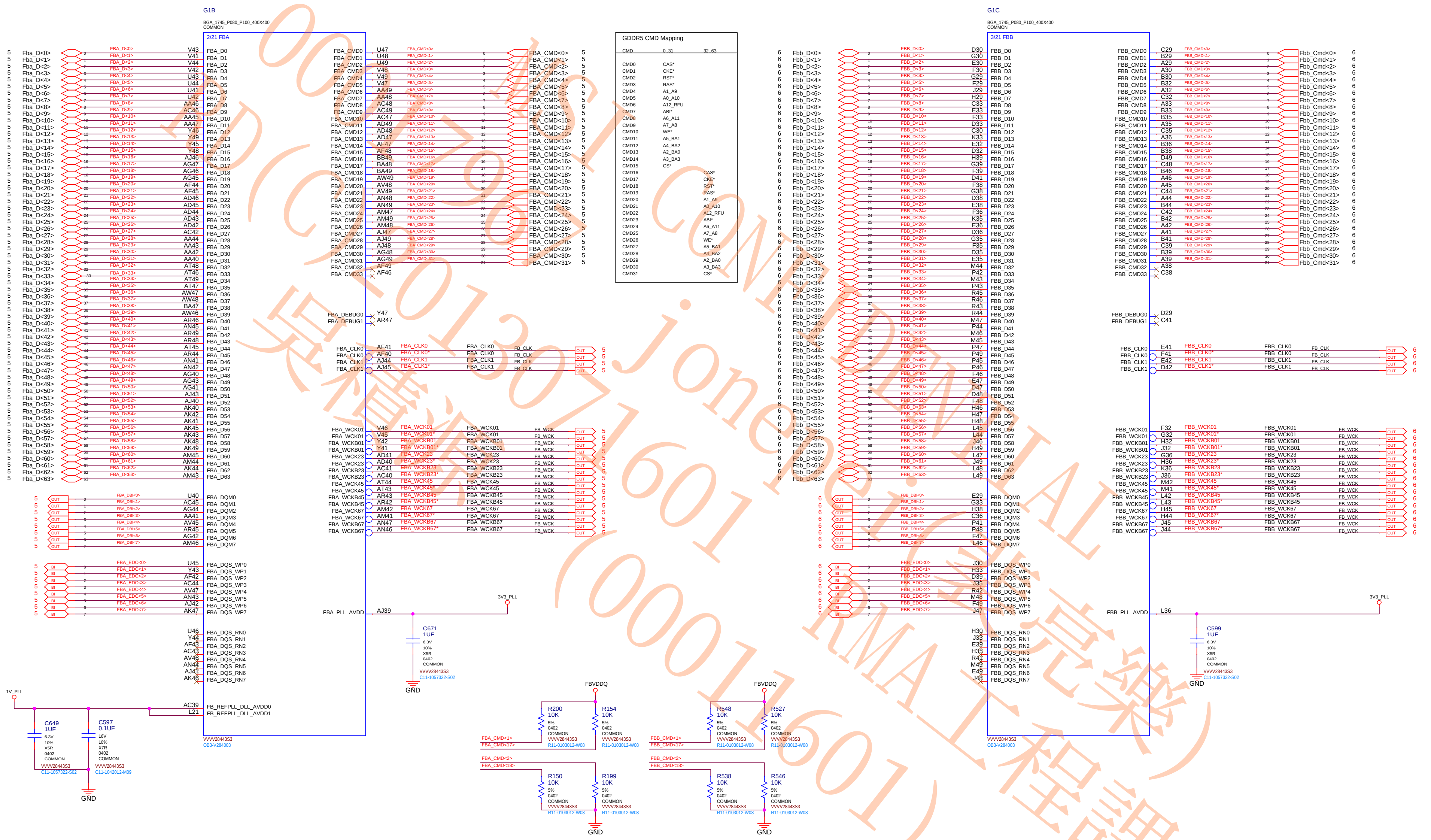
Page4: MEMORY: GPU Partition A/B



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MS-V284		
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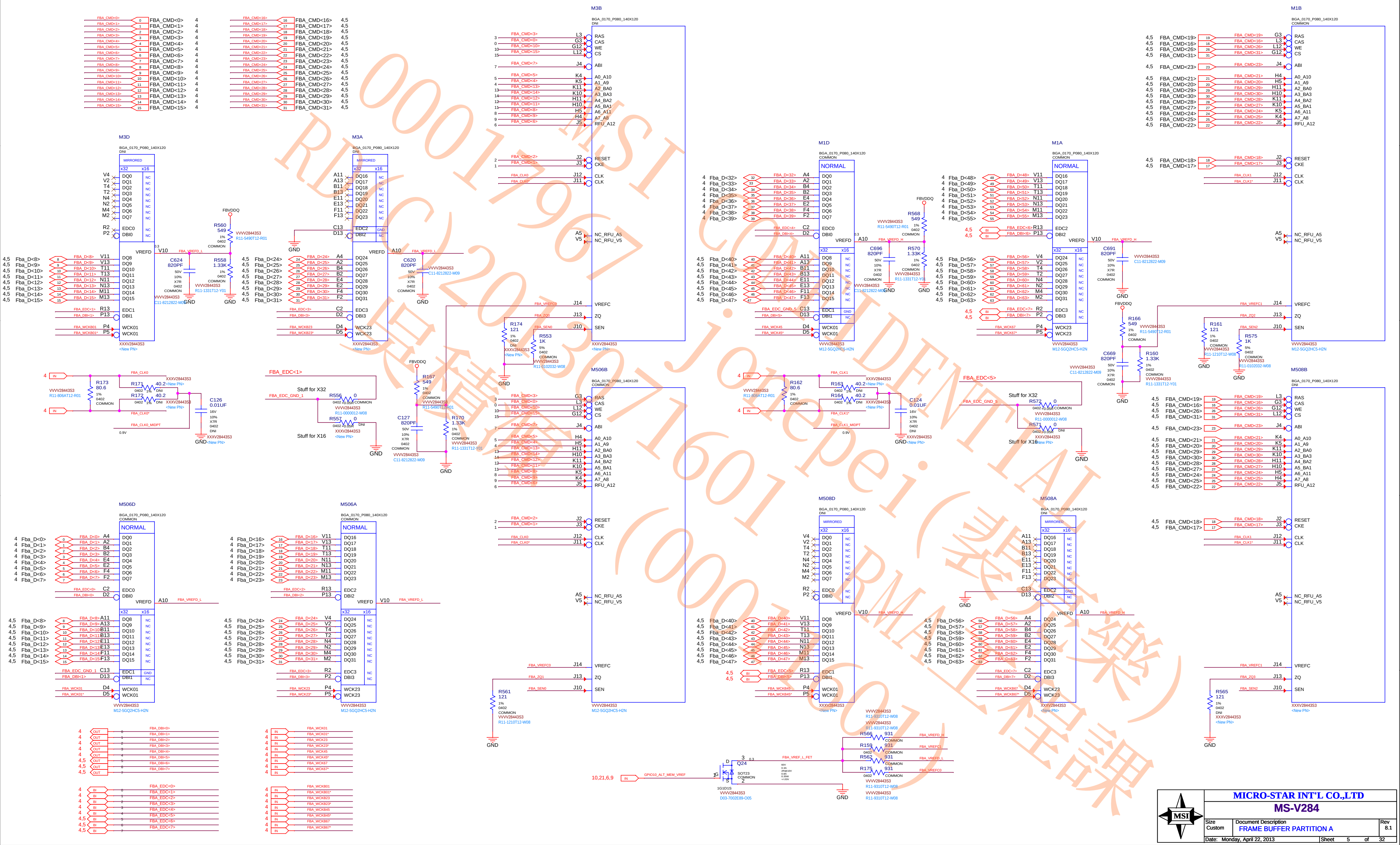
PAGE5: FRAME BUFFER PARTITION A



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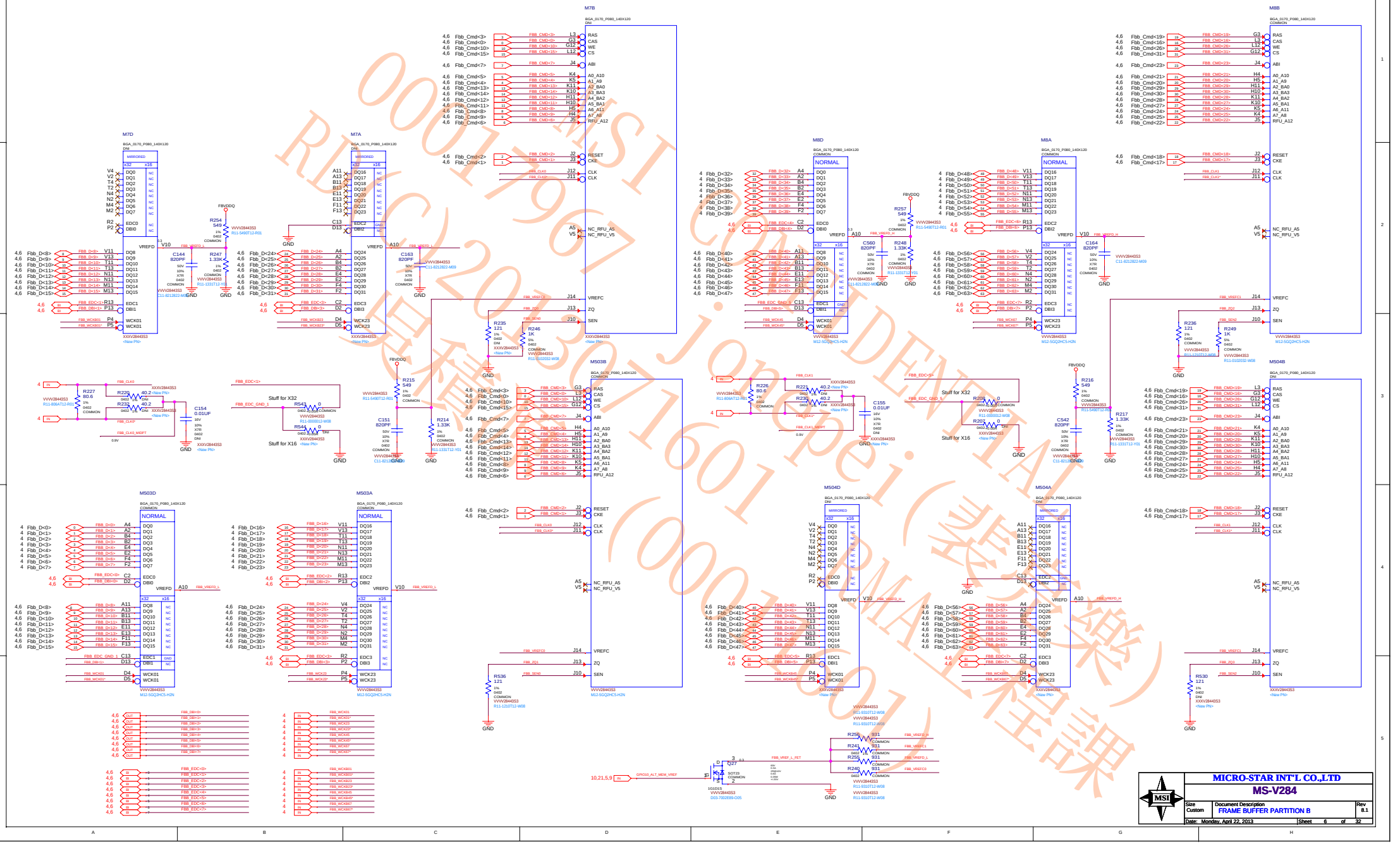
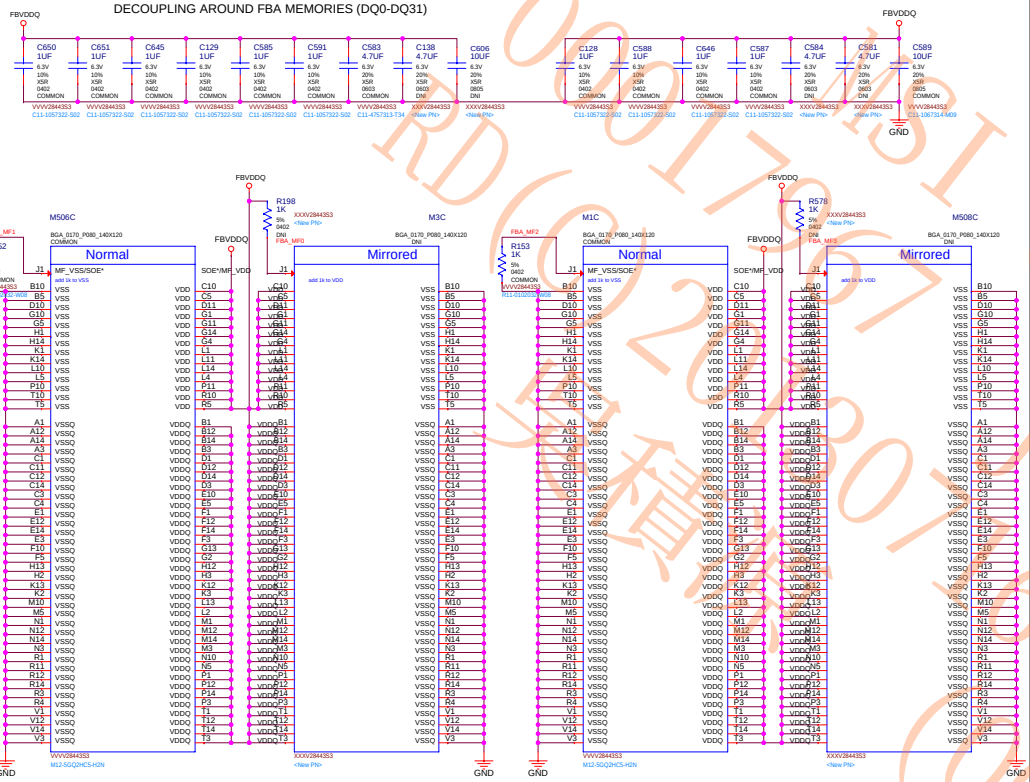
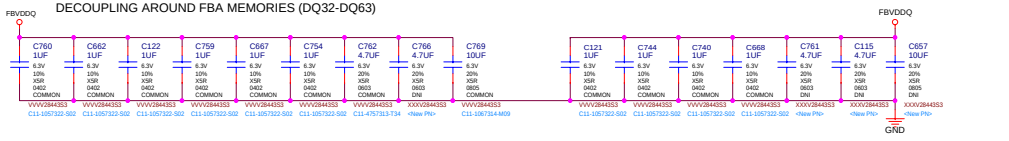
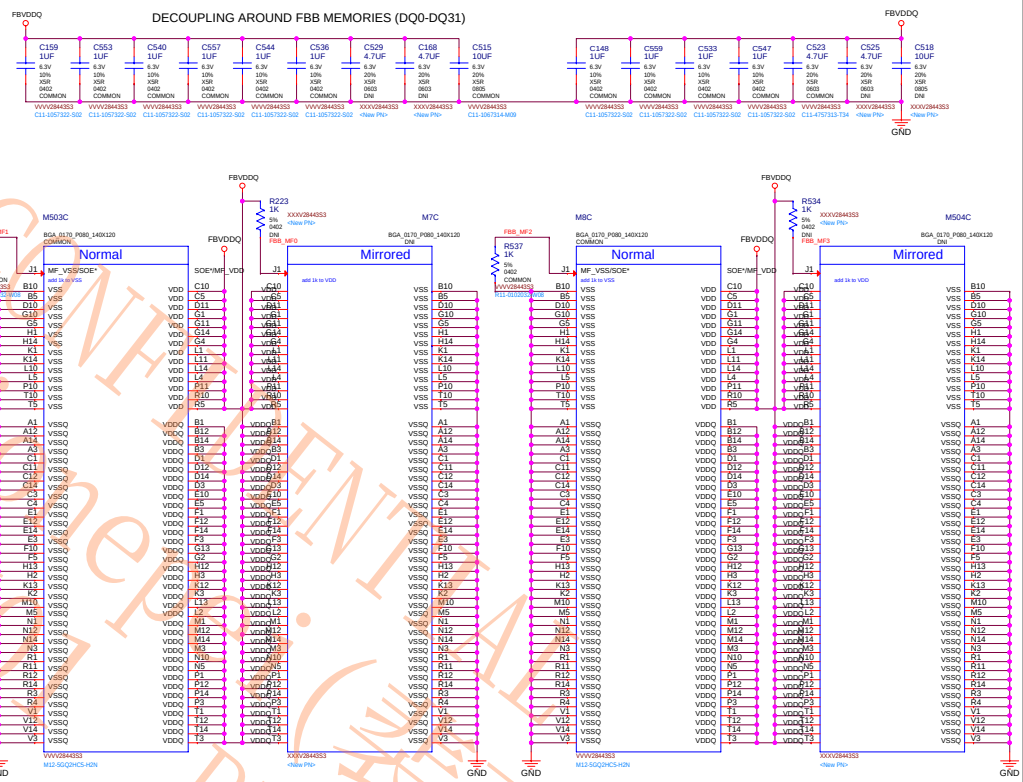
PAGE6: FRAME BUFFER PARTITION B

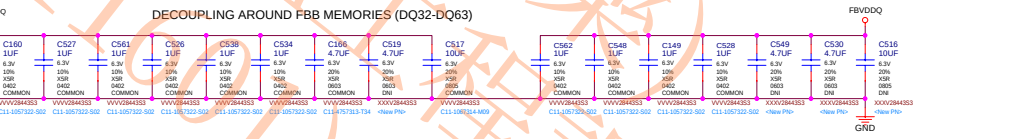


PAGE7: FRAME BUFFER PARTITION A/B DECOUPLING









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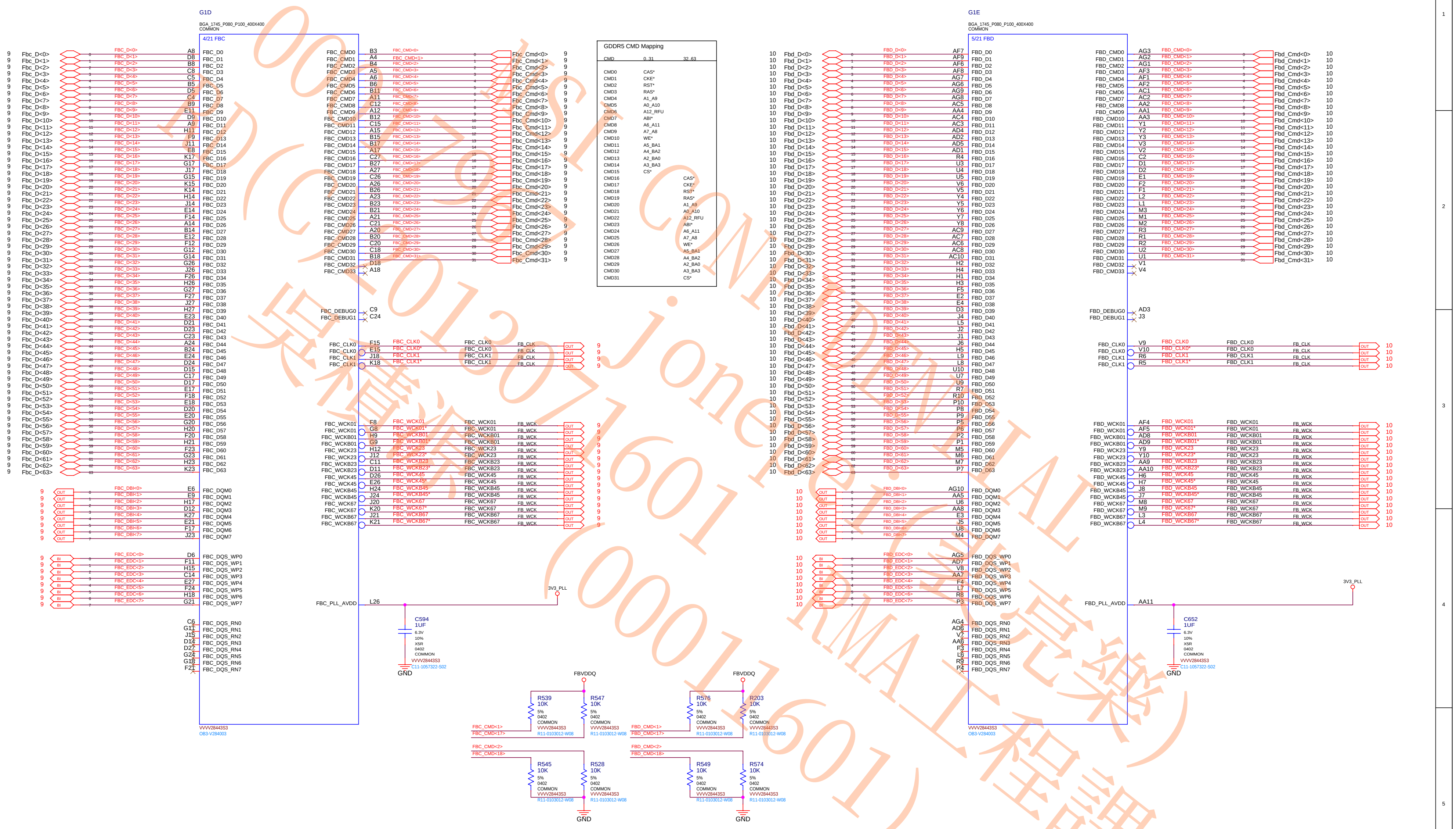
Page8: MEMORY: GPU Partition C/D



GDDR5 CMD Mapping

CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

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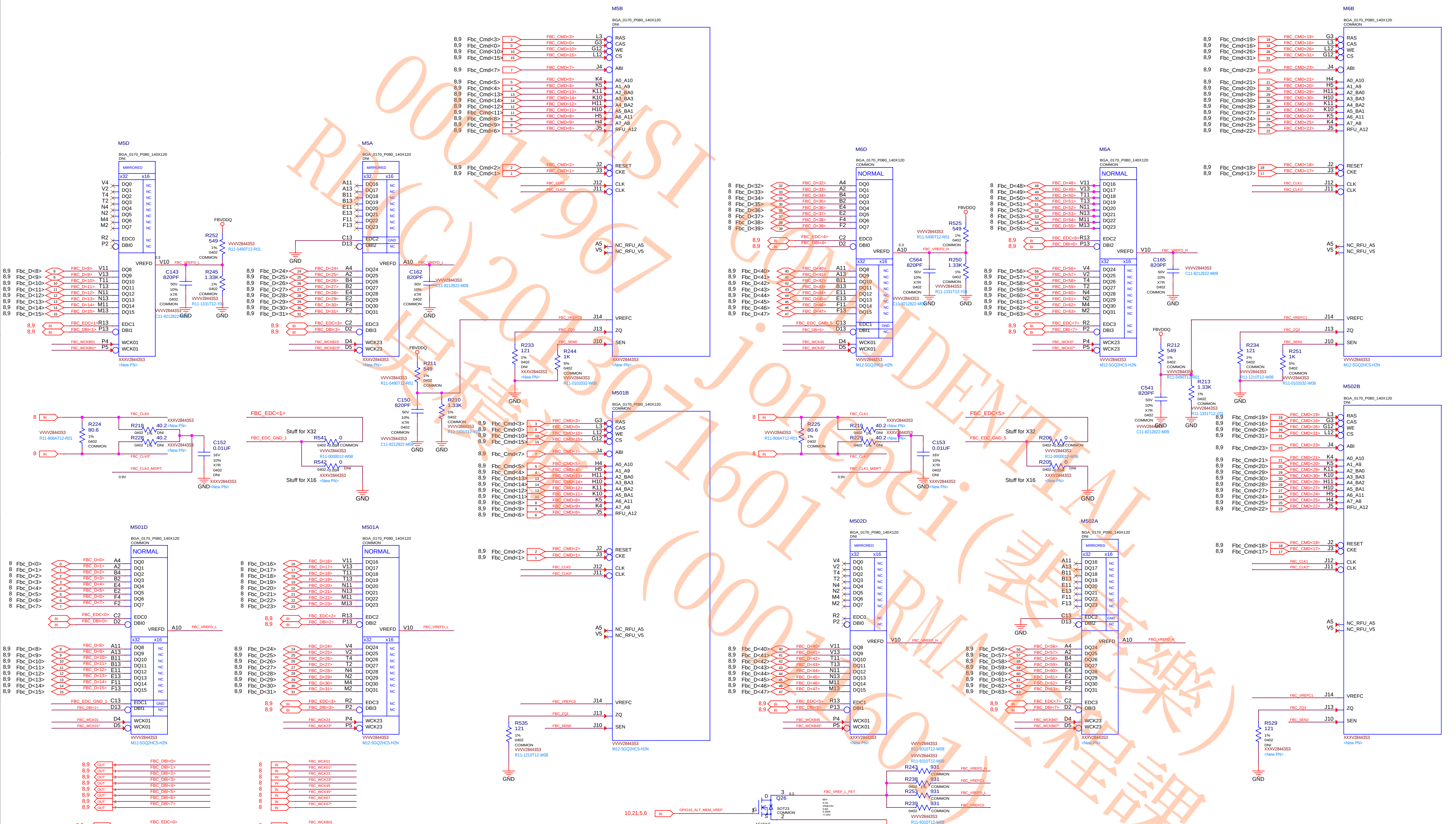
PAGE9: FRAME BUFFER PARTITION C



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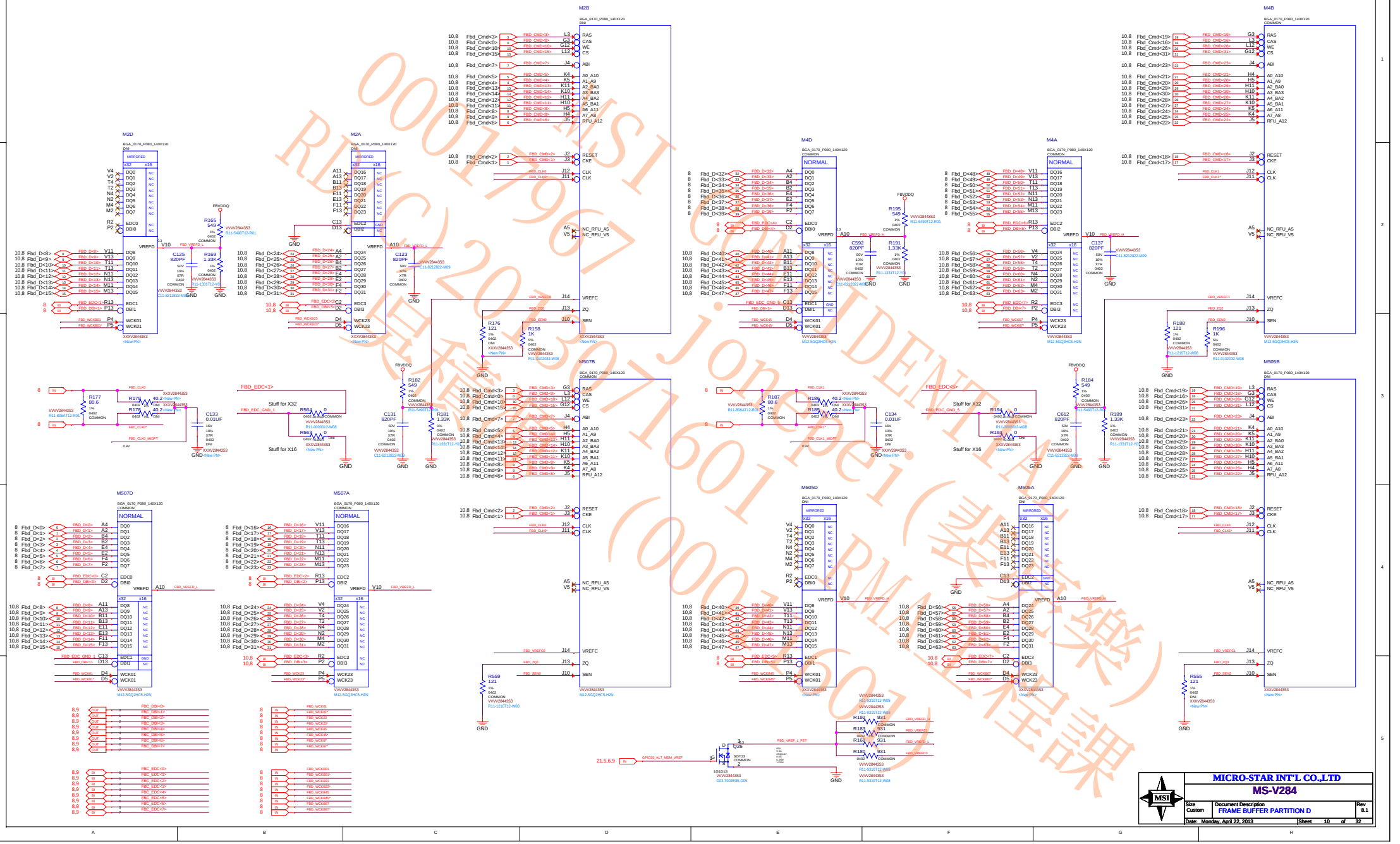
PAGE10: FRAME BUFFER PARTITION D



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Size: Custom	Document Description: FRAME BUFFER PARTITION D
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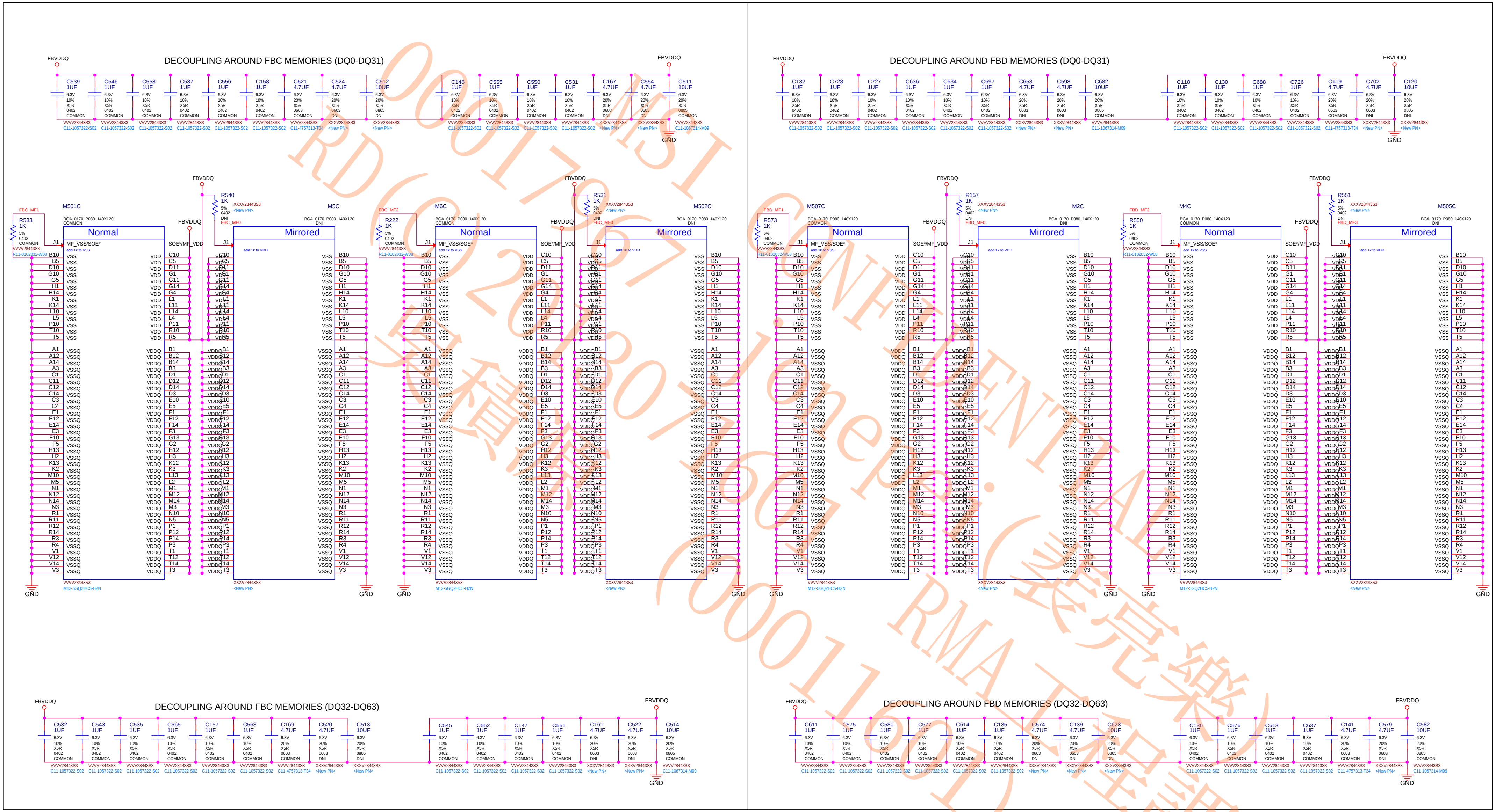
PAGE11: FRAME BUFFER PARTITION C/D DECOUPLING



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Page12: GPU PWR and GND

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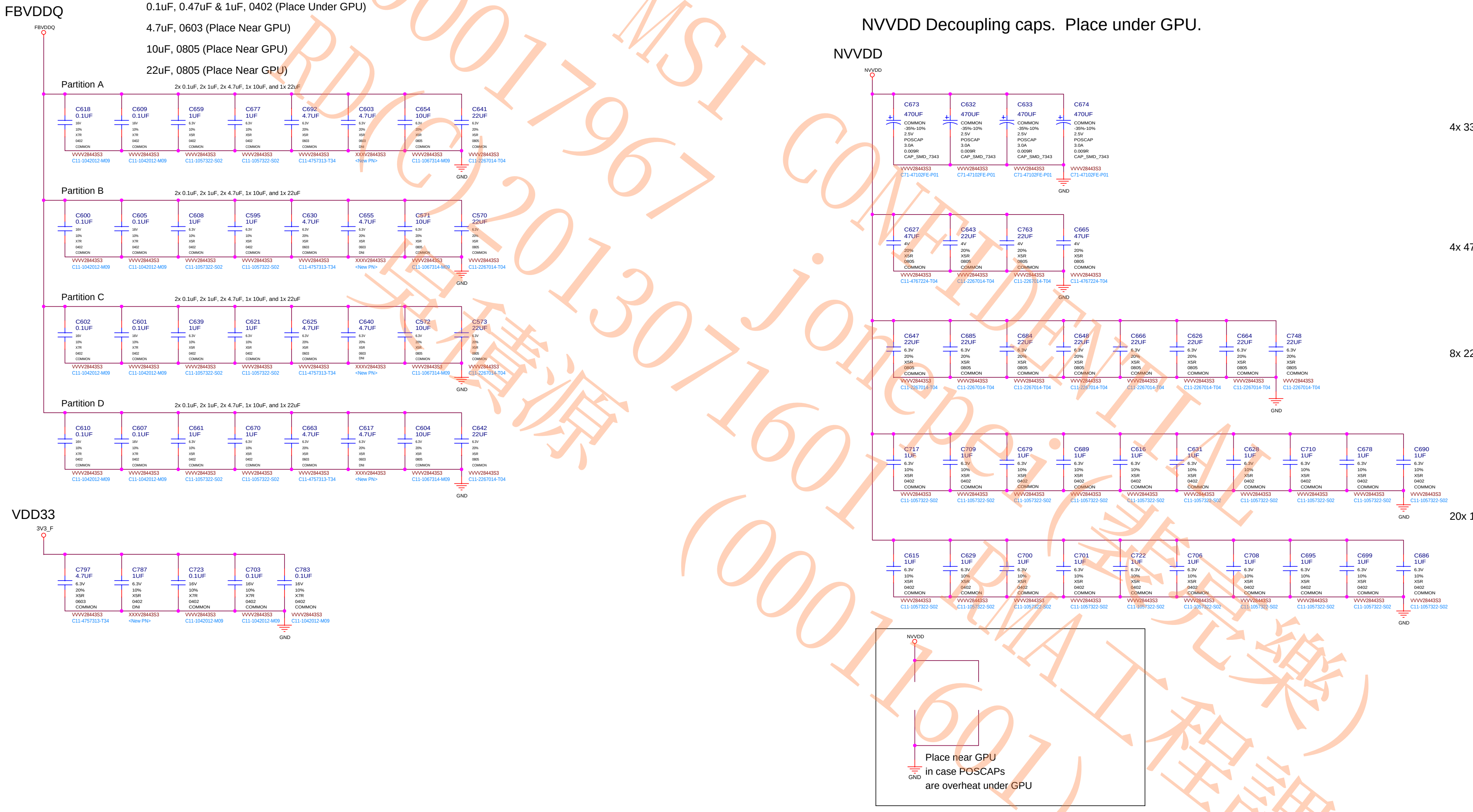
Page13: GPU Decoupling

Based on GB2-X GDDR5 FBVDDQ Decap Guideline



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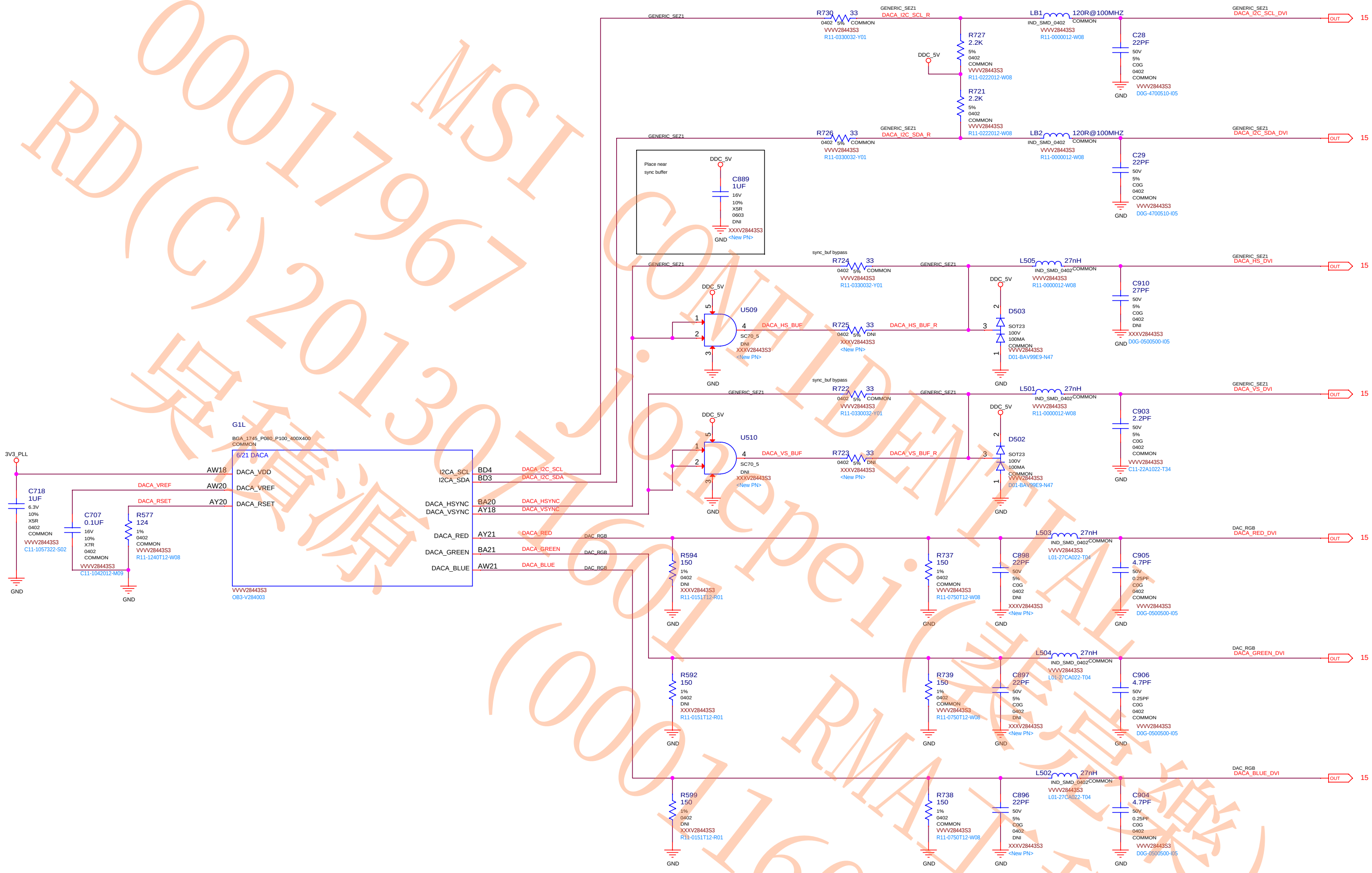
Page14: DACA Interface



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Size: Custom	Document Description: DACA Interface	Rev: 8.1
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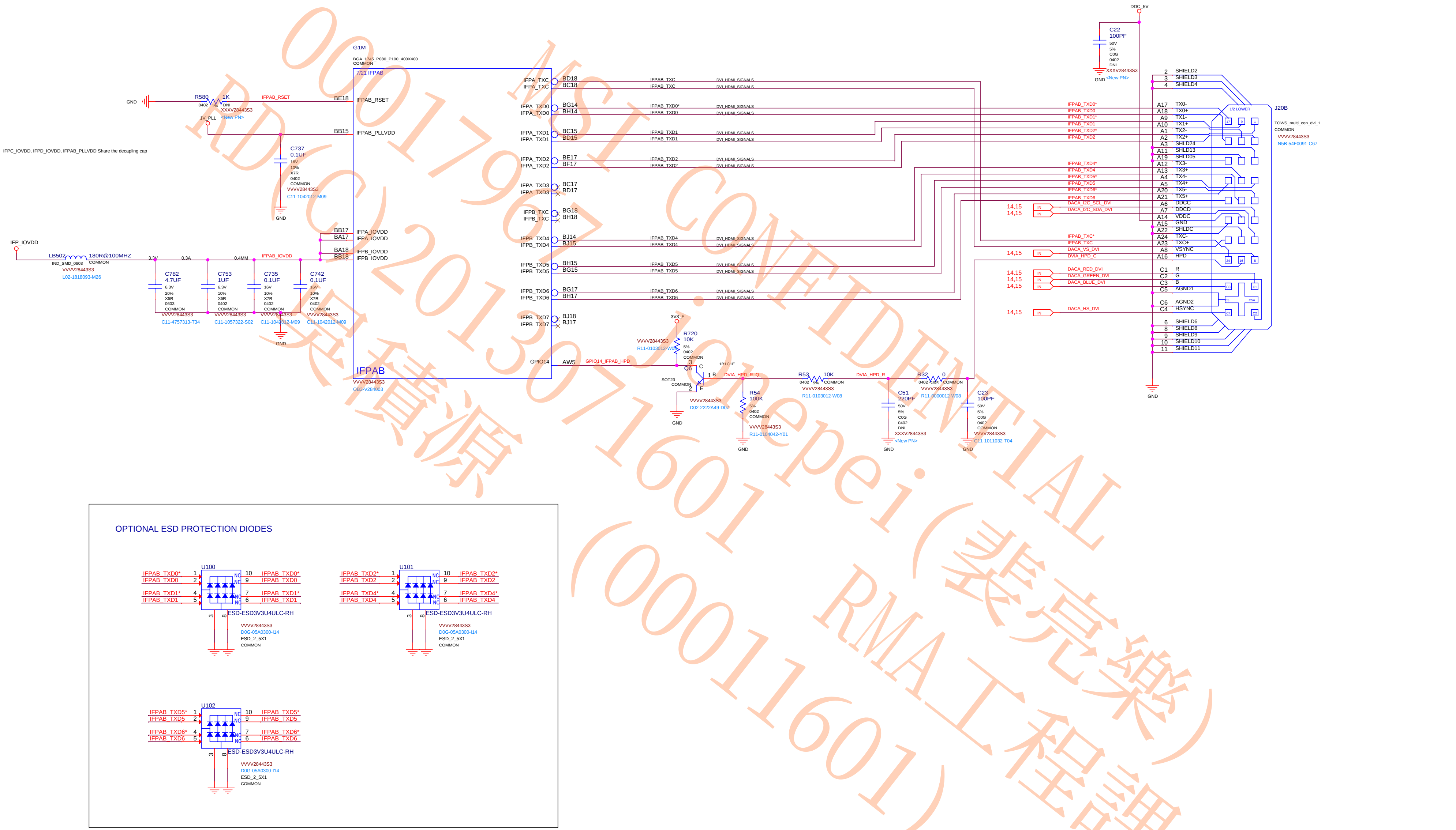
Page15: IFPAB DVI-I-DL



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Size: Custom	Document Description: IFPAB DVI-I-DL	Rev: 8.1
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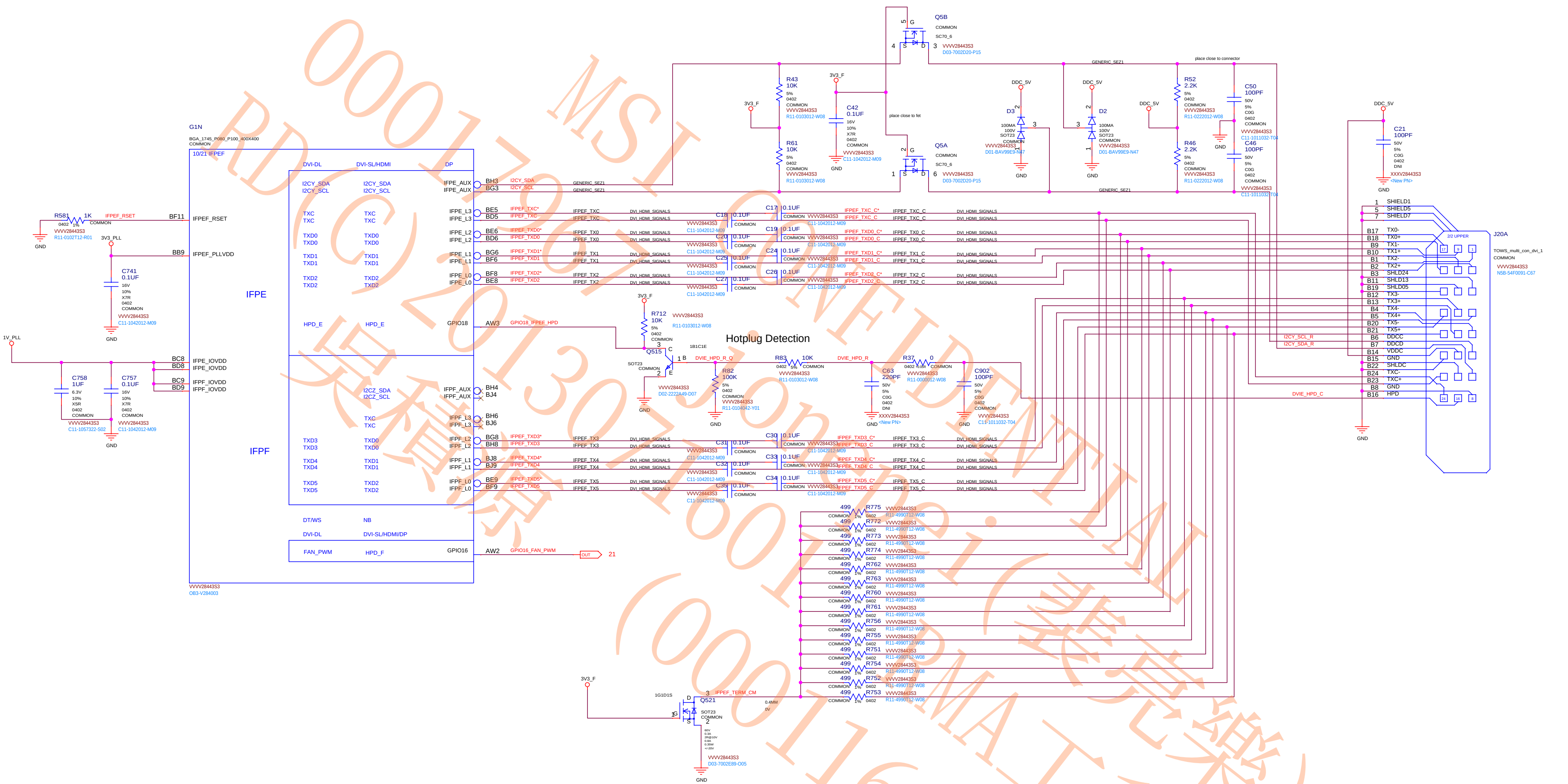
Page16: IFPEF DVI-D-DL



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Size: Custom	Document Description: IFPEF DVI-D-DL	Rev: 8.1
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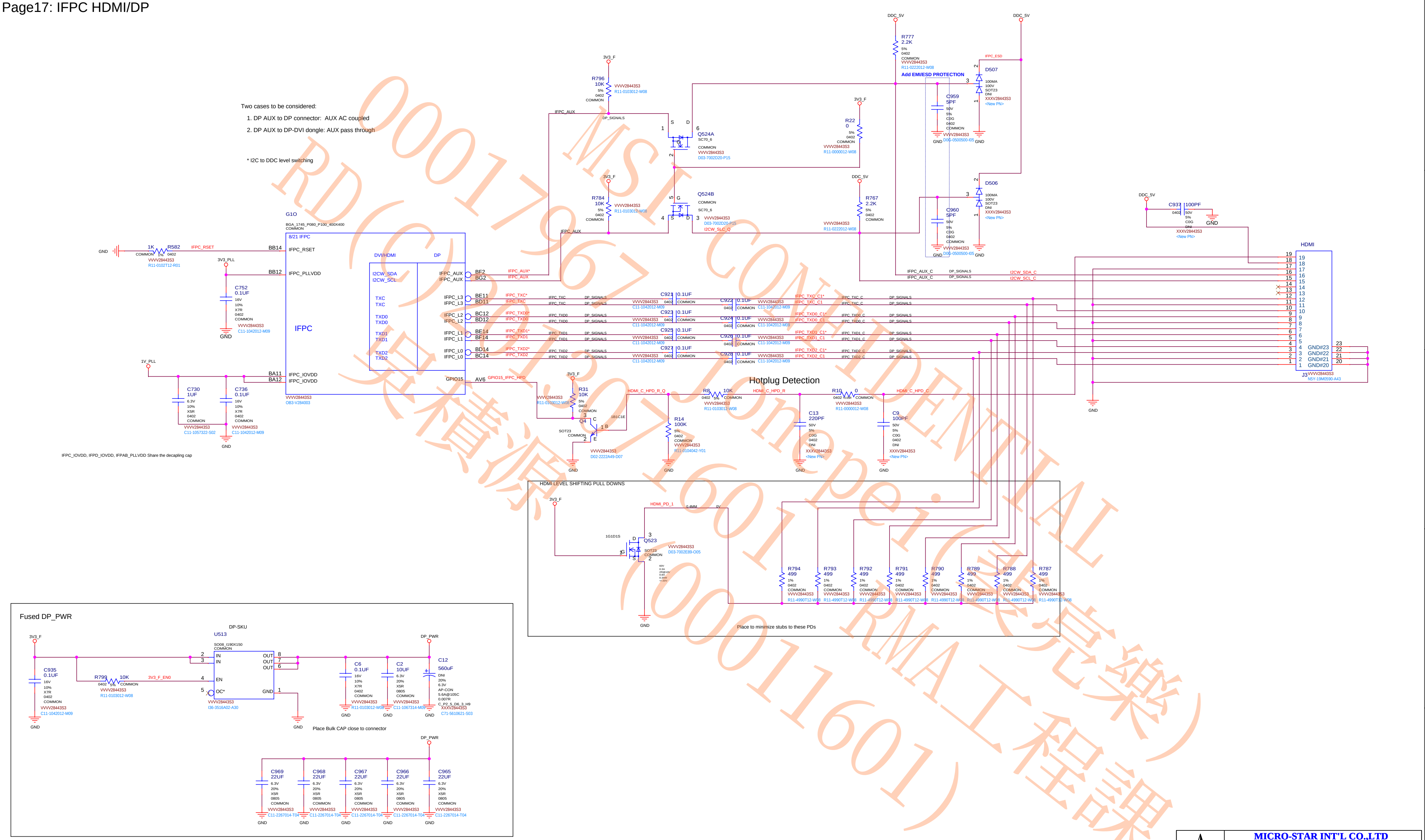
Page17: IFPC HDMI/DP



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Custom	IFPC HDMI/DP	8.1

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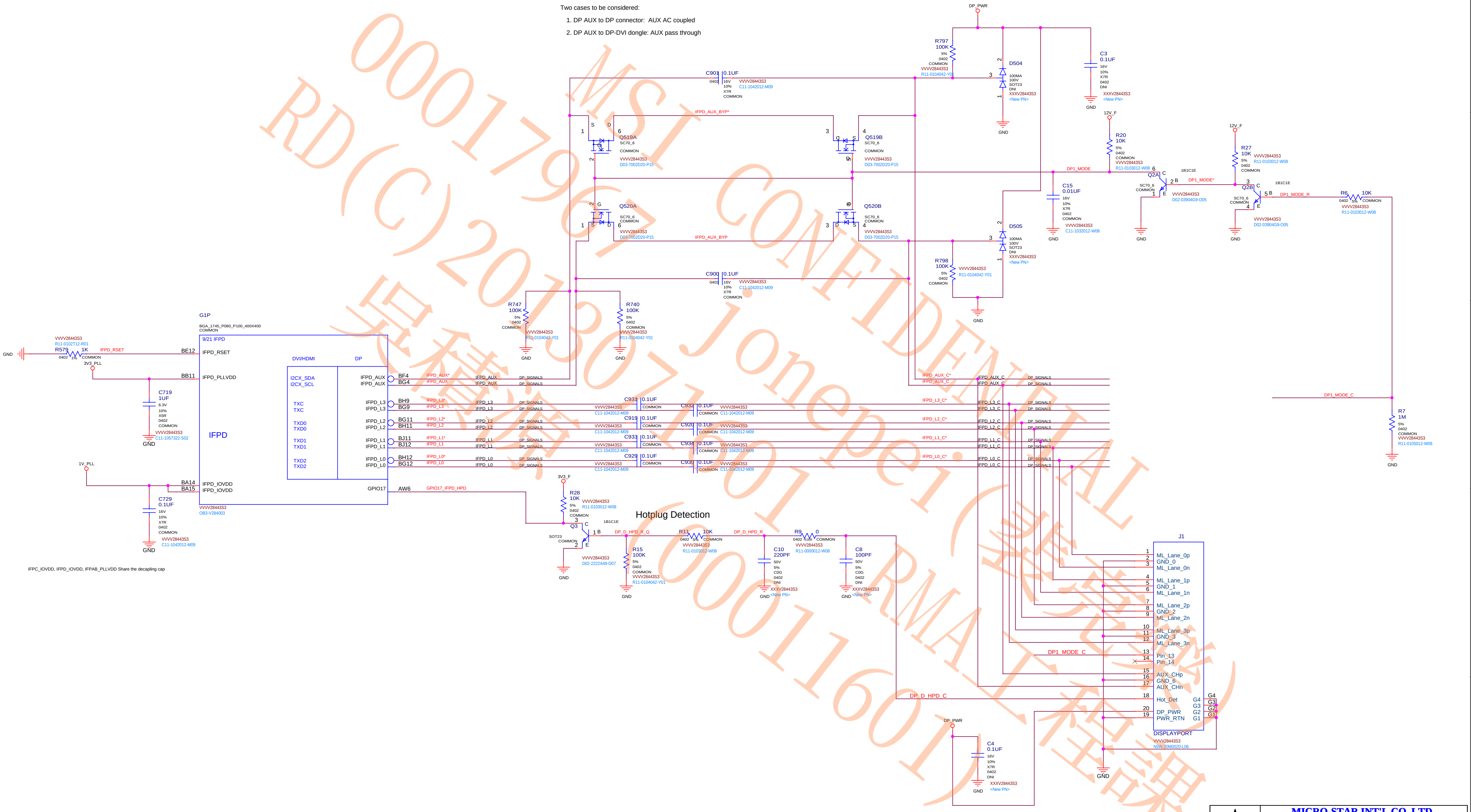
Page18: IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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Custom	IFPD DP	8.1

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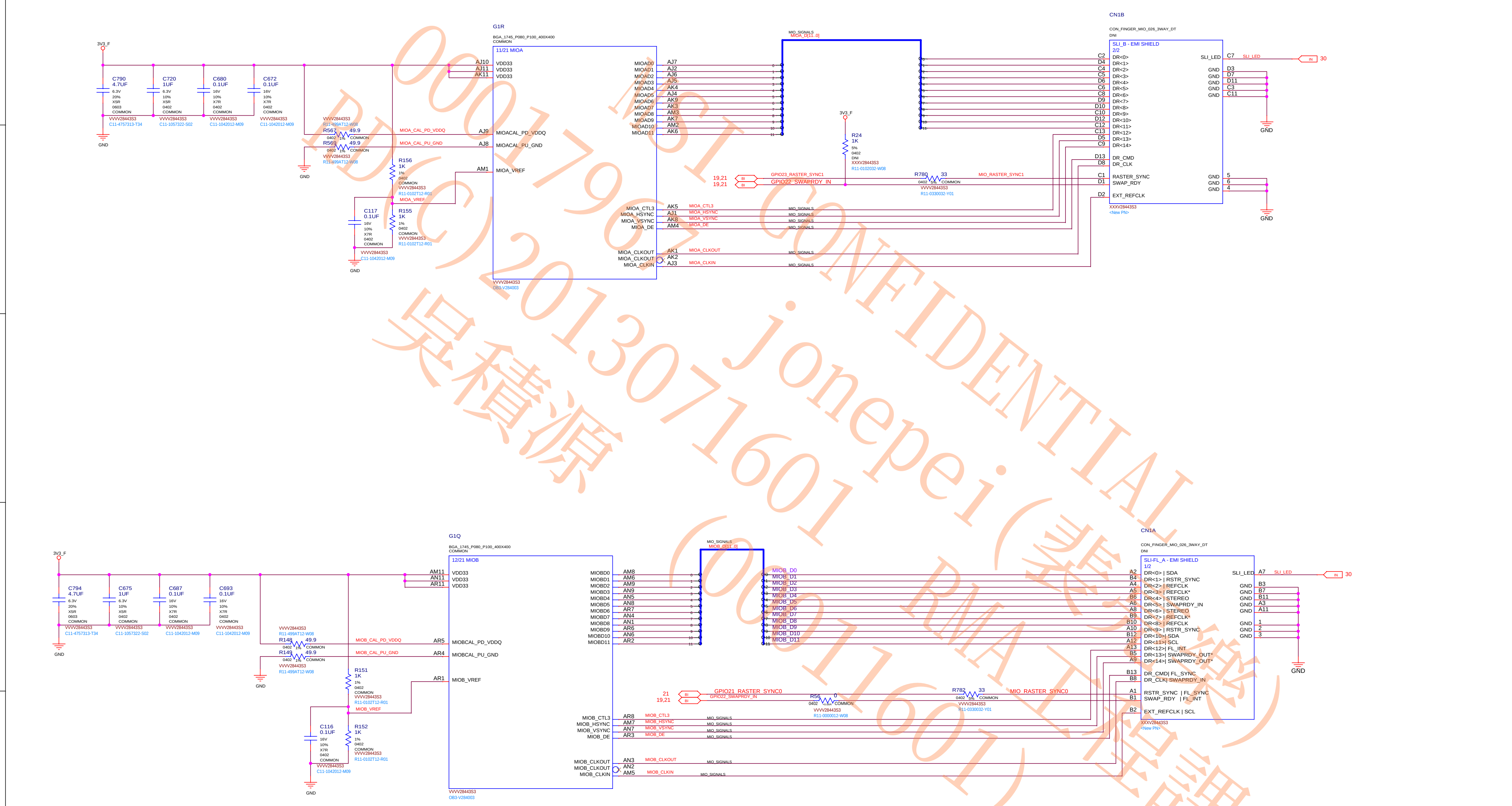
Page19: MIOA/B Interface and Frame Lock



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Page20: Stereo Connector

remove

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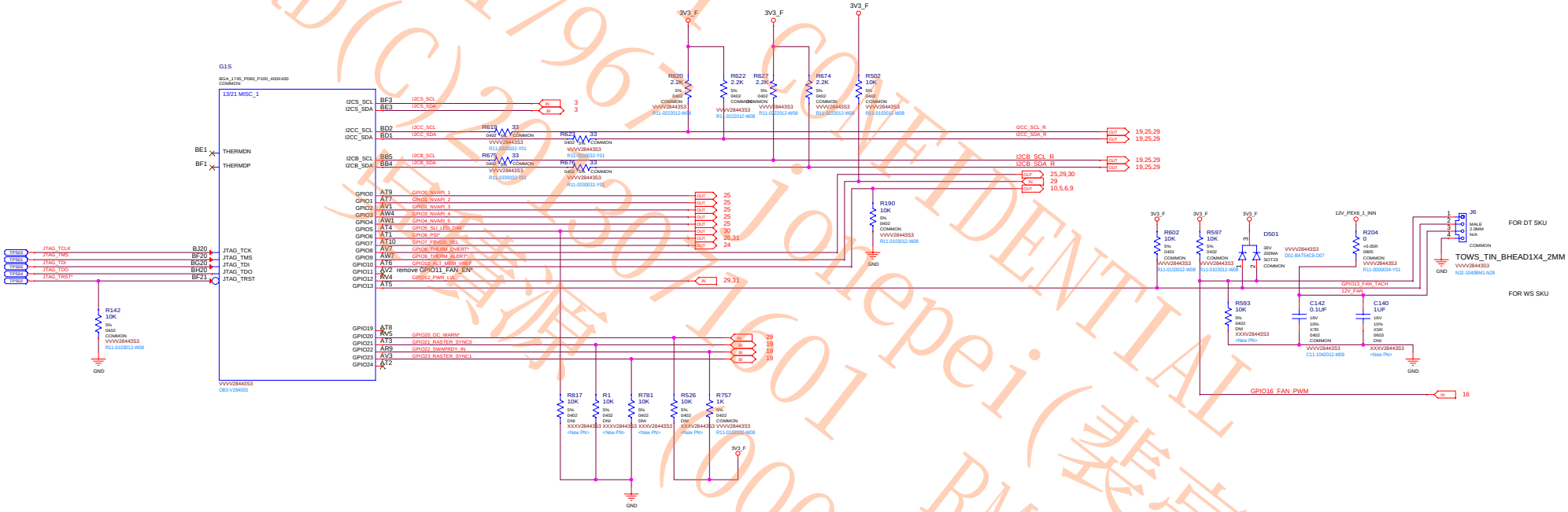

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Size: Custom	Document Description: Fan, Thermal, JTAG,GPIO
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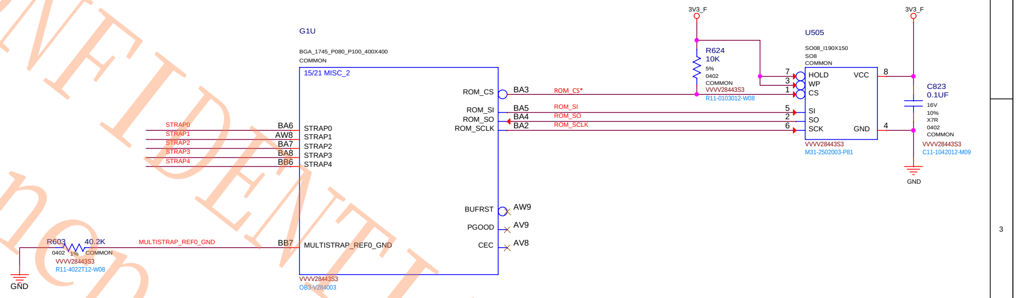
Page22: MISC2: ROM, XTAL, Straps

STRAP0	USER_BIT [3:0]*	0000*		5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*		5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	1001 - (0x1189)*		10K PU -325 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*		45K PU*
STRAP4	DP_PLL_VDD_33V*	1*	FOR 3_3V*	45K PD*
	PEX_MAX_SPEED*	1*	FOR GEN2/3*	
	PEX_SPD_CHANGE_GEN3*	1*	ENABLED*	
	*			
ROM_SI	RAMCFG[0]*	0*		64Mx32 256 bit hynix for SKU5 primary memory 35K PD*
	RAMCFG[1]*	1*		
	RAMCFG[2]*	1*		
	RAMCFG[3]*	0*		
ROM_SO	VGA_DEVICE*	1*		30k PD*
	SMB_ALT_ADDR*	0*		
	FB[0]_APERTURE_SIZE*	1*	For 128MB*	
	FB[1]_APERTURE_SIZE*	0*	For 128MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0*	DISABLE*	25K PD*
	PCI_DEVID_EXT[5]*	0*	For 0x1189*	
	SUB_VENDOR*	1*	Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0*	For 0x1189*	

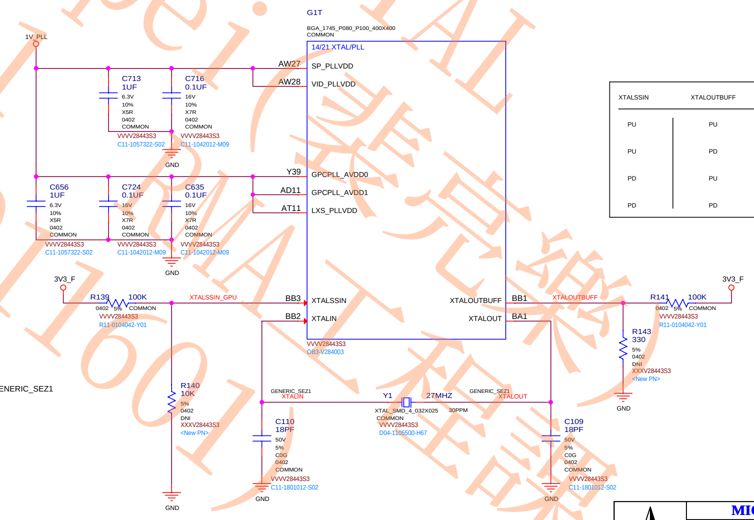
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

X32 MODE 256bit

CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	32Mx32	256-bit	Elpida
0010	32Mx32	256-bit	Hynix
0011	32Mx32	256-bit	Samsung
0100	Reserved		
0101	64Mx32	256-bit	Elpida
0110	64Mx32	256-bit	Hynix
0111	64Mx32	256-bit	Samsung

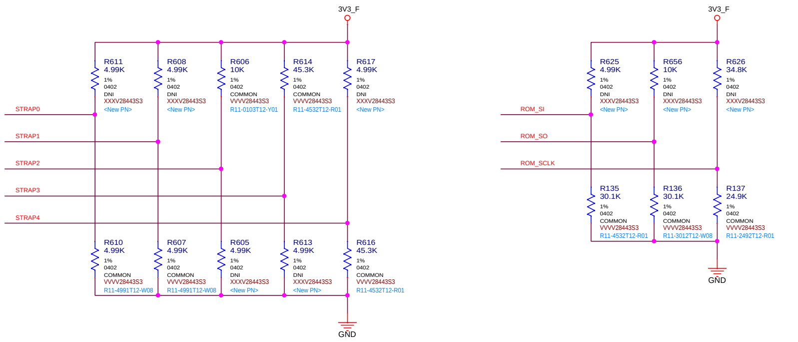


	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND



remove XTALSSIN_GPU/GENERIC_SEZ1

XTALSSIN	XTALOUTBUFF	Inverted SmartFan PWM %
PU	PU	66(33% high)
PU	PD	50(50% high)
PD	PU	33(66% high)
PD	PD	0(100% high)



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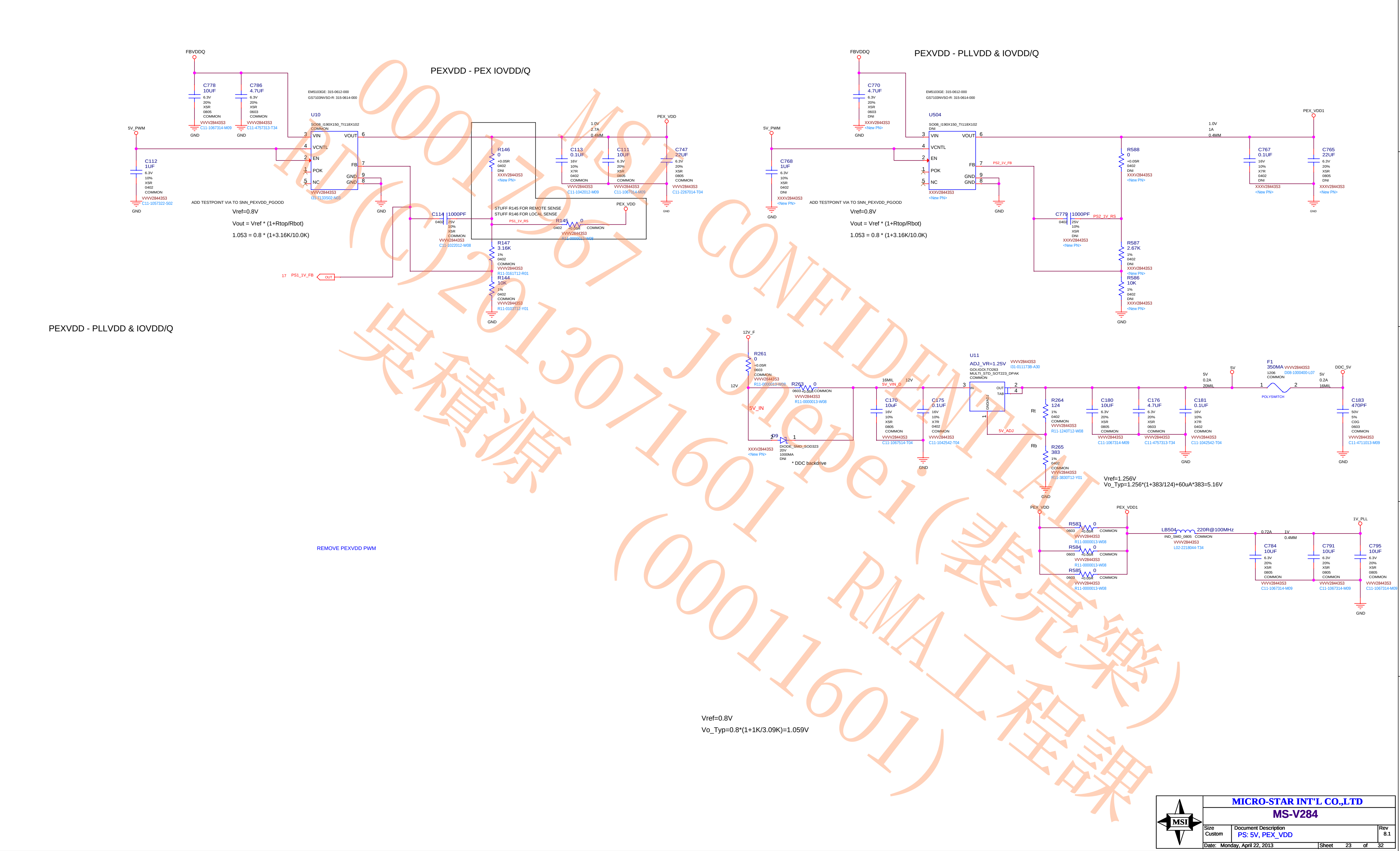
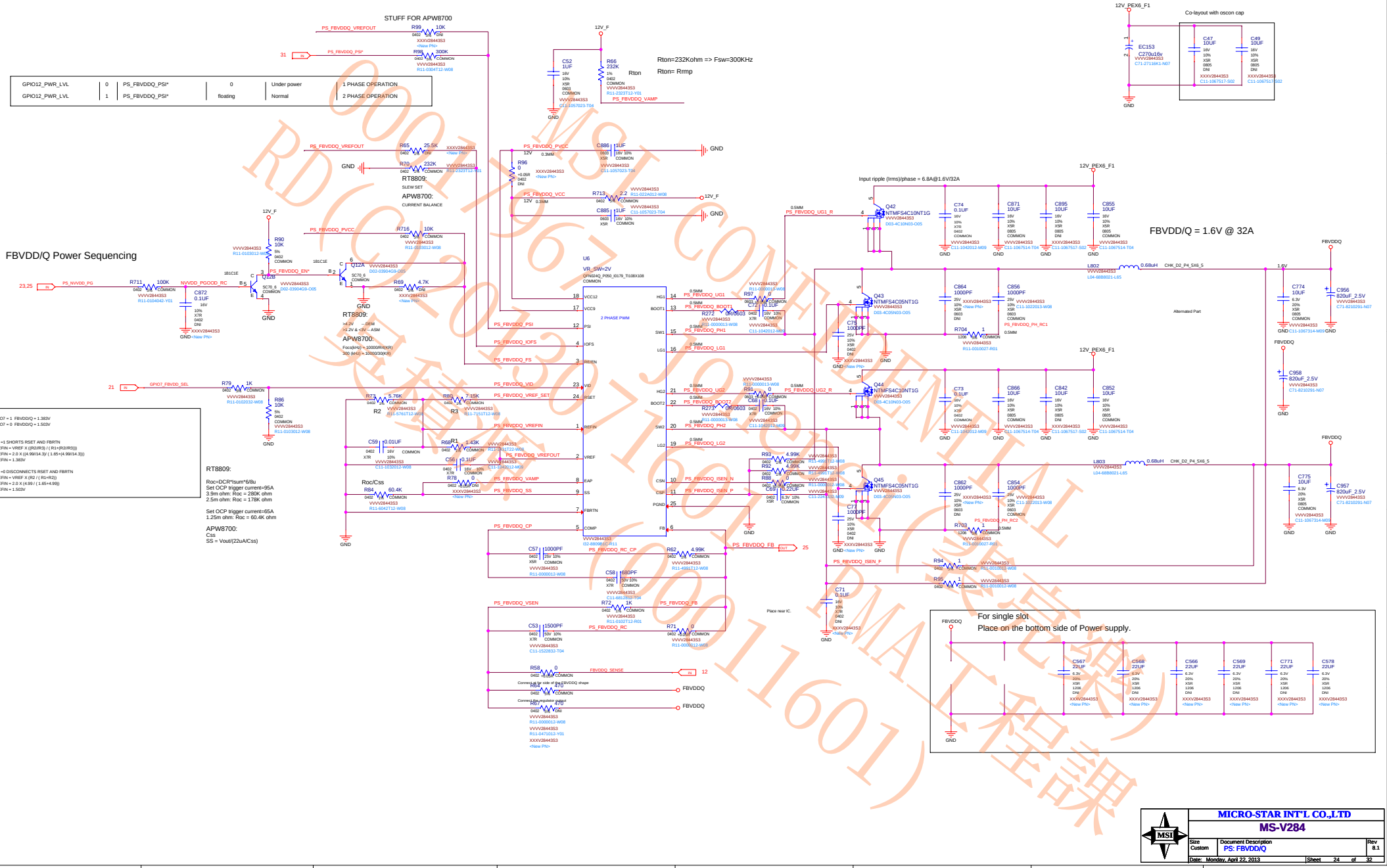
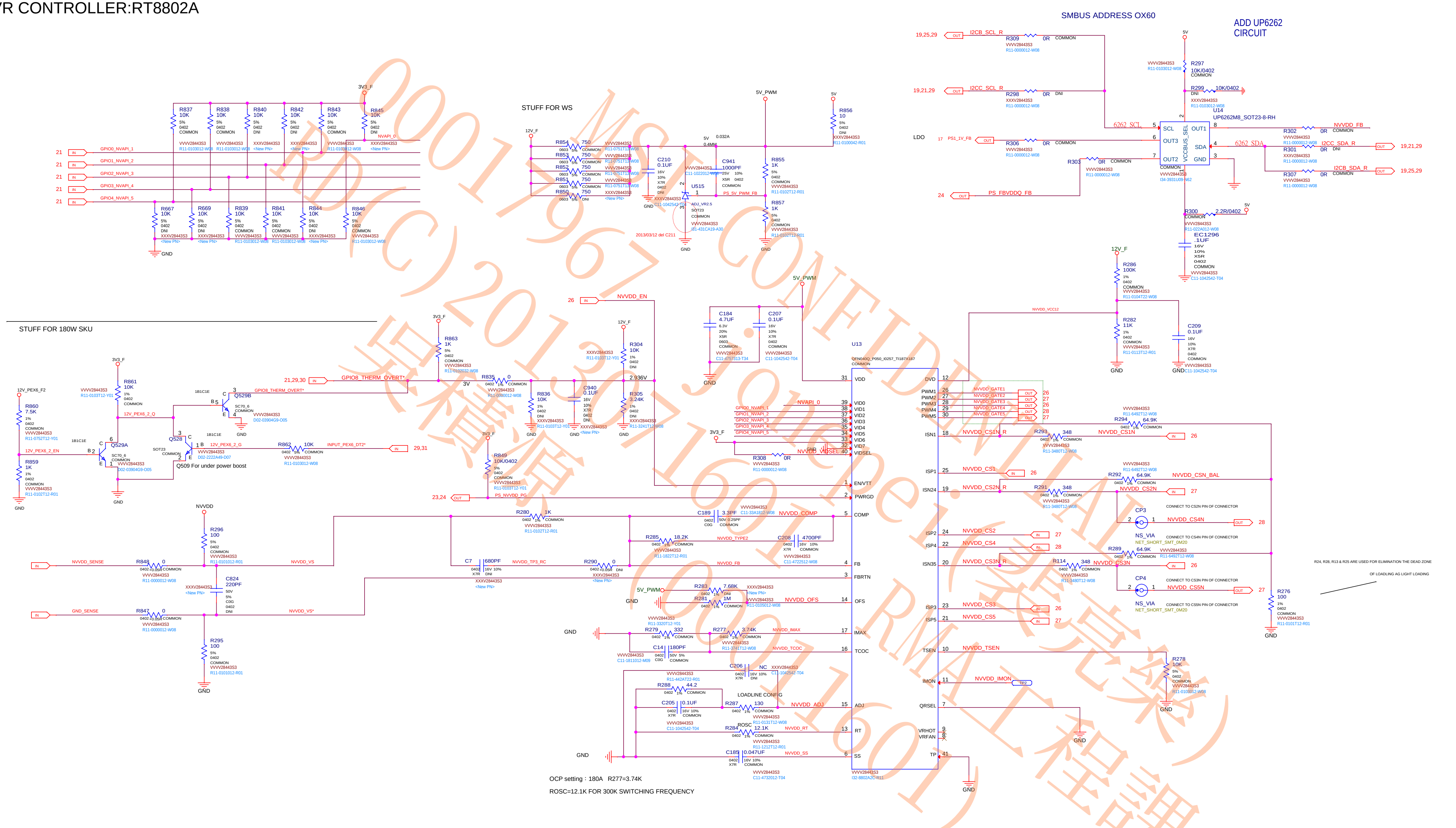
Page23: PS: 5V, PEX_VDD



Page24: PS: FBVDD/Q



Page25: POWER SUPPLY: NVVDD Controller
VR CONTROLLER:RT8802A



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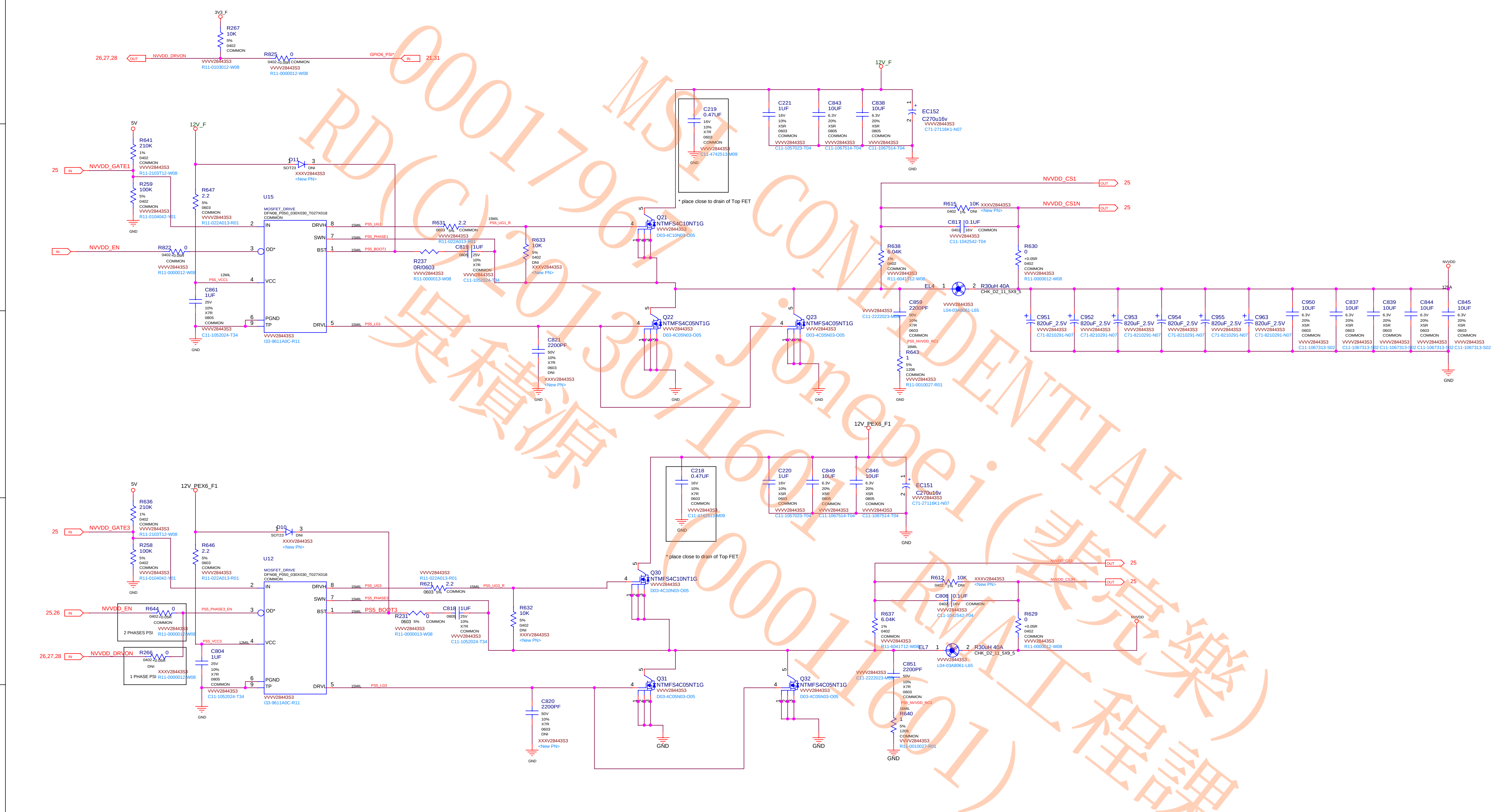
Page26: PS: NVVDD Phase 1 & 3



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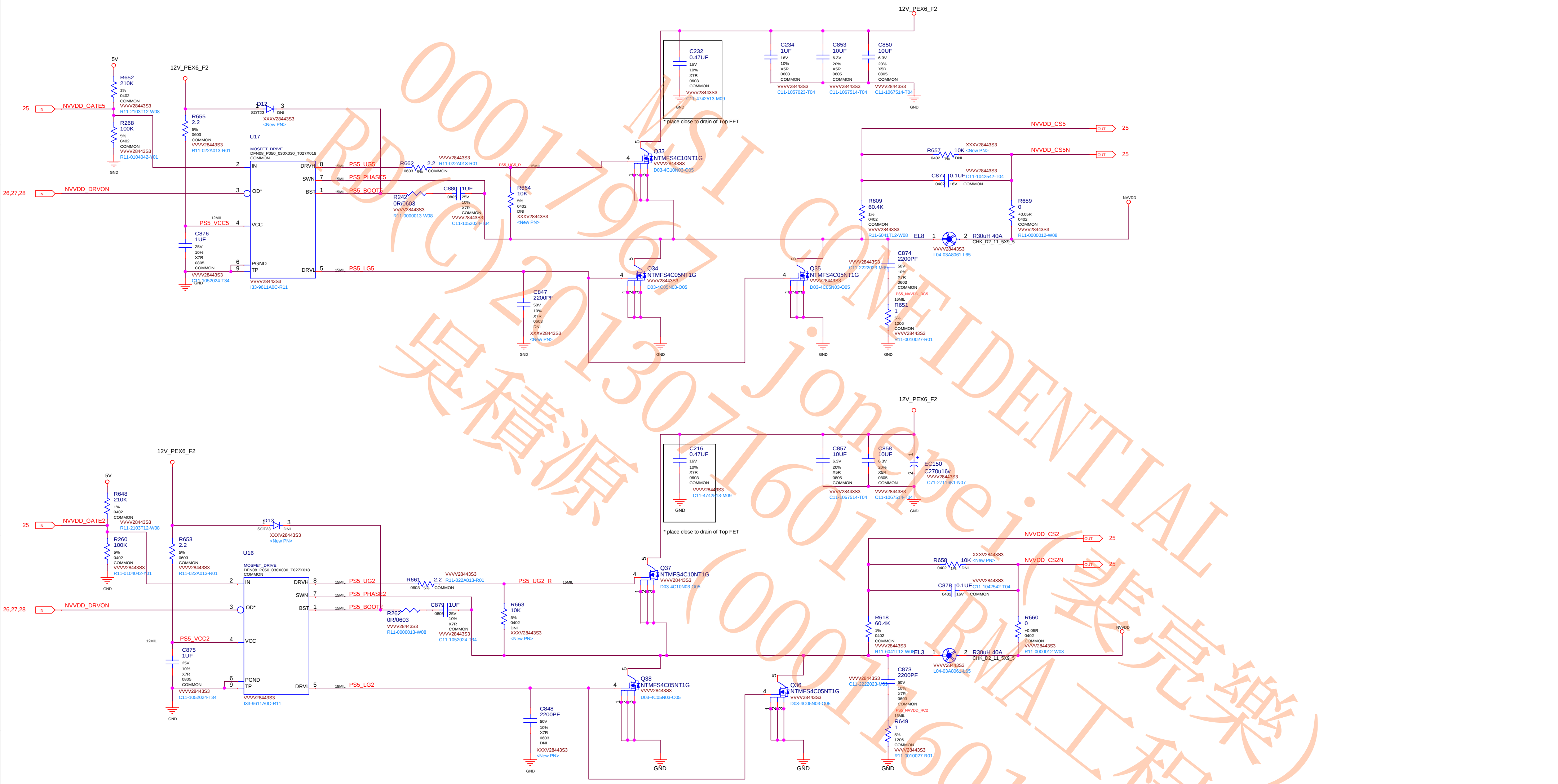
Page27: PS: NVVDD Phase 2 & 5



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Size: Custom	Document Description: PS: NVVDD Phase 2 & 5 — Rev 8.1
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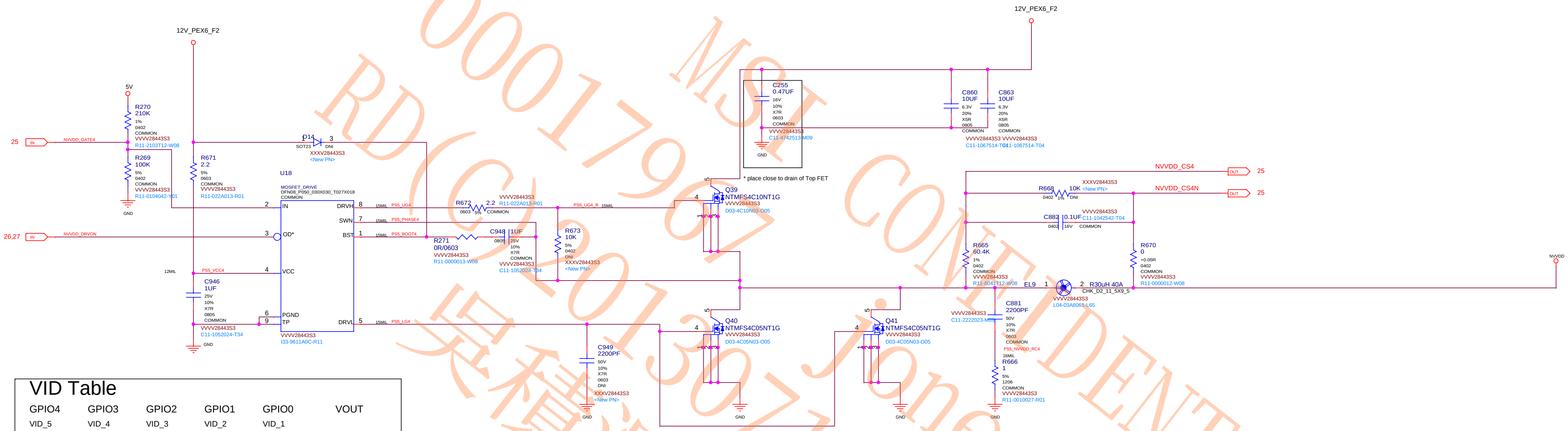
Page29: PS: NVVDD Phase 4



VID Table

GPIO4 VID_5	GPIO3 VID_4	GPIO2 VID_3	GPIO1 VID_2	GPIO0 VID_1	VOUT
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

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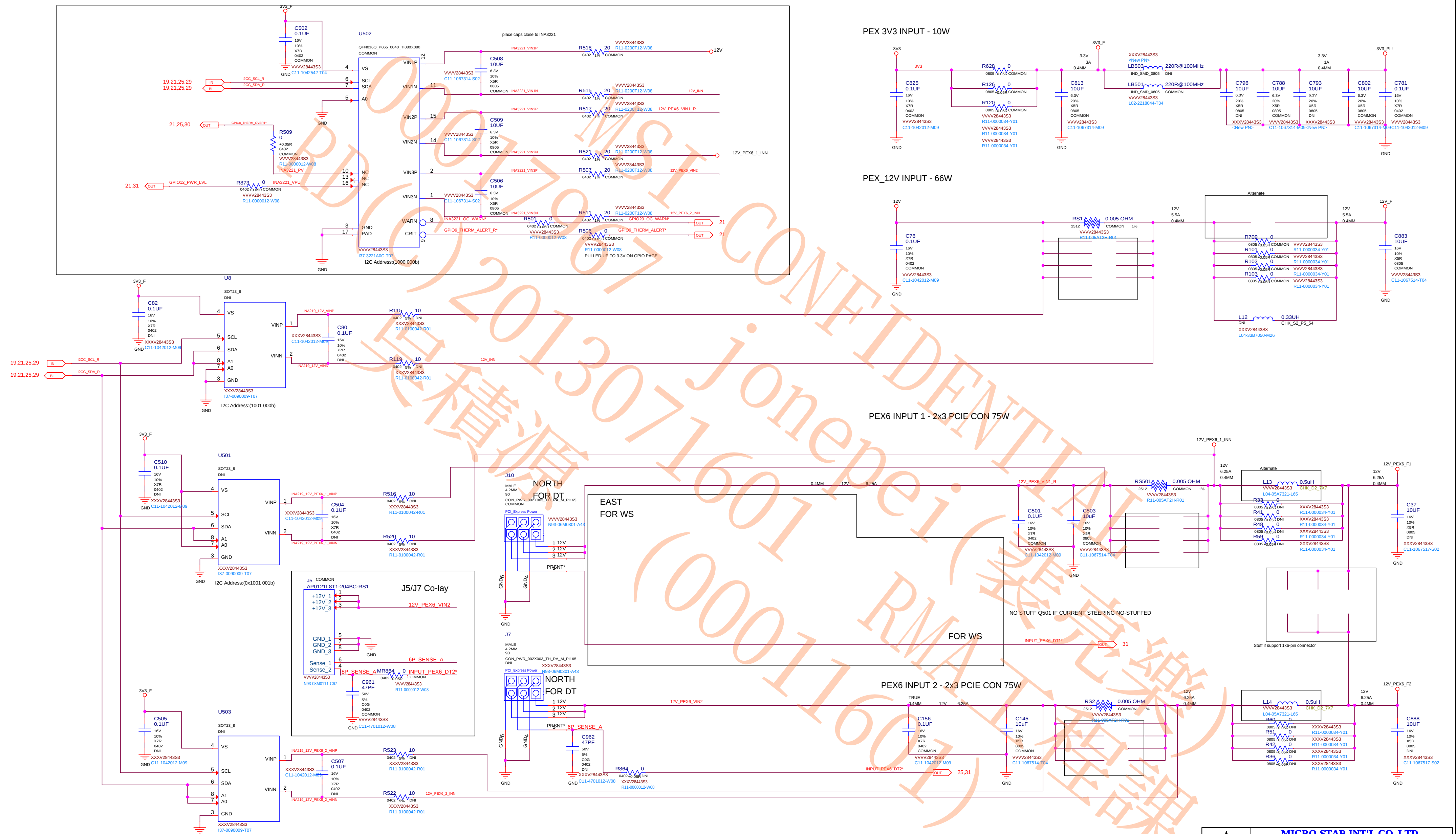
Page28: PS: Inputs, Filtering, and Monitoring



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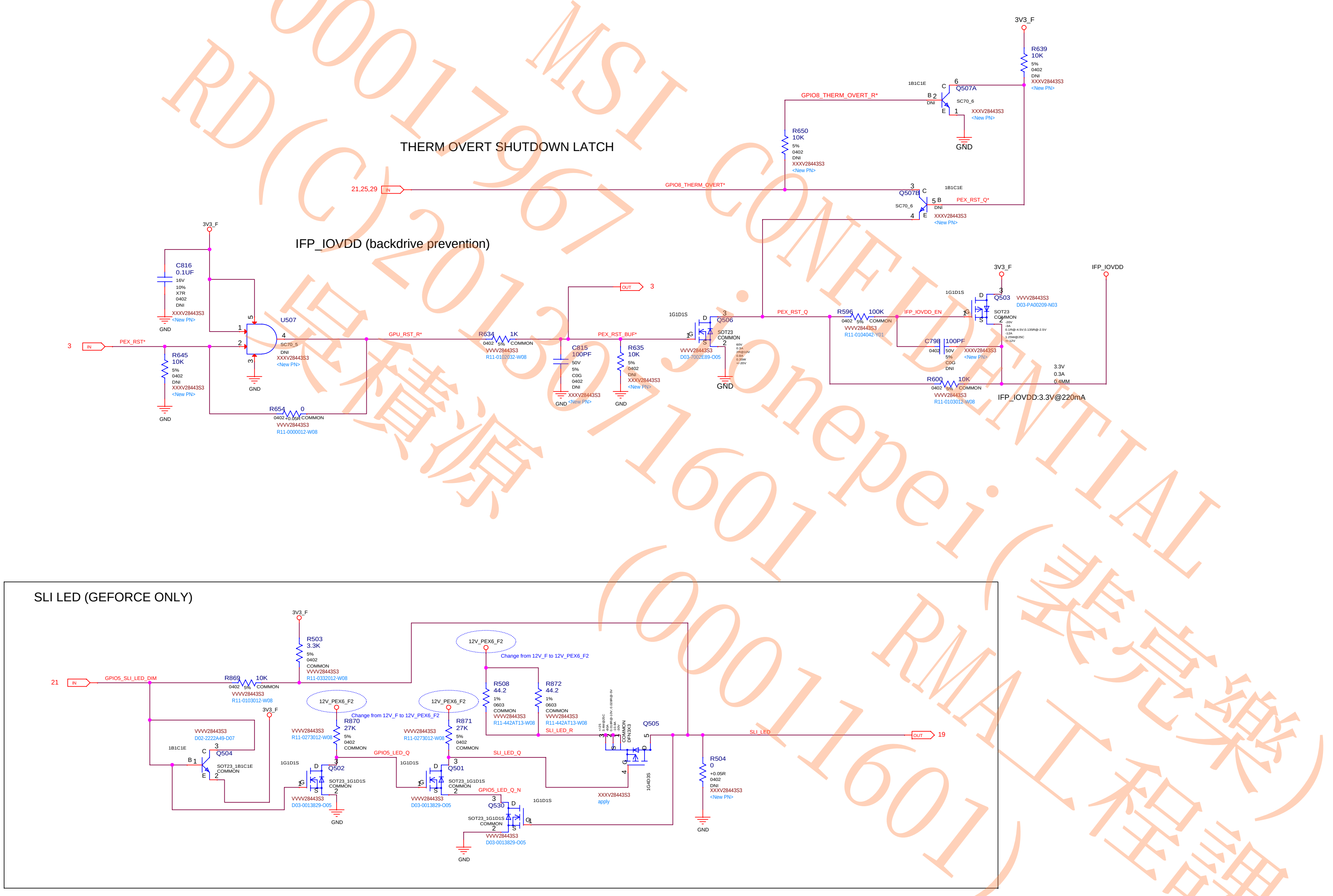
Page29: PS: Thermal Shutdown& Light SLI DRIVER



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Size: Custom	Document Description: Thermal Shutdown& Light SLI	Rev: 8.1
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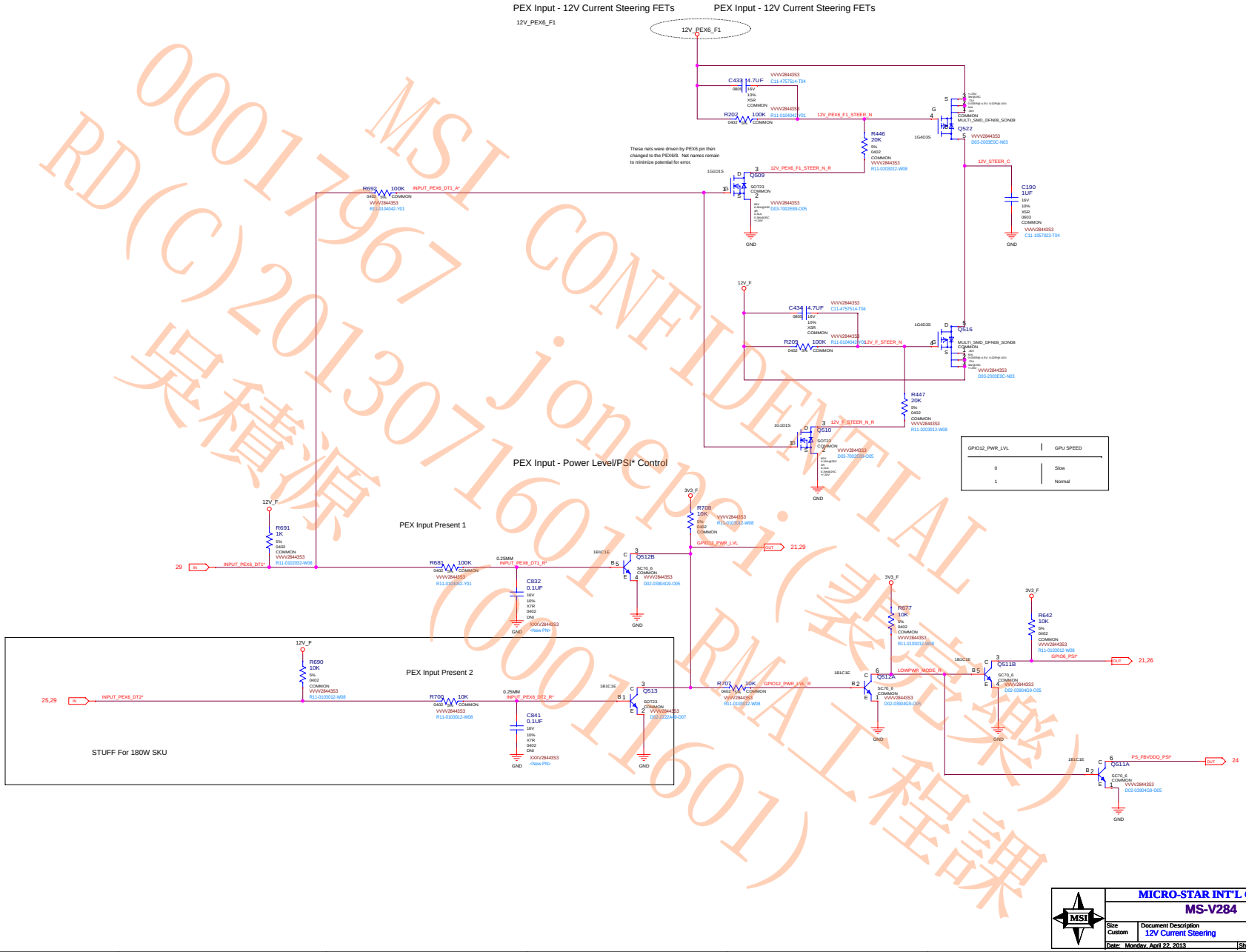
Page30: PS: 12V Current Steering



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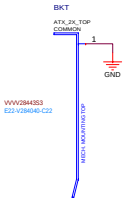
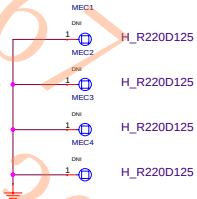
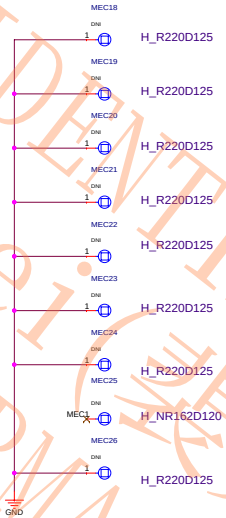
Brackets:



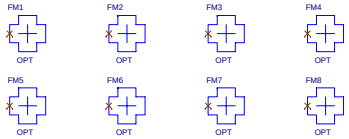
GPU Stiffener:



MOUNTING HOLES FOR HS:



optical cross point



Top & bottom each layer set 4 points