

PG160-B02

8GB GDDR6, 256b, X16

Tall DVI-D + USBC/DP + DP + HDMI/DP + DP

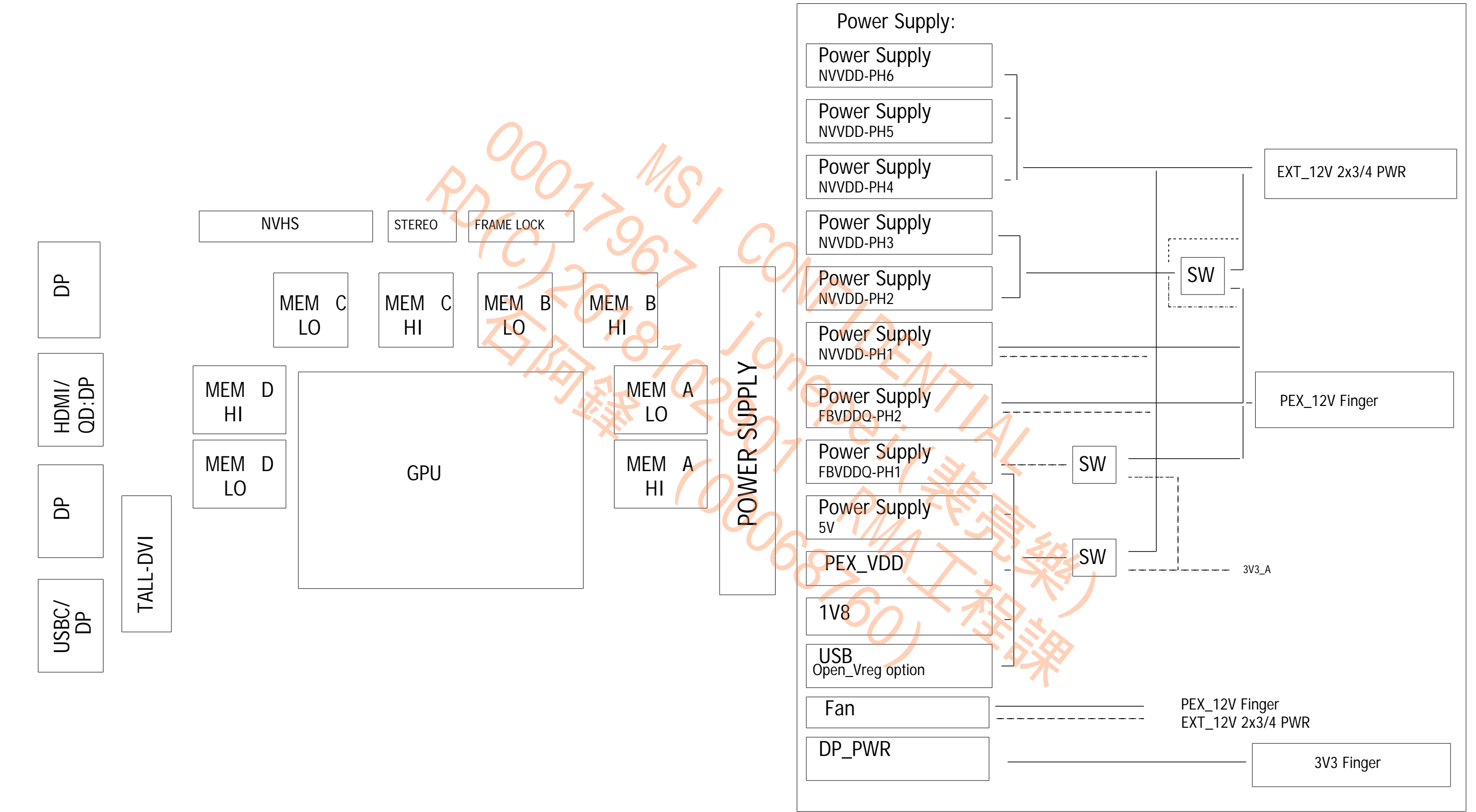
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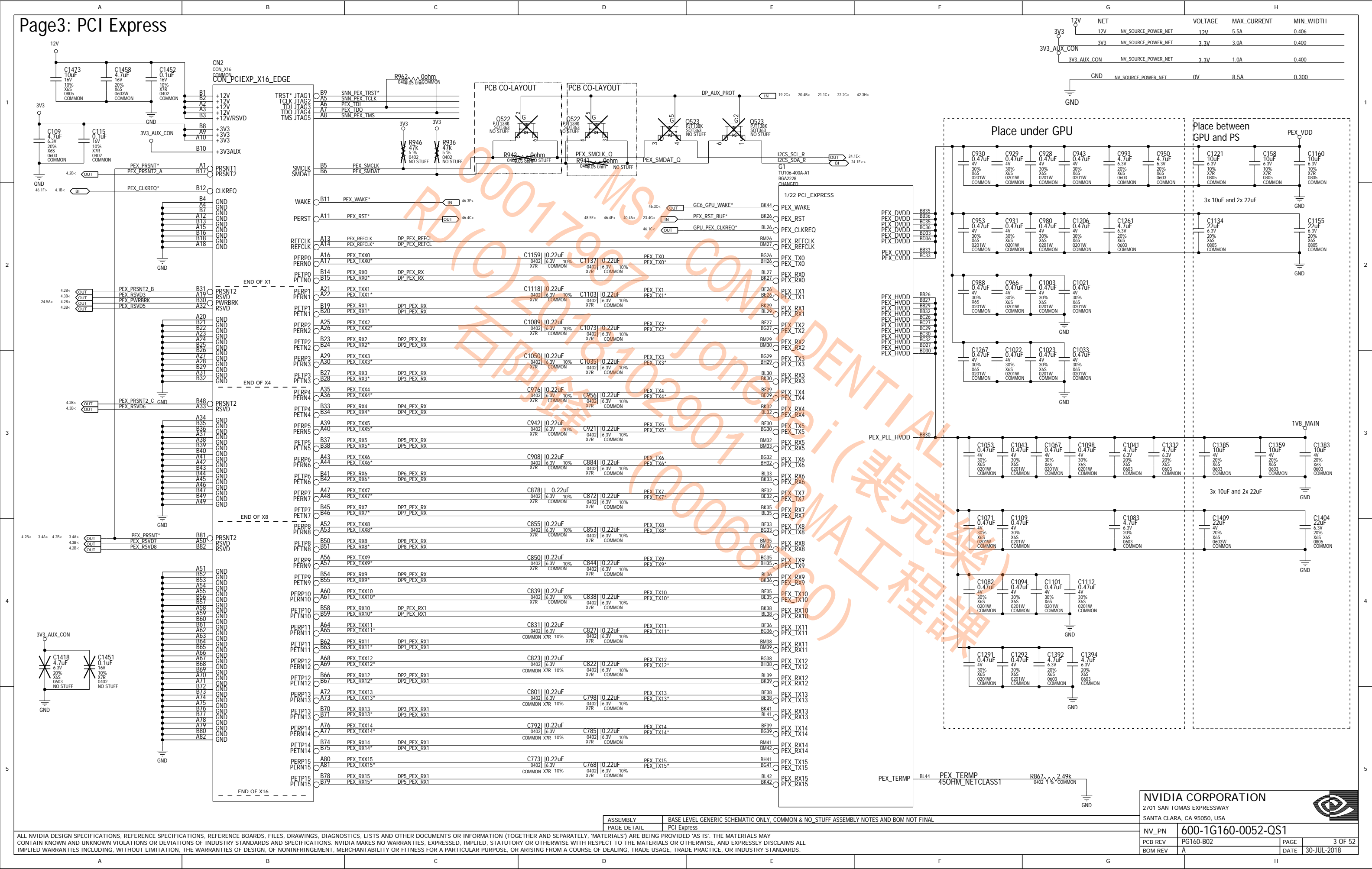
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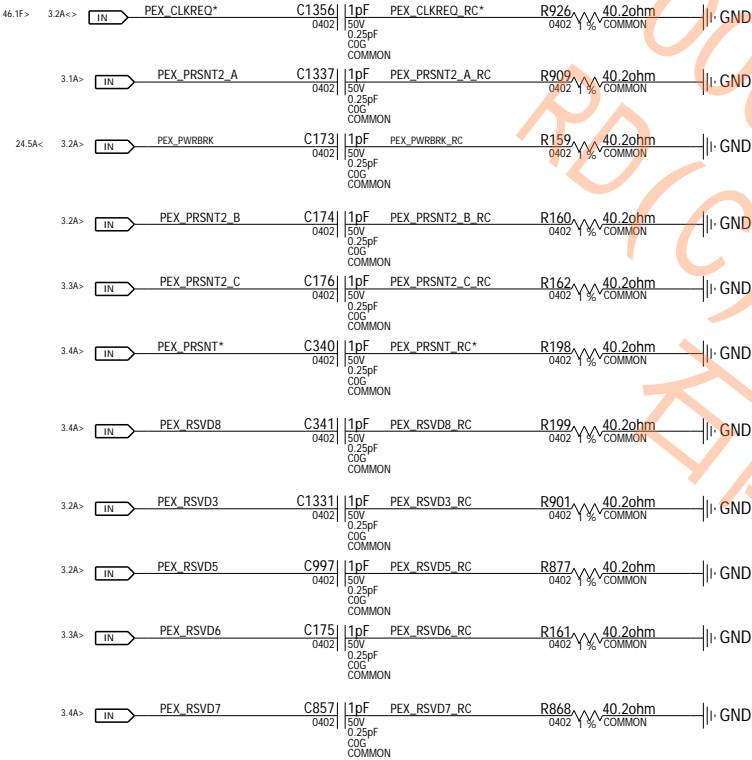


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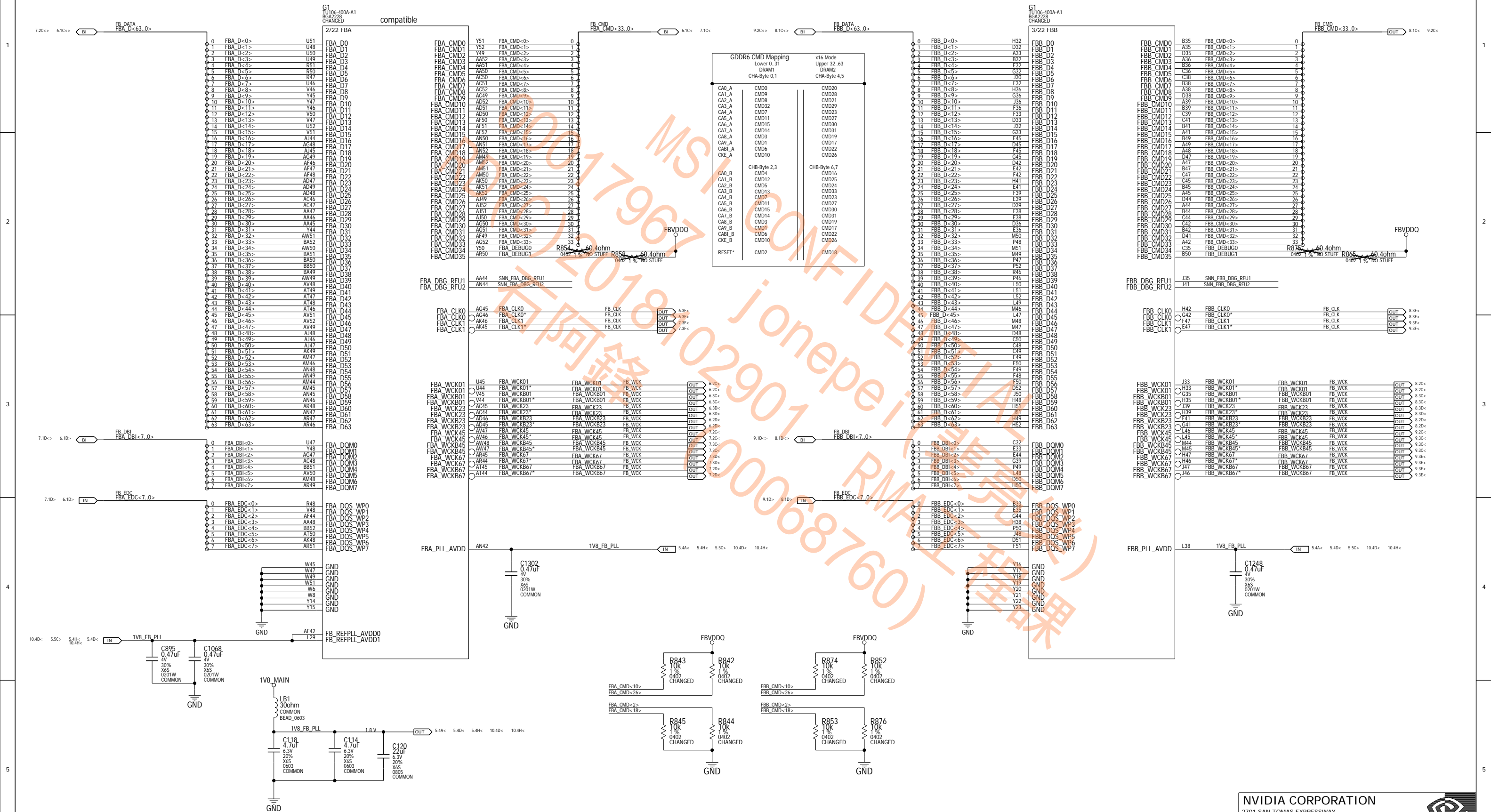
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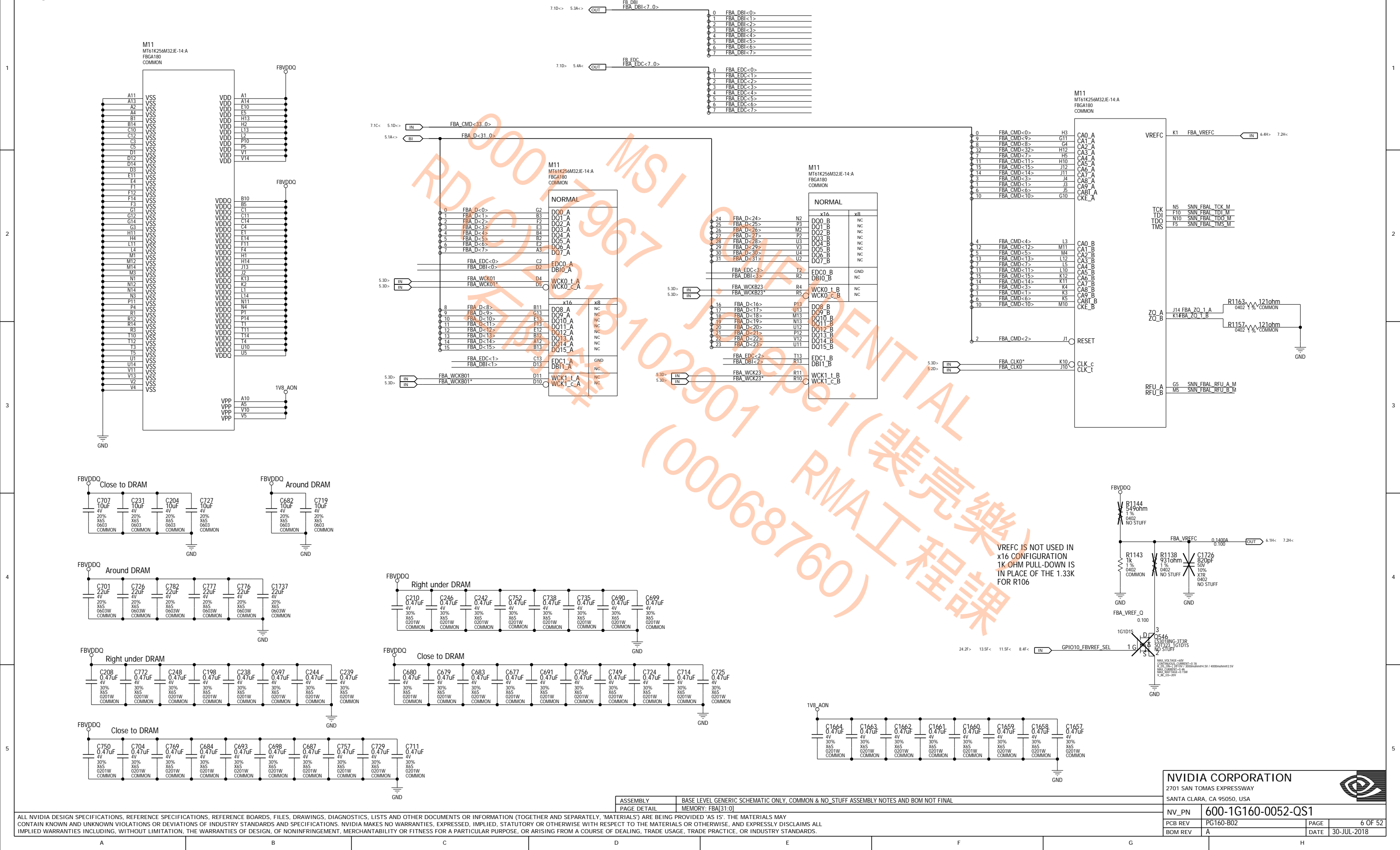
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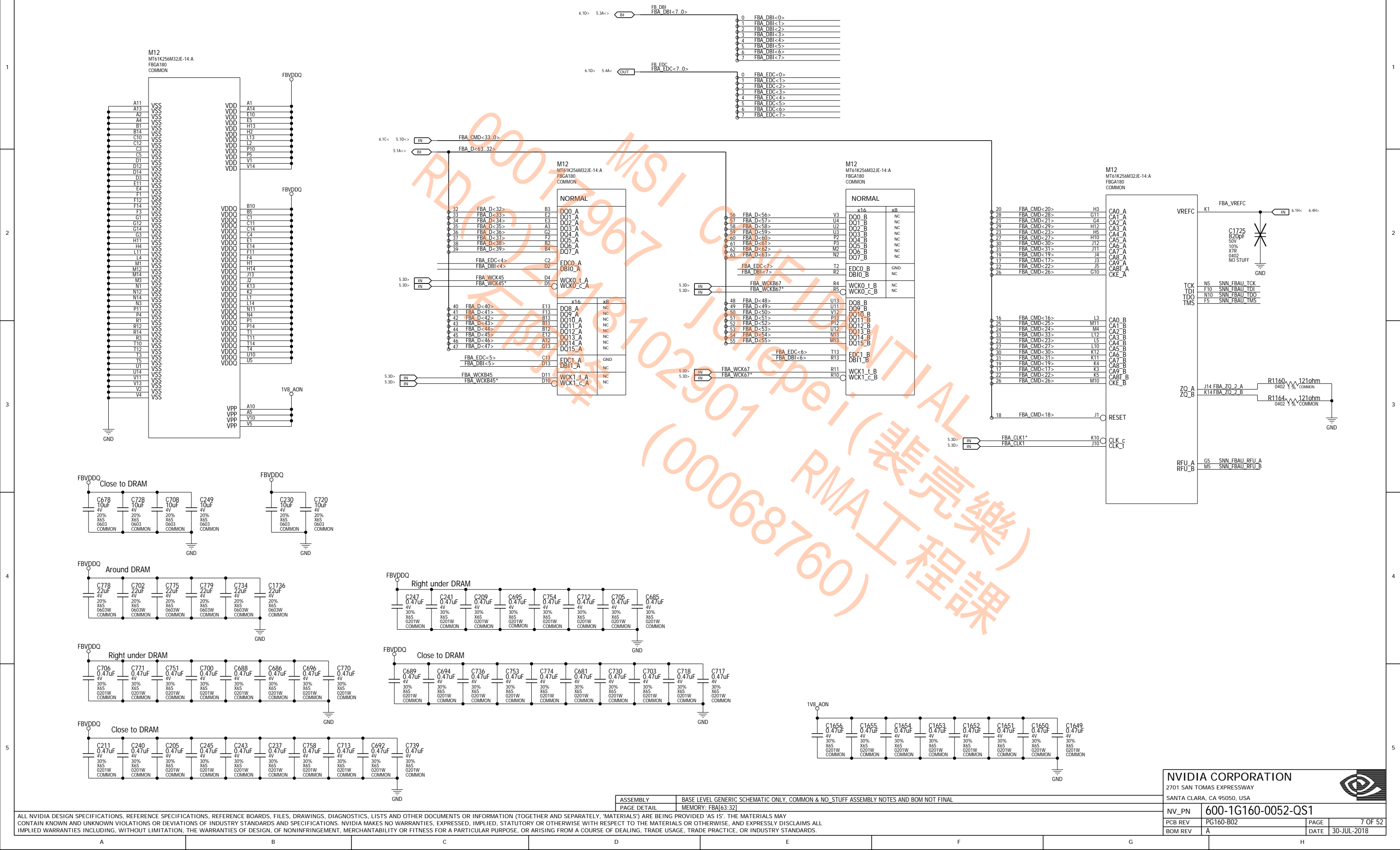


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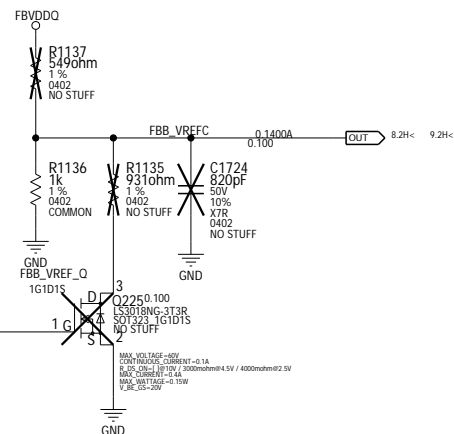
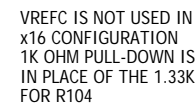
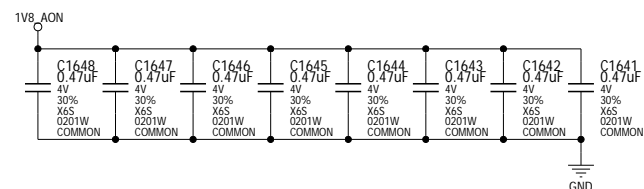
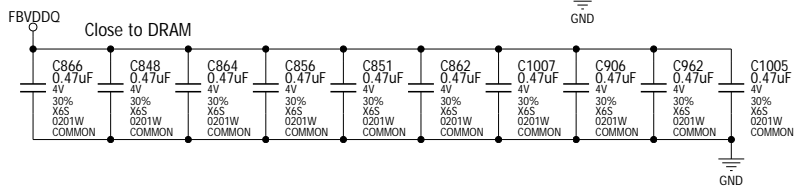
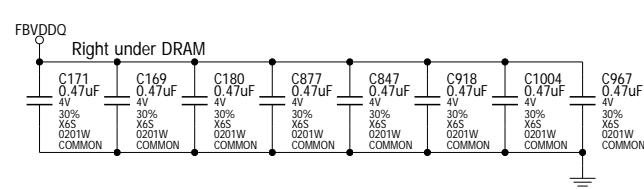
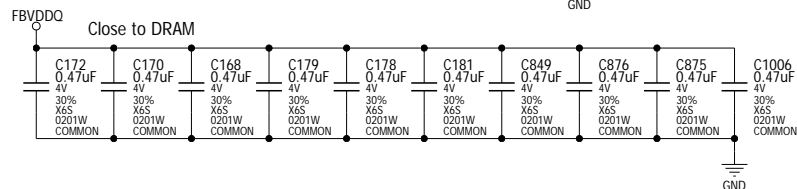
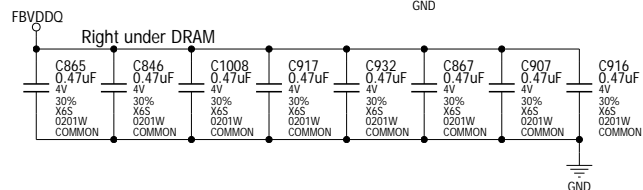
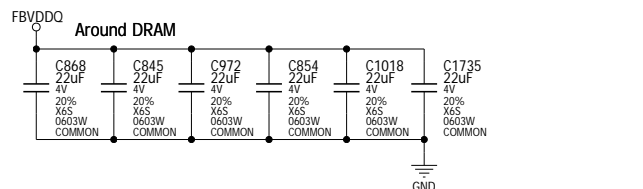
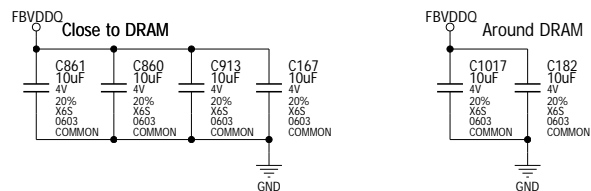
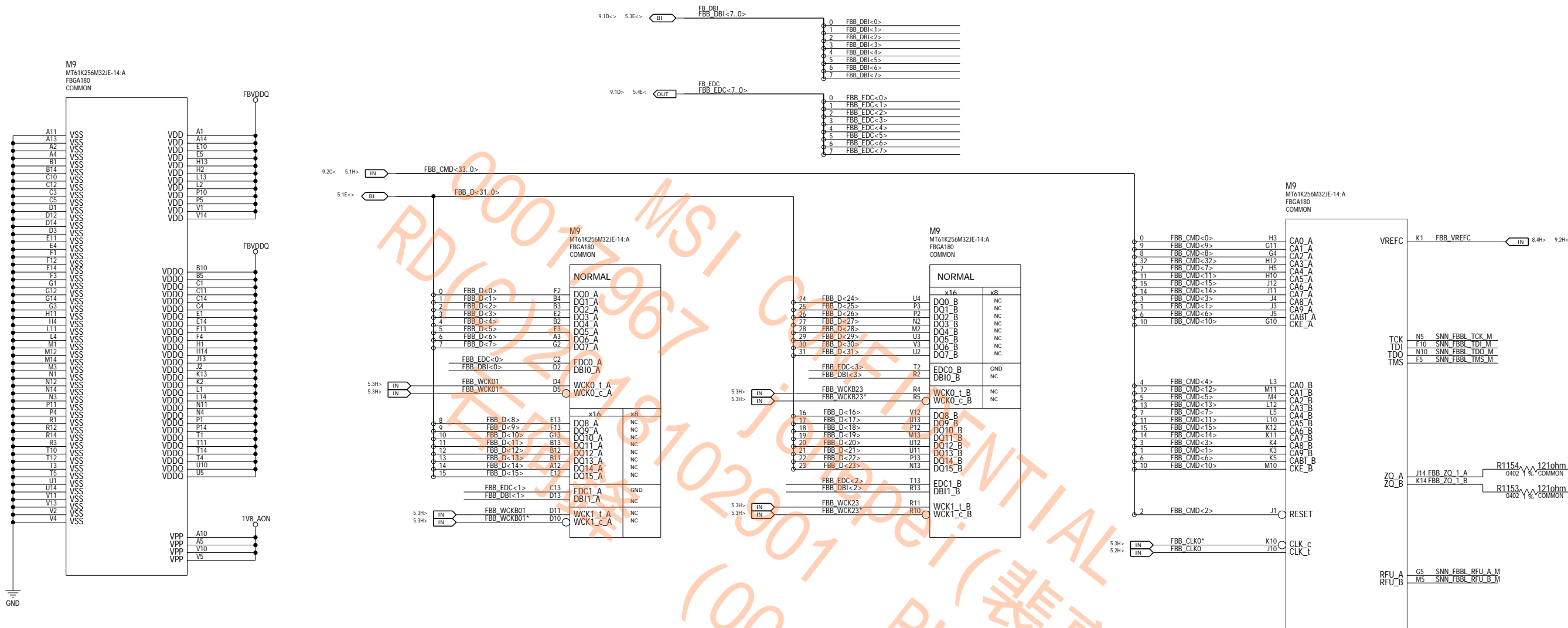




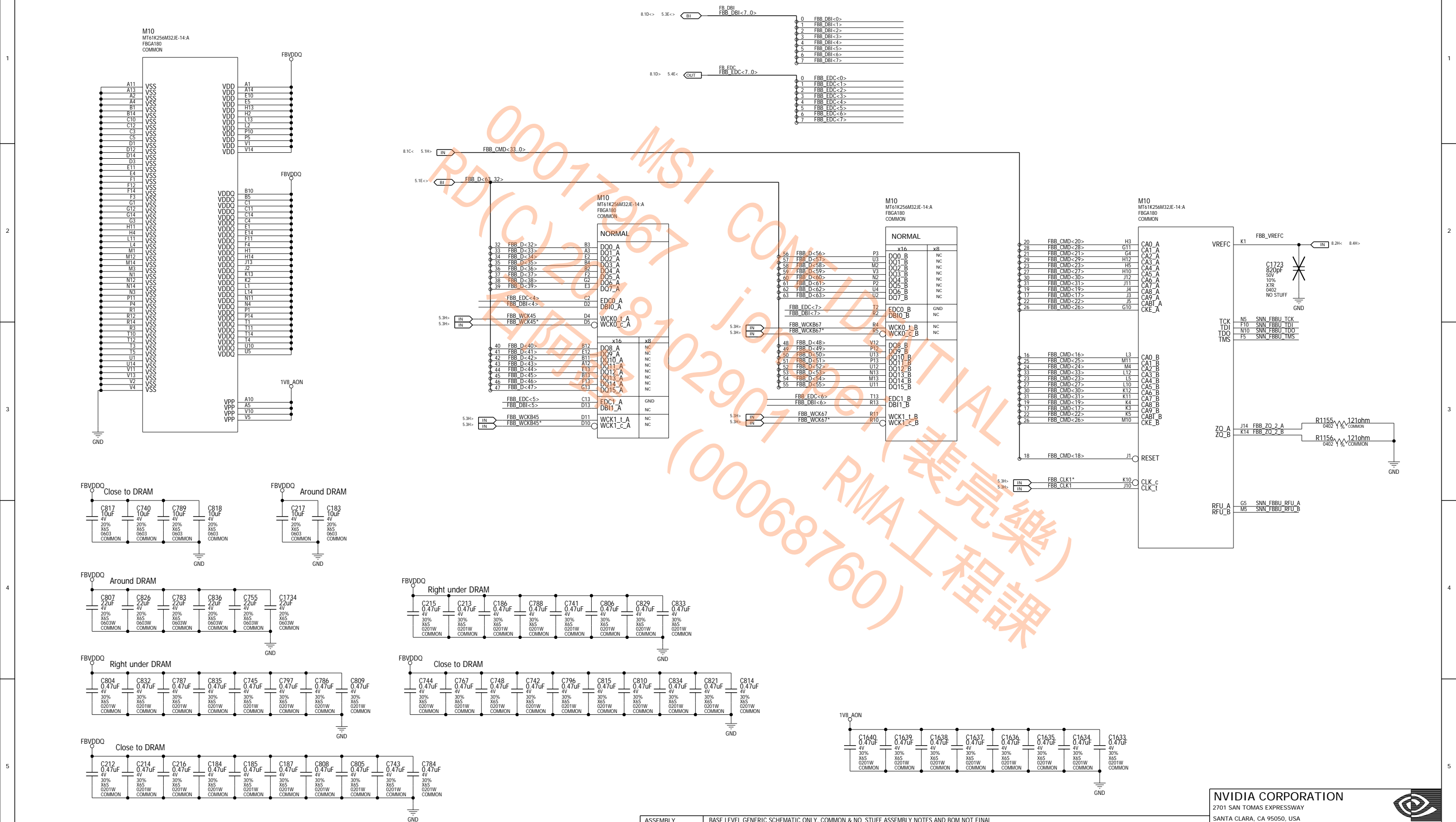









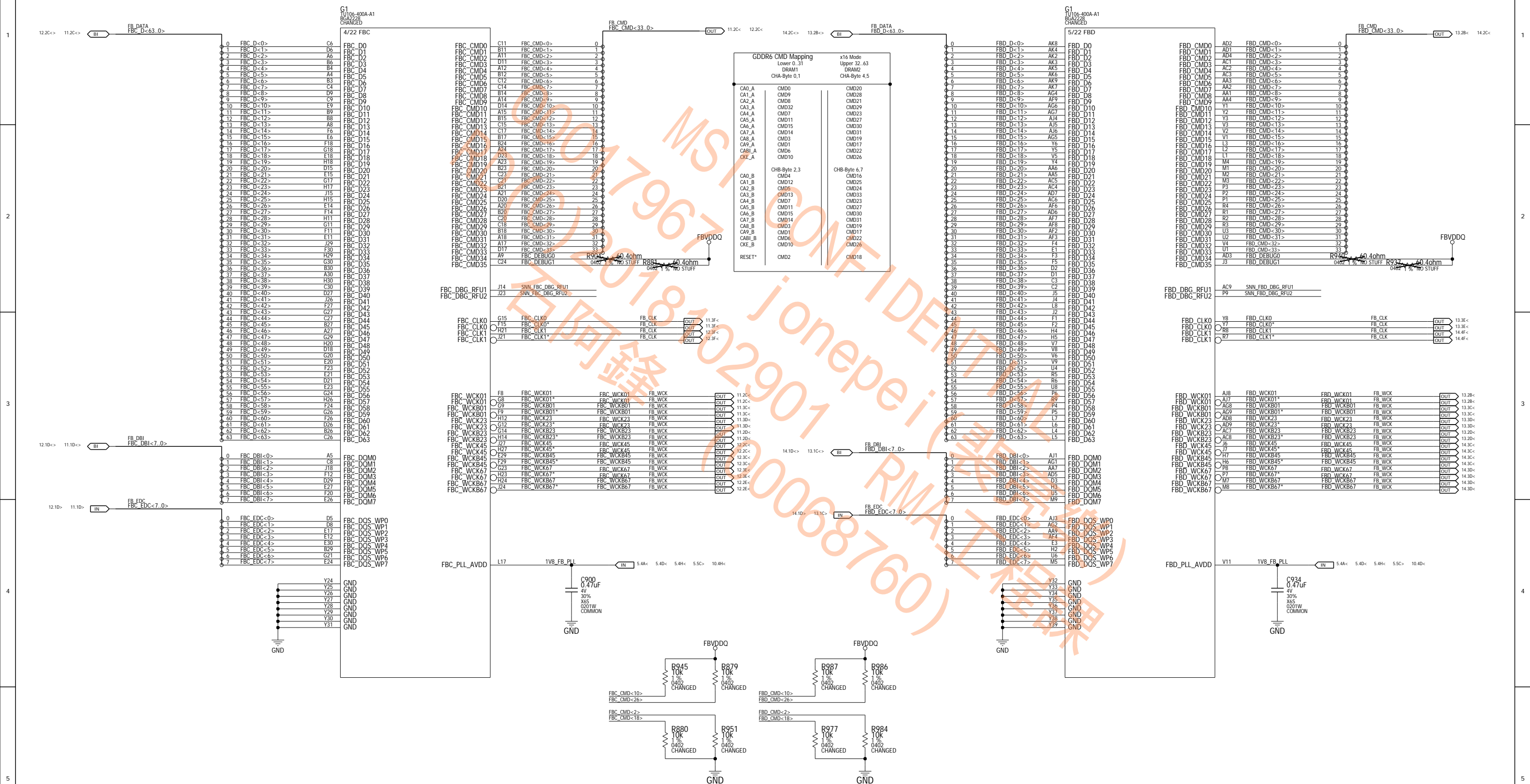


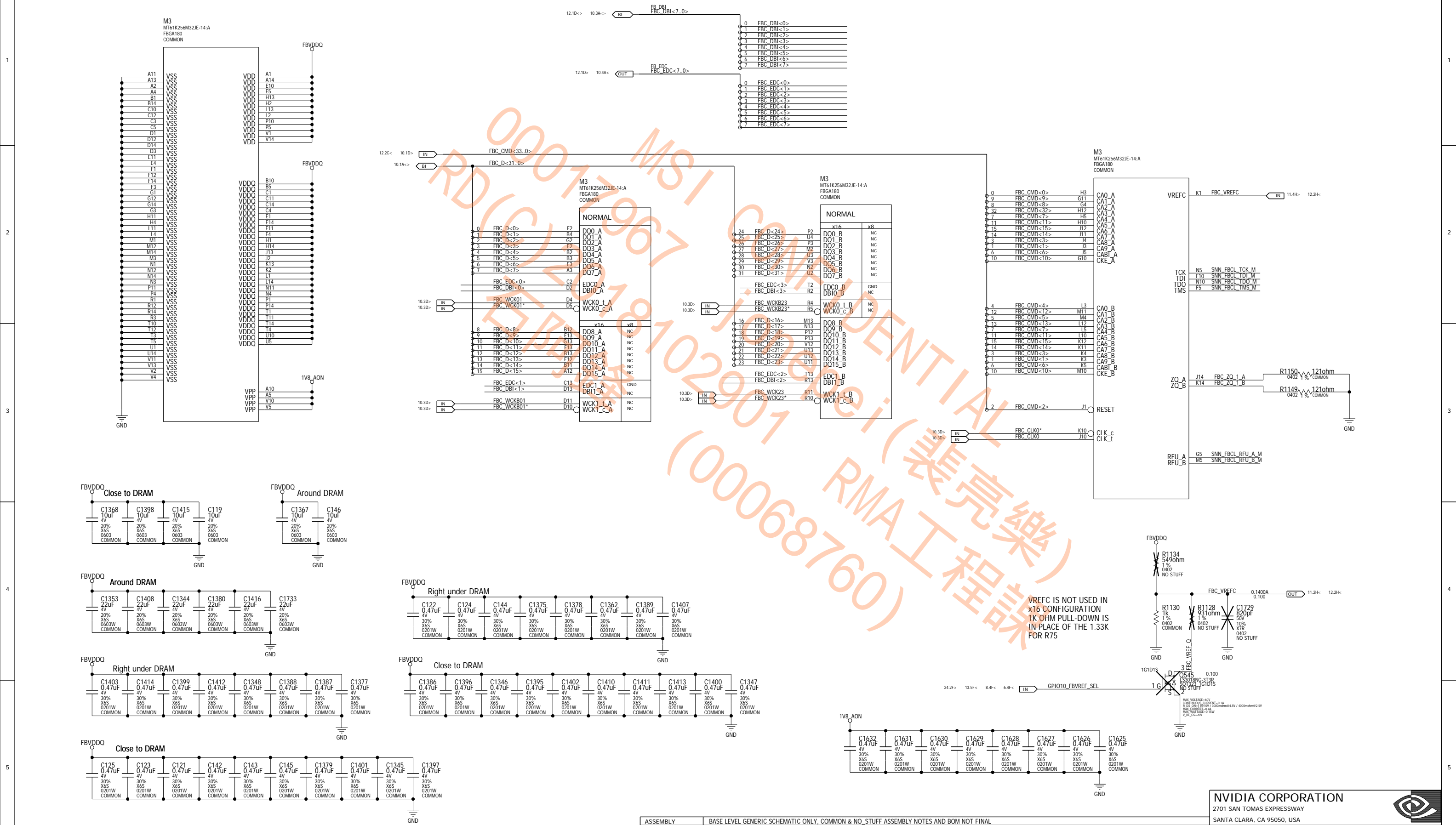


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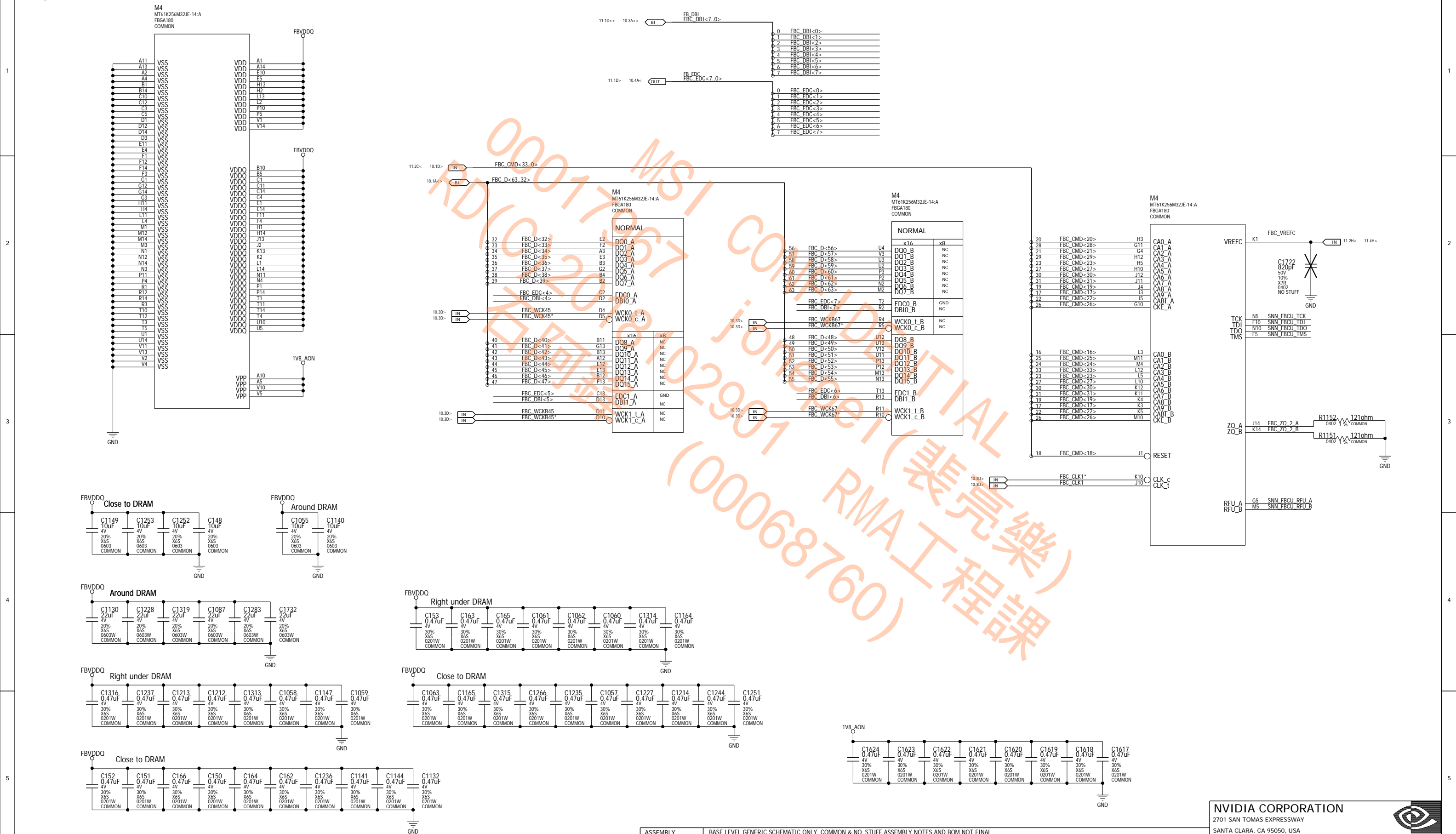
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<b>NV_PN</b>		<b>600-1G160-0052-QS1</b>		
<b>PCB REV</b>	<b>PG160-B02</b>	<b>PAGE</b>	<b>9 OF 52</b>	
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## Page12: MEMORY: FBC Partition 63..32

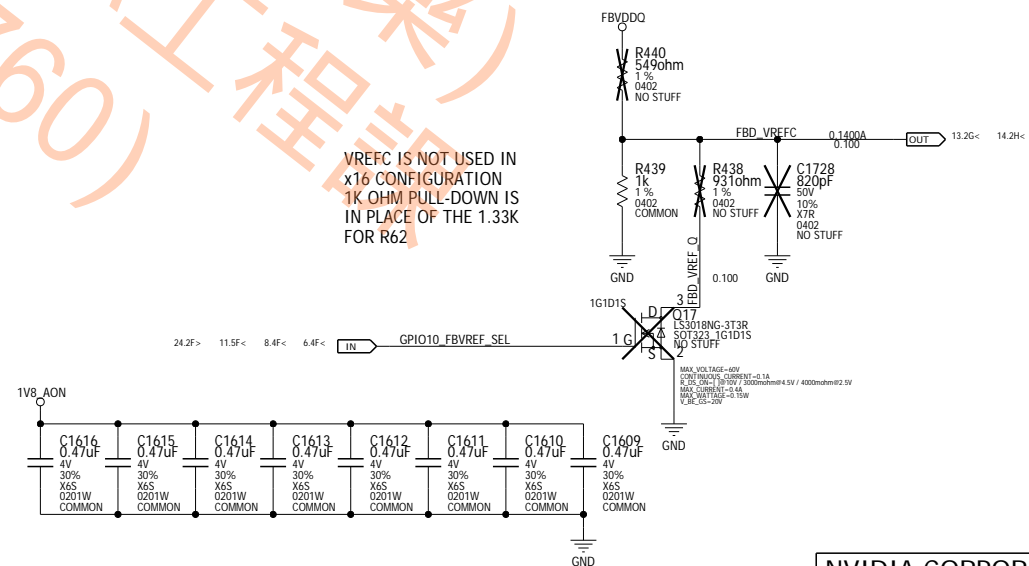
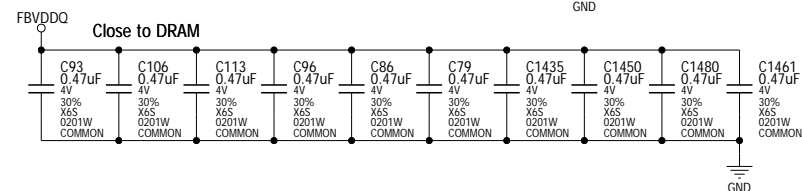
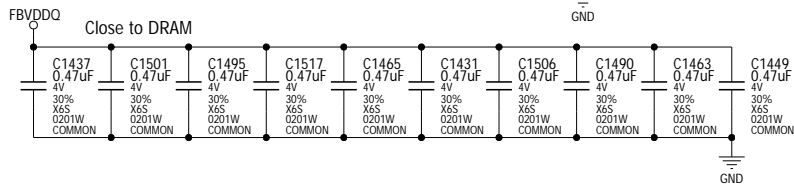
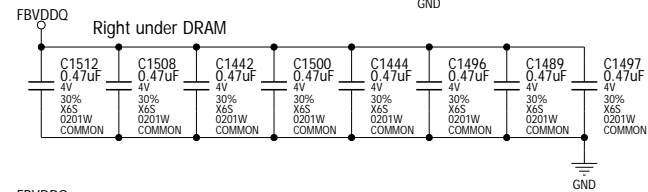
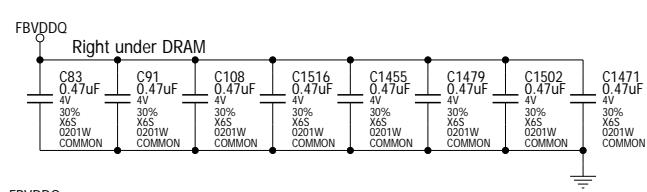
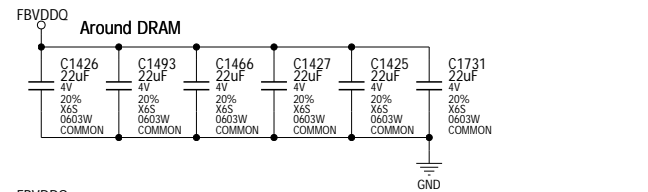
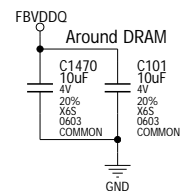
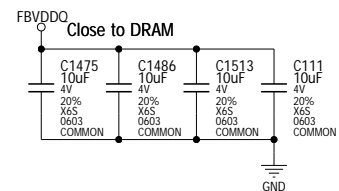
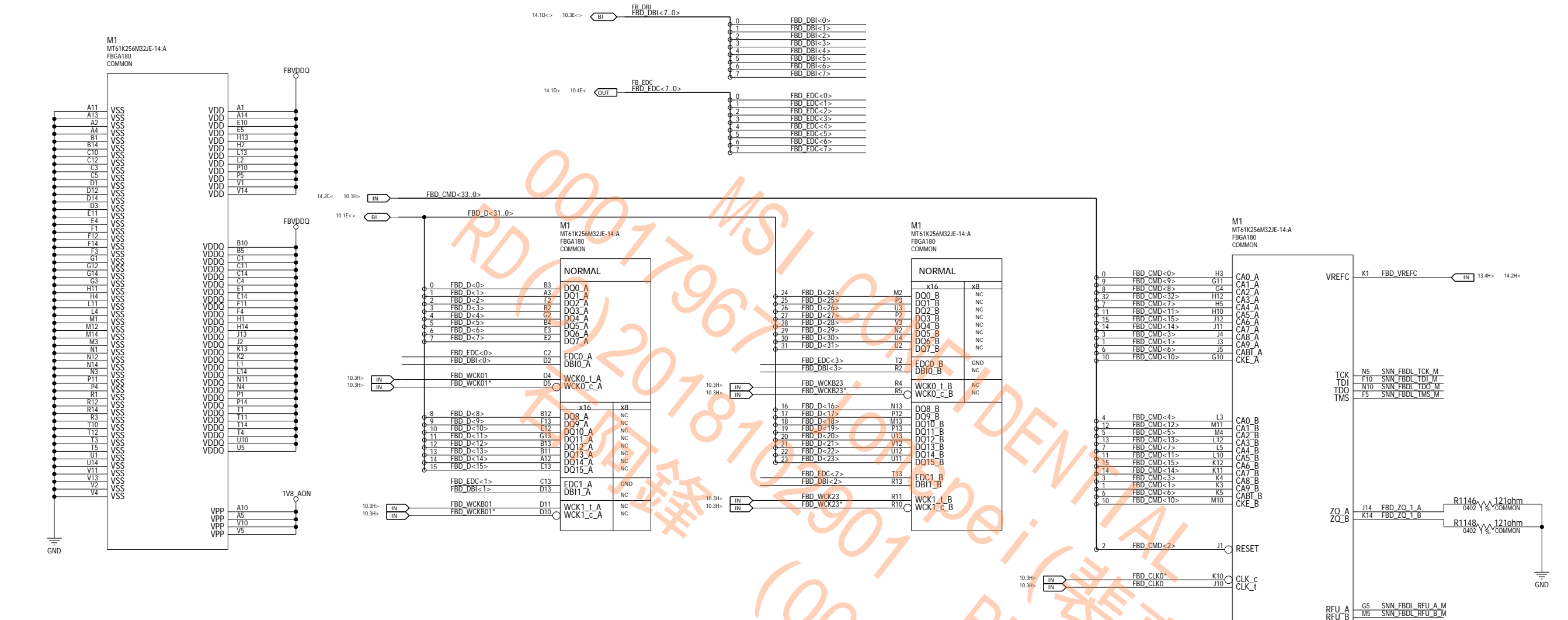


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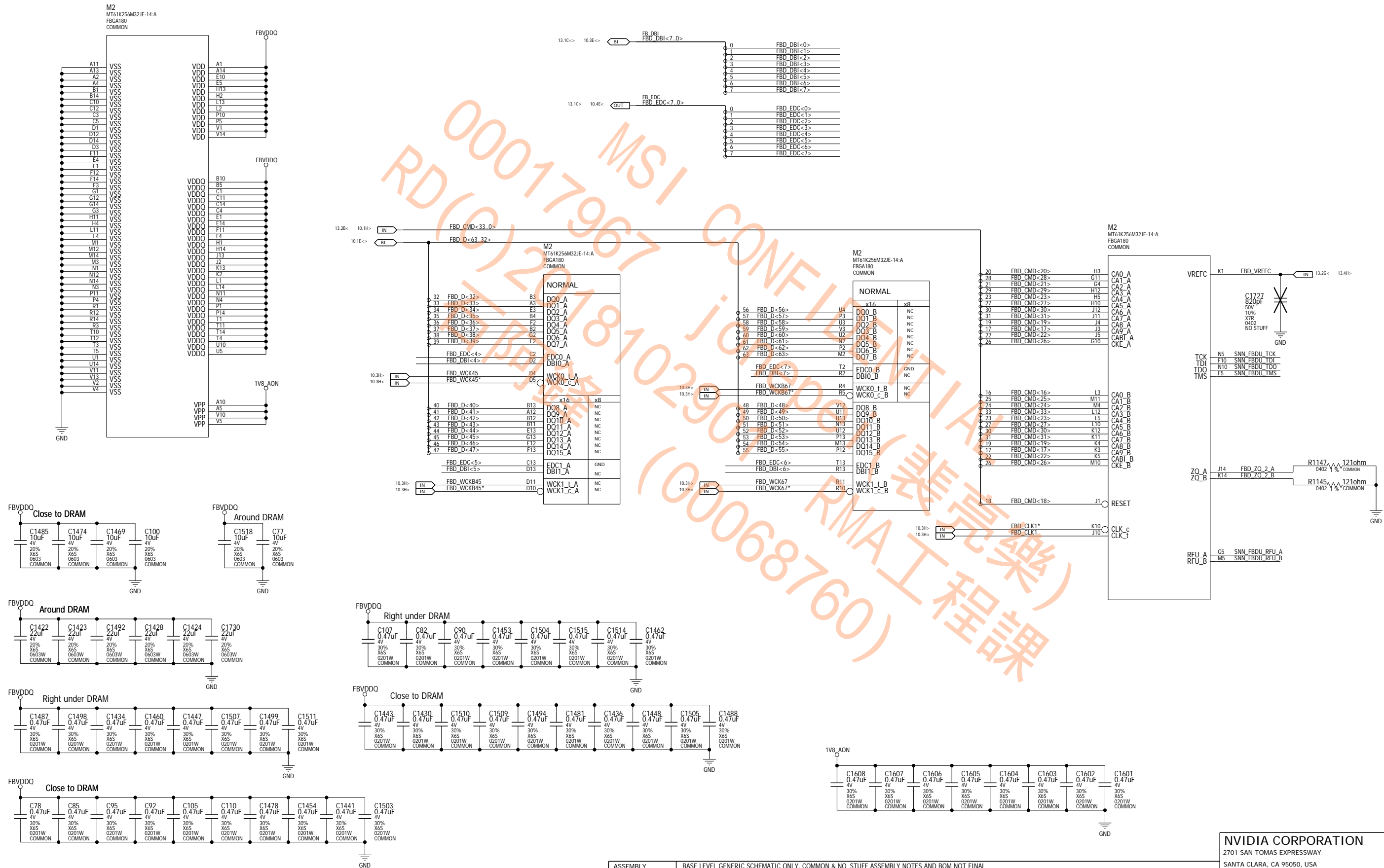
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<b>PCB REV</b>	<b>PG160-B02</b>	<b>PAGE</b>	<b>12 OF 52</b>	
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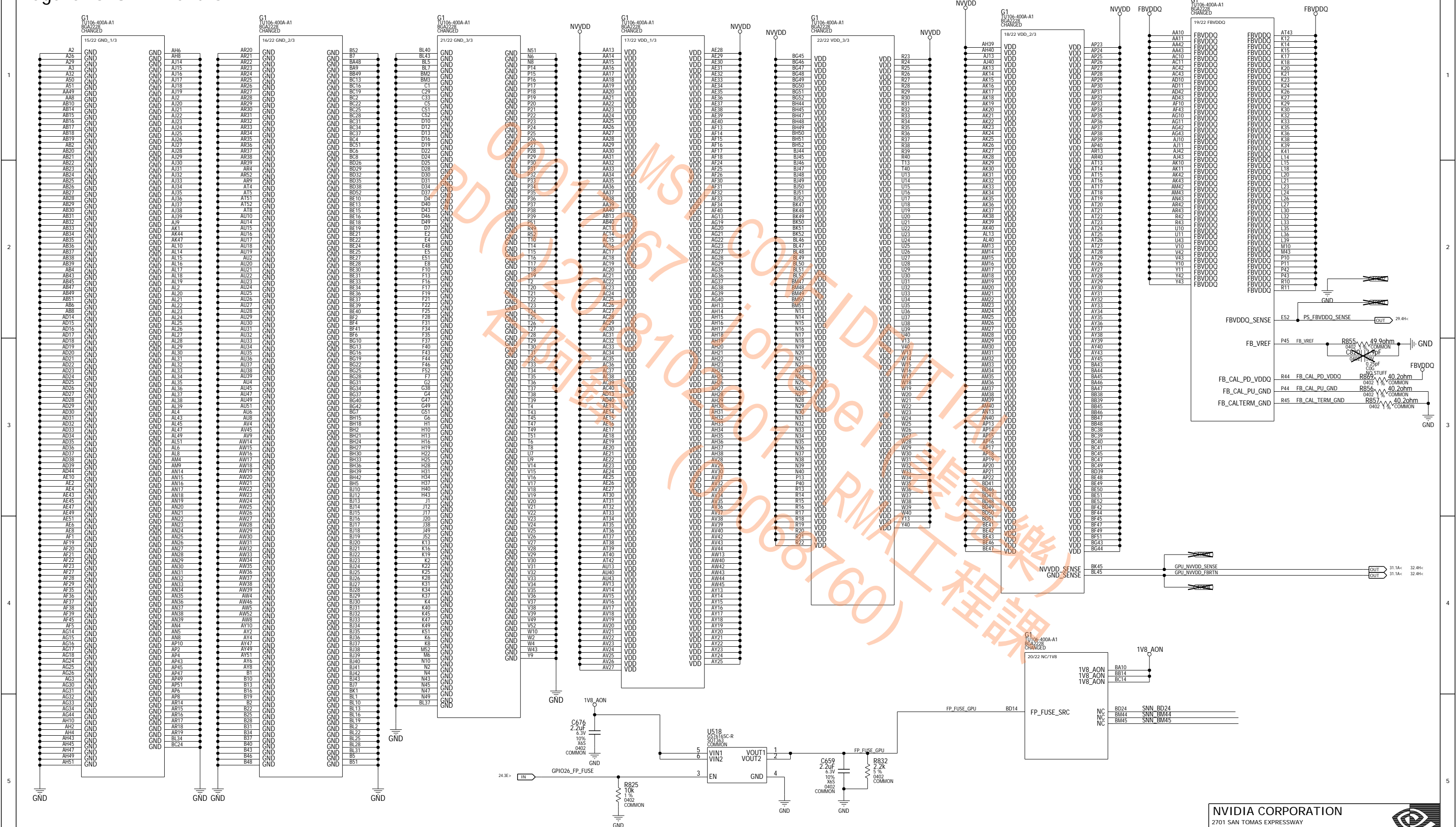


VREFC IS NOT USED IN  
x16 CONFIGURATION  
1K OHM PULL-DOWN IS  
IN PLACE OF THE 1.33K  
FOR R62

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## Page15: GPU PWR and GND



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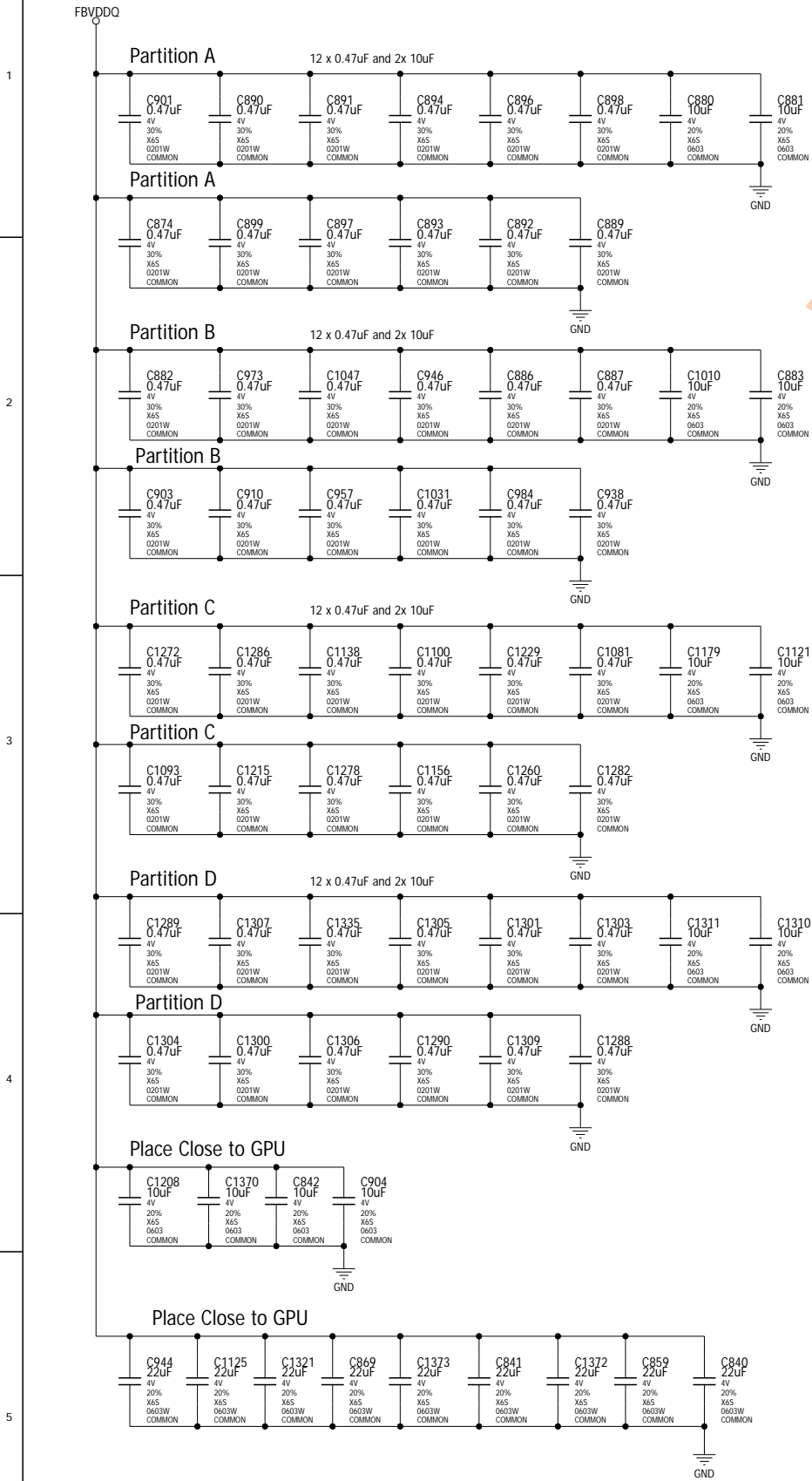
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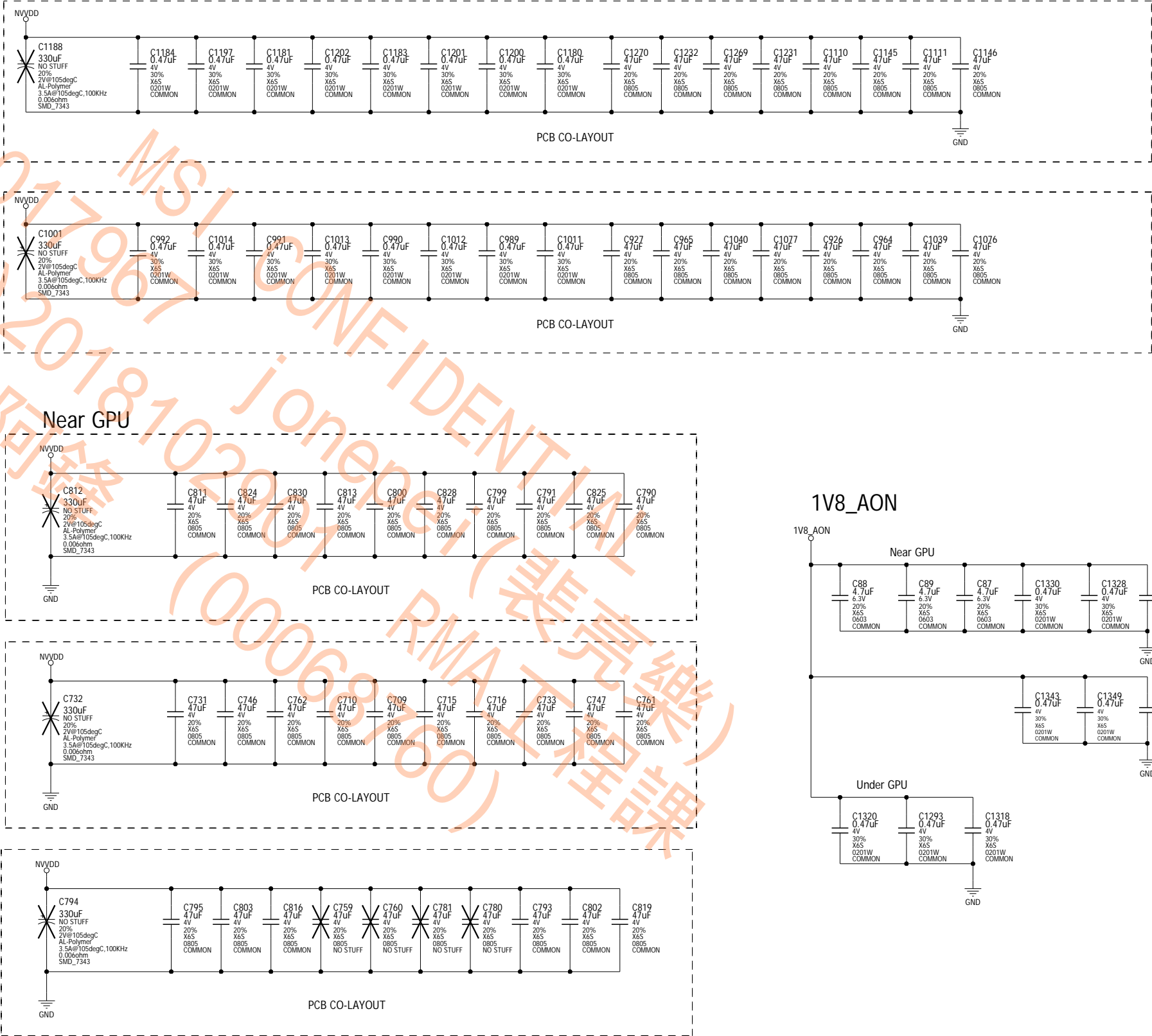
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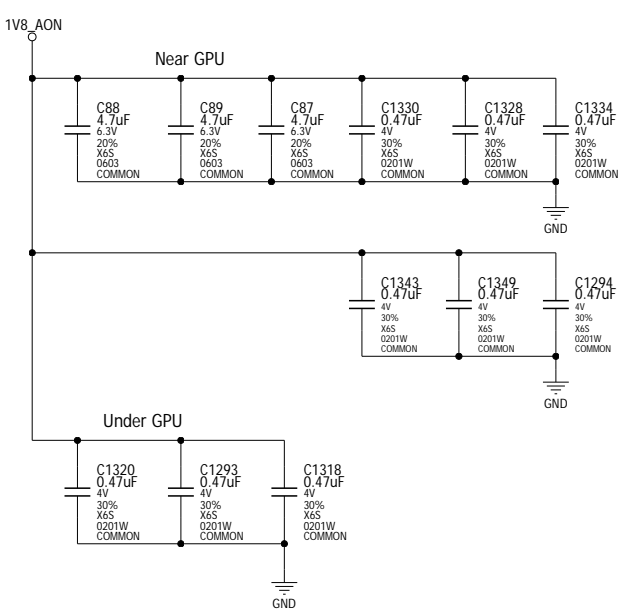
FBVDDQ



Under GPU



1V8\_AON



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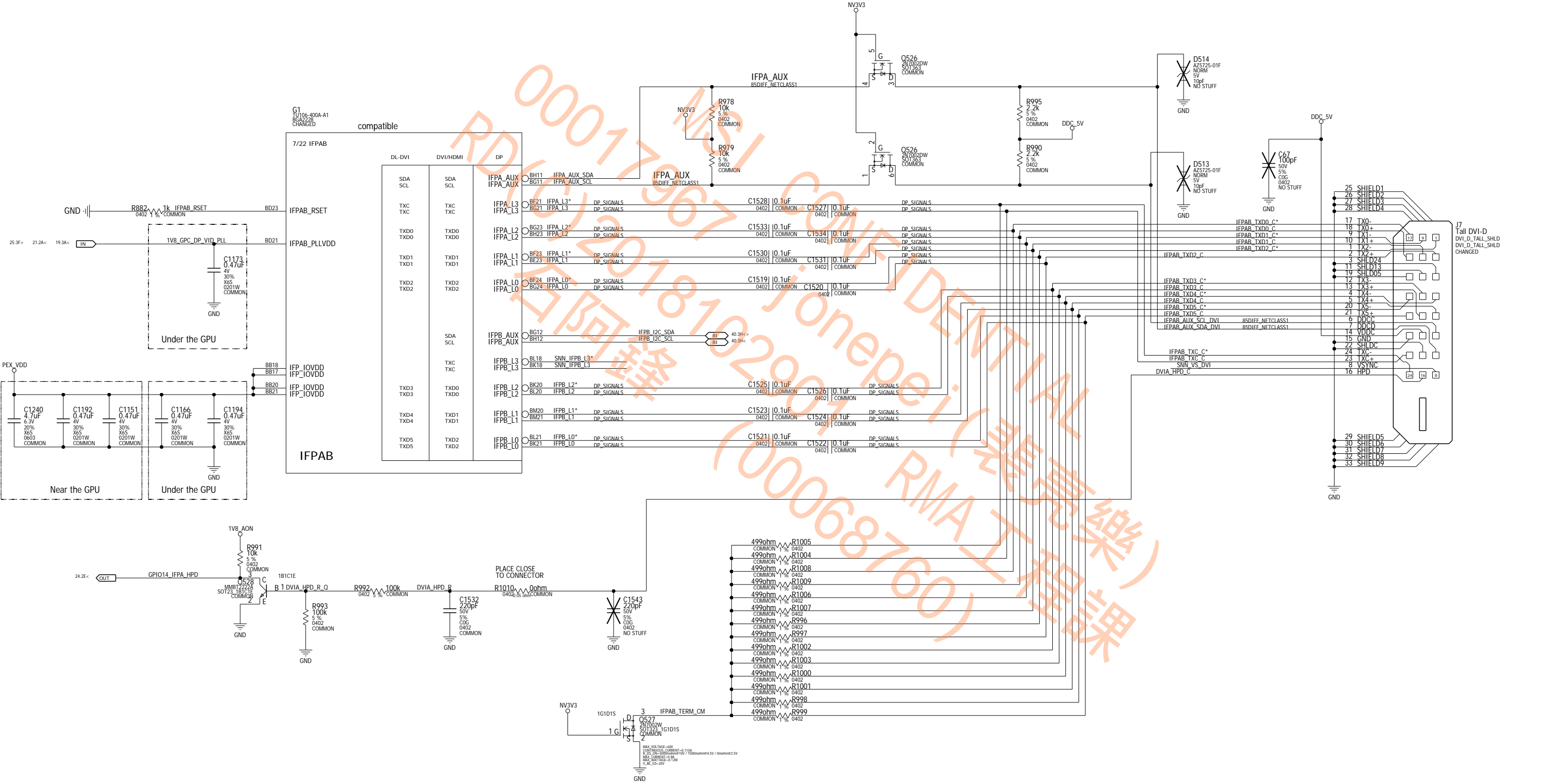


Page17: GPU Decoupling 2

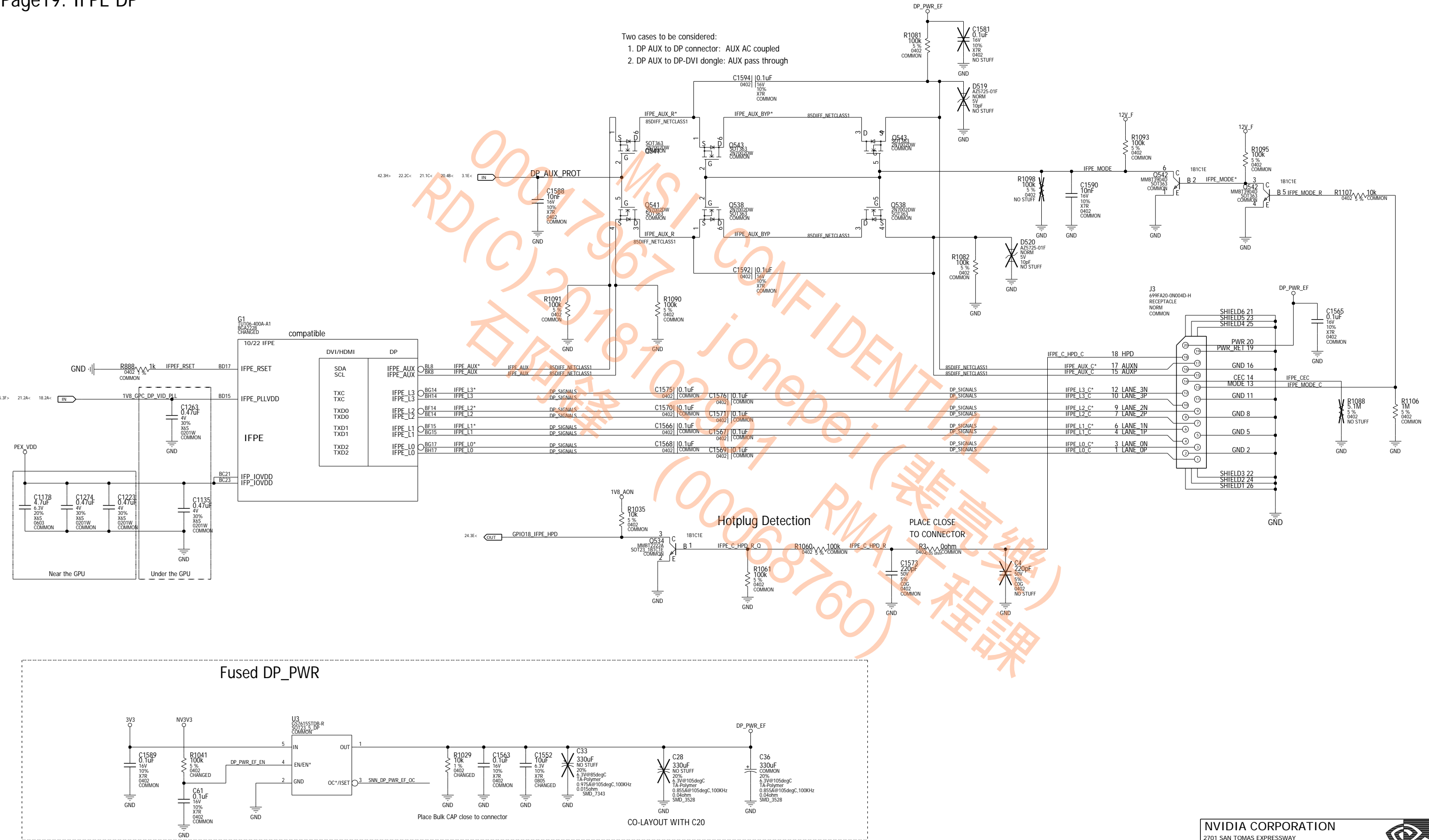
NVVDD



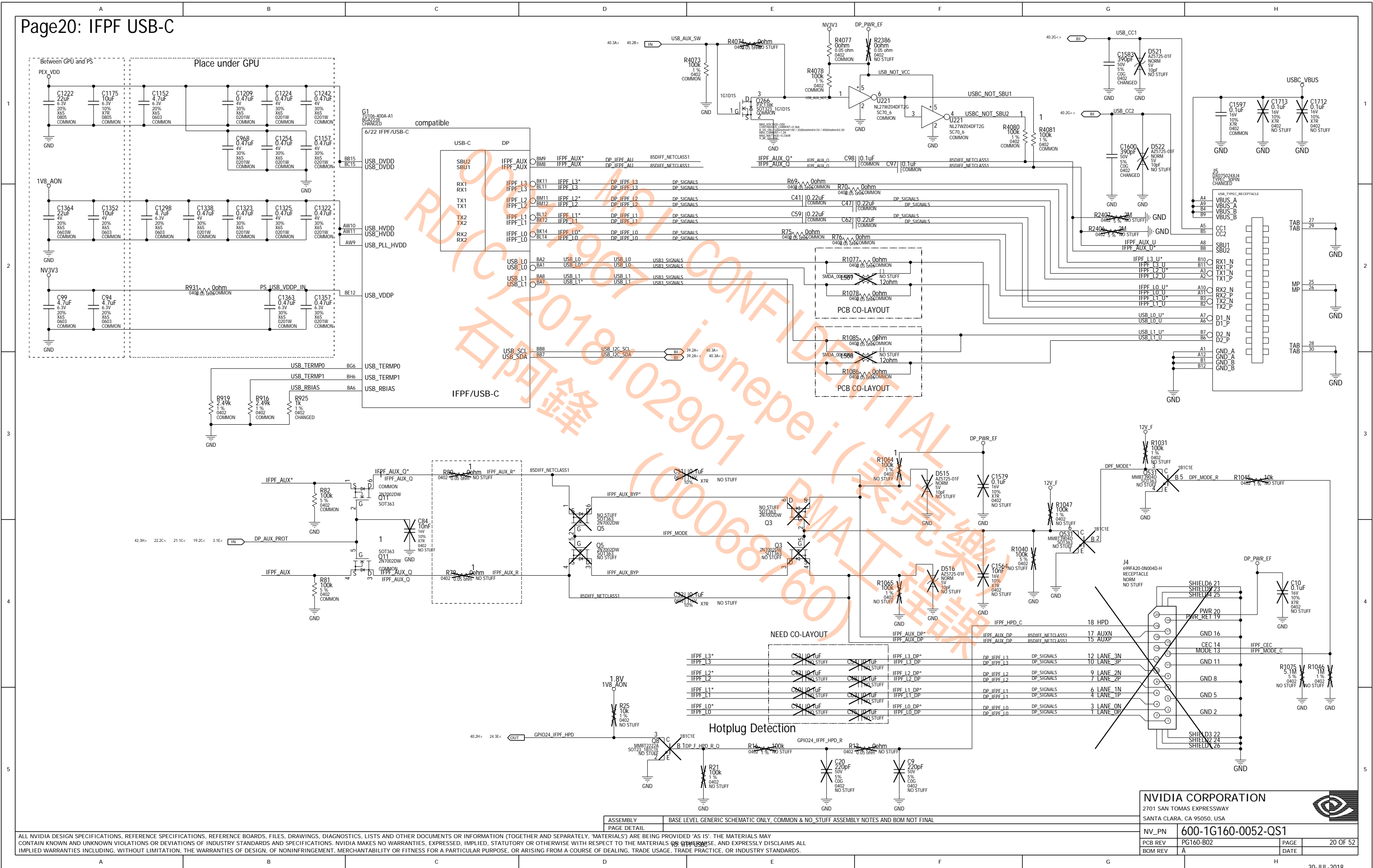
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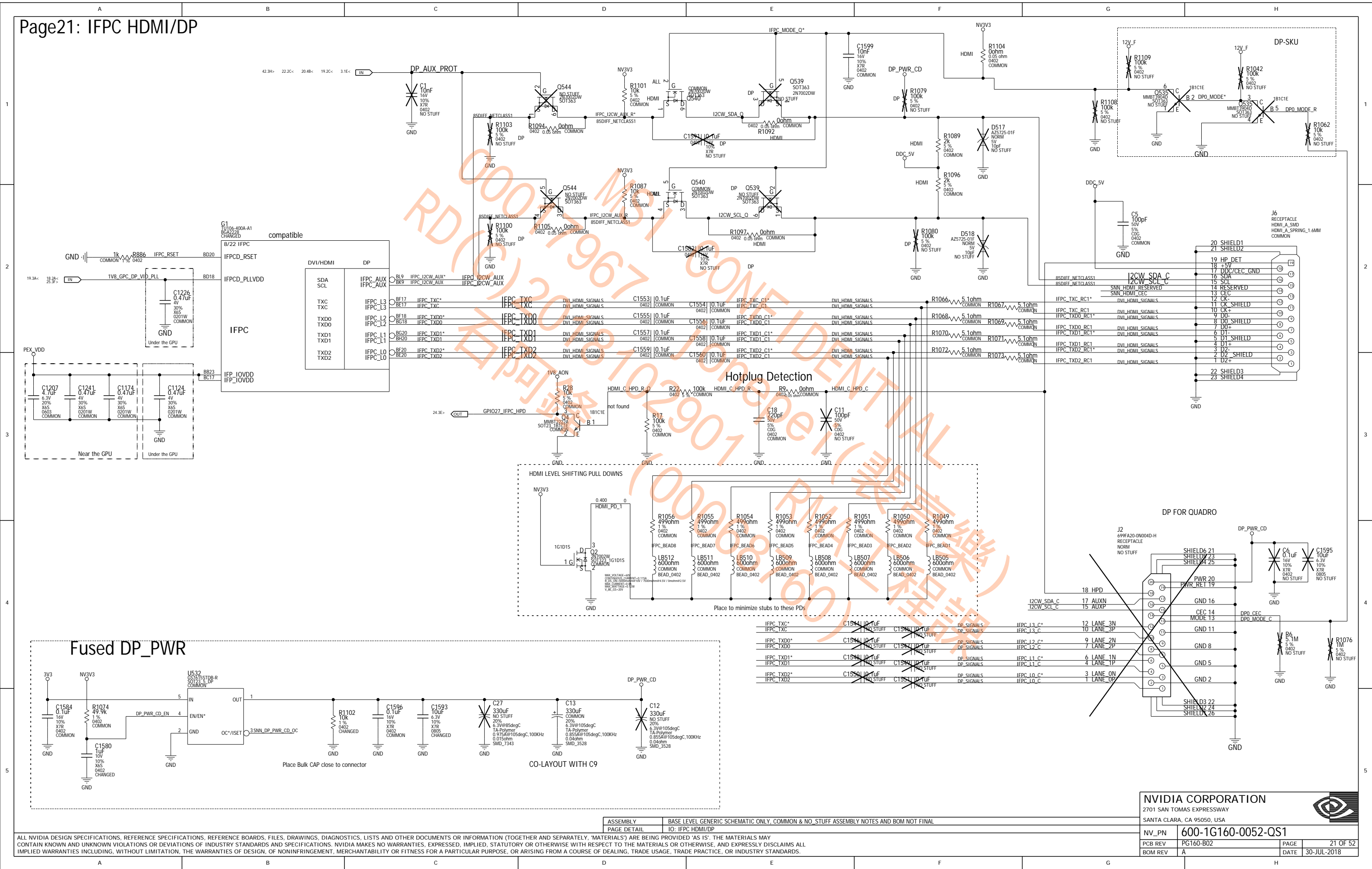
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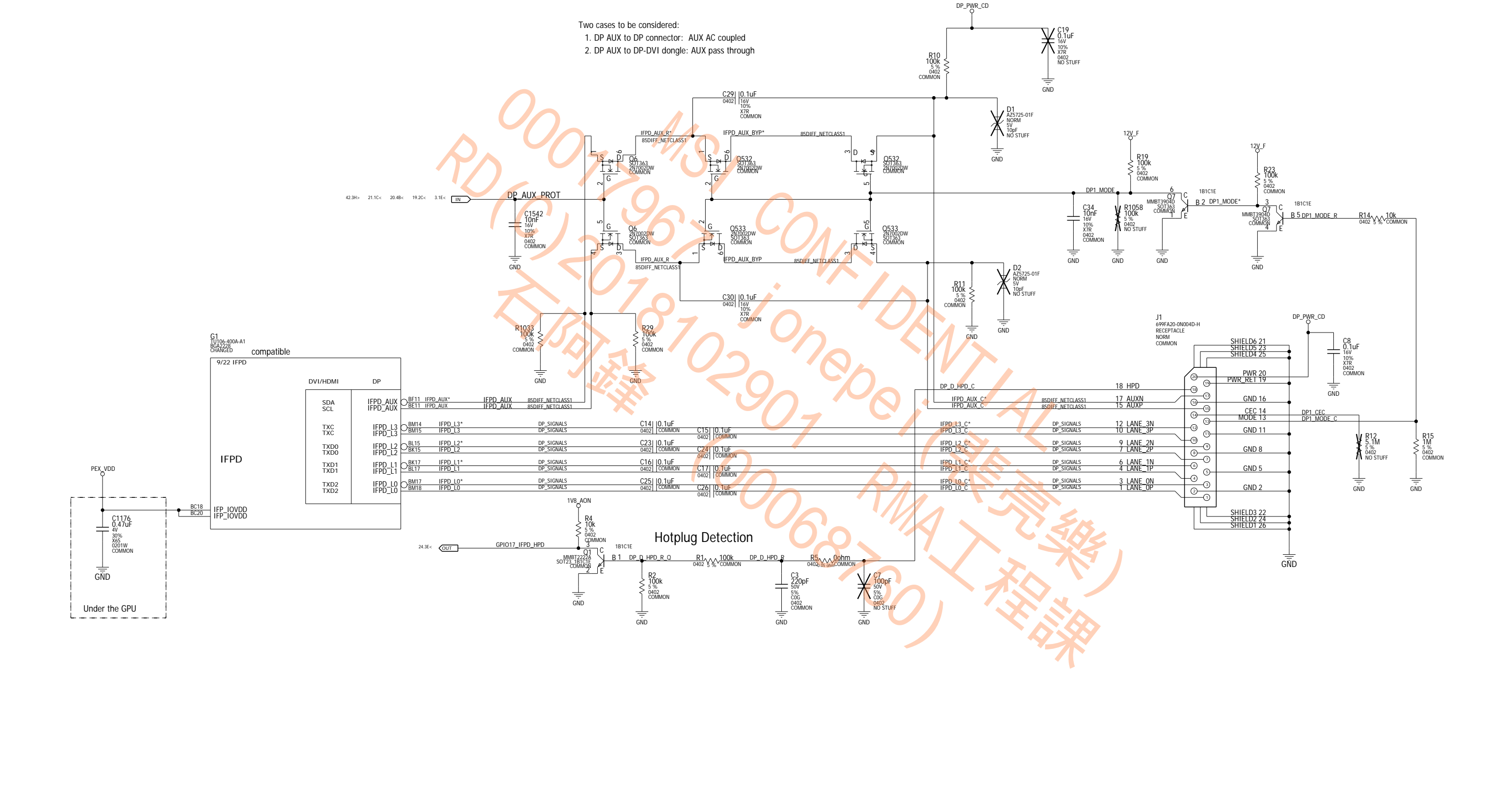


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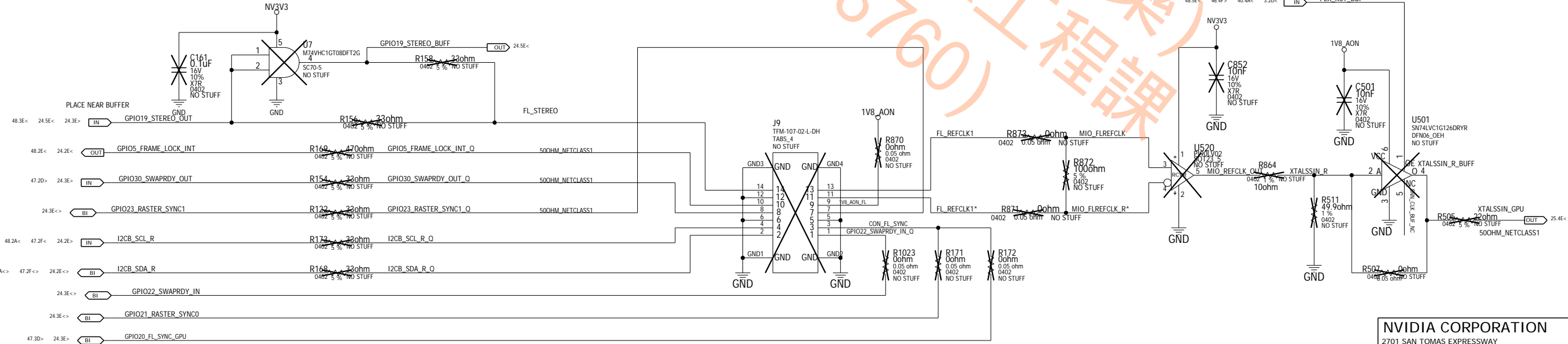
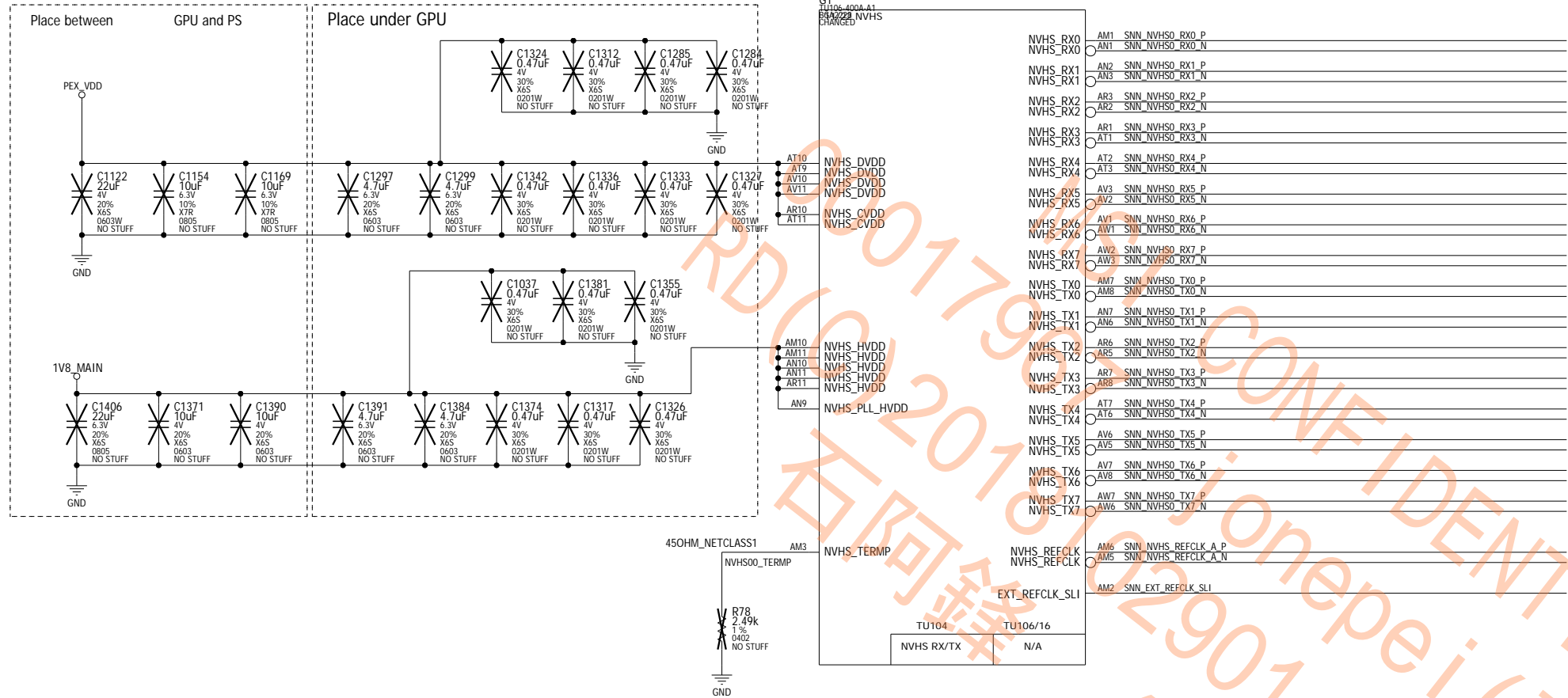






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## Page23: NVHS Interface and Frame Lock



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PAGE DETAIL	IO: NVHS Interface and Frame Lock

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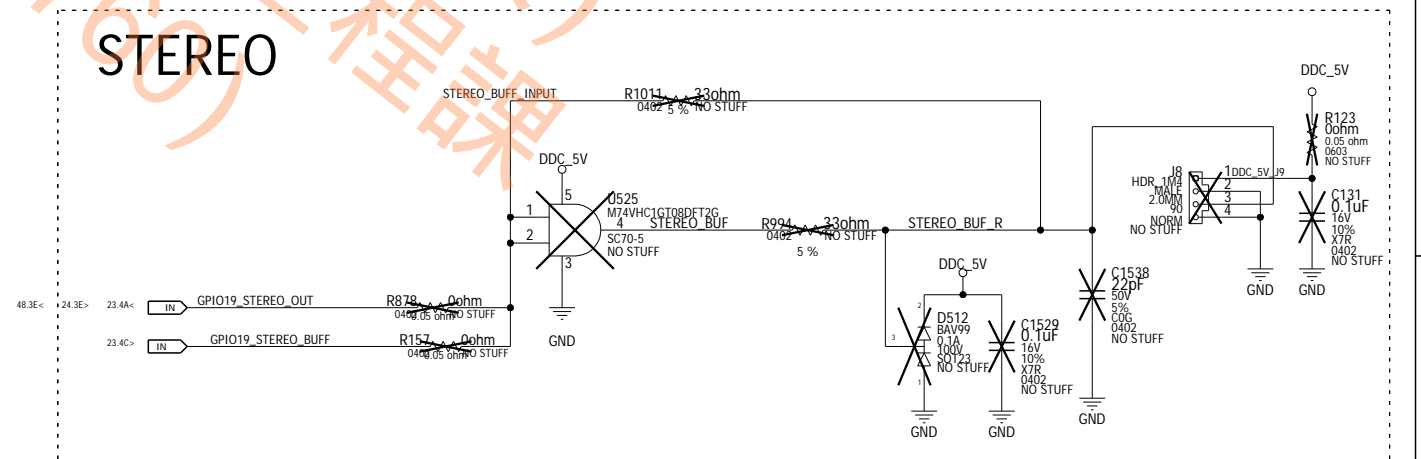
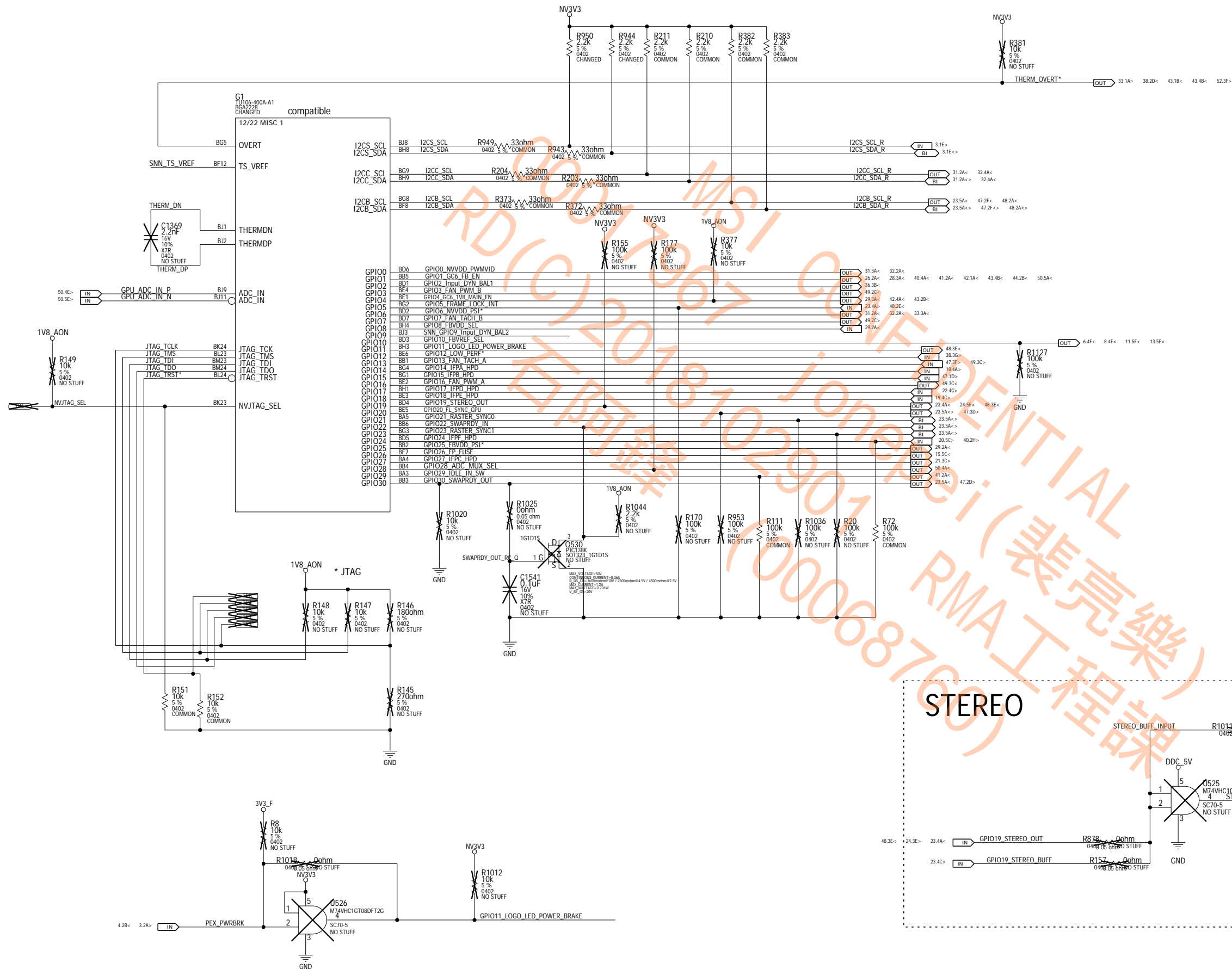
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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

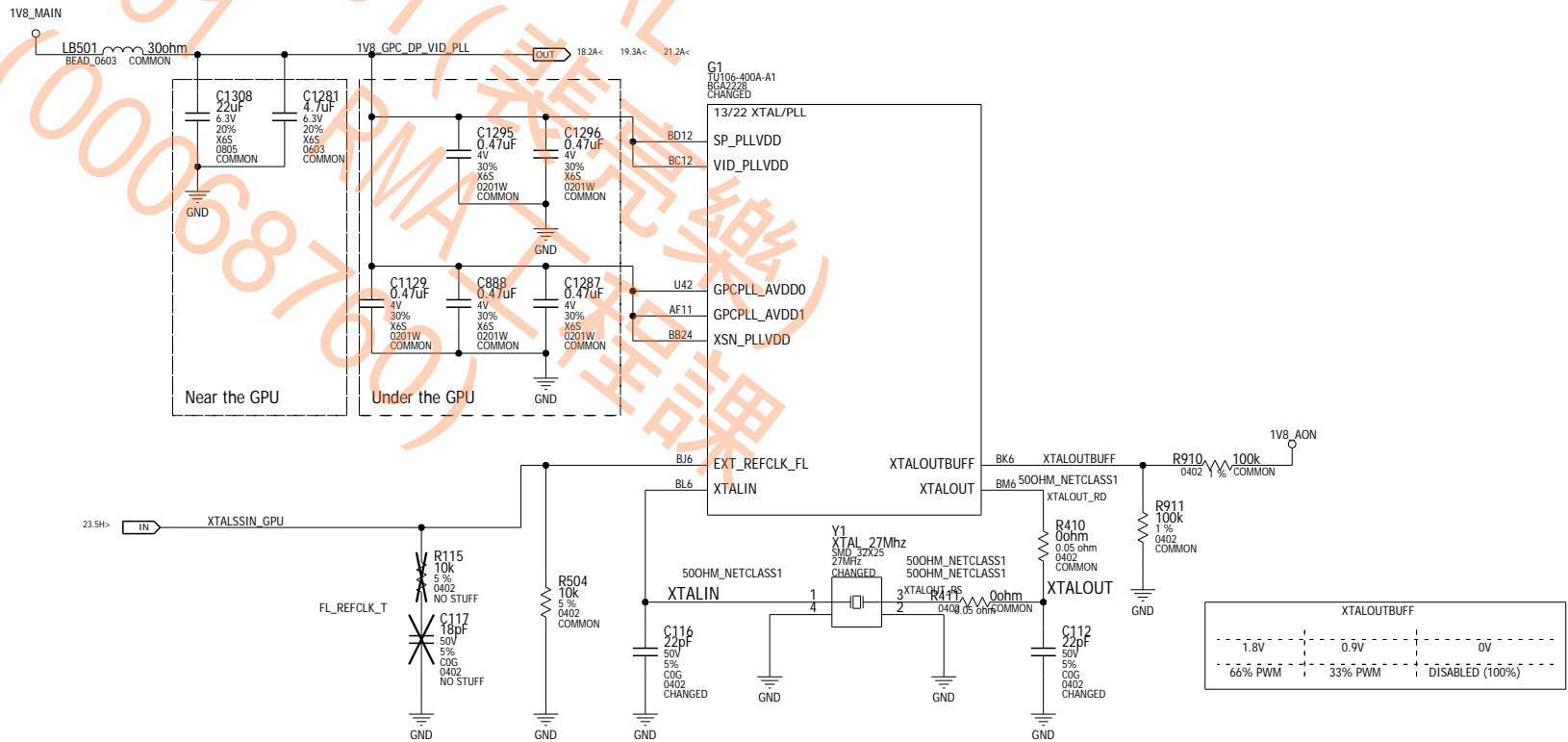
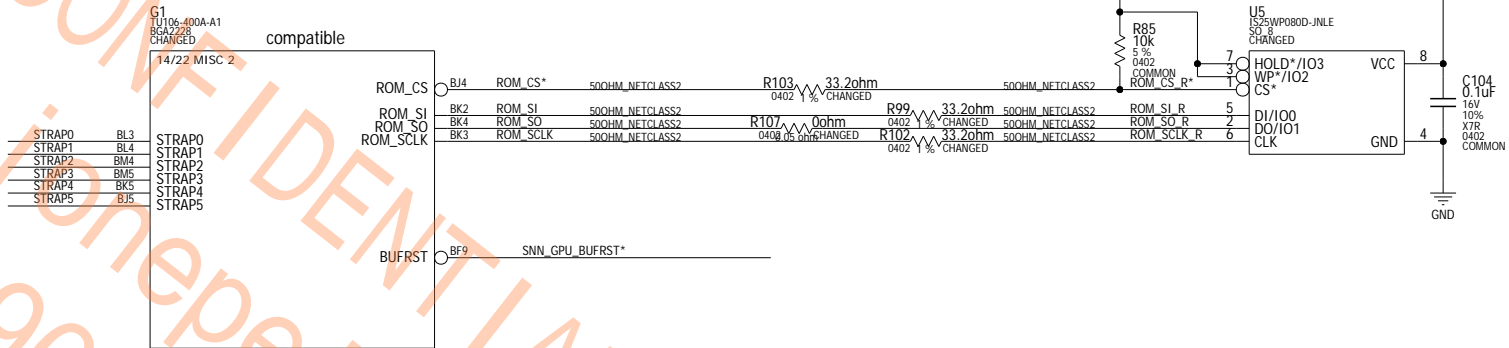
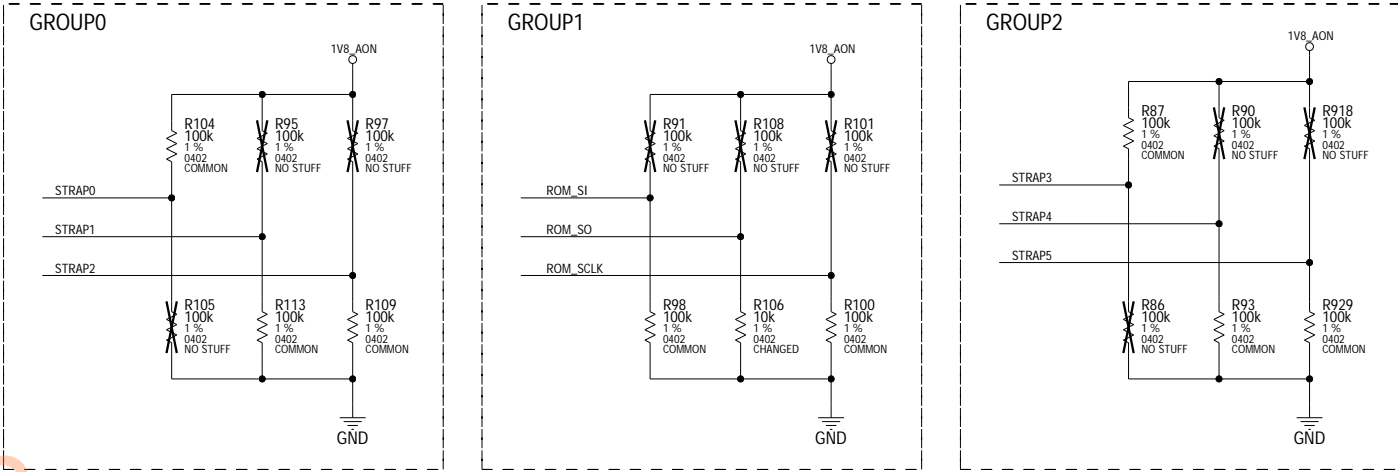
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

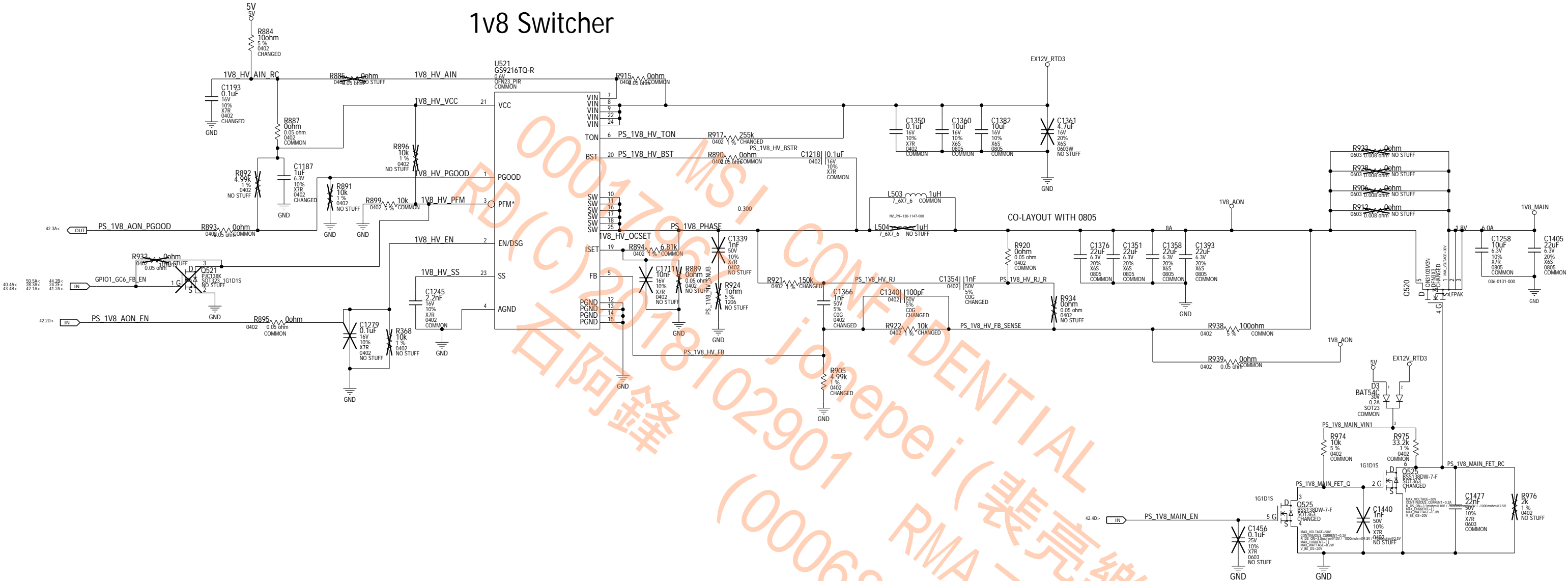
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

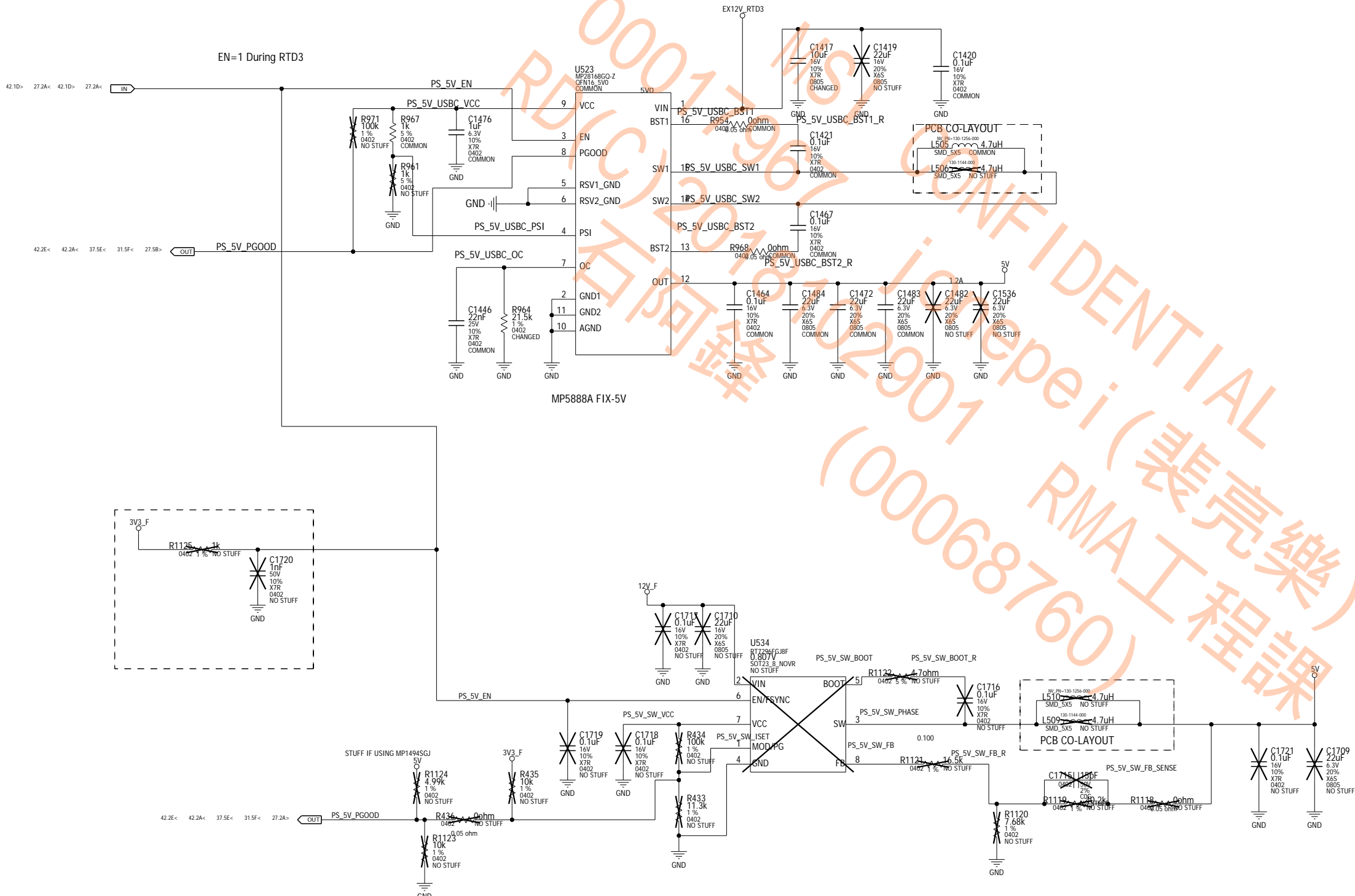
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



1v8 Switcher



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PAGE DETAIL	PS: 5V

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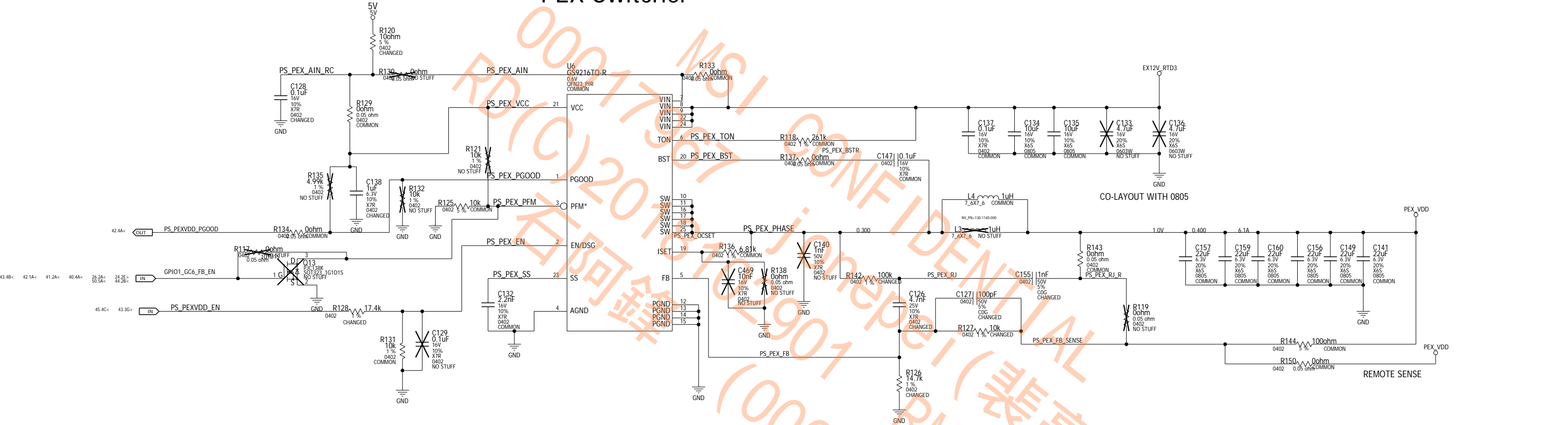
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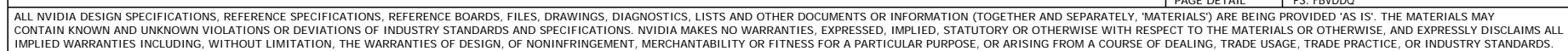
PCB REV	PG160-B02	PAGE	27 OF 52
BOM REV	A	DATE	30-JUL-2018

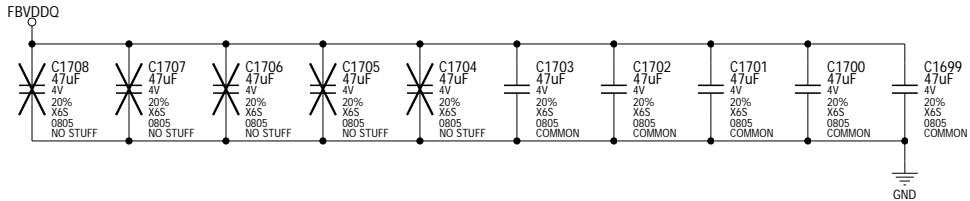
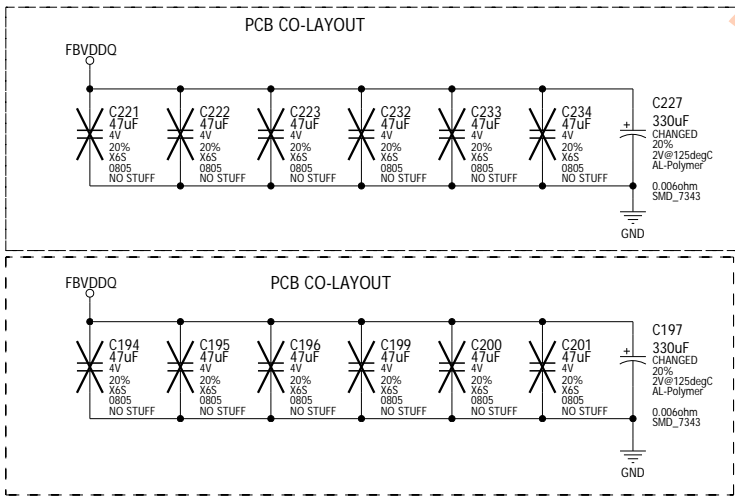
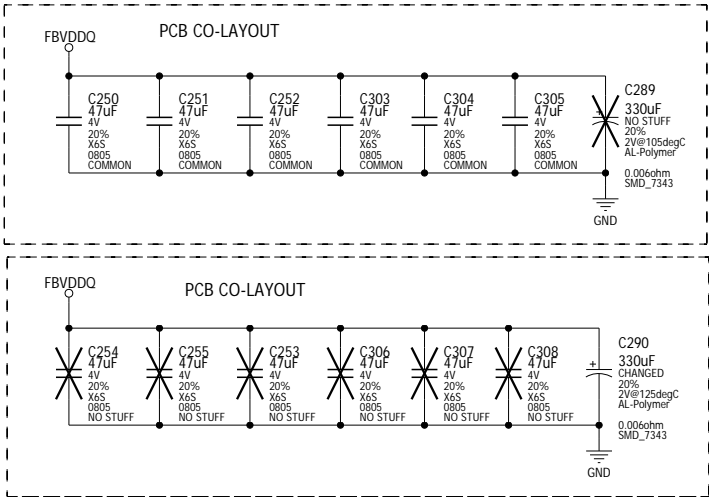
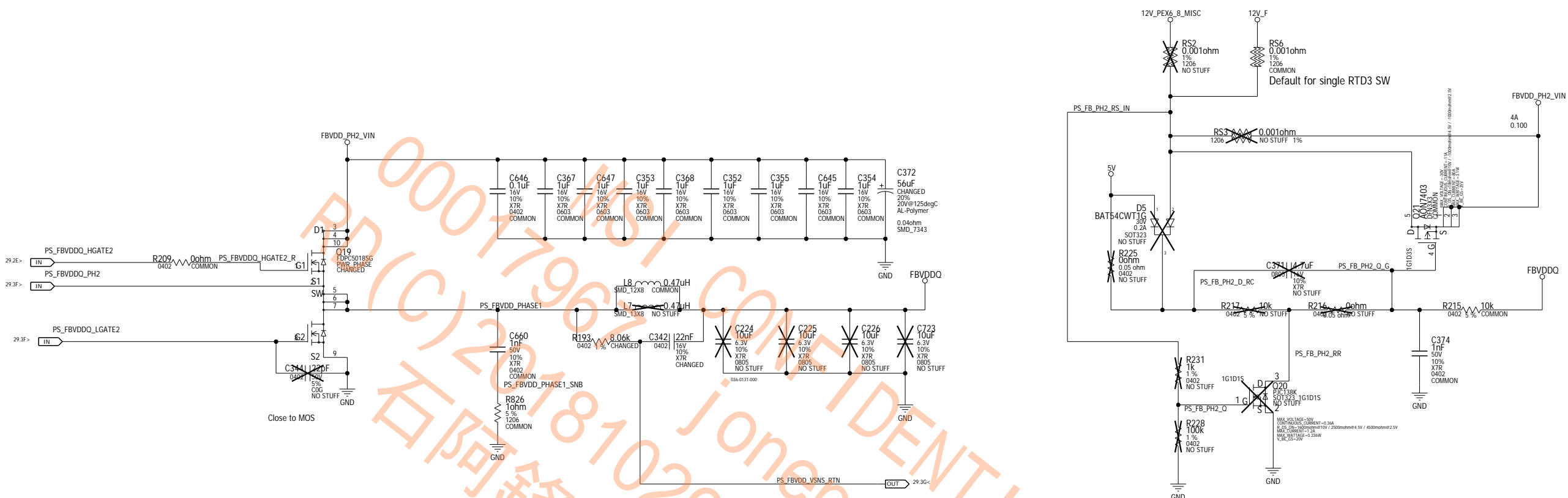
PEX Switcher



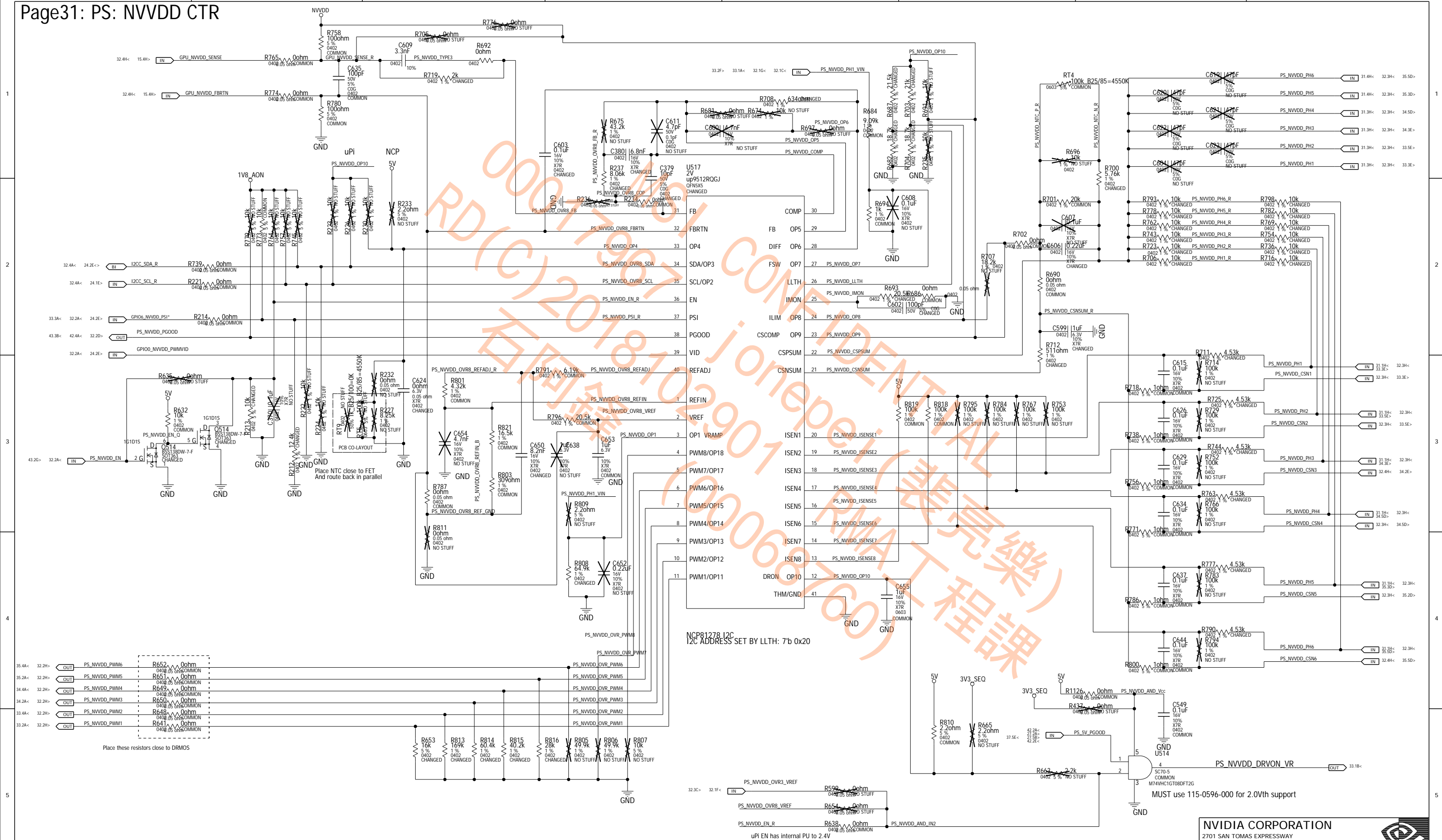
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PAGE DETAIL	PS: NVVDD Controller

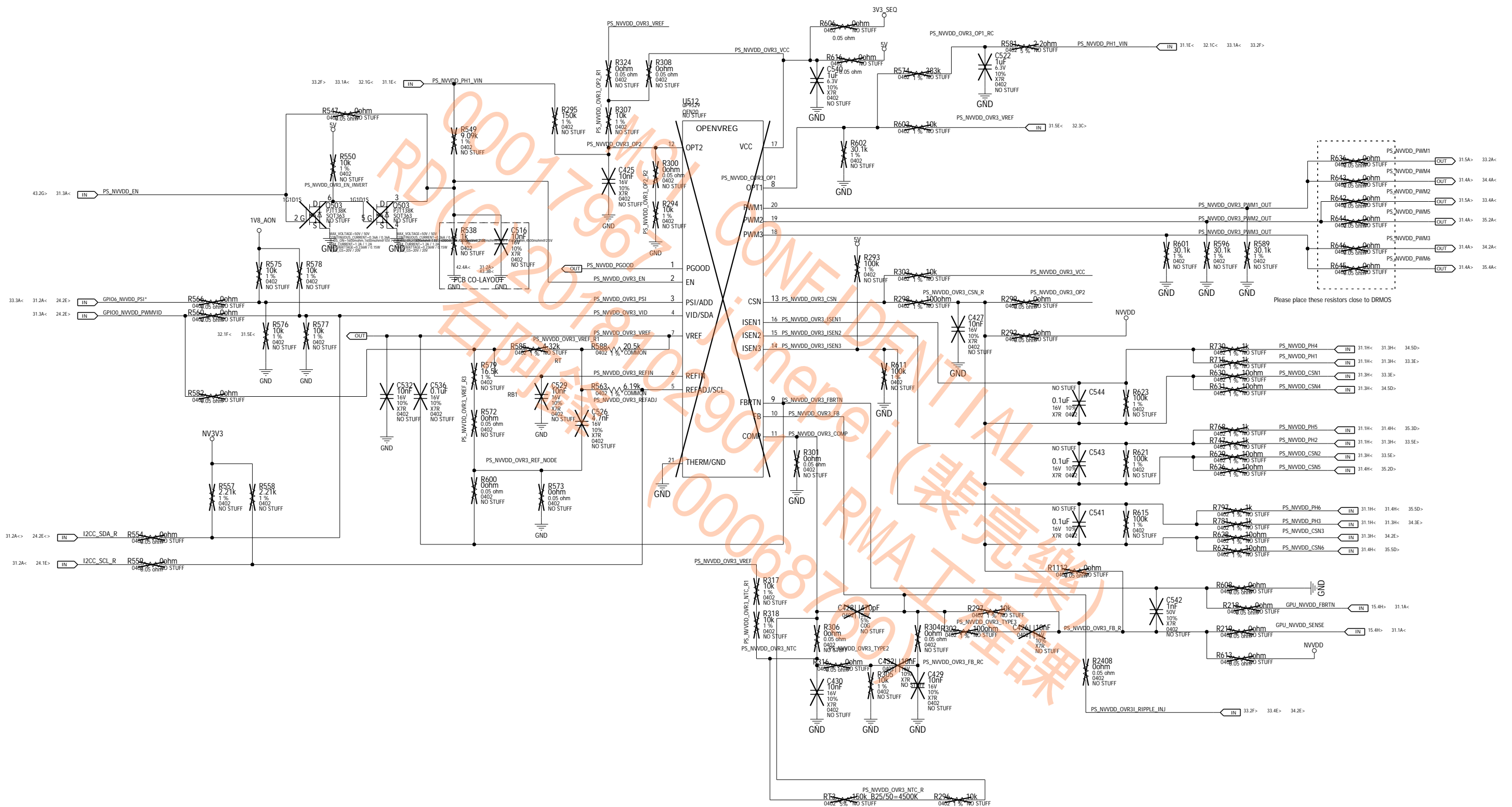
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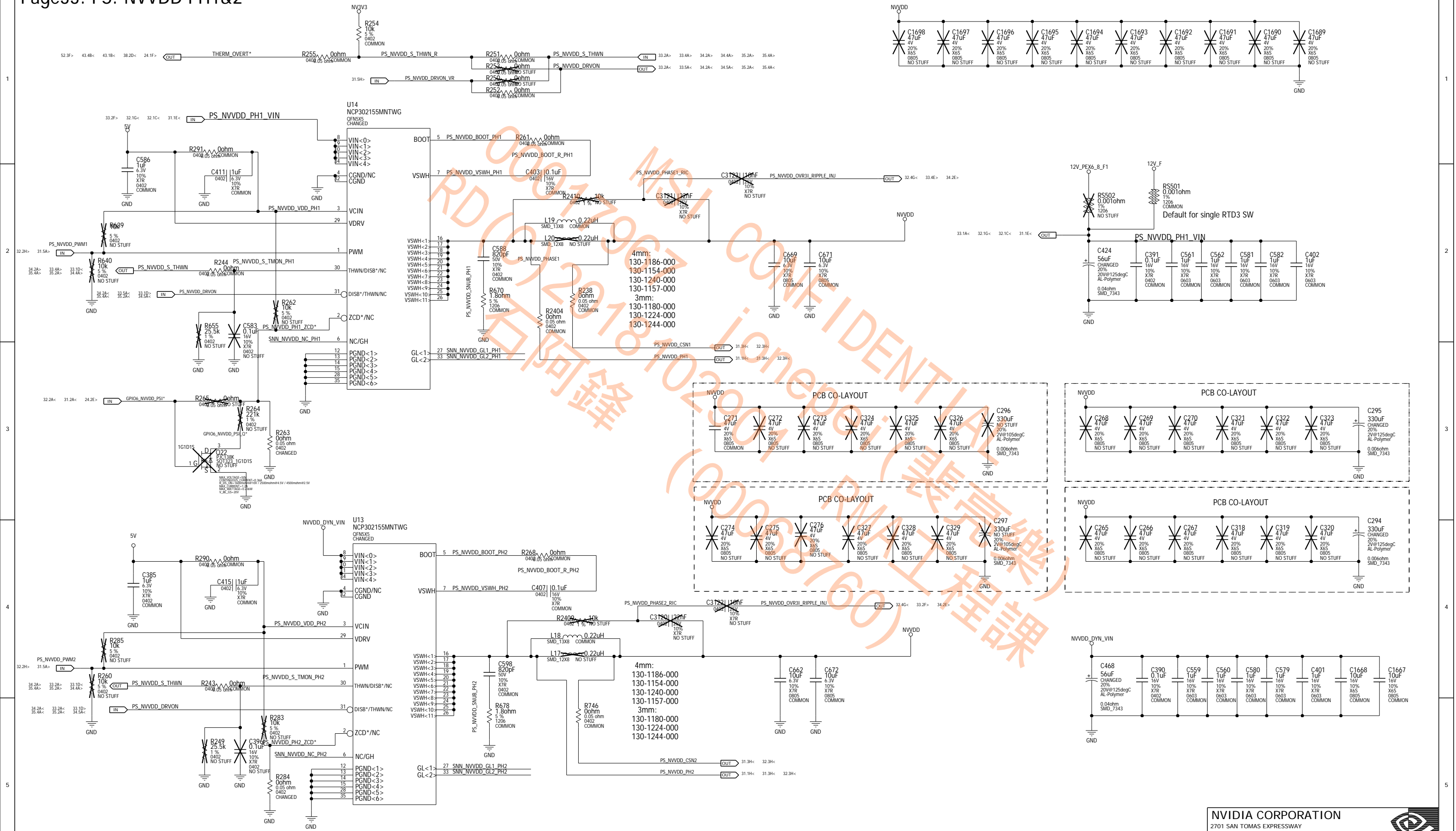
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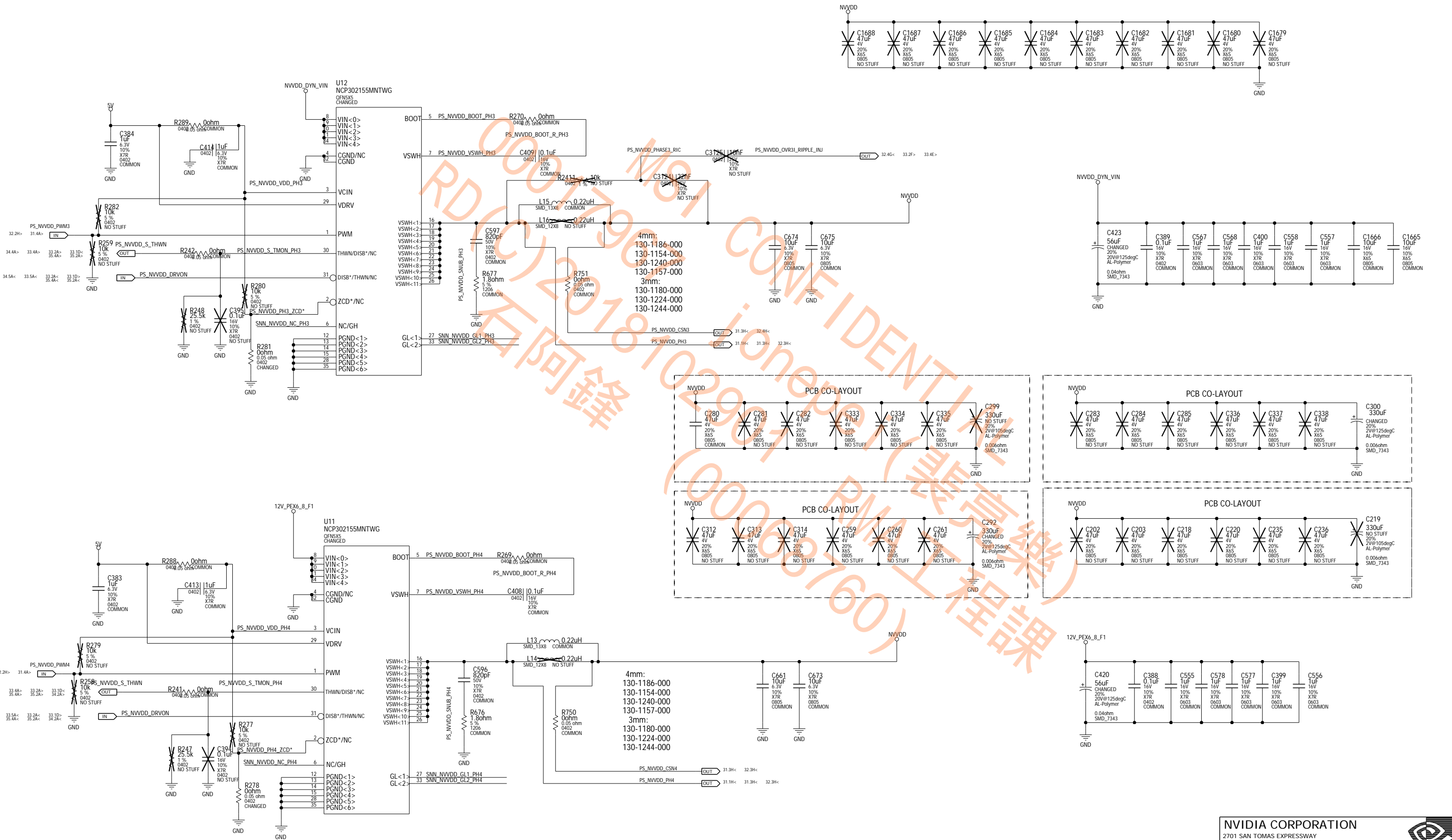
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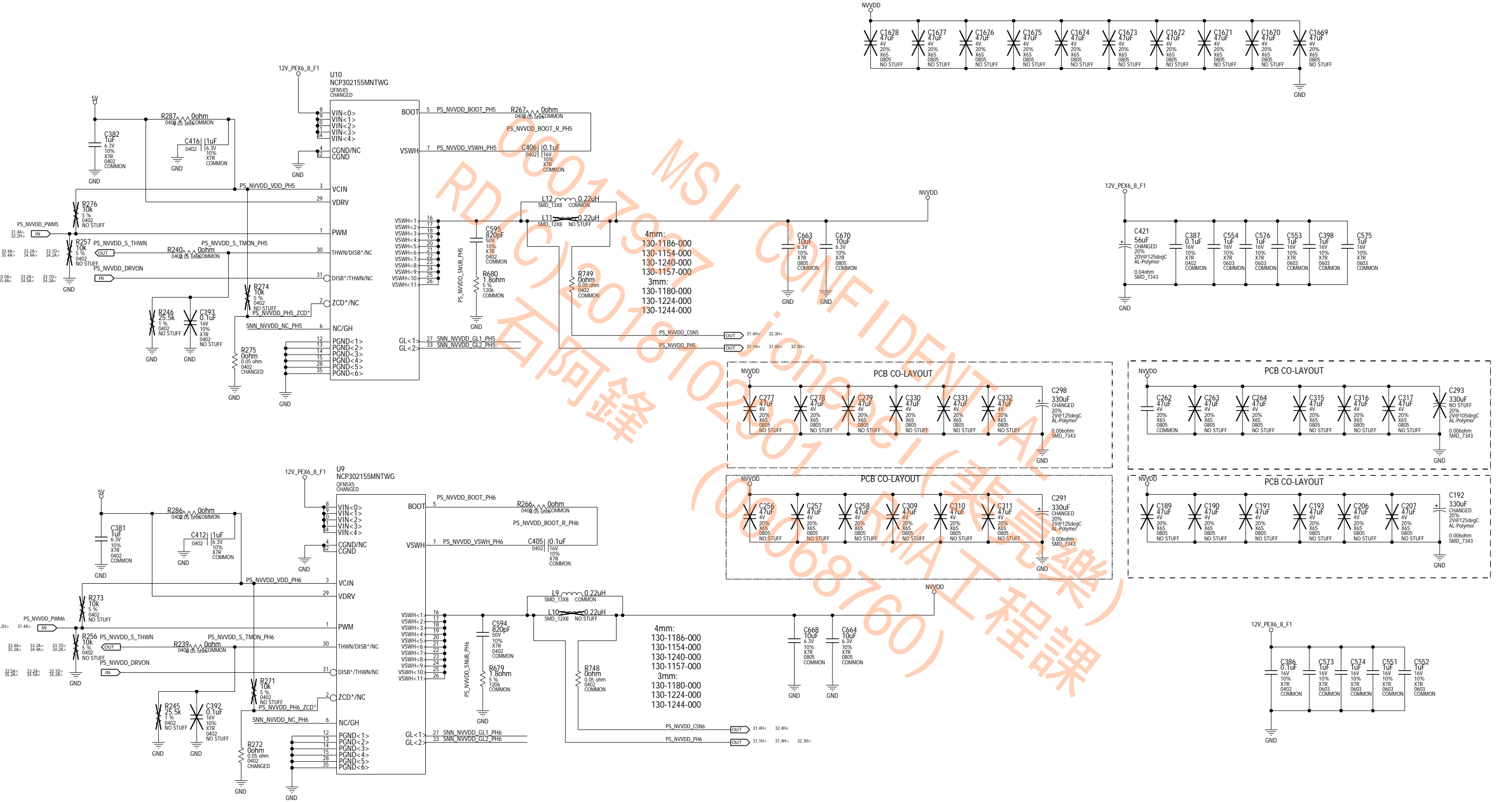
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PAGE DETAIL	PS: NVVDD Phase 1,2

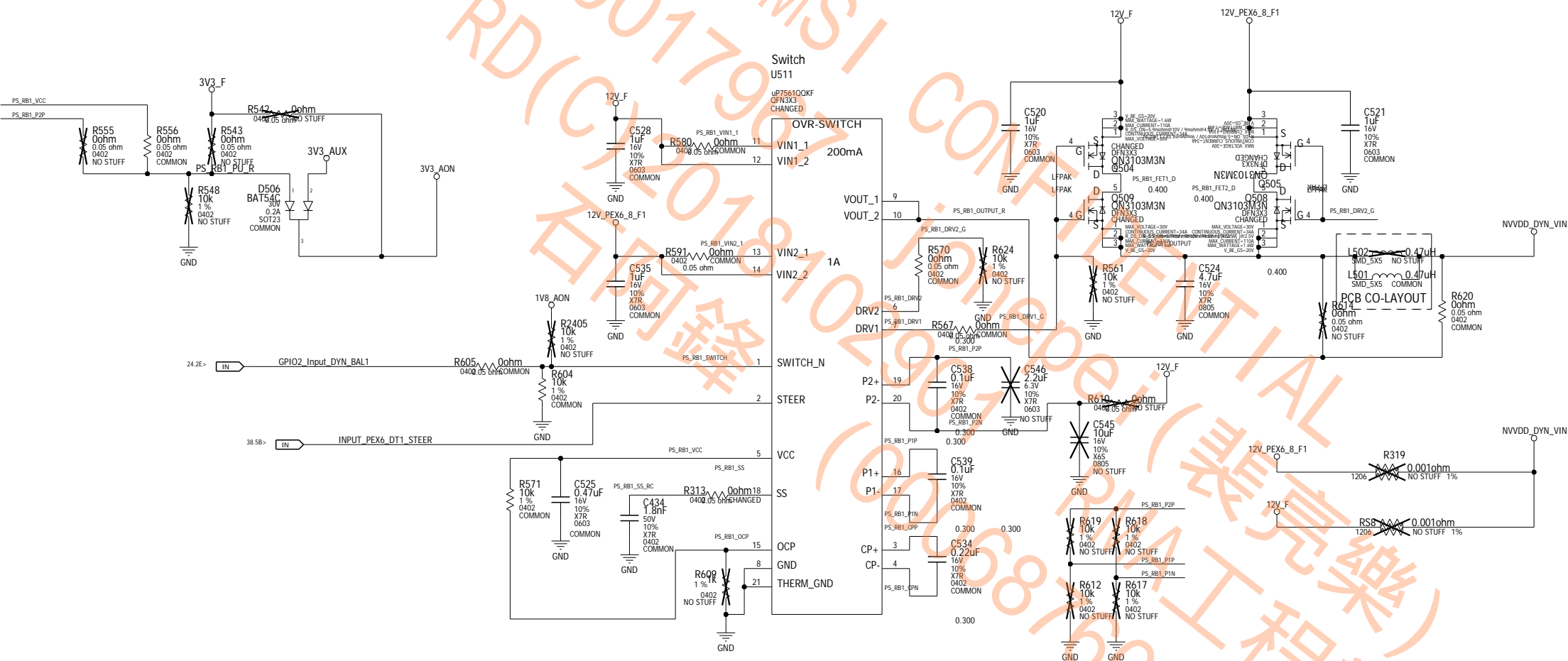
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PCB REV	PG160-B02	PAGE	33 OF 52	
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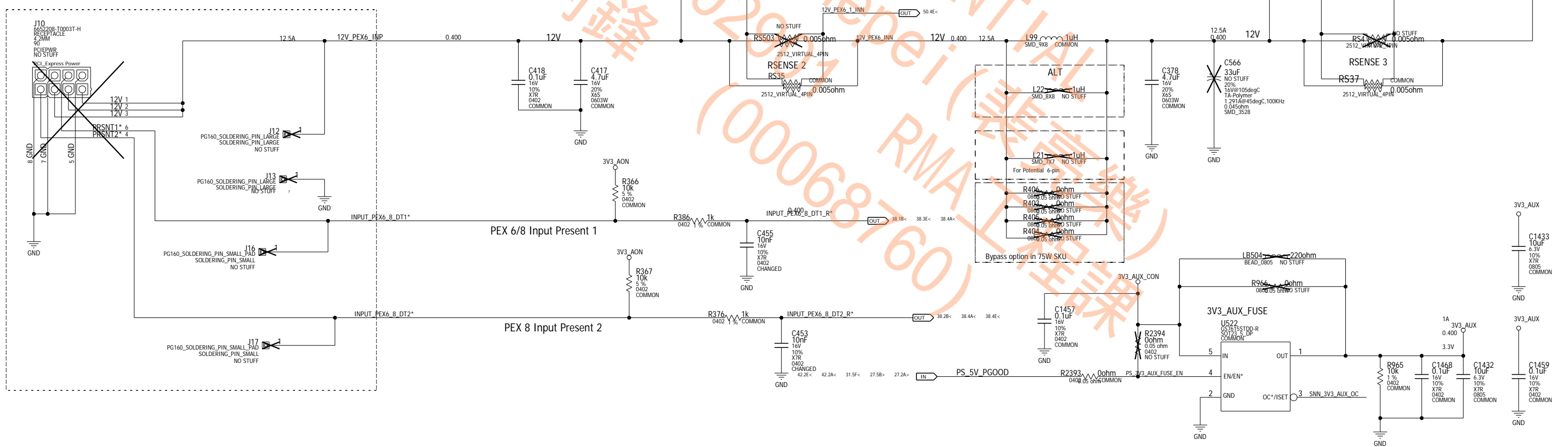
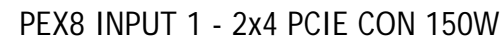
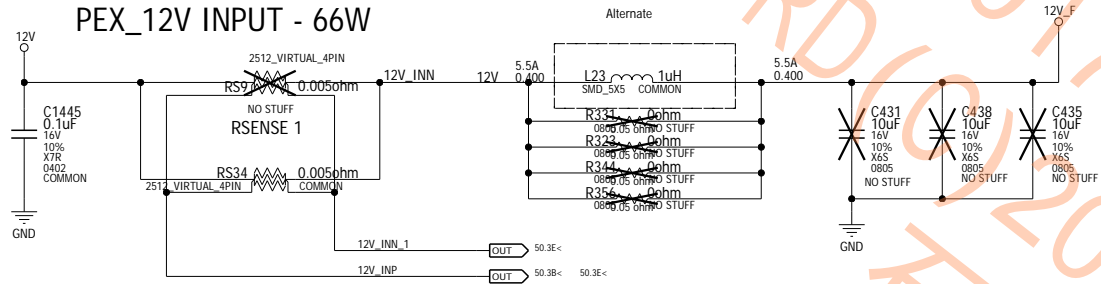
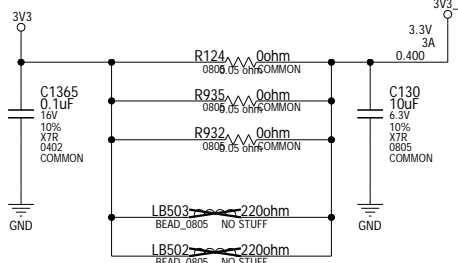


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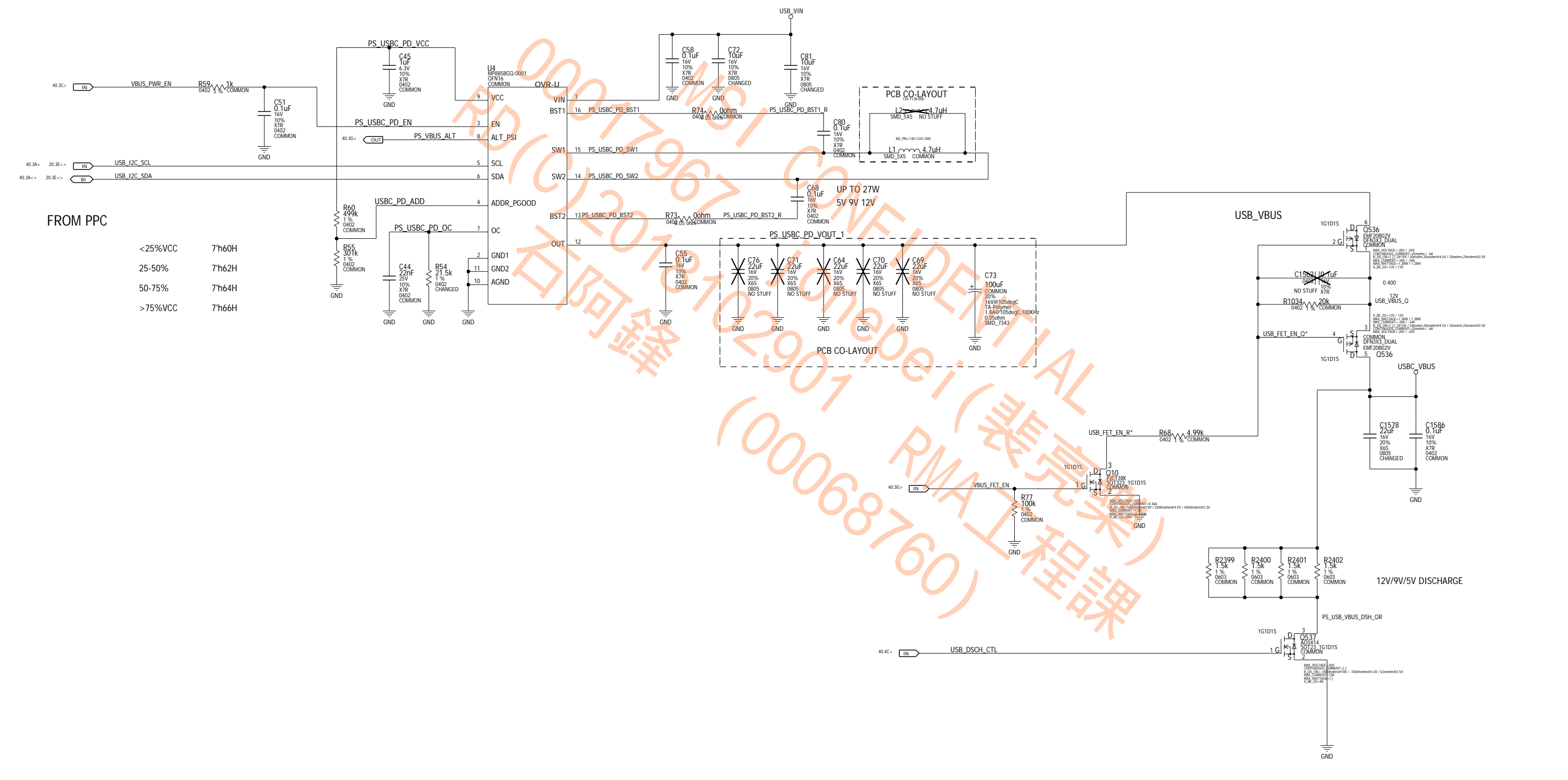
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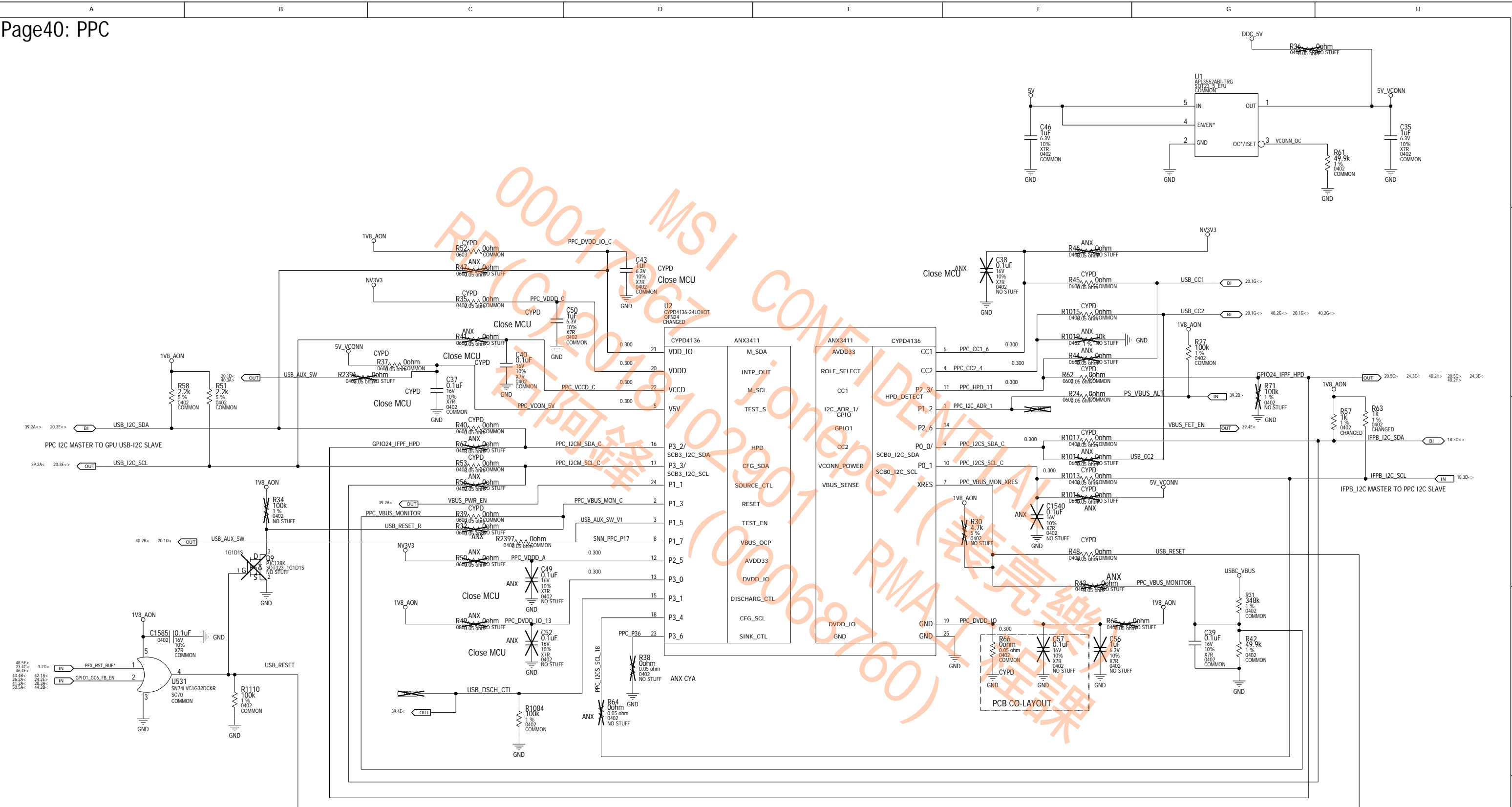
PAGE 37 OF 52

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	SCL	SDA
CYPD I2C SLAVE	PIN 10	PIN 9
CYPD I2C MASTER	PIN 17	PIN 16
ANX I2C SLAVE	PIN 18	PIN 17
ANX I2C MASTER	PIN 22	PIN 21

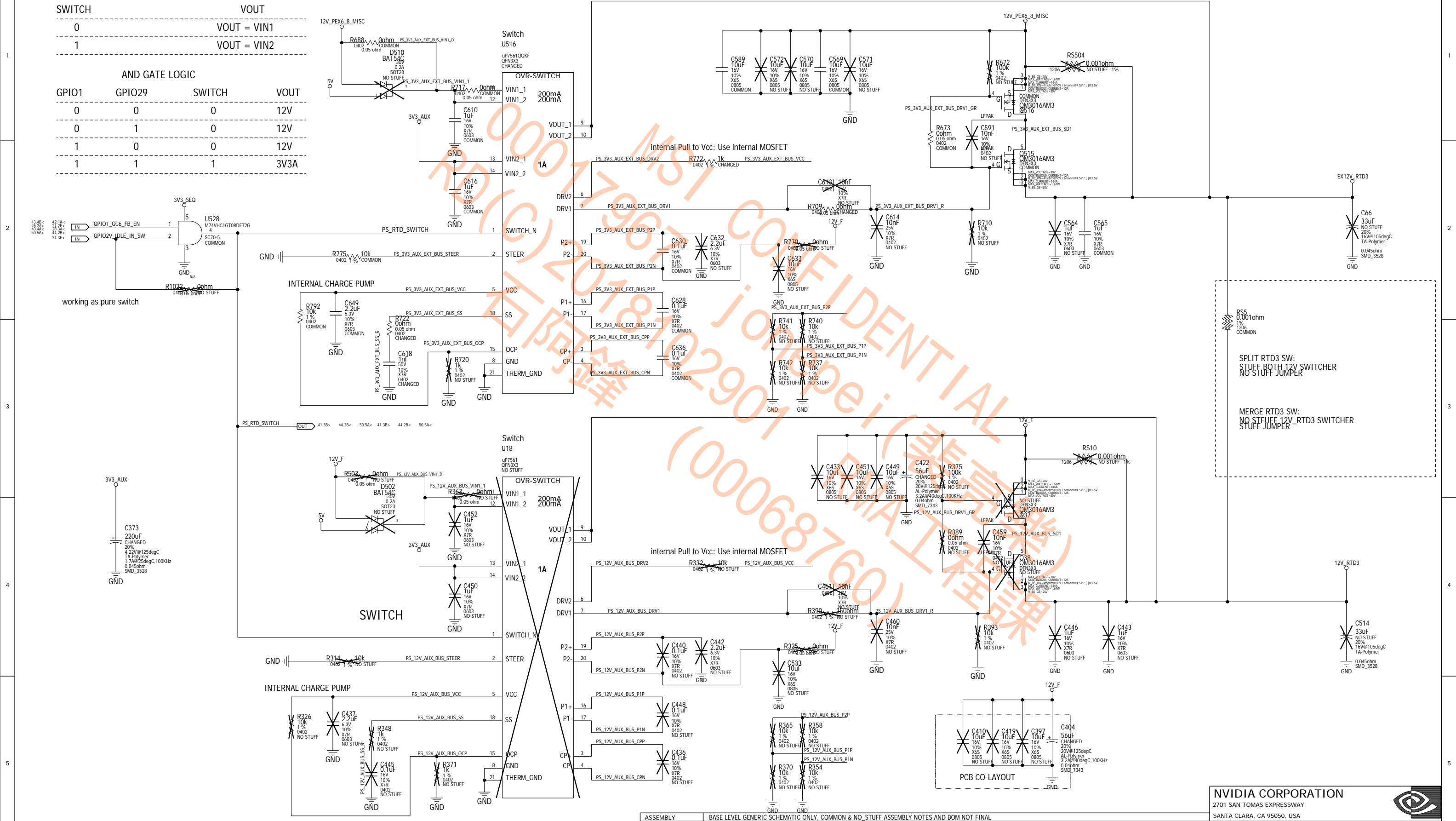
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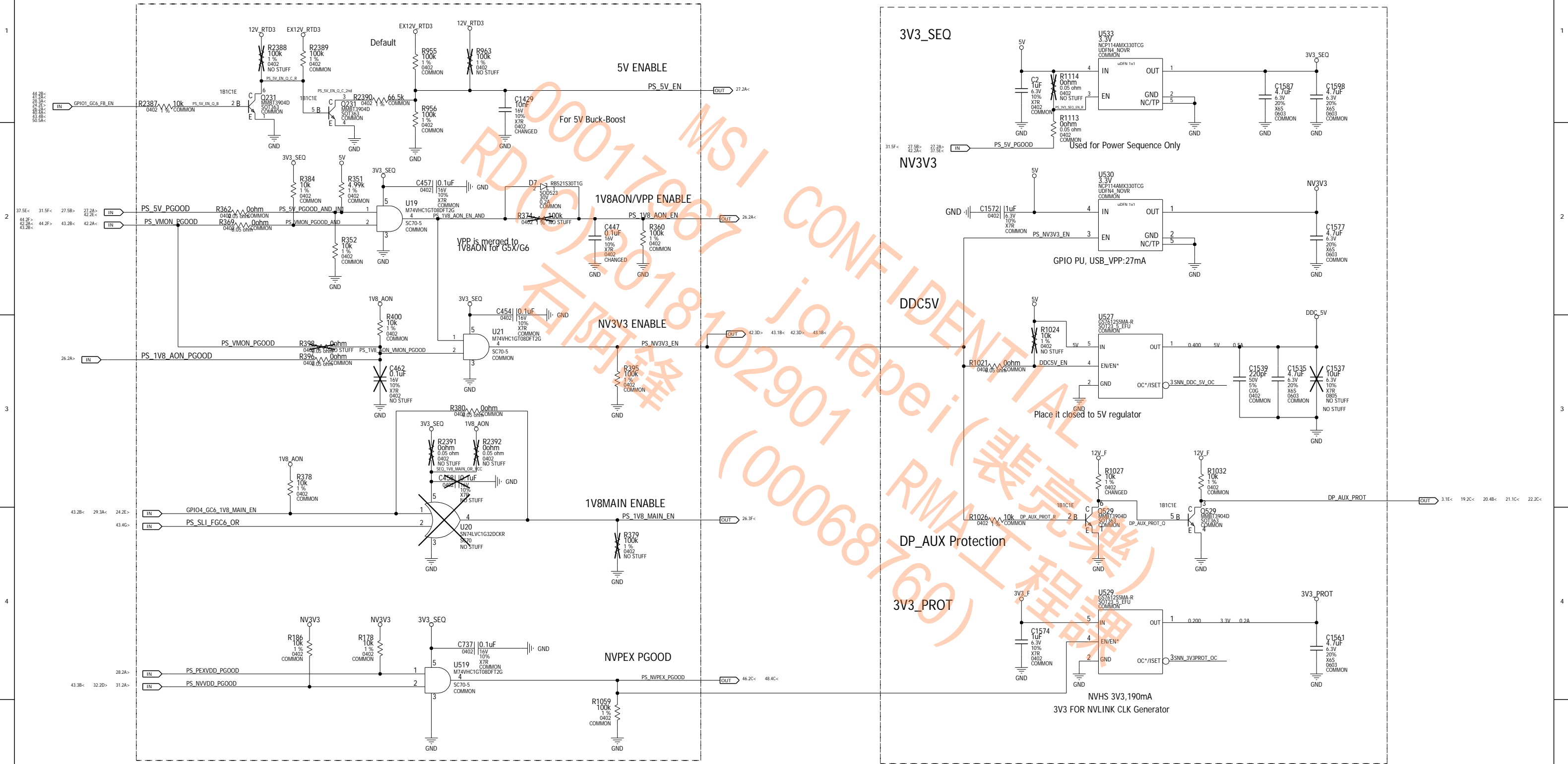
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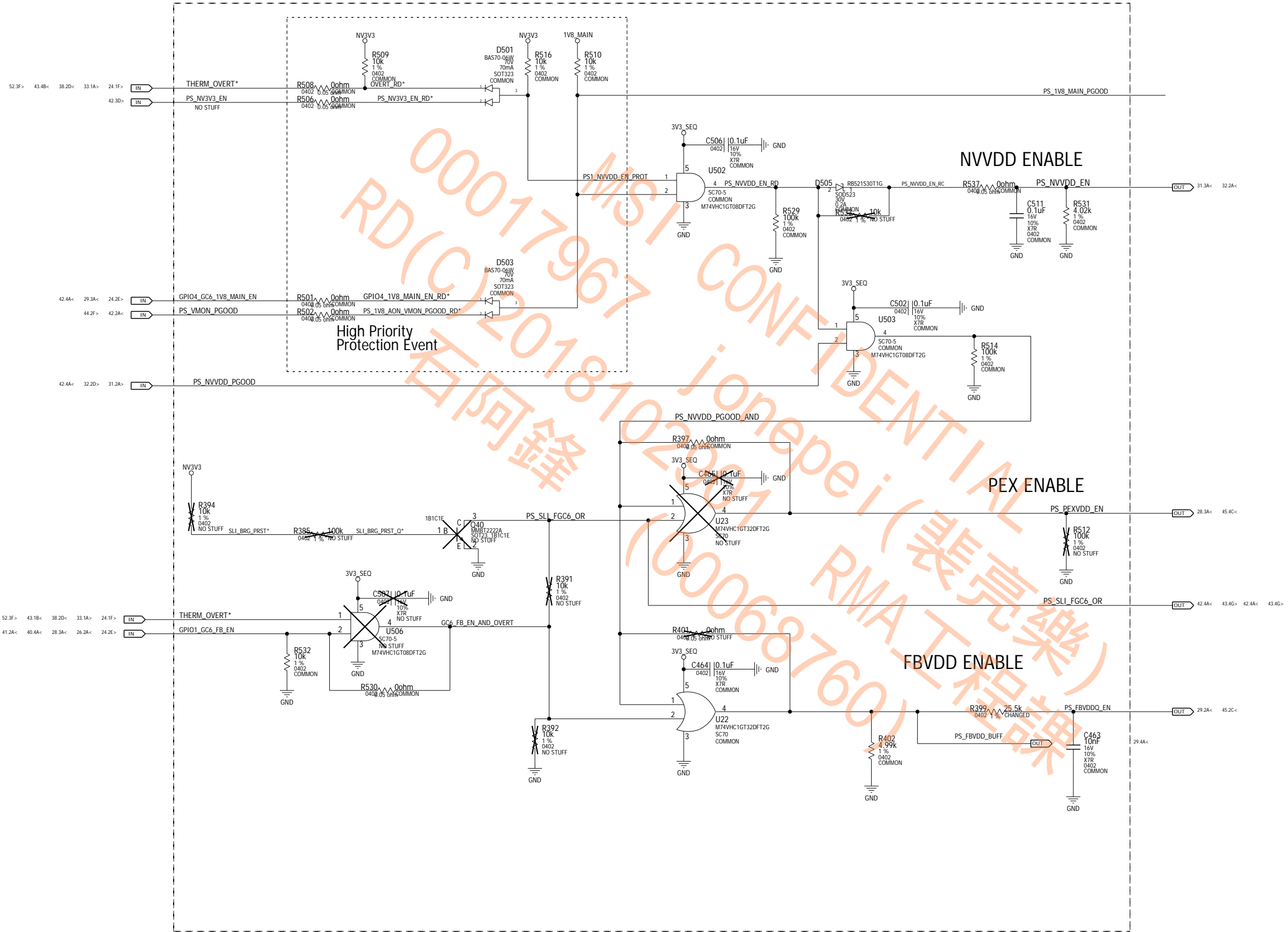




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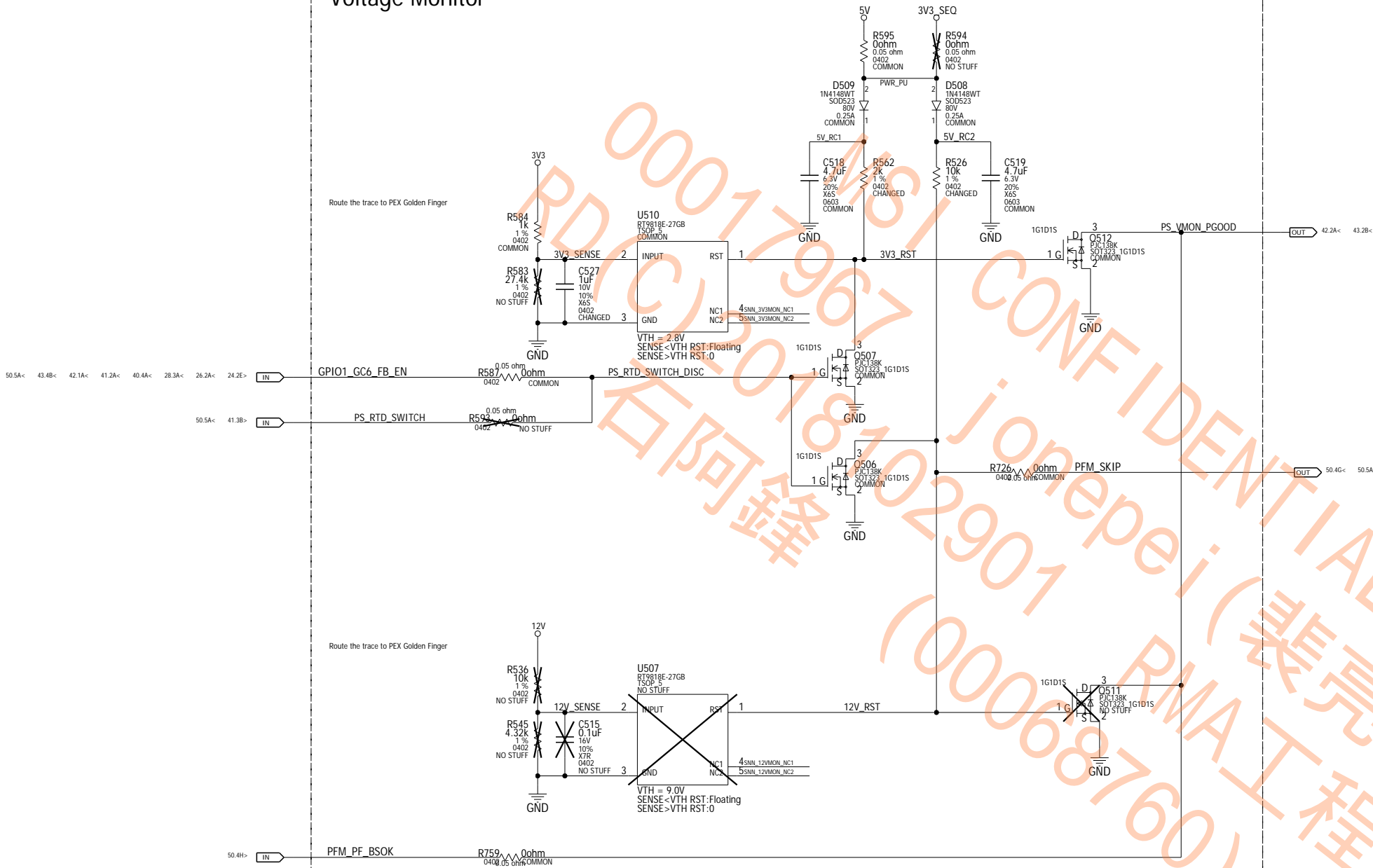


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Voltage Monitor

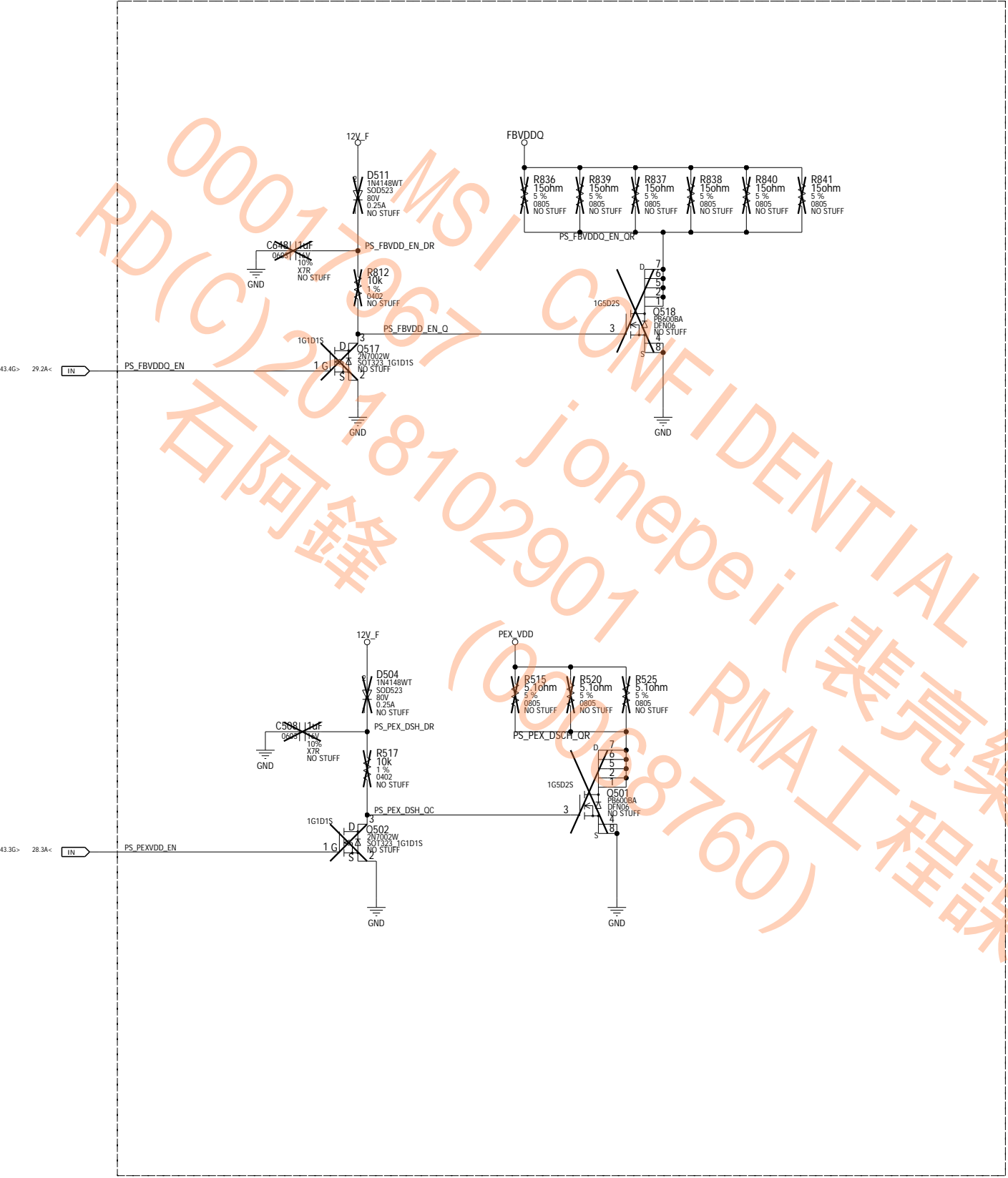


BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

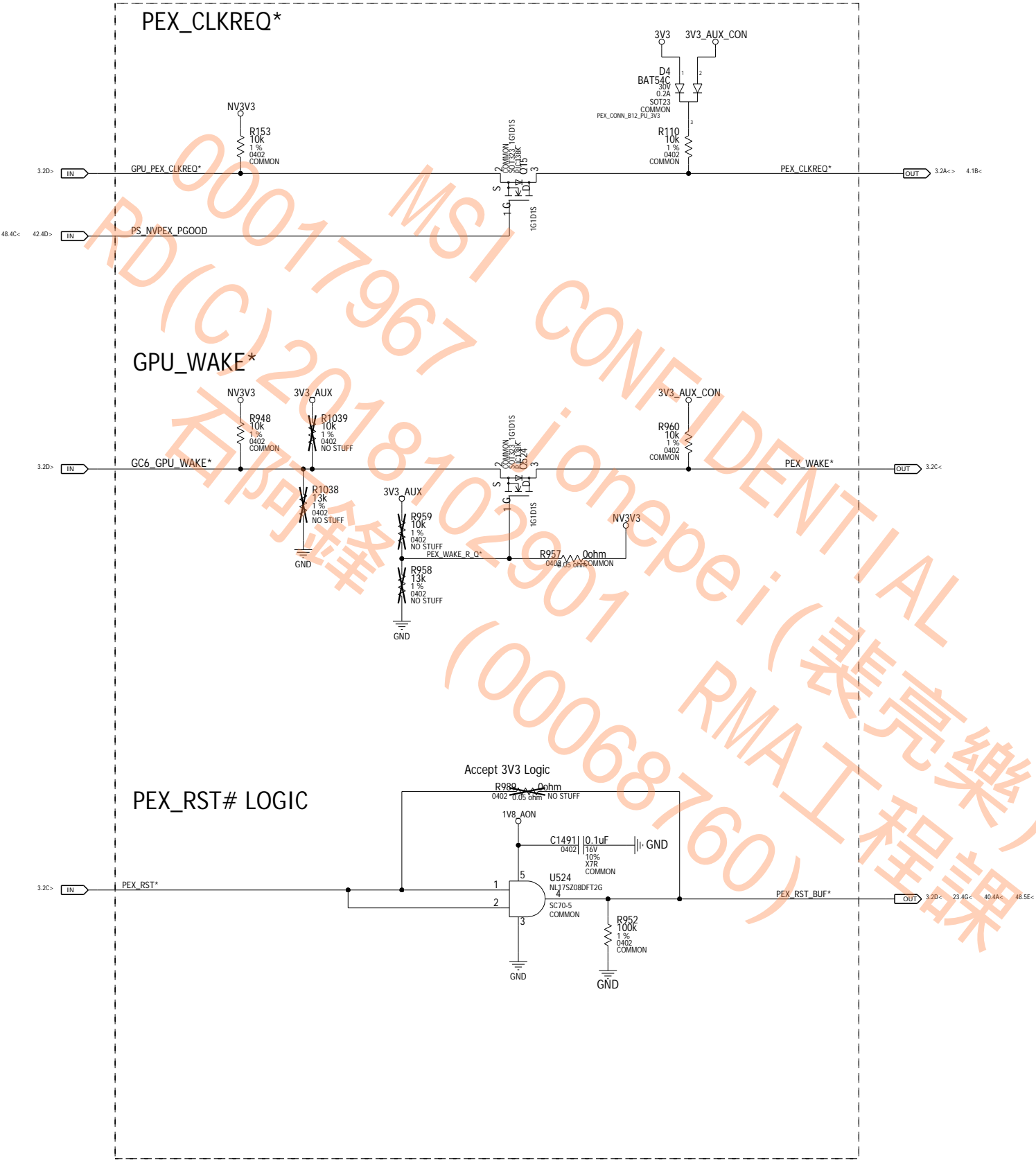
Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)





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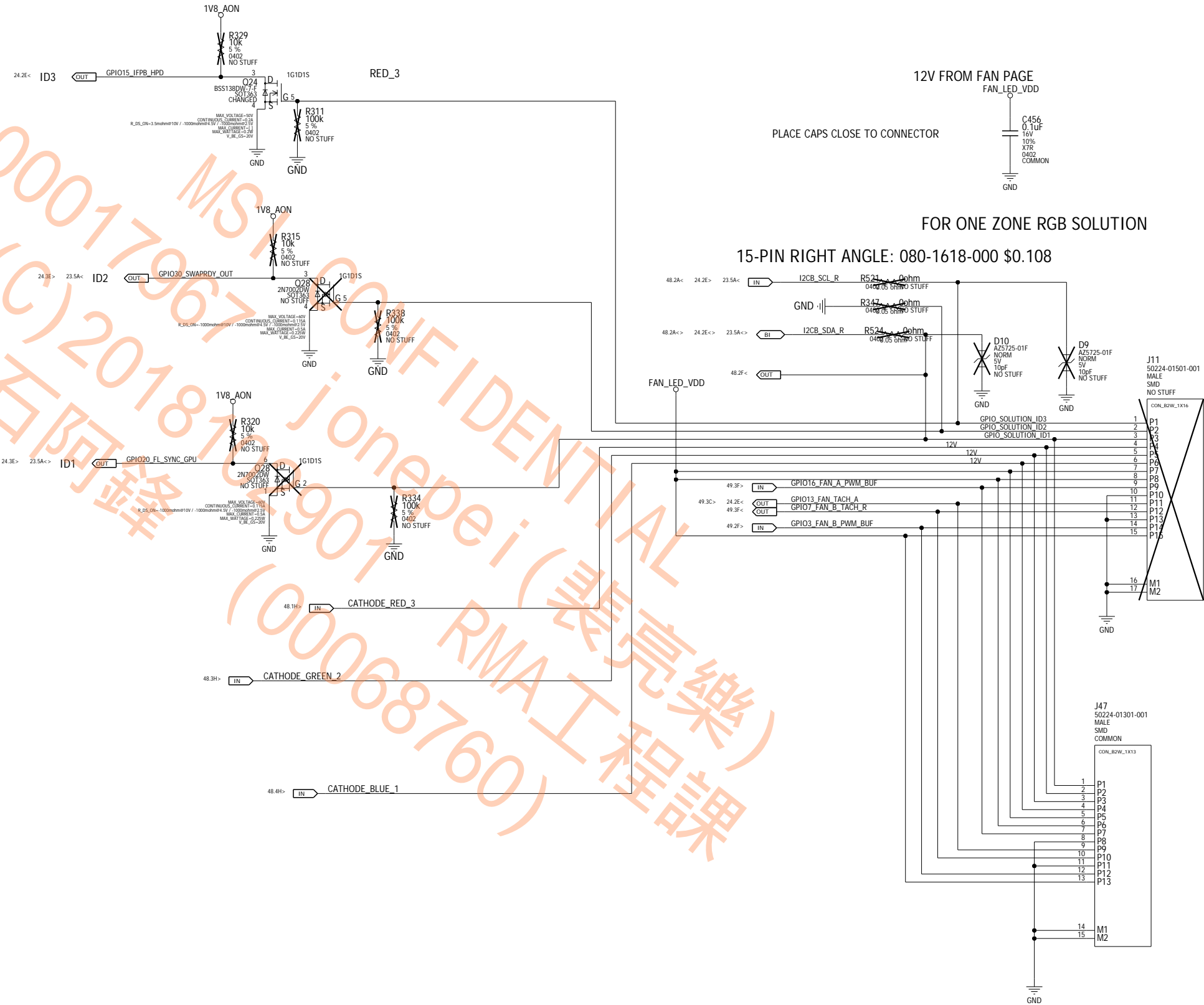
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PCB REV	PG160-B02	PAGE	45 OF 52
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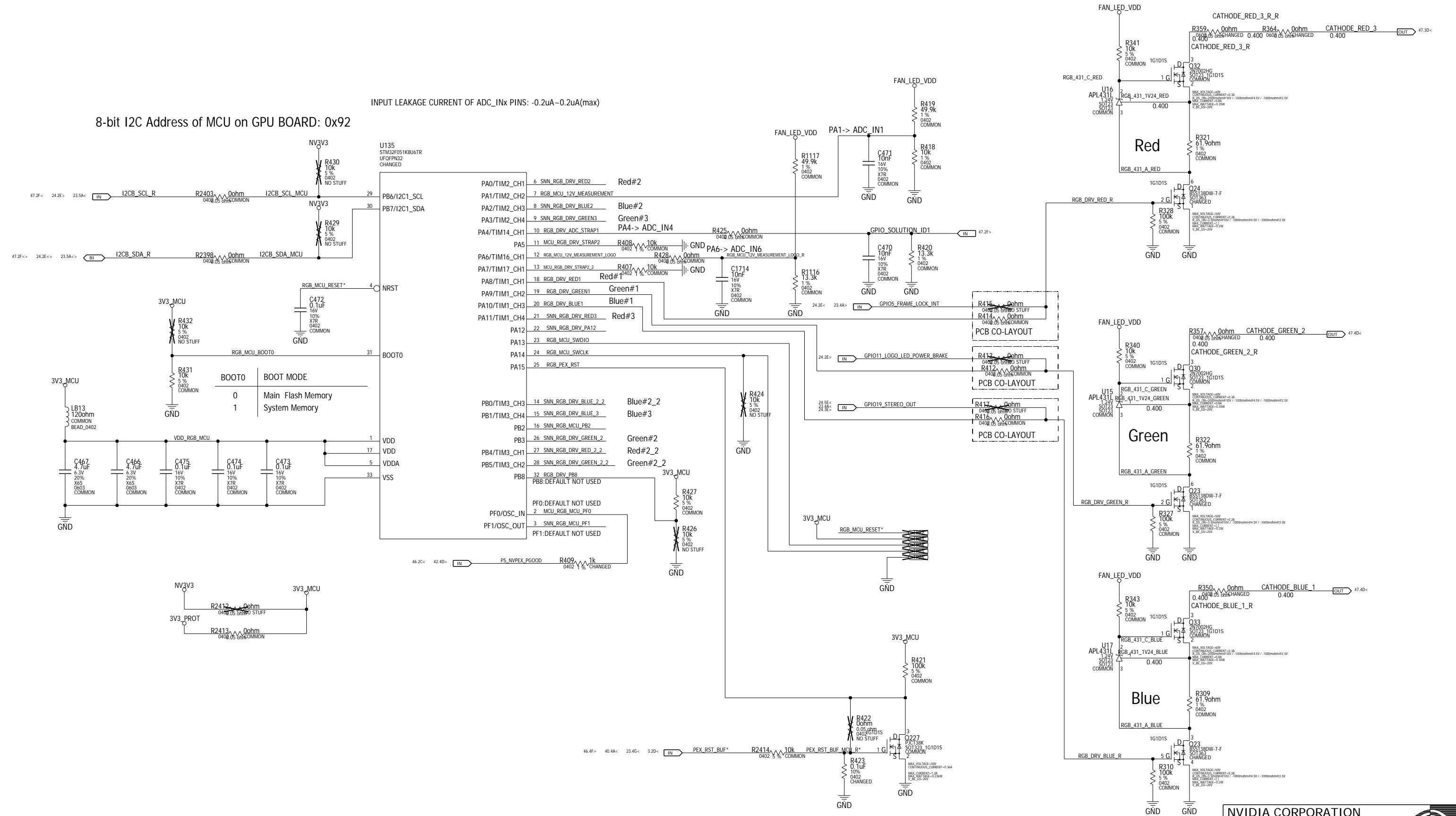
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NV_PN	600-1G160-0052-QS1		
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For ONE ZONE RGB/cable	
PIN SEQ	Pin Name
1	ID3
2	ID2
3	ID1
4	DRIVE3/R
5	DRIVE2/G
6	DRIVE1/B
7	12V
8	12V
9	FAN_PWM1
10	GND
11	FAN_TACH1
12	FAN_TACH2
13	GND
14	FAN_PWM2
15	12V



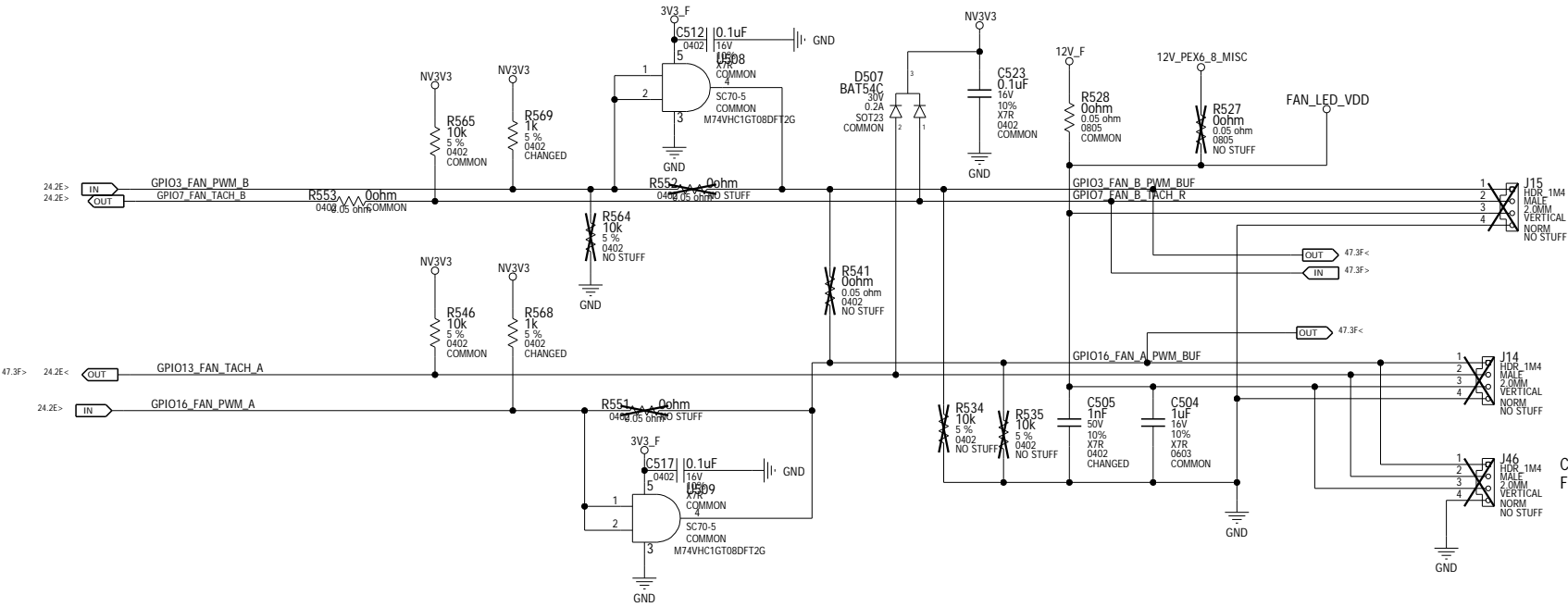
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Page48: LED DRIVER & Boost

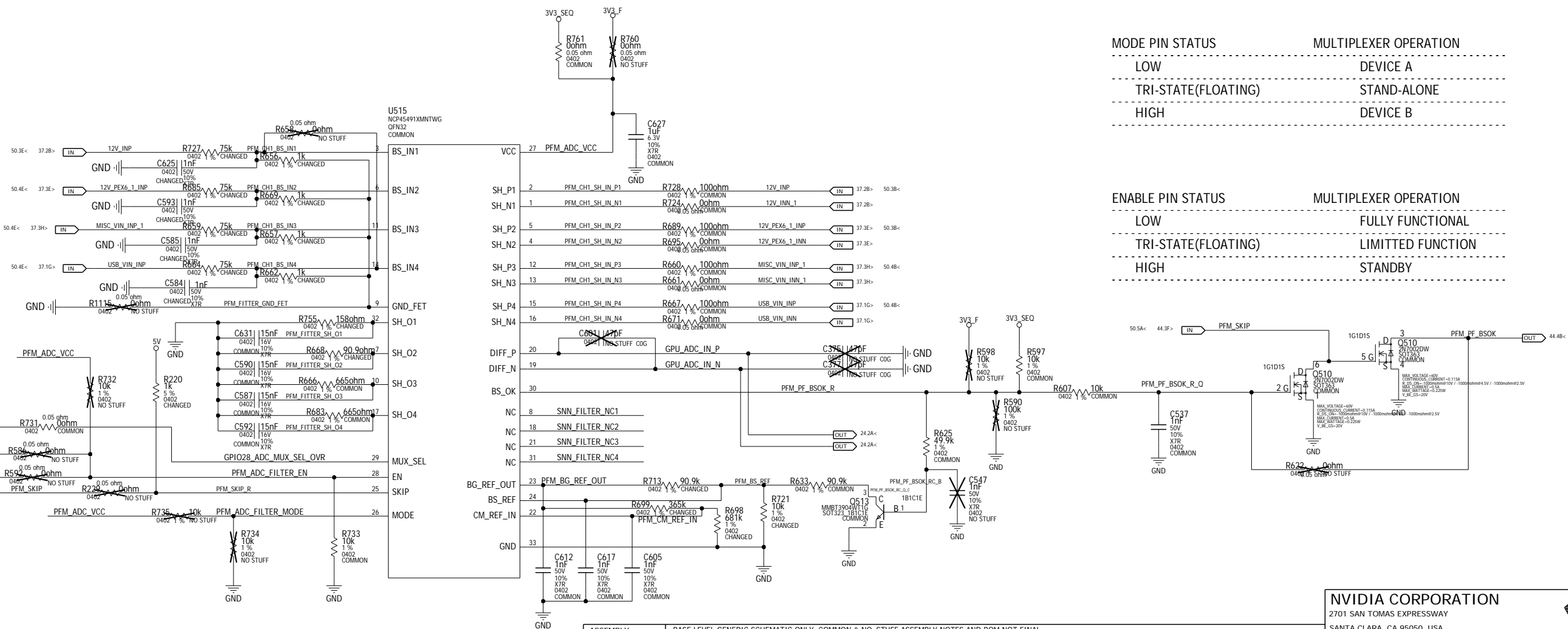


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MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

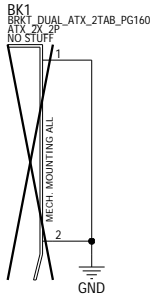
  

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

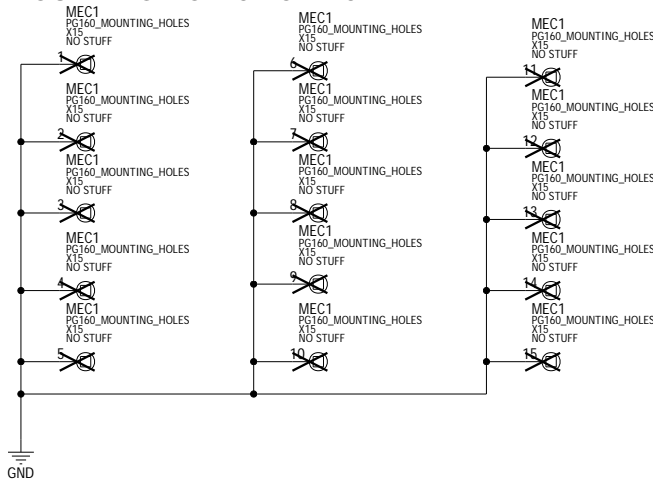
<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN	600-1G160-0052-QS1		
PCB REV	PG160-B02	PAGE	50 OF 52
BOM REV	A	DATE	30-JUL-2018

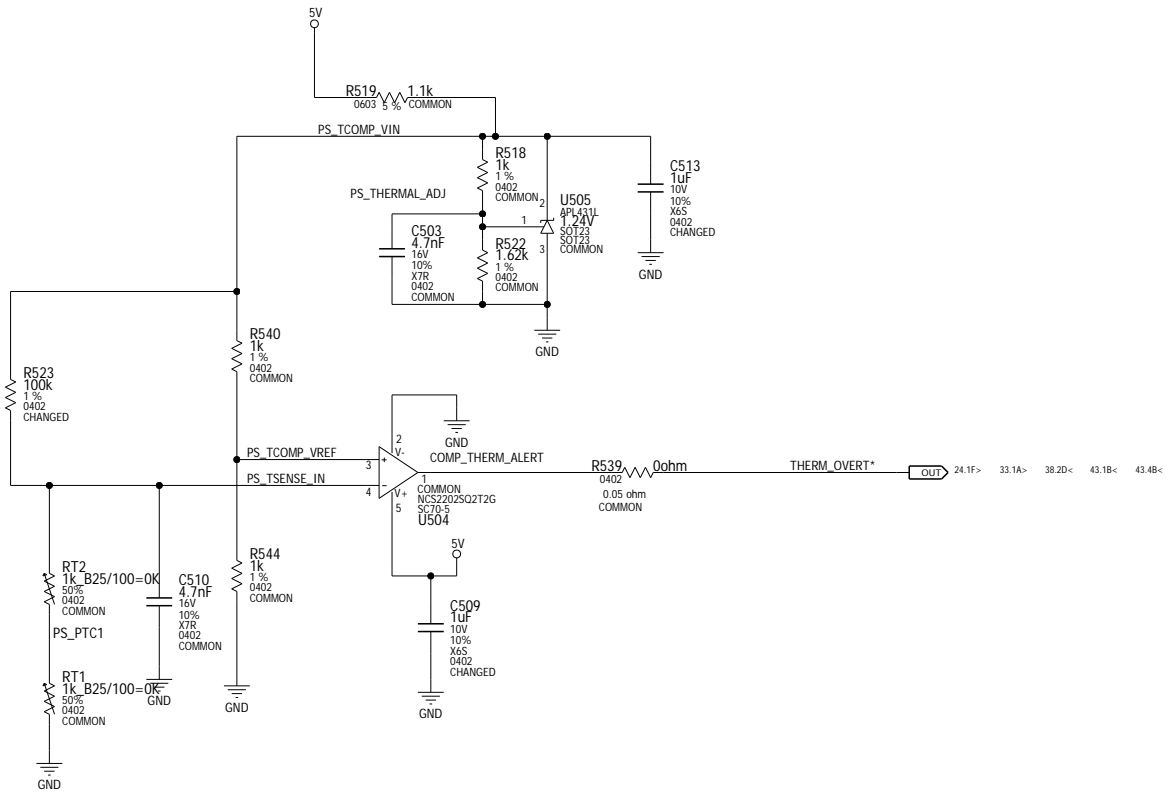
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Brackets:



MOUNTING HOLES FOR HS:





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