1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J207: MLB-A

LAST_MODIFICATION=Tue Oct 4 09:02:14 2016

J207_MLB_B SYNC VER 3.5.0

WIFI_MLB SYNC VER 0.29.0

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
5	0007236685	ENGINEERING RELEASED	2016-10-04

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-01015	1	SCHEM,MLB-A,(YN),J207	SCH1	CRITICAL	
820-00432	1	PCBF,MLB-A,(YN),J207	PCB1	CRITICAL	

SYNC_MASTER= SYNC_DATE=

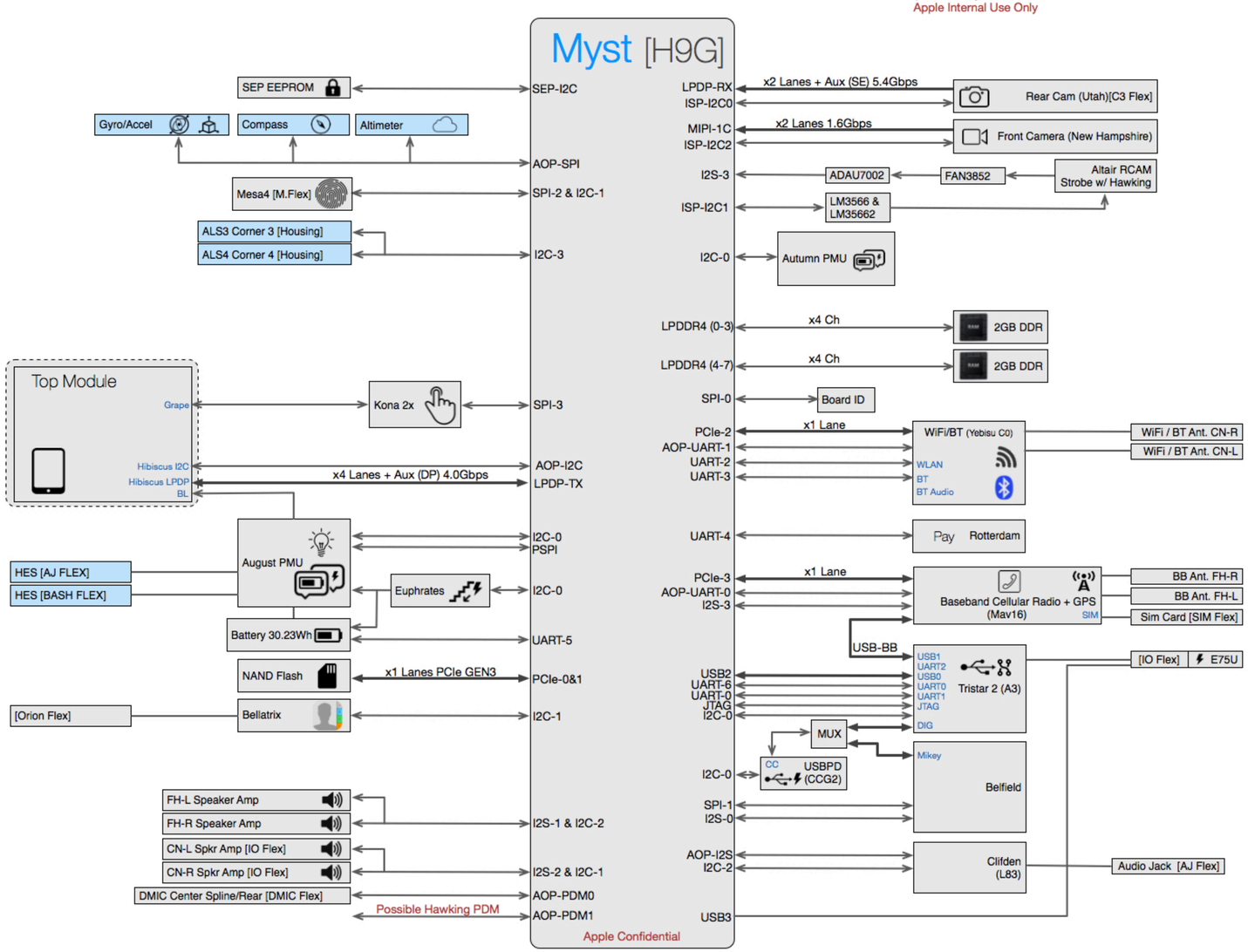
DRAWING TITLE

TABLE OF CONTENTS

SCHEM,MLB-A,(YN),J207

J208 P2 System Block Diagram

Updated: July 11, 2016
Apple Internal Use Only



SYNC_MASTER=MLB_B
SYNC_DATE=05/14/2016
PAGE TITLE

BLOCK DIAGRAM

CKPLUS WAIVE TABLE

CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-09232	1	CAN,TOUCH,MLB	TOUCH_FENCE	CRITICAL	
806-08286	1	CAN,RADIO,MLB_B	RADIO_FENCE	CRITICAL	MLB_B
806-08942	1	FENCE,AP,MLB	AP_FENCE	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR 639-01321 (MLB A BETTER)	EEEE_HFRC	CRITICAL	EEEE_MLB_A_BETTER
825-7691	1	EEEE FOR 639-03350 (MLB A EXTREME)	EEEE_HN82	CRITICAL	EEEE_MLB_A_EXTREME
825-7691	1	EEEE FOR 639-01325 (MLB A ULTIMATE)	EEEE_GPMM	CRITICAL	EEEE_MLB_A_ULTIMATE
825-7691	1	EEEE FOR 639-01327 (MLB A SUPREME)	EEEE_GPMN	CRITICAL	EEEE_MLB_A_SUPREME
825-7691	1	EEEE FOR 639-01322 (MLB B BETTER)	EEEE_HFR9	CRITICAL	EEEE_MLB_B_BETTER
825-7691	1	EEEE FOR 639-03349 (MLB B EXTREME)	EEEE_HN81	CRITICAL	EEEE_MLB_B_EXTREME
825-7691	1	EEEE FOR 639-01326 (MLB B ULTIMATE)	EEEE_GPMQ	CRITICAL	EEEE_MLB_B_ULTIMATE
825-7691	1	EEEE FOR 639-01328 (MLB B SUPREME)	EEEE_GPMV	CRITICAL	EEEE_MLB_B_SUPREME

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00172	1	IC,MYST	U0600	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S00173	343S00172		U0600	DIFF ASSEMBLY HOUSE

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S00103	2	IC,DRAM,SAMSUNG,FBGA480	U1600,U1700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S00104	333S00103		U1600,U1700	HYNIX DRAM
333S00105	333S00103		U1600,U1700	MICRON DRAM

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00118	1	IC,PMU,AUGUST,D2400AA,OTP-BE	U8100	CRITICAL	
343S00120	1	IC,PMU,AUTUMN,WLCSP121,OTP-BD	U7700	CRITICAL	

EUPHRATES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00121	1	IC,EUPHRATES,D2355A1,OTP-CD	U8500	CRITICAL	

NAND

BETTER FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00155	1	TOSHIBA,32GB,MLC,ULGA70,BETTER	U1800	CRITICAL	BETTER_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00160	335S00155	BETTER_PROD	U1800	HYNIX NAND

ULTIMATE FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00174	1	TOSHIBA,128GB,TLC,ULGA70,ULTIMATE	U1800	CRITICAL	ULTIMATE_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00165	335S00174	ULTIMATE_PROD	U1800	SANDISK NAND

SUPREME FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00188	1	TOSHIBA,256GB,TLC,ULGA70,SUPREME	U1800	CRITICAL	SUPREME_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00166	335S00188	SUPREME_PROD	U1800	SANDISK NAND

EXTREME FLASH CONFIGURATIONS

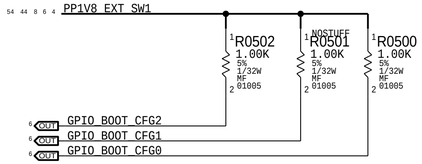
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00265	1	NAND,512GB,3DV2,ULGA70,XTREME	U1800	CRITICAL	EXTREME_PROD

SYNC_MASTER=MLB_B SYNC_DATE=08/26/2016

PAGE TITLE

BOM TABLES

BOOT CONFIG ID

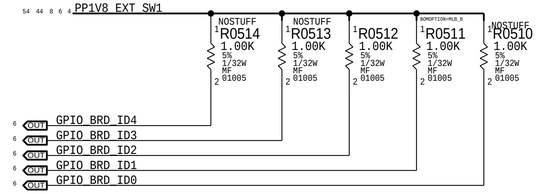


BOOT_CFG[3:0]	MODE
000	RESERVED
001	RESERVED
010	NVME0 X2
011	NVME0 X2 TEST
100	NVME0 X1
CURRENT SETTING ---> 101	NVME0 X1 TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID



BRD_ID[4-0]	
00100	J207 AP
00101	J207 DEV
00110	J208 AP
CURRENT SETTING ---> 00111	J208 DEV

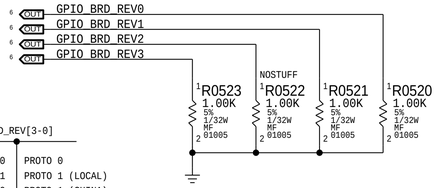
S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

RDAR//PROBLEM/24427656

BOARD REVISION

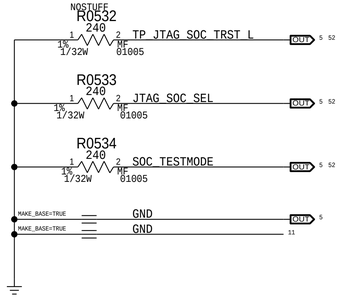
NOTE: STUFFING RESISTOR MEANS 0



BRD_REV[3-0]	
0000	PROTO 0
0001	PROTO 1 (LOCAL)
0010	PROTO 1 (CHINA)
0011	PROTO 2
CURRENT SETTING ---> 0100	EVT
0101	UNUSED
0110	UNUSED
0111	UNUSED
1000	UNUSED

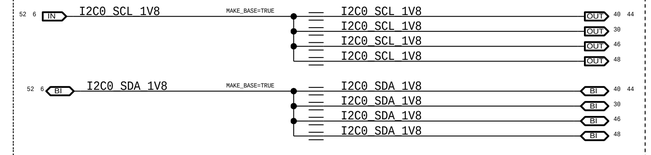
S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ



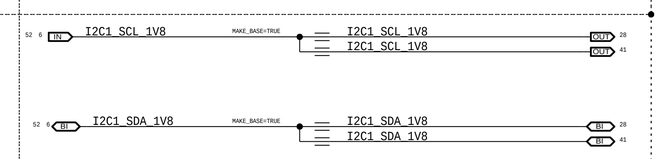
I2C0

DEVICE	8-BIT	7-BIT
AUGUST	0X78	0X3C
AUTUMN	0X80	0X40
TRISTAR	0X34	0X1A
EUPHRATES	0XEA	0X75
USB PD	0X24	0X12



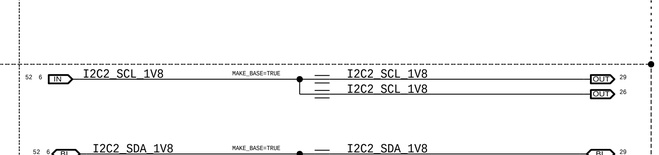
I2C1

DEVICE	8-BIT	7-BIT
SKR AMP CN R	0X64	0X32
SKR AMP CN L	0X62	0X31
BELLATRIX	0X26	0X13



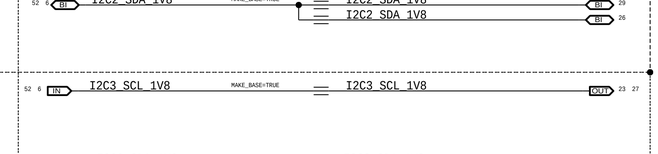
I2C2

DEVICE	8-BIT	7-BIT
SKR AMP FH R	0X64	0X32
SKR AMP FH L	0X62	0X31
CLIFDEN	0X90	0X48



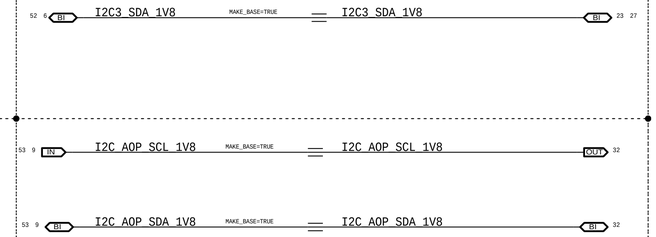
I2C3

DEVICE	8-BIT	7-BIT
ALS (FH-L)	0X52	0X29
ALS (FH-R)	0X72	0X39



AOP I2C

DEVICE	8-BIT	7-BIT
TCON(HIBISCUS)	0X18-0X27	
TCON MICRO	0XAC	0X56
TCON TEMP	0X48-0X4F	



SYNC_MASTER=MLB_B SYNC_DATE=08/26/2016

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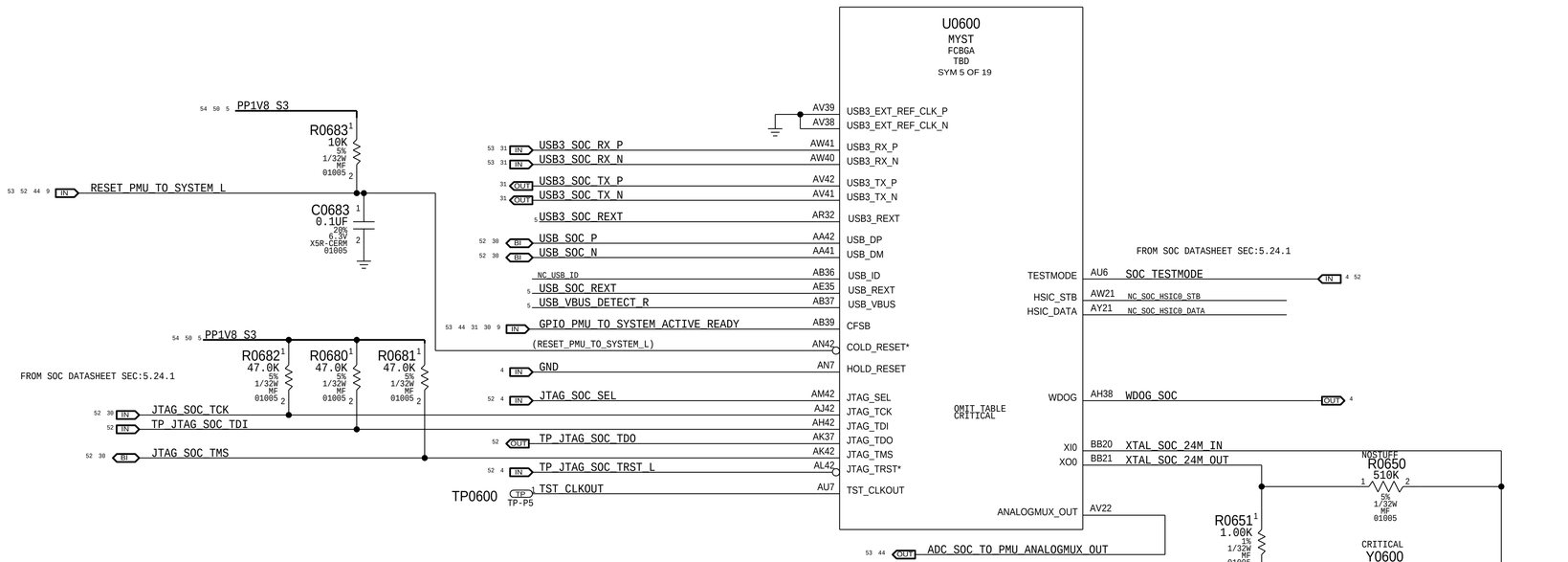
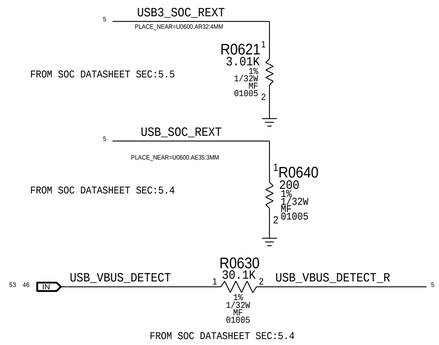
SOC: MISC & ALIASES

USB/JTAG/XTAL



USB SUPPORT



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0590	197S0591		Y0600	EPSON,24MHZ.XTAL
197S0588	197S0591		Y0600	TXC,24MHZ,XTAL

SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016
PAGE TITLE
SOC: MAIN

I2S/SPI/I2C

U0600 MYST FCBGA TBD SYM 17 OF 19 — OMIT TABLE CRITICAL

I2S0_BCLK	AY32	I2S0 SOC TO BELFIELD BCLK	OUT	53 26	
I2S0_DIN	BA33	I2S0 BELFIELD TO SOC DOUT	IN	53 26	
I2S0_DOUT	AW32	I2S0 SOC TO BELFIELD DOUT	OUT	53 26	
I2S0_LRCK	AW33	I2S0 SOC TO BELFIELD LRCK	OUT	53 26	
I2S0_MCK	BB32	I2S0 SOC TO BELFIELD MCLK R			
I2S1_BCLK	AP4	I2S1 SOC TO SPKRAMP FH BCLK	OUT	53 29	
I2S1_DIN	AP5	I2S1 SPKRAMP FH TO SOC DOUT	IN	53 29	
I2S1_DOUT	AP2	I2S1 SOC TO SPKRAMP FH DOUT	OUT	53 29	
I2S1_LRCK	AJ6	I2S1 SOC TO SPKRAMP FH LRCK	OUT	53 29	
I2S1_MCK	AN3	I2S1 SOC TO SPKRAMP FH MCLK R			
I2S2_BCLK	AY33	I2S2 SOC TO SPKRAMP CN BCLK	OUT	53 28	
I2S2_DIN	AU32	I2S2 SPKRAMP CN TO SOC DOUT	IN	53 28	
I2S2_DOUT	AY34	I2S2 SOC TO SPKRAMP CN DOUT	OUT	53 28	
I2S2_LRCK	AV32	I2S2 SOC TO SPKRAMP CN LRCK	OUT	53 28	
I2S2_MCK	BA32	I2S2 SOC TO SPKRAMP CN MCLK R			
I2S3_BCLK	AP3	I2S3 SOC TO HAWKING BCLK	OUT	53 22	
I2S3_DIN	AR4	I2S3 HAWKING TO SOC DOUT	IN	53 22	
I2S3_DOUT	AK7	NC_I2S3_DOUT			
I2S3_LRCK	AR5	I2S3 SOC TO HAWKING LRCK	OUT	53 22	
I2S3_MCK	AK1	GPIO_CODEC_TO_SOC_IRQ_L	IN	53 26	

I2S1 : FOREHEAD (J207)

I2S2 : CHIN (J120 / J207)

R0705 33 5% 1/32W MF 01005 — PLACE_NEAR=U0600.BB32:10MM
R0701 33 5% 1/32W MF 01005 — PLACE_NEAR=U0600.AN3:10MM
R0703 33 5% 1/32W MF 01005 — PLACE_NEAR=U0600.BA32:10MM

I2C0_SCL	AC42	I2C0_SCL_1V8	OUT	4 6 52	
I2C0_SDA	AD42	I2C0_SDA_1V8	BI	4 6 52	
I2C1_SCL	BB36	I2C1_SCL_1V8	OUT	4 6 52	
I2C1_SDA	BB33	I2C1_SDA_1V8	BI	4 6 52	
I2C2_SCL	AT1	I2C2_SCL_1V8	OUT	4 6 52	
I2C2_SDA	AP1	I2C2_SDA_1V8	BI	4 6 52	
I2C3_SCL	BB35	I2C3_SCL_1V8	OUT	4 6 52	
I2C3_SDA	BB37	I2C3_SDA_1V8	BI	4 6 52	

SPI0_MISO		GPIO_BRD_ID2	IN	4	AP7
SPI0_MOSI		GPIO_BRD_ID1	IN	4	BA3
SPI0_SCLK		GPIO_BRD_ID0	IN	4	AV7
SPI0_SSIN		GPIO_BRD_ID3	IN	4	AY5
SPI1_MISO	AT37	SPI_BELFIELD_MISO	IN	53 26	
SPI1_MOSI	AV34	SPI_BELFIELD_MOSI	OUT	53 26	
SPI1_SCLK	BA35	SPI_BELFIELD_SCLK	OUT	53 26	
SPI1_SSIN	AV33	SPI_BELFIELD_CS_L	OUT	53 26	
SPI2_MISO	AR36	SPI_MESA_MISO	IN	53 34	
SPI2_MOSI	AT39	SPI_MESA_MOSI	OUT	34	
SPI2_SCLK	AU34	SPI_MESA_SCLK_R			
SPI2_SSIN	AU33	GPIO_MESA_TO_SOC_IRQ	IN	52 34	
SPI3_MISO	AE41	SPI_SOC_TO_GRAPE_MISO	IN	53 19	
SPI3_MOSI	AE40	SPI_SOC_TO_GRAPE_MOSI_R			
SPI3_SCLK	AF42	SPI_SOC_TO_GRAPE_SCLK_R			
SPI3_SSIN	AE36	SPI_SOC_TO_GRAPE_CS_L	OUT	53 19	

SPI_MESA_SCLK — R0706 33 5% 1/32W MF 01005 — PLACE_NEAR=U0600.AU34:5MM
SPI_SOC_TO_GRAPE_MOSI — R0708 33 5% 1/32W MF 01005 — PLACE_NEAR=U0600.AE40:5MM
SPI_SOC_TO_GRAPE_SCLK — R0707 43.2 1% 1/32W MF 01005 — PLACE_NEAR=U0600.AF42:5MM

SEP_I2C_SCL	AR1	SEP_I2C_SCL_1V8		6	
SEP_I2C_SDA	AV5	SEP_I2C_SDA_1V8		6	
SEP_SPI0_MISO	AV6	NC_SEP_SPI0_MISO			
SEP_SPI0_MOSI	AU2	NC_SEP_SPI0_MOSI			
SEP_SPI0_SCLK	AU3	NC_SEP_SPI0_SCLK			
SOCHOT	AE42	SOCHOT1_SOC_TO_PMU_L	OUT	6 44 52	
DROOP	AE38	VCCMAIN_DROOP_PMU_TO_SOC_L	IN	6 44 52	
CPU_TRIGGER0	AD36	GPIO_PMU_TO_CPU_TRIGGER_0	IN	44 52	
CPU_TRIGGER1	AB38	GPIO_PMU_TO_CPU_TRIGGER_1	IN	44 52	
GPU_TRIGGER0	AC40	GPIO_PMU_TO_GPU_TRIGGER_0	IN	44 52	
GPU_TRIGGER1	AC39	GPIO_PMU_TO_GPU_TRIGGER_1	IN	44 52	

GPIO/UART/CLK

U0600 MYST FCBGA TBD SYM 18 OF 19 — OMIT TABLE CRITICAL

GPIO_0	AW4	NC_GPIO_ALS_C2_TO_SOC_IRQ_L			
GPIO_1	AG4	NC_GPIO_SOC_TO_BB_RADIO_ON_L	OUT	51	
GPIO_2	AF3	GPIO_SOC_TO_NAND_FW_STRAP	OUT	17	
GPIO_3	AJ5	NC_GPIO_BB_TO_SOC_RESET_DET_L	IN	51	
GPIO_4	AJ4	NC_GPIO_BB_IPC	BI	51	
GPIO_5	AV3	GPIO_SOC_TO_GRAPE_RESET_L	OUT	53 20 19	
GPIO_6	AW6	GPIO_GRAPE_TO_SOC_IRQ_L	IN	53 19	
GPIO_7	AW3	GPIO_ALS_C3_TO_SOC_IRQ_L	IN	52 23	
GPIO_8	AH2	NC_GPIO_BB_TO_SOC_GPS_SYNC	IN	51	
GPIO_9	AG7	NC_GPIO_SOC_TO_BB_RESET_L	OUT	51	
GPIO_10	AJ2	GPIO_SOC_TO_USB3_XBAR_DIS_PULSE_L	OUT	31	
GPIO_11	AJ3	GPIO_SOC_TO_USB3_XBAR_EN_PULSE_L	OUT	31	
GPIO_12	AP6	SWD_USBPD_SWDIO	BI	48	
GPIO_13	AR3	GPIO_BELFIELD_TO_SOC_IRQ_L	OUT	52 26	
GPIO_14	AU4	GPIO_SOC_TO_ROTTERDAM_DWLD_REQ	OUT	51	
GPIO_15	AL7	NC_GPIO_SOC_TO_BB_COREDUMP	OUT	51	
GPIO_16	AY4	GPIO_USBPD_TO_SOC_IRQ_L	IN	48	
GPIO_17	AR2	GPIO_SOC_TO_LED_DRIVER_EN	OUT	52 25	
GPIO_18	AW1	GPIO_BOOT_CFG0	IN	4	
GPIO_19	AT4	GPIO_SOC_TO_ROTTERDAM_DEV_WAKE	OUT	51	
GPIO_20	AU5	GPIO_SOC_TO_ROTTERDAM_EN	OUT	51	
GPIO_21	BB7	GPIO_ALS_C4_TO_SOC_IRQ_L	IN	52 27	
GPIO_22	AC36	GPIO_TS_TO_SOC_TO_PMU_IRQ	IN	52 44 38	
GPIO_23	AW7	GPIO_SOC_TO_AUTUMN_REARCAM_ADJ	OUT	48	
GPIO_24	AY6	GPIO_SOC_TO_USBPD_RESET_L	OUT	48	
GPIO_25	AR7	GPIO_BOOT_CFG1	IN	4	
GPIO_26	AT6	GPIO_FORCE_DFU	IN	52 50	
GPIO_27	AL6	TP_GPIO_DFU_STATUS	OUT	53	
GPIO_28	AT7	GPIO_BOOT_CFG2	IN	4	
GPIO_29	AY2	GPIO_BRD_ID4	IN	4	
GPIO_30	AY3	GPIO_SOC_TO_BT_TO_GRAPE_TS_SYNC	OUT	53 51 20 19	
GPIO_31	AF39	GPIO_EUPHRATES_TO_SOC_TO_PMU_IRQ_L	IN	53 46 44	
GPIO_32	AD41	GPIO_ORION_TO_SOC_TO_PMU_IRQ	IN	52 44 43	
GPIO_33	AR6	GPIO_SOC_TO_1V8_TOUCH_EXT_SW_ON	OUT	52 47	
GPIO_34	BB5	GPIO_BRD_REV3	IN	4	
GPIO_35	BB4	GPIO_BRD_REV2	IN	4	
GPIO_36	AV2	GPIO_BRD_REV1	IN	4	
GPIO_37	BB6	GPIO_BRD_REV0	IN	4	
GPIO_38	AM6	NCX			

BOOT CFG<1> — FORCE_DFU — DFU_STATUS — BOOT CFG<2> — BRD ID<4>

UART0_RXD	BB38	UART_DEBUG_TO_SOC_TX	IN	30 52	
UART0_TXD	BB39	UART_SOC_TO_DEBUG_TX	OUT	30 52	
UART1_CTS*	AE7	NC_UART_GPS_TO_SOC_RTS_L	NO_TEST=1		
UART1_RTS*	AE2	NC_UART_SOC_TO_GPS_RTS_L	NO_TEST=1		
UART1_RXD	AE5	NC_UART_GPS_TO_SOC_TX	NO_TEST=1		
UART1_TXD	AE6	NC_UART_SOC_TO_GPS_TX	NO_TEST=1		
UART2_CTS*	AV35	UART_WLAN_TO_SOC_RTS_L	IN	51 53	
UART2_RTS*	AT36	UART_SOC_TO_WLAN_RTS_L	OUT	51 53	
UART2_RXD	AY38	UART_WLAN_TO_SOC_TX	IN	51 53	
UART2_TXD	BA38	UART_SOC_TO_WLAN_TX	OUT	51 53	
UART3_CTS*	AY37	UART_BT_TO_SOC_RTS_L	IN	51 53	
UART3_RTS*	AY36	UART_SOC_TO_BT_RTS_L	OUT	51	
UART3_RXD	AR37	UART_BT_TO_SOC_TX	IN	51 53	
UART3_TXD	AW36	UART_SOC_TO_BT_TX	OUT	51	
UART4_CTS*	AF2	UART_ROTTERDAM_TO_SOC_RTS_L	IN	51	
UART4_RTS*	AF7	UART_SOC_TO_ROTTERDAM_RTS_L	OUT	51	
UART4_RXD	AE3	UART_ROTTERDAM_TO_SOC_TX	IN	51	
UART4_TXD	AE4	UART_SOC_TO_ROTTERDAM_TX	OUT	51	
UART5_RTXD	AU35	UART_BATT_HDQ	BI	44 49 52	
UART6_RXD	AD39	UART_ACC_TO_SOC_TX	IN	30 52	
UART6_TXD	AD40	UART_SOC_TO_ACC_TX	OUT	30 52	
UART7_RXD	BA5	GPIO_SOC_TO_SPKRAMP_RESET_L	OUT	28 29	
UART7_TXD	BA4	NC_GPIO_ALS_C1_TO_SOC_IRQ_L			

NOTE: CLK32K_OUT CAN GENERATE UPTO 24MHZ
PLEASE USE 155S0610 FOR DESENSE DOE

CLK32K_OUT — BB34
NAND_SYS_CLK — AE1

R0731 33 5% 1/32W MF 01005 — PLACE_NEAR=U0600.BB34:5MM — CLK_GRAPE_24MHZ — CLK_SOC_TO_GRAPE_24MHZ OUT 19
R0730 33 5% 1/32W MF 01005 — PLACE_NEAR=U0600.AE1:5MM — CLK_NAND_24MHZ — CLK_SOC_TO_NAND_24MHZ OUT 17

TMR32_PWM0	BA39	GPIO_SOC_TO_WLAN_DEVICE_WAKE	OUT	51 53
TMR32_PWM1	BA36	SWD_USBPD_SWCLK	OUT	48
TMR32_PWM2	AY39	GPIO_WLAN_TO_SOC_ATSP_R	IN	51

SEP EEPROM

APN:335S0946

54 PP1V8_EXT_SW1 — C0700 1.0UF 20% 6.3V X5R 0201-1 — VCC (A1)
U0701 M34128-FCS6_P/T SCL WLCSP SDA — CRITICAL — VSS (B2)
6 SEP_I2C_SCL_1V8 (B1) — SEP_I2C_SDA_1V8 (A2) 6

54 52 43 PP1V8_ALWAYS
54 44 8 6 4 PP1V8_EXT_SW1
R0790 47.0K 5% 1/32W MF 01005
R0791 47.0K 5% 1/32W MF 01005
52 44 6 VCCMAIN_DROOP_PMU_TO_SOC_L
52 44 6 SOCHOT1_SOC_TO_PMU_L

I2C PULL UPS

54 44 8 6 4 PP1V8_EXT_SW1

R0750 1.00K 5% 1/32W MF 01005
R0751 1.00K 5% 1/32W MF 01005
R0752 2.2K 5% 1/32W MF 01005
R0753 2.2K 5% 1/32W MF 01005
R0754 2.2K 5% 1/32W MF 01005
R0755 2.2K 5% 1/32W MF 01005
R0758 1.00K 5% 1/32W MF 01005
R0759 1.00K 5% 1/32W MF 01005
R0756 2.2K 5% 1/32W MF 01005
R0757 2.2K 5% 1/32W MF 01005

52 6 4 I2C0_SCL_1V8
52 6 4 I2C0_SDA_1V8
52 6 4 I2C1_SCL_1V8
52 6 4 I2C1_SDA_1V8
52 6 4 I2C2_SCL_1V8
52 6 4 I2C2_SDA_1V8
52 6 4 I2C3_SCL_1V8
52 6 4 I2C3_SDA_1V8
6 SEP_I2C_SCL_1V8
6 SEP_I2C_SDA_1V8

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00066	335S0946		U0701	ON SEMI EEPROM ALT

SYNC_MASTER=MLB_B — SYNC_DATE=07/29/2016
PAGE TITLE:
SOC: I/OS

LPDP RX/TX

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CAMERA

AW11	LPDPRX_BYP_CLK_P	
AV11	LPDPRX_BYP_CLK_N	
AV8	LPDPRX_AUX_D0_P	53 23 BI LPDP_SOC_TO_UT_AUX
AV9	LPDPRX_AUX_D1_P	NC_LPDPRX_AUX1
AW9	LPDPRX_AUX_D2_P	NC_LPDPRX_AUX2
AU12	LPDPRX_AUX_D3_P	NC_LPDPRX_AUX3
AV12	LPDPRX_AUX_D4_P	NC_LPDPRX_AUX4
BA8	LPDPRX_RX_D0_P	53 23 IN LPDP_UT_TO_SOC_DATA_P<0>
AY8	LPDPRX_RX_D0_N	53 23 IN LPDP_UT_TO_SOC_DATA_N<0>
BB9	LPDPRX_RX_D1_P	53 23 IN LPDP_UT_TO_SOC_DATA_P<1>
BA9	LPDPRX_RX_D1_N	53 23 IN LPDP_UT_TO_SOC_DATA_N<1>
BA10	LPDPRX_RX_D2_P	53 GND
AY10	LPDPRX_RX_D2_N	53 GND
BB11	LPDPRX_RX_D3_P	53 GND
BA11	LPDPRX_RX_D3_N	53 GND
BA12	LPDPRX_RX_D4_P	53 GND
AY12	LPDPRX_RX_D4_N	53 GND
AU10	LPDPRX_RCAL_P	7 PPVDD_S1_FIXED_SOC
AV10	LPDPRX_RCAL_N	7 LPDPRX_RCAL_NEG
AR15	LPDPRX_EXT_C	NC_LPDPRX_EXT_C

DISPLAY

Y41	LPDP_SOC_TO_TCON_DATA_P<0>	LPDP_TX0P / LPDP_TX0N, OUT 33
Y40	LPDP_SOC_TO_TCON_DATA_N<0>	
Y38	LPDP_SOC_TO_TCON_DATA_P<1>	LPDP_TX1P / LPDP_TX1N, OUT 33
Y37	LPDP_SOC_TO_TCON_DATA_N<1>	
W42	LPDP_SOC_TO_TCON_DATA_P<2>	LPDP_TX2P / LPDP_TX2N, OUT 33
W41	LPDP_SOC_TO_TCON_DATA_N<2>	
W39	LPDP_SOC_TO_TCON_DATA_P<3>	LPDP_TX3P / LPDP_TX3N, OUT 33
W38	LPDP_SOC_TO_TCON_DATA_N<3>	
V41	NC_LPDP_TX4_P	LPDP_TX4P / LPDP_TX4N
V40	NC_LPDP_TX4_N	
V38	NC_LPDP_TX5_P	LPDP_TX5P / LPDP_TX5N
V37	NC_LPDP_TX5_N	
U42	LPDP_SOC_TO_TCON_AUX_P	LPDP_AUX_P / LPDP_AUX_N, BI 33
U41	LPDP_SOC_TO_TCON_AUX_N	
AA34	LPDP_CAL_DRV_OUT	LPDP_CAL_DRV_OUT / LPDP_CAL_VSS_EXT
AA33	LPDP_CAL_VSS_EXT	
AG40	LPDP_TCON_TO_SOC_HPD	EDP_HPD, IN 33 52
AC37	NC_DP_WAKEUP	DP_WAKEUP

R0890 100 1% 1/32W MF 01005 — PLACE_NEAR=U0600.AA34:4MM
C0890 20PF 5% 16V NP0-C0G-CERM 01005 — PLACE_NEAR=U0600.AA34:4MM

C0892 MUST BE NOSTUFF PER SEG

MIPI/ISP

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ISP / SENSOR

AH6	ISP_I2C0_SCL	23 7 OUT ISP_UT_CAM_SCL
AH7	ISP_I2C0_SDA	23 7 BI ISP_UT_CAM_SDA
AL1	ISP_I2C1_SCL	52 25 7 OUT ISP_STB_SCL
AL2	ISP_I2C1_SDA	52 25 7 BI ISP_STB_SDA
AH1	ISP_I2C2_SCL	24 7 OUT ISP_FRONT_CAM_SCL
AL3	ISP_I2C2_SDA	24 7 BI ISP_FRONT_CAM_SDA
AL4	ISP_I2C3_SCL	NC_ISP_I2C3_SCL
AL5	ISP_I2C3_SDA	NC_ISP_I2C3_SDA
BA29	MIPI0C_DPCLK	53 GND
BB29	MIPI0C_DNCLK	53 GND
AY28	MIPI0C_DPDATA0	53 GND
BA28	MIPI0C_DNDATA0	53 GND
AY30	MIPI0C_DPDATA1	53 GND
BA30	MIPI0C_DNDATA1	53 GND
AY26	MIPI1C_DPCLK	53 GND
BA26	MIPI1C_DNCLK	53 GND
BA27	MIPI1C_DPDATA0	53 GND
BB27	MIPI1C_DNDATA0	53 GND
BA25	MIPI1C_DPDATA1	53 GND
BB25	MIPI1C_DNDATA1	53 GND

AK3	SENSOR_INT	NC_SENSOR_INT
AK4	SENSOR4_RST	NC_SENSOR4_RST
AH5	SENSOR3_RST	NC_SENSOR3_RST
AJ1	SENSOR2_CLK	NC_SENSOR2_CLK
AG6	SENSOR2_RST	NC_SENSOR2_RST
AM1	SENSOR0_CLK	CLK_SOC_TO_REAR_CAM_12MHZ_R
AM3	SENSOR0_RST	GPIO_SOC_TO_REAR_CAM_SHTDWN_L, OUT 23
AM4	SENSOR0_ISTRB	NC_SENSOR0_ISTRB
AN4	SENSOR0_XSHUTDOWN	NC_GPIO_SOC_TO_BB_MESA_ON, OUT 51
AN1	SENSOR1_CLK	CLK_SOC_TO_FRONT_CAM_12MHZ_R
AM2	SENSOR1_RST	GPIO_SOC_TO_FRONT_CAM_SHTDWN_L, OUT 24
AH4	SENSOR1_ISTRB	GPIO_BTN_VOL_UP_L (USE INTERNAL PU), IN 23
AJ7	SENSOR1_XSHUTDOWN	GPIO_BTN_VOL_DOWN_L (USE INTERNAL PU), IN 23
BA23	MIPI2C_DPCLK	MIPI_NH_CAM_TO_SOC_CLK_P, IN 24 53
BB23	MIPI2C_DNCLK	MIPI_NH_CAM_TO_SOC_CLK_N, IN 24 53
AY22	MIPI2C_DPDATA0	MIPI_NH_CAM_TO_SOC_DATA_P<0>, IN 24 53
BA22	MIPI2C_DNDATA0	MIPI_NH_CAM_TO_SOC_DATA_N<0>, IN 24 53
AY24	MIPI2C_DPDATA1	MIPI_NH_CAM_TO_SOC_DATA_P<1>, IN 24 53
BA24	MIPI2C_DNDATA1	MIPI_NH_CAM_TO_SOC_DATA_N<1>, IN 24 53
AT25	MIPI0C_REXT	GND, 53
AT24	MIPI1C_REXT	GND, 53
AT22	MIPI2C_REXT	MIPI2C_REXT

R0812 33 1/32W 5% MF 01005 — PLACE_NEAR=U0600.AM1:5MM
C0812 15PF 5% 16V NP0-C0G-CERM 01005
R0811 33 1/32W 5% MF 01005 — PLACE_NEAR=U0600.AN1:5MM
C0811 15PF 5% 16V NP0-C0G-CERM 01005
R0800 200 1% 1/32W MF 01005 — PLACE_NEAR=U0600.AT22:6MM

SYNOPSYS MIPI DPHY DATABOOK

LPDP RX CAL

54 13 PPVDD_S1_FIXED_SOC
7 PPVDD_S1_FIXED_SOC — PLACE_NEAR=U0600.AU10:4MM
R0891 300 1% 1/32W MF 01005-1
7 LPDPRX_RCAL_NEG — PLACE_NEAR=U0600.AV10:4MM
C0891 100PF 5% 16V NP0-C0G 01005

ISP I2C PULL UPS

54 24 PP1V8_SW1_CAM
R0805 1.00K 5% 1/32W MF 01005
R0803 1.00K 5% 1/32W MF 01005
24 7 ISP_FRONT_CAM_SCL
24 7 ISP_FRONT_CAM_SDA

54 23 7 PP1V8_SW1_CAM
R0804 1.00K 5% 1/32W MF 01005
R0802 1.00K 5% 1/32W MF 01005
23 7 ISP_UT_CAM_SCL
23 7 ISP_UT_CAM_SDA

54 23 7 PP1V8_SW1_CAM
R0850 1.00K 5% 1/32W MF 01005
R0851 1.00K 5% 1/32W MF 01005
52 25 7 ISP_STB_SCL
52 25 7 ISP_STB_SDA

SYNC_MASTER=MLB_B
SYNC_DATE=09/19/2016
PAGE TITLE

SOC: LPDP & MIPI

PCIE

PER PCISIG SPEC, AC COUPLING CAPS SHOULD BE BETWEEN
176 NF AND 265 NF FOR GEN1/2/3

NAND

- 53 17 IN PCIE_NAND_TO_SOC_TX_P<0> → AV14 PCIE_RX0_P
- 53 17 IN PCIE_NAND_TO_SOC_TX_N<0> → AW14 PCIE_RX0_N
- 53 17 OUT PCIE_SOC_TO_NAND_TX_P<0> → C0930 (CRITICAL, GND_VOID=TRUE, 0.22UF, 10%, 01005, CER-X5R, 6.3V) → PCIE_SOC_TO_NAND_TX_C_P<0> → BA14 PCIE_TX0_P
- 53 17 OUT PCIE_SOC_TO_NAND_TX_N<0> → C0931 (CRITICAL, GND_VOID=TRUE, 0.22UF, 10%, 01005, CER-X5R, 6.3V) → PCIE_SOC_TO_NAND_TX_C_N<0> → BB14 PCIE_TX0_N
- 53 17 OUT PCIE_SOC_TO_NAND_REFCLK_P → AU24 PCIE_REF_CLK0_P
- 53 17 OUT PCIE_SOC_TO_NAND_REFCLK_N → AV24 PCIE_REF_CLK0_N
- 17 8 IN PCIE_NAND_TO_SOC_CLKREQ_L → AG3 PCIE_CLKREQ0*
- 17 8 OUT PCIE_SOC_TO_NAND_RESET_L → AF6 PCIE_PERST0*

U0600

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BASEBAND

- PCIE_RX3_P AU17 ← NC_PCIE_BB_TO_SOC_TX_P IN 51
- PCIE_RX3_N AV17 ← NC_PCIE_BB_TO_SOC_TX_N IN 51
- PCIE_TX3_P AY17 → NC_PCIE_SOC_TO_BB_TX_C_P OUT 51
- PCIE_TX3_N BA17 → NC_PCIE_SOC_TO_BB_TX_C_N OUT 51
- PCIE_REF_CLK3_P AV27 → NC_PCIE_SOC_TO_BB_REFCLK_P OUT 51
- PCIE_REF_CLK3_N AW27 → NC_PCIE_SOC_TO_BB_REFCLK_N OUT 51
- PCIE_CLKREQ3* AG1 ← NC_PCIE_BB_TO_SOC_CLKREQ_L IN 51
- PCIE_PERST3* AF1 → NC_PCIE_SOC_TO_BB_RESET_L OUT 51

AC COUPLING CAPS ARE IN RADIO PAGES

- NC_PCIE_RX1_P → AU15 PCIE_RX1_P
- NC_PCIE_RX1_N → AV15 PCIE_RX1_N
- PCIE_RX4_P AV18 NC_PCIE_RX4_P
- PCIE_RX4_N AW18 NC_PCIE_RX4_N
- NC_PCIE_TX1_P → AY15 PCIE_TX1_P
- NC_PCIE_TX1_N → BA15 PCIE_TX1_N
- PCIE_TX4_P BA18 NC_PCIE_TX4_P
- PCIE_TX4_N BB18 NC_PCIE_TX4_N
- NC_PCIE_REF_CLK1_P → AV25 PCIE_REF_CLK1_P
- NC_PCIE_REF_CLK1_N → AW25 PCIE_REF_CLK1_N
- PCIE_REF_CLK4_P AU28 NC_PCIE_REF_CLK4_P
- PCIE_REF_CLK4_N AV28 NC_PCIE_REF_CLK4_N
- NC_PCIE_CLKREQ1 → AH3 PCIE_CLKREQ1*
- NC_PCIE_PERST1 → AF4 PCIE_PERST1*
- PCIE_CLKREQ4* AV4 NC_PCIE_CLKREQ4
- PCIE_PERST4* AM5 NC_PCIE_PERST4

54 44 6 4 PP1V8_EXT_SW1

R0930 47.0K 5% 1/32W MF 01005 (1 → 2)

R0940 47.0K 5% 1/32W MF 01005 (1 → 2)

- 17 8 PCIE_NAND_TO_SOC_CLKREQ_L
- 53 51 8 PCIE_WLAN_TO_SOC_CLKREQ_L

BB HAS A 100K PU ON THEIR SIDE

WLAN/BT

- 53 51 IN PCIE_WLAN_TO_SOC_TX_P → AV16 PCIE_RX2_P
- 53 51 IN PCIE_WLAN_TO_SOC_TX_N → AW16 PCIE_RX2_N
- 51 OUT PCIE_SOC_TO_WLAN_TX_P → C0940 (CRITICAL, GND_VOID=TRUE, 0.1UF, 10%, 01005, CER-X5R, 6.3V) → PCIE_SOC_TO_WLAN_TX_C_P → BA16 PCIE_TX2_P
- 51 OUT PCIE_SOC_TO_WLAN_TX_N → C0941 (CRITICAL, GND_VOID=TRUE, 0.1UF, 10%, 01005, CER-X5R, 6.3V) → PCIE_SOC_TO_WLAN_TX_C_N → BB16 PCIE_TX2_N
- 53 51 OUT PCIE_SOC_TO_WLAN_REFCLK_P → AU26 PCIE_REF_CLK2_P
- 53 51 OUT PCIE_SOC_TO_WLAN_REFCLK_N → AV26 PCIE_REF_CLK2_N
- PCIE_RX5_P AU19 NC_PCIE_RX5_P
- PCIE_RX5_N AV19 NC_PCIE_RX5_N
- PCIE_TX5_P AY19 NC_PCIE_TX5_P
- PCIE_TX5_N BA19 NC_PCIE_TX5_N
- PCIE_REF_CLK5_P AV29 NC_PCIE_REF_CLK5_P
- PCIE_REF_CLK5_N AW29 NC_PCIE_REF_CLK5_N
- 53 51 8 IN PCIE_WLAN_TO_SOC_CLKREQ_L → AU1 PCIE_CLKREQ2*
- 53 51 8 OUT PCIE_SOC_TO_WLAN_RESET_L → AV1 PCIE_PERST2*
- PCIE_CLKREQ5* AM7 GPIO_SOC_TO_BELFIELD_RESET_L OUT 26
- PCIE_PERST5* AT3 GPIO_SOC_TO_CODEC_RESET_L OUT 26

- 17 8 PCIE_SOC_TO_NAND_RESET_L
- 53 51 8 PCIE_SOC_TO_WLAN_RESET_L

R0941 100K 5% 1/32W MF 01005 (1 → 2)

R0931 100K 5% 1/32W MF 01005 (1 → 2)

AT17 PCIE_EXT_REF_CLK_P
AT18 PCIE_EXT_REF_CLK_N

S3E_RESET* AF5 GPIO_SOC_TO_NAND_RESET_L OUT 17

PCIE_REXT AR18 PCIE_SOC_REXT
PLACE_NEAR=U0600.AR18:4MM

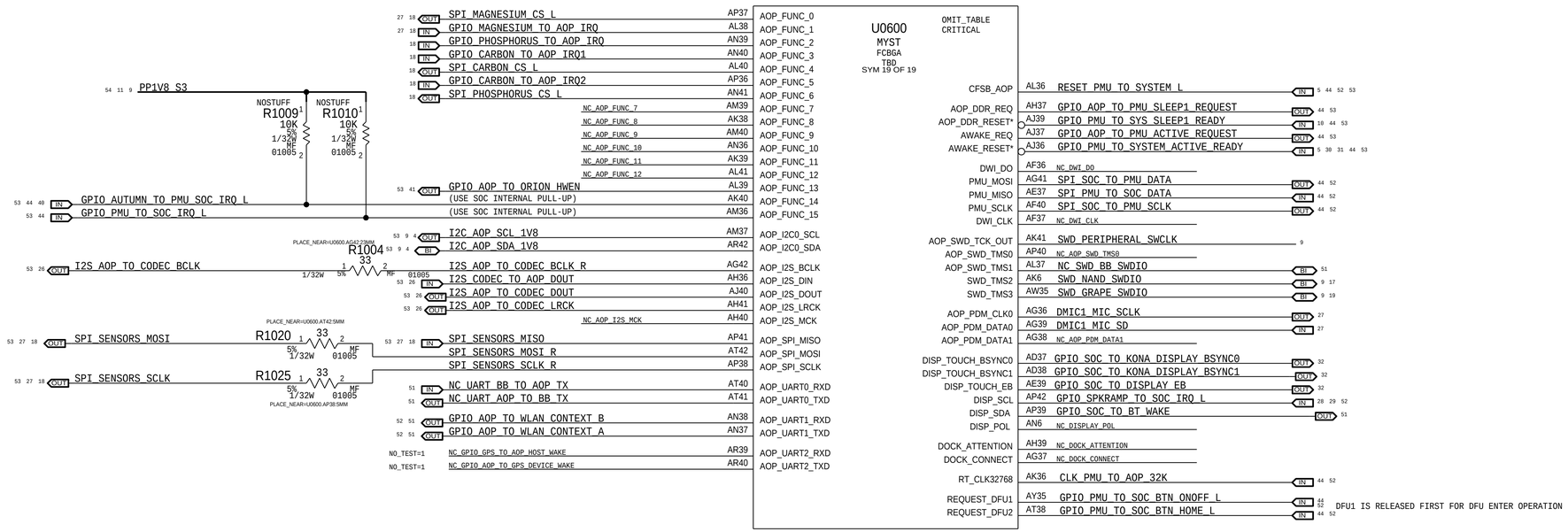
R0921 200 1% 1/32W MF 01005 (1 → 2)

SYNOPSYS PCIE 3.0 PHY DATABOOK

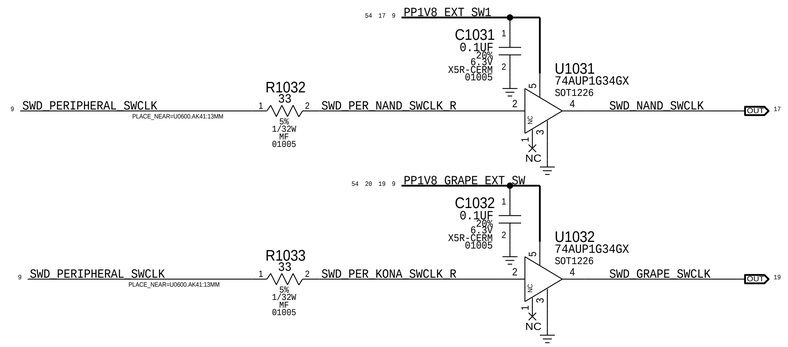
SYNC_MASTER=MLB_B
SYNC_DATE=08/26/2016
PAGE TITLE

SOC: PCIE

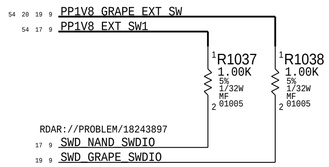
AOP/MISC



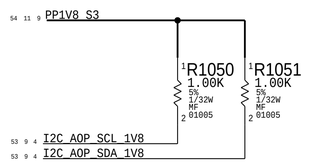
THESE GATES HAVE BACKPOWER PROTECTION



SWDIO PULL-UPS:



AOP I2C PULL-UPS:



SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

SOC: AOP

DDR [0:3]

OMIT_TABLE
CRITICAL
U0600
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DDR0_CA<0>	U7	DDR0_CA_0	DDR1_CA_0	J7	DDR1_CA<0>
DDR0_CA<1>	U8	DDR0_CA_1	DDR1_CA_1	J8	DDR1_CA<1>
DDR0_CA<2>	AA8	DDR0_CA_2	DDR1_CA_2	N8	DDR1_CA<2>
DDR0_CA<3>	AB6	DDR0_CA_3	DDR1_CA_3	P6	DDR1_CA<3>
DDR0_CA<4>	AB8	DDR0_CA_4	DDR1_CA_4	P8	DDR1_CA<4>
DDR0_CA<5>	AC8	DDR0_CA_5	DDR1_CA_5	R8	DDR1_CA<5>
DDR0_CK_P	Y3	DDR0_CK_P	DDR1_CK_P	M3	DDR1_CK_P
DDR0_CK_N	Y2	DDR0_CK_N	DDR1_CK_N	M2	DDR1_CK_N
DDR0_CKE	Y6	DDR0_CKE	DDR1_CKE	M6	DDR1_CKE
DDR0_CS	W7	DDR0_CS	DDR1_CS	L7	DDR1_CS
DDR0_DM<0>	V5	DDR0_DMI_0	DDR1_DMI_0	K5	DDR1_DM<0>
DDR0_DM<1>	AB5	DDR0_DMI_1	DDR1_DMI_1	P5	DDR1_DM<1>
DDR0_DQ<0>	U1	DDR0_DQ_0	DDR1_DQ_0	J1	DDR1_DQ<0>
DDR0_DQ<1>	U3	DDR0_DQ_1	DDR1_DQ_1	J3	
DDR0_DQ<2>	U4		DDR1_DQ_2	J4	DDR1_DQ<2>
DDR0_DQ<3>	U5	DDR0_DQ_3	DDR1_DQ_3	J5	
DDR0_DQ<4>	W1	DDR0_DQ_4	DDR1_DQ_4	L1	
DDR0_DQ<5>	W3	DDR0_DQ_5	DDR1_DQ_5	L3	DDR1_DQ<5>
DDR0_DQ<6>	W4	DDR0_DQ_6	DDR1_DQ_6	L4	
DDR0_DQ<7>	W5	DDR0_DQ_7	DDR1_DQ_7	L5	
DDR0_DQ<8>	AC5	DDR0_DQ_8	DDR1_DQ_8	R5	DDR1_DQ<8>
DDR0_DQ<9>	AC4	DDR0_DQ_9	DDR1_DQ_9	R4	
	AC3	DDR0_DQ_10	DDR1_DQ_10	R3	
DDR0_DQ<11>	AC1		DDR1_DQ_11	R1	
	AA5	DDR0_DQ_12	DDR1_DQ_12	N5	
DDR0_DQ<13>	AA4	DDR0_DQ_13	DDR1_DQ_13	N4	
	AA3	DDR0_DQ_14	DDR1_DQ_14	N3	
DDR0_DQ<15>	AA1	DDR0_DQ_15	DDR1_DQ_15	N1	DDR1_DQ<15>
DDR0_DQS_P<0>	V2	DDR0_DQS_P_0	DDR1_DQS_P_0	K2	DDR1_DQS_P<0>
DDR0_DQS_N<0>	V1	DDR0_DQS_N_0	DDR1_DQS_N_0	K1	DDR1_DQS_N<0>
DDR0_DQS_P<1>	AB2	DDR0_DQS_P_1	DDR1_DQS_P_1	P2	DDR1_DQS_P<1>
DDR0_DQS_N<1>	AB1	DDR0_DQS_N_1	DDR1_DQS_N_1	P1	DDR1_DQS_N<1>
	AA7	DDR0_RESET*	DDR1_RESET*	N7	
GPIO_PMU_TO_SYS_SLEEP1_READY	W8	DDR0_RET*	DDR1_RET*	L8	GPIO_PMU_TO_SYS_SLEEP1_READY
DDR0_RREF	AD1	DDR0_RREF	DDR1_RREF	T1	DDR1_RREF
SYS_ALIVE	Y8	DDR0_SYS_ALIVE	DDR1_SYS_ALIVE	M8	SYS_ALIVE

	C5	DDR2_CA_0	DDR3_CA_0	G16	DDR3_CA<0>
	B5	DDR2_CA_1	DDR3_CA_1	H16	DDR3_CA<1>
	F6	DDR2_CA_2	DDR3_CA_2	H12	DDR3_CA<2>
	D4	DDR2_CA_3	DDR3_CA_3	F11	DDR3_CA<3>
	D3		DDR3_CA_4	H11	
DDR2_CA<5>	G6	DDR2_CA_5	DDR3_CA_5	H10	DDR3_CA<5>
DDR2_CK_P	D2	DDR2_CK_P	DDR3_CK_P	C13	DDR3_CK_P
DDR2_CK_N	D1	DDR2_CK_N	DDR3_CK_N	B13	DDR3_CK_N
DDR2_CKE	C4	DDR2_CKE	DDR3_CKE	F13	DDR3_CKE
DDR2_CS	A5	DDR2_CS	DDR3_CS	G14	DDR3_CS
DDR2_DM<0>	E7	DDR2_DMI_0	DDR3_DMI_0	E15	DDR3_DM<0>
DDR2_DM<1>	F5	DDR2_DMI_1	DDR3_DMI_1	E11	DDR3_DM<1>
	A8		DDR3_DQ_0	A16	
DDR2_DQ<1>	C8	DDR2_DQ_1	DDR3_DQ_1	C16	DDR3_DQ<1>
DDR2_DQ<2>	D8	DDR2_DQ_2	DDR3_DQ_2	D16	DDR3_DQ<2>
DDR2_DQ<3>	E8	DDR2_DQ_3	DDR3_DQ_3	E16	DDR3_DQ<3>
DDR2_DQ<4>	A6	DDR2_DQ_4	DDR3_DQ_4	A14	DDR3_DQ<4>
DDR2_DQ<5>	C6	DDR2_DQ_5	DDR3_DQ_5	C14	DDR3_DQ<5>
DDR2_DQ<6>	D6	DDR2_DQ_6	DDR3_DQ_6	D14	DDR3_DQ<6>
DDR2_DQ<7>	E6	DDR2_DQ_7	DDR3_DQ_7	E14	DDR3_DQ<7>
DDR2_DQ<8>	G5	DDR2_DQ_8	DDR3_DQ_8	E10	DDR3_DQ<8>
DDR2_DQ<9>	G4		DDR3_DQ_9	D10	DDR3_DQ<9>
	G3	DDR2_DQ_10	DDR3_DQ_10	C10	
	G1	DDR2_DQ_11	DDR3_DQ_11	A10	DDR3_DQ<11>
DDR2_DQ<12>	E5	DDR2_DQ_12	DDR3_DQ_12	E12	DDR3_DQ<12>
	E4	DDR2_DQ_13	DDR3_DQ_13	D12	DDR3_DQ<13>
DDR2_DQ<14>	E3	DDR2_DQ_14	DDR3_DQ_14	C12	DDR3_DQ<14>
DDR2_DQ<15>	E1		DDR3_DQ_15	A12	DDR3_DQ<15>
DDR2_DQS_P<0>	B7		DDR3_DQS_P_0	B15	DDR3_DQS_P<0>
DDR2_DQS_N<0>	A7		DDR3_DQS_N_0	A15	DDR3_DQS_N<0>
DDR2_DQS_P<1>	F2		DDR3_DQS_P_1	B11	DDR3_DQS_P<1>
	F1		DDR3_DQS_N_1	A11	
NC_SOC_DDR2_RESET_L	F7	DDR2_RESET*	DDR3_RESET*	G12	
GPIO_PMU_TO_SYS_SLEEP1_READY	H6	DDR2_RET*	DDR3_RET*	H14	GPIO_PMU_TO_SYS_SLEEP1_READY
DDR2_RREF	H1	DDR2_RREF	DDR3_RREF	A9	DDR3_RREF
SYS_ALIVE	G7	DDR2_SYS_ALIVE	DDR3_SYS_ALIVE	H13	SYS_ALIVE

DDR [4:7]

OMIT_TABLE
CRITICAL
U0600
MYST
FCBGA
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SYM 2 OF 19

DDR4_CA<0>	G25	DDR4_CA_0	DDR5_CA_0	G33	DDR5_CA<0>
DDR4_CA<1>	H25	DDR4_CA_1	DDR5_CA_1	H33	DDR5_CA<1>
DDR4_CA<2>	H21	DDR4_CA_2	DDR5_CA_2	H29	DDR5_CA<2>
DDR4_CA<3>	F20	DDR4_CA_3	DDR5_CA_3	F28	DDR5_CA<3>
DDR4_CA<4>	H20	DDR4_CA_4	DDR5_CA_4	H28	DDR5_CA<4>
DDR4_CA<5>	H19	DDR4_CA_5		H27	DDR5_CA<5>
DDR4_CK_P	C22	DDR4_CK_P	DDR5_CK_P	C30	DDR5_CK_P
DDR4_CK_N	B22	DDR4_CK_N	DDR5_CK_N	B30	DDR5_CK_N
DDR4_CKE	F22	DDR4_CKE	DDR5_CKE	F30	DDR5_CKE
DDR4_CS	G23	DDR4_CS	DDR5_CS	G31	DDR5_CS
DDR4_DM<0>	E24	DDR4_DMI_0	DDR5_DMI_0	E32	DDR5_DM<0>
DDR4_DM<1>	E20	DDR4_DMI_1	DDR5_DMI_1	E28	DDR5_DM<1>
DDR4_DQ<0>	A25	DDR4_DQ_0	DDR5_DQ_0	A33	DDR5_DQ<0>
DDR4_DQ<1>	C25	DDR4_DQ_1	DDR5_DQ_1	C33	DDR5_DQ<1>
DDR4_DQ<2>	D25	DDR4_DQ_2	DDR5_DQ_2	D33	DDR5_DQ<2>
DDR4_DQ<3>	E25	DDR4_DQ_3	DDR5_DQ_3	E33	DDR5_DQ<3>
DDR4_DQ<4>	A23	DDR4_DQ_4	DDR5_DQ_4	A31	DDR5_DQ<4>
DDR4_DQ<5>	C23	DDR4_DQ_5	DDR5_DQ_5	C31	DDR5_DQ<5>
DDR4_DQ<6>	D23	DDR4_DQ_6	DDR5_DQ_6	D31	DDR5_DQ<6>
DDR4_DQ<7>	E23	DDR4_DQ_7	DDR5_DQ_7	E31	DDR5_DQ<7>
DDR4_DQ<8>	E19	DDR4_DQ_8	DDR5_DQ_8	E27	DDR5_DQ<8>
DDR4_DQ<9>	D19	DDR4_DQ_9	DDR5_DQ_9	D27	DDR5_DQ<9>
DDR4_DQ<10>	C19	DDR4_DQ_10	DDR5_DQ_10	C27	DDR5_DQ<10>
DDR4_DQ<11>	A19	DDR4_DQ_11	DDR5_DQ_11	A27	DDR5_DQ<11>
DDR4_DQ<12>	E21	DDR4_DQ_12	DDR5_DQ_12	E29	DDR5_DQ<12>
DDR4_DQ<13>	D21	DDR4_DQ_13	DDR5_DQ_13	D29	DDR5_DQ<13>
DDR4_DQ<14>	C21	DDR4_DQ_14	DDR5_DQ_14	C29	DDR5_DQ<14>
DDR4_DQ<15>	A21	DDR4_DQ_15	DDR5_DQ_15	A29	DDR5_DQ<15>
DDR4_DQS_P<0>	B24	DDR4_DQS_P_0	DDR5_DQS_P_0	B32	DDR5_DQS_P<0>
DDR4_DQS_N<0>	A24	DDR4_DQS_N_0	DDR5_DQS_N_0	A32	DDR5_DQS_N<0>
DDR4_DQS_P<1>	B20	DDR4_DQS_P_1		B28	DDR5_DQS_P<1>
DDR4_DQS_N<1>	A20	DDR4_DQS_N_1		A28	DDR5_DQS_N<1>
	G21	DDR4_RESET*		G29	NC_SOC_DDR5_RESET_L
GPIO_PMU_TO_SYS_SLEEP1_READY	H23	DDR4_RET*		H31	GPIO_PMU_TO_SYS_SLEEP1_READY
DDR4_RREF	A18	DDR4_RREF	DDR5_RREF	A26	DDR5_RREF
SYS_ALIVE	H22	DDR4_SYS_ALIVE	DDR5_SYS_ALIVE	H30	SYS_ALIVE

DDR6_CA<0>	C38	DDR6_CA_0	DDR7_CA_0	J36	DDR7_CA<0>
DDR6_CA<1>	B38	DDR6_CA_1	DDR7_CA_1	J35	DDR7_CA<1>
DDR6_CA<2>	F37	DDR6_CA_2	DDR7_CA_2	N35	DDR7_CA<2>
DDR6_CA<3>	D39	DDR6_CA_3		P37	DDR7_CA<3>
DDR6_CA<4>	D40	DDR6_CA_4	DDR7_CA_4	P35	DDR7_CA<4>
DDR6_CA<5>	G37	DDR6_CA_5	DDR7_CA_5	R35	DDR7_CA<5>
DDR6_CK_P	D41	DDR6_CK_P	DDR7_CK_P	M40	DDR7_CK_P
DDR6_CK_N	D42	DDR6_CK_N	DDR7_CK_N	M41	DDR7_CK_N
DDR6_CKE	C39	DDR6_CKE	DDR7_CKE	M37	DDR7_CKE
DDR6_CS	A38	DDR6_CS	DDR7_CS	L36	DDR7_CS
DDR6_DM<0>	E36	DDR6_DMI_0	DDR7_DMI_0	K38	DDR7_DM<0>
DDR6_DM<1>	F38	DDR6_DMI_1	DDR7_DMI_1	P38	DDR7_DM<1>
DDR6_DQ<0>	A35	DDR6_DQ_0		J42	DDR7_DQ<0>
DDR6_DQ<1>	C35	DDR6_DQ_1	DDR7_DQ_1	J40	DDR7_DQ<1>
DDR6_DQ<2>	D35	DDR6_DQ_2	DDR7_DQ_2	J39	DDR7_DQ<2>
DDR6_DQ<3>	E35	DDR6_DQ_3	DDR7_DQ_3	J38	DDR7_DQ<3>
DDR6_DQ<4>	A37	DDR6_DQ_4	DDR7_DQ_4	L42	DDR7_DQ<4>
DDR6_DQ<5>	C37	DDR6_DQ_5	DDR7_DQ_5	L40	DDR7_DQ<5>
DDR6_DQ<6>	D37	DDR6_DQ_6	DDR7_DQ_6	L39	DDR7_DQ<6>
DDR6_DQ<7>	E37	DDR6_DQ_7	DDR7_DQ_7	L38	DDR7_DQ<7>
DDR6_DQ<8>	G38	DDR6_DQ_8	DDR7_DQ_8	R38	DDR7_DQ<8>
DDR6_DQ<9>	G39	DDR6_DQ_9		R39	DDR7_DQ<9>
DDR6_DQ<10>	G40	DDR6_DQ_10	DDR7_DQ_10	R40	DDR7_DQ<10>
DDR6_DQ<11>	G42	DDR6_DQ_11	DDR7_DQ_11	R42	DDR7_DQ<11>
DDR6_DQ<12>	E38	DDR6_DQ_12	DDR7_DQ_12	N38	DDR7_DQ<12>
DDR6_DQ<13>	E39	DDR6_DQ_13	DDR7_DQ_13	N39	DDR7_DQ<13>
DDR6_DQ<14>	E40	DDR6_DQ_14	DDR7_DQ_14	N40	DDR7_DQ<14>
DDR6_DQ<15>	E42	DDR6_DQ_15	DDR7_DQ_15	N42	DDR7_DQ<15>
DDR6_DQS_P<0>	B36	DDR6_DQS_P_0	DDR7_DQS_P_0	K41	DDR7_DQS_P<0>
DDR6_DQS_N<0>	A36	DDR6_DQS_N_0	DDR7_DQS_N_0	K42	DDR7_DQS_N<0>
DDR6_DQS_P<1>	F41	DDR6_DQS_P_1		P41	DDR7_DQS_P<1>
DDR6_DQS_N<1>	F42	DDR6_DQS_N_1	DDR7_DQS_N_1	P42	DDR7_DQS_N<1>
GPIO_DDR6_RESET_L	F36	DDR6_RESET*	DDR7_RESET*	N36	GPIO_DDR7_RESET_L
GPIO_PMU_TO_SYS_SLEEP1_READY	H37	DDR6_RET*	DDR7_RET*	L35	GPIO_PMU_TO_SYS_SLEEP1_READY
DDR6_RREF	H42	DDR6_RREF	DDR7_RREF	T42	DDR7_RREF
SYS_ALIVE	G36	DDR6_SYS_ALIVE	DDR7_SYS_ALIVE	M35	SYS_ALIVE

PP1V1_S1_EXT_SW

R1100	240 1% 1/32W MF 01005	DDR0_RREF PLACE_NEAR=U0600.AD1:5MM
R1110	240 1% 1/32W MF 01005	DDR1_RREF PLACE_NEAR=U0600.T1:5MM
R1120	240 1% 1/32W MF 01005	DDR2_RREF PLACE_NEAR=U0600.H1:5MM
	240 1% 1/32W MF 01005	DDR3_RREF PLACE_NEAR=U0600.A9:5MM
R1140	240 1% 1/32W MF 01005	DDR4_RREF PLACE_NEAR=U0600.A18:5MM
R1150	240 1% 1/32W MF 01005	DDR5_RREF PLACE_NEAR=U0600.A26:5MM
R1160	240 1% 1/32W MF 01005	DDR6_RREF
R1170	01005	DDR7_RREF PLACE_NEAR=U0600.T42:5MM

SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016
PAGE TITLE

SOC: DDR

DDR PWR

1.2V/1.8V

VDD12_PLL_CPU: 1.2V @ 7MA
VDD12_PLL_SOC: 1.2V @ 4MA
VDD12_PLL_GPU: 1.2V @ 7MA
VDD12_PLL_LPDP: 1.2V @ 9MA
VDD12_PCIE_REFBUF: 1.2V @ 48MA
VDD12_LPDP_TX: 1.2V @ 45MA
VDD12_LPDP_RX: 1.2V @ 55MA
VDD12_USB3: 1.2V @ 25MA

VDD18_ADP: 1.8V @ TBDMA
VDD18_USB: 1.8V @ 17MA
VDD18_TSADC: 1.8V @ 10.4MA
VDDIO18_GRP: 1.8V @ TBDMA
VDD18_MIPI: 1.8V @ 2MA
VDD18_XTAL: 1.8V @ 2MA
VDD18_LPOSC: 1.8V @ 1MA
VDD18_FMON: 1.8V @ 1MA
VDD18_PCIE: 1.8V @ 81.7MA
VDD33_USB: 3.3V @ 5MA

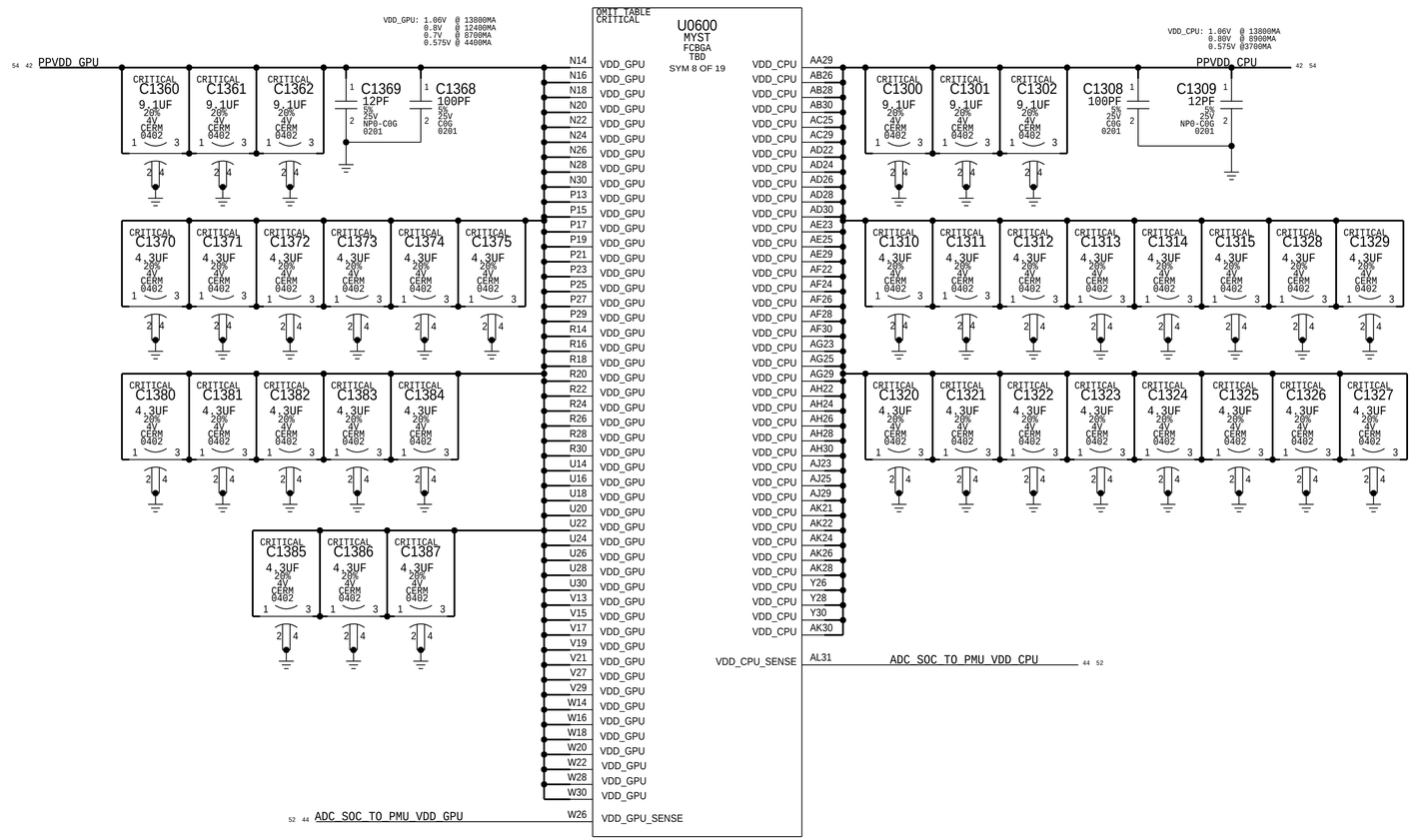
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00032	138S0831		C1221 & MORE	RDAR://PROBLEM/19974064
138S00049	138S0831		C1221 & MORE	RDAR://PROBLEM/19974064
138S00006	138S0835		C1201 & MORE	RDAR://PROBLEM/26931418

SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016
PAGE TITLE

SOC: POWER (IO)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00056	138S1100		C1300, ETC	QUALIFIED IN J127

CPU/GPU



SYNC_MASTER=MLB_B SYNC_DATE=07/29/2010

PAGE TITLE

SOC: POWER (CPU, GPU)

CPU/GPU SRAM

54 PPVDD_GPU_SRAM

VDD_GPU_SRAM: 1.06V @1400MA

C1470 CRITICAL 4.3UF 20% 4V CERM 0402
C1471 CRITICAL 4.3UF 20% 4V CERM 0402
C1451 CRITICAL 4.3UF 20% 4V CERM 0402
C1453 CRITICAL 4.3UF 20% 4V CERM 0402

C1478 100PF 5% 25V C0G 0201
C1479 12PF 5% 25V NP0-C0G 0201

OMIT_TABLE
CRITICAL

U0600
MYST
FCBGA
TBD
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M13	VDD_GPU_SRAM	VDD_CPU_SRAM	AA27
M15	VDD_GPU_SRAM	VDD_CPU_SRAM	AC23
M17	VDD_GPU_SRAM	VDD_CPU_SRAM	AC27
M19	VDD_GPU_SRAM	VDD_CPU_SRAM	AC30
M21	VDD_GPU_SRAM	VDD_CPU_SRAM	AE24
M23	VDD_GPU_SRAM	VDD_CPU_SRAM	AE27
M25	VDD_GPU_SRAM	VDD_CPU_SRAM	AE30
M27	VDD_GPU_SRAM	VDD_CPU_SRAM	AG24
M29	VDD_GPU_SRAM	VDD_CPU_SRAM	AG27
T13	VDD_GPU_SRAM	VDD_CPU_SRAM	AG30
T15	VDD_GPU_SRAM	VDD_CPU_SRAM	AH21
T17	VDD_GPU_SRAM	VDD_CPU_SRAM	AJ24
T19	VDD_GPU_SRAM	VDD_CPU_SRAM	AJ27
T21	VDD_GPU_SRAM	VDD_CPU_SRAM	AK25
T23	VDD_GPU_SRAM	VDD_CPU_SRAM	AK27
T25	VDD_GPU_SRAM	VDD_CPU_SRAM	AK29
T27	VDD_GPU_SRAM		
T29	VDD_GPU_SRAM		
W27	VDD_GPU_SRAM		
W29	VDD_GPU_SRAM		
Y13	VDD_GPU_SRAM		
Y15	VDD_GPU_SRAM		
Y17	VDD_GPU_SRAM		
Y19	VDD_GPU_SRAM		
Y21	VDD_GPU_SRAM		

VDD_CPU_SRAM: 1.6V @ 3000MA

C1450 CRITICAL 4.3UF 20% 4V CERM 0402
C1410 CRITICAL 4.3UF 20% 4V CERM 0402
C1452 CRITICAL 4.3UF 20% 4V CERM 0402
C1407 CRITICAL 4.3UF 20% 4V CERM 0402

C1459 12PF 5% 25V NP0-C0G 0201
C1458 100PF 5% 25V C0G 0201

PPVDD_CPU_SRAM 54

C1472 CRITICAL 4.3UF 20% 4V CERM 0402
C1473 CRITICAL 4.3UF 20% 4V CERM 0402
C1463 CRITICAL 4.3UF 20% 4V CERM 0402

VDD_FIXED_CPU: 0.8V @ 6MA
VDD_FIXED_PCIE:0.8V @ 290.1MA
VDD_FIXED_PCIE_REFBUF: 0.8V @ 4MA
VDD_FIXED_USB: 0.8V @ 6.6MA
VDD_FIXED_USB3: 0.8V @ 89.4MA
VDD_FIXED_USB3: 0.8V @ 89.4MA
VDD_FIXED_PLL_SOC: 0.8V @ 10MA
VDD_FIXED_PLL_GPU: 0.8V @ 6MA
VDD_FIXED_PLL_DDR: 0.8V @ 4MA
VDD_FIXED_MIPI: 0.8V @ 10MA
VDD_FIXED_PLL_LPDP: 0.8V @ 2MA
VDD_FIXED_LPDP_TX: 0.8V @ 13.2MA
VDD_FIXED_LPDP_RX: 0.8V @ 5.2MA

SOC/FIXED

54 7 PPVDD_S1_FIXED_SOC

VDD_FIXED: 0.8V @ 4840MA

C1477 10UF 20% 6.3V CERM-X5R 0402-9
C1476 10UF 20% 6.3V CERM-X5R 0402-9

C1400 CRITICAL 4.3UF 20% 4V CERM 0402
C1402 CRITICAL 4.3UF 20% 4V CERM 0402
C1405 CRITICAL 4.3UF 20% 4V CERM 0402
C1411 CRITICAL 4.3UF 20% 4V CERM 0402

C1401 CRITICAL 4.3UF 20% 4V CERM 0402
C1474 CRITICAL 4.3UF 20% 4V CERM 0402
C1475 CRITICAL 4.3UF 20% 4V CERM 0402
C1403 CRITICAL 4.3UF 20% 4V CERM 0402
C1404 CRITICAL 0.47UF 20% 6.3V CERM 0402

C1408 2.2UF 20% 6.3V X5R-CERM 0201
C1413 2.2UF 20% 6.3V X5R-CERM 0201
C1412 2.2UF 20% 6.3V X5R-CERM 0201
C1406 12PF 5% 25V NP0-C0G 0201

C1480 CRITICAL 4.3UF 20% 4V CERM 0402
C1481 CRITICAL 4.3UF 20% 4V CERM 0402
C1482 CRITICAL 4.3UF 20% 4V CERM 0402
C1484 CRITICAL 4.3UF 20% 4V CERM 0402

C1485 CRITICAL 4.3UF 20% 4V CERM 0402
C1486 CRITICAL 4.3UF 20% 4V CERM 0402
C1488 CRITICAL 4.3UF 20% 4V CERM 0402

C148E 100PF 5% 25V C0G 0201

OMIT_TABLE
CRITICAL

U0600
MYST
FCBGA
TBD
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AA12	VDD_FIXED	VDD_FIXED_PLL_DDR0	J6
AA14	VDD_FIXED	VDD_FIXED_PLL_DDR1	F9
AA16	VDD_FIXED	VDD_FIXED_PLL_DDR2	F16
AA18	VDD_FIXED	VDD_FIXED_PLL_DDR3	F25
AA20	VDD_FIXED	VDD_FIXED_PLL_DDR4	F33
AA22	VDD_FIXED	VDD_FIXED_PLL_DDR5	F34
AA24	VDD_FIXED	VDD_FIXED_PLL_DDR6	J37
AB11	VDD_FIXED	VDD_FIXED_PLL_DDR7	
AB13	VDD_FIXED		
AB15	VDD_FIXED		
AB17	VDD_FIXED		
AB19	VDD_FIXED	VDD_FIXED_PLL_GPU	AJ18
AB21	VDD_FIXED	VDD_FIXED_PLL_LPDP	AE32
AB23	VDD_FIXED	VDD_FIXED_PLL_SOC	AK17
AB25	VDD_FIXED	VDD_FIXED_PLL_SOC	AK18
AC12	VDD_FIXED	VDD_FIXED_CPU	AD21
AC14	VDD_FIXED	VDD_FIXED_LPDP_RX	AN14
AC16	VDD_FIXED	VDD_FIXED_LPDP_RX	AN16
AC18	VDD_FIXED	VDD_FIXED_LPDP_TX	AA32
AC20	VDD_FIXED	VDD_FIXED_LPDP_TX	AC32
AC31	VDD_FIXED	VDD_FIXED_MIPI	AP24
AD11	VDD_FIXED	VDD_FIXED_PCIE_ANA	AN18
AD13	VDD_FIXED	VDD_FIXED_PCIE_ANA	AN20
AD15	VDD_FIXED	VDD_FIXED_PCIE_ANA	AP19
AD17	VDD_FIXED	VDD_FIXED_PCIE_ANA	AP21
AD19	VDD_FIXED	VDD_FIXED_PCIE_REFBUF	AM23
AE12	VDD_FIXED	VDD_FIXED_PCIE_REFBUF	AN22
AE14	VDD_FIXED		
AE16	VDD_FIXED	VDD_FIXED_USB	AF35
AE18	VDD_FIXED	VDD_FIXED_USB3	AP30
AE20	VDD_FIXED		
AE31	VDD_FIXED		
AF11	VDD_FIXED	VDD_FIXED	L24
AF13	VDD_FIXED	VDD_FIXED	L26
AF15	VDD_FIXED	VDD_FIXED	L28
AF17	VDD_FIXED	VDD_FIXED	L30
AF19	VDD_FIXED	VDD_FIXED	L32
AF21	VDD_FIXED	VDD_FIXED	M11
AG12	VDD_FIXED	VDD_FIXED	M31
AG14	VDD_FIXED	VDD_FIXED	N12
AG16	VDD_FIXED	VDD_FIXED	N32
AG18	VDD_FIXED	VDD_FIXED	P11
AG20	VDD_FIXED	VDD_FIXED	P31
AG31	VDD_FIXED	VDD_FIXED	R12
AG32	VDD_FIXED	VDD_FIXED	R32
AH11	VDD_FIXED	VDD_FIXED	T11
AH13	VDD_FIXED	VDD_FIXED	T31
AH15	VDD_FIXED	VDD_FIXED	U12
AH17	VDD_FIXED	VDD_FIXED	U32
AH19	VDD_FIXED	VDD_FIXED	V11
AJ12	VDD_FIXED	VDD_FIXED	V23
AJ14	VDD_FIXED	VDD_FIXED	V25
AJ20	VDD_FIXED	VDD_FIXED	V31
AJ32	VDD_FIXED	VDD_FIXED	W12
AK11	VDD_FIXED	VDD_FIXED	W24
AK13	VDD_FIXED	VDD_FIXED	W32
AK15	VDD_FIXED	VDD_FIXED	Y11
AK19	VDD_FIXED	VDD_FIXED	Y23
AL12	VDD_FIXED	VDD_FIXED	Y31
AL14	VDD_FIXED		
AL16	VDD_FIXED	VDD_FIXED_SENSE	Y25
AL18	VDD_FIXED		
AL20	VDD_FIXED		
AL23	VDD_FIXED		
AL25	VDD_FIXED		
AL27	VDD_FIXED		
AL29	VDD_FIXED		
AM11	VDD_FIXED		
AM13	VDD_FIXED		
AM15	VDD_FIXED		
AM17	VDD_FIXED		
AM24	VDD_FIXED		
AM26	VDD_FIXED		
AM28	VDD_FIXED		
AM30	VDD_FIXED		
L12	VDD_FIXED		
L14	VDD_FIXED		
L16	VDD_FIXED		
L18	VDD_FIXED		
L20	VDD_FIXED		
L22	VDD_FIXED		

U6 PPVDD_S1_FIXED_SOC 54

C1492 2.2UF 20% 6.3V X5R-CERM 0201

54 13 PPVDD_S1_FIXED_SOC

C14A9 0.1UF 20% 6.3V X5R-CERM 01005

C1495 1.0UF 20% 6.3V X5R 0201-1

C1409 CRITICAL 4.3UF 20% 4V CERM 0402

C1490 2.2UF 20% 6.3V X5R-CERM 0201

C1499 2.2UF 20% 6.3V X5R-CERM 0201

C1498 2.2UF 20% 6.3V X5R-CERM 0201

C1497 CRITICAL 4.3UF 20% 4V CERM 0402

PPVDD_S1_FIXED_SOC 13 54

C1493 2.2UF 20% 6.3V X5R-CERM 0201

C1496 CRITICAL 4.3UF 20% 4V CERM 0402

C14B0 0.22UF 20% 6.3V X5R 0100S-1

C14B1 15PF 5% 16V NP0-C0G-CERM 01005

C14C0 CRITICAL 4.3UF 20% 4V CERM 0402
C14C1 CRITICAL 4.3UF 20% 4V CERM 0402
C14C2 CRITICAL 4.3UF 20% 4V CERM 0402
C14C3 CRITICAL 4.3UF 20% 4V CERM 0402

C14C4 0.01UF 10% 6.3V X5R 01005

C14C5 15PF 5% 16V NP0-C0G-CERM 01005

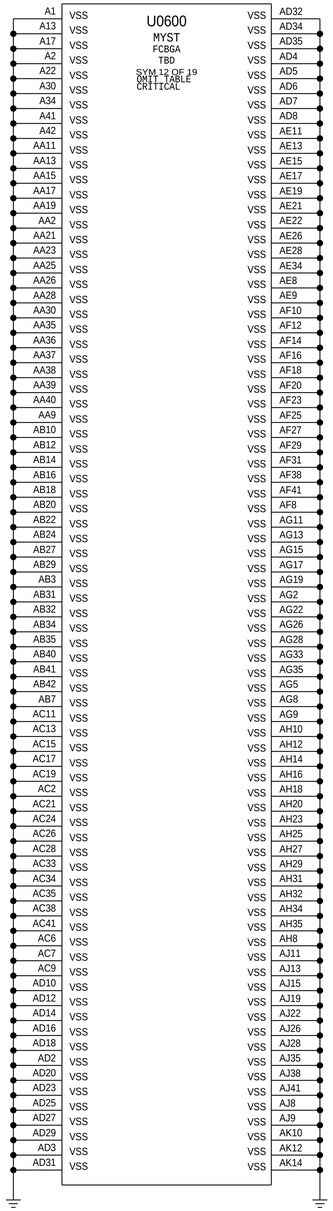
ADC_SOC_TO_PMU_VDD_SOC 44 52

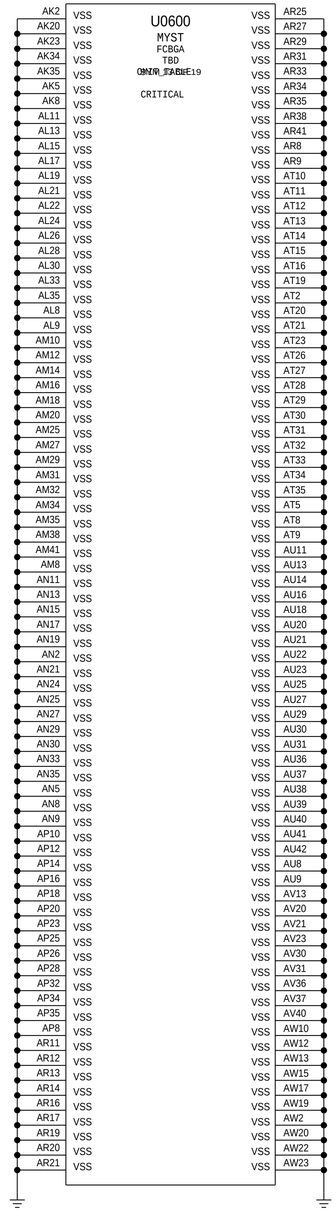
SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016

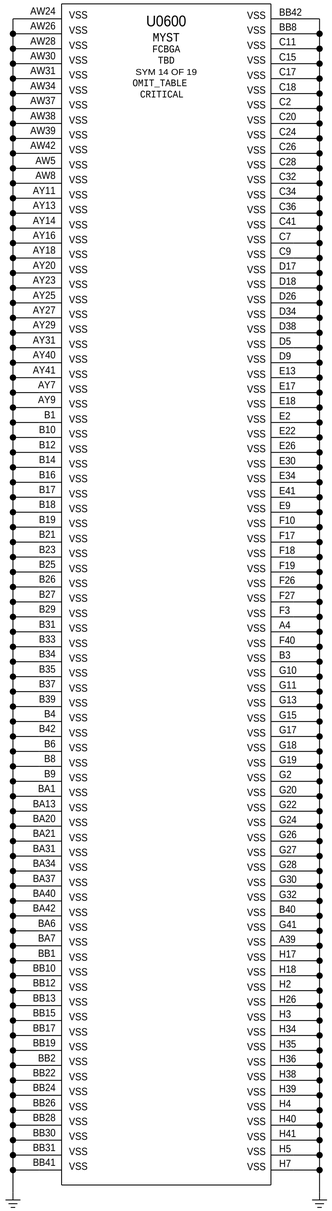
PAGE TITLE

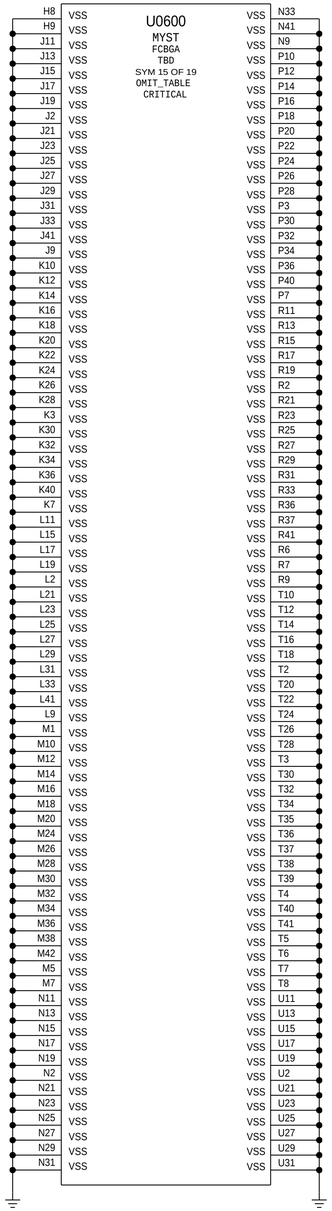
SOC: POWER (SRAM, SOC)

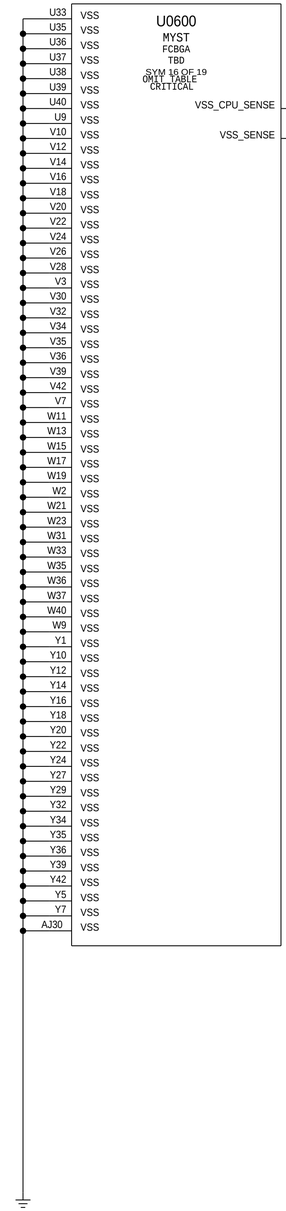
SOC GND:











AK31 — TP_VSS_CPU_SENSE — 52

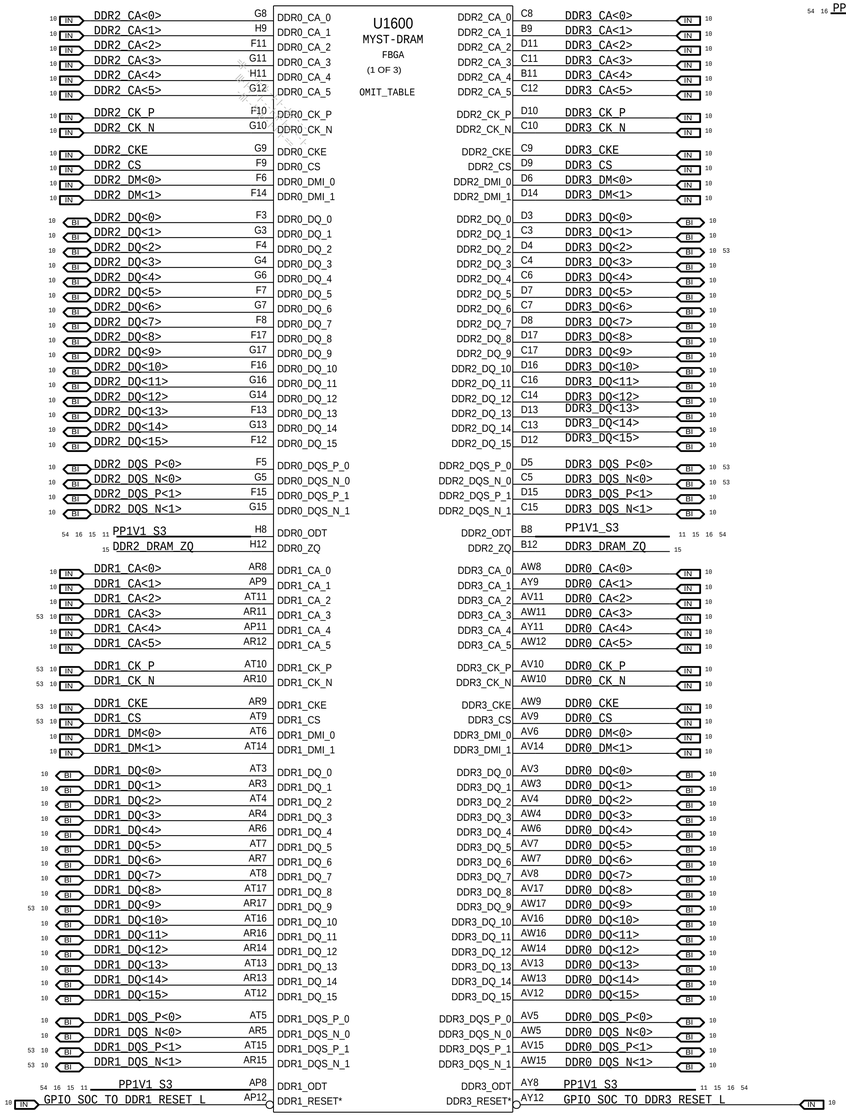
W25 — TP_VSS_SENSE — 52

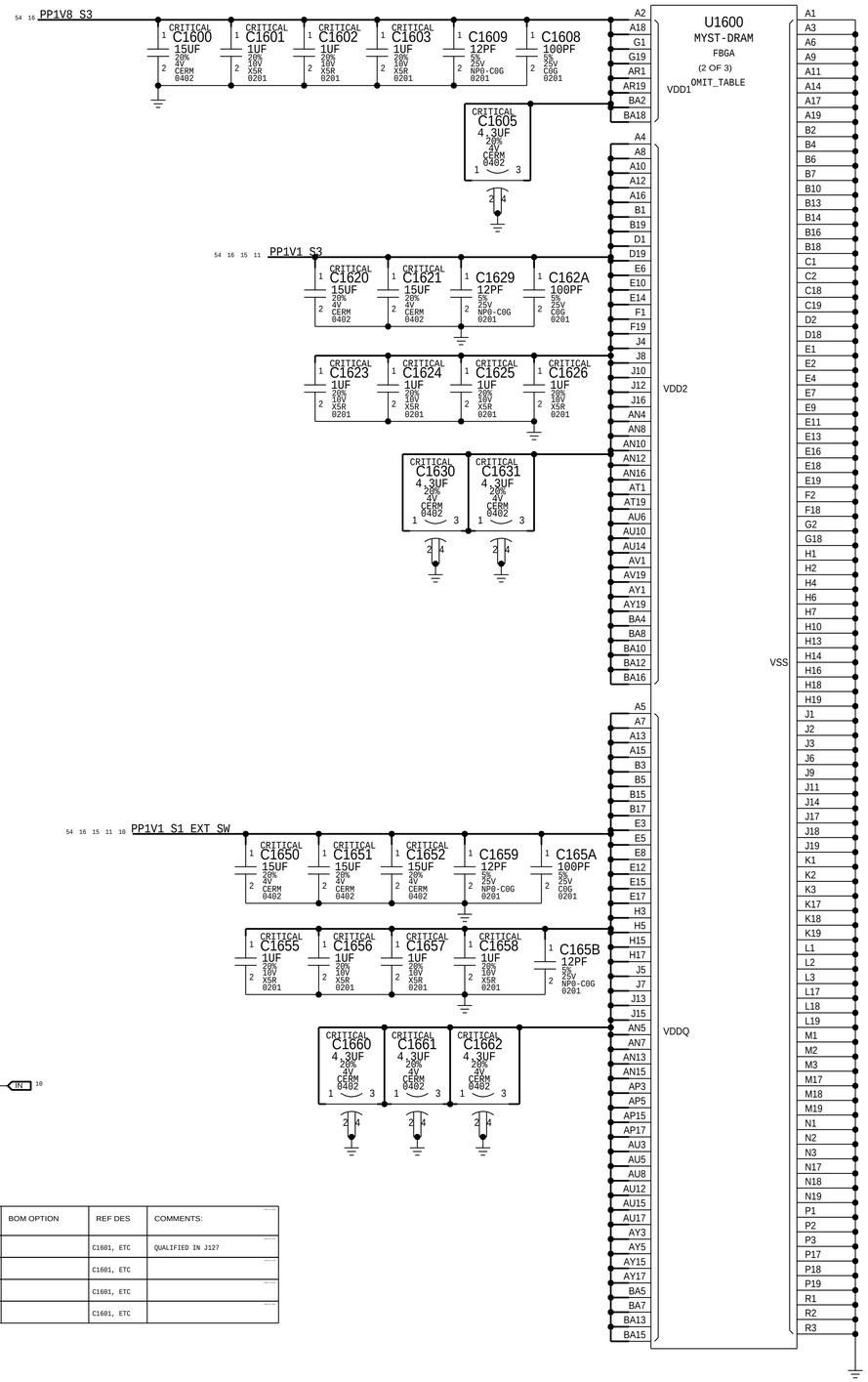
SYNC_MASTER=MLB_B SYNC_DATE=07/29/2010

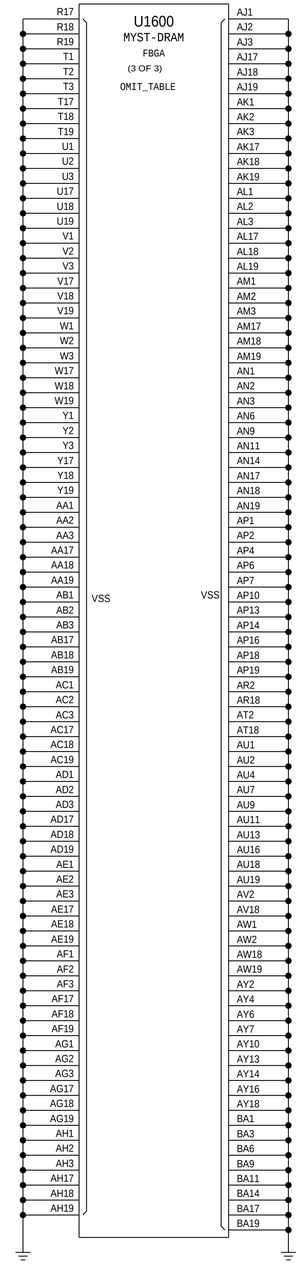
PAGE TITLE

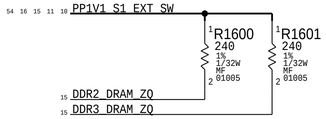
SOC: GND

DRAM1









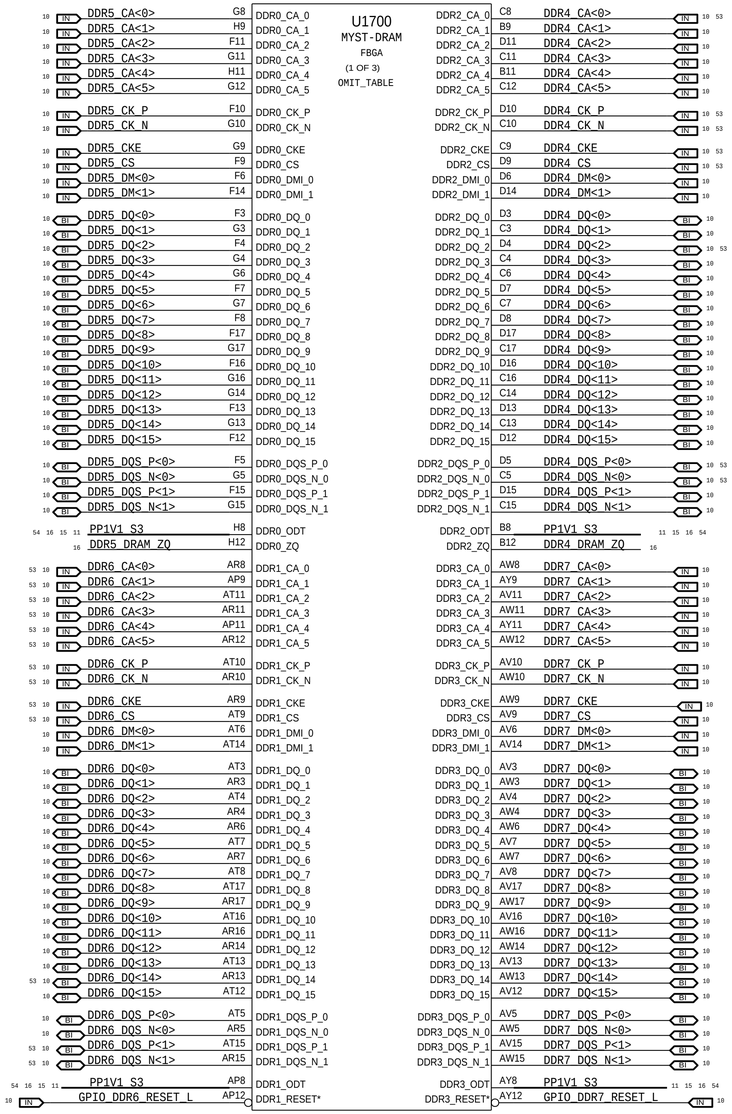
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0706	138S0739		C1601, ETC	QUALIFIED IN J127
138S0945	138S0739		C1601, ETC	
138S0739	138S0706		C1601, ETC	
138S0945	138S0706		C1601, ETC	

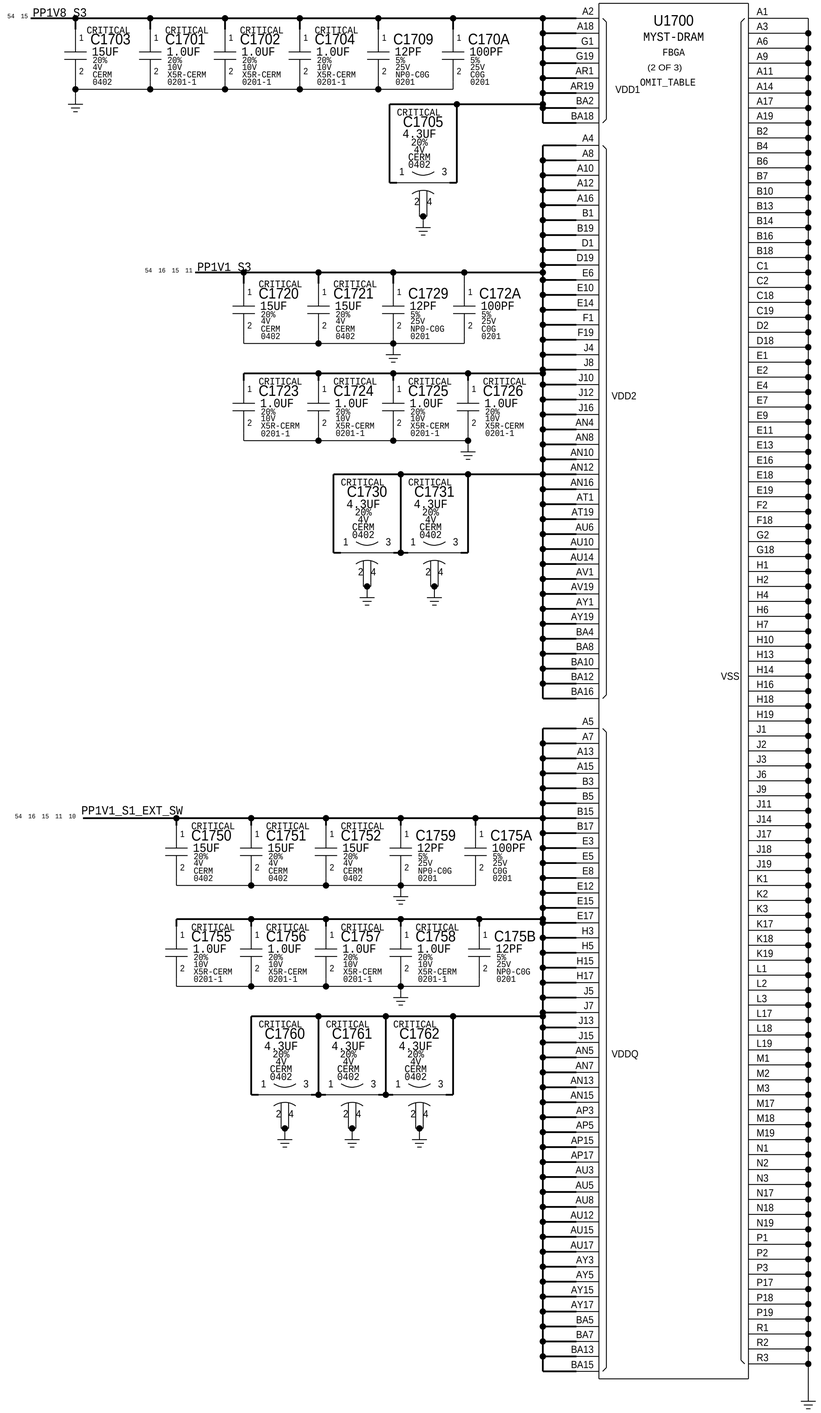
SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016

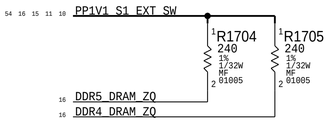
PAGE TITLE

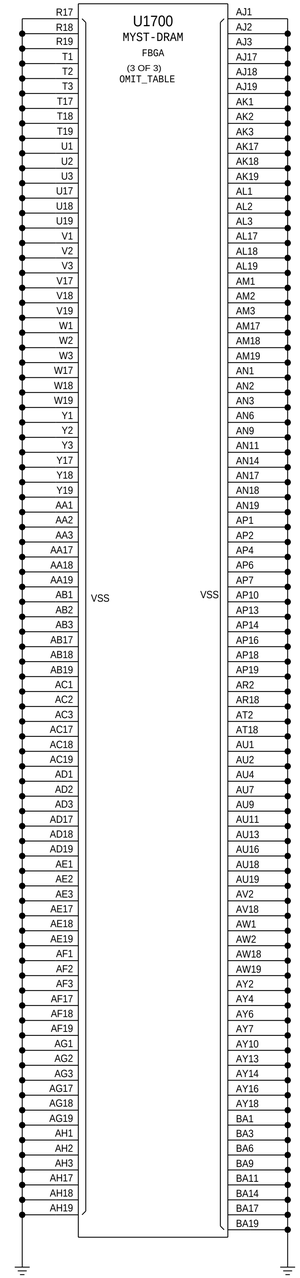
DRAM: CHANNELS 0-3

DRAM2







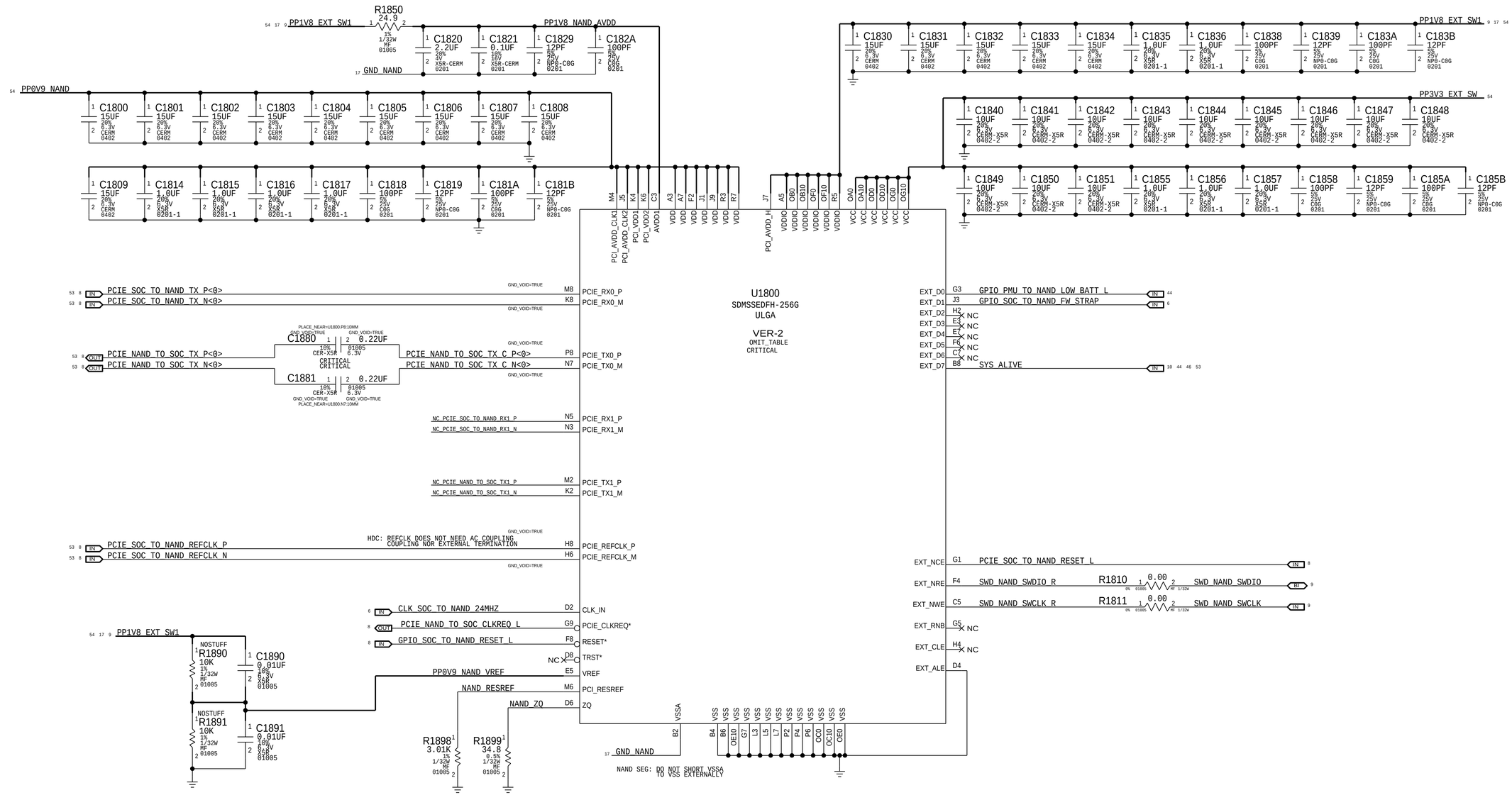


SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016
PAGE TITLE

DRAM: CHANNELS 4-7

NAND

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00005	138S0888		C1800	RDAR://PROBLEM/20618160
138S00003	138S0888		C1800	RDAR://PROBLEM/20618160



SYNC_MASTER=MLB_B SYNC_DATE=08/26/2016

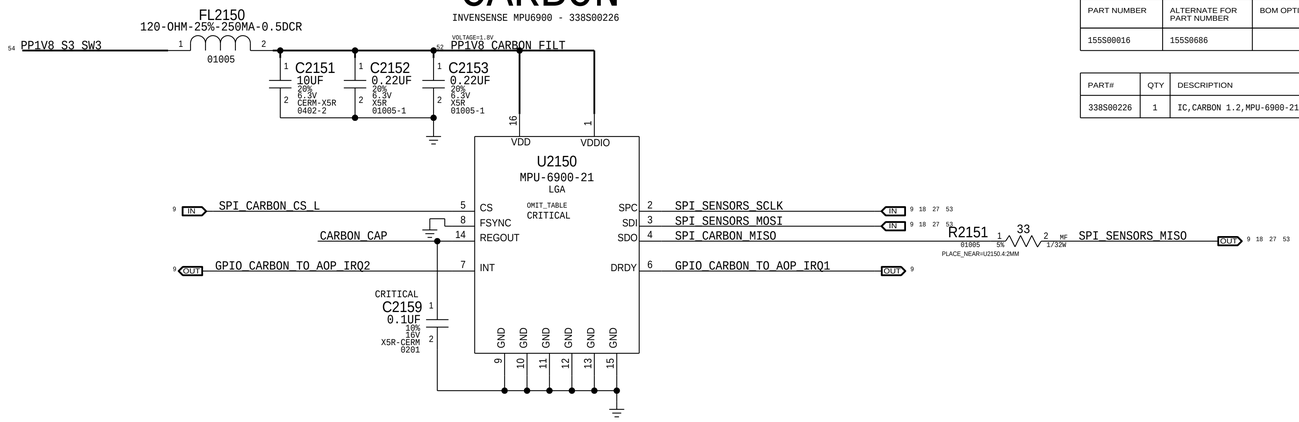
PAGE TITLE

NAND: NAND

SENSORS

CARBON

INVENSENSE MPU6900 - 338S00226

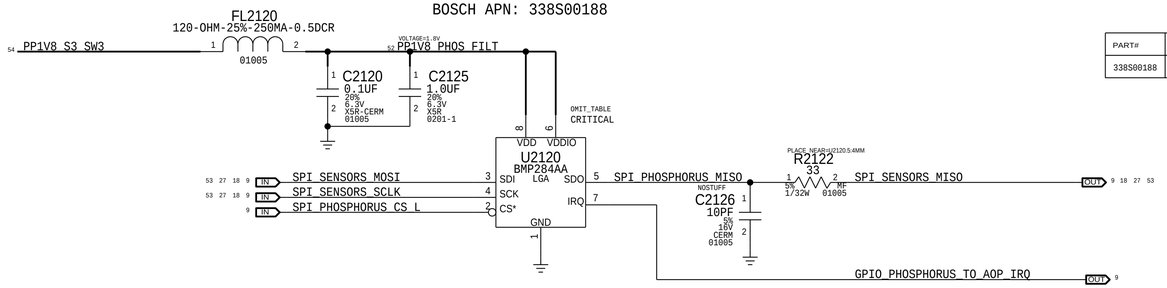


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00016	155S0686		FL2120,ECT	RDAR://PROBLEM/15809407

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00226	1	IC,CARBON 1.2,MPU-6900-21	U2150	CRITICAL	

PHOSPHORUS

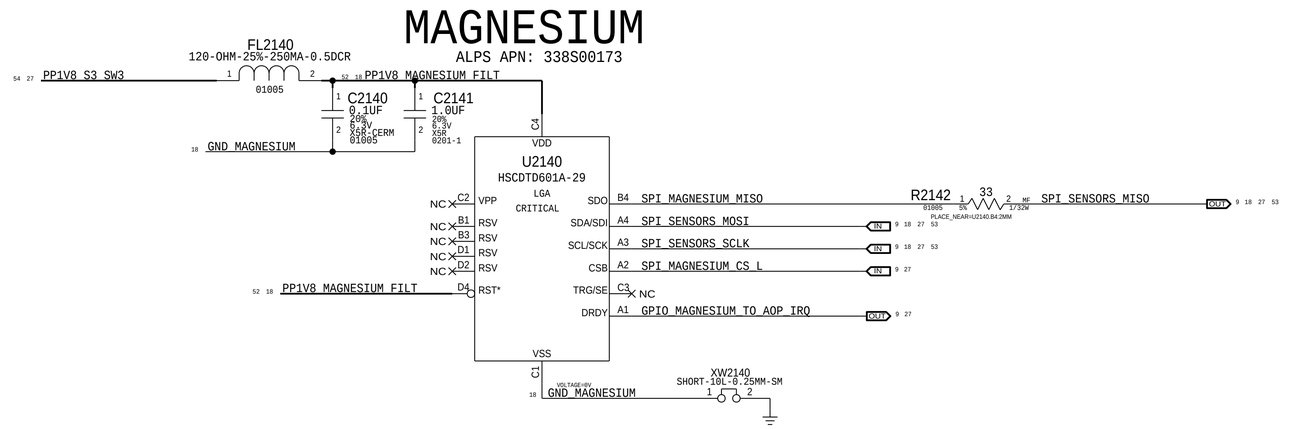
BOSCH APN: 338S00188



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00188	1	PHOSPHORUS2, BMP284AA,LGA8	U2120	CRITICAL	

MAGNESIUM

ALPS APN: 338S00173



SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

SENSOR: CARBON, PHOS, MAGN

KONA MASTER

U2200 BCM15900B0K BGA — SYM 1 OF 2 (CRITICAL)

E11	AUXADC_REF	
G12	AUXBUF_AIO_INPUT_3V	
F13	AUXBUF_AIO_OUTPUT	NC
D10	GPIO_ADC_00	KONA S TO KONA M INT L (IN)
D12	GPIO_ADC_01	NC
D11	GPIO_ADC_02	NC
F12	GPIO_ADC_03	TP KONA GPIO ADC 03
E10	GPIO_ADC_04	UART DEBUG TO GRAPE TX (IN)
F10	GPIO_ADC_05	UART GRAPE TO DEBUG TX (OUT)
G10	GPIO_ADC_06	GPIO SOC TO BT TO GRAPE TS SYNC (IN)
G9	GPIO_ADC_07	GPIO TOUCH TO BT SYNC (OUT)
F8	GPIO_08	SPI KONA M TO KONA S SCLK (OUT)
H11	GPIO_09	SPI KONA M TO KONA S MOSI (OUT)
J9	GPIO_10	SPI KONA M TO KONA S MISO (IN)
H9	GPIO_11	SPI KONA M TO KONA S CS L (OUT)
F7	GPIO_12	NC
J10	GPIO_13	NC
A6	GPIO_14	KONA S TO KONA M RESET DET L (IN)
C6	GPIO_15	KONA M GPIO 15
D9	GPIO_16	GPIO SOC TO GRAPE BSYNC0 (IN)
E8	GPIO_17	GPIO SOC TO GRAPE BSYNC1 (IN)
C9	GPIO_18	GPIO SOC TO GRAPE EB (IN)
C5	GPIO_19	NC
A7	H_INT*	GPIO GRAPE TO SOC IRQ L (OUT)
A8	H_SCLK	SPI SOC TO GRAPE SCLK (IN)
A9	H_SDI	SPI SOC TO GRAPE MOSI (IN)
B8	H_SDO	SPI SOC TO GRAPE MISO R
B6	H_CS*	SPI SOC TO GRAPE CS L (IN)
B5	H_ALT_CS*	NC
A5	I2C_SCL	NC
A4	I2C_SDA	NC
A12	KMSI_MISO	KMSI MISO (IN)
B13	KMSI_MOSI	KMSI MOSI (OUT)
B12	KMSI_STRB_IN	KMSI STRB IN (IN)
A13	KMSI_STRB_OUT	KMSI STRB OUT (OUT)
C14	PSE_SYNC	
B14	BOOST_ATEST	KONA BOOST ATEST
A15	BOOST_FBIN	KONA BOOST FBIN
B15	BOOST_ISENSE	KONA BOOST ISENSE
D13	BOOST_NGATE	KONA BOOST NGATE
C15	BOOST_VBAT	KONA BOOST VBAT
D14	BOOST_VBAT_EN	KONA BOOST EN
E9	JTAG_RTCK	NC
J7	JTAG_TCK	SWD GRAPE SWCLK (IN)
E7	JTAG_TMS	SWD GRAPE SWDIO (IN)
G7	JTAG_TDI	NC
H8	JTAG_TDO	NC
G6	JTAG_TRST*	NC
C7	JTAG_SRST*	NC
H7	RESET*	GPIO SOC TO GRAPE RESET L
K9	TEST_MODE	KONA M TEST MODE
K7	BOOT_CFG_0	KONA BOOT0 M
J8	BOOT_CFG_1	KONA BOOT1 M
R5	AFE_IO_BGBIAS	KONA BGBIAS
J15	XTALN	NC
K15	XTALP	
J13	XTAL_O_CLK_EXT	
B4	IFO_CLK_EXT	NC
N5	PAD_I_SELFCAPEXT	NC
N4	PAD_O_GUARDBUFFER	NC
C11	CORE_PMU_O_AON_TEST_PMU	NC

J5	PAD_I_TOUCH0	GRAPE RX<25> (IN)
H3	PAD_I_TOUCH1	GRAPE RX<24> (IN)
J2	PAD_I_TOUCH2	GRAPE RX<23> (IN)
J3	PAD_I_TOUCH3	GRAPE RX<22> (IN)
J4	PAD_I_TOUCH4	GRAPE RX<21> (IN)
K5	PAD_I_TOUCH5	GRAPE RX<20> (IN)
K4	PAD_I_TOUCH6	GRAPE RX<19> (IN)
K3	PAD_I_TOUCH7	GRAPE RX<18> (IN)
M5	PAD_I_TOUCH8	GRAPE RX<17> (IN)
L5	PAD_I_TOUCH9	GRAPE RX<16> (IN)
M1	PAD_I_TOUCH10	GRAPE RX<15> (IN)
K1	PAD_I_TOUCH11	GRAPE RX<14> (IN)
L6	PAD_I_TOUCH12	GRAPE RX<13> (IN)
N1	PAD_I_TOUCH13	GRAPE RX<12> (IN)
P6	PAD_I_TOUCH14	GRAPE RX<11> (IN)
N6	PAD_I_TOUCH15	GRAPE RX<10> (IN)
R7	PAD_I_TOUCH16	GRAPE RX<9> (IN)
N7	PAD_I_TOUCH17	GRAPE RX<8> (IN)
R8	PAD_I_TOUCH18	GRAPE RX<7> (IN)
M6	PAD_I_TOUCH19	GRAPE RX<6> (IN)
P7	PAD_I_TOUCH20	GRAPE RX<5> (IN)
M7	PAD_I_TOUCH21	GRAPE RX<4> (IN)
N9	PAD_I_TOUCH22	GRAPE RX<3> (IN)
P9	PAD_I_TOUCH23	GRAPE RX<2> (IN)
M9	PAD_I_TOUCH24	GRAPE RX<1> (IN)
R9	PAD_I_TOUCH25	GRAPE RX<0> (IN)
N10	PAD_I_TOUCH26	NC
M10	PAD_I_TOUCH27	NC
R10	PAD_I_TOUCH28	NC
P10	PAD_I_TOUCH29	NC
D2	PAD_I_TOUCH30	NC
D1	PAD_I_TOUCH31	NC
C2	PAD_I_TOUCH32	NC
C1	PAD_I_TOUCH33	NC
B1	PAD_I_TOUCH34	NC
P3	PAD_I_TOUCH35	NC
N2	PAD_I_TOUCH36	NC
P1	PAD_I_TOUCH37	NC
P2	PAD_I_TOUCH38	NC
P4	PAD_I_TOUCH39	NC
G3	PAD_I_TOUCH40	GRAPE TX<20> (OUT)
D4	PAD_I_TOUCH41	GRAPE TX<21> (OUT)
D3	PAD_I_TOUCH42	GRAPE TX<22> (OUT)
G4	PAD_I_TOUCH43	GRAPE TX<23> (OUT)
E4	PAD_I_TOUCH44	GRAPE TX<24> (OUT)
E3	PAD_I_TOUCH45	GRAPE TX<25> (OUT)
F1	PAD_I_TOUCH46	GRAPE TX<26> (OUT)
F4	PAD_I_TOUCH47	GRAPE TX<27> (OUT)
F3	PAD_I_TOUCH48	GRAPE TX<28> (OUT)
H5	PAD_I_TOUCH49	GRAPE TX<29> (OUT)
F2	PAD_I_TOUCH50	GRAPE TX<30> (OUT)
G2	PAD_I_TOUCH51	GRAPE TX<31> (OUT)
G1	PAD_I_TOUCH52	GRAPE TX<32> (OUT)
H1	PAD_I_TOUCH53	GRAPE TX<33> (OUT)
P11	PAD_I_TOUCH54	GRAPE TX<34> (OUT)
N15	PAD_I_TOUCH55	GRAPE TX<35> (OUT)
N12	PAD_I_TOUCH56	GRAPE TX<36> (OUT)
P13	PAD_I_TOUCH57	GRAPE TX<37> (OUT)
P12	PAD_I_TOUCH58	GRAPE TX<38> (OUT)
R12	PAD_I_TOUCH59	GRAPE TX<39> (OUT)
N13	PAD_I_TOUCH60	NC
M12	PAD_I_TOUCH61	NC
R13	PAD_I_TOUCH62	NC
L13	PAD_I_TOUCH63	NC
P14	PAD_I_TOUCH64	NC
M14	PAD_I_TOUCH65	NC
M13	PAD_I_TOUCH66	NC
N14	PAD_I_TOUCH67	NC
M15	PAD_I_TOUCH68	NC
R14	PAD_I_TOUCH69	NC

R2205 0.00 5% 1/32W MF 01005 — SPI_SOC_TO_GRAPE_CS_L (IN) — TODO: CHECK BSYNC CONNECTIVITY

R2215 33 5% 1/32W MF 01005 — SPI_SOC_TO_GRAPE_MISO (OUT)

R2214 1.00M 5% 1/32W MF 01005 — PP3V3_GRAPE_FILT

R2224 10K 5% 1/32W MF 01005 — PP1V8_GRAPE_EXT_SW

R2211 10K 5% 1/32W MF 01005 — GPIO_SOC_TO_GRAPE_RESET_L / KONA_M_TEST_MODE

C2216 20PF 5% 16V NP0-C0G-CERM 01005 — CLK_SOC_TO_GRAPE_24MHZ (IN) / CLK_TOUCH_24MHZ_C

XW2202 — CLK_KONA_S_24MHZ (OUT) / SHORT-8L-0.091MM-SM

XW2201 SHORT-8L-0.091MM-SM — CLK_KONA_M_24MHZ

C2217 10PF 5% 16V CERM 01005

U2200 BCM15900B0K BGA — SYM 2 OF 2 (CRITICAL)

MARKED AS CRITICAL DUE TO PART ISSUES IN THE PAST W/0201

B3	AFE_I_VDDHV15_EXT	PP15V0_TOUCH_FILT (R2222 3.3 5% 1/16W MF-LF 402; C2221–C2223, C2232 0.47UF 20% 25V CER-X5R 0201)
C4	AFE_I_VDDHV15_EXT	
L7	AFE_I_VDDHV15_EXT	
E5	AFE_I_VDDHV15_EXT	
M11	AFE_I_VDDHV15_EXT	
H2	AFE_I_VDDHV15_EXT	
K6	AFE_I_VDDHV15_EXT	
L1	AFE_I_VDDHV15_EXT	
L9	AFE_I_VDDHV15_EXT	
M3	AFE_I_VDDHV15_EXT	
E2	AFE_I_VDDHV15_EXT	
N3	AFE_I_VDDHV15_EXT	
L12	AFE_I_VDDHV15_EXT	
G5	AFE_I_VDDHV15_EXT	
R15	AFE_I_VDDHV15_EXT	
E13	BOOST_VDDA	L2204 FERR-220-OHM 0402 — PP3V3_GRAPE_FILT (C2238 100PF 5% 25V C0G 0201; C2239 12PF 5% 25V NP0-C0G 0201; C2224 0.1UF 10% 10V X5R-CERM 0201; C2225 0.1UF 10% 10V X5R-CERM 0201; C2231 0.22UF 20% 10V CERM-X5R 0201)
C12	OTP_TMON_I_VDDA_3P3_EXT	
R1	AFE_PMU_I_VDDA_3P3_EXT	
G13	AUXBUF_PMU_I_VDDA_3P3_EXT	
G14	AUXBUF_PMU_I_VDDHV_AUX_EXT	
G15	AUXBUF_PMU_O_VDD_AUX_CAP	NC
C3	AFE_I_VDDANA_3P3_AFE_PMU	PP2V8_KONA_M_VDDANA (C2278 100PF 5% 25V C0G 0201; C2279 12PF 5% 25V NP0-C0G 0201; C2201 0.1UF 10% 10V X5R-CERM 0201; C2202 0.1UF 10% 10V X5R-CERM 0402; C2203 0.1UF 10% 10V X5R-CERM 0201; C2204 0.1UF 10% 10V X5R-CERM 0201; C2205 0.1UF 10% 10V X5R-CERM 0201; C2206 2.2UF 10% 10V X5R-CERM 0402)
D5	AFE_I_VDDANA_3P3_AFE_PMU	
H6	AFE_I_VDDANA_3P3_AFE_PMU	
L4	AFE_I_VDDANA_3P3_AFE_PMU	
L3	AFE_I_VDDANA_3P3_AFE_PMU	
L8	AFE_I_VDDANA_3P3_AFE_PMU	
M2	AFE_I_VDDANA_3P3_AFE_PMU	
R11	AFE_I_VDDANA_3P3_AFE_PMU	
M8	AFE_I_VDDANA_3P3_AFE_PMU	
N8	AFE_I_VDDANA_3P3_AFE_PMU	
J6	AFE_I_VDDANA_3P3_AFE_PMU	
L11	AFE_I_VDDANA_3P3_AFE_PMU	
L14	AFE_I_VDDANA_3P3_AFE_PMU	
R6	AFE_I_VDDANA_3P3_AFE_PMU	
R2	AFE_PMU_O_VDDANA_3P3_PMU	
R4	AFE_PMU_O_AVDD1P2_CAP	KONA M VDDADC CAP (C2229 1UF 10% 10V X5R-CERM 0402)
J14	XTAL_PLL_AVDD1P8_I_VDDLDO_1P8_EXT	L2203 FERR-220-OHM 0402 — PP1V8_GRAPE_XTAL_FILT (C2227 0.1UF 10% 25V X5R 0201; C2228 0.047UF 10% 25V X5R 0201)
F11	AUXADC_AVDDC_I_VDDIO_1P8_3P3_EXT	PP1V8_GRAPE_EXT_SW (C2248 100PF 5% 25V C0G 0201; C2249 12PF 5% 25V NP0-C0G 0201; C2207 2.2UF 10% 10V X5R-CERM 0402; C2208 0.1UF 10% 6.3V CERM-X5R 0201; C2209 0.1UF 10% 6.3V CERM-X5R 0201; C2210 0.1UF 10% 6.3V CERM-X5R 0201)
E12	AUXADC_AVDD_I_VDDIO_1P8_3P3_EXT	
R3	AFE_PMU_I_VDDLDO_1P8_EXT	
B9	AON_PAD_I_VDDIO_1P8_3P3_EXT	
D7	AON_PAD_I_VDDIO_1P8_3P3_EXT	
E6	AON_PAD_I_VDDIO_1P8_3P3_EXT	
A2	I2C_PAD_I_VDDIO_1P8_3P3_EXT	
C13	CORE_PAD_I_VDDIO_1P8_3P3_EXT	
C8	CORE_PAD_I_VDDIO_1P8_3P3_EXT	
B11	CORE_PMU_I_AON_VDDIO_1P8_3P3_EXT	R2281 100 1% 1/20W MF 201 — PP1V8_GRAPE_AON_RC; C2281 2.2UF 10% 10V X5R-CERM 0402
A10	CORE_PMU_I_VDDLDO_1P8_EXT	
A11	CORE_PMU_O_VDDCORE_1P2_CAP	KONA M VDDCORE CAP (C2218 1UF 10% 10V X5R-CERM 0402; C2219 0.1UF 10% 6.3V CERM-X5R 0201)

F14	AUXBUF_AVSS	
C10	AUXADC_AVSS	
D6	VSS	
D8	VSS	
F6	VSS	
F9	VSS	
G8	VSS	
H10	VSS	
K8	VSS	
A14	VSS	
E14	VSS	
A1	VSS	
A3	VSS	
B7	VSS	
H12	VSS	
H13	VSS	
K11	VSS	
K12	VSS	
K13	VSS	
D15	VSS	
E15	VSS	
F15	VSS	
G11	VSS	
J11	VSS	
J12	VSS	
K10	VSS	
H15	XTAL_AVSS	
K14	XTAL_AVSS	
B10	CORE_PMU_I_AVSS	
H14	AUXBUF_PMU_I_AVSS	
B2	PAD_I_AVSS	
E1	PAD_I_AVSS	
J1	PAD_I_AVSS	
N11	PAD_I_AVSS	
L2	PAD_I_AVSS	
P15	PAD_I_AVSS	
K2	PAD_I_AVSS	
L10	PAD_I_AVSS	
L15	PAD_I_AVSS	
M4	PAD_I_AVSS	
F5	PAD_I_AVSS	
P5	PAD_I_AVSS	
P8	PAD_I_AVSS	
H4	PAD_I_AVSS	

BOOT OPTION

PP1V8_GRAPE_EXT_SW — R2201 10K (NOSTUFF) — KONA_BOOT0_M; R2202 10K — KONA_BOOT0_M; R2203 10K — KONA_BOOT1_M; R2204 10K (NOSTUFF) — KONA_BOOT1_M

15V BOOST

Q2201 SIA445EDJ SC70-6L (CRITICAL) — PPVCC_MAIN

R2207 10K 5% 1/32W MF 01005 — C2211 1UF 20% 10V CER-X5R 0201 — NO_XNET_CONNECTION=1

R2206 1.00K 5% 1/32W MF 01005 — KONA_BOOST_EN — KONA_BOOST_EN_R

C2226 0.1UF 10% 25V X5R 0201; C2220 10UF 20% 10V X5R-CERM 0402-7 — KONA_BOOST_MAIN_GATED

R2208 0.15 1% 1/8W MF 0402 — KONA_BOOST_MAIN_R

XW2204 SHORT-8L-0.091MM-SM NO_XNET_CONNECTION=1

XW2203 SHORT-8L-0.091MM-SM NO_XNET_CONNECTION=1

L2201 22UH-20%-0.61A-0.60HM VLF504010-SM (CRITICAL) — KONA_BOOST_LX (DIDT=TRUE, SWITCH_NODE=TRUE)

Q2202 CSD17381F4 0402 (CRITICAL) — KONA_BOOST_VBAT / KONA_BOOST_ISENSE / KONA_BOOST_NGATE

D2201 SOD523 (CRITICAL) — ZLLS350

C2212 10UF 20% 25V X5R-CERM 0603; C2213 10UF 20% 25V X5R-CERM 0603; C2214 10UF 20% 25V X5R-CERM 0603; C2215 10UF 20% 25V X5R-CERM 0603; C2268 100PF 5% 25V C0G 0201 — PP15V0_TOUCH

XW2205 SHORT-8L-0.091MM-SM NO_XNET_CONNECTION=1 — KONA_BOOST_FBIN

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0641	138S0700		C2206,ETC	RDAR://PROBLEM/20618071
376S00191	376S00061		Q2202	

SYNC_MASTER=MLB_B — SYNC_DATE=07/29/2016

PAGE TITLE

TOUCH: KONA MASTER

KONA: SLAVE

U2301
BCM15900B0K
BGA
SYM 1 OF 2
CRITICAL

E11	AUXADC_REF		
G12	AUXBUF_AIO_INPUT_3V		
F13	AUXBUF_AIO_OUTPUT		
D10	GPIO_ADC_00		
D12	GPIO_ADC_01		
D11	GPIO_ADC_02		
F12	GPIO_ADC_03	53	TP_KONA_S_UART_RX
E10	GPIO_ADC_04	53	TP_KONA_S_UART_TX
F10	GPIO_ADC_05		
G10	GPIO_ADC_06	53 51 19 6 IN	GPIO_SOC_TO_BT_TO_GRAPE_TS_SYNC
G9	GPIO_ADC_07		
F8	GPIO_08	53	TP_KONA_IPC_EVENT_0
H11	GPIO_09	53	TP_KONA_IPC_EVENT_1
J9	GPIO_10	53	TP_KONA_IPC_EVENT_2
H9	GPIO_11	53	TP_KONA_IPC_EVENT_3
F7	GPIO_12	53	TP_KONA_IPC_EVENT_4
J10	GPIO_13	53	TP_KONA_IPC_EVENT_5
A6	GPIO_14	53 19 OUT	KONA_S_TO_KONA_M_RESET_DET_L
C6	GPIO_15		
D9	GPIO_16	53 32 19 IN	GPIO_SOC_TO_GRAPE_BSYNC0
E8	GPIO_17	53 32 19 IN	GPIO_SOC_TO_GRAPE_BSYNC1
C9	GPIO_18	32 19 IN	GPIO_SOC_TO_GRAPE_EB
C5	GPIO_19		
A7	H_INT*	19 OUT	KONA_S_TO_KONA_M_INT_L
A8	H_SCLK	19 IN	SPI_KONA_M_TO_KONA_S_SCLK
A9	H_SDI	19 IN	SPI_KONA_M_TO_KONA_S_MOSI
B8	H_SDO	19 OUT	SPI_KONA_M_TO_KONA_S_MISO
B6	H_CS*	19 IN	SPI_KONA_M_TO_KONA_S_CS_L
B5	H_ALT_CS*		
A5	I2C_SCL		
A4	I2C_SDA		
A12	KMSI_MISO	53 19 IN	KMSI_MISO
B13	KMSI_MOSI	53 19 OUT	KMSI_MOSI
B12	KMSI_STRB_IN	53 19 IN	KMSI_STRB_OUT
A13	KMSI_STRB_OUT	53 19 OUT	KMSI_STRB_IN
C14	PSE_SYNC	53 19 BI	PSE_SYNC
B14	BOOST_ATEST		
A15	BOOST_FBIN		
B15	BOOST_ISENSE		
D13	BOOST_NGATE		
C15	BOOST_VBAT		
D14	BOOST_VBAT_EN		
E9	JTAG_RTCK		
J7	JTAG_TCK		
E7	JTAG_TMS		
G7	JTAG_TDI		
H8	JTAG_TDO		
G6	JTAG_TRST*		
C7	JTAG_SRST*		
H7	RESET*	53 19 6 IN	GPIO_SOC_TO_GRAPE_RESET_L
K9	TEST_MODE		KONA_S_TEST_MODE
K7	BOOT_CFG_0	20	KONA_BOOT0_S
J8	BOOT_CFG_1	20	KONA_BOOT1_S
R5	AFE_IO_BGBIAS	19	KONA_BGBIAS
J15	XTALN		
K15	XTALP	19 IN	CLK_KONA_S_24MHZ
J13	XTAL_O_CLK_EXT		
B4	IFO_CLK_EXT		
N5	PAD_I_SELFCAPEXT		
N4	PAD_O_GUARDBUFFER		
C11	CORE_PMU_O_AON_TEST_PMU		

J5	PAD_I_TOUCH0	GRAPE_RX<51>	21 IN
H3	PAD_I_TOUCH1	GRAPE_RX<50>	21 IN
J2	PAD_I_TOUCH2	GRAPE_RX<49>	21 IN
J3	PAD_I_TOUCH3	GRAPE_RX<48>	21 IN
J4	PAD_I_TOUCH4	GRAPE_RX<47>	21 IN
K5	PAD_I_TOUCH5	GRAPE_RX<46>	21 IN
K4	PAD_I_TOUCH6	GRAPE_RX<45>	21 IN
K3	PAD_I_TOUCH7	GRAPE_RX<44>	21 IN
M5	PAD_I_TOUCH8	GRAPE_RX<43>	21 IN
L5	PAD_I_TOUCH9	GRAPE_RX<42>	21 IN
M1	PAD_I_TOUCH10	GRAPE_RX<41>	21 IN
K1	PAD_I_TOUCH11	GRAPE_RX<40>	21 IN
L6	PAD_I_TOUCH12	GRAPE_RX<39>	21 IN
N1	PAD_I_TOUCH13	GRAPE_RX<38>	21 IN
P6	PAD_I_TOUCH14	GRAPE_RX<37>	21 IN
N6	PAD_I_TOUCH15	GRAPE_RX<36>	21 IN
R7	PAD_I_TOUCH16	GRAPE_RX<35>	21 IN
N7	PAD_I_TOUCH17	GRAPE_RX<34>	21 IN
R8	PAD_I_TOUCH18	GRAPE_RX<33>	21 IN
M6	PAD_I_TOUCH19	GRAPE_RX<32>	21 IN
P7	PAD_I_TOUCH20	GRAPE_RX<31>	21 IN
M7	PAD_I_TOUCH21	GRAPE_RX<30>	21 IN
N9	PAD_I_TOUCH22	GRAPE_RX<29>	21 IN
P9	PAD_I_TOUCH23	GRAPE_RX<28>	21 IN
M9	PAD_I_TOUCH24	GRAPE_RX<27>	21 IN
R9	PAD_I_TOUCH25	GRAPE_RX<26>	21 IN
N10	PAD_I_TOUCH26	NC	
M10	PAD_I_TOUCH27	NC	
R10	PAD_I_TOUCH28	NC	
P10	PAD_I_TOUCH29	NC	
D2	PAD_I_TOUCH30	NC	
D1	PAD_I_TOUCH31	NC	
C2	PAD_I_TOUCH32	NC	
C1	PAD_I_TOUCH33	NC	
B1	PAD_I_TOUCH34	NC	
P3	PAD_I_TOUCH35	NC	
N2	PAD_I_TOUCH36	NC	
P1	PAD_I_TOUCH37	NC	
P2	PAD_I_TOUCH38	NC	
P4	PAD_I_TOUCH39	NC	
G3	PAD_I_TOUCH40	GRAPE_TX<0>	21 OUT
D4	PAD_I_TOUCH41	GRAPE_TX<1>	21 OUT
D3	PAD_I_TOUCH42	GRAPE_TX<2>	21 OUT
G4	PAD_I_TOUCH43	GRAPE_TX<3>	21 OUT
E4	PAD_I_TOUCH44	GRAPE_TX<4>	21 OUT
E3	PAD_I_TOUCH45	GRAPE_TX<5>	21 OUT
F1	PAD_I_TOUCH46	GRAPE_TX<6>	21 OUT
F4	PAD_I_TOUCH47	GRAPE_TX<7>	21 OUT
F3	PAD_I_TOUCH48	GRAPE_TX<8>	21 OUT
H5	PAD_I_TOUCH49	GRAPE_TX<9>	21 OUT
F2	PAD_I_TOUCH50	GRAPE_TX<10>	21 OUT
G2	PAD_I_TOUCH51	GRAPE_TX<11>	21 OUT
G1	PAD_I_TOUCH52	GRAPE_TX<12>	21 OUT
H1	PAD_I_TOUCH53	GRAPE_TX<13>	21 OUT
P11	PAD_I_TOUCH54	GRAPE_TX<14>	21 OUT
N15	PAD_I_TOUCH55	GRAPE_TX<15>	21 OUT
N12	PAD_I_TOUCH56	GRAPE_TX<16>	21 OUT
P13	PAD_I_TOUCH57	GRAPE_TX<17>	21 OUT
P12	PAD_I_TOUCH58	GRAPE_TX<18>	21 OUT
R12	PAD_I_TOUCH59	GRAPE_TX<19>	21 OUT
N13	PAD_I_TOUCH60	NC	
M12	PAD_I_TOUCH61	NC	
R13	PAD_I_TOUCH62	NC	
L13	PAD_I_TOUCH63	NC	
P14	PAD_I_TOUCH64	NC	
M14	PAD_I_TOUCH65	NC	
M13	PAD_I_TOUCH66	NC	
N14	PAD_I_TOUCH67	NC	
M15	PAD_I_TOUCH68	NC	
R14	PAD_I_TOUCH69	NC	

R2308 0.00 1/32W MF 01005 NOSTUFF
R2306 0.00 1/32W MF 01005
R2307 0.00 1/32W MF 01005
R2309 0.00 1/32W MF 01005
R2305 10K 5% 1/32W MF 01005
C2301 10PF 5% 16V CERM 01005

U2301
BCM15900B0K
BGA
SYM 2 OF 2
CRITICAL

B3	AFE_I_VDDHV15_EXT		
C4	AFE_I_VDDHV15_EXT		
L7	AFE_I_VDDHV15_EXT		
E5	AFE_I_VDDHV15_EXT		
M11	AFE_I_VDDHV15_EXT		
H2	AFE_I_VDDHV15_EXT		
K6	AFE_I_VDDHV15_EXT		
L1	AFE_I_VDDHV15_EXT		
L9	AFE_I_VDDHV15_EXT		
M3	AFE_I_VDDHV15_EXT		
E2	AFE_I_VDDHV15_EXT		
N3	AFE_I_VDDHV15_EXT		
L12	AFE_I_VDDHV15_EXT		
G5	AFE_I_VDDHV15_EXT		
R15	AFE_I_VDDHV15_EXT		
E13	BOOST_VDDA	53 19	PP3V3_GRAPE_FILT
C12	OTP_TMON_I_VDDA_3P3_EXT		
R1	AFE_PMU_I_VDDA_3P3_EXT		
G13	AUXBUF_PMU_I_VDDA_3P3_EXT		
G14	AUXBUF_PMU_I_VDDHV_AUX_EXT		
G15	AUXBUF_PMU_O_VDD_AUX_CAP	NC	
C3	AFE_I_VDDANA_3P3_AFE_PMU	52	PP2V8_KONA_S_VDDANA
D5	AFE_I_VDDANA_3P3_AFE_PMU		
H6	AFE_I_VDDANA_3P3_AFE_PMU		
L4	AFE_I_VDDANA_3P3_AFE_PMU		
L3	AFE_I_VDDANA_3P3_AFE_PMU		
L8	AFE_I_VDDANA_3P3_AFE_PMU		
M2	AFE_I_VDDANA_3P3_AFE_PMU		
R11	AFE_I_VDDANA_3P3_AFE_PMU		
M8	AFE_I_VDDANA_3P3_AFE_PMU		
N8	AFE_I_VDDANA_3P3_AFE_PMU		
J6	AFE_I_VDDANA_3P3_AFE_PMU		
L11	AFE_I_VDDANA_3P3_AFE_PMU		
L14	AFE_I_VDDANA_3P3_AFE_PMU		
R6	AFE_I_VDDANA_3P3_AFE_PMU		
R2	AFE_PMU_O_VDDANA_3P3_PMU		
R4	AFE_PMU_O_AVDD1P2_CAP		KONA_S_VDDADC_CAP
J14	XTAL_PLL_AVDD1P8_I_VDDLDO_1P8_EXT	53 19	PP1V8_GRAPE_XTAL_FILT
F11	AUXADC_AVDDC_I_VDDIO_1P8_3P3_EXT	54 20 19 9	PP1V8_GRAPE_EXT_SW
E12	AUXADC_AVDD_I_VDDIO_1P8_3P3_EXT		
R3	AFE_PMU_I_VDDLDO_1P8_EXT		
B9	AON_PAD_I_VDDIO_1P8_3P3_EXT		
D7	AON_PAD_I_VDDIO_1P8_3P3_EXT		
E6	AON_PAD_I_VDDIO_1P8_3P3_EXT		
A2	I2C_PAD_I_VDDIO_1P8_3P3_EXT		
C13	CORE_PAD_I_VDDIO_1P8_3P3_EXT		
C8	CORE_PAD_I_VDDIO_1P8_3P3_EXT		
B11	CORE_PMU_I_AON_VDDIO_1P8_3P3_EXT	53 19	PP1V8_GRAPE_AON_RC
A10	CORE_PMU_I_VDDLDO_1P8_EXT		
A11	CORE_PMU_O_VDDCORE_1P2_CAP	53	KONA_S_VDDCORE_CAP
F14	AUXBUF_AVSS		
C10	AUXADC_AVSS		
D6	VSS		
D8	VSS		
F6	VSS		
F9	VSS		
G8	VSS		
H10	VSS		
K8	VSS		
A14	VSS		
E14	VSS		
A1	VSS		
A3	VSS		
B7	VSS		
H12	VSS		
H13	VSS		
K11	VSS		
K12	VSS		
K13	VSS		
D15	VSS		
E15	VSS		
F15	VSS		
G11	VSS		
J11	VSS		
J12	VSS		
K10	VSS		
H15	XTAL_AVSS		
K14	XTAL_AVSS		
B10	CORE_PMU_I_AVSS		
H14	AUXBUF_PMU_I_AVSS		
B2	PAD_I_AVSS		
E1	PAD_I_AVSS		
J1	PAD_I_AVSS		
N11	PAD_I_AVSS		
L2	PAD_I_AVSS		
P15	PAD_I_AVSS		
K2	PAD_I_AVSS		
L10	PAD_I_AVSS		
L15	PAD_I_AVSS		
M4	PAD_I_AVSS		
F5	PAD_I_AVSS		
P5	PAD_I_AVSS		
P8	PAD_I_AVSS		
H4	PAD_I_AVSS		

52 19 PP15V0_TOUCH_FILT
C2311 0.47UF 20% 25V CER-X5R 0201
C2312 0.47UF 20% 25V CER-X5R 0201
C2313 0.47UF 20% 25V CER-X5R 0201
C2317 0.47UF 20% 25V CER-X5R 0201
C2333 0.47UF 20% 25V CER-X5R 0201
C2334 0.47UF 20% 25V CER-X5R 0201
C2335 0.47UF 20% 25V CER-X5R 0201
C2315 0.1UF 10% 10V X5R-CERM 0201
C2316 0.1UF 10% 10V X5R-CERM 0201
C2320 0.22UF 20% 10V CERM-X5R 0201
C2378 100PF 5% 25V C0G 0201
C2379 12PF 5% 25V NP0-C0G 0201
C2302 0.1UF 10% 10V X5R-CERM 0201
C2303 0.1UF 10% 10V X5R-CERM 0201
C2304 0.1UF 10% 10V X5R-CERM 0201
C2305 0.1UF 10% 10V X5R-CERM 0201
C2306 0.1UF 10% 10V X5R-CERM 0201
C2307 2.2UF 10% 10V X5R-CERM 0402
C2318 1UF 10% 10V X5R-CERM 0402
C2321 0.1UF 10% 25V X5R 0201
C2322 0.047UF 10% 25V X5R 0201
C2308 0.1UF 10% 6.3V CERM-X5R 0201
C2309 0.1UF 10% 6.3V CERM-X5R 0201
C2310 0.1UF 10% 6.3V CERM-X5R 0201
C2325 1UF 10% 10V X5R-CERM 0402
C2314 0.1UF 10% 6.3V CERM-X5R 0201

BOOT OPTION

54 20 19 9 PP1V8_GRAPE_EXT_SW
R2301 10K 5% 1/32W MF 01005
R2303 10K 5% 1/32W MF 01005
20 KONA_BOOT0_S
20 KONA_BOOT1_S
R2302 10K 5% 1/32W MF 01005 NOSTUFF
R2304 10K 5% 1/32W MF 01005 NOSTUFF

SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016
PAGE TITLE
TOUCH: KONA SLAVE

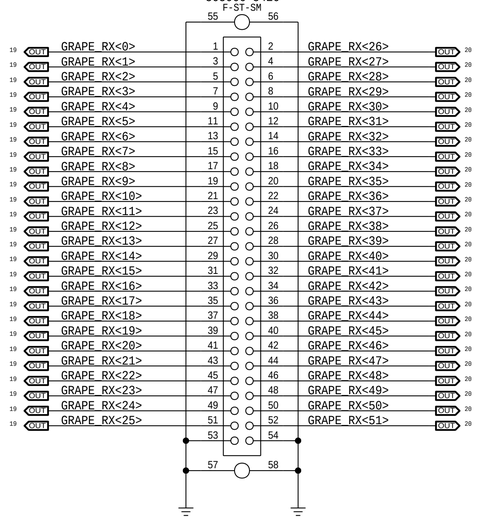
TOUCH FLEX CONNECTOR (SENSE)

MATCHES J207_GRAPE_FLEX 051-01606_3.0.0

MLB: 516S00063
FLEX: 516S00064

MOUNTING PINS CAN BE USED FOR ELECTRICAL CONNECTIONS

CRITICAL
J2400
505066-5420
F-ST-SM



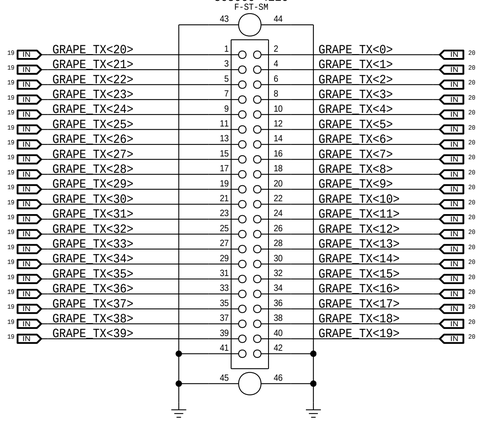
TOUCH FLEX CONNECTOR (DRIVE)

MATCHES J207_GRAPE_FLEX 051-01606_3.0.0

MLB: 516S00224
FLEX: 516S00225

MOUNTING PINS CAN BE USED FOR ELECTRICAL CONNECTIONS

CRITICAL
J2401
505066-4220
F-ST-SM



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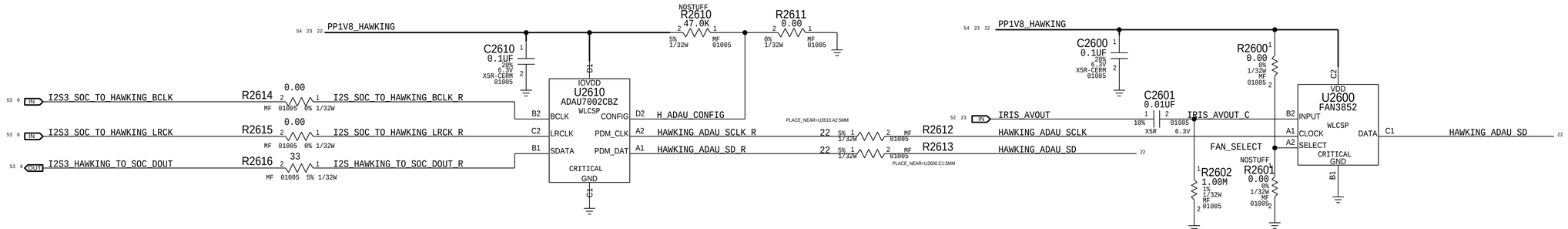
SYNC_DATE=07/29/2016

PAGE TITLE

TOUCH: GRAPE CONN

HAWKING



HAWKING ADAU CONFIG

0-OHM PULL UP	I2S FORMAT
0-OHM PULL DOWN	TDM SLOT 1 TO SLOT 2
OPEN	TDM SLOT 3 TO SLOT 4
47K-OHM PULL UP	TDM SLOT 5 TO SLOT 6
47K-OHM PULL DOWN	TDM SLOT 7 TO SLOT 8

FAN3850 SELECT INPUT

GND	RISING EDGE SELECT
VDD	FALLING EDGE SELECT

SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

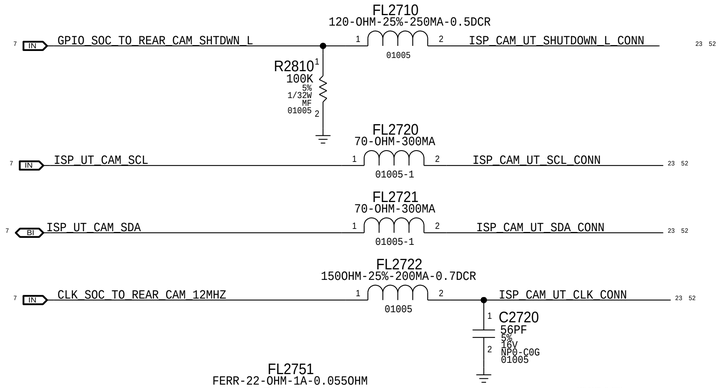
HAWKING

CORNER3 XFER FLEX B2B

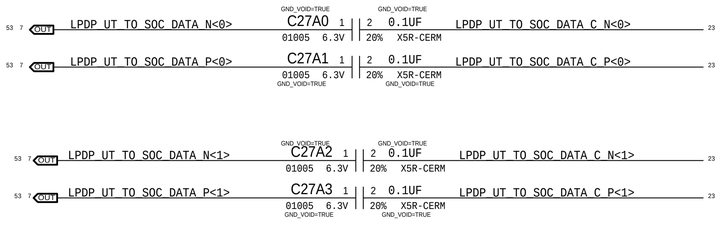
MATCHES J207_C3_TRANSFER_B2B_FLEX_051-01950_0.5.0

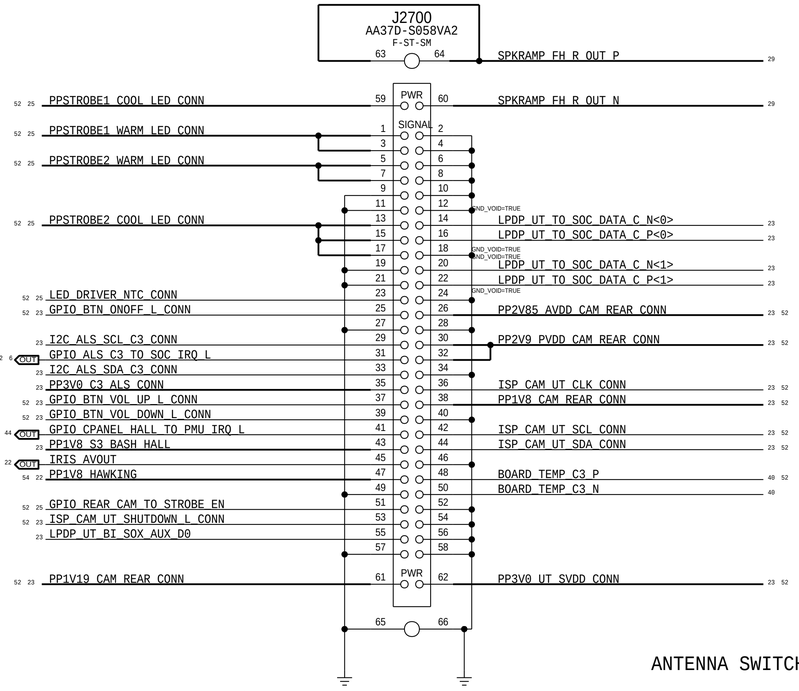
MLB: 516S00259
FLEX: 516S00260

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00017	155S0755		FL2771, ETC	QUALIFIED IN J127

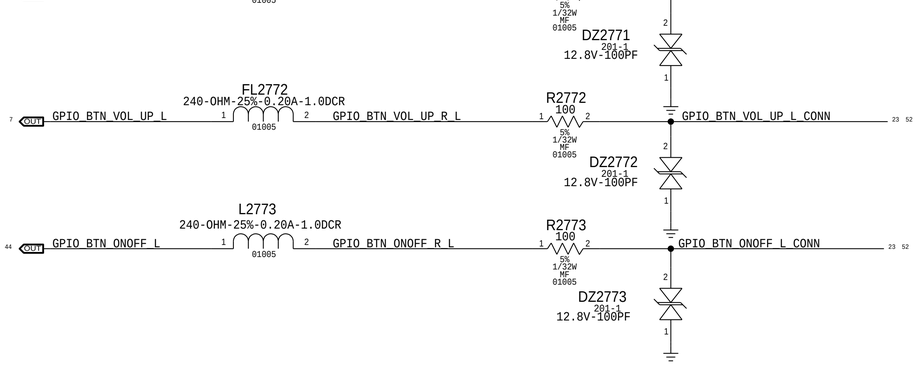


LPDP AC COUPLING CAPS



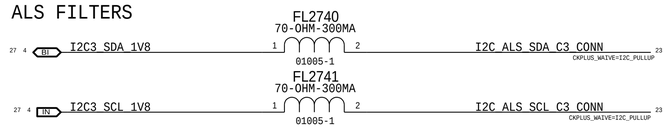


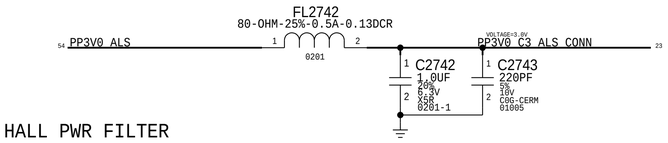
BUTTON FILTERS/ESD



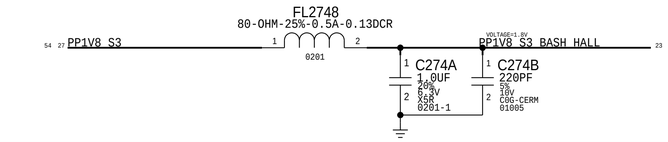
ANTENNA SWITCH FILTERS

ALS FILTERS





HALL PWR FILTER



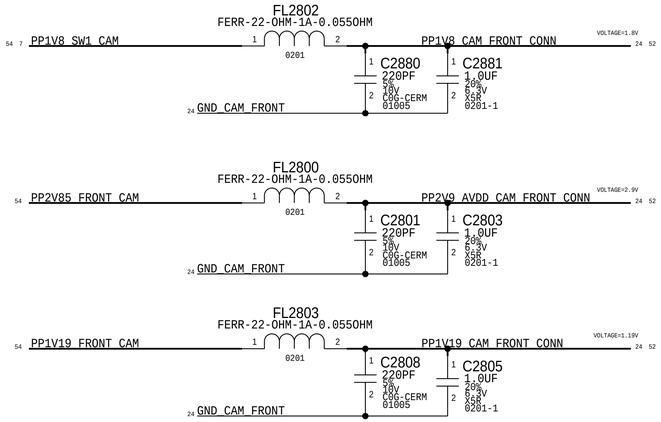
SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016

PAGE TITLE

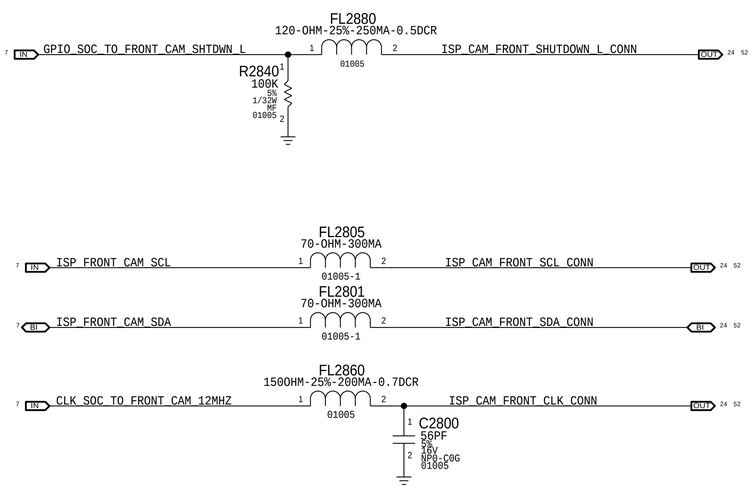
FLEX CONNS: CORNER 3

FRONT CAMERA (NH)

POWER FILTERS



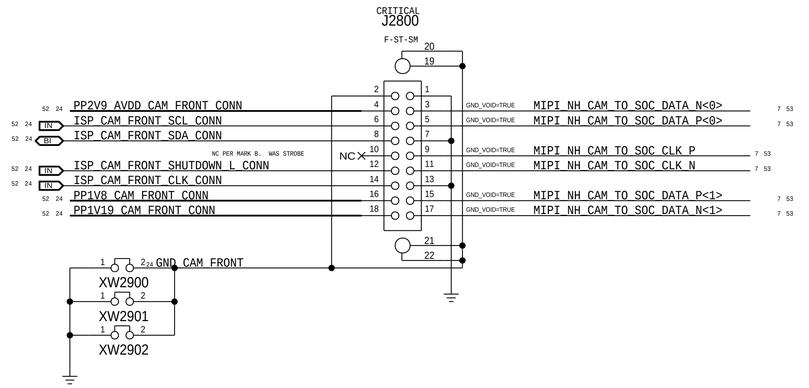
IO FILTERS



FRONT CAMERA CONNECTOR

MATCHES J120_FRONT_CAM_FLEX_051-01272_2.0.0

FLEX SIDE: 516S00194
MLB SIDE: 516S00193



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00200	155S0610		FL2860,ECT	RDAR://PROBLEM/12850271

SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

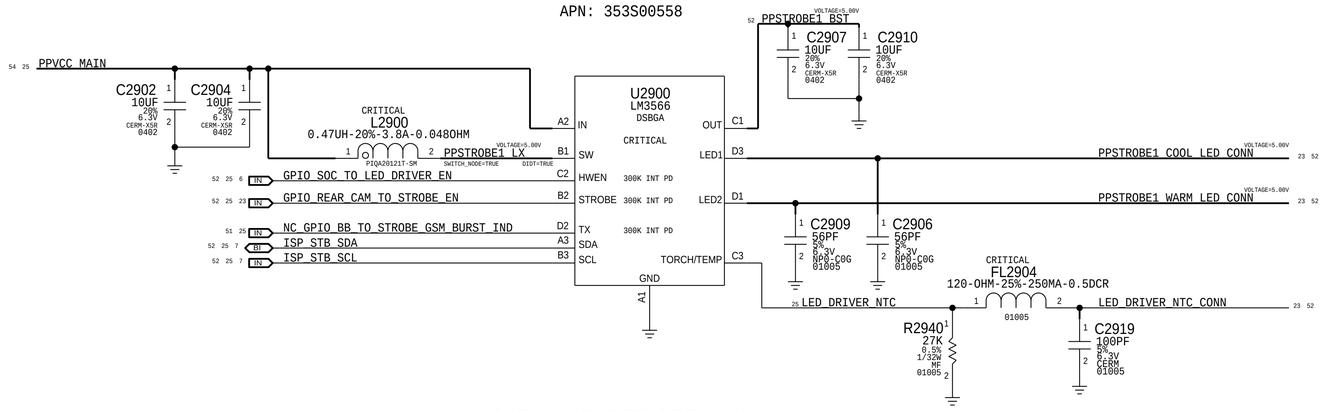
CAMERA: FRONT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0875	138S0678		C2902, ETC	RDAR://PROBLEM/26929420

STROBE CIRCUITRY

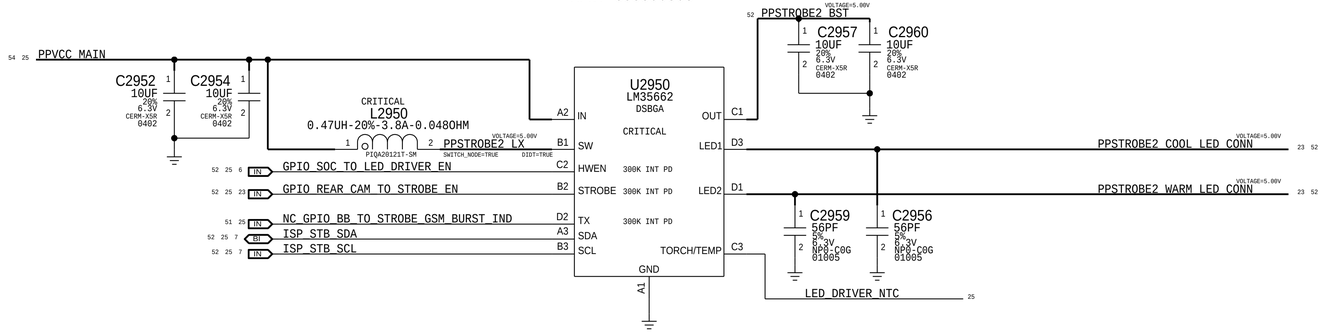
LED DRIVER 1

APN: 353S00558



LED DRIVER 2

APN: 353S00868



SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

CAMERA: STROBE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0661	155S0511		L3000,ECT	RDAR://PROBLEM/12639854
138S0847	138S0786		C3010	

CLIFDEN

54 26 PP1V8_S2_EXT_SW2
R3098 10K 5% 1/32W MF 01005
R3099 10K 5% 1/32W MF 01005
26 8 GPIO_SOC_TO_BELFIELD_RESET_L
26 8 GPIO_SOC_TO_CODEC_RESET_L

54 PP1V8_S2_VA_VCP
C3001 4.7UF 20% 6.3V X5R 402 CRITICAL
C3003 0.1UF 10% 6.3V CERM-X5R 0201 CRITICAL
C3009 2.2UF 20% 6.3V X5R-CERM 0201 CRITICAL
C3051 2.2UF 20% 6.3V X5R-CERM 0201 CRITICAL
52 26 GND_AUDIO_CODEC
L83_PVCP
L83_NVCP
C3008 4.7UF 20% 6.3V X5R 402 CRITICAL
C3007 4.7UF 20% 6.3V X5R 402 CRITICAL
54 26 PPVCC_MAIN
R3019 10K 5% 1/32W MF 01005 VL_SEL

U3000
CS42L83A
WLCSP-SKT

VCP	B6	
VA	B1	
VD_FILT	A1	NC
VL	A2	
VP	B7	
+VCP_FILT	E6	
-VCP_FILT	G6	
GNDCP	F6	
VL_SEL	C4	
DIGLDO_PDN*	D4	
INT*	B7	53 6 OUT GPIO_CODEC_TO_SOC_IRQ_L
WAKE*	C6	52 44 OUT GPIO_CODEC_TO_PMU_WAKE_L
RESET*	C5	26 8 IN GPIO_SOC_TO_CODEC_RESET_L
SPDIF_TX	A6	NC
SWIRE_SEL	D3	
ASP_LRCK/FSYNC	B5	53 9 IN I2S_AOP_TO_CODEC_LRCK
SWIRE_SD/ASP_SDIN	A5	53 9 IN I2S_AOP_TO_CODEC_DOUT
ASP_SDOUT	A4	I2S_CLIFDEN_TO_AOP_DOUT_R
SWIRE_CLK/ASP_SCLK	B4	53 9 IN I2S_AOP_TO_CODEC_BCLK
AD0	C3	
AD1	B2	
SDA	A1	4 BI I2C2_SDA_1V8
SCL	A2	4 IN I2C2_SCL_1V8
FLYP	E7	
FLYC	F7	
FLYN	G7	
FILT_P	C1	
GNDA	D2	
GNDHS	C2	
GNDD	G1	
GNDD	C7	
GNDD	B6	
GNDL	B3	

53 9 OUT I2S_CODEC_TO_AOP_DOUT
R3011 22 5% 1/32W MF 01005

CRITICAL C3005 4.7UF 20% 6.3V X5R 402 L83_FLYP
L83_FLYC
CRITICAL C3006 4.7UF 20% 6.3V X5R 402 L83_FLYN
L83_FILT
C3010 10UF 20% 10V X5R-CERM 0402-3
52 26 GND_AUDIO_CODEC VOLTAGE=0V
XW3000 SM

PLACE_NEAR=U3000.A15MM
C3002 0.1UF 20% 6.3V X5R-CERM 0201
54 PP1V8_S2_EXT_SW2
C3004 0.1UF 20% 6.3V CERM-X5R 0201
C3040 10UF 20% 6.3V CERM-X5R 0402-9 CRITICAL
C3041 10UF 20% 6.3V CERM-X5R 0402-9 CRITICAL
C3042 10UF 20% 6.3V CERM-X5R 0402-9 CRITICAL
PPVCC_MAIN

HPSENSA	D5	
HPOUTA	E5	CODEC_HP_LEFT
HPSENSB	F5	
HPOUTB	G5	CODEC_HP_RIGHT
HS4	F1	CODEC_HP_HS4
HS_CLAMP2	E2	
HSIN+	E1	CODEC_HP_HSINP
HS3	G2	CODEC_HP_HS3
HS_CLAMP1	F2	
HSIN-	D1	CODEC_HP_HSINN
HS4_REF	F4	CODEC_HP_HS4_REF
HS3_REF	G4	CODEC_HP_HS3_REF
RING_SENSE	G3	NC
TIP_SENSE	E4	CODEC_HP_DET
HSBIAS_FILT	F3	HSBIAS_FILT
HSBIAS_FILT_REF	E3	HSBIAS_FILT_REF

SM XW3006 NO_XNET_CONNECTION=1
SM XW3007 NO_XNET_CONNECTION=1
CRITICAL C3012 4.7UF 20% 6.3V X5R 402
R3020 3.3K 5% 1/32W MF 01005
R3021 1.00K 5% 1/32W MF 01005
R3022 1.00K 5% 1/32W MF 01005

L3000 FERR-33-OHM-0.8A-0.09-OHM 0201 CRITICAL — CODEC_HP_LEFT_CONN OUT 27 52
L3001 FERR-33-OHM-0.8A-0.09-OHM 0201 CRITICAL — CODEC_HP_RIGHT_CONN OUT 27 52
L3002 FERR-33-OHM-0.8A-0.09-OHM 0201 CRITICAL — CODEC_HP_HS4_CONN IN 27 52
L3003 FERR-33-OHM-0.8A-0.09-OHM 0201 CRITICAL — CODEC_HP_HS3_CONN IN 27 52
L3004 FERR-33-OHM-0.8A-0.09-OHM 0201 CRITICAL — CODEC_HP_HS4_REF_CONN IN 27 52
L3005 FERR-33-OHM-0.8A-0.09-OHM 0201 CRITICAL — CODEC_HP_HS3_REF_CONN IN 27 52
L3020 240-OHM-0.2A-0.8-OHM 0201-2 — CODEC_HP_HEADSET_DET_CONN IN 27 52

C3033 470PF 10% 16V CER-X7R 01005 NOSTUFF
C3034 470PF 10% 16V CER-X7R 01005 NOSTUFF
C3035 470PF 10% 16V CER-X7R 01005 NOSTUFF
RDAR//PROBLEM/26018872
CODEC_HP_DET_R
C3020 470PF 10% 16V CER-X7R 01005 NOSTUFF

BELFIELD

54 26 PPVCC_MAIN
C3062 0.1UF 10% 16V XSR-CERM 0201
PP1V8_S2_EXT_SW2 26 54
C3061 0.1UF 20% 6.3V X5R-CERM 01005
NC

U3050
CS46L10
WLCSP
CRITICAL

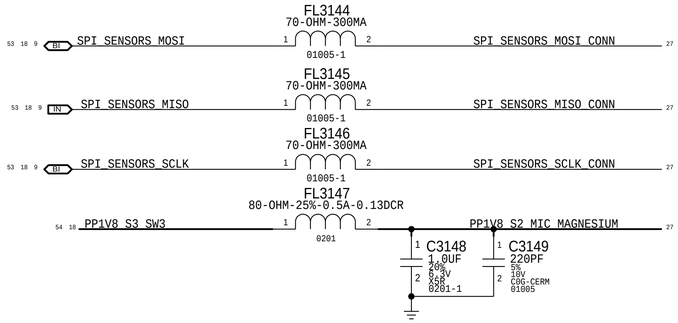
VP	D5	
VD	B5	
VD_FILT	A5	
WAKE*	D2	52 44 OUT GPIO_BELFIELD_TO_PMU_WAKE_L
INT*	D3	52 6 OUT GPIO_BELFIELD_TO_SOC_IRQ_L
RESET*	D4	26 8 IN GPIO_SOC_TO_BELFIELD_RESET_L
MCLK	B1	53 6 IN I2S0_SOC_TO_BELFIELD_MCLK
SCLK	A1	53 6 IN I2S0_SOC_TO_BELFIELD_BCLK
LRCK/FSYNC	B2	53 6 IN I2S0_SOC_TO_BELFIELD_LRCK
AD2/SDOUT	A2	53 6 OUT I2S0_BELFIELD_TO_SOC_DOUT
SDIN	A3	53 6 IN I2S0_SOC_TO_BELFIELD_DOUT
AD0/CS_L	B3	53 6 IN SPI_BELFIELD_CS_L
SCL/CCLK	A4	53 6 IN SPI_BELFIELD_SCLK
AD1/MOSI	C4	53 6 IN SPI_BELFIELD_MOSI
SDA/MISO	B4	53 6 OUT SPI_BELFIELD_MISO
DIGLDO_PDN	C3	
D+	D1	BELFIELD_MBUS_P
D-	C1	BELFIELD_MBUS_N
MBUS_REF	C2	BELFIELD_MBUS_REF IN 30
GND	C5	

C3030 100PF 5% 16V NP0-C0G 01005
R3030 12 5% 1/20W MF 201
C3031 100PF 5% 16V NP0-C0G 01005 NOSTUFF NO_XNET_CONNECTION=1
R3031 12 5% 1/20W MF 201
C3032 100PF 5% 16V NP0-C0G 01005
MIKEY_TS_P BI 48 52
MIKEY_TS_N BI 48 52

SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016
PAGE TITLE
AUDIO: CLIFDEN, BELFIELD

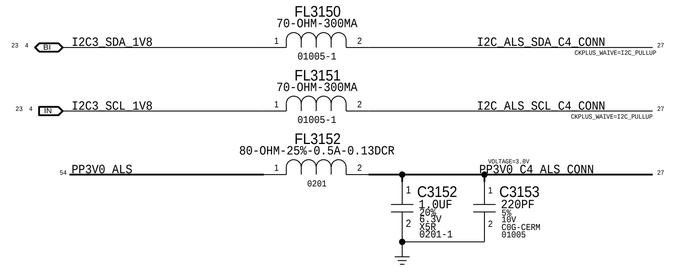
CORNER 4 + DMIC FLEX FILTERS

MAGNESIUM SPI FILTERS

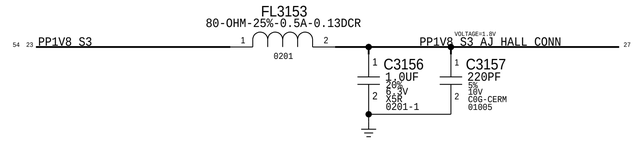


ANTENNA SWITCH FILTERS

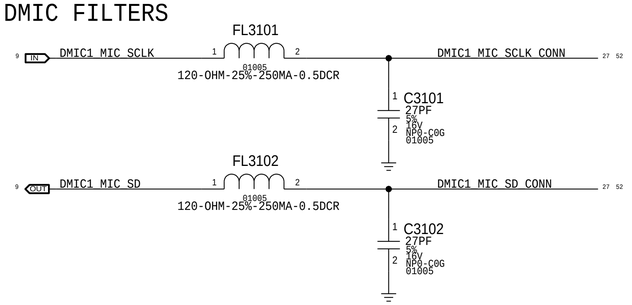
ALS FILTERS



HALL FILTER



DMIC FILTERS

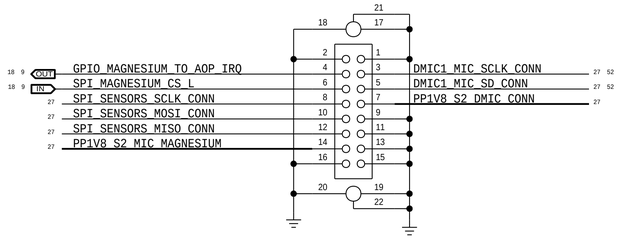


MIC FLEX B2B

MATCHES J207_MIC_FLEX_051-01915_0.5.0

MLB APN: 516S1278
FLEX APN: 516S1280

CRITICAL
J3100
24-5857-016-201-829
F-ST-SM



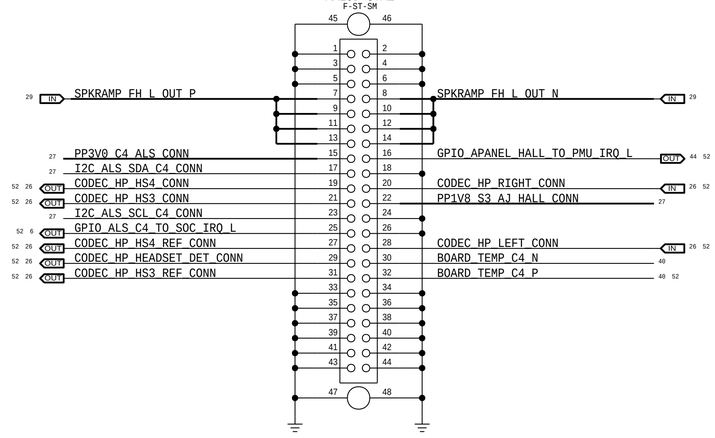
ROUTING	BUS	SELECT	LOCATION	DATA ASSERTS ON	DATA LATCHED ON
MIC1	DMIC1	HIGH	CENTER SPLINE	CLK RISING EDGE	CLK FALLING EDGE
MIC2	DMIC1	LOW	REAR	CLK FALLING EDGE	CLK RISING EDGE

CORNER 4 B2B

MATCHES J207_C4_TRANSFER_FLEX_051-01724_2.16.0

MLB APN: 516S00222
FLEX APN: 526S00223

J3150
AA29D-SVA1
F-ST-SM

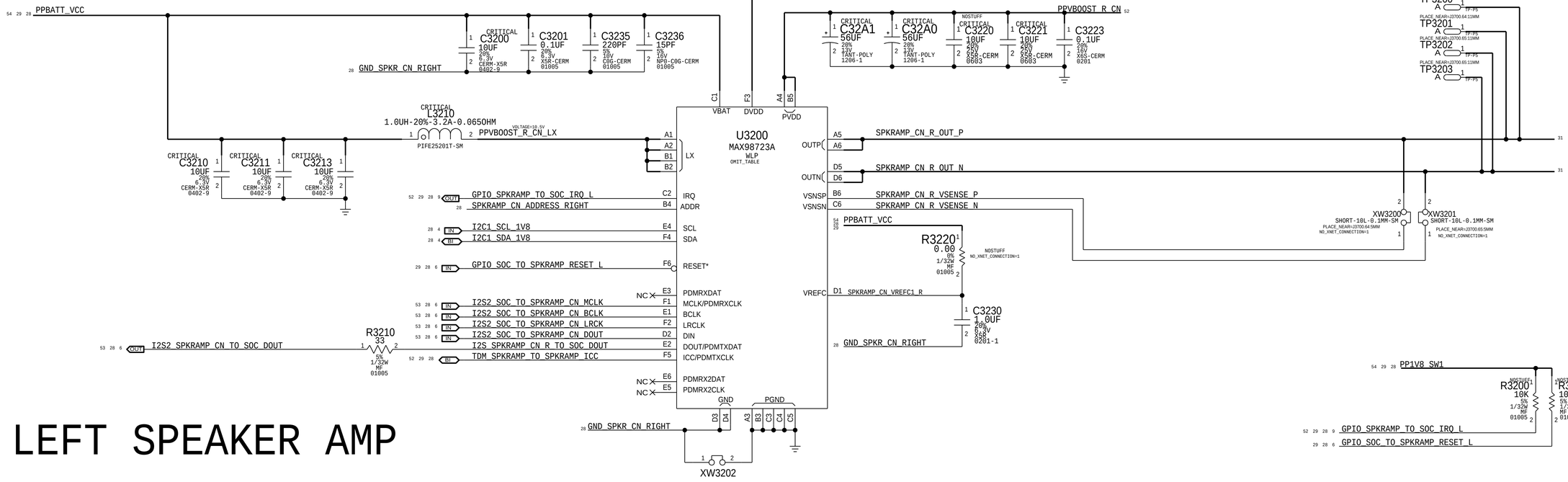


SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016

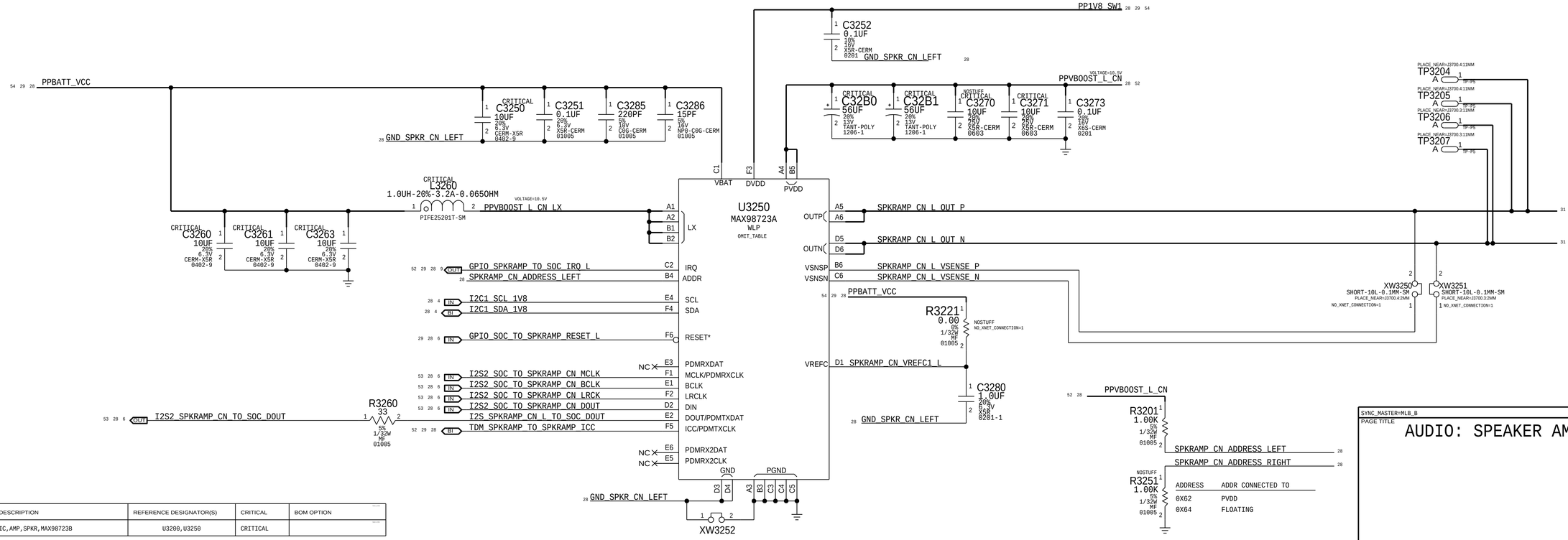
PAGE TITLE

FLEX CONNS: C4 & DMIC

CN RIGHT SPEAKER AMP



CN LEFT SPEAKER AMP



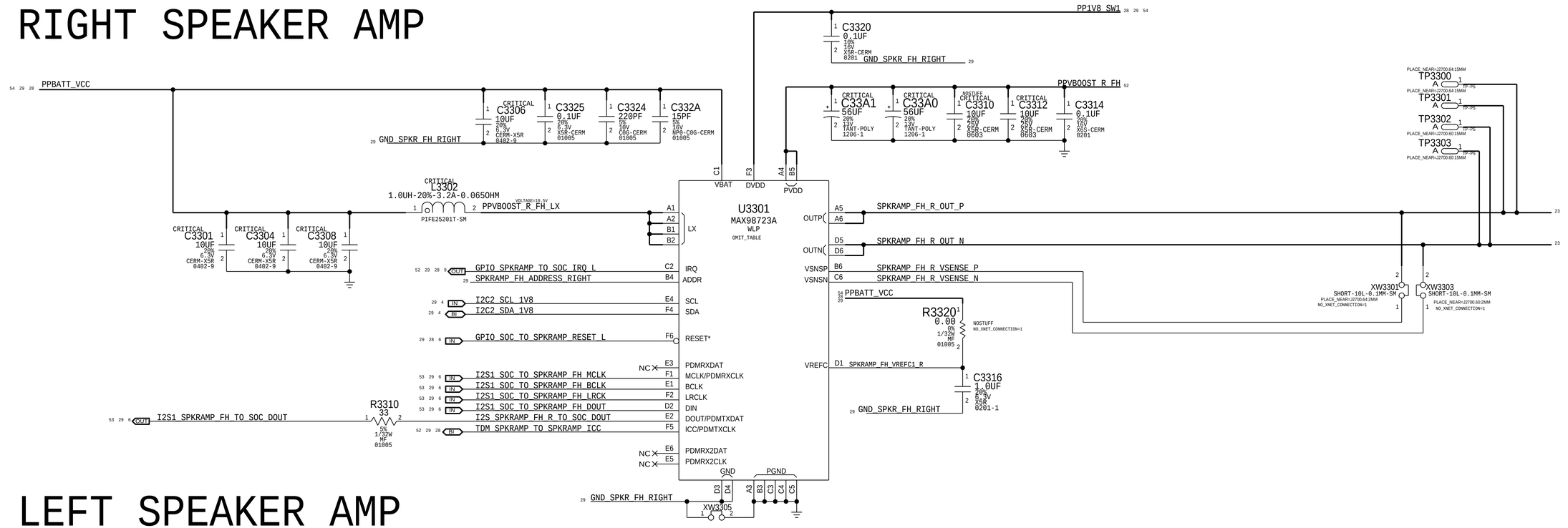
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01072	1	IC,AMP,SPKR,MAX98723B	U3200,U3250	CRITICAL	

SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

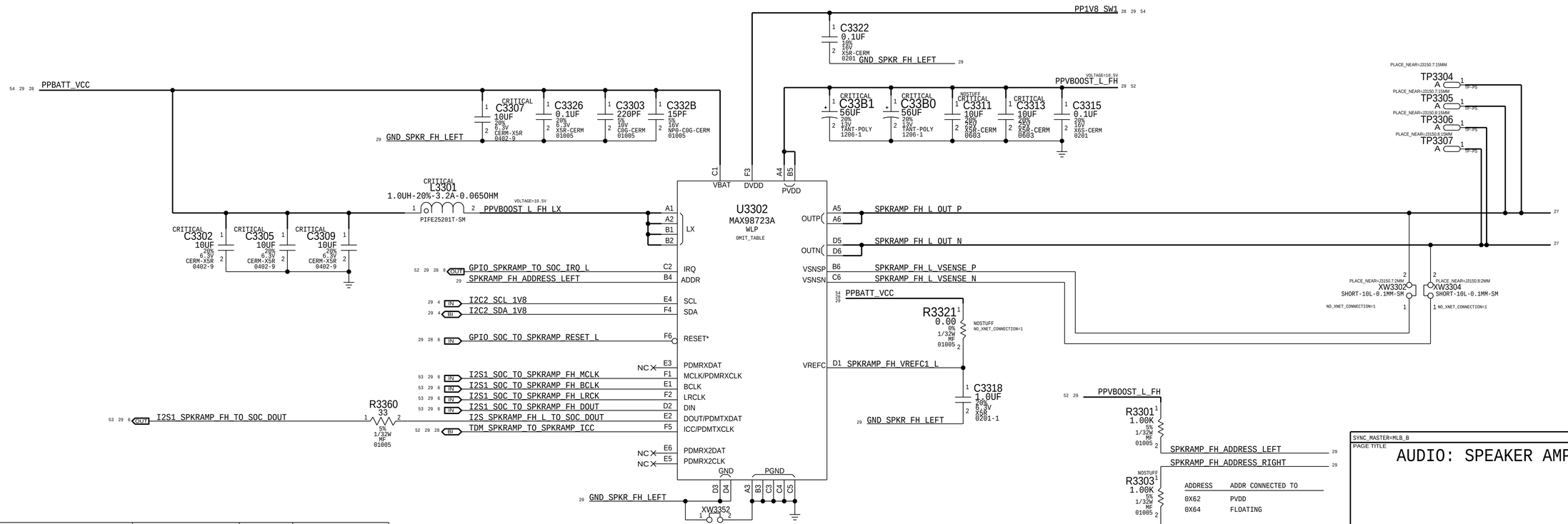
PAGE TITLE

AUDIO: SPEAKER AMPS (CN)

FH RIGHT SPEAKER AMP



FH LEFT SPEAKER AMP



ADDRESS	ADDR CONNECTED TO
0X62	PVDD
0X64	FLOATING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01072	1	IC,AMP,SPKR,MAX98723B	U3301,U3302	CRITICAL	

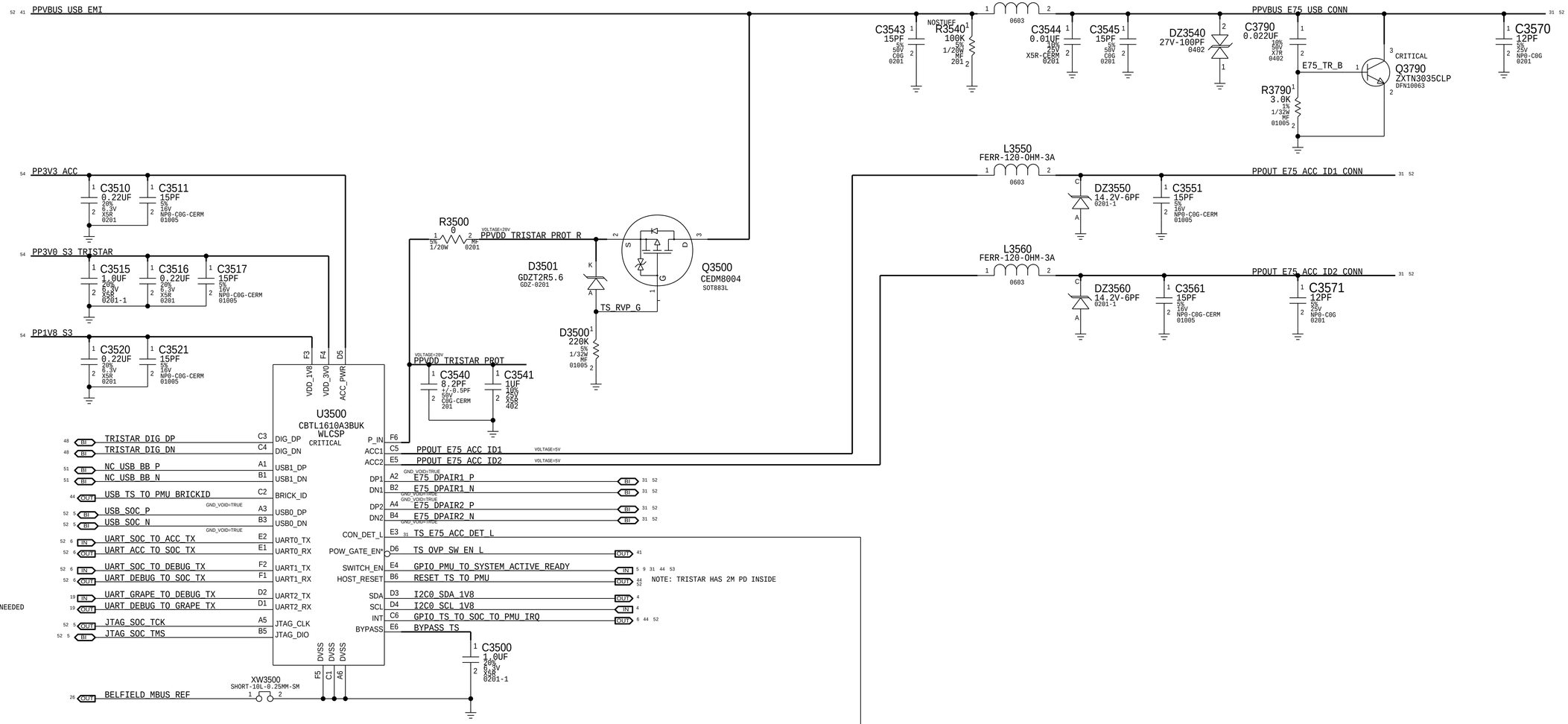
SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016
PAGE TITLE

AUDIO: SPEAKER AMPS (FH)

TRISTAR

TRISTAR TX IS AN INPUT
AND ITS RX IS AN OUT

TODO: CHECK IF THIS IO IS NEEDED



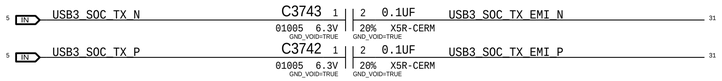
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0116	377S0108		DZ3540	RDAR://PROBLEM/8370432

SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

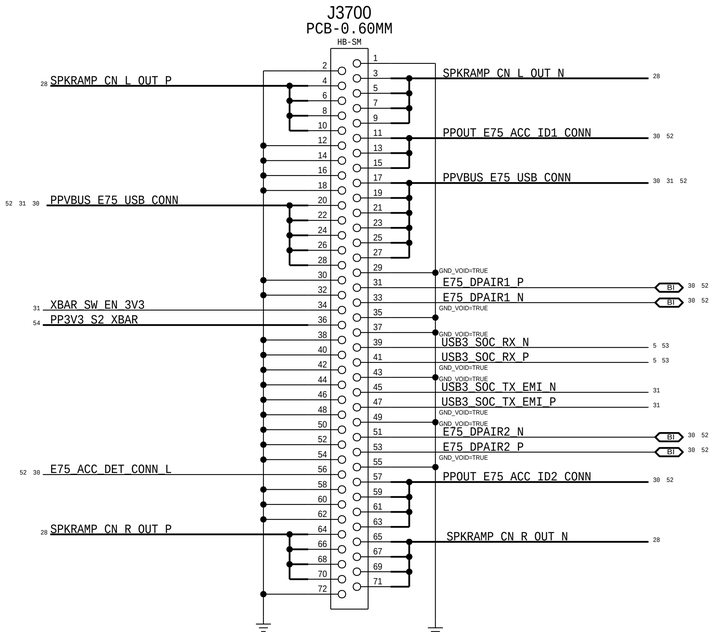
IO: TRISTAR

USB3 DC BLOCKING CAPS

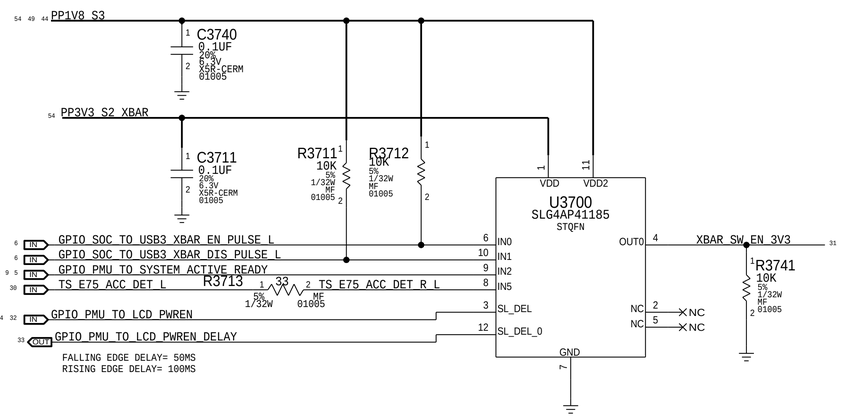


HOTBAR CONNECTOR TO I/0 FLEX

MATCHES J207_IO_FLEX_051-01873_1.0.0
MLB APN: 998-01935
FLEX APN: 998-01936



XBAR SWITCH GLUE LOGIC & LCD PWR DELAY



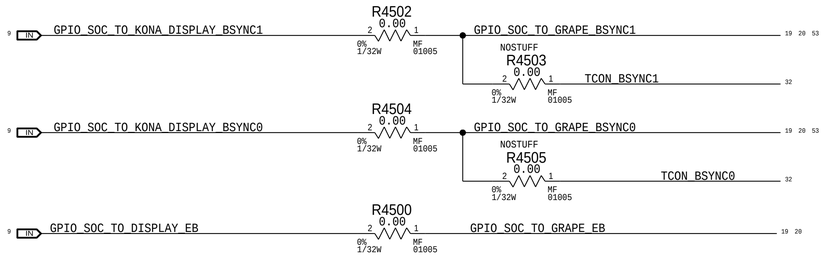
SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

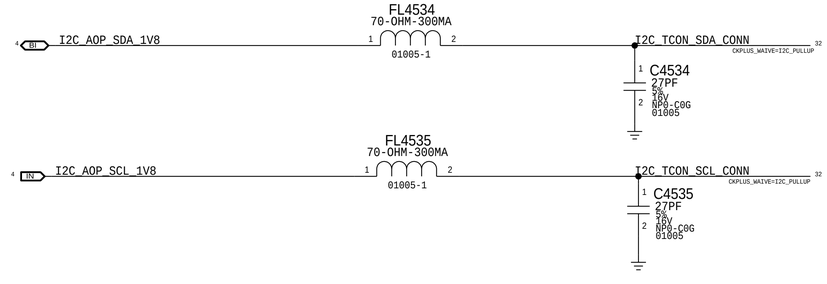
IO: HOTBAR,SIM,XBAR

EDP FLEX FILTERS AND CONNECTORS

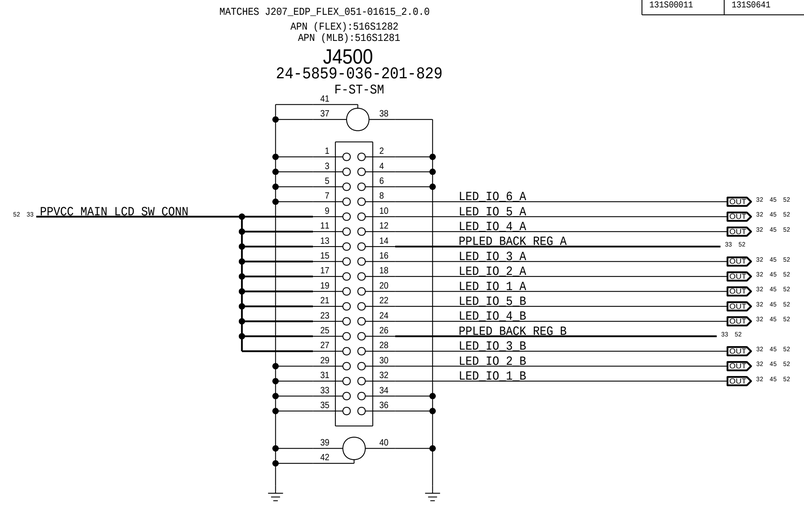
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
131S00011	131S0641		C4502,ETC	RADAR://PROBLEM/15682101



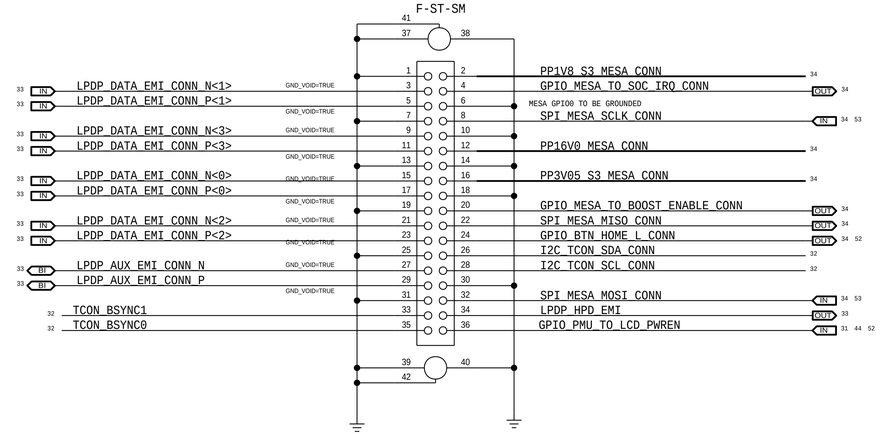
TCON I2C FILTERS



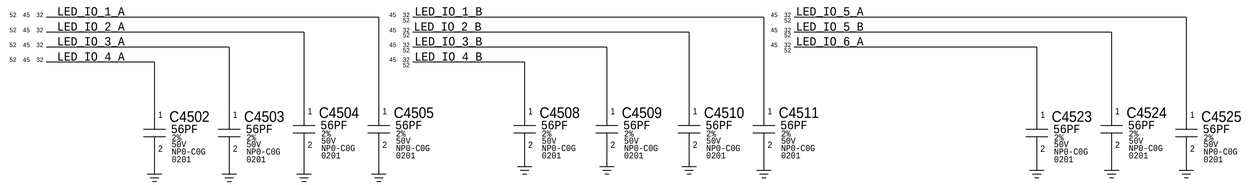
MATCHES J207_EDP_FLEX_051-01615_2.0.0
APN (FLEX):516S1282
APN (MLB):516S1281



MATCHES J207_EDP_FLEX_051-01615_2.0.0
APN (FLEX): 516S1282
APN (MLB): 516S1281



LED DRIVER FILTERS



SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016

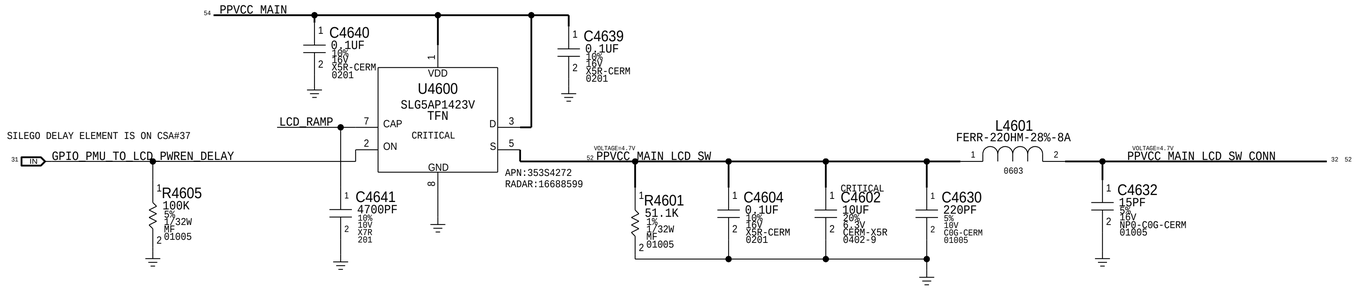
PAGE TITLE

DISPLAY CONN

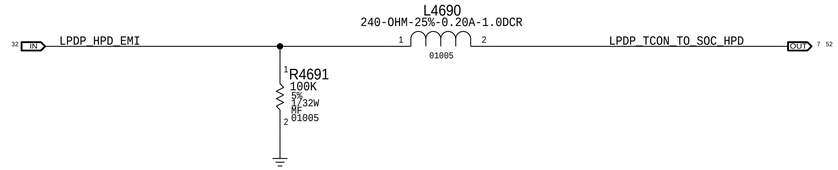
EDP CONNECTOR SUPPORT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0914	155S0897		L4602,ETC	RADAR://PROBLEM/21527418

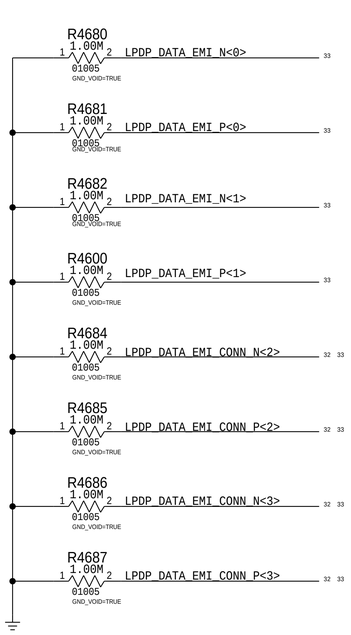
DISPLAY PWR SWITCH

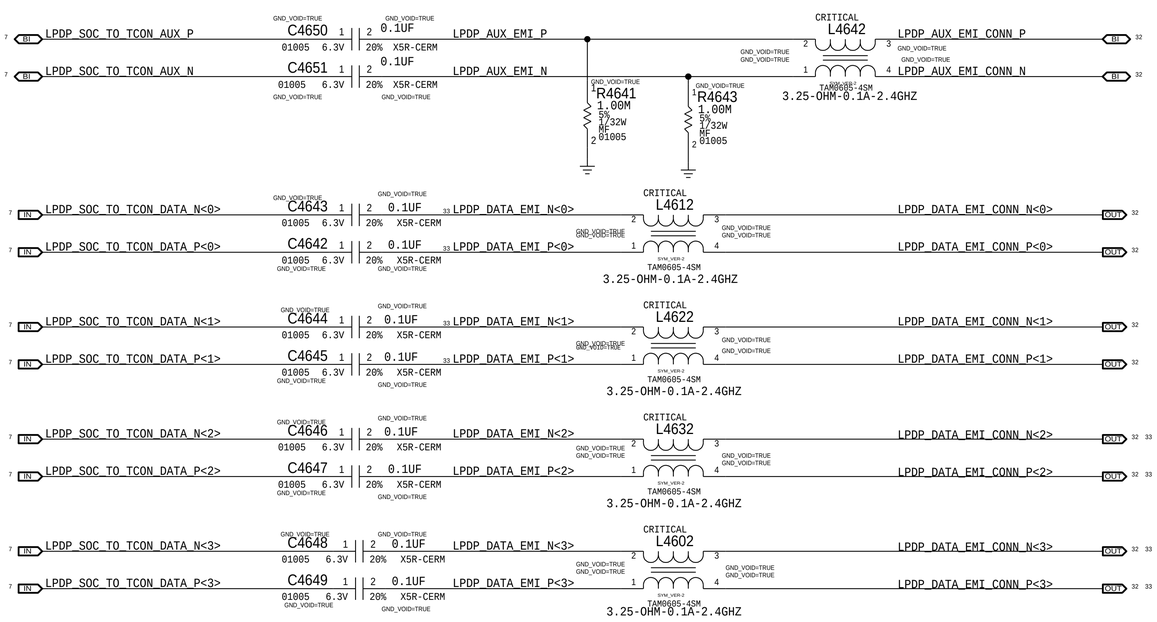


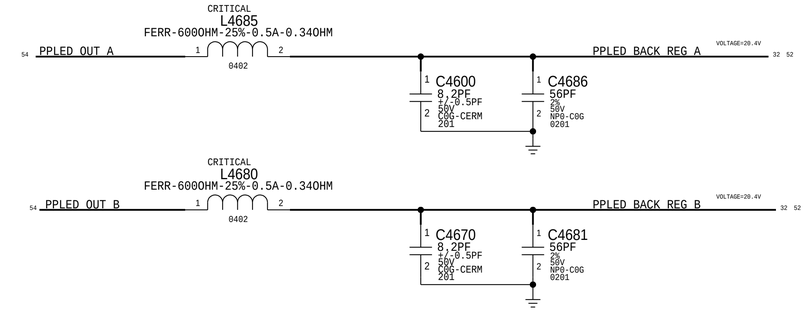
HIBISCUS HPD VOLTAGE IS 1.8V COMPATIBLE, VOLTAGE DIVIDER REMOVED
VOLTAGE DIVIDER REFERENCE IN PREVIOUS PLATFORMS; RDAR://PROBLEM/15390794



LPDP-AC COUPLING & CMC







SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

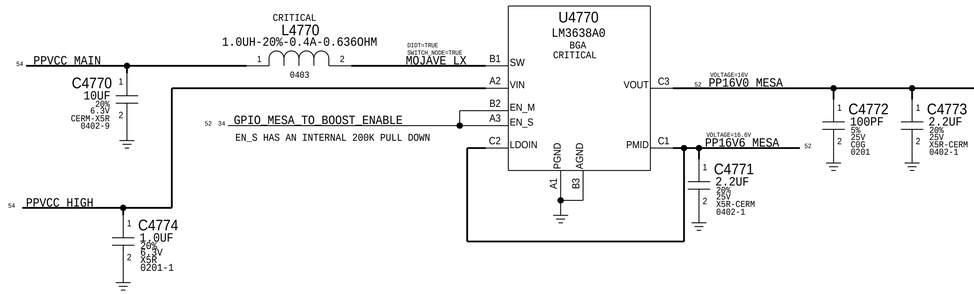
DISPLAY: EDP SUPPORT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00088	132S0639		C4746, ETC	RDAR://PROBLEM/26928883

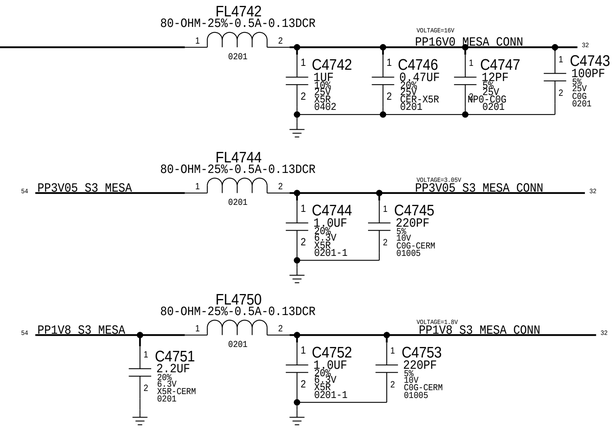
MESA & HOME BUTTON

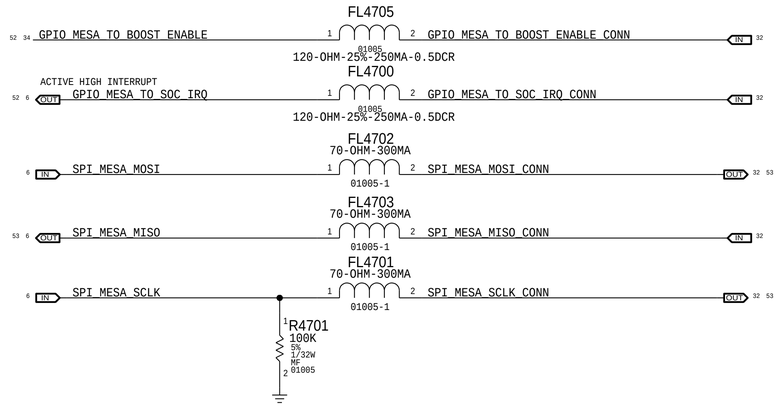
MOJAVE

USING A0 (APN 353S00671)

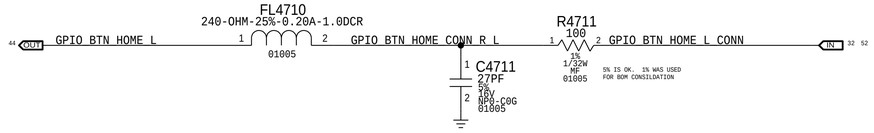


FILTERS





HOME BUTTON FILTERS

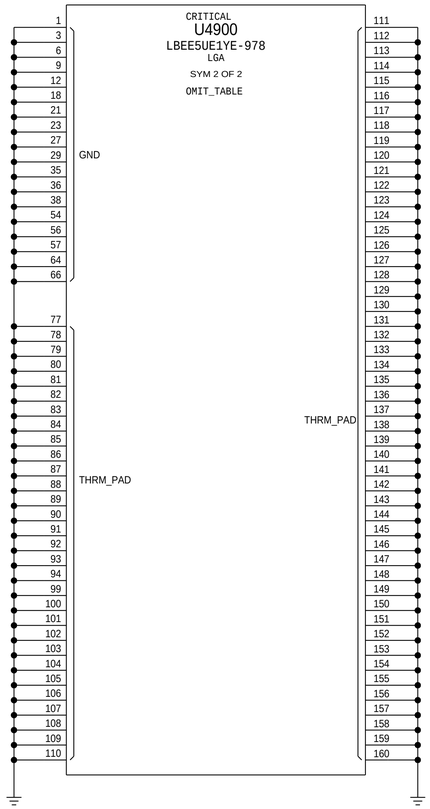


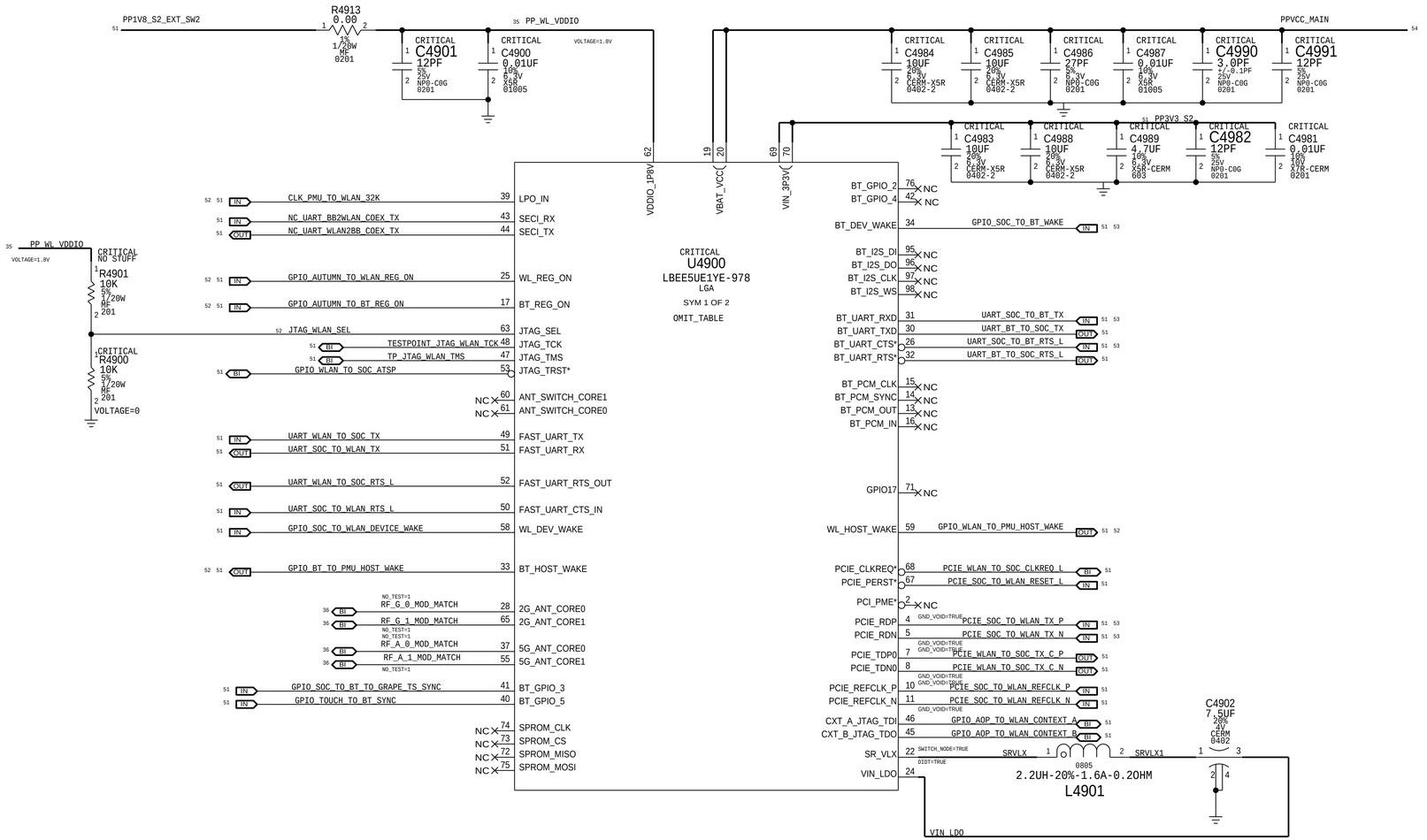
SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

SENSOR: MESA

WIFI/BT: J207/208: YEBISU MODULE, POWER, I/O





MODULE: USI ALTERNATES FOR MUR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00246	339S00248		U4900	USI ALT FOR MUR
339S00247	339S00249		U4900	CIDRE USI ALT FOR MUR

MODULE: BOM OPTION FOR CIDRE IN MLB_A, NOT IN MLB_B

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00248	1	YEBISU MURATA ES2	U4900	CRITICAL	MLB_B
339S00249	1	YEBISU CIDRE MURATA ES2	U4900	CRITICAL	MLB_A

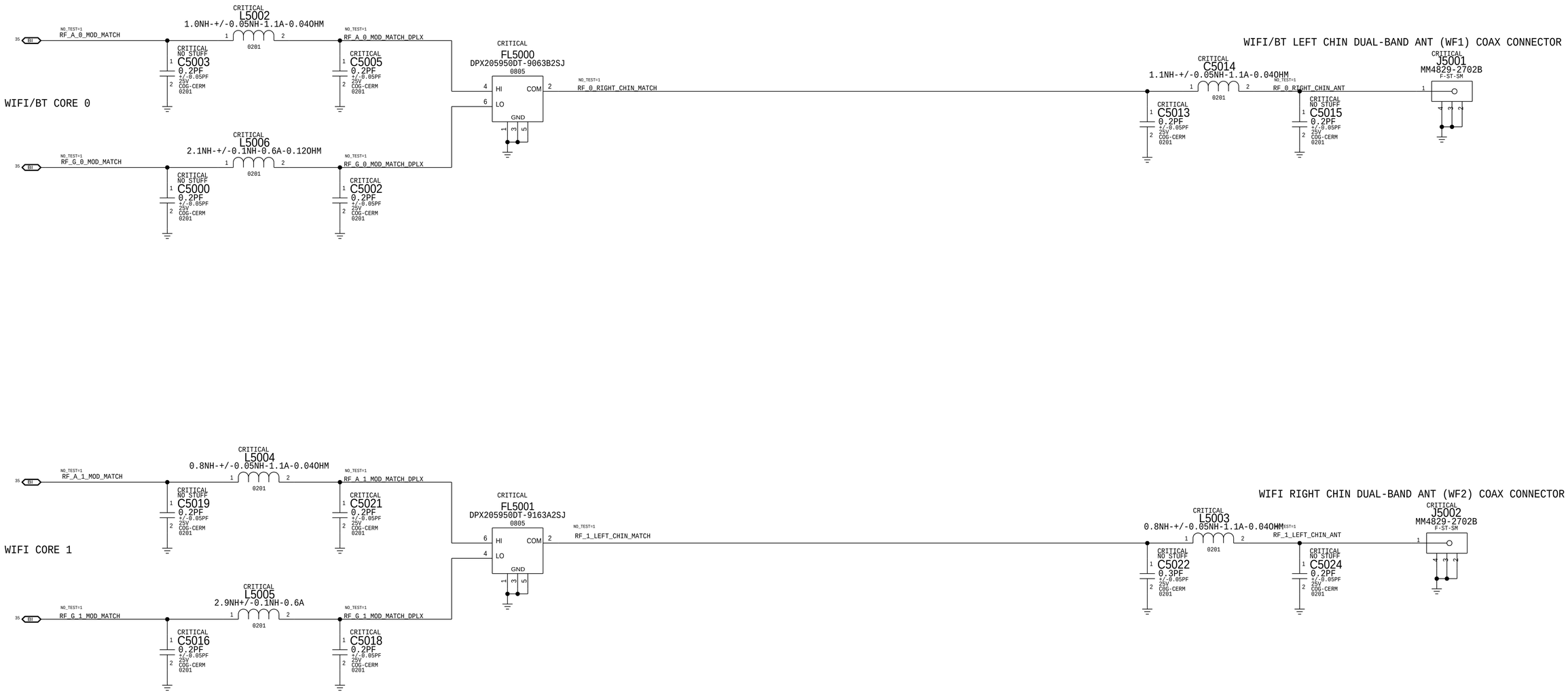
LAST UPDATED: 09/29/2016

SYNC_MASTER=WIFI_MLB SYNC_DATE=09/30/2016

PAGE TITLE

WIFI/BT: MODULE

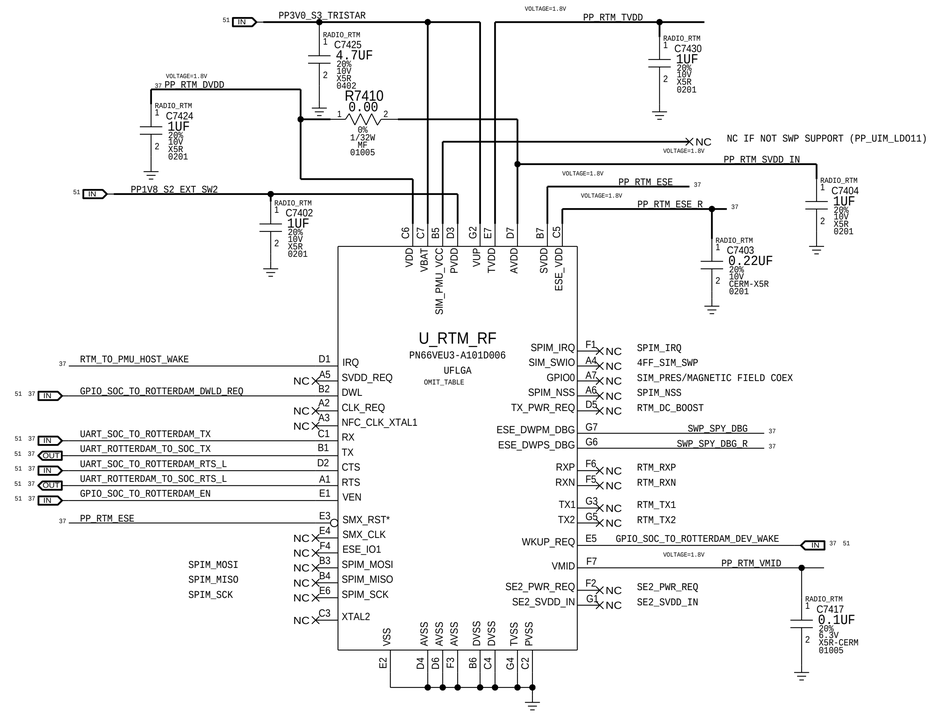
WIFI/BT: J207 (WIFI/BT ONLY) RF FRONT END



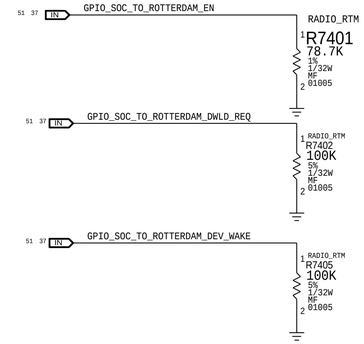
LAST UPDATED: 09/29/2016

SYNC_MASTER=WIFI_MLB	SYNC_DATE=09/30/2016
PAGE TITLE	
WIFI/BT: J207 FRONT END	

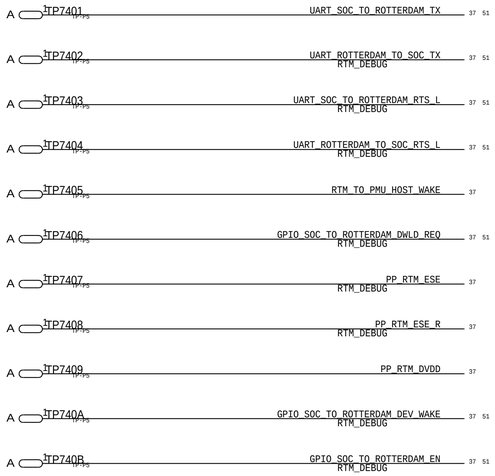
RTM/SECURE ELEMENT



SUPPORT PULLS

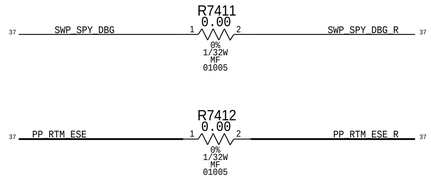


TEST POINTS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00157	1	ROTTERDAM,PN67VEU3	U_RTM_RF	CRITICAL	

IMPORTANT
DEBUG FEATURES

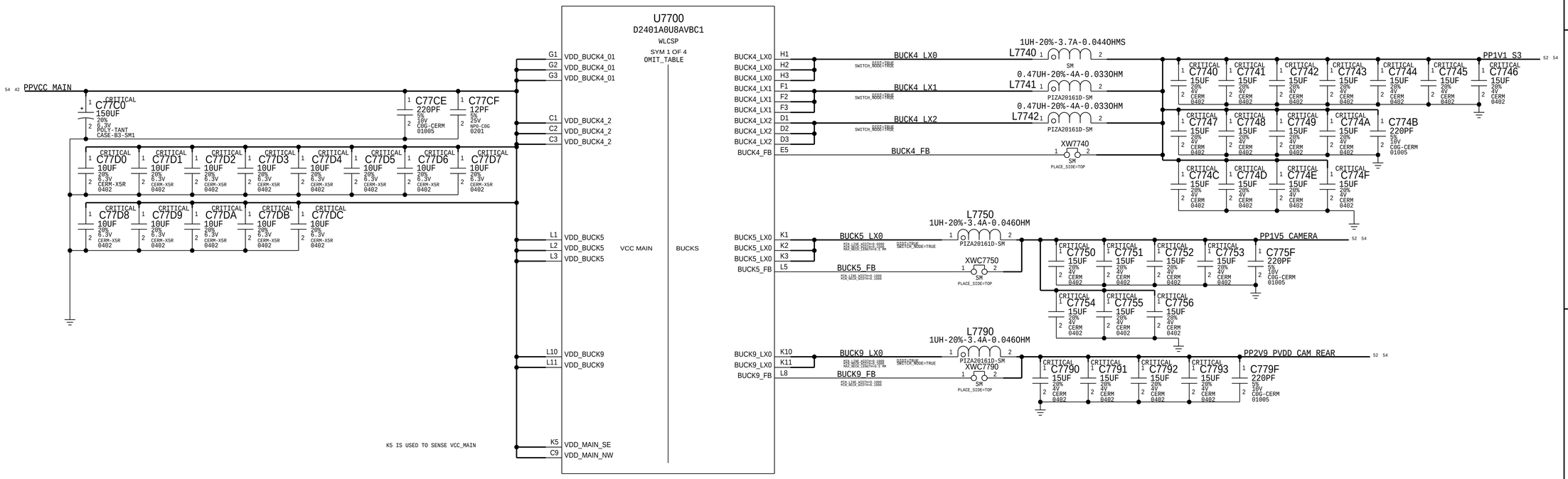


SYNC_MASTER=MLB_B
SYNC_DATE=08/26/2016

PAGE TITLE

STOCKHOLM

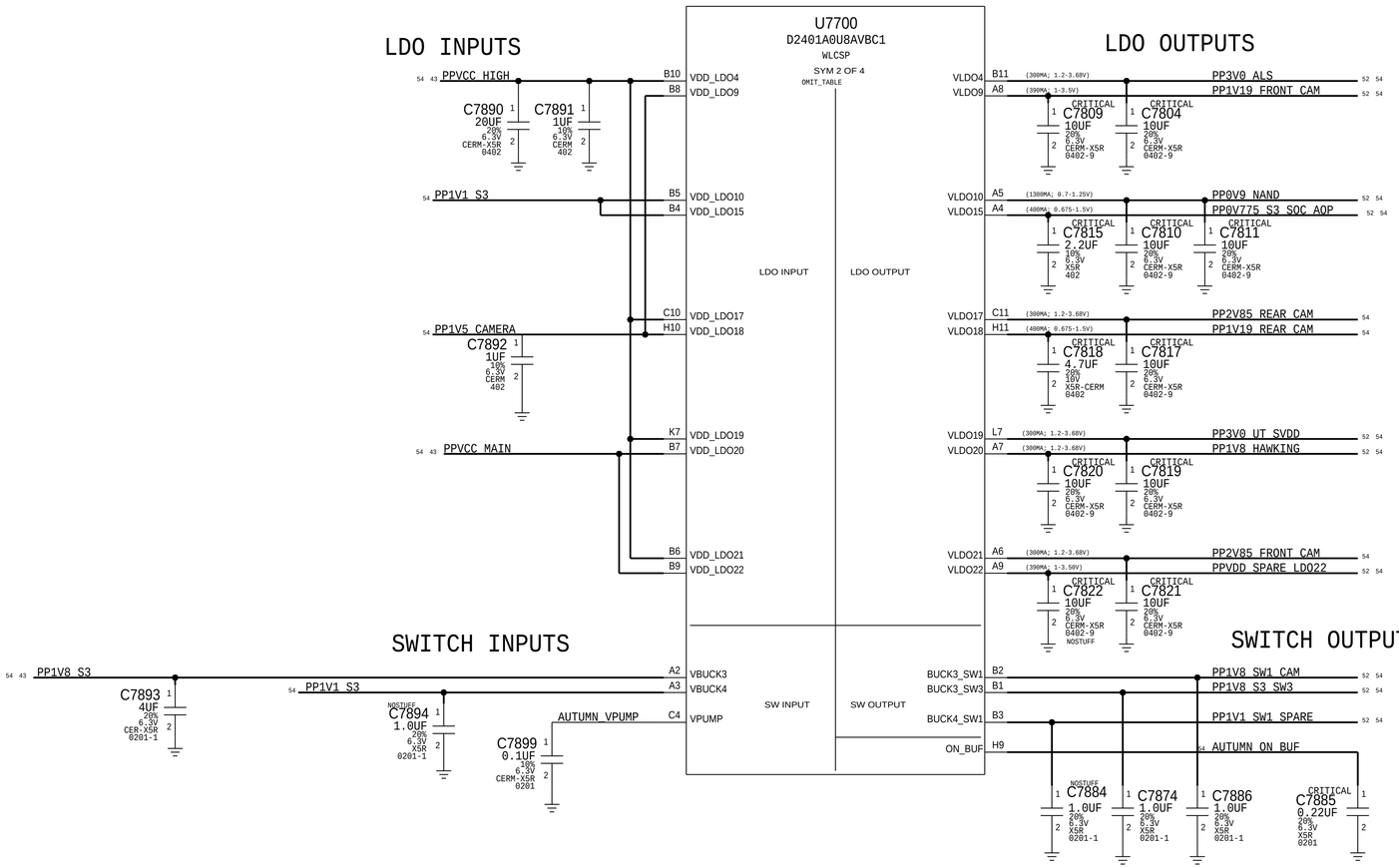
AUTUMN BUCKS



SYNC_MASTER=MLB_B	SYNC_DATE=07/29/2016
PAGE TITLE	
POWER: AUTUMN (1/3)	

AUTUMN LDOS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00071	138S00116		C7893	

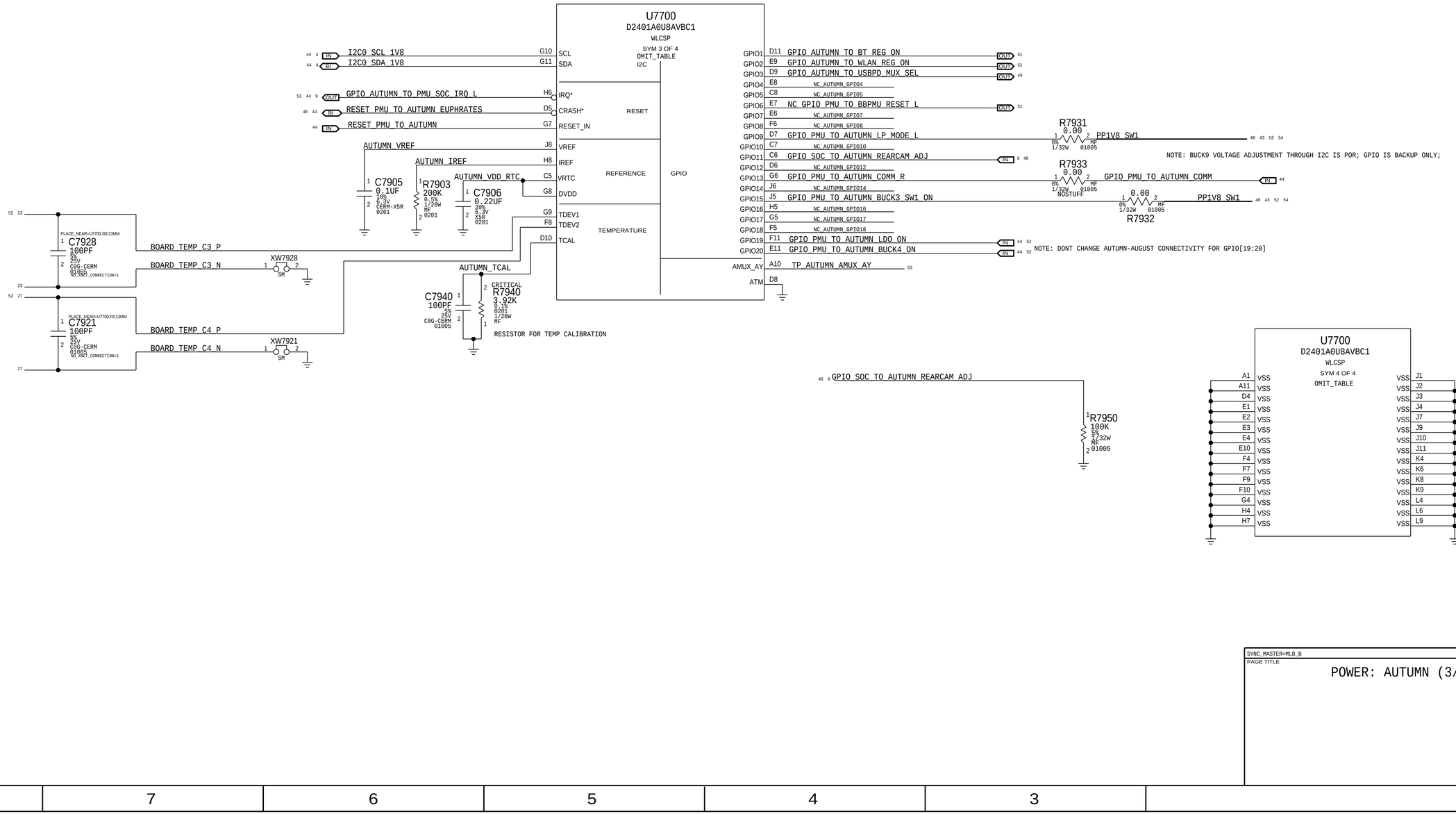


SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

POWER: AUTUMN (2/3)

AUTUMN GPIO



SYNC_MASTER=MLB_B	SYNC_DATE=07/29/2016
PAGE TITLE	
POWER: AUTUMN (3/3)	

BELLATRIX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00190	376S00119		Q8000, Q8001	

XW8000 — SM — NO_XNET_CONNECTION=1
49 PPVDD_USBPD_DET (VOLTAGE=20V)

CRITICAL
Q8001
CSD58900L
LGA
A1 S1 B1 S1 D1 S1 E1 S1 — S2 A2 S2 B2 S2 D2 S2 E2
C1 G1 — G2 C2

54 46 41 PPVBUS_PROT
41 PPVBUS_USB_RVP
EXT_PWRIN_EN1
EXT_PWRIN_EN2

CRITICAL
POWERDI3333
DMP3017SFG
Q8061
3 S S 2 S 1 — D D D D
PPVBUS_USB_EMI 30 52

CRITICAL
DZ8061
BZT52C10LP
LLP
K A
E75_RVP_G

R8061 220K 1% 1/20W MF 201
FOR CONTAMINATION RESISTANCE MEASUREMENT

R8060 499 1% 1/10W MF-LF 603

CRITICAL
Q8000
CSD58900L
LGA
A1 S1 B1 S1 D1 S1 E1 S1 — S2 A2 S2 B2 S2 D2 S2 E2
C1 G1 — G2 C2

42 PPVBUS_ORION_RVP
ACC_PWRIN_EN1
ACC_PWRIN_EN2

CRITICAL
LGA
CSD68832L
Q8051
3 S S 2 S 1 — D D D D
VOLTAGE=14.5V
PPVBUS_ORION 49

CRITICAL
DZ8051
BZT52C10LP
LLP
K A
NOTE: 10V ZENER
ORION_RVP
ORION_RVP_G

R8051 220K 2% 1/20W MF 201

54 46 41 PPVBUS_PROT
C8023 0.1UF 10% 25V X5R 0201

VOLTAGE=20V
PPVBUS_USB_RVP_R
R8020 0.00 0% 1/32W MF 01005
FROM E75_RVP_FET PPVBUS_USB_RVP 41
C8020 1.0UF 10% 35V CERM-X5R 0402

SYS_VBUS_PWR E1
EXT_PWRIN_EN1 D2
EXT_PWRIN_EN2 D1
ACC_PWRIN_EN1 E2
ACC_PWRIN_EN2 F2
EXT_VBUS_PWR C1

54 PPVCC_MAIN
54 PP1V8_S3
C8072 1UF 20% 6.3V X5R 0201
C8070 1UF 20% 10V X5R 0201

CRITICAL
U8000
CD3258A
WCSP

D3 D4 D5 D6 E3 E4 E5 E6 — VP
A4 VDD_1V8
A2 VDD_INT_1V8 (1UF TYPICAL)
PP1V8_INT_ORION
C8071 1.0UF 20% 6.3V X5R 0201-1

53 9 IN GPIO_AOP_TO_ORION_HWEN
R8070 100K 2% 1/32W MF 01005 NOSTUFF
C4 HWEN (TO BE SET TO HIGH BY DEF) 2M INT PD

52 44 6 OUT GPIO_ORION_TO_SOC_TO_PMU_IRQ
A5 INT
4 BI I2C1_SCL_1V8
C5 SCL
4 BI I2C1_SDA_1V8
B6 SDA

53 46 OUT OVP_SW_EN_L
C6 VBUS_VALID*
30 IN TS_OVP_SW_EN_L
R8071 0.00 0% 1/32W MF 01005
TS_OVP_SW_EN_R_L
C3 EXT_VBUS_VALID* 100K INT PD
NC_ORION_CONN_STATUS
B3 CONN_STATUS* (OUTPUT)
NC_ORION_GPIO1
B5 GPIO1 (I/O - HI-Z @ POR)
NC_ORION_GPIO2
B4 GPIO2

A1 GND A6 GND F1 GND

F3 F4 F5 F6 — ACC_PWR
DATA A3 ORION_COMM_FILT BI 49
GND/DFT C2
ADC_CH1 B2
ADC_CH2 B1

SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016
PAGE TITLE
ORION

AUGUST BUCKS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S00069	128S00032		C81C0,ECT	
128S00062	128S00032		C81C0,ECT	

U8100
AUGUST_PMU
WLCSP
SYM 1 OF 5
OMIT_TABLE

VCC MAIN
BUCKS

M11 IS USED TO SENSE VCC_MAIN

CRITICAL=CRITICAL

PPVCC MAIN
C81A0 C81A1 C81A2 C81A3 C81A4 10UF 20% 6.3V CERM-X5R 0402
R1 VDD_BUCK0_01_0
R2 VDD_BUCK0_01_1
R3 VDD_BUCK0_01_2
L1 VDD_BUCK0_23_0
L2 VDD_BUCK0_23_1
L3 VDD_BUCK0_23_2

PPVCC MAIN
C81B0 C81B1 C81B2 C81B3 C81B4 10UF 20% 6.3V CERM-X5R 0402
C1 VDD_BUCK1_10_0
C2 VDD_BUCK1_10_1
C3 VDD_BUCK1_10_2
G1 VDD_BUCK1_32_0
G2 VDD_BUCK1_32_1
G3 VDD_BUCK1_32_2

PPVCC MAIN
C81B8 C81B9 10UF 20% 6.3V CERM-X5R 0402
V8 VDD_BUCK2_01_0
W8 VDD_BUCK2_01_1
A9 VDD_BUCK3_0
B9 VDD_BUCK3_1

PPVCC MAIN
C81C0 C81C1 C81C2 150UF 20% 6.3V POLY-TANT CASE-B3-SM1
C81CE 220PF 5% 10V C0G-CERM 01005
C81CF 12PF 5% 25V NP0-C0G 0201
V12 VDD_BUCK6_0
W12 VDD_BUCK6_1
U13 VDD_BYP_BUCK6_0
V13 VDD_BYP_BUCK6_1
W13 VDD_BYP_BUCK6_2

C81D0 C81D1 C81D2 C81D3 C81D4 C81D5 C81D6 C81D7 10UF 20% 6.3V CERM-X5R 0402
W1 VDD_BUCK7_0
W2 VDD_BUCK7_1
W3 VDD_BUCK7_2

C81D8 C81D9 C81DA 10UF 20% 6.3V CERM-X5R 0402
A5 VDD_BUCK8_0
B5 VDD_BUCK8_1

J6 VDD_MAIN_E
E6 VDD_MAIN_N
G12 VDD_MAIN_NW
P8 VDD_MAIN_S
U16 VDD_MAIN_SW
M11 VDD_MAIN_S_ADC
E16 VDD_MAIN_W

BUCK0_LX0_0 T1 BUCK0_LX0 DIDT=TRUE SWITCH_MODE=TRUE
BUCK0_LX0_1 T2
BUCK0_LX0_2 T3
BUCK0_LX1_0 P1 BUCK0_LX1 DIDT=TRUE SWITCH_MODE=TRUE
BUCK0_LX1_1 P2
BUCK0_LX1_2 P3
BUCK0_LX2_0 M1 BUCK0_LX2 DIDT=TRUE SWITCH_MODE=TRUE
BUCK0_LX2_1 M2
BUCK0_LX2_2 M3
BUCK0_LX3_0 K1 BUCK0_LX3 DIDT=TRUE SWITCH_MODE=TRUE
BUCK0_LX3_1 K2
BUCK0_LX3_2 K3
BUCK0_FB M5 BUCK0_FB
L8100 L8101 L8102 L8103 1UH-20%-3.7A-0.044OHMS 0.22UH-20%-7.0A-0.018OHM SM PIZA20161D-SM
XW8100 PLACE_SIDE=TOP
R8100 0.00 0% 1/32W MF 01005 NOSTUFF NO_XNET_CONNECTION=1
PPVDD_CPU 42 52 54
C8100 C8101 C8102 C8103 C8104 C8105 C8106 C8107 C8108 C8109 C810A C810B C810C C810D C810E C810G C810H C810J C810K 15UF 20% 4V CERM 0402
C810F 220PF 5% 10V C0G-CERM 01005

BUCK1_LX0_0 B1 BUCK1_LX0 DIDT=TRUE SWITCH_MODE=TRUE
BUCK1_LX0_1 B2
BUCK1_LX0_2 B3
BUCK1_LX1_0 D1 BUCK1_LX1 DIDT=TRUE SWITCH_MODE=TRUE
BUCK1_LX1_1 D2
BUCK1_LX1_2 D3
BUCK1_LX2_0 F1 BUCK1_LX2 DIDT=TRUE SWITCH_MODE=TRUE
BUCK1_LX2_1 F2
BUCK1_LX2_2 F3
BUCK1_LX3_0 H1 BUCK1_LX3 DIDT=TRUE SWITCH_MODE=TRUE
BUCK1_LX3_1 H2
BUCK1_LX3_2 H3
BUCK1_FB F5 BUCK1_FB
L8110 L8111 L8112 L8113 1UH-20%-3.7A-0.044OHMS 0.22UH-20%-7.0A-0.018OHM SM PIZA20161D-SM
XW8110 PLACE_SIDE=TOP
R8110 0.00 0% 1/32W MF 01005 NOSTUFF NO_XNET_CONNECTION=1
PPVDD_GPU 42 52 54
C8110 C8111 C8112 C8113 C8114 C8115 C8116 C8117 C8118 C8119 C811A C811B C811C C811D C811E C811G C811H C811J C811K 15UF 20% 4V CERM 0402
C811F 220PF 5% 10V C0G-CERM 01005

BUCK2_LX0_0 V7 BUCK2_LX0 DIDT=TRUE SWITCH_MODE=TRUE
BUCK2_LX0_1 W7
BUCK2_LX1_0 V9 BUCK2_LX1 DIDT=TRUE SWITCH_MODE=TRUE
BUCK2_LX1_1 W9
BUCK2_FB T7 BUCK2_FB
L8120 L8121 1UH-20%-3.7A-0.044OHMS
XW8120 PLACE_SIDE=TOP
R8120 0.00 0% 1/32W MF 01005 NOSTUFF NO_XNET_CONNECTION=1
PPVDD_S1_FIXED_SOC 52 54
C8120 C8121 C8122 C8123 C8124 C8125 C8126 C8127 C8128 C8129 15UF 20% 4V CERM 0402
C812F 220PF 5% 10V C0G-CERM 01005

BUCK3_LX0_0 A8 BUCK3_LX0 DIDT=TRUE SWITCH_MODE=TRUE
BUCK3_LX0_1 B8
BUCK3_FB D7 BUCK3_FB
L8130 1UH-20%-3.7A-0.044OHMS
XW8130 SM PLACE_SIDE=TOP
PP1V8_S3 52 54
C8130 C8131 C8132 C8133 C8134 C8135 C8136 C8137 C8138 15UF 20% 4V CERM 0402
C813F 220PF 5% 10V C0G-CERM 01005

VBUCK6_BYP0 U14
VBUCK6_BYP1 V14
VBUCK6_BYP2 W14
BUCK6_LX0 V11 BUCK6_LX0 DIDT=TRUE SWITCH_MODE=TRUE
BUCK6_LX1 W11
BUCK6_FB T11 BUCK6_FB
L8160 1UH-20%-3.7A-0.044OHMS
XW8160 SM PLACE_SIDE=TOP
PP3V3_S2 52 54
C8160 C8161 C8162 C8163 C8164 C8165 C8166 C8167 C8168 C8169 C816B C816C 20UF 20% 6.3V CERM-XSR 0402
C816A 220PF 5% 10V C0G-CERM 01005

BUCK7_LX0_0 V1 BUCK7_LX0 DIDT=TRUE SWITCH_MODE=TRUE
BUCK7_LX0_1 V2
BUCK7_LX0_2 V3
BUCK7_FB V5 BUCK7_FB
L8170 1UH-20%-3.7A-0.044OHMS
XW8170 SM PLACE_SIDE=TOP
PPVDD_CPU_SRAM 52 54
C8170 C8171 C8172 C8173 C8174 15UF 20% 4V CERM 0402
C817F 220PF 5% 10V C0G-CERM 01005

BUCK8_LX0_0 A6 BUCK8_LX0 DIDT=TRUE SWITCH_MODE=TRUE
BUCK8_LX0_1 B6
BUCK8_FB D6 BUCK8_FB
L8181 1UH-20%-3.4A-0.046OHM PIZA20161D-SM
XW8180 SM PLACE_SIDE=TOP
PPVDD_GPU_SRAM 42 52 54

PPVDD_CPU 42 52 54
C810L C810M C810N C810P C810Q 15UF 20% 4V CERM 0402

PPVDD_GPU 42 52 54
C811L C811M C811N C811P C811Q 15UF 20% 4V CERM 0402

PPVDD_GPU_SRAM 42 52 54
C8180 C8181 C8182 C8183 C8184 15UF 20% 4V CERM 0402
C818F 220PF 5% 10V C0G-CERM 01005

SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016
PAGE TITLE
POWER: AUGUST (1/4)

AUGUST LDOS

U8100 AUGUST_PMU WLCSP — SYM 5 OF 5

OMIT_TABLE

A1	VSS	VSS	U8
E1	VSS	VSS	C9
J1	VSS	VSS	U9
N1	VSS	VSS	U10
U1	VSS	VSS	V10
A2	VSS	VSS	W10
E2	VSS	VSS	G11
J2	VSS	VSS	H11
N2	VSS	VSS	J11
U2	VSS	VSS	N11
A3	VSS	VSS	U11
E3	VSS	VSS	T12
J3	VSS	VSS	U12
N3	VSS	VSS	A13
U3	VSS	VSS	B13
A4	VSS	VSS	C13
B4	VSS	VSS	J13
C4	VSS	VSS	T13
D4	VSS	VSS	C14
E4	VSS	VSS	E14
F4	VSS	VSS	F14
G4	VSS	VSS	H14
H4	VSS	VSS	L14
J4	VSS	VSS	P14
K4	VSS	VSS	T14
L4	VSS	VSS	A15
M4	VSS	VSS	B15
N4	VSS	VSS	C15
P4	VSS	VSS	E15
R4	VSS	VSS	F15
T4	VSS	VSS	H15
U4	VSS	VSS	L15
V4	VSS	VSS	P15
W4	VSS	VSS	T15
C5	VSS	VSS	U15
E5	VSS	VSS	C16
J5	VSS	VSS	F16
U5	VSS	VSS	H16
W5	VSS	VSS	L16
C6	VSS	VSS	P16
G6	VSS	VSS	T16
H6	VSS	VSS	C17
K6	VSS	VSS	F17
L6	VSS	VSS	G17
U6	VSS	VSS	H17
V6	VSS	VSS	R17
W6	VSS	VSS	T17
A7	VSS	VSS	A18
B7	VSS	VSS	B18
C7	VSS	VSS	C18
U7	VSS	VSS	H18
C8	VSS		

CRITICAL=CRITICAL

LDO INPUTS

54 39 PPVCC_HIGH
54 PP1V8_S3

C8291 1UF 10% 6.3V CERM 402
C8292 1UF 10% 6.3V CERM 402

54 39 PPVCC_MAIN

54 39 PP1V8_S3

C8293 1.0UF 20% 6.3V X5R 0201-1
C8295 1.0UF 20% 6.3V X5R 0201-1

PMU_VPUMP

C8299 0.1UF 10% 6.3V CERM-X5R 0201

U8100 AUGUST_PMU WLCSP — SYM 3 OF 5

OMIT_TABLE

VDD_LDO1	U17	LDO INPUT	LDO OUTPUT
VDD_LDO2	B10		
VDD_LDO3	J17		
VDD_LDO5	P17		
VDD_LDO6	V16		
VDD_LDO6_1	V15		
VDD_LDO7	L17		
VDD_LDO8	M17		
VDD_LDO11	N17		
VDD_LDO13	K17		
VDD_LDO14	C10		
VDD_LDO16_0	V17		
VDD_LDO16_1	V18		
VBUCK3_0	B11	SWITCHED INPUT	
VBUCK3_1	B12		
VPUMP	C12		

CRITICAL=CRITICAL

SWITCHED OUTPUT

REFERENCE

V1V2_BUFF	H13	PP1V2_BUF
V1V2_BUFF_FB	G13	

C8275 0.22UF 20% 6.3V X5R 0201

LDO OUTPUTS

VLDO1	U18	(300MA; 1.2-3.68V)	PP3V0_S3_TRISTAR	52 54
VLDO2	A10	(100MA; 1.2-1.805V)	PP1V8_S2_VA_VCP	52 54
VLDO3	J18	(300MA; 1.2-3.68V)	PP3V3_S2_XBAR	52 54
VLDO5	P18	(300MA; 1.2-3.68V)	PPVDD_SPARE_LDO5	52 54
VLDO6	W15	(150MA; 2.5-3.6V)	PP3V3_ACC	52 54
VLDO6	W16			
VLDO7	L18	(300MA; 1.2-3.68V)	PP3V3	52 54
VLDO8	M18	(300MA; 1.2-3.68V)	PP3V05_S3_MESA	52 54
VLDO11	N18	(300MA; 1.2-3.68V)	PP3V0_SPARE_LDO11	52 54
VLDO13	K18	(300MA; 1.2-3.68V)	PP3V3_GRAPE	52 54
VLDO14	D10	(300MA; 0.675-1.5V)	PP1V2_SOC	52 54
VLDO16	W17			
VLDO16	W18	(300MA; 1.0-3.5V)	PP1V8_S3_MESA	52 54
ON_BUF	F13	(30MA; 1.8V)	PP1V8_ALWAYS	6 52 54
BUCK3_SW1	A12		PP1V8_SW1	40 52 54
BUCK3_SW2	A11		PP1V8_SW2_SPARE	52 54

CRITICAL C8204 20UF 20% 6.3V CERM-X5R 0402
CRITICAL C8200 10UF 20% 6.3V CERM-X5R 0402-9

CRITICAL C8208 10UF 20% 6.3V CERM-X5R 0402-9

CRITICAL C8220 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8217 10UF 20% 6.3V CERM-X5R 0402 NOSTUFF

CRITICAL C8228 10UF 20% 6.3V CERM-X5R 0402-9
CRITICAL C8224 10UF 20% 6.3V CERM-X5R 0402-9

CRITICAL C8244 10UF 20% 6.3V CERM-X5R 0402-9
CRITICAL C8240 10UF 20% 6.3V CERM-X5R 0402-9 NOSTUFF

CRITICAL C8248 4.7UF 20% 6.3V X5R 402

CRITICAL C8260 0.22UF 20% 6.3V X5R 0201
CRITICAL C8256 4.7UF 20% 6.3V X5R 402

NOSTUFF C8274 1.0UF 20% 6.3V X5R 0201-1
C8270 1UF 10% 6.3V CERM 402

CRITICAL C8275 0.22UF 20% 6.3V X5R 0201

SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

POWER: AUGUST (2/4)

AUGUST GPIO/MISC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
118S0764	118S0717		R8340	RDAR://PROBLEM/8380367
107S0150	107S0208		R8321-R8328	RDAR://PROBLEM/8380367
197S0399	197S0392		Y8300	RDAR://PROBLEM/9936684

U8100 AUGUST_PMU WLCSP

SYM_2 OF 5
OMIT_TABLE

DIG INPUT

R11	BUTTON1	GPIO_BTN_HOME_L
P9	BUTTON2	GPIO_BTN_ONOFF_L
P10	BUTTON3	NC_PMU_BTN3
P11	BUTTON4	NC_PMU_BTN4
M10	BUTTONO1	GPIO_PMU_TO_SOC_BTN_HOME_L
M9	BUTTONO2	GPIO_PMU_TO_SOC_BTN_ONOFF_L
N8	BUTTONO3	NC_PMU_BTN03

ANA INPUT

R12	BRICK_ID	USB_TS_TO_PMU_BRICKID_R
P12	ADC_IN7	ADC_IN7

REFERENCES

H12	VREF	PMU_VREF
J12	IREF	PMU_IREF
M6	VRTC_E	PMU_VDD_RTC
D12	VRTC*	
K11	DVDD	
D9	FORCE_SYNC	PMU_SYNC

32K CLK

N10	OUT_32K	CLK_PMU_TO_WLAN_32K
N9	SLEEP_32K	CLK_PMU_TO_AOP_32K

RESET

D11	PRE_UVLO	VCCMAIN_DROOP_PMU_TO_SOC_L_R
E13	SYS_ALIVE	(SYS_ALIVE)
R8	CRASH*	AUGUST_CRASH
E8	BUCK0_IPEAK*	(GPIO_PMU_TO_CPU_UV_PEAKI_L)
K5	BUCK0_SNSN	ADC_SOC_TO_PMU_VDD_CPU
L5	BUCK0_SNSP	PPVDD_BUCK0_SENSE
E10	BUCK0_UV_WARN*	(GPIO_PMU_TO_CPU_UV_WARN_L)
F6	BUCK1_IPEAK*	(GPIO_PMU_TO_GPU_UV_PEAKI_L)
H5	BUCK1_SNSN	ADC_SOC_TO_PMU_VDD_GPU (INTERNAL PD)
G5	BUCK1_SNSP	PPVDD_BUCK1_SENSE
E9	BUCK1_UV_WARN*	(GPIO_PMU_TO_GPU_UV_WARN_L)
T10	RESET_IN1	GPIO_SOC_TO_PMU_WDOG
T9	RESET_IN2	RESET_TS_TO_PMU
T8	RESET_IN3	SOCHOT1_SOC_TO_PMU_L
R9	RESET*	RESET_PMU_TO_SYSTEM_L
R10	RESET_OUT	RESET_PMU_TO_AUTUMN_R (PU IN SOC)
M8	IRQ_IN*	GPIO_AUTUMN_TO_PMU_SOC_IRQ_L (PU IN SOC)
N7	IRQ*	GPIO_PMU_TO_SOC_IRQ_L
D5	SHDWN	PMU_SHUTDOWN

I2C & SPI

E11	SLEEP1_REQ	GPIO_AOP_TO_PMU_SLEEP1_REQUEST_R
E12	SLEEP1_RDY	GPIO_PMU_TO_SYS_SLEEP1_READY
E7	ACTIVE_REQ	GPIO_AOP_TO_PMU_ACTIVE_REQUEST_R
D8	ACTIVE_RDY	GPIO_PMU_TO_SYSTEM_ACTIVE_READY
F10	SCL	I2C0_SCL_1V8
F11	SDA	I2C0_SDA_1V8
F9	MOSI	SPI_SOC_TO_PMU_DATA
F8	MISO	SPI_PMU_TO_SOC_DATA
F7	SCLK	SPI_SOC_TO_PMU_SCLK

TEMPERATURE

R13	TDEV1	PA_NTC_P
P13	TDEV2	
N13	TDEV3	
N12	TDEV4	
M13	TDEV5	
M12	TDEV6	
K13	TDEV7	
L12	TDEV8	
K12	TCAL	PMU_TCAL

CRITICAL=CRITICAL

GPIO

G10	GPIO1	GPIO_CPANEL_HALL_TO_PMU_IRQ_L
G9	GPIO2	GPIO_WLAN_TO_PMU_HOST_WAKE
G8	GPIO3	GPIO_ORION_TO_SOC_TO_PMU_IRQ
G7	GPIO4	GPIO_BELFIELD_TO_PMU_WAKE_L (USE INTERNAL PU)
H10	GPIO5	NC_GPIO_PMU_TO_BB_VBUS_DET
H9	GPIO6	UART_BATT_HDQ
H8	GPIO7	GPIO_BT_TO_PMU_HOST_WAKE
H7	GPIO8	GPIO_PMU_TO_SOC_FORCE_DFU
J10	GPIO9	NC_GPIO_BB_TO_PMU_HOST_WAKE_L
J9	GPIO10	GPIO_CODEC_TO_PMU_WAKE_L
J8	GPIO11	GPIO_APANEL_HALL_TO_PMU_IRQ_L
J7	GPIO12	GPIO_TS_TO_SOC_TO_PMU_IRQ
K10	GPIO13	GPIO_PMU_TO_AUTUMN_COMM
K9	GPIO14	GPIO_EUPHRATES_TO_PMU_WAKE
K8	GPIO15	GPIO_EUPHRATES_TO_SOC_TO_PMU_IRQ_L
K7	GPIO16	GPIO_PMU_TO_NAND_LOW_BATT_L
L7	GPIO17	GPIO_PMU_TO_1V1_EXT_SW_ON
L8	GPIO18	GPIO_PMU_TO_LCD_PWREN
L9	GPIO19	GPIO_PMU_TO_AUTUMN_LDO_ON
L10	GPIO20	GPIO_PMU_TO_AUTUMN_BUCK4_ON
C11	GPIO21	GPIO_PMU_TO_1V8_EXT_SW2_ON
F12	GPIO22	GPIO_PMU_TO_3V3_EXT_SW_ON
M7	GPIO23	GPIO_PMU_TO_EUPHRATES_LINCH_EN

ANALOG MUX

T6	AMUX_A0	ADC_SOC_TO_PMU_ANALOGMUX_OUT
R6	AMUX_A1	ADC_SOC_TO_PMU_VDD_CPU
R5	AMUX_A2	ADC_SOC_TO_PMU_VDD_GPU
T5	AMUX_A3	ADC_SOC_TO_PMU_VDD_SOC
P6	AMUX_AY	TP_AMUX_AY
R7	AMUX_B0	NC_ADC_BB_TO_PMU_SW1_VOUT
P7	AMUX_B1	NC_ADC_BB_TO_PMU_SW3_VOUT
N6	AMUX_B2	NC_ADC_BB_TO_PMU_PP_1V85
N5	AMUX_B3	NC
P5	AMUX_BY	TP_AMUX_BY

CRYSTAL

R18	XTAL1	PMU_EXTAL
T18	XTAL2	PMU_XTAL

MISC

L11	ATM	
L13	IM_MEAS	

BUTTON PULLUPS

PP1V8_ALWAYS
PP1V8_S3
R8395 100K 5% 1/32W MF 01005
R8396 100K 5% 1/32W MF 01005
GPIO_BTN_HOME_L
GPIO_BTN_ONOFF_L

DFU GPIO OTP SETTING : HI-Z OR INPUT

NOTE: DONT CHANGE AUTUMN-AUGUST CONNECTIVITY FOR GPIO[19:20]

NOTE: MAY NEED TO CHANGE XTAL CKT BASED ON CHARACTERIZATION

PLACE CAPS AND XWS NEAR PMU

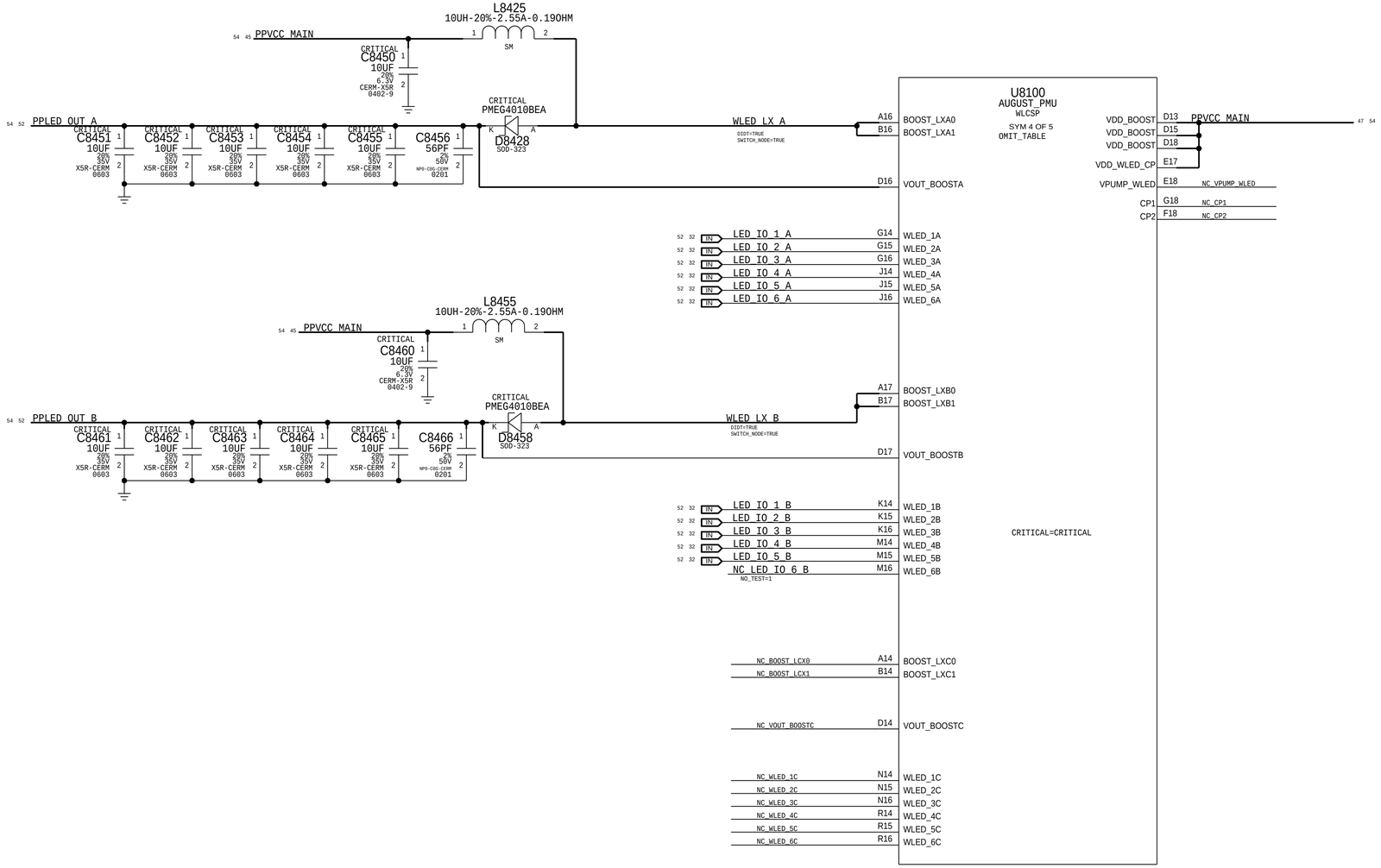
RESISTOR FOR TEMP CALIBRATION

SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2010
PAGE TITLE

POWER: AUGUST (3/4)

AUGUST BACKLIGHT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0730	371S0490		D8428,ETC	RDAR://PROBLEM/26932011



SYNC_MASTER=MLB_B	SYNC_DATE=07/29/2016
PAGE TITLE	
POWER: AUGUST (4/4)	

EUPHRATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00071	376S00073		Q8580,ECT	RDAR://PROBLEM/20277540
128S00059	128S00034		C8580,ECT	ALT FOR 47UF POLY TANT CAPS

PPVBUS_PROT 54 41

CRITICAL C8500 10UF 20% 35V X5R-CERM 0603
CRITICAL C8501 10UF 20% 35V X5R-CERM 0603
CRITICAL C8502 10UF 20% 35V X5R-CERM 0603

U8500 D2355A0 WLCSP
CRITICAL OMIT_TABLE

J11 VBUS
K11 VBUS
L11 VBUS
M11 VBUS

PPVDD_EUPHRATES_GPIO
PPVDD_EUPHRATES_CORE
PPVDD_REF_CHG

C8510 0.1UF 10% 16V X5R-CERM 0201
C8511 0.1UF 10% 16V X5R-CERM 0201
C8512 0.1UF 10% 16V X5R-CERM 0201
CRITICAL C8513 2.2UF 20% 25V X5R-CERM 0402-1
C8516 0.1UF 10% 16V X5R-CERM 0201

H11 VDD_GPIO
G11 VDDCORE
E4 VDD_REF_CHARGE_PH1
M4 VDD_REF_CHARGE_PH0
M7 VDD_REF_CHARGE

C8514 0.1UF 10% 6.3V CERM-X5R 0201

NC_EUPHRATES_ADC_IN_POS
NC_EUPHRATES_ADC_IN_NEG
EUPHRATES_ADC_REF

B11 ADC_IN_P
C11 ADC_IN_N
E11 ADC_REF

R8520 4.7K 1/32W 5% MF 01005
IN OVP_SW_EN_L 53 41
OVP_SW_EN_L_R
K9 VBUS_OVP_OFF(GPIO1)

R8521 0.00 1/32W 0% MF 01005
IN GPIO_PMU_TO_EUPHRATES_LINCH_EN 53 44
GPIO_PMU_TO_EUPHRATES_LINCH_EN_R
D11 LINCH_EN(GPIO4)

R8522 0.00 1/32W 0% MF 01005
NO_XNET_CONNECTION=1
NOSTUFF
IN SYS_ALIVE 53 46 44 17 10
BI RESET_PMU_TO_AUTUMN_EUPHRATES 44 40
M6 CRASH_L(GPIO2)
NC_EUPHRATES_BOOST_PRE_UVLO
H9 BOOST_PRE_UVLO(GPIO3)
OUT GPIO_EUPHRATES_TO_PMU_WAKE 53 46 44
D9 WAKEUP(GPIO5)
OUT USB_VBUS_DET 53 5
L6 USB_VBUS_DET(GPIO6)
NC_GPIO_EUPHRATES_TO_PMU_VSYS_HI_SW
G9 VSYS_HI_SWITCH(GPIO7)
GPIO_PMU_TO_EUPHRATES_BOOST_EN
J9 BOOST_EN(GPIO8)

R8523 0.00 1/32W 0% MF 01005
PP1V8_SW1 54 50
R8524 0.00 1/32W 0% MF 01005
NO_XNET_CONNECTION=1
NOSTUFF
SYS_ALIVE 53 46 44 17 10
OUT GPIO_EUPHRATES_TO_SOC_TO_PMU_IRQ_L 53 46 44 6
E10 IRQ*

B5 H_TEST_MODE

IN I2C0_SCL_1V8 4
L5 SCL
BI I2C0_SDA_1V8 4
M5 SDA

IN BATT_NTC 52 49
D10 TBAT

EUPHRATES_IREF
EUPHRATES_VREF
M9 IREF
M8 VREF

R8515 200K 0.5% 1/28W MF 0201
C8515 0.1UF 10% 6.3V CERM-X5R 0201

PP1V8_ALWAYS 54 44
R8525 10K 5% 1/32W MF 01005
R8526 10K 5% 1/32W MF 01005
GPIO_EUPHRATES_TO_PMU_WAKE 53 46 44
GPIO_EUPHRATES_TO_SOC_TO_PMU_IRQ_L 53 46 44 6

G10 VSSA_1
L7 VSSA_2
E6 VSSA_3

J1 VSS_PH0
J2 VSS_PH0
J3 VSS_PH0
J4 VSS_PH0
H1 VSS_PH1
H2 VSS_PH1
H3 VSS_PH1
H4 VSS_PH1

H10 VSSD_FRAME

E7 VSS_BOOST

A11 VSS_ESD
C1 VSS_ESD
C2 VSS_ESD
C3 VSS_ESD
D5 VSS_ESD
D8 VSS_ESD
E1 VSS_ESD
E5 VSS_ESD
E8 VSS_ESD
E9 VSS_ESD
F10 VSS_ESD
F11 VSS_ESD
F5 VSS_ESD
F6 VSS_ESD
F7 VSS_ESD
F8 VSS_ESD
F9 VSS_ESD
G6 VSS_ESD
G7 VSS_ESD
G8 VSS_ESD
H5 VSS_ESD
H6 VSS_ESD
H7 VSS_ESD
H8 VSS_ESD
J5 VSS_ESD
J6 VSS_ESD
J7 VSS_ESD
J8 VSS_ESD
K6 VSS_ESD
K7 VSS_ESD
K8 VSS_ESD
L8 VSS_ESD
L9 VSS_ESD
M1 VSS_ESD

NOTE: FOR NO BATTERY SITUATION
PPBATT_VCC 54 52 48
CRITICAL C8591 10UF 20% 6.3V CERM-X5R 0402-9
CRITICAL C8592 10UF 20% 6.3V CERM-X5R 0402-9
PPBATT_POS_RC 52
R8591 0.5 1% 1/10W MF 402

VCENTER_3 J10
VCENTER_3 K10
VCENTER_3 L10
VCENTER_3 M10
VCENTER_0 L4
VCENTER_0 L1
VCENTER_0 L2
VCENTER_0 L3
VCENTER_1 F1
VCENTER_1 F2
VCENTER_1 F3
VCENTER_1 F4

PPVCENTER 52
CRITICAL C8550 10UF 20% 35V X5R-CERM 0603
CRITICAL C8551 10UF 20% 35V X5R-CERM 0603
CRITICAL C8552 10UF 20% 35V X5R-CERM 0603

CRITICAL C8555 0.1UF 10% 50V X5R-CERM 0402
CRITICAL C8556 0.1UF 10% 50V X5R-CERM 0402
CRITICAL C8557 0.1UF 10% 50V X5R-CERM 0402

VBOOT_DRV0 M2
VBOOT_N0 M3
EUPTES_VBOOT0
CRITICAL C8560 0.1UF 10% 50V X5R-CERM 0402
LX_BOOT_PH0 K5
EUPHRATES_VBOOT_PH0

VBOOT_DRV1 E2
VBOOT_N1 E3
EUPHRATES_VBOOT1
CRITICAL C8561 0.1UF 10% 50V X5R-CERM 0402
LX_BOOT_PH1 G5
EUPHRATES_VBOOT_PH1

LX_PH0 K1
LX_PH0 K2
LX_PH0 K3
LX_PH0 K4
LX_PH1 G1
LX_PH1 G2
LX_PH1 G3
LX_PH1 G4 46
EUPHRATES_LX0
EUPHRATES_LX1

CRITICAL L8570 1.5UH-20%-5.5A-0.03220HM PIHA051D-SM
CRITICAL L8571 1.5UH-20%-5.5A-0.03220HM PIHA051D-SM

CRITICAL D8500 SOD-123W PMEG4030ER
CRITICAL D8501 SOD-123W PMEG4030ER

PPVCC_MAIN 45 52 54
CRITICAL C8570 10UF 20% 16V X5R-CERM 0402-7
CRITICAL C8571 10UF 20% 16V X5R-CERM 0402-7
CRITICAL C8572 10UF 20% 16V X5R-CERM 0402-7
CRITICAL C8573 10UF 20% 16V X5R-CERM 0402-7
CRITICAL C8574 10UF 20% 16V X5R-CERM 0402-7

VSYS_LO_1 A9
VSYS_LO_1 B9
VSYS_LO_1 C9
VSYS_LO_2 A8
VSYS_LO_2 B8
VSYS_LO_2 C8
VSYS_LO_S D7

LX_BOOST D1
LX_BOOST D2
LX_BOOST D3
LX_BOOST D4
EUPHRATES_LX1 46

BOOST_HS_SUPPLY C5
EUPHRATES_HS_SPLY
CRITICAL C8562 1.0UF 20% 16V X5R-CERM 0201-1
BOOST_HS_SOURCE C4
EUPHRATES_HS_SRC
VSYS_HI_S A5

PPVCC_HIGH 52 54
CRITICAL C8580 47UF 20% 11V TANT-POLY CASE-A3-LLP
CRITICAL C8588 47UF 20% 11V TANT-POLY CASE-A3-LLP
CRITICAL C8589 47UF 20% 11V TANT-POLY CASE-A3-LLP
CRITICAL C8581 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8582 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8583 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8584 1.0UF 20% 6.3V X5R 0201-1

VSYS_HI B1
VSYS_HI B2
VSYS_HI B3
VSYS_HI B4
EUPHRATES_HIGH_DIO
NOSTUFF R8581 470K 5% 1/32W MF 01005
CRITICAL Q8581 FDMC6683-P MLP3.3X3.3
VSYS_HI_EXT_DIO C6

VSYS_LO_BYPASS A1
VSYS_LO_BYPASS A2
VSYS_LO_BYPASS A3
VSYS_LO_BYPASS A4
CHICKEN BIT IF EUPHRATES DOES NOT WORK
BAT IT WILL WORK... R10477 =1
PPVCC_MAIN 46 52 54

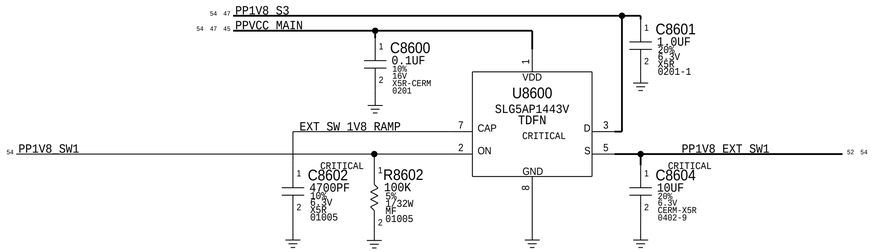
VSYS_LO_EXT_DIO D6
EUPHRATES_LOW_DIO
NOSTUFF R8580 470K 5% 1/32W MF 01005
CRITICAL Q8580 FDMC6686P POWER33

IBAT_1 A10
IBAT_1 B10
IBAT_1 C10
IBAT_2 A7
IBAT_2 B7
IBAT_2 C7
CHICKEN BIT IF EUPHRATES DOES NOT WORK
BAT IT WILL WORK... R10477 =1

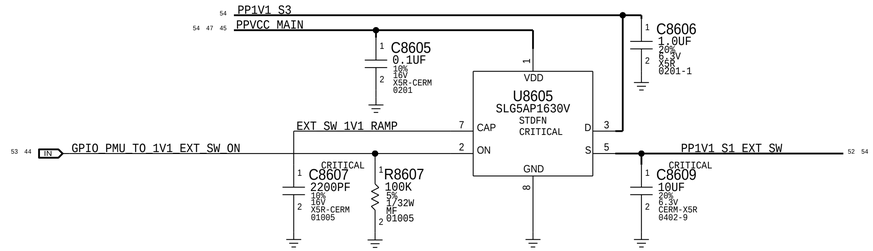
IBAT_S A6
VBAT B6
PPBATT_VCC 46 52 54
R8593 499 1% 1/20W MF 201
CRITICAL C8590 10UF 20% 16V X5R-CERM 0402-7
PLACE_NEAR=U8500,A7:3MM
BATT_SNS_R
R8592 0.00 0% 1/32W MF 01005
BATT_SNS IN 49 52

SYNC_MASTER=MLB_B
SYNC_DATE=07/29/2016
PAGE TITLE
POWER: CHARGER

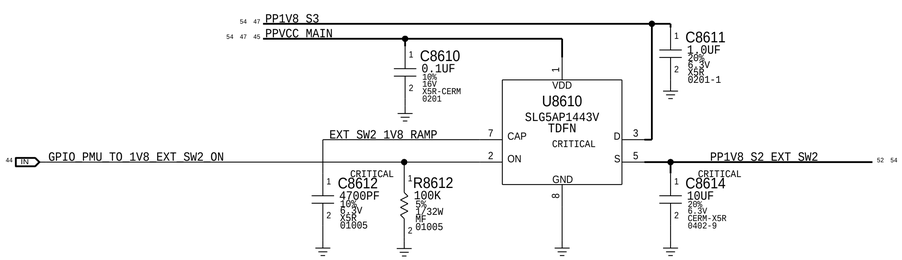
1.8V EXTERNAL SWITCH 1



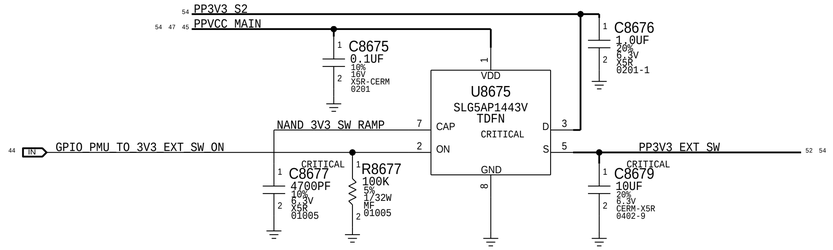
DDR 1.1V SWITCH



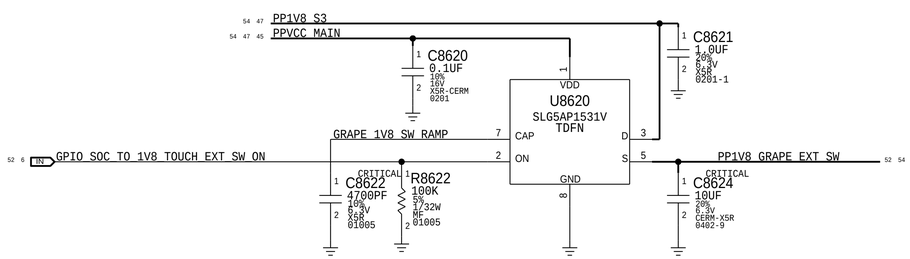
1.8V EXTERNAL SWITCH 2



NAND 3.3V SWITCH



GRAPE 1.8V SWITCH

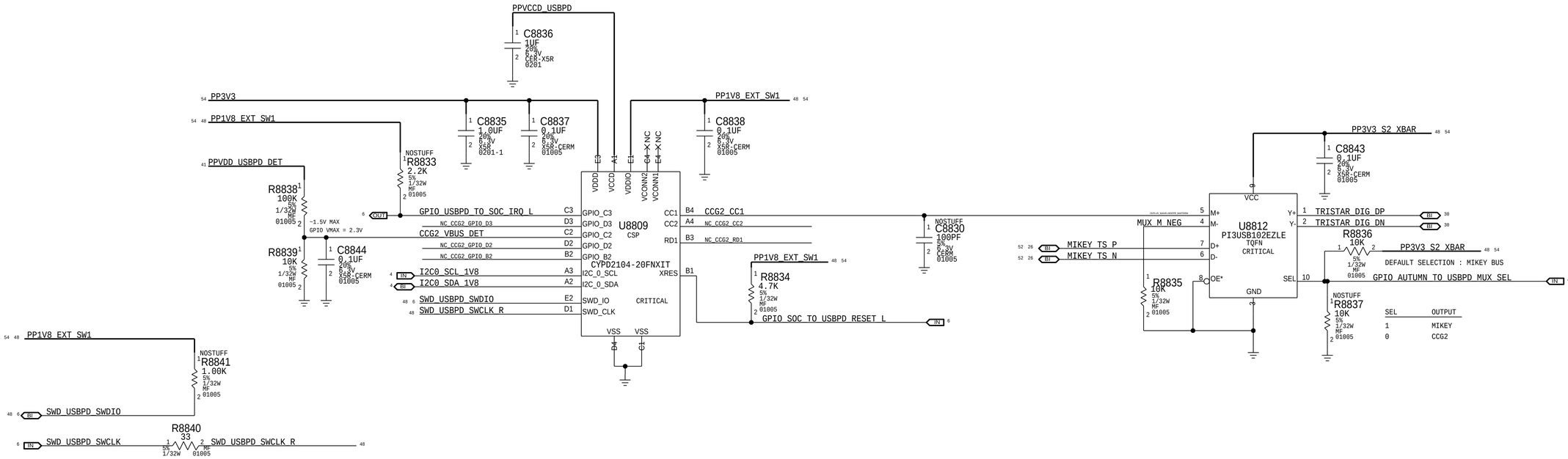


SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

POWER: EXTERNAL SWITCHES & LDOS

USBPD

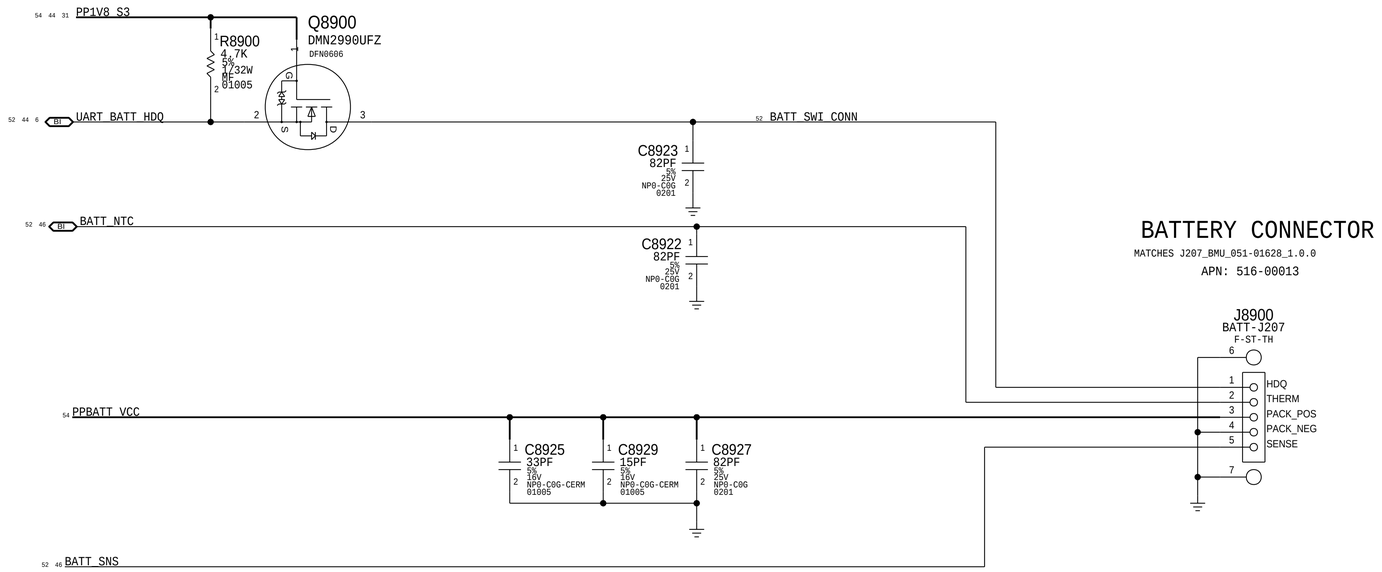


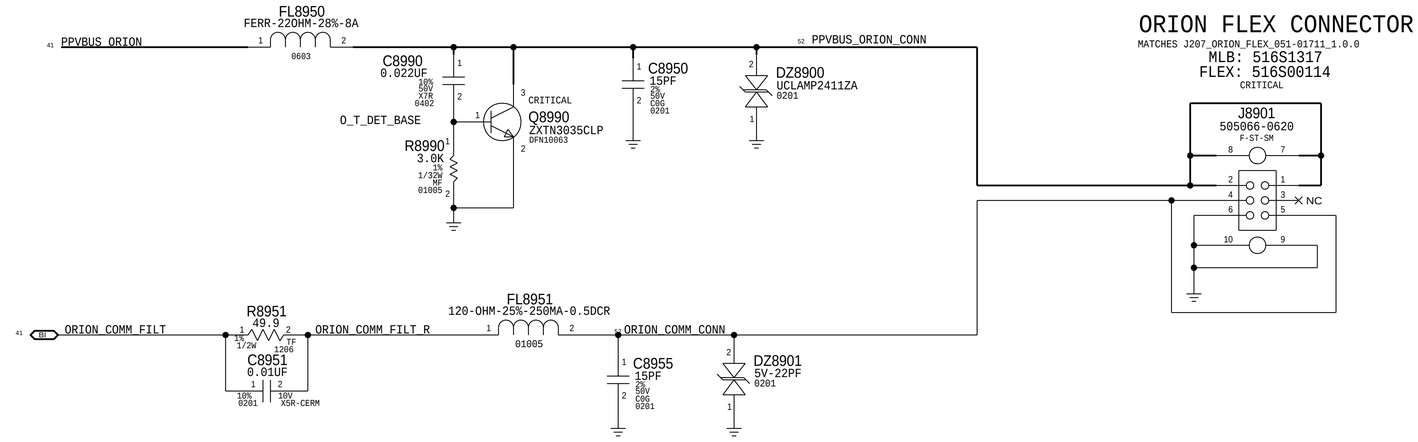
SYNC_MASTER=MLB_B

SYNC_DATE=07/29/2016

PAGE TITLE

POWER: USB PD



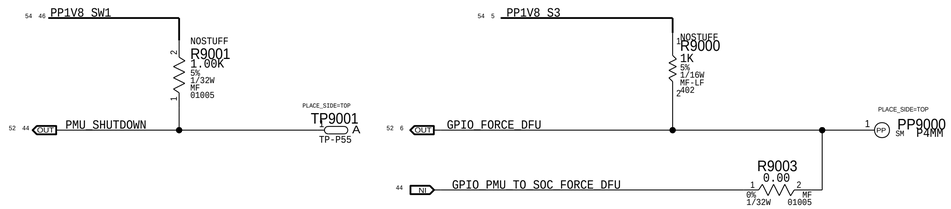


SYNC_MASTER=MLB_B SYNC_DATE=07/29/2016

PAGE TITLE

POWER: BATTERY & ORION CONN

DEBUG RESET ACCESS



SYNC_MASTER=MLB_B SYNC_DATE=08/26/2016

PAGE TITLE

SOC: DEBUG

CELLULAR AND WLAN/BT ALIASES

BASEBAND

SOC GPIOS

6	IN	NC_GPIO_SOC_TO_BB_RADIO_ON_L	NC_GPIO_SOC_TO_BB_RADIO_ON_L	MAKE_BASE=TRUE	
6	IN	NC_GPIO_SOC_TO_BB_RESET_L	NC_GPIO_SOC_TO_BB_RESET_L	MAKE_BASE=TRUE	
6	OUT	NC_GPIO_BB_TO_SOC_RESET_DET_L	NC_GPIO_BB_TO_SOC_RESET_DET_L	MAKE_BASE=TRUE	
6	IN	NC_GPIO_SOC_TO_BB_COREDUMP	NC_GPIO_SOC_TO_BB_COREDUMP	MAKE_BASE=TRUE	
7	IN	NC_GPIO_SOC_TO_BB_MESA_ON	NC_GPIO_SOC_TO_BB_MESA_ON	MAKE_BASE=TRUE	
9	BI	NC_SWD_BB_SWDIO	NC_SWD_BB_SWDIO	MAKE_BASE=TRUE	
40	IN	NC_GPIO_PMU_TO_BBPMU_RESET_L	NC_GPIO_PMU_TO_BBPMU_RESET_L	MAKE_BASE=TRUE	
44	IN	NC_GPIO_PMU_TO_BB_VBUS_DET	NC_GPIO_PMU_TO_BB_VBUS_DET	MAKE_BASE=TRUE	
44	OUT	NC_GPIO_BB_TO_PMU_HOST_WAKE_L	NC_GPIO_BB_TO_PMU_HOST_WAKE_L	MAKE_BASE=TRUE	
9	IN	NC_UART_AOP_TO_BB_TX	NC_UART_AOP_TO_BB_TX	MAKE_BASE=TRUE	
9	OUT	NC_UART_BB_TO_AOP_TX	NC_UART_BB_TO_AOP_TX	MAKE_BASE=TRUE	
6	OUT	NC_GPIO_BB_TO_SOC_GPS_SYNC	NC_GPIO_BB_TO_SOC_GPS_SYNC	MAKE_BASE=TRUE	
6	BI	NC_GPIO_BB_IPC	NC_GPIO_BB_IPC	MAKE_BASE=TRUE	
25	OUT	NC_GPIO_BB_TO_STROBE_GSM_BURST_IND	NC_GPIO_BB_TO_STROBE_GSM_BURST_IND	MAKE_BASE=TRUE	

PCIE

8	IN	NC_PCIE_SOC_TO_BB_REFCLK_P	NC_PCIE_SOC_TO_BB_REFCLK_P	MAKE_BASE=TRUE	
8	IN	NC_PCIE_SOC_TO_BB_REFCLK_N	NC_PCIE_SOC_TO_BB_REFCLK_N	MAKE_BASE=TRUE	
8	OUT	NC_PCIE_BB_TO_SOC_CLKREQ_L	NC_PCIE_BB_TO_SOC_CLKREQ_L	MAKE_BASE=TRUE	
8	IN	NC_PCIE_SOC_TO_BB_RESET_L	NC_PCIE_SOC_TO_BB_RESET_L	MAKE_BASE=TRUE	
8	OUT	NC_PCIE_SOC_TO_BB_TX_C_P	NC_PCIE_SOC_TO_BB_TX_C_P	MAKE_BASE=TRUE	
8	OUT	NC_PCIE_SOC_TO_BB_TX_C_N	NC_PCIE_SOC_TO_BB_TX_C_N	MAKE_BASE=TRUE	
8	OUT	NC_PCIE_BB_TO_SOC_TX_P	NC_PCIE_BB_TO_SOC_TX_P	MAKE_BASE=TRUE	
8	OUT	NC_PCIE_BB_TO_SOC_TX_N	NC_PCIE_BB_TO_SOC_TX_N	MAKE_BASE=TRUE	

USB

30	BI	NC_USB_BB_P	NC_USB_BB_P	MAKE_BASE=TRUE	
30	BI	NC_USB_BB_N	NC_USB_BB_N	MAKE_BASE=TRUE	

PMU ADC

44	OUT	NC_ADC_BB_TO_PMU_PP_1V85	NC_ADC_BB_TO_PMU_PP_1V85	MAKE_BASE=TRUE	
44	OUT	NC_ADC_BB_TO_PMU_SW1_VOUT	NC_ADC_BB_TO_PMU_SW1_VOUT	MAKE_BASE=TRUE	
44	OUT	NC_ADC_BB_TO_PMU_SW3_VOUT	NC_ADC_BB_TO_PMU_SW3_VOUT	MAKE_BASE=TRUE	

WLAN

POWER

54		PP3V3_S2	PP3V3_S2		35
54		PP1V8_S2_EXT_SW2	PP1V8_S2_EXT_SW2		35

GPIOS

40	IN	GPIO_AUTUMN_TO_WLAN_REG_ON	MAKE_BASE=TRUE	GPIO_AUTUMN_TO_WLAN_REG_ON	OUT	35	52
44	OUT	GPIO_WLAN_TO_PMU_HOST_WAKE	MAKE_BASE=TRUE	GPIO_WLAN_TO_PMU_HOST_WAKE	IN	35	52
53 6	IN	GPIO_SOC_TO_WLAN_DEVICE_WAKE	MAKE_BASE=TRUE	GPIO_SOC_TO_WLAN_DEVICE_WAKE	OUT	35	
44	IN	CLK_PMU_TO_WLAN_32K	MAKE_BASE=TRUE	CLK_PMU_TO_WLAN_32K	OUT	35	52
35		NC_UART_BB2WLAN_COEX_TX	MAKE_BASE=TRUE	NC_UART_BB2WLAN_COEX_TX	MAKE_BASE=TRUE		
35		NC_UART_WLAN2BB_COEX_TX	MAKE_BASE=TRUE	NC_UART_WLAN2BB_COEX_TX	MAKE_BASE=TRUE		
52 9	IN	GPIO_AOP_TO_WLAN_CONTEXT_A	MAKE_BASE=TRUE	GPIO_AOP_TO_WLAN_CONTEXT_A	OUT	35	
52 9	IN	GPIO_AOP_TO_WLAN_CONTEXT_B	MAKE_BASE=TRUE	GPIO_AOP_TO_WLAN_CONTEXT_B	OUT	35	

UART

53 6	IN	UART_SOC_TO_WLAN_TX	MAKE_BASE=TRUE	UART_SOC_TO_WLAN_TX	OUT	35	
53 6	IN	UART_SOC_TO_WLAN_RTS_L	MAKE_BASE=TRUE	UART_SOC_TO_WLAN_RTS_L	OUT	35	
53 6	OUT	UART_WLAN_TO_SOC_TX	MAKE_BASE=TRUE	UART_WLAN_TO_SOC_TX	IN	35	
53 6	OUT	UART_WLAN_TO_SOC_RTS_L	MAKE_BASE=TRUE	UART_WLAN_TO_SOC_RTS_L	IN	35	

CHYUS_WAS=SINGLE_NODENET
FUNC_TEST=TRUE

52		TESTPOINT_JTAG_WLAN_TCK	MAKE_BASE=TRUE	TESTPOINT_JTAG_WLAN_TCK	35
52		TP_JTAG_WLAN_TMS	MAKE_BASE=TRUE	TP_JTAG_WLAN_TMS	35
52 51		GPIO_WLAN_TO_SOC_ATSP	MAKE_BASE=TRUE	GPIO_WLAN_TO_SOC_ATSP	35

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0.00
0% 1/32W MF 01005

6	OUT	GPIO_WLAN_TO_SOC_ATSP_R	2	1 GPIO_WLAN_TO_SOC_ATSP	51 52

PCIE

53 8	IN	PCIE_SOC_TO_WLAN_REFCLK_P	MAKE_BASE=TRUE	PCIE_SOC_TO_WLAN_REFCLK_P	OUT	35	
53 8	IN	PCIE_SOC_TO_WLAN_REFCLK_N	MAKE_BASE=TRUE	PCIE_SOC_TO_WLAN_REFCLK_N	OUT	35	
8	IN	PCIE_SOC_TO_WLAN_TX_P	MAKE_BASE=TRUE	PCIE_SOC_TO_WLAN_TX_P	OUT	35	53
8	IN	PCIE_SOC_TO_WLAN_TX_N	MAKE_BASE=TRUE	PCIE_SOC_TO_WLAN_TX_N	OUT	35	53
51		PCIE_WLAN_TO_SOC_TX_C_P	MAKE_BASE=TRUE	PCIE_WLAN_TO_SOC_TX_C_P	IN	35	
51		PCIE_WLAN_TO_SOC_TX_C_N	MAKE_BASE=TRUE	PCIE_WLAN_TO_SOC_TX_C_N	IN	35	
53 8	OUT	PCIE_WLAN_TO_SOC_CLKREQ_L	MAKE_BASE=TRUE	PCIE_WLAN_TO_SOC_CLKREQ_L	IN	35	
53 8	IN	PCIE_SOC_TO_WLAN_RESET_L	MAKE_BASE=TRUE	PCIE_SOC_TO_WLAN_RESET_L	OUT	35	

BLUETOOTH

SOC GPIOS

44	OUT	GPIO_BT_TO_PMU_HOST_WAKE	MAKE_BASE=TRUE	GPIO_BT_TO_PMU_HOST_WAKE	IN	35	52
40	IN	GPIO_AUTUMN_TO_BT_REG_ON	MAKE_BASE=TRUE	GPIO_AUTUMN_TO_BT_REG_ON	OUT	35	52
9	IN	GPIO_SOC_TO_BT_WAKE	MAKE_BASE=TRUE	GPIO_SOC_TO_BT_WAKE	OUT	35	53

UART

6	IN	UART_SOC_TO_BT_TX	MAKE_BASE=TRUE	UART_SOC_TO_BT_TX	OUT	35	53
6	IN	UART_SOC_TO_BT_RTS_L	MAKE_BASE=TRUE	UART_SOC_TO_BT_RTS_L	OUT	35	53
53 6	OUT	UART_BT_TO_SOC_TX	MAKE_BASE=TRUE	UART_BT_TO_SOC_TX	IN	35	
53 6	OUT	UART_BT_TO_SOC_RTS_L	MAKE_BASE=TRUE	UART_BT_TO_SOC_RTS_L	IN	35	

53 20 19 6	IN	GPIO_SOC_TO_BT_TO_GRAPE_TS_SYNC	MAKE_BASE=TRUE	GPIO_SOC_TO_BT_TO_GRAPE_TS_SYNC	OUT	35	
53 19	IN	GPIO_TOUCH_TO_BT_SYNC	MAKE_BASE=TRUE	GPIO_TOUCH_TO_BT_SYNC	OUT	35	

ROTTERDAM

POWER

54	PP3V0_S3_TRISTAR		PP3V0_S3_TRISTAR	37
54	PP1V8_S2_EXT_SW2		PP1V8_S2_EXT_SW2	37

SOC GPIOS

6	IN	GPIO_SOC_TO_ROTTERDAM_DEV_WAKE	MAKE_BASE=TRUE	GPIO_SOC_TO_ROTTERDAM_DEV_WAKE	OUT	37	
6	IN	GPIO_SOC_TO_ROTTERDAM_DWLD_REQ	MAKE_BASE=TRUE	GPIO_SOC_TO_ROTTERDAM_DWLD_REQ	OUT	37	
6	IN	GPIO_SOC_TO_ROTTERDAM_EN	MAKE_BASE=TRUE	GPIO_SOC_TO_ROTTERDAM_EN	OUT	37	

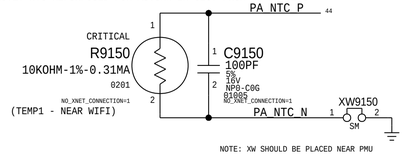
UART

6	IN	UART_SOC_TO_ROTTERDAM_TX	MAKE_BASE=TRUE	UART_SOC_TO_ROTTERDAM_TX	OUT	37	
6	OUT	UART_ROTTERDAM_TO_SOC_TX	MAKE_BASE=TRUE	UART_ROTTERDAM_TO_SOC_TX	IN	37	
6	IN	UART_SOC_TO_ROTTERDAM_RTS_L	MAKE_BASE=TRUE	UART_SOC_TO_ROTTERDAM_RTS_L	OUT	37	
6	OUT	UART_ROTTERDAM_TO_SOC_RTS_L	MAKE_BASE=TRUE	UART_ROTTERDAM_TO_SOC_RTS_L	IN	37	

53 8	PCIE_WLAN_TO_SOC_TX_P	C9160 1 (GND_VOID=TRUE)	2 (GND_VOID=TRUE) 0.1UF	PCIE_WLAN_TO_SOC_TX_C_P	51
		20% X5R 01005 6.3V			
53 8	PCIE_WLAN_TO_SOC_TX_N	C9161 1 (GND_VOID=TRUE)	2 (GND_VOID=TRUE) 0.1UF	PCIE_WLAN_TO_SOC_TX_C_N	51
		20% X5R 01005 6.3V			

AUTUMN NTC

NOTE: NTC REPURPOSED FOR AUTUMN IN J207 FROM BB IN J208



NOTE: XW SHOULD BE PLACED NEAR PMU

SYNC_MASTER=MLB_A_ELBA
SYNC_DATE=04/24/2016
PAGE TITLE:
ALIASES: BB/WLAN/BT

SMT TEST FIXTURE TP

POWER - BUCKS

TP9301	A	1	PPVDD_CPU	42 54
TP9302	A	1	PPVDD_GPU	42 54
TP9303	A	1	PPVDD_S1_FIXED_SOC	42 54
TP9304	A	1	PP1V8_S3	42 54
TP9305	A	1	PP1V8_SW1	40 43 54
TP9306	A	1	PP1V8_EXT_SW1	47 54
TP9307	A	1	PP1V8_SW1_CAM	39 54
TP9308	A	1	PP1V8_S2_EXT_SW2	47 54
TP9309	A	1	PP1V8_SW2_SPARE	43 54
TP9310	A	1	PP1V8_S3_SW3	39 54
TP9311	A	1	PP1V1_S3	38 54
TP9312	A	1	PP1V1_SW1_SPARE	39 54
TP9314	A	1	PP1V1_S1_EXT_SW	47 54
TP9316	A	1	PP3V3_S2	42 54
TP9318	A	1	PP3V3_EXT_SW	47 54
TP9319	A	1	PPVDD_CPU_SRAM	42 54
TP9320	A	1	PPVDD_GPU_SRAM	42 54
TP9321	A	1	PP1V8_GRAPE_EXT_SW	47 54
TP9384	A	1	PP2V9_PVDD_CAM_REAR	38 54
TP9385	A	1	PP1V5_CAMERA	38 54

POWER - LDOS

TP9322	A	1	PP3V0_S3_TRISTAR	43 54
TP9323	A	1	PP1V8_S2_VA_VCP	43 54
TP9324	A	1	PP3V3_S2_XBAR	43 54
TP9325	A	1	PP3V0_ALS	39 54
TP9326	A	1	PPVDD_SPARE_LDO5	43 54
TP9327	A	1	PP3V3_ACC	43 54
TP9328	A	1	PP3V3	43 54
TP9329	A	1	PP3V05_S3_MESA	43 54
TP9330	A	1	PP1V19_FRONT_CAM	39 54
TP9331	A	1	PP0V9_NAND	39 54
TP9332	A	1	PP3V0_SPARE_LDO11	43 54
TP9333	A	1	PP3V0_UT_SVDD	39 54
TP9334	A	1	PP1V2_SOC	43 54
TP9335	A	1	PP0V775_S3_SOC_AOP	39 54
TP9336	A	1	PP1V8_S3_MESA	43 54
TP9386	A	1	PP3V3_GRAPE	43 54
TP9387	A	1	PP1V8_HAWKING	39 54
TP9388	A	1	PPVDD_SPARE_LDO22	39 54

POWER - OTHER

TP9340	A	1	PPVCENTER	46
TP9341	A	1	PPVBUS_PROT	54
TP9342	A	1	PPVCC_HIGH	46 54
TP9343	A	1	PP1V8_ALWAYS	6 43 54
TP9344	A	1	PPBATT_VCC	46 52 54
TP9345	A	1	PPLED_OUT_A	45 54
TP9346	A	1	PPLED_OUT_B	45 54
TP9347	A	1	PPVCC_MAIN	46 54
TP9348	A	1	PPBATT_POS_RC	46
TP9349	A	1	PPVBUS_USB_EMI	30 41 52
TP934A	A	1	PP16V0_MESA	34

POWER - CAMERA (NH)

TP9350	A	1	PP1V19_CAM_FRONT_CONN	24
TP9351	A	1	PP1V8_CAM_FRONT_CONN	24
TP9352	A	1	PP2V9_AVDD_CAM_FRONT_CONN	24

POWER - CAMERA (UT)

TP9353	A	1	PP1V19_CAM_REAR_CONN	23
TP9354	A	1	PP1V8_CAM_REAR_CONN	23
TP9355	A	1	PP2V85_AVDD_CAM_REAR_CONN	23
TP9356	A	1	PP3V0_UT_SVDD_CONN	23
TP9357	A	1	PP2V9_PVDD_CAM_REAR_CONN	23

POWER - DISPLAY

TP9360	A	1	PPVCC_MAIN_LCD_SW_CONN	32 33
TP9361	A	1	PPVCC_MAIN_LCD_SW	33

POWER - BACKLIGHT

TP9362	A	1	PPLED_BACK_REG_A	32 33
TP9363	A	1	LED_IO_1_A	32 45
TP9364	A	1	LED_IO_2_A	32 45
TP9365	A	1	LED_IO_3_A	32 45
TP9366	A	1	LED_IO_4_A	32 45
TP9367	A	1	LED_IO_5_A	32 45
TP9374	A	1	LED_IO_6_A	32 45
TP9368	A	1	PPLED_BACK_REG_B	32 33
TP9369	A	1	LED_IO_1_B	32 45
TP9370	A	1	LED_IO_2_B	32 45
TP9371	A	1	LED_IO_3_B	32 45
TP9372	A	1	LED_IO_4_B	32 45
TP9373	A	1	LED_IO_5_B	32 45

BATTERY

TP9380	A	1	BATT_SWI_CONN	49
TP9381	A	1	BATT_NTC	46 49
TP9382	A	1	BATT_SNS	46 49
TP9383	A	1	UART_BATT_HDQ	6 44 49

TRISTAR

TP938A	A	1	GPIO_TS_TO_SOC_TO_PMU_IRQ	6 30 44
TP938B	A	1	RESET_TS_TO_PMU	30 44

TP9390 A 1 TP-1P0-TOP (PLACE_NEAR=J3700.19:20MM)
TP9391 A 1 TP-1P0-TOP (PLACE_NEAR=J3700.19:20MM)
TP9392 A 1 TP-1P0-TOP (PLACE_NEAR=J3700.19:20MM) — PPVBUS_E75_USB_CONN 30 31 52
TP9393 A 1 TP-1P0-TOP (PLACE_NEAR=J3700.9:30MM)
TP9394 A 1 TP-1P0-TOP (PLACE_NEAR=J3700.9:30MM)
TP9395 A 1 TP-1P0-TOP (PLACE_NEAR=J3700.9:30MM)

TP9396 A 1 TP-1P0-TOP (PLACE_NEAR=J8900.4:15MM)
TP9397 A 1 TP-1P0-TOP (PLACE_NEAR=J8900.4:15MM)
TP9398 A 1 TP-1P0-TOP (PLACE_NEAR=J8900.4:15MM)

TP9399 A 1 TP-1P0-TOP (PLACE_NEAR=J8900.3:15MM)
TP939A A 1 TP-1P0-TOP (PLACE_NEAR=J8900.3:15MM)
TP939B A 1 TP-1P0-TOP (PLACE_NEAR=J8900.3:15MM) — PPBATT_VCC 46 52 54

PMU

TP93A0	A	1	GPIO_WLAN_TO_PMU_HOST_WAKE	35 51
TP93A1	A	1	GPIO_BT_TO_PMU_HOST_WAKE	35 51
TP93A3	A	1	PMU_TCAL	44
TP93A5	A	1	BOARD_TEMP2_P	44
TP93A6	A	1	BOARD_TEMP3_P	44
TP93A7	A	1	BOARD_TEMP4_P	44
TP93A8	A	1	BOARD_TEMP5_P	44
TP93A9	A	1	BOARD_TEMP6_P	44
TP93AA	A	1	BOARD_TEMP7_P	44
TP93B1	A	1	BOARD_TEMP8_P	44
TP93B3	A	1	TP_AUTUMN_AMUX_AY	40
TP93B4	A	1	TP_AMUX_AY	44
TP93B5	A	1	TP_AMUX_BY	44
TP93B6	A	1	SPI_SOC_TO_PMU_DATA	9 44
TP93B7	A	1	SPI_PMU_TO_SOC_DATA	9 44
TP93B8	A	1	SPI_SOC_TO_PMU_SCLK	9 44
TP93B9	A	1	GPIO_PMU_TO_CPU_TRIGGER_0	6 44
TP93BA	A	1	GPIO_PMU_TO_CPU_TRIGGER_1	6 44
TP93BB	A	1	VCCMAIN_DROOP_PMU_TO_SOC_L	6 44
TP93BC	A	1	SOCHOT1_SOC_TO_PMU_L	6 44
TP93BD	A	1	PMU_SHUTDOWN	44 50
TP93BE	A	1	GPIO_PMU_TO_GPU_TRIGGER_0	6 44
TP93BF	A	1	GPIO_PMU_TO_GPU_TRIGGER_1	6 44
TP93BG	A	1	BOARD_TEMP_C3_P	23 40
TP93BH	A	1	BOARD_TEMP_C4_P	27 40
TP93BI	A	1	GPIO_PMU_TO_SOC_BTN_HOME_L	9 44
TP93BJ	A	1	GPIO_PMU_TO_SOC_BTN_ONOFF_L	9 44
TP93BK	A	1	GPIO_PMU_TO_AUTUMN_LDO_ON	40 44
TP93BL	A	1	GPIO_PMU_TO_AUTUMN_BUCK4_ON	40 44

SOC - JTAG/RESET

TP93C1	A	1	JTAG_SOC_SEL	4 5
TP93C2	A	1	JTAG_SOC_TCK	5 30
TP93C3	A	1	JTAG_SOC_TMS	5 30
TP93C4	A	1	TP_JTAG_SOC_TDI	5
TP93C5	A	1	TP_JTAG_SOC_TRST_L	4 5
TP93C6	A	1	TP_JTAG_SOC_TDO	5
TP93C7	A	1	SOC_TESTMODE	4 5
TP93C8	A	1	RESET_PMU_TO_SYSTEM_L	4 5 9 44 53
TP93C9	A	1	GPIO_FORCE_DFU	6 50

SOC - UART

TP93D0	A	1	UART_SOC_TO_DEBUG_TX	6 30
TP93D1	A	1	UART_DEBUG_TO_SOC_TX	6 30

SOC - USB

TP93D2	A	1	USB_SOC_N	5 30
TP93D3	A	1	USB_SOC_P	5 30

E75

TP93D4	A	1	E75_ACC_DET_CONN_L	30 31
TP93D5	A	1	PPVBUS_E75_USB_CONN	30 31 52
TP93D6	A	1	PPOUT_E75_ACC_ID1_CONN	30 31
TP93D7	A	1	PPOUT_E75_ACC_ID2_CONN	30 31
TP93D8	A	1	E75_DPAIR1_N	30 31
TP93D9	A	1	E75_DPAIR1_P	30 31
TP93E0	A	1	E75_DPAIR2_N	30 31
TP93E1	A	1	E75_DPAIR2_P	30 31
TP93EB	A	1	PPVBUS_USB_EMI	30 41 52

ORION

TP93E2	A	1	PPVBUS_ORION_RVP	41
TP93E3	A	1	PPVBUS_ORION_CONN	49 52
TP93E9	A	1	ORION_COMM_CONN	49
TP93EA	A	1	GPIO_ORION_TO_SOC_TO_PMU_IRQ	6 41 44

AUDIO - HEADPHONE

TP93E5	A	1	CODEC_HP_HEADSET_DET_CONN	26 27
TP93E6	A	1	CODEC_HP_HS3_CONN	26 27
TP93E7	A	1	CODEC_HP_HS3_REF_CONN	26 27
TP93E8	A	1	CODEC_HP_HS4_CONN	26 27
TP93E9	A	1	CODEC_HP_HS4_REF_CONN	26 27
TP93FO	A	1	CODEC_HP_LEFT_CONN	26 27
TP93F1	A	1	CODEC_HP_RIGHT_CONN	26 27

AUDIO - SPEAKER AMPS

TP93F2	A	1	PPVBOOST_R_CN	28
TP93F3	A	1	PPVBOOST_L_CN	28
TP93F4	A	1	PPVBOOST_R_FH	29
TP93F5	A	1	PPVBOOST_L_FH	29
TP93FA	A	1	GPIO_SPKRAMP_TO_SOC_IRQ_L	9 28 29
TP93FB	A	1	TDM_SPKRAMP_TO_SPKRAMP_I2C	28 29

AUDIO - CODEC

TP93F6	A	1	GPIO_CODEC_TO_PMU_WAKE_L	26 44
TP93F7	A	1	GND_AUDIO_CODEC	26
TP93F8	A	1	MIKEY_TS_P	26 48
TP93F9	A	1	MIKEY_TS_N	26 48

POWER - SENSORS

TP93G0	A	1	PP1V8_CARBON_FILT	18
TP93G2	A	1	PP1V8_PHOS_FILT	18
TP93G3	A	1	PP1V8_MAGNESIUM_FILT	18

BUTTONS

TP93G4	A	1	GPIO_BTN_HOME_L_CONN	32 34
TP93G5	A	1	GPIO_BTN_ONOFF_L_CONN	23
TP93G6	A	1	GPIO_BTN_VOL_UP_L_CONN	23
TP93G7	A	1	GPIO_BTN_VOL_DOWN_L_CONN	23

I2C

TP93G8	A	1	I2C0_SCL_1V8	4 6
TP93G9	A	1	I2C0_SDA_1V8	4 6
TP93GA	A	1	I2C1_SCL_1V8	4 6
TP93GB	A	1	I2C1_SDA_1V8	4 6
TP93GC	A	1	I2C2_SCL_1V8	4 6
TP93GD	A	1	I2C2_SDA_1V8	4 6
TP93GE	A	1	I2C3_SCL_1V8	4 6
TP93GF	A	1	I2C3_SDA_1V8	4 6

BASEBAND

BASEBAND - SIM CARD

WIFI/BT

TP93I0	A	1	GPIO_AUTUMN_TO_BT_REG_ON	35 51
TP93I1	A	1	GPIO_AUTUMN_TO_WLAN_REG_ON	35 51
TP93I2	A	1	CLK_PMU_TO_WLAN_32K	35 51
TP93I3	A	1	TP_JTAG_WLAN_TMS	51
TP93I4	A	1	GPIO_WLAN_TO_SOC_ATSP	51
TP93I5	A	1	JTAG_WLAN_SEL	35
TP93I6	A	1	TESTPOINT_JTAG_WLAN_TCK	51
TP93I7	A	1	GPIO_AOP_TO_WLAN_CONTEXT_A	9 51
TP93I8	A	1	GPIO_AOP_TO_WLAN_CONTEXT_B	9 51

CAMERA - NH

TP93I3	A	1	ISP_CAM_FRONT_CLK_CONN	24
TP93I4	A	1	ISP_CAM_FRONT_SCL_CONN	24
TP93I5	A	1	ISP_CAM_FRONT_SDA_CONN	24
TP93I6	A	1	ISP_CAM_FRONT_SHUTDOWN_L_CONN	24

CAMERA - UT

TP93I7	A	1	ISP_CAM_UT_CLK_CONN	23
TP93I8	A	1	ISP_CAM_UT_SCL_CONN	23
TP93I9	A	1	ISP_CAM_UT_SDA_CONN	23
TP93J0	A	1	ISP_CAM_UT_SHUTDOWN_L_CONN	23

MESA

TP93J1	A	1	GPIO_MESA_TO_SOC_IRQ	6 34
TP93JC	A	1	PP16V6_MESA	34
TP93JD	A	1	GPIO_MESA_TO_BOOST_ENABLE	34

HALL EFFECT

TP93J5	A	1	GPIO_APANEL_HALL_TO_PMU_IRQ_L	27 44
TP93J6	A	1	GPIO_CPANEL_HALL_TO_PMU_IRQ_L	23 44

ALS

TP93J7	A	1	GPIO_ALS_C3_TO_SOC_IRQ_L	6 23
TP93J8	A	1	GPIO_ALS_C4_TO_SOC_IRQ_L	6 27

DISPLAY

TP93J9	A	1	LPDP_TCON_TO_SOC_HPD	7 33
TP93K0	A	1	GPIO_PMU_TO_LCD_PWREN	31 32 44

AOP

TP93K1	A	1	CLK_PMU_TO_AOP_32K	9 44

AUDIO - DIGITAL MICS

TP93K2	A	1	DMIC1_MIC_SCLK_CONN	27
TP93K3	A	1	DMIC1_MIC_SD_CONN	27

AUDIO- BELFIELD

TP93R0	A	1	GPIO_BELFIELD_TO_PMU_WAKE_L	26 44
TP93R1	A	1	GPIO_BELFIELD_TO_SOC_IRQ_L	6 26

CAMERA-STROBE/HAWKING

TP93K6	A	1	PPSTROBE1_COOL_LED_CONN	23 25
TP93K7	A	1	PPSTROBE1_WARM_LED_CONN	23 25
TP93K8	A	1	PPSTROBE2_COOL_LED_CONN	23 25
TP93M0	A	1	PPSTROBE2_WARM_LED_CONN	23 25
TP93M1	A	1	LED_DRIVER_NTC_CONN	23 25
TP93M2	A	1	GPIO_REAR_CAM_TO_STROBE_EN	23 25
TP93M3	A	1	PPSTROBE1_BST	25
TP93M4	A	1	PPSTROBE2_BST	25
TP93M5	A	1	IRIS_AVOUT	22 23
TP93M6	A	1	ISP_STB_SCL	7 25
TP93M7	A	1	ISP_STB_SDA	7 25
TP93M8	A	1	GPIO_SOC_TO_LED_DRIVER_EN	6 25

TOUCH

TP93N1	A	1	PP15V0_TOUCH_FILT	19 20
TP93N2	A	1	PP2V8_KONA_M_VDDANA	19
TP93N3	A	1	PP2V8_KONA_S_VDDANA	20
TP93N4	A	1	KONA_BOOST_VBAT	19
TP93N5	A	1	KONA_BOOST_EN	19
TP93N6	A	1	GPIO_SOC_TO_1V8_TOUCH_EXT_SW_ON	6 47

SOC - ACC UART

TP93N8	A	1	UART_SOC_TO_ACC_TX	6 30
TP93N9	A	1	UART_ACC_TO_SOC_TX	6 30

SOC - GND

TP93NA	A	1	TP_VSS_SENSE	14
TP93NB	A	1	TP_VSS_CPU_SENSE	14

SOC - PWR

TP93NC	A	1	ADC_SOC_TO_PMU_VDD_CPU	12 44
TP93ND	A	1	ADC_SOC_TO_PMU_VDD_GPU	12 44
TP93NE	A	1	ADC_SOC_TO_PMU_VDD_SOC	13 44

PLACE VSS SENSE TEST POINTS NEAR BY

ORION

TP939F A 1 TP-1P0-TOP
TP939C A 1 TP-1P0-TOP — PPVBUS_ORION_CONN 49 52

TP939G A 1 TP-1P0-TOP
TP939E A 1 TP-1P0-TOP

CAN MOUNTING HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM
APN: 998-2691

SL9300 TH-NSP 1 SL-1.1X0.4-1.4X0.7
SL9303 TH-NSP 1 SL-1.1X0.4-1.4X0.7
SL9304 TH-NSP 1 SL-1.1X0.4-1.4X0.7
SL9305 TH-NSP 1 SL-1.1X0.4-1.4X0.7
SL9310 TH-NSP 1 SL-1.1X0.4-1.4X0.7

STANDOFFS

APN:860-00677 (TH), 860-00676/00522 (SMT)

STD9312 3.3X1.8R-1.4ID-1.1H-SM
STD9313 3.3X1.8R-1.4ID-1.1H-SM
STD9314 3.3X1.8R-1.4ID-1.1H-SM
STD9315 3.3X1.8R-1.4ID-1.1H-SM
STD9320 STDOFF-3.8X2.5R-1.1H-TH
STD9321 STDOFF-3.8X2.5R-1.1H-TH
STD9316 3.3X1.8R-1.4ID-1.1H-SM
STD9317 3.3X1.8R-1.4ID-1.185H-SM
STD9318 3.3X1.8R-1.4ID-1.185H-SM
STD9319 3.3X1.8R-1.4ID-1.1H-SM
STD9322 3.3X1.8R-1.4ID-1.1H-SM
STD9323 3.3X1.8R-1.4ID-1.1H-SM

FIDUCIALS

FID9300 FID 0P5SM1P0SQ-NSP
FID9301 FID 0P5SM1P0SQ-NSP
FID9302 FID 0P5SM1P0SQ-NSP
FID9303 FID 0P5SM1P0SQ-NSP
FID9304 FID 0P5SM1P0SQ-NSP
FID9305 FID 0P5SM1P0SQ-NSP

SYNC_MASTER=MLB_B
SYNC_DATE=06/01/2016
PAGE TITLE
TEST: TPS/HOLES/FIDUCUALS

EE CHARACTERIZATION PP/TP

SOC

PUT BACK PLACE_SIDE=TOP FOR CHINA BUILD

PP9501 P3MM SM (PP) 1 RESET_PMU_TO_SYSTEM_L — 5 9 44 52
PP9502 P3MM SM (PP) 1 TP_GPIO_DFU_STATUS — 6
PP9504 P3MM SM (PP) 1 ADC_SOC_TO_PMU_ANALOGMUX_OUT — 5 44
PP950A P3MM SM (PP) 1 GPIO_AOP_TO_PMU_SLEEP1_REQUEST — 9 44
PP950B P3MM SM (PP) 1 GPIO_PMU_TO_SYS_SLEEP1_READY — 9 10 44
PP950C P3MM SM (PP) 1 GPIO_AOP_TO_PMU_ACTIVE_REQUEST — 9 44
PP950D P3MM SM (PP) 1 GPIO_PMU_TO_SYSTEM_ACTIVE_READY — 5 9 30 31 44
PP950E P3MM SM (PP) 1 I2C_AOP_SCL_1V8 — 4 9
PP950F P3MM SM (PP) 1 I2C_AOP_SDA_1V8 — 4 9

CODEC I2S

PP9510 P4MM SM (PP) 1 I2S_AOP_TO_CODEC_BCLK — 9 26
PP9511 P4MM SM (PP) 1 I2S_AOP_TO_CODEC_LRCK — 9 26
PP9512 P4MM SM (PP) 1 I2S_AOP_TO_CODEC_DOUT — 9 26
PP9513 P4MM SM (PP) 1 I2S_CODEC_TO_AOP_DOUT — 9 26

BELFIELD I2S

PP9514 P4MM SM (PP) 1 I2S0_SOC_TO_BELFIELD_BCLK — 6 26
PP9515 P4MM SM (PP) 1 I2S0_SOC_TO_BELFIELD_LRCK — 6 26
PP9516 P4MM SM (PP) 1 I2S0_SOC_TO_BELFIELD_DOUT — 6 26
PP9517 P4MM SM (PP) 1 I2S0_BELFIELD_TO_SOC_DOUT — 6 26
PP9518 P4MM SM (PP) 1 I2S0_SOC_TO_BELFIELD_MCLK — 6 26

FH SPEAKER I2S

PP9520 P4MM SM (PP) 1 I2S1_SOC_TO_SPKRAMP_FH_MCLK — 6 29
PP9521 P4MM SM (PP) 1 I2S1_SOC_TO_SPKRAMP_FH_BCLK — 6 29
PP9522 P4MM SM (PP) 1 I2S1_SOC_TO_SPKRAMP_FH_LRCK — 6 29
PP9523 P4MM SM (PP) 1 I2S1_SOC_TO_SPKRAMP_FH_DOUT — 6 29
PP9524 P4MM SM (PP) 1 I2S1_SPKRAMP_FH_TO_SOC_DOUT — 6 29

CN SPEAKER I2S

PP9525 P4MM SM (PP) 1 I2S2_SOC_TO_SPKRAMP_CN_MCLK — 6 28
PP9526 P4MM SM (PP) 1 I2S2_SOC_TO_SPKRAMP_CN_BCLK — 6 28
PP9527 P4MM SM (PP) 1 I2S2_SOC_TO_SPKRAMP_CN_LRCK — 6 28
PP9528 P4MM SM (PP) 1 I2S2_SOC_TO_SPKRAMP_CN_DOUT — 6 28
PP9529 P4MM SM (PP) 1 I2S2_SPKRAMP_CN_TO_SOC_DOUT — 6 28

HAWKING

PP952A P4MM SM (PP) 1 I2S3_SOC_TO_HAWKING_BCLK — 6 22
PP952B P4MM SM (PP) 1 I2S3_SOC_TO_HAWKING_LRCK — 6 22
PP952C P4MM SM (PP) 1 I2S3_HAWKING_TO_SOC_DOUT — 6 22

EUPHRATES

PP9539 P4MM SM (PP) 1 SYS_ALIVE — 10 17 44 46

AUDIO

PP953A P4MM SM (PP) 1 GPIO_CODEC_TO_SOC_IRQ_L — 6 26

ORION

PP953B P4MM SM (PP) 1 GPIO_AOP_TO_ORION_HWEN — 9 41

UNUSED MIPI LANES

7 GND — MAKE_BASE=TRUE
7 GND — MAKE_BASE=TRUE
7 GND — MAKE_BASE=TRUE
7 GND — MAKE_BASE=TRUE
7 GND — MAKE_BASE=TRUE
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7 GND — MAKE_BASE=TRUE
7 GND — MAKE_BASE=TRUE
7 GND — MAKE_BASE=TRUE

BELFIELD SPI LINES

PP9540 P3MM SM (PP) 1 SPI_BELFIELD_CS_L — 6 26
PP9541 P3MM SM (PP) 1 SPI_BELFIELD_SCLK — 6 26
PP9542 P3MM SM (PP) 1 SPI_BELFIELD_MOSI — 6 26
PP9543 P3MM SM (PP) 1 SPI_BELFIELD_MISO — 6 26

SENSOR SPI LINES

PP9544 P3MM SM (PP) 1 SPI_SENSORS_SCLK — PLACE_NEAR=U2150.2.10MM — 9 18 27 53
PP9545 P3MM SM (PP) 1 SPI_SENSORS_MISO — PLACE_NEAR=U0600.AD40.10MM — 9 18 27
PP9546 P3MM SM (PP) 1 SPI_SENSORS_MOSI — PLACE_NEAR=U2150.3.10MM — 9 18 27 53
PP9547 P3MM SM (PP) 1 SPI_SENSORS_SCLK — PLACE_NEAR=U2120.4.10MM — 9 18 27 53
PP9548 P3MM SM (PP) 1 SPI_SENSORS_SCLK — PLACE_NEAR=U2140.A3.10MM — 9 18 27 53
PP9549 P3MM SM (PP) 1 SPI_SENSORS_MOSI — PLACE_NEAR=U2120.3.10MM — 9 18 27 53
PP954A P3MM SM (PP) 1 SPI_SENSORS_MOSI — PLACE_NEAR=U2140.A4.10MM — 9 18 27 53

MESA SPI LINES

PP954B P3MM SM (PP) 1 SPI_MESA_MISO — 6 34
PP954C P3MM SM (PP) 1 SPI_MESA_MOSI_CONN — 32 34
PP954D P3MM SM (PP) 1 SPI_MESA_SCLK_CONN — 32 34

CAMERA - FRONT

PP9560 P2MM SM (PP) 1 MIPI_NH_CAM_TO_SOC_CLK_P — NO_XNET_CONNECTION=1 — 7 24
PP9561 P2MM SM (PP) 1 MIPI_NH_CAM_TO_SOC_CLK_N — NO_XNET_CONNECTION=1 — 7 24
PP9562 P2MM SM (PP) 1 MIPI_NH_CAM_TO_SOC_DATA_P<0> — NO_XNET_CONNECTION=1 — 7 24
PP9563 P2MM SM (PP) 1 MIPI_NH_CAM_TO_SOC_DATA_N<0> — NO_XNET_CONNECTION=1 — 7 24
PP9564 P2MM SM (PP) 1 MIPI_NH_CAM_TO_SOC_DATA_P<1> — NO_XNET_CONNECTION=1 — 7 24
PP9565 P2MM SM (PP) 1 MIPI_NH_CAM_TO_SOC_DATA_N<1> — NO_XNET_CONNECTION=1 — 7 24

GRAPE

PP9580 P3MM SM (PP) 1 SPI_SOC_TO_GRAPE_SCLK — 6 19
PP9581 P3MM SM (PP) 1 SPI_SOC_TO_GRAPE_MISO — 6 19
PP9582 P3MM SM (PP) 1 SPI_SOC_TO_GRAPE_MOSI — 6 19
PP9583 P3MM SM (PP) 1 SPI_SOC_TO_GRAPE_CS_L — 6 19
PP9584 P3MM SM (PP) 1 GPIO_SOC_TO_GRAPE_RESET_L — 6 19 20
PP9585 P3MM SM (PP) 1 GPIO_GRAPE_TO_SOC_IRQ_L — 6 19
PP9586 P3MM SM (PP) 1 KONA_S_TO_KONA_M_RESET_DET_L — 19 20
PP9587 P3MM SM (PP) 1 PSE_SYNC — 19 20
PP9588 P3MM SM (PP) 1 KMSI_MISO — 19 20
PP9589 P3MM SM (PP) 1 KMSI_MOSI — 19 20
PP958A P3MM SM (PP) 1 KMSI_STRB_IN — 19 20
PP958B P3MM SM (PP) 1 KMSI_STRB_OUT — 19 20
PP958C P3MM SM (PP) 1 KONA_BOOST_ATEST — 19
PP958D P3MM SM (PP) 1 TP_KONA_S_UART_TX — 20
PP958E P3MM SM (PP) 1 TP_KONA_S_UART_RX — 20
PP958F P3MM SM (PP) 1 TP_KONA_IPC_EVENT_0 — 20
PP958G P3MM SM (PP) 1 TP_KONA_IPC_EVENT_1 — 20
PP958H P3MM SM (PP) 1 TP_KONA_IPC_EVENT_2 — 20
PP958I P3MM SM (PP) 1 TP_KONA_IPC_EVENT_3 — 20
PP958J P3MM SM (PP) 1 TP_KONA_IPC_EVENT_4 — 20
PP958K P3MM SM (PP) 1 TP_KONA_IPC_EVENT_5 — 20
PP958L P3MM SM (PP) 1 TP_KONA_GPIO_ADC_03 — 19
PP958M P3MM SM (PP) 1 CLK_KONA_M_24MHZ — 19
PP958N P3MM SM (PP) 1 GPIO_SOC_TO_GRAPE_BSYNC0 — 19 20 32
PP958P P3MM SM (PP) 1 GPIO_SOC_TO_GRAPE_BSYNC1 — 19 20 32

GRAPE POWER

PP958R P3MM SM (PP) 1 PP3V3_GRAPE_FILT — 19 20
PP958S P3MM SM (PP) 1 PP1V8_GRAPE_XTAL_FILT — 19 20
PP958T P3MM SM (PP) 1 KONA_M_VDDCORE_CAP — 19
PP958U P3MM SM (PP) 1 KONA_S_VDDCORE_CAP — 20
PP958V P3MM SM (PP) 1 PP1V8_GRAPE_AON_RC — 19 20

UNUSED LPDP RX LANES

7 GND — MAKE_BASE=TRUE
7 GND — MAKE_BASE=TRUE
7 GND — MAKE_BASE=TRUE
7 GND — MAKE_BASE=TRUE
7 GND — MAKE_BASE=TRUE
7 GND — MAKE_BASE=TRUE

DDR

PP9590 P2MM SM (PP) 1 DDR6_CS — PLACE_NEAR=U1700.AT9:1MM — 10 16
PP9591 P2MM SM (PP) 1 DDR6_CKE — PLACE_NEAR=U1700.AR9:1MM — 10 16
PP9592 P2MM SM (PP) 1 DDR6_CA<0> — PLACE_NEAR=U1700.AR8:1MM — 10 16
PP9593 P2MM SM (PP) 1 DDR6_CA<1> — PLACE_NEAR=U1700.AP9:1MM — 10 16
PP9594 P2MM SM (PP) 1 DDR6_CA<2> — PLACE_NEAR=U1700.AT11:1MM — 10 16
PP9595 P2MM SM (PP) 1 DDR6_CA<3> — PLACE_NEAR=U1700.AR11:1MM — 10 16
PP9596 P2MM SM (PP) 1 DDR6_CA<4> — PLACE_NEAR=U1700.AP11:1MM — 10 16
PP9597 P2MM SM (PP) 1 DDR6_CA<5> — PLACE_NEAR=U1700.AR12:1MM — 10 16
PP9598 P2MM SM (PP) 1 DDR6_DQ<14> — PLACE_NEAR=U1700.AR13:1MM — 10 16 53
PP9599 P2MM SM (PP) 1 DDR6_DQS_P<1> — PLACE_NEAR=U1700.AT15:1MM — 10 16 53
PP959A P2MM SM (PP) 1 DDR6_DQS_N<1> — PLACE_NEAR=U1700.AR15:1MM — 10 16 53
PP959B P2MM SM (PP) 1 DDR6_CK_P — PLACE_NEAR=U1700.AT10:1MM — 10 16
PP959C P2MM SM (PP) 1 DDR6_CK_N — PLACE_NEAR=U1700.AR10:1MM — 10 16
PP959D P2MM SM (PP) 1 DDR6_DQ<14> — PLACE_NEAR=U0600.F43:1MM — 10 16 53
PP959E P2MM SM (PP) 1 DDR6_DQS_P<1> — PLACE_NEAR=U0600.H45:1MM — 10 16 53
PP959F P2MM SM (PP) 1 DDR6_DQS_N<1> — PLACE_NEAR=U0600.H46:1MM — 10 16 53

LPDDR4 TPS

PP95A0 P2MM SM (PP) 1 DDR1_CS — PLACE_NEAR=U1600.AT9:1MM — 10 15
PP95A1 P2MM SM (PP) 1 DDR1_CKE — PLACE_NEAR=U1600.AR9:1MM — 10 15
PP95A2 P2MM SM (PP) 1 DDR1_CA<3> — PLACE_NEAR=U1600.AR11:1MM — 10 15
PP95A3 P2MM SM (PP) 1 DDR1_DQ<9> — PLACE_NEAR=U1600.AR17:1MM — 10 15 53
PP95A4 P2MM SM (PP) 1 DDR1_DQS_P<1> — PLACE_NEAR=U1600.AT15:1MM — 10 15 53
PP95A5 P2MM SM (PP) 1 DDR1_DQS_N<1> — PLACE_NEAR=U1600.AR15:1MM — 10 15 53
PP95A6 P2MM SM (PP) 1 DDR1_CK_P — PLACE_NEAR=U1600.AT10:1MM — 10 15
PP95A7 P2MM SM (PP) 1 DDR1_CK_N — PLACE_NEAR=U1600.AR10:1MM — 10 15
PP95A8 P2MM SM (PP) 1 DDR1_DQ<9> — PLACE_NEAR=U0600.AB4:1MM — 10 15 53
PP95A9 P2MM SM (PP) 1 DDR1_DQS_P<1> — PLACE_NEAR=U0600.AB2:1MM — 10 15 53
PP95AA P2MM SM (PP) 1 DDR1_DQS_N<1> — PLACE_NEAR=U0600.AB1:1MM — 10 15 53

WIFI

PP95B3 P4MM SM (PP) 1 UART_BT_TO_SOC_TX — 6 51
PP95B4 P4MM SM (PP) 1 UART_SOC_TO_BT_TX — 35 51
PP95B5 P4MM SM (PP) 1 UART_SOC_TO_WLAN_TX — 6 51
PP95B6 P4MM SM (PP) 1 UART_WLAN_TO_SOC_TX — 6 51
PP95BD P4MM SM (PP) 1 GPIO_SOC_TO_WLAN_DEVICE_WAKE — 6 51
PP95BE P4MM SM (PP) 1 GPIO_SOC_TO_BT_WAKE — 35 51
PP95BF P4MM SM (PP) 1 UART_SOC_TO_WLAN_RTS_L — 6 51
PP95BG P4MM SM (PP) 1 UART_WLAN_TO_SOC_RTS_L — 6 51
PP95BH P4MM SM (PP) 1 UART_SOC_TO_BT_RTS_L — 35 51
PP95BI P4MM SM (PP) 1 UART_BT_TO_SOC_RTS_L — 6 51
PP95BL P4MM SM (PP) 1 GPIO_SOC_TO_BT_TO_GRAPE_TS_SYNC — 6 19 20 51
PP95BM P4MM SM (PP) 1 GPIO_TOUCH_TO_BT_SYNC — 19 51

PMU/EUPHRATES

PP95G0 P4MM SM (PP) 1 GPIO_AUTUMN_TO_PMU_SOC_IRQ_L — 9 40 44
PP95G1 P4MM SM (PP) 1 GPIO_PMU_TO_SOC_IRQ_L — 9 44
PP95G2 P4MM SM (PP) 1 GPIO_EUPHRATES_TO_PMU_WAKE — 44 46
PP95G3 P4MM SM (PP) 1 GPIO_EUPHRATES_TO_SOC_TO_PMU_IRQ_L — 6 44 46
PP95G4 P4MM SM (PP) 1 OVP_SW_EN_L — 41 46
PP95G5 P4MM SM (PP) 1 GPIO_PMU_TO_EUPHRATES_LINCH_EN — 44 46
PP95G6 P4MM SM (PP) 1 GPIO_PMU_TO_1V1_EXT_SW_ON — 44 47
PP95G7 P4MM SM (PP) 1 USB_VBUS_DETECT — 5 46

DDR

PP95C0 P2MM SM (PP) 1 DDR4_CS — PLACE_NEAR=U1700.D9:1MM — 10 16
PP95C1 P2MM SM (PP) 1 DDR4_CKE — PLACE_NEAR=U1700.C9:1MM — 10 16
PP95C2 P2MM SM (PP) 1 DDR4_CA<0> — PLACE_NEAR=U1700.C8:1MM — 10 16
PP95C3 P2MM SM (PP) 1 DDR4_DQ<2> — PLACE_NEAR=U1700.D4:1MM — 10 16 53
PP95C4 P2MM SM (PP) 1 DDR4_DQS_P<0> — PLACE_NEAR=U1700.D5:1MM — 10 16 53
PP95C5 P2MM SM (PP) 1 DDR4_DQS_N<0> — PLACE_NEAR=U1700.C5:1MM — 10 16 53
PP95C6 P2MM SM (PP) 1 DDR4_CK_P — PLACE_NEAR=U1700.D10:1MM — 10 16
PP95C7 P2MM SM (PP) 1 DDR4_CK_N — PLACE_NEAR=U1700.C10:1MM — 10 16
PP95C8 P2MM SM (PP) 1 DDR4_DQ<2> — PLACE_NEAR=U0600.F24:1MM — 10 16 53
PP95C9 P2MM SM (PP) 1 DDR4_DQS_P<0> — PLACE_NEAR=U0600.B24:1MM — 10 16 53
PP95CA P2MM SM (PP) 1 DDR4_DQS_N<0> — PLACE_NEAR=U0600.A24:1MM — 10 16 53
PP95CB P2MM SM (PP) 1 DDR3_DQ<2> — PLACE_NEAR=U0600.F14:1MM — 10 15
PP95CC P2MM SM (PP) 1 DDR3_DQS_P<0> — PLACE_NEAR=U0600.B14:1MM — 10 15
PP95CD P2MM SM (PP) 1 DDR3_DQS_N<0> — PLACE_NEAR=U0600.A14:1MM — 10 15

NAND PCIE TPS

PP95D0 P2MM SN (PP) 1 — PLACE_NEAR=U0600.AW5:3MM — PCIE_NAND_TO_SOC_TX_P<0> — 8 17
PP95D1 P2MM SN (PP) 1 — PLACE_NEAR=U0600.AV5:3MM — PCIE_NAND_TO_SOC_TX_N<0> — 8 17
PP95D2 P2MM SN (PP) 1 — PLACE_NEAR=U1800.M8:3MM — PCIE_SOC_TO_NAND_TX_P<0> — 8 17
PP95D3 P2MM SN (PP) 1 — PLACE_NEAR=U1800.K8:3MM — PCIE_SOC_TO_NAND_TX_N<0> — 8 17
PP95D4 P2MM SN (PP) 1 — PLACE_NEAR=U1800.H8:3MM — PCIE_SOC_TO_NAND_REFCLK_P — 8 17
PP95D5 P2MM SN (PP) 1 — PLACE_NEAR=U1800.H6:3MM — PCIE_SOC_TO_NAND_REFCLK_N — 8 17

WLAN PCIE TPS

PP95E0 P2MM SM (PP) 1 — PLACE_NEAR=U0600.AW7:3MM — PCIE_WLAN_TO_SOC_TX_P — 8 51
PP95E1 P2MM SM (PP) 1 — PLACE_NEAR=U0600.AV7:3MM — PCIE_WLAN_TO_SOC_TX_N — 8 51
PP95E2 P2MM SM (PP) 1 — PLACE_NEAR=U0600.BA29:4MM — PCIE_WLAN_TO_SOC_CLKREQ_L — 8 51
PP95E3 P2MM SM (PP) 1 — PLACE_NEAR=U4900.4:3MM — PCIE_SOC_TO_WLAN_TX_P — 35 51
PP95E4 P2MM SM (PP) 1 — PLACE_NEAR=U4900.5:3MM — PCIE_SOC_TO_WLAN_TX_N — 35 51
PP95E5 P2MM SM (PP) 1 — PLACE_NEAR=U4900.10:3MM — PCIE_SOC_TO_WLAN_REFCLK_P — 8 51
PP95E6 P2MM SM (PP) 1 — PLACE_NEAR=U4900.11:3MM — PCIE_SOC_TO_WLAN_REFCLK_N — 8 51
PP95E7 P2MM SM (PP) 1 — PLACE_NEAR=U4900.67:3MM — PCIE_SOC_TO_WLAN_RESET_L — 8 51

BB PCIE TPS

LPDPRX TPS

PP95E0 P2MM SM (PP) 1 — PLACE_NEAR=U0600.BA8:3MM — LPDP_UT_TO_SOC_DATA_P<0> — 7 23
PP95E1 P2MM SM (PP) 1 — PLACE_NEAR=U0600.AY8:3MM — LPDP_UT_TO_SOC_DATA_N<0> — 7 23
PP95E2 P2MM SM (PP) 1 — PLACE_NEAR=U0600.BB9:4MM — LPDP_UT_TO_SOC_DATA_P<1> — 7 23
PP95E3 P2MM SM (PP) 1 — PLACE_NEAR=U0600.BA9:3MM — LPDP_UT_TO_SOC_DATA_N<1> — 7 23
PP95E4 P2MM SM (PP) 1 — PLACE_NEAR=U0600.AV8:3MM — LPDP_SOC_TO_UT_AUX — 7 23

USB3

PP95BN P2MM SM (PP) 1 — PLACE_NEAR=U0600.AW40:3MM — USB3_SOC_RX_N — 5 31
PP95BP P2MM SM (PP) 1 — PLACE_NEAR=U0600.AW41:3MM — USB3_SOC_RX_P — 5 31

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SYNC_DATE=06/01/2016

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TEST: EE TP/PP

POWER CONNECTIONS

AUGUST_BUCK0 (ACTIVE)

52 42 PPVDD_CPU — MAKE_BASE=TRUE — PPVDD_CPU — 12 42

XWC190 (SHORT-10L-0.1MM-SM): 1 — 2

52 42 PPVDD_CPU — MAKE_BASE=TRUE — PPVDD_BUCK0_SENSE — 44

AUGUST_BUCK1 (SW CONTROL)

52 42 PPVDD_GPU — MAKE_BASE=TRUE — PPVDD_GPU — 12 42

XWC191 (SHORT-10L-0.1MM-SM): 1 — 2

52 42 PPVDD_GPU — MAKE_BASE=TRUE — PPVDD_BUCK1_SENSE — 44

AUGUST_BUCK2 (SLEEP1)

52 42 PPVDD_S1_FIXED_SOC — MAKE_BASE=TRUE — PPVDD_S1_FIXED_SOC — 7 13

PPVDD_S1_FIXED_SOC — 13

PPVDD_S1_FIXED_SOC — 13

PPVDD_S1_FIXED_SOC — 13

PPVDD_S1_FIXED_SOC — 13

PPVDD_S1_FIXED_SOC — 13

PPVDD_S1_FIXED_SOC — 13

PPVDD_S1_FIXED_SOC — 13

PPVDD_S1_FIXED_SOC — 13

PPVDD_S1_FIXED_SOC — 13

PPVDD_S1_FIXED_SOC — 13

AUGUST_BUCK3 (SLEEP3)

52 42 PP1V8_S3 — MAKE_BASE=TRUE — PP1V8_S3 — 15 16

PP1V8_S3 — 30

PP1V8_S3 — 23 27

PP1V8_S3 — 31 44 49

PP1V8_S3 — 47

PP1V8_S3 — 39 43

PP1V8_S3 — 43

PP1V8_S3 — 41

PP1V8_S3 — 9 11

PP1V8_S3 — 5 50

BUCK3_SW

AUGUST_BUCK3_SW1 (ACTIVE)

52 43 49 PP1V8_SW1 — MAKE_BASE=TRUE — PP1V8_SW1 — 28 29

PP1V8_SW1 — 47

PP1V8_SW1 — 46 50

AUGUST BUCK3_SW2 (SPARE)

52 43 PP1V8_SW2_SPARE — 1138

AUTUMN_BUCK3_SW1 (ACTIVE)

52 39 PP1V8_SW1_CAM — MAKE_BASE=TRUE — PP1V8_SW1_CAM — 7 24

PP1V8_SW1_CAM — 7 23

AUTUMN BUCK3_SW3 (SLEEP2)

52 39 PP1V8_S3_SW3 — MAKE_BASE=TRUE — PP1V8_S3_SW3 — 18

PP1V8_S3_SW3 — 18

PP1V8_S3_SW3 — 18 27

BUCK3_EXT_SW1 (ACTIVE)

52 47 PP1V8_EXT_SW1 — MAKE_BASE=TRUE — PP1V8_EXT_SW1 — 11

PP1V8_EXT_SW1 — 11

PP1V8_EXT_SW1 — 11

PP1V8_EXT_SW1 — 11

PP1V8_EXT_SW1 — 9 17

PP1V8_EXT_SW1 — 6

PP1V8_EXT_SW1 — 4 6 8 44

PP1V8_EXT_SW1 — 11

PP1V8_EXT_SW1 — 11

PP1V8_EXT_SW1 — 48

BUCK3_S2_EXT_SW2 (SLEEP2)

52 47 PP1V8_S2_EXT_SW2 — MAKE_BASE=TRUE — PP1V8_S2_EXT_SW2 — 51

PP1V8_S2_EXT_SW2 — 51

PP1V8_S2_EXT_SW2 — 26

PP1V8_S2_EXT_SW2 — 27

EXTERNAL SWITCH (SW CONTROL)

52 47 PP1V8_GRAPE_EXT_SW — MAKE_BASE=TRUE — PP1V8_GRAPE_EXT_SW — 9 19 20

AUTUMN_BUCK4 (SLEEP3)

52 38 PP1V1_S3 — MAKE_BASE=TRUE — PP1V1_S3 — 47

PP1V1_S3 — 39

PP1V1_S3 — 39

PP1V1_S3 — 11 15 16

AUTUMN_BUCK4_SW1 (SPARE)

52 39 PP1V1_SW1_SPARE — MAKE_BASE=TRUE — 1138

BUCK4_EXT_SW (SLEEP1)

52 47 PP1V1_S1_EXT_SW — MAKE_BASE=TRUE — PP1V1_S1_EXT_SW — 10 11 15 16

PP1V1_S1_EXT_SW — 11

AUTUMN_BUCK5

52 38 PP1V5_CAMERA — MAKE_BASE=TRUE — PP1V5_CAMERA — 39

AUGUST_BUCK6 (SLEEP2)

52 42 PP3V3_S2 — MAKE_BASE=TRUE — PP3V3_S2 — 51

PP3V3_S2 — 47

BUCK6_EXT_SW (ACTIVE)

52 47 PP3V3_EXT_SW — MAKE_BASE=TRUE — PP3V3_EXT_SW — 17

AUGUST_BUCK7 (ACTIVE)

52 42 PPVDD_CPU_SRAM — MAKE_BASE=TRUE — PPVDD_CPU_SRAM — 13

AUGUST_BUCK8 (SW CONTROL)

52 42 PPVDD_GPU_SRAM — MAKE_BASE=TRUE — PPVDD_GPU_SRAM — 13

AUTUMN_BUCK9 (SW CONTROL)

52 38 PP2V9_PVDD_CAM_REAR — MAKE_BASE=TRUE — PP2V9_PVDD_CAM_REAR — 23

AUGUST_LDO1 (SLEEP3)

52 43 PP3V0_S3_TRISTAR — MAKE_BASE=TRUE — PP3V0_S3_TRISTAR — 30

PP3V0_S3_TRISTAR — 51

AUGUST_LDO2 (S2 - BYPASS)

52 43 PP1V8_S2_VA_VCP — MAKE_BASE=TRUE — PP1V8_S2_VA_VCP — 26

AUGUST_LDO3 (SLEEP 2)

52 43 PP3V3_S2_XBAR — MAKE_BASE=TRUE — PP3V3_S2_XBAR — 31

PP3V3_S2_XBAR — 31

PP3V3_S2_XBAR — 48

AUTUMN_LDO4 (SW CONTROL)

52 39 PP3V0_ALS — MAKE_BASE=TRUE — PP3V0_ALS — 23

PP3V0_ALS — 27

AUGUST_LDO5 (SPARE)

52 43 PPVDD_SPARE_LDO5 — MAKE_BASE=TRUE

AUGUST_LDO6 (SW CONTROL)

52 43 PP3V3_ACC — MAKE_BASE=TRUE — PP3V3_ACC — 30

AUGUST_LDO7 (ACTIVE)

52 43 PP3V3 — MAKE_BASE=TRUE — PP3V3 — 11

PP3V3 — 48

AUGUST_LDO8 (SLEEP3)

52 43 PP3V05_S3_MESA — MAKE_BASE=TRUE — PP3V05_S3_MESA — 34

AUTUMN_LDO9 (ACTIVE)

52 39 PP1V19_FRONT_CAM — MAKE_BASE=TRUE — PP1V19_FRONT_CAM — 24

AUTUMN_LDO10 (ACTIVE)

52 39 PP0V9_NAND — MAKE_BASE=TRUE — PP0V9_NAND — 17

AUGUST_LDO11 (SLEEP2)

52 43 PP3V0_SPARE_LDO11 — MAKE_BASE=TRUE — 1138

AUGUST_LDO13 (SW CONTROL)

52 43 PP3V3_GRAPE — MAKE_BASE=TRUE — PP3V3_GRAPE — 19

AUGUST_LDO14 (ACTIVE)

52 43 PP1V2_SOC — MAKE_BASE=TRUE — PP1V2_SOC — 11

PP1V2_SOC — 11

PP1V2_SOC — 11

PP1V2_SOC — 11

AUTUMN_LDO15 (SLEEP2)

52 39 PP0V775_S3_SOC_AOP — MAKE_BASE=TRUE — PP0V775_S3_SOC_AOP — 11

AUGUST_LDO16 (SLEEP3)

52 43 PP1V8_S3_MESA — MAKE_BASE=TRUE — PP1V8_S3_MESA — 34

AUTUMN_LDO17 (SW CONTROL)

39 PP2V85_REAR_CAM — MAKE_BASE=TRUE — PP2V85_REAR_CAM — 23

AUTUMN_LDO18 (SW CONTROL)

39 PP1V19_REAR_CAM — MAKE_BASE=TRUE — PP1V19_REAR_CAM — 23

AUTUMN_LDO19 (SW CONTROL)

52 39 PP3V0_UT_SVDD — MAKE_BASE=TRUE — PP3V0_UT_SVDD — 23

AUTUMN_LDO20 (SW CONTROL)

AUTUMN_LDO20 (SW CONTROL)

52 39 PP1V8_HAWKING — MAKE_BASE=TRUE — PP1V8_HAWKING — 22 23

AUTUMN_LDO21 (SW CONTROL)

39 PP2V85_FRONT_CAM — MAKE_BASE=TRUE — PP2V85_FRONT_CAM — 24

AUTUMN_LDO22 (SPARE)

52 39 PPVDD_SPARE_LDO22 — MAKE_BASE=TRUE — 1138

AUTUMN_ON_BUF

39 AUTUMN_ON_BUF — MAKE_BASE=TRUE — 1138

AUGUST_V1V2_BUF

43 PP1V2_BUF — MAKE_BASE=TRUE — 1138

CHARGER MAIN

52 46 PPVCC_MAIN — MAKE_BASE=TRUE — PPVCC_MAIN — 42

PPVCC_MAIN — 42

PPVCC_MAIN — 42

PPVCC_MAIN — 38 42

PPVCC_MAIN — 39 43

PPVCC_MAIN — 26

PPVCC_MAIN — 33

PPVCC_MAIN — 45

PPVCC_MAIN — 34

PPVCC_MAIN — 35

PPVCC_MAIN — 41

PPVCC_MAIN — 25

PPVCC_MAIN — 45 47

PPVCC_MAIN — 19

CHARGER HIGH

52 46 PPVCC_HIGH — MAKE_BASE=TRUE — PPVCC_HIGH — 39 43

PPVCC_HIGH

PPVCC_HIGH — 34

BATTERY

52 49 PPBATT_VCC — MAKE_BASE=TRUE — PPBATT_VCC — 49

PPBATT_VCC

PPBATT_VCC — 28 29

USB POWER INPUT

52 PPVBUS_PROT — MAKE_BASE=TRUE — PPVBUS_PROT — 41 46

ON_BUF

52 43 6 PP1V8_ALWAYS — MAKE_BASE=TRUE — PP1V8_ALWAYS — 44 46

BACKLIGHT BOOST

52 45 PPLED_OUT_A — MAKE_BASE=TRUE — PPLED_OUT_A — 33

52 45 PPLED_OUT_B — MAKE_BASE=TRUE — PPLED_OUT_B — 33

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