# 電子類元件 零件承認書文件 CHECK LIST

零件廠商：**MPS**　　品名規格：MP1475DJ-LF-Z

技嘉料號：10TA1-601475-11R

| 項次 | 文件項目 |
|---|---|
| **Data Sheet 檢核項目** | |
| 1 | DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**) |
| 2 | 零件 Making 文字面說明 |
| 3 | 零件 Part Number 說明 |
| 4 | 零件 Qualification Test Report |
| 5 | 料件包裝方式及包裝 Label 之零件 Part number 說明 |
| 6 | UL Safety Report (If Request ) |
| 7 | 零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2** |
| 8 | 零件樣品 20PCS(Chipset 等高單價，至少 1PCS) |
| **9** | **電子零件承認基本調查表。註 3** |
| 10 | 以上資料電子檔為 PDF 檔，且是同 1 個 File |
| **GSCM 綠色產品管理系統-物料管制文件檢核清單** | |
| 物料管制文件 1 | GSCM 綠色產品管理系統：零件照片 |
| 物料管制文件 2 | GSCM 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4** |
| 物料管制文件 3 | GSCM 綠色產品管理系統：Data Sheet |
| **GSCM 綠色產品管理系統-MCD 表格** | |
| MCD 表格 | 物質內容宣告表格 (Material Content Declaration, MCD) |
| **其他文件 (僅適用電阻、電容類之系列元件)** | |
| 附件 1 | 危害物質測試報告 Test Report of Hazardous Substances。**註 5** |
| 附件 2 | 元件調查表 Component Composition Table |

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等

※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)

2.1. 基本需符合 JEDEC 規範

2.2. Ambient Temp. (Reflow Temp endurace): >225℃, 70 sec. 零件塑膠材質需 PA9T(含)等級以上

2.3. PASTE IN HOLE 零件塑膠材質需 PA9T(含)等級以上

※ **3. 電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G*,11T***

**非 IC 類：10C*,11C*,10L*,11L*,10X*,11X*,10R*,11B***

※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”

※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

# 電子零件承認基本調查表

| 一、原物料規格/來源 | | | |
|---|---|---|---|
| 項次 | 部位名稱/規格 | 材質 | 原物料來源產地 |
| 1 | LEAD FRAME | COPPER ALLOY | China |
| 2 | TIN PLATE | PURE TIN | China |
| 3 | MOLD COMPOUND | FUSED SILICA | China |
| 4 | FLUX | FLUX | China |
| 5 | DIE | SILICON CHIP | TW |

| 二、晶圓廠(非 IC 類免填) | | | | | |
|---|---|---|---|---|---|
| 項次 | 工廠名稱 | 生產產地 | Wafer (吋) | 投產率(%) | 自有/外包 |
| 1 | HHNEC | China | 8 | 21.82 | Subcon |
| 2 | ASMC | China | 8 | 75 | Subcon |
| 3 | SMIC | China | 8 | 30 | Subcon |

| 三、封裝廠(IC 類)；成品之生產製造工廠(非 IC 類) | | | | |
|---|---|---|---|---|
| 項次 | 工廠名稱 | 生產產地 | 投產比率(%) | 自有/外包 |
| 1 | ASE GROUP | China | According to planning department | Subcon |
| 2 | ANST | China | According to planning department | Subcon |
| 3 | UNISEM | China | According to planning department | Subcon |

| 四、產能 | |
|---|---|
| 總產能(月/PCS) | 可供技嘉產能(月/PCS) |
| 200M | According to planning department |

※ 1. IC 類之晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 2. 非 IC 類零件之成品生產製造工廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 3. 以上資訊欄位若有不足，可自行增加行數

# MP1475

## High-Efficiency, 3A, 16V, 500kHz Synchronous, Step-Down Converter

The Future of Analog IC Technology

## DESCRIPTION

The MP1475 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution to achieve a 3A continuous output current with excellent load and line regulation over a wide input supply range. The MP1475 has synchronous mode operation for higher efficiency over the output current load range.

Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection and thermal shut down.

The MP1475 requires a minimal number of readily-available standard external components, and is available in a space-saving 8-pin TSOT23 package.

## FEATURES

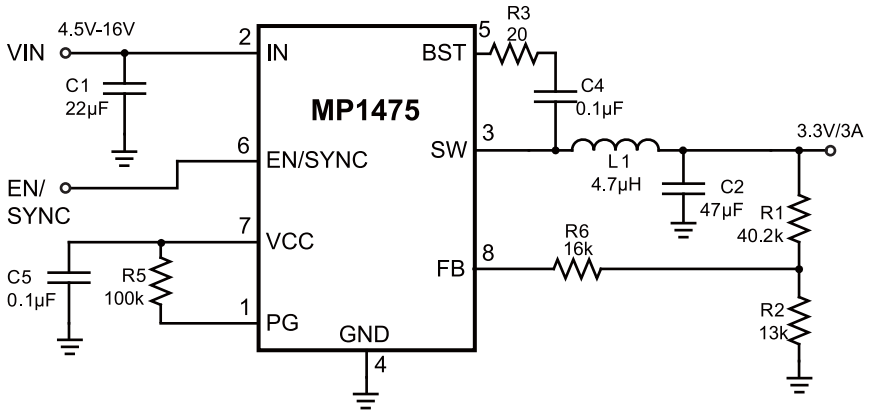
- Wide 4.5V-to-16V Operating Input Range
- 80mΩ/30mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Fixed 500kHz Switching Frequency
- Synchronizes from a 200kHz-to-2MHz External Clock
- Power-Save Mode at light load
- Internal Soft-Start
- Power Good Indicator
- OCP Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in an 8-pin TSOT-23 Package

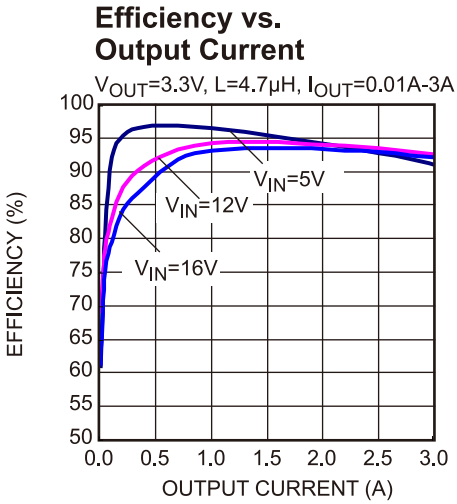
## APPLICATIONS

- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- Distributed Power Systems



## TYPICAL APPLICATION



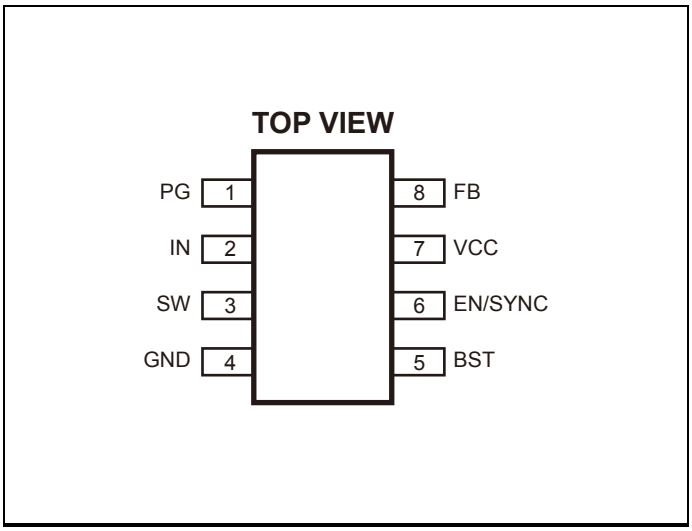



## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP1475DJ | TSOT-23-8 | ADP |

* For Tape & Reel, add suffix –Z (e.g. MP1475DJ–Z);
For RoHS Compliant Packaging, add suffix –LF (e.g. MP1475DJ–LF–Z)

## PACKAGE REFERENCE




## ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN}$ ..... -0.3V to 17V
$V_{SW}$ .....
-0.3V (-5V for <10ns) to 17V (19V for <10ns)
$V_{BST}$ ..... $V_{SW}$+6V
All Other Pins.....-0.3V to 6V (2)
Continuous Power Dissipation ($T_A$ = +25°C) (3)
.....1.25W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-65°C to 150°C

## *Recommended Operating Conditions* (4)

Supply Voltage $V_{IN}$ ..... 4.5V to 16V
Output Voltage $V_{OUT}$.....0.8V to $V_{IN}$ x $D_{MAX}$
Operating Junction Temp. ($T_J$). -40°C to +125°C

## *Thermal Resistance* (5) $\theta_{JA}$ $\theta_{JC}$

TSOT-23-8 ..... 100 ..... 55 ... °C/W

**Notes:**

1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS MAX rating, please refer to Page 9, Enable/SYNC control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS (6)

**$V_{IN}$ = 12V, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Current (Shutdown) | $I_{IN}$ | $V_{EN}$ = 0V | | 7 | | μA |
| Supply Current (Quiescent) | $I_q$ | $V_{EN}$ = 2V, $V_{FB}$ = 1V | | 0.6 | 1 | mA |
| HS Switch-On Resistance | $HS_{RDS-ON}$ | $V_{BST-SW}$=5V | | 80 | | mΩ |
| LS Switch-On Resistance | $LS_{RDS-ON}$ | $V_{CC}$ =5V | | 30 | | mΩ |
| Switch Leakage | $SW_{LKG}$ | $V_{EN}$ = 0V, $V_{SW}$ =12V | | | 1 | μA |
| Current Limit (6) | $I_{LIMIT}$ | Under 40% Duty Cycle | 4.2 | 5 | | A |
| Oscillator Frequency | $f_{SW}$ | $V_{FB}$=0.75V | 430 | 500 | 570 | kHz |
| Fold-Back Frequency | $f_{FB}$ | $V_{FB}$<400mV | | 0.25 | | $f_{SW}$ |
| Maximum Duty Cycle | $D_{MAX}$ | $V_{FB}$=700mV | 90 | 95 | | % |
| Minimum On Time(6) | $\tau_{ON\_MIN}$ | | | 40 | | ns |
| Sync Frequency Range | $f_{SYNC}$ | | 0.2 | | 2 | MHz |
| Feedback Voltage | $V_{FB}$ | $T_A$ =25°C | 791 | 807 | 823 | mV |
| | | -40°C<$T_A$<85°C (7) | 787 | 807 | 827 | |
| Feedback Current | $I_{FB}$ | $V_{FB}$=820mV | | 10 | 50 | nA |
| EN Rising Threshold | $V_{EN\_RISING}$ | | 1.2 | 1.4 | 1.6 | V |
| EN Falling Threshold | $V_{EN\_FALLING}$ | | 1.1 | 1.25 | 1.4 | V |
| EN Input Current | $I_{EN}$ | $V_{EN}$=2V | | 2 | | μA |
| | | $V_{EN}$=0 | | 0 | | μA |
| EN Turn-Off Delay | $EN_{td-off}$ | | | 5 | | μs |
| Power-Good Rising Threshold | $PG_{vth-Hi}$ | | | 0.9 | | $V_{FB}$ |
| Power-Good Falling Threshold | $PG_{vth-Lo}$ | | | 0.85 | | $V_{FB}$ |
| Power-Good Delay | $PG_{Td}$ | | | 0.4 | | ms |
| Power-Good Sink Current Capabilily | $V_{PG}$ | Sink 4mA | | | 0.4 | V |
| Power-Good Leakage Current | $I_{PG-LEAK}$ | | | | 1 | μA |
| VIN Under-Voltage Lockout Threshold-Rising | $INUV_{Vth}$ | | 3.7 | 3.9 | 4.1 | V |
| VIN Under-Voltage Lockout Threshold-Hysteresis | $INUV_{HYS}$ | | | 650 | | mV |
| VCC Regulator | $V_{CC}$ | | | 5 | | V |
| VCC Load Regulation | | $I_{CC}$=5mA | | 3 | | % |
| Soft-Start Period | $\tau_{SS}$ | | | 1.2 | | ms |
| Thermal Shutdown (6) | | | | 150 | | °C |
| Thermal Hysteresis (6) | | | | 20 | | °C |

**Notes:**

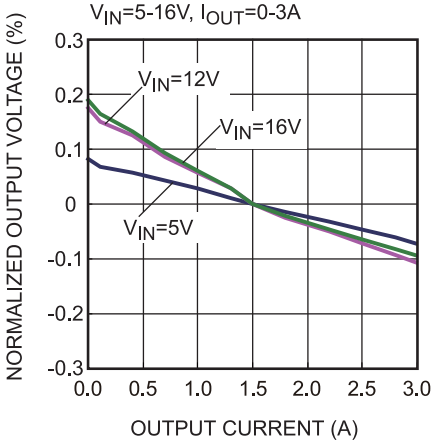
6) Guaranteed by design.

7) Not tested in production and guaranteed by over-temperature correlation.

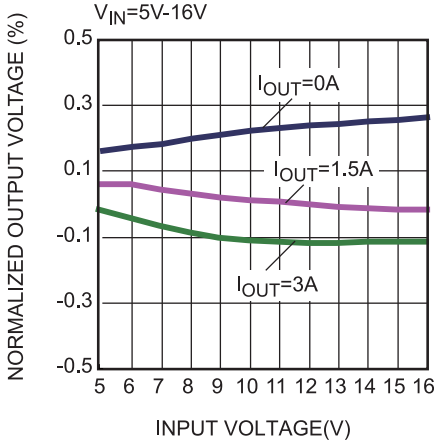
## TYPICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, L=4.7µH, $T_A$ = 25°C, unless otherwise noted.**

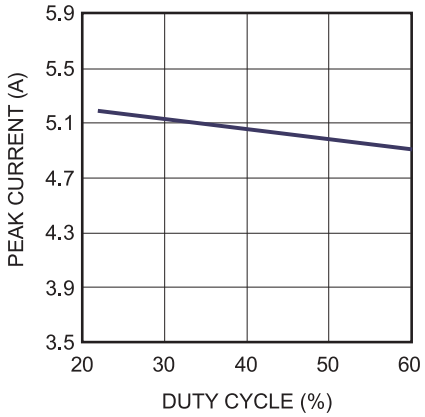
### Load Regulation



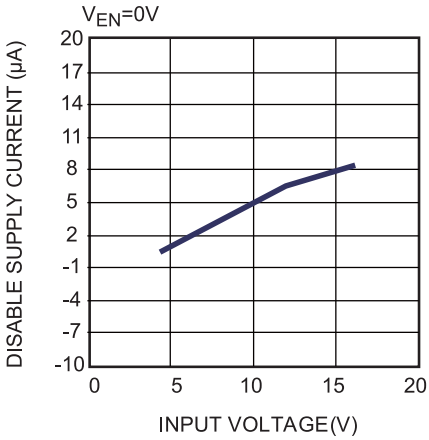

### Line Regulation



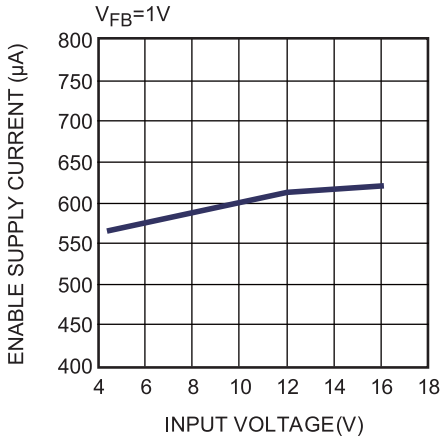

### Peak Current vs. Duty Cycle




### Disabled Supply Current vs. Input Voltage




### Enabled Supply Current vs. Input Voltage

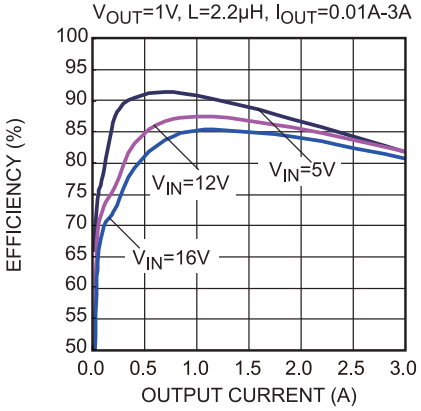


# TYPICAL PERFORMANCE CHARACTERISTICS

**Performance waveforms are tested on the evaluation board of the Design Example section.**
**$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, L=4.7µH, $T_A$ = 25°C, unless otherwise noted.**

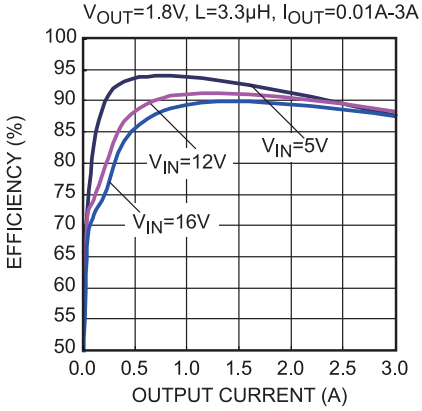
### Efficiency vs. Output Current

$V_{OUT}$=1V, L=2.2µH, $I_{OUT}$=0.01A-3A



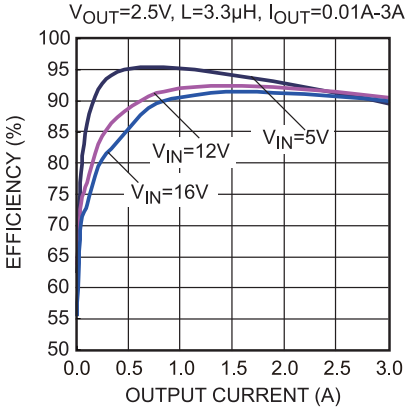

### Efficiency vs. Output Current

$V_{OUT}$=1.8V, L=3.3µH, $I_{OUT}$=0.01A-3A



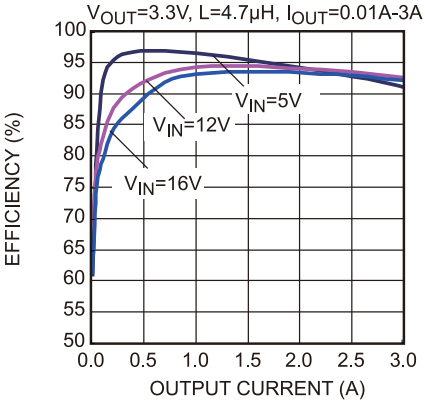

### Efficiency vs. Output Current

$V_{OUT}$=2.5V, L=3.3µH, $I_{OUT}$=0.01A-3A



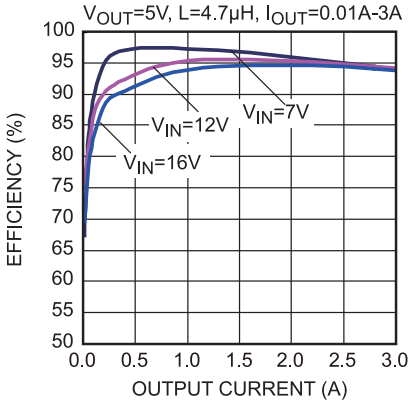

### Efficiency vs. Output Current

$V_{OUT}$=3.3V, L=4.7µH, $I_{OUT}$=0.01A-3A



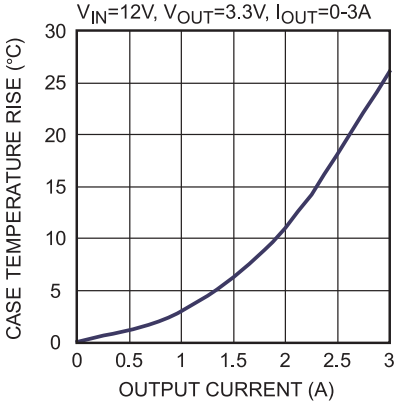

### Efficiency vs. Output Current

$V_{OUT}$=5V, L=4.7µH, $I_{OUT}$=0.01A-3A



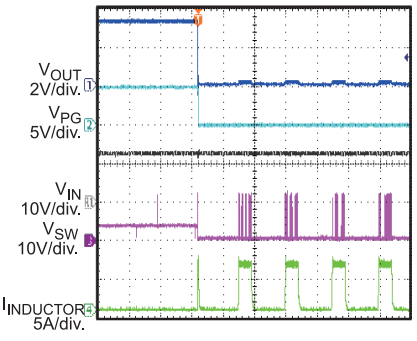

### Case Temperature Rise vs. Output Current

$V_{IN}$=12V, $V_{OUT}$=3.3V, $I_{OUT}$=0-3A



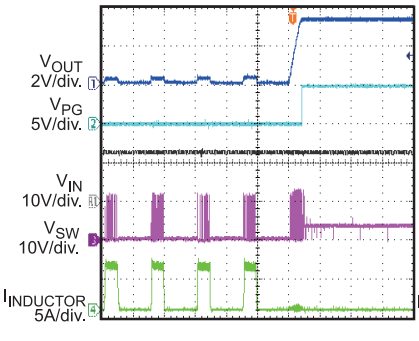

### Short Entry

$I_{OUT}$=0A



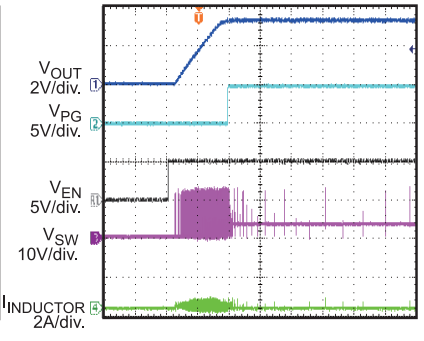

### Short Recovery

$I_{OUT}$=0A




### Startup through Enable

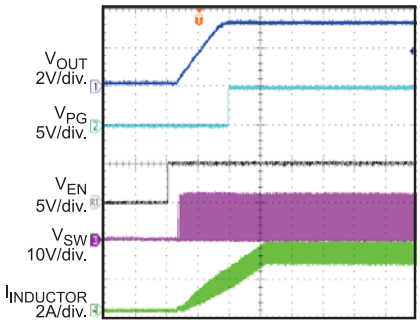
$I_{OUT}$=0A



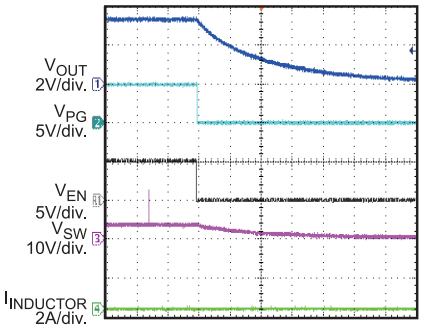
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board of the Design Example section.**
**$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, L=5.5µH, $T_A$ = 25°C, unless otherwise noted.**

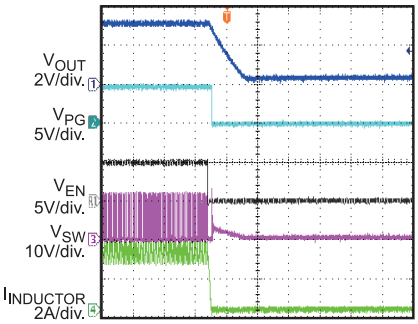
**Startup through Enable**
$I_{OUT}$=3A



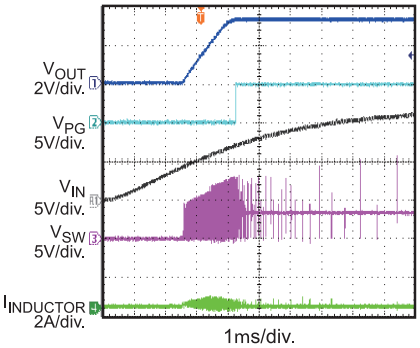

**Shutdown through Enable**
$I_{OUT}$=0A



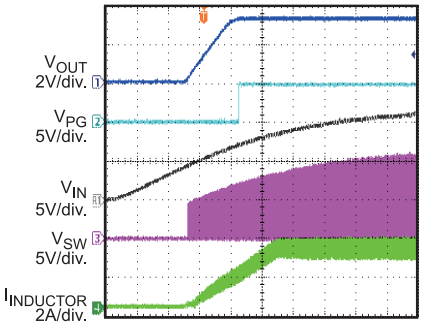

**Shutdown through Enable**
$I_{OUT}$=3A



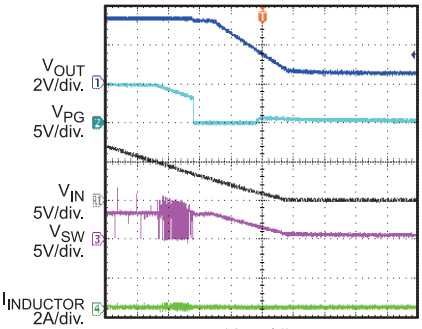

**Startup through Input Voltage**
$I_{OUT}$=0A



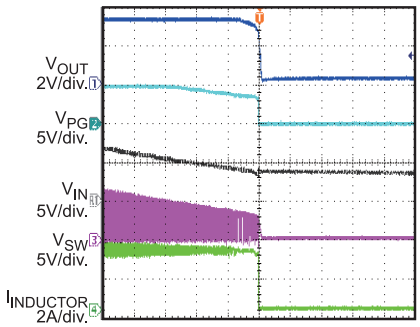

**Startup through Input Voltage**
$I_{OUT}$=3A



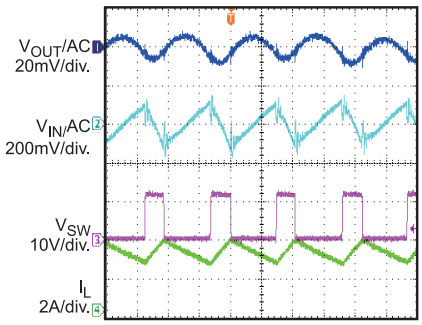

**Shutdown through Input Voltage**
$I_{OUT}$=0A



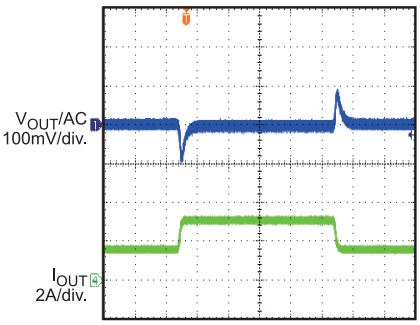

**Shutdown through Input Voltage**
$I_{OUT}$=3A




**Input / Output Ripple**
$I_{OUT}$=3A




**Load Transient Reponse**
$I_{OUT}$=1.5A-3A



## PIN FUNCTIONS

| Package Pin # | Name | Description |
|---|---|---|
| 1 | PG | Power Good Output. The output of this pin is an open drain that goes high if the output voltage exceeds 90% of the normal voltage. There is a 0.4ms delay between when FB≥90% to when the PG pin goes high. |
| 2 | IN | Supply Voltage. The IN pin supplies power for internal MOSFET and regulator. The MP1475 operates from a +4.5V to +16V input rail. Requires a low-ESR, and low-inductance capacitor (C1) to decouple the input rail. Place the input capacitor very close to this pin and connect it with wide PCB traces and multiple vias to make the connection. |
| 3 | SW | Switch Output. Connect this pin to the inductor and bootstrap capacitor. This pin is driven up to $V_{IN}$ by the high-side switch during the PWM duty cycle ON-time. The inductor current drives the SW pin negative during the OFF-time. The ON-resistance of the low-side switch and the internal body diode fixes the negative voltage. Connect using wide PCB traces and multiple vias. |
| 4 | GND | System Ground. Reference ground of the regulated output voltage. PCB layout requires extra care. For best results connect to GND with copper and vias. |
| 5 | BST | Bootstrap. Requires a capacitor connected between SW and BST pins is required to form a floating supply across the high-side switch driver. |
| 6 | EN/SYNC | Enable. EN=high to enable the MP1475. Apply an external clock to change the switching frequency. For automatic start-up, connect EN pin to $V_{IN}$ with an 100kΩ resistor. |
| 7 | VCC | Internal 5V LDO output. Powers the driver and control circuits are powered from this voltage. Decouple with a 0.1μF-0.22μF capacitor. Do not use a capacitor ≥0.22μF. |
| 8 | FB | Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 400mV to prevent current limit runaway during a short-circuit fault condition. Place the resistor divider as close to the FB pin as possible. Avoid placing vias on the FB traces. |

## FUNCTIONAL BLOCK DIAGRAM

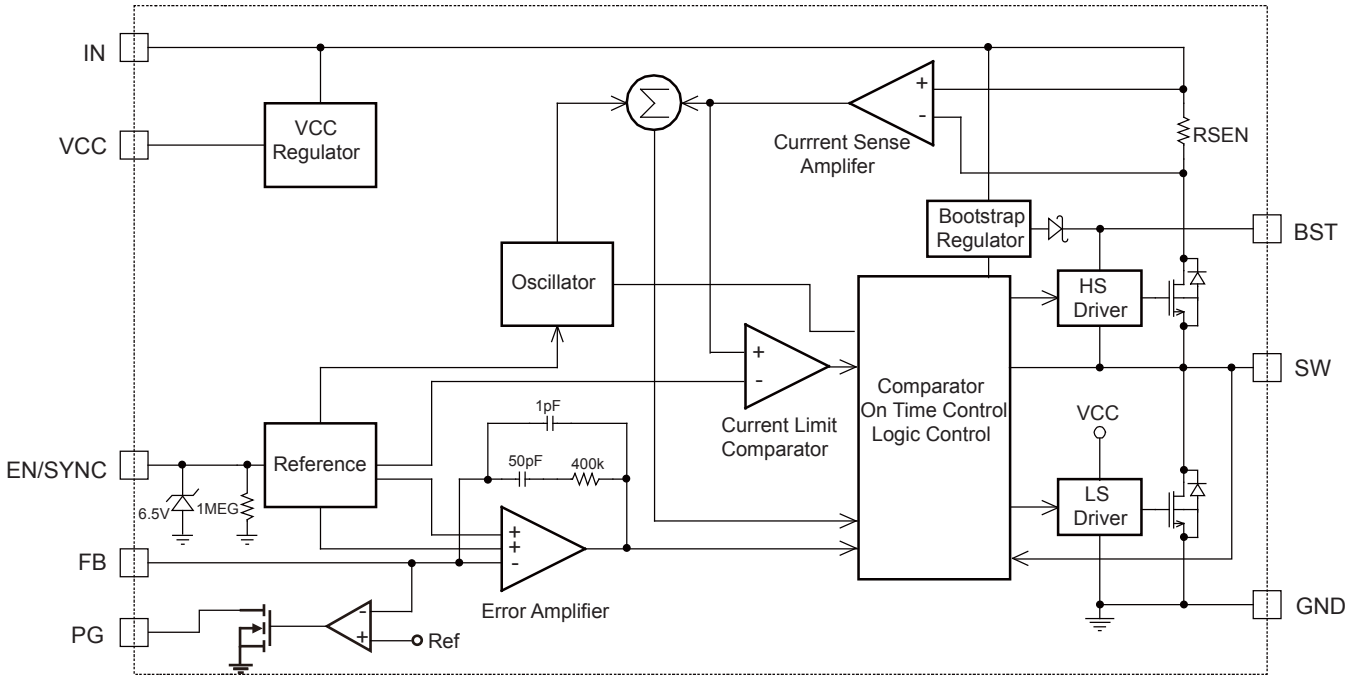



**Figure 1: Functional Block Diagram**

## OPERATION

The MP1475 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves a 3A continuous output current with excellent load and line regulation over a wide input supply range.

The MP1475 operates in a fixed-frequency, peak-current–control mode to regulate the output voltage. An internal clock initiates a PWM cycle. The integrated high-side power MOSFET turns on and remains on until the current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, within 95% of one PWM period, the current in the power MOSFET does not reach the value set by the COMP value, the power MOSFET is forced to turn off.

### Internal Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes the $V_{IN}$ input and operates in the full $V_{IN}$ range. When $V_{IN}$ exceeds 5.0V, the output of the regulator is in full regulation. When $V_{IN}$ is less than 5.0V, the output decreases, and the part requires a 0.1μF ceramic decoupling capacitor.

### Error Amplifier

The error amplifier compares the FB pin voltage to the internal 0.807V reference ($V_{REF}$) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form the COMP voltage, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

### Enable/SYNC control

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive it low to turn it off. An internal 1MΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

The EN pin is clamped internally using a 6.5V series-Zener-diode as shown in Figure 2. Connecting the EN input pin through a pullup resistor to the voltage on the IN pin limits the EN input current to less than 100μA.

For example, with 12V connected to IN, $R_{PULLUP}$ ≥ (12V – 6.5V) ÷ 100μA = 55kΩ.

Connecting the EN pin is directly to a voltage source without any pullup resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

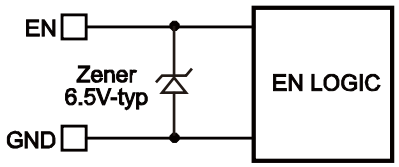



**Figure 2: 6.5V Zener Diode Connection**

For external clock synchronization, connect a clock with a frequency range between 200kHz and 2MHz 2ms after the output voltage is set: The internal clock rising edge will synchronize with the external clock rising edge. Select an external clock signal with a pulse width less than 1.7μs.

### Under-Voltage Lockout (UVLO)

The MP1475 has under-voltage lock-out protection (UVLO). When the VCC voltage exceeds the UVLO rising threshold voltage, the MP1475 will power up. It shuts off when the VCC voltage drops below the UVLO falling threshold voltage. This is non-latch protection.

The MP1475 is disabled when the input voltage falls below 3.25V. If an application requires a higher under-voltage lockout (UVLO) threshold, use the EN pin as shown in Figure 3 to adjust the input voltage UVLO by using two external resistors. For best results, set the UVLO falling threshold (VSTOP) above 4.5V using the enable resistors. Set the rising threshold (VSTART) to provide enough hysteresis to allow for any input supply variations.

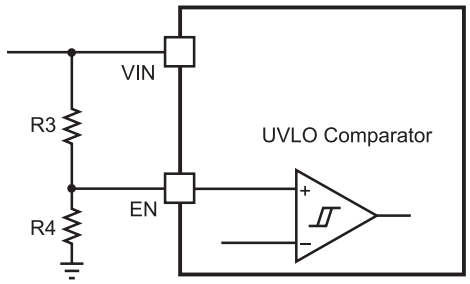



**Figure 3: Adjustable UVLO**

### Internal Soft-Start

The soft-start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage ($V_{SS}$) that ramps up from 0V to 1.2V. When $V_{SS}$ is less than $V_{REF}$, the error amplifier uses $V_{SS}$ as the reference. When $V_{SS}$ exceeds $V_{REF}$, the error amplifier uses $V_{REF}$ as the reference. The SS time is internally set to 1.2ms.

### Power Good Indicator

MP1475 has an open drain pin as the power-good indicator (PG). Pull this up to VCC or another external source through a 100kΩ resistor. When $V_{FB}$ exceeds 90% of $V_{REF}$, PG switches goes high with 0.4ms delay time. If $V_{FB}$ goes below 85% of $V_{REF}$, an internal MOSFET pulls the PG pin down to ground.

The internal circuit keeps the PG low once the input supply exceeds 1.2V.

### Over-Current-Protection and Hiccup

The MP1475 has a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, the output voltage drops until $V_{FB}$ is below the under-voltage (UV) threshold—typically 50% below the reference. Once UV is triggered, the MP1475 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground, and greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator. The MP1475 exits the hiccup mode once the over-current condition is removed.

### Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 150°C, it shuts down the whole chip. When the temperature drops below its lower threshold, typically 130°C, the chip is enabled again.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by $V_{IN}$ through D1, M1, R3, C4, L1 and C2 (Figure 4). If ($V_{IN}$-$V_{SW}$) exceeds 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4. A 20Ω resistor placed between SW and BST cap. is strongly recommended to reduce SW spike voltage.

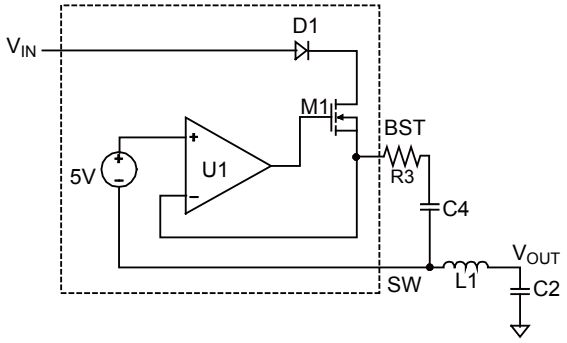



**Figure 4: Internal Bootstrap Charging Circuit**

### Startup and Shutdown

If both $V_{IN}$ and $V_{EN}$ exceed their respective thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: $V_{EN}$ low, $V_{IN}$ low, and thermal shutdown. During the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

## APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). Choose R1 around 40kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.807V} - 1}$$

The T-type network—as shown in Figure 5—is highly recommended when $V_{OUT}$ is low.

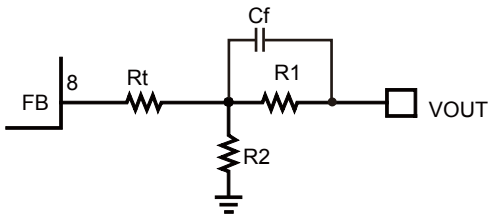



**Figure 5: T-Type Network**

Table 1 lists the recommended T-type resistors value for common output voltages.

**Table 1: Resistor Selection for Common Output Voltages**

| $V_{OUT}$ (V) | R1 (kΩ) | R2 (kΩ) | Rt (kΩ) | Cf(pF) | L(μH) |
|---|---|---|---|---|---|
| 1.0 | 20.5 | 84.5 | 82 | 15 | 2.2 |
| 1.2 | 30.1 | 61.9 | 82 | 15 | 2.2 |
| 1.8 | 40.2 | 32.4 | 33 | 15 | 3.3 |
| 2.5 | 40.2 | 19.1 | 33 | 15 | 3.3 |
| 3.3 | 40.2 | 13 | 16 | 15 | 4.7 |
| 5 | 40.2 | 7.68 | 16 | 15 | 4.7 |

### Selecting the Inductor

Use a1μH-to-10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where $\Delta I_L$ is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Use a larger inductor for improved efficiency under light-load conditions—below 100mA.

### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore requires a capacitor is to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 22μF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high quality ceramic capacitor (e.g. 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated as:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

### Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where $L_1$ is the inductor value and $R_{ESR}$ is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP1475 can be optimized for a wide range of capacitance and ESR values.

### External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- $V_{OUT}$ is 5V or 3.3V; and
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, add an external BST diode from the VCC pin to BST pin, as shown in Figure 6.

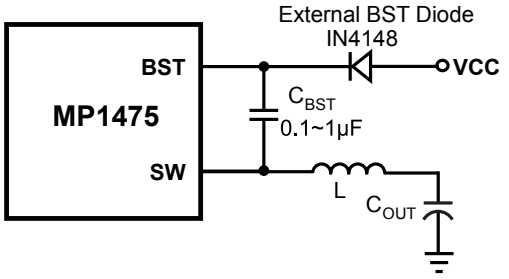



**Figure 6: Optional External Bootstrap Diode to Enhance Efficiency**

The recommended external BST diode is IN4148, and the BST capacitor value is 0.1μF to 1μF.

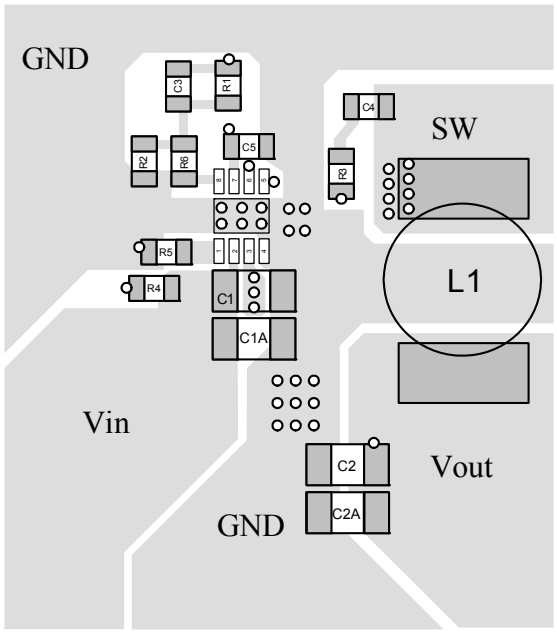
## PC Board Layout [8]

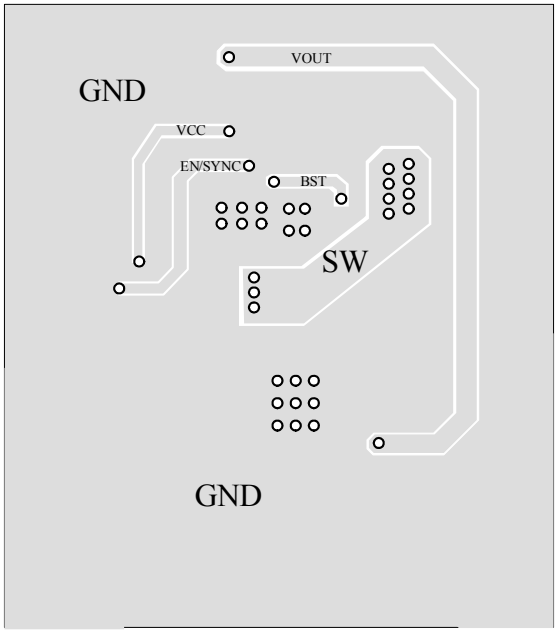
PCB layout is very important to achieve stable operation especially for VCC capacitor and input capacitor placement. For best results, follow these guidelines:

1. Use large ground plane directly connect to GND pin. Add vias near the GND pin if bottom layer is ground plane.
2. Place the VCC capacitor to VCC pin and GND pin as close as possible. Make the trace length of VCC pin-VCC capacitor anode-VCC capacitor cathode-chip GND pin as short as possible.
3. Place the ceramic input capacitor close to IN and GND pins. Keep the connection of input capacitor and IN pin as short and wide as possible.
4. Route SW, BST away from sensitive analog areas such as FB. It's not recommended to route SW, BST trace under chip's bottom side.
5. Place the T-type feedback resistor R6 close to chip to ensure the trace which connects to FB pin as short as possible

**Notes:**

8) The recommended layout is based on the Figure 7 Typical Application circuit on the next page.




## Design Example

Below is a design example following the application guidelines for the specifications:

**Table 2: Design Example**

| | |
|---|---|
| $V_{IN}$ | 12V |
| $V_{OUT}$ | 3.3V |
| Io | 3A |

The detailed application schematic is shown in Figure 8. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

# TYPICAL APPLICATION CIRCUITS

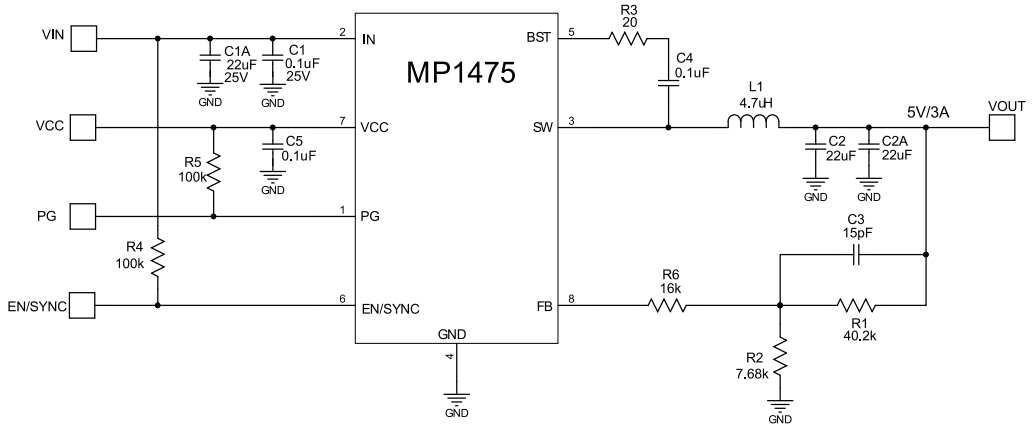



**Figure 7: $12V_{IN}$, 5V/3A Output**

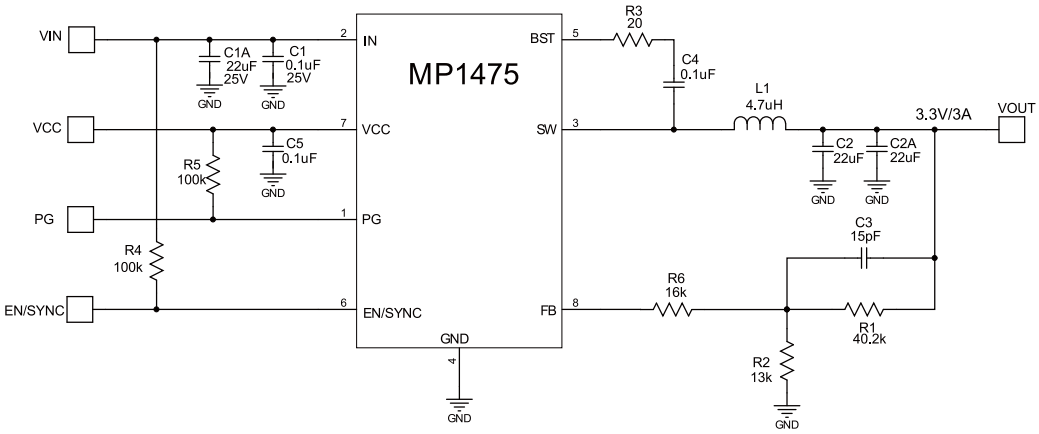



**Figure 8: $12V_{IN}$, 3.3V/3A Output**

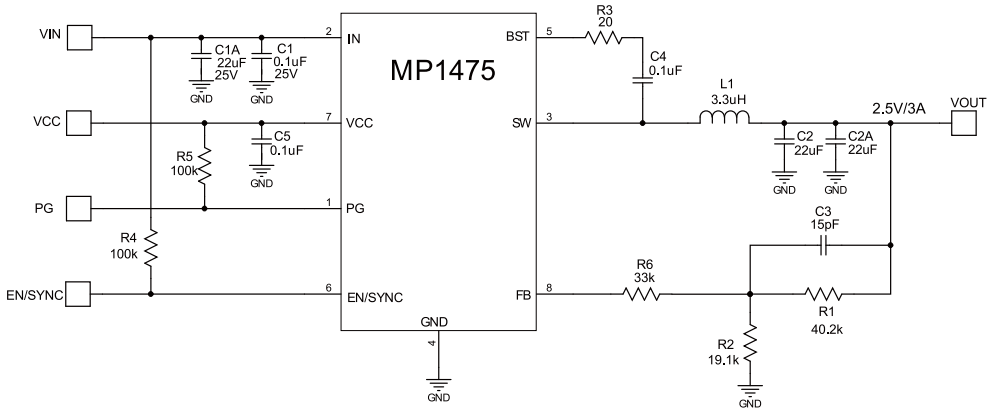



**Figure 9: $12V_{IN}$, 2.5V/3A Output**

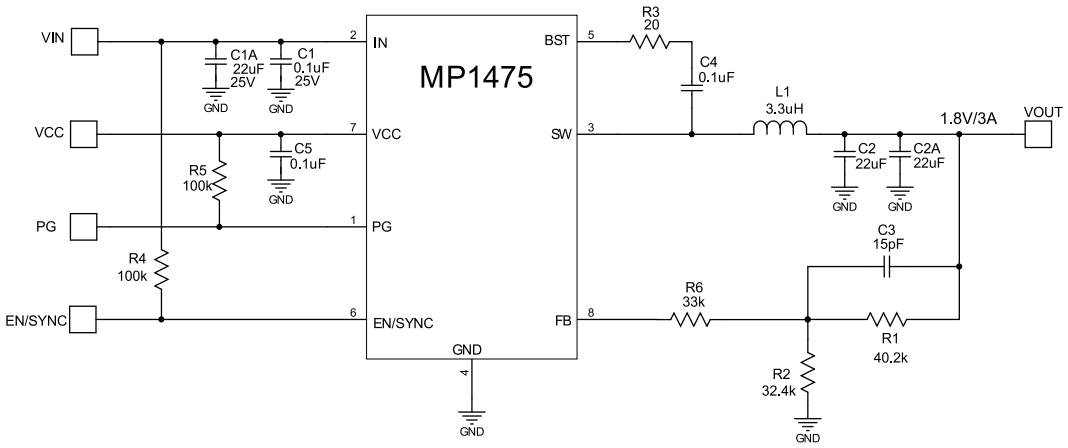



**Figure 10: $12V_{IN}$, 1.8V/3A Output**

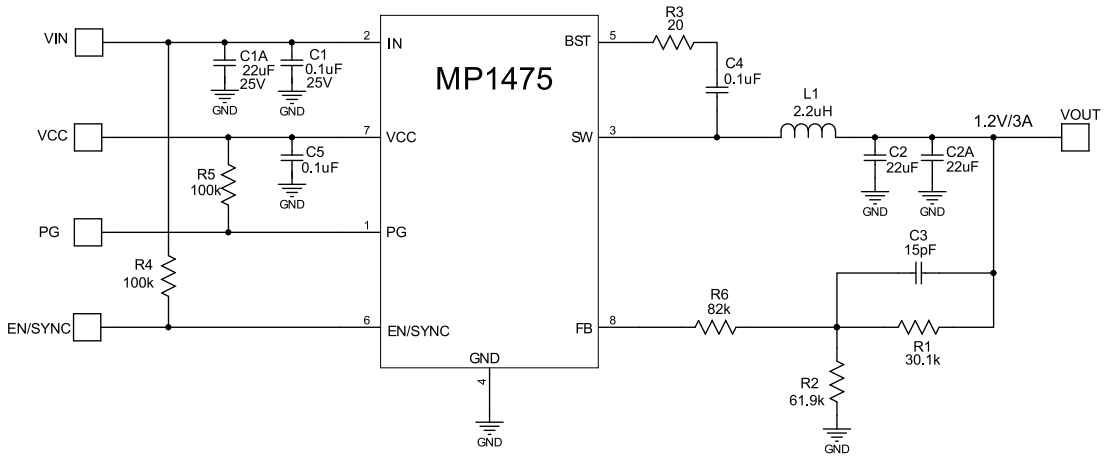



**Figure 11: $12V_{IN}$, 1.2V/3A Output**

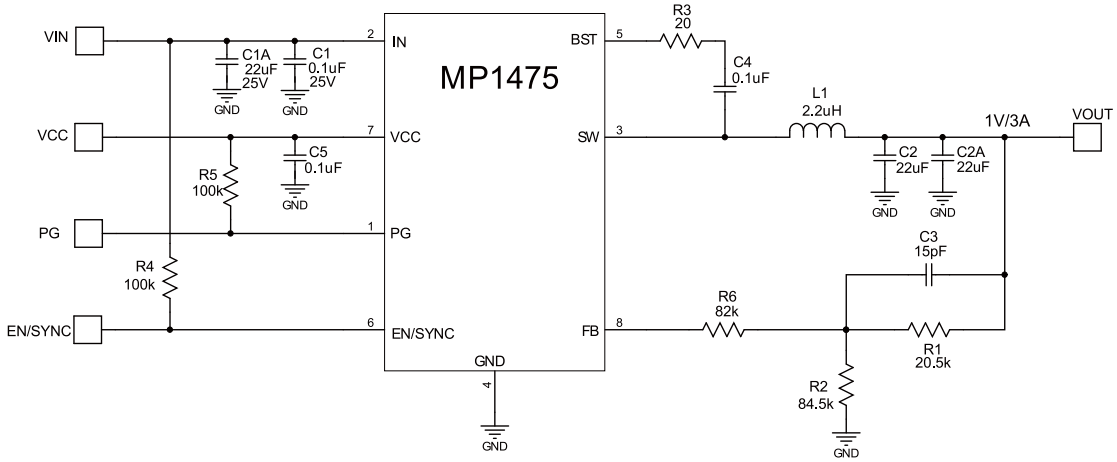
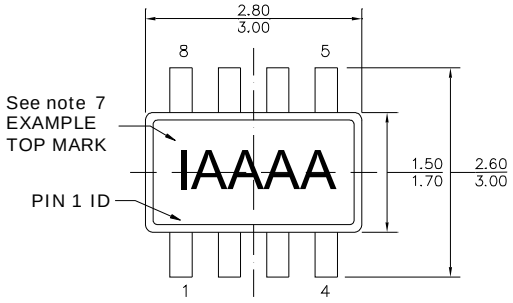


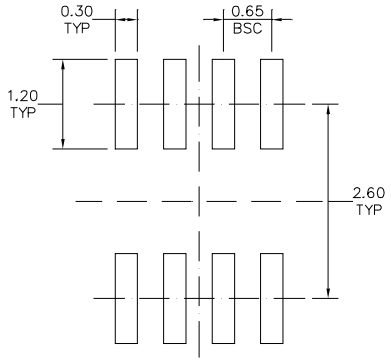

**Figure 12: $12V_{IN}$, 1V/3A Output**

## PACKAGE INFORMATION

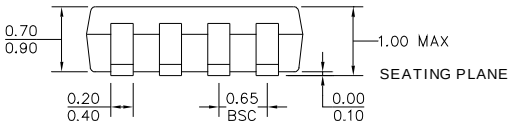
### TSOT23-8



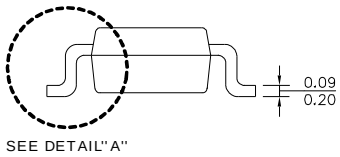

TOP VIEW



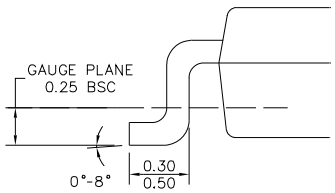

RECOMMENDED LAND PATTERN




FRONT VIEW




SIDE VIEW




DETAIL "A"

NOTE:

**1) ALL DIMENSIONS ARE IN MILLIMETERS**
**2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR**
**3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION**
**4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX**
**5) JEDEC REFERENCE IS MO-193, VARIATION BA**
**6) DRAWING IS NOT TO SCALE**
**7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)**

| | | | |
|---|---|---|---|
| The Future of Analog IC Technology™<br>**Proprietary Information** | **SPEC NO: MF-AS-P-0006** | **REV:11.0** | **PAGE 1 OF 12** |
| | **TITLE: MOISTURE SENSITIVITY LEVEL LIST**<br>**潮湿敏感度等级表** | | |

| **Originator:** | **Date:** | **Extension:** | **ECN#:** |
|---|---|---|---|
| **KEVIN WAN** | **06/30/2015** | **3603** | **S-05762** |
| **Affected Facility:**<br>☒ San Jose<br>☒ Chengdu | **Type of Change:**<br>**Permanent** unless otherwise noted. | **Level of Change:**<br>Major Change ☒<br>Minor Change ☐ | **Effective Date:**<br>**07/06/2015** |

**DESCRIPTION OF CHANGE/MODIFICATION**

| **From:** | **To:** |
|---|---|
| 10.0:<br>FCQFN/FCTQFN-2x2 | 11.0:<br>Change to: FCQFN/FCTQFN/FCUTQFN-2x2 |
| FCMQFN-2X2: MSL 1 | Change to: FCMQFN-2X2: MSL 3 |
| FCMQFN-2.5X3.0: MSL 1 | Change to: FCMQFN-2.5X3.0: MSL 3 |
| FCMQFN-3X5: MSL 1 | Change to: FCMQFN-3X5: MSL 3 |
| | New: FCMQFN-4X4 |
| FCMQFN-5X5: MSL 1 | Change to: FCMQFN-5X5: MSL 3 |
| | New: FCSOT563-6 |
| QFN/TQFN-2x2 | Change to: QFN/TQFN/UTQFN-2x2 |
| QFN/TQFN-3x3 | Change to: QFN/TQFN/UTQFN-3x3 |
| | New: QFN/TQFN-6x8 |
| TSOT23-5/6/8 | Change to: TSOT23-4/5/6/8 |

**REASON FOR CHANGE**

Update to show current standards and practices 更新以示当前标准及操作

**SIGNATURES REQUIRED FOR APPROVAL**

| TITLE/NAME | APPRV'D | REJECTED (Provide Reason) | * Date Signed |
|---|---|---|---|
| Originator:<br>Kevin Wan | X | APPROVED USING WORKFLOW | 07/02/15 |
| Dir., Package and Reliability:<br>Hunt Jiang | X | APPROVED USING WORKFLOW | 07/03/15 |
| Dir., Quality Assurance &<br>Information Systems<br>Henry Zhao | X | APPROVED USING WORKFLOW | 07/06/15 |
| Document Control:<br>Silvia Martinez | X | APPROVED USING WORKFLOW | 07/06/15 |

**OWNER**

| | Name | Department | Section | Notes |
|---|---|---|---|---|
| Owner | Hunt Jiang | Package Engineering | All | N/A |

**AFFECTED DEPARTMENTS**

| | | |
|---|---|---|
| ☒Application Engineering<br>☐Customer Service<br>☐Design<br>☐Failure Analysis<br>☐Finance<br>☐Foundry<br>☐HR | ☐IT<br>☐Logistics<br>☐Maintenance<br>☐Material<br>☒Package<br>☒Planning | ☒Product Engineering<br>☒Production<br>☒Quality<br>☐Safety and Security<br>☐Test Engineering<br>☐Other _____ |

**FOR DOCUMENT CONTROL USE ONLY**

*** Original signatures and dates are on file in Document Control**

## 1. PURPOSE 目的

1.1. The purpose of this specification is to define the Moisture Sensitivity Level (MSL) List for the lead free surface mount products.

本文件旨在为表面贴装无铅产品定义潮湿敏感度等级 (MSL)

## 2. SCOPE 范围

2.1. This specification applies to both MPS HQ and CD sites.

本文件适用于 MPS 总部和成都公司

## 3. RESPONSIBILITIES 职责

3.1. It is Package Engineering's responsibility to update the MSL List.

封装工程部负责更新 MSL 等级表

## 4. DEFINITIONS 定义

4.1. Moisture Sensitivity Level (MSL)

潮湿敏感等级

A rating indicating a component's susceptibility to damage due to absorbed moisture when subjected to reflow soldering. The MSL is expressed in numbers, with the MSL number increasing with the vulnerability of the package to popcorn cracking.

用来标示器件在回流焊时因吸收潮气而造成损伤的敏感度等级。MSL 用数字标示，随着数字增加，产品出现爆米花式破裂的可能性越高

4.2. Plastic Surface Mount Devices (PSMD)

塑封表面贴装原件

The families of components which are attached to the surface of printed circuit board by solder reflow, rather than inserting through holes in the board, such as MSOP, QFN, SOIC, TSOT, TSSOP, etc.

该系列器件是通过回流焊的方式焊接在印刷电路板表面的，而不是插入电路板的通孔，例如 MSOP, QFN, SOIC, TSOT, TSSOP 等

**ATTACHMENT 1**

## MPS - MSL Level for Lead Free Products (260ºC max)

| Package Type | Lead Finish | MSL Level |
|---|---|---|
| FCQFN/FCTQFN-1.0x1.5 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-1.4x1.8 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-1.5X2.0 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-2.2X2.6 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-2.5X3.0 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN/FCUTQFN-2x2 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-2x3 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN/FCUTQFN-3x3 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-3x4 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-3x5 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-4x4 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-4x5 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-4x6 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-5x4 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-5x5 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-5x6 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-5x8 | 100% Matte Sn | 1 |
| FCQFN/FCTQFN-6x6 | 100% Matte Sn | 1 |
| FCMQFN-2X2 | 100% Matte Sn | 3 |
| FCMQFN-2.5X3.0 | 100% Matte Sn | 3 |
| FCMQFN-3X5 | 100% Matte Sn | 3 |
| FCMQFN-4X4 | 100% Matte Sn | 3 |

| Package Type | Lead Finish | MSL Level |
|---|---|---|
| FCMQFN-5X5 | 100% Matte Sn | 3 |
| FCSOIC-8/16 | 100% Matte Sn | 1 |
| FCSOT563-6 | 100% Matte Sn | 1 |
| FCTSOT23-5/6/8 | 100% Matte Sn | 1 |
| MPMQFN-12X12 | 100% Matte Sn | 3 |
| MPMQFN-12X15 | 100% Matte Sn | 3 |
| MPMQFN-15X15 | 100% Matte Sn | 3 |
| MSOP-8/10 | 100% Matte Sn | 1 |
| MSOP-8/10-EP | 100% Matte Sn | 2 |
| PDIP-7/8/16 | 100% Matte Sn | N/A |
| PDIP-8-EP | 100% Matte Sn | N/A |
| UTQFN-1.6x1.2 | NiPdAu | 1 |
| QFN/TQFN/UTQFN-2x2 | 100% Matte Sn | 1 |
| QFN/TQFN-2x3 | 100% Matte Sn | 1 |
| QFN/TQFN-3X2 | 100% Matte Sn | 1 |
| QFN/TQFN/UTQFN-3x3 | 100% Matte Sn | 1 |
| QFN/TQFN-3x4 | 100% Matte Sn | 1 |
| QFN/TQFN-3x5 | 100% Matte Sn | 1 |
| QFN/TQFN-3.5x3.5 | 100% Matte Sn | 1 |
| QFN/TQFN-4x4 | 100% Matte Sn | 1 |
| QFN/TQFN-4x5 | 100% Matte Sn | 2 |
| QFN/TQFN-4x6 | 100% Matte Sn | 2 |
| QFN/TQFN-5x5 | 100% Matte Sn | 2 |
| QFN/TQFN-5x6 | 100% Matte Sn | 2 |
| QFN/TQFN-6x6 | 100% Matte Sn | 2 |

| Package Type | Lead Finish | MSL Level |
|---|---|---|
| QFN/TQFN-6x8 | 100% Matte Sn | 2 |
| QFN/TQFN-7x7 | 100% Matte Sn | 2 |
| QFN/TQFN-8x8 | 100% Matte Sn | 3 |
| QFP/TQFP-7X7 | 100% Matte Sn | 3 |
| SC70 | 100% Matte Sn | 1 |
| SOD123 | 100% Matte Sn | 1 |
| SOICN-7/8/14/16 | 100% Matte Sn | 2 |
| SOICN-8/16-EP | 100% Matte Sn | 2a |
| SOICW-18/20/24/28 | 100% Matte Sn | 3 |
| SOT23-3/5/6 | 100% Matte Sn | 1 |
| TO220 | 100% Matte Sn | N/A |
| TO252 | 100% Matte Sn | 3 |
| TO263 | 100% Matte Sn | 3 |
| TSOT23-4/5/6/8 | 100% Matte Sn | 1 |
| TSSOP-8/14/16/20/24/28 | 100% Matte Sn | 2 |
| TSSOP-16/20/28-EP | 100% Matte Sn | 2a |
| WLCSP | NA | 1 |

**ATTACHMENT 2**

## MSL Level List for Special Part

| Package Type | Package Type | Lead Finish | MSL Level |
|---|---|---|---|
| HF81GS | SOIC-8 | 100% Matte Sn | 1 |
| MP18030GQN | QFN7X7-28 | 100% Matte Sn | 3 |
| MP1930GQN | QFN7X7-28 | 100% Matte Sn | 3 |
| MP2910ES | SOIC-14 | 100% Matte Sn | 3 |
| MP2930GQK | QFN6X6-40 | 100% Matte Sn | 3 |
| MP2933DQN | QFN7X7-56 | 100% Matte Sn | 3 |
| MP2935DQK | QFN6X6-40 | 100% Matte Sn | 3 |
| MP2936DQK | QFN6X6-40 | 100% Matte Sn | 3 |
| MP2938GQK | QFN6X6-48 | 100% Matte Sn | 3 |
| MP2953GU | QFN5X5-40 | 100% Matte Sn | 3 |
| MP3394EY | SOIC-20 | 100% Matte Sn | 3 |
| MP6911DU | QFN5X5-32 | 100% Matte Sn | 3 |
| MP8049DQK | QFN6X6-40 | 100% Matte Sn | 3 |
| MP8619EQJ | QFN5X6-30 | 100% Matte Sn | 3 |
| MPQ5680GQN | QFN7X7-48 | 100% Matte Sn | 3 |
| NB648DQJ | QFN5X6-30 | 100% Matte Sn | 3 |
| NB649EQJ | QFN5X6-30 | 100% Matte Sn | 3 |
| NB658EQJ | QFN5X6-30 | 100% Matte Sn | 3 |
| HF500GS-15 | SOIC8-7 | 100% Matte Sn | 3 |
| HF500GS-7 | SOIC8-7 | 100% Matte Sn | 3 |
| MP023GS-10 | SOIC8-7 | 100% Matte Sn | 3 |
| MP4029-15GS | SOIC8-7 | 100% Matte Sn | 3 |

| Package Type | Package Type | Lead Finish | MSL Level |
|---|---|---|---|
| MP4053-15GS | SOIC8-7 | 100% Matte Sn | 3 |
| MP4053-7GS | SOIC8-7 | 100% Matte Sn | 3 |
| MP8619EQJ-S-LF | QFN5X6-30 | 100% Matte Sn | 3 |
| NB648EQJ-S-LF | QFN5X6-30 | 100% Matte Sn | 3 |
| NB649EQJ-S-LF | QFN5X6-30 | 100% Matte Sn | 3 |
| MP6914DN-LF | SOIC8-EP | 100% Matte Sn | 3 |

**REVISION HISTORY**

| REV | ECN | DATE | DESCRIPTION OF CHANGE | ORIGINATOR |
|---|---|---|---|---|
| 0.0 | S-03723 | 02/26/08 | Initial release<br>首次发行 | Kevin Wan |
| 1.0 | S-04200 | 05/03/10 | Complete re-write<br>完全重写 | Kevin Wan |
| 2.0 | S-04677 | 04/23/12 | add MSL information for FCQFN1.0x1.5, FCQFN1.4x1.8, FCQNF1.5x2.0, FCQFN2x2, FCQFN2x3, FCQFN/UTQFN3x3, FCQFN3x5, FCQFN5x4, FCQFN5x6, FCQFN5x8, FCSOIC8, FCSOIC16,FCTSOT5/6/8, PDIP8EP, UTQFN1.6x1.2, UTQFN2x2, UTQFN3x3, QFN3.5x3.5, QFN5x8, SOICN8-7, SOICN14, SOICW18, TO220-5, TO263-5, TSOT23-8, TSSOP24 and TSSOP28EP.<br>2.0 新增 FCQFN1.0x1.5, FCQFN1.4x1.8, FCQNF1.5x2.0, FCQFN2x2, FCQFN2x3, FCQFN/UTQFN3x3, FCQFN3x5, FCQFN5x4, FCQFN5x6, FCQFN5x8, FCSOIC8, FCSOIC16,FCTSOT5/6/8, PDIP8EP, UTQFN1.6x1.2, UTQFN2x2, UTQFN3x3, QFN3.5x3.5, QFN5x8, SOICN8-7, SOICN14, SOICW18, TO220-5, TO263-5, TSOT23-8, TSSOP24 and TSSOP28EP MSL 信息 | Kevin Wan |
| 3.0 | S-04841 | 09/16/12 | Update 1.1 to "…lead free surface mount products." And add "Definitions" section to Cover Sheet. Add MSL information for FCQFN2.5x3.0, FCQFN4X4, FCTQFN4x5, FCQFN4x6, PDIP8-7A, PDIP8-7B, SOIC8-7A and SOIC8-7B. Remove N from SOICN-8, SOICN-8-7A, SOICN-8-EP, SOICN-14 and SOICN-16. Remove W from SOICW-18, SOICW-20, SOICW-24 and SOICW-28.<br>3.0: 更新 1.1 为"…lead free surface mount products."新增"Definitions"部分；新增 FCQFN2.5x3.0、FCQFN4X4、FCTQFN4x5、FCQFN4x6、PDIP8-7A、PDIP8-7B、SOIC8-7A 及 SOIC8-7B 的 MSL 信息. 将 N 从 SOICN-8、SOICN-8-7A、SOICN-8-EP、SOICN-14 及 SOICN-16 中移除. 将 W 从 SOICW-18、SOICW-20、SOICW-24 及 SOICW-28 中移除。 | Kevin Wan |

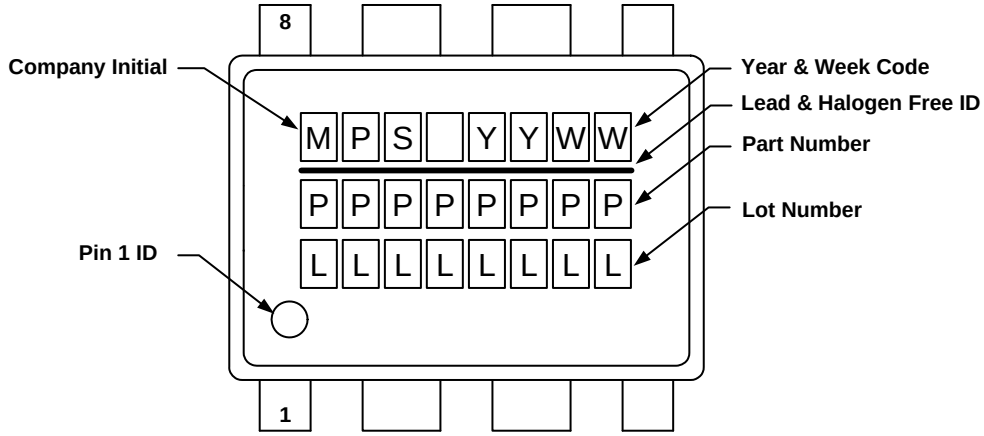
| | | | | |
|---|---|---|---|---|
| 4.0 | S-04962 | 03/06/13 | Change the MSL level of FCQFN/FCTQFN-4x5, FCQFN-<br>4X6, FCQFN-5X4, FCQFN/FCTQFN-5x5, FCQFN/FCTQFN-5x6, FCQFN-5X8, FCQFN/FCTQFN-<br>6x6, FCSOIC-8 and FCSOIC-16 to level 2.<br>FCQFN/FCTQFN-4x5, FCQFN-4X6, FCQFN-5X4,<br>FCQFN/FCTQFN-5x5, FCQFN/FCTQFN-5x6, FCQFN-<br>5X8, FCQFN/FCTQFN-6x6, FCSOIC-8 和 FCSOIC-16 的<br>MSL 等级修改为 2 – **REJECTED.** | Tony Tang |
| 5.0 | S-04971 | 03/12/13 | Change the MSL level of FCQFN/FCTQFN-4x5, FCQFN-4X6, FCQFN-5X4, FCQFN/FCTQFN-5x5, FCQFN/FCTQFN-5x6, FCQFN-5X8, FCQFN/FCTQFN-6x6, FCSOIC-8 and FCSOIC-16 to level 2.<br>Take away the FC prefix for the package type of FCQFN-1.0X1.5, FCQFN-1.4X1.8, FCQFN-1.5X2.0, FCQFN -2.5X3, FCQFN-3X5, FCQFN-4X6, FCQFN-5X4, FCQFN-5X8, FCSOIC-8, FCSOIC16 and FCTSOT-5/6/8.<br>FCQFN/FCTQFN-4x5, FCQFN-4X6, FCQFN-5X4, FCQFN/FCTQFN-5x5, FCQFN/FCTQFN-5x6, FCQFN-5X8, FCQFN/FCTQFN-6x6, FCSOIC-8 和 FCSOIC-16 的 MSL 等级修改为 2.<br>FCQFN-1.0X1.5, FCQFN-1.4X1.8, FCQFN-1.5X2.0, FCQFN -2.5X3, FCQFN-3X5, FCQFN-4X6, FCQFN-5X4, FCQFN-5X8, FCSOIC-8, FCSOIC16 and FCTSOT-5/6/8 的 package 名称去掉前缀 FC – **REJECTED.** | Tony Tang |
| 6.0 | S-04973 | 03/18/13 | Change QFN/TQFN 4x5, 4x6 and 5x4 to be level 1.<br>QFN/TQFN 4x5, 4x6 和 5x4 的 MSL 等级修改为 1. | Tony Tang |

| | | | | |
|---|---|---|---|---|
| 7.0 | S-05209 | 12/03/13 | Change title to Moisture Sensitivity Level List; Change QFN/TQFN-8x8, TO263 to be level 3; Add MSL information for FCQFN, MODULE and TO252; Add attachment 2 MSL level for special part.<br>标题改为潮湿敏感度等级表；QFN8X8, TO263 的 MSL 等级修改为 3，增加 FLIP CHIP,MODULE 和 TO252 的 MSL 等级;增加附件 2 特殊产品的 MSL level.<br>**REJECTED** | Kevin Wan |
| 8.0 | S-05214 | 12/10/13 | Change Package Type of MP2930GQK, MP2935DQK, MP2936DQK from QFN6X6-48 to QFN6x6-40 in ATTACHMENT2, add MPMQFN-15X15 to ATTACHMENT1, add MP8049DQK to ATTACHMETN2. | Jenny Wu |
| 9.0 | S-04391 | 06/20/14 | Change MSL 2A to 2a; remove MP2932GQK from special part list.<br>把 MSL 等级的 2A 改为 2a;把 MP2932GQK 从特别产品列表里移除。 | Kevin Wan |
| 10.0 | S-05526 | 11/09/14 | Add MSL information for FCQFN-2.5X3.0, FCMQFN-2X2, MPMQFN-12X12 and QFP/TQFP-7X7; change the Lead Finish for UTQFN-1.6X1.2 to NiPdAu.<br>Add HF500GS-15, HF500GS-7, MP023-10, MP4029-15GS, MP4053-15GS, MP4053-7GS, MP8619EQJ-S-LF, NB648EQJ-S-LF, NB649EQJ-S-LF and MP6914DN-LF to special part list.<br>增加 FCQFN-2.5X3.0, FCMQFN-2X2, MPMQFN-12X12, QFP/TQFP-7X7 的 MSL 信息; 把 HF500GS-15, HF500GS-7, MP023-10, MP4029-15GS, MP4053-15GS, MP4053-7GS, MP8619EQJ-S-LF, NB648EQJ-S-LF, NB649EQJ-S-LF, MP6914DN-LF 加入特别产品列表里。 | Kevin Wan |

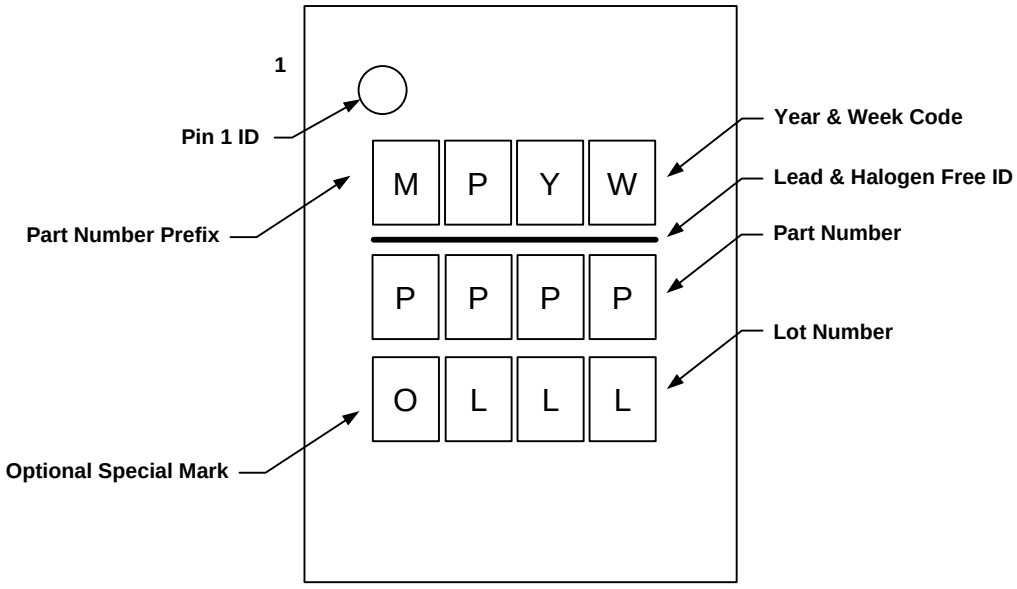
| | | | | |
|---|---|---|---|---|
| 11.0 | S-05762 | 06/30/15 | Change to: FCQFN/FCTQFN/FCUTQFN-2x2; Change to: FCMQFN-2X2: MSL 3; Change to: FCMQFN-2.5X3.0: MSL 3; Change to: FCMQFN-3X5: MSL 3; New: FCMQFN-4X4; Change to: FCMQFN-5X5: MSL 3; New: FCSOT563-6; Change to: QFN/TQFN/UTQFN-2x2; Change to: QFN/TQFN/UTQFN-3x3; New: QFN/TQFN-6x8; Change to: TSOT23-4/5/6/8 | Kevin Wan |

# MARKING LAYOUT EXAMPLE

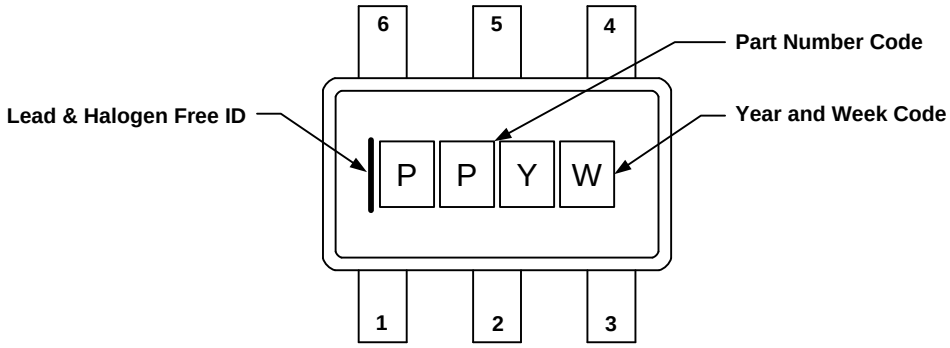
## TOP MARKING EXAMPLE 1:




## TOP MARKING EXAMPLE 2:




## TOP MARKING EXAMPLE 3:



## YEAR, WEEK AND COUNTRY CODE DEFINATION

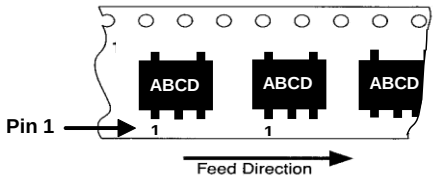
| SINGLE DIGIT YEAR (Y) DEFINITION | | SINGLE DIGIT WORK WEEK (W) DEFINITION | | SOT23/SOT23 COUNTRY OF ORIGIN | |
|---|---|---|---|---|---|
| 0 | 2000 | A | 1 – 4 | C | China |
| 1 | 2001 | B | 5 – 8 | M | Malaysia |
| 2 | 2002 | C | 9 – 12 | T | Thailand |
| 3 | 2003 | D | 13 – 16 | | |
| 4 | 2004 | E | 17 – 20 | | |
| 5 | 2005 | F | 21 – 24 | | |
| 6 | 2006 | G | 25 – 28 | | |
| 7 | 2007 | H | 29 – 32 | | |
| 8 | 2008 | J | 33 – 36 | | |
| 9 | 2009 | K | 37 – 40 | | |
| A | 2010 | M | 41 – 44 | | |
| B | 2011 | N | 45 – 48 | | |
| C | 2012 | P | 49 – 53 | | |
| D | 2013 | | | | |
| E | 2014 | | | | |
| F | 2015 | | | | |
| G | 2016 | | | | |
| H | 2017 | | | | |
| J | 2018 | | | | |
| K | 2019 | | | | |
| M | 2020 | | | | |
| N | 2021 | | | | |
| P | 2022 | | | | |
| R | 2023 | | | | |
| S | 2024 | | | | |
| T | 2025 | | | | |
| V | 2026 | | | | |
| W | 2027 | | | | |
| X | 2028 | | | | |
| Y | 2029 | | | | |
| Z | 2030 | | | | |

## 1. Table of Standard Tape and Reel Configurations
## 标准编带卷盘封装规范

| Part Number<br>产品号 | Package Description 封装 | Quantity /Reel<br>每盘数量 | Quantity /Rail*<br> | Reel Diameter<br>卷盘直径 | Carrier Tape Width<br>载带宽度 | Carrier Tape Pitch<br>载带线距 |
|---|---|---|---|---|---|---|
| MP####xJ-Z | TSOT23-5/6/8 | 3000 | N/A | 7 in. | 8 mm | 4 mm |

**Pin 1 Orientation by Package Type**

- **SOT23, TSOT23 & SC70 Packages**



# MPS Recommended IR Reflow Temperature Profile

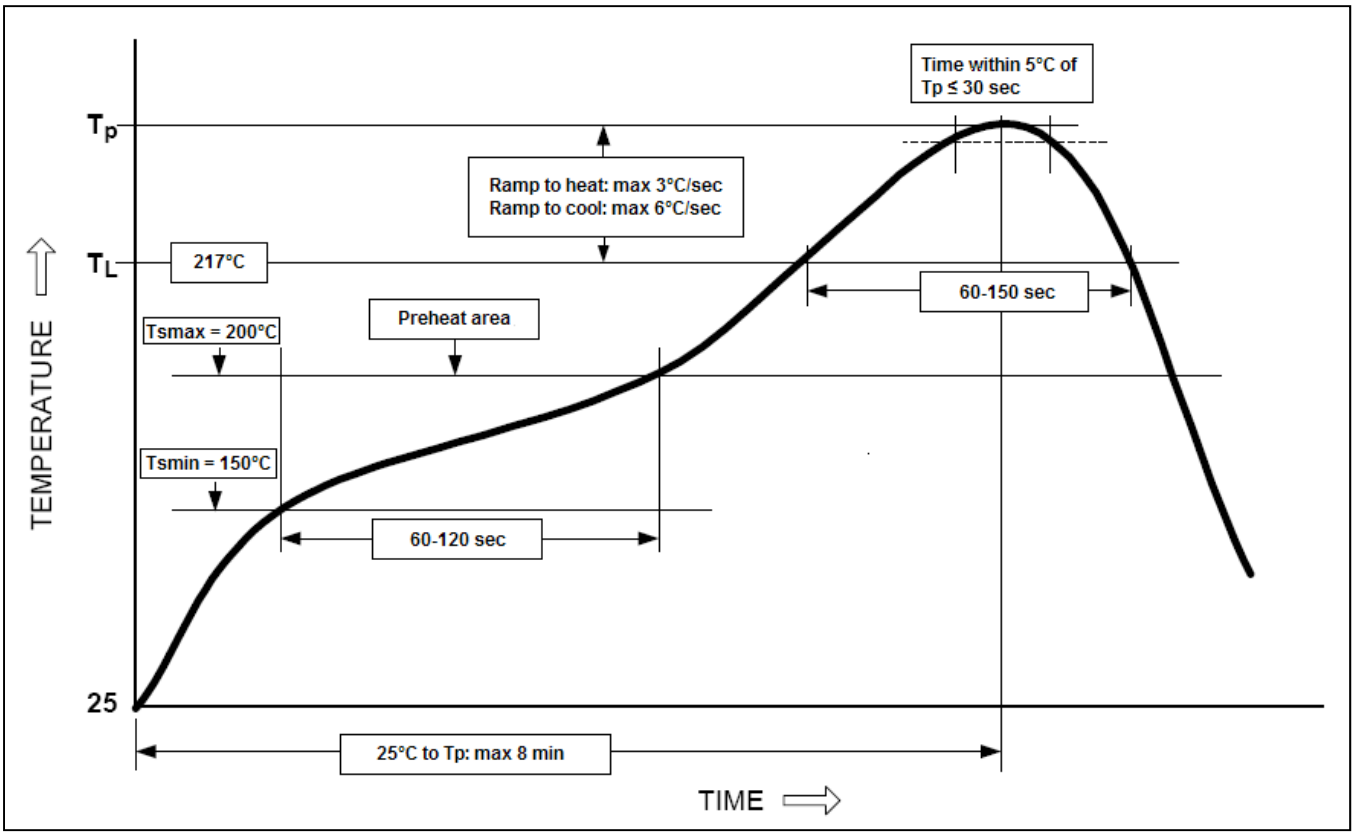



**Table: $T_P$ for Pb-Free Process**

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350 - 2000 | Volume $mm^3$ >2000 |
|---|---|---|---|
| <1.6 mm | ≤ 260°C | ≤ 260°C | ≤ 260°C |
| 1.6 mm - 2.5 mm | ≤ 260°C | ≤ 250°C | ≤ 245°C |
| >2.5 mm | ≤ 250°C | ≤ 245°C | ≤ 245°C |

The profile meets IPC/JEDEC J-STD-020 spec.