

PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

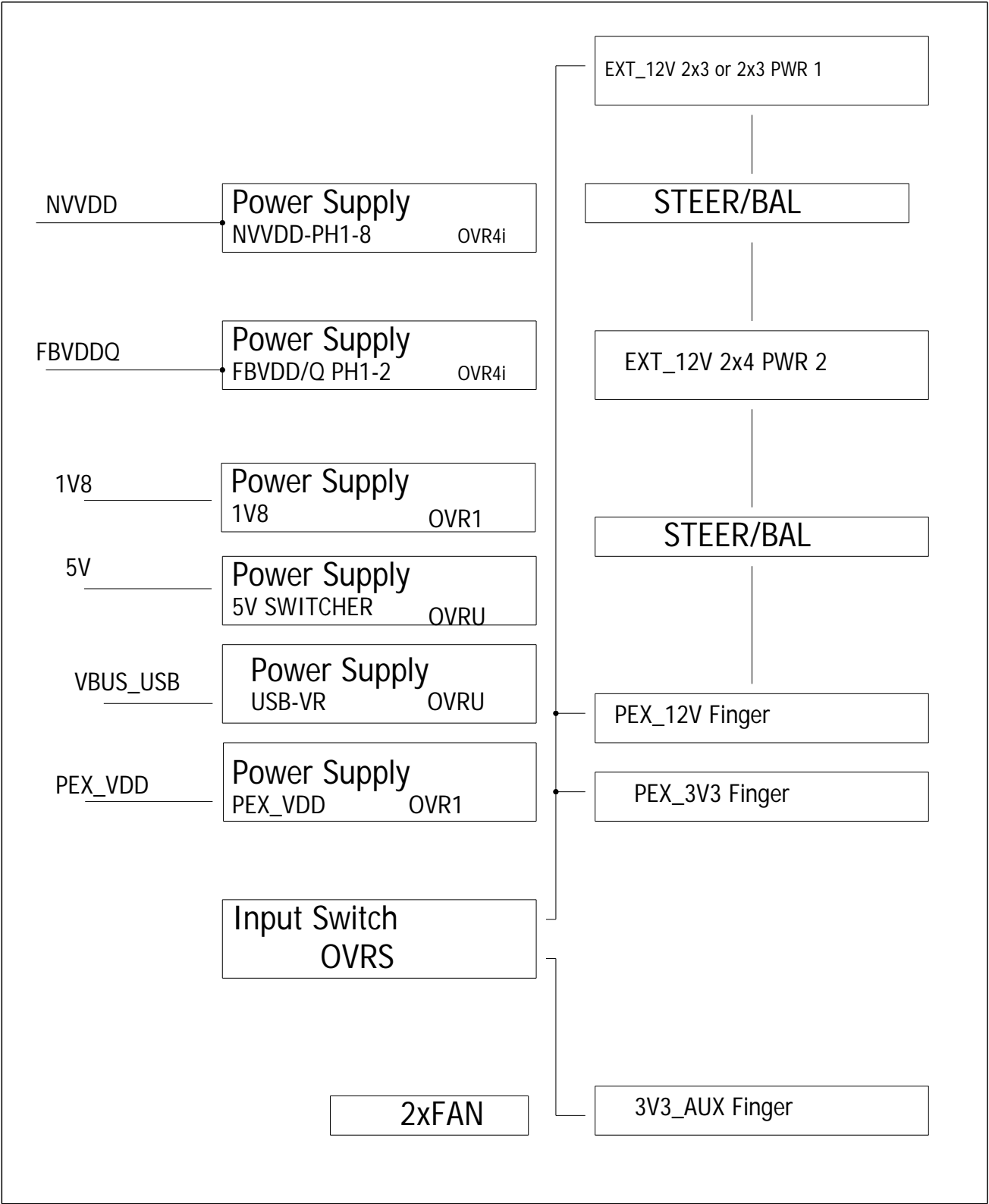
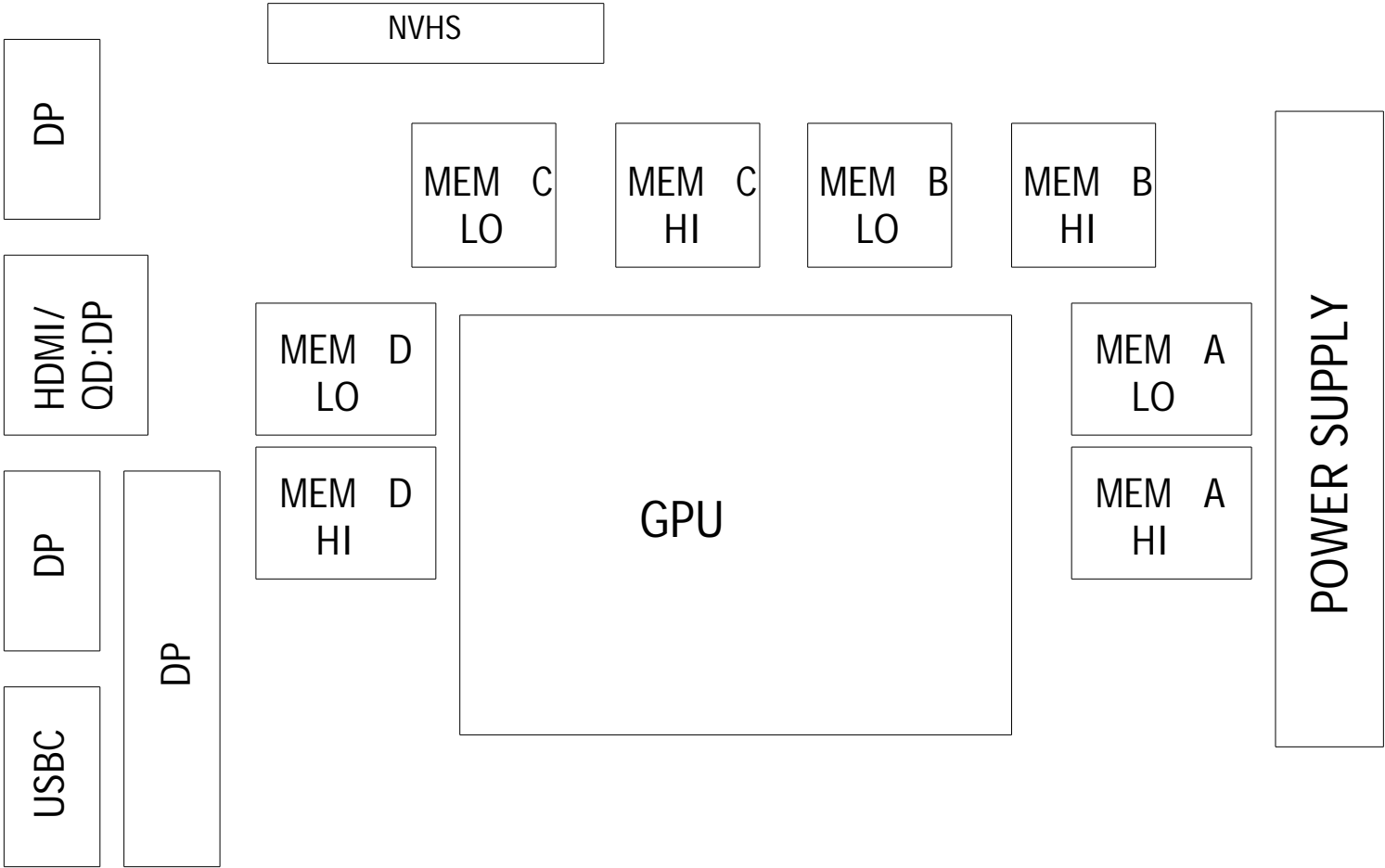
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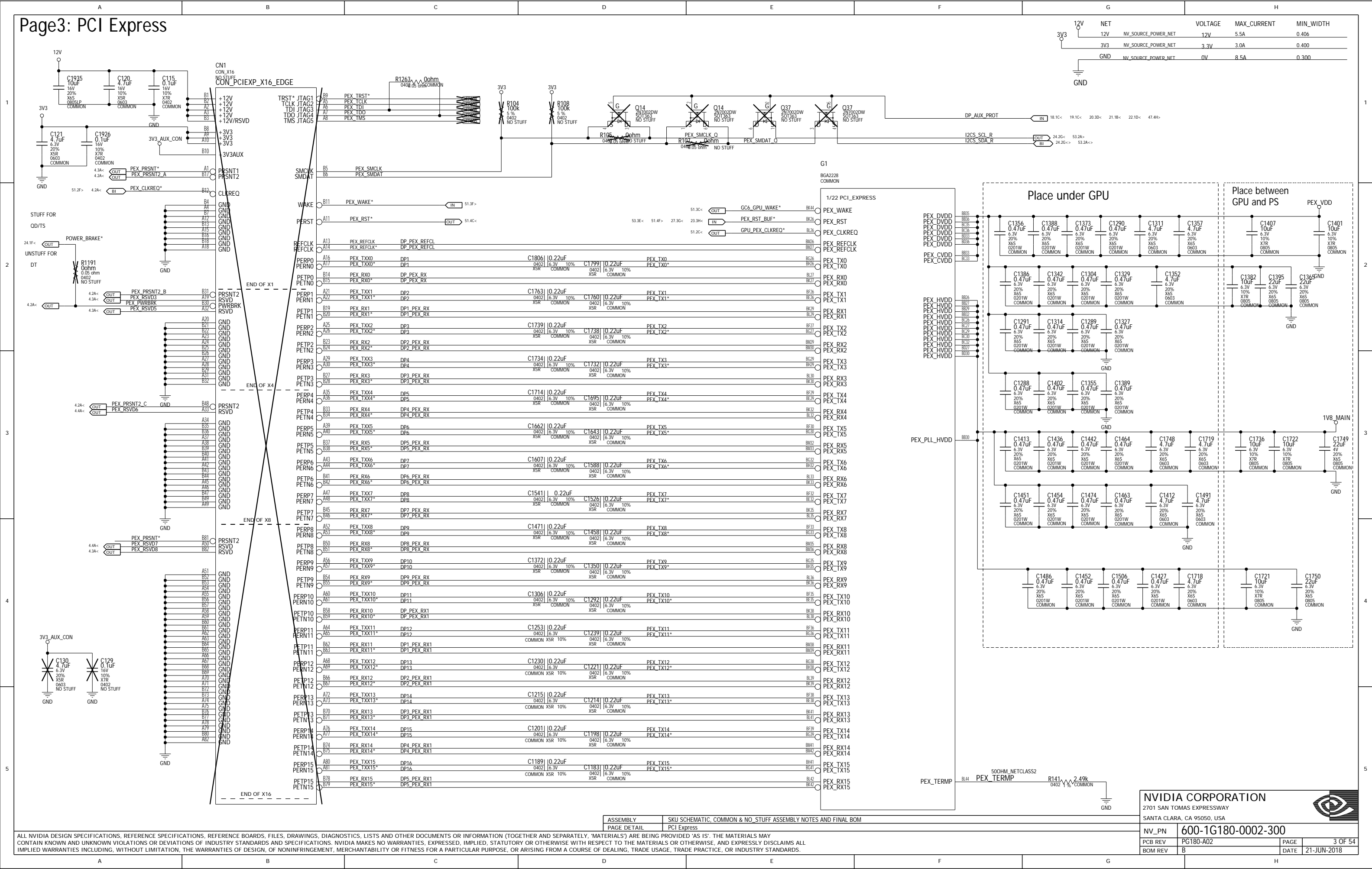
Page2: Block Diagram



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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	Block Diagram

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
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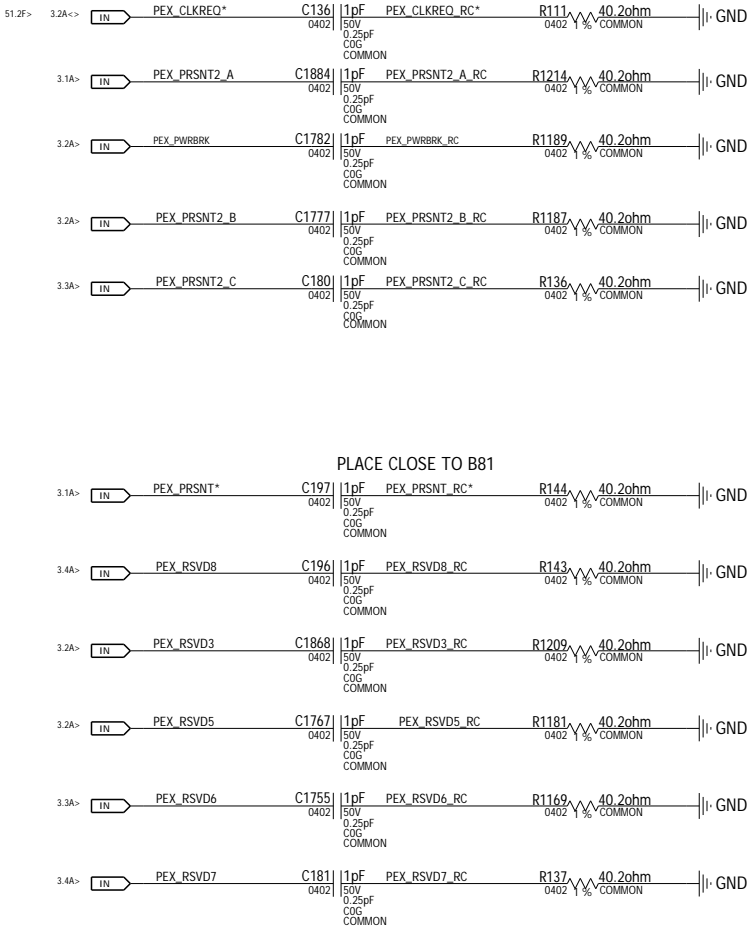
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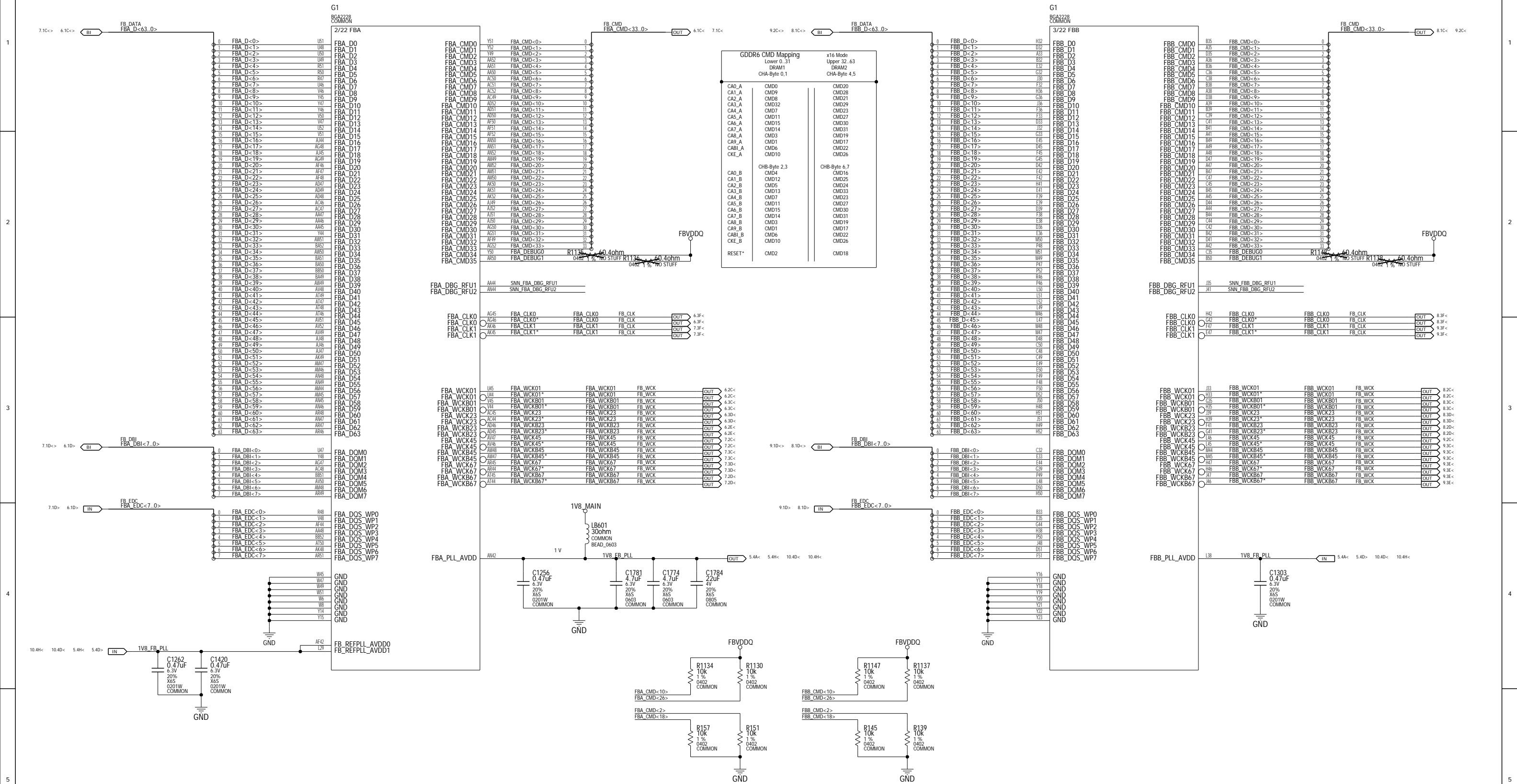
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Page4: PCI Termination



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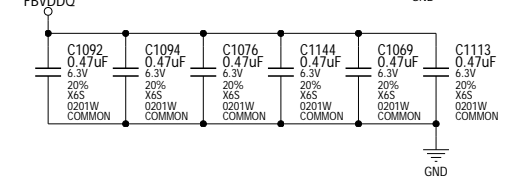
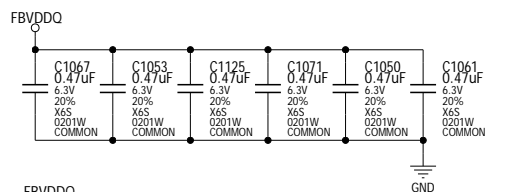
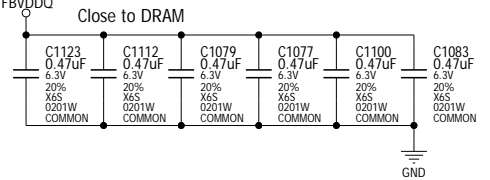
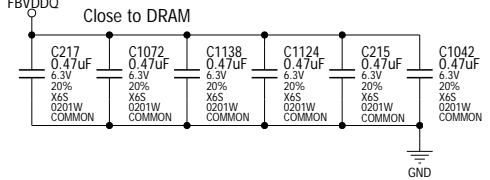
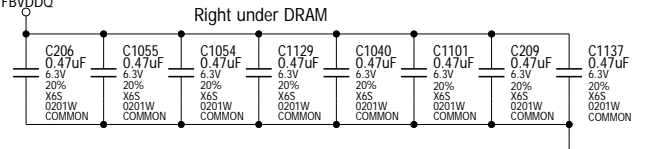
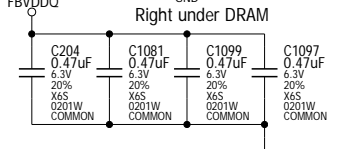
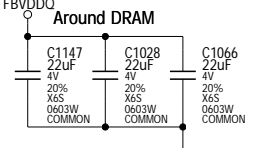
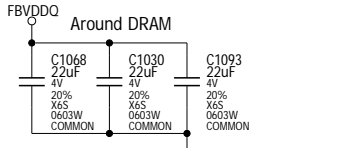
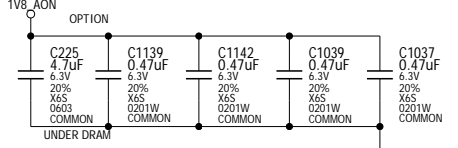
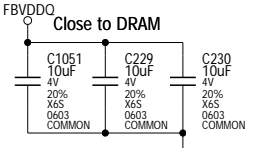
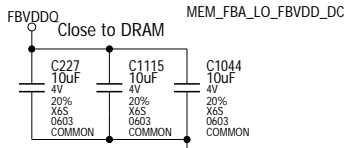
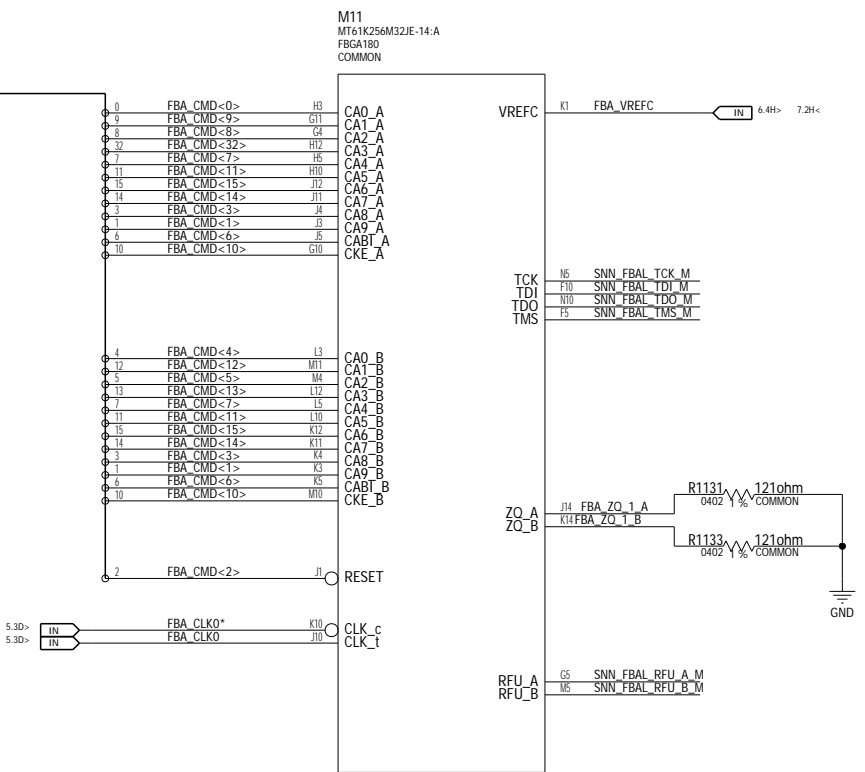
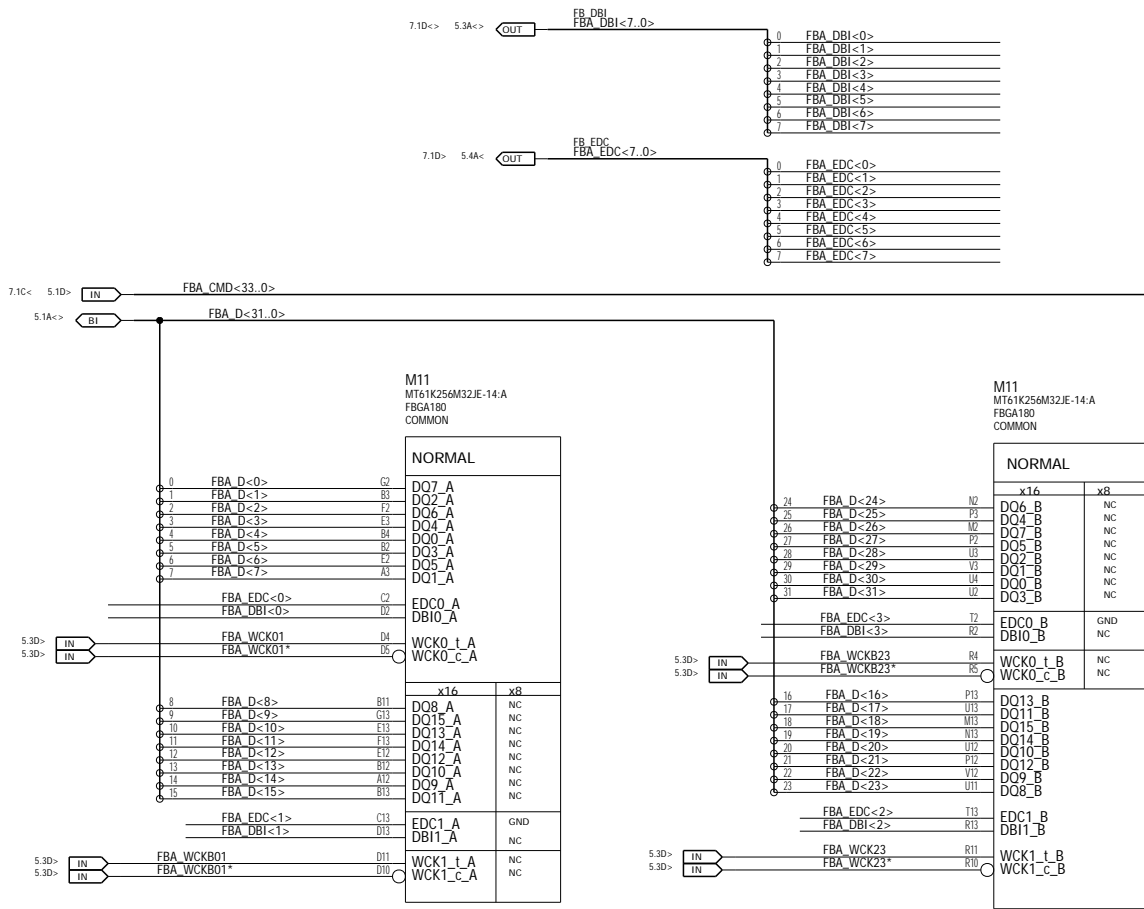
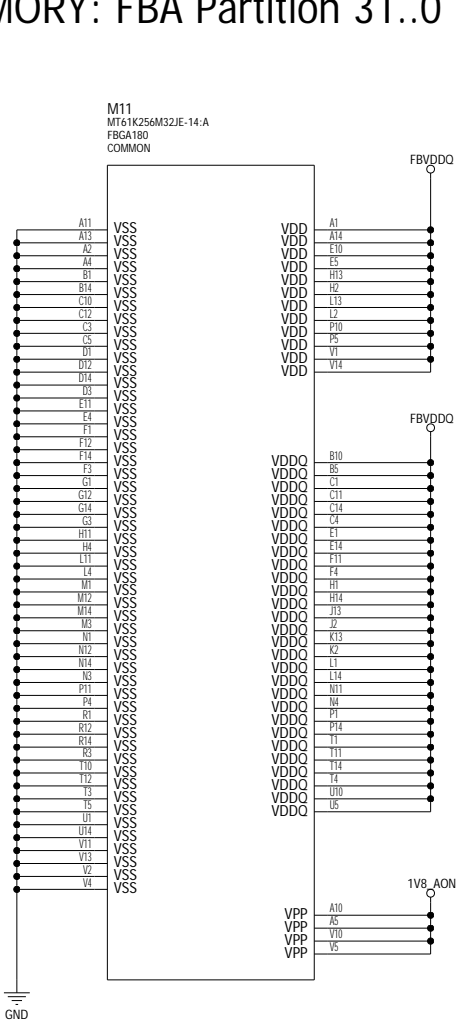
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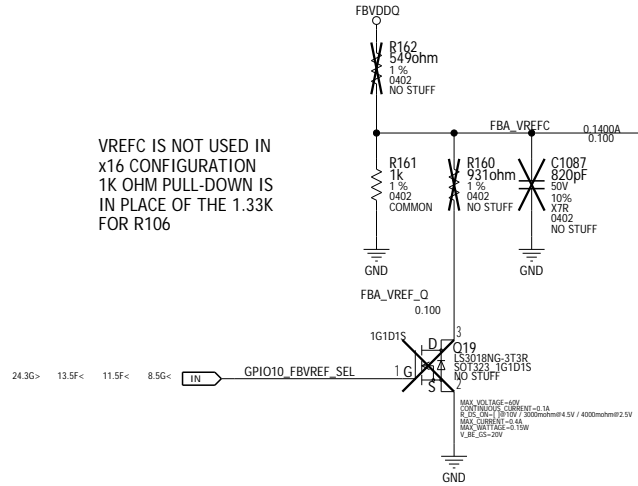
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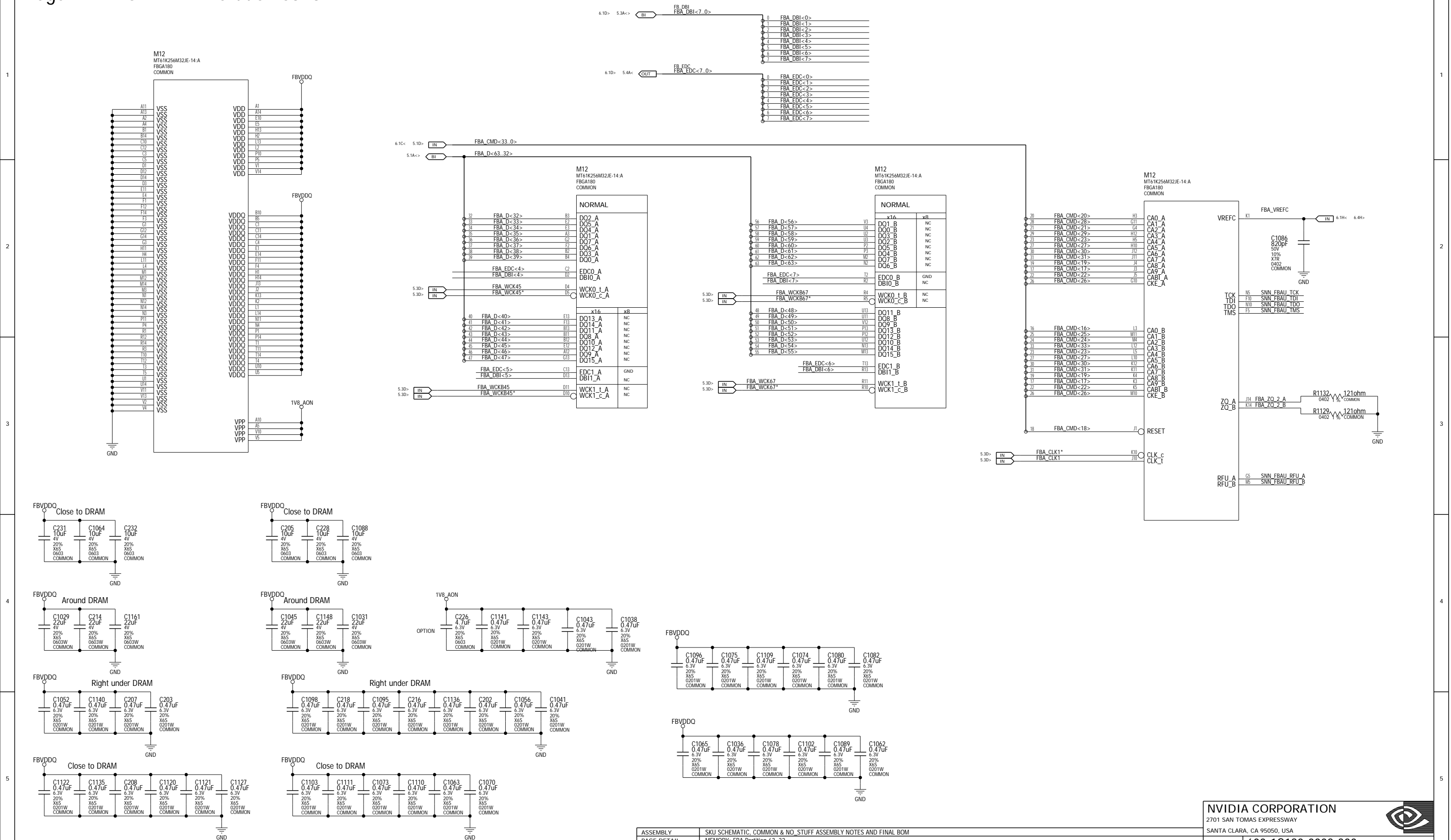
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VREFC IS NOT USED IN x16 CONFIGURATION 1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R106




Page7: MEMORY: FBA Partition 63..32

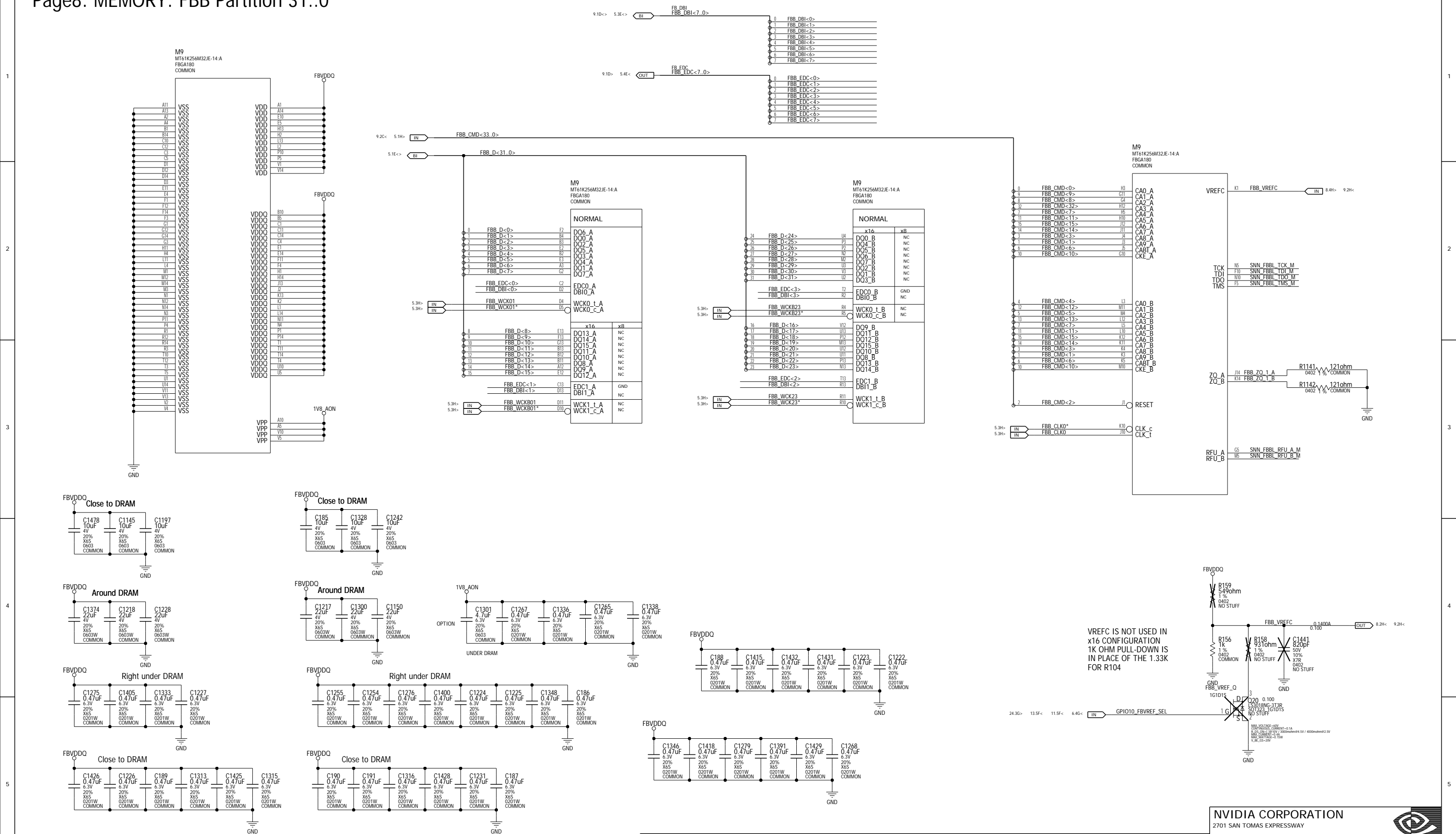


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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	MEMORY: FBA Partition 63..32

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Nv_PN PCB REV BOM REV	600-1G180-0002-300 PG180-A02 B	PAGE DATE	7 OF 54 21-JUN-2018

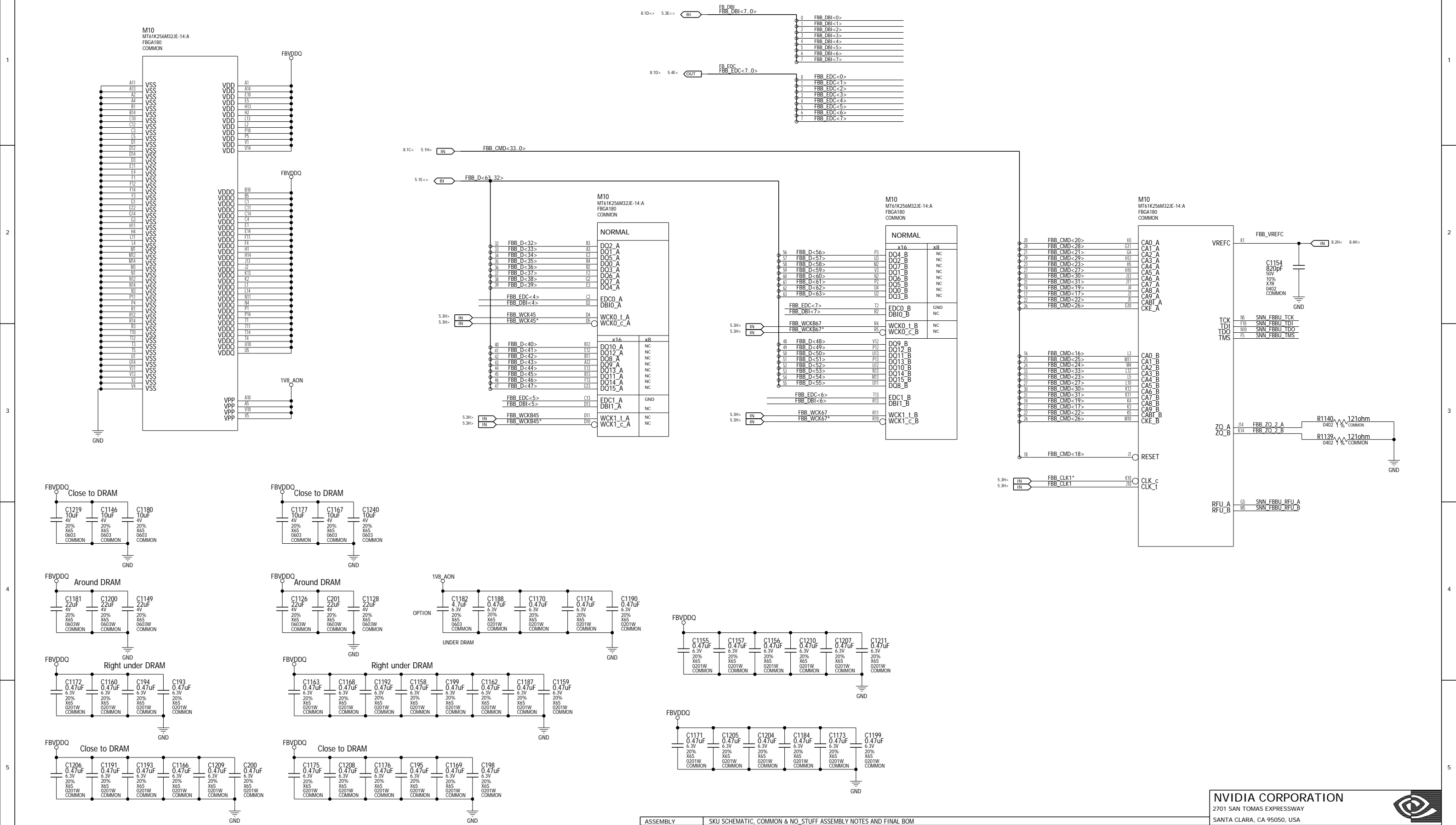
Page8: MEMORY: FBB Partition 31..0



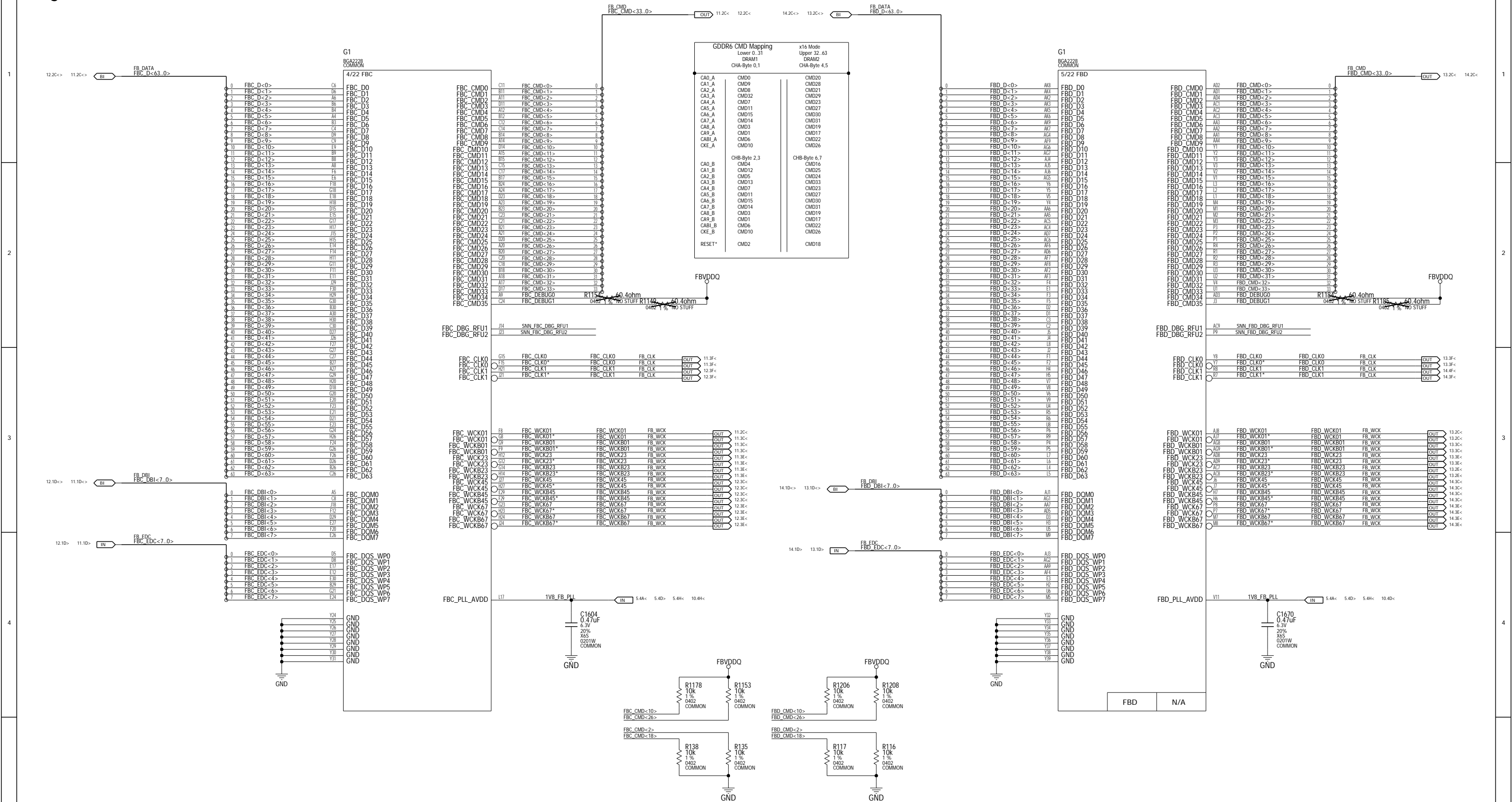
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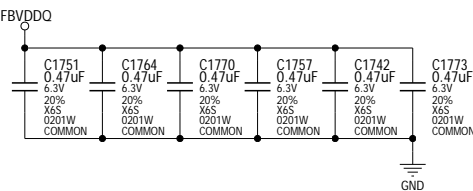
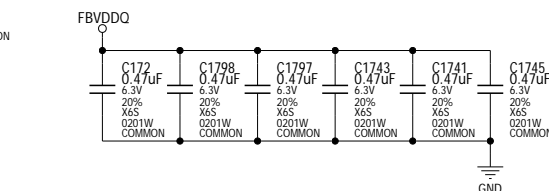
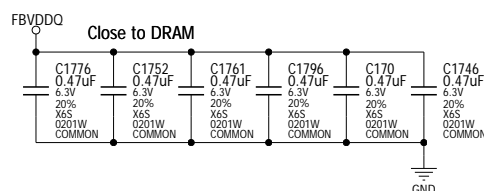
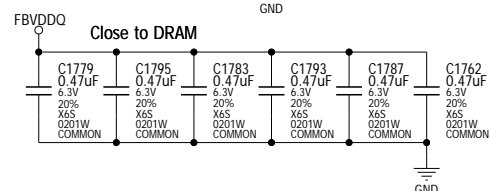
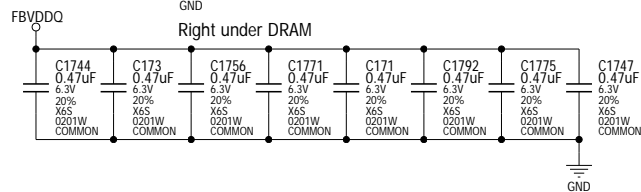
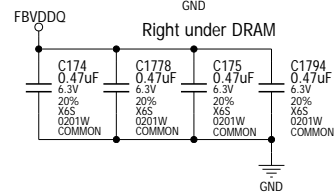
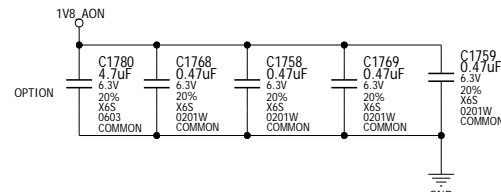
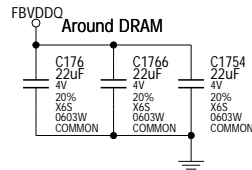
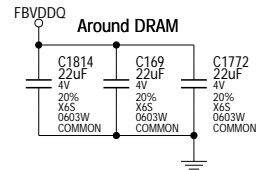
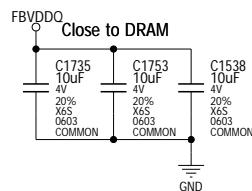
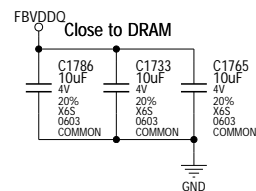
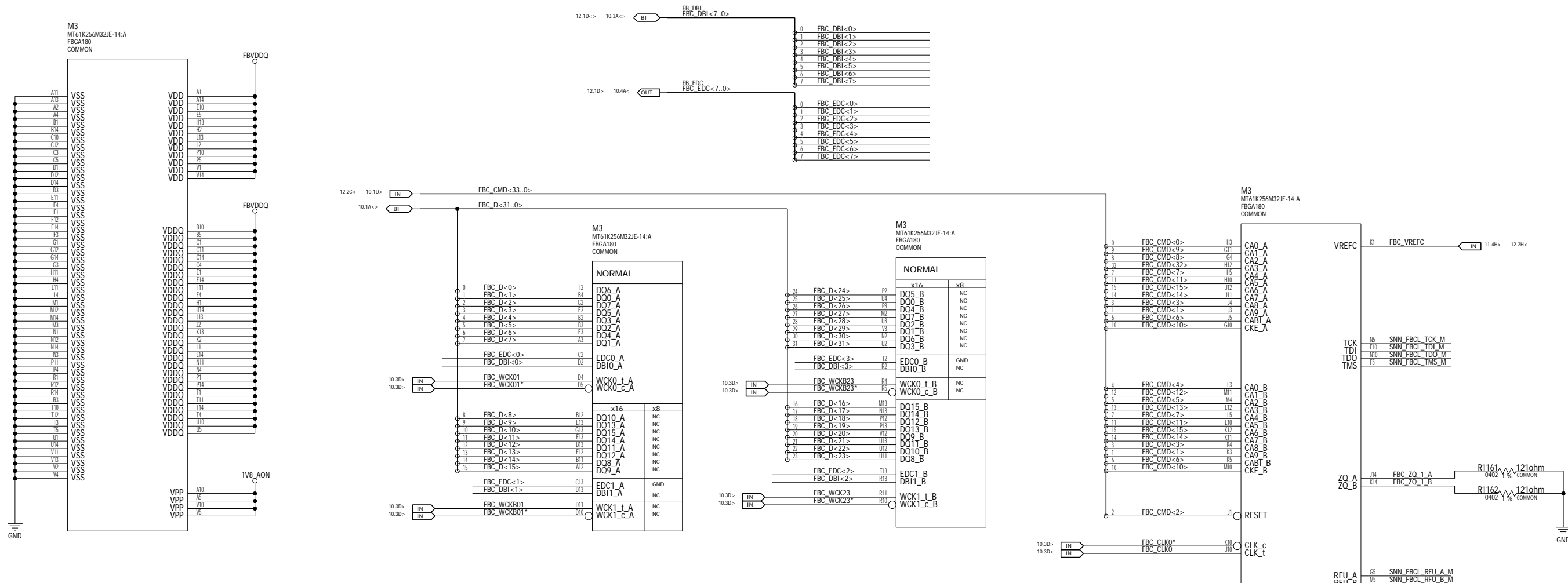
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PAGE DETAIL	MEMORY: FBB Partition 31..0

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN PCB REV BOM REV	600-1G180-0002-300 PG180-A02 B		PAGE DATE 8 OF 54 21-JUN-2018

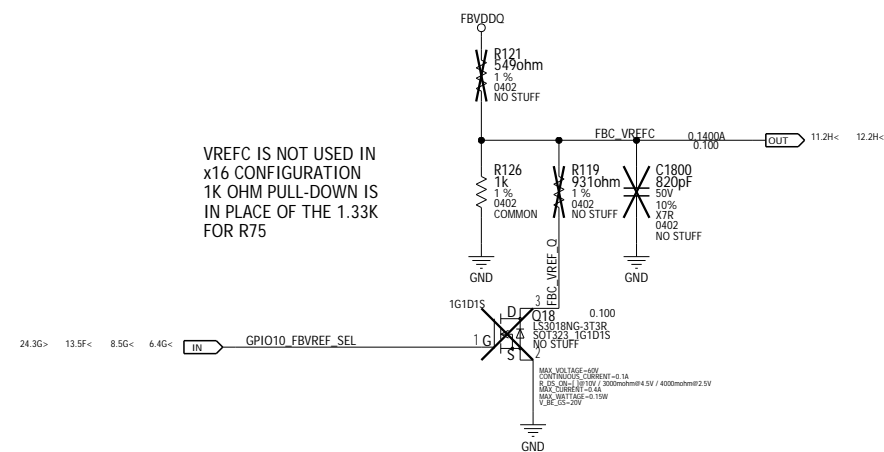


Page10: MEMORY: GPU Partition C/D





VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R75



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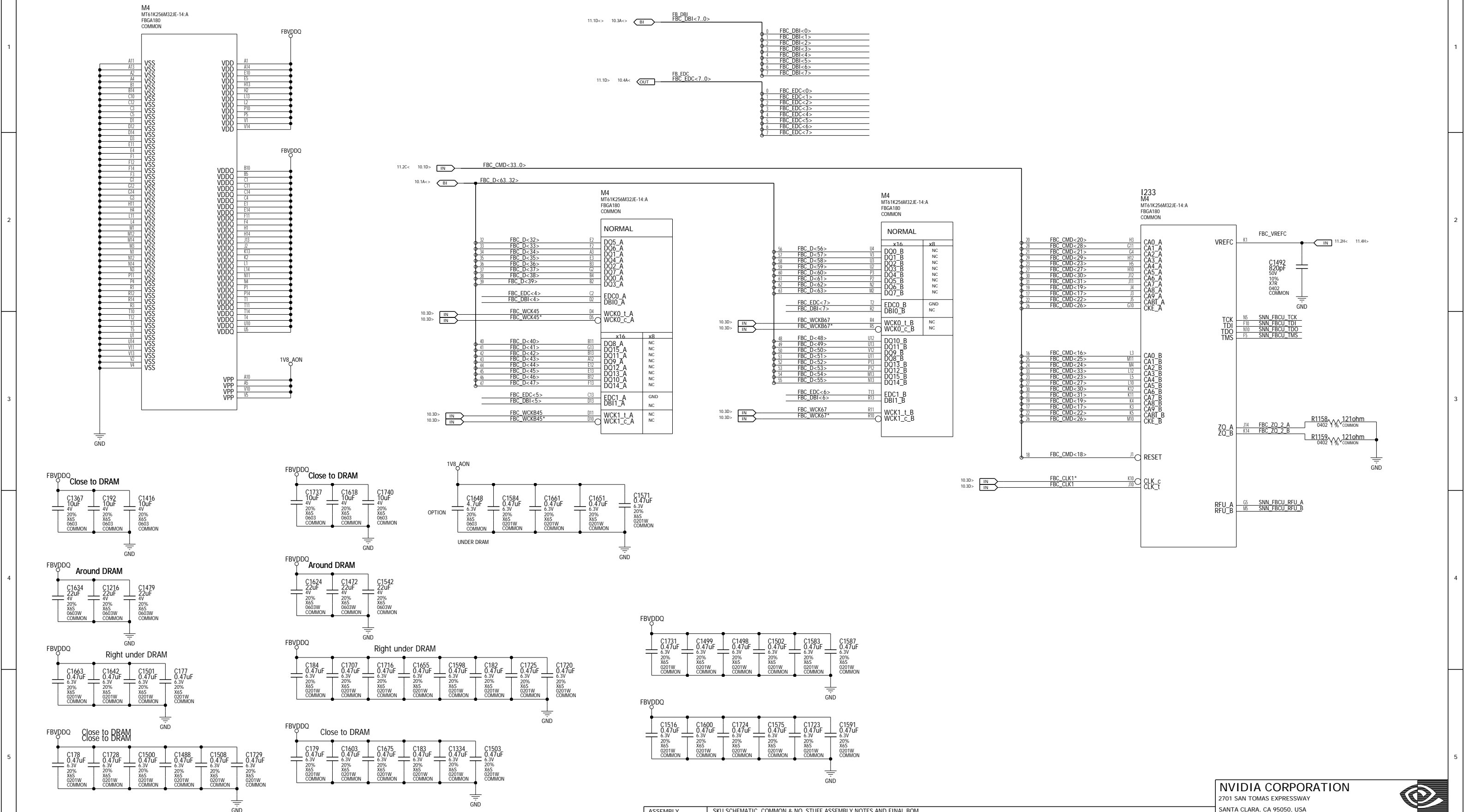
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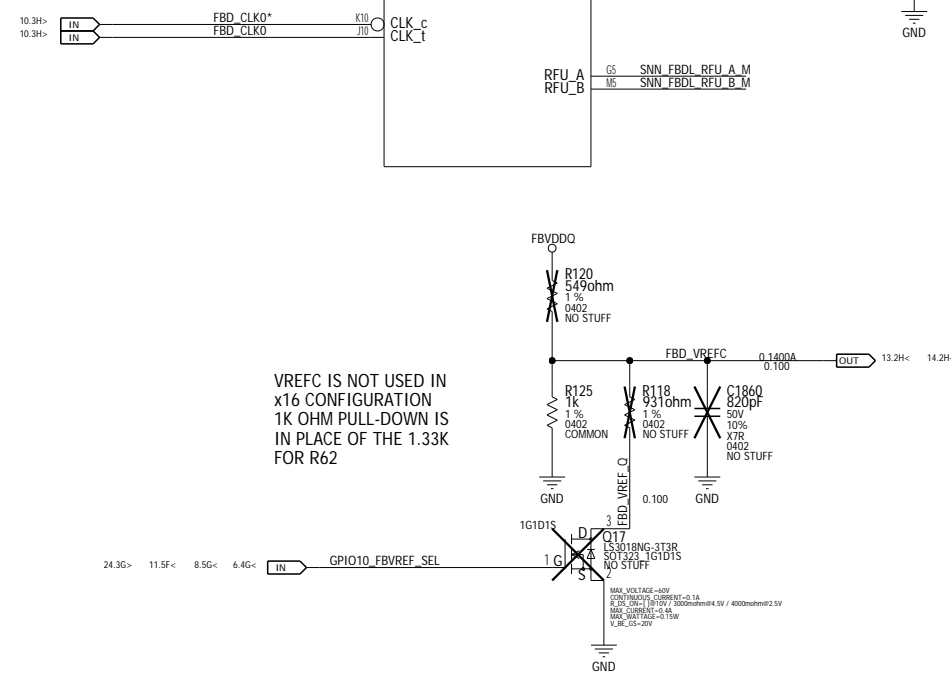
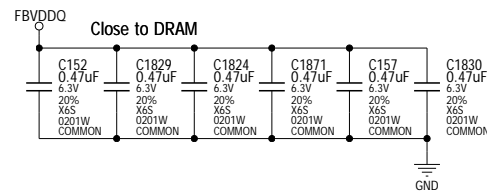
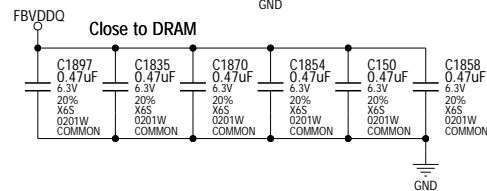
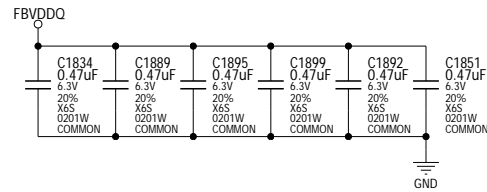
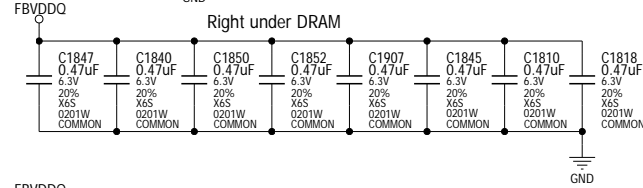
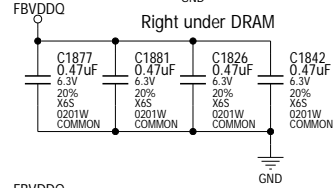
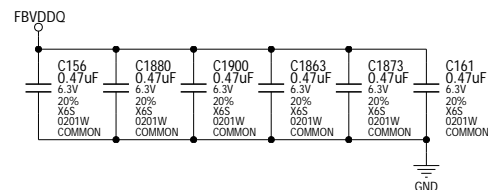
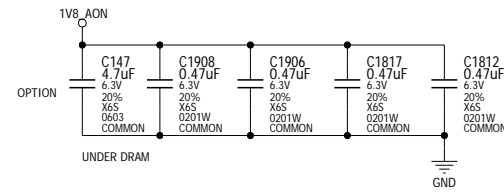
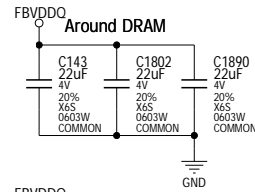
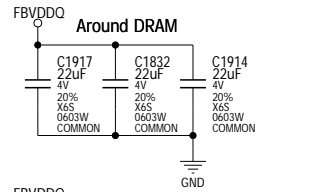
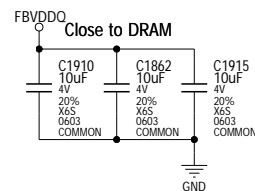
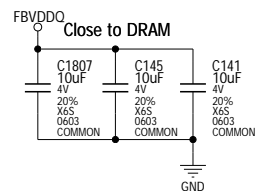
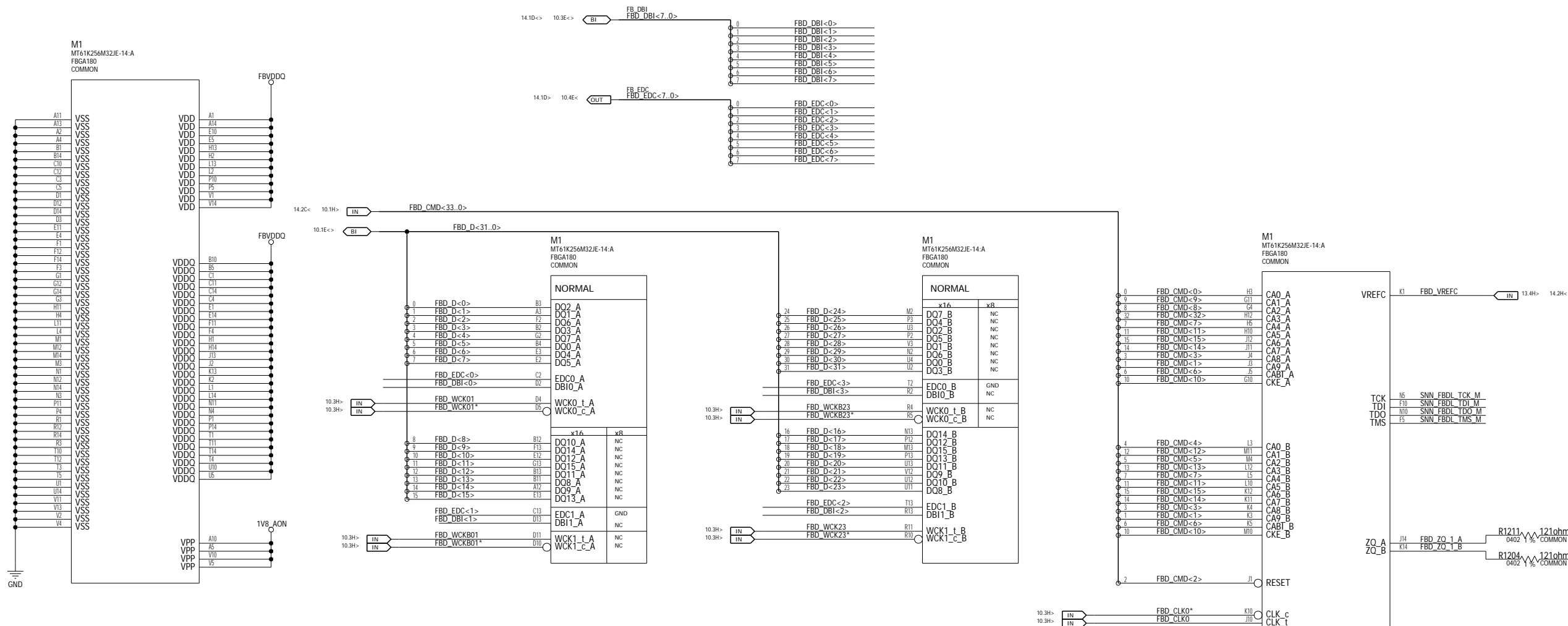
Page12: MEMORY: FBC Partition 63..32



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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	MEMORY: FBC Partition 63..32

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
Nv_PN PCB REV BOM REV	600-1G180-0002-300 PG180-A02 B		PAGE DATE 12 OF 54 21-JUN-2018



VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R62

ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	MEMORY: FBD Partition 31.0

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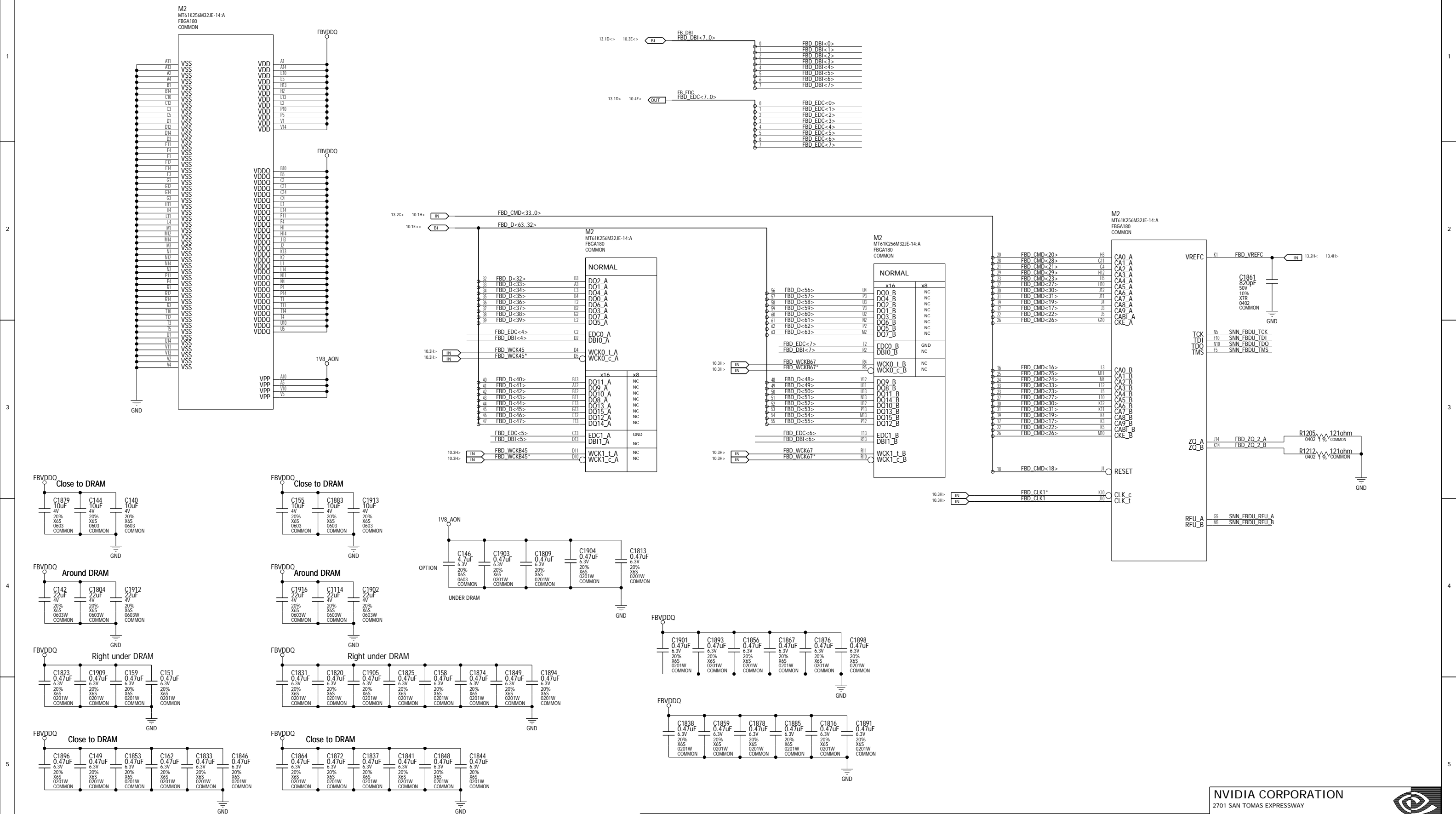
SANTA CLARA, CA 95050, USA

NV PN	600-1G180-0002-300
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Page14: MEMORY: FBD Partition 63..32

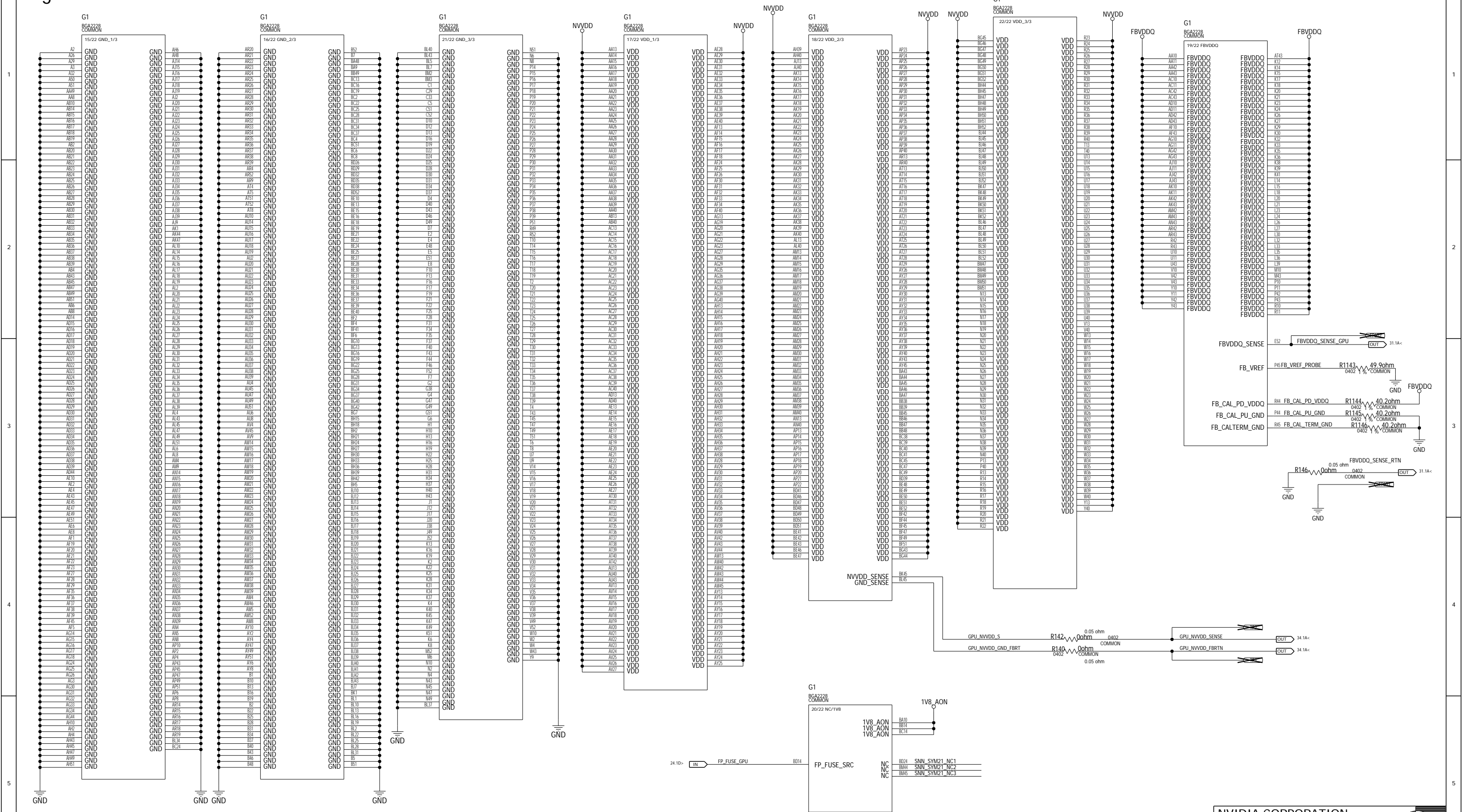


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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	MEMORY: FBD Partition 63..32

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
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Page15: GPU PWR and GND



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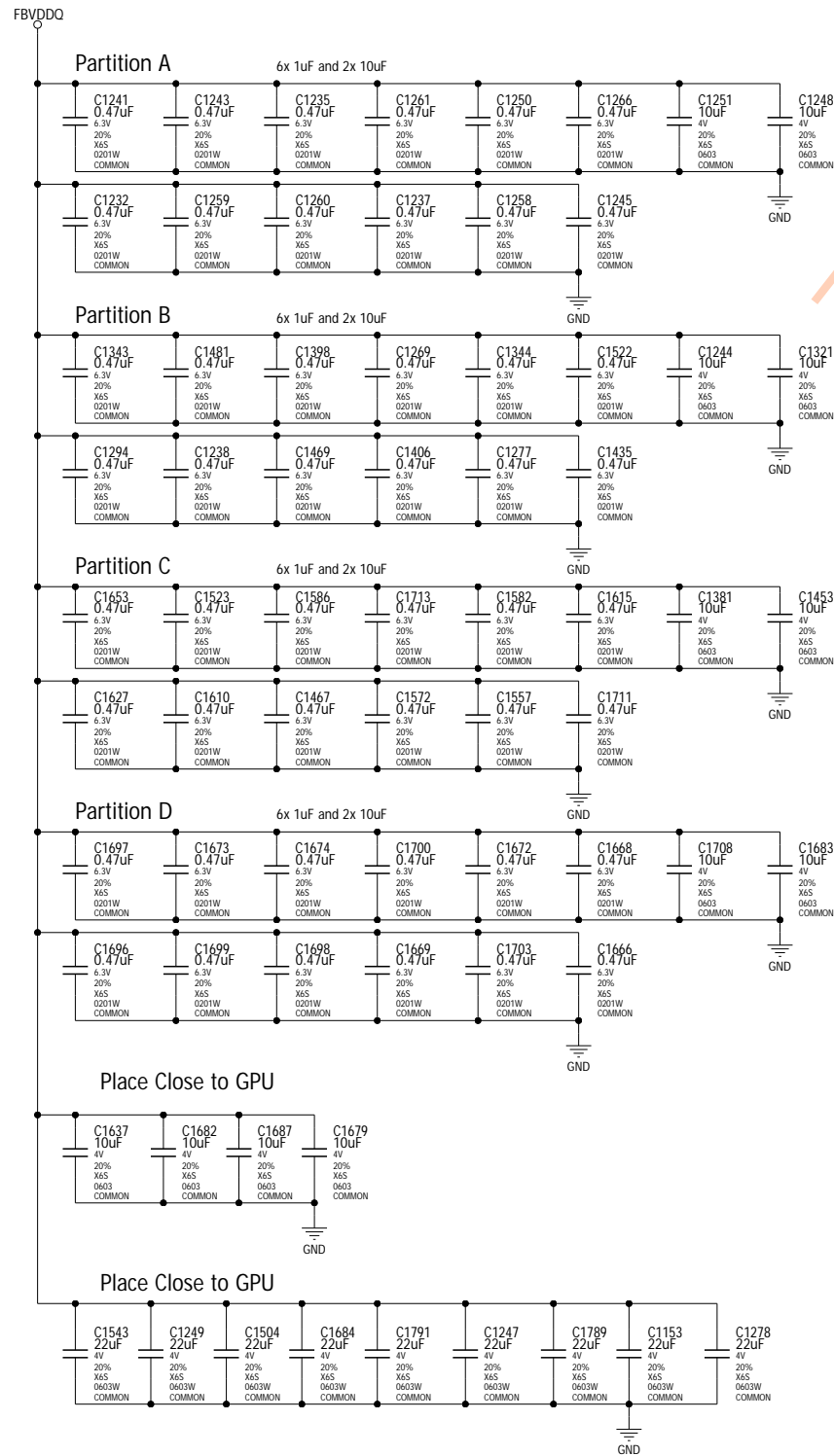
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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	GPU PWR and GND

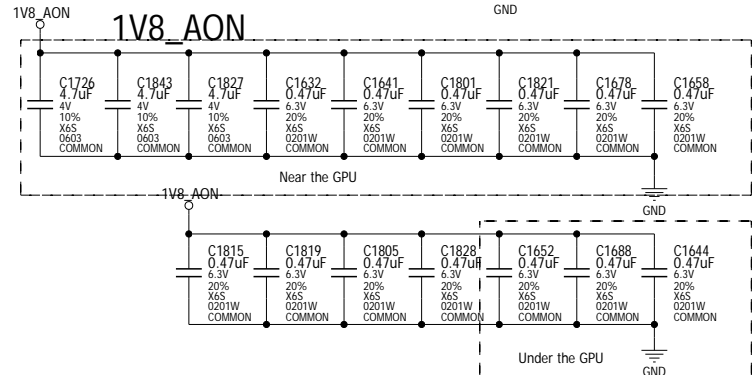
FBVDDQ



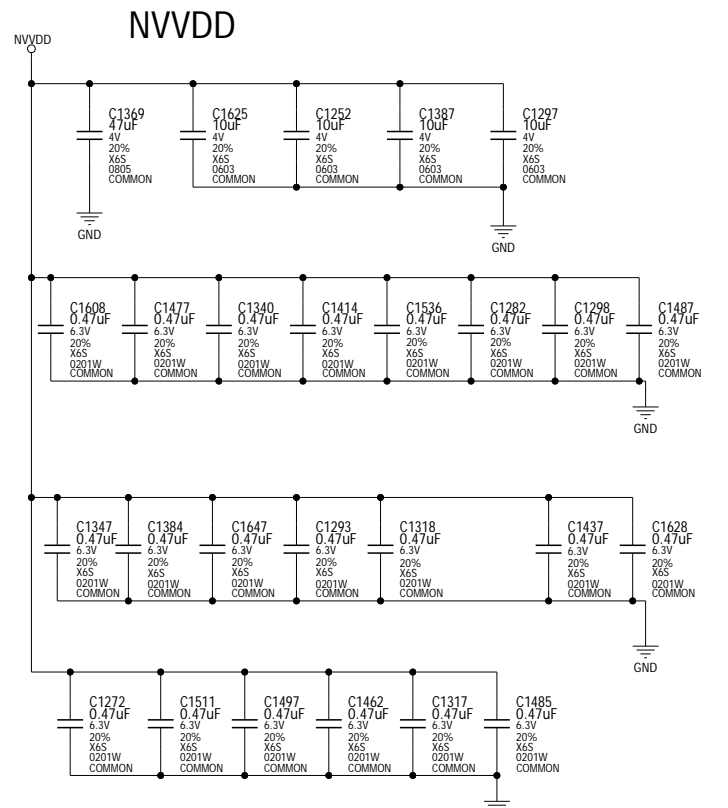
NVVDD



1V8 AON



NVVDD



032-0532-000

X6S
0805

ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	GPU Decoupling

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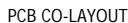
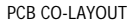
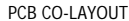
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Page17: GPU Decoupling



ASSEMBLY	SKU SCHEMATIC, (
PAGE DETAIL	GPU DECOUPLING

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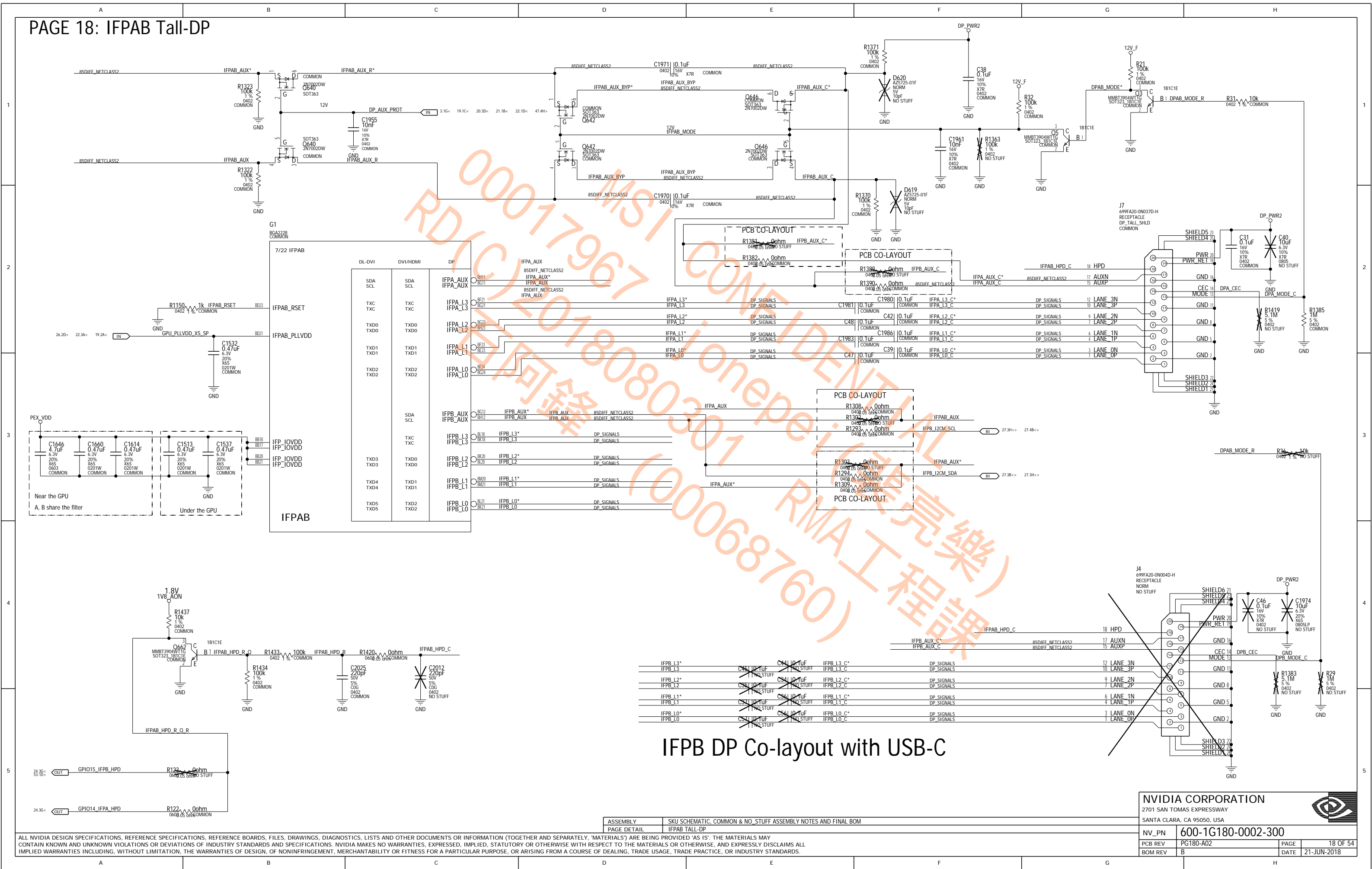
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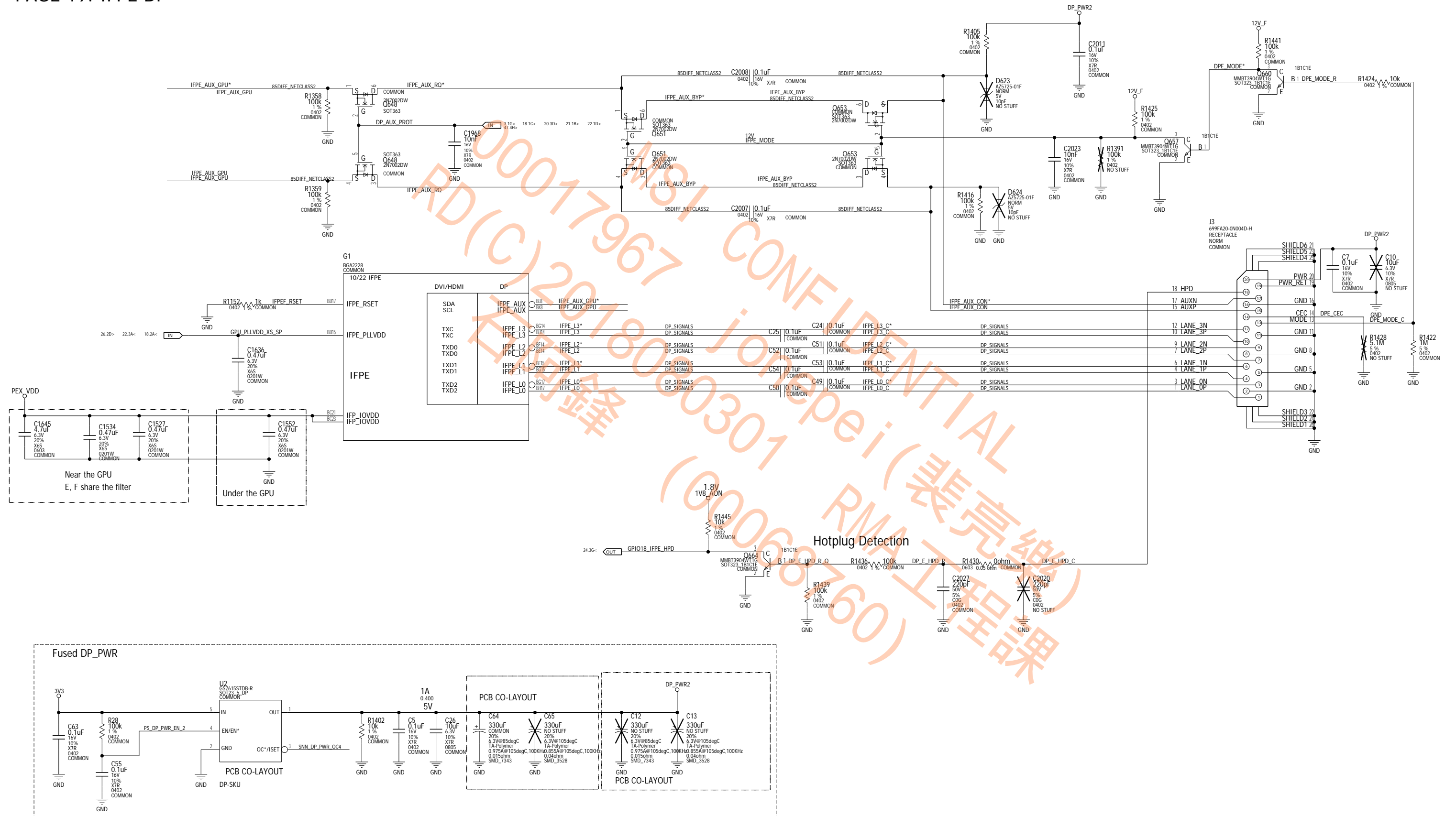
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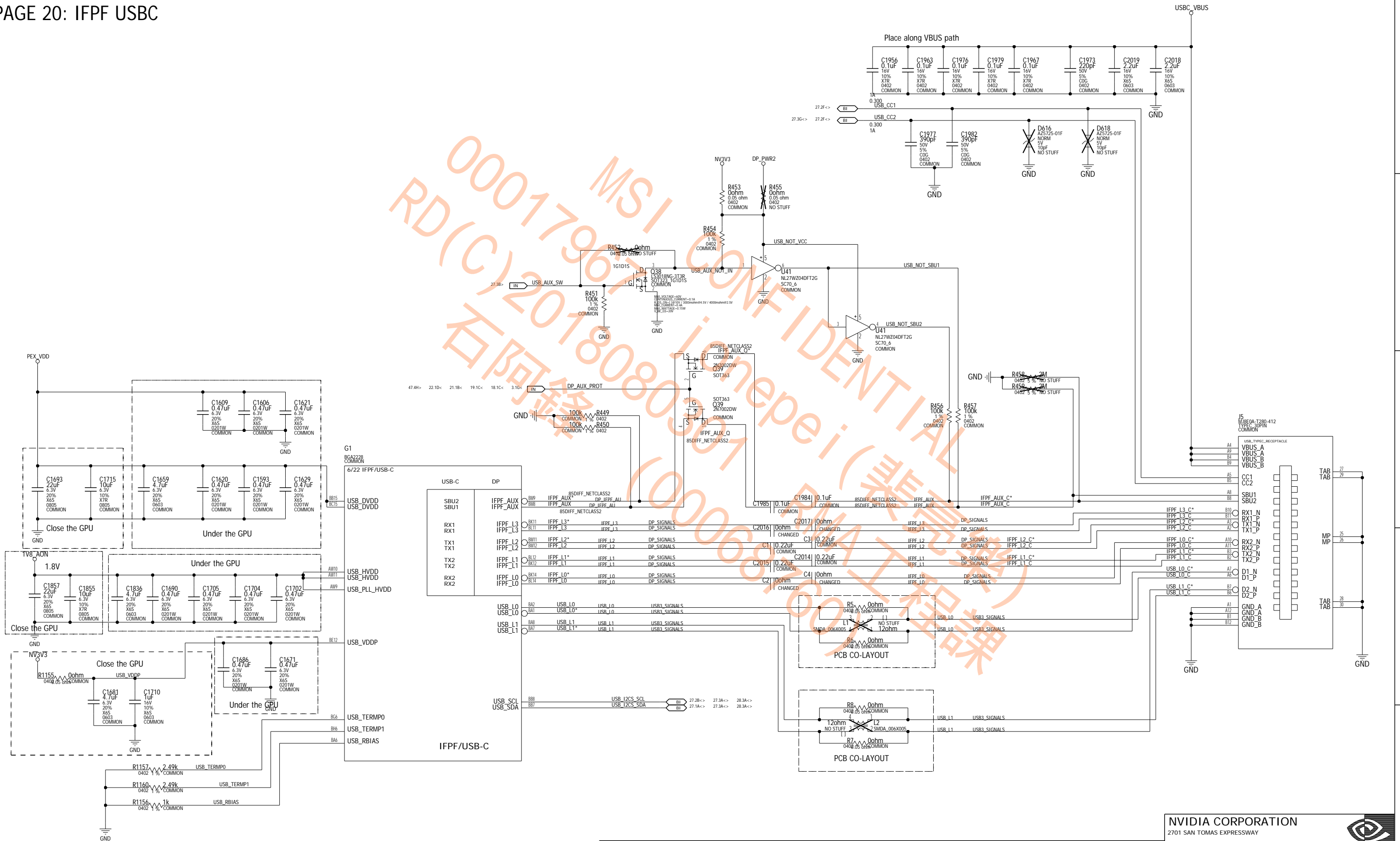


PAGE 18: IFPAB Tall-DP



PAGE 19: IFPE DP





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PAGE DETAIL	IFPF USBC

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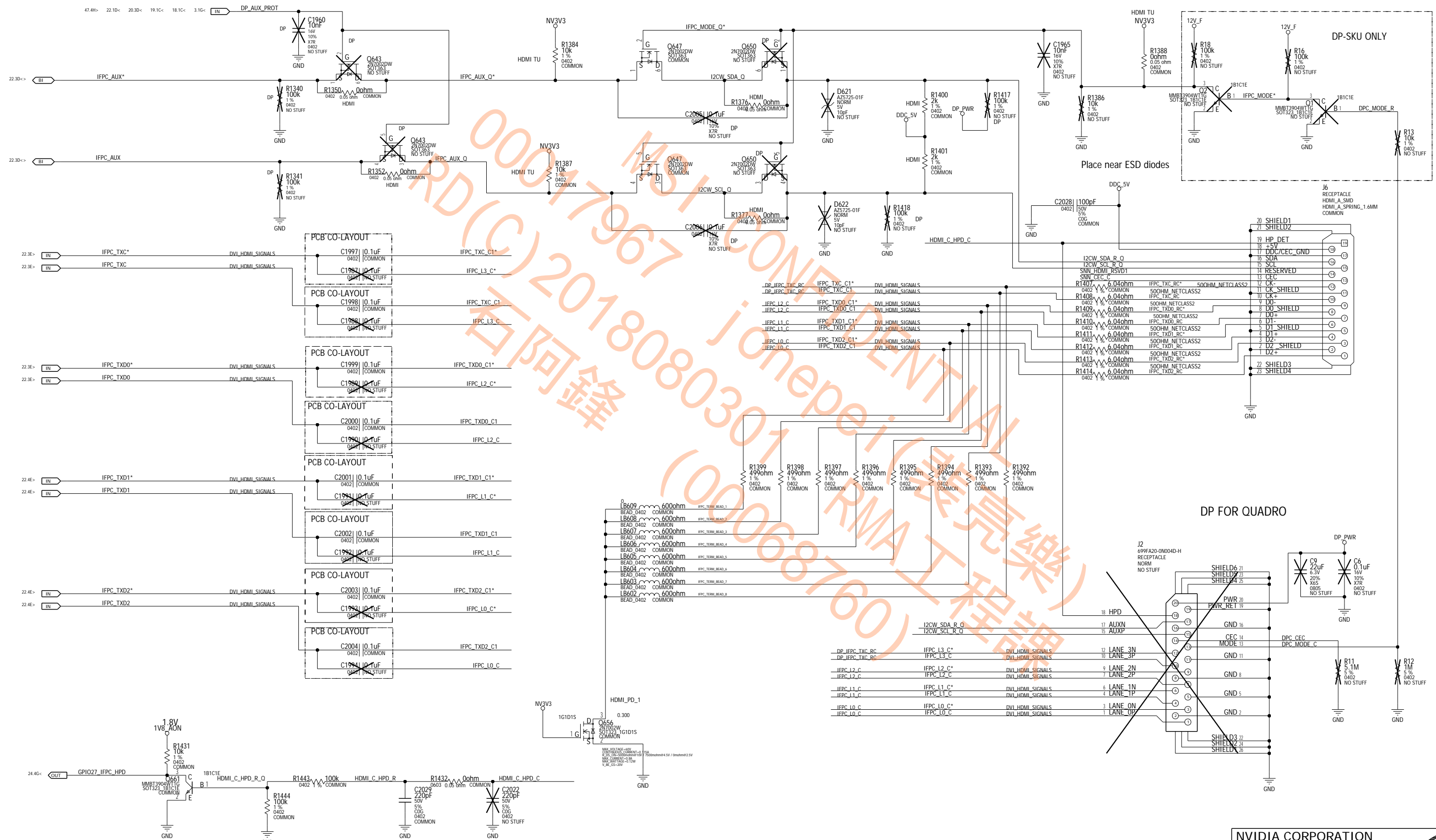
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PAGE 21:IFPC HDMI 2.0/DP



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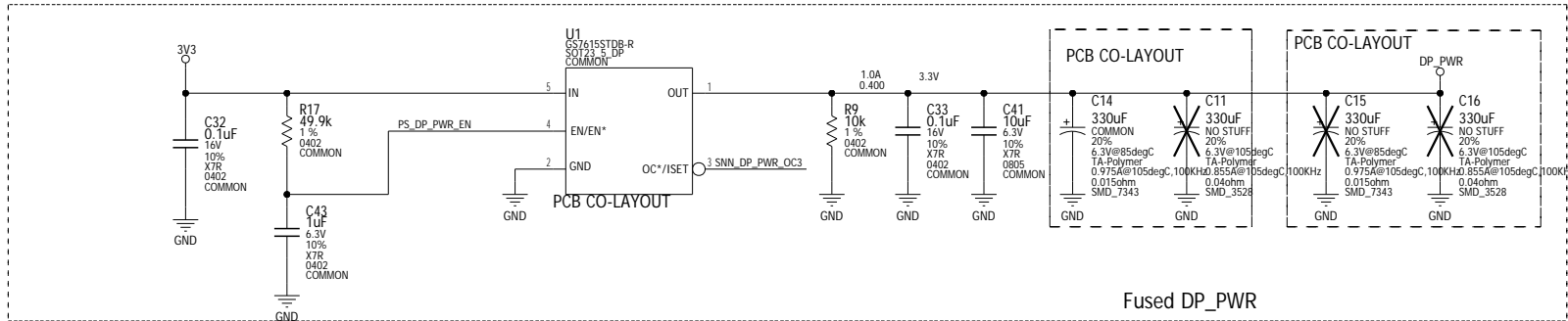
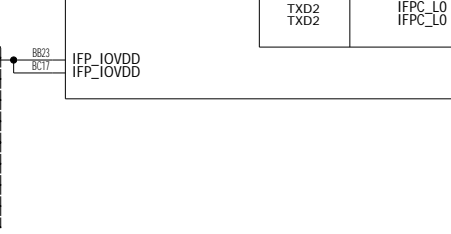
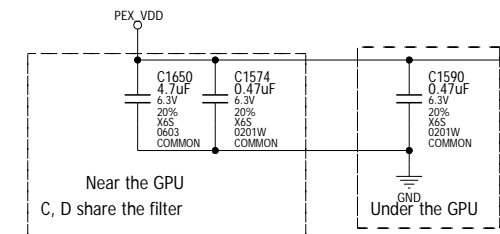
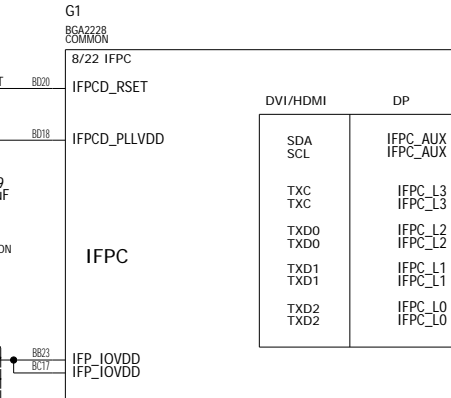
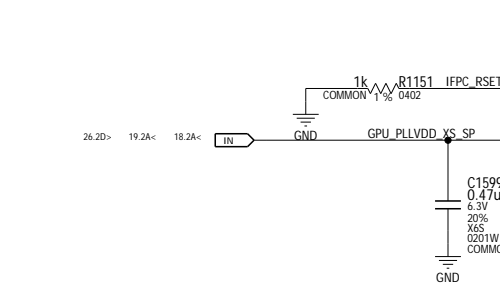
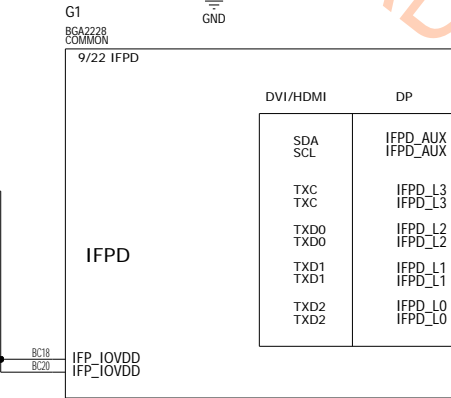
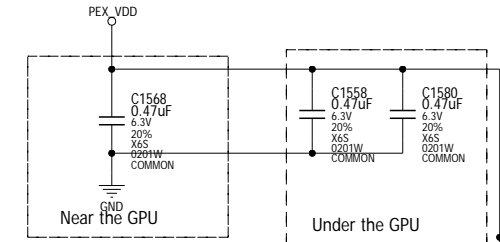
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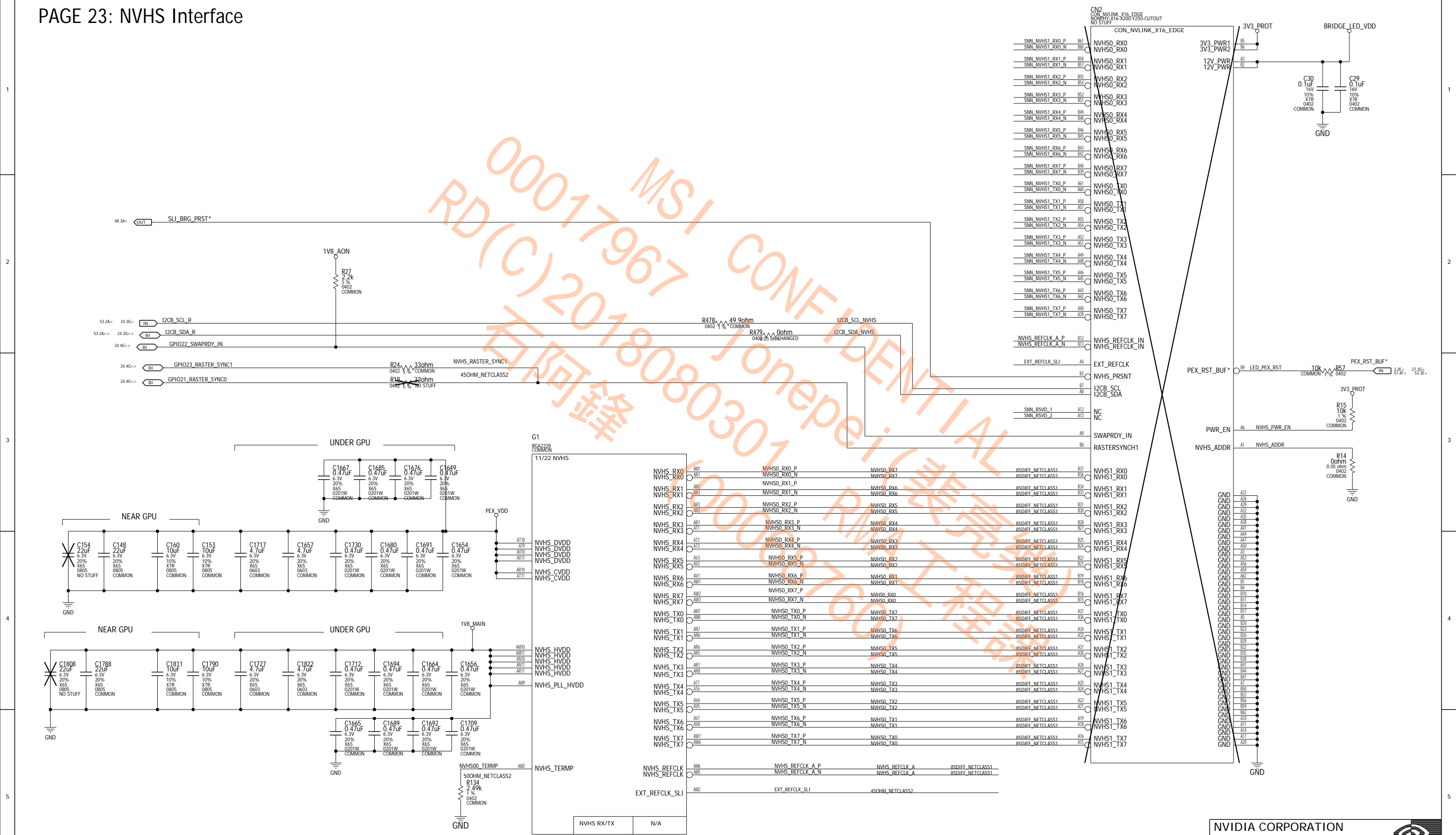


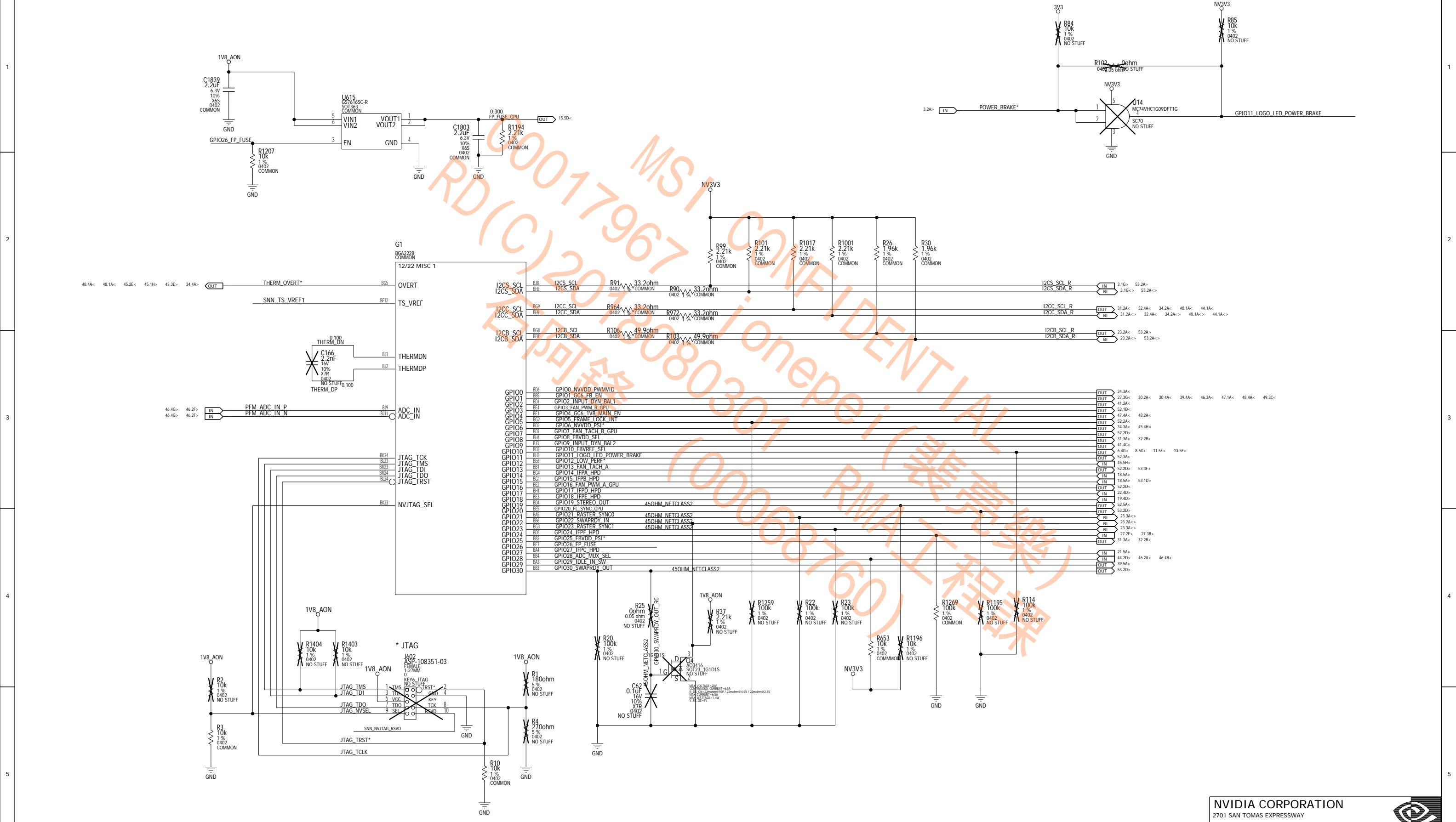
ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	IFPD DP

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PAGE 23: NVHS Interface





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PAGE 25: MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	RAMCFG TBD	DEFAULT
L	L	L	00000	RAMCFG TBD	
L	L	H	00001	RAMCFG TBD	
L	H	L	00010	RAMCFG TBD	
L	H	H	00011	RAMCFG TBD	
H	H	L	00110	RAMCFG TBD	
H	H	H	00111	RAMCFG TBD	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE FS_OVERT ENABLE	DEFAULT
L	L	L	XXX1	FS_OVERT ENABLE	
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	Default
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	

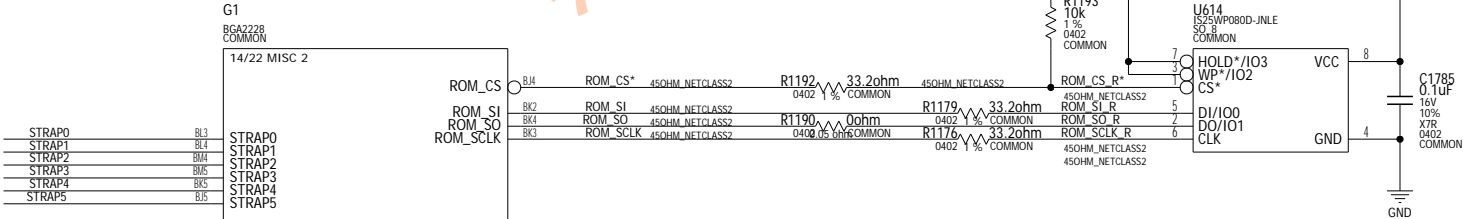
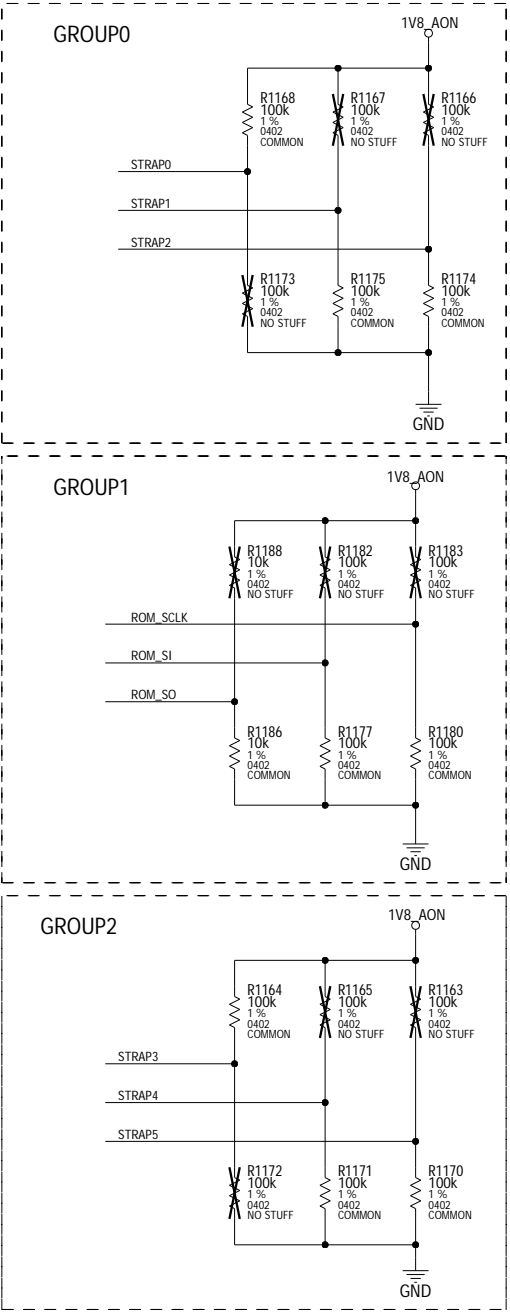
RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Hynix
00111	16Gb	256-bit	Samsung
01000	16Gb	256-bit	Micron

- 1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

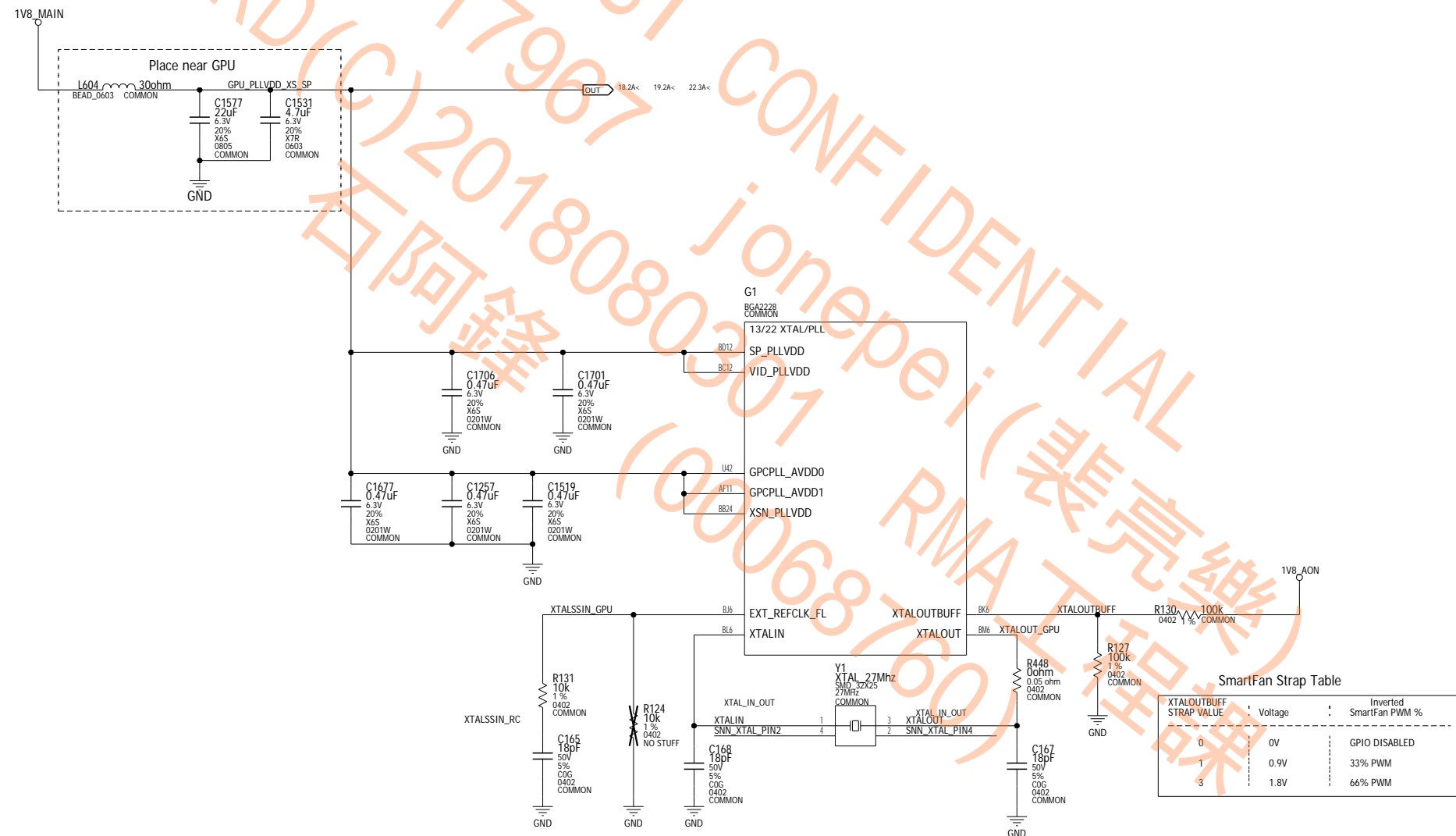
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

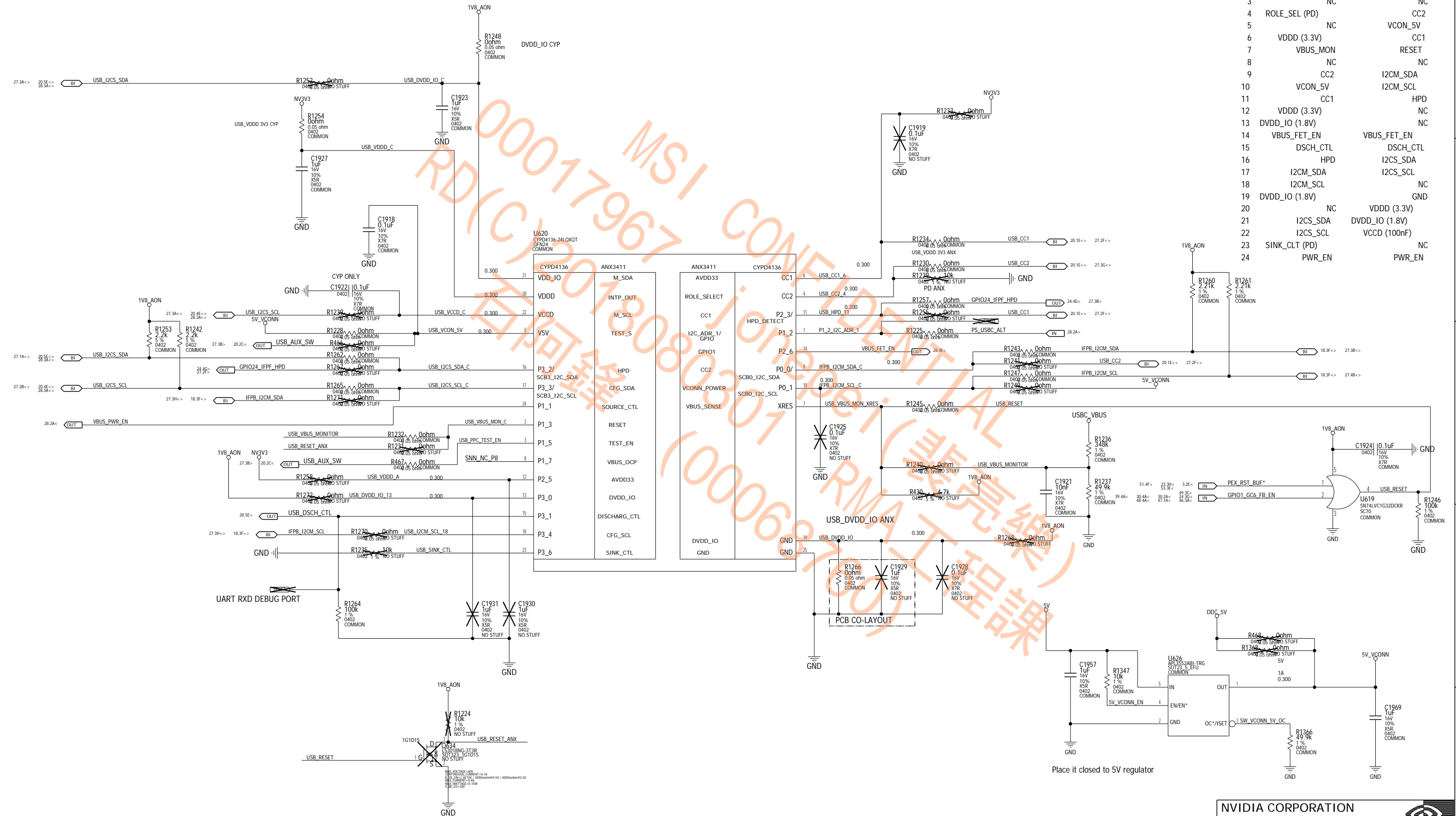
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



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PAGE 27: MISC: USB PPC

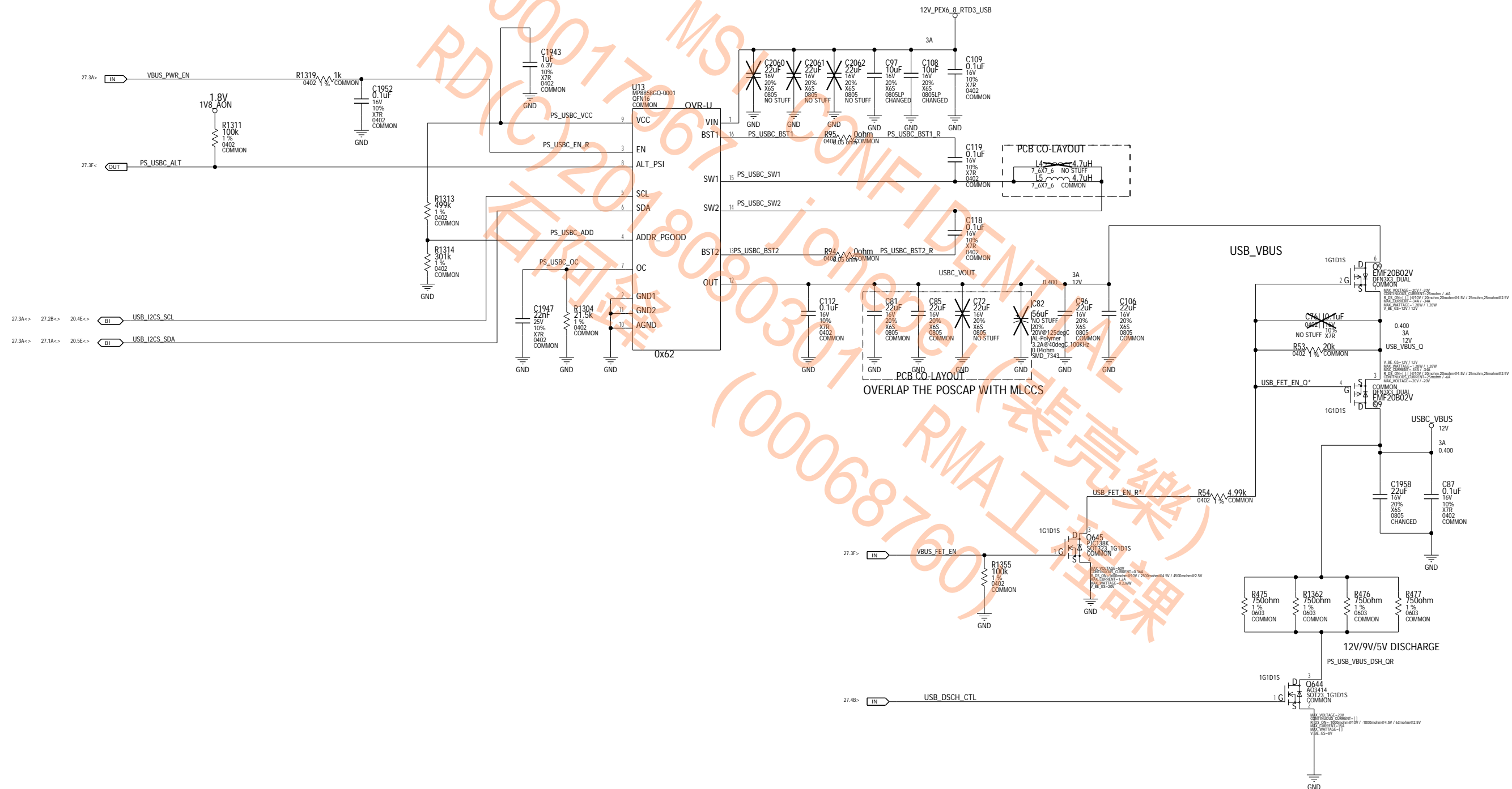


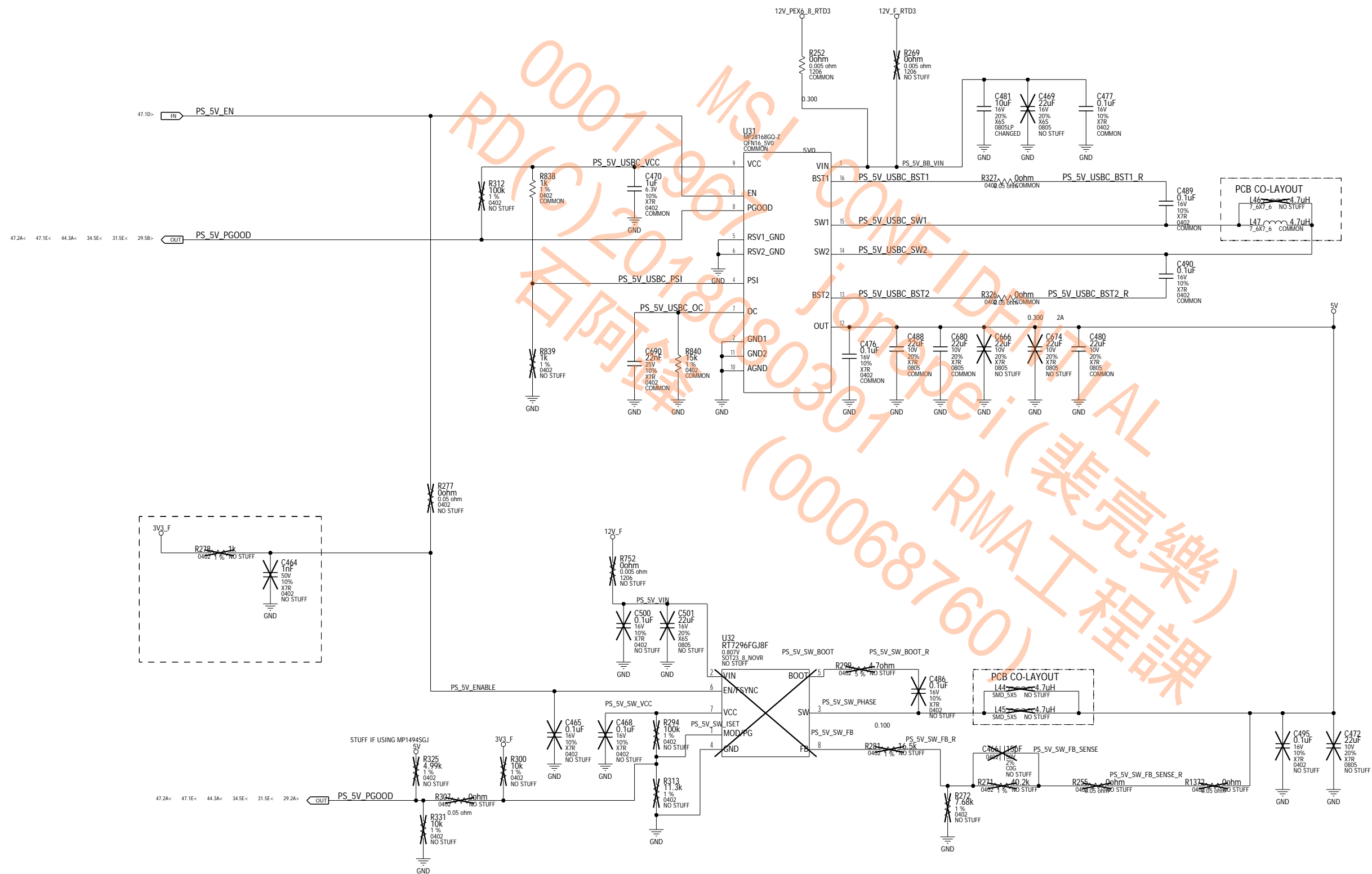
PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN


ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	MISC: USB PPC

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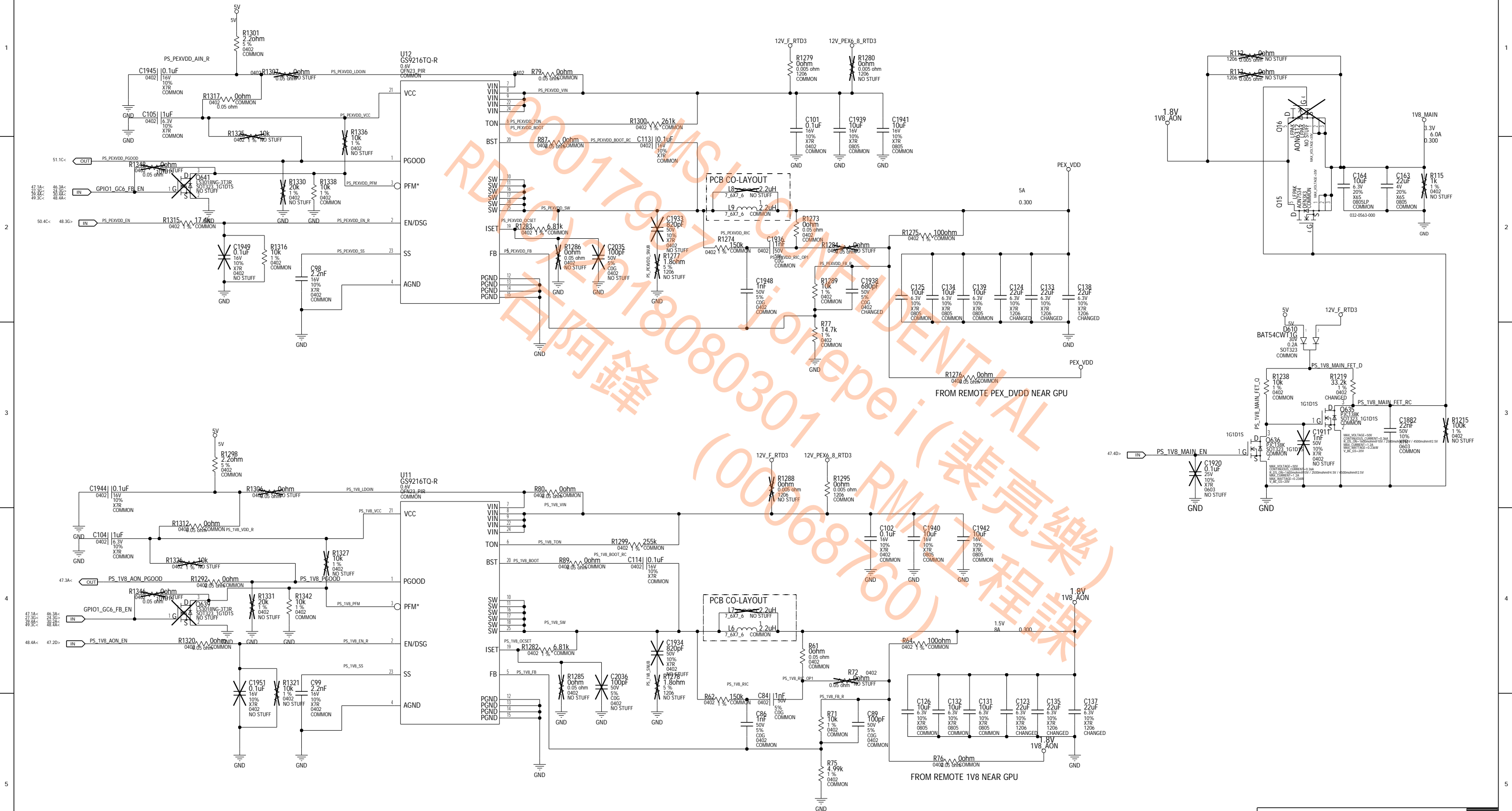
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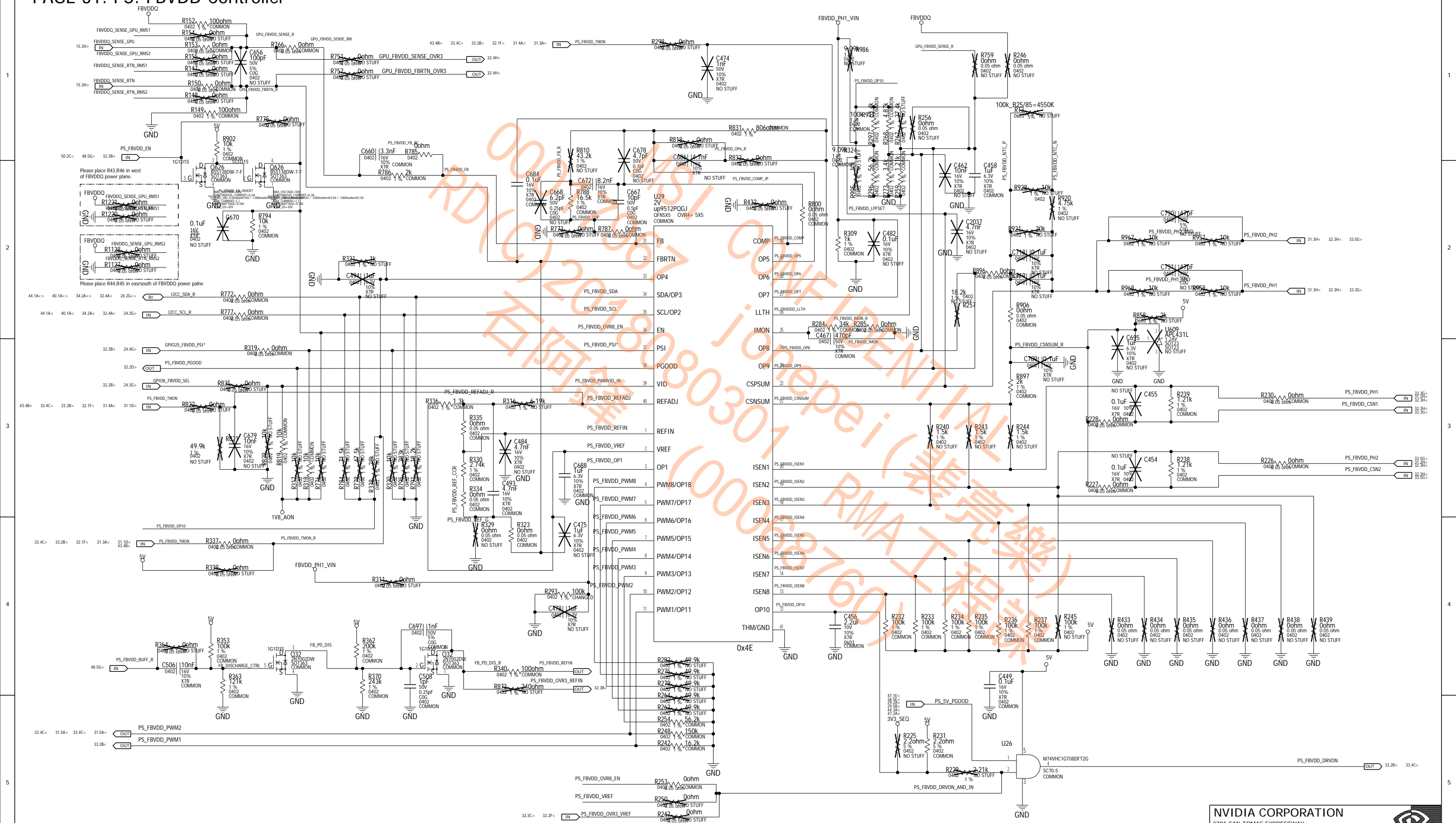


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PAGE 31: PS: FBVDD Controller



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PAGE DETAIL	PS: FBVDD CONTROLLER

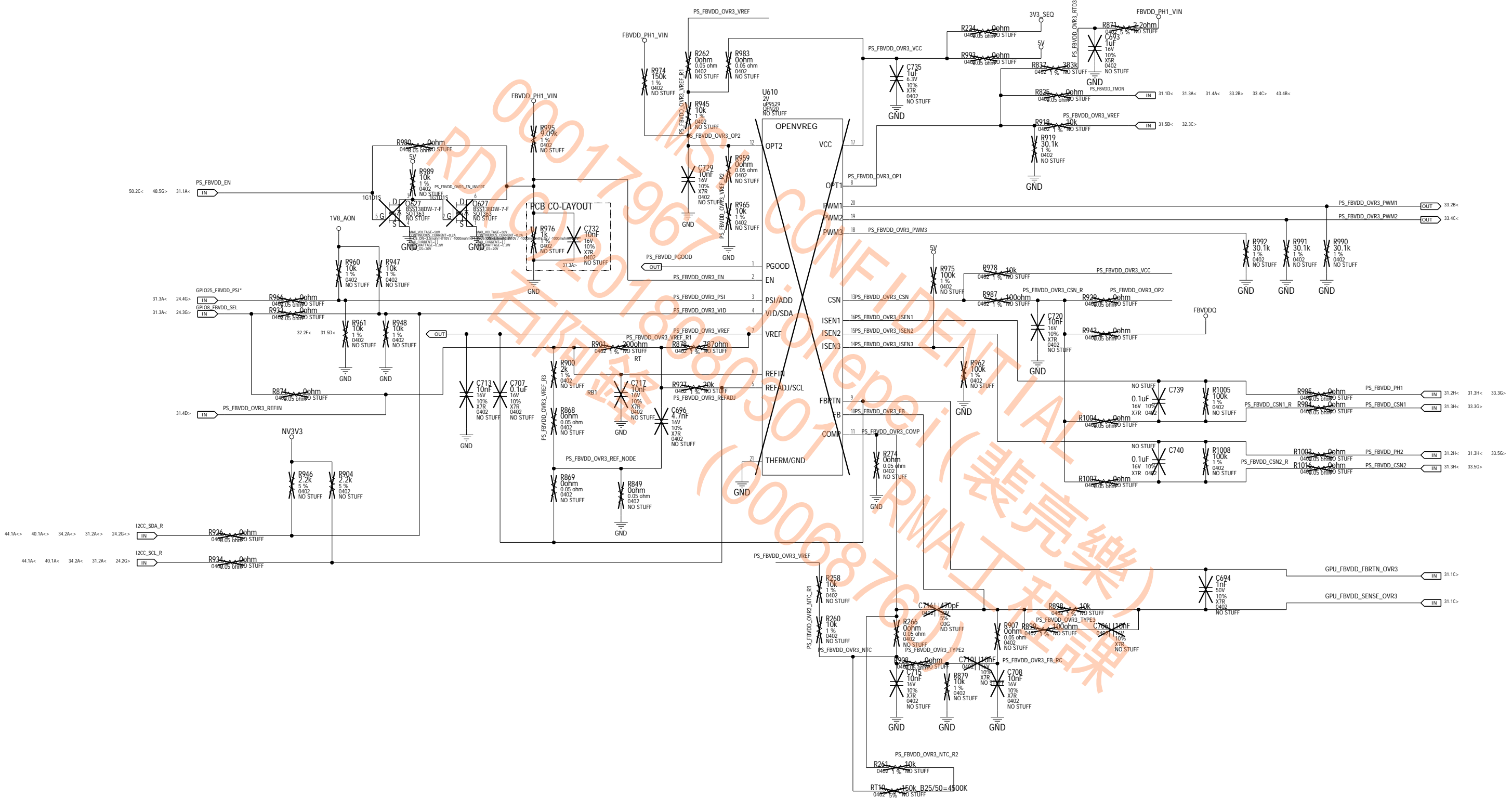
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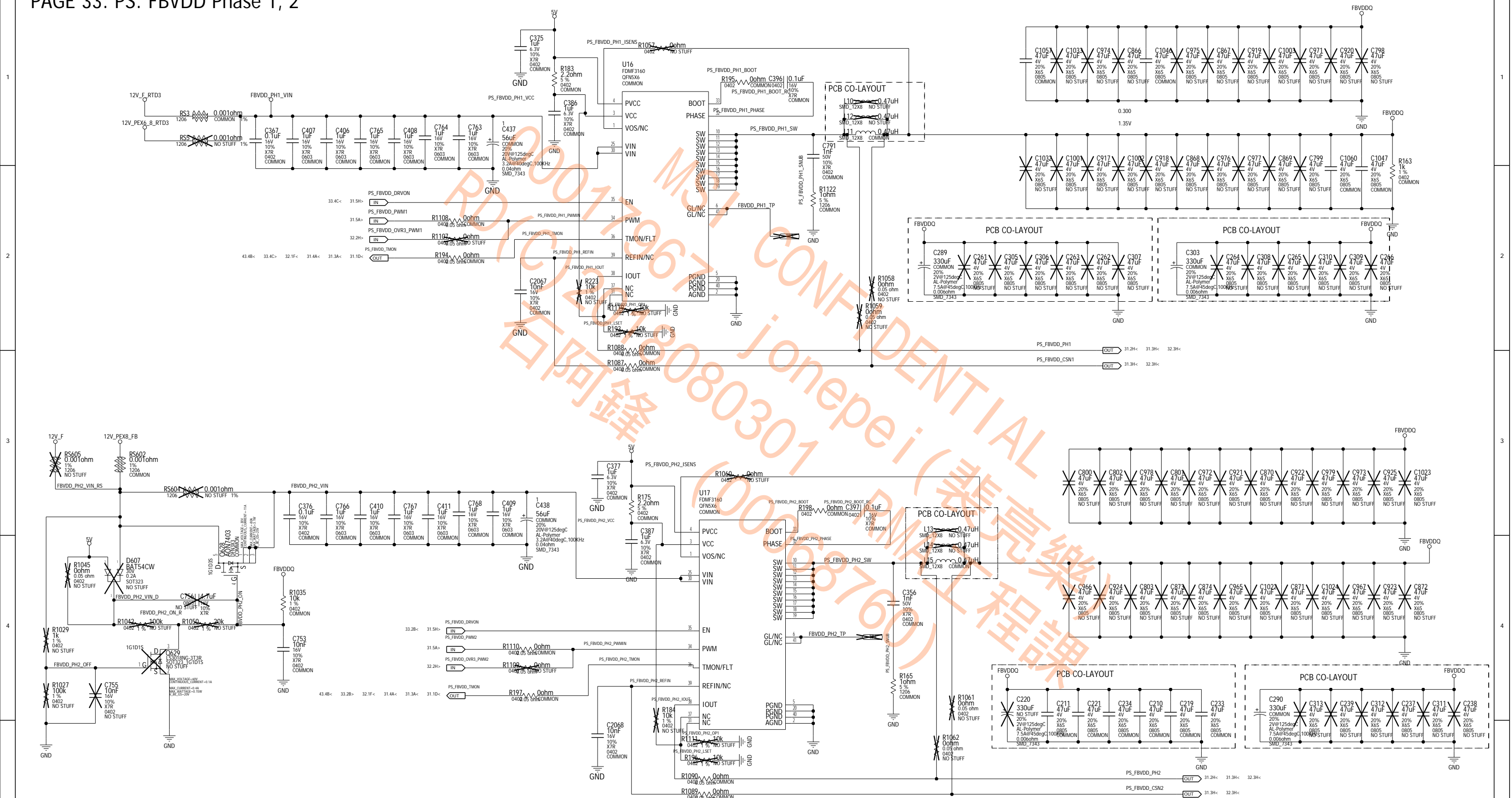
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PAGE 33: PS: FBVDD Phase 1, 2



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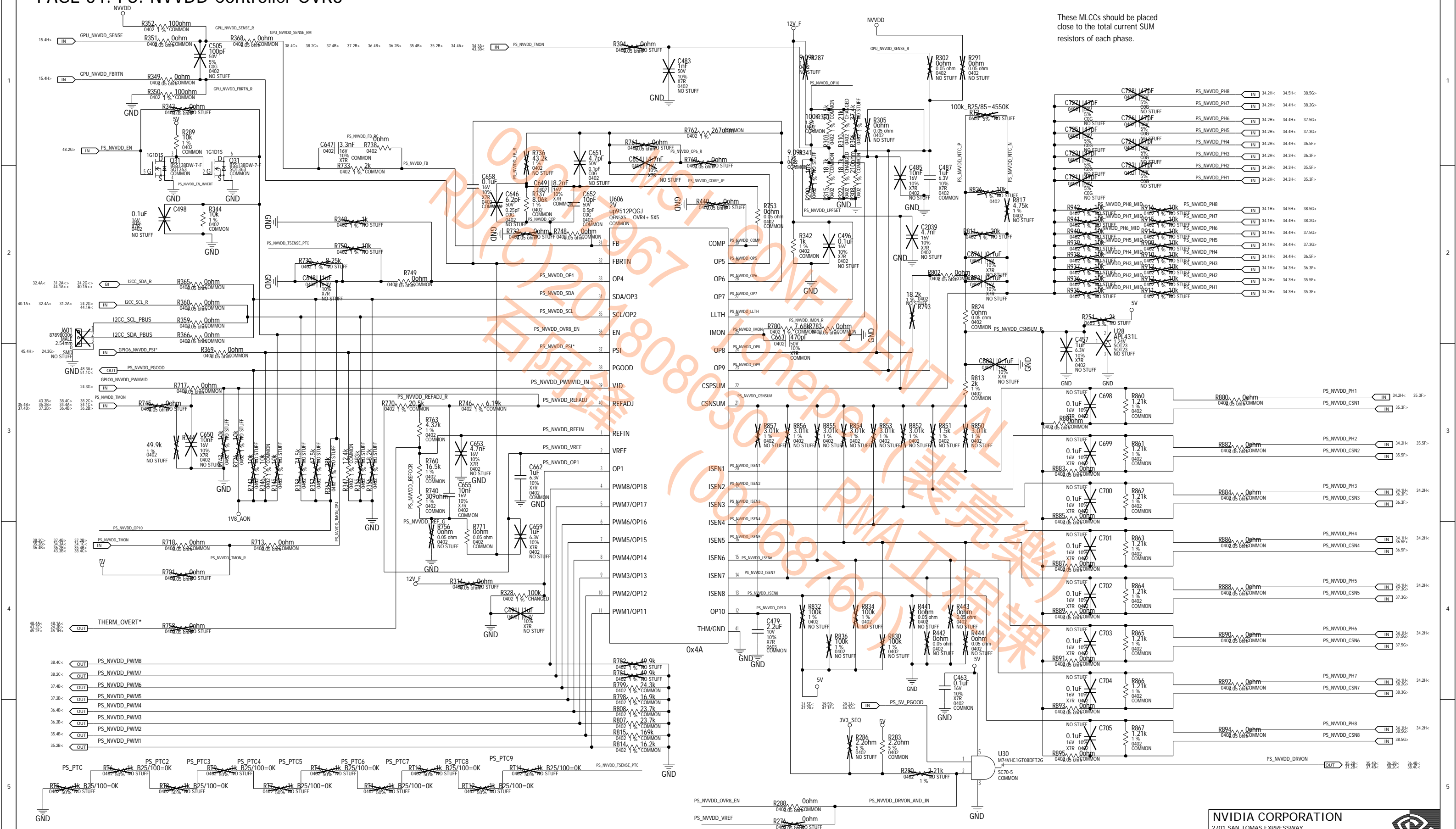
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PAGE DETAIL	PS: FBVDD PHASE 1, 2

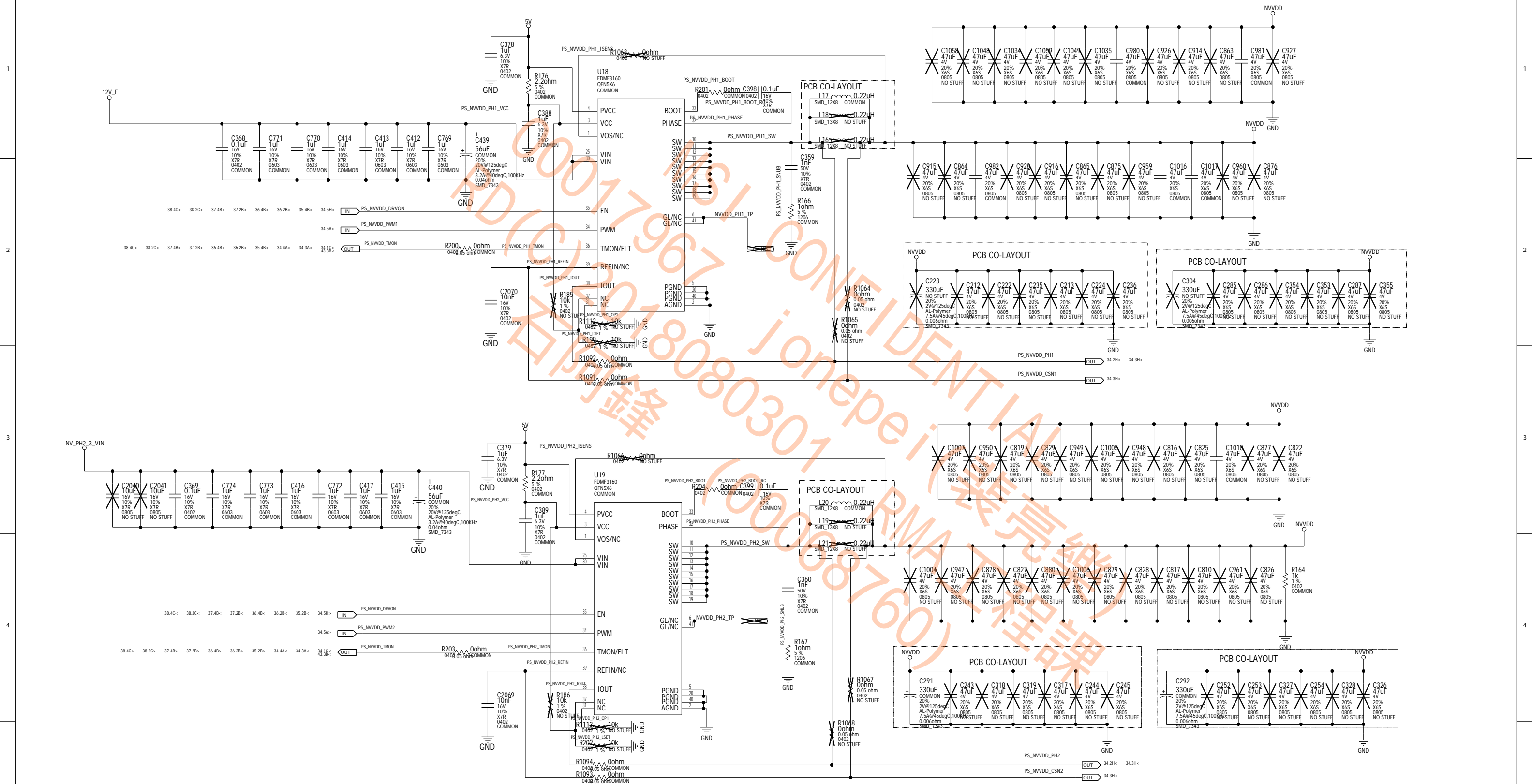
PAGE 34: PS: NVVDD Controller OVR8

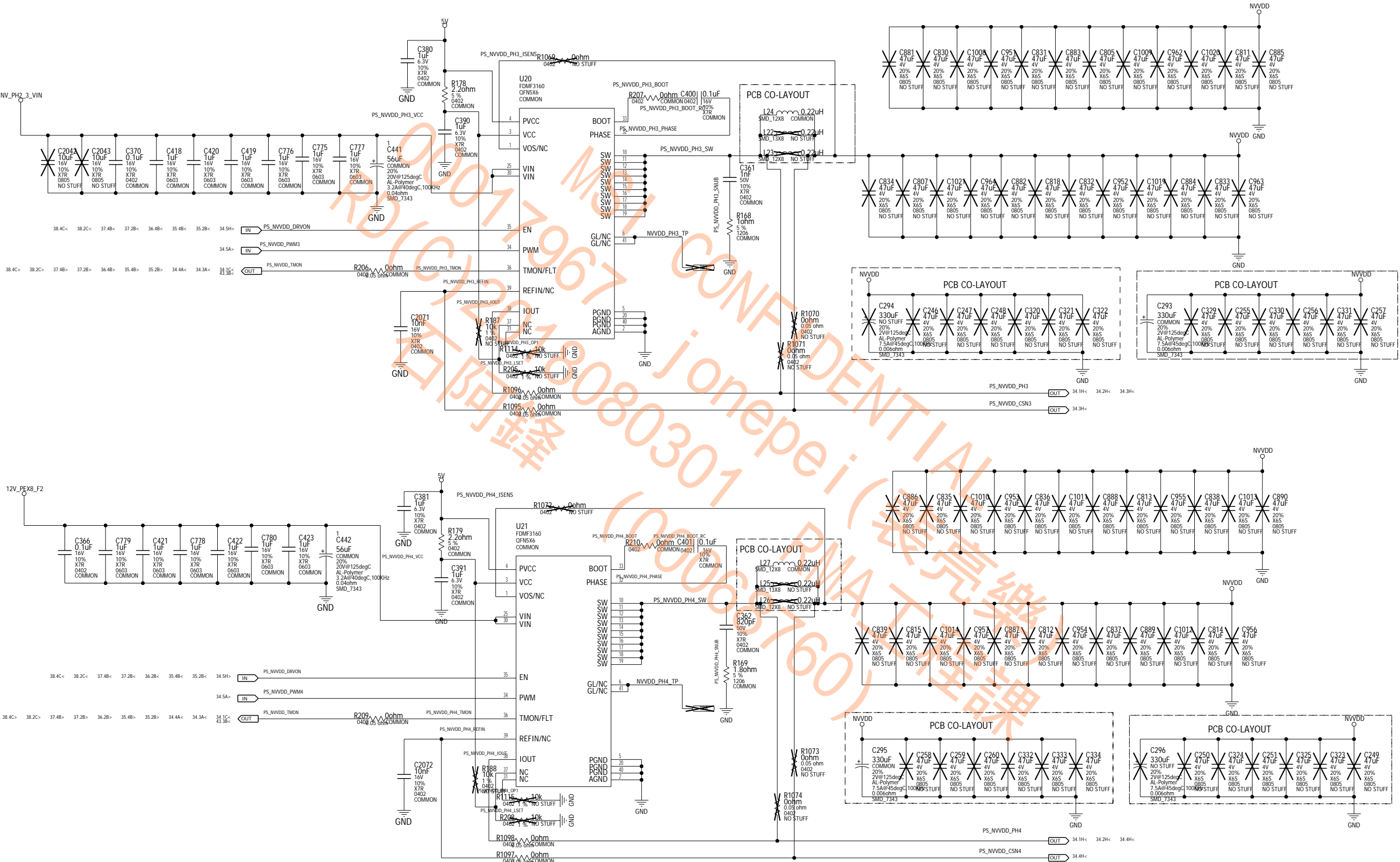


These MLCCs should be placed close to the total current SUM resistors of each phase.

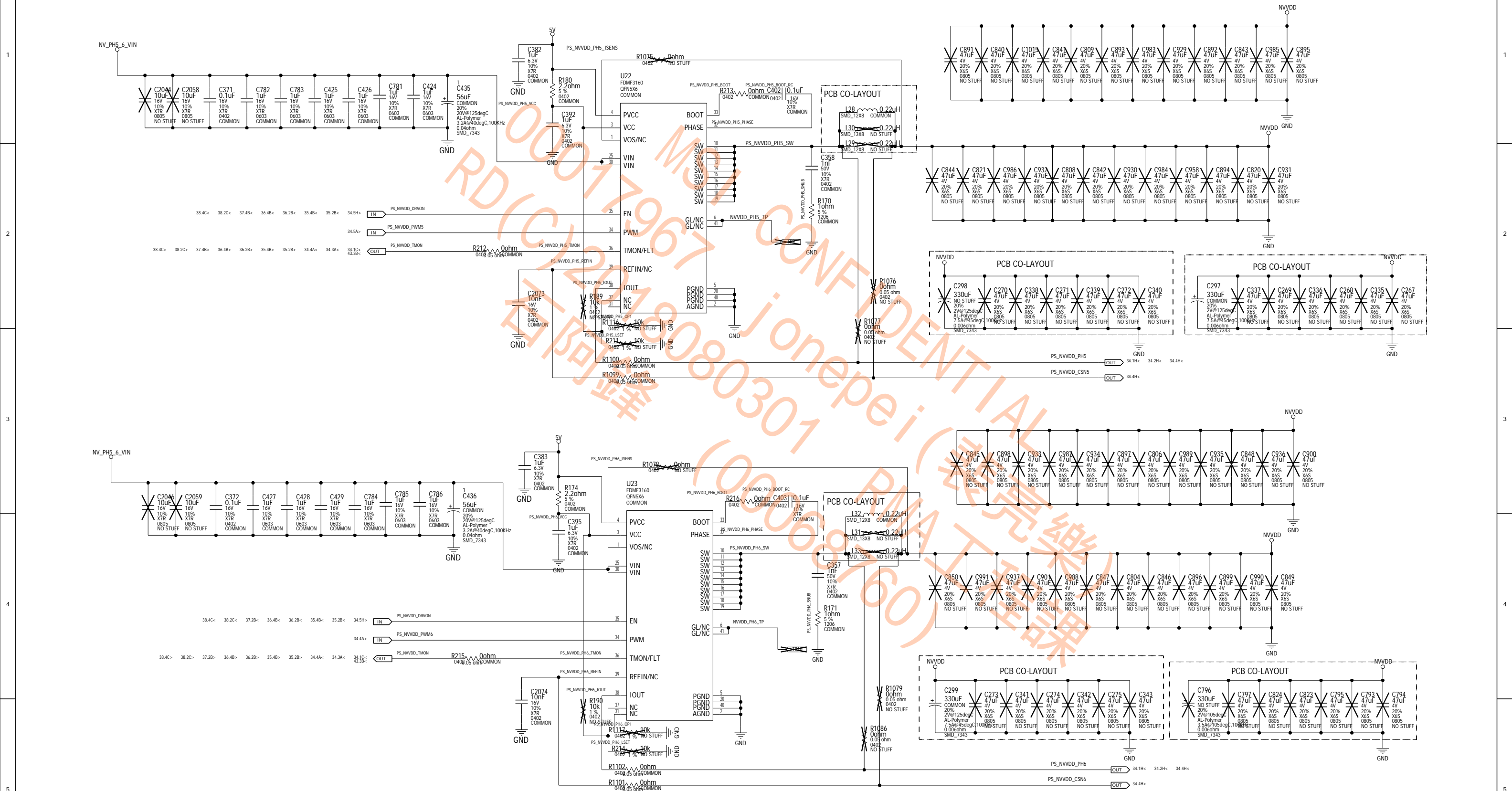
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NV_PN 600-1G180-0002-300			
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BOM REV	B	DATE	21-JUN-2018

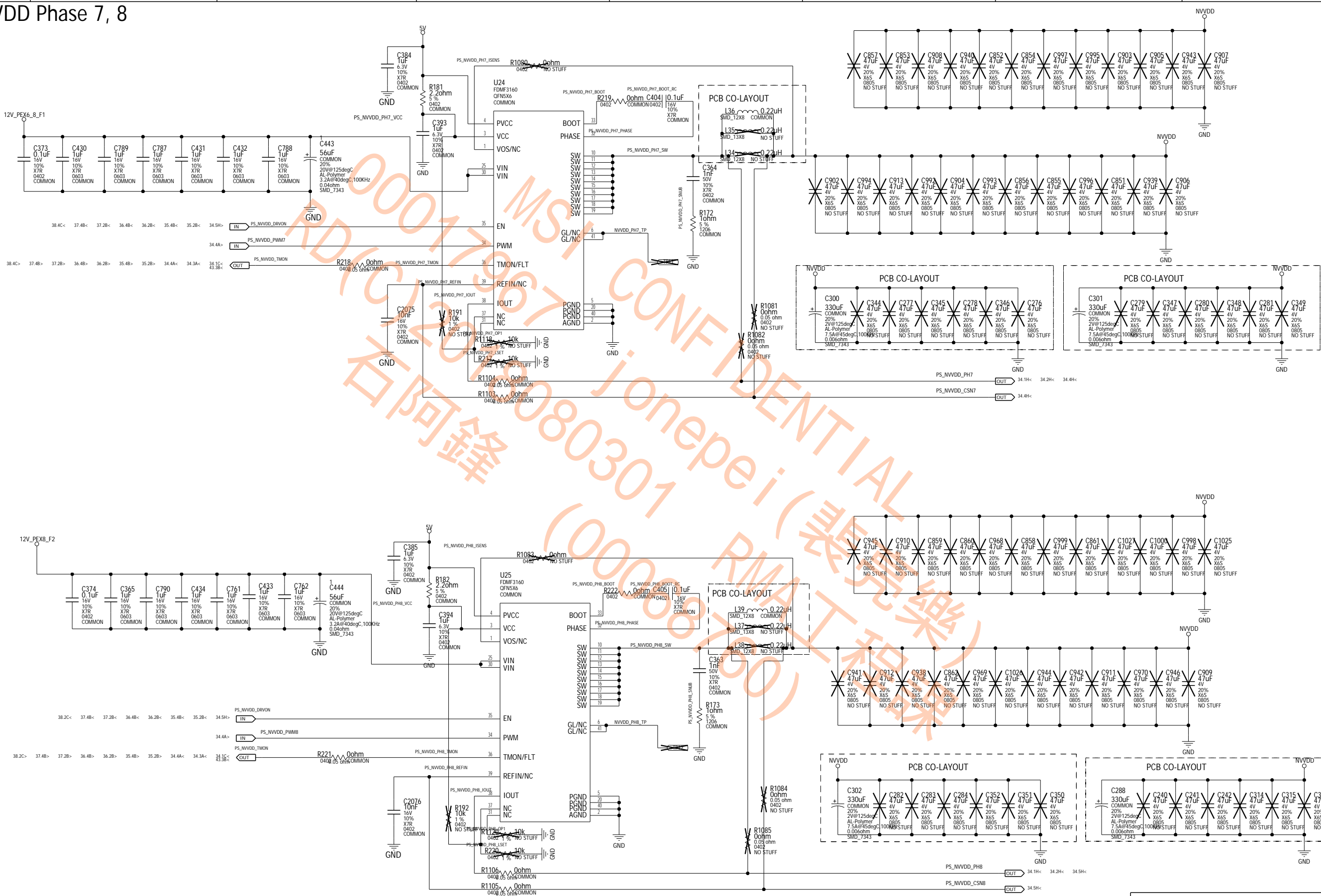
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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PS: NVVDD Phase 7, 8

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PCB REV PG180-A02

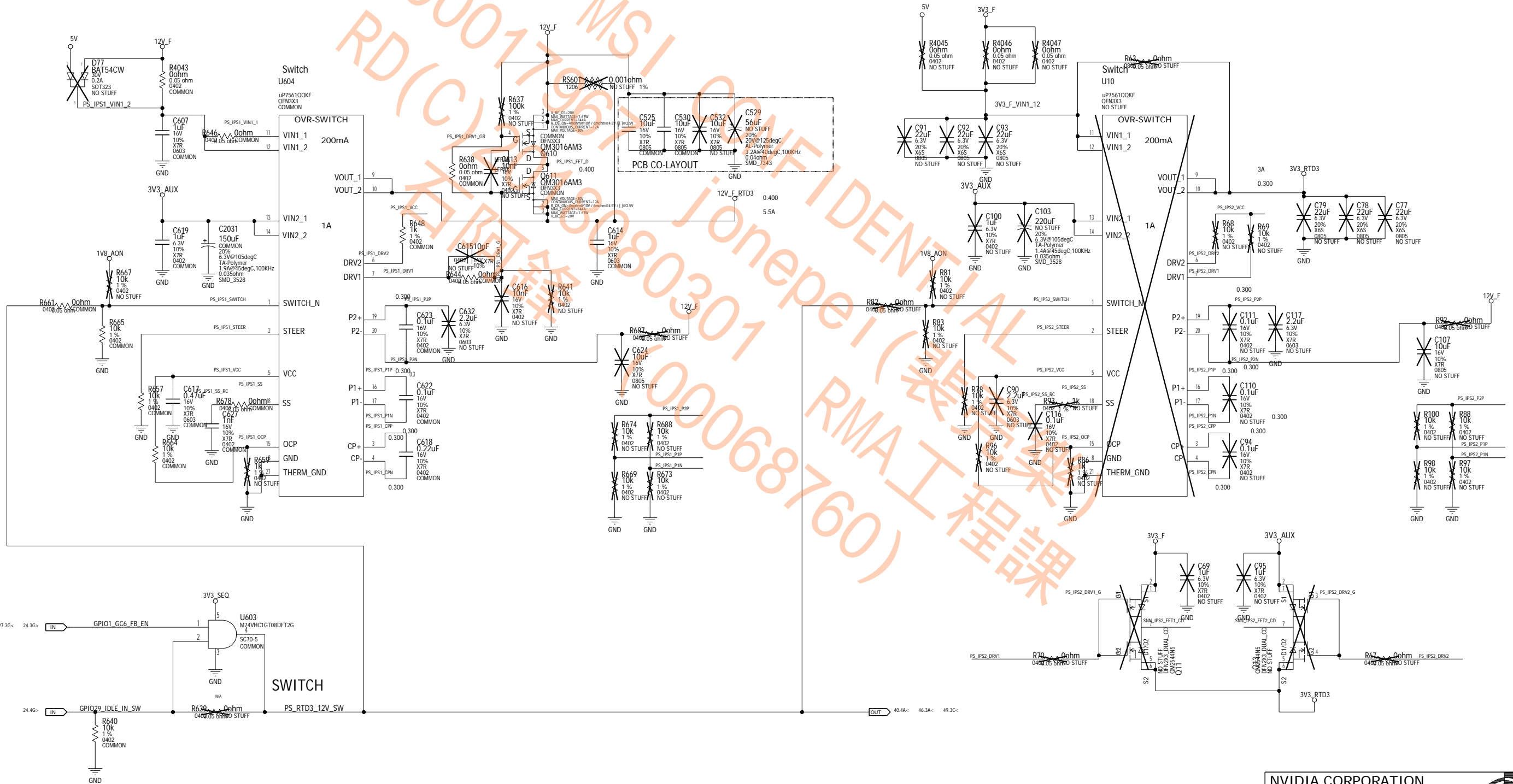
BOM REV B

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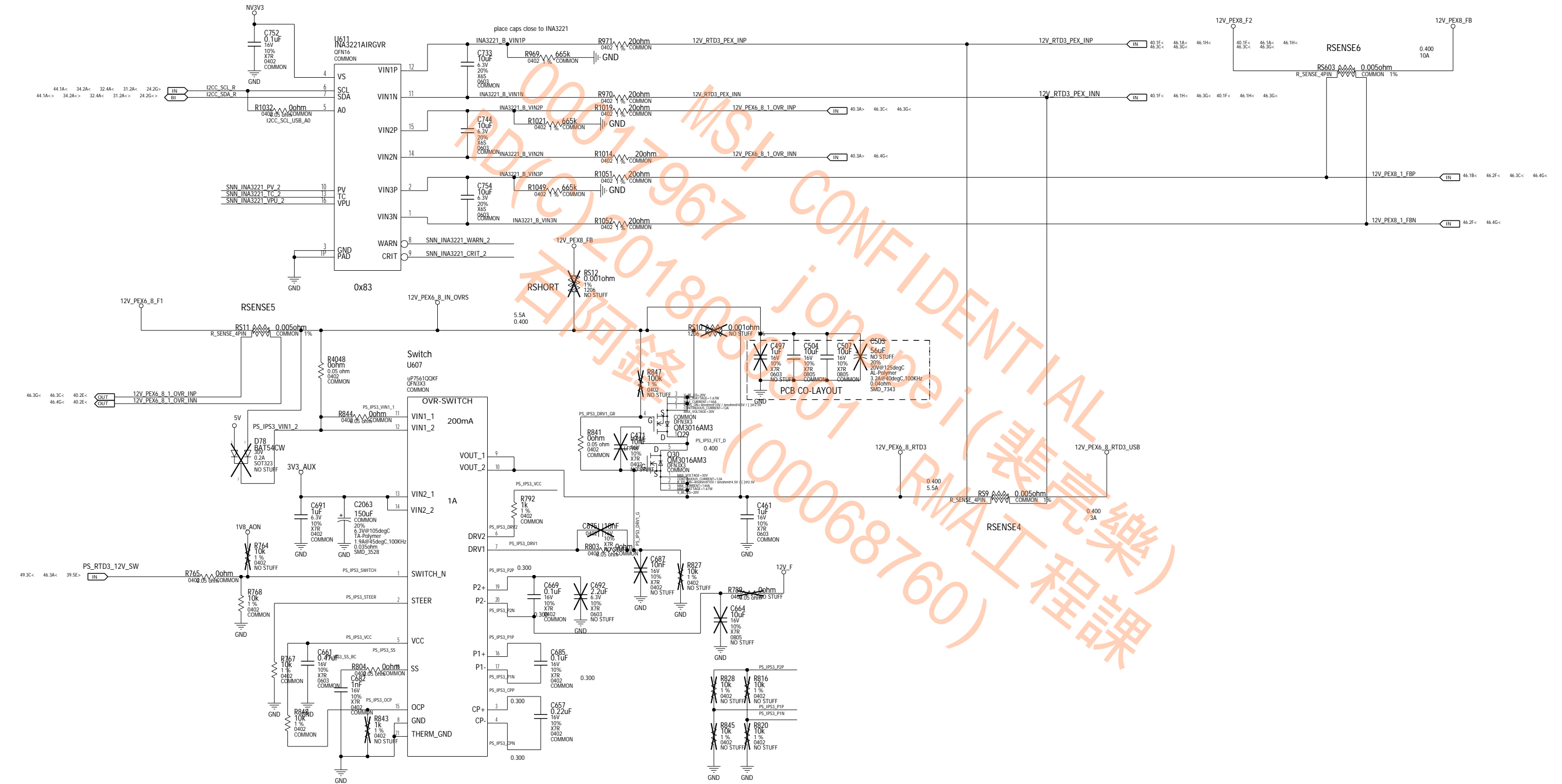
DATE 21-JUN-2018

AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A




PAGE 40: PS: INPUT SWITCH RTD3 USB

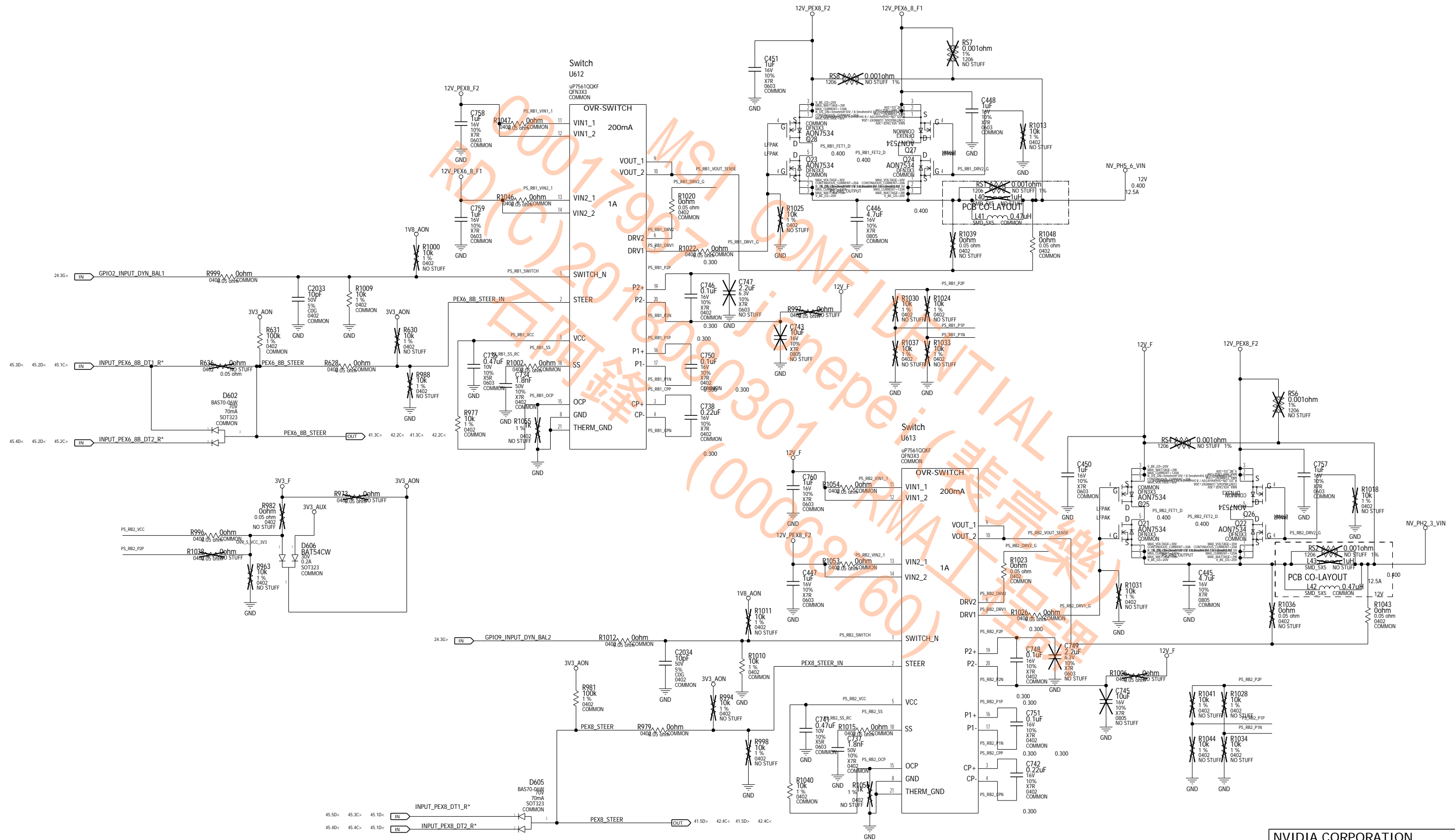


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ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PS: INPUT SWITCH RTD3 USB

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PAGE 41: PS: INPUT SWITCH Rail Balance



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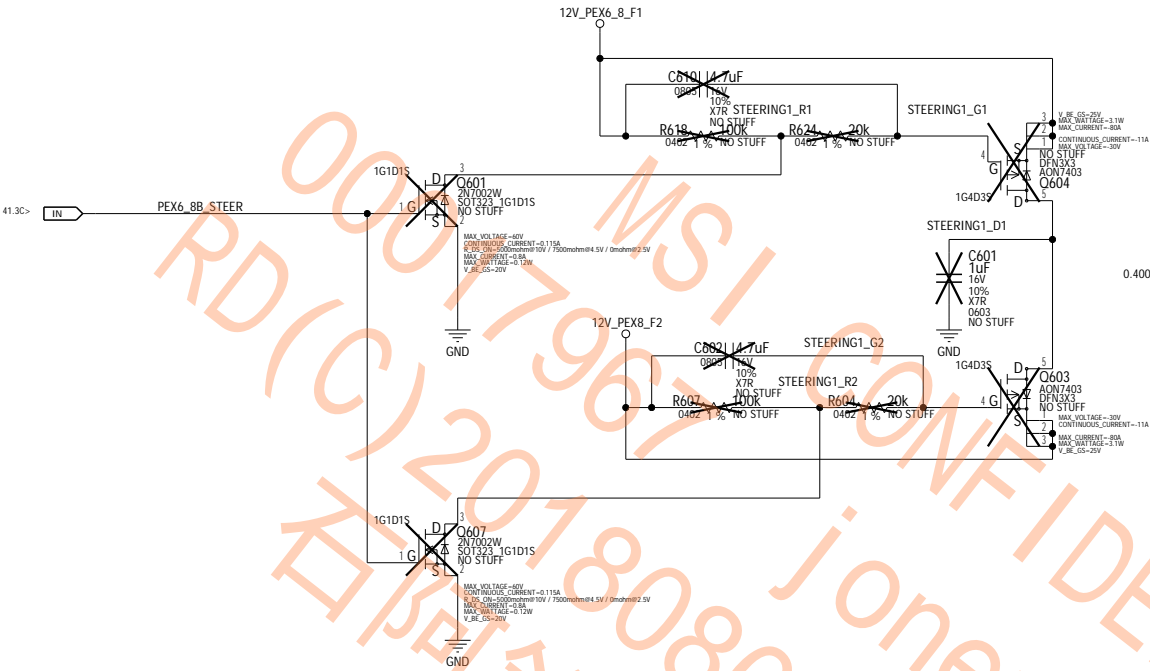


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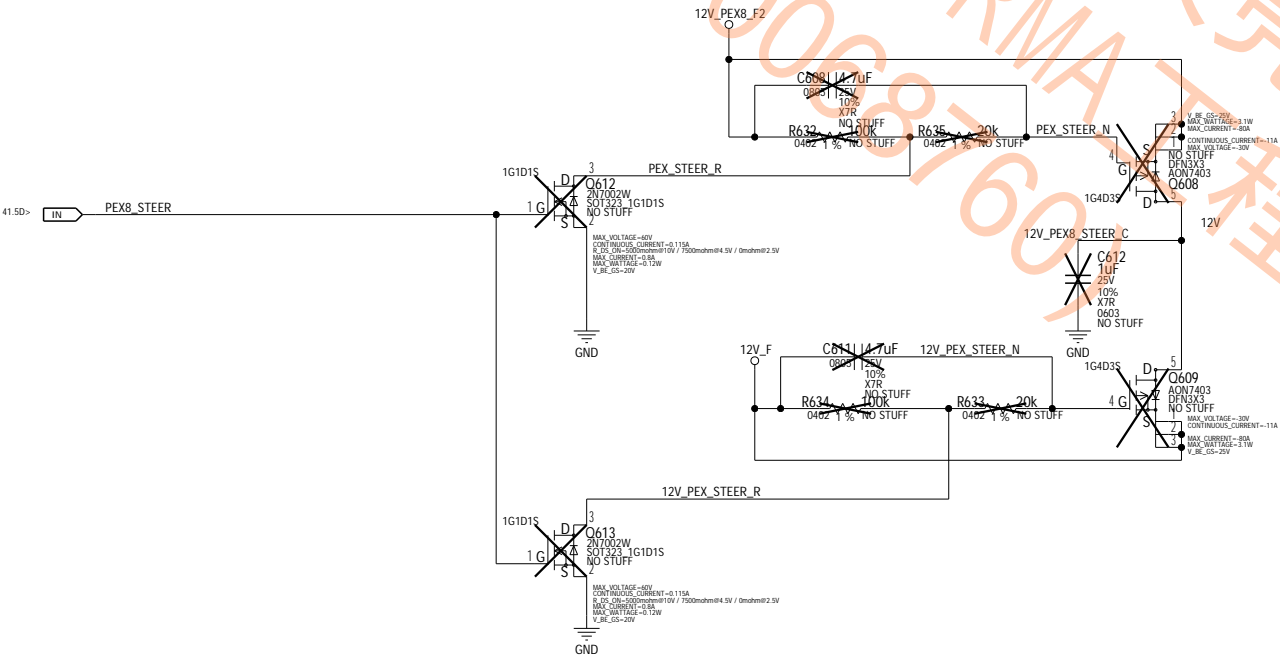
PCB REV	PG180-A02	PAGE	41 OF 54
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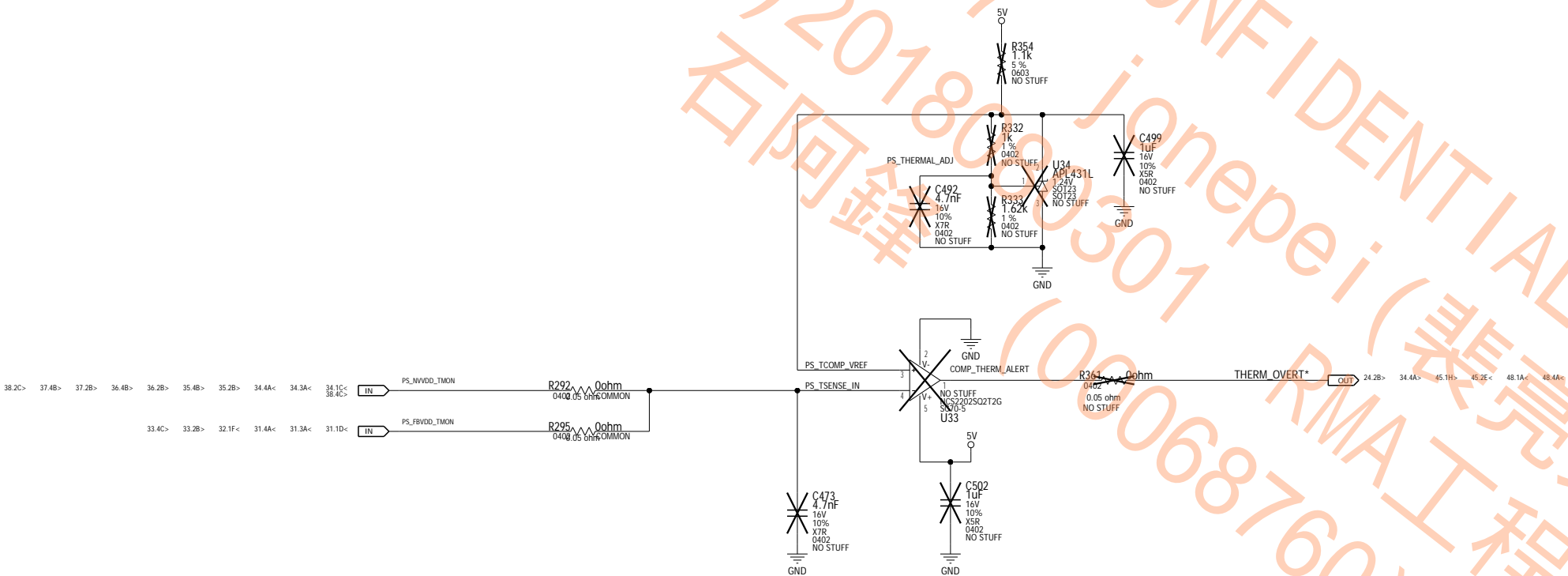
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

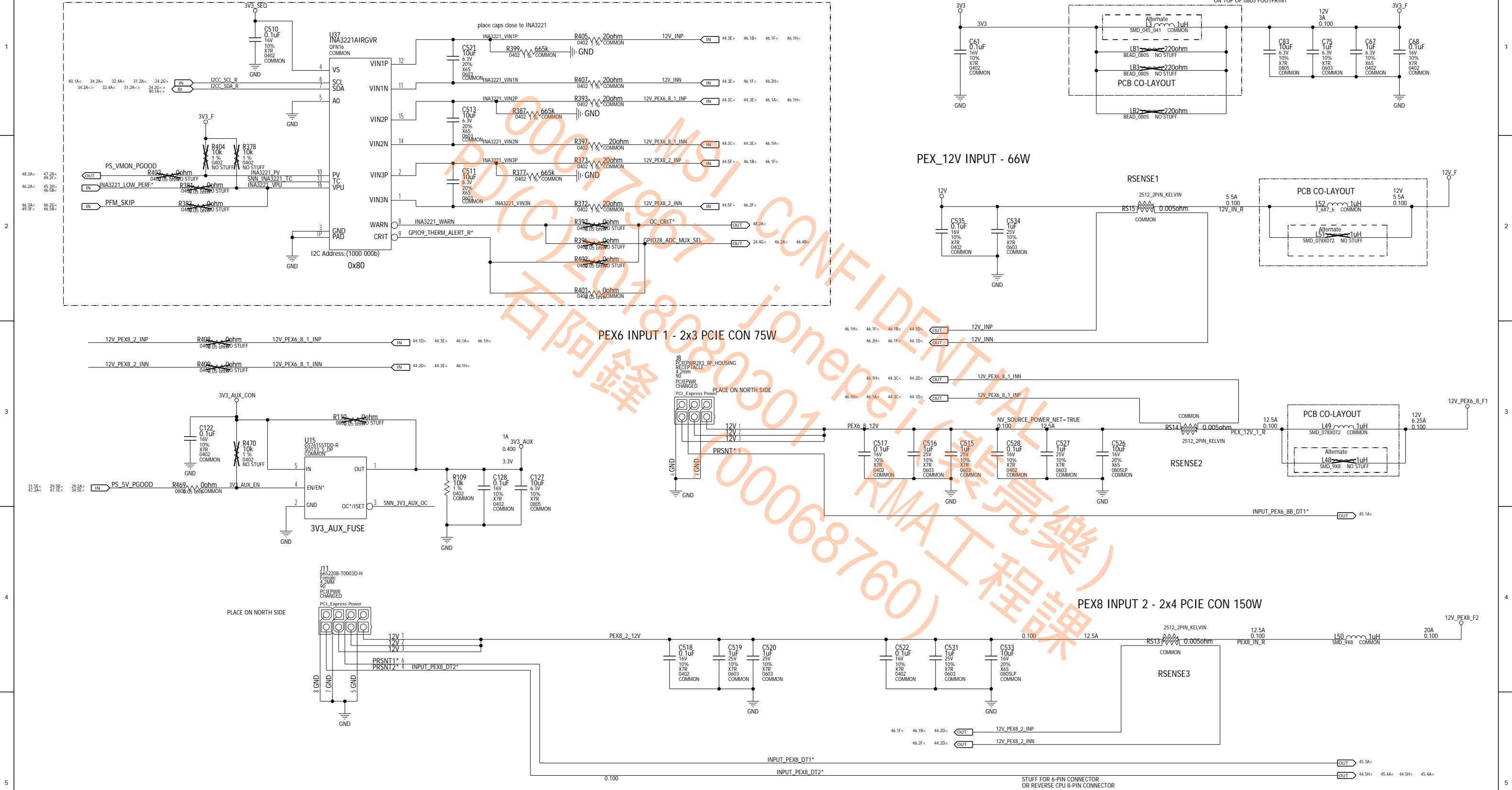


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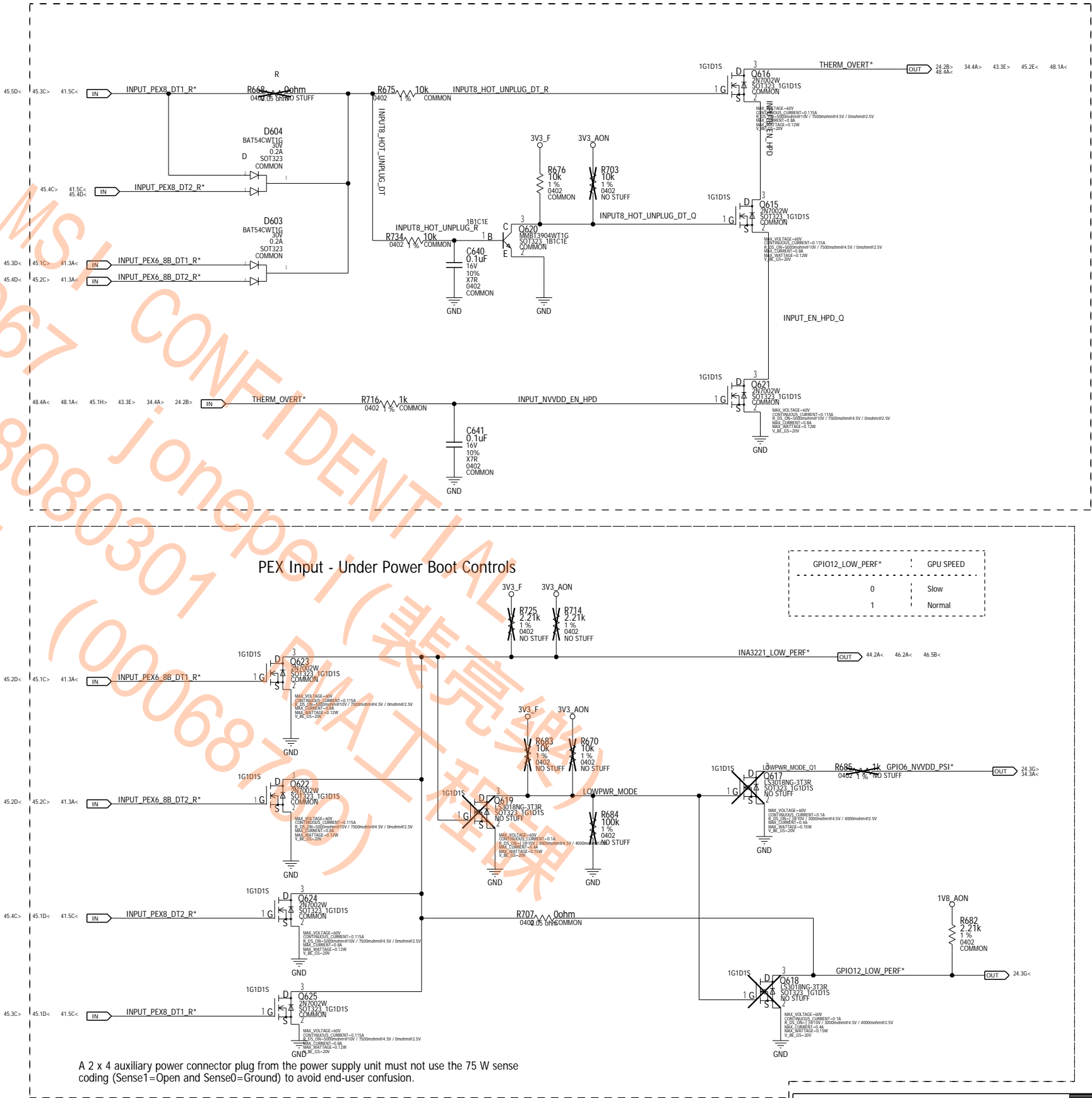
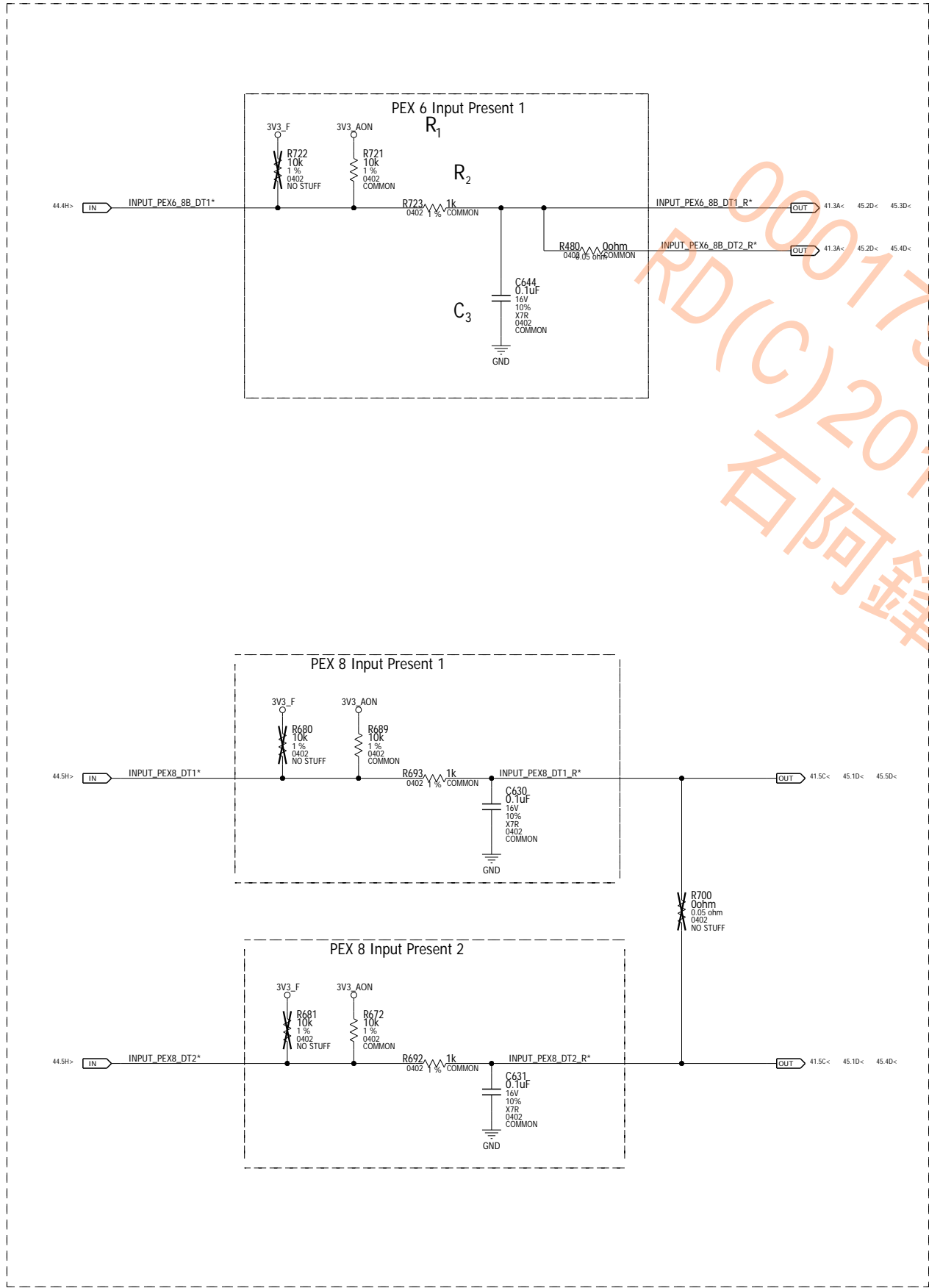


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PAGE 44: PS: Inputs, Filtering, and Monitoring



PAGE 45: PS: Current Steering, Hot Unplug Detect



A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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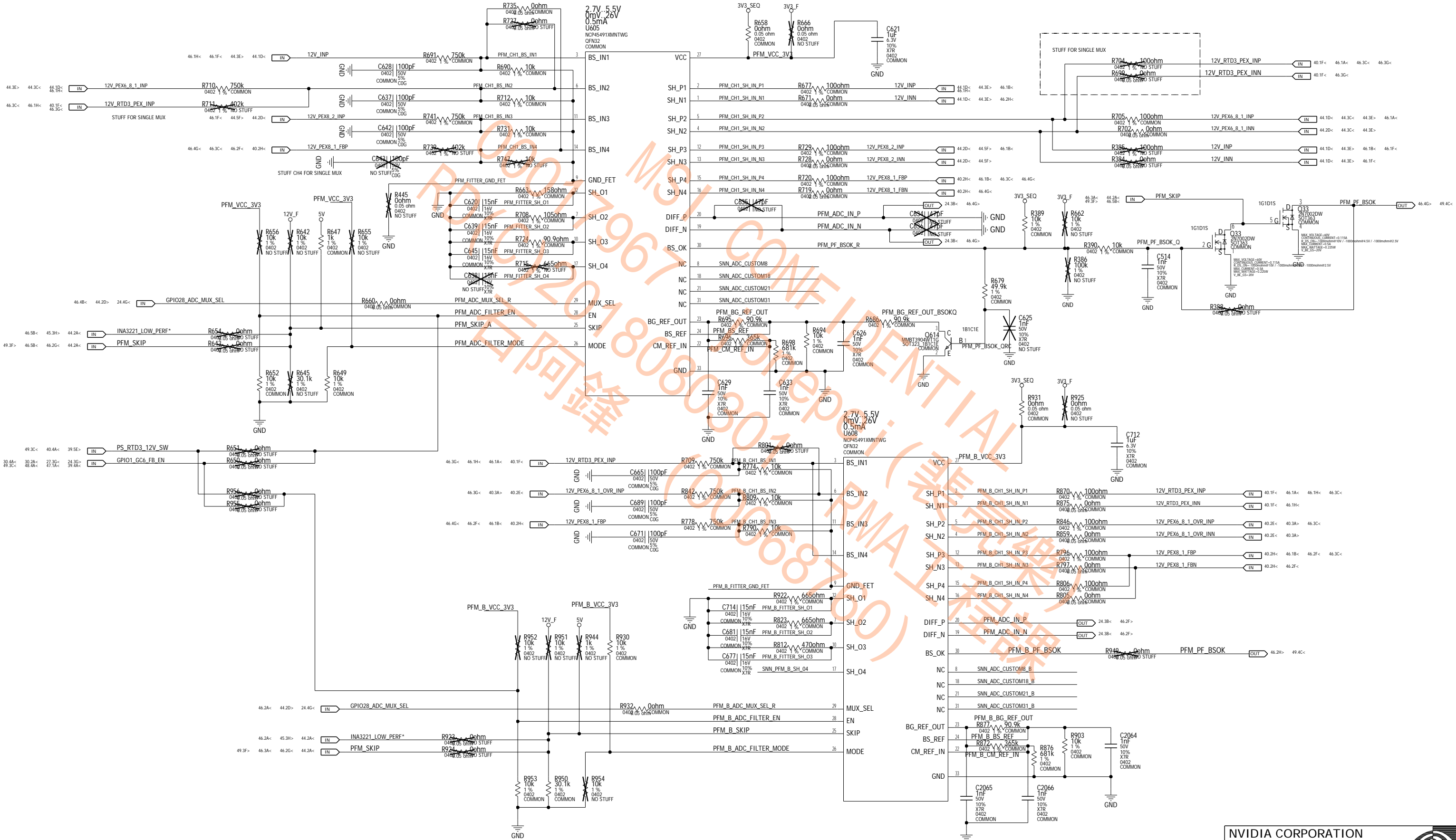


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PAGE46; PS: Pre-Filter

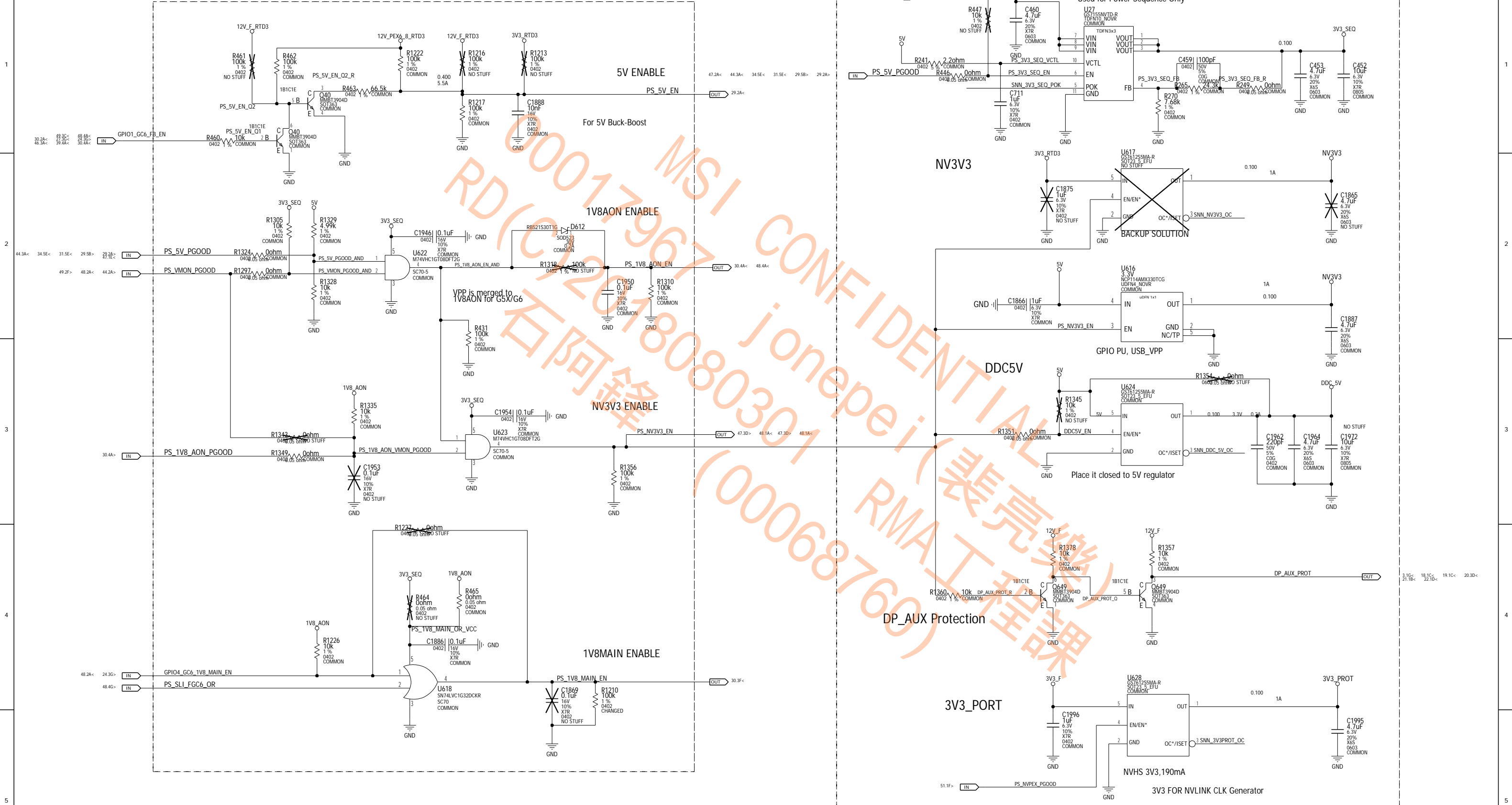
STUFF IF USING 2XMUX



ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PS: PRE-FILTER

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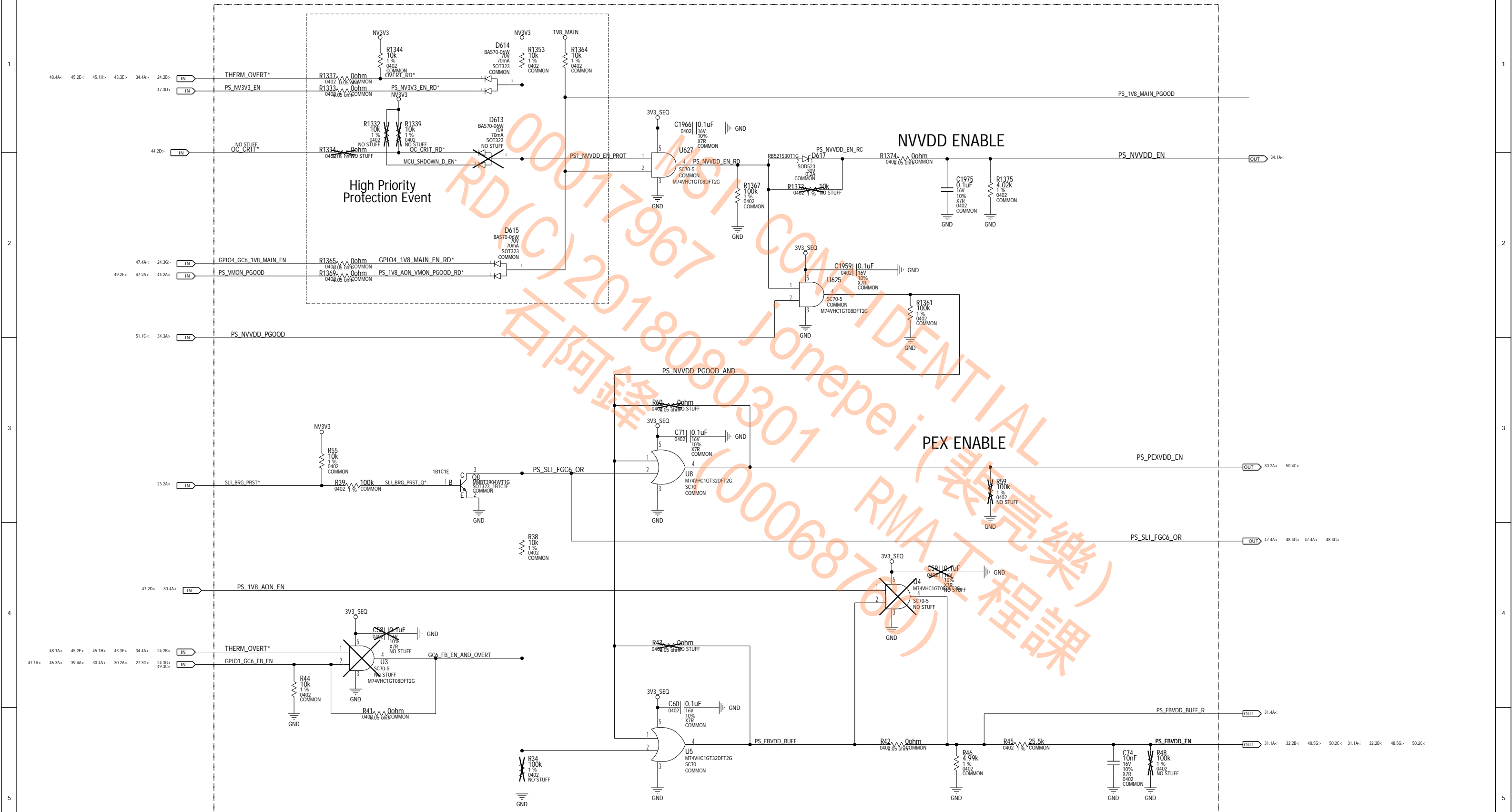
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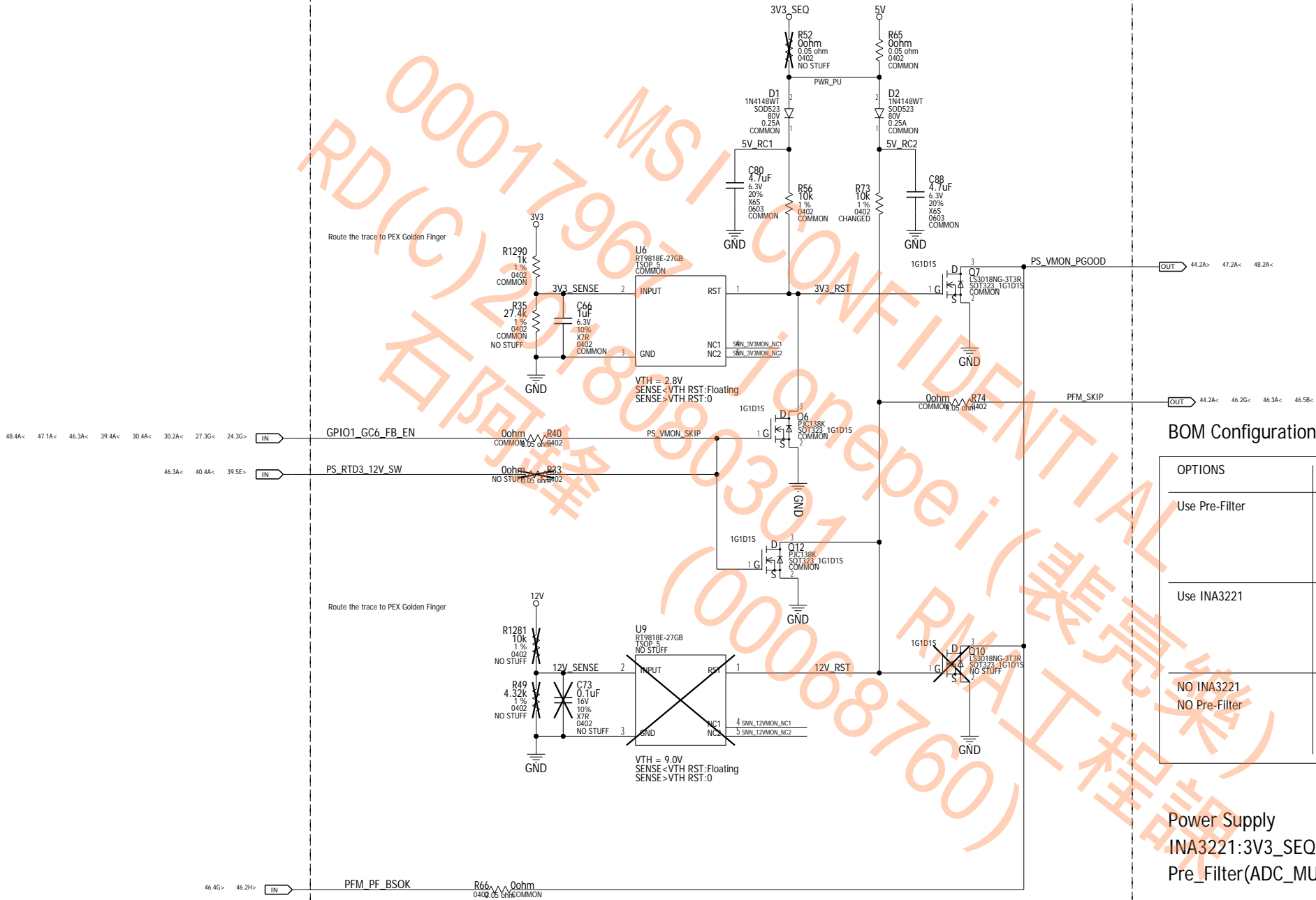
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PCIE Voltage Monitor



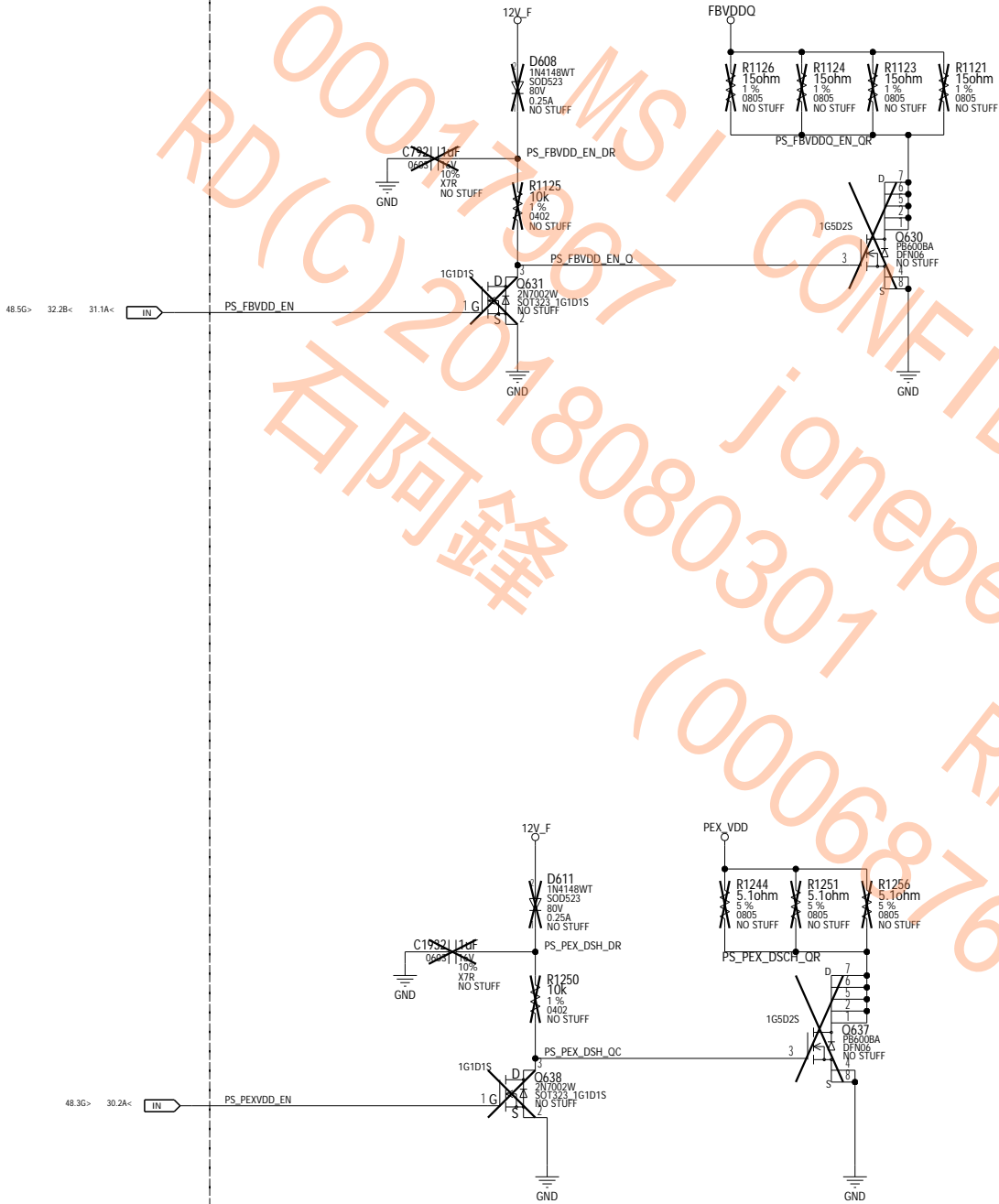
BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply
INA3221:3V3_SEQ
Pre_Filter(ADC_MUX):3V3(PEX)

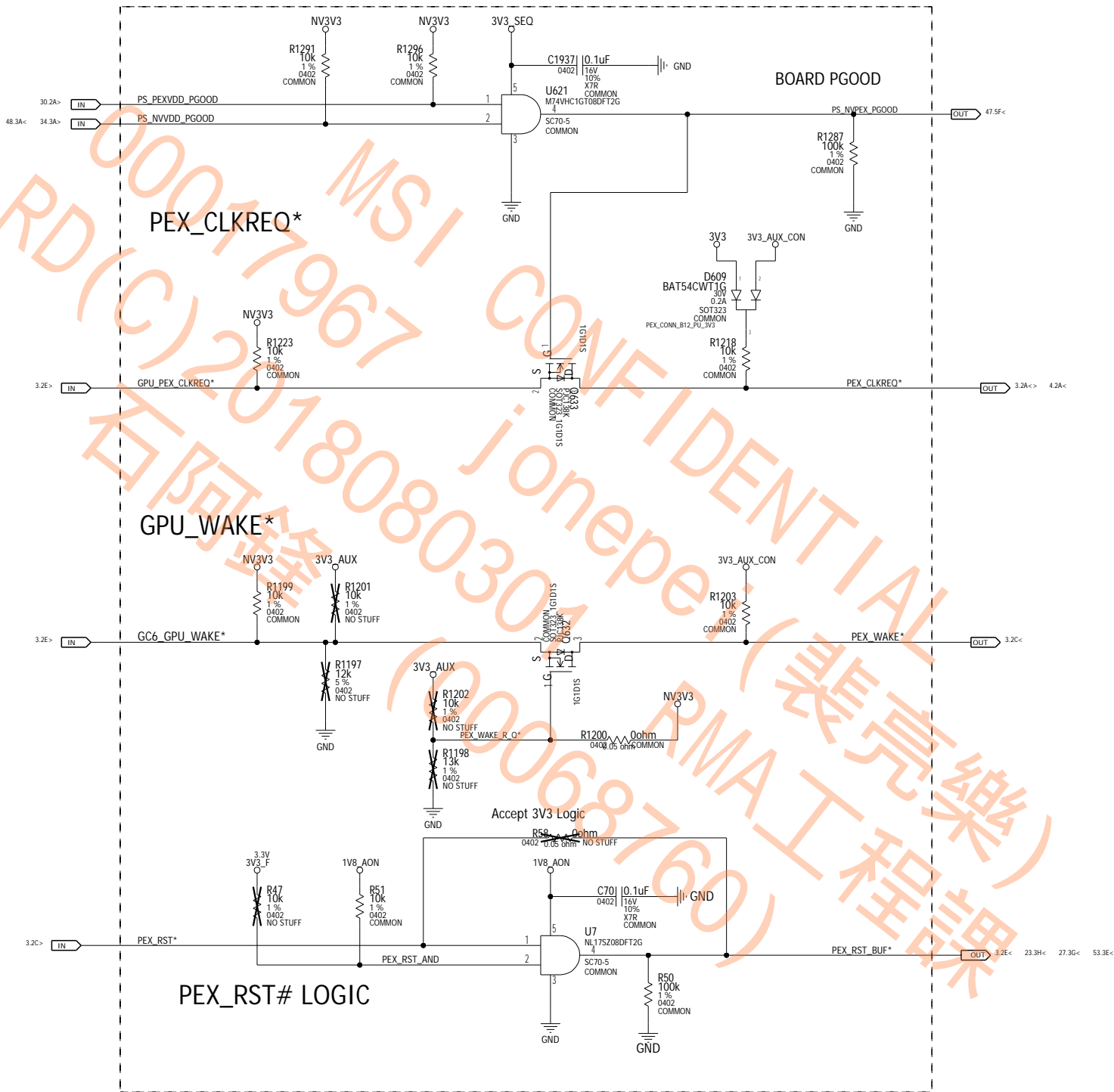
Dual Pre-Filter case:
Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSKOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW



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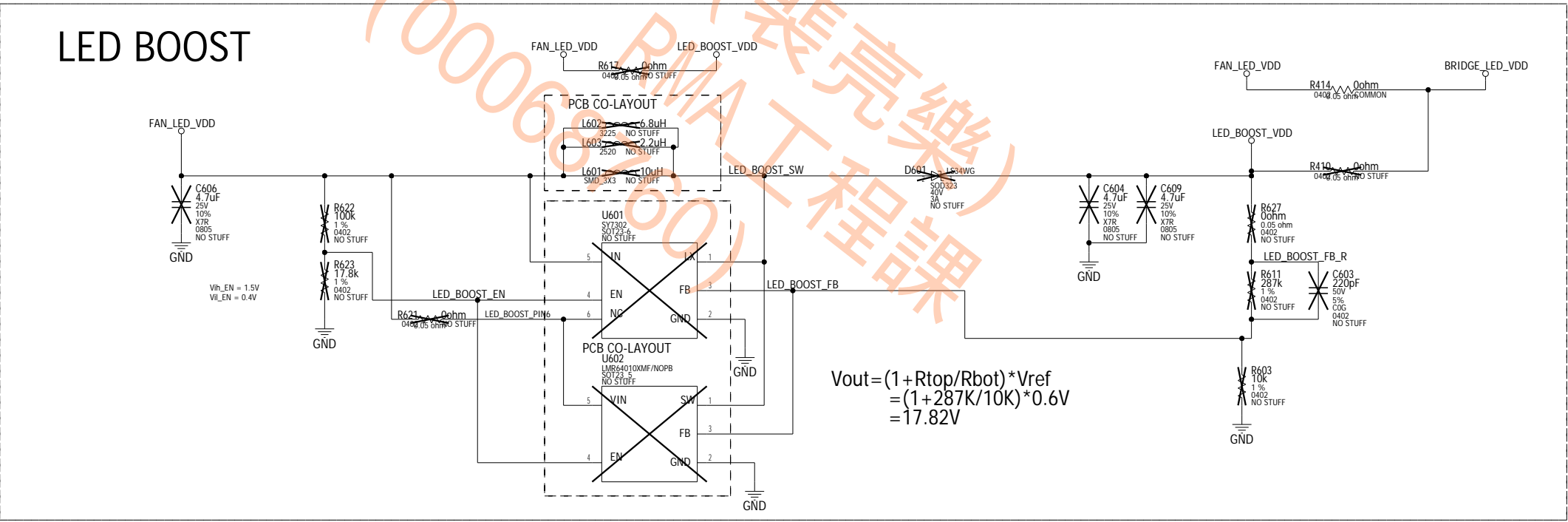
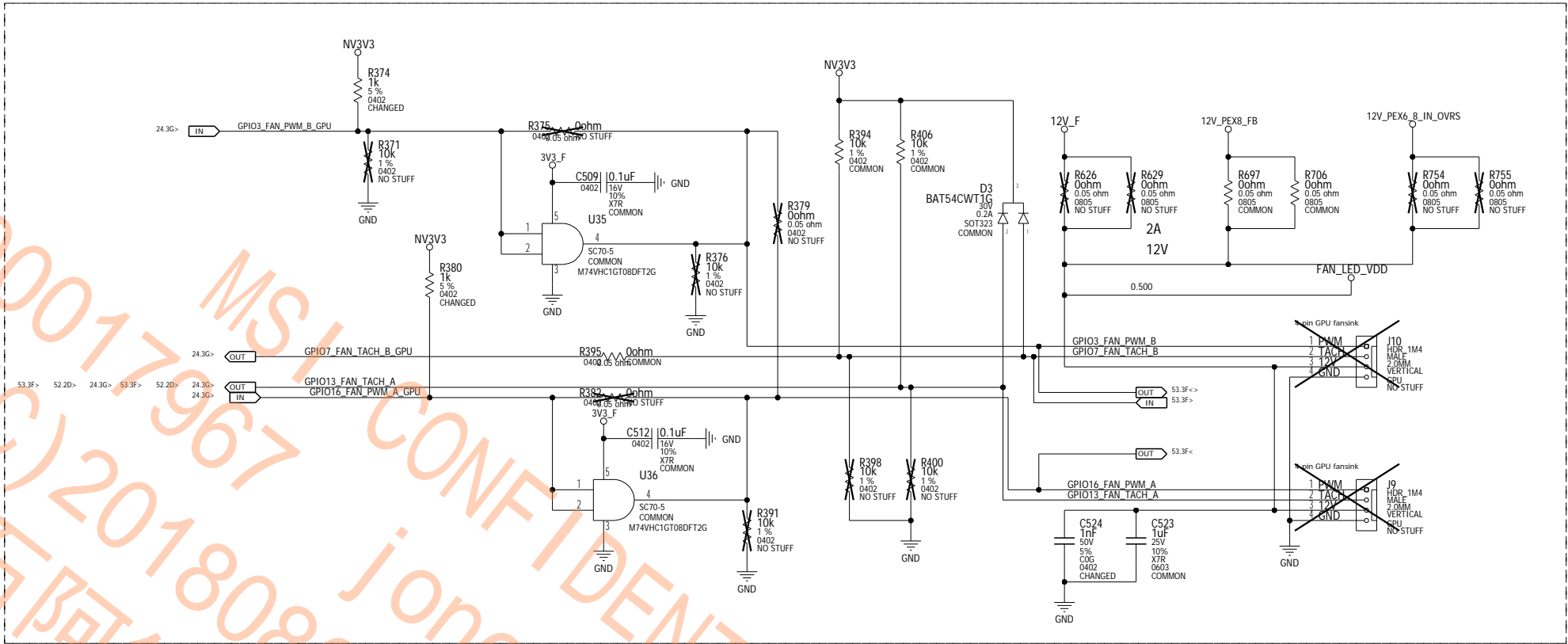
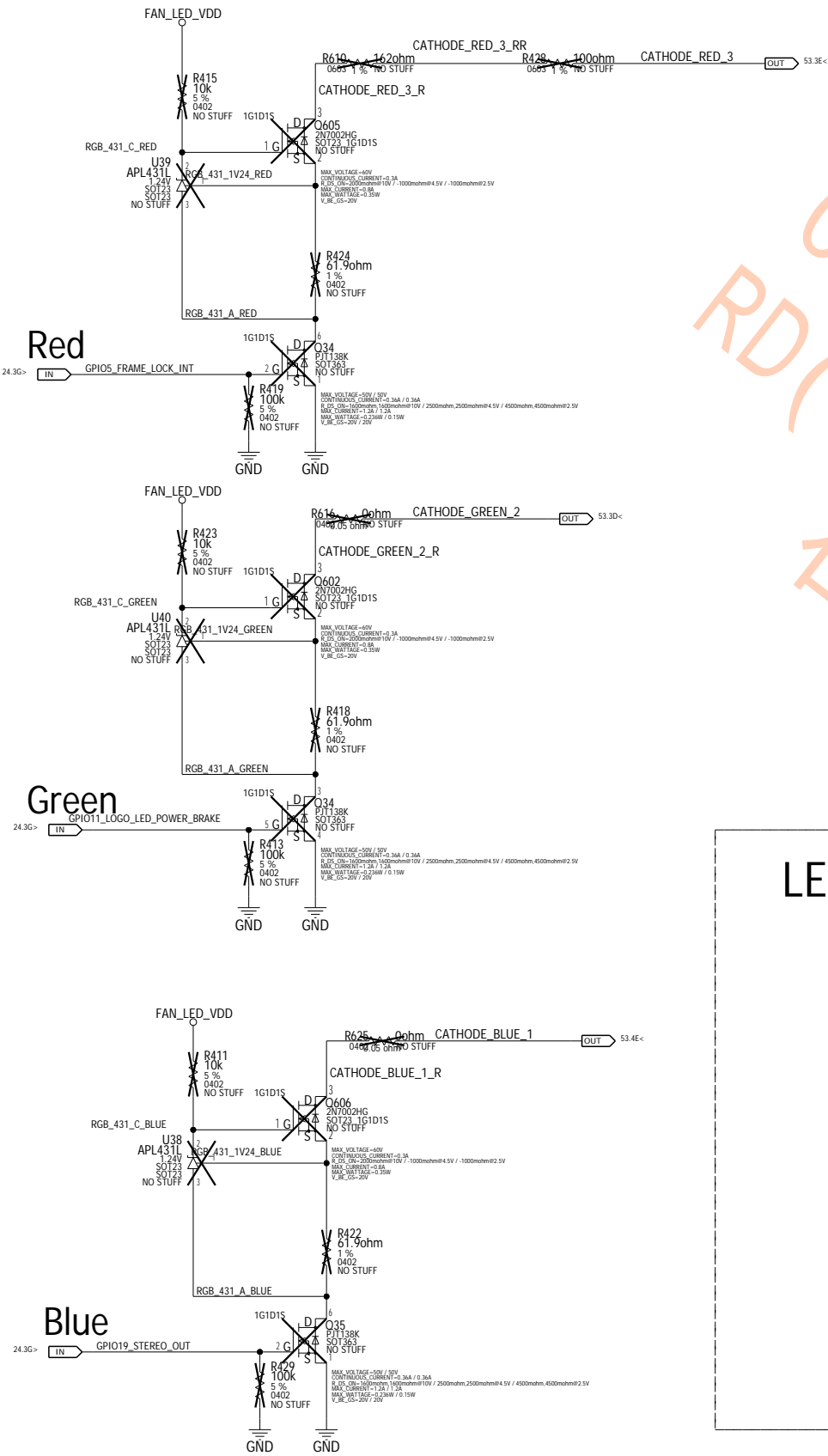
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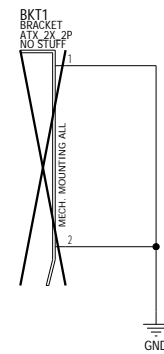
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PAGE 52: LED & FAN HEADERS



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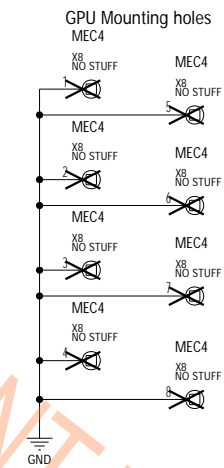


Bracket Screw

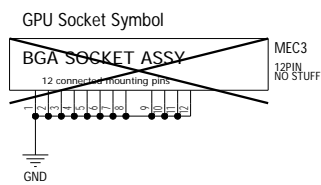
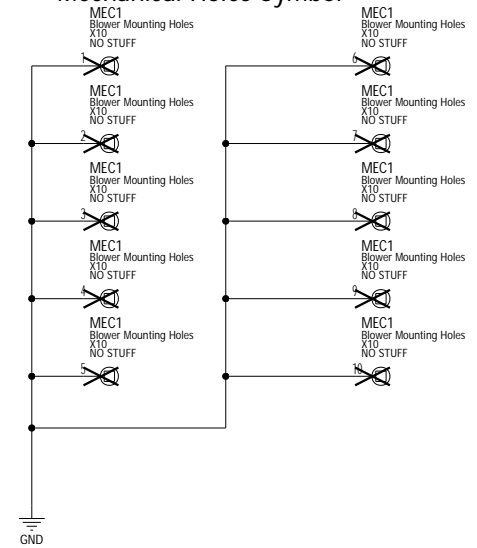
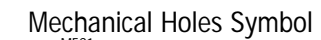
1

MEC2
PH M2.5X4.5X10MM_SCREW
STD
NO STUFF

new LF screw --155-0001-000.
ROHS screw --154-0003-700.



STIFFENER



ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	Mechanical: Bracket/Thermal Solution

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