

P561: G98, DDR2 MEMORY 32MX16/16Mx16/64MX16

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Page 15: Basenet Report

Page 16: Cref Part

REV HISTORY

History 10

96/09/27 page 08 add AV\_OUT

page 13 change Q1, Q2 to TO252

page 14 add FBVDDQ-linear block, change U2 footprint

96/09/28 page 07 change J4 footprint

page 12 add J7 (co-lay J6)

page 13 add R572 for RT9259A, R570 footprint change to 0805,

change L11, C11, C12, C31 footprint

page 14 remove PWM block

add D20, D21, C211, C212, C213, C214

96/10/01 page 14 add R210, R211

page 09 add R75~R88, R63~R69, L15~L21 for DVI (EMI\_solution)

96/10/02 page 12 add FAN Control Function

96/10/03 page 09 and netname (Between common Choke and DVI connector)

96/10/05 page 12 cnage Y501 (4 pin to 2 pin)

96/10/12 page 12 add L30, remove L10

96/10/12 baseon PCB:2.0 CIRCUIT DSN CAHNGE to PCB :1.0

ONLY CHANGE page 13 remove PWM solution, ADD linear solutin

remove C301~~C308 ( EMI solution for FBVDDQ)

96/10/17 page 11 add CABLE and PCB

96/10/18 page 14 add C301~~C308 ( EMI solution for FBVDDQ)

History 20

96/10/03 page 14 remove FBVDDQ-LINNEAR block, add FBVDDQ-PWM function

change L15 footprint as CHK4417C\_3R3S01, change C35 footprint

96/10/05 page 12 cahnge Y501 (4pin to 2 pin)

96/10/09 page 11 add FM1~~ FM6 for Fiducial Point

add U301~~U306 for EMI

page 13 add C309 for EMI

page 14 add C301~~C308, C310~~C312 for EMI

96/10/10 page 13 add L30


96/10/11 page 13 remove L10

96/10/17 page 11 add cable

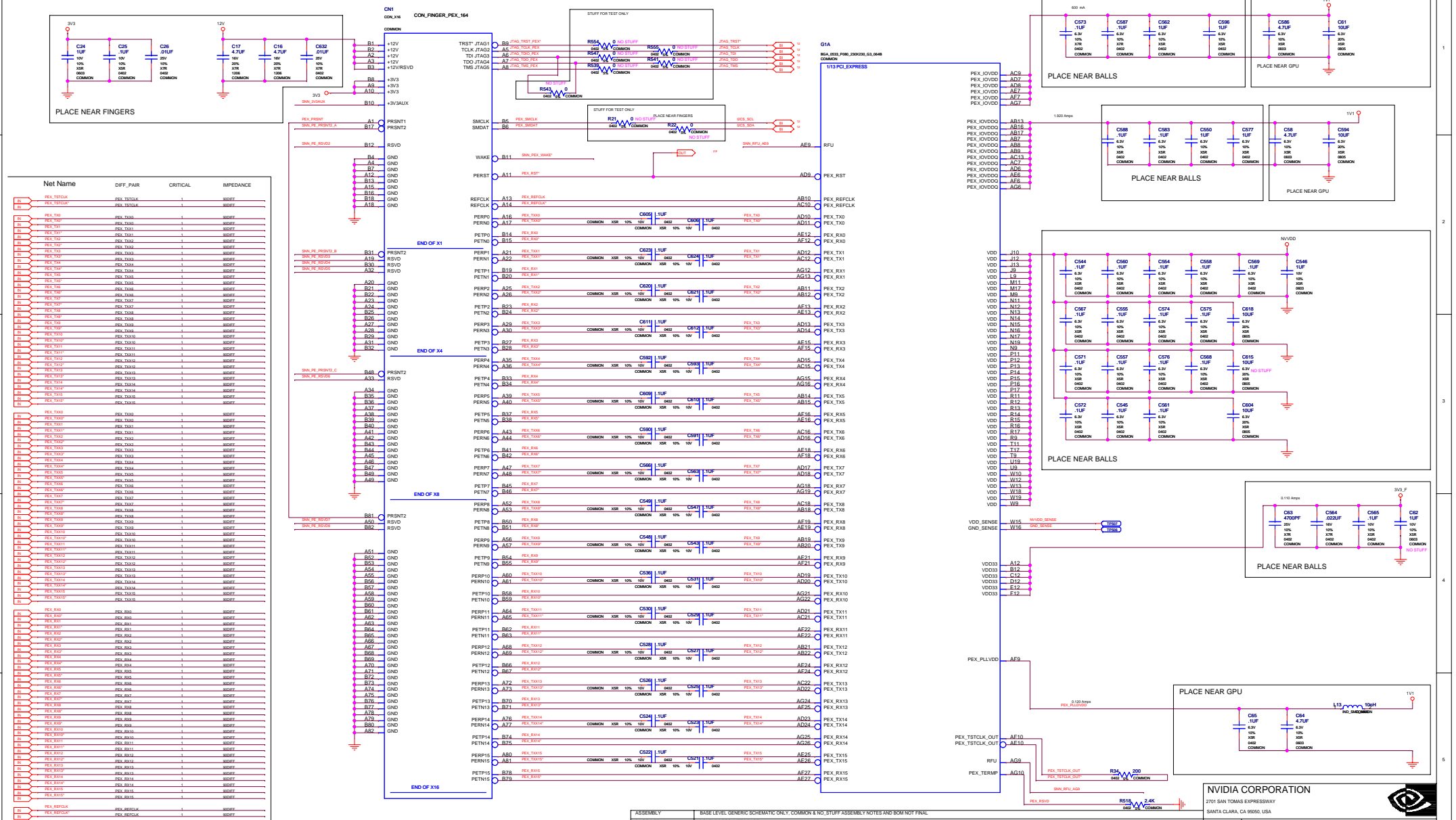
REV	VARIANT	WV/PN	ASSEMBLY
0	BASE	600-10561-xxxx-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10561-0000-100	P561: G98-300, 64 BIT DDR2 16Mx16 MEMORY, VGA+DVI+Hdout
2	SKU0001	600-10561-0001-100	P561: G98-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+Hdout
3	SKU0987	600-10561-0987-100	P561: G98-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+HDOUT
4	SKU0987	600-10561-0987-200	P561: G98-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+HDOUT
5	SKU0001	600-10561-0001-200	P561: G98-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+HDOUT
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P561 Overview

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## PCI Express Interface



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PAGE DETAIL	PCI EXPRESS INTERFACE

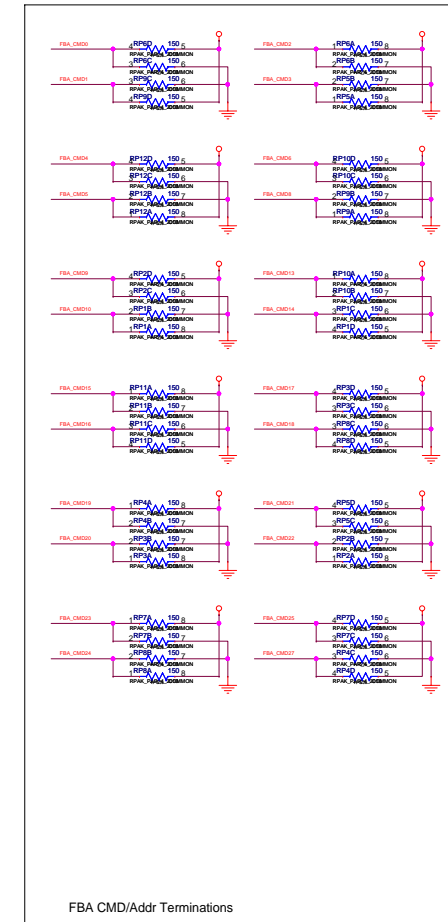
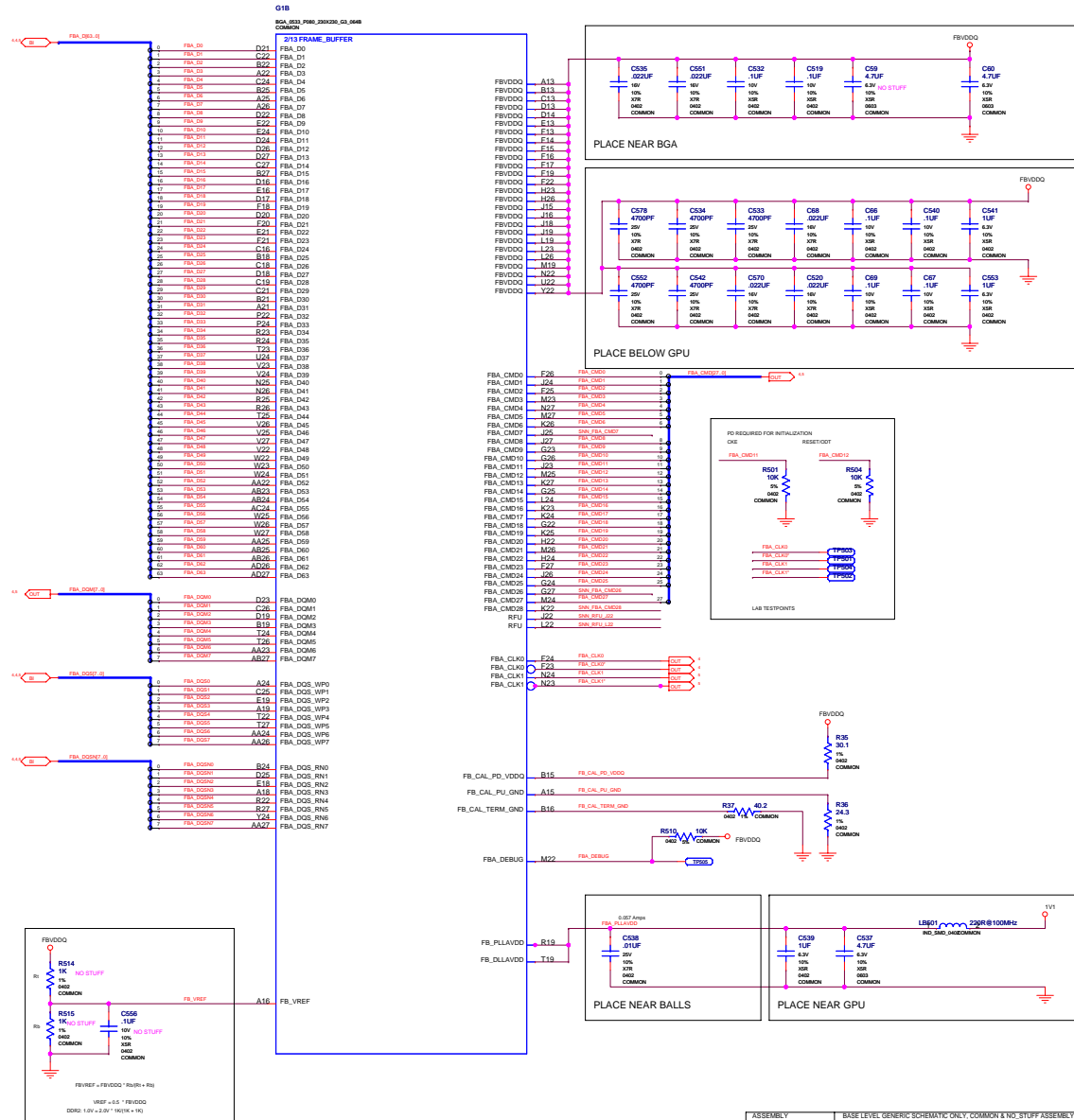
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## Frame Buffer Interface



### FBA CMD/Addr Terminations

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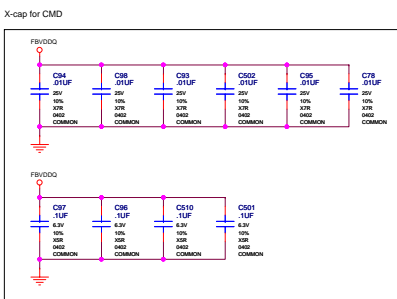
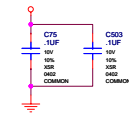
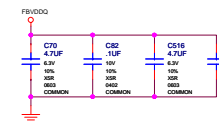
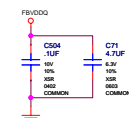
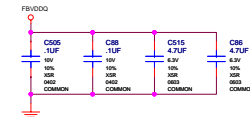
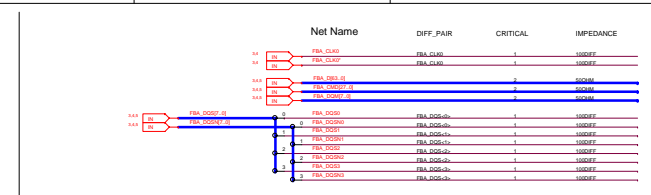
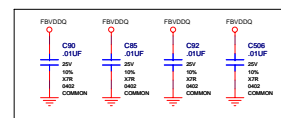
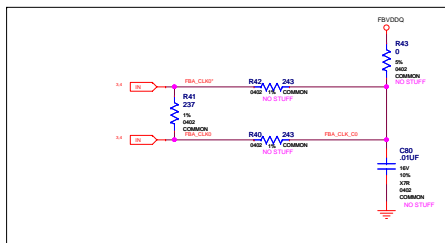
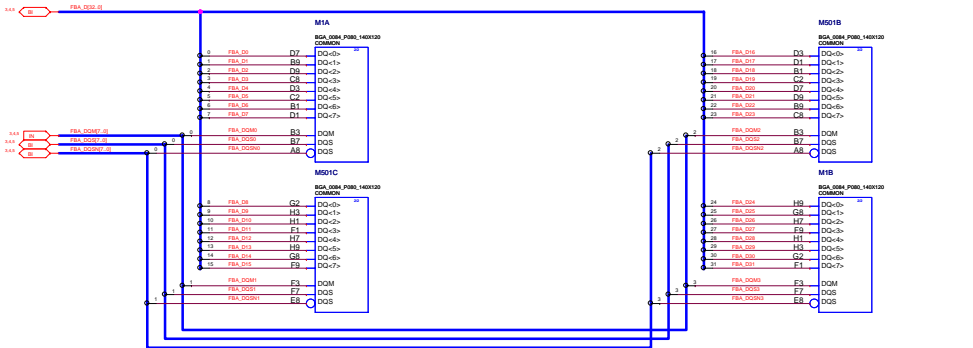
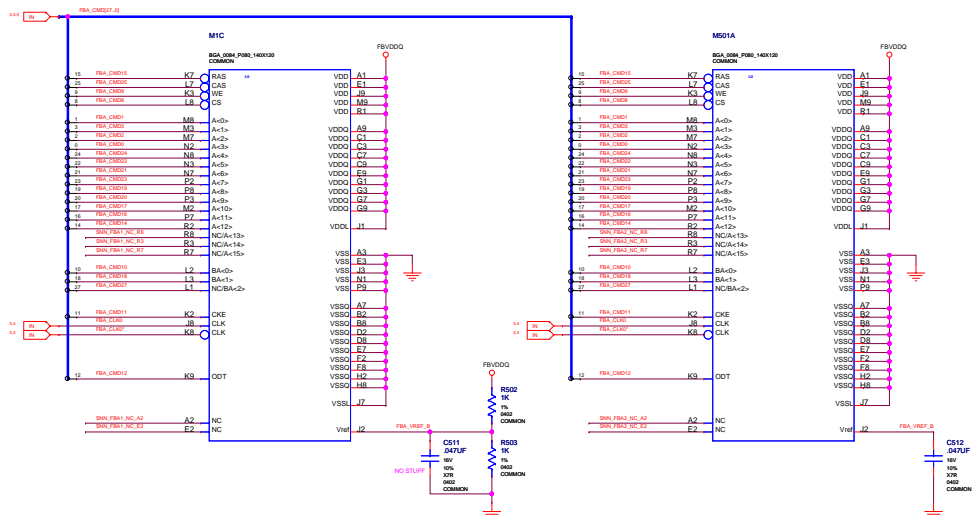
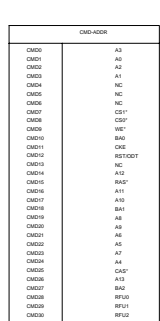
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PAGE DETAIL	Frame Buffer Interface

## Memory 1st Bank 0..31

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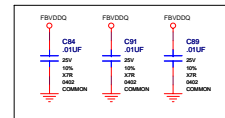
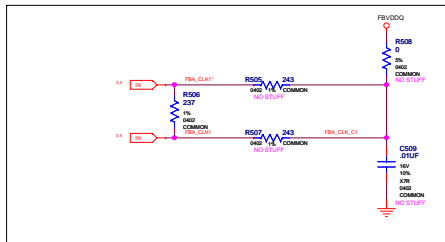
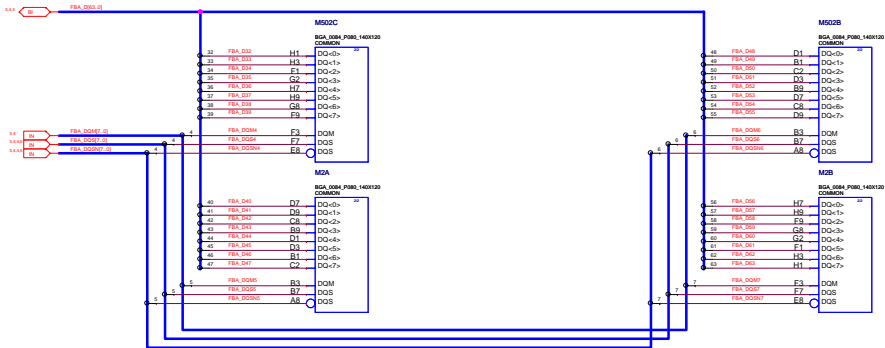
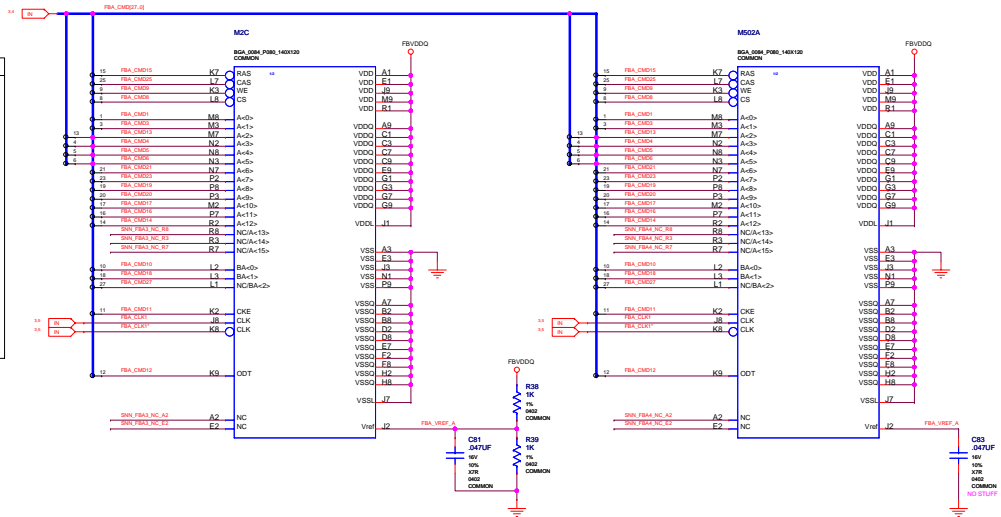
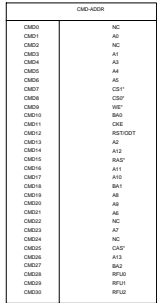


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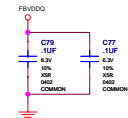
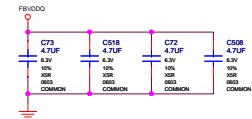
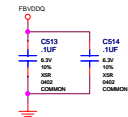
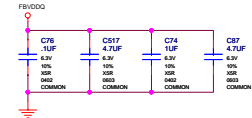
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PAGE DETAIL	Memory 1st Bank 0.31

Memory 1st Bank 32..63



	Net Name	DIFF_PAIR	CRITICAL	IMPEDANCE
0.0	FBA_CLK1	FBA_CLK1	1	100PFF
0.0	FBA_CLK2	FBA_CLK2	1	100PFF
0.0	FBA_CLK3	FBA_CLK3	1	100PFF
0.0	FBA_CLK00E0	FBA_CLK00E0	1	100PFF
0.0	FBA_CLK00E1	FBA_CLK00E1	1	100PFF
0.0	FBA_CLK00E2	FBA_CLK00E2	1	100PFF
0.0	FBA_CLK00E3	FBA_CLK00E3	1	100PFF
0.0	FBA_CLK00E4	FBA_CLK00E4	1	100PFF
0.0	FBA_CLK00E5	FBA_CLK00E5	1	100PFF
0.0	FBA_CLK00E6	FBA_CLK00E6	1	100PFF
0.0	FBA_CLK00E7	FBA_CLK00E7	1	100PFF
0.0	FBA_CLK00E8	FBA_CLK00E8	1	100PFF
0.0	FBA_CLK00E9	FBA_CLK00E9	1	100PFF
0.0	FBA_CLK00F0	FBA_CLK00F0	1	100PFF
0.0	FBA_CLK00F1	FBA_CLK00F1	1	100PFF
0.0	FBA_CLK00F2	FBA_CLK00F2	1	100PFF
0.0	FBA_CLK00F3	FBA_CLK00F3	1	100PFF
0.0	FBA_CLK00F4	FBA_CLK00F4	1	100PFF
0.0	FBA_CLK00F5	FBA_CLK00F5	1	100PFF
0.0	FBA_CLK00F6	FBA_CLK00F6	1	100PFF
0.0	FBA_CLK00F7	FBA_CLK00F7	1	100PFF
0.0	FBA_CLK00F8	FBA_CLK00F8	1	100PFF
0.0	FBA_CLK00F9	FBA_CLK00F9	1	100PFF
0.0	FBA_CLK0100	FBA_CLK0100	1	100PFF
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0.0	FBA_CLK0114	FBA_CLK0114	1	100PFF
0.0	FBA_CLK0115	FBA_CLK0115	1	100PFF
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0.0	FBA_CLK0123	FBA_CLK0123	1	100PFF
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0.0	FBA_CLK0145	FBA_CLK0145	1	100PFF
0.0	FBA_CLK0146	FBA_CLK0146	1	100PFF</



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PAGE DETAIL	Memory 1st Bank 32..63

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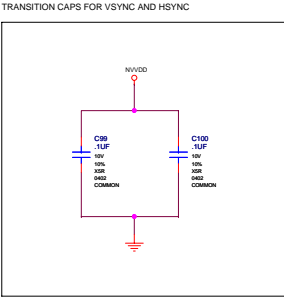
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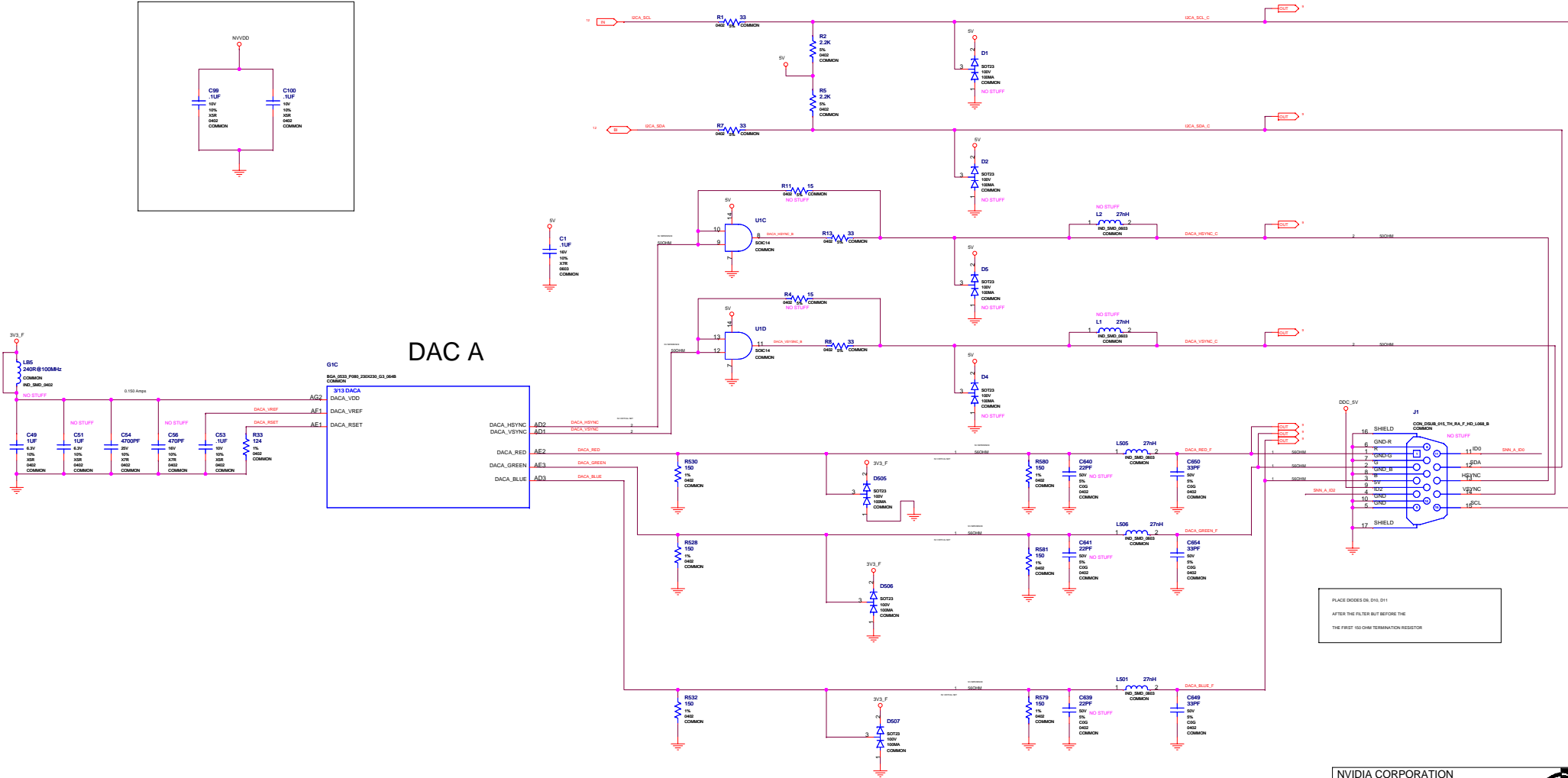
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DACA, Slim DB15 Connector



DAC A



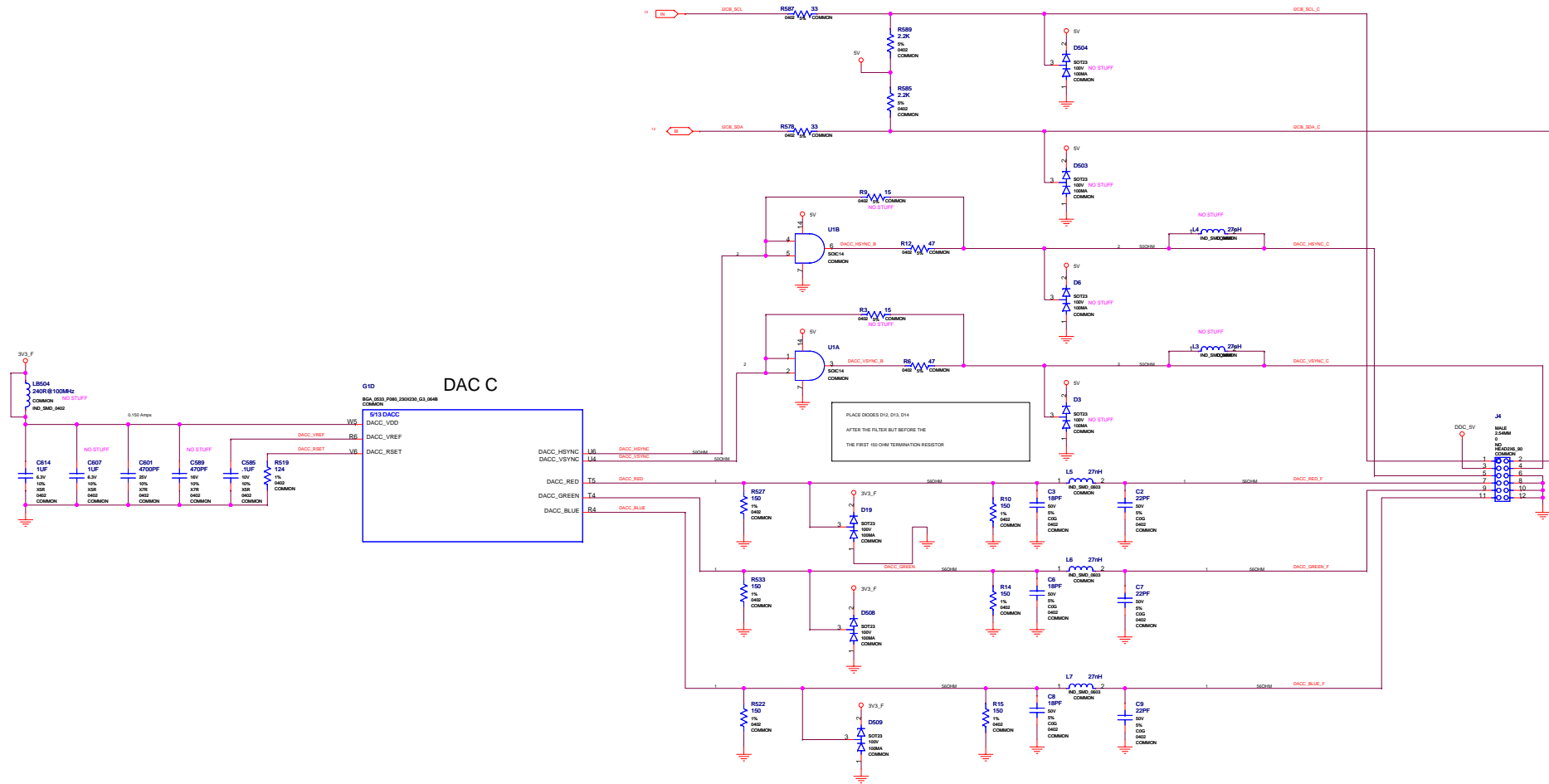
PLACE DIODES D6, D10, D11  
AFTER THE FILTER BUT BEFORE THE  
THE FIRST 150 OHM TERMINATION RESISTOR

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PAGE DETAIL	DACA, Slim DB15 Connector

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## DAC C,2x6 Header



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PAGE DETAIL	DACC_2x6 Header

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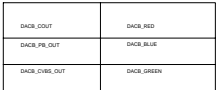


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A



AV\_OUT NO STUFF

2 3 4

1 DACB\_CV1B3\_OUT

JACK+RCA-D3-SB-YL

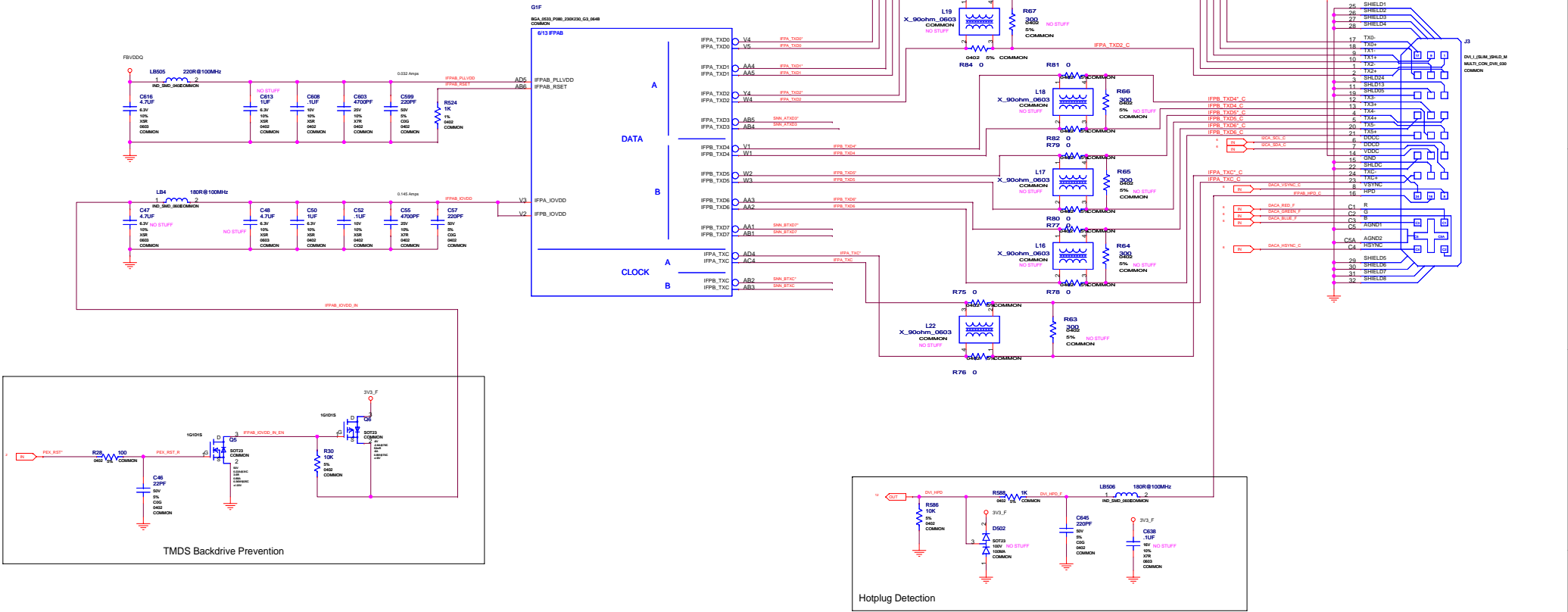
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	VIDEO CONNECTORS: MiniDIN

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TMDS Interface



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS Interface

NVIDIA CORPORATION

3701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA

NV\_PN

600-10561-xxxx-100 D

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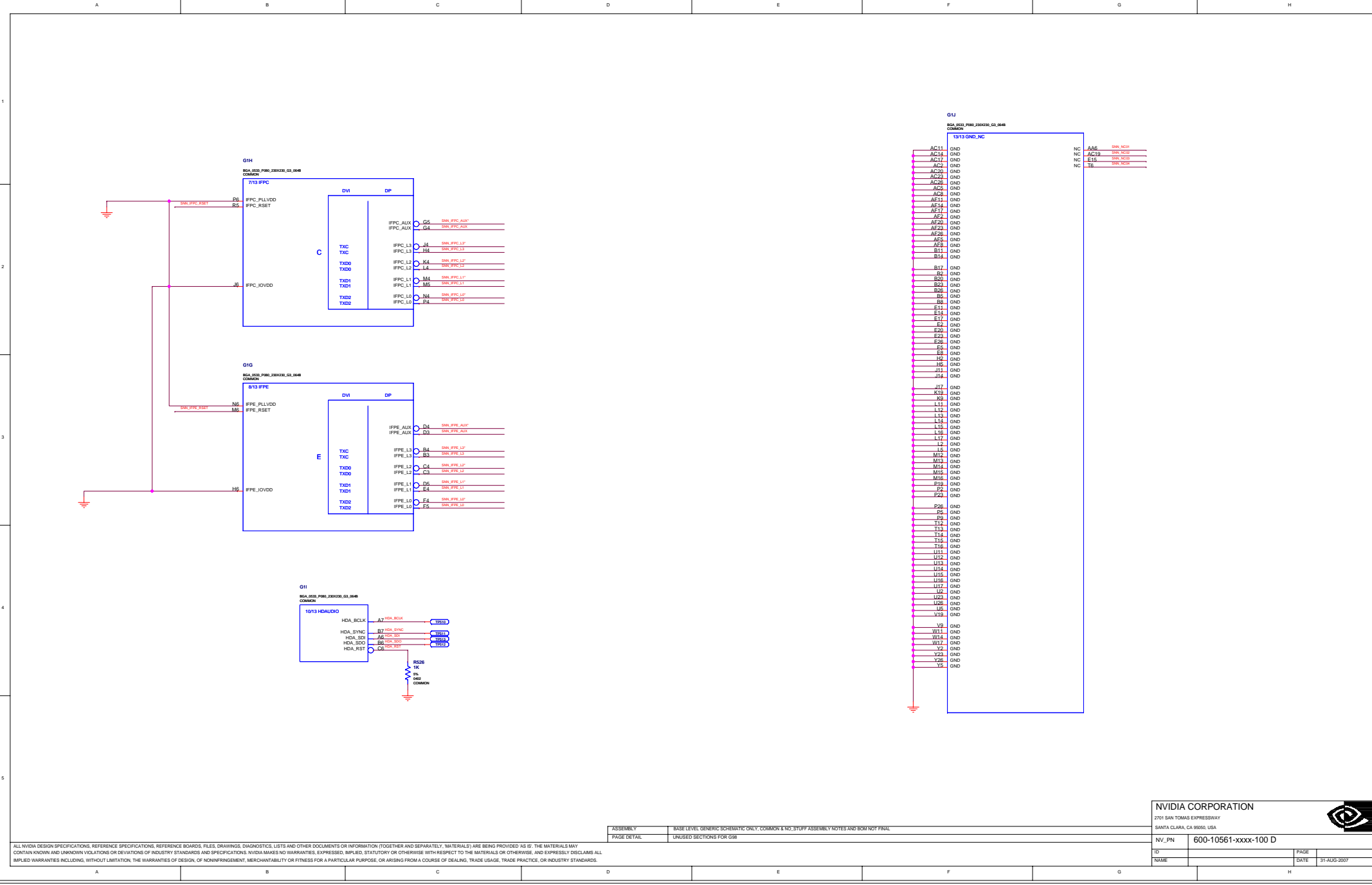
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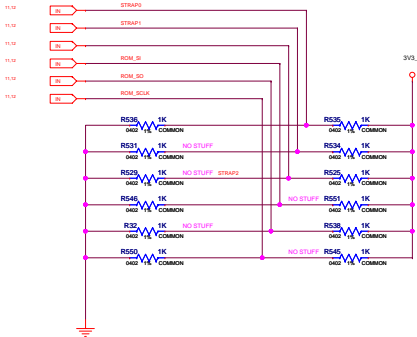
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Straps, Mechanical Parts

MULTI LEVEL STRAPS



Each strap pin represents a 4 bit value  
Pullup or Pulldown configures the MSB  
Resistor Value determines the 3 LSBs  
Resistor range is R\*n  
where n is 0-9 and R is 5K ohm.

Resistor Value	MultiLevel	Tied to VCC	Tied to Ground
3 Kohna	Y	1000	0000
4 Kohna	Y	1001	0001
12 Kohna	Y	1010	0010
24 Kohna	Y	1011	0011
48 Kohna	Y	1100	0100
96 Kohna	Y	1101	0101
192 Kohna	Y	1110	0110
384 Kohna	Y	1111	0111
2 Kohna*	N	None	None

MULTILEVEL MODE	
STRAP_CAL_PUL_GND0 (R512) = 40K	
STRAP_CAL_PUL_GND1 (R513) = 40K	
SIGNAL	FUNCTION
STRAP0	USER0[0]
STRAP1	3G0_PAND0[0], LUT_ADDR[0]
STRAP2	3G0_PAND0[1], LUT_ADDR[1]
ROM_SCL	POL_DEV0[0]
ROM_SI	POL_DEV0[1], SUB_VENDOR, SLOT_ID, CFG, PEX_PUL_EN, TERN10
ROM_SO	RAMCFG[0]
	KOLK_377, TYNODE0[0]

BRINGUP BINARY MODE	
STRAP_CAL_PUL_GND0 (R512) = NO STUFF	
STRAP_CAL_PUL_GND1 (R513) = NO STUFF	
SIGNAL	FUNCTION
STRAP0	3G0_PAND0[0], LUT_ADDR[0]
STRAP1	3G0_PAND0[1], LUT_ADDR[1]
STRAP2	3G0_PAND0[2], LUT_ADDR[2]
ROM_SCL	3G0_PAND0[3], LUT_ADDR[3]
ROM_SI	POL_DEV0[0]
ROM_SO	SUB_VENDOR
	KOLK_377

PRODUCTION BINARY MODE	
STRAP_CAL_PUL_GND0 (R512) = NO STUFF	
STRAP_CAL_PUL_GND1 (R513) = 40K	
SIGNAL	FUNCTION
STRAP0	RAMCFG[0]
STRAP1	RAMCFG[1]
STRAP2	RAMCFG[2]
ROM_SCL	POL_DEV0[0]
ROM_SI	POL_DEV0[1]
ROM_SO	KOLK_377

STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz (MULTI LEVEL) R511= 40K, R512=40K

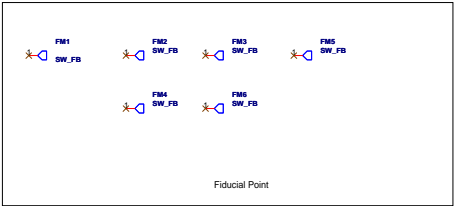
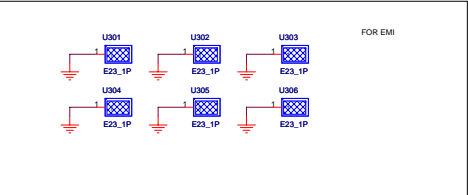
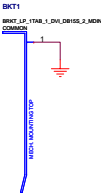
3V3_F	GND	PNOSIGNAL	FUNCTION
5K	5K	STRAP0	USER0[0]
5K	5K	STRAP1	3G0_PAND0[0], LUT_ADDR[0]
25K	25K	STRAP2	POL_DEV0[0]
25K	25K	ROM_SCL	POL_DEV0[1], SUB_VENDOR, SLOT_ID, CFG, PEX_PUL_EN, TERN10
40K	40K	ROM_SI	RAMCFG[0]
		ROM_SO	KOLK_377, TYNODE0[0]

STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz (BRINGUP BINARY) R511= NO STUFF, R512=NO STUFF

3V3_F	GND	PNOSIGNAL	FUNCTION
5K	5K	STRAP0	3G0_PAND0[0], LUT_ADDR[0]
5K	5K	STRAP1	3G0_PAND0[1], LUT_ADDR[1]
5K	5K	STRAP2	3G0_PAND0[2], LUT_ADDR[2]
5K	5K	ROM_SCL	3G0_PAND0[3], LUT_ADDR[3]
5K	5K	ROM_SI	POL_DEV0[0]
5K	5K	ROM_SO	SUB_VENDOR
			KOLK_377

STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz (PRODUCTION BINARY) R511= 40K, R512=NO STUFF

3V3_F	GND	PNOSIGNAL	FUNCTION
5K	5K	STRAP0	RAMCFG[0]
5K	5K	STRAP1	RAMCFG[1]
5K	5K	STRAP2	RAMCFG[2]
5K	5K	ROM_SCL	POL_DEV0[0]
5K	5K	ROM_SI	POL_DEV0[1]
5K	5K	ROM_SO	KOLK_377



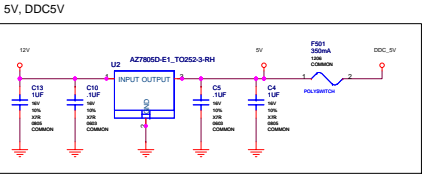
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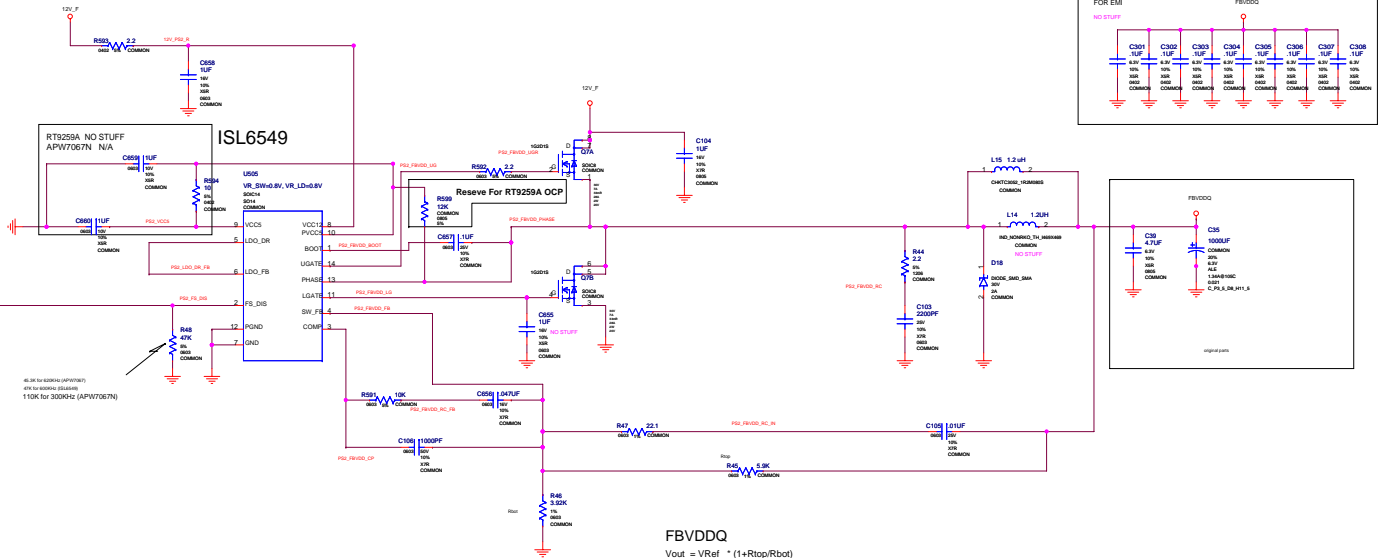
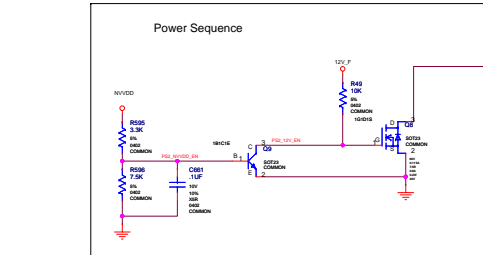
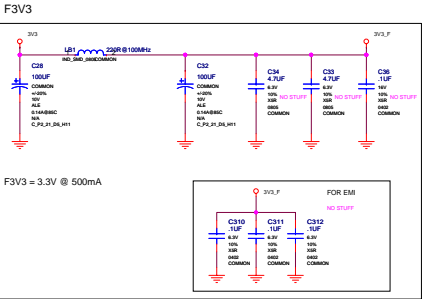




Power Supply II: 5V, DDC5V, F3V3, FBVDDQ



Net Name	MIN_LINE_WIDTH	CURRENT	VOLTAGE
5V	1.25mm	0.25A	5V
DDC5V	1.25mm	0.25A	5V
F3V3	1.25mm	1A	3.3V
FBVDDQ	1.25mm	1A	1.8V



FBVDDQ

$$V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$$

1.800V = 0.8V \* (1 + (5.9k/4.7k)) (ISL6549)  
2.000V = 0.8V \* (1 + (5.9k/3.92k)) (ISL6549)  
2.156V = 0.8V \* (1 + (5.9k/3.4k)) (ISL6549)

[illegible]

A		B		C		D		E		F		G		H	
Title: Crd Part Revision: 001 Date: Aug 15 13859 2007		C34 (4.4F) C35 (4.4E) C36 (4.5G) C37 (4.3F) C38 (4.4G) C39 (8.2B) C100 (8.2B) C103 (14.4F) C104 (14.3G) C105 (14.4G) C3 (7.4E) C107 (12.5A) C5 (14.1B) C6 (7.4E) C7 (7.4F) C8 (7.5E) C9 (7.5F) C10 (14.1A) C11 (13.2G) C12 (13.2E) C13 (14.1A) C14 (13.2E) C15 (13.2E) C16 (3.1B) C17 (2.1B) C20 (13.3F) C22 (12.2G) C23 (13.4A) C24 (2.1A) C25 (2.1A) C26 (2.1A) C27 (13.4G) C28 (14.2A) C29 (13.2F) C30 (13.3B) C31 (13.3F) C32 (14.2A) C33 (14.2B) C34 (14.2B) C35 (14.2B) C36 (14.2B) C37 (13.2F) C38 (13.2G) C39 (14.2G) C42 (12.4A) C43 (13.2G) C44 (13.2G) C45 (13.2B) C46 (8.4A) C47 (8.3A) C48 (8.3B) C49 (8.4A) C50 (8.3B) C51 (8.4A) C52 (8.3B) C53 (8.4B) C54 (8.4A) C55 (8.3C) C56 (8.4A) C57 (8.3C) C58 (12.2F) C59 (3.1G) C60 (3.1E) C61 (2.1B) C62 (2.4E) C63 (2.4E) C64 (2.5E) C65 (2.5G) C66 (3.2G) C67 (3.2E) C68 (3.2G) C69 (3.2G) C70 (8.3F) C71 (4.2G) C72 (3.3G) C73 (8.3F) C74 (3.3G) C75 (4.3F) C76 (8.2F) C77 (3.3G) C78 (14.4E) C79 (8.3F) C80 (4.3G) C81 (8.3G) C82 (4.3G) C83 (8.3E) C84 (8.5E) C85 (4.5E) C86 (4.3G) C87 (8.2G) C88 (4.2G) C89 (8.5E) C90 (4.5E) C91 (8.5E) C92 (4.5E) C93 (4.4G)		C34 (4.4F) C35 (4.4E) C36 (4.5G) C37 (4.3F) C38 (4.4G) C39 (8.2B) C100 (8.2B) C103 (14.4F) C104 (14.3G) C105 (14.4G) C3 (7.4E) C107 (12.5A) C5 (14.1B) C6 (7.4E) C7 (7.4F) C8 (7.5E) C9 (7.5F) C10 (14.1A) C11 (13.2G) C12 (13.2E) C13 (14.1A) C14 (13.2E) C15 (13.2E) C16 (3.1B) C17 (2.1B) C20 (13.3F) C22 (12.2G) C23 (13.4A) C24 (2.1A) C25 (2.1A) C26 (2.1A) C27 (13.4G) C28 (14.2A) C29 (13.2F) C30 (13.3B) C31 (13.3F) C32 (14.2A) C33 (14.2B) C34 (14.2B) C35 (14.2B) C36 (14.2B) C37 (13.2F) C38 (13.2G) C39 (14.2G) C42 (12.4A) C43 (13.2G) C44 (13.2G) C45 (13.2B) C46 (8.4A) C47 (8.3A) C48 (8.3B) C49 (8.4A) C50 (8.3B) C51 (8.4A) C52 (8.3B) C53 (8.4B) C54 (8.4A) C55 (8.3C) C56 (8.4A) C57 (8.3C) C58 (12.2F) C59 (3.1G) C60 (3.1E) C61 (2.1B) C62 (2.4E) C63 (2.4E) C64 (2.5E) C65 (2.5G) C66 (3.2G) C67 (3.2E) C68 (3.2G) C69 (3.2G) C70 (8.3F) C71 (4.2G) C72 (3.3G) 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