

REFERENCE DESIGN

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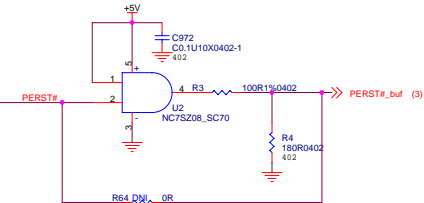
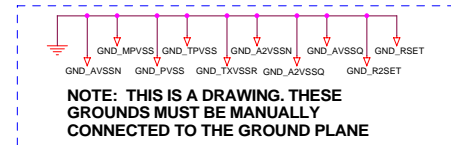
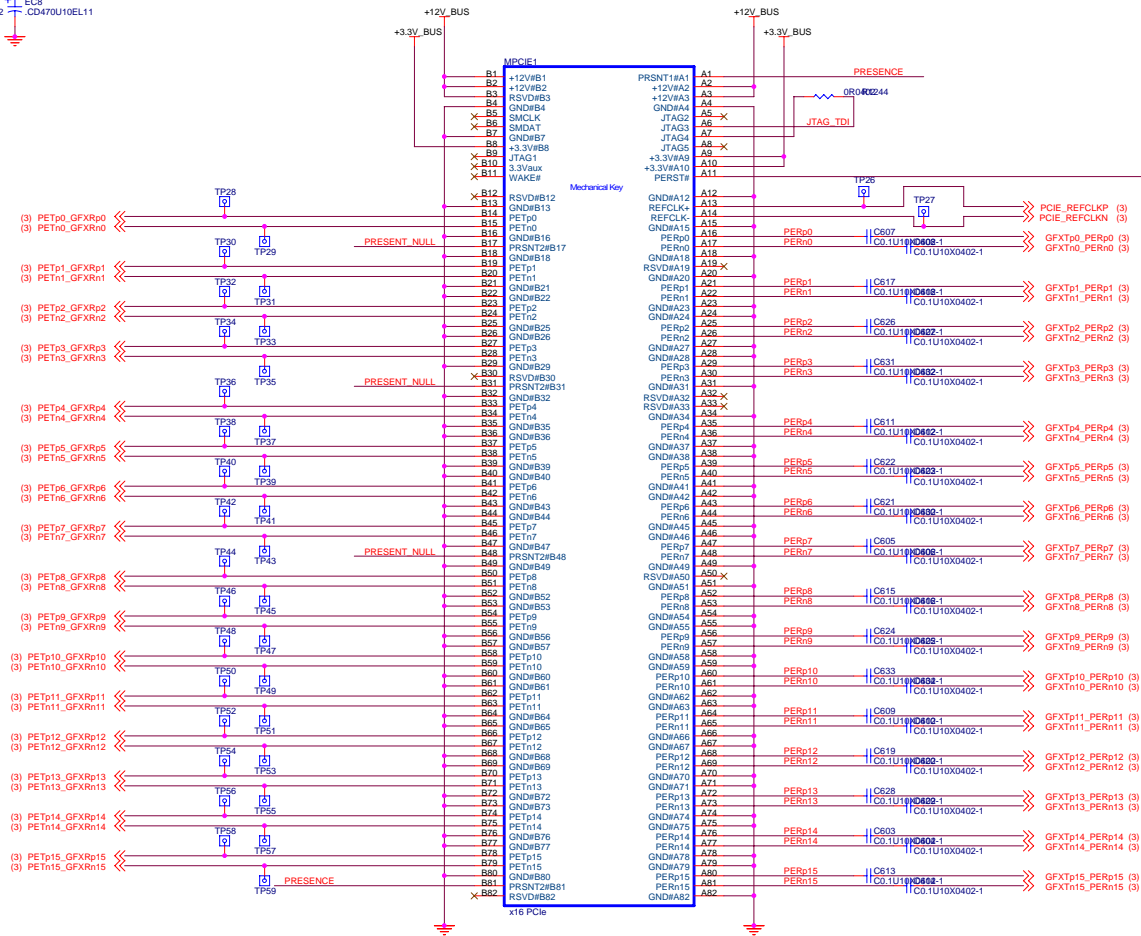
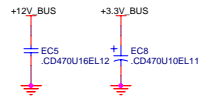
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(905) 882-2600

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PCI-EXPRESS EDGE CONNECTOR

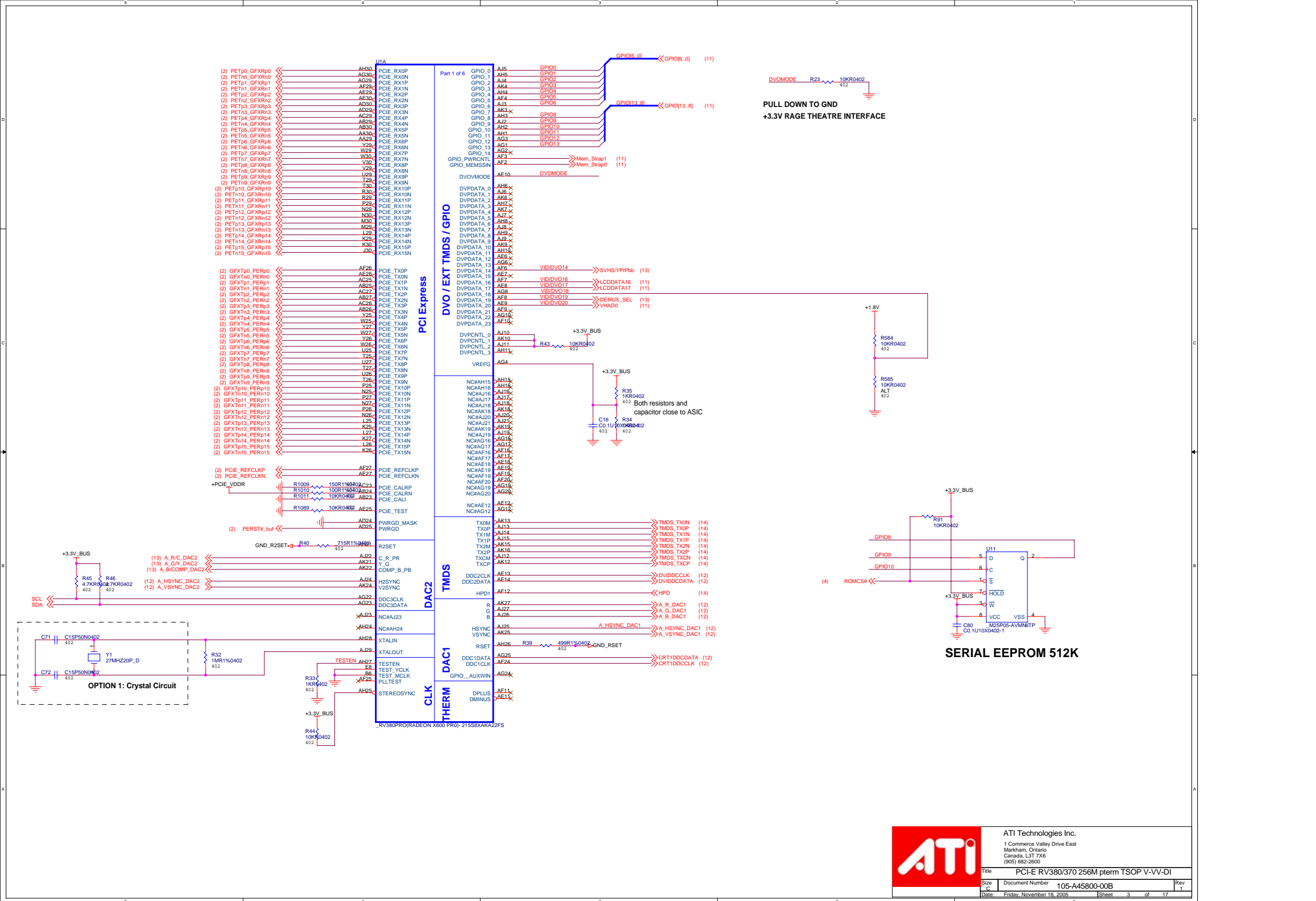


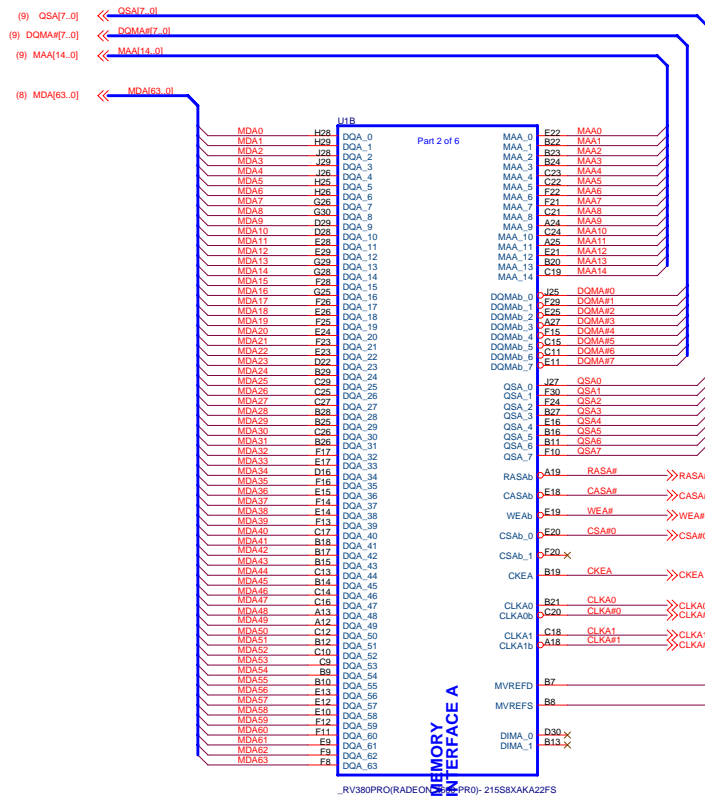
SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND



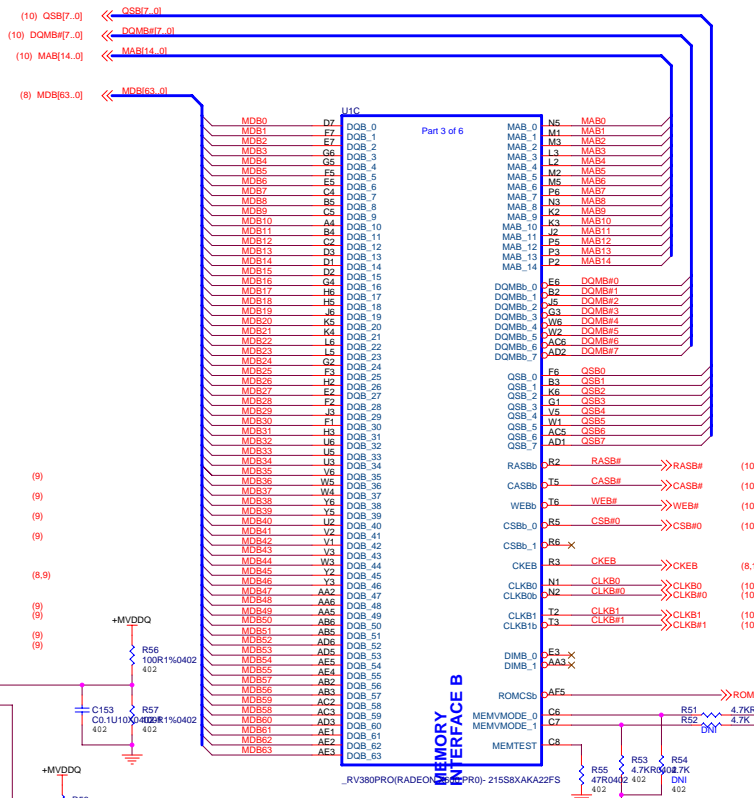
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MEMORY CHANNEL A



MEMORY CHANNEL B

PLACE C351/152 VERY CLOSE TO ASIC
R56/57/58/59 CLOSE TO ASIC AS WELL

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE
REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

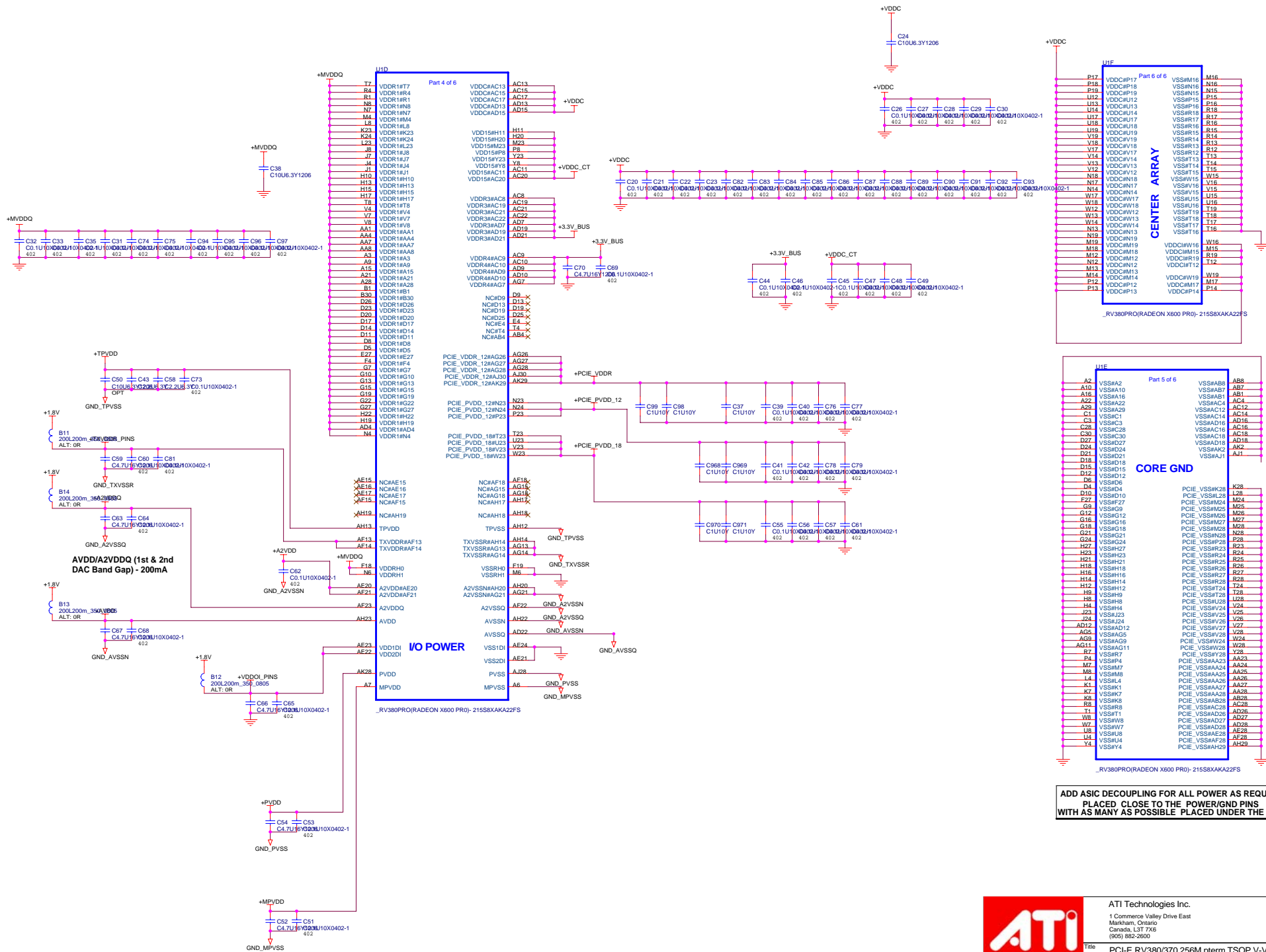
VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

DEFAULT



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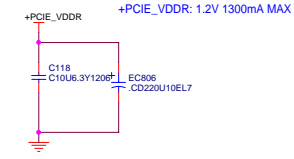


ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC

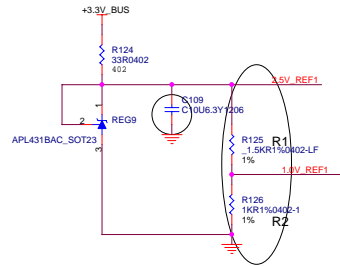


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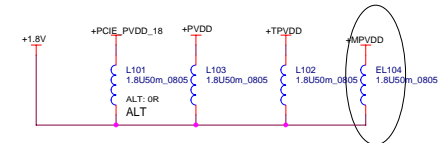
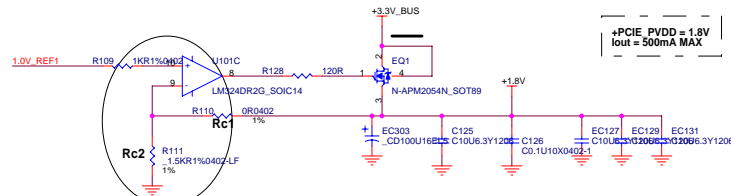
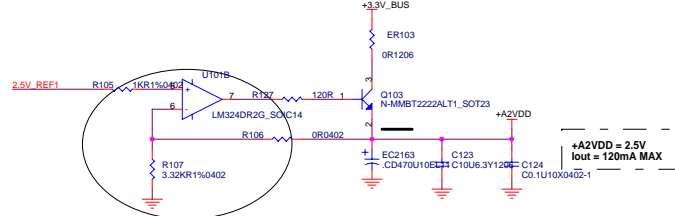
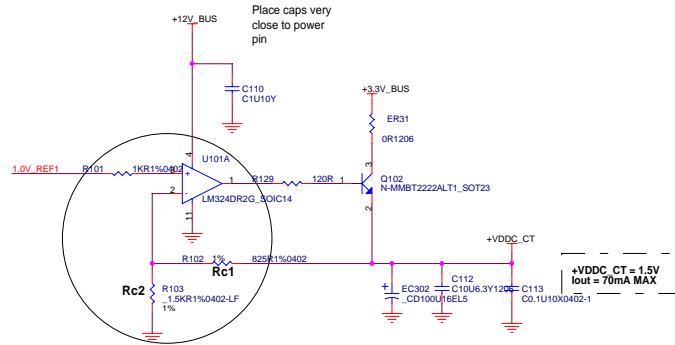
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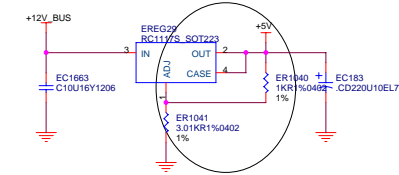
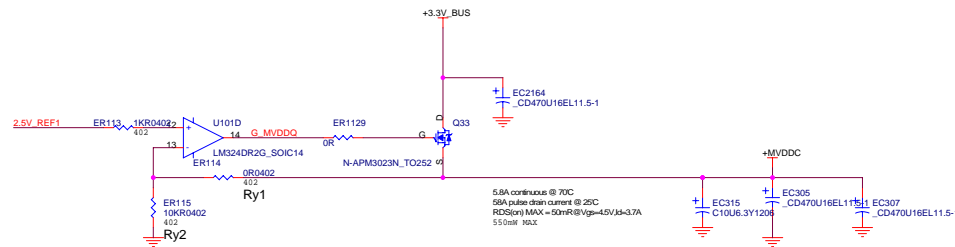
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MPVDD	Rc1	Rc2
1.2V	301R 1% P/N: 3240301000	1.50K 1% P/N: 3240150100
1.3V	442R 1% P/N: 3240442000	1.50K 1% P/N: 3240150100
1.4V	604R 1% P/N: 3240604000	1.50K 1% P/N: 3240150100
1.5V	750R 1% P/N: 3240750000	1.50K 1% P/N: 3240150100
1.6V	909R 1% P/N: 3240909000	1.50K 1% P/N: 3240150100
1.7V	1.05K 1% P/N: 3240105100	1.50K 1% P/N: 3240150100
1.8V	1.21K 1% P/N: 3240121100	1.50K 1% P/N: 3240150100
1.88V	1.33K 1% P/N: 3240133100	1.50K 1% P/N: 3240150100



Rails derived from +1.8V
+AVDD: 10mA MAX
+A2VDD: 20mA MAX
+VDDIO_PINS: 20mA MAX
+TXVDDR_PINS: 20mA MAX

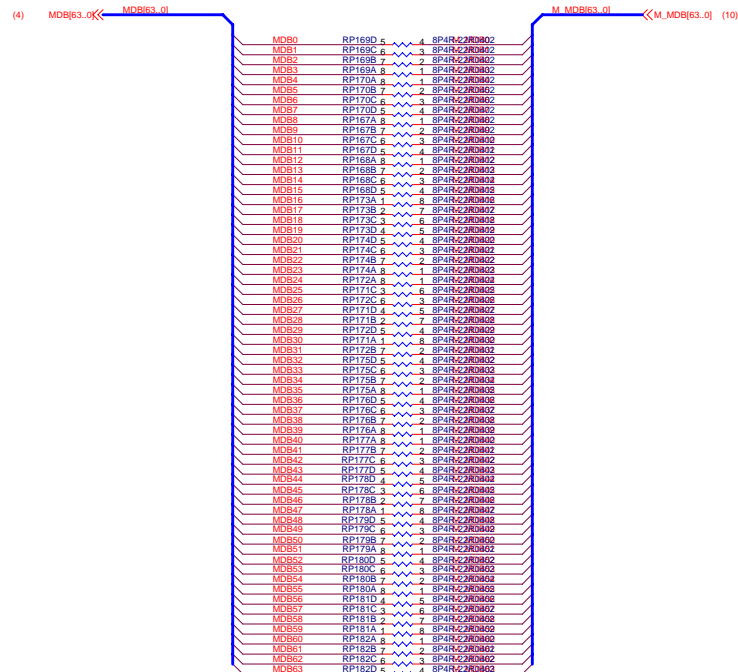
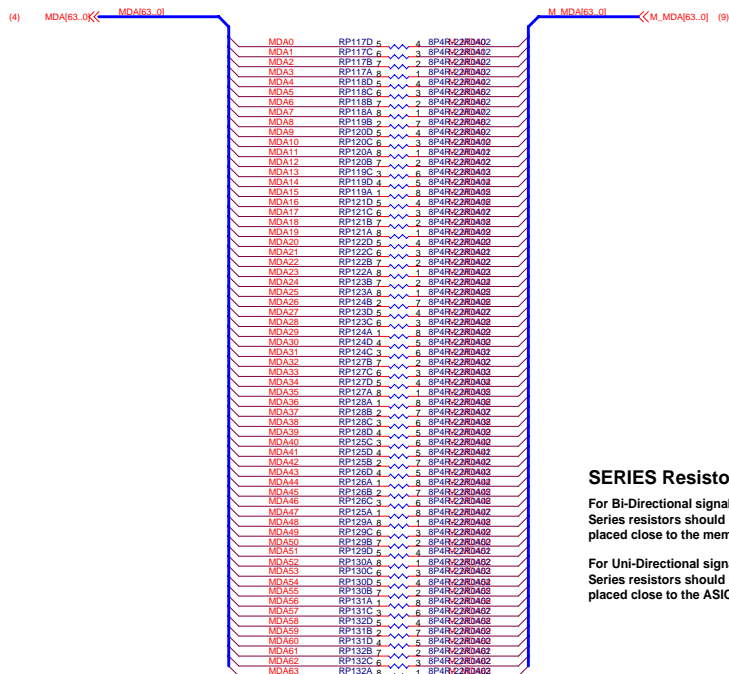


Regulator for +5V
Vout = 5V
Iout = 800mA MAX



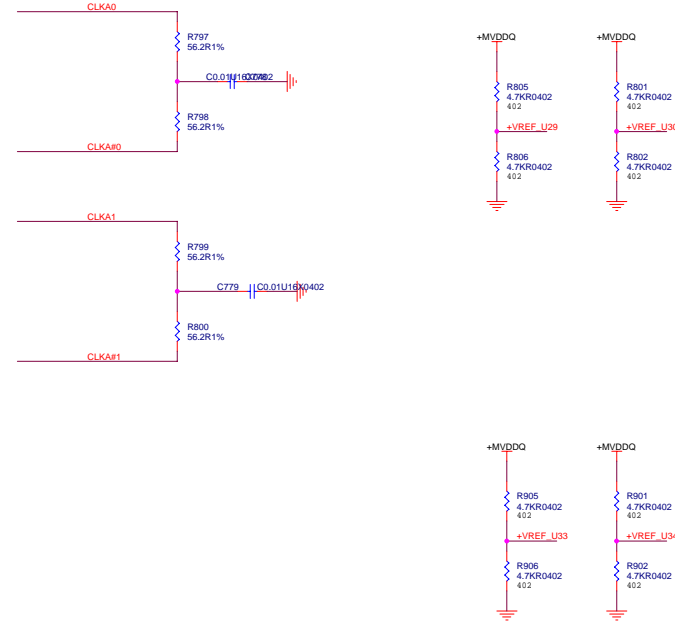
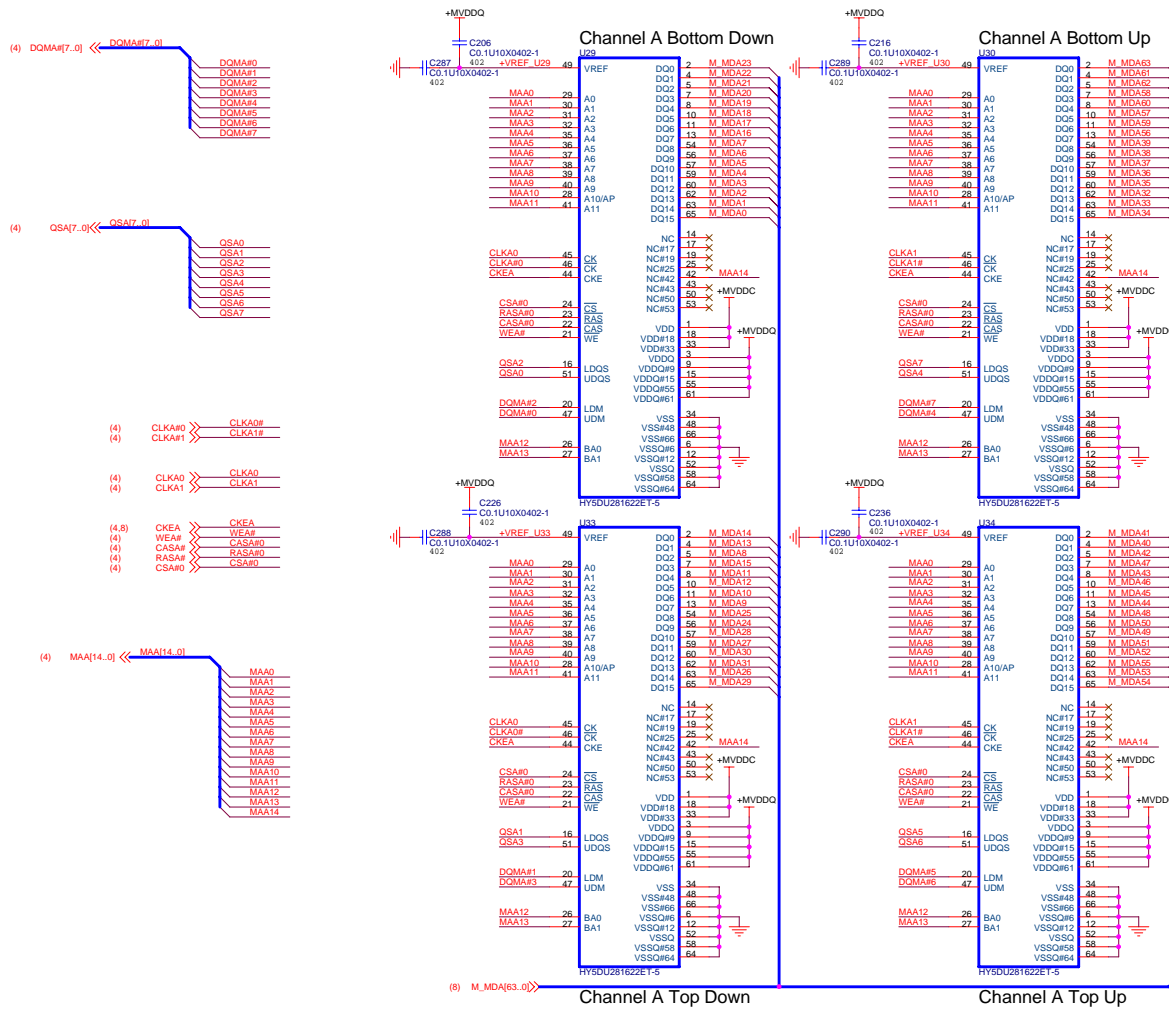
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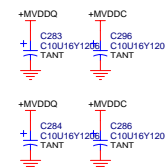
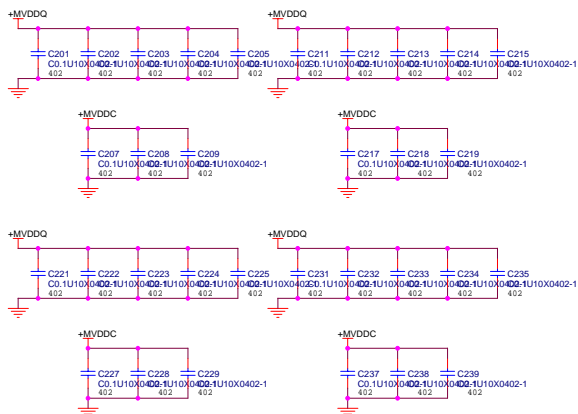


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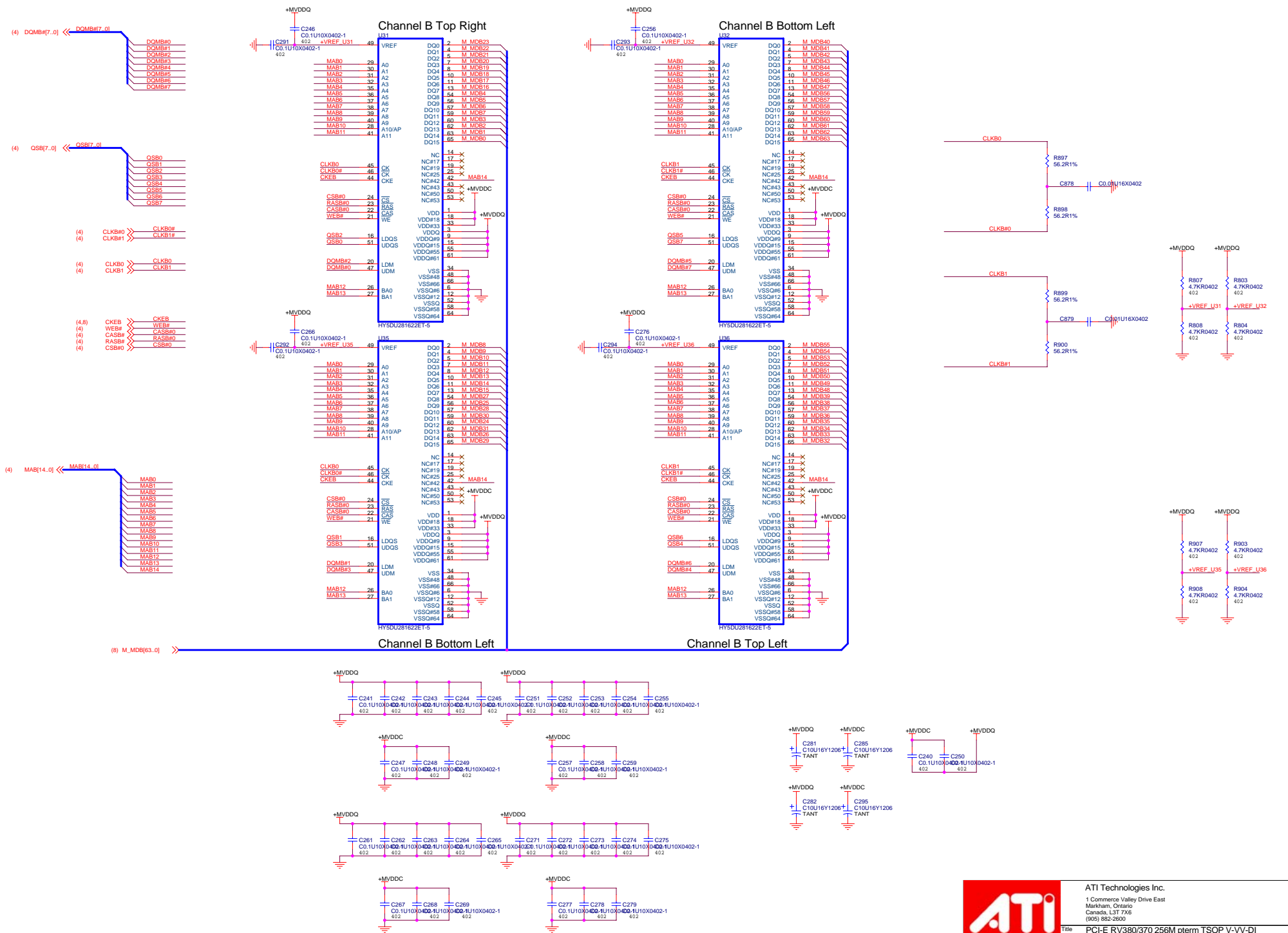


Put 1 1uF cap per power pin of memory

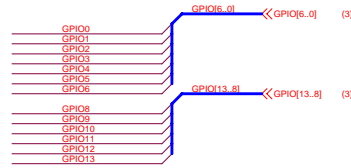
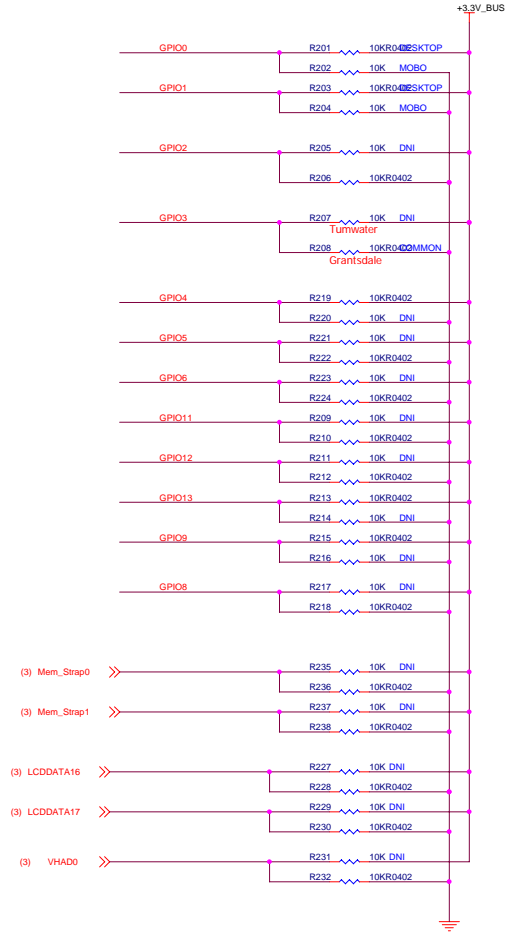


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OPTION STRAPS



STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0a mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Turmwater) 11: PCI Express 1.0a mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHADO net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present 1 - No slave VIP host port devices reporting presence during reset	

STRAP P	INTERRUPT
LOW	ENABLED (DEFAULT)
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	0	0
INF	1	0
HYN	0	1
ELPIDA	1	1

STRAPS	PIN	DESCRIPTION
NTSC/PAL	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)

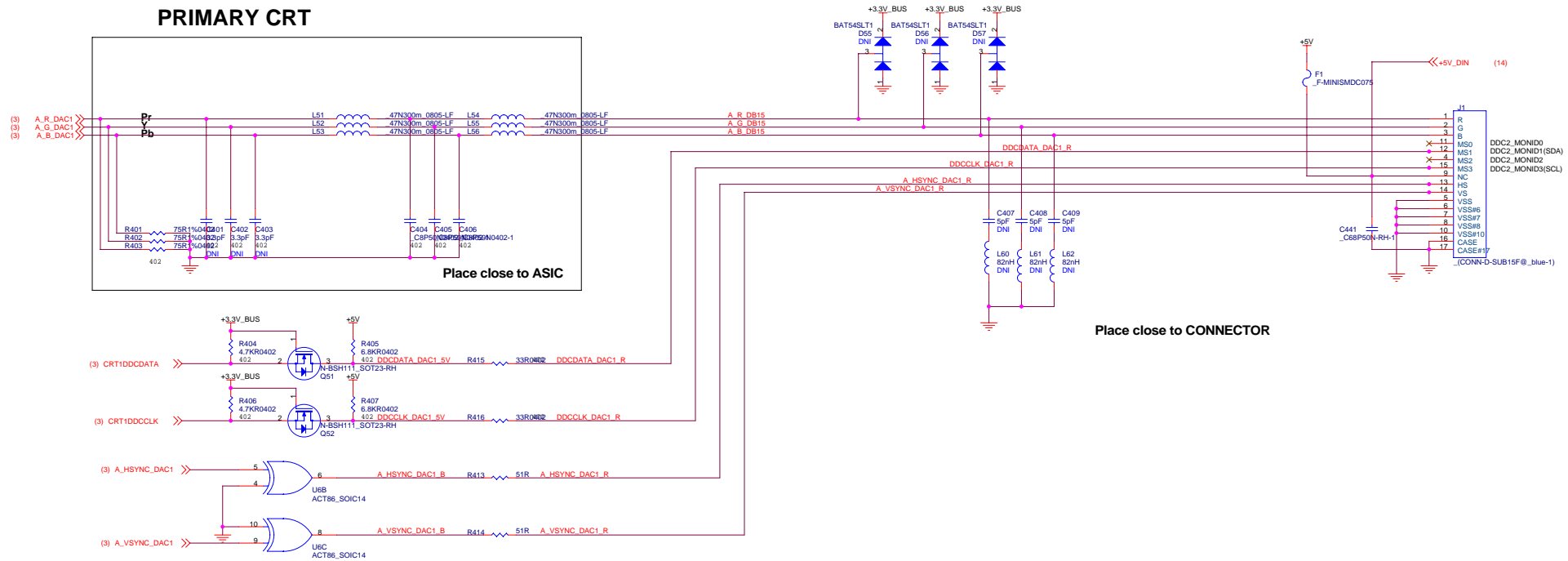


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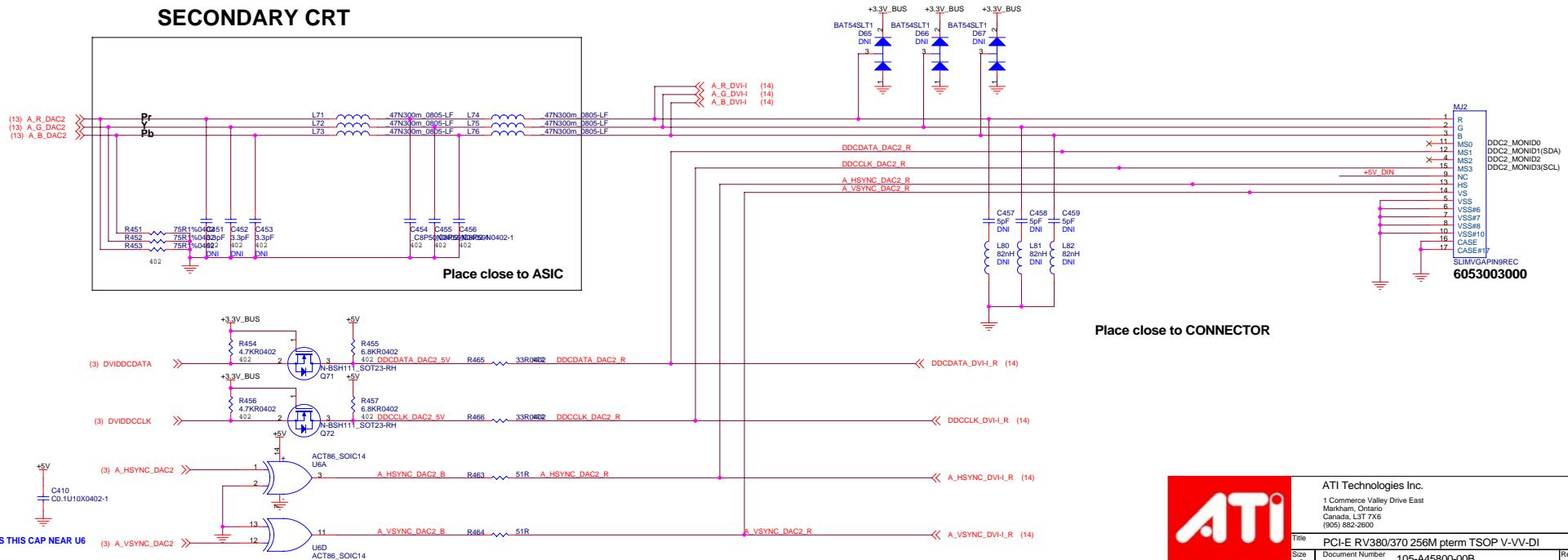
OPTIONAL ESD/HOTPLUG PROTECTION DIODES

PRIMARY CRT



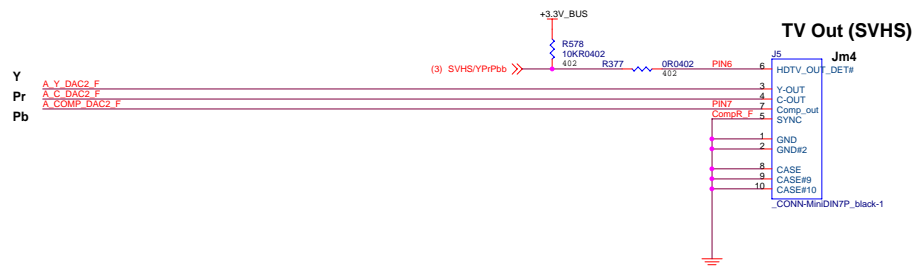
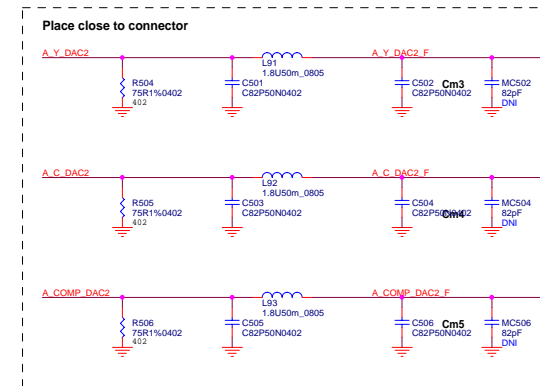
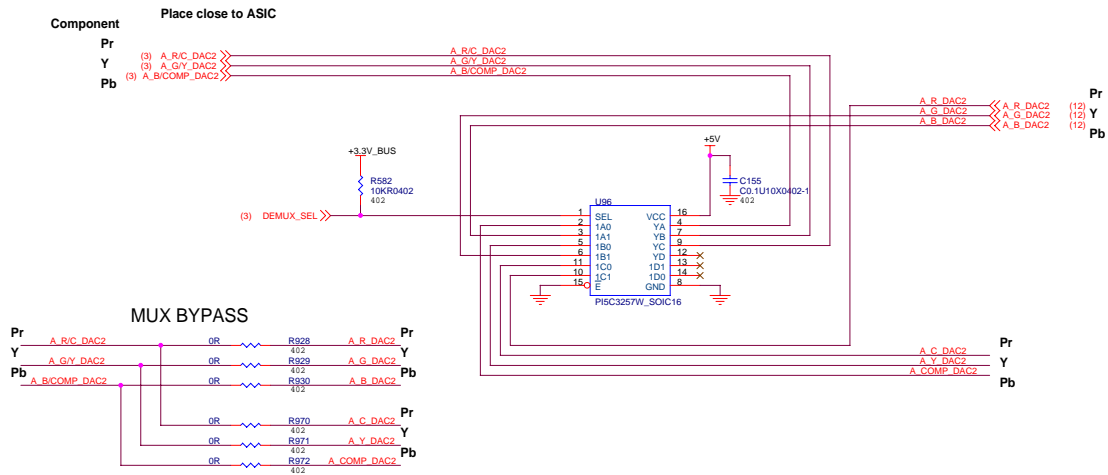
OPTIONAL ESD/HOTPLUG PROTECTION DIODES

SECONDARY CRT



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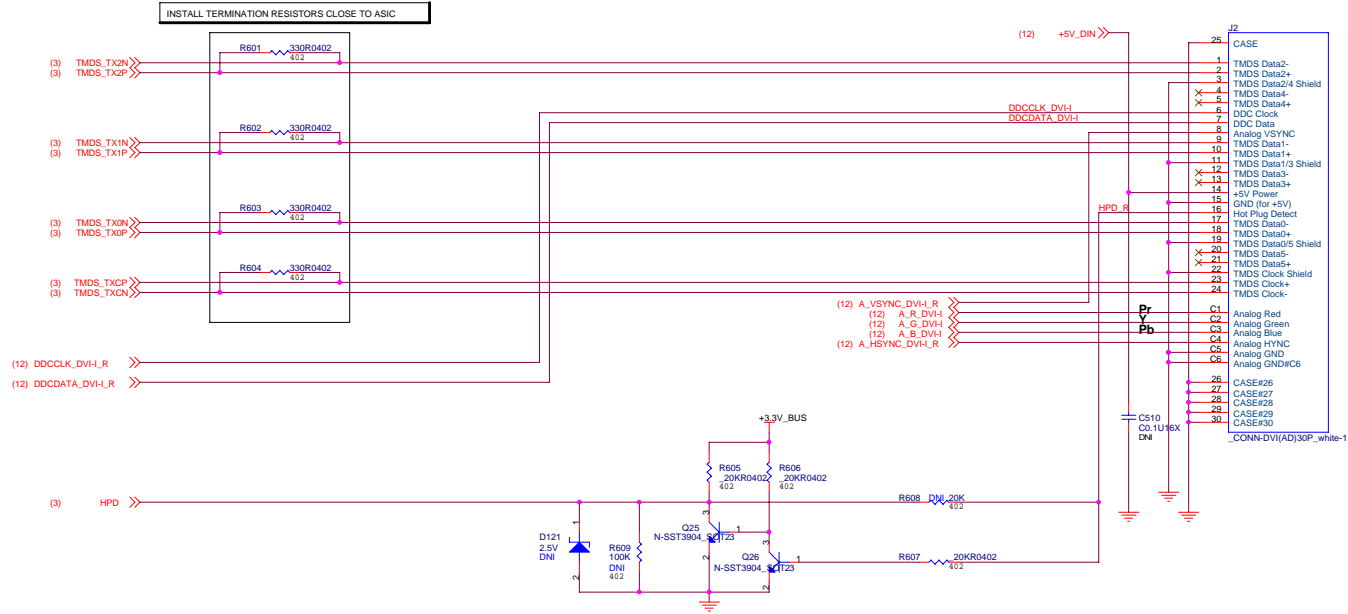
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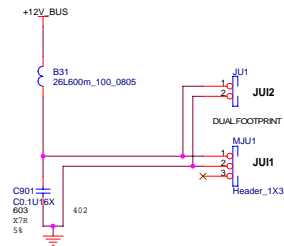
PRIMARY DVI-I CONNECTOR



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TEMPERATURE SENSE AND SPEED CONTROLLED FAN



Spring push-pin

ITW push-pin



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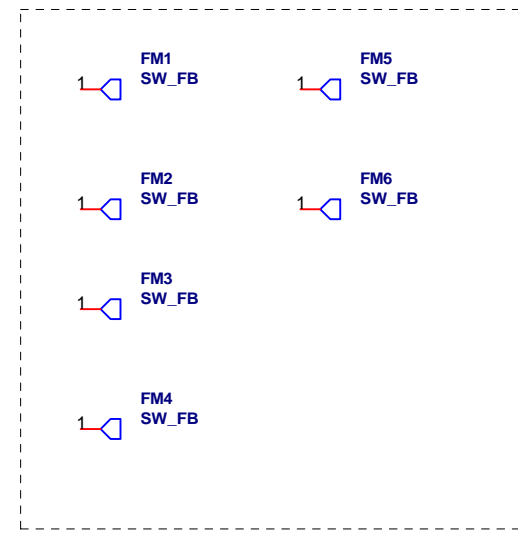
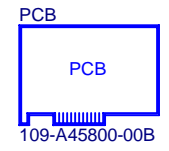
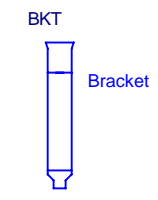
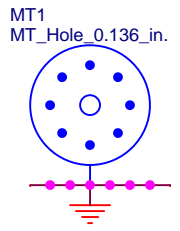
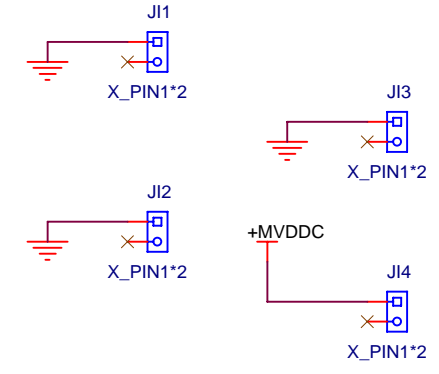
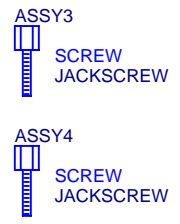
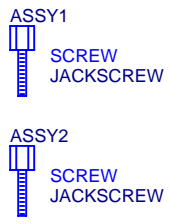
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