

PG411 A01

GP104 - 8GB GDDR5, 256b, 256Mx32  
Tall DVI-D + DP + DP + DP/HDMI + DP

TABLE OF CONTENTS

Page	Description	Page	Description
1	Table of Contents	26	PS: FBVDD
2	Block Diagram	27	PS: NVVDD_OVR8
3	PCI Express	28	PS: Blank Page
4	MEMORY: GPU Partition A/B	29	PS: NVVDD Phase 1-4
5	MEMORY: FBA[31:0]	30	PS: NVVDD Phase 5 & 6
6	MEMORY: FBA[63:32]	31	PS: Blank Page
7	MEMORY: FBB[31:0]	32	PS: Dynamic Power Balance Phases
8	MEMORY: FBB[63:32]	33	PS: Dynamic Power Balance Logic
9	MEMORY: GPU Partition C/D	34	PS: NV3V3, NV12V
10	MEMORY: FBC[31:0]	35	PS: Inputs, Filtering, and Monitoring
11	MEMORY: FBC[63:32]	36	PS: Shutdown and Sequencing
12	MEMORY: FBD[31:0]	37	PS: 12V Current Steering PSI Control and LED
13	MEMORY: FBD[63:32]	38	MECH: Bracket/Thermal
14	GPU PWR and GND		
15	GPU Decoupling		
16	IFPAB DVI-D-DL		
17	IFPE DP		
18	IFPEF DP		
19	IFPC HDMI 2.0/DP		
20	IFPD DP		
21	MIOA/B Interface and Frame Lock		
22	MISC1: Fan, Thermal, JTAG, GPIO, Stereo		
23	MISC2: ROM, XTAL, Straps		
24	PS: 1V8, 1V8_AON		
25	PS: 5V, PEX_VDD		

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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	Table of Contents

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PCB REV

1G411-A01

BOM REV

A

PAGE

1 OF 38

DATE

29-MAR-2016

A

B

C

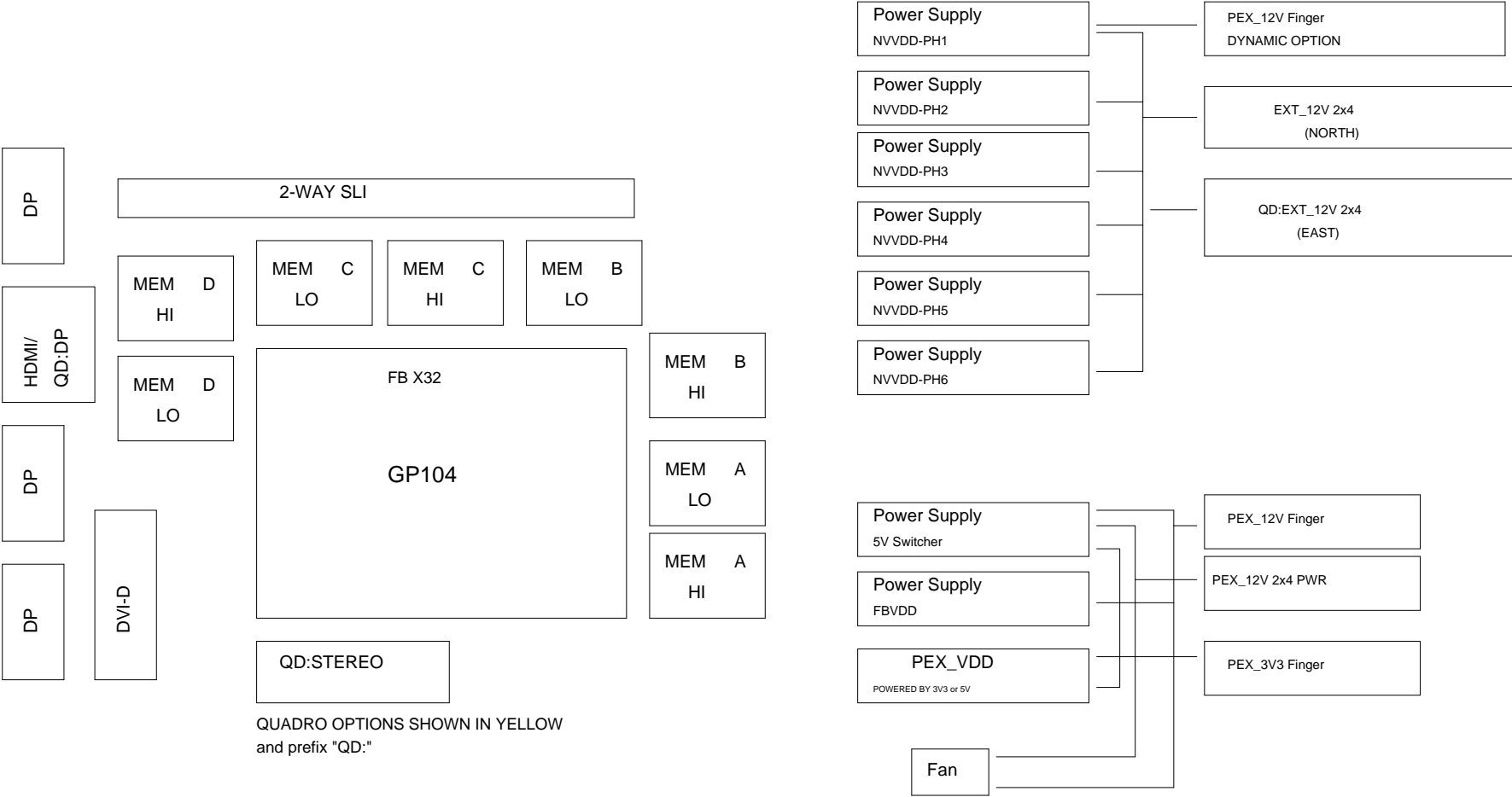
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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	Block Diagram


NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-1G411-BASE-100	PAGE	2 OF 38
PCB REV	1G411-A01	DATE	29-MAR-2016
BOM REV	A		

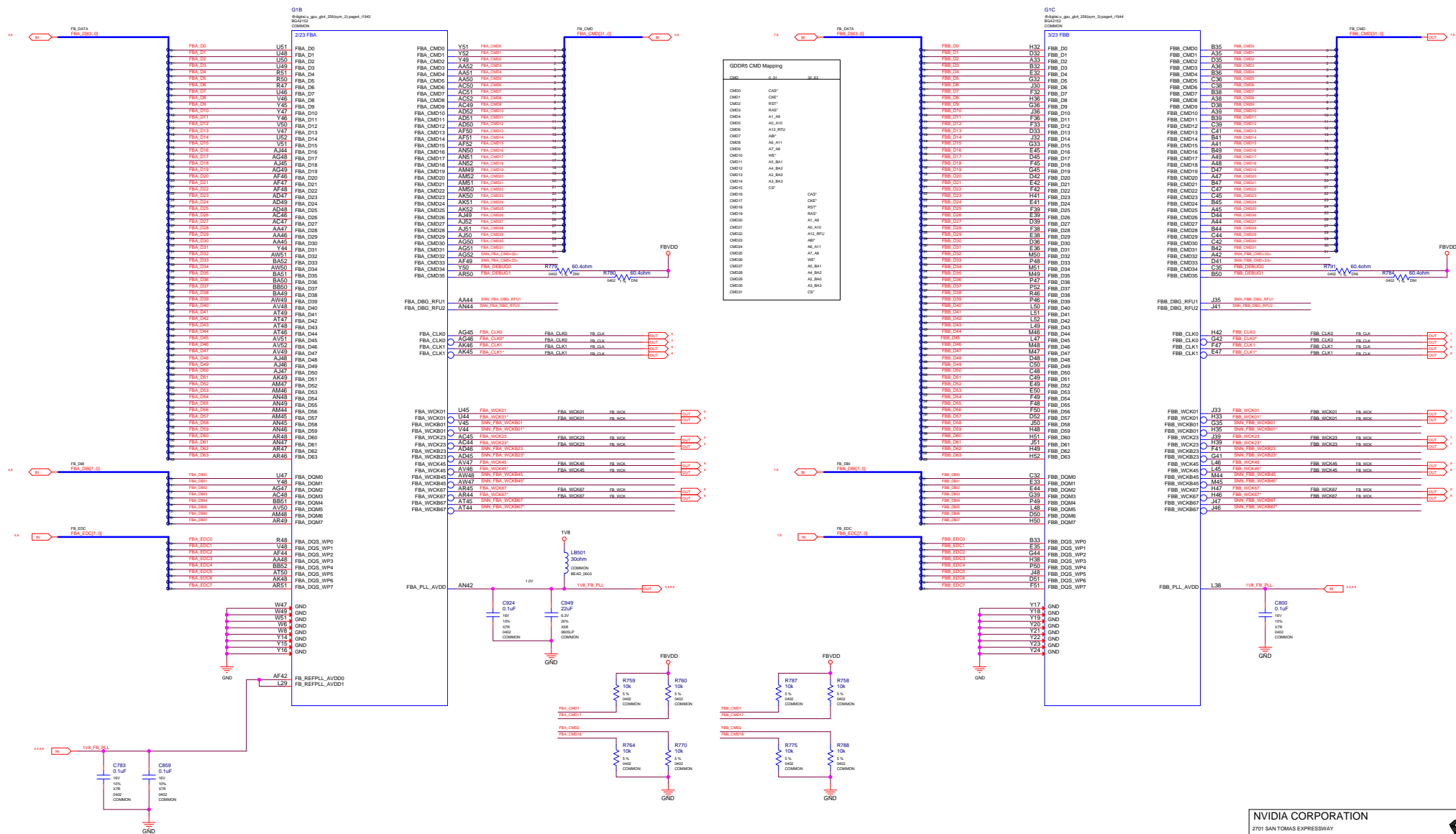
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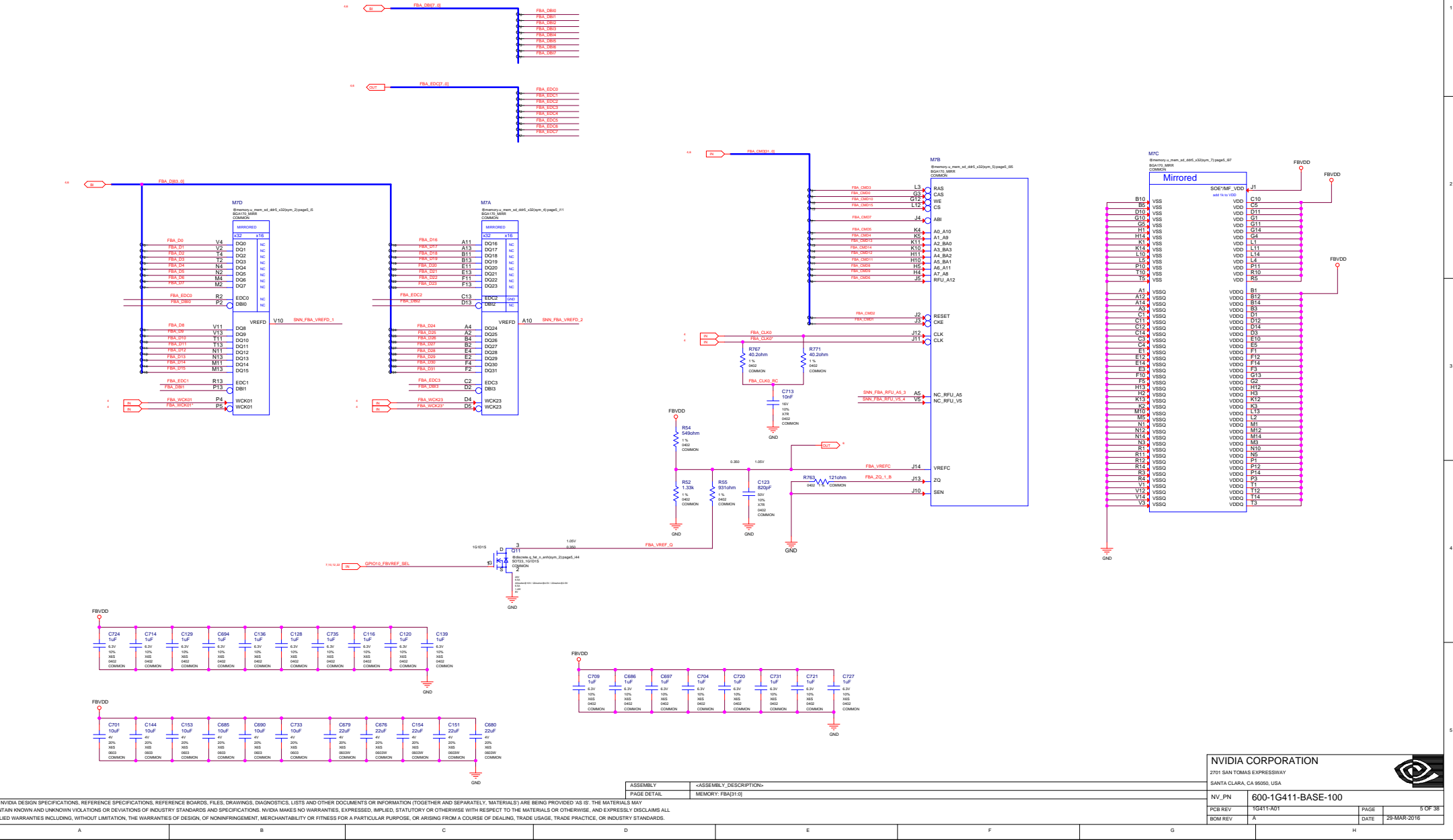


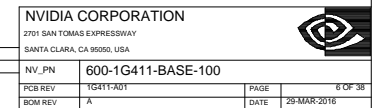
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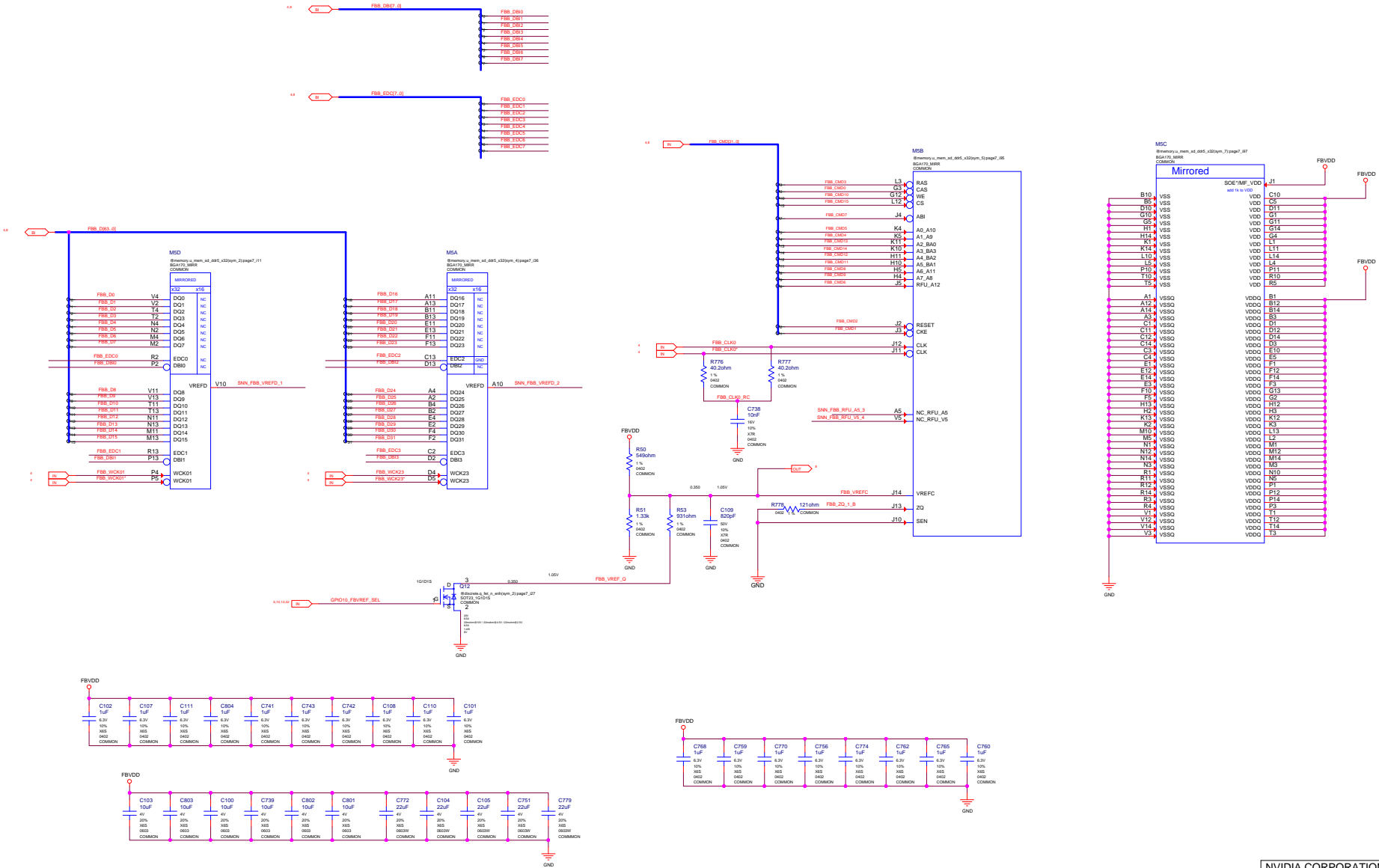
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PAGE DETAIL	PCI Express

<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
<b>NV_PN</b>		<b>600-1G411-BASE-100</b>		
<b>PCB REV</b>	74111-A01	<b>PAGE</b>	3 OF 38	
<b>BOM REV</b>	A	<b>DATE</b>	29-MAR-2016	





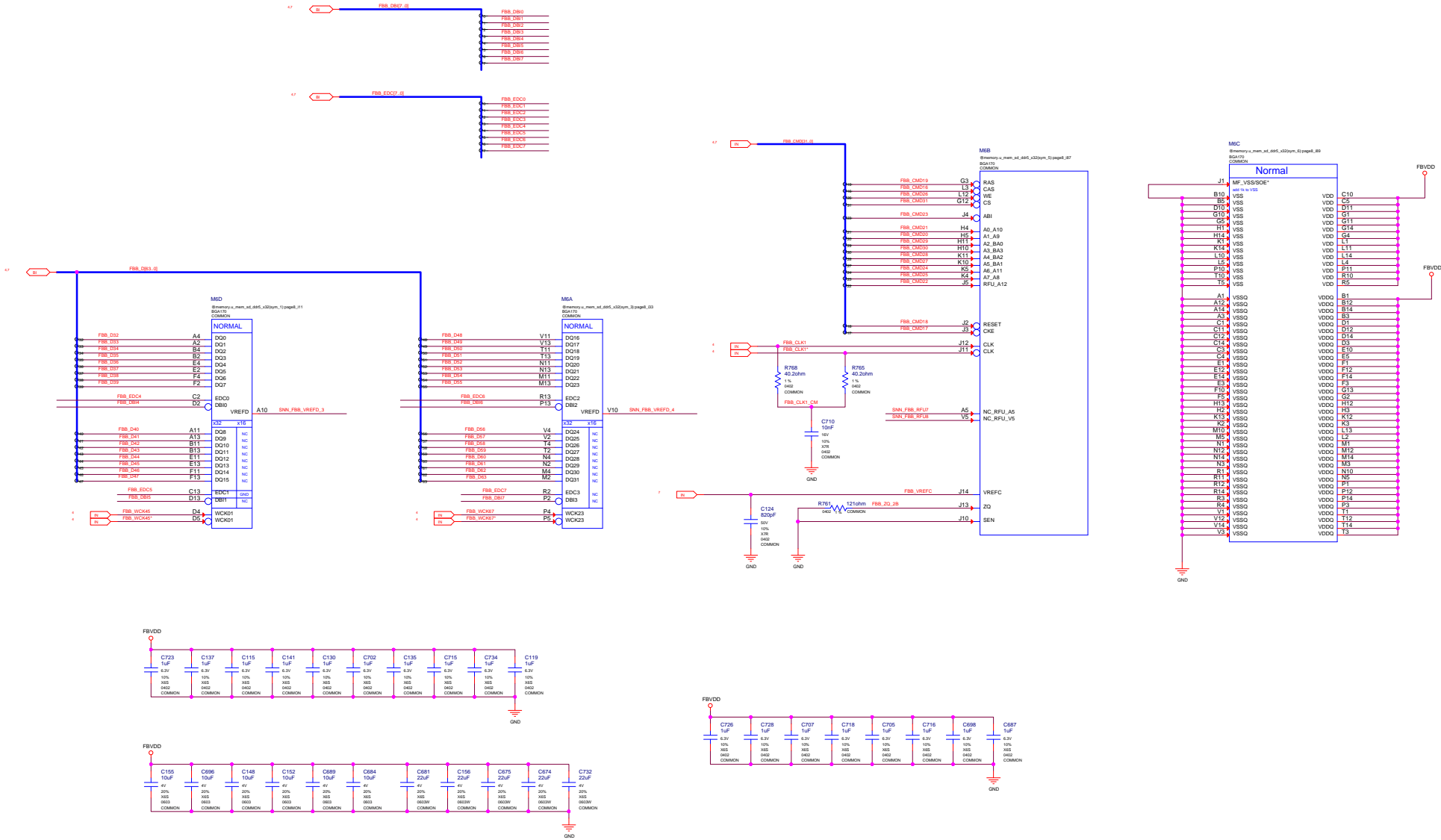




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ASSEMBLY	ASSEMBLY DESCRIPTION
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INV. PN	600-1G411-BASE-100
PCB REV	1G411-A01
BOB REV	A
PAGE	7 OF 38
DATE	29-MAR-2016

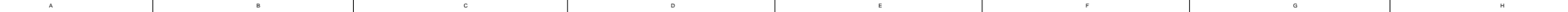


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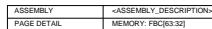
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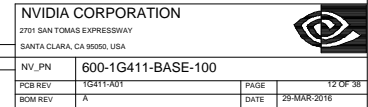
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NV_PN	600-1G411-BASE-100
PCB REV	1G411-A01
BOB REV	A
PAGE	8 OF 38
DATE	29-MAR-2016

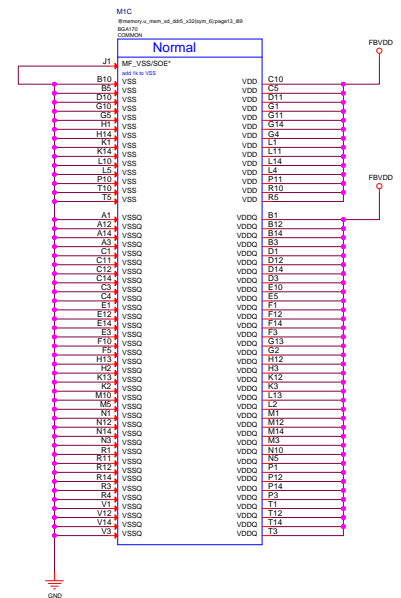
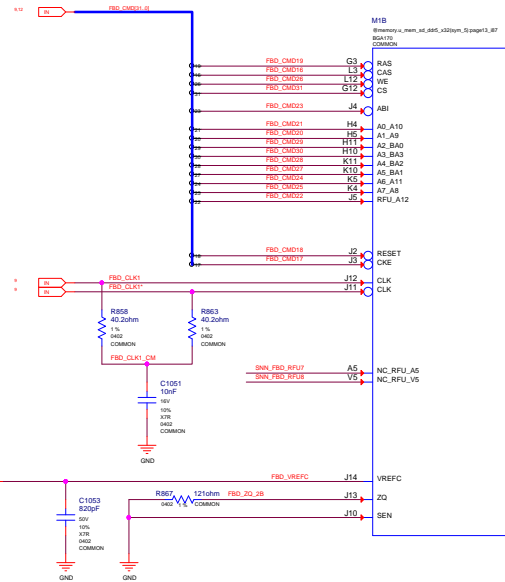
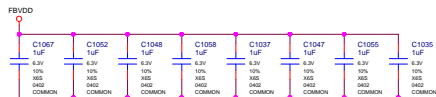
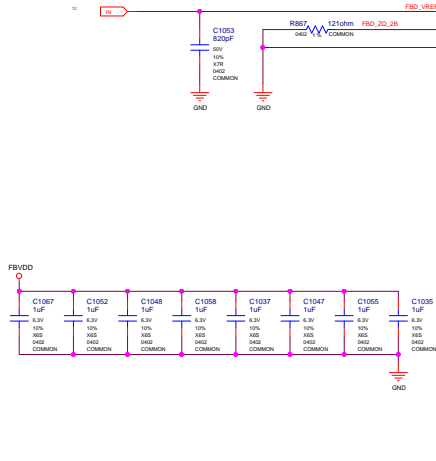







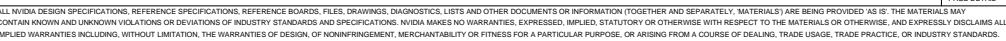







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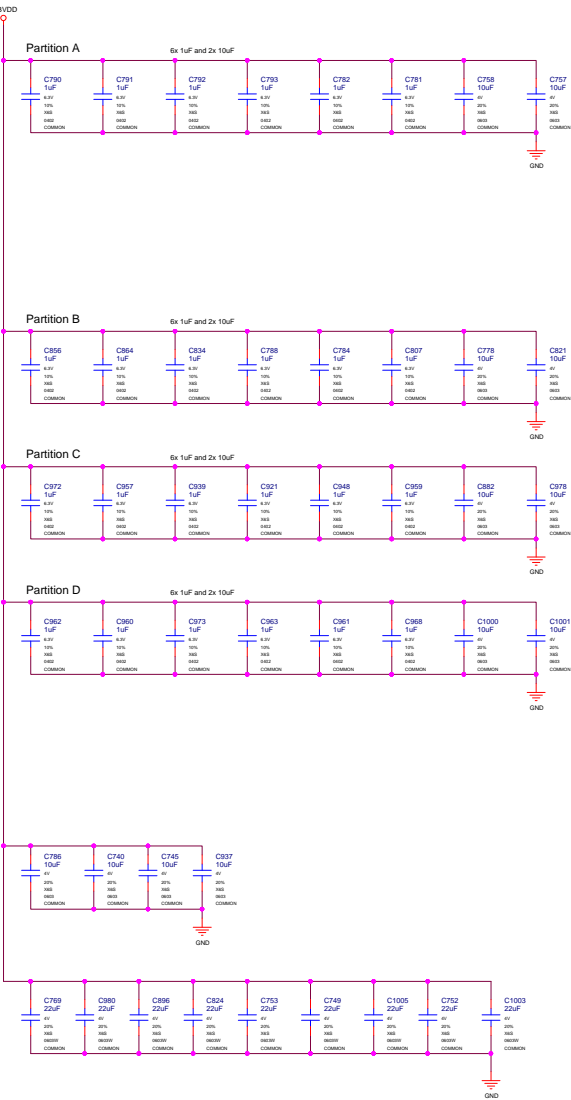
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NV_PN	600-1G411-BASE-100			
PCB REV	7G411-A01		PAGE	13 OF 38
BOM REV	A		DATE	29-MAR-2016



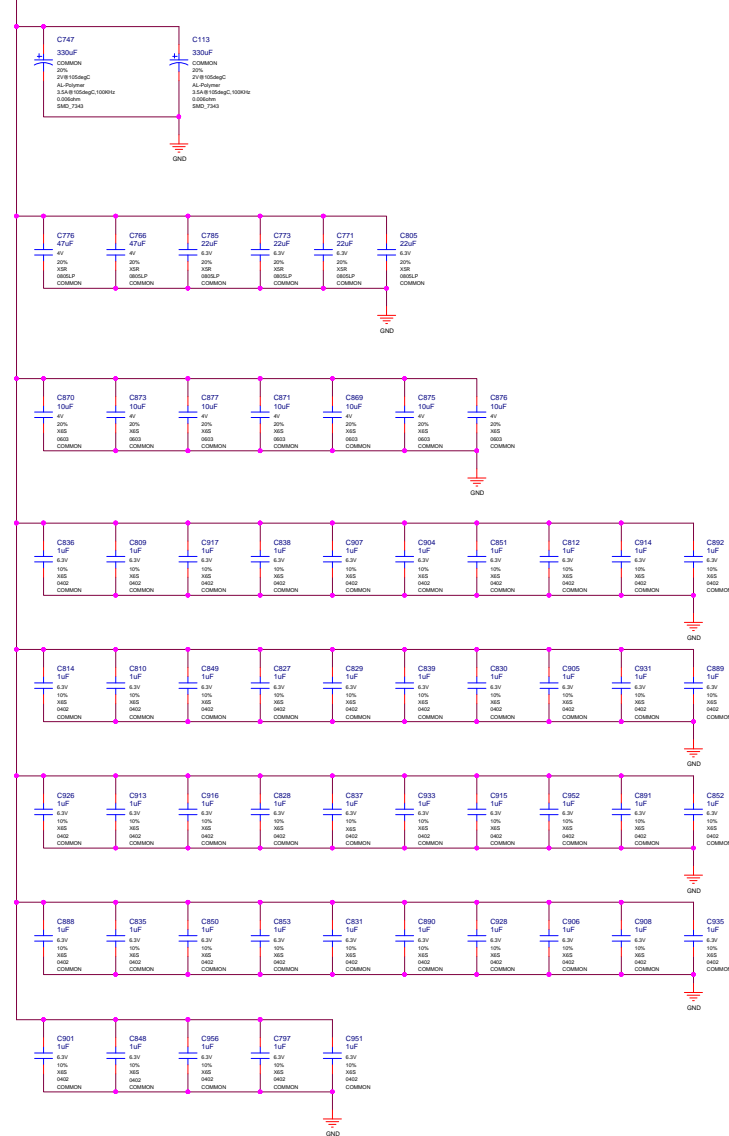
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NV_PN	600-1G411-BASE-100		
PCB REV	1G411-A01	PAGE	14 OF 38
BOM REV	A	DATE	29-MAR-2016



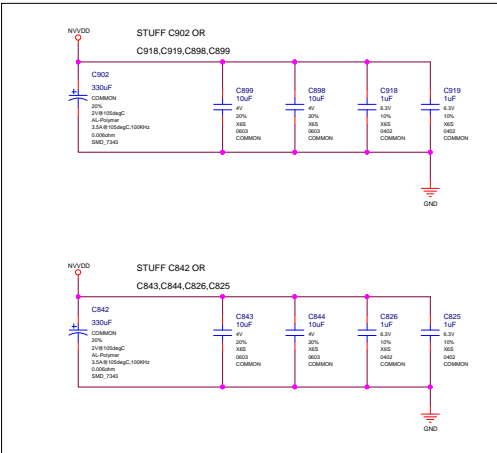
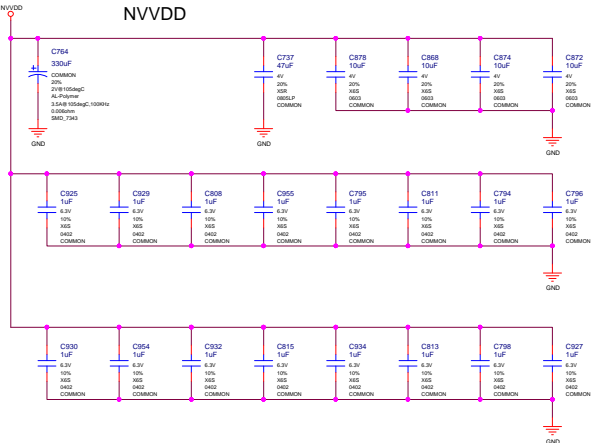
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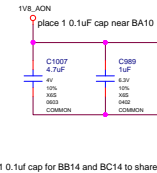
NVVDD



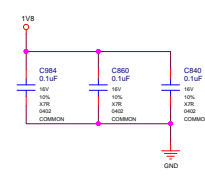
NVVDD



1V8\_AON



VDD18




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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	GPU Decoupling

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2701 SAN TOMAS EXPRESSWAY			
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NV_PN	600-1G411-BASE-100		
PCB REV	1G411-A01	PAGE	15 OF 38
BCM REV	A	DATE	29-MAR-2016

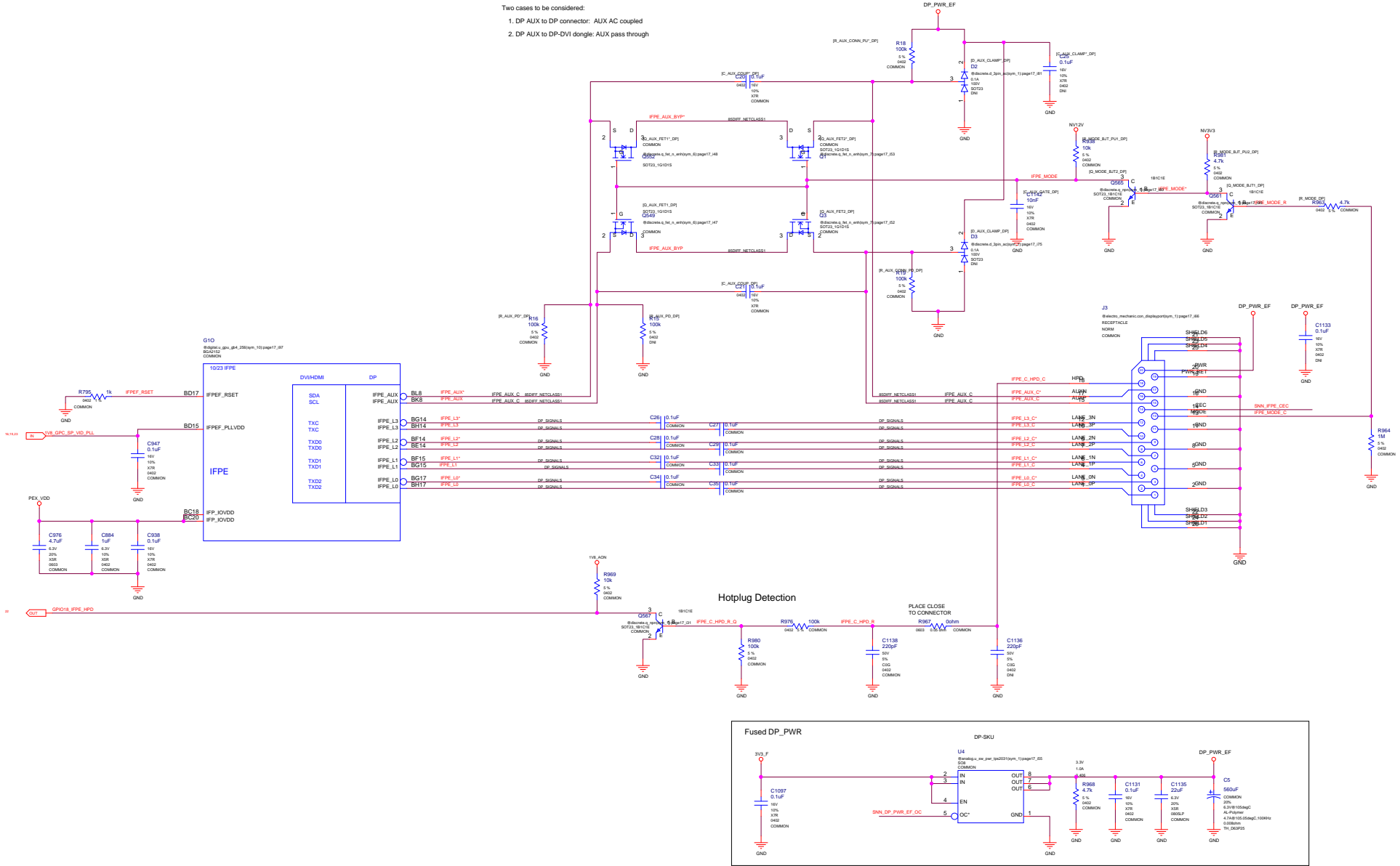


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NV_PN	600-1G411-BASE-100		
PCB REV	7G411-A01	PAGE	16 OF 38
BOM REV	A	DATE	29-MAR-2016





- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
  2. DP AUX to DP-DVI dongle: AUX pass through

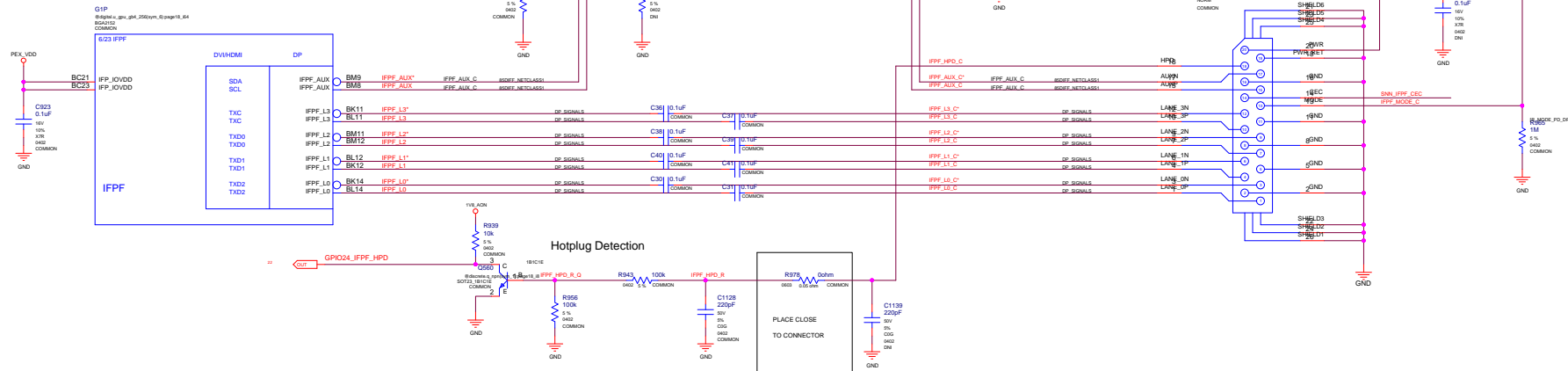


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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	IFPE DP

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2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-1G411-BASE-100	PAGE	17 OF 38
PCB REV	1G411-A01	DATE	29-MAR-2016
BCM REV	A		

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



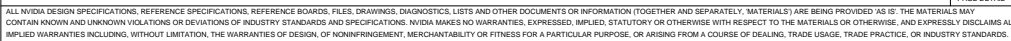
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NV_PN	600-1G411-BASE-100		
PCB REV	1G411-A01	PAGE	18 OF 38
BOM REV	A	DATE	29-MAR-2016

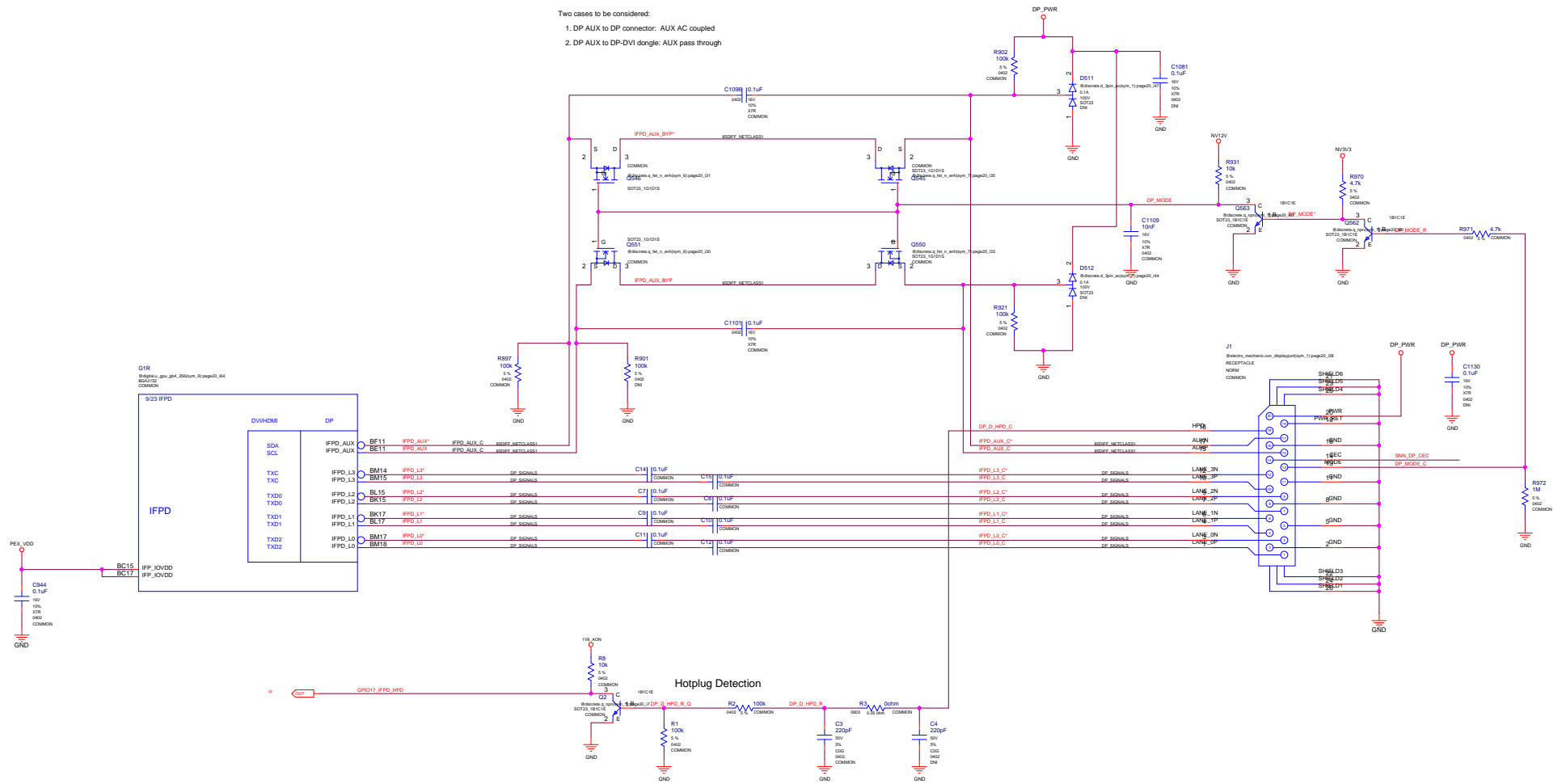
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PCB REV	1G411-A01	PAGE	19 OF 38
BOM REV	A	DATE	29-MAR-2016

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPD DP

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NV_PN	600-1G411-BASE-100
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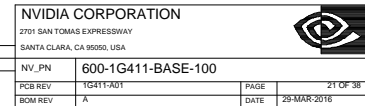
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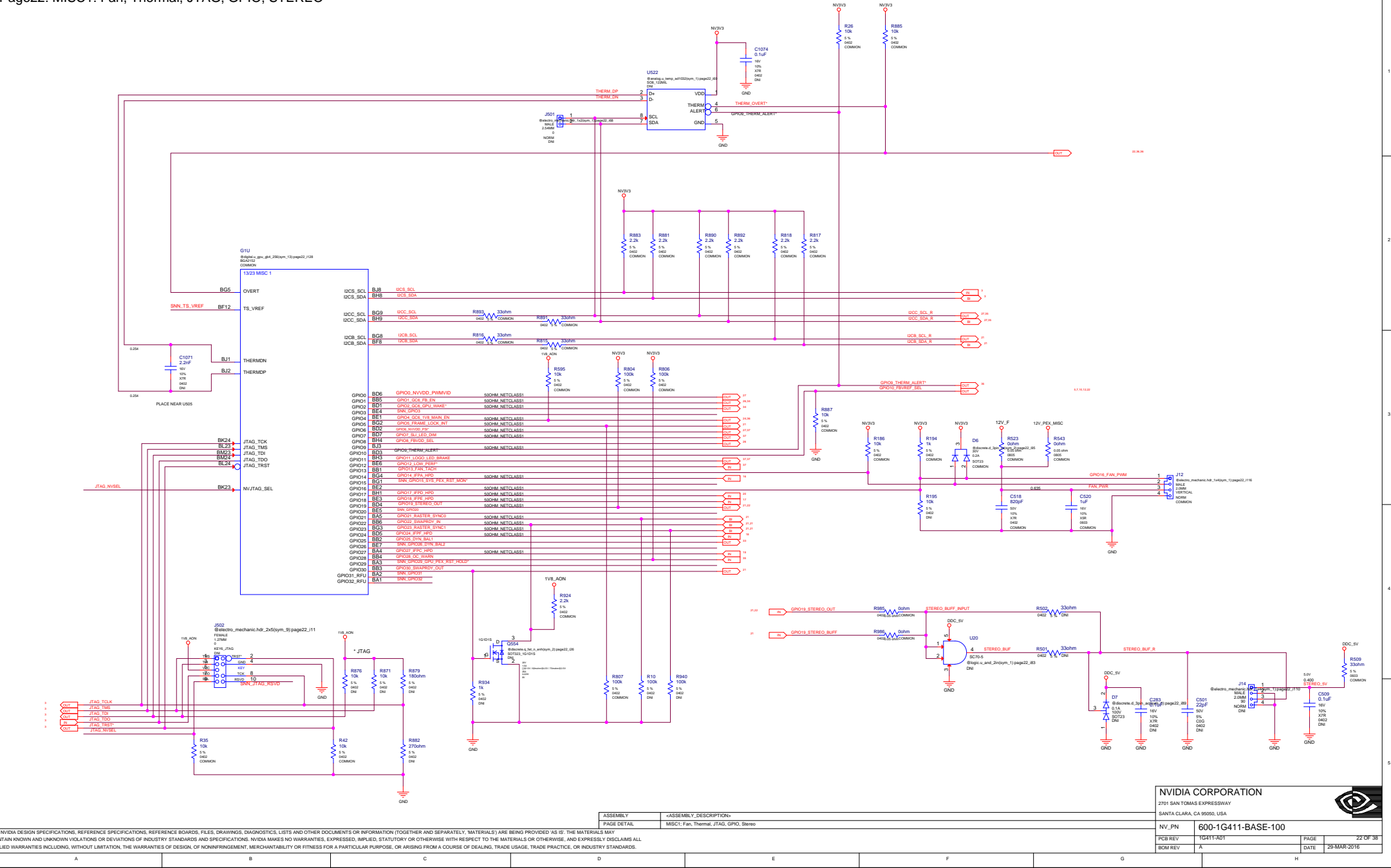
BOM REV	A
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PAGE	20 OF 38
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DATE	29-MAR-2016
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NV_PN	600-1G411-BASE-100
PCB REV	1G411-A01
BCM REV	A
PAGE	22 OF 38
DATE	29-MAR-2016

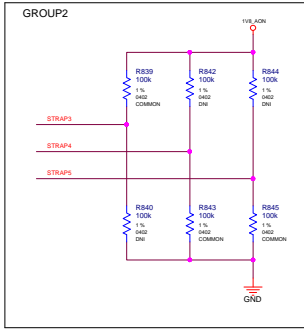
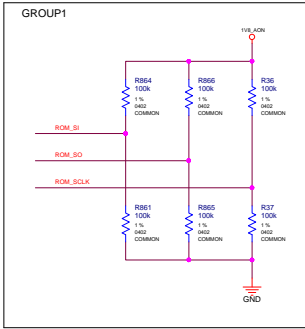
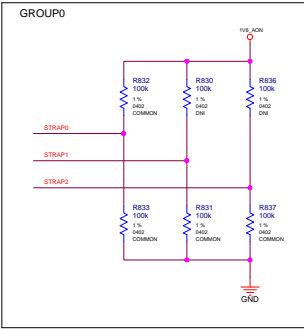
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L	L	L	00000	
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	0	1	0
L	H	M	1	0	1	1
L	M	H	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
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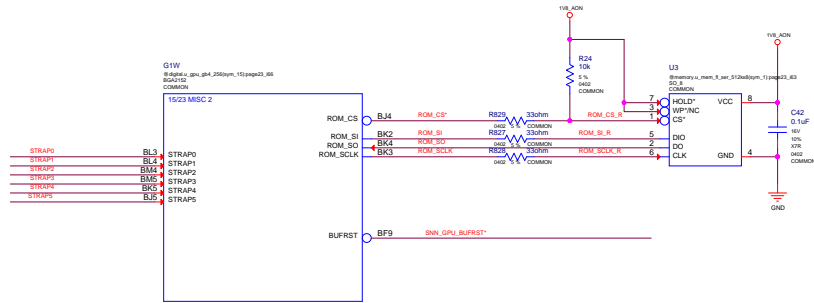
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M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



CFG[3:0] Config Width	Vendor
0000	256Mx32 256-bit Samsung
0001	256Mx32 256-bit Micron
0010	256Mx32 256-bit Hynix
0011	Reserved
0100	Reserved
0101	Reserved
0110	Reserved
0111	Reserved









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NV_PN	600-1G411-BASE-100
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PCB REV	1G411-A01
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FCD REV	12/11/12
BOM REV	A



PAGE	25 OF 38
------	----------


DATE	29-MAR-2016
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GPIO8 LEVEL	FBVDD OUTPUT VOLTAGE
0	1.35V
1	1.55V

ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	PS: FBVDD

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PCB REV	1G411-A01	PAGE	26 OF 38	
BOM REV	A	DATE	29-MAR-2016	




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NV_PN	600-1G411-BASE-100		
PCB REV	1G411-A01	PAGE	27 OF 38
BOM REV	A	DATE	29-MAR-2016

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NV_PN	600-1G411-BASE-100		
PCB REV	1G411-A01	PAGE	28 OF 38
BOM REV	A	DATE	29-MAR-2016



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NV_PN	600-1G411-BASE-100		
PCB REV	1G411-A01	PAGE	29 OF 38
BOM REV	A	DATE	29-MAR-2016




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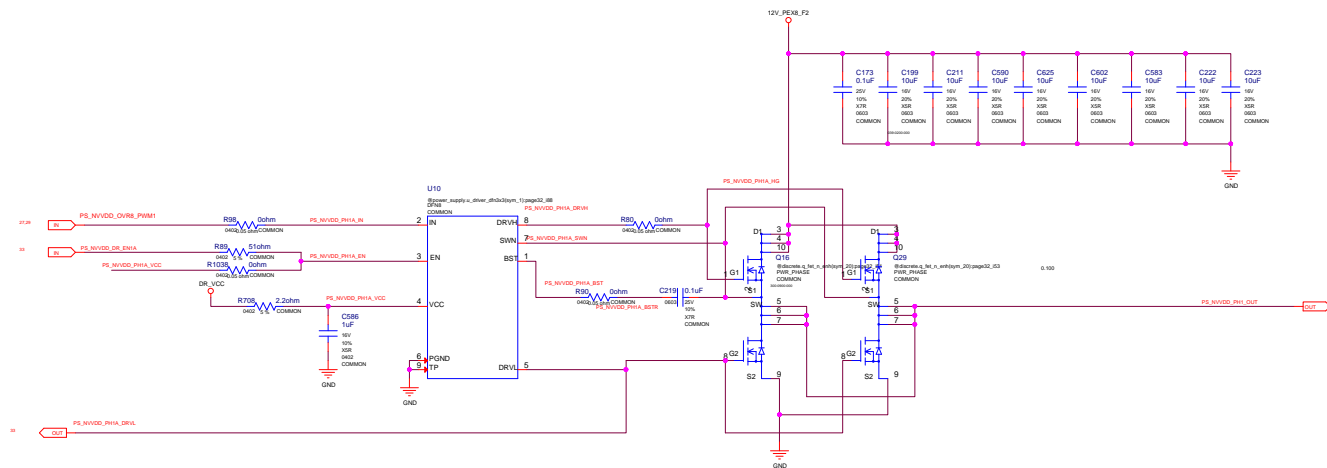
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NV_PN	600-1G411-BASE-100		
PCB REV	1G411-A01	PAGE	31 OF 38
BOM REV	A	DATE	29-MAR-2016



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PAGE DETAIL	PS: Dynamic Power Balance Phases

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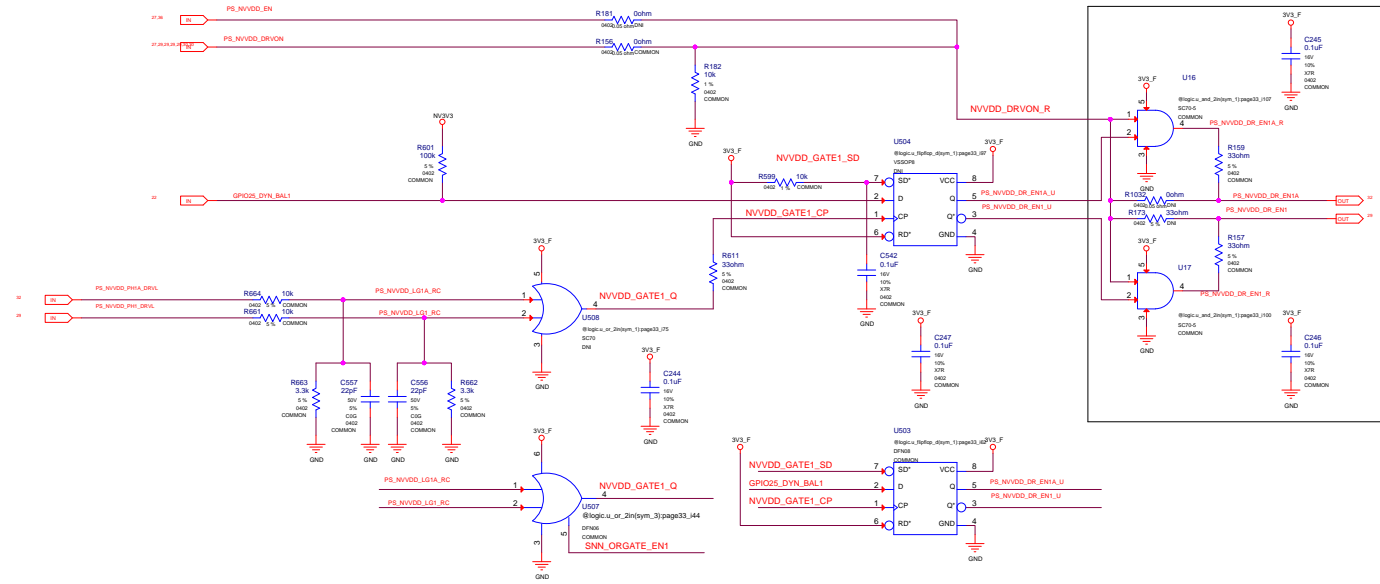
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NV_PN	600-1G411-BASE-100		
PCB REV	1G411-A01	PAGE	32 OF 38
BOM REV	A	DATE	29-MAR-2016

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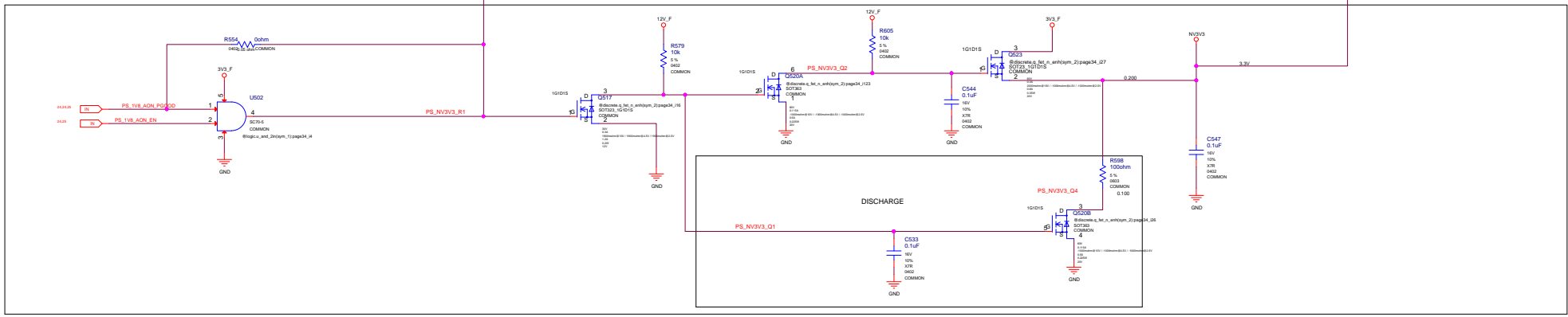
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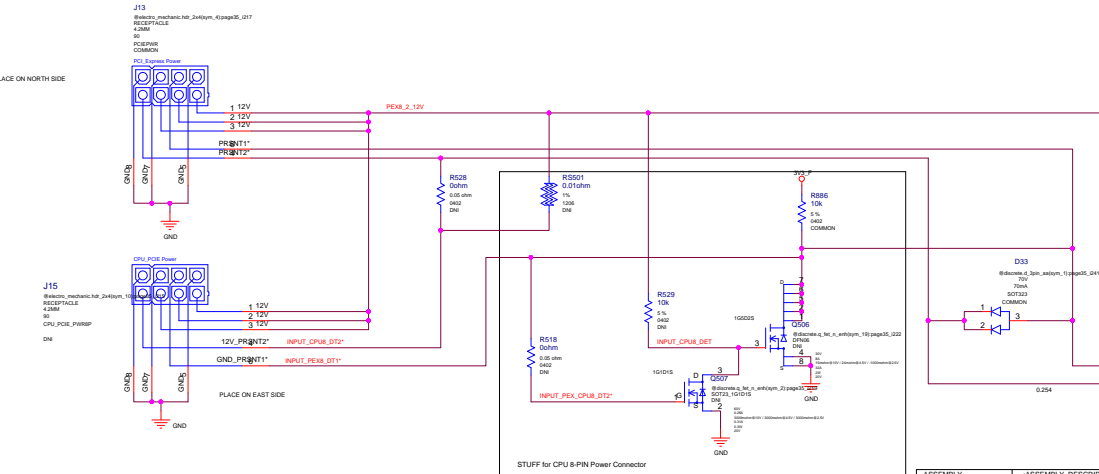
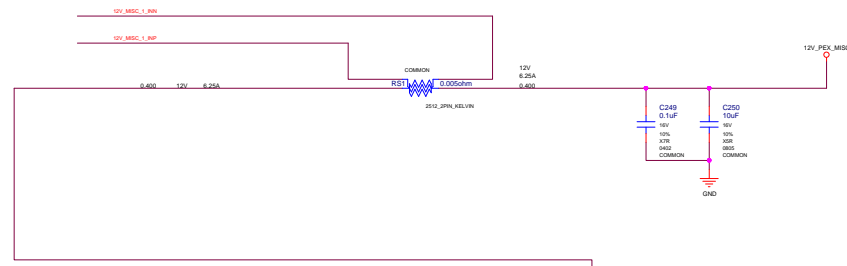
NV_PN	600-1G411-BASE-100		
PCB REV	1G411-A01	PAGE	33 OF 38
BOM REV	A	DATE	29-MAR-2016

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PCB REV	1G411-A01	PAGE	34 OF 38	
BOM REV	A	DATE	29-MAR-2016	

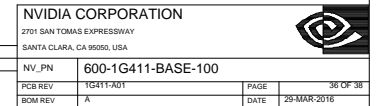
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PCB REV	1G411-A01	PAGE	34 OF 38
BOM REV	A	DATE	29-MAR-2016

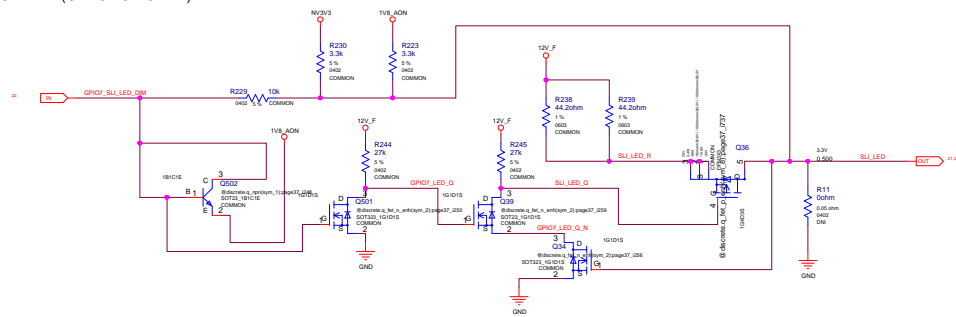
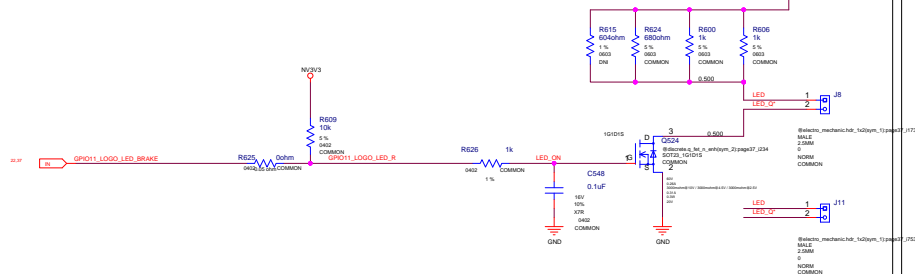
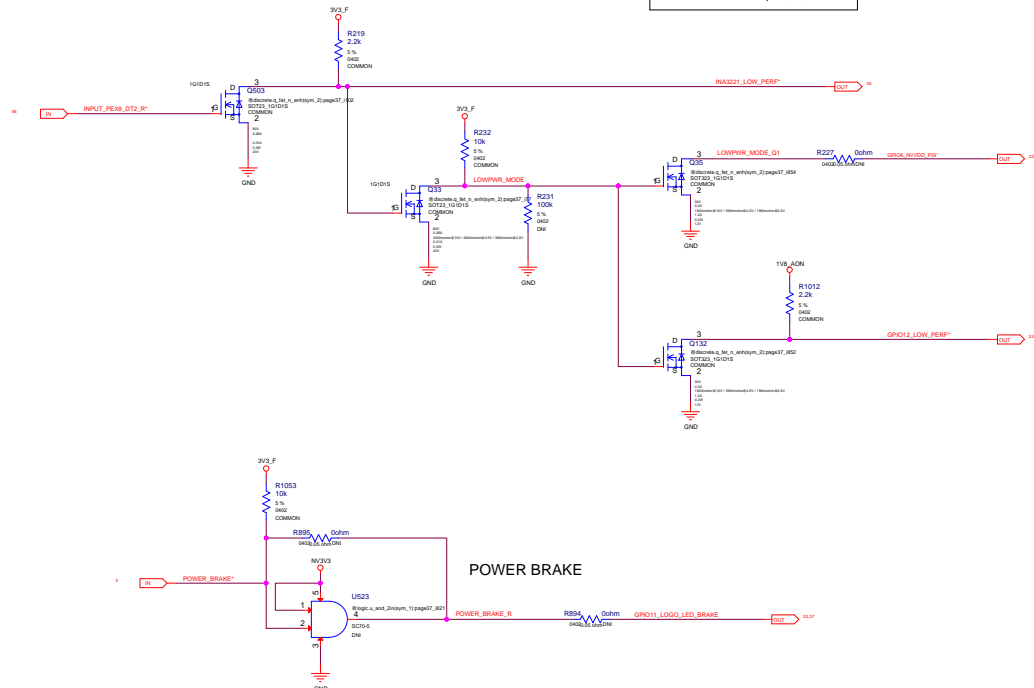
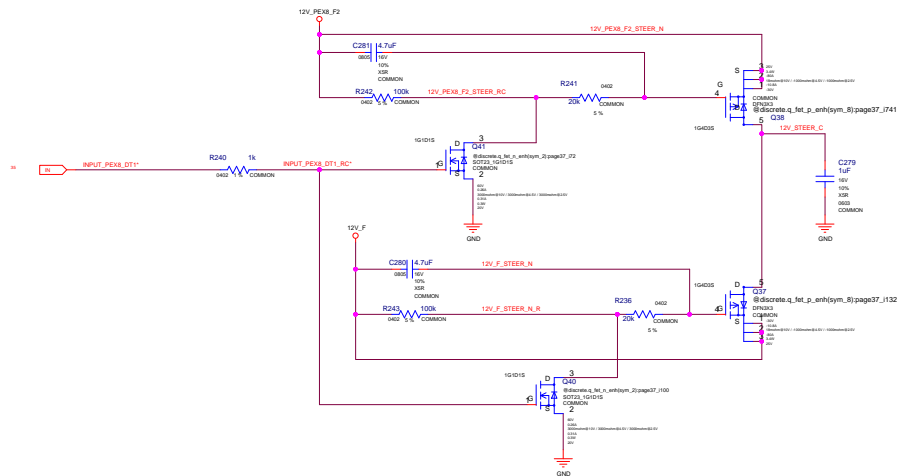
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NV_PN	600-1G411-BASE-100
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PCB REV	1G411-A01	PAGE	35 OF 38
BOM REV	A	DATE	29-MAR-2016





Brackets:



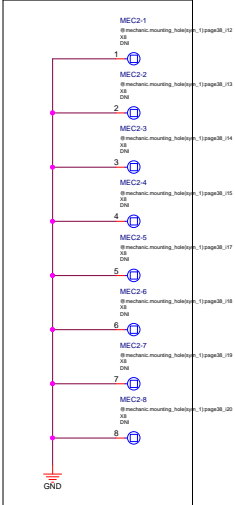
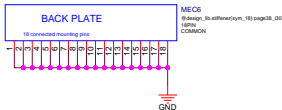
BGA SOCKET ASSY



GPU Stiffner



Mechanical Holes Symbol



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NV_PN	600-1G411-BASE-100	PAGE	38 OF 38
PCB REV	1G411-A01	DATE	29-MAR-2016
BOM REV	A		