P561: G98, DDR2 MEMORY 32MX16/16Mx16/64MX16

Page 1: P561 Overview

Page 2: PCI Express Interface

Page 3: Frame Buffer Interface

Page 4: Memory 1st Bank 0..31

Page 5: Memory 1st Bank 32..63

Page 6: DACA, Slim DB15 Connector

Page 7: DACC,2x6 Header

Page 8: VIDEO CONNECTORS: MiniDIN

Page 9: TMDS Interface

Page 10: UNUSED SECTIONS FOR G98

Page 11: Straps, Mechanical Parts

Page 12: XTAL, GPIO, BIOS, FAN, JTAG, HDCP, SPDIF

Page 13: Power Supply I: NVVDD, PLLVDD

Page 14: Power Supply II: F3V3, 5V, DDC5V, FBVDDQ

Page 15: Basenet Report

Page 16: Cref Part

REV HISTORY

History 10 96/09/27 page 08 add AV_OUT

page 13 change Q1, Q2 to TO252

page 14 add FBVDDQ-linear block, change U2 footprint

96/09/28 page 07 change J4 footprint page 12 add J7 (co-lay J6)

add R572 for RT9259A, R570 footprint change to 0805, page 13

change L11, C11, C12, C31 footprint

page 14 remove PWM block

add D20, D21, C211, C212, C213, C214

96/10/01 page 14 add R210, R211 page 09 add R75~R88, R63~R69, L15~L21 for DVI (EMI solution)

96/10/02 page 12 add FAN Control Function

96/10/03 page 09 and netname (Between common Choke and DVI connector)

96/10/05 page 12 cnage Y501 (4 pin to 2 pin)

96/10/12 page 12 add L30, remove L10

96/10/12 baseon PCB:2.0 CIRCUIT DSN CAHNGE to PCB:1.0

ONLY CHANGE page 13 remove PWM solution, ADD linear solutin

remove C301~~C308 (EMI solution for FBVDDQ)

96/10/17 page 11 add CABLE and PCB

96/10/18 page 14 add C301~~C308 (EMI solution for FBVDDQ)

History 20

96/10/03 page 14 remove FBVDDQ-LINNEAR block, add FBVDDQ-PWM function change L15 footprint as CHK4417C_3R3S01, change C35 footprint

96/10/05 page 12 cahnge Y501 (4pin to 2 pin)

96/10/09 page 11 add FM1~~ FM6 for Fiducial Point

add U301~~U306 for EMI

page 13 add C309 for EMI

page 14 add C301~~C308, C310~~C312 for EMI

96/10/10 page 13 add L30

96/10/11 page 13 remove L10

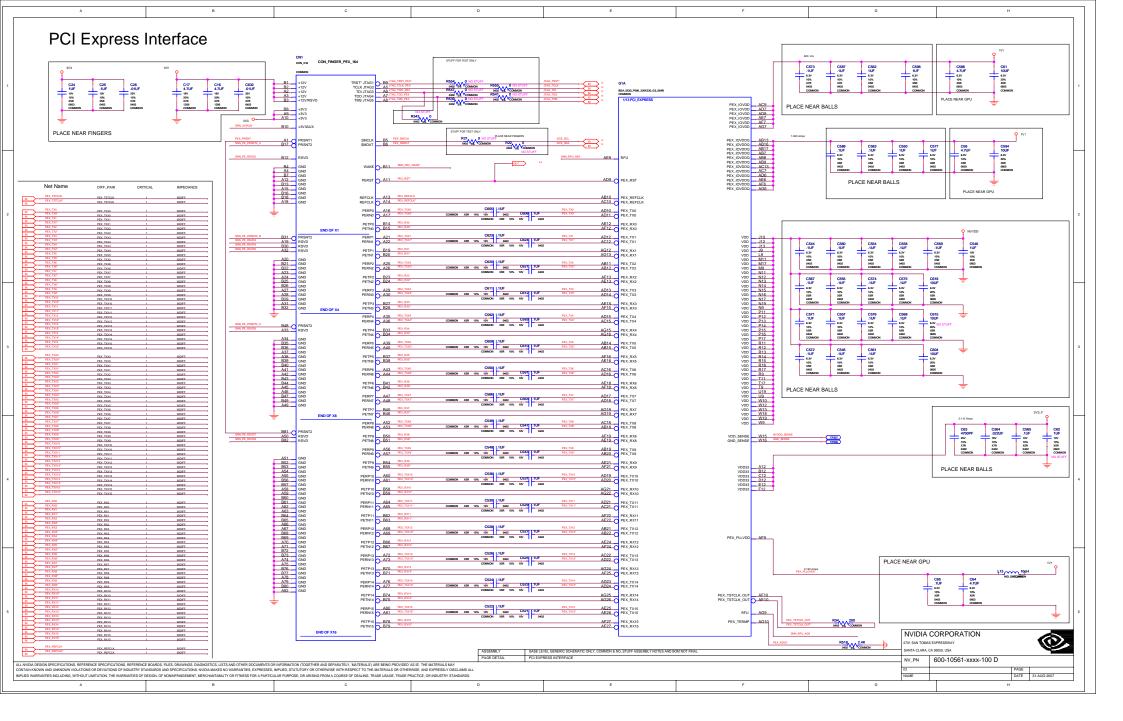
96/10/17 page 11 add cable

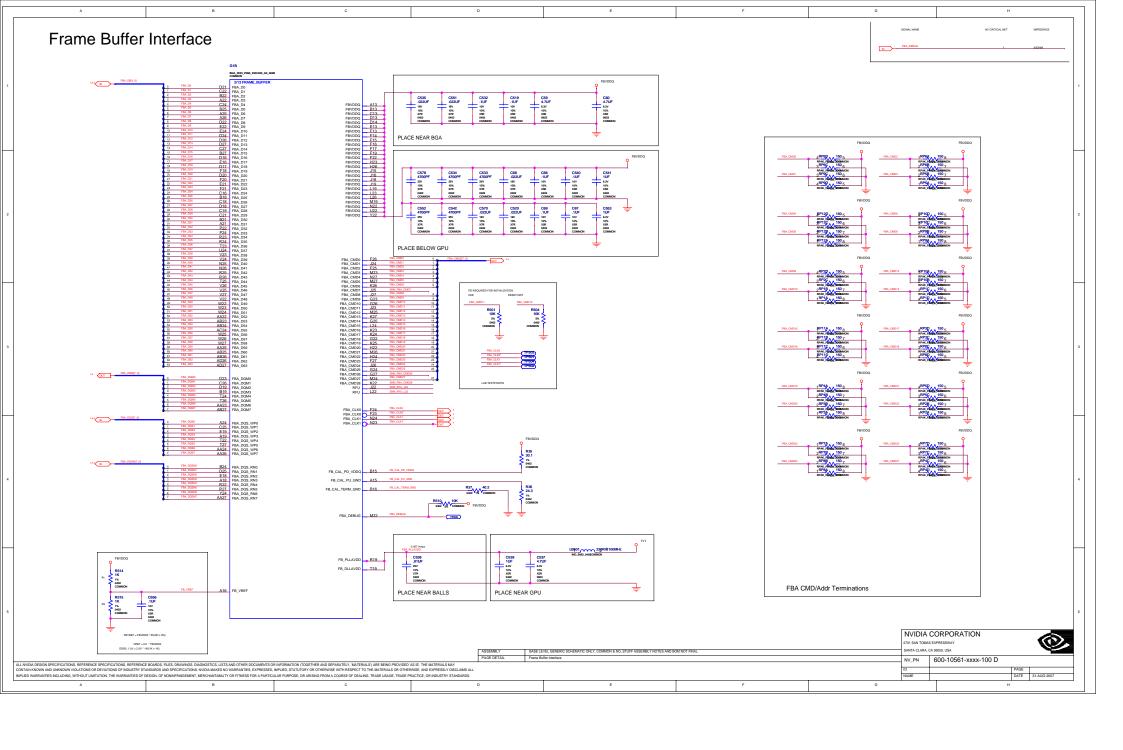
ſ	2003	VARIANT	NVPN	ASSEMBLY
Γ	В	BASE	600-10561-xxxx-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
- 1	-1	SKU0000	600-10561-0000-100	P561: G98-300, 64 BIT DDR2 16Mx16 MEMORY, VGA+DVI+HDout
- 1	2	SKU0001	600-10561-0001-100	P561: G98-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+HDout
- 1	3	SKU0997	600-10561-0997-100	P561: G98-300, 64 BIT DDR2 32MX16 MEMORY, VGA+DVI+HDOUT
- 1	4	SKU0997	600-10561-0997-200	P561: G98-300, 64 BIT DDR2 32MX16 MEMORY, VGA+DVI+HDOUT
- 1	5	SKU0001	600-10561-0001-200	P561: G98-300, 64 BIT DDR2 32MX16 MEMORY, VGA+DVI+HDOUT
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- 1	7	<undefined></undefined>	«UNDEFINED»	<undefined></undefined>
	8	<undefined></undefined>	<undefined></undefined>	<und><underined></underined></und>
- 1	9	<undefined></undefined>	«UNDEFINED»	<undefined></undefined>
- 1	10	<undefined></undefined>	<undefined></undefined>	<und rows<="" th=""></und>
- 1	11	<undefined></undefined>	<undefined></undefined>	<und rows<="" th=""></und>
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- 1	14	<undefined></undefined>	«UNDEFINED»	<undefined></undefined>

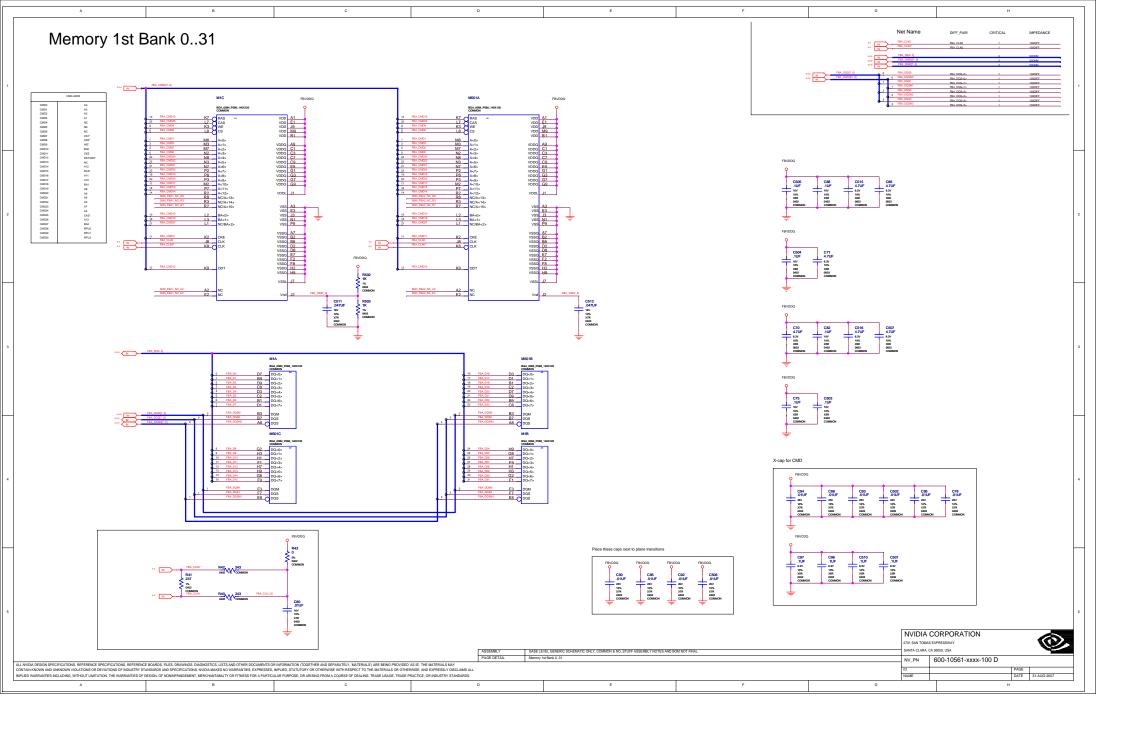
NVIDIA CORPORATION

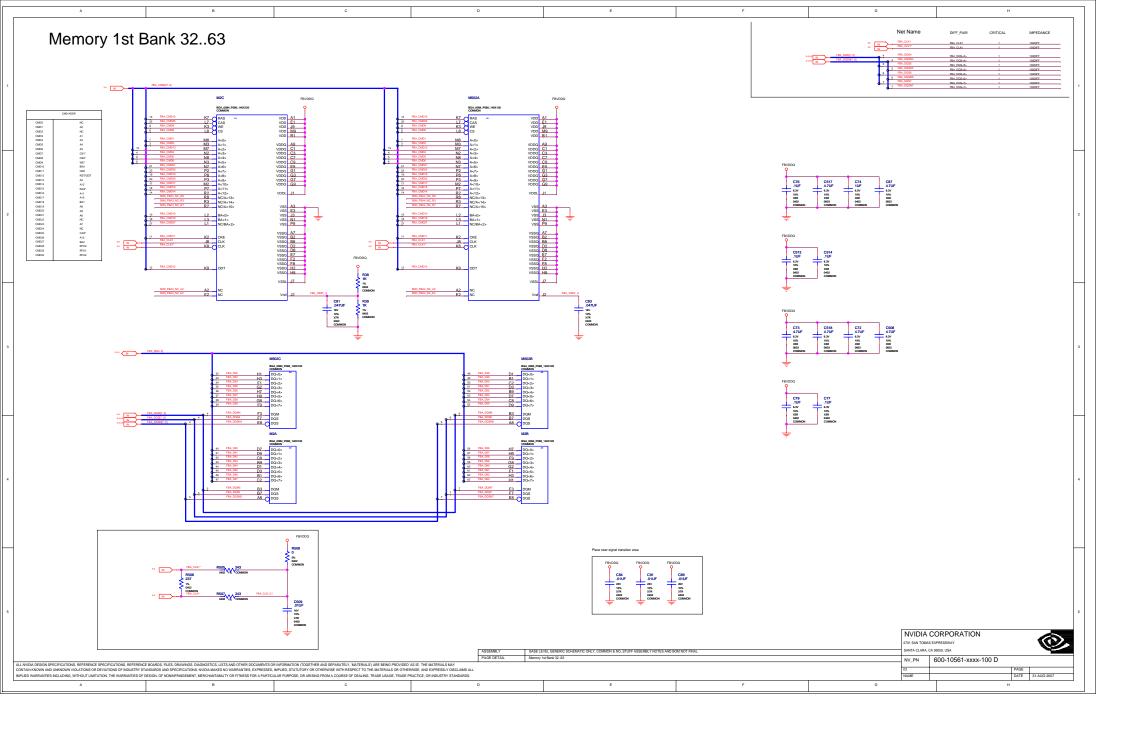
600-10561-xxxx-100 D NV_PN

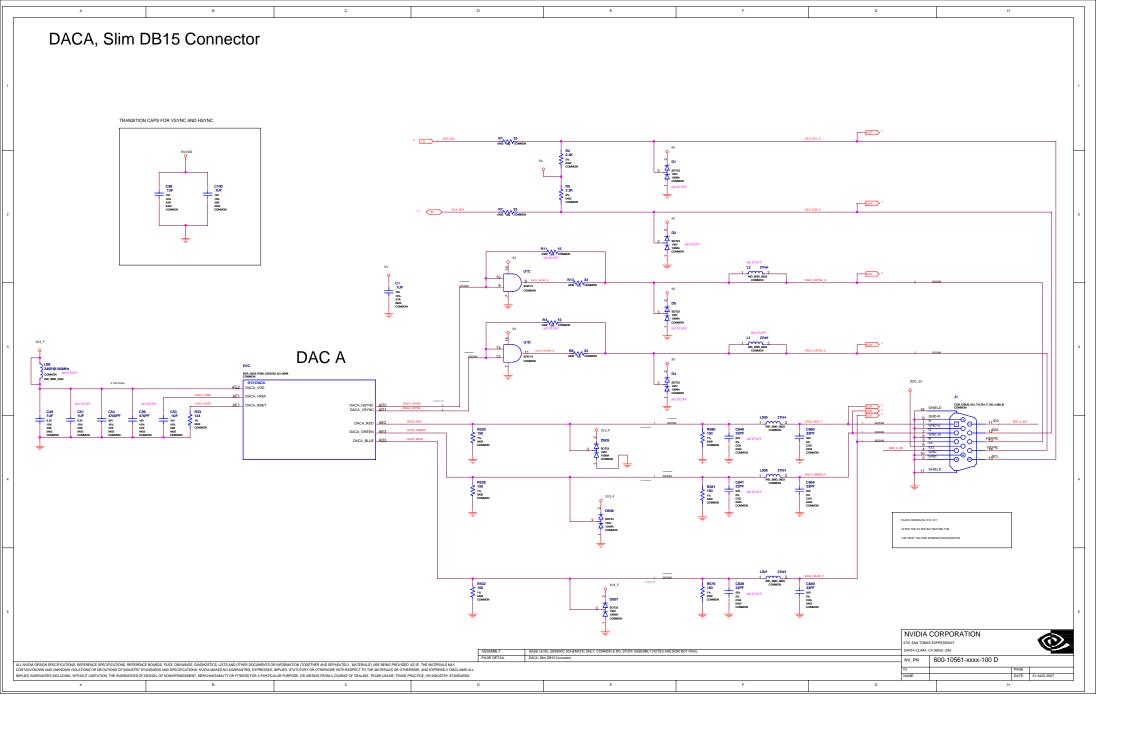
IED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRIN

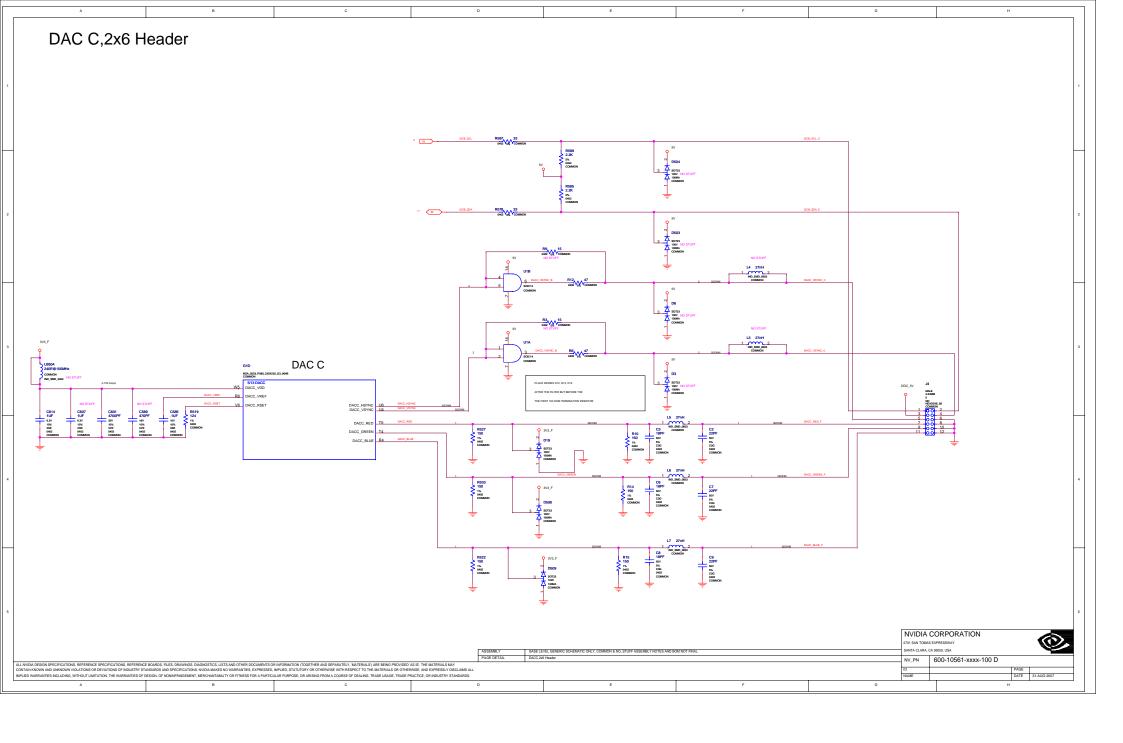


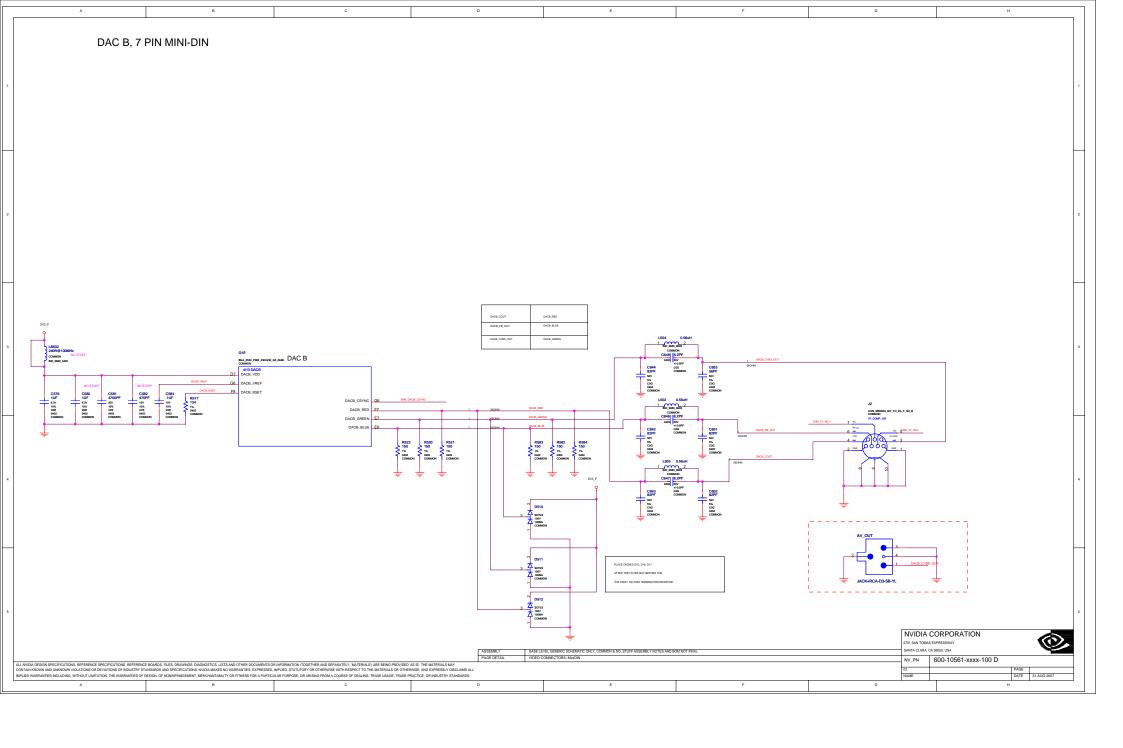


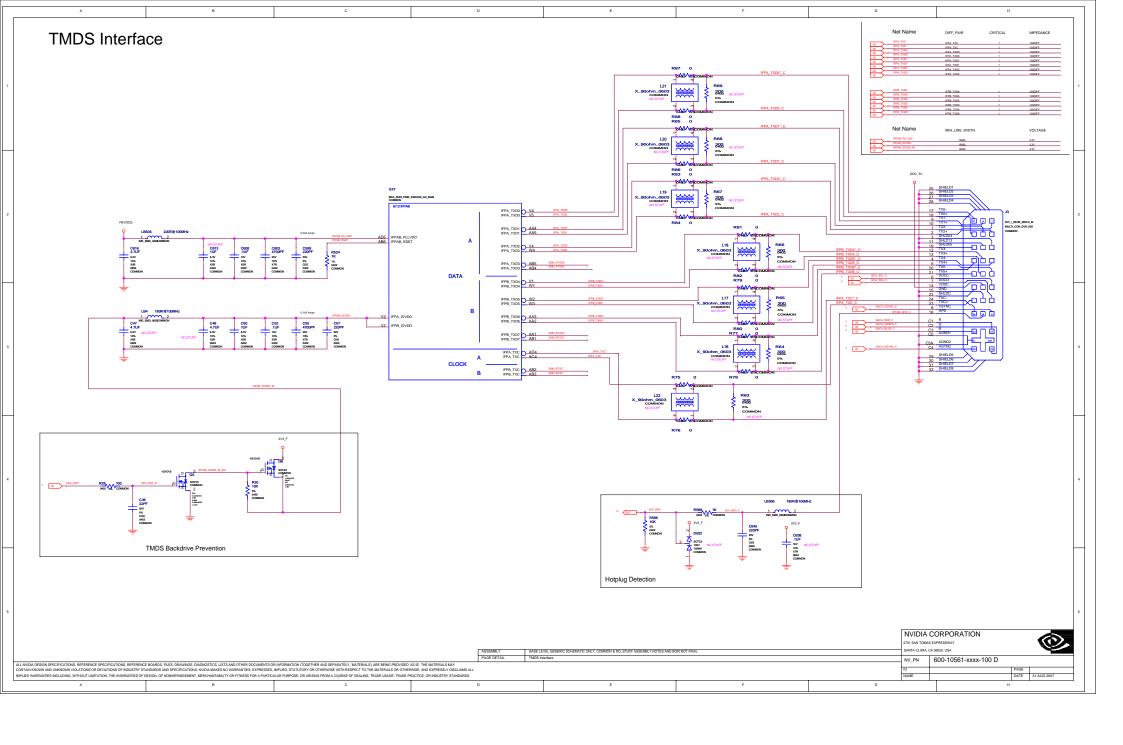


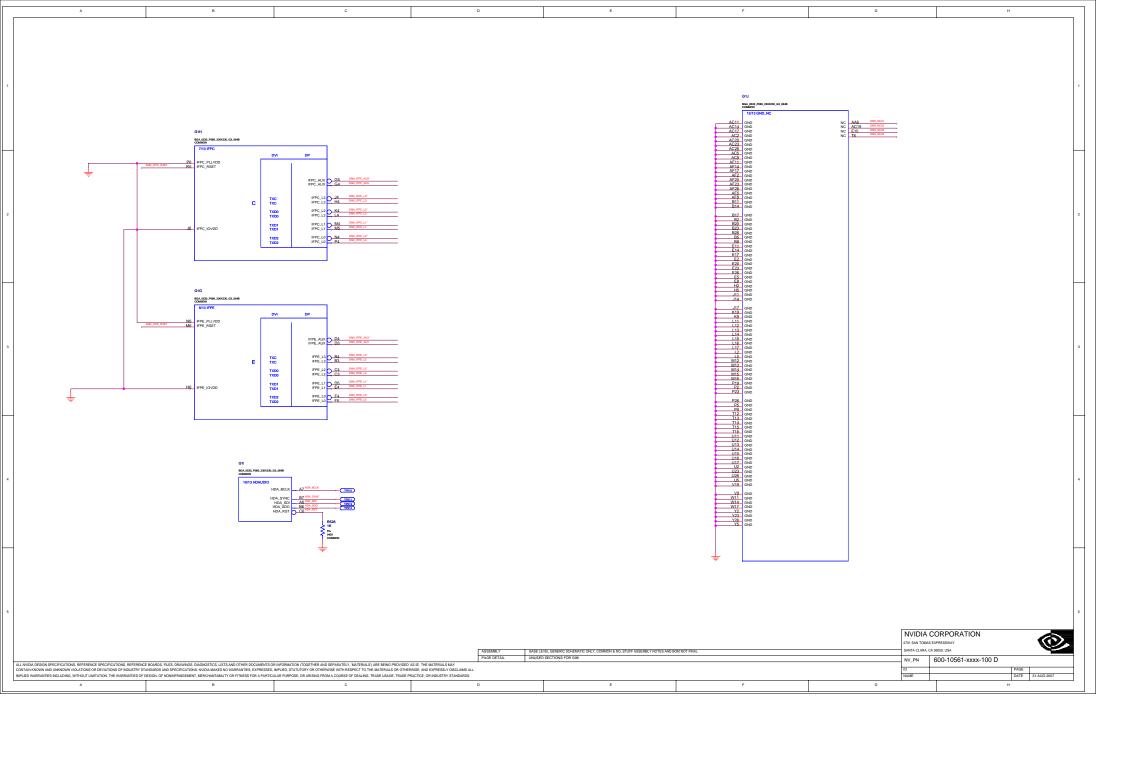




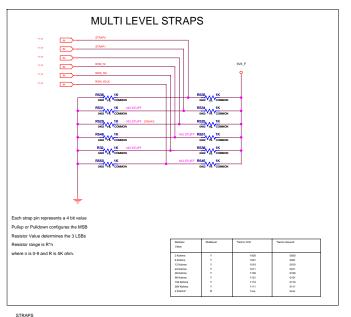
















STRAPHI	3G10 PADCEG LUT ADRIST
STRAPIZE	3G10 PADCEG LUT ADRIZI
ROM SCLK	3G10 PADCEG LUT ADRIS
ROM_SI	SUB VENDOR
ROM SO	NOLK 277
KOM_SO	Man, 411
KONESO	3040_20T
KON_SO	
	STRAP_CAL_PU_CALD0 (RS12) = NO STUFF
PRODUCTION BINARY MODE	
	STRAP_CAL_PU_CALD0 (RS12) = NO STUFF

STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz (MULTI LEVEL) R511= 40K, R512=40K

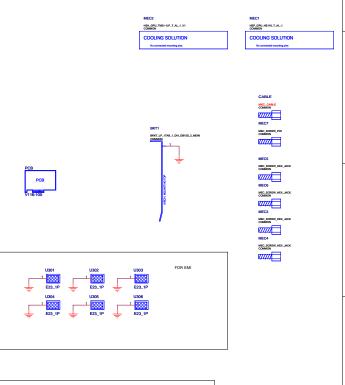
STRAP(I) STRAP(I)	USER[3.0]
STRAP[2] ROM_SCLK	SGD_PACCEG_LUT_ADR(\$1.0] PCI_DEVID[1.0] PCI_DEVID_EXT_SUB_VENDOR, \$1.0T_CLK_CFG, PEX_PLI_EN_TERMHOD
ROM_SI ROM_SO	RAMOTICIA. () XCLK_277, TVMODRIJZ. ()
	ROM_SCLK ROM_SI

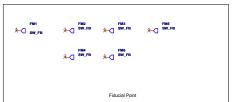
STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz (BRINGUP BINARY) R511= NO STUFF, R512=NO STUFF

3V3_F	GND	PIN(SIGNAL)	FUNCTION
	SK SK SK	STRAP[0] STRAP[1] STRAP[2] ROM SCLK	SCHE, PACCICE, LUT, JORGIN SCHE, PACCICE, LUT, JORGIN SCHE, PACCICE, LUT, JORGIN SCHE PACCICE, LUT, JORGIN
sk sk		ROM_SI ROM_SO	DIA VENDOS NEIX, 277

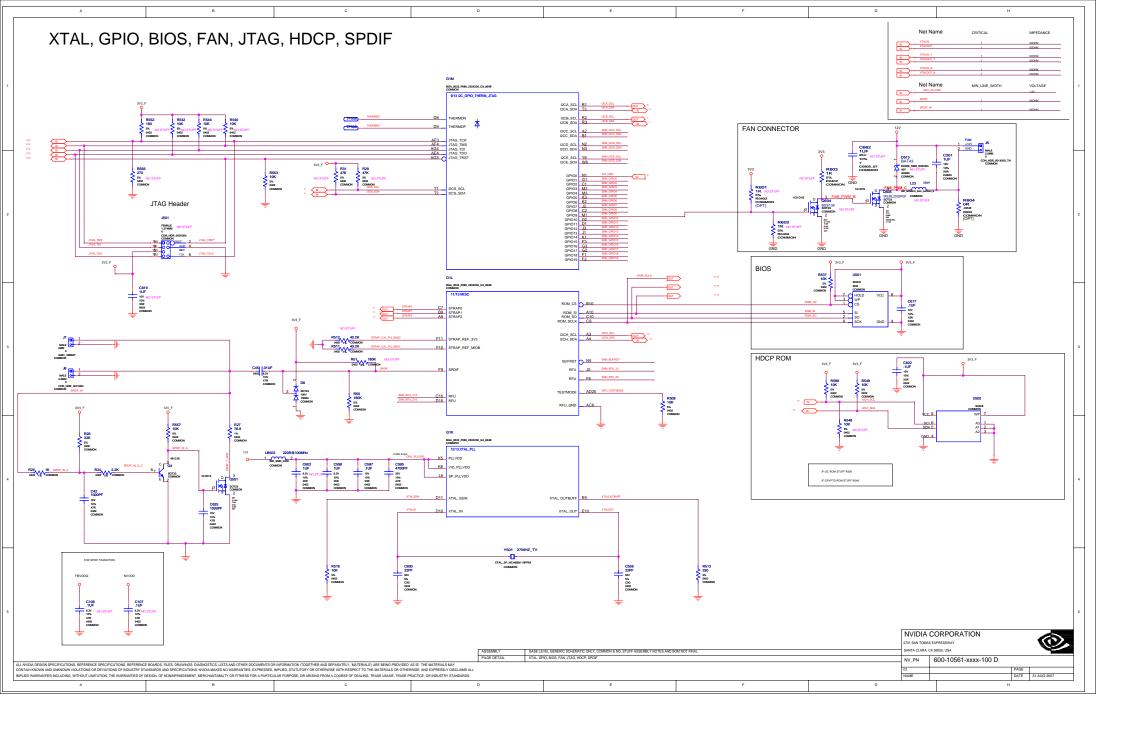
STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz (PRODUCTION BINARY) R511= 40K, R512= NO STUFF

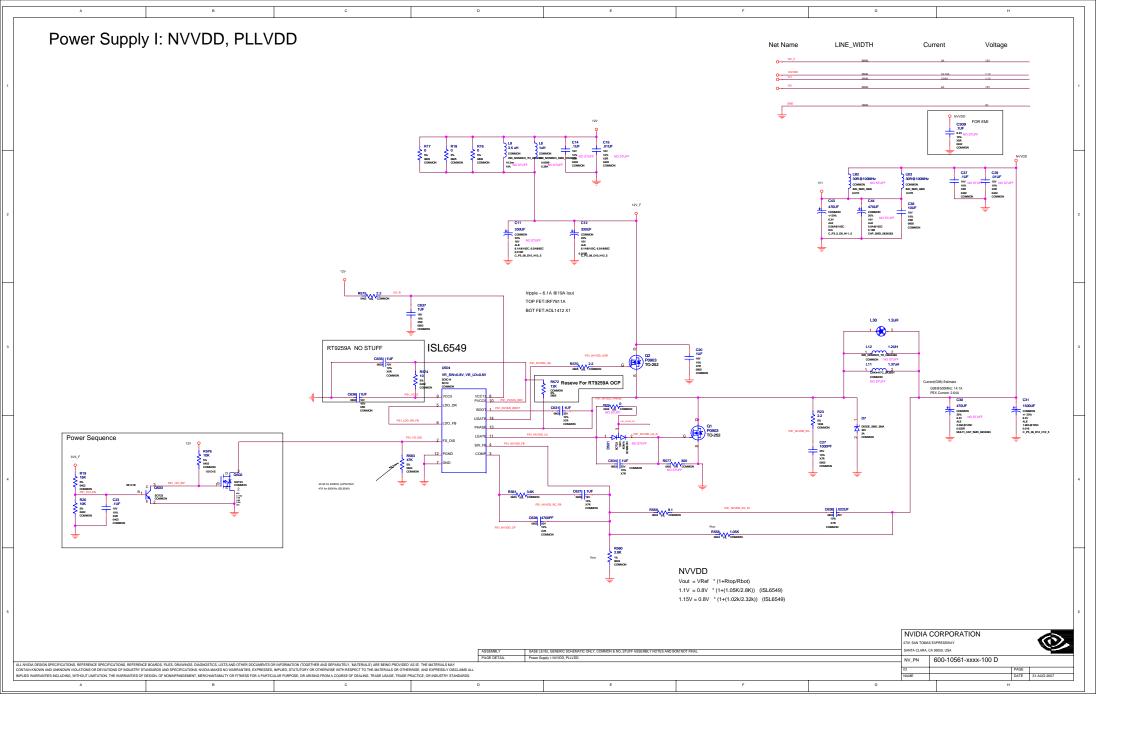
3V3_F	GND	PIN(SIGNAL)	FUNCTION
SK SK		STRAP(0)	RAMCFG[0]
SK		STRAP[1]	RAMCFG[1]
sk		STRAP[2]	RAMCFG[2]
	SK	ROM_SCLK	PCI_DEVID[3]
	SK	ROM_SI	PC_DEVID_EXT
SK		ROM_SO	NCLK, 277



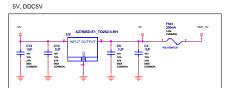


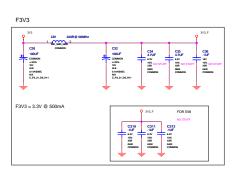
							NVIDIA CORPORATION				
								2701 SAN TOMAS EXPRESSWAY			
				BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL				NTA CLARA, CA 95050, USA			
	PAGE DETAIL Strape, Machanical Parts							600-10561-xxxx-100 D			
CONTAIN KNOWN AND UNKNOWN VIOLATIONS OF DEVIATIONS OF INDUSTRY STA	NINDA DESIGN PECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE SOURCE, BEES DRAININGS, DUAGNOSTICS, LISTS AND OTHER DOCUMENTS OR REFORMATION (OFFICIAL PROJECT AND THE PROJEC										
INFLED WARRANTES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF DOWNFRINGEMENT, HERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DELINIO, TRADE USING, TRADE PRACTICE, OR INDUSTRY STANDARDS.								DATE	31-AUG-2007		
A	В	c	D	E	F	G		н			



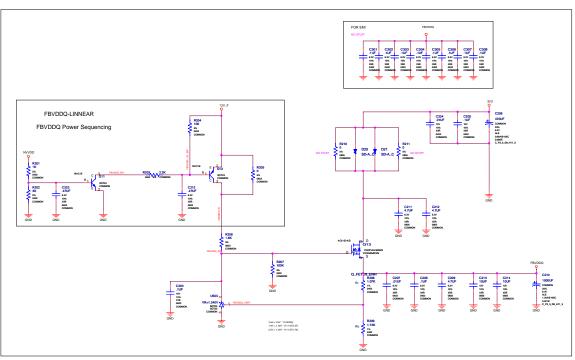


Power Supply II: 5V, DDC5V, F3V3, FBVDDQ









FBVDDQ = 2.0V @ 2.6A

Title: Basenet Report
Design: p561
Date: Aug 15 1:38:59 2007 5.28 5.2C FBA_CMD<19> 3.3C 3.3F 4.28 4.2C PS1_12V_EN* 13.4B PS1_FS_DIS 13.4C 3.48 4.1G 4.4D PEX_RX4 5.2B 5.2C FBA DQS<3> 3.48 4.1G 4.4D PEX RX4° 23C 2.4Ac PS1 LDO DR FB 13.4C SNN IZCE SDA 12.2E FBA_CMD-20> 3.9C 3.3F 4.2B 4.2C 5.2B 5.2C FBA CMD<21> 3.3C 3.3G 4.2B 4.2C pd61 lib.P561(Rp561 lib.p561(sch 1) FBA DQS<6> 3.48 5.1G 5.4D PEX_RX6* 2.3C 2.5A PS1 NVVDD DR 13.4E SNN_IFPC_L0 10.2C SNN_IFPC_L0* 10.2C Base Signal Location([Zone][dir] 5.2B 5.2C FBA_DQS<7> 3.48 5.1G 5.4D 2.3C 2.5Ac PS1_NVVDD_FB 13.4D FBA_CMD<23> 3.9C 3.9G 428 420 FBA_CMD<23> 3.9C 3.4F 428 420 PEX_RX7
PEX_RX7*
PEX_RX8 PS1_NVVDD_LG 13.4D PS1_NVVDD_LG_D 13.4E PS1_NVVDD_PHASE 13.3E SNN_IFPC_L1 10.2C SNN_IFPC_L1* 10.2C SNN_IFPC_L2 10.2C FBA_DQ8N<7.0> 3.4A<>4.1G<4.4A</br> 5.2B 5.2C 5.1G< 5.4A< 2.4C 2.5Ac 3V3 14.1G 3V3_F 14.1G 5V 14.1G 12V 13.1F 12V_F 13.1F 12V_PS2_R 14.2C 12V_R 13.3C DACA_BLUE 6.4C FBA_CMD<24> 3.3C 3.4F 4.2B 4.2C FBA_CMD<25> 3.3C 3.4G 4.1B 4.1C FBA_DQSN<1> 3.48 4.1G 4.4B FBA_DQSN<2> 3.48 4.1G 4.4D FBA_DQSN<3> 3.48 4.1G 4.4D PEX_RX8* PEX_RX9 PS1_NVVDD_RC 13.4F PS1_NVVDD_RC_FB 13.4D SNN_IFPC_L2* 10.2C SNN_IFPC_L3 10.2C SNN_IFPC_L3* 10.2C 5.1B 5.1C PEX_RX9* 2.4C 2.5Ac PS1_NVVDD_RC_IN 13.4F FBA CMD<27> 3.3C 3.4G 4.2B 4.2C FBA DQSN<4> 3.48 5.1G 5.46 PEX RX10 2.4C 2.5Ac PS1_NVVDD_UG 13.3D SNN IFPC RSET 10.2A FBA_DQSN-55> 3.48 5.1G 5.48 FBA_DQSN-65> 3.48 5.1G 5.4D FBA_DQSN-7> 3.48 5.1G 5.4D PEX_RX10° PEX_RX11° PEX_RX11° PS1_NVVDD_UGR 13.3E PS1_PVCC5_DRV 13.3D PS1_VCC5 13.3C SNN_IFPE_AUX* 10.3C SNN_IFPE_L0 10.3C 5.28 5.2C 528 5.2C FBA_D<0> 3.18 4.38 FBA_D<32.0> 4.3A<> 2.4C 2.5A DACA BLUE F 6.4G> 9.3G< 3.1Ac> 4.1G< 5.3Ac FBA PLLAVDD 3.5C PEX RX12 2.4C 2.5Ac PS2 12V EN 14.4A SNN IFPE LOT 10.3C DACA_GREEN_F 63G> 93G-FBA_Dx83.0> 3.1A> 4.1G< 5.3A< FBA_Dx1> 3.1B 4.3B PEX_RX12* PEX_RX13 2.4C 2.5Ac 2.5Ac 2.5C PS2_FBVDD_BOOT 14:3D PS2_FBVDD_CP 14:4D PS2_FBVDD_FB 14:3D SNN_IFPE_L1 10.3C SNN_IFPE_L1 10.3C SNN IFPE L2 10.3C DACA HSYNC 6.3C FBA, D-d> 3.18 4.38 FBA, D-d> 3.18 4.48 FBA D-2> 3.18 4.38 FB_CAL_PD_VDDQ 3.4C PEX RX13* 2.5A< 2.5C PS2_FBVDD_LG 14.3D PS2_FBVDD_PHASE 14.3D 14.3E 14.3F PS2_FBVDD_RC 14.3F DACA HSYNC B 62D PEX_RX14 2.5A< 2.5C SNN IFPE L2* 10.3C DACA_HSYNC_C 62G>93G4 DACA_RED 64C FB_CAL_PU_GND 3.4C FB_CAL_TERM_GND 3.4C PEX_RX14* SNN_IFPE_L3 10.3C SNN_IFPE_L3 10.3C PEX_RX15 2.5A< 2.50 SNN_IFPE_RSET 10.3A SNN_NC01 10.1G SNN_NC02 10.1G SNN_NC03 10.1G DACA RED F 6:3G> 9:3G-FB VREF 3.5B PEX RX15* 2.5A< 2.5C PS2 FBVDD RC FB 14.4D FB_VREF 3.5B

GND_SENSE 2.4F

GPU_PLLVDD 12.1G<12.4C

GPU_TESTMODE 12.3E PEX_SMCLK PEX_SMDAT PS2_FBVDD_RC_IN 14.4F PS2_FBVDD_UG 14.3D DACA_VSYNC 6:3C PEX_TSTCLK 2.2Ac PS2_FBVDD_UGR 14:3E DACA VSYNC C 63G> 93G+ HDA_BCLK 10.4C PEX TSTCLK* 2.2Ac PS2_FS_DIS 14.3C PS2_LDO_DR_FB 14.3C PS2_NVVDD_EN 14.4A SNN NC04 10.1G DACA_VSYSNC_B 6.3D DACB_BLUE 8.4D HDA_RST HDA_SDI PEX_TSTCLK_OUT 2:5F PEX_TSTCLK_OUT 2:5F 10.4C DACB COUT 8.4F HDA SDO PEX TX0 2.2A<2.2E PS2 PVCC5 DRV 14.3D SNN PE PRSNT2 B 2.2B HDA SYNC 10.4C DACB CVBS OUT 8:3F 8:4G PEX TX0* 2.2A<2.2E PS2 VCC5 14.3C SNN PE PRSNT2 C 2.38 DACB_GREEN 8.4D DACB_PB_OUT 8.4F FBA_D<16> FBA_D<16> FBA_D<17> I2CA_SCL 6.1D<12.1E> I2CA_SCL_C 6.1G>9.2G< PEX_TX1
PEX_TX1*
PEX_TX2 ROM_CS* 12.3E 12.3F ROM_SCLK 11.1A<11.1 11.1A< 11.1A< 12.2F DACB RED 8.3D 3.2B 4.3D I2CA SDA 62D-0 12.1E-0 2.2A<2.2E 12.2F> 12.2F> SNN PE RSVD4 2.2B 12.2F> 12.2F> ROM SI 11.1Ac 11.1Ac 12.3F> FBA_D<18> 328 430 328 430 PEX_TX2* PEX_TX3 DACB RSET 8.38 I2CA SDA C 62G> 9.3G< 2.2A< 2.2E SNN PE RSVD5 2.2B I2CB_SCL DACC_BLUE_F 7.4C 7.4E DACC_BLUE_F 7.4F FBA_D<20> 3.2B 4.3D 3.2B 4.3D 12CB_SCL_C 7.1F PEX_TX3* PEX_TX4 2.2A< 2.3E ROM_SO 11.1Ac 11.1Ac 12.3Fs SNN_PE_RSVD7 2.4B SNN_PE_RSVD8 2.4B IZCB SDA 7.2D to 12.1E to 2.2A<2.3E 12.3F> 12.3F> 12.3F> 12.3F>
SNN_3V3AUX 2.1B
SNN_ATXD3 9.2E
SNN_ATXD3* 9.2E FBA_D-22> FBA_D-23> FBA_D-24> 3.28 4.3D 3.28 4.3D PEX_TX8*
PEX_TX8* SNN_RFU_AE9 2.2E SNN_RFU_AG9 2.5F SNN_RFU_C15 12.3C 12CB SDA C 7.2F DACC_HSYNC 7.3C 3.2B 4.4D 12CH_SDA 12.3E⇔ 12.3F< 2.2A< 2.3E SNN_ATXD3* 9.2E SNN_A_ID0 6.4H SNN_A_ID2 6.4G SNN_BTXC 9.3E SNN_BTXC* 9.3E SNN_BTXD7 9.3E DACC_HSYNC_B 7.2D DACC_HSYNC_C 7.2F DACC_RED 7.4C 7.4E FBA_D<26> FBA_D<26> FBA_D<27> FBA_D<28> FBA_D<29> 3.28 4.4D 3.28 4.4D 3.28 4.4D I2CS_SCL 2.1E-> 12.2C->
I2CS_SDA 2.1E-> 12.2C->
IFPAB_HPD_C 9.9G PEX_TX8
PEX_TX8*
PEX_TX7 2.2A<2.3E 2.2A<2.3E 2.2A<2.3E SNN_RFU_D15 12:3C SNN_RFU_F6 12:3E SNN_RFU_J5 12:3E PEX_TX7* PEX_TX8 SNN_RFU_J22 3.3C SNN_RFU_J22 3.3C DACC RED F 7.4F 3.28 4.40 IFPAB IOVDD 9.1G< 9.3C 2.2A<2.3E DACC RSET 7.38 3.2B 4.4D IFPAB IOVDD IN 9.2G< 9.3B 23A<2.4E DACC_VREF 7.38 DACC_VSYNC 7.9C FBA_D<30> 3.28 4.4D 3.28 4.4D IFPAB_IOVDD_IN_EN 9.48 IFPAB_PLLVDD 9.1Gc 9.2C PEX_TX8* PEX_TX9 SNN_TV_NC1 8.4G SNN_TV_NC2 8.4G DACC_VSYNC_B 7.3D DACC_VSYNC_C 7.3F FBA_D<32> FBA_D<33> FBA_D<34> 3.28 5.38 3.28 5.38 3.28 5.38 #PAB_RSET 9.2C #PA_TXC 9.1G<9.3E 9.3G #PA_TXC* 9.1G<9.3E 9.3G PEX_TX0* PEX_TX10* PEX_TX10* SNN_DACB_CSYNC 8.3C SNN_FBA1_NC_A2 4.3B SNN_FBA1_NC_E2 4.3B SPDIF 12.1G< 12.3C SPDIF_IN 12.1G< 12.3A 12.3A SPDIF_IN_C 12.4A 2.3A<2.4E 2.3A<2.4E DVI_HPD 9.3E> 12.2E< DVI_HPD_F 9.3F FBA_D<35> 3.2B 5.3B 3.2B 5.3B IFPA_TXD0 9.1G< 9.2E 9.20 PEX_TX11
PEX_TX11* 2.3A<2.4E SNN_FBA1_NC_R3 4.28 SNN_FBA1_NC_R7 4.28 SPDIF_IN_G 12.48 SPDIF_IN_G_C 12.4A IFPA TXD0* 9.1G< 9.2E 9.2 2.3A< 2.4E SNN_FBA1_NC_R8 4.2B SNN_FBA2_NC_A2 4.3C SNN_FBA2_NC_E2 4.3C SPDIF_T_GND 12.4B STRAP0 11.1A< 11.1A< 12.90 FBA_CLK0* 3.3D 3.4D> 4.1G< FBA_Dol0> FBA_Dol0> 3.2B 5.3B IFPA_TXD2 9.1G< 9.2E 9.2G PEX_TX13 2.3A< 2.5E STRAP1 11.1Ac 11.1Ac 12.3Co 4.2A< 4.2C< 4.5B< FBA_CLK1 3.3D 3.4D>5.1G IFPA_TXD2* IFPB_TXD4 9.1G< 9.2E 9.26 9.1G< 9.2G 9.38 PEX_TX13* PEX_TX14 SNN_FBA2_NC_R3 4.2C SNN_FBA2_NC_R7 4.2C 11 1Ac 11 1Ac 12 30 5.2A< 5.2C< 5.5B< FBA_CLK1* 3.3D 3.4D> 5.1G< IFPB_TXD4* IFPB_TXD5 PEX_TX14* PEX_TX15 FBA_D+42> 3.28 5.48 3.28 5.48 9.1G< 9.2E 9.2G 9.1G< 9.2G 9.3E 2.3A< 2.5E SNN_FBA2_NC_R8 4.2C SNN_FBA3_NC_A2 5.3B STRAP_CAL_PU_GND1 12:3C 2.3A< 2.5E THERMDA 3.28 5.48 3.38 5.48 3.38 5.48 IFPB_TXD5*
IFPB_TXD6*
IFPB_TXD6* 9.1G< 9.2G 9.3E 9.1G< 9.2G 9.3E 9.1G< 9.2G 9.3E PEX_TXIS* PEX_TXXX PEX_TXXX 23A< 25E 22C 23A< SNN_FBA3_NC_F2 5.3B SNN_FBA3_NC_R3 5.2B SNN_FBA3_NC_R7 5.2B THERMOC XTALIN XTALIN_B 5.2A< 5.2C< 5.5B< FBA_CLK_C0 4.5B FBA_CLK_C1 5.5B FBA_CMD+0> 3.2C 3.2F 4.2B 4.2C FBA_CMD+27.0> 3.2D> 4.1A< 4.1G+ FBA_D+47> 3.38 5.48 3.38 5.30 JTAG_TCLK 2.1E-o 12.1A-c PEX_TXX1
PEX_TXX1* 2.2C 2.3A< SNN_FBA3_NC_R8 5.2B SNN_FBA4_NC_A2 5.3C XTALIN_T XTALOUT 12.1G< 12.1G< 12.4E FBA_D<60>
FBA_D<60>
FBA_D<60>
FBA_D<61>
FBA_D<62>
FBA_D<63> 3.38 5.30 SNN_FBA4_NC_E2 5.3C JTAG_TCLK_PEX 2.1C PEX_TXX2 2.2C 2.3A XTALOUTBUFF 12.4E FBA_CMD<1> 3.2C 3.2F 4.1B 4.1C 3.38 5.3D JTAG_TDI 2.1E-o 12.2A-o PEX_TXX2* 2.2C 2.3A< SNN_FBA4_NC_R3 5.20 XTALOUT_B 12.1Gc 3.38 5.3D 3.38 5.3D 3.38 5.3D PEX_TXX3* PEX_TXX4* 23A< 23C SNN_FBA4_NC_R7 5.2C SNN_FBA4_NC_R8 5.2C SNN_FBA_CMD7 3.3C XTALOUT_T 12.1Gc XTALSSIN 12.4C JTAG_TDIO_PEX 2.1C
JTAG_TDO 2.1E-> 12.2A-> FBA_D-d5-FBA_D-d5-FBA_D-d5-FBA_D-d7-FBA_D-d8-5.1B 5.1C 3.38 5.3D 12.2Ac> PEX_TXX4* 2.3A< 2.3C SNN_FBA_CMD26 3.3C FBA_CMD-4> 32C 32F 52B 52C FBA_CMD-6> 32C 32F 52B 52C 3.38 5.3D 3.38 5.4D JTAG_TMS 2.1E 12.1Ac PEX_TXXS
PEX_TXXS 2.3A< 2.3C 2.3A< 2.3C SNN_FBA_CMD28 3.3C SNN_GPI00 12.2E SNN_GPI02 12.2E SNN_GPI03 12.2E PEX_TXX8* FBA_CMD-6> 3.2G 3.3C 5.2B 5.2C FBA_CMD-8> 3.2G 3.3C 4.1B 4.1C 3.38 5.4D 3.38 5.4D 12.1Ac> JTAG_TMS_PEX 2.1C 2.3A< 2.3C 2.3C 2.4A< 12.2E 12.2E 12.2E 12.2E 12.2E 12.2E 12.2E 12.2E FBA_D<60> FBA_D<61> JTAG_TRST* 2.1E-o 12.2A-o
12.2A-o
JTAG_TRST_PEX* 2.1C PEX_TXX7*
PEX_TXX8* 2.3C 2.4Ac 2.3C 2.4Ac SNN_GPIOS SNN_GPIOS 5.18.5.1C FBA_CMD
45> 3.2F 3.3C 4.18.4.1C 5.1B 5.1C 3.38 5.4D 2.4A< 2.4C SNN_GPIO6 NVVDD 13.1F NVVDD_SENSE 2.4F PEX_PLLDVDD 2.5F PEX_PRSNT 2.18 FBA CMD+10+ 33C 33E 42B 42C PEX_TXXXI
PEX_TXXXI
PEX_TXXXI SNN_GPIO7 SNN_GPIO8 SNN_GPIO9 FBA_D-62> 3.38 5.4D 246-240 528 5.2C FBA_CMD<11> 3.3C 3.3D 4.2B 4.2C FBA_D=63> FBA_DEBUG 2.4A<2.4C 3.1G< 3.40 5.28 5.2C FBA_DQM<0> 3.38 4.38 PEX_TXX10 2.4A< 2.4C SNN_GPIO10 FBA_CMD<12> 3.3C 3.3D 4.2B 4.2C FBA_DQM<7.0> 3.3A> 4.1G< 4.4A PEX_REFCLK 2.2C 2.5Ac PEX_TXX10" 2.4A<2.4C PEX_TXX11 2.4A<2.4C PEX_TXX11" 2.4A<2.4C SNN_GPI011 SNN_GPI012 SNN_GPI013 528 5.2C FBA_CMD<13> 3.2G 3.3C 5.1B 5.1C FBA_CMD<14> 3.3C 3.3G 4.2B 4.2C FBA_DQM<1> 3.3B 4.4B PEX_RST* 2.20> 2.20> 9.4A FBA_DQM<2> 3.3B 4.3D PEX_RST_R 9.4A PEX_TXX12 2.4A<2.4C SNN_GPI014 12.2E 528 5.2C FBA_CMD<15> 3.3C 3.3F 4.18 4.10 FBA_DQM<3> 3.38 4.4D FBA_DQM<4> 3.38 5.38 PEX_RSVD PEX_RX0 PEX_RX0* PEX_TXX12* PEX_TXX13 2.4A< 2.4C 2.4A< 2.5C SNN_GPI015 SNN_GPI016 SNN_GPI017 5.1B 5.1C FBA_DQM<5> 3.38 5.48 2.2C 2.4Ac PEX_TXX13* 2.4A< 2.5C FBA CMD+16> 33C 33E 42B 42C FRA DOM/65 338 530 PFY RY1 220.244 PEX TXX14 2.44-2.50 SNN GPIO18 12.2F PEX_RX1*
PEX_RX2*
PEX_RX2*
PEX_RX3 5.28 5.2C FBA_CMD<17> 3.3C 3.3G 4.28 4.2C 5.28 5.2C PEX_TXX15* 2.4A<2.5C PEX_TXX15* 2.4A<2.5C PEX_TXX15* 2.4A<2.5C FBA_DQS<0> 3.48 4.1G 4.48 SNN_I2CC_SCL 12.1E SNN_I2CC_SDA 12.1E 2.2C 2.4Ac FBA_DQS<7.0> 3.4Ac> 4.1G< 4.4Ac> 2.2C 2.4Ac FBA_CMD<18> 3.3C 3.3G 4.2B 4.2C 5 10 - 5 44 -230.246 PS1_3V3_EN 13.4A SNN_I2CD_SCL 12.1E NVIDIA CORPORATION 701 SAN TOMAS EXPRESSWA ANTA CLARA, CA 95050, USA BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL DAGE DETAIL «edit here to insert page detail» NV PN 600-10561-xxxx-100 D OWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS INVIDIA MAKES NO WARRANTIES EXPRESSED HIM/LED STATLITORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE AND EXPRESSLY DISCLAIMS ALL DATE 31-AUG-2007

