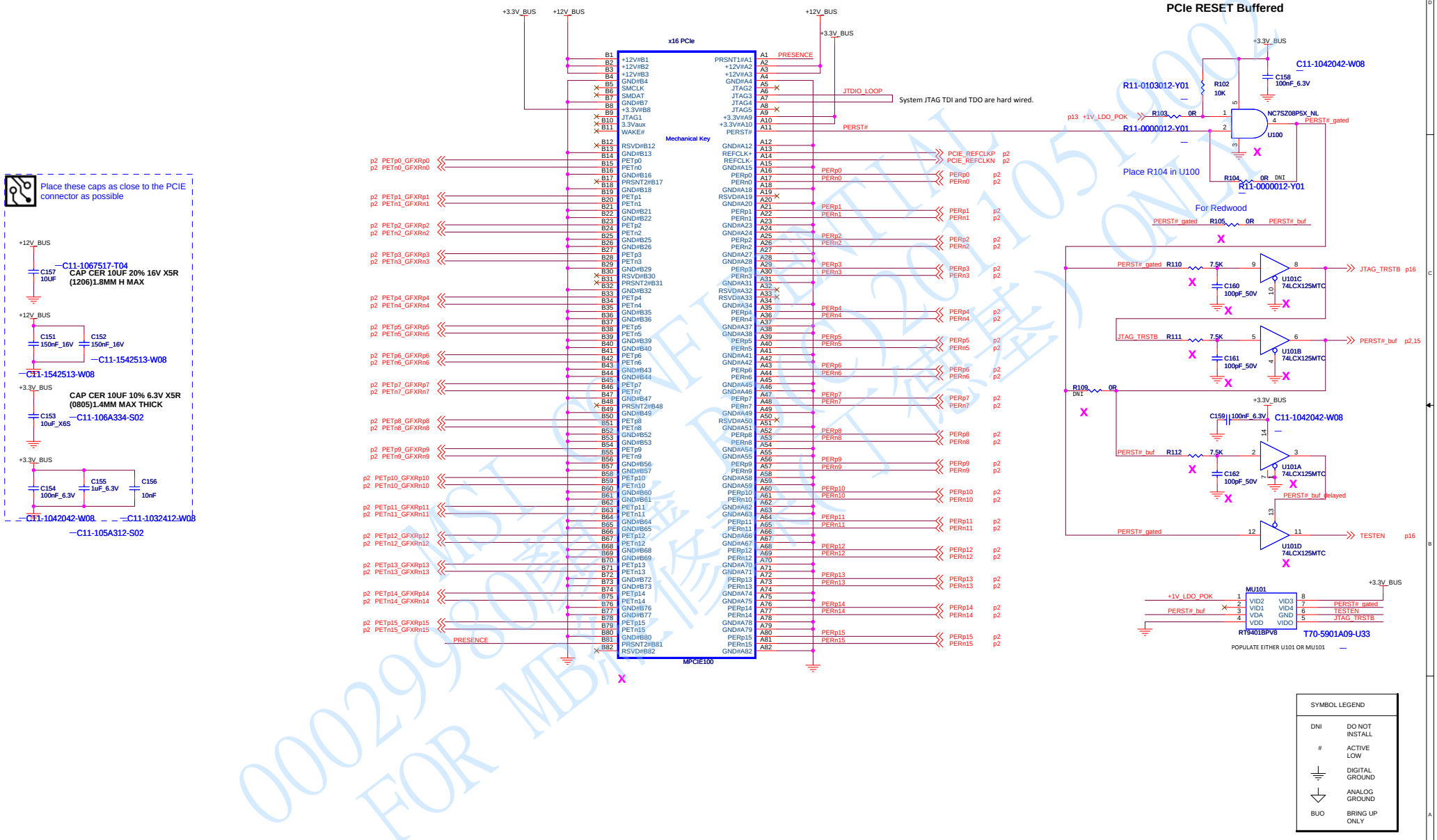
PCI-EXPRESS EDGE CONNECTOR



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Title RH Juniper G5 512MB 4pcs 32Mx32 VGA/DP+HDMI/DP+DVI+L FH 6.6"

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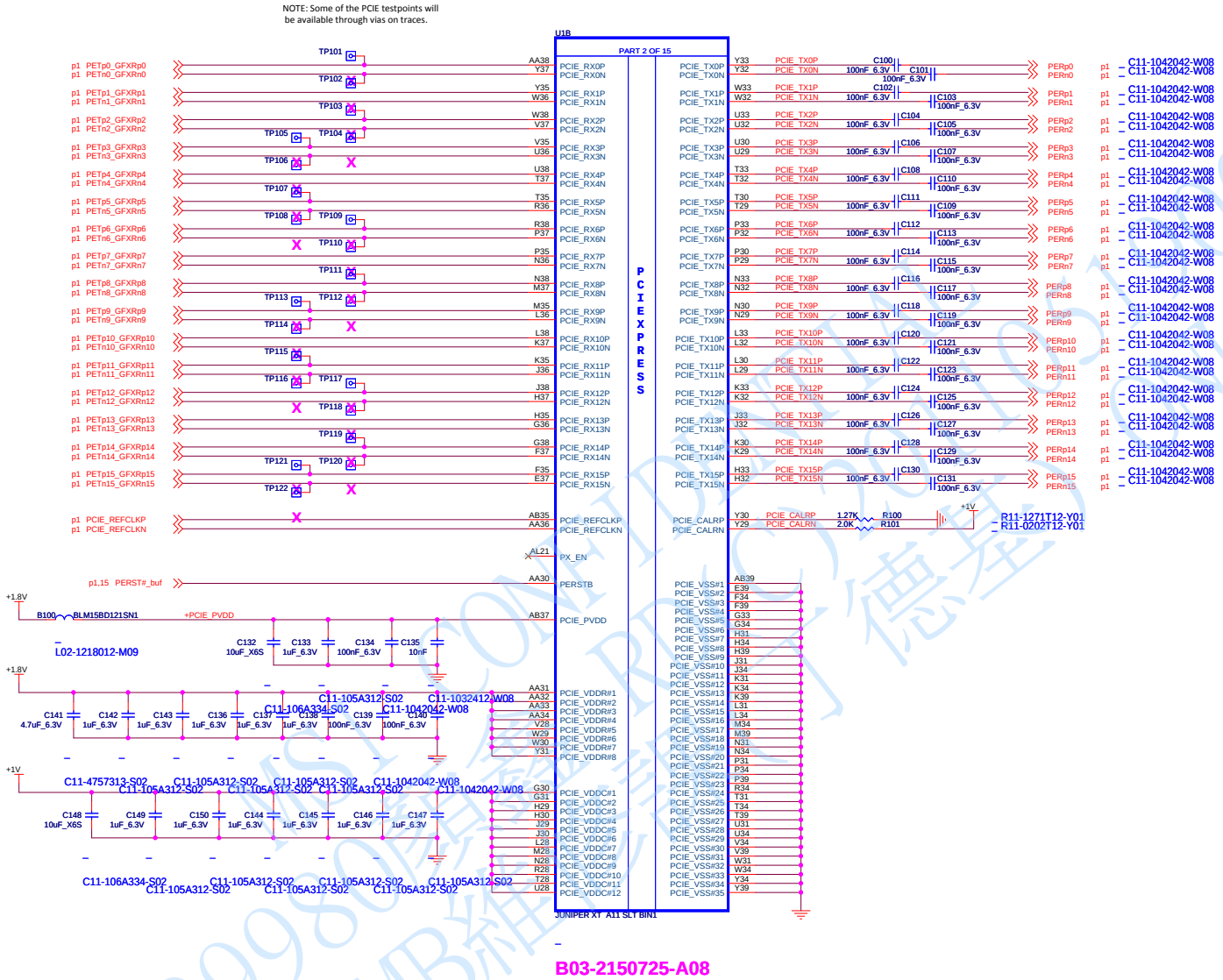
(2) M2 PCIe Interface



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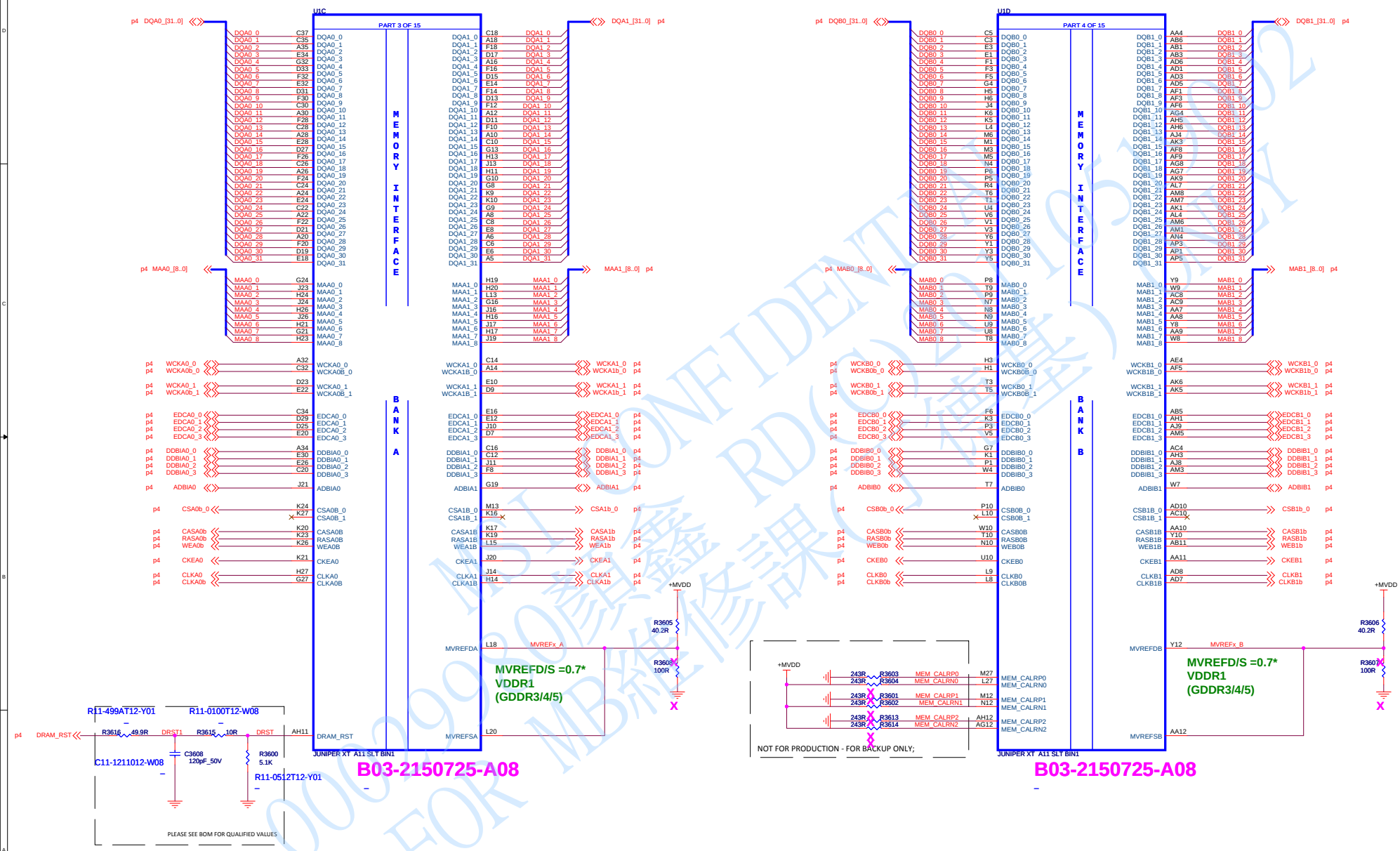
Doc No	

(3) M2 MEM Interface Ch A&B



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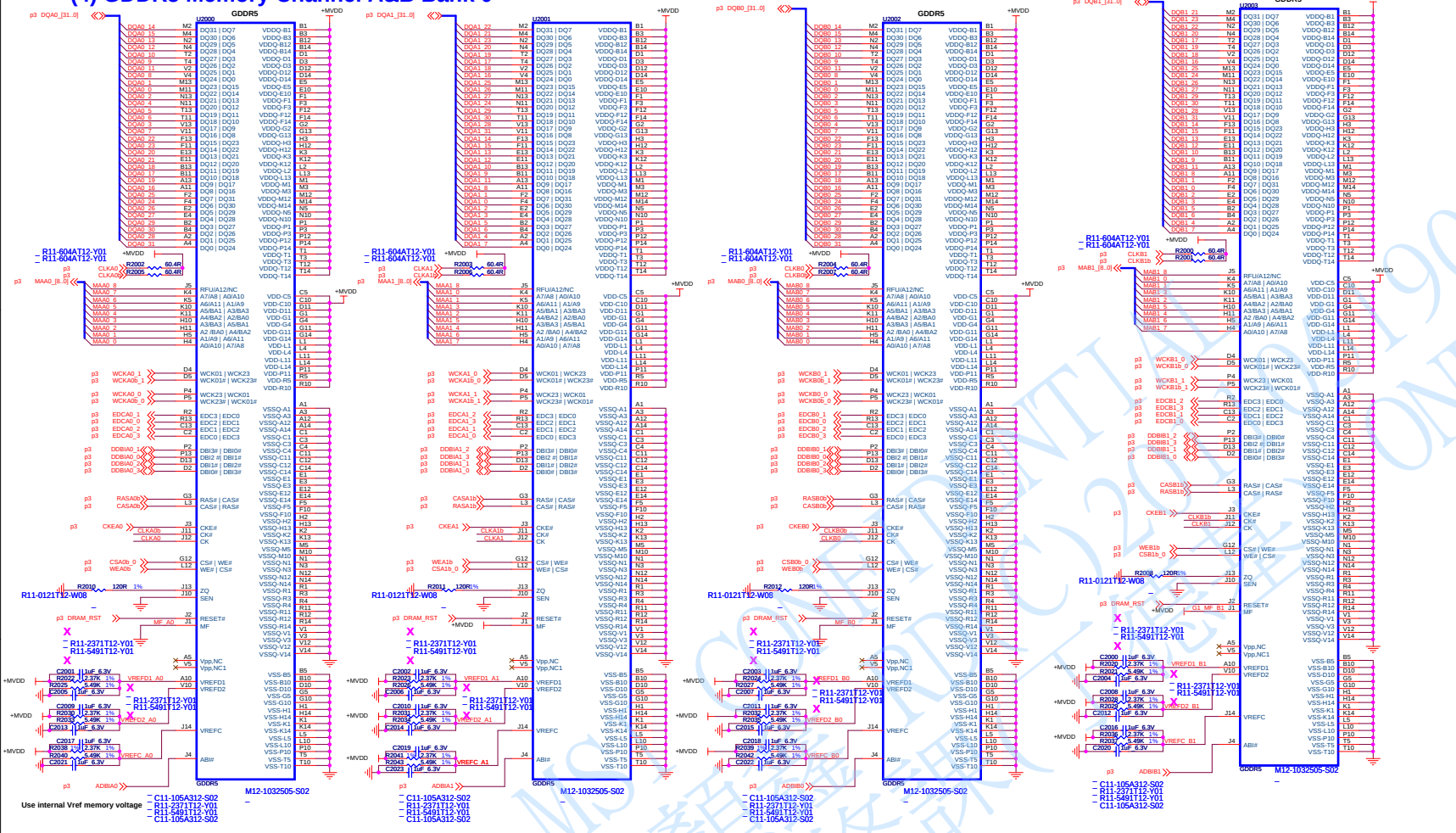
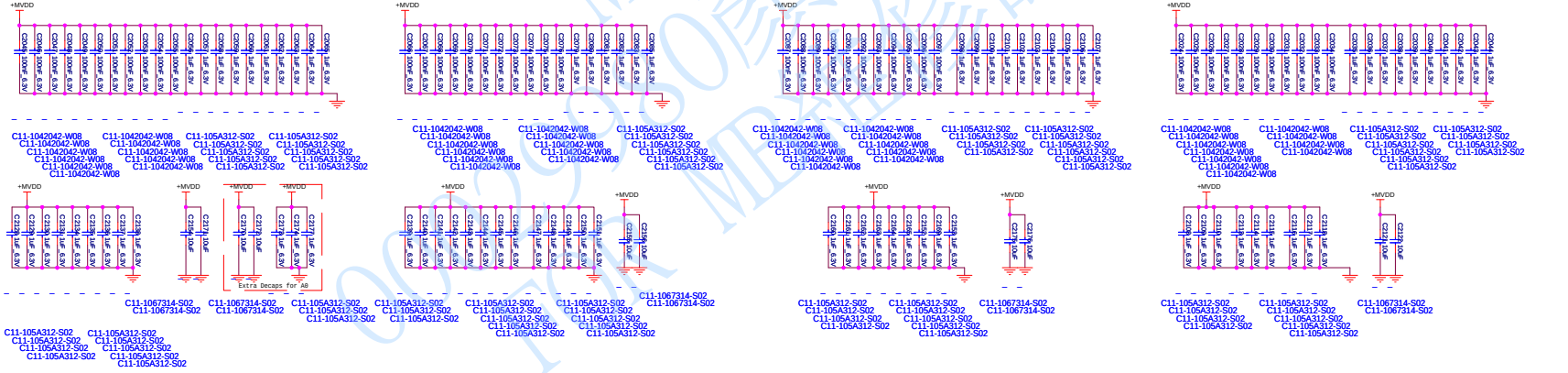
Property	105-C099xx-00B

(4) GDDR5 Memory Channel A&B Bank 0





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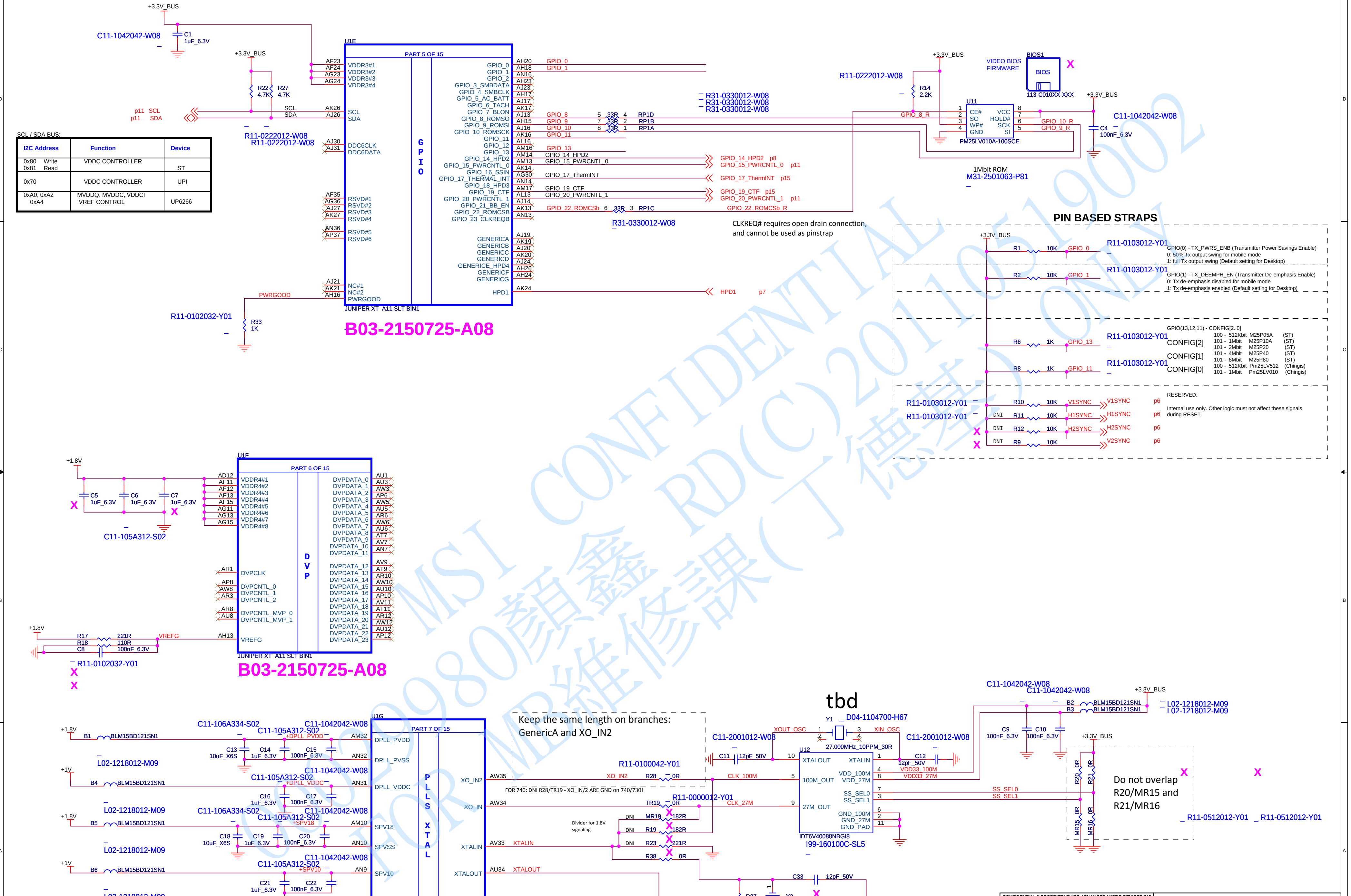
(06) M2 GPIOs Strap CF XTAL OSC



I2C Address	Function	Device
0x80 Write 0x81 Read	VDDC CONTROLLER	ST
0x70	VDDC CONTROLLER	UPI
0xA0, 0xA2 0xA4	MVDDQ, MVDDC, VDDCI VREF CONTROL	UP6266

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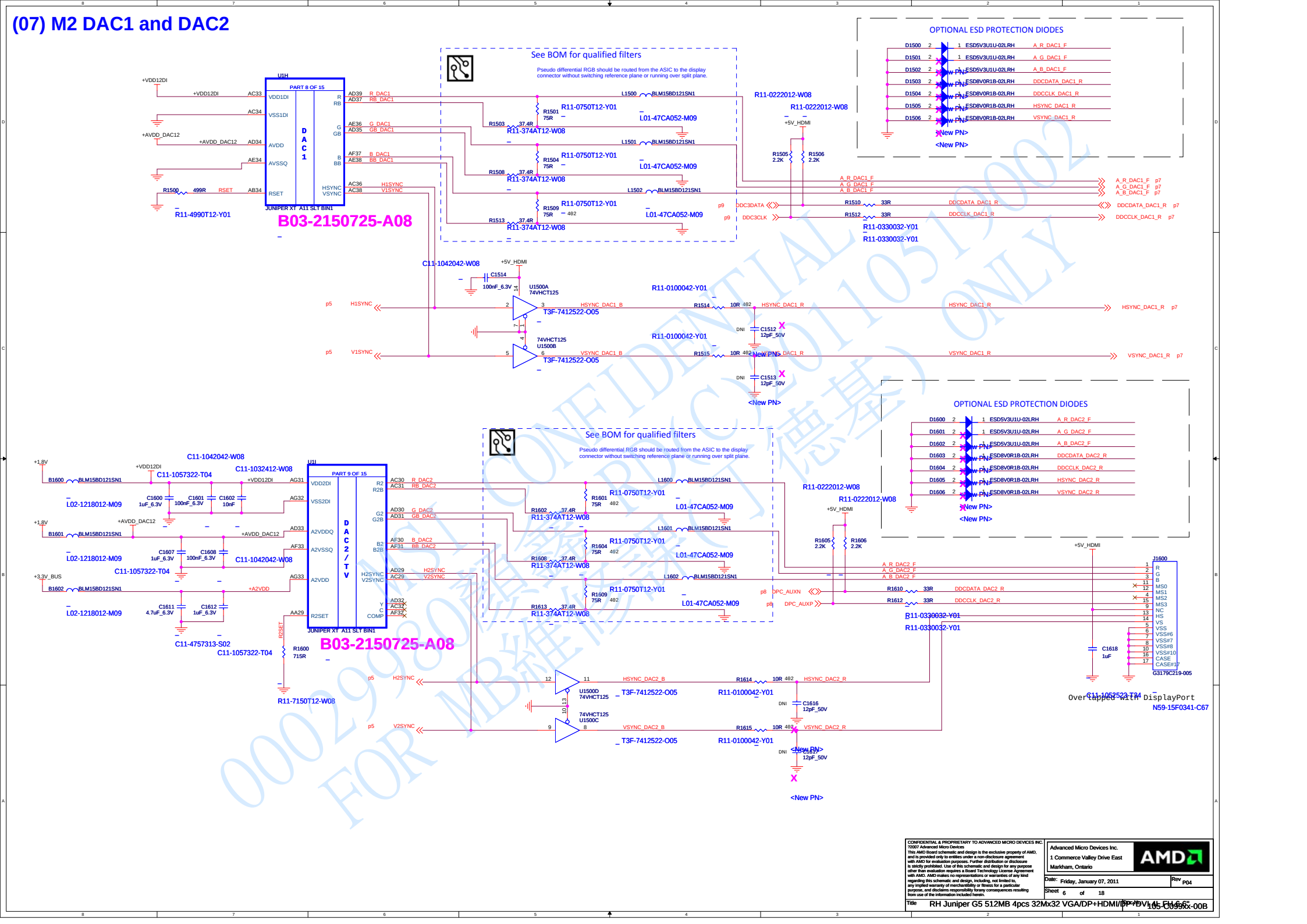
(07) M2 DAC1 and DAC2



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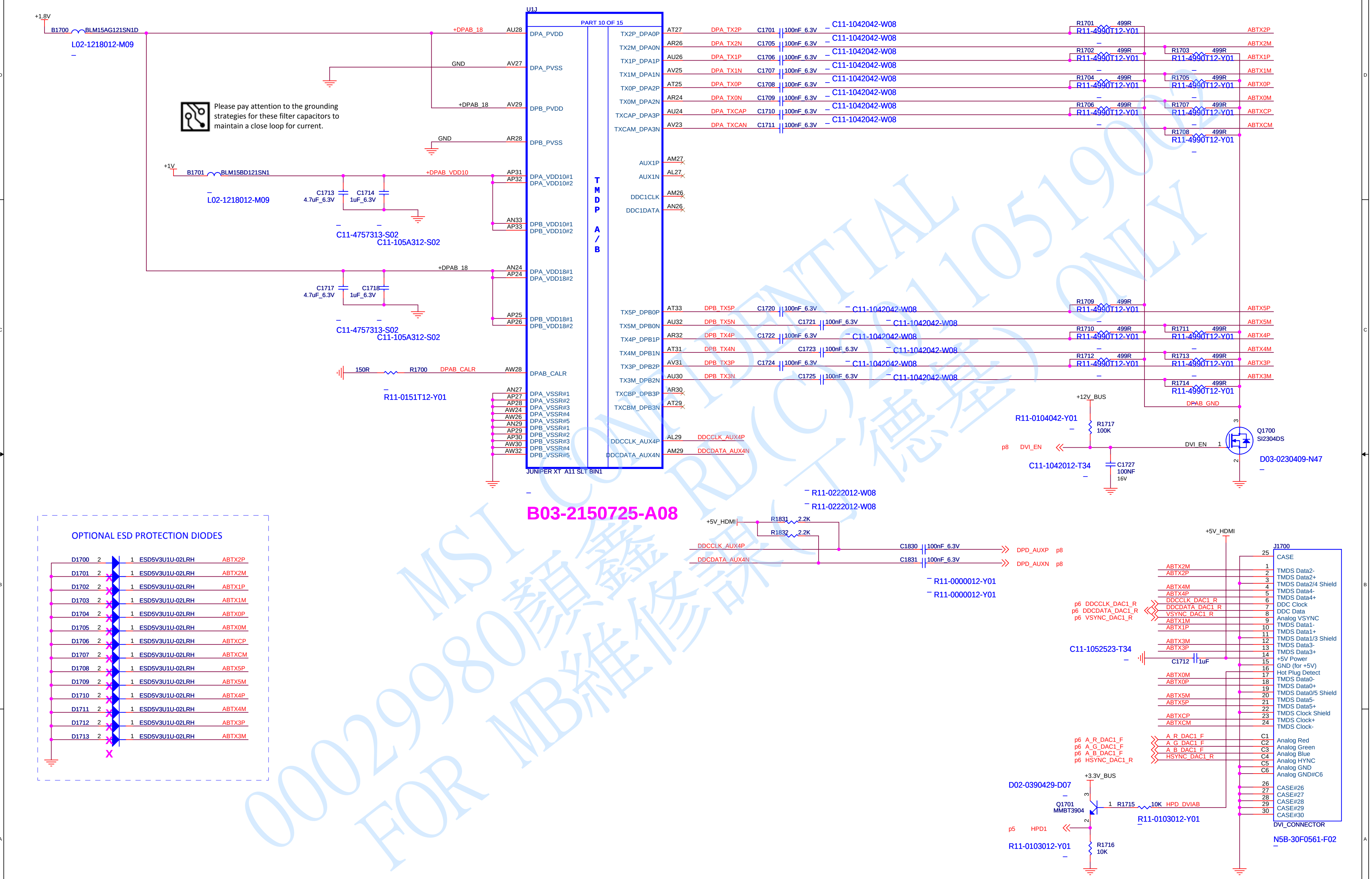
(08) M2 TMDP A&B dDVI-I TOP



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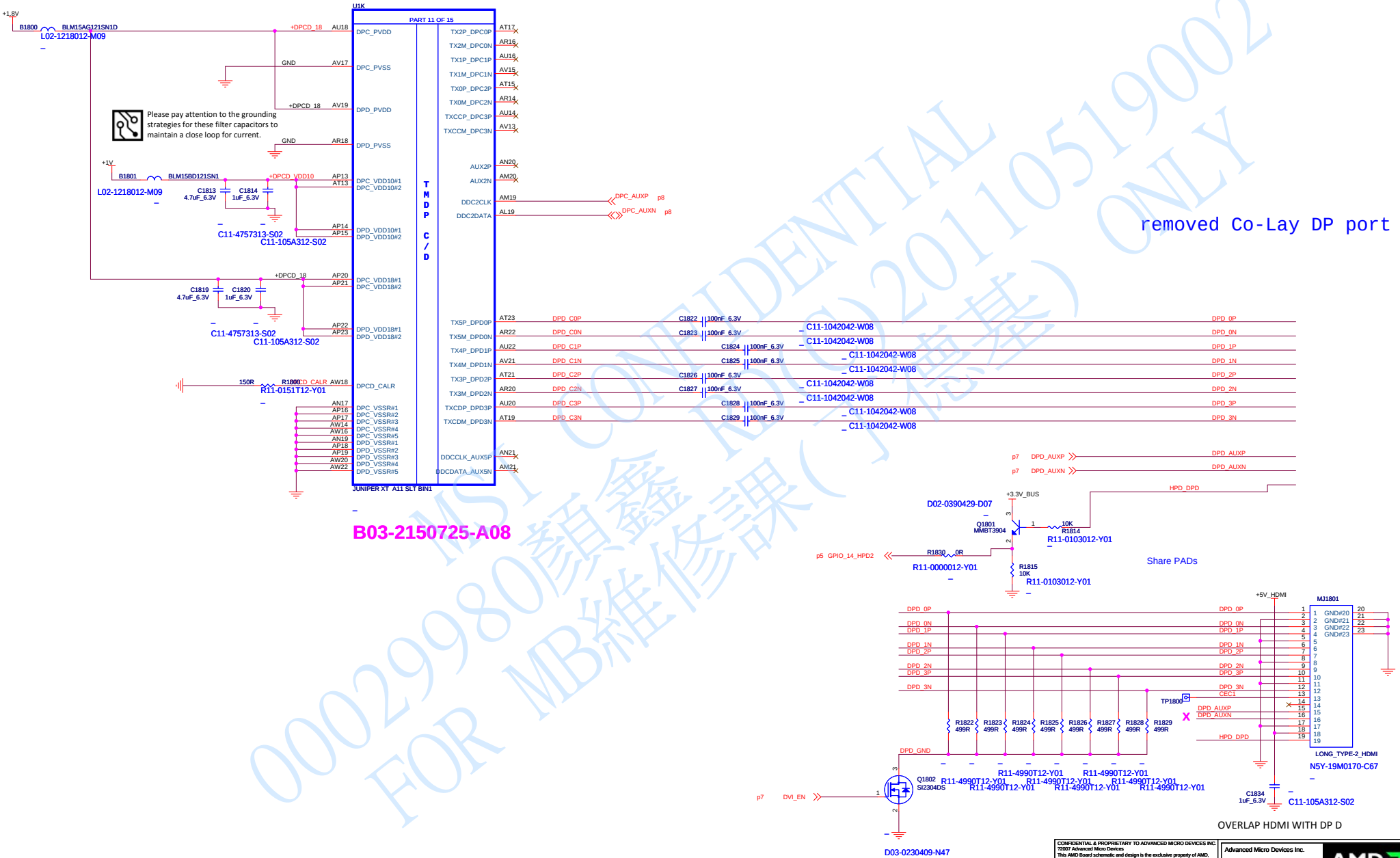
(09) M2 Display Port C & Display Port/HDMI D



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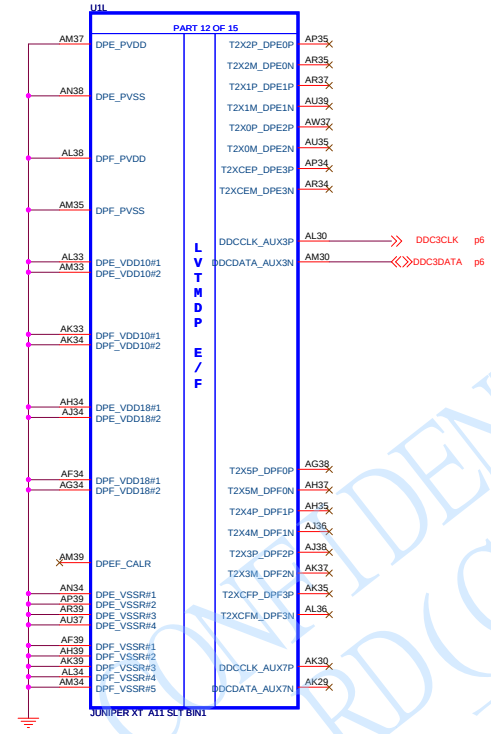
(10) M2 LVTMDP E&F



B03-2150725-A08

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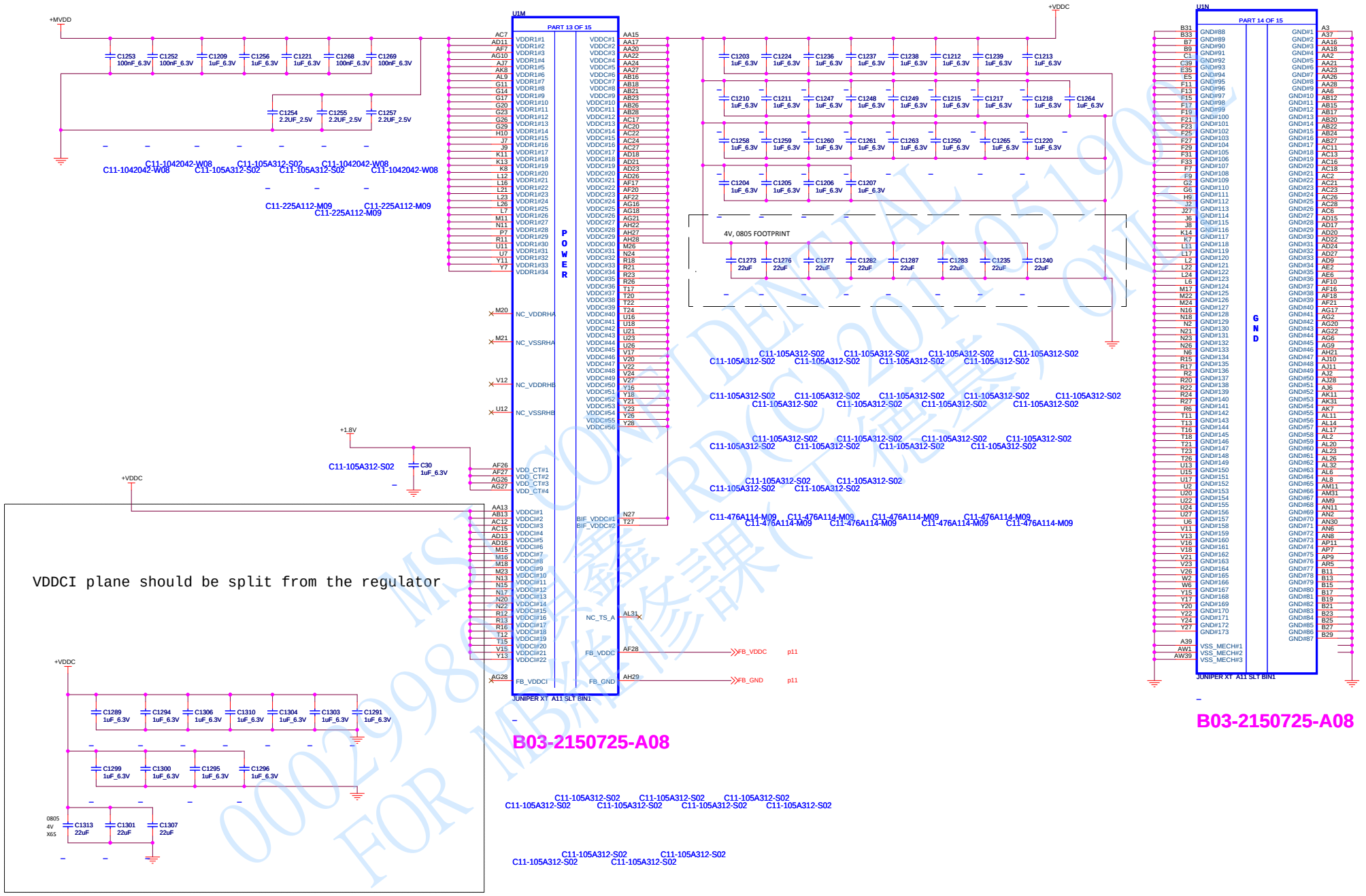
(11) M2 Power & GND



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(11) VDDC

PHASE 1

PHASE 2

PHASE 3

Table 1 MODE Pin Definition Table

VPM Mode	Mode Pin Status	Mode Pin Voltage (V)	Phase Operation		
			Phase 1	Phase 2	Phase 3
3-Phase Mode	0	0	Enabled	Enabled	Enabled
2-Phase Mode	1	3.3	Enabled	Enabled	Disabled
1-Phase Mode	Floating	~ 1.7	Enabled	Disabled	Disabled

Circuitry that have to be placed close to the device:
- current sense,
- compensation network,
- thermal compensation network (Droop, OCP, etc)

Output MLCC

Output Bulk CAPs

UP

SM

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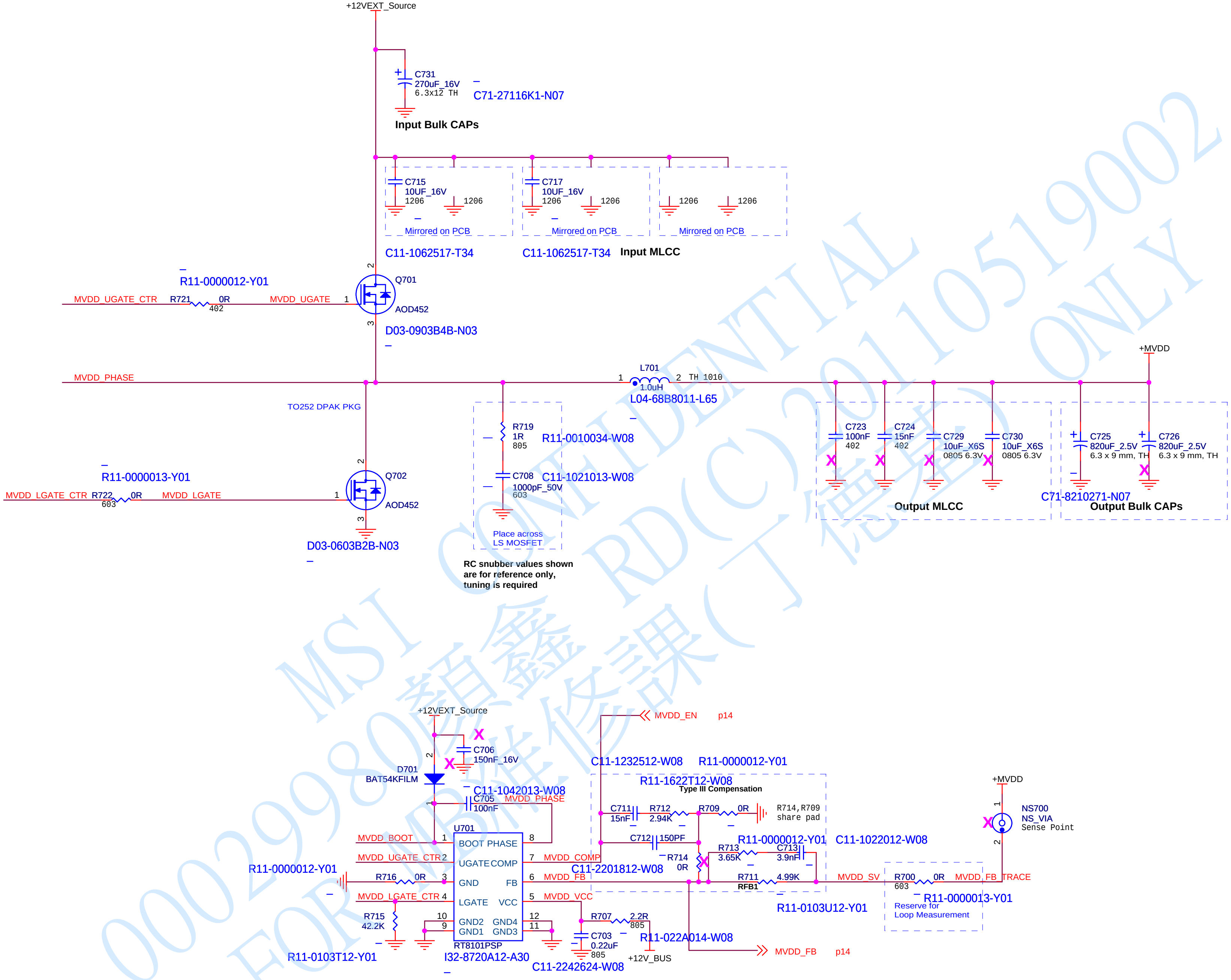

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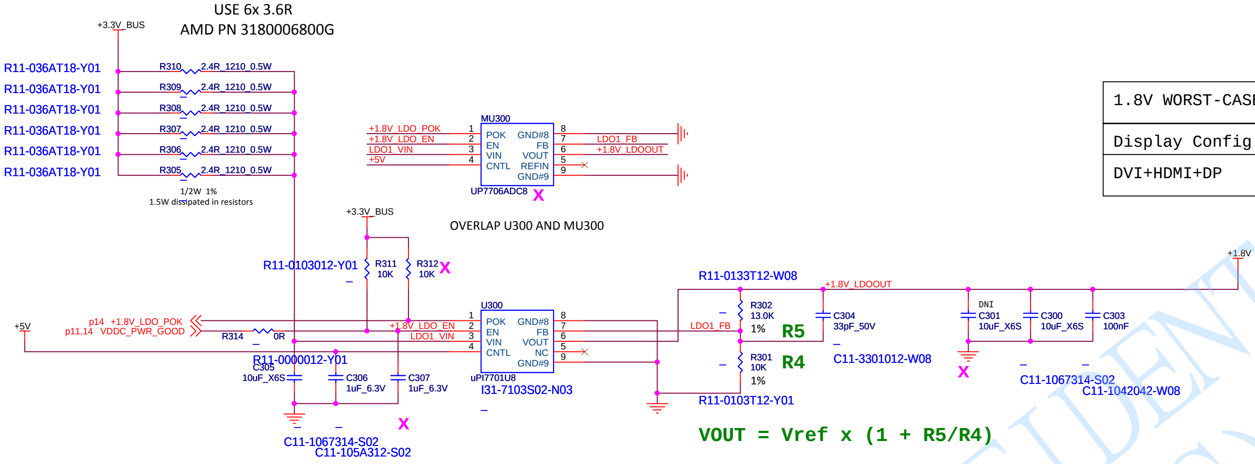
(15) Linear Regulators

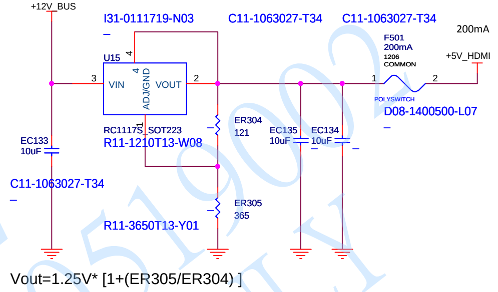
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

Regulators for +5V, +5V_VESA and +5V_HDMI



1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

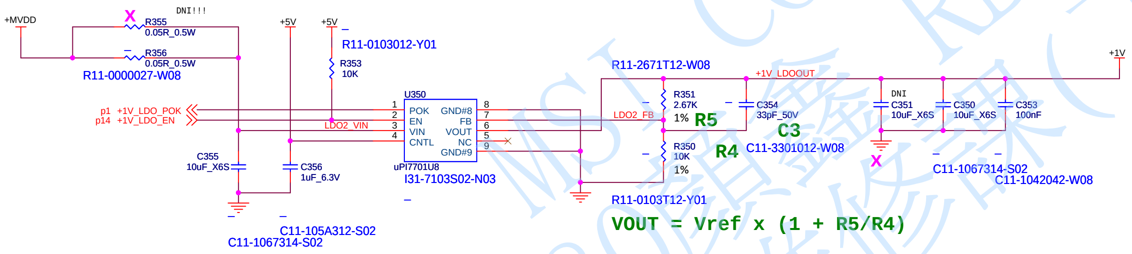


Change +5V REGULATOR to A1117
copy from MS-V208-5.0

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA



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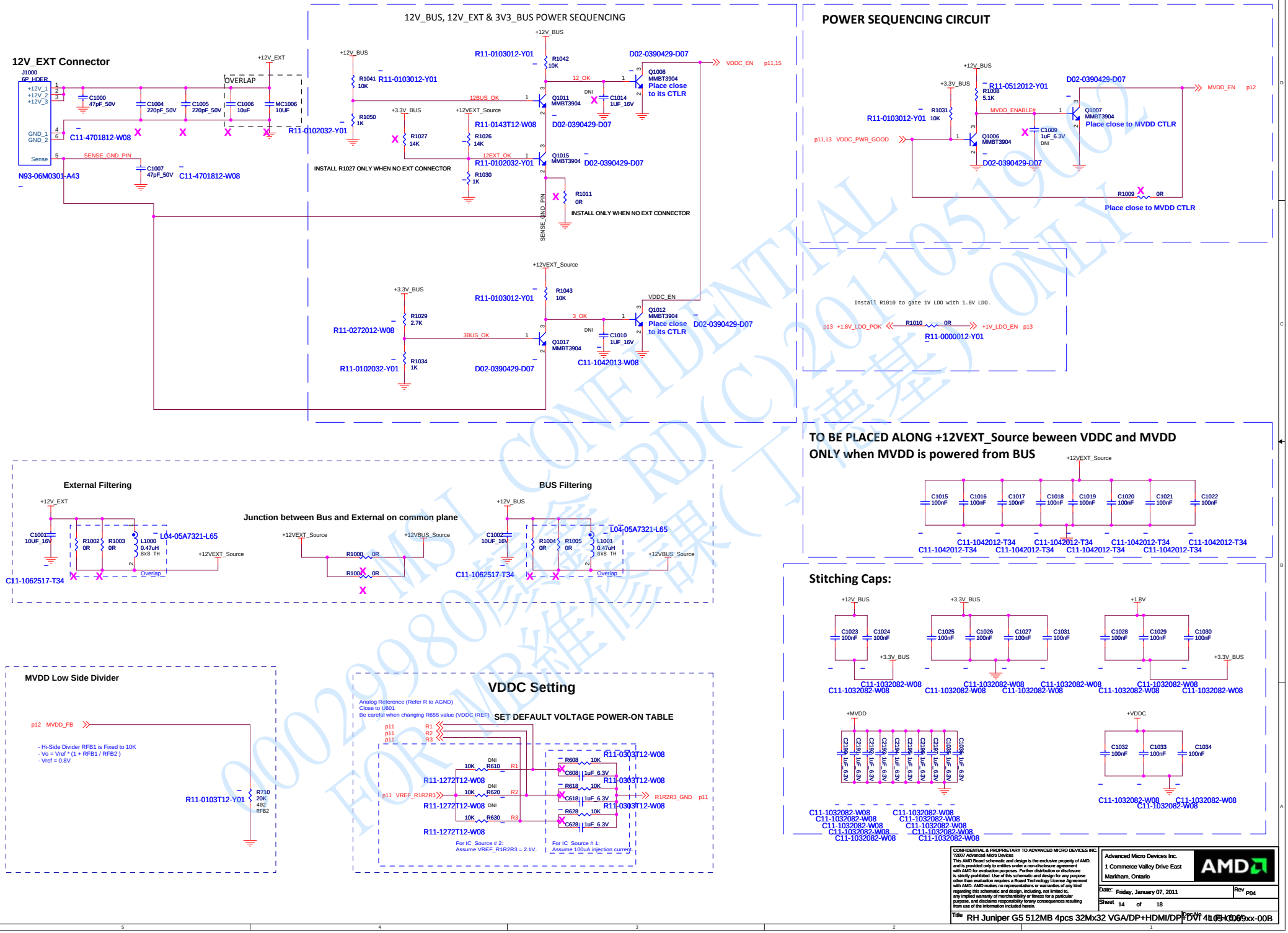
(16) Power Management - Power Gating and Dynamic Voltage Control



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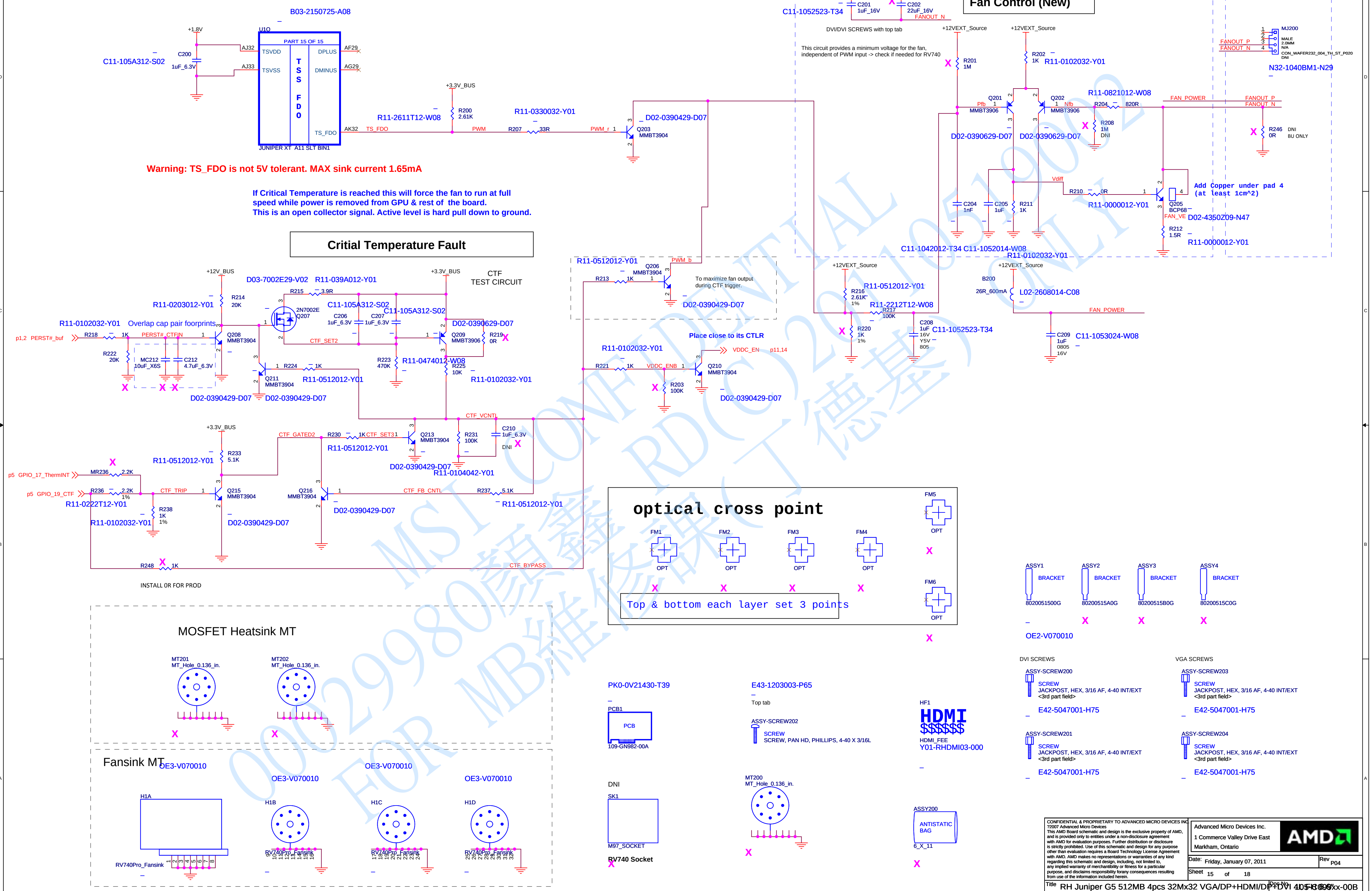
(19) Mechanical and Thermal Management



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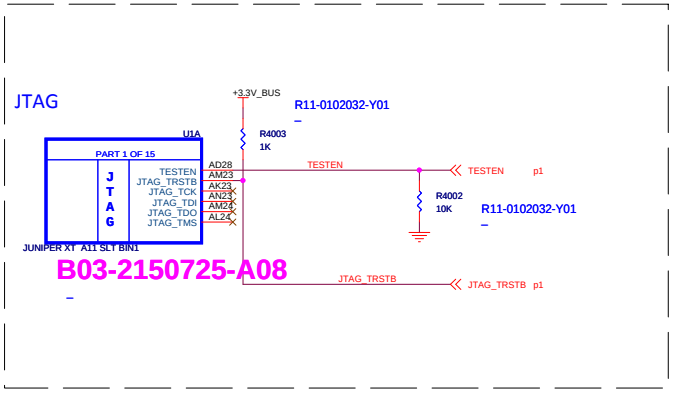
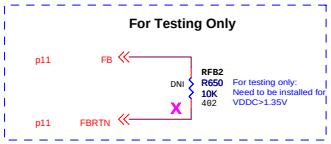
(19) Debug Circuits





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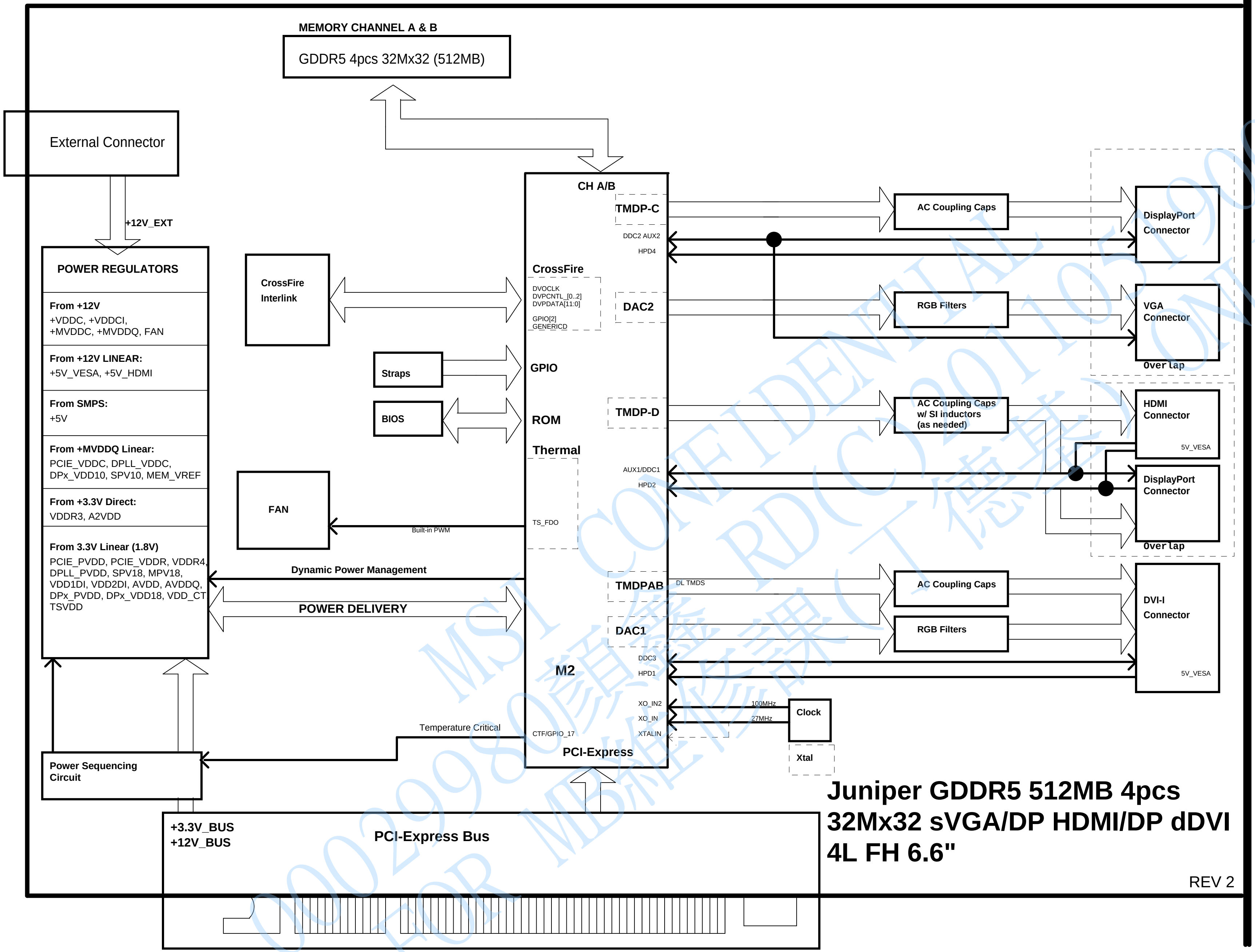

Juniper GDDR5 512MB 4pcs 32Mx32 sVGA/DP HDMI/DP dDVI 4L FH 6.6"

REV 2

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Title	Schematic No.	Date:
RH Juniper G5 512MB 4pcs 32Mx32 VGA/DP+HDMI/DP+DVI 4L FH 6.6"	105-C099xx-00B	Friday, January 07, 2011

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

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Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/12/12	RH Juniper G5 512MB 4pcs 32Mx32 VGA/DP+HDMI/DP+DVI 4L FH 6.6" sCF - based on B740 M2 4L
MS-V214	3.0	2011/01/04	01. PAGE 05 removed U2 & relation for DP DNI 02. PAGE 06 stuff DAC2 03. PAGE 07 delete DUAL ANALOG SWITCH (U1802) 04. PAGE 08 delete Co-Lay DP port 05. PAGE 11 changed to Power Stage MOSFET 06. PAGE 11 removed Low-Side gate damping resistor 07. PAGE 11 removed co-lay choke & changed choke footprint 08. PAGE 11 changed 12V input CAP & removed partial 12V input MLCC 09. PAGE 11 changed Output CAP 10. PAGE 12 changed PWM IC to ANPEC/APW8720AKAE-TRG 11. PAGE 12 changed choke footprint 12. PAGE 12 stuff snuber 13. PAGE 12 changed MOFET to NIKO 0903 vs 0603 14. PAGE 12 changed 12V input CAP & removed partial 12V input MLCC 15. PAGE 12 changed Output CAP 16. PAGE 12 add R716 17. PAGE 13 changed LDO to I31-7103S02-N03 18. PAGE 13 combine +5V_HDMI & +5V_VESA use A1117 reg. 19. PAGE 14 change 12V input filter choke 20. PAGE 15 change FAN housing to 4pin 21. PAGE 15 add optical cross point & HDMI Fee symbol
			.....