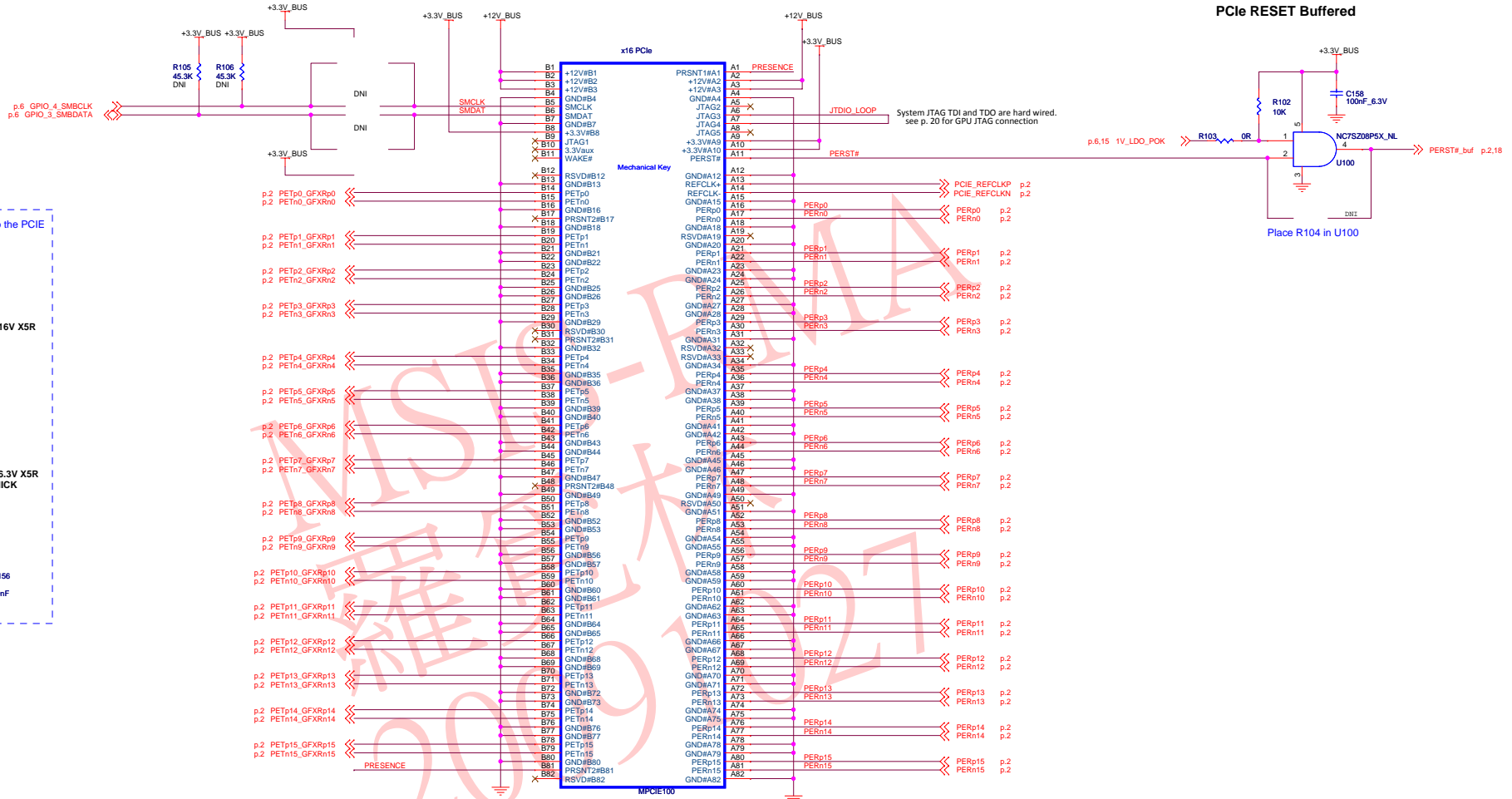


# PCI-EXPRESS EDGE CONNECTOR

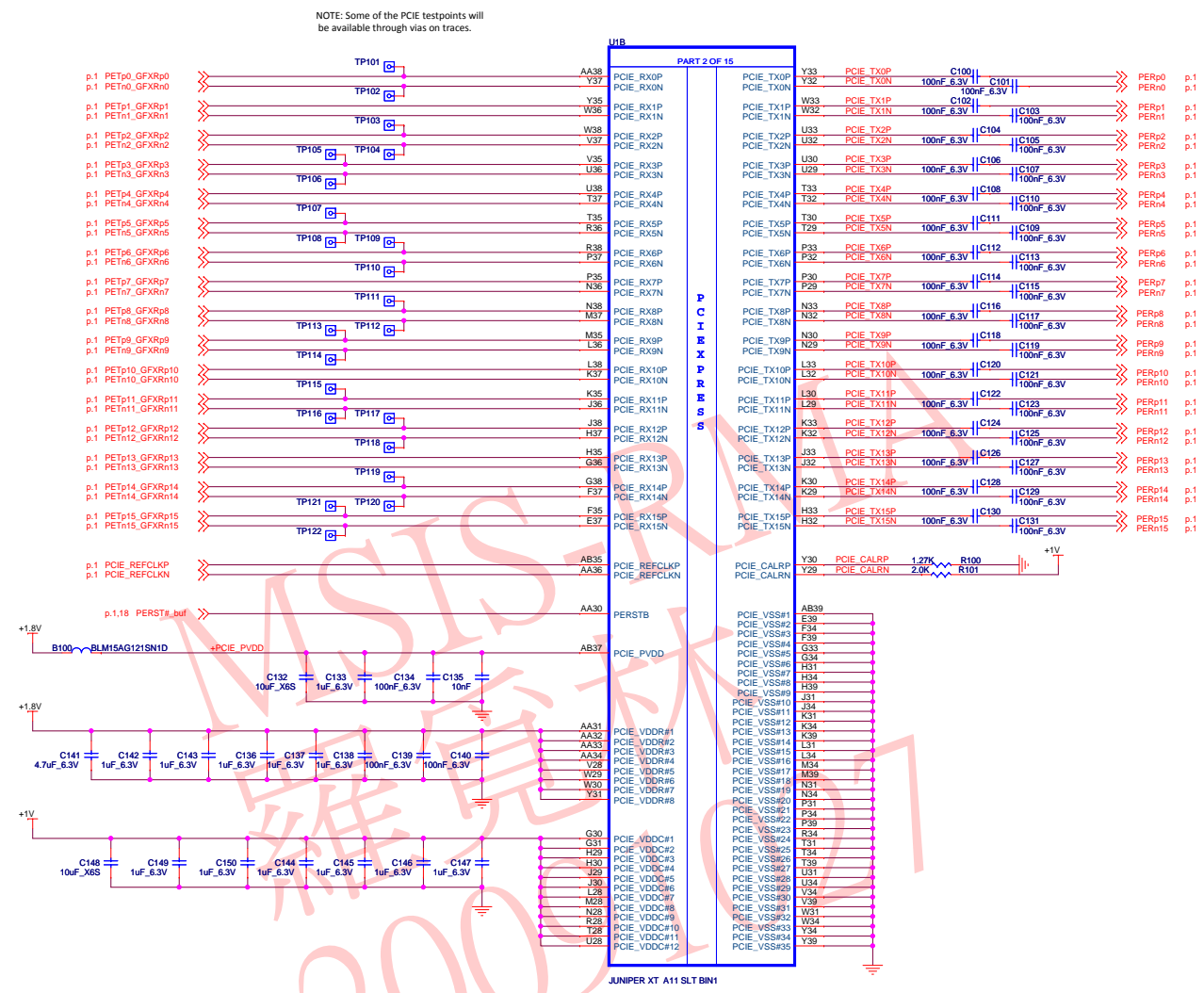


Place these caps as close to the PCIe connector as possible

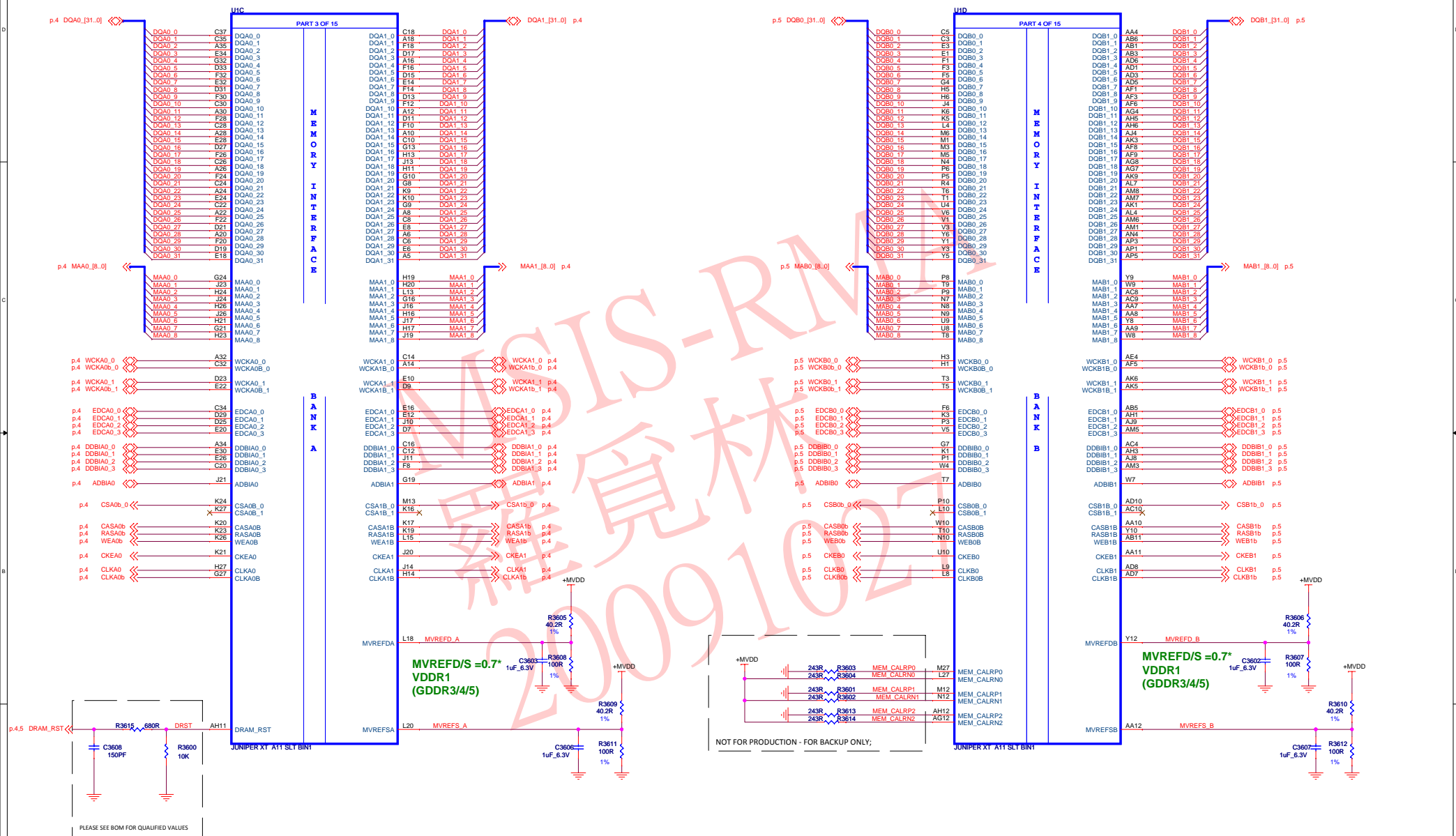
Place R104 in U100

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
	BRING UP ONLY

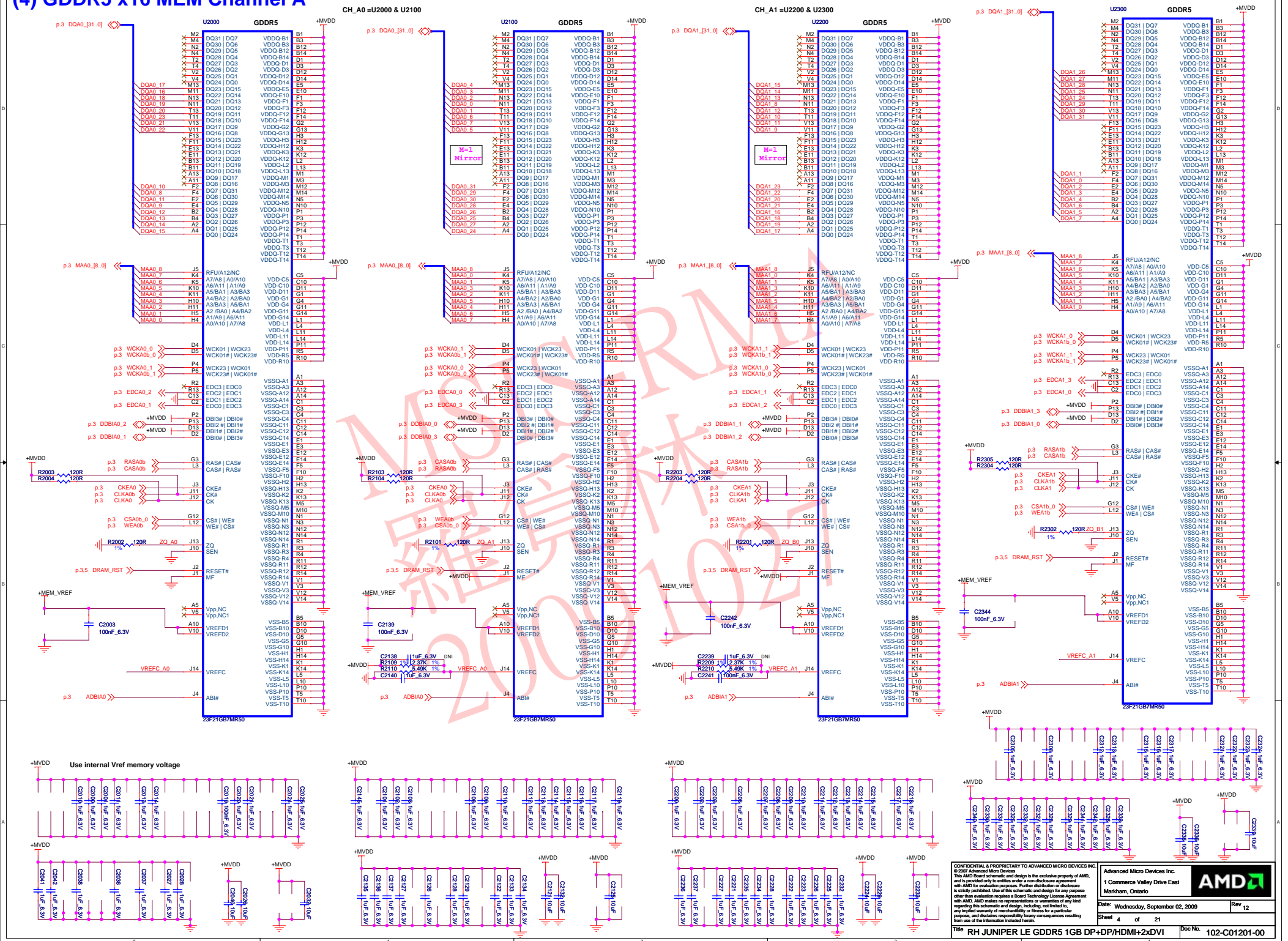
(2) JUNIPER PCIe Interface

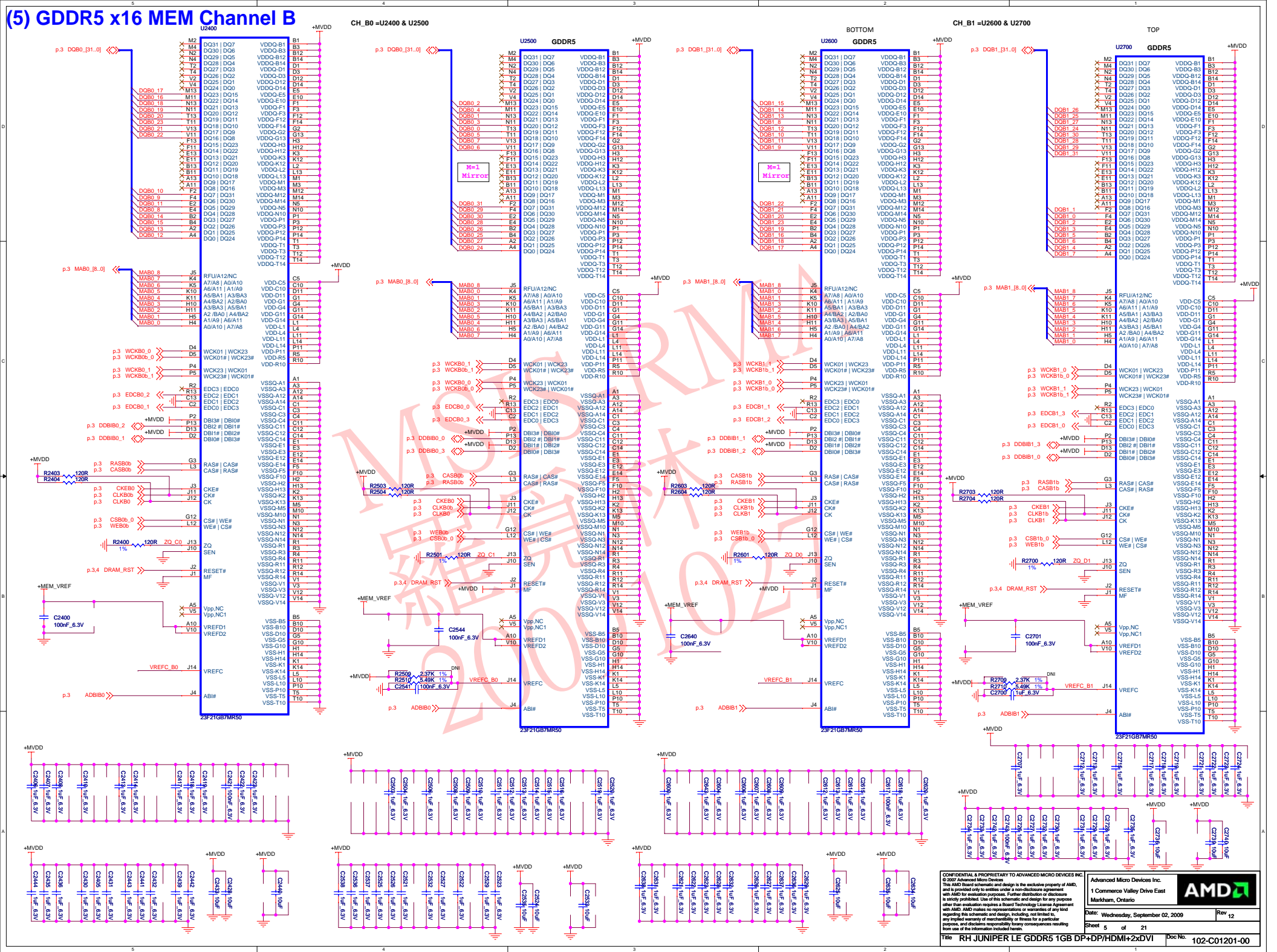


### (3) JUNIPER MEM Interface Ch A&B



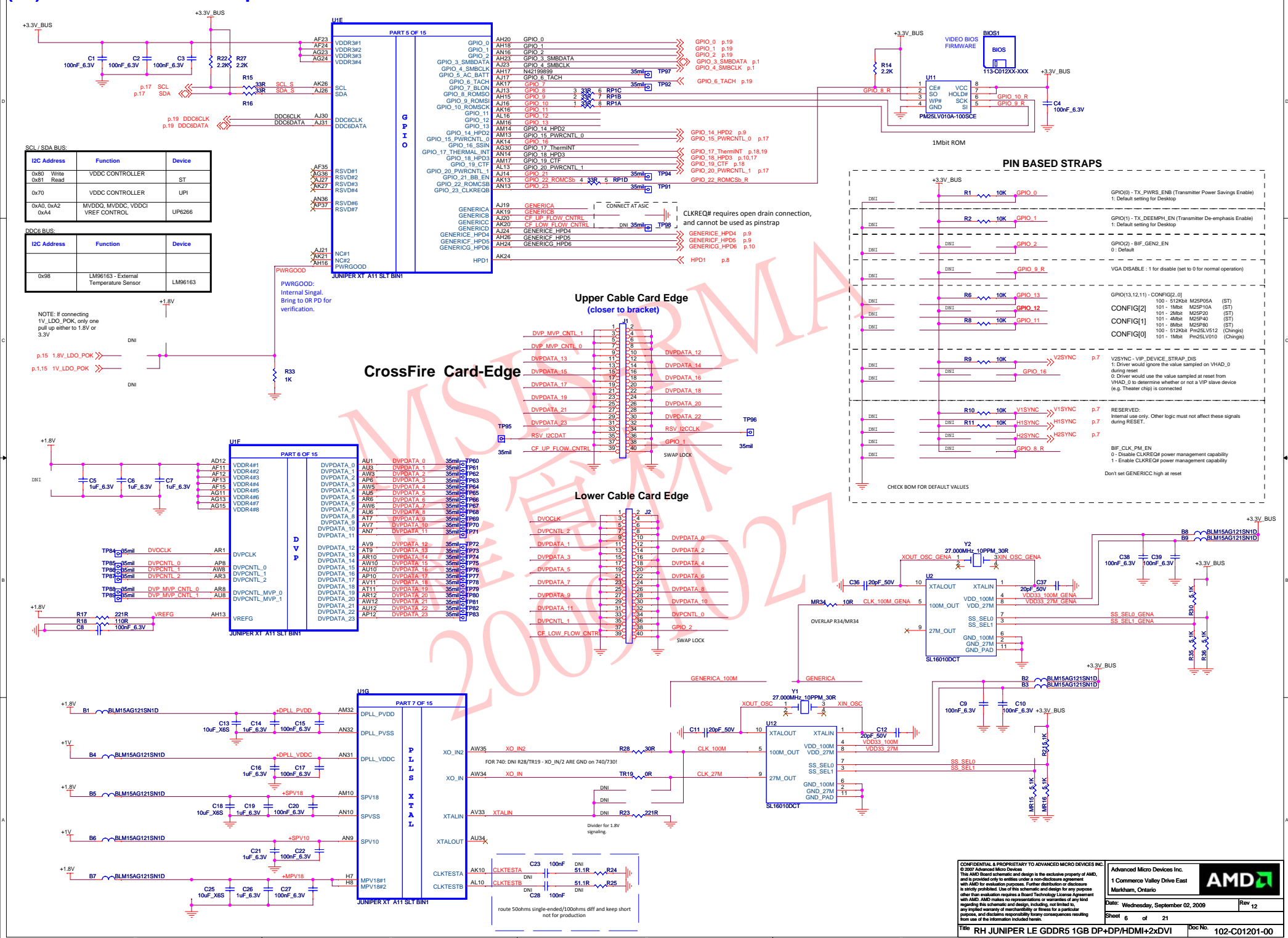
**(4) GDDR5 x16 MEM Channel A**



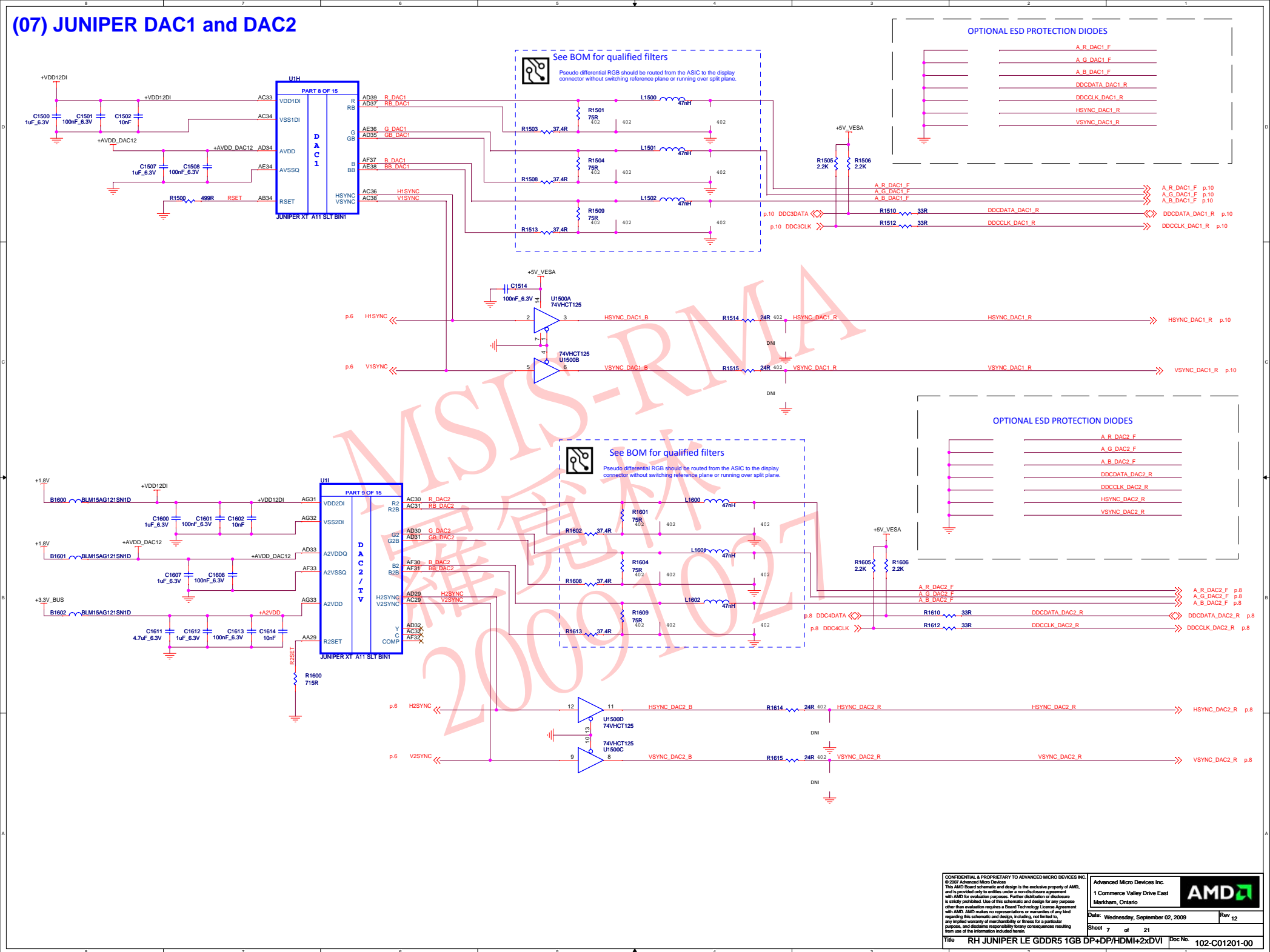




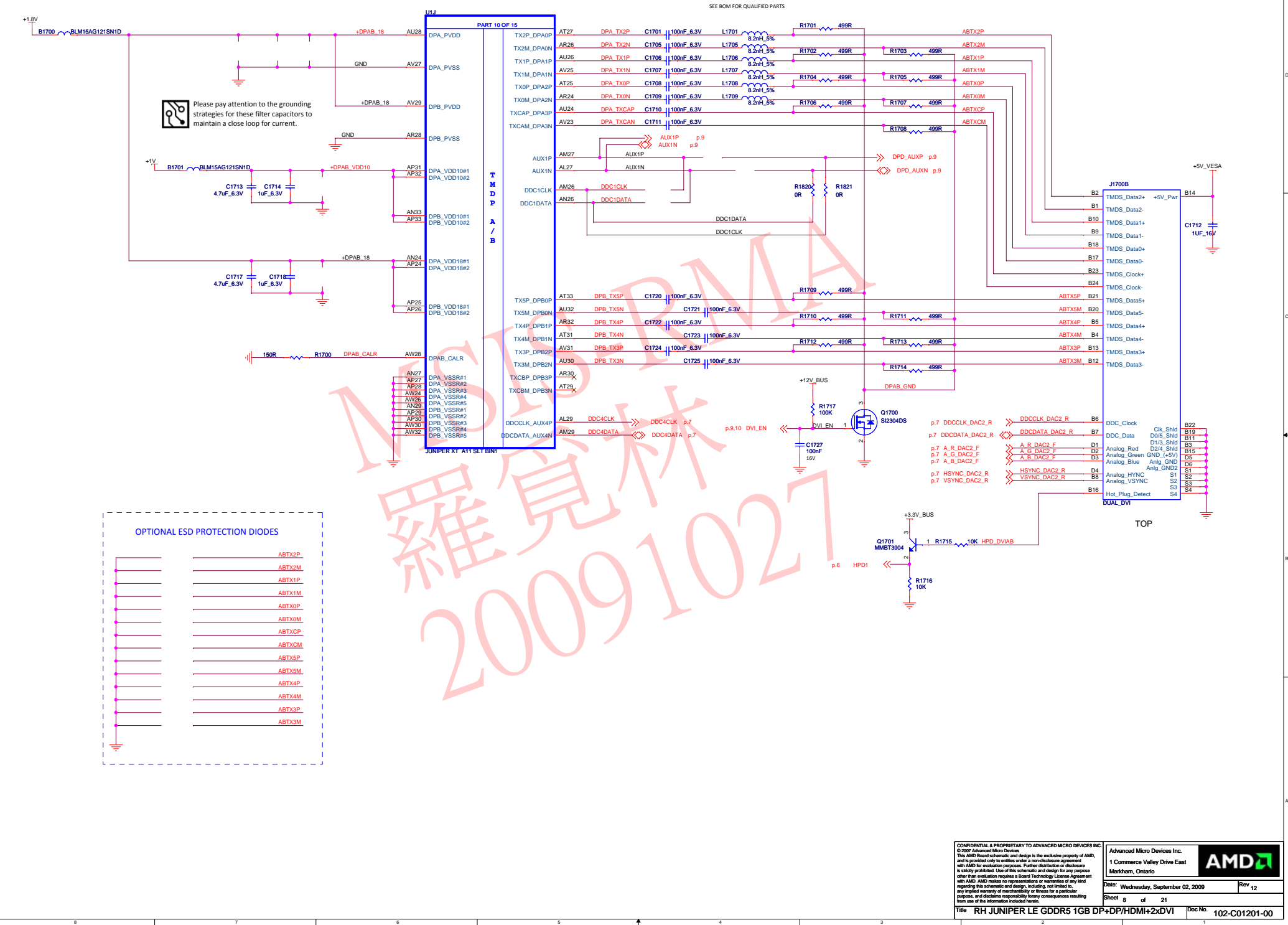
# (06) JUNIPER GPIOs Strap CF XTAL OSC



## (07) JUNIPER DAC1 and DAC2

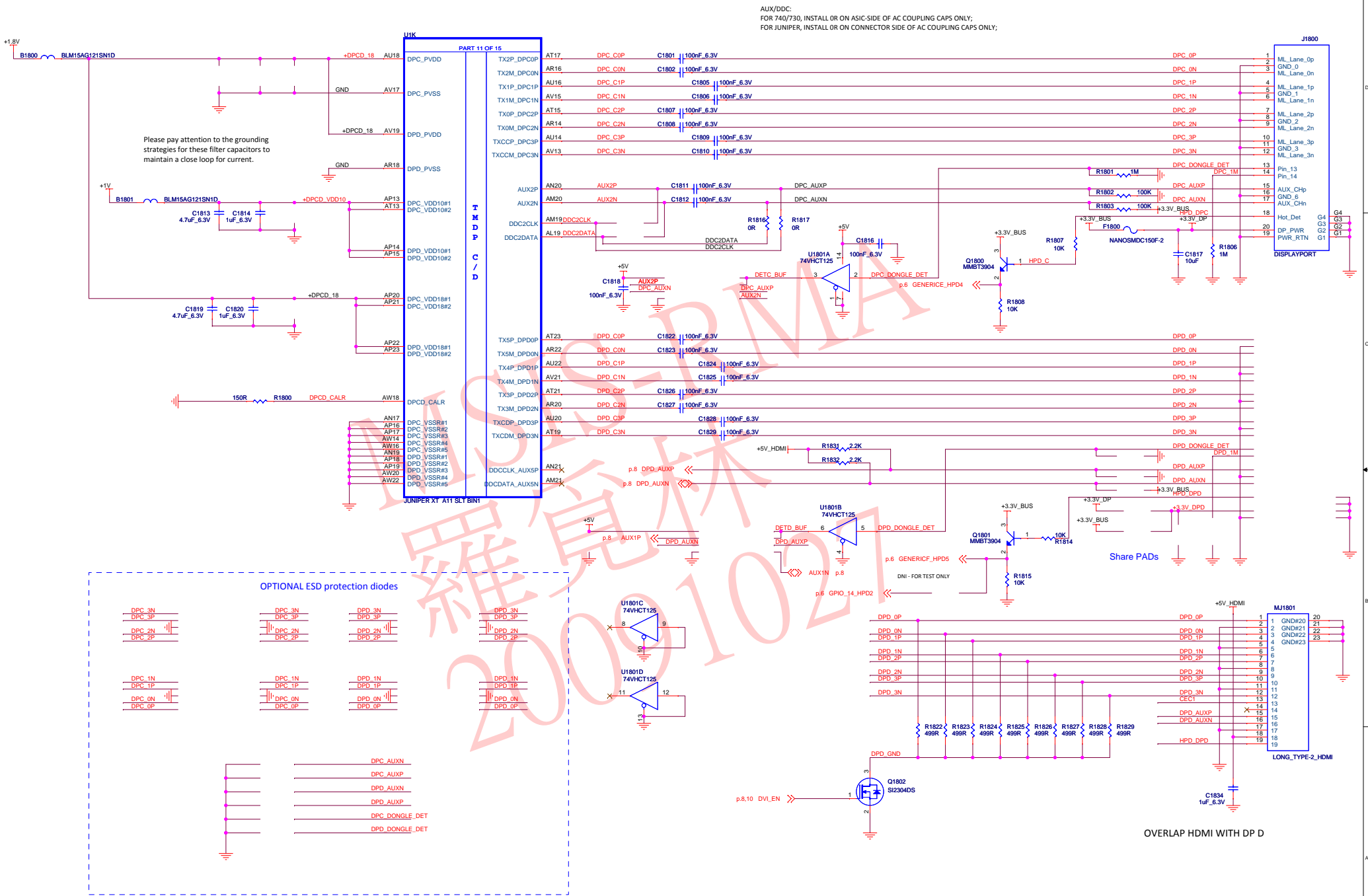



(08) JUNIPER TMDP A&B dDVI-I TOP



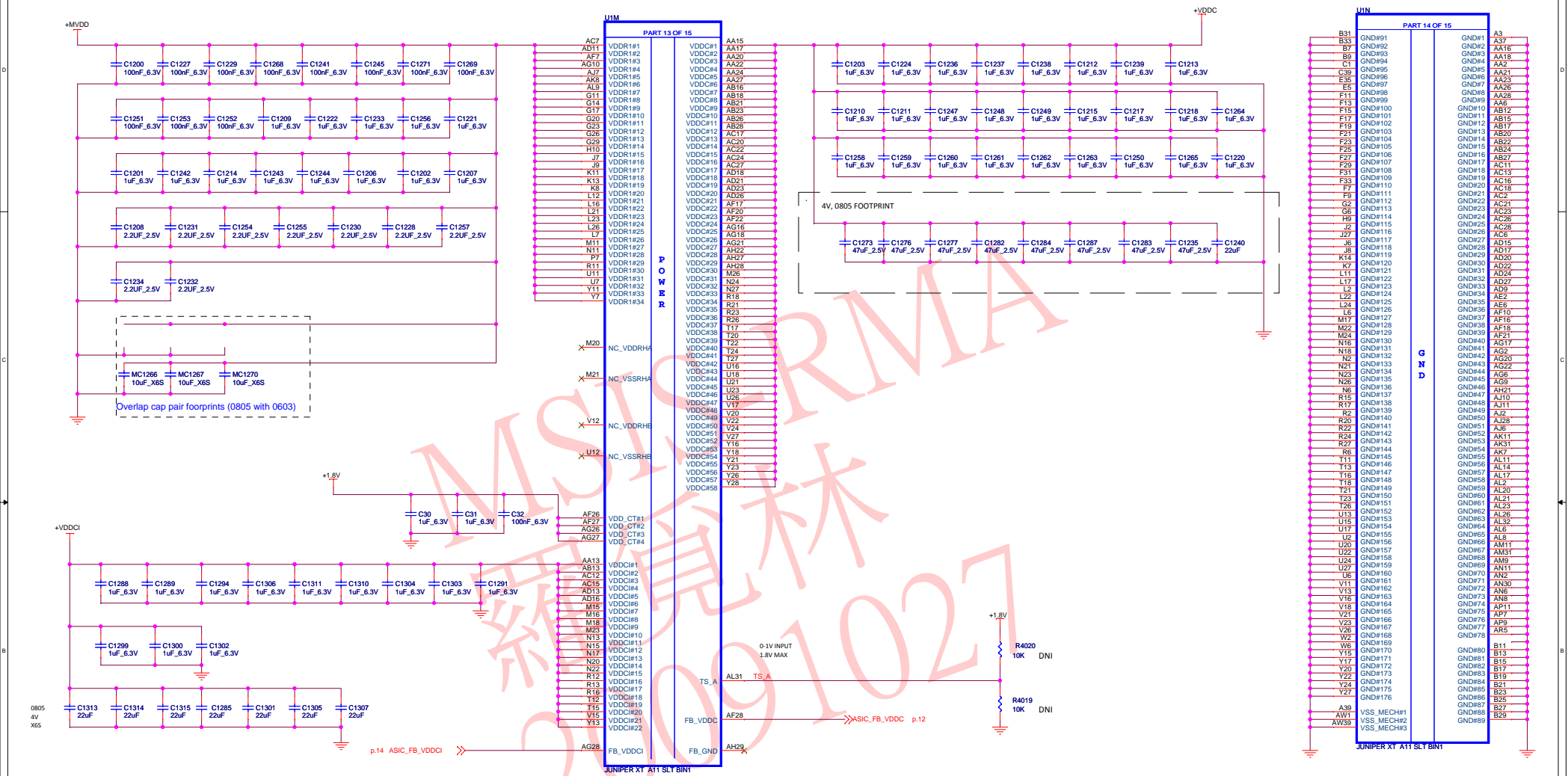


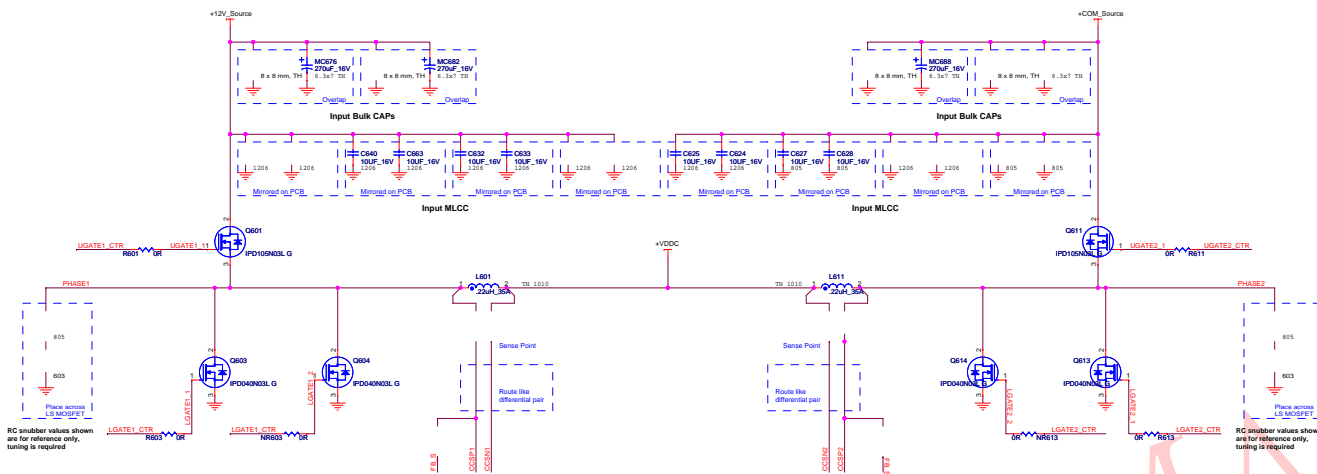
(09) JUNIPER Display Port C & Display Port/HDMI D



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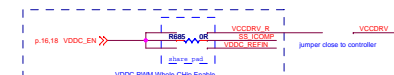
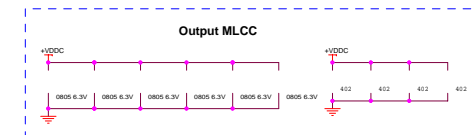
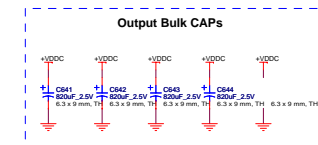
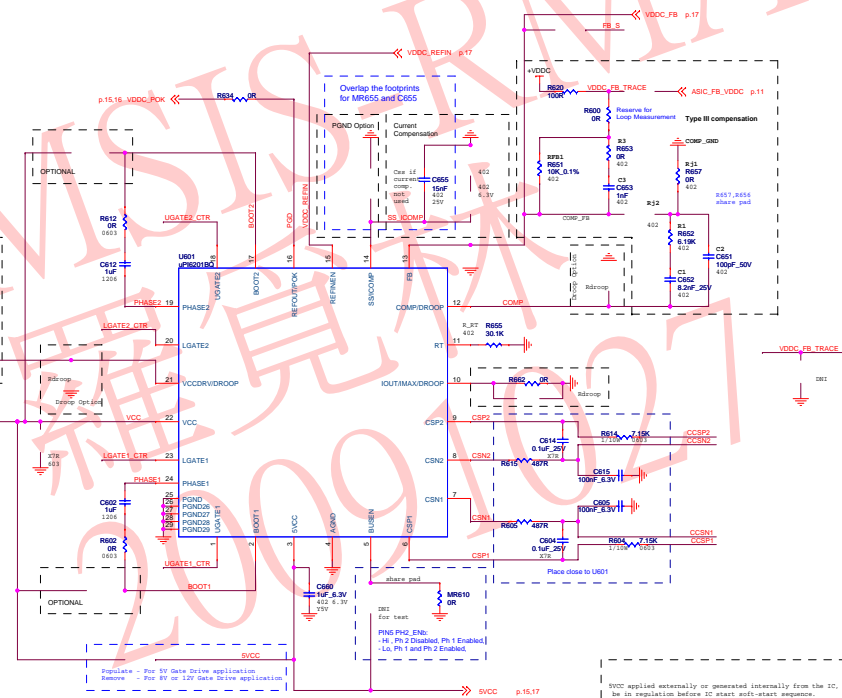
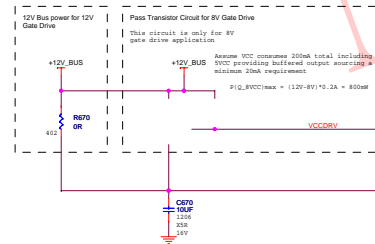
## (11) JUNIPER Power & GND





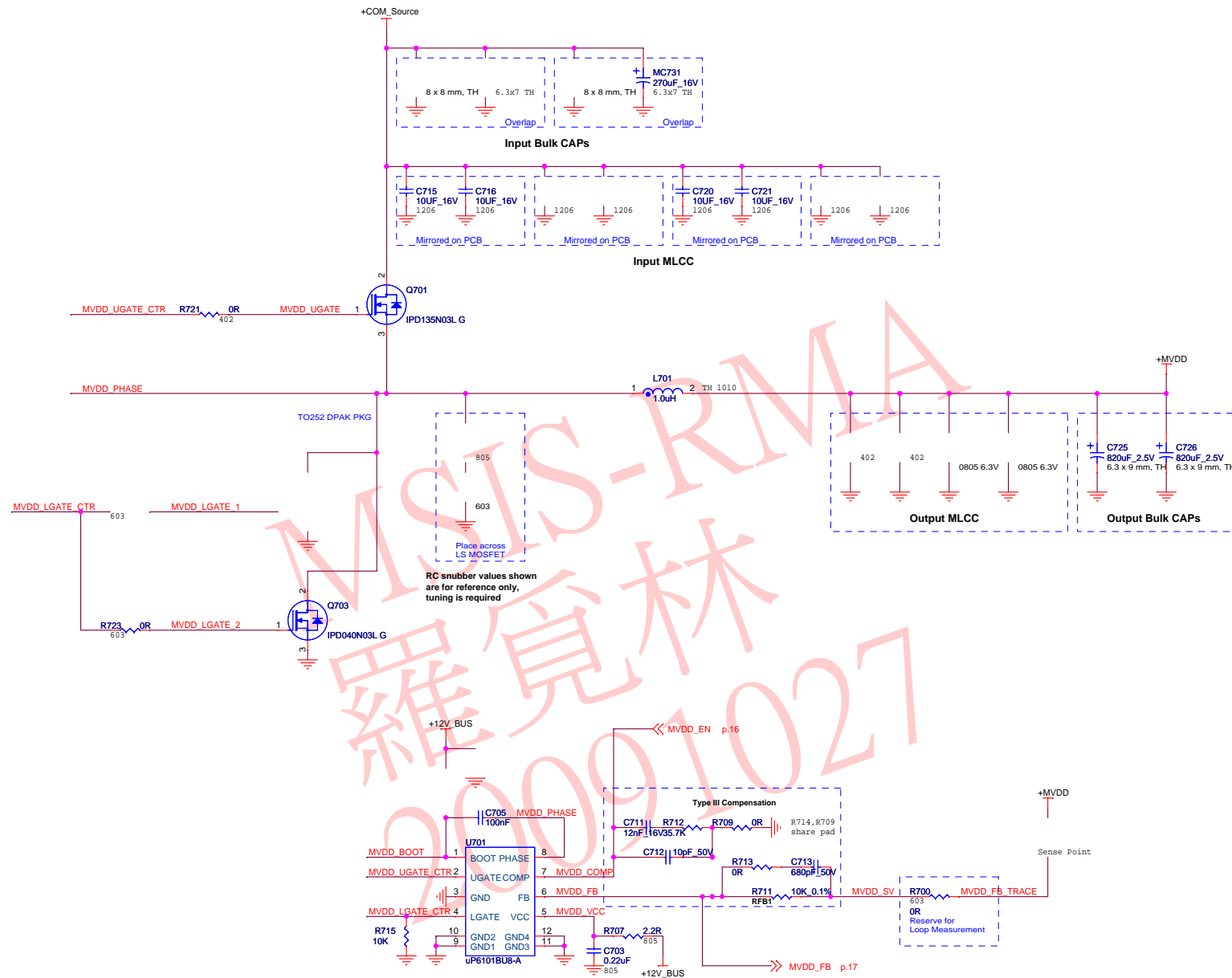
Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R641, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R641, Q661



VDDC applied externally or generated internally from the IC, must be in regulation before IC start soft-start sequence.

1. For 8V Gate Drive application: External filtered +5V\_EXT is applied to this pin.
2. For 8V or 12V Gate Drive application: +5VDC is generated internally and this is an output with 20mA maximum current capability.



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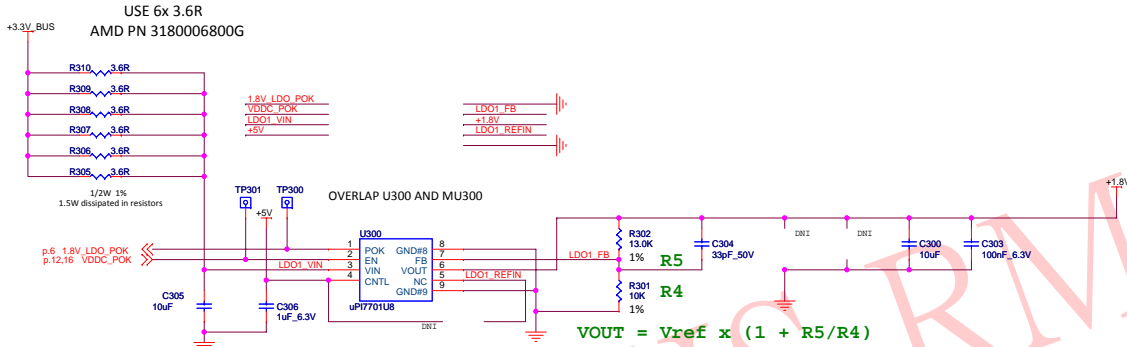
Title RH JUNIPER LE GDDR5 1GB DP+DP/HDMI+2xDVI Doc No. 102-C01201-00



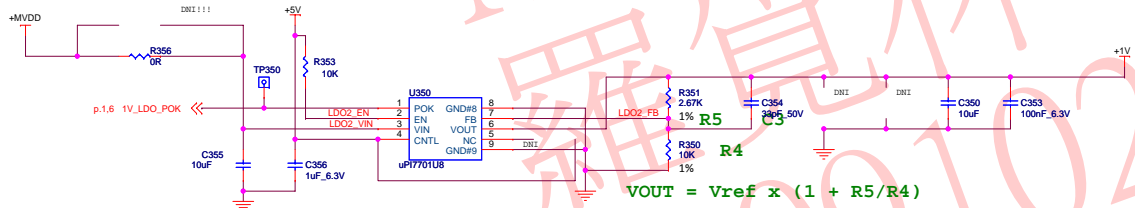


(15) Linear Regulators

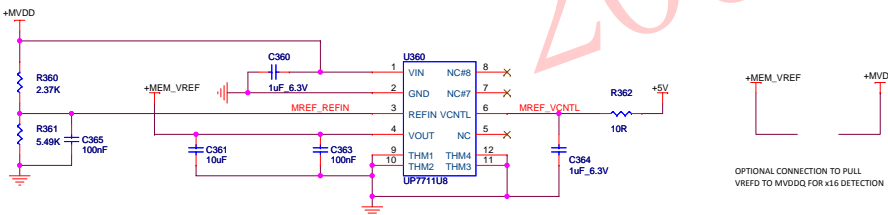
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling



LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling

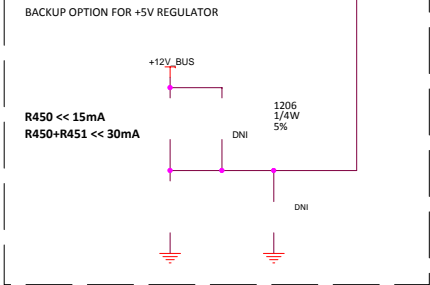
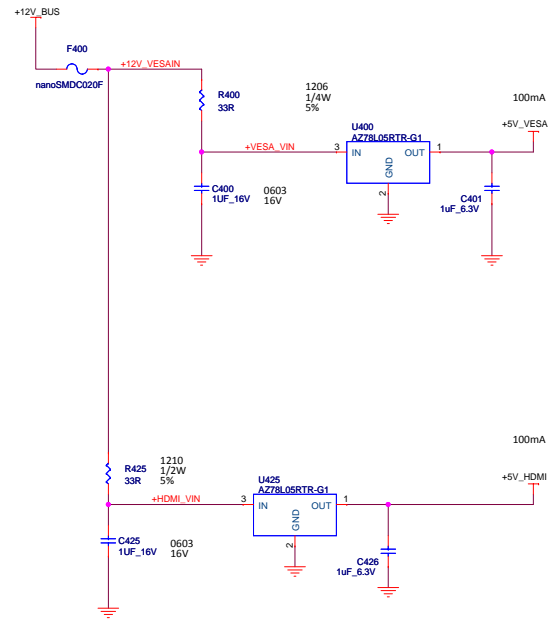


Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ

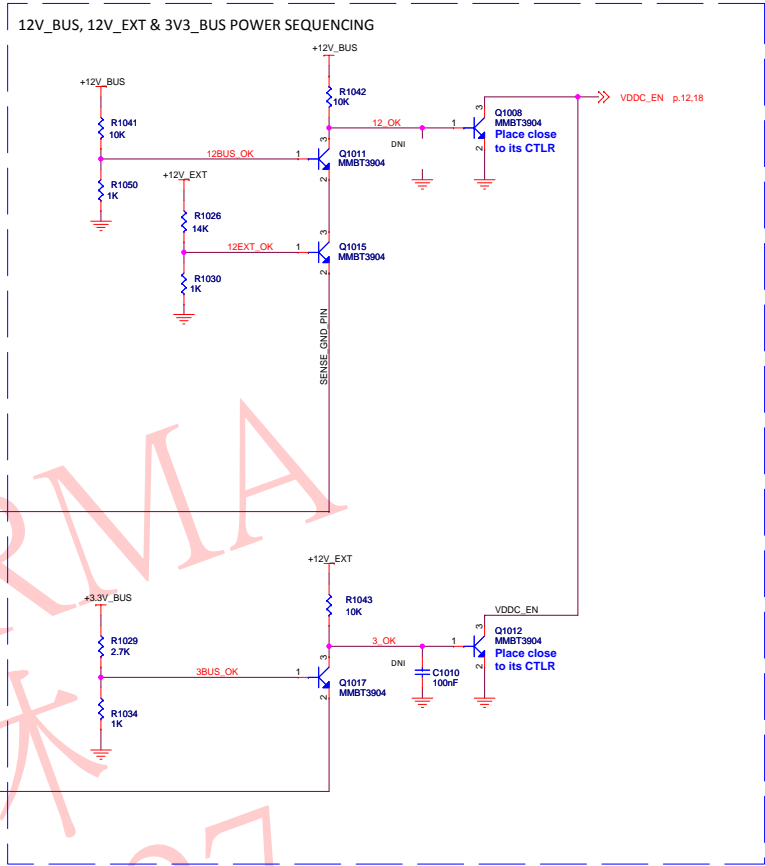
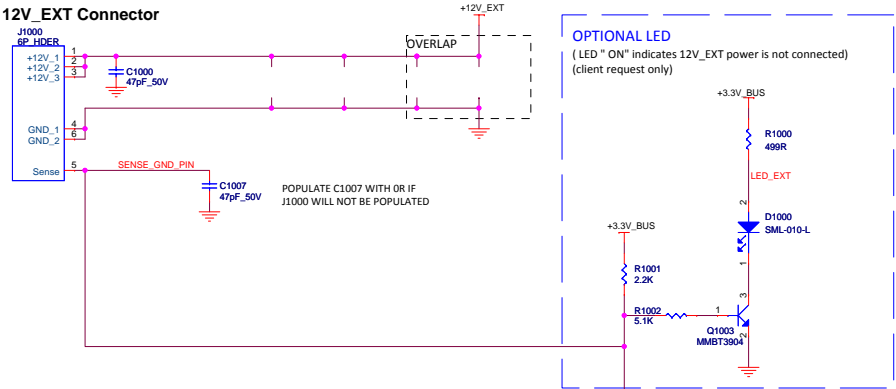


There must be one 100nF at each VREF pin  
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices

Regulators for +5V, +5V\_VESA and +5V\_HDMI

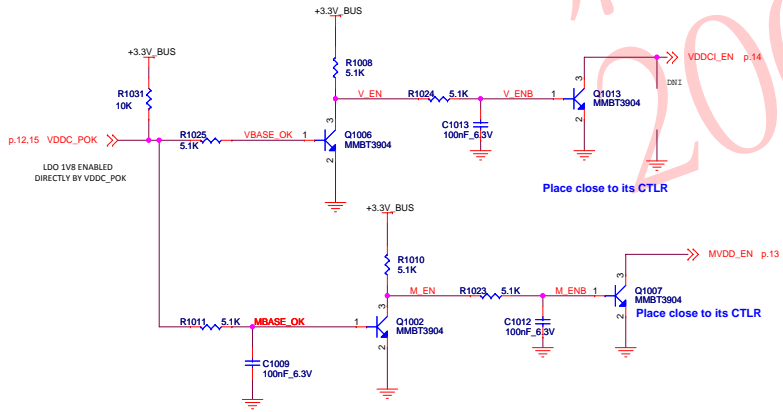


(16) Power Management - Power Gating and External Power Detect



**POWER SEQUENCING CIRCUIT**

FOR MVDD & VDDCI  
(ENABLES CANNOT BE SHARED SINCE IT IS ALSO THE COMPENSATION PIN OF THE SMPS REGULATOR)



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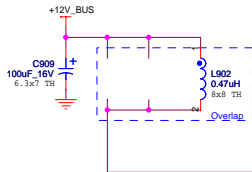
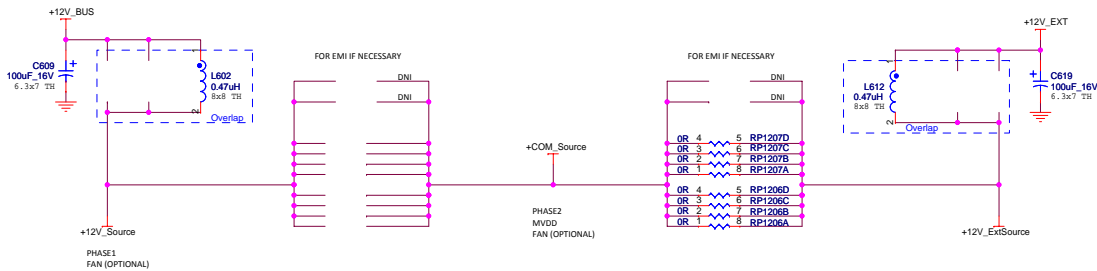
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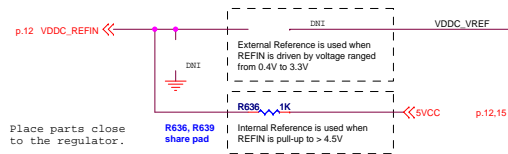
(18) Power Management 2



IZC VOLTAGE REFERENCE FOR VDDC (not for production)



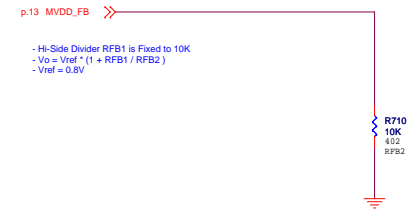
VDDC Reference Voltage Selection



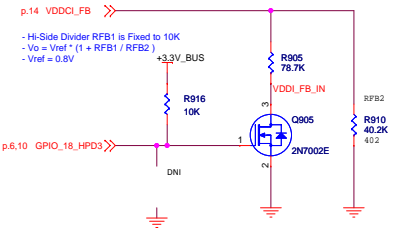
VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

MVDD Low Side Divider

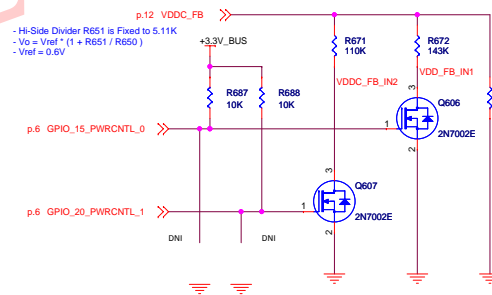


VDDCI Low Side Divider

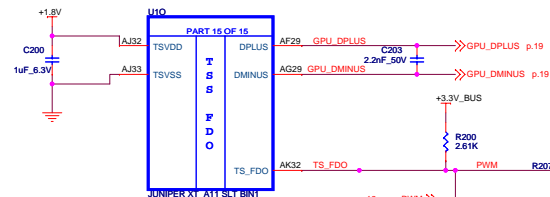


VDDC Low Side Divider

R650 must be populated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.

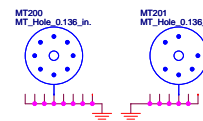
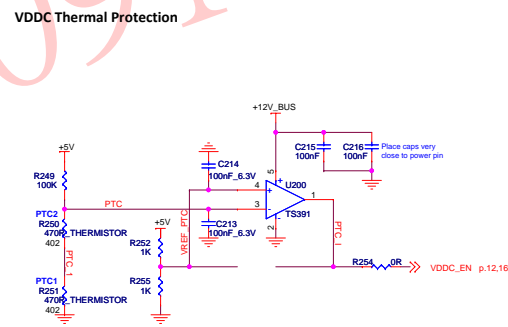
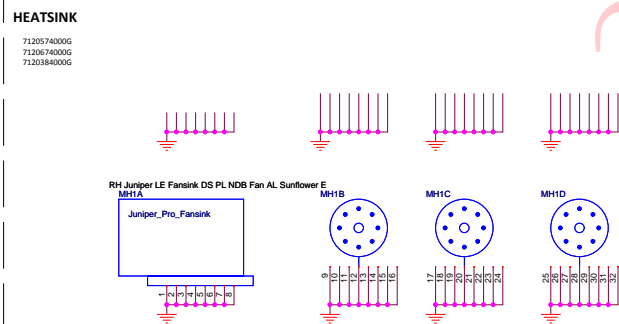
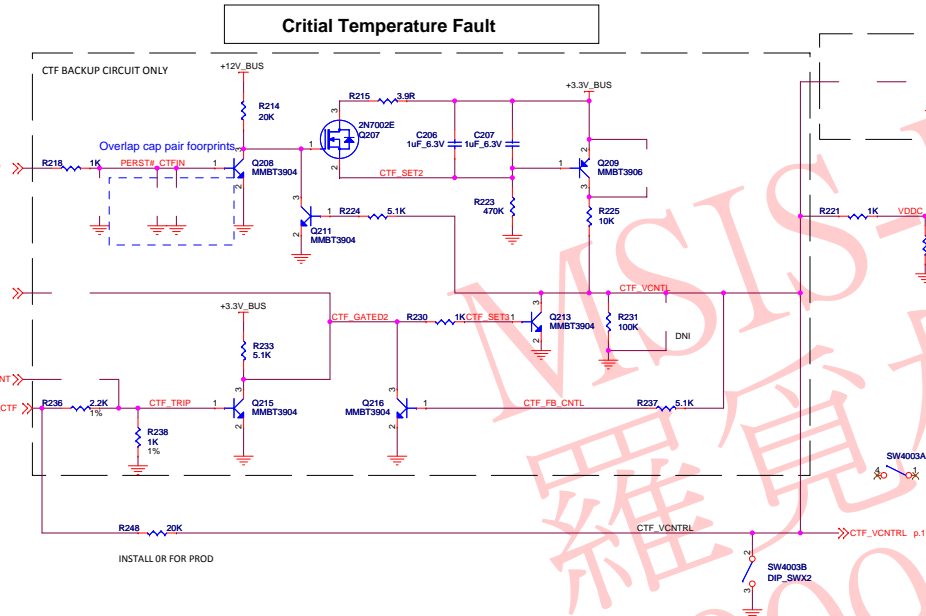
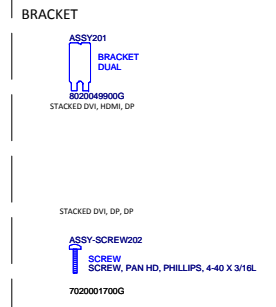
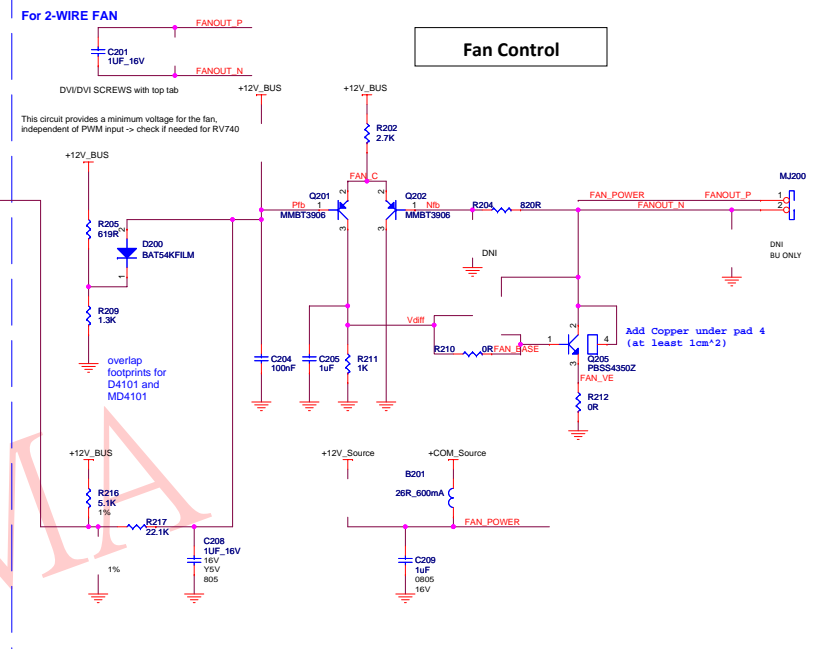



## (19) Mechanical and Thermal Management



**Warning: TS\_FDO is not 5V tolerant. MAX sink current 1.65mA**

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.

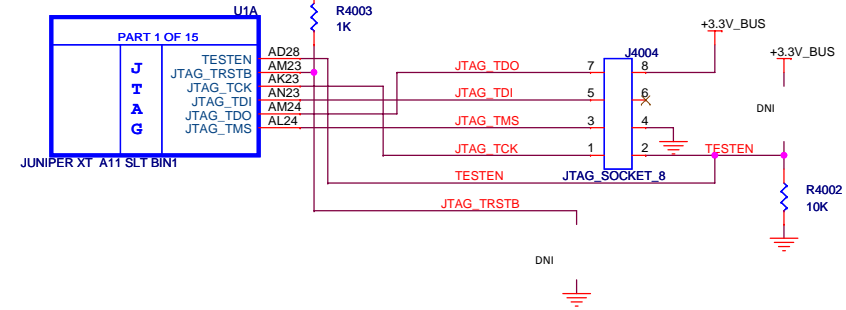


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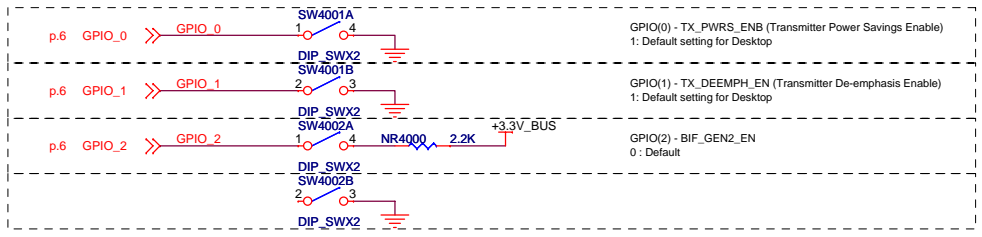


# (19) Debug Circuits

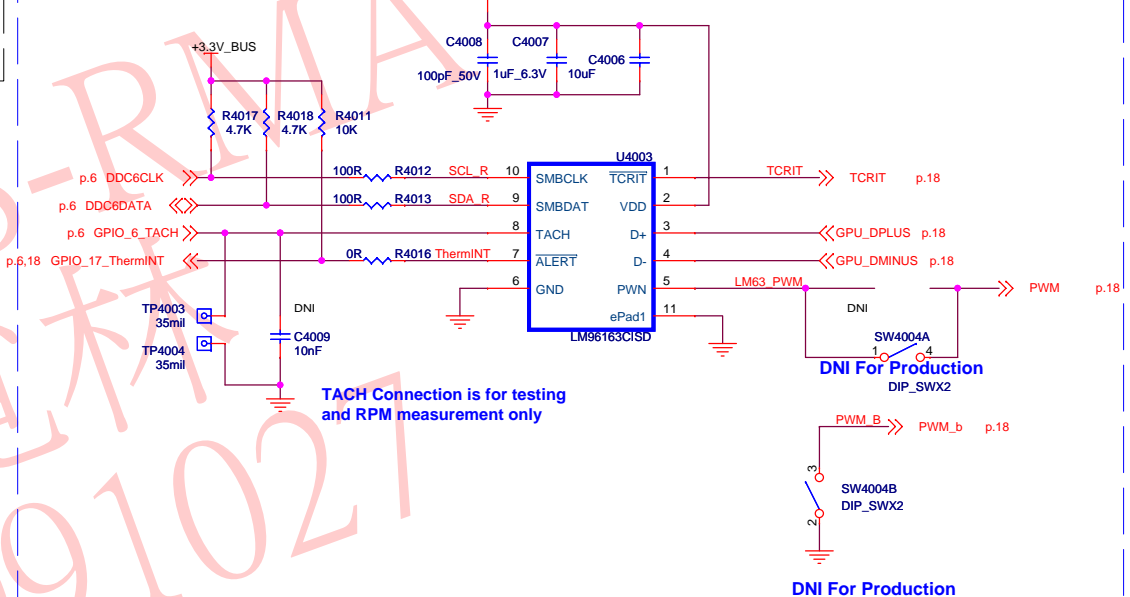
## JTAG



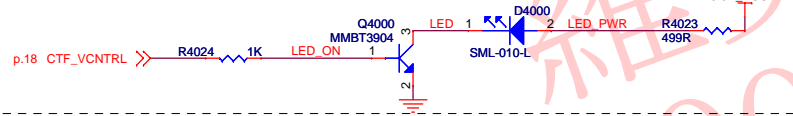
## SWITCH CONNECTIONS TO PINSTRAPS



## LM96163 FOR BACKUP THERMAL CONTROL



## LED RED "ON" shows Fault



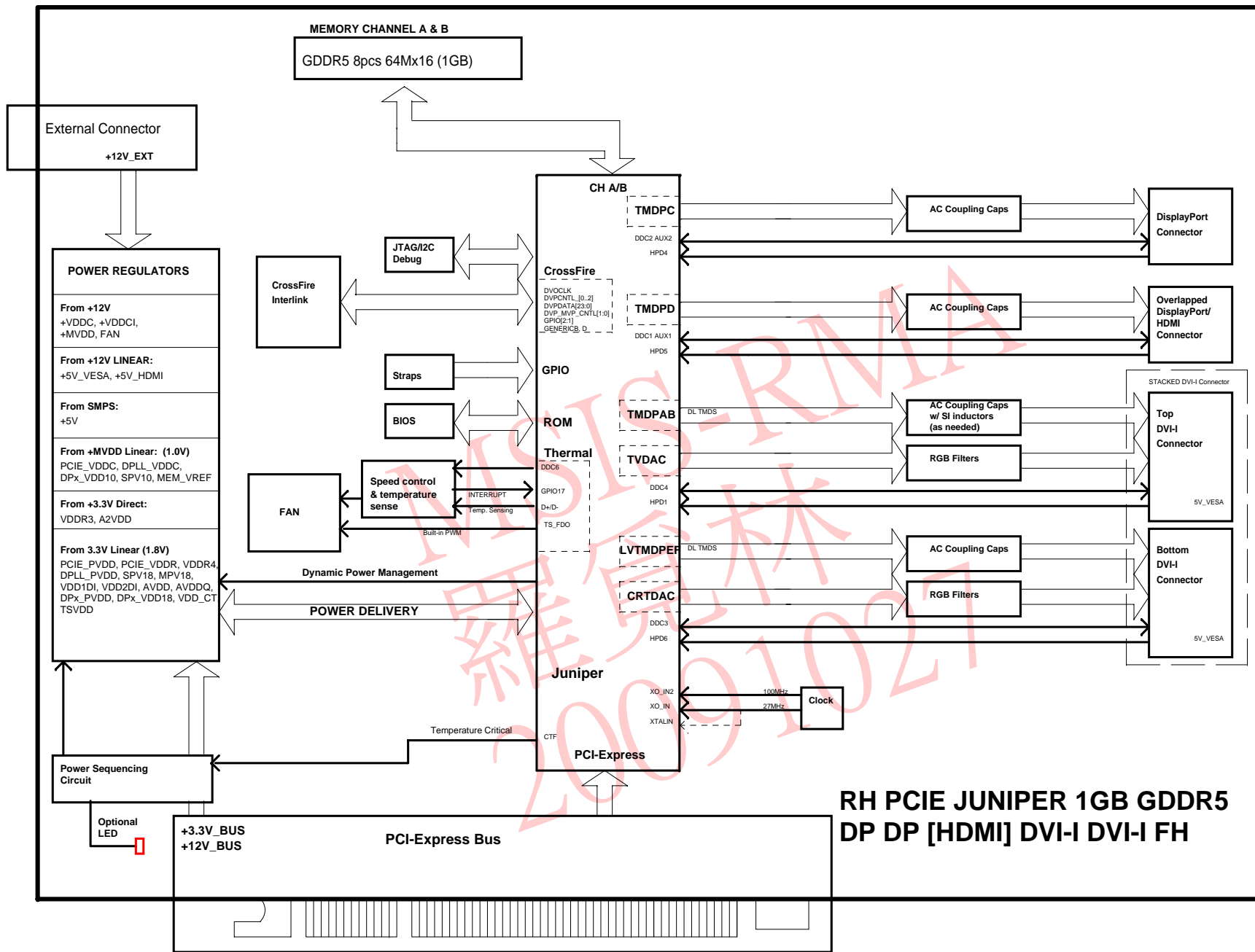
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**RH PCIE JUNIPER 1GB GDDR5**  
**DP DP [HDMI] DVI-I DVI-I FH**

<div>AMD</div>			Title		Schematic No.		Date:	
			RH JUNIPER LE GDDR5 1GB DP+DP/HDMI+2xDVI		102-C01201-00		Wednesday, September 02, 2009	
			REVISION HISTORY					NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION					
00	00A	2009/03/23	INITIAL -00A RELEASE					
01	00B	2009/07/13	INITIAL -00B RELEASE					
<div>MSIS-RMA</div> <div>羅覓林</div> <div>20091027</div>								
5		4		3		2		1