G94-P545-A01 - GDDR3, DVI/VGA + DVI/VGA + HDTV/SDTV-Out

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10545-base-100	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU9100	600-10545-9100-100	G94-400 650MHz/1000MHz 512MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out (Bring Up SKU)
2	SKU0000	600-10545-0000-100	G94-400 650MHz/1000MHz 512MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
3	SKU0010	600-10545-0010-100	G94-300 500MHz/800MHz 512MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
4	SKU0020	600-10545-0020-100	G94-200 500MHz/800MHz 384MB 16Mx32 BGA136 GDDR3, DVI-I-DL+DVI-I-DL+HDTV-Out
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V127-0A Base on P545

1.PAGE18: ADD Display port circuit
2.PAGE21: ADD GPIO circuit
3.PAGE 21: change SPDIF circuit
4.PAGE 27: remove PEX_VDD power switch circuit
5.PAGE 27: remove IFP_PLLVDD/2V5 power switch circuit cahnge APL5713 and APL5910 circuit
6.PAGE 28: remove FBVDDQ power switch circuit change APW7067N power circuit
7.PAGE 29: remove NVVDD VID circuit
8.PAGE 30: change NNVDD POWER APW7088 circuit
9.PAGE 16/17 : ADD EMI bridge R
10.PAGE 17 CO-LAYOUT HDIM CONNECT
11.PAGE 15 remove J2 D_SUB SLIM CONNECT
12.PAGE 29 ADD CH7322 circuit

V127-20 Base on V127-0A

1.PAGE30 .CO-LAYOUT RT9258 circuit

V143-0A Base on V127-20

1.PAGE3 update R611,R610 1KOhm
2.PAGE5/7/9/11 Remove DDR3 circuit, change DDR2 circuit
3.PAGE14.copy LAYOUT VGA slim
4.PAGE18. Remove DIP Display port circuit , power
5.PAGE18. ADD HDMI PORT CIRCUIT GPIO 19/21 , I2CD_SCL/SDA circuit
6.PAGE21ADD GPIO 19/21 , I2CD_SCL/SDA circuit
7.PAGE19. J3 modifty Pin header ,fly cable circuit

ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview

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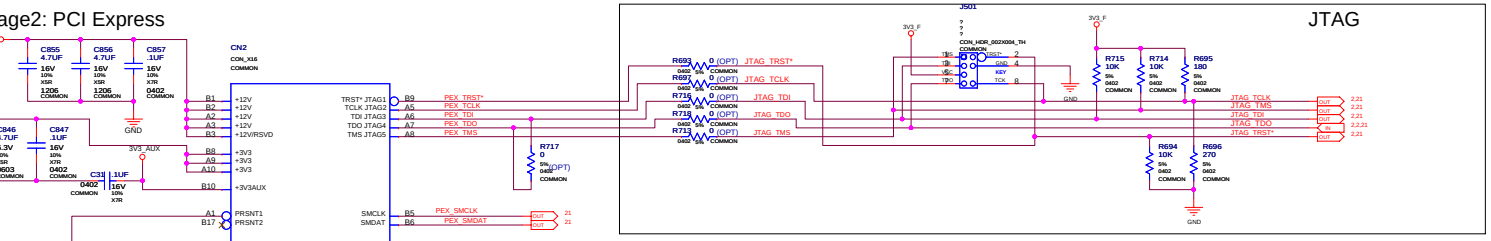

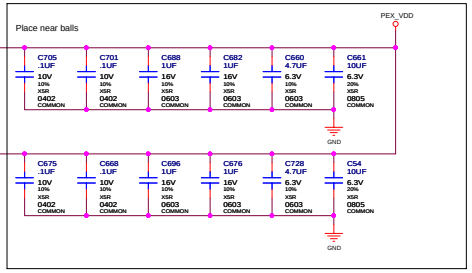

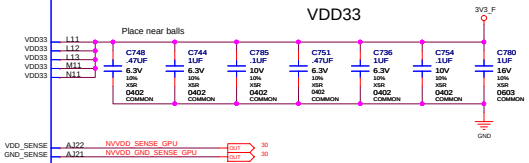

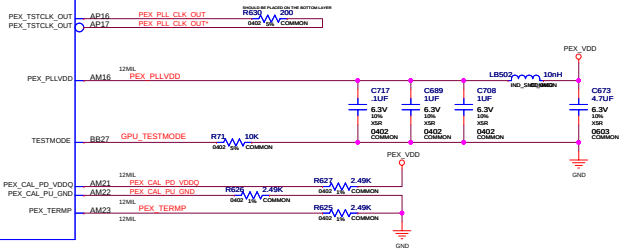

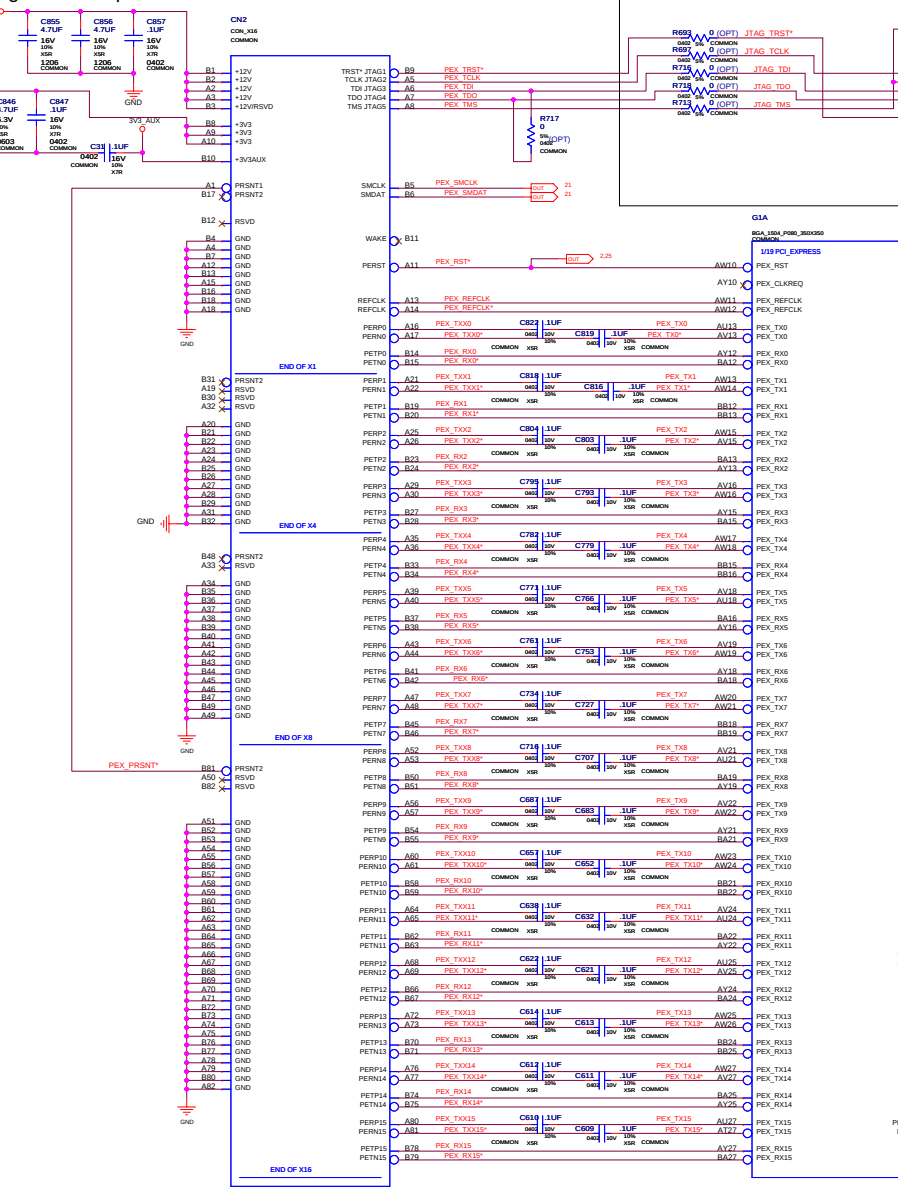

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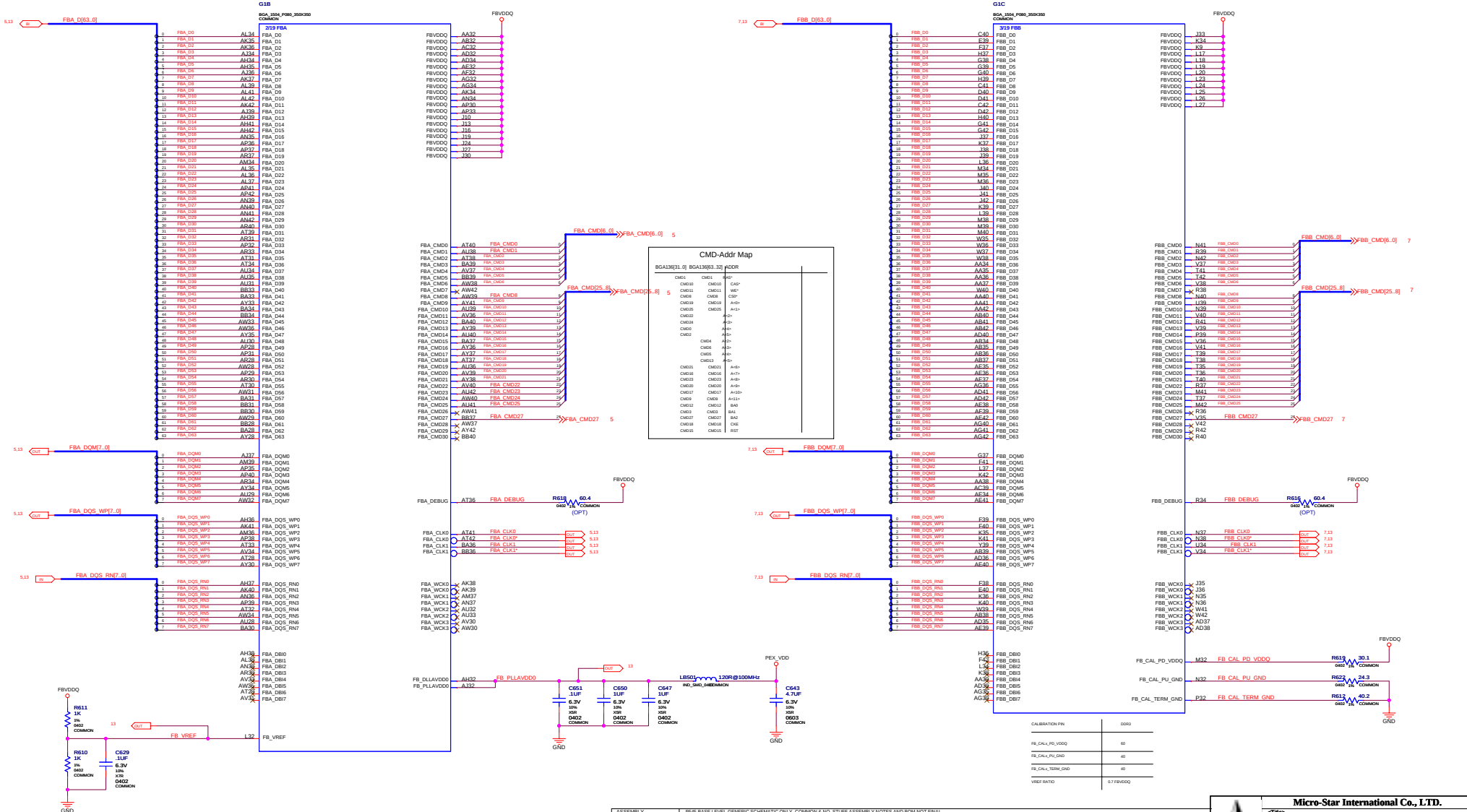

CALIBRATION PIN	DDR3
FB_CAL_PD_VDDQ	60
FB_CAL_PU_GND	40
FB_CAL_TERM_GND	40
VREF RATIO	0.7 FBVDDQ

ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: GPU Partition A/B

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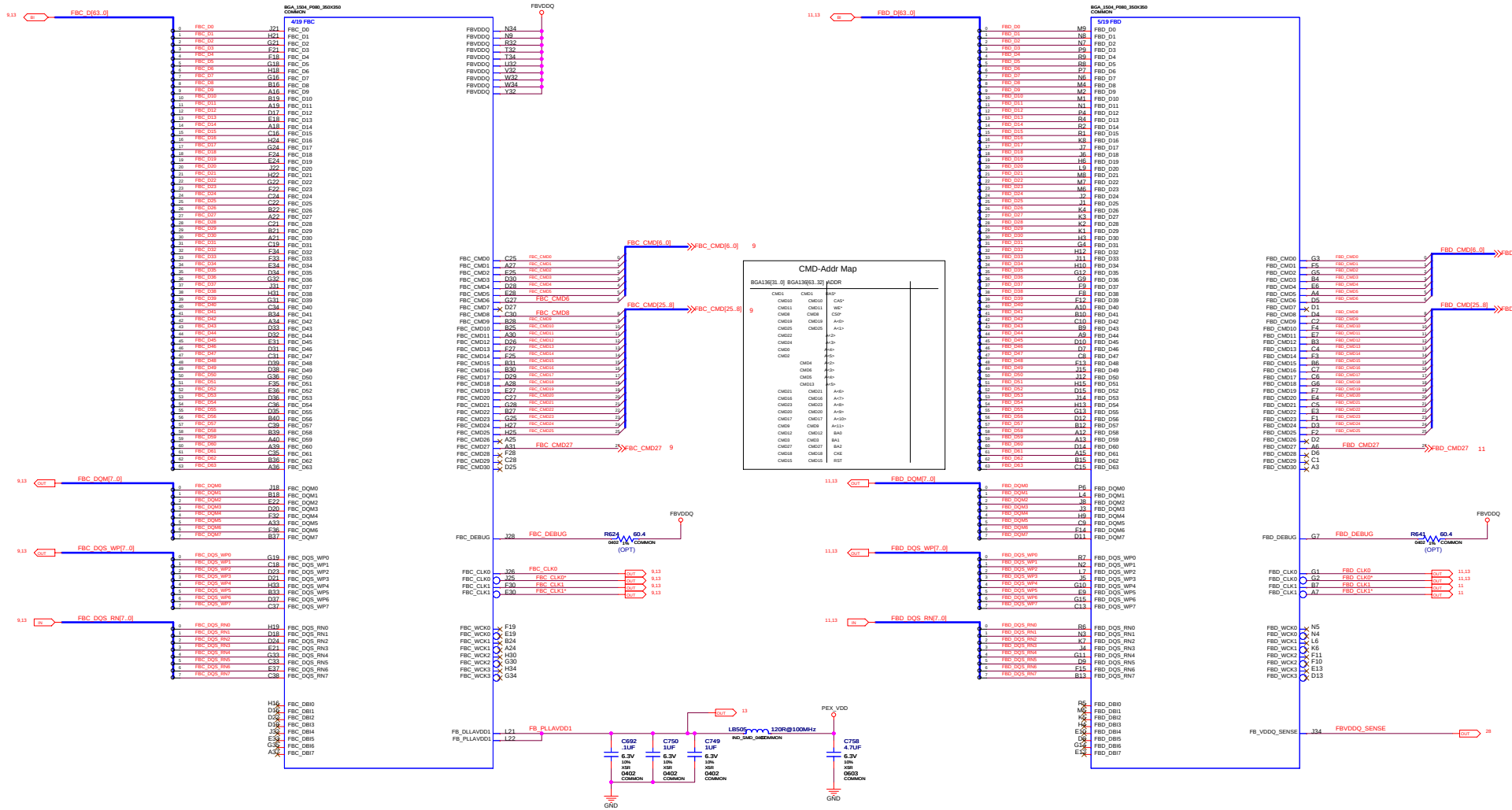

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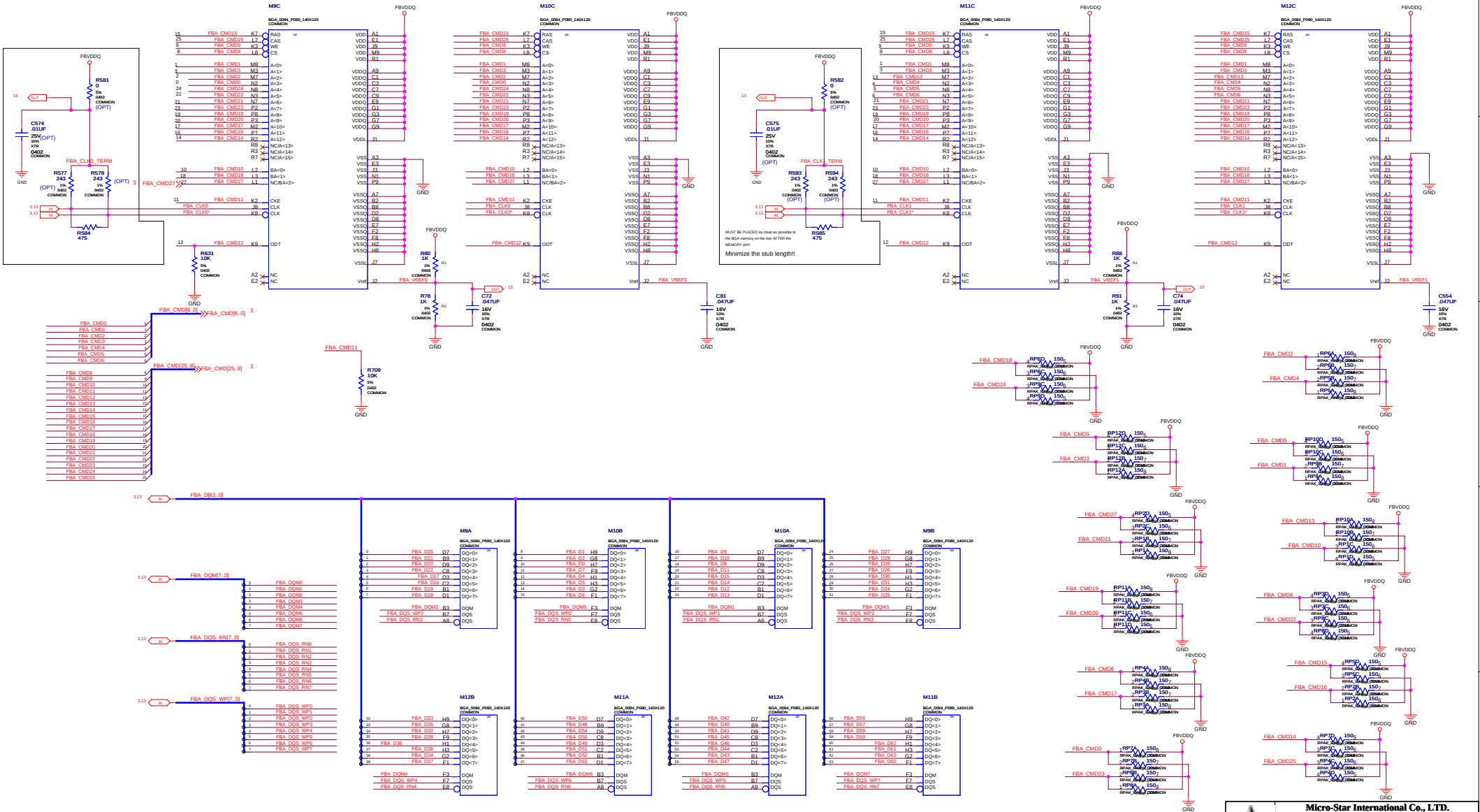
Page5: FBA Partition



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PAGE DETAIL	FBA Partition

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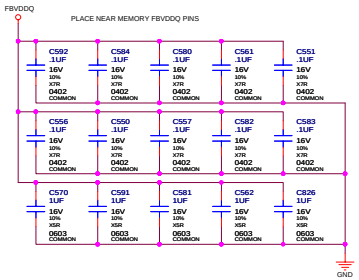

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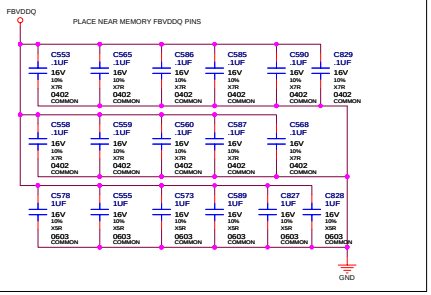

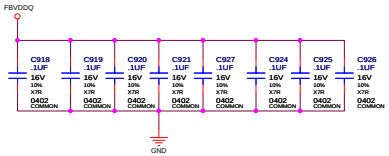

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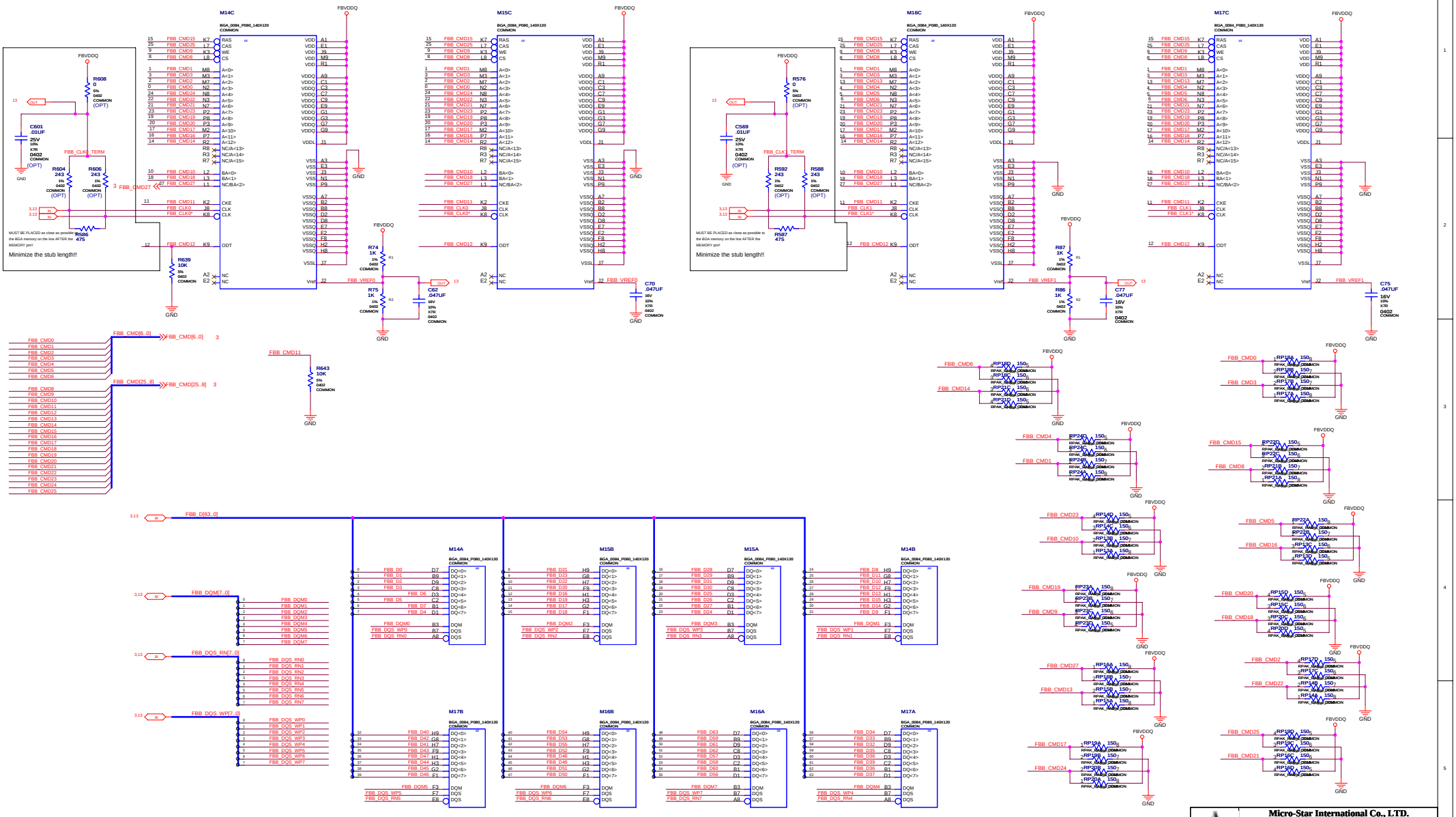

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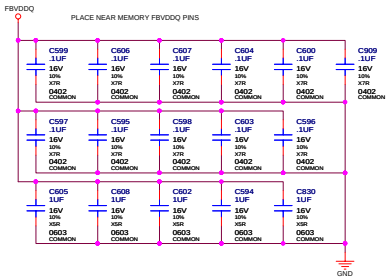

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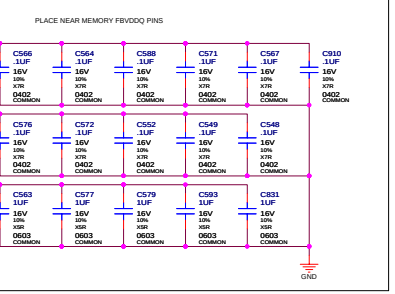

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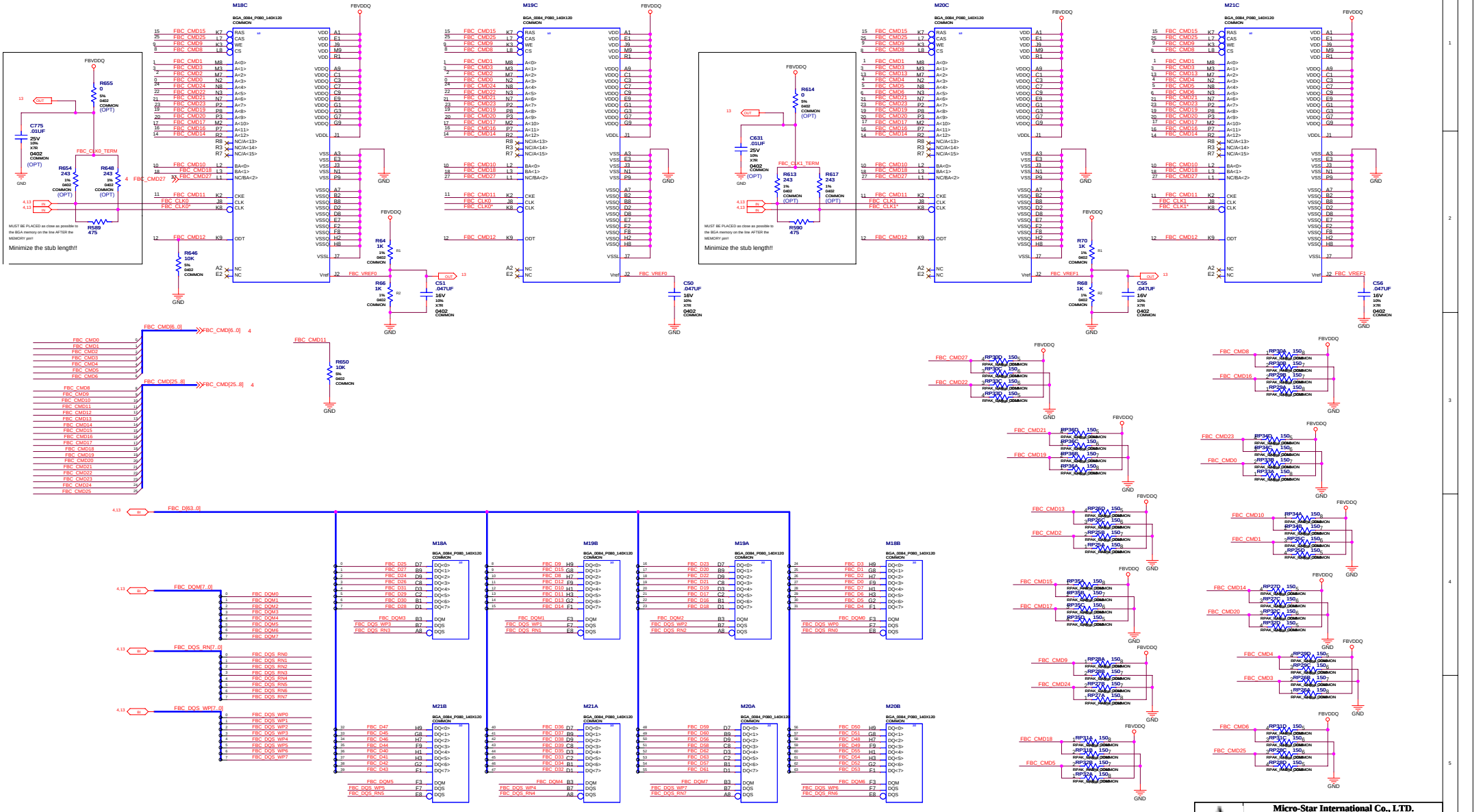

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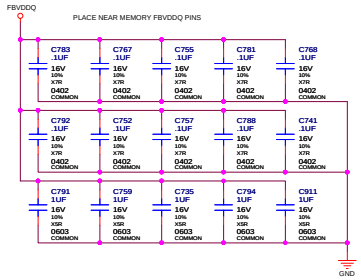

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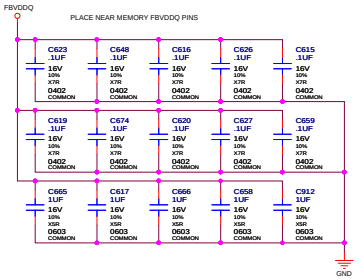

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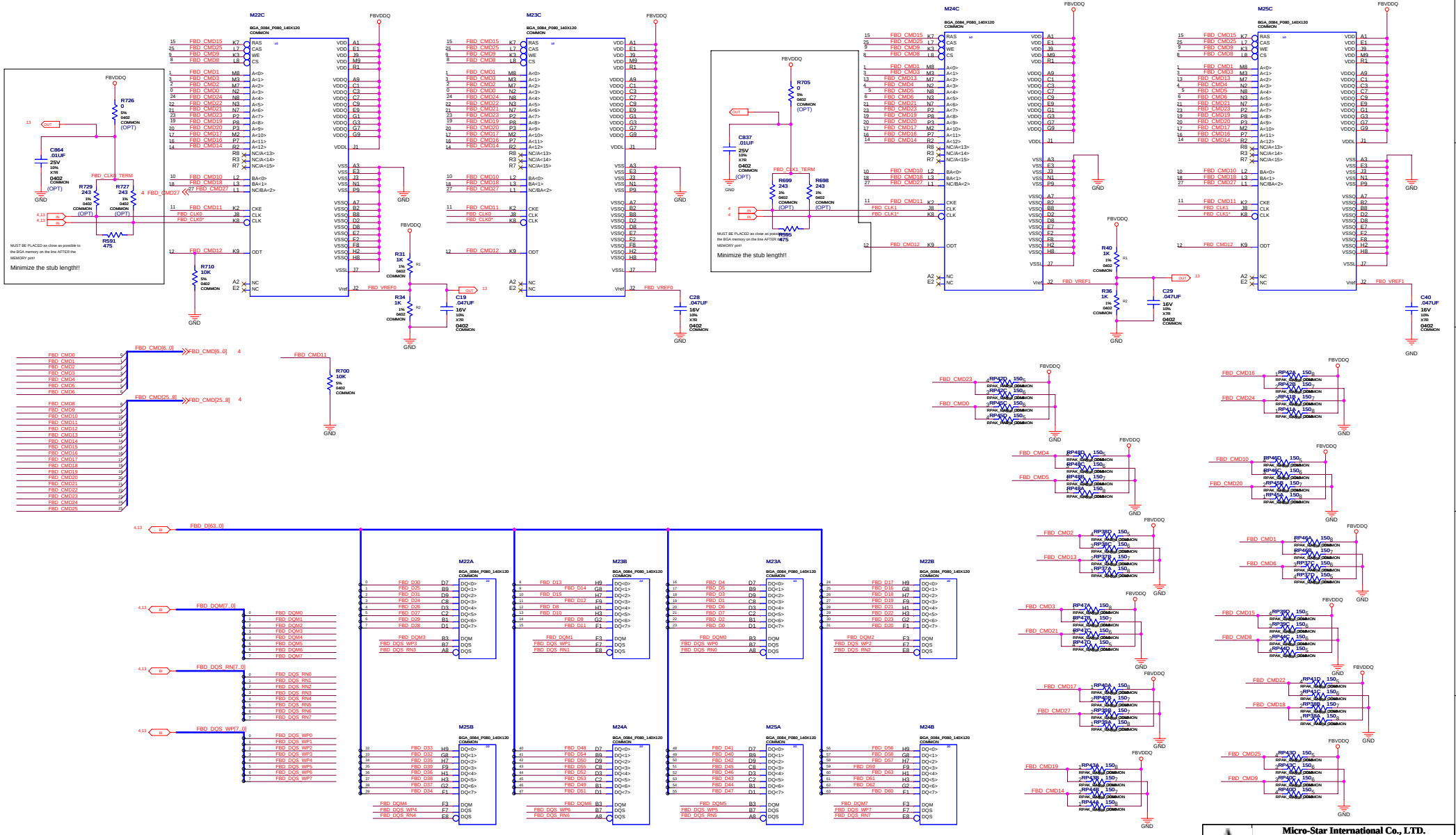

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PAGE DETAIL	FBD Partition

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Page12: FBD Partition Decoupling

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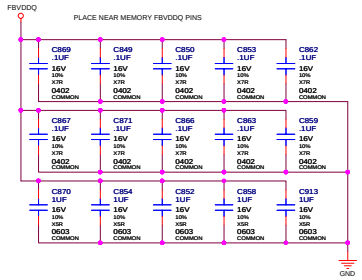

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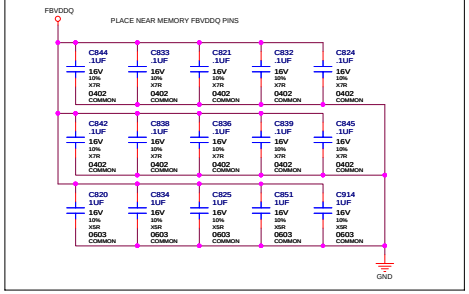

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Size	Document Number	Rev
Custom	<Doc>	<FevCode>

Date: Monday, April 14, 2008 Sheet 12 of 32

Page13: FB Net Properties

NET RULES for FBA and FBB

NET RULES for FBC and FBD

ASSEMBLY | PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL | FB Net Properties

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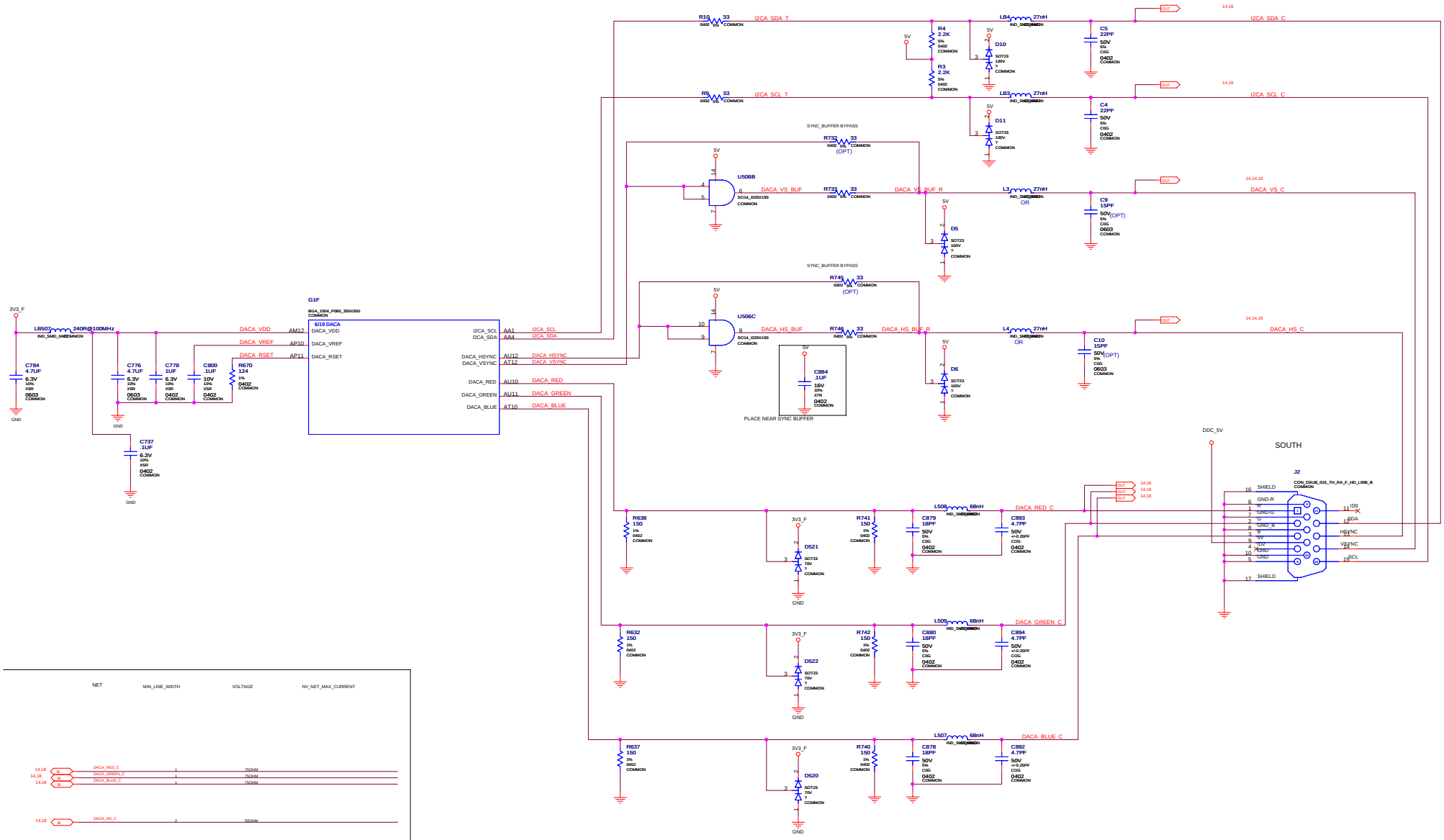
Date: Wednesday, April 09, 2008 Sheet 13 of 32

Page14: DACA Interface

DACA RGB-FILTER



NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
DACA_RED_C	1		75OHM
DACA_GREEN_C	1		75OHM
DACA_BLUE_C	1		75OHM
DACA_HS_C	2		50OHM
DACA_VS_C	2		50OHM

ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA Interface

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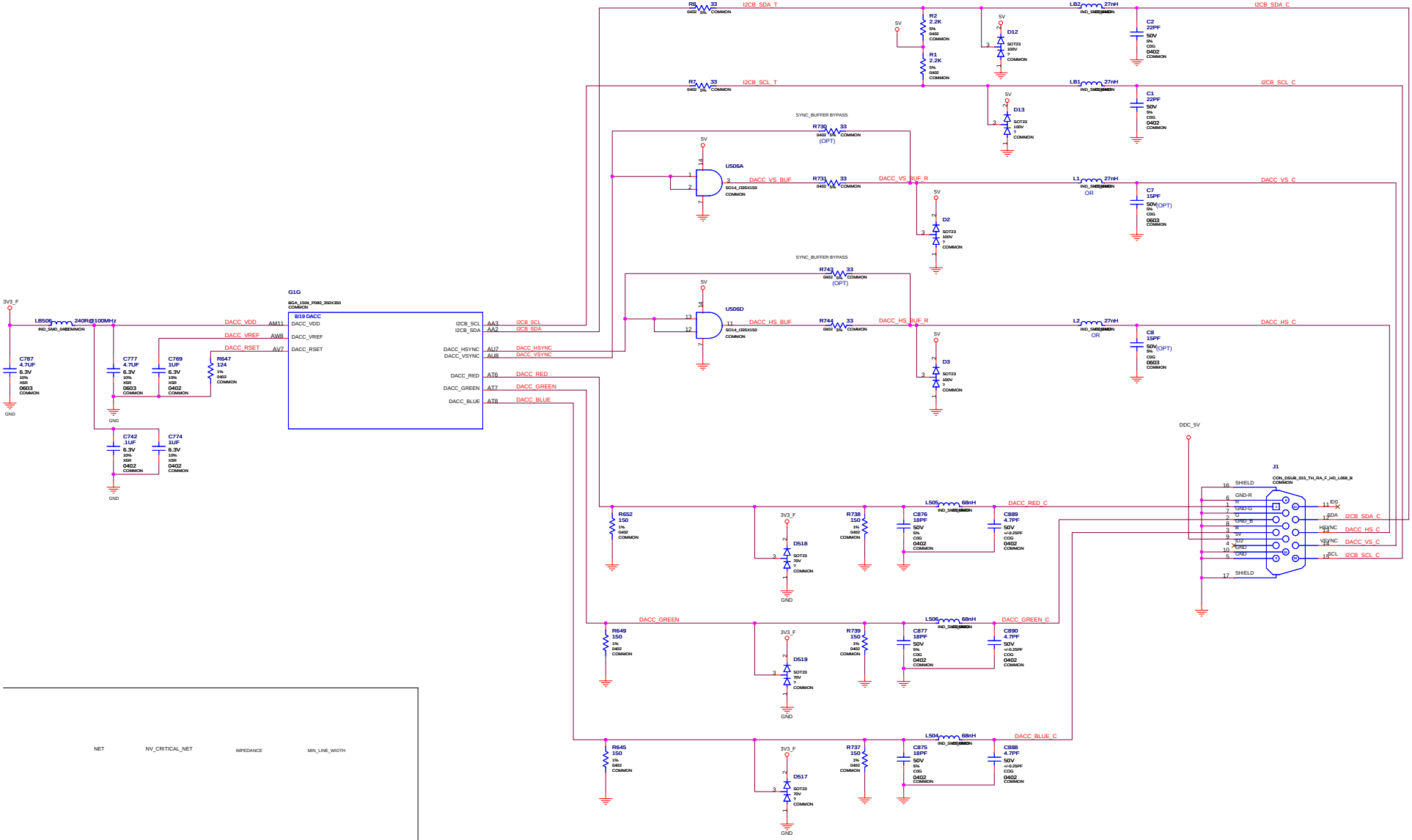
<Title>			
Size: Custom	Document Number: <Doc>		Rev: <RevCode>
Date: Monday, April 14, 2008	Sheet 14 of 32		

Page15: DACC Interface

DACC RGB-FILTER



NET	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH

ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC Interface

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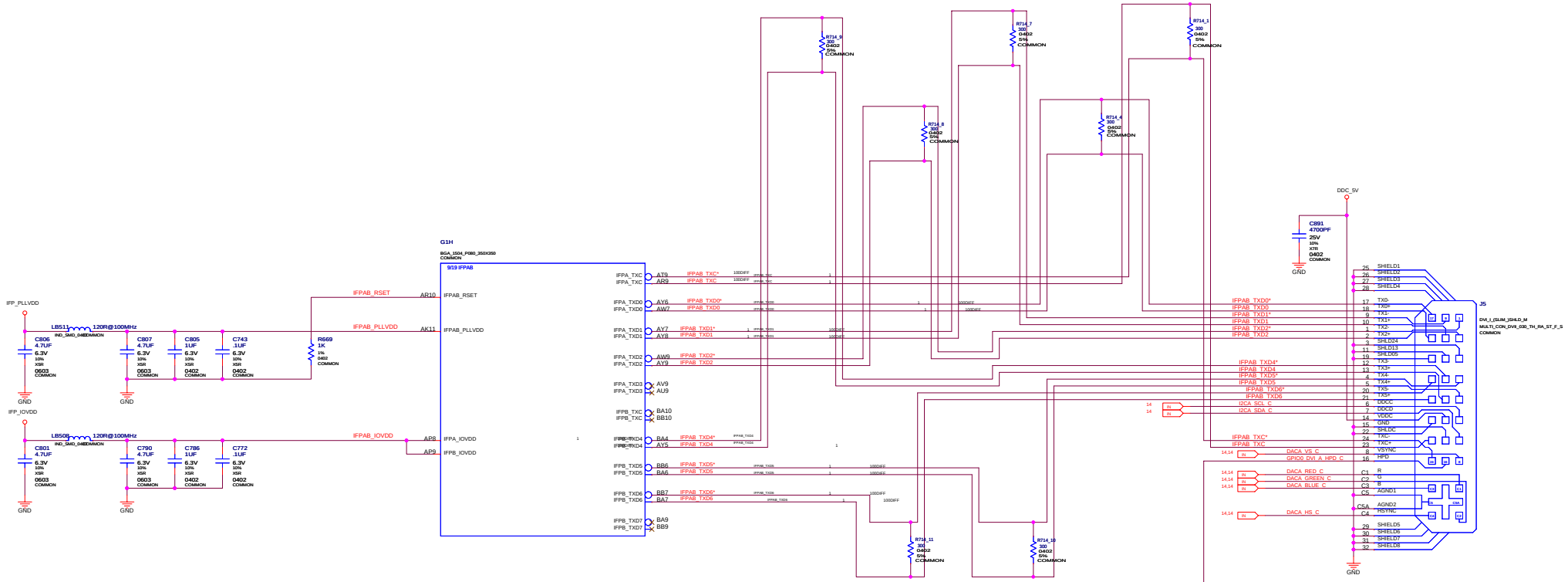
Size	Document Number	Rev
Custom	<Doc>	<FevCode>

Date: Monday, April 14, 2008 Sheet 15 of 32

Page16: IFP A/B Interface -- DVI Connector South



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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP A/B Interface -- DVI Connector South

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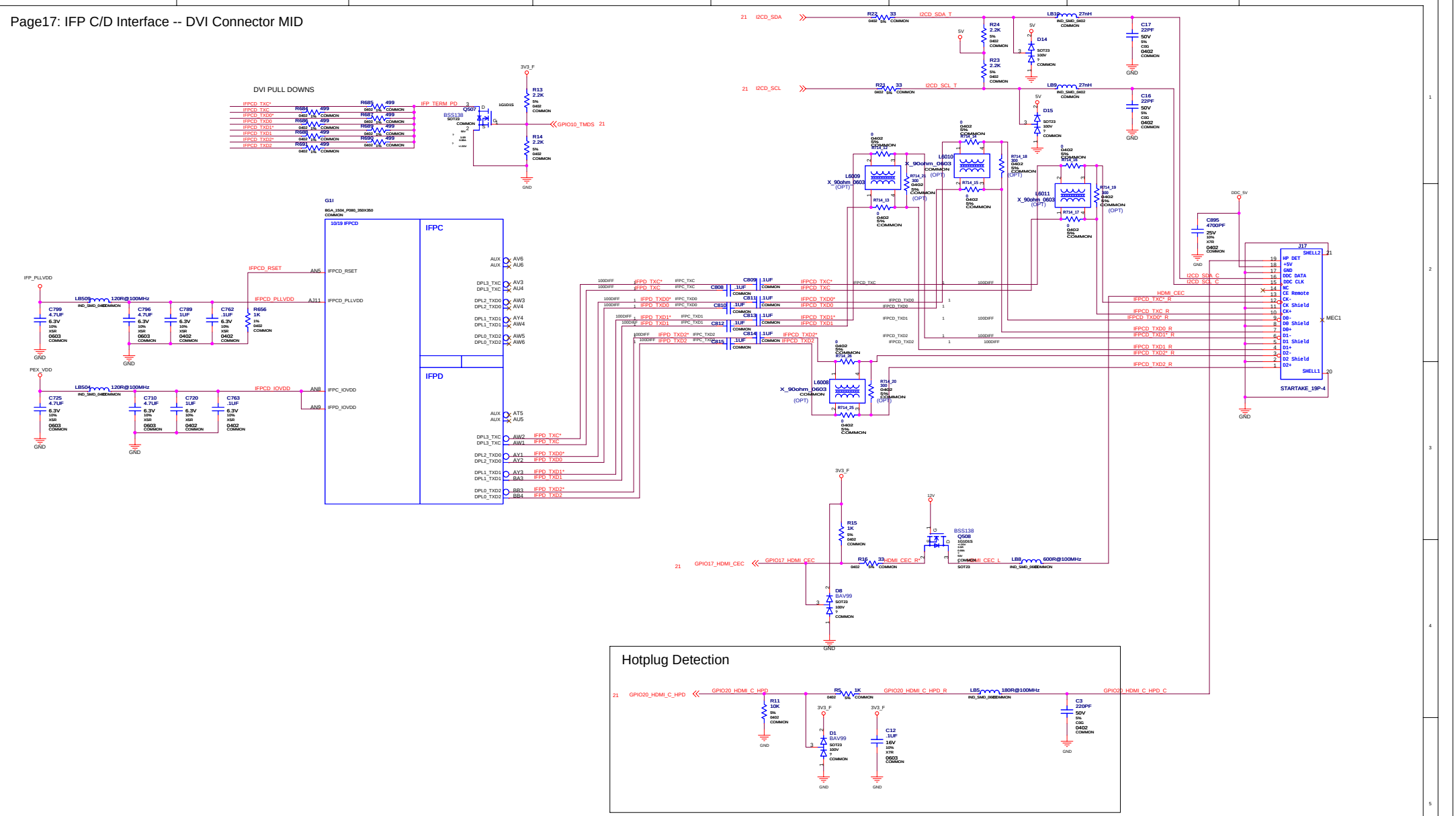
Date: Monday, April 14, 2008 Sheet 16 of 32

Page17: IFP C/D Interface -- DVI Connector MID



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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP C/D Interface -- DVI Connector MID

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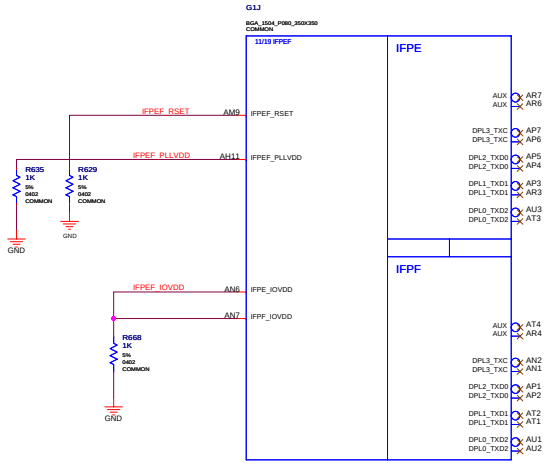
<Title>

Size	Document Number	Rev
Custom	<Doc>	<RevCode>

Date: Monday, April 14, 2008 Sheet 17 of 32

Page18: IFP E/F Interface -- Unused

TMDS E : Display Port



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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFP E/F Interface -- Unused

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<Title>

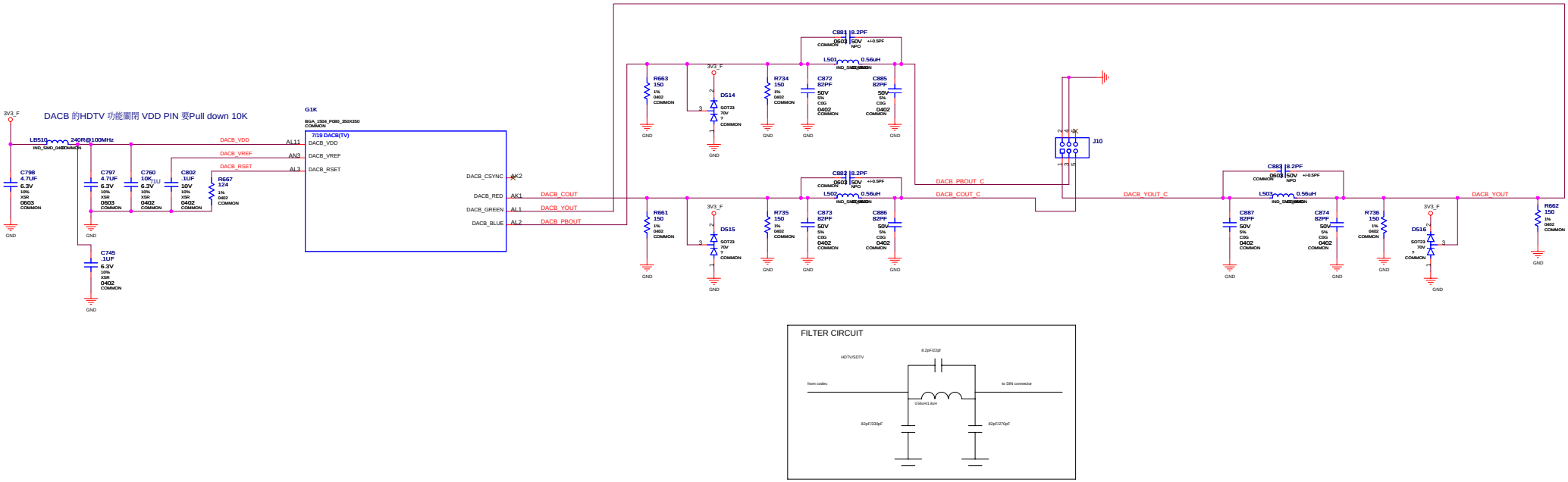
Size	Document Number	Rev
Custom	<Doc>	<FevCode>

Date: Monday, April 14, 2008 Sheet 18 of 32

Page19: DACB and HDTV/SDTV-Out

NET NET NV_CRITICAL_NET IMPEDANCE

DACB 的HDTV 功能關閉 VDD PIN 要Pull down 10K



FILTER CIRCUIT

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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB and HDTV/SDTV-Out

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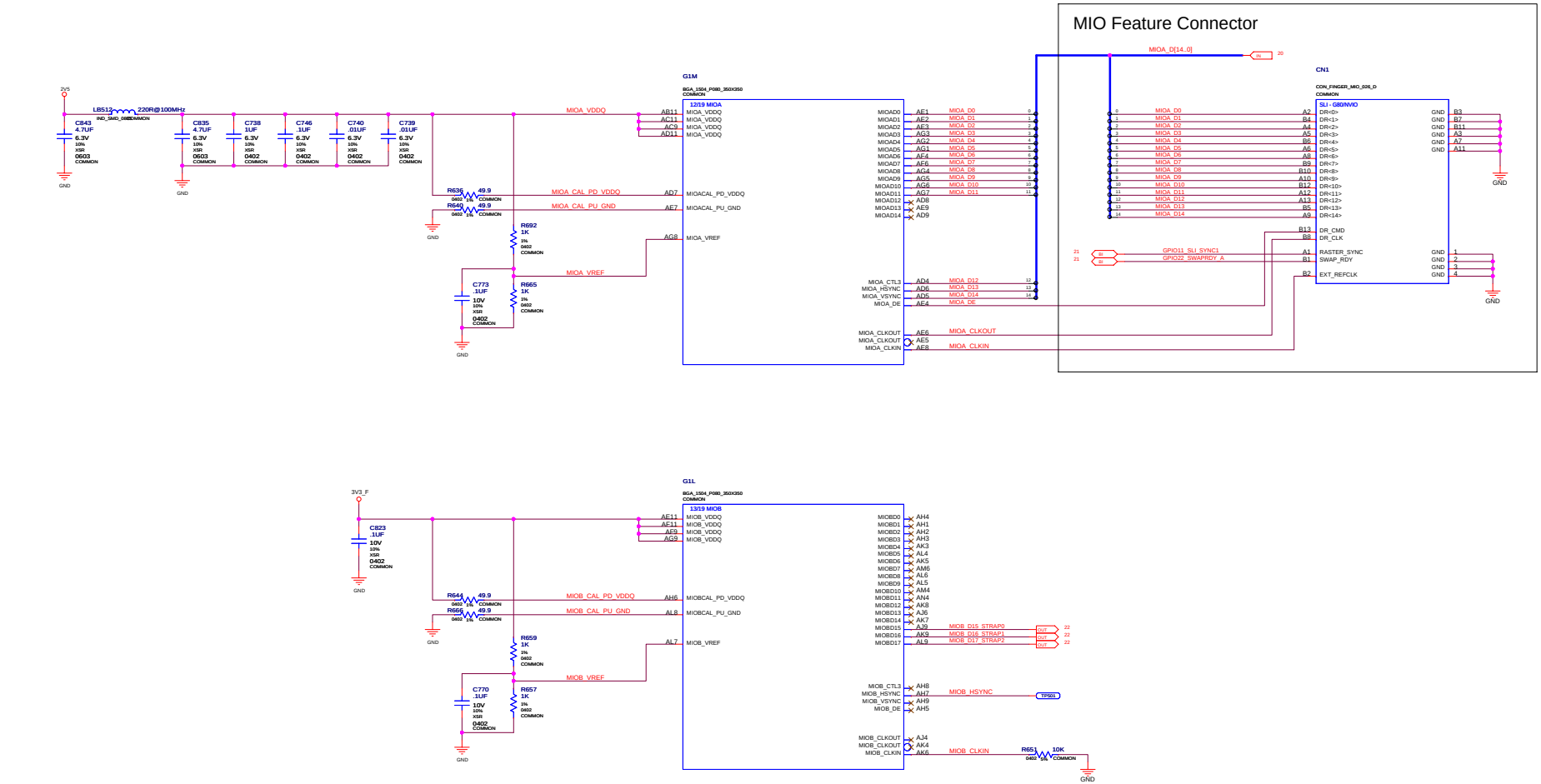
<Title>

Size	Document Number	Rev
Custom	<Doc>	<FevCode>

Date: Monday, April 14, 2008 Sheet 19 of 32

Page20: MIO A/B Interface



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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIO A/B Interface

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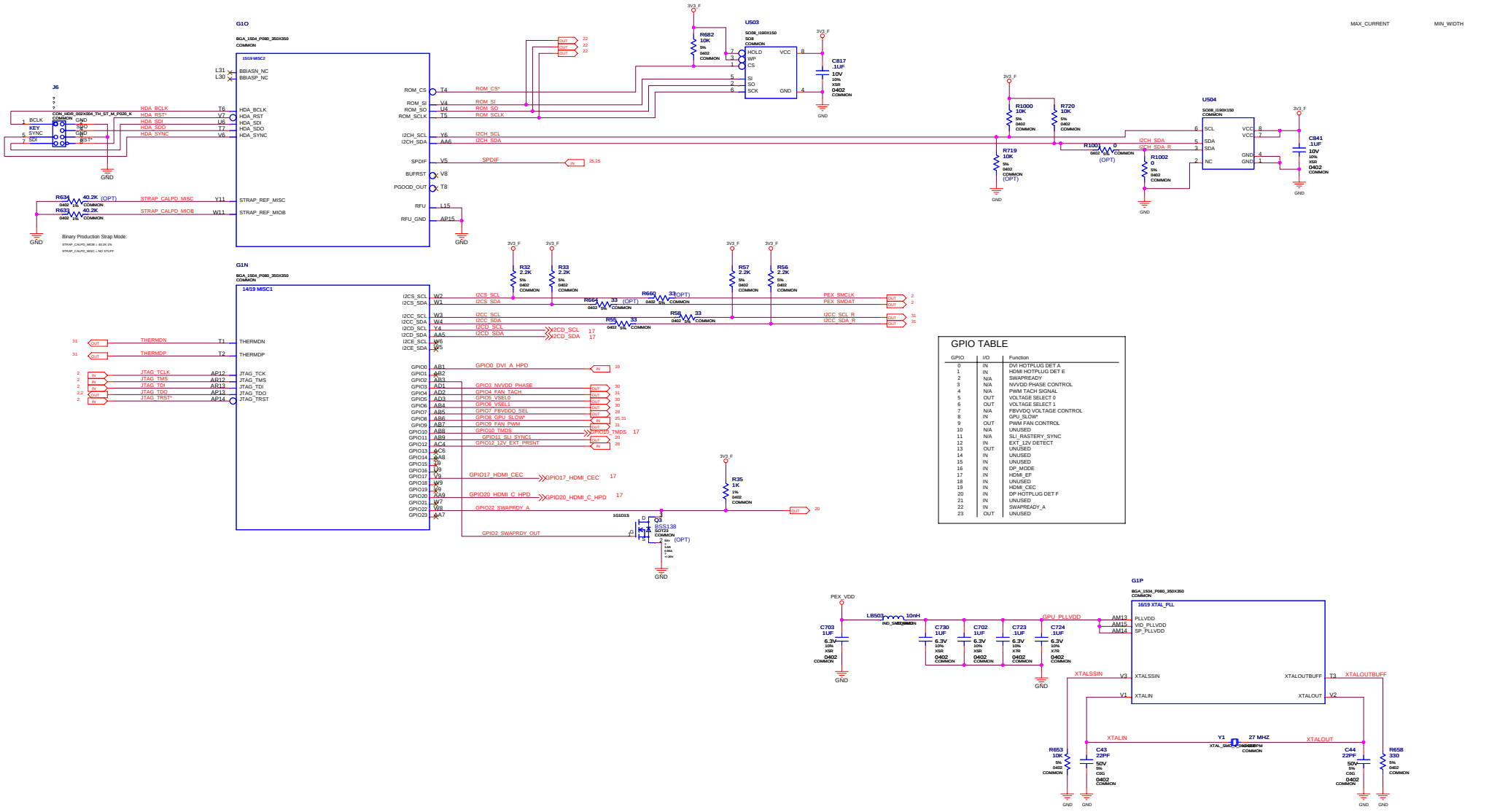
<Title>

Size	Document Number	Rev
Custom	<Doc>	<FevCode>

Date: Monday, April 14, 2008 Sheet 20 of 32

Page21: MISC: GPIO, I2C, ROM, HDCP, and XTAL



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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO, I2C, ROM, HDCP, and XTAL

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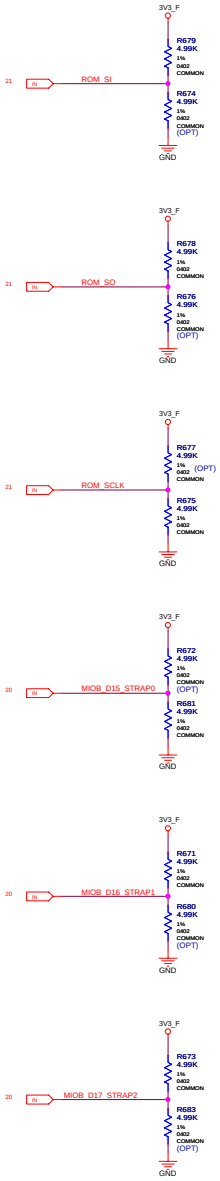
<Title>

Size	Document Number	Rev
Custom	<Doc>	<FevCode>

Date: Monday, April 14, 2008 Sheet 21 of 32

Page22: Strap Configuration



STRAP PIN	STRAP NAME
ROM_SI	PCI_DEVID_EXT

STRAP PIN	STRAP NAME
ROM_SO	SLOT_CLK_CFG

STRAP PIN	STRAP NAME
ROM_SCLK	PCI_DEVID[3]

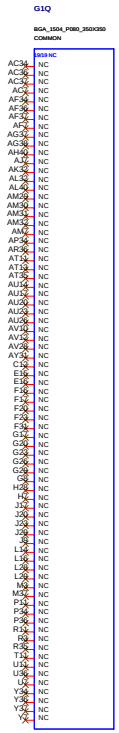
STRAP PIN	STRAP NAME
STRAP0	RAMCFG0
STRAP1	RAMCFG1
STRAP2	RAMCFG2

* RAMCFG[2:0]

256MB (8Mx32)	512MB (16Mx32)	1024MB (32Mx32)
101 --- 256-bit Qimonda 110 --- 256-bit Hynix 111 --- 256-bit Samsung	001 --- 256-bit Qimonda 010 --- 256-bit Hynix 011 --- 256-bit Samsung	101 --- 256-bit Hynix 110 --- 256-bit Hynix 111 --- 256-bit Samsung

* VBIOS will be defined on a per SKU basis.

	3V3	GND
5K	1	0



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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Strap Configuration

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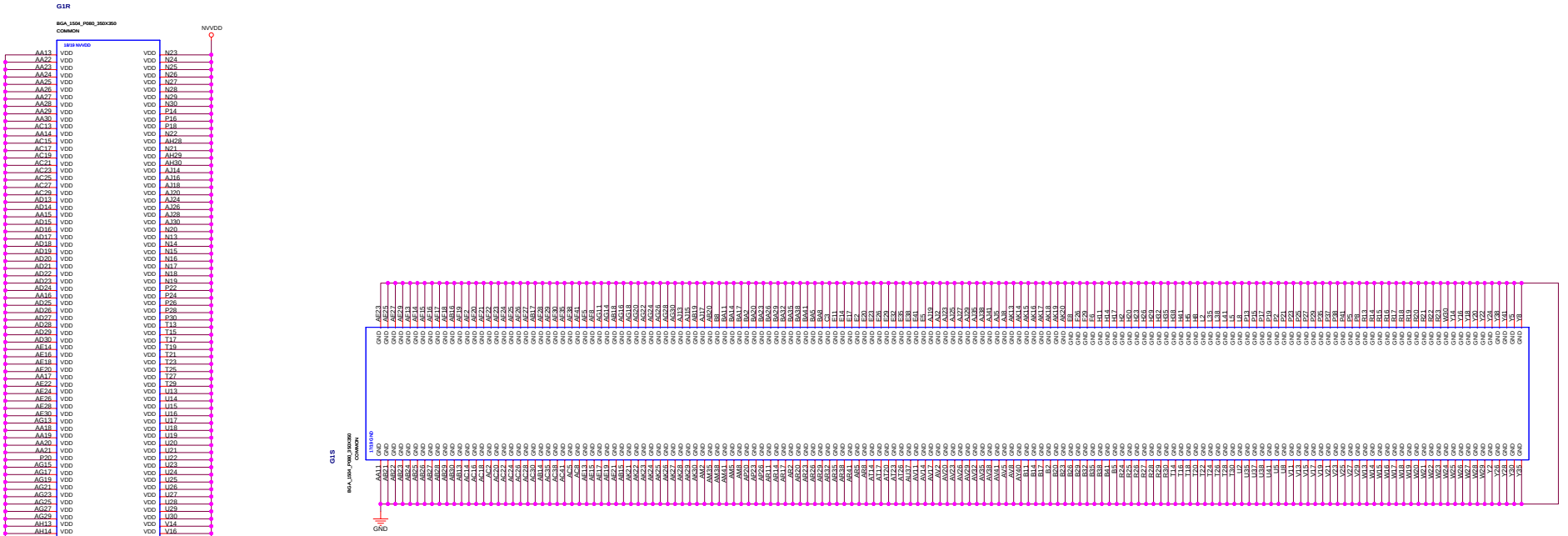
<Title>

Size	Document Number	Rev
Custom	<Doc>	<FevCode>

Date: Monday, April 14, 2008 Sheet 22 of 32

Page23: PWR and GND Signals



ASSEMBLY: P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL: PWR and GND Signals

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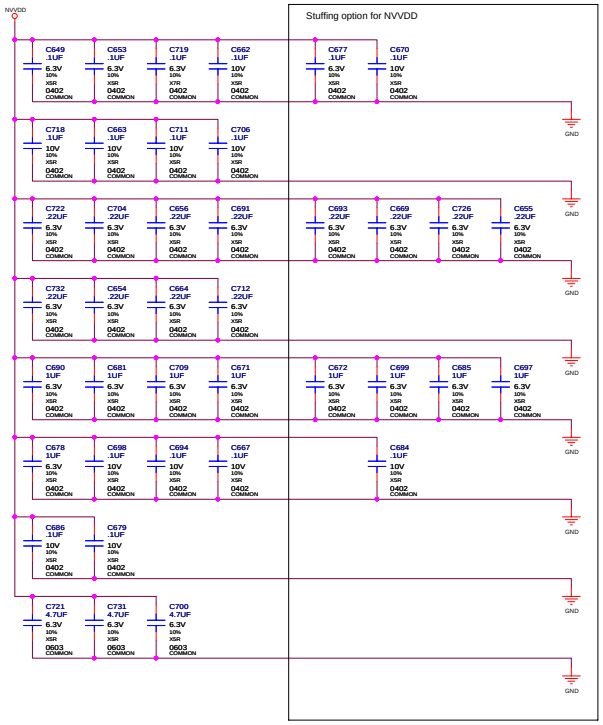
Size	Document Number	Rev
Custom	<Doc>	<FevCode>

Date: Monday, April 14, 2008 Sheet 23 of 32

Page24: NVVDD and FBVDDQ Decoupling

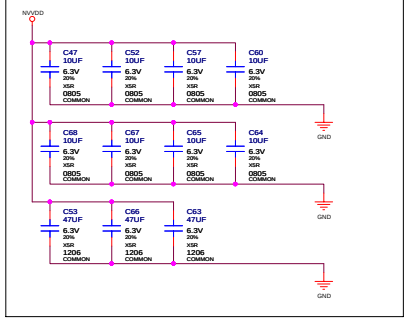
NVVDD

Place under GPU



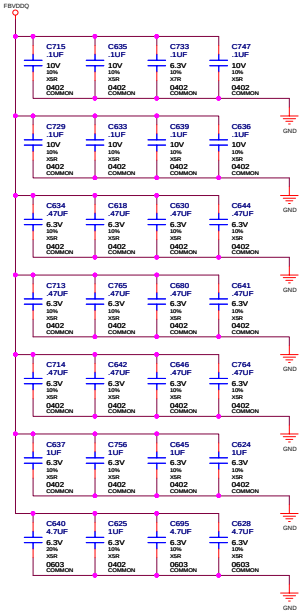
NVVDD

Place close to GPU



FBVDDQ

Place near BGA



ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	NVVDD and FBVDDQ Decoupling

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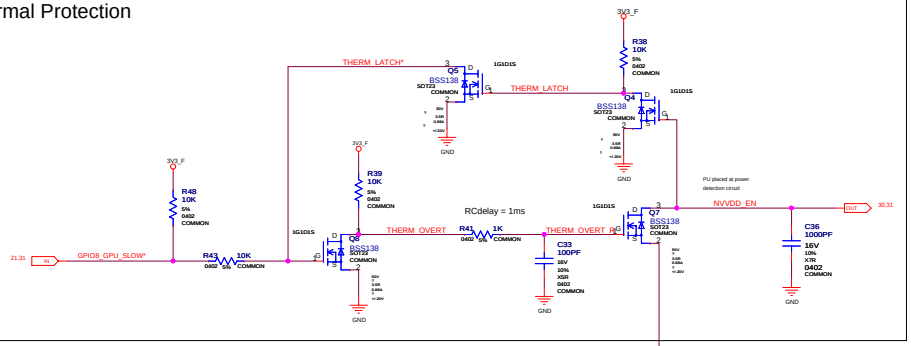
Size	Document Number	Rev
Custom	<Doc>	<FevCode>
Date: Monday, April 14, 2008	Sheet 24 of 32	

Page25: SPDIF Input, Thermal Protection, and IFP_IOVDD Power Supply

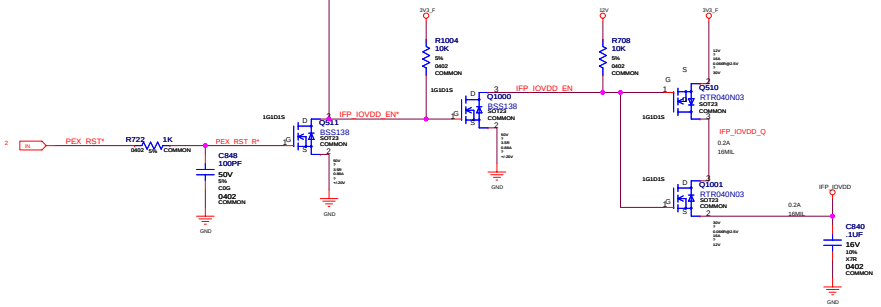
NET	IMPEDANCE	NV_CRITICAL_NET
21,25 IN SPDIF	55OHM	1

Thermal Protection

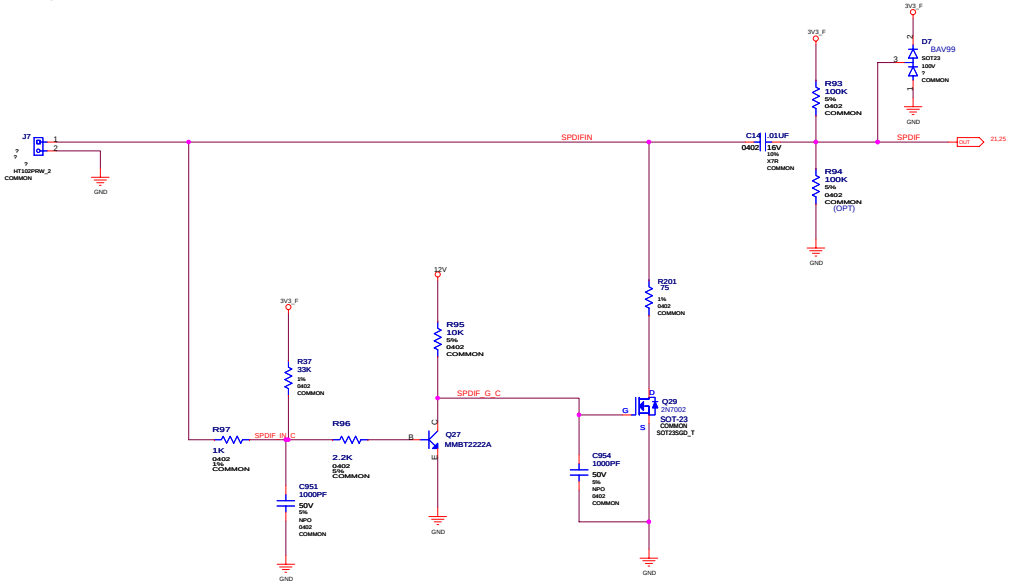


IFP_IOVDD Backdrive Prevention

Stuffing posibilities for thermal control and protection:



SPDIF Input



ASSEMBLY	PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF Input, Backdrive Protection, and IFP_IOVDD Power Supply

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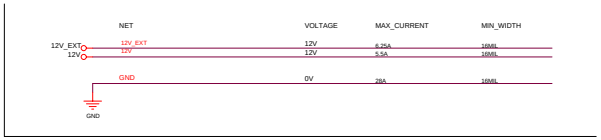
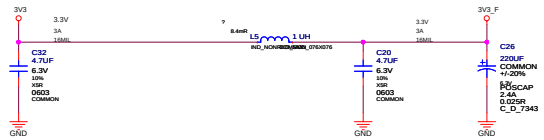
<Title>		
Size: Custom	Document Number: <Doc>	Rev: <FevCode>
Date: Monday, April 14, 2008	Sheet 25 of 32	

Page26: PS I: 3V3, 12V, and 12V_EXT Power Supply Filter



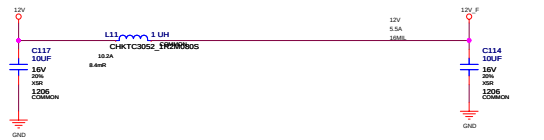
3V3 Power Supply Filter

3V3_F = 3.3V @ 2.5A



12V Power Supply Filter

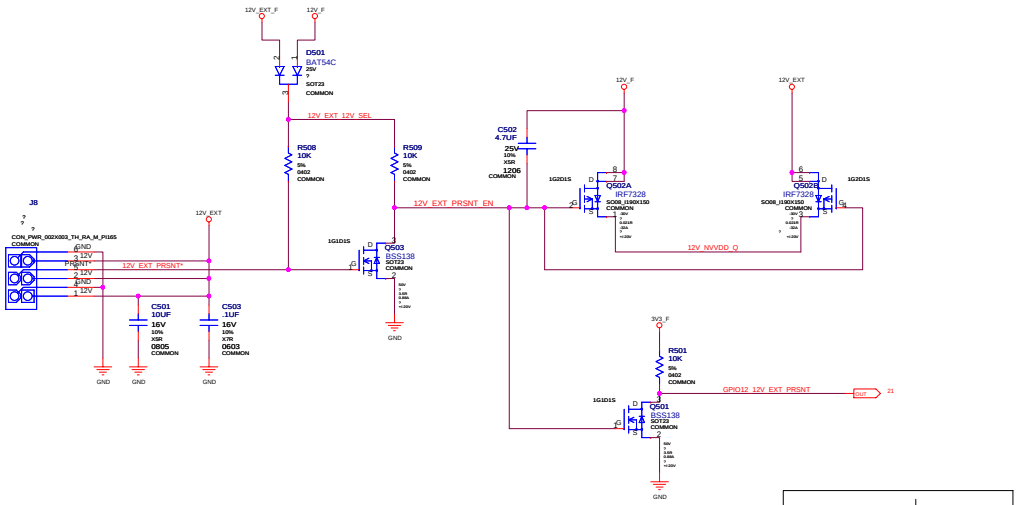
12V_F = 12V @ 5.5A



12V_EXT Power Supply Filter

12V_EXT_F = 12V @ 6.25A

INPUT POWER SELECTION for NVVDD



	GPIO12
EMERENCY MODE (12V_EXT present)	0
150W POWER MODE (12V_EXT NOT present)	1

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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS I: 3V3, 12V, and 12V_EXT Power Supply Filter

Micro-Star International Co., LTD.

<Title>

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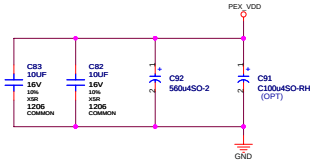
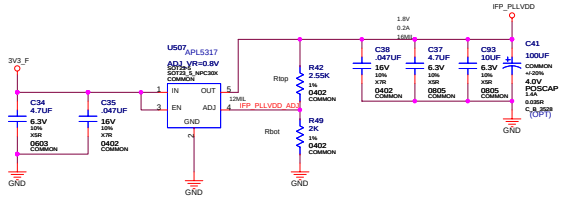
Page27: PS II: IFP_PLLVDD, 2V5, 5V, and DDC_5V Power Supply



IFP_PLLVDD Power Supply

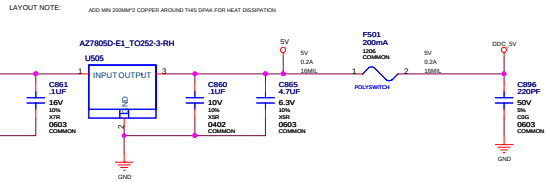
IFP_PLLVDD = 1.8V @ 200mA



IFP_PLLVDD = VREF * (1 + (Rtop / Rbot))
1.82V = 0.8V * (1 + (2.5K/2K))

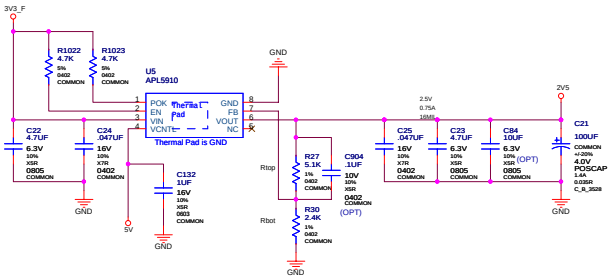
5V and DDC_5V Power Supply

DDC_5V = 5V @ 200mA



2V5 Power Supply

2V5 = 2.5V @ 750mA



2V5 = VREF * (1 + (Rtop / Rbot))
2.5V = 0.8V * (1 + (5.1K/2.4K))

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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS II: PEX_VDD, IFP_PLLVDD, 2V5, 5V, and DDC_5V Power Supply

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<Title>

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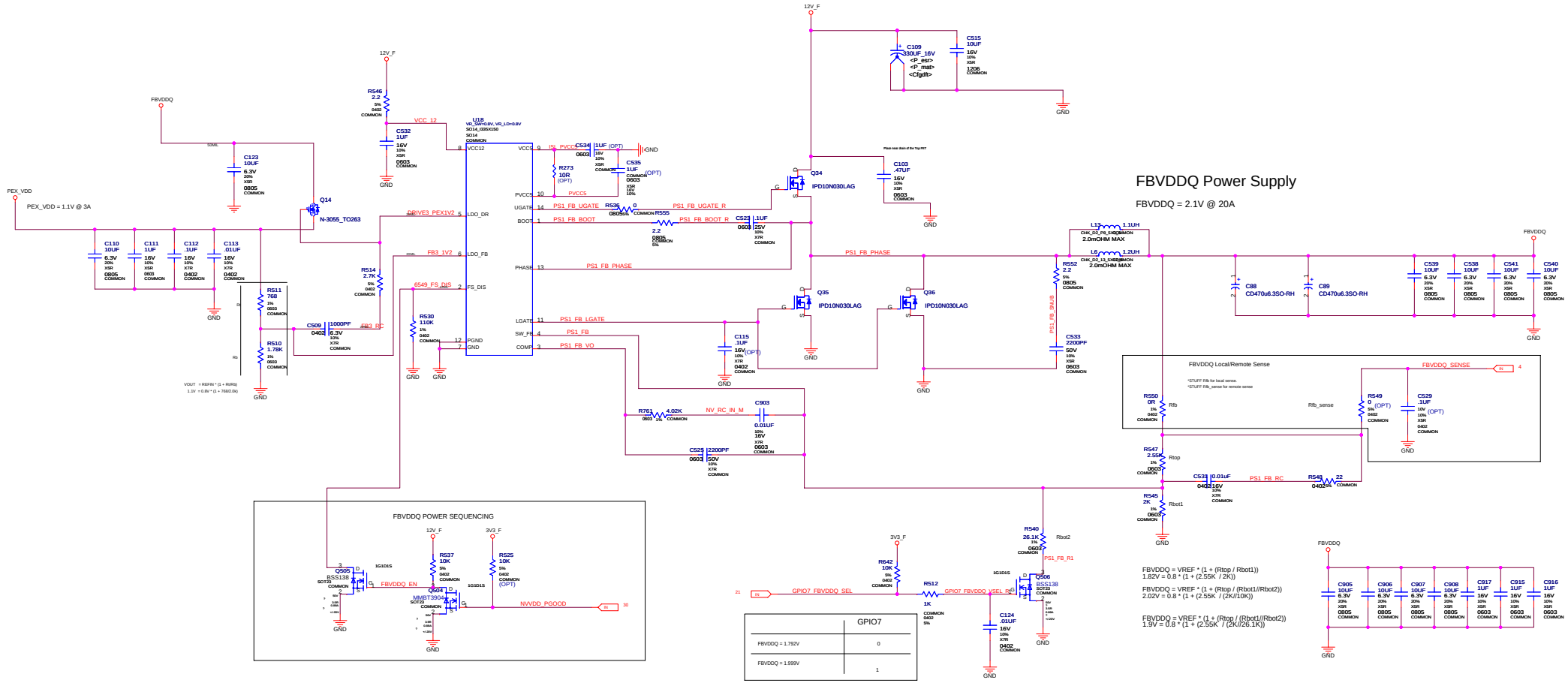
Page28: PS III: FBVDDQ Power Supply



ASSEMBLY: PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: PS III: FBVDDQ Power Supply

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Page29: PS IV: NVVDD VID Control

NVVDD Voltage Select

NVVDD range 0.80V-1.40V

Regulator: ADP3208
Control via NV_GPIOs NV_VSEL[1..0]

VID							NVVDD	
6	5	4	3	2	1	0	Vout	G94
0	1	1	1	0	0	0	0.80V	
0	1	1	0	1	0	0	0.85V	
0	1	1	0	0	0	0	0.90V	
0	1	0	1	1	0	0	0.95V	
0	1	0	1	0	0	0	1.00V	=> Default
0	1	0	0	1	0	0	1.05V	=> Voltage1
0	1	0	0	0	0	0	1.10V	=> Voltage2
0	0	1	1	1	0	0	1.15V	
0	0	1	1	0	0	0	1.20V	
0	0	1	0	1	0	0	1.25V	
0	0	1	0	0	0	0	1.30V	
0	0	0	1	1	0	0	1.35V	
0	0	0	1	0	0	0	1.40V	

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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS IV: NVVDD VID Control

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<Title>

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Page30: PS V: NVVDD Power Supply

GPIO6	GPIO5	NVVDD
1	0	1.1V
0	1	1.05V
0	0	1.0V

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH

NVVDD Power Supply

NVVDD = 0.9-1.1V @ 40-50A

NVVDD Sequence

	GPIO3
2-PHASE CONFIG	0
1-PHASE CONFIG	1

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ASSEMBLY: PS45 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: PS V: NVVDD Power Supply

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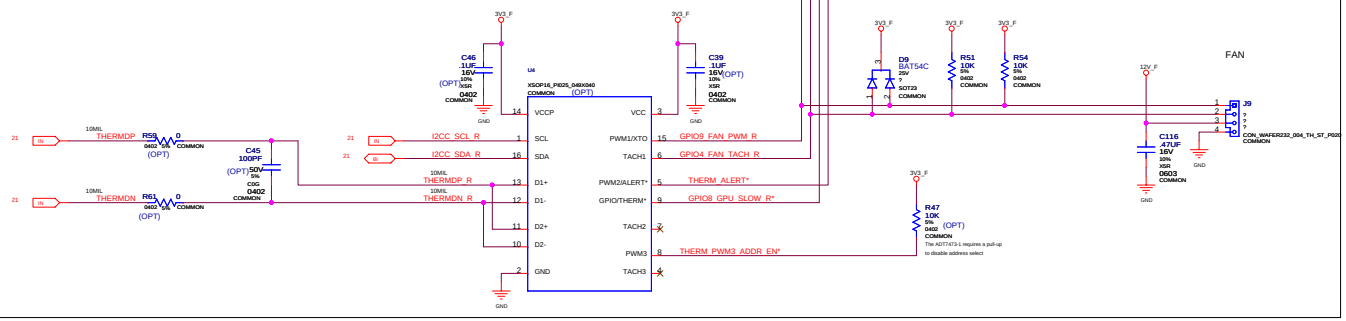
Date: Monday, April 14, 2008 | Sheet 30 of 32

Page31: Thermal Diode and Fan Control

ADT7473 External Fan/Thermal Control



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ASSEMBLY	P545 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Diode and Fan Control

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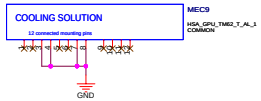
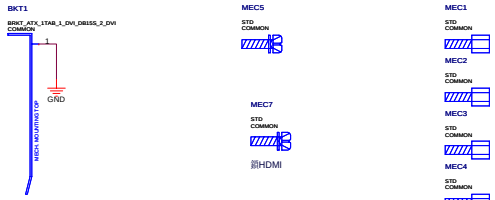
Page32: Thermal, Mechanical, and Bracket

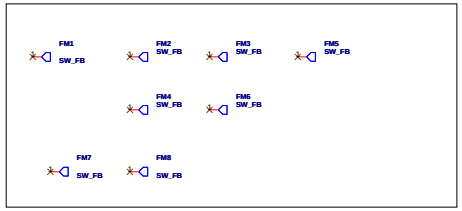
Thermal

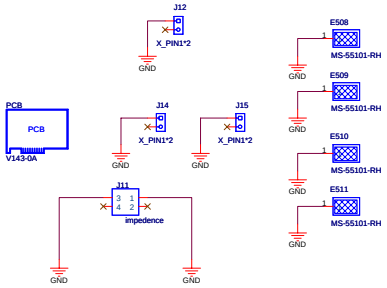


Mechanical

Bracket







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PAGE DETAIL	Thermal, Mechanical, and Bracket

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