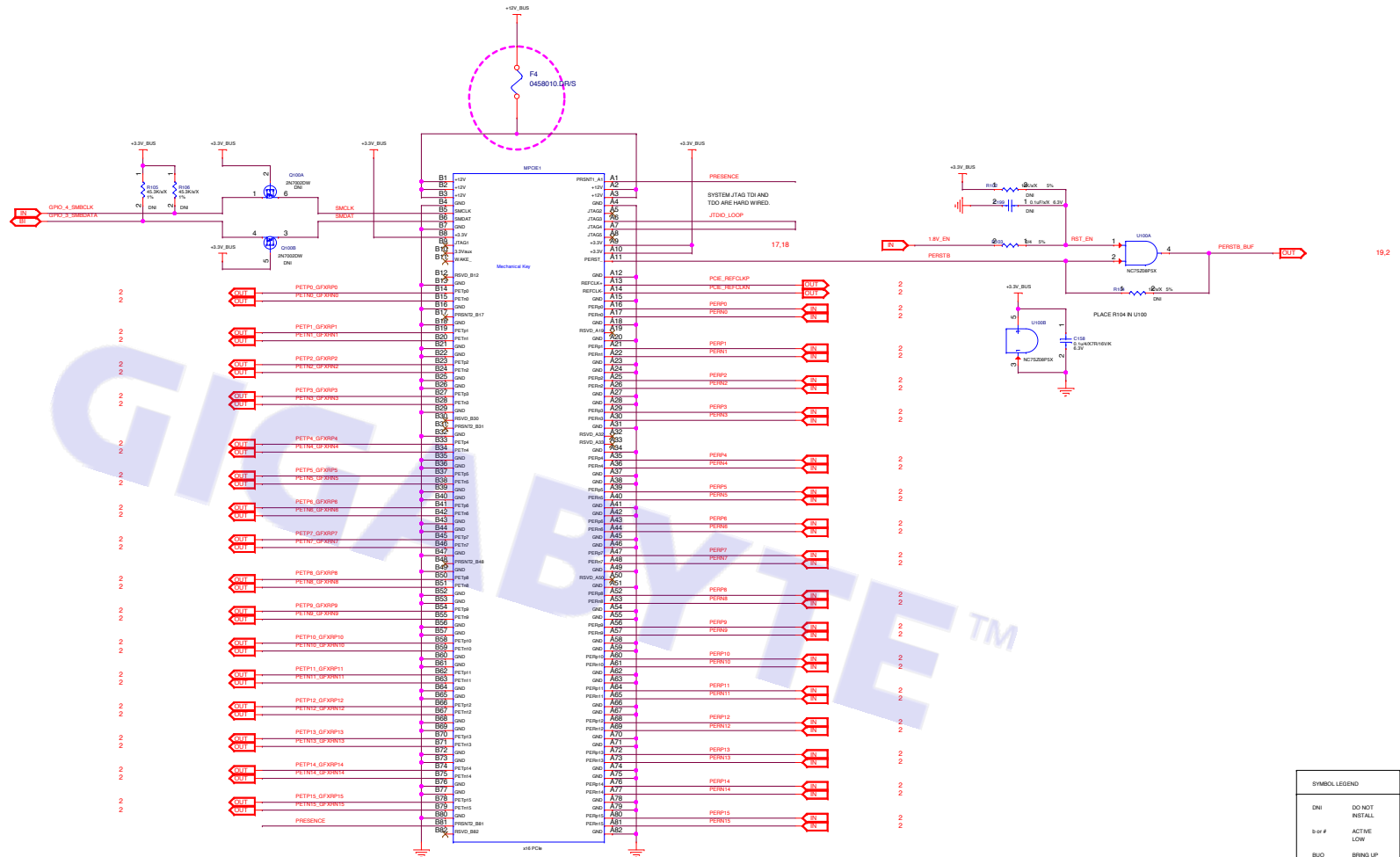
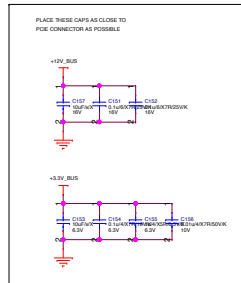
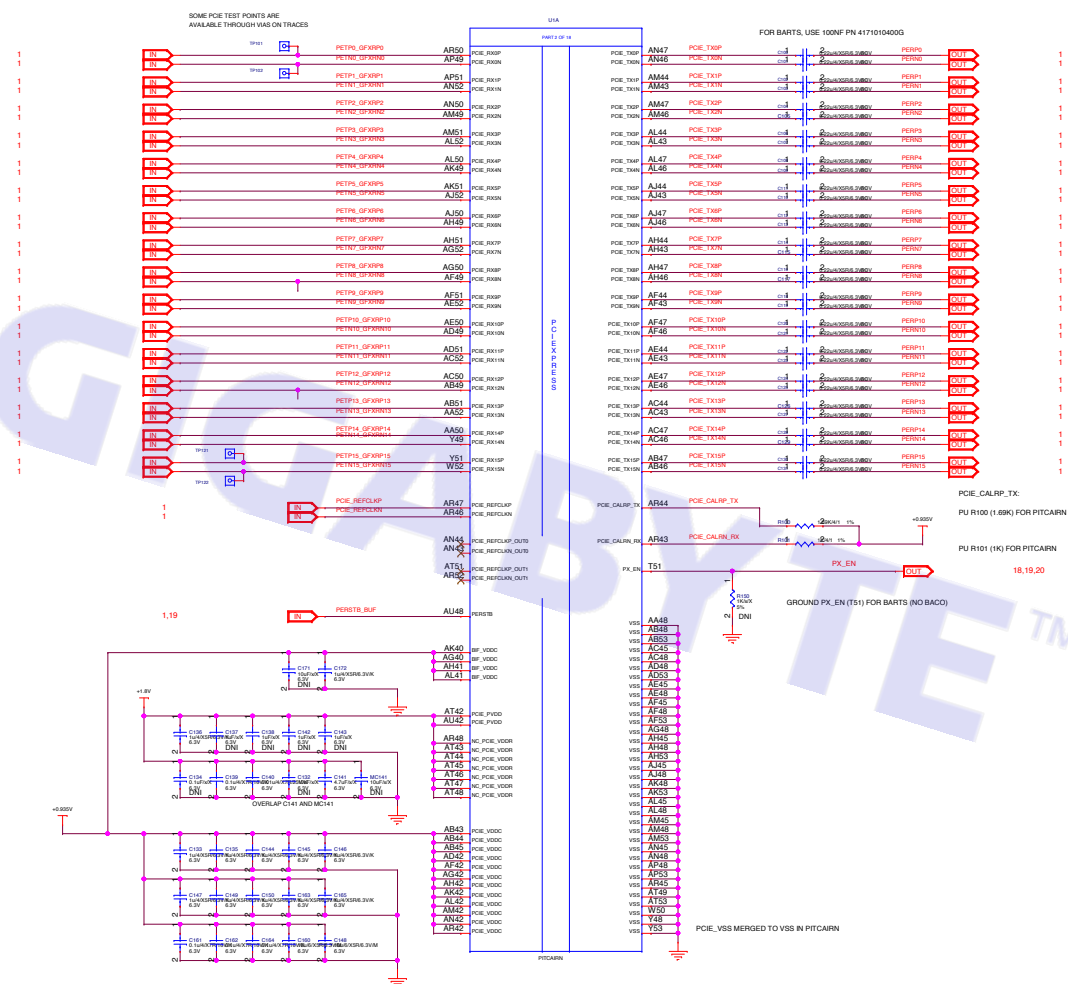


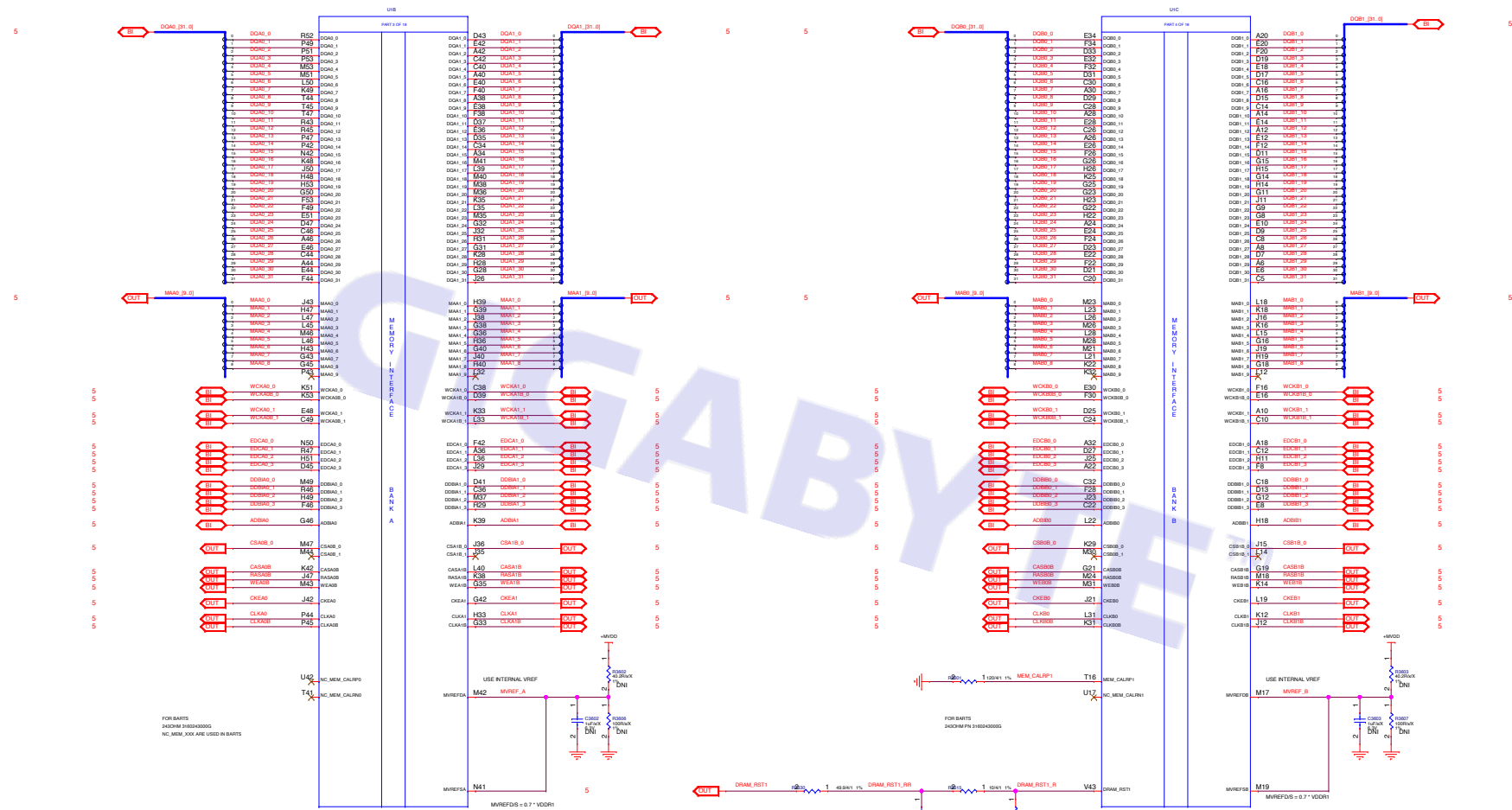
(1) PCI-EXPRESS EDGE CONNECTOR



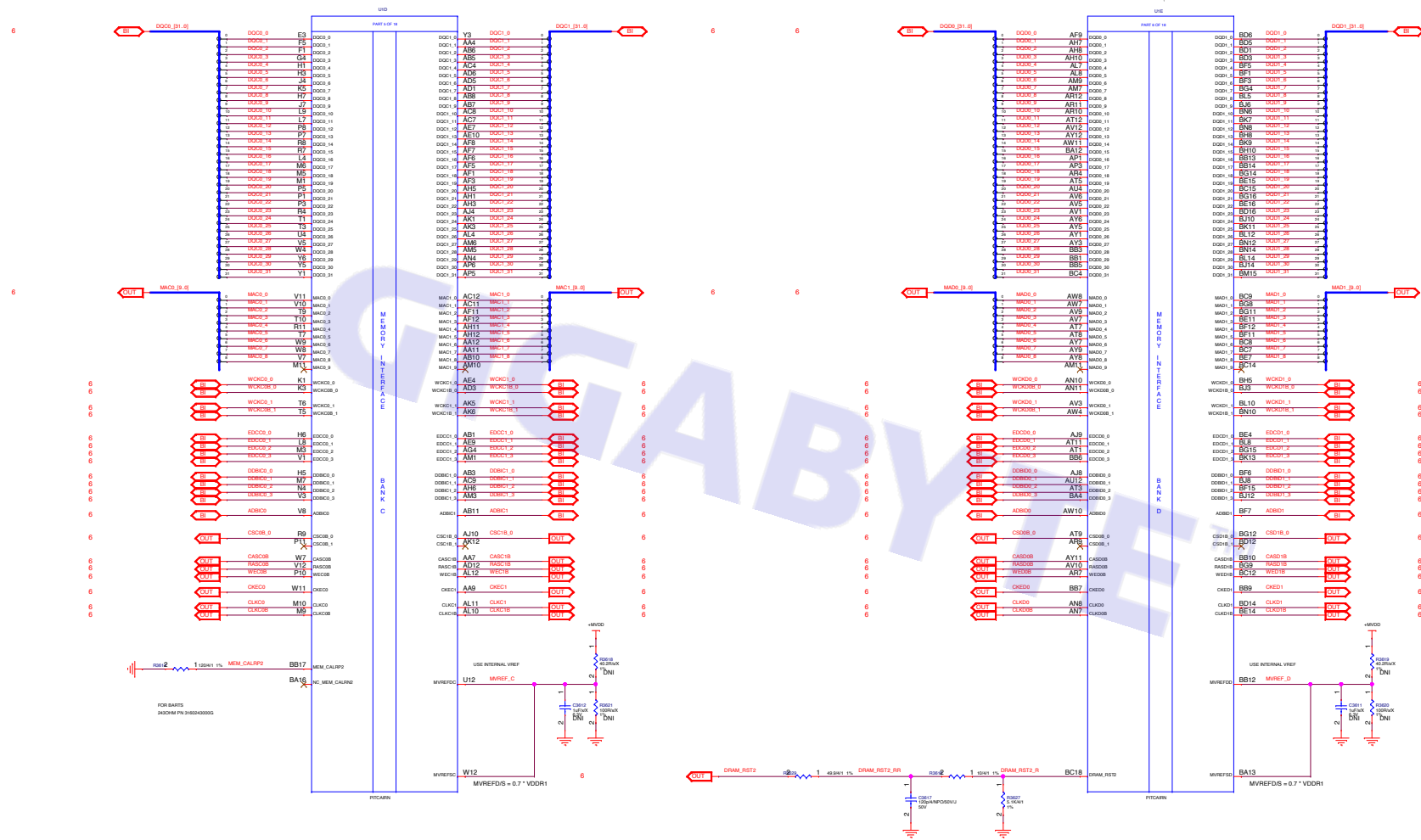
(2) CURACAO PCIE INTERFACE



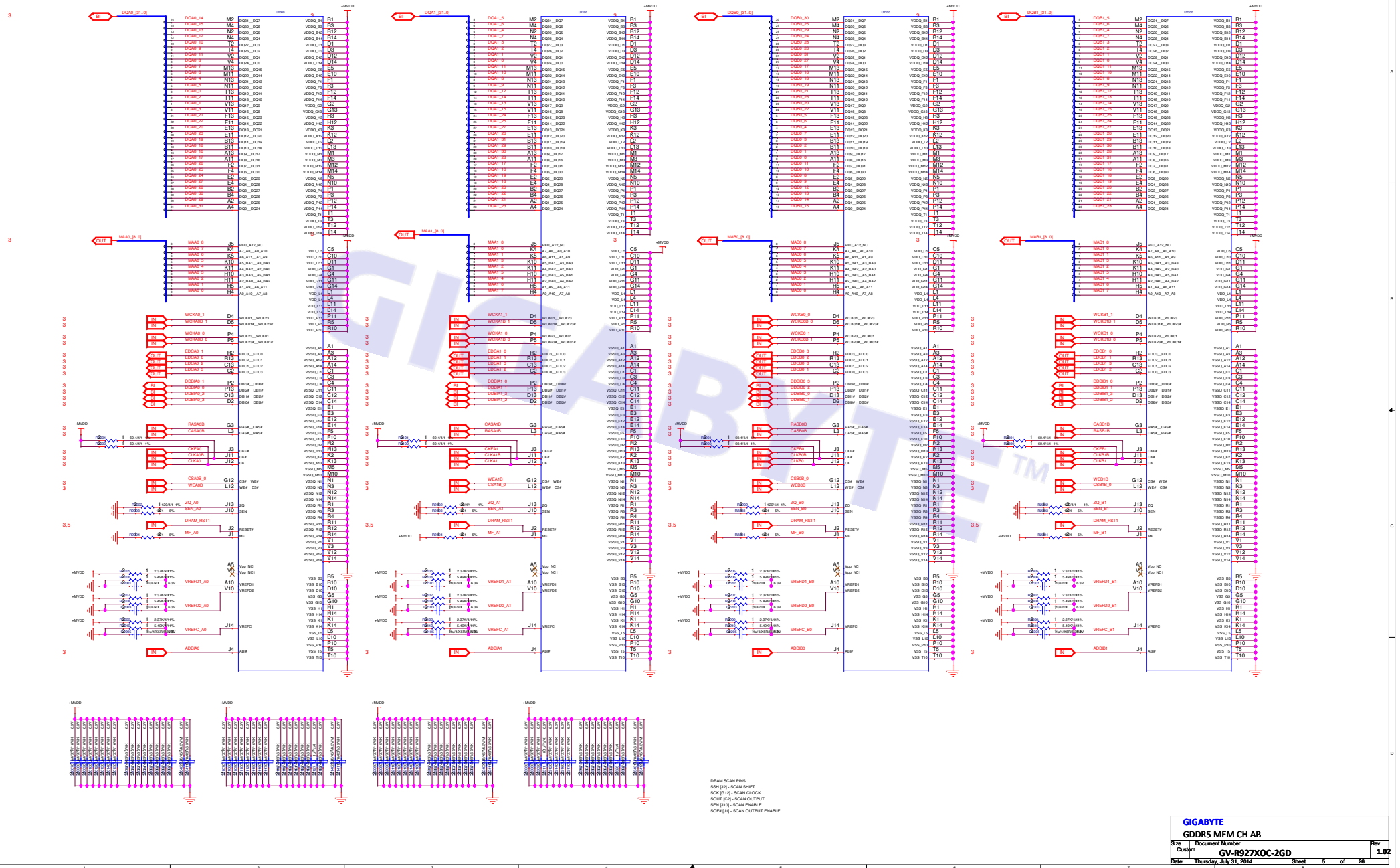
(3) CURACAO MEM INTERFACE CH AB

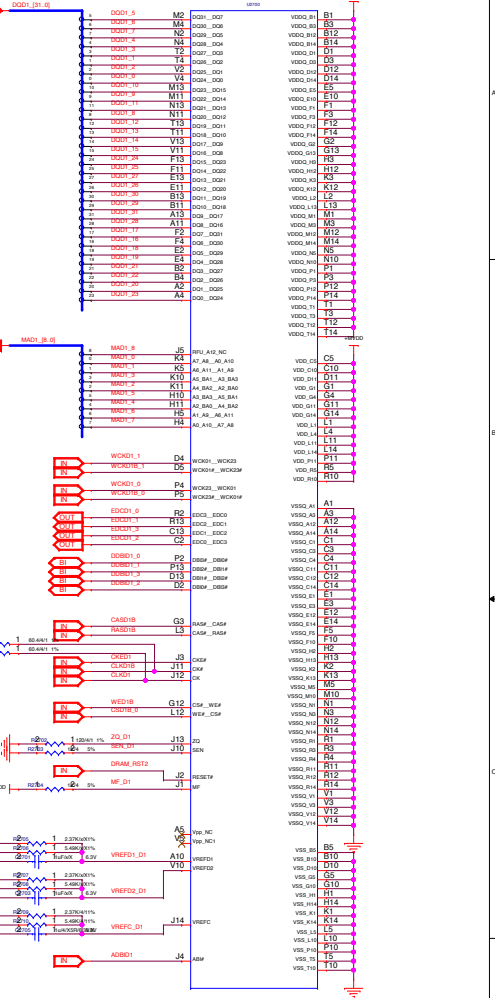
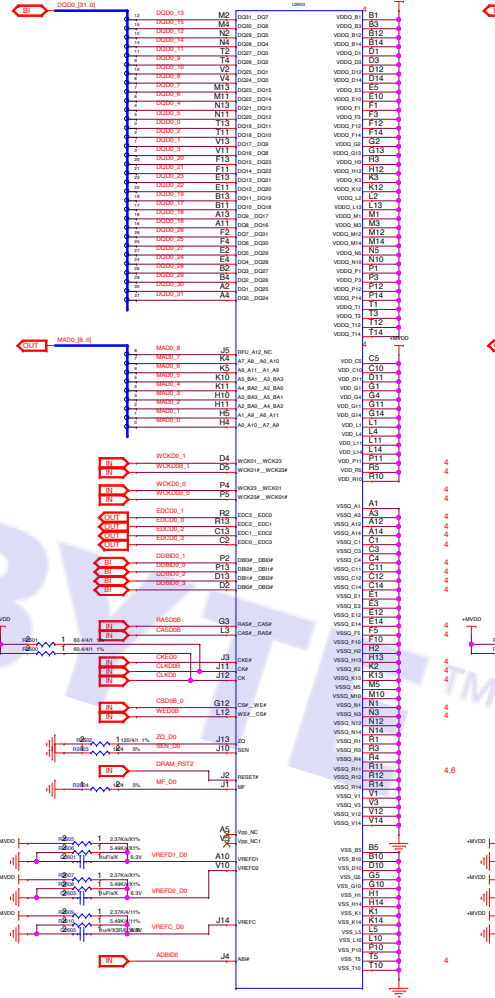
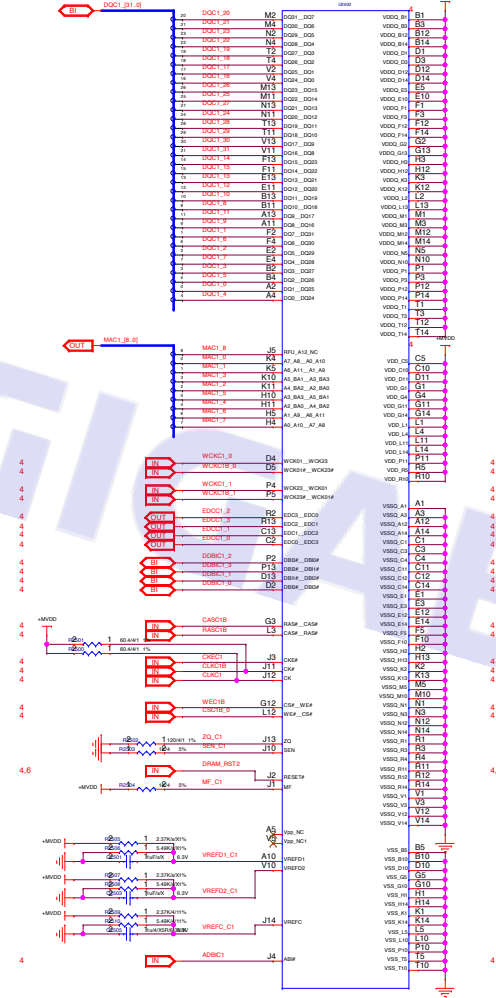


(4) CURACAO MEM INTERFACE CH CD



(5) GDDR5 MEM CH AB



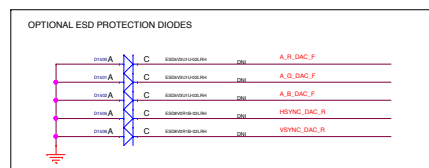
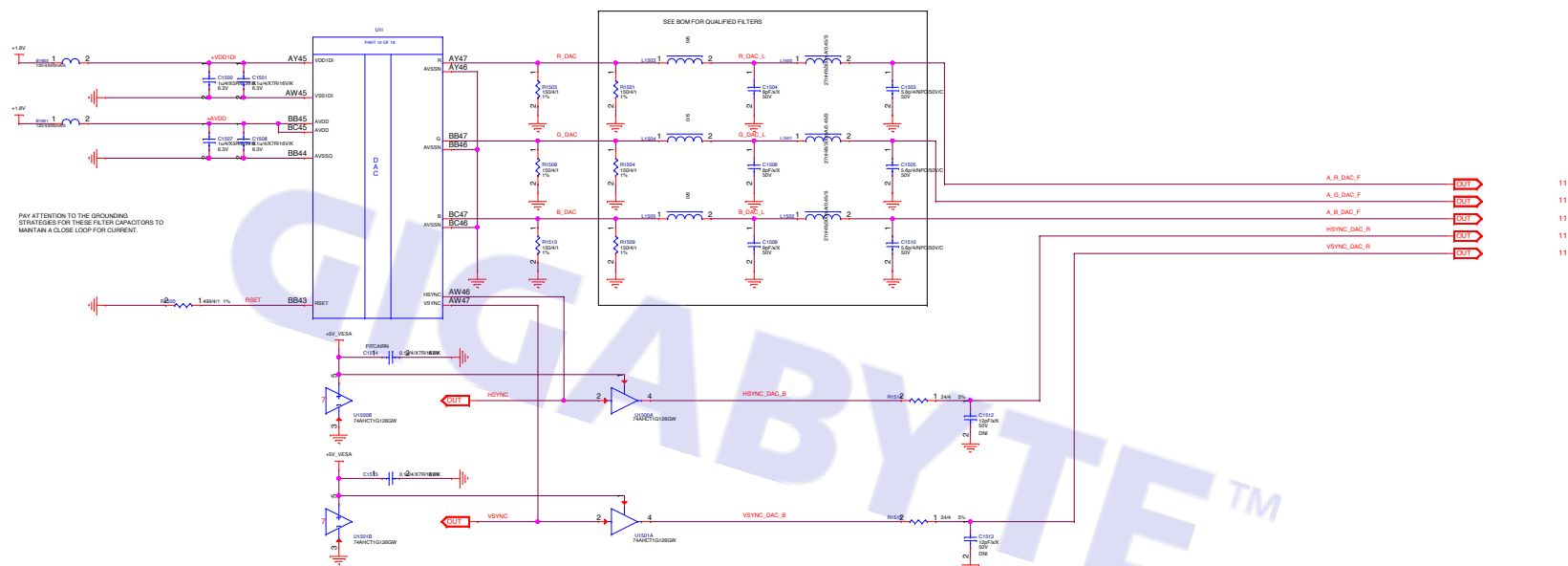
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1.02

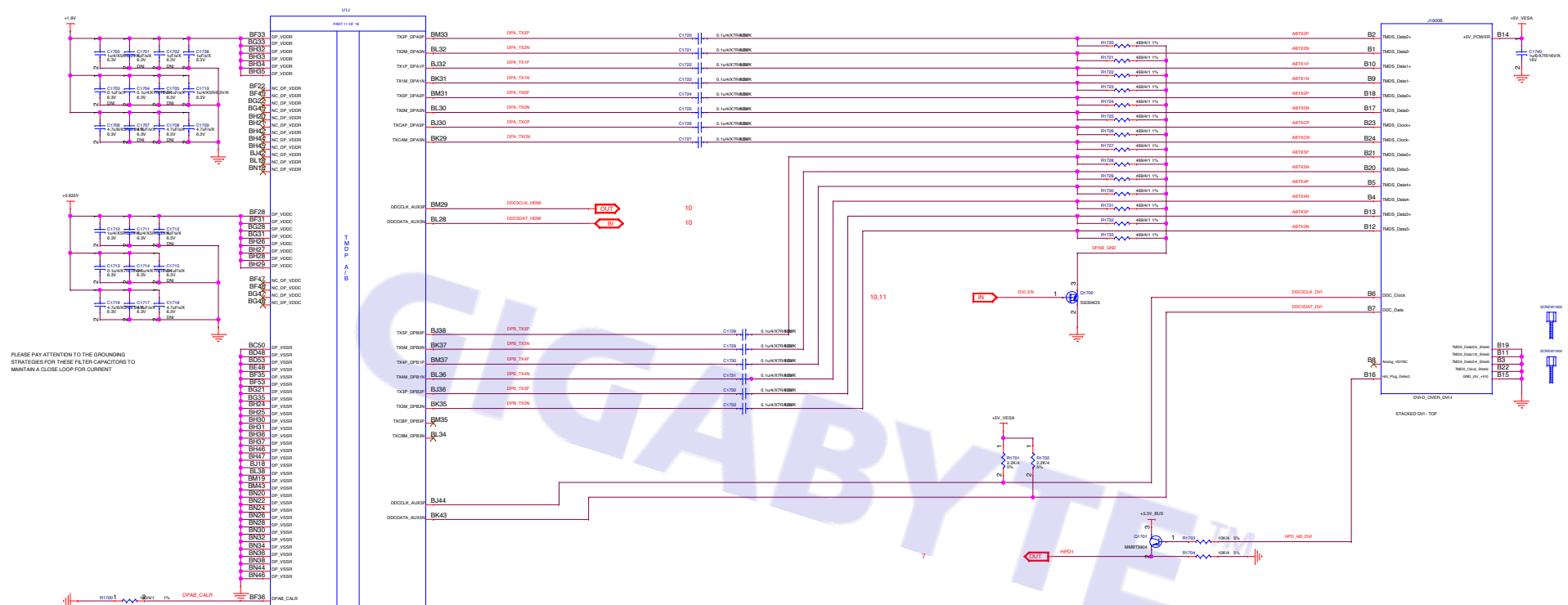
MLPS STRAPS FOR FITCARN



(8) CURACAO DAC



(9) CURACAO TMDPAB sDVI

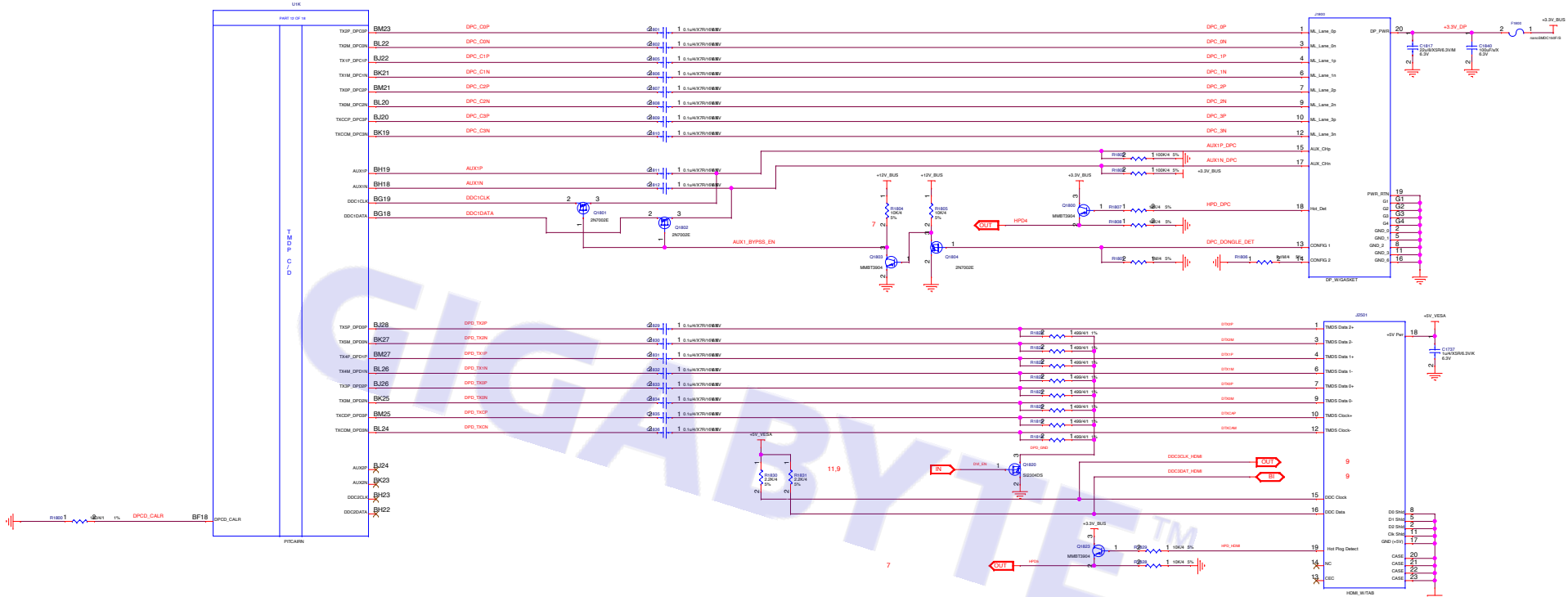


OPTIONAL ESD PROTECTION DIODES

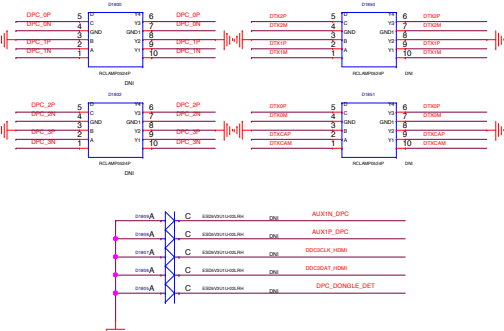


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SHEET: CURACAO PTCAPM TMDPAB DEV1 TOP		DATE: Wed Jul 17 02:26:13 2013		REV: 1.0	
SHEET NUMBER: 9 OF 26		TITLE:		<TITLE>	
DOCUMENT NUMBER: GV-P827XOC-050					

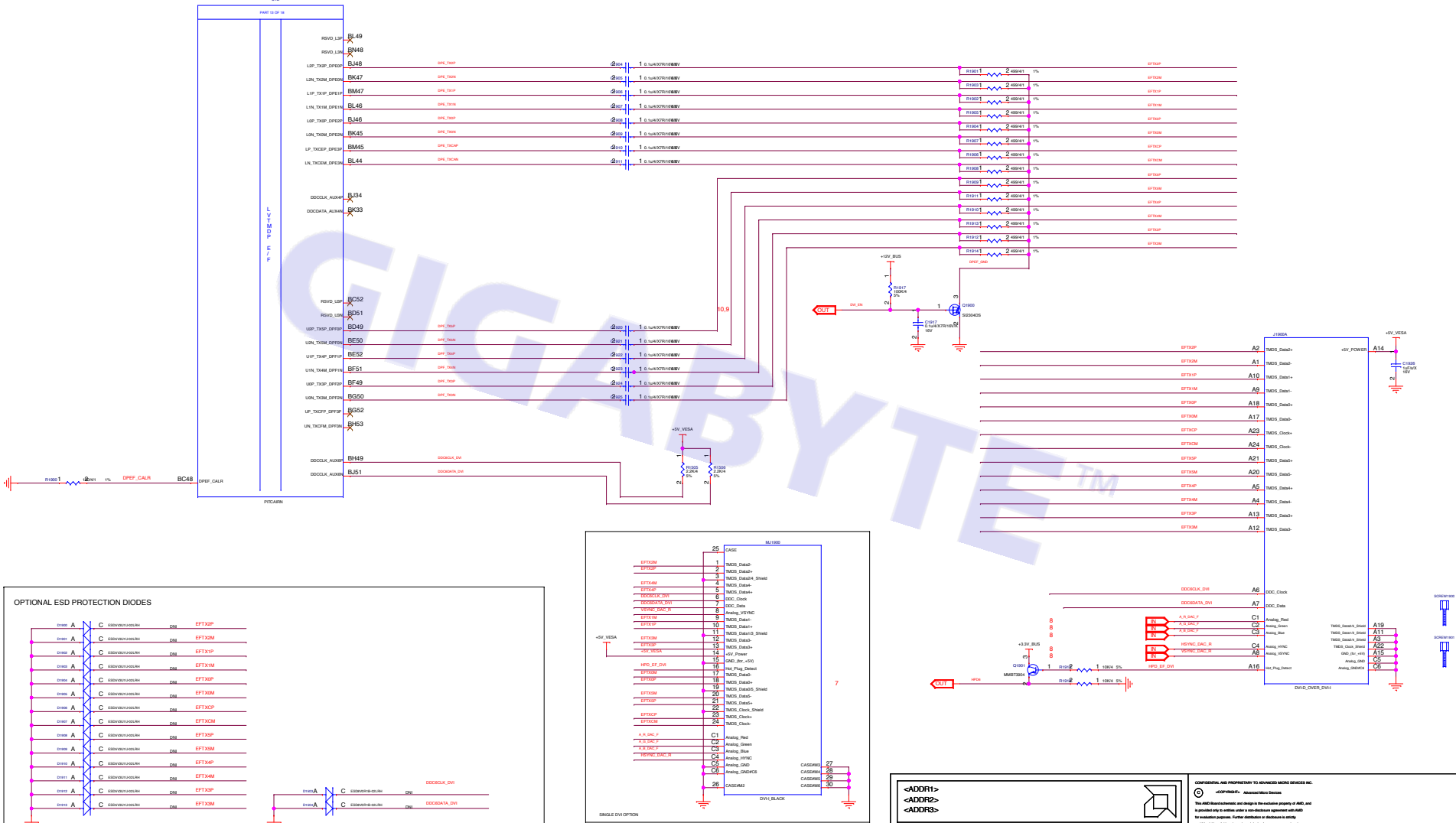
(10) CURACAO TMDPCD DP HDMI





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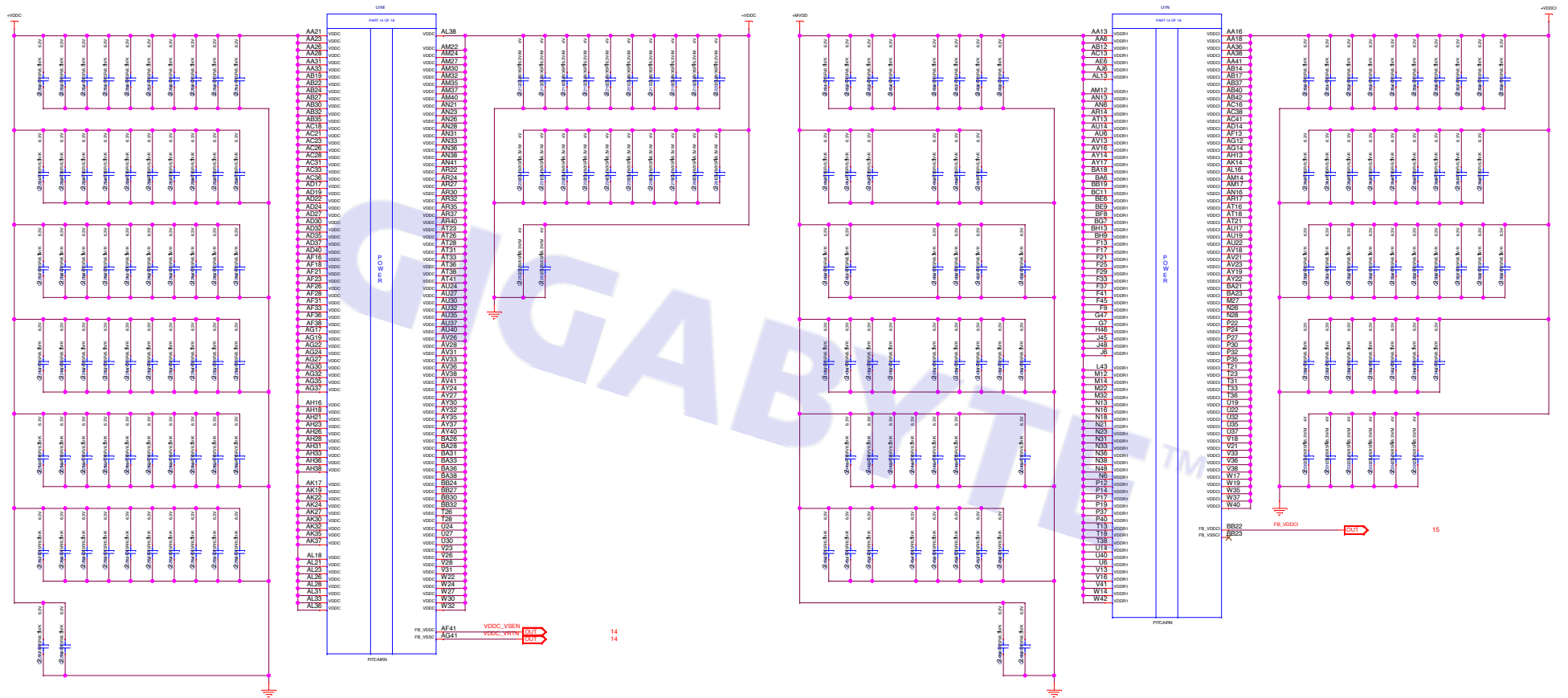
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(11) CURACAO LVTMDPEF dDVI



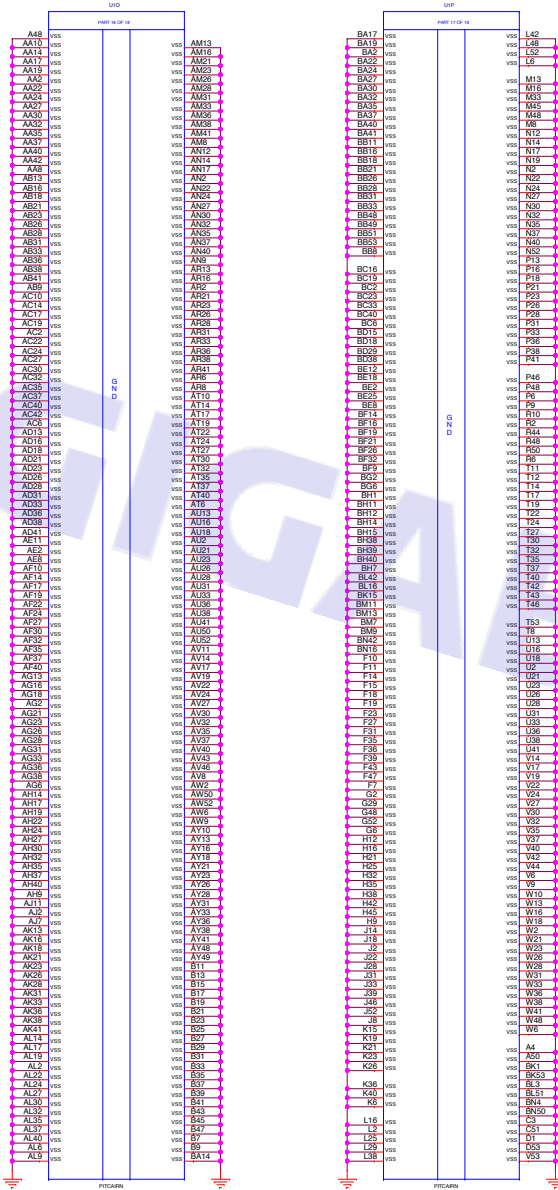
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DATE: Wed Jul 27 02:26:14 2013		REV: 1.0		<TITLE>	
SHEET NUMBER: 11 OF 26		<TITLE>			
DOCUMENT NUMBER: GV-FR27XOC-20D					



(12) CURACAO POWER



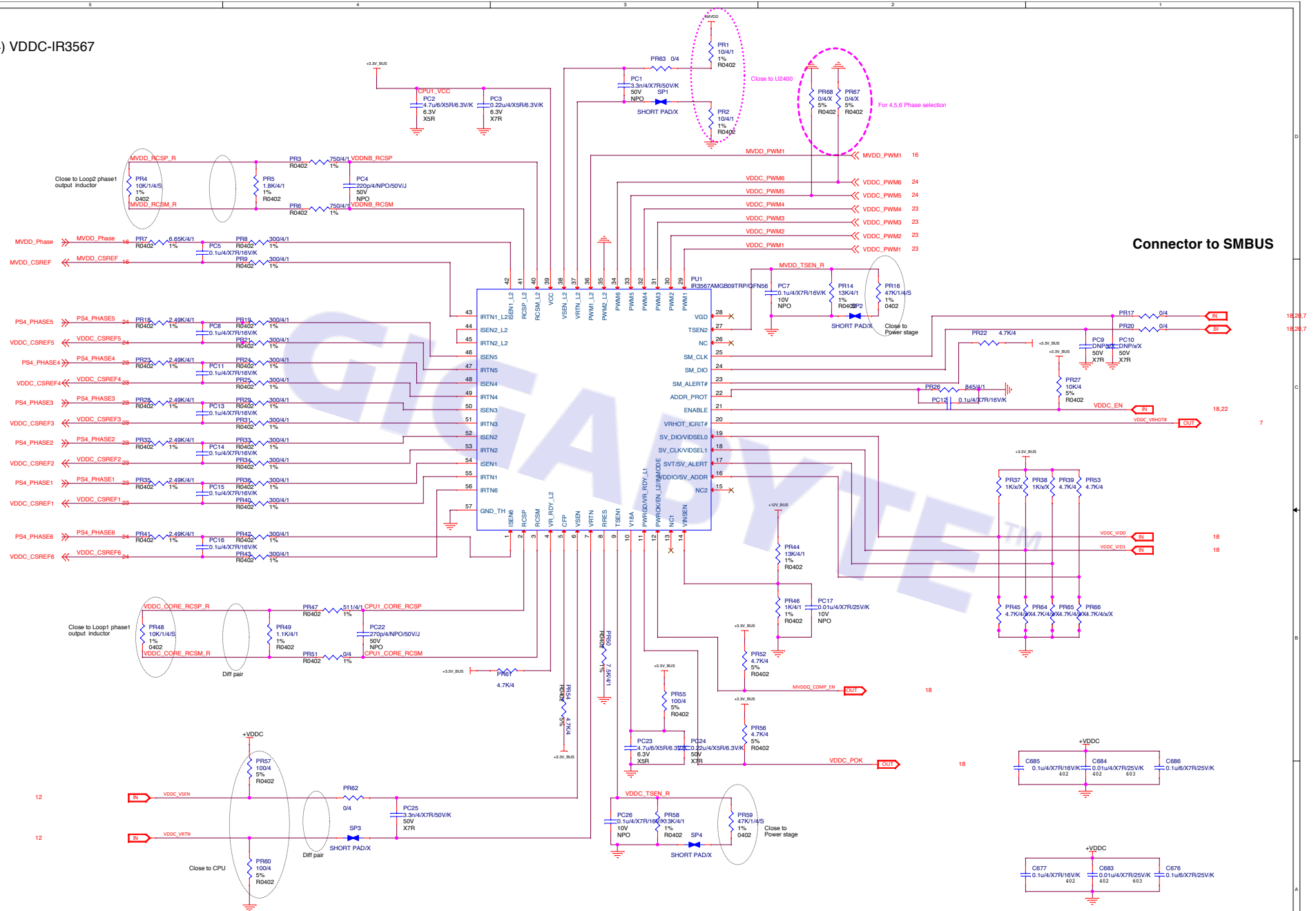
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<p>SHEET NUMBER: 12 OF 26</p>		<p>REV: 1.0</p>	
<p>DOCUMENT NUMBER: GV-R827XOC-2GD</p>		<p>TITLE: <TITLE></p>	

(13) CURACAO GND

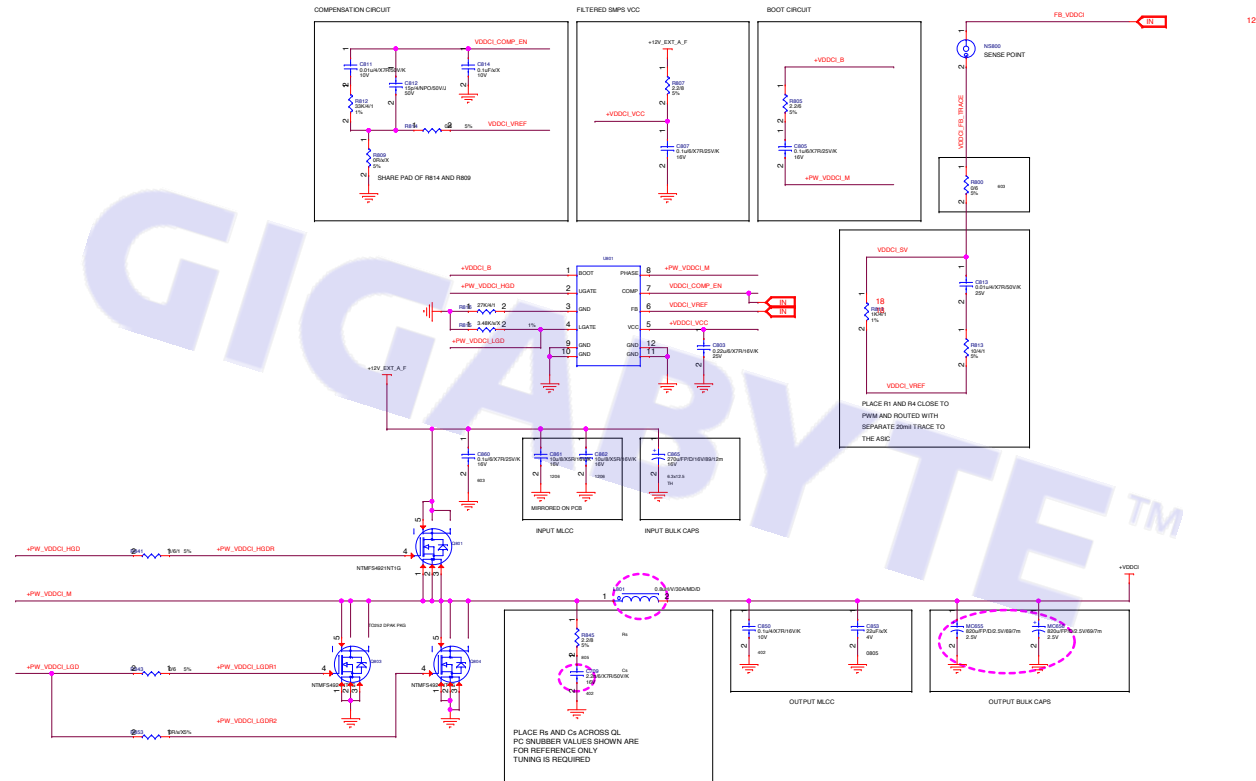


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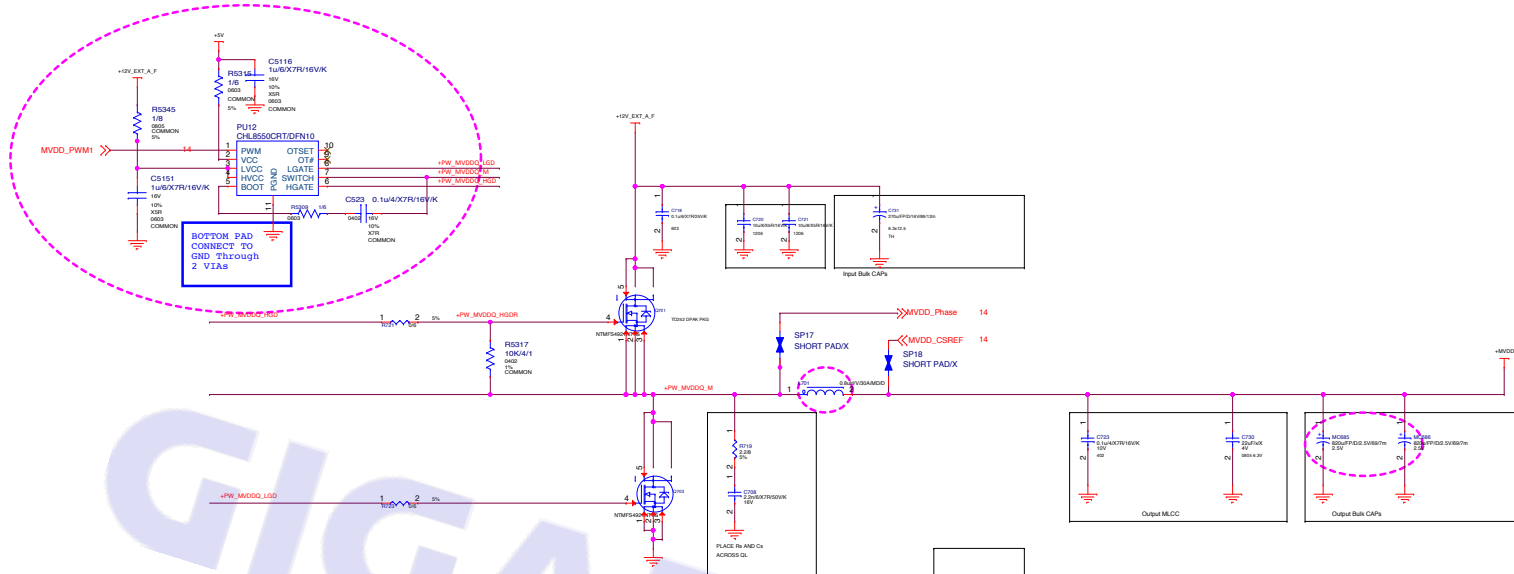
(14) VDDC-IR3567



(15) VDDCI



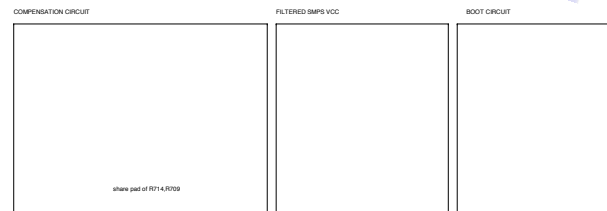
(16) MVDD



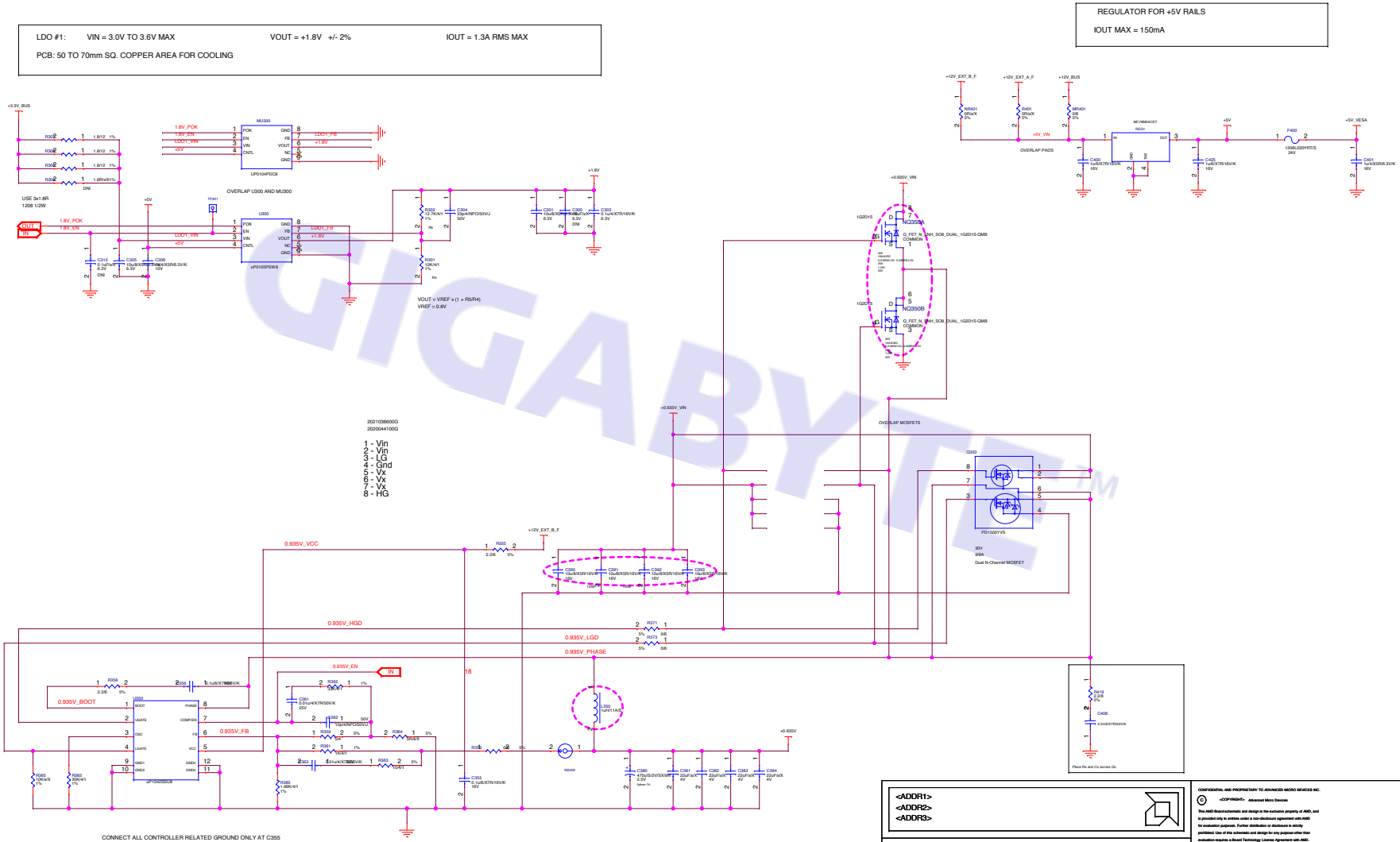
LAYOUT GUIDELINE


1. POSITION THE CONTROLLER (C702) SUCH THAT LGATE (P146) IS THE CLOSEST TO THE GATE OF THE MOSFETS. YOU CAN PLACE THE GATE RESISTORS R721 AND R722 NEXT TO THE GATE OF THE MOSFETS. MAKE THE GATE DRIVE TRACES (PW_MVDDQ_LGDNQ2) AS SHORT AS POSSIBLE TO REDUCE THE TRACE INDUCTANCE.
2. PLACE THE BYPASS CAPACITORS FOR VCC (C703) AS WELL AS BOOST CAPS (C705) AS CLOSE TO THE CONTROLLER AS POSSIBLE.
3. VOLTAGE AMPLIFIER COMPENSATION NETWORK: PLACE R714 CLOSE TO THE PIN 7.
4. PLACE THE REST OF THE COMPENSATION NETWORK (R716, R711, R712, R713, C711, C712 AND C713) CLOSE TO THE PINS 7 AND 8.

PLACE R1 AND R4
CLOSE TO PWM AND
ROUTE WITH
SEPARATE 20mil TRACE

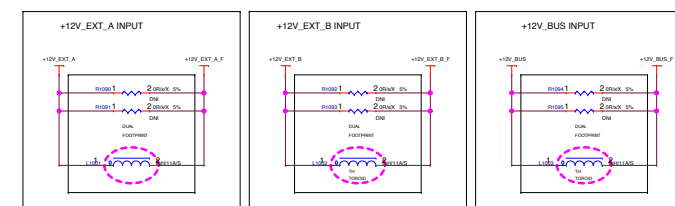
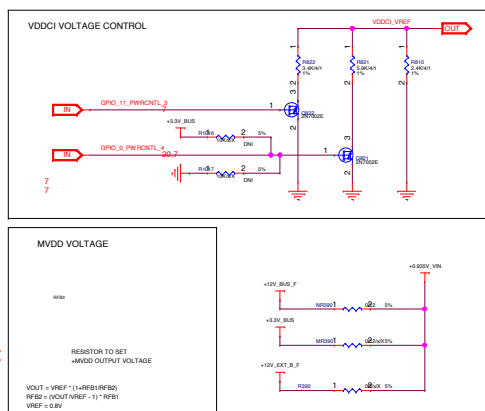
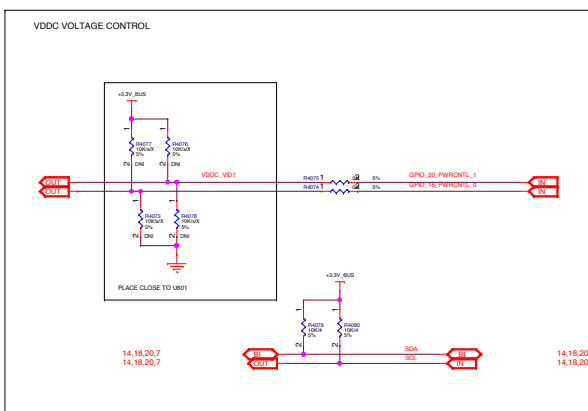
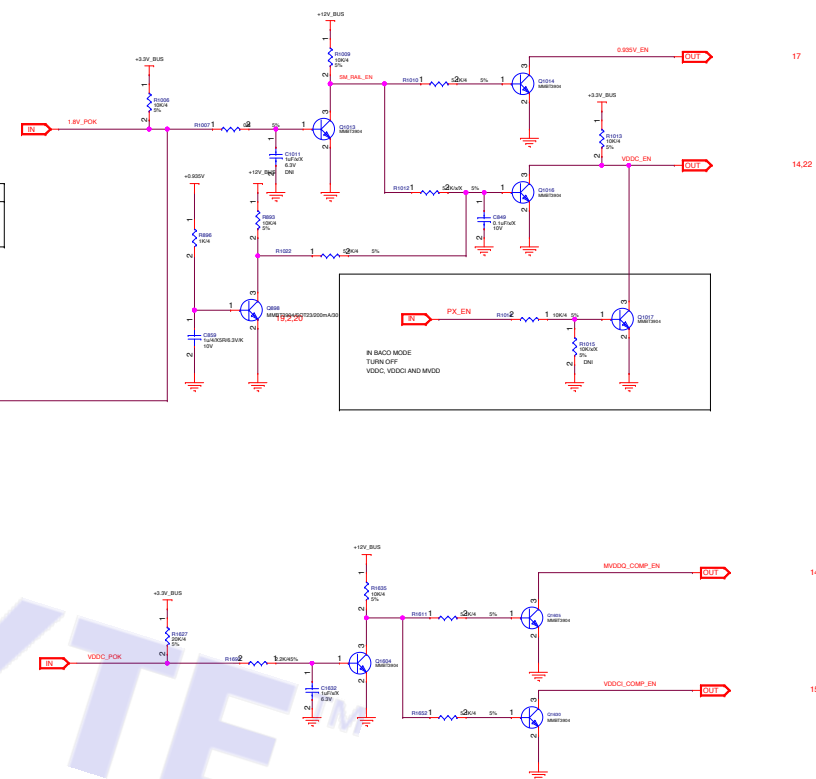
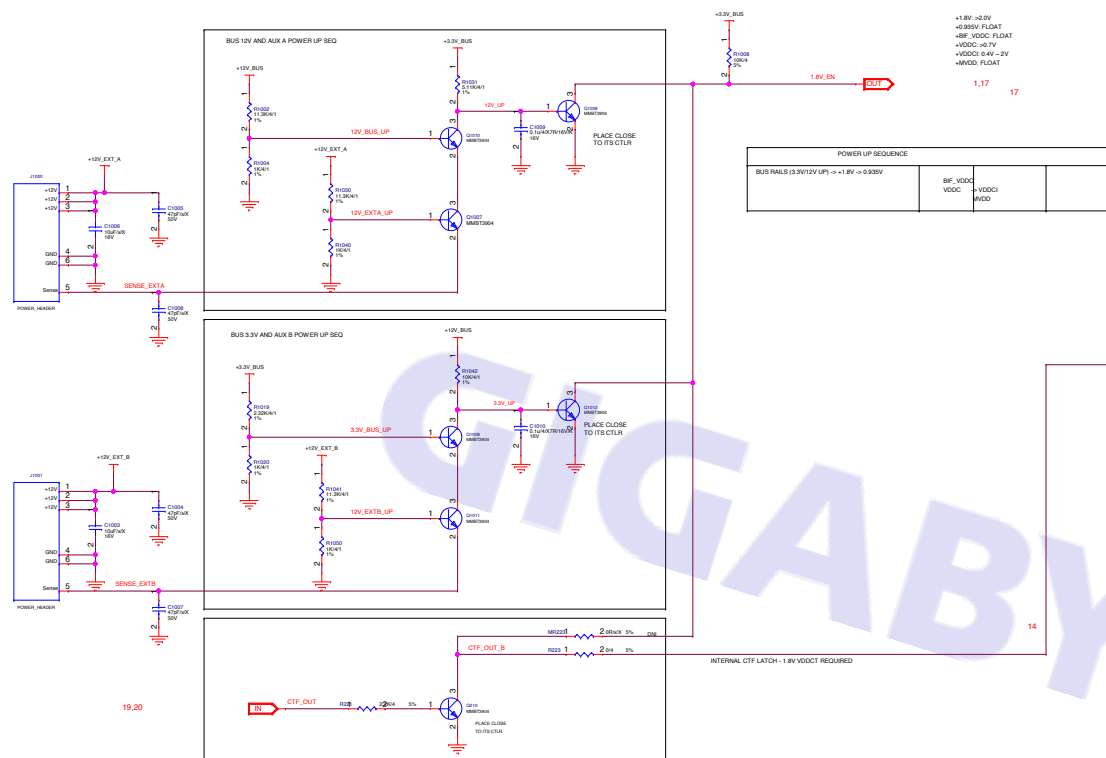



(17) SMALL RAIL REGULATOR



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<p>SHEET: 00001 Rev. 0000000000</p>		<p>DATE: Wed Jul 02 20:26:16 2013</p>		<p>REV: 1.0</p>	
<p>SHEET NUMBER: 17 OF 26</p>		<p>TITLE:</p>			
<p>DOCUMENT NUMBER: GV-9827X0C-050</p>		<p><TITLE></p>			

(18) POWER MANAGEMENT

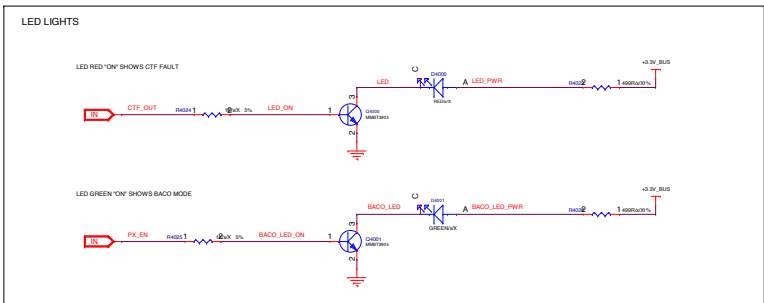
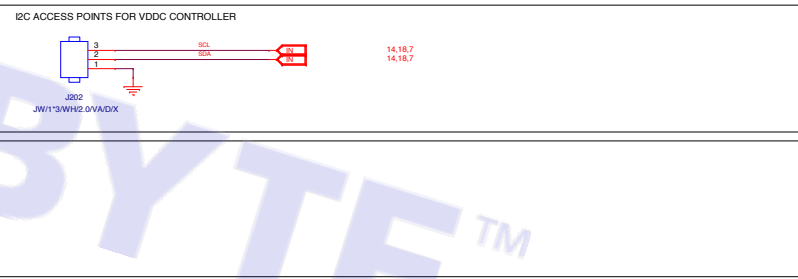
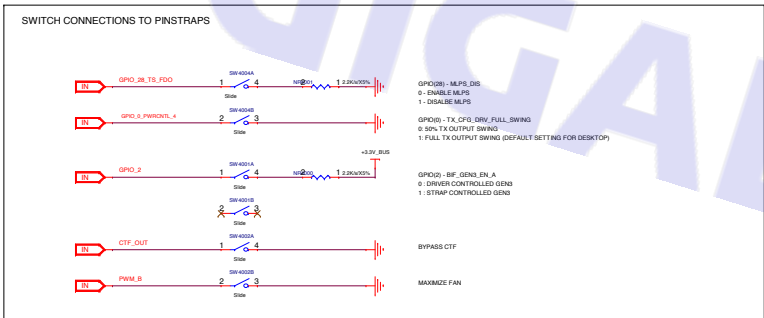
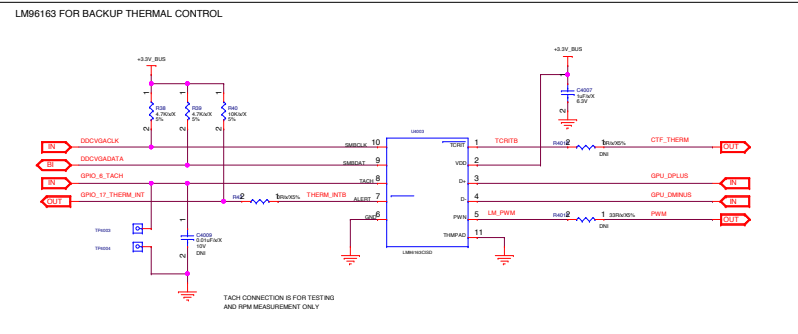
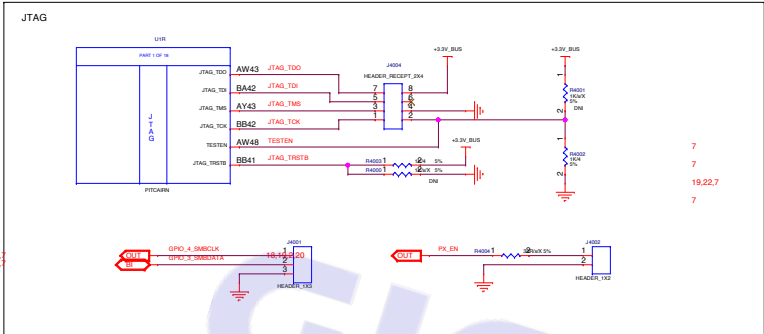


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DATE: Wed Jul 17 02:26:16 2013		REV: 1.0			
SHEET NUMBER: 18		OF 26		TITLE:	
DOCUMENT NUMBER: GV-R827XOC-23D				<TITLE>	

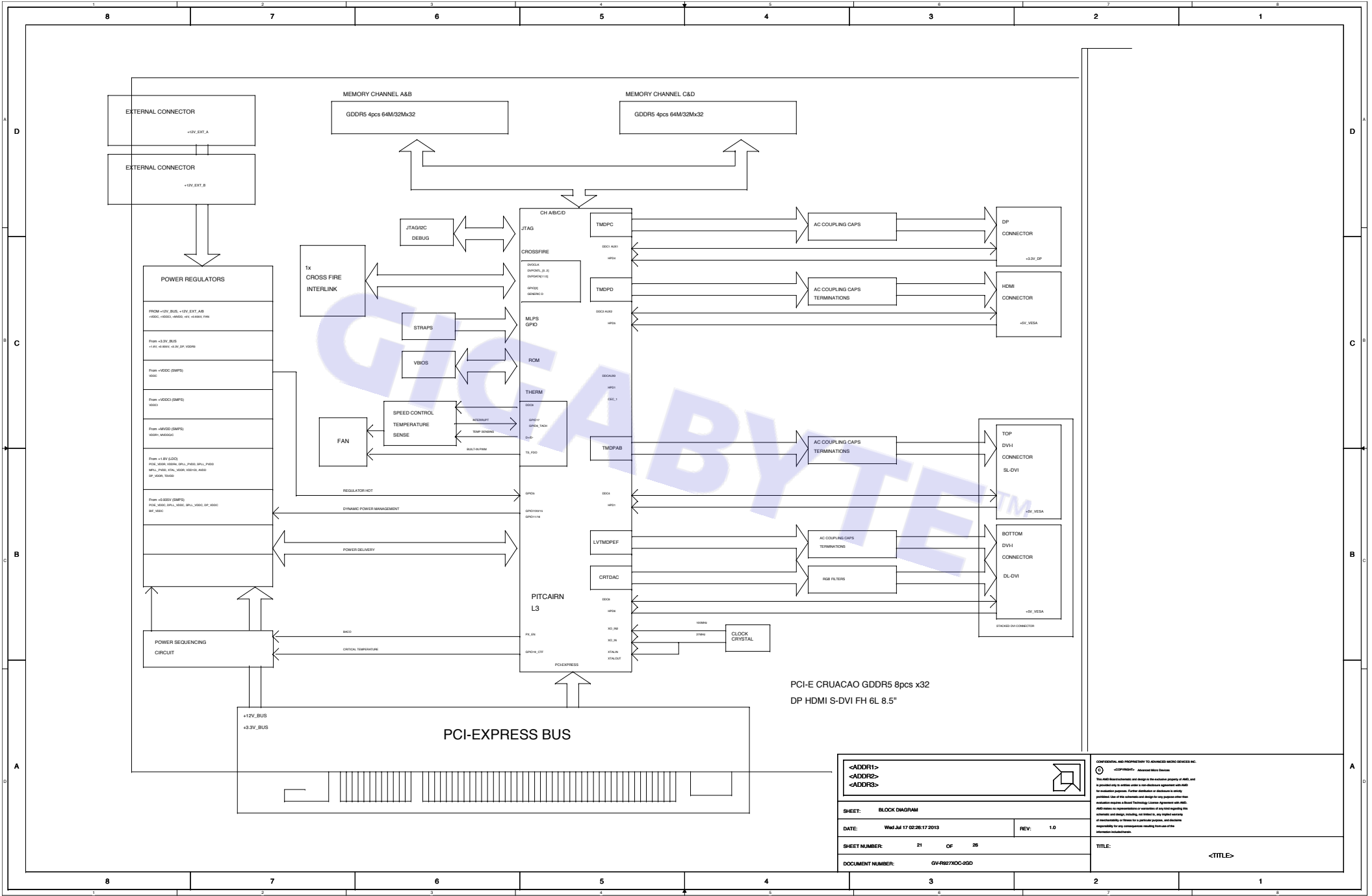
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(20) DEBUG CIRCUIT

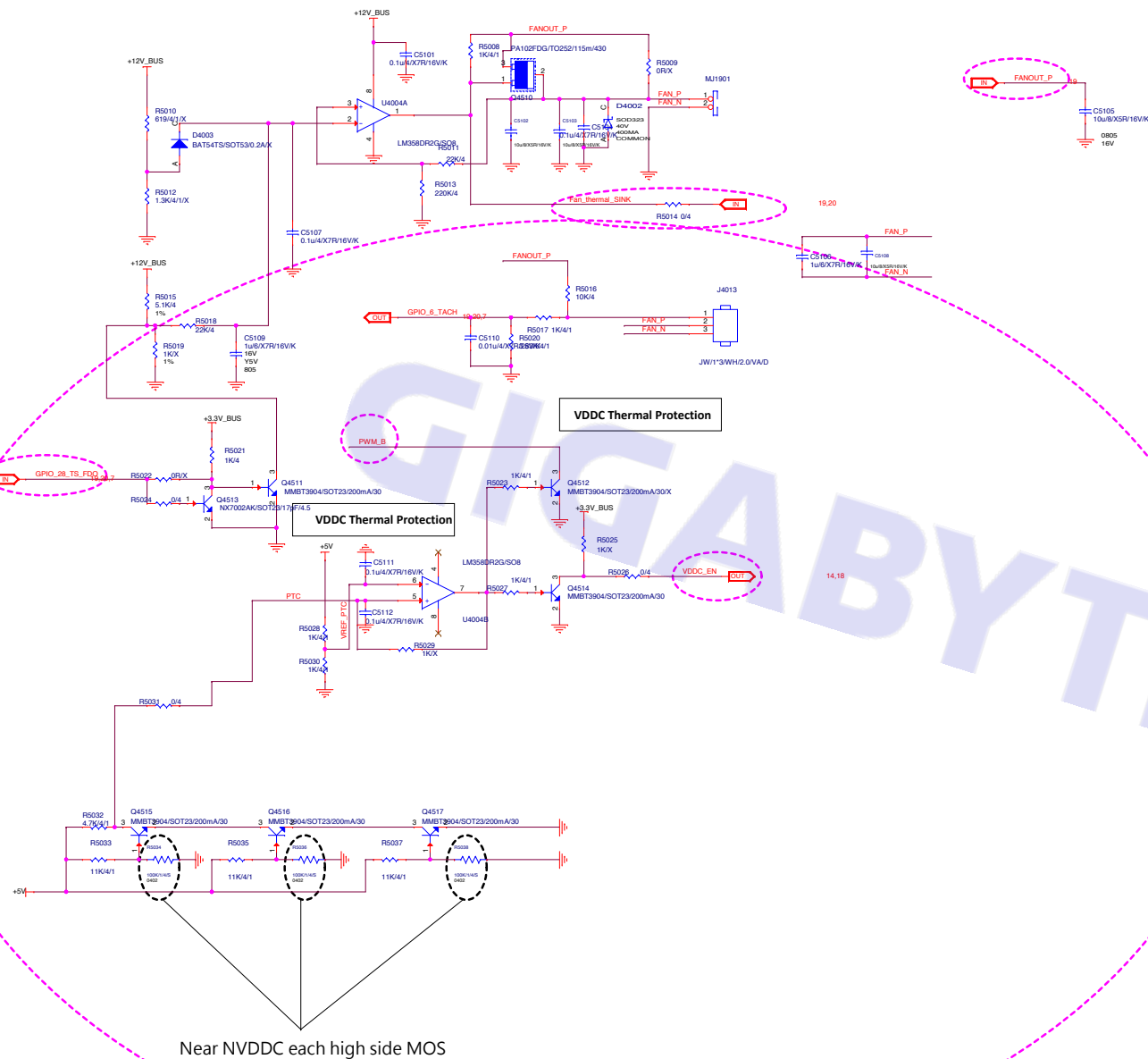


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<p>SHEET: 20 OF 20</p>		<p>DATE: Wed Jul 17 02:26:17 2013</p>	
<p>SHEET NUMBER: 20 OF 20</p>		<p>REV: 1.0</p>	
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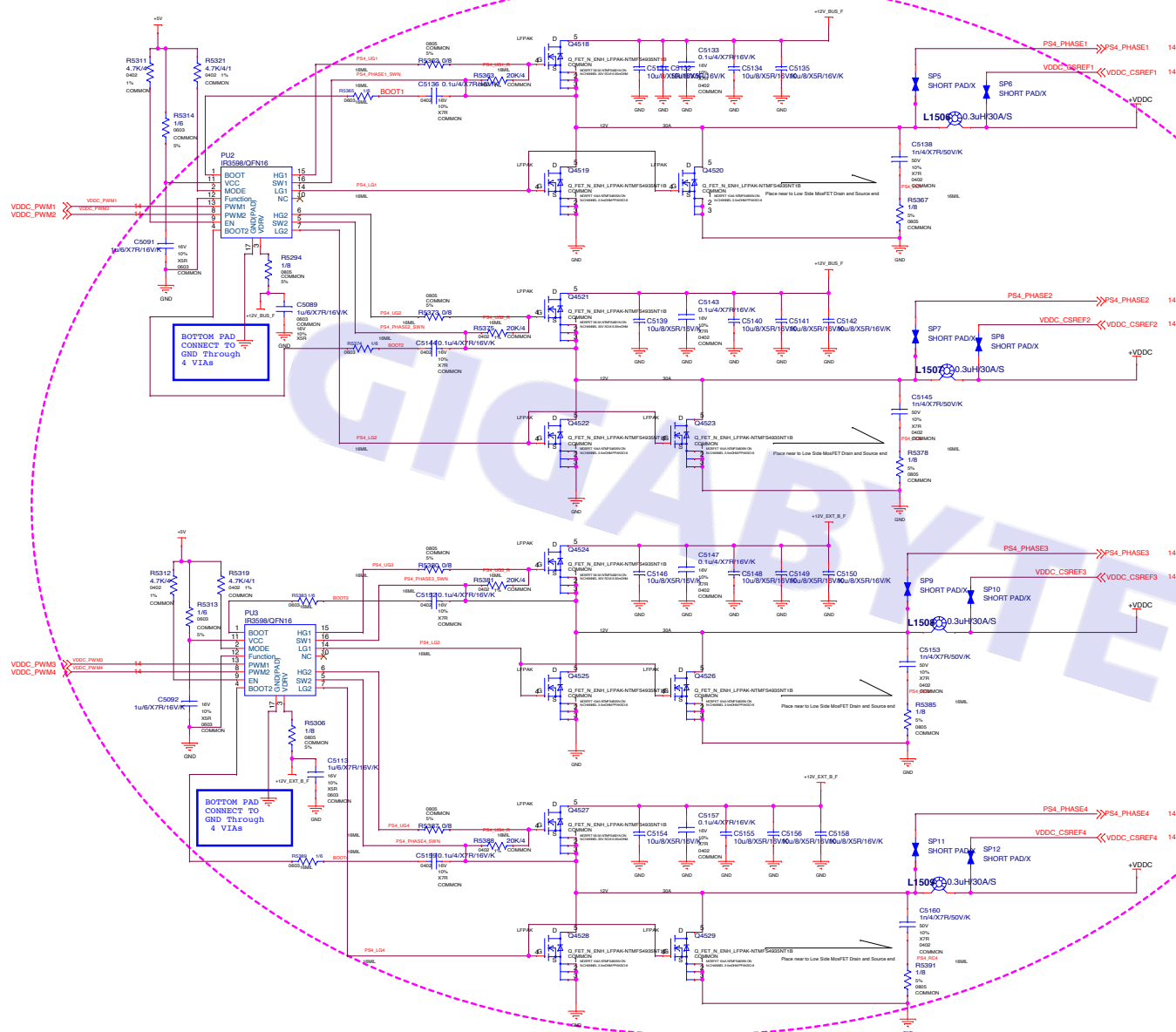
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DATE: Wed Jul 17 02:26:17 2013		REV: 1.0	
SHEET NUMBER: 21 OF 26			
DOCUMENT NUMBER: GV-R927XOC-2GD			

(22) 3 Pin Fan Control

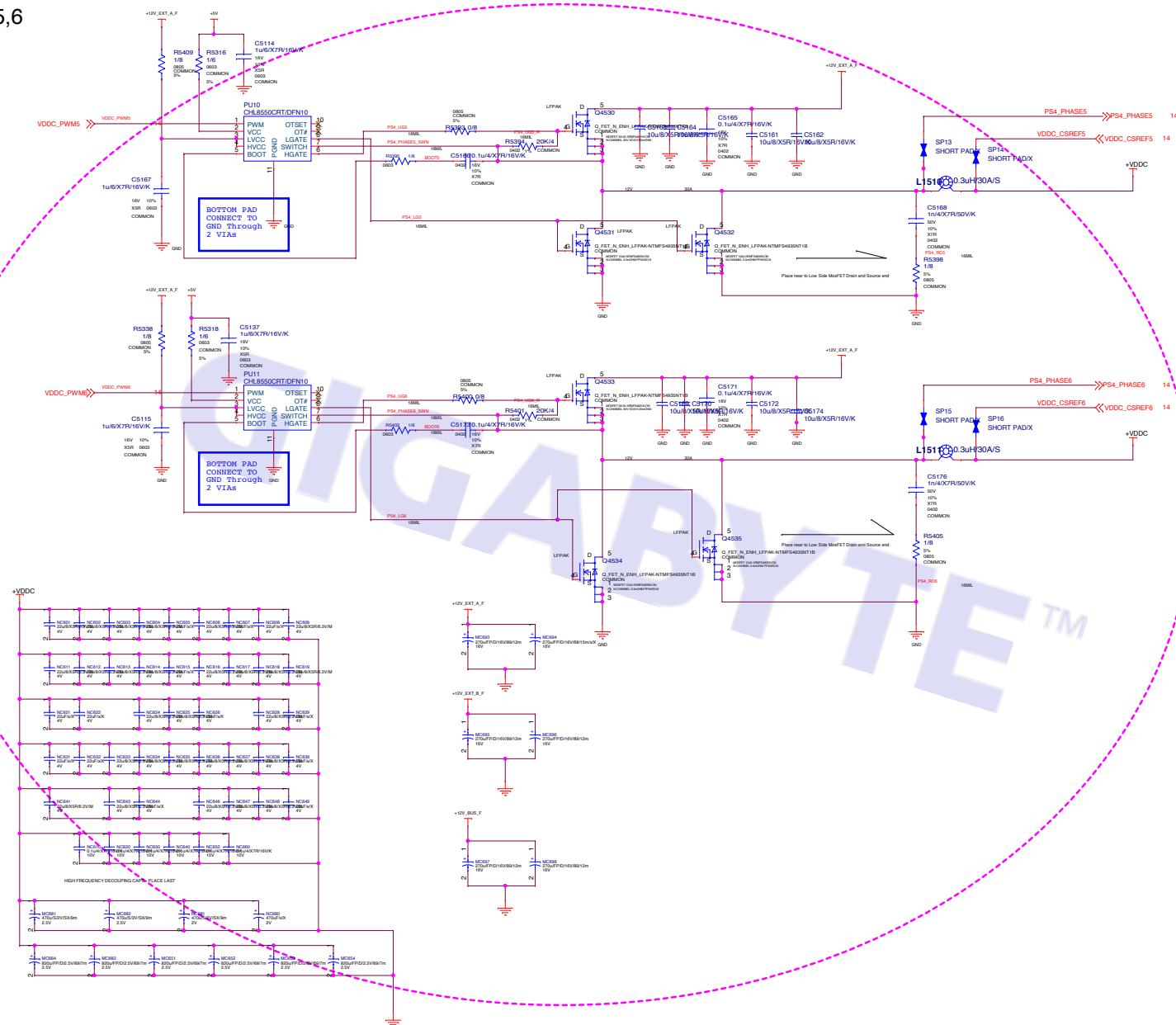


Near NVDDC each high side MOS

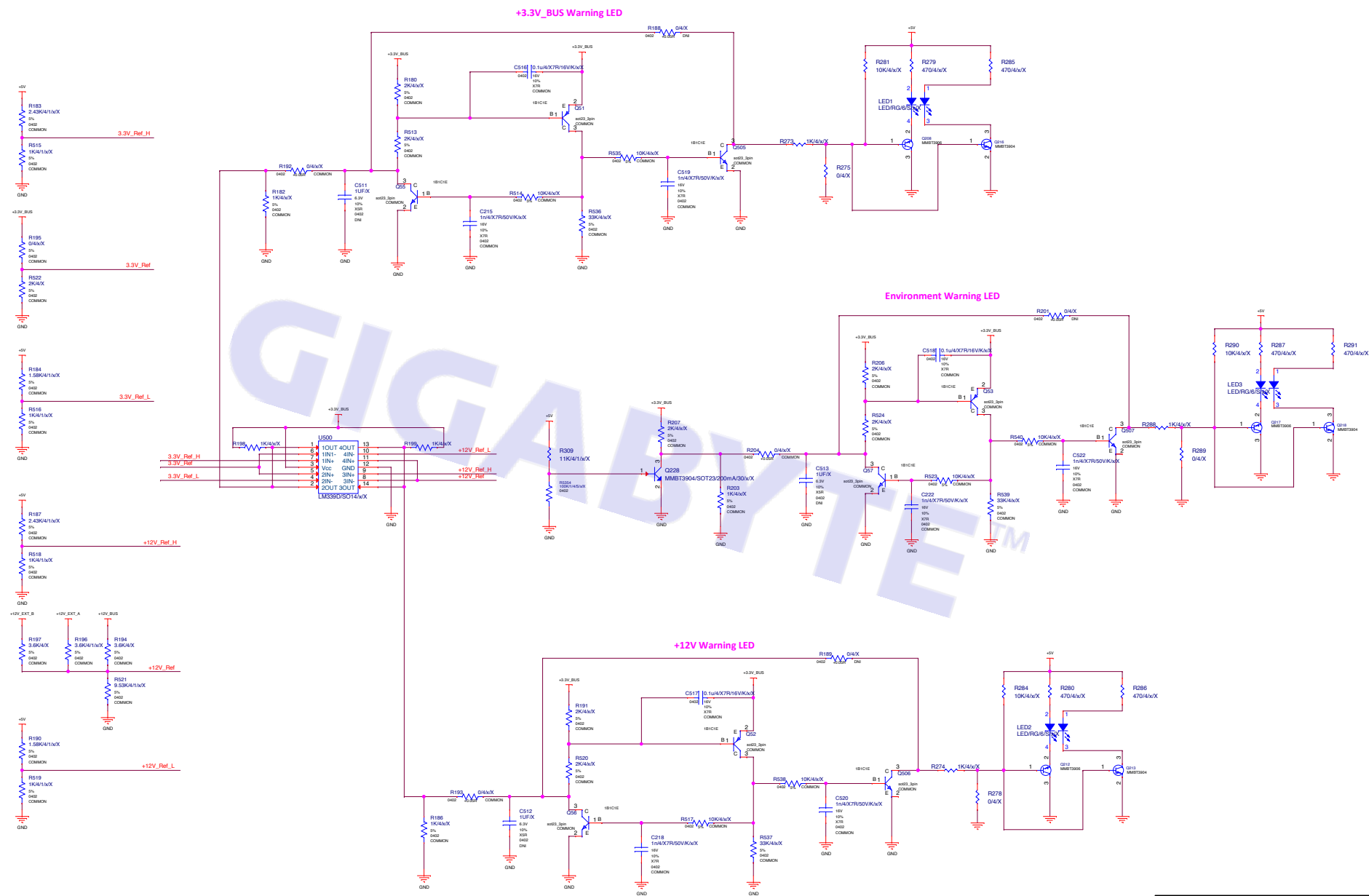
(23) VDDC Phase 1,2,3,4



(24) VDDC Phase 5.6



(25) Warning LED



AMD

TITLE:

<TITLE>

DOCUMENT NUMBER:

105_CR81XOC_000

DATE:

Wed Jul 17 02:26:17 2013

SHEET NUMBER:

22

OF

23

REV:

<REV>

REVISION HISTORY

ENGINEER:

<ENGINEER>

NOTES:

NOTE

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SCH Rev	PCB Rev	Date	REVISION DESCRIPTION
0	000	06/20/13	INITIAL SCHEMATIC BASED ON CASE
1	000	06/20/13	ADD POWER CON. LDR
1	000	06/20/13	REMOVE L1700 - L1703
			REMOVE RE pin for SP_VDDPWR_VDDC
000	000001		update power sequence to make 0.05V power up before vddc

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REVISION HISTORY

Size	Document Number	Rev
Custom	GV-R927XOC-2GD	1.00
Date	Thursday, July 31, 2014	Sheet 26 of 26