PCI-EXPRESS EDGE CONNECTOR

x16 PCIe

Mechanical Key

MPCIE1

Connector left side (B pins):
+12V#B1, +12V#B2, +12V#B3, GND#B4, SMCLK, SMDAT, GND#B7, +3.3V#B8, JTAG1, 3.3Vaux, WAKE#, RSVD#B12, GND#B13, PETp0, PETn0, GND#B16, PRSNT2#B17, GND#B18, PETp1, PETn1, GND#B21, PETp2, PETn2, GND#B24, PETp3, PETn3, GND#B27, RSVD#B30, PRSNT2#B31, GND#B32, PETp4, PETn4, GND#B35, PETp5, PETn5, GND#B39, PETp6, PETn6, GND#B43, PETp7, PETn7, GND#B47, PRSNT2#B48, GND#B49, PETp8, PETn8, GND#B53, PETp9, PETn9, GND#B56, PETp10, PETn10, GND#B60, PETp11, PETn11, GND#B64, PETp12, PETn12, GND#B68, PETp13, PETn13, GND#B72, PETp14, PETn14, GND#B77, PETp15, PETn15, GND#B80, PRSNT2#B81, RSVD#B82

Connector right side (A pins):
PRSNT1#A1, +12V#A2, +12V#A3, GND#A4, JTAG2, JTAG3, JTAG4, JTAG5, +3.3V#A9, +3.3V#A10, PERST#, GND#A12, REFCLK+, REFCLK-, GND#A15, PERp0, PERn0, GND#A18, RSVD#A19, GND#A20, PERp1, PERn1, GND#A23, PERp2, PERn2, GND#A26, PERp3, PERn3, GND#A28, RSVD#A32, GND#A33, PERp4, PERn4, GND#A37, PERp5, PERn5, GND#A41, PERp6, PERn6, GND#A45, PERp7, PERn7, GND#A49, RSVD#A50, PERp8, PERn8, GND#A54, PERp9, PERn9, GND#A58, PERp10, PERn10, GND#A62, PERp11, PERn11, GND#A66, PERp12, PERn12, GND#A70, PERp13, PERn13, GND#A74, PERp14, PERn14, GND#A78, PERp15, PERn15, GND#A82

Signal labels (left):
(2) PETp0_GFXRp0 / PETn0_GFXRn0
(2) PETp1_GFXRp1 / PETn1_GFXRn1
(2) PETp2_GFXRp2 / PETn2_GFXRn2
(2) PETp3_GFXRp3 / PETn3_GFXRn3
(2) PETp4_GFXRp4 / PETn4_GFXRn4
(2) PETp5_GFXRp5 / PETn5_GFXRn5
(2) PETp6_GFXRp6 / PETn6_GFXRn6
(2) PETp7_GFXRp7 / PETn7_GFXRn7
(2) PETp8_GFXRp8 / PETn8_GFXRn8
(2) PETp9_GFXRp9 / PETn9_GFXRn9
(2) PETp10_GFXRp10 / PETn10_GFXRn10
(2) PETp11_GFXRp11 / PETn11_GFXRn11
(2) PETp12_GFXRp12 / PETn12_GFXRn12
(2) PETp13_GFXRp13 / PETn13_GFXRn13
(2) PETp14_GFXRp14 / PETn14_GFXRn14
(2) PETp15_GFXRp15 / PETn15_GFXRn15

SMCLK, SMDAT
PRESENCE

Signal labels (right):
PRESENCE
JTDI, JTDO
PERST#
PCIE_REFCLKP (2), PCIE_REFCLKN (2)
GFXTp0_PERp0 (2), GFXTn0_PERn0 (2)
GFXTp1_PERp1 (2), GFXTn1_PERn1 (2)
GFXTp2_PERp2 (2), GFXTn2_PERn2 (2)
GFXTp3_PERp3 (2), GFXTn3_PERn3 (2)
GFXTp4_PERp4 (2), GFXTn4_PERn4 (2)
GFXTp5_PERp5 (2), GFXTn5_PERn5 (2)
GFXTp6_PERp6 (2), GFXTn6_PERn6 (2)
GFXTp7_PERp7 (2), GFXTn7_PERn7 (2)
GFXTp8_PERp8 (2), GFXTn8_PERn8 (2)
GFXTp9_PERp9 (2), GFXTn9_PERn9 (2)
GFXTp10_PERp10 (2), GFXTn10_PERn10 (2)
GFXTp11_PERp11 (2), GFXTn11_PERn11 (2)
GFXTp12_PERp12 (2), GFXTn12_PERn12 (2)
GFXTp13_PERp13 (2), GFXTn3_PERn13 (2)
GFXTp14_PERp14 (2), GFXTn14_PERn14 (2)
GFXTp15_PERp15 (2), GFXTn15_PERn15 (2)

Top-left U3 circuit:
+3.3V
R1 4.7K DNI, R2 4.7K DNI
C1 100nF_6.3V
U3 NC7WB66K8X
VCC OE1 / 1B OE2 / 2B 1A / GND 2A
(3) GPIO_4, (3) GPIO_3
R3 0R
+3.3V
C2 100nF_6.3V
0R R4
0R R5
DNI , To Bypass U3

+3.3V_BUS
+12V_BUS

Decoupling groups:
Place at regular intervals between VDDC and MVDD regulator.
+12V_BUS
C90 100nF, C91 100nF, C92 100nF

+12V_BUS
C14 10UF
CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX

+12V_BUS / +12V_BUS
C20 150nF_16V, C21 150nF_16V
LF CAP CER 150NF 10% 16V X7R (0603)

+3.3V_BUS
C27 10uF
CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK

+3.3V_BUS
C33 1uF_6.3V, C34 1uF_6.3V, C35 10nF

Place these caps last, ideally as close to the bus connector as possible

Bottom-left caps:
+12V_BUS
C43 100nF, C44 100nF
+3.3V_BUS C45 100nF_6.3V
+3.3V C46 100nF_6.3V
+VDDC C49 100nF_6.3V
+1.1V C50 100nF_6.3V
+1.8V C51 100nF_6.3V

Right side decoupling caps:
C3 100nF / C4 100nF
C5 100nF / C6 100nF
C7 100nF / C9 100nF
C10 100nF / C11 100nF
C12 100nF / C13 100nF
C15 100nF / C16 100nF
C17 100nF / C18 100nF
C19 100nF / C22 100nF
C23 100nF / C24 100nF
C25 100nF / C26 100nF
C28 100nF / C29 100nF
C30 100nF / C31 100nF
C32 100nF / C36 100nF
C37 100nF / C38 100nF
C39 100nF / C40 100nF
C41 100nF / C42 100nF

Right PERST# circuit:
+3.3V
R68 1K
+3.3V_BUS
C76 100nF_6.3V, R67 2.2K
C8 100nF
(3,13,14) PWR_GOOD
R64 0R
R61 0R
U4 NC7SZ08P5X_NL
PERST#_buf (2,22)

SYMBOL LEGEND
DNI — DO NOT INSTALL
— ACTIVE LOW
DIGITAL GROUND
ANALOG GROUND

NOTE: some of the PCIE testpoints will
be available through on via on traces.

U1A
PART 1 OF 10

PCI-EXPRESS INTERFACE

Left signals	Pin		Right signals	Pin	
(1) PETp0_GFXRp0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	GFXTp0_PERp0 (1)
(1) PETn0_GFXRn0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	GFXTn0_PERn0 (1)
(1) PETp1_GFXRp1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	GFXTp1_PERp1 (1)
(1) PETn1_GFXRn1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	GFXTn1_PERn1 (1)
(1) PETp2_GFXRp2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	GFXTp2_PERp2 (1)
(1) PETn2_GFXRn2	AC31	PCIE_RX2N	PCIE_TX2N	AE26	GFXTn2_PERn2 (1)
(1) PETp3_GFXRp3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	GFXTp3_PERp3 (1)
(1) PETn3_GFXRn3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	GFXTn3_PERn3 (1)
(1) PETp4_GFXRp4	AB30	PCIE_RX4P	PCIE_TX4P	AC25	GFXTp4_PERp4 (1)
(1) PETn4_GFXRn4	AA31	PCIE_RX4N	PCIE_TX4N	AB25	GFXTn4_PERn4 (1)
(1) PETp5_GFXRp5	AA29	PCIE_RX5P	PCIE_TX5P	Y23	GFXTp5_PERp5 (1)
(1) PETn5_GFXRn5	Y28	PCIE_RX5N	PCIE_TX5N	Y24	GFXTn5_PERn5 (1)
(1) PETp6_GFXRp6	Y30	PCIE_RX6P	PCIE_TX6P	AB27	GFXTp6_PERp6 (1)
(1) PETn6_GFXRn6	W31	PCIE_RX6N	PCIE_TX6N	AB26	GFXTn6_PERn6 (1)
(1) PETp7_GFXRp7	W29	PCIE_RX7P	PCIE_TX7P	Y27	GFXTp7_PERp7 (1)
(1) PETn7_GFXRn7	V28	PCIE_RX7N	PCIE_TX7N	Y26	GFXTn7_PERn7 (1)
(1) PETp8_GFXRp8	V30	PCIE_RX8P	PCIE_TX8P	W24	GFXTp8_PERp8 (1)
(1) PETn8_GFXRn8	U31	PCIE_RX8N	PCIE_TX8N	W23	GFXTn8_PERn8 (1)
(1) PETp9_GFXRp9	U29	PCIE_RX9P	PCIE_TX9P	V27	GFXTp9_PERp9 (1)
(1) PETn9_GFXRn9	T28	PCIE_RX9N	PCIE_TX9N	U26	GFXTn9_PERn9 (1)
(1) PETp10_GFXRp10	T30	PCIE_RX10P	PCIE_TX10P	U24	GFXTp10_PERp10 (1)
(1) PETn10_GFXRn10	R31	PCIE_RX10N	PCIE_TX10N	U23	GFXTn10_PERn10 (1)
(1) PETp11_GFXRp11	R29	PCIE_RX11P	PCIE_TX11P	T26	GFXTp11_PERp11 (1)
(1) PETn11_GFXRn11	P28	PCIE_RX11N	PCIE_TX11N	T27	GFXTn11_PERn11 (1)
(1) PETp12_GFXRp12	P30	PCIE_RX12P	PCIE_TX12P	T24	GFXTp12_PERp12 (1)
(1) PETn12_GFXRn12	N31	PCIE_RX12N	PCIE_TX12N	T23	GFXTn12_PERn12 (1)
(1) PETp13_GFXRp13	N29	PCIE_RX13P	PCIE_TX13P	P27	GFXTp13_PERp13 (1)
(1) PETn13_GFXRn13	M28	PCIE_RX13N	PCIE_TX13N	P26	GFXTn13_PERn13 (1)
(1) PETp14_GFXRp14	M30	PCIE_RX14P	PCIE_TX14P	P24	GFXTp14_PERp14 (1)
(1) PETn14_GFXRn14	L31	PCIE_RX14N	PCIE_TX14N	P23	GFXTn14_PERn14 (1)
(1) PETp15_GFXRp15	L29	PCIE_RX15P	PCIE_TX15P	M27	GFXTp15_PERp15 (1)
(1) PETn15_GFXRn15	K30	PCIE_RX15N	PCIE_TX15N	N26	GFXTn15_PERn15 (1)

(1) PCIE_REFCLKP	AK30	PCIE_REFCLKP	PCIE_CALRN	AA22	PCIE_CALRN 2.0K R8 402 +1.1V
(1) PCIE_REFCLKN	AK32	PCIE_REFCLKN	PCIE_CALRP	Y22	PCIE_CALRP 1.27K R9 402

(1,22) PERST#_buf — AL27 PERSTB

RV710 A11 HF MVD FT1 BIN1

Test points: TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28

U1B
PART 2 OF 10

DVP PORT

U1	DVPCLK	
AC7	DVPCNTL_0	
Y2	DVPCNTL_1	
U5	DVPCNTL_2	
AA1	DVPCNTL_MVP_0	
Y4	DVPCNTL_MVP_1	

Y7	DVPDATA_0
V2	DVPDATA_1
Y8	DVPDATA_2
V4	DVPDATA_3
AB7	DVPDATA_4
W1	DVPDATA_5
AB8	DVPDATA_6
W3	DVPDATA_7
AB9	DVPDATA_8
W5	DVPDATA_9
AC6	DVPDATA_10
W6	DVPDATA_11
AD7	DVPDATA_12
AA3	DVPDATA_13
AC5	DVPDATA_14
AA5	DVPDATA_15
AE8	DVPDATA_16
AA6	DVPDATA_17
AE9	DVPDATA_18
AB4	DVPDATA_19
AD9	DVPDATA_20
AB2	DVPDATA_21
AC10	DVPDATA_22
AC5	DVPDATA_23

I/O

U6	GPIO_0	GPIO_0
U10	GPIO_1	GPIO_1
T10	GPIO_2	GPIO_2
U8	GPIO_3_SMBDATA	GPIO_3
U7	GPIO_4_SMBCLK	GPIO_4
T9	GPIO_5_AC_BATT	GPIO_5
T7	GPIO_6_TACH	GPIO_7
P10	GPIO_7_BLON	GPIO8_SO
P4	GPIO_8_ROMSO	GPIO9_SI
P2	GPIO_9_ROMSI	GPIO10_SCK
N6	GPIO_10_ROMSCK	
N5	GPIO_11	GPIO_11
N3	GPIO_12	GPIO_12
Y9	GPIO_13	GPIO_13
N1	GPIO_14_HPD2	PWRCNTL_0
M4	GPIO_15_PWRCNTL_0	GPIO_16
R6	GPIO_16_SSIN	ThermINT
W10	GPIO_17_THERMAL_INT	HPD3
M2	GPIO_18_HPD3	CTF
P8	GPIO_19_CTF	PWRCNTL_1
N8	GPIO_20_PWRCNTL_1	
N7	GPIO_21_BB_EN	
L6	GPIO_22_ROMCSB	GPIO_22_CS
	GPIO_23_CLKREQB	JTAG_TRSTB
L5	JTAG_TRSTB	
L3	JTAG_TDI	
L1	JTAG_TCK	
K4	JTAG_TMS	
	JTAG_TDO	

AB13	GENERICA	GENERICB
W8	GENERICB	GENERICC
W9	GENERICC	GENERICD
W7	GENERICD	
AD10	GENERICE_HPD4	HPD4
AC14	HPD1	HPD1
AC16	VREFG	VREFG

N10	NC_PWRGOOD	PWR_GOOD_GPU
AB22	RSVD#8	
AC22	RSVD#9	

RESERVED

L9	NC#1	
N9	NC#2	
AB16	RSVD#3	
AB12	RSVD#2	
AB11	RSVD#1	
AF24	TESTEN	

RV710 A11 HF MVD FT1 BIN1

DAC1

AM26	R	A_R_DAC1 (17)
AK26	RB	A_RB_DAC1 (17)
AL25	G	A_G_DAC1 (17)
AJ25	GB	A_GB_DAC1 (17)
AH24	B	A_B_DAC1 (17)
AG25	BB	A_BB_DAC1 (17)
AH26	HSYNC	A_HSYNC_DAC1 (10,17)
AJ27	VSYNC	A_VSYNC_DAC1 (10,17)
AG24	AVDD	+AVDD
AE22	AVSSQ	
AE23	VDD1DI	+VDD1DI
AD23	VSS1DI	
AD22	RSET	RSET R12 499R

DAC2

AM12	R2	A_R_DAC2 (19)
AK12	R2B	A_RB_DAC2 (19)
AL11	G2	A_G_DAC2 (19)
AJ11	G2B	A_GB_DAC2 (19)
AK10	B2	A_B_DAC2 (19)
AL9	B2B	A_BB_DAC2 (19)
AL13	H2SYNC	A_HSYNC_DAC2 (10,19)
AJ13	V2SYNC	A_VSYNC_DAC2 (10,19)
AH12	C	
AM10	Y	
AJ9	COMP	
AE20	A2VDD	+A2VDD
AE17	A2VDDQ	+A2VDDQ
AE19	A2VSSQ	
AD19	VDD2DI	+VDD2DI
AC19	VSS2DI	
AG13	R2SET	R2SET R23 715R

+1.8V_DAC

C1050 10nF 10V X7R 402 10%
C1051 100nF 10V X5R 402 10%
C1052 1uF_6.3V 6.3V X5R 402 10%
C1056 4.7uF_6.3V

C1053 10nF 10V X7R 402 10%
C1054 100nF 10V X5R 402 10%
C1055 1uF_6.3V 6.3V X5R 402 10%

Place very close to ASIC balls.

+3.3V B3 120R_300mA
C2058 10nF   C2051 100nF   C2050 1uF_6.3V   C2057 4.7uF_6.3V

+1.8V_DAC
C2052 100nF   C2053 1uF_6.3V

+1.8V_DAC
C2054 10nF   C2055 100nF   C2056 1uF_6.3V

Place very close to ASIC balls.

+1.8V_DAC +1.8V
B1 BLM15BD121SN1

+3.3V
R4003 10K

(10) GPIO_0
(10) GPIO_1
(10) GPIO_2
(1) GPIO_3
(1) GPIO_4
(10) GPIO_5
(10) GPIO_7
(10) GPIO_8   R13 33R   GPIO8_SO
(10) GPIO_9   R14 33R   GPIO9_SI
(10) GPIO_10 R15 33R   GPIO10_SCK
(10) GPIO_11
(10) GPIO_12
(10) GPIO_13
(14) PWRCNTL_0
(10) GPIO_16
TP43
(22) CTF
(14) PWRCNTL_1
GPIO_22 R16 33R   GPIO_22_CS
R62 1K

(10) GENERICB
TP41
(10) GENERICD
(20) HPD4
(21) HPD1

+1.8V R21 221R   VREFG
+1.8V R22 110R
C53 100nF

Overlap R59/R60.
R59 10K DNI
R60 10K DNI

+3.3V_BUS +1.8V
R25 5.1K   R26 5.1K
(1,13,14) PWR_GOOD
R35 1K

+3.3V
R24 10K

U2
GPIO_22 1 CE#   VCC 8 +3.3V
GPIO_8   2 SO   HOLD# 7
         3 WP#   SCK 6 GPIO_10
         4 GND   SI 5   GPIO_9
PM25LV512A-100SCE

C57 100nF

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario

AMD

Date: Friday, May 15, 2009   Rev 2
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Title: RH LP RV710 DDR3 VGA (header) HDMI DVI
Doc No. 105-B890XX-00B

U1J — Part 10 of 10

XTAL / PLL

RV710: Do not install B6, C60, C61, C62, C58.
RV810: Install B6, C60, C61, C62, C58..

+1.8V
B6 BLM15BD121SN1
Overlap
MC58 4.7uF_6.3V
C58 10uF_X6S
C60 1uF_6.3V
C61 1uF_6.3V
C62 100nF

NS6 NS_VIA

+SPV18 — H7 NC_SPV18

GND_SPVSS — J7 SPVSS
GND_SPVSS

+1.1V
B9 BLM15BD121SN1
+VDDC
B10 BLM15BD121SN1

+SPV10 — H8 SPV10

C69 1uF_6.3V
C70 1uF_6.3V
C71 100nF
C72 10nF

RV710: Install B10, do not install B9
RV810: Install B9, do not install B10

DPLL_PVDD AF14 +DPLL_PVDD
DPLL_PVSS AE14 GND_PVSS
GND_PVSS
DPLL_VDDC AD14 +DPLL_VDDC
PCIE_PVDD AM30 +PCIE_PVDD
NC_MPV18 L8 +MPVDD

Overlap
C59 10nF
C64 100nF
C63 10uF_X6S
MC63 4.7uF_6.3V
C88 10uF_X6S
MC88 4.7uF_6.3V
B7 BLM15BD121SN1 +1.8V
NS_VIA NS5

Overlap
C65 10nF
C66 100nF
C67 1uF_6.3V
C68 10uF_X6S
MC68 4.7uF_6.3V
+1.1V

Overlap
C73 1uF_6.3V
C74 10nF
C75 100nF
C89 10uF_X6S
MC89 4.7uF_6.3V
B11 BLM15BD121SN1 +1.8V

60R B12 +1.8V
C79 100nF
C80 1uF_6.3V
C81 1uF_6.3V
C77 10uF_X6S
MC77 4.7uF_6.3V
Overlap

RV710: Do not install B12, C77, C79, C80, C81.
RV810: Install B12, C77, C79, C80, C81.

XTALIN_S
C82 12pF_50V
R30 0R
R31 1M
XTALIN AM28 XTALIN
XTALOUT_S
XTALOUT
XTALOUT AK28 XTALOUT
C83 12pF_50V
Y2 27.000MHz_10PPM

RV710 A11 HF MVD FT1 BIN1

DDC6 BUS:

I2C Address	Function	Device
0x90	I2C VDDC Control	DS4402
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A

U1H — Part 8 of 10

I2C / DDC / AUX

+3.3V
R36 4.7K
R37 4.7K
DDC6CLK AC1 DDC6CLK
DDC6DATA AC3 DDC6DATA

+3.3V
R33 4.7K
R34 4.7K
SCL R1 SCL
SDA R3 SDA

AUX1P AD2
AUX1N AD4
DDC1CLK AE6 DDC1CLK (19)
DDC1DATA AE5 DDC1DATA (19)

AUX2P AD13
AUX2N AD11
DDC2CLK AC11 DDC2CLK (21)
DDC2DATA AC13 DDC2DATA (21)

DDCCLK_AUX5P AE16 DDCAUX5P (17)
DDCDATA_AUX5N AD16 DDCAUX5N (17)
NC_DDCCLK_AUX7P AD20
NC_DDCDATA_AUX7N AC20

TMDP / DAC1
LVTTMDP / DAC2

RV710 A11 HF MVD FT1 BIN1

U1I — Part 9 of 10

TSS FDO

+1.8V
+TSVDD AD17 TSVDD
TS_FDO R5 TS_FDO (22)
C4020 1uF_6.3V
C4021 100nF
GND AC17 TSVSS
DPLUS T4 GPU_DPLUS
C4004 2.2nF_50V
DMINUS T2 GPU_DMINUS

RV710 A11 HF MVD FT1 BIN1

Advanced Micro Devices Inc.
1 Commerce Valley Drive East
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Date: Friday, May 15, 2009
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Title: RH LP RV710 DDR3 VGA (header) HDMI DVI
Doc No. 105-B890XX-00B

(05) RV710 TMDP A&B

TMDP INTERFACE

U1F

PART 6 OF 10

DPA

AG8	DPA_PVDD	TX2P_DPA0P	AK3
		TX2M_DPA0N	AK1
AG7	DPA_PVSS	TX1P_DPA1P	AH3
		TX1M_DPA1N	AH1
		TX0P_DPA2P	AG3
		TX0M_DPA2N	AG5
AF11	NC_DPA_VDD18#2	TXCAP_DPA3P	AF2
AE11	NC_DPA_VDD18#1	TXCAM_DPA3N	AF4

DPA_VSSR#5 AH5
DPA_VSSR#3 AG1
DPA_VSSR#4 AG6
DPA_VSSR#2 AE3
DPA_VSSR#1 AE1

AF6 DPA_VDD10#1
AF7 DPA_VDD10#2

DPB

		TX5P_DPB0P	AK8	TX2P (21)
		TX5M_DPB0N	AL7	TX2M (21)
+1.8V		TX4P_DPB1P	AJ7	TX1P (21)
B2503 BR2503 0R	+DPB_PVDD	TX4M_DPB1N	AH6	TX1M (21)
AG10	DPB_PVDD	TX3P_DPB2P	AK6	TX0P (21)
		TX3M_DPB2N	AM5	TX0M (21)
AG11	DPB_PVSS	TXCBP_DPB3P	AK5	TXCAP (21)
		TXCBM_DPB3N	AM3	TXCAM (21)

C2509 4.7uF_6.3V C2510 1uF_6.3V C2501 1uF_6.3V C2511 100nF

DPB_VSSR#5 AM8
DPB_VSSR#2 AG9
DPB_VSSR#1 AF10
DPB_VSSR#4 AM6
DPB_VSSR#3 AH8

+1.8V
B2504 BLM15BD121SN1 +DPB_VDD18

AE13 NC_DPB_VDD18#1
AF13 NC_DPB_VDD18#2

C2512 4.7uF_6.3V C2513 1uF_6.3V C2504 1uF_6.3V C2514 100nF

CALIBRATION

+1.1V
BR2505 0R +DPB_VDD10

AF8 DPB_VDD10#1
AF9 DPB_VDD10#2

AE10 DPAB_CALR | DPAB_CALR | 150R R2500 1%

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C2515 4.7uF_6.3V C2516 1uF_6.3V C2507 1uF_6.3V C2517 100nF

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LVTMDP INTERFACE

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DPF

Pin	Signal		Signal	Pin	Net
AG19	NC_DPF_PVDD		RSVD#6	AK24	
			RSVD#4	AJ23	
			T2X5P_DPF0P	AL23	T2X5P (20)
			T2X5M_DPF0N	AK22	T2X5M (20)
AF20	NC_DPF_PVSS		T2X4P_DPF1P	AH22	T2X4P (20)
			T2X4M_DPF1N	AJ21	T2X4M (20)
AG17	DPF_VDD18#2		T2X3P_DPF2P	AL21	T2X3P (20)
AF16	DPF_VDD18#1		T2X3M_DPF2N	AK20	T2X3M (20)
			T2XCFP_DPF3P	AH20	
			T2XCFM_DPF3N	AJ19	
			DPF_VSSR#4	AM22	
			DPF_VSSR#5	AM24	
AG22	DPF_VDD10#2		DPF_VSSR#2	AG23	
AF22	DPF_VDD10#1		DPF_VSSR#1	AF23	
			DPF_VSSR#3	AM20	

DPE

		RSVD#7	AL19	
		RSVD#5	AK18	
		T2X2P_DPE0P	AH18	T2X2P (20)
		T2X2M_DPE0N	AJ17	T2X2M (20)

+1.8V

BR1500 0R +DPE_PVDD AG18 DPE_PVDD | T2X1P_DPE1P | AL17 | T2X1P (20) |
| T2X1M_DPE1N | AK16 | T2X1M (20) |

C1500 4.7uF_6.3V C1501 1uF_6.3V C1509 1uF_6.3V C1502 100nF

| | | T2X0P_DPE2P | AH16 | T2X0P (20) |
| | | T2X0M_DPE2N | AJ15 | T2X0M (20) |

AF19 DPE_PVSS | T2XCEP_DPE3P | AL15 | T2XCEP (20) |
| T2XCEM_DPE3N | AK14 | T2XCEM (20) |

+1.8V

B1501 BLM15BD121SN1 +DPE_VDD18 AG16 DPE_VDD18#2
AG15 DPE_VDD18#1

DPE_VSSR#3	AM14
DPE_VSSR#2	AH14
DPE_VSSR#1	AG14
DPE_VSSR#4	AM16
DPE_VSSR#5	AM18

C1503 4.7uF_6.3V C1504 1uF_6.3V C1510 1uF_6.3V C1505 100nF

CALIBRATION

+1.1V

+DPE_VDD10 AG21 DPE_VDD10#2
AG20 DPE_VDD10#1

AF17 DPEF_CALR 150R 1% R1500

1A

C1506 4.7uF_6.3V C1507 1uF_6.3V C1511 1uF_6.3V C1508 100nF

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MEMORY INTERFACE

(15,16) M_MDA[63..0]

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MEMORY INTERFACE

M_MDA0	K27	DQA_0
M_MDA1	J29	DQA_1
M_MDA2	H30	DQA_2
M_MDA3	H32	DQA_3
M_MDA4	G29	DQA_4
M_MDA5	F28	DQA_5
M_MDA6	F32	DQA_6
M_MDA7	F30	DQA_7
M_MDA8	C30	DQA_8
M_MDA9	F27	DQA_9
M_MDA10	A28	DQA_10
M_MDA11	C28	DQA_11
M_MDA12	E27	DQA_12
M_MDA13	G26	DQA_13
M_MDA14	D26	DQA_14
M_MDA15	F25	DQA_15
M_MDA16	A25	DQA_16
M_MDA17	C25	DQA_17
M_MDA18	E25	DQA_18
M_MDA19	D24	DQA_19
M_MDA20	E23	DQA_20
M_MDA21	F23	DQA_21
M_MDA22	D22	DQA_22
M_MDA23	F21	DQA_23
M_MDA24	E21	DQA_24
M_MDA25	D20	DQA_25
M_MDA26	F19	DQA_26
M_MDA27	A19	DQA_27
M_MDA28	D18	DQA_28
M_MDA29	F17	DQA_29
M_MDA30	A17	DQA_30
M_MDA31	C17	DQA_31
M_MDA32	E17	DQA_32
M_MDA33	D16	DQA_33
M_MDA34	F15	DQA_34
M_MDA35	A15	DQA_35
M_MDA36	D14	DQA_36
M_MDA37	F13	DQA_37
M_MDA38	A13	DQA_38
M_MDA39	C13	DQA_39
M_MDA40	E11	DQA_40
M_MDA41	A11	DQA_41
M_MDA42	C11	DQA_42
M_MDA43	F11	DQA_43
M_MDA44	A9	DQA_44
M_MDA45	C9	DQA_45
M_MDA46	F9	DQA_46
M_MDA47	D8	DQA_47
M_MDA48	E7	DQA_48
M_MDA49	A7	DQA_49
M_MDA50	C7	DQA_50
M_MDA51	F7	DQA_51
M_MDA52	A5	DQA_52
M_MDA53	E5	DQA_53
M_MDA54	C3	DQA_54
M_MDA55	E1	DQA_55
M_MDA56	G7	DQA_56
M_MDA57	G6	DQA_57
M_MDA58	G1	DQA_58
M_MDA59	G3	DQA_59
M_MDA60	J6	DQA_60
M_MDA61	J1	DQA_61
M_MDA62	J3	DQA_62
M_MDA63	J5	DQA_63

MAA_0	K17	M_MAA0	
MAA_1	J20	M_MAA1	
MAA_2	H23	M_MAA2	
MAA_3	G23	M_MAA3	
MAA_4	G24	M_MAA4	
MAA_5	H24	M_MAA5	
MAA_6	J19	M_MAA6	
MAA_7	K19	M_MAA7	
MAA_8	J14	M_MAA8	
MAA_9	K14	M_MAA9	
MAA_10	J11	M_MAA10	
MAA_11	J13	M_MAA11	

M_MAA[14..0] (15,16,18)

MAA_BA0 J16 BA0 (15,16,18)
MAA_BA1 L15 BA1 (15,16,18)
MAA_12 H11 M_MAA12
MAA_BA2 G11 BA2 (15,16,18)

DQMA_0	E32	M_DQMA#0
DQMA_1	E30	M_DQMA#1
DQMA_2	A21	M_DQMA#2
DQMA_3	C21	M_DQMA#3
DQMA_4	E13	M_DQMA#4
DQMA_5	D12	M_DQMA#5
DQMA_6	E3	M_DQMA#6
DQMA_7	F4	M_DQMA#7

M_DQMA#[7..0] (15,16)

QSA_0	H28	M_QSA0
QSA_1	C27	M_QSA1
QSA_2	A23	M_QSA2
QSA_3	E19	M_QSA3
QSA_4	E15	M_QSA4
QSA_5	D10	M_QSA5
QSA_6	D6	M_QSA6
QSA_7	G5	M_QSA7

M_QSA[7..0] (15,16)

QSA_0B	H27	M_QSA#0
QSA_1B	A27	M_QSA#1
QSA_2B	C23	M_QSA#2
QSA_3B	C19	M_QSA#3
QSA_4B	C15	M_QSA#4
QSA_5B	E9	M_QSA#5
QSA_6B	C5	M_QSA#6
QSA_7B	H4	M_QSA#7

M_QSA#[7..0] (15,16)

WRITE STROBE READ STROBE

ODTA0 L18 ODTA0 (15,16,18)
ODTA1 K16 ODTA1 (15,16,18)

CLKA0 H26 CLKA0 (15,16)
CLKA1 G9 CLKA1 (15,16)

CLKA0B H25 CLKA#0 (15,16)
CLKA1B H9 CLKA#1 (15,16)

RASA0B G22 RASA#0 (15,16,18)
RASA1B G17 RASA#1 (15,16,18)

CASA0B G19 CASA#0 (15,16,18)
CASA1B G16 CASA#1 (15,16,18)

CSA0B_0 H22 CSA#0_0 (15)
CSA0B_1 J22 CSA#0_1 (16)

CSA1B_0 G13 CSA#1_0 (15)
CSA1B_1 K13 CSA#1_1 (16)

CKEA0 K20 CKEA0 (15,16,18)
CKEA1 J17 CKEA1 (15,16,18)

WEA0B G25 WEA#0 (15,16,18)
WEA1B H10 WEA#1 (15,16,18)

DRAM_RST L10 DRAM_RST

+MVDD

R291 100R

MVREFD_A K26 MVREFDA
J26 MVREFSA

R292 100R
C295 100nF
C296 10nF

+MVDD

R293 100R

MVREFS_A

R294 100R
C297 100nF
C298 10nF

CLKTESTA K8 CLKTESTA
CLKTESTB L7 CLKTESTB

MEMTEST J8 MEM_CALRP1

+MVDD

R296 4.7K
R297 4.7K
R298 243R

M_MAA[14..0] (15,16,18)

M_MAA13 G20 NC_MAA_13
M_MAA14 G14 NC_MAA_14
K7 NC_MEM_CALRN1
R300 4.7K K25 NC_MEM_CALRP1
R301 4.7K J25 NC_MEM_CALRP0
R302 4.7K NC_MEM_CALRN0

+MVDD

R295 2.0K

DRAM_RST (15,16)

C299 1uF_6.3V
MR295 4.7K Overlap

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DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R

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(08) RV710 Power

Overlap cap footprints (0805 with 0603).

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U1D

POWER

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+MVDD

C120 10nF C121 10nF C122 10nF C123 10nF C124 10nF C125 100nF C126 100nF C127 100nF C128 100nF C129 100nF

C134 1uF_6.3V C135 1uF_6.3V C136 1uF_6.3V C137 1uF_6.3V C138 1uF_6.3V C139 1uF_6.3V C140 1uF_6.3V C141 100nF C142 100nF

Overlap cap footprints (0805 with 0603).

C130 10uF_X6S C131 10uF_X6S C132 10uF_X6S C133 10uF_X6S

MC130 4.7uF_6.3V MC131 4.7uF_6.3V MC132 4.7uF_6.3V MC133 4.7uF_6.3V

+1.8V

Overlap

MC159 4.7uF_6.3V C159 10uF_X6S C160 100nF C161 1uF_6.3V C162 1uF_6.3V C163 100nF

+VDD_CT

+3.3V

C164 1uF_6.3V C165 1uF_6.3V C166 100nF C167 100nF

+1.8V

C178 1uF_6.3V C179 100nF C180 1uF_6.3V C181 100nF

+MVDD

+VDDRH1

C191 1uF_6.3V C192 1uF_6.3V

GND_VSSRH1

NS11 NS_VIA
GND_VSSRH1

H13 VDDR1#1
H16 VDDR1#2
H19 VDDR1#3
J10 VDDR1#4
J23 VDDR1#5
J24 VDDR1#6
J9 VDDR1#7
K10 VDDR1#8
K23 VDDR1#9
K24 VDDR1#10
K9 VDDR1#11
L11 VDDR1#12
L12 VDDR1#13
L13 VDDR1#14
L20 VDDR1#15
L21 VDDR1#16
L22 VDDR1#17

AA20 VDD_CT#1
AB20 VDD_CT#2
AB21 VDD_CT#3
VDD_CT#4

AA17 VDDR3#1
AA18 VDDR3#2
AB17 VDDR3#3
AB18 VDDR3#4

AA11 VDDR4#1
AA12 VDDR4#2
Y11 VDDR4#3
Y12 VDDR4#4

U11 VDDR5#1
U12 VDDR5#2
V11 VDDR5#3
V12 VDDR5#4

L17 VDDRHA

L16 VSSRHA

VDDCI#1 M13
VDDCI#2 M15
VDDCI#3 M16
VDDCI#4 M17
VDDCI#5 M18
VDDCI#6 M20
VDDCI#7 M21
VDDCI#8 N20

PCIE_VDDR#1 AB23
PCIE_VDDR#2 AC23
PCIE_VDDR#3 AD24
PCIE_VDDR#4 AE24
PCIE_VDDR#5 AE25
PCIE_VDDR#6 AE26
PCIE_VDDR#7 AF25
PCIE_VDDR#8 AG26

PCIE_VDDC#1 L23
PCIE_VDDC#2 L24
PCIE_VDDC#3 L25
PCIE_VDDC#4 L26
PCIE_VDDC#5 N22
PCIE_VDDC#6 N23
PCIE_VDDC#7 N24
PCIE_VDDC#8 R22
PCIE_VDDC#9 T22
PCIE_VDDC#10 U22
PCIE_VDDC#11 V22
PCIE_VDDC#12

VDDC#1 AA15
VDDC#2 M11
VDDC#3 M12
VDDC#4 N15
VDDC#5 N17
VDDC#6 R13
VDDC#7 R16
VDDC#8 R18
VDDC#9 R21
VDDC#10 T12
VDDC#11 T15
VDDC#12 T17
VDDC#13 T20
VDDC#14 U13
VDDC#15 U16
VDDC#16 U18
VDDC#17 U21
VDDC#18 V15
VDDC#19 V17
VDDC#20 V20
VDDC#21 V21
VDDC#22 Y13
VDDC#23 Y16
VDDC#24 Y18
VDDC#25 Y21

+1.8V

Overlap

C143 1uF_6.3V C144 1uF_6.3V C145 1uF_6.3V C146 1uF_6.3V C149 100nF C148 10nF

C147 10uF_X6S MC147 4.7uF_6.3V

+1.1V

Overlap

C150 1uF_6.3V C151 1uF_6.3V C152 1uF_6.3V C153 1uF_6.3V C154 1uF_6.3V C155 1uF_6.3V C156 1uF_6.3V C157 1uF_6.3V

C158 10uF_X6S MC158 4.7uF_6.3V

+VDDC

+VDDCI

Overlap

C86 100nF C87 100nF C193 100nF C194 1uF_6.3V C195 1uF_6.3V

C196 10uF_X6S MC196 4.7uF_6.3V

+VDDC

Overlap

+VDDC

C168 1uF_6.3V C169 1uF_6.3V C170 1uF_6.3V C171 1uF_6.3V C172 1uF_6.3V C173 1uF_6.3V C85 1uF_6.3V

C182 1uF_6.3V C183 1uF_6.3V C184 1uF_6.3V C185 1uF_6.3V C186 1uF_6.3V C187 1uF_6.3V C188 1uF_6.3V C189 1uF_6.3V C190 1uF_6.3V

Overlap cap footprints (0805 with 0603).

+VDDC

C174 10uF_X6S C175 10uF_X6S C176 10uF_X6S C177 10uF_X6S

MC174 4.7uF_6.3V MC175 4.7uF_6.3V MC176 4.7uF_6.3V MC177 4.7uF_6.3V

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GND

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Pin	Signal		Signal	Pin
AA27	PCIE_VSS#1		GND#33	F18
AB24	PCIE_VSS#2		GND#34	F2
AB32	PCIE_VSS#3		GND#35	F20
AC24	PCIE_VSS#4		GND#36	F22
AC26	PCIE_VSS#5		GND#37	F24
AC27	PCIE_VSS#6		GND#38	F26
AD25	PCIE_VSS#7		GND#39	F6
AD32	PCIE_VSS#8		GND#40	F8
AE27	PCIE_VSS#9		GND#41	G10
AF32	PCIE_VSS#10		GND#42	G27
AG27	PCIE_VSS#11		GND#43	G31
AH32	PCIE_VSS#12		GND#44	G8
K28	PCIE_VSS#13		GND#45	H14
K32	PCIE_VSS#14		GND#46	H17
L27	PCIE_VSS#15		GND#47	H2
M32	PCIE_VSS#16		GND#48	H20
N25	PCIE_VSS#17		GND#49	H6
N27	PCIE_VSS#18		GND#50	J27
P25	PCIE_VSS#19		GND#51	J31
P32	PCIE_VSS#20		GND#52	K11
R27	PCIE_VSS#21		GND#53	K2
T25	PCIE_VSS#22		GND#54	K22
T32	PCIE_VSS#23		GND#55	K6
U25	PCIE_VSS#24		GND#56	M6
U27	PCIE_VSS#25		GND#57	N11
V32	PCIE_VSS#26		GND#58	N12
W25	PCIE_VSS#27		GND#59	N13
W26	PCIE_VSS#28		GND#60	N16
W27	PCIE_VSS#29		GND#61	N18
Y25	PCIE_VSS#30		GND#62	N21
Y32	PCIE_VSS#31		GND#63	P6
			GND#64	P9
			GND#65	R12
			GND#66	R15
A3	GND#1		GND#67	R17
A30	GND#2		GND#68	R20
AA13	GND#3		GND#69	T13
AA16	GND#4		GND#70	T16
AB10	GND#5		GND#71	T18
AB15	GND#6		GND#72	T21
AB6	GND#7		GND#73	T6
AC9	GND#8		GND#74	U15
AD6	GND#9		GND#75	U17
AD8	GND#10		GND#76	U20
AE7	GND#11		GND#77	U3
AG12	GND#12		GND#78	U9
AH10	GND#13		GND#79	V13
AH28	GND#14		GND#80	V16
B10	GND#15		GND#81	V18
B12	GND#16		GND#82	V6
B14	GND#17		GND#83	Y10
B16	GND#18		GND#84	Y15
B18	GND#19		GND#85	Y17
B20	GND#20		GND#86	Y20
B22	GND#21		GND#87	Y6
B24	GND#22		GND#88	T11
B26	GND#23		GND#89	R11
B6	GND#24			
B8	GND#25			
C1	GND#26			
C32	GND#27			
E28	GND#28			
F10	GND#29			
F12	GND#30		VSS_MECH#1	A32
F14	GND#31		VSS_MECH#2	AM1
F16	GND#32		VSS_MECH#3	AM32

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(10) RV710 STRAPS

PIN BASED STRAPS

+3.3V

DNI · R43 · 10K · A_VSYNC_DAC2 (3,19)
VIP_DEVICE_STRAP_EN
0: Driver would ignore the value sampled on VHAD_0 during reset
1: Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no).

DNI · R44 · 10K · GPIO_9 · GPIO_9 (3)
VGA DISABLE : 1 for disable (set to 0 for normal operation)

R45 · 10K · GPIO_0 · GPIO_0 (3)
GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

R46 · 10K · GPIO_1 · GPIO_1 (3)
GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

R47 · 10K · GPIO_2 · GPIO_2 (3)
GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

R48 · 10K · GPIO_11 · GPIO_11 (3)
DNI · R49 · 10K · GPIO_13 · GPIO_13 (3)
DNI · R50 · 10K · GPIO_12 · GPIO_12 (3)

GPIO(13, 12,11) - CONFIG[2..0]

CONFIG[2]	100 - 512Kbit	M25P05A	(ST)
	101 - 1Mbit	M25P10A	(ST)
	101 - 2Mbit	M25P20	(ST)
CONFIG[1]	101 - 4Mbit	M25P40	(ST)
	101 - 8Mbit	M25P80	(ST)
CONFIG[0]	100 - 512Kbit	Pm25LV512	(Chingis)
	101 - 1Mbit	Pm25LV010	(Chingis)

DNI · R51 · 10K · A_VSYNC_DAC1 (3,17)
AUD[0]

R52 · 10K · A_HSYNC_DAC1 (3,17)
AUD[1]

DNI · R53 · 10K · GPIO_8 · GPIO_8 (3)
BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

R54 · 10K · GPIO_5 · GPIO_5 (3)
[GPIO_5 : GPIO_16]

DNI · R55 · 10K · GPIO_16 · GPIO_16 (3)
Quimonda [0:0]
Hynix [0:1]
Samsung [1:0]

DNI · R56 · 10K · A_HSYNC_DAC2 (3,19)
RESERVED :Internal use only. Other logic must not affect this signal during RESET.

NTSC · R57 · 10K · GPIO_7 · GPIO_7 (3)
TV OUT STANDARD 0 - PAL TVO   1 - NTSC TVO

DNI · R70 · 10K · GENERICB · GENERICB (3)
DNI · R71 · 10K · GENERICD · GENERICD (3)
GenericB and GenericD will be used for additional memory vendor straps.

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Title: RH LP RV710 DDR3 VGA (header) HDMI DVI
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(11) VDDC

COMPENSATION CIRCUIT

FILTERED SMPS VCC

BOOT CIRCUIT

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(12) MVDD

COMPENSATION CIRCUIT

C711 33nF_16V 402 10V X7R 10%
C712 56pF_50V 603 50V NPO 5%
C714 100nF 402 10V X5R 10%
402 MVDDC_COMP
R712 6.04K 402 1%
R714 0R MVDDC_FB
R709 0R

FILTERED SMPS VCC

+12V_BUS
+MVDD_VCC
R706 2.2R
603 X7R 5% C707 100nF

BOOT CIRCUIT

+12V_BUS
D701 BAT54KFILM
C706 150nF_16V
+MVDDC_B
C705 100nF 603 X7R 5% 16V
+PW_MVDDC_M

U703 uP6101BU
1 BOOT PHASE 8 +PW_MVDDC_M
2 UGATE COMP 7 MVDDC_COMP
3 GND FB 6 MVDDC_FB
4 LGATE VCC 5 +MVDD_VCC

+MVDDC_B
+PW_MVDDC_HGD
+PW_MVDDC_LGD
R708 20K
R715 42.2K 402
C703 0.22uF
place R715 close to IC pin4

MVDD_EN (14)

Layout guideline
1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

+MVDDC_S
+12V_BUS
B702 60R R702 0R
C730 100uF_16V

C715 10UF 1206
C716 10UF 1206
C717 4.7uF_16V 805
C719 4.7uF_16V 805
C718 150nF_16V 603
Mirrored on PCB
Mirrored on PCB

+PW_MVDDC_HGD R721 0R 1 Q701 P0903BDL 402

+PW_MVDDC_M
L701 1.6uH 18A CHK_D2_P5_1 L04-16A7171-T15

+PW_MVDDC_LGD R722 0R 1 Q702 P0603BDL 603

NS700 NS_VIA Sense Point

R719 1R 0805 1% Rs
C708 10nF_25V 402 X7R 25V Cs
Place Rs and Cs across QL
RC snubber values shown are for reference only, tuning is required

+MVDD

MVDD_FB_TRACE
R716 0R 603 Reserve for Loop Measurement

C726 820uF_2.5V 8 x 8 mm, TH C_P3_5_D8_H9 C71-8210281-N07

C723 10uf Y5V 12066.3V
C724 10uf Y5V 12066.3V

MVDD_SV
C713 1.8nF_50V 402 16V 10% X7R

RFB1 R711 10K 402 1%
R713 7.87K 402 5%

0.8V Ref
R4 = (R1 x 0.8V) / (Vout1 - 0.8V)
(14) MVDDC_FB MVDDC_FB

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(13) Linear Regulators

LDO #2:   Vin = 2.1V to 3.6V MAX   Vout = +1.8V   +/- 2%   Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

Regulators for +5V_VESA

Overlap 1206 / 1210 footprints.

+12V_BUS
R861 470R
+5V_SHUNT
+5V_SHUNT
D861 5.1V
+3.3V_BUS
+MVDD
B880 220R_2A
0805
MR880 0R
Overlap
+1.8V
R880 0R
0805
+1.8V_LDO2
R815 0R
PWR_GOOD_R
(1,3,14) PWR_GOOD
(14) LDO2-3_EN
U861
POK GND#8
EN FB
VIN VOUT
CNTL REFIN GND#9
uP7706U8
+5V_SHUNT
R866 0R
DNI
LDO2_FB
R865 12.7K_0.1%
C865 33pF_50V
R864 10K_0.1%
DNI 0.1%
C862 10uF_X6S
C861 10uF_X6S
C864 100nF
C866 10uF_X6S
C868 1uF_6.3V
R5 C3
R4

VOUT = Vref x (1 + R5/R4)

+12V_BUS
F812 nanoSMDC020F 1206
MR812 0R 0805 1/8W 5%
MU810 MCP1702T-5002E/MB
2 IN   OUT 3
GND
+5V_VESA
+VESA_IN
U810
VIN VOUT#2
NC VOUT#3
NC#8 VOUT#6
ADJ VOUT
LM317LCDR
VESA_FB
C810 100nF 0603 16V
R813 499R 0402
C811 1uF_6.3V
R814 1.5K 0402
C812 10uF_10V
TEST
R1
R2

Vout(V) = Vref (1+R2/R1)

LDO #3:   Vin = +1.4V to 2.087VMAX   Vout = +1.1V   +/- 2.5%   Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

+MVDD
1210 1/2W
PWR_GOOD_R
LDO2-3_EN
U851
POK GND#8
EN FB
VIN VOUT
CNTL REFIN GND#9
uP7706U8
+5V_SHUNT
C856 10uF_X6S
C858 1uF_6.3V
R856 0R
DNI
LDO3_FB
R855 3.92K
C855 33pF_50V
R854 10K
C852 10uF_X6S
C851 10uF_X6S
C854 100nF
DNI
LDO3_OUT
R860 0R
+1.1V
R860 0R
Overlap
MR890 0R
B890 220R_2A
+VDDC
R5 C3
R4

VOUT = Vref x (1 + R5/R4)

+5V_VESA   +5V_VESA2
C820 100nF
C821 100nF
C822 100nF
Place near DDC pull-up resistors.

+5V_VESA   +5V_VESA2   +5V_SHUNT
R820 0R   R821 0R

+5V_VESA2
+VESA_IN
U830
VIN VOUT#2
NC VOUT#3
NC#8 VOUT#6
ADJ VOUT
LM317LCDR
C830 100nF 0603 16V
R833 499R 0402
C831 1uF_6.3V
R834 1.5K 0402
R1
R2

Vout(V) = Vref (1+R2/R1)

(14) Power Management

Power Play

VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V)					
		Rf1= Rf2=		Rf1= Rf2=		Rf1= Rf2=	
0	0						
0	1						
1	0						
1	1	1	0	1		Power-up Default	

MVDD Voltage Settings Using GPIOs

PWRCNTL_2 GPIO_6	Output Voltage (V)					
	Rf1= Rf2=		Rf1= Rf2=		Rf1= Rf2=	
0						
1	1	0	1		Power-up Default	

Power up/down Sequencing

Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.

Node 1

Node 1
Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)
Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)
Typical trigger when +12V ramps above 10V (1.1V)

When +12V_BUS ramps above min Vbe, SMPS_EN will be held low

22.6K: 1.154V, PN: 3160226200G
23.2K: 1.145, PN: 3160232200G
23.7K: 1.1376 PN: 3160237200G

Test cct for low VDDC voltage.
DNI

Place close to R611 in the VDDC section.

Place close to R711 in the MVDD section.

31607871000Ω
R710=7.68K

VDD_EN (11,22)
VDDC_FB (11)
LDO2-3_EN (13)
MVDD_EN (12)
MVDDC_FB (12)
PWR_GOOD (1,3,13)
ALL_RAILS_UP (20,21)
PWRCNTL_0 (3)
PWRCNTL_1 (3)

Rf1 R1226 80.6K 1%
Rf2 R1225 40.2K 1%
R610 10K
R4 RFB2 R710 3.24K

Node 1: R857 4.7K, R850 475R, R852 1.62K, Q850 MMBT3904, Q851 MMBT3904, Q852 MMBT3904, C846 100nF, R851 200R, R853 200R
R843 5.1K, R841 1K, Q840 MMBT3904, C841 1uF_6.3V, R844 5.1K, R845 5.1K, Q841 MMBT3904, R846 5.1K, Q842 MMBT3904
R890 5.1K, R893 5.1K, R891 5.1K, Q853 MMBT3904
R892 0R, Q845 SI2304DS, C842 10uF_X6S, R840 100K
R848 100K, R849 10K, R847 10K, Q843 MMBT3904, Q844 MMBT3904, C844 100nF_6.3V, C843 100NF 402 X5R 16V, MR847 10K DNI
R1240 10K, R1241 10K, MR1240 10K DNI, MR1241 10K DNI
Q1200 2N7002E, Q1201 2N7002E

(15) DDR3 RANK1

RANK1: 256MB/512MB DDR3

Should be 240 Ohms +-1%

Share VREFD/VREFC to save PCB space

Overlap 0805 / 0603 footprints.

80R for dual rank?

100-BALL SDRAM DDR3
23E22387MNG8

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RANK2: 256MB/512MB DDR3

This schematic page contains DDR3 memory circuit diagrams with four SDRAM chips (U301, U302, U303, U304) labeled as "100-BALL SDRAM DDR3 23E22387MNG8".

Each chip has notation "Should be 240 Ohms +-1%" with resistors R317 (243R), R318 (243R), R319 (243R), R320 (243R).

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DAC 1 OUTPUT

Optional ESD Protection Diodes

Place close to Connector
ALLOW FOR A LOW INDUCTANCE PATH TO PIN 5

+5V_VESA

Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane
Resistors are footprint options for the inductors. Footprints should be overlapped. (R1024-26)

R1024   0R   DNI
R1025   0R   DNI
R1026   0R   DNI

(3) A_R_DAC1
(3) A_RB_DAC1

(3) A_G_DAC1
(3) A_GB_DAC1

(3) A_B_DAC1
(3) A_BB_DAC1

A_R_DAC1_M   L1001   16NH_500MA
A_G_DAC1_M   L1002   16NH_500MA
A_B_DAC1_M   L1003   16NH_500MA

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F

C1011
1uF

R1029   R1028   R1027
37.4R   37.4R   37.4R

R1003   R1002   R1001
75R   75R   75R

C1001   C1002   C1003
8.0pF   8.0pF   8.0pF
402   402   402

C1004   C1005   C1006
8.0pF   8.0pF   8.0pF

MJ1001
1   R
2   G
3   B
11   MS0
12   MS1
4   MS2
15   MS3
9   NC
13   HS
14   VS
5   VSS
6   VSS#6
7   VSS#7
8   VSS#8
10   VSS#10
16   CASE
17   CASE#17
G3179C219-005

DDCDATA_DAC1_R
DDCCLK_DAC1_R
A_HSYNC_DAC1_R
A_VSYNC_DAC1_R

C1010
68pF

DDCDATA_DAC1_R   (20)
DDCCLK_DAC1_R   (20)
A_HSYNC_DAC1_R   (20)
A_VSYNC_DAC1_R   (20)
A_R_DAC1_F   (20)
A_G_DAC1_F   (20)
A_B_DAC1_F   (20)

To DVI connector.

+5V_VESA

R1005
2.2K
402

(4) DDCAUX5N

R1006   33R   402   DDCDATA_DAC1_R

+5V_VESA

R1008
2.2K
402

(4) DDCAUX5P

R1009   33R   402   DDCCLK_DAC1_R

+5V_VESA

C1999   100nF   U1999A

(3,10) A_HSYNC_DAC1

2   3   A_HSYNC_DAC1_B

R1010   33R   402   A_HSYNC_DAC1_R

74AHCT125
U1999B

(3,10) A_VSYNC_DAC1

5   6   A_VSYNC_DAC1_B

R1011   33R   402   A_VSYNC_DAC1_R

74AHCT125

C1007
12pF_50V

C1008
12pF_50V

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

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(17) DDR3 Termination

(7,15,16) CKEA0
(7,15,16) ODTA0
(7,15,16) RASA#0
(7,15,16) CASA#0
(7,15,16) WEA#0

(7,15,16) CKEA1
(7,15,16) ODTA1
(7,15,16) RASA#1
(7,15,16) CASA#1
(7,15,16) WEA#1

+MVDD R240 56R CKEA0   R241 56R
+MVDD R242 56R ODTA0   R243 56R

+MVDD R246 56R RASA#0 R247 56R
+MVDD R248 56R CASA#0 R246 56R
+MVDD R250 56R WEA#0   R251 56R

+MVDD R252 56R CKEA1   R253 56R
+MVDD R254 56R ODTA1   R255 56R

+MVDD R258 56R RASA#1 R259 56R
+MVDD R260 56R CASA#1 R261 56R
+MVDD R262 56R WEA#1   R263 56R

(7,15,16) M_MAA[14..0]

M_MAA0
M_MAA1
M_MAA2
M_MAA3
M_MAA4
M_MAA5
M_MAA6
M_MAA7
M_MAA8
M_MAA9
M_MAA10
M_MAA11
M_MAA12
M_MAA13
M_MAA14

+MVDD R271 56R M_MAA0   R270 56R
+MVDD R273 56R M_MAA1   R272 56R
+MVDD R275 56R M_MAA2   R274 56R
+MVDD R289 56R M_MAA3   R288 56R
+MVDD R235 56R M_MAA4   R290 56R
+MVDD R269 56R M_MAA5   R268 56R

+MVDD R279 56R M_MAA6   R278 56R
+MVDD R281 56R M_MAA7   R280 56R
+MVDD R283 56R M_MAA8   R282 56R
+MVDD R285 56R M_MAA9   R284 56R
+MVDD R287 56R M_MAA10 R286 56R
+MVDD R277 56R M_MAA11 R276 56R

+MVDD R399 56R M_MAA12 R299 56R
+MVDD R332 56R M_MAA13 R331 56R
+MVDD R334 56R M_MAA14 R333 56R

(7,15,16) BA0
(7,15,16) BA1
(7,15,16) BA2

+MVDD R328 56R BA0 R327 56R
+MVDD R326 56R BA1 R325 56R
+MVDD R330 56R BA2 R329 56R

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DAC 2 OUTPUT

Optional ESD Protection Diods

Place near D2002, D2003, D2004, D2005

Place close to Connector

Place close to Connector
Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane

(3) A_R_DAC2
(3) A_RB_DAC2

(3) A_G_DAC2
(3) A_GB_DAC2

(3) A_B_DAC2
(3) A_BB_DAC2

R2024   0R   DNI
R2025   0R   DNI
R2026   0R   DNI

A_R_DAC2_M   L2001   16NH_500MA   A_R_DAC2_F
A_G_DAC2_M   L2002   16NH_500MA   A_G_DAC2_F
A_B_DAC2_M   L2003   16NH_500MA   A_B_DAC2_F

OVERLAP

DDCDATA_DAC2_R
DDCCLK_DAC2_R
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R

R2029   R2028   R2027
37.4R   37.4R   37.4R

R2003   R2002   R2001
75R   75R   75R

C2004   C2005   C2006
8.0pF   8.0pF   8.0pF

+5V_VESA2

C2011   C2010
1uF   68pF

A_R_DAC2_F   A_G_DAC2_F
A_B_DAC2_F

J2
1 2
3 4
5 6
7 8
9 10
A_HSYNC_DAC2_R   11 12
DDCCLK_DAC2_R   13 14   DDCDATA_DAC2_R
                  15 16   A_VSYNC_DAC2_R
Header_16_Pin_2X8

RV710: DDC2 is 5V tolerant. Do not install level shifter.
--> Do not install R2013, R2015, Q2001, Q2002. Install R2014, R2016.
RV810: DDC2 is NOT 5V tolerant. Install level shifter.
--> Do not install R2014, R2016. Install R2013, R2015, Q2001, Q2002.

2X8 HEADER FOR VGA RIBBON CONNECTOR

+3.3V   R2014   0R
         BSH111   +5V_VESA2
R2013   Q2001   R2005
10K   2.2K
                  402
(4) DDC1DATA   R2006   33R 402   DDCDATA_DAC2_R

+3.3V   R2016   0R
         BSH111   +5V_VESA2
R2015   Q2002   R2008
10K   2.2K
                  402
(4) DDC1CLK   R2009   33R 402   DDCCLK_DAC2_R

U1999C
74AHCT125
(3,10) A_HSYNC_DAC2   9   8   A_HSYNC_DAC2_B   R2010   33R 402   A_HSYNC_DAC2_R

C2007
12pF_50V

U1999D
74AHCT125
13, 10
(3,10) A_VSYNC_DAC2   12   11   A_VSYNC_DAC2_B   R2011   33R 402   A_VSYNC_DAC2_R

C2008
12pF_50V

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

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DPE / DPF OUTPUT

+5V_VESA

J1601

Pin	Signal
25	CASE
1	TMDS Data2-
2	TMDS Data2+
3	TMDS Data2/4 Shield
4	TMDS Data4-
5	TMDS Data4+
6	DDC Clock
7	DDC Data
8	Analog VSYNC
9	TMDS Data1-
10	TMDS Data1+
11	TMDS Data1/3 Shield
12	TMDS Data3-
13	TMDS Data3+
14	+5V Power
15	GND (for +5V)
16	Hot Plug Detect
17	TMDS Data0-
18	TMDS Data0+
19	TMDS Data0/5 Shield
20	TMDS Data5-
21	TMDS Data5+
22	TMDS Clock Shield
23	TMDS Clock+
24	TMDS Clock-
C1	Analog Red
C2	Analog Green
C3	Analog Blue
C4	Analog HYNC
C5	Analog GND
C6	Analog GND#C6
26	CASE#26
27	CASE#27
28	CASE#28
29	CASE#29
30	CASE#30

DVI_CONNECTOR

(6) T2X2M C1601 100nF_6.3V R1601 499R T2X2M_C
(6) T2X2P C1602 100nF_6.3V T2X2P_C
(6) T2X4M C1603 100nF_6.3V R1602 499R R1603 499R T2X4M_C
(6) T2X4P C1604 100nF_6.3V R1604 499R T2X4P_C
(17) DDCCLK_DAC1_R DDCCLK_DAC1_R
(17) DDCDATA_DAC1_R DDCDATA_DAC1_R
(17) A_VSYNC_DAC1_R A_VSYNC_DAC1_R
(6) T2X1M C1605 100nF_6.3V R1605 499R T2X1M_C
(6) T2X1P C1606 100nF_6.3V T2X1P_C
(6) T2X3M C1607 100nF_6.3V R1606 499R R1607 499R T2X3M_C
(6) T2X3P C1608 100nF_6.3V R1608 499R T2X3P_C
(6) T2X0M C1609 100nF_6.3V R1609 499R T2X0M_C DVI_HPD
(6) T2X0P C1610 100nF_6.3V T2X0P_C
(6) T2X5M C1611 100nF_6.3V R1610 499R R1611 499R T2X5M_C
(6) T2X5P C1612 100nF_6.3V R1613 499R T2X5P_C
(6) T2XCEP C1613 100nF_6.3V R1612 499R T2XCEP_C
(6) T2XCEM C1614 100nF_6.3V R1614 499R T2XCEM_C

(17) A_R_DAC1_F A_R_DAC1_F
(17) A_G_DAC1_F A_G_DAC1_F
(17) A_B_DAC1_F A_B_DAC1_F
(17) A_HSYNC_DAC1_R A_HSYNC_DAC1_R

U1601 SI2304DS
(14,21) ALL_RAILS_UP

+3.3V

Q1602 MMBT3904
HPD4_IN R1618 10K
(3) HPD4
R1617 10K

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TMDP-B OUTPUT

HDMI CONNECTOR

+5V_VESA

C2710
1uF

(5) TX2P C2701 100nF_6.3V R2701 499R TX2P_C
(5) TX2M C2702 100nF_6.3V R2702 499R TX2M_C
(5) TX1P C2703 100nF_6.3V R2703 499R TX1P_C
(5) TX1M C2704 100nF_6.3V R2704 499R TX1M_C

(5) TX0P C2705 100nF_6.3V R2705 499R TX0P_C
(5) TX0M C2706 100nF_6.3V R2706 499R TX0M_C
(5) TXCAP C2707 100nF_6.3V R2707 499R TXCAP_C
(5) TXCAM C2708 100nF_6.3V R2708 499R TXCAM_C

J2701

		SHELL1	21
1	D2+		
2	D2 Shield		23
3	D2-		
4	D1+		
5	D1 Shield		
6	D1-		
7	D0+		
8	D0 Shield	MEC1	
9	D0-		
10	CK+		
11	CK Shield		
12	CK-		
13	CE Remote		
14	NC		
15	DDC CLK		22
16	DDC DATA		
17	GND		
18	+5V		
19	HP DET	SHELL2	20

CONN-HDMI19P_BLACK-RH-16
N5Y-19M0061-L06

DDC2_CLK_C
DDC2_DATA_C

Q2701
SI2304DS

(14,20) ALL_RAILS_UP

+3.3V
R2717 10K HPD_HDMI1
Q2704
MMBT3904
C2709
68pF

Place C2709 close to J2701

(3) HPD1
R2716
10K

MR2702 0R
+3.3V
R2711 10K
BSH111
Q2702
R2712 2.2K
+5V_VESA
(4) DDC2CLK DDC2_CLK_L R2718 33R

MR2703 0R
+3.3V
R2713 10K
402
BSH111
Q2703
R2714 2.2K
402
+5V_VESA
(4) DDC2DATA DDC2_DATA_L R2719 33R

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AMD

Date: Thursday, May 14, 2009
Rev 2
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Title: RH LP RV710 DDR3 VGA (header) HDMI DVI
Doc No. 105-B890XX-00B

Critial Temperature Fault

CTF TEST CIRCUIT

+12V_BUS

R4055 20K

R4056 3.9R

+3.3V_BUS

VDD_EN   VDD_EN   (11,14)

R4051 1K

Q4010 MMBT3904

2N7002E Q4014

C4013 1uF_6.3V
C4014 1uF_6.3V

Q4008 MMBT3906

R4050 0R

(1,2) PERST#_buf

R4054 1K

Q4013 MMBT3904

CTF_SET2

R4061 20K

Q4016 MMBT3904

R4060 1K

R4043 470K

R4045 10K

CTF_VCNTL

Use on RV810 if low-voltage VDDC latch is used on power sequencing.

DNI

+3.3V_BUS

CTF_GATED2

R4044 1K CTF_SET3

Q4009 MMBT3904

R4047 100K

C4015 1uF_6.3V

R4040 5.1K

DNI

(3) CTF

R4038 2.2K 1%

CTF_TRIP

Q4006 MMBT3904

Q4007 MMBT3904

CTF_FB_CNTL

R4046 5.1K

Debug Only

CTF SHOULD BE ACTIVE HI.

R4039 1K 1%

R4062 0R
DNI

FAN_PWM_INV

Q4017 MMBT3904

R4059 1K

To maximize fan output during CTF trigger.

Fan Control

WARNING!
Be cautious when using a 3-wire fan with this fan control circuit. The negative pin will not always be ground. Some 3-wire fans with tachometers will only work if the negative pin of the fan is ground.

+12V_BUS

B4001 26R_600mA

Alternate to Q4103.

FAN_OUT_N

Vdiff

Q4104 MMBT3904

FAN_VE

Alternate to Q4101 and Q4102.

CUR_SRC

Pfb

Nfb

Q4105A BC857BS

Q4105B BC857BS

Vdiff

+12V_BUS

R4105 1K

C4008 1uF 805 16V Y5V

+12V_BUS

+12V_BUS

R4102 1K

R4104 1M DNI

CUR_SRC

Q4101 MMBT3906

Q4102 MMBT3906

R4107 820R

FAN_OUT_P
FAN_OUT_N

JU4001

This circuit provides a minimum voltage for the fan, independent of PWM input.

+3.3V

R4108 1M DNI

R4100 2.61K

R4103

22K

Vdiff

Q4103 PBSS4350Z

R4109 0R

C4010 10uF DNI

+12V_BUS

R4112 1K

(4) TS_FDO

R4101 10K

Q4100 MMBT3904

R4111 1K

C4100 1nF

FAN_VE

D4100

Pfb

Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

C4102 1.0uF

R4106 1K

R4110 1.5R

FAN_OUT_P

C4103 1uF

FAN_OUT_N

BAT54KFILM

R4113 1K

R4010 0R
DNI

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Date: Tuesday, February 10, 2009

Rev 2

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Title RH LP RV710 DDR3 VGA (header) HDMI DVI

Doc No. 105-B890XX-00B

H1A   RV610_FANSINK

H1B

H1C

H1D

FM1
OPT
F_PAD_X
<New PN>

FM4
OPT
F_PAD_X
<New PN>

FM2
OPT
F_PAD_X
<New PN>

FM6
OPT
F_PAD_X
<New PN>

FM3
OPT
F_PAD_X
<New PN>

FM5
OPT
F_PAD_X
<New PN>

7120036200G

SK1

Socket_RV710-M92_50.8

H3
HEATSINK

H2
RV610_LP_HEATSINK

ASSY1   BRACKET

8020040100G

ASSY2   BRACKET
LP

8020040400G

MT2
MT_Hole_0.136_in.

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

RV610_FANSINK
RV610_FANSINK
RV610_FANSINK

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Date: Friday, May 15, 2009
Rev 2

Sheet 23 of 25

Title RH LP RV710 DDR3 VGA (header) HDMI DVI

Doc No. 105-B890XX-00B

MEMORY CHANNEL A

DDR3 4pcs 64Mx16 (4x128MB)

MEMORY CHANNEL A

DDR3 4pcs 64Mx16 (4x128MB)

RANK0   RANK1

DAC2

CRT1
H/VSync

DDC1

POWER REGULATORS

From +12V
+VDDC, VDDCI,
SPV10, +MVDD

From +12V LINEAR:
+5V_VESA, +5V_SHUNT

From +12V DIRECT:
FAN

From +MVDD Linear (1.1V):
PCIE_VDDC, DPLL_VDDC,
DPx_VDD10

From +3.3V Direct:
VDDR3,

From 3.3V Linear (1.8V)
VDDR4, VDDR5, VDD_CT,
TSVDD, PCIE_VDDR,
PCIE_PVDD, DPLL_PVDD,
VDD1DI, AVDD, DPx_PVDD

+PCIE_SOURCE
+3.3V   +12V_BUS

RBG Filters

VGA
Header

Straps

BIOS

Speed control
& temperature
sense

FAN

GPIO

ROM

Thermal

INTERRUPT

Temp. Sensing

Built-in PWM

GPIO17, GPIO6

D+/D-

TS_FDO

TMDP

DPB

HPD1

DDC2

DDCAUX7

AC Coupling Caps

HDMI

Connector

LVTMDP

DPE/DPF   DL-TMDS

GPIO15, GPIO20

AC Coupling Caps

dDVI

Connector

POWER DELIVERY

Dynamic VDDC

DAC1

CRT1
H/VSync

HPD4

DDCAUX5

RBG Filters

RV710

3.3V_BUS
delayed circuit

SMPS Enable
Circuit

Temperature Critical

CTF

PCI-Express

XTALIN

XTALOUT

Oscillator

XTAL

+3.3V_BUS
+12V_BUS

PCI-Express Bus

RH PCIE RV710 DDR3
VGA(header) + HDMI + DVI

REV 1

6 Layer PCB

	5		4		3		2		1	

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

RV710 ENGINEERING BOARD   REVISION DESCRIPTION

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	2008.12.30	INITIAL RELEASE OF CUSTOM-WIDE BOARD. BASED ON B625 REV06.
1	00B	2009.01.22	Sch no change. just modify HDMI connnecro location on PCB