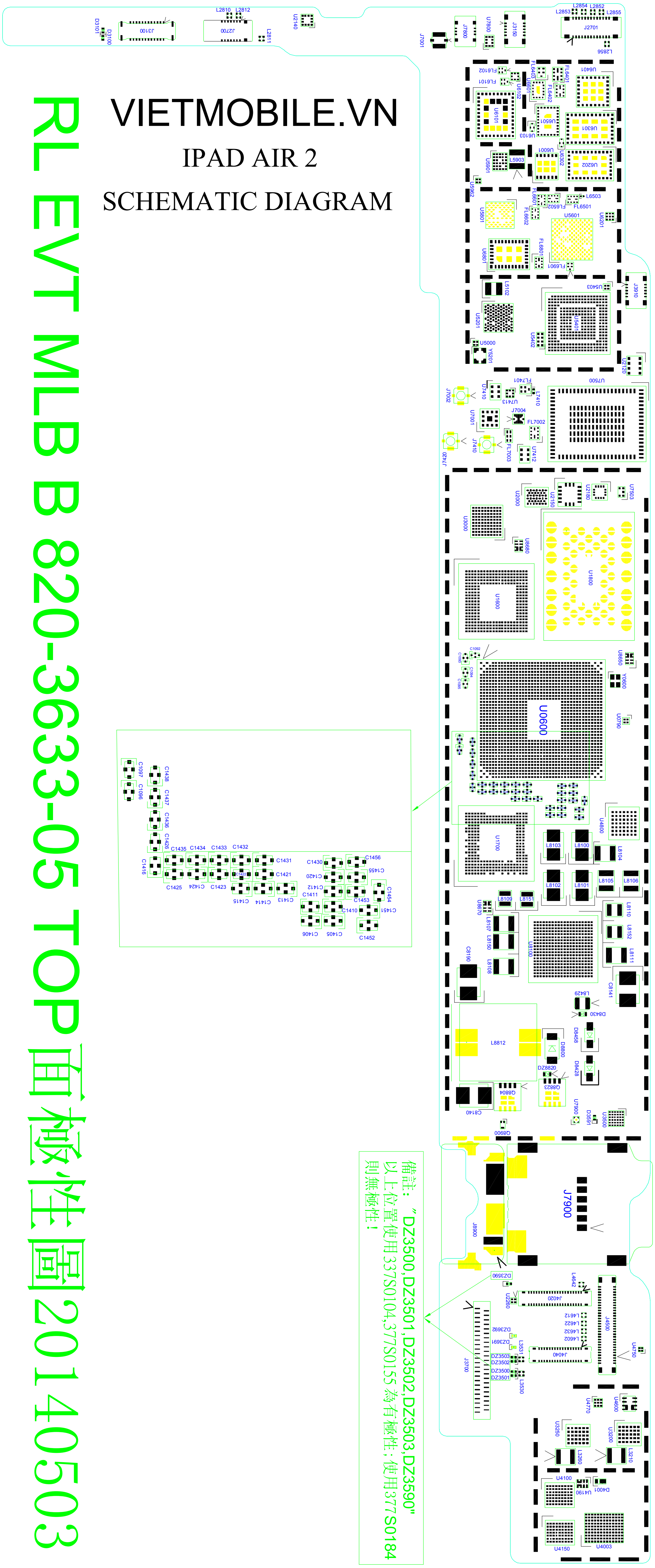
VIETMOBILE.VN

IPAD AIR 2

SCHEMATIC DIAGRAM

RL EVT MLB B 820-3633-05 TOP面極性圖20140503



備註："DZ3500,DZ3501,DZ3502,DZ3503,DZ3590"
以上位置使用377S0104,377S0155為有極性；使用377S0184
則無極性！

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
B	0003279770	PRODUCTION RELEASED	2014-09-29

MLB B - PVT

LAST_MODIFIED=Mon Sep 29 18:09:18 2014

RADIO_MLB SYNC VER 0.109.0
WIFI_DEV SYNC VER 0.68.0
ROTTERDAM SYNC VER 0.11.0

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	TABLE OF CONTENTS	N/A	N/A
2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A
3	4	BOM TABLES	N/A	N/A
4	5	SOC: MISC & ALIASES	N/A	N/A
5	6	SOC: MAIN	N/A	N/A
6	7	SOC: I/OS	N/A	N/A
7	8	SOC: NAND	N/A	N/A
8	9	SOC: MIPI, ISP	N/A	N/A
9	10	SOC: EDP, PCIE	N/A	N/A
10	11	SOC: DDR	N/A	N/A
11	12	SOC: IO POWER	N/A	N/A
12	13	SOC: SOC POWER AND GND	N/A	N/A
13	14	SOC: CPU, GPU, SRAM POWER	N/A	N/A
14	16	DDR: CHANNEL 0 AND 1	N/A	N/A
15	17	DDR: CHANNEL 2 AND 3	N/A	N/A
16	18	NAND	N/A	N/A
17	20	SENSOR: OSCAR	N/A	N/A
18	21	SENSOR: CARBON, PHOS+, MAGN	N/A	N/A
19	22	SENSOR: HALL EFFECT	N/A	N/A
20	27	CAMERA: CAM CONNS	N/A	N/A
21	28	CAMERA: CAM SUPPORT	N/A	N/A
22	30	AUDIO: L81 CODEC	N/A	N/A
23	31	AUDIO: HP/DMIC FLEX CONNS	N/A	N/A
24	32	AUDIO: SPEAKER AMPS	N/A	N/A
25	35	IO: TRISTAR	N/A	N/A
26	36	IO: FILTERS	N/A	N/A
27	37	IO: HOTBAR PADS	N/C	N/A
28	39	IO: BUTTON FLEX CONN	N/A	N/A
29	40	GRAPE: STINGER & CONN	N/A	N/A
30	41	GRAPE: CUMULUS	N/A	N/A
31	45	DISPLAY: CONNECTOR	N/A	N/A
32	46	DISPLAY: EDP SUPPORT	N/A	N/A
33	47	MESA: SUPPORT	N/A	N/A
34	48	ROTTERDAM	ROTTERDAM	05/13/2014
35	50	CELL: PROBE PTS & DEBUG CONN	RADIO	09/29/2014
36	51	CELL: BB PMU (1/2)	RADIO	09/29/2014
37	52	CELL: BB PMU (2/2)	RADIO	09/29/2014
38	53	CELL: BASEBAND (1/2)	RADIO	09/29/2014
39	54	CELL: BASEBAND (2/2)	RADIO	09/29/2014
40	55	CELL: BASEBAND (3/3)	RADIO	09/29/2014
41	56	CELL: RF TXCVR (1/3)	RADIO	09/29/2014
42	57	CELL: RF TXCVR (2/3)	RADIO	09/29/2014
43	58	CELL: RF TXCVR (3/3)	RADIO	09/29/2014
44	59	CELL: QFE DCDC	RADIO	09/29/2014
45	60	CELL: 2G PA	RADIO	09/29/2014
46	61	CELL: VLB PAD	RADIO	09/29/2014
47	62	CELL: LB PAD	RADIO	09/29/2014
48	63	CELL: MB PAD	RADIO	09/29/2014
49	64	CELL: HB PAD	RADIO	09/29/2014
50	65	CELL: ANTENNA SWITCH	RADIO	09/29/2014
51	66	CELL: HB SWITCH	RADIO	09/29/2014
52	67	CELL: RX DIV (1/2)	RADIO	09/29/2014
53	68	CELL: RX DIV (2/2)	RADIO	09/29/2014
54	69	CELL: GPS	RADIO	09/29/2014
55	70	CELL: ANT FEEDS & GPS (J82)	RADIO	09/29/2014
56	74	WIFI/BT: J82 ANT INTERFACE	WIFI	09/29/2014
57	75	WIFI/BT: WIFI/BT MODULE	WIFI	09/29/2014
58	78	SENSOR: HAMMERHEAD	N/A	N/A
59	79	CELL: SIM AND ANT SW FILT	N/A	N/A
60	81	PMU: ARABELA (1/3)	N/A	N/A
61	82	PMU: ARABELA (2/3)	N/A	N/A
62	83	PMU: ARABELA (3/3)	N/A	N/A
63	84	POWER: J82 SPECIFIC	N/A	N/A
64	86	POWER: EXTERNAL SWITCHES	N/A	N/A
65	88	PMU: CHARGER BUCK	N/A	N/A
66	89	POWER: BATTERY CONN	N/A	N/A
67	90	SOC: DEBUG	N/A	N/A
68	91	ALIASES: BB/WLAN/BT	N/A	N/A
69	93	TEST: TPS/HOLES/FIDUCUALS	N/A	N/A
70	95	TEST: EE TP/PP	N/A	N/A
71	96	TEST: CELL EE TP/PP	N/A	N/A
72	121	POWER: ALIASES	N/A	N/A
73	155	BB/WLAN VOLTAGE ATTRIBUTES	N/A	N/A

DRAWING

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-0301	1	SCH,MLB-B,J82	SCH1	CRITICAL	
820-3633	1	PCBF,MLB-B,J82	PCB1	CRITICAL	

DRAWING TITLE: SCHEM,MLB-B,X190

Apple Inc.

DRAWING NUMBER: 051-0301 SIZE: D
REVISION: B.0.0
BRANCH:
PAGE: 1 OF 155
SHEET: 1 OF 73

CAPRI

SPI3

UART8

I2C2

SPI2

I2C1

LPDP

DWI1

UART5 (HDQ)

DWI0

I2C0

GPIO

DDR0 DDR1 DDR2 DDR3

FMI0 FMI1

ISP0
ISP0_I2C
MIPI0C

REAR CAMERA
CSA 27

ISP1
ISP1_I2C
MIPI1C

FRONT CAMERA
CSA 27

I2S4
UART3
PCIE1
UART2

BT / WIFI/BT / WLAN / COEX (CSA)

MIMO

WIFI/BT ANT

WIFI/BT ANT

OSCAR

CELLULAR/ GPS

COEX
UART
HSIC
IPC
UART
USB

HSIC0
GPIO
UART1

NOT ON WIFI-ONLY CONFIG

PRIMARY CELLULAR ANT

DIVERSITY CELLULAR ANT

GPS ANT

SIM CARD

TRISTAR
CSA 35

USB1
UART2
I2C
USB0
UART1
UART0
JTAG
DIG

I2C0

USB2.0
UART0
UART6
JTAG

SPI1
I2S0
I2S1

L81 AUDIO CODEC
CSA 30
SPI
ASP
XSP
MBUS

HP

MIC1

MIC2

I2S3

AMP
CSA 33

AMP
CSA 32

RIGHT SPEAKER
IO FLEX

LEFT SPEAKER
IO FLEX

GRAPE CSA 41
CUMULUS CUMULUS

STINGER
CSA 40 I2C

DISPLAY/ TOUCH PANEL
BACKLIGHT
EDP

I2C MESA
SPI

ALS (MIC) I2C
ALS (AJ) I2C

COMPASS CSA 21 SPI
PHOSPHOROUS+ CSA 21 SPI
GRYO CSA 21 SPI
ACCEL CSA 21 SPI

PROX SENSOR CSA 78 I2C
TEMP SENSOR CSA 78 I2C
HELIUM CSA 78 I2C

OSCAR CSA 20
I2C
SPI (M)
I2C
UART
UART

BASEBAND

PMU ARABELA
CSA 81-83

BMU
BATTERY
HDQ

IRQ
DWI
I2C
GPIO

HALL EFF 1
CSA 22

HALL EFF 2
IO FLEX

BUTTON FLEX
CSA 39

LPDDR3
CSA 16

LPDDR3
CSA 17

NAND FLASH
CSA 18

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
BLOCK DIAGRAM: SYSTEM

Apple Inc.

DRAWING NUMBER 051-0301
SIZE D
REVISION
BRANCH B.0.0

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-7118	1	RADIO FENCE X190	PD_FENCE_RADIO	CRITICAL	MLB_B
806-00001	1	AP FENCE X190	PD_FENCE_AP	CRITICAL	
806-6353	1	GRAPE FENCE X190	PD_FENCE_GRAPE	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-00067	1	EEEE FOR 639-5813 (MLB A 16GB)	EEEE_FQJ3	CRITICAL	EEEE_MLB_A_16GB
825-00067	1	EEEE FOR 639-5814 (MLB A 32GB)	EEEE_FQJ0	CRITICAL	EEEE_MLB_A_32GB
825-00067	1	EEEE FOR 639-5815 (MLB A 64GB)	EEEE_FQJ1	CRITICAL	EEEE_MLB_A_64GB
825-00067	1	EEEE FOR 639-5816 (MLB A 128GB)	EEEE_FQJ2	CRITICAL	EEEE_MLB_A_128GB
825-00067	1	EEEE FOR 639-4747 (MLB B 16GB)	EEEE_FH54	CRITICAL	EEEE_MLB_B_16GB
825-00067	1	EEEE FOR 639-5809 (MLB B 32GB)	EEEE_FQHY	CRITICAL	EEEE_MLB_B_32GB
825-00067	1	EEEE FOR 639-5810 (MLB B 64GB)	EEEE_FQHW	CRITICAL	EEEE_MLB_B_64GB
825-00067	1	EEEE FOR 639-5811 (MLB B 128GB)	EEEE_FQHV	CRITICAL	EEEE_MLB_B_128GB

CKPLUS WAIVE TABLE

CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00016	1	IC,CAPRI,A1,PROD,ASE	U0600	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S00021	343S00016		U0600	IC,CAPRI,A1,PROD,SCK

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0675	1	IC,PMU,ARABELA,D2207A0,TOP-AC,FCBGA380	U8100	CRITICAL	

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0803	2	IC,CAPRI,DRAM,10X10MM,FBGA261	U1600,U1700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0804	333S0803		U1600,U1700	ELPIDA DRAM
333S00014	333S0803		U1600,U1700	SAMSUNG DRAM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0972	1	TOSHIBA 16GB MLC 1YNM PPN1.5	U1800	CRITICAL	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S1035	335S0972	16GB_PROD	U1800	HYNIX 16GB MLC 1YNM PPN1.5

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00011	1	SANDISK 64GB TLC 1YNM PPN1.5	U1800	CRITICAL	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00017	335S00011	64GB_PROD	U1800	TOSHIBA 64GB TLC 1YNM PPN

128GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00012	1	SANDISK 128GB TLC 1YNM PPN1.5	U1800	CRITICAL	128GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00018	335S00012	128GB_PROD	U1800	TOSHIBA 128GB TLC 1YNM PPN

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

BOM TABLES

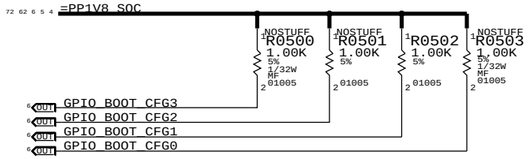
Apple Inc.

DRAWING NUMBER 051-0301 SIZE D

REVISION

BRANCH B.0.0

BOOT CONFIG ID

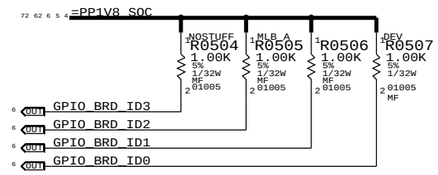


BOOT_CFG[3:0]	MODE
0000	SPI
0001	SPI W/TEST
CURRENT SETTING ---> 0010	NAND
0011	NAND W/TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID



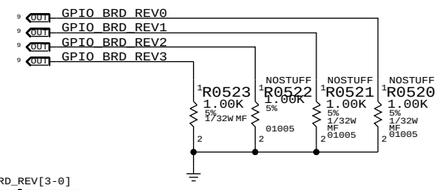
BRD_ID[3-0]	
0000	RESERVED
0001	RESERVED
0010	MLB_B AP
0011	MLB_B DEV
0100	RESERVED
0101	RESERVED
0110	MLB_A AP
0111	MLB_A DEV
1000	UNUSED
1001	UNUSED
1010	UNUSED
1011	UNUSED
1100	RESERVED
1101	RESERVED

RDAR://PROBLEM/15529479

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

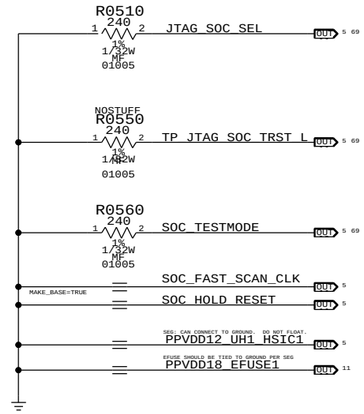
BOARD REVISION

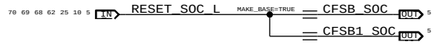


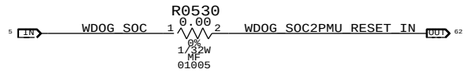
BRD_REV[3-0]	
0000	RESERVED
0001	RESERVED
0010	PROTO 1 (BRING UP)
0011	PROTO 1 (LOCAL/CHINA)
0100	PROTO 2
0101	PRE-EVT
0110	EVT
CURRENT SETTING ---> 0111	DVT & PVT
1000	UNUSED

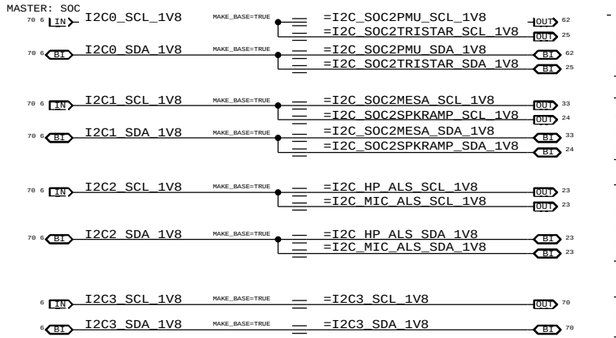
S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ









TO:
ARIADELA ADDR: 0B0111100X
TRISTAR ADDR: 0B0011010X

TO:
MESA EEPROM (MEM) ADDR: 0B1010000X
MESA EEPROM (ID) ADDR: 0B1011000X
SPEAKER AMP LEFT ADDR: 0B0110001X
SPEAKER AMP RIGHT ADDR: 0B0110100X

TO:
ALS(MIC) ADDR: 0B0101001X
ALS(HP) ADDR: 0B1001001X

TO:
PROBE POINTS

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
SOC: MISC & ALIASES

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D
REVISION B.0.0
BRANCH
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ON IN HIBERNATE
VDD1, VDD2, VDDIOD_DDRXCA (VDDCA), VDD12_CKE_DDR0, VDD12_CKE_DDR1

=PP1V2_HSIC_SOC
C0610 0.22UF 20% 6.3V X5R 01005-1
C0611 0.22UF 20% 6.3V X5R 01005-1
C0612 0.22UF 20% 6.3V X5R 01005-1
C0615 0.01UF 10% 6.3V X5R 01005
C0620 100PF 5% 16V NP0-C0G 01005

PPVDD12_UH1_HSIC1

=PP0V95_USB_SOC
C0630 0.01UF 10% 6.3V X5R 01005
C0631 0.22UF 20% 6.3V X5R 01005-1
C0632 100PF 5% 16V NP0-C0G 01005

=PP3V3_USB_SOC
C0640 0.01UF 10% 6.3V X5R 01005
C0645 0.22UF 20% 6.3V X5R 01005-1
C0641 100PF 5% 16V NP0-C0G 01005

H24, AM33: SEG: CAN CONNECT TO GROUND. DO NOT FLOAT. CKPLUS_WAIVE=PWRTERM2GND
F23 VDDH_USB 20MA
J25 VDD095_USB 5MA
H25 VDD33_USB
VDD12_UH0_HSIC0
VDD12_UH1_HSIC1
13MA EACH

U0600
TMKP88A0-N
FCBGA
SYM 4 OF 15
OMIT_TABLE

HSIC_BB_DATA	D25	UH1_HSIC0_DATA	
HSIC_BB_STB	E25	UH1_HSIC0_STB	
NC_HSIC1_DATA (NO_TEST=TRUE)	AV38	UH2_HSIC1_DATA	
NC_HSIC1_STB (NO_TEST=TRUE)	AU38	UH2_HSIC1_STB	
JTAG_SOC_SEL	U37	JTAG_SEL	
NC_JTAG_SOC_TRTCK (NO_TEST=TRUE)	R36	JTAG_TRTCK	
TP_JTAG_SOC_TRST_L	U40	JTAG_TRST*	
TP_JTAG_SOC_TDO	U36	JTAG_TDO	
	T41	JTAG_TDI	
JTAG_SOC_TMS	U38	JTAG_TMS	
JTAG_SOC_TCK	U41	JTAG_TCK	
RESET_SOC_L	AR41	RESET*	
CFSB_SOC	AR39	CFSB	
CFSB1_SOC	AN26	CFSB1	
SOC_HOLD_RESET	AN38		
SOC_TST_CLKOUT	AM40	TST_CLKOUT	
SOC_FAST_SCAN_CLK	AR40	FAST_SCAN_CLK	ALWAYS-ON 1.8V (REQUEST_DFU1_L)
SOC_TESTMODE	AT39	TESTMODE	(REQUEST_DFU2_L)
ANALOGMUXOUT	G35	TP_ANALOGMUXOUT	
USB_DP	B26	USB_SOC_P	
USB_DM	C26	USB_SOC_N	
USB_VBUS (USB_VBUS HAS 70K INPUT IMPEDANCE VIN 5.6V MAX)	F22	USB_VBUS_DETECT_R	
USB_ID	F25	NC_USB_ID (NO_TEST=TRUE)	
USB_REXT	F24	USB_REXT0	
WDOG	AN39	WDOG_SOC	
XI0	H41	XTAL_SOC_24M_I	
XO0	H40	XTAL_SOC_24M_O	
HOLD_KEY*	AP27	GPIO_BTN_ONOFF_L	
MENU_KEY*	AM26	GPIO_BTN_HOME_L	

=PP1V8_SOC
R0610 100K 5% 1/32W MF 01005
R0611 100K 5% 1/32W MF 01005
R0612 100K 5% 1/32W MF 01005

=PP1V8_SOC
R0634 10K 5% 1/32W MF 01005

JTAG_SOC_TDI
JTAG_SOC_TMS
JTAG_SOC_TCK

RESET_SOC_L
C0660 0.01UF 10% 10V X5R-CERM 0201

POWER-ON RESET FAIL SAFE I/O

TP0600 TP-P55

R0630 68.1K 1% 1/32W MF 01005
USB_VBUS_DETECT

R0640 1.00M 1% 1/32W MF 01005
R0641 1.33K 1% 1/32W MF 01005
R0660 200 1% 1/32W MF 01005 PLACE_NEAR=U0600.F24:5MM

CRITICAL Y0600 1.60X1.20MM-SM 24.000MHZ-30PPM-9.5PF-60OHM SOC_24M_O
CRITICAL C0650 12PF 5% 16V CERM 01005 NO_TEST=TRUE
CRITICAL C0651 12PF 5% 16V CERM 01005

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE: SOC: MAIN
Apple Inc.
DRAWING NUMBER: 051-0301 SIZE: D
REVISION: B.0.0
BRANCH:
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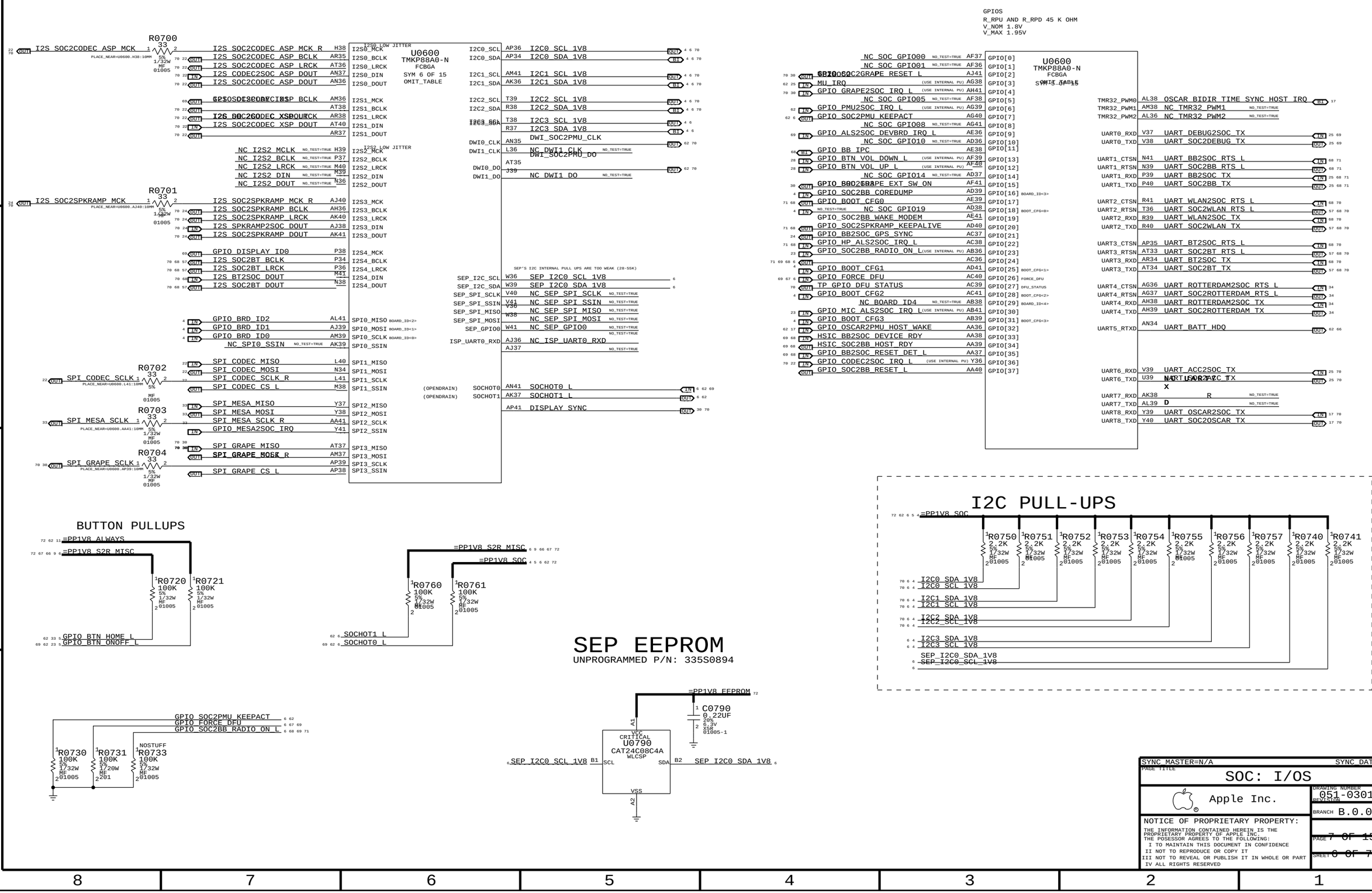
R0700
33
I2S SOC2CODEC ASP MCK
I2S SOC2CODEC ASP MCK R
I2S SOC2CODEC ASP BCLK
I2S SOC2CODEC ASP LRCK
I2S CODEC2SOC ASP DOUT
I2S SOC2CODEC ASP DOUT
GPIO SOC2CODEC ASP BCLK
I2S SOC2CODEC XSP BCLK
I2S SOC2CODEC XSP LRCK
I2S SOC2CODEC XSP DOUT
NC I2S2 MCLK
NC I2S2 BCLK
NC I2S2 LRCK
NC I2S2 DIN
NC I2S2 DOUT
R0701
33
I2S SOC2SPKRAMP MCK
I2S SOC2SPKRAMP MCK R
I2S SOC2SPKRAMP BCLK
I2S SOC2SPKRAMP LRCK
I2S SPKRAMP2SOC DOUT
I2S SOC2SPKRAMP DOUT
GPIO DISPLAY ID0
I2S SOC2BT BCLK
I2S SOC2BT LRCK
I2S BT2SOC DOUT
I2S SOC2BT DOUT
GPIO BRD ID2
GPIO BRD ID1
GPIO BRD ID0
NC SPI0 SSIN
R0702
33
SPI CODEC SCLK
SPI CODEC MISO
SPI CODEC MOSI
SPI CODEC SCLK R
SPI CODEC CS L
R0703
33
SPI MESA SCLK
SPI MESA MISO
SPI MESA MOSI
SPI MESA SCLK R
GPIO MESA2SOC IRQ
R0704
33
SPI GRAPE SCLK
SPI GRAPE MISO
SPI GRAPE MOSI R
SPI GRAPE CS L
U0600
TMKP88A0-N
FCBGA
SYM 6 OF 15
OMIT_TABLE
I2S0 LOW JITTER
I2S0_MCK
I2S0_BCLK
I2S0_LRCK
I2S0_DIN
I2S0_DOUT
I2S1_MCK
I2S1_BCLK
I2S1_LRCK
I2S1_DIN
I2S1_DOUT
I2S2 LOW JITTER
I2S2_MCK
I2S2_BCLK
I2S2_LRCK
I2S2_DIN
I2S2_DOUT
I2S3_MCK
I2S3_BCLK
I2S3_LRCK
I2S3_DIN
I2S3_DOUT
I2S4_MCK
I2S4_BCLK
I2S4_LRCK
I2S4_DIN
I2S4_DOUT
SPI0_MISO
SPI0_MOSI
SPI0_SCLK
SPI0_SSIN
SPI1_MISO
SPI1_MOSI
SPI1_SCLK
SPI1_SSIN
SPI2_MISO
SPI2_MOSI
SPI2_SCLK
SPI2_SSIN
SPI3_MISO
SPI3_MOSI
SPI3_SCLK
SPI3_SSIN
I2C0_SCL
I2C0_SDA
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA
I2C3_SCL
I2C3_SDA
DWI0_CLK
DWI1_CLK
DWI0_DO
DWI1_DO
DWI_SOC2PMU_CLK
NC DWI1 CLK
DWI_SOC2PMU_DO
NC DWI1 DO
SEP'S I2C INTERNAL PULL UPS ARE TOO WEAK (28-55K)
SEP_I2C_SCL
SEP_I2C_SDA
SEP_SPI_SCLK
SEP_SPI_SSIN
SEP_SPI_MISO
SEP_SPI_MOSI
SEP_GPIO0
ISP_UART0_RXD
NC SEP I2C0 SCL 1V8
NC SEP I2C0 SDA 1V8
NC SEP SPI SCLK
NC SEP SPI SSIN
NC SEP SPI MISO
NC SEP SPI MOSI
NC SEP GPIO0
NC ISP UART0 RXD
SOCHOT0
SOCHOT1
DISPLAY SYNC
SOCHOT0 L
SOCHOT1 L
GPIOS
R_RPU AND R_RPD 45 K OHM
V_NOM 1.8V
V_MAX 1.95V
GPIO SOC2PMU KEEPACT
GPIO FORCE DFU
GPIO SOC2BB RADIO ON L
GPIO BB IPC
GPIO BTN VOL DOWN L
GPIO BTN VOL UP L
GPIO BOOT CFG0
GPIO SOC2SPKRAMP KEEPALIVE
GPIO BB2SOC GPS SYNC
GPIO HP ALS2SOC IRQ L
GPIO BOOT CFG1
GPIO FORCE DFU
TP GPIO DFU STATUS
GPIO BOOT CFG2
GPIO MIC ALS2SOC IRQ L
GPIO BOOT CFG3
GPIO OSCAR2PMU HOST WAKE
HSIC BB2SOC DEVICE RDY
HSIC SOC2BB HOST RDY
GPIO BB2SOC RESET DET L
GPIO CODEC2SOC IRQ L
GPIO SOC2BB RESET L
U0600
TMKP88A0-N
FCBGA
SYM 5 OF 15
GPIO[0]
GPIO[1]
GPIO[2]
GPIO[3]
GPIO[4]
GPIO[5]
GPIO[6]
GPIO[7]
GPIO[8]
GPIO[9]
GPIO[10]
GPIO[11]
GPIO[12]
GPIO[13]
GPIO[14]
GPIO[15]
GPIO[16]
GPIO[17]
GPIO[18]
GPIO[19]
GPIO[20]
GPIO[21]
GPIO[22]
GPIO[23]
GPIO[24]
GPIO[25]
GPIO[26]
GPIO[27]
GPIO[28]
GPIO[29]
GPIO[30]
GPIO[31]
GPIO[32]
GPIO[33]
GPIO[34]
GPIO[35]
GPIO[36]
GPIO[37]
NC SOC GPIO00
NC SOC GPIO01
GPIO GRAPE2SOC RESET L
MU IRQ
GPIO GRAPE2SOC IRQ L
NC SOC GPIO05
GPIO PMU2SOC IRQ L
GPIO SOC2PMU KEEPACT
NC SOC GPIO08
GPIO ALS2SOC DEVBRD IRQ L
NC SOC GPIO10
GPIO BB IPC
GPIO BTN VOL DOWN L
GPIO BTN VOL UP L
NC SOC GPIO14
GPIO GRAPE EXT SW ON
GPIO SOC2BB COREDUMP
GPIO BOOT CFG0
NC SOC GPIO19
GPIO SOC2BB WAKE MODEM
GPIO SOC2SPKRAMP KEEPALIVE
GPIO BB2SOC GPS SYNC
GPIO HP ALS2SOC IRQ L
GPIO SOC2BB RADIO ON L
NC BOARD ID4
GPIO MIC ALS2SOC IRQ L
GPIO BOOT CFG3
GPIO OSCAR2PMU HOST WAKE
HSIC BB2SOC DEVICE RDY
HSIC SOC2BB HOST RDY
GPIO BB2SOC RESET DET L
GPIO CODEC2SOC IRQ L
GPIO SOC2BB RESET L
TMR32_PWM0
TMR32_PWM1
TMR32_PWM2
UART0_RXD
UART0_TXD
UART1_CTSN
UART1_RTSN
UART1_RXD
UART1_TXD
UART2_CTSN
UART2_RTSN
UART2_RXD
UART2_TXD
UART3_CTSN
UART3_RTSN
UART3_RXD
UART3_TXD
UART4_CTSN
UART4_RTSN
UART4_RXD
UART4_TXD
UART5_RTXD
UART6_RXD
UART6_TXD
UART7_RXD
UART7_TXD
UART8_RXD
UART8_TXD
OSCAR BIDIR TIME SYNC HOST IRQ
NC TMR32 PWM1
NC TMR32 PWM2
UART DEBUG2SOC TX
UART SOC2DEBUG TX
UART BB2SOC RTS L
UART SOC2BB RTS L
UART BB2SOC TX
UART SOC2BB TX
UART WLAN2SOC RTS L
UART SOC2WLAN RTS L
UART WLAN2SOC TX
UART SOC2WLAN TX
UART BT2SOC RTS L
UART SOC2BT RTS L
UART BT2SOC TX
UART SOC2BT TX
UART ROTTERDAM2SOC RTS L
UART SOC2ROTTERDAM RTS L
UART ROTTERDAM2SOC TX
UART SOC2ROTTERDAM TX
UART BATT HDQ
UART ACC2SOC TX
UART SOC2ACC TX
UART OSCAR2SOC TX
UART SOC2OSCAR TX
BUTTON PULLUPS
=PP1V8 ALWAYS
=PP1V8 S2R MISC
R0720
100K
R0721
100K
GPIO BTN HOME L
GPIO BTN ONOFF L
=PP1V8 S2R MISC
=PP1V8 SOC
R0760
100K
R0761
100K
SOCHOT1 L
SOCHOT0 L
SEP EEPROM
UNPROGRAMMED P/N: 335S0894
=PP1V8 EEPROM
C0790
0.22UF
U0790
CAT24C08C4A
WLCSP
SCL
SDA
VCC
VSS
SEP I2C0 SCL 1V8
SEP I2C0 SDA 1V8
R0730
100K
R0731
100K
R0733
100K
NOSTUFF
I2C PULL-UPS
=PP1V8 SOC
R0750
2.2K
R0751
2.2K
R0752
2.2K
R0753
2.2K
R0754
2.2K
R0755
2.2K
R0756
2.2K
R0757
2.2K
R0740
2.2K
R0741
2.2K
I2C0 SDA 1V8
I2C0 SCL 1V8
I2C1 SDA 1V8
I2C1 SCL 1V8
I2C2 SDA 1V8
I2C2 SCL 1V8
I2C3 SDA 1V8
I2C3 SCL 1V8
SEP I2C0 SDA 1V8
SEP I2C0 SCL 1V8
SYNC MASTER=N/A
SYNC DATE=N/A
PAGE TITLE
SOC: I/OS
Apple Inc.
DRAWING NUMBER 051-0301
SIZE D
REVISION
BRANCH B.0.0
PAGE 7 OF 155
SHEET 6 OF 73
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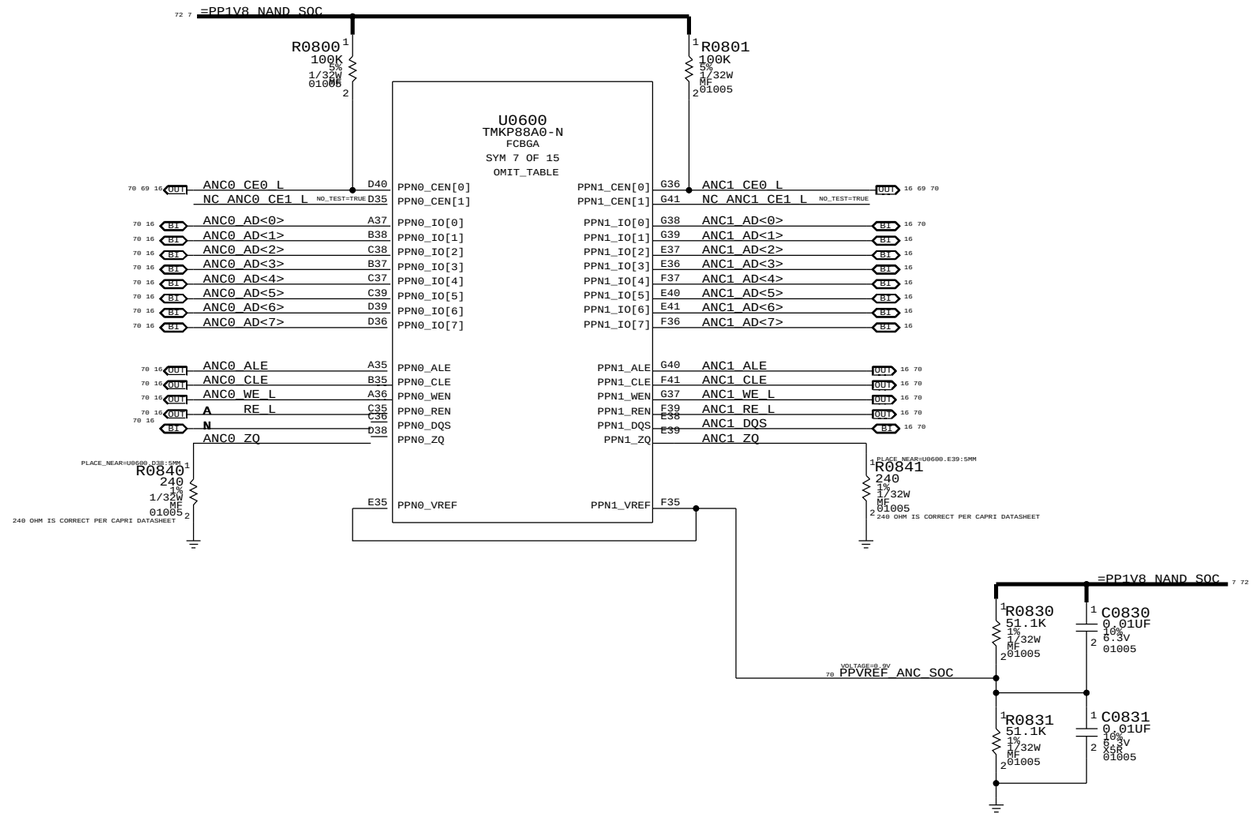

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PAGE TITLE	SOC: NAND
Apple Inc.	DRAWING NUMBER 051-0301 SIZE D
	REVISION BRANCH B.0.0
NOTICE OF PROPRIETARY PROPERTY:	PAGE 8 OF 155
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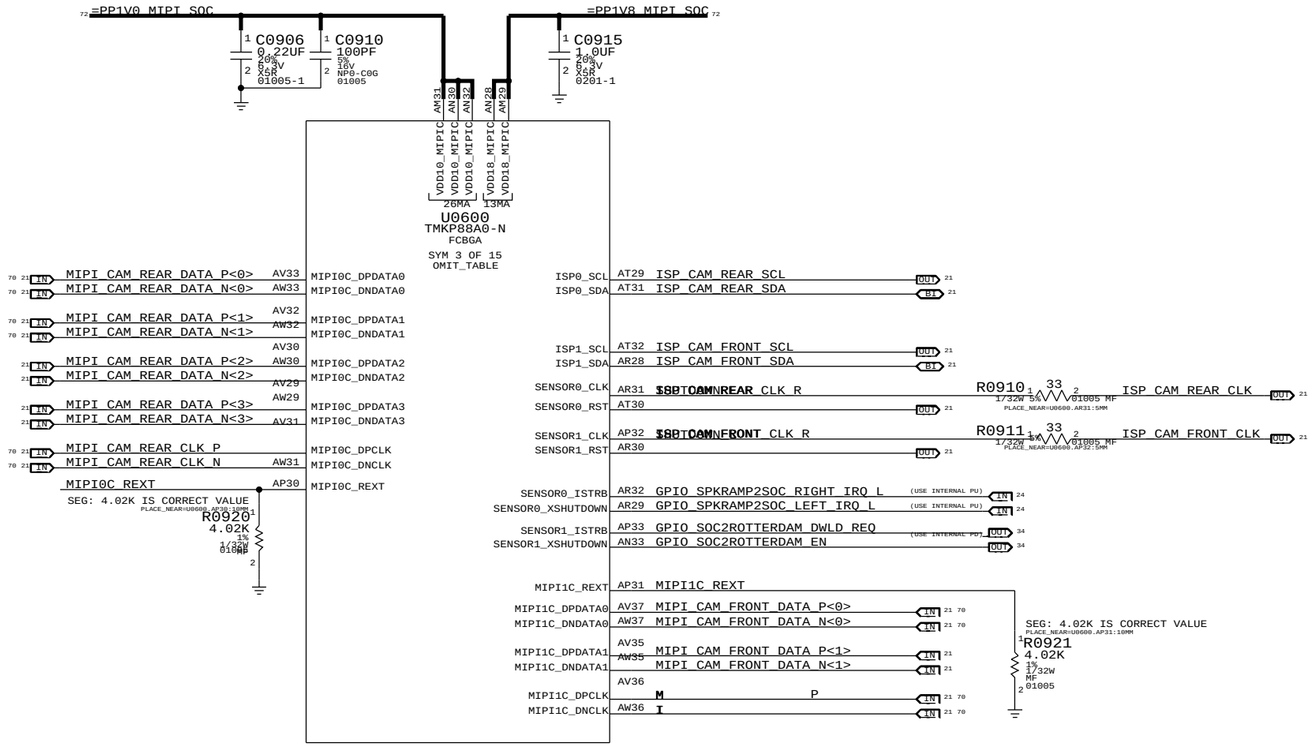

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PAGE TITLE

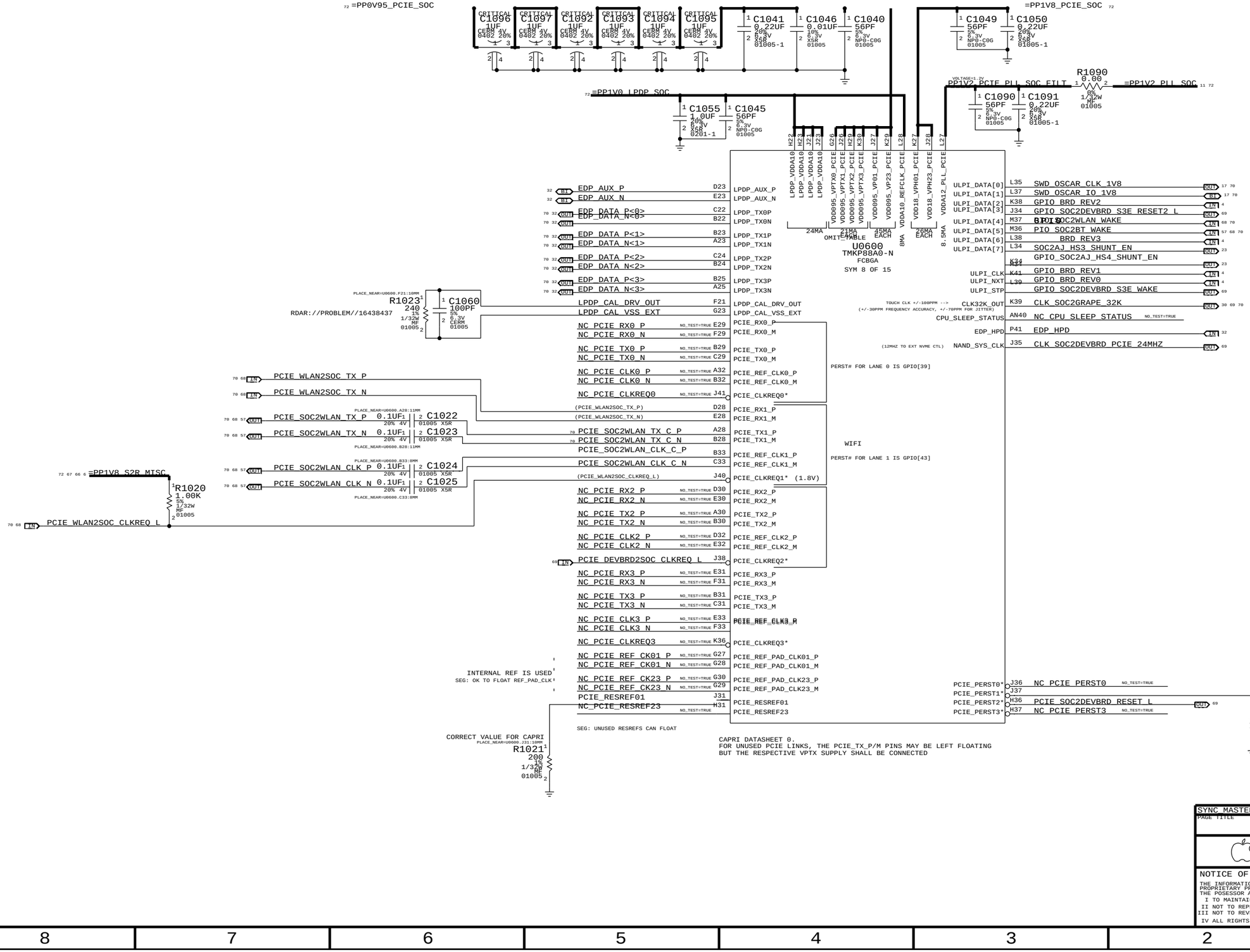
SOC: MIPI, ISP

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D

REVISION

BRANCH B.0.0


=PP0V95_PCIE_SOC
C1096 1UF CERM 4V 0402 20%
C1097 1UF CERM 4V 0402 20%
C1092 1UF CERM 4V 0402 20%
C1093 1UF CERM 4V 0402 20%
C1094 1UF CERM 4V 0402 20%
C1095 1UF CERM 4V 0402 20%
C1041 0.22UF 20% 6.3V X5R 01005-1
C1046 0.01UF 10% 6.3V X5R 01005
C1040 56PF 5% 6.3V NP0-C0G 01005
C1049 56PF 5% 6.3V NP0-C0G 01005
C1050 0.22UF 20% 6.3V X5R 01005-1
=PP1V8_PCIE_SOC
=PP1V0_LPDP_SOC
C1055 1.0UF 20% 6.3V X5R 0201-1
C1045 56PF 5% 6.3V NP0-C0G 01005
PP1V2_PCIE_PLL_SOC_FILT
R1090 0.00 5% 1/32W MF 01005
=PP1V2_PLL_SOC
C1090 56PF 5% 6.3V NP0-C0G 01005
C1091 0.22UF 20% 6.3V X5R 01005-1
LPDP_VDDA10
VDD095_VPTX0_PCIE
VDD095_VPTX1_PCIE
VDD095_VPTX2_PCIE
VDD095_VPTX3_PCIE
VDD095_VP01_PCIE
VDD095_VP23_PCIE
VDDA10_REFCLK_PCIE
VDD18_VPH01_PCIE
VDD18_VPH23_PCIE
VDDA12_PLL_PCIE
24MA
21MA EACH
OMITTABLE
45MA EACH
8MA
26MA EACH
8.5MA
U0600
TMKP88A0-N
FCBGA
SYM 8 OF 15
EDP_AUX_P
EDP_AUX_N
EDP_DATA_P<0>
EDP_DATA_N<0>
EDP_DATA_P<1>
EDP_DATA_N<1>
EDP_DATA_P<2>
EDP_DATA_N<2>
EDP_DATA_P<3>
EDP_DATA_N<3>
LPDP_CAL_DRV_OUT
LPDP_CAL_VSS_EXT
R1023 240 1% 1/32W MF 01005
C1060 100PF 5% 6.3V CERM 01005
RDAR://PROBLEM//16438437
NC_PCIE_RX0_P
NC_PCIE_RX0_N
NC_PCIE_TX0_P
NC_PCIE_TX0_N
NC_PCIE_CLK0_P
NC_PCIE_CLK0_N
NC_PCIE_CLKREQ0
PCIE_WLAN2SOC_TX_P
PCIE_WLAN2SOC_TX_N
PCIE_SOC2WLAN_TX_P
PCIE_SOC2WLAN_TX_N
C1022 0.1UF 20% 4V 01005 X5R
C1023 0.1UF 20% 4V 01005 X5R
PCIE_SOC2WLAN_TX_C_P
PCIE_SOC2WLAN_TX_C_N
PCIE_SOC2WLAN_CLK_C_P
PCIE_SOC2WLAN_CLK_C_N
C1024 0.1UF 20% 4V 01005 X5R
C1025 0.1UF 20% 4V 01005 X5R
PCIE_SOC2WLAN_CLK_P
PCIE_SOC2WLAN_CLK_N
=PP1V8_S2R_MISC
R1020 1.00K 5% 1/32W MF 01005
PCIE_WLAN2SOC_CLKREQ_L
(PCIE_WLAN2SOC_TX_P)
(PCIE_WLAN2SOC_TX_N)
(PCIE_WLAN2SOC_CLKREQ_L)
PCIE_DEVBRD2SOC_CLKREQ_L
NC_PCIE_RX2_P
NC_PCIE_RX2_N
NC_PCIE_TX2_P
NC_PCIE_TX2_N
NC_PCIE_CLK2_P
NC_PCIE_CLK2_N
NC_PCIE_RX3_P
NC_PCIE_RX3_N
NC_PCIE_TX3_P
NC_PCIE_TX3_N
NC_PCIE_CLK3_P
NC_PCIE_CLK3_N
NC_PCIE_CLKREQ3
NC_PCIE_REF_CK01_P
NC_PCIE_REF_CK01_N
NC_PCIE_REF_CK23_P
NC_PCIE_REF_CK23_N
PCIE_RESREF01
NC_PCIE_RESREF23
INTERNAL REF IS USED
SEG: OK TO FLOAT REF_PAD_CLK
SEG: UNUSED RESREFS CAN FLOAT
CORRECT VALUE FOR CAPRI
R1021 200 1% 1/32W MF 01005
PERST# FOR LANE 0 IS GPIO[39]
WIFI
PERST# FOR LANE 1 IS GPIO[43]
CAPRI DATASHEET 0.
FOR UNUSED PCIE LINKS, THE PCIE_TX_P/M PINS MAY BE LEFT FLOATING
BUT THE RESPECTIVE VPTX SUPPLY SHALL BE CONNECTED
ULPI_DATA[0]
ULPI_DATA[1]
ULPI_DATA[2]
ULPI_DATA[3]
ULPI_DATA[4]
ULPI_DATA[5]
ULPI_DATA[6]
ULPI_DATA[7]
ULPI_CLK
ULPI_NXT
ULPI_STP
SWD_OSCAR_CLK_1V8
SWD_OSCAR_IO_1V8
GPIO_BRD_REV2
GPIO_SOC2DEVBRD_S3E_RESET2_L
GPIO_SOC2WLAN_WAKE
PIO_SOC2BT_WAKE
BRD_REV3
SOC2AJ_HS3_SHUNT_EN
GPIO_SOC2AJ_HS4_SHUNT_EN
GPIO_BRD_REV1
GPIO_BRD_REV0
GPIO_SOC2DEVBRD_S3E_WAKE
CLK32K_OUT
CPU_SLEEP_STATUS
EDP_HPD
NAND_SYS_CLK
CLK_SOC2GRAPE_32K
NC_CPU_SLEEP_STATUS
CLK_SOC2DEVBRD_PCIE_24MHZ
PCIE_PERST0*
PCIE_PERST1*
PCIE_PERST2*
PCIE_PERST3*
NC_PCIE_PERST0
NC_PCIE_PERST3
PCIE_SOC2DEVBRD_RESET_L
PCIE_SOC2WLAN_RESET_L
R1022 100K 5% 1/32W MF 01005
SYNC_MASTER=N/A
SYNC_DATE=N/A
PAGE TITLE
SOC: EDP, PCIE
Apple Inc.
DRAWING NUMBER 051-0301
SIZE D
REVISION
BRANCH B.0.0
PAGE 10 OF 155
SHEET 9 OF 79
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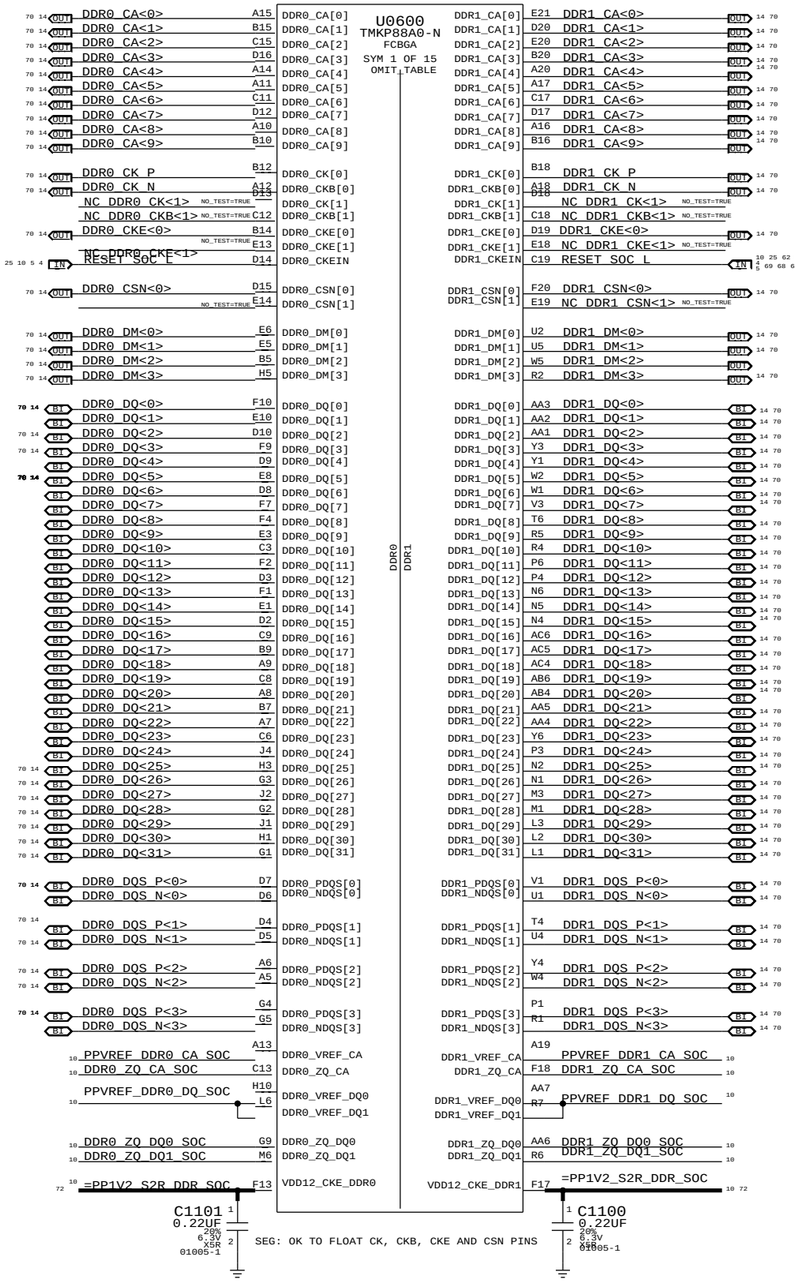
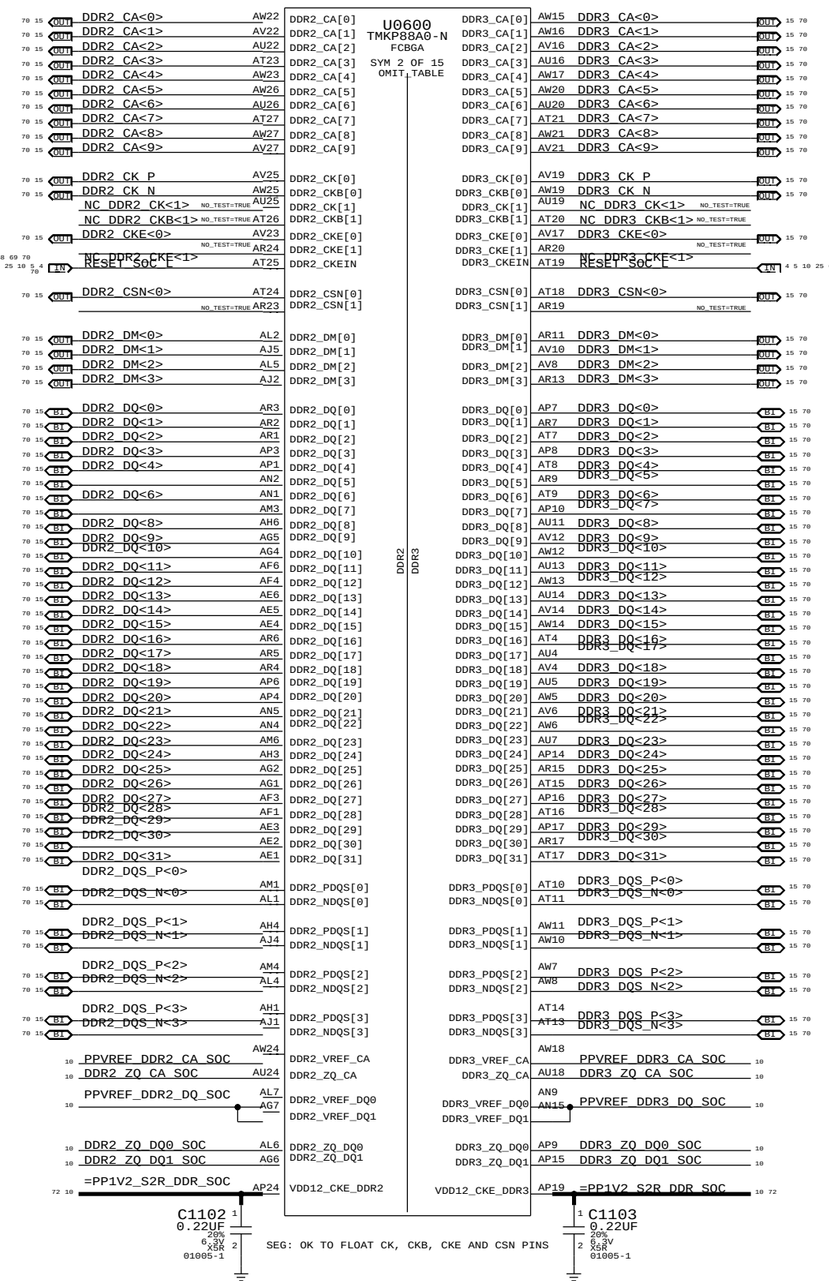
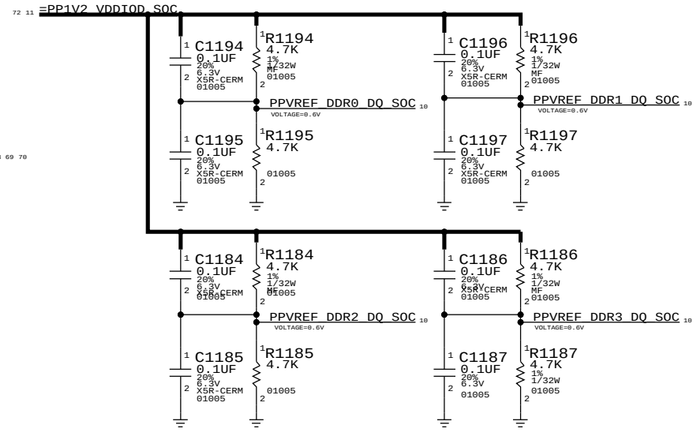
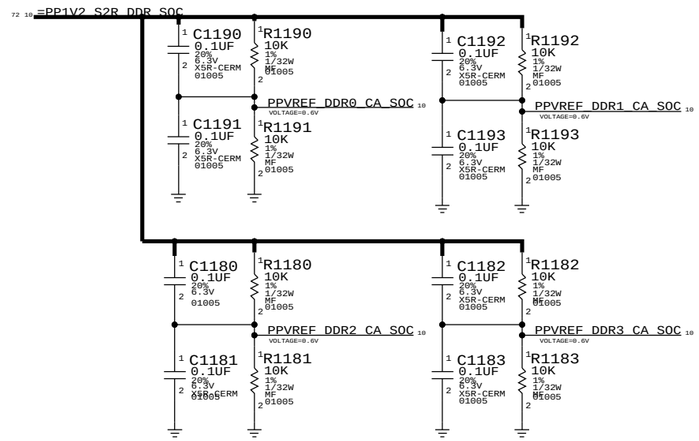






ONCE ROUTED SEG NEEDS TO CHECK PI OF *_VREF_DQ0 AND *_VREF_DQ1 BEING TIED TOGETHER



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

SOC: DDR

Apple Inc.

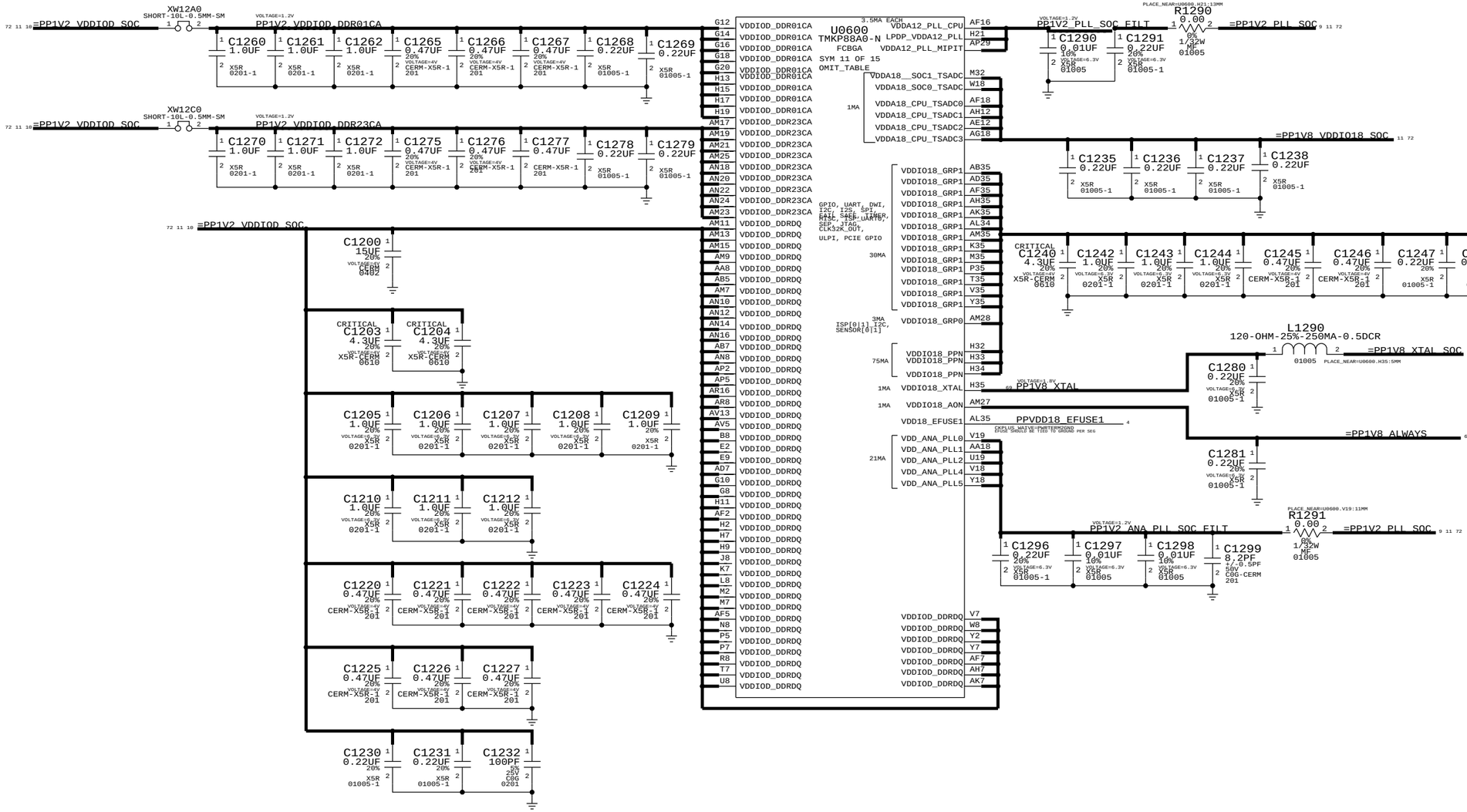
DRAWING NUMBER 051-0301 SIZE D

REVISION B.0.0

BRANCH

PAGE 11 OF 155

SHEET 10 OF 73



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657			QTY 22 RDAR://PROBLEM/8837828
138S0702	138S0657			QTY 22 RDAR://PROBLEM/8837828

REFDES FOR ALTERATIVE TABLE

C1203,C1204,C1240, C1305-C1308, C1404-C1409,C1464-C1469,C1445,C1446

C1602,C1603,C1642,C1643, C1702,C1703,C1742,C1743

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

SOC: IO POWER

Apple Inc.

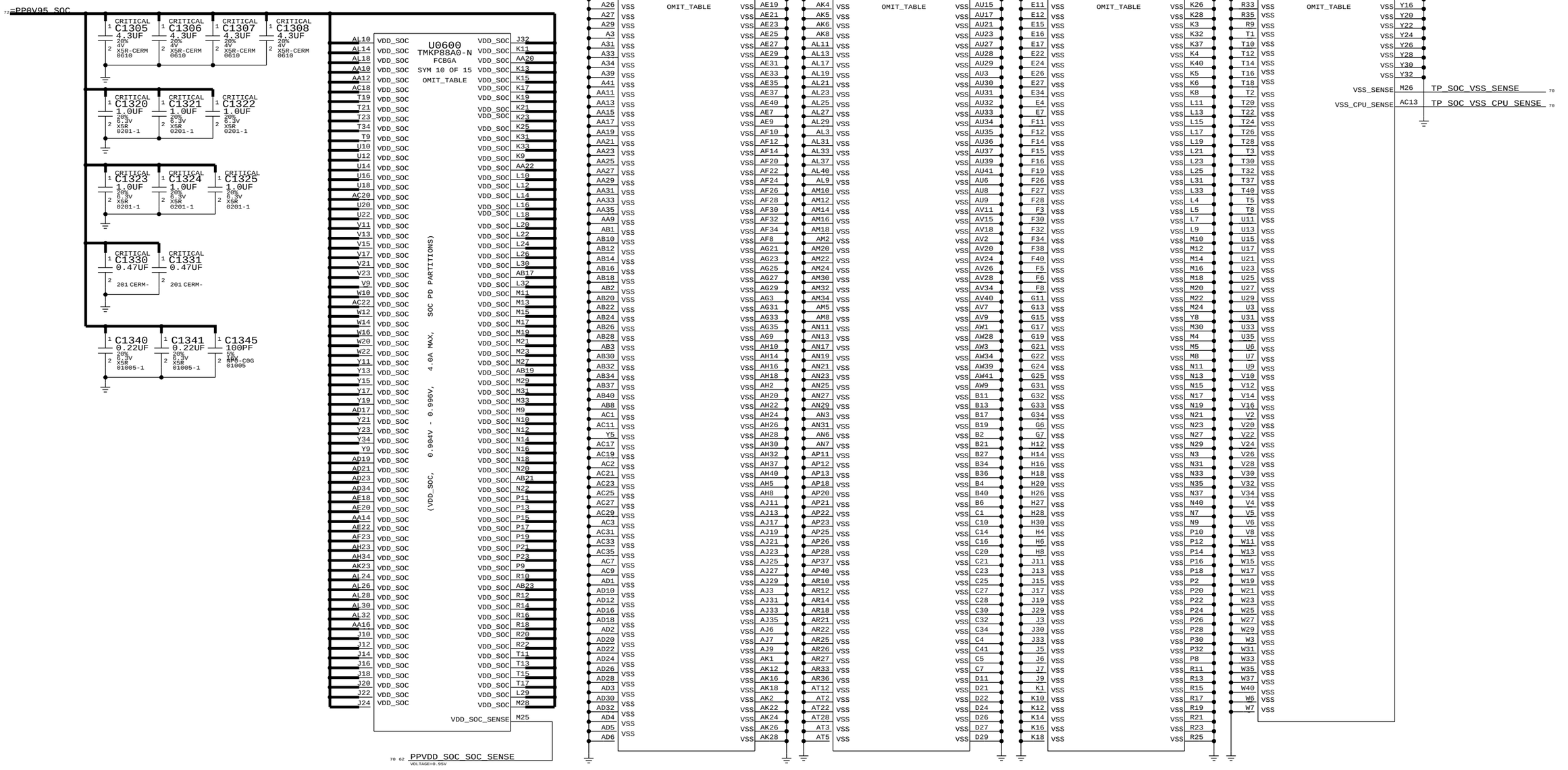
DRAWING NUMBER 051-0301 SIZE D

REVISION B.0.0

BRANCH

PAGE 12 OF 155

SHEET 11 OF 73



SYNC_MASTER=N/A		SYNC_DATE=N/A
PAGE TITLE: SOC: SOC POWER AND GND		
Apple Inc.	DRAWING NUMBER: 051-0301	SIZE: D
	REVISION: B.0.0	
	BRANCH:	
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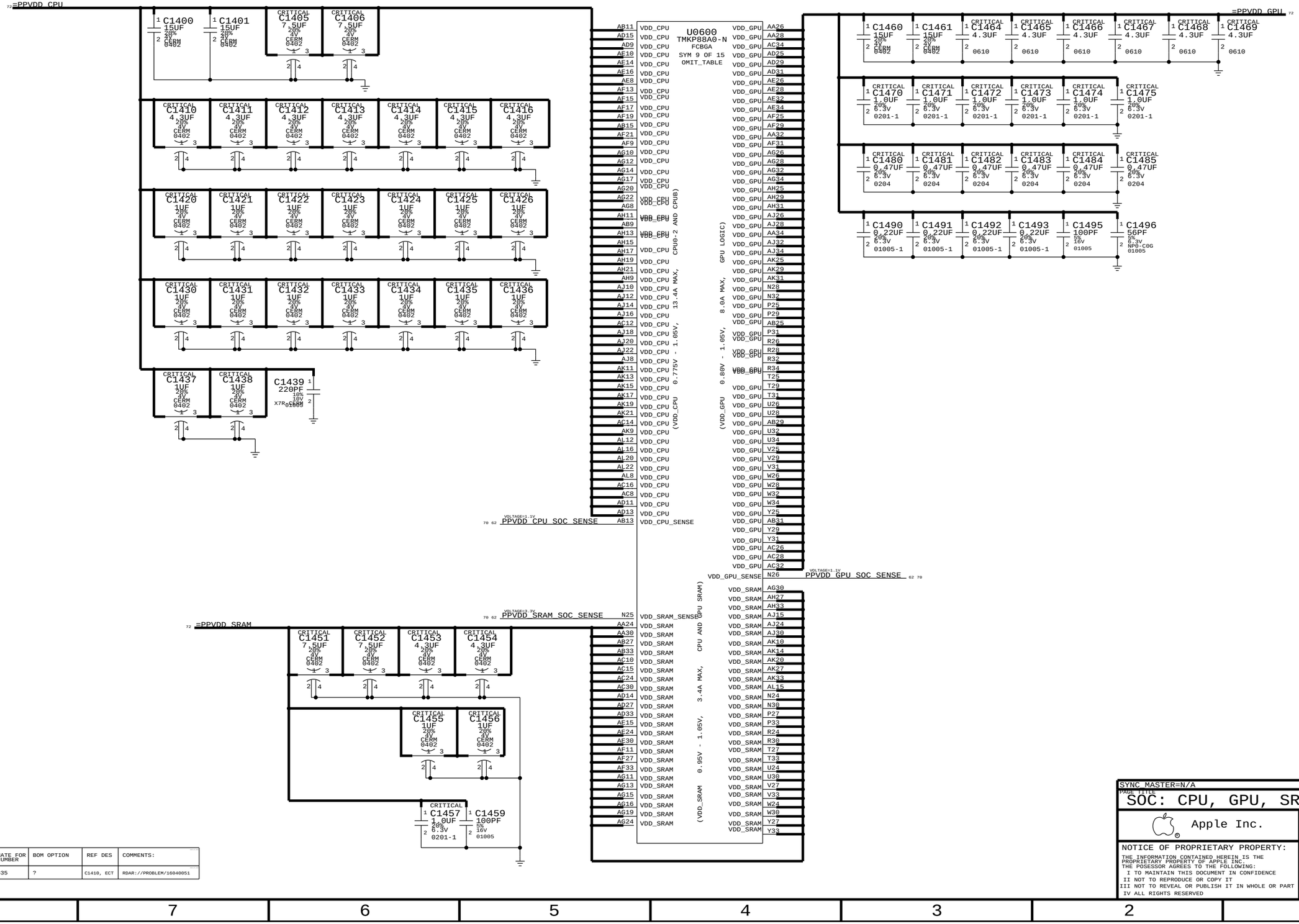
	SHEET: 12 OF 73	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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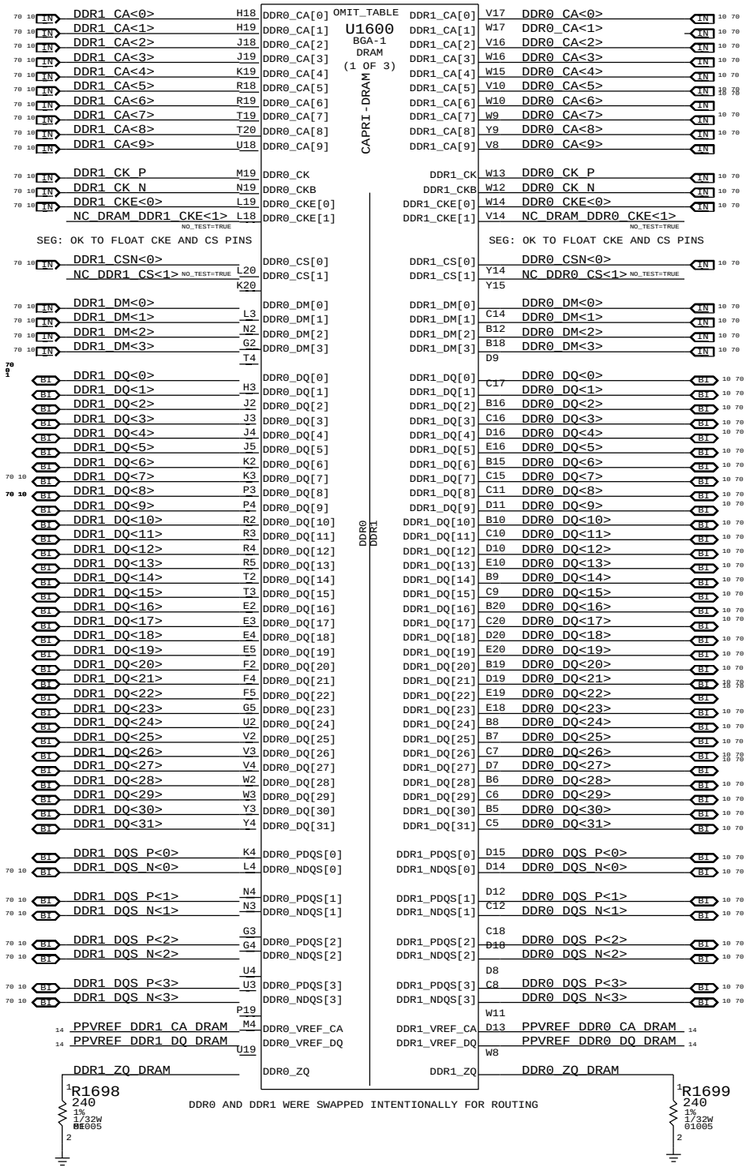
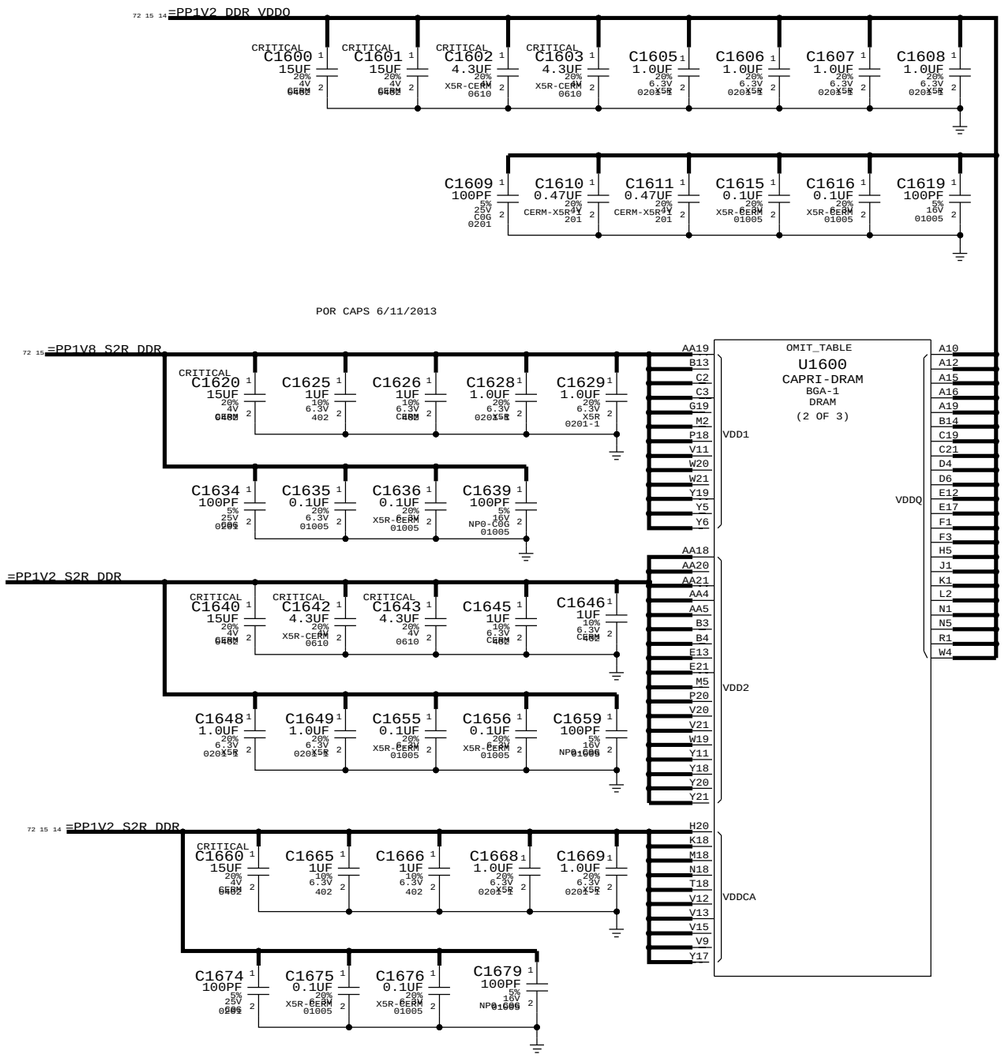
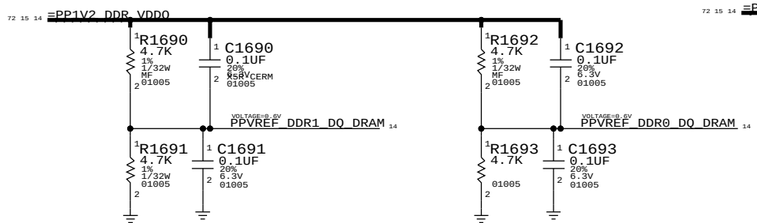
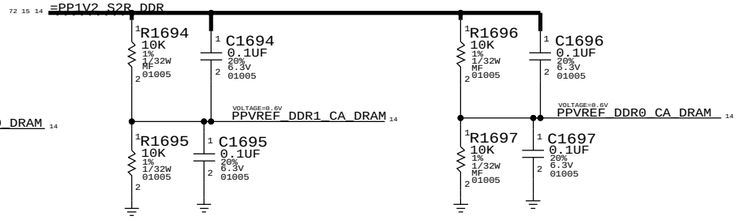








SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

DDR: CHANNEL 0 AND 1

Apple Inc.

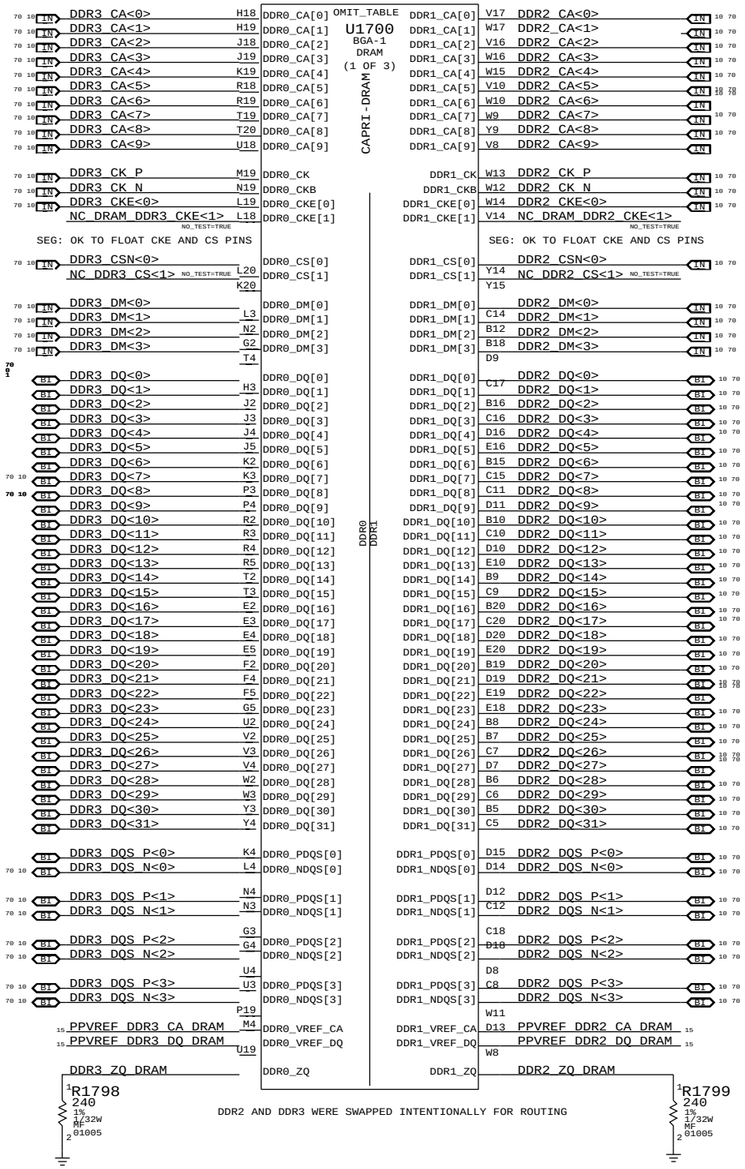
DRAWING NUMBER 051-0301 SIZE D

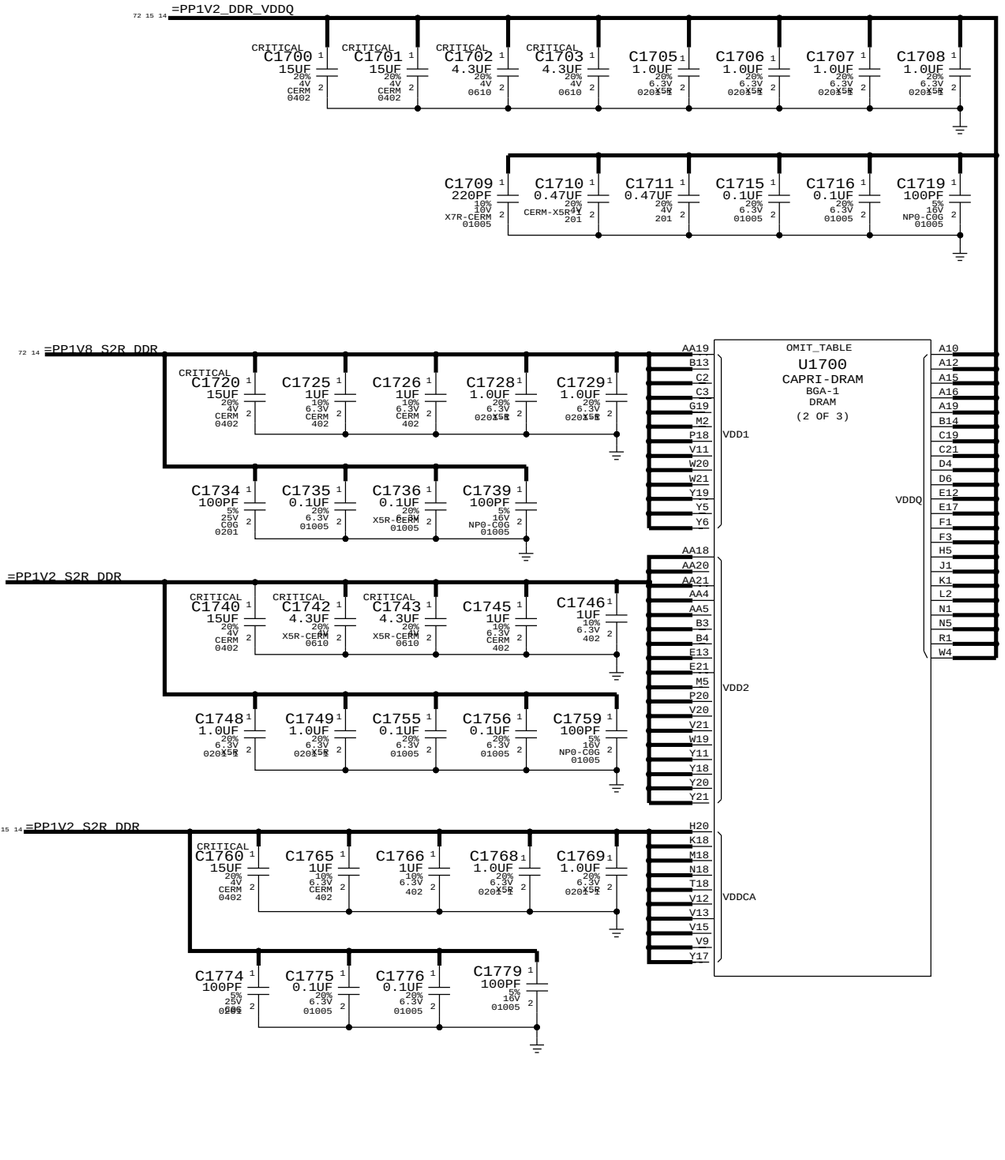
REVISION

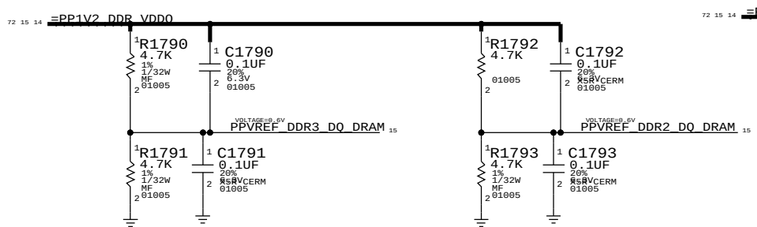
BRANCH B.0.0

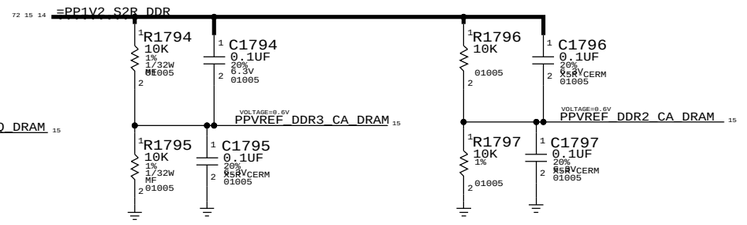
PAGE 16 OF 155

SHEET 14 OF 73









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PAGE TITLE

DDR: CHANNEL 2 AND 3

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D

REVISION

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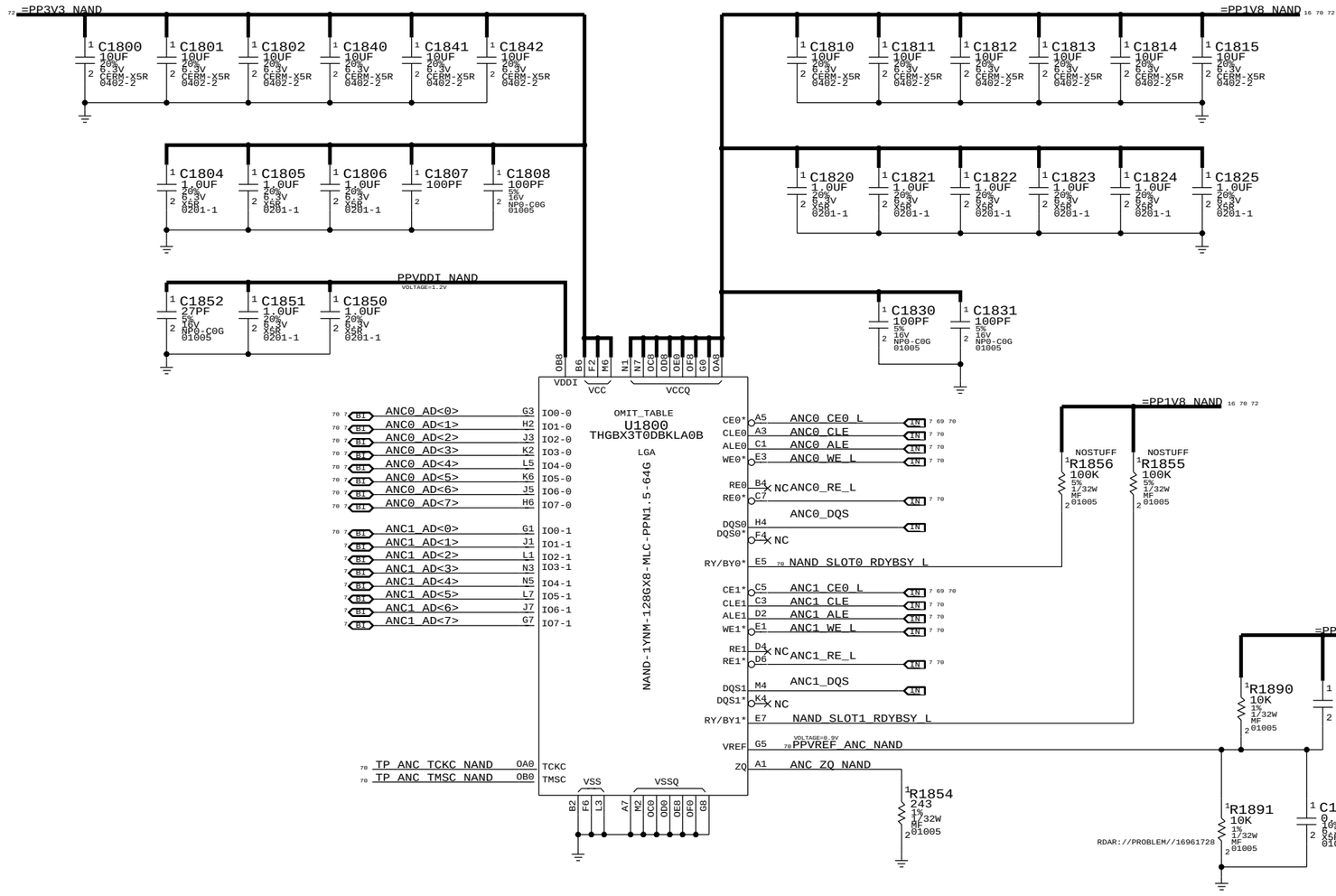

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PAGE TITLE

NAND

Apple Inc.

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OSCAR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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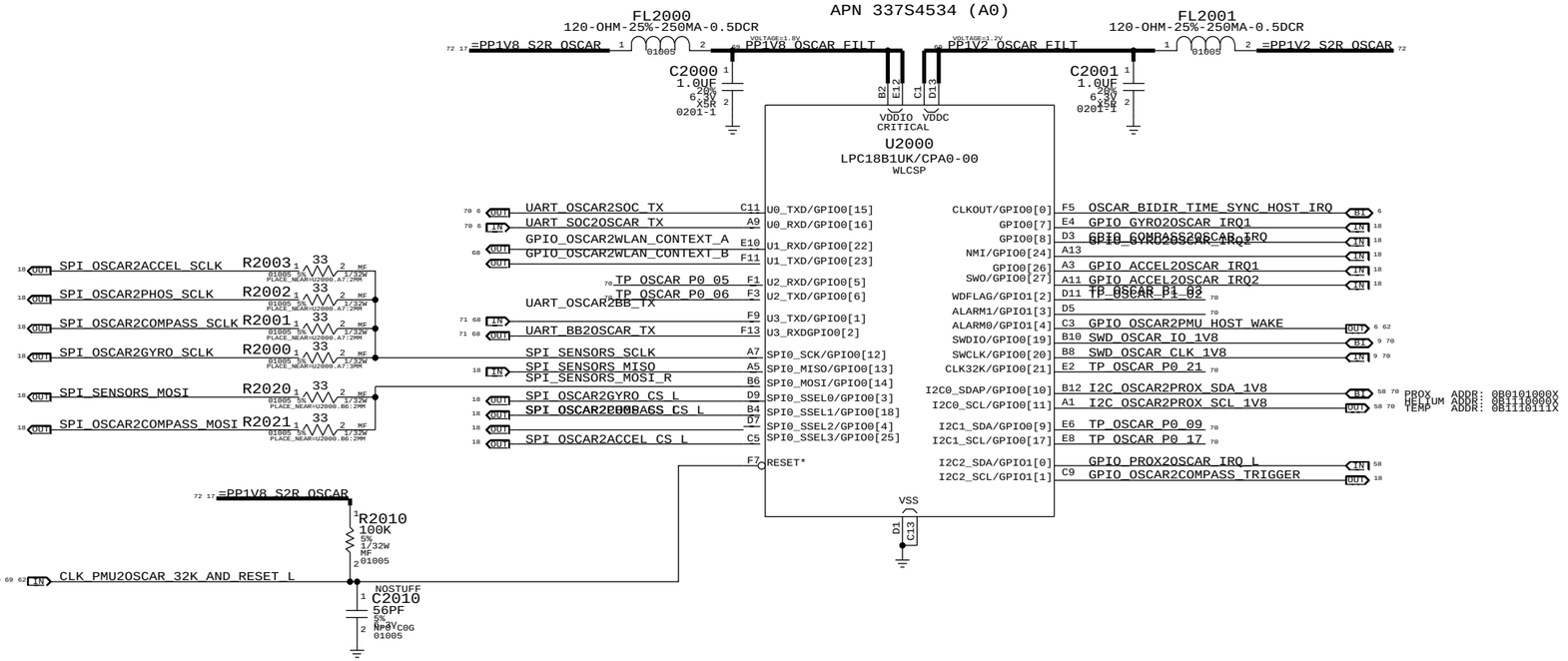
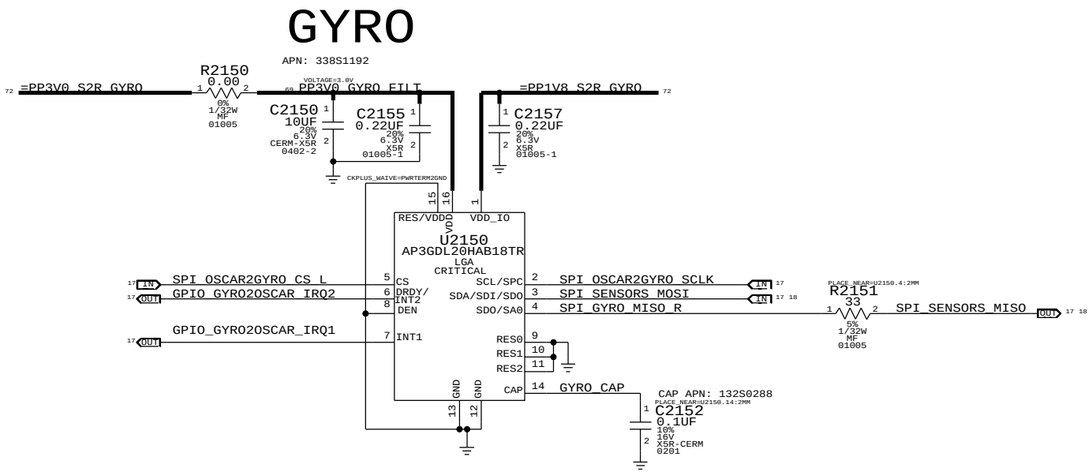
OSCAR2

APN 337S4534 (A0)

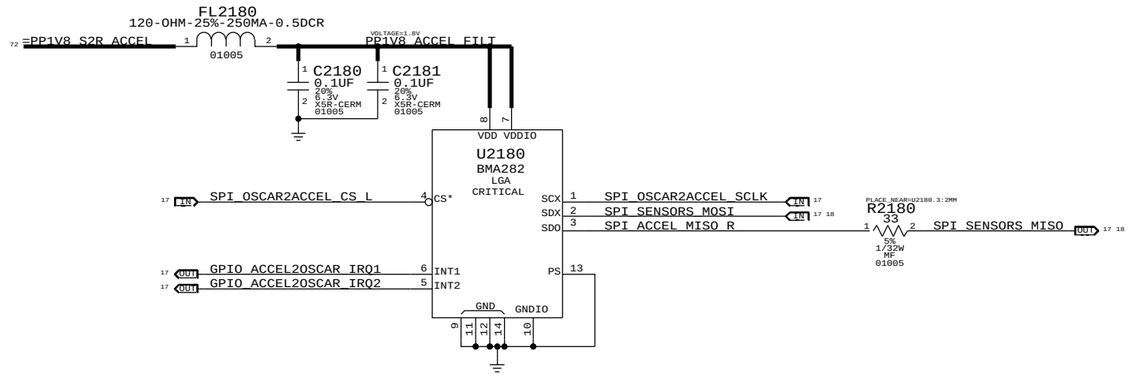


SENSORS

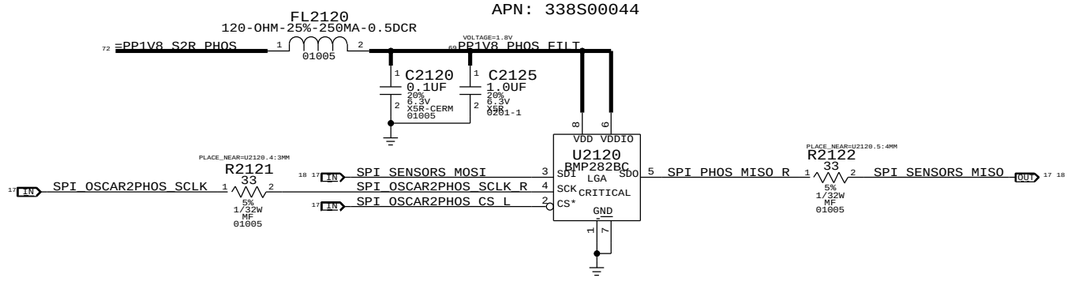
GYRO



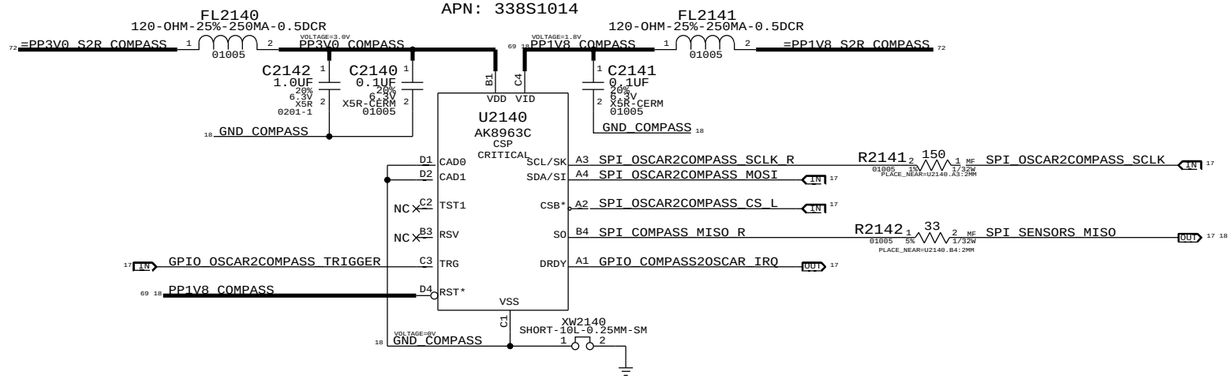
ACCEL



PHOSPHORUS



COMPASS



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PAGE TITLE	SENSOR: CARBON, PHOS+, MAGN
Apple Inc.	DRAWING NUMBER 051-0301 SIZE D
	REVISION B.0.0
	BRANCH
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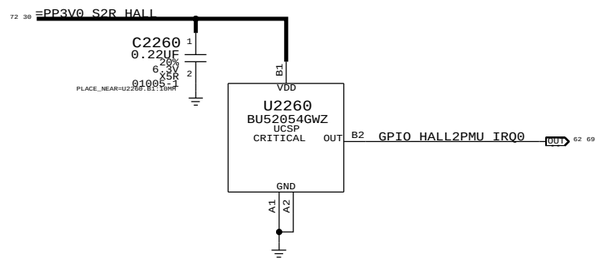
	SHEET 18 OF 73

HALL EFFECT

HALL EFFECT

APN 353S3687



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PAGE TITLE

SENSOR: HALL EFFECT

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D

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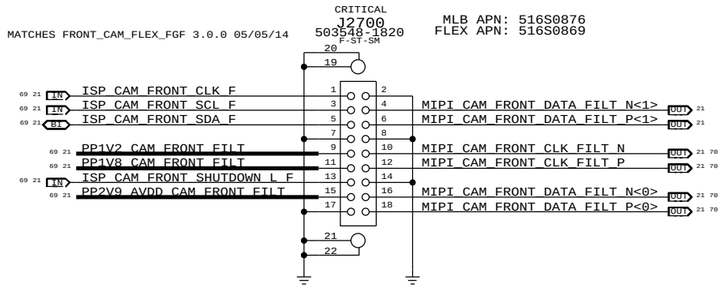
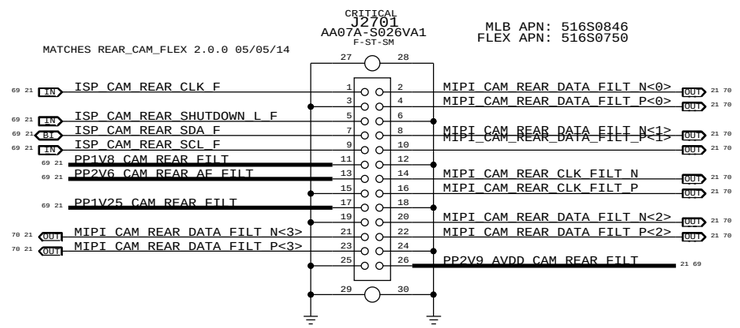
FRONT & REAR CAMERA CONNECTORS

FRONT CAMERA CONNECTOR



REAR CAMERA CONNECTOR



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PAGE TITLE
CAMERA: CAM CONNS

Apple Inc.

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FRONT CAMERA SUPPORT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S00018	7	FERRITE,80OHM,25%,500MA,0.18DCR	FL2800,FL2802,FL2803,FL2861,FL2871,FL2881,FL2891	CRITICAL	
155S0667	8	COMMON MODE CHOKE,90OHM,100MA	L2810,L2811,L2812,L2852,L2853,L2854,L2855,L2856	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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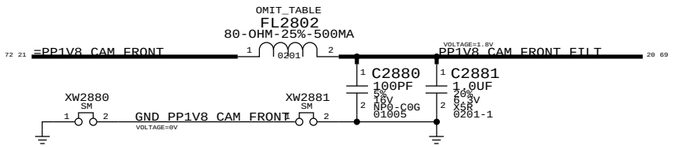
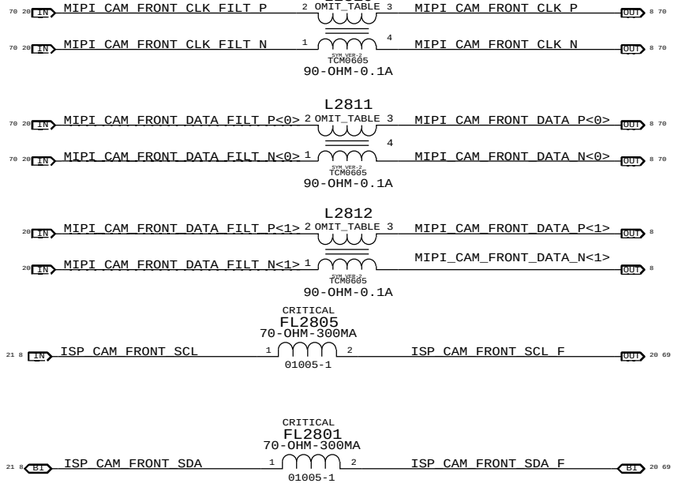
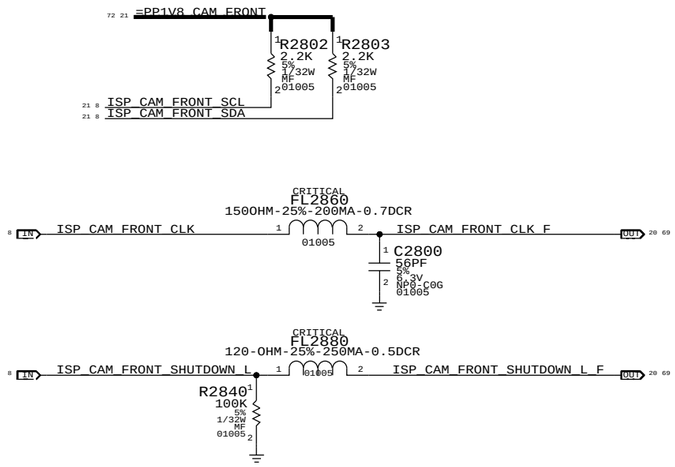
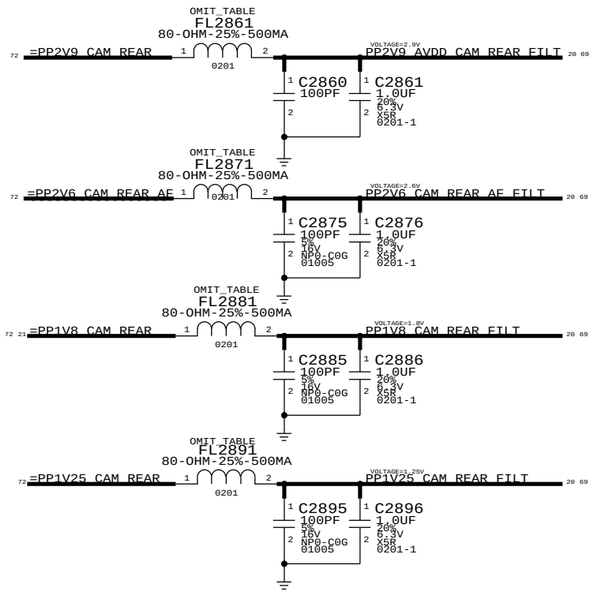
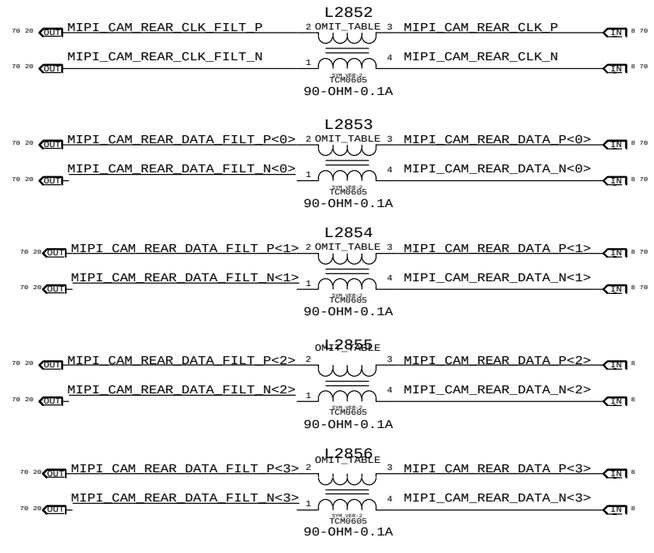


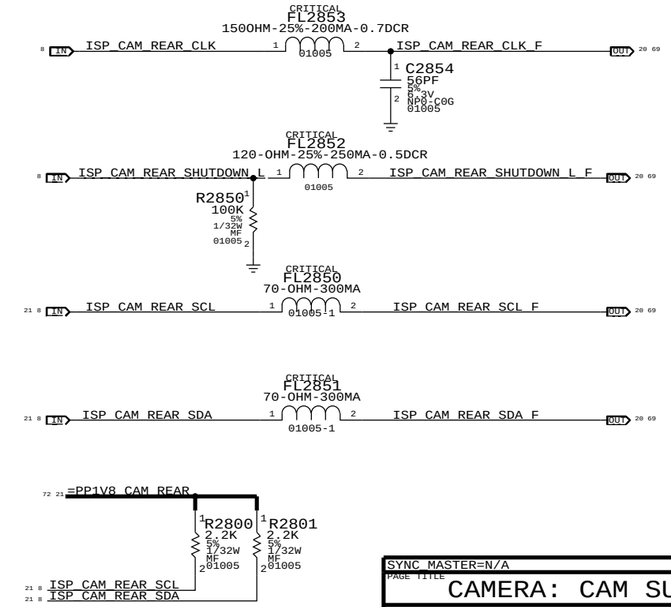




REAR CAMERA SUPPORT







SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
CAMERA: CAM SUPPORT

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D
REVISION
BRANCH B.0.0

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S1213	338S1116		U3000	RDAR://PROBLEM/13394605
155S0661	155S0511			RDAR://PROBLEM/12639854

L3000,L3001,L3002,L3003,L3004,L3005

MIKEY BUS FILTER

=PPVCC_MAIN_AUDIO
=PP1V8_AUDIO
=PP1V7_VA_VCP
GND_AUDIO_CODEC
PP1V7_VCP
PPVCC_VPROG_CP
PPVCC_VPROG_MB_F
L81_FLYP
L81_FLYC
L81_FLYN
L81_PVCP
L81_NVCP
L81_FILT
L81_MBUS_P
L81_MBUS_N
MIKEY_TS_P
MIKEY_TS_N
CONN_HP_LEFT_FILT
CONN_HP_RIGHT_FILT
CONN_HP_HS3_FILT
CONN_HP_HS4_FILT
CONN_HP_HS3_REF_FILT
CONN_HP_HS4_REF_FILT
CONN_HP_HEADSET_DET_FILT
TO HEADPHONE JACK
CODEC_HP_HS4
CODEC_HP_HS3
HP_MIC_POS
HP_MIC_NEG
CODEC_HP_DET_R
CODEC_AIN
CODEC_MIC_BIAS_FILT
I2S_CODEC2SOC_ASP_DOUT
I2S_CODEC2SOC_XSP_DOUT
DMIC_BTN_SD
DMIC_BTN_SCLK
DMIC_MIC_SD
DMIC_MIC_SCLK

NOTE: EXTMIC INPUTS FROM HS3/HS4 MUST USE EXTERNAL SWITCHES FOR RETURN CURRENTS

U3000 CS42L81-CWZR-A1 WLCSP SYM 1 OF 2

U3000 CS42L81-CWZR-A1 WLCSP SYM 2 OF 2

SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE	AUDIO: L81 CODEC
Apple Inc.	DRAWING NUMBER 051-0301 SIZE D
	BRANCH B.0.0
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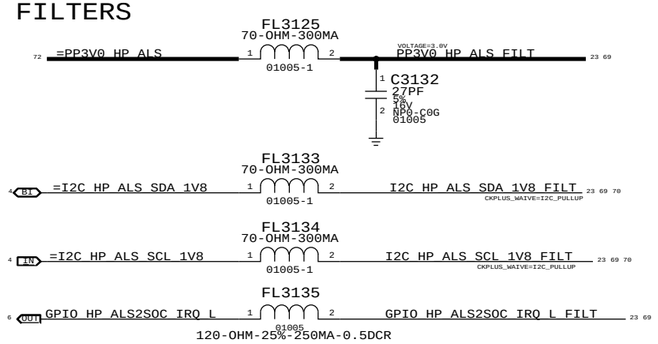
	SHEET 22 OF 73

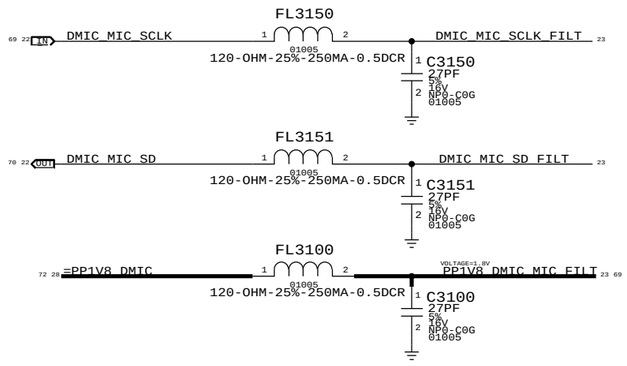
AUDIO JACK AND DMIC CONN

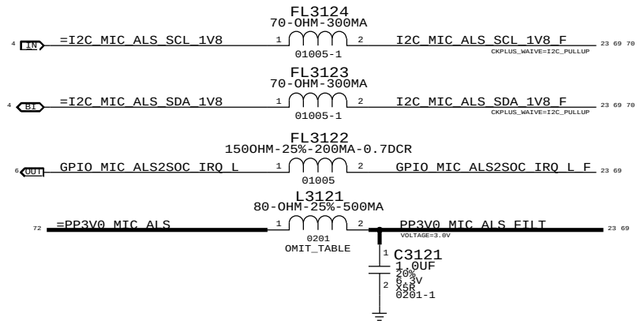
ALS FILTERS



SHUNT FILTERS

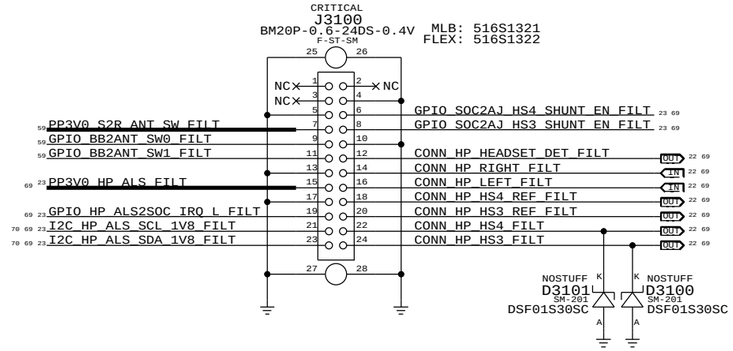
DMIC FILTERS



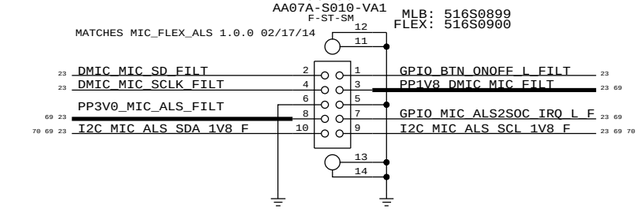


AUDIO JACK B2B CONNECTOR

MATCHES ALS_AUDIO_JACK_FLEX 2.1.0 02/18/14



MIC FLEX CONNECTOR



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S00018	1	FERRITE,80OHM,25%,500MA,0.18DCR	L3121	CRITICAL	

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PAGE TITLE: AUDIO: HP/DMIC FLEX CONNS

Apple Inc.

DRAWING NUMBER: 051-0301 SIZE: D

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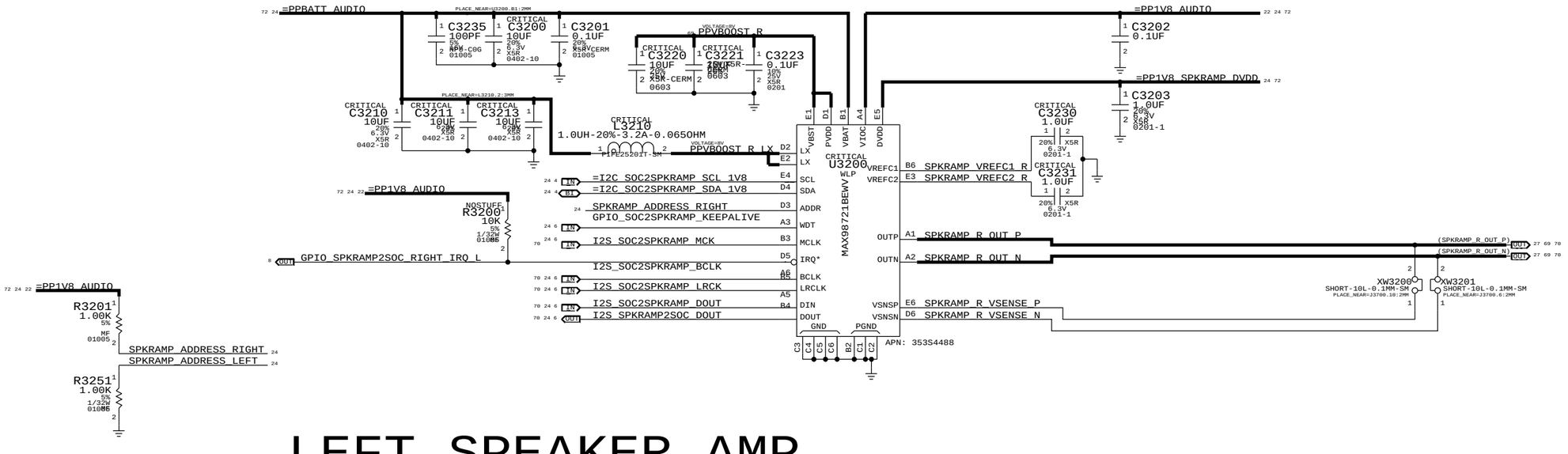
RIGHT SPEAKER AMP



LEFT SPEAKER AMP

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

AUDIO: SPEAKER AMPS

Apple Inc.

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0667	2	COMMON MODE CHOKE,90OHM,100MA	L3530,L3531	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0155	377S0104	?		RDAR://PROBLEM/12840267

DZ3500,DZ3501,DZ3502,DZ3503,DZ3590

=PP3V0_S2R_TRISTAR
=PP3V3_ACC
=PP1V8_S2R_TRISTAR
PP5VBUS_PROT

C3530 1.0UF 20% 6.3V X5R 0201-1
C3535 0.22UF 20% 6.3V X5R 0201
C3540 15PF 5% 16V NP0-C0G-CERM 01005
C3542 15PF 5% 16V NP0-C0G-CERM 01005
C3532 0.22UF 10% 6.3V X5R 0204
C3531 0.22UF 20% 6.3V X5R 0201
C3541 15PF 5% 16V NP0-C0G-CERM 01005
C3543 8.2PF +/-0.5PF 50V C0G-CERM 201
C3534 1UF 10% 25V X5R 402
C3545 1UF 10% 25V X5R 402

U3500
CBTL1610A1UK
WLCSP
CRITICAL

VDD_1V8 F3
VDD_3V0 F4
ACC_PWR D5
P_IN F6
ACC1 C5 PPOUT_E75_ACC_ID1
ACC2 E5 PPOUT_E75_ACC_ID2
DIG_DP C3 MIKEY_TS_P
DIG_DN C4 MIKEY_TS_N
USB1_DP A1 USB_BB_P
USB1_DN B1 USB_BB_N
BRICK_ID C2 PMU_USB_BRICKID
USB0_DP A3 USB_SOC_P
USB0_DN B3 USB_SOC_N
UART0_TX E2 UART_SOC2ACC_TX
UART0_RX E1 UART_ACC2SOC_TX
UART1_TX F2 UART_SOC2DEBUG_TX
UART1_RX F1 UART_DEBUG2SOC_TX
UART2_TX D2 UART_BB2SOC_TX
UART2_RX D1 UART_SOC2BB_TX
JTAG_CLK A5 JTAG_SOC_TCK_R
JTAG_DIO B5 JTAG_SOC_TMS_R
DP1 A2 E75_DPAIR1_P
DN1 B2 E75_DPAIR1_N
DP2 E75_DPAIR2_P
DN2 E75_DPAIR2_N
CON_DET_L E3 TS_E75_ACC_DET_L
POW_GATE_EN* D6 OVP_SW_EN_L
SWITCH_EN E4 RESET_SOC_L
HOST_RESET B6 GPIO_TS2PMU_RESET
SDA D3 =I2C_SOC2TRISTAR_SDA_1V8
SCL D4 =I2C_SOC2TRISTAR_SCL_1V8
C6 GPIO_TS2SOC2PMU_IRQ
BYPASS E6 BYPASS_TS
DVSS F5 C1 A6

ACCESSORY USB
ACCESSORY UART
TRISTAR TX IS AN INPUT AND ITS RX IS AN OUT
SOC DEBUG UART
BB DEBUG UART (T'S OFF TO SOC UART)

R3530 0.00 0% 1/32W MF 01005 PLACE_NEAR=U3500.A5:5MM
JTAG_SOC_TCK
R3531 0.00 0% 1/32W MF 01005 PLACE_NEAR=U3500.B5:5MM
JTAG_SOC_TMS

C3533 1.0UF 20% 6.3V X5R 0201-1

XW3500 SHORT-10L-0.25MM-SM
L81_MBUS_REF

OMIT_TABLE
L3530 90-OHM-0.1A TCM0605 SYM_VER:1
E75_DPAIR1_CONN_P
E75_DPAIR1_CONN_N
CRITICAL DZ3500 ESD0P2RF-02LS TSSLP-2-1 0.4PF
CRITICAL DZ3501 ESD0P2RF-02LS TSSLP-2-1 0.4PF

OMIT_TABLE
L3531 90-OHM-0.1A TCM0605 SYM_VER:1
E75_DPAIR2_CONN_P
E75_DPAIR2_CONN_N
CRITICAL DZ3502 ESD0P2RF-02LS TSSLP-2-1 0.4PF
CRITICAL DZ3503 ESD0P2RF-02LS TSSLP-2-1 0.4PF

R3590 10K 5% 1/32W MF 01005
E75_ACC_DET_R_L
FL3590 120-OHM-25%-250MA-0.5DCR 01005
E75_ACC_DET_CONN_L
CRITICAL D3591L SM-201 DSF01S30SC
NOSTUFF C3590 15PF 5% 16V NP0-C0G-CERM 01005
CRITICAL DZ3590 ESD0P2RF-02LS TSSLP-2-1

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PAGE TITLE: IO: TRISTAR
Apple Inc.
DRAWING NUMBER 051-0301 SIZE D
DEVIATION
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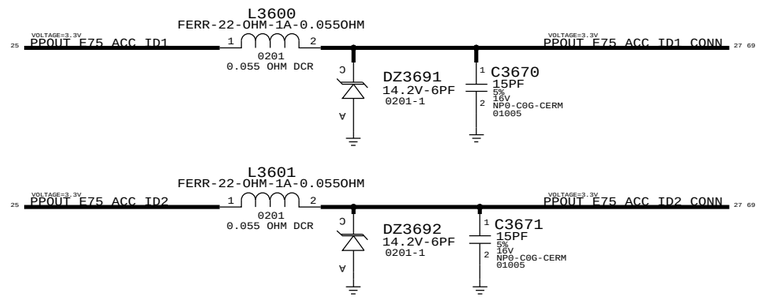

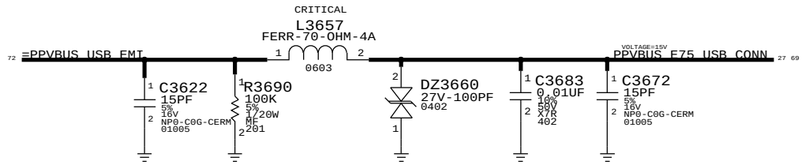

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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155S0320	155S0513		L3600,L3601	RDAR://PROBLEM/9625601
155S0741	155S0397		L3657	RDAR://PROBLEM/11238851

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

IO: FILTERS

Apple Inc.

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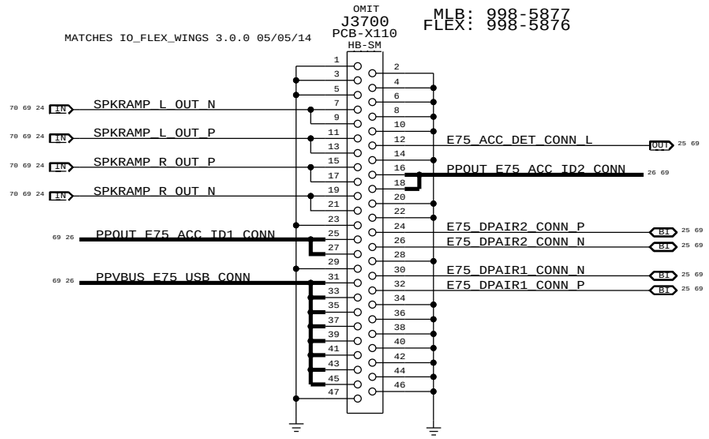
IO FLEX HOTBAR PADS

OMIT
J3700
PCB-X110
HB-SM

MLB: 998-5877
FLEX: 998-5876

MATCHES IO_FLEX_WINGS 3.0.0 05/05/14



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PAGE TITLE
IO: HOTBAR PADS

Apple Inc.

DRAWING NUMBER 051-0301
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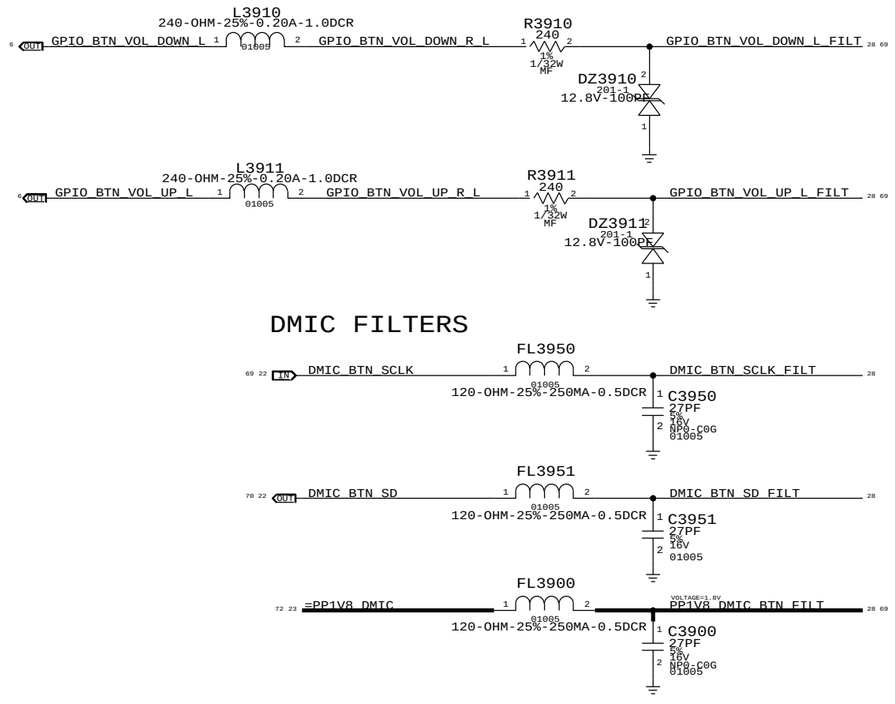
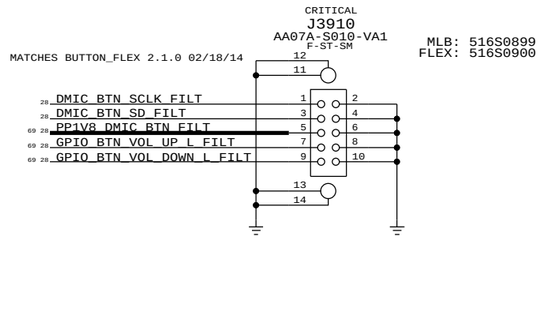
BUTTON CONNECTOR



DMIC FILTERS



MLB: 516S0899
FLEX: 516S0900

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
IO: BUTTON FLEX CONN

Apple Inc.

DRAWING NUMBER 051-0301
SIZE D
REVISION
BRANCH B.0.0

STINGER

CRITICAL
J4020
AA21
F-ST-SM

MATCHES GRAPE_FLEX_ALT3 1.1.0 01/13/14

MLB APN: 516S1070
FLEX APN: 516S1071

		43	44		
		1	2		
70 29	MT_PANEL_OUT<39>	3	4	MT_PANEL_OUT<0>	29 70
70 29	MT_PANEL_OUT<38>	5	6	MT_PANEL_OUT<1>	29 70
70 29	MT_PANEL_OUT<37>	7	8	MT_PANEL_OUT<2>	29 70
70 29	MT_PANEL_OUT<36>	9	10	MT_PANEL_OUT<3>	29 70
70 29	MT_PANEL_OUT<35>	11	12	MT_PANEL_OUT<4>	29 70
70 29	MT_PANEL_OUT<34>	13	14	MT_PANEL_OUT<5>	29 70
70 29	MT_PANEL_OUT<33>	15	16	MT_PANEL_OUT<6>	29 70
70 29	MT_PANEL_OUT<32>	17	18	MT_PANEL_OUT<7>	29 70
70 29	MT_PANEL_OUT<31>	19	20	MT_PANEL_OUT<8>	29 70
70 29	MT_PANEL_OUT<30>	21	22	MT_PANEL_OUT<9>	29 70
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70 29	MT_PANEL_OUT<27>	27	28	MT_PANEL_OUT<12>	29 70
70 29	MT_PANEL_OUT<26>	29	30	MT_PANEL_OUT<13>	29 70
70 29	MT_PANEL_OUT<25>	31	32	MT_PANEL_OUT<14>	29 70
70 29	MT_PANEL_OUT<24>	33	34	MT_PANEL_OUT<15>	29 70
70 29	MT_PANEL_OUT<23>	35	36	MT_PANEL_OUT<16>	29 70
70 29	MT_PANEL_OUT<22>	37	38	MT_PANEL_OUT<17>	29 70
70 29	MT_PANEL_OUT<21>	39	40	MT_PANEL_OUT<18>	29 70
70 29	MT_PANEL_OUT<20>	41	42	MT_PANEL_OUT<19>	29 70
		45	46		

CRITICAL
J4040

MATCHES GRAPE_FLEX_ALT3 1.1.0 01/13/14

MLB APN: 516S1174
FLEX APN: 516S1175

		35	36		
69 30	PP3V0_S2R_GRAPE_HALL_FILT	1	2	GPIO_HALL2PMU_IRQ1_FILT	OUT 30 69
		3	4		
70 30	MT_PANEL_IN<29>	5	6	MT_PANEL_IN<14>	OUT 30 70
70 30	MT_PANEL_IN<28>	7	8	MT_PANEL_IN<13>	OUT 30 70
70 30	MT_PANEL_IN<27>	9	10	MT_PANEL_IN<12>	OUT 30 70
70 30	MT_PANEL_IN<26>	11	12	MT_PANEL_IN<11>	OUT 30 70
70 30	MT_PANEL_IN<25>	13	14	MT_PANEL_IN<10>	OUT 30 70
70 30	MT_PANEL_IN<24>	15	16	MT_PANEL_IN<9>	OUT 30 70
70 30	MT_PANEL_IN<23>	17	18	MT_PANEL_IN<8>	OUT 30 70
70 30	MT_PANEL_IN<22>	19	20	MT_PANEL_IN<7>	OUT 30 70
70 30	MT_PANEL_IN<21>	21	22	MT_PANEL_IN<6>	OUT 30 70
70 30	MT_PANEL_IN<20>	23	24	MT_PANEL_IN<5>	OUT 30 70
70 30	MT_PANEL_IN<19>	25	26	MT_PANEL_IN<4>	OUT 30 70
70 30	MT_PANEL_IN<18>	27	28	MT_PANEL_IN<3>	OUT 30 70
70 30	MT_PANEL_IN<17>	29	30	MT_PANEL_IN<2>	OUT 30 70
70 30	MT_PANEL_IN<16>	31	32	MT_PANEL_IN<1>	OUT 30 70
70 30	MT_PANEL_IN<15>	33	34	MT_PANEL_IN<0>	OUT 30 70
		37	38		

72 30 =PP5V25_GRAPE
72 30 29 =PPVCC_MAIN_GRAPE
PPVDD_STINGER_BOOST 29 69
=PP1V8_GRAPE_EXT_SW 29 30 72

C4016 0.1UF 10% 10V X5R-CERM 0201
C4018 4.7UF 20% 6.3V X5R-CERM1 402
C4019 4.7UF 20% X5R-CERM 0402
C4020 0.1UF 0201
C4021 10UF 20% 25V X5R-CERM 0603
C4022 0.1UF 20% 25V 01005

VBAT N7, VBATDRV N9, VDDH B6 E6 H7 J5 L5, VDDHV B5 F5 H6 H9 K5 M5, VDDIO J10

CRITICAL
U4003
STINGER
CSP

30	CUMULUS_VSTM<0>	A2	TXI0	A3	MT_PANEL_OUT<0>
30	CUMULUS_VSTM<1>	A4	TXI1	A5	MT_PANEL_OUT<1>
30	CUMULUS_VSTM<2>	A7	TXI2	A6	MT_PANEL_OUT<2>
30	CUMULUS_VSTM<3>	A9	TXI3	A8	MT_PANEL_OUT<3>
30	CUMULUS_VSTM<4>	B1	TXI4	B2	MT_PANEL_OUT<4>
30	CUMULUS_VSTM<5>	B3	TXI5	B4	MT_PANEL_OUT<5>
30	CUMULUS_VSTM<6>	B8	TXI6	B7	MT_PANEL_OUT<6>
30	CUMULUS_VSTM<7>	B10	TXI7	B9	MT_PANEL_OUT<7>
30	CUMULUS_VSTM<8>	C1	TXI8	C2	MT_PANEL_OUT<8>
30	CUMULUS_VSTM<9>	C3	TXI9	C4	MT_PANEL_OUT<9>
	CUMULUS_VSTM<10>	C8	TXI10	C7	
30	CUMULUS_VSTM<11>	C10	TXI11	C9	MT_PANEL_OUT<11>
30	CUMULUS_VSTM<12>	D1	TXI12	D2	MT_PANEL_OUT<12>
30	CUMULUS_VSTM<13>	D3	TXI13	D4	MT_PANEL_OUT<13>
30	CUMULUS_VSTM<14>	D5	TXI14	D6	MT_PANEL_OUT<14>
30	CUMULUS_VSTM<15>	D8	TXI15	D7	MT_PANEL_OUT<15>
30	CUMULUS_VSTM<16>	D10	TXI16	D9	MT_PANEL_OUT<16>
30	CUMULUS_VSTM<17>	E1	TXI17	E2	MT_PANEL_OUT<17>
	CUMULUS_VSTM<18>	E3	TXI18	E4	MT_PANEL_OUT<18>
30	CUMULUS_VSTM<19>	E8	TXI19	E7	MT_PANEL_OUT<19>
30	CUMULUS_VSTM<20>	E10	TXI20	E9	MT_PANEL_OUT<20>
30	CUMULUS_VSTM<21>	F1	TXI21	F2	MT_PANEL_OUT<21>
30	CUMULUS_VSTM<22>	F3	TXI22	F4	MT_PANEL_OUT<22>
30	CUMULUS_VSTM<23>	F8	TXI23	F7	MT_PANEL_OUT<23>
30	CUMULUS_VSTM<24>	F10	TXI24	F9	MT_PANEL_OUT<24>
30	CUMULUS_VSTM<25>	G1	TXI25	G2	MT_PANEL_OUT<25>
30	CUMULUS_VSTM<26>	G3	TXI26	G4	MT_PANEL_OUT<26>
30	CUMULUS_VSTM<27>	G5	TXI27	G6	MT_PANEL_OUT<27>
30	CUMULUS_VSTM<28>	G8	TXI28	G7	MT_PANEL_OUT<28>
30	CUMULUS_VSTM<29>	G10	TXI29	G9	MT_PANEL_OUT<29>
30	CUMULUS_VSTM<30>	H1	TXI30	H2	MT_PANEL_OUT<30>
30	CUMULUS_VSTM<31>	H3	TXI31	H4	MT_PANEL_OUT<31>
30	CUMULUS_VSTM<32>	J1	TXI32	J2	MT_PANEL_OUT<32>
30	CUMULUS_VSTM<33>	J3	TXI33	J4	MT_PANEL_OUT<33>
30	CUMULUS_VSTM<34>	K1	TXI34	K2	MT_PANEL_OUT<34>
30	CUMULUS_VSTM<35>	K3	TXI35	K4	MT_PANEL_OUT<35>
30	CUMULUS_VSTM<36>	L1	TXI36	L2	MT_PANEL_OUT<36>
30	CUMULUS_VSTM<37>	L3	TXI37	L4	MT_PANEL_OUT<37>
30	CUMULUS_VSTM<38>	M1	TXI38	M2	MT_PANEL_OUT<38>
30	CUMULUS_VSTM<39>	M3	TXI39	M4	MT_PANEL_OUT<39>

R4010 78.7K 1% 1/32W MF 01005
C4012 33000PF 10% 6.3V X5R 201

STINGER_FREQ J6 FREQ
STINGER_SS L7 SS
DIDT=TRUE SWITCH_NODE=TRUE STINGER_LX M8 M9 M10 SW
STINGER_COMP M6 COMP
29 STINGER_FB K10 FBK_IN
70 30 I2C_GRAPE_SCL_1V8 N2 SCL
70 30 I2C_GRAPE_SDA_1V8 N3 SDA

R4011 3.09K 1% 1/20W MF 201
STINGER_COMP_R
C4013 33000PF 10% 6.3V X5R 201

AVSS C6 F6 H5 N6
PGND L8 L9 L10
FBK_GND K9
SGND N8
PBKG A1 A10 C5 E5 H8 M7 N1 N10

GAIN0 L6 =PP1V8_GRAPE_EXT_SW 29 30 72
GAIN1 K6
GAIN2 J7
PCTL0 K8
PCTL1 K7
PD* J9 GPIO_GRAPE2STINGER_SHDWN_L IN 30
SYNC J8 GPIO_GRAPE2STINGER_SYNC IN 30
EN N5 GPIO_GRAPE2STINGER_EN IN 30
STEP_CLOCK H10 IN 30
RDY/TMUX N4 CLK_GRAPE2STINGER_STEP IN 30

29 STINGER_FB
R4013 10K 1% 1/32W MF 01005
VOLTAGE=0V GND_STINGER_FB
R4012 154K 1% 1/32W MF 01005

BOOST INPUT
72 30 29 =PPVCC_MAIN_GRAPE
CRITICAL
L4001 10UH-20%-0.89A-228MOHM VLS4012E-SM
D4001 NSR10F40NXT5G DSN2
VOLTAGE=21.2V PPVDD_STINGER_BOOST 29 69
C4015 10UF 20% 6.3V 0402-10
C4014 10UF 20% 0603
C4017 10UF 20% X5R-CERM 0603

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE
GRAPE: STINGER & CONN

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D
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BRANCH B.0.0
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SHEET 29 OF 73

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00018	2	IC,CUMULUS,C1,OPTION1	U4100,U4150	CRITICAL	

=PP1V8_GRAPE_EXT_SW
R4102 4.7K 1% 1/32W MF 01005
R4152 4.7K 1% 1/32W MF 01005
CUMULUS_M_BCFG_RTCK
JTAG_CUMULUS_M_TMS
JTAG_CUMULUS_S_TMS
CUMULUS_S_BCFG_RTCK
R4104 4.7K 1% 1/32W MF 01005
R4154 4.7K 1% 1/32W MF 01005

=PP1V8_GRAPE_EXT_SW
R4180 4.7K 1% 1/32W MF 01005
R4181 4.7K 1% 1/32W MF 01005
I2C_GRAPE_SCL_1V8
I2C_GRAPE_SDA_1V8

MASTER CUMULUS

=PP5V25_GRAPE
C4100 1UF 20% 10V X5R 0201
C4101 100PF 5% 6.3V NP0-C0G 01005
=PP1V8_GRAPE_EXT_SW
C4106 0.1UF 20% 4V X5R 01005
PPVDDCORE_CUMULUS_M VOLTAGE=1.8V
PPVDDANA_CUMULUS_M VOLTAGE=1.8V
C4105 56PF 5% 6.3V 01005
C4102 2.2UF 20% 4V X5R-CERM 0201
C4103 2.2UF 20% 4V X5R-CERM 0201
C4104 56PF 5% 6.3V 01005
=PP1V8_GRAPE_EXT_SW
C4108 4.7UF 20% 6.3V X5R 0402
C4109 0.1UF 20% 4V X5R 01005
C4110 100PF 5% 6.3V NP0-C0G 01005

U4100 CUMULUS-C1 WLBGA OMIT_TABLE

MT_PANEL_IN<0>	B9	IN0_0	
MT_PANEL_IN<1>	B8	IN1_0	
MT_PANEL_IN<2>	A9	IN2_0	
MT_PANEL_IN<3>	B7	IN3_0	
MT_PANEL_IN<4>	B6	IN4_0	
MT_PANEL_IN<5>	A8	IN5_0	
MT_PANEL_IN<6>	B5	IN6_0	
MT_PANEL_IN<7>	B4	IN7_0	
MT_PANEL_IN<8>	A7	IN8_0	
MT_PANEL_IN<9>	B3	IN9_0	
MT_PANEL_IN<10>	A6	IN10_0	
MT_PANEL_IN<11>	A3	IN11_0	
MT_PANEL_IN<12>	A5	IN12_0	
MT_PANEL_IN<13>	A4	IN13_0	
MT_PANEL_IN<14>	B2	IN14_0	
NC_CUMULUS_M_IN14_1 (NO_TEST=TRUE)	A2	IN14_1	
SPI_GRAPE_CS_L	E4	H_CS*	
GPIO_GRAPE2SOC_IRQ_L	F1	H_INT*	
SPI_GRAPE_SCLK	D3	H_SCLK	
SPI_GRAPE_MOSI	D2	H_SDI	
SPI_GRAPE_MISO	E1	H_SDO	
TP_JTAG_CUMULUS_M_TCK	C4	JTAG_TCK	
TP_JTAG_CUMULUS_M_TDI	C3	JTAG_TDI	
I2C_GRAPE_SDA_1V8	E2	JTAG_TDO	
JTAG_CUMULUS_M_TMS	C6	JTAG_TMS	
CUMULUS_M_BCFG_RTCK	E3	BCFG_RTCK	
CLK_SOC2GRAPE_32K	D1	CLKIN/RESET*	
	D9	RSTOVR*	

	E9	VSTM_0	CUMULUS_VSTM<0>
	E5	VSTM_1	CUMULUS_VSTM<1>
	F7	VSTM_2	CUMULUS_VSTM<2>
	E6	VSTM_3	CUMULUS_VSTM<3>
	E7	VSTM_4	CUMULUS_VSTM<4>
	F8	VSTM_5	CUMULUS_VSTM<5>
	G9	VSTM_6	CUMULUS_VSTM<6>
	D6	VSTM_7	CUMULUS_VSTM<7>
	D7	VSTM_8	CUMULUS_VSTM<8>
	D8	VSTM_9	CUMULUS_VSTM<9>
	F9	VSTM_10	CUMULUS_VSTM<10>
	D5	VSTM_11	CUMULUS_VSTM<11>
	F6	VSTM_12	CUMULUS_VSTM<12>
	F5	VSTM_13	CUMULUS_VSTM<13>
	G4	VSTM_14	CUMULUS_VSTM<14>
	E8	VSTM_15	CUMULUS_VSTM<15>
	G8	VSTM_16	CUMULUS_VSTM<16>
	G7	VSTM_17	CUMULUS_VSTM<17>
	G6	VSTM_18	CUMULUS_VSTM<18>
	G5	VSTM_19	CUMULUS_VSTM<19>
	G1	GPIO_1/CK	CUMULUS_M2S_CLK
	D4	GPIO_2/SD	CUMULUS_M2S_SDA
	F2	GPIO_3	DISPLAY_SYNC
	F3	GPIO_4	CUMULUS_M_GPIO_4
	C2	TM_ACS*	NC_CUMULUS_M_TM_ACS_L (NO_TEST=TRUE)
	G3	TM_OVR	I2C_GRAPE_SCL_1V8

GPIO_SOC2GRAPE_RESET_L
R4101 4.7K 1% 1/32W MF 01005
R4106 100K 5% 1/32W MF 01005
R4110 4.7K 1% 1/32W MF 01005
GND
C7 C9 C2

SLAVE CUMULUS

=PP5V25_GRAPE
C4150 1UF 20% 10V X5R 0201
=PP1V8_GRAPE_EXT_SW
C4156 0.1UF 20% 4V X5R 01005
PPVDDCORE_CUMULUS_S VOLTAGE=1.8V
PPVDDANA_CUMULUS_S VOLTAGE=1.8V
C4155 56PF 5% 6.3V NP0-C0G 01005
C4152 2.2UF 20% 4V X5R-CERM 0201
C4153 2.2UF 20% 4V X5R-CERM 0201
C4154 56PF 5% 6.3V NP0-C0G 01005
=PP1V8_GRAPE_EXT_SW
C4159 0.1UF 20% 4V X5R 01005
C4158 100PF 5% 6.3V NP0-C0G 01005

U4150 CUMULUS-C1 WLBGA OMIT_TABLE

MT_PANEL_IN<15>	B9	IN0_0	
MT_PANEL_IN<16>	B8	IN1_0	
MT_PANEL_IN<17>	A9	IN2_0	
MT_PANEL_IN<18>	B7	IN3_0	
MT_PANEL_IN<19>	B6	IN4_0	
MT_PANEL_IN<20>	A8	IN5_0	
MT_PANEL_IN<21>	B5	IN6_0	
MT_PANEL_IN<22>	B4	IN7_0	
MT_PANEL_IN<23>	A7	IN8_0	
MT_PANEL_IN<24>	B3	IN9_0	
MT_PANEL_IN<25>	A6	IN10_0	
MT_PANEL_IN<26>	A3	IN11_0	
MT_PANEL_IN<27>	A5	IN12_0	
MT_PANEL_IN<28>	A4	IN13_0	
MT_PANEL_IN<29>	B2	IN14_0	
NC_CUMULUS_S_IN14_1 (NO_TEST=TRUE)	A2	IN14_1	
TP_CUMULUS_S_CS_L	E4	H_CS*	
CLK_GRAPE2STINGER_STEP	F1	H_INT*	
GPIO_GRAPE2STINGER_SYNC	D3	H_SCLK	
GPIO_GRAPE2STINGER_RDY	D2	H_SDI	
GPIO_GRAPE2STINGER_EN	E1	H_SDO	
NC_CUMULUS_S_TCK (NO_TEST=TRUE)	C4	JTAG_TCK	
NC_CUMULUS_S_TDI (NO_TEST=TRUE)	C3	JTAG_TDI	
NC_CUMULUS_S_TDO (NO_TEST=TRUE)	E2	JTAG_TDO	
JTAG_CUMULUS_S_TMS	C6	JTAG_TMS	
CUMULUS_S_BCFG_RTCK	E3	BCFG_RTCK	
CLK_SOC2GRAPE_32K	D1	CLKIN/RESET*	
GPIO_SOC2GRAPE_RESET_L	D9	RSTOVR*	

	E9	VSTM_0	CUMULUS_VSTM<20>
	E5	VSTM_1	CUMULUS_VSTM<21>
	F7	VSTM_2	CUMULUS_VSTM<22>
	E6	VSTM_3	CUMULUS_VSTM<23>
	E7	VSTM_4	CUMULUS_VSTM<24>
	F8	VSTM_5	CUMULUS_VSTM<25>
	G9	VSTM_6	CUMULUS_VSTM<26>
	D6	VSTM_7	CUMULUS_VSTM<27>
	D7	VSTM_8	CUMULUS_VSTM<28>
	D8	VSTM_9	CUMULUS_VSTM<29>
	F9	VSTM_10	CUMULUS_VSTM<30>
	D5	VSTM_11	CUMULUS_VSTM<31>
	F6	VSTM_12	CUMULUS_VSTM<32>
	F5	VSTM_13	CUMULUS_VSTM<33>
	G4	VSTM_14	CUMULUS_VSTM<34>
	E8	VSTM_15	CUMULUS_VSTM<35>
	G8	VSTM_16	CUMULUS_VSTM<36>
	G7	VSTM_17	CUMULUS_VSTM<37>
	G6	VSTM_18	CUMULUS_VSTM<38>
	G5	VSTM_19	CUMULUS_VSTM<39>
	G1	GPIO_1/CK	CUMULUS_M2S_CLK
	D4	GPIO_2/SD	CUMULUS_M2S_SDA
	F2	GPIO_3	TP_CUMULUS_S_GPIO_3
	F3	GPIO_4	GPIO_GRAPE2STINGER_SHDWN_L
	C2	TM_ACS*	NC_CUMULUS_S_TM_ACS_L (NO_TEST=TRUE)
	G3	TM_OVR	

R4159 4.7K 1% MF 01005
GND
C27 C69 C22

HALL EFFECT

FL4124 240-OHM-25%-0.20A-1.0DCR
GPIO_HALL2PMU_IRQ1
GPIO_HALL2PMU_IRQ1_FILT
FL4125 70-OHM-25%-3.0A
=PP3V0_S2R_HALL
PP3V0_S2R_GRAPE_HALL_FILT
C4125 27PF 5% 16V NP0-C0G 01005

=PP1V8_S2R_GRAPE_EXTERNAL_SW
=PPVCC_MAIN_GRAPE
C4190 0.1UF
C4196 1.0UF 20% 6.3V X6S 0201-1
U4190 SLG5AP1443V TDFN (CRITICAL)
VCC_MAIN_GRAPE_RAMP
GPIO_SOC2GRAPE_EXT_SW_ON
PP1V8_GRAPE_EXT_SW
C4193 4700PF 10% 10V X7R 0201 (CRITICAL)
R4194 100K 5% 1/32W MF 01005
C4195 10UF 20% 6.3V X6S 0402-10 (CRITICAL)

LAYOUT NOTE:
PUT THERMAL VIAS AROUND U4100 IN CASE OF SHORTED CONDITION

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE: GRAPE: CUMULUS
Apple Inc.
DRAWING NUMBER 051-0301 SIZE D
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DISPLAY CONNECTOR

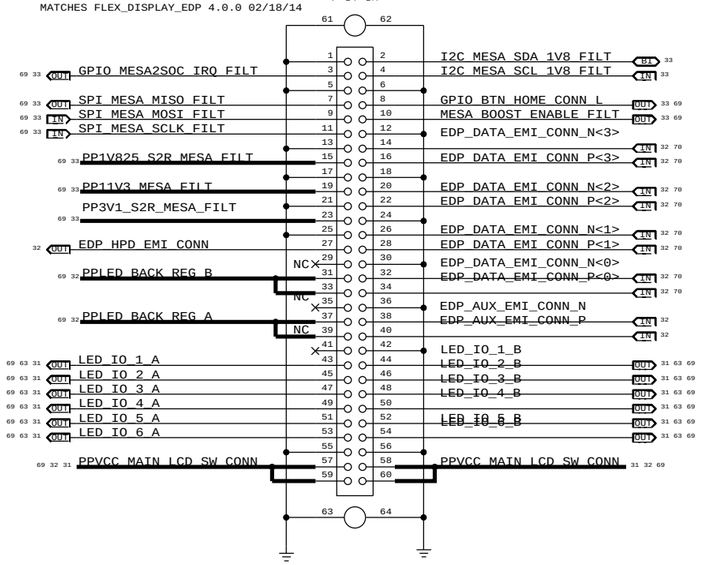
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
131S00011	131S0641	?	C4550, ECT	RDAR://PROBLEM/15682101

DISPLAY CONNECTOR

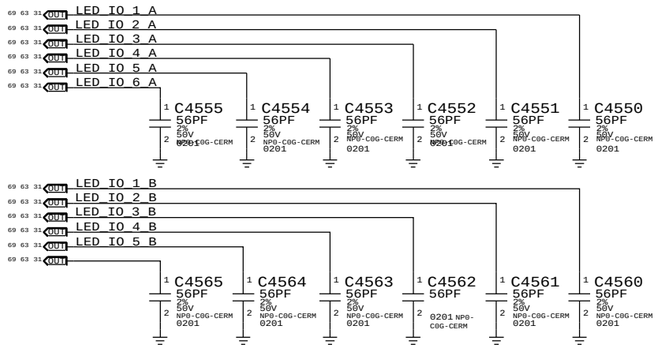
CRITICAL

J4500
BM15P1.0-60DS-0.35V MLB APN: 516S1243
F-ST-SM FLEX APN: 516S1244

MATCHES FLEX_DISPLAY_EDP 4.0.0 02/18/14



SWAPPED LED STRING A AND B INTENTIONALLY TO EASE ROUTING



SYNC_MASTER=N/A SYNC_DATE=N/A

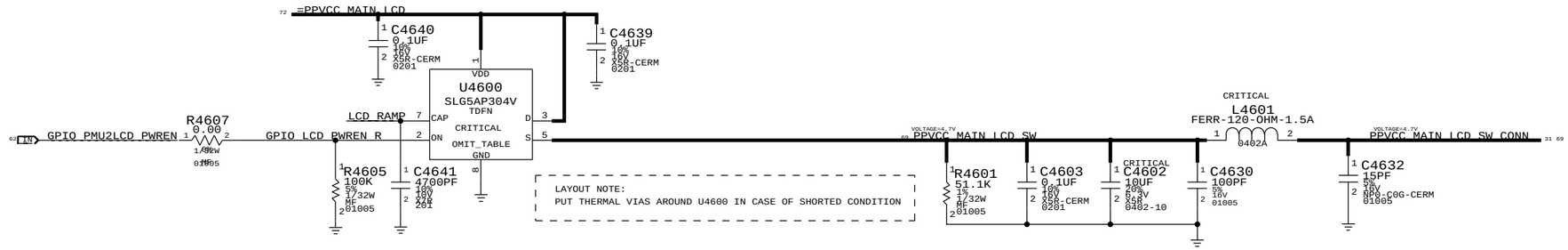
PAGE TITLE
DISPLAY: CONNECTOR

Apple Inc.

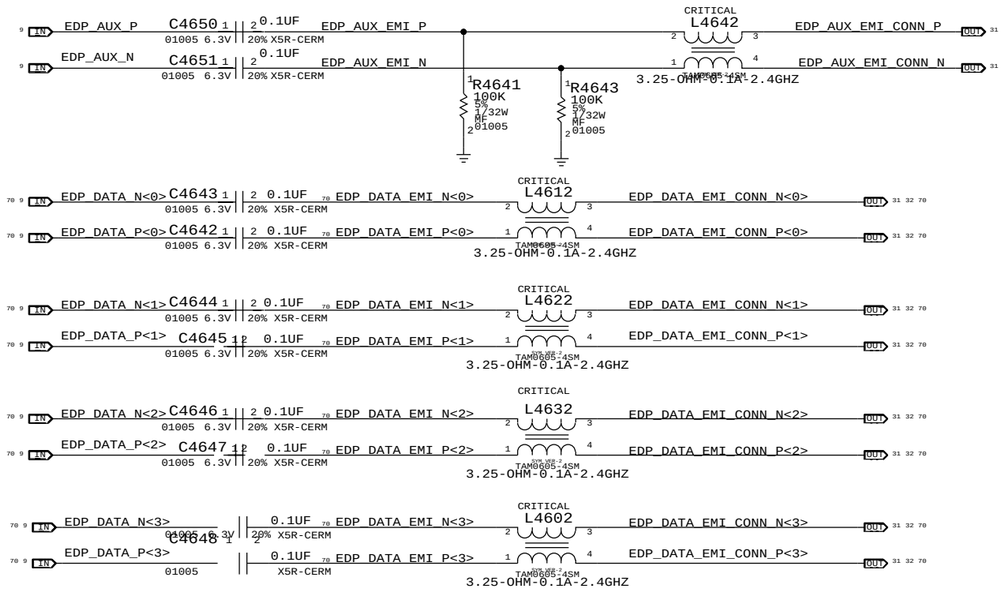
DRAWING NUMBER 051-0301 SIZE D
BRANCH B.0.0

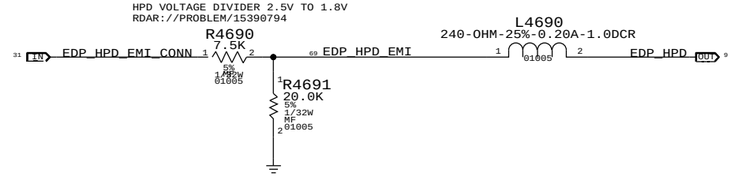
EDP CONNECTOR SUPPORT

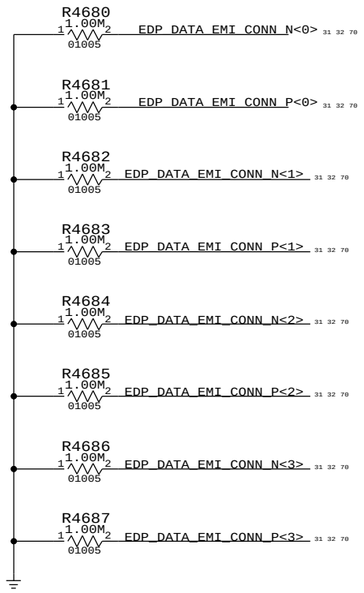
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0914	155S0897	?	L4602, ECT	RDAR://PROBLEM/15954071

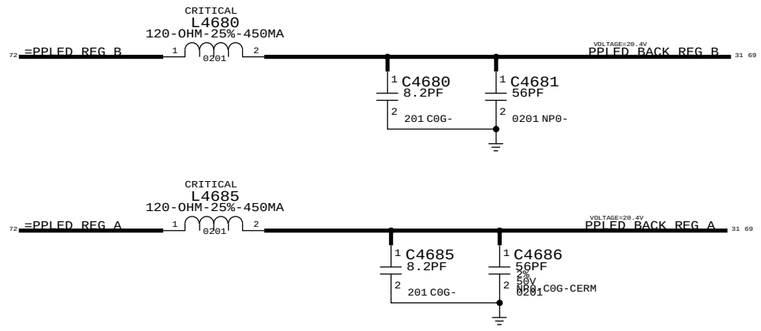


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4272	1	IC,SLG5AP1423V	U4600	CRITICAL	?









SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
DISPLAY: EDP SUPPORT

Apple Inc.

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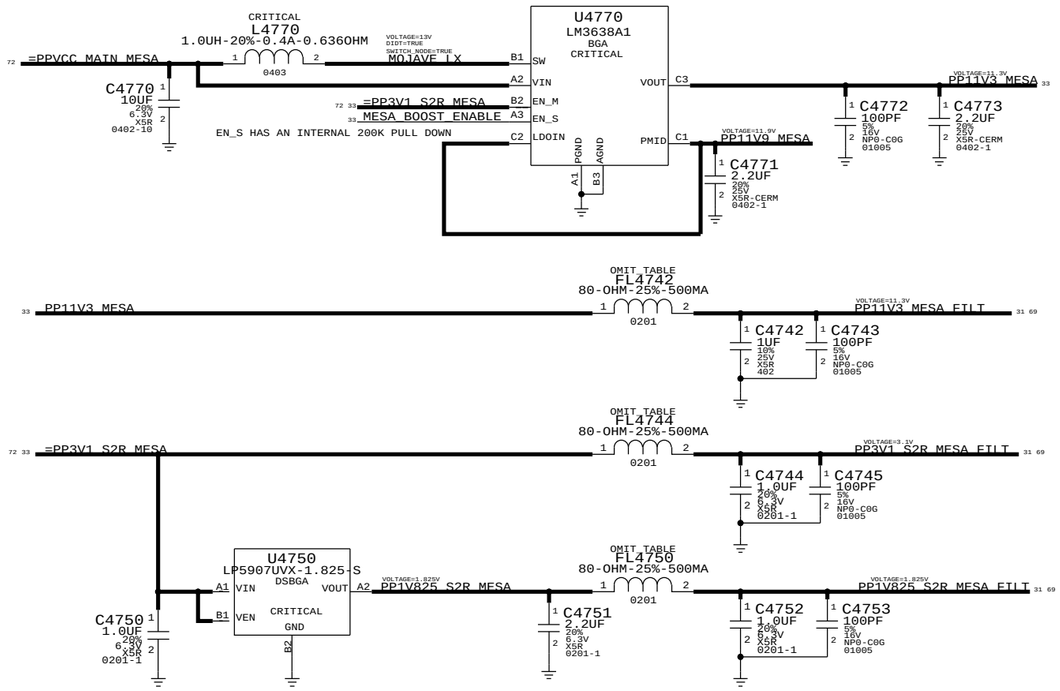
MESA & HOME BUTTON

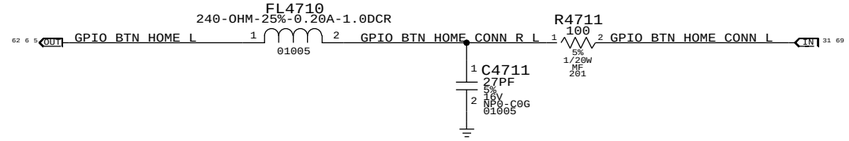
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S00018	3	FERRITE,800HM,25%,500MA,0.18DCR	FL4742,FL4744,FL4750	CRITICAL	

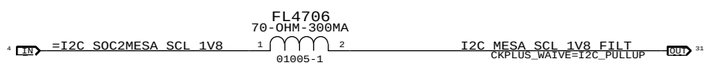
MOJAVE

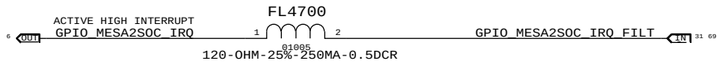
USING A1 BECAUSE NAVAJO NEEDS 11V3

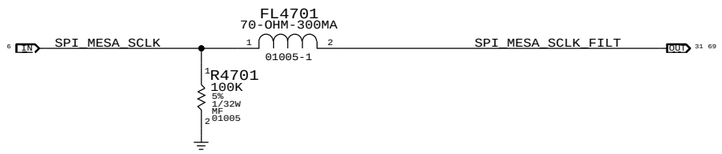


HOME BUTTON FILTERS









PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00017	155S0755			RDAR://PROBLEM/15807137

FL3910,FL3911,FL4124,L4690,FL4710

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00018	155S0664			RDAR://PROBLEM/15796569

FL2800,FL2802,FL2803,FL2861,FL2871,FL2881,FL2891,FL4742,FL4744,FL4750,FL7900

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
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J82 - ROTTERDAM

PP4800 P4MM 1 UART_SOC2ROTTERDAM_TX 6 34
PP4801 P4MM 1 UART_ROTTERDAM2SOC_TX 6 34
PP4802 P4MM 1 UART_SOC2ROTTERDAM_RTS_L 6 34
PP4803 P4MM 1 UART_ROTTERDAM2SOC_RTS_L 6 34
PP4804 P4MM 1 GPIO_SOC2ROTTERDAM_EN 8 34
PP4806 P4MM 1 GPIO_SOC2ROTTERDAM_DWLD_REQ 8 34

72 34 =PP1V8_S2R_ROTTERDAM
NOSTUFF
R4800 100K 5% 1/32W MF 01005
34 8 GPIO_SOC2ROTTERDAM_EN
34 8 GPIO_SOC2ROTTERDAM_DWLD_REQ
NOSTUFF
R4801 100K 5% 1/32W MF 01005

72 =PPVCC_MAIN_ROTTERDAM
C4800 4.7UF 20% 16V X5R-CERM 0402
72 34 =PP1V8_S2R_ROTTERDAM
C4801 1UF 20% 10V X5R 0201
PPVDD_ROTTERDAM
PPSVDD_ROTTERDAM
C4820 0.1UF 20% 6.3V X5R-CERM 01005
C4810 1UF 20% 10V X5R 0201
C4811 0.1UF 20% 6.3V X5R-CERM 01005

U4800
PN65V
UFLGA
OMIT_TABLE

NC	D1	IRQ	
NC	B3	SVDD_REQ	
34 8 IN	A1	DWL	GPIO_SOC2ROTTERDAM_DWLD_REQ
NC	A2	CLK_REQ	
NC	A3	CLK_XTAL1	
34 6 IN	C1	RX	UART_SOC2ROTTERDAM_TX
34 6 OUT	D2	TX	UART_ROTTERDAM2SOC_TX
34 6 IN	B1	CTS	UART_SOC2ROTTERDAM_RTS_L
34 6 OUT	B2	RTS	UART_ROTTERDAM2SOC_RTS_L
34 8 IN	E1	VEN	GPIO_SOC2ROTTERDAM_EN
34	E3	SMX_RST*	PPSVDD_ROTTERDAM
NC	E4	SMX_CLK	
NC	F4	ESE_IO1	
NC	E6	ESE_IO2	
NC	A7	ESE_IO3	
NC	A6	ESE_IO4	
NC	F3	XTAL2	
SIM_SWIO	A4		NC
SIM_VCC	A5		NC
SIM_PMU_VCC	B5		NC
TX_PWR_REQ	F2		NC
ESE_DWPM_DBG	D5		NC
ESE_DWPS_DBG	E5		NC
ANT1	G7		NC
RXP/RF_CLK_RX	F6		NC
TX1	G3		NC
TX2	G5		NC
RXN/RF_CLK_RX	F5		NC
ANT2	G6		NC
VMID	F7		NC
RF_CLK_TX	F1		NC
RF_DATA_IO	B4		NC

VDD/RF_IF_VDD C6, VBAT C7, VDHF D7, PVDD D6, VUP_G2, TVDD_E7, SVDD_IN G1, SVDD_B7, ESE_VDD C5
VSS E2, GND B6, GND C4, GND D4, GND D6, GND F3, TVSS G4, PVSS C2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00043	1	IC,ROTTERDAM,MP,UFLGA49	U4800	CRITICAL	

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Apple Inc.
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AP INTERFACE & DEBUG CONNECTOR

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TEST POINTS

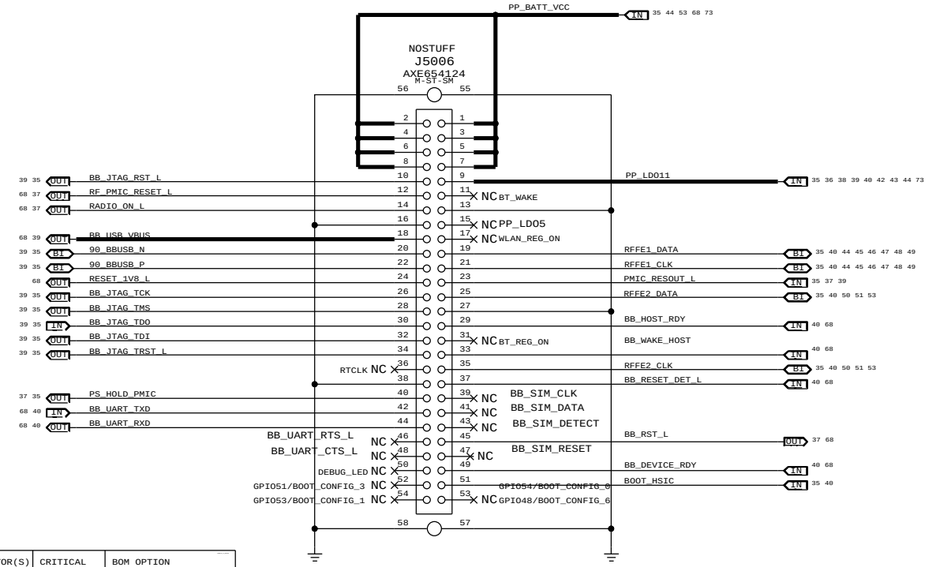
TP5000 A 1 TP-PS 50_BB_HSIC_STROBE 39 68
TP5001 A 1 TP-PS 50_BB_HSIC_DATA 39 68
TP5002 A 1 TP-PS BB_DEBUG_ERROR 40
TP5003 A 1 TP-PS PS_HOLD_PMIC 35 37
TP5004 A 1 TP-PS PMIC_RESOUT_L 35 37 39
TP5005 A 1 TP-PS MDM_CLK 37 39
TP5006 A 1 TP-PS PP_LDO11 35 36 38 39 40 42 43 44 73
TP5007 A 1 TP-PS SPMI_DATA 37 39
TP5008 A 1 TP-PS SPMI_CLK 37 39
TP5025 A 1 TP-PS BOUNDARY_SCAN_EN 39 69
TP5021 A 1 TP-PS PP_BATT_VCC 35 44 53 68 73
TP5028 A 1 TP-PS
TP5026 A 1 TP-PS
TP5027 A 1 TP-PS

TP5009 A 1 TP-PS BB_JTAG_RST_L 35 39
TP5010 A 1 TP-PS BB_JTAG_TCK 35 39
TP5011 A 1 TP-PS BB_JTAG_TMS 35 39
TP5012 A 1 TP-PS BB_JTAG_TDO 35 39
TP5013 A 1 TP-PS BB_JTAG_TDI 35 39
TP5014 A 1 TP-PS BB_JTAG_TRST_L 35 39
TP5015 A 1 TP-PS BB_DEBUG_STATUS 40
TP5016 A 1 TP-PS BOOT_HSIC 35 40
TP5017 A 1 TP-PS RFFE1_CLK 35 40 44 45 46 47 48 49
TP5018 A 1 TP-PS RFFE1_DATA 35 40 44 45 46 47 48 49
TP5019 A 1 TP-PS RFFE2_CLK 35 40 50 51 53
TP5020 A 1 TP-PS RFFE2_DATA 35 40 50 51 53
TP5031 A 1 TP-PS 90_BBUSB_N 35 39
TP5030 A 1 TP-PS 90_BBUSB_P 35 39

PROBE POINTS

PP5000 P4MM SM 1 PP SLEEP_CLK_32K 37 39
PP5001 P4MM SM 1 PP BB_EEPROM_SCL 39 40
PP5002 P4MM SM 1 PP BB_EEPROM_SDA 39 40
PP5003 P4MM SM 1 PP ET_DAC_P 40 44
PP5004 SM 1 PP ET_DAC_N 40 44
TP5029 A 1 TP-PS PP_LDO6 36 69 71 73

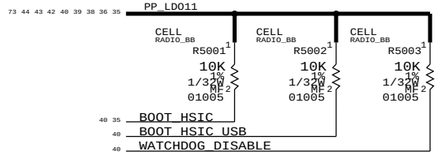
DEBUG CONNECTOR

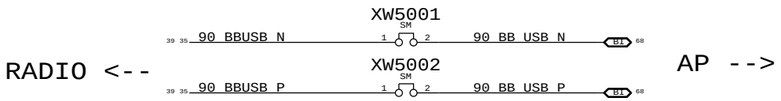


CONFIG _RF BOM OPTIONS

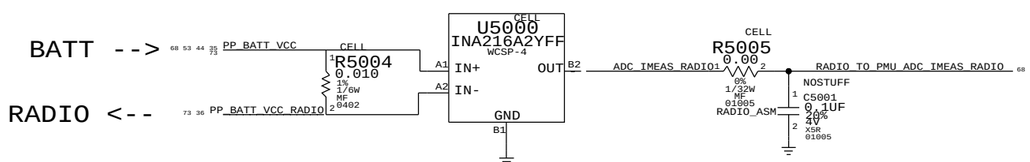
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S0273	1	0.8PF 0201	C6001	CRITICAL	X137_RF
131S0273	1	0.8PF 0201	C6001	CRITICAL	X202_RF
131S0431	1	0.2PF 0201	C6013	CRITICAL	X190_RF
131S0273	1	0.8PF 0201	C6013	CRITICAL	X137_RF
131S0273	1	0.8PF 0201	C6013	CRITICAL	X202_RF
152S2020	1	3.6NH +/-0.1NH 400MA 0201	L6001	CRITICAL	X190_RF
152S2022	1	4.3NH 3% 500MA 0201	L6001	CRITICAL	X137_RF
152S2022	1	4.3NH 3% 500MA 0201	L6001	CRITICAL	X202_RF
131S0323	1	1.1PF 0201	C6421	CRITICAL	X190_RF
152S1217	1	1.0NH +/-0.1NH 750MA 0201	L6402	CRITICAL	X190_RF
152S2042	1	1.8NH +/-0.1NH 800MA 0201	L6402	CRITICAL	X137_RF
152S2042	1	1.8NH +/-0.1NH 800MA 0201	L6402	CRITICAL	X202_RF
152S1994	1	6.8NH 3% 210MA 01005	C6202	CRITICAL	X190_RF
152S1977	1	10.0NH 3% 170MA 01005	C6202	CRITICAL	X137_RF
152S1994	1	6.8NH 3% 210MA 01005	C6202	CRITICAL	X202_RF
152S00028	1	22NH 3% 120MA 01005	L6720	CRITICAL	X190_RF
152S1979	1	18NH 1% 140MA 01005	L6720	CRITICAL	X137_RF
152S1979	1	18NH 1% 140MA 01005	L6720	CRITICAL	X202_RF
138S0831	5	MURATA 2.2UF CAPACITOR	C5101,C5121,C5122,C6010,C6011	CRITICAL	CELL

REPLACES 138S0917 - 138S0017 CAN ONLY BE USED ON RAILS WITH 3V OR LESS





PP_VCC_MAIN CURRENT SENSE



BOM ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1850	152S1721		L5101,L5103,L5104	MURATA IN, 2.2UH, 2016
152S2050	152S1857		L5902	TAIYO IND, 2.2UH, 2012

REVISION DATE: 9/29/2014

SYNC_MASTER=RADIO SYNC_DATE=09/29/2014
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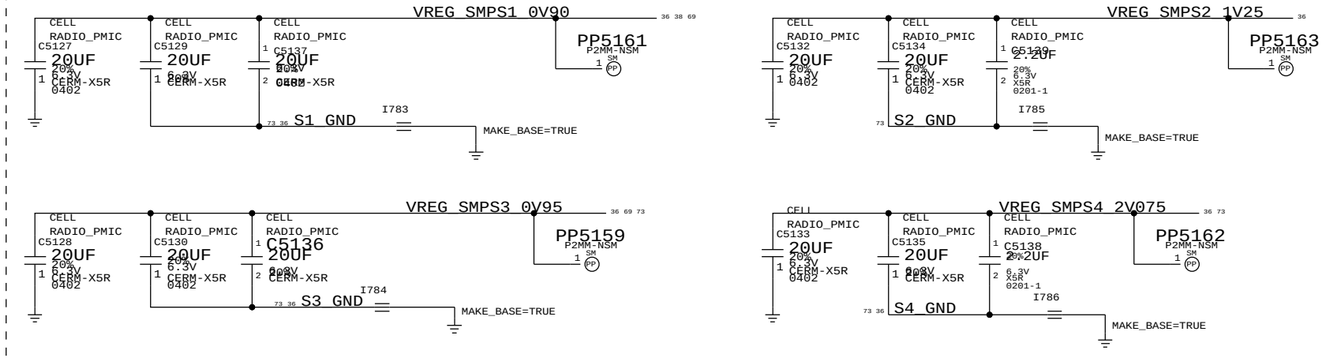
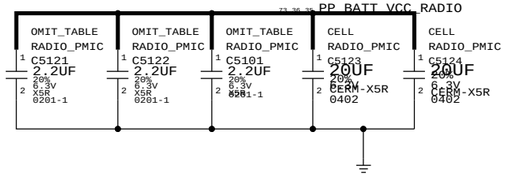
BASEBAND PMU (1 OF 2)

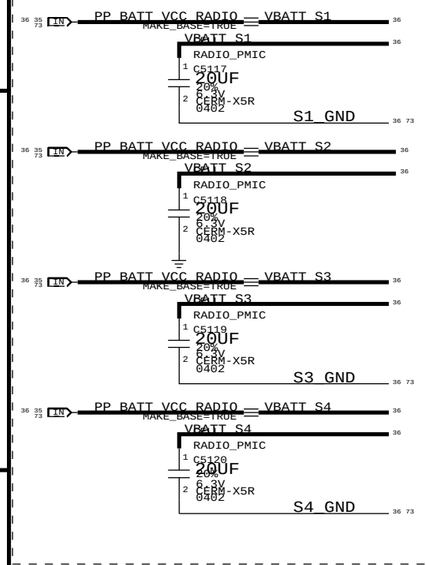
C332
R302
L304
U301

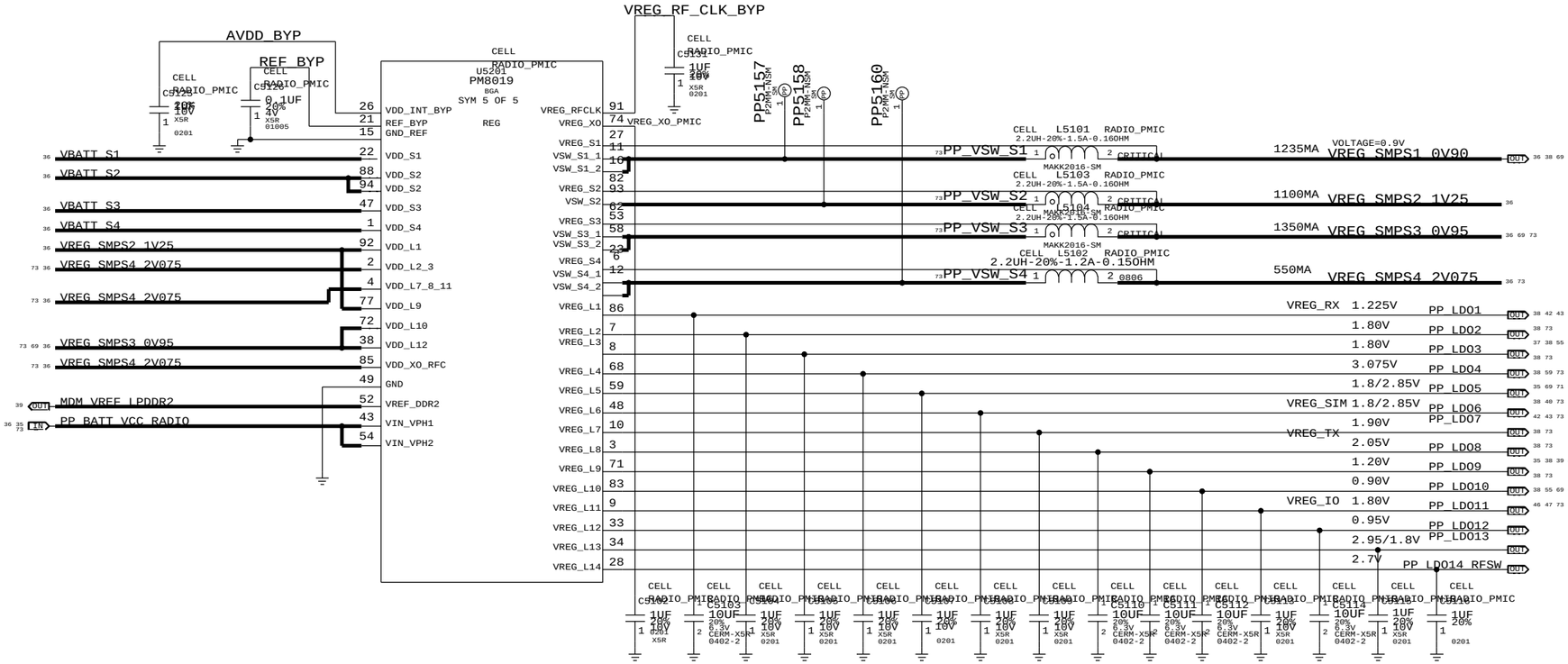
SWITCHERS OUTPUT CAPS





SWITCHERS BULK CAPS

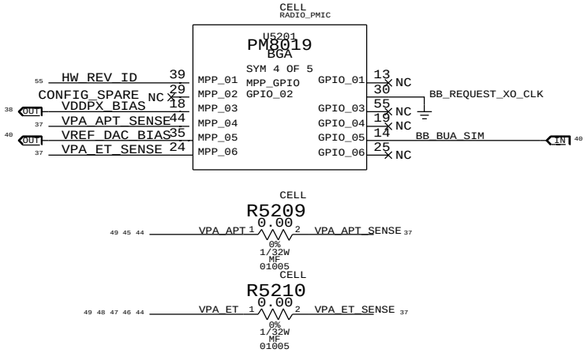


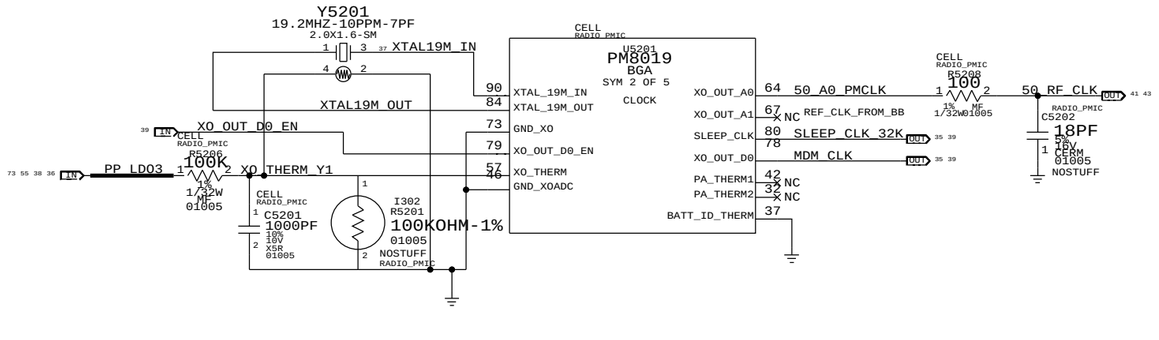


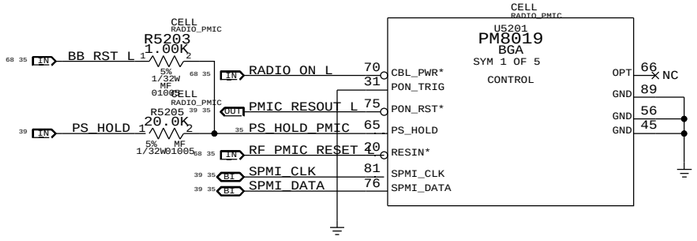
BASEBAND PMU (2 OF 2)

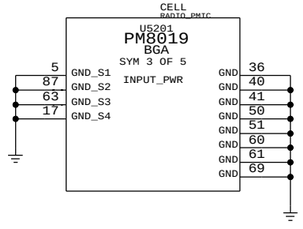
C401
R411
L400
U404

HW_REV_ID	R5202	R5207	J82 REV	J97 REV	J99 REV
0.10V	887K	51.1K	N/A	PROTO0	N/A
0.20V	422K	51.1K	PROTO0	PROTO0B	PROTO0
0.30V	255K	51.1K	PROTO1	PROTO1	PROTO1
0.40V	178K	51.1K	PROTO2		
0.50V	255K	100K	EVT		
0.60V	102K	51.1K	DVT		
0.70V	82.5K	51.1K	PVT		









PAGE TITLE
CELL: BB PMU (2/2)

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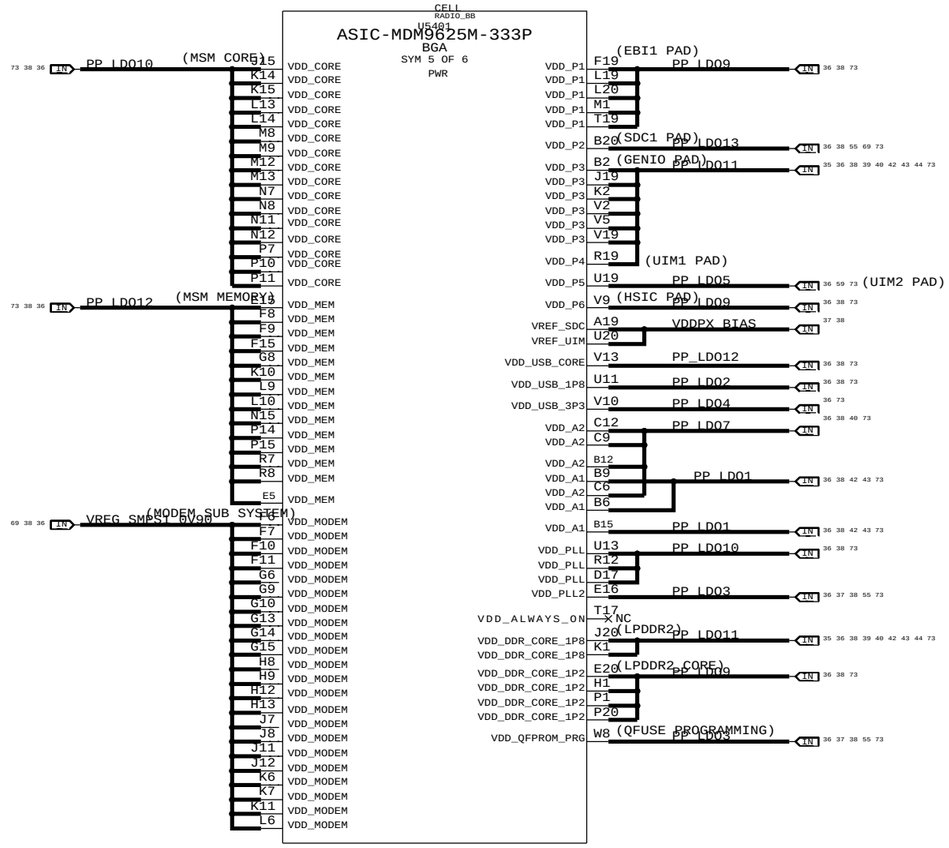
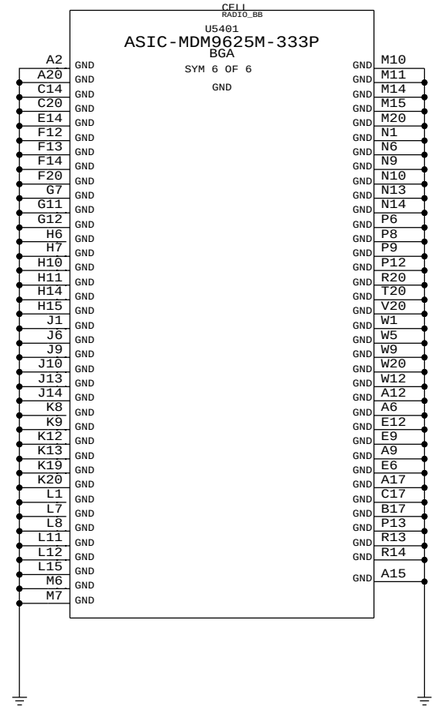
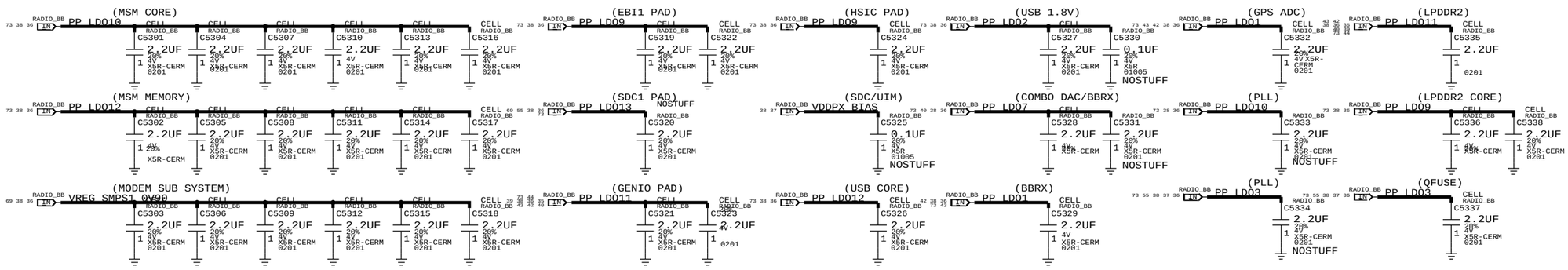
C538
R500
L500
U502







PAGE TITLE

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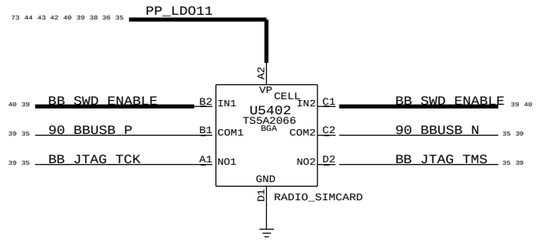
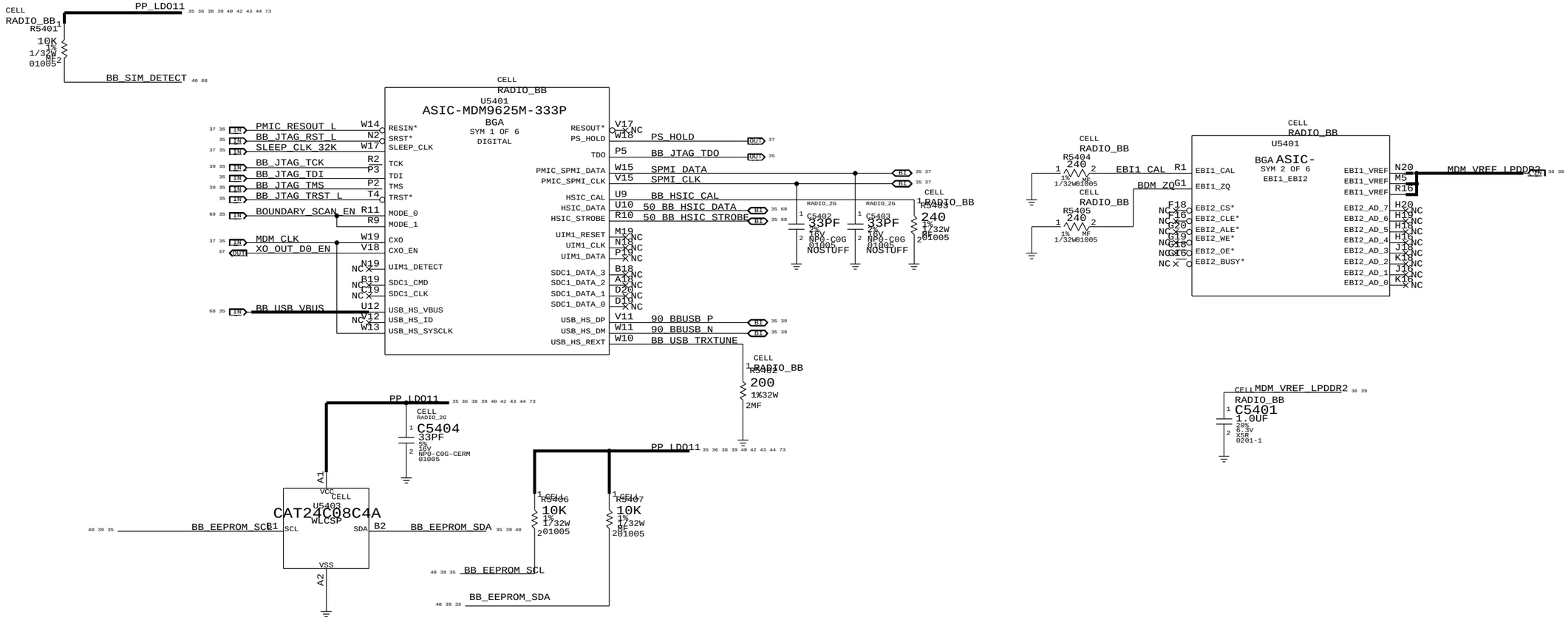
C600
R606
L600
U602





CELL: BASEBAND (2/2)

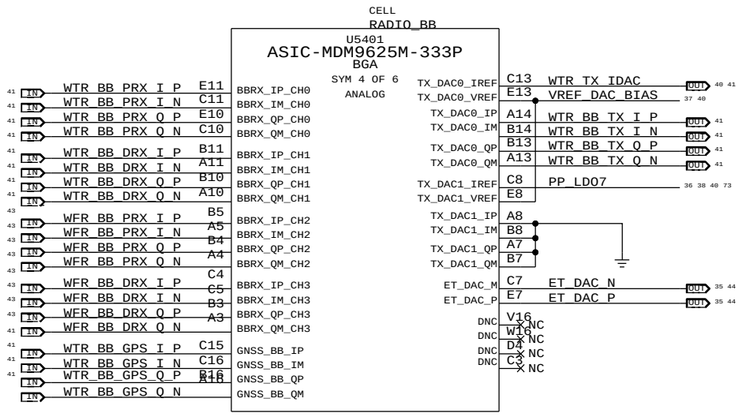
Apple Inc.

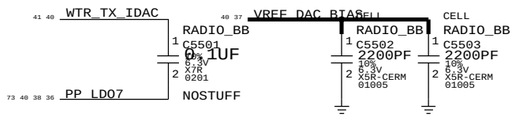
DRAWING NUMBER 051-0301
SIZE D
REVISION B.0.0
BRANCH
PAGE 54 OF 155
SHEET 39 OF 73

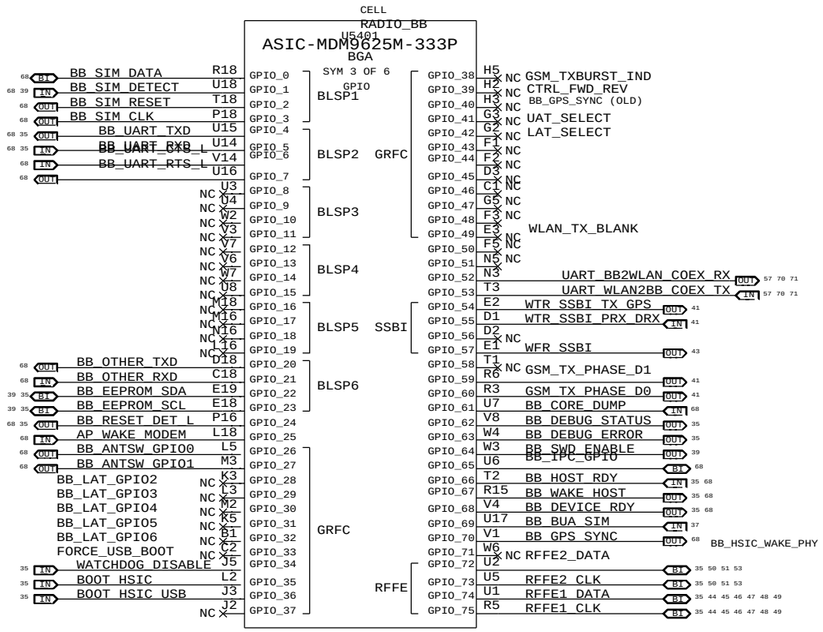
BASEBAND (3 OF 3)

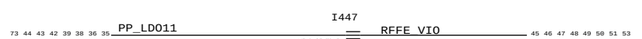
C704

U702









PAGE TITLE

CELL: BASEBAND (3/3)

Apple Inc.

DRAWING NUMBER 051-0301

SIZE D

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WTR TRANSCEIVER (1 OF 2)

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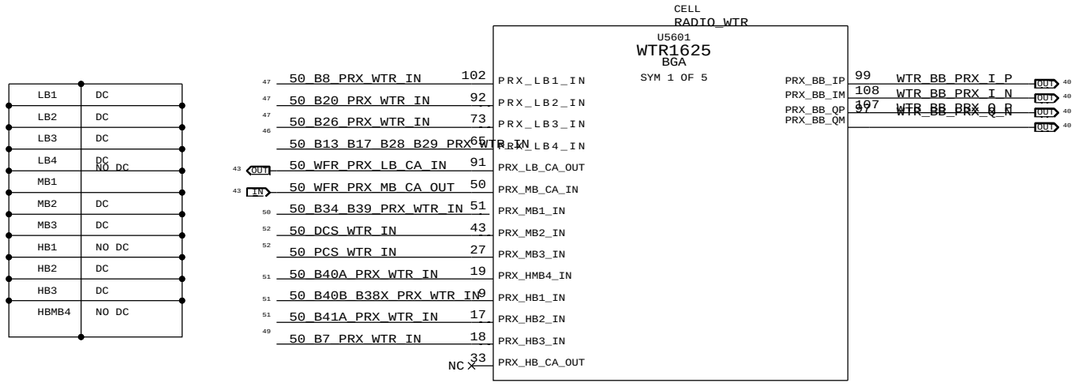
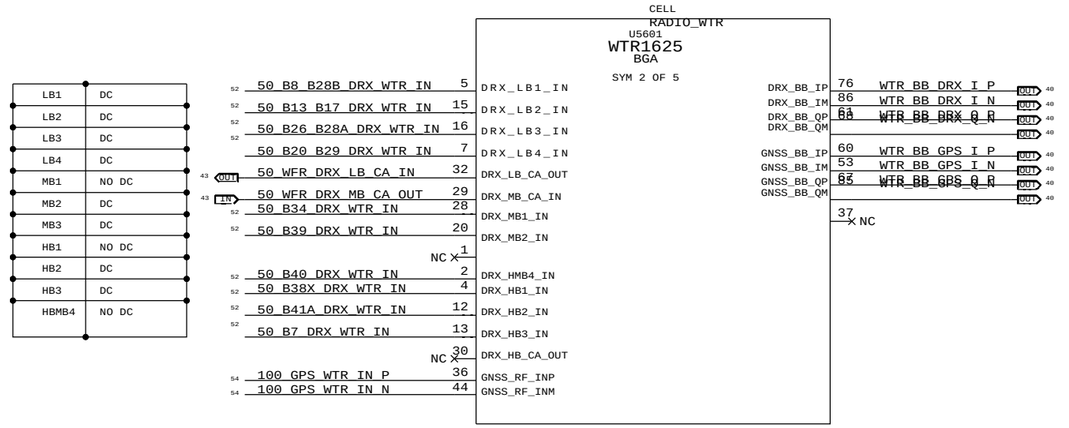
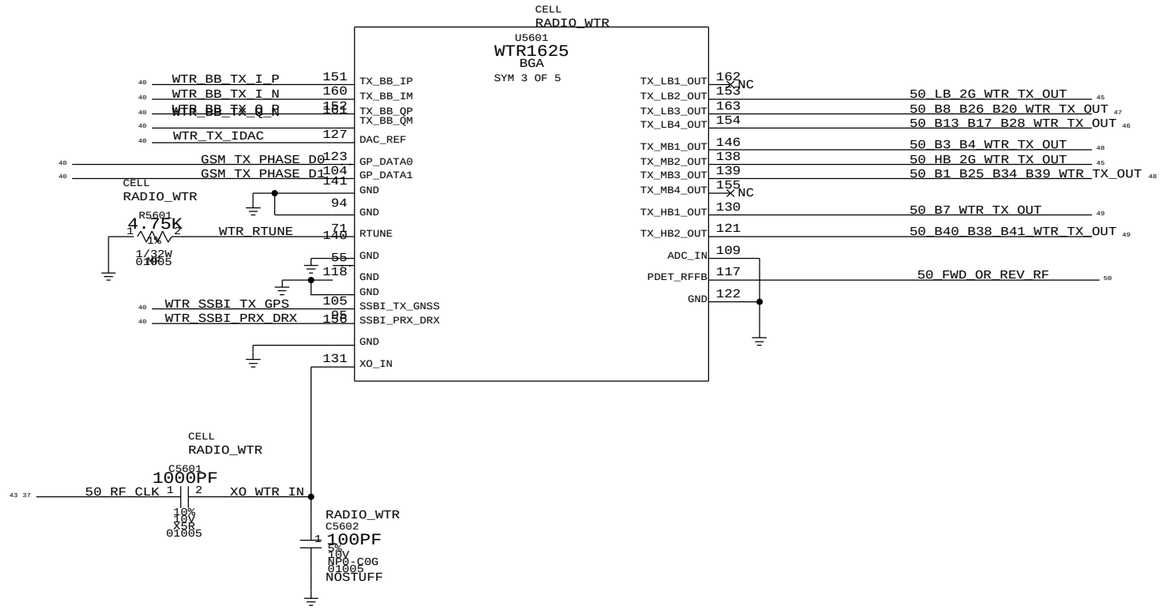
C802
R802
L800
U803







RF_CLK IS SHARED BETWEEN WTR AND WFR. LENGTH DIFFERENCE BETWEEN THE TWO SHOULD BE < 5MM.

PAGE TITLE
CELL: RF TXCVR (1/3)

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WTR TRANSCEIVER (2 OF 2)

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C934
R926
L3802_RF
U902

WTR DECOUPLING CAPS

PP_LDO8 TRUE — VREG_2V
PP_LDO1 TRUE — VREG_1P3V

R5705 0 5% 1/20W MF 201 — MAKE_BASE=TRUE — VREG_2V_FILT1
R5707 0 5% 1/20W MF 201 — MAKE_BASE=TRUE — VREG_1P3V_FILT2
L5701 22NH-3%-0.25A 0201 — VREG_1P3V_FILT2
MAKE_BASE=TRUE — VREG_1P3V_FILT2

CELL RADIO_WTR C5701 10UF 20% 6.3V CERM-X5R 0402-2
CELL RADIO_WTR C5704 10UF 20% 6.3V CERM-X5R 0402-2
CELL RADIO_WTR C5707 10UF 20% 6.3V CERM-X5R 0402-2

VDD_DRX_BB_2V — RADIO_WTR C5710 100PF 5% 10V NP0-C0G 01005 NOSTUFF
VDD_TX_DA_2V — RADIO_WTR C5711 100PF 5% 10V NP0-C0G 01005 NOSTUFF
VDD_TX_BBF_2V — RADIO_WTR C5712 100PF 5% 10V NP0-C0G 01005 NOSTUFF
VDD_PRX_BB_2V — RADIO_WTR

R5703 0.00 1% 1/20W MF 0201 — VDD_PRX_VCO_2V — RADIO_WTR C5713 0.1UF 20% 4V X5R 01005
R5704 0.00 1% 1/20W MF 0201 — VDD_SHDR_VCO_2V — RADIO_WTR C5714 0.1UF 20% 4V X5R 01005
R5702 0.00 1% 1/20W MF 0201 — VDD_TX_VCO_2V — RADIO_WTR C5715 0.1UF 20% 01005
VDD_TX_PLL_2V — RADIO_WTR C5702 0.1UF 20% 4V X5R 01005
R5706 0.00 0% 1/32W MF 01005 — VDD_XO_2V — RADIO_WTR C5703 0.1UF 10% 6.3V CERM-X5R 0201
VDD_FBRX_2V — RADIO_WTR C5716 0.1UF 20% 4V X5R 01005
I175 — VDD_PRX_2V

MAKE_BASE=TRUE — PP_LDO11 — VDD_MSM_1P8V — RADIO_WTR C5709 1.0UF 20% 6.3V X5R 0201-1 — RADIO_WTR C5717 0.1UF 20% X5R 01005 NOSTUFF

VDD_PRX_PLL_1P3V — RADIO_WTR C5718 0.1UF 20% 4V X5R 01005 NOSTUFF
VDD_SHDR_PLL_1P3V — RADIO_WTR C5719 0.1UF 20% 4V X5R 01005
VDD_PRX_HBMB_1P3V
VDD_SHDR_VCO_1P3V — RADIO_WTR C5720 0.1UF 20% 4V X5R 01005
VDD_PRX_VCO_1P3V
DELETED C3805 PR REVIEW FEEDBACK
VDD_PRX_LO_HBMB_1P3V — RADIO_WTR C5705 0.1UF 20% 4V X5R 01005
VDD_TX_SYNTH_1P3V — RADIO_WTR C5721 0.1UF 20% 4V X5R 01005
VDD_TX_LO_1P3V — RADIO_WTR C5722 0.1UF 20% 4V X5R 01005
VDD_TX_UPC_1P3V — RADIO_WTR C5723 100PF 5% 10V NP0-C0G 01005
R5708 0.00 1% 1/20W MF 0201 — VDD_TX_VCO_1P3V — RADIO_WTR C5706 0.1UF 20% 4V X5R 01005
L5702 8.2NH-3%-0.19A-1.60HM 01005 — VDD_TX_DA_1P3V — RADIO_WTR C5724 100PF 5% 10V NP0-C0G 01005 NOSTUFF

VDD_PRX_LO_HB_1P3V — RADIO_WTR C5727 0.1UF 20% 4V X5R 01005
VDD_DRX_LB_1P3V
VDD_PRX_LB_1P3V
VDD_DRX_LO2_1P3V — RADIO_WTR C5728 0.1UF 20% X5R 01005
VDD_DRX_LO1_1P3V — RADIO_WTR C5708 0.1UF 20% 4V X5R 01005
VDD_DRX_MB_1P3V
VDD_DRX_HB_1P3V
R5701 0.00 1% 1/20W MF 20201
VREG_1P3V_FILT2_GPS — MAKE_BASE=TRUE — VDD_GPS_LNA_1P3V — RADIO_WTR C5725 0.1UF 20% 4V X5R 01005
VDD_GPS_BB_1P3V
VDD_GPS_PLL_1P3V — RADIO_WTR C5726 0.1UF 20% 4V X5R 01005
VDD_GPS_VCO_1P3V — RADIO_WTR

U5601 WTR1625 BGA — SYM 4 OF 5

VDD_PRX_VCO_1P3V	90	VDD_RF1_P_VCO	
VDD_PRX_VCO_2V	80	VDD_RF2_P_VCO	
VDD_PRX_LO_HB_1P3V	25	VDD_RF1_P_HB_LO	
VDD_PRX_LB_1P3V	72	VDD_RF1_P_LB	
VDD_PRX_HBMB_1P3V	34	VDD_RF1_P_HMB	
VDD_PRX_LO_HBMB_1P3V	57	VDD_RF1_P_HMB_LO	
	79	VDD_RF1_P_PLL	
VDD_PRX_BB_2V	98	VDD_RF2_P_BB	
VDD_PRX_2V	100	VDD_RF2_P_RX	
VDD_DRX_LO1_1P3V	14	VDD_RF1_D_LB_LO	
VDD_DRX_LO2_1P3V	38	VDD_RF1_D_LOM	
VDD_DRX_LB_1P3V	31	VDD_RF1_D_LB	
VDD_DRX_HB_1P3V	22	VDD_RF1_D_HB	
VDD_DRX_MB_1P3V	11	VDD_RF1_D_MB	
VDD_DRX_BB_2V	54	VDD_RF2_D_BB	
VDD_SHDR_VCO_1P3V	48	VDD_RF1_S_VCO	
VDD_SHDR_VCO_2V	62	VDD_RF2_S_VCO	
VDD_SHDR_PLL_1P3V	78	VDD_RF1_S_PLL	

VDD_RF2_T_DA	129	VDD_TX_DA_2V	
VDD_RF1_T_DA	137	VDD_TX_DA_1P3V	
VDD_RF1_T_UPC	136	VDD_TX_UPC_1P3V	
VDD_RF1_T_LO	135	VDD_TX_LO_1P3V	
VDD_RF2_T_BB	126	VDD_TX_BBF_2V	
VDD_RF2_FBRX	116	VDD_FBRX_2V	
VDD_RF2_T_VCO	157	VDD_TX_VCO_2V	
VDD_RF1_T_VCO	149	VDD_TX_VCO_1P3V	
VDD_RF1_T_SYN	115	VDD_TX_SYNTH_1P3V	
VDD_RF2_T_PLL	114	VDD_TX_PLL_2V	
VDD_RF1_G_LNA	52	VDD_GPS_LNA_1P3V	
VDD_RF1_G_VCO	74	VDD_GPS_VCO_1P3V	
VDD_RF1_G_PLL	93	VDD_GPS_PLL__1P3V	
VDD_RF1_G_BB	59	VDD_GPS_BB_1P3V	
GND	113	PWRTERM2GND	
VDD_RF2_XO	147	VDD_XO_2V	
VDD_DIO	103	VDD_MSM_1P8V	

U5601 WTR1625 BGA — SYM 5 OF 5

GND: 89, 56, 83, 82, 58, 35, 8, 26, 64, 42, 41, 81, 21, 6, 24, 39, 10, 3, 23, 46, 49, 69, 88, 70, 63, 40, 47, 87, 77, 96

GND: 111, 101, 110, 145, 144, 143, 128, 120, 119, 106, 150, 134, 159, 142, 125, 124, 148, 158, 133, 112, 132, 45, 66, 84, 75, 164

PAGE TITLE: CELL: RF TXCVR (2/3)

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WFR TRANSCEIVER

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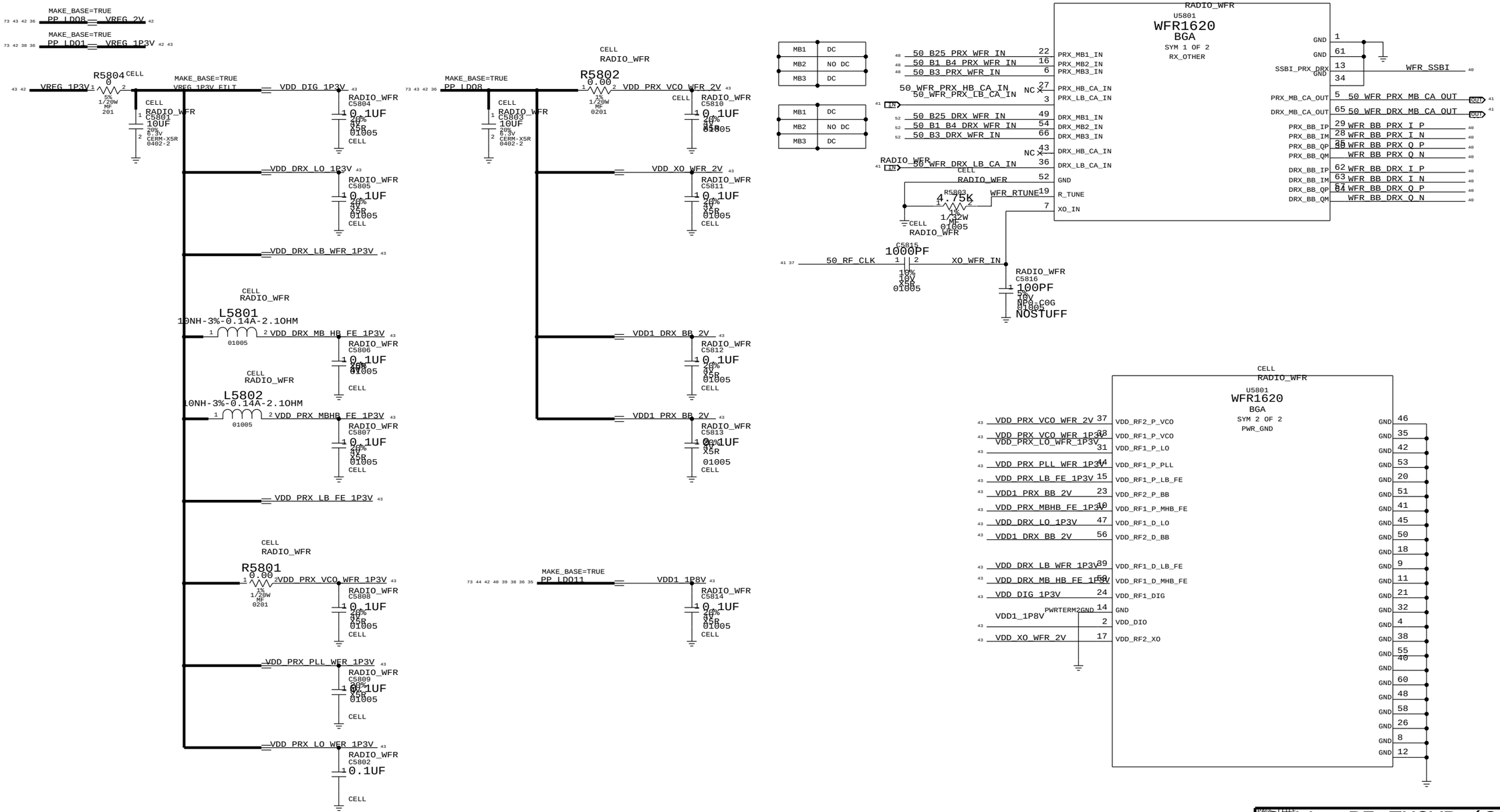
C1019
R1016
L1000
U1002



PAGE TITLE

CELL: RF TXCVR (3/3)

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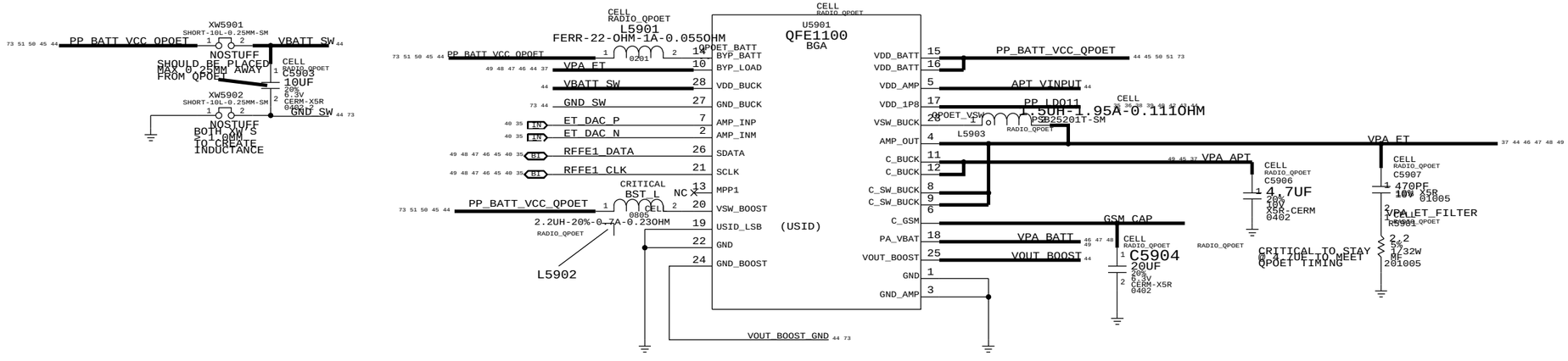
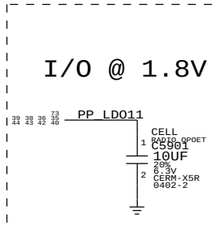
SIZE D
REVISION
BRANCH B.0.0

QFE DCDC

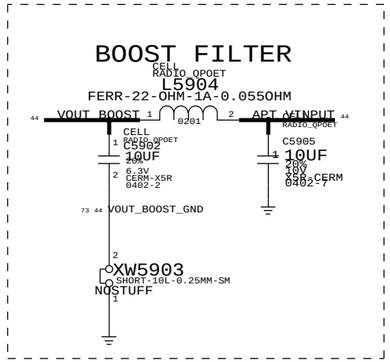
C1110
R1102
L1104
U1101



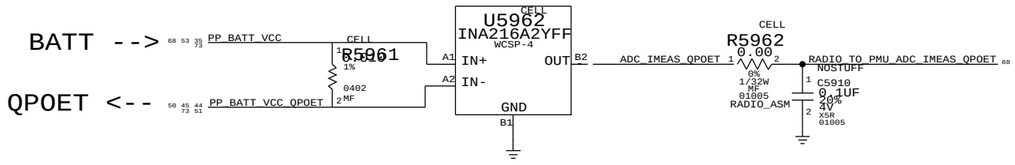
I/O @ 1.8V



BOOST FILTER



PP_VCC_MAIN CURRENT SENSE



PAGE TITLE	CELL: QFE DCDC
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BRANCH	B.0.0
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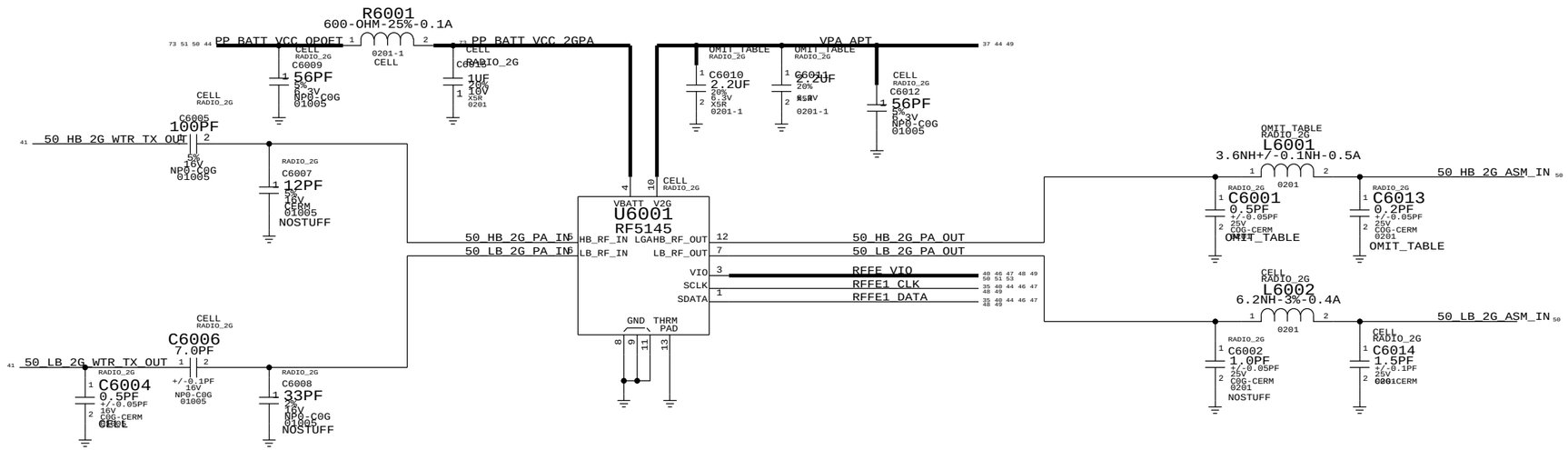
2G PA

C1208
R1200
L1204
U1201

CHANGE TO VBATT!!!!



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VERY LOW BAND PAD (B13, B17, B28)

C1332
R1300
L4215_RF
U1304

50_B28_WTR_TX_OUT
C6106 100PF 5% 10V NP0-C0G 01005
L6106 22NH-5%-0.1A 01005 NOSTUFF
50_B17_FILTER_TX_OUT
C6107 9.1NH-3%-0.17A-1.7OHM 01005
L6107 22NH-5%-0.1A 01005 NOSTUFF
50_B13_FILTER_TX_OUT
C6119 1.8NH+/-0.1%-0.380A 01005
L6108 22NH-5%-0.1A 01005 NOSTUFF
50_B28_PAD_IN
50_B17_PAD_IN
50_B13_PAD_IN
CTRL_VLB_BAND_SELECT_2
B28IN
B17IN
B13IN
SW1
SW2
RX_OUT
VPA_ET
VPA_BATT
C6112 47PF 5% 16V CERM 01005
C6113 47PF 5% 16V CERM 01005 NOSTUFF
C6109 1UF 20% 10V X5R 01005
R6101 0.00 5% 1/32W MF 01005 NOSTUFF
VLB_ET_RC_FILT
VBAT VCC1 VCC2
U6101
RF5147
LGA
B28A_ANT 50_B28A_PAD_ANT
B28B_ANT 50_B28B_PAD_ANT
B17ANT 50_B17_PAD_ANT
B13ANT 50_B13_PAD_ANT
B29_RX_IN 50_B29_PAD_ANT
VIO RFFE_VIO_VLB_PAD
SCLK RFFE1_CLK
SDATA RFFE1_DATA
GND
THRM PAD
R6102 0.00 1/32W MF 01005
RFFE_VIO
C6121 47PF 5% 16V CERM 01005
L6102 6.2NH-3%-0.22A-1.3OHM 01005
50_B28A_ASM_TRX
L6112 18NH-3%-140MA 01005 NOSTUFF
C6103 1.3PF +/-0.1PF 16V NP0-C0G 01005
L6103 9.1NH-3%-0.17A-1.7OHM 01005
PLACE INDUCTOR CLOSE TO PA
50_B28B_ASM_TRX
L6113 1.5PF +/-0.1PF 16V NP0-C0G 01005-1
C6102 1.5PF 16V NP0-C0G 01005-1
U6103 BAND17 LFL15710MTCTD717
C6117 100PF 5% 10V NP0-C0G 01005
50_B17_PAD_LPF_IN
50_B17_PAD_LPF_OUT
50_B17_ASM_TRX
L6114 2.7PF +/-0.1PF 16V NP0-C0G 01005-1
C6116 1.0PF +/-0.1PF 16V NP0-C0G 01005
L6117 22NH-5%-0.1A 01005 NOSTUFF
C6114 9.1NH-3%-0.17A-1.7OHM 01005
C6115 2.7NH+/-0.1NH-0.370A 01005
50_B13_ASM_TRX
L6115 18NH-3%-140MA 01005 NOSTUFF
L6116 15NH-3%-140MA 01005 NOSTUFF
PLACE INDUCTOR CLOSE TO PA
L6101 5.1NH-3%-0.250A 01005
50_B29_ASM_TRX
L6111 NOSTUFF 01005
C6120 100PF 5% 16V NP0-C0G 01005
50_B13_B17_B28_B29_PAD_RX
50_B13_B17_B28_B29_PRX_WTR_IN
L6118 22NH-100MA 01005
C6118 1.0PF +/-0.1PF 01005 NOSTUFF
CTRL_VLB_BAND_SELECT_1
CTRL_VLB_BAND_SELECT_2
C6105 100PF 5% 10V NP0-C0G 01005
C6108 100PF 5% 10V NP0-C0G 01005
PP_MDP014_RFSW
C6101 47PF 5% 16V CERM 01005
U6102
CXA2973GC
BGA
VDD V1 V2
RF1 50_VLB_SW_MCH_IN
RF2 50_B28_WTR_TX_OUT
RF3 50_B13_WTR_TX_OUT
RF4 50_B17_WTR_TX_OUT
C6111 47PF 5% 16V CERM 01005
50_B13_TX_FILT_IN
FL6101 SAW-BAND13-TX-INTERSTAGE B8817 LGA
INPUT_UNBAL OUTPUT_UNBAL GND
50_B13_FILTER_TX_OUT
L6110 18NH-3%-0.140A 01005-1
C6110 5.6NH-3%-0.23A-1.3OHM 01005
50_B17_WTR_FILT_IN
L6109 15NH-3%-0.140A 01005 NOSTUFF
FL6102 SAW-BAND17-TX-INTERSTAGE B8822 LGA
50_B17_FILTER_TX_OUT
C6104 100PF 5% 10V NP0-C0G 01005
50_B13_B17_B28_WTR_TX_OUT
L6104 22NH-5%-0.1A 01005 NOSTUFF
50_VLB_SW_MCH_IN
L6105 22NH-5%-0.1A 01005 NOSTUFF

V2	V1	BAND
0	1	B28
1	0	B13
1	1	B17

PAGE TITLE: CELL: VLB PAD

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LOW BAND PAD (B8, B26, B20)

C4317_RF
R1400
L4316_RF
U1402

CAPACITOR THAT'S SUPPOSED TO GO HERE IS LOCATED ON MID BAND PAD. THE 2 PAD'S NEED TO SHARE DECOUPLING

WTR OUTPUT HAS DC FIRST SHUNT MUST BE A CAPACITOR.

PLACE INDUCTOR CLOSE TO PA

PLACE INDUCTOR CLOSE TO PA

PLACE INDUCTOR CLOSE TO PA

V2	V1	BAND
0	1	B8
1	0	B20
1	1	B26

PAGE TITLE: CELL: LB PAD

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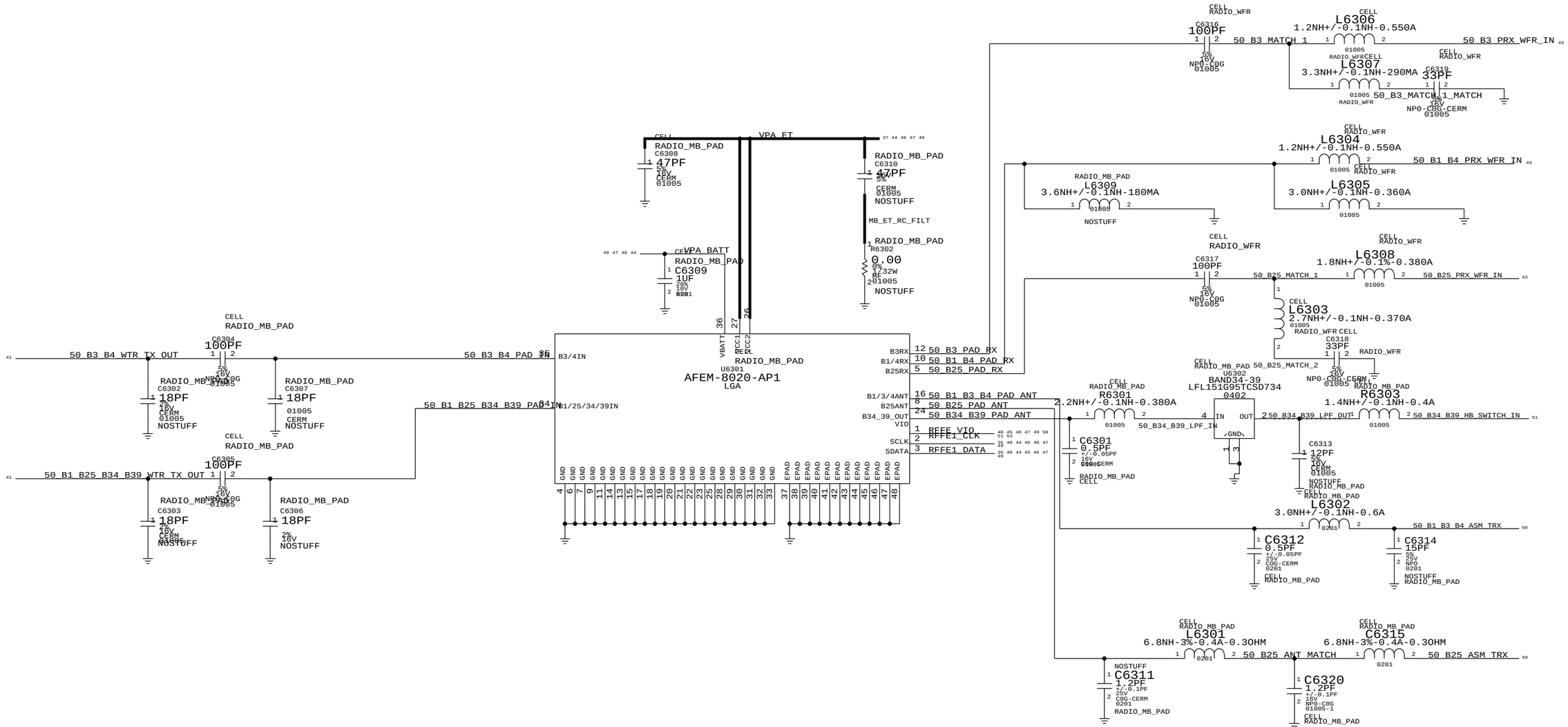
MID BAND PAD (B1, B25, B3, B4, B34, B39)

C1510
R1500
L4409_RF
U1501



PAGE TITLE	CELL: MB PAD	
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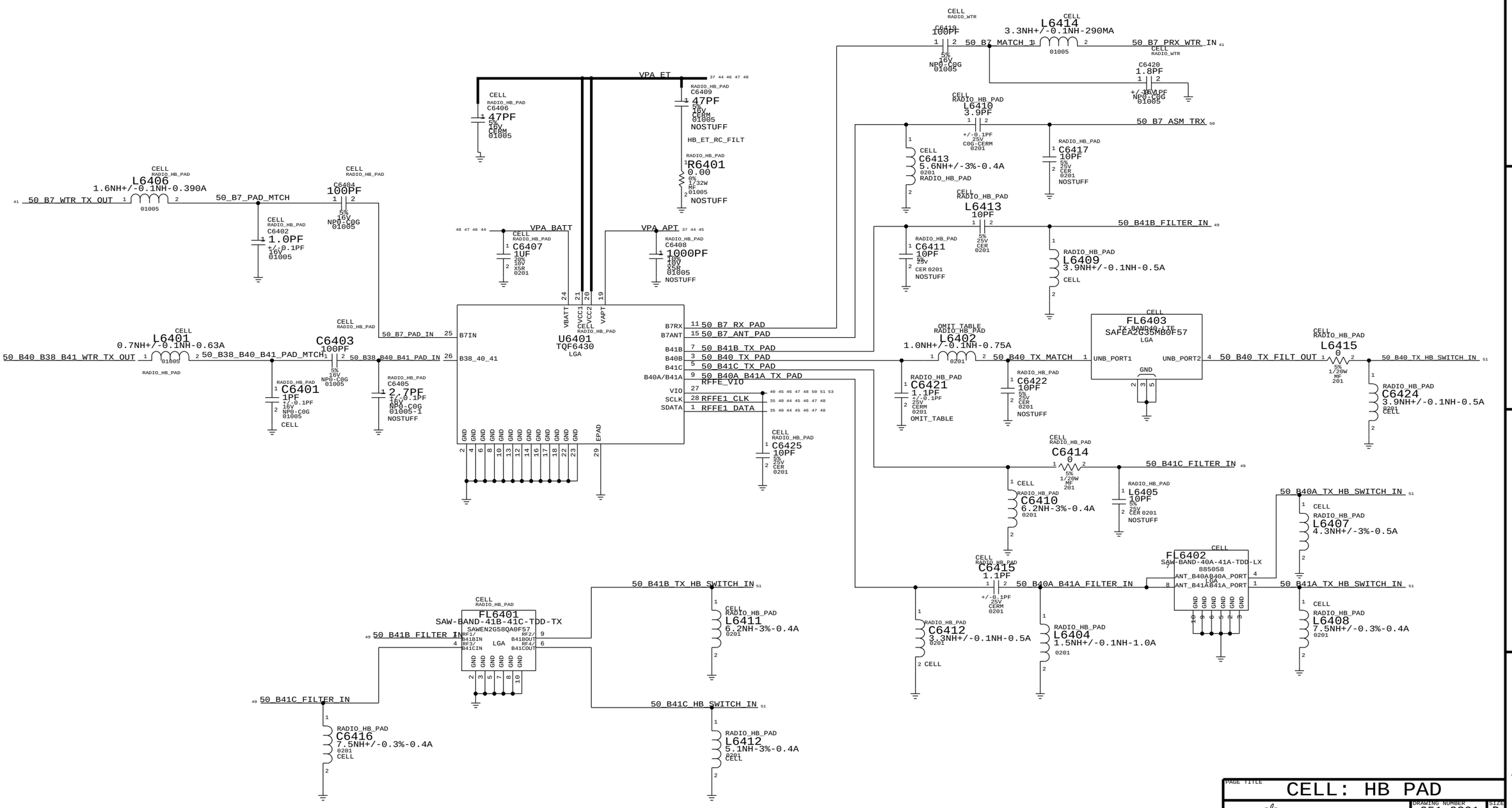
HIGH BAND PAD (B7, B38, B40, B41, XGP)

C1614
R1600
L1616
U1601



PAGE TITLE	CELL: HB PAD
	Apple Inc.
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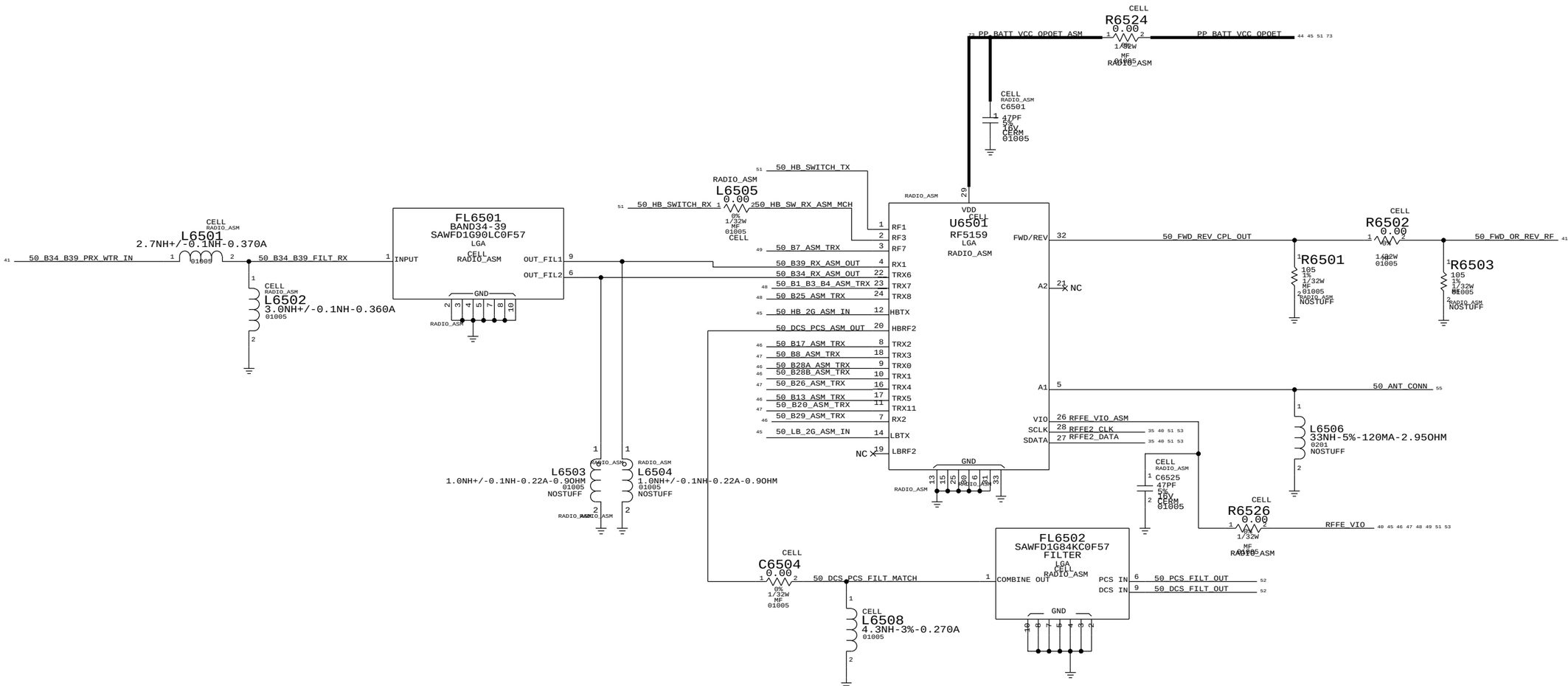
ANTENNA SWITCH

C1702
R1700
L4608_RF
U1702

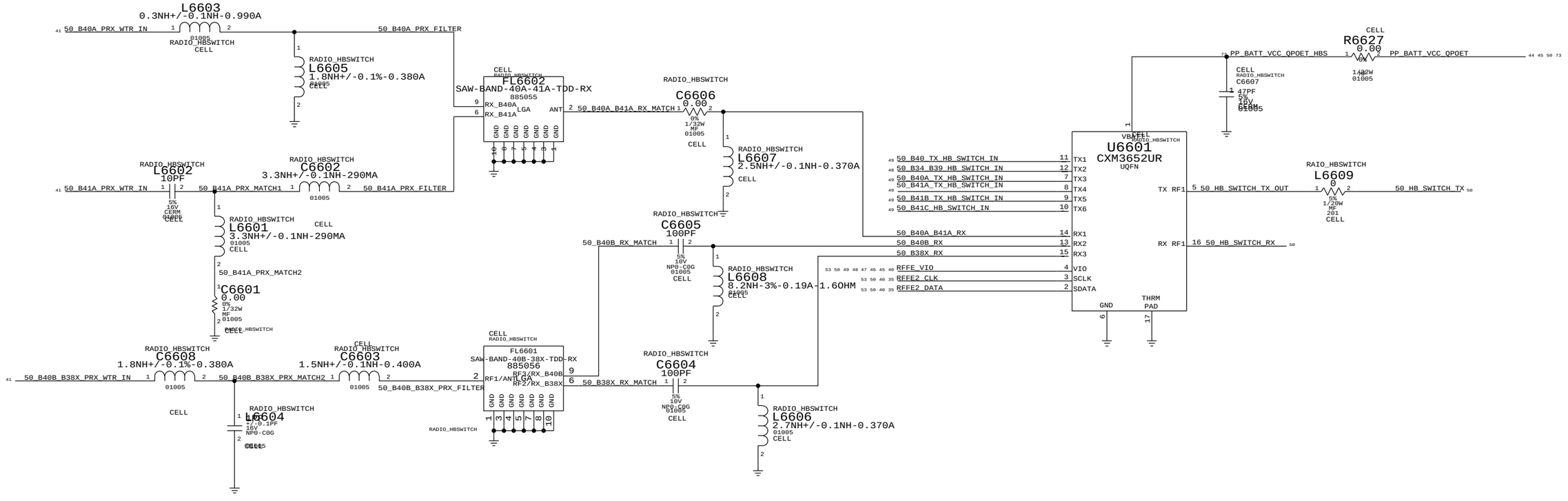


PAGE TITLE
CELL: ANTENNA SWITCH

Apple Inc.

DRAWING NUMBER 051-0301
SIZE D
REVISION
BRANCH B.0.0

HIGH BAND SWITCH



PAGE TITLE	CELL: HB SWITCH
	Apple Inc.
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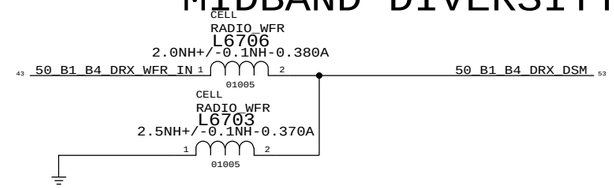
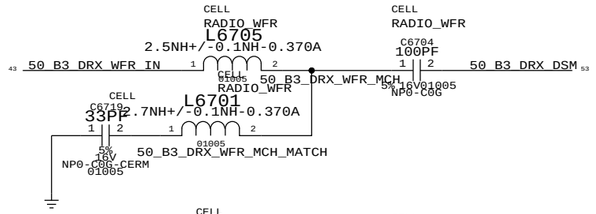
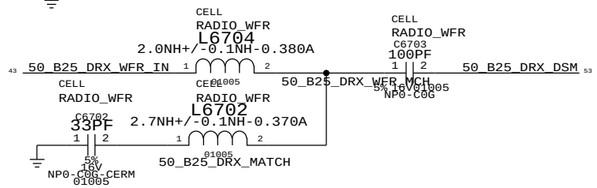
RX DIVERSITY (1 OF 2)

C4826_RF
R1800
L1829
U1801

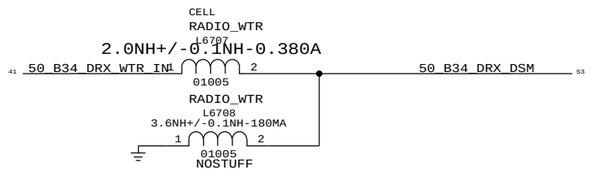
MIDBAND MIDBAND DIVERSITY - WFR

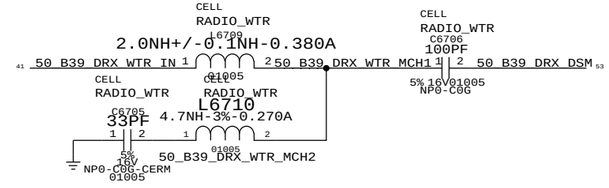




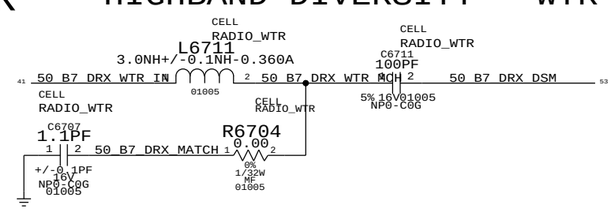


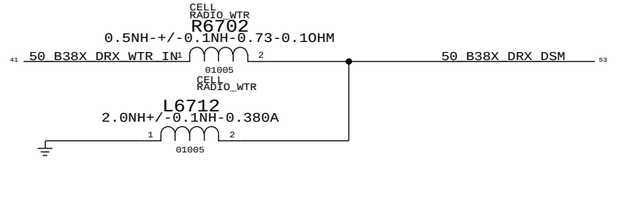
MIDBAND DIVERSITY - WTR

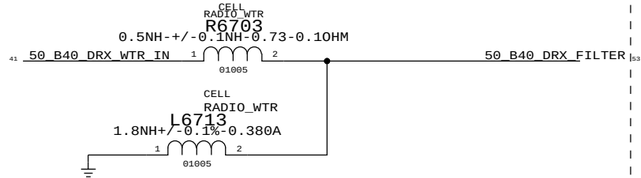


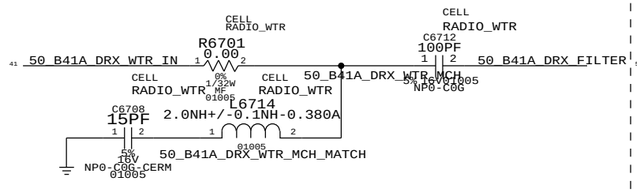


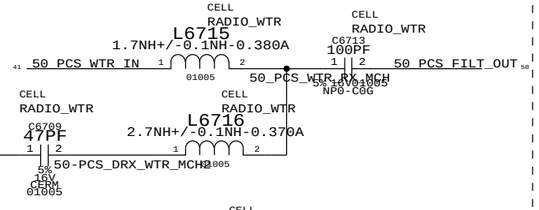
HIGHBAND DIVERSITY - WTR

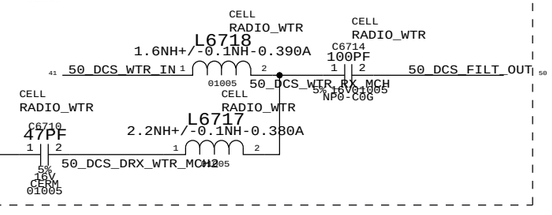




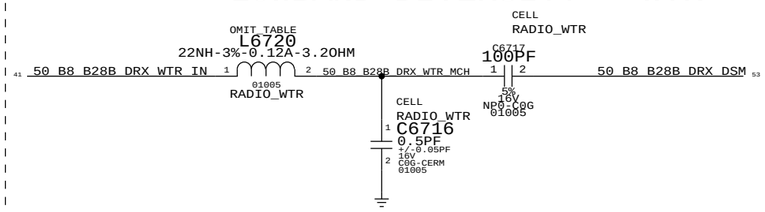


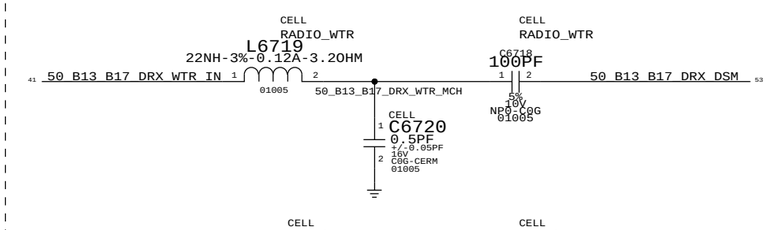


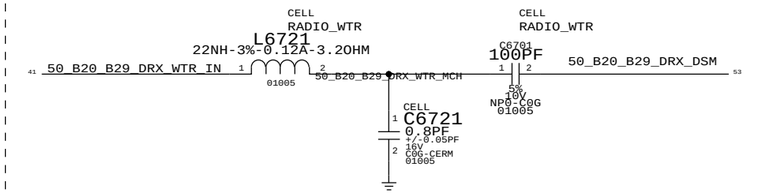


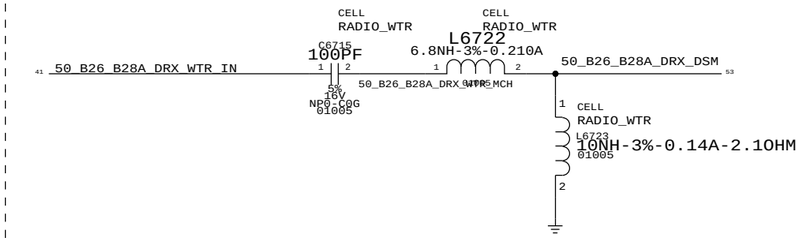


LOWBAND DIVERSITY - WTR









PAGE TITLE: CELL: RX DIV (1/2)

Apple Inc.

DRAWING NUMBER: 051-0301
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REVISION: B.0.0
BRANCH:
PAGE: 67 OF 155
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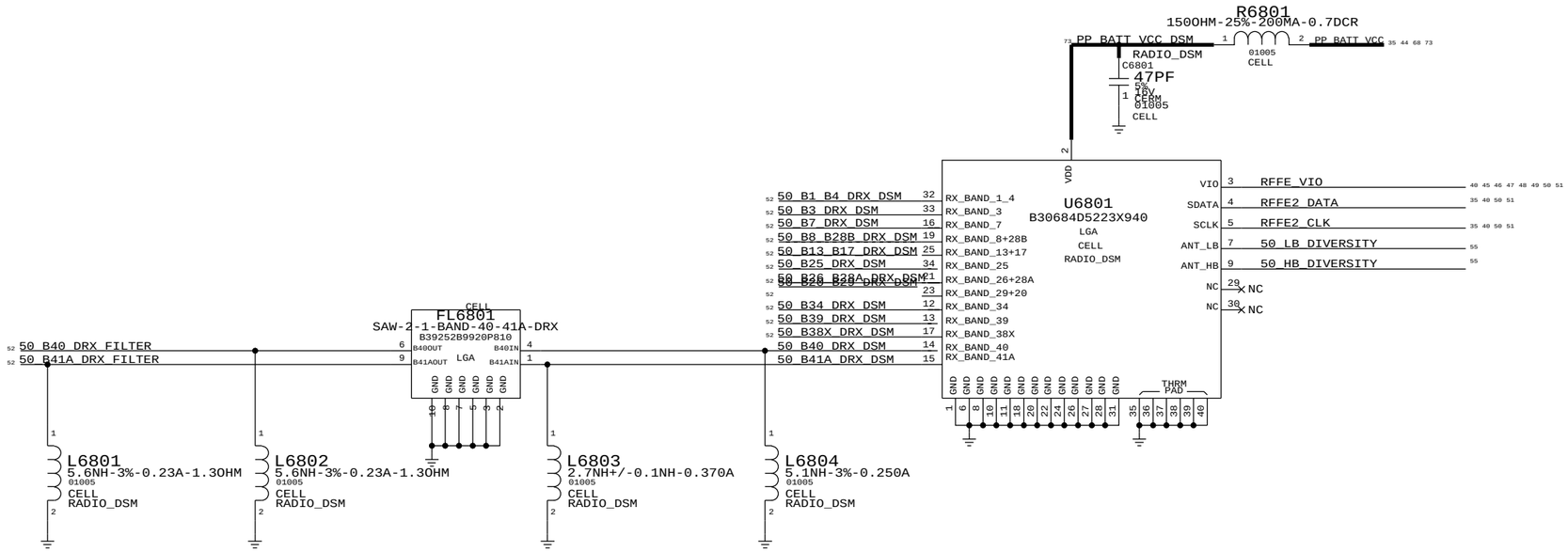
RX DIVERSITY (2 OF 2)

C1900
R1900
L1900
U1901



PAGE TITLE
CELL: RX DIV (2/2)

Apple Inc.

DRAWING NUMBER 051-0301
SIZE D
REVISION
BRANCH B.0.0

GPS

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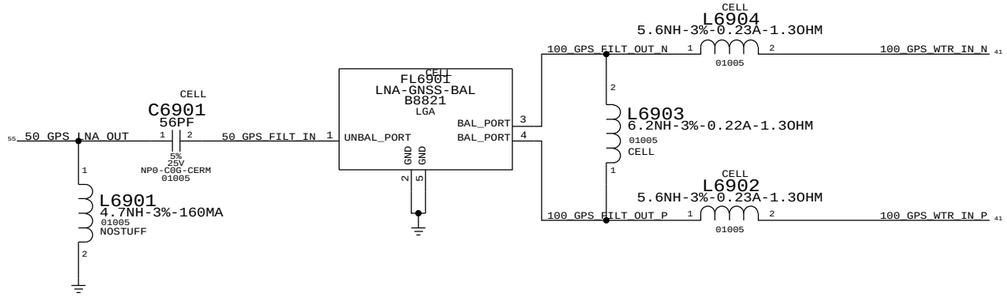

PAGE TITLE	CELL: GPS
	Apple Inc.
DRAWING NUMBER	051-0301
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NOTICE OF PROPRIETARY PROPERTY:

ANTENNA FEEDS AND GPS (J82)

PRI_ANT COAX

CRITICAL CELL
J7001
MM5829-2700
F-ST-SM

50_ANT_CONN

GPS_DRX_ANT

CELL CRITICAL
J7410
MM4829-2702
F-ST-SM

50 GPS DRX WIFI G0 ANT COAX

CELL
DPX162690DT-8049C1SJ
FL7003
SM

50 LB DIVERSITY
LOW_BAND
HIGH_BAND
COMMON
GND

50 GPS HB WIFI G0

CELL
R7001
0
5%
1/20W
MF
201

C7001
0.2PF
+/-0.1PF
25V
C0G-CERM
201
NOSTUFF

50 GPS DRX WIFI G0 NOTCHPLEXER

L7003
3.2NH+/-0.1NH-0.5A
0201
CELL

50 NOTCHPLEXER SMD2

C7002
7.5NH+/-0.3%-0.4A
0201
NOSTUFF

CELL
FL7002
885000
DIPLEXER-CELL-WIFI
LGA

RF1
SMD2_RF1/SMD4_GND
RF3
RF2
SMD1_RF2
GND

50 GPS DRX NOTCHPLEXER

50 NOTCHPLEXER SMD1

L7002
3.6NH+/-0.1NH-0.5A
0201
CELL

50 WIFI G1

CELL
R7002
6.8PF
+/-0.1PF
25V
C0G
0201

50 NOTCHPLEXER MATCH

C7004
6.8PF+/-3%-0.4A
0201

CELL
J7004
MM8830-2600B
F-RT-SM

50 GPS DRX SW CONN

CELL
L7004
0.3PF
+/-0.1PF
25V C0G-CERM
201

CELL
R7004
1.8NH+/-0.1NH-0.8A
0201

50 GPS EXTRACT ANT

NOSTUFF
L7005
5.6NH-3%-0.35A
0201

R7003
150OHM-25%-200MA-0.7DCR
01005
CELL

PP_LDO13_GPS
PP_LDO13

OLD: LDO6
NEW: LDO13

BYPASS INTEGRATED INTO MODULE

CELL
U7001
LNA-CELL-GPS
LGA

VDD
GPS_OUT
ANT
TBD
CELL_OUT
GND
EPAD

50 GPS LNA OUT

CELL
R7005
0
5%
1/20W
MF
201

50 EXTRACT DRX
50 HB DIVERSITY

C7006
0.2PF
+/-0.1PF
25V
C0G-CERM
201
NOSTUFF

J82 HW_ID (MAPPING PG 52)

EVT

RADIO_PMIC
PP_LDO3

R7010
102K
1%
1/32W
MF
01005
CELL

HW_REV_ID

R7011
51.1K
1%
1/32W
MF
01005
CELL

HW_REV_ID	R7010	R7011	J82 REV	J97 REV	J99 REV
0.10V	887K	51.1K	N/A	PROTO0	PROTO0
0.20V	422K	51.1K	PROTO0	PROTO0B	PROTO1
0.30V	255K	51.1K	PROTO1	PROTO1	PROTO2
0.40V	178K	51.1K	PROTO2		
0.50V	255K	100K	PRE-EVT		
0.60V	102K	51.1K	EVT		
0.70V	82.5K	51.1K	DVT		

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0565	197S0598		Y5201	KDS XTAL, 19.2MHZ
197S0593	197S0598		Y5201	NDK XTAL, 19.2MHZ

SYNC DATE=09/29/2014

PAGE TITLE
CELL: ANT FEEDS & GPS (J82)

Apple Inc.

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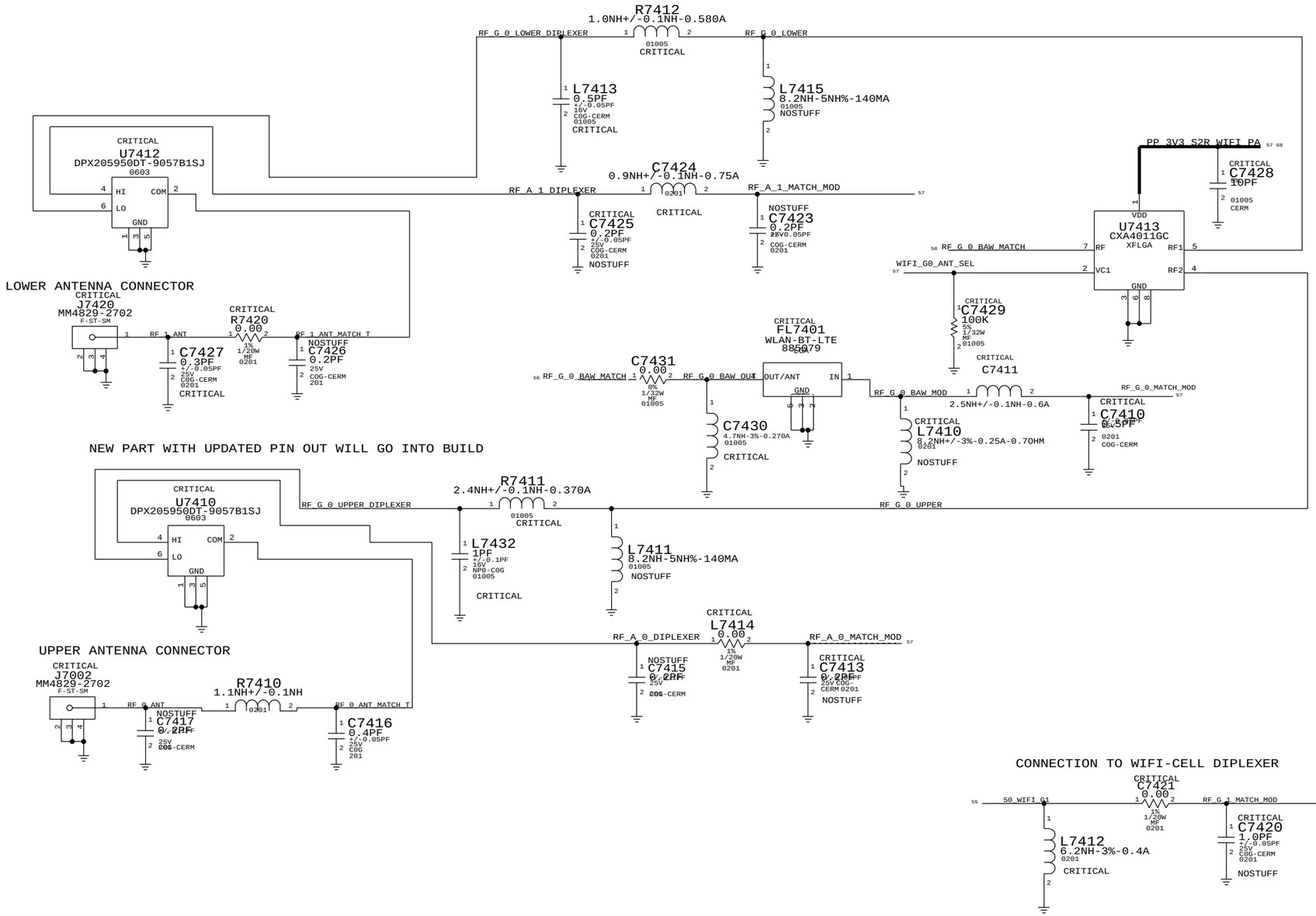
WIFI/BT (2 OF 5)
WIFI/BT FRONT END FOR J82



PAGE TITLE
WIFI/BT: J82 ANT INTERFACE

Apple Inc.

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WIFI/BT (3 OF 5)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0251	1	MODULE, WIFI/BT, STELLA CIDRE	U7500	CRITICAL	MLB_A
339S0241	1	MODULE, WIFI/BT, STELLA	U7500	CRITICAL	MLB_B

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0250	339S0251	MLB_A	U7500	STELLA CIDRE ALT
339S0229	339S0241	MLB_B	U7500	STELLA ALT

NOTE* PIN5 SHOULD BE NC FOR J81/J96/J97/J98/J99

U7500
LBEE5UAZLC-670
LGA
SYM 2 OF 2
OMIT_TABLE

GND: 15, 19, 23, 24, 26, 27, 29, 30, 32, 33, 34, 36, 37, 38, 40, 57, 59, 64, 67, 69, 72, 75, 78

THRM_PAD: 81–113, 114–170

PP_1V8_S2R_VDDIO_WLAN_BT → R7513 0.00 (0% 1/32W MF 01005) → PP_WL_VDDIO
C7501 27PF (5% 16V NP0-C0G 01005)
C7500 0.01UF (10% 6.3V X5R 01005)

PP_VCC_MAIN_WLAN
C7583 4.7UF (20% 6.3V X5R-CERM1 402)
C7584 4.7UF (20% 6.3V X5R-CERM1 402)

PP_3V3_S2R_WIFI_PA
C7580 4.7UF (20% 6.3V X5R-CERM1 402)
C7581 10UF (20% 6.3V CERM-X5R 0402-2)
C7582 10UF (20% 6.3V CERM-X5R 0402-2)

U7500
LBEE5UAZLC-670
LGA
339S0229 2
CRITICAL
MODULE_INST
OMIT_TABLE

VDDIO_1P8	11		
BATT_VCC	58		
BATT_RF_VCC	25		
BATT_RF_VCC	35		
CLK_PMU2WLAN_32K	68	CLK32K_AP	
UART_SOC2WLAN_TX	48	FAST_UART_RX	
UART_WLAN2SOC_RX	54	FAST_UART_TX	
WLAN_GPIO_8	53	WL_GPIO_8	
UART_WLAN2SOC_CTS_L	46	FAST_RTS_OUT	
GPIO_PMU2WLAN_REG_ON	60	WLAN_REG_ON	
GPIO_PMU2BT_REG_ON	56	BT_REG_ON	
JTAG_WLAN_SEL	45	JTAG_SEL	
	NC	ANT_SWITCH_CORE1	
WIFI_G0_ANT_SEL	5	ANT_SWITCH_CORE0	
WLAN_GPIO_10 / GPIO_SOC2WLAN_PCIE_DEV_WAKE	NC	HSIC_WLAN_DATA	
	NC	HSIC_WLAN_STROBE	
	47	HSIC_DEV_RDY	
	61	HSIC_HOST_READY_PCIE_DEV_WAKE	
	62	HSIC_RESUME_FAST_CTS_IN_JTAG_TCK	
JTAG_WLAN_TMS	63	JTAG_TMS	
JTAG_WLAN_TRST	44	JTAG_TRST	
WLAN_SECI_IN	43	SEC_IN/JTAG_TDI	
UART_WLAN2BB_COEX_TX	42	SEC_OUT/JTAG_TDO	
GPIO_BT2PMU_HOST_WAKE	17	HOST_WAKE_BT	
RF_G_0_MATCH_MOD	22	2G_CORE0_ANT	
RF_G_1_MATCH_MOD	31	2G_CORE1_ANT	
RF_A_0_MATCH_MOD	28	5G_CORE0_ANT	
RF_A_1_MATCH_MOD	39	5G_CORE1_ANT	
BT_EXT_SYNC	20	BT_GPIO3	
BT_EXT_CLK	21	BT_GPIO5	
	41	NC	

R7500 10K (5% 1/32W MF 01005) — UART_SOC2WLAN_RTS_L
R7592 0.00 (0% 1/32W MF 01005) — UART_SOC2WLAN_RTS_L_RES

R7589 0.00 (0% 1/32W MF 01005) — UART_BB2WLAN_COEX_RX → JTAG_WLAN_TRST

BT_GPIO4	10	NC	
BT_WAKE	16	GPIO_SOC2BT_WAKE	
BT_USB_DP	3	NC	
BT_USB_DN	4	NC	
BT_UART_RXD	13	UART_SOC2BT_TX	
BT_UART_TXD	12	UART_BT2SOC_RX	
BT_UART_CTS*	9	UART_SOC2BT_RTS_L	
BT_UART_RTS*	8	UART_BT2SOC_CTS_L	
BT_PCM_CLK	6	I2S_SOC2BT_BCLK	
BT_PCM_SYNC	18	I2S_SOC2BT_LRCK	
BT_PCM_OUT	14	I2S_BT2SOC_DIN	
BT_PCM_IN	7	I2S_SOC2BT_DOUT	
WL_GPIO_9	52	WLAN_GPIO_9	OSCAR_CONTEXT_A
WL_GPIO_13	51	OSCAR2RADIO_CONTEXT_B	
WL_HOST_WAKE	55	GPIO_WLAN2PMU_HOST_WAKE	
WLAN_PCIE_PME	79	PCIE_WLAN2PMU_WAKE_L	
WLAN_PCIE_CLKREQ	80	PCIE_WLAN2SOC_CLKREQ	
WLAN_PERST	1	PCIE_SOC2WLAN_PERST	
WLAN_PCIE_RDP0	77	PCIE_SOC2WLAN_TX_P	
WLAN_PCIE_RDN0	76	PCIE_SOC2WLAN_TX_N	
WLAN_PCIE_TDP0	73	PCIE_TX_P	
WLAN_PCIE_TDN0	74	PCIE_TX_N	
WLAN_PCIE_REFCLKP	71	PCIE_SOC2WLAN_CLK_P	
WLAN_PCIE_REFCLKN	70	PCIE_SOC2WLAN_CLK_N	
WL_UART_RX	50	WL_UART_RX	
WL_UART_TX	49		

C7589 0.1UF (20% 6.3V X5R-CERM 01005) — PCIE_WLAN2SOC_RX_P
C7590 0.1UF (20% 6.3V X5R-CERM 01005) — PCIE_WLAN2SOC_RX_N

PP7590 P4MM SM — WL_UART_RX
PP7591 P4MM SM — WL_UART_TX

BOOTSTRAP CONFIGURATION

PP_1V8_S2R_VDDIO_WLAN_BT
R7586 10K (5% 1/32W MF 01005)
R7587 10K (5% 1/32W MF 01005)
R7590 10K (5% 1/32W MF 01005) — GPIO_PMU2WLAN_REG_ON → WLAN_REG_RC
R7585 10K (5% 1/32W MF 01005)

GPIO 10 → WLAN_GPIO_10
GPIO 09 → WLAN_GPIO_9
GPIO 08 → WLAN_GPIO_8

GPIO [10:8] = 011 FOR PCIE

C7592 0.01UF (10% 6.3V X5R 01005)
U7503 74AUC1G126 BGA-YZP
OSCAR2RADIO_CONTEXT_A → WLAN_GPIO_9
C7588 4.7UF (20% 6.3V X5R-CERM1 402)

LAST UPDATED: 11/6/2013

SYNC_MASTER=WIFI	SYNC_DATE=09/29/2014
PAGE TITLE	WIFI/BT: WIFI/BT MODULE
Apple Inc.	DRAWING NUMBER 051-0301
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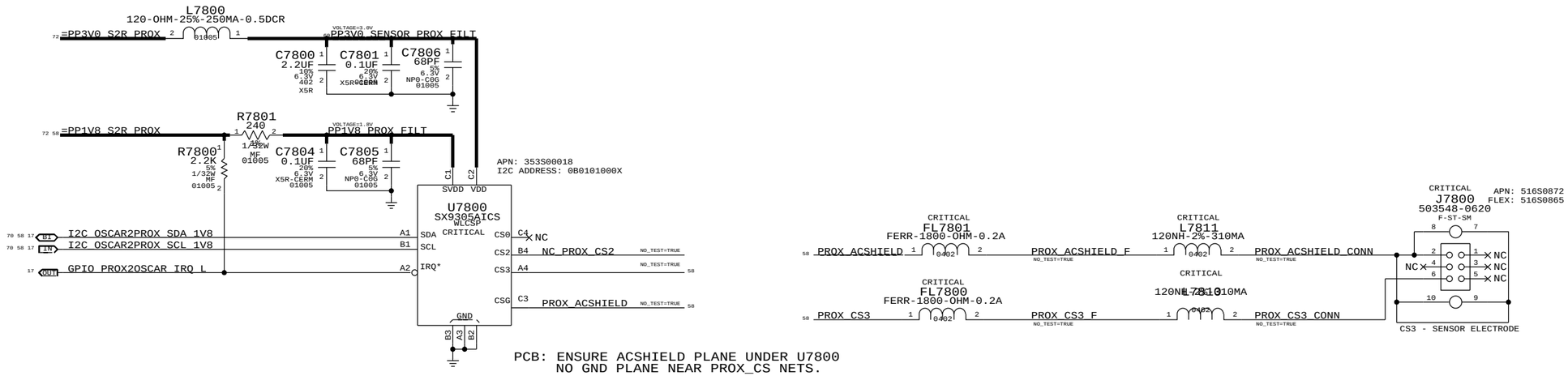
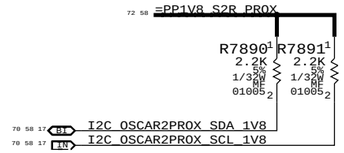


PCB: ENSURE ACSHIELD PLANE UNDER U7800
NO GND PLANE NEAR PROX_CS NETS.

PCB: ACSHIELD NEEDS TO BE A PLANE UNDER
PROX_CS NETS AND ALSO TIE TO CONNECTOR.



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PAGE TITLE: SENSOR: HAMMERHEAD

Apple Inc.

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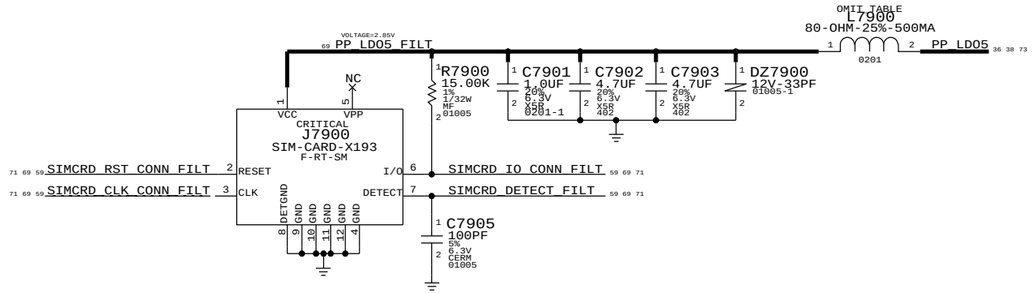
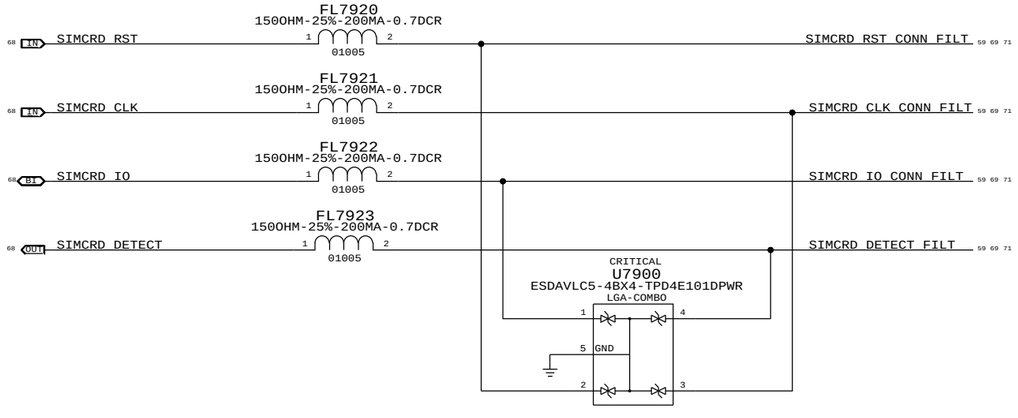
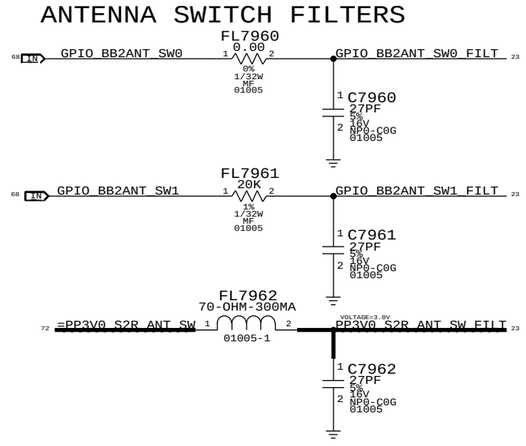
SIM CARD AND ANTENNA SWITCH FILTERS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S00018	1	FERRITE,800HM,25%,500MA,0.18DCR	L7900	CRITICAL	







SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
CELL: SIM AND ANT SW FILT

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D

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REPURPOSED CAPS TO BE PLACED NEAR BB VBATT

PLACE NEAR CODEC

U8100
D2207A0
BGA
SYM 1 OF 4

OMIT_TABLE

VCC_MAIN BYPASS
PLACE TWO 10UF CAP AT EACH VDD INPUT

C8137 0201 OKAY IF GRAPE HAS EXT FET

ADDITIONAL DISTRIBUTED 910F (NO DERATING) PPVDD_CPU

ADDITIONAL DISTRIBUTED 65UF (NO DERATING) PPVDD_GPU

ADDITIONAL DISTRIBUTED 31UF (NO DERATING) PP0V95_SOC

ADDITIONAL DISTRIBUTED 40UF (NO DERATING) PP1V8_S2R

ADDITIONAL DISTRIBUTED 94UF (NO DERATING) PP1V2_S2R

ADDITIONAL DISTRIBUTED 26UF (NO DERATING) PPVDD_SRAM

ADDITIONAL DISTRIBUTED 25UF (NO DERATING) PP3V3_S2R

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
PMU: ARABELA (1/3)

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D
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PCB: ADD A VIA PER PIN FOR ALL VSS_* AND VSSA_* PINS

U8100
D2207A0
BGA
SYM 4 OF 4
OMIT_TABLE

H1 H2 VSS_BUCK01
D1 D2 VSS_BUCK1_12
M1 M2 VSS_BUCK0_12
W4 Y4 VSS_BUCK2
Y1 Y2 Y3 VSS_BUCK4
A3 B3 VSS_BUCK5
W8 Y8
A7 B7 VSS_BUCK56
T1 T2 VSS_BUCK04
D18 VSS_WLED
D19
B18
A1 A2 A19 C3 C4 C5 C6 C8 C11 C14 D3 D12 D13 E3 E15 E17 F3 F7 F8 F9 F10 F11 F12 F13 F15 G3 G7 G8 G9 G10 G11 G12 G13 G15 H3 H7 H8 H9 H10 H11 H12 H13 H15 J3 J7 J8 VSS

J9 J10 J11 J12 J13 K3 K7 K8 K9 K10 K11 K12 K13 K15 L3 L7 L8 L9 L10 L11 L12 L13 L15 M3 M7 M8 M9 M10 M11 M12 M13 M16 N3 N7 N8 N9 N10 N11 N12 N13 N15 P3 P7 P8 P9 P10 P11 P12 P13 P15 R3 R7 R8 R9 R10 R11 R12 R13 R15 T3 T8 T10 U3 U9 U19 V3 V5 V6 V7 V9 W3 Y19 VSS

VOLTAGE=0V

LDO INPUTS

72 69 60 PP1V8_S2R — 1 CAP PER PIN
C8200 1UF 10% 6.3V 2 402
C8203 1UF 10% 6.3V 2 402

72 69 60 PP1V2_S2R
C8201 1UF 10% 6.3V CERM 2 402

72 69 65 64 61 60 PPVCC_MAIN

U8100
D2207A0
BGA OMIT_TABLE
SYM 2 OF 4

LDO INPUT
VDD_LDO1_3_4 V17
VDD_LDO2 C13
VDD_LDO5 B13
VDD_LDO6 B12
VDD_LDO7 B14
VDD_LDO8 W18
VDD_LDO9 B16
VDD_LDO10 B17
VDD_LDO11 C15
VDD_LDO13 W17
VDD_LDO14 C16

LCD BACKLIGHT / LCM/GRAPE
WLED_LXA0 C18
WLED_LXA1 C19
VOUT_WLED_A D16
WLED1_A E14
WLED2_A F14
WLED3_A G14
WLED4_A H14
WLED5_A J14
WLED6_A J15
WLED_LXB0 E18
WLED_LXB1 E19
VOUT_WLED_B E16
WLED1_B K14
WLED2_B L14
WLED3_B M14
WLED4_B M15
WLED5_B N14
WLED6_B P14

70 63 WLED_LX_A
63 =PPLED_PMU_OUT_A
63 LN LED_PMU_1_A
63 LN LED_PMU_2_A
63 LN LED_PMU_3_A
63 LN LED_PMU_4_A
63 LN LED_PMU_5_A
63 LN LED_PMU_6_A
70 63 WLED_LX_B
63 =PPLED_PMU_OUT_B
63 LN LED_PMU_1_B
63 LN LED_PMU_2_B
63 LN LED_PMU_3_B
63 LN LED_PMU_4_B
63 LN LED_PMU_5_B
63 LN LED_PMU_6_B

LDO OUTPUTS

VLDO1 U18 (50MA; 2.5-3.3V) PP3V0_S2R_HALL 61 69 72
VLDO2 C12 (100MA; 1.65-1.885V) PP1V7_VA_VCP 61 69 72
VLDO3 V18 (50MA; 2.5-3.3V) PP3V0_S2R_SENSOR 61 69 72
VLDO4 T19 (50MA; 2.5-3.3V) PP3V0_ALS 61 69 72
VLDO5 A13 (1000MA; 2.5-3.6V) PP3V1_S2R_MESA 61 69 72
VLDO6 A12 (150MA; 2.5-3.6V) PP3V3_ACC 61 69 72
VLDO7 A14 (300MA; 1.7-3.0V) PP3V0_S2R_TRISTAR 61 69 72
VLDO8 Y18 (300MA; 1.7-3.0V) PP3V0_MISC 61 69 72
VLDO9 A16 (300MA; 1.2-3.6V) PP1V25_CAM 61 69 72
VLDO10 A17 (150MA; 0.6-1.2V) PP1V0_SOC 61 69 72
VLDO11 B15 P 6 AF 61 69 72
VLDO13 Y17 P 61 69 72
VLDO14 A15 (100MA; 1.2-3.0V) PP1V8_SPARE 61 69 72
ON_BUF T13 (50MA; 1.8V; ON_BUFF) P 1 8 ALWAYS 61 69 72

VDD_LCM_SW C17 (NOTE: 2MHZ) 72
VDD_BOOST_LCM — 63 70
BOOST_LCM_LX A19 (VOLTAGE=6.0V) LCM_LX 63
LCM_FB D15 (VOLTAGE=6.0V) PP6V0_LCM_VBOOST 63 69
VDD_LCM
VLCM1 T16 (100MA; 5.0-6.0V) PP5V25_GRAPE 69 72
VLCM2 T18 (100MA; 5.0-6.0V) NO_TEST=TRUE NC_VLCM2
LCM2_EN D7
VLCM3 T17 (5MA; 5.0-6.0V) NO_TEST=TRUE NC_VLCM3

C8212 10UF 20% 25V X5R CERM 0603

XTAL
XTAL1 W19 PMU_XTAL
XTAL2 V19 PMU_EXTAL

CRITICAL Y8200 32.768K-20PPM-12.5PF 2012
CRITICAL C8215 18PF 5% 25V C0G-CERM 0201
CRITICAL C8216 18PF 5% 25V C0G-CERM 0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392		Y8200	RDAR://PROBLEM/9936684
138S0703	138S0648		C8235	AND ~15X MORE REFDES

LDO BYPASS

72 69 61 PP3V0_S2R_HALL
72 69 61 PP1V7_VA_VCP
72 69 61 PP3V0_S2R_SENSOR
72 69 61 PP3V0_ALS
72 69 61 PP3V1_S2R_MESA
72 69 61 PP3V3_ACC
72 69 61 PP3V0_S2R_TRISTAR

CRITICAL C8232 10UF 20% 0402-10
CRITICAL C8235 4.7UF 20% 6.3V X5R 402
CRITICAL C8233 20UF 20% 6.3V CERM 0402
CRITICAL C8234 4.7UF 20% 6.3V X5R 402
CRITICAL C82AB 2.2UF 10% 6.3V X5R 402
CRITICAL C8237 2.2UF 10% 6.3V X5R 402
CRITICAL C8231 10UF 20% 6.3V X5R 0402-10
CRITICAL C8230 2.2UF 10% 6.3V X5R 402

72 69 61 PP3V0_MISC
72 69 61 PP1V25_CAM
72 69 61 PP1V0_SOC
72 69 61 PP2V6_CAM_AF
72 69 61 PP2V9_CAM
72 69 61 PP1V8_SPARE
72 69 61 PP1V8_ALWAYS

CRITICAL C8242 0.22UF 20% 6.3V X5R 0201
CRITICAL C8270 4.7UF 20% 6.3V X5R 402
CRITICAL C8241 10UF 20% 6.3V X5R 0402-10
CRITICAL C8240 10UF 20% 6.3V X5R 0402-10
CRITICAL C8239 4.7UF 20% 6.3V X5R 402
C82A9 100PF 5% 16V C0G 0201
CRITICAL C8238 4.7UF 20% 6.3V X5R 402
CRITICAL C8271 10UF 20% 6.3V X5R 0402-10

SYNC_MASTER=N/A SYNC_DATE=N/A
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I2C ADDRESS: 0111100X (0X78)

U8100 OMIT_TABLE
D2207A0
BGA
SYM 3 OF 4

BUTTON1				GPIO_BTN_HOME_L	C9
BUTTON2				GPIO_BTN_ONOFF_L	C10
BUTTON3				NC_PMU_BTN3 (NO_TEST=TRUE)	E8
BUTTON4				NC_PMU_BTN4 (NO_TEST=TRUE)	E9
ACC_DET					R4
ADC_IN7	ANALOG INPUT	REFRENCES		PMU_USB_BRICKID_R	R16
ADC_IN31				ADC_IN7	N16
KEEPACT	DIGITAL INPUT	32K CLK	IREF	PMU_IREF	R14
SHDN			VREF	PMU_VREF	D9
RESET_IN1	WDOG		VDD_REF	PMU_VDD_REF	U12
RESET_IN2			VDD_REF_A		N6
RESET_IN3	RESET		VDD_RTC	PMU_VDD_RTC	P6
RESET*			OUT_32K	NC_PMU_OUT_32K (NO_TEST=TRUE)	R6
IRQ*			GPIO1	CLK_PMU2OSCAR_32K_AND_RESET_L	D10
SCL	I2C & DWI	GPIO	GPIO2	CLK_PMU2WLAN_32K	E4
SDA			GPIO3	GPIO_PMU2BT_REG_ON	E12
DWI_CK			GPIO4	GPIO_PMU2WLAN_REG_ON	E13
DWI_DI			GPIO5	GPIO_PMU2BBPMU_RESET_R_L	D11
DWI_DO			GPIO6	UART_BATT_HDQ	E11
TDEV1			GPIO7	GPIO_BT2PMU_HOST_WAKE	E10
TDEV2			GPIO8	GPIO_WLAN2PMU_HOST_WAKE	V4
TDEV3			GPIO9	GPIO_BB2PMU_HOST_WAKE_L	V10
TDEV4			GPIO10	GPIO_CODEC2PMU_HS_IRQ_L	T11
TDEV5			GPIO11	GPIO_HALL2PMU_IRQ0	T12
TDEV6			GPIO12		L5
TDEV7			GPIO13	GPIO_HALL2PMU_IRQ1	T6
TDEV8			GPIO14	PCIE_WLAN2PMU_WAKE_L	N4
TBAT	TEMPERATURE		GPIO15	GPIO_PMU2CODEC_RESET_L (USE INTERNAL PU)	P5
TCAL			GPIO16	GPIO_OSCAR2PMU_HOST_WAKE	T15
			GPIO17	GPIO_PMU2BB_VBUS_DET	T14
			GPIO18	GPIO_PMU2LCD_PWREN	
			GPIO19	NC_PMU_GPIO19 (NO_TEST=TRUE)	
			GPIO20	GPIO_DEVBRD2PMU_WAKE_L	
			GPIO21	NC_PMU_GPIO21 (NO_TEST=TRUE)	
			AMUX_A0	PPVDD_CPU_SOC_SENSE	
			AMUX_A1	PPVDD_GPU_SOC_SENSE	
			AMUX_A2	PPVDD_SRAM_SOC_SENSE	
			AMUX_A3	ADC_BB2PMU_IMEAS_RADIO	
			AMUX_AY	TP_AMUX_AY	
			AMUX_B0	NC_PMU_AMUX_B0 (NO_TEST=TRUE)	
			AMUX_B1	NC_PMU_AMUX_B1 (NO_TEST=TRUE)	
			AMUX_B2	PPVDD_SOC_SOC_SENSE	
			AMUX_B3	TP_CAMBUCK2PMU_IMEAS_OPOET	
			AMUX_BY		
			BUCK_LDO_UOV	TP_BUCK_LDO_UOV	
			BUCK_SLPD_MUX	TP_BUCK_SLPD_MUX	
			PRE_UVLO	SOCHOT0_L_R	
			SYS_ALIVE*	(SYS_ALIVE)	

R8399 0.00 1% 1/20W MF 0201
C8301 0.01UF 10% 6.3V X5R 01005
C8302 0.01UF 10% 6.3V X5R 01005
C8305 0.1UF 10% 6.3V CERM-X5R 0201
R8303 200K 0.5% 1/20W MF 0201
C8306 0.1UF 10% 6.3V CERM-X5R 0201
C8307 1UF 20% 10V X5R 402-1
C8308 1UF 20% 10V X5R 0201
R8330 1.00K 1% 1/32W MF 01005
C8340 100PF 5% 16V NP0-C0G 01005
R8340 3.92K 0.1% 1/20W MF 0201
RESISTOR FOR TEMP CALIBRATION

R8370 10K 5% 1/32W MF 01005
R8372 100K 5% 1/32W MF 01005
R8371 0.00 0% 1/32W MF 01005

=PP1V8_ALWAYS		
=PP1V8_SOC		
NOSTUFF		
SOCHOT0_L	OUT	
SYS_ALIVE	OUT	

R8328 10KOHM-1%-0.31MA 0201 (TEMP2 - NEAR SPEAKER AMPS)
R8321 10KOHM-1%-0.31MA 0201 (TEMP3 - NEAR WIFI)
R8322 10KOHM-1%-0.31MA 0201 (TEMP4 - NEAR REAR CAM)
R8323 10KOHM-1%-0.31MA 0201 (TEMP5 - NEAR NAND)
R8324 10KOHM-1%-0.31MA 0201 (TEMP6 - NEAR FRONT CAM)
R8325 10KOHM-1%-0.31MA 0201 (TEMP7 - NEAR PMU)
R8326 10KOHM-1%-0.31MA 0201 (TEMP8 - NEAR SOC)

C8328 100PF 5% 16V NP0-C0G 01005
C8321 100PF 5% 16V NP0-C0G 01005
C8322 100PF 5% 16V NP0-C0G 01005
C8323 100PF 5% 16V NP0-C0G 01005
C8324 100PF 5% 16V NP0-C0G 01005
C8325 100PF 5% 16V NP0-C0G 01005
C8326 100PF 5% 16V NP0-C0G 01005

BOARD_TEMP2_P / BOARD_TEMP2_N
BOARD_TEMP3_P / BOARD_TEMP3_N
BOARD_TEMP4_P / BOARD_TEMP4_N
BOARD_TEMP5_P / BOARD_TEMP5_N
BOARD_TEMP6_P / BOARD_TEMP6_N
BOARD_TEMP7_P / BOARD_TEMP7_N
BOARD_TEMP8_P / BOARD_TEMP8_N

XW8328 XW8321 XW8322 XW8323 XW8324 XW8325 XW8326 (SM)

PLACE XW AND CAP CLOSE TO PMU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0706	138S0739		C8308	
118S0764	118S0717		R8340	RDAR://PROBLEM/8380367
107S0150	107S0208		R8321-R8328	RDAR://PROBLEM/8380367

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE: PMU: ARABELA (3/3)
Apple Inc.
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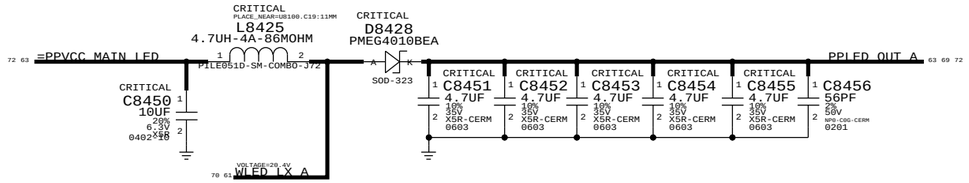
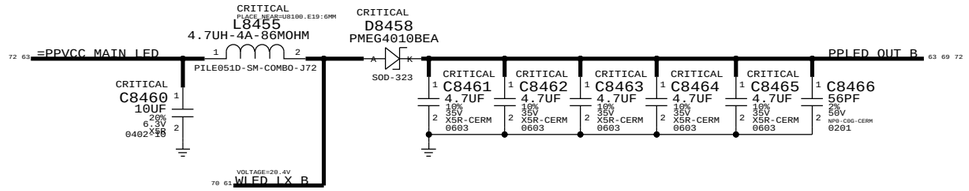
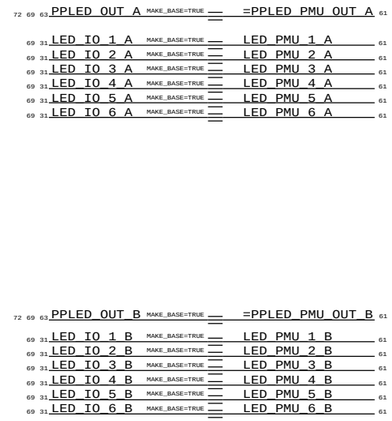
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1837	152S1789		L8425,L8455	RDAR://PROBLEM/13487208

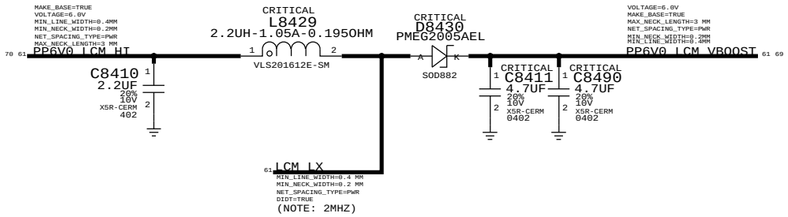
BACKLIGHT CIRCUIT MOVED HERE TO PERMIT SYNCING WITH DESIGNS USING BEACON







LCM BOOST MOVED HERE TO PERMIT SYNCING WITH DESIGNS USING KONA



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
POWER: J82 SPECIFIC

Apple Inc.

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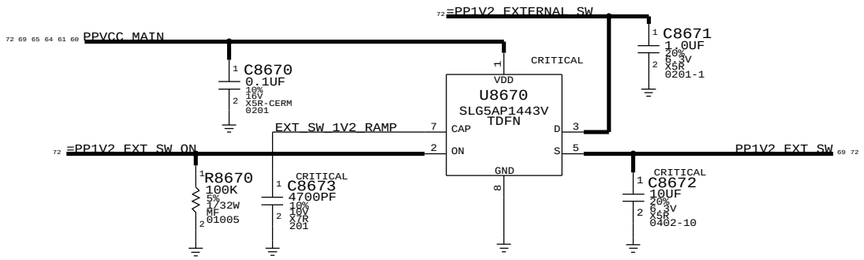
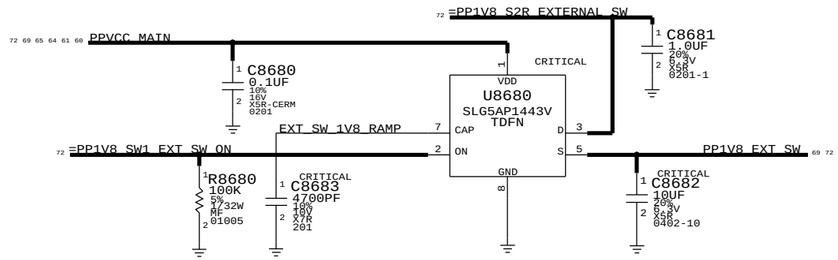
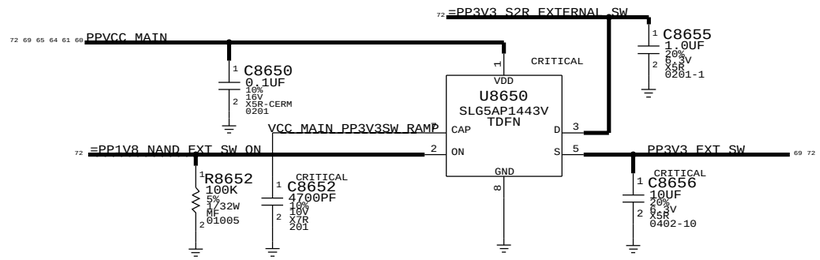




BUCK6 POWER IS ON IN HIBERNATE DUE TO WIFI PAS
SWITCH NEEDED TO GATE POWER TO NAND AND SOC



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
POWER: EXTERNAL SWITCHES

Apple Inc.

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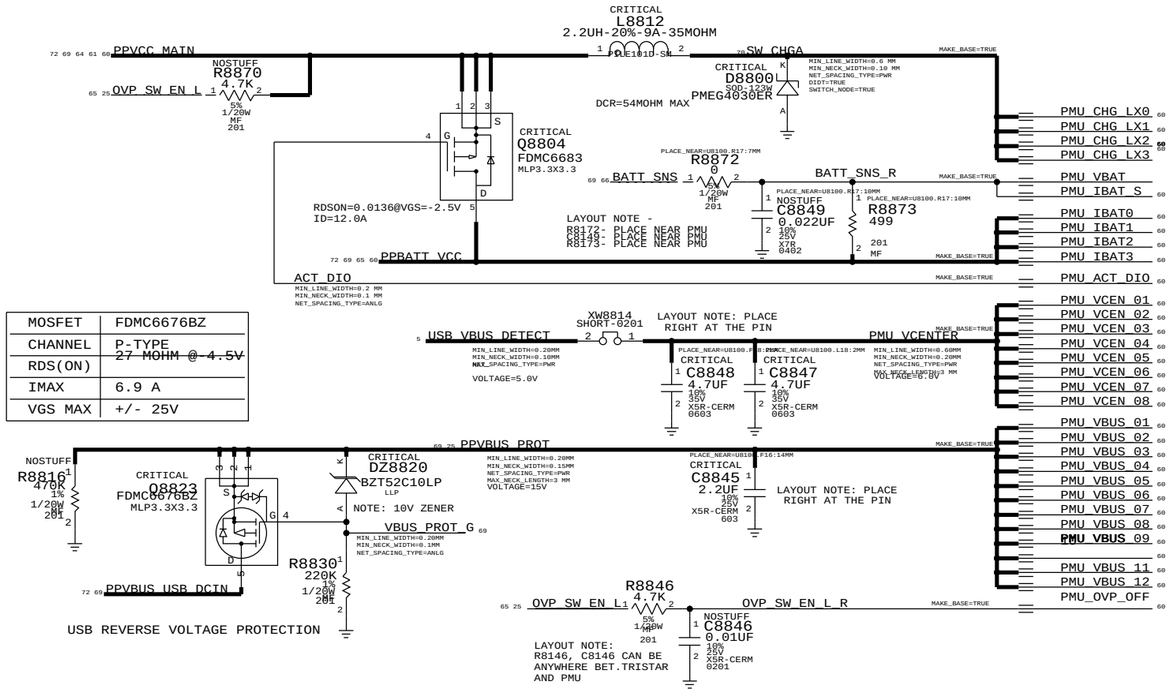
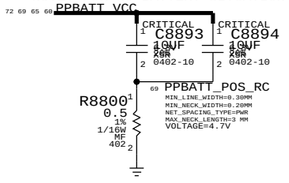
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1192	376S0929	?	Q8823	RDAR://PROBLEM/16073848



MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	~~27 MOHM @ 4.5V~~
IMAX	6.9 A
VGS MAX	+/- 25V

NOTE: FOR NO BATTERY SITUATION



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: PMU: CHARGER BUCK

Apple Inc.

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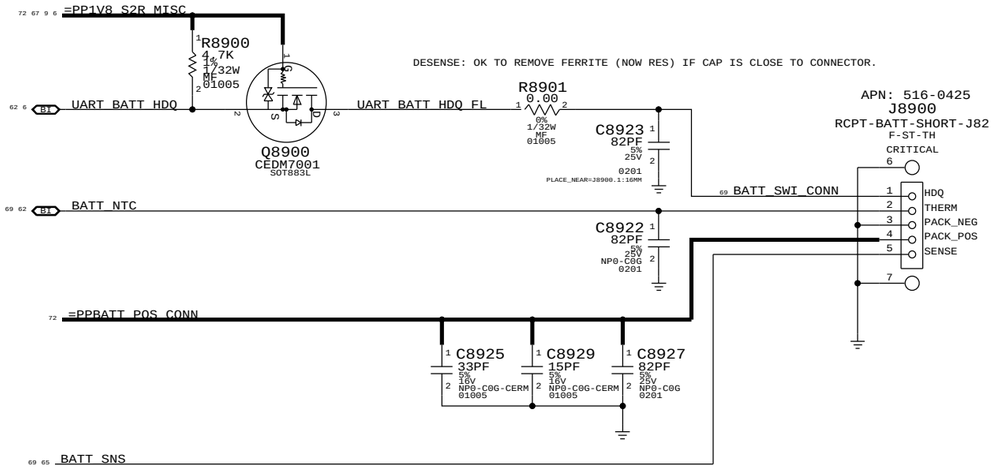

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0823		FL8900	RDAR://PROBLEM/11282371

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

POWER: BATTERY CONN

Apple Inc.

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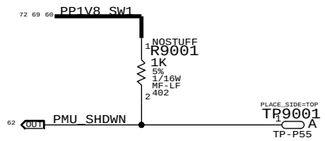
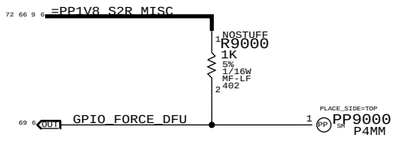
DEBUG RESET ACCESS





SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

SOC: DEBUG

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CELLULAR AND WLAN/BT ALIASES

BASEBAND

GPIO

71 69 6	IN	GPIO_SOC2BB_RADIO_ON_L	MAKE_BASE=TRUE	RADIO_ON_L	OUT 35 37
69 6	IN	GPIO_SOC2BB_RESET_L	MAKE_BASE=TRUE	BB_RST_L	OUT 35 37
69 6	OUT	GPIO_BB2SOC_RESET_DET_L	MAKE_BASE=TRUE	BB_RESET_DET_L	IN
70 69 62 71	IN	GPIO_PMU2BBPMU_RESET_L	MAKE_BASE=TRUE	RF_PMIC_RESET_L	OUT 35 37
71 6	IN	GPIO_SOC2BB_WAKE_MODEM	MAKE_BASE=TRUE	AP_WAKE_MODEM	OUT 40
70 69 62 25 10 5 4	OUT	RESET_SOC_L	MAKE_BASE=TRUE	RESET_1V8_L	IN 35
71 6	IN	GPIO_SOC2BB_COREDUMP	MAKE_BASE=TRUE	BB_CORE_DUMP	OUT 40
9	BI	GPIO_BB_IPC	MAKE_BASE=TRUE	BB_IPC_GPIO	BI 40
71 6	OUT	GPIO_BB2SOC_GPS_SYNC	MAKE_BASE=TRUE	BB_GPS_SYNC	IN 40
70 69 62	OUT	GPIO_BB2PMU_HOST_WAKE_L	MAKE_BASE=TRUE	BB_WAKE_HOST	IN 35 40

UART

71 25 6	OUT	UART_BB2SOC_TX	MAKE_BASE=TRUE	BB_UART_TXD	IN 35 40
71 25 6	IN	UART_SOC2BB_TX	MAKE_BASE=TRUE	BB_UART_RXD	OUT 35 40
71 6	OUT	UART_BB2SOC_RTS_L	MAKE_BASE=TRUE	BB_UART_RTS_L	IN 40
71 6	IN	UART_SOC2BB_RTS_L	MAKE_BASE=TRUE	BB_UART_CTS_L	OUT 40
71 17	IN	UART_OSCAR2BB_TX	MAKE_BASE=TRUE	BB_OTHER_RXD	OUT 40
71 17	OUT	UART_BB2OSCAR_TX	MAKE_BASE=TRUE	BB_OTHER_TXD	IN 40

HSIC

69 6	IN	HSIC_SOC2BB_HOST_RDY	MAKE_BASE=TRUE	BB_HOST_RDY	OUT 35 40
69 6	OUT	HSIC_BB2SOC_DEVICE_RDY	MAKE_BASE=TRUE	BB_DEVICE_RDY	IN 35 40
71 5	BI	HSIC_BB_DATA	MAKE_BASE=TRUE	50_BB_HSIC_DATA	BI 35 39
71 5	BI	HSIC_BB_STB	MAKE_BASE=TRUE	50_BB_HSIC_STROBE	BI 35 39

USB

71 69 62	IN	GPIO_PMU2BB_VBUS_DET	MAKE_BASE=TRUE	BB_USB_VBUS	OUT 35 39
71 25	BI	USB_BB_P	MAKE_BASE=TRUE	90_BB_USB_P	BI 35
71 25	BI	USB_BB_N	MAKE_BASE=TRUE	90_BB_USB_N	BI 35

SIM CARD

59	IN	SIMCRD_DETECT	MAKE_BASE=TRUE	BB_SIM_DETECT	OUT 39 40
59	OUT	SIMCRD_RST	MAKE_BASE=TRUE	BB_SIM_RESET	IN 40
59	OUT	SIMCRD_CLK	MAKE_BASE=TRUE	BB_SIM_CLK	IN 40
	BI	SIMCRD_IO	MAKE_BASE=TRUE	BB_SIM_DATA	BI 40

ADC

62	OUT	ADC_BB2PMU_IMEAS_RADIO	MAKE_BASE=TRUE	RADIO_TO_PMU_ADC_IMEAS_RADIO	IN 35
62	OUT	ADC_BB2PMU_IMEAS_QPOET	MAKE_BASE=TRUE	RADIO_TO_PMU_ADC_IMEAS_QPOET	IN 44

POWER

72		=PPBATT_VCC_BB		PP_BATT_VCC	35 44 53 73

LOWER ANT CTRL

59	OUT	GPIO_BB2ANT_SW0	MAKE_BASE=TRUE	BB_ANTSW_GPIO0	IN 40
59	OUT	GPIO_BB2ANT_SW1	MAKE_BASE=TRUE	BB_ANTSW_GPIO1	IN 40

SLOTS FOR RADIO FENCE

SL9110 TH-NSP 1 — SL-1.1X0.4-1.4X0.7 — SL9111 TH-NSP 1 — SL-1.1X0.4-1.4X0.7

NTC FOR BB

CRITICAL
R9127
10KOHM-1%-0.31MA
0201
PLACE_NEAR=U5401.A2:11MM
NO_XNET_CONNECTION=TRUE
(TEMP1 - NEAR BB)

C9127
100PF
5%
16V
NP0-C0G
01005
PLACE_NEAR=U8100.V4:11MM
NO_XNET_CONNECTION=TRUE

PA_NTC_P — 62 70
PA_NTC_N — XW9127 SM — PLACE_NEAR=U8100.V4:11MM

WLAN/BT

GPIO

70 69 68 62 57	IN	CLK_PMU2WLAN_32K	MAKE_BASE=TRUE	CLK_PMU2WLAN_32K	OUT 57 62 68 69 70
70 69 68 62 57	IN	GPIO_PMU2BT_REG_ON	MAKE_BASE=TRUE	GPIO_PMU2BT_REG_ON	OUT 57 62 68 69 70
70 69 68 62 57	IN	GPIO_PMU2WLAN_REG_ON	MAKE_BASE=TRUE	GPIO_PMU2WLAN_REG_ON	OUT 57 62 68 69 70
70 68 57 9	IN	GPIO_SOC2BT_WAKE	MAKE_BASE=TRUE	GPIO_SOC2BT_WAKE	OUT 9 57 68 70
70 9	IN	GPIO_SOC2WLAN_WAKE	MAKE_BASE=TRUE	GPIO_SOC2WLAN_PCIE_DEV_WAKE	OUT 57
70 68 62 57	OUT	GPIO_BT2PMU_HOST_WAKE	MAKE_BASE=TRUE	GPIO_BT2PMU_HOST_WAKE	IN 57 62 68 70
70 68 62 57	OUT	GPIO_WLAN2PMU_HOST_WAKE	MAKE_BASE=TRUE	GPIO_WLAN2PMU_HOST_WAKE	IN 57 62 68 70

PCIE

70 9	IN	PCIE_SOC2WLAN_RESET_L	MAKE_BASE=TRUE	PCIE_SOC2WLAN_PERST	OUT 57
70 9	OUT	PCIE_WLAN2SOC_CLKREQ_L	MAKE_BASE=TRUE	PCIE_WLAN2SOC_CLKREQ	IN 57
68 62 57	OUT	PCIE_WLAN2PMU_WAKE_L	MAKE_BASE=TRUE	PCIE_WLAN2PMU_WAKE_L	IN 57 62 68
70 68 57 9	IN	PCIE_SOC2WLAN_CLK_P	MAKE_BASE=TRUE	PCIE_SOC2WLAN_CLK_P	OUT 9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_CLK_N	MAKE_BASE=TRUE	PCIE_SOC2WLAN_CLK_N	OUT 9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_TX_P	MAKE_BASE=TRUE	PCIE_SOC2WLAN_TX_P	OUT 9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_TX_N	MAKE_BASE=TRUE	PCIE_SOC2WLAN_TX_N	OUT 9 57 68 70
70 9	OUT	PCIE_WLAN2SOC_TX_P	MAKE_BASE=TRUE	PCIE_WLAN2SOC_RX_P	IN 57
70 9	OUT	PCIE_WLAN2SOC_TX_N	MAKE_BASE=TRUE	PCIE_WLAN2SOC_RX_N	IN 57
TO KEEP PP NAMING CONSISTENT	70	PCIE_WLAN2SOC_TX_C_P	MAKE_BASE=TRUE	PCIE_TX_P	57
	70	PCIE_WLAN2SOC_TX_C_N	MAKE_BASE=TRUE	PCIE_TX_N	57

UART

70 68 57 6	IN	UART_SOC2BT_TX	MAKE_BASE=TRUE	UART_SOC2BT_TX	OUT 6 57 68 70
70 68 57 6	IN	UART_SOC2BT_RTS_L	MAKE_BASE=TRUE	UART_SOC2BT_RTS_L	OUT 6 57 68 70
70 6	OUT	UART_BT2SOC_TX	MAKE_BASE=TRUE	UART_BT2SOC_RX	IN 57
70 6	OUT	UART_BT2SOC_RTS_L	MAKE_BASE=TRUE	UART_BT2SOC_CTS_L	IN 57
70 68 57 6	IN	UART_SOC2WLAN_TX	MAKE_BASE=TRUE	UART_SOC2WLAN_TX	OUT 6 57 68 70
70 68 57 6	IN	UART_SOC2WLAN_RTS_L	MAKE_BASE=TRUE	UART_SOC2WLAN_RTS_L	OUT 6 57 68 70
70 6	OUT	UART_WLAN2SOC_TX	MAKE_BASE=TRUE	UART_WLAN2SOC_RX	IN 57
70 6	OUT	UART_WLAN2SOC_RTS_L	MAKE_BASE=TRUE	UART_WLAN2SOC_CTS_L	IN 57
RESOLVES CKPLUS ERROR IN NAME		TP_WL_UART_RX	MAKE_BASE=TRUE	WL_UART_RX	57
		TP_WL_UART_TX	MAKE_BASE=TRUE	WL_UART_TX	57

I2S

70 6	OUT	I2S_BT2SOC_DOUT	MAKE_BASE=TRUE	I2S_BT2SOC_DIN	IN 57
70 68 57 6	IN	I2S_SOC2BT_DOUT	MAKE_BASE=TRUE	I2S_SOC2BT_DOUT	OUT 6 57 68 70
70 68 57 6	IN	I2S_SOC2BT_BCLK	MAKE_BASE=TRUE	I2S_SOC2BT_BCLK	OUT 6 57 68 70
70 68 57 6	IN	I2S_SOC2BT_LRCK	MAKE_BASE=TRUE	I2S_SOC2BT_LRCK	OUT 6 57 68 70

OSCAR CONTEXT

17	IN	GPIO_OSCAR2WLAN_CONTEXT_A	MAKE_BASE=TRUE	OSCAR2RADIO_CONTEXT_A	OUT 57 70
17	IN	GPIO_OSCAR2WLAN_CONTEXT_B	MAKE_BASE=TRUE	OSCAR2RADIO_CONTEXT_B	OUT 57 70

JTAG

70	OUT	TP_JTAG_WLAN_TMS	MAKE_BASE=TRUE	JTAG_WLAN_TMS	IN 57
70	OUT	TP_JTAG_WLAN_TRST	MAKE_BASE=TRUE	JTAG_WLAN_TRST	IN 57

POWER

72		=PPVCC_MAIN_WLAN		PP_VCC_MAIN_WLAN	57
72		=PP3V3_S2R_WIFI_PA		PP_3V3_S2R_WIFI_PA	56 57
72		=PP1V8_S2R_VDDIO_WLAN_BT		PP_1V8_S2R_VDDIO_WLAN_BT	57 73

NO CONNECT

		NC_WLAN_GPIO3	NO_TEST=TRUE MAKE_BASE=TRUE	BT_EXT_SYNC	OUT 57
		NC_WLAN_GPIO5	NO_TEST=TRUE MAKE_BASE=TRUE	BT_EXT_CLK	OUT 57

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: ALIASES: BB/WLAN/BT

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SMT TEST FIXTURE TP

POWER - BUCKS

MUST HAVE

PPVDD_CPU	FUNC_TEST=TRUE	60 72
PPVDD_GPU	FUNC_TEST=TRUE	60 72
PP0V95_SOC	FUNC_TEST=TRUE	60 72
PP1V8_S2R	FUNC_TEST=TRUE	60 61 72
PP1V8_SW1	FUNC_TEST=TRUE	60 67 72
PP1V8_SW1_FOREHEAD	FUNC_TEST=TRUE	72
PP1V8_EXT_SW	FUNC_TEST=TRUE	64 72
PP1V8_SW2	FUNC_TEST=TRUE	60 72
PP1V8_GRAPE_EXT_SW	FUNC_TEST=TRUE	30 72
PP1V8_S2R_SW3	FUNC_TEST=TRUE	60 72
PP1V2_S2R	FUNC_TEST=TRUE	60 61 72
PP1V2_SW1	FUNC_TEST=TRUE	60 72
PP1V2_EXT_SW	FUNC_TEST=TRUE	64 72
PP1V2_S2R_SW2	FUNC_TEST=TRUE	60 72
PPVDD_SRAM	FUNC_TEST=TRUE	60 72
PP3V3_S2R	FUNC_TEST=TRUE	60 72
PP3V3_EXT_SW	FUNC_TEST=TRUE	64 72

POWER - LDOS

PP1V7_VA_VCP	FUNC_TEST=TRUE	61 72
PP3V0_S2R_SENSOR	FUNC_TEST=TRUE	61 72
PP3V0_ALS	FUNC_TEST=TRUE	61 72
PP3V3_ACC	FUNC_TEST=TRUE	61 72
PP3V0_S2R_TRISTAR	FUNC_TEST=TRUE	61 72
PP3V1_S2R_MESA	FUNC_TEST=TRUE	61 72
PP1V0_SOC	FUNC_TEST=TRUE	61 72
PP1V8_SPARE	FUNC_TEST=TRUE	61 72
PP3V0_S2R_HALL	FUNC_TEST=TRUE	61 72
PP3V0_MISC	FUNC_TEST=TRUE	61 72
PP1V25_CAM	FUNC_TEST=TRUE	61 72
PP2V6_CAM_AF	FUNC_TEST=TRUE	61 72
PP2V9_CAM	FUNC_TEST=TRUE	61 72

POWER - OTHER

MUST HAVE

PP1V8_ALWAYS	FUNC_TEST=TRUE	61 72
PPBATT_VCC	FUNC_TEST=TRUE	60 65 69 72
PPLED_OUT_A	FUNC_TEST=TRUE	63 72
PPLED_OUT_B	FUNC_TEST=TRUE	63 72
PP5V25_GRAPE	FUNC_TEST=TRUE	61 72
PP1V8_XTAL	FUNC_TEST=TRUE	11
PPVCC_MAIN	FUNC_TEST=TRUE	60 61 64 65 72
PPBATT_POS_RC	FUNC_TEST=TRUE	65
PP6V0_LCM_VBOOST	FUNC_TEST=TRUE	61 63
PPVBUS_USB_DCIN	FUNC_TEST=TRUE	65 72
PPVBUS_PROT	FUNC_TEST=TRUE	25 65
VBUS_PROT_G	FUNC_TEST=TRUE	65

POWER - CAMERA (FRONT)

MUST HAVE

PP1V2_CAM_FRONT_FILT	FUNC_TEST=TRUE	20 21
PP1V8_CAM_FRONT_FILT	FUNC_TEST=TRUE	20 21
PP2V9_AVDD_CAM_FRONT_FILT	FUNC_TEST=TRUE	20 21

POWER - CAMERA (REAR)

MUST HAVE

PP1V25_CAM_REAR_FILT	FUNC_TEST=TRUE	20 21
PP1V8_CAM_REAR_FILT	FUNC_TEST=TRUE	20 21
PP2V6_CAM_REAR_AF_FILT	FUNC_TEST=TRUE	20 21
PP2V9_AVDD_CAM_REAR_FILT	FUNC_TEST=TRUE	20 21

POWER - AUDIO

PP1V8_DMIC_MIC_FILT	FUNC_TEST=TRUE	23
PP1V8_DMIC_BTN_FILT	FUNC_TEST=TRUE	28
PP1V7_VCP	FUNC_TEST=TRUE	22
PPVBOOST_R	FUNC_TEST=TRUE	24
PPVBOOST_L	FUNC_TEST=TRUE	24

POWER - SENSORS

PP1V8_COMPASS	FUNC_TEST=TRUE	18
PP1V8_PHOS_FILT	FUNC_TEST=TRUE	18
PP1V8_OSCAR_FILT	FUNC_TEST=TRUE	17
PP1V2_OSCAR_FILT	FUNC_TEST=TRUE	17
PP3V0_GYRO_FILT	FUNC_TEST=TRUE	18
PP3V0_SENSOR_PROX_FILT	FUNC_TEST=TRUE	58

POWER - DISPLAY

MUST HAVE

PPVCC_MAIN_LCD_SW_CONN	FUNC_TEST=TRUE	31 32
PPVCC_MAIN_LCD_SW	FUNC_TEST=TRUE	32

POWER - MESA

MUST HAVE

PP1V825_S2R_MESA_FILT	FUNC_TEST=TRUE	31 33
PP3V1_S2R_MESA_FILT	FUNC_TEST=TRUE	31 33
PP11V3_MESA_FILT	FUNC_TEST=TRUE	33

POWER - GRAPE

PPVDD_STINGER_BOOST	FUNC_TEST=TRUE	29

POWER - BACKLIGHT

MUST HAVE

PPLED_BACK_REG_A	FUNC_TEST=TRUE	31 32
LED_IO_1_A	FUNC_TEST=TRUE	31 63
LED_IO_2_A	FUNC_TEST=TRUE	31 63
LED_IO_3_A	FUNC_TEST=TRUE	31 63
LED_IO_4_A	FUNC_TEST=TRUE	31 63
LED_IO_5_A	FUNC_TEST=TRUE	31 63
LED_IO_6_A	FUNC_TEST=TRUE	31 63
PPLED_BACK_REG_B	FUNC_TEST=TRUE	31 32
LED_IO_1_B	FUNC_TEST=TRUE	31 63
LED_IO_2_B	FUNC_TEST=TRUE	31 63
LED_IO_3_B	FUNC_TEST=TRUE	31 63
LED_IO_4_B	FUNC_TEST=TRUE	31 63
LED_IO_5_B	FUNC_TEST=TRUE	31 63
LED_IO_6_B	FUNC_TEST=TRUE	31 63

SOC - JTAG/RESET

MUST HAVE

JTAG_SOC_SEL	FUNC_TEST=TRUE	4 5
JTAG_SOC_TCK	FUNC_TEST=TRUE	5 25
JTAG_SOC_TDI	FUNC_TEST=TRUE	5
JTAG_SOC_TMS	FUNC_TEST=TRUE	5 25
TP_JTAG_SOC_TRST_L	FUNC_TEST=TRUE	4 5
TP_JTAG_SOC_TDO	FUNC_TEST=TRUE	5
SOC_TESTMODE	FUNC_TEST=TRUE	4 5
RESET_SOC_L	FUNC_TEST=TRUE	4 5 10 25 62 68 70
GPIO_FORCE_DFU	FUNC_TEST=TRUE	6 67

SOC - UART

UART_SOC2DEBUG_TX	FUNC_TEST=TRUE	6 25
UART_DEBUG2SOC_TX	FUNC_TEST=TRUE	6 25

SOC - USB

USB_SOC_N	FUNC_TEST=TRUE	5 25
USB_SOC_P	FUNC_TEST=TRUE	5 25

E75_ACC_DET_CONN_L	FUNC_TEST=TRUE	25 27
PPVBUS_E75_USB_CONN	FUNC_TEST=TRUE	26 27 69
PPOUT_E75_ACC_ID1_CONN	FUNC_TEST=TRUE	26 27
PPOUT_E75_ACC_ID2_CONN	FUNC_TEST=TRUE	26 27
E75_DPAIR1_CONN_N	FUNC_TEST=TRUE	25 27
E75_DPAIR1_CONN_P	FUNC_TEST=TRUE	25 27
E75_DPAIR2_CONN_N	FUNC_TEST=TRUE	25 27
E75_DPAIR2_CONN_P	FUNC_TEST=TRUE	25 27

AUDIO - HEADPHONE

MUST HAVE

CONN_HP_HEADSET_DET_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS3_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS3_REF_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS4_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS4_REF_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_LEFT_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_RIGHT_FILT	FUNC_TEST=TRUE	22 23
GPIO_SOC2AJ_HS3_SHUNT_EN_FILT	FUNC_TEST=TRUE	23
GPIO_SOC2AJ_HS4_SHUNT_EN_FILT	FUNC_TEST=TRUE	23

AUDIO - SPEAKER AMPS

SPKRAMP_L_OUT_N	FUNC_TEST=TRUE	24 27 70
SPKRAMP_L_OUT_P	FUNC_TEST=TRUE	24 27 70
SPKRAMP_R_OUT_N	FUNC_TEST=TRUE	24 27 70
SPKRAMP_R_OUT_P	FUNC_TEST=TRUE	24 27 70

AUDIO - CODEC

AIN3P	FUNC_TEST=TRUE	22
AIN3N	FUNC_TEST=TRUE	22
GPIO_CODEC2PMU_HS_IRQ_L	FUNC_TEST=TRUE	22 62 70
GND_AUDIO_CODEC	FUNC_TEST=TRUE	22
MIKEY_TS_P	FUNC_TEST=TRUE	22 25
MIKEY_TS_N	FUNC_TEST=TRUE	22 25

AUDIO - DIGITAL MICS

DMIC_MIC_SCLK	FUNC_TEST=TRUE	22 23
DMIC_BTN_SCLK	FUNC_TEST=TRUE	22 28

BUTTONS

GPIO_BTN_HOME_CONN_L	FUNC_TEST=TRUE	31 33
GPIO_BTN_ONOFF_L	FUNC_TEST=TRUE	5 6 23 62
GPIO_BTN_VOL_UP_L_FILT	FUNC_TEST=TRUE	28
GPIO_BTN_VOL_DOWN_L_FILT	FUNC_TEST=TRUE	28

NAND

ANC0_CE0_L	FUNC_TEST=TRUE	7 16 70
ANC1_CE0_L	FUNC_TEST=TRUE	7 16 70

BATTERY

MUST HAVE

BATT_SWI_CONN	FUNC_TEST=TRUE	66
BATT_NTC	FUNC_TEST=TRUE	62 66
BATT_SNS	FUNC_TEST=TRUE	65 66

GRAPE

CLK_SOC2GRAPE_32K	FUNC_TEST=TRUE	9 30 70

BASEBAND

MUST HAVE

BOUNDARY_SCAN_EN	FUNC_TEST=TRUE	35 39
GPIO_PMU2BBPMU_RESET_L	FUNC_TEST=TRUE	62 68 70 71
GPIO_SOC2BB_RADIO_ON_L	FUNC_TEST=TRUE	6 68 71
HSIC_SOC2BB_HOST_RDY	FUNC_TEST=TRUE	6 68
GPIO_BB2SOC_RESET_DET_L	FUNC_TEST=TRUE	6 68
HSIC_BB2SOC_DEVICE_RDY	FUNC_TEST=TRUE	6 68
GPIO_SOC2BB_RESET_L	FUNC_TEST=TRUE	6 68
GPIO_PMU2BB_VBUS_DET	FUNC_TEST=TRUE	62 68 71
GPIO_BB2PMU_HOST_WAKE_L	FUNC_TEST=TRUE	62 68 70

BASEBAND - POWER

PP_LDO6	FUNC_TEST=TRUE	35 36 71 73
PP_LDO13	FUNC_TEST=TRUE	36 38 55 73
VREG_SMPS1_0V90	FUNC_TEST=TRUE	36 38
VREG_SMPS3_0V95	FUNC_TEST=TRUE	36 73

BASEBAND - SIM CARD

MUST HAVE

PP_LDO5_FILT	FUNC_TEST=TRUE	59
SIMCRD_RST_CONN_FILT	FUNC_TEST=TRUE	59 71
SIMCRD_CLK_CONN_FILT	FUNC_TEST=TRUE	59 71
SIMCRD_IO_CONN_FILT	FUNC_TEST=TRUE	59 71
SIMCRD_DETECT_FILT	FUNC_TEST=TRUE	59 71

WIFI/BT

MUST HAVE

GPIO_PMU2BT_REG_ON	FUNC_TEST=TRUE	57 62 68 70
GPIO_PMU2WLAN_REG_ON	FUNC_TEST=TRUE	57 62 68 70
CLK_PMU2WLAN_32K	FUNC_TEST=TRUE	57 62 68 70

CAMERA - REAR

ISP_CAM_REAR_CLK_F	FUNC_TEST=TRUE	20 21
ISP_CAM_REAR_SCL_F	FUNC_TEST=TRUE	20 21
ISP_CAM_REAR_SDA_F	FUNC_TEST=TRUE	20 21
ISP_CAM_REAR_SHUTDOWN_L_F	FUNC_TEST=TRUE	20 21

CAMERA - FRONT

ISP_CAM_FRONT_CLK_F	FUNC_TEST=TRUE	20 21
ISP_CAM_FRONT_SCL_F	FUNC_TEST=TRUE	20 21
ISP_CAM_FRONT_SDA_F	FUNC_TEST=TRUE	20 21
ISP_CAM_FRONT_SHUTDOWN_L_F	FUNC_TEST=TRUE	20 21

MESA

MUST HAVE

GPIO_MESA2SOC_IRQ_FILT	FUNC_TEST=TRUE	31 33
MESA_BOOST_ENABLE_FILT	FUNC_TEST=TRUE	31 33
SPI_MESA_MISO_FILT	FUNC_TEST=TRUE	31 33
SPI_MESA_MOSI_FILT	FUNC_TEST=TRUE	31 33
SPI_MESA_SCLK_FILT	FUNC_TEST=TRUE	31 33

HALL EFFECT

GPIO_HALL2PMU_IRQ0	FUNC_TEST=TRUE	19 62
GPIO_HALL2PMU_IRQ1_FILT	FUNC_TEST=TRUE	29 30
PP3V0_S2R_GRAPE_HALL_FILT	FUNC_TEST=TRUE	29 30

ALS

MUST HAVE

PP3V0_MIC_ALS_FILT	FUNC_TEST=TRUE	23
PP3V0_HP_ALS_FILT	FUNC_TEST=TRUE	23
GPIO_HP_ALS2SOC_IRQ_L_FILT	FUNC_TEST=TRUE	23
GPIO_MIC_ALS2SOC_IRQ_L_F	FUNC_TEST=TRUE	23
I2C_HP_ALS_SCL_1V8_FILT	FUNC_TEST=TRUE	23 70
I2C_HP_ALS_SDA_1V8_FILT	FUNC_TEST=TRUE	23 70
I2C_MIC_ALS_SCL_1V8_F	FUNC_TEST=TRUE	23 70
I2C_MIC_ALS_SDA_1V8_F	FUNC_TEST=TRUE	23 70

DISPLAY

MUST HAVE

EDP_HPD_EMI	FUNC_TEST=TRUE	32

OSCAR

MUST HAVE

CLK_PMU2OSCAR_32K_AND_RESET_L	FUNC_TEST=TRUE	17 62 70

SOCHOT0_L	FUNC_TEST=TRUE	6 62

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

SL9300 APN: 998-2691 TH-NSP
SL9301 TH-NSP SL-1.1X0.4-1.4X0.7
SL9302 TH-NSP SL-1.1X0.4-1.4X0.7
SL-1.1X0.4-1.4X0.7
SL9320 TH-NSP
SL-1.1X0.4-1.4X0.7 SL9321 TH-NSP
SL-1.1X0.4-1.4X0.7

FOREHEAD B2B STANDOFFS

STD9300 APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM

C9301 0.01UF 10% 6.3V X5R 01005
STD9301 APN: 860-8373 STDOFF-3.3X1.8R1.05H-SM
STD9301_AC_R
09/17/13 AC CAP RDAR://PROBLEM//14999426
STD9303 APN: 860-00013 STDOFF-3.3X1.8R0.84H-TH

BUTTON FLEX B2B STANDOFFS

STD9302 APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM

GRAPE AND DISPLAY B2B STANDOFFS

STD9305 APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM
STD9306
STDOFF-3.3X1.8R1.05H-SM
STD9307
STDOFF-3.3X1.8R1.05H-SM

FID9300 FID 0P5SM1P0SQ-NSP
FID9301 FID 0P5SM1P0SQ-NSP
FID9302 FID 0P5SM1P0SQ-NSP
FID9303 FID 0P5SM1P0SQ-NSP
FID9304 FID 0P5SM1P0SQ-NSP
FID9305 FID 0P5SM1P0SQ-NSP

TP9310A TP9311A TP9312A TP9315A TP9316A TP9317A
TP-1P0-TOP PLACE_NEAR=J3700.9:20MM / PLACE_NEAR=J3700.9:30MM
PPVBUS_E75_USB_CONN 26 27 69

TP9300A TP9301A TP9302A TP9305A TP9306A TP9307A
TP-1P0-TOP PLACE_NEAR=J8900.4:20MM / PLACE_NEAR=J8900.3:20MM
PPBATT_VCC 60 65 69 72

DEV BOARD NET TERMINATION

NC_SOC_GPIO09	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_ALS2SOC_DEVBRD_IRQ_L	6
NC_PMU_GPIO20	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_DEVBRD2PMU_WAKE_L	62
NC_ULPI_STP	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_SOC2DEVBRD_S3E_WAKE	9
NC_ULPI_DATA3	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_SOC2DEVBRD_S3E_RESET2_L	9
NC_PCIE_CLKREQ2	NO_TEST=TRUE MAKE_BASE=TRUE	PCIE_DEVBRD2SOC_CLKREQ_L	9
NC_PCIE_PERST2	NO_TEST=TRUE MAKE_BASE=TRUE	PCIE_SOC2DEVBRD_RESET_L	9
NC_NAND_SYS_CLK	NO_TEST=TRUE MAKE_BASE=TRUE	CLK_SOC2DEVBRD_PCIE_24MHZ	9
NC_I2S4_MCK	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_DISPLAY_ID0	6
NC_I2S1_MCK	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_DISPLAY_ID1	6

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE
TEST: TPS/HOLES/FIDUCUALS

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EE CHARACTERIZATION TP

SOC

PP9501 P4MM SM (PP) 1 RESET_SOC_L — PLACE_SIDE=TOP — 4 5 10 25 62 68 69
PP9503 P4MM SM (PP) 1 SOCHOT0_L_R — 62
FUNC_TEST=TRUE — 6
PP9502 P4MM SM (PP) 1 TP_ANALOGMUXOUT — 5
PP9507 P4MM SM (PP) 1 PPVDD_CPU_SOC_SENSE — PLACE_NEAR=U0600.AB13:1.5MM — 13 62
PP9508 P4MM SM (PP) 1 PPVDD_GPU_SOC_SENSE — PLACE_NEAR=U0600.N26:1.5MM — 13 62
PP9509 P4MM SM (PP) 1 PPVDD_SRAM_SOC_SENSE — PLACE_NEAR=U0600.N25:1.5MM — 13 62
PP9513 P4MM SM (PP) 1 PPVDD_SOC_SOC_SENSE — PLACE_NEAR=U0600.M25:1.5MM — 12 62
PP9509 P4MM SM (PP) 1 TP_SOC_VSS_SENSE — PLACE_NEAR=U0600.M26:1MM — 12
PP9510 P4MM SM (PP) 1 TP_SOC_VSS_CPU_SENSE — PLACE_NEAR=U0600.AC13:1MM — 12

NAND

ANC0_AD<1..7> — FUNC_TEST=TRUE — 7 16
ANC0_CE0_L — FUNC_TEST=TRUE — 7 16 69
ANC0_ALE — FUNC_TEST=TRUE — 7 16
ANC0_CLE — FUNC_TEST=TRUE — 7 16
ANC0_WE_L — FUNC_TEST=TRUE — 7 16
ANC0_RE_L — FUNC_TEST=TRUE — 7 16
ANC1_AD<0> — FUNC_TEST=TRUE — 7 16
ANC1_CE0_L — FUNC_TEST=TRUE — 7 16 69
ANC1_ALE — FUNC_TEST=TRUE — 7 16
ANC1_CLE — FUNC_TEST=TRUE — 7 16
ANC1_WE_L — FUNC_TEST=TRUE — 7 16
ANC1_RE_L — FUNC_TEST=TRUE — 7 16
ANC1_DQS — FUNC_TEST=TRUE — 7 16
PPVREF_ANC_SOC — FUNC_TEST=TRUE — 7
PPVREF_ANC_NAND — FUNC_TEST=TRUE — 16
NAND_SLOT0_RDYBSY_L — FUNC_TEST=TRUE — 16

PP9505 P4MM SM (PP) 1 ANC0_AD<0> — PLACE_SIDE=BOTTOM — 7 16
PP9506 P4MM SM (PP) 1 ANC0_DQS — NO_XNET_CONNECTION=TRUE — PLACE_SIDE=BOTTOM — PLACE_NEAR=U0600.C36:2MM — 7 16
PP9500 P4MM SM (PP) 1 GND — (PLACE_SIDE=TOP)
PP9504 P4MM SM (PP) 1 =PP1V8_NAND — (PLACE_SIDE=TOP) — 16 72
PP95G0 P4MM SM (PP) 1 TP_ANC_TCKC_NAND — (PLACE_SIDE=TOP) — 16
PP95G4 P4MM SM (PP) 1 TP_ANC_TMSC_NAND — (PLACE_SIDE=TOP) — 16

PMU

GPIO_PMU2BBPMU_RESET_L — FUNC_TEST=TRUE — 62 68 69 71
GPIO_BT2PMU_HOST_WAKE — FUNC_TEST=TRUE — 57 62 68 70
GPIO_BB2PMU_HOST_WAKE_L — FUNC_TEST=TRUE — 62 68 69
GPIO_CODEC2PMU_HS_IRQ_L — FUNC_TEST=TRUE — 22 62 69
PMU_TCAL — FUNC_TEST=TRUE — 62
CLK_PMU2WLAN_32K — FUNC_TEST=TRUE — 57 62 68 69 70
CLK_PMU2OSCAR_32K_AND_RESET — FUNC_TEST=TRUE — 17 62 69
PA_NTC_P — FUNC_TEST=TRUE — 62 68
BOARD_TEMP2_P — FUNC_TEST=TRUE — 62
BOARD_TEMP3_P — FUNC_TEST=TRUE — 62
BOARD_TEMP4_P — FUNC_TEST=TRUE — 62
BOARD_TEMP5_P — FUNC_TEST=TRUE — 62
BOARD_TEMP6_P — FUNC_TEST=TRUE — 62
BOARD_TEMP7_P — FUNC_TEST=TRUE — 62
BOARD_TEMP8_P — FUNC_TEST=TRUE — 62
TP_BUCK_LDO_VOV — FUNC_TEST=TRUE — 62
TP_BUCK_SLPD_MUX — FUNC_TEST=TRUE — 62
TP_AMUX_AY — FUNC_TEST=TRUE — 62
TP_AMUX_BY — FUNC_TEST=TRUE — 62

PP9511 P4MM SM (PP) 1 DWI_SOC2PMU_CLK — NO_TEST=TRUE — 6 62
PP9512 P4MM SM (PP) 1 DWI_SOC2PMU_DO — NO_TEST=TRUE — 6 62
PP95F1 P4MM SM (PP) 1 SYS_ALIVE — 62

GRAPE

I2C_GRAPE_SDA_1V8 (CUMULUS TDO) — FUNC_TEST=TRUE — 29 30
TP_JTAG_CUMULUS_M_TCK — FUNC_TEST=TRUE — 30
TP_JTAG_CUMULUS_M_TDI — FUNC_TEST=TRUE — 30
JTAG_CUMULUS_M_TMS — FUNC_TEST=TRUE — 30
SPI_GRAPE_SCLK — FUNC_TEST=TRUE — 6 30
SPI_GRAPE_MISO — FUNC_TEST=TRUE — 6 30
SPI_GRAPE_MOSI — FUNC_TEST=TRUE — 6 30
SPI_GRAPE_CS_L — FUNC_TEST=TRUE — 6 30
GPIO_SOC2GRAPE_RESET_L — FUNC_TEST=TRUE — 6 30
GPIO_GRAPE2SOC_IRQ_L — FUNC_TEST=TRUE — 6 30
DISPLAY_SYNC — FUNC_TEST=TRUE — 6 30
CLK_SOC2GRAPE_32K — FUNC_TEST=TRUE — 9 30 69
CUMULUS_M2S_CLK — FUNC_TEST=TRUE — 30
CUMULUS_M2S_SDA — FUNC_TEST=TRUE — 30
I2C_GRAPE_SDA_1V8 — FUNC_TEST=TRUE — 29 30 70
I2C_GRAPE_SCL_1V8 — FUNC_TEST=TRUE — 29 30

PP9514 P4MM SM (PP) 1 TP_CUMULUS_S_CS_L — 30
PP9515 P4MM SM (PP) 1 TP_CUMULUS_S_GPIO_3 — 30

AUDIO

DMIC_MIC_SD — FUNC_TEST=TRUE — 22 23
DMIC_BTN_SD — FUNC_TEST=TRUE — 22 28
GPIO_CODEC2SOC_IRQ_L — FUNC_TEST=TRUE — 6 22

TP9500 A (1) TP-P5
TP9501 A (1) TP-P5 — SPKRAMP_R_OUT_P — FUNC_TEST=TRUE — 24 27 69
TP9502 A (1) TP-P5 — SPKRAMP_R_OUT_N — FUNC_TEST=TRUE — 24 27 69
TP9503 (TP) P5 (1)
TP9510 A (1) TP-P5
TP9511 A (1) TP-P5 — SPKRAMP_L_OUT_P — FUNC_TEST=TRUE — 24 27 69
TP9512 A (1) TP-P5 — SPKRAMP_L_OUT_N — FUNC_TEST=TRUE — 24 27 69
TP9513 A (1) P5

PP95D0 P4MM SM (PP) 1 I2S_SOC2SPKRAMP_MCK — 6 24
PP95D1 P4MM SM (PP) 1 I2S_SOC2SPKRAMP_BCLK — 6 24
PP95D2 P4MM SM (PP) 1 I2S_SOC2SPKRAMP_LRCK — 6 24
PP95D3 P4MM SM (PP) 1 I2S_SOC2SPKRAMP_DOUT — 6 24
PP95D4 P4MM SM (PP) 1 I2S_SPKRAMP2SOC_DOUT — 6 24
PP95D7 P4MM SM (PP) 1 I2S_SOC2CODEC_ASP_MCK — 6 22
PP95D8 P4MM SM (PP) 1 I2S_SOC2CODEC_ASP_BCLK — 6 22
PP95D9 P4MM SM (PP) 1 I2S_SOC2CODEC_ASP_LRCK — 6 22
PP95DA P4MM SM (PP) 1 I2S_SOC2CODEC_ASP_DOUT — 6 22
PP95DB P4MM SM (PP) 1 I2S_CODEC2SOC_ASP_DOUT — 6 22
PP95DC P4MM SM (PP) 1 I2S_SOC2CODEC_XSP_BCLK — 6 22
PP95DD P4MM SM (PP) 1 I2S_SOC2CODEC_XSP_LRCK — 6 22
PP95DE P4MM SM (PP) 1 I2S_SOC2CODEC_XSP_DOUT — 6 22
PP95DF P4MM SM (PP) 1 I2S_CODEC2SOC_XSP_DOUT — 6 22

CAMERA - FRONT

PP9520 P4MM SM (PP) 1 MIPI_CAM_FRONT_CLK_P — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AV36:3MM — 8 21 70
PP9521 P4MM SM (PP) 1 MIPI_CAM_FRONT_CLK_N — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AW36:3MM — 8 21 70
PP9522 P4MM SM (PP) 1 MIPI_CAM_FRONT_DATA_P<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AV37:3MM — 8 21 70
PP9523 P4MM SM (PP) 1 MIPI_CAM_FRONT_DATA_N<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AW37:3MM — 8 21 70

CAMERA - REAR

PP9524 P4MM SM (PP) 1 MIPI_CAM_REAR_CLK_P — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AV31:3MM — 8 21 70
PP9525 P4MM SM (PP) 1 MIPI_CAM_REAR_CLK_N — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AW31:3MM — 8 21 70
PP9526 P4MM SM (PP) 1 MIPI_CAM_REAR_DATA_P<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AV33:3MM — 8 21 70
PP9527 P4MM SM (PP) 1 MIPI_CAM_REAR_DATA_N<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AW33:3MM — 8 21 70

OSCAR

PP95C0 P4MM SM (PP) 1 TP_OSCAR_P0_05 — 17
PP95C1 P4MM SM (PP) 1 TP_OSCAR_P0_06 — 17
PP95C2 P4MM SM (PP) 1 TP_OSCAR_P0_09 — 17
PP95C3 P4MM SM (PP) 1 TP_OSCAR_P0_17 — 17
PP95C4 P4MM SM (PP) 1 TP_OSCAR_P0_21 — 17
PP95C8 P4MM SM (PP) 1 TP_OSCAR_P1_02 — 17
PP95C9 P4MM SM (PP) 1 TP_OSCAR_P1_03 — 17
PP95CD P4MM SM (PP) 1 SWD_OSCAR_IO_1V8 — 9 17
PP95CF P4MM SM (PP) 1 SWD_OSCAR_CLK_1V8 — 9 17

CHAN 0 NEAR DRAM

PP9534 P4MM SM (PP) 1 DDR0_CK_P — PLACE_NEAR=U1600.W13:1MM — 10 14 70
PP9535 P4MM SM (PP) 1 DDR0_CK_N — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.W12:1MM — 10 14 70
PP9536 P4MM SM (PP) 1 DDR0_CKE<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.W14:1MM — 10 14 70
PP9537 P4MM SM (PP) 1 DDR0_CA<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.V17:1MM — 10 14 70
PP9538 P4MM SM (PP) 1 DDR0_CA<1> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.W17:1MM — 10 14 70
PP9539 P4MM SM (PP) 1 DDR0_CA<2> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.V16:1MM — 10 14 70
PP9540 P4MM SM (PP) 1 DDR0_CA<3> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.W16:1MM — 10 14 70
PP9541 P4MM SM (PP) 1 DDR0_CSN<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.Y14:1MM — 10 14 70
PP9530 P4MM SM (PP) 1 DDR0_DQS_P<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.D15:1MM — 10 14 70
PP9531 P4MM SM (PP) 1 DDR0_DQS_N<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.D14:1MM — 10 14 70
PP9532 P4MM SM (PP) 1 DDR0_DQ<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.C17:1MM — 10 14 70

CHAN 0 NEAR SOC

PP9570 P4MM SM (PP) 1 DDR0_DQS_P<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.D7:1MM — 10 14 70
PP9571 P4MM SM (PP) 1 DDR0_DQS_N<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.D6:1MM — 10 14 70
PP9572 P4MM SM (PP) 1 DDR0_DQ<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.F10:1MM — 10 14 70

CHAN 1 NEAR DRAM

PP9542 P4MM SM (PP) 1 DDR1_DQS_P<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.K4:1MM — 10 14 70
PP9543 P4MM SM (PP) 1 DDR1_DQS_N<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.L4:1MM — 10 14 70
PP9544 P4MM SM (PP) 1 DDR1_DQ<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1600.H3:1MM — 10 14 70

CHAN 1 NEAR SOC

PP9582 P4MM SM (PP) 1 DDR1_DQS_P<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.V1:1MM — 10 14 70
PP9583 P4MM SM (PP) 1 DDR1_DQS_N<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.U1:1MM — 10 14 70
PP9584 P4MM SM (PP) 1 DDR1_DQ<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AA3:1MM — 10 14 70

WIFI

TP_JTAG_WLAN_TMS — FUNC_TEST=TRUE — 68
TP_JTAG_WLAN_TRST — FUNC_TEST=TRUE — 68
JTAG_WLAN_SEL — (TDI) FUNC_TEST=TRUE — 57
(TDO) FUNC_TEST=TRUE — 6 57 68
TP95B0 A (1) TP-P5 — WLAN_SOC2WLAN_RTS_L — FUNC_TEST=TRUE — 57
OSCAR2RADIO_CONTEXT_A — FUNC_TEST=TRUE — 57 68
FUNC_TEST=TRUE — 57 68
FUNC_TEST=TRUE — UART_BT2SOC_TX — 6 68
SOC2BT — FUNC_TEST=TRUE — 6 57
TRU — 68
E — 6 57 68
UART_SOC2WLAN_TX — WLAN2SOC — 6 68
40 57 71
UART_WLAN2BB_COEX_TX — FUNC_TEST=TRUE — 40 57
FUNC_TEST=TRUE — 71
FUNC_TEST=TRUE
I2S_SOC2BT_LRCK — FUNC_TEST=TRUE — 6 57 68
FUNC_TEST=TRUE
I2S_BT2SOC_DOUT — FUNC_TEST=TRUE — 6 68
FUNC_TEST=TRUE — 6 57 68
FUNC_TEST=TRUE — 57 62 68 69 70
CLK_PMU2WLAN_32K — FUNC_TEST=TRUE — 57 62 68 69
GPIO_PMU2WLAN_REG_ON — FUNC_TEST=TRUE — 68 69
FUNC_TEST=TRUE — 57 62
GPIO_2BBPMU_HOST_WAKE — FUNC_TEST=TRUE — 68
FUNC_TEST=TRUE — 68 70
FUNC_TEST=TRUE — 68

OTHER PPS
PP95B8 P4MM SM (PP) 1 WLAN_GPIO_8 — NO_TEST=TRUE — 57
PP95B9 P4MM SM (PP) 1 WLAN_GPIO_10 — NO_TEST=TRUE — 57

CHAN 2 NEAR DRAM

PP9548 P4MM SM (PP) 1 DDR2_CK_P — PLACE_NEAR=U1700.W13:1MM — 10 15 70
PP9549 P4MM SM (PP) 1 DDR2_CK_N — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.W12:1MM — 10 15 70
PP9550 P4MM SM (PP) 1 DDR2_CKE<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.W14:1MM — 10 15 70
PP9551 P4MM SM (PP) 1 DDR2_CA<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.V17:1MM — 10 15 70
PP9552 P4MM SM (PP) 1 DDR2_CA<1> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.W17:1MM — 10 15 70
PP9553 P4MM SM (PP) 1 DDR2_CA<2> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.V16:1MM — 10 15 70
PP9554 P4MM SM (PP) 1 DDR2_CA<3> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.W16:1MM — 10 15 70
PP9555 P4MM SM (PP) 1 DDR2_CSN<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.Y14:1MM — 10 15 70
PP9545 P4MM SM (PP) 1 DDR2_DQS_P<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.D15:1MM — 10 15 70
PP9546 P4MM SM (PP) 1 DDR2_DQS_N<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.D14:1MM — 10 15 70
PP9547 P4MM SM (PP) 1 DDR2_DQ<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.C17:1MM — 10 15 70

CHAN 2 NEAR SOC

PP9585 P4MM SM (PP) 1 DDR2_DQS_P<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AM1:1MM — 10 15 70
PP9586 P4MM SM (PP) 1 DDR2_DQS_N<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AL1:1MM — 10 15 70
PP9587 P4MM SM (PP) 1 DDR2_DQ<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AR3:1MM — 10 15 70

CHAN 3 NEAR DRAM

PP9556 P4MM SM (PP) 1 DDR3_DQS_P<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.K4:1MM — 10 15 70
PP9557 P4MM SM (PP) 1 DDR3_DQS_N<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.L4:1MM — 10 15 70
PP9558 P4MM SM (PP) 1 DDR3_DQ<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U1700.H3:1MM — 10 15 70

CHAN 3 NEAR SOC

PP9596 P4MM SM (PP) 1 DDR3_DQS_P<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AT10:1MM — 10 15 70
PP9597 P4MM SM (PP) 1 DDR3_DQS_N<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AT11:1MM — 10 15 70
PP9598 P4MM SM (PP) 1 DDR3_DQ<0> — NO_XNET_CONNECTION=TRUE — PLACE_NEAR=U0600.AP7:1MM — 10 15 70

I2C

I2C_OSCAR2PROX_SDA_1V8 — FUNC_TEST=TRUE — 17 58
I2C_OSCAR2PROX_SCL_1V8 — FUNC_TEST=TRUE — 17 58
I2C0_SCL_1V8 — FUNC_TEST=TRUE — 4 6
I2C0_SDA_1V8 — FUNC_TEST=TRUE — 4 6
I2C1_SCL_1V8 — FUNC_TEST=TRUE — 4 6
I2C1_SDA_1V8 — FUNC_TEST=TRUE — 4 6
I2C2_SCL_1V8 — FUNC_TEST=TRUE — 4 6
I2C2_SDA_1V8 — FUNC_TEST=TRUE — 4 6

PP95F4 P4MM SM (PP) 1 =I2C3_SDA_1V8 — 4
PP95F5 P4MM SM (PP) 1 =I2C3_SCL_1V8 — 4

I2C_HP_ALS_SCL_1V8_FILT — FUNC_TEST=TRUE — 23 69
I2C_HP_ALS_SDA_1V8_FILT — FUNC_TEST=TRUE — 23 69
I2C_MIC_ALS_SCL_1V8_F — FUNC_TEST=TRUE — 23 69
I2C_MIC_ALS_SDA_1V8_F — FUNC_TEST=TRUE — 23 69

UART

UART_SOC2ACC_TX — FUNC_TEST=TRUE — 6 25
UART_ACC2SOC_TX — FUNC_TEST=TRUE — 6 25
UART_SOC2OSCAR_TX — FUNC_TEST=TRUE — 6 17
UART_OSCAR2SOC_TX — FUNC_TEST=TRUE — 6 17

PP95B5 P4MM SM (PP) 1 UART_WLAN2SOC_RTS_L — 6 68
PP95B6 P4MM SM (PP) 1 UART_BT2SOC_RTS_L — 6 68
PP95B7 P4MM SM (PP) 1 UART_SOC2BT_RTS_L — 6 57 68

SOC SIDE PCIE TPS
PP95A0 P4MM SM (PP) 1 PLACE_NEAR=U0600.D28:3MM — PCIE_WLAN2SOC_TX_P — 9 68 70
PP95A1 P4MM SM (PP) 1 PLACE_NEAR=U0600.E28:3MM — PCIE_WLAN2SOC_TX_N — 9 68 70

REMOVED PCIE_SOC2WLAN_TX_C_P PP BECAUSE THE IT BLOCKED THE SHIM RING.
REMOVED PCIE_SOC2WLAN_TX_C_N PP BECAUSE THE "_P VERSION WAS REMOVED
PP95A6 P4MM SM (PP) 1 PLACE_NEAR=U0600.J40:3MM — PCIE_WLAN2SOC_CLKREQ_L — 9 68 70

WLAN SIDE PCIE TPS
PP95A7 P4MM SM (PP) 1 PLACE_NEAR=U7500.73:3MM — PCIE_WLAN2SOC_TX_C_P — 68 70
PP95A8 P4MM SM (PP) 1 PLACE_NEAR=U7500.74:3MM — PCIE_WLAN2SOC_TX_C_N — 68 70
PP95A9 P4MM SM (PP) 1 PLACE_NEAR=U7500.77:3MM — PCIE_SOC2WLAN_TX_P — 9 57 68 70
PP95B0 P4MM SM (PP) 1 PLACE_NEAR=U7500.76:3MM — PCIE_SOC2WLAN_TX_N — 9 57 68 70
PP95B1 P4MM SM (PP) 1 PLACE_NEAR=U7500.71:3MM — PCIE_SOC2WLAN_CLK_P — 9 57 68 70
PP95B2 P4MM SM (PP) 1 PLACE_NEAR=U7500.70:3MM — PCIE_SOC2WLAN_CLK_N — 9 68 70
PP95B3 P4MM SM (PP) 1 PLACE_NEAR=U7500.1:3MM — PCIE_SOC2WLAN_RESET_L

HIGH SPEED, NO TEST

DDR0_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR0_CK_P — NO_TEST=TRUE — 10 14 70
DDR0_CK_N — NO_TEST=TRUE — 10 14 70
DDR0_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR0_CKE<0..1> — NO_TEST=TRUE — 10 14
DDR0_CSN<0..1> — NO_TEST=TRUE — 10 14 70
DDR0_DM<0..3> — NO_TEST=TRUE — 10 14
DDR0_DQ<0..31> — NO_TEST=TRUE — 10 14 70
DDR0_DQS_P<0..3> — NO_TEST=TRUE — 10 14 70
DDR0_DQS_N<0..3> — NO_TEST=TRUE — 10 14 70
DDR1_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR1_CK_P — NO_TEST=TRUE — 10 14
DDR1_CK_N — NO_TEST=TRUE — 10 14
DDR1_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR1_CKE<0..1> — NO_TEST=TRUE — 10 14
DDR1_CSN<0..1> — NO_TEST=TRUE — 10 14
DDR1_DM<0..3> — NO_TEST=TRUE — 10 14
DDR1_DQ<0..31> — NO_TEST=TRUE — 10 14 70
DDR1_DQS_P<0..3> — NO_TEST=TRUE — 10 14 70
DDR1_DQS_N<0..3> — NO_TEST=TRUE — 10 14 70
DDR2_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR2_CK_P — NO_TEST=TRUE — 10 15 70
DDR2_CK_N — NO_TEST=TRUE — 10 15 70
DDR2_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR2_CKE<0..1> — NO_TEST=TRUE — 10 15 70
DDR2_CSN<0..1> — NO_TEST=TRUE — 10 15 70
DDR2_DM<0..3> — NO_TEST=TRUE — 10 15
DDR2_DQ<0..31> — NO_TEST=TRUE — 10 15 70
DDR2_DQS_P<0..3> — NO_TEST=TRUE — 10 15 70
DDR2_DQS_N<0..3> — NO_TEST=TRUE — 10 15 70
DDR3_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR3_CK_P — NO_TEST=TRUE — 10 15
DDR3_CK_N — NO_TEST=TRUE — 10 15
DDR3_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR3_CKE<0..1> — NO_TEST=TRUE — 10 15
DDR3_CSN<0..1> — NO_TEST=TRUE — 10 15
DDR3_DM<0..3> — NO_TEST=TRUE — 10 15
DDR3_DQ<0..31> — NO_TEST=TRUE — 10 15 70
DDR3_DQS_P<0..3> — NO_TEST=TRUE — 10 15 70
DDR3_DQS_N<0..3> — NO_TEST=TRUE — 10 15 70

MIPI_CAM_REAR_CLK_P — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_CLK_N — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_DATA_P<0..1> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_DATA_N<0..1> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_CLK_FILT_P — NO_TEST=TRUE — 20 21
MIPI_CAM_REAR_CLK_FILT_N — NO_TEST=TRUE — 20 21
MIPI_CAM_REAR_DATA_FILT_P<0..3> — NO_TEST=TRUE — 20 21
MIPI_CAM_REAR_DATA_FILT_N<0..3> — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_CLK_P — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_CLK_N — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_DATA_P<0> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_DATA_N<0> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_CLK_FILT_P — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_CLK_FILT_N — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_DATA_FILT_P<0> — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_DATA_FILT_N<0> — NO_TEST=TRUE — 20 21

EDP_DATA_P<0..3> — NO_TEST=TRUE — 9 32
EDP_DATA_N<0..3> — NO_TEST=TRUE — 9 32
EDP_DATA_EMI_P<0..3> — NO_TEST=TRUE — 32
EDP_DATA_EMI_N<0..3> — NO_TEST=TRUE — 32
EDP_DATA_EMI_CONN_P<0..3> — NO_TEST=TRUE — 31 32
EDP_DATA_EMI_CONN_N<0..3> — NO_TEST=TRUE — 31 32

PCIE_WLAN2SOC_TX_P — NO_TEST=TRUE — 9 68 70
PCIE_WLAN2SOC_TX_N — NO_TEST=TRUE — 9 68 70
PCIE_SOC2WLAN_TX_P — NO_TEST=TRUE — 9 57 68 70
PCIE_SOC2WLAN_TX_N — NO_TEST=TRUE — 9 57 68 70
PCIE_SOC2WLAN_CLK_P — NO_TEST=TRUE — 9 57 68 70
PCIE_SOC2WLAN_CLK_N — NO_TEST=TRUE — 9 57 68 70
PCIE_WLAN2SOC_TX_C_P — NO_TEST=TRUE — 68 70
PCIE_WLAN2SOC_TX_C_N — NO_TEST=TRUE — 68 70
PCIE_SOC2WLAN_TX_C_P — NO_TEST=TRUE — 9
PCIE_SOC2WLAN_TX_C_N — NO_TEST=TRUE — 9
PCIE_WLAN2SOC_CLKREQ_L — NO_TEST=TRUE — 9 68 70
PCIE_SOC2WLAN_RESET_L — NO_TEST=TRUE

POWER, NO TEST

PP6V0_LCM_HI — NO_TEST=TRUE — 61 63
SW_CHGA — NO_TEST=TRUE — 65
WLED_LX_A — NO_TEST=TRUE — 61 63
WLED_LX_B — NO_TEST=TRUE — 61 63
L81_PVCP — NO_TEST=TRUE — 22
L81_NVCP — NO_TEST=TRUE — 22
L81_FLYC — NO_TEST=TRUE — 22
L81_FLYN — NO_TEST=TRUE — 22
L81_FLYP — NO_TEST=TRUE — 22

GRAPE NO_TEST
MT_PANEL_IN<0..29> — NO_TEST=TRUE — 29 30
MT_PANEL_OUT<0..39> — NO_TEST=TRUE — 29

SYNC_MASTER=N/A — SYNC_DATE=N/A
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RF TEAM REQUESTED TPS

SIMCRD_RST_CONN_FILT	FUNC_TEST=TRUE	59 69
SIMCRD_CLK_CONN_FILT	FUNC_TEST=TRUE	59 69
SIMCRD_IO_CONN_FILT	FUNC_TEST=TRUE	59 69
SIMCRD_DETECT_FILT	FUNC_TEST=TRUE	59 69
PP_LDO6	FUNC_TEST=TRUE	35 36 69 73
UART_BB2SOC_TX	FUNC_TEST=TRUE	6 25 68
UART_SOC2BB_TX	FUNC_TEST=TRUE	6 25 68
UART_BB2SOC_RTS_L	FUNC_TEST=TRUE	6 68
UART_SOC2BB_RTS_L	FUNC_TEST=TRUE	6 68
UART_OSCAR2BB_TX	FUNC_TEST=TRUE	17 68
UART_BB2OSCAR_TX	FUNC_TEST=TRUE	17 68
UART_BB2WLAN_COEX_RX	FUNC_TEST=TRUE	40 57 70
UART_WLAN2BB_COEX_TX	FUNC_TEST=TRUE	40 57 70
GPIO_SOC2BB_WAKE_MODEM	FUNC_TEST=TRUE	6 68
GPIO_BB2SOC_GPS_SYNC	FUNC_TEST=TRUE	6 68
USB_BB_P	FUNC_TEST=TRUE	25 68
USB_BB_N	FUNC_TEST=TRUE	25 68
GPIO_SOC2BB_COREDUMP	FUNC_TEST=TRUE	6 68
GPIO_SOC2BB_RADIO_ON_L	FUNC_TEST=TRUE	6 68 69
GPIO_PMU2BBPMU_RESET_L	FUNC_TEST=TRUE	62 68 69 70
GPIO_PMU2BB_VBUS_DET	FUNC_TEST=TRUE	62 68 69

PP9600_P4MM_SM	HSIC_BB_DATA	5 68
PP9601_P4MM_SM	HSIC_BB_STB	5 68

SYNC_MASTER=N/A SYNC_DATE=N/A

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TEST: CELL EE TP/PP

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POWER CONNECTIONS

BUCK0 (DWI DVC)

69 60 PPVDD_CPU — =PPVDD_CPU 13
MAKE_BASE=TRUE
VOLTAGE=1.1V

BUCK1 (DWI DVC)

69 60 PPVDD_GPU — =PPVDD_GPU 13
MAKE_BASE=TRUE
VOLTAGE=1.1V

BUCK2

69 60 PP0V95_SOC
MAKE_BASE=TRUE
VOLTAGE=0.95V
- =PP0V95_SOC 12
- =PP0V95_PCIE_SOC 9
- =PP0V95_USB_SOC 5

BUCK3

69 61 60 PP1V8_S2R
MAKE_BASE=TRUE
VOLTAGE=1.8V
- =PP1V8_S2R_DDR 14 15
- =PP1V8_S2R_GRAPE_EXTERNAL_SW 30
- =PP1V8_S2R_TRISTAR 25
- =PP1V8_S2R_VDDIO_WLAN_BT 68
- =PP1V8_S2R_MISC 6 9 66 67
- =PP1V8_S2R_EXTERNAL_SW 64
- =PP1V8_S2R_ROTTERDAM 34

BUCK3_SW

BUCK3_SW1

69 67 60 PP1V8_SW1
MAKE_BASE=TRUE
VOLTAGE=1.8V
- =PP1V8_AUDIO 22 24
- =PP1V8_SW1_EXT_SW_ON 64
- XWC130 SM 1 2 PP1V8_SW1_FOREHEAD 69 72

72 69 PP1V8_SW1_FOREHEAD
MAKE_BASE=TRUE
VOLTAGE=1.8V
- =PP1V8_CAM_FRONT 21
- =PP1V8_CAM_REAR 21
- =PP1V8_DMIC 23 28

BUCK3_SW1_EXT

69 64 PP1V8_EXT_SW
MAKE_BASE=TRUE
VOLTAGE=1.8V
- =PP1V8_VDDIO18_SOC 11
- =PP1V8_XTAL_SOC 11
- =PP1V8_PCIE_SOC 9
- =PP1V8_MIPI_SOC 8
- =PP1V8_NAND_SOC 7
- =PP1V8_NAND 16 70
- =PP1V8_NAND_EXT_SW_ON 64
- =PP1V8_SOC 4 5 6 62
- =PP1V8_EEPROM 6

BUCK3_SW2

69 60 PP1V8_SW2
MAKE_BASE=TRUE
VOLTAGE=1.8V
- =PP1V8_SPKRAMP_DVDD 24

69 30 PP1V8_GRAPE_EXT_SW
MAKE_BASE=TRUE
VOLTAGE=1.8V
- =PP1V8_GRAPE_EXT_SW 29 30

BUCK3_SW3

69 60 PP1V8_S2R_SW3
MAKE_BASE=TRUE
VOLTAGE=1.8V
- =PP1V8_S2R_OSCAR 17
- =PP1V8_S2R_PHOS 18
- =PP1V8_S2R_GYRO 18
- =PP1V8_S2R_COMPASS 18
- =PP1V8_S2R_ACCEL 18
- =PP1V8_S2R_PROX 58

BUCK4

69 61 60 PP1V2_S2R
MAKE_BASE=TRUE
VOLTAGE=1.2V
- =PP1V2_EXTERNAL_SW 64
- =PP1V2_S2R_DDR 14 15
- =PP1V2_S2R_DDR_SOC 10

BUCK4_SW1

69 60 PP1V2_SW1
MAKE_BASE=TRUE
VOLTAGE=1.2V
- =PP1V2_EXT_SW_ON 64

69 64 PP1V2_EXT_SW
MAKE_BASE=TRUE
VOLTAGE=1.2V
- =PP1V2_DDR_VDDQ 14 15
- =PP1V2_VDDIOD_SOC 10 11
- =PP1V2_HSIC_SOC 5
- =PP1V2_PLL_SOC 9 11
- =PP1V2_CAM_FRONT 21

BUCK4_SW2

69 60 PP1V2_S2R_SW2
MAKE_BASE=TRUE
VOLTAGE=1.2V
- =PP1V2_S2R_OSCAR 17

BUCK5 (DWI DVC)

69 60 PPVDD_SRAM
MAKE_BASE=TRUE
VOLTAGE=1.1V
- =PPVDD_SRAM 13

BUCK6

69 60 PP3V3_S2R
MAKE_BASE=TRUE
VOLTAGE=3.3V
- =PP3V3_S2R_EXTERNAL_SW 64
- =PP3V3_S2R_WIFI_PA 68

69 64 PP3V3_EXT_SW
MAKE_BASE=TRUE
VOLTAGE=3.3V
- =PP3V3_NAND 16
- =PP3V3_USB_SOC 5

LDO1

69 61 PP3V0_S2R_HALL
MAKE_BASE=TRUE
VOLTAGE=3.0V
- =PP3V0_S2R_HALL 19 30

LDO2

69 61 PP1V7_VA_VCP
MAKE_BASE=TRUE
VOLTAGE=1.7V
- =PP1V7_VA_VCP 22

LDO3

69 61 PP3V0_S2R_SENSOR
MAKE_BASE=TRUE
VOLTAGE=3.0V
- =PP3V0_S2R_PROX 58
- =PP3V0_S2R_COMPASS 18
- =PP3V0_S2R_GYRO 18

LDO4

69 61 PP3V0_ALS
MAKE_BASE=TRUE
VOLTAGE=3.0V
- =PP3V0_HP_ALS 23
- =PP3V0_MIC_ALS 23

LDO5

69 61 PP3V1_S2R_MESA
MAKE_BASE=TRUE
VOLTAGE=3.1V
- =PP3V1_S2R_MESA 33

LDO6

69 61 PP3V3_ACC
MAKE_BASE=TRUE
VOLTAGE=3.3V
- =PP3V3_ACC 25

LDO7

69 61 PP3V0_S2R_TRISTAR
MAKE_BASE=TRUE
VOLTAGE=3.0V
- =PP3V0_S2R_TRISTAR 25
- =PP3V0_S2R_ANT_SW 59

LDO8

72 69 61 PP3V0_MISC
MAKE_BASE=TRUE
VOLTAGE=3.0V
- PP3V0_MISC 61 69 72

LDO9

69 61 PP1V25_CAM
MAKE_BASE=TRUE
VOLTAGE=1.25V
- =PP1V25_CAM_REAR 21

LDO10

69 61 PP1V0_SOC
MAKE_BASE=TRUE
VOLTAGE=1.0V
- =PP1V0_MIPI_SOC 8
- =PP1V0_LPDP_SOC 9

LDO11

69 61 PP2V6_CAM_AF
MAKE_BASE=TRUE
VOLTAGE=2.6V
- =PP2V6_CAM_REAR_AF 21

LDO13

69 61 PP2V9_CAM
MAKE_BASE=TRUE
VOLTAGE=2.9V
- =PP2V9_CAM_FRONT 21
- =PP2V9_CAM_REAR 21

LDO14

72 69 61 PP1V8_SPARE
MAKE_BASE=TRUE
VOLTAGE=1.8V
- PP1V8_SPARE 61 69 72

VLCM1

69 61 PP5V25_GRAPE
MAKE_BASE=TRUE
VOLTAGE=5.25V
- =PP5V25_GRAPE 29 30

CHARGER MAIN

69 65 64 61 60 PPVCC_MAIN
MAKE_BASE=TRUE
VOLTAGE=4.7V
- =PPVCC_MAIN_AUDIO 22
- =PPVCC_MAIN_LED 63
- =PPVCC_MAIN_CPU 60
- =PPVCC_MAIN_GPU 60
- =PPVCC_MAIN_SOC 60
- =PPVCC_MAIN_GRAPE 29 30
- =PPVCC_MAIN_LCD 32
- =PPVCC_MAIN_VDD_LCM 61
- =PPVCC_MAIN_WLAN 68
- =PPVCC_MAIN_MESA 33
- =PPVCC_MAIN_ROTTERDAM 34

BATTERY

69 65 60 PPBATT_VCC
MAKE_BASE=TRUE
VOLTAGE=4.7V
- =PPBATT_POS_CONN 66
- =PPBATT_VCC_BB 68
- =PPBATT_AUDIO 24

USB POWER INPUT

69 65 PPVBUS_USB_DCIN
MAKE_BASE=TRUE
VOLTAGE=16V
- =PPVBUS_USB_EMI 26

ON_BUF

69 61 PP1V8_ALWAYS
MAKE_BASE=TRUE
VOLTAGE=1.8V
- =PP1V8_ALWAYS 6 11 62

BACKLIGHT BOOST

69 63 PPLED_OUT_A
MAKE_BASE=TRUE
VOLTAGE=20.4V
- =PPLED_REG_A 32

69 63 PPLED_OUT_B
MAKE_BASE=TRUE
VOLTAGE=20.4V
- =PPLED_REG_B 32

SYNC_MASTER=N/A SYNC_DATE=N/A

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1.225V	PP_LDO1	36 38 42 43
1.8V	PP_LDO2	36 38
1.8V	PP_LDO3	36 37 38 55
3.075V	PP_LDO4	36 38
2.85V	PP_LDO5	36 38 59
2.85V	PP_LDO6	35 36 69 71
1.9V	PP_LDO7	36 38 40
2.05V	PP_LDO8	36 42 43
1.2V	PP_LDO9	36 38
0.9V	PP_LDO10	36 38
1.8V	PP_LDO11	35 36 38 39 40 42 43 44
0.95V	PP_LDO12	36 38
2.95V	PP_LDO13	36 38 55 69
2.95V	PP_LDO13_GPS	55
2.7V	PP_LDO14_RFSW	36 46 47
0.95V	VREG_SMPS3_0V95	36 69
2.075V	VREG_SMPS4_2V075	36

0.9V	PP_VSW_S1	36
1.25V	PP_VSW_S2	36
0.95V	PP_VSW_S3	36
2.075V	PP_VSW_S4	36

4.7V	PP_BATT_VCC	35 44 53 68
4.7V	PP_VCC_MAIN	73
4.2V	PP_BATT_VCC_2GPA	45
4.2V	PP_BATT_VCC_QPOET	44 45 50 51
4.2V	PP_BATT_VCC_RADIO	35 36
4.7V	PP_BATT_VCC_DSM	53
4.2V	PP_BATT_VCC_QPOET_HBS	51
4.2V	PP_BATT_VCC_QPOET_ASM	50
1.8V	PP_1V8_S2R_VDDIO_WLAN_BT	57 68
1.8V	PP_WL_VDDIO	57
4.7V	PP_VCC_MAIN	73

	S1_GND	36
0V	S2_GND	36
0V		36
		36
0V	GND_SW	44
0V	VOUT_BOOST_GND	44

SYNC_MASTER=N/A SYNC_DATE=N/A

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BB/WLAN VOLTAGE ATTRIBUTES

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