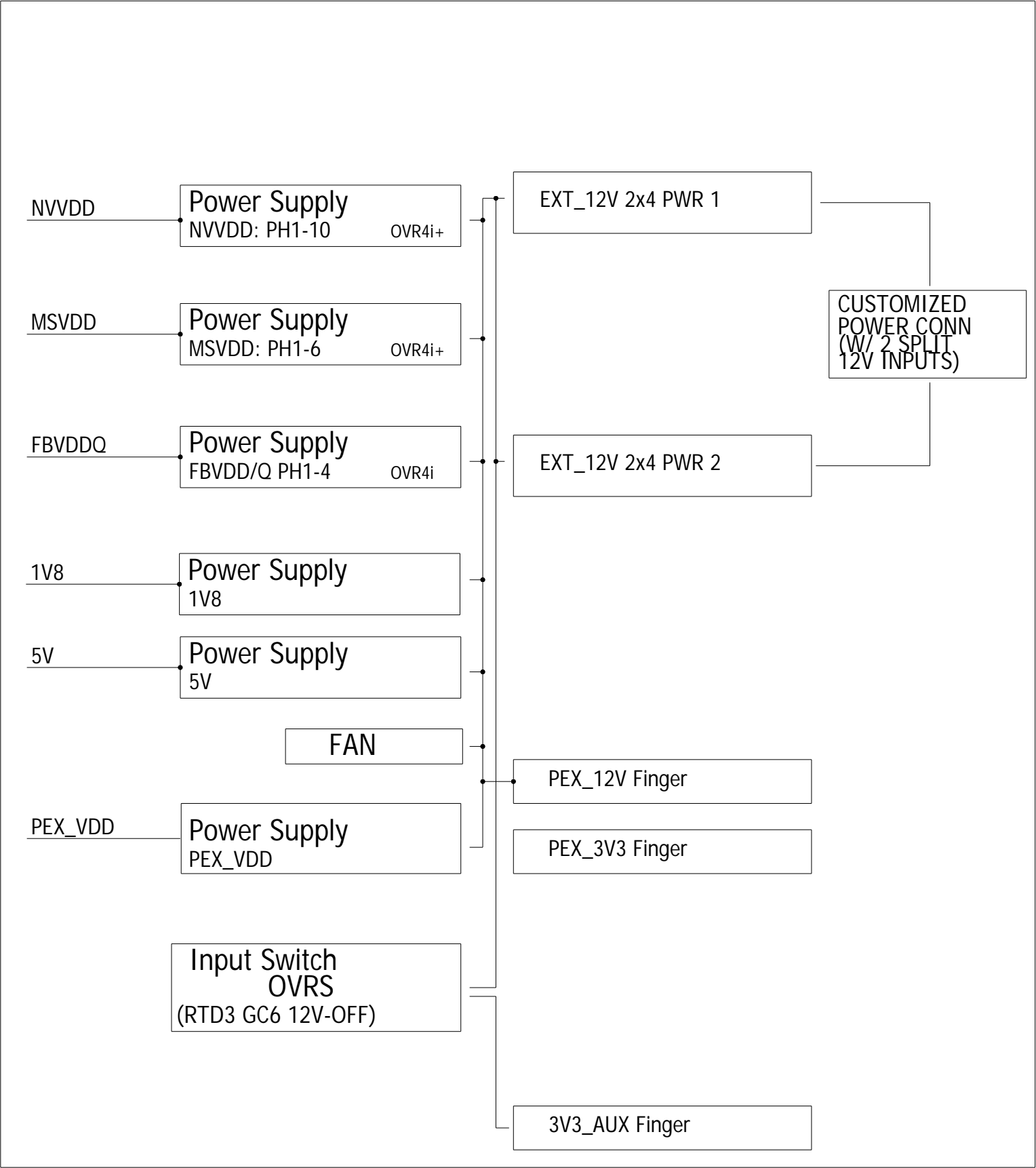
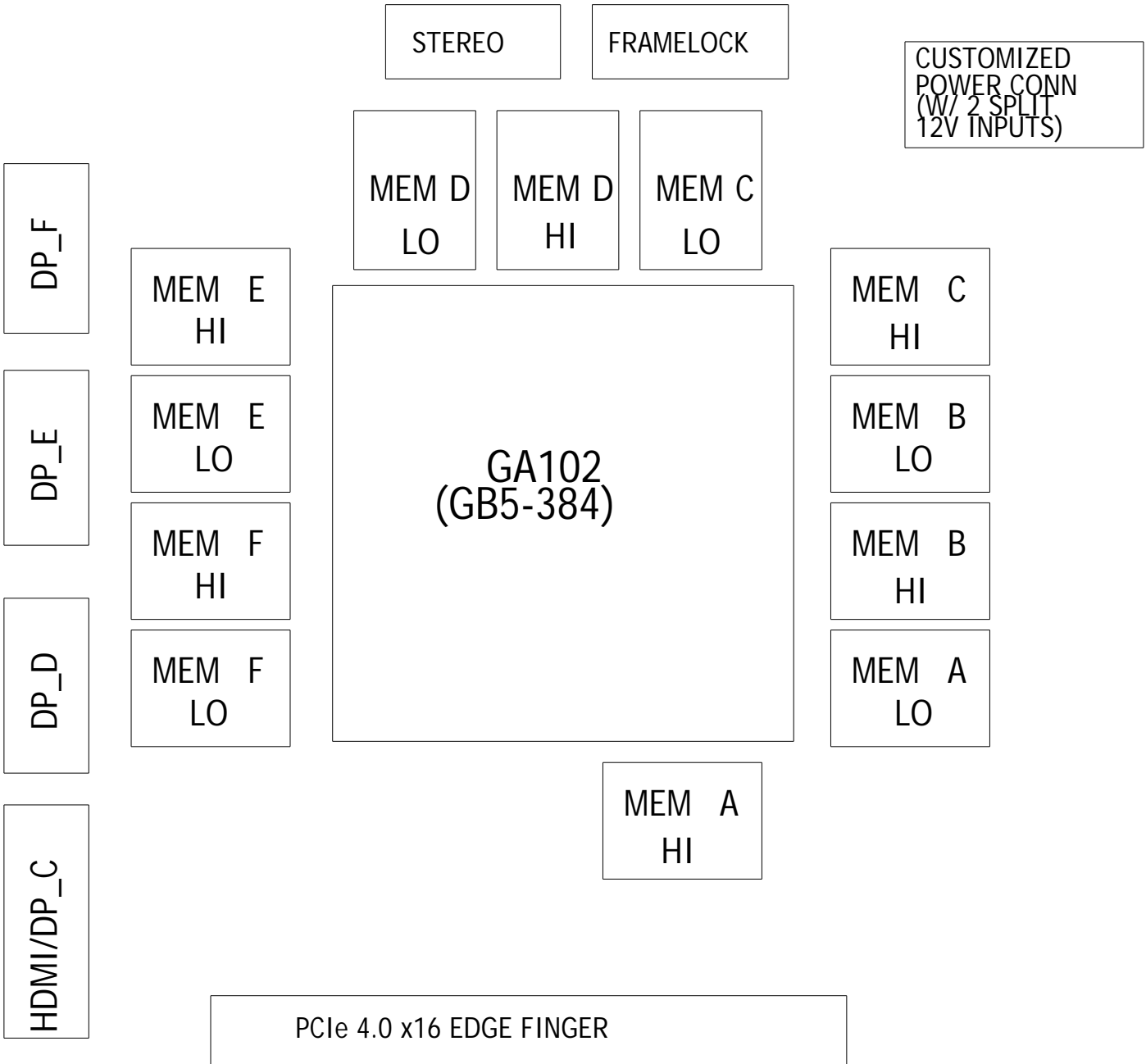


## 1

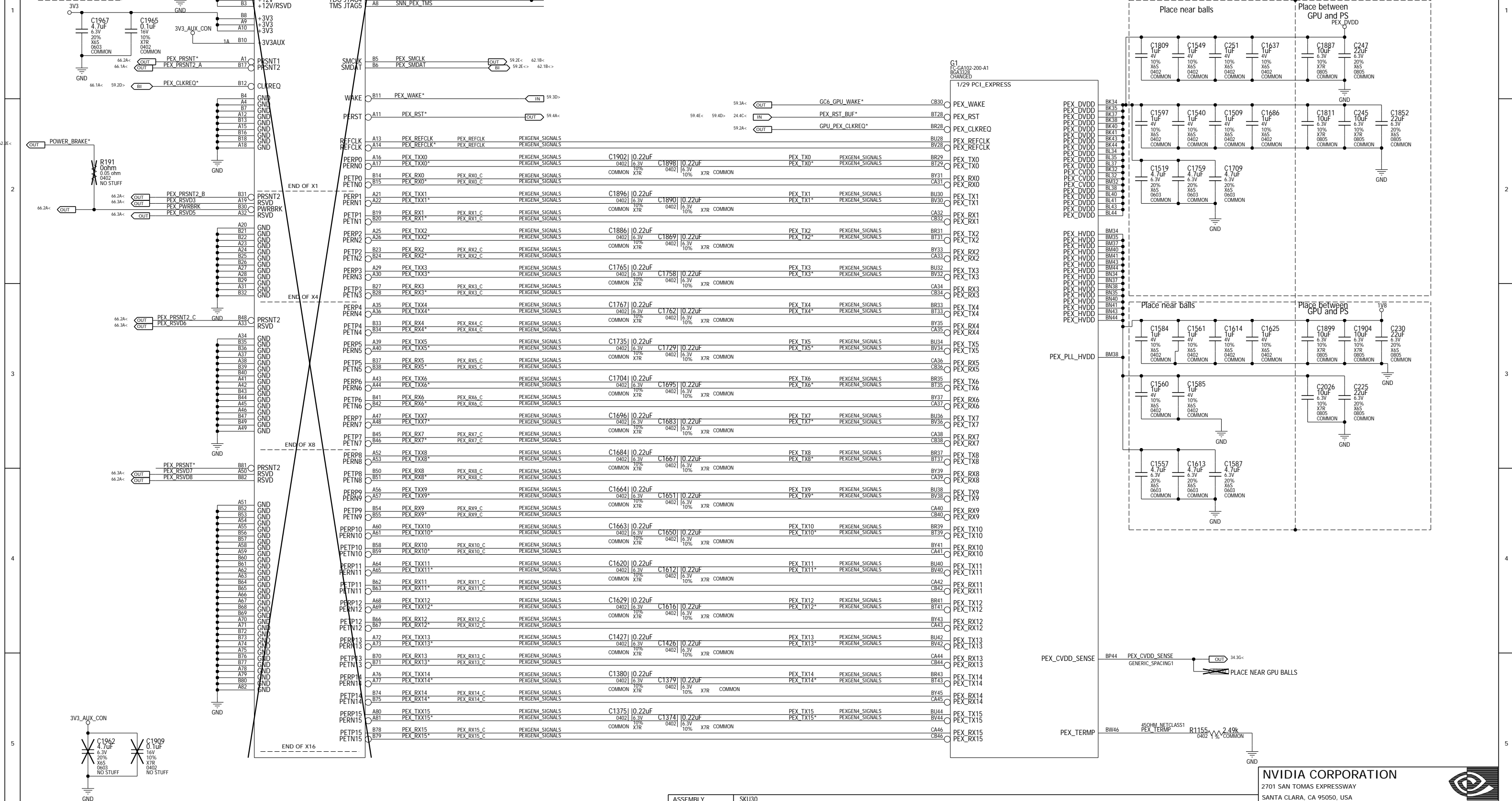
## 2

345

Page 2: Block Diagram



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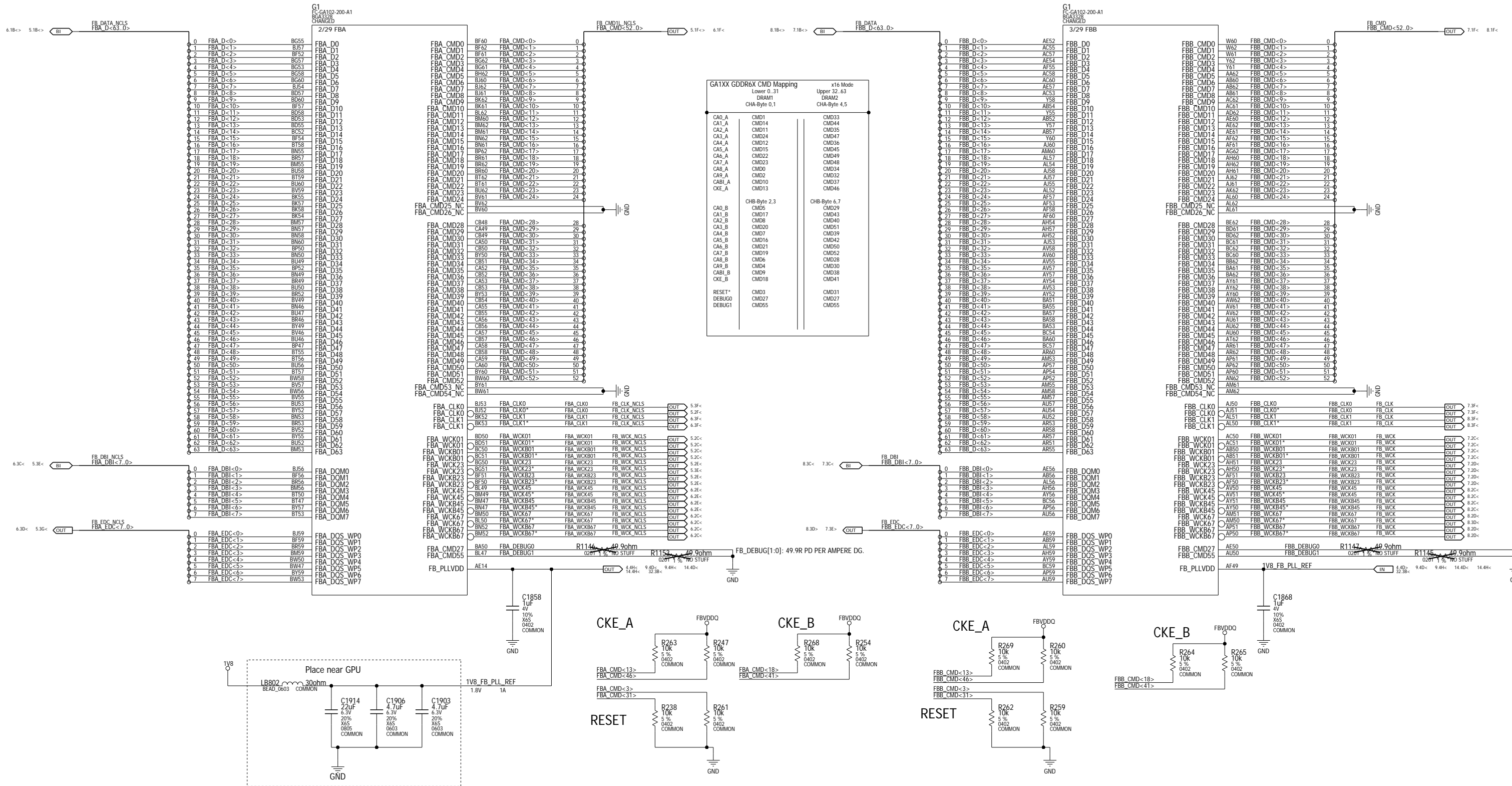
2701 SAN TOMAS EXPRESSWAY

PCB REV	PG133-A03	PAGE	3 OF 67
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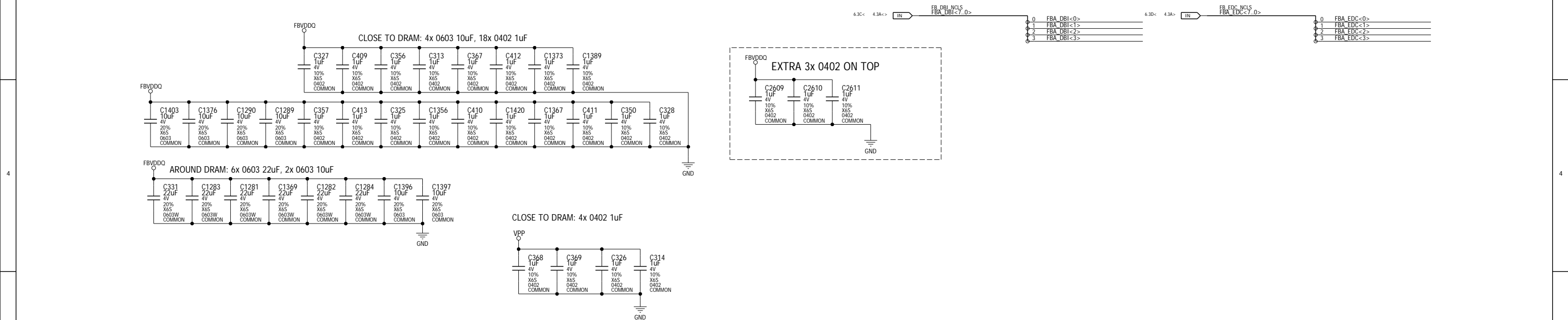
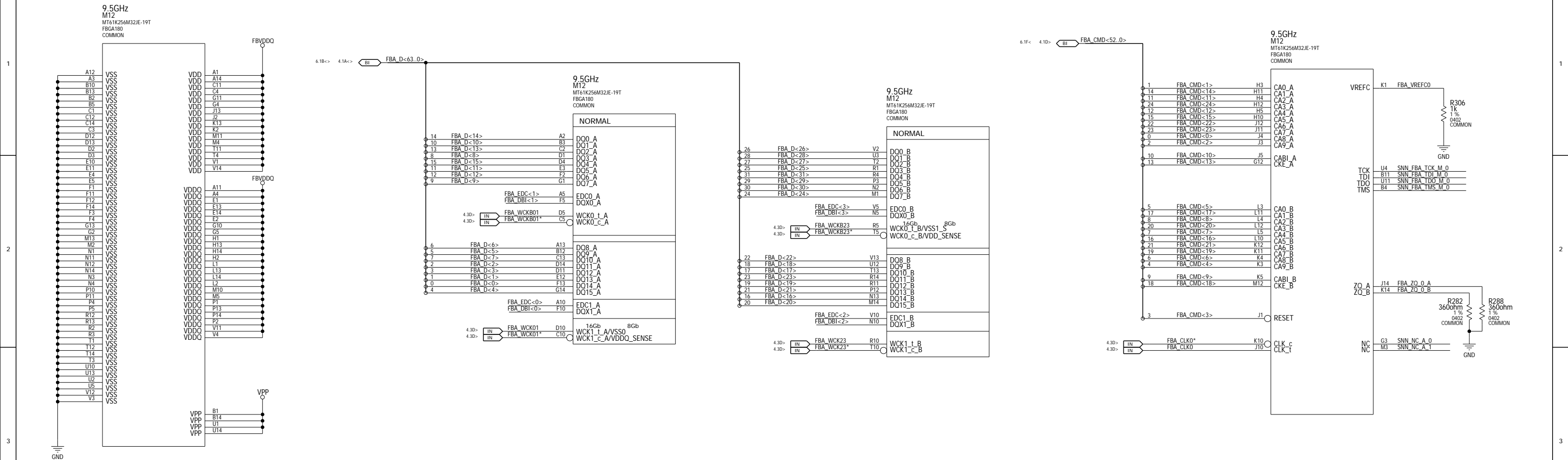
BOM REV	A	DATE	11-JUN-2020
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[illegible]

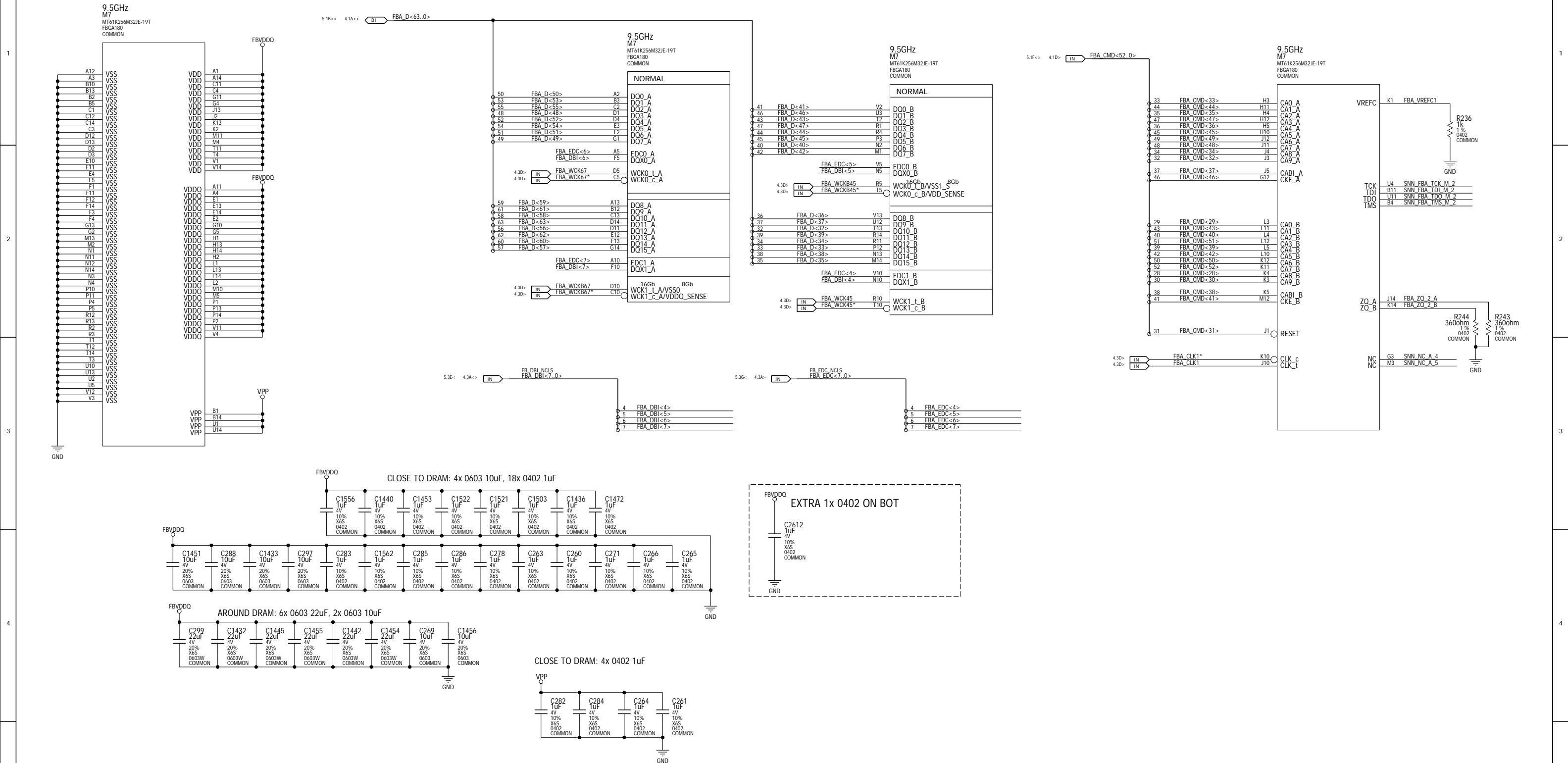
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## Page5: MEMORY: FBA Partition 31..0



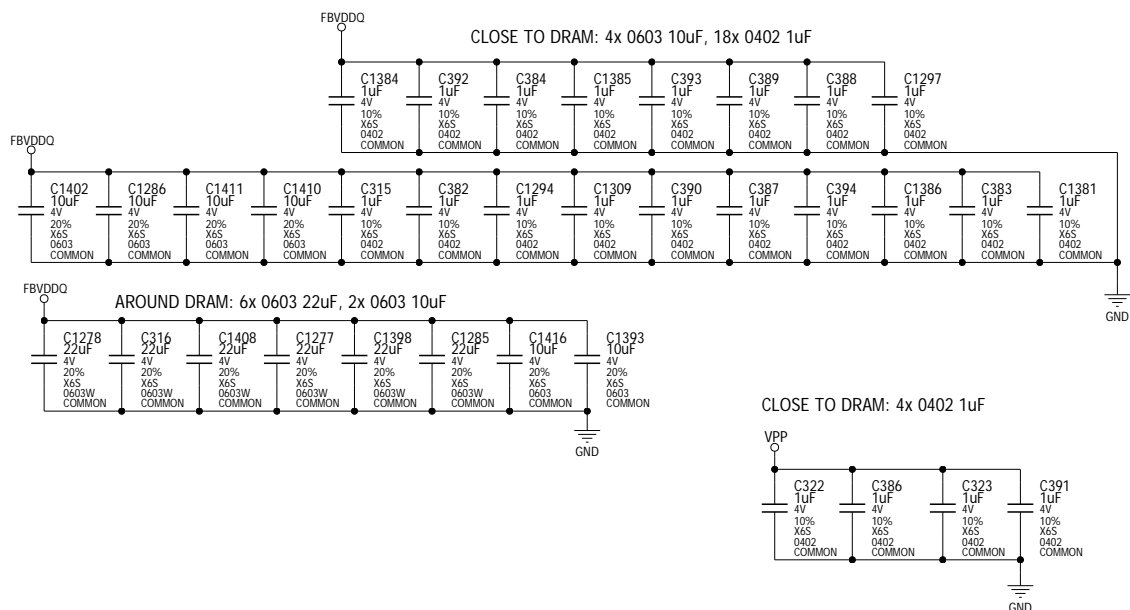
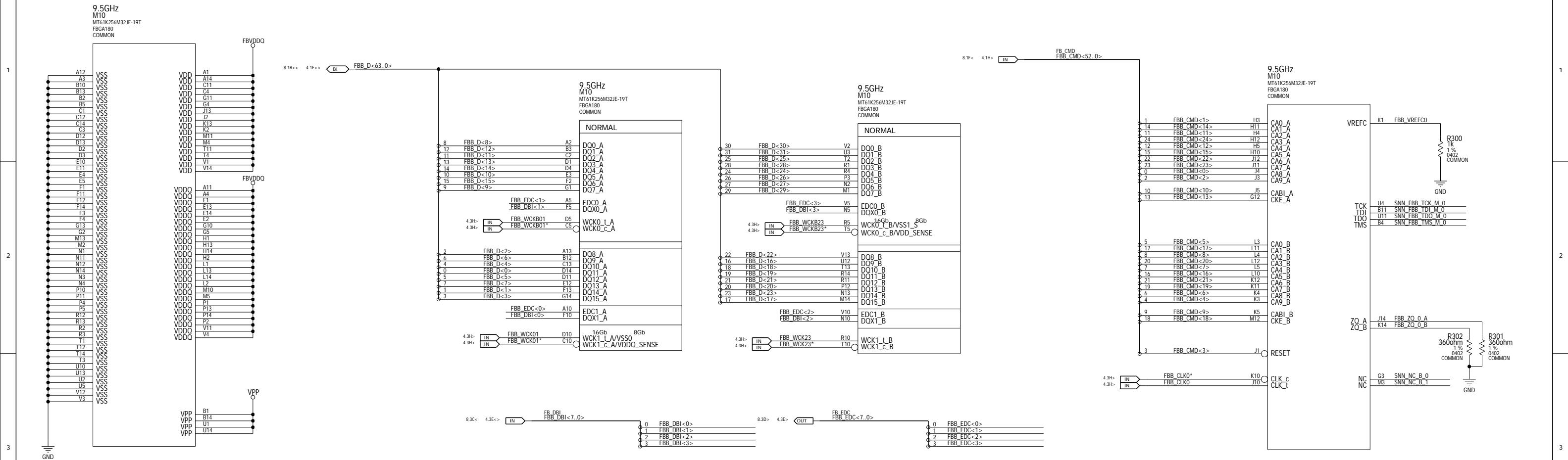
## Page6: MEMORY: FBA Partition 63..32



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<b>NV_PN</b>		<b>600-1G133-0030-900</b>		
<b>PCB REV</b>	<b>PG133-A03</b>	<b>PAGE</b>	<b>6 OF 67</b>	
<b>BOM REV</b>	<b>A</b>	<b>DATE</b>	<b>11-JUN-2020</b>	


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## Page7: MEMORY: FBB Partition 31..0

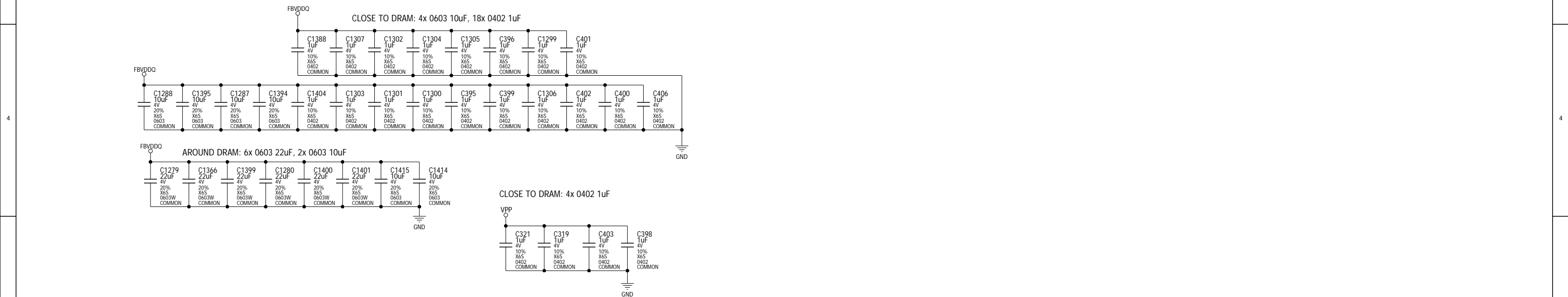
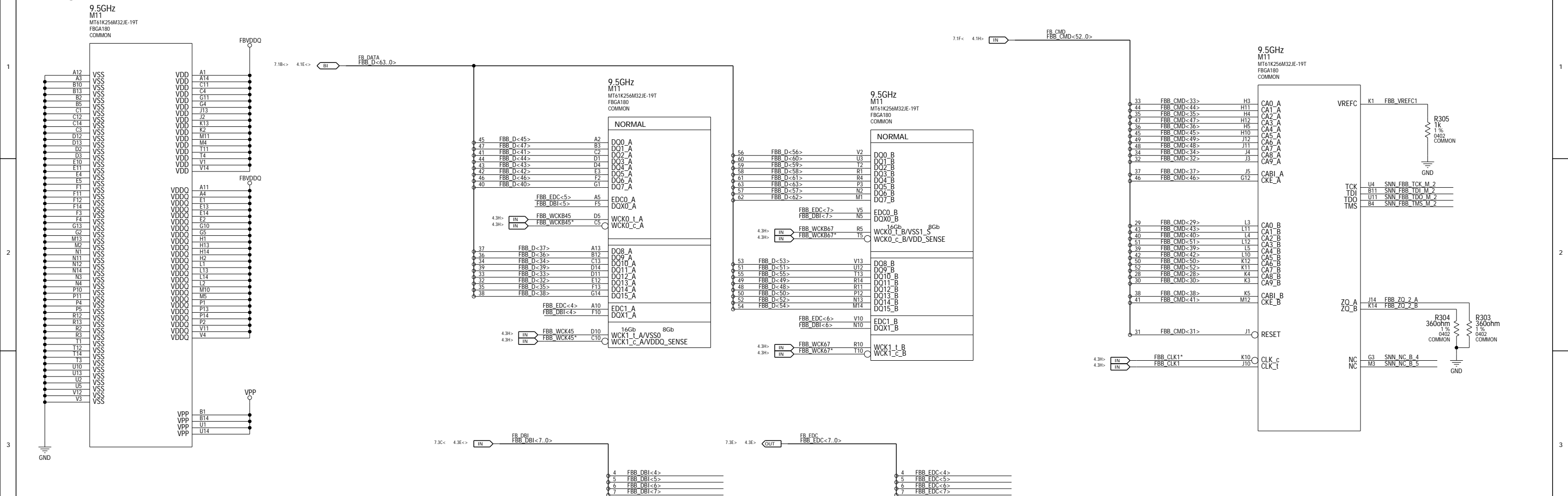


ASSEMBLY	SKU30
PAGE DETAIL	MEMORY: FBB PARTITION[31:0]

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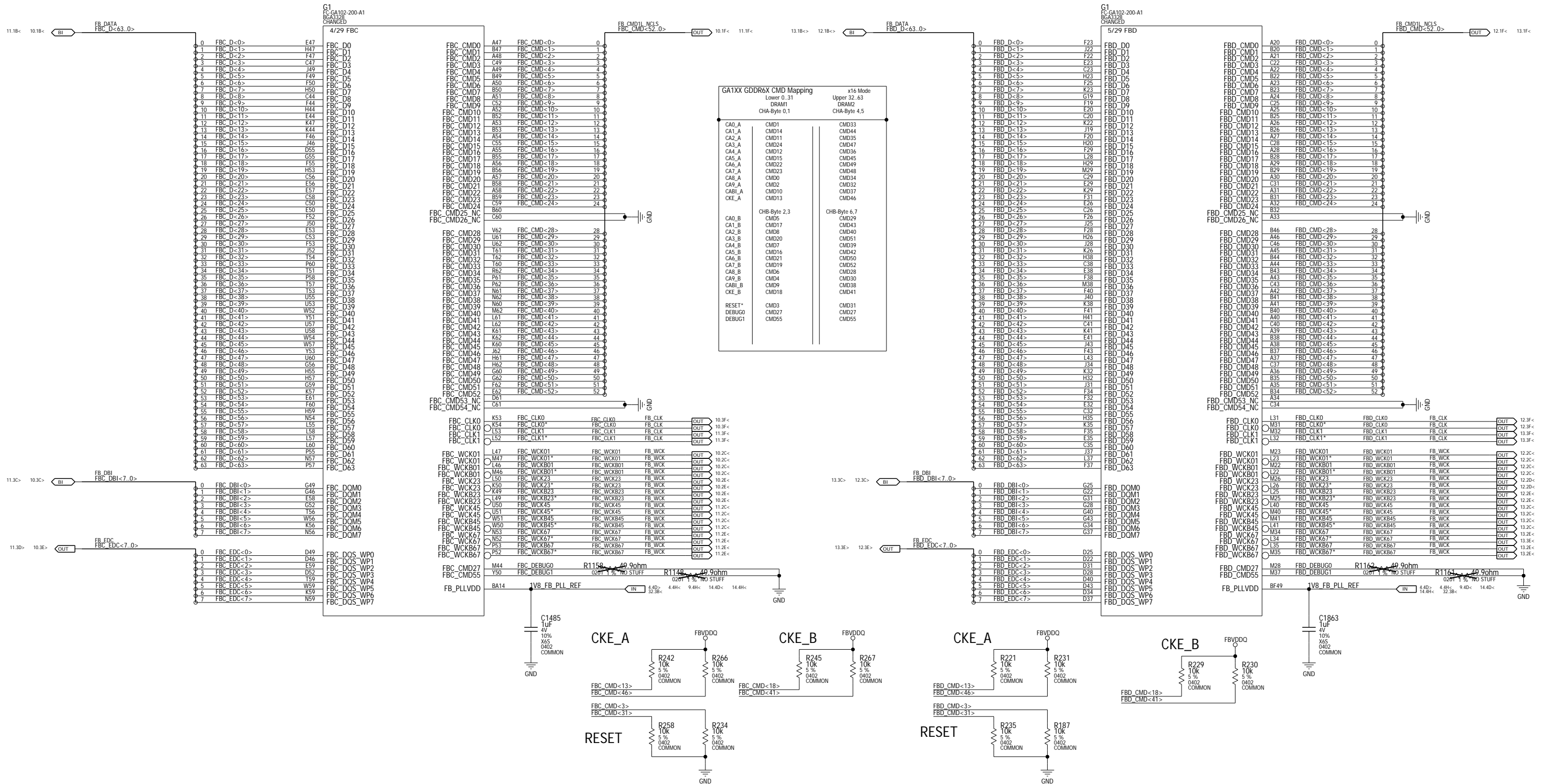
<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
<b>NV_PN</b>	<b>600-1G133-0030-900</b>		
<b>PCB REV</b>	<b>PG133-A03</b>	<b>PAGE</b>	<b>7 OF 67</b>
<b>BOM REV</b>	<b>A</b>	<b>DATE</b>	<b>11-JUN-2020</b>

## Page8: MEMORY: FBB Partition 63..32

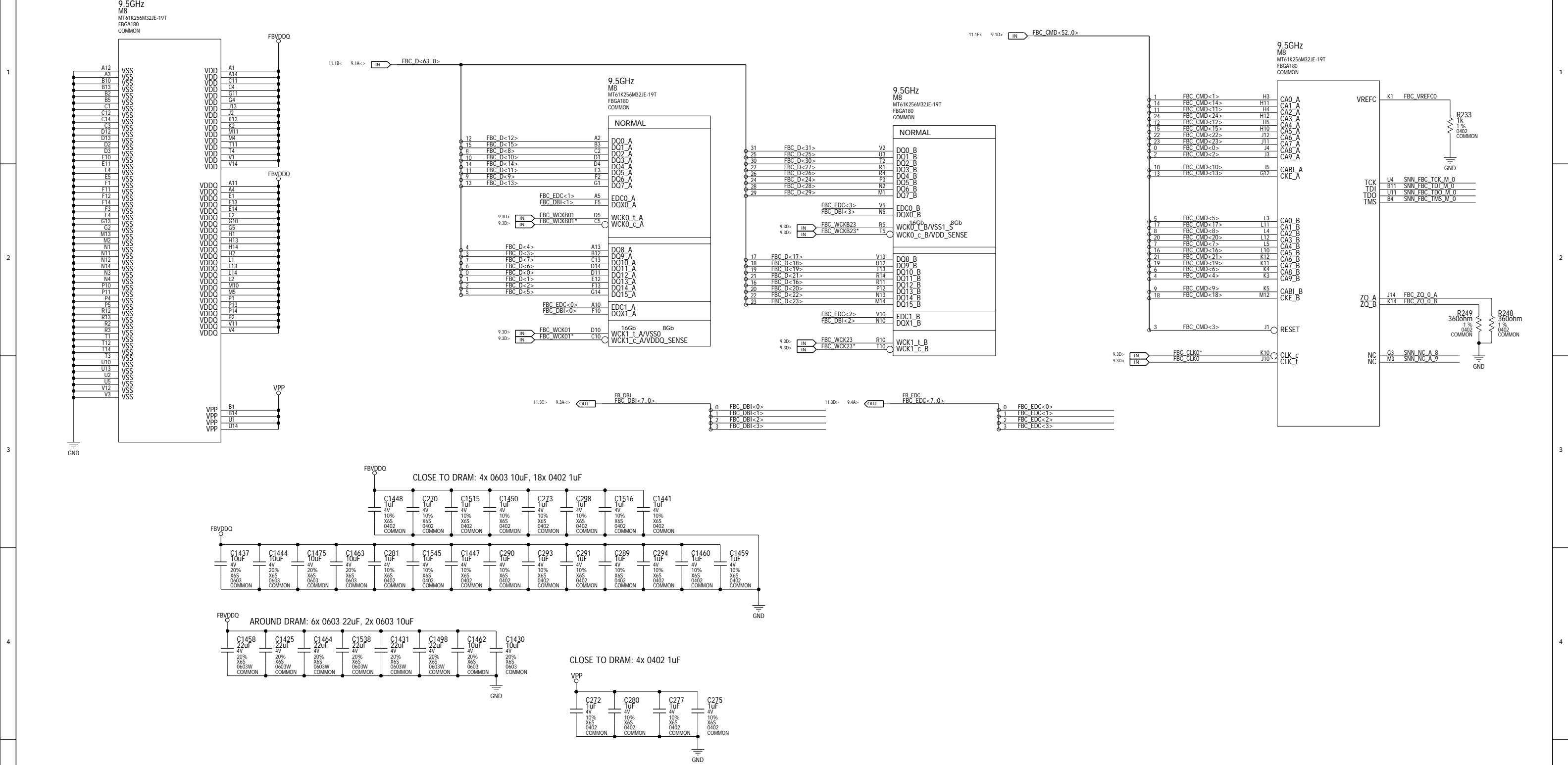


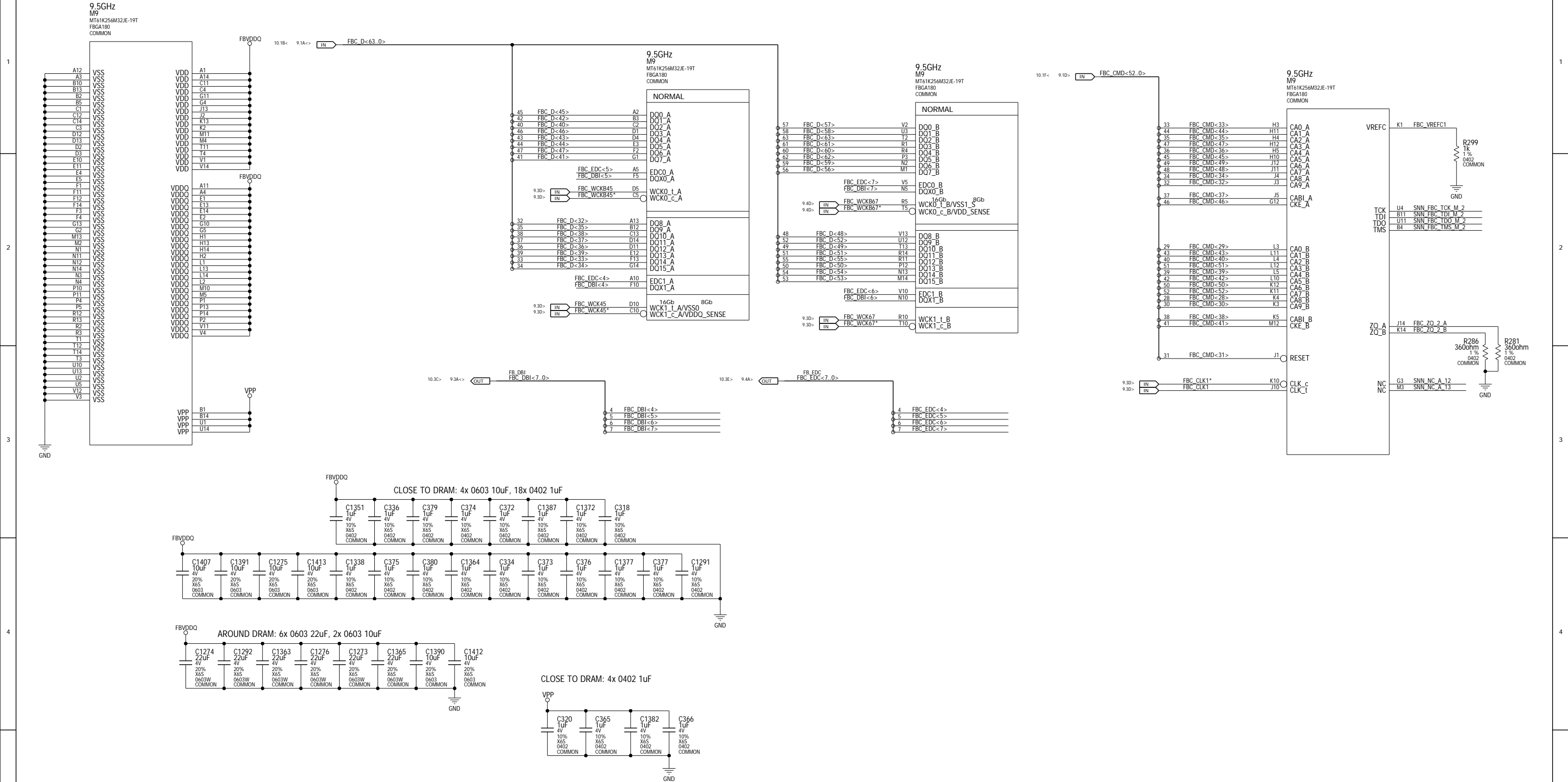


## Page 9: MEMORY: GPU Partition C/D

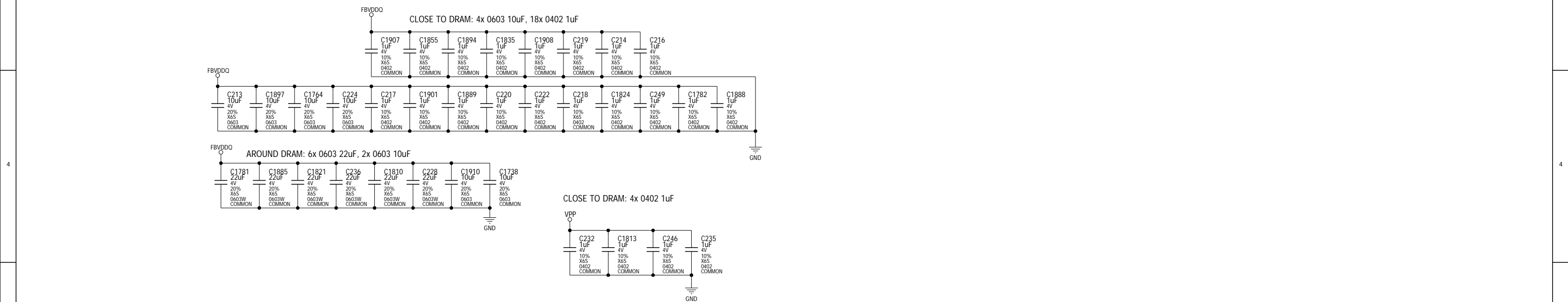
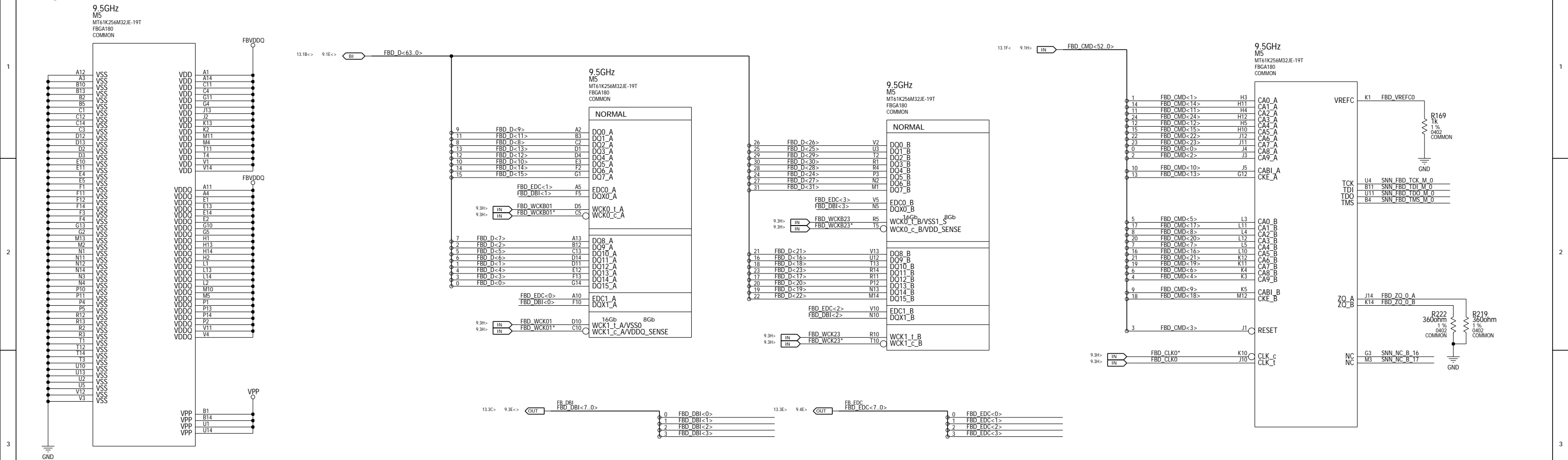


Page 10: MEMORY: FBC Partition 31..0

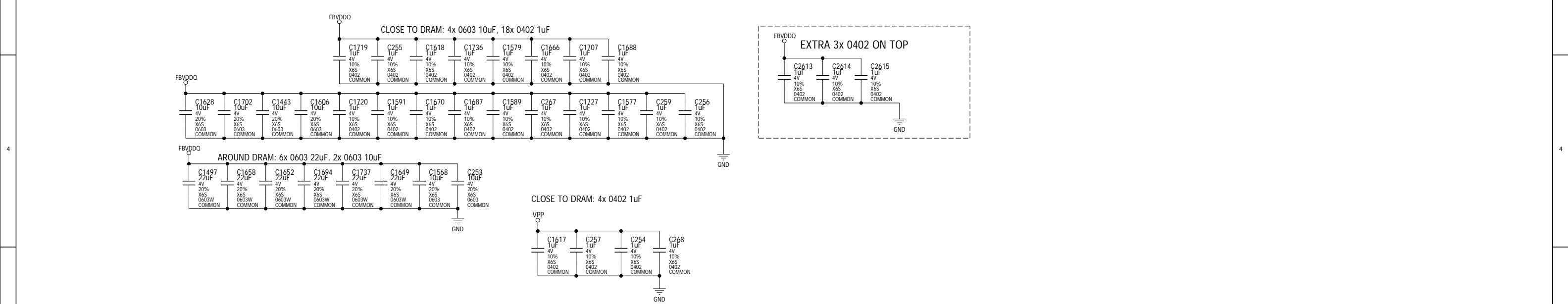
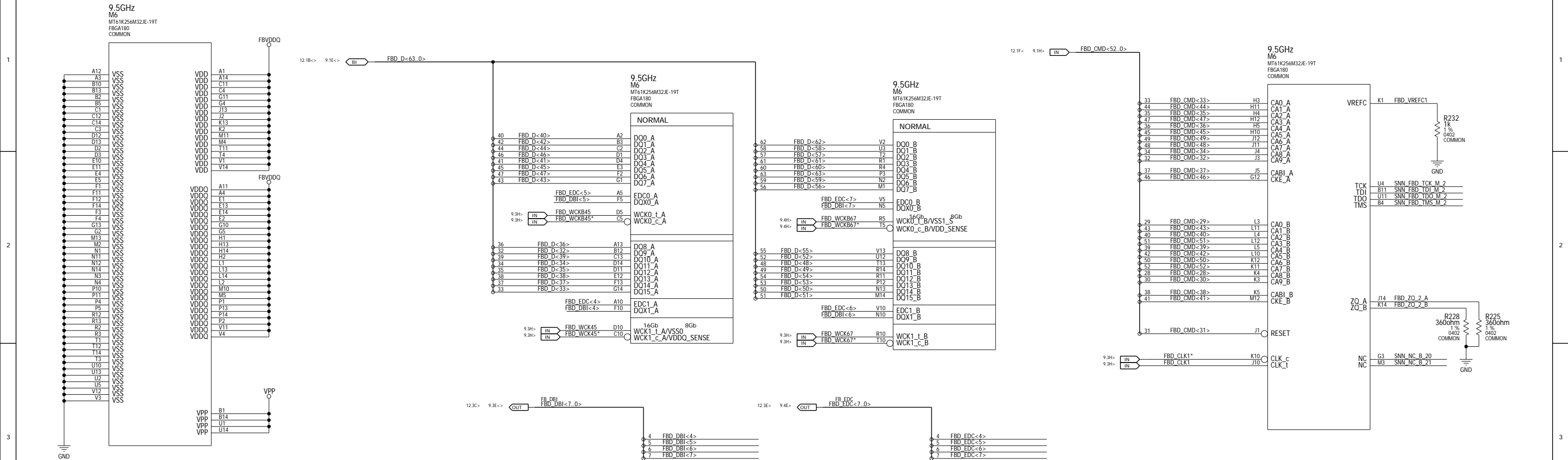




## Page 12: MEMORY: FBD Partition 31..0



Page 13: MEMORY: FBD Partition 63..32



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BOM REV

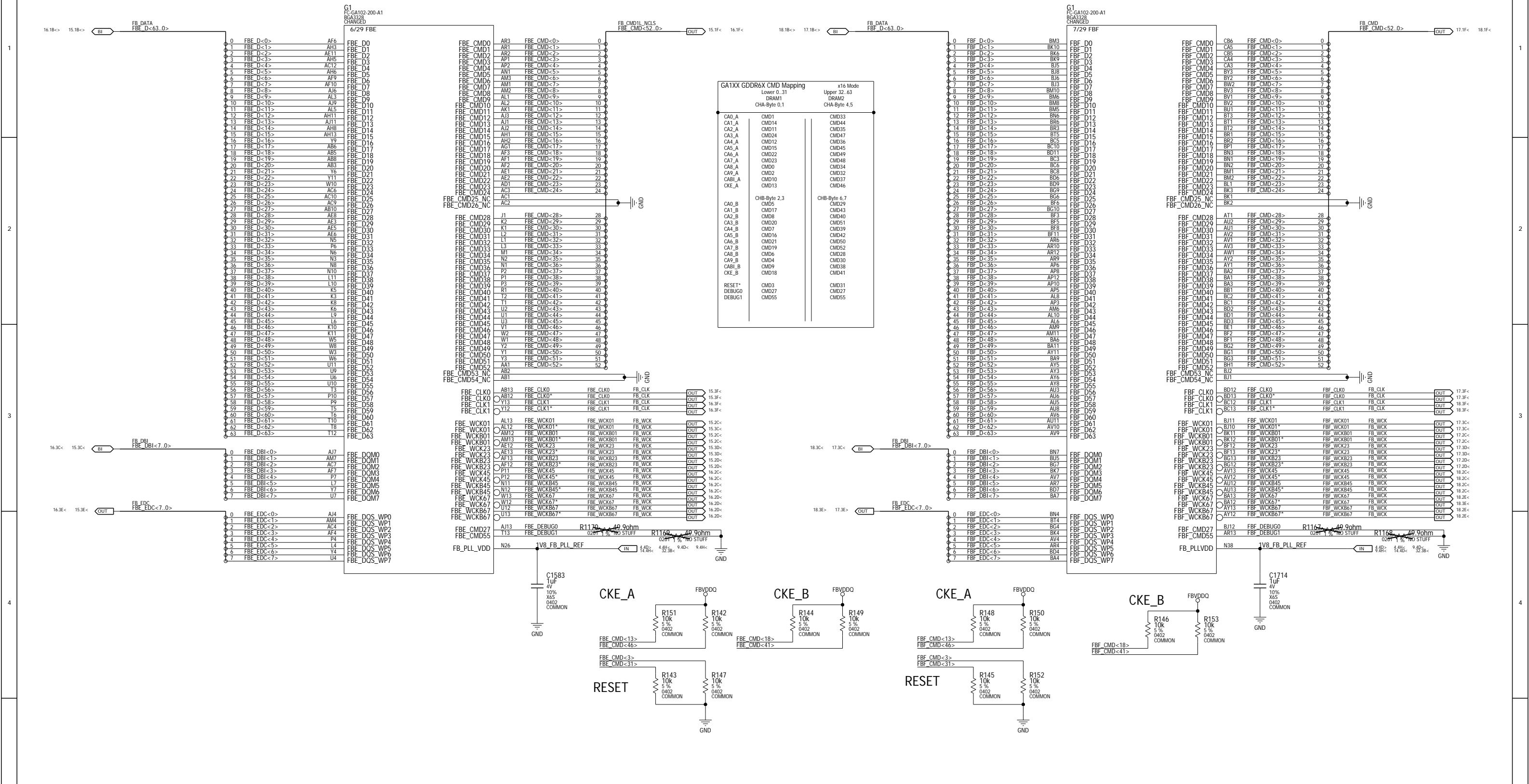
A

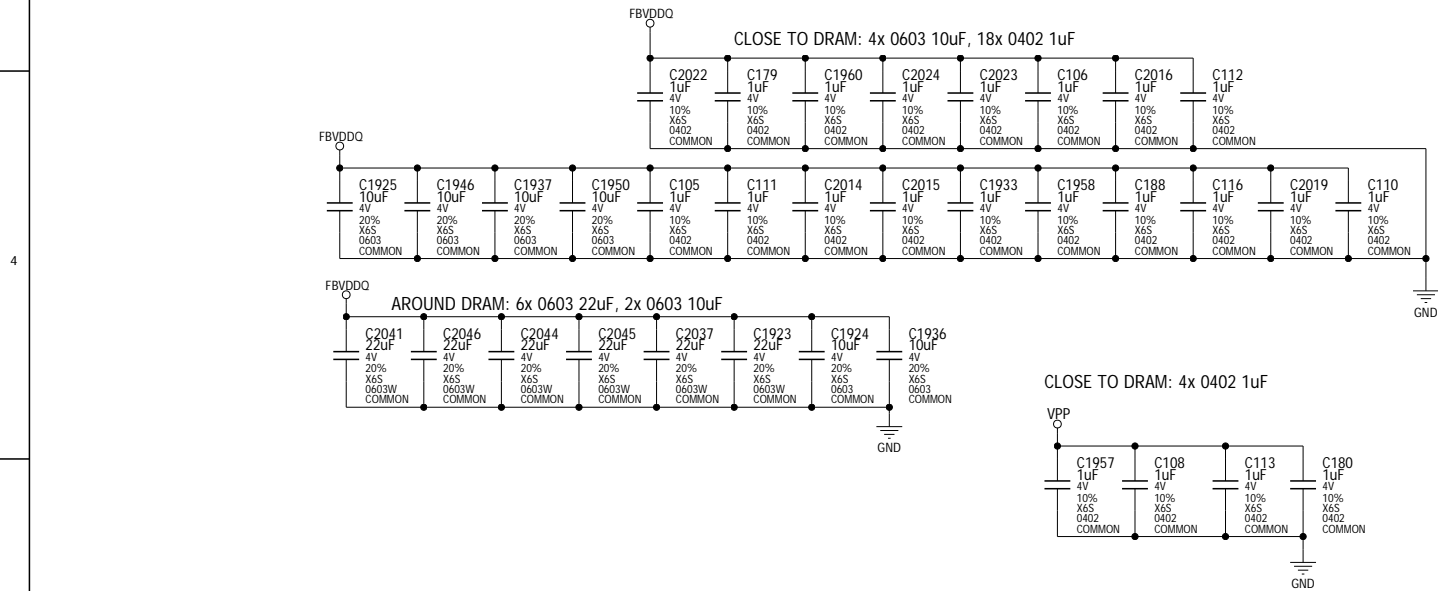
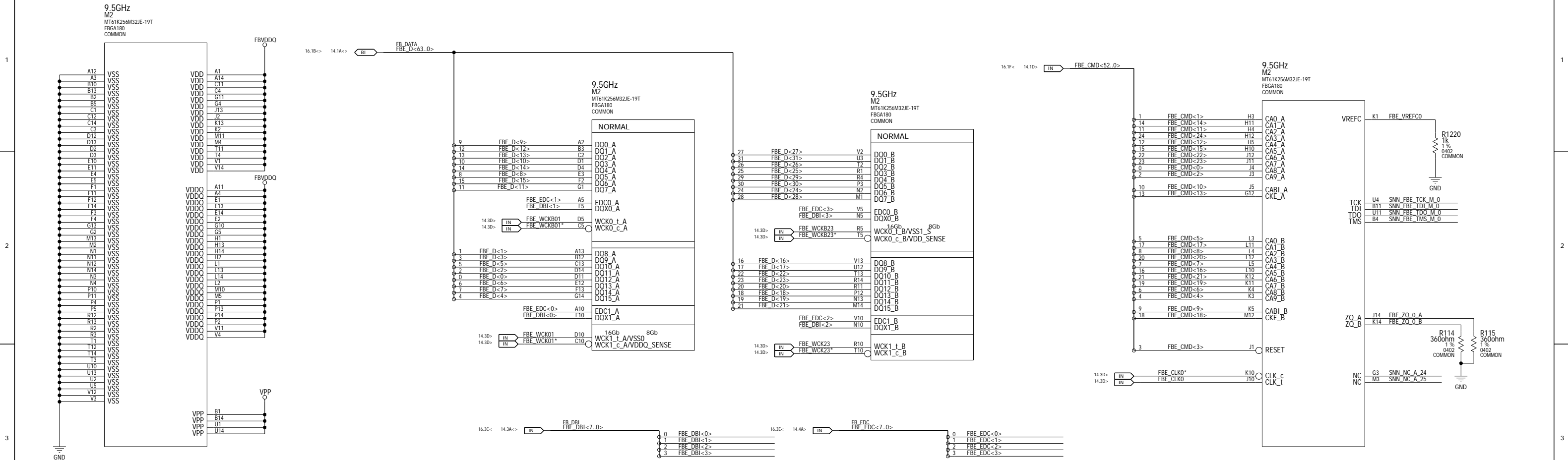
DATE

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ASSEMBLY	SKU30
PAGE DETAIL	MEMORY: FBD PARTITION[63:32]

## Page 14: MEMORY: GPU Partition E/F





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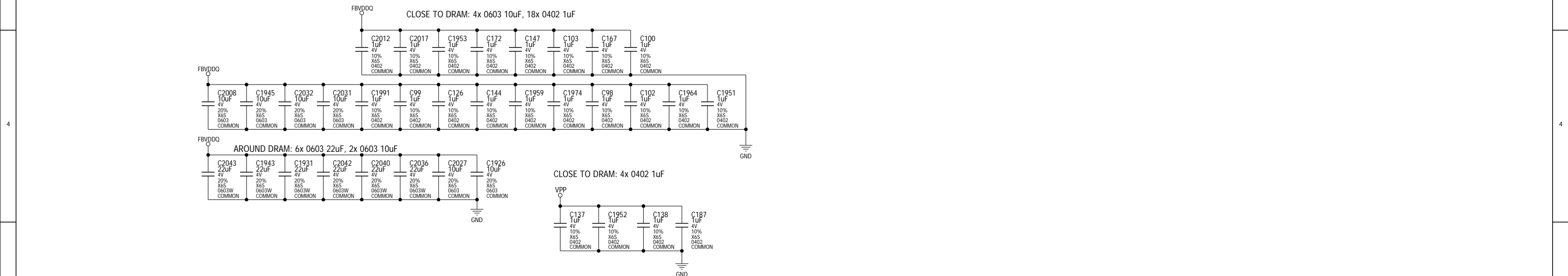
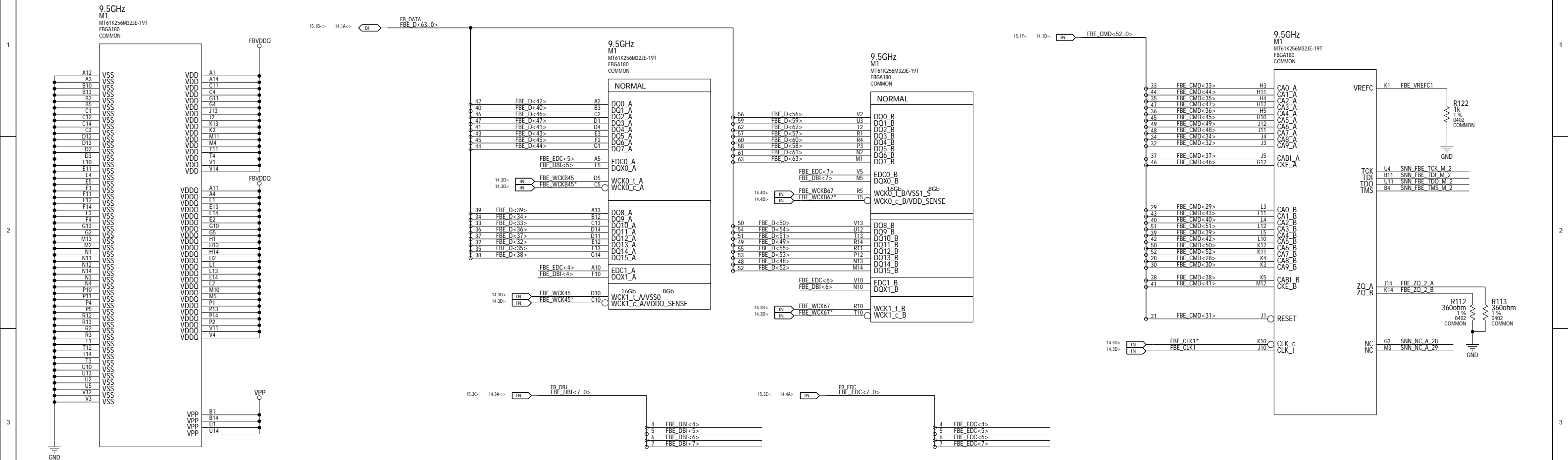
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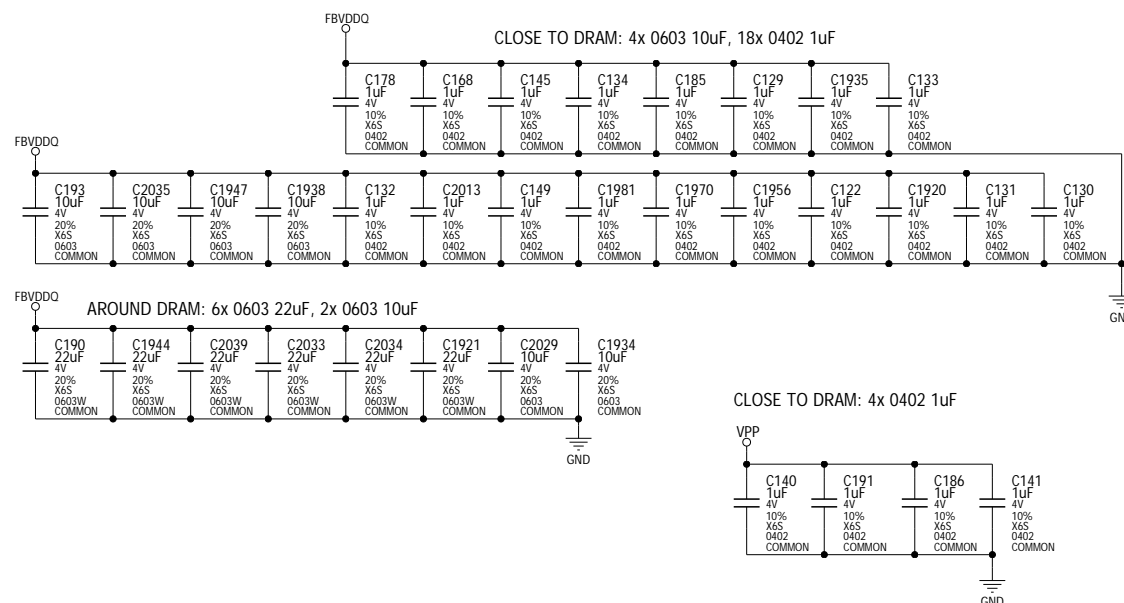
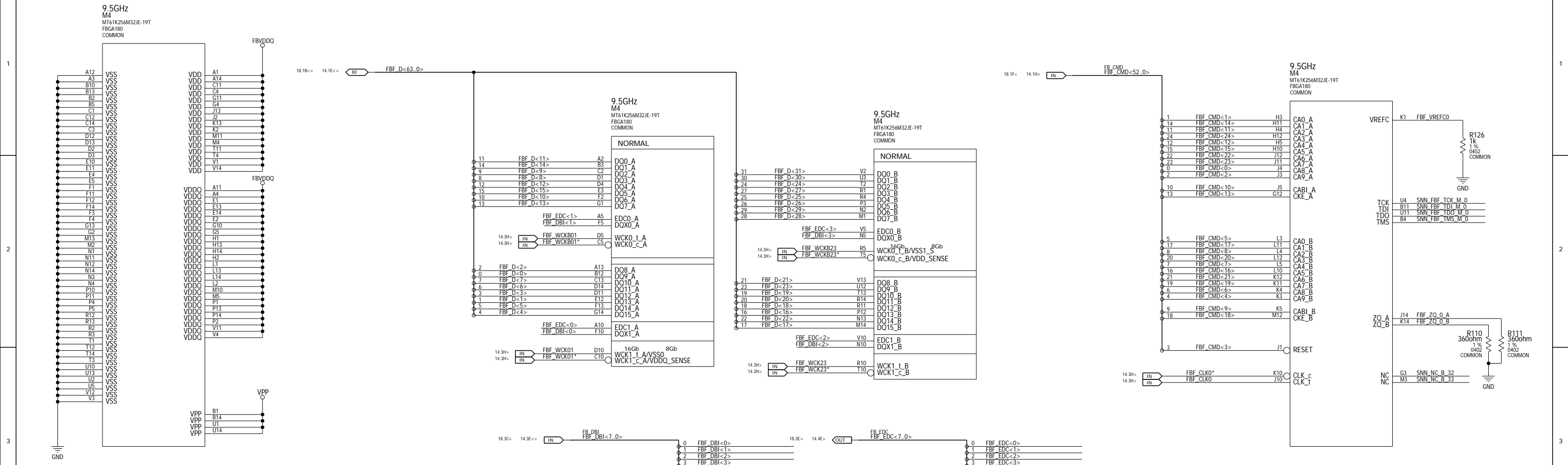
ASSEMBLY SKU30  
PAGE DETAIL MEMORY: FBE PARTITION[31:0]

## Page 16: MEMORY: FBE Partition 63..32

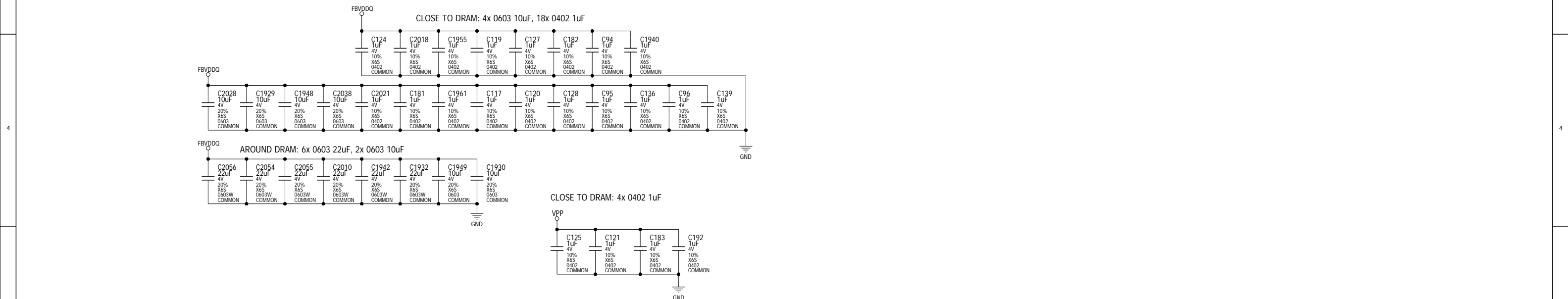
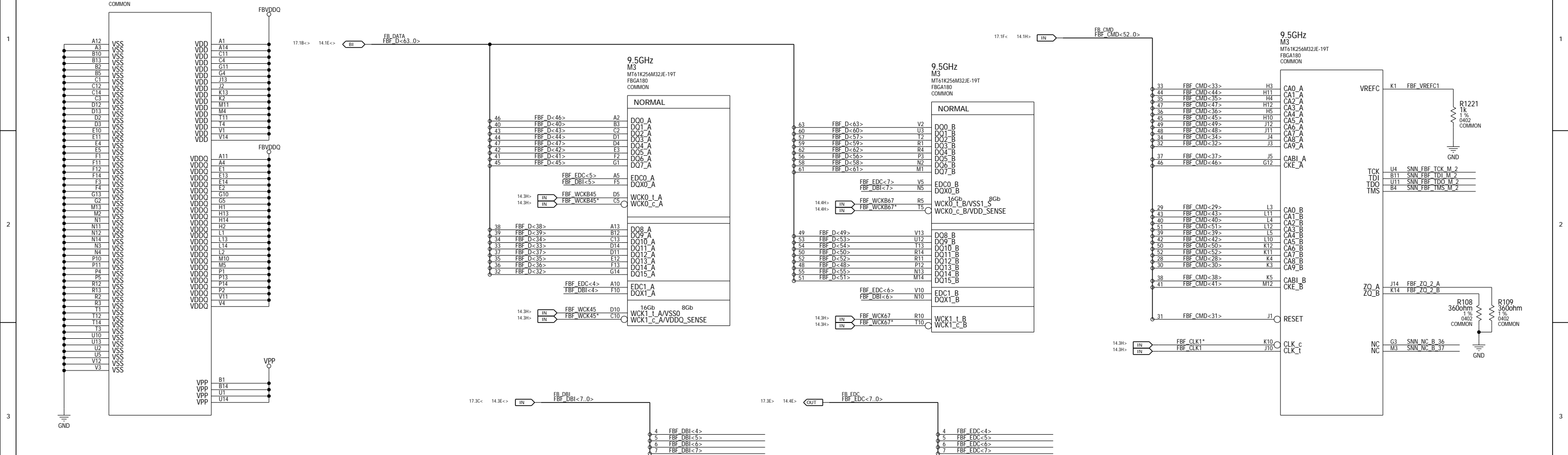





## Page 17: MEMORY: FBF Partition 31..0

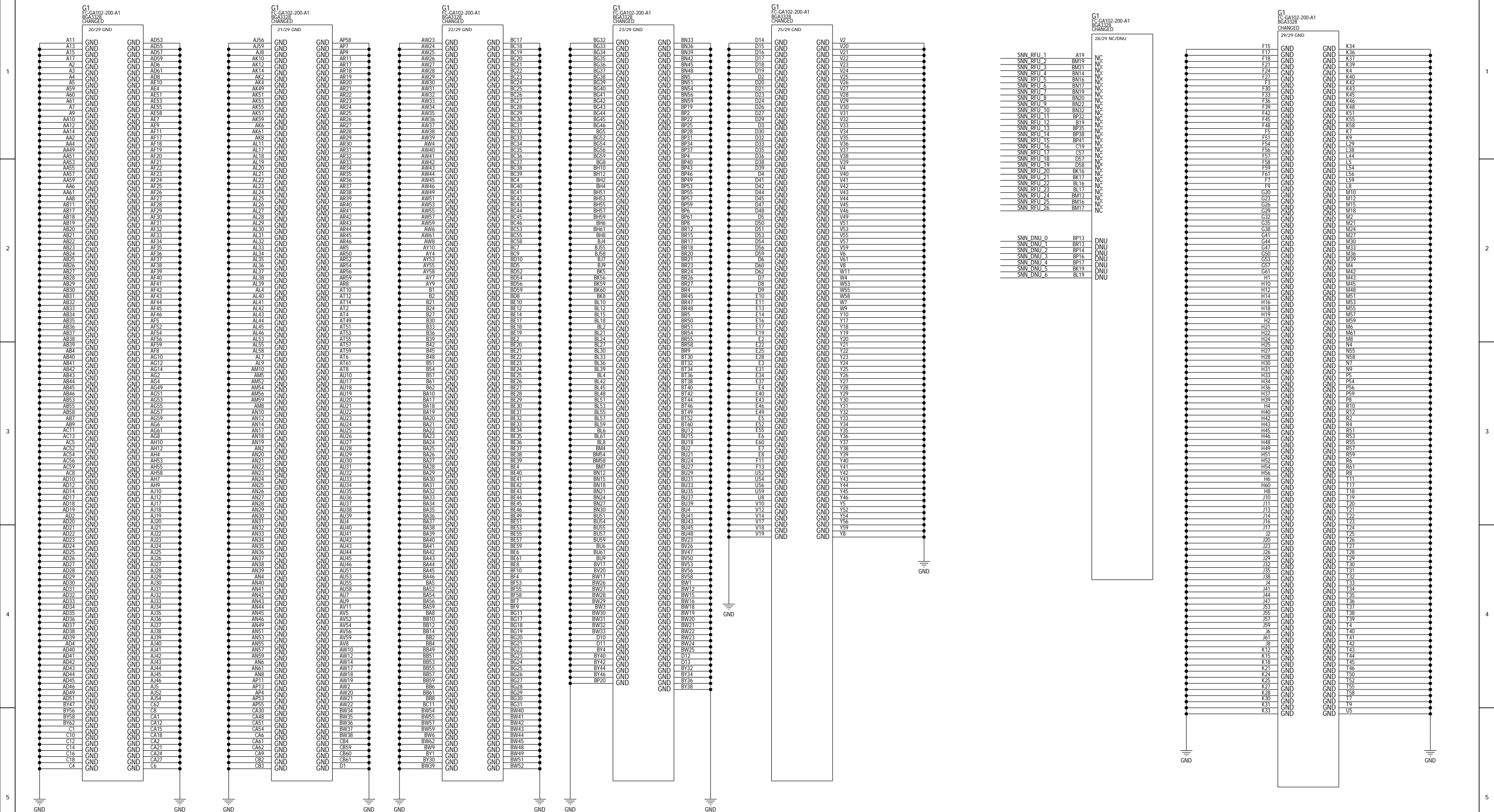


## Page 18: MEMORY: FBF Partition 63..32

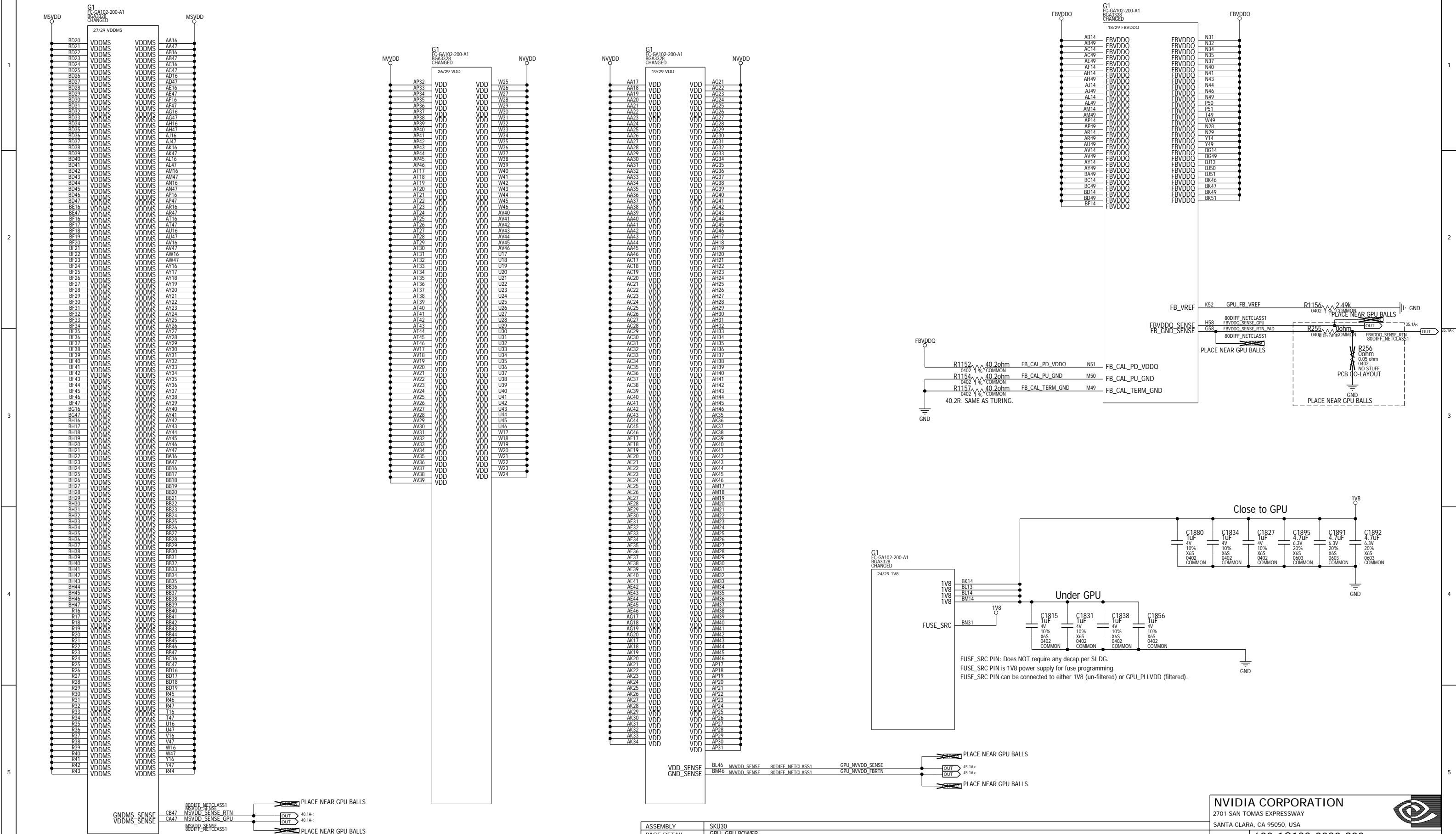


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## Page20: GPU POWER

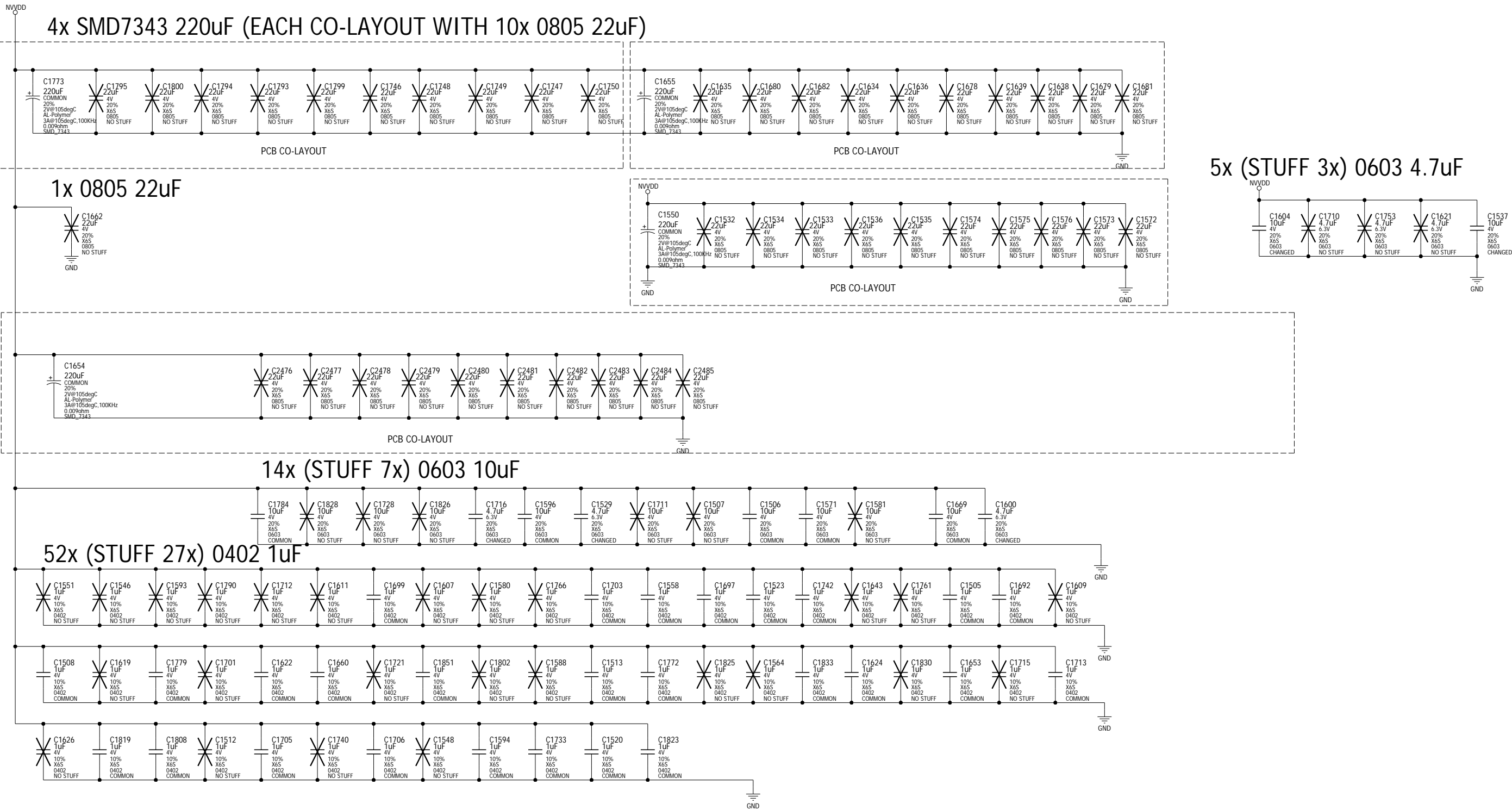


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ASSEMBLY	SKU30
PAGE DETAIL	GPU: GPU POWER

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NV_PN	600-1G133-0030-900		
PCB REV	PG133-A03	PAGE	20 OF 67
BOM REV	A	DATE	11-JUN-2020

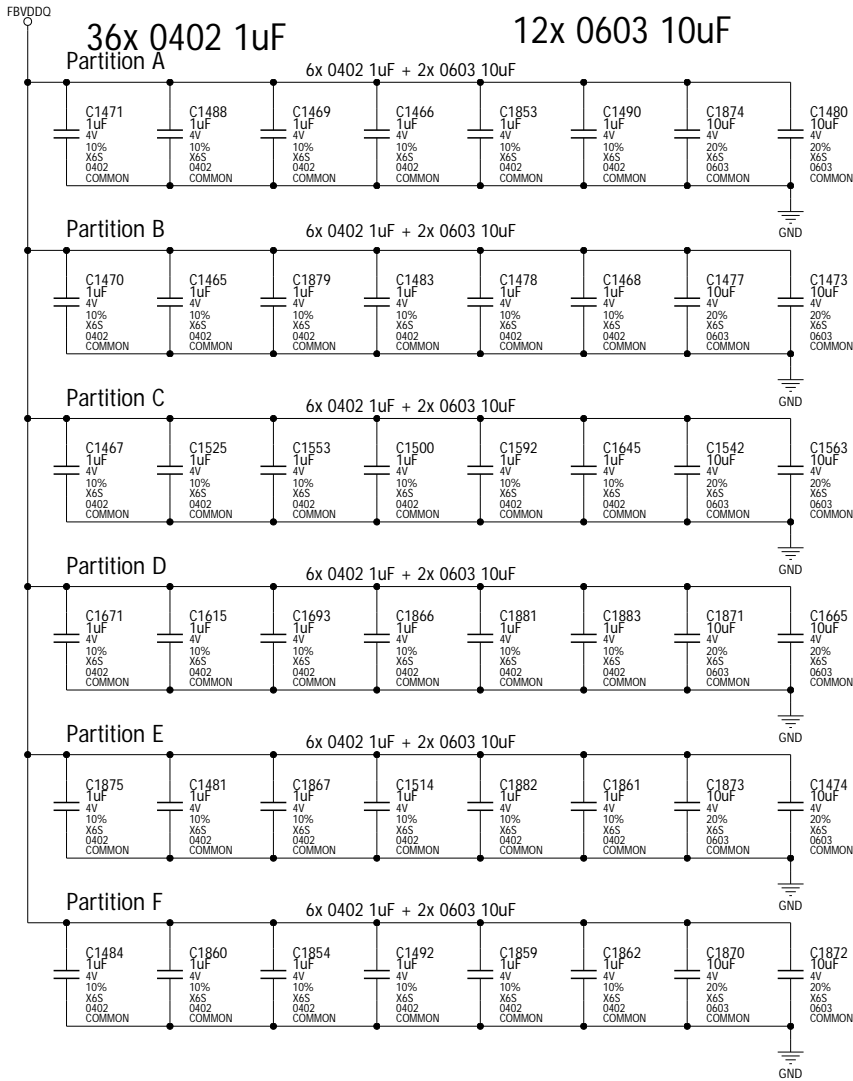
# NVVDD UNDER GPU



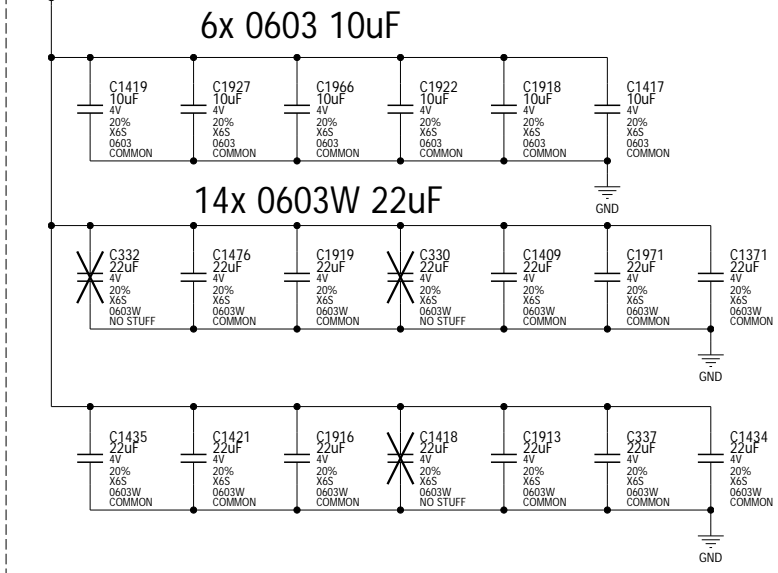
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FBVDDQ

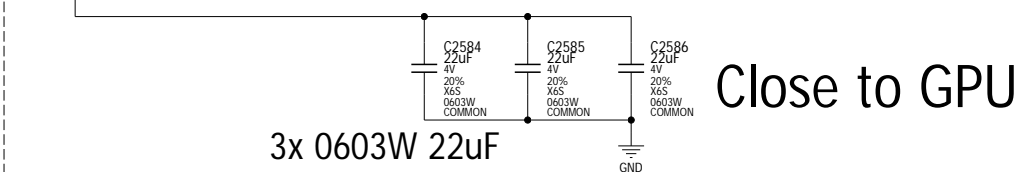
Under GPU



Close to GPU



Added for A00 x16



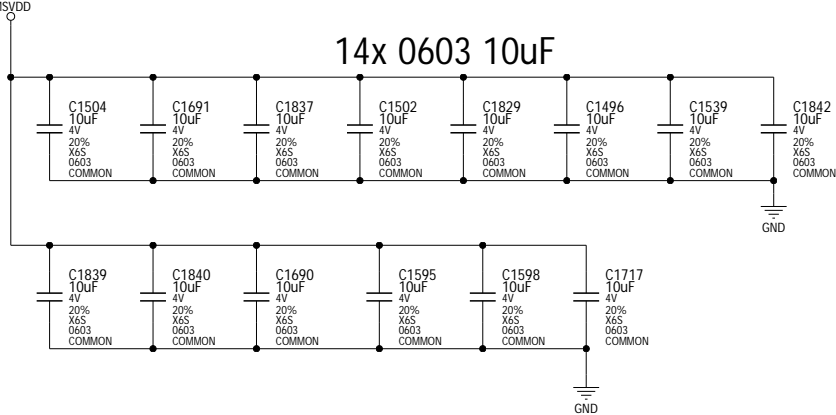
Close to GPU

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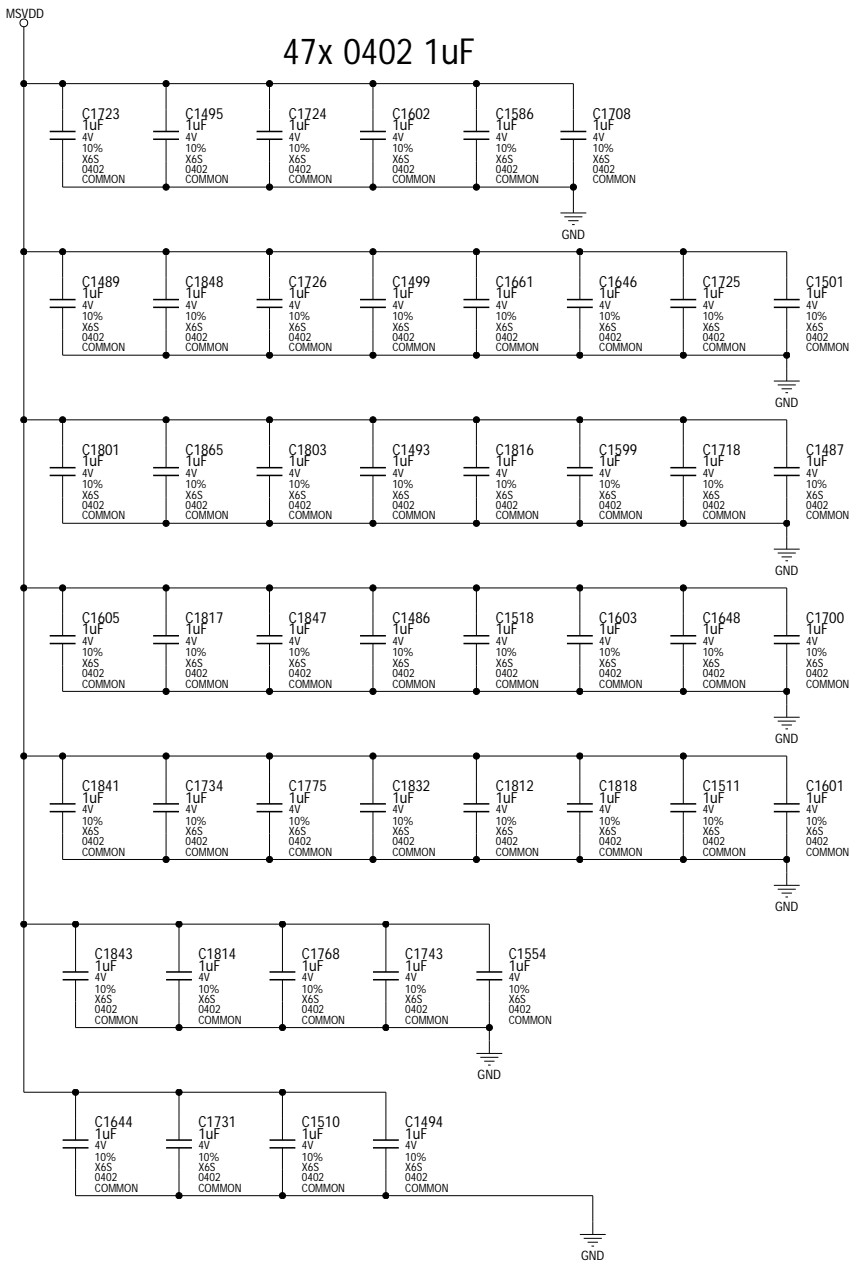
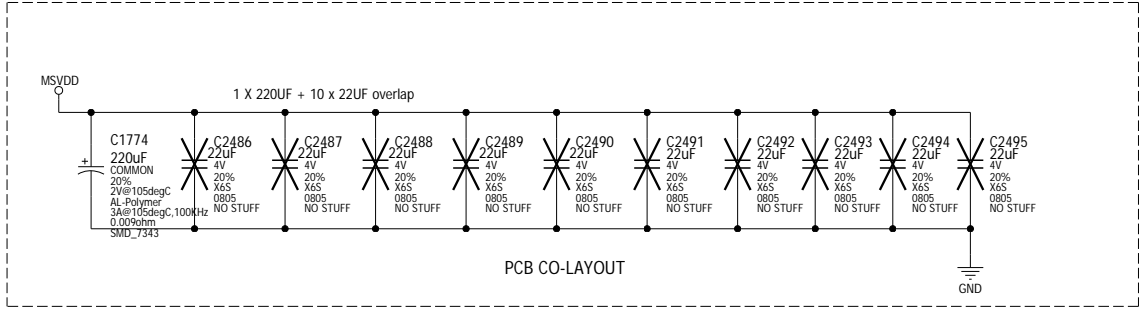
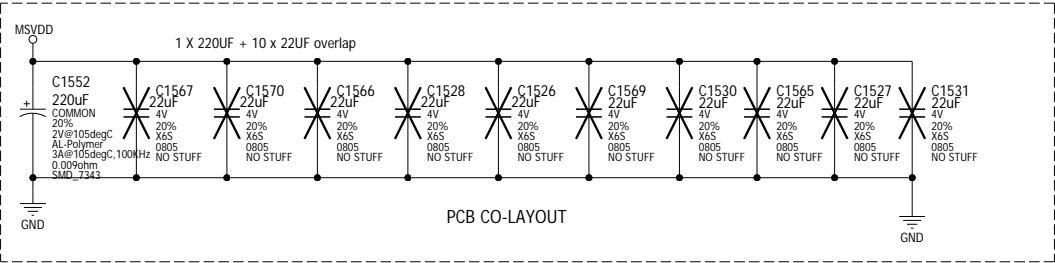
Page 23: GPU: MSVDD DECOUPLING

MSVDD

UNDER GPU



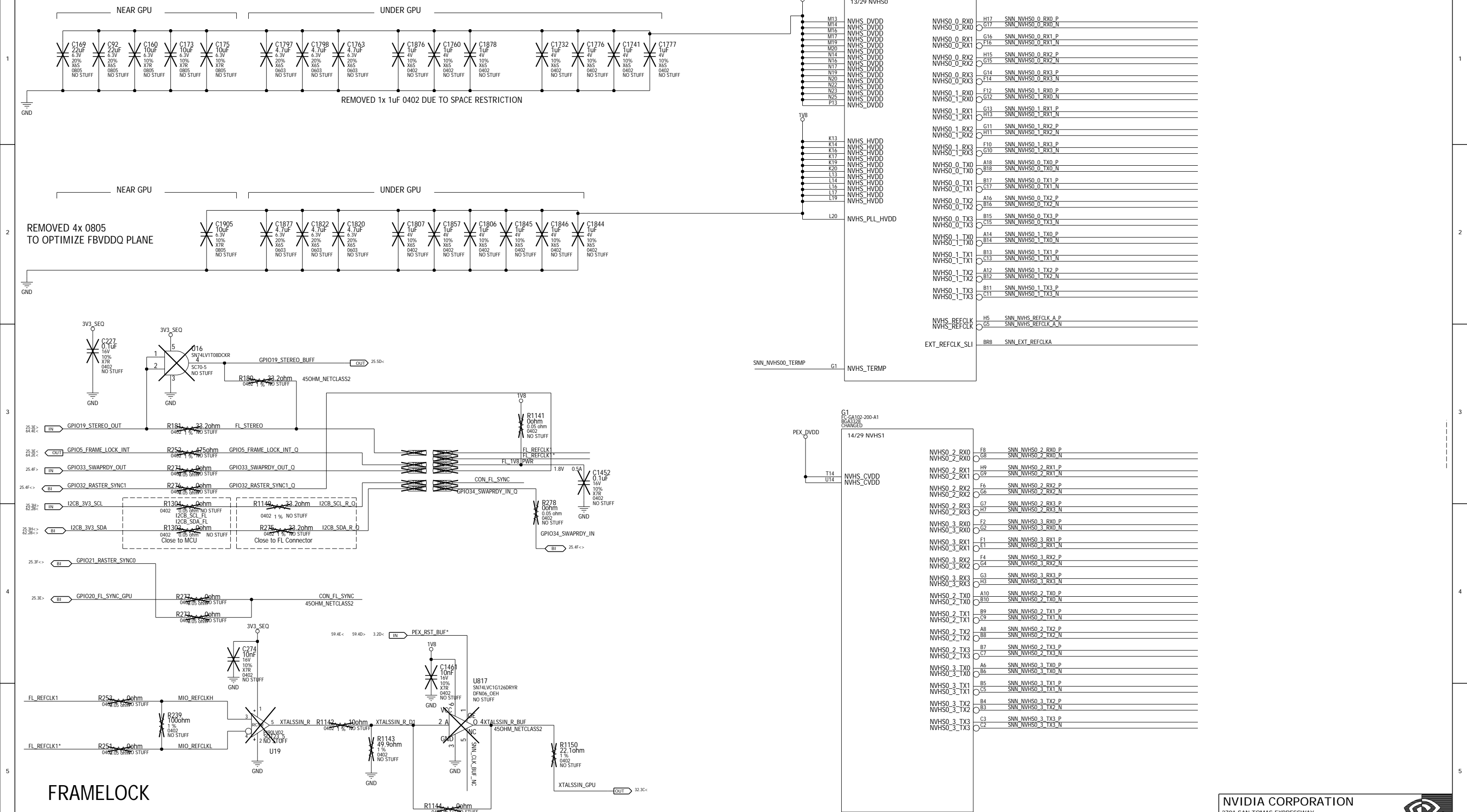
2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

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## Page 24: GPU: NVHS x16, FRAMELOCK



FRAMELOCK

ASSEMBLY	SKU30
PAGE DETAIL	GPU: NVHS x16, FRAMELOCK

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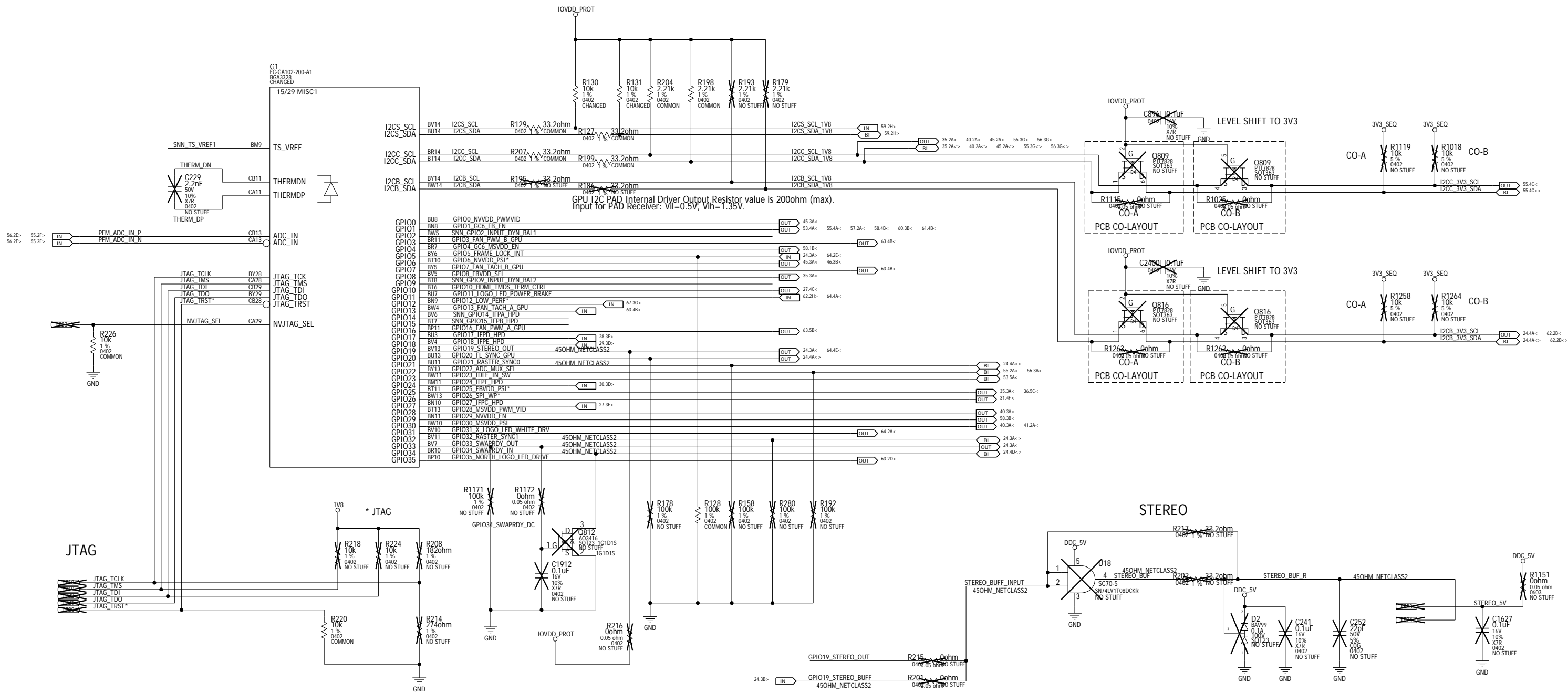
NV PN	600-1G133-0030-900
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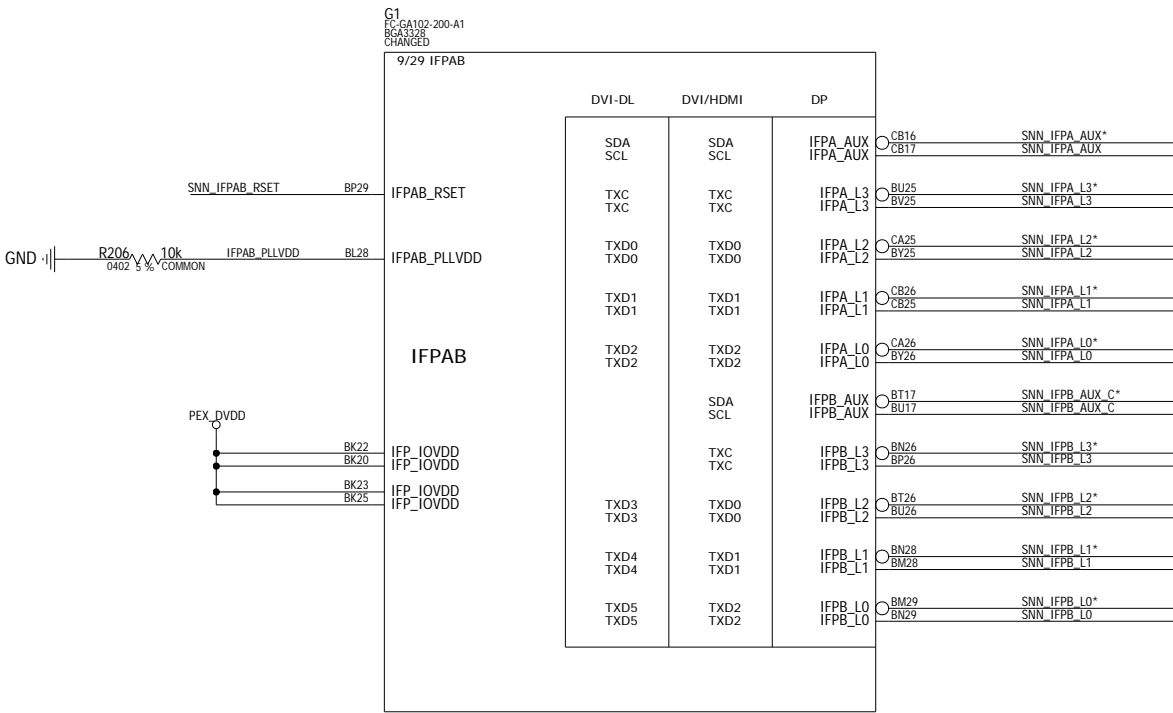
PCB REV	PG133-A03	PAGE	24 OF 67
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REMOVED CYA FUSE\_SRC LOAD SWITCH.







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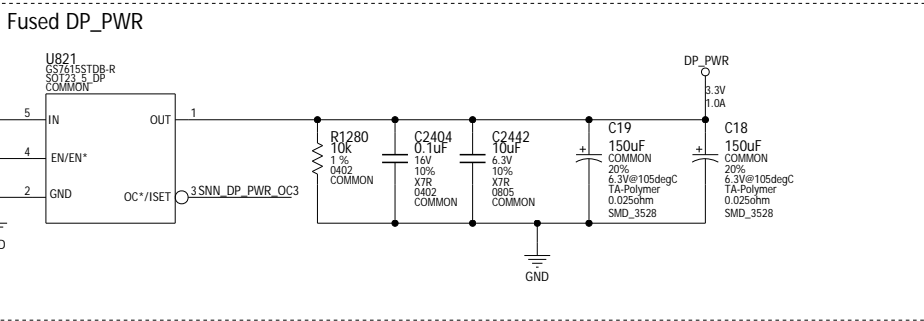
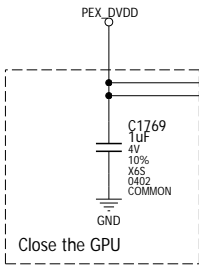
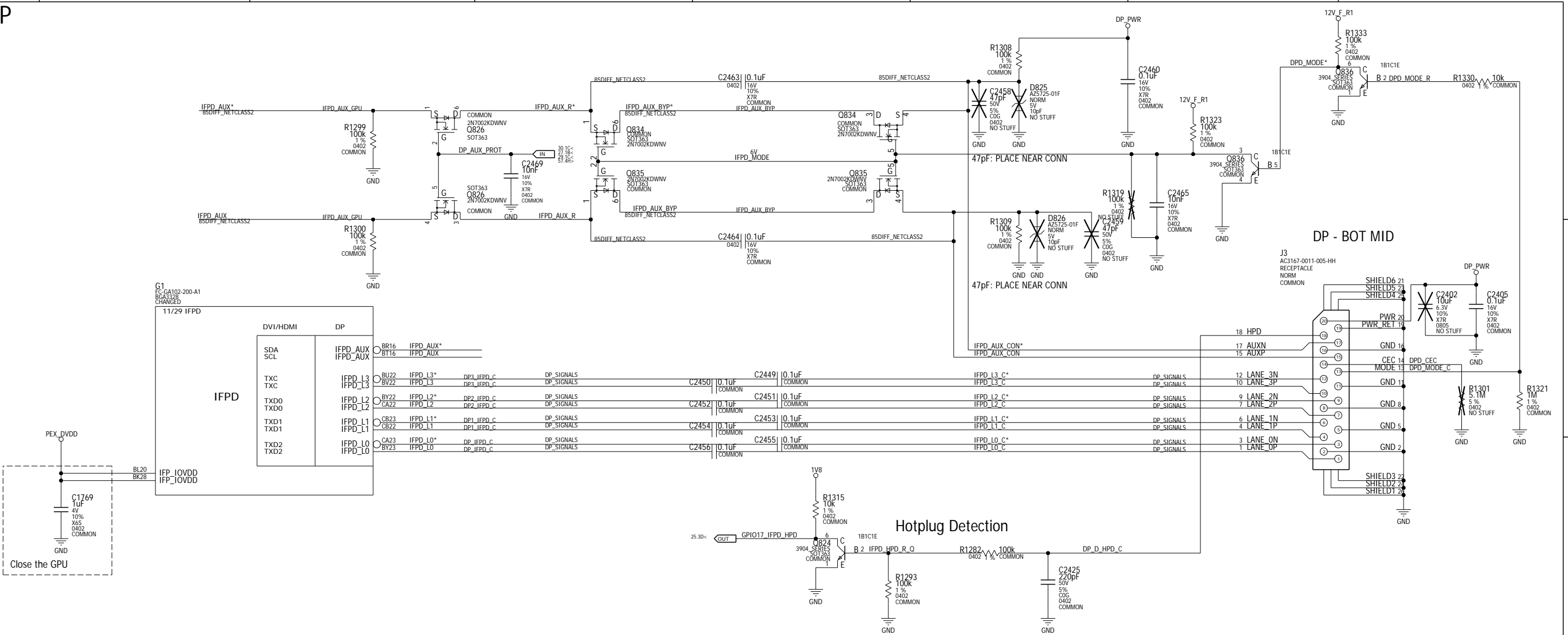
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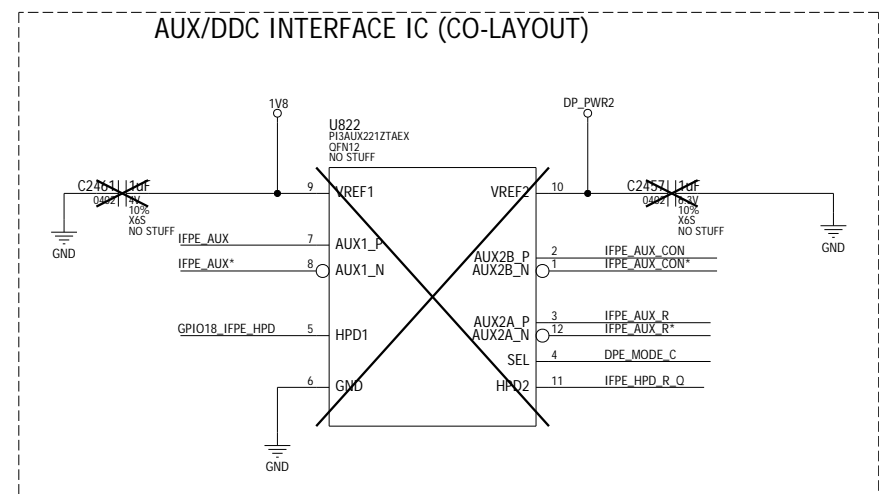
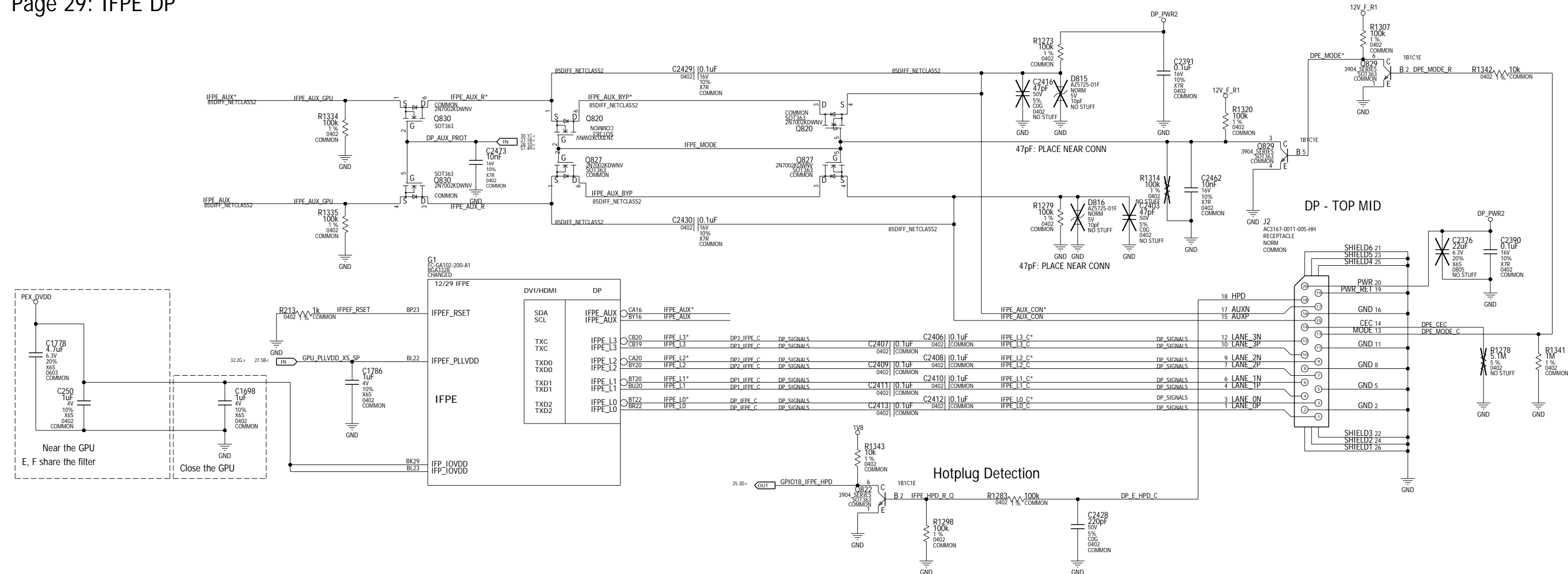
PCB REV	PG133 A03	
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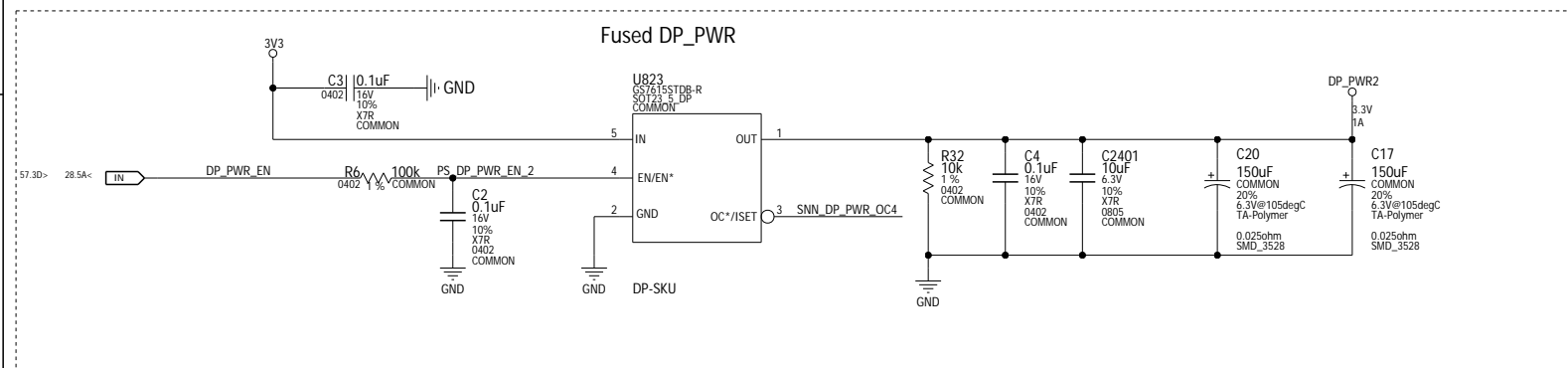
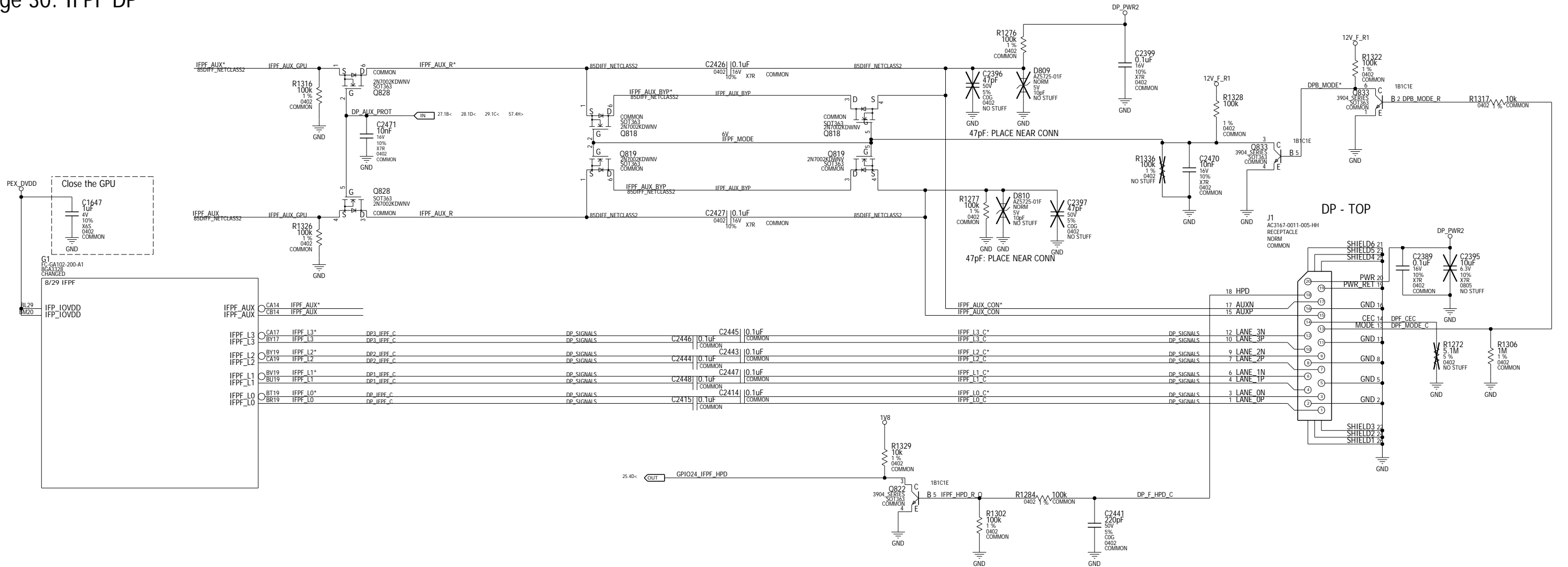
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ASSEMBLY	SKU30
PAGE DETAIL	IFPF DR

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Page 31: MISC: ROM, Straps

GROUP0 STRAP2	STRAP1	STRAPO	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
M	H	L	01110	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

<-A01 PCB

<-OLD

<-DISMISSED

<-LATEST A02/A03 PCB

GROUP1 ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	M	L	1001	FAN0/1=33%/33%, FS_OVERT ENABLE
H	H	H	0111	FAN0/1=66%/66%, FS_OVERT ENABLE

<-DEFAULT

GROUP2 STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

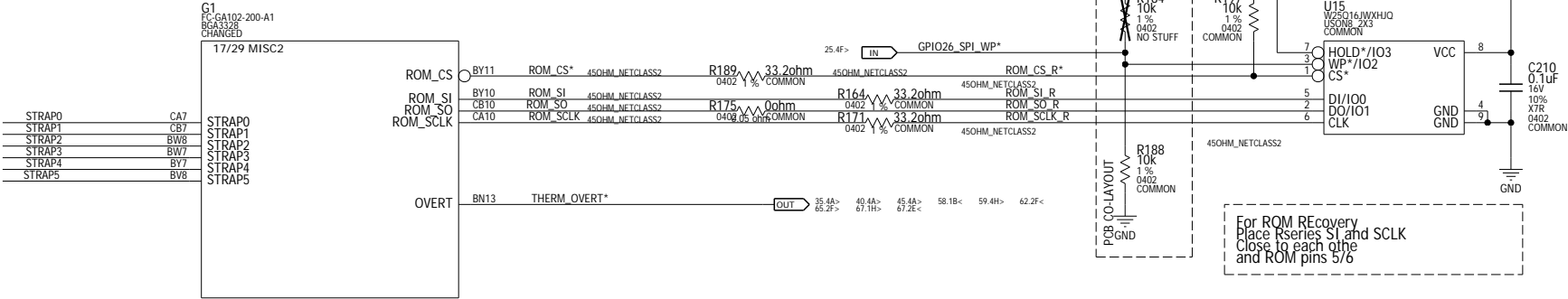
1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE

1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER

1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

<-Default



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NV\_PN 600-1G133-0030-900

PCB REV PG133-A03

BOM REV A

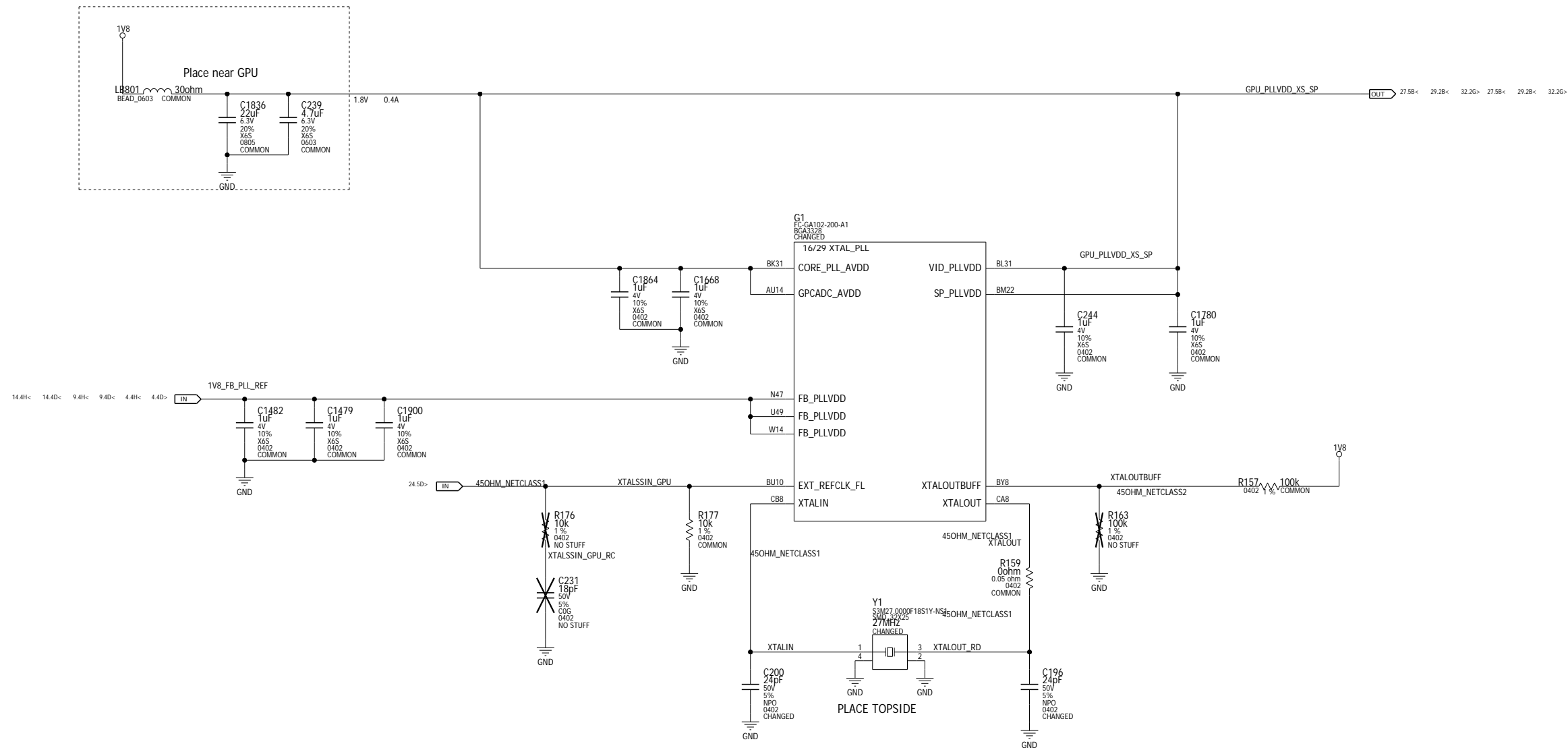
PAGE

DATE 11-JUN-2020

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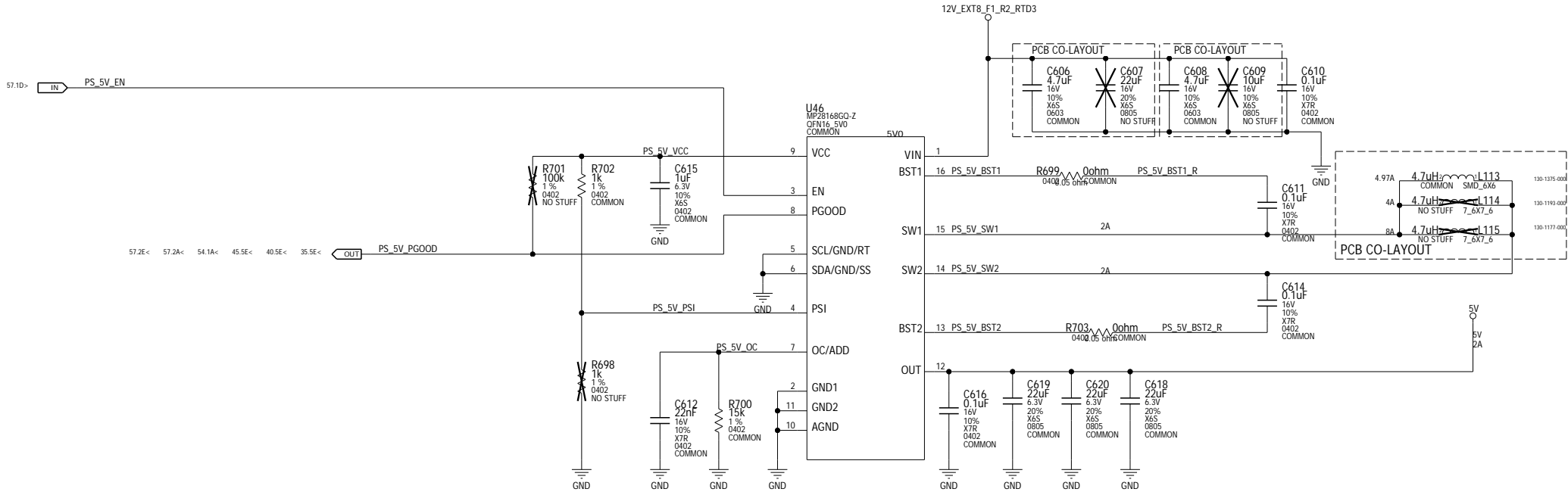
## Page 32: MISC: XTAL. PLL



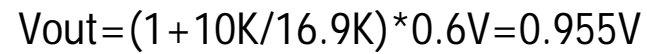
<b>NVIDIA CORPORATION</b> 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
<b>NV_PN</b> 600-1G133-0030-900			
PCB REV	P133-A03	PAGE	32 OF 67
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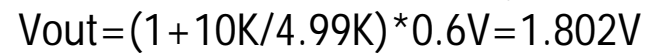





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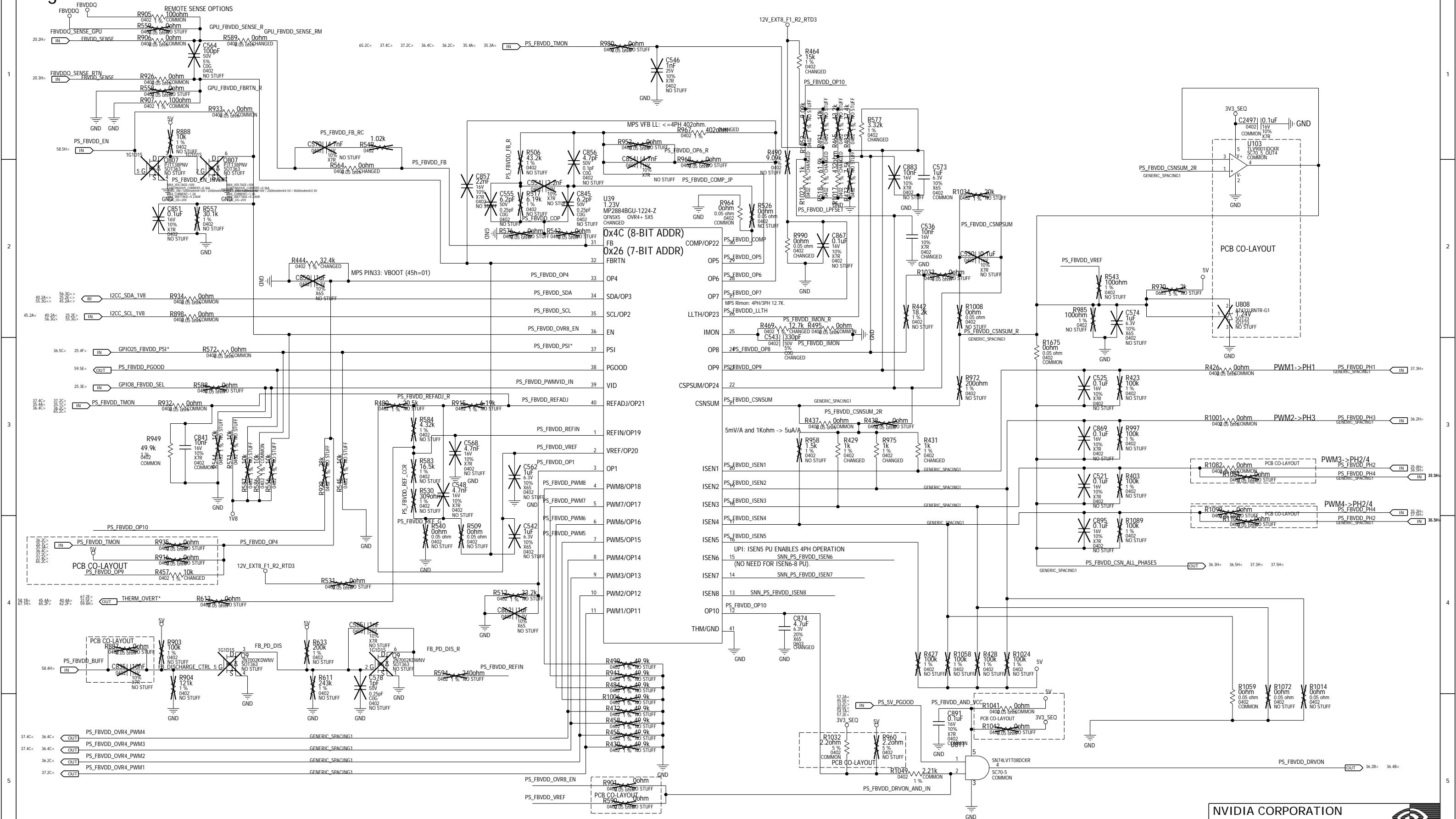
1V8



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<b>NV_PN</b>		<b>600-1G133-0030-900</b>		
<b>PCB REV</b>		<b>PG133-A03</b>		<b>PAGE</b> 34 OF 67
<b>BOM REV</b>		<b>A</b>		<b>DATE</b> 11-JUN-2020

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## Page 35: PS: FBVDD Controller



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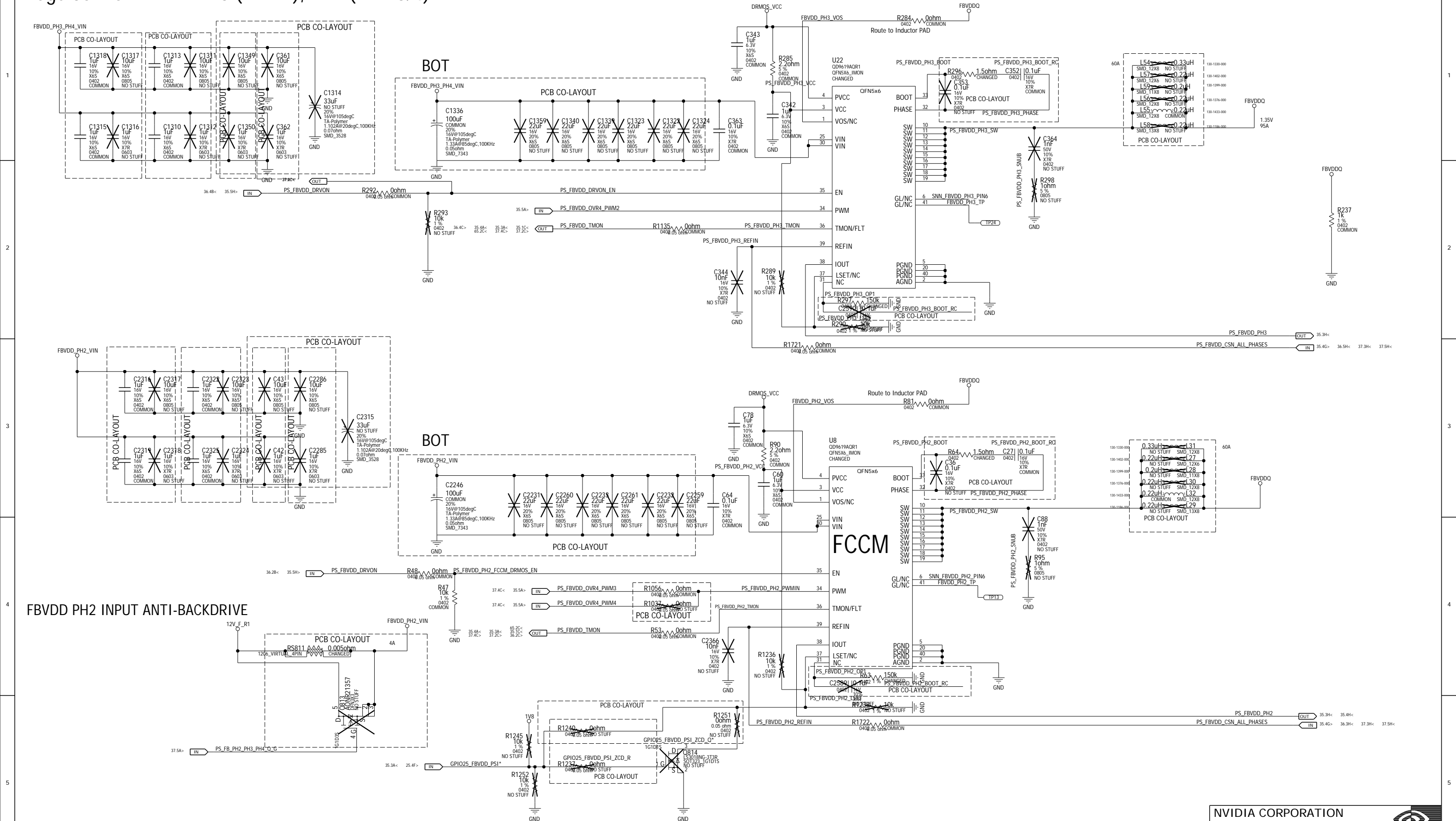


NV_PN	600-1G133-0030-900
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BOM REV	A	DATE	11-JUN-2020

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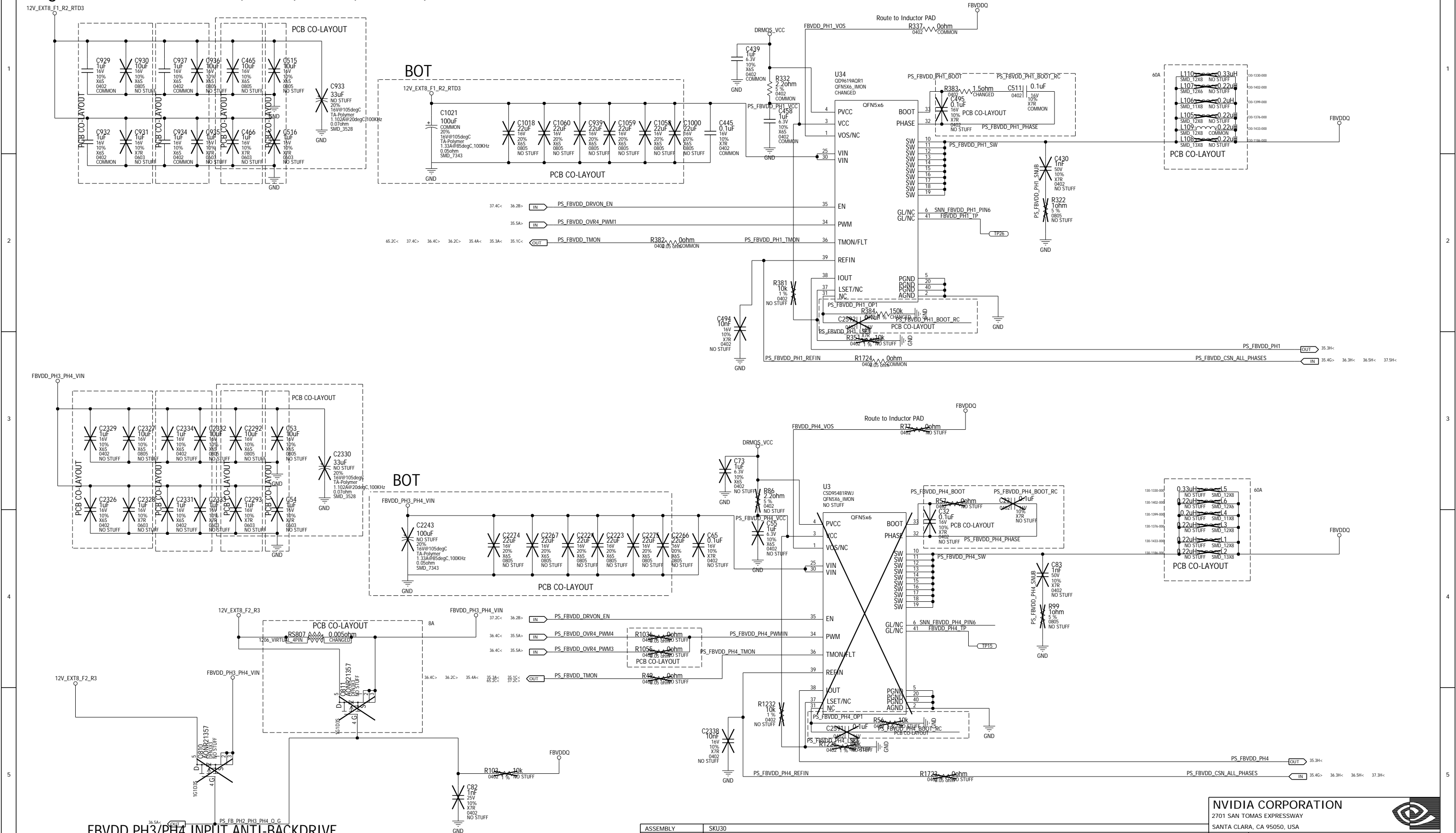
Page 36: PS: FBVDD PH3 (PWM2), PH2 (PWM3/4)



FBVDD PH2 INPUT ANTI-BACKDRIVE


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## Page 37: PS: FBVDD PH1 (PWM1), PH4 (PWM3/4)

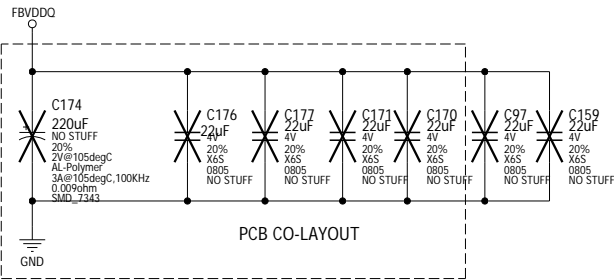


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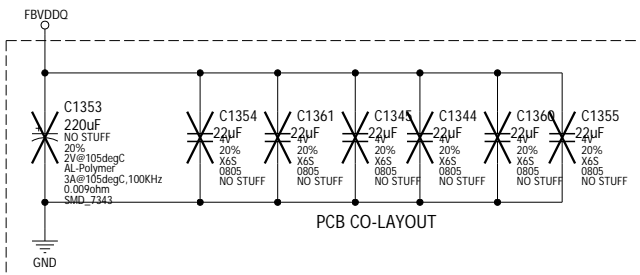
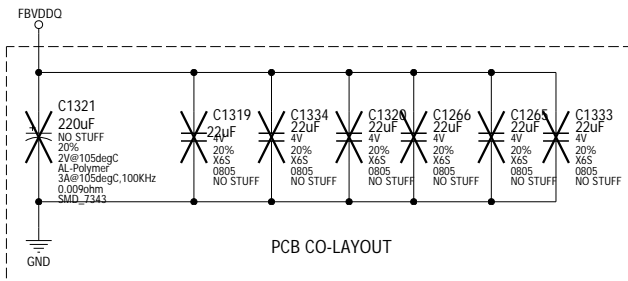
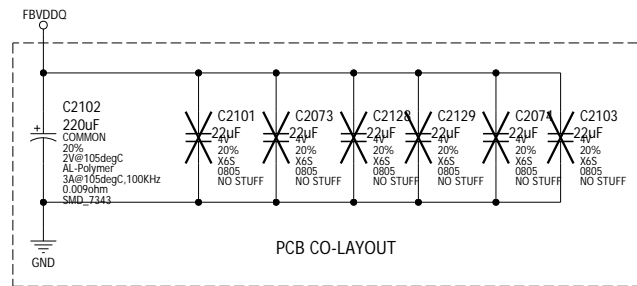
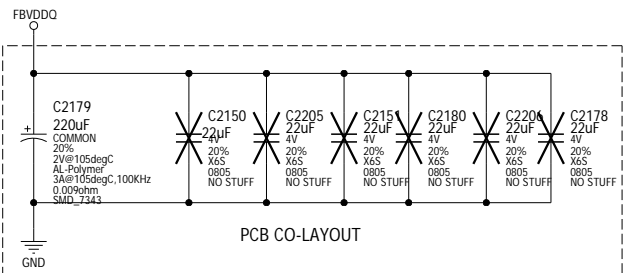
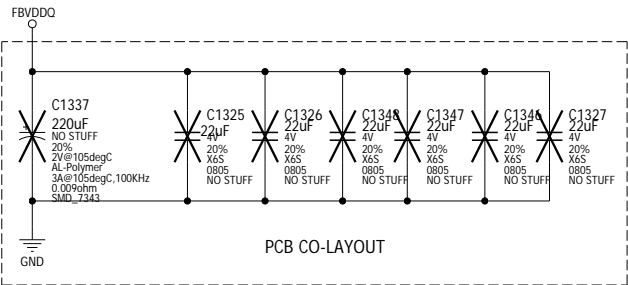
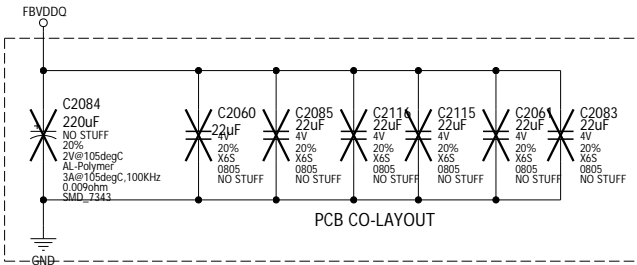
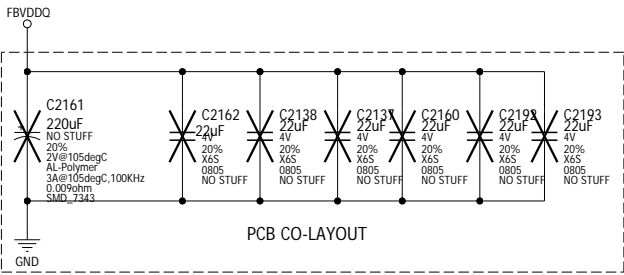
ASSEMBLY	SKU30
PAGE DETAIL	PS: FBVDD PH1 (PWM1 ) and PH4 (PWM3/4 )

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<b>INV_PN</b> PCB REV BOM REV	<b>600-1G133-0030-900</b> PG133-A03 A		<b>PAGE</b> <b>DATE</b> 37 OF 67 11-JUN-2020

PLACE NEAR POWER SUPPLY  
8x SMD7343 330uF CO-LAYOUT WITH 48x 0805 22uF



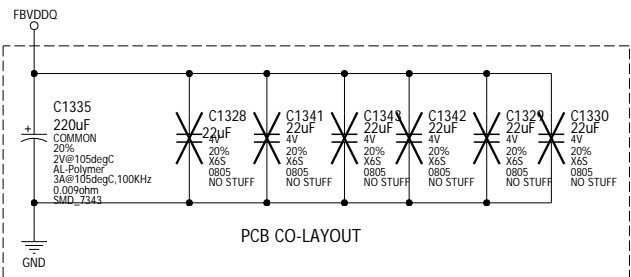
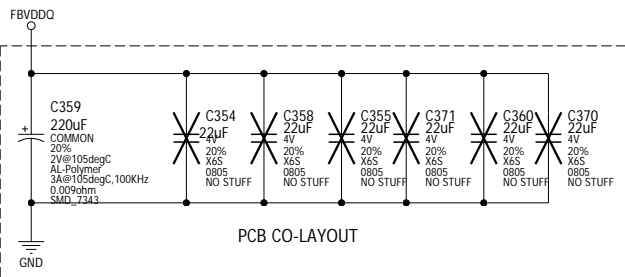
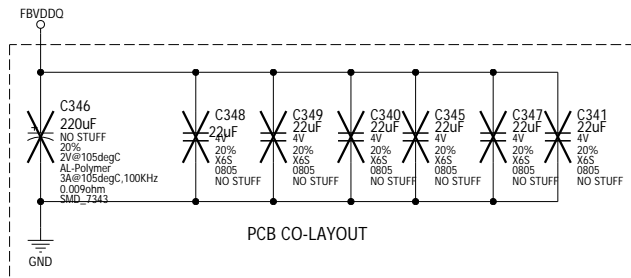
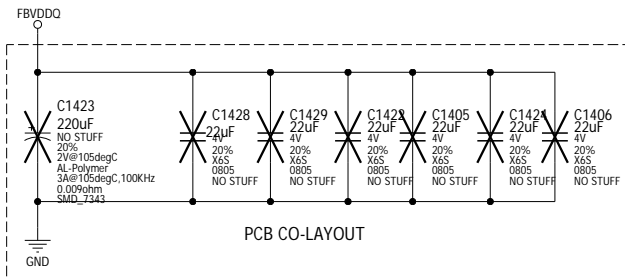
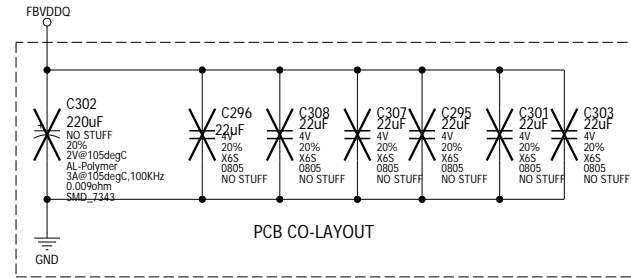
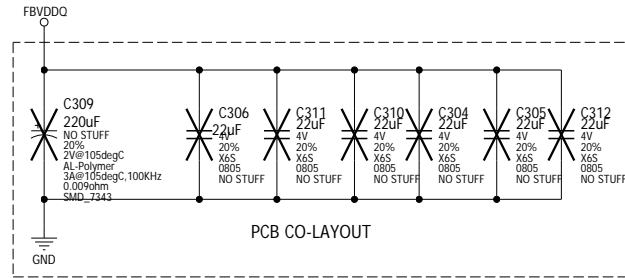
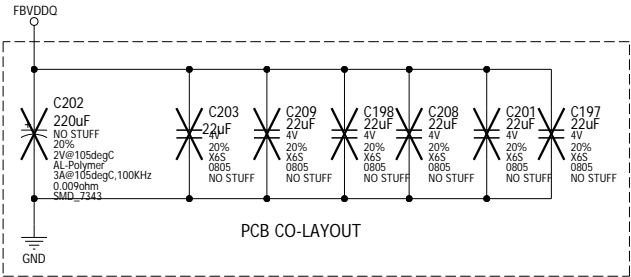
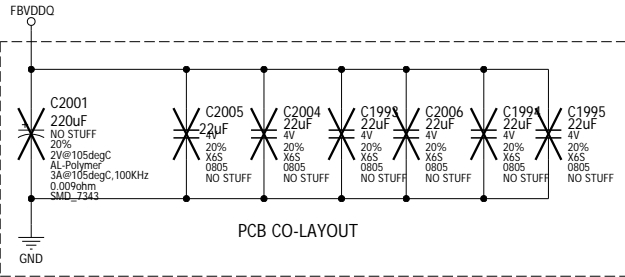
TOP WEST OF PCB



BACK EAST OF PCB

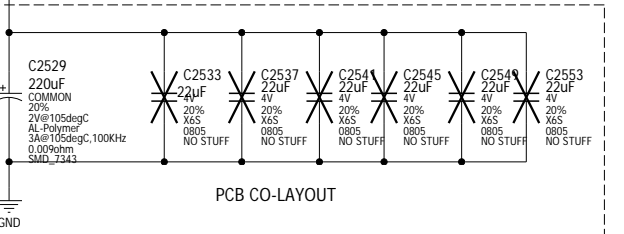
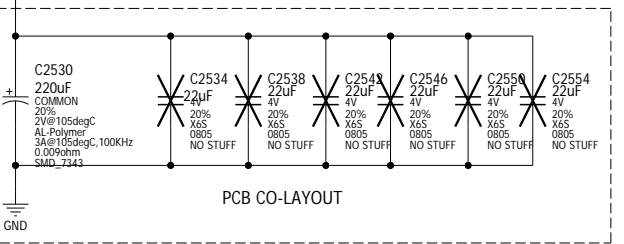
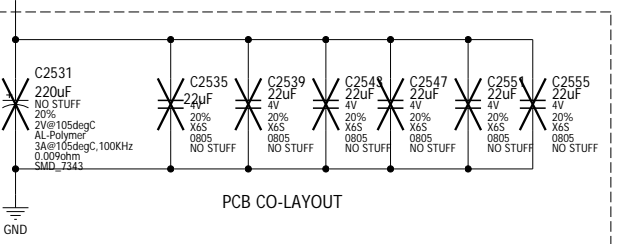
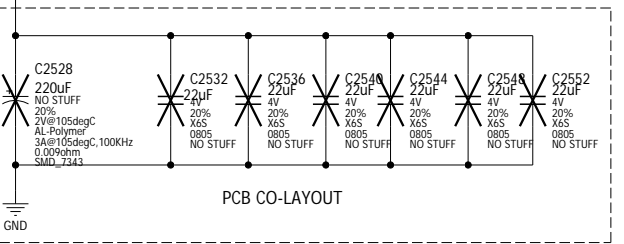
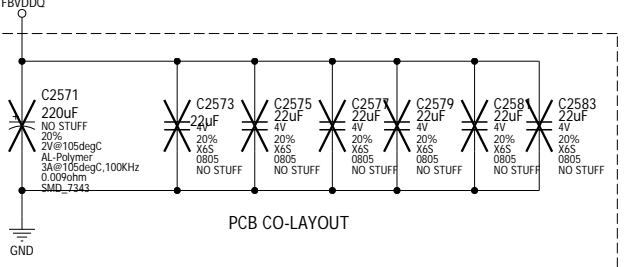
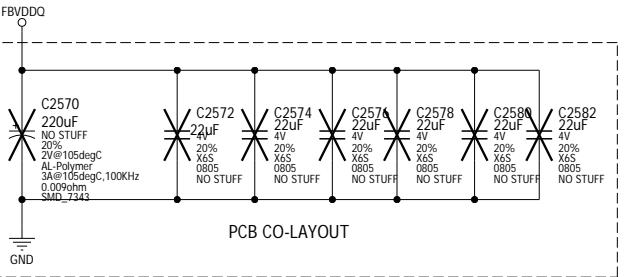
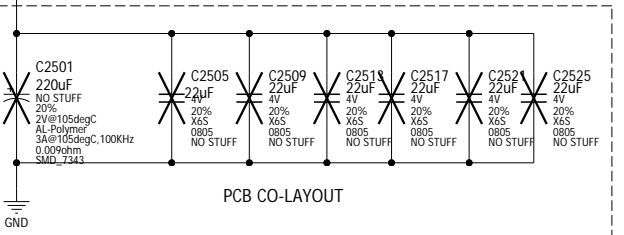
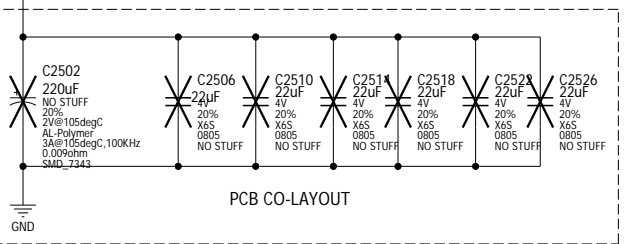
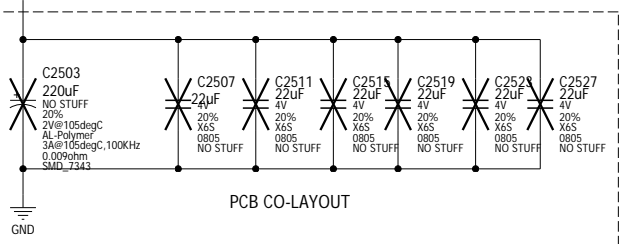
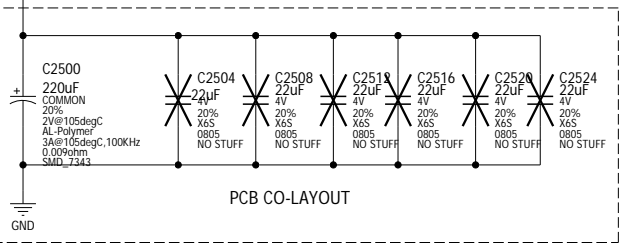
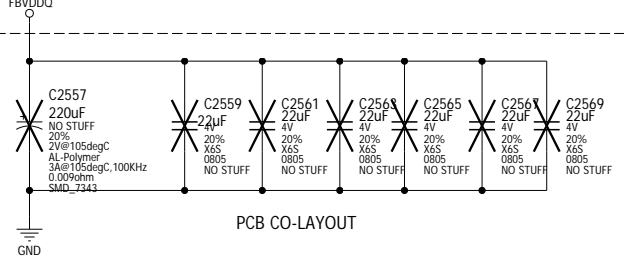
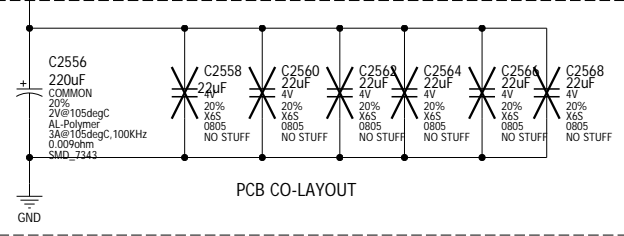
BACK WEST OF PCB

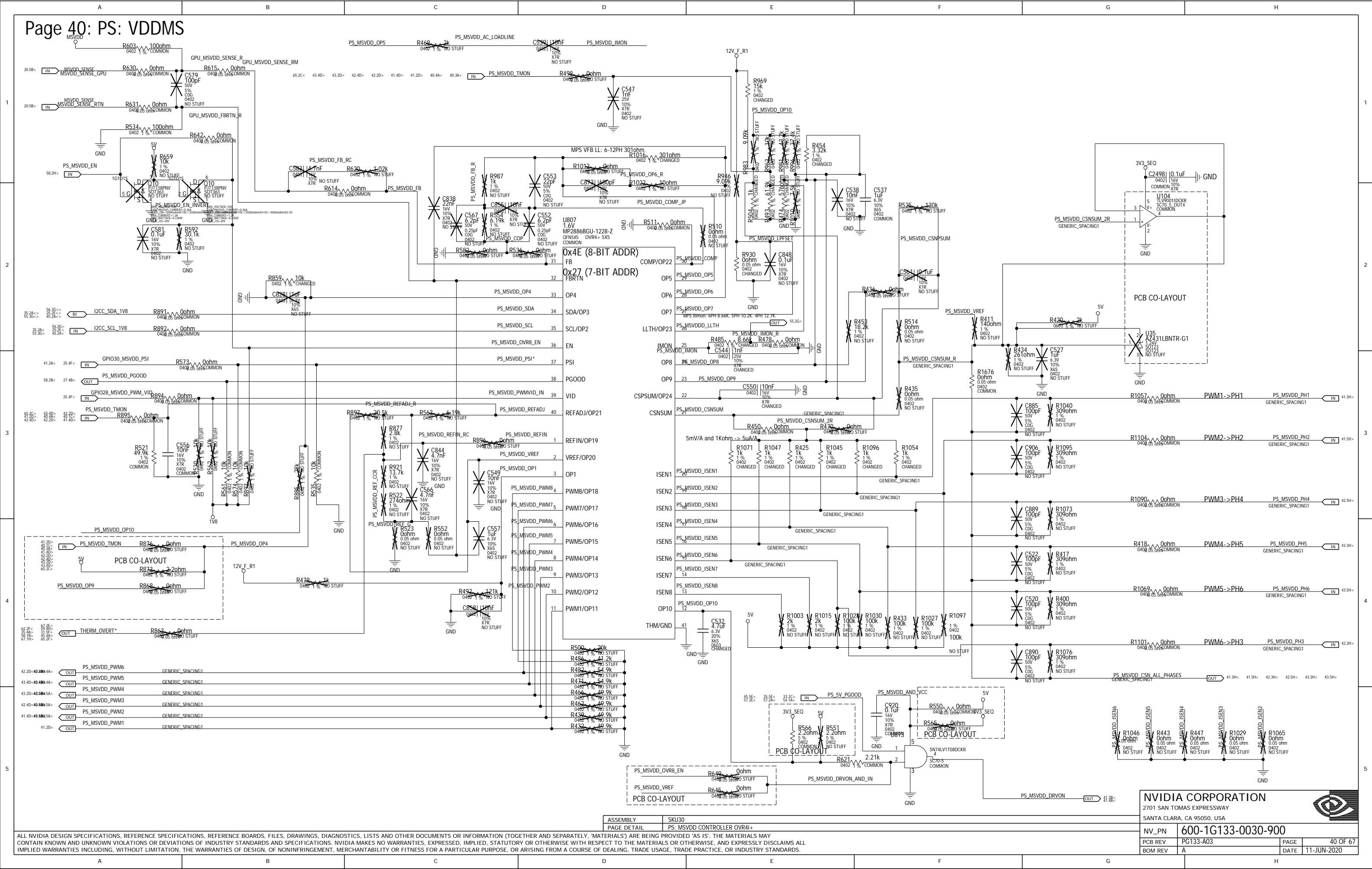
PLACE NEAR MEMORY



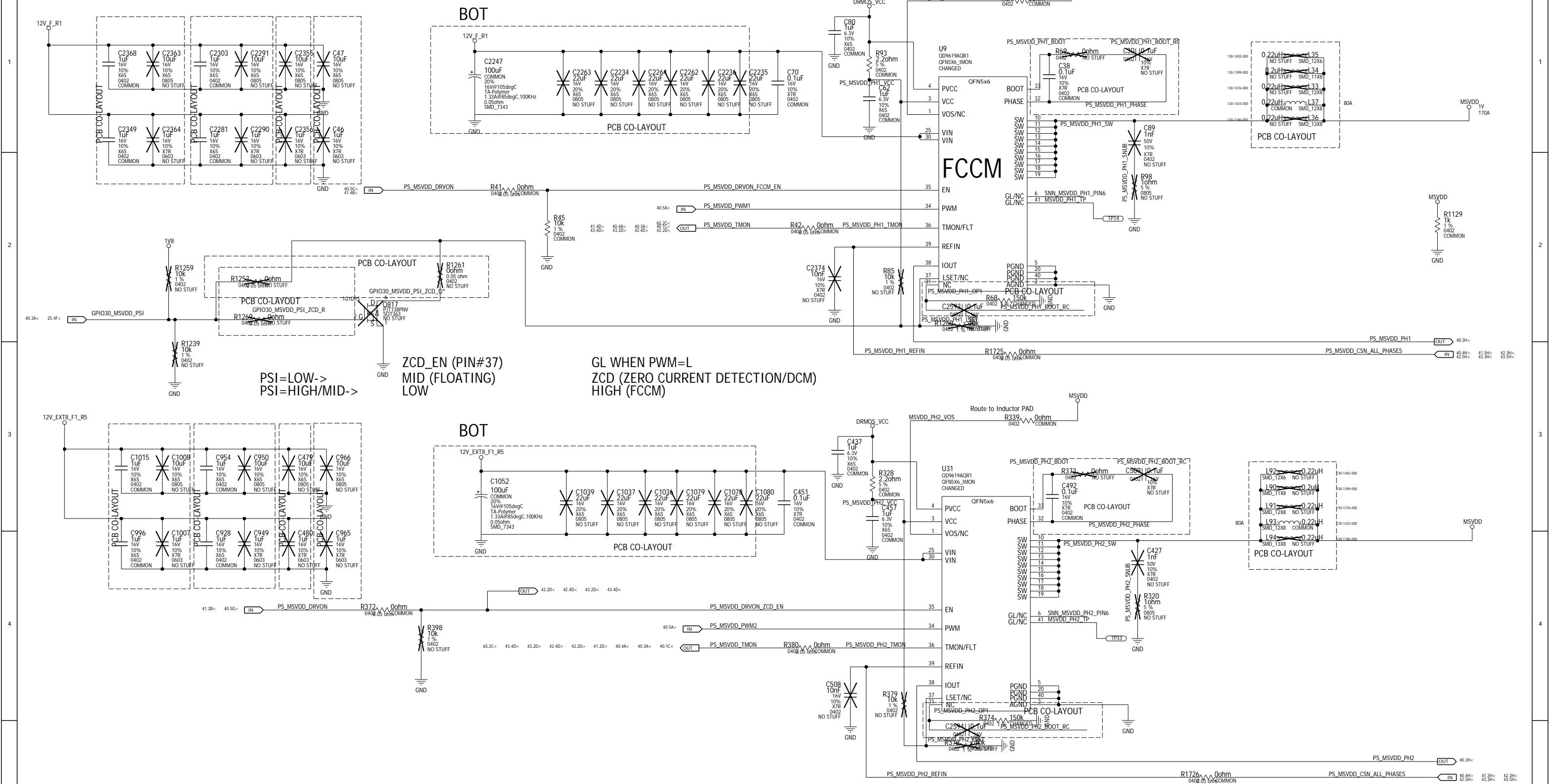
Added for A00 x16

ADDED FOR A00 x16 DESIGN: PLACE UNDER MEMORIES





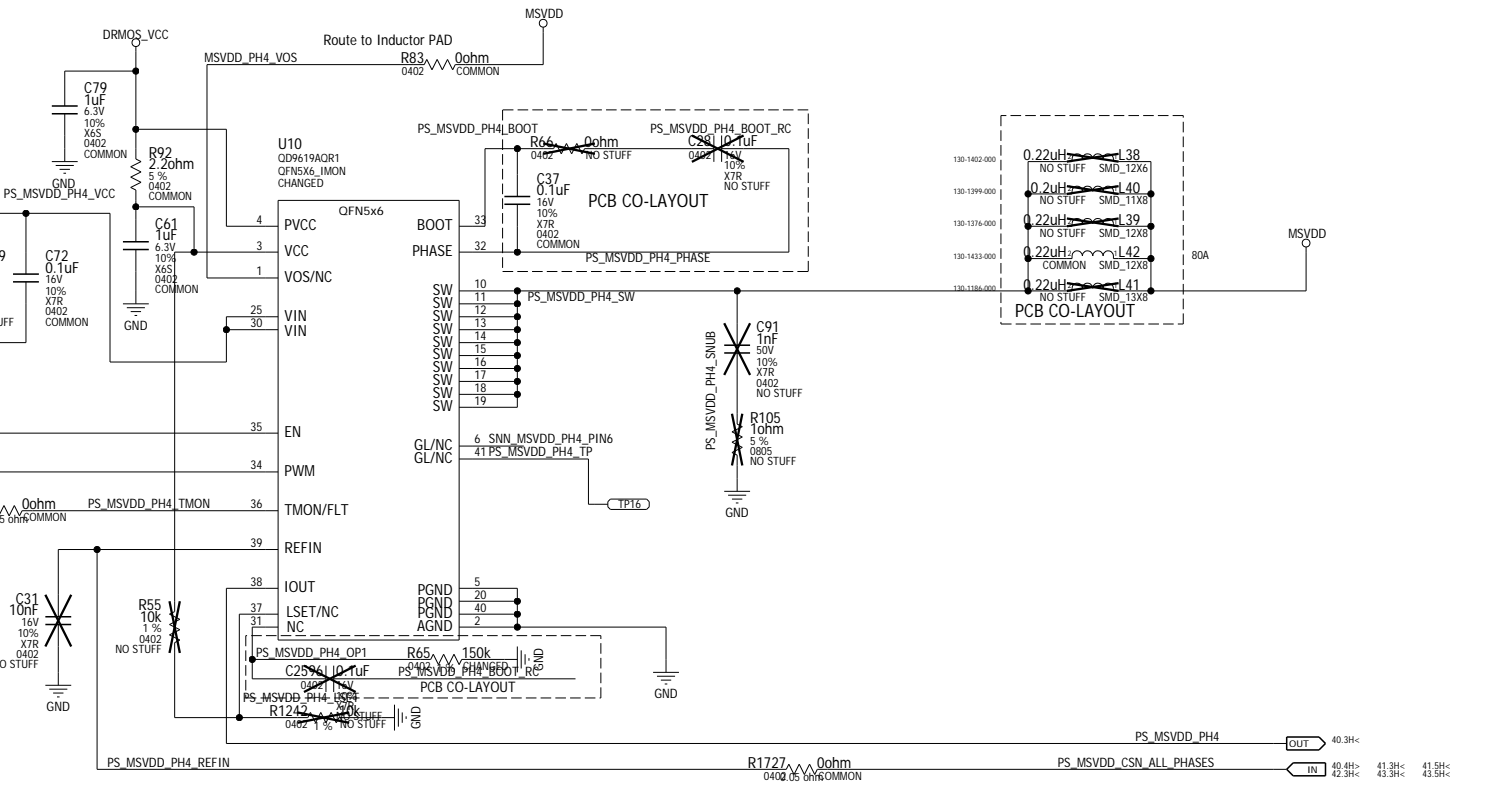
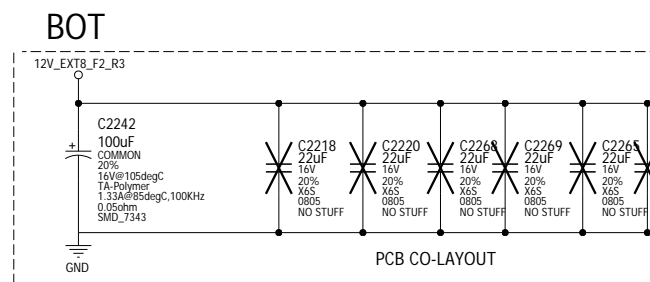
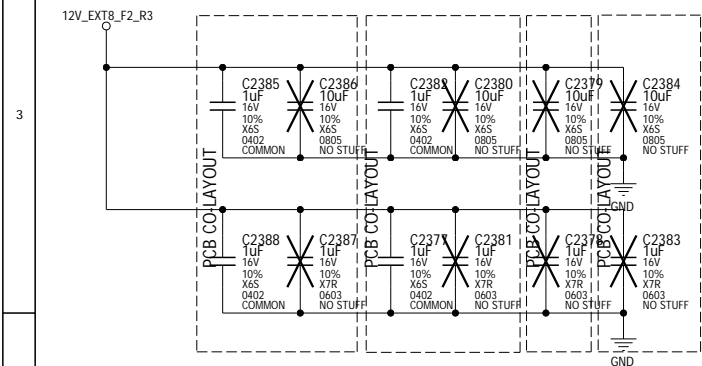
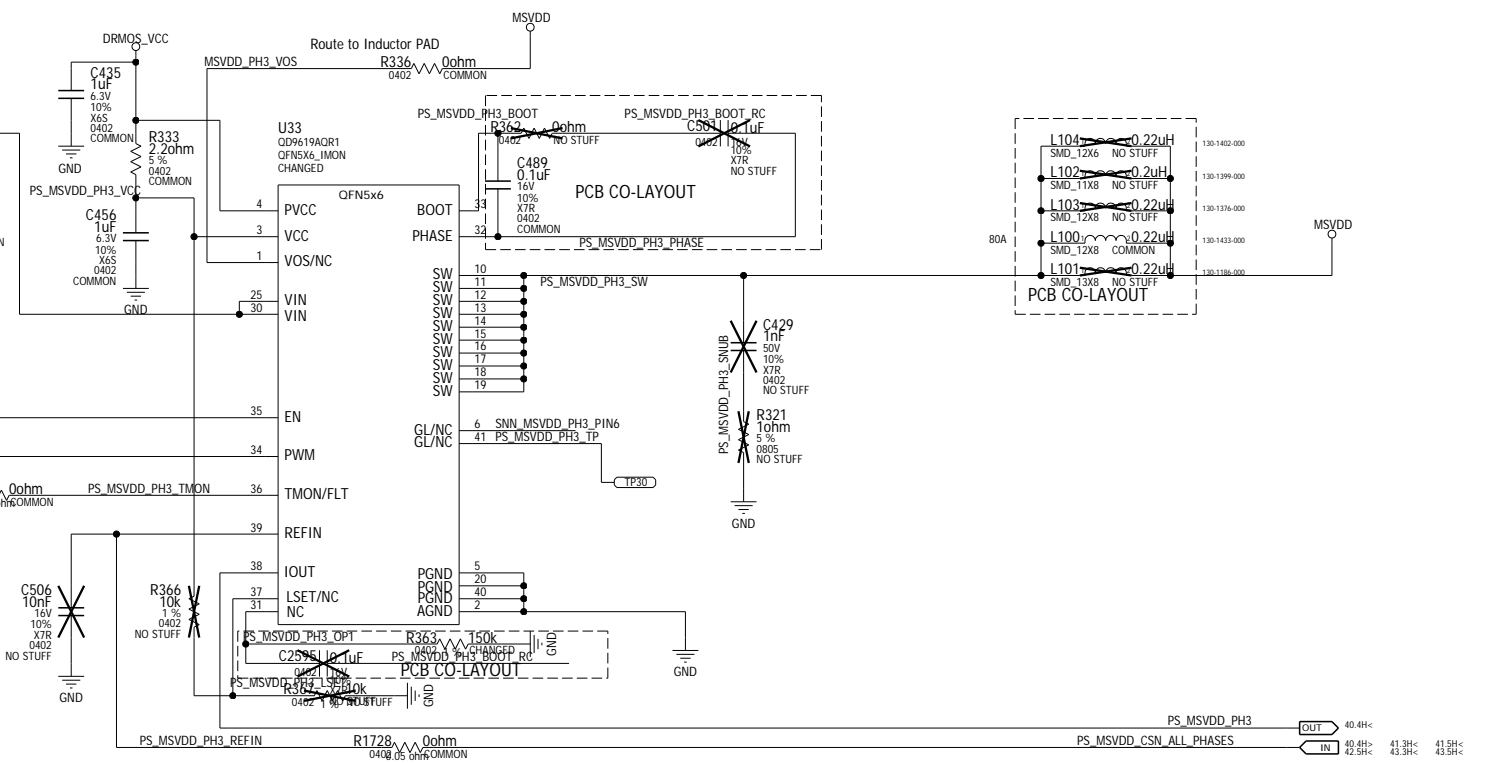
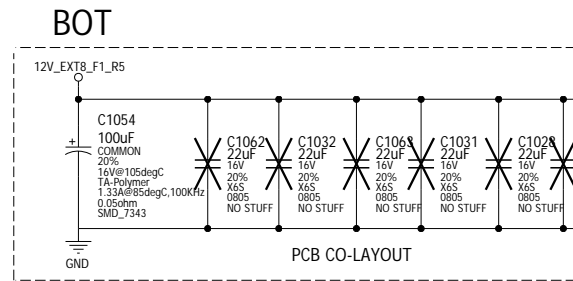
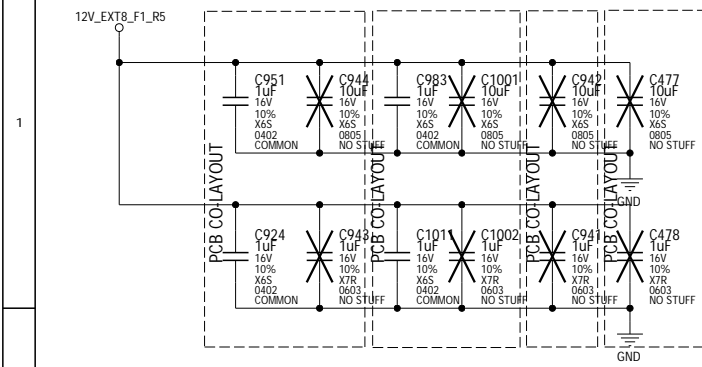




ASSEMBLY	SKU30
PAGE DETAIL	PS: MSVDD PH1 (PWM1 ) and PH2 (PWM2

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## Page 42: PS: MSVDD PH3 (PWM6), PH4 (PWM3)



ASSEMBLY	SKU30
PAGE DETAIL	PS: MSVDD PH3 (PWM6 ) and PH4 (PWM3

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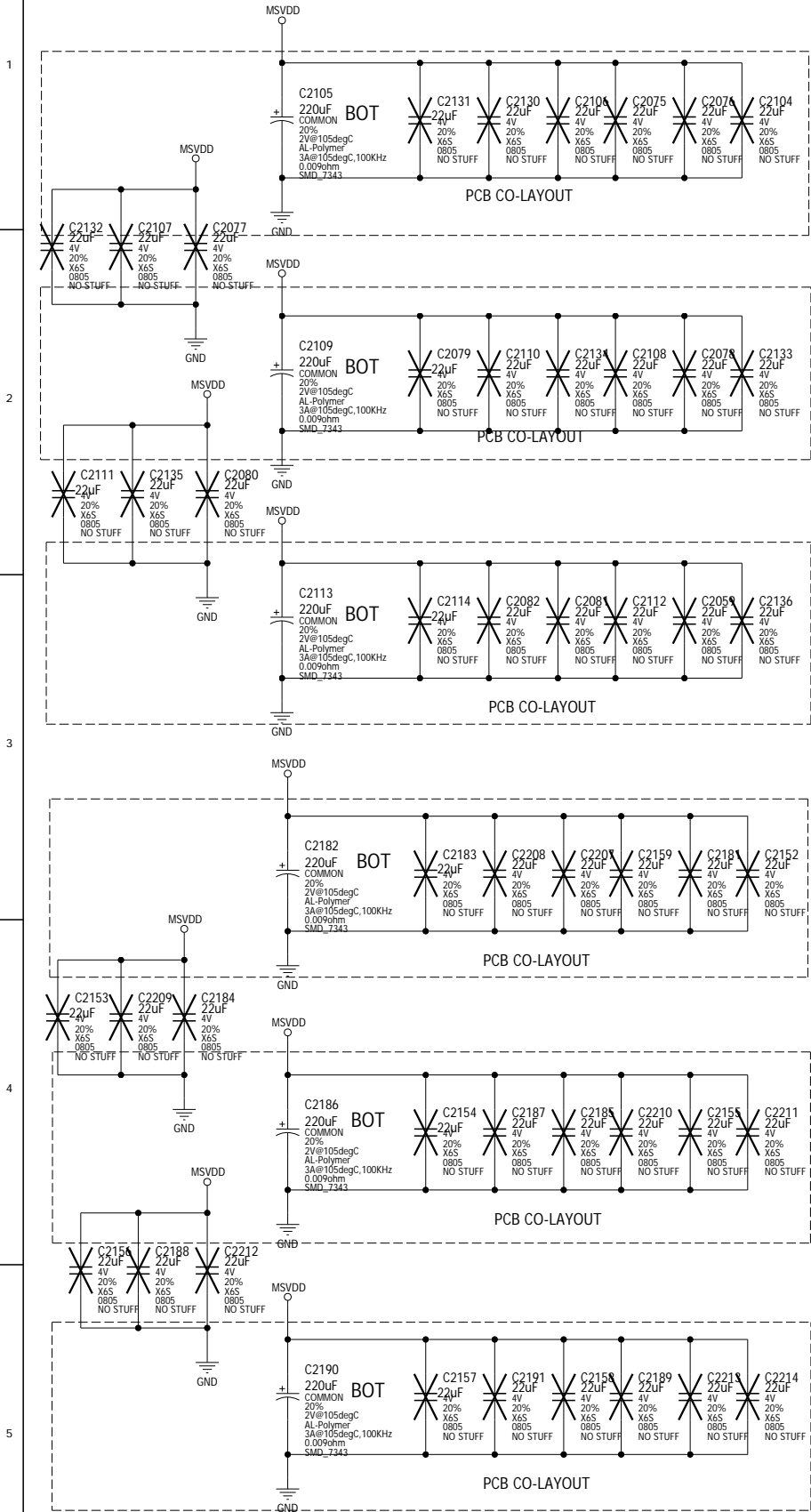
NIV. RN	600-1G133-0030-900
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PCB REV	PG133-A03	PAGE	42 OF 67
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PCB REV	PCB55-A03	PAGE	42 of 67
BOM REV	A	DATE	11-JUN-2020

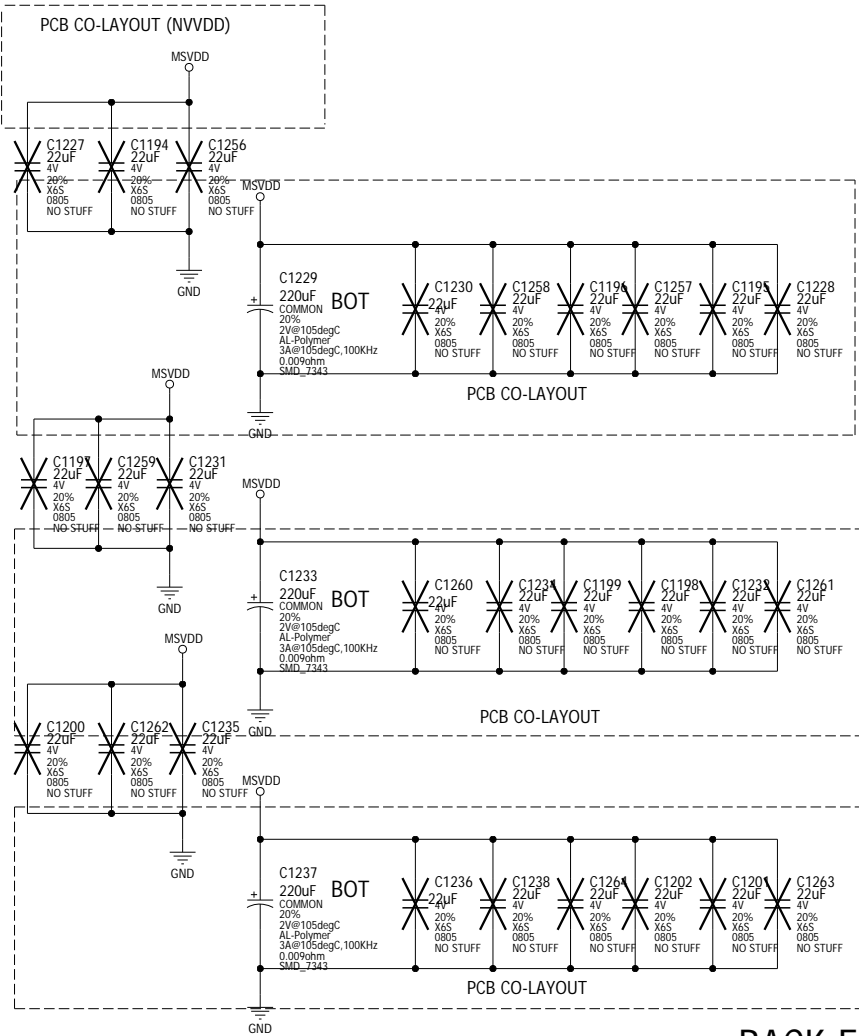
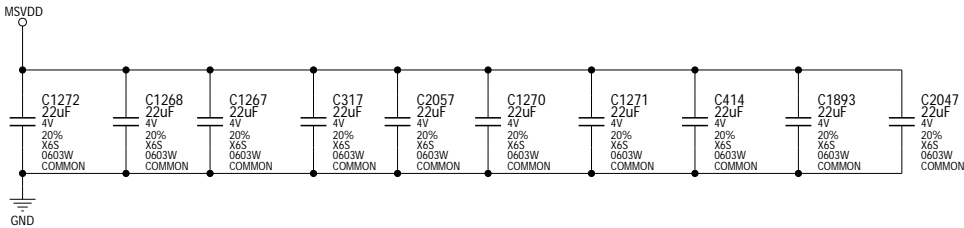


Page 44: PS: MSVDD OUTPUT CAP  
12x SMD7343 330uF CO-LAYOUT WITH 72x 0805 22uF



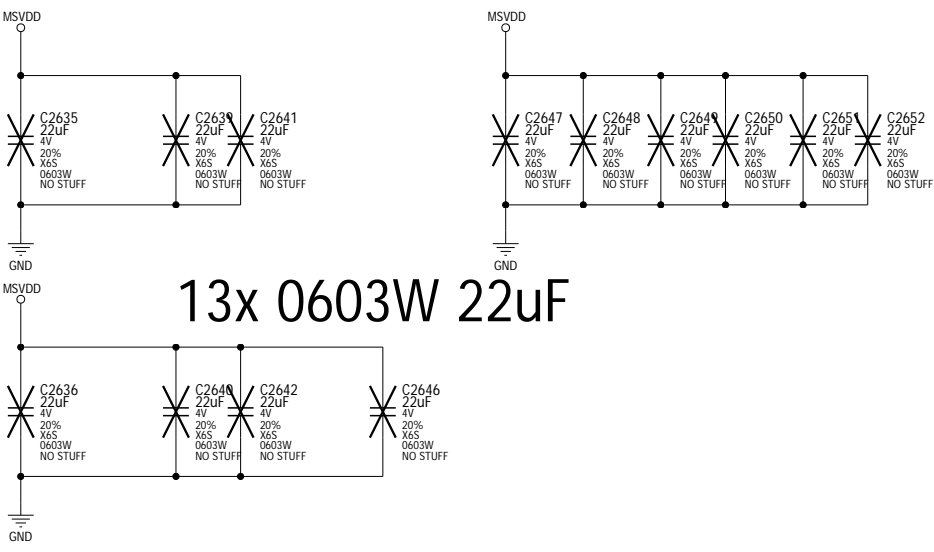
BACK WEST OF PCB

10x 0603W 22uF BETWEEN GPU AND VRM



BACK EAST OF PCB

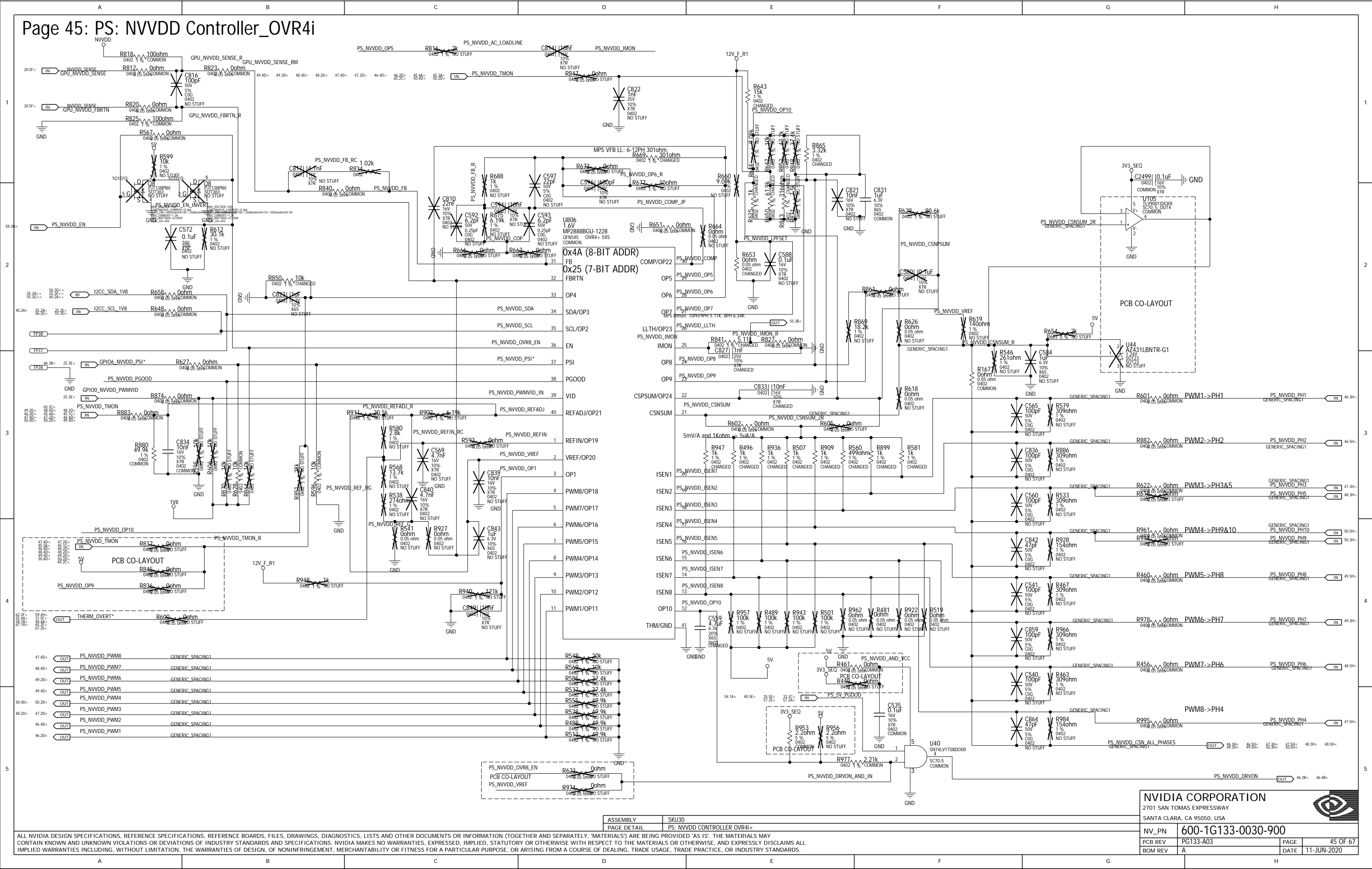
Added for A00 x16



13x 0603W 22uF

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NV_PN	600-1G133-0030-900		
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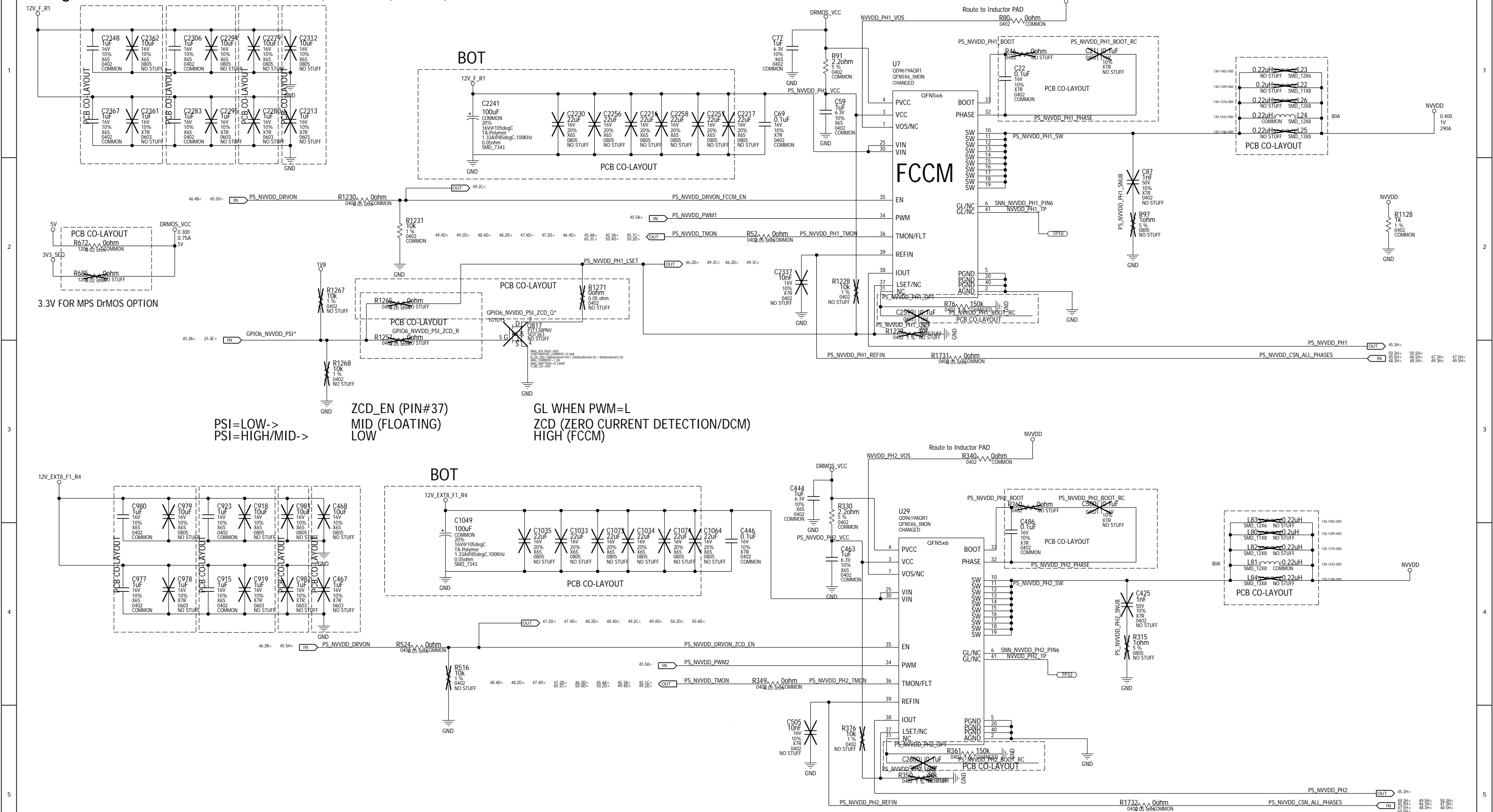
PCB REV PG133-A03

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DATE 11-JUN-2020

## Page 46: PS: NVVDD PH 1 (PWM1), PH 2 (PWM2)



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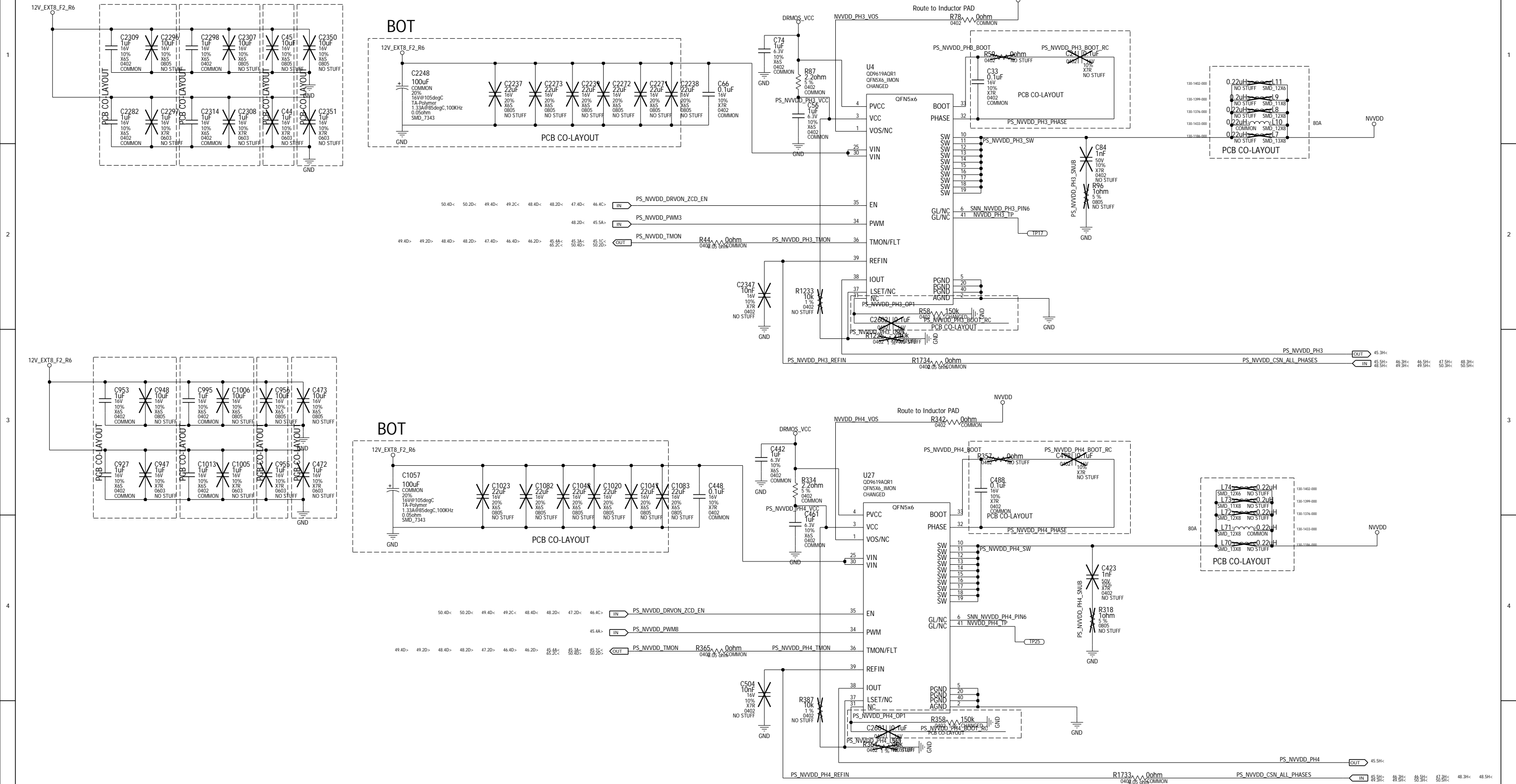
	SANTA CLARA, CA 95050, USA
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NV PN	600-1G133-0030-900
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PCB REV	PG133-A03	PAGE	46 OF 67
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## Page 47: PS: NVVDD PH 3 (PWM3), PH 4 (PWM8)



ASSEMBLY	SKU30
PAGE DETAIL	PS: NVVDD PH3 (PWM3 ) and PH4 (PWM8

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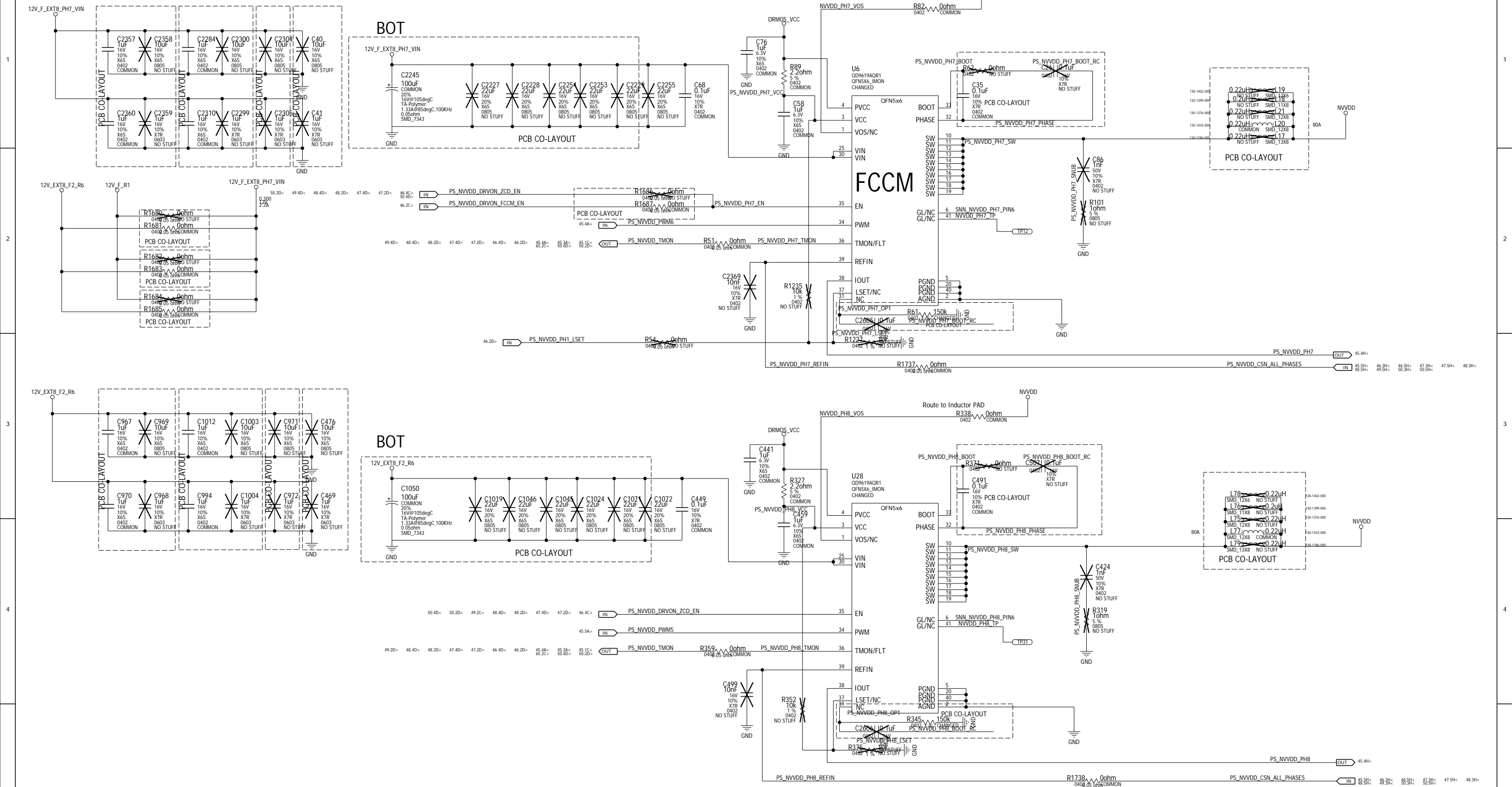
PCB REV	PG133-A03	PAGE	47 OF 67
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## Page 49: PS: NVVDD PH 7 (PWM6), PH8 (PWM5)



ASSEMBLY	SKU30
PAGE DETAIL	PS: NVVDD PH7 (PWM6 ) and PH8 (PWM5

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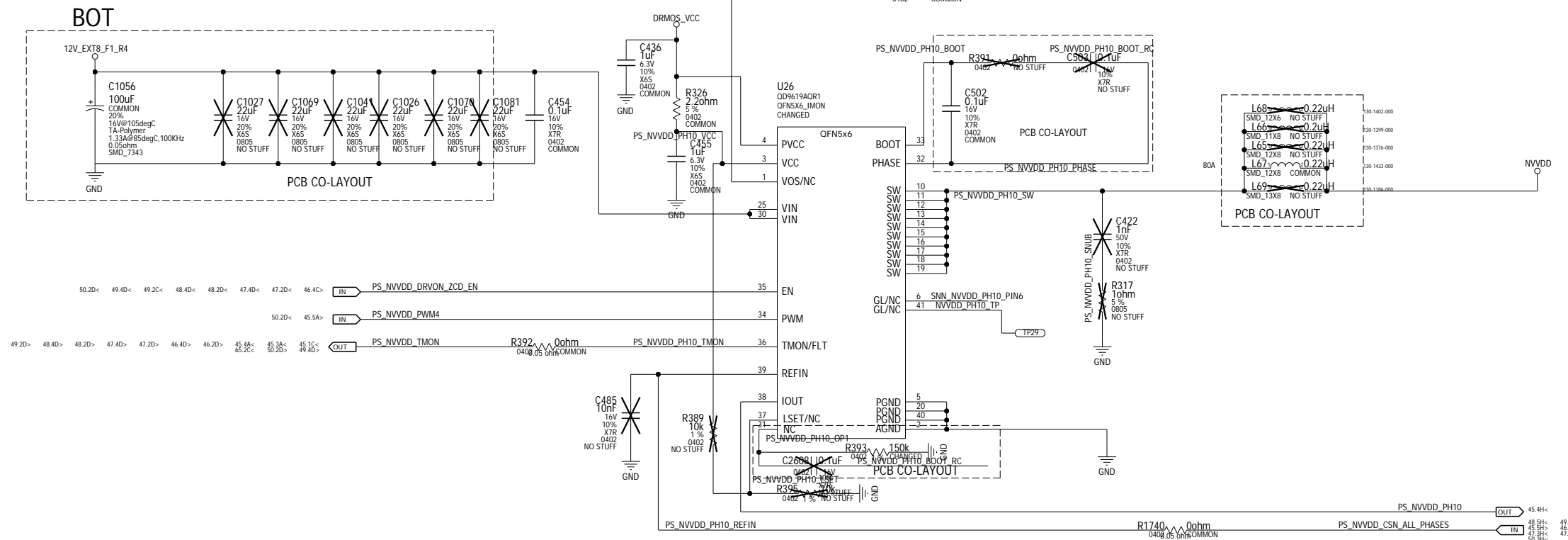
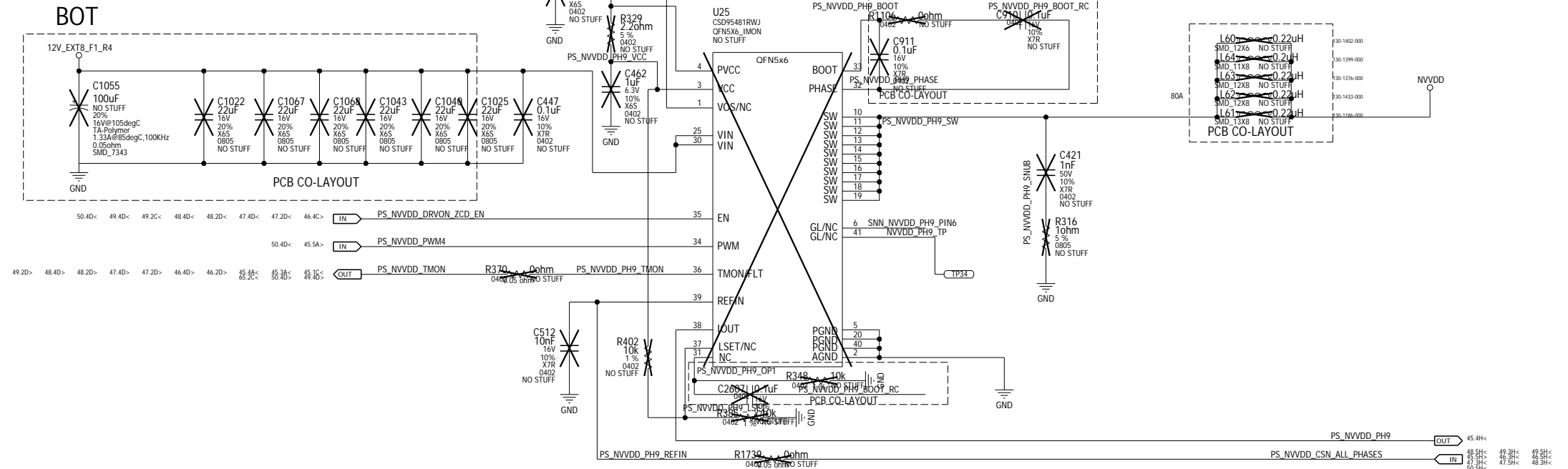
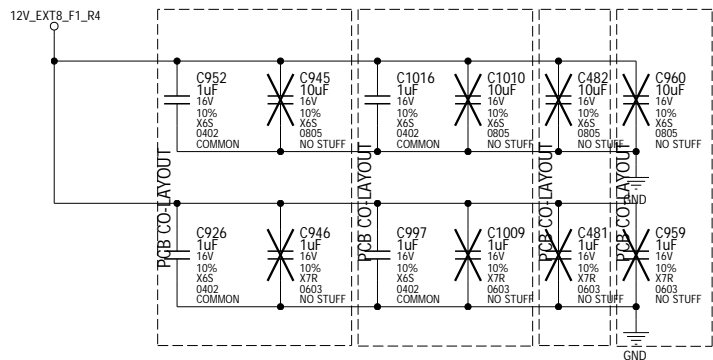
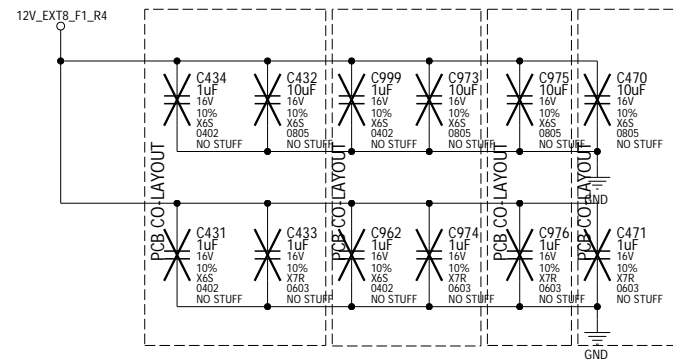
PCB REV	PG133-A03
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BOM REV

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DATE	11-JUN-2020
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ASSEMBLY	SKU30
PAGE DETAIL	PS: NVVDD PH9 (PWM4 ), PH10 (PWM4 )

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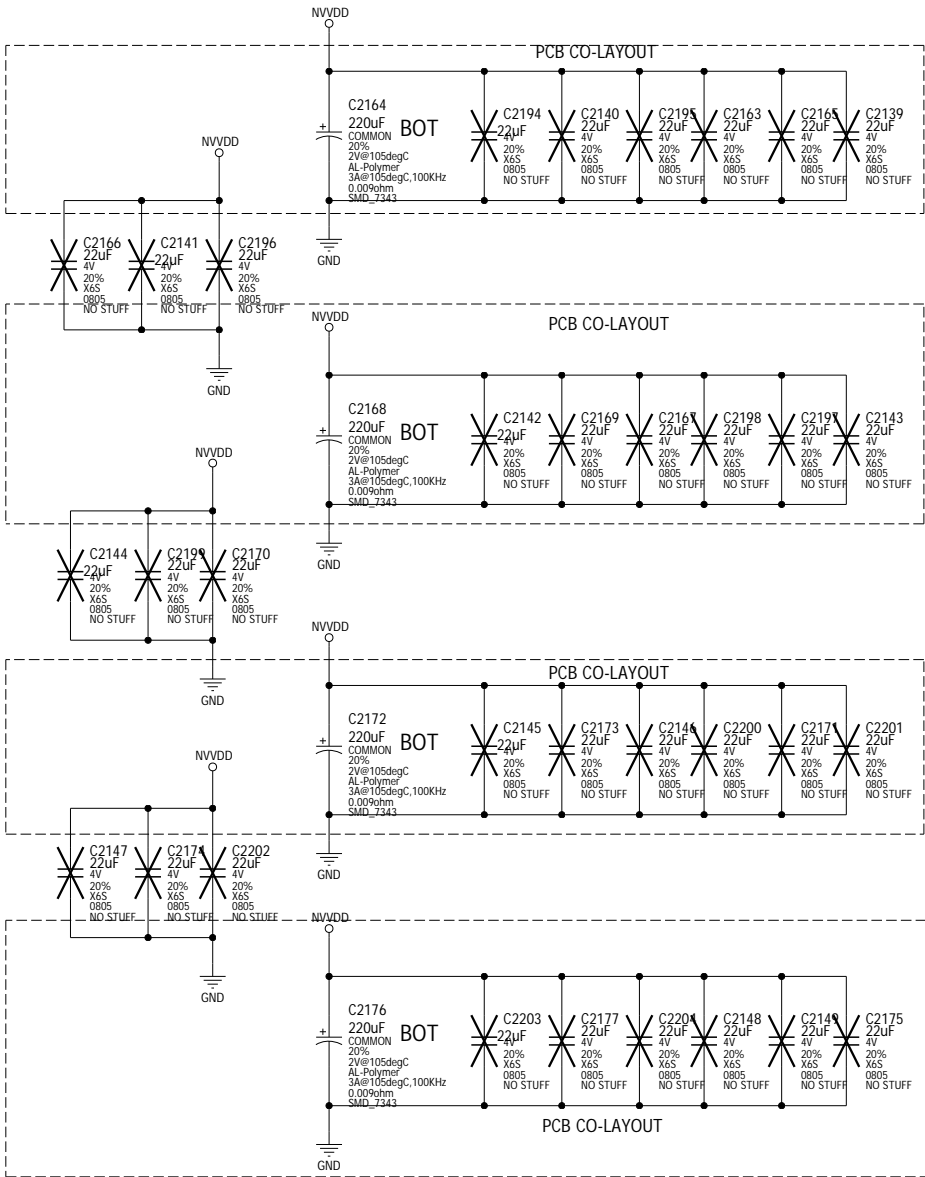
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NV_PN	600-1G133-0030-900
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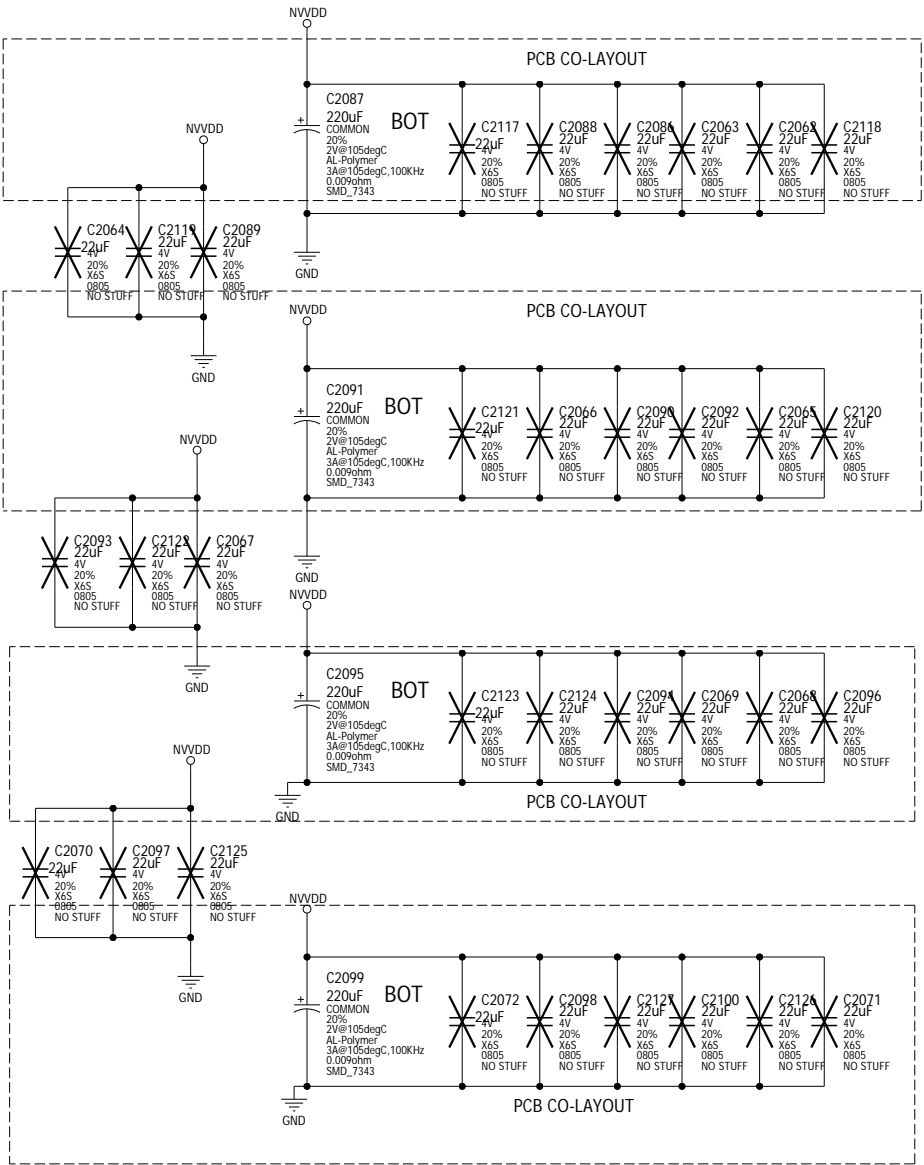
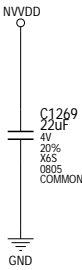
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20x SMD7343 220uF CO-LAYOUT WITH 120x 0805 22uF



BACK WEST OF PCB

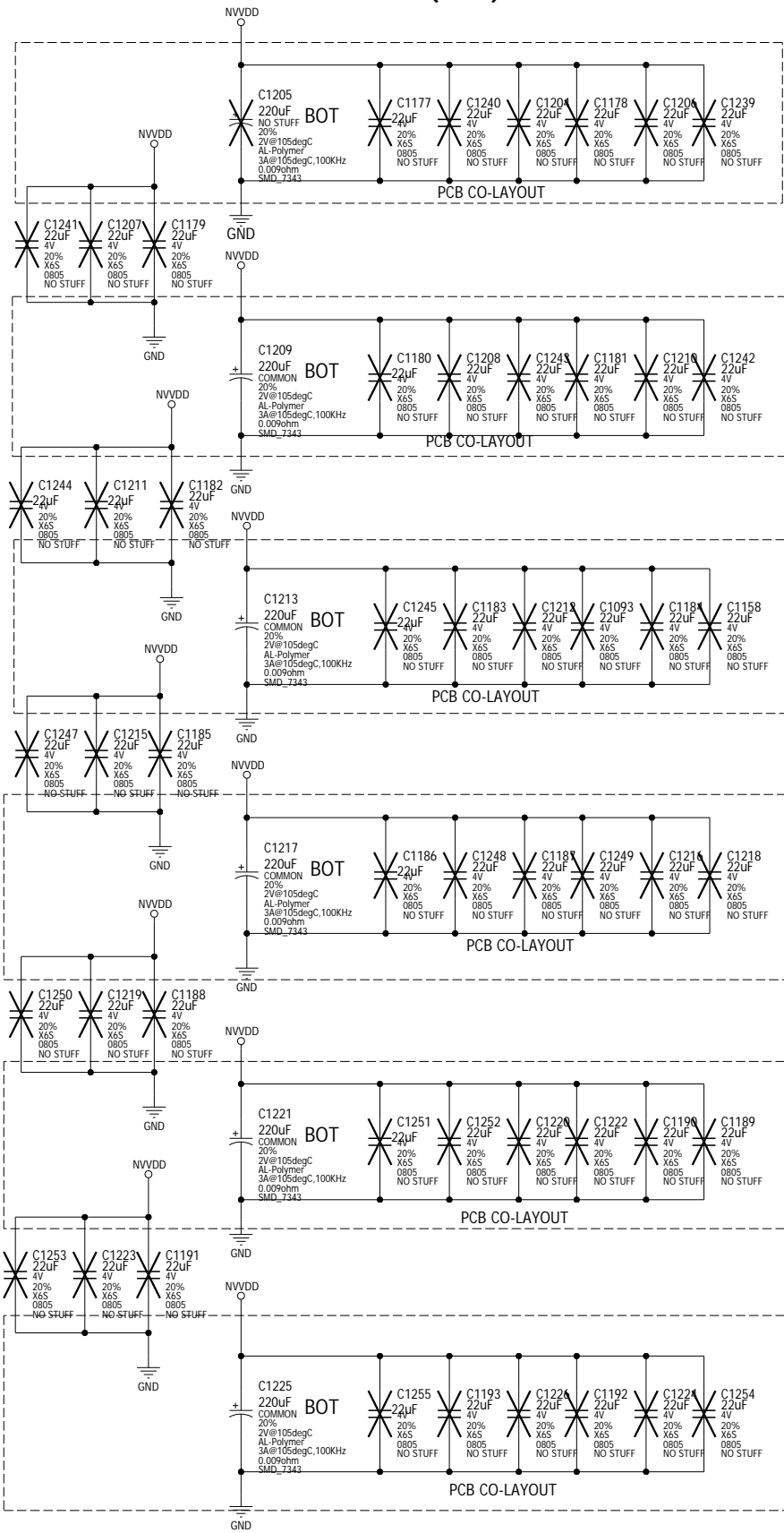


BACK WEST OF PCB

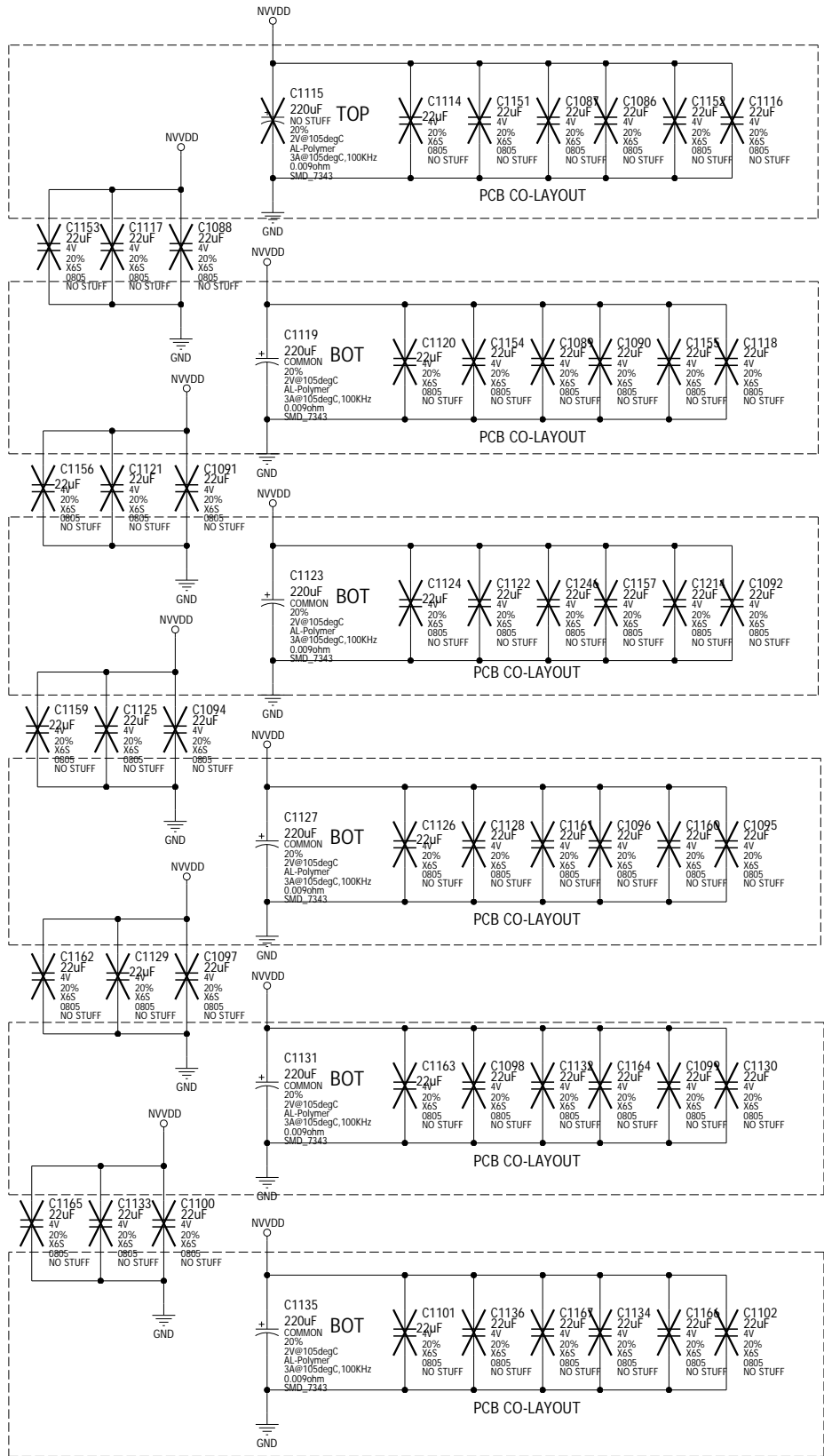
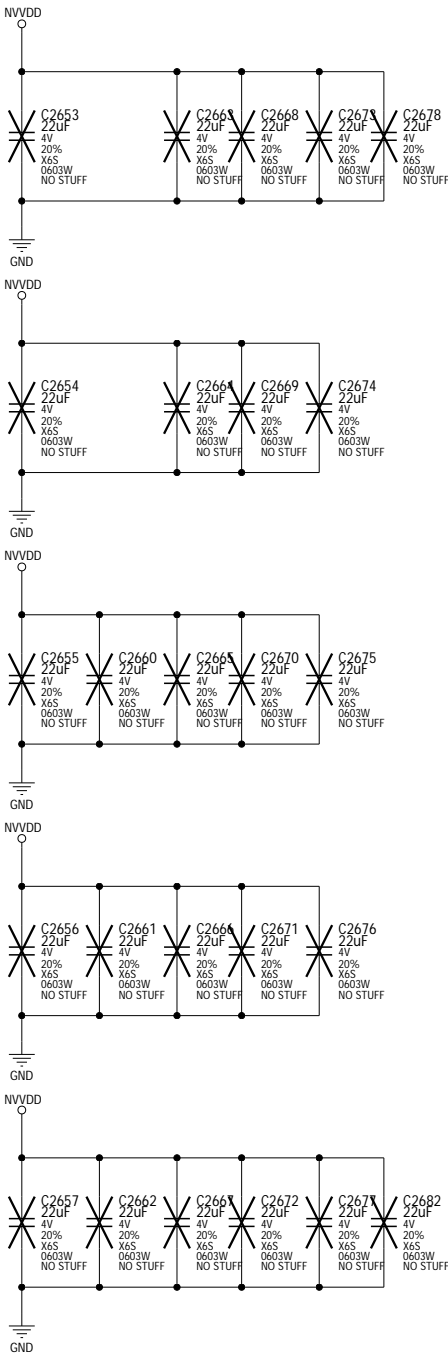
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ASSEMBLY	SKU30
PAGE DETAIL	PS: NVVDD OUTPUT CAP (1/2)

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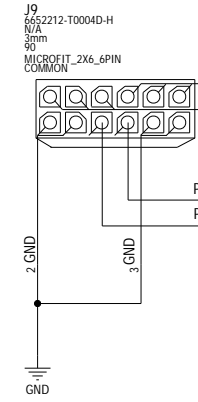
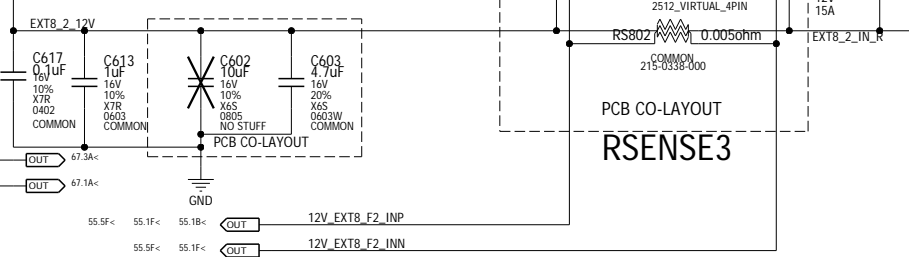
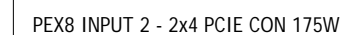
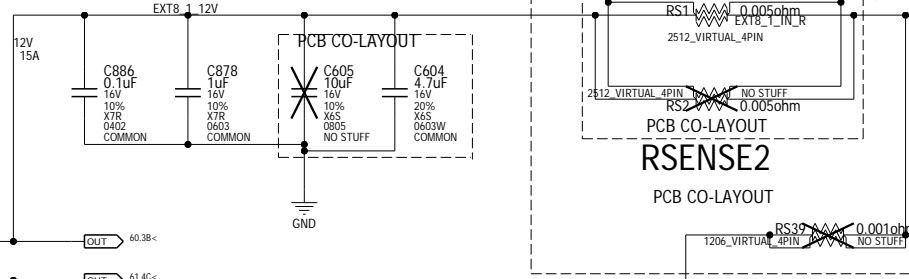
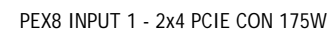
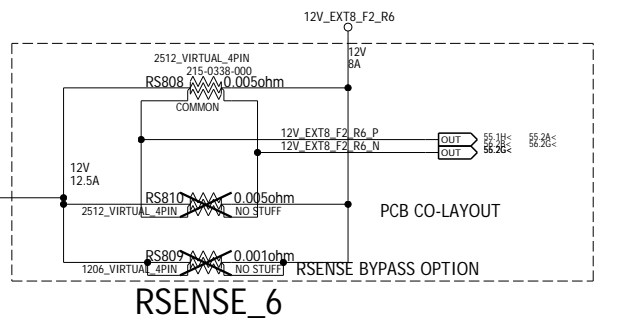
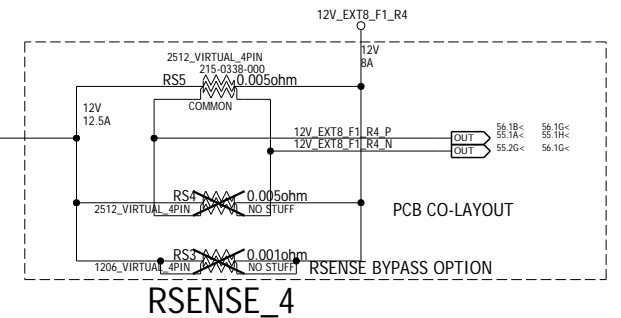
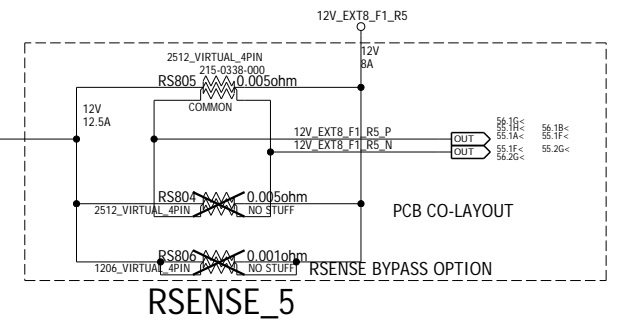
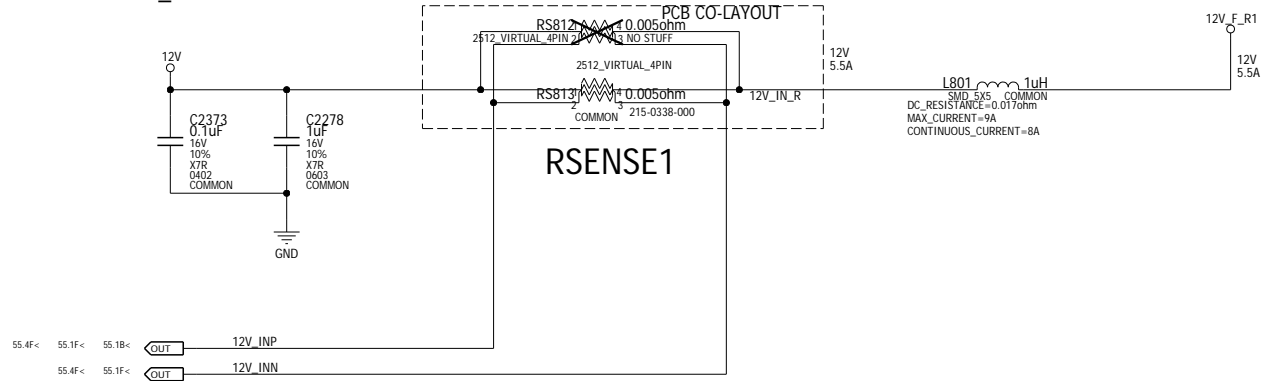
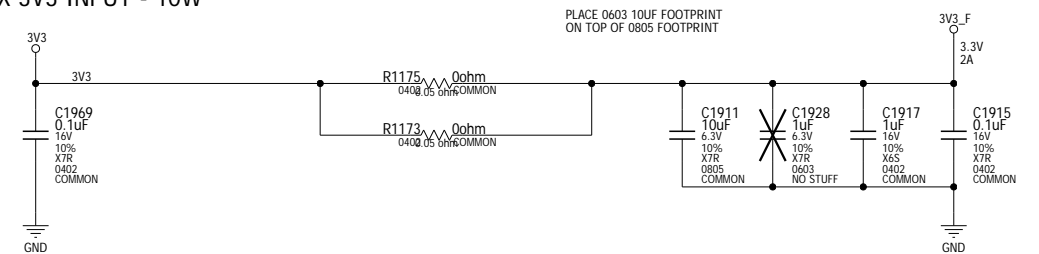
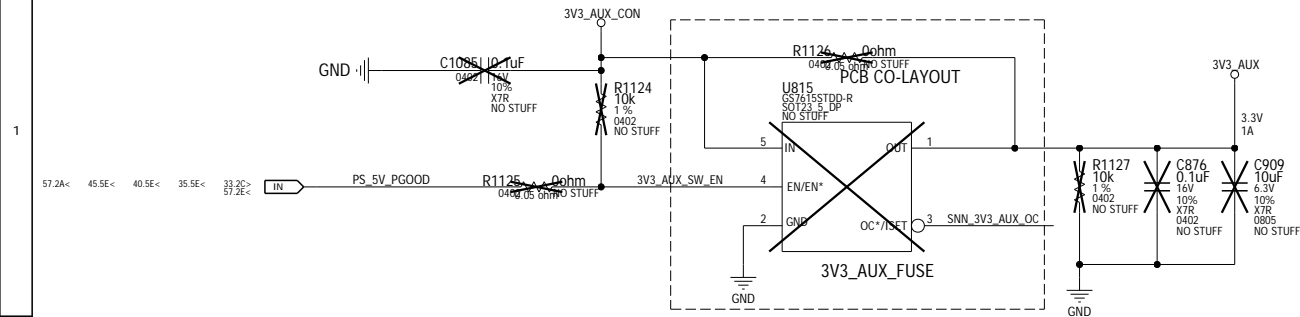


Added for A00 x16  
25x 0603W 22uF



BACK EAST OF PCB





MICROFIT-12PIN (GF)

ASSEMBLY	SKU30
PAGE DETAIL	PS: INPUTS, FILTERING, MONITORING

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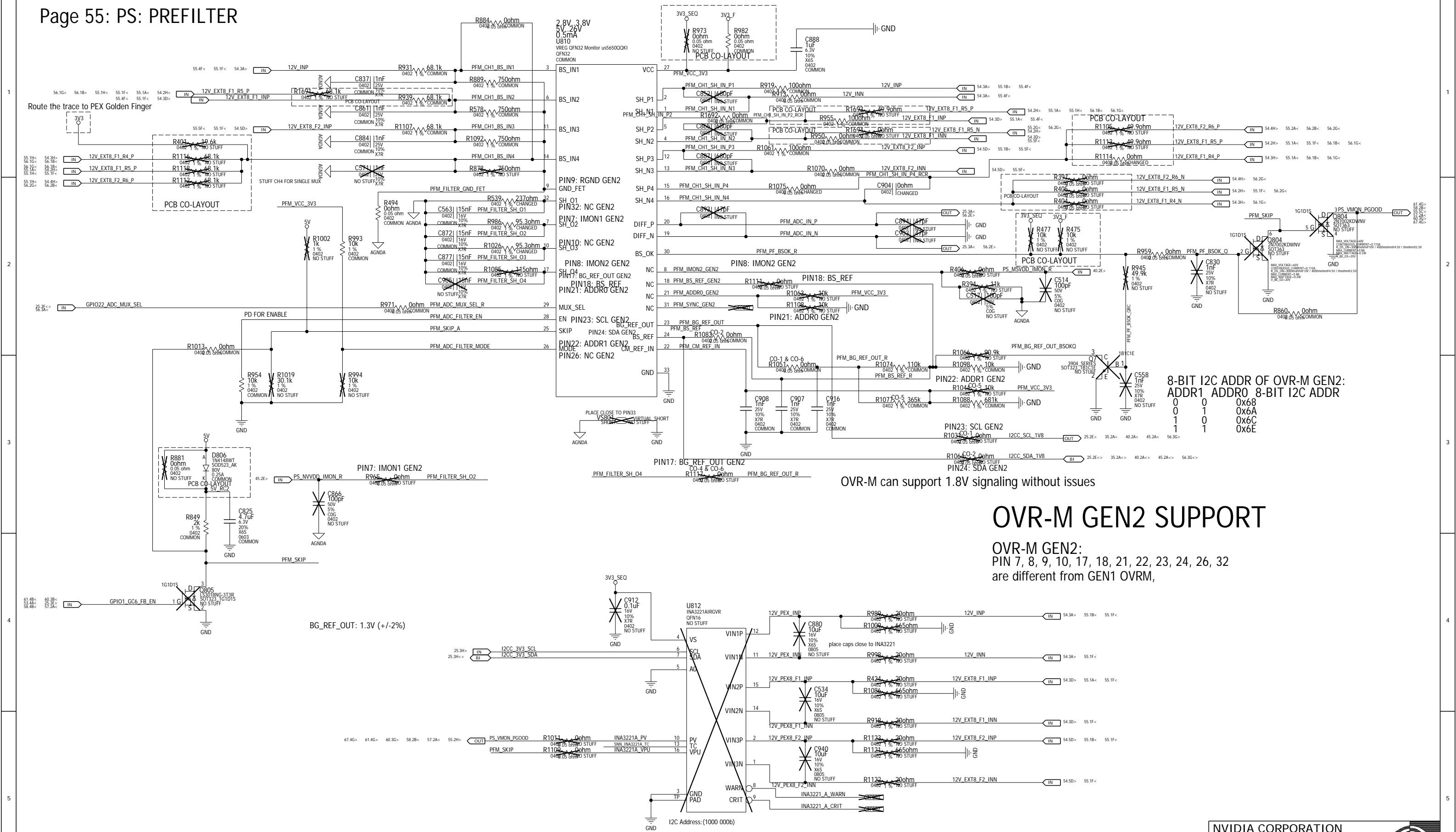
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ASSEMBLY	SKU30
PAGE DETAIL	PS: PREFILTER A/INA3221

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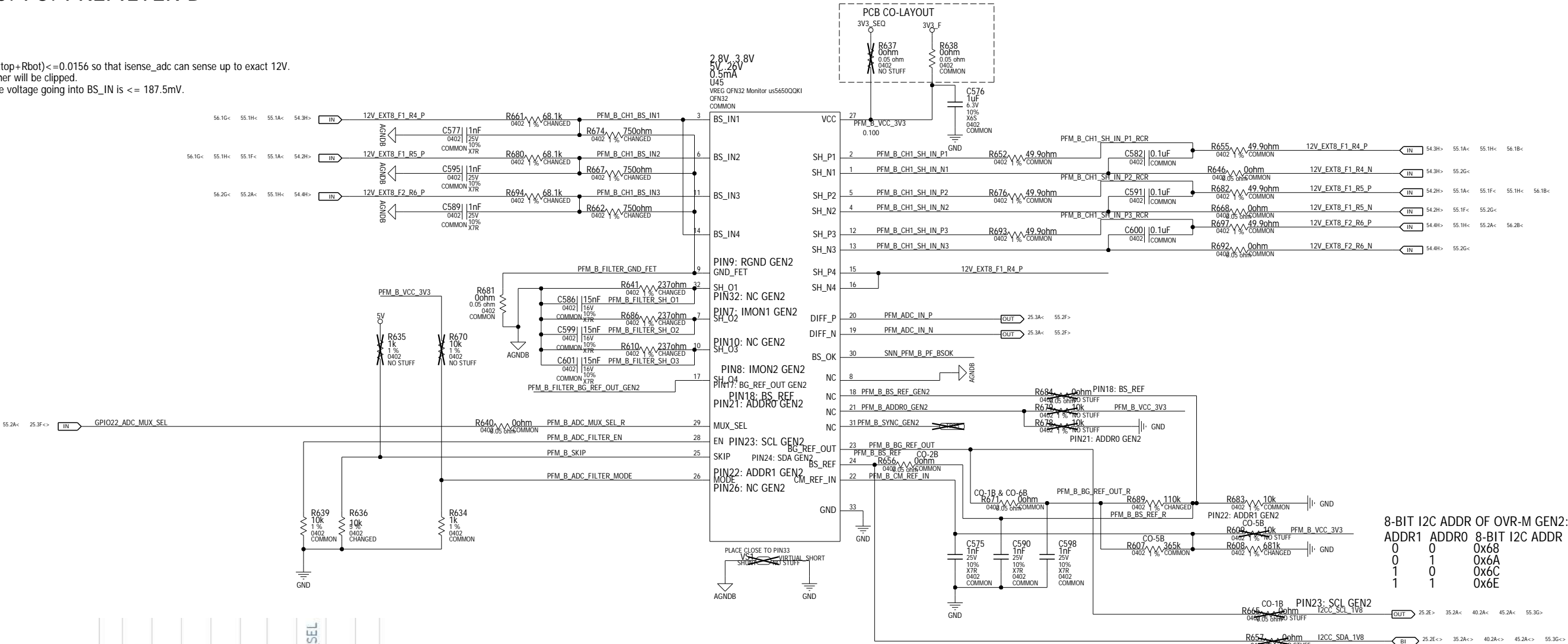
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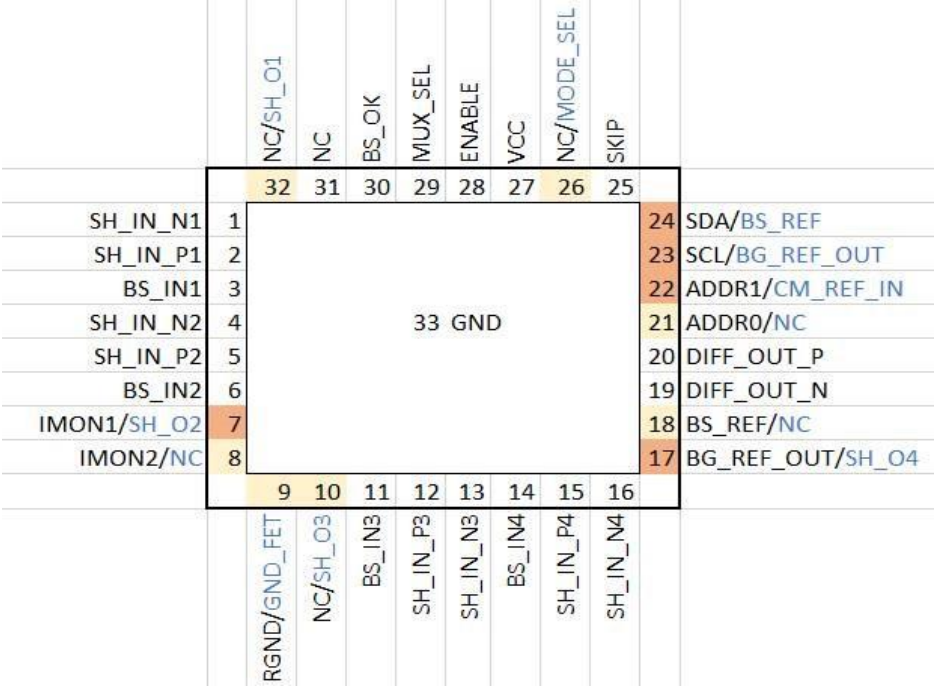
PCB REV	PG133-A03	PAGE	55 OF 67
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BUS:  $R_{bot}/(R_{top}+R_{bot}) \leq 0.0156$  so that  $isense\_adc$  can sense up to exact 12V.  
Anything higher will be clipped.  
Make sure the voltage going into BS\_IN is  $\leq 187.5mV$ .



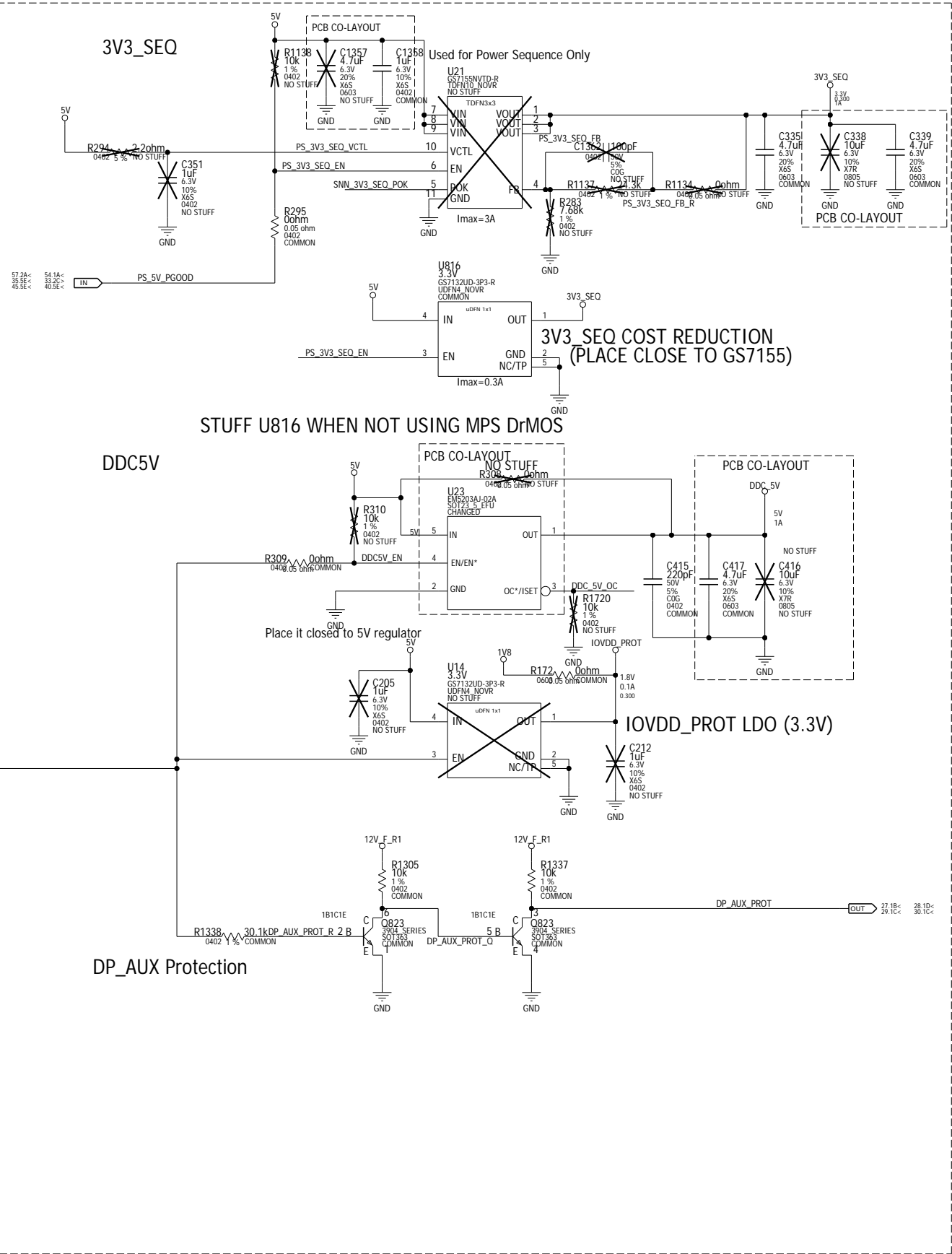
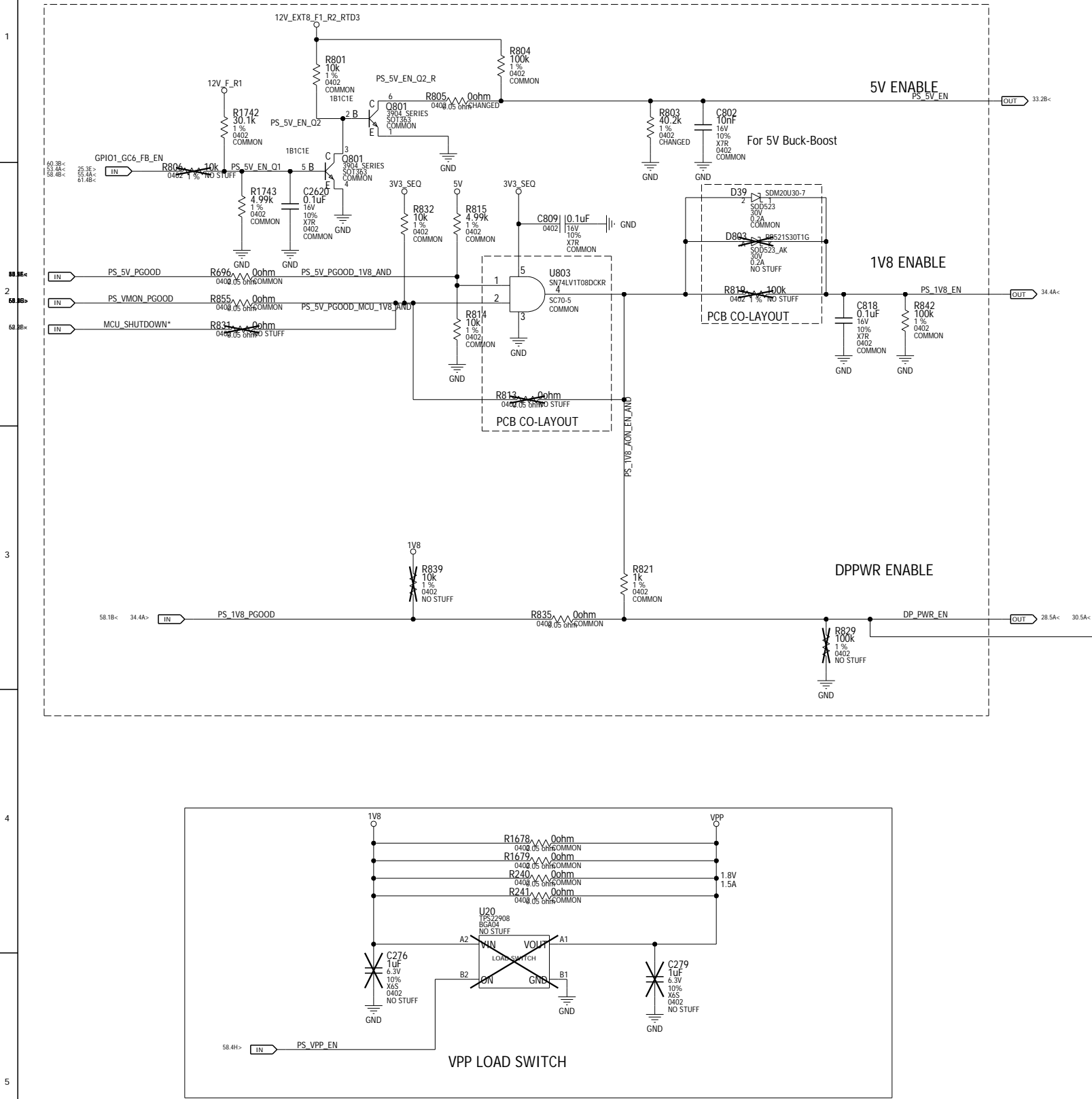
OVR-M GEN2 SUPPORT

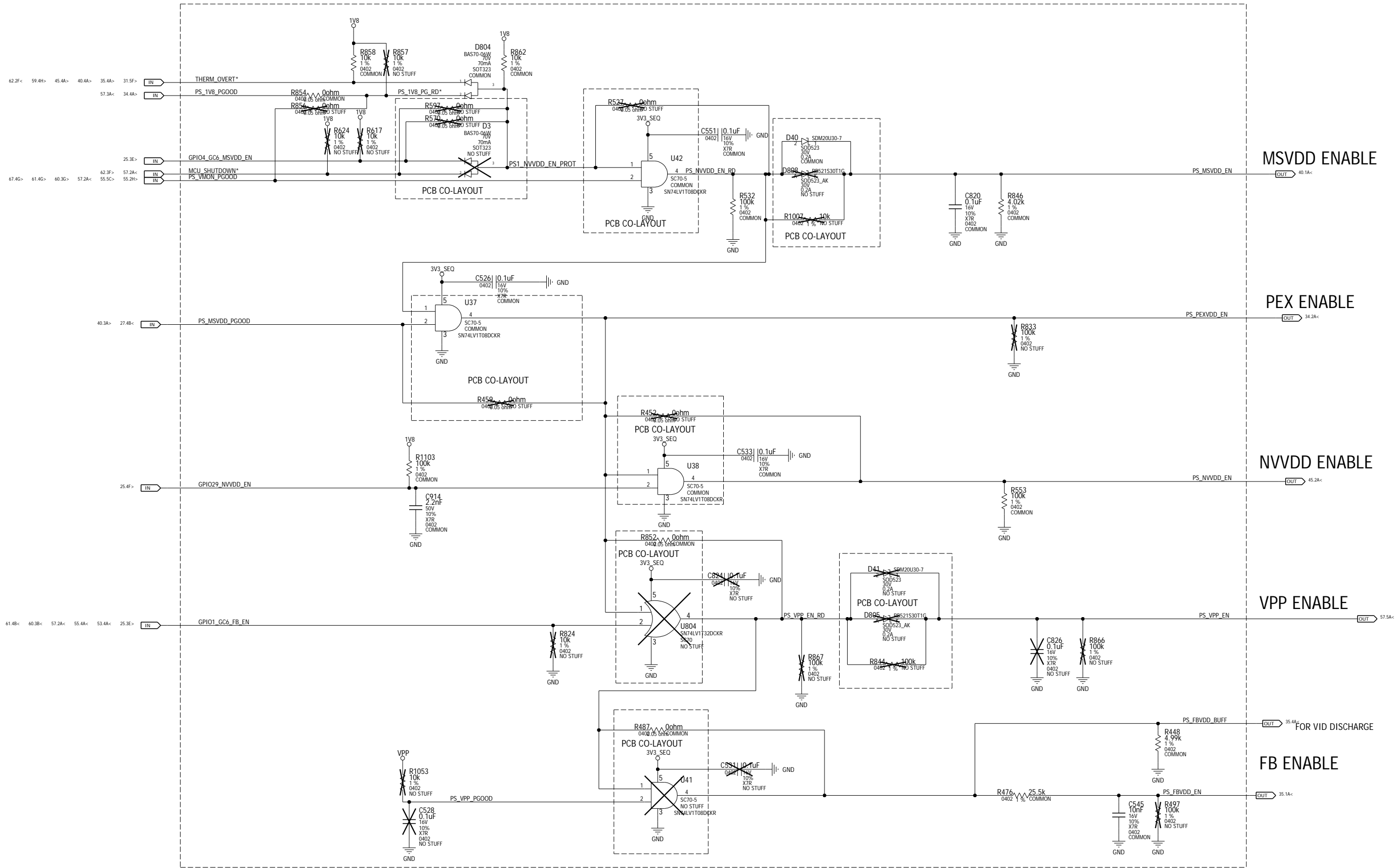
OVR-M can support 1.8V signaling without issues



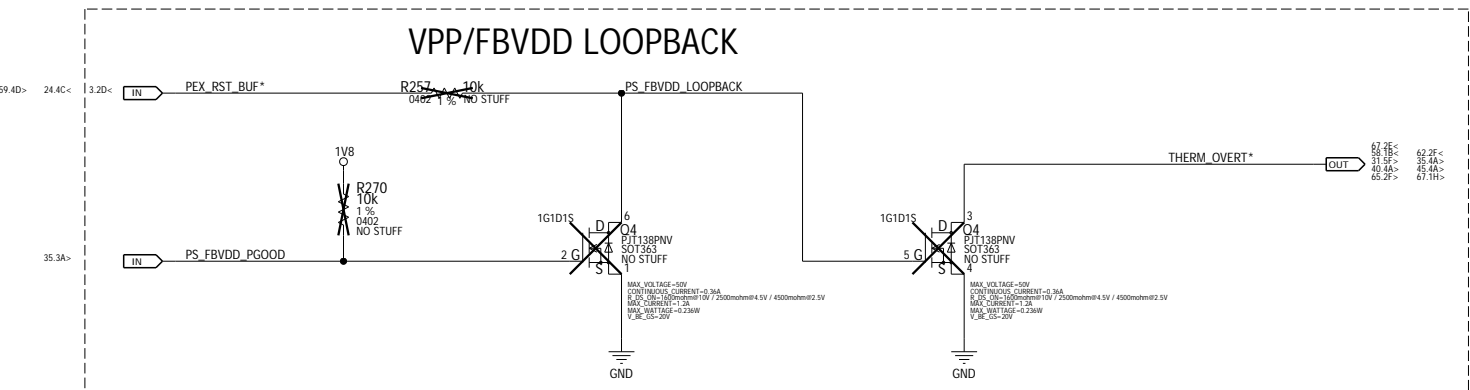
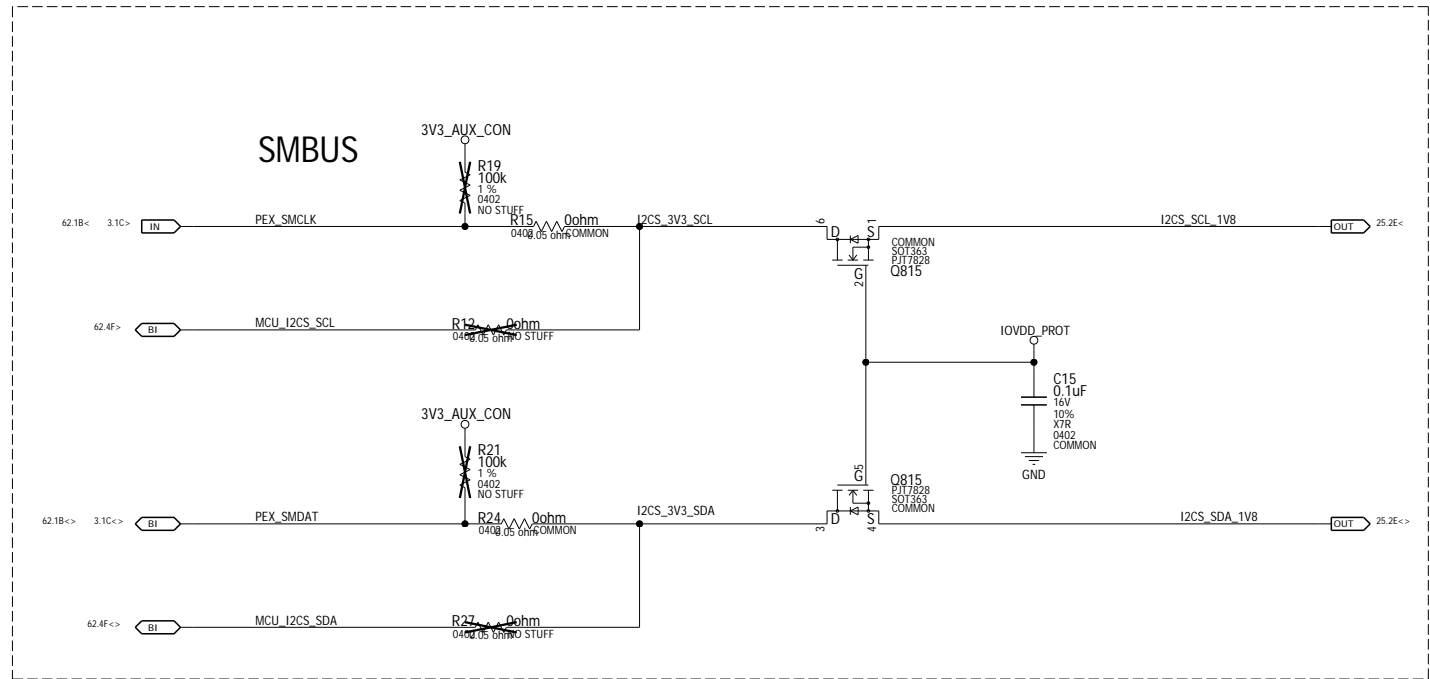
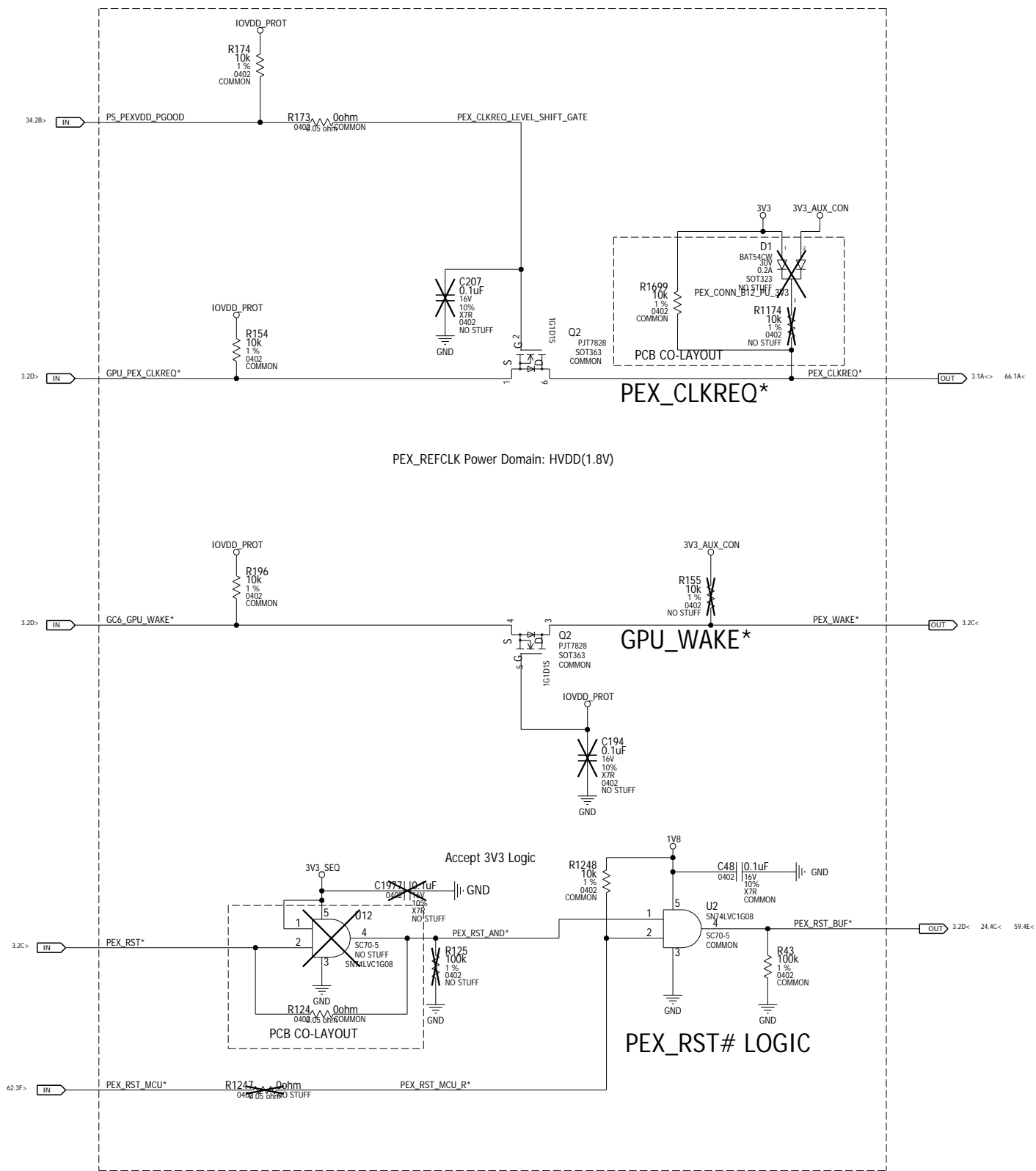
OVR-M GEN2:  
PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32  
are different from GEN1 OVRM,







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## 2

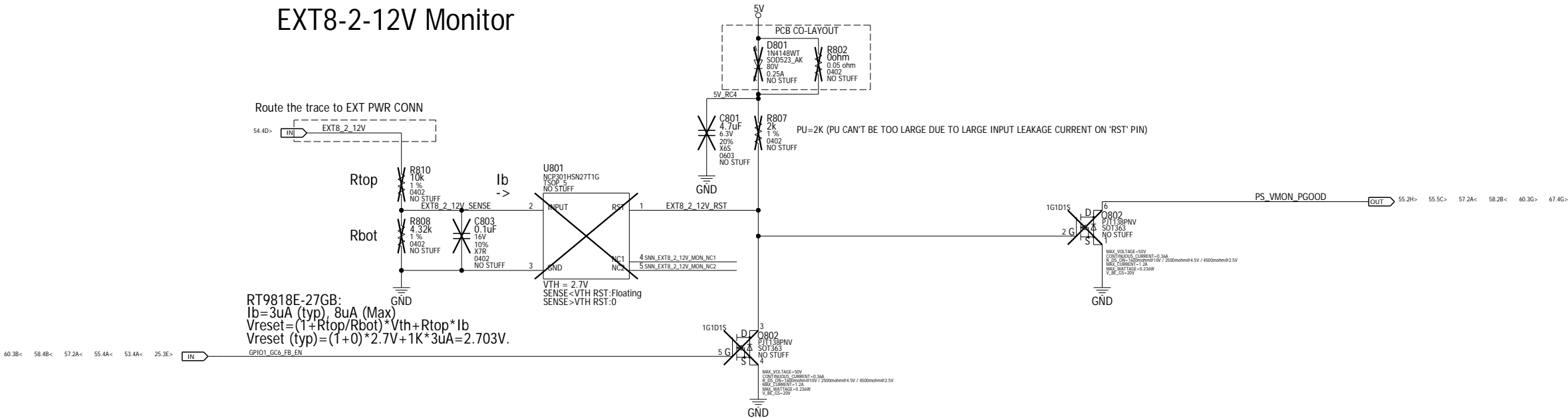
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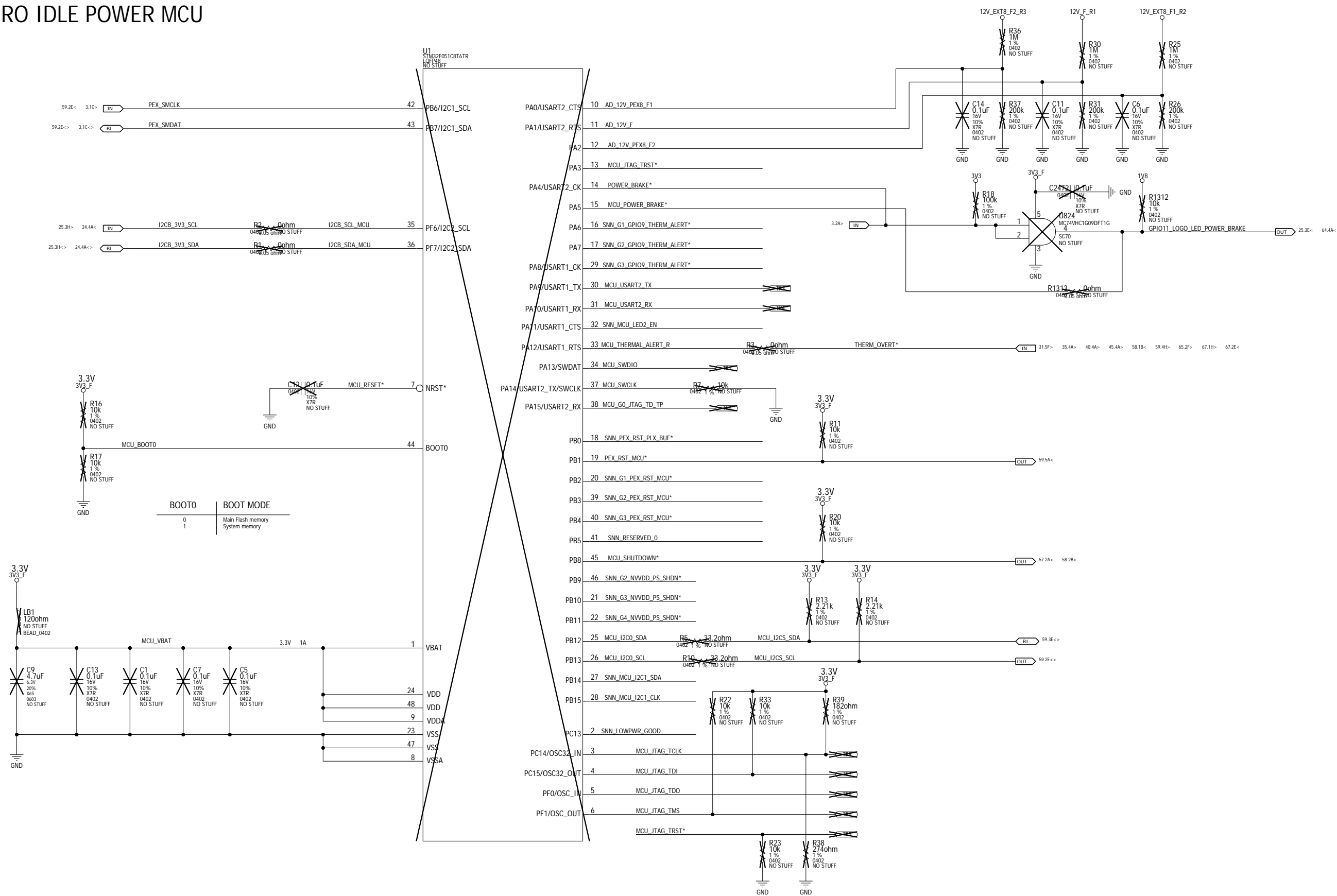
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EXT8-1-12V Monitor: Co-layout with PEX3V3 Monitor

EXT8-2-12V Monitor



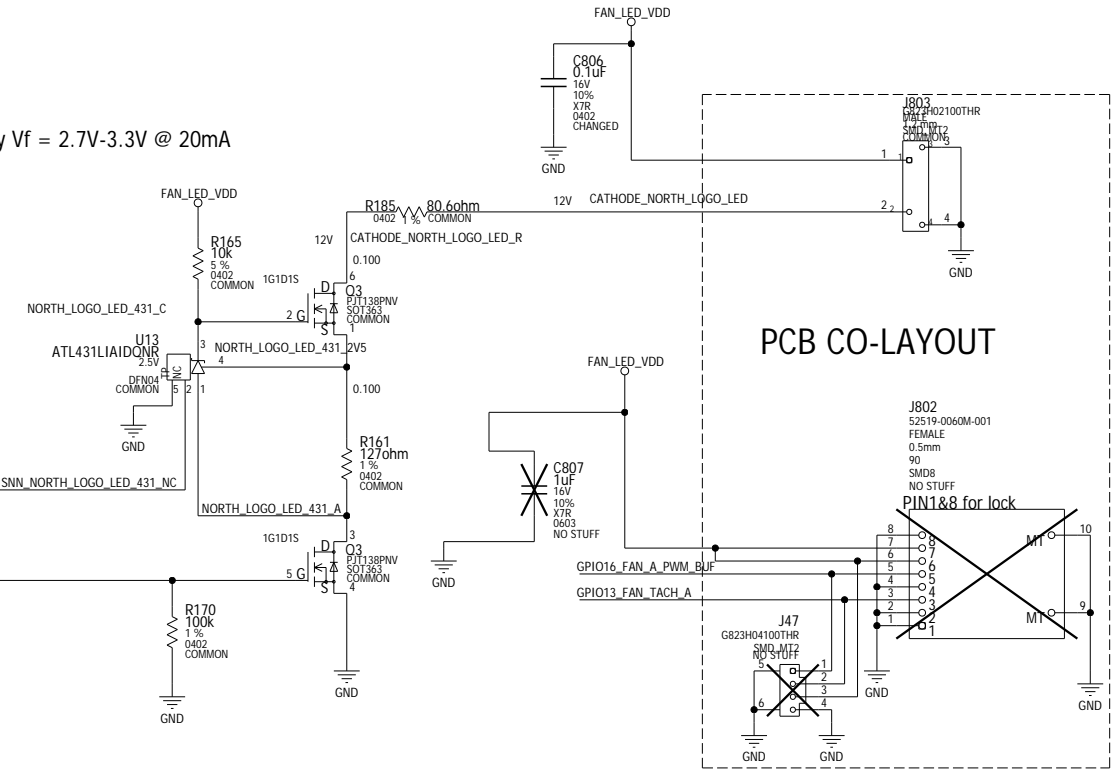


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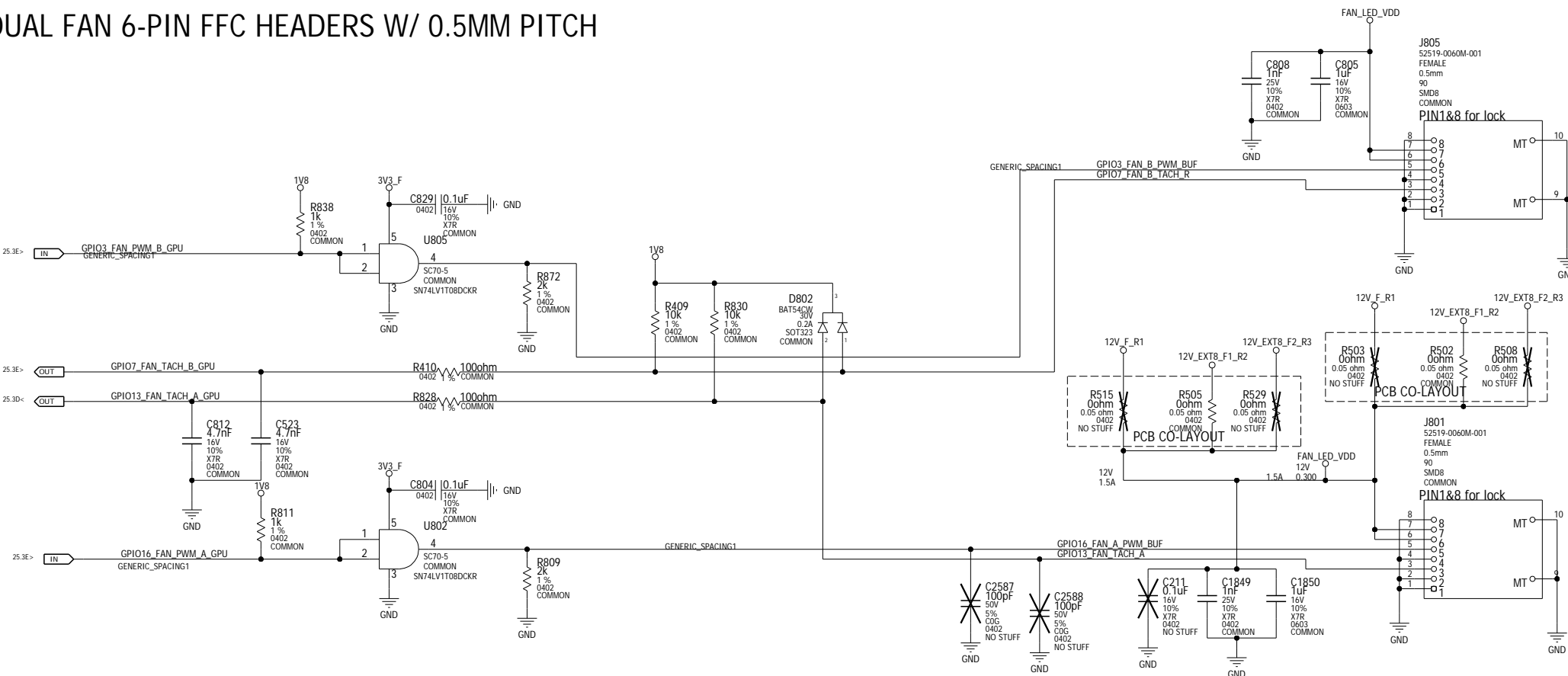
2-PIN LED HEADER FOR NORTH LOGO LED (WHITE)

White LED: Preliminary Vf = 2.7V-3.3V @ 20mA

NORTH LOGO LED (WHITE)



DUAL FAN 6-PIN FFC HEADERS W/ 0.5MM PITCH

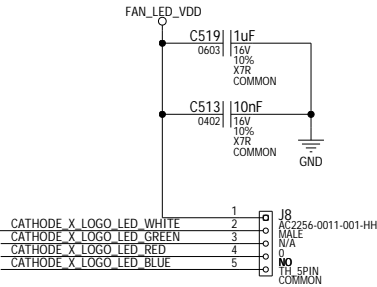


FAN B (RIGHT)

FAN A (LEFT)

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5-PIN POGO-PIN HEADERS FOR 'X/V' LEDs



- 1: 12V  
2: White  
3: GREEN  
4: RED  
5: Blue

X/V LED WHITE (3PCS)



X/V LED RED (3PCS)



X/V LED GREEN (3PCS)



X/V LED BLUE (3PCS)



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1

2

3

4

5

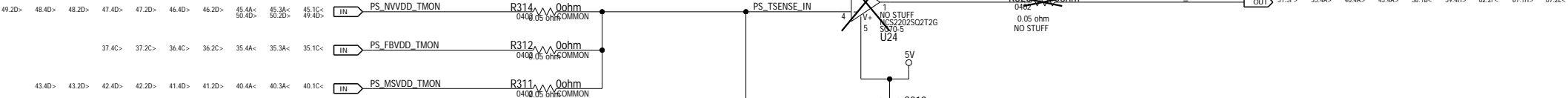
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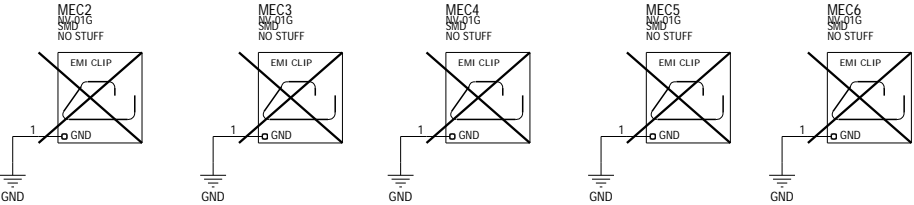
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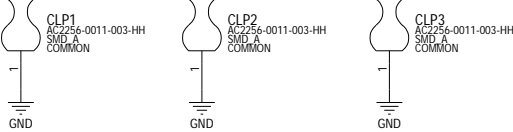


TOP: 5x EMI CLIPS

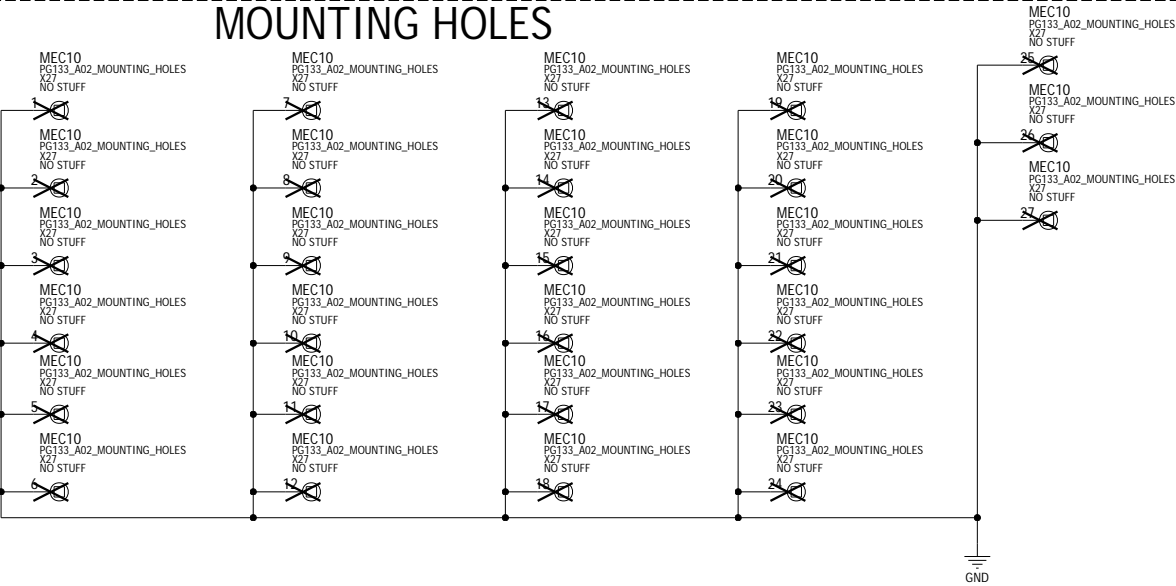
EMISTOP: 320-1764-000  
TYCO: 320-1742-000



BOT: 3x RETENTION SPRINGS



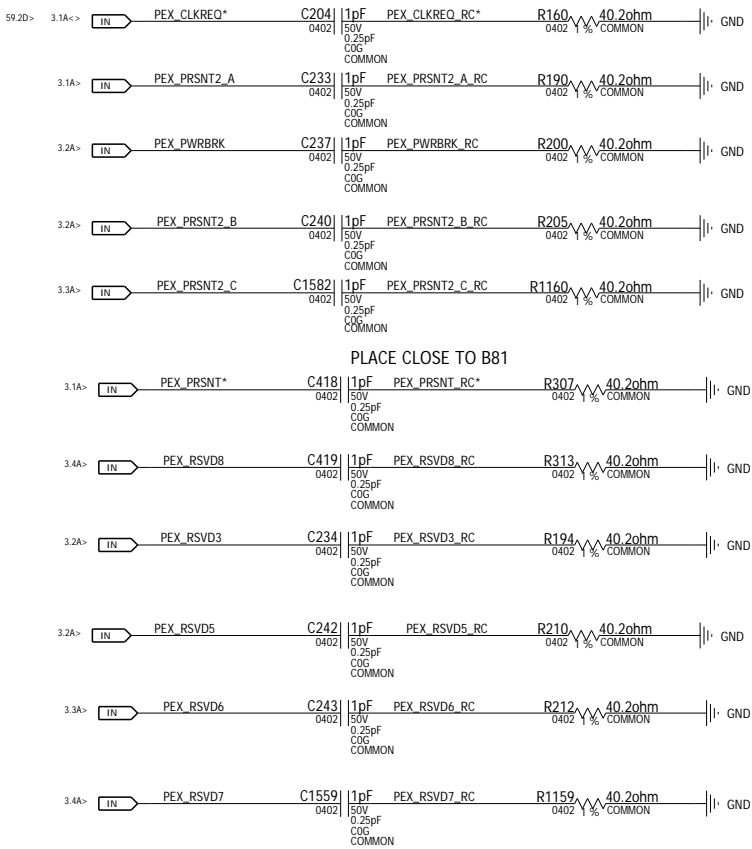
MOUNTING HOLES



ASSEMBLY	SKU30
PAGE DETAIL	MECH & VR THERMAL PROTECTION

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ASSEMBLY

PAGE DETAIL

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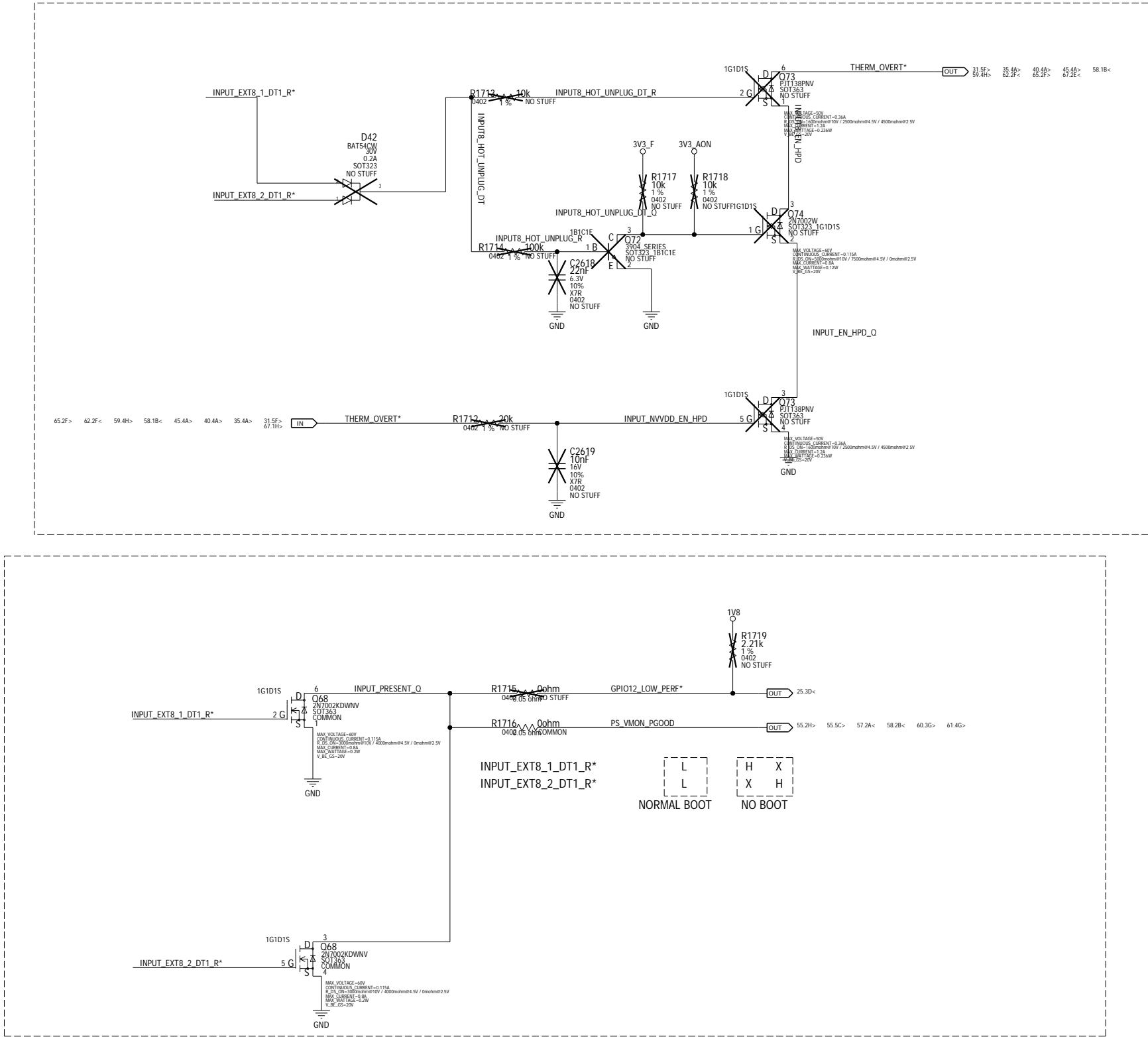
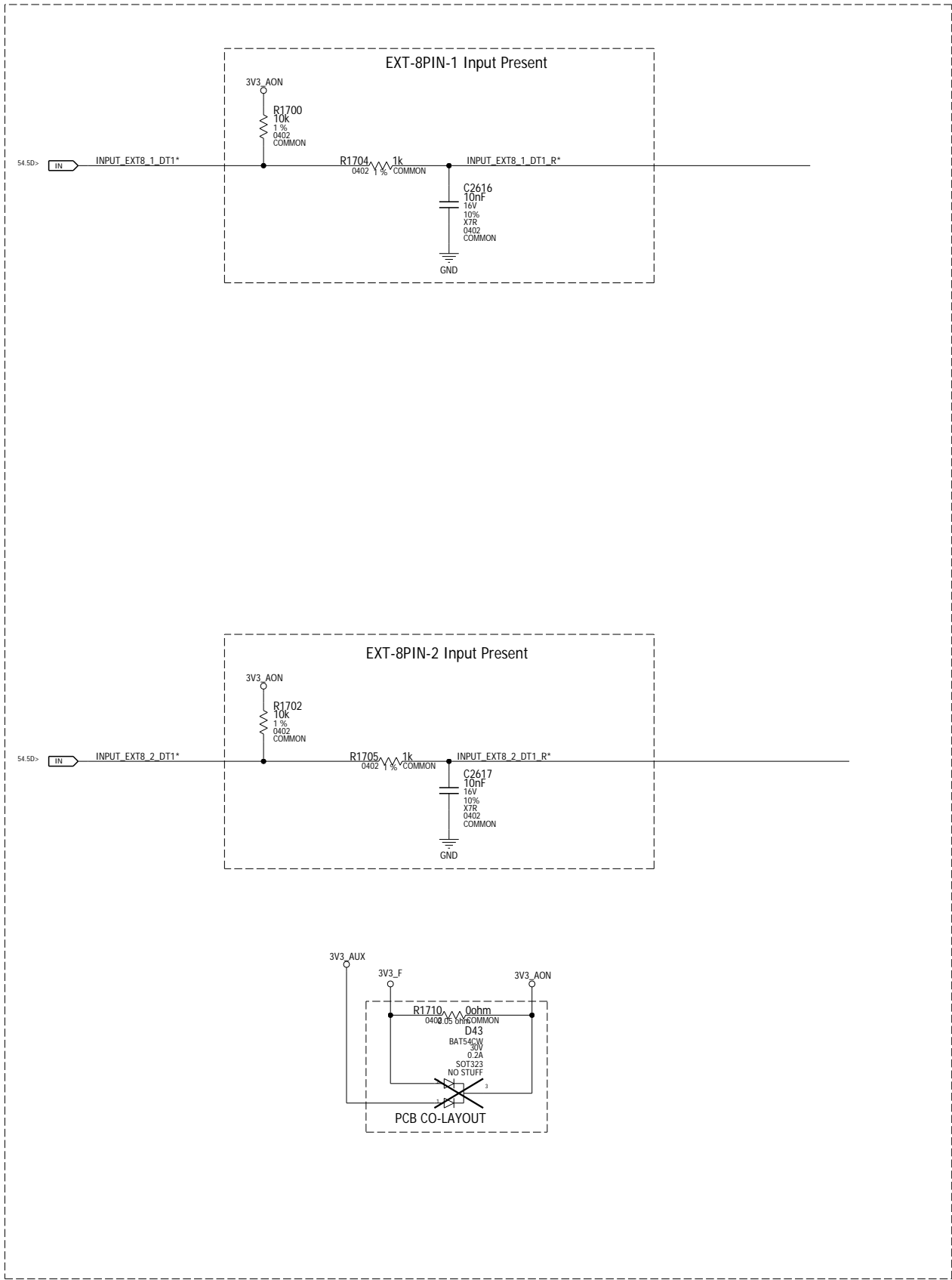
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