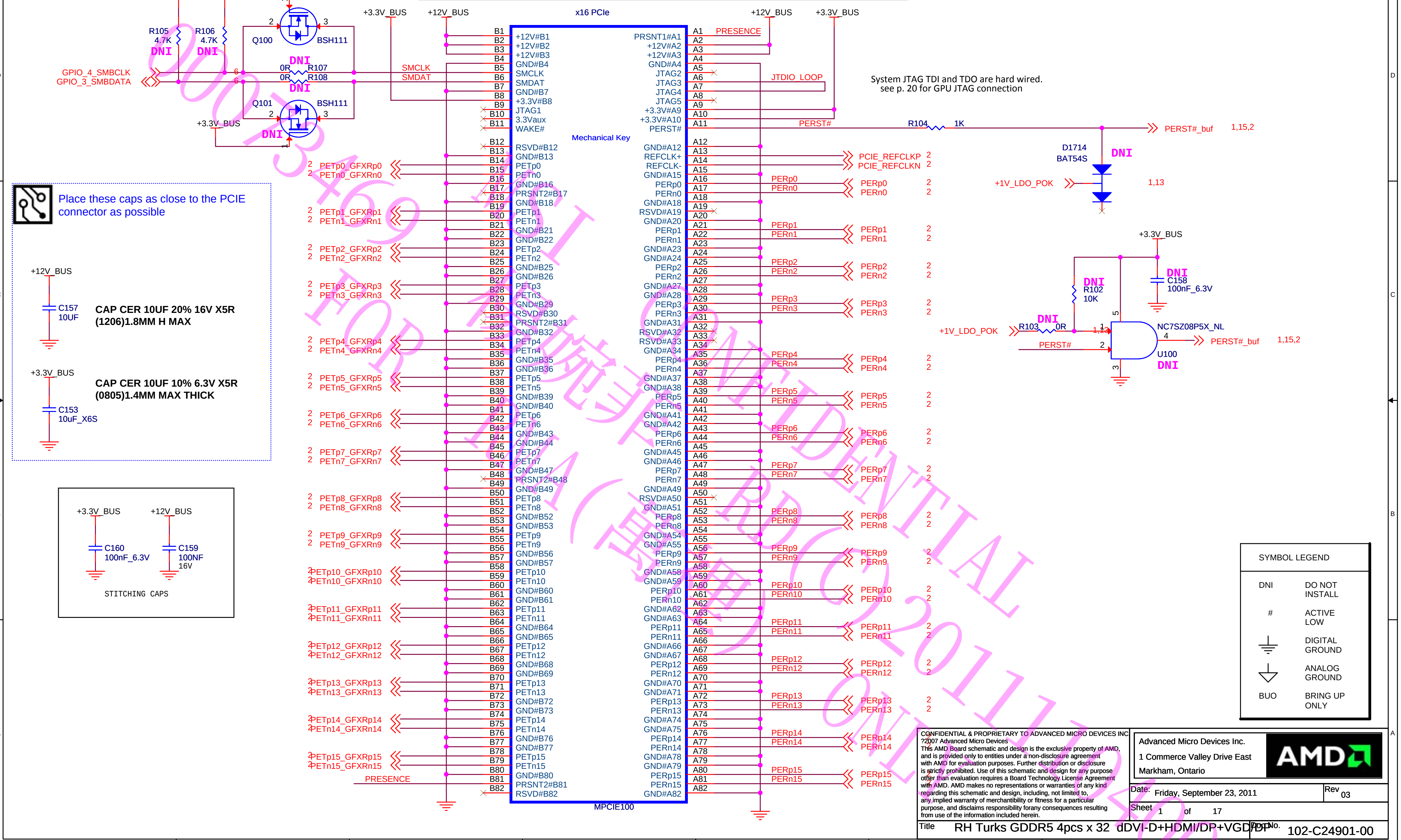
PCI-EXPRESS EDGE CONNECTOR



x16 PCIe
+3.3V_BUS
+12V_BUS
R105 4.7K DNI
R106 4.7K DNI
Q100 BSH111 DNI
Q101 BSH111 DNI
R107 0R DNI
R108 0R DNI
GPIO_4_SMBCLK
GPIO_3_SMBDATA
SMCLK
SMDAT
B1 +12V#B1
B2 +12V#B2
B3 +12V#B3
B4 GND#B4
B5 SMCLK
B6 SMDAT
B7 GND#B7
B8 +3.3V#B8
B9 JTAG1
B10 3.3Vaux
B11 WAKE#
Mechanical Key
B12 RSVD#B12
B13 GND#B13
B14 PETp0
B15 PETn0
B16 GND#B16
B17 PRSNT2#B17
B18 GND#B18
PETp0_GFXRp0
PETn0_GFXRn0
PETp1_GFXRp1 ... PETp15_GFXRp15
PETn1_GFXRn1 ... PETn15_GFXRn15
B82 RSVD#B82
B81 PRSNT2#B81
PRESENCE
A1 PRSNT1#A1
A2 +12V#A2
A3 +12V#A3
A4 GND#A4
A5 JTAG2
A6 JTAG3
A7 JTAG4
A8 JTAG5
A9 +3.3V#A9
A10 +3.3V#A10
A11 PERST#
A12 GND#A12
A13 REFCLK+
A14 REFCLK-
A15 GND#A15
A16 PERp0
A17 PERn0
A82 GND#A82
JTDIO_LOOP
System JTAG TDI and TDO are hard wired.
see p. 20 for GPU JTAG connection
PERST#
R104 1K
PERST#_buf 1,15,2
D1714 BAT54S DNI
+1V_LDO_POK 1,13
PCIE_REFCLKP 2
PCIE_REFCLKN 2
PERp0 ... PERp15
PERn0 ... PERn15
R102 10K DNI
C158 100nF_6.3V DNI
R103 0R DNI
NC7SZ08P5X_NL
U100 DNI
MPCIE100
Place these caps as close to the PCIE connector as possible
C157 10UF
CAP CER 10UF 20% 16V X5R (1206)1.8MM H MAX
C153 10uF_X6S
CAP CER 10UF 10% 6.3V X5R (0805)1.4MM MAX THICK
C160 100nF_6.3V
C159 100NF 16V
STITCHING CAPS
SYMBOL LEGEND
DNI DO NOT INSTALL
ACTIVE LOW
DIGITAL GROUND
ANALOG GROUND
BUO BRING UP ONLY
Advanced Micro Devices Inc.
1 Commerce Valley Drive East
Markham, Ontario
Date: Friday, September 23, 2011
Rev 03
Sheet 1 of 17
Title RH Turks GDDR5 4pcs x 32 dDVI-D+HDMI/DP+VGDP
Doc No. 102-C24901-00

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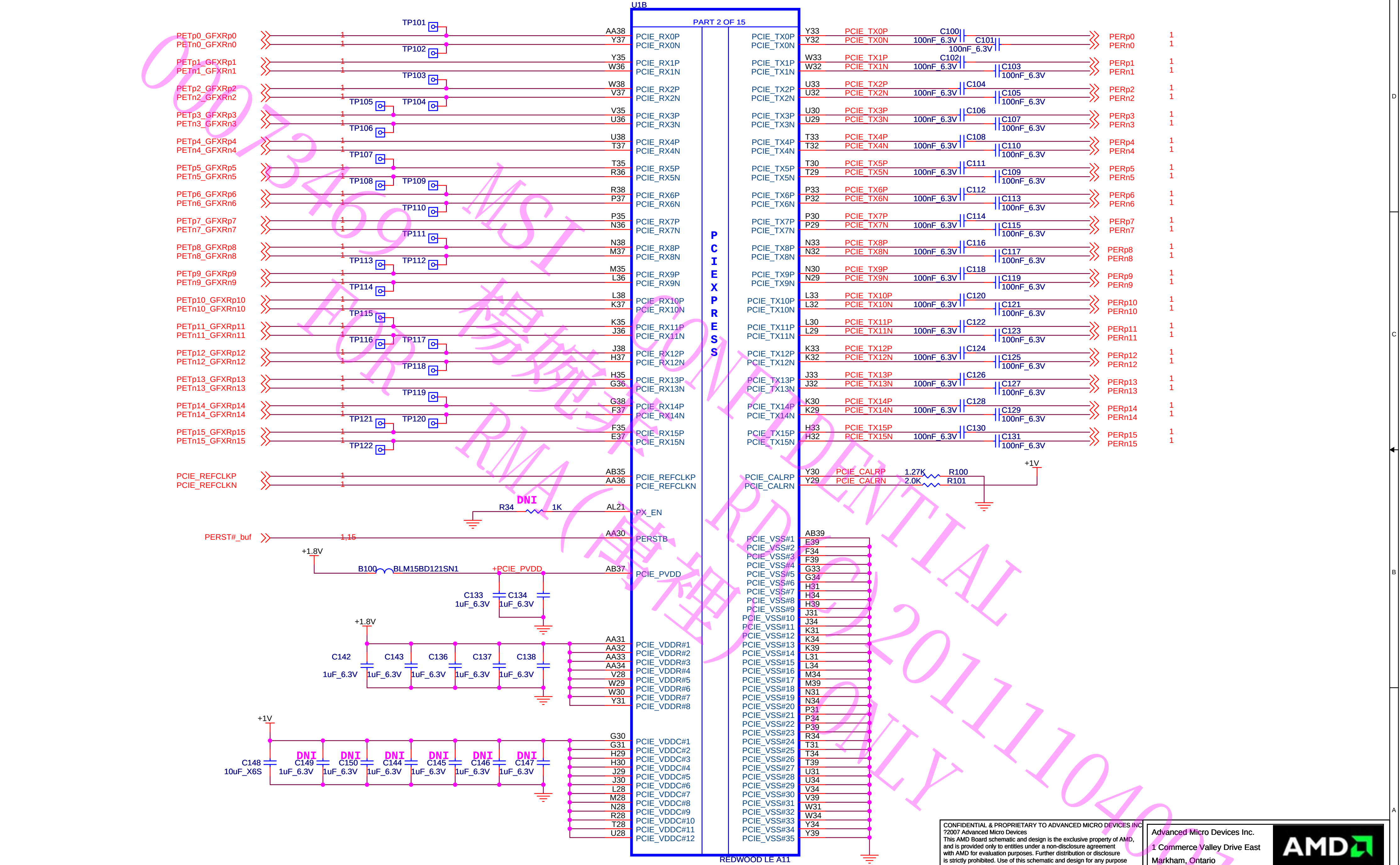

U1B
PART 2 OF 15
PCI EXPRESS
REDWOOD LE A11
PCIE_RX0P ... PCIE_RX15P
PCIE_RX0N ... PCIE_RX15N
PCIE_TX0P ... PCIE_TX15P
PCIE_TX0N ... PCIE_TX15N
PETp0_GFXRp0 ... PETp15_GFXRp15
PETn0_GFXRn0 ... PETn15_GFXRn15
PERp0 ... PERp15
PERn0 ... PERn15
TP101 ... TP122
C100 ... C131
100nF_6.3V
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CALRP
PCIE_CALRN
1.27K R100
2.0K R101
+1V
PX_EN
R34 DNI 1K
PERST#_buf
PERSTB
+1.8V
B100 BLM15BD121SN1
+PCIE_PVDD
PCIE_PVDD
C133 1uF_6.3V
C134 1uF_6.3V
C142 C143 C136 C137 C138
1uF_6.3V
PCIE_VDDR#1 ... PCIE_VDDR#8
C148 10uF_X6S
DNI
C149 C150 C144 C145 C146 C147
PCIE_VDDC#1 ... PCIE_VDDC#12
PCIE_VSS#1 ... PCIE_VSS#35

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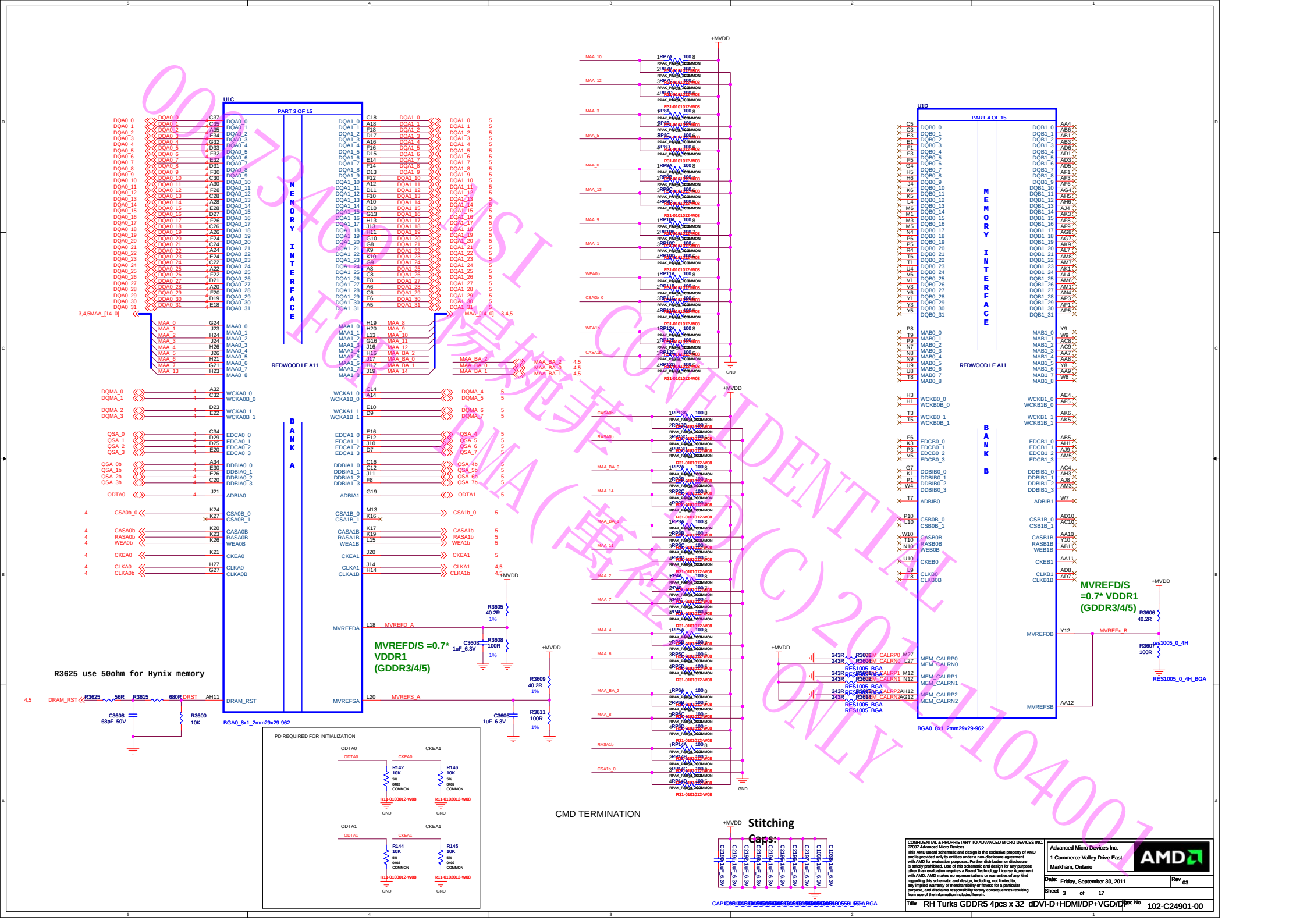
Sheet 2 of 17

Title RH Turks GDDR5 4pcs x 32 dDVI-D+HDMI/DP+VGD/DP | Doc No. 102-C24901-00



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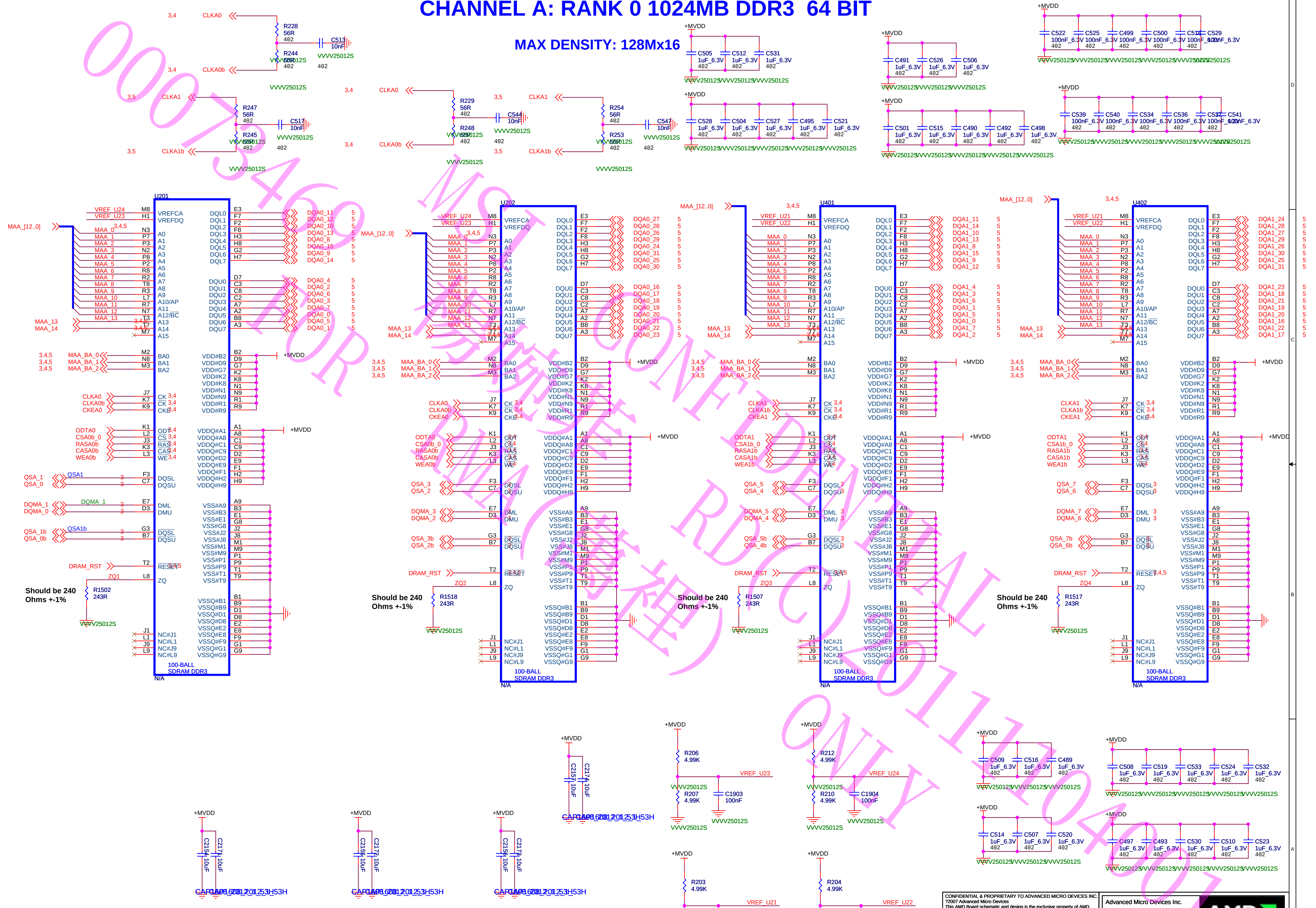
Date:	Friday, September 30, 2011
Rev	03
Sheet	3 of 17
Title	RH Turks GDDR5 4pcs x 32 dDVI-D+HDMI/DP+VGD/DP
Doc No.	102-C24901-00

CHANNEL A: RANK 0 1024MB DDR3 64 BIT

MAX DENSITY: 128Mx16



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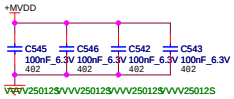
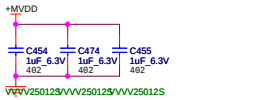
Date: Thursday, October 06, 2011 | Rev 03

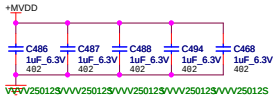
Sheet 4 of 17

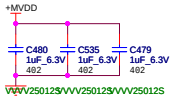
Title: RH Turks GDDR5 4pcs x 32 dDVI-D+HDMI/DP+VGD/DP | Doc No. 102-C24901-00

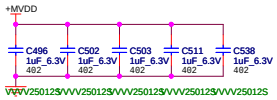
MAX DENSITY: 128Mx16

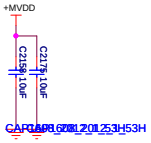


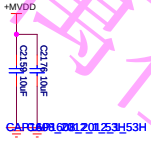


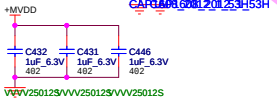


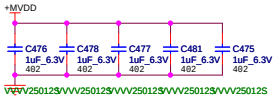


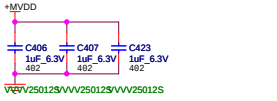


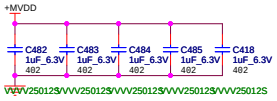


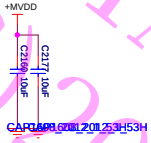


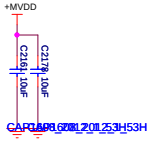












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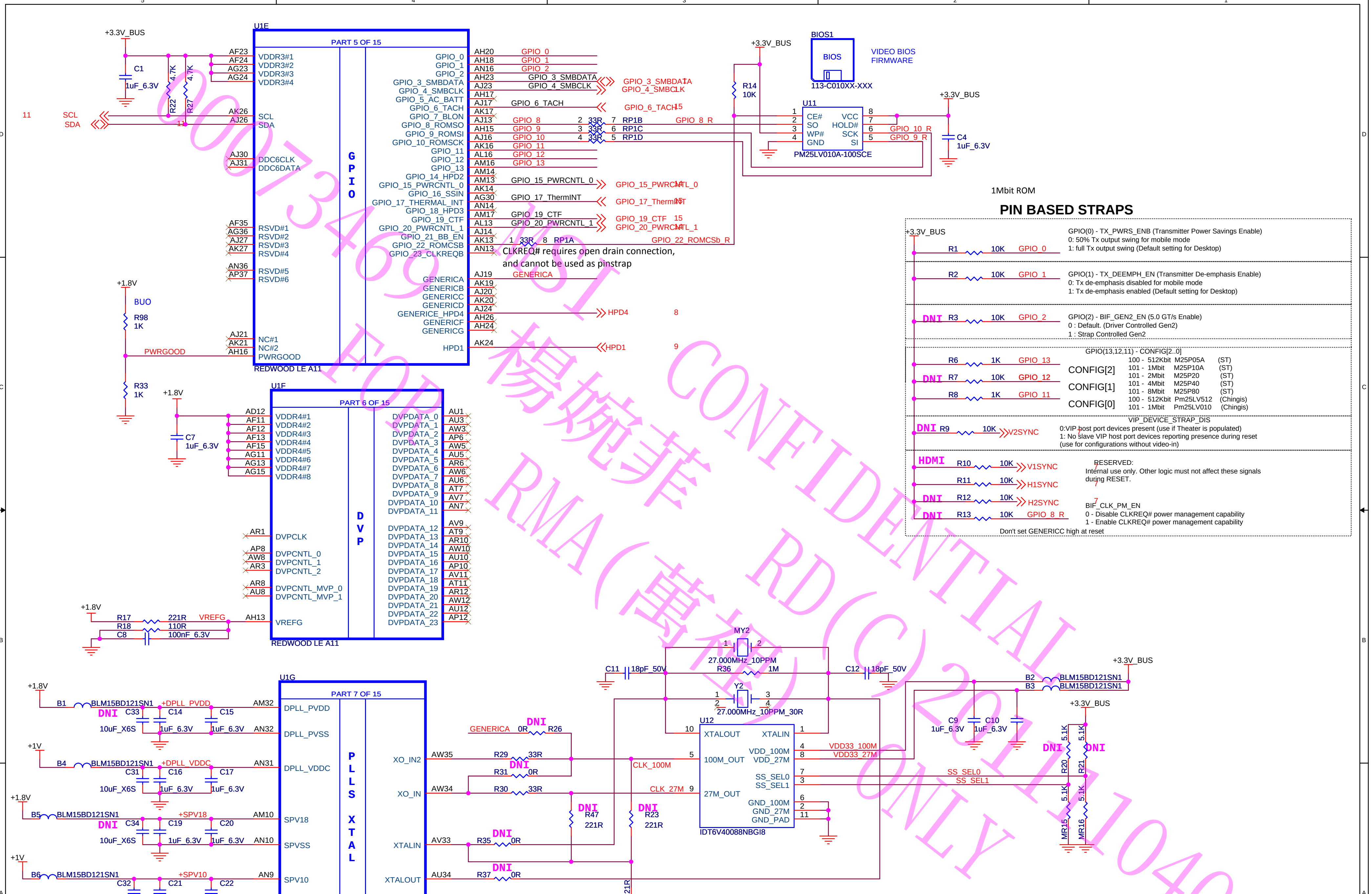
Date:	Wednesday, October 05, 2011
Rev	03
Sheet	5 of 17
Title	RH Turks GDDR5 4pcs x 32 dDVI-D+HDMI/DP+VGD/DP
Doc No.	102-C24901-00


U1E
PART 5 OF 15
GPIO
REDWOOD LE A11
BIOS1
BIOS
VIDEO BIOS FIRMWARE
113-C010XX-XXX
U11
PM25LV010A-100SCE
1Mbit ROM
CLKREQ# requires open drain connection, and cannot be used as pinstrap
PIN BASED STRAPS
GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)
GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)
GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2
GPIO(13,12,11) - CONFIG[2..0]
CONFIG[2]
CONFIG[1]
CONFIG[0]
100 - 512Kbit M25P05A (ST)
101 - 1Mbit M25P10A (ST)
101 - 2Mbit M25P20 (ST)
101 - 4Mbit M25P40 (ST)
101 - 8Mbit M25P80 (ST)
100 - 512Kbit Pm25LV512 (Chingis)
101 - 1Mbit Pm25LV010 (Chingis)
VIP_DEVICE_STRAP_DIS
0:VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset
(use for configurations without video-in)
RESERVED:
Internal use only. Other logic must not affect these signals during RESET.
BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability
Don't set GENERICC high at reset
U1F
PART 6 OF 15
DVP
REDWOOD LE A11
U1G
PART 7 OF 15
PLLS XTAL
REDWOOD LE A11
MY2
27.000MHz_10PPM
Y2
27.000MHz_10PPM_30R
U12
IDT6V40088NBGI8
route 50ohms single-ended/100ohms diff and keep short

Option	Populated	Not Populated
Crystal only	Y2, C11, C12, R36, R35, R23	U12, R26
Oscilator	Y2, C11, C12, U12	R36, R35, R23, R26

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Date:	Friday, September 23, 2011
Rev	03
Sheet	6 of 17
Title	RH Turks GDDR5 4pcs x 32 dDVI-D+HDMI/DP+VGD/DP
Doc No.	102-C24901-00

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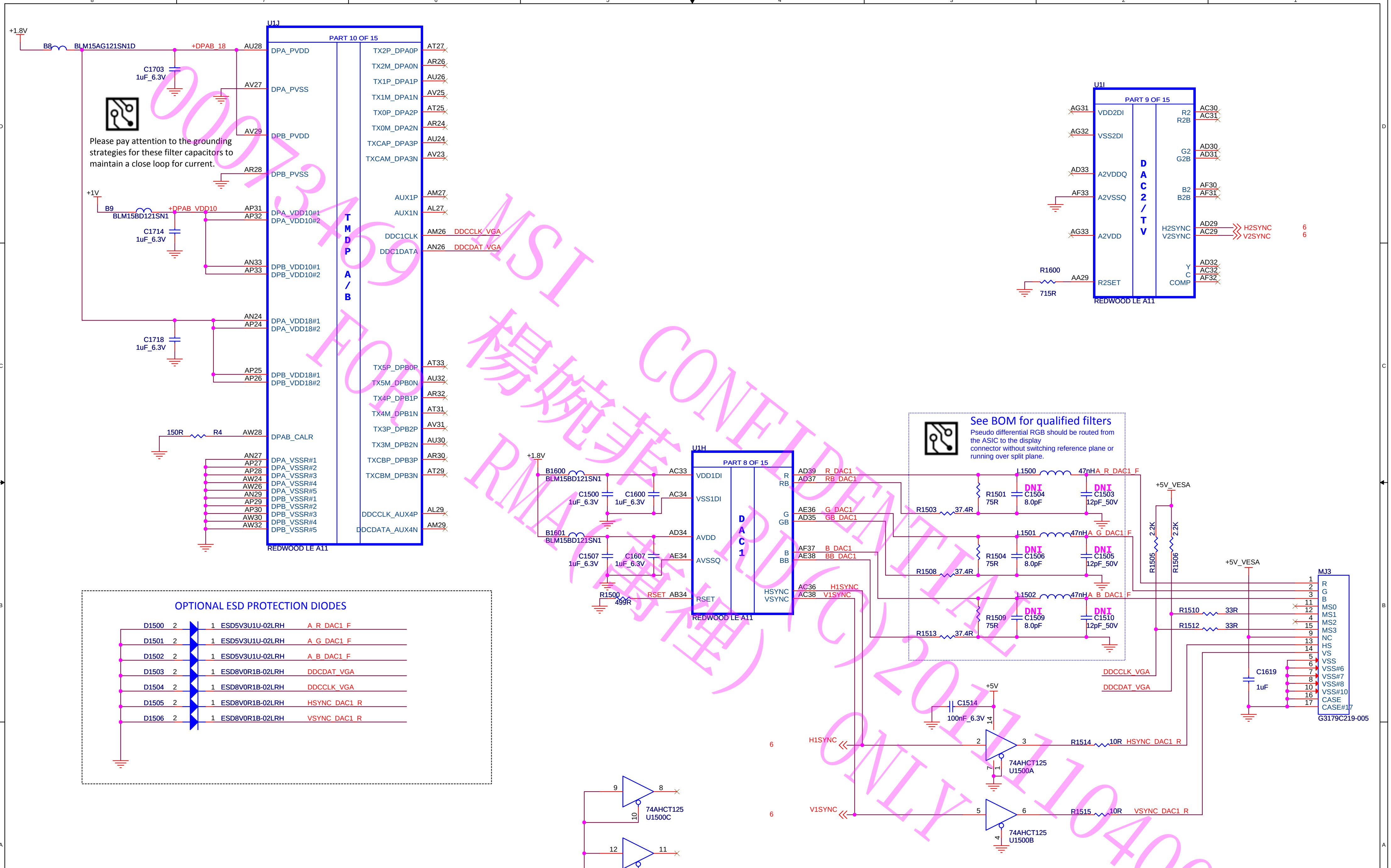
U1J
PART 10 OF 15
DPA_PVDD
DPA_PVSS
DPB_PVDD
DPB_PVSS
DPA_VDD10#1
DPA_VDD10#2
DPB_VDD10#1
DPB_VDD10#2
DPA_VDD18#1
DPA_VDD18#2
DPB_VDD18#1
DPB_VDD18#2
DPAB_CALR
TMDP A/B
TX2P_DPA0P
TX2M_DPA0N
TX1P_DPA1P
TX1M_DPA1N
TX0P_DPA2P
TX0M_DPA2N
TXCAP_DPA3P
TXCAM_DPA3N
AUX1P
AUX1N
DDC1CLK
DDC1DATA
TX5P_DPB0P
TX5M_DPB0N
TX4P_DPB1P
TX4M_DPB1N
TX3P_DPB2P
TX3M_DPB2N
TXCBP_DPB3P
TXCBM_DPB3N
DDCCLK_AUX4P
DDCDATA_AUX4N
REDWOOD LE A11
+1.8V
B8 BLM15AG121SN1D
+DPAB_18
C1703 1uF_6.3V
+1V
B9 BLM15BD121SN1
+DPAB_VDD10
C1714 1uF_6.3V
C1718 1uF_6.3V
150R R4
DDCCLK_VGA
DDCDAT_VGA
Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.
U1I
PART 9 OF 15
VDD2DI
VSS2DI
A2VDDQ
A2VSSQ
A2VDD
R2SET
DAC2/TV
R2 R2B
G2 G2B
B2 B2B
H2SYNC V2SYNC
Y C COMP
R1600 715R
H2SYNC
V2SYNC
U1H
PART 8 OF 15
VDD1DI
VSS1DI
AVDD
AVSSQ
RSET
DAC1
R RB
G GB
B BB
HSYNC VSYNC
B1600 BLM15BD121SN1
B1601 BLM15BD121SN1
C1500 1uF_6.3V
C1600 1uF_6.3V
C1507 1uF_6.3V
C1607 1uF_6.3V
R1500 499R
R_DAC1
RB_DAC1
G_DAC1
GB_DAC1
B_DAC1
BB_DAC1
H1SYNC
V1SYNC
See BOM for qualified filters
Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.
L1500 47nH A_R_DAC1_F
L1501 47nH A_G_DAC1_F
L1502 47nH A_B_DAC1_F
R1501 75R
R1504 75R
R1509 75R
DNI C1504 8.0pF
DNI C1503 12pF_50V
DNI C1506 8.0pF
DNI C1505 12pF_50V
DNI C1509 8.0pF
DNI C1510 12pF_50V
R1503 37.4R
R1508 37.4R
R1513 37.4R
+5V_VESA
R1505 2.2K
R1506 2.2K
R1510 33R
R1512 33R
C1619 1uF
MJ3
R G B MS0 MS1 MS2 MS3 NC HS VS VSS VSS#6 VSS#7 VSS#8 VSS#10 CASE CASE#17
G3179C219-005
+5V
C1514 100nF_6.3V
74AHCT125 U1500A
74AHCT125 U1500B
74AHCT125 U1500C
74AHCT125 U1500D
R1514 10R HSYNC_DAC1_R
R1515 10R VSYNC_DAC1_R
OPTIONAL ESD PROTECTION DIODES
D1500 ESD5V3U1U-02LRH A_R_DAC1_F
D1501 ESD5V3U1U-02LRH A_G_DAC1_F
D1502 ESD5V3U1U-02LRH A_B_DAC1_F
D1503 ESD8V0R1B-02LRH DDCDAT_VGA
D1504 ESD8V0R1B-02LRH DDCCLK_VGA
D1505 ESD8V0R1B-02LRH HSYNC_DAC1_R
D1506 ESD8V0R1B-02LRH VSYNC_DAC1_R

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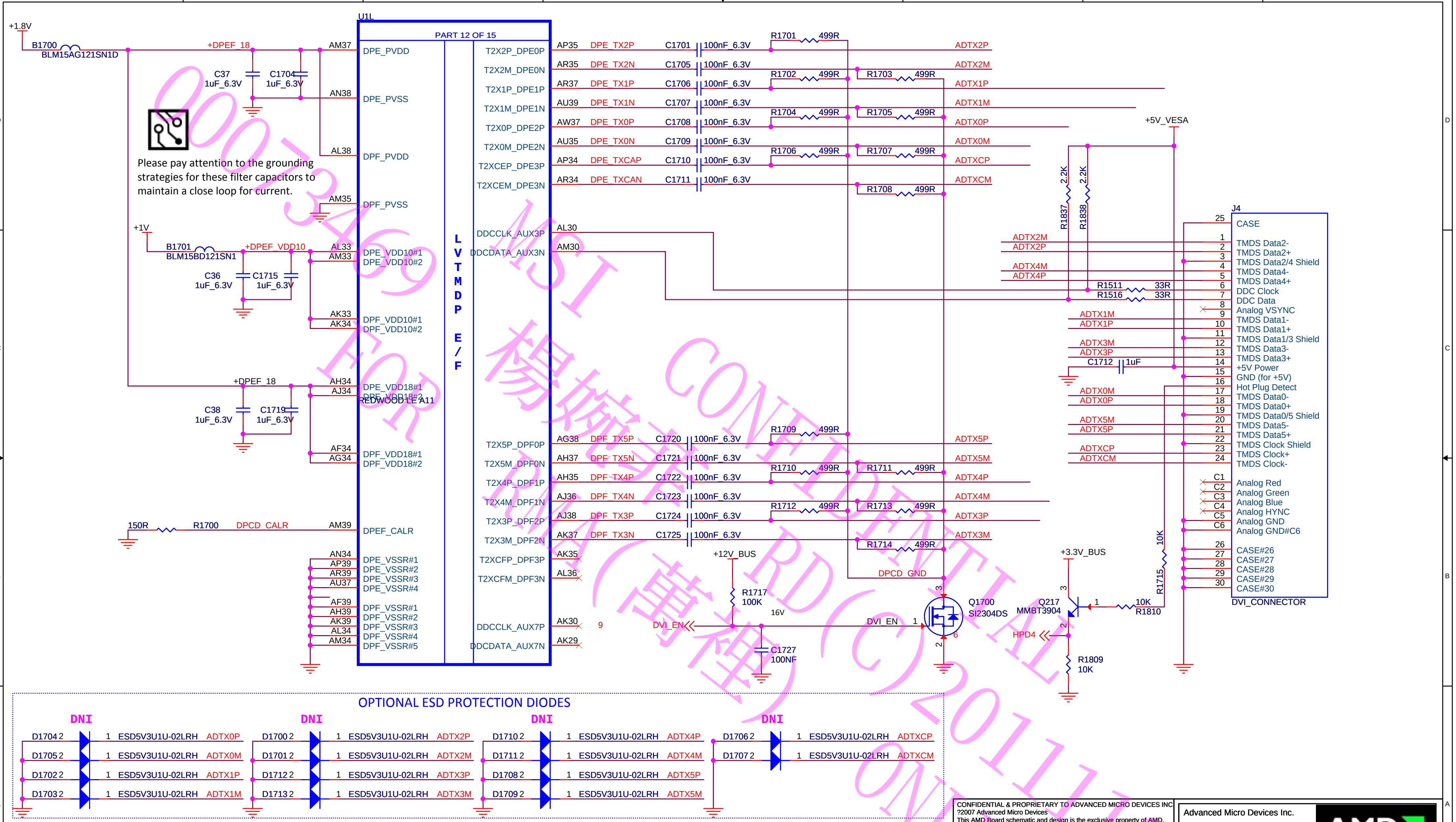
Date: Friday, September 23, 2011 | Rev 03
Sheet 7 of 17

Title: RH Turks GDDR5 4pcs x 32 dDVI-D+HDMI/DP+VGA/DP
Doc No. 102-C24901-00


U1L
PART 12 OF 15
LVTMDP E/F
DPE_PVDD
DPE_PVSS
DPF_PVDD
DPF_PVSS
DPE_VDD10#1
DPE_VDD10#2
DPF_VDD10#1
DPF_VDD10#2
DPE_VDD18#1
DPE_VDD18#2
DPF_VDD18#1
DPF_VDD18#2
DPEF_CALR
REDWOOD LE A11
T2X2P_DPE0P
T2X2M_DPE0N
T2X1P_DPE1P
T2X1M_DPE1N
T2X0P_DPE2P
T2X0M_DPE2N
T2XCEP_DPE3P
T2XCEM_DPE3N
DDCCLK_AUX3P
DDCDATA_AUX3N
T2X5P_DPF0P
T2X5M_DPF0N
T2X4P_DPF1P
T2X4M_DPF1N
T2X3P_DPF2P
T2X3M_DPF2N
T2XCFP_DPF3P
T2XCFM_DPF3N
DDCCLK_AUX7P
DDCDATA_AUX7N
+1.8V
B1700 BLM15AG121SN1D
+DPEF_18
C37 1uF_6.3V
C1704 1uF_6.3V
Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.
+1V
B1701 BLM15BD121SN1
+DPEF_VDD10
C36 1uF_6.3V
C1715 1uF_6.3V
+DPEF_18
C38 1uF_6.3V
C1719 1uF_6.3V
150R R1700 DPCD_CALR
J4
DVI_CONNECTOR
CASE
TMDS Data2-
TMDS Data2+
TMDS Data2/4 Shield
TMDS Data4-
TMDS Data4+
DDC Clock
DDC Data
Analog VSYNC
TMDS Data1-
TMDS Data1+
TMDS Data1/3 Shield
TMDS Data3-
TMDS Data3+
+5V Power
GND (for +5V)
Hot Plug Detect
TMDS Data0-
TMDS Data0+
TMDS Data0/5 Shield
TMDS Data5-
TMDS Data5+
TMDS Clock Shield
TMDS Clock+
TMDS Clock-
Analog Red
Analog Green
Analog Blue
Analog HYNC
Analog GND
Analog GND#C6
CASE#26
CASE#27
CASE#28
CASE#29
CASE#30
+5V_VESA
R1837 2.2K
R1838 2.2K
R1511 33R
R1516 33R
C1712 1uF
+12V_BUS
R1717 100K
C1727 100NF 16V
DVI_EN
Q1700 SI2304DS
DPCD_GND
+3.3V_BUS
Q217 MMBT3904
HPD4
R1810 10K
R1715 10K
R1809 10K
OPTIONAL ESD PROTECTION DIODES
DNI
ESD5V3U1U-02LRH

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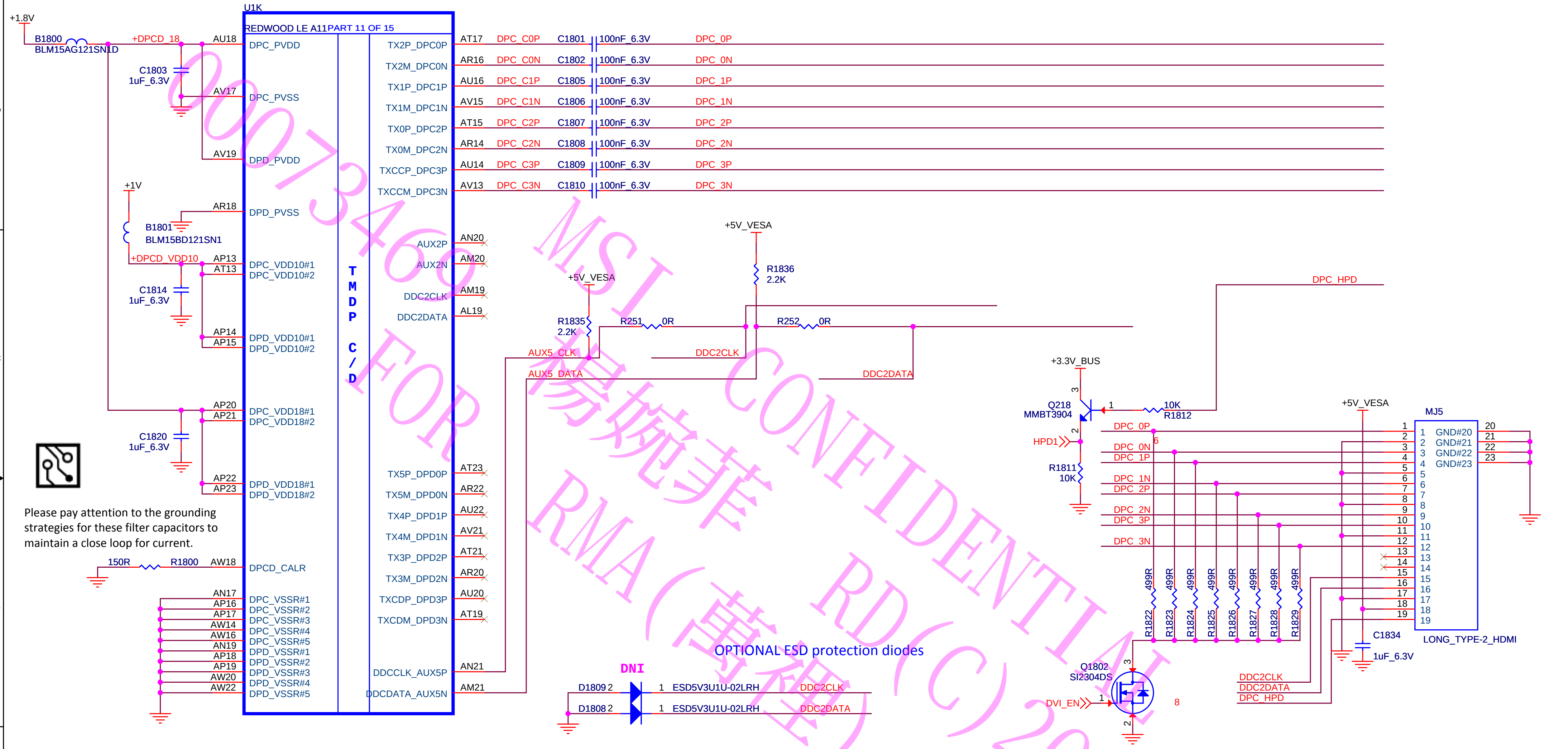

U1K
REDWOOD LE A11PART 11 OF 15
TMDP C/D
+1.8V
B1800
BLM15AG121SN1D
+DPCD_18
C1803
1uF_6.3V
AU18 DPC_PVDD
AV17 DPC_PVSS
AV19 DPD_PVDD
+1V
AR18 DPD_PVSS
B1801
BLM15BD121SN1
+DPCD_VDD10
AP13 DPC_VDD10#1
AT13 DPC_VDD10#2
C1814
1uF_6.3V
AP14 DPD_VDD10#1
AP15 DPD_VDD10#2
AP20 DPC_VDD18#1
AP21 DPC_VDD18#2
C1820
1uF_6.3V
AP22 DPD_VDD18#1
AP23 DPD_VDD18#2
150R R1800 AW18 DPCD_CALR
AN17 DPC_VSSR#1
AP16 DPC_VSSR#2
AP17 DPC_VSSR#3
AW14 DPC_VSSR#4
AW16 DPC_VSSR#5
AN19 DPD_VSSR#1
AP18 DPD_VSSR#2
AP19 DPD_VSSR#3
AW20 DPD_VSSR#4
AW22 DPD_VSSR#5
TX2P_DPC0P AT17 DPC_C0P C1801 100nF_6.3V DPC_0P
TX2M_DPC0N AR16 DPC_C0N C1802 100nF_6.3V DPC_0N
TX1P_DPC1P AU16 DPC_C1P C1805 100nF_6.3V DPC_1P
TX1M_DPC1N AV15 DPC_C1N C1806 100nF_6.3V DPC_1N
TX0P_DPC2P AT15 DPC_C2P C1807 100nF_6.3V DPC_2P
TX0M_DPC2N AR14 DPC_C2N C1808 100nF_6.3V DPC_2N
TXCCP_DPC3P AU14 DPC_C3P C1809 100nF_6.3V DPC_3P
TXCCM_DPC3N AV13 DPC_C3N C1810 100nF_6.3V DPC_3N
AUX2P AN20
AUX2N AM20
DDC2CLK AM19
DDC2DATA AL19
TX5P_DPD0P AT23
TX5M_DPD0N AR22
TX4P_DPD1P AU22
TX4M_DPD1N AV21
TX3P_DPD2P AT21
TX3M_DPD2N AR20
TXCDP_DPD3P AU20
TXCDM_DPD3N AT19
DDCCLK_AUX5P AN21
DDCDATA_AUX5N AM21
+5V_VESA
R1835
2.2K
R251 0R
R252 0R
R1836
2.2K
AUX5_CLK
AUX5_DATA
DDC2CLK
DDC2DATA
DPC_HPD
+3.3V_BUS
Q218
MMBT3904
10K
R1812
HPD1
R1811
10K
DPC_0P DPC_0N DPC_1P DPC_1N DPC_2P DPC_2N DPC_3P DPC_3N
R1822 R1823 R1824 R1825 R1826 R1827 R1828 R1829
499R
Q1802
SI2304DS
DVI_EN
C1834
1uF_6.3V
DDC2CLK
DDC2DATA
DPC_HPD
MJ5
GND#20 GND#21 GND#22 GND#23
LONG_TYPE-2_HDMI
OPTIONAL ESD protection diodes
DNI
D1809 ESD5V3U1U-02LRH DDC2CLK
D1808 ESD5V3U1U-02LRH DDC2DATA

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

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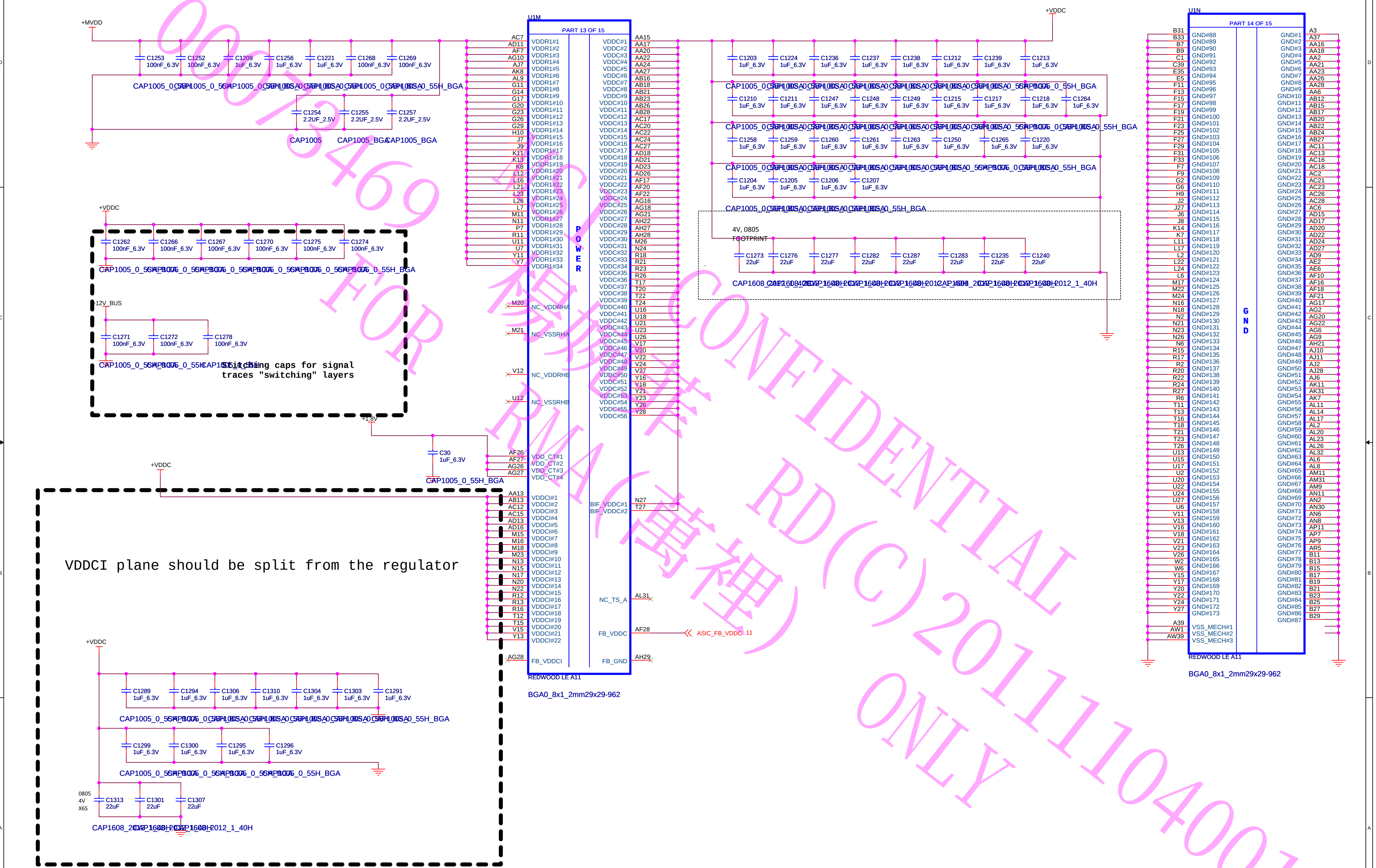

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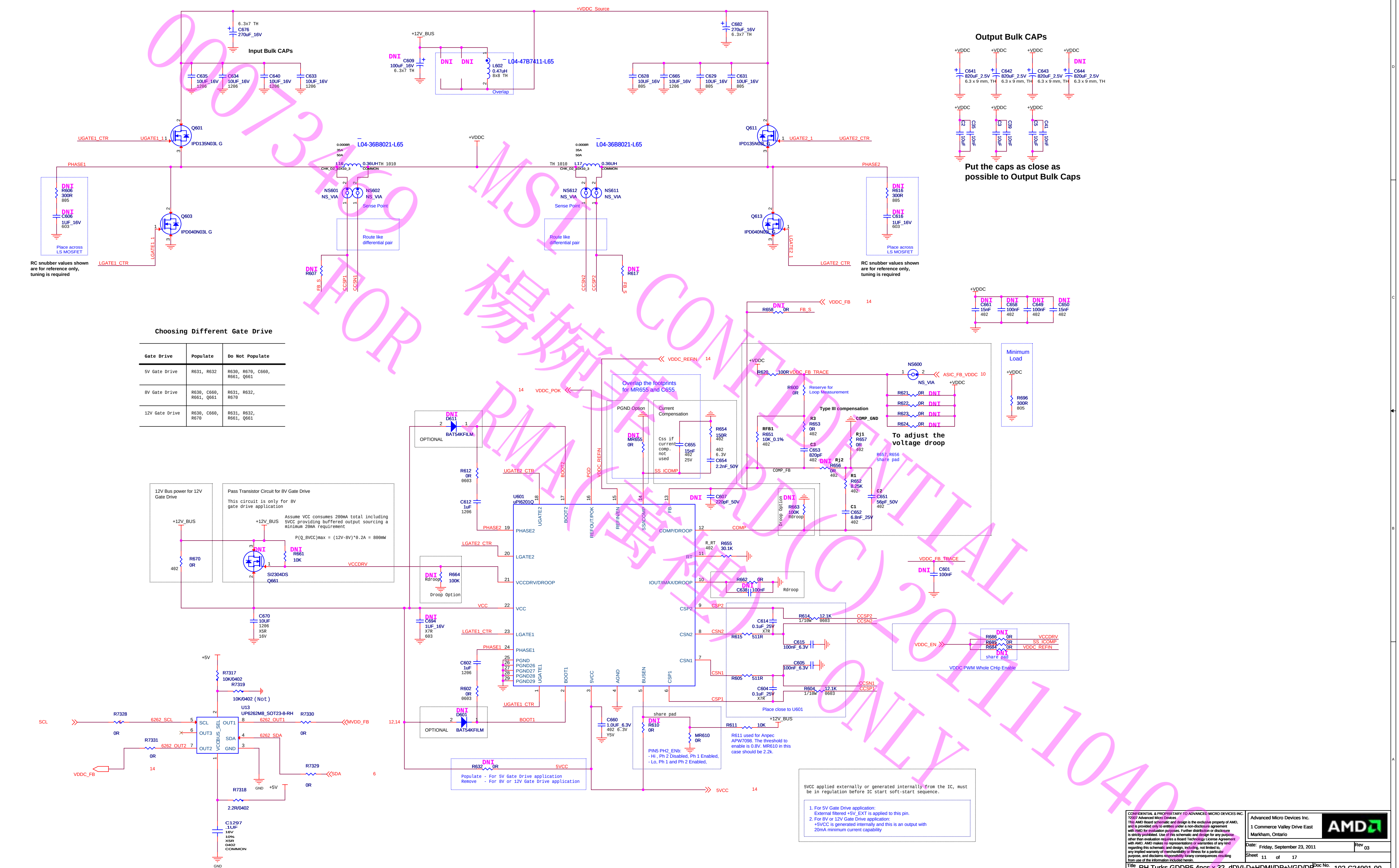

Input Bulk CAPs
Output Bulk CAPs
Put the caps as close as possible to Output Bulk Caps
+VDDC_Source
+12V_BUS
+VDDC
L04-47B7411-L65
L04-36B8021-L65
Overlap
Sense Point
Route like differential pair
Place across LS MOSFET
RC snubber values shown are for reference only, tuning is required
UGATE1_CTR
UGATE2_CTR
LGATE1_CTR
LGATE2_CTR
PHASE1
PHASE2
Q601 IPD135N03L G
Q611 IPD135N03L G
Q603 IPD040N03L G
Q613 IPD040N03L G
VDDC_FB
VDDC_REFIN
VDDC_POK
ASIC_FB_VDDC
NS_VIA
Minimum Load
Overlap the footprints for MR655 and C655
PGND Option
Current Compensation
Css if current comp. not used
Type III compensation
To adjust the voltage droop
R657,R656 share pad
Reserve for Loop Measurement
OPTIONAL
BAT54KFILM
U601 uP6201Q
PHASE2
LGATE2
VCCDRV/DROOP
VCC
LGATE1
PHASE1
PGND
COMP/DROOP
RT
IOUT/IMAX/DROOP
CSP2
CSN2
CSN1
UGATE2
BOOT2
REFOUT/POK
REFIN/EN
SS/ICOMP
FB
UGATE1
BOOT1
5VCC
AGND
BUSEN
CSP1
Droop Option
Rdroop
Place close to U601
12V Bus power for 12V Gate Drive
Pass Transistor Circuit for 8V Gate Drive
This circuit is only for 8V gate drive application
Assume VCC consumes 200mA total including 5VCC providing buffered output sourcing a minimum 20mA requirement
P(Q_8VCC)max = (12V-8V)*0.2A = 800mW
SI2304DS Q661
VCCDRV
VDDC_EN
VDDC PWM Whole Chip Enable
share pad
PIN5 PH2_ENb:
- Hi , Ph 2 Disabled, Ph 1 Enabled.
- Lo, Ph 1 and Ph 2 Enabled.
R611 used for Anpec APW7098. The threshold to enable is 0.8V. MR610 in this case should be 2.2k.
Populate - For 5V Gate Drive application
Remove - For 8V or 12V Gate Drive application
5VCC applied externally or generated internally from the IC, must be in regulation before IC start soft-start sequence.
1. For 5V Gate Drive application: External filtered +5V_EXT is applied to this pin.
2. For 8V or 12V Gate Drive application: +5VCC is generated internally and this is an output with 20mA minimum current capability
U13 UP6262M8_SOT23-8-RH
SCL
SDA
VDDC_FB
MVDD_FB

Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661

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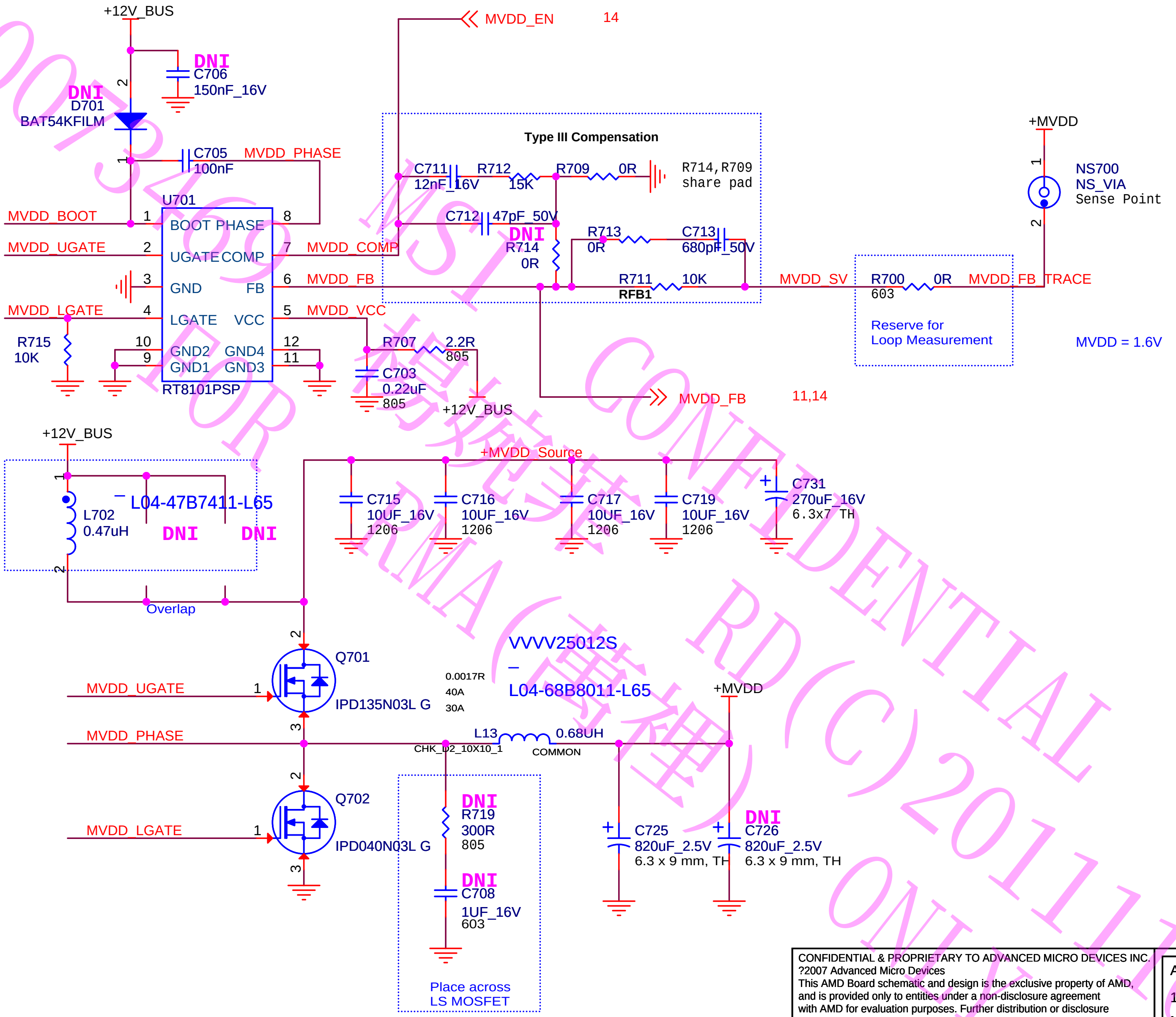

+12V_BUS
DNI
C706
150nF_16V
DNI
D701
BAT54KFILM
C705
100nF
MVDD_PHASE
MVDD_EN
14
Type III Compensation
C711
12nF_16V
R712
15K
R709
0R
R714,R709
share pad
C712
47pF_50V
DNI
R714
0R
R713
0R
C713
680pF_50V
R711
10K
RFB1
MVDD_SV
R700
0R
603
MVDD_FB_TRACE
Reserve for
Loop Measurement
+MVDD
NS700
NS_VIA
Sense Point
MVDD = 1.6V
U701
MVDD_BOOT
MVDD_UGATE
MVDD_LGATE
BOOT PHASE
UGATE COMP
GND FB
LGATE VCC
GND2 GND4
GND1 GND3
RT8101PSP
MVDD_COMP
MVDD_FB
MVDD_VCC
R715
10K
R707
2.2R
805
C703
0.22uF
805
+12V_BUS
MVDD_FB
11,14
+12V_BUS
L702
0.47uH
L04-47B7411-L65
DNI
DNI
Overlap
+MVDD_Source
C715
10UF_16V
1206
C716
10UF_16V
1206
C717
10UF_16V
1206
C719
10UF_16V
1206
C731
270uF_16V
6.3x7 TH
Q701
IPD135N03L G
MVDD_UGATE
MVDD_PHASE
MVDD_LGATE
Q702
IPD040N03L G
0.0017R
40A
30A
VVVV25012S
L04-68B8011-L65
+MVDD
L13
0.68UH
CHK_D2_10X10_1
COMMON
DNI
R719
300R
805
DNI
C708
1UF_16V
603
Place across
LS MOSFET
C725
820uF_2.5V
6.3 x 9 mm, TH
DNI
C726
820uF_2.5V
6.3 x 9 mm, TH

RC snubber values shown are for reference only, tuning is required

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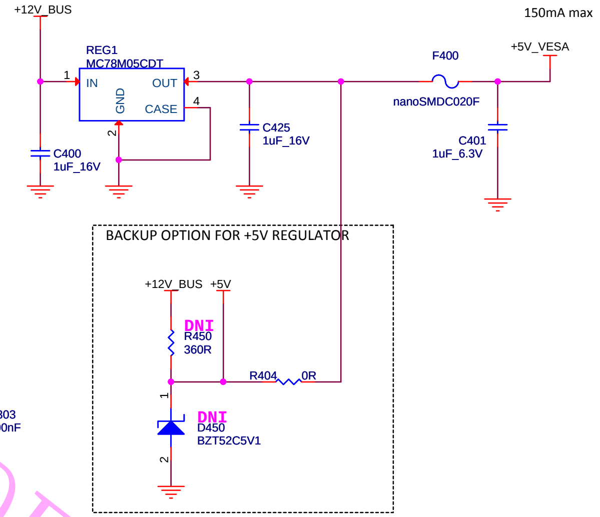
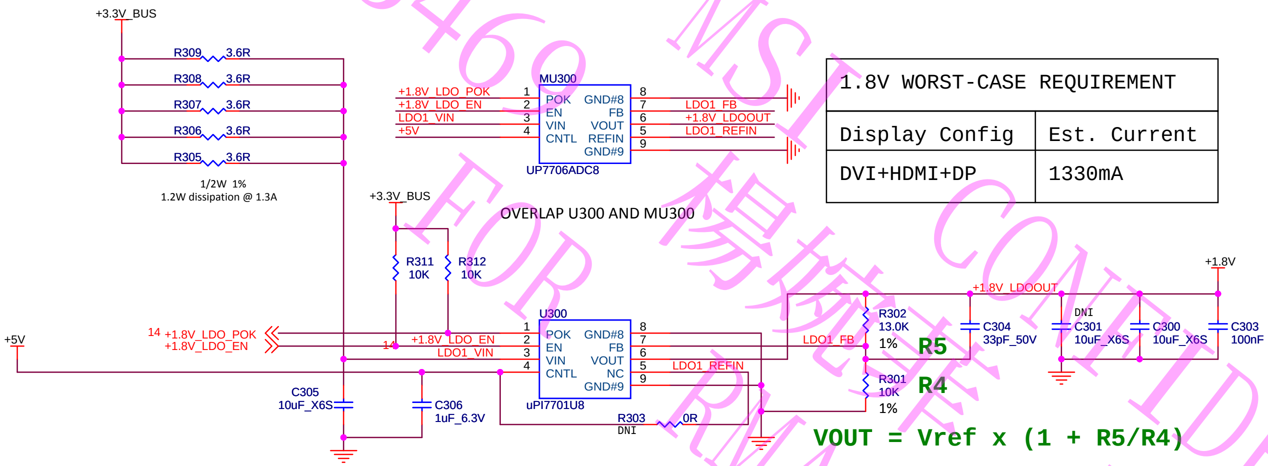
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

Regulator for +5V and +5V_VESA
Iout max = 150mA (VGA+DVI+HDMI)



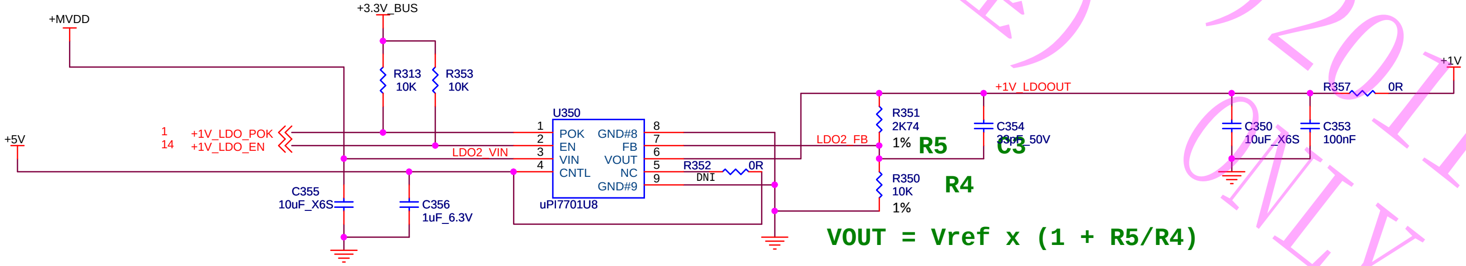
1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA



+3.3V_BUS
R309 3.6R
R308 3.6R
R307 3.6R
R306 3.6R
R305 3.6R
1/2W 1%
1.2W dissipation @ 1.3A
MU300
+1.8V_LDO_POK
+1.8V_LDO_EN
LDO1_VIN
+5V
POK
EN
VIN
CNTL
GND#8
FB
VOUT
REFIN
GND#9
LDO1_FB
+1.8V_LDOOUT
LDO1_REFIN
UP7706ADC8
+3.3V_BUS
OVERLAP U300 AND MU300
R311 10K
R312 10K
U300
+5V
+1.8V_LDO_POK
+1.8V_LDO_EN
uPI7701U8
NC
C305
10uF_X6S
C306
1uF_6.3V
R303
DNI
0R
+1.8V_LDOOUT
+1.8V
R302
13.0K
1%
R5
R301
10K
1%
R4
C304
33pF_50V
DNI
C301
10uF_X6S
C300
10uF_X6S
C303
100nF
VOUT = Vref x (1 + R5/R4)

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA



+MVDD
+3.3V_BUS
R313 10K
R353 10K
+5V
+1V_LDO_POK
+1V_LDO_EN
LDO2_VIN
U350
POK
EN
VIN
CNTL
GND#8
FB
VOUT
NC
GND#9
uPI7701U8
R352
DNI
0R
C355
10uF_X6S
C356
1uF_6.3V
LDO2_FB
+1V_LDOOUT
R351
2K74
1%
R5
R350
10K
1%
R4
C354
33pF_50V
C3
C350
10uF_X6S
C353
100nF
R357
0R
+1V
VOUT = Vref x (1 + R5/R4)

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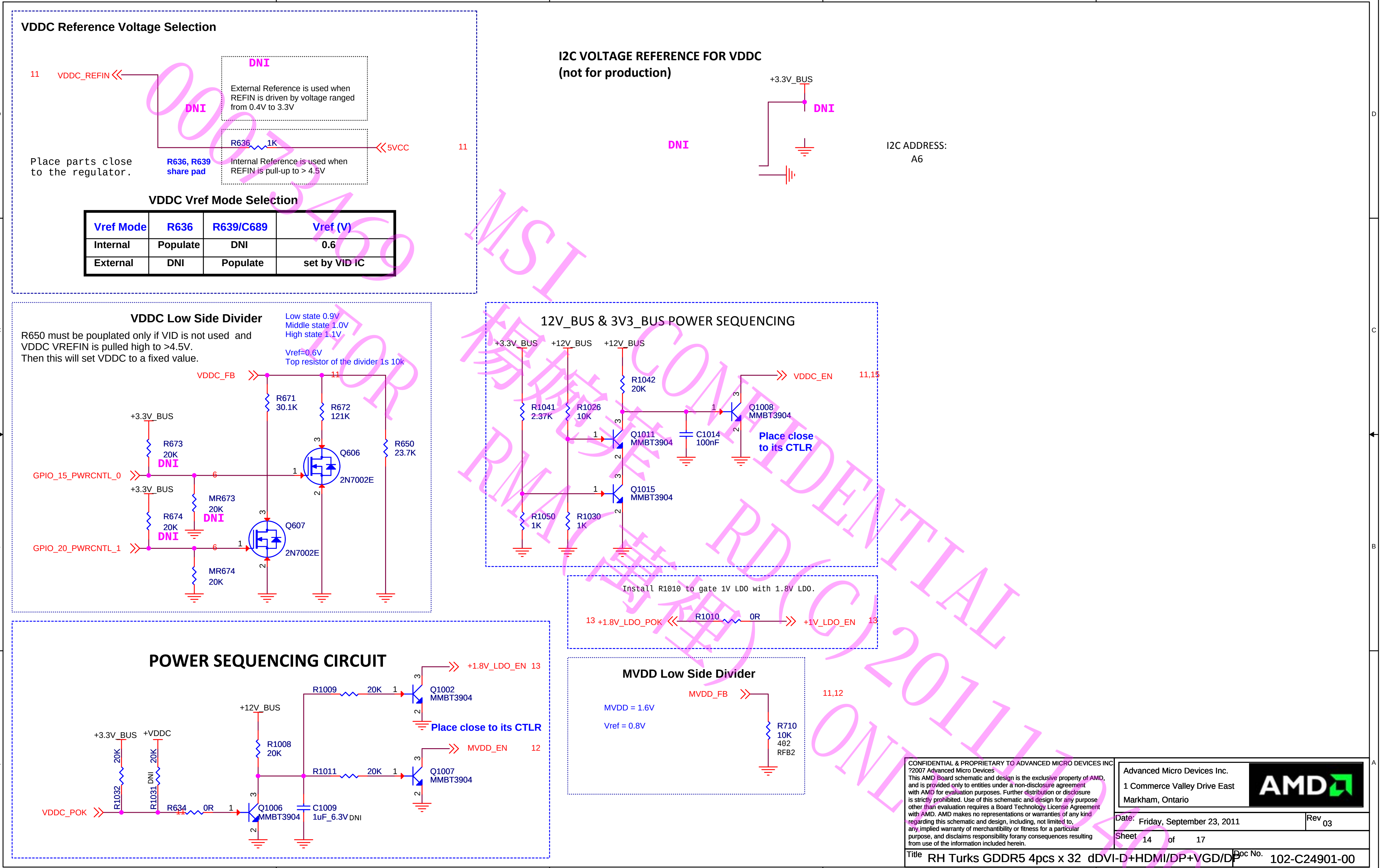

VDDC Reference Voltage Selection
11 VDDC_REFIN
DNI
External Reference is used when REFIN is driven by voltage ranged from 0.4V to 3.3V
DNI
R636 1K
5VCC 11
Internal Reference is used when REFIN is pull-up to > 4.5V
Place parts close to the regulator.
R636, R639 share pad
I2C VOLTAGE REFERENCE FOR VDDC (not for production)
+3.3V_BUS
DNI
DNI
I2C ADDRESS: A6
VDDC Low Side Divider
R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.
Low state 0.9V
Middle state 1.0V
High state 1.1V
Vref=0.6V
Top resistor of the divider 1s 10k
VDDC_FB 11
R671 30.1K
R672 121K
R650 23.7K
+3.3V_BUS
R673 20K DNI
GPIO_15_PWRCNTL_0
Q606 2N7002E
+3.3V_BUS
MR673 20K DNI
R674 20K DNI
Q607 2N7002E
GPIO_20_PWRCNTL_1
MR674 20K
12V_BUS & 3V3_BUS POWER SEQUENCING
+3.3V_BUS +12V_BUS +12V_BUS
R1042 20K
VDDC_EN 11,15
R1041 2.37K
R1026 10K
Q1008 MMBT3904
Q1011 MMBT3904
C1014 100nF
Place close to its CTLR
Q1015 MMBT3904
R1050 1K
R1030 1K
Install R1010 to gate 1V LDO with 1.8V LDO.
13 +1.8V_LDO_POK R1010 0R +1V_LDO_EN 13
POWER SEQUENCING CIRCUIT
+1.8V_LDO_EN 13
R1009 20K
Q1002 MMBT3904
+12V_BUS
Place close to its CTLR
R1008 20K
MVDD_EN 12
+3.3V_BUS +VDDC
R1011 20K
Q1007 MMBT3904
R1032 20K
R1031 20K DNI
VDDC_POK 11 R634 0R
Q1006 MMBT3904
C1009 1uF_6.3V DNI
MVDD Low Side Divider
MVDD_FB 11,12
MVDD = 1.6V
Vref = 0.8V
R710 10K 402 RFB2

VDDC Vref Mode Selection

Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

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Sheet 14 of 17
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Use Q203 2020002300G, R200, R249, D1719 and C3609 for cheaper fan controller. Requires big change in fan table.

2 wires DC fan control

Cheaper 2 wires fan control

Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

Critial Temperature Fault

For one time CTF use R239 47k.
For resetable CTF use R239 2k.

CTF By-pass

Place close to its CTLR

To maximize fan output during CTF trigger.

For 4-WIRE FAN ONLY

N32-1040801-H06

TOP
MEM to GPU : 4.85mil / 45ohm

TOP
Diffenential_Memory Clock
4.85 / 7.08mil 80 ohm +/- 10%

BOTTOM
Diffenential_Memory Clock
4.85 / 7.08mil 80 ohm +/- 10%

BOTTOM
MEM to GPU : 4.85mil / 45ohm

47W XT
Dual-slot
Heatsink

30W PRO
Single-slot
Heatsink

47W XT
Single-slot
Heatsink

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Sheet 15 of 17

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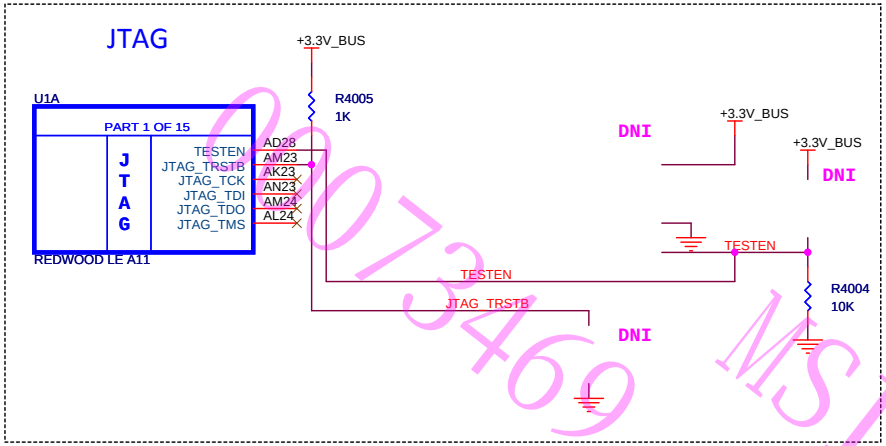
SWITCH CONNECTIONS TO PINSTRAPS



LM96163 FOR BACKUP THERMAL CONTROL

SCL/SDA PORT DEBUG ACCESS

Place connector on the back side
(easily accessible and not blocked by the heatsink).

TACH Connection is for testing and RPM measurement only

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Date: Friday, September 23, 2011 | Rev 03

Sheet 16 of 17

Title: RH Turks GDDR5 4pcs x 32 dDVI-D+HDMI/DP+VGD/DP | Doc No. 102-C24901-00

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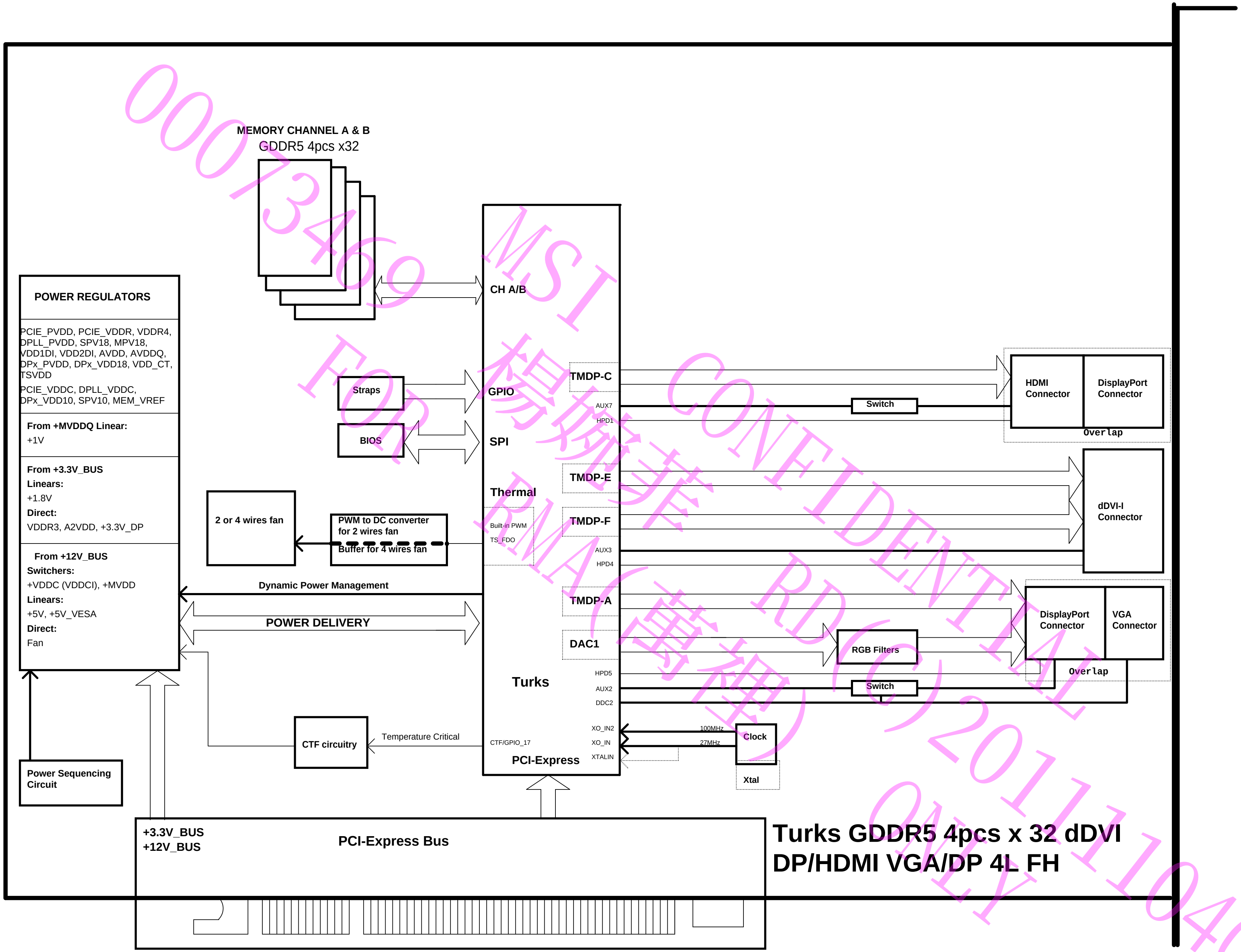
MEMORY CHANNEL A & B
GDDR5 4pcs x32
POWER REGULATORS
PCIE_PVDD, PCIE_VDDR, VDDR4, DPLL_PVDD, SPV18, MPV18, VDD1DI, VDD2DI, AVDD, AVDDQ, DPx_PVDD, DPx_VDD18, VDD_CT, TSVDD
PCIE_VDDC, DPLL_VDDC, DPx_VDD10, SPV10, MEM_VREF
From +MVDDQ Linear:
+1V
From +3.3V_BUS
Linears:
+1.8V
Direct:
VDDR3, A2VDD, +3.3V_DP
From +12V_BUS
Switchers:
+VDDC (VDDCI), +MVDD
Linears:
+5V, +5V_VESA
Direct:
Fan
Straps
BIOS
2 or 4 wires fan
PWM to DC converter for 2 wires fan
Buffer for 4 wires fan
Dynamic Power Management
POWER DELIVERY
CTF circuitry
Temperature Critical
Power Sequencing Circuit
CH A/B
GPIO
SPI
Thermal
Built-in PWM
TS_FDO
Turks
CTF/GPIO_17
PCI-Express
TMDP-C
AUX7
HPD1
TMDP-E
TMDP-F
AUX3
HPD4
TMDP-A
DAC1
HPD5
AUX2
DDC2
XO_IN2
XO_IN
XTALIN
100MHz
27MHz
Clock
Xtal
Switch
HDMI Connector
DisplayPort Connector
Overlap
dDVI-I Connector
RGB Filters
DisplayPort Connector
VGA Connector
Overlap
Switch
+3.3V_BUS
+12V_BUS
PCI-Express Bus
Turks GDDR5 4pcs x 32 dDVI DP/HDMI VGA/DP 4L FH

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Date:	Friday, September 23, 2011	Rev	03
Sheet	of	102-C24901-00	
Title	RH Turks GDDR5 4pcs x 32 dDVI-D+HDMI/DP+VGD/DP	Doc No.	17 17

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Date:	Wednesday, October 05, 2011	Rev	03
Sheet 18 of 17		Doc No. 102-C24901-00	
Title	RH Turks GDDR3 4pcs x 32 dDVI-D+HDMI/DP+VGD/DP	Custom	

00A	00A	Nov 11, 2010	1)Based on: V250-3.0
		09.22.2011	1. Change 128X8 to 128x16 P.04 2. Add FAN PWM TACH P.15 3. Add reference MLCC P.04 & 05

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