

P727-A01: G96, GB1-128, GDDR3, DL-DVI, DL-DVI/VGA, SD/HDTV

REV HISTORY

2/18 PAGE 2 add SPDIF_IN_M from PCIE's connector PIN_BA2

PAGE 15 remove DP function
PAGE 16 remove SLI function
PAGE 17 add SCART (the same as V096-3.0)
PAGE 18 add SPDIF_IN_M
PAGE 19 remove GPIO_11_SLI_SYNC0 / GPIO12_SWAPRDY / GPIO15_DP_HPD / GPIO18_DP_MODE / GPIO19_DP_CEC / GPIO22_SWAPRDY_A

add GPIO2_TV_SCART / GPIO13_TV_SCART_SEL / GPIO14_TV_SCART_SEL / GPIO20_TV_LOAD_TEST / GPIO16_SEL_HDTV_SDTV

2/20 PAGE 16 MIOB VDD from 2V5 change to 3V3_F

2/21 PAGE 20 remove J5 (HDA function), remove 2V5
PAGE 19 remove I2CD_SDA and I2CD_SCL (for DP)
remove GPIO2/GPIO13/GPIO14
PAGE 17 3V3 chnage to 3V3_F
remove SCART_TV_SEL function
remove TV_CVBS_SCART_F
PAGE 21 remove Q15, C870, R737 (for DP_hotplug_detect_E)
PAGE 22 remove 2V5 function

2/22 PAGE 22 IFPEF_RSET PULL LOW
PAGE 18 ADD U601,U602,U603,U604 for EMI
ADD MEC10, MEC11 for external FAN holder
ADD FM7, FM8

2/22 PAGE 14 add bridge R1103,R1104,R1105,R1106 for EMI
PAGE 18 rename U514-U515,and U601-U604 to EM1 -EM8

PAGE SUMMARY:

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- Page 2: PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS
- Page 3: FBA MEMORY INTERFACE, GPU NVVDD & FBVDDQ DECOUPLING CAPS
- Page 4: FBA 16/32Mx32 GDDR3 MEMORIES, FBA COMMAND BUS PU'S, FBA CLK TERMS
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- Page 19: POWER SUPPLY LINEARS: 5V, DDC5V, IFP PLLVDD, IFP IOVDD, MIO VDD, 3V3 FILTER, 12V FILTER
- Page 20: POWER SUPPLY: FBVDDQ SINGLE PHASE SWITCHER
- Page 21: POWER SUPPLY: PEX_VDD SINGLE PHASE SWITCHER
- Page 22: POWER SUPPLY: NVVDD DUAL PHASE SWITCHER
- Page 23: POWER SUPPLY: NVVDD VOLTAGE SELECTION

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10727-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	600-10727-0000-100	G96-A02, 650/800MHz 256MB 16MX32 GDDR3, DVI DVI HDTV-Out
2	SKU001	600-10727-0001-100	G96-300, 550/800MHz 256MB 16MX32 GDDR3, DVI DVI HDTV-Out
3	SKU002	600-10727-0002-100	G96-300, 550/800MHz 256MB 16MX32 GDDR3, DVI DVI
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PAGE DETAIL	TABLE OF CONTENTS

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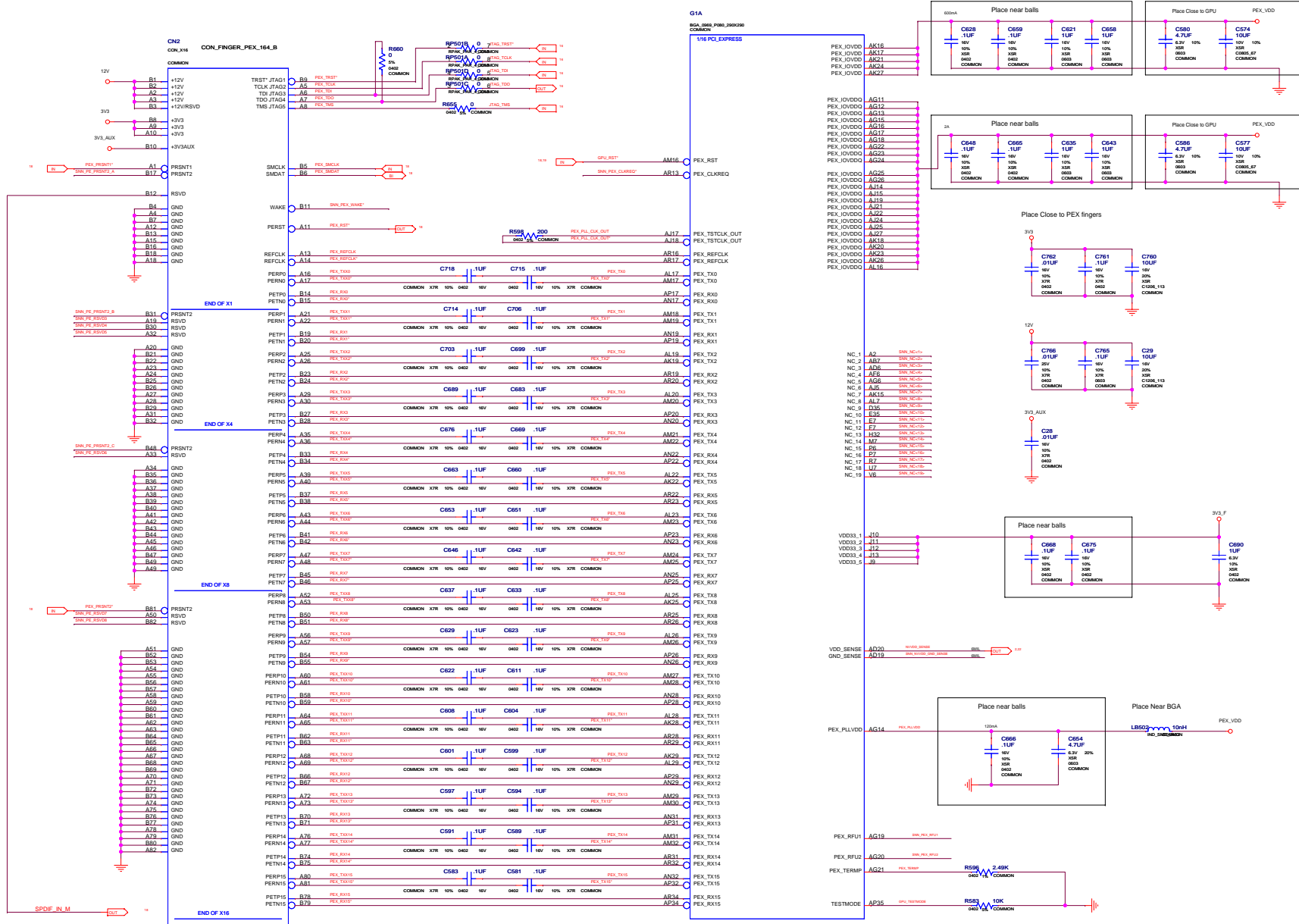
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16X PEX INTERFACE



	NET	DIFFER	NU_IMPEDANCE	NU_CRITICAL
10	PEX 1001A	PEX 1001A	100000	+
11	PEX 1001B	PEX 1001B	100000	+
12	PEX 1001C	PEX 1001C	100000	+
13	PEX 1001D	PEX 1001D	100000	+
14	PEX 1001E	PEX 1001E	100000	+
15	PEX 1001F	PEX 1001F	100000	+
16	PEX 1001G	PEX 1001G	100000	+
17	PEX 1001H	PEX 1001H	100000	+
18	PEX 1001I	PEX 1001I	100000	+
19	PEX 1001J	PEX 1001J	100000	+
20	PEX 1001K	PEX 1001K	100000	+
21	PEX 1001L	PEX 1001L	100000	+
22	PEX 1001M	PEX 1001M	100000	+
23	PEX 1001N	PEX 1001N	100000	+
24	PEX 1001O	PEX 1001O	100000	+
25	PEX 1001P	PEX 1001P	100000	+
26	PEX 1001Q	PEX 1001Q	100000	+
27	PEX 1001R	PEX 1001R	100000	+
28	PEX 1001S	PEX 1001S	100000	+
29	PEX 1001T	PEX 1001T	100000	+
30	PEX 1001U	PEX 1001U	100000	+
31	PEX 1001V	PEX 1001V	100000	+
32	PEX 1001W	PEX 1001W	100000	+
33	PEX 1001X	PEX 1001X	100000	+
34	PEX 1001Y	PEX 1001Y	100000	+
35	PEX 1001Z	PEX 1001Z	100000	+
36	PEX 1002A	PEX 1002A	100000	+
37	PEX 1002B	PEX 1002B	100000	+
38	PEX 1002C	PEX 1002C	100000	+
39	PEX 1002D	PEX 1002D	100000	+
40	PEX 1002E	PEX 1002E	100000	+
41	PEX 1002F	PEX 1002F	100000	+
42	PEX 1002G	PEX 1002G	100000	+
43	PEX 1002H	PEX 1002H	100000	+
44	PEX 1002I	PEX 1002I	100000	+
45	PEX 1002J	PEX 1002J	100000	+
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57	PEX 1002V	PEX 1002V	100000	+
58	PEX 1002W	PEX 1002W	100000	+
59	PEX 1002X	PEX 1002X	100000	+
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61	PEX 1002Z	PEX 1002Z	100000	+
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63	PEX 1003B	PEX 1003B	100000	+
64	PEX 1003C	PEX 1003C	100000	+
65	PEX 1003D	PEX 1003D	100000	+
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67	PEX 1003F	PEX 1003F	100000	+
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97	PEX 1004J	PEX 1004J	100000	+
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99	PEX 1004L	PEX 1004L	100000	+
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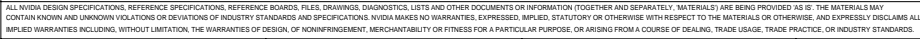
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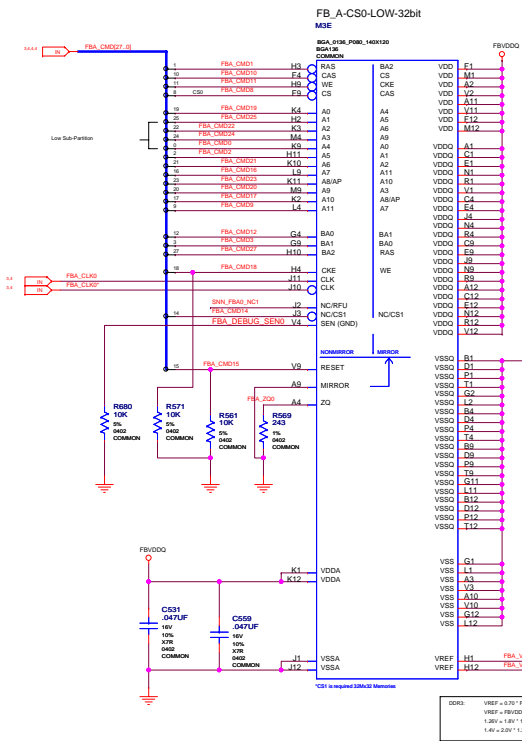


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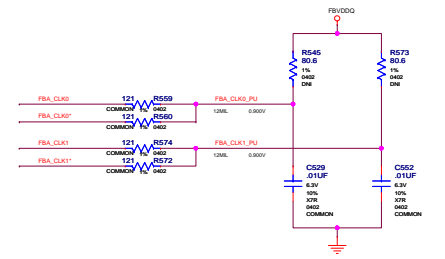
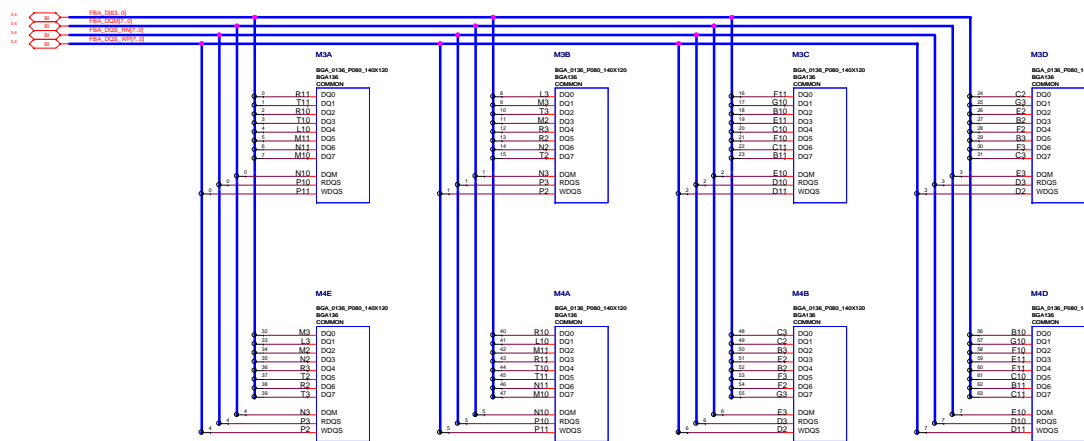
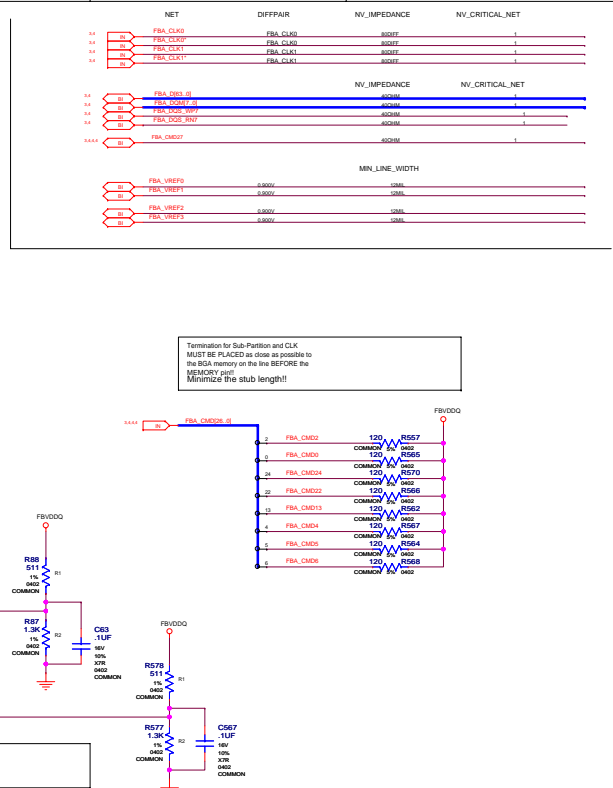
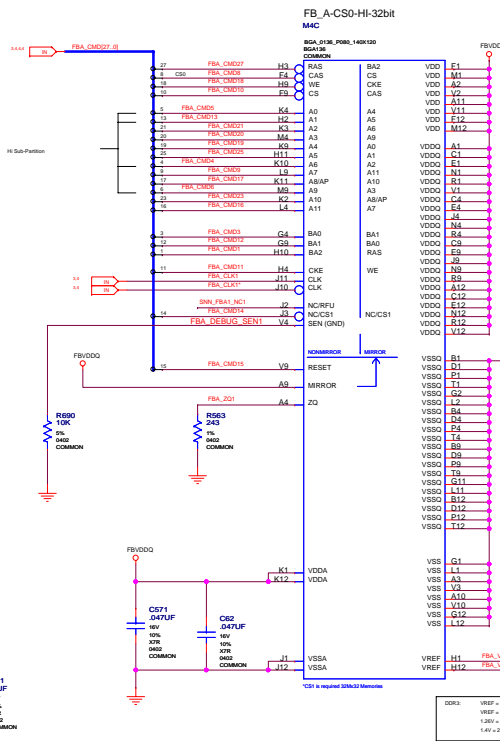
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS



FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3



FBA Partition	
136BGA CMD Mapping	
CMD	ADDR
CM01	RA0*
CM10	CA0*
CM11	VE*
CM18	CNE
CM15	RESET/ODT
CM09	CS0*
CM19	Ar0a
CM05	Ar1a
CM02	Ar0a
CM04	Ar0a
CM03	Ar0a
CM02	Ar0a
CM04	Ar0a
CM06	Ar0a
CM05	Ar0a
CM13	Ar0a
CM01	Ar0b
CM16	Ar0c*
CM03	Ar0b
CM20	Ar0b
CM17	Ar10
CM09	Ar11a
CM14	Ar12a
CM12	BA0
CM03	BA1
CM27	BA1



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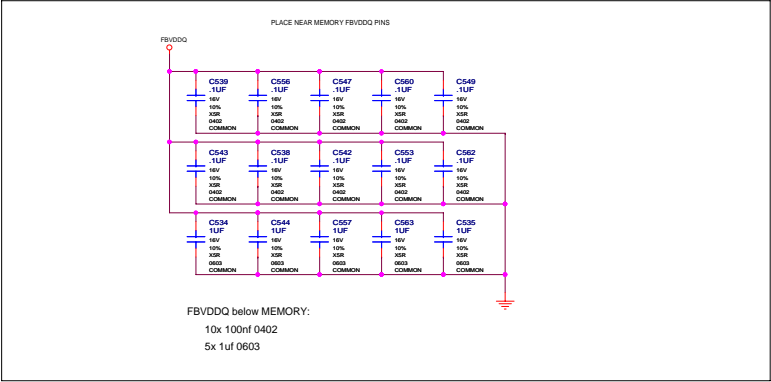
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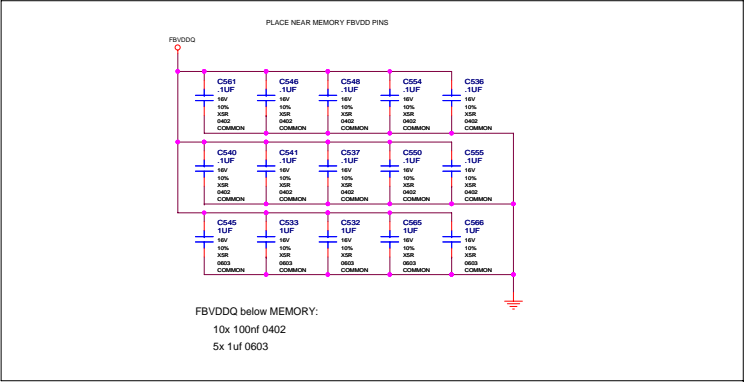
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PAGE DETAIL	FBA 16/32Mx32 GDDR3 MEMORIES, FBA COMMAND BUS PUTS, FBA CLK TERMS

FRAME BUFFER: PARTITION A DECOUPLING

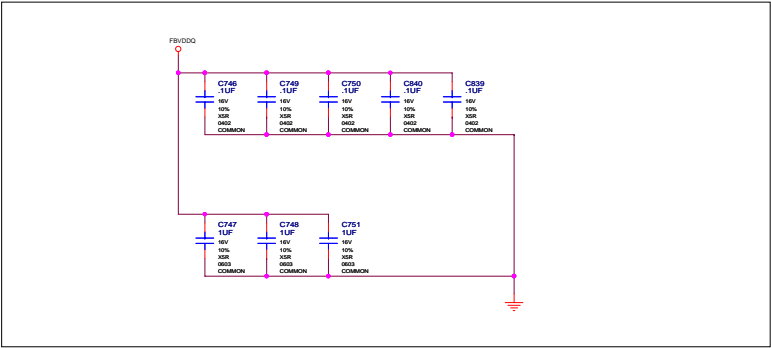
Decoupling for FBA 0..31



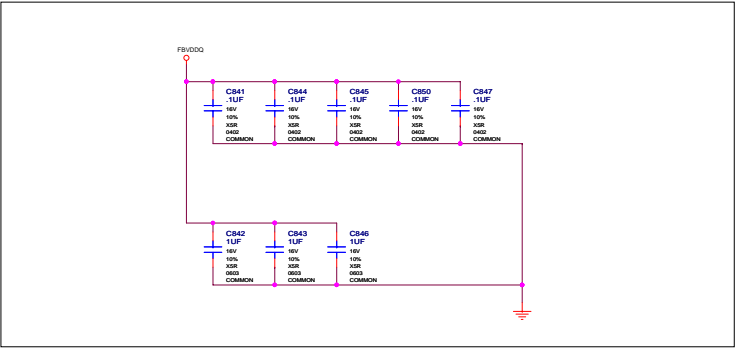
Decoupling for FBA 32..63



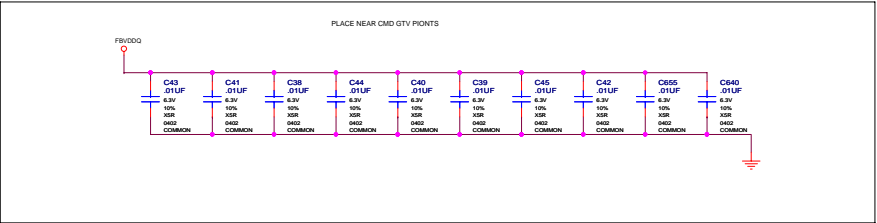
Decoupling for FBA A1 0..31



Decoupling for FBA A1 0..31



Return path coupling GND/FBVDDQ for FBA

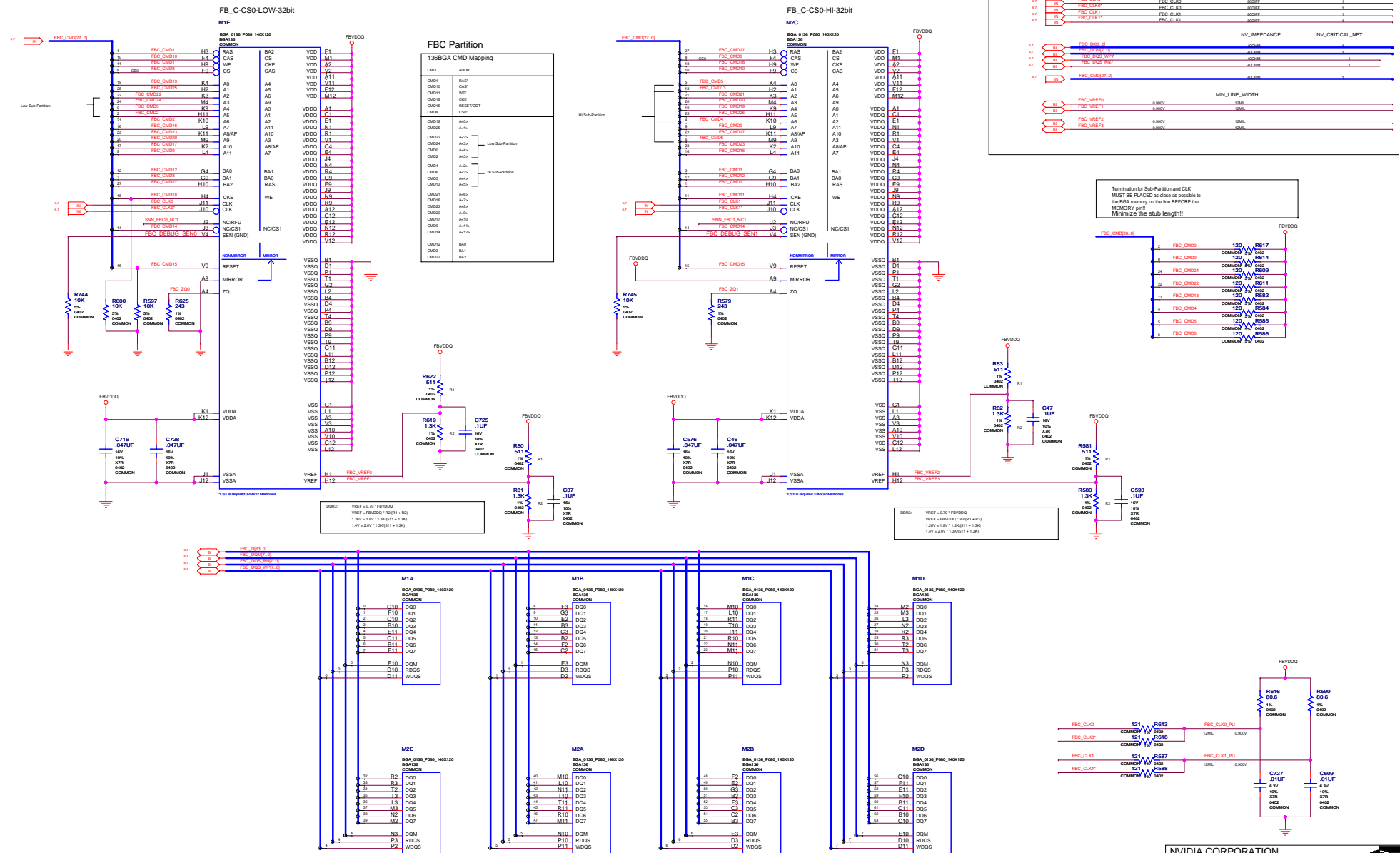


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ASSEMBLY	BASE LEVEL "GENERIC" SCHEMATIC ONLY. COMMON & NO. 3100FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

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FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS P/U'S, FBC CLK TERMS

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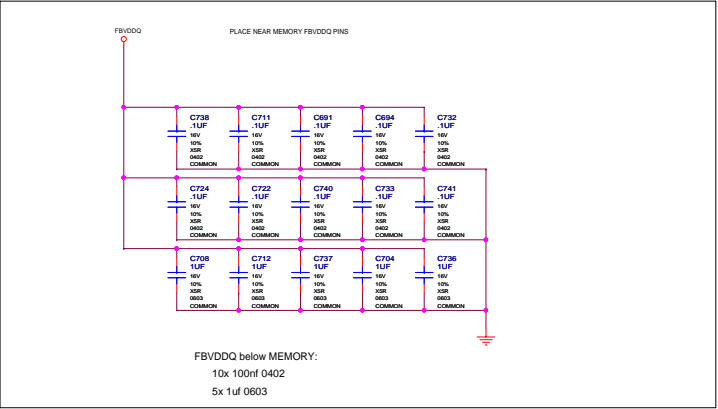
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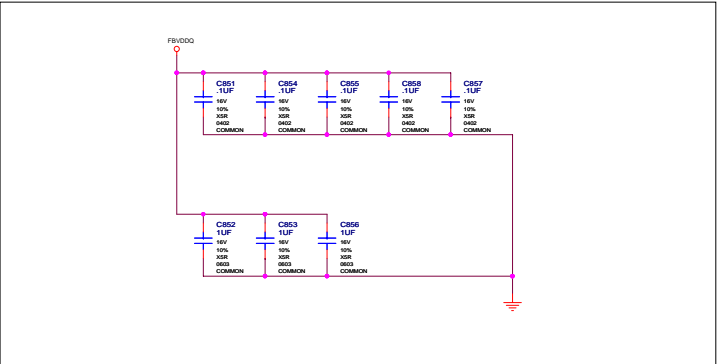
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FRAMEBUFFER: PARTITION C DECOUPLING

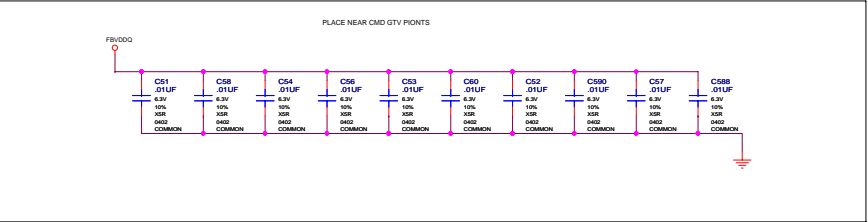
Decoupling for FBC 0..31



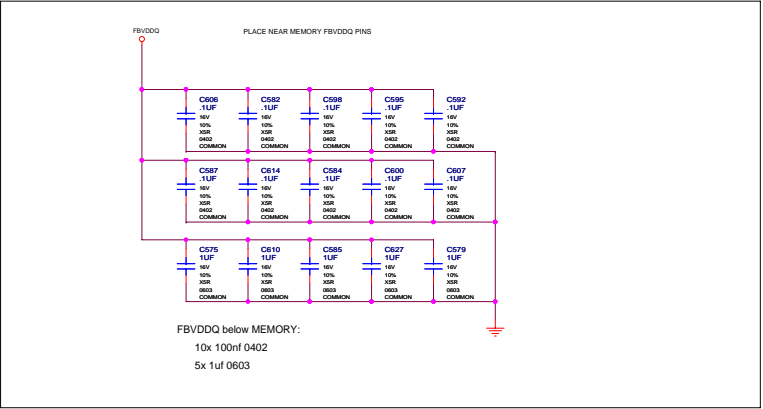
Decoupling for FBC C1 0..31



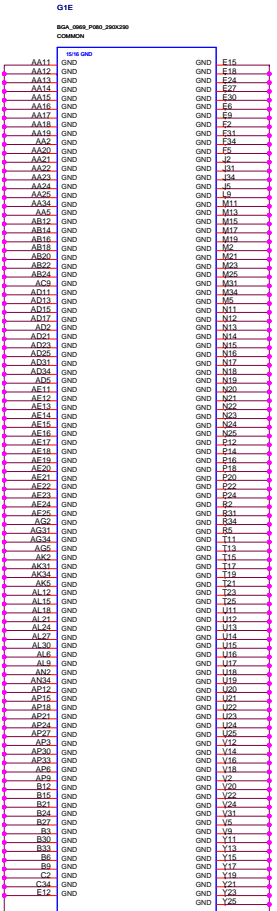
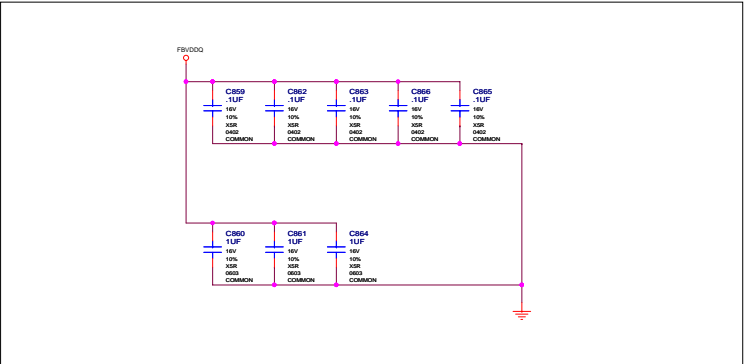
Return path coupling GND/FBVDDQ for FBC



Decoupling for FBC 32..63



Decoupling for FBC C1 32..63



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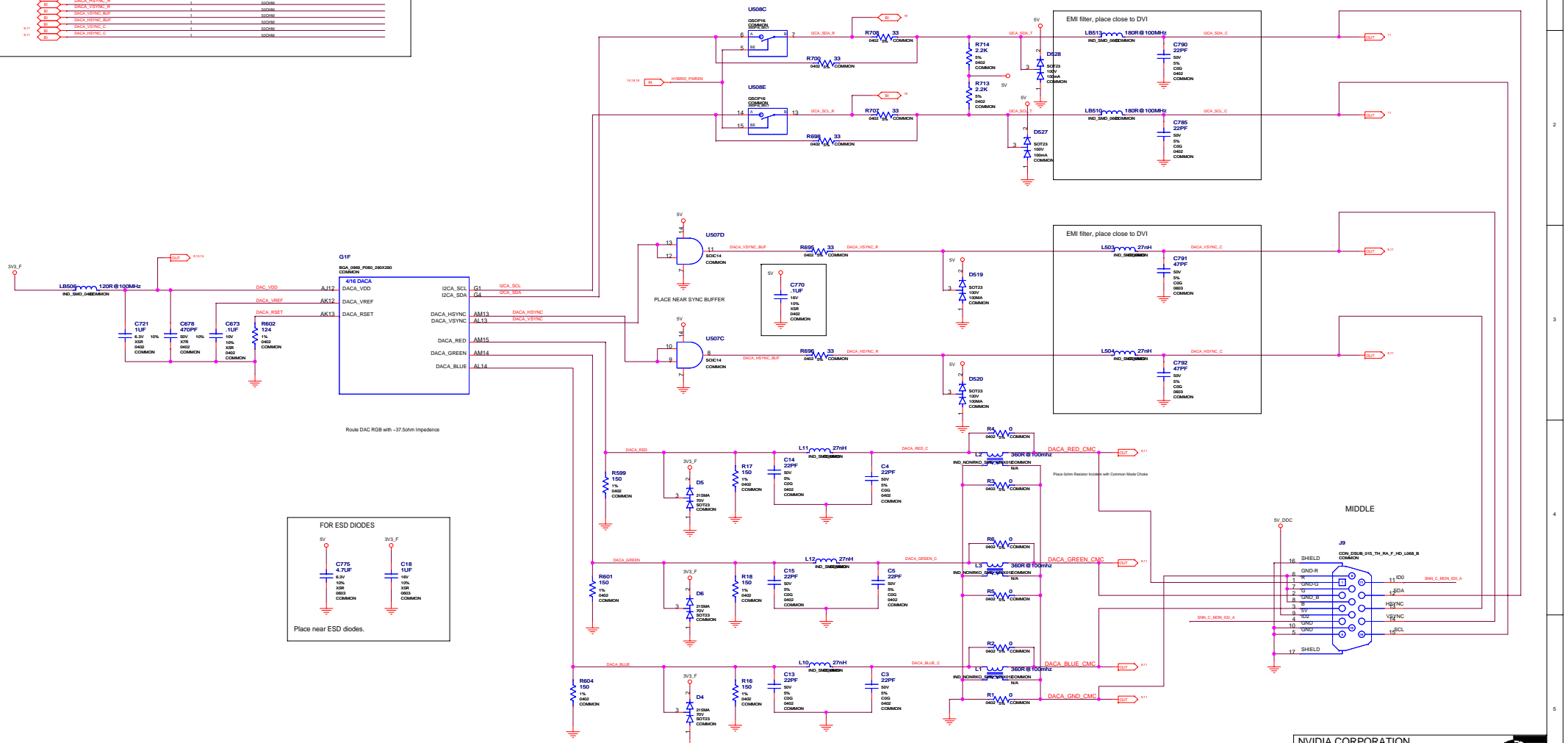
ASSEMBLY	BASE LEVEL "GENERIC" SCHEMATIC ONLY. COMMON & NC: BYOFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS, GPU GND CONNECTIONS

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	A		B
	NET_NAME	INV_CRITICAL_NET	IMPEDANCE
10.1	DAC0_DAC		33V 100M
	DACA_VREF		100M
	DACA_IBUF		100M
	DACA_PSD	1	7500M
	DACA_DRIVER_OSC	1	7500M
	DACA_BLUE_OSC	1	7500M
	DACA_PSD_C	1	7500M
	DACA_DRIVER_OSC_C	1	7500M
	DACA_BLUE_OSC_C	1	7500M
11	DAC1_DAC		2V 100M
	DACA1_VREF		100M
	DACA1_DRIVER_OSC	1	7500M
	DACA1_BLUE_OSC	1	7500M
	DACA1_PSDING	1	1000M
	DACA1_PSDING_B	1	1000M
	DACA1_PSDING_BUF	1	1000M
	DACA1_PSDING_BUF_B	1	1000M
	DACA1_PSDING_C	1	1000M
	DACA1_PSDING_C_B	1	1000M

Primary Display (DACA), DVI-I

DACA RGB-FILTER



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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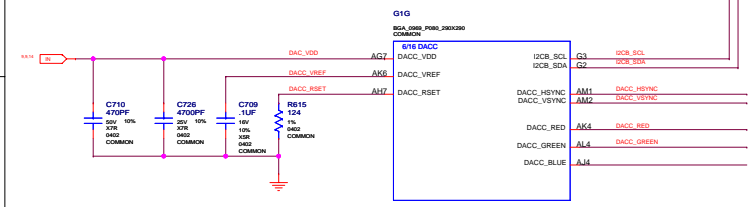
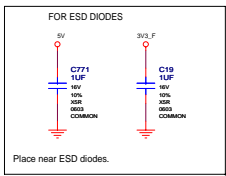


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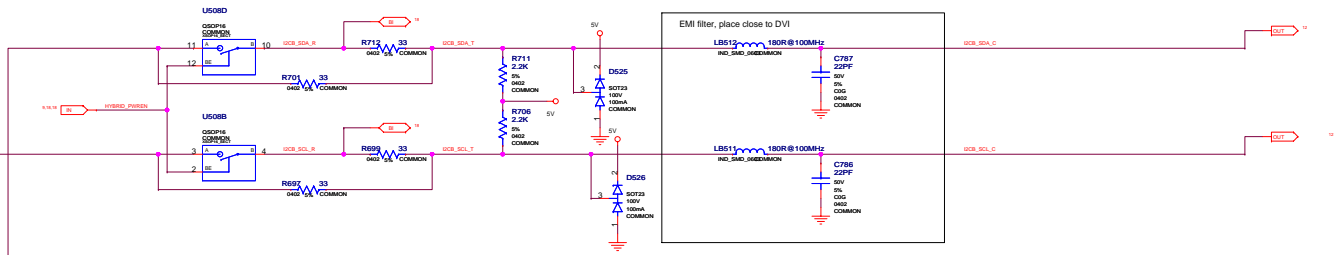
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NET_NAME	INV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACC_VREF		120M	
DACC_VREF		120M	
DACC_RED	1	250M	
DACC_GREEN	1	250M	
DACC_BLUE	1	250M	
DACC_RED_C	1	250M	
DACC_GREEN_C	1	250M	
DACC_BLUE_C	1	250M	
DACC_DMD_DMC		0V	120M
DACC_RED_DMC	1	250M	
DACC_GREEN_DMC	1	250M	
DACC_BLUE_DMC	1	250M	
DACC_HSYNC	1	500M	
DACC_VSYNC_F	1	500M	
DACC_VSYNC_R	1	500M	
DACC_VSYNC_G	1	500M	
DACC_VSYNC_BFP	1	500M	
DACC_VSYNC_RFP	1	500M	
DACC_VSYNC_G	1	500M	
DACC_VSYNC_C	1	500M	
DACC_VSYNC_C	1	500M	



Secondary Display (DACC), Slim DB15

DACC RGB-FILTER



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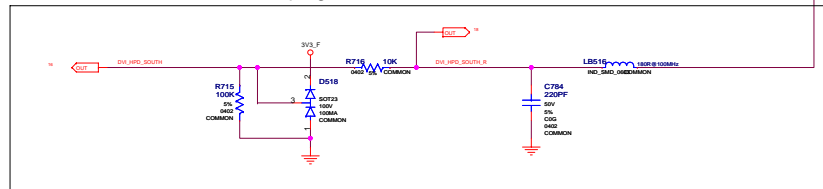
ASSEMBLY	BASE LEVEL "GENERIC" BOARD ONLY. COMMON & NO. 310FF ASSEMBLY NOTES AND BOM NOT FINAL.
PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID


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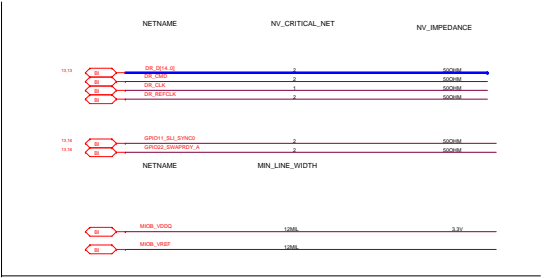
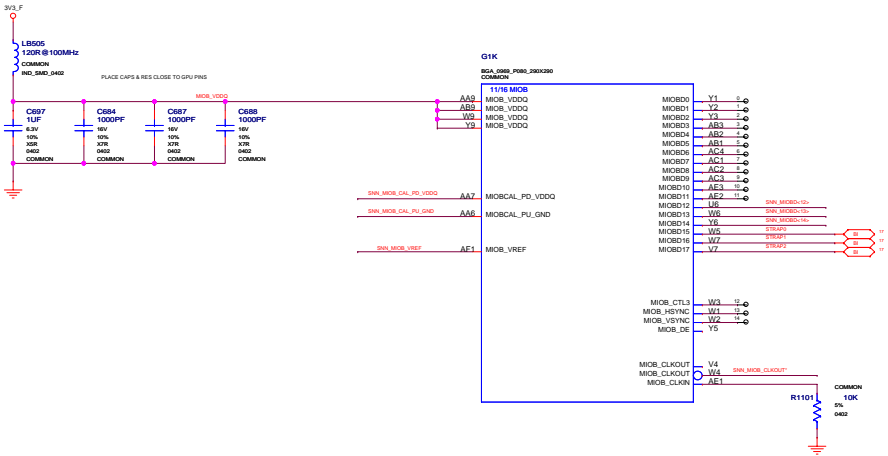
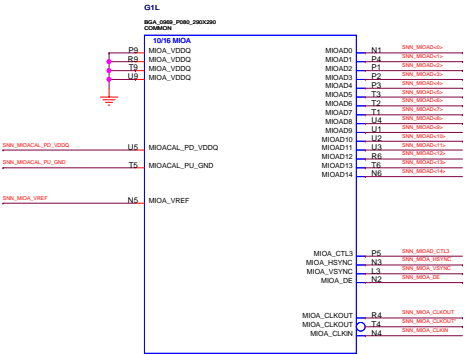
NV_PN	600-10727-base-sch A		
ID		PAGE	
NAME		DATE	31-OCT-2007

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NV_PN		600-10727-base-sch A	
ID		PAGE	
NAME		DATE	31-OCT-2007

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MIOA/B SLI

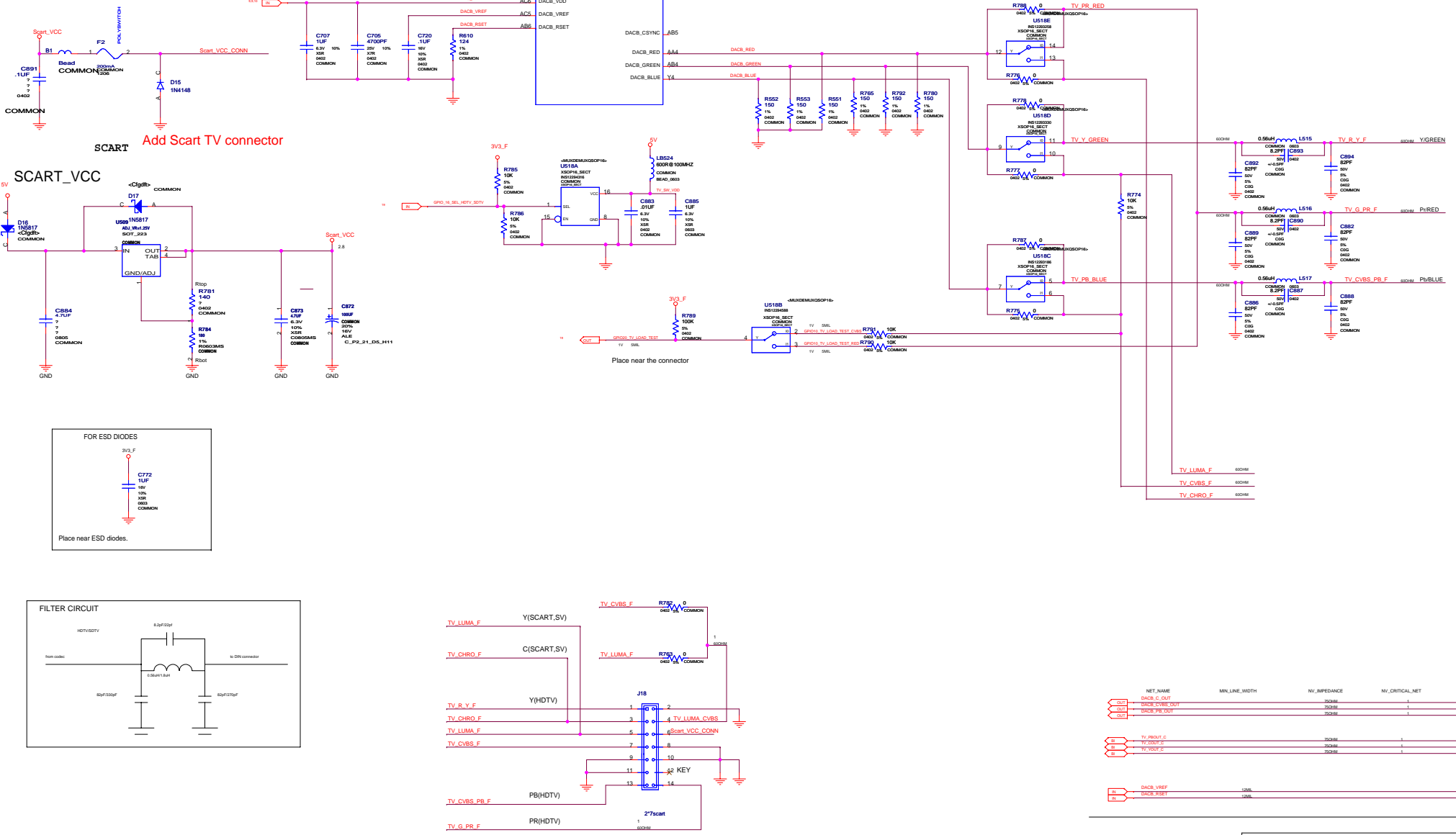


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ASSEMBLY	BASE LEVEL GENERIC BOARDING ONLY, COMMON & NO. 3Y0FF ASSEMBLY NOTES AND BOARD NOT FINAL
PAGE DETAIL	MIOA & MIOB SLI CONNECTOR

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NV_PN	600-10727-base-sch A		
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NAME		DATE	31-OCT-2007

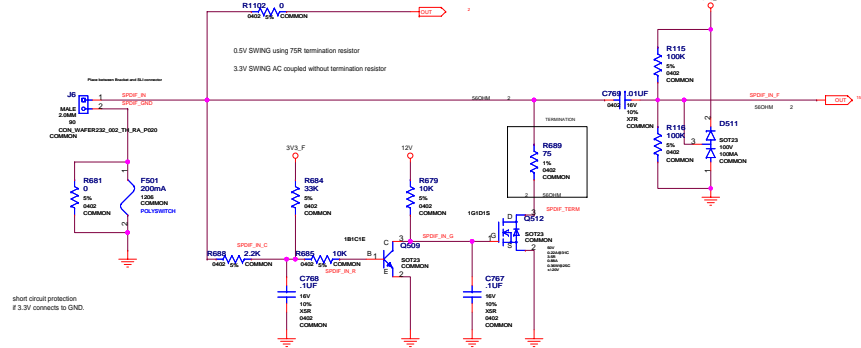
DACB: SD/HD VIDEO OUT CONNECTOR



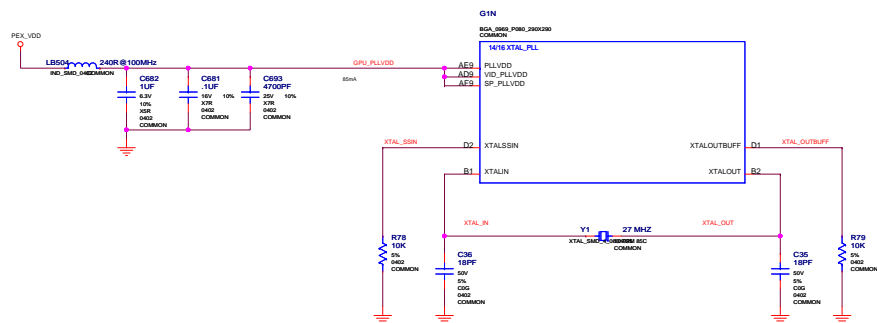
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XTAL/PLLVD/SPDIF IN

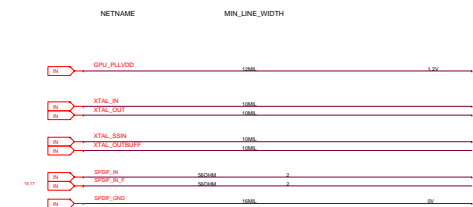
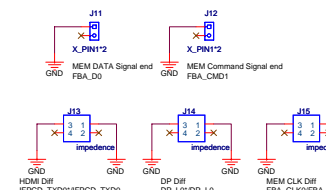
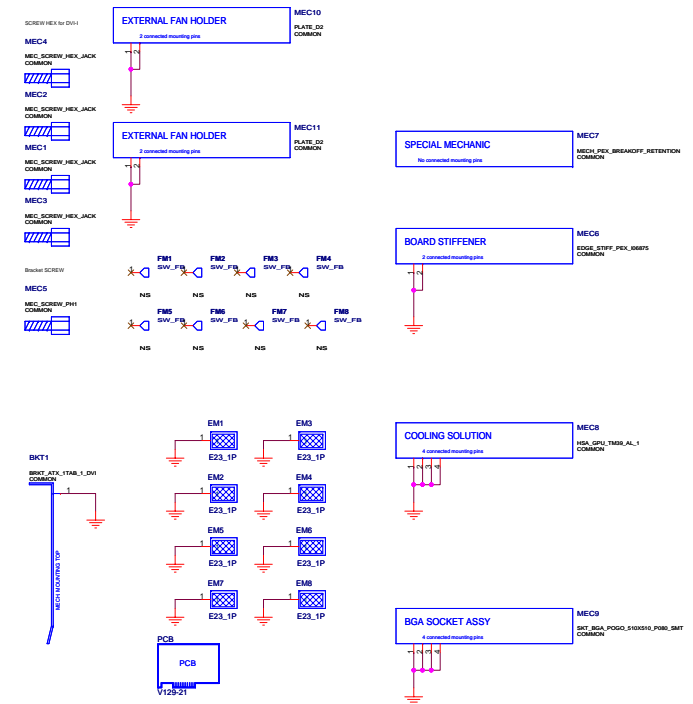
SPDIF IN



XTAL/GPU_PLLVDD



MECHANICALS & THERMALS



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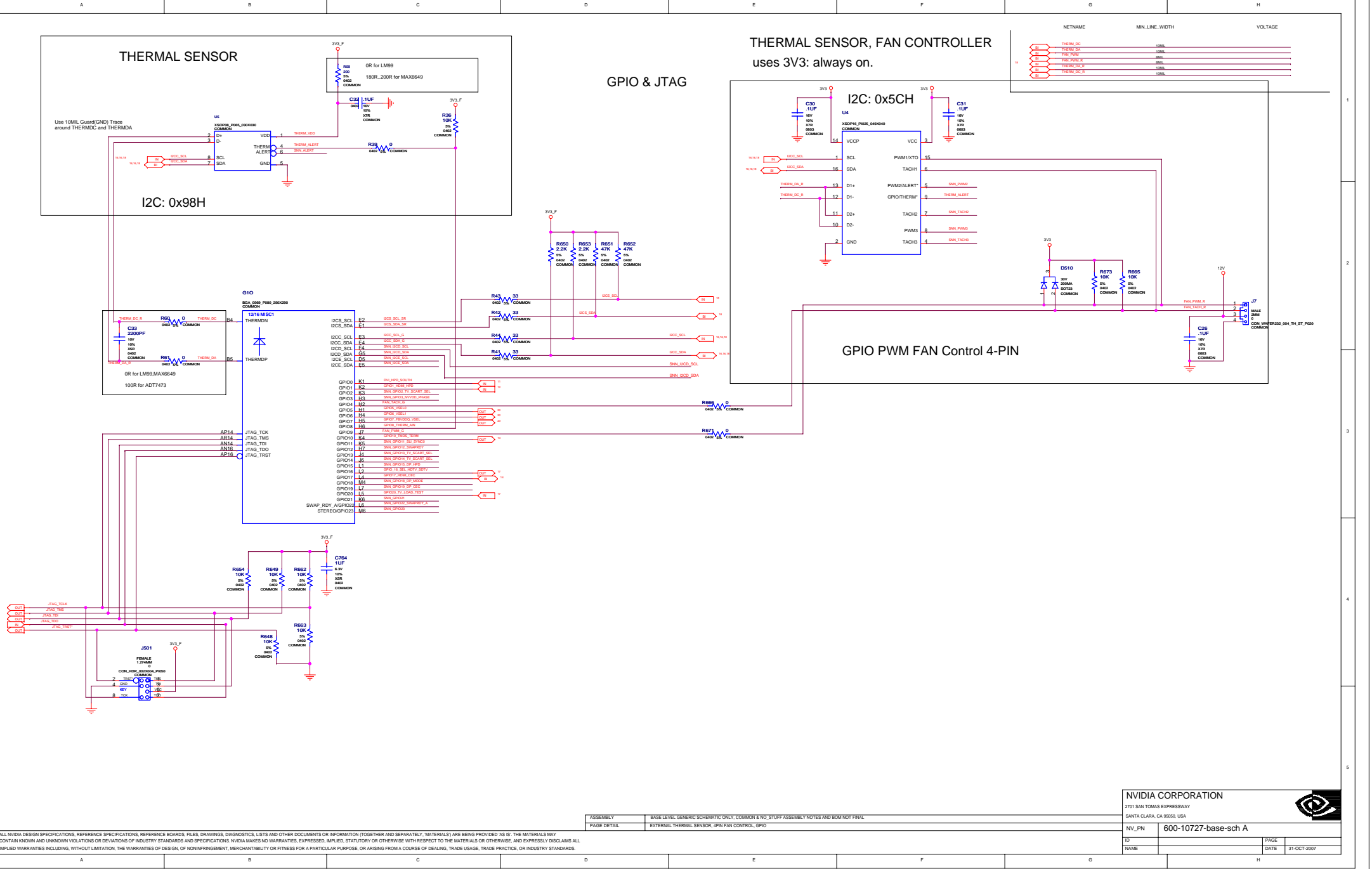
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NAME		DATE	31-OCT-2007

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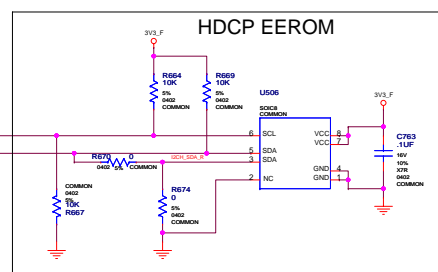
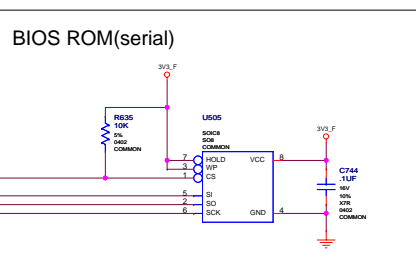
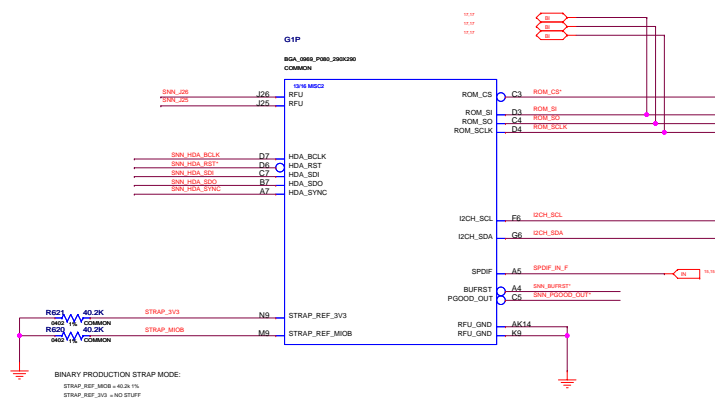
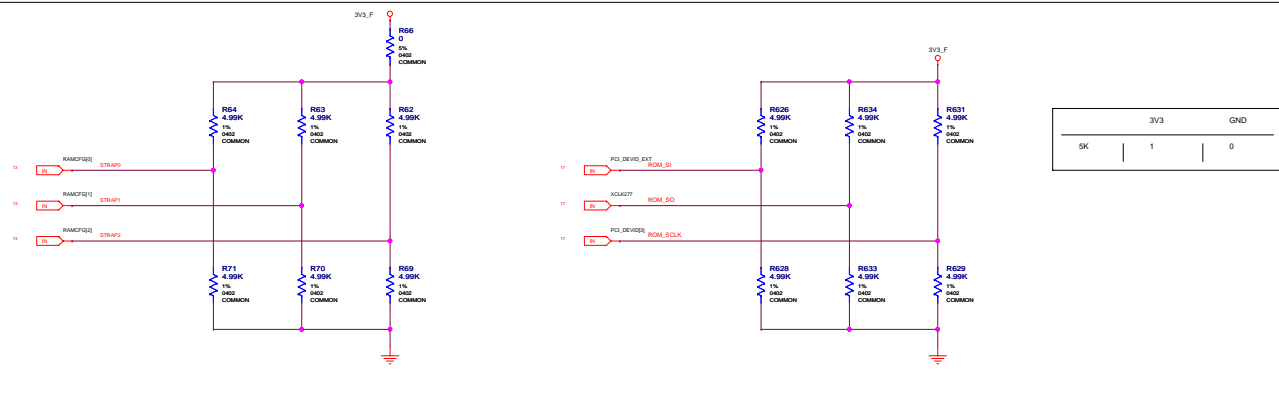
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PAGE DETAIL	SPDIF-IN, XTAL, MECHANICALS, THERMALS



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STRAPPING OPTIONS

Assembly: BIOS



	NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
OUT	HDA_BCLK		50ΩΩM	2
OUT	HDA_RST*		50ΩΩM	2
OUT	HDA_SPS		50ΩΩM	2
OUT	HDA_SSDO		50ΩΩM	2
OUT	HDA_STXNC		50ΩΩM	2

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

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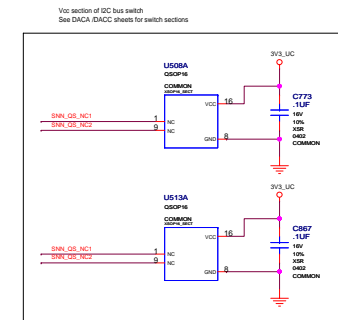
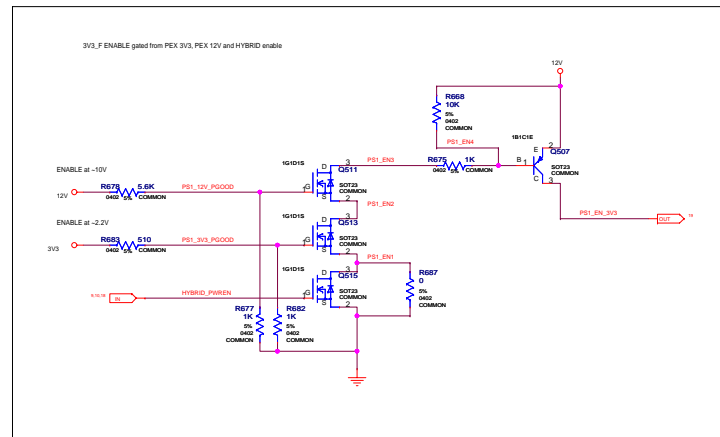
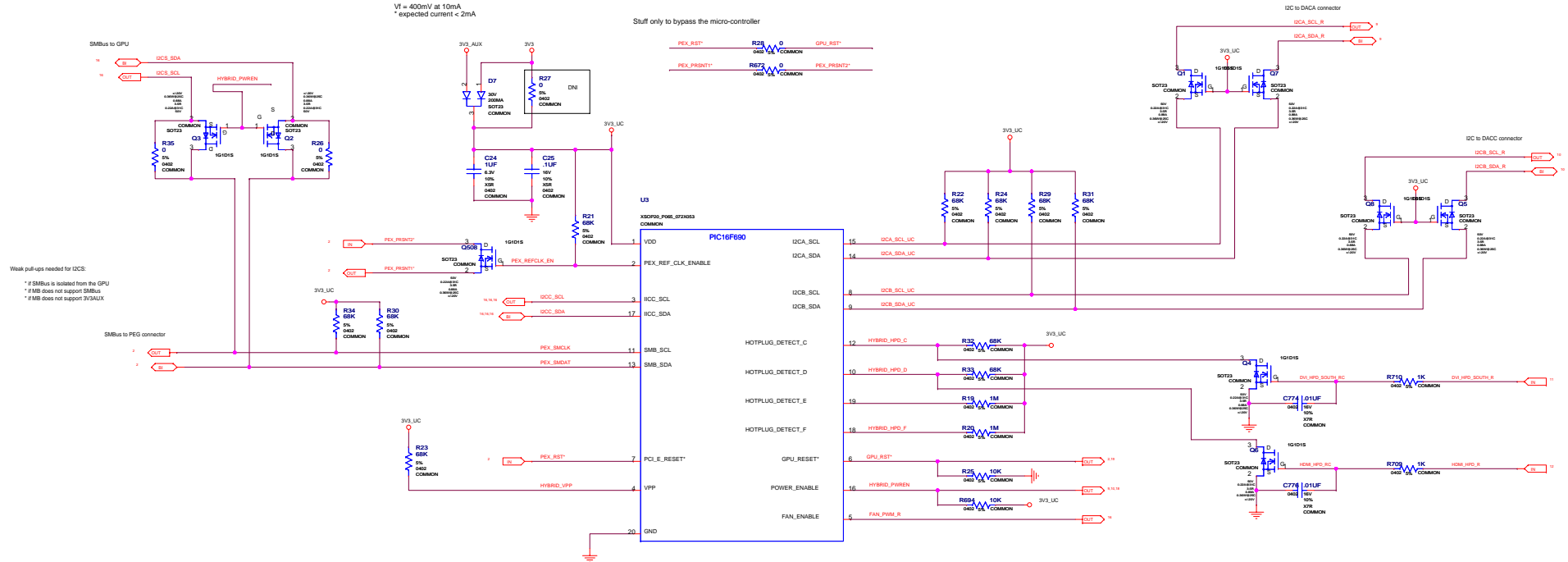
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HYBRID POWER

Per Datasheet:

Vf = 400mV at 10mA
* expected current < 2

Stuff only to bypass the micro-controller



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	HYBRID POWER CIRCUIT

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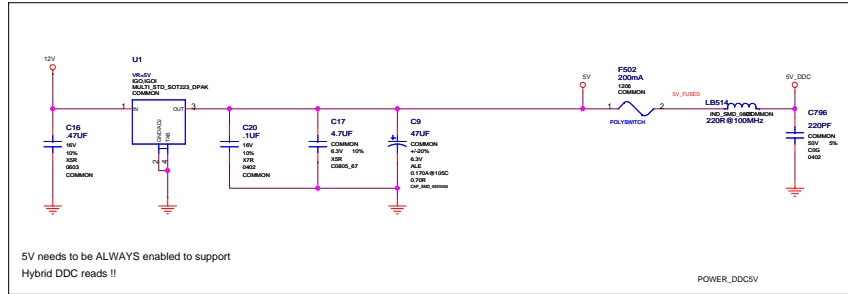


NV_PN	600-10727-base-sch A
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NAME	DATE 31-OCT-2007

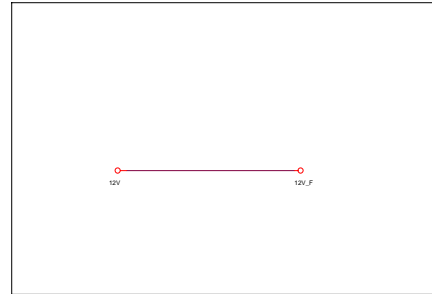
Power Supply: 5V, 5V_DDC, TMDS, MIOA_VDDQ

5V REGULATOR

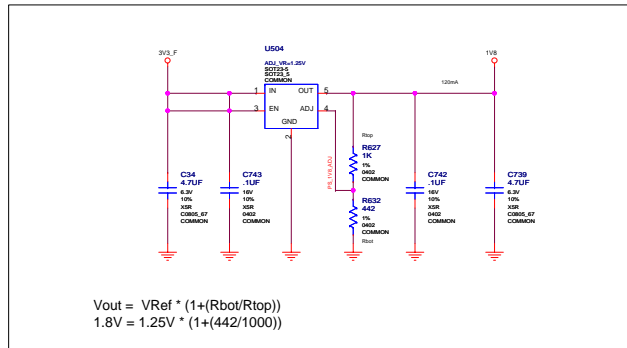


5V DDC

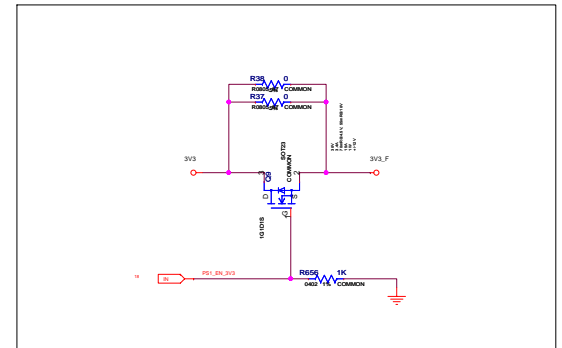
12V filter



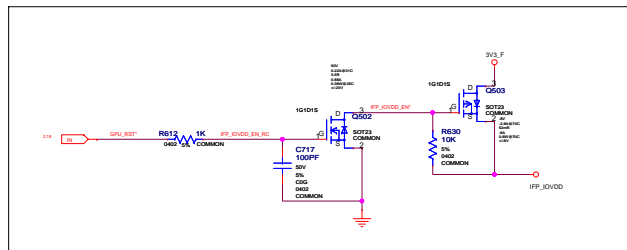
IFP PLL Supply 1.8V



3V3 switch



IFP_IOVDD BACKDRIVE PREVENTION



	NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
B	EV_PUBED	0.1A	12800	5V
	EV_300C	0.1A	12800	5V
	5V_300C	0.15A	12800	5V
	5V	0.15A	12800	5V
	PS_1V0_A02	1.85V	12800	1.85V
C	10B	0.12A	12800	1.85V
	20V	0.3A	12800	2.20V
	PS_5V	0.50A	12800	5V
	GND	0.50A	12800	0V
	12V3_F	3.2A	12800	3.3V
D	12V_F	6A	20400	12V
	12V_F			12V_F

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY LINES: 5V, DDC5V, IFF PLLVDD, IFF IOVDD, MIO VDD, 3V3 FILTER, 12V FILTER

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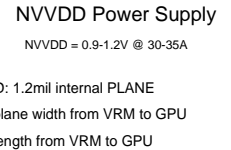
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NAME		DATE	31-OCT-2007

Net Name	LINE_WIDTH	Current	Voltage
N1020	30MIL	10A	1.2V
FEED10	30MIL	1.5A	1.2000V
N1020_SENSE	10MIL	0.5A	1.2V
N1020_SENSE_W	10MIL	0.5A	1.2V

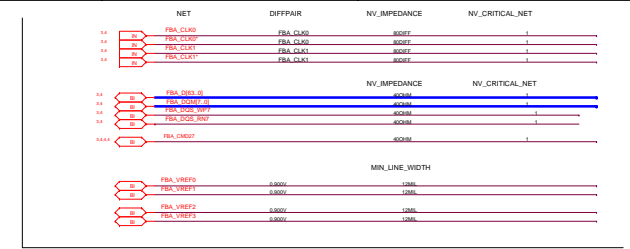
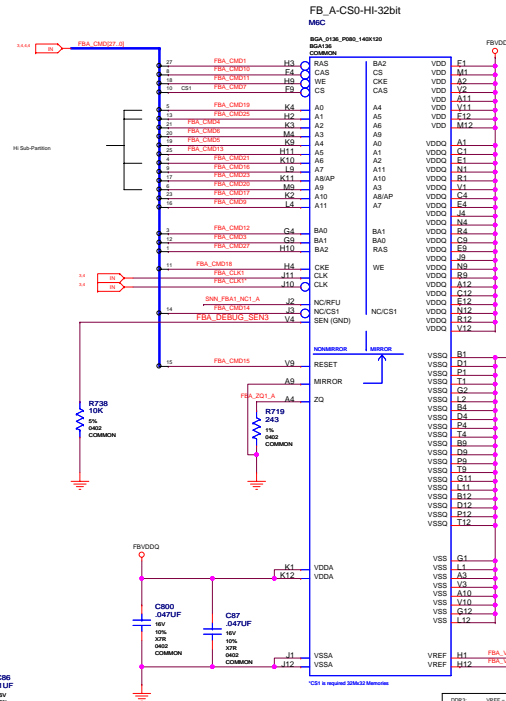
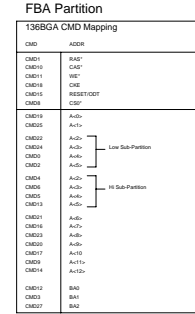
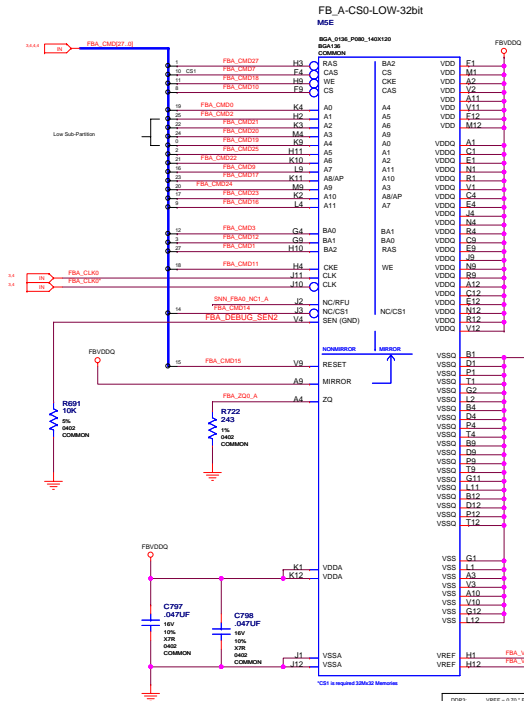


	GPIO6	GPIO5
NVDD = 1.00V R7403 1.54K R7329 6.19K	0	0
NVDD = 1.05V R7403 1.54K R7329 6.19K R661 24.3K	0	1
NVDD = 1.10V R7403 1.54K R7329 6.19K R676 12.1K	1	0
NVDD = 1.15V (Undervolt) R7403 1.54K R7329 6.19K R661 24.3K R676 12.1K	1	1

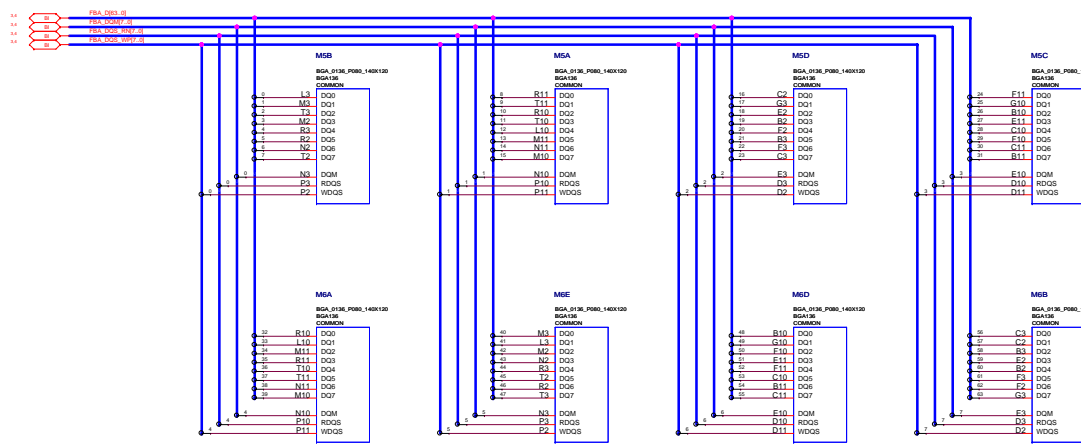
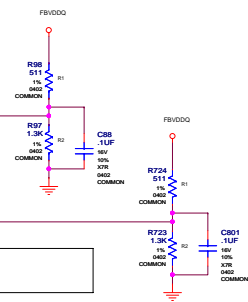
	GPI05
$V_{DD} = 0.95V$ R7403 1.00K R7329 5.36K	1
$V_{DD} = 1.00V$ R7403 1.00K R7329 5.36K R661 16.2K	0

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FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3



Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 16/32Mx32 GDDR3 MEMORIES, FBA COMMAND BUS P/U'S, FBA CLK TERMS

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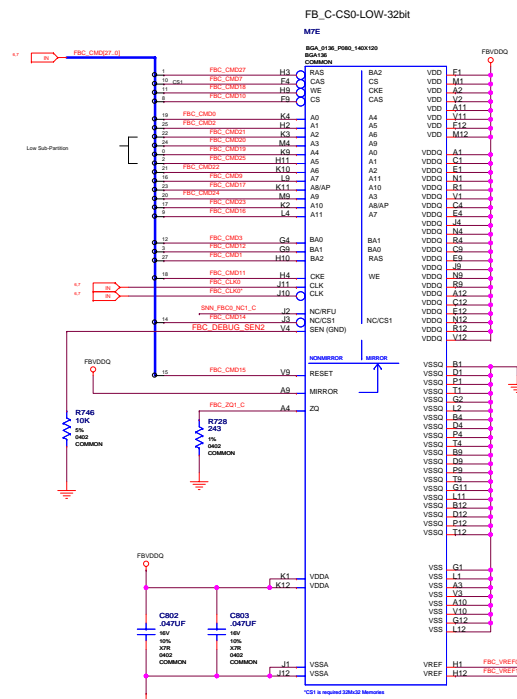
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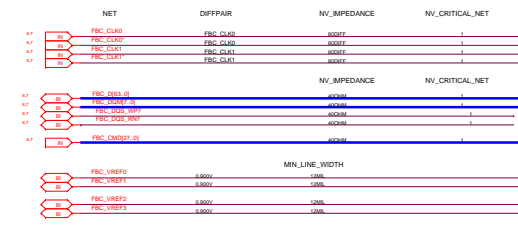
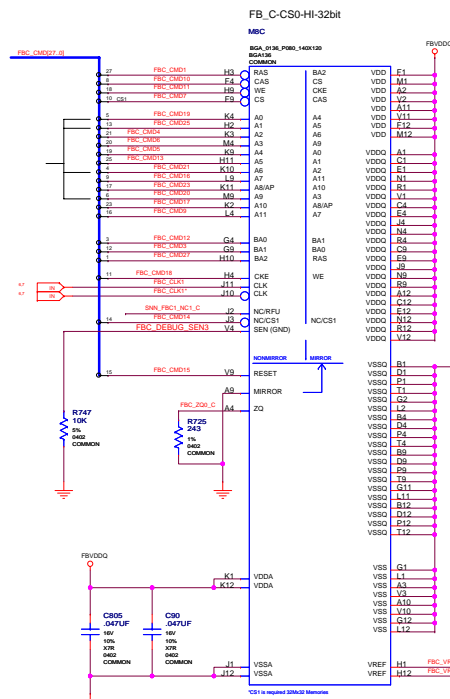
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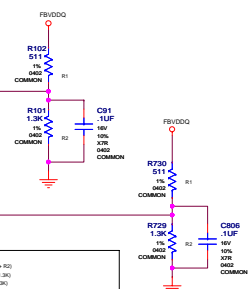
FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3



FBC Partition			CSD
CMD	ADDR		
CMD1	RAS*		
CMD2	CAS*		
CMD11	WE*		
CMD18	CKE		
CMD16	RESET/ODT		
CMD8	CS*		
CMD19	Ar1*		
CMD25	Ar2*		
CMD3	Ar3*	} Low Sub-Partition	
CMD0	Ar4*		
CMD2	Ar5*		
CMD4	Ar6*	} H8 Sub-Partition	
CMD6	Ar7*		
CMD8	Ar8*		
CMD13	Ar9*		
CMD21	Ar10*		
CMD16	Ar11*		
CMD23	Ar12*		
CMD30	Ar13*		
CMD17	Ar14*		
CMD6	Ar11*		
CMD14	Ar12*		
CMD12	BA0		
CMD3	BA1		
CMD27	BA2		



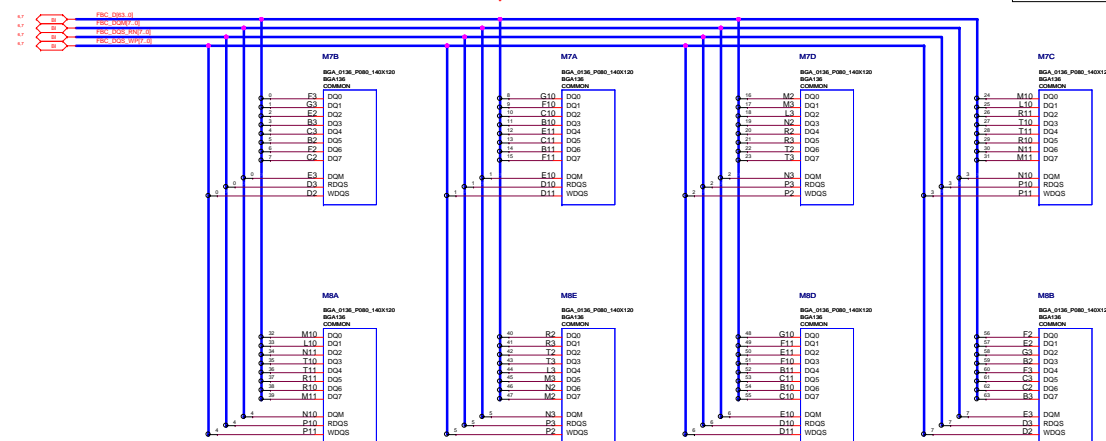
Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!



```

COR2:  VREF = 0.70 * FBVDDO
        VREF = FBVDDO * R2/(R1 + R2)
        1.26V = 1.8V * 1.3K/(511 + 1.3K)
        1.4V = 2.0V * 1.3K/(511 + 1.3K)

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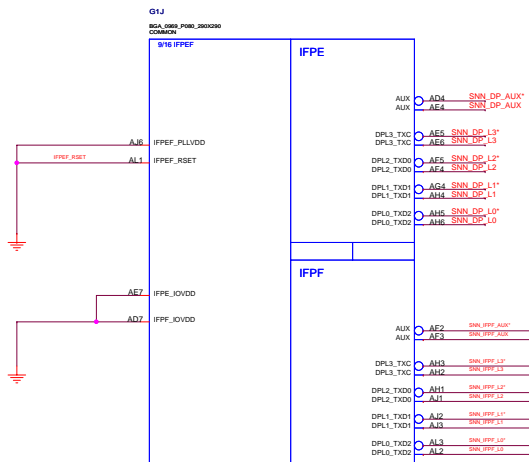
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS P/U'S, FBC CLK TERMS

TMDS E : Display Port




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ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STOP ASSEMBLY NOTES AND NOT FINAL

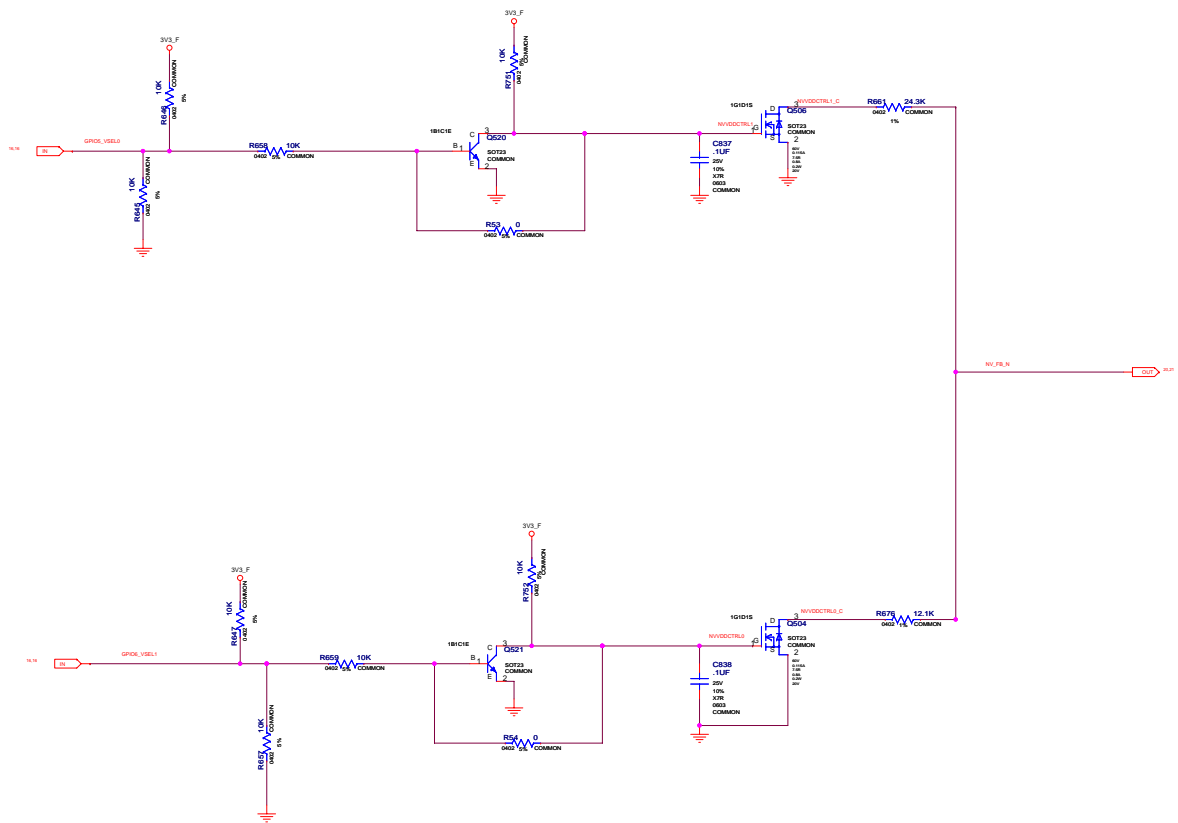
PAGE DETAIL: TMDS LINK C/D, AC COUPLING, PDs, DVI CONNECTOR MID

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DYNAMIC NVVDD



Dynamic NVVDD

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: NVDD DUAL PHASE SWITCHER

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