P141-A03, NV31/NV34/NV18B
4(8,16)Mx16, 64(128,256)MB, VIDEO IN/OUT, DVI-I, VGA

Page Overview

HISTORY:

A00

X00: INITIAL VERSION

X01: First Review
- Replaced series resistors in sync lines with 33ohms
- Moved clamping diodes next to GPU
- Added parallel caps to EMI filter DACB
- Removed not needed strap on SAA7114
- Connected RESET and WP of SST ROM to ROMVCC
- Added parallel ROM and Strapps
- Added FBVDD regulator
- Added STEREO glasses circuit
- Removed Decoupling CAPs on VIP VDD, covered by Caps on page 2
- Added ROM_VCC for cleaner planes
- Changed used TMDS lines of IFPA and IFPB to TP from NTP
- Changed Resistor for AGP Vref circuit to 158k

X02: Final Review
- Added clock termination resistors
- Added net name for FBCALxxx
- Added cap on filter input for FB_DLLVDD, DACA_VDD & DACB_VDD
- Changed netnames for SAA7114 NTPs to NTP_xxx
- Added 1uF cap parallel to fan connector
- Changed all xxCALxx resistors to 50 Ohms
- Changed all FBxDQS*<x> to NTP_FBxDQS*<x> with NO_TEST property

A01

X00: Fixed pin swap on parallel ROM A12 & A13
- Added charge pump for SC2612
- Added resitstors to swap GPIO for DACB loadtest
- Added resitstors for I2C on internal Video IN connector

X01: Updated variant information for new Sbom structure

A02

X00: Added sw adjust for NVVDD
- Exchanged TMDSIOVDD regulator to lower the voltage drop
- Changed TMDSPLLVDD regulator bypass to A3V3
- Addrd 1k series resistor in DACB load detection circuit

A03

X00: Removed GPIO5 from NVVDD adjust
- Fixed values for DAC Rset resitors
- Removed Sync Buffer bypass
- Removed 2nd voltage selection fet
- Changed to new internal video connector
- Added snubber to NVVDD and FBVDD regulator

8912 version 210 base on P141-A03 Modify.
1.Page 13 add 1*4 pin vedio-in connector.

602-10141-0000-000 Base Schematic

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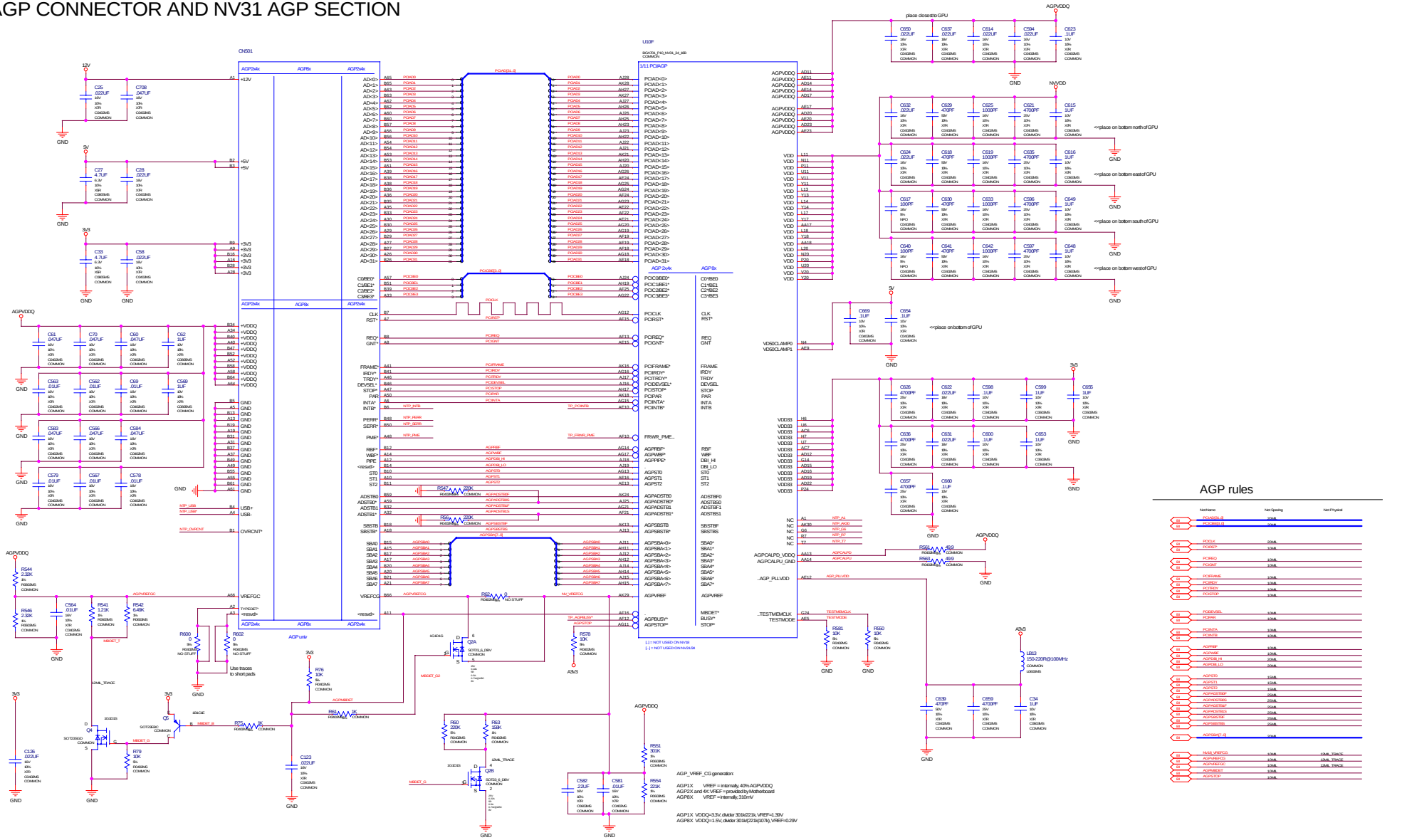
MS-8912 base on P141-A03 modify
Size: Custom | Document Number: TOP PAGE | Rev: 300
Date: Monday, March 31, 2003 | Sheet 1 of 17

AGP CONNECTOR AND NV31 AGP SECTION



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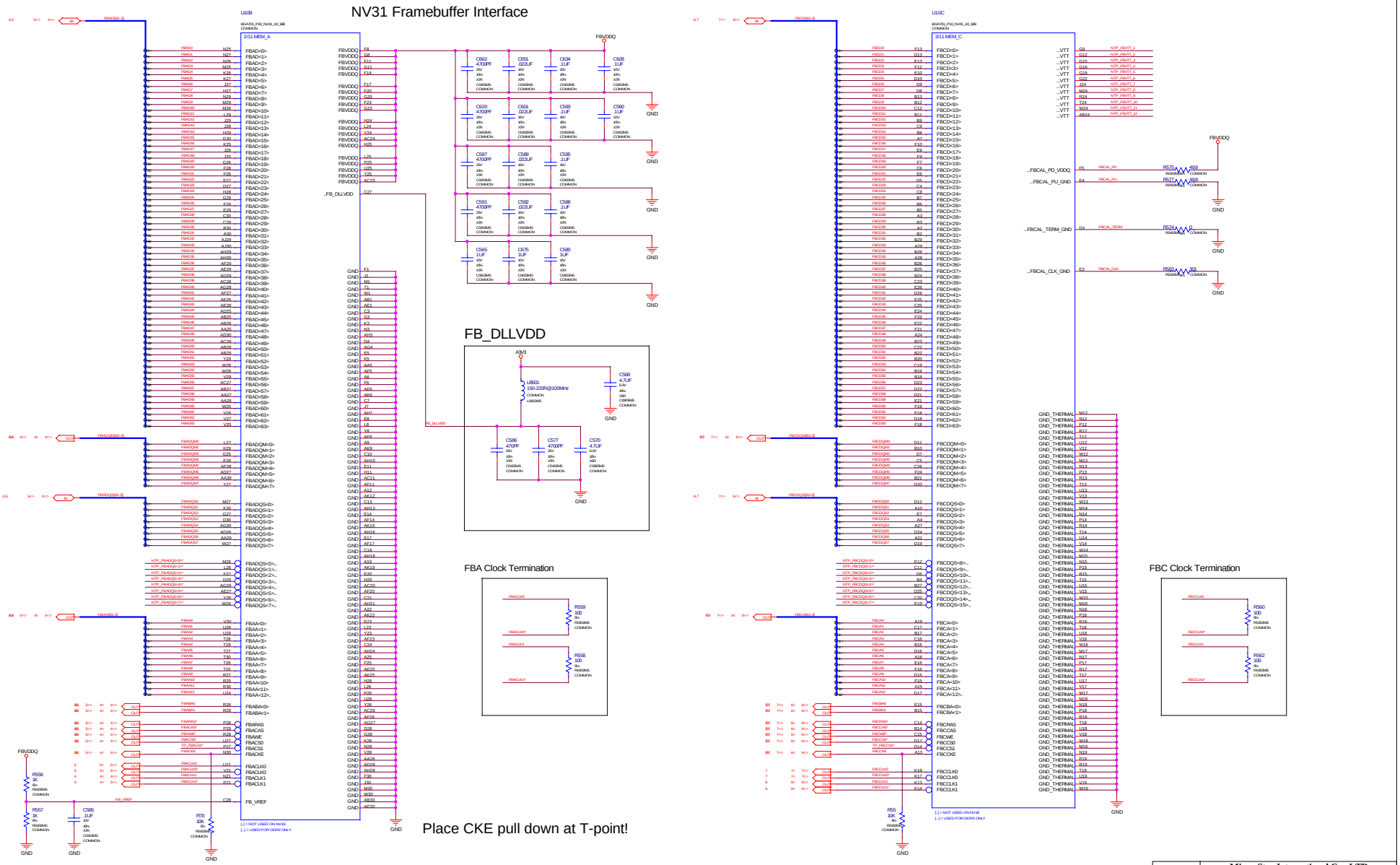
Size:	Document Number: AGP CONNECTOR AND NV31 AGP SECTION
Rev:	300
Date: Monday, March 31, 2003	Sheet 2 of 17

NV31 Framebuffer Interface



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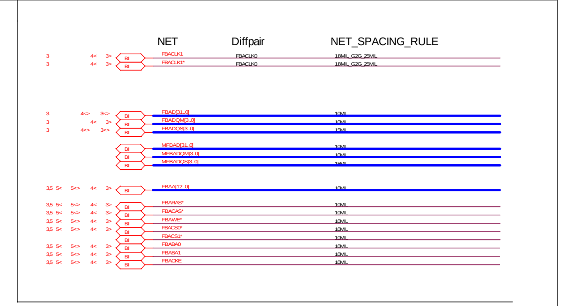
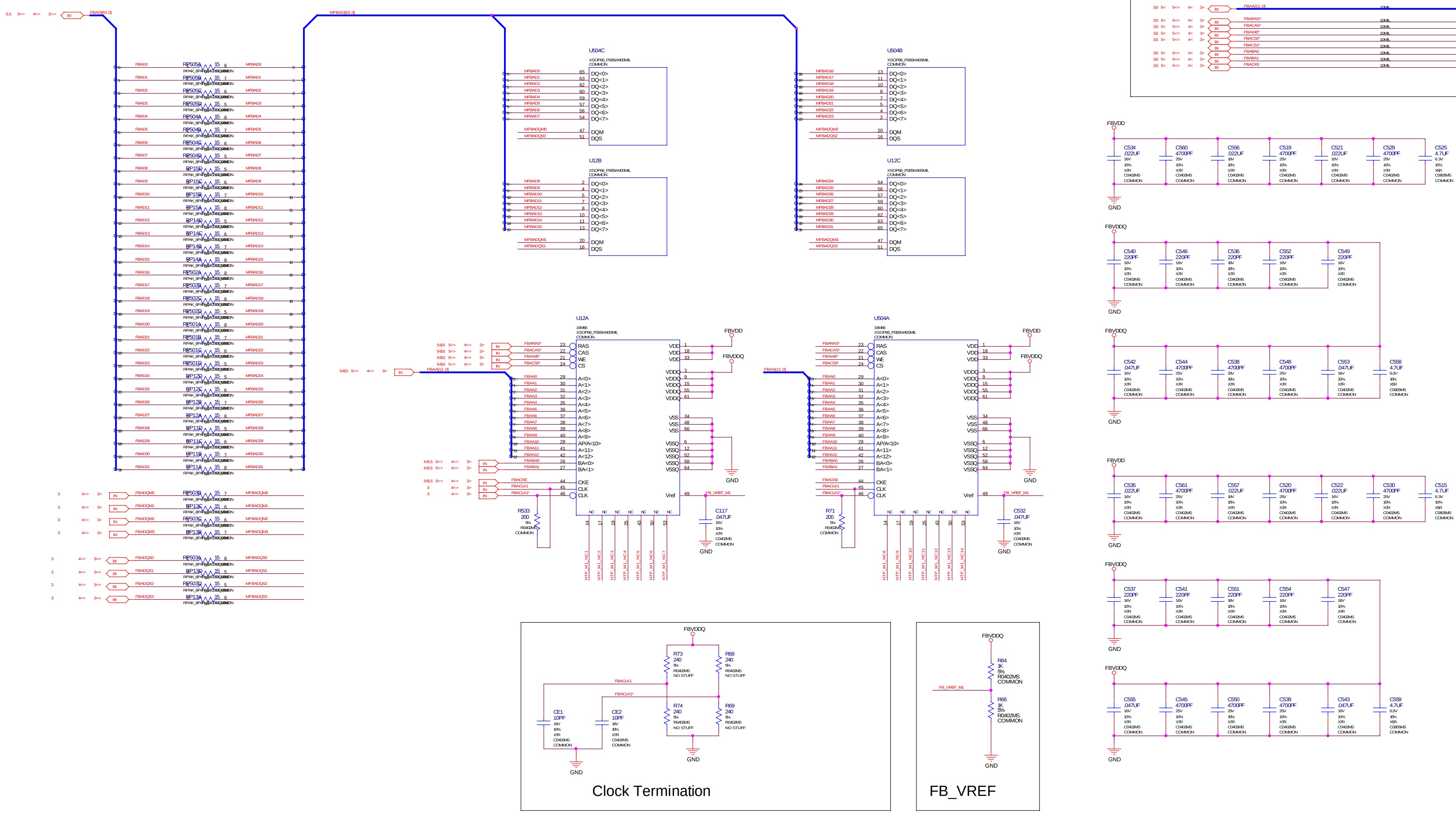
Rev: 300	
Date: Monday, March 31, 2003	Sheet 3 of 17

MEMORY 8(16)Mx16DDR Partition A , Bits 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!





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MS-8912 base on P141-A03 modify		
Size Custom	Document Number MEMORY 8(16)Mx16DDR Partition A , Bits 0..31	Rev 300
Date: Monday, March 31, 2003	Sheet 4 of 17	

MEMORY 8(16)Mx16DDR Partition A , Bits 32..63

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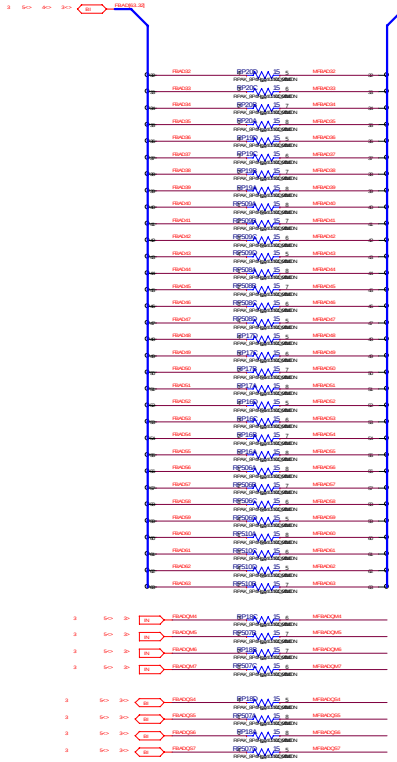

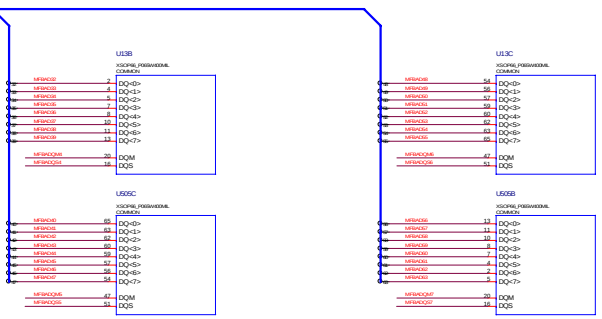

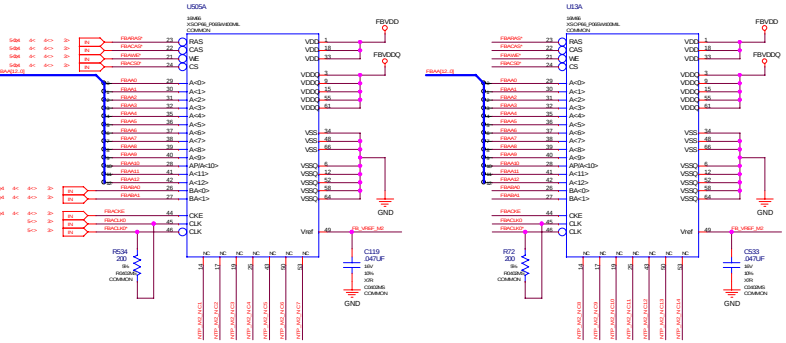

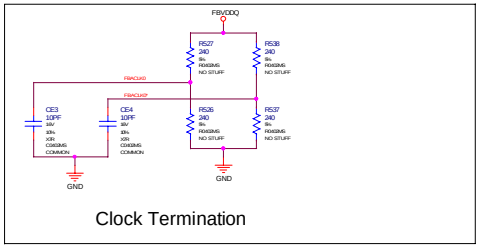

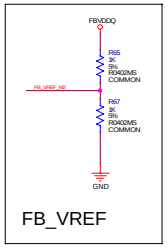

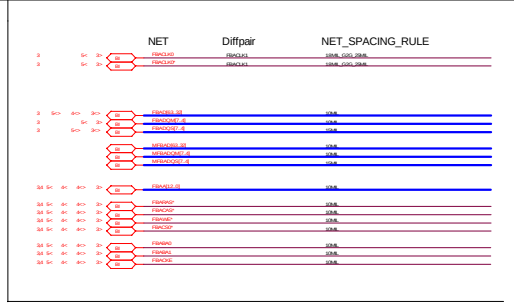

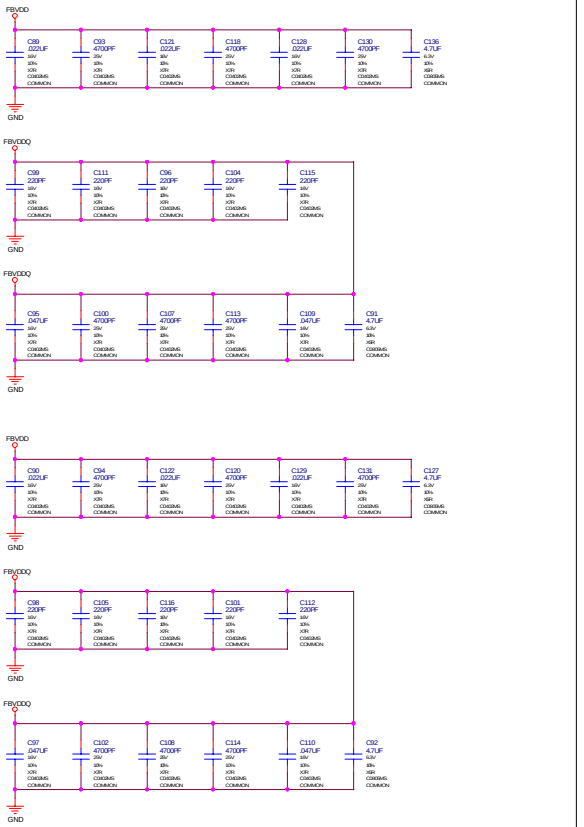

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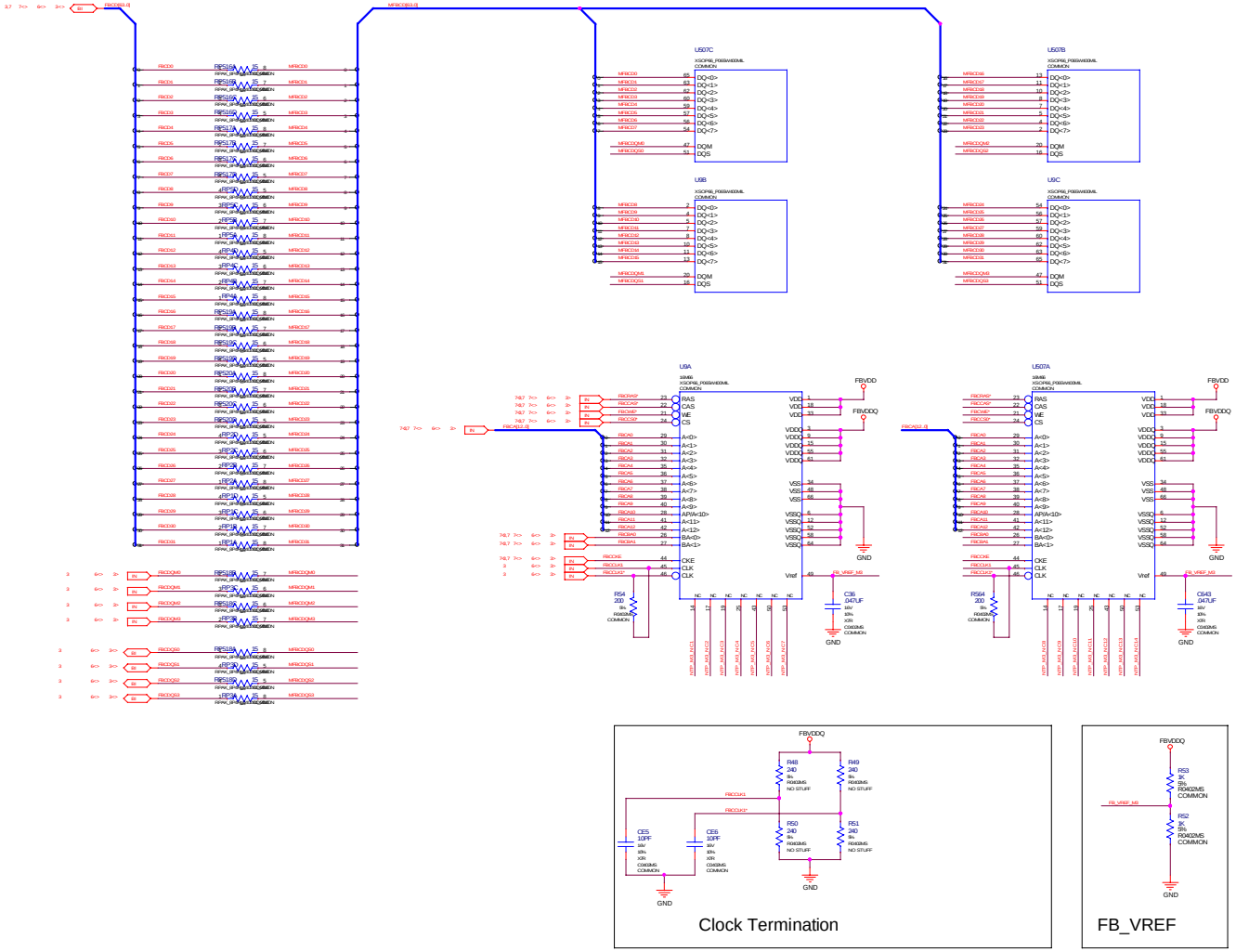
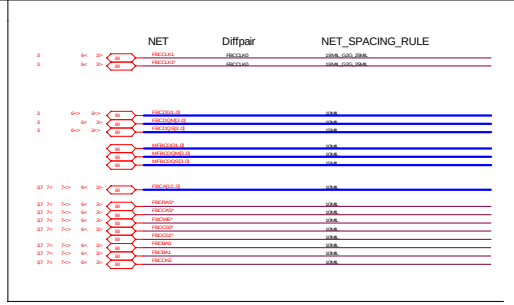
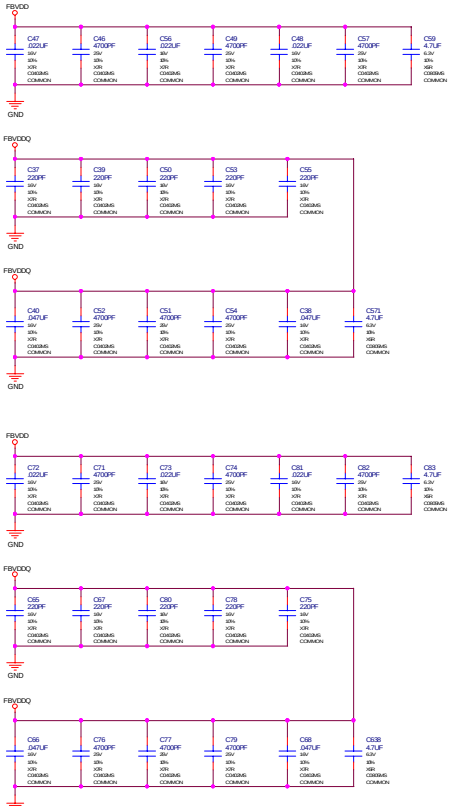
Size: Custom	Document Number: MEMORY 8(16)Mx16DDR Partition A , Bits 32..63		Rev: 300
Date: Monday, March 31, 2003		Sheet 5 of 17	

MEMORY 8(16)Mx16DDR Partition C , Bits 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!







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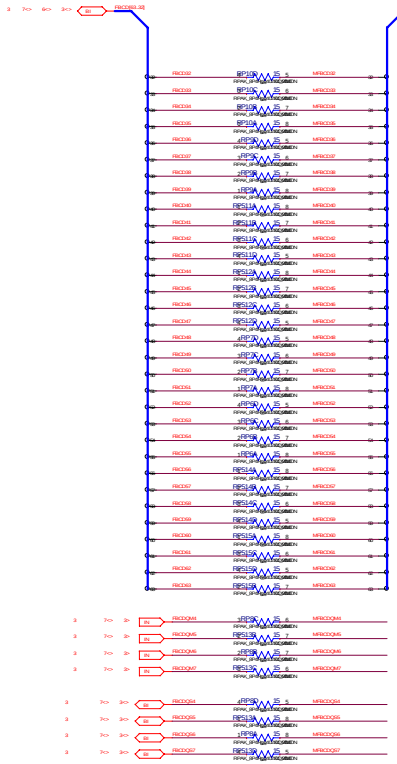
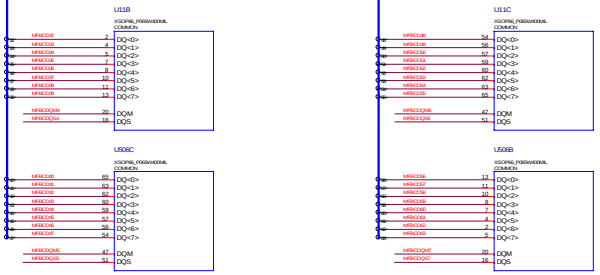
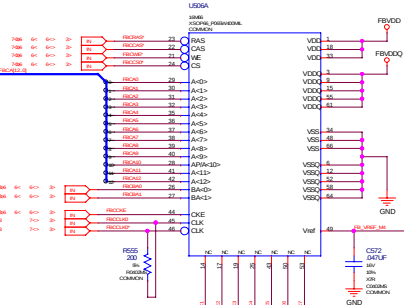
Size: Custom	Document Number: MEMORY 8(16)Mx16DDR Partition C , Bits 0..31		Rev: 300
Date: Monday, March 31, 2003	Sheet: 6 of 17		

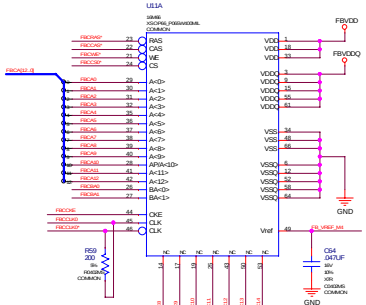
MEMORY 8(16)Mx16DDR Partition C , Bits 32..63

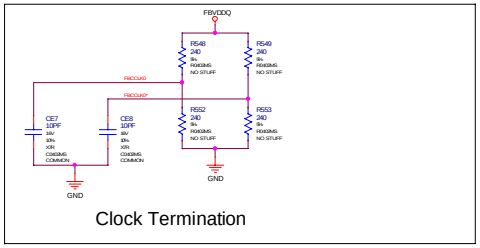
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

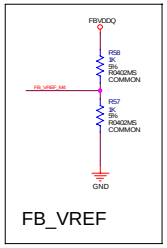


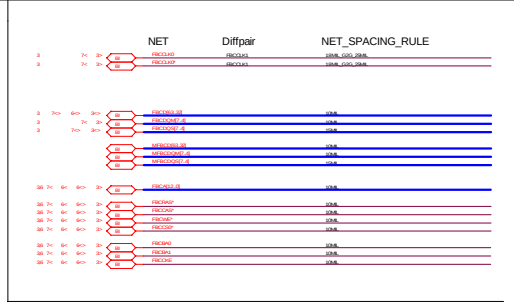


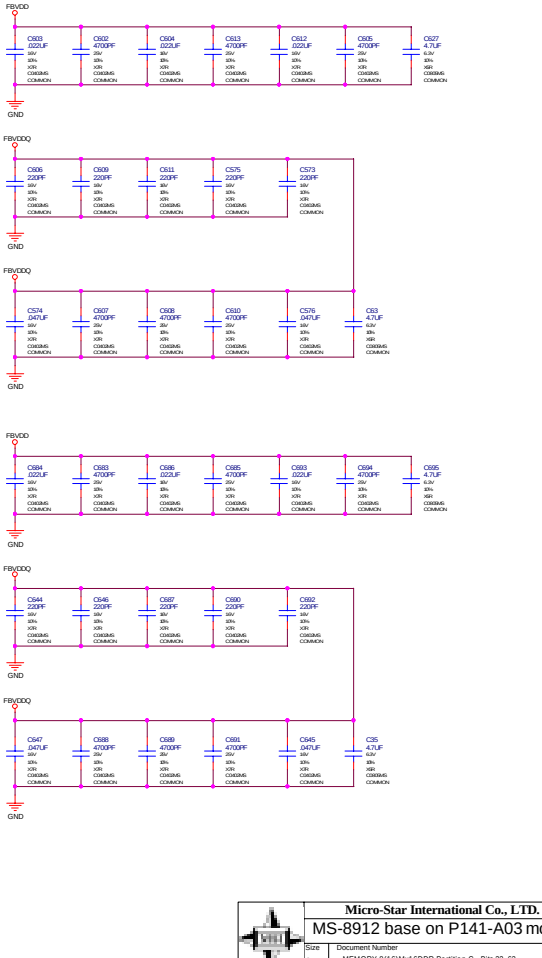












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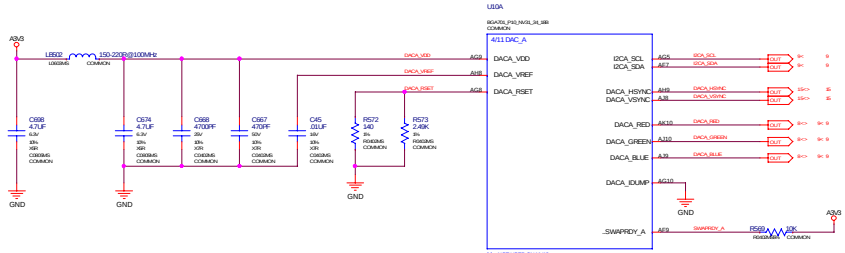
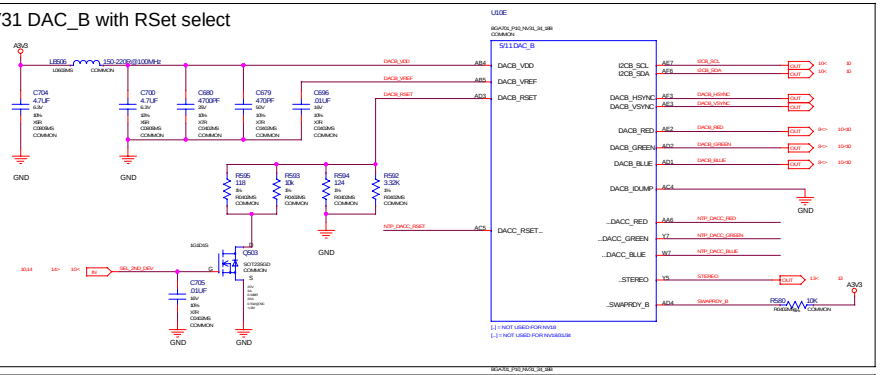
Size	Document Number		Rev
Custom	MEMORY 8(16)Mx16DDR Partition C , Bits 32..63		300
Date:	Monday, March 31, 2003	Sheet 7 of 17	

NV31 DAC_A, DAC_B, PLL, SYNC Buffer

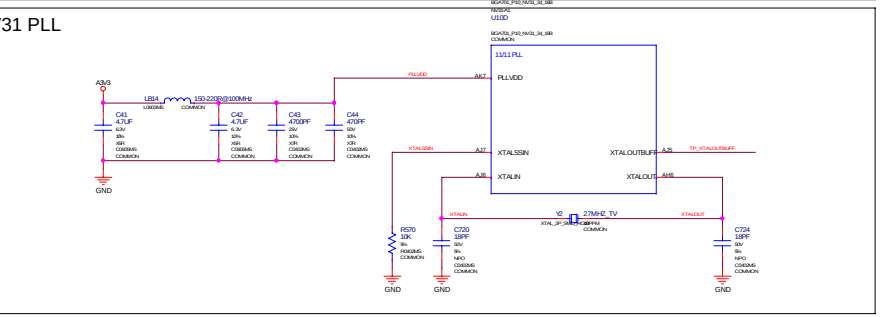
NV31 DAC_A



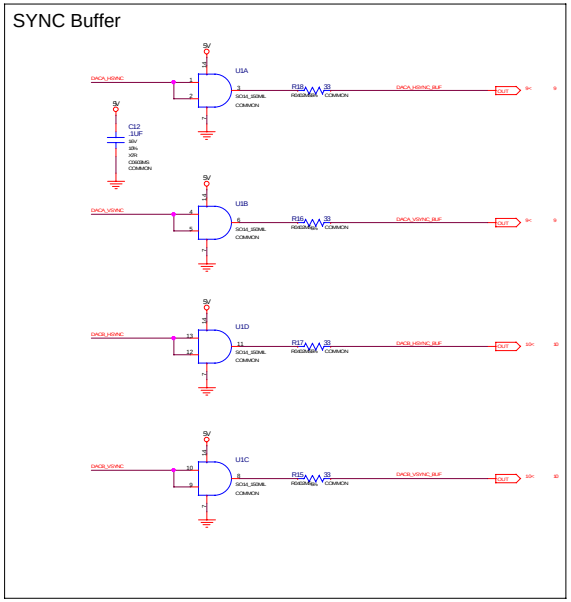
NV31 DAC_B with RSet select

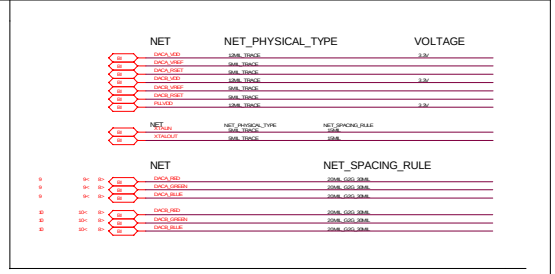


NV31 PLL



SYNC Buffer





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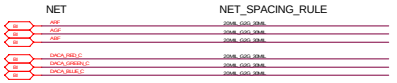
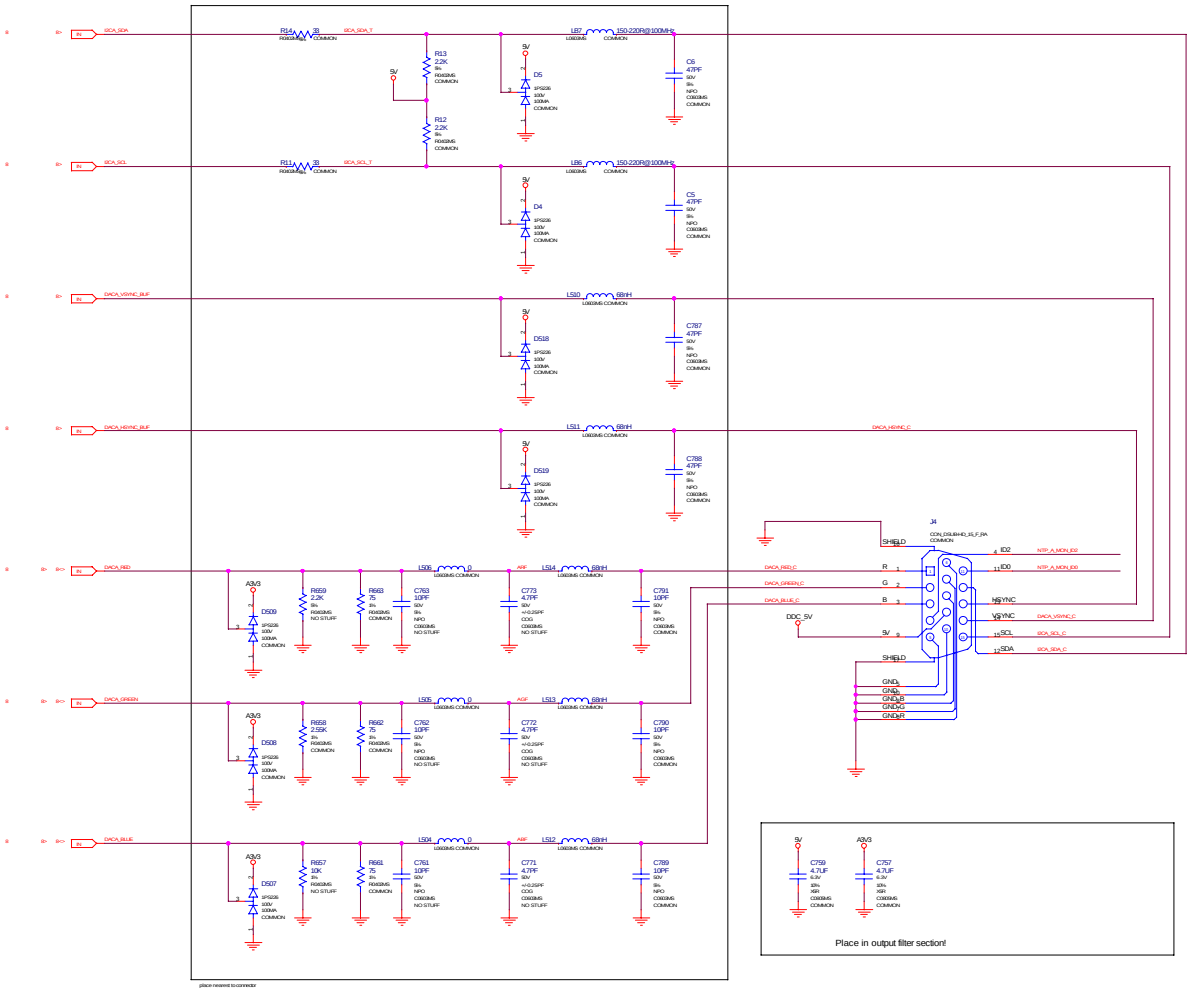
Size	Document Number: NV31 DAC_A, DAC_B, PLL, SYNC Buffer — Rev: 300
Custom	
Date: Monday, March 31, 2003	Sheet 8 of 17

Primary Display (DACA), DB15 only!



EMI-FILTER



Place all filter components on the side nearest to the reference GND plane!

Route all signals only on layers referenced to GND!

Don't split the reference GND plane beneath a RGB signal!

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MS-8912 base on P141-A03 modify

Size	Document Number	Rev
Custom	Primary Display (DACA), DB15 only!	300
Date: Monday, March 31, 2003	Sheet 9 of 17	

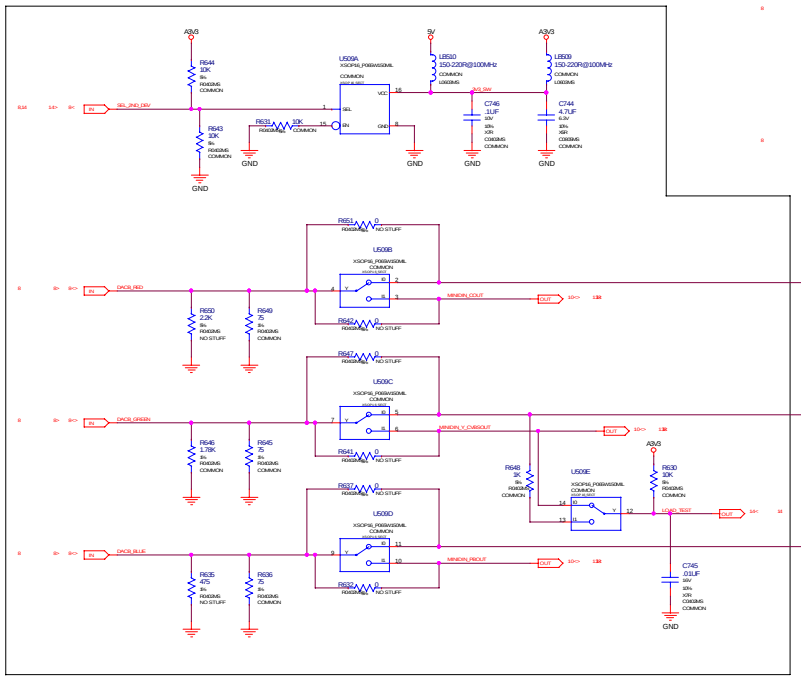
Secondary Display (DACB), SILM DB15 optional
DVI-I

Place all filter components
on the side nearest to the
reference GND plane!

Route all signals only on
layers referenced to GND!

Don't split the reference
GND plane beneath
a RGB signal!

DACB Multiplexer



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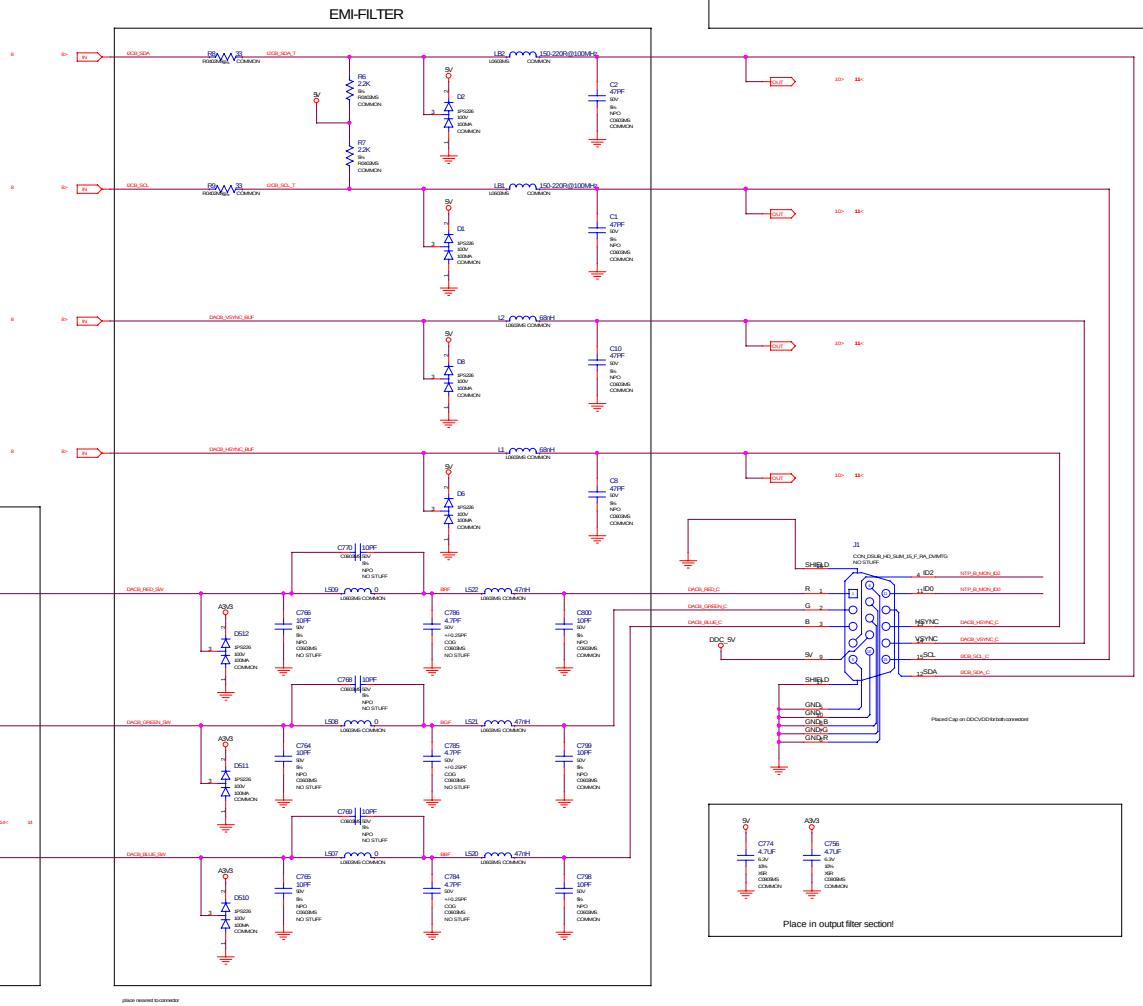

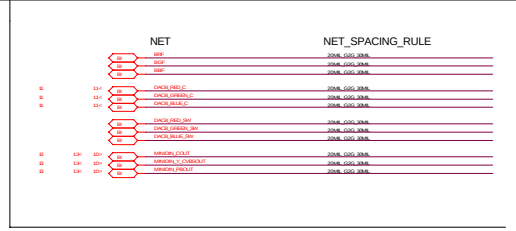

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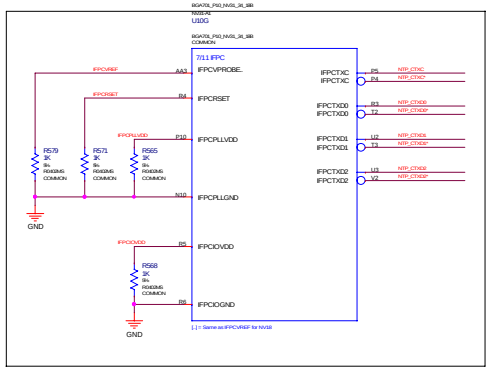
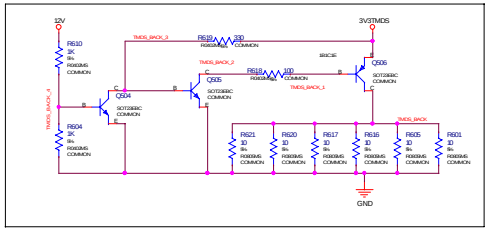
MS-8912 base on P141-A03 modify			
Size: Custom	Document Number: Secondary Display (DACB), SILM DB15 optional DVI-I		Rev: 300
Date: Monday, March 31, 2003		Sheet: 10 of 17	

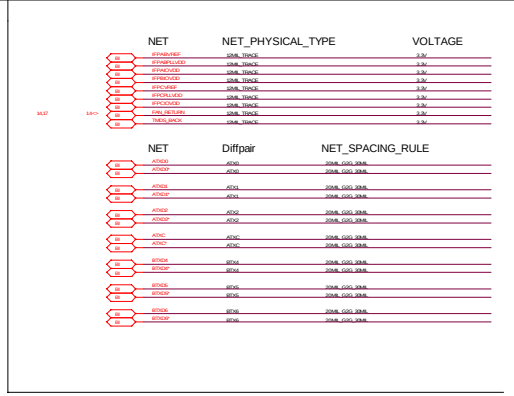
INTERNAL DUAL LINK TMDS POWER AND DECOUPLING

Unused Transmitter

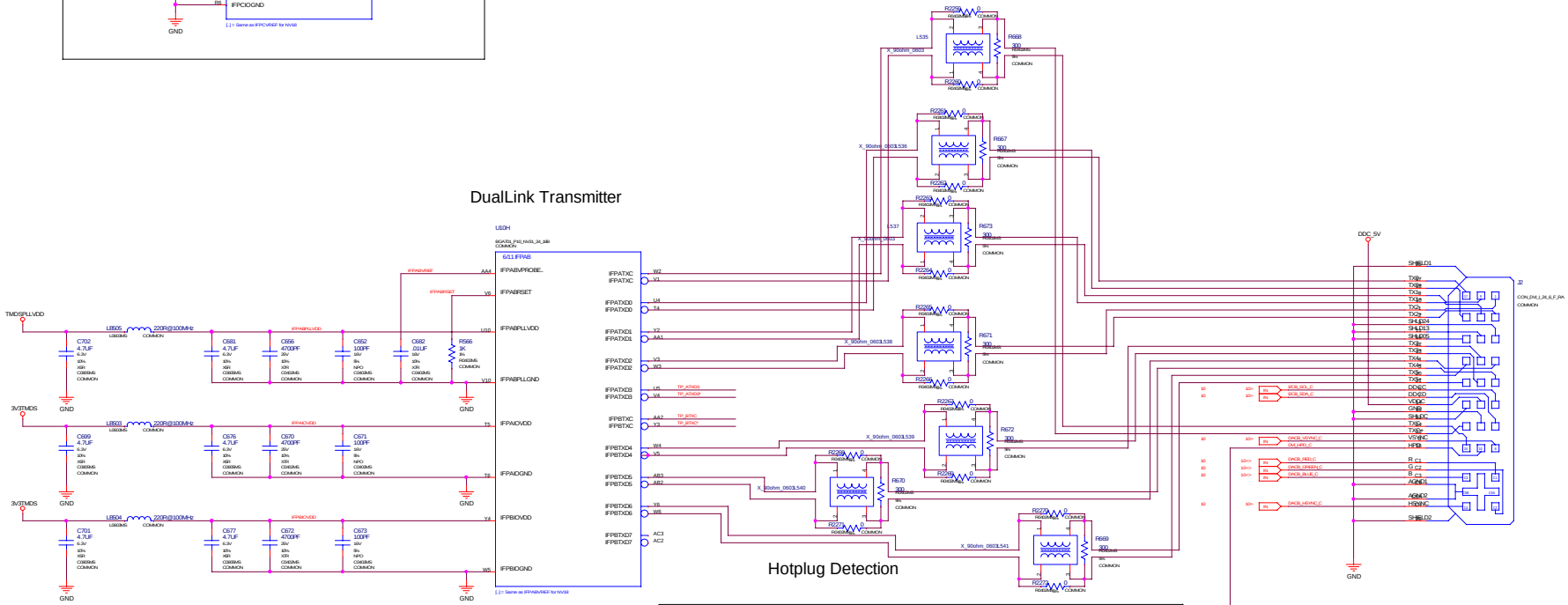


TMDS backdrive prevention

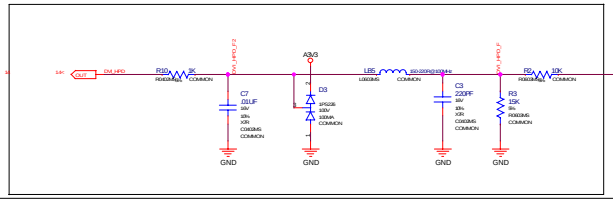


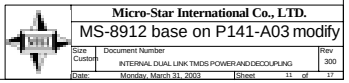


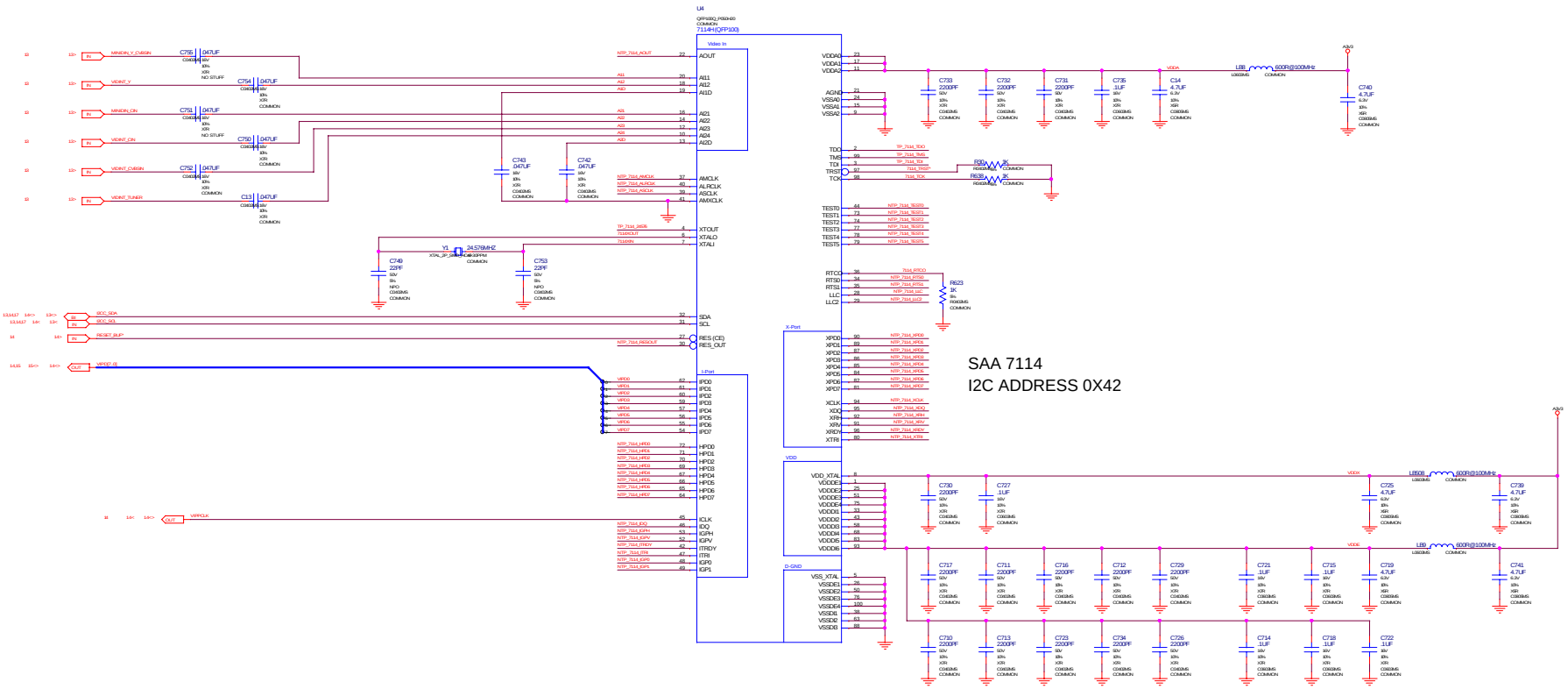
DualLink Transmitter



Hotplug Detection







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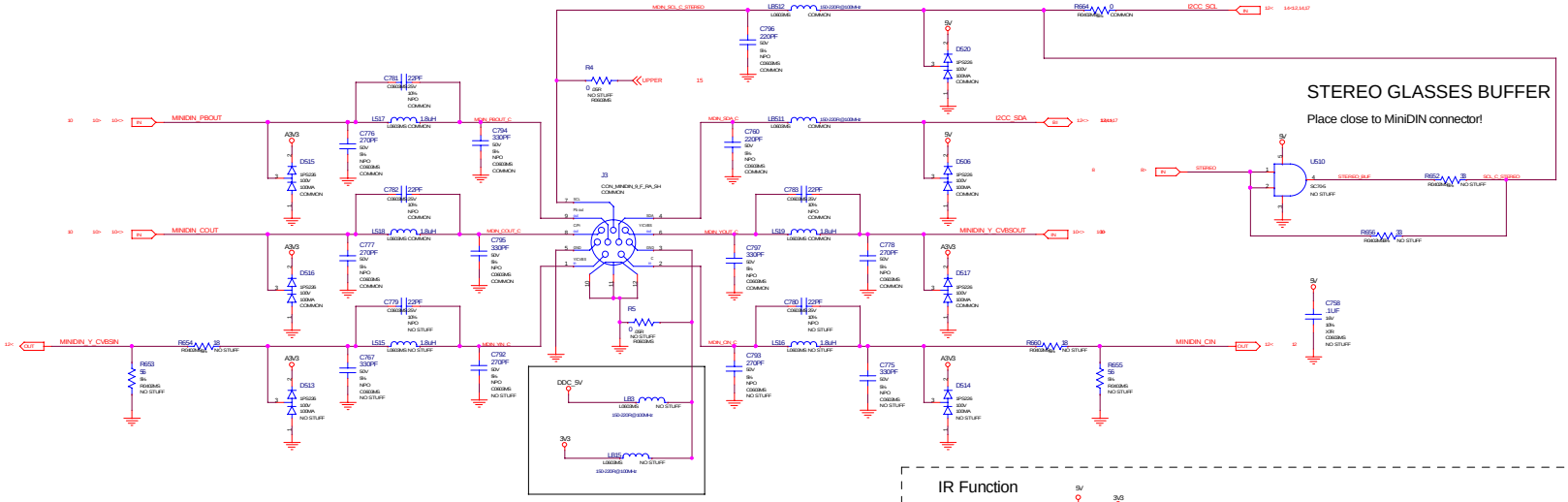
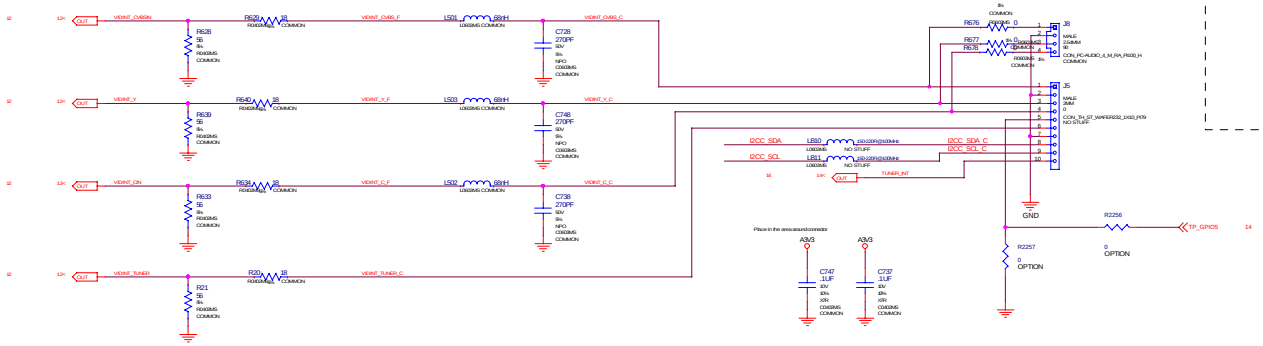
MS-8912 base on P141-A03 modify	
Size: Custom	Document Number: VIDEO CAPTURE
Rev: 300	
Date: Monday, March 31, 2003	Sheet 12 of 17

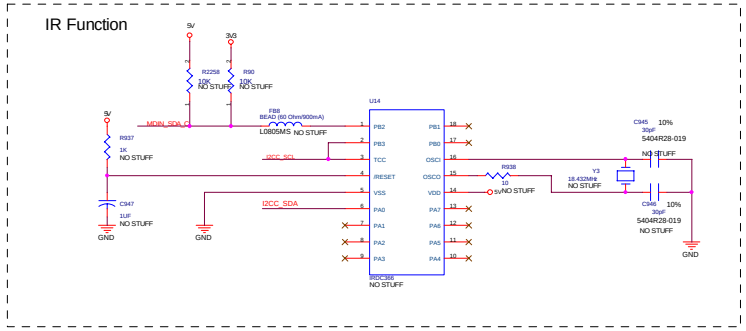
VIDEO IN/OUT CONNECTOR /STEREO GLASSES



INTERNAL VIDEO IN CONNECTOR



IR Function



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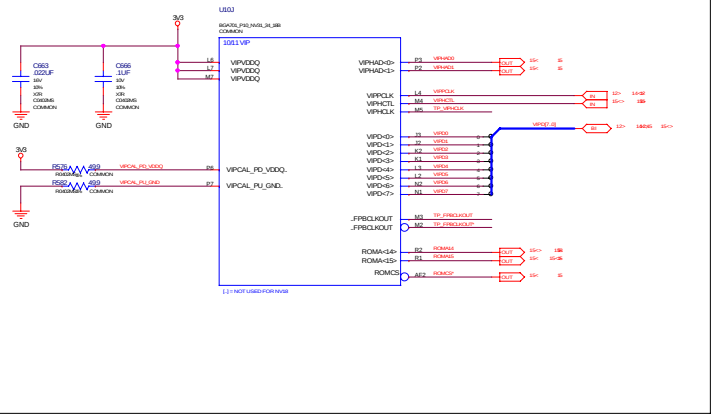
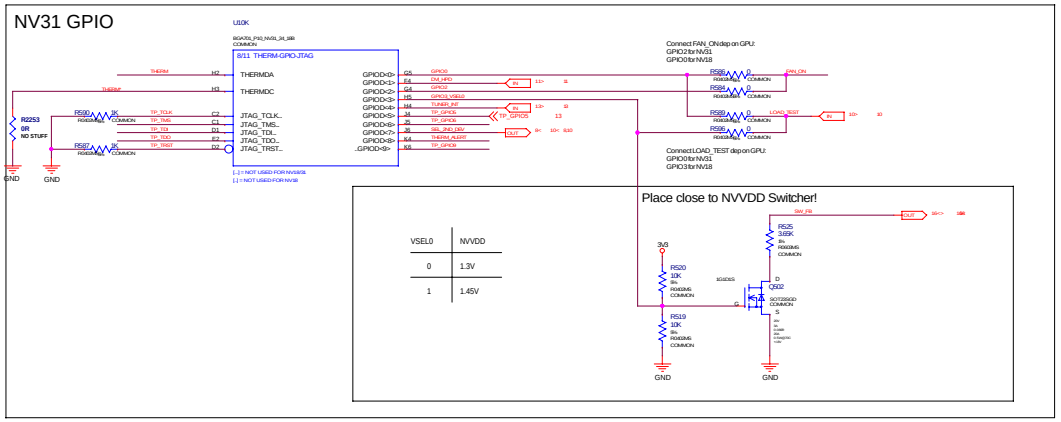
MS-8912 base on P141-A03 modify		
Size: Custom	Document Number: MINIDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES	Rev: 300
Date: Monday, March 31, 2003	Sheet: 13 of 17	

NV31 DVO, VIP AND GPIO SECTION, FAN CONTROL AND TEMP SENSOR

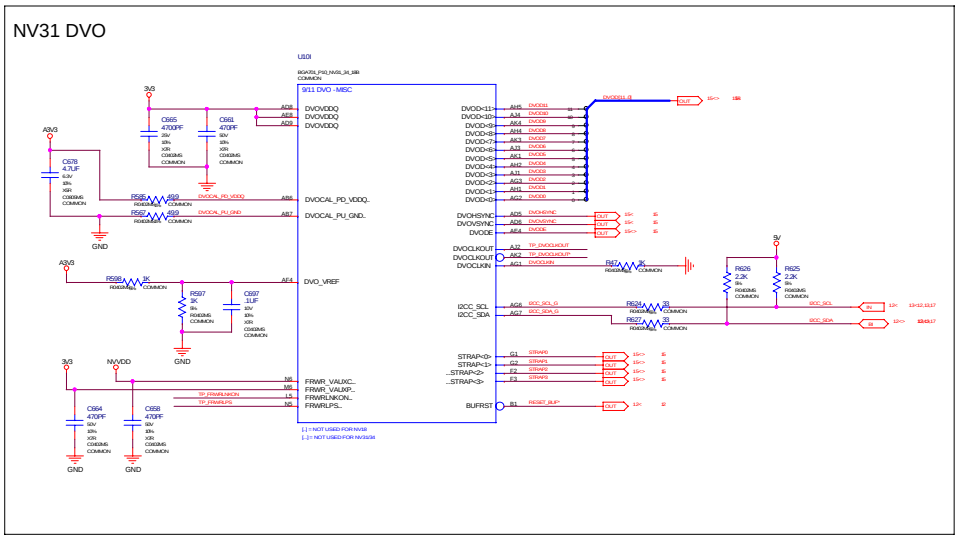
NV31 VIP



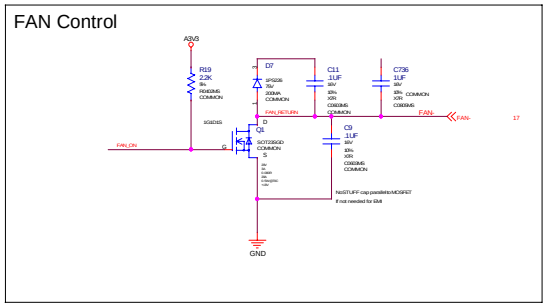
NV31 GPIO



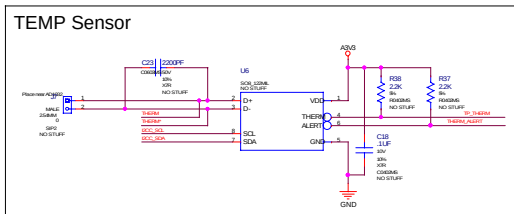
NV31 DVO



FAN Control

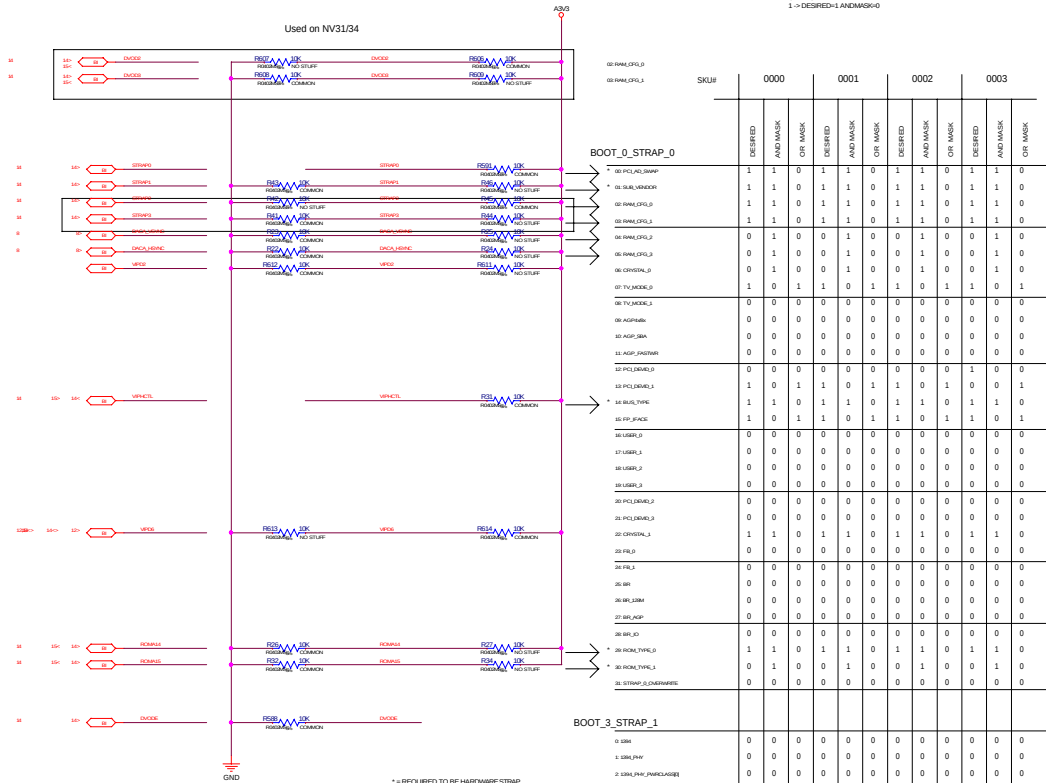


TEMP Sensor



Micro-Star International Co., LTD.		
MS-8912 base on P141-A03 modify		
Size	Document Number	Rev 300
Custom	NV31 DVO, VIP AND GPIO SECTION, FAN CONTROL AND TEMP SENSOR	
Date: Monday, March 31, 2003	Sheet 14 of 17	

NV31 BIOS STRAPPING



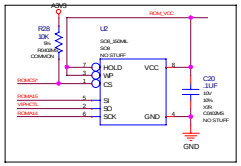
SKU#	0000			0001			0002			0003		
	DESIRED	AND MASK	OR MASK	DESIRED	AND MASK	OR MASK	DESIRED	AND MASK	OR MASK	DESIRED	AND MASK	OR MASK
BOOT_0_STRAP_0												
* 00: PCI_AD_SWAP	1	1	0	1	1	0	1	1	0	1	1	0
* 01: SUB_VENDOR	1	1	0	1	1	0	1	1	0	1	1	0
02: RAM_CFG_0	1	1	0	1	1	0	1	1	0	1	1	0
03: RAM_CFG_1	1	1	0	1	1	0	1	1	0	1	1	0
04: RAM_CFG_2	0	1	0	0	1	0	0	1	0	0	1	0
05: RAM_CFG_3	0	1	0	0	1	0	0	1	0	0	1	0
06: CRYSTAL_0	0	1	0	0	1	0	0	1	0	0	1	0
07: TV_MODE_0	1	0	1	1	0	1	1	0	1	1	0	1
08: TV_MODE_1	0	0	0	0	0	0	0	0	0	0	0	0
09: AGPrate	0	0	0	0	0	0	0	0	0	0	0	0
10: AGP_SBA	0	0	0	0	0	0	0	0	0	0	0	0
11: AGP_FASTWR	0	0	0	0	0	0	0	0	0	0	0	0
12: PCI_DEVEL_0	0	0	0	0	0	0	0	0	0	1	0	0
13: PCI_DEVEL_1	1	0	1	1	0	1	1	0	1	0	0	1
* 14: BUS_TYPE	1	1	0	1	1	0	1	1	0	1	1	0
15: FP_IFACE	1	0	1	1	0	1	1	0	1	1	0	1
16: USER_0	0	0	0	0	0	0	0	0	0	0	0	0
17: USER_1	0	0	0	0	0	0	0	0	0	0	0	0
18: USER_2	0	0	0	0	0	0	0	0	0	0	0	0
19: USER_3	0	0	0	0	0	0	0	0	0	0	0	0
20: PCI_DEVID_2	0	0	0	0	0	0	0	0	0	0	0	0
21: PCI_DEVID_3	0	0	0	0	0	0	0	0	0	0	0	0
22: CRYSTAL_1	1	1	0	1	1	0	1	1	0	1	1	0
23: FB_0	0	0	0	0	0	0	0	0	0	0	0	0
24: FB_1	0	0	0	0	0	0	0	0	0	0	0	0
25: BR	0	0	0	0	0	0	0	0	0	0	0	0
26: BR_128M	0	0	0	0	0	0	0	0	0	0	0	0
27: BR_AGP	0	0	0	0	0	0	0	0	0	0	0	0
28: BR_IO	0	0	0	0	0	0	0	0	0	0	0	0
* 29: ROM_TYPE_0	1	1	0	1	1	0	1	1	0	1	1	0
* 30: ROM_TYPE_1	0	1	0	0	1	0	0	1	0	0	1	0
31: STRAP_0_OVERWRITE	0	0	0	0	0	0	0	0	0	0	0	0
BOOT_3_STRAP_1												
0: 1394	0	0	0	0	0	0	0	0	0	0	0	0
1: 1394_PHY	0	0	0	0	0	0	0	0	0	0	0	0
2: 1394_PHY_PWRCLASS[0]	0	0	0	0	0	0	0	0	0	0	0	0
3: 1394_PHY_PWRCLASS[1]	0	0	0	0	0	0	0	0	0	0	0	0
4: VGA_DEVICE	1	0	1	1	0	1	1	0	1	1	0	1
5: MEM_LSB_SWAP	0	0	0	0	0	0	0	0	0	0	0	0
6: BR_LAST_DEV	0	0	0	0	0	0	0	0	0	0	0	0
7: BR_BNRS_BCASTONLY	0	0	0	0	0	0	0	0	0	0	0	0
31: STRAP_1_OVERWRITE	0	0	0	0	0	0	0	0	0	0	0	0

600-01641-0000
600-01641-0001
600-01641-0002

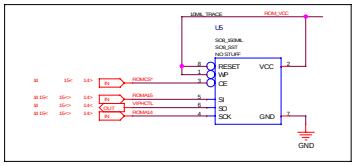
600-01641-0003

NV Register Description	NV Address	BIOS Address	Data SKU#0000-0002	Data SKU#0003
BOOT_0_STRAP_0 0x00101000			0x2040E08F	0x2040C08F
BOOT_1_STRAP_0_ANDMASK 0x00101004		0x58	0x6040407F	0x6040407F
BOOT_2_STRAP_0_ORMASK 0x00101008		0x5C	0x00008080	0x00008080
BOOT_3_STRAP_1 0x0010100C			0x00000010	0x00000010
BOOT_4_STRAP_1_ANDMASK 0x00101010		0x60	0x00000000	0x00000000
BOOT_5_STRAP_1_ORMASK 0x00101014		0x64	0x00000010	0x00000010

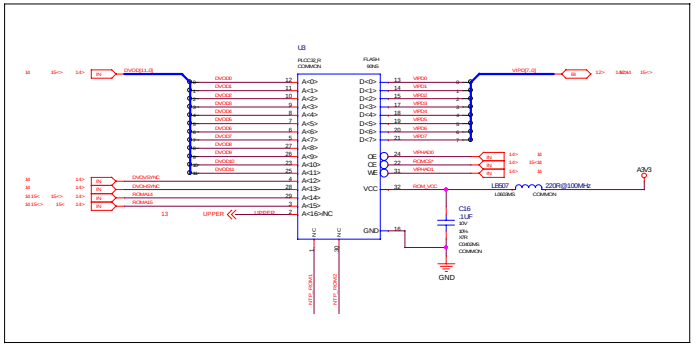
BIOS (serial)



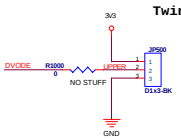
BIOS (serial alternative)



BIOS (parallel alternative)



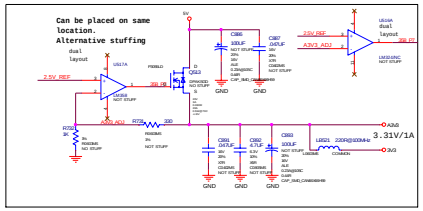
Twin BIOS



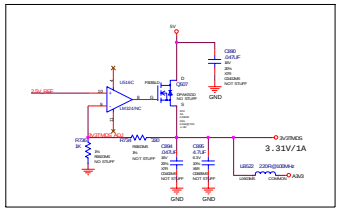
Micro-Star International Co., LTD.			
MS-8912 base on P141-A03 modify			
Size: Custom	Document Number: NV31 BIOS STRAPPING		Rev: 300
Date: Monday, March 31, 2003	Sheet: 15 of 17		

POWER SUPPLY

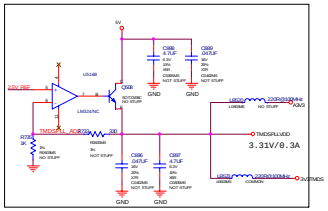
ANALOG 3V3



TMDS 3V3 Supply

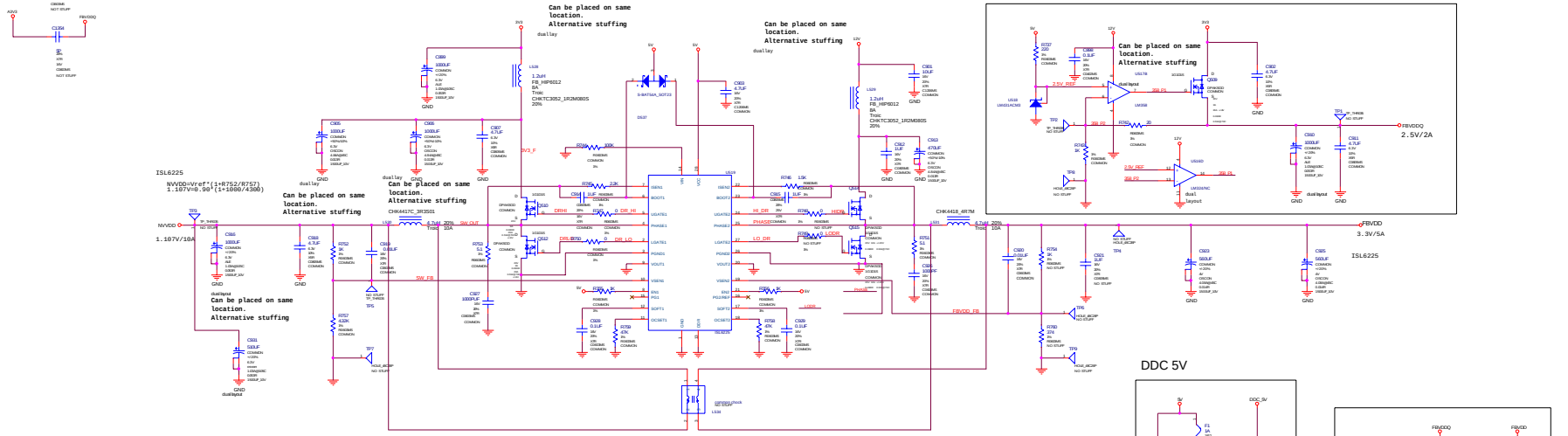


TMDS PLL Supply

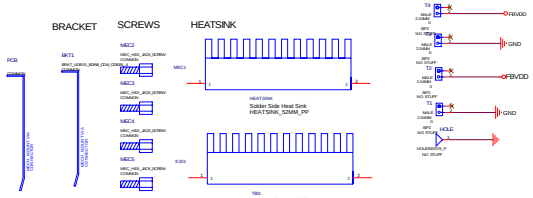


NVVDD-SWITCHER / FBVDDQ-LDO CONT ROLER

Replaced ISL6529 with ISL6225.
Replaced P07DG3LV with APM7312.



BRACKET SCREWS HEATSINK



FBVDDQ= VRef * (1+Rtop/ Rbot)

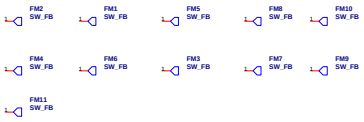
ISL6529	2.5V = 0.800V * (1+2.37k/1.13k)
SC2610	2.5V = 1.250V * (1+1.02k/1.02k)

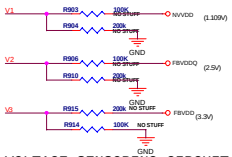
Vo=[0.9V*(Rtop +Rbot)] / Rbot

ISL6225	FBVDD = [0.9V * (1K+375)] / 375=3.3V
NV31	NVVDD= 0.9V * (1K+4.3K)] / 4.3K
NV18B	Stable Volt need 1.656 V.

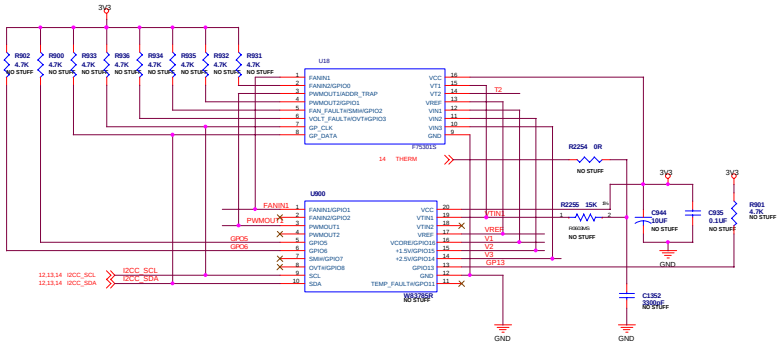
Micro-Star International Co., LTD.	
MS-8912 base on P141-A03 modify	
Size: D	Document Number: POWER SUPPLY
Date: Monday, March 31, 2003	Sheet: 38 of 59

H/W Monitor Funtion

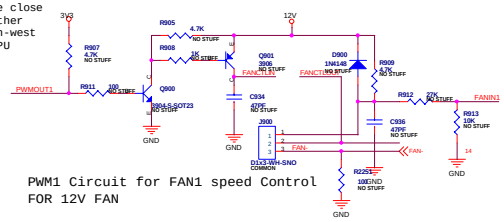




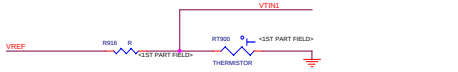
VOLTAGE SENSORING CIRCUIT



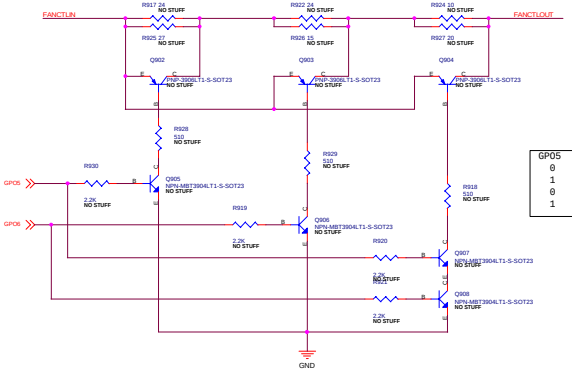
Place close
together
south-west
of GPU



PWM1 Circuit for FAN1 speed Control
FOR 12V FAN



TEMPERATURE SENSORING CIRCUIT



GPO5	GPO6	Q1	Q2	Q3	Vout
0	0	off	off	off	9V
1	0	on	off	off	10V
0	1	off	on	off	11V
1	1	on	on	on	12V

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MS-8912 base on P141-A03 modify		
Size: Custom	Document Number: H/W Monitor Funtion	Rev: 300
Date: Monday, March 31, 2003	Sheet: 17 of 17	