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P160 HISTORY:

X00	INITIAL VERSION
X01	Cleaned up schematics - changes from initial design review meeting
X02	Imported board file #65 and synchronized with latest version of schematics
Х03	Nov 18/02 - Replaced LB502 with an 805 bead, changed PLLVDD rail to 3V3 instead of A3V3, and removed AGPVDDQ deoupling caps C130, C257, and C570.
X04	Nov 21/02 - C75 is changed to decouple 3V3 to GND.
X05	Nov 22/02 - VIP interface rail changed to 3V3 instead of A3V3 due to short between VIPVDDQ and VDD33.
X06	Nov 25/02 - FRWR_VAUXP rail changed to 3V3.
X07	Nov 26/02 - Changed DACB_LOAD_TEST GPIO assignment for NV34.
X08	Dec 02/02 - AGP_PLL_VDD and FB_DLLVDD are supplied from A3V3 rail.

P162-A00 History:

- 1-Added P162 specific features:
 - SW PS, TMDS LinkA, Backdrive, new slim VGA, Fan Cntl.
 - Added Current sharing, TMDS IO and PLL linear regulators.
- 2-Added TH parts in PS section as ALT.
- 3-Added SST serial support.
- 4-Changed AGP_PLL_VDD, FB_PLLVDD, DAC_A/B_VDD and PLL_VDD to A3V3.
- 5-Added 10 caps as part of P160 sync up.
- 6-Added PU resitors on Jtag TMS and TDI
- 7-Incorporated recommendations from PS Vendor.
- 8-Added extra X elements near connectors to bridge CGND and GND cut.
- 9-Added an option to use a single dual FET for low end bd.
- 10-Fixed error on 6529 power good and current supplement.
- 11-Changed C302 to 0603 (too big pkg for .1uf in 0805)
- 12-Deleted C296 and C293 (shared them with C313, C324)
- 13-Changed C329 and C324 to 0603 pkg.
- 14-Removed alternate Semtech SW (could not route).

- Changes after the design review:
 1-Remove C301 and R137-left over from Semtech PS circuit.
 - 2-Remove sync buffer bypass resistors.
- 3-Remove R122 and R123 from Intersil power rails.
- 4-Add snubber circuit for NVVDD PS.
- 5-Add PD res on TP_XTALOUTBUF to terminate the signal.
- 6-Fan controler PU to 3V3 from A3V3.
- 7-Cleaned up Unnamed nets.
- 8-Split CGND into 2 nets (added CGND1 to J6.25 and J2. 16).
- 9-Added PD resistor on FAN ON.
- 10-Added 8 caps for DQS/DQM routings that break plane reference.

X-RELEASE.

P162-A01 History:

Merged net IFPBIOVDD with IFPAIOVDD.

Merged Q4 and Q5 into one package.

Implemented TV signal return scheme thru zero Ohm resistors.

P162-A02 History:

The main changes for this revision is to improve routing for DAC B and add 100ps inter-pair skew to pass EMC as modeled on A01 board. See 149- document for detail.

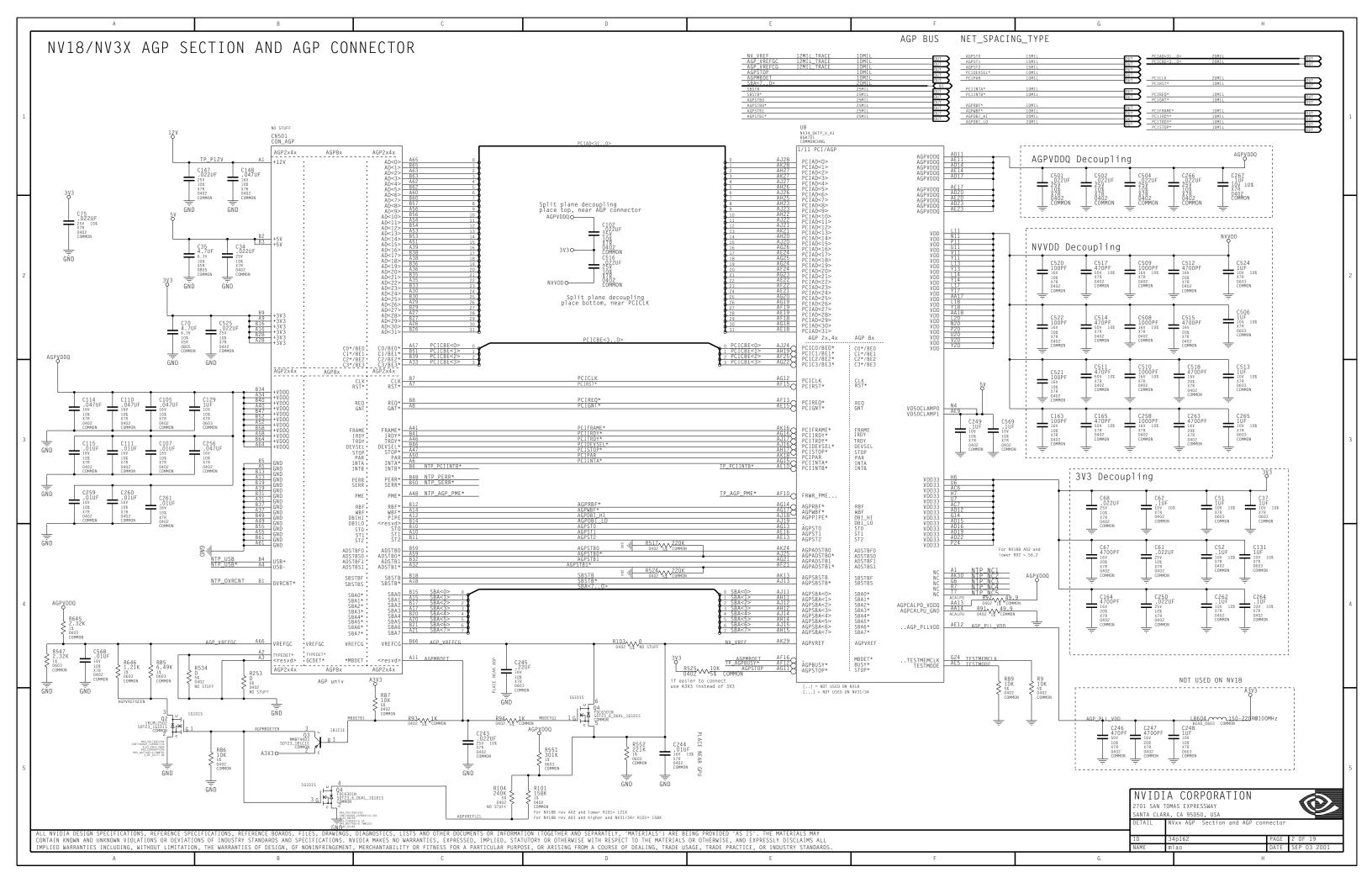
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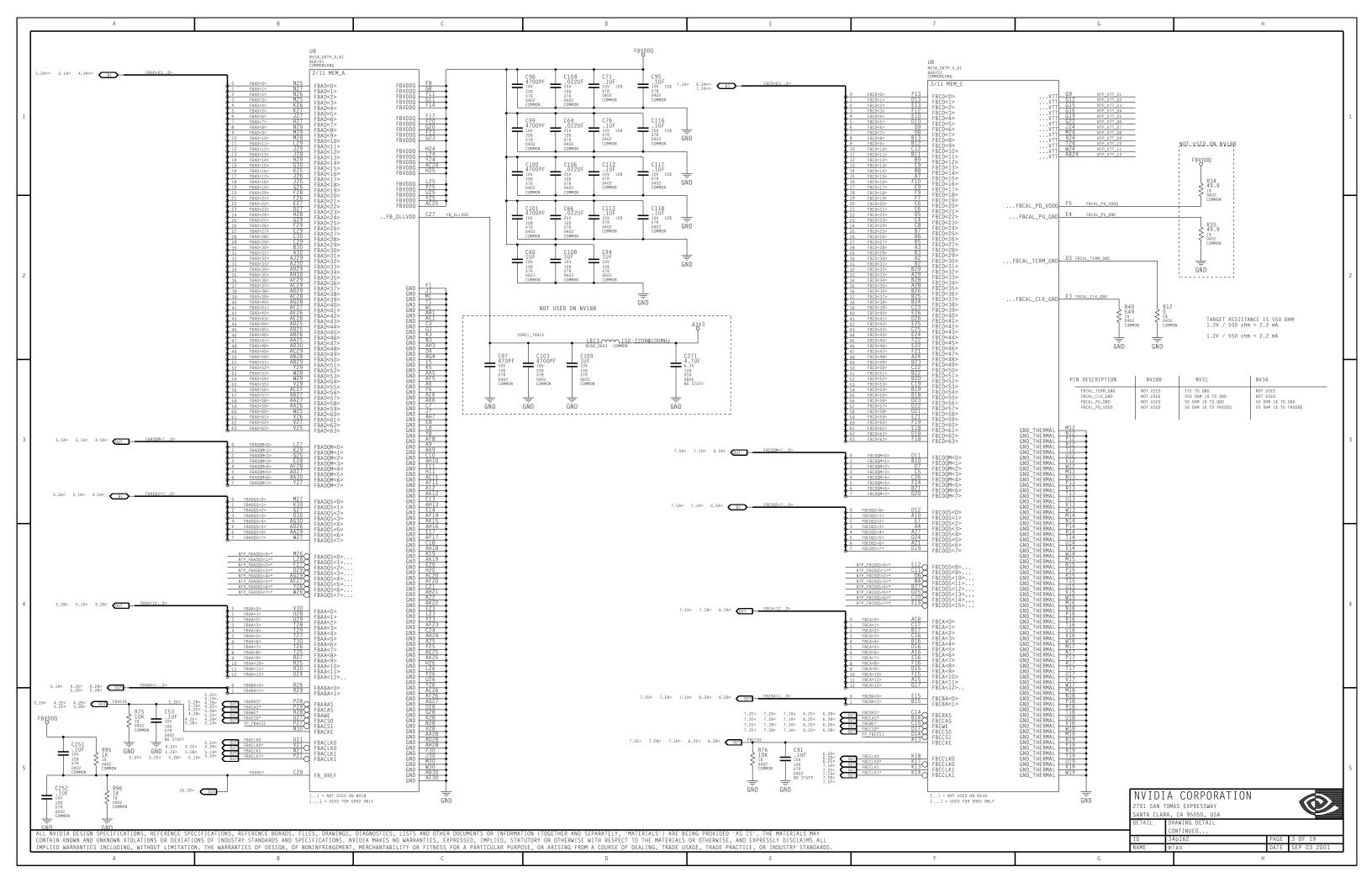
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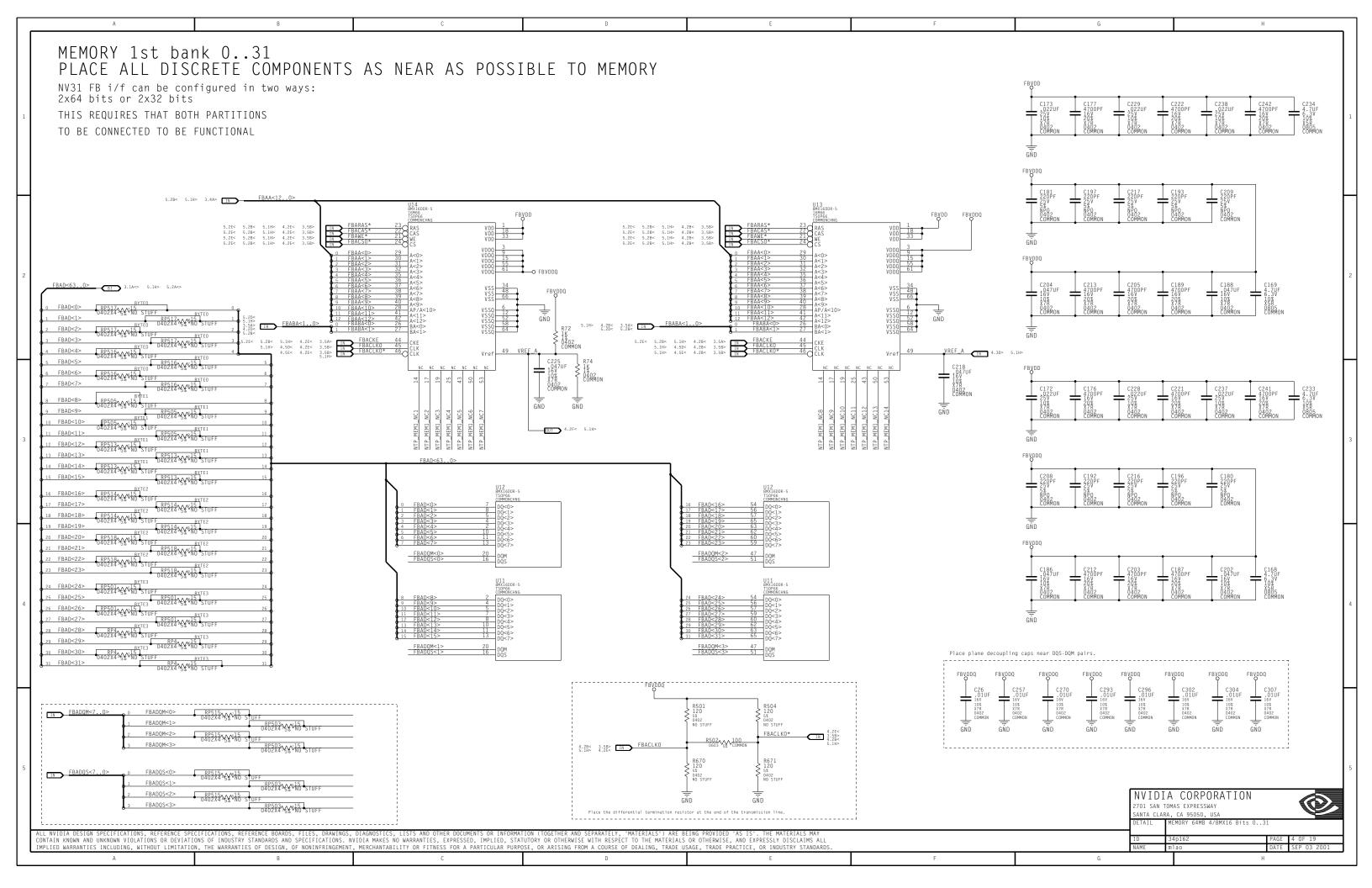
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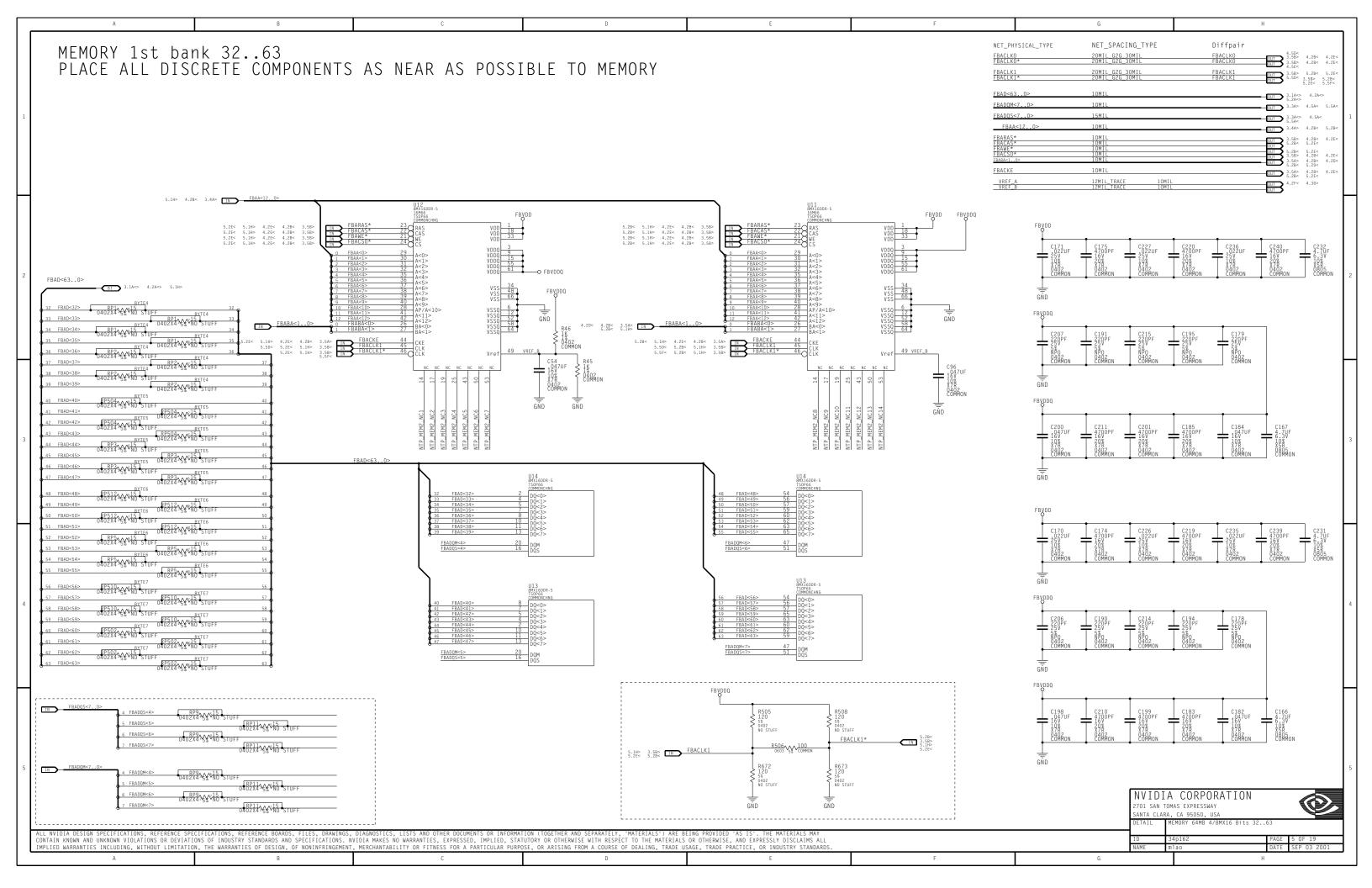
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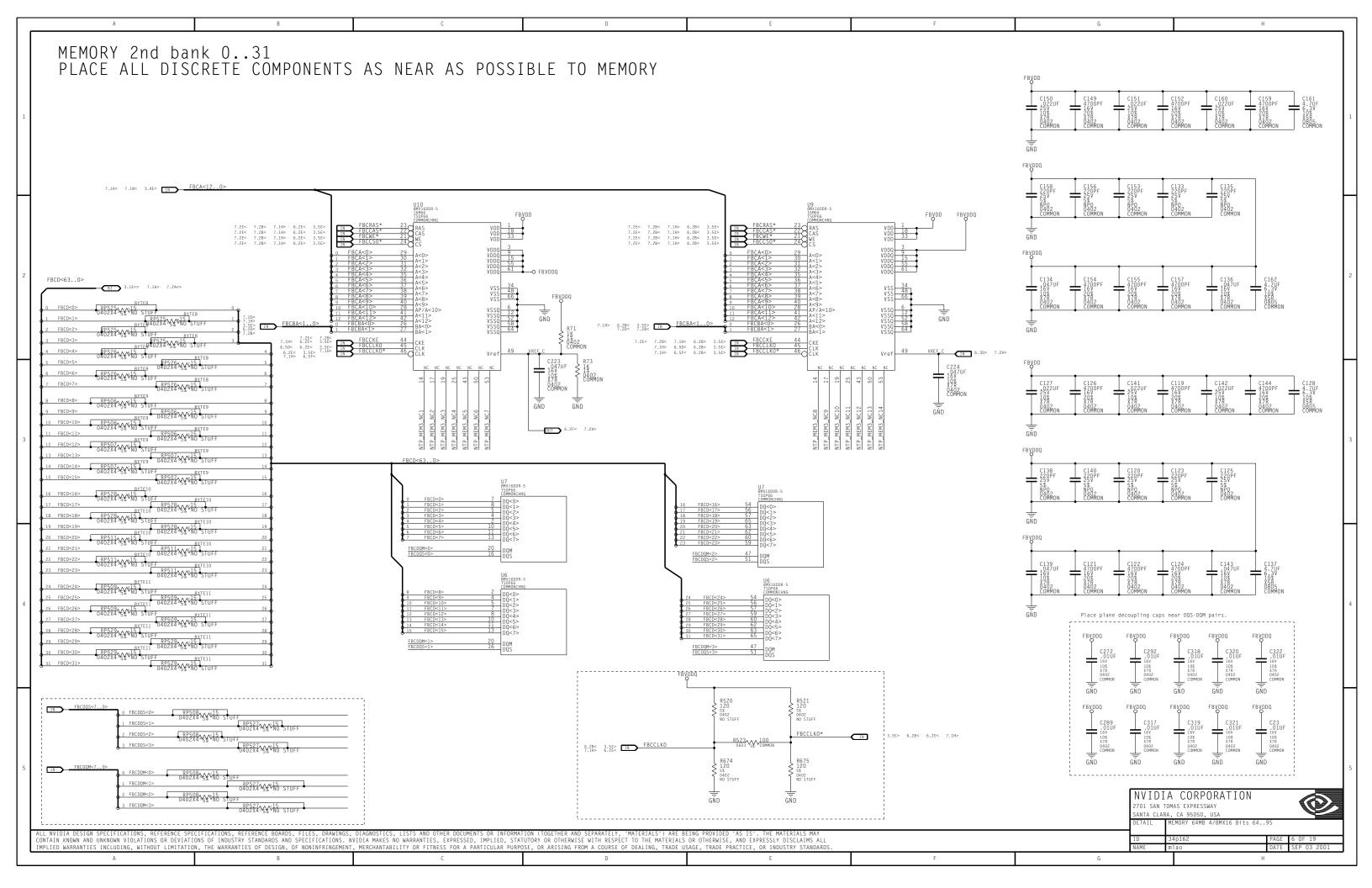
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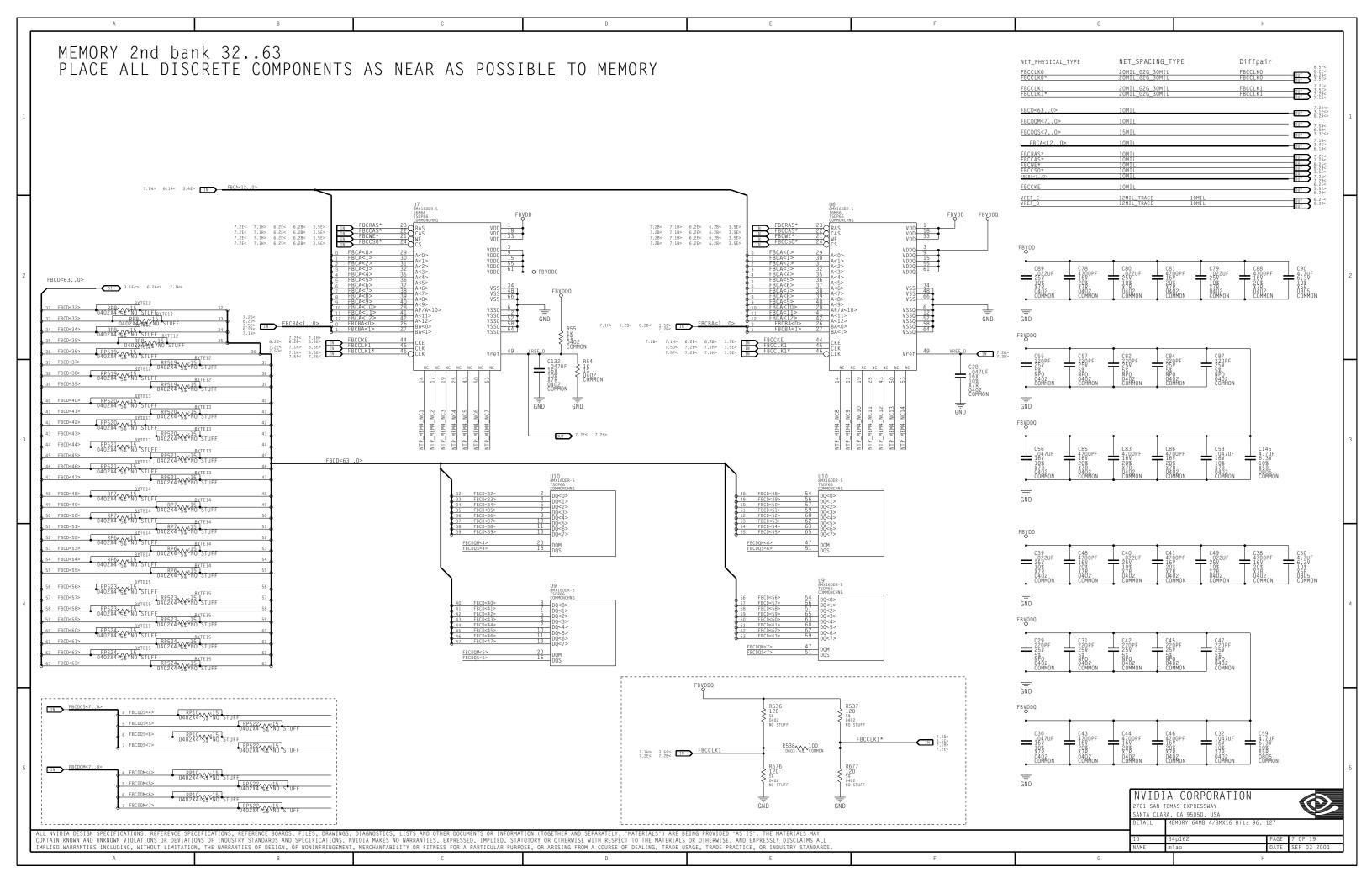


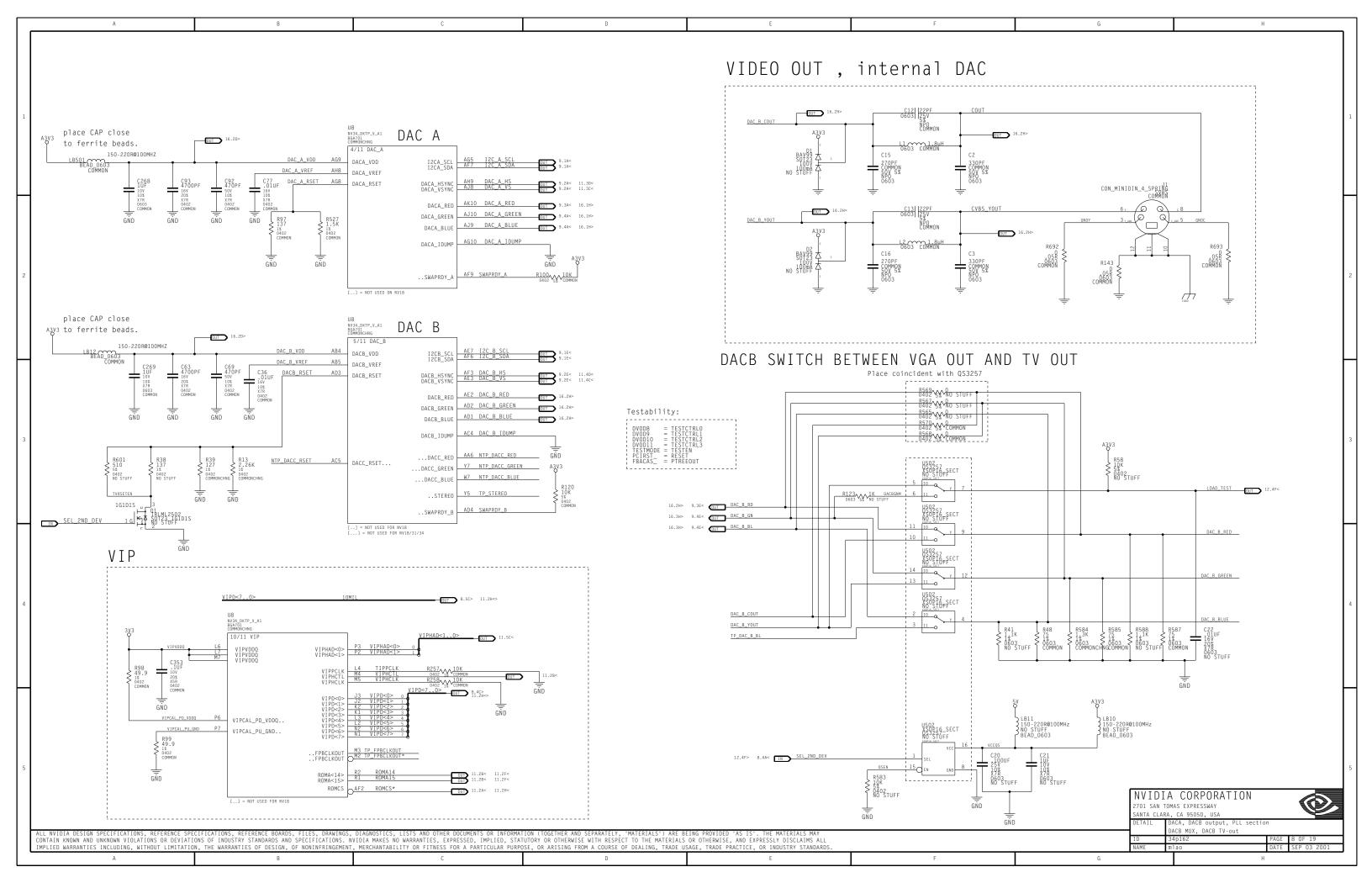


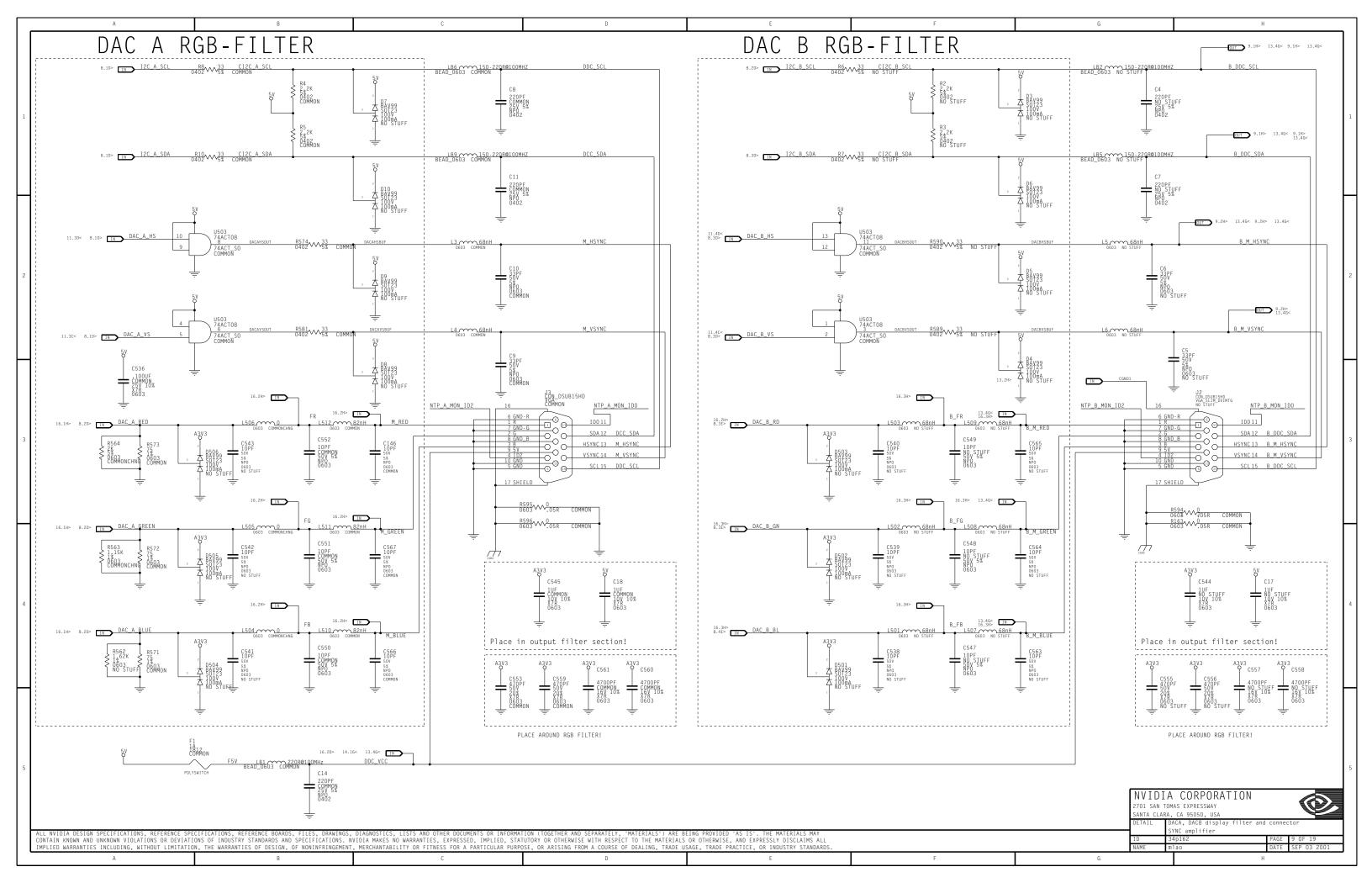




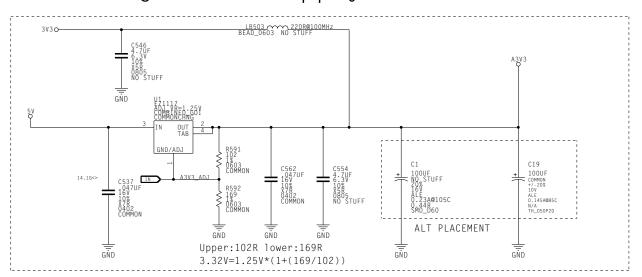




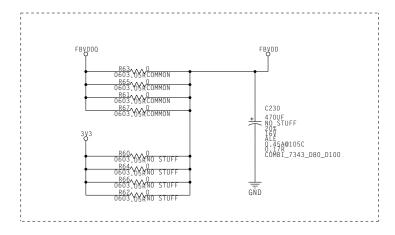


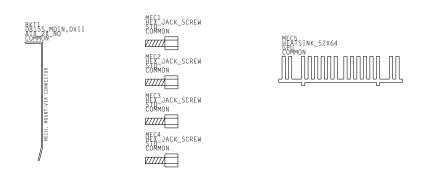


Analog Power Supply



FBVDD 3.3/2.5V

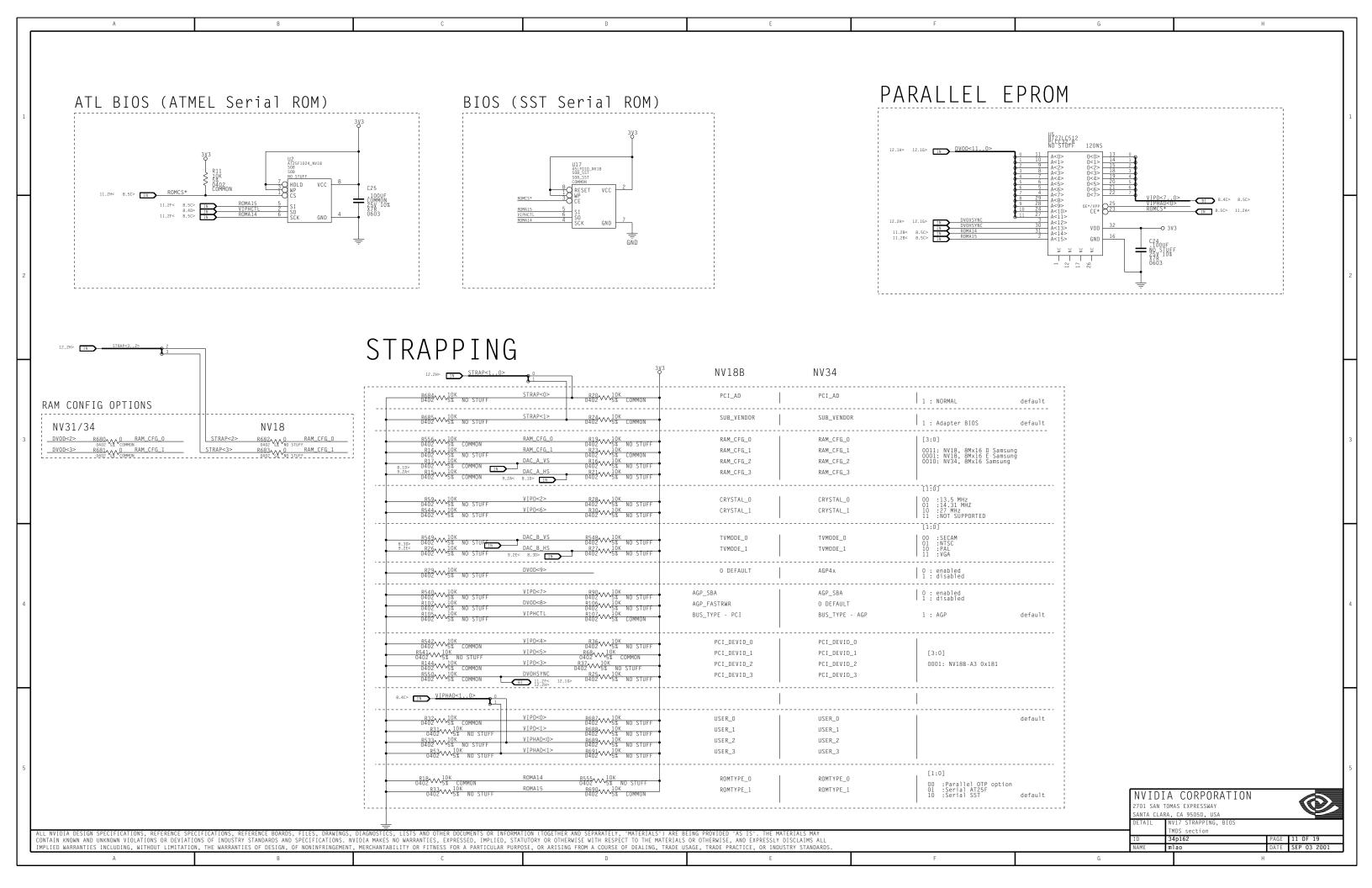


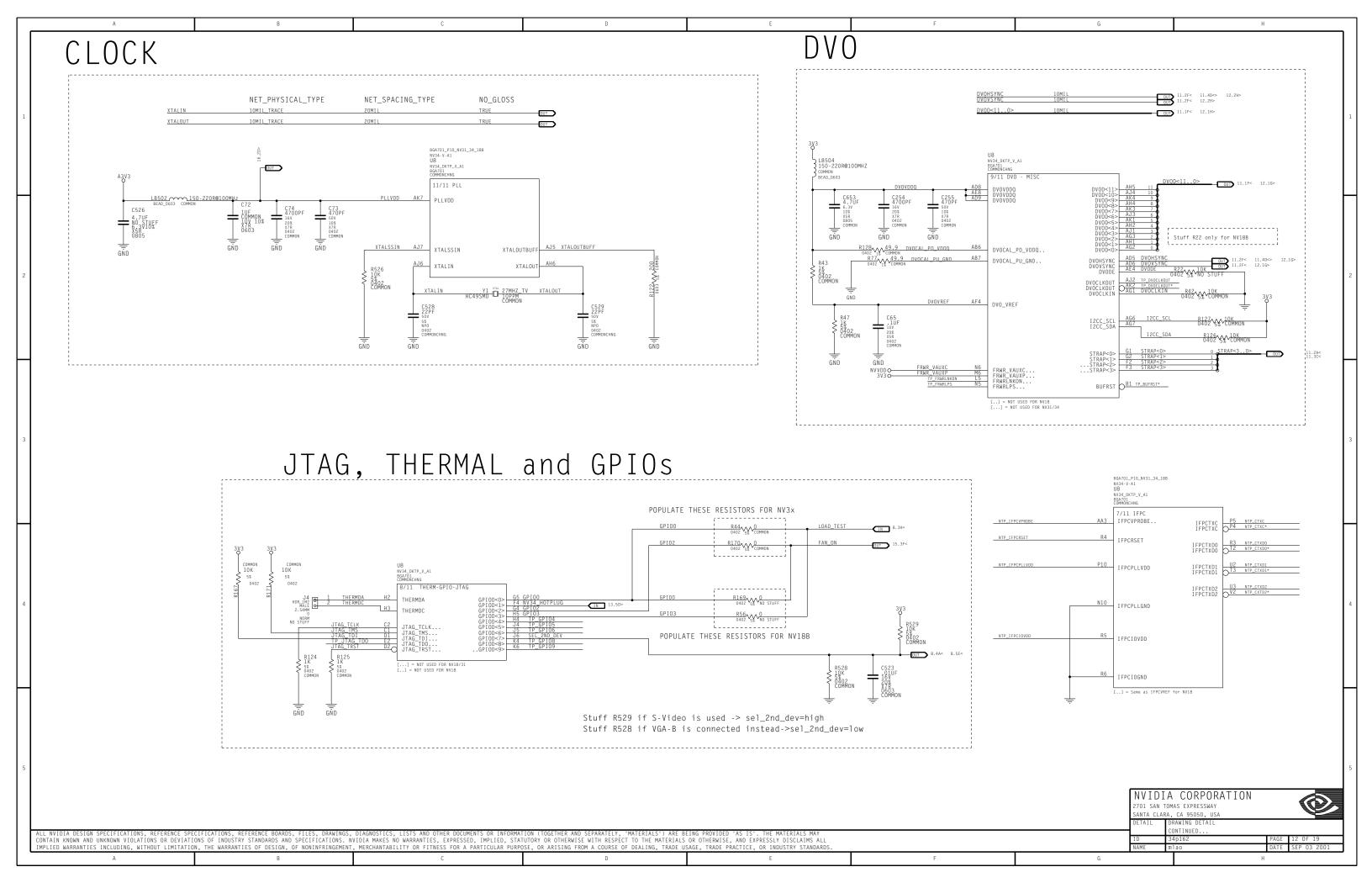


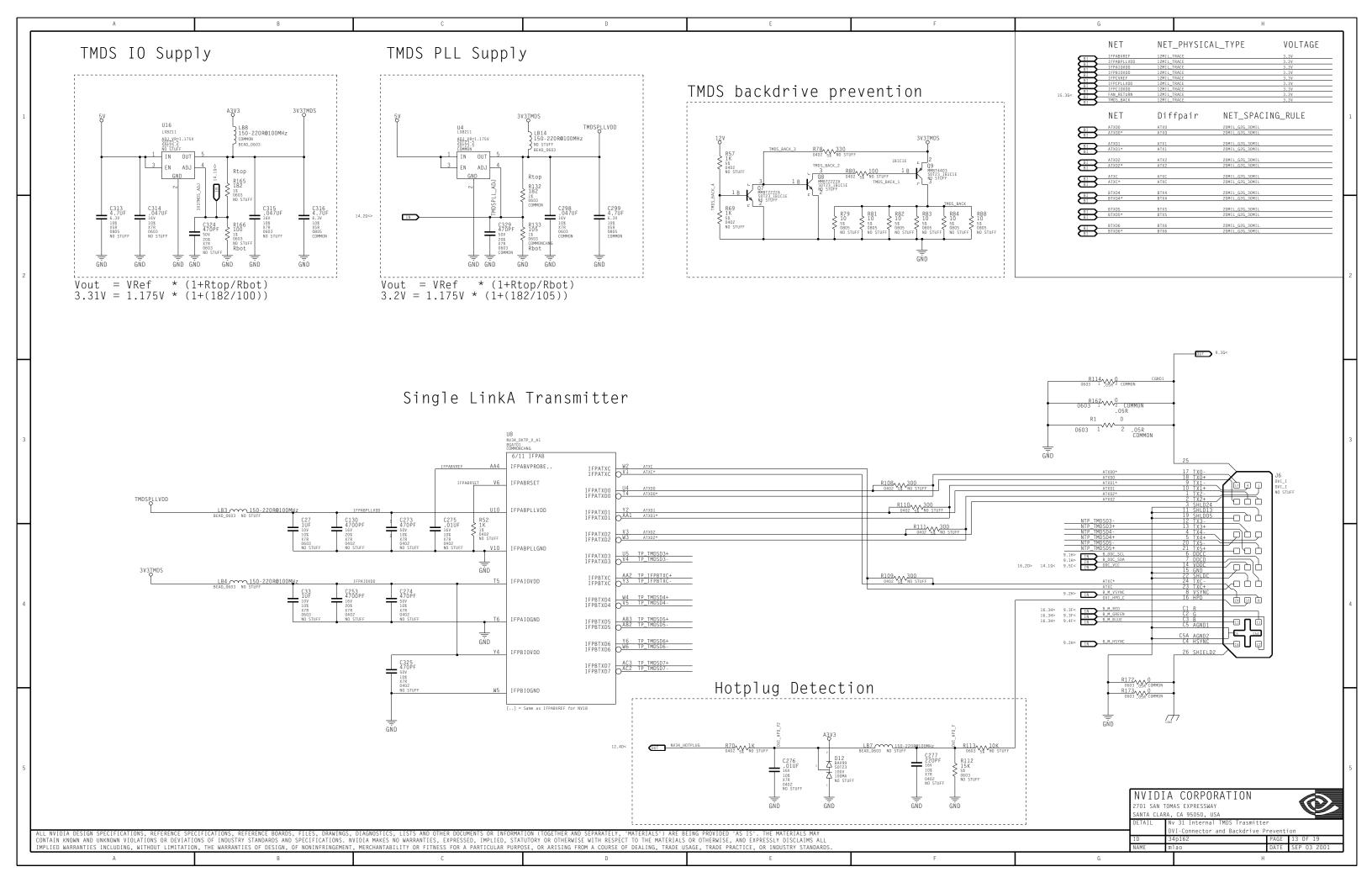
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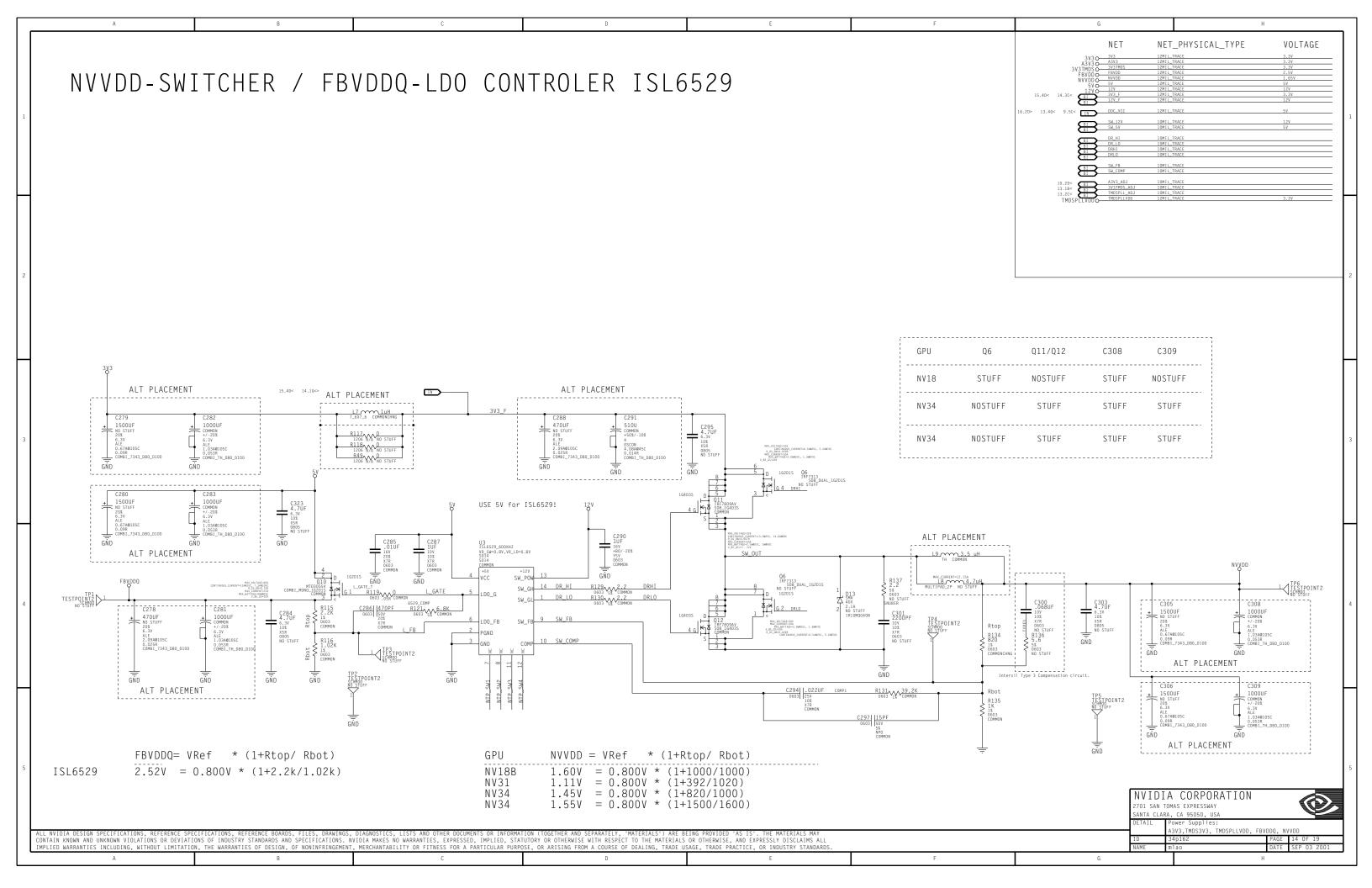
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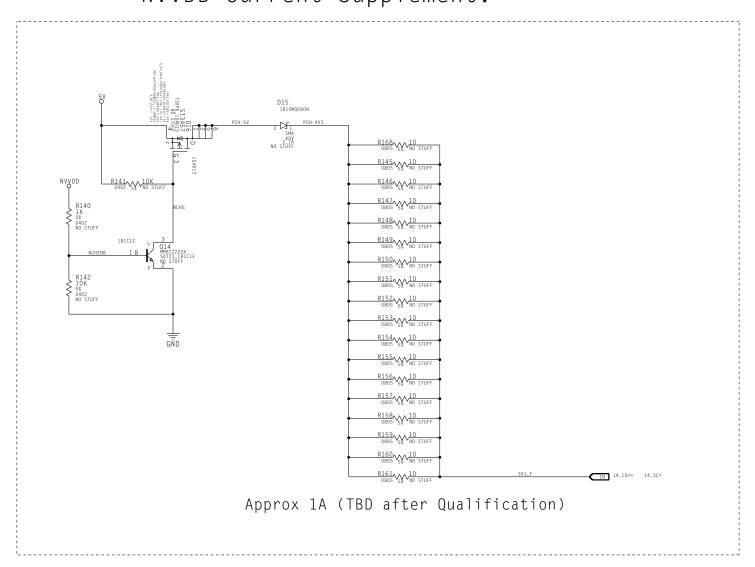




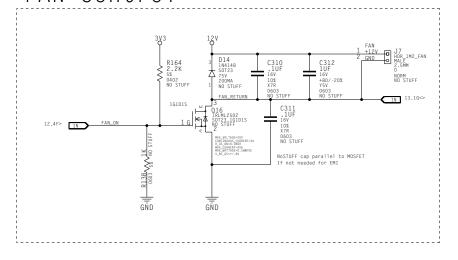




NVVDD Current Supplement.



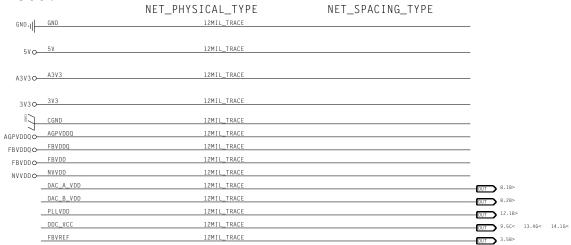
FAN Control



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NET RULES

Power Nets:



RAM_DAC : impedance controlled by constraint manager

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	NO_GLOSS	
DAC_A_RED		20MIL	TRUE	0IIT 8.2D> 9.3A<
DAC_A_GREEN		20MIL	TRUE	OUT 8.2D> 9.4A<
DAC_A_BLUE		20MIL	TRUE	OUT 8.2D> 9.4A<
FR		20MIL	TRUE	OUT 9.38<
FG		20MIL	TRUE	OUT 9.3B<
FB		20MI L	TRUE	OUT 9.4B<
M_RED		20MI L	TRUE	OUT 9.3B<
M_GREEN		20MIL	TRUE	OUT 9.3B<
M_BLUE		20MIL	TRUE	OUT 9.4B<
				_
DAC_B_RED		20MIL	TRUE	OUT 8.3D>
DAC_B_GREEN		20MIL	TRUE	OUT 8.3D>
DAC_B_BLUE		20MIL	TRUE	OUT 8.3D>
DAC_B_YOUT		20MIL	TRUE	OUT 8.2E>
DAC_B_COUT		20MIL	TRUE	OUT 8.1E>
CVBS_YOUT		20MIL	TRUE	OUT 8.26>
COUT		20MIL	TRUE	OUT 8.1F>
DAC_B_RD		20MIL	TRUE	OUT 8.3E> 9.3E<
DAC_B_GN		20MIL	TRUE	OUT 8.3E> 9.4E<
DAC_B_BL		20MIL	TRUE	OUT 8.4E> 9.4E<
B_FR		20MIL	TRUE	OUT 9.3F<
B_FG		20MIL	TRUE	OUT 9.3F<
B_FB		20MIL	TRUE	OUT 9.4F<
B_M_RED		20MI L	TRUE	OUT 9.3F< 13.4G<
B_M_GREEN		20MI L	TRUE	0UT 9.3F< 13.4G<
B_M_BLUE		20MIL	TRUE	OUT 9.4F< 13.4G<

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3.5E> 6.2B< 6.2E< 7.1H> 7.2B< 7.2E< *** Signal Cross-Reference for the entire design ** FBCCS0* 2.1H> 2.1H> FBAD<3> 3.1A 4.2A 5.1H 5.2A PCICBE<3> FRAD<4> 3.1A 4.2A 5.1H 5.2A 3.1F 6.2A 7.1H 7.2A PCTCLK A3V3_ADJ 10.2D< 14.1G<> FBAD<7> 3.1A 4.2A 5.1H 5.2A FBCD<2> 3.1E 6.2A 7.1H 7.2A PCIGNT* 2.1H> AGPDBI HI 2.1G> 2.1G> 2.1F> 2.1G> FBAD<8> 3.1A 4.2A 5.1H 5.2A FBCD<3> 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ PCIINTA* 2.1G> 2.1G> 2.1H> 2.1G> FBAD<9>
FBAD<10>
FBAD<11> 3.1E \diamond 6.2A \diamond 7.1H \diamond 7.2A \diamond 3.1A 4.2A 5.1H 5.2A AGPDBI_L AGPMBDET AGPRBF* FBCD<5> FBCD<6> PCIIRDY* AGPSTO 2.16> FBAD<12> 3.1A 4.2A 5.1H 5.2A FBCD<7> 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ PCIREO* 2.1H> FBAD<12>
FBAD<14>
FBAD<15>
FBAD<16> 2.1H> 2.1H> 2.1H> 2.1H> 12.1B> 16.2D> AGPST1 3 1Ac> 4 2Ac> 5 1H> 5 2Ac> FRCD<8> 3 1Fc> 6 2Ac> 7 1H> 7 2Ac> PCIRST* 3.1E\to 6.2A\to 7.1H\to 7.2A\to 3.2A\to 7.2A\to 7.2A\to 3.2A\to 7.2A\to 7.2A\t FBCD<10 FBCD<11> PLLVDD AGPSTB0 AGPSTB1 2.1F> FBAD<17> 3.1A 4.2A 5.1H 5.2A FBCD<12> 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ ROMA14 8.5C> 11.2B< 11.2F FBAD<18> FBAD<19> FBAD<20> 3.1A\to 4.2A\to 5.1H\to 5.2A\to 3.1A\to 4.2A\to 5.2A\to 3.2A\to 3.2A\t 3.1E \Leftrightarrow 6.2A \Leftrightarrow 7.1H \Rightarrow 7.2A \Leftrightarrow 3.1E \Leftrightarrow 6.2A \Leftrightarrow 7.1H \Rightarrow 7.2A \Leftrightarrow 3.1E \Leftrightarrow 6.2A \Leftrightarrow 7.1H \Rightarrow 7.2A \Leftrightarrow 8.5C> 11.2B< 11.2F< 8.5C> 11.2A< 11.2H< ROMA15 ROMCS* AGPWBF* FBCD<15> AGP_VREFCG 2.1F> 2.1F> FBAD<21> FBAD<22> 3.1A 4.2A 5.1H 5.2A FBCD<16> 3.1E <> 6.2A <> 7.1H > 7.2A <> SBA<7..0> 2.1F <> AGP VREFGO 3.1A 4.2A 5.1H 5.2A FBCD<17> SBA<1> 2.1F 2.1F 2.1F 2.1F FBAD<23> FBAD<24> 3.1A 4.2A 5.1H 5.2A 3.1A 4.2A 5.1H 5.2A 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ SBA<2> SBA<3> SBA<4> FBAD<25> 3.1A 4.2A 5.1H 5.2A 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ ATXDO 13.16<> FBCD<20> ATXD0* 13.16<> FBAD<26> FBAD<27> 3.1A 4.2A 5.1H 5.2A FBCD<21> 3.1F 6.2A 7.1H 7.2A SBA<5> SBA<6> 2.1F⇔ 2.1F⇔ ATYD1 3 1A<> 4 2A<> 5 1H> 5 2A<> FRCD<22 3 1F<> 6 2A<> 7 1H> 7 2A<> 13.16 13.16 FBAD<28> FBAD<29> 3.1A 4.2A 5.1H 5.2A 3.1A 4.2A 5.1H 5.2A 3.1A 4.2A 5.1H 5.2A FBCD<23> FBCD<24> 3.1E 0.2A 7.1h 7.2A 3.1E 6.2A 7.1h 7.2A 3.1E 6.2A 7.1h 7.2A SBA<7> SBSTB ATXD2* 13.16<> FBAD<30> 3.1A 4.2A 5.1H 5.2A FBCD<25> 3.1E <> 6.2A <> 7.1H > 7.2A <> FBAD<31>
FBAD<32>
FBAD<33>
FBAD<34>
FBAD<35> BTXD4 13.2G⇔ 13.2G⇔ 13.2G⇔ 3.1A 4.2A 5.1H 5.2A FBCD<262 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ SEL 2ND DEV 8.4A< 8.5F< 12.4F> 3 1A<> 4 2A<> 5 1H> 5 2A<< 3.1E 6.2A 7.1H 7.2A 3.1E 6.2A 7.1H 7.2A BTXD5* 13.2G<> 3.1A 4.2A 5.1H 5.2A FBCD<29> STRAP<3..0> 11.2A< 11.3C< 12.2H BTXD6 13.2G<> 3.1A 4.2A 5.1H 5.2A FBCD<30> 3.1E <> 6.2A <> 7.1H > 7.2A <> STRAP<1> 11.3C< 12.2H> FBAD<36> FBAD<37> FBAD<38> 3.1E \diamond 6.2A \diamond 7.1H \diamond 7.2A \diamond 3.1A 4.2A 5.1H 5.2A 3.1A 4.2A 5.1H 5.2A FBCD<31> STRAP<2> B_DDC_SCL B_DDC_SDA 9.1H> 13.4G< 9.1H> 13.4G< B_FB 9.4F< 16.3H> FBAD<39> 3.1A 4.2A 5.1H 5.2A FBCD<34> 3.1E 6.2A 7.1H 7.2A SW_5V SW_12V 14.1G<> 9.3F< 16.3H> FBAD<40> 3.1A 4.2A 5.1H 5.2A FBCD<35> 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ 14.16<> 9.3F< 16.3H> 9.4F< 13.4G< 16.3H> 9.3F< 13.4G< 16.3H> FBAD<41> FBAD<42> FBAD<43> 3.1A 4.2A 5.1H 5.2A 3.1A 4.2A 5.1H 5.2A 3.1A 4.2A 5.1H 5.2A 3.1A 4.2A 5.1H 5.2A FBCD<36> FBCD<37> FBCD<38> 3.1E \diamond 6.2A \diamond 7.1H \diamond 7.2A \diamond 14.16 14.16 13.26< 14.26 B_M_GREEN TMDSPLL_AD B M HSYNC 9.2H> 13.4G< FBAD<44> 3.1A 4.2A 5.1H 5.2A FBCD<39> 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ TMDS BACK 13.1G<> FBAD<45> FBAD<46> FBAD<47> FBAD<48> 8.4C> 8.5C> 11.2H< B M RED 9.3F< 13.4G< 16.3H 3.1A 4.2A 5.1H 5.2A FBCD<40> 3.1F 6.2A 7.1H 7.2A 3.1A 4.2A 5.1H 5.2A 3.1E\times 6.2A\times 7.1H\times 7.2A\times VIPD<7..0> VIPD<1> 8.4C> 8.5C> 11.2H 8.4C> 8.5C> 11.2H FBCD<41> FBCD<42 CGND1 COUT VIPD<2> 8.1F> 16.2H> FBCD<43> 8.4C> 8.5C> 11.2H< CVBS YOUT 8.2G> 16.2H> FBAD<49> FBAD<50> 3.1A 4.2A 5.1H 5.2A FBCD<44> 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ VIPD<3> 8.4C> 8.5C> 11.2H< DAC A BLUE 8.2D> 9.4A< 16.1H> 3.1A 4.2A 5.1H> 5.2A FBCD<45> 3.1F 6.2A 7.1H 7.2A V T PD<4> 8.4C> 8.5C> 11.2H< FBAD<51> FBAD<52> FBAD<53> 3.1E \diamond 6.2A \diamond 7.1H \diamond 7.2A \diamond 3.1A 4.2A 5.1H 5.2A 5.1A 5.2A 5.1A 4.2A 5.1H 5.2A VIPD<5> VIPD<6> DAC_A_HS 8.1D> 9.2A< 11.3D< 8.2D> 9.3A< 16.1H> FBCD<47> 8.4C> 8.5C> 11.2H< DAC_A_RED 3.1A 4.2A 5.1H 5.2A FBCD<48> VIPD<7> 8.4C> 8.5C> 11.2H< DAC A VDD 8.1B> 16.2D> FBAD<54> 3.1A 4.2A 5.1H 5.2A FBCD<49> 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ VIPHAD<0> 8.4C> 11.5C< DAC_A_VS DAC_B_BL 8.1D> 9.2A< 11.3C< 8.4E> 9.4E< 16.3H> FBAD<55 3.1E \diamond 6.2A \diamond 7.1H \gt 7.2A \diamond 3.1E \diamond 6.2A \diamond 7.1H \gt 7.2A \diamond 3.1A 4.2A 5.1H 5.2A VIPHAD<1.. DAC_B_BLUE 8.3D> 16.2H> FBAD<57 3.1A 4.2A 5.1H 5.2A FBCD<52> 3.1E <> 6.2A <> 7.1H > 7.2A <> VIPHCTL 8.4D> 11.2B< FBAD<58> DAC B COUT 8.1E> 16.2H> 3.1A 4.2A 5.1H 5.2A FBCD<53> 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ VREF A 4.2F< 4.3D> 5.1H> 8 3F> 9 4F< 16 3H> FBAD<59> 3 1Ac> 4 2Ac> 5 1H> 5 2Ac> FRCD<543 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ VREF B 8.3D> 16.2H> 8.3D> 9.2E< 11.4D< FBAD<60> FBAD<61> 3.1A 4.2A 5.1H 5.2A 3.1A 4.2A 5.1H 5.2A 5.1H 5.2A FBCD<55> FBCD<56> 3.1E 0.2A 7.1h 7.2A 3.1E 6.2A 7.1h 7.2A 3.1E 6.2A 7.1h 7.2A VREF_C VREF_D 6.2F< 6.3D> 7.2H> 7.2F< 7.2H> 7.3D> DAC_B_HS DAC_B_RD 8.3E> 9.3E< 16.2H> FBAD<62> 3.1A 4.2A 5.1H 5.2A FBCD<57> 3.1E <> 6.2A <> 7.1H > 7.2A <> XTALIN 12.1D> 12.1D> DAC B RED 8.3D> 16.2H> FBAD<63> 3.1A 4.2A 5.1H 5.2A FBCD<58> 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ XTALOUT FBADQM<0>
FBADQM<7.
FBADQM<1> 3.1E \Leftrightarrow 6.2A \Leftrightarrow 7.1H \Rightarrow 7.2A \Leftrightarrow 3.1E \Leftrightarrow 6.2A \Leftrightarrow 7.1H \Rightarrow 7.2A \Leftrightarrow 3.1E \Leftrightarrow 6.2A \Leftrightarrow 7.1H \Rightarrow 7.2A \Leftrightarrow 3.3A> 4.5A< 5.1H> 5.5A< FBCD<59 3.3A> 4.5A< 5.1H> 5.5A< 3.3A> 4.5A< 5.1H> 5.5A< FBCD<60> FBCD<61> DAC_B_YOUT 8.2E> 16.2H> 9.5C< 13.4G< 14.1G< 16.2D> DDC_VCC FBADQM<2> 3.3A> 4.5A< 5.1H> 5.5A< FBCD<62> 3.1E <> 6.2A <> 7.1H > 7.2A <> FBADOM<3> 3.3A> 4.5A< 5.1H> 5.5A< FBCD<63> 3.1E⇔ 6.2A⇔ 7.1H> 7.2A⇔ FBADQM<4>
FBADQM<5> 3.3A> 4.5A< 5.1H> 5.5A< 3.3A> 4.5A< 5.1H> 5.5A< FBCDQM<0>
FBCDQM<7..0> 3.3E> 6.5A< 7.1H> 7.5A< 3.3E> 6.5A< 7.1H> 7.5A< DR_HI FBADQM<6> 3.3E> 6.5A< 7.1H> 7.5A< DR_LO 14.16<> 3.3A> 4.5A< 5.1H> 5.5A< FBCDQM<1> DV0D<11...0> 11.1F< 12.16> 12.1H> FRADOM<7> 3.3A> 4.5A< 5.1H> 5.5A< FBCDOM<2> 3.3F> 6.5A< 7.1H> 7.5A< 3.3E> 6.5A< 7.1H> 7.5A< 3.3E> 6.5A< 7.1H> 7.5A< 3.3E> 6.5A< 7.1H> 7.5A< 3.3E> 6.5A< 7.1H> 7.5A< FBADQS<0> FBADQS<7. DV0D<8> 11.1F< 12.1G> 12.1H> FBADQS<1> 3.3A<> 4.5A< 5.1H> 5.5A< FBCDQM<5> 3.3E> 6.5A< 7.1H> 7.5A< DV0D<9> 11.1F< 12.1G> 12.1H> FBADQS<2> 3.3A<> 4.5A< 5.1H> 5.5A< FBCDQM<6> DVOHSYNO 11.2E< 11.4D<> 12.1G> 12.2H> FRADOS<32 3.3A<> 4.5A< 5.1H> 5.5A< FBCDOM<7> 3.3F> 6.5A< 7.1H> 7.5A< 11.2F< 12.1G> 12.2H> 12.4F> 15.3F< 13.1G<> 15.3G< 3.3A<> 4.5A< 5.1H> 5.5A< 3.3E<> 6.5A< 7.1H> 7.5A< FAN_RETURN FBADQS<6> FBCDQS<1> 9.4B< 16.2H> FBADQS<7> 3.3A<> 4.5A< 5.1H> 5.5A< FBCDQS<2> 3.3E<> 6.5A< 7.1H> 7.5A< FRAA<0> 3.4A> 4.2B< 5.1H> 5.2B< FBARAS* 3.5B> 4.2B< 4.2E< 5.1H> 5.2B< 5.2E< FBCDOS<3> 3.3F<> 6.5A< 7.1H> 7.5A< FBCDQS<4>
FBCDQS<5> FBAWE* FBAA<2> 3.4A> 4.2B< 5.1H> 5.2B< FBCDQS<6> 3.3E<> 6.5A< 7.1H> 7.5A< FBAA<3> 3.4A> 4.2B< 5.1H> 5.2B< FBCA<0> 3.4E> 6.1A< 7.1B< 7.1H> FBCDOS<7> 3.3E<> 6.5A< 7.1H> 7.5A< 3.4A> 4.2B< 5.1H> 5.2B< 3.4A> 4.2B< 5.1H> 5.2B< 3.4A> 4.2B< 5.1H> 5.2B< 3.4A> 4.2B< 5.1H> 5.2B< FBCA<12. FBCA<1> FBCA<2> 3.4E> 6.1A< 7.1B< 7.1H> 3.4E> 6.1A< 7.1B< 7.1H> 3.4E> 6.1A< 7.1B< 7.1H> 3.4E> 6.1A< 7.1B< 7.1H> FBCRAS* 3.5E> 6.2B< 6.2E< 7.1H> 7.2B< 7.2E< FBCWE* 3.5E> 6.2B< 6.2E< 7.1H> 7.2B< 7.2E< FBAA<6> FBAA<7> 3.4A> 4.2B< 5.1H> 5.2B< FBCA<3> 3.4E> 6.1A< 7.1B< 7.1H> FBCA<4> FBCA<5> FBCA<6> FRAA<R> 3 4A> 4 2B< 5 1H> 5 2B< 3 AF> 6 1A< 7 1B< 7 1H FBVREF 3.5B> 16.3D> 3.4A> 4.2B< 5.1H> 5.2B< 3.4A> 4.2B< 5.1H> 5.2B< 3.4E> 6.1A< 7.1B< 7.1H> 3.4E> 6.1A< 7.1B< 7.1H> 9.3B< 16.2H> 9.3B< 16.2H> FBAA<10 I2C_A_SCL FBAA<11> 3.4A> 4.2B< 5.1H> 5.2B< FBCA<7> 3.4E> 6.1A< 7.1B< 7.1H> 8.1D> 9.1A< 8.1D> 9.1A< FBAA<12> 3.4A> 4.2B< 5.1H> 5.2B< FBCA<8> 3.4E> 6.1A< 7.1B< 7.1H> I2C A SDA I2C_B_SCL I2C_B_SDA FRARA<0: 3.5A> 4.2B< 4.2D< 5.1H> 5.2B< 5.2D< FBCA<9> FBCA<10 3.4E> 6.1A< 7.1B< 7.1H> 8 2N> 9 1F< 3.4E> 6.1A< 7.1B< 7.1H> 3.4E> 6.1A< 7.1B< 7.1H> 3.5A> 4.2B< 4.2D< 5.1H> 5.2B< 5.2D< FBABA<1..0> FBCA<11> IFPABPLLVDD 13.1G<> FBCA<12> 3.4E> 6.1A< 7.1B< 7.1H> IFPABVREF 13.1G<> FBABA<1> 3.5A> 4.2B< 4.2D< 5.1H> 5.2B< 5.2D< FBCBA<0> 3.5E> 6.2B< 6.2D< 7.1H> 7.2B< 7.2D< 3.5E> 6.2B< 6.2D< 7.1H> 7.2B< 7.2D< IFPCPLLVDD 13.1G<> FBACKE 3.5A> 4.2B< 4.2F< 5.1H> 5.2B< 5.2F< FRCRA<1> 3.5E> 6.2B< 6.2D< 7.1H> 7.2B< 7.2D< TEPCVREE 8 3H> 12 4F< 3.5B> 4.2B< 4.2E< 4.5D< 5.1H> FBCCAS* 3.5E> 6.2B< 6.2E< 7.1H> 7.2B< 7.2E< FBACLKO* 3.5B> 4.2B< 4.2E< 4.5E< 5.1H> M_GREEN FBCCKE 3.5E> 6.2B< 6.2E< 7.1H> 7.2B< 7.2E< FBACLK1 3.5B> 5.1H> 5.2B< 5.2E< 5.5D< M_RED 9.3B< 16.2H> FBACLK1 3.5B> 5.1H> 5.2B< 5.2F< 5.5F< NV34 HOTPLUG 12.4D< 13.5D EBCCI KO 3 5F> 6 2R< 6 2F< 6 5D< 7 1H> FBCCLK1 3.5E> 7.1H> 7.2B< 7.2E< 7.5D< PCICBE<0> NVIDIA CORPORATION FBAD<63..0> 3.1A 4.2A 5.1H 5.2A FBCCLK1* 3.5E> 7.1H> 7.2B< 7.2E< 7.5F< PCICBE<3..0> 2.1H> 3.1A 4.2A 5.1H 5.2A PCICBE<1> 2701 SAN TOMAS EXPRESSWAY ANTA CLARA. CA 95050. USA ONTINUED ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS DATE | SEP 03 200 G

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A	## Part Cross-Reference for the entire design *** ### BRETI BREEKET 10.4C C1	A
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