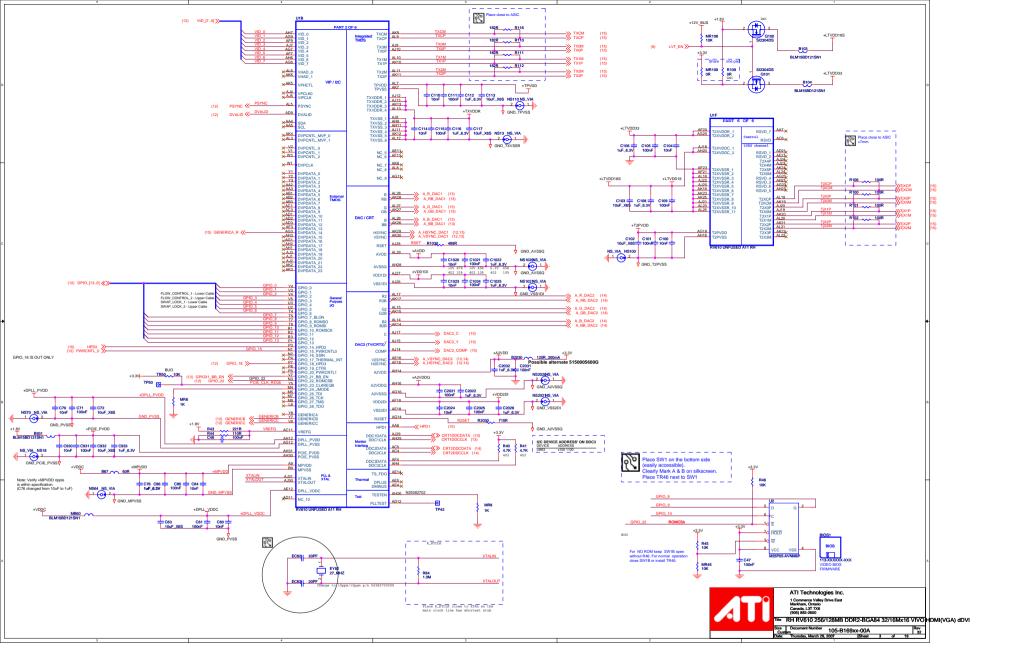
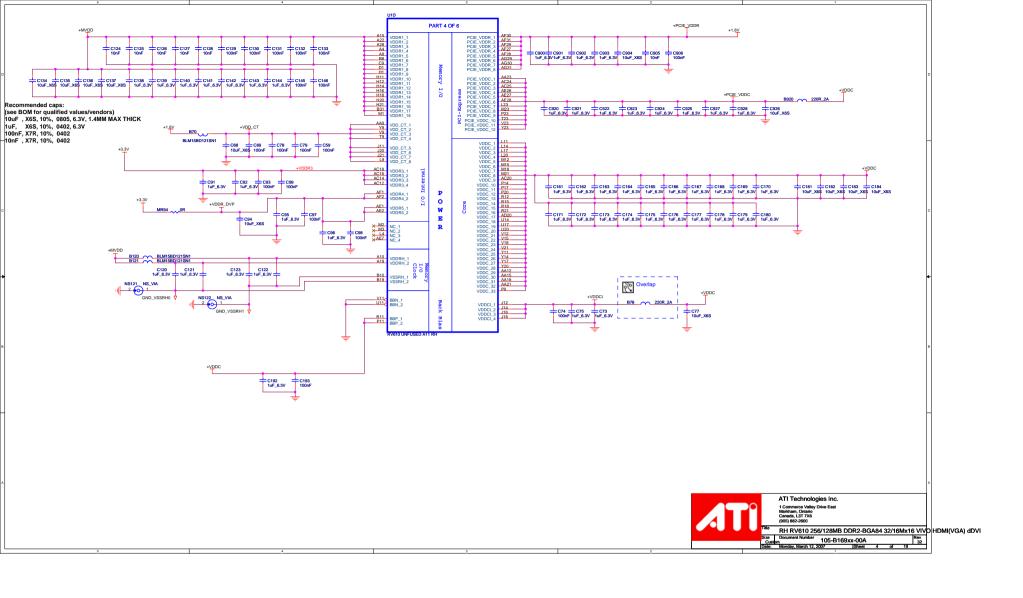
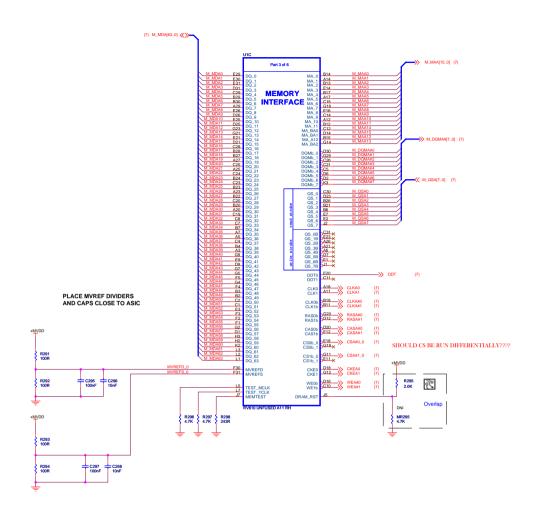


ATT Technologies Inc.

1 Comment Valley Drive East
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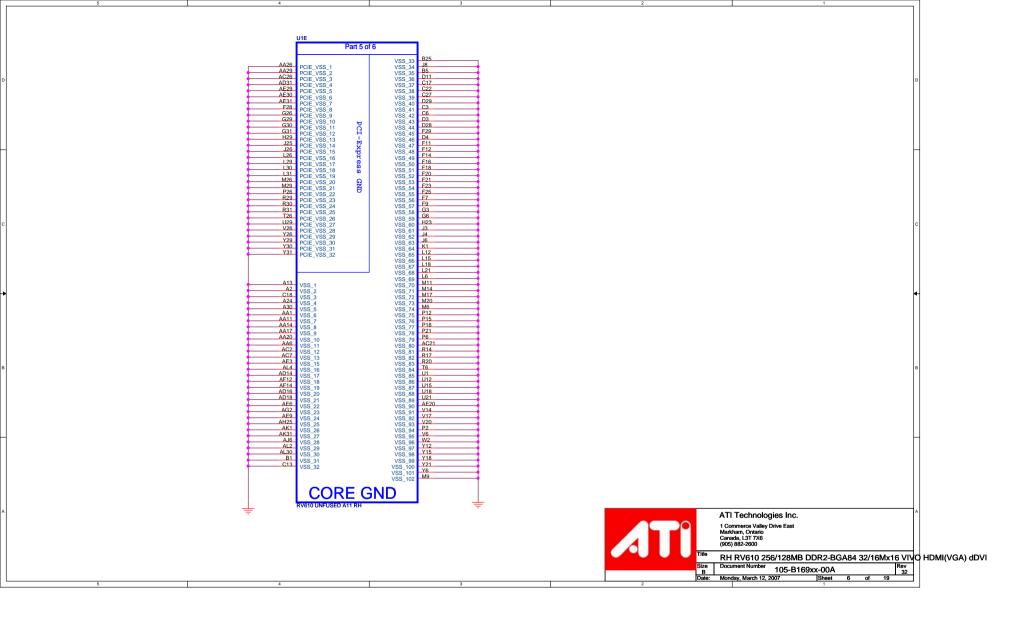


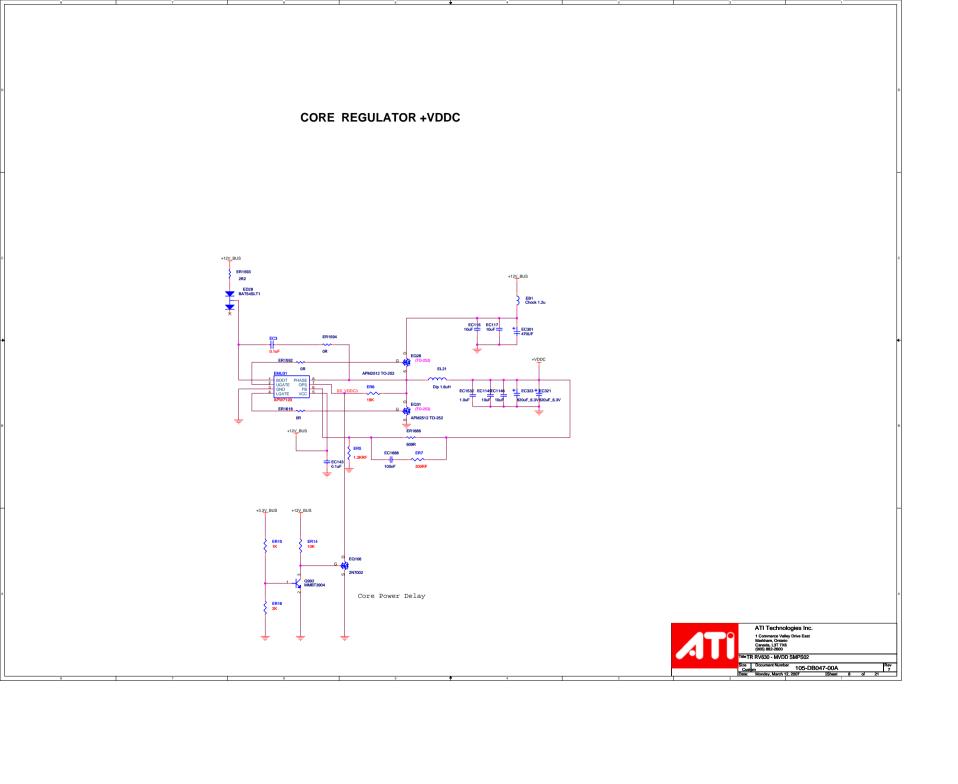


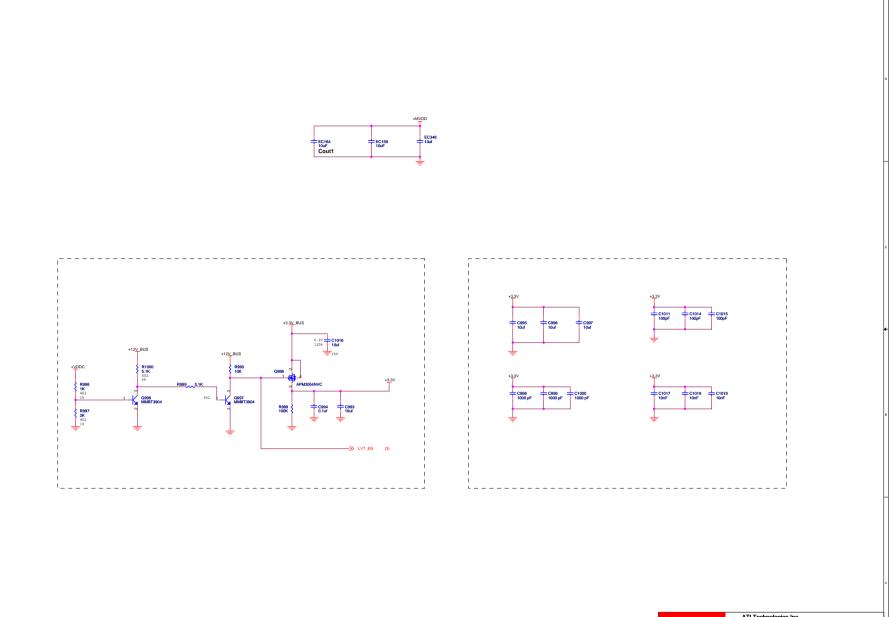


DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

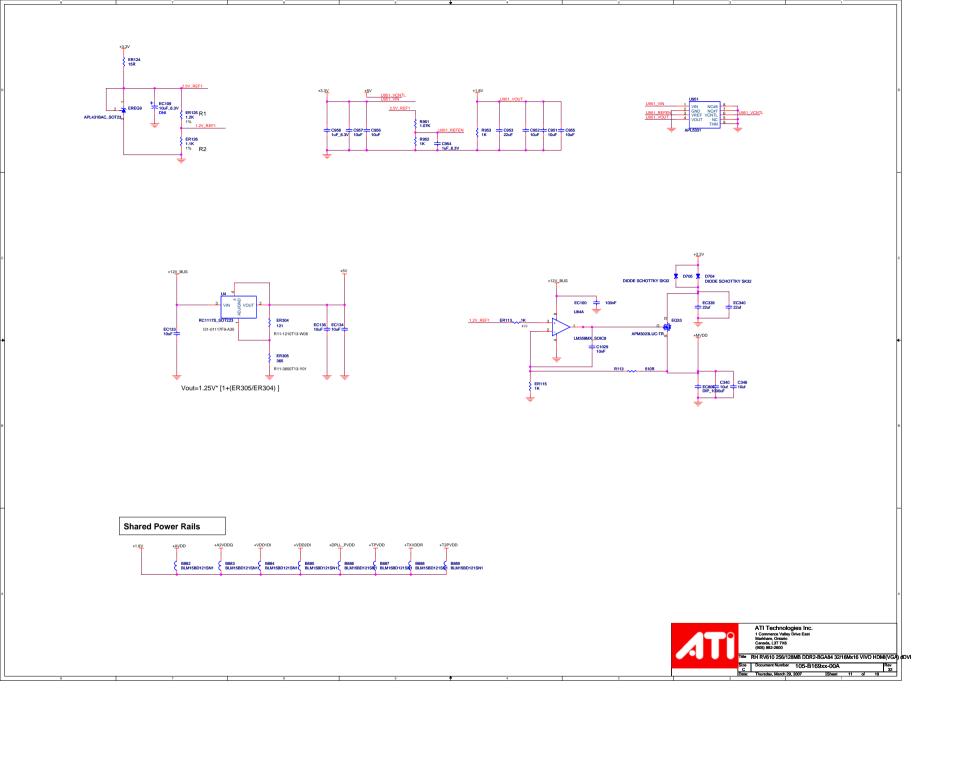


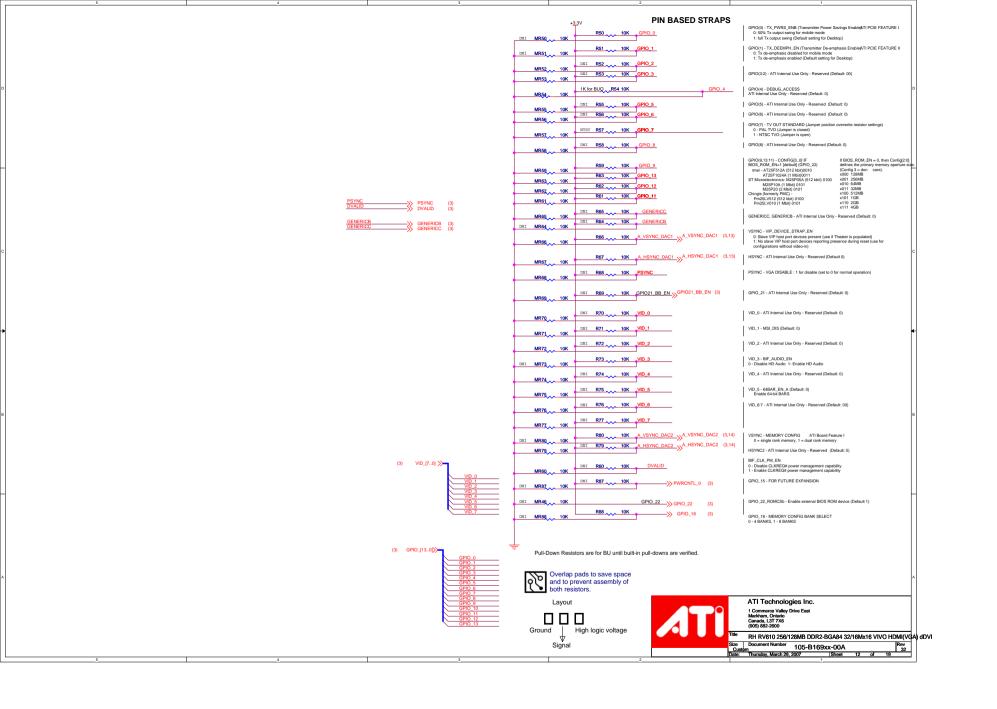


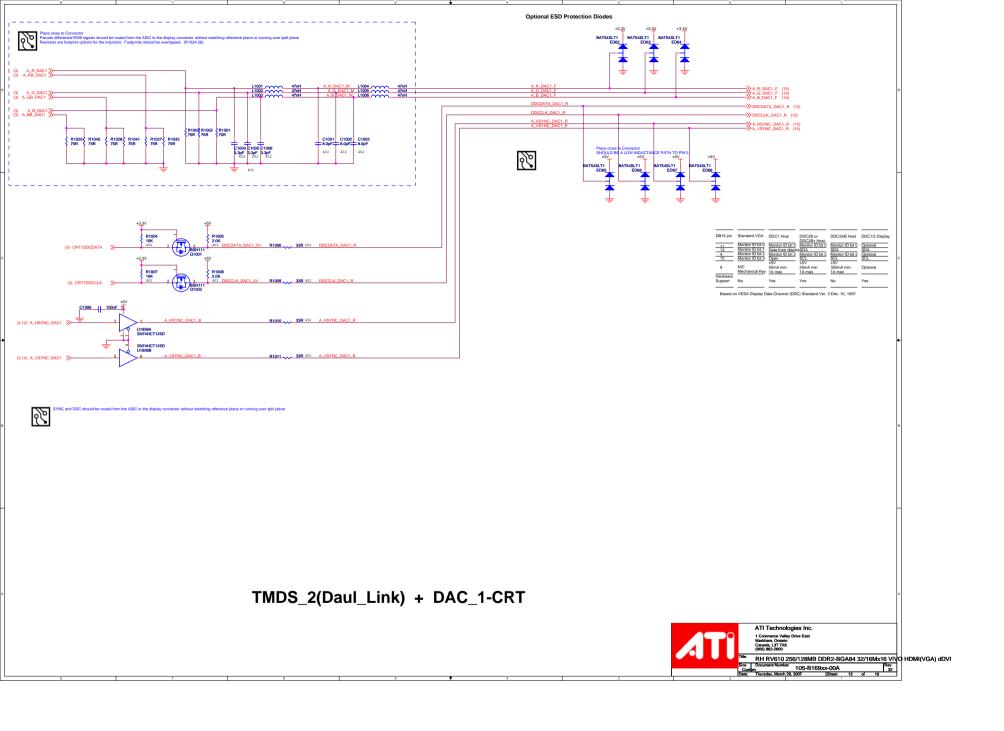


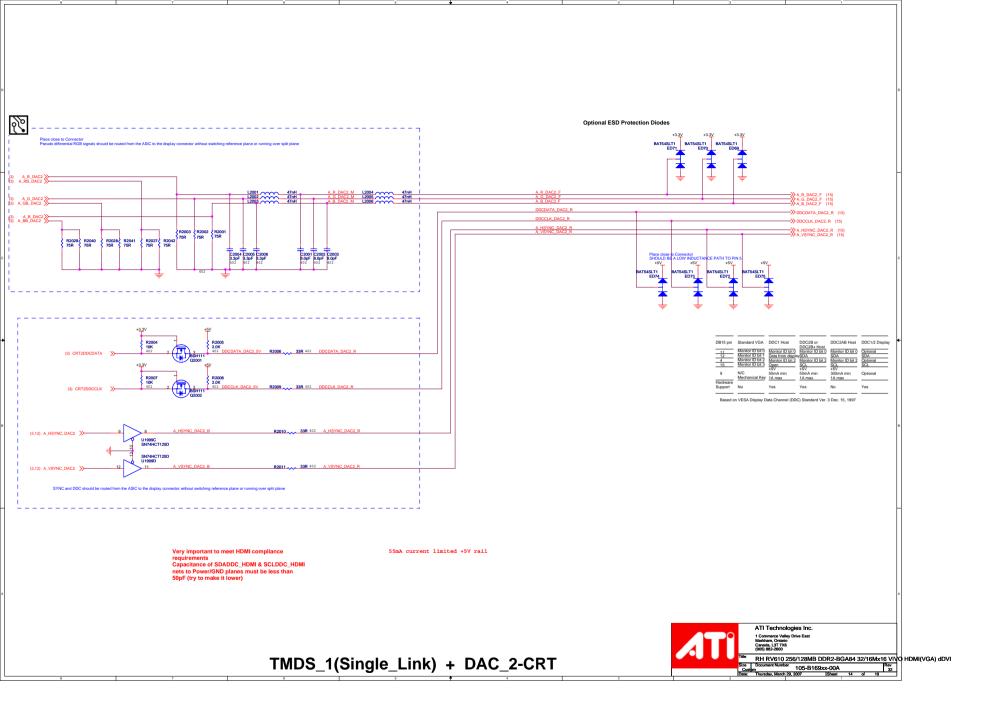


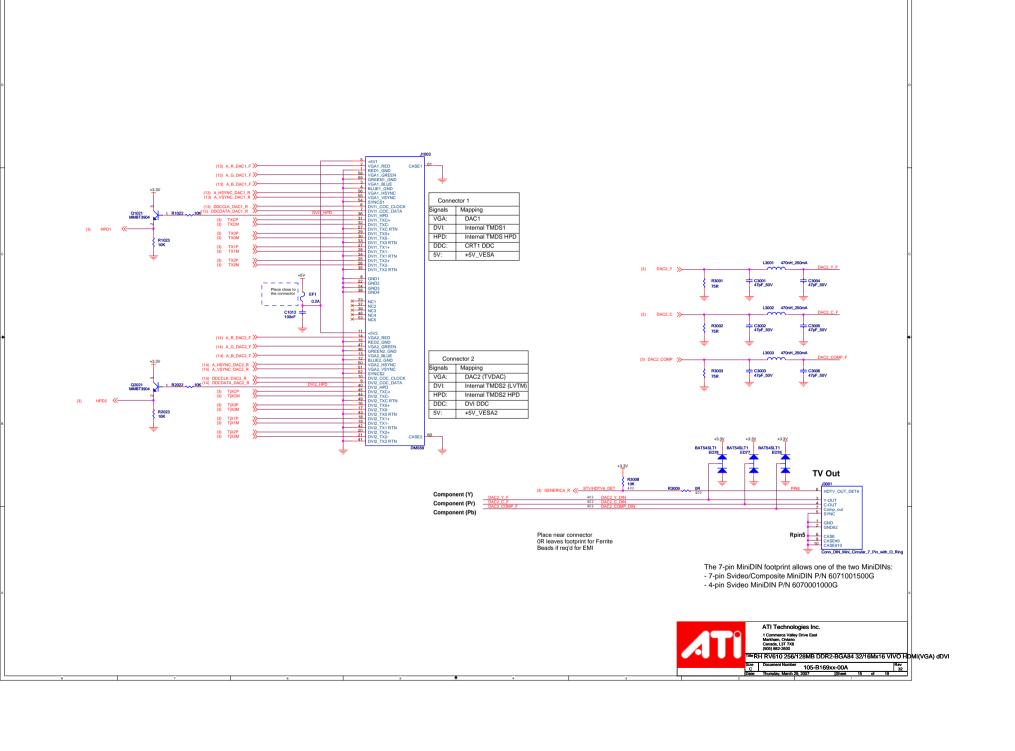


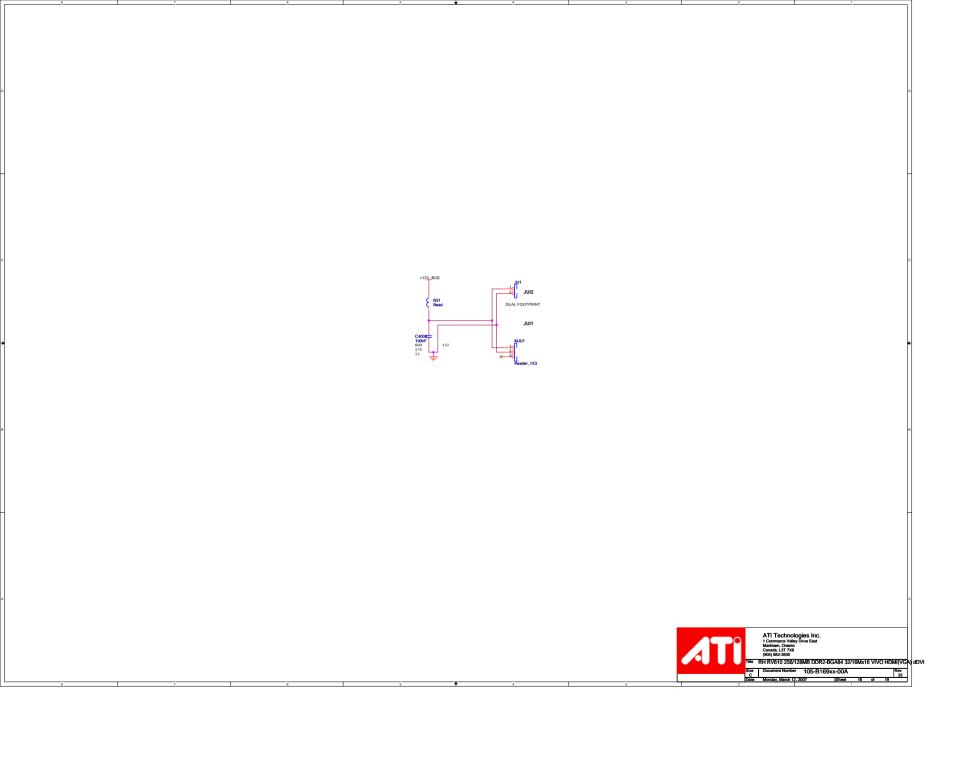


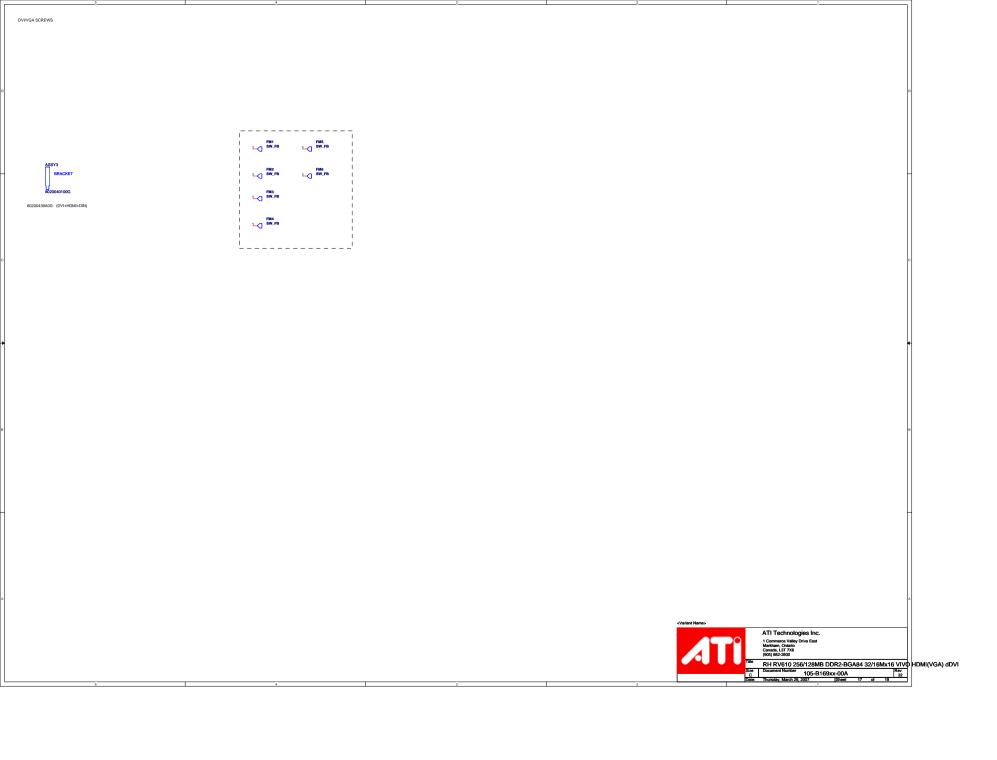














Title

Schematic No. RH RV610 256/128MB DDR2-BGA84 32/16Mx16 VIVO HDM (VG65-457V59xx-00A Date:

Thursday, March 01, 2007

## **REVISION HISTORY**

This schematic represents the PCB, it does not represent any specific SKU.

For Stuffing options (component values, DNI, ? please consult the product specific BOM.

Please contact ATI representative to obtain latest BOM closest to the application desired. NOTE:

Rev

32

	Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
			2006.12.01	UPDATE SCHEM. BOM MANAGEMENT.
			2006.12.14	UPDATE SCHEMATIC TO NETLIST WITH NO ERRORS
			2006.12.18	DORINA UPDATE MEM SWAP
			2006.12.19	REMOVE TP ON MEM - TO BE REPLCED BY 0.8MM PADS ON ALL LINES
С			2006.12.20	CHANGED B67 to PN 5260014800G AND C76 to PN 4172010500G
	0	00A	2006.12.21	J2 REMOVED
•			2007.01.15	NC626 removed (VDDC output cap). LDO output resistor (R879, R880) moved closer to LDO. MVDD LDO input resistors changed to 1R. Debug header changed to include Gen1/2 switch. HDMI caps removed. Added thermal shutdown option to power sequencing.
			2007.01.16	REMOVE BACK BIAS, REMOVE MC624
			2007.01.17	REMOVE R5515, R5516, R5521, R5524 REMOVE R94
В			2007.01.22	ADDED H3, H4, H5
			2007.01.22	DECAP CHANGES ON PAGE 3
			2007.01.23	HEATSINK GROUNDING ADJUSTED
_			2007.01.23	DORINA - HEATSINK GNDING PINS ADJUSTED
			2007.01.24	RM JTAG + SMA CLOCK CONNECTIONS TO EASE LAYOUT CONGESTION
			2007.01.24	ADDED C300, C301, C302 (STITCHING CAPS) TO IMPROVE DDC LINES
Α_			2007.01.24	FIXED ORCAD NETLIST PROBLEM; NO EFFECTIVE CHANGE.
			2007.01.24	ADD Q102 TO SOLVE A11 VDDR3 LEAKAGE PROBLEM.
	1	00B	2007.01.25	CHNG REF DES OF VDDR3 LEAKAGE BLOCK TO Q/R-90
	2	00C	2007.02.09	PCB mechanical updates only. No Schematic changes.
			5	4 3 2 1

