PG161-A00

TU106 6GB GDDR6, 192b, X16

DVI-D/DP + DP + HDMI

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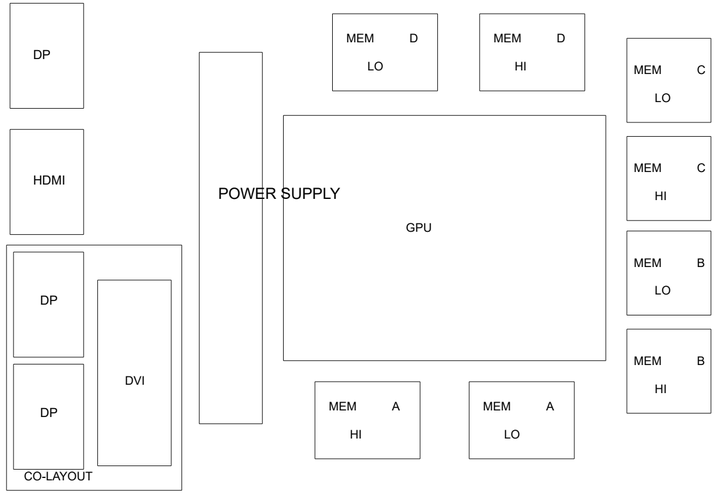
Page2: Block Diagram



Power Supply:

- Power Supply NVVDD-PH5
- Power Supply NVVDD-PH4
- Power Supply NVVDD-PH3
- Power Supply NVVDD-PH2
- Power Supply NVVDD-PH1
- Power Supply FBVDDQ-PH2
- Power Supply FBVDDQ-PH1
- Power Supply 5V
- PEX_VDD
- 1V8
- Fan
- DP_PWR

EXT_12V 2x4 PWR

PEX_12V Finger

3V3 Finger

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Engineer: James_Huang
OrgName
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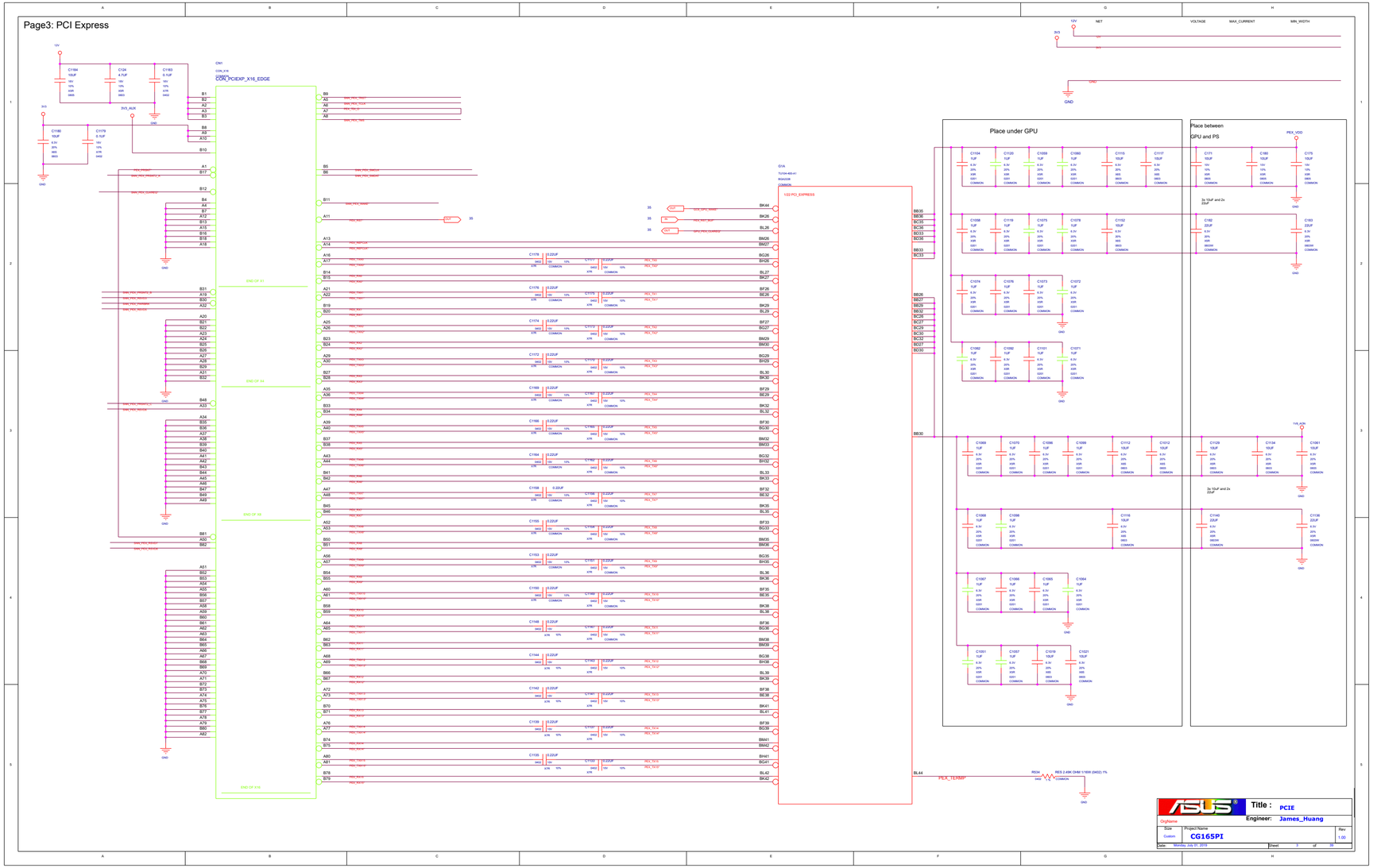
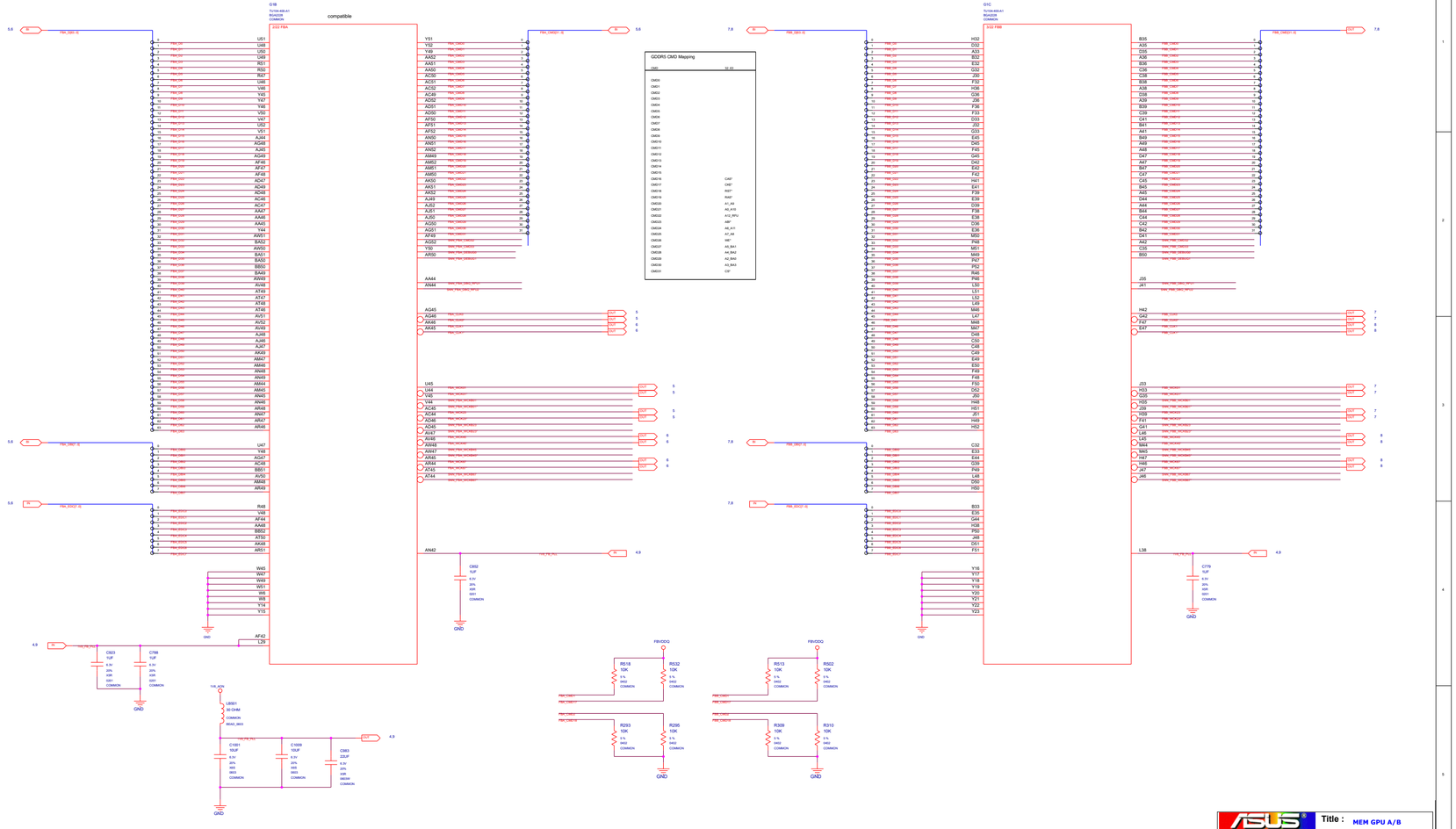
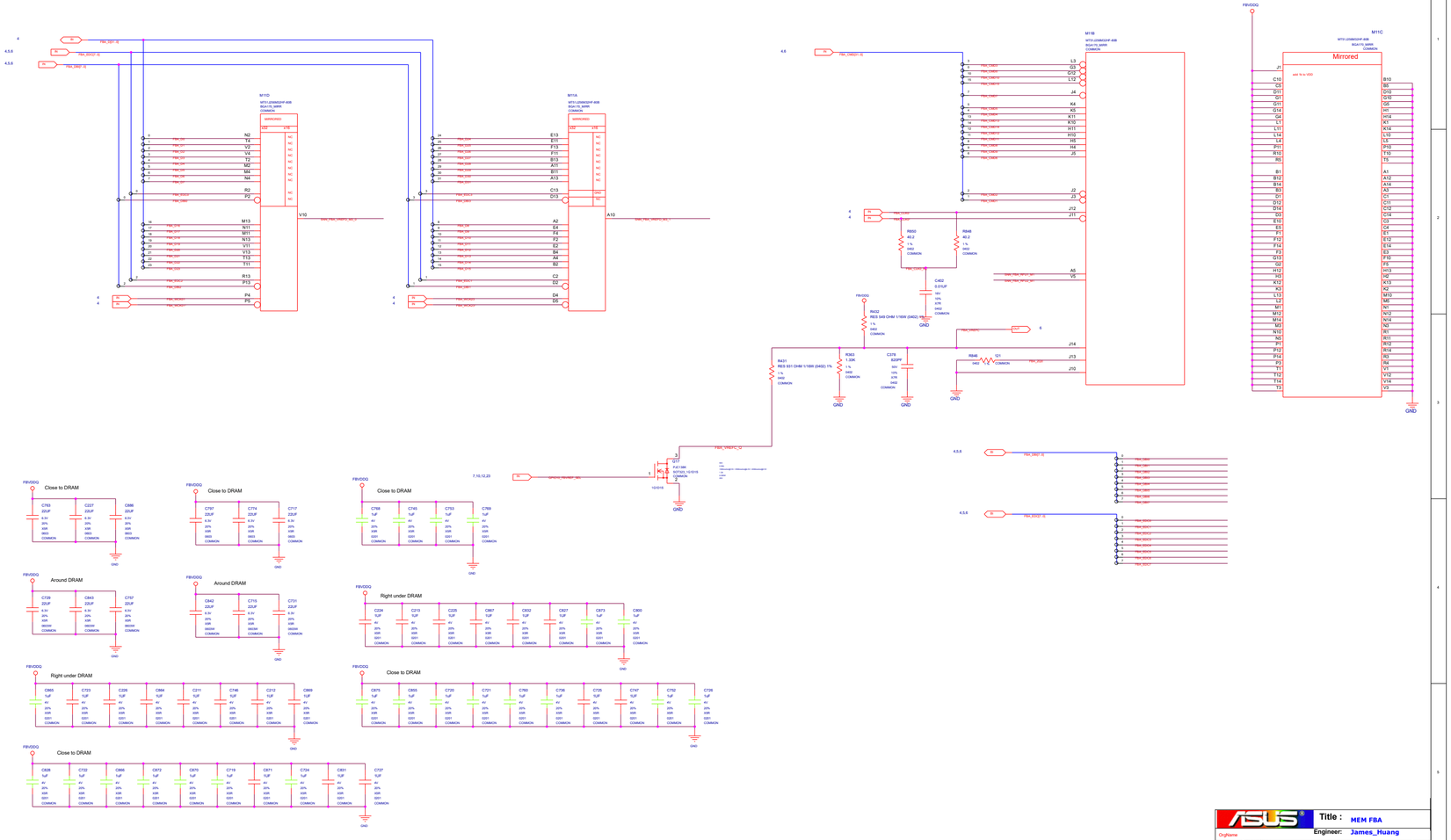
Page3: PCI Express



Page4: MEMORY: GPU Partition A/B



Page5: MEMORY: FBA Partition 31..0



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Orgname	Engineer:	James_Huang	
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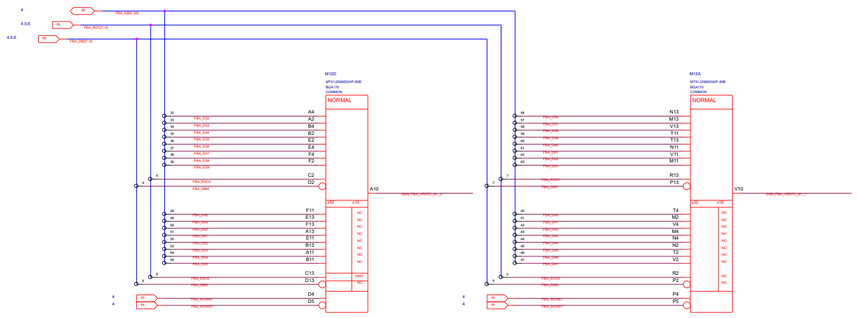
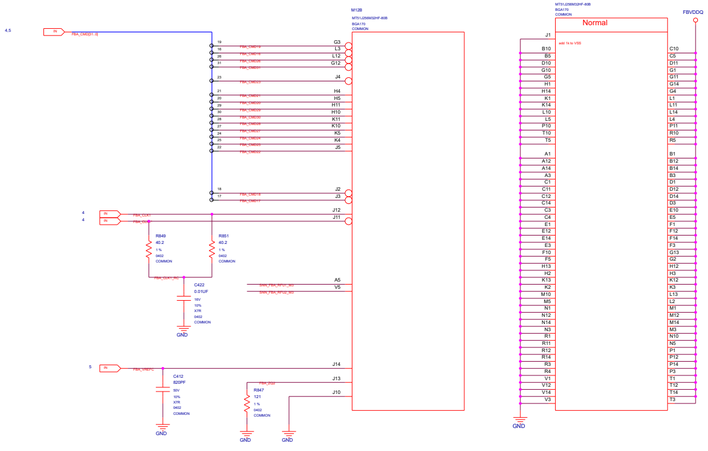
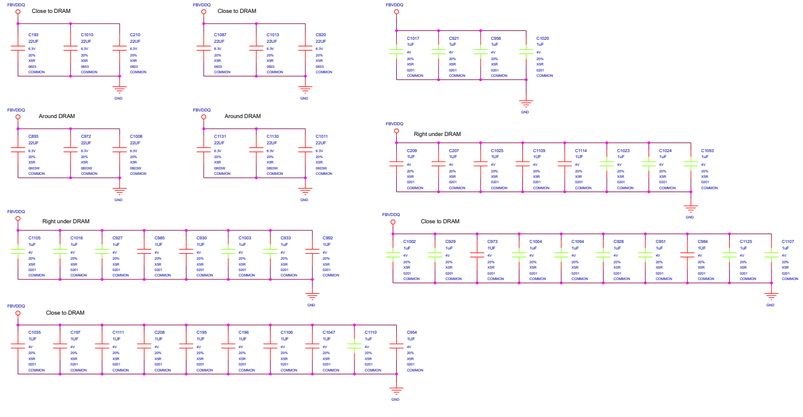
Page6: MEMORY: FBA Partition 63..32







Title : MEM FBA 2

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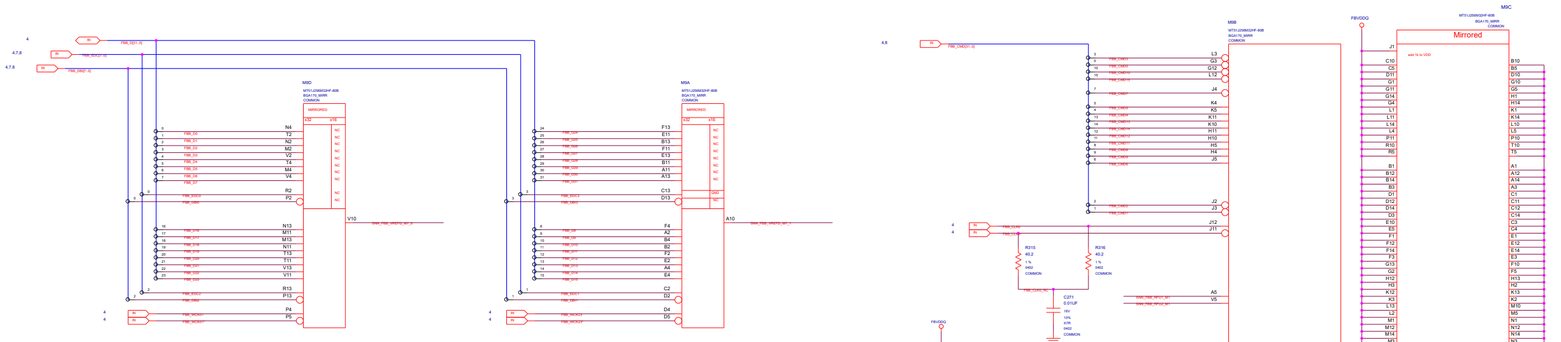

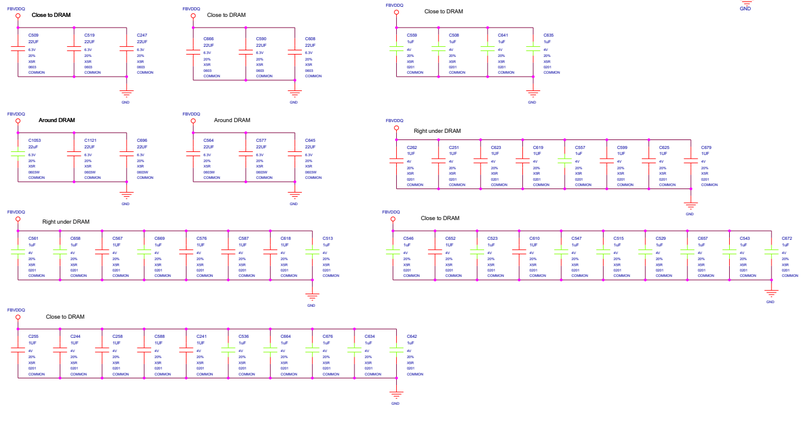

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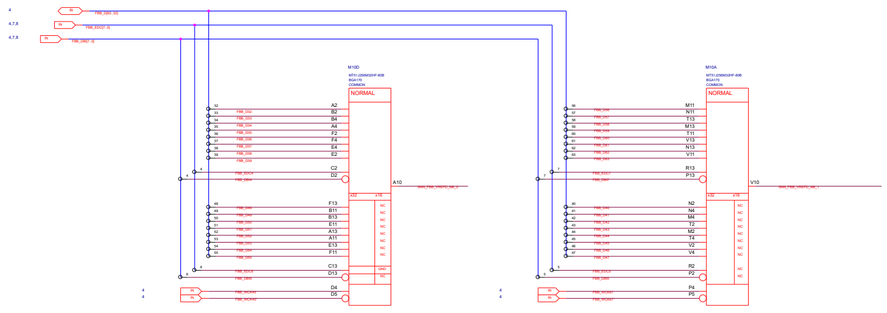

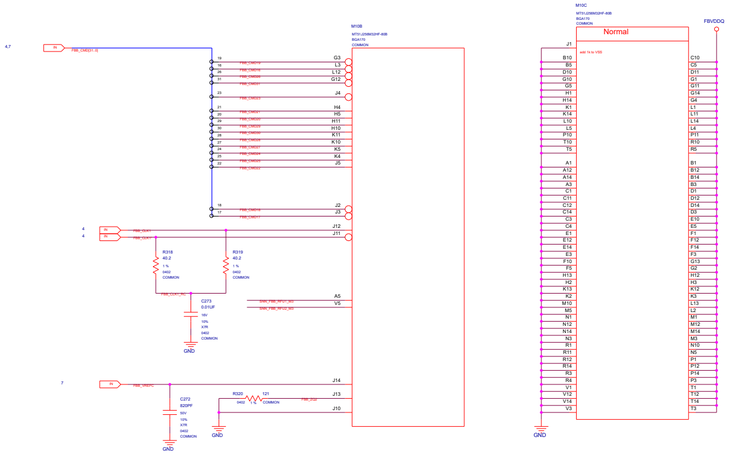

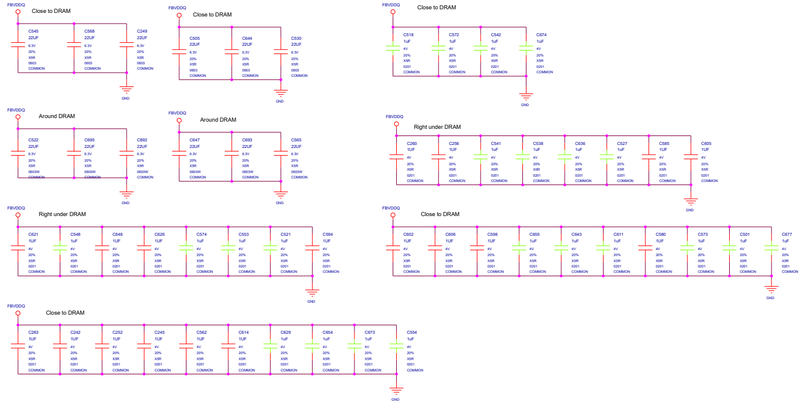

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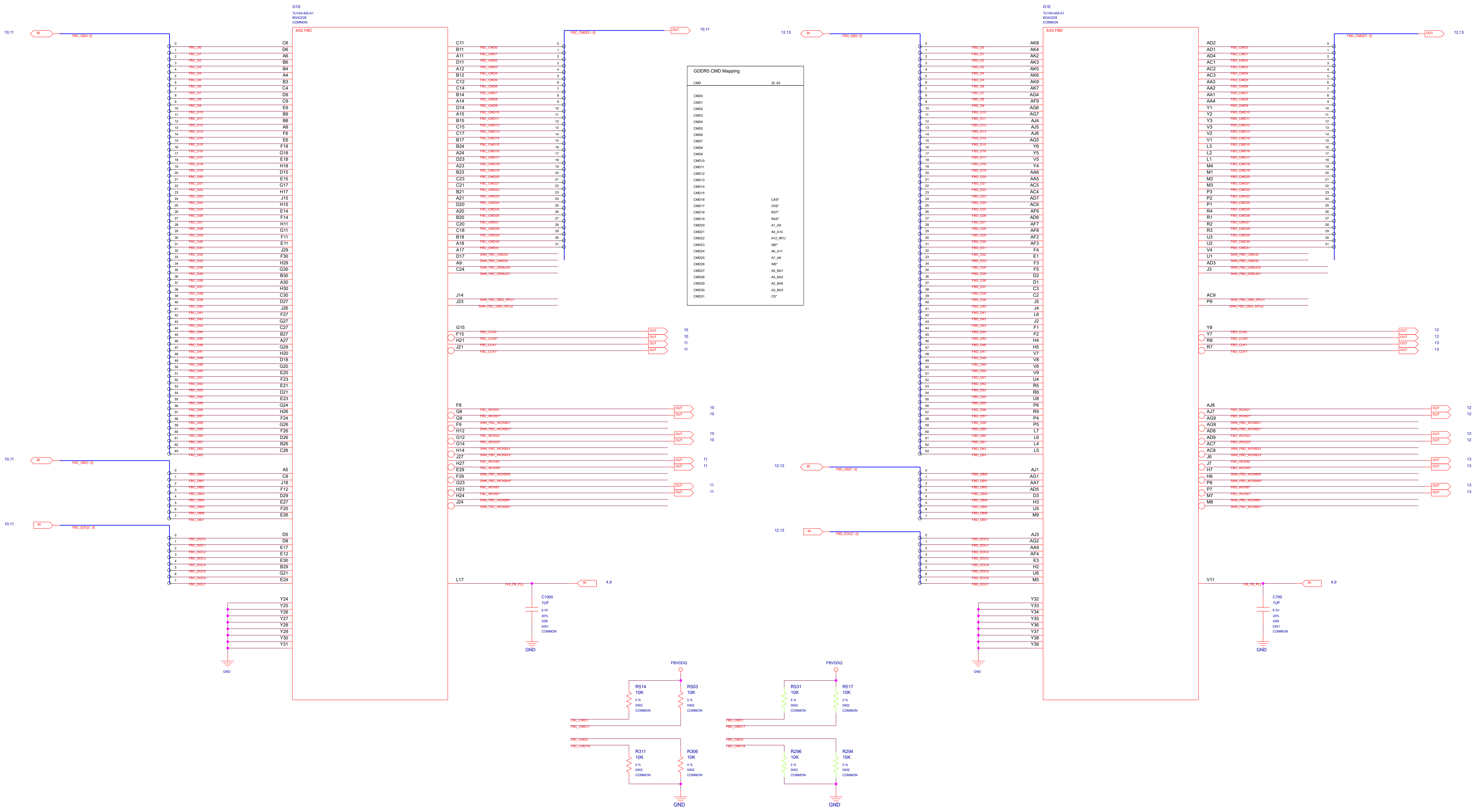
Page10: MEMORY: GPU Partition C/D



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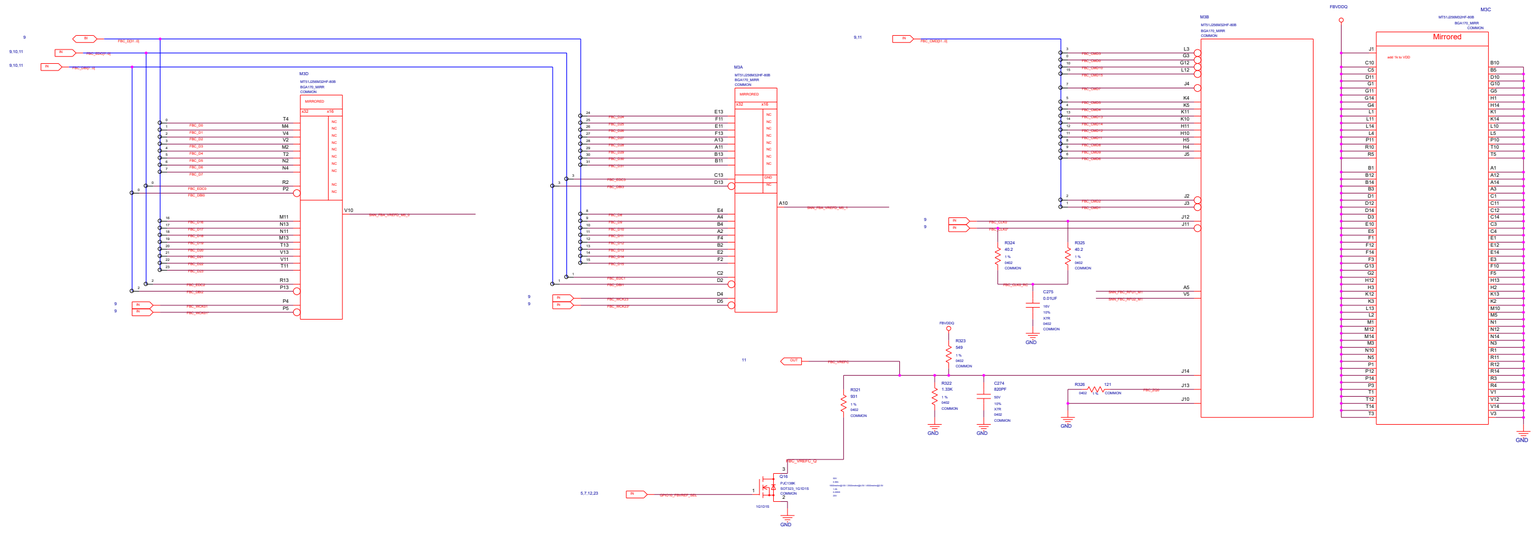
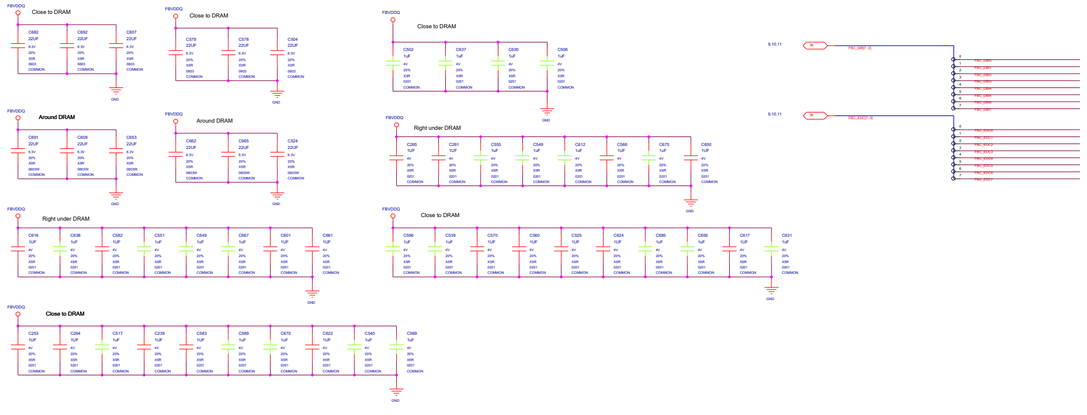
Page10: MEMORY: FBC Partition 31..0





Title :	MEM FBC
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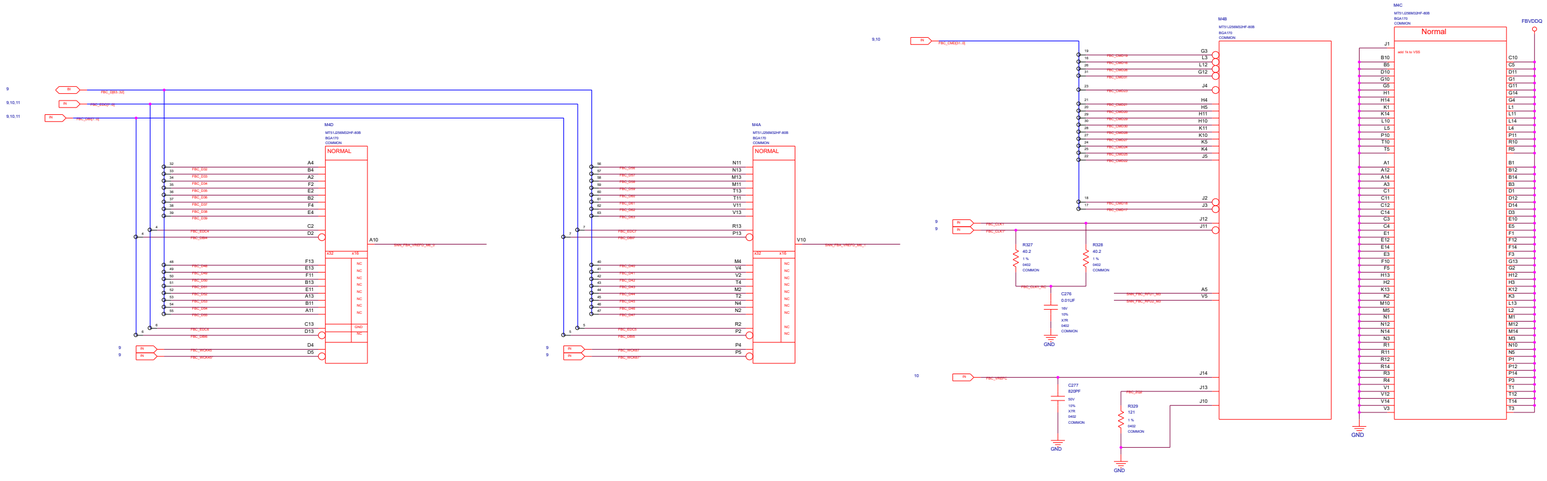

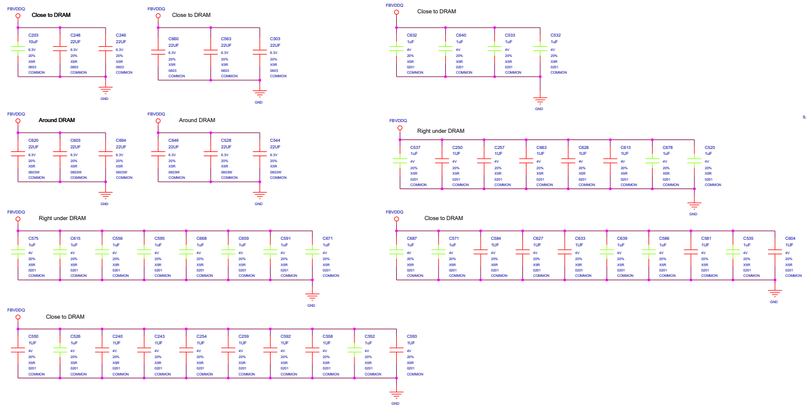

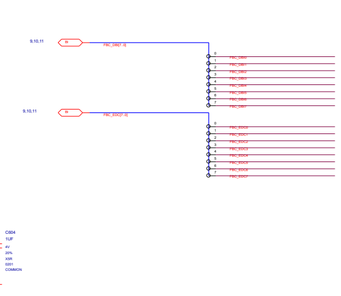

ASUSTeK	Title : MEM FBC2		
	Engineer: James_Huang		
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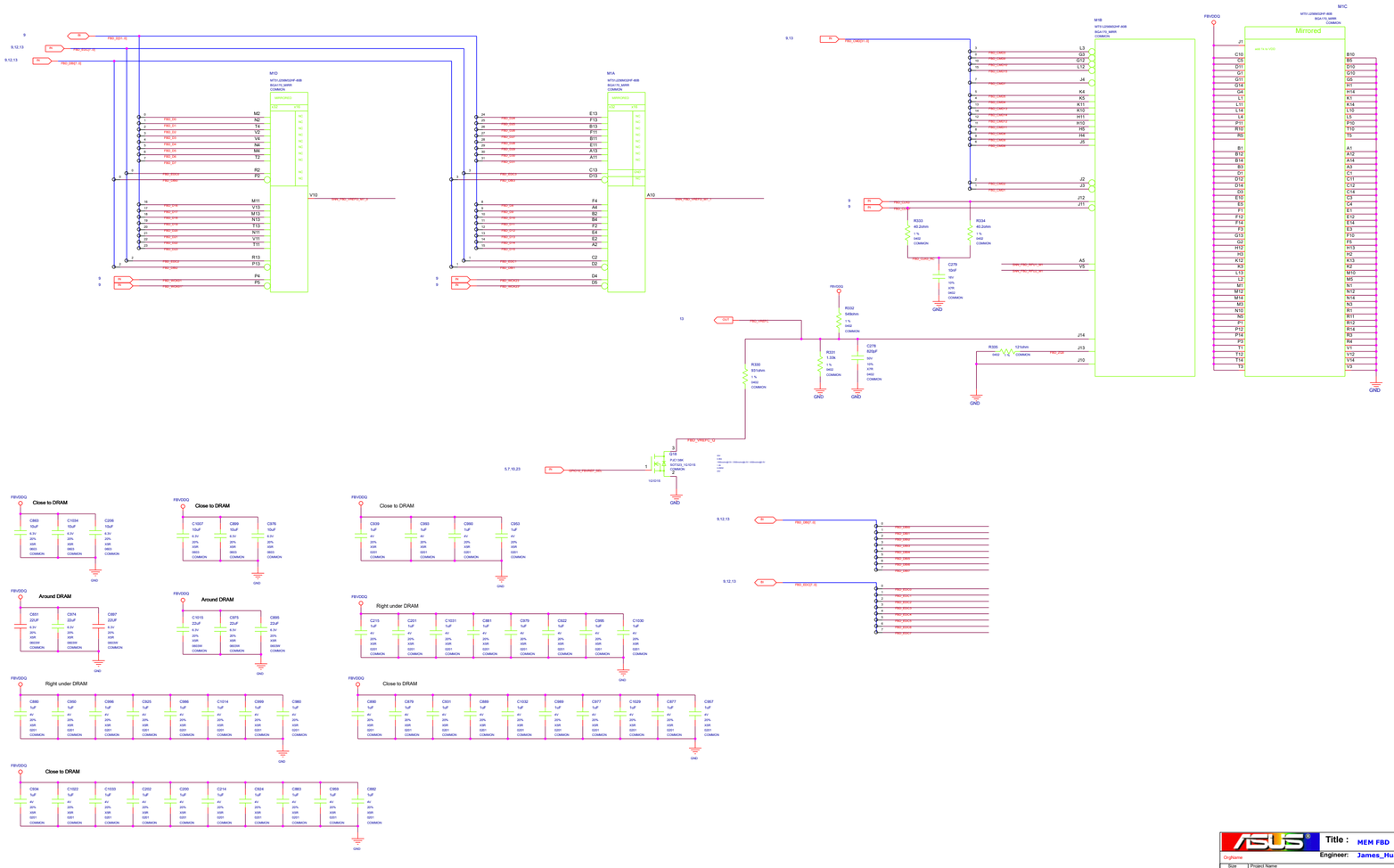
Page12: MEMORY: FBD Partition 31..0



ASUS	Title :	MEM FBD	
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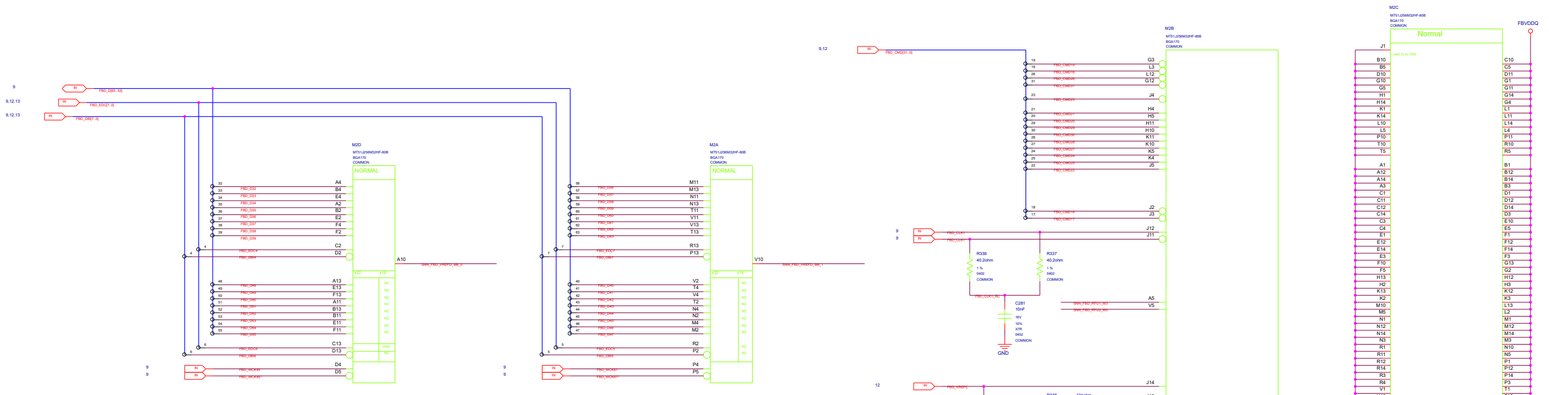

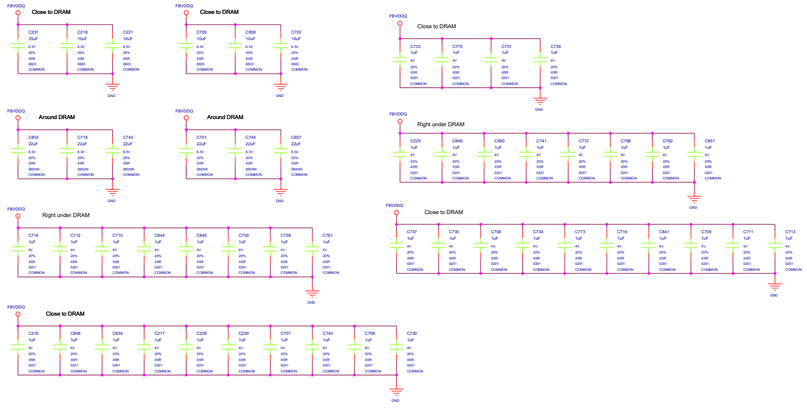

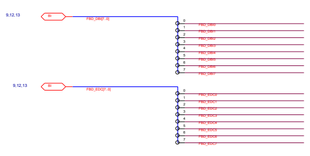

ASUS	Title :	MEM FBD	
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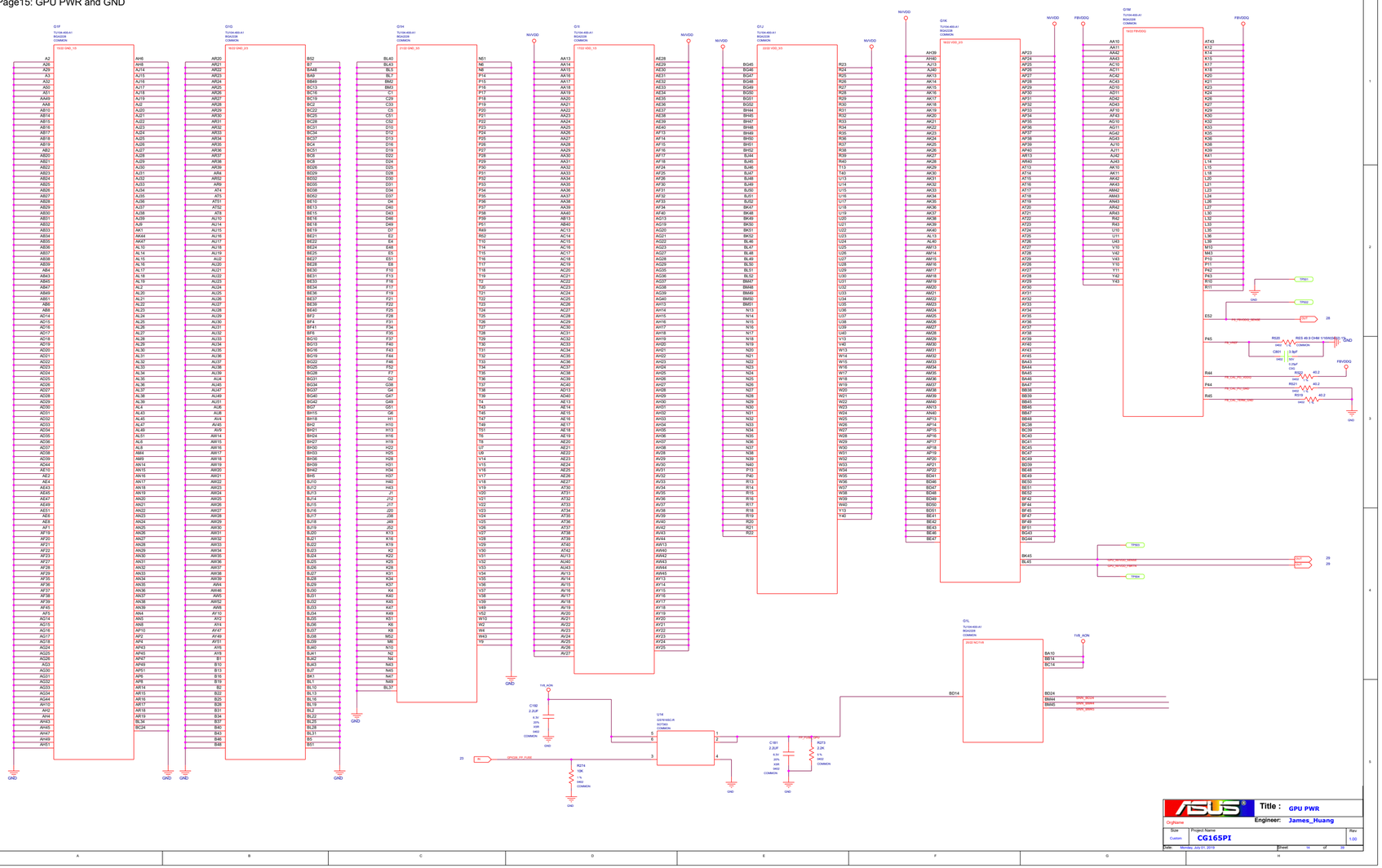
Page15: GPU PWR and GND



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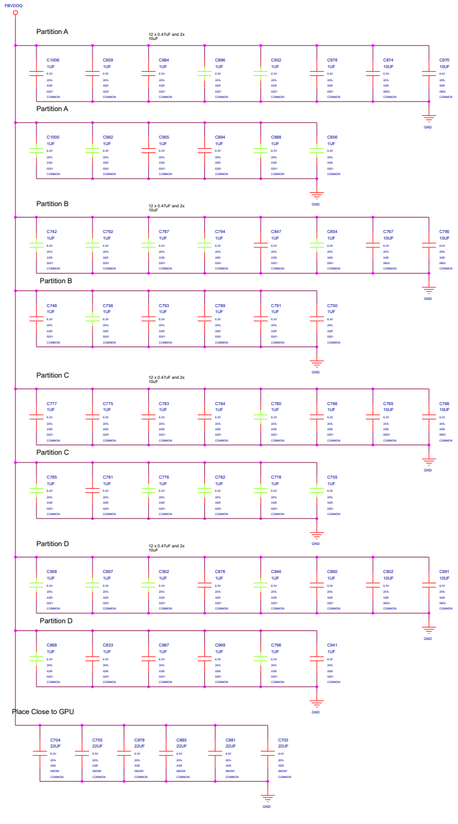
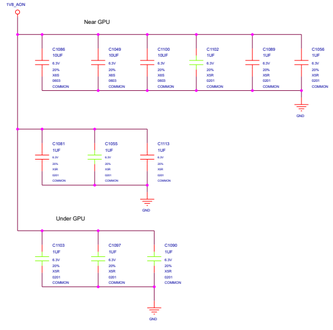
Page15: GPU Decoupling 1

FBVDDQ



NVVDD

1V8_AON



Title : GPU Decoupling			
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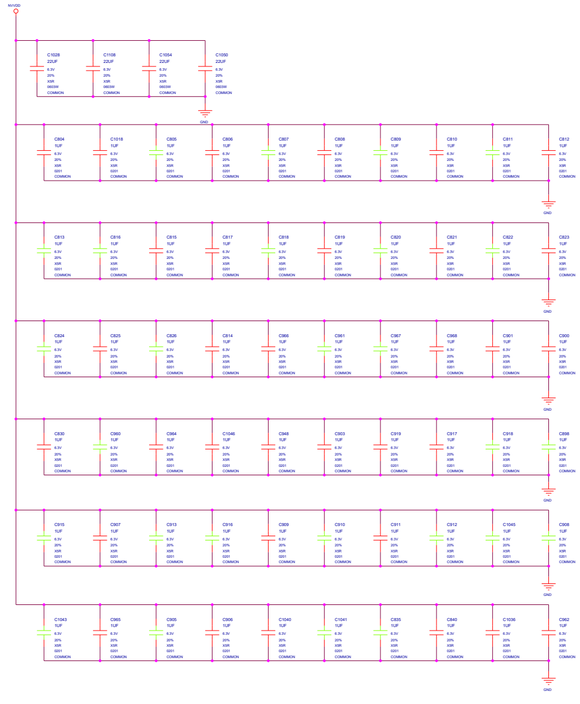
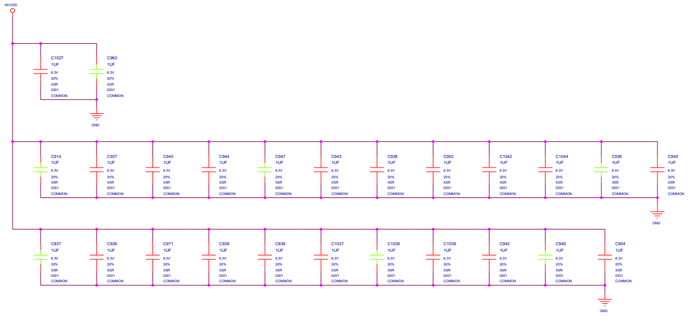
Page16: GPU Decoupling 2

NVVDD





Title : GPU Decoupling2			
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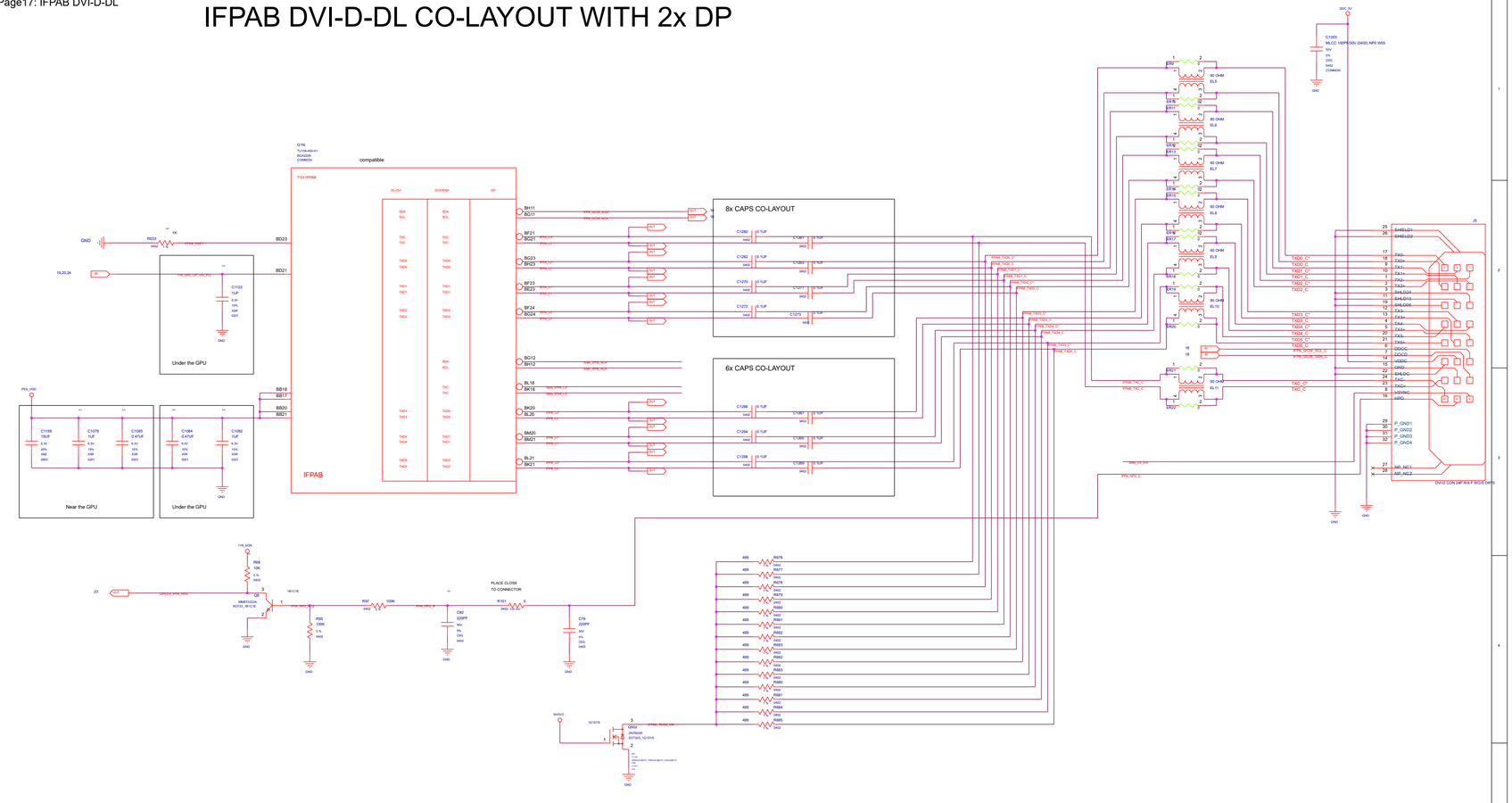
Page17: IFPAB DVI-D-DL

IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



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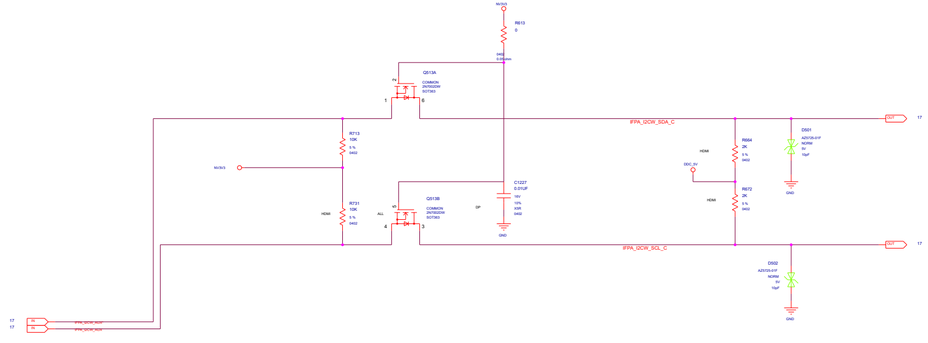
Page18: IFPA DP



IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

Title :	IO IFPA DP		
Orgname	Engineer:	James_Huang	
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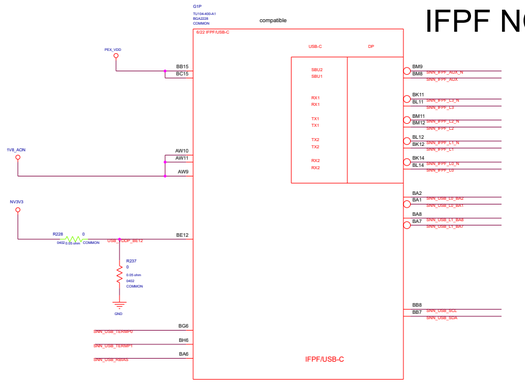
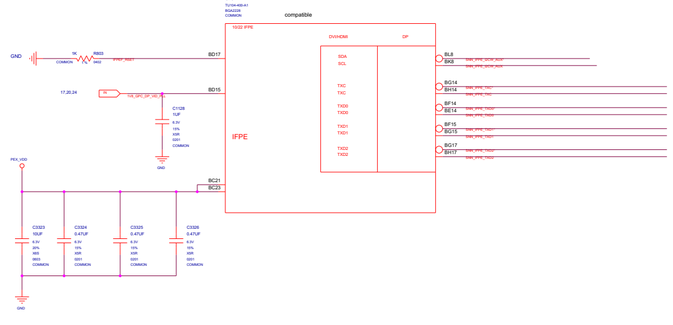
Page20: IFPE IFPF USB-C NC

IFPF NC





Title :	IFPE NC		
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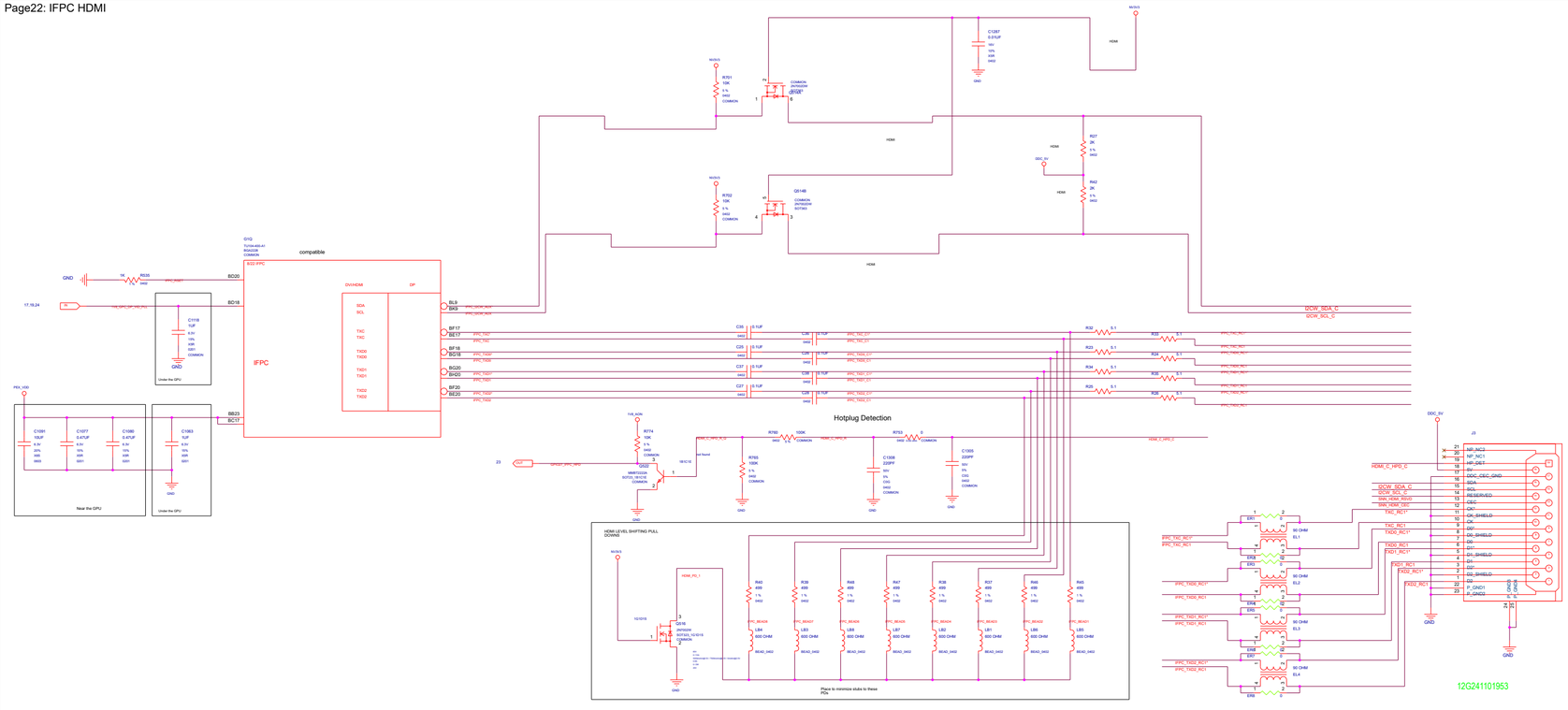
Page22: IFPC HDMI



Title :	IFPC HDMI		
Engineer:	James_Huang		
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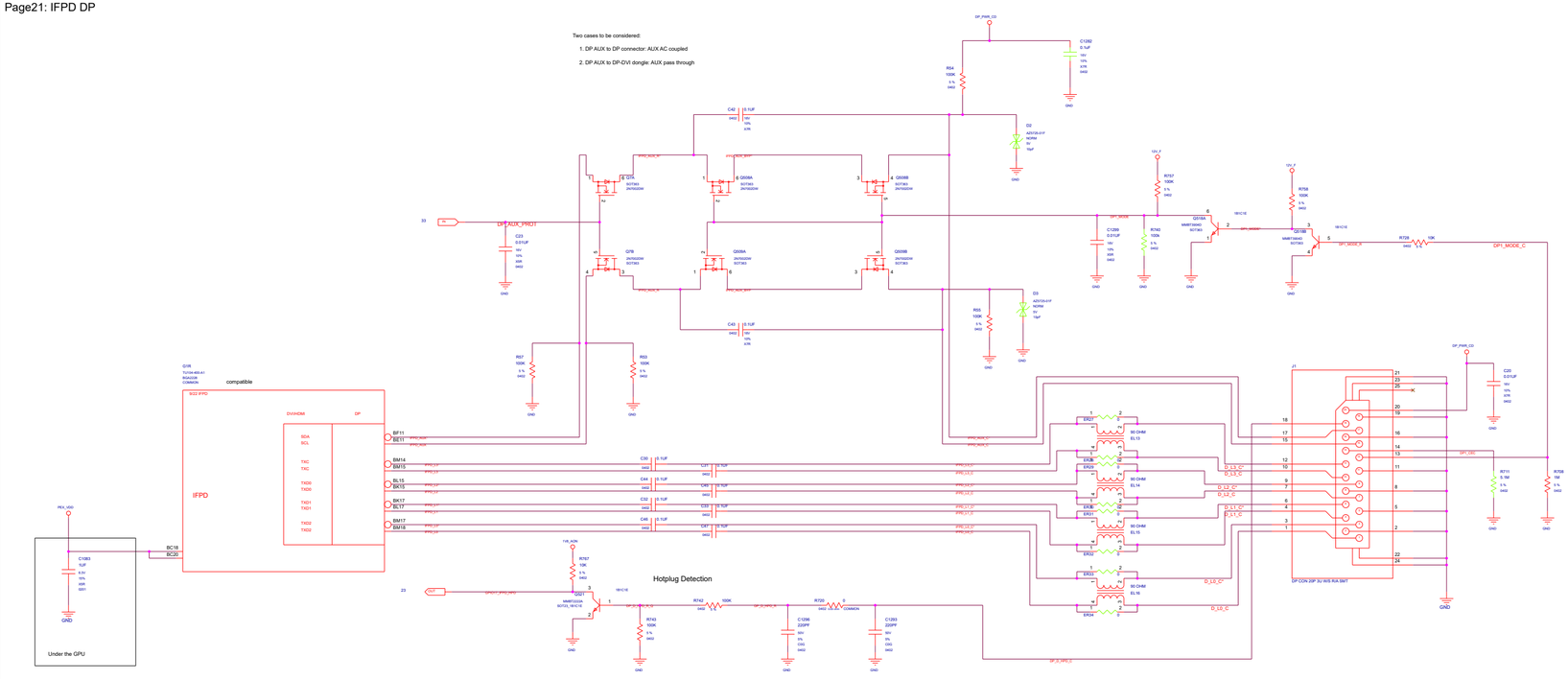
Page21: IFPD DP

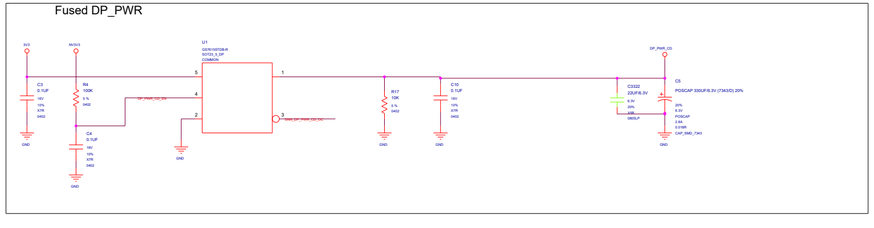
Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled

2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR



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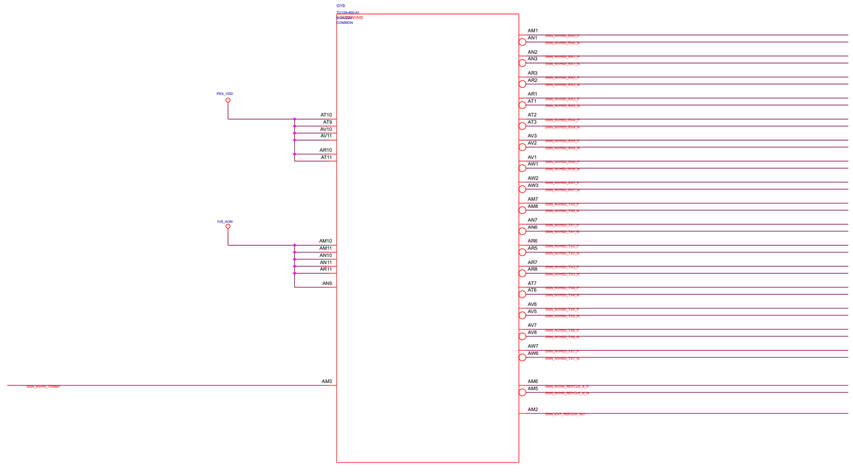
Page22: NVHS Interface and Frame Lock



Title :	NVHS Interface		
Engineer:	James_Huang		
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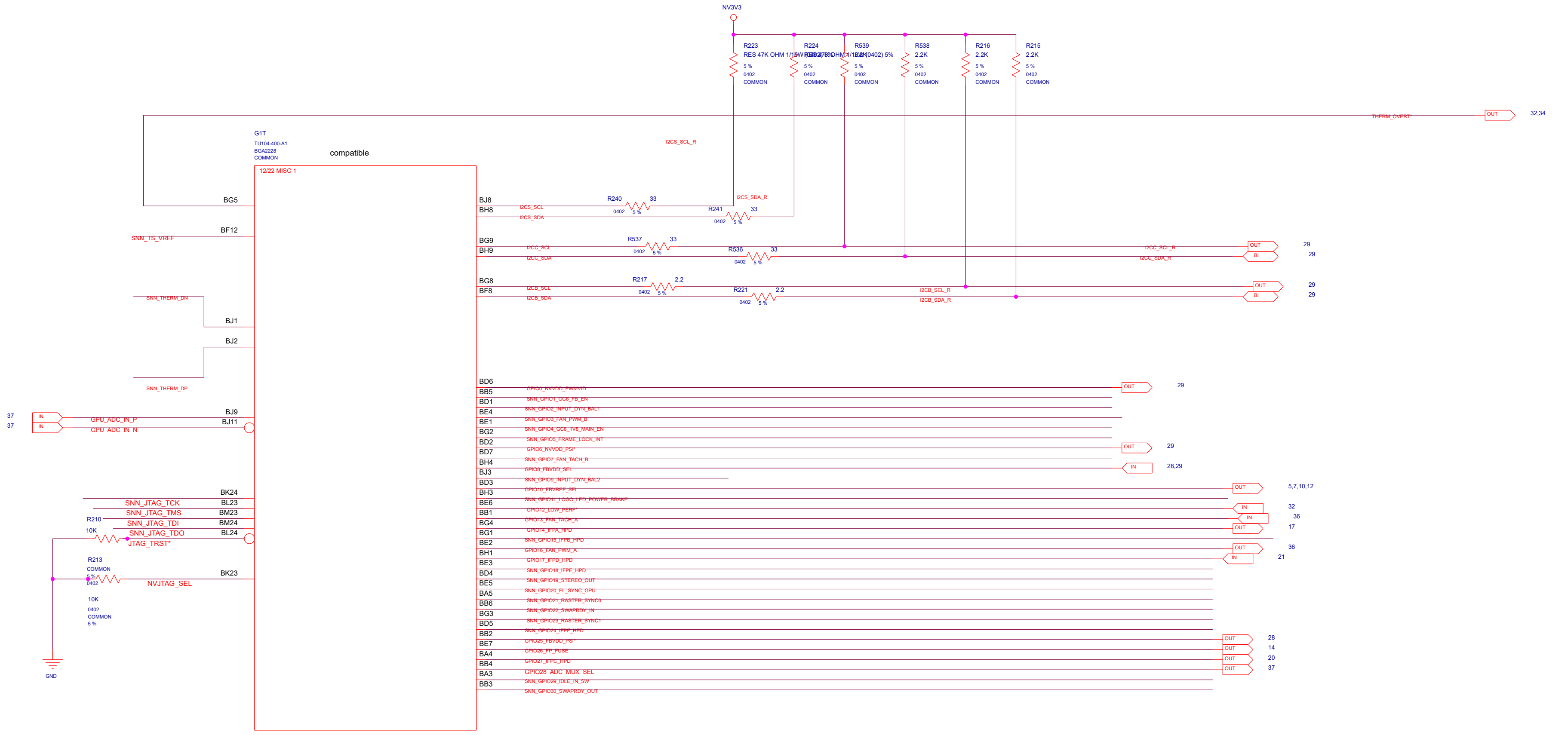
Page23: MISC1: Fan, Thermal, JTAG, GPIO



Title :	MISC1	
OrgName	Engineer:	James_Huang
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Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A:Z版 B
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V

M=Middle:Tied to 0.9V

L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE

0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND

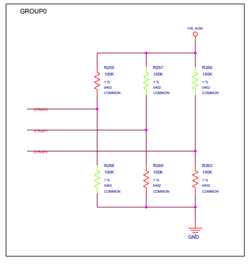
0:DEVID_SEL ORIGNAL

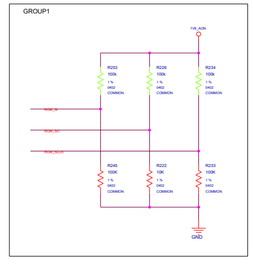
1:PCIE_CFG LOW POWER

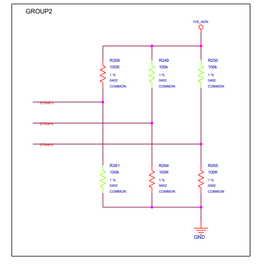
0:PCIE_CFG HIGH POWER

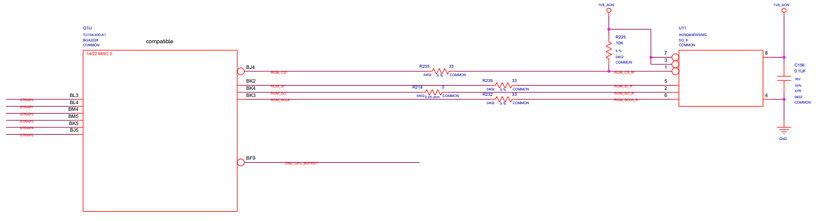
1:VGA_DEVICE ENABLE

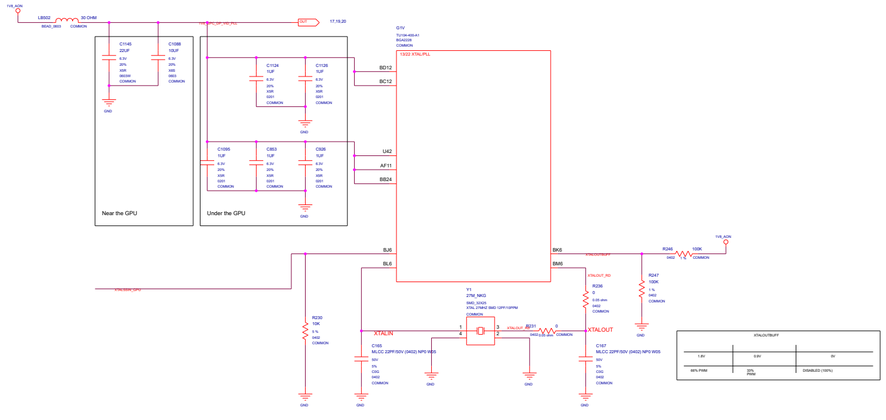
0:VGA_DEVICE DISABLE





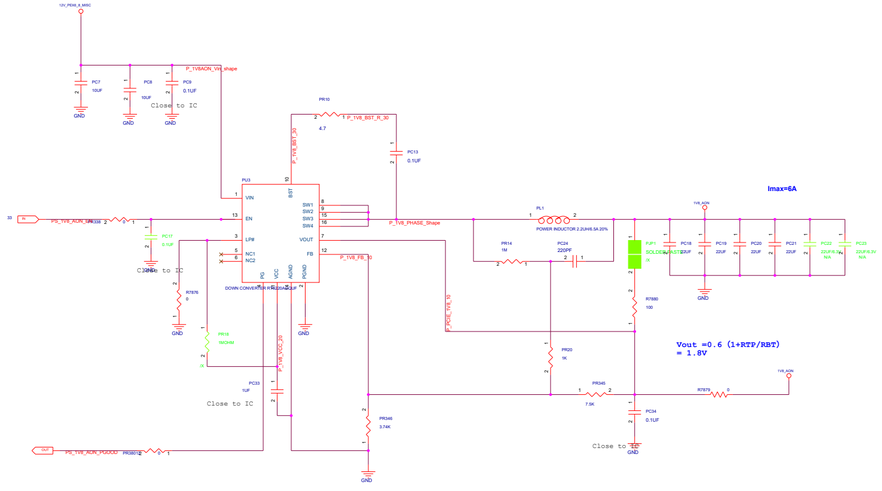






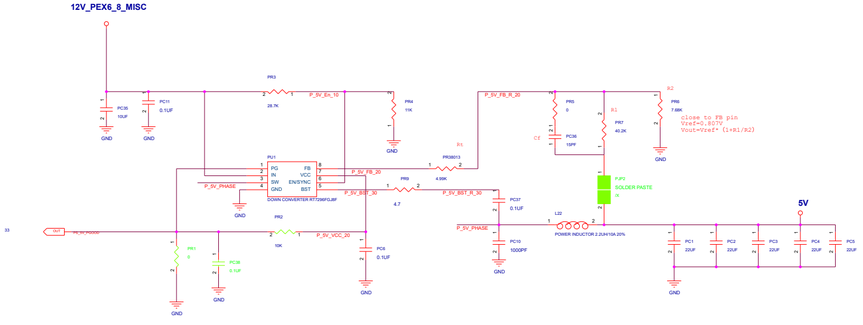
ASUS	Title :	MISC2	
OrgName	Engineer:	James_Huang	
Size: Custom	Project Name: CG165PI		Rev: 1.00
Date: Monday, July 01, 2019	Sheet 24 of 39		

Page25: PS: 1V8_AON



Title : 1V8_AON			
Engineer: James_Huang			
Size: Custom	Project Name: CG165PI		Rev: 1.00
Date: Monday, July 01, 2019	Sheet 25 of 39		

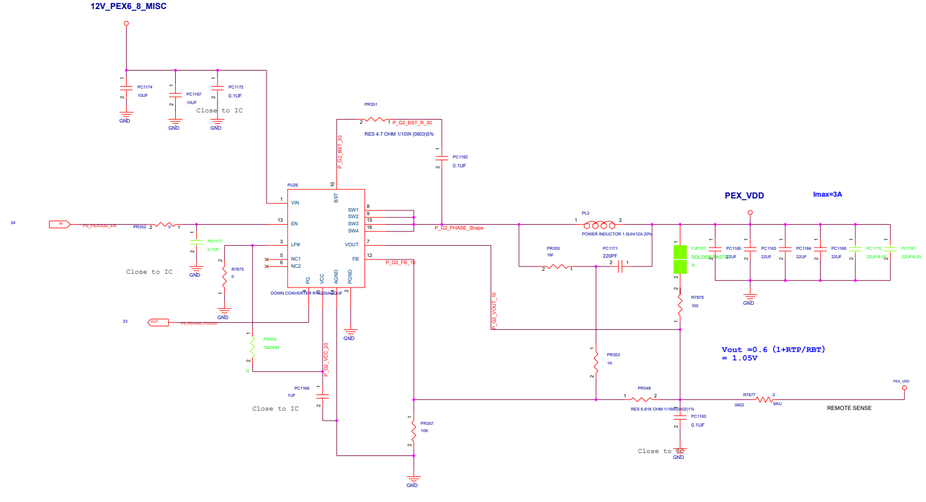
Page26: PS: 5V



Title : 5V			
Engineer: James_Huang			
Size: Custom	Project Name: CG165PI		Rev: 1.00
Date: Monday, July 01, 2019	Sheet: 26	of: 30	

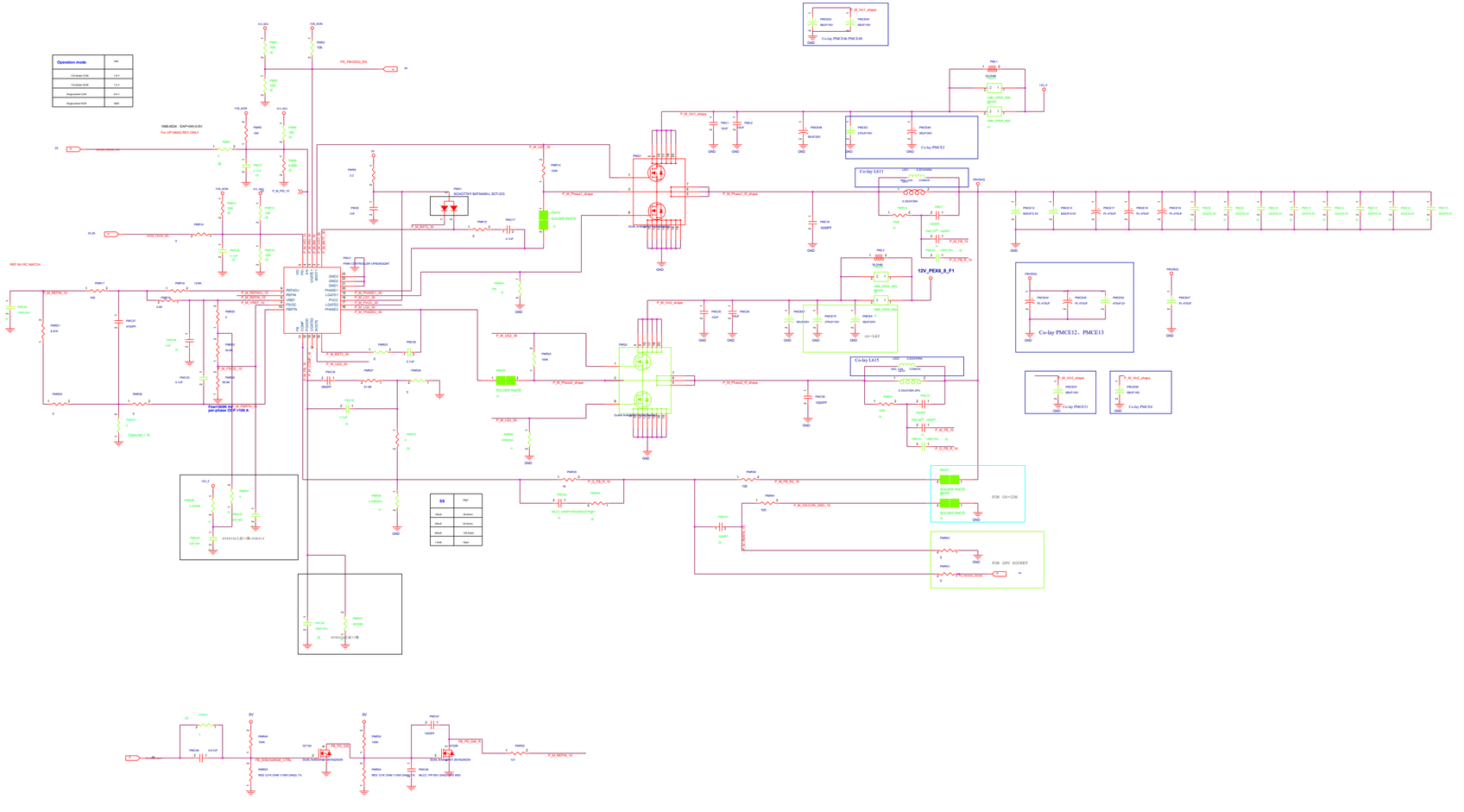
Page27: PS: PEXVDD

PEX Switcher

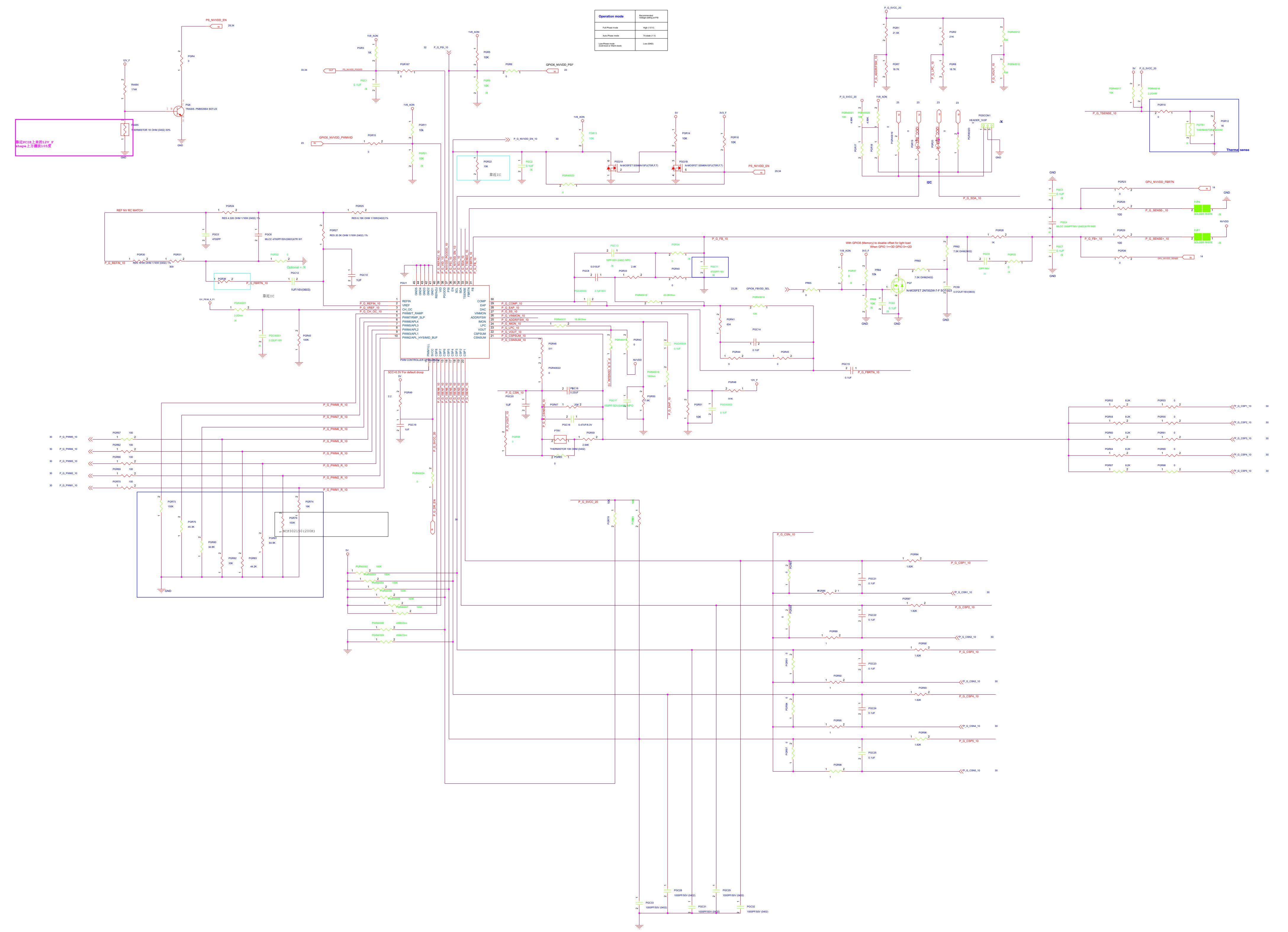


ASUS	Title : PS_PEX		
OrgName	Engineer: James_Huang		
Size: Custom	Project Name: CG165PI		Rev: 1.00
Date: Monday, July 01, 2019	Sheet 27 of 39		

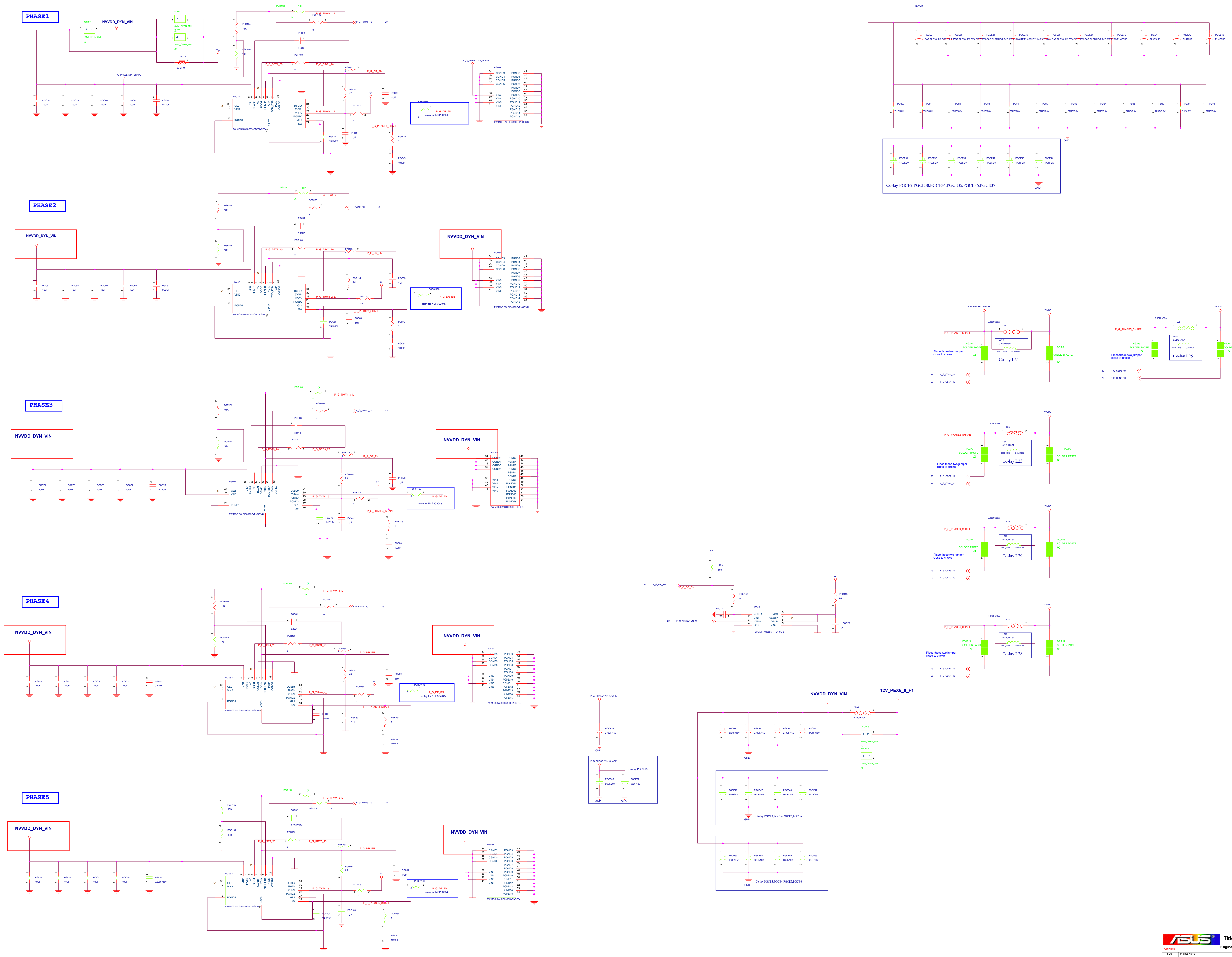
Page28: PS: FBVDDQ



Page29: PS: NVVDD CTR OVR3i



Title :	NVVDD Controller	
OrgName	Engineer:	James_Huang
Size: E	Project Name: CG165PI	Rev: 1.00
Date: Monday, July 01, 2019	Sheet 29 of 39	



Title :	NVVDD MOS
OrgName	Engineer: James_Huang
Size: Custom	Project Name: CG165PI
Rev	1.00
Date: Monday, July 01, 2019	Sheet 30 of 39

Page31: PS: Inputs, Filtering, and Monitoring

PEX 3V3 INPUT - 10W

PEX_12V INPUT - 66W

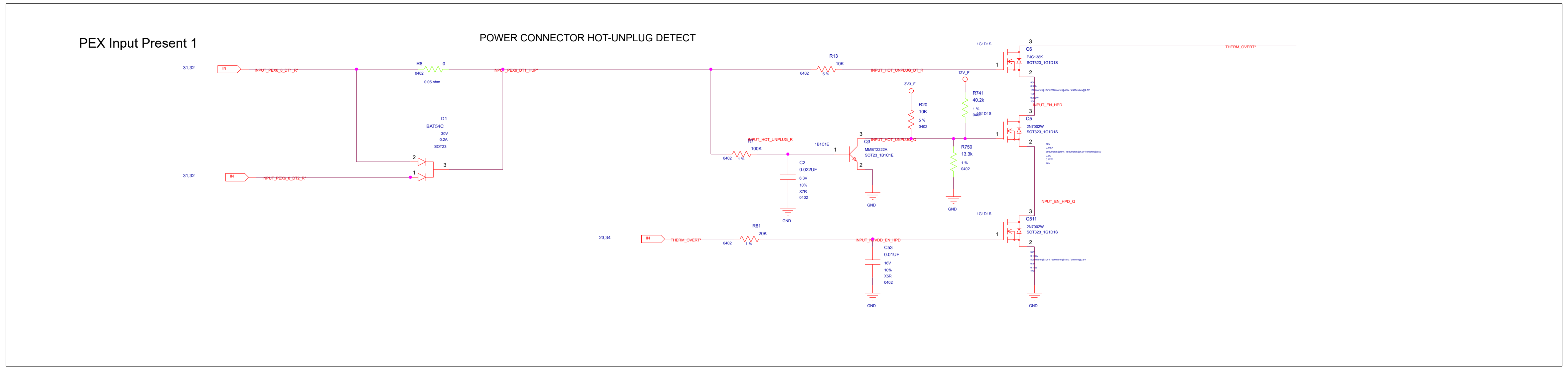
PEX8 INPUT 1 - 2x4 PCIE CON 150W

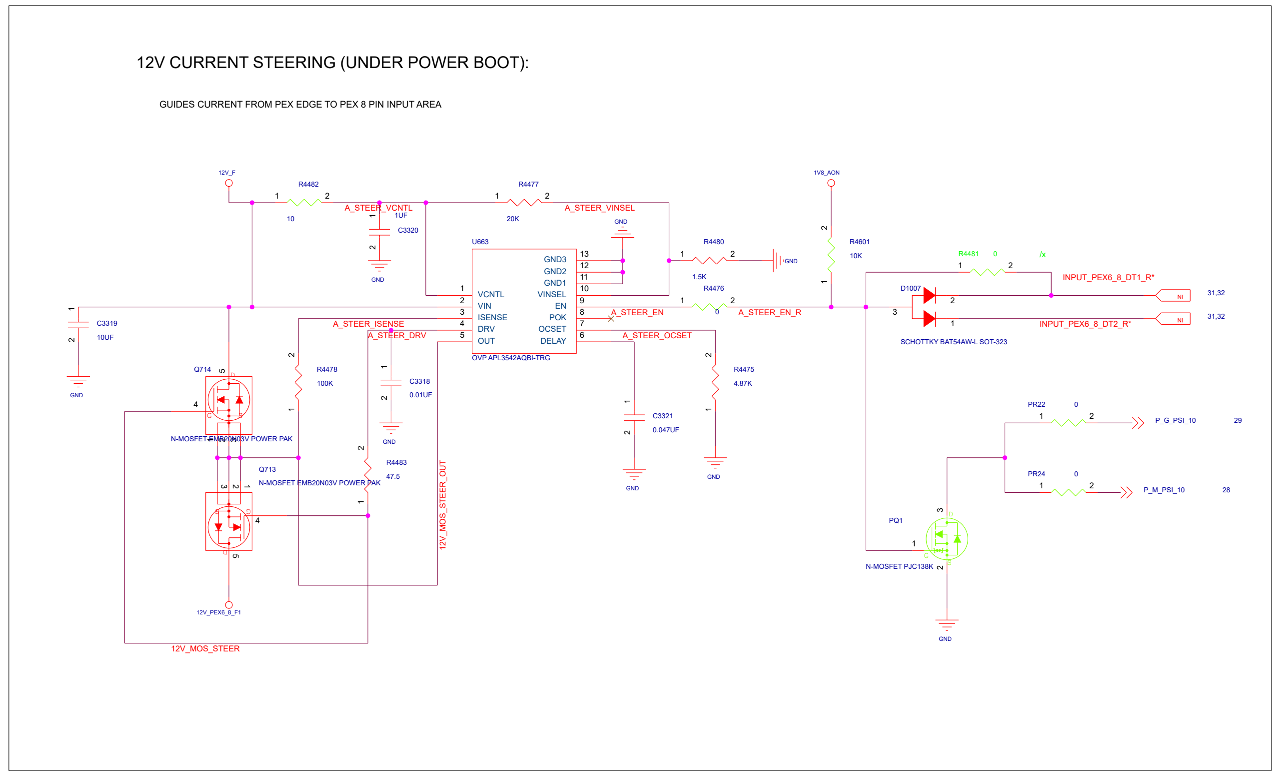
PEX 6/8 Input Present 1

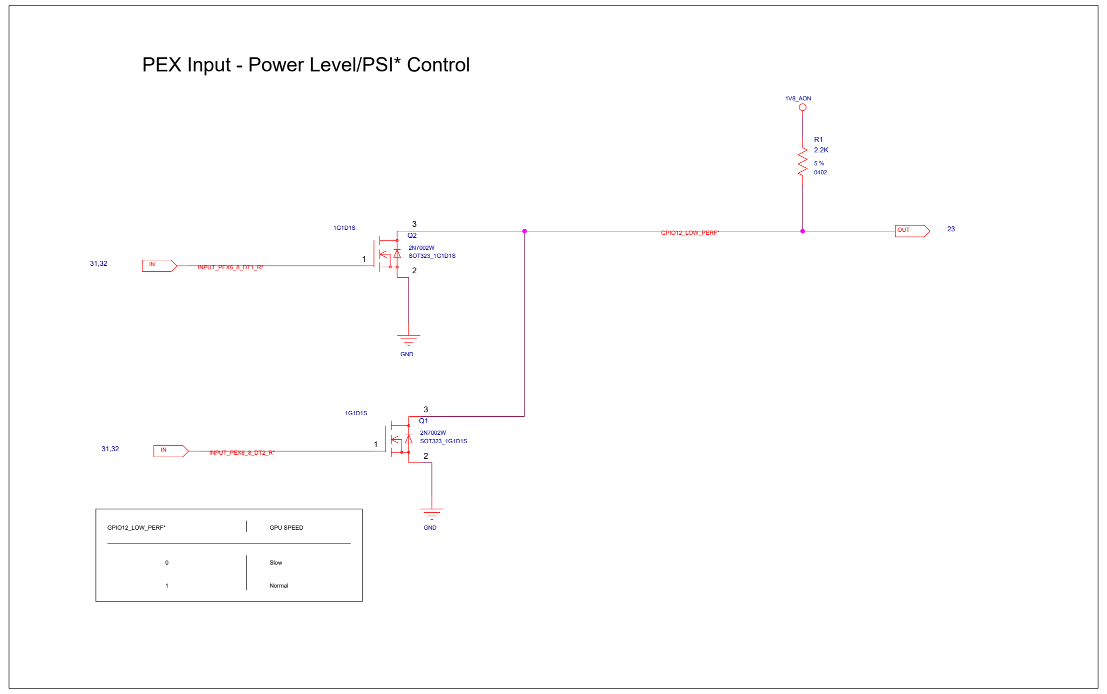
PEX 8 Input Present 2

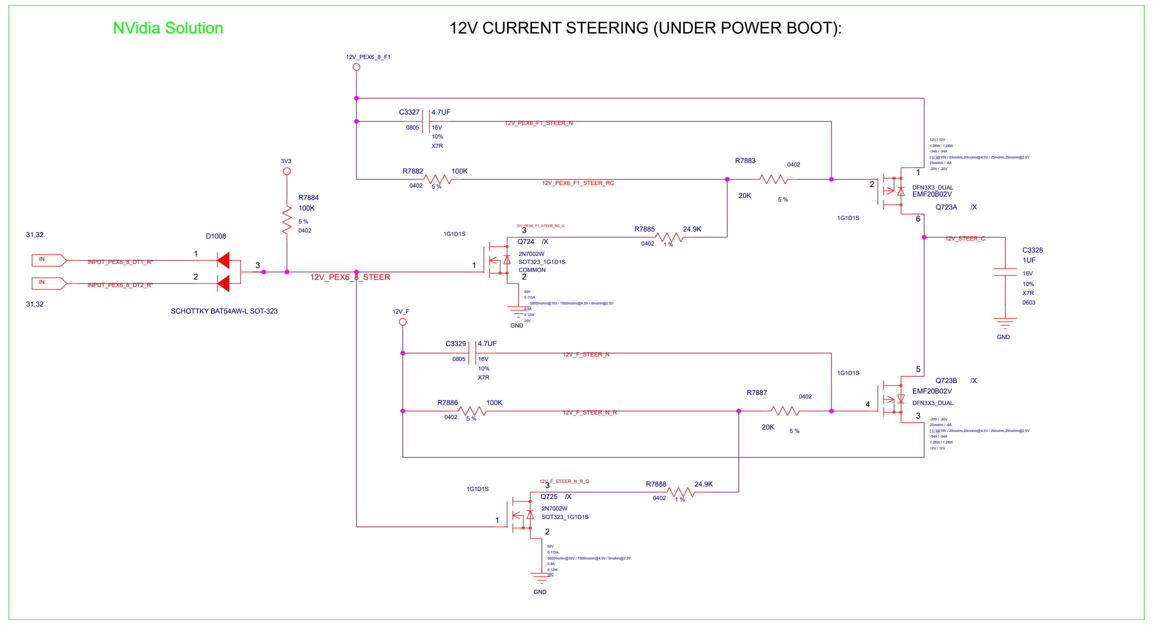
Title :	PS INPUT		
Orgname	Engineer:	James_Huang	
Size: Custom	Project Name: CG165PI		Rev: 1.00
Date: Monday, July 01, 2019	Sheet 31 of 38		

Page32: PS: HOT-UNPLUG, UNDER POWER BOOT, CURRENT STEERING



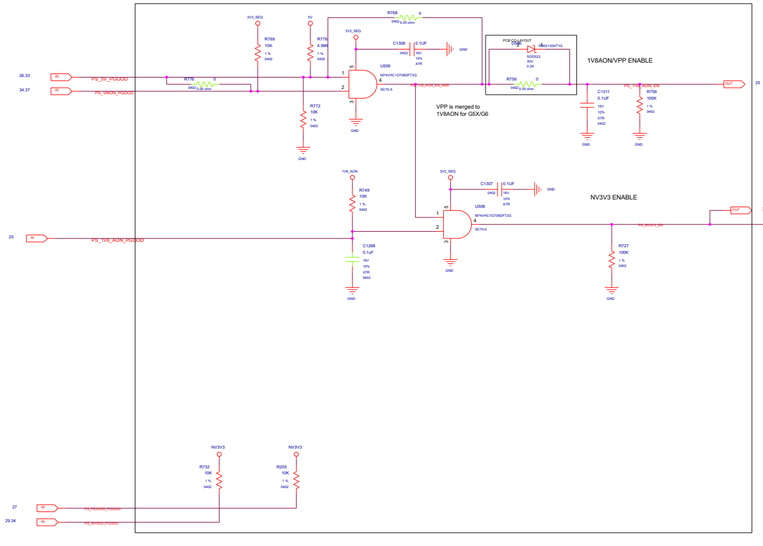


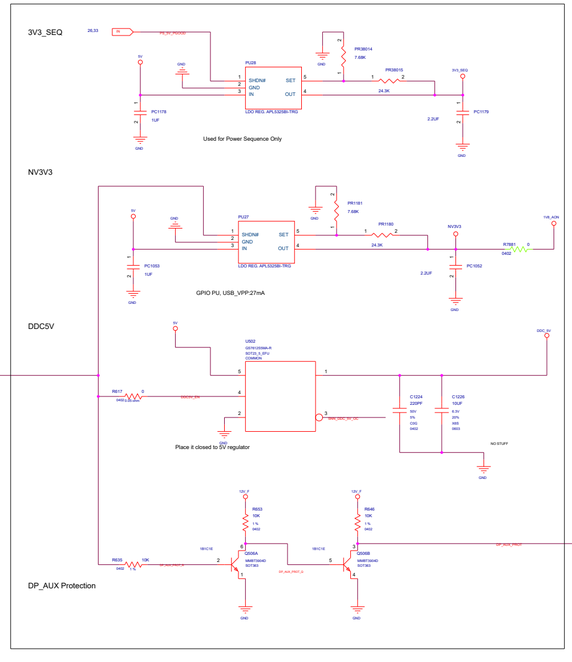




OrgName	Title : PS STEERING	
	Engineer: James_Huang	
Size: Custom	Project Name: CG165PI	Rev: 1.00
Date: Monday, July 01, 2019	Sheet 32 of 39	

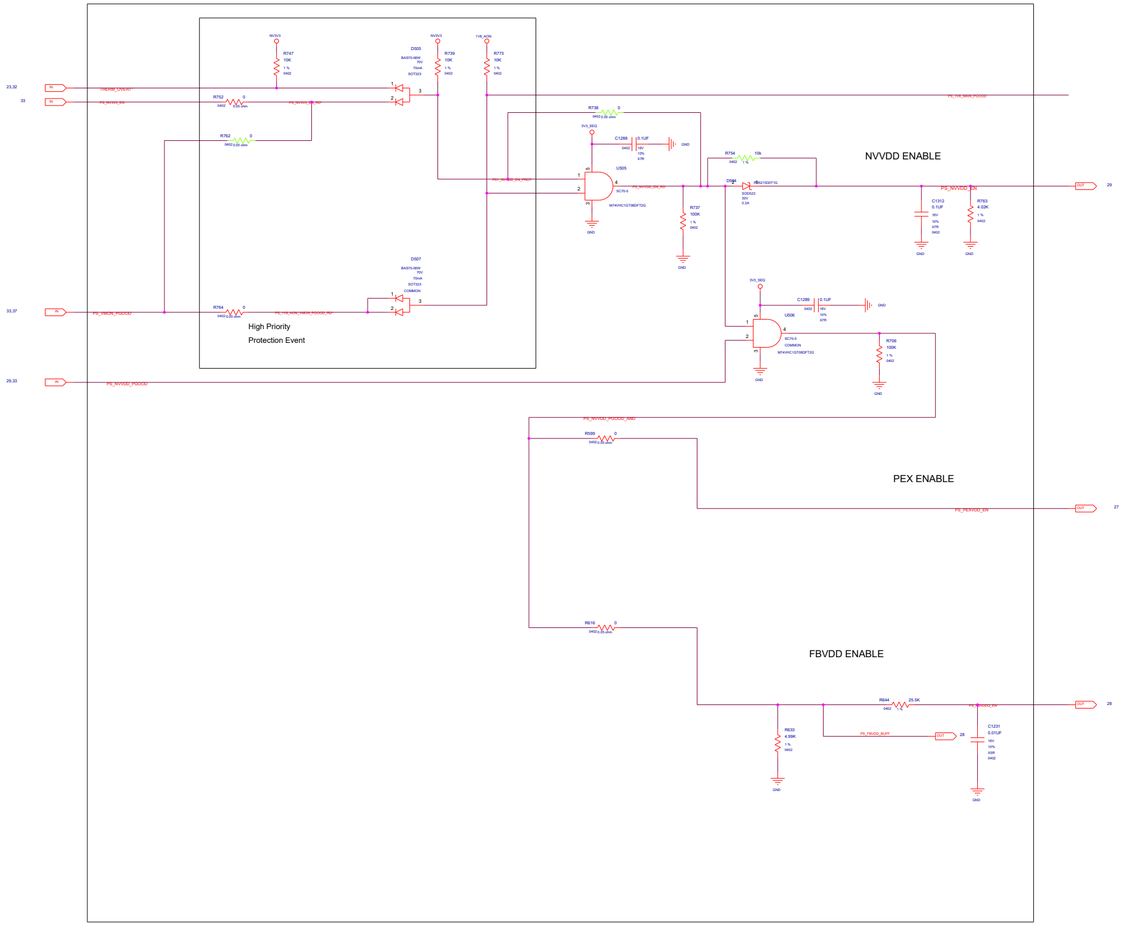
Page33: SEQ:5V,1V8,NV3V3 ENABLE





ASUS	Title : SEQ_5V		
Orgname	Engineer: James_Huang		
Size: Custom	Project Name: CG165PI		Rev: 1.00
Date: Monday, July 01, 2019	Sheet 33 of 39		

Page44: SEQ:NV,PEX,FB ENABLE



Title :	SEQ_NV
Engineer:	James_Huang
Size: Custom	Project Name: CG165PI
Rev:	1.00
Date:	Monday, July 01, 2019
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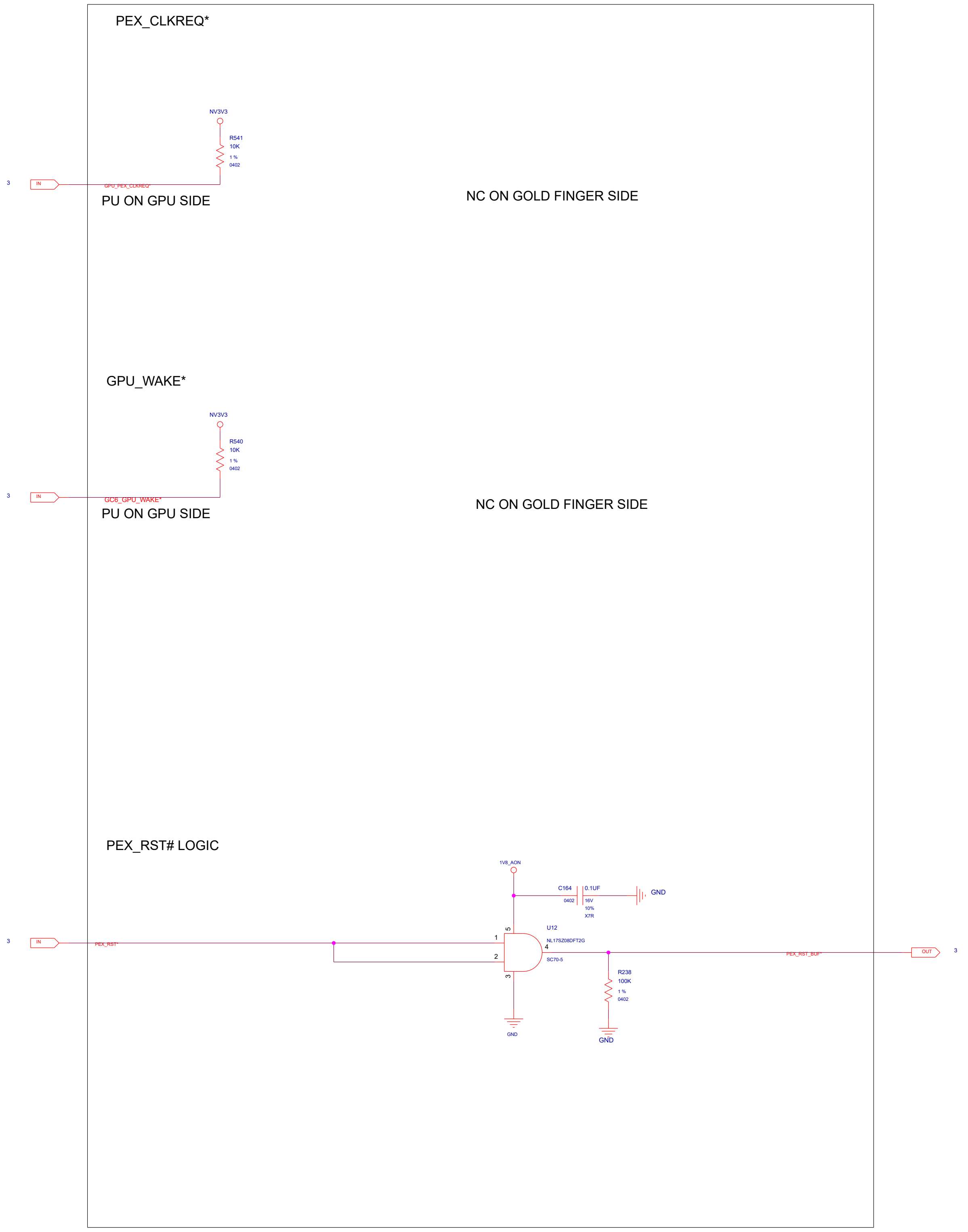
Page35: SEQUENCE:MISC



OrgName	Title : SEQ_MISC	
	Engineer: James_Huang	
Size: Custom	Project Name: CG165PI	Rev: 1.00
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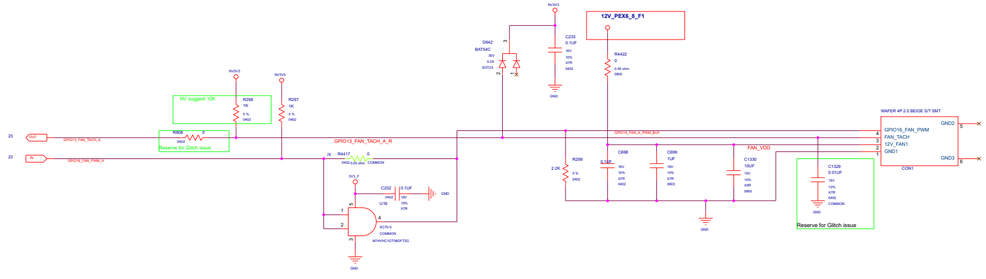
Page36: FAN

Add PWM FAN Solution



Title :	FAN
Engineer:	James_Huang
Size: Custom	Project Name: CG165PI
Rev: 1.00	
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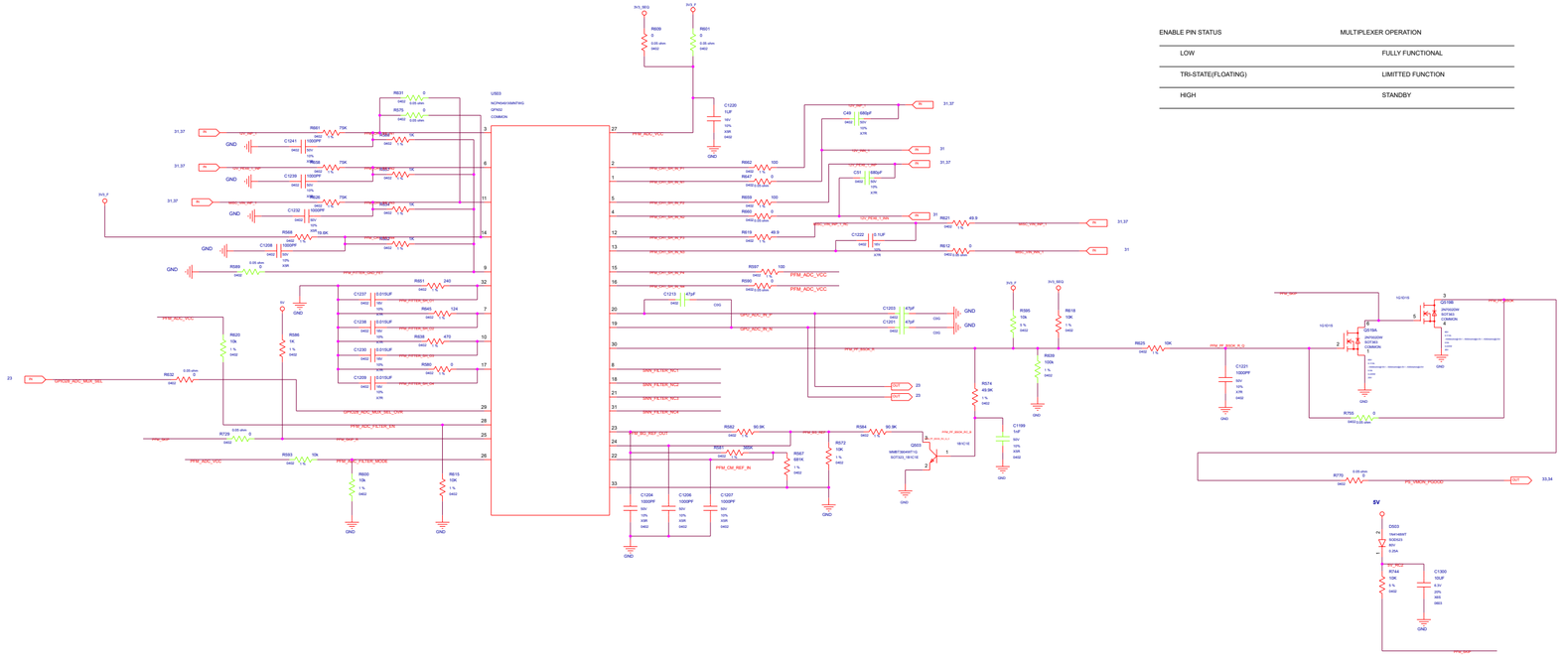
Page37:OVRM PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY

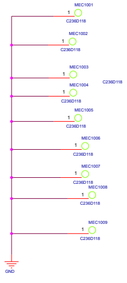


Title :	PS_Filter	
Orgname	Engineer:	James_Huang
Size: Custom	Project Name: CG165PI	Rev: 1.00
Date: Monday, July 01, 2019	Sheet 37 of 38	

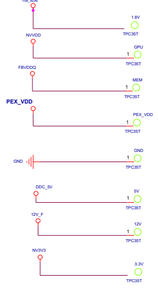
Page52: MECH

Bracket:

MOUNTING HOLES FOR HS:



BACK STIFFENER:



ASUS	Title : MECH	
OrgName	Engineer: James_Huang	
Size: Custom	Project Name: CG165PI	Rev: 1.00
Date: Monday, July 01, 2019	Sheet 39 of 39	

ASUS VGA PCB Logo

LOGO1
1 CE
CE
/X

LOGO2
1 VCCI
VCCI
/X

LOGO3
1 EMI_D33005_H
EMI_D33005_H
/X

LOGO4
1 FCC
FCC
/X

LOGO5
1 RCM
RCM
/X

LOGO6
1 CAN ICES-3(B)/NMB-3(B)
CAN_ICES_3B_NMB_3B
/X

CAN ICES-3 (B)/NMB-3(B)

LOGO7
1 KC R-R-MSQ-XXXXXXXXXXXXX
KC_R_R_LOGO
/X

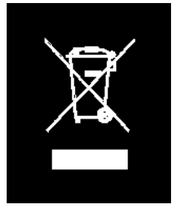
LOGO8
1 UKRAINE
UKRAINE
/X

LOGO9
1 PCB MADE IN CHINA
PCB_MADE_IN_CHINA
/X

PCB MADE IN CHINA

LOGO10
1 MARK_L
S_MARK_L
/X

LOGO11
1 WEEE_LOGO
WEEE_LOGO
/X



ASUSTEK COMPUTER INC	Title :	PCB Logo	
	Engineer:	Tomo	
Size	Project Name	ASUS VGA Logo	Rev 1.00
Date: Monday, July 01, 2019	Sheet 39 of 39		