41-P260, NV41 256bit, 4M/8Mx32bit DDR1 (350Mhz)

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10260-base-300	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10260-0000-300	NV41 128MB, 4Mx32 DDR1, VGA+DVI-I+HDTV-out; PCI-E Desktop
2	SKU0001	600-10260-0001-300	NV41 128MB, 4Mx32 DDR1, VGA+DVI-I+HD/VIVO; PCI-E Desktop
3	SKU0002	600-10260-0002-300	NV41 256MB, 8Mx32 DDR1, VGA+DVI-I+HDTV-out; PCI-E Desktop
4	SKU0500	600-50260-0000-300	NV41GL Quadro FX 1400 (NV41GLP260) 128MB, 256bit, DVI-DL+DVI-DL+Stereo, WS
5	SKU0800	600-10260-0800-300	NV41 Bringup SKU, 128MB, 4Mx32 DDR1
6	SKU0004	600-10260-0004-300	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
7	SKU0501	600-50260-0001-300	NV41GL Quadro FX 1400 256MB 256bit DVI-I+DVI-I+Stereo WS
8	SKU0005	600-10260-0005-300	NV41 Personal Cinema baseboard SKU (NTSC+PAL) 128MB VGA+DVI-I+VIVO/HD-Out + PCI-E
9	SKU0007	600-10260-0007-300	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+HDTV-out PCI-E Desktop - HP Sku
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

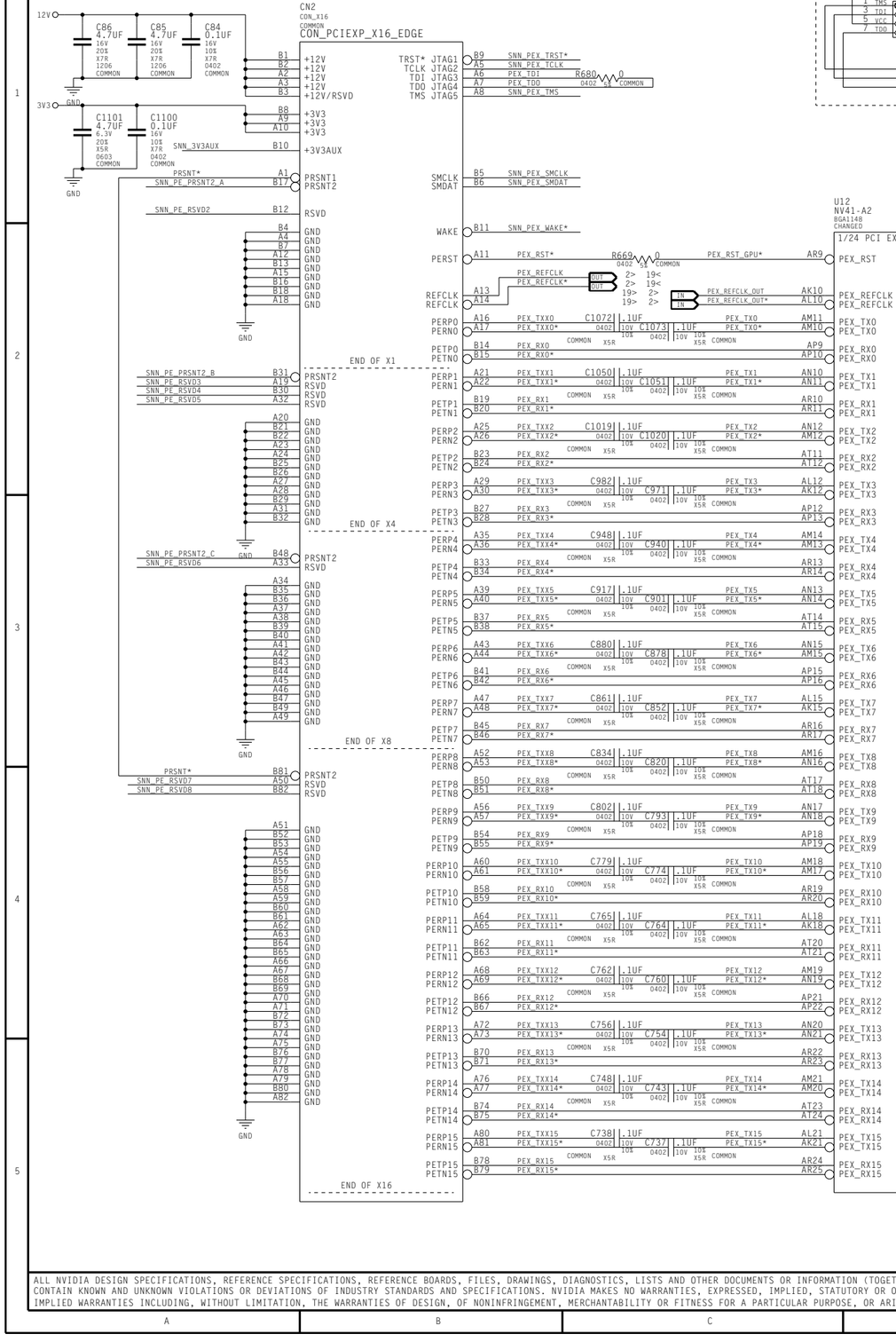
Page Overview

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	Overview

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	1 OF 37
NAME	JLAM	DATE	19-AUG-2004

2 PCI Express 1.0



3GIO NET RULES

NET	SPACING	LINE_WIDTH	DIFFPAIR
PEX_REFCLK	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_REFCLK
PEX_REFCLK*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_REFCLK
PEX_REFCLK_OUT	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_REFCLK_OUT
PEX_REFCLK_OUT*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_REFCLK_OUT
PEX_TXX0	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX0
PEX_TXX0*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX0
PEX_TXX1	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX1
PEX_TXX1*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX1
PEX_TXX2	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX2
PEX_TXX2*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX2
PEX_TXX3	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX3
PEX_TXX3*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX3
PEX_TXX4	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX4
PEX_TXX4*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX4
PEX_TXX5	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX5
PEX_TXX5*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX5
PEX_TXX6	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX6
PEX_TXX6*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX6
PEX_TXX7	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX7
PEX_TXX7*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX7
PEX_TXX8	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX8
PEX_TXX8*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX8
PEX_TXX9	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX9
PEX_TXX9*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX9
PEX_TXX10	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX10
PEX_TXX10*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX10
PEX_TXX11	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX11
PEX_TXX11*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX11
PEX_TXX12	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX12
PEX_TXX12*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX12
PEX_TXX13	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX13
PEX_TXX13*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX13
PEX_TXX14	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX14
PEX_TXX14*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX14
PEX_TXX15	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX15
PEX_TXX15*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TXX15
PEX_RX0	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX0
PEX_RX0*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX0
PEX_RX1	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX1
PEX_RX1*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX1
PEX_RX2	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX2
PEX_RX2*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX2
PEX_RX3	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX3
PEX_RX3*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX3
PEX_RX4	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX4
PEX_RX4*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX4
PEX_RX5	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX5
PEX_RX5*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX5
PEX_RX6	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX6
PEX_RX6*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX6
PEX_RX7	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX7
PEX_RX7*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX7
PEX_RX8	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX8
PEX_RX8*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX8
PEX_RX9	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX9
PEX_RX9*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX9
PEX_RX10	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX10
PEX_RX10*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX10
PEX_RX11	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX11
PEX_RX11*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX11
PEX_RX12	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX12
PEX_RX12*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX12
PEX_RX13	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX13
PEX_RX13*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX13
PEX_RX14	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX14
PEX_RX14*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX14
PEX_RX15	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX15
PEX_RX15*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_RX15
PEX_TX0	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX0
PEX_TX0*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX0
PEX_TX1	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX1
PEX_TX1*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX1
PEX_TX2	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX2
PEX_TX2*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX2
PEX_TX3	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX3
PEX_TX3*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX3
PEX_TX4	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX4
PEX_TX4*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX4
PEX_TX5	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX5
PEX_TX5*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX5
PEX_TX6	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX6
PEX_TX6*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX6
PEX_TX7	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX7
PEX_TX7*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX7
PEX_TX8	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX8
PEX_TX8*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX8
PEX_TX9	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX9
PEX_TX9*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX9
PEX_TX10	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX10
PEX_TX10*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX10
PEX_TX11	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX11
PEX_TX11*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX11
PEX_TX12	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX12
PEX_TX12*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX12
PEX_TX13	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX13
PEX_TX13*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX13
PEX_TX14	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX14
PEX_TX14*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX14
PEX_TX15	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX15
PEX_TX15*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	PEX_TX15
PEX_PLL_CLK_OUT			PEX_PLL_CLK_OUT
PEX_PLL_CLK_OUT*			PEX_PLL_CLK_OUT

Matching Rule of Thumb

4 inch from Top of Gold Fingers to GPU

*2 inch Lane to Lane Skew

*No real Skew rule, but reducing the skew will minimize latency

NET	VOLTAGE
PEX_IOVDDQ	1.2V
PEX_IOVDD	1.2V
PEX_PLLAVDD	1.2V
PEX_PLLDVDD	1.2V
3V3	3.3V
12V	12V

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	PCI Express 1.0

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	2 OF 37
NAME	JLAM	DATE	19-AUG-2004

3 FrameBuffer: GPU Partition A/B

NET RULES

NET	VOLTAGE
FBA_PLLVDD	3.3 V
FBB_PLL_VDD	3.3 V
FBAB_PLLAVDD	1.4 V

U12
NV41-A2
BGA1148
CHANGED

2/4 MEM_A

0	FBAD<0>	AH35	FBADO
1	FBAD<1>	AH36	FBAD1
2	FBAD<2>	AH34	FBAD2
3	FBAD<3>	AJ34	FBAD3
4	FBAD<4>	AK36	FBAD4
5	FBAD<5>	AJ36	FBAD5
6	FBAD<6>	AK34	FBAD6
7	FBAD<7>	AL34	FBAD7
8	FBAD<8>	AH32	FBAD8
9	FBAD<9>	AK33	FBAD9
10	FBAD<10>	AJ33	FBAD10
11	FBAD<11>	AH33	FBAD11
12	FBAD<12>	AL33	FBAD12
13	FBAD<13>	AN32	FBAD13
14	FBAD<14>	AN33	FBAD14
15	FBAD<15>	AN31	FBAD15
16	FBAD<16>	AL32	FBAD16
17	FBAD<17>	AP30	FBAD17
18	FBAD<18>	AP32	FBAD18
19	FBAD<19>	AE30	FBAD19
20	FBAD<20>	AE31	FBAD20
21	FBAD<21>	AC30	FBAD21
22	FBAD<22>	AC32	FBAD22
23	FBAD<23>	AD30	FBAD23
24	FBAD<24>	AG36	FBAD24
25	FBAD<25>	AG34	FBAD25
26	FBAD<26>	AG35	FBAD26
27	FBAD<27>	AF36	FBAD27
28	FBAD<28>	AD36	FBAD28
29	FBAD<29>	AD34	FBAD29
30	FBAD<30>	AD35	FBAD30
31	FBAD<31>	AE34	FBAD31
32	FBAD<32>	AP36	FBAD32
33	FBAD<33>	AN35	FBAD33
34	FBAD<34>	AM34	FBAD34
35	FBAD<35>	AP35	FBAD35
36	FBAD<36>	AP34	FBAD36
37	FBAD<37>	AP33	FBAD37
38	FBAD<38>	AT34	FBAD38
39	FBAD<39>	AR34	FBAD39
40	FBAD<40>	AM22	FBAD40
41	FBAD<41>	AM25	FBAD41
42	FBAD<42>	AN26	FBAD42
43	FBAD<43>	AN24	FBAD43
44	FBAD<44>	AK24	FBAD44
45	FBAD<45>	AL22	FBAD45
46	FBAD<46>	AK23	FBAD46
47	FBAD<47>	AM23	FBAD47
48	FBAD<48>	AT32	FBAD48
49	FBAD<49>	AT33	FBAD49
50	FBAD<50>	AR33	FBAD50
51	FBAD<51>	AP31	FBAD51
52	FBAD<52>	AR30	FBAD52
53	FBAD<53>	AT30	FBAD53
54	FBAD<54>	AP30	FBAD54
55	FBAD<55>	AT29	FBAD55
56	FBAD<56>	AP26	FBAD56
57	FBAD<57>	AP27	FBAD57
58	FBAD<58>	AT25	FBAD58
59	FBAD<59>	AP25	FBAD59
60	FBAD<60>	AR28	FBAD60
61	FBAD<61>	AP28	FBAD61
62	FBAD<62>	AT28	FBAD62
63	FBAD<63>	AP29	FBAD63

0	FBADQM<0>	AK35	FBADQM0
1	FBADQM<1>	AM33	FBADQM1
2	FBADQM<2>	AF33	FBADQM2
3	FBADQM<3>	AF34	FBADQM3
4	FBADQM<4>	AN34	FBADQM4
5	FBADQM<5>	AM24	FBADQM5
6	FBADQM<6>	AP32	FBADQM6
7	FBADQM<7>	AR27	FBADQM7

	TP_FBADQS0*	AL35	FBADQS_RN0
	TP_FBADQS1*	AK32	FBADQS_RN1
	TP_FBADQS2*	AG33	FBADQS_RN2
	TP_FBADQS3*	AE36	FBADQS_RN3
	TP_FBADQS4*	AM36	FBADQS_RN4
	TP_FBADQS5*	AN22	FBADQS_RN5
	TP_FBADQS6*	AR31	FBADQS_RN6
	TP_FBADQS7*	AT27	FBADQS_RN7

0	FBADQS<0>	AL36	FBADQS_WP0
1	FBADQS<1>	AL32	FBADQS_WP1
2	FBADQS<2>	AG32	FBADQS_WP2
3	FBADQS<3>	AE35	FBADQS_WP3
4	FBADQS<4>	AN36	FBADQS_WP4
5	FBADQS<5>	AN23	FBADQS_WP5
6	FBADQS<6>	AJ31	FBADQS_WP6
7	FBADQS<7>	AJ26	FBADQS_WP7

	FB_VREF1	J29	FB_VREF1

FBA_CMD0	AK28	FBA_CMD<0>	0
FBA_CMD1	AK29	FBA_CMD<1>	1
FBA_CMD2	AN30	FBA_CMD<2>	2
FBA_CMD3	AM27	FBA_CMD<3>	3
FBA_CMD4	AN28	FBA_CMD<4>	4
FBA_CMD5	AL29	FBA_CMD<5>	5
FBA_CMD6	AM30	FBA_CMD<6>	6
FBA_CMD7	AJ31	FBA_CMD<7>	7
FBA_CMD8	AK31	FBA_CMD<8>	8
FBA_CMD9	AH31	FBA_CMD<9>	9
FBA_CMD10	AK25	FBA_CMD<10>	10
FBA_CMD11	AM26	FBA_CMD<11>	11
FBA_CMD12	AL31	TP_FBA_CMD12	
FBA_CMD13	AN29	FBA_CMD<13>	13
FBA_CMD14	AK27	FBA_CMD<14>	14
FBA_CMD15	AK26	FBA_CMD<15>	15
FBA_CMD16	AN27	FBA_CMD<16>	16
FBA_CMD17	AL25	FBA_CMD<17>	17
FBA_CMD18	AJ30	FBA_CMD<18>	18
FBA_CMD19	AM31	FBA_CMD<19>	19
FBA_CMD20	AH30	FBA_CMD<20>	20
FBA_CMD21	AL30	FBA_CMD<21>	21
FBA_CMD22	AH29	FBA_CMD<22>	22
FBA_CMD23	AL28	FBA_CMD<23>	23
FBA_CMD24	AH28	FBA_CMD<24>	24
FBA_CMD25	AM28	FBA_CMD<25>	25
FBA_CMD26	AG30	TP_FBA_CMD_26	

FBA_CMD<0..26> OUT 5<

FBA_CLK0	AH26	FBA_CLKO	OUT 5<
FBA_CLK0	AH27	FBA_CLKO*	OUT 5<
FBA_CLK1	AJ29	FBA_CLK1	OUT 5<
FBA_CLK1	AJ28	FBA_CLK1*	OUT 5<

144BGA CMD_Mapping

CMD	ADDR
CMD0	A<3>
CMD1	A<0>
CMD2	A<2>
CMD3	A<1>
CMD4	A<3>
CMD5	A<4>
CMD6	A<5>
CMD7	CS1* *not used
CMD8	CS0*
CMD9	WE*
CMD10	BA0
CMD11	CKE
CMD12	RESET
CMD13	A<2>
CMD14	A<12>
CMD15	RAS*
CMD16	A<11>
CMD17	A<10
CMD18	BA1
CMD19	A<8>
CMD20	A<9>
CMD21	A<6>
CMD22	A<5>
CMD23	A<7>
CMD24	A<4>
CMD25	CAS*
CMD26	A<13> *not used

If Refclk is not used
Stuff 10K to GND

HW now powers down the Pads when not used.
No longer need pulldowns.

RFU	AJ24	SNN_FBA_RFU0	
RFU	AH24	SNN_FBA_RFU1	
FBA_DEBUG	AH25	TP_FBA_DEBUG	
FBA_REFCLK	AF28	FBA_REFCLK	
FBA_REFCLK	AG28	FBA_REFCLK*	

R596 10K 5% 0402 NO STUFF
R599 10K 5% 0402 NO STUFF

FBCALO_PD_VDDQ	J28	FBCALO_PD_VDDQ	R595 43.2 0402 1% CHANGED → FBVDDQ
FBCALO_PU_GND	H28	FBCALO_PU_GND	R593 43.2 0402 1% CHANGED
FBCALO_TERM_GND	H29	FBCALO_TERM_GND	R590 0 0402 5% COMMON → GND

FBA_PLLVDD	AF29	FBA_PLLVDD	MIN_LINE_WIDTH=12MIL
FBA_PLLAVDD	AD29	FBAB_PLLAVDD	MIN_LINE_WIDTH=10MIL
FBA_PLLGND	AE29		

150-220R@100MHz LB502 BEAD_0603 COMMON → A3V3

C781 .01UF 16V 10% X7R 0402 COMMON
C771 .1UF 10V 10% X5R 0402 COMMON
C759 4.7UF 6.3V 20% X5R 0603 COMMON
C755 4.7UF 6.3V 20% X5R 0603 COMMON

150-220R@100MHz LB501 BEAD_0603 COMMON → NVVDD

C790 .01UF 16V 10% X7R 0402 COMMON
C791 .1UF 10V 10% X5R 0402 COMMON
C758 4.7UF 6.3V 20% X5R 0603 COMMON
C753 4.7UF 6.3V 20% X5R 0603 COMMON

FBVDDQ
C780 .1UF 10V 10% X5R 0402 NO STUFF
R592 1K 1% 0402 COMMON
C766 .1UF 10V 10% X5R 0402 COMMON
R589 1K 1% 0402 COMMON
GND GND

U12
NV41-A2
BGA1148
CHANGED

3/4 MEM_B

0	FBBD<0>	G36	FBBDO
1	FBBD<1>	G35	FBBD1
2	FBBD<2>	H36	FBBD2
3	FBBD<3>	H34	FBBD3
4	FBBD<4>	J35	FBBD4
5	FBBD<5>	J34	FBBD5
6	FBBD<6>	K34	FBBD6
7	FBBD<7>	K35	FBBD7
8	FBBD<8>	J31	FBBD8
9	FBBD<9>	K32	FBBD9
10	FBBD<10>	J30	FBBD10
11	FBBD<11>	H30	FBBD11
12	FBBD<12>	L32	FBBD12
13	FBBD<13>	K30	FBBD13
14	FBBD<14>	M31	FBBD14
15	FBBD<15>	L30	FBBD15
16	FBBD<16>	G31	FBBD16
17	FBBD<17>	J32	FBBD17
18	FBBD<18>	J33	FBBD18
19	FBBD<19>	F33	FBBD19
20	FBBD<20>	H31	FBBD20
21	FBBD<21>	E33	FBBD21
22	FBBD<22>	F31	FBBD22
23	FBBD<23>	F32	FBBD23
24	FBBD<24>	F35	FBBD24
25	FBBD<25>	G34	FBBD25
26	FBBD<26>	F36	FBBD26
27	FBBD<27>	F34	FBBD27
28	FBBD<28>	C35	FBBD28
29	FBBD<29>	D34	FBBD29
30	FBBD<30>	C36	FBBD30
31	FBBD<31>	D35	FBBD31
32	FBBD<32>	N35	FBBD32
33	FBBD<33>	M34	FBBD33
34	FBBD<34>	L34	FBBD34
35	FBBD<35>	N36	FBBD35
36	FBBD<36>	P36	FBBD36
37	FBBD<37>	P34	FBBD37
38	FBBD<38>	R36	FBBD38
39	FBBD<39>	R34	FBBD39
40	FBBD<40>	AC33	FBBD40
41	FBBD<41>	Y33	FBBD41
42	FBBD<42>	Y30	FBBD42
43	FBBD<43>	AB30	FBBD43
44	FBBD<44>	AA32	FBBD44
45	FBBD<45>	AD32	FBBD45
46	FBBD<46>	AD33	FBBD46
47	FBBD<47>	AA33	FBBD47
48	FBBD<48>	T36	FBBD48
49	FBBD<49>	R35	FBBD49
50	FBBD<50>	T34	FBBD50
51	FBBD<51>	U36	FBBD51
52	FBBD<52>	W35	FBBD52
53	FBBD<53>	U34	FBBD53
54	FBBD<54>	V34	FBBD54
55	FBBD<55>	W36	FBBD55
56	FBBD<56>	AC36	FBBD56
57	FBBD<57>	AA36	FBBD57
58	FBBD<58>	AC34	FBBD58
59	FBBD<59>	AB34	FBBD59
60	FBBD<60>	AA35	FBBD60
61	FBBD<61>	Y34	FBBD61
62	FBBD<62>	Y36	FBBD62
63	FBBD<63>	W34	FBBD63

0	FBBDQM<0>	J36	FBBDQM0
1	FBBDQM<1>	M32	FBBDQM1
2	FBBDQM<2>	H33	FBBDQM2
3	FBBDQM<3>	E34	FBBDQM3
4	FBBDQM<4>	N34	FBBDQM4
5	FBBDQM<5>	Y32	FBBDQM5
6	FBBDQM<6>	T35	FBBDQM6
7	FBBDQM<7>	AA34	FBBDQM7

	TP_FBBDQS0*	L36	FBBDQS_RN0
	TP_FBBDQS1*	K33	FBBDQS_RN1
	TP_FBBDQS2*	G32	FBBDQS_RN2
	TP_FBBDQS3*	E36	FBBDQS_RN3
	TP_FBBDQS4*	M36	FBBDQS_RN4
	TP_FBBDQS5*	AB32	FBBDQS_RN5
	SNN_FBBDQS6*	V35	FBBDQS_RN6
	TP_FBBDQS7*	AB35	FBBDQS_RN7

0	FBBDQS<0>	K36	FBBDQS_WP0
1	FBBDQS<1>	L33	FBBDQS_WP1
2	FBBDQS<2>	G33	FBBDQS_WP2
3	FBBDQS<3>	D36	FBBDQS_WP3
4	FBBDQS<4>	M35	FBBDQS_WP4
5	FBBDQS<5>	AB31	FBBDQS_WP5
6	FBBDQS<6>	V36	FBBDQS_WP6
7	FBBDQS<7>	AB36	FBBDQS_WP7

	FB_VREF2	J27	FB_VREF2

FBB_CMD0	P33	FBB_CMD<0>	0
FBB_CMD1	N33	FBB_CMD<1>	1
FBB_CMD2	R31	FBB_CMD<2>	2
FBB_CMD3	U33	FBB_CMD<3>	3
FBB_CMD4	V30	FBB_CMD<4>	4
FBB_CMD5	T33	FBB_CMD<5>	5
FBB_CMD6	T30	FBB_CMD<6>	6
FBB_CMD7	N32	FBB_CMD<7>	7
FBB_CMD8	R32	FBB_CMD<8>	8
FBB_CMD9	P32	FBB_CMD<9>	9
FBB_CMD10	U32	FBB_CMD<10>	10
FBB_CMD11	U30	FBB_CMD<11>	11
FBB_CMD12	P30	SNN_FBB_CMD12	
FBB_CMD13	V31	FBB_CMD<13>	13
FBB_CMD14	T28	FBB_CMD<14>	14
FBB_CMD15	W30	FBB_CMD<15>	15
FBB_CMD16	V32	FBB_CMD<16>	16
FBB_CMD17	T32	FBB_CMD<17>	17
FBB_CMD18	N30	FBB_CMD<18>	18
FBB_CMD19	P28	FBB_CMD<19>	19
FBB_CMD20	P29	FBB_CMD<20>	20
FBB_CMD21	U29	FBB_CMD<21>	21
FBB_CMD22	N28	FBB_CMD<22>	22
FBB_CMD23	R30	FBB_CMD<23>	23
FBB_CMD24	M30	FBB_CMD<24>	24
FBB_CMD25	T29	FBB_CMD<25>	25
FBB_CMD26	N29	SNN_FBB_CMD26	

FBB_CMD<0..26> OUT 7<

FBB_CLK0	M28	FBB_CLKO	OUT 7<
FBB_CLK0	L28	FBB_CLKO*	OUT 7<
FBB_CLK1	W31	FBB_CLK1	OUT 7<
FBB_CLK1	W32	FBB_CLK1*	OUT 7<

If Refclk is not used
Stuff 10K to GND

RFU	R28	SNN_FBB_RFU0	
RFU	K29	SNN_FBB_RFU1	
FBB_DEBUG	C34	TP_FBB_DEBUG	
FBB_REFCLK	AA30	FBB_REFCLK	
FBB_REFCLK	Y29	FBB_REFCLK*	

R594 10K 5% 0402 NO STUFF
R591 10K 5% 0402 NO STUFF

FBCAL1_PD_VDDQ	H27	FBCAL1_PD_VDDQ	R600 43.2 0402 1% CHANGED → FBVDDQ
FBCAL1_PU_GND	H26	FBCAL1_PU_GND	R601 43.2 0402 1% CHANGED
FBCAL1_TERM_GND	J26	FBCAL1_TERM_GND	R602 0 0402 5% COMMON → GND

FBB_PLLVDD	AB28	FBB_PLL_VDD	MIN_LINE_WIDTH=12MIL
FBB_PLLAVDD	AC29	FBAB_PLLAVDD	
FBB_PLLGND	AC28		

150-220R@100MHz LB503 BEAD_0603 COMMON → A3V3

C796 .01UF 16V 10% X7R 0402 COMMON
C805 .1UF 10V 10% X5R 0402 COMMON
C757 4.7UF 6.3V 20% X5R 0603 COMMON
C763 4.7UF 6.3V 20% X5R 0603 COMMON

FBVDDQ
C800 .1UF 10V 10% X5R 0402 NO STUFF
R598 1K 1% 0402 COMMON
C799 .1UF 10V 10% X5R 0402 COMMON
R597 1K 1% 0402 COMMON
GND GND

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	MEMORY: GPU Partition A/B

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	3 OF 37
NAME	JLAM	DATE	19-AUG-2004

4 FrameBuffer: GPU Partition C/D

NET RULES

NET	VOLTAGE
FBC_PLLVDD	3.3 V
FBD_PLLVDD	3.3 V
FBCD_AVDD	1.4 V

U12
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4/24 MEM_C

9<>	BI	FBCD<63..0>	
9<>	OUT	FBCDQM<7..0>	
9<>	BI	FBCDQS<7..0>	

0	FBCD<0>	C18	FBCD0
1	FBCD<1>	C17	FBCD1
2	FBCD<2>	A17	FBCD2
3	FBCD<3>	B16	FBCD3
4	FBCD<4>	C14	FBCD4
5	FBCD<5>	A16	FBCD5
6	FBCD<6>	C15	FBCD6
7	FBCD<7>	A14	FBCD7
8	FBCD<8>	A18	FBCD8
9	FBCD<9>	A19	FBCD9
10	FBCD<10>	B19	FBCD10
11	FBCD<11>	B18	FBCD11
12	FBCD<12>	B21	FBCD12
13	FBCD<13>	C19	FBCD13
14	FBCD<14>	B22	FBCD14
15	FBCD<15>	C21	FBCD15
16	FBCD<16>	E15	FBCD16
17	FBCD<17>	D16	FBCD17
18	FBCD<18>	D17	FBCD18
19	FBCD<19>	G16	FBCD19
20	FBCD<20>	E16	FBCD20
21	FBCD<21>	E14	FBCD21
22	FBCD<22>	G13	FBCD22
23	FBCD<23>	D13	FBCD23
24	FBCD<24>	A22	FBCD24
25	FBCD<25>	C22	FBCD25
26	FBCD<26>	C23	FBCD26
27	FBCD<27>	A23	FBCD27
28	FBCD<28>	A24	FBCD28
29	FBCD<29>	C24	FBCD29
30	FBCD<30>	C25	FBCD30
31	FBCD<31>	B24	FBCD31
32	FBCD<32>	C28	FBCD32
33	FBCD<33>	B27	FBCD33
34	FBCD<34>	C27	FBCD34
35	FBCD<35>	B28	FBCD35
36	FBCD<36>	C29	FBCD36
37	FBCD<37>	A29	FBCD37
38	FBCD<38>	B30	FBCD38
39	FBCD<39>	A30	FBCD39
40	FBCD<40>	E31	FBCD40
41	FBCD<41>	E28	FBCD41
42	FBCD<42>	D28	FBCD42
43	FBCD<43>	F29	FBCD43
44	FBCD<44>	F30	FBCD44
45	FBCD<45>	D33	FBCD45
46	FBCD<46>	D32	FBCD46
47	FBCD<47>	D31	FBCD47
48	FBCD<48>	G27	FBCD48
49	FBCD<49>	F25	FBCD49
50	FBCD<50>	G26	FBCD50
51	FBCD<51>	D26	FBCD51
52	FBCD<52>	G29	FBCD52
53	FBCD<53>	G28	FBCD53
54	FBCD<54>	E27	FBCD54
55	FBCD<55>	F28	FBCD55
56	FBCD<56>	A34	FBCD56
57	FBCD<57>	C32	FBCD57
58	FBCD<58>	B34	FBCD58
59	FBCD<59>	C33	FBCD59
60	FBCD<60>	C31	FBCD60
61	FBCD<61>	B31	FBCD61
62	FBCD<62>	A31	FBCD62
63	FBCD<63>	C30	FBCD63

0	FBCDQM<0>	C16	FBCDQM0
1	FBCDQM<1>	C20	FBCDQM1
2	FBCDQM<2>	G14	FBCDQM2
3	FBCDQM<3>	C26	FBCDQM3
4	FBCDQM<4>	A28	FBCDQM4
5	FBCDQM<5>	D29	FBCDQM5
6	FBCDQM<6>	D27	FBCDQM6
7	FBCDQM<7>	B33	FBCDQM7

	TP_FBCDQS0*	B15	FBCDQS_RN0
	TP_FBCDQS1*	A21	FBCDQS_RN1
	TP_FBCDQS2*	D14	FBCDQS_RN2
	TP_FBCDQS3*	B25	FBCDQS_RN3
	TP_FBCDQS4*	A27	FBCDQS_RN4
	TP_FBCDQS5*	E30	FBCDQS_RN5
	TP_FBCDQS6*	E25	FBCDQS_RN6
	TP_FBCDQS7*	A33	FBCDQS_RN7

0	FBCDQS<0>	A15	FBCDQS_WP0
1	FBCDQS<1>	A20	FBCDQS_WP1
2	FBCDQS<2>	E13	FBCDQS_WP2
3	FBCDQS<3>	A25	FBCDQS_WP3
4	FBCDQS<4>	A26	FBCDQS_WP4
5	FBCDQS<5>	D30	FBCDQS_WP5
6	FBCDQS<6>	E26	FBCDQS_WP6
7	FBCDQS<7>	A32	FBCDQS_WP7

FBC_CMD0	F18	FBC_CMD<0>	0
FBC_CMD1	H20	FBC_CMD<1>	1
FBC_CMD2	E18	FBC_CMD<2>	2
FBC_CMD3	E20	FBC_CMD<3>	3
FBC_CMD4	D23	FBC_CMD<4>	4
FBC_CMD5	G24	FBC_CMD<5>	5
FBC_CMD6	D24	FBC_CMD<6>	6
FBC_CMD7	G23	FBC_CMD<7>	7
FBC_CMD8	D20	FBC_CMD<8>	8
FBC_CMD9	E22	FBC_CMD<9>	9
FBC_CMD10	J21	FBC_CMD<10>	10
FBC_CMD11	E21	FBC_CMD<11>	11
FBC_CMD12	G20	TP_FBC_CMD12	
FBC_CMD13	F22	FBC_CMD<13>	13
FBC_CMD14	H21	FBC_CMD<14>	14
FBC_CMD15	E17	FBC_CMD<15>	15
FBC_CMD16	E19	FBC_CMD<16>	16
FBC_CMD17	D21	FBC_CMD<17>	17
FBC_CMD18	E23	FBC_CMD<18>	18
FBC_CMD19	F19	FBC_CMD<19>	19
FBC_CMD20	E24	FBC_CMD<20>	20
FBC_CMD21	G21	FBC_CMD<21>	21
FBC_CMD22	G19	FBC_CMD<22>	22
FBC_CMD23	G25	FBC_CMD<23>	23
FBC_CMD24	G18	FBC_CMD<24>	24
FBC_CMD25	G22	FBC_CMD<25>	25
FBC_CMD26	G17	TP_FBC_CMD_26	

FBC_CMD<0..26> OUT 9<

FBC_CLK0	H17	FBC_CLK0	
FBC_CLK0	J16	FBC_CLK0*	OUT 9<
FBC_CLK1	J24	FBC_CLK1	OUT 9<
FBC_CLK1	H23	FBC_CLK1*	OUT 9<

144BGA CMD_Mapping

CMD	ADDR
CMD0	A<3>
CMD1	A<0>
CMD2	A<2>
CMD3	A<1>
CMD4	A<3>
CMD5	A<4>
CMD6	A<5>
CMD7	CS1* *not used
CMD8	CS0*
CMD9	WE*
CMD10	BA0
CMD11	CKE
CMD12	RESET
CMD13	A<2>
CMD14	A<12>
CMD15	RAS*
CMD16	A<11>
CMD17	A<10
CMD18	BA1
CMD19	A<8>
CMD20	A<9>
CMD21	A<6>
CMD22	A<5>
CMD23	A<7>
CMD24	A<4>
CMD25	CAS*
CMD26	A<13> *not used

RFU	H24	SNN_FBC_RFU0	
RFU	J25	SNN_FBC_RFU1	
FBC_DEBUG	H16	TP_FBC_DEBUG	
FBC_REFCLK	F15	FBC_REFCLK	
FBC_REFCLK	G15	FBC_REFCLK*	

If Refclk is not used
Stuff 10K to GND

R613 10K 5% 0402 NO STUFF
R614 10K 5% 0402 NO STUFF
GND

FBC_PLLVDD	H13	FBC_PLLVDD	12MIL
FBC_PLLAVDD	J12	FBCD_PLLAVDD	10MIL
FBC_PLLGND	J13		

LB505 150-220R@100MHz BEAD_0603 COMMON A3V3
LB506 150-220R@100MHz BEAD_0603 COMMON NVVDD

C935	.01UF	16V	10% X7R 0402 COMMON
C934	.1UF	10V	10% X5R 0402 COMMON
C920	4.7UF	6.3V	20% X5R 0603 COMMON
C860	4.7UF	6.3V	20% X5R 0603 COMMON
C942	.01UF	16V	10% X7R 0402 COMMON
C960	.1UF	10V	10% X5R 0402 COMMON
C957	4.7UF	6.3V	20% X5R 0603 COMMON
C939	4.7UF	6.3V	20% X5R 0603 COMMON

GND

U12
NV41-A2
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5/24 MEM_D

11<>	BI	FBDD<63..0>	
11<>	OUT	FBDDQM<7..0>	
11<>	BI	FBDDQS<7..0>	

0	FBDD<0>	H3	FBDD0
1	FBDD<1>	J3	FBDD1
2	FBDD<2>	J1	FBDD2
3	FBDD<3>	J2	FBDD3
4	FBDD<4>	M3	FBDD4
5	FBDD<5>	K3	FBDD5
6	FBDD<6>	L3	FBDD6
7	FBDD<7>	M1	FBDD7
8	FBDD<8>	H1	FBDD8
9	FBDD<9>	G3	FBDD9
10	FBDD<10>	G1	FBDD10
11	FBDD<11>	G2	FBDD11
12	FBDD<12>	F3	FBDD12
13	FBDD<13>	E1	FBDD13
14	FBDD<14>	D1	FBDD14
15	FBDD<15>	D2	FBDD15
16	FBDD<16>	P4	FBDD16
17	FBDD<17>	N7	FBDD17
18	FBDD<18>	M7	FBDD18
19	FBDD<19>	N5	FBDD19
20	FBDD<20>	P5	FBDD20
21	FBDD<21>	R7	FBDD21
22	FBDD<22>	T7	FBDD22
23	FBDD<23>	P7	FBDD23
24	FBDD<24>	C1	FBDD24
25	FBDD<25>	C5	FBDD25
26	FBDD<26>	C2	FBDD26
27	FBDD<27>	B4	FBDD27
28	FBDD<28>	A3	FBDD28
29	FBDD<29>	B3	FBDD29
30	FBDD<30>	C4	FBDD30
31	FBDD<31>	C3	FBDD31
32	FBDD<32>	A6	FBDD32
33	FBDD<33>	C6	FBDD33
34	FBDD<34>	C7	FBDD34
35	FBDD<35>	A7	FBDD35
36	FBDD<36>	C8	FBDD36
37	FBDD<37>	C9	FBDD37
38	FBDD<38>	A9	FBDD38
39	FBDD<39>	B9	FBDD39
40	FBDD<40>	E12	FBDD40
41	FBDD<41>	E9	FBDD41
42	FBDD<42>	F9	FBDD42
43	FBDD<43>	G10	FBDD43
44	FBDD<44>	D10	FBDD44
45	FBDD<45>	G12	FBDD45
46	FBDD<46>	F12	FBDD46
47	FBDD<47>	D11	FBDD47
48	FBDD<48>	F4	FBDD48
49	FBDD<49>	E4	FBDD49
50	FBDD<50>	D4	FBDD50
51	FBDD<51>	D5	FBDD51
52	FBDD<52>	D8	FBDD52
53	FBDD<53>	E7	FBDD53
54	FBDD<54>	D7	FBDD54
55	FBDD<55>	D9	FBDD55
56	FBDD<56>	B13	FBDD56
57	FBDD<57>	C11	FBDD57
58	FBDD<58>	A13	FBDD58
59	FBDD<59>	C13	FBDD59
60	FBDD<60>	A11	FBDD60
61	FBDD<61>	A10	FBDD61
62	FBDD<62>	B10	FBDD62
63	FBDD<63>	C10	FBDD63

0	FBDDQM<0>	K2	FBDDQM0
1	FBDDQM<1>	E3	FBDDQM1
2	FBDDQM<2>	N4	FBDDQM2
3	FBDDQM<3>	D3	FBDDQM3
4	FBDDQM<4>	B7	FBDDQM4
5	FBDDQM<5>	G11	FBDDQM5
6	FBDDQM<6>	F5	FBDDQM6
7	FBDDQM<7>	C12	FBDDQM7

	TP_FBDDQS0*	K1	FBDDQS_RN0
	TP_FBDDQS1*	F2	FBDDQS_RN1
	TP_FBDDQS2*	R6	FBDDQS_RN2
	TP_FBDDQS3*	A4	FBDDQS_RN3
	TP_FBDDQS4*	B6	FBDDQS_RN4
	TP_FBDDQS5*	E10	FBDDQS_RN5
	TP_FBDDQS6*	E6	FBDDQS_RN6
	TP_FBDDQS7*	A12	FBDDQS_RN7

0	FBDDQS<0>	L1	FBDDQS_WP0
1	FBDDQS<1>	F1	FBDDQS_WP1
2	FBDDQS<2>	R5	FBDDQS_WP2
3	FBDDQS<3>	A5	FBDDQS_WP3
4	FBDDQS<4>	A6	FBDDQS_WP4
5	FBDDQS<5>	E11	FBDDQS_WP5
6	FBDDQS<6>	D6	FBDDQS_WP6
7	FBDDQS<7>	B12	FBDDQS_WP7

FBD_CMD0	M6	FBD_CMD<0>	0
FBD_CMD1	G5	FBD_CMD<1>	1
FBD_CMD2	L7	FBD_CMD<2>	2
FBD_CMD3	K5	FBD_CMD<3>	3
FBD_CMD4	J10	FBD_CMD<4>	4
FBD_CMD5	G8	FBD_CMD<5>	5
FBD_CMD6	F8	FBD_CMD<6>	6
FBD_CMD7	G6	FBD_CMD<7>	7
FBD_CMD8	H6	FBD_CMD<8>	8
FBD_CMD9	F6	FBD_CMD<9>	9
FBD_CMD10	K8	FBD_CMD<10>	10
FBD_CMD11	L5	FBD_CMD<11>	11
FBD_CMD12	H4	TP_FBD_CMD12	
FBD_CMD13	G4	FBD_CMD<13>	13
FBD_CMD14	K9	FBD_CMD<14>	14
FBD_CMD15	L4	FBD_CMD<15>	15
FBD_CMD16	K4	FBD_CMD<16>	16
FBD_CMD17	K7	FBD_CMD<17>	17
FBD_CMD18	G7	FBD_CMD<18>	18
FBD_CMD19	J4	FBD_CMD<19>	19
FBD_CMD20	F7	FBD_CMD<20>	20
FBD_CMD21	J5	FBD_CMD<21>	21
FBD_CMD22	J6	FBD_CMD<22>	22
FBD_CMD23	H7	FBD_CMD<23>	23
FBD_CMD24	L8	FBD_CMD<24>	24
FBD_CMD25	J7	FBD_CMD<25>	25
FBD_CMD26	M5	TP_FBD_CMD_26	

FBD_CMD<0..26> OUT 11<

FBD_CLK0	L9	FBD_CLK0	
FBD_CLK0	M9	FBD_CLK0*	OUT 11<
FBD_CLK1	J9	FBD_CLK1	OUT 11<
FBD_CLK1	J8	FBD_CLK1*	OUT 11<

RFU	H10	SNN_FBD_RFU0	
RFU	L11	SNN_FBD_RFU1	
FBD_DEBUG	N8	TP_FBD_DEBUG	
FBD_REFCLK	G9	FBD_REFCLK	
FBD_REFCLK	H9	FBD_REFCLK*	

If Refclk is not used
Stuff 10K to GND

R622 10K 5% 0402 NO STUFF
R621 10K 5% 0402 NO STUFF
GND

FBD_PLLVDD	H11	FBD_PLLVDD	12MIL
FBD_PLLAVDD	J11	FBCD_PLLAVDD	
FBD_PLLGND	H12		

LB507 150-220R@100MHz BEAD_0603 COMMON A3V3

C966	.01UF	16V	10% X7R 0402 COMMON
C965	.1UF	10V	10% X5R 0402 COMMON
C973	4.7UF	6.3V	20% X5R 0603 COMMON
C987	4.7UF	6.3V	20% X5R 0603 COMMON

GND

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	MEMORY: GPU Partition C/D

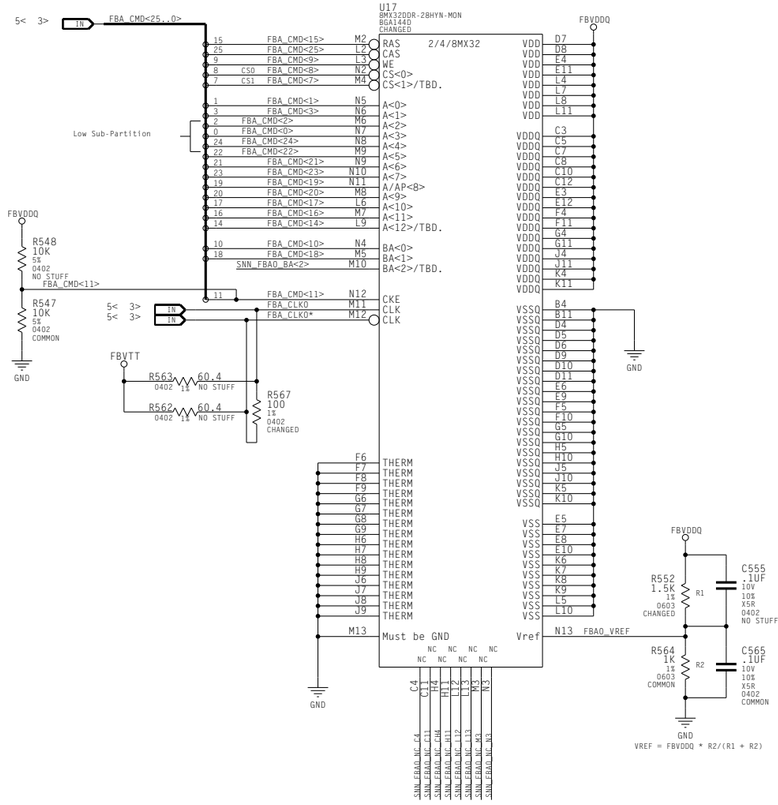
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	4 OF 37
NAME	JLAM	DATE	19-AUG-2004

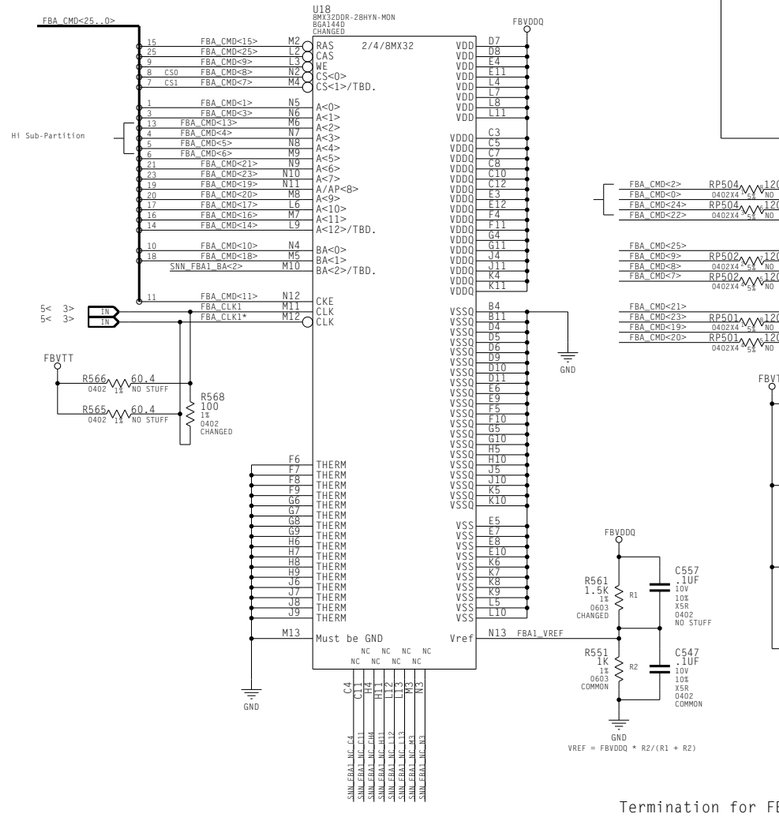
5 FrameBuffer: Partition A 4Mx32 BGA144 DDR1

144BGA CMD Mapping	
CMD	ADDR
CMD15	RAS*
CMD25	CAS*
CMD9	WE*
CMD11	CKE
CMD12	RESET *not used
CMD8	CS0*
CMD7	CS1* *8Mx32 stacked die
CMD1	A<0>
CMD3	A<1>
CMD2	A<2>
CMD0	A<3> — Low Sub-Partition
CMD24	A<4>
CMD22	A<5>
CMD13	A<2>
CMD4	A<3> — H1 Sub-Partition
CMD5	A<4>
CMD6	A<5>
CMD21	A<6>
CMD23	A<7>
CMD19	A<8>
CMD20	A<9>
CMD17	A<10>
CMD16	A<11>
CMD14	A<12>
CMD10	BA0
CMD18	BA1

A-CSO-LOW-32bit



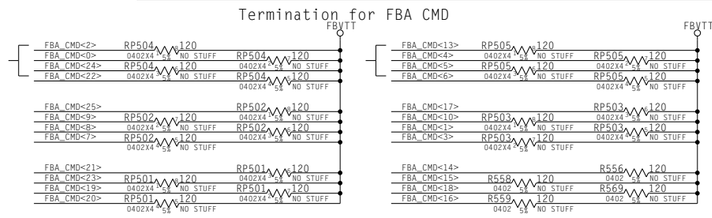
A-CSO-HI-32bit



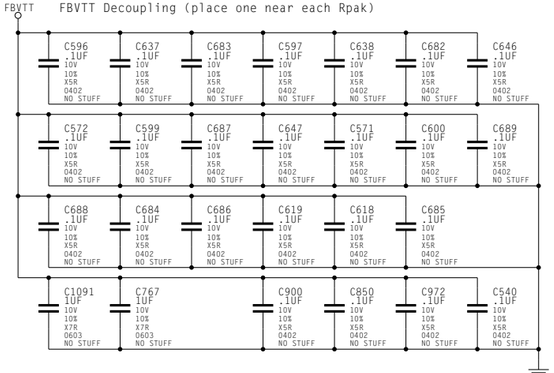
NET RULES

NET	DIFFPAIR	SPACING
FBA_CLK0	FBA_CLK0	10MIL_G2G_20MIL
FBA_CLK0*	FBA_CLK0	10MIL_G2G_20MIL
FBA_CLK1	FBA_CLK1	10MIL_G2G_20MIL
FBA_CLK1*	FBA_CLK1	10MIL_G2G_20MIL
FBA_CMD<25..0>		10MIL
FBA0<63..0>		10MIL
FBADQM<7..0>		10MIL
FBADQS<7..0>		10MIL

Termination for FBA CMD

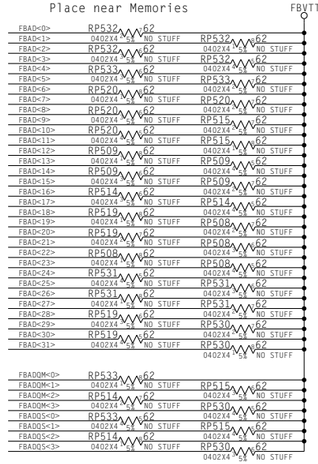


FBVTT Decoupling (place one near each Rpak)



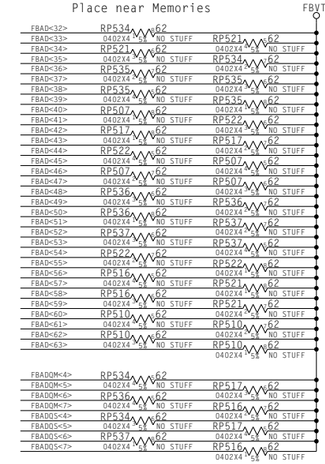
Termination for FBA 0..31

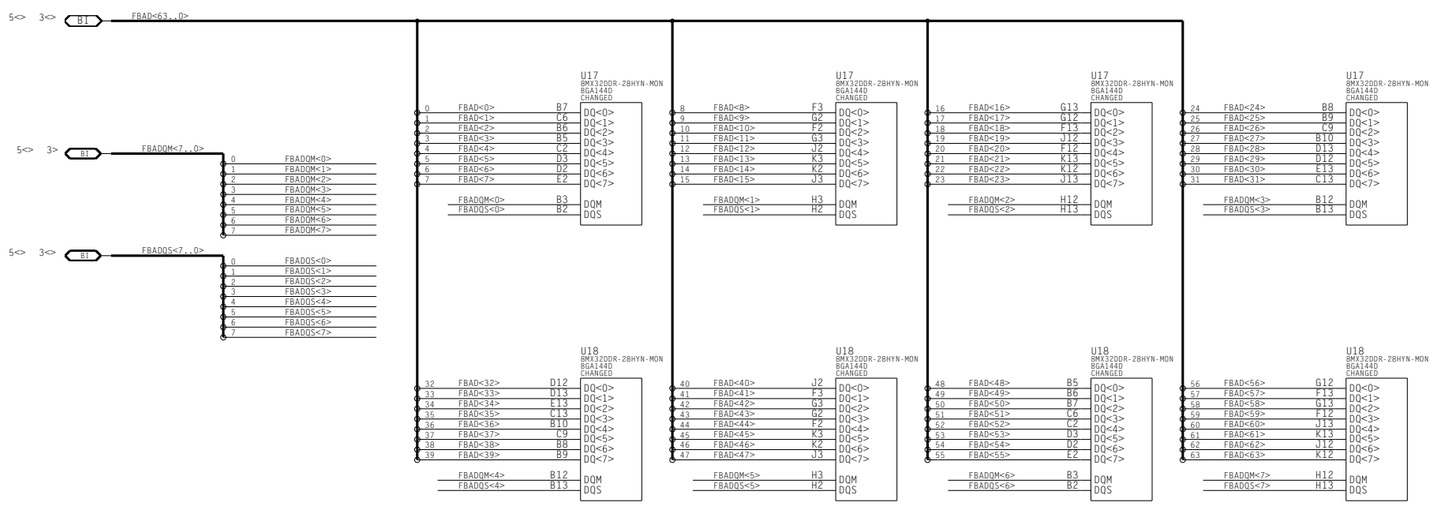
Place near Memories



Termination for FBA 32..63

Place near Memories





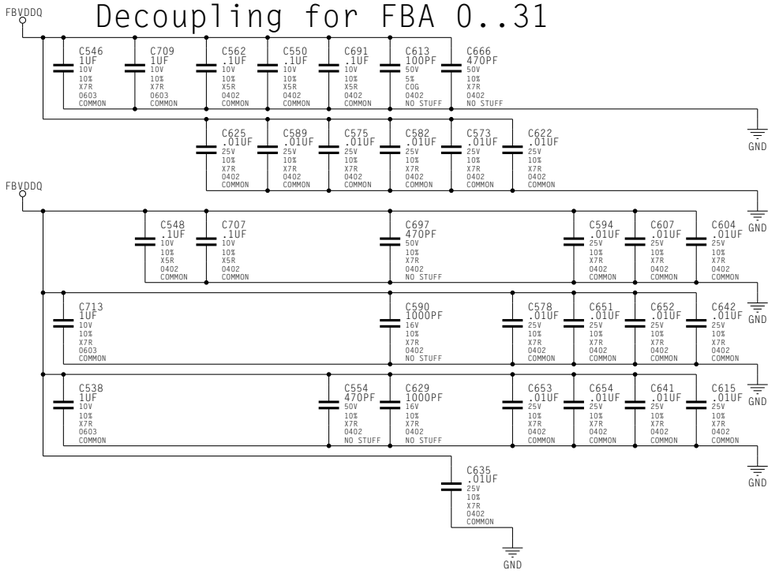
ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	FrameBuffer: Partition A 4Mx32 BGA144 DDR1

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

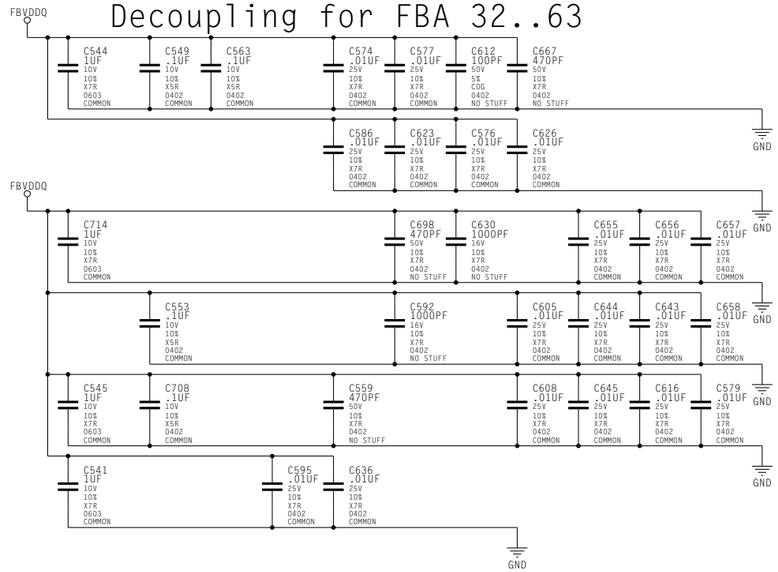
NV_PN	600-10260-0004-300		
ID	design	PAGE	5 OF 37
NAME	JLAM	DATE	19-AUG-2004

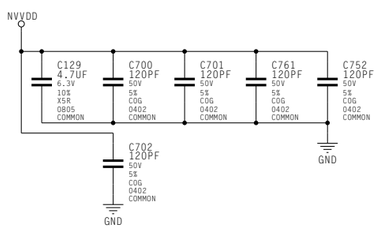
6 FrameBuffer: Partition A Decoupling

Decoupling for FBA 0..31



Decoupling for FBA 32..63





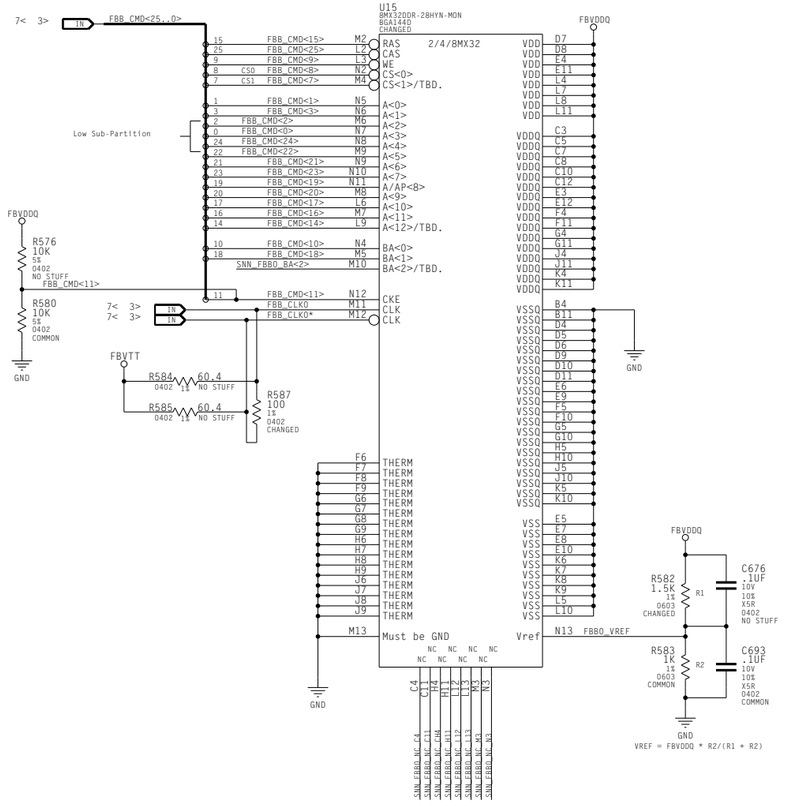
ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	FrameBuffer: Partition A Decoupling

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

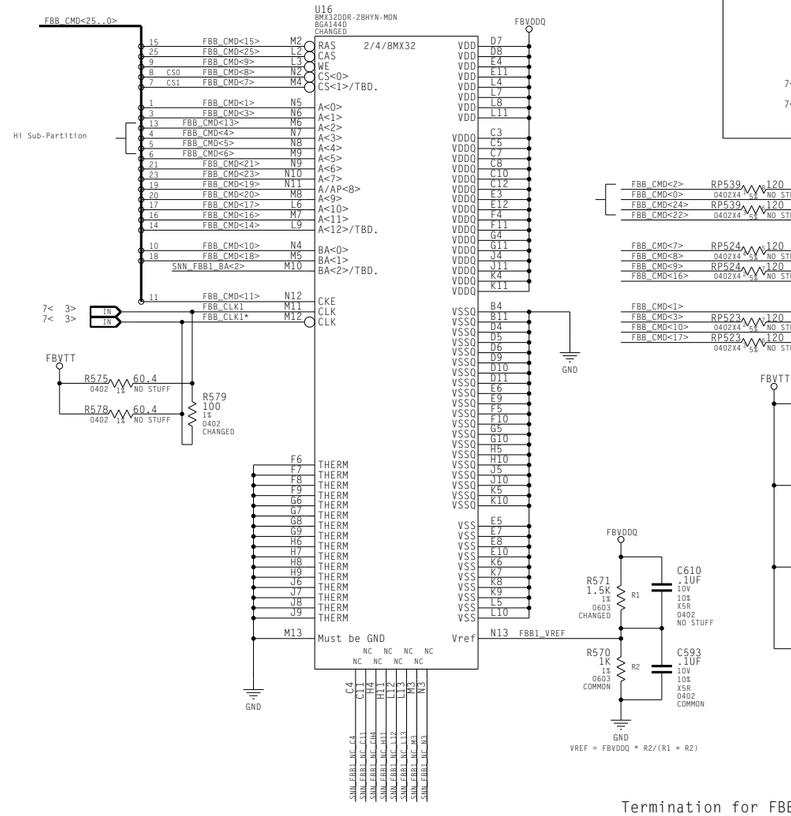
NV_PN	600-10260-0004-300		
ID	design	PAGE	6 OF 37
NAME	JLAM	DATE	19-AUG-2004

7 FrameBuffer: Partition B 4Mx32 BGA144 DDR1

A-CSO-LOW-32bit



A-CSO-HI-32bit

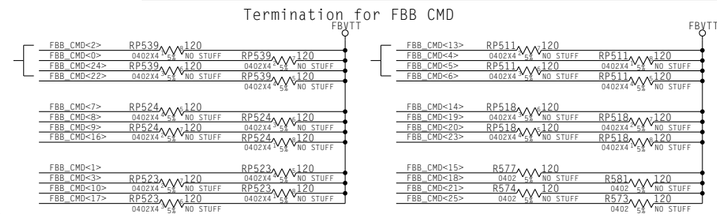


144BGA CMD Mapping	
CMD	ADDR
CMD15	RAS*
CMD25	CAS*
CMD9	WE*
CMD11	CKE
CMD12	RESET *not used
CMD8	CS0*
CMD7	CS1* *8Mx32 stacked die
CMD1	A<0>
CMD3	A<1>
CMD2	A<2> — Low Sub-Partition
CMD0	A<3> — Low Sub-Partition
CMD24	A<4> — Low Sub-Partition
CMD22	A<5> — Low Sub-Partition
CMD13	A<2> — Hi Sub-Partition
CMD4	A<3> — Hi Sub-Partition
CMD5	A<4> — Hi Sub-Partition
CMD6	A<5> — Hi Sub-Partition
CMD21	A<6>
CMD23	A<7>
CMD19	A<8>
CMD20	A<9>
CMD17	A<10>
CMD16	A<11>
CMD14	A<12>
CMD10	BA0
CMD18	BA1

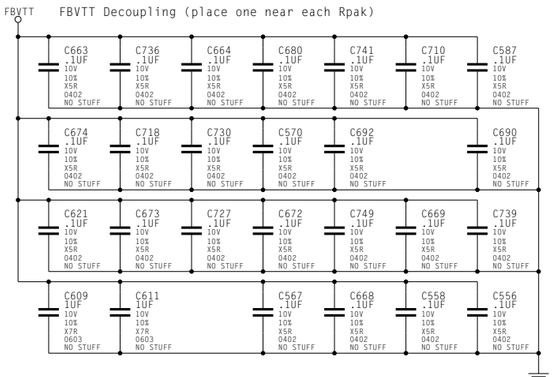
NET RULES

NET	DIFFPAIR	SPACING
FBB_CLK0	FBB_CLK0	10MIL_G2G_20MIL
FBB_CLK0*	FBB_CLK0	10MIL_G2G_20MIL
FBB_CLK1	FBB_CLK1	10MIL_G2G_20MIL
FBB_CLK1*	FBB_CLK1	10MIL_G2G_20MIL
FBB_CMD<25..0>		10MIL
FBBD<63..0>		10MIL
FBBDQM<7..0>		10MIL
FBBDQS<7..0>		10MIL

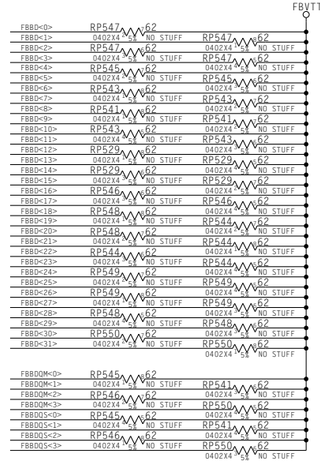
Termination for FBB CMD



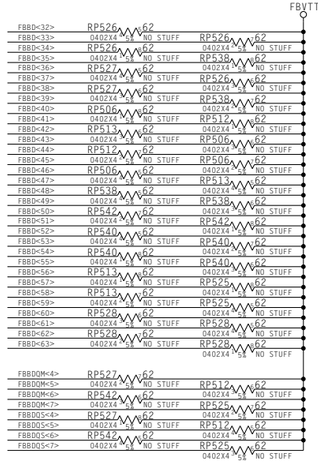
FBVTT Decoupling (place one near each Rpak)

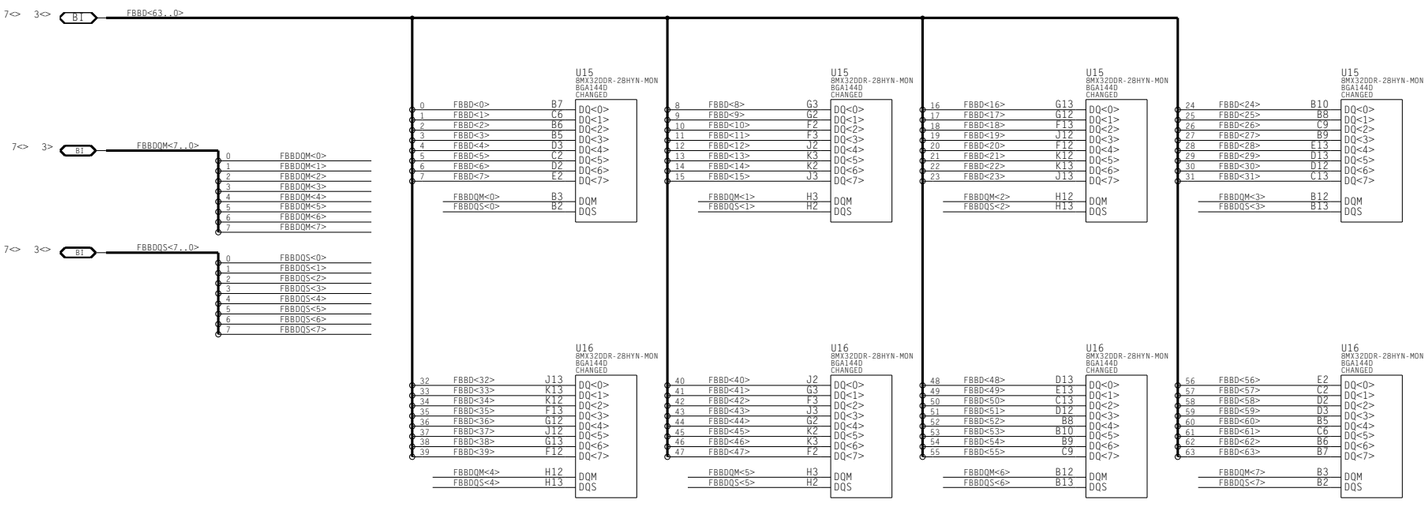


Termination for FBB 0..31



Termination for FBB 32..63





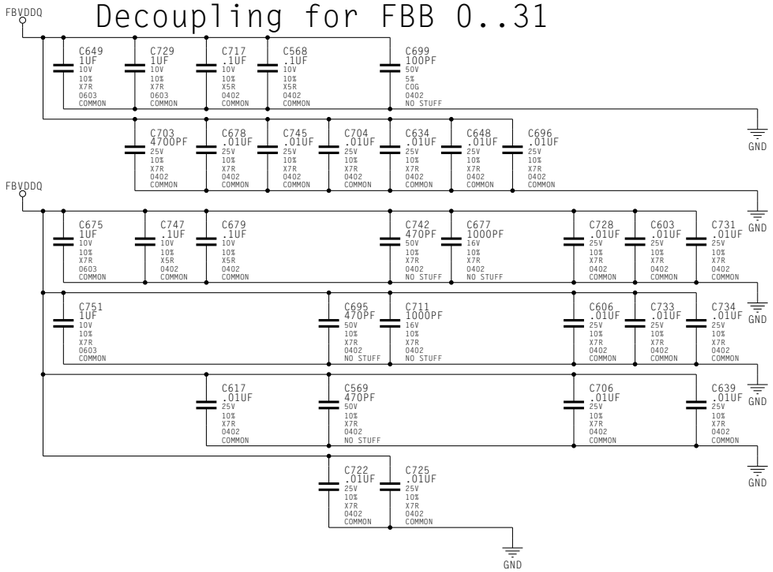
ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	FrameBuffer: Partition B 4Mx32 BGA144 DDR1

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

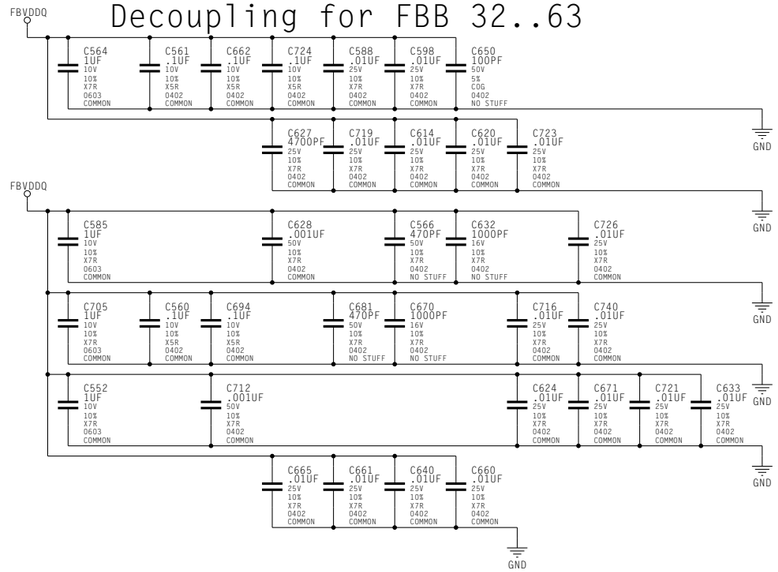
NV_PN	600-10260-0004-300		
ID	design	PAGE	7 OF 37
NAME	JLAM	DATE	19-AUG-2004

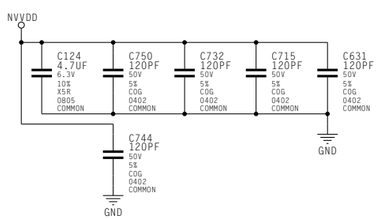
8 FrameBuffer: Partition B Decoupling

Decoupling for FBB 0..31



Decoupling for FBB 32..63





ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	FrameBuffer: Partition B Decoupling

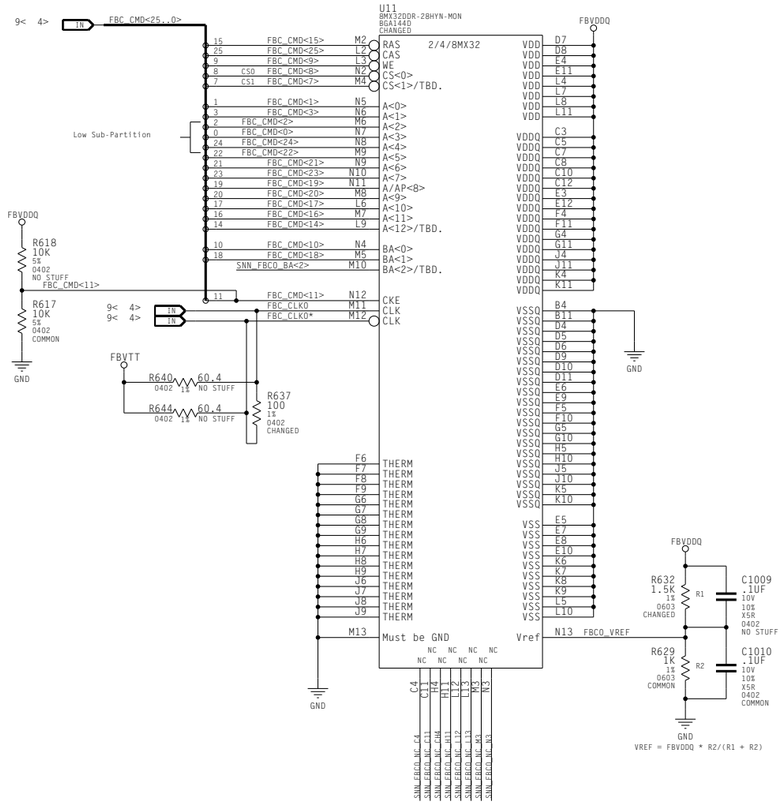
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	8 OF 37
NAME	JLAM	DATE	19-AUG-2004

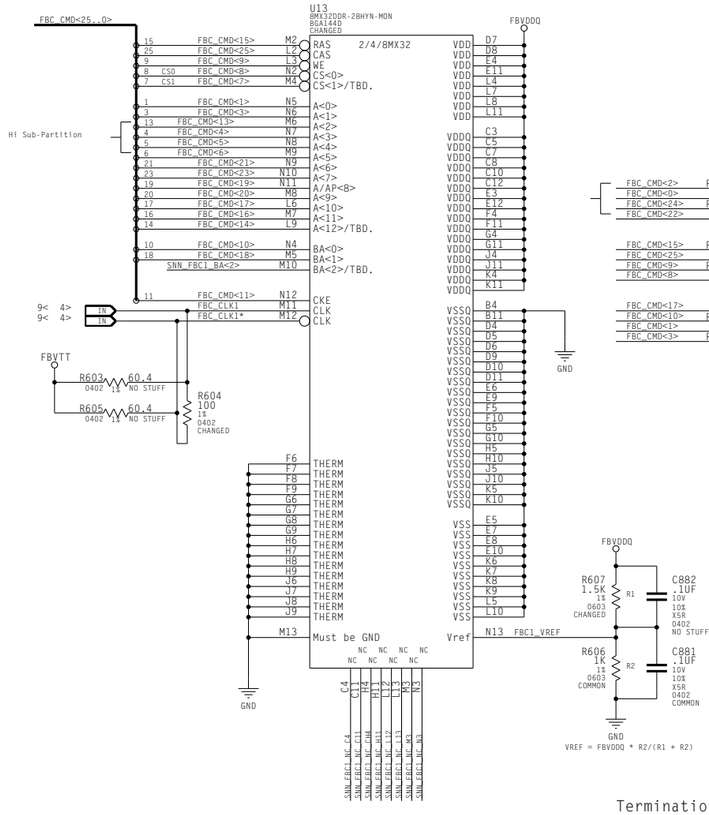
9 FrameBuffer: Partition C 4Mx32 BGA144 DDR1

144BGA CMD Mapping	
CMD	ADDR
CMD15	RAS*
CMD25	CAS*
CMD9	WE*
CMD11	CKE
CMD12	RESET *not used
CMD8	CS0*
CMD7	CS1* *8Mx32 stacked die
CMD1	A<0>
CMD3	A<1>
CMD2	A<2>
CMD0	A<3> — Low Sub-Partition
CMD24	A<4>
CMD22	A<5>
CMD13	A<2>
CMD4	A<3> — Hi Sub-Partition
CMD5	A<4>
CMD6	A<5>
CMD21	A<6>
CMD23	A<7>
CMD19	A<8>
CMD20	A<9>
CMD17	A<10>
CMD16	A<11>
CMD14	A<12>
CMD10	BA0
CMD18	BA1

A-CSO-LOW-32bit



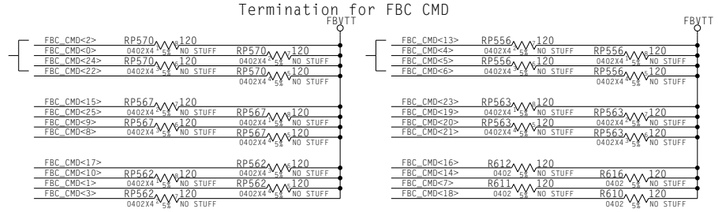
A-CSO-HI-32bit



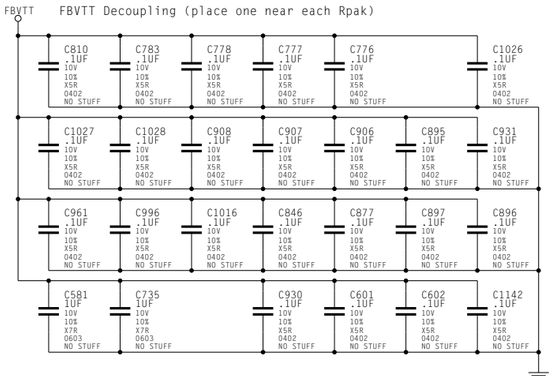
NET RULES

NET	DIFFPAIR	SPACING
FBC_CLKO	FBC_CLKO	10MIL_G2G_20MIL
FBC_CLKO*	FBC_CLKO	10MIL_G2G_20MIL
FBC_CLK1	FBC_CLK1	10MIL_G2G_20MIL
FBC_CLK1*	FBC_CLK1	10MIL_G2G_20MIL
FBC_CMD<25..0>		10MIL
FBCD<63..0>		10MIL
FBCDQM<7..0>		10MIL
FBCDQS<7..0>		10MIL

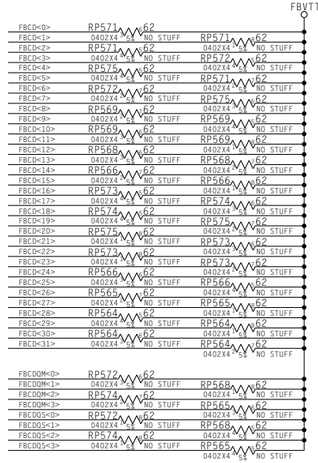
Termination for FBC CMD



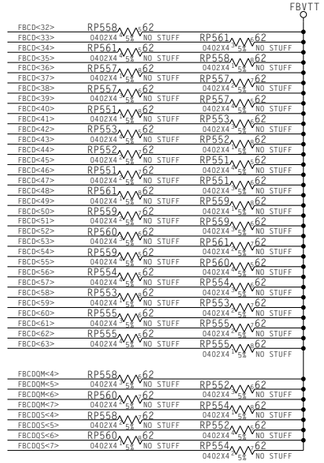
FBVTT Decoupling (place one near each Rpak)

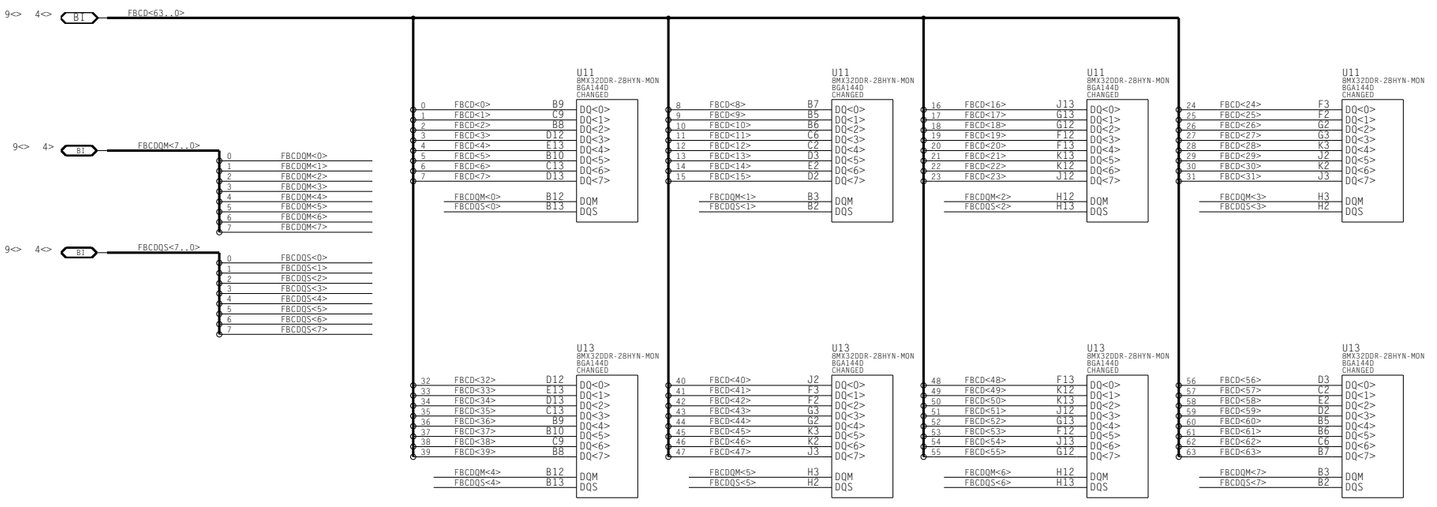


Termination for FBC 0..31



Termination for FBC 32..63





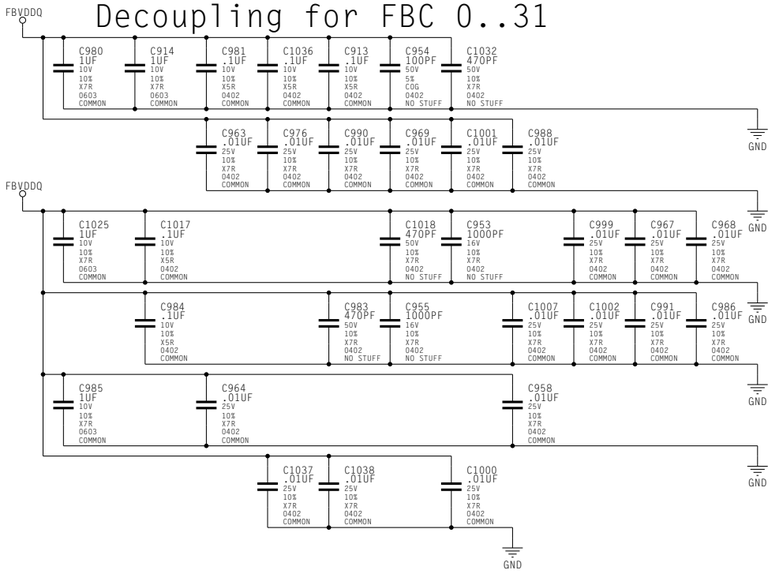
ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	FrameBuffer: Partition C 4Mx32 BGA144 DDR1

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

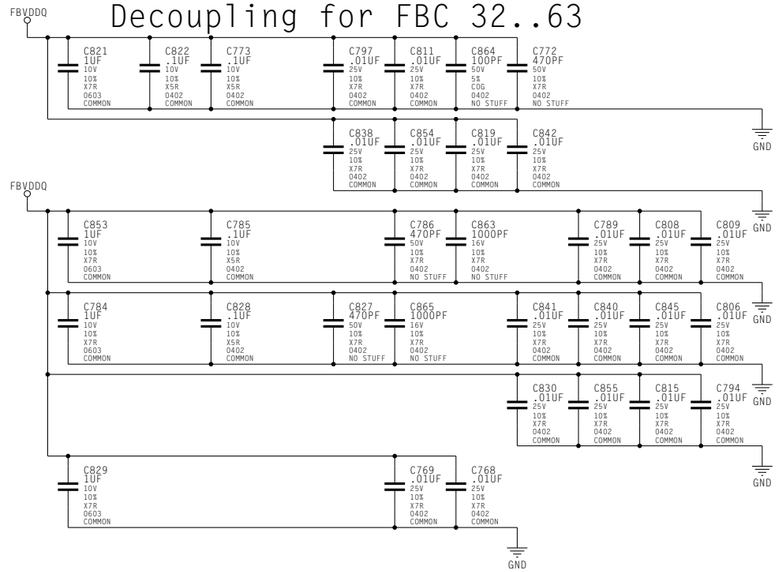
NV_PN	600-10260-0004-300		
ID	design	PAGE	9 OF 37
NAME	JLAM	DATE	19-AUG-2004

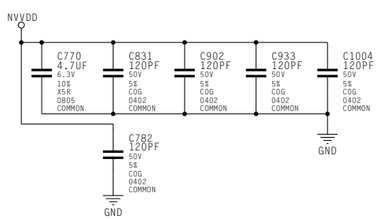
10 FrameBuffer: Partition C Decoupling

Decoupling for FBC 0..31



Decoupling for FBC 32..63





ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	FrameBuffer: Partition C Decoupling

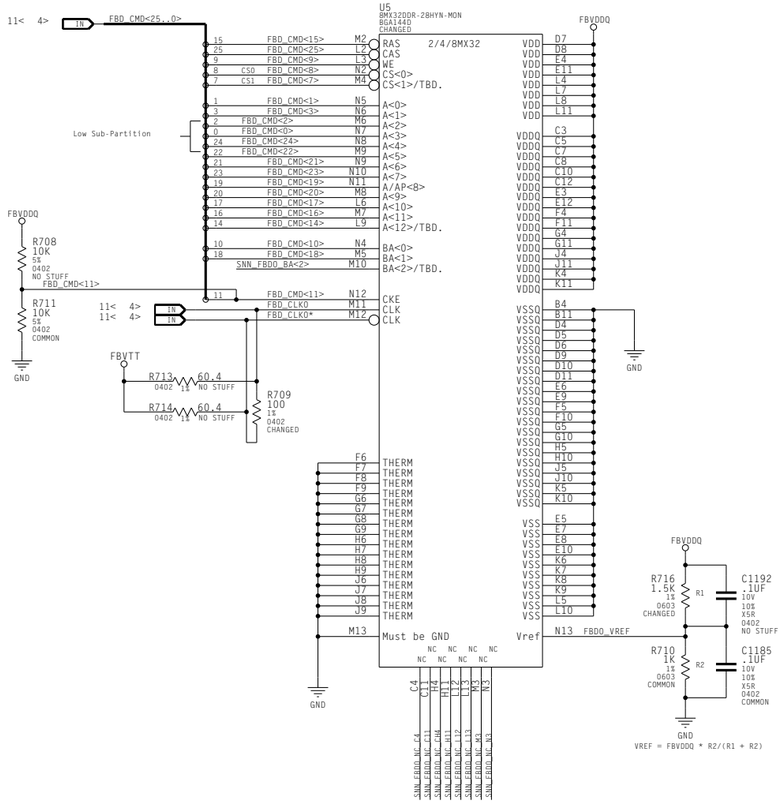
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	10 OF 37
NAME	JLAM	DATE	19-AUG-2004

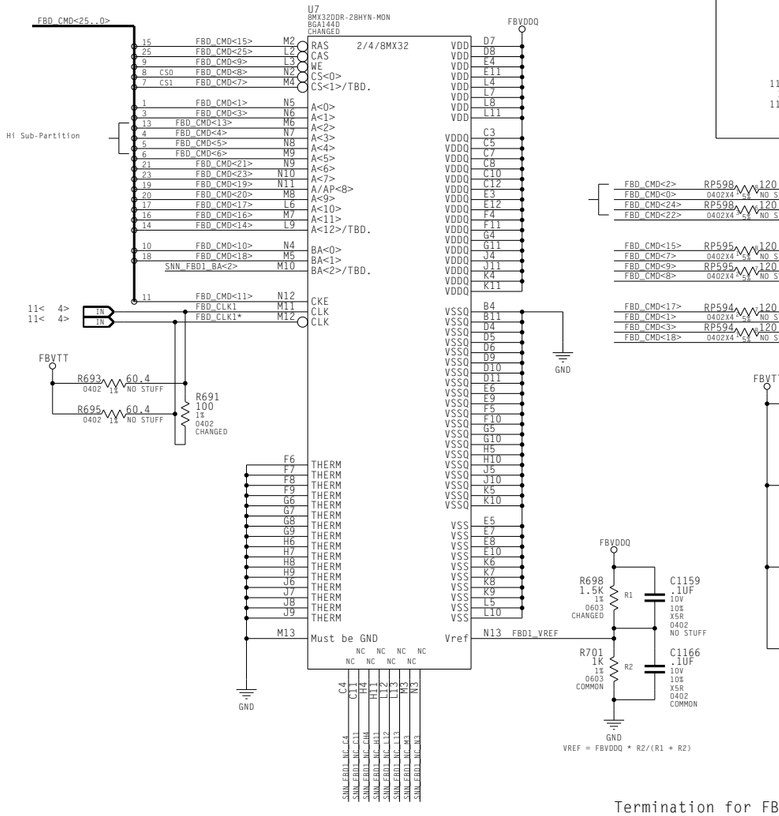
5 FrameBuffer: Partition D 4Mx32 BGA144 DDR1

144BGA CMD Mapping	
CMD	ADDR
CMD15	RAS*
CMD25	CAS*
CMD9	WE*
CMD11	CKE
CMD12	RESET *not used
CMD8	CS0*
CMD7	CS1* *8Mx32 stacked die
CMD1	A<0>
CMD3	A<1>
CMD2	A<2> — Low Sub-Partition
CMD0	A<3> — Low Sub-Partition
CMD24	A<4> — Low Sub-Partition
CMD22	A<5> — Low Sub-Partition
CMD13	A<2> — Hi Sub-Partition
CMD4	A<3> — Hi Sub-Partition
CMD5	A<4> — Hi Sub-Partition
CMD6	A<5> — Hi Sub-Partition
CMD21	A<6>
CMD23	A<7>
CMD19	A<8>
CMD20	A<9>
CMD17	A<10>
CMD16	A<11>
CMD14	A<12>
CMD10	BA0
CMD18	BA1

A-CSO-LOW-32bit



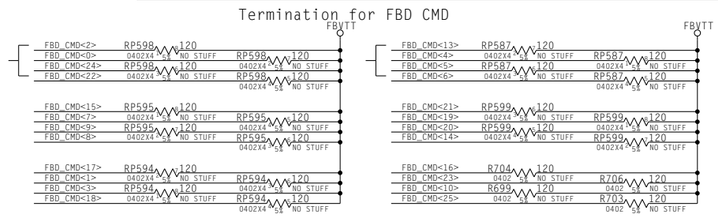
A-CSO-HI-32bit



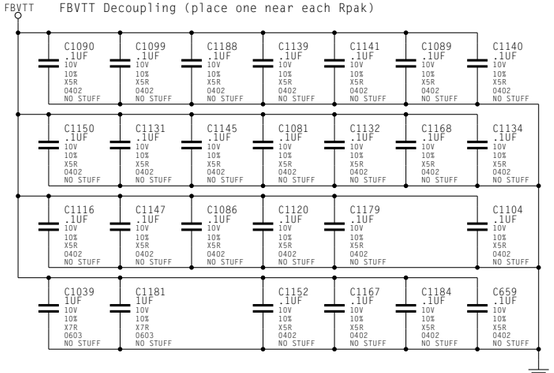
NET RULES

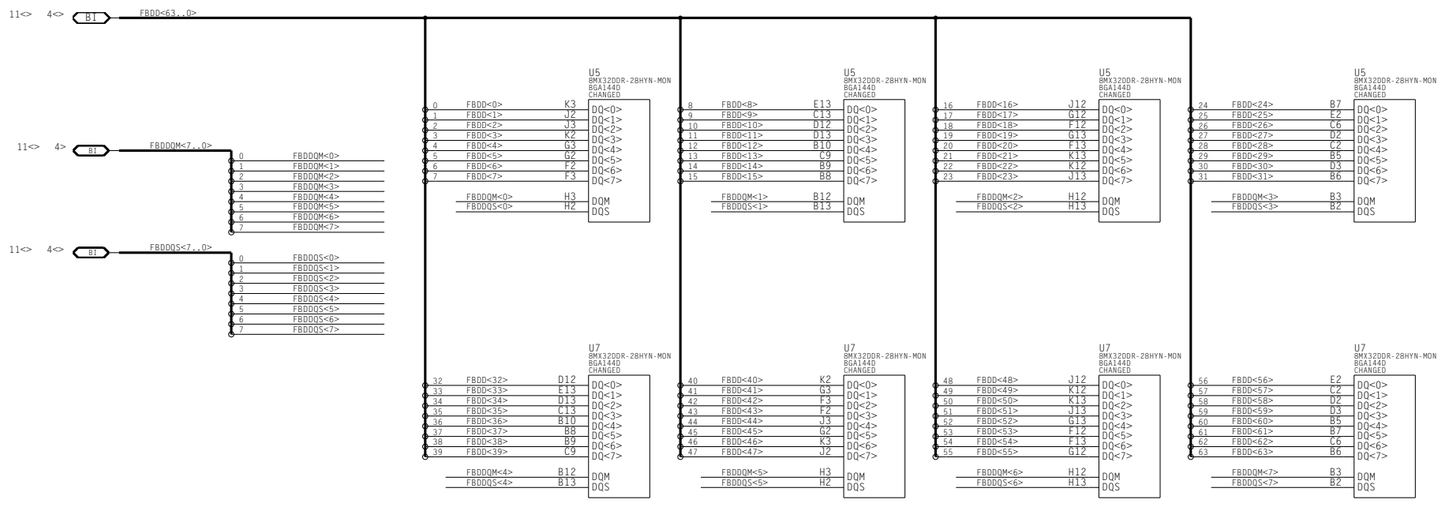
	NET	DIFFPAIR	SPACING
11< 4> IN	FBD_CLK0	FBD_CLK0	10MIL_G2G_20MIL
11< 4> IN	FBD_CLK0*	FBD_CLK0	10MIL_G2G_20MIL
11< 4> IN	FBD_CLK1	FBD_CLK1	10MIL_G2G_20MIL
11< 4> IN	FBD_CLK1*	FBD_CLK1	10MIL_G2G_20MIL
11< 4> IN	FBD_CMD<25..0>		10MIL
11<> 4<> BI	FBDD<63..0>		10MIL
11<> 4> BI	FBDDQM<7..0>		10MIL
11<> 4<> BI	FBDDQS<7..0>		10MIL

Termination for FBD CMD

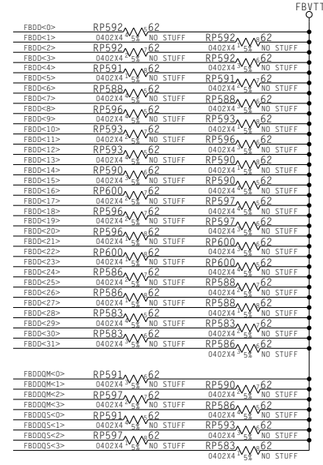


FBVTT Decoupling (place one near each Rpak)

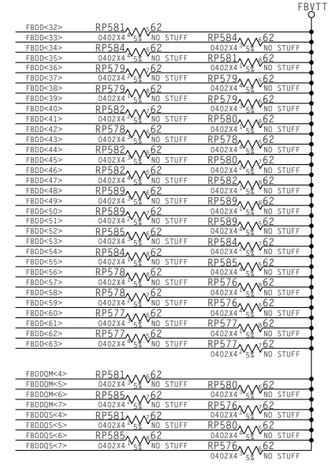




Termination for FBD 0..31



Termination for FBD 32..63



ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	FrameBuffer: Partition D 4Mx32 BGA144 DDR1

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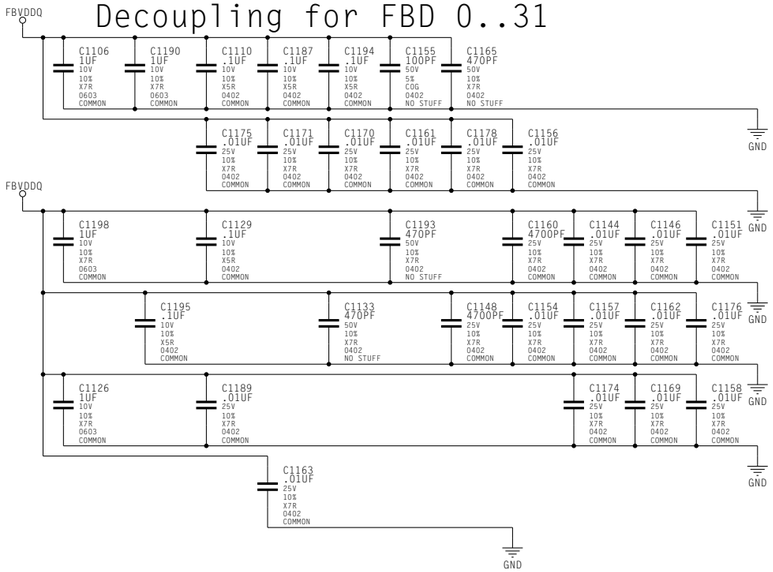
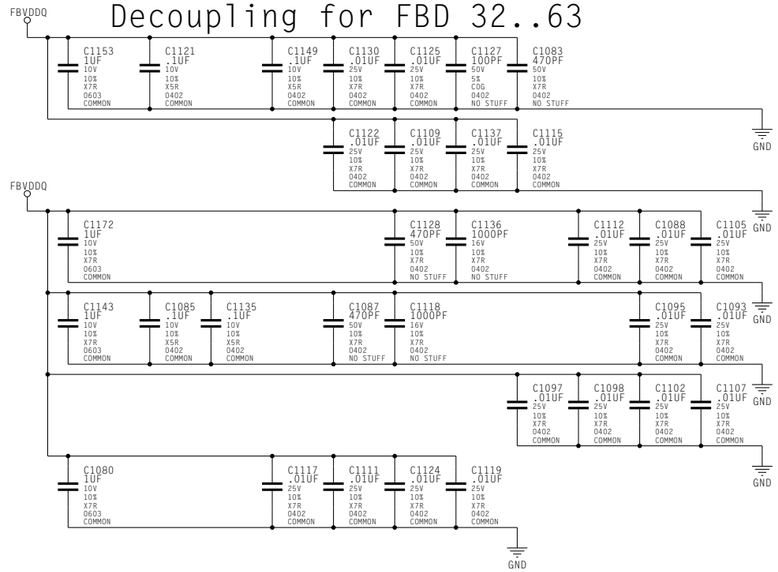
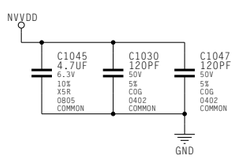
12 FrameBuffer: Partition D Decoupling

Decoupling for FBD 0..31



Decoupling for FBD 32..63





ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	FrameBuffer: Partition D Decoupling

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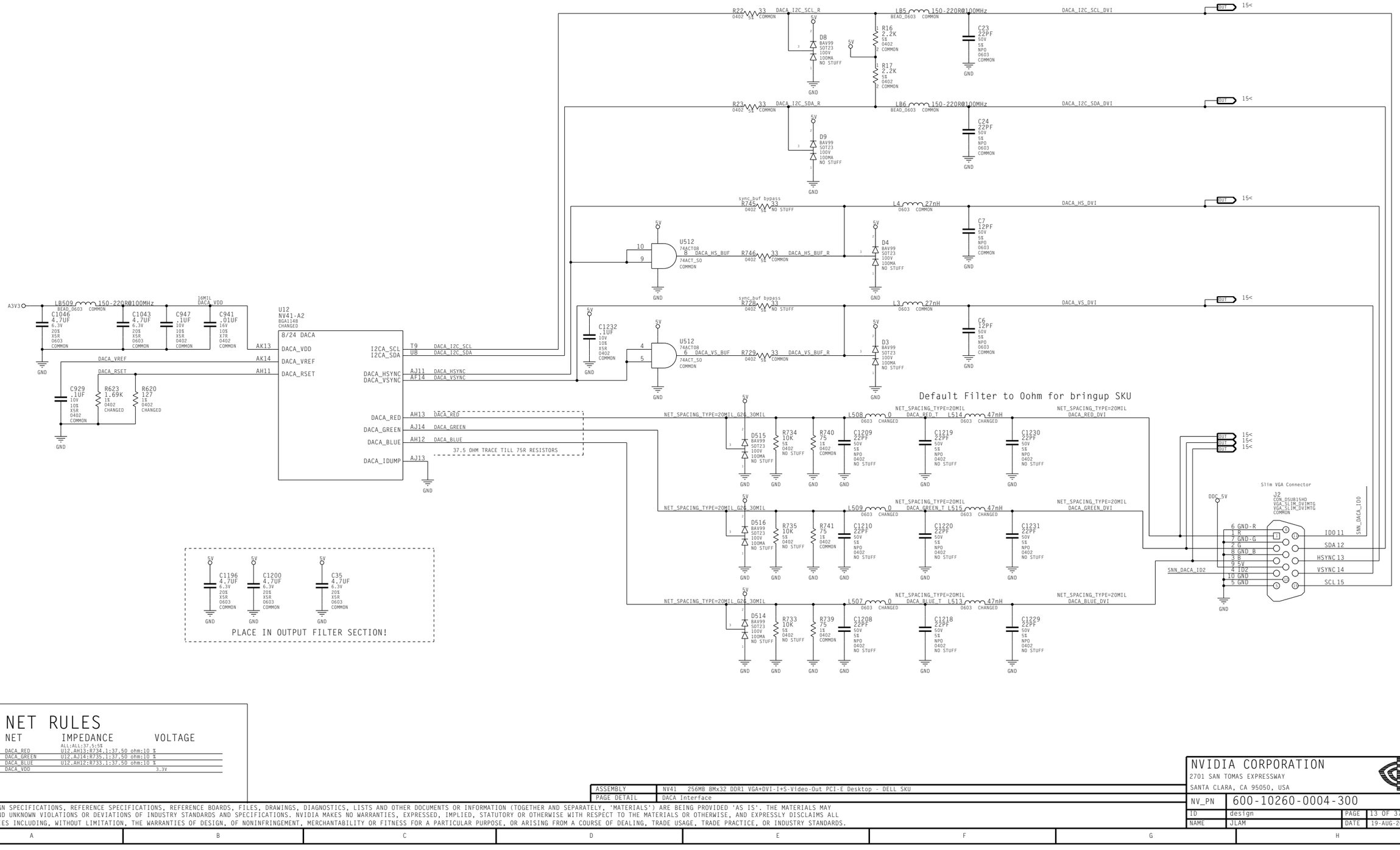
13 DACA Interface



NET RULES

	NET	IMPEDANCE	VOLTAGE
		ALL:ALL:37.5:5%	
IN	DACA_RED	U12.AH13:R734.1:37.50 ohm:10 %	
IN	DACA_GREEN	U12.AJ14:R735.1:37.50 ohm:10 %	
IN	DACA_BLUE	U12.AH12:R733.1:37.50 ohm:10 %	
IN	DACA_VDD		3.3V

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	DACA Interface

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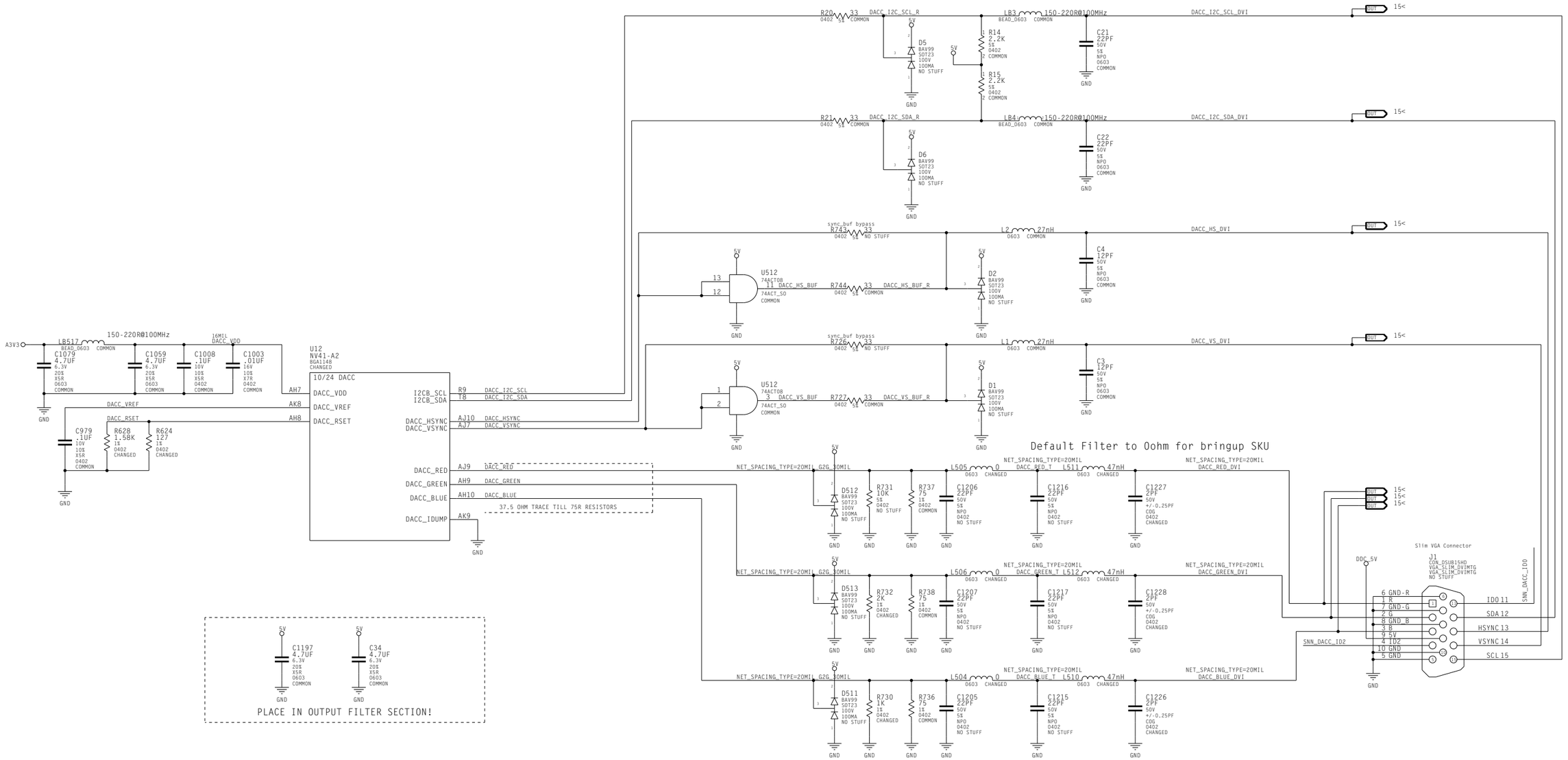
14 DACC Interface



NET RULES

	NET	IMPEDANCE (ALL:ALL:37.5:5%)	VOLTAGE
IN	DACC_RED	U12.AJ9:R731.1:37.50 ohm:10 %	
IN	DACC_GREEN	U12.AH9:R732.1:37.50 ohm:10 %	
IN	DACC_BLUE	U12.AH10:R730.1:37.50 ohm:10 %	
IN	DACC_VDD		3.3V

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	DACC Interface

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15 IFP A/B and C/D Interface

NET RULES

NET	DIFFPAIR	SPACING
IFPAB_TXC*	IFPAB_TXC	20MIL
IFPAB_TXC	IFPAB_TXC	20MIL
IFPAB_TXD0*	IFPAB_TXD0	20MIL
IFPAB_TXD0	IFPAB_TXD0	20MIL
IFPAB_TXD1*	IFPAB_TXD1	20MIL
IFPAB_TXD1	IFPAB_TXD1	20MIL
IFPAB_TXD2*	IFPAB_TXD2	20MIL
IFPAB_TXD2	IFPAB_TXD2	20MIL
SNN_IFPAB_TXD3*		
SNN_IFPAB_TXD3		
SNN_IFPB_TXC*		
SNN_IFPB_TXC		
IFPAB_TXD4*	IFPAB_TXD4	20MIL
IFPAB_TXD4	IFPAB_TXD4	20MIL
IFPAB_TXD5*	IFPAB_TXD5	20MIL
IFPAB_TXD5	IFPAB_TXD5	20MIL
IFPAB_TXD6*	IFPAB_TXD6	20MIL
IFPAB_TXD6	IFPAB_TXD6	20MIL
SNN_IFPAB_TXD7*		
SNN_IFPAB_TXD7		

NET RULES

NET	VOLTAGE
IFPAB_PLLVDD	3.3V
IFPA_IOVDD	3.3V
IFPB_IOVDD	3.3V
IFPCD_PLLVDD	3.3V
IFPC_IOVDD	3.3V
IFPD_IOVDD	3.3V

NET RULES

NET	DIFFPAIR	SPACING
IFPC_TXC*	IFPC_TXC	20MIL
IFPC_TXC	IFPC_TXC	20MIL
IFPCD_TXD0*	IFPCD_TXD0	20MIL
IFPCD_TXD0	IFPCD_TXD0	20MIL
IFPCD_TXD1*	IFPCD_TXD1	20MIL
IFPCD_TXD1	IFPCD_TXD1	20MIL
IFPCD_TXD2*	IFPCD_TXD2	20MIL
IFPCD_TXD2	IFPCD_TXD2	20MIL
SNN_IFPCD_TXC*		
SNN_IFPCD_TXC		
IFPCD_TXD4*	IFPCD_TXD4	20MIL
IFPCD_TXD4	IFPCD_TXD4	20MIL
IFPCD_TXD5*	IFPCD_TXD5	20MIL
IFPCD_TXD5	IFPCD_TXD5	20MIL
IFPCD_TXD6*	IFPCD_TXD6	20MIL
IFPCD_TXD6	IFPCD_TXD6	20MIL

Place Pullups as Close as Possible to GPU

Place Pullups as Close as Possible to GPU

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	IFP A/B and C/D Interface

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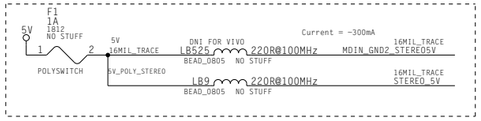
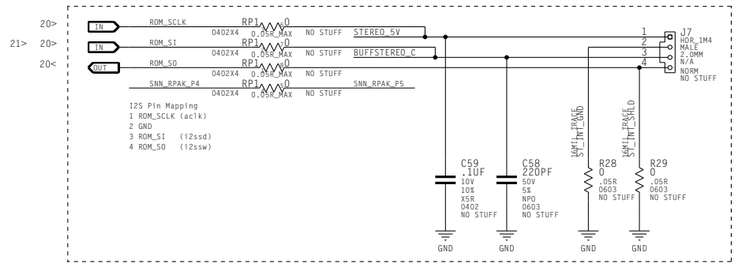
16 DACB Interface

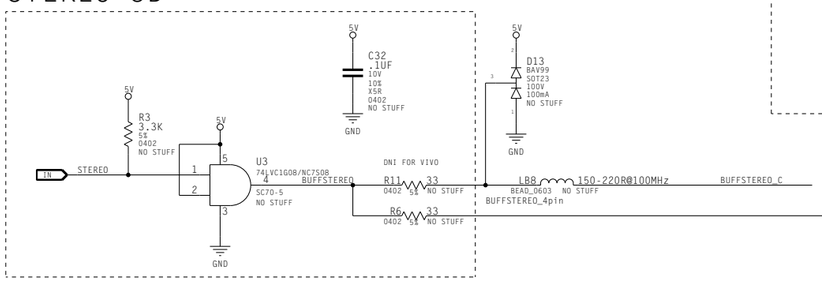
STEREO 5V



Internal Stereo Out/ I2S (Optional)

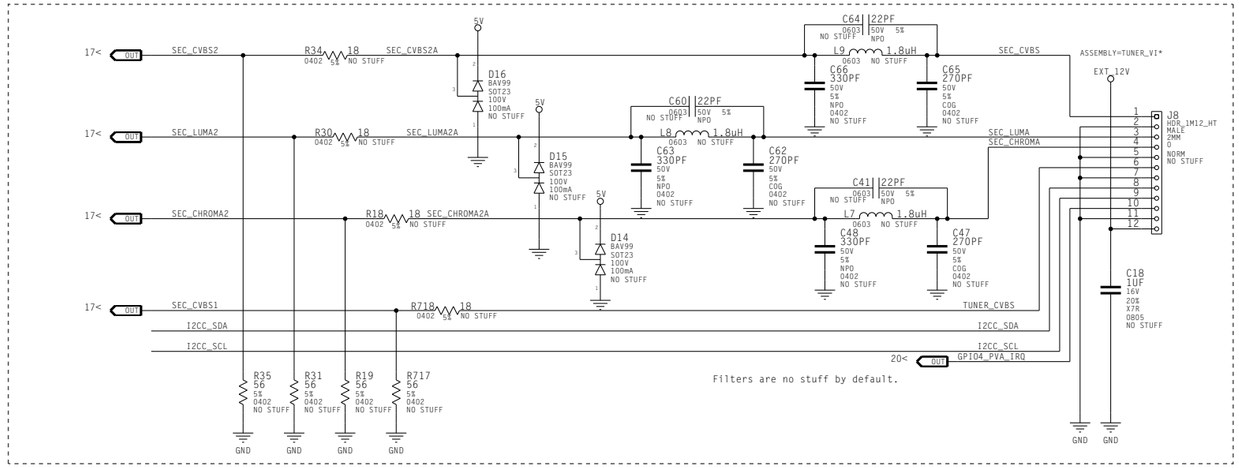


STEREO 3D



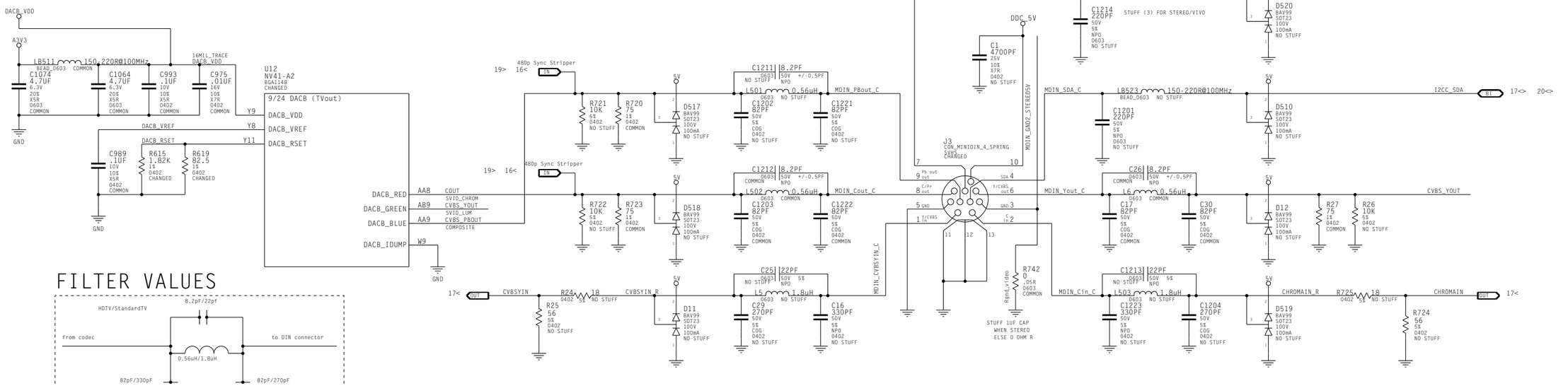
PVA (PCI TUNER / INTERNAL VIDEO)

Notes:
1X5 header can be used if only internal video is required.
1X12 header will be populated for both PCI tuner and internal video.



NET RULES

NET	IMPEDENCE	SPACING	VOLTAGE
	ALL:ALL:37.5:5%		
COUT	U12.AA8:R723.1:37.50 ohm:10 %	20MIL_G2G_30MIL	
CVBS_YOUT	U12.AB9:R27.1:37.50 ohm:10 %	20MIL_G2G_30MIL	
CVBS_PBOUT	U12.AA9:R72O.1:37.50 ohm:10 %	20MIL_G2G_30MIL	



FILTER VALUES

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	DACB Interface

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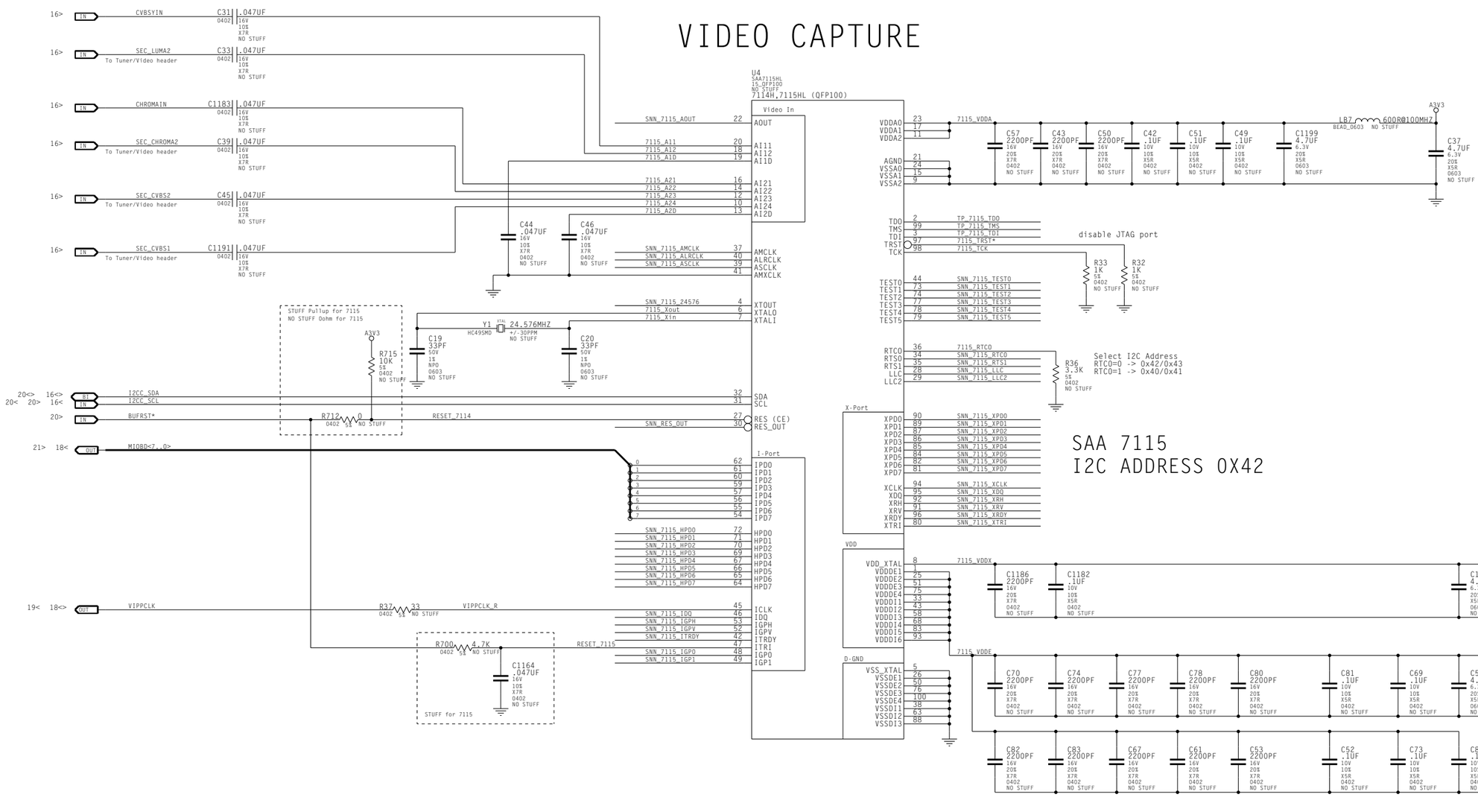
17 Video Capture (Philips 7115)

NET RULES

NET	SPACING	LINE_WIDTH	VOLTAGE
7115_VDDA		12MIL	3.3V
7115_VDDE		12MIL	3.3V
7115_VDDX		12MIL	3.3V
7115_Xout	20MIL		
7115_Xin	20MIL		

VIDEO CAPTURE



ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	Video Capture (Philips 7115)

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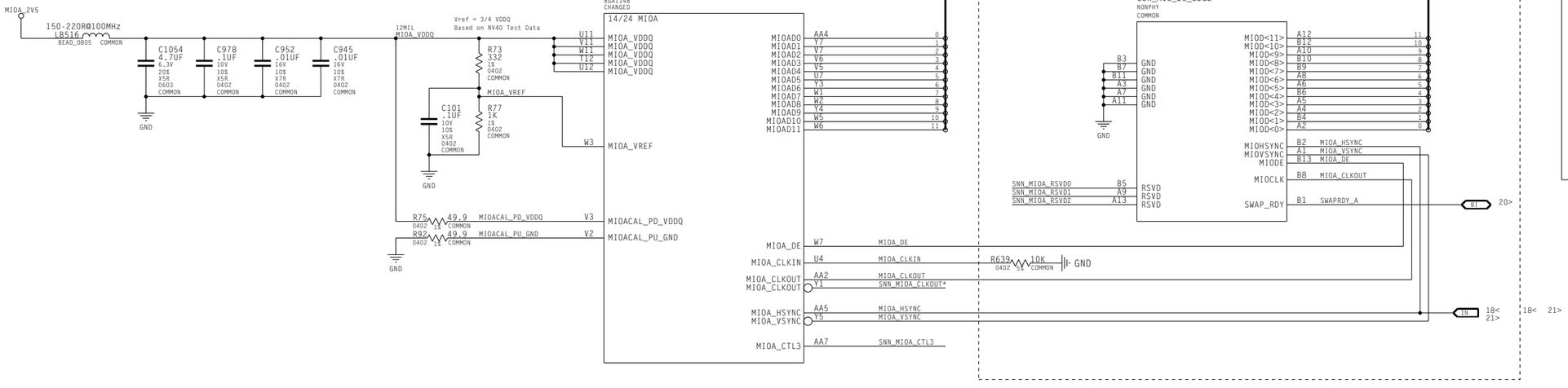
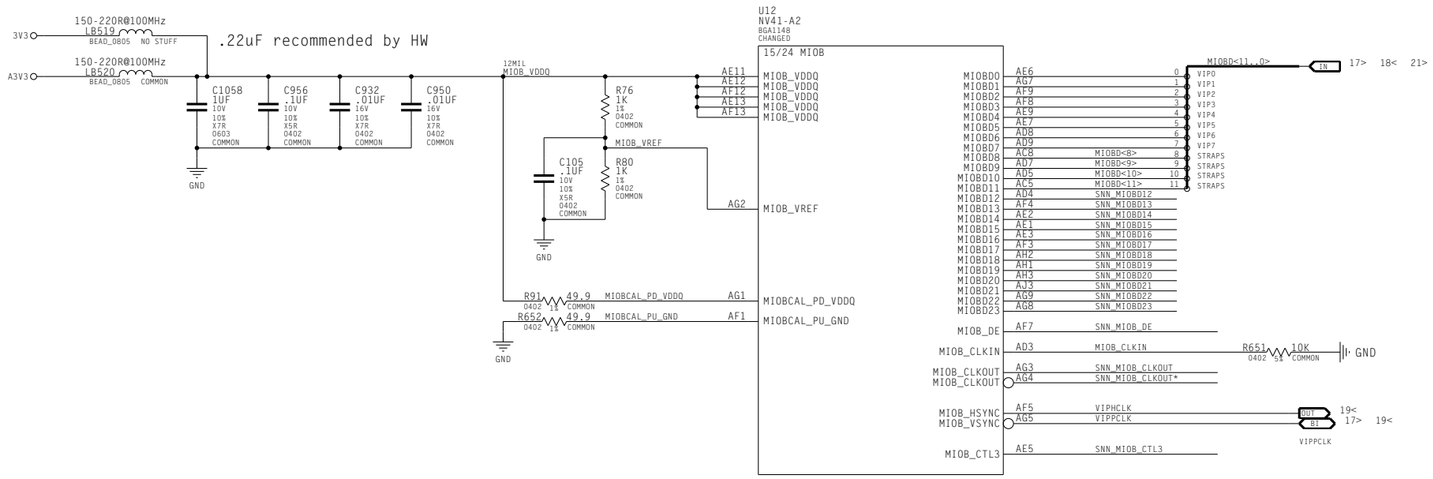
18 MIO Interface and Feature Connnector



Review Input Rail:

PCIEX - May want to use 3.3V from system



ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	MIO Interface and Feature Connnector

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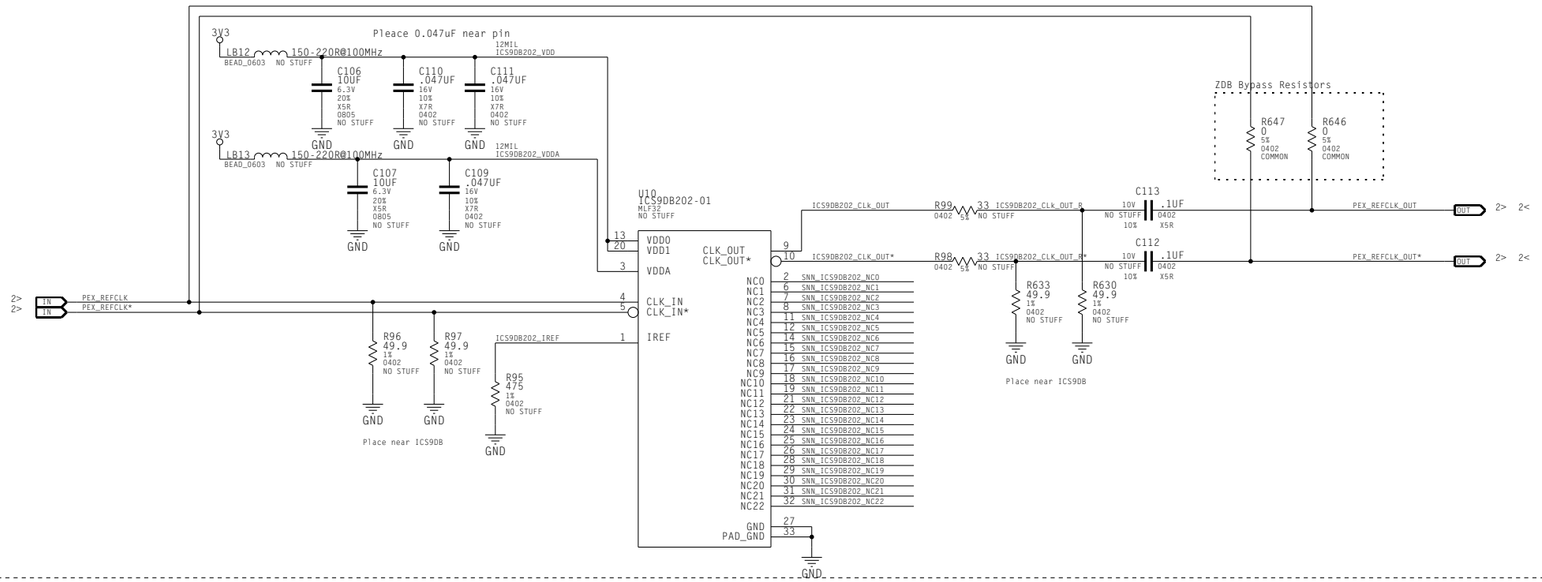
19 MISC Circuits: PEX-ZDB & SYNC STRIPPER

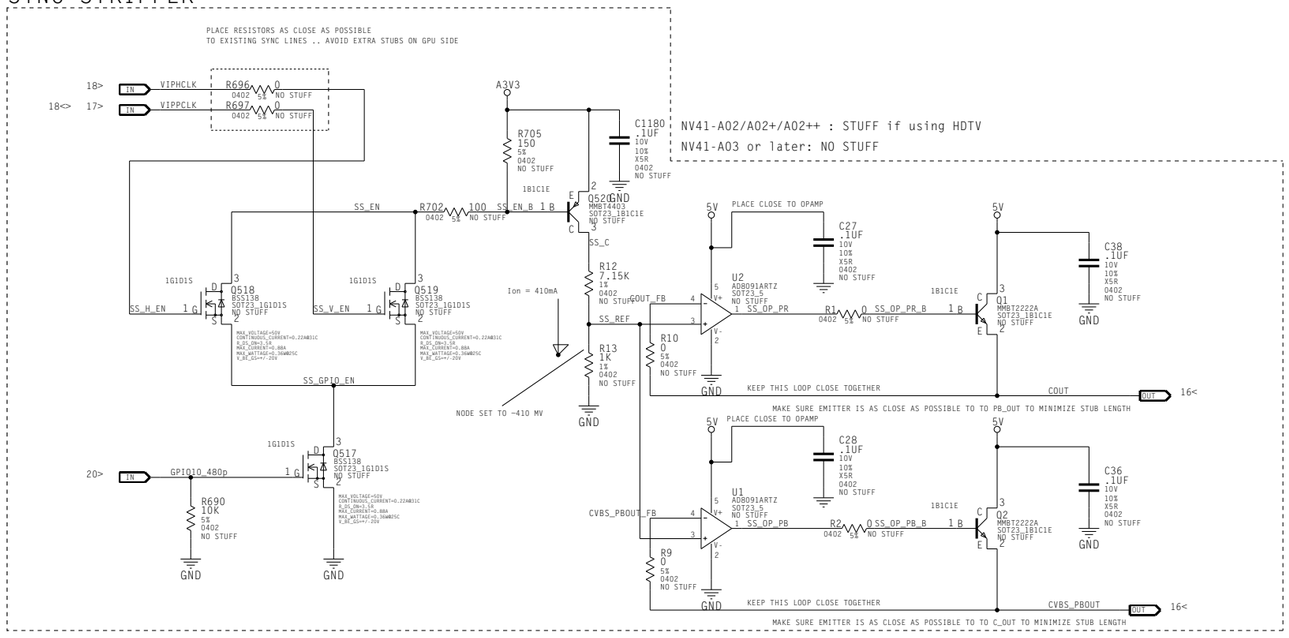
NET RULES

NET	SPACING	LINE_WIDTH	DIFFPAIR
ICS9DB202_Clk_OUT	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	ICS9DB202_CLK_OUT
ICS9DB202_CLK_OUT*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	ICS9DB202_CLK_OUT
ICS9DB202_Clk_OUT_R	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	ICS9DB202_CLK_OUT_R
ICS9DB202_CLK_OUT_R*	20MIL_G2G_30MIL_USER_DIFF	3.5MIL	ICS9DB202_CLK_OUT_R

PEX REFCLK Zero Delay Buffer



SYNC STRIPPER



ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	PEX: Zero Delay Buffer

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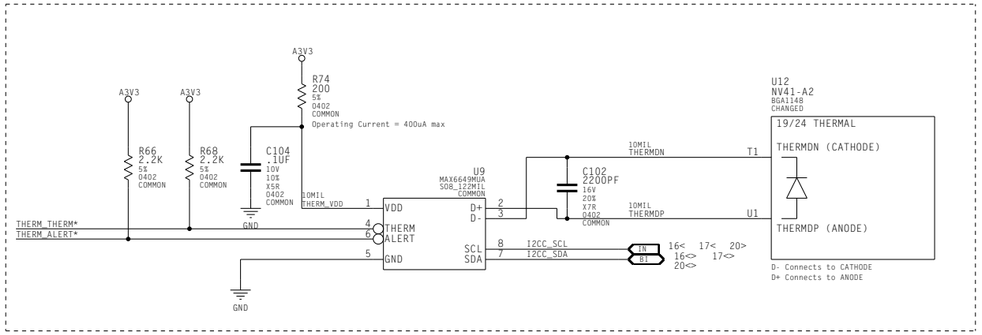
20 MISC: GPIO, I2C, THERMAL, BIOS, XTAL

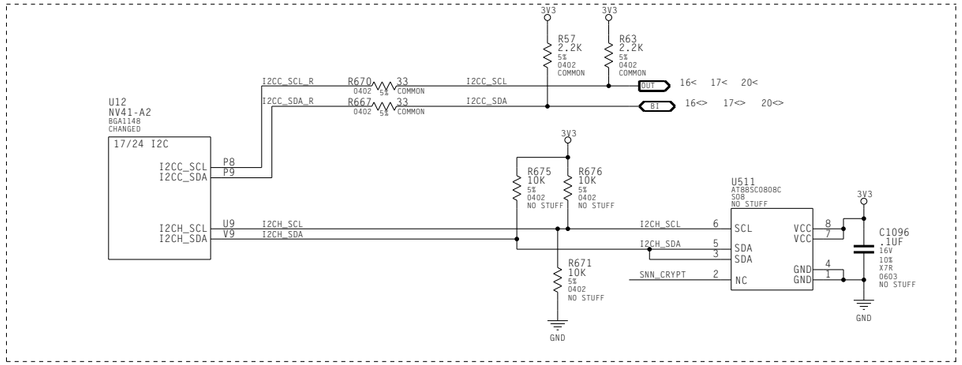
NET RULES

NET	VOLTAGE
DISP_PLLVDD	3.3V
PLLVDD	3.3V
PLLAVDD	1.4V

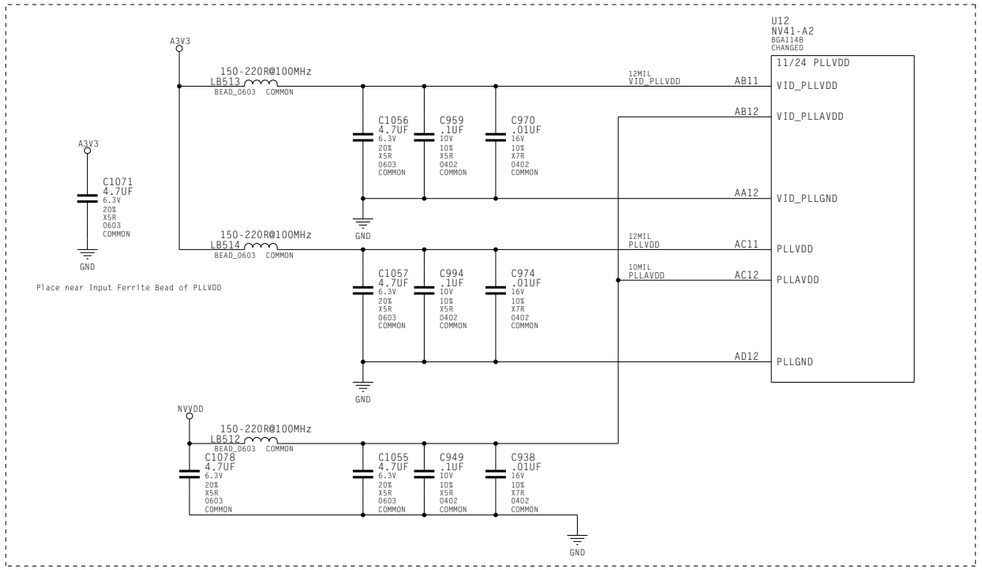
Thermal Diode



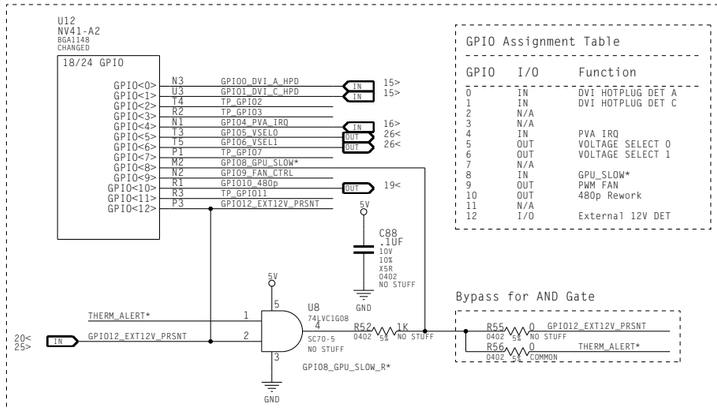
I2CC / I2CH(+ HDCP ROM)



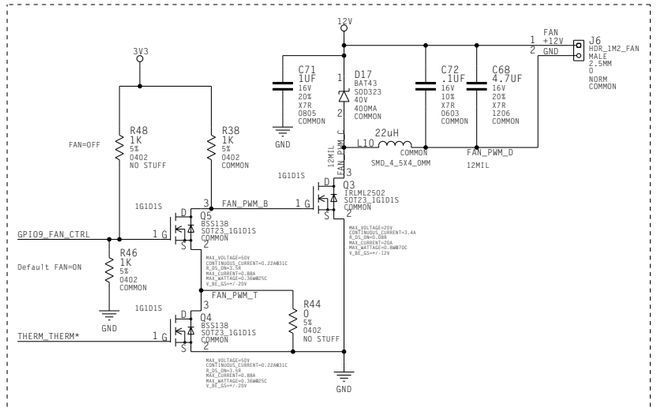
PLLVDD/VID_PLLVDD



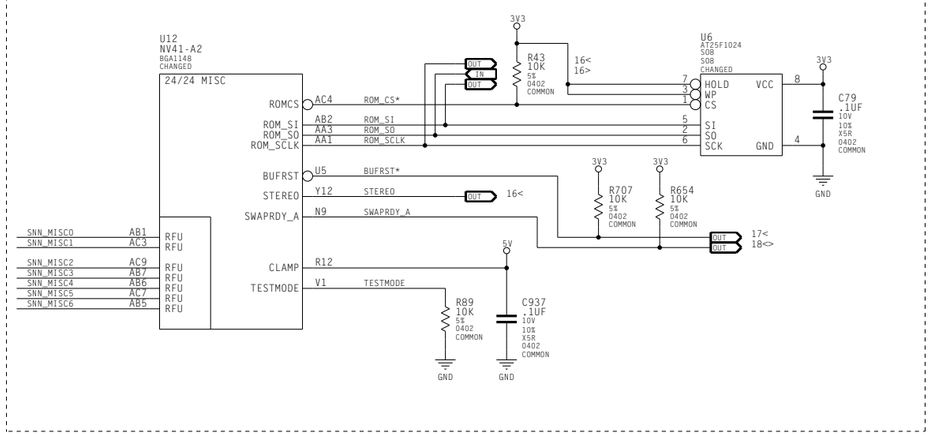
GPIO



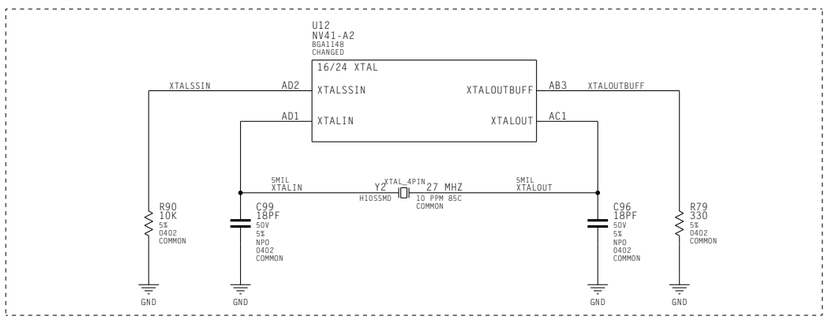
FAN CONTROL



ROM / MISC (BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)



XTAL



ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	MISC: GPIO, I2C, THERMAL, BIOS, XTAL

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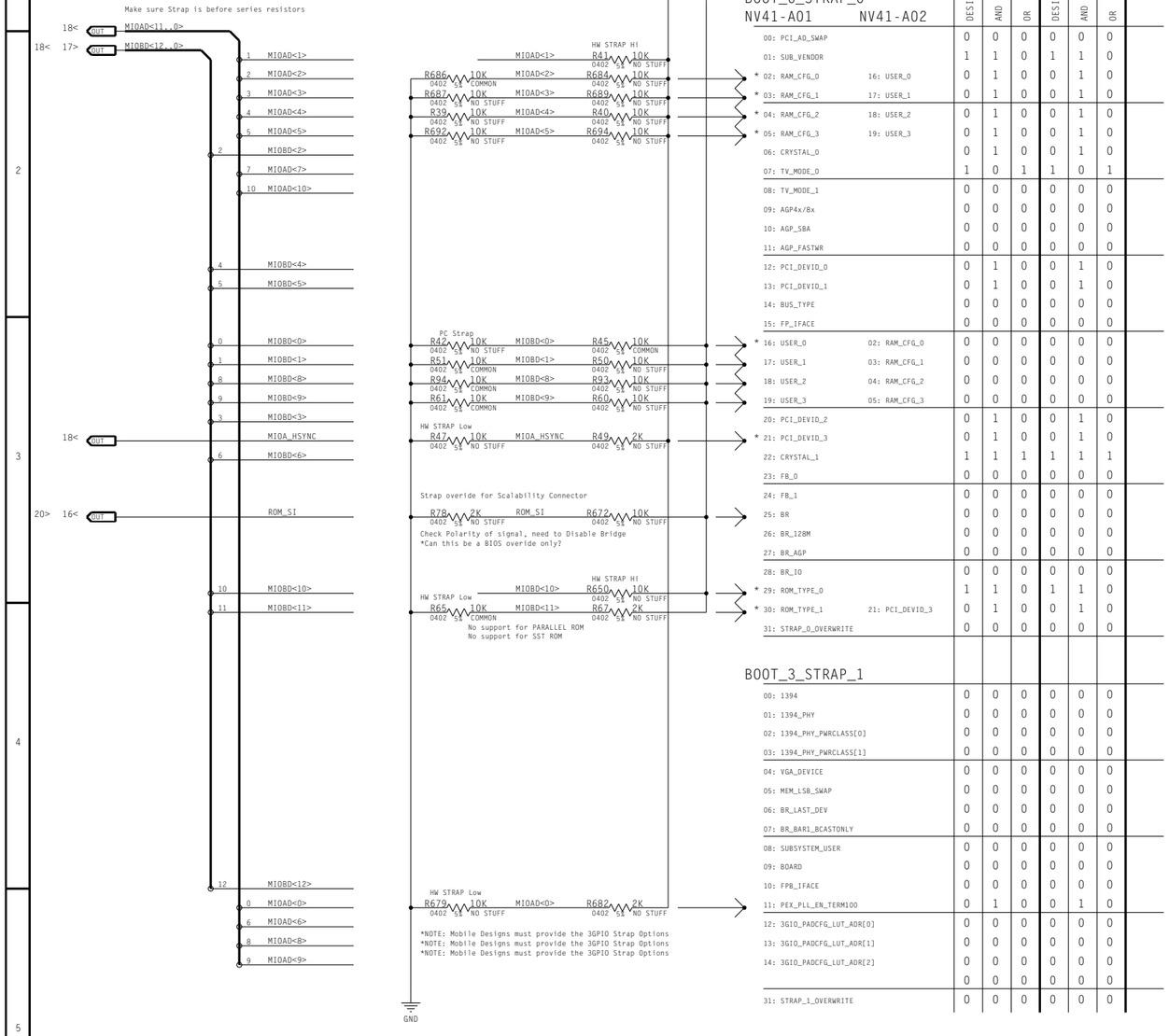
21 Strapping Configuration



Standardized Straps
SUBVENDOR
ROMTYPE[1:0]
PCI_AD
BUS_TYPE
RAMCFG[3:0]
USER[0]
DEVID[3]

AND MASK
1 -> HARDWARE STRAP
0 -> BIOS STRAP

OR MASK
1 -> DESIRED=1 ANDMASK=0

SKU#	(256Mb) 0000			(256Mb) xxxx		
BOOT_0_STRAP_0 NV41-A01 NV41-A02	DESIRED	AND MASK	OR MASK	DESIRED	AND MASK	OR MASK
00: PCI_AD_SWAP	0	0	0	0	0	0
01: SUB_VENDOR	1	1	0	1	1	0
* 02: RAM_CFG_0 16: USER_0	0	1	0	0	1	0
* 03: RAM_CFG_1 17: USER_1	0	1	0	0	1	0
* 04: RAM_CFG_2 18: USER_2	0	1	0	0	1	0
* 05: RAM_CFG_3 19: USER_3	0	1	0	0	1	0
06: CRYSTAL_0	0	1	0	0	1	0
07: TV_MODE_0	1	0	1	1	0	1
08: TV_MODE_1	0	0	0	0	0	0
09: AGP4x/Bx	0	0	0	0	0	0
10: AGP_SBA	0	0	0	0	0	0
11: AGP_FASTWR	0	0	0	0	0	0
12: PCI_DEVID_0	0	1	0	0	1	0
13: PCI_DEVID_1	0	1	0	0	1	0
14: BUS_TYPE	0	0	0	0	0	0
15: FP_IFACE	0	0	0	0	0	0
* 16: USER_0 02: RAM_CFG_0	0	0	0	0	0	0
17: USER_1 03: RAM_CFG_1	0	0	0	0	0	0
18: USER_2 04: RAM_CFG_2	0	0	0	0	0	0
19: USER_3 05: RAM_CFG_3	0	0	0	0	0	0
20: PCI_DEVID_2	0	1	0	0	1	0
* 21: PCI_DEVID_3	0	1	0	0	1	0
22: CRYSTAL_1	1	1	1	1	1	1
23: FB_O	0	0	0	0	0	0
24: FB_1	0	0	0	0	0	0
25: BR	0	0	0	0	0	0
26: BR_128M	0	0	0	0	0	0
27: BR_AGP	0	0	0	0	0	0
28: BR_IO	0	0	0	0	0	0
* 29: ROM_TYPE_O	1	1	0	1	1	0
* 30: ROM_TYPE_1 21: PCI_DEVID_3	0	1	0	0	1	0
31: STRAP_O_OVERWRITE	0	0	0	0	0	0
BOOT_3_STRAP_1						
00: 1394	0	0	0	0	0	0
01: 1394_PHY	0	0	0	0	0	0
02: 1394_PHY_PWRCLASS[0]	0	0	0	0	0	0
03: 1394_PHY_PWRCLASS[1]	0	0	0	0	0	0
04: VGA_DEVICE	0	0	0	0	0	0
05: MEM_LSB_SWAP	0	0	0	0	0	0
06: BR_LAST_DEV	0	0	0	0	0	0
07: BR_BAR1_BCASTONLY	0	0	0	0	0	0
08: SUBSYSTEM_USER	0	0	0	0	0	0
09: BOARD	0	0	0	0	0	0
10: FPB_IFACE	0	0	0	0	0	0
11: PEX_PLL_EN_TERM100	0	1	0	0	1	0
12: 3GIO_PADCFG_LUT_ADR[0]	0	0	0	0	0	0
13: 3GIO_PADCFG_LUT_ADR[1]	0	0	0	0	0	0
14: 3GIO_PADCFG_LUT_ADR[2]	0	0	0	0	0	0
	0	0	0	0	0	0
31: STRAP_1_OVERWRITE	0	0	0	0	0	0

Please Verify against HW Manual

Last Checked Dec 19, 2003

```
                NV_STRAP_0
                ------------------------------------------
HW Default      BIT FUNCTION            NORMAL PIN (RTL Name)
                ------------------------------------------
                  0  PCI_AD              'NV_PEXTDEV_BOOT_O_STRAP_PCI_AD_NORMAL
                1 1  SUB_VENDOR         MIOAD1 (Ccirra_data[1])
                  2  RAMCFG[O]           MIOAD2 (Ccirra_data[2])
                  3  RAMCFG[1]           MIOAD3 (Ccirra_data[3])
                  4  RAMCFG[2]           MIOAD4 (Ccirra_data[4])
                  5  RAMCFG[3]           MIOAD5 (Ccirra_data[5])
                0 6  CRYSTAL[O]          MIOBD2 (Ccirb_data[2])
                1 7  TVMODE[O]           MIOAD7 (Ccirra_data[7])
                0 8  TVMODE[1]           MIOAD10 (Ccira_data[10])
                  9  AGP_4X              'NV_PEXTDEV_BOOT_O_STRAP_AGP_4X_DISABLED
                  10 AGP_SBA             'NV_PEXTDEV_BOOT_O_STRAP_AGP_SBA_DISABLED
                  11 AGP_FASTWR          'NV_PEXTDEV_BOOT_O_STRAP_AGP_FASTWR_DISABLED
                0 12 PCI_DEVID[0]        MIOBD4 (Ccirb_data[4])
                0 13 PCI_DEVID[1]        MIOBD5 (Ccirb_data[5])
                  14 AGP                 'NV_PEXTDEV_BOOT_O_STRAP_BUS_TYPE_PCI
                  15 FP_IFACE            'NV_PEXTDEV_BOOT_O_STRAP_FP_IFACE_12BIT
                  16 Strap_user[O]       MIOBD0 (Ccirb_data[0])
                  17 Strap_user[1]       MIOBD1 (Ccirb_data[1])
                  18 Strap_user[2]       MIOBD8 (Ccirb_data[8])
                  19 Strap_user[3]       MIOBD9 (Ccirb_data[9])
                0 20 PCI_DEVID[2]        MIOBD3 (Ccirb_data[3])
                0 21 PCI_DEVID[3]        MIOA_HSYNC (ccira_hsync)
                  22 CRYSTAL[1]          MIOBD6 (Ccirb_data[6])
                  23 FB[O]               0
                  24 FB[1]               1
                1 25 BR                  ROM_SI (Rom_si)
                  26 BR_128M             'NV_PEXTDEV_BOOT_O_STRAP_BR_REG_128M_DISABLED
                  27 BR_AGP              'NV_PEXTDEV_BOOT_O_STRAP_BR_AGP_DEV_DISABLED
                  28 BR_IO               'NV_PEXTDEV_BOOT_O_STRAP_BR_IO_DEV_DISABLED
                1 29 ROMTYPE[O]          MIOBD10 (Ccirb_data[10])
                0 30 ROMTYPE[1]          MIOBD11 (Ccirb_data[11])

                NV_STRAP_1
                ------------------------------------------
                BIT FUNCTION             NORMAL PIN (RTL Name)
                ------------------------------------------
                  0  1394                'NV_PEXTDEV_BOOT_3_STRAP_1_1394_DISABLED
                  1  1394_PHY            'NV_PEXTDEV_BOOT_3_STRAP_1_1394_PHY_DISABLED
                  2  1394_PHY_PWRCLASS[0] O
                  3  1394_PHY_PWRCLASS[1] O
                  4  VGA_DEVICE          'NV_PEXTDEV_BOOT_3_STRAP_1_VGA_DEVICE_ENABLED
                  5  MEM_LSB_SWAP        'NV_PEXTDEV_BOOT_3_STRAP_1_MEM_LSB_SWAP_DISABLED
                  6  BR_LAST_DEV         'NV_PEXTDEV_BOOT_3_STRAP_1_BR_LAST_DEV_DISABLED
                  7  BR_BAR1_BCASTONLY   'NV_PEXTDEV_BOOT_3_STRAP_1_BR_BAR1_BCASTONLY_ENABLED
                  8  SUBSYSTEM_USER      'NV_PEXTDEV_BOOT_3_STRAP_1_SUBSYSTEM_USER_DISABLED
                  9  BOARD               'NV_PEXTDEV_BOOT_3_STRAP_1_BOARD_O
                1 10 FPB_IFACE           MIOBD12 (Ccirb_data[12])
                0 11 PEX_PLL_EN_TERM100  MIOADO (Ccira_data[0])
                0 12 3GIO_PADCFG_LUT_ADR[0] MIOAD6 (Ccira_data[6])
                0 13 3GIO_PADCFG_LUT_ADR[1] MIOAD8 (Ccira_data[8])
                0 14 3GIO_PADCFG_LUT_ADR[2] MIOAD9 (Ccira_data[9])
*HW has Internal 10K Strap, need 1K to overide
```

SUB_VENDOR[0]	0 - NO_BIOS 1 - READ FROM BIOS (DESIRED)
RAM_CFG[3:0]	0000 N/A 0001 8pcs 8Mx32 Monolithic 0010 N/A 0011 8pcs 8Mx32 Stacked Die 0100 N/A 0101 N/A 0110 8PCS 4Mx32 Hynix 0111 N/A
CRYSTAL[1:0]	00 - 13.5 MHz 01 - 14.31818 MHz 10 - 27.000 MHz (DESIRED) 11 - UNKNOWN
TVMODE[1:0]	00 - SECAM 01 - NTSC (DESIRED) 10 - PAL 11 - CRT
PCI_DEVID[3:0]	0000 = NV41 = 0x000 1100 = NV41-U-A1 = 0x0C0
USER[3:0]	0000 - USER STRAP
FB[1:0]	00 - 64MEG (DESIRED) 01 - 128MEG 10 - 256MEG 11 - 512MEG
ROM_TYPE[1:0]	00 - PARALLEL (NOT SUPPORTED) 01 - SERIAL AT25F (DESIRED) 10 - SERIAL SST45VF/LF 11 - RFU
BR	0 - ENABLE 1 - DISABLED (Default)
FPB_IFACE	0 - 12Bit 1 - 24bit (Default)
PEX_PLL_EN_TERM100	0 - ENABLED (Internal 100ohm Term) 1 - DISABLED
3GIO_PADCFG_LUT_ADR[2:0]	000 = DEFAULT
STRAP_OVERWITE	0 - DISABLED (DESIRED) 1 - ENABLED

NV Register Description	NV Address	BIOS Address	Data SKU#0000	Data SKU#xxxx
BOOT_0_STRAP_0	0x00101000		0xXXXXXXXX	0xXXXXXXXX
BOOT_1_STRAP_0_ANDMASK	0x00101004	0x58	0xXXXXXXXX	0xXXXXXXXX
BOOT_2_STRAP_0_ORMASK	0x00101008	0x5C	0xXXXXXXXX	0xXXXXXXXX
BOOT_3_STRAP_1	0x0010100C		0x0000XXXX	0x0000XXXX
BOOT_4_STRAP_1_ANDMASK	0x00101010	0x60	0x0000XXXX	0x0000XXXX
BOOT_5_STRAP_1_ORMASK	0x00101014	0x64	0x0000XXXX	0x0000XXXX

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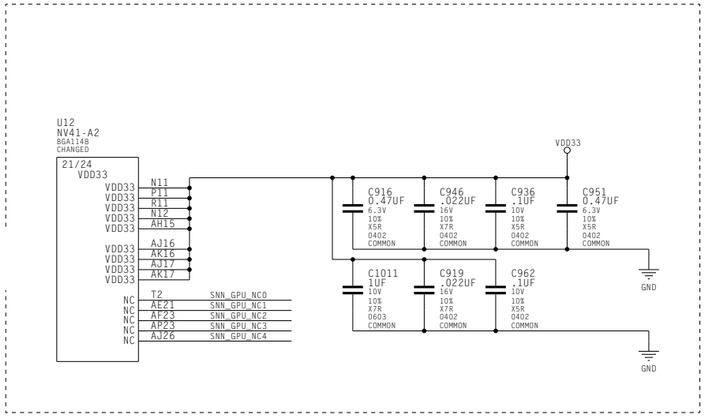
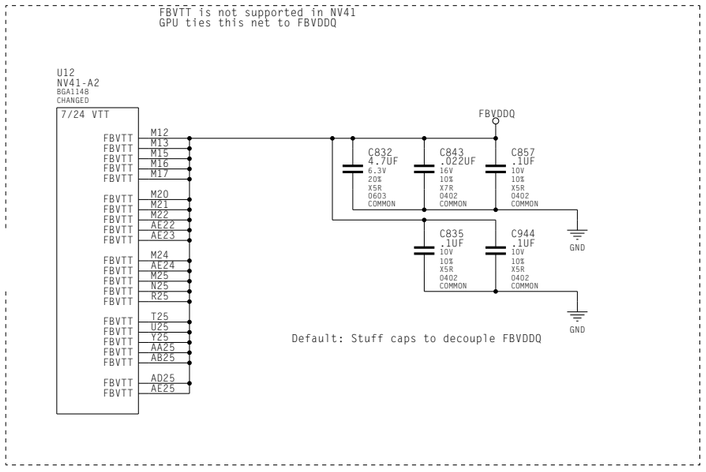
22 Power/GND and Decoupling

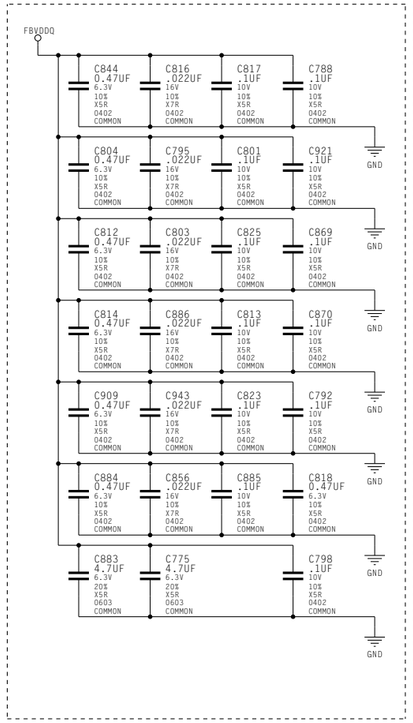
VDD33



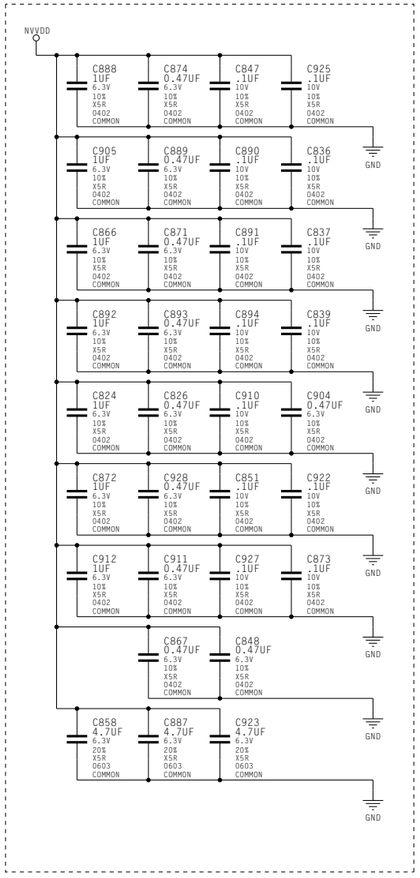
FBVTT

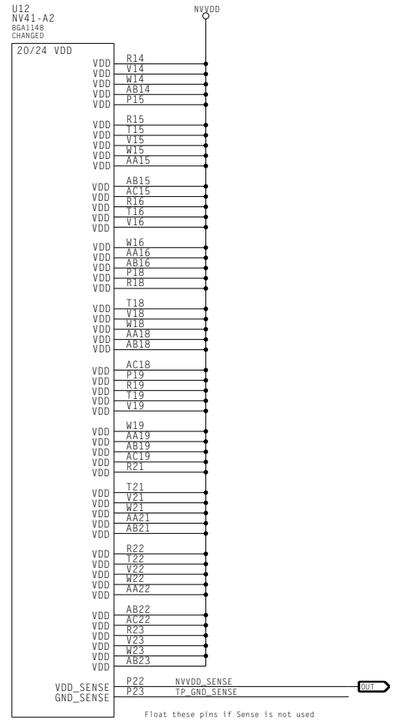


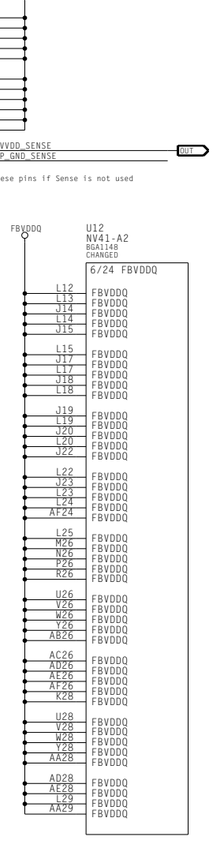
FBVDDQ

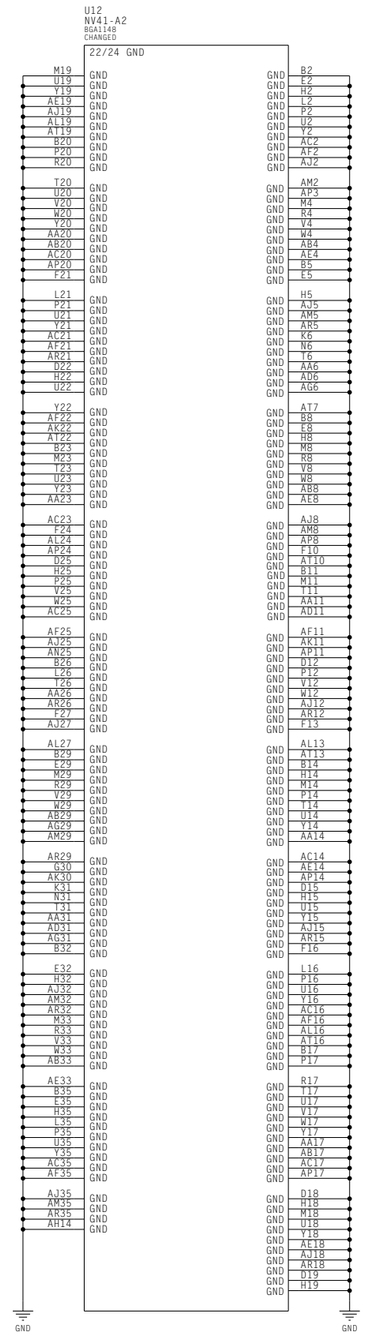


NVVDD









NET RULES

NET	VOLTAGE
FBVTT IN	FBVTT 1.35V
	VTTGEN 1.35V

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	Power/GND and Decoupling

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	22 OF 37
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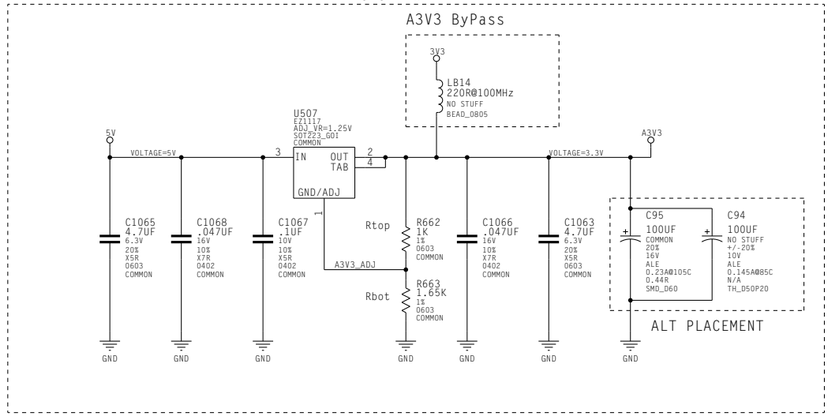
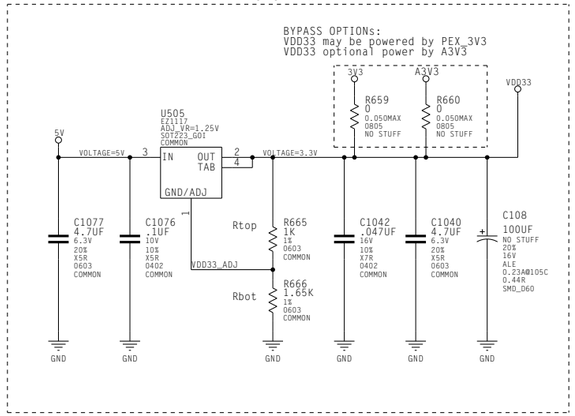
23 Power Supply I: Analog 3.3V

Analog 3.3V Power Supply



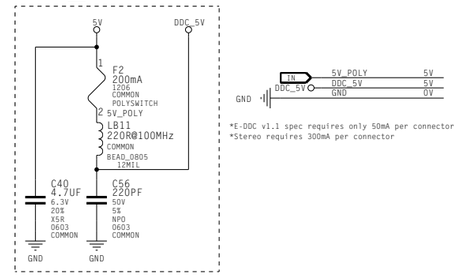
Vout = VRef * (1+Rbot/Rtop)
3.31V = 1.25V * (1+1650/1000)

VDD33 Power Supply



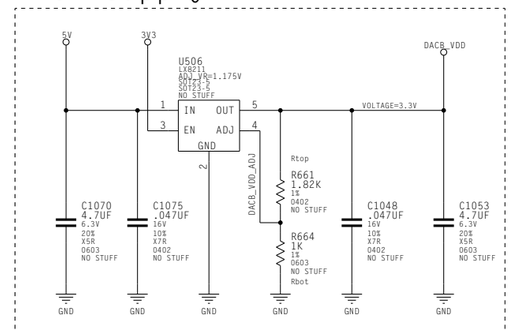
Vout = VRef * (1+Rbot/Rtop)
3.31V = 1.25V * (1+1650/1000)

DDC_5V



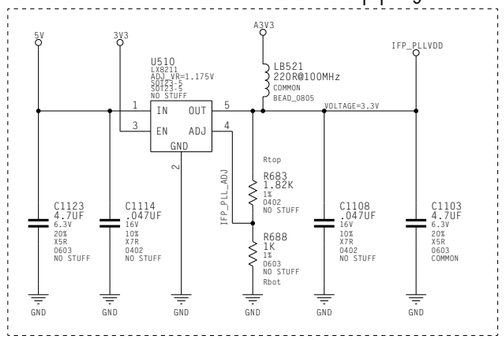
*E-DDC v1.1 spec requires only 50mA per connector
*Stereo requires 300mA per connector

DACB Supply



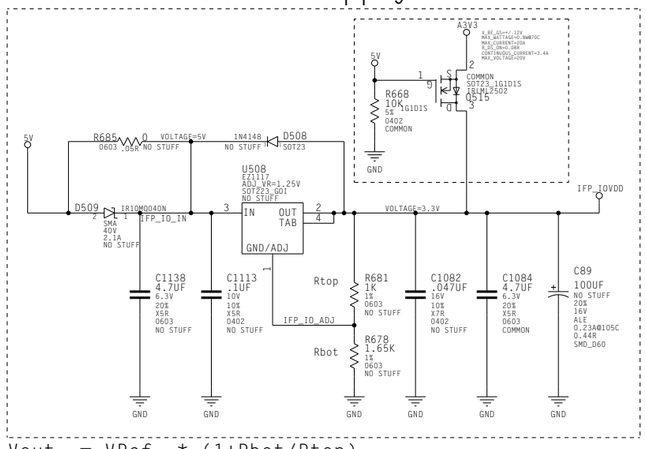
Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+1820/1000)

Internal TMDS PLL Supply



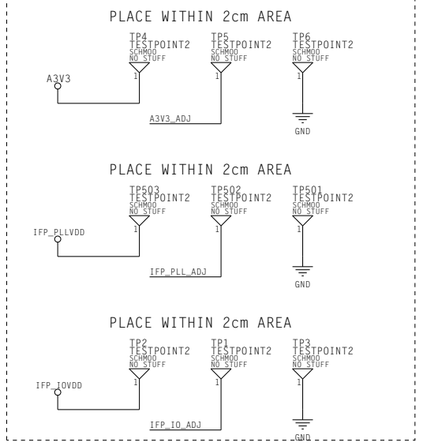
Vout = VRef * (1+Rtop/Rbot)
2.8V = 1.175V * (1+1400/1000)
3.31V = 1.175V * (1+1820/1000)

Internal TMDS IO Supply

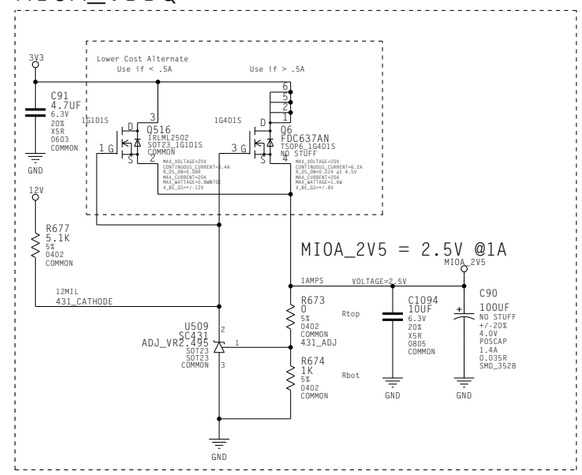


Vout = VRef * (1+Rbot/Rtop)
3.31V = 1.25V * (1+1650/1000)

SHMOO Testpoints



MIOA_VDDQ



Vout = Vref * (1+Rtop/Rbot)
Vout = 2.5V * (1+0R/NO STUFF) = 2.5V

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	Power Supply I: Analog 3.3V

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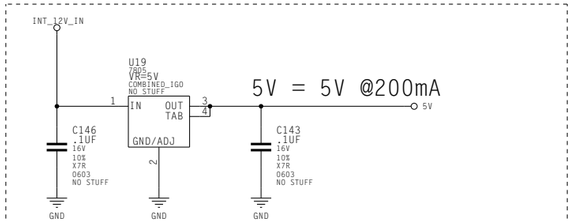
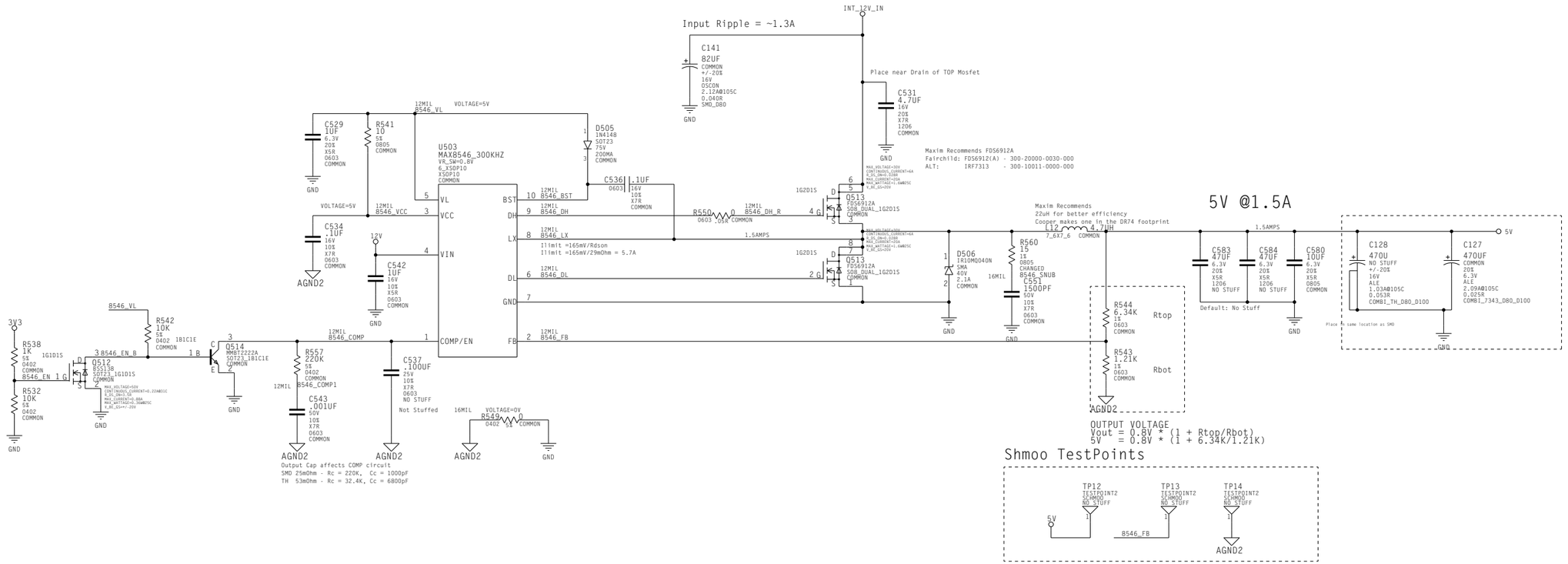
24 Power Supply II: 5V

Alternate 5V regulator



Only use this Alternate when A3V3 regulator is not Stuffed

Conditions for Linear 5V:
1- If all Analog 3.3V circuits are tested to +/-10% tolerance
2- 5V Linear will supply DDC 5V + Diode protection circuits
3- Must Not use when Stereo is an Option



Shmoo TestPoints

PLACE WITHIN 2cm AREA

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	Power Supply II: 5V

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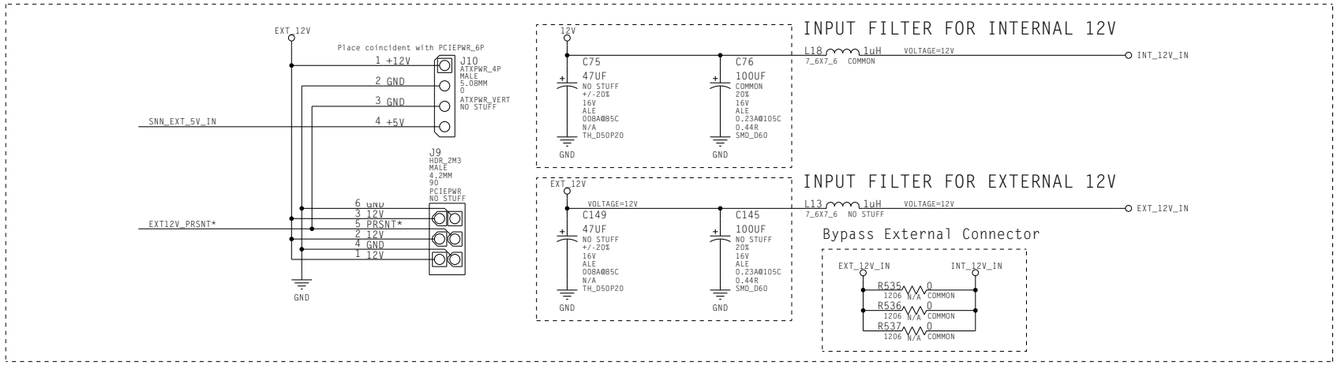
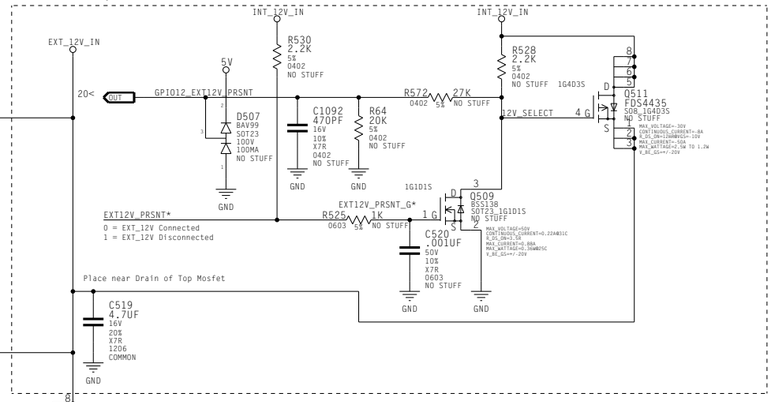
25 Power Supply III: NVVDD/FBVDDQ

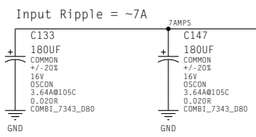
Internal & External 12V Input Filters



12V Input Selection for FBVDDQ



Input Ripple = ~7A



Shmoo TestPoints

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	Power Supply III: NVVDD/FBVDDQ

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2701 SAN TOMAS EXPRESSWAY
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NV_PN	600-10260-0004-300		
ID	design	PAGE	25 OF 37
NAME	JLAM	DATE	19-AUG-2004

26 Power Supply IV: NVVDD

NET RULES

NET	PHYSICAL	VOLTAGE
NVVDD	36MIL_TRACE	1.4V
NV_PHASE1	12MIL_TRACE	1.2V
NV_PHASE2	12MIL_TRACE	1.2V
NV_VCC	12MIL_TRACE	5V
NV_BOOT1	10MIL_TRACE	3.3V
NV_BOOT2	10MIL_TRACE	3.3V
NV_COMP	10MIL_TRACE	3.3V
NV_COMP_FB	10MIL_TRACE	3.3V
NV_FB	10MIL_TRACE	3.3V
NV_PWM1	10MIL_TRACE	3.3V
NV_PWM2	10MIL_TRACE	3.3V
NV_VDIFF	10MIL_TRACE	3.3V
NV_OFS	10MIL_TRACE	3.3V
NV_ISEN1	10MIL_TRACE	3.3V
NV_ISEN2	10MIL_TRACE	3.3V
PH1_SNB	10MIL_TRACE	1.2V
PH2_SNB	10MIL_TRACE	1.2V
NV_UGATE1	24MIL_TRACE	12V
NV_UGATE2	24MIL_TRACE	12V
NV_UGATE1_R	24MIL_TRACE	12V
NV_UGATE2_R	24MIL_TRACE	12V
NV_LGATE1	24MIL_TRACE	12V
NV_LGATE2	24MIL_TRACE	12V
NV_LGATE1_R	24MIL_TRACE	12V
NV_LGATE2_R	24MIL_TRACE	12V

Input Ripple = ~ 11A

11AMPS

INT_12V_IN

Place near Drain of Top Mosfet

C132 330UF NO STUFF 16V OSCON 4.72A@105C 0.016R COMBI_7343D80D1001812

C144 330UF COMMON +/-20% 16V OSCON 4.72A@105C 0.016R COMBI_7343D80D1001812

C151 330UF COMMON +/-20% 16V OSCON 4.72A@105C 0.016R COMBI_7343D80D1001812

C521 4.7UF 16V 20% X7R 1206 COMMON

C523 .01UF 0402 25V 10% X7R COMMON

R529 6.34K 1% 0402 COMMON

12MIL ILIM1

Notes: LFPAK Footprint allows SO8 alternates
FET Options:
1. TOP - IRF7821, BOT - HAT2165H
2. TOP - IRF7821, BOT - 2xIRF7832
3. TOP - HAT2168H, BOT - HAT2165H

Overcurrent Sense:
Ipeak = 200uA * Rilim/Rdson
91A = 200uA * 6.34K/0.0139R

Q507 HAT2168H LFPAK COMMON

Q508 HAT2168H LFPAK NO STUFF

R531 2.2 5% 0402 COMMON

C526 .1UF 0402 10V 10% X5R COMMON

Q501 IRF7832 SO8_1G4D3S CHANGED

Q503 IRF7832 SO8_1G4D3S CHANGED

Low Side FET ALT: SI7880DP - 300-17880-0000-000

C501 1500PF 50V 10% X7R 0603 NO STUFF

Stuff cap if needed to improve Cgs/Cgd ratio!

Pd = 1.6W@70C on SO8 FETs
*Efficiency needs to be 80%+ to use SO8
Estimate for NVVDD = 25A:
Pd_HS = 1.6W
Pd_LS = 4.6W

Output Inductor Options:
Vishay - 131-20000-0031-000 1.2mOhm, 41A
Vishay - 131-20000-0032-000 1.3mOhm, 38A
Toko - 131-20000-0033-000 1.12mOhm, 32.3A
Falco - 131-20000-0038-000 0.72mOhm, 30.3A
Abracon- 2.5mOhm, 30A

NVVDD = 1.1V..1.4V (25A - 30A)

30AMPS

CONTINUOUS_CURRENT=38A

L14 0.47UH SMD_590x530 COMMON

VOLTAGE=1.4V

D501 IR10MQ040N SMA 40V 2.1A COMMON

R503 1 5% 1206 COMMON

C505 1500PF 16V 10% X7R 0603 COMMON

Place near Low Side Mosfet

C153 100UF 6.3V 20% X5R 1210 COMMON

C123 100UF 6.3V 20% X5R 1210 NO STUFF

C591 4.7UF 6.3V 10% X5R 0805 COMMON

C533 47UF 6.3V 20% X5R 1206 NO STUFF

C535 47UF 6.3V 20% X5R 1206 NO STUFF

C532 47UF 6.3V 20% X5R 1206 NO STUFF

C539 47UF 6.3V 20% X5R 1206 NO STUFF

Place on Bottom
*Default = No Stuff

C125 1200UF COMMON +/-20% 4V OSCON 5.44A@105C 0.012R COMBI_7343D80D1001812

C126 1000UF NO STUFF +/-20% 4V OSCON 5.04A@45C 0.012R COMBI_TH_D8O_D10O

C136 1200UF COMMON +/-20% 4V OSCON 5.44A@105C 0.012R COMBI_7343D80D1001812

C138 1000UF NO STUFF +/-20% 4V OSCON 5.04A@45C 0.012R COMBI_TH_D8O_D10O

Place in same location as SMD

30AMPS

NVVDD

Est. Eff = 78%-80%

NVVDD Remote Sensing Option

NVVDD 22>

NVVDD_SENSE

C506 680PF 50V 5% NPO 0603 NO STUFF

C511 680PF 50V 5% NPO 0603 COMMON

FB1_NVVDD_RC

R504 22K 5% 0603 NO STUFF

R515 232K 1% 0603 CHANGED

R510 22K 5% 0603 COMMON

R509 34.8K 1% 0603 CHANGED

Compensation for NVVDD

12MIL COMP1_NVVDD

12MIL FB1_NVVDD

C516 33PF 50V 5% NPO 0603 COMMON

C509 4700PF 16V 10% X7R 0603 COMMON

COMP1_NVVDD_RC

R501 33.2K 1% 0603 COMMON

R514 53.6K 1% 0603 CHANGED

AGND

NVVDD = 0.8V * (1 + Rtop/Rbot) = Vout
NVVDD = 0.8V * (1 + 30.2k/80.6K) = 1.1V
NVVDD = 0.8V * (1 + 30.2k/60.4K) = 1.2V
NVVDD = 0.8V * (1 + 30.2k/47.5K) = 1.3V
NVVDD = 0.8V * (1 + 30.2k/40.2K) = 1.4V

NVVDD = 0.8V * (1 + 30.2k/53.6K) = 1.25V (Dell SKU)

Shmoo TestPoints

TP21 TESTPOINT2 SCHMOO NO STUFF

TP19 TESTPOINT2 SCHMOO NO STUFF

TP17 TESTPOINT2 SCHMOO NO STUFF

NVVDD

FB1_NVVDD

AGND

PLACE WITHIN 2cm AREA

VSEL1	VSEL0	NVVDD
0	0	1.1V
0	1	1.2V *Default
1	0	1.3V
1	1	1.4V

Dynamic NVVDD GPIO Voltage Selection

3V3

R545 10K 5% 0402 NO STUFF

GPIO5_VSEL0

R517 1.5K 5% 0603 NO STUFF

NV_VSEL0_G

R546 10K 5% 0402 NO STUFF

R516 232K 1% 0603 NO STUFF

Rbot0

R513 121K 1% 0603 NO STUFF

Rbot1

NV_VSEL0_R

Q504 BSS138 SOT23_1G1D1S NO STUFF

R103 10K 5% 0402 NO STUFF

GPIO6_VSEL1

R105 1.5K 5% 0603 NO STUFF

NV_VSEL1_G

R104 10K 5% 0402 NO STUFF

NV_VSEL1_R

Q502 BSS138 SOT23_1G1D1S NO STUFF

Place close to NVVDD feedback loop!

ASSEMBLY: NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL: Power Supply IV: NVVDD

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN: 600-10260-0004-300
ID: design | PAGE: 26 OF 37
NAME: JLAM | DATE: 19-AUG-2004

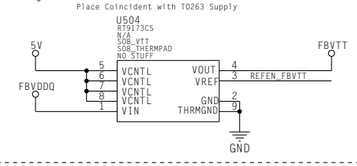
27 Power Supply V: FBVTT

S08 Regulator (Option)

S08 Part is only good for 1.5A

Only Stuff for 128bit FB Interface

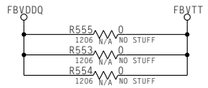
Place Coincident with TO263 Supply



Bypass FBVTT to FBVDDDQ

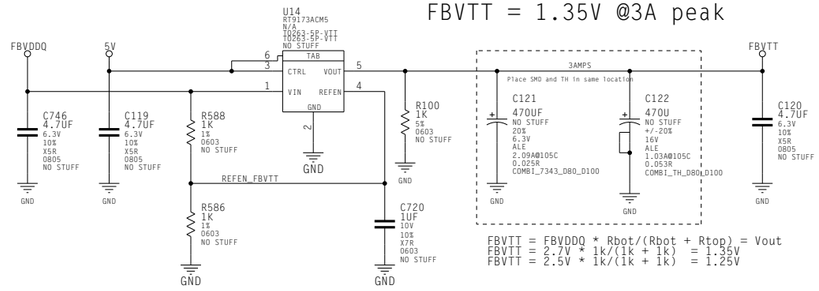
Stuff for NV41-A01

FBVTT bypass needed for IO Pullups



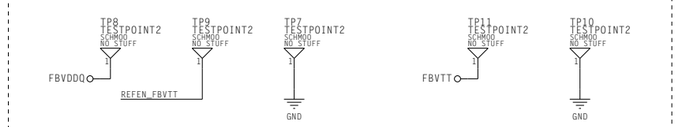
Ptot = (2.7V-1.35V)*3A = 4.05W

FBVTT = 1.35V @3A peak



FBVTT = FBVDDQ * Rbot/(Rbot + Rtop) = Vout
FBVTT = 2.7V * 1k/(1k + 1k) = 1.35V
FBVTT = 2.5V * 1k/(1k + 1k) = 1.25V

Shmoo TestPoints



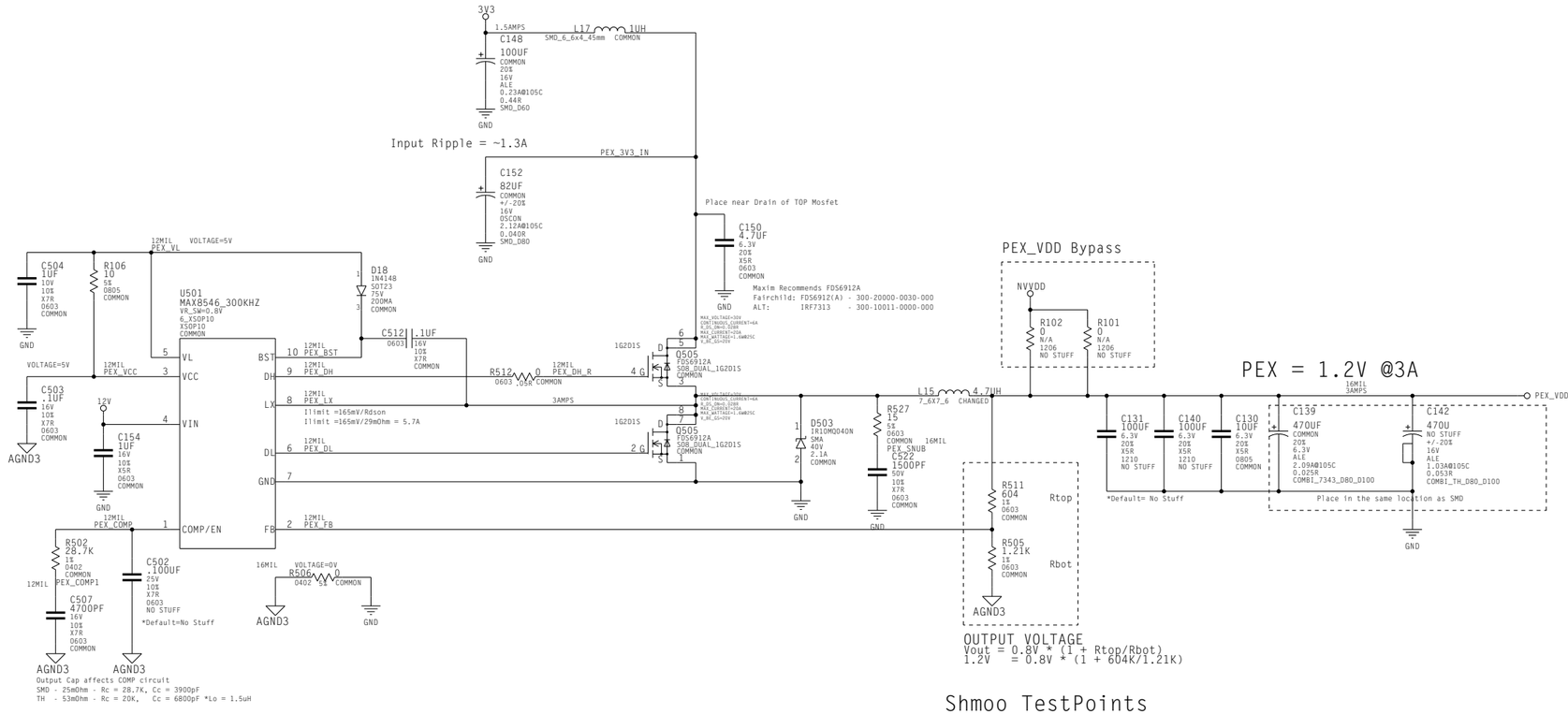
PLACE WITHIN 2cm AREA

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	Power Supply V: FBVTT

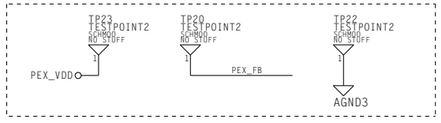
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	27 OF 37
NAME	JLAM	DATE	19-AUG-2004

28 Power Supply VI: PEX



Shmoo TestPoints



PLACE WITHIN 2cm AREA

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	Power Supply VI: PEX

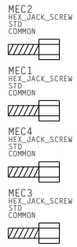
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	28 OF 37
NAME	JLAM	DATE	19-AUG-2004

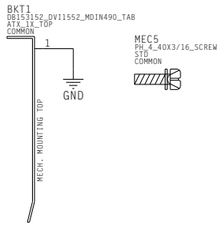
29 Mechanical: Bracket/Thermal Solution

Brackets:
151-10001-0006-000 DVI,DVI,MDIN (text - 1-South, 2-North)
151-10001-0006-001 DB15,DVI,MDIN
151-10001-0006-002 DVI,DB15,MDIN
151-10001-0006-003 DB15,DB15,MDIN (text - 1-South, 2-North)

Connector Screws

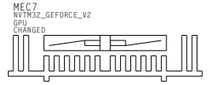


Bracket Screw



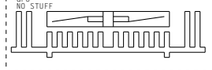
Heatsink

095-20000-0033-000 - NVTM32



Alternate Heatsink

095-00021-0013-000 - NVTM4+



ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	Mechanical: Bracket/Thermal Solution

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	29 OF 37
NAME	JLAM	DATE	19-AUG-2004

*** Signal Cross-Reference for the entire design ***

```
5V_POLY          23.1G 23.1G<
7115_XIN         17.1G< 17.2C
7115_XOUT        17.1G< 17.2C
BST1             25.4B< 26.2B>
BUFRST*          17.3A< 20.5F>
CHROMAIN         16.5H> 17.2A<
COMP1_NVVDD      25.4B< 26.4B>
COUT             16.1F< 16.4C< 19.4F>
CVBSYIN          16.5C> 17.1A<
CVBS_PBOUT       16.1F< 16.4C< 19.5F>
CVBS_YOUT        16.1F< 16.4C 16.4G
DACA_BLUE        13.3C 13.5A<
DACA_BLUE_DVI    13.3G> 15.2F<
DACA_GREEN       13.3C 13.5A<
DACA_GREEN_DVI   13.3G> 15.2F<
DACA_HS_DVI      13.2G> 15.2F<
DACA_I2C_SCL_DVI  13.1G> 15.2F<
DACA_I2C_SDA_DVI  13.2G> 15.2F<
DACA_RED         13.3C 13.5A<
DACA_RED_DVI     13.3G> 15.2F<
DACA_VDD         13.3B 13.5A<
DACA_VS_DVI      13.3G> 15.2F<
DACC_BLUE        14.3C 14.5A<
DACC_BLUE_DVI    14.3G> 15.4F<
DACC_GREEN       14.3C 14.5A<
DACC_GREEN_DVI   14.3G> 15.4F<
DACC_HS_DVI      14.2G> 15.4F<
DACC_I2C_SCL_DVI  14.1G> 15.4F<
DACC_I2C_SDA_DVI  14.2G> 15.4F<
DACC_RED         14.3C 14.5A<
DACC_RED_DVI     14.3G> 15.4F<
DACC_VDD         14.3B 14.5A<
DACC_VS_DVI      14.3G> 15.4F<
DH1              25.4B> 26.2B<
DISP_PLLVDD      20.1G<
DL1              25.4B> 26.2B<
FB1_NVVDD        25.4B< 26.4B> 26.5B
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FBBD<9>          3.2F 7.4D 7.4F
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FBBDQM<2>        3.3F 7.4B 7.4E 7.5F
FBBDQM<3>        3.4F 7.4B 7.4E 7.5F
FBBDQM<4>        3.4F 7.4B 7.5C 7.5G
FBBDQM<5>        3.4F 7.4B 7.5D 7.5G
FBBDQM<6>        3.4F 7.4B 7.5E 7.5G
FBBDQM<7>        3.4F 7.4B 7.5E 7.5G
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FBBDQS<7..0>     3.1E<> 7.1G<> 7.4B<>
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FBBDQS<2>        3.4F 7.4B 7.4E 7.5F
FBBDQS<3>        3.4F 7.4B 7.4E 7.5F
FBBDQS<4>        3.4F 7.4B 7.5C 7.5G
FBBDQS<5>        3.4F 7.4B 7.5D 7.5G
FBBDQS<6>        3.4F 7.4B 7.5E 7.5G
FBBDQS<7>        3.4F 7.5B 7.5E 7.5G
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FBB_CLKO*        3.2H> 7.1G< 7.2B<
FBB_CLK1         3.2H> 7.1G< 7.2D<
FBB_CLK1*        3.2H> 7.1G< 7.2D<
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FBB_CMD<15>      3.2G 7.1B 7.1E 7.2G
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FBCD<41>         4.3B 9.4G 9.5D
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FBCD<57>         4.3B 9.4G 9.5E
FBCD<58>         4.3B 9.4G 9.5E
FBCD<59>         4.3B 9.4G 9.5E
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FBCD<62>         4.3B 9.4G 9.5E
FBCD<63>         4.3B 9.5E 9.5G
FBCDQM<0>        4.3B 9.4B 9.4C 9.5F
FBCDQM<7..0>     4.1A> 9.1G<> 9.4B<>
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FBCDQM<2>        4.3B 9.4B 9.4E 9.5F
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FBCDQM<4>        4.4B 9.4B 9.5C 9.5G
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FBCDQM<6>        4.4B 9.4B 9.5E 9.5G
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FBCDQS<7>        4.4B 9.5B 9.5E 9.5G
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ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	30 OF 37
NAME	JLAM	DATE	19-AUG-2004

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FBC_CMD<16>	4.2C 9.1B 9.1E 9.2G
FBC_CMD<17>	4.2C 9.1B 9.1E 9.2F
FBC_CMD<18>	4.2C 9.2B 9.2E 9.2G
FBC_CMD<19>	4.2C 9.1B 9.1E 9.2G
FBC_CMD<20>	4.2C 9.1B 9.1E 9.2G
FBC_CMD<21>	4.2C 9.1B 9.1E 9.2G
FBC_CMD<22>	4.2C 9.1B 9.1F
FBC_CMD<23>	4.2C 9.1B 9.1E 9.2G
FBC_CMD<24>	4.2C 9.1B 9.1F
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FBDD<7>	4.1F 11.4C 11.4F
FBDD<8>	4.1F 11.4D 11.4F
FBDD<9>	4.2F 11.4D 11.4F
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FBDD<46>	4.3F 11.4G 11.5D
FBDD<47>	4.3F 11.4G 11.5D
FBDD<48>	4.3F 11.4G 11.5E
FBDD<49>	4.3F 11.4G 11.5E
FBDD<50>	4.3F 11.4G 11.5E
FBDD<51>	4.3F 11.4G 11.5E
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FBDD<57>	4.3F 11.4G 11.5E

FBDD<58>	4.3F 11.4G 11.5E
FBDD<59>	4.3F 11.4G 11.5E
FBDD<60>	4.3F 11.4G 11.5E
FBDD<61>	4.3F 11.4G 11.5E
FBDD<62>	4.3F 11.4G 11.5E
FBDD<63>	4.3F 11.5E 11.5G
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FBDDQM<2>	4.3F 11.4B 11.4E 11.5F
FBDDQM<3>	4.4F 11.4B 11.4E 11.5F
FBDDQM<4>	4.4F 11.4B 11.5C 11.5G
FBDDQM<5>	4.4F 11.4B 11.5D 11.5G
FBDDQM<6>	4.4F 11.4B 11.5E 11.5G
FBDDQM<7>	4.4F 11.4B 11.5E 11.5G
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FBDDQS<4>	4.4F 11.4B 11.5C 11.5G
FBDDQS<5>	4.4F 11.4B 11.5D 11.5G
FBDDQS<6>	4.4F 11.4B 11.5E 11.5G
FBDDQS<7>	4.4F 11.5B 11.5E 11.5G
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FBD_CLKO*	4.2H> 11.1G< 11.2B<
FBD_CLK1	4.2H> 11.1G< 11.2D<
FBD_CLK1*	4.2H> 11.1G< 11.2D<
FBD_CMD<0>	4.1G 11.1B 11.1F
FBD_CMD<25..0>	11.1B< 11.1D 11.1G<
FBD_CMD<0..26>	4.1H>
FBD_CMD<1>	4.1G 11.1B 11.1E 11.2F
FBD_CMD<2>	4.1G 11.1B 11.1F
FBD_CMD<3>	4.1G 11.1B 11.1E 11.2F
FBD_CMD<4>	4.1G 11.1E 11.1G
FBD_CMD<5>	4.1G 11.1E 11.1G
FBD_CMD<6>	4.1G 11.1E 11.1G
FBD_CMD<7>	4.1G 11.1B 11.1E 11.2F
FBD_CMD<8>	4.1G 11.1B 11.1E 11.2F
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FBD_CMD<13>	4.2G 11.1E 11.1G
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FBD_CMD<16>	4.2G 11.1B 11.1E 11.2G
FBD_CMD<17>	4.2G 11.1B 11.1E 11.2F
FBD_CMD<18>	4.2G 11.2B 11.2E 11.2F
FBD_CMD<19>	4.2G 11.1B 11.1E 11.2G
FBD_CMD<20>	4.2G 11.1B 11.1E 11.2G
FBD_CMD<21>	4.2G 11.1B 11.1E 11.2G
FBD_CMD<22>	4.2G 11.1B 11.1F
FBD_CMD<23>	4.2G 11.1B 11.1E 11.2G
FBD_CMD<24>	4.2G 11.1B 11.1F
FBD_CMD<25>	4.2G 11.1B 11.1E 11.2G
FBD_PLLVDD	4.1G< 4.4G
GPIO0_DVI_A_HPD	15.3D> 20.2E<
GPIO1_DVI_C_HPD	15.5D> 20.2E<
GPIO4_PVA_IRQ	16.2F> 20.3E<
GPIO5_VSEL0	20.3E> 26.4E<
GPIO6_VSEL1	20.3E> 26.5E<
GPIO10_480P	19.5B< 20.3E>
GPIO12_EXT12V_PRSNT	20.3D< 20.3D< 20.3F 25.2E>
I2CC_SCL	16.2D 16.2G 16.3H< 17.3A< 20.1F> 20.2C<
I2CC_SDA	16.2D 16.2G 16.4H<> 17.3A<> 20.1F<> 20.2C<>
ICS9DB202_CLK_OUT	19.1H> 19.2D
ICS9DB202_CLK_OUT*	19.1H> 19.2D
ICS9DB202_CLK_OUT_R	19.1H> 19.2E
ICS9DB202_CLK_OUT_R*	19.1H> 19.2E
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IFPA_IOVDD	15.1G<
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IFPCD_PLLVDD	15.1G< 15.3B
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ILIM1	25.3B< 26.2B>
LX1	25.4B< 26.2B>
MIOAD<0>	21.5A 21.5B
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MIOAD<2>	21.2A 21.2B
MIOAD<3>	21.2A 21.2B
MIOAD<4>	21.2A 21.2B
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MIOAD<6>	21.5A
MIOAD<7>	21.2A
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MIOA_DE	18.1G< 18.2D 18.2F
MIOA_HSYNC	18.1G< 18.3G< 18.3G< 21.3A> 21.3B
MIOA_VDDQ	18.1G< 18.2B
MIOA_VSYNC	18.1G< 18.2F 18.3D
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MIOBD<7..0>	17.3A>
MIOBD<11..0>	18.4E<
MIOBD<12..0>	21.2A>
MIOBD<23..0>	18.2G<
MIOBD<1>	21.3A 21.3B
MIOBD<2>	21.2A
MIOBD<3>	21.3A
MIOBD<4>	21.2A
MIOBD<5>	21.2A
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MIOBD<8>	18.4D 21.3A 21.3B
MIOBD<9>	18.4D 21.3A 21.3B
MIOBD<10>	18.4D 21.3A 21.3B
MIOBD<11>	18.4D 21.4A 21.4B
MIOBD<12>	21.4A
MIOBD_R<23..0>	18.1G<
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MIOB_CLKOUT*	18.2G< 18.2G<
MIOB_CLKOUT_R	18.2G< 18.2G<
MIOB_CLKOUT_R*	18.2G< 18.2G<
MIOB_DE	18.2G<
MIOB_DE_R	18.1G<
MIOB_HSYNC	18.2G<
MIOB_HSYNC_R	18.1G<
MIOB_VDDQ	18.1G< 18.4B
MIOB_VSYNC	18.2G<
MIOB_VSYNC_R	18.1G<
NVVDD_SENSE	22.3G> 26.3D<
NV_BOOT1	26.1G<>
NV_BOOT2	26.1G<>
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PEX_RX2	2.2B 2.2H>
PEX_RX2*	2.2B 2.2H>
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PEX_RX4*	2.2H> 2.3B
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PEX_RX8*	2.3H> 2.4B
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ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	31 OF 37
NAME	JLAM	DATE	19-AUG-2004

VIPPCLK	17.4A> 18.5E<> 19.4B<
VTTGEN	22.5A<

ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	32 OF 37
NAME	JLAM	DATE	19-AUG-2004

*** Part Cross-Reference for the entire design ***

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ASSEMBLY	NV41 256MB 8Mx32 DDR1 VGA+DVI-I+S-Video-Out PCI-E Desktop - DELL SKU
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NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10260-0004-300		
ID	design	PAGE	33 OF 37
NAME	JLAM	DATE	19-AUG-2004

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RP595	R_PAK	11
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RP597	R_PAK	11
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RP599	R_PAK	11
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TP10	TESTPOINT	27
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TP12	TESTPOINT	24
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TP20	TESTPOINT	28
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TP502	TESTPOINT	23
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U15	U_MEM_SD_DDR_X32	7
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U18	U_MEM_SD_DDR_X32	5
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U505	U_VREG_3PIN	23
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