

TABLE OF CONTENTS

Page	Description	Page	Description

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11062-base-100	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKL0001	600-11062-0001-100	GF106-300 1536MB 64Mx16 BGA100 1dDQ3, HDMI/VGA/DVI-I
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>


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ASSEMBLY	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Table of Contents

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2701 SAN TOMAS EXPRESSWAY

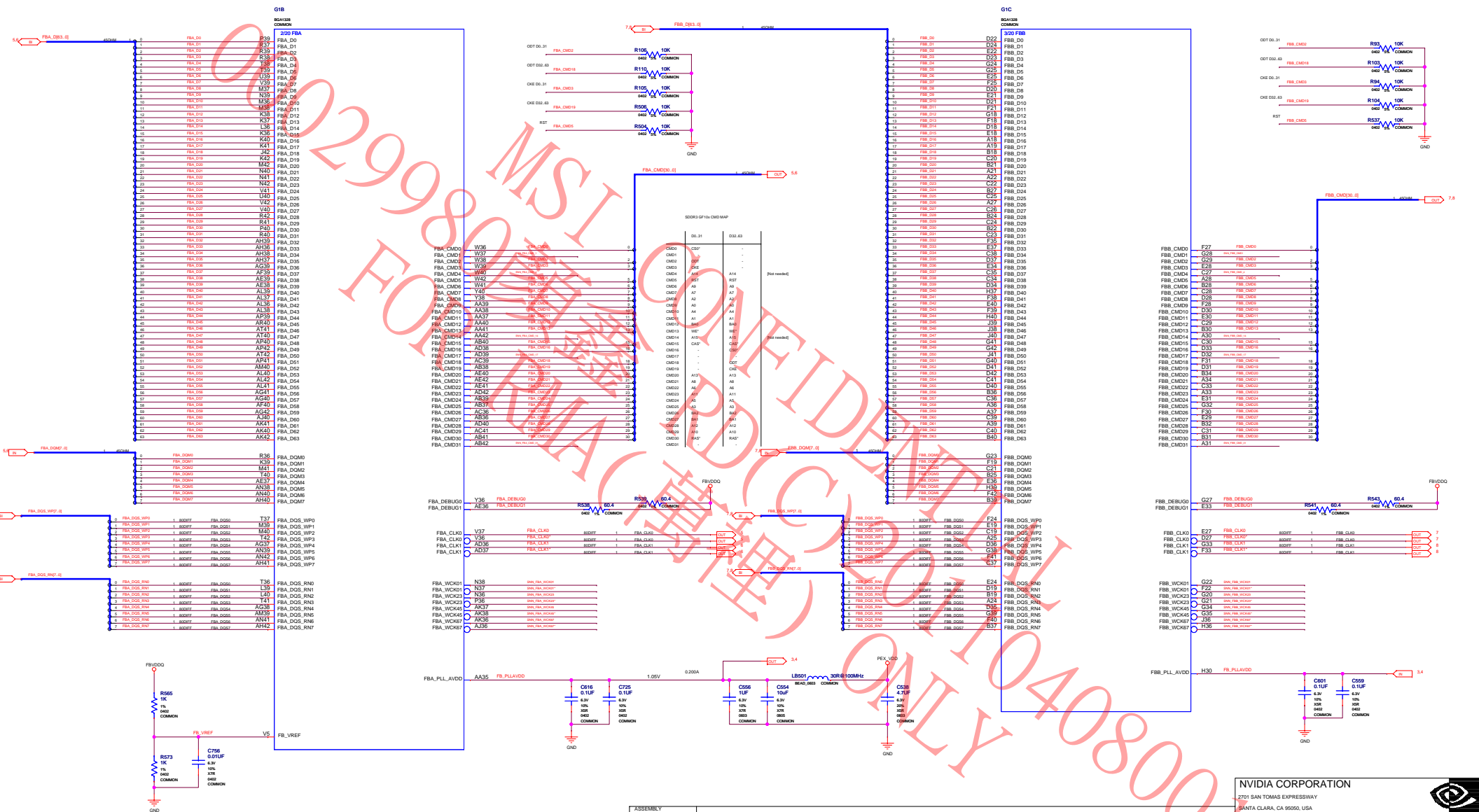
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NV_PN	600-11062-base-100
PCB REV	P1062-B00
BOM REV	A
PAGE	
DATE	06-APR-2010

MS7S(Andy)

MEMORY: GPU FB Partition A and B



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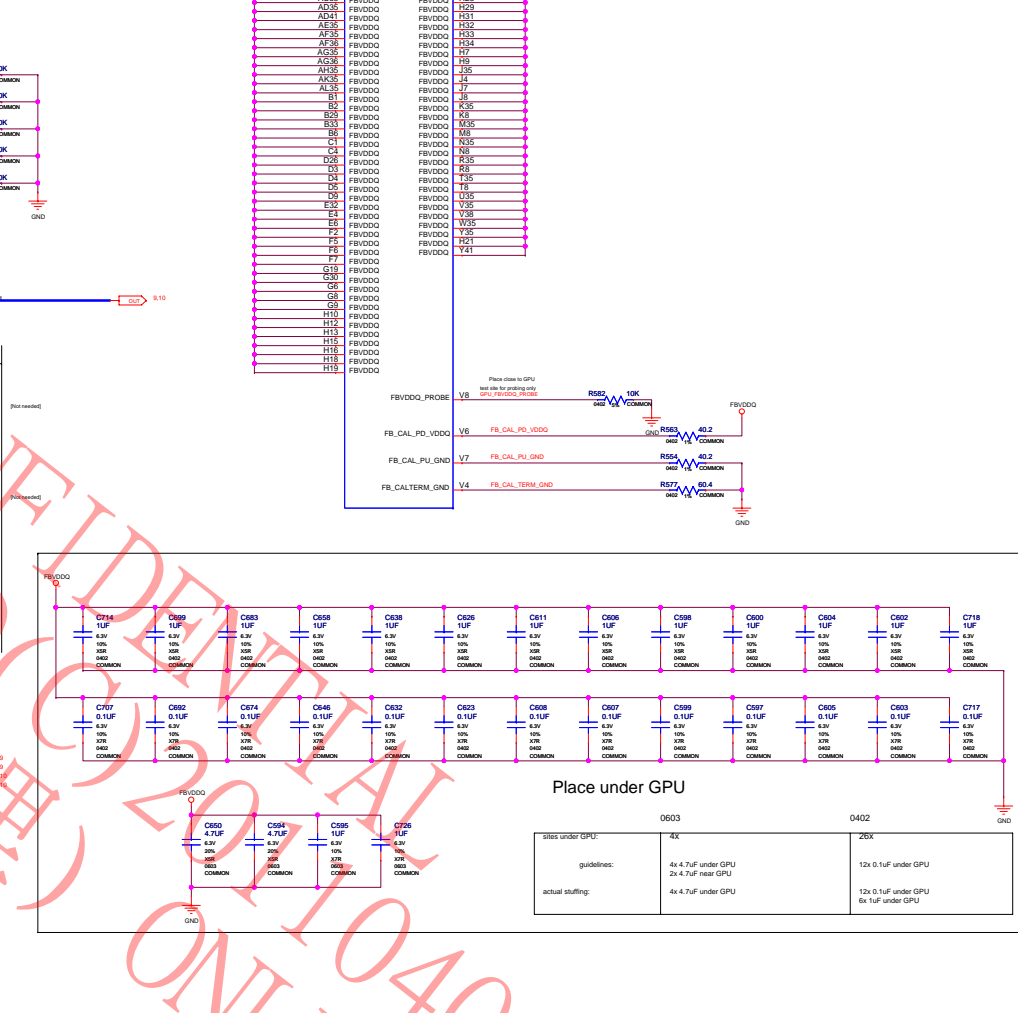
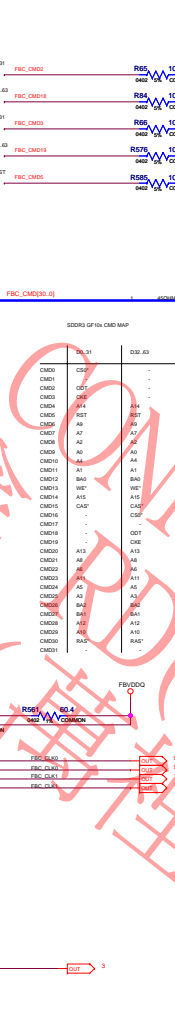
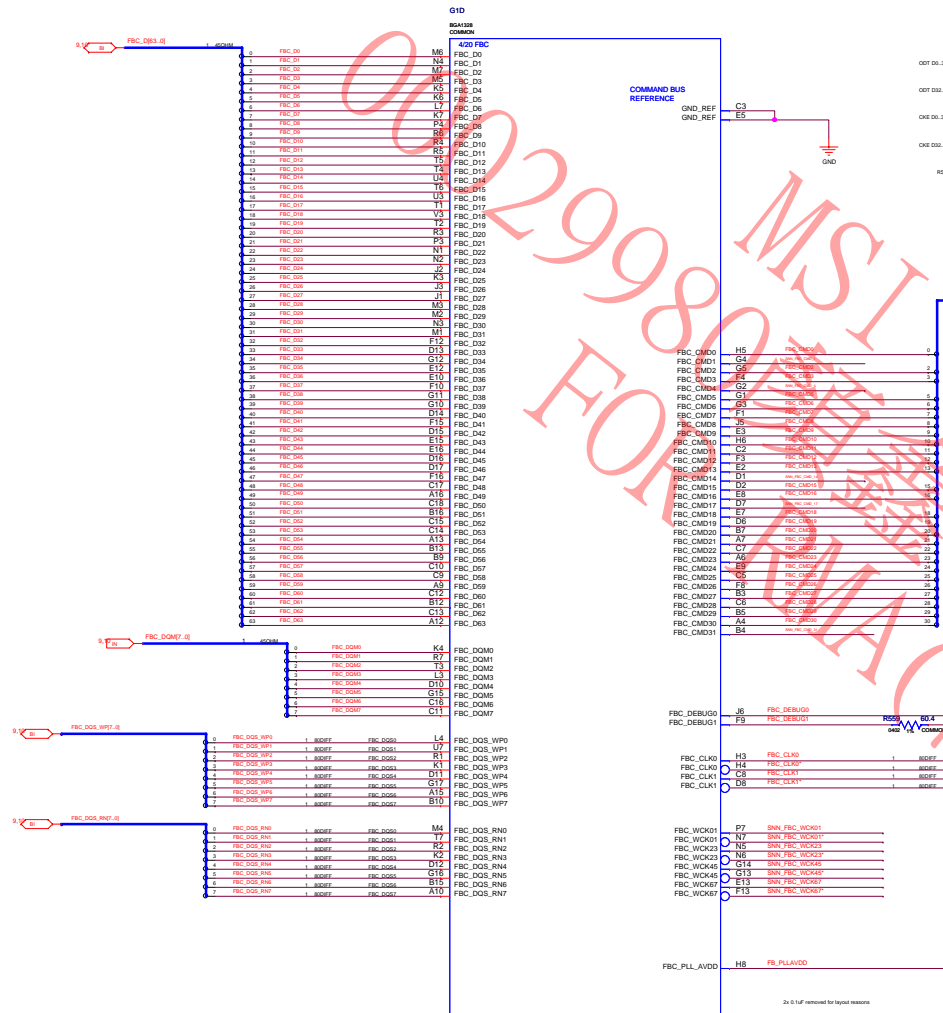
ASSEMBLY
PAGE DETAIL
GPU FB PARTITION A AND B

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NV_PN	600-11062-base-100
PCB REV	P1002-2800
BOM REV	A
PAGE	1
DATE	06-APR-2010

MS7S(Andy)

MEMORY: GPU FB Partition C AND GPU FB Decap

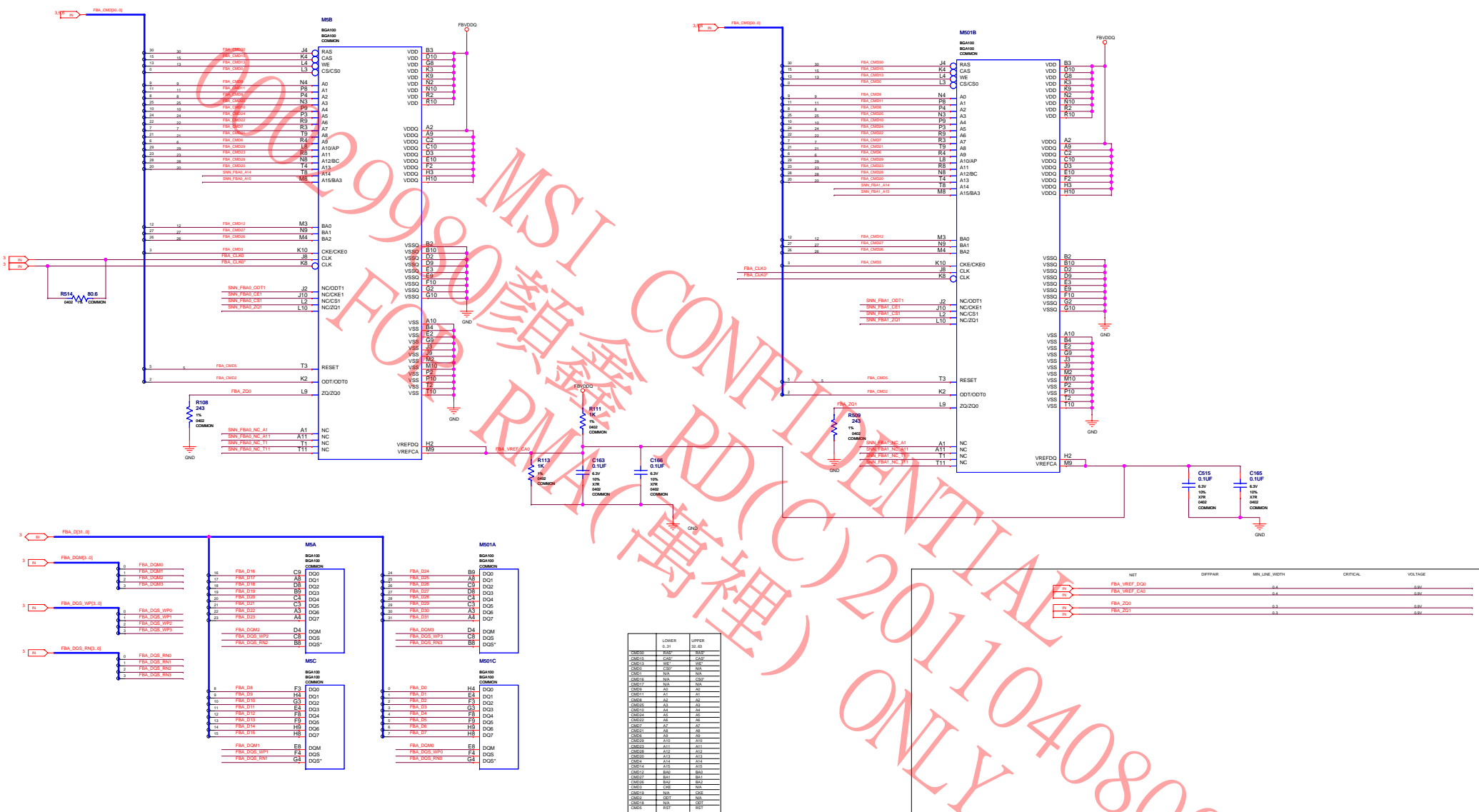


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ASSEMBLY P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO.3 STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL GPU FB Partition C and GPU FB Decap

NVIDIA CORPORATION	
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NV_PN	600-11062-base-100
PCB REV	P1062-2000
BOM REV	A
PAGE	
DATE	06-APR-2010


Memory Lower Partition A



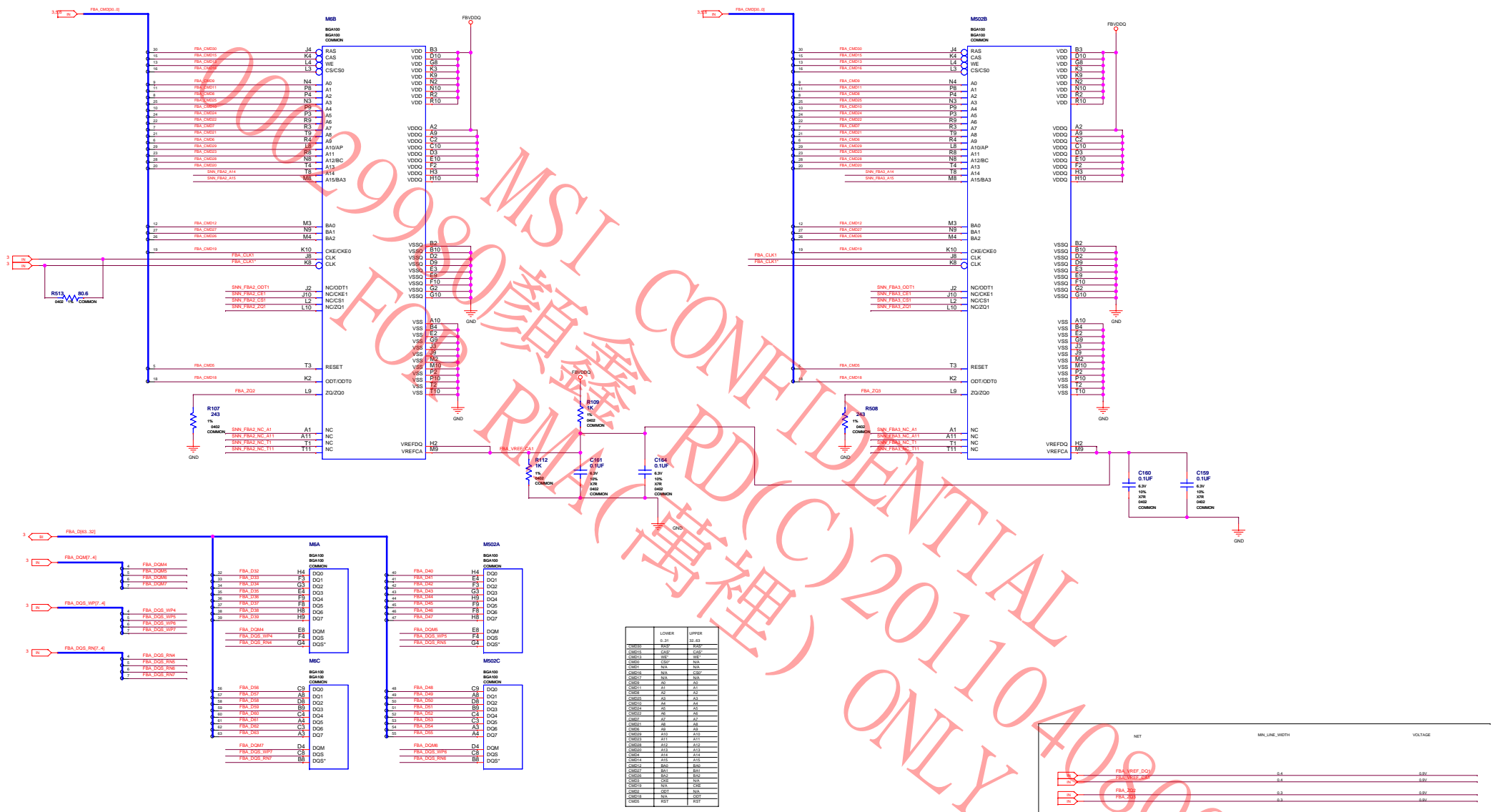
	LOWER 0.31	UPPER 32.65
CM001	CM001	CM001
CM010	CAS2	CAS2
CM013	WB1	WB1
CM014	WB2	WB2
CM01	N/A	N/A
CM012	N/A	CM012
CM015	N/A	N/A
CM06	AS	AS
CM07	A1	A1
CM08	A2	A2
CM020	A3	A3
CM021	A4	A4
CM024	AS	AS
CM025	AS	AS
CM026	AS	AS
CM027	A7	A7
CM028	AS	AS
CM029	AS	AS
CM029	AT02	AT02
CM029	A11	A11
CM029	AT02	A12
CM029	AT03	A13
CM029	AT04	A14
CM014	AT05	AT05
CM012	BA0	BA0
CM013	BA1	BA1
CM019	BA2	BA2
CM013	CBE	N/A
CM019	N/A	CBE
CM02	CO07	N/A
CM019	N/A	CO07
CM025	REST	REST

ASSEMBLY	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Memory Lower Partition A

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NV_PN	600-11062-base-100		
PCB REV	P1062-B00	PAGE	
BOM REV	A	DATE	06-APR-2010

Memory Upper Partition A



	LOWER	UPPER
	A-31	32-83
CAGE06	WAS	WAS
CAGE05	CAS	CAS
CAGE04	WEC	WEC
CAGE03	CDF	N/A
CAGE02	N/A	N/A
CAGE01	N/A	CDF
CAGE07	N/A	N/A
CAGE08	A2	A2
CAGE11	A1	A1
CAGE09	A2	A2
CAGE10	A3	A3
CAGE020	A8	A8
CAGE14	A5	A5
CAGE022	A6	A6
CAGE07	A7	A7
CAGE01	A8	A8
CAGE05	A9	A9
CAGE09	A10	A10
CAGE11	A11	A11
CAGE08	A12	A12
CAGE020	A13	A13
CAGE04	A14	A14
CAGE04	A15	A15
CAGE02	B05	B05
CAGE01	B01	B01
CAGE05	B02	BA2
CAGE08	N/A	N/A
CAGE19	N/A	CNE
CAGE08	N/A	COT
CAGE01	RYT	RYT

	NET	MIN_LINE_WIDTH	VOLTAGE
U1	FBA_REF_DOJ FBA_REF_DOJ	0.4	0.0V
U2		0.4	0.0V
U3	FBA_302	0.3	0.0V
U4	FBA_403	0.3	0.0V

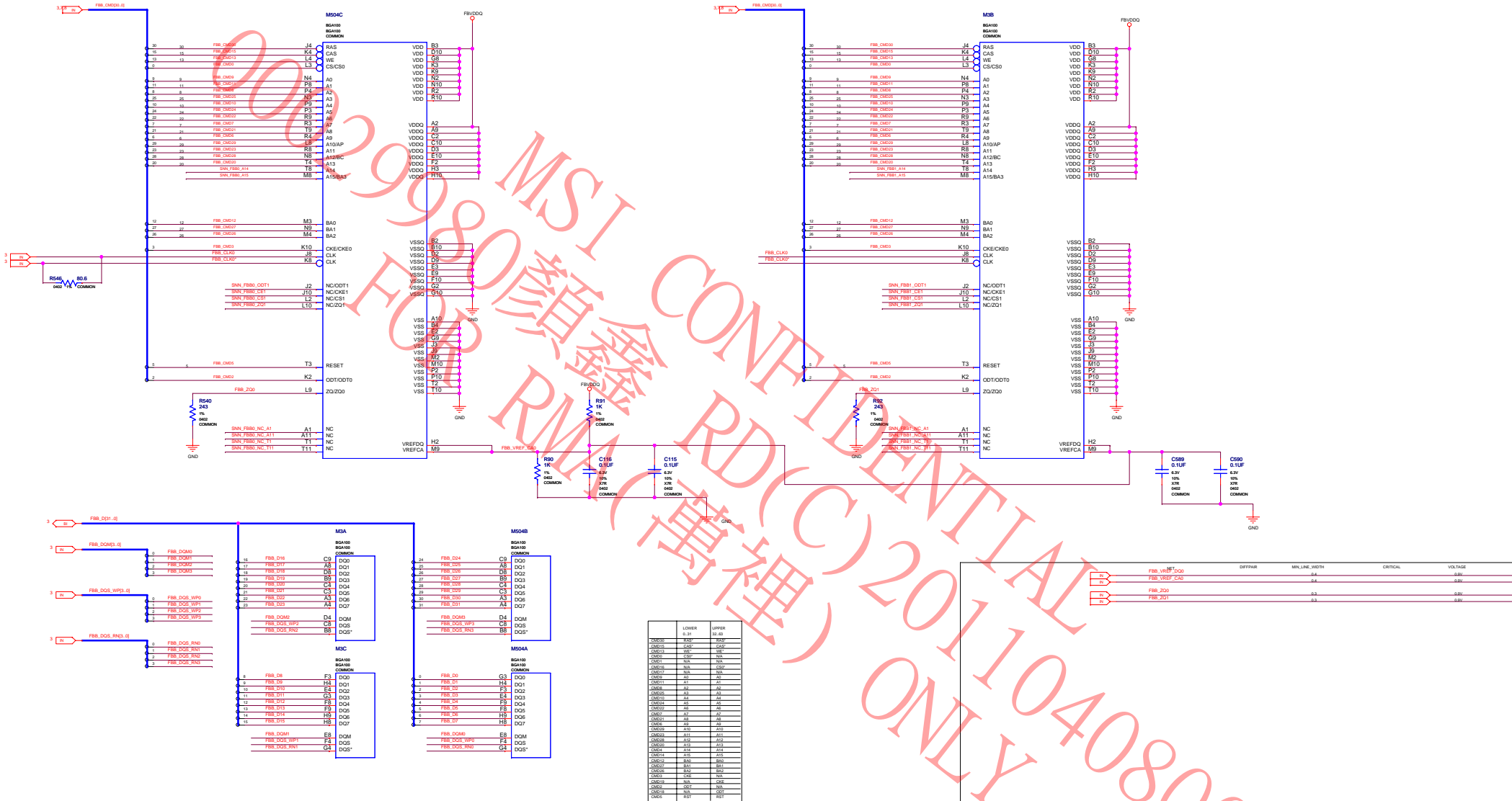
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IN USE ON THIS PAGE	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Memory Upper Partition A

NV_PN	600-11062-base-100		
PCB REV	P1062-B00	PAGE	
BOM REV	A	DATE	06-APR-2010

Memory Lower Partition B



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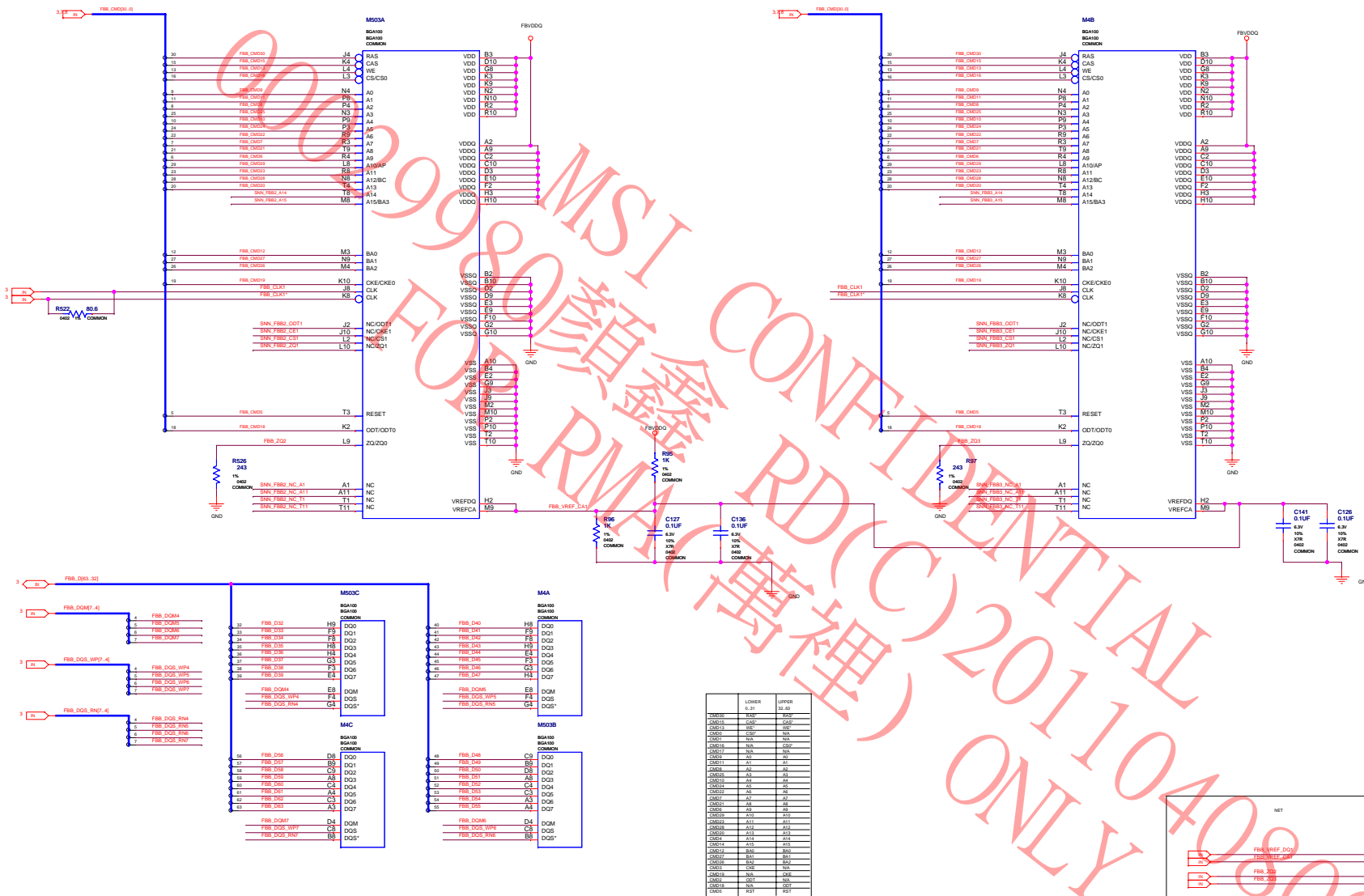
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NV_PN	600-11062-base-100
PCB REV	P1062-300
BOM REV	A

PAGE	1
DATE	06/APR/2010

MS7S(Andy)

Memory Upper Partition B



	LOWER	UPPER
CM005	8-21	32-41
CM006	WRT	WRT
CM010	CAS ²	CAS ²
CM013	WR ²	WR ²
CM014	WR	WR
CM017	N/A	N/A
CM018	N/A	N/A
CM019	N/A	N/A
CM020	AS	AS
CM021	A1	A1
CM022	A2	A2
CM023	A3	A3
CM024	A4	A4
CM024	AS	AS
CM025	AS	AS
CM027	A7	A7
CM028	AS	AS
CM029	A8	A8
CM030	AS	AS
CM032	AT0	AT0
CM032	A11	A11
CM032	A12	A12
CM032	A13	A13
CM032	A14	A14
CM034	A15	A15
CM042	BA0	BA0
CM043	BA1	BA1
CM048	BA2	BA2
CM049	C0E	C0E
CM050	C0E	C0E
CM052	C0T	C0T
CM053	C0N	C0T
CM055	RST	RST

	NET	MIN. LINE WIDTH	VOLTAGE
	FRS (REF. DO)	0.4	28V
	ESG (REF. DO)	0.4	30V
10	FRS_100	0.3	28V
10	FRS_100	0.3	30V

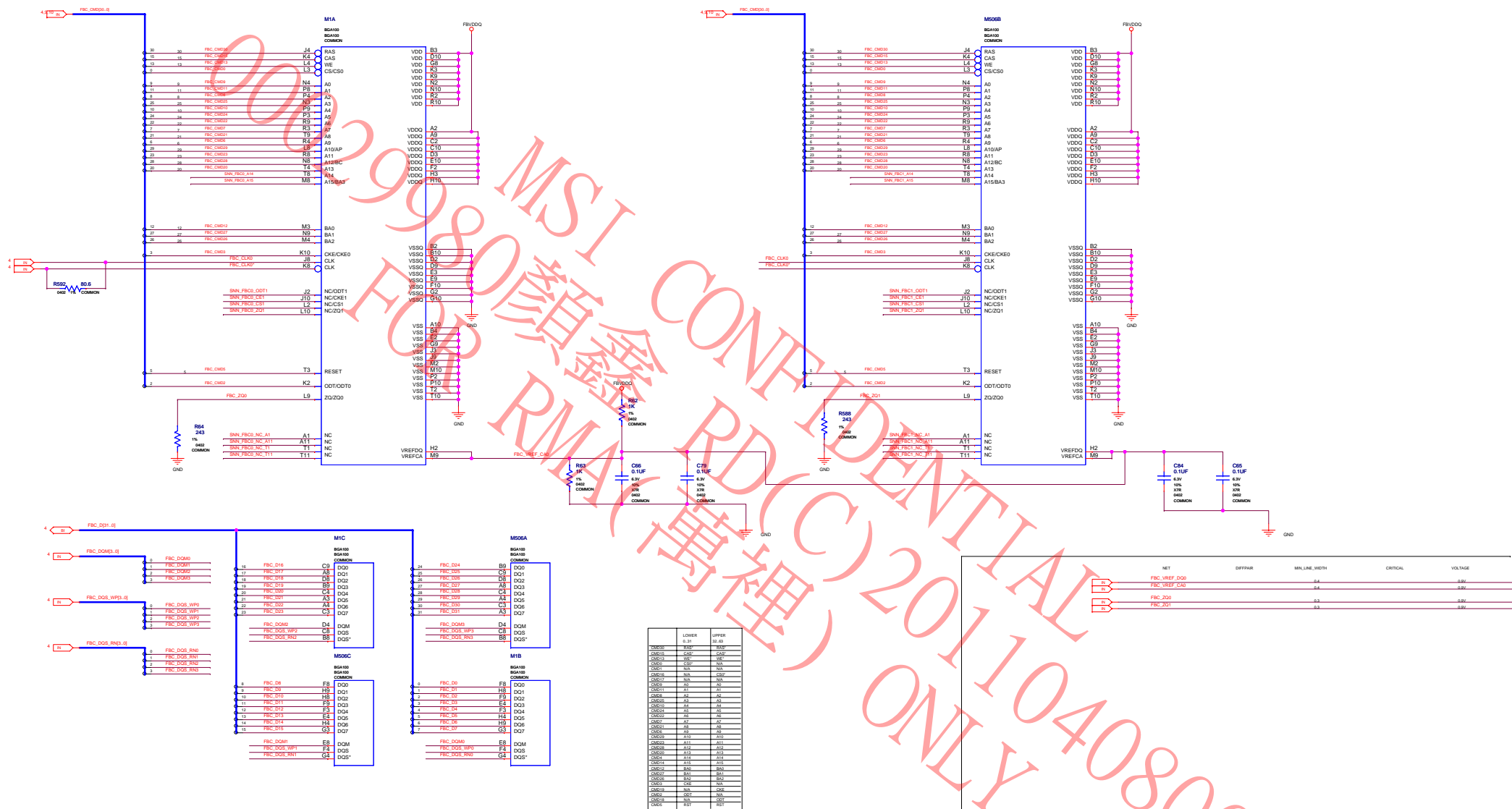
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NV_PN	600-11062-base-100		
PCB REV	P1062-B00	PAGE	
RCM REV	A	DATE	06 APR 2010

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Memory Lower Partition C



	LOWER 6-31	UPPER 32-63
Q000	Q000	Q000
Q0013	CAS2	CAS2
Q0014	WE1	WE1
Q0015	C002	C002
Q0017	N/A	N/A
Q0018	N/A	C002
Q0019	N/A	N/A
Q0020	AS	AS
Q0021	A1	A1
Q0022	A2	A2
Q0023	A3	A3
Q0024	A12	A12
Q0025	A5	A5
Q0026	A5	A5
Q0027	A5	A5
Q0028	A7	A7
Q0029	A8	A8
Q0030	A9	A9
Q0031	A10	A10
Q0032	A11	A11
Q0033	A12	A12
Q0034	A13	A13
Q0035	A15	A15
Q0036	A14	A14
Q0037	B60	B60
Q0038	B41	B41
Q0039	B42	B42
Q0040	C8E	N/A
Q0041	N/A	C8E
Q0042	Q007	N/A
Q0043	N/A	Q007
Q0044	Q017	Q017

NET	DIFFPAIR	MIN_LINE_WIDTH	CRITICAL	VOLTAGE
B1	FBC_VREF_DQ0	0.4		0.9V
B1	FBC_VREF_CA0	0.4		0.9V
B1	FBC_Z00	0.3		0.9V
B1	FBC_Z01	0.3		0.9V

IN USE ON

ASSEMBLY	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Memory Lower Partition C

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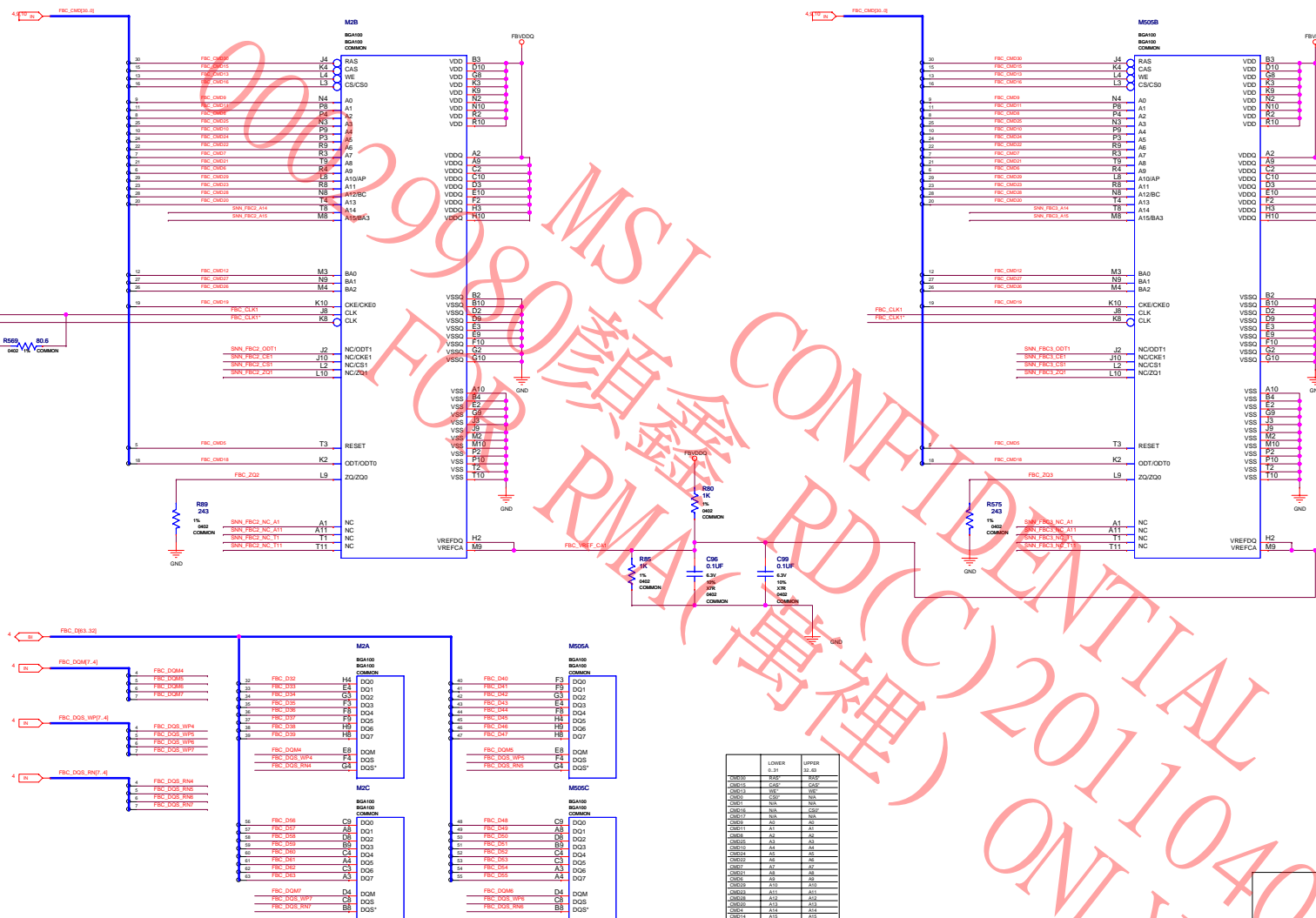
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NV_PN	600-11062-base-100		
PCB REV	P1062-B00	PAGE	
BOM REV	A	DATE	06-APR-2010

Memory Upper Partition C



	LOWER	UPPER
MEM01	0-31	32-63
MEM02	0-31	32-63
MEM03	0-31	32-63
MEM04	0-31	32-63
MEM05	0-31	32-63
MEM06	0-31	32-63
MEM07	0-31	32-63
MEM08	0-31	32-63
MEM09	0-31	32-63
MEM10	0-31	32-63
MEM11	0-31	32-63
MEM12	0-31	32-63
MEM13	0-31	32-63
MEM14	0-31	32-63
MEM15	0-31	32-63
MEM16	0-31	32-63
MEM17	0-31	32-63
MEM18	0-31	32-63
MEM19	0-31	32-63
MEM20	0-31	32-63
MEM21	0-31	32-63
MEM22	0-31	32-63
MEM23	0-31	32-63
MEM24	0-31	32-63
MEM25	0-31	32-63
MEM26	0-31	32-63
MEM27	0-31	32-63
MEM28	0-31	32-63
MEM29	0-31	32-63
MEM30	0-31	32-63
MEM31	0-31	32-63
MEM32	0-31	32-63
MEM33	0-31	32-63
MEM34	0-31	32-63
MEM35	0-31	32-63
MEM36	0-31	32-63
MEM37	0-31	32-63
MEM38	0-31	32-63
MEM39	0-31	32-63
MEM40	0-31	32-63
MEM41	0-31	32-63
MEM42	0-31	32-63
MEM43	0-31	32-63
MEM44	0-31	32-63
MEM45	0-31	32-63
MEM46	0-31	32-63
MEM47	0-31	32-63
MEM48	0-31	32-63
MEM49	0-31	32-63
MEM50	0-31	32-63
MEM51	0-31	32-63
MEM52	0-31	32-63
MEM53	0-31	32-63
MEM54	0-31	32-63
MEM55	0-31	32-63
MEM56	0-31	32-63
MEM57	0-31	32-63
MEM58	0-31	32-63
MEM59	0-31	32-63
MEM60	0-31	32-63
MEM61	0-31	32-63
MEM62	0-31	32-63
MEM63	0-31	32-63
MEM64	0-31	32-63
MEM65	0-31	32-63
MEM66	0-31	32-63
MEM67	0-31	32-63
MEM68	0-31	32-63
MEM69	0-31	32-63
MEM70	0-31	32-63
MEM71	0-31	32-63
MEM72	0-31	32-63
MEM73	0-31	32-63
MEM74	0-31	32-63
MEM75	0-31	32-63
MEM76	0-31	32-63
MEM77	0-31	32-63
MEM78	0-31	32-63
MEM79	0-31	32-63
MEM80	0-31	32-63
MEM81	0-31	32-63
MEM82	0-31	32-63
MEM83	0-31	32-63
MEM84	0-31	32-63
MEM85	0-31	32-63
MEM86	0-31	32-63
MEM87	0-31	32-63
MEM88	0-31	32-63
MEM89	0-31	32-63
MEM90	0-31	32-63
MEM91	0-31	32-63
MEM92	0-31	32-63
MEM93	0-31	32-63
MEM94	0-31	32-63
MEM95	0-31	32-63
MEM96	0-31	32-63
MEM97	0-31	32-63
MEM98	0-31	32-63
MEM99	0-31	32-63
MEM100	0-31	32-63

IN USE ON THIS PAGE

ASSEMBLY P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO.310FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL Memory Upper Partition C

NET MIN LINE WIDTH VOLTAGE

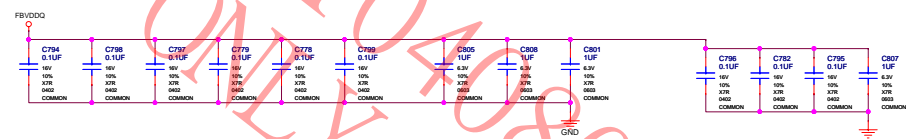
FBC_VREF_D01	0.4	0.9V
FBC_VREF_D01	0.4	0.9V
FBC_VREF_D01	0.4	0.9V
FBC_VREF_D01	0.4	0.9V
FBC_VREF_D01	0.4	0.9V

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NV_PN	600-11062-base-100
PCB REV	P1062-2000
BOM REV	A

PAGE 06/04/2010

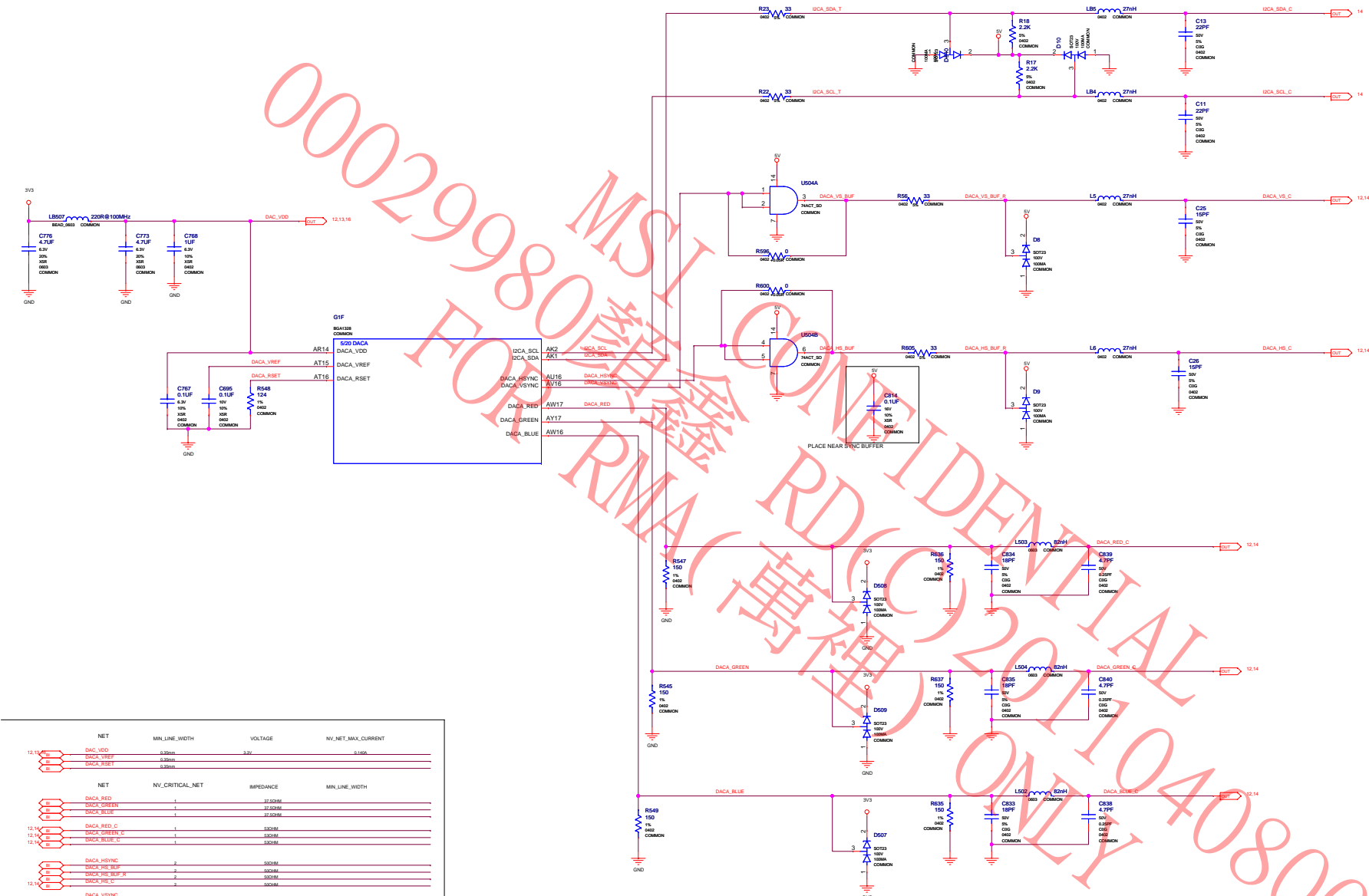
Memory FBVDD/Q Decoupling



BOM REV	A	DATE	06-APR-2010
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DACA for South DVI Interface

DACA RGB-FILTER



NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
12.14	DACA_VDD	0.35mm	3.3V
12.14	DACA_VREF	0.35mm	0.15A
12.14	DACA_RSET	0.35mm	

NET	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
12.14	DACA_RED	1	37.028M
12.14	DACA_GREEN	1	37.028M
12.14	DACA_BLUE	1	37.028M
12.14	DACA_RED_C	1	500M
12.14	DACA_GREEN_C	1	500M
12.14	DACA_BLUE_C	1	500M
12.14	DACA_HSYNC	2	500M
12.14	DACA_VS_BUF_X	2	500M
12.14	DACA_VS_BUF_Y	2	500M
12.14	DACA_VS_BUF_Z	2	500M
12.14	DACA_VS_BUF_W	2	500M
12.14	DACA_VS_BUF_V	2	500M
12.14	DACA_VS_BUF_U	2	500M
12.14	DACA_VS_BUF_T	2	500M
12.14	DACA_VS_BUF_S	2	500M
12.14	DACA_VS_BUF_R	2	500M
12.14	DACA_VS_BUF_Q	2	500M
12.14	DACA_VS_BUF_P	2	500M
12.14	DACA_VS_BUF_O	2	500M
12.14	DACA_VS_BUF_N	2	500M
12.14	DACA_VS_BUF_M	2	500M
12.14	DACA_VS_BUF_L	2	500M
12.14	DACA_VS_BUF_K	2	500M
12.14	DACA_VS_BUF_J	2	500M
12.14	DACA_VS_BUF_I	2	500M
12.14	DACA_VS_BUF_H	2	500M
12.14	DACA_VS_BUF_G	2	500M
12.14	DACA_VS_BUF_F	2	500M
12.14	DACA_VS_BUF_E	2	500M
12.14	DACA_VS_BUF_D	2	500M
12.14	DACA_VS_BUF_C	2	500M
12.14	DACA_VS_BUF_B	2	500M
12.14	DACA_VS_BUF_A	2	500M

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PAGE DETAIL	DACA Interface to DVI

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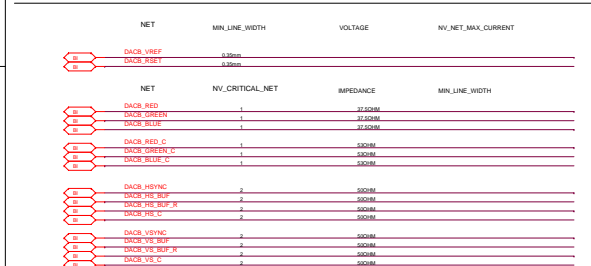
PAGE


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DATE

06/04/2010

DACB RGB-FILTER



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BOM REV	A	DATE	06-APR-2010

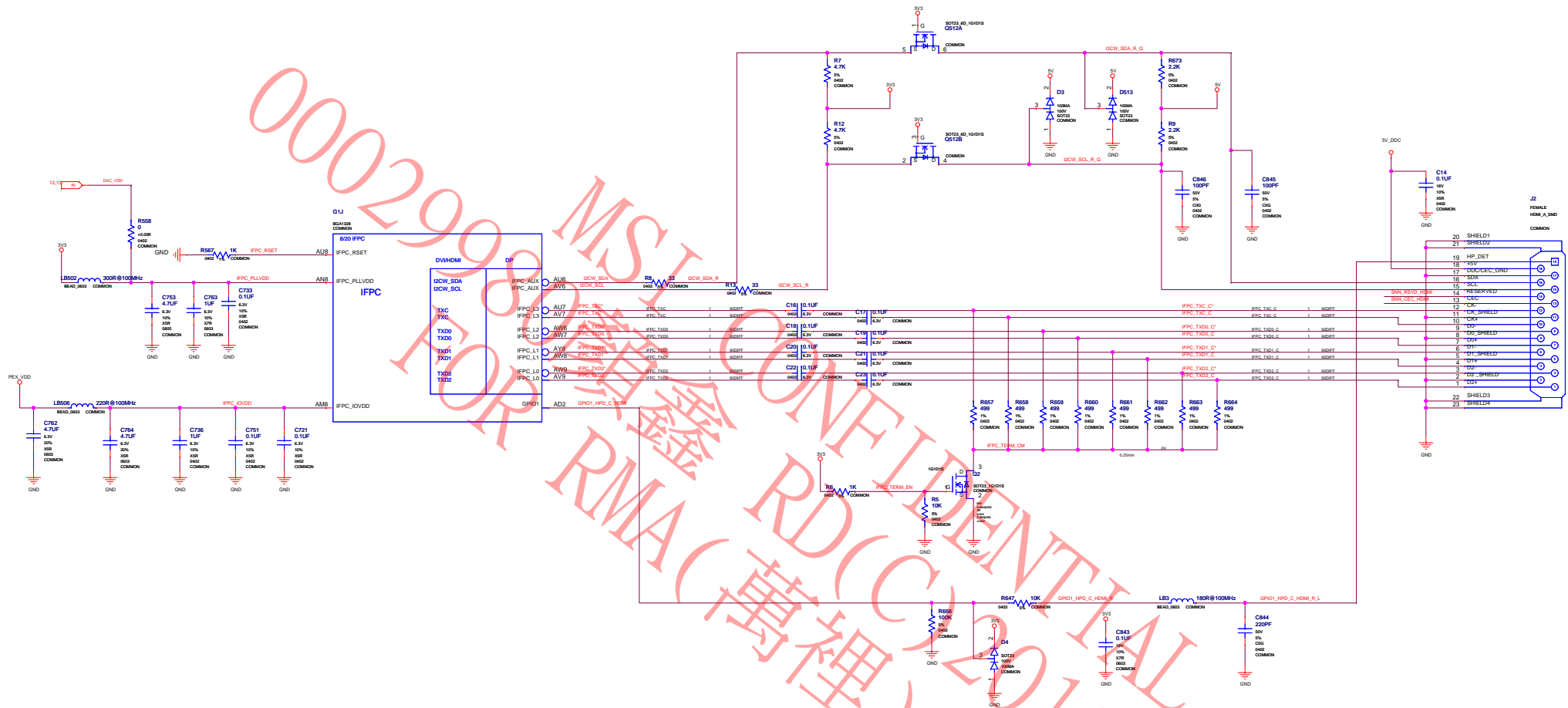
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IFP C Interface -- HDMI, North



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PAGE DETAIL	IFPC Interface -- HDMI

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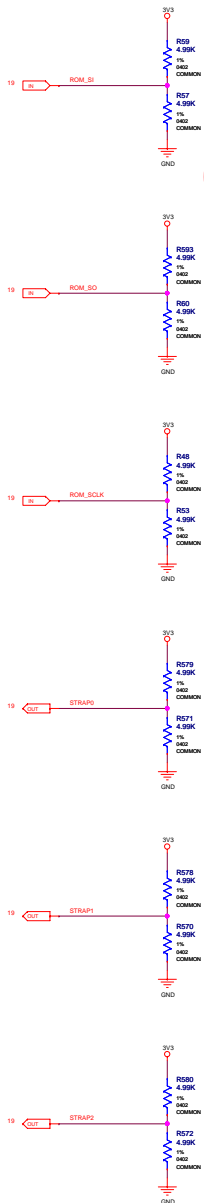


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Strap Configuration

GF106-300: 0x0DC0



ROM_S0	VGA_DEVICE SMB_ALT_ADDR PU_0_B4H_SIZE VCLK_43T	LSb MSb	1: VGA_DEVICE 0: Disabled(POR) 0: Disabled(POR) 0: Disabled(POR)	PU	PD 15K
ROM_S1	ROM_OFFSET		0000:16 100-bit Sensing 0000:16 100-bit Sensing 0000:16 100-bit Sensing 0000:16 100-bit Sensing	20K PD 10K PD 10K PD 5K PD	20K
ROM_SCLX	PEL_PEL_EN_TERMINA SLOT_CLK_CONFIG SMBALTEACH PCL_DEV0_EXT	LSb MSb	0: Disabled (POR) 1: GPU and MCH COMMON REFCLK 1: MCH COMMON IS PRESENT 0: PCLDEV0EN		35K
STRAP0	USER_BUTTON		0: Disabled (POR)		5K
STRAP1	3GIO_FUNC0FS_LUT_PORT0		0: Disabled (POR)		5K
STRAP2	GPU_DEVICE		0: Disabled (POR)		5K

Multi-level Strap Resistor Values	
Strap PU(PD) Value (kOhm)	
0 PU 5	
1 PU 10	
2 PU 15	
3 PU 20	
4 PU 25	
5 PU 30	
6 PU 35	
7 PU 40	
8 PU 45	
9 PU 50	
10 PU 55	
11 PU 60	
12 PU 65	
13 PU 70	
14 PU 75	
15 PU 80	

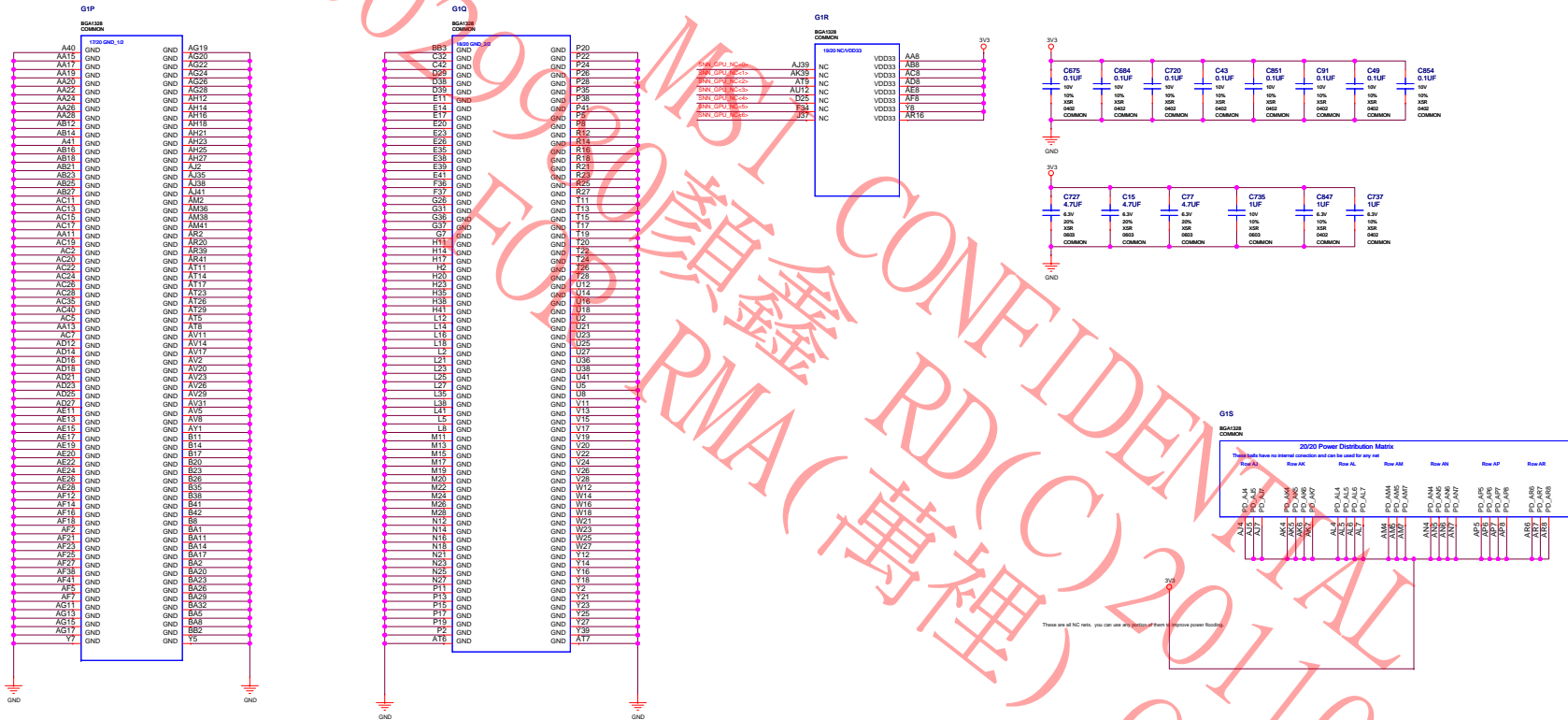
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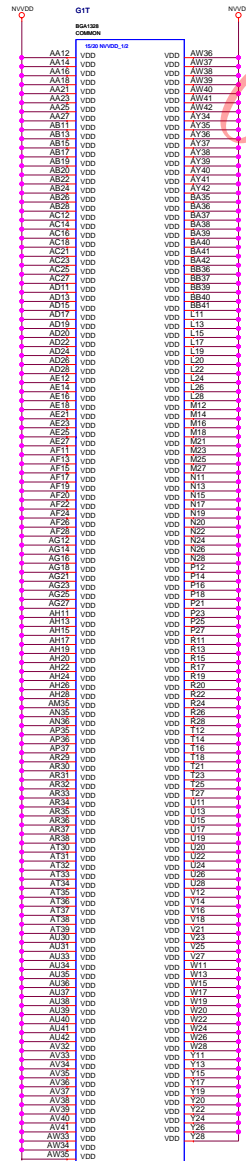
PWR and GND Signals



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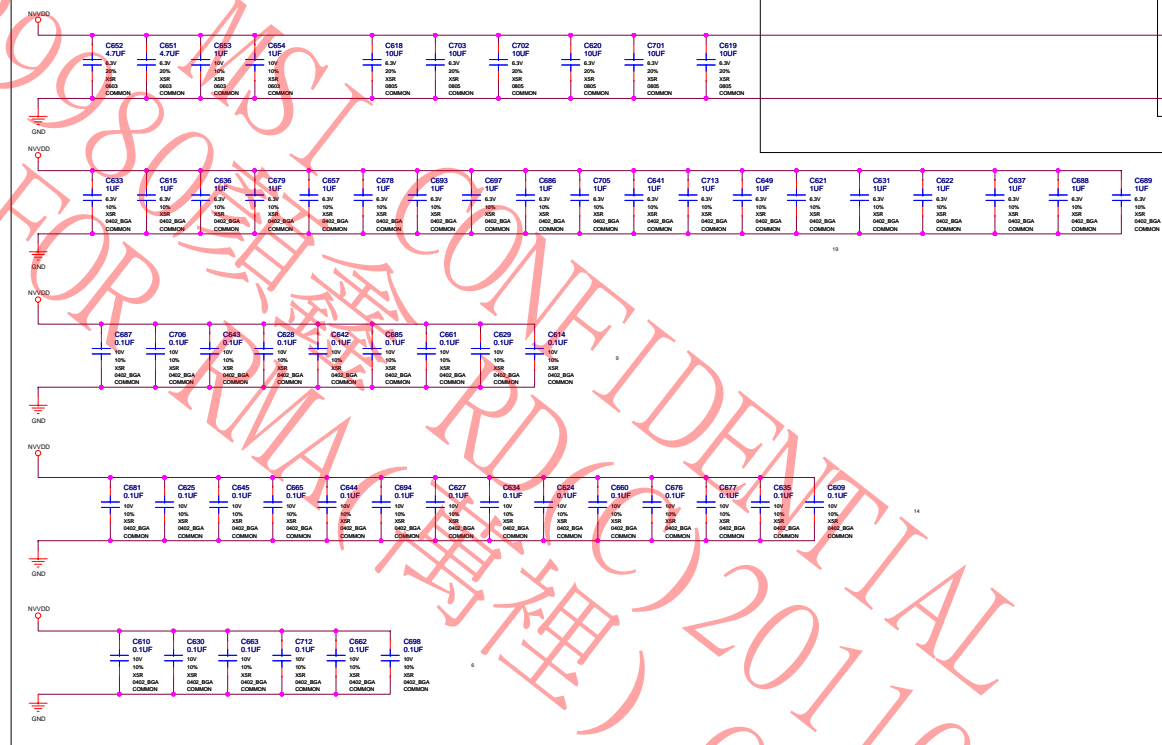
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BOM REV	A	DATE	06-APR-2010

NVVDD Decoupling



	0805	0603	0402
Sites placed under GPU:	6x		4x
Stuff under GPU:	5x 10uF 1x 22uF		2x 4.7uF (2x unused)
			15x 1uF 16x 0.1uF (17x unused)

Place under GPU



Place in NVVDD corridor



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PAGE DETAIL	NVDD Decoupling

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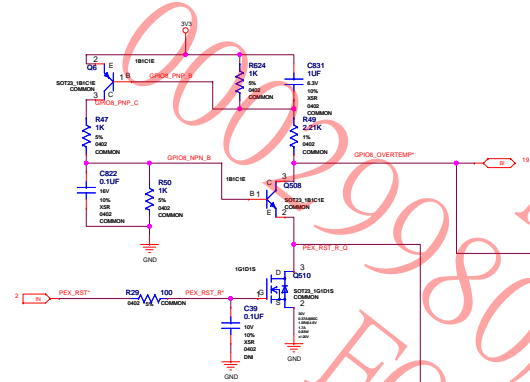


NV_PN	600-11062-base-100		
PCB REV	P1062-B00	PAGE	
BOM REV	A	DATE	06-APR-2010

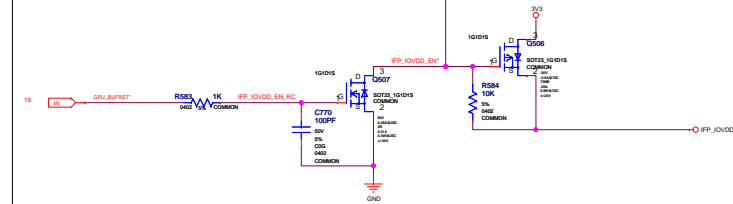
MSJS(Andy)

Power Sequencing, Thermal Protection, and IFP_IOVDD Power Supply

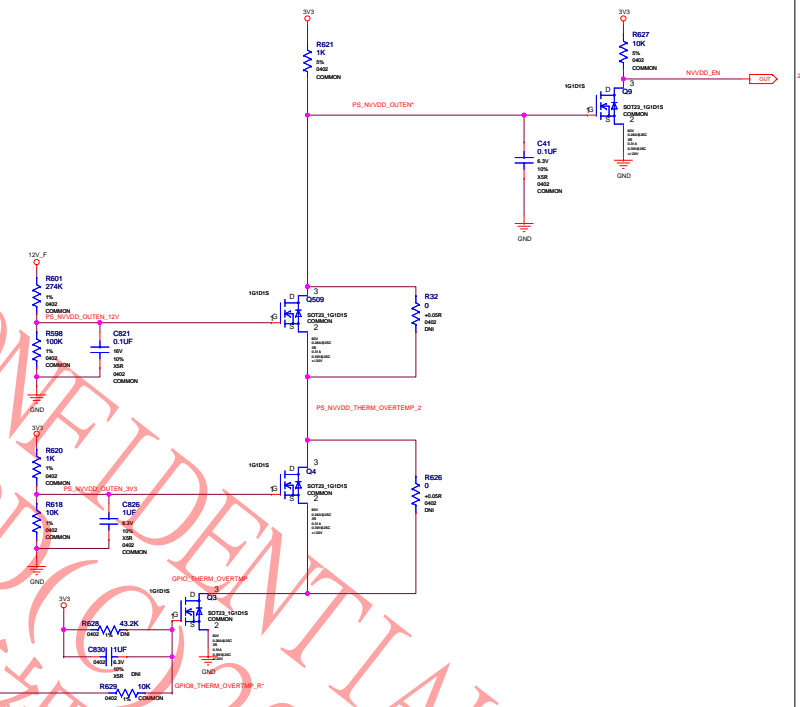
Thermal Protection (latch)



IFP_IOVDD Backdrive Prevention



NVVDD Sequence



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PAGE DETAIL	Backdrive Protection, Thermal Protection, and Power Sequencing

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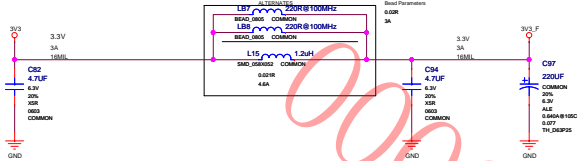
NV_PN	600-11062-base-100		
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PS I: 3V3, 12V, and 12V_EXT Power Supply Filter, 5V, DDC VOLTAGE

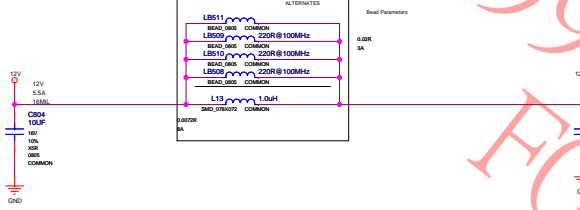
3V3 Power Supply Filter

3V3_F = 3.3V @ 2.4A

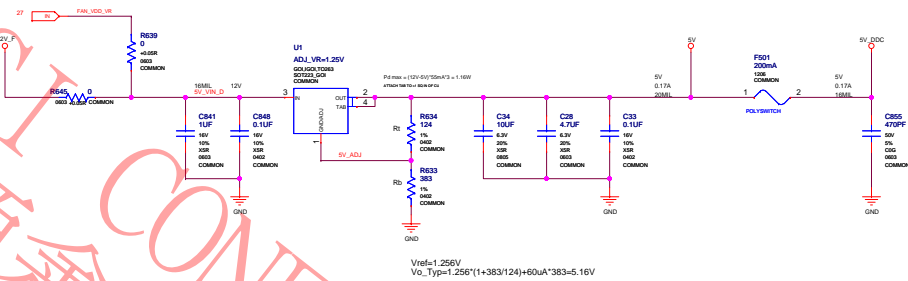


12V Power Supply Filter

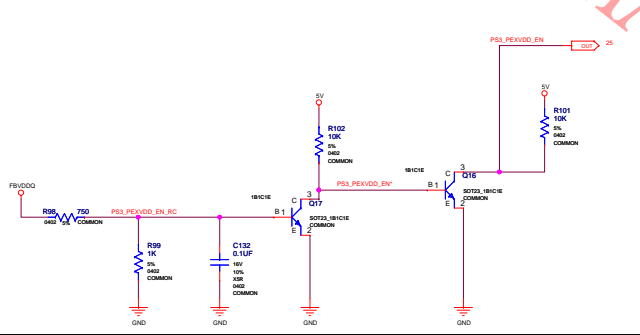
12V_F = 12V @ 5.5A



5V POWER SUPPLY, DDC POWER



PEXVDD ENABLE

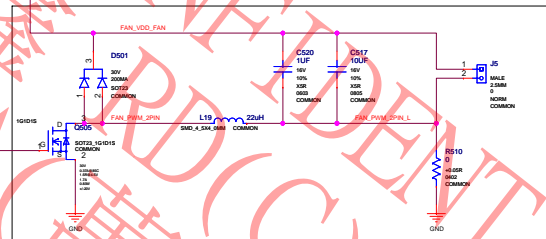
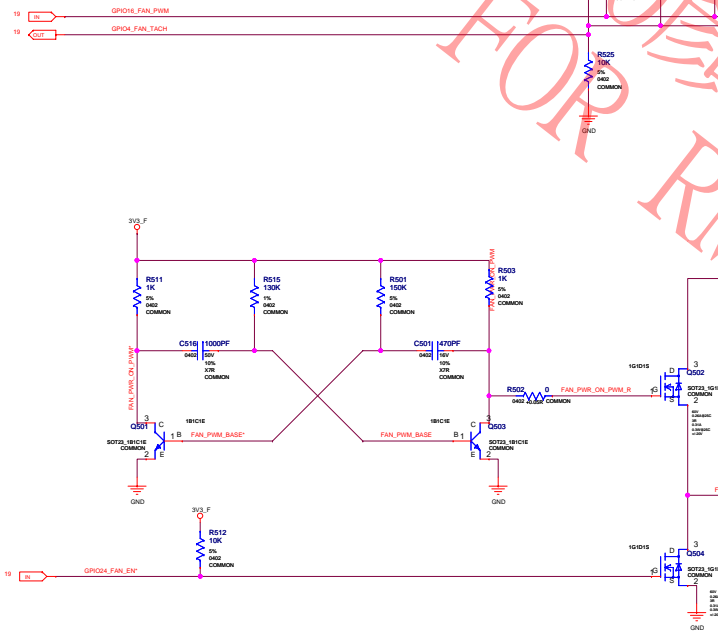
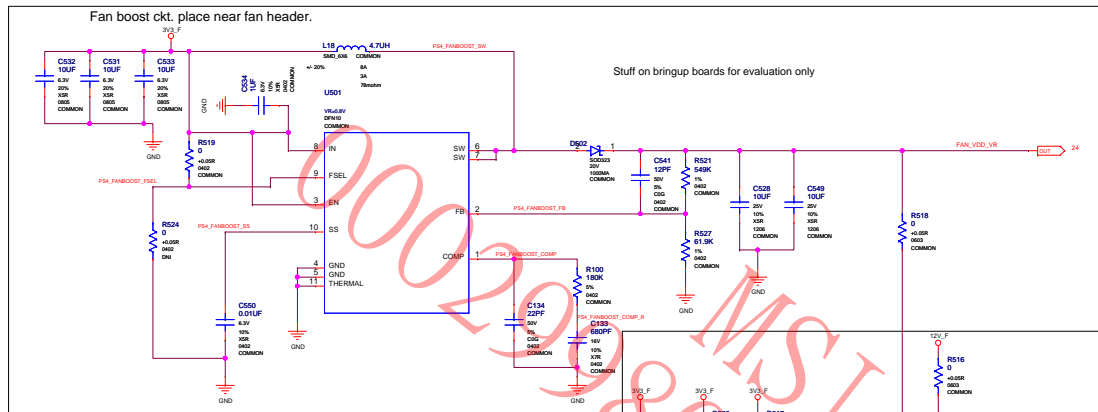


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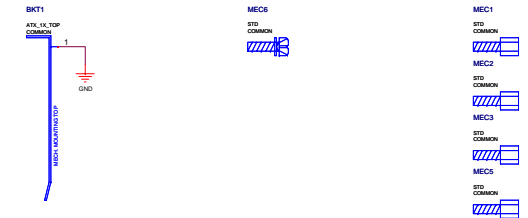
ASSEMBLY	PI062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PEXVDD ENABLE, 3V3, 12V Power Supply Filter, 5V AND DDC VOLTAGE

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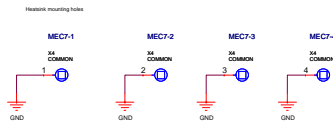
Thermal, Mechanical, and Bracket



Bracket



SPECIAL MECHANIC

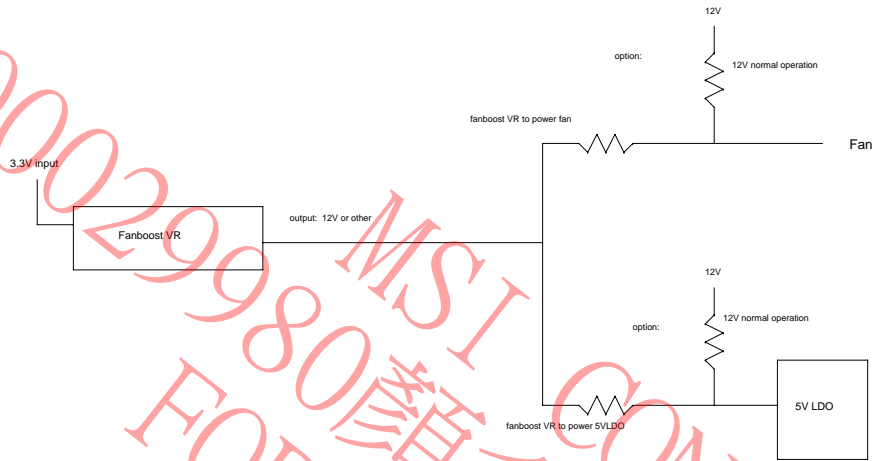


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ASSEMBLY	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Fanboost VR, multivibrator, Thermal, and Mechanical

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ASSEMBLY	P1062 BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Block diagram of 12V options for fan and 5V LDO

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PCB REV	P1062-B00	PAGE	
BOM REV	A	DATE	06-APR-2010

