P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz

PCI DEVICE ID 0x017A

HISTORY:

A00 - First Rev release

1. Fix strapping for GPU0 and GPU1 See ECO3336 and ECO3320.

A01 -

1. Added R1176 on (1.b Block hierarchy). Used to connect SPCI_AD24 to ST_IDSEL_GPU0, due to intel specifications referencing not to use AD16 (SLOT 0) because bridge may use that resource.

2. Added R1266 on (2.a PCI Edge Connector). This is used to help risetime of IRQ symbol due to excessive capacative loading on that signal.

3. Added R1177 on (2.b PCI bus bridge). This was added as option of disabling the feature which turns off the PCI clocks in stand by. This mode isn't well tested yet, this is why the resistor was added.

4. Swapped S_REQ_[3..0] buss on U100 on (2.b PCI bus bridge). This was due to a previous error in symbol for BGA for pinout causing swap on this S_REQ_[3..0] for BGA symbol only.

5. Added U903, R1264, C1531, C1532 , R1180, (changed R6) on (2.b PCI bus bridge). This is due to a bug in NV17 where input receiver on reset is not properly filtered inside asic, therefore external schmitt trigger was added.

6. Added R1178 on (2.b PCI bus bridge). Pin 102 was missing from QFP symbol, therefore causing floating input. LOCK_I pin is not being used by secondary PCI bus, however unused input needed to be terminated.

7. Added R1179 on (2.b PCI bus bridge). Pin 49 was missing from QFP symbol, therefore causing floating input., unused input needed to be terminated.

8. Added R1265 on (2.b PCI bus bridge). Pin 62 was missing from QFP symbol, according to Intel specification they needed to have pull down for NAND tree access.

9. Added pin# 125, 131 connected to 3.3V_REG on U101 (2.b PCI bus bridge). Pin 125,131 was missing from QFP symbol, Intel specification shows they needed to be connected to VCC, without connection to VCC this causes boot up issues with power supplies that have slow rise time.

10. Removed 3-pin inductors on RGB filters due to DFM issue with middle pin being plated and causing solder flow issues when installing regular 0603 inductor which is non 3-pin.

11. On page (3.g Panel), resistors R274, R277 were change from COMMON to NO_STUFF.

A02 -

1. On page (5.a NVVDD / FBVDD(Q) POWER SUPPLY), changed diode D800, D802 PCB footprint from SMDA to RECT_SMDA

PAGE OVERVIEW

[Subbom suffix] Stuffing Options	Meaning
[-000] COMMON	common components for all skus
[-010] HINT_BGA_33	Hint TBGA 33 Mhz option
[-011] HINT_BGA_66	Hint TBGA 66 Mhz option
[-012] HINT_INTEL_PQFP	Hint PQFP SE33P or Intel 21152 option
[-020] RGB_PROT	ESD diodes on RGB/sync signals
[-030] NV_32MB_INF	Nvidia's 32 MB per GPU option using Infineon Memory
[-031] NV_32MB_SAM	Nvidia's 32 MB per GPU option using Samsung Memory
[-040] SC1775	SC1175 Switch Mode Controller option
[-041] IRU3047	IRU3047 Switch Mode Controller option
[-050] NO_PWR_INDUCTOR	Option to bypass power supply inductor
[-051] PWR_INDUCTOR	Option to fit inductor on 5V supply from PCI connector
[-052] IND_PWR_CAP	Option to fit capacitor on Input supply
[-053] ANALOG_REG	3.3V regulator to feed analog supplies
[-054] NO_ANALOG_REG	Bypass regulator and drive from PCI bus instead
[-055] DIGITAL_REG	3.3V regulator to feed digital ic's
[-056] NO_DIGITAL_REG	Bypass regulator and feed from PCI bus directly
[-057] NV_POWER	Special power supply components for NV configuration
[-058] Q3D_POWER	Special power supply components for Q3D configuration
[-059] BYPASS_ANALOG_REG	Bypass Analog regulator and drive A3.3 from V3.3_REG
[-060] PASSIVE_HS	Sub bom to stuff Passive Heatsinks
[-070] NO_NVSYNC	NVidia's option to bypass Quantum 3D's Nvsync logic
[-071] Q3D_NVSYNC	Quantum 3D's nVsync option
[-072] Q3D_64MB_INF	Quantum 3D's 64 MB per GPU stuffing option using Infineon
[-073] Q3D_64MB_SAM	Quantum 3D's 64 MB per GPU stuffing option using Samsung
[-080] IFP_REG	TMDS Regulator stuffing option for 2.8V supply
[-081] NO_IFP_REG	3.3V bypass to TMDS PLL net
[-999] NO_STUFF	Not Assembled

A03:
1- Fixed unnamed nets.
2- Config the bd to be 25W max by disconnected PRSNT2#
3- Added TMDS backdrive.
4- Added a FET to block 5V backdrive from both GPU when power is off.

A04:
1- Swap D805, Pin 1 and 2 WAS backwards in A03 netlist, correct on A04 netlist

140-50077-0000-A04
602-50077-0000-A04

NVIDIA Corporation
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Santa Clara, CA 95050, USA

GPU

P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz

Size: Custom | CAGE Code | DWG NO | Rev

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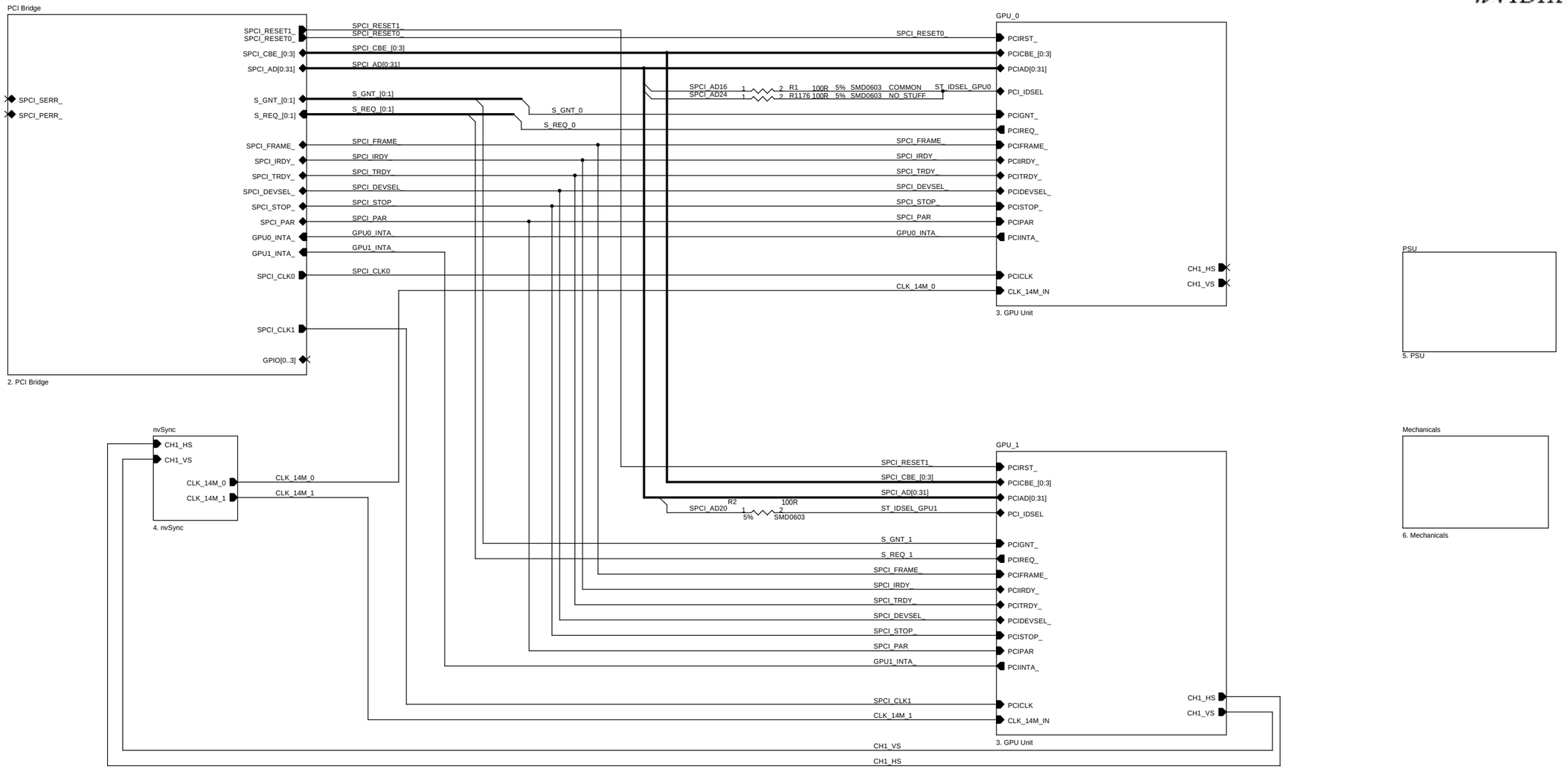
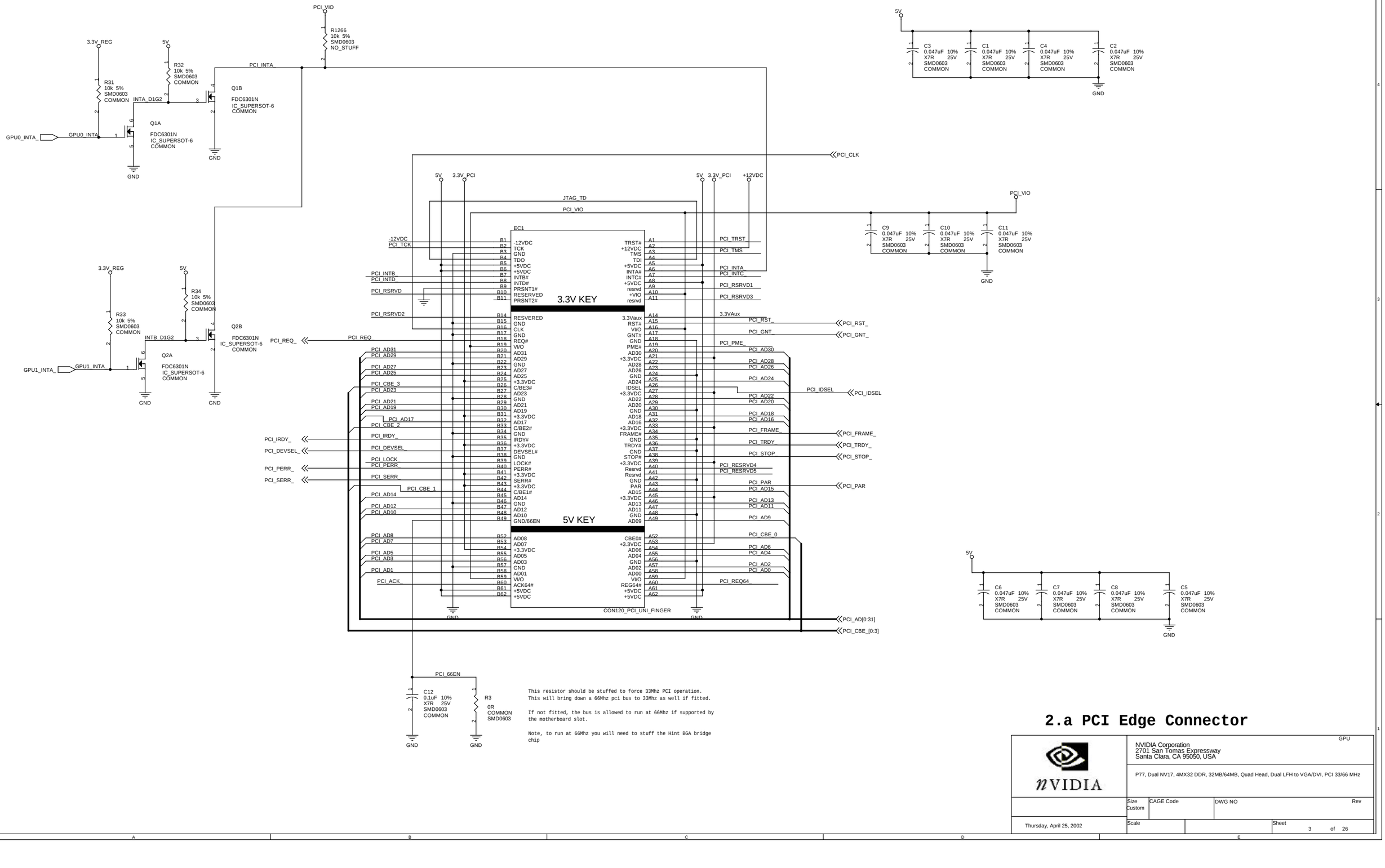
P77, Dual NV17, 4MX32 DDR, 32MB/64MB, DUAL LFH , PCI

PCI DEVICE ID 0X0=0X171 FOR NV17-128D.



1.b Block hierarchy

NVIDIA	GPU NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA
	P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz
	Size: Custom; CAGE Code; DWG NO; Rev
Thursday, April 25, 2002	Scale; Sheet: 2 of 26



2.a PCI Edge Connector

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GPU

P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz

Size	CAGE Code	DWG NO	Rev
Custom			

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Scale

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Do not use SPCI_RST from bridge chips; targeted reset as OS walks through buses will cause a reset of first device when 2nd is targeted. This can lose the settings of the first chip and result in only one chip being visible. Varies from OS to OS. Safer to use the pci rst signal buffered and level adjusted

Stuffing options are any _one_ of the following:
1/ HB1-SE33 - 160 TBGA package or
2/ HB1-SE66 - 160 TBGA package or
3/ HB1-SE33P - 160 PQFP package (Intel 21152 compat) or
4/ Intel 21152 - 160 PQFP package

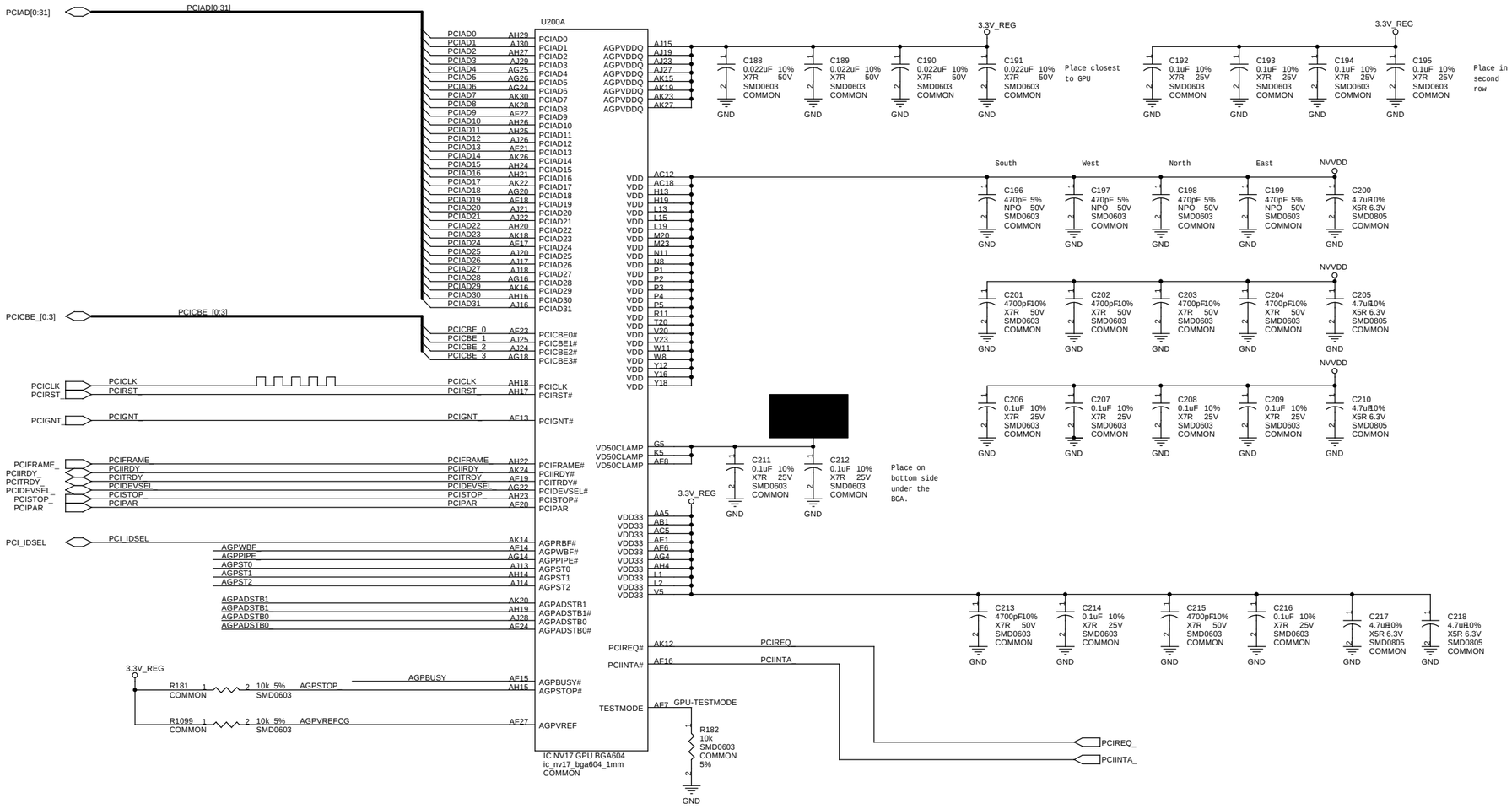
BGA and PQFP bridge chips can exist inside one another on the PCB

These trace lengths should be matched. Source termnators located near bridge chip

INVESTIGATE 1K PULLDOWN, LAYOUT, REVIEW

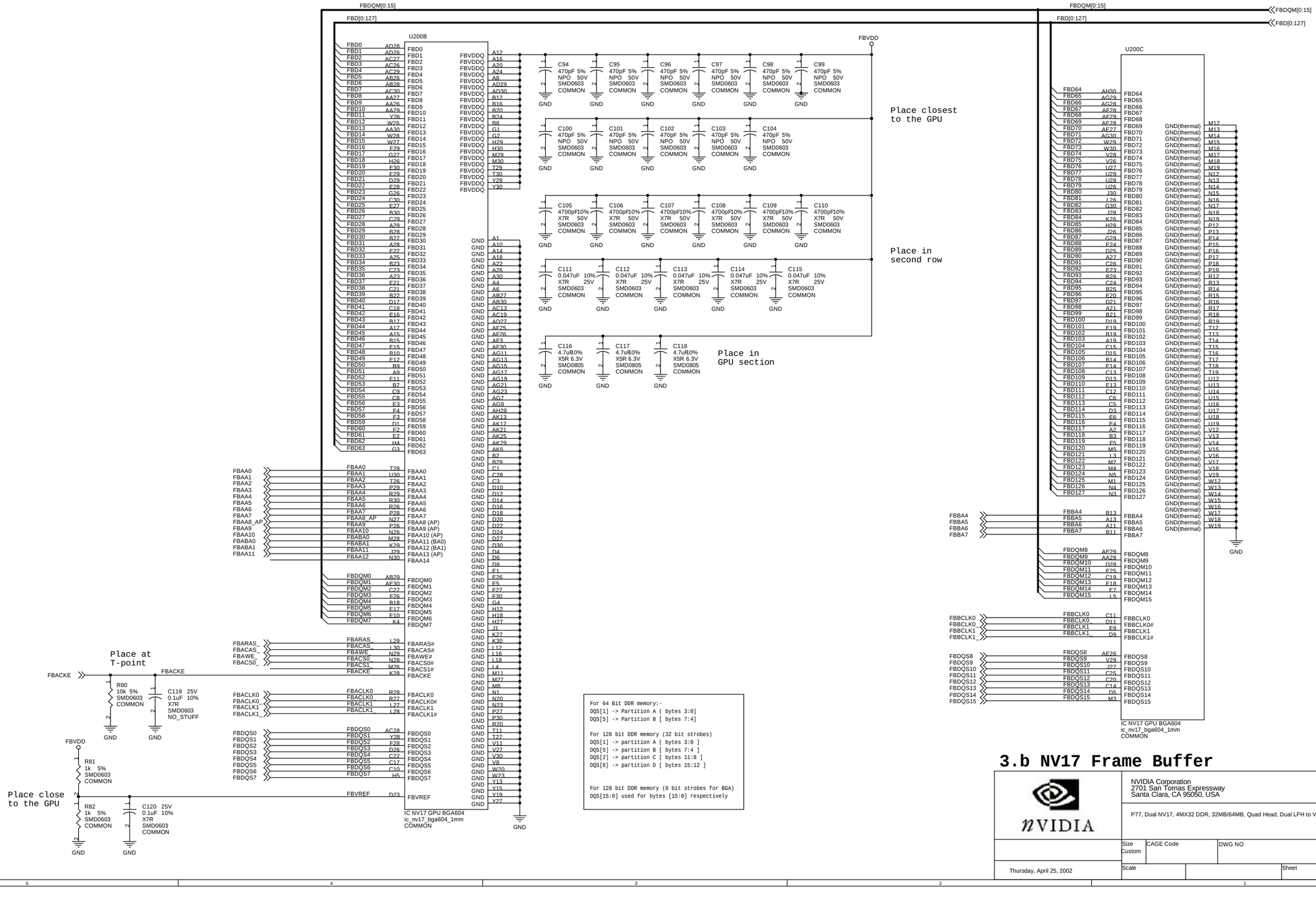
2.b PCI bus bridge

NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA	GPU	
P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz		
	Size: Custom	CAGE Code / DWG NO / Rev
Thursday, April 25, 2002	Scale	Sheet: 4 of 26



3.a PCI interface, core decoupling

NVIDIA	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA	GPU 0
	P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz	
	Size: Custom; CAGE Code; DWG NO; Rev	
Thursday, April 25, 2002	Scale; Sheet 5 of 26	



3.b NV17 Frame Buffer

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2701 San Tomas Expressway
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GPU 0

P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz

Size	CAGE Code	DWG NO	Rev
Custom			

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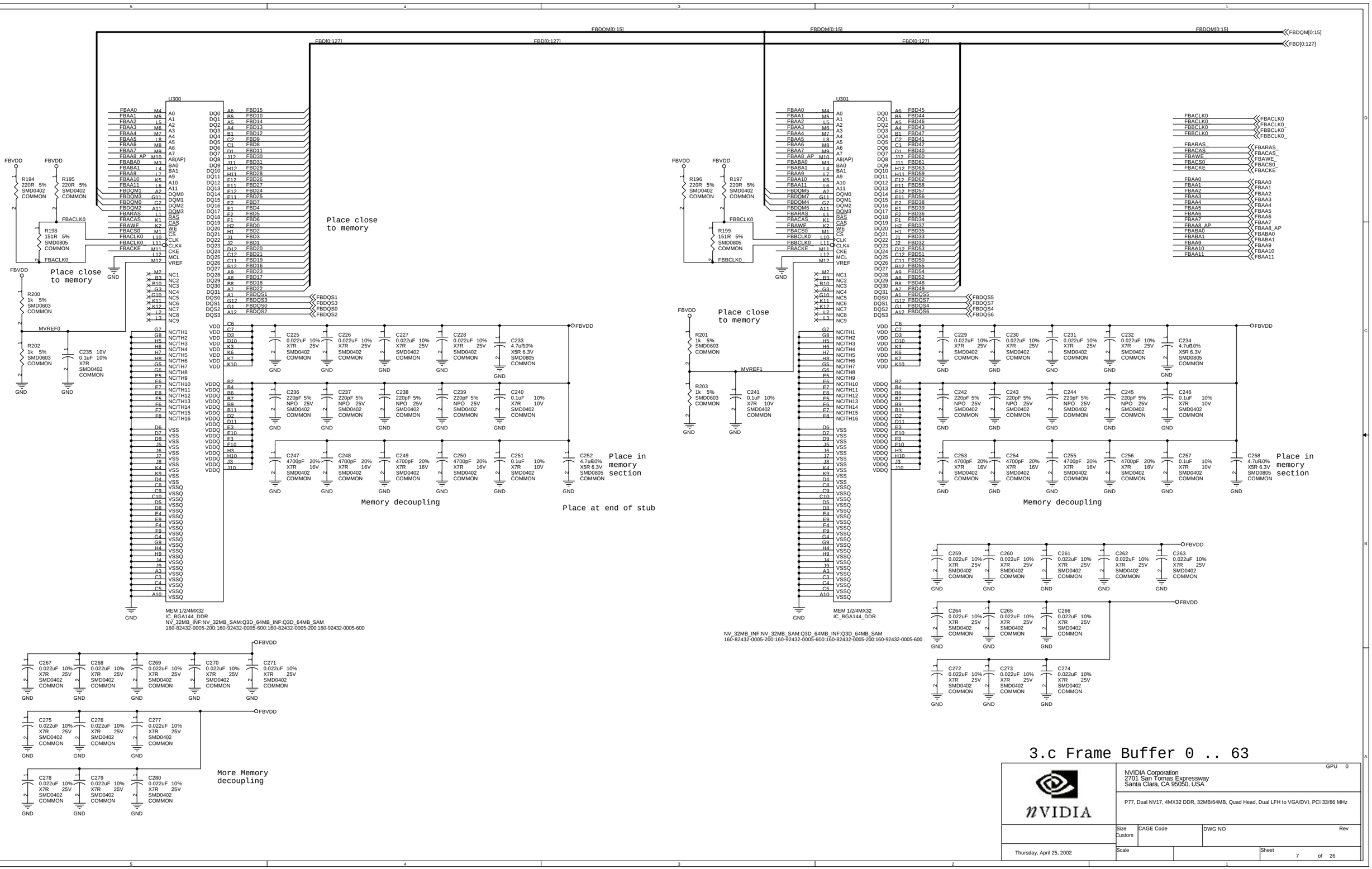
FBDQM[0:15]
FBD[0:127]
U300
U301
MEM 1/2/4MX32
IC_BGA144_DDR
NV_32MB_INF:NV_32MB_SAM:Q3D_64MB_INF:Q3D_64MB_SAM
160-82432-0005-200:160-92432-0005-600:160-82432-0005-200:160-92432-0005-600
Place close to memory
Place in memory section
Place at end of stub
Memory decoupling
More Memory decoupling
FBVDD
GND
MVREF0
MVREF1
FBACLK0
FBBCLK0
3.c Frame Buffer 0 .. 63
NVIDIA Corporation
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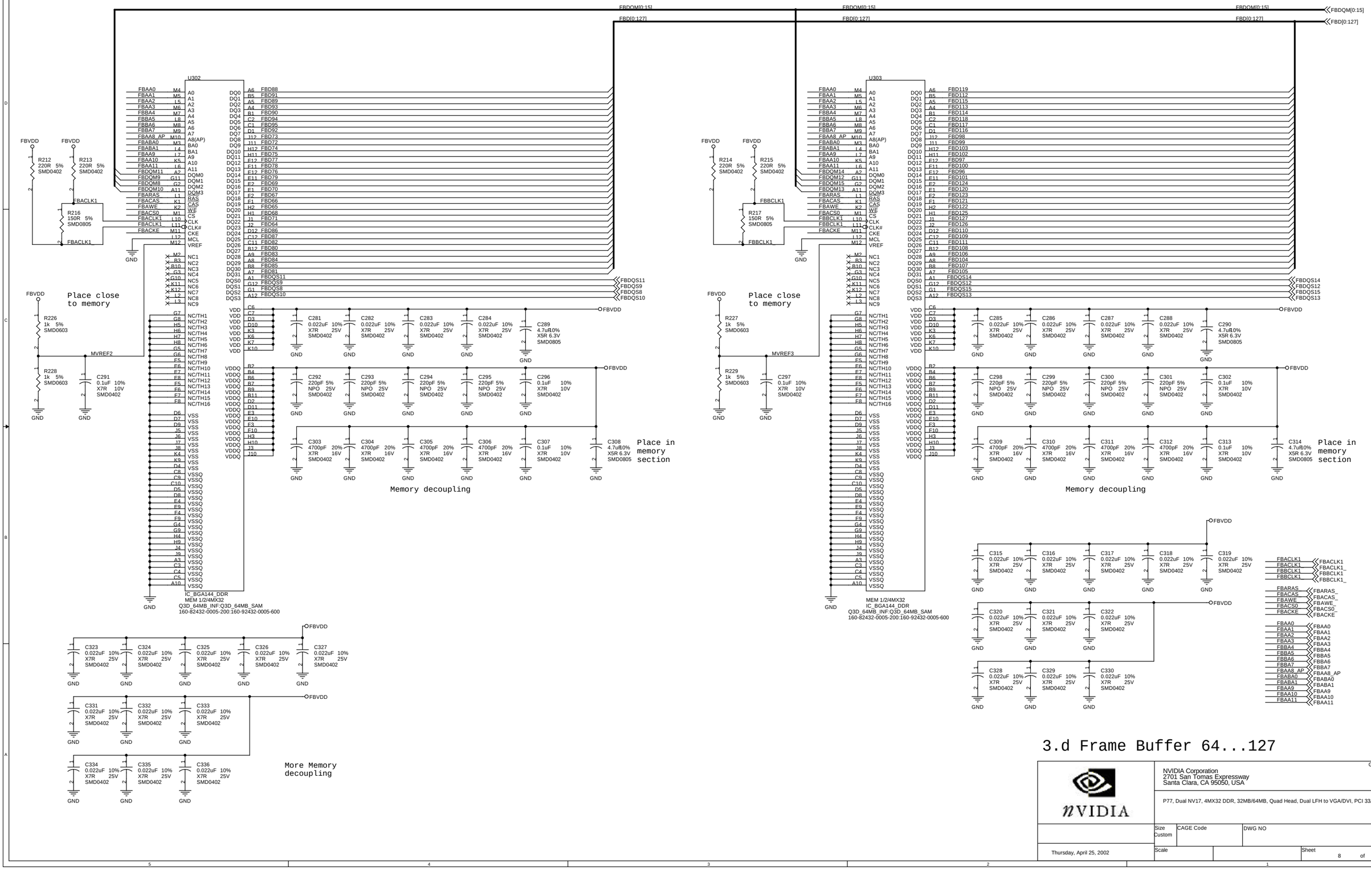
Santa Clara, CA 95050, USA
GPU 0
P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz
Size Custom
CAGE Code
DWG NO
Rev
Thursday, April 25, 2002
Scale
Sheet 7 of 26


FBDQM[0:15]
FBD[0:127]
U302
U303
FBVDD
FBBCLK1
FBACLK1
MVREF2
MVREF3
Place close to memory
Place in memory section
Memory decoupling
More Memory decoupling
IC_BGA144_DDR
MEM 1/2/4MX32
Q3D_64MB_INF:Q3D_64MB_SAM
160-82432-0005-200:160-92432-0005-600
3.d Frame Buffer 64...127
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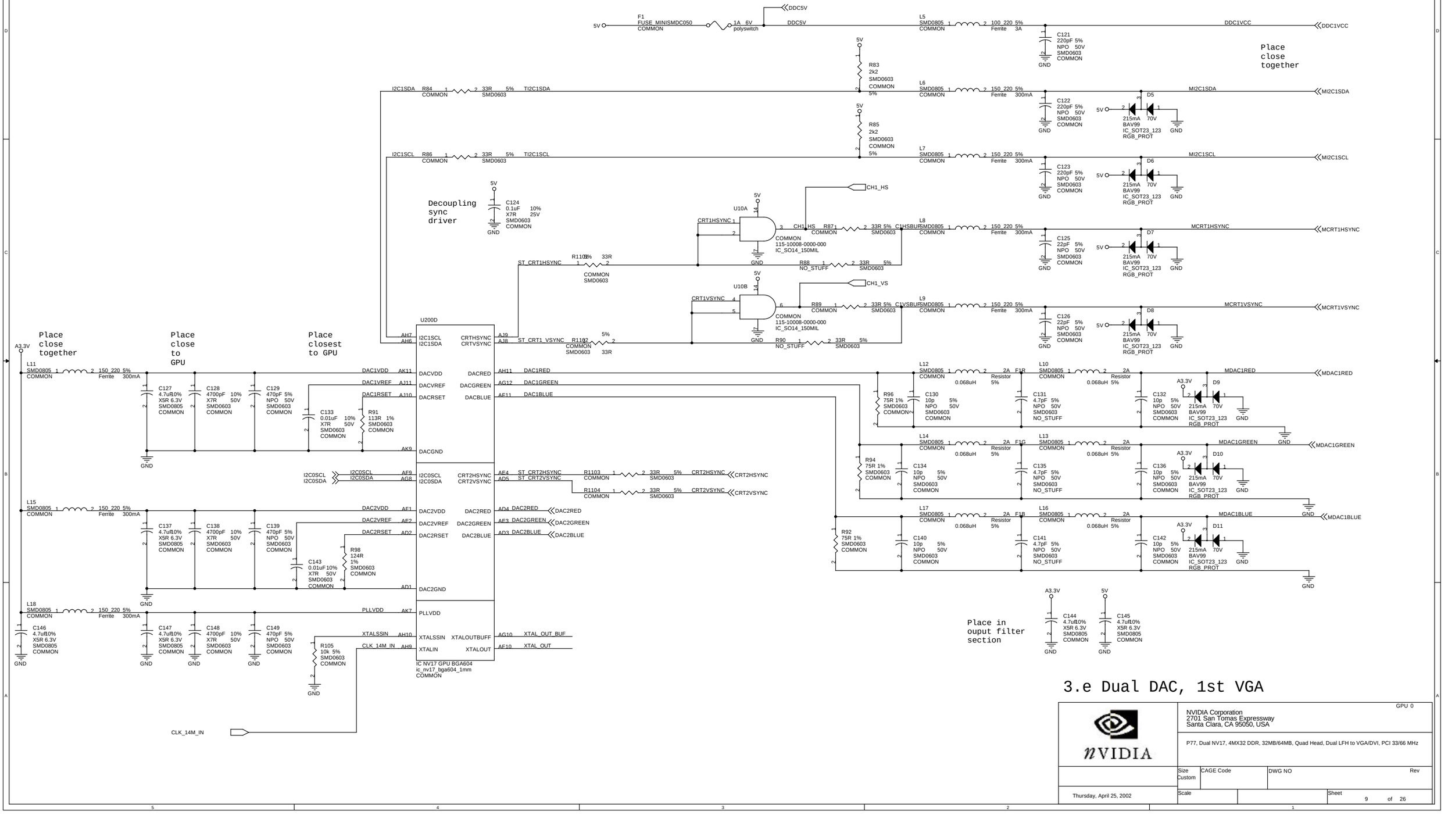
Santa Clara, CA 95050, USA
P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz
GPU 0
Thursday, April 25, 2002
Sheet 8 of 26


Place close together
Place close to GPU
Place closest to GPU
Decoupling sync driver
Place close together
Place in ouput filter section
U200D
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
COMMON
3.e Dual DAC, 1st VGA
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
GPU 0
P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz
Thursday, April 25, 2002
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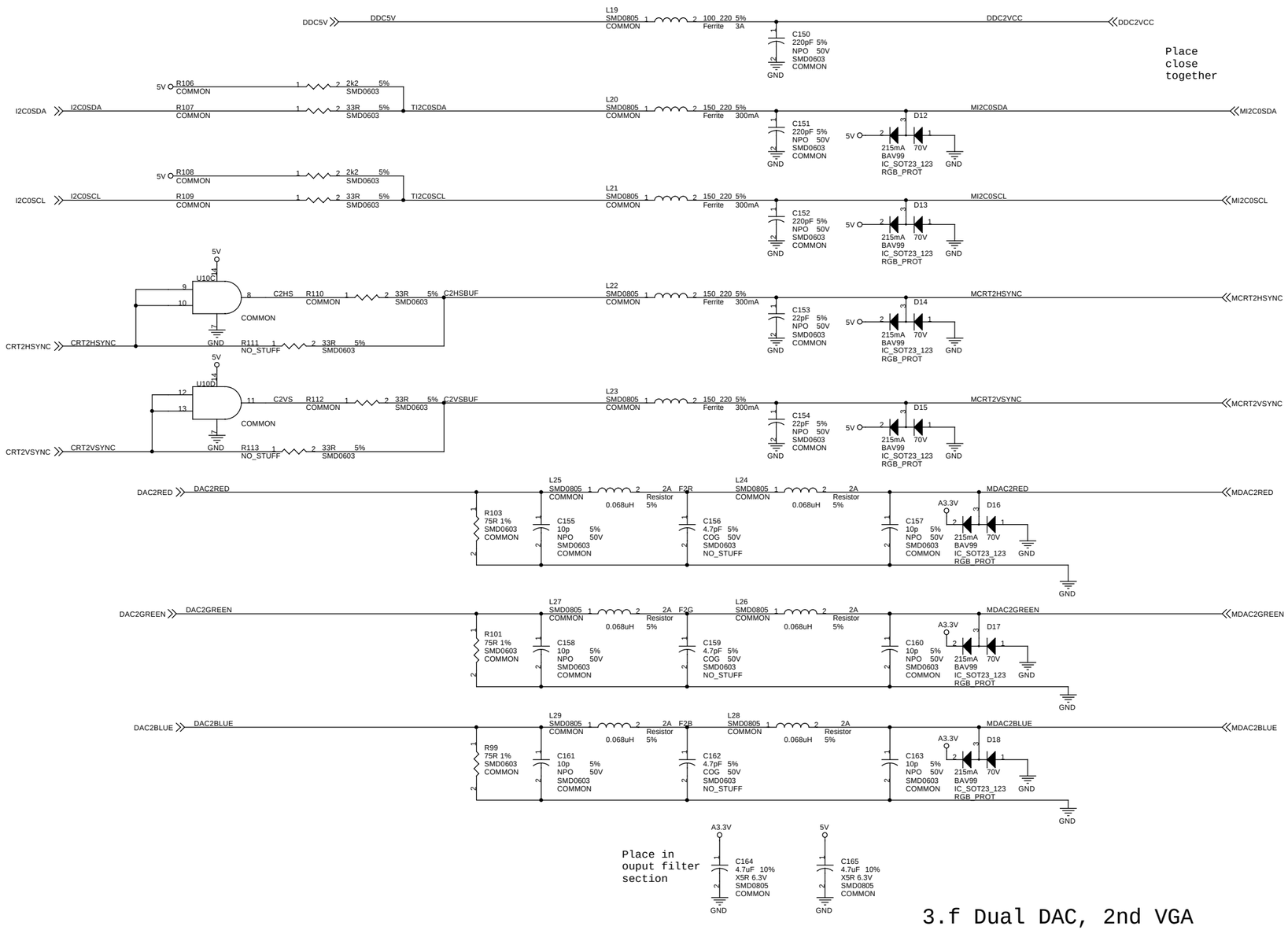

3.f Dual DAC, 2nd VGA

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Santa Clara, CA 95050, USA

GPU 0

P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz

Size	CAGE Code	DWG NO	Rev
Custom			

Thursday, April 25, 2002

Scale

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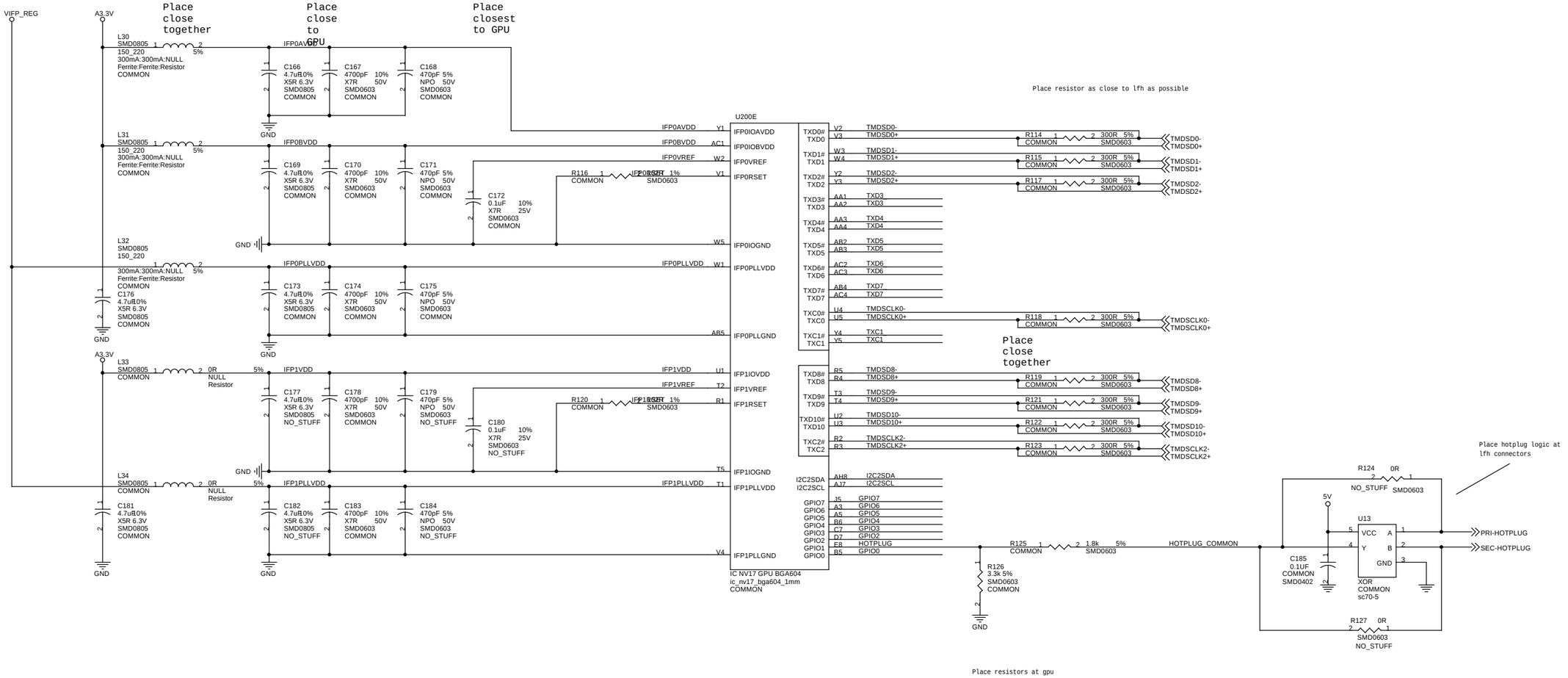

3.g Panel

NVIDIA	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA	GPU 0
	P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz	
	Size: Custom; CAGE Code; DWG NO; Rev	
Thursday, April 25, 2002	Scale; Sheet: 11 of 26	

Strapping Configuration

Strap Bits				Options (* = default)
0	PCI_AD_SWAP	R131 COMMON 10k 5% SMD0402	PCI_AD_SWAP	0: REVERSED 1: NORMAL(*)
1	SUB_VENDOR	R132 NO_STUFF 10k 5% SMD0402 R133 COMMON 10k 5% SMD0402	SUB_VENDOR	0: system BIOS 1: adapter BIOS (*)
2	RAM_CFG0	R134 NO_STUFF 10k 5% SMD0402 R135 COMMON 10k 5% SMD0402	RAM_CFG[3:0]	1111: 4Mx32 DDR SDRAM, DQS per 32 bits, dll-on, low drive strength
3	RAM_CFG1	R136 COMMON 10k 5% SMD0402 R137 NO_STUFF 10k 5% SMD0402		
4	RAM_CFG2	R138 NO_STUFF 10k 5% SMD0402 R139 COMMON 10k 5% SMD0402		
5	RAM_CFG3	R140 NO_STUFF 10k 5% SMD0402 R141 COMMON 10k 5% SMD0402		
6	CRYSTAL0	R142 NO_STUFF 10k 5% SMD0402 R143 COMMON 10k 5% SMD0402	CRYSTAL[1:0]	00: 13.5MHz 01: 14.318MHz (*) 10: 27MHz 11: unknown
22	CRYSTAL1	R144 COMMON 10k 5% SMD0402 R145 NO_STUFF 10k 5% SMD0402		
7	TV_MODE0	R146 NO_STUFF 10k 5% SMD0402 R147 COMMON 10k 5% SMD0402	TVMODE[1:0]	00: SECAM 01: NTSC 10: PAL 11: VGA (*)
8	TV_MODE1	R148 NO_STUFF 10k 5% SMD0402 R149 COMMON 10k 5% SMD0402		
9	AGP4x	R152 NO_STUFF 10k 5% SMD0402 R153 COMMON 10k 5% SMD0402	AGP4x	0: enabled 1: disabled (*)
11	AGP_FW	R154 NO_STUFF 10k 5% SMD0402 R155 COMMON 10k 5% SMD0402	AGP_FW	0: enabled 1: disabled (*)
12	PCI_DEVID0	R157 NO_STUFF 10k 5% SMD0402 R158 NO_STUFF 10k 5% SMD0402	PCI_DEVID[0:3]	NV17 - P77 - 017Ah - A = 1010b
13	PCI_DEVID1	R159 NO_STUFF 10k 5% SMD0402 R160 COMMON 10k 5% SMD0402		
20	PCI_DEVID2	R161 COMMON 10k 5% SMD0402 R162 NO_STUFF 10k 5% SMD0402		
21	PCI_DEVID3	R163 NO_STUFF 10k 5% SMD0402 R164 COMMON 10k 5% SMD0402		
14	BUS_TYPE	R165 COMMON 10k 5% SMD0402	BUS_TYPE	0: PCI (*) ONLY 1: AGP not supported
16	USER_0	R167 COMMON 10k 5% SMD0402	USER[3:0]	USER[0]=0: PC (*) USER[0]=1: MAC Not supported
17	USER_1	R169 COMMON 10k 5% SMD0402 R170 NO_STUFF 10k 5% SMD0402		
18	USER_2	R171 COMMON 10k 5% SMD0402 R172 NO_STUFF 10k 5% SMD0402		
19	USER_3	R173 COMMON 10k 5% SMD0402 R174 NO_STUFF 10k 5% SMD0402		
29	ROMTYPE[0]	R176 COMMON 10k 5% SMD0402	ROMTYPE[1:0]	00: parallel - not supported 01: serial AT25F (*) 10: serial SST45V - not supported 11: serial future - not supported
30	ROMTYPE[1]	R177 COMMON 10k 5% SMD0402		

DVOD[0:11]

VIPD[0:7]

VIPHAD1

VIPHAD0

DVOHSYNC

3.3V_REG

GND

R156 10k SMD0603 COMMON 5%

DVOD0

DVOD1

VIPD0

ROMCS

U15

AT25F1024 3.3V IC_SO8 NO_STUFF

C187 0.1uF 10% X7R 25V SMD0603 COMMON

A3.3V

R185 1k 5% SMD0603 COMMON

U200F

ROMCS# ROMA14 ROMA15 DVOVSYNC DVOHSYNC DVODE DVOCLKIN DVOCLKOUT DVOCLKOUT# DVOD0 DVOD1 DVOD2 DVOD3 DVOD4 DVOD5 DVOD6 DVOD7 DVOD8 DVOD9 DVOD10 DVOD11 VDDDVO VDDDVO VDDDVO DVOVREF BUFRST# VIPPCLK VIPHAD1 VIPHAD0 VIPHCTL VIPHCLK VIPD0 VIPD1 VIPD2 VIPD3 VIPD4 VIPD5 VIPD6 VIPD7 NC

IC NV17 GPU BGA604 ic_nv17_bga604_1mm COMMON

R186 10k 5% SMD0603 COMMON

R187 1k 5% SMD0603 COMMON

R189 1k 5% SMD0603 COMMON

C222 0.1uF 10% X7R 25V SMD0603 COMMON

Place south west of GPU.

C220 0.022uF 10% X7R 50V SMD0603 COMMON

C221 4.7uF 10% X5R 6.3V SMD0805 COMMON

3.h BIOS, Strapping

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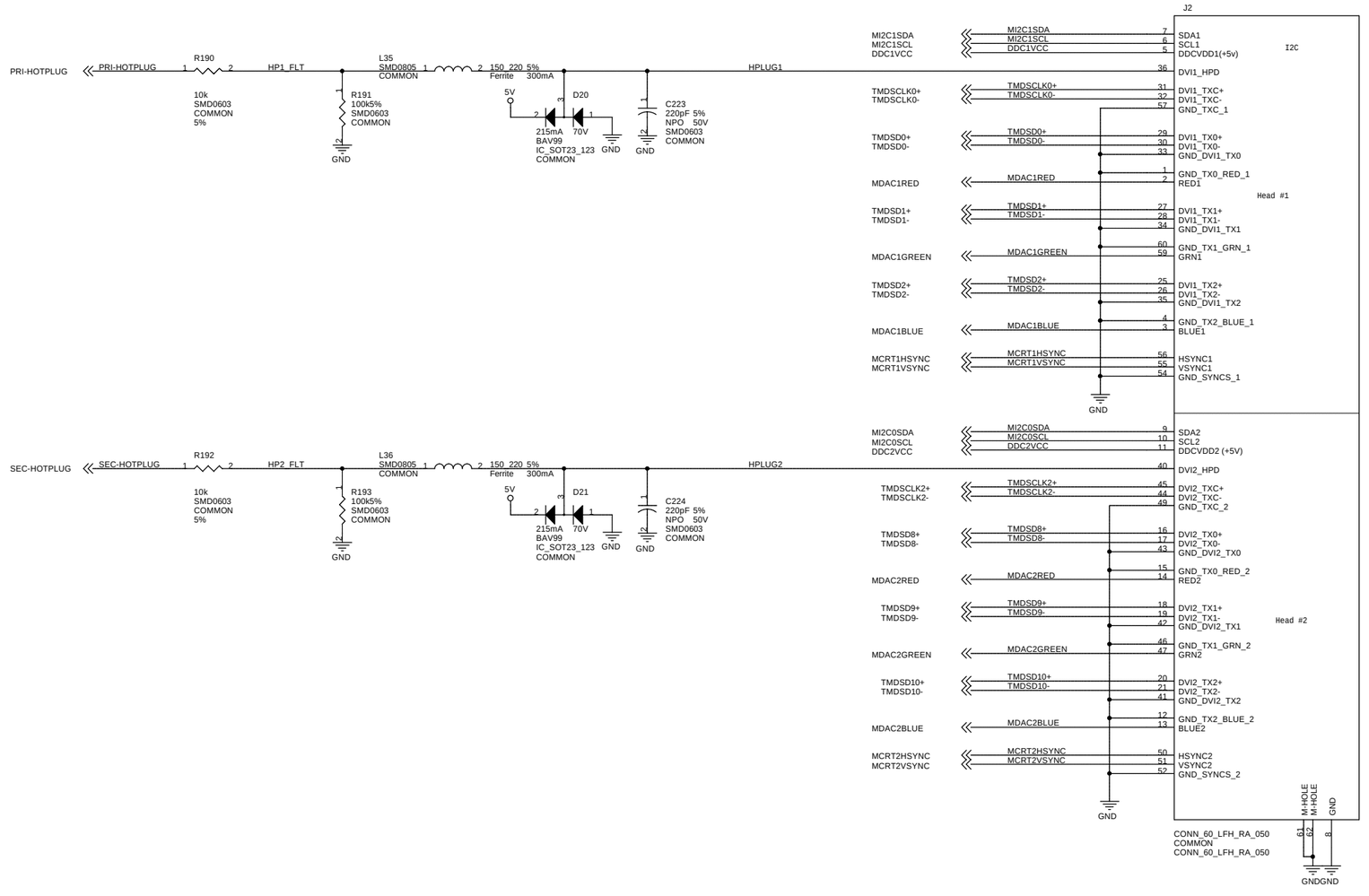
GPU 0

P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz

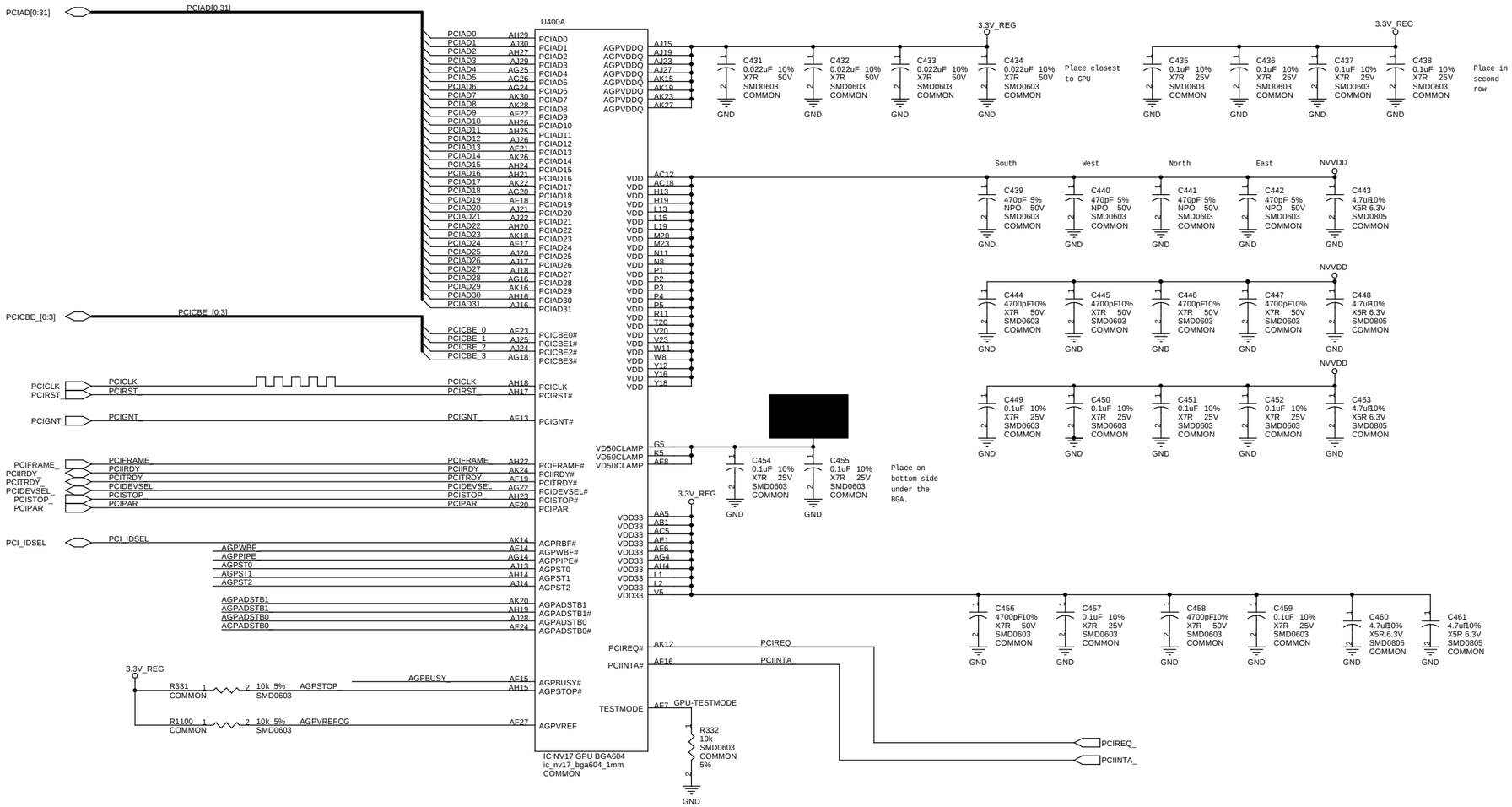
Size: Custom | CAGE Code | DWG NO | Rev

Thursday, April 25, 2002 | Scale | Sheet 12 of 26



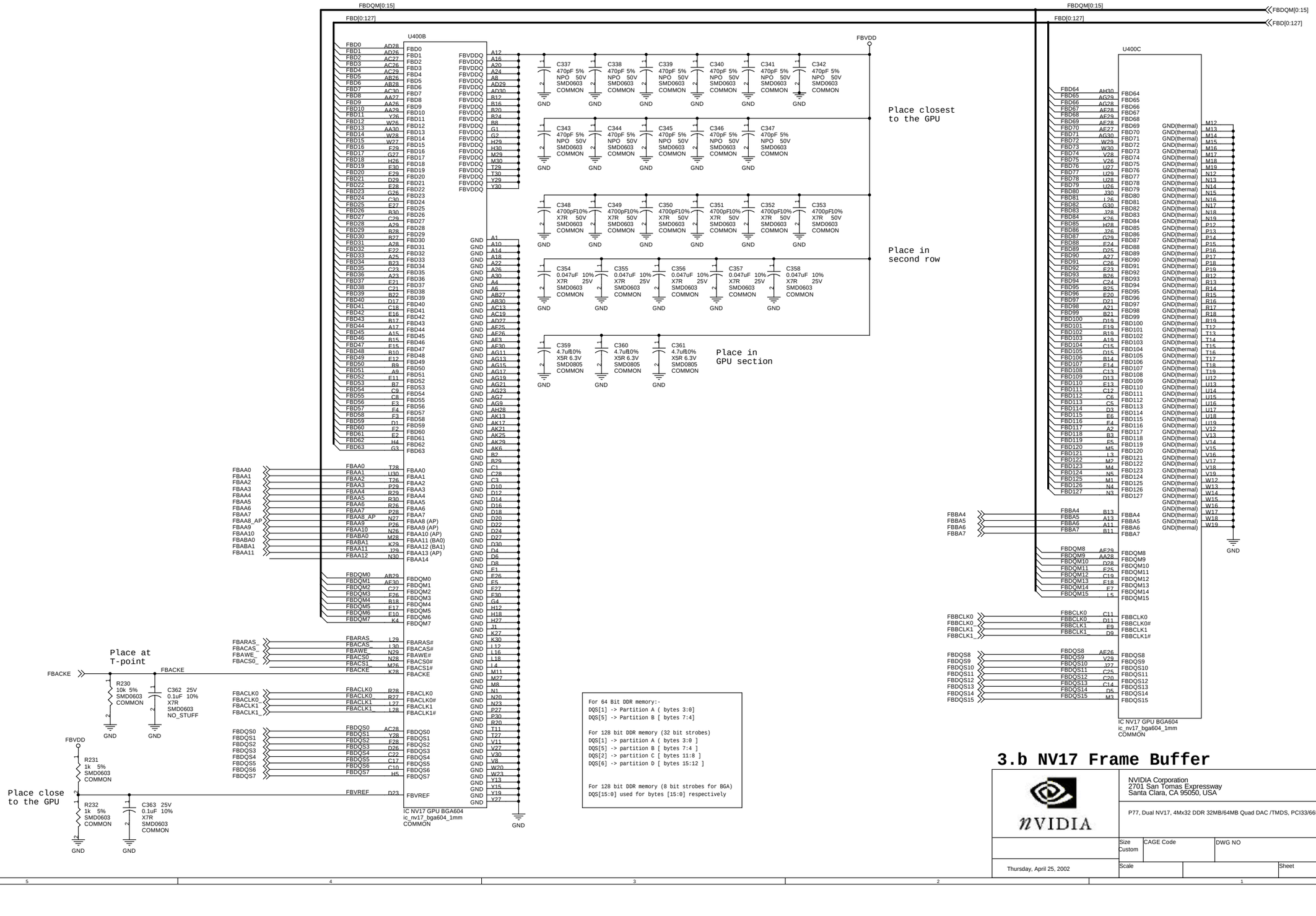
3.i Video Connector

NVIDIA	GPU 0		
	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA		
	P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz		
	Size: Custom	CAGE Code	DWG NO / Rev
Thursday, April 25, 2002	Scale		Sheet 13 of 26



3.a PCI interface, core decoupling

NVIDIA	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA	GPU 1
	P77, Dual NV17, 4Mx32 DDR 32MB/64MB Quad DAC /TMDS, PCI33/66Mhz	
	Size: Custom; CAGE Code; DWG NO; Rev	
Thursday, April 25, 2002	Scale; Sheet 14 of 26	



3.b NV17 Frame Buffer

NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA			GPU 1
P77, Dual NV17, 4Mx32 DDR 32MB/64MB Quad DAC /TMDS, PCI33/66Mhz			
	Size Custom	CAGE Code	DWG NO / Rev
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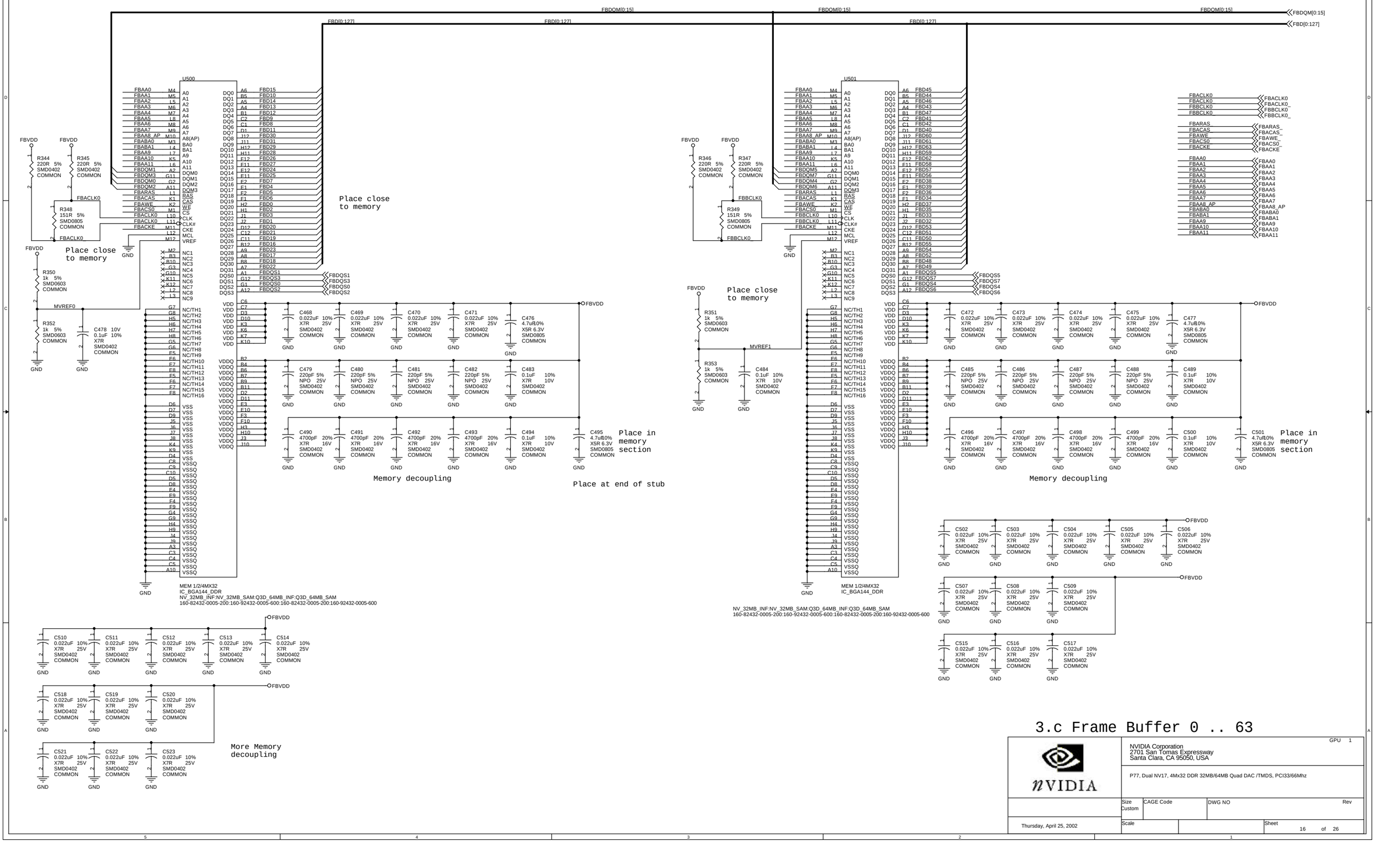
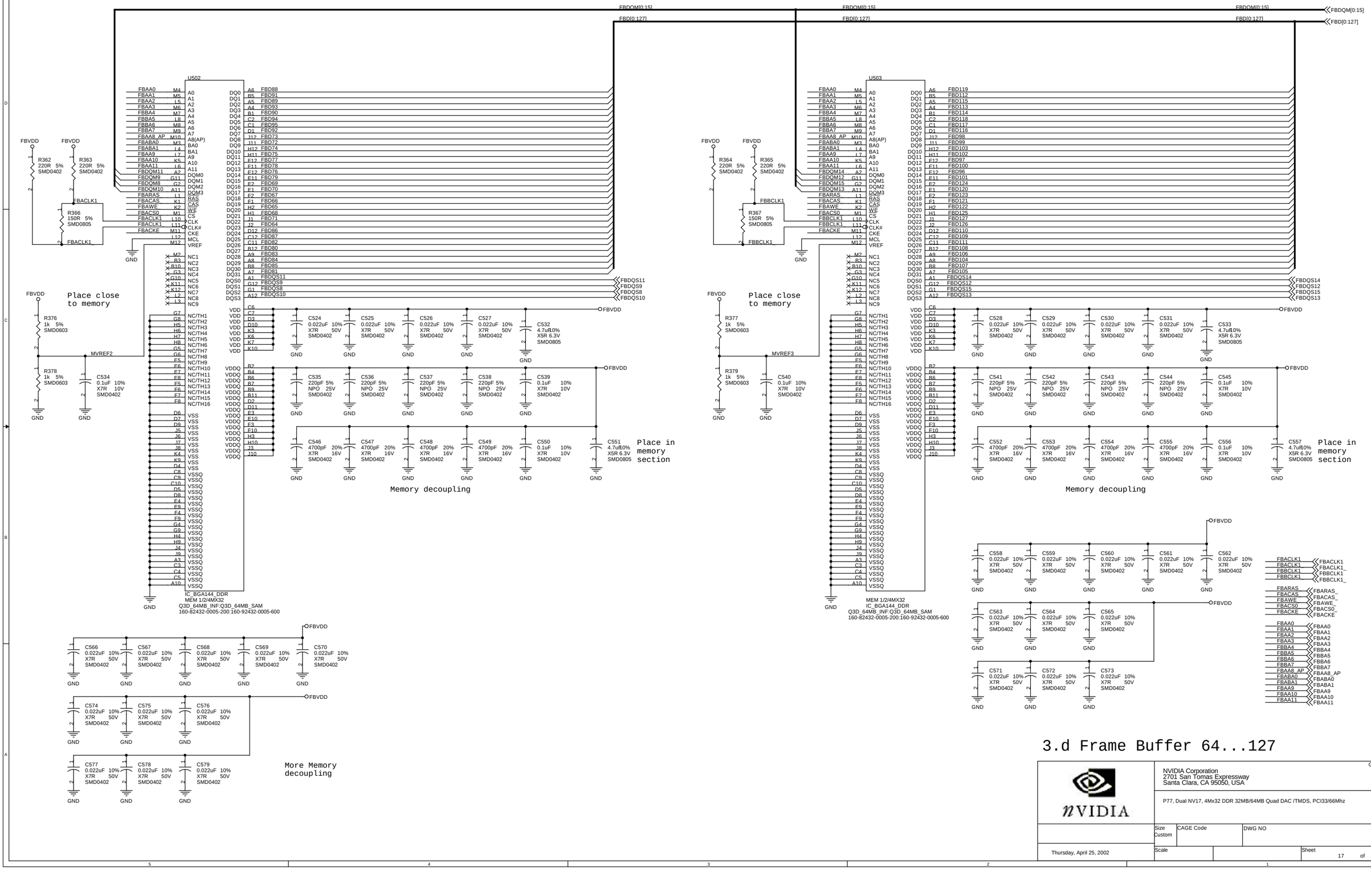
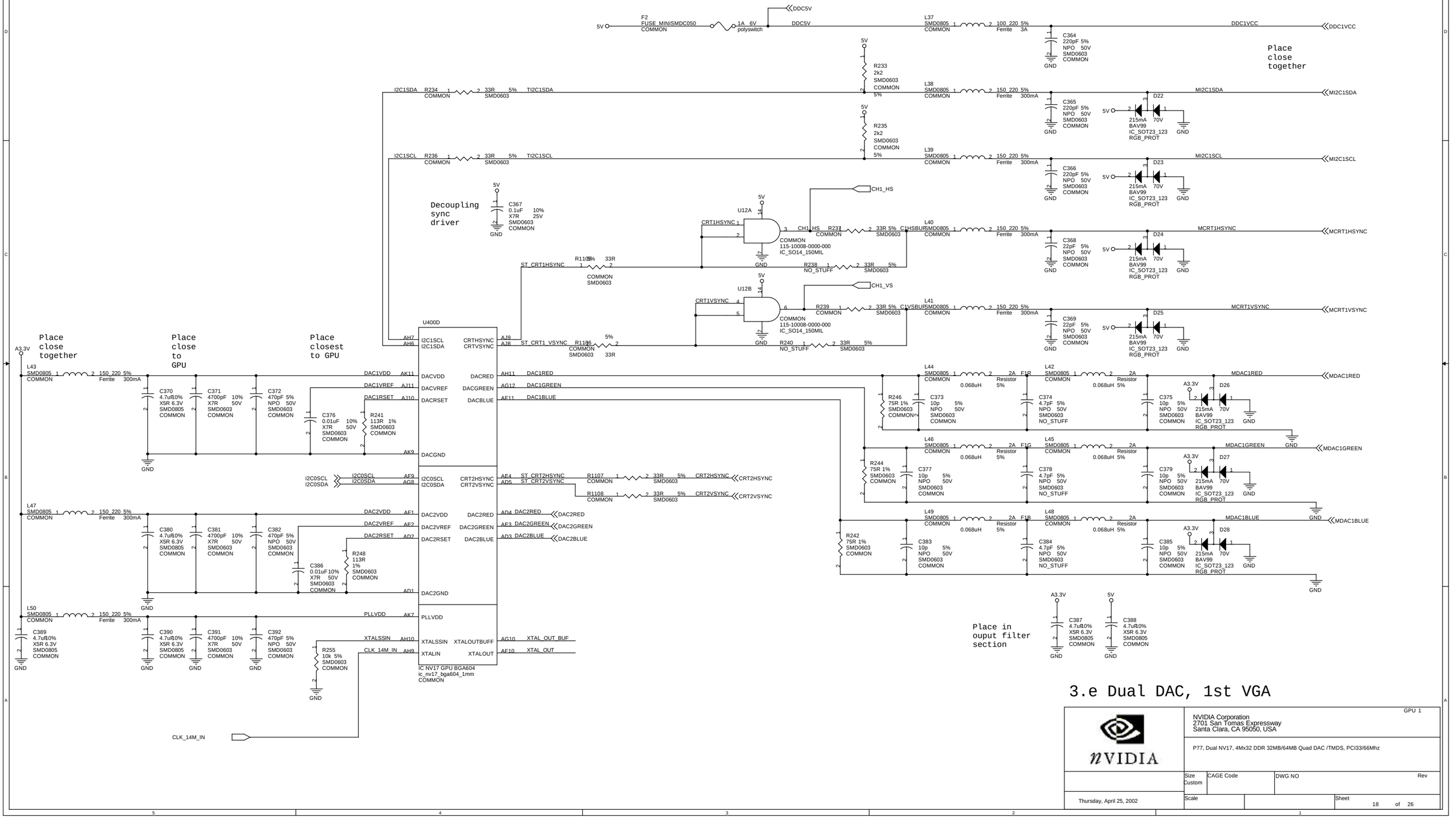
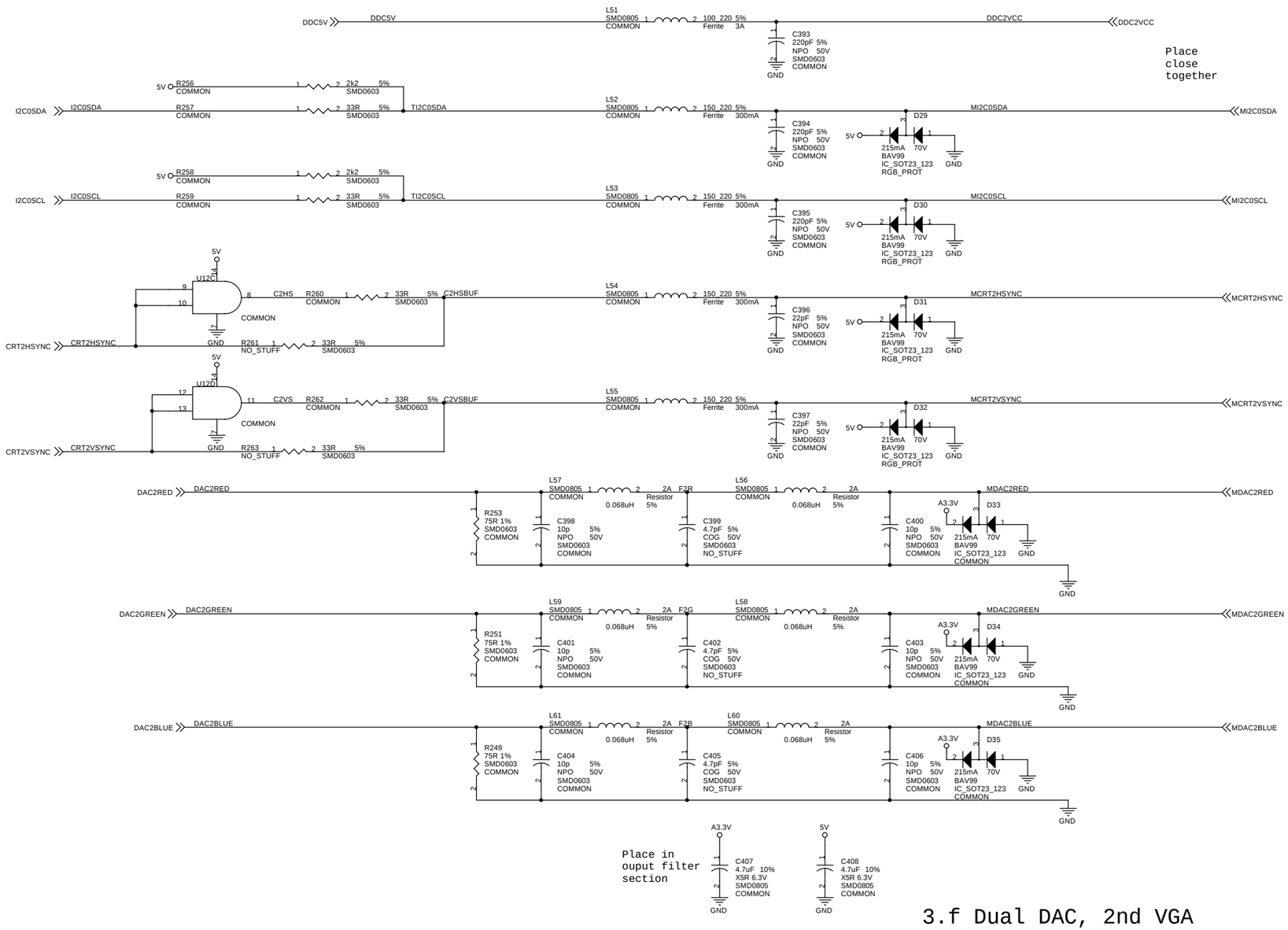

FBDQM[0:15]
FBD[0:127]
U500
U501
Place close to memory
Place in memory section
Memory decoupling
Place at end of stub
More Memory decoupling
MEM 1/2/4MX32
IC_BGA144_DDR
NV_32MB_INF:NV_32MB_SAM:Q3D_64MB_INF:Q3D_64MB_SAM
160-82432-0005-200:160-92432-0005-600:160-82432-0005-200:160-92432-0005-600
3.c Frame Buffer 0 .. 63
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P77, Dual NV17, 4Mx32 DDR 32MB/64MB Quad DAC /TMDS, PCI33/66Mhz
GPU 1
Thursday, April 25, 2002
Sheet 16 of 26


FBDQM[0:15]
FBD[0:127]
U502
U503
IC_BGA144_DDR
MEM 1/2/4MX32
Q3D_64MB_INF:Q3D_64MB_SAM
160-82432-0005-200:160-92432-0005-600
Place close to memory
Place in memory section
Memory decoupling
More Memory decoupling
FBVDD
FBDQS11
FBDQS9
FBDQS8
FBDQS10
FBDQS14
FBDQS12
FBDQS15
FBDQS13
MVREF2
MVREF3
FBACLK1
FBBCLK1
3.d Frame Buffer 64...127
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P77, Dual NV17, 4Mx32 DDR 32MB/64MB Quad DAC /TMDS, PCI33/66Mhz
GPU 1
Size Custom
CAGE Code
DWG NO
Rev
Thursday, April 25, 2002
Scale
Sheet 17 of 26


Place close together
Place close to GPU
Place closest to GPU
Place close together
Decoupling sync driver
Place in ouput filter section
U400D
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
COMMON
CLK_14M_IN
3.e Dual DAC, 1st VGA
NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA
P77, Dual NV17, 4Mx32 DDR 32MB/64MB Quad DAC /TMDS, PCI33/66Mhz
GPU 1
Thursday, April 25, 2002
Sheet 18 of 26



3.f Dual DAC, 2nd VGA

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

GPU 1

P77, Dual NV17, 4Mx32 DDR 32MB/64MB Quad DAC /TMDS, PCI33/66Mhz

Size	CAGE Code	DWG NO	Rev
Custom			

Thursday, April 25, 2002

Scale

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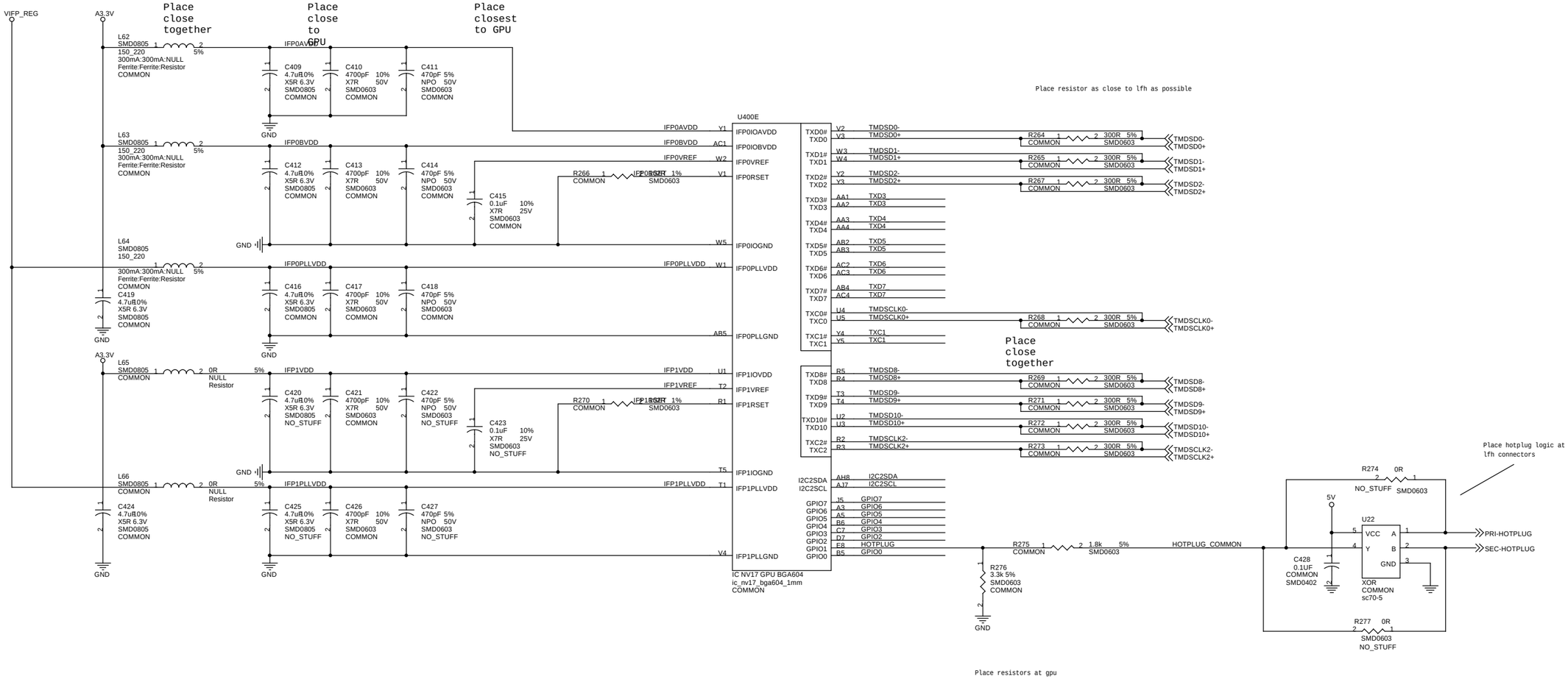

3.g Panel

NVIDIA	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA	GPU 1
	P77, Dual NV17, 4Mx32 DDR 32MB/64MB Quad DAC /TMDS, PCI33/66Mhz	
	Size: Custom; CAGE Code; DWG NO; Rev	
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Strapping Configuration

Strap Bits				Options (* = default)
0	PCI_AD_SWAP	R281 COMMON 10k 5% SMD0402	PCI_AD_SWAP	0: REVERSED 1: NORMAL(*)
1	SUB_VENDOR	R282 NO_STUFF 10k 5% SMD0402 R283 COMMON 10k 5% SMD0402	SUB_VENDOR	0: system BIOS 1: adapter BIOS (*)
2	RAM_CFG0	R284 NO_STUFF 10k 5% SMD0402 R285 COMMON 10k 5% SMD0402	RAM_CFG[3:0]	1111: 4Mx32 DDR SDRAM, DQS per 32 bits, dll-on, low drive strength
3	RAM_CFG1	R286 COMMON 10k 5% SMD0402 R287 NO_STUFF 10k 5% SMD0402		
4	RAM_CFG2	R288 NO_STUFF 10k 5% SMD0402 R289 COMMON 10k 5% SMD0402		
5	RAM_CFG3	R290 NO_STUFF 10k 5% SMD0402 R291 COMMON 10k 5% SMD0402		
6	CRYSTAL0	R292 NO_STUFF 10k 5% SMD0402 R293 COMMON 10k 5% SMD0402	CRYSTAL[1:0]	00: 13.5MHz 01: 14.318MHz (*) 10: 27MHz 11: unknown
22	CRYSTAL1	R294 COMMON 10k 5% SMD0402 R295 NO_STUFF 10k 5% SMD0402		
7	TV_MODE0	R296 NO_STUFF 10k 5% SMD0402 R297 COMMON 10k 5% SMD0402	TVMODE[1:0]	00: SECAM 01: NTSC 10: PAL 11: VGA (*)
8	TV_MODE1	R298 NO_STUFF 10k 5% SMD0402 R299 COMMON 10k 5% SMD0402		
9	AGP4x	R302 NO_STUFF 10k 5% SMD0402 R303 COMMON 10k 5% SMD0402	AGP4x	0: enabled 1: disabled (*)
11	AGP_FW	R304 NO_STUFF 10k 5% SMD0402 R305 COMMON 10k 5% SMD0402	AGP_FW	0: enabled 1: disabled (*)
12	PCI_DEVID0	R307 NO_STUFF 10k 5% SMD0402 R308 NO_STUFF 10k 5% SMD0402	PCI_DEVID[0:3]	NV17 - P77 - 017Ah - A = 1010b
13	PCI_DEVID1	R309 NO_STUFF 10k 5% SMD0402 R310 COMMON 10k 5% SMD0402		
20	PCI_DEVID2	R311 COMMON 10k 5% SMD0402 R312 NO_STUFF 10k 5% SMD0402		
21	PCI_DEVID3	R313 NO_STUFF 10k 5% SMD0402 R314 COMMON 10k 5% SMD0402		
14	BUS_TYPE	R315 COMMON 10k 5% SMD0402	BUS_TYPE	0: PCI (*) ONLY 1: AGP not supported
16	USER_0	R317 COMMON 10k 5% SMD0402	USER[3:0]	USER[0]=0: PC (*) USER[0]=1: MAC Not supported
17	USER_1	R319 COMMON 10k 5% SMD0402 R320 NO_STUFF 10k 5% SMD0402		
18	USER_2	R321 COMMON 10k 5% SMD0402 R322 NO_STUFF 10k 5% SMD0402		
19	USER_3	R323 COMMON 10k 5% SMD0402 R324 NO_STUFF 10k 5% SMD0402		
29	ROMTYPE[0]	R326 COMMON 10k 5% SMD0402	ROMTYPE[1:0]	00: parallel - not supported 01: serial AT25F (*) 10: serial SST45V - not supported 11: serial future - not supported
30	ROMTYPE[1]	R327 COMMON 10k 5% SMD0402		

3.3V_REG

DVOD[0:11]

VIPD0

VIPD1

VIPD2

VIPD3

VIPD4

VIPD5

VIPD6

VIPD7

VIPD[0:7]

VIPHAD1

VIPHAD0

DVOHSYNC

GND

R306 10k SMD0603 COMMON 5%

U24 AT25F1024 3.3V IC_SO8 NO_STUFF

SI, SCK, SO, CS, VDD, HOLD, WP, GND

C430 0.1uF 10% X7R 25V SMD0603 COMMON

A3.3V

R335 1k 5% SMD0603 COMMON

U400F

ROMCS, ROMA14, ROMA15, DVOVSYNC, DVOHSYNC, DVODE, DVOCLKIN, DVOCLKOUT, DVOCLKOUT#, DVOD0–DVOD11, VDDDVO, DVOVREF

BUFRST#, VIPPCLK, VIPHAD1, VIPHAD0, VIPHCTL, VIPHCLK, VIPD0–VIPD7

NC

IC NV17 GPU BGA604 ic_nv17_bga604_1mm COMMON

R336 10k 5% SMD0603 COMMON

R337 1k 5% SMD0603 COMMON

R339 1k 5% SMD0603 COMMON

C465 0.1uF 10% X7R 25V SMD0603 COMMON

C463 0.022uF 10% X7R 50V SMD0603 COMMON

C464 4.7uF 10% X5R 6.3V SMD0805 COMMON

Place south west of GPU.

3.h BIOS, Strapping

NVIDIA Corporation
2701 San Tomas Expressway
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GPU 1

P77, Dual NV17, 4Mx32 DDR 32MB/64MB Quad DAC /TMDS, PCI33/66Mhz

Size: Custom | CAGE Code | DWG NO | Rev

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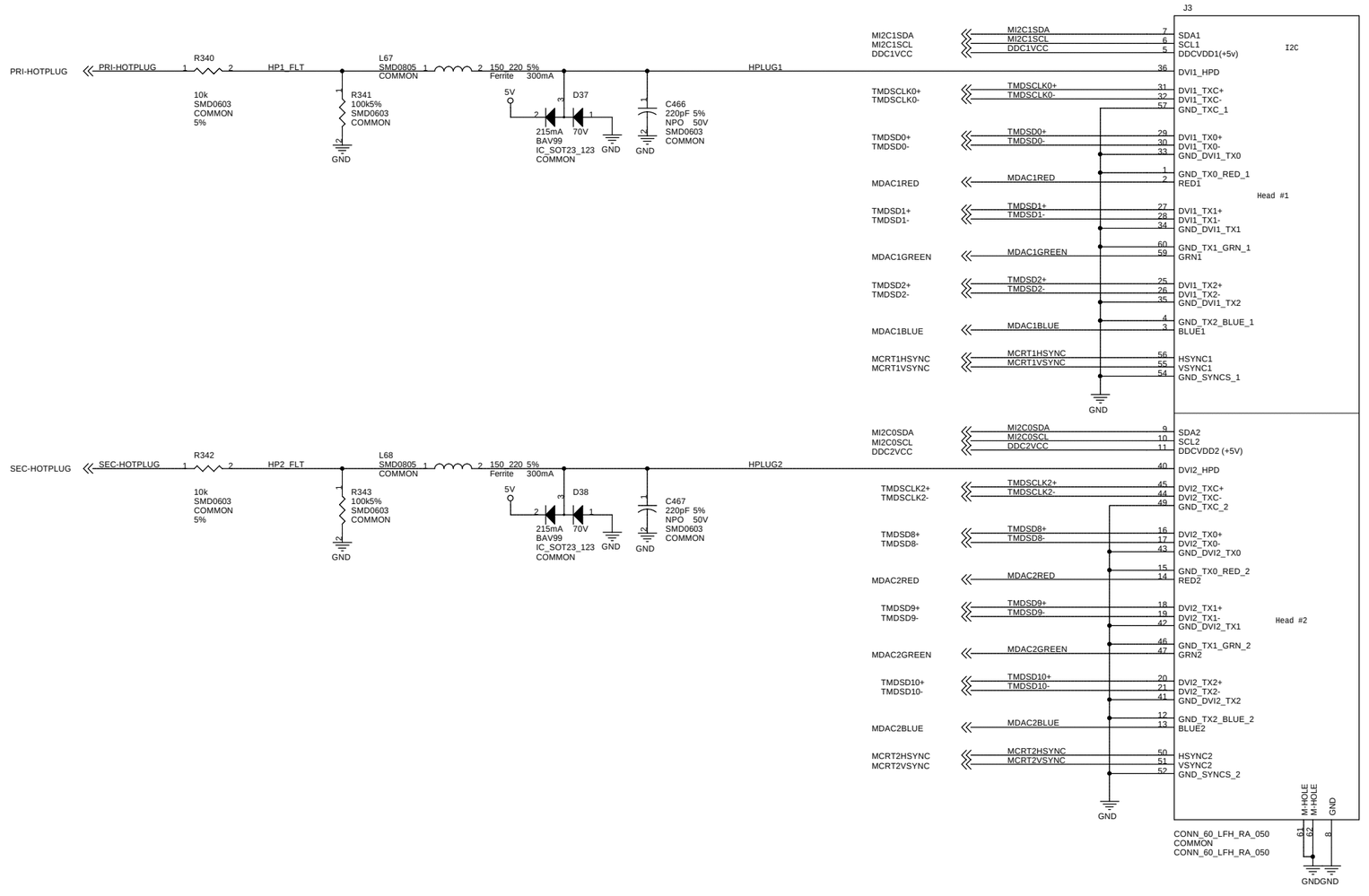

3.i Video Connector

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

GPU 1

P77, Dual NV17, 4Mx32 DDR 32MB/64MB Quad DAC /TMDS, PCI33/66Mhz

Size	CAGE Code	DWG NO	Rev
Custom			

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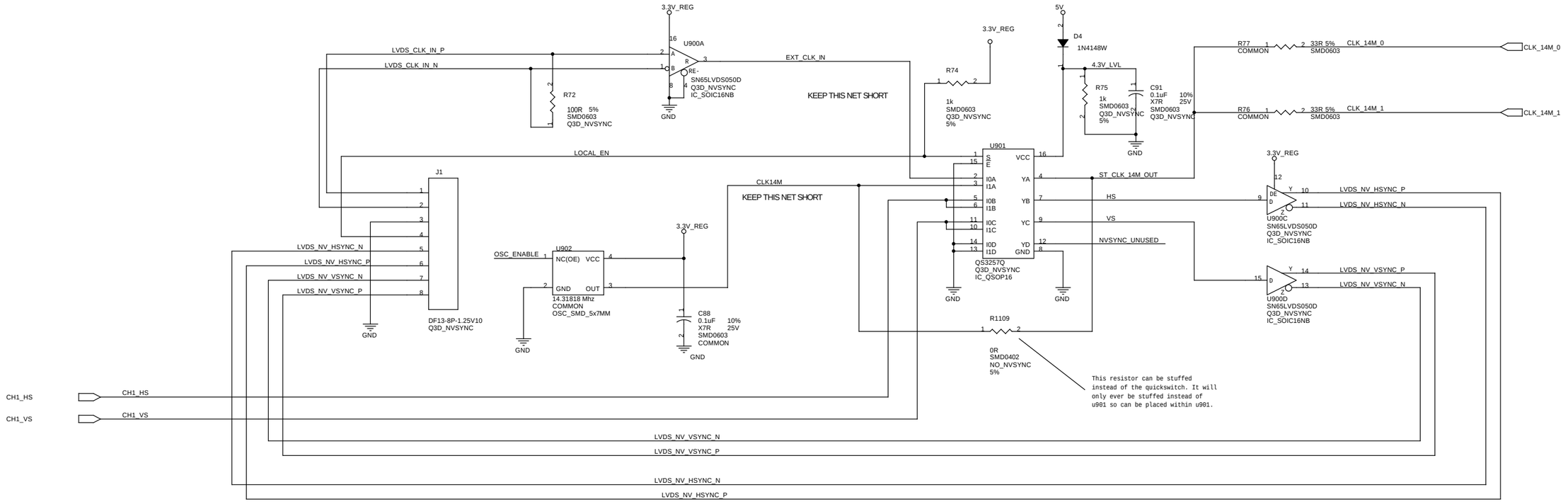
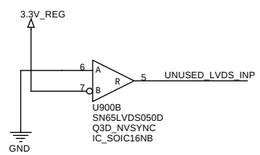
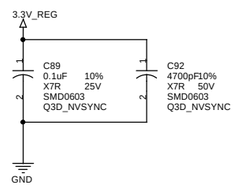
CROSS-TALK SENSITIVE, ROUTE IMPEDENCE 40-50ohm TO NV20 PIN AM1







4. nvSync (tm)

NVIDIA	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA		GPU
	P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz		
	Size: Custom	CAGE Code	DWG NO / Rev
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FET's are rated to carry 20Amps. Actually need 9.3A peak, but mean RMS is lower. However other used FET's did not have the capability to dissipate enough current. The rdsOn was also too high and pushed our power outside of the PCI budget. Hence seperate FET's in a larger package are used for high current and lower rds(on) - should improve our efficiency overall

No sense resistor, so disable CL circuit inside SC1175 to permanently enable with no over current sense

For a 3.9uH inductor, Iripple (max) =~ 0.9 Amps.
Note if use an IRU3047 this increases by 50%!

L801 1UH 20% 6.6A IND_CDR73 PWR_INDUCTOR

0R SMD0805 R814 NO_PWR_INDUCTOR

0R SMD0805 R812 NO_PWR_INDUCTOR

SMD0805 R815 0R NO_PWR_INDUCTOR

SMD0805 R813 0R NO_PWR_INDUCTOR

5V — Can be placed on same location. Alternatice stuffing

C818 1000UF ALE INP_PWR_CAP 170mO 0.45A 6.3V 20%

C819 820uF 20% CAPS_TH_3_5_8-5_0_10 NO_STUFF 110mO ALE 0.56A 6.3V

CAPS_SMD_8_0-10_0_SANYO

5VFLT

C815 0.039UF SMD0603 COMMON 16V 10%

C816 0.039UF COMMON SMD0603 16V 10%

C817 0.1UF SMD0603 COMMON 25V 10%

We need to source at least 6 Amps on the 5V supply (for Q3D's option) For NV only 5 amps is necessary so one of the 0R resistors can be removed

U_V_IN_1

C805 4.7UF SMD0805 COMMON 6.3V 10%

COMMON SMD0603 R800 2.2R 5%

Q801 Si4410DY 30V 10A COMMON IC_SO8

C804 16V SMD0805 80/-20% COMMON

U_G1 — U_DH1

SMD0603 COMMON R801 2.2R 5% — U_DL11 — U_G3

Q802 Si4410DY 30V 10A COMMON IC_SO8

D800 COMMON RECT_SMDA 40V, 2.1A SMDA

SMD0805 COMMON 100R R823 5% SCSNBR1

C837 2200PF SMD0603 COMMON 100V 5%

L802 IND 3.9uH 9A RMS MULTI PAD:IND IRON SMT SMT 12.5x12.5@4.7uH @10A Q3D_POWER:NV_POWER

D803 IRU_3047 IC_SOT23_123 BAR43 Vr=30V, 100mA

U_CL1+ — R809 0R R810 SC1175 SMD0603 — IRU_3047 SMD0603

U_CL1-

5V — SMD0603 COMMON R802 2.2R 5% — VCC_REG_U

U_BSTC1

R811 0R SC1175 SMD0603

Stuff for SC1175 vs IRU3047

C810 10V 10% 0.22UF SMD0603 COMMON

SOFTSTART

C811 0.22UF SMD0603 COMMON

GND10V 10%

U_IN1

C813 50V 10% 0.01UF SMD0603 COMMON

VADJ

VOUT = 1.25 (1 + (ROUT/RGND))
Vout = 1.25 (1 + 130/475) = 1.60V

TP1 NO_STUFF HOLE_48C28P TEST POINT

R803 130R 1% SMD0603 COMMON

TP2 NO_STUFF HOLE_48C28P TEST POINT

R804 475R 1% SMD0603 COMMON

TP3 NO_STUFF HOLE_48C28P TEST POINT

1.60V — NVVDD

C807 470UF CAPS_SMD_8_0-10_0_SANYO NV_POWER — 25mO ALE-EX 2.09A 6.3V 20%

C808 510UF Q3D_POWER CAPS_TH_3_5_8-5_0_10 50/-10% 4V OSCON 14mO 4.08A

C806 1500uF 6.3V Q3D_POWER 90mO ALE 0.67A 20%

C809 510UF NO_STUFF CAPS_TH_3_5_8-5_0_10 50/-10% 4V OSCON 14mO 4.08A

CAPS_SMD_8_0-10_0_SANYO

Can be placed on same location. Alternatice stuffing

Can be placed on same location. Alternatice stuffing

NVIDIA option draws lower power allowing larger inductor/smaller ripple current. With a 3.9uH inductor, ripple current is approx 1Amp. So 2 caps just meet the requirement. Further derating would be adviseable. For Q3D however, the current is higher, limiting the inductor size and causing higher ripple. For this configuration an OSCON should be fitted instead.

U800 IC REG SWITCH SC1175 IC_SOIC20WB COMMON

SC1175

GND, U_IN1, SOFTSTART, U_CL1+, U_CL1-, U_BSTC1, U_DH1, U_DL1, VCC_REG_U, PGND, BSTC, DL1, BST1, DH1, BST2, DL2, SW2, SW1, SS/EN, PWRGD, IN1, Vref, +IN2, -IN2, VCC, CL2-, CL2+, SCVREF

5V COMMON IC_SOT23_123 BAT54ALT1 D801 — 5VSC1 — 5VSC2

SMD0603 R821 2.2R 5% COMMON

SMD0603 R822 2.2R 5% COMMON

5VFLT

C834 470UF NV_POWER — 25mO ALE-EX 2.09A 6.3V 20%

C836 620uF Q3D_POWER CAPS_TH_3_5_8-5_0_10 50/-10% 6.3V OSCON 13mO 4.08A

C802 470UF NV_POWER — 25mO ALE-EX 2.09A 6.3V 20%

C803 620uF Q3D_POWER CAPS_TH_3_5_8-5_0_10 50/-10% 6.3V OSCON 13mO 4.08A

CAPS_SMD_8_0-10_0_SANYO

Can be placed on same location. Alternatice stuffing

Can be placed on same location. Alternatice stuffing

C820 1nF SMD0603 COMMON 50V 5%

R818 0R SC1175 SMD0603

R819 0R IRU_3047 SMD0603

TP4 NO_STUFF HOLE_48C28P TEST POINT

2.5V — FBVDD

C825 1uF 80/-20% SMD0805 16V COMMON

R820 0R SC1175 SMD0603

SC-FB

R805 150R 1% SMD0603 COMMON

TP5 NO_STUFF HOLE_48C28P TEST POINT

C826 10V 10% 0.22UF SMD0603 COMMON

R806 150R 1% SMD0603 COMMON

TP6 NO_STUFF HOLE_48C28P TEST POINT

C823 470UF CAPS_SMD_8_0-10_0_SANYO NV_POWER — 25mO ALE-EX 2.09A 6.3V 20%

C824 510UF Q3D_POWER CAPS_TH_3_5_8-5_0_10 50/-10% 4V OSCON 14mO 4.08A

Can be placed on same location. Alternatice stuffing

The ALE stuffing option can only be used if a larger inductor is fitted. Otherwise ripple current exceeds the part's rating.

COMMON SMD0805 C827 1uF 80/-20% 16V

U_BST2

C828 0.01UF SMD0603 COMMON 50V 10%

U_V_IN_2

C829 4.7UF SMD0805 COMMON 6.3V 10%

Q800A IRF7311 IC_SO8 COMMON

L800 SMT 12.5X12.5@4.7UH@10A FALCO:SDIP0811-477 IND_MULTIPADS COMMON

C832 220pF SMD0603 COMMON 50V 5%

C830 0.1UF SMD0603 COMMON 25V 10%

C833 0.039UF SMD0603 COMMON 16V 10%

C831 4.7UF SMD0805 COMMON 6.3V 10%

Cbs1

U_G6 — R807 2.2R 5% SMD0603 COMMON

R808 2.2R — U_G4

SMD0603 5% COMMON

COMMON IC_SO8 IRF7311 Q800B

D802 COMMON RECT_SMDA 40V, 2.1A SMDA

SMD0805 COMMON 100R R824 5% SCSNBR2

C838 2200PF SMD0603 COMMON 100V 5%

D804 IRU_3047 IC_SOT23_123 BAR43 Vr=30V, 100mA

NVVVDD = 1.6 V , 9.0Amps worst case
FBVDD = FBVDDQ = 2.5 V, 3 Amps worst case

5.a NVVDD / FBVDD(Q) POWER SUPPLY

Please make ALL TPXX visible on silkscreen.

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

GPU

P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz

Size	CAGE Code	DWG NO	Rev
Custom			

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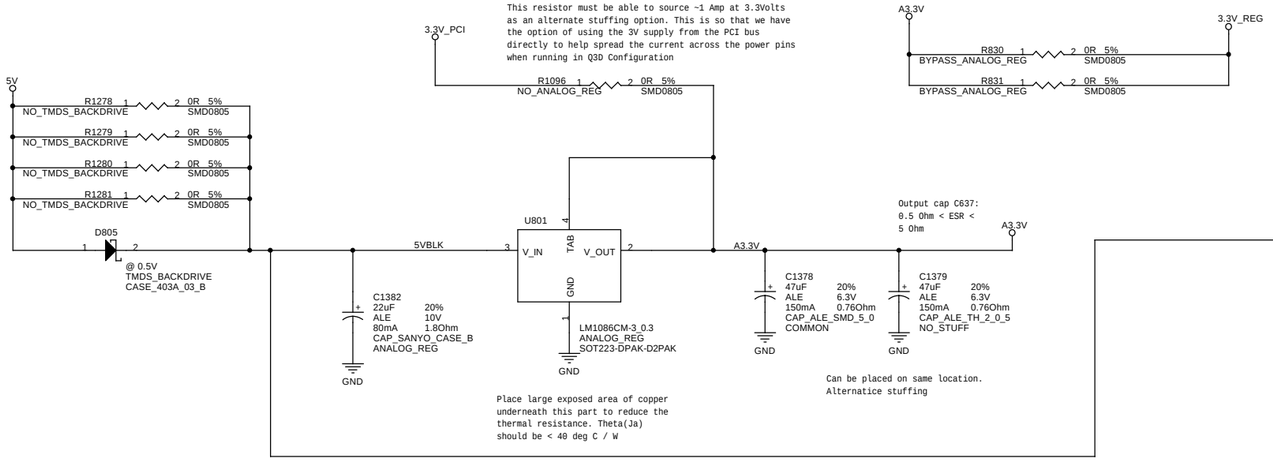
Analog 3.3V

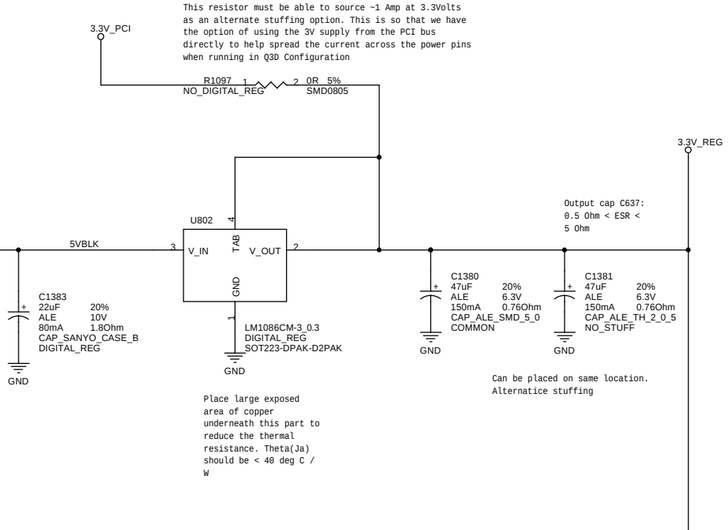
The Analog 3.3V feeds the TMDS and DAC components and GPU pll's. It should source ~1.2 Amps maximum.

Since we now have TMDS from another regulator, we can probably load one linear regulator with both nets. These resistors allow you to drive the digital connectiosn from analog - this is for a bom pricing solution and will compromise analog supply noise levels.

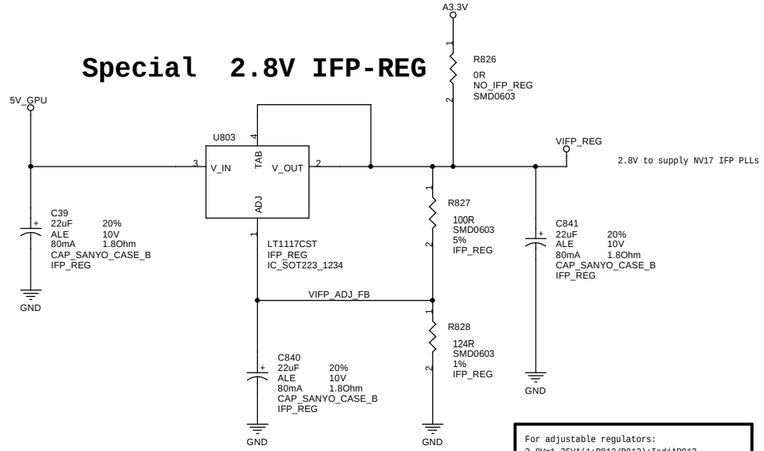


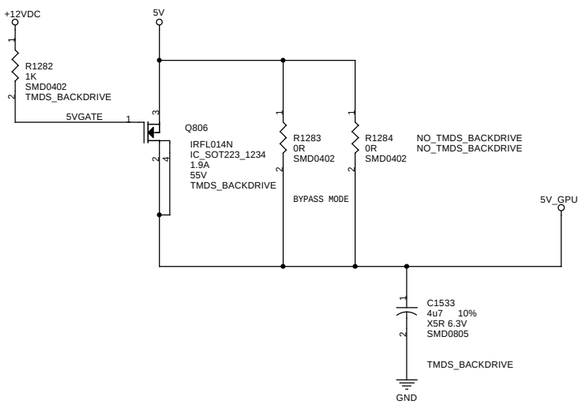
Regulated 3.3V

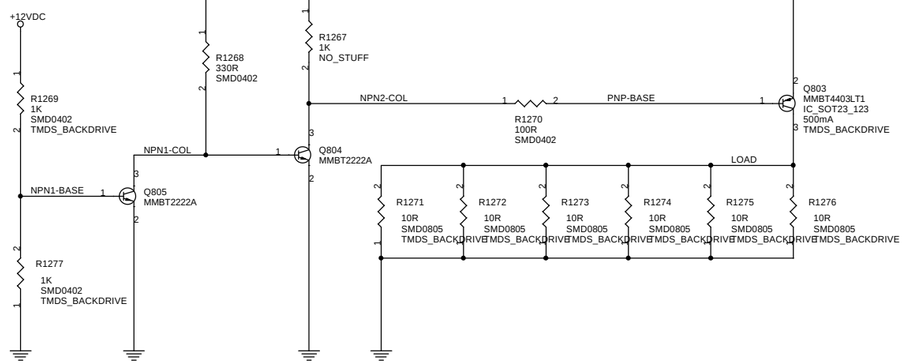
The Digital 3.3V plane needs to source at least 1 Amp to drive the AGPVDDQ, VDD33 and miscellaneous 3 volt components on the PCB



Special 2.8V IFP-REG







5.b Regulated 3.3V supplies

NVIDIA	NVIDIA Corporation 2701 San Tomas Expressway Santa Clara, CA 95050, USA		GPU
	P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz		
	Size: Custom	CAGE Code	DWG NO / Rev
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M3

Passive
HEATSINK_45MM_PP
PASSIVE_HS

M4

Passive
HEATSINK_45MM_PP
PASSIVE_HS

M2

BRKT_PCI_DUAL_LFH60
BRKT, DUAL 60PIN (LFH) (1.234) and (3.055)
COMMON

6.a Mechanicals

NVIDIA Corporation
2701 San Tomas Expressway
Santa Clara, CA 95050, USA

GPU

P77, Dual NV17, 4MX32 DDR, 32MB/64MB, Quad Head, Dual LFH to VGA/DVI, PCI 33/66 MHz

Size	CAGE Code	DWG NO	Rev
Custom			

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Scale

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