

A	B	C	D	E	F	G	H
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1

2

34

Block Diagram

DP

DP / HDMI

DP

DP

DVI-I

LINK C

LINK D

LINK A

LINK B

LINK AB

GP107

MEM B LO

MEM B HI

MEM A LO

MEM A HI

5V LDO

Fan

Power Supply FBVDD / FBVDDQ

Power Supply NVVDD-PH3

Power Supply NVVDD-PH1

Power Supply NVVDD-PH2

PEX_VDD

IO_VDD

EXT6_12V

DET

PEX_12V Finger

PEX_3V3 Finger

ASSEMBLY

PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL

Block Diagram

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Block Diagram

DP

DP / HDMI

DP

DP

DVI-I

LINK C

LINK D

LINK A

LINK B

LINK AB

GP107

MEM B LO

MEM B HI

MEM A LO

MEM A HI

5V LDO

Fan

Power Supply FBVDD / FBVDDQ

Power Supply NVVDD-PH3

Power Supply NVVDD-PH1

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EXT6_12V

DET

PEX_12V Finger

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ASSEMBLY

PAGE DETAIL

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Block Diagram

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Block Diagram

DP

DP / HDMI

DP

DP

DVI-I

LINK C

LINK D

LINK A

LINK B

LINK AB

GP107

MEM B LO

MEM B HI

MEM A LO

MEM A HI

5V LDO

Fan

Power Supply FBVDD / FBVDDQ

Power Supply NVVDD-PH3

Power Supply NVVDD-PH1

Power Supply NVVDD-PH2

PEX_VDD

IO_VDD

EXT6_12V

DET

PEX_12V Finger

PEX_3V3 Finger

ASSEMBLY

PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL

Block Diagram

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This diagram illustrates the Block Diagram of the GP107 GPU system, showing its connections to various components.

The central component is the **GP107** GPU, which interfaces with several input/output ports and memory modules:

- Input/Output Ports:** DP, DP/HDMI, DP, DVI-I, and DP.
- Memory Modules:** MEM B LO, MEM B HI, MEM A LO, and MEM A HI.

The GPU is connected to a series of power supply rails and other system components:

- Power Supply Rails:** FBVDD/FBVDDQ, NVVDD-PH3, NVVDD-PH1, NVVDD-PH2, PEX_VDD, and IO_VDD.
- Other Components:** 5V LDO, Fan, EXT6_12V, DET, PEX_12V Finger, and PEX_3V3 Finger.

The diagram shows the following connections:

- DP, DP/HDMI, DP, DVI-I, and DP are connected to the GPU via LINK C, LINK D, LINK A, LINK B, and LINK AB respectively.
- MEM B LO and MEM B HI are connected to the GPU via LINK C and LINK D respectively.
- MEM A LO and MEM A HI are connected to the GPU via LINK A and LINK B respectively.
- The GPU is connected to the Power Supply FBVDD/FBVDDQ, NVVDD-PH3, NVVDD-PH1, NVVDD-PH2, PEX_VDD, and IO_VDD.
- The Power Supply FBVDD/FBVDDQ is connected to the 5V LDO and Fan.
- The Power Supply NVVDD-PH3 is connected to the EXT6_12V and DET.
- The Power Supply NVVDD-PH1 is connected to the PEX_12V Finger.
- The Power Supply NVVDD-PH2 is connected to the PEX_3V3 Finger.
- The PEX_VDD and IO_VDD are connected to the PEX_3V3 Finger.

Legend:

ASSEMBLY	PAGE DETAIL
BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL	Block Diagram

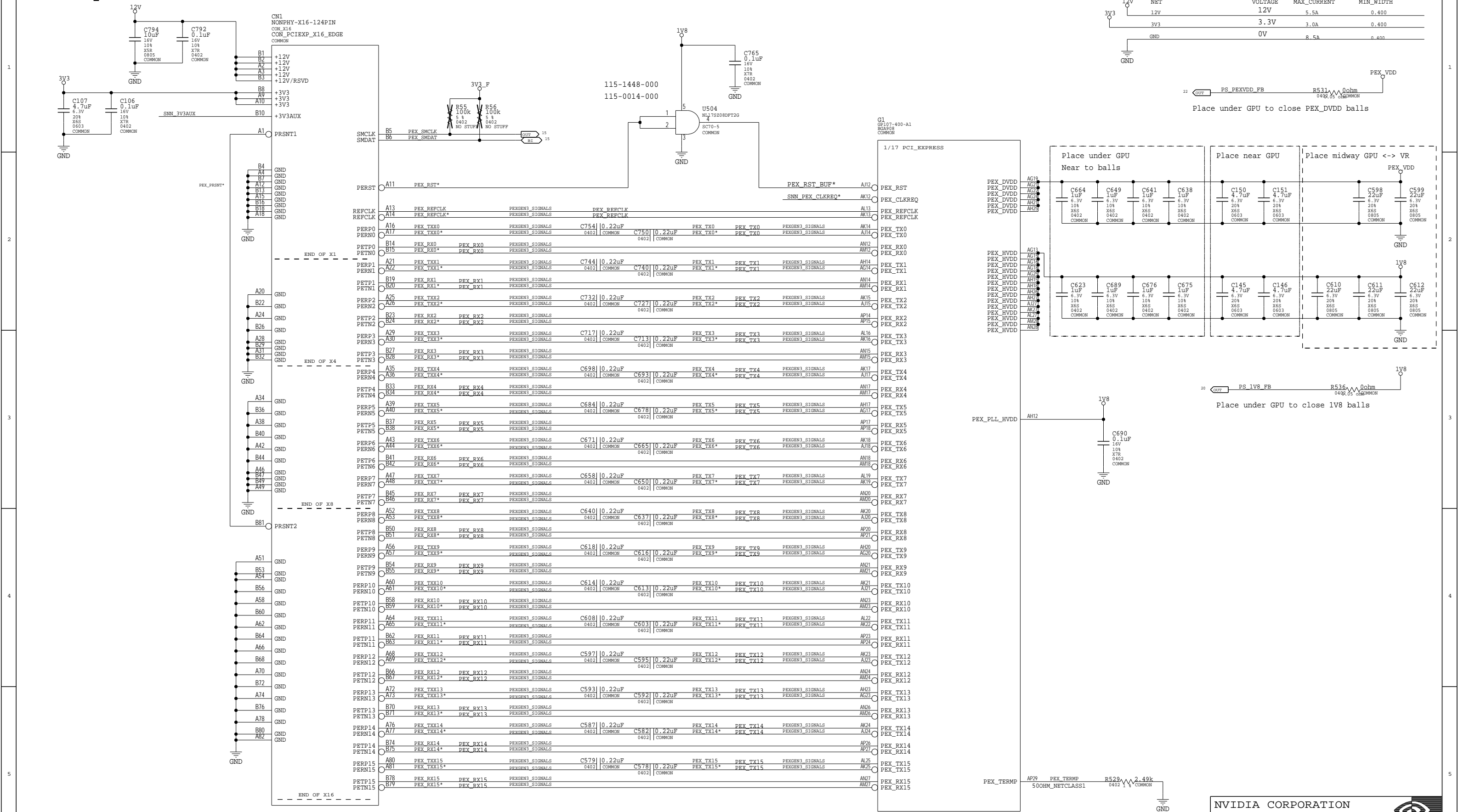
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PCI Express



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PAGE DETAIL	PCI Express

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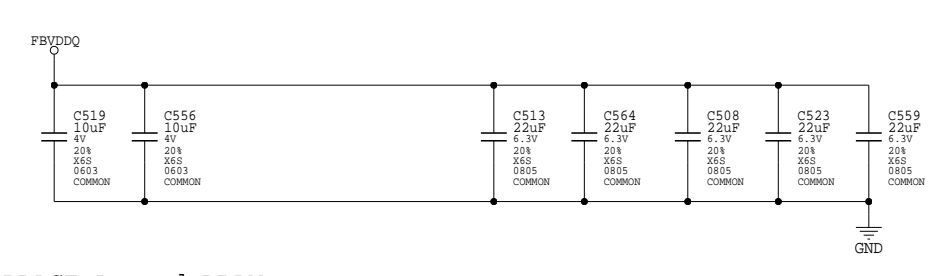
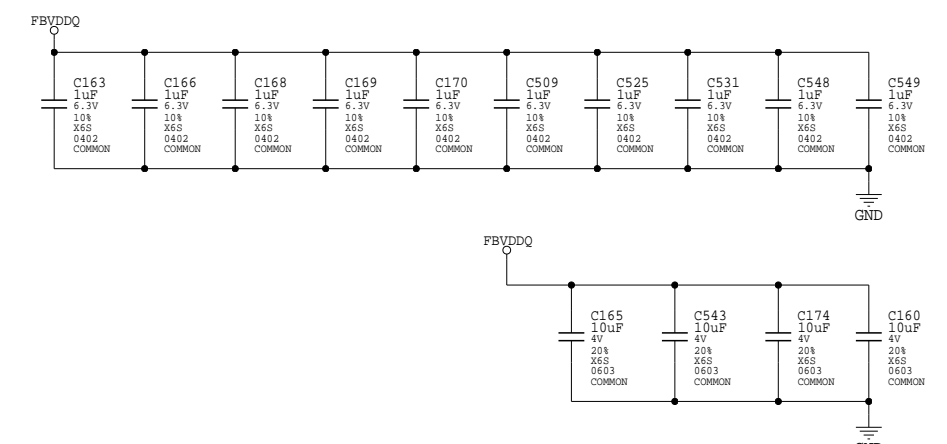
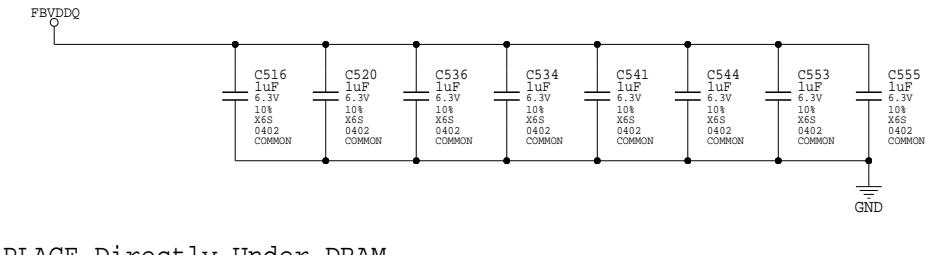
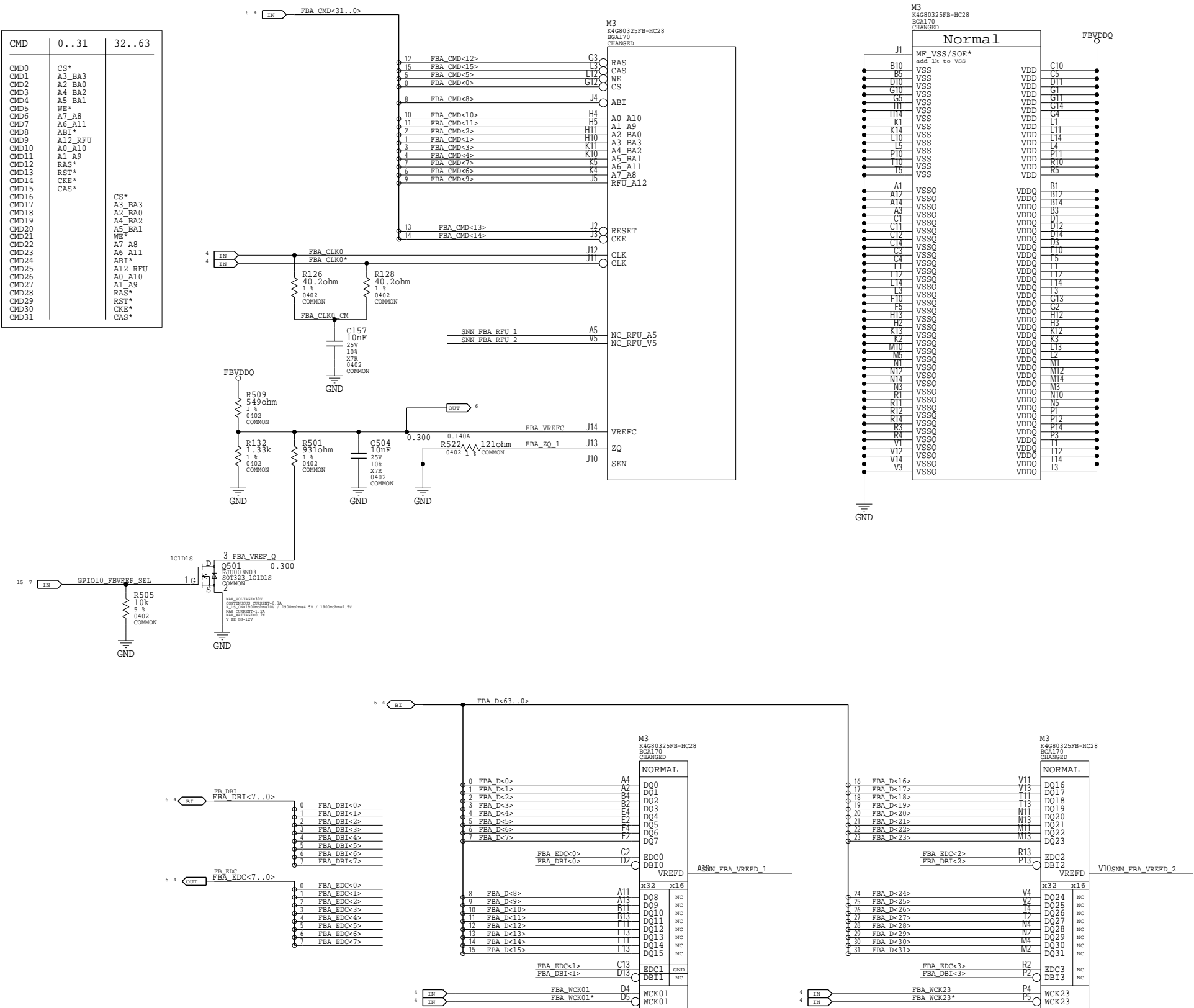
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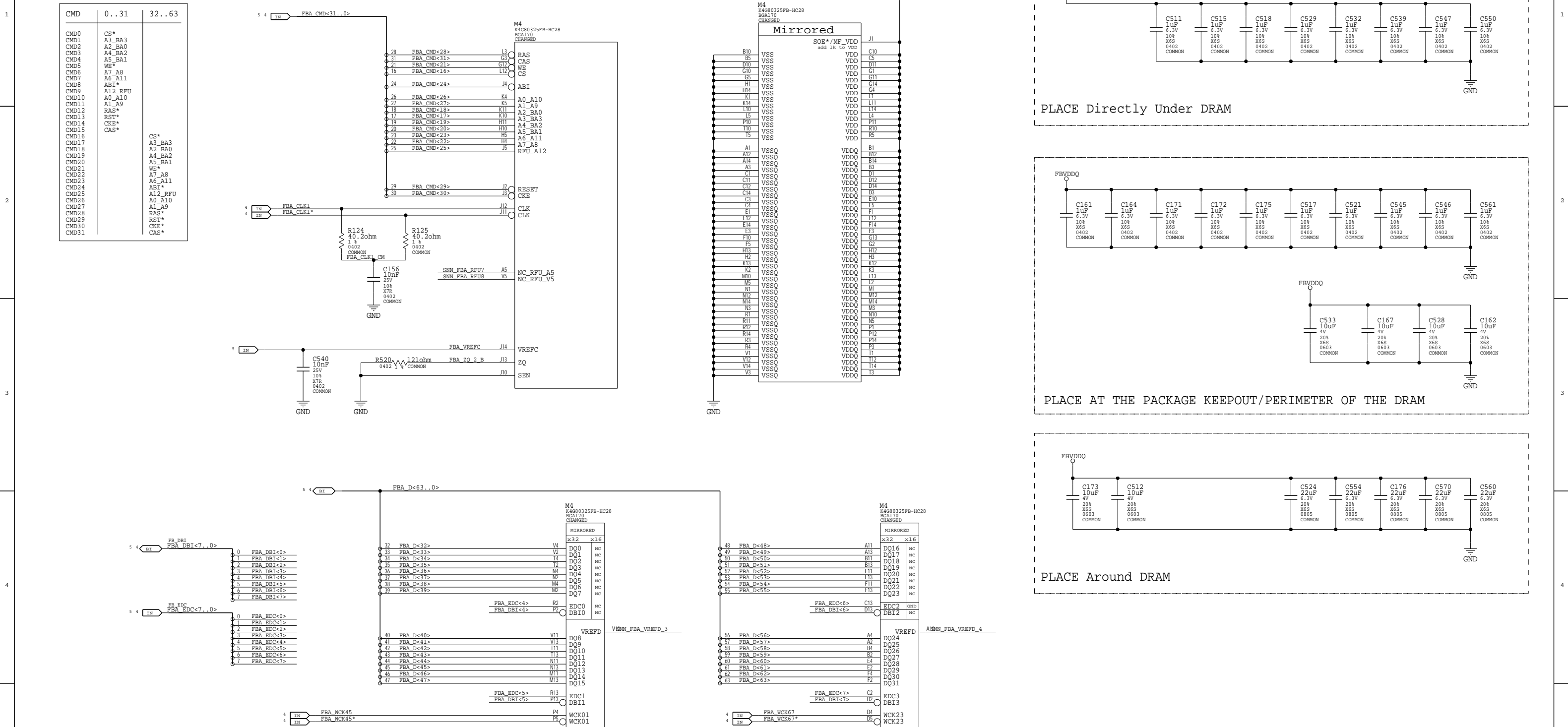
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: GPU Partition A/B

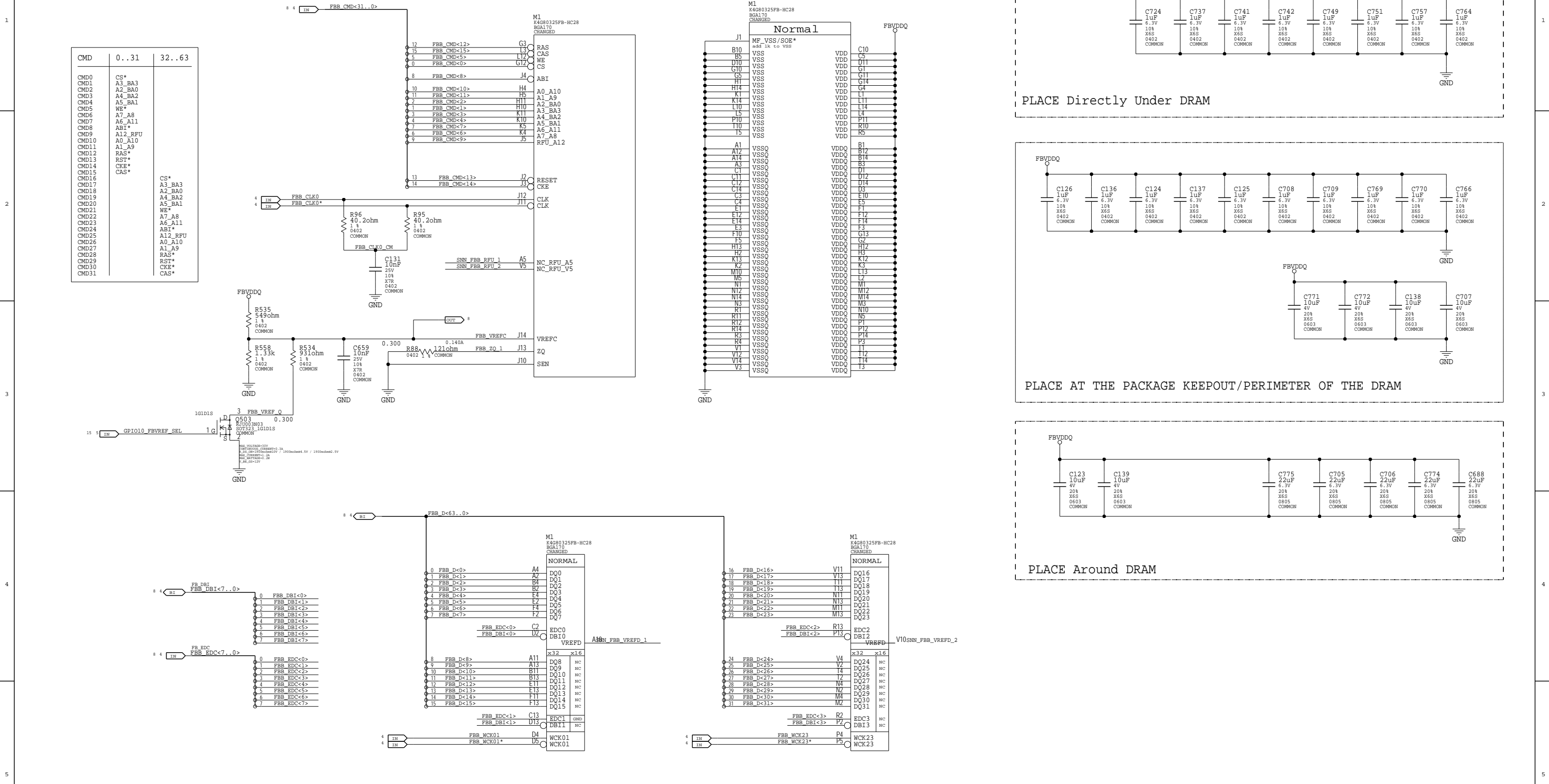
MEMORY: FBA Partition 31..0



MEMORY: FBA Partition 63..32



MEMORY: FBB Partition 31..0



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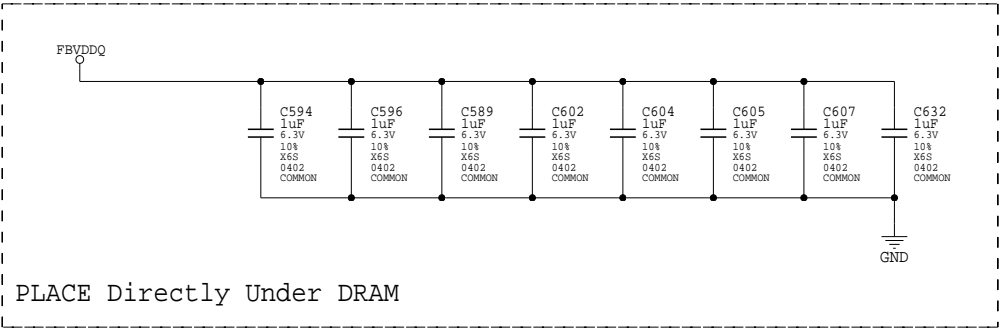
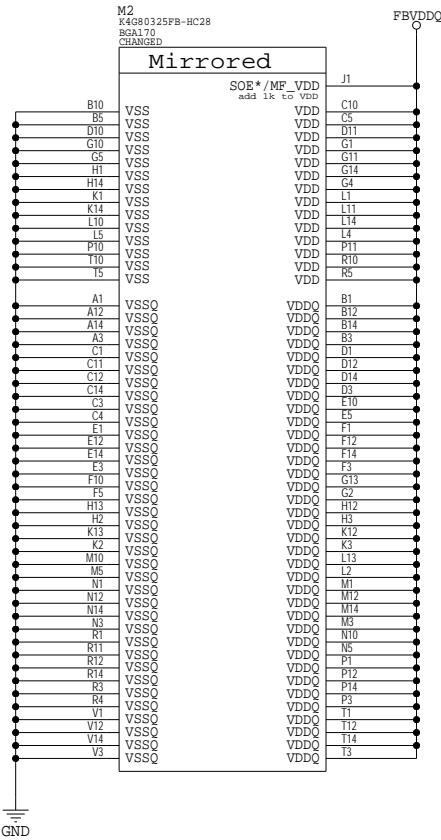
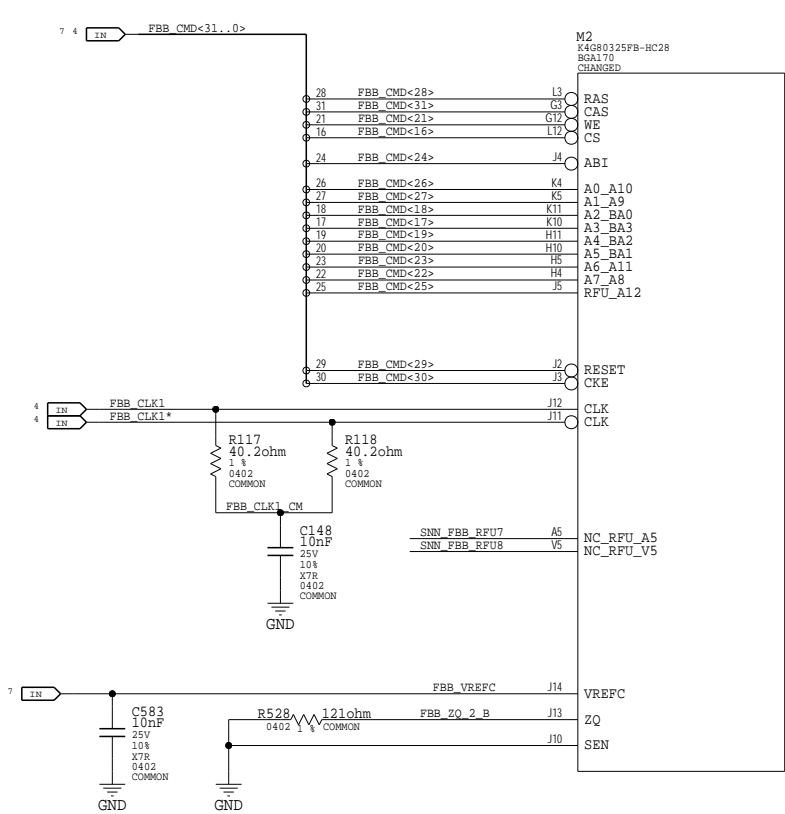
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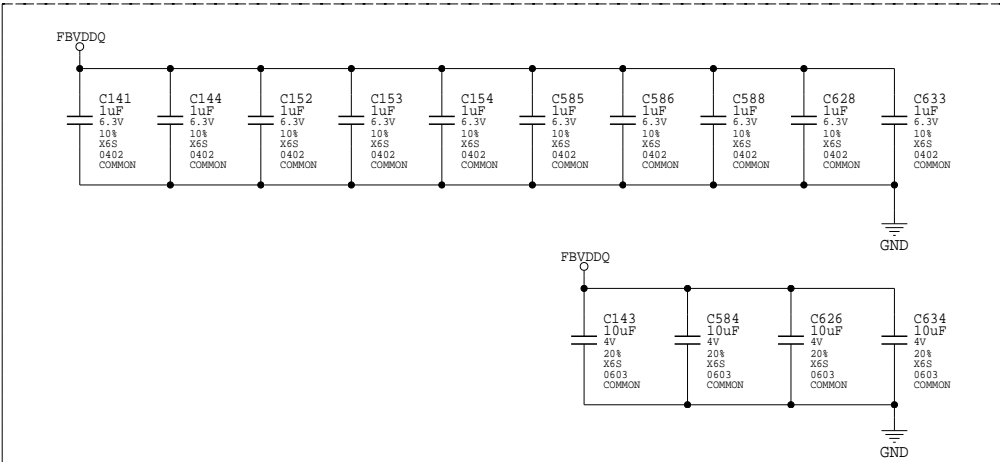
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MEMORY: FBB Partition 63..32

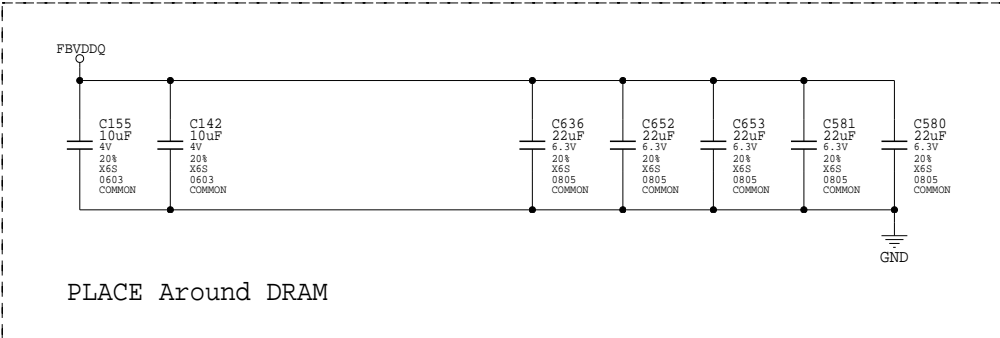
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CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



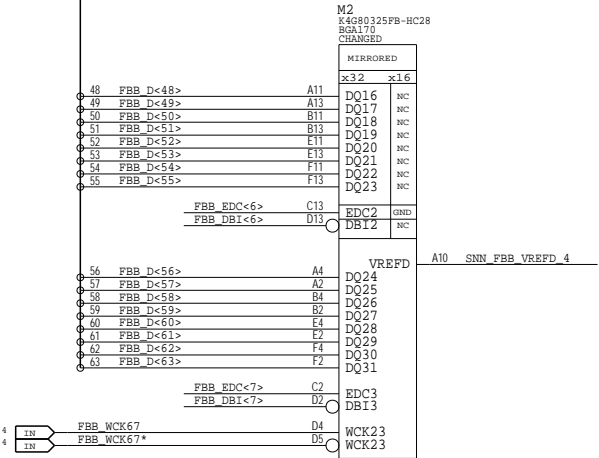
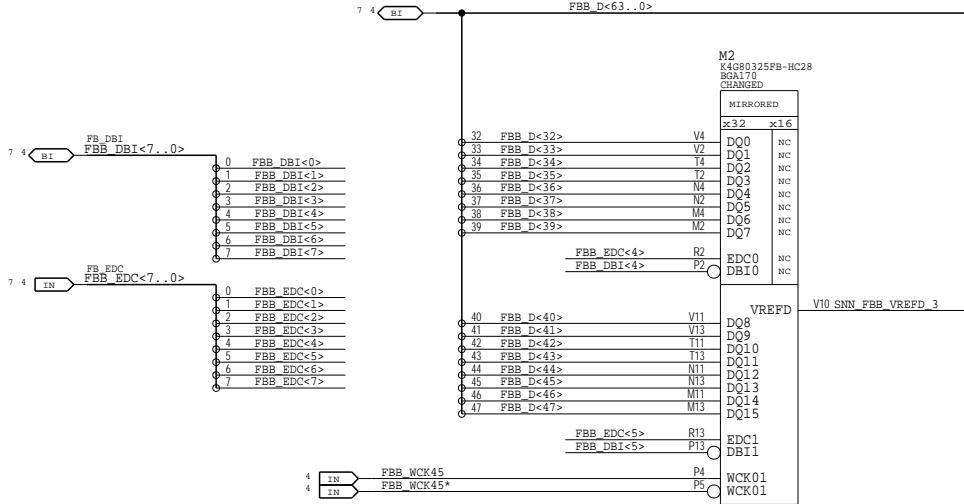
PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM



PLACE Around DRAM



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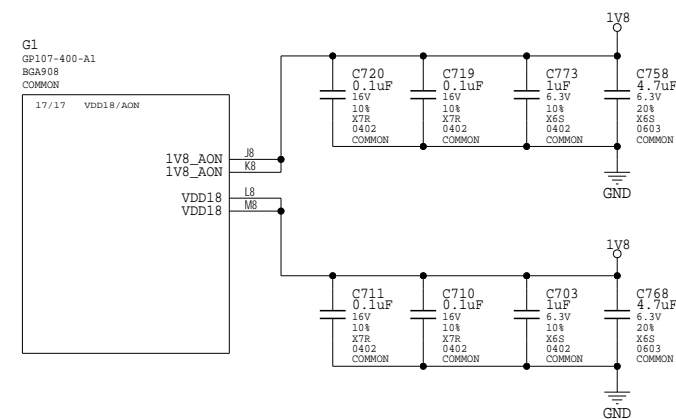
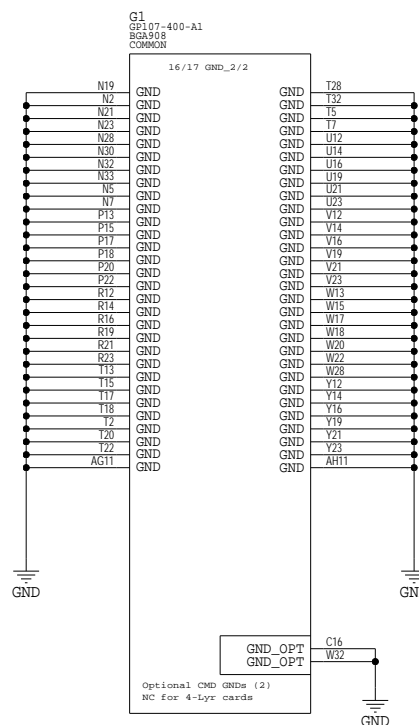
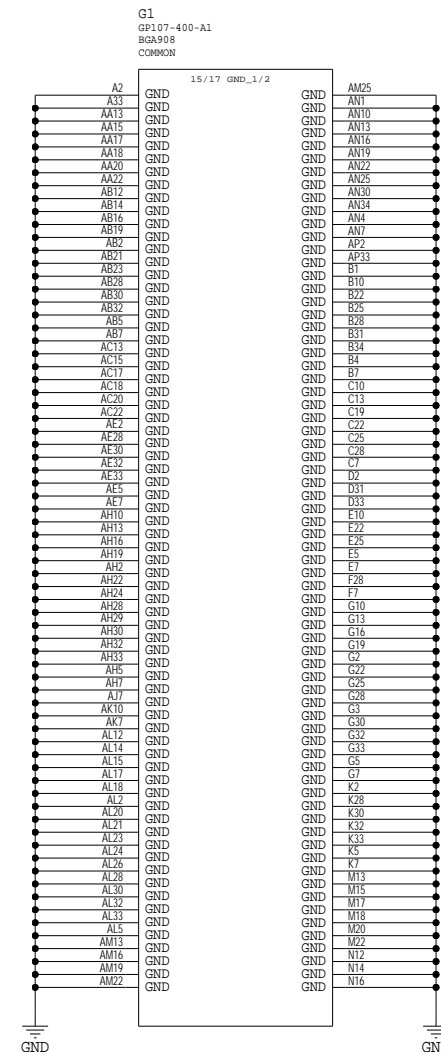
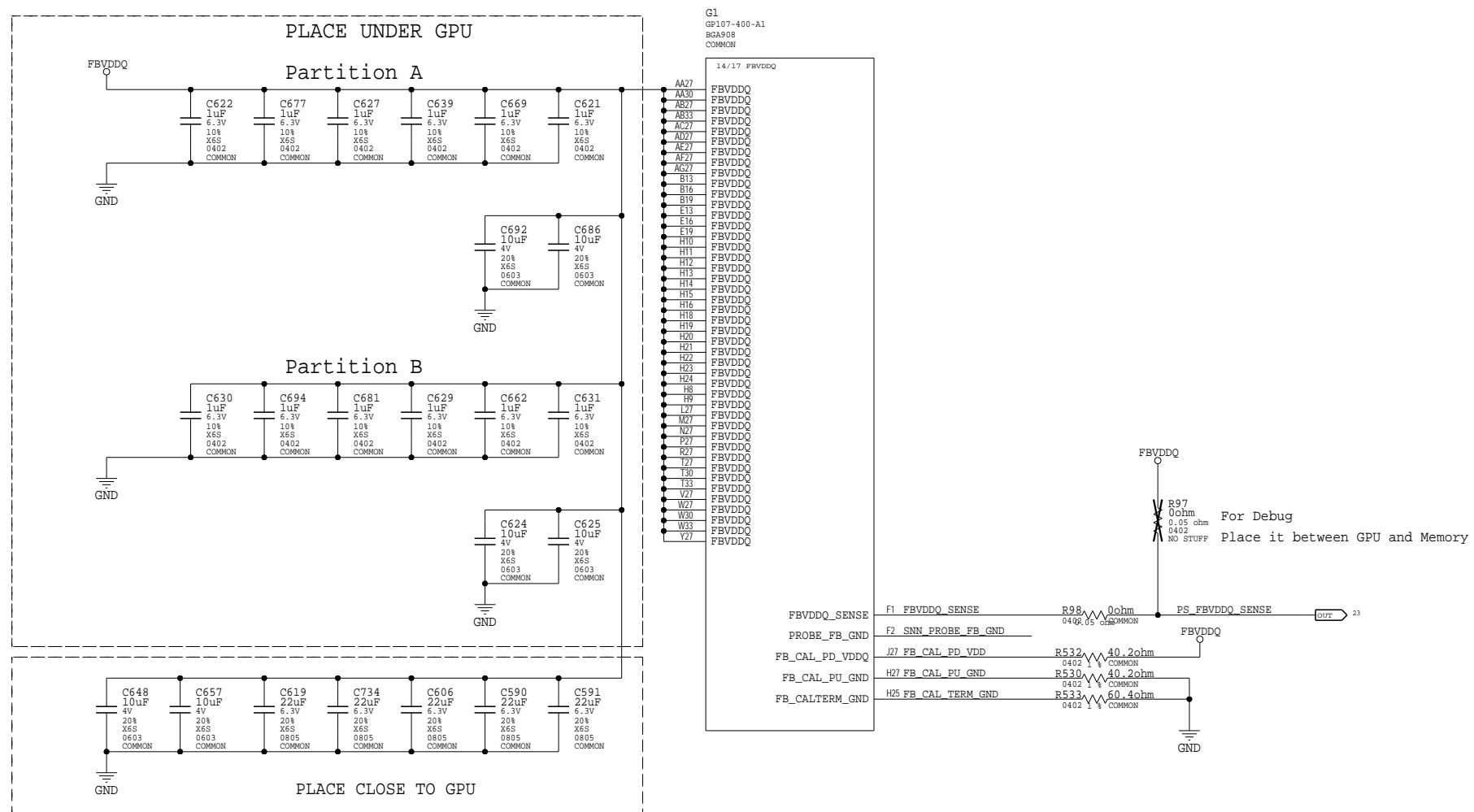
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GPU FBVDDQ & 1V8 Decoupling



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PAGE DETAIL	GPU FBVDDQ & I/V8 Decoupling

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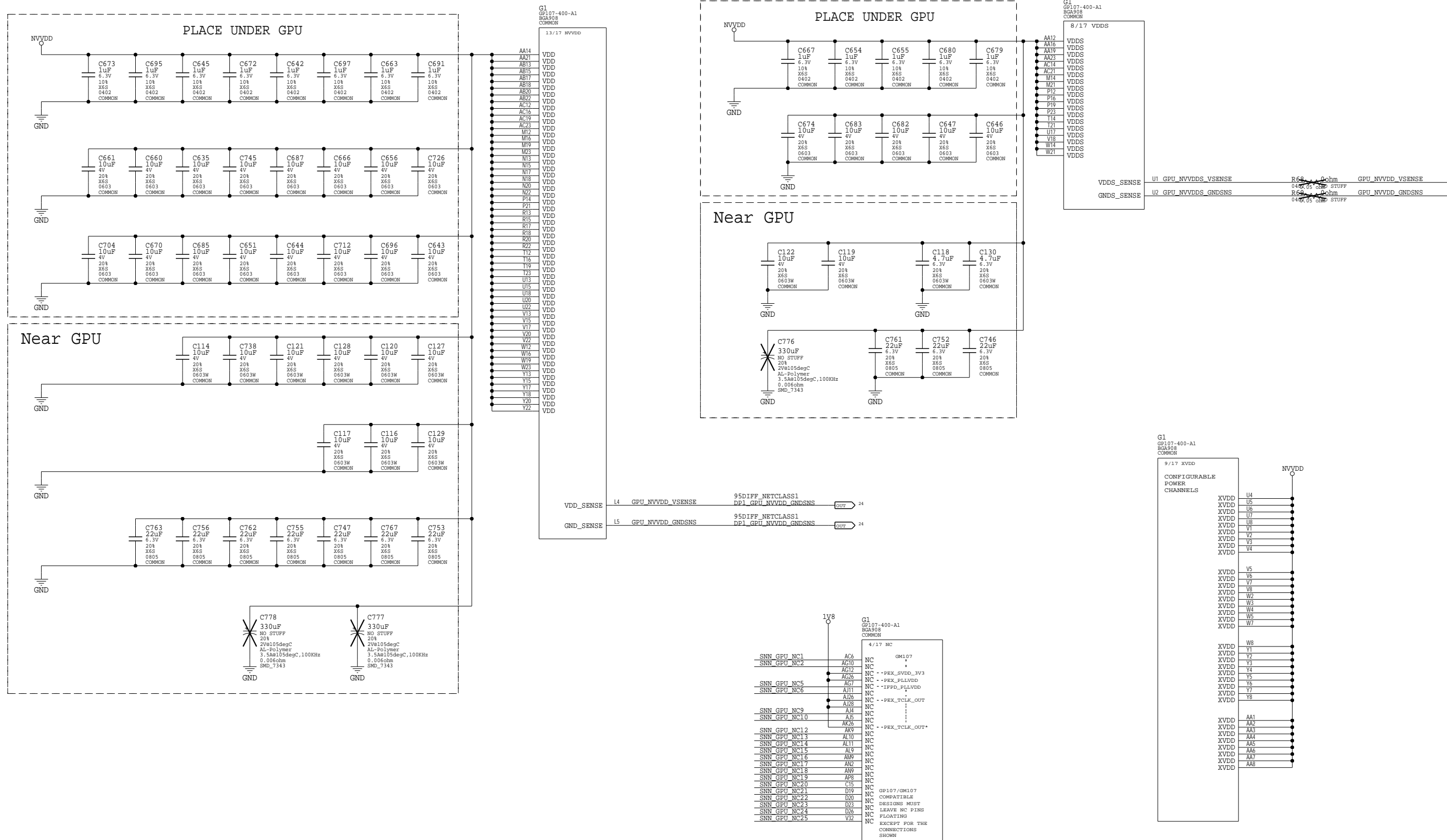
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GPU NVVDD & NVVDDS Decoupling



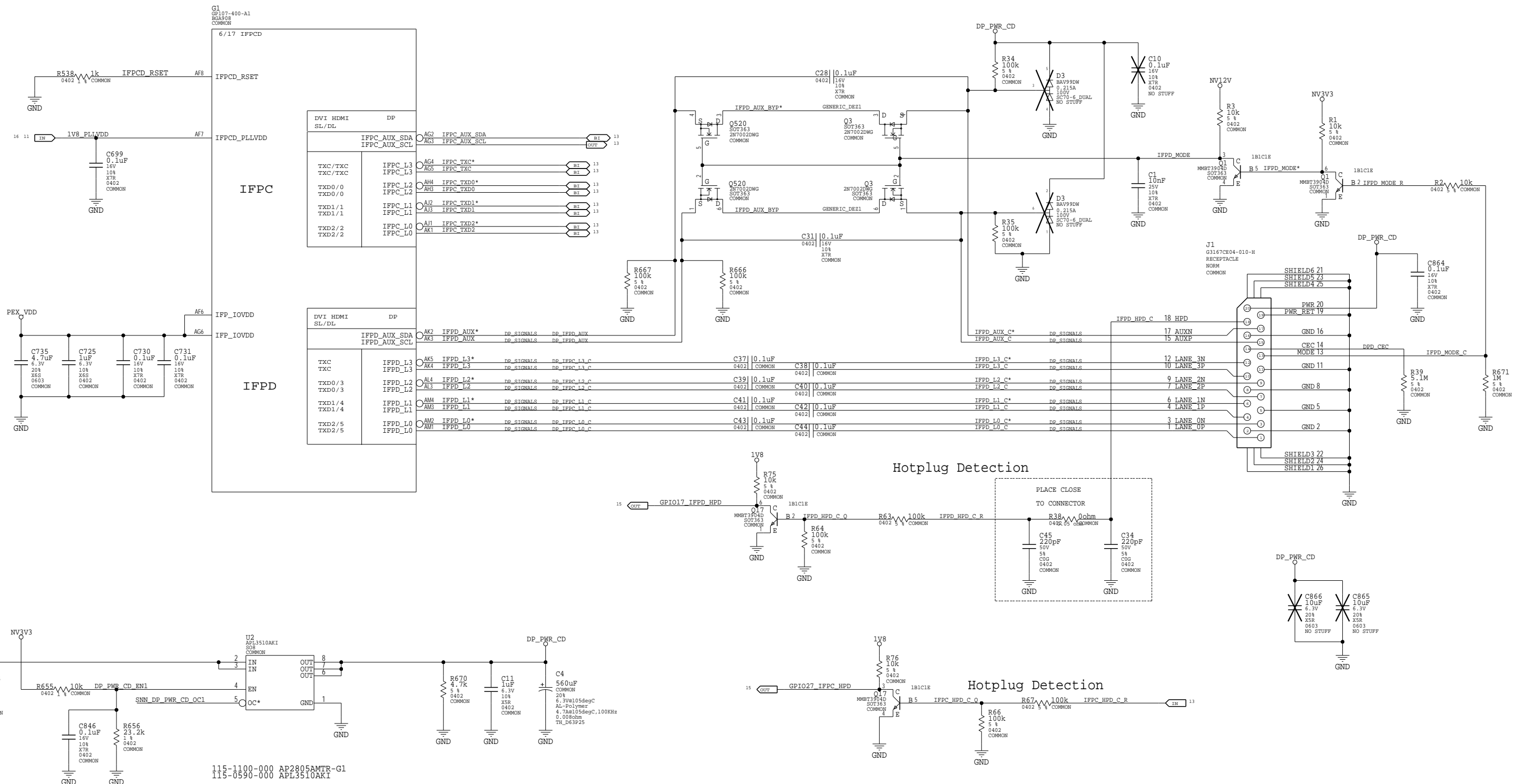
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IFPD DP



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PAGE DETAIL	IFPD DP

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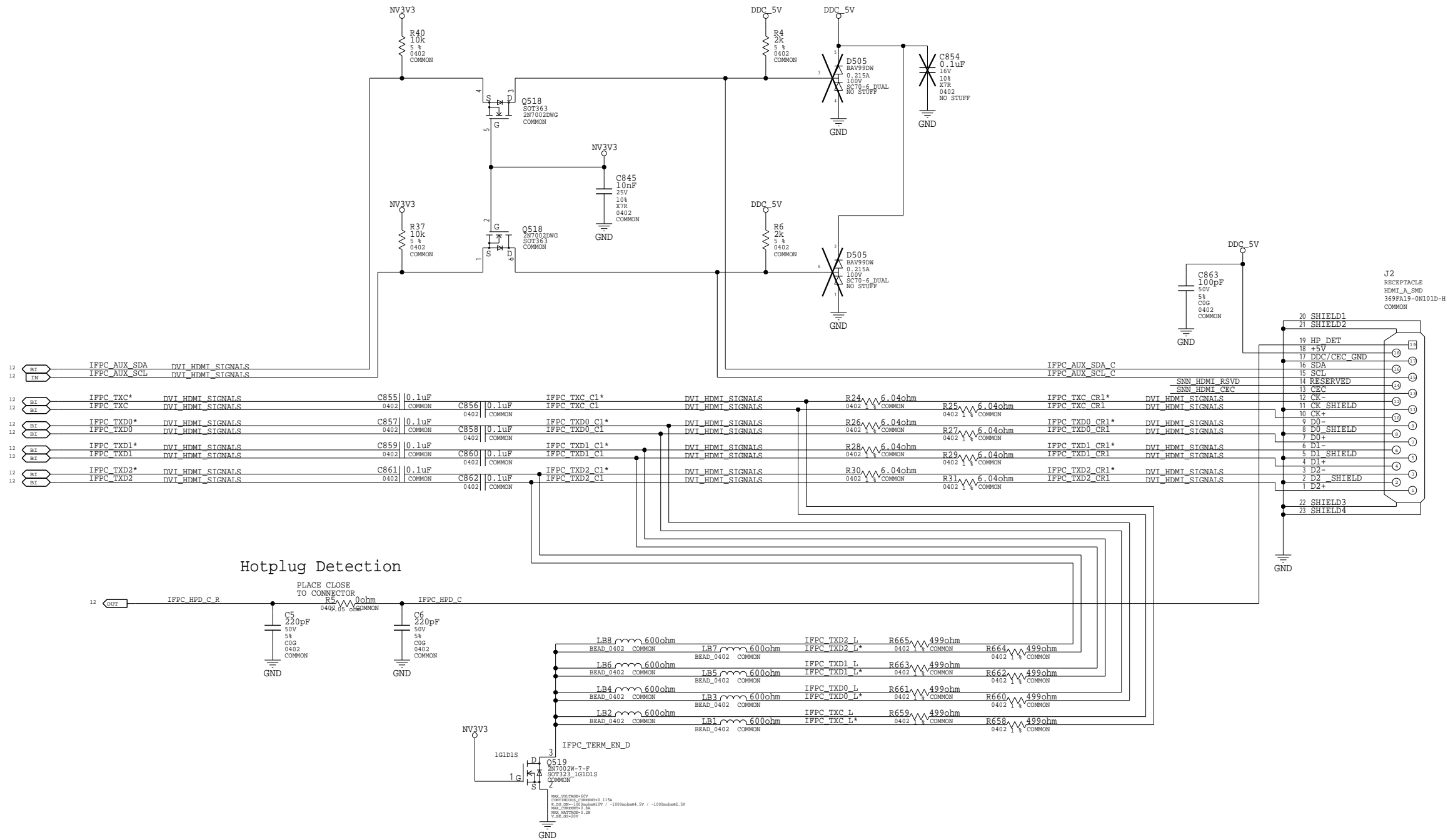
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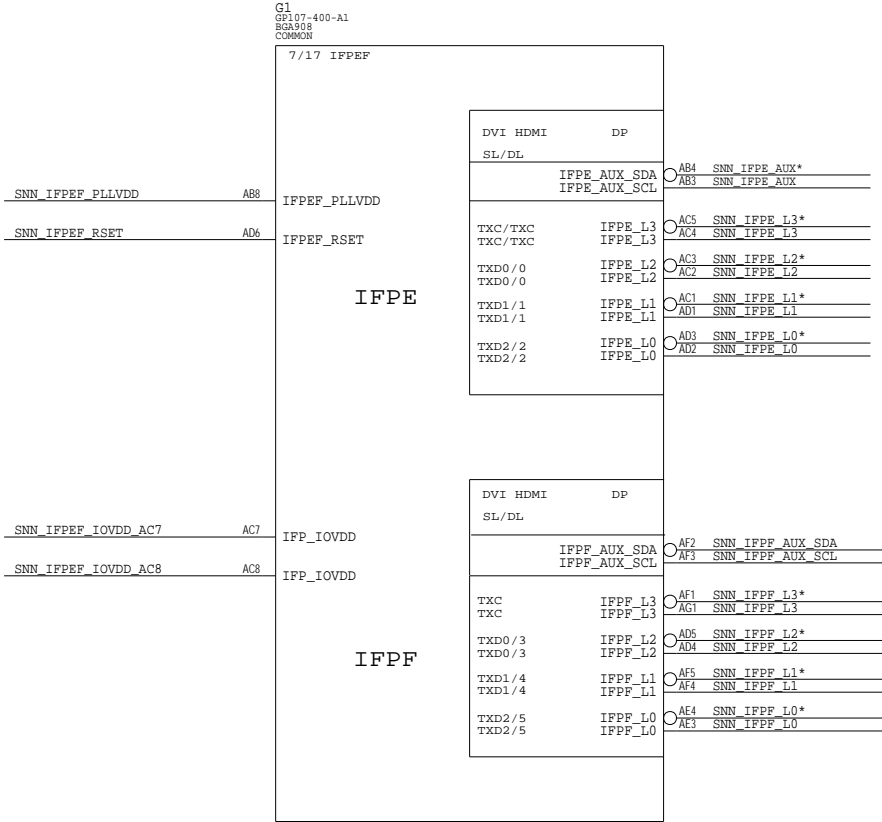


IFPC HDMI



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MISC1: GPIO, Fan, Thermal, JTAG

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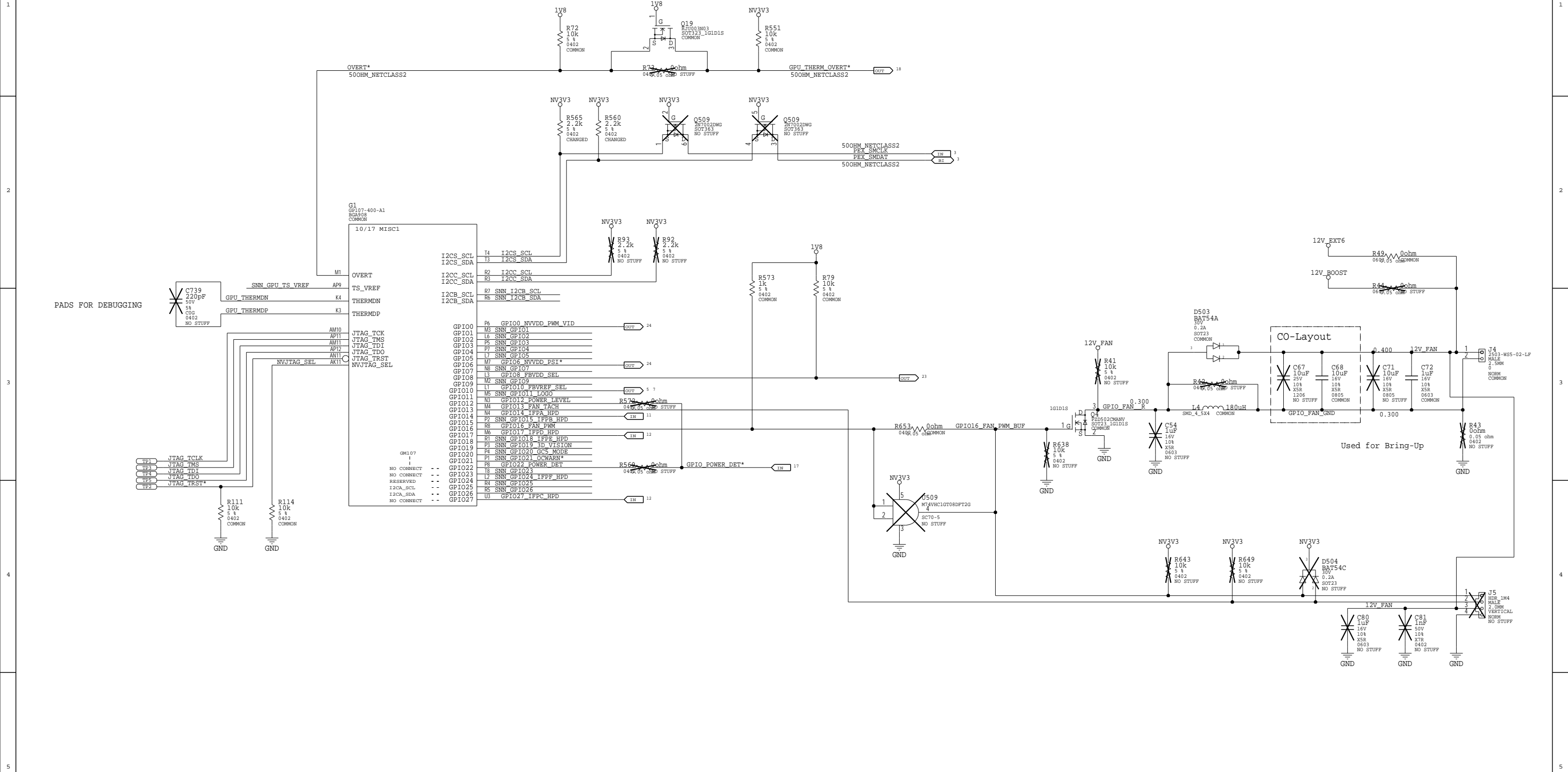
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PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO

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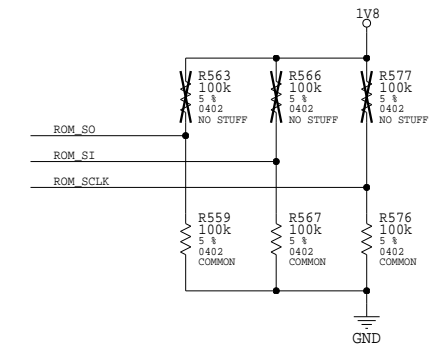
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MISC2: ROM, XTAL, Straps

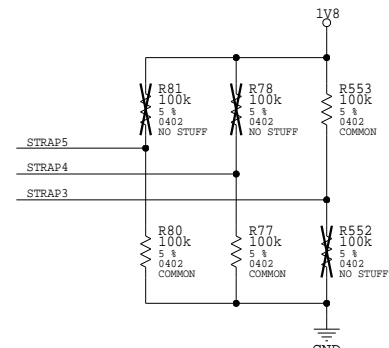
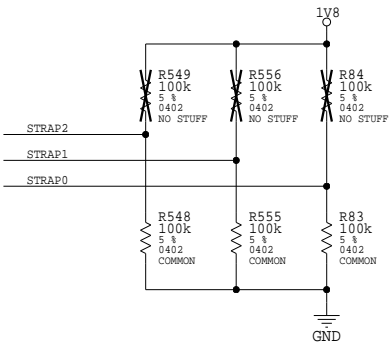
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L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

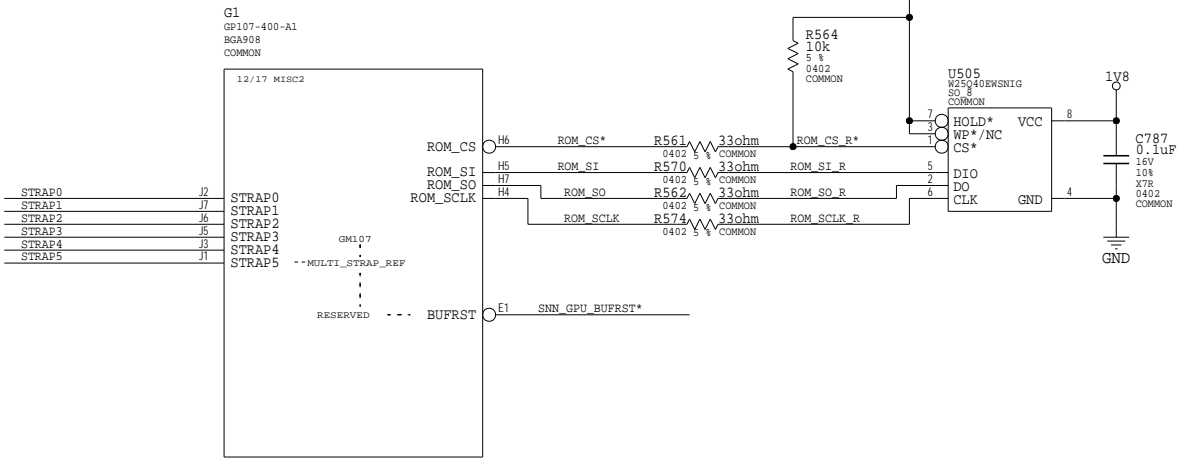


1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

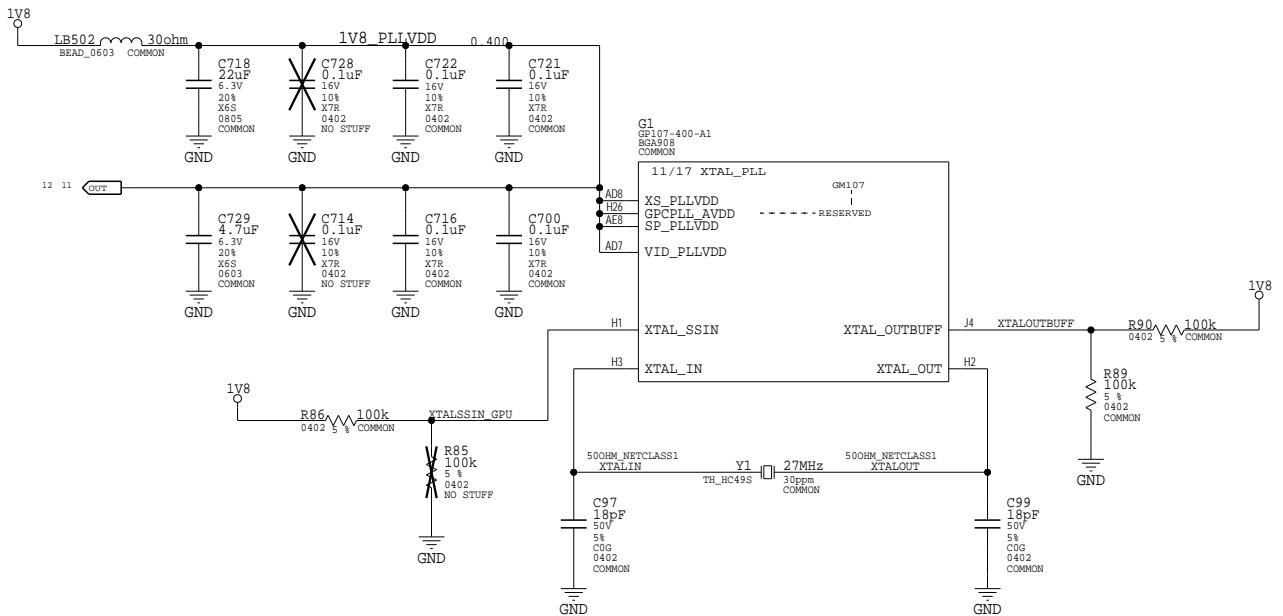
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



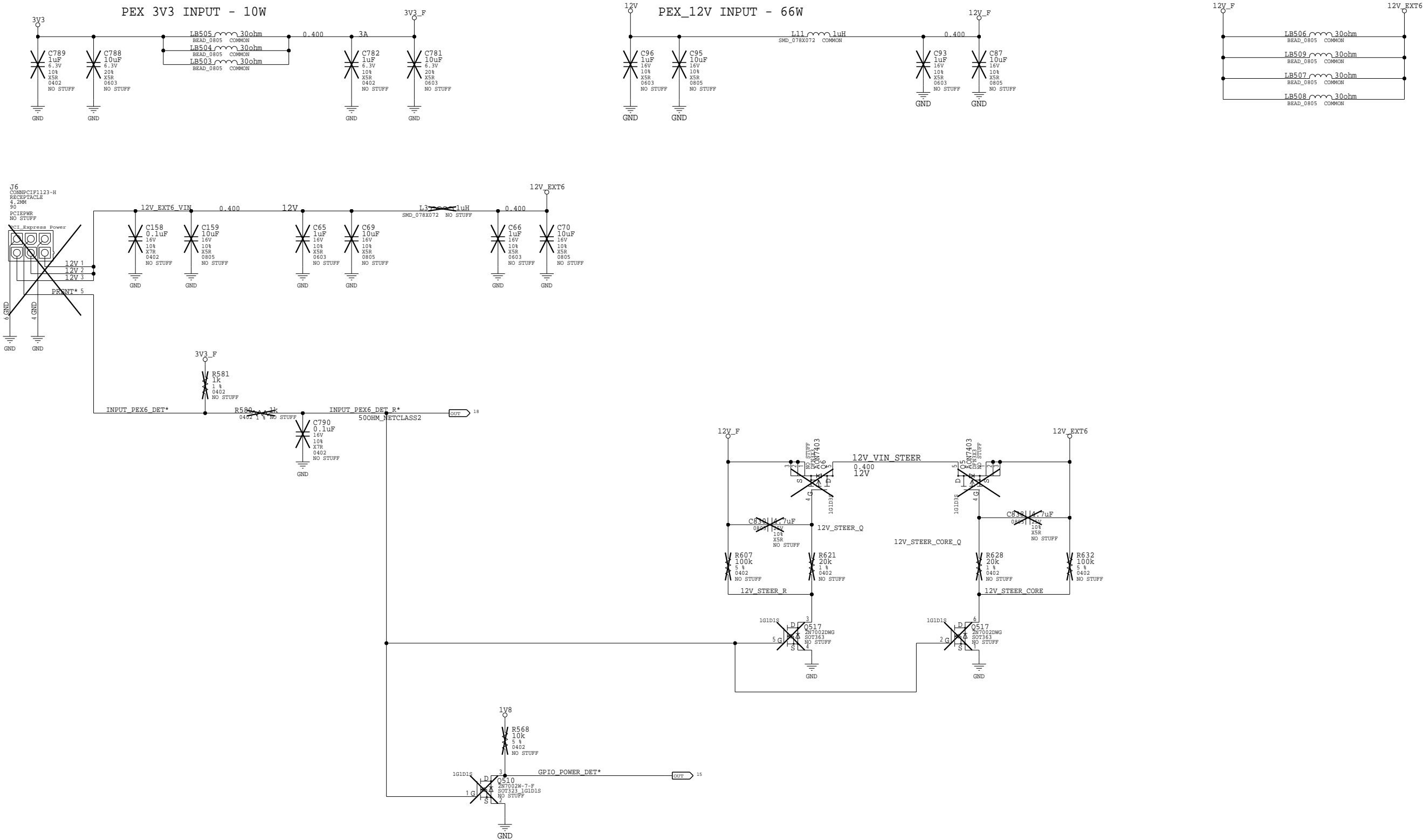
Smart Fan

XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



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Power Inputs and Filtering



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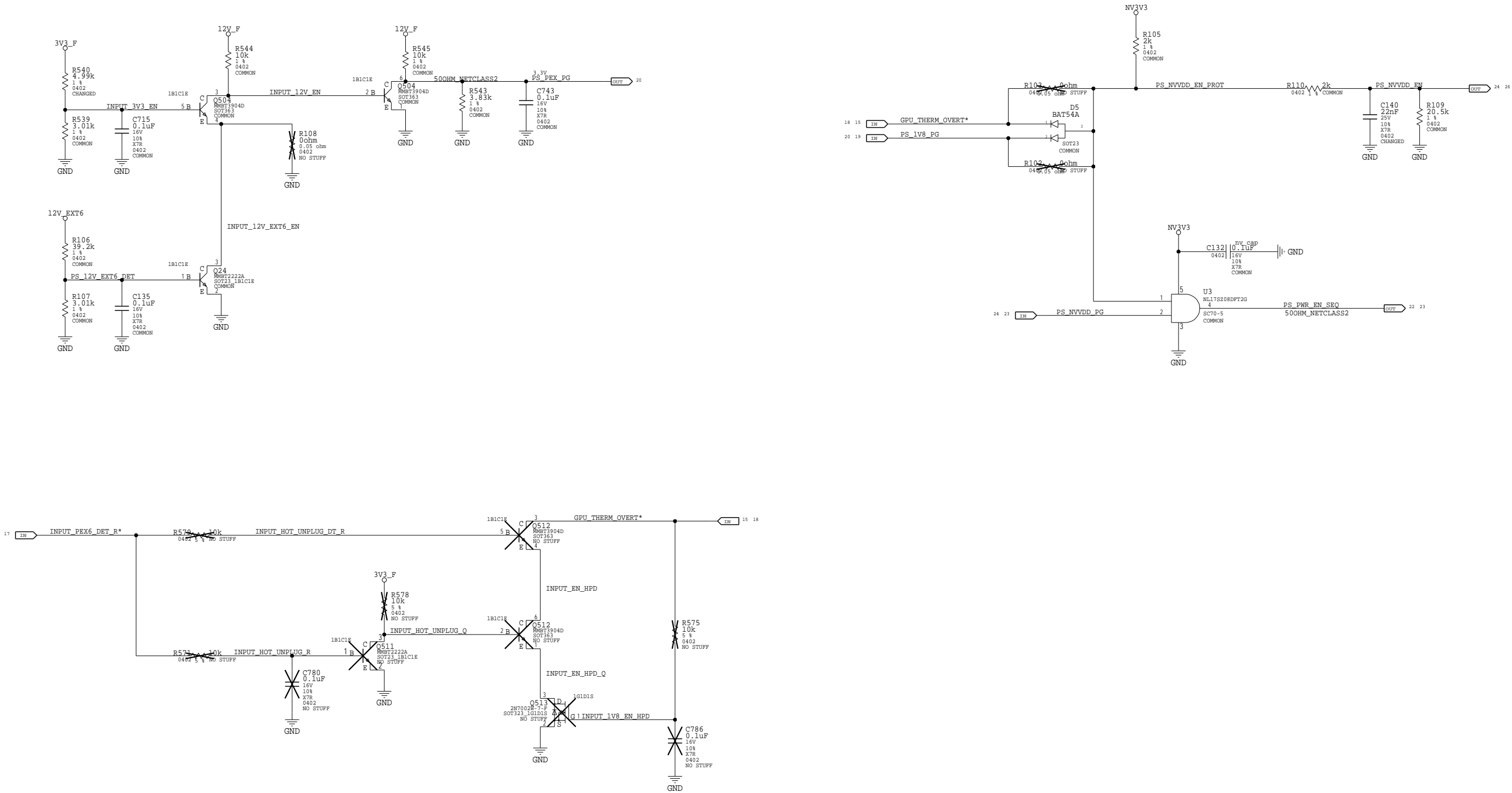
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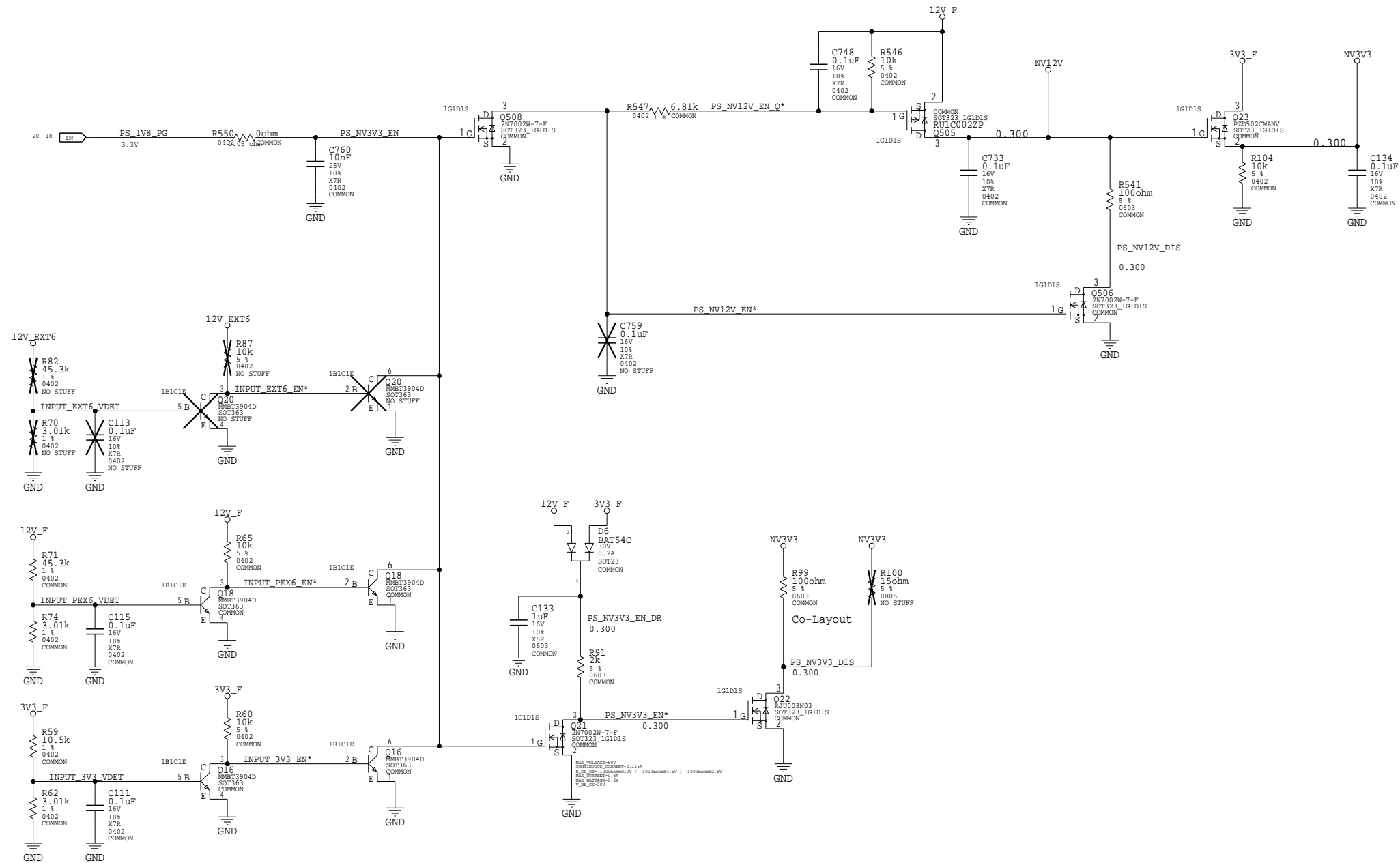
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Power sequence




PS: NV3V3 & NV12V



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PAGE DETAIL	PS: NV3V3 & NV12V

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A	B	C	D	E	
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A

B

c

D

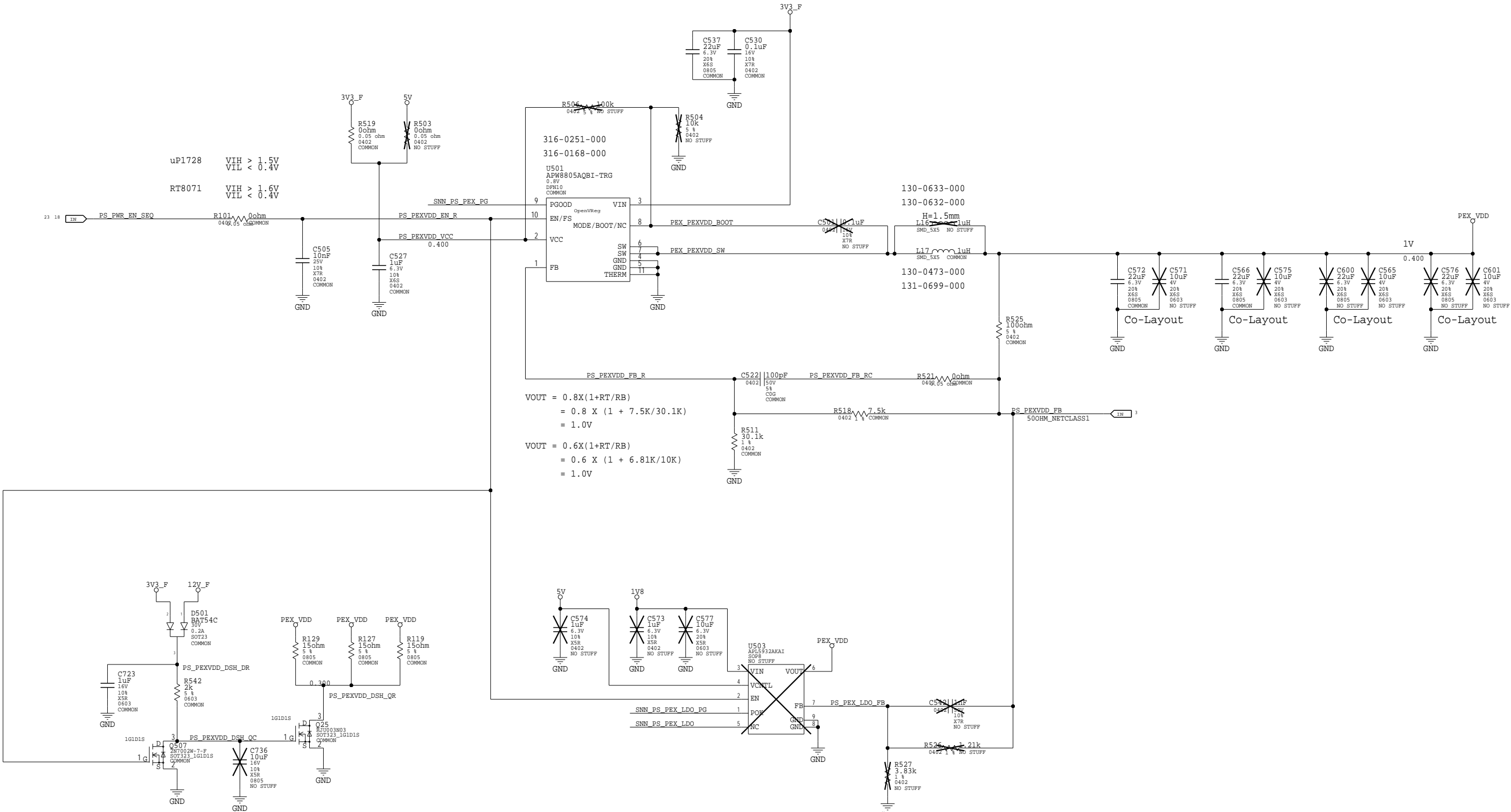
E

F₁

G

H


PS III: PEXVDD



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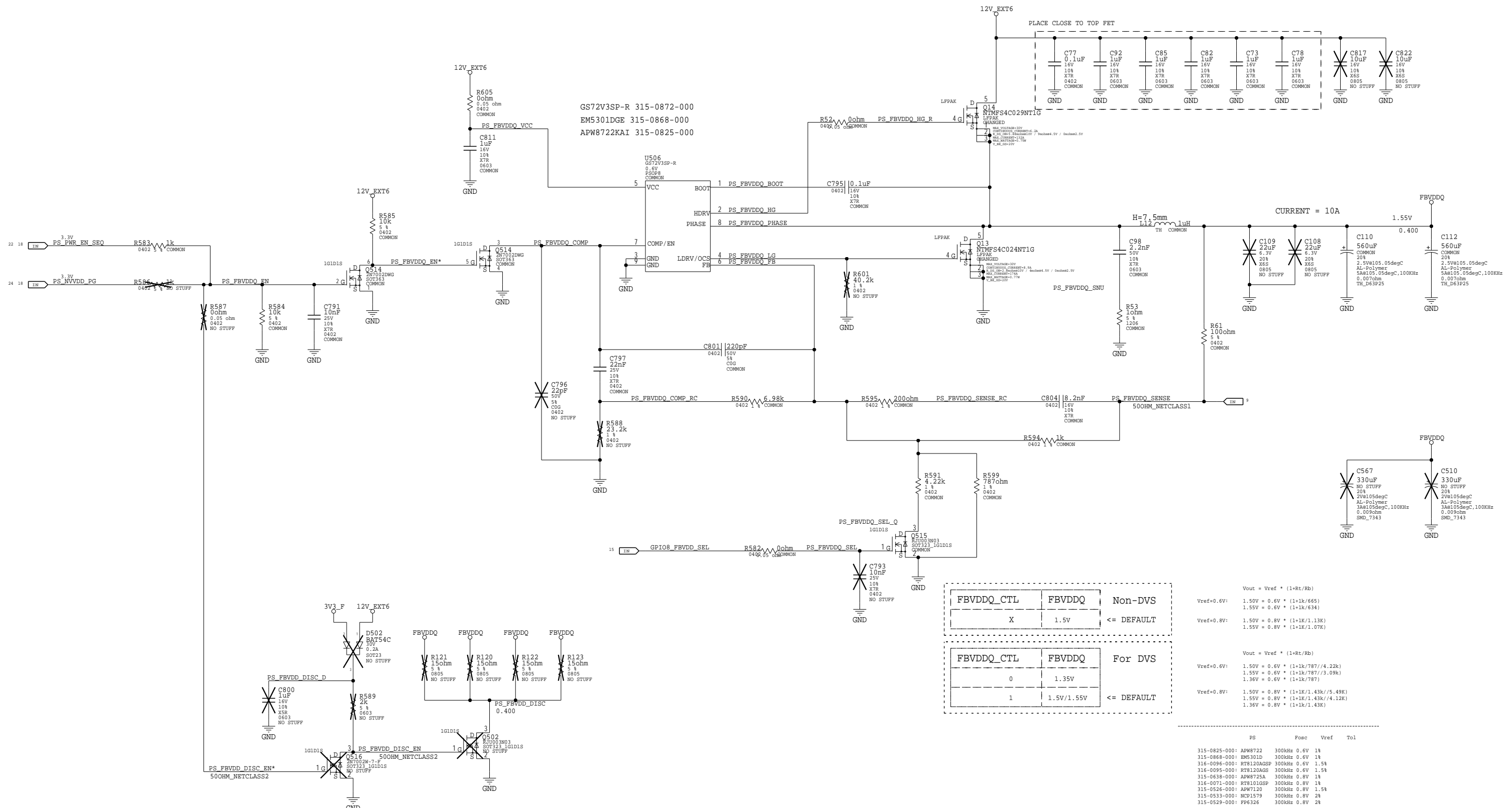
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PAGE DETAIL	PS III: PEXVDD

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PS IV: FBVDDQ



	PS	Fosc	Vref	Tol
315-0825-000:	APW8722	300kHz	0.6V	1%
315-0868-000:	EMS301D	300kHz	0.6V	1%
315-0096-000:	RT8120A0GS	300kHz	0.6V	1.5%
315-0095-000:	RT8120A0GS	300kHz	0.6V	1.5%
315-0638-000:	APW8725A	300kHz	0.8V	1%
315-0071-000:	RT8101G1SP	300kHz	0.8V	1%
315-0526-000:	APW7100	300kHz	0.8V	1.5%
315-0533-000:	NCP1579	300kHz	0.8V	2%
315-0529-000:	FP6326	300kHz	0.8V	2%

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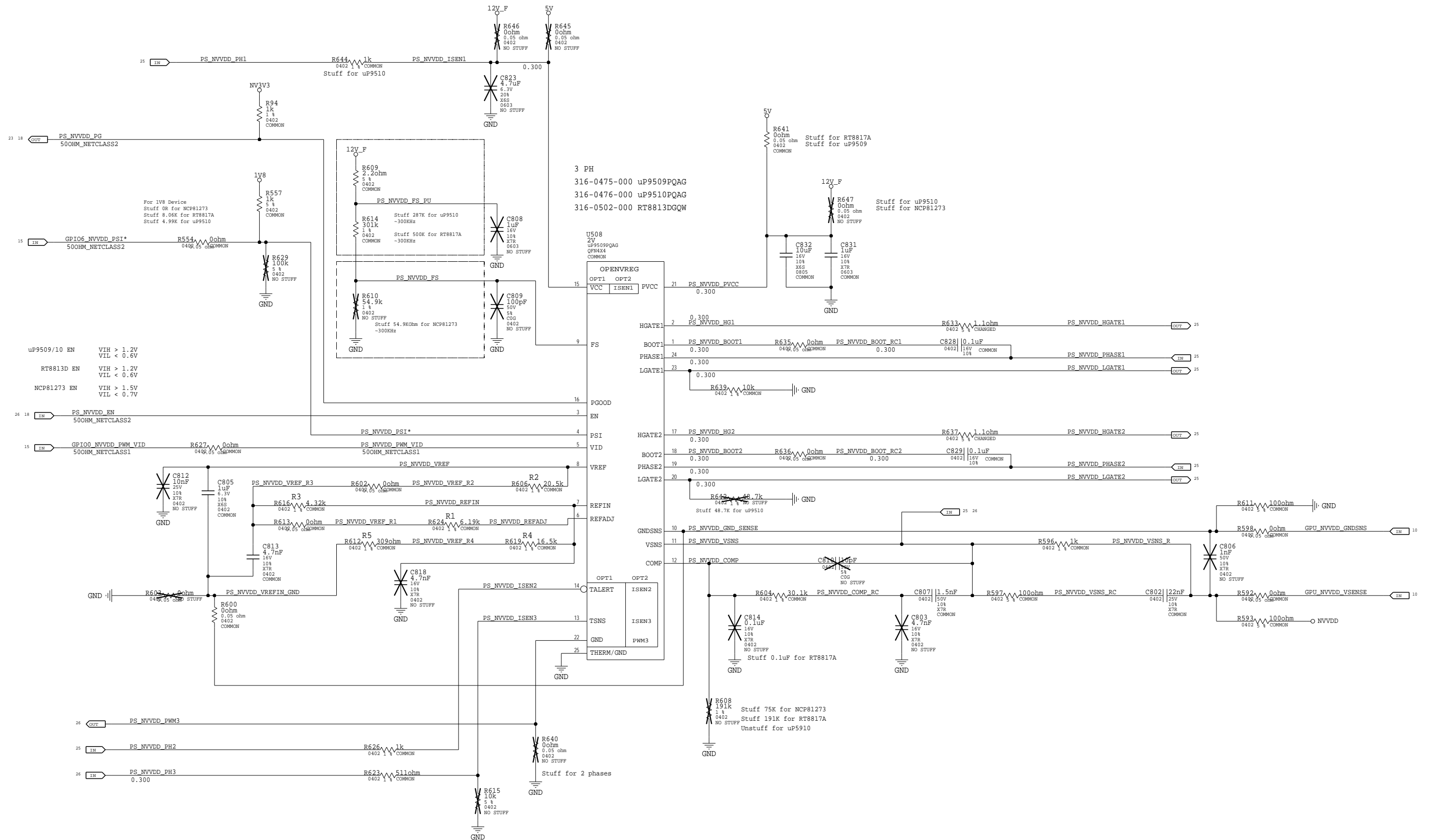


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PAGE DETAIL	PS IV: FBVDDQ

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PS V: NVVDD OVR2+1



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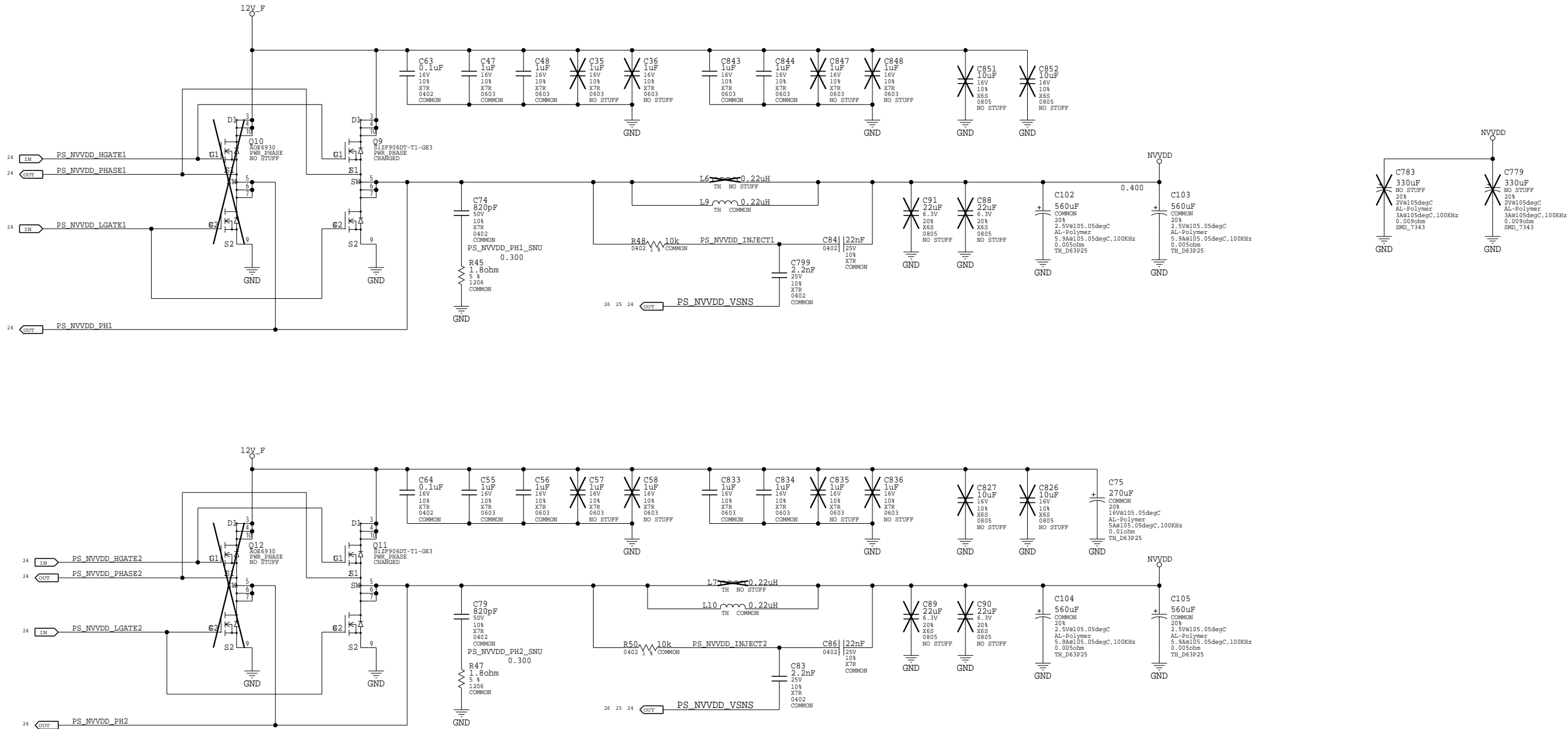
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PS V: NVVDD Phase 1,2



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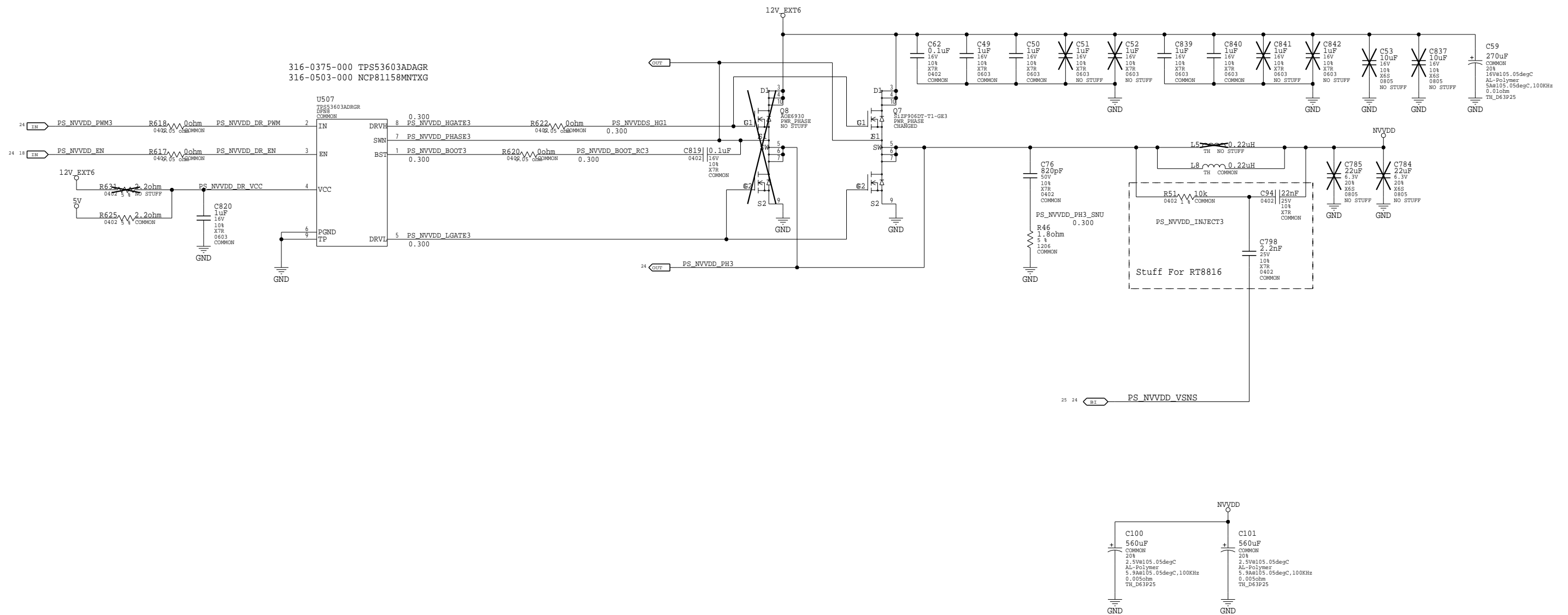
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PS V: NVVDD Phase 3

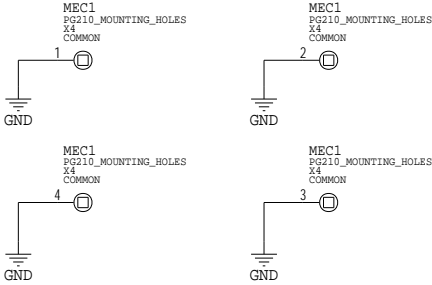
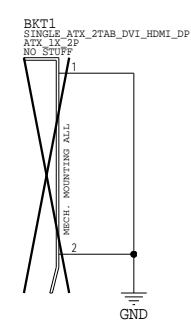


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Mechanical: Bracket/Thermal Solution

Brackets:



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