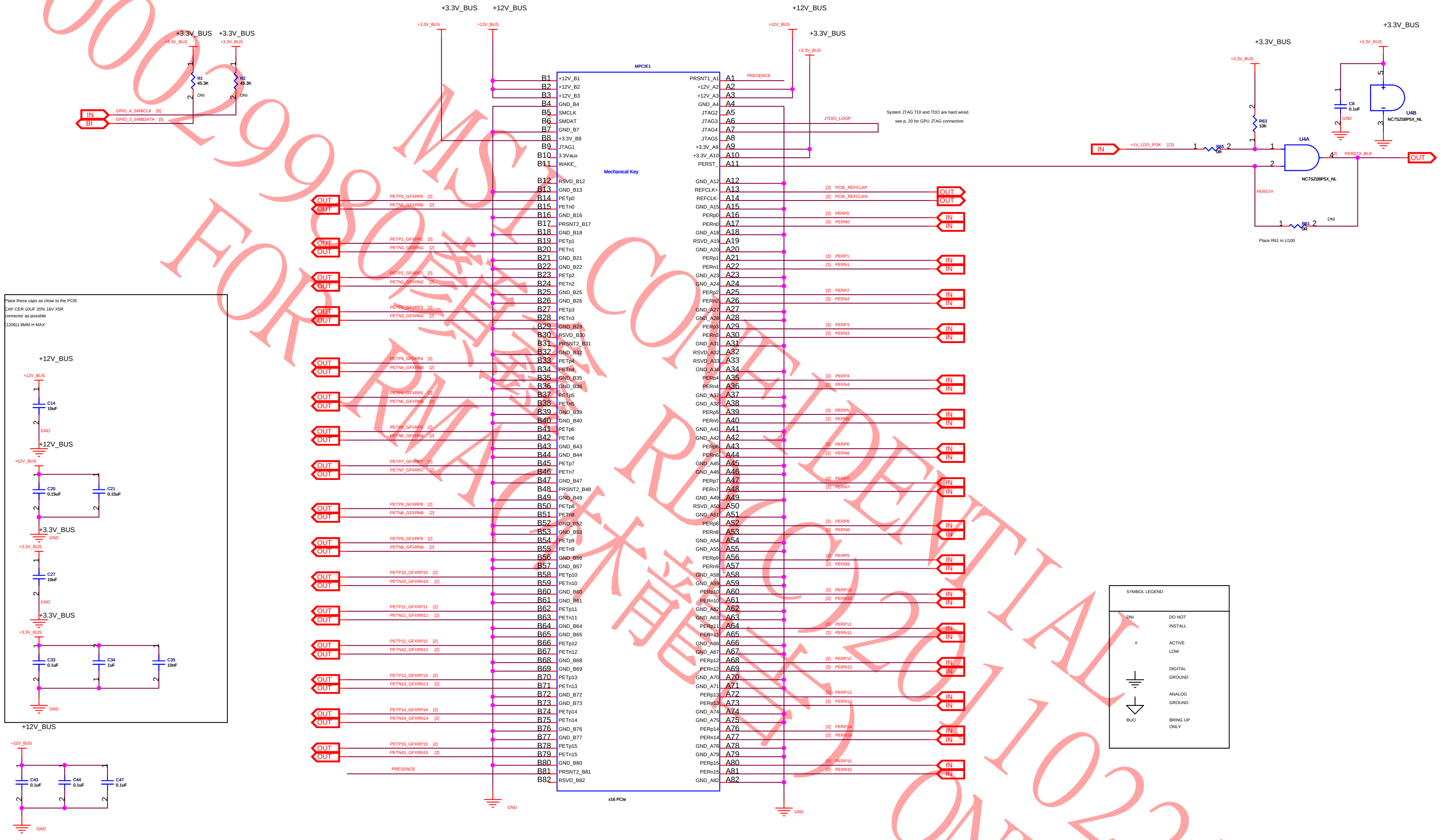
PCI-EXPRESS EDGE CONNECTOR



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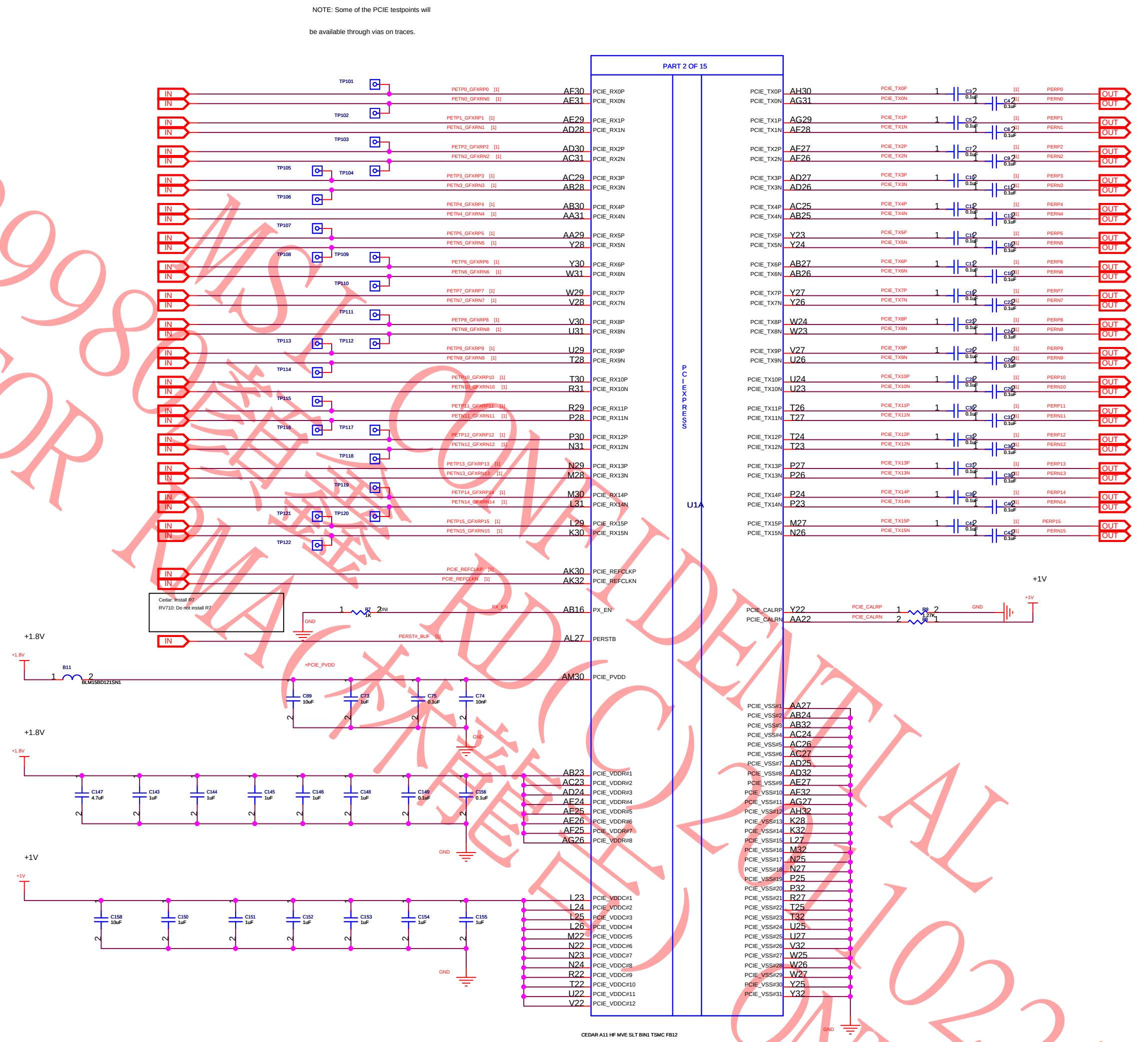
SHANGHAI CHINA 201203

Date: Thursday, September 30, 2010 | Rev P00

Title: HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA
PCI-E Edge Connector

Doc No. 105-C264XX-00A

CAICOS/CEDAR PCIe Interface



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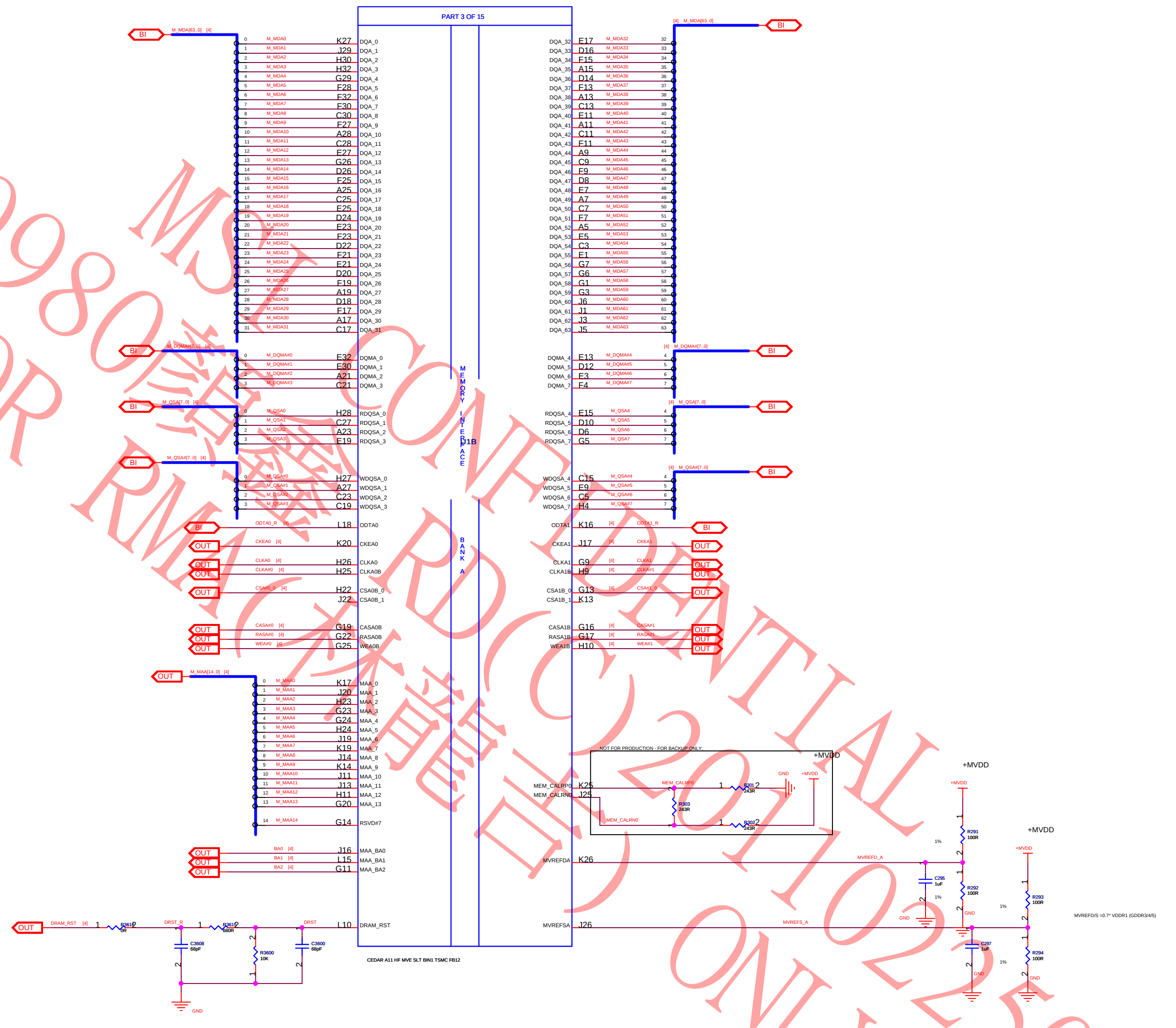
Date: Thursday, September 30, 2010	Rev P00
Sheet 2 of 18	
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA CAICOS PCIE Interface	Doc No. 105-C264XX-00A



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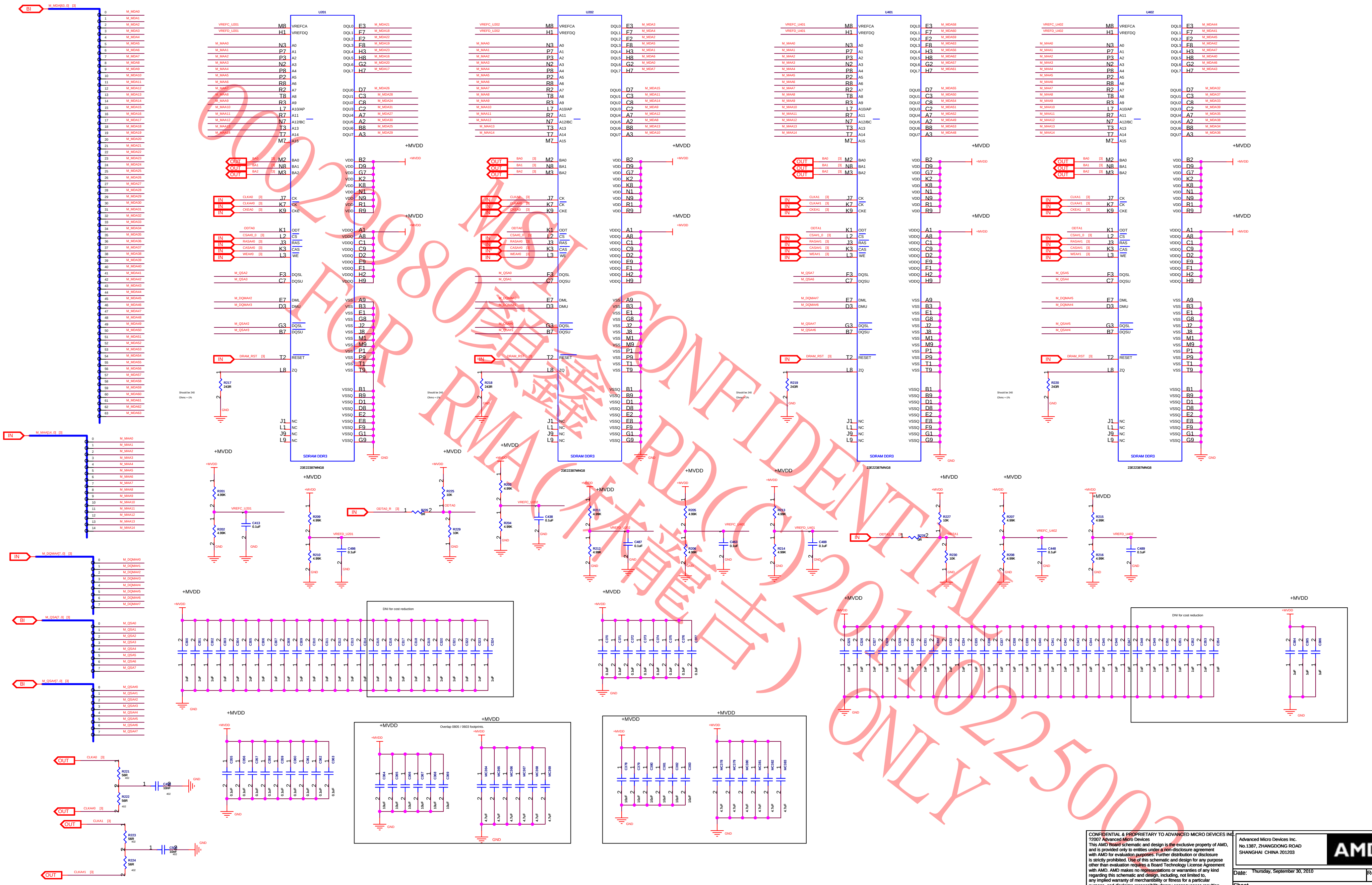
SHANGHAI CHINA 201203

Date: Thursday, September 30, 2010 | Rev P00

Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA
CAICOS MEM I/F CHA

Doc No. 105-C264XX-00A

CHANNEL A: 256MB/512MB DDR3



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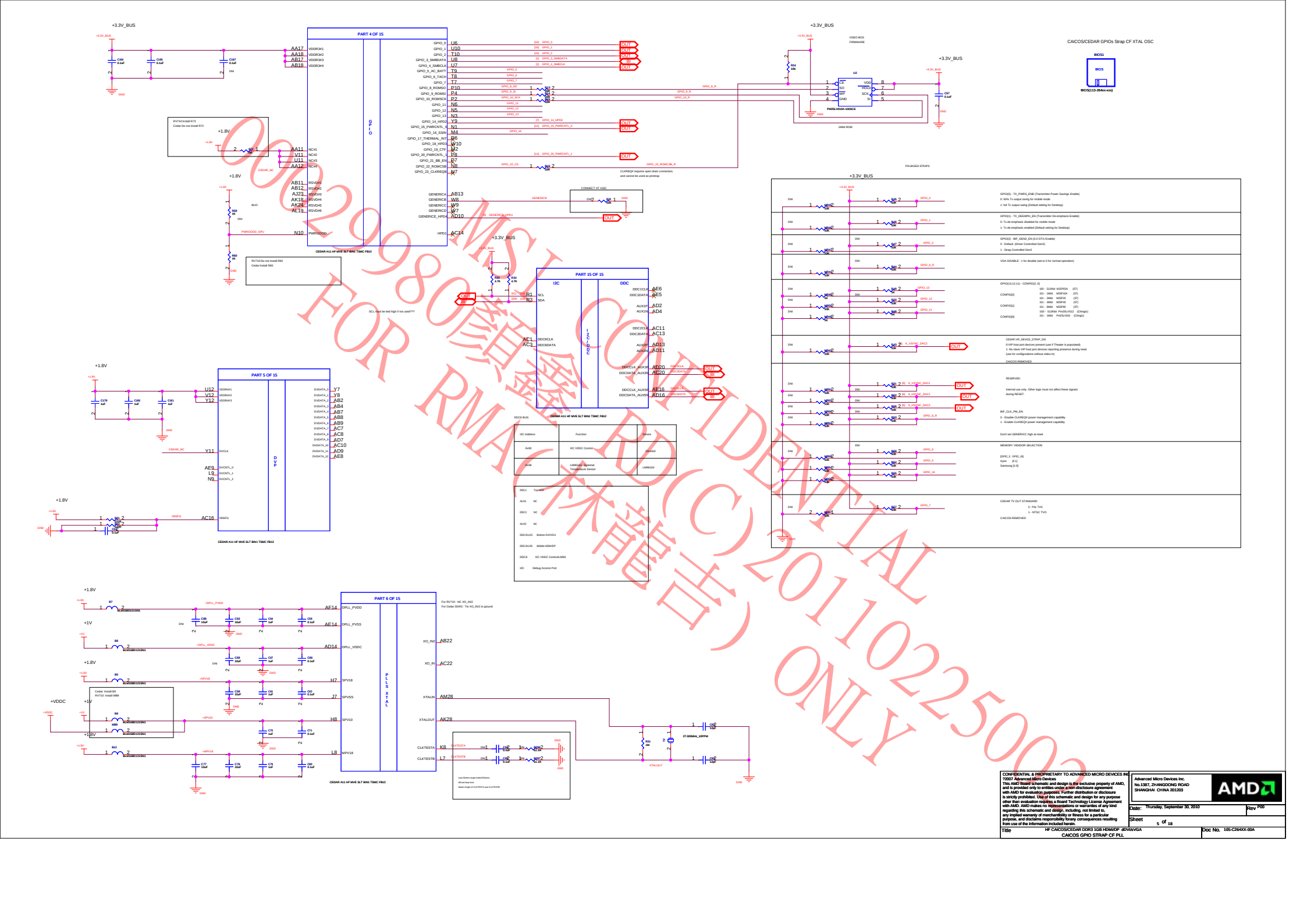
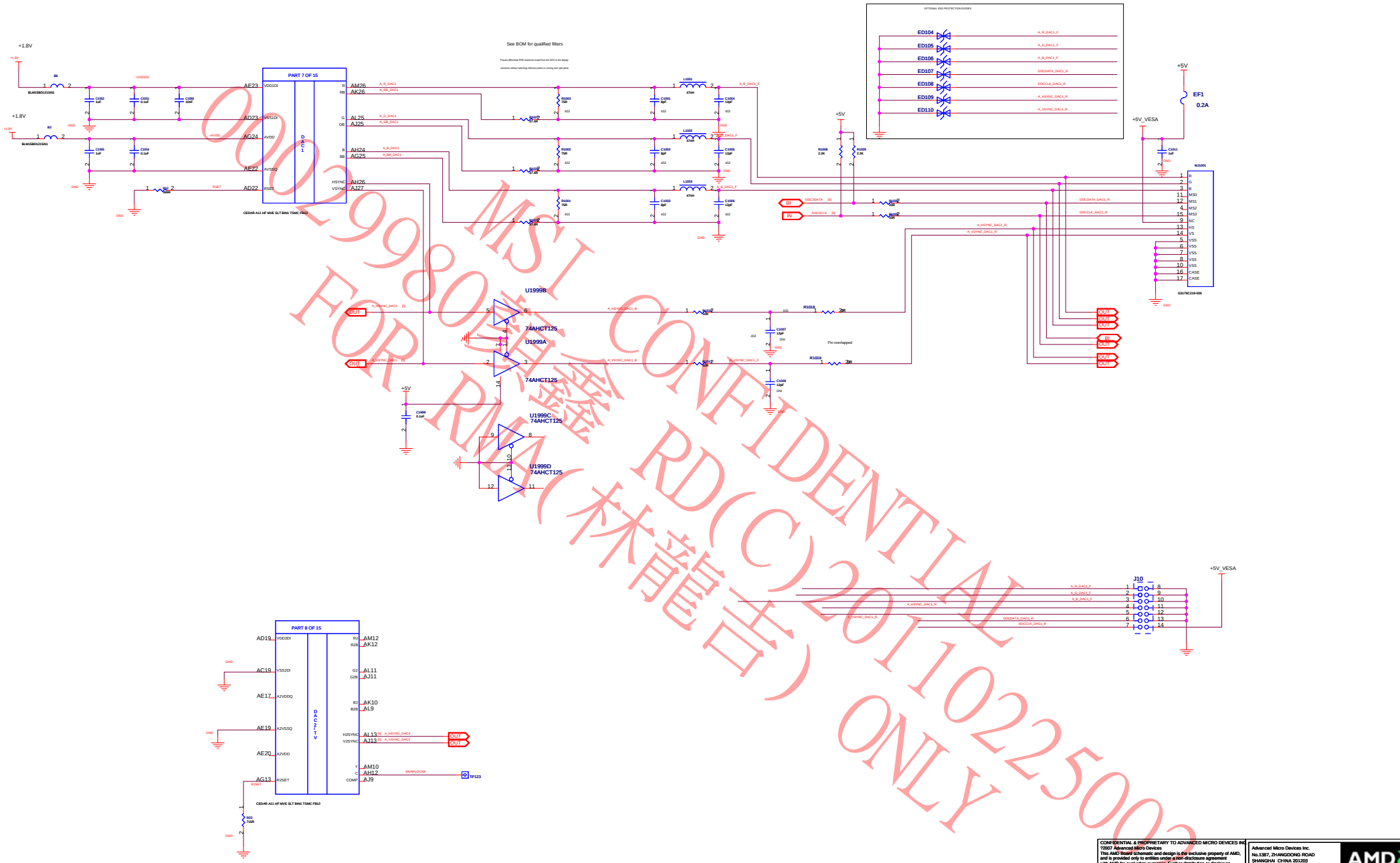
SHANGHAI CHINA 201203

Date:	Thursday, September 30, 2010	Rev	P00
Sheet	4 of 18		
Title	HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA DDR3 CHA	Doc No.	105-C264XX-00A





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Date:	Thursday, September 30, 2010
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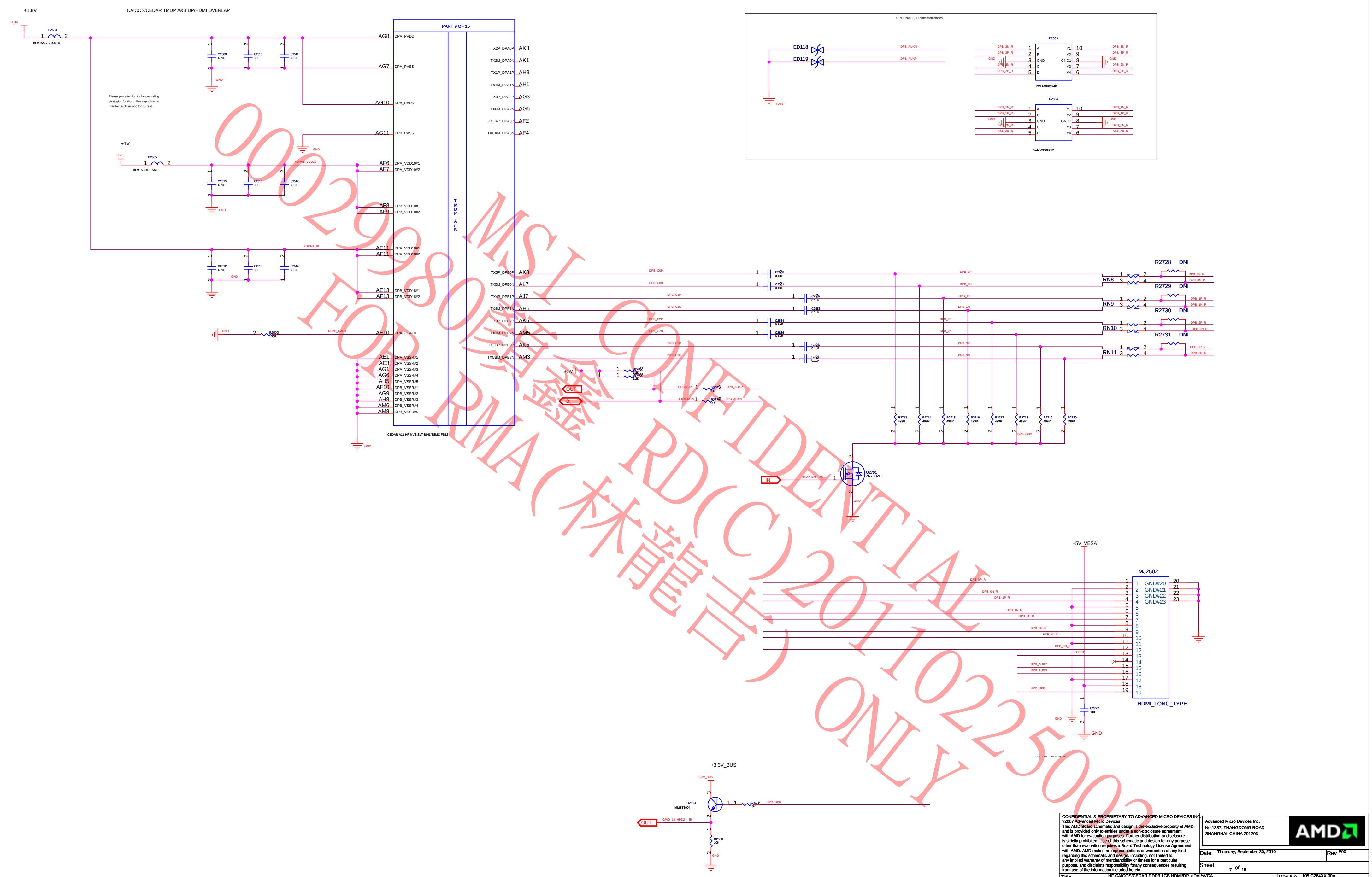
Sheet	6 of 18
Title	HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/dVGA CAICOS DAC
Doc No.	105-C26400-00A



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SHANGHAI CHINA 201203

Date: Thursday, September 30, 2010	Rev P00
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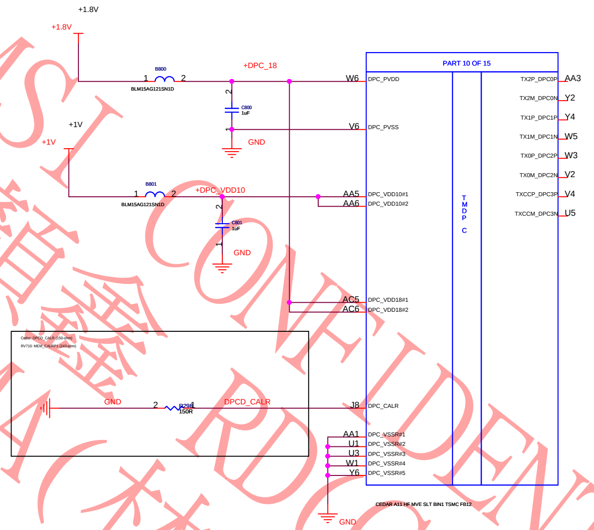
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA CAICOS TMDP A&B HDMI/DP	Doc No. 105-C264XX-00A

CAICOS/CEDAR Display Port C (Unused)



+1.8V
+1.8V
B800
1
2
BLM15AG121SN1D
+DPC_18
C800
1uF
GND
+1V
+1V
B801
BLM15AG121SN1D
+DPC_VDD10
C801
1uF
GND
Cedar: DPCD_CALR (150-ohm)
RV710: MEM_CALRP1 (243-ohm)
GND
R298
150R
DPCD_CALR
W6 DPC_PVDD
V6 DPC_PVSS
AA5 DPC_VDD10#1
AA6 DPC_VDD10#2
AC5 DPC_VDD18#1
AC6 DPC_VDD18#2
J8 DPC_CALR
AA1 DPC_VSSR#1
U1 DPC_VSSR#2
U3 DPC_VSSR#3
W1 DPC_VSSR#4
Y6 DPC_VSSR#5
GND
PART 10 OF 15
TMDP C
TX2P_DPC0P AA3
TX2M_DPC0N Y2
TX1P_DPC1P Y4
TX1M_DPC1N W5
TX0P_DPC2P W3
TX0M_DPC2N V2
TXCCP_DPC3P V4
TXCCM_DPC3N U5
CEDAR A11 HF MVE SLT BIN1 TSMC FB12

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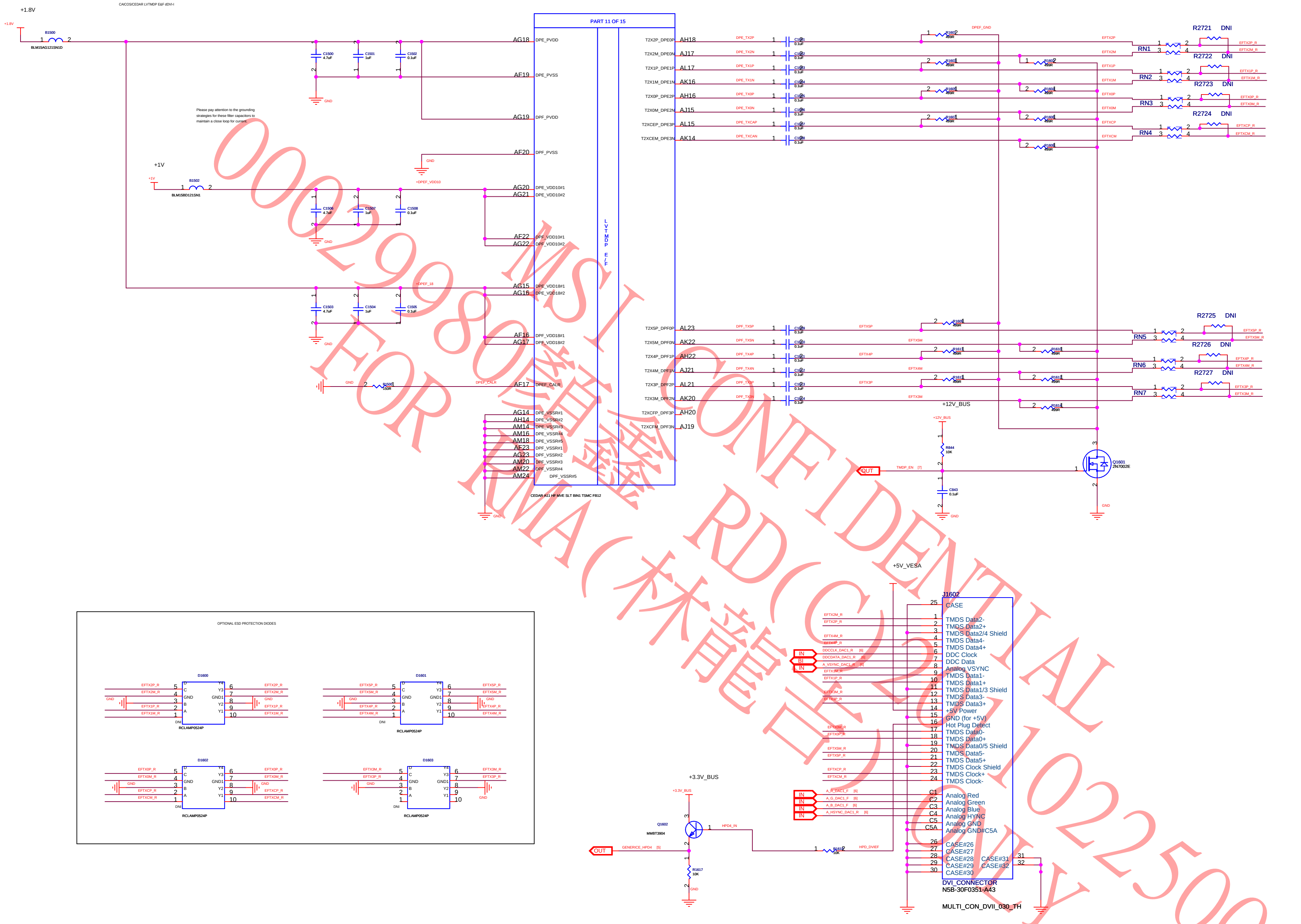
Sheet 8 of 18	
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA CAICOS TMDP C (UNUSED)	Doc No. 105-C264XX-00A


CAICOS/CEDAR LVTMDP E&F dDVI-I
+1.8V
+1V
PART 11 OF 15
LVTMDP E/F
CEDAR A11 HF MVE SLT BIN1 TSMC FB12
Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.
+12V_BUS
Q1601
2N7002E
+5V_VESA
J1602
CASE
TMDS Data2-
TMDS Data2+
TMDS Data2/4 Shield
TMDS Data4-
TMDS Data4+
DDC Clock
DDC Data
Analog VSYNC
TMDS Data1-
TMDS Data1+
TMDS Data1/3 Shield
TMDS Data3-
TMDS Data3+
+5V Power
GND (for +5V)
Hot Plug Detect
TMDS Data0-
TMDS Data0+
TMDS Data0/5 Shield
TMDS Data5-
TMDS Data5+
TMDS Clock Shield
TMDS Clock+
TMDS Clock-
Analog Red
Analog Green
Analog Blue
Analog HYNC
Analog GND
Analog GND#C5A
DVI_CONNECTOR
N5B-30F0351-A43
MULTI_CON_DVII_030_TH
+3.3V_BUS
Q1602
MMBT3904
OPTIONAL ESD PROTECTION DIODES
D1600
D1601
D1602
D1603
RCLAMP0524P

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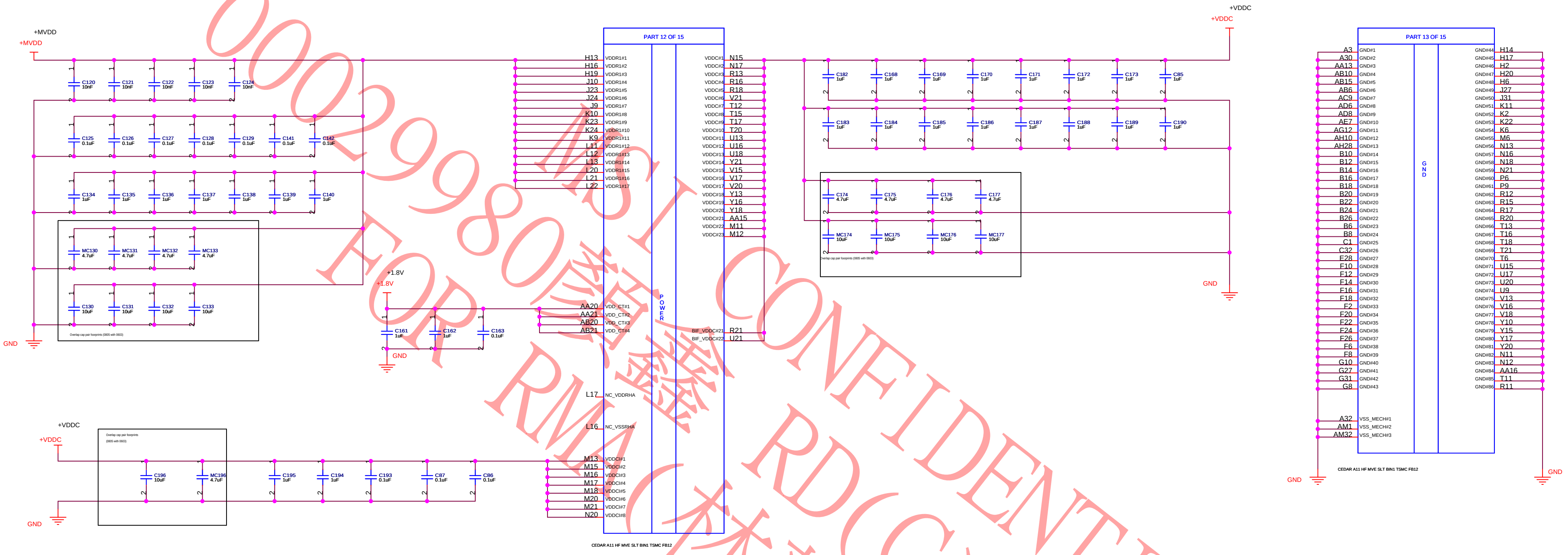
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA CAICOS LVTMDP E&F dDVI-I	Doc No. 105-C264XX-00A

CAICOS/CEDAR Power & GND



Advanced Micro Devices Inc.
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SHANGHAI CHINA 201203

AMD

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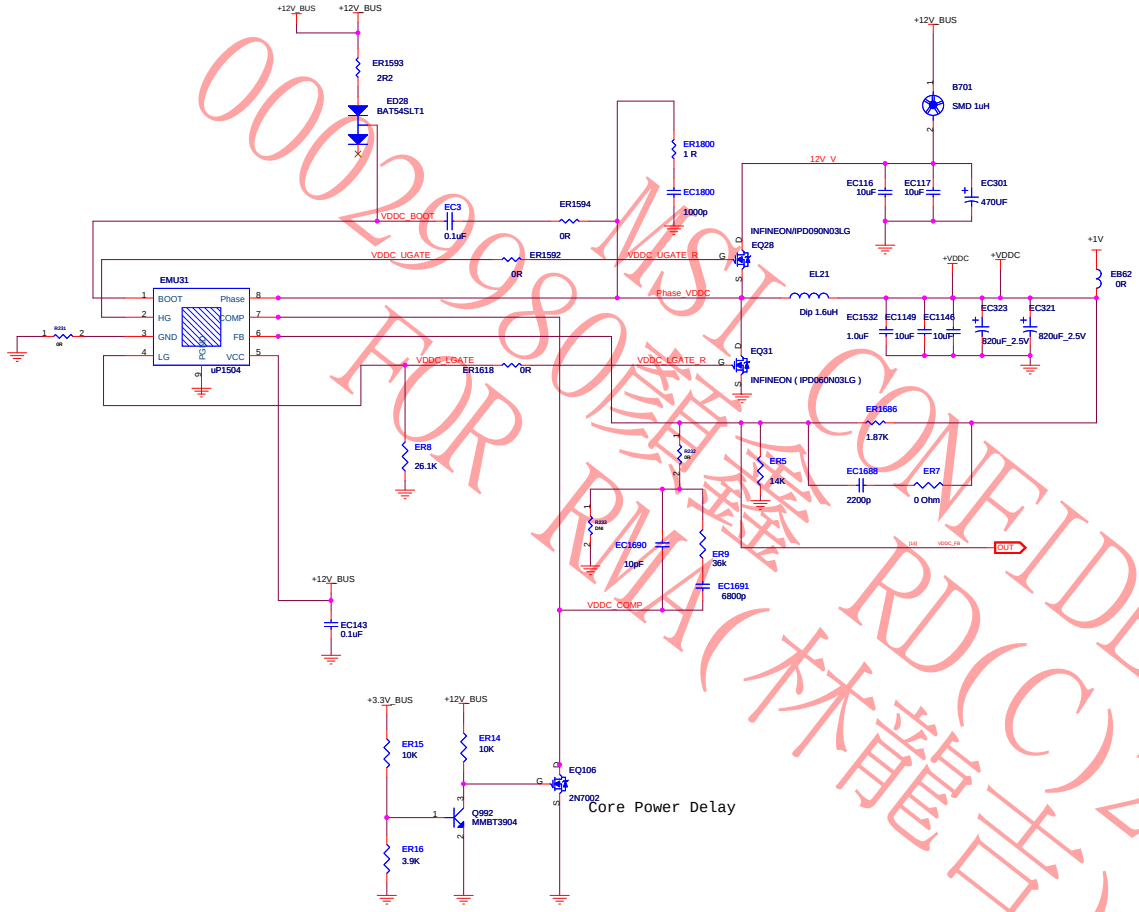
Sheet 10 of 18

Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA
CAICOS POWER&GND

Doc No. 105-C264XX-00A



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Date: Thursday, September 30, 2010	Rev P00
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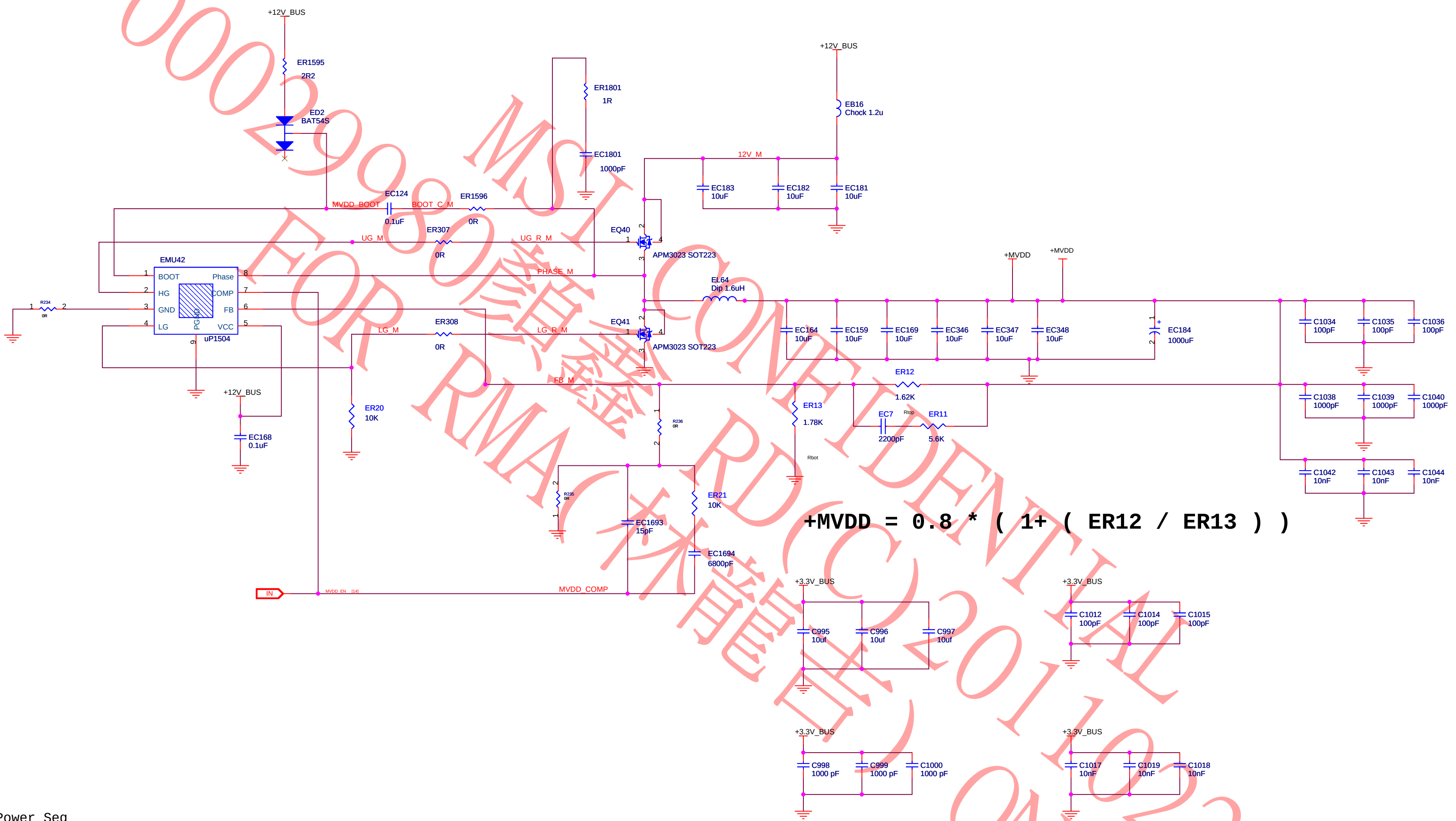
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA VDDC	Doc No. 105-C264XX-00A


+12V_BUS
ER1595
2R2
ED2
BAT54S
ER1801
1R
EC1801
1000pF
+12V_BUS
EB16
Chock 1.2u
12V_M
EC183
10uF
EC182
10uF
EC181
10uF
EC124
0.1uF
MVDD_BOOT
BOOT_C_M
ER1596
0R
ER307
0R
UG_M
UG_R_M
EQ40
APM3023 SOT223
EMU42
BOOT
Phase
HG
COMP
GND
FB
LG
VCC
uP1504
PHASE_M
R234
0R
+MVDD
+MVDD
EL64
Dip 1.6uH
EC164
10uF
EC159
10uF
EC169
10uF
EC346
10uF
EC347
10uF
EC348
10uF
EC184
1000uF
C1034
100pF
C1035
100pF
C1036
100pF
ER308
0R
LG_M
LG_R_M
EQ41
APM3023 SOT223
FB_M
ER12
1.62K
C1038
1000pF
C1039
1000pF
C1040
1000pF
+12V_BUS
ER20
10K
R236
0R
ER13
1.78K
EC7
2200pF
ER11
5.6K
Rtop
Rbot
EC168
0.1uF
C1042
10nF
C1043
10nF
C1044
10nF
R235
0R
ER21
10K
EC1693
15pF
EC1694
6800pF
IN
MVDD_EN
MVDD_COMP
+3.3V_BUS
C995
10uf
C996
10uf
C997
10uf
+3.3V_BUS
C1012
100pF
C1014
100pF
C1015
100pF
+3.3V_BUS
C998
1000 pF
C999
1000 pF
C1000
1000 pF
+3.3V_BUS
C1017
10nF
C1019
10nF
C1018
10nF

+MVDD = 0.8 * (1+ (ER12 / ER13))

Memory Power Seq

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SHANGHAI CHINA 201203

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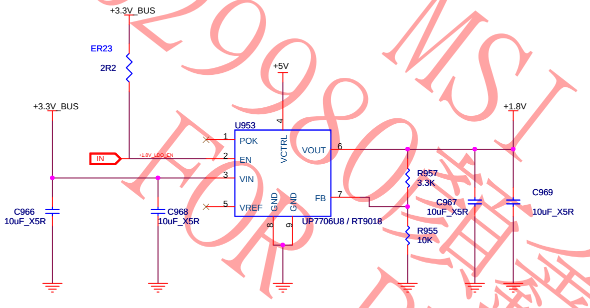
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA MVDD	Doc No. 105-C264XX-00A

Linear Regulators

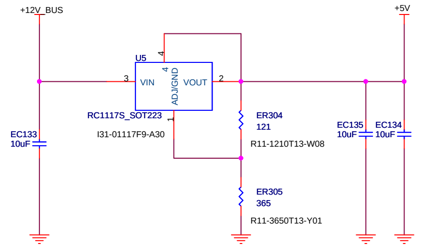
LDO #1:	Vin = 3.00V to 3.60V (3.3V +/- 9%)	Vout = +1.8V +/- 2%;	Iout = 1.6A (TBV) RMS MAX
	PCB: 50 to 70mm sq. copper area for cooling		



Vout=0.8V * (1+ R957 / R955)

1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

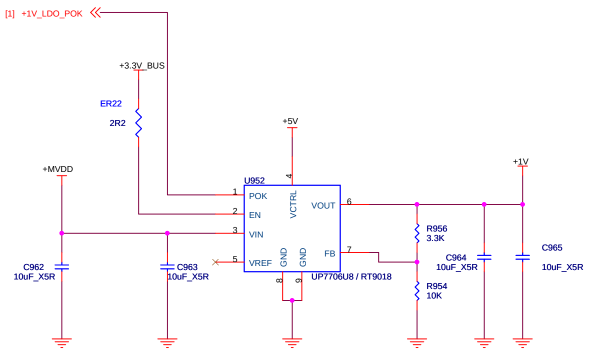
Regulators for +5V, +5V_VESA and +5V_VESA2



Vout=1.25V* [1+(ER305/ER304)]

LDO #2:	Vin = +1.32V to 1.84VMAX	Vout = +1.01V +/- 2%	Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling			

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA



Vout=0.8V * (1+ R956 / R954)

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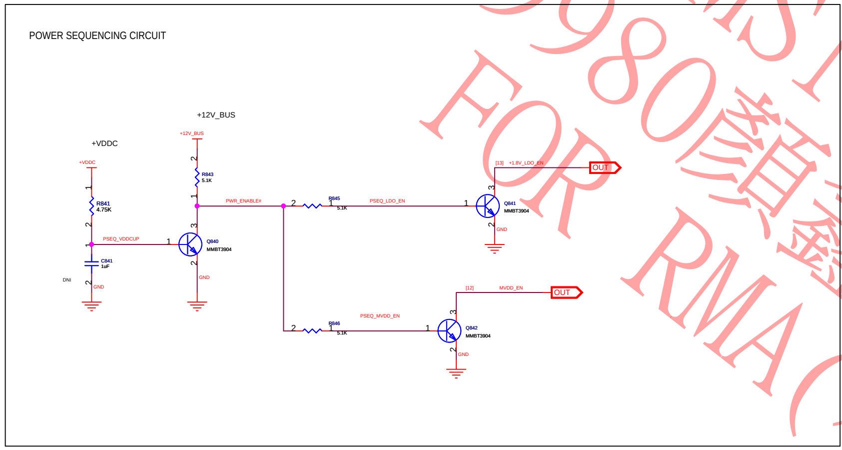

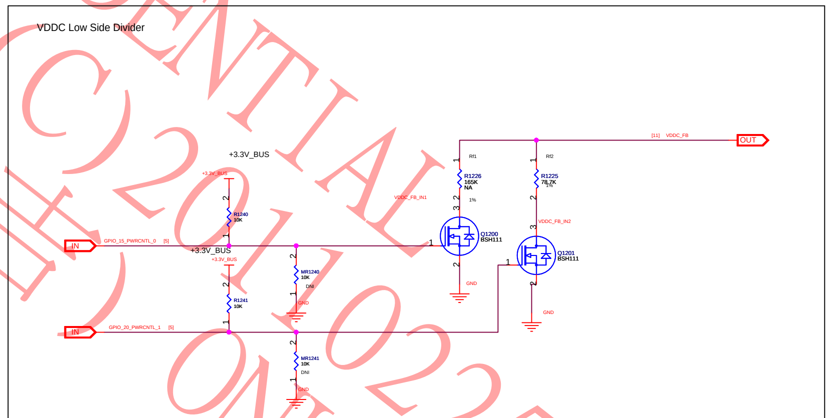

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Date: Thursday, September 30, 2010	Rev P00
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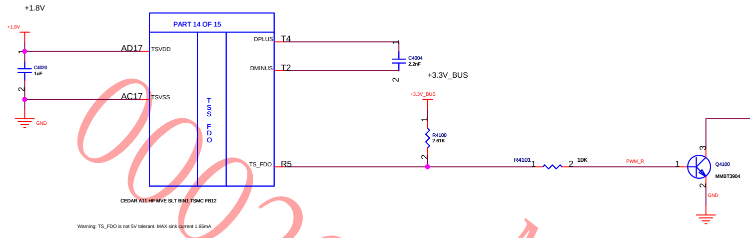
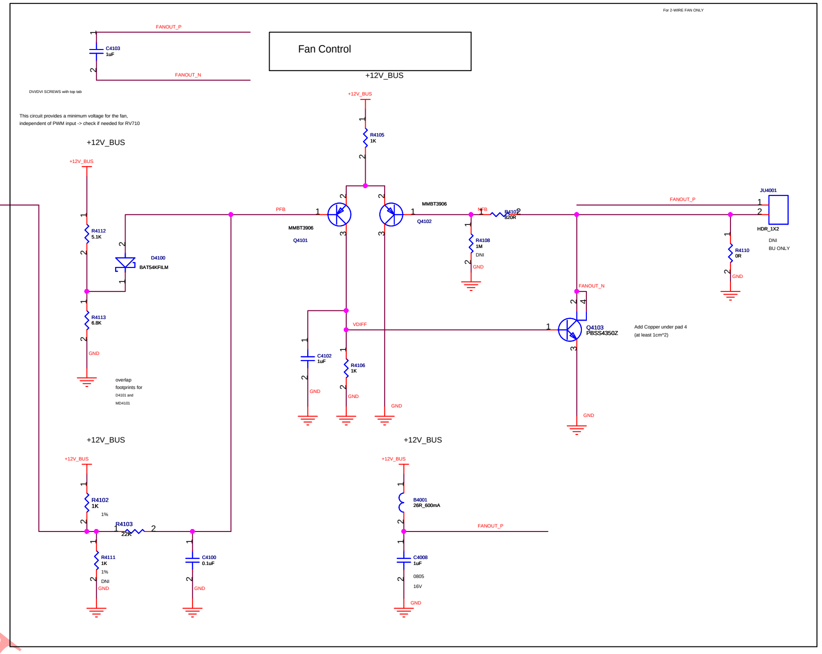
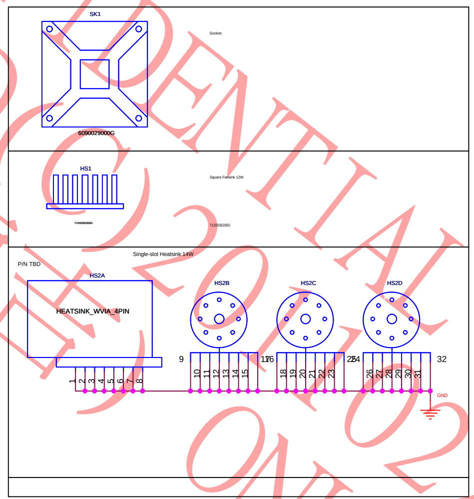
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA PWR& MGMT &SEQ	Doc No. 105-C264XX-00A

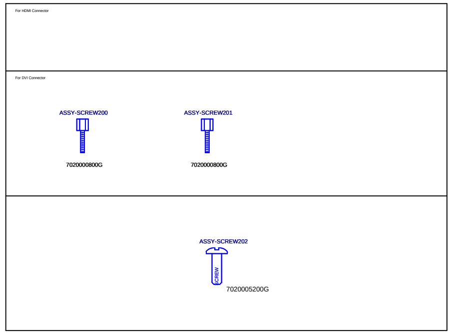
Mechanical and Thermal Management





Fan Control
+12V_BUS
FANOUT_P
FANOUT_N
C4103 1uF
This circuit provides a minimum voltage for the fan, independent of PWM input -> check if needed for RV710
R4105 1K
R4112 5.1K
R4113 6.8K
D4100 BAT54KFILM
Q4101 MMBT3906
Q4102 MMBT3906
Q4103 PBSS4350Z
C4102 1uF
R4106 1K
R4108 1M DNI
R4110 0R
JU4001 HDR_1X2
DNI BU ONLY
Add Copper under pad 4 (at least 1cm^2)
R4102 1K 1%
R4103 22K
R4111 1K 1% DNI
C4100 0.1uF
R4001 26R_600mA
C4008 1uF 0805 16V



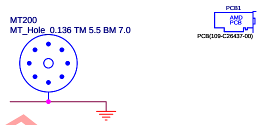


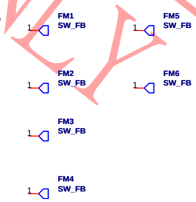

```
TOP
Single end
Address branch
50 ohm +/- 5 ohm
3.82 mils
```

```
Bottom
Single end
Memory data
45 ohm +/- 5 ohm
4.724 mils
```

```
TOP
Different
TMDS
85 ohm +/- 10 %
4.33 mils /  5.511 mils
```

```
Bottom
Different
PEX_PCIE
85 ohm +/- 10 %
4.921 mils /  6.889 mils
```





SKU	P/N	CONFIGURATION	Form Factor
JUNBONATOR	80200528A0G	dDVI-I + HDMI	FH / SS
JUNBONATOR-COMMERCIAL	8020052800G	dDVI-I + DP	FH / SS
JUNBONATOR-COMMERCIAL	8020051600G	DVI + DP	LP / SS
JUNBONATOR	80200516A0G	DVI +HDMI	LP / SS
	8020051700G	DVI + DP + VGA	FH / DS
	80200517A0G	DVI +HDMI+ VGA	FH / DS

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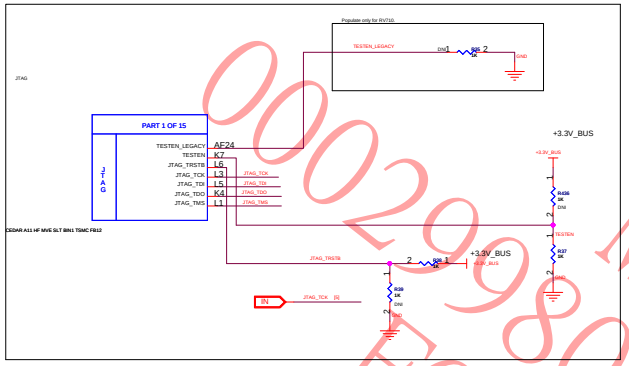
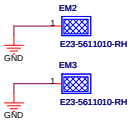
Date: Thursday, October 21, 2010 | Rev P00

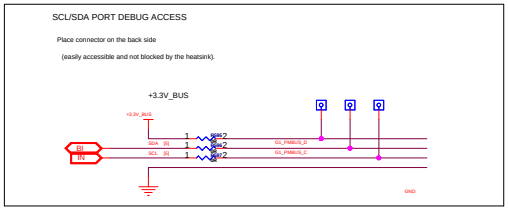
Title: HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA
MECH/THERMAL MANAGEMENT

Doc No. 105-C264XX-00A

(19) Debug Circuits







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No.1387, ZHANGDONG ROAD
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Date: Thursday, September 30, 2010 Rev P00

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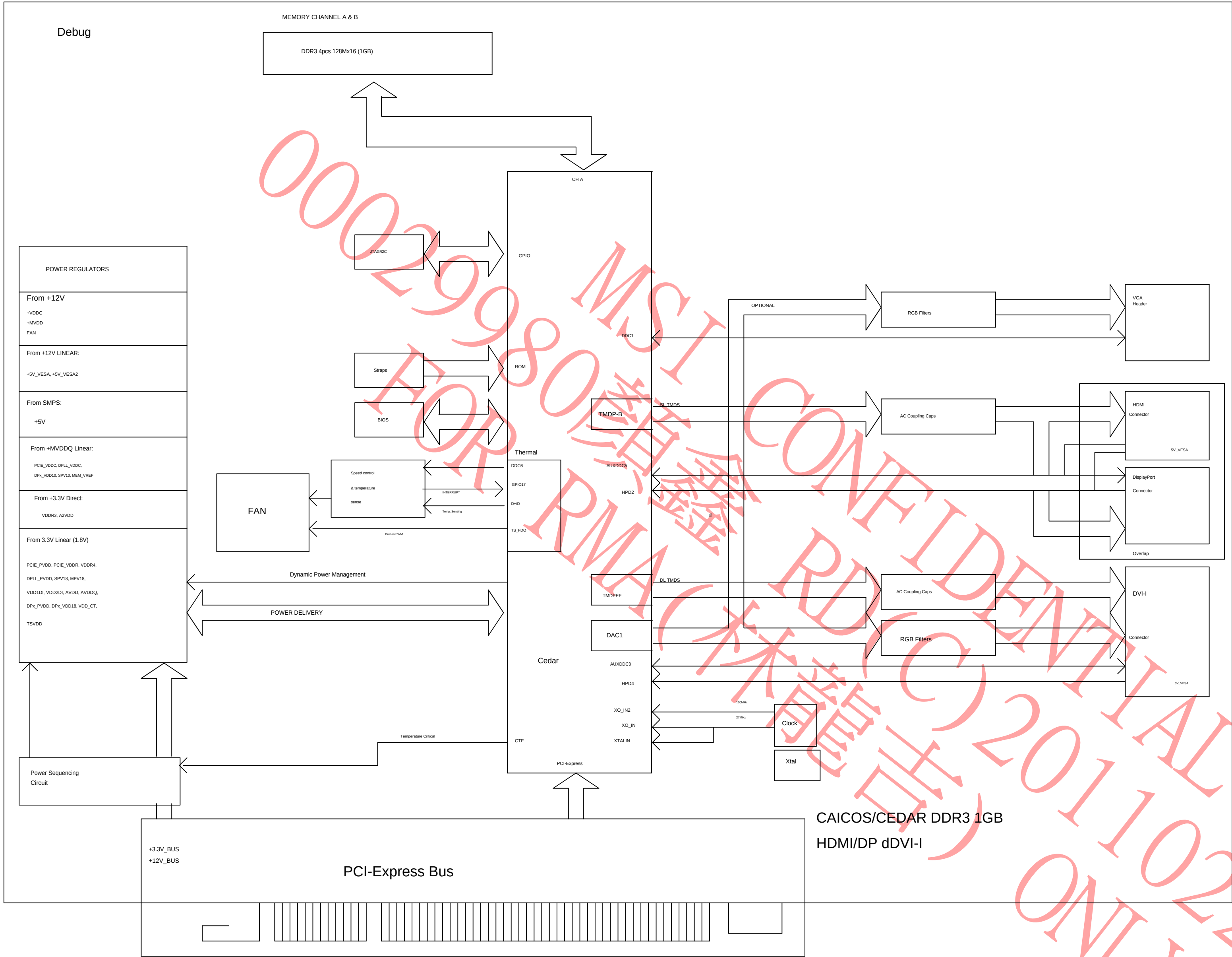
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA DEBUG CIRCUIT

Doc No. 105-C26400-00A


Debug
MEMORY CHANNEL A & B
DDR3 4pcs 128Mx16 (1GB)
CH A
GPIO
ROM
Straps
BIOS
TMDP-B
DL TMDS
Thermal
DDC6
GPIO17
D+/D-
TS_FDO
AUXDDC5
HPD2
DDC1
OPTIONAL
RGB Filters
VGA
Header
AC Coupling Caps
HDMI
Connector
5V_VESA
DisplayPort
Connector
Overlap
DVI-I
Connector
TMDPEF
DAC1
AUXDDC3
HPD4
XO_IN2
XO_IN
XTALIN
CTF
PCI-Express
Cedar
Clock
Xtal
100MHz
27MHz
Speed control
& temperature
sense
INTERRUPT
Temp. Sensing
Built-in PWM
FAN
POWER REGULATORS
From +12V
+VDDC
+MVDD
FAN
From +12V LINEAR:
+5V_VESA, +5V_VESA2
From SMPS:
+5V
From +MVDDQ Linear:
PCIE_VDDC, DPLL_VDDC,
DPx_VDD10, SPV10, MEM_VREF
From +3.3V Direct:
VDDR3, A2VDD
From 3.3V Linear (1.8V)
PCIE_PVDD, PCIE_VDDR, VDDR4,
DPLL_PVDD, SPV18, MPV18,
VDD1DI, VDD2DI, AVDD, AVDDQ,
DPx_PVDD, DPx_VDD18, VDD_CT,
TSVDD
Dynamic Power Management
POWER DELIVERY
Temperature Critical
Power Sequencing
Circuit
+3.3V_BUS
+12V_BUS
PCI-Express Bus

CAICOS/CEDAR DDR3 1GB
HDMI/DP dDVI-I

Advanced Micro Devices Inc.
No.1387, ZHANGDONG ROAD
SHANGHAI CHINA 201203

Date: Thursday, September 30, 2010 | Rev P00
Sheet 17 of 18
Title HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA BLOCK DIAGRAM | Doc No. 105-C264XX-00A

	Title	Schematic No.	Date:
AMD	HF CAICOS/CEDAR DDR3 1GB HDMI/DP dDVI/sVGA	105-C264XX-00A	Thursday, September 30, 2010

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev P00

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2010/03/31	Initial Caicos Schematic, based on C026XX-10
			.....