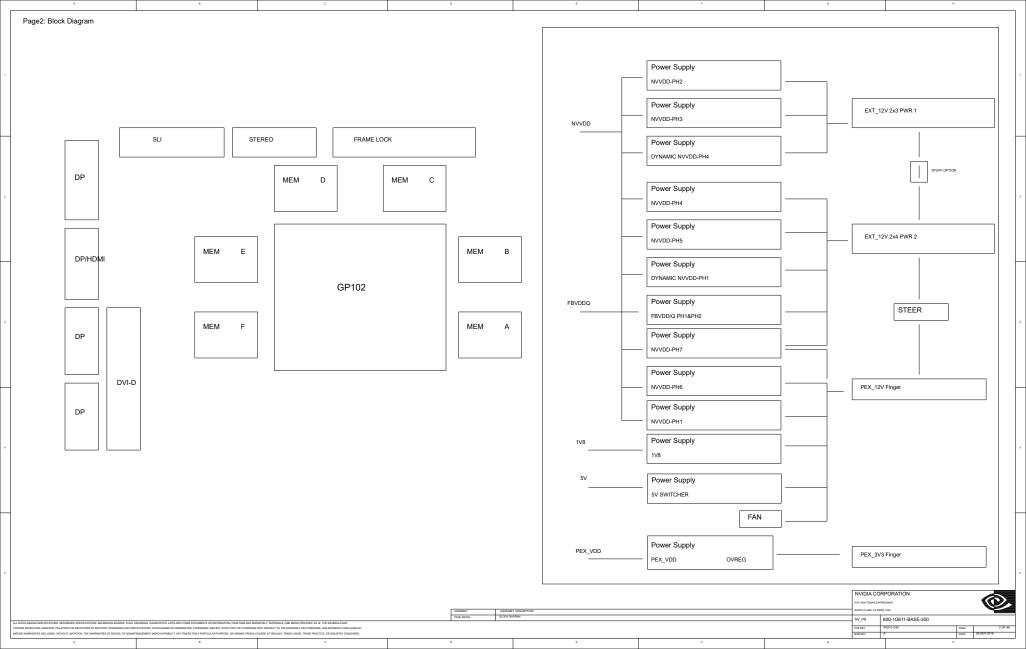
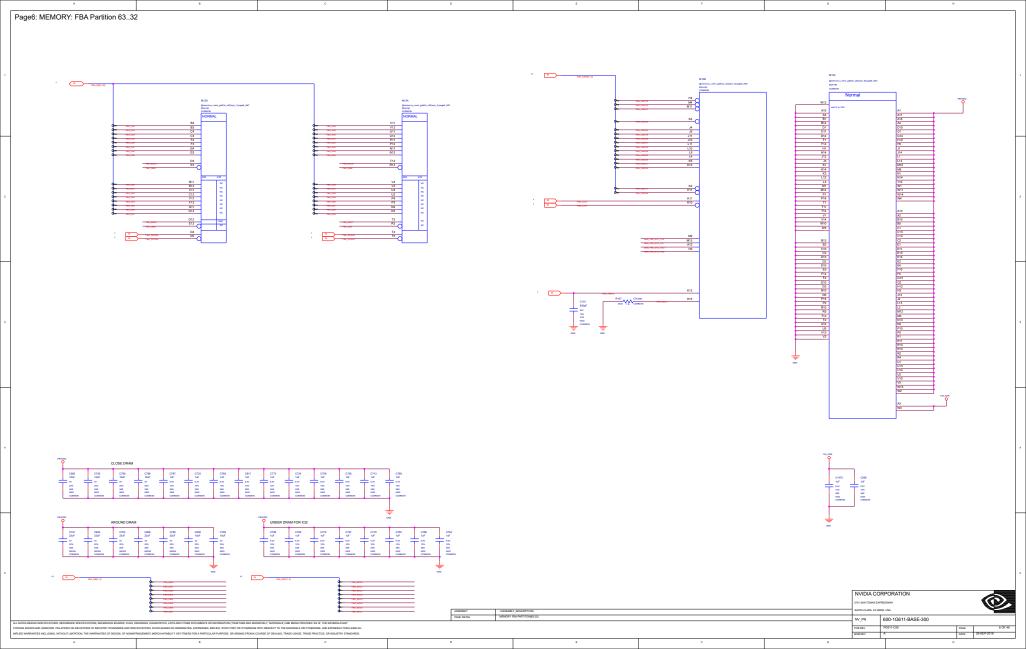
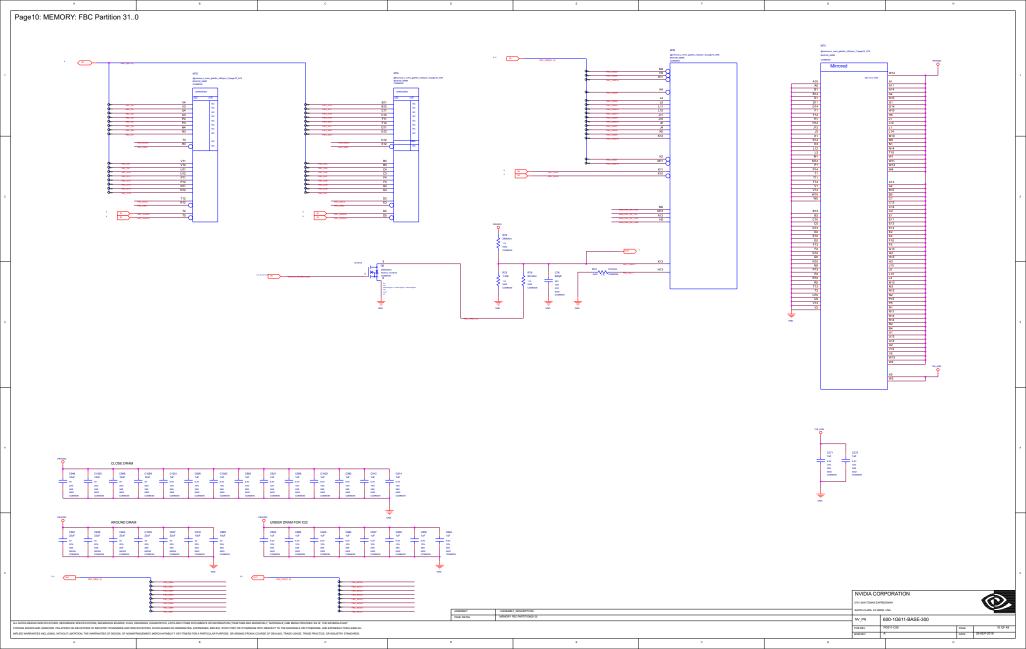
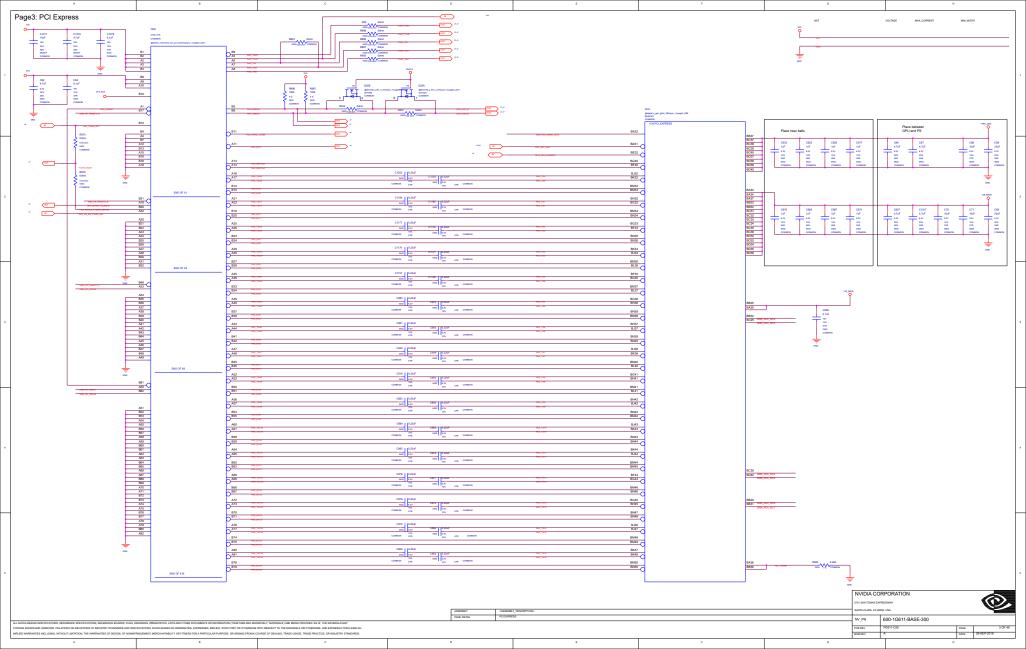
PG611 C00												
12GB GDDR5X, 384b, 256Mx32												
TALL DVI-D + DP + DP + HDMI/DP + DP												
TABLE OF C	CONTENTS											
Page	Description			Page	Description							
1	Table of Contents			26	MIOA/B INTERFACE & FRAME LOCK					-		
2	BLOCK DIAGRAM			27	MISC: FAN, THERMAL, JTAG, GPIO, STEREO							
3	PCI EXPRESS			28	MISC: ROM, STRAPS							
4	MEMORY: GPU PARTITION A/B			29	MISC: XTAL, PLL							
5	MEMORY: FBA PARTITION[31:0]			30	PS: 5V, PEXVDD							
6	MEMORY: FBA PARTITION[63:32]			31	PS: 1V8 Rails					2		
7	MEMORY: FBB PARTITION[31:0]			32	PS: FBVDDQ							
8	MEMORY: FBB PARTITION[63:31]			33	PS: NVVDD Controller_OVR8							
9	MEMORY: GPU PARTITION C/D			34	PS: NVVDD Controller_PWR-MODULE							
10	MEMORY: FBC PARTITION[31:0]			35	PS: NVVDD Phase 1, 2							
11				36	PS: NVVDD Phase 3, 4							
12				37	PS: NVVDD Phase 5							
13				38	PS: NVVDD Phase 6, 7							
14				39	PS: Dynamic power balance phase							
15				40	PS: Dynamic power balance logic					3		
16				41	PS: Input, filtering, and Monitoring							
17				42	PS: Current Sterring, Hot Unplug PS: NVVDD ENABLE							
18				43	PS: NVVDD ENABLE PS: GC6 MISC							
19				44 45	PS: GC6 MISC GEFORCE LED AND SLI LED							
20				45	PS: NV3V3, NV12V							
22				47	PS: MCU							
23				48	MECH							
24				49	VR Thermal Protection							
25												
										4		
										5		
								NVIDIA COF				
			ASSEMBLY	*ASSEMBLY_DESCRIPTION*				SANTA CLARA, CA 9505	Q, USA			
LL NYON DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE SO	RDS, FLES, CRAWNIGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND S RDS AND SPECIFICATIONS. INVIOLATIANCES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTIORY OR OTHERWI	SEPARATELY, MATERIALS) ARE BEING PROVIDED 'AS IS: THE MATERIALS MAY	PAGE DETAL	Table of Contents				NV_PN	600-1G611-BASE-300	Touce 1 10F49		
IPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESK	N, OF NONNFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM	AA COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.						BOM REV	A	DATE 28-SEP-2016		
A	0	c c	0		F	1	G		1 "	1		

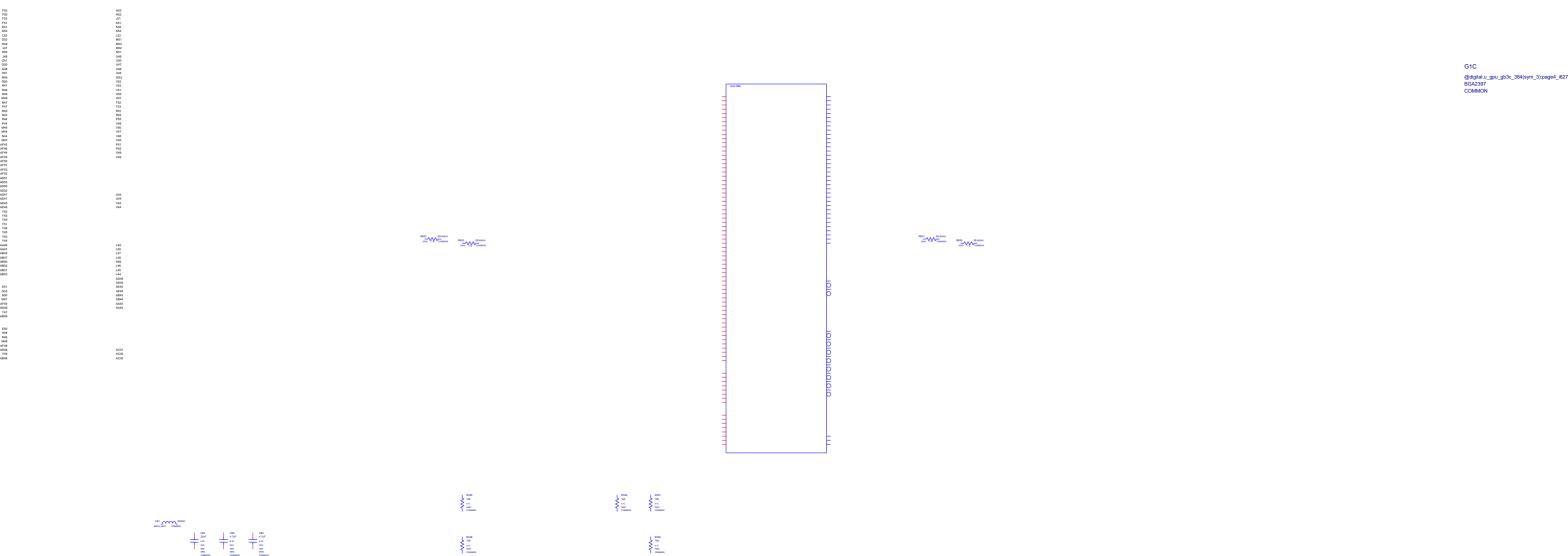


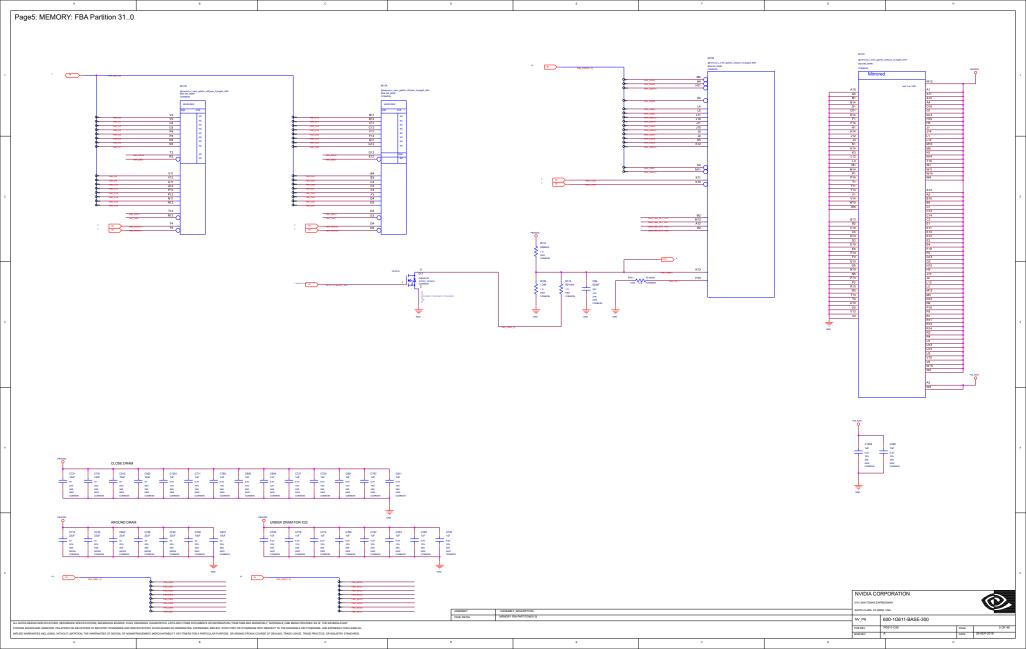


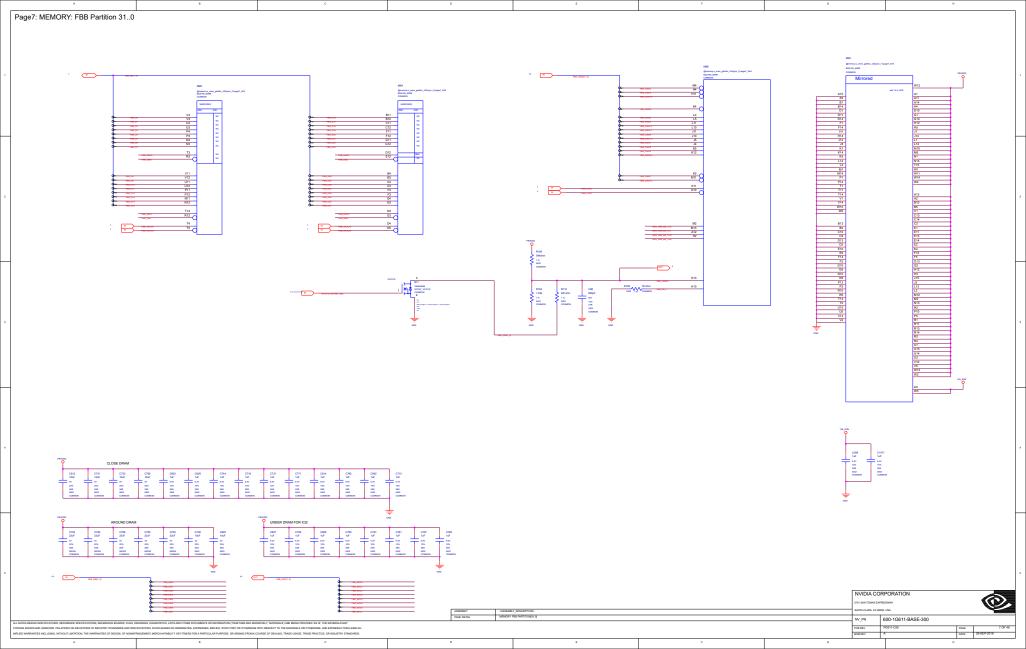


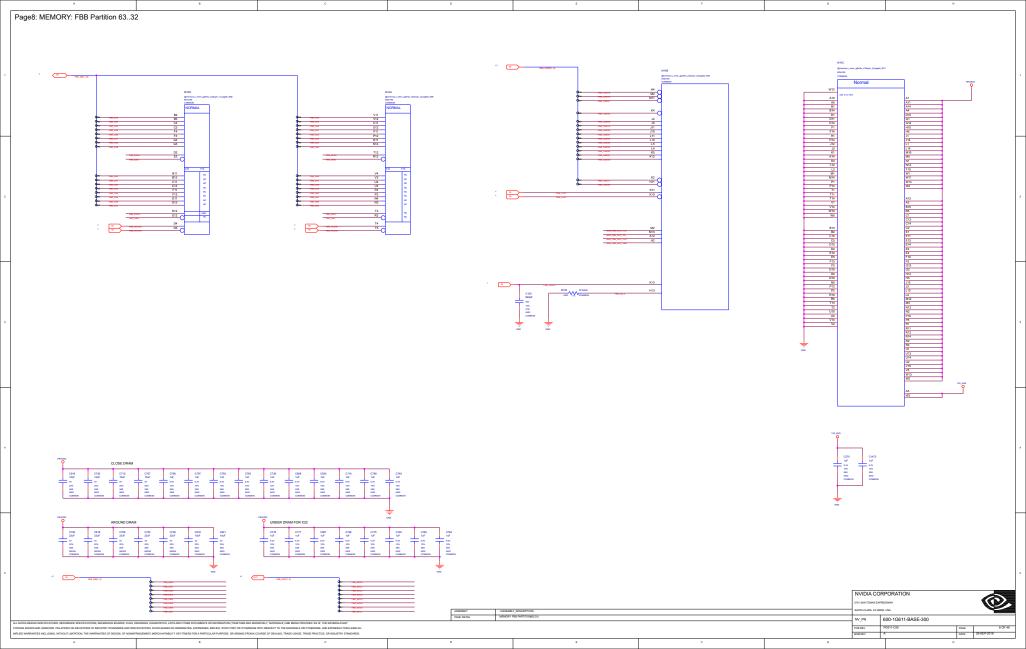
AB III II I	SATE SATE		G1E @digital.u_gpu_gb3c_384(eym_5):page9_i602 COMMON
807 CO C			Common
67 807 108 808 811 201			
60 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			
123 1623 1623		OI	
		E	

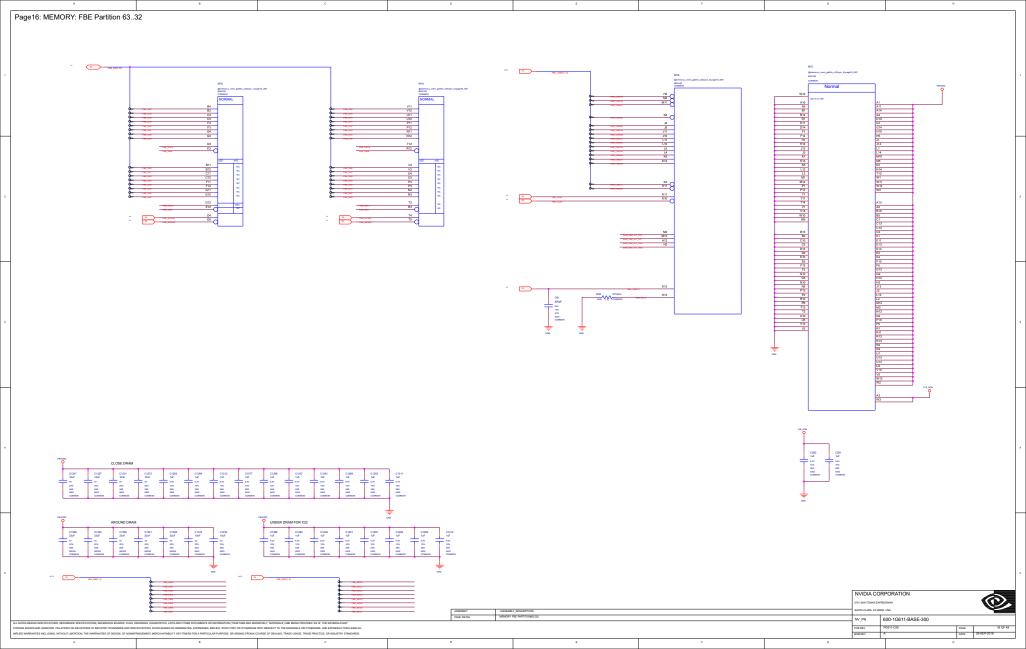


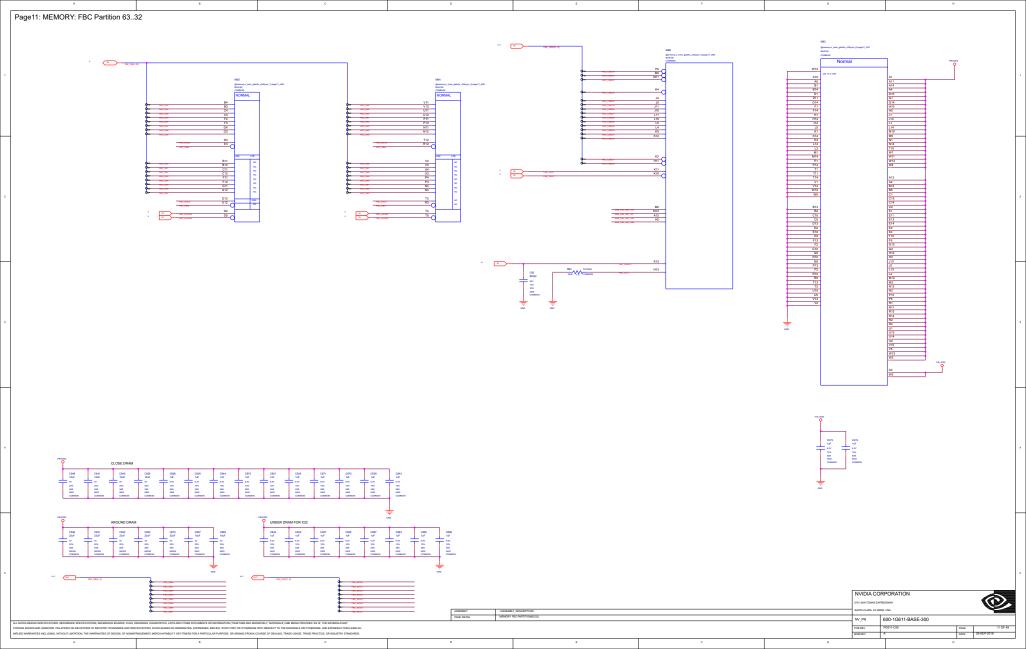


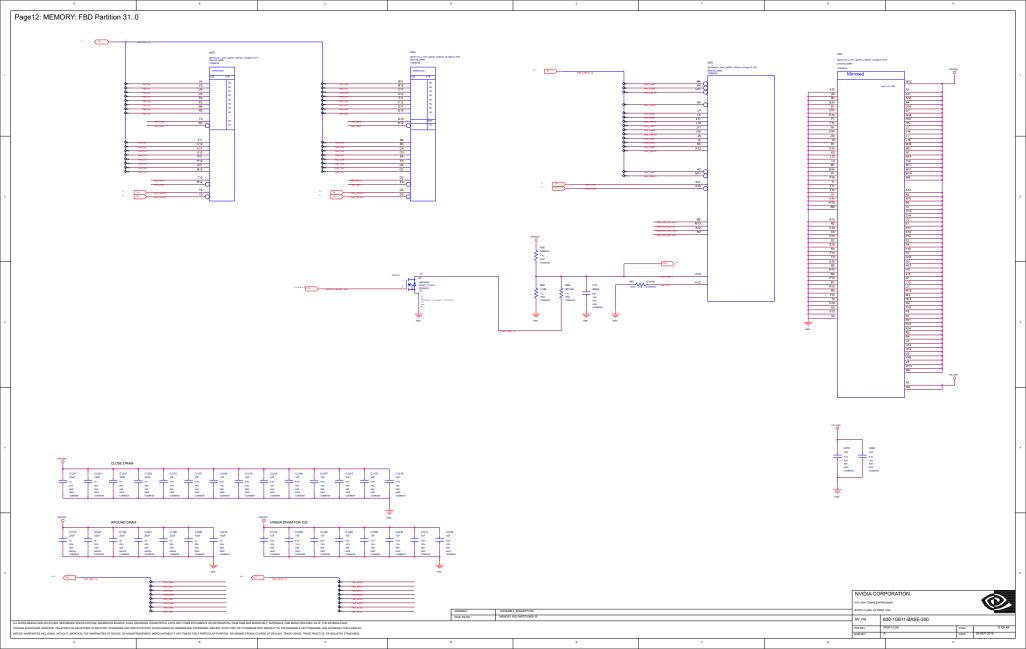


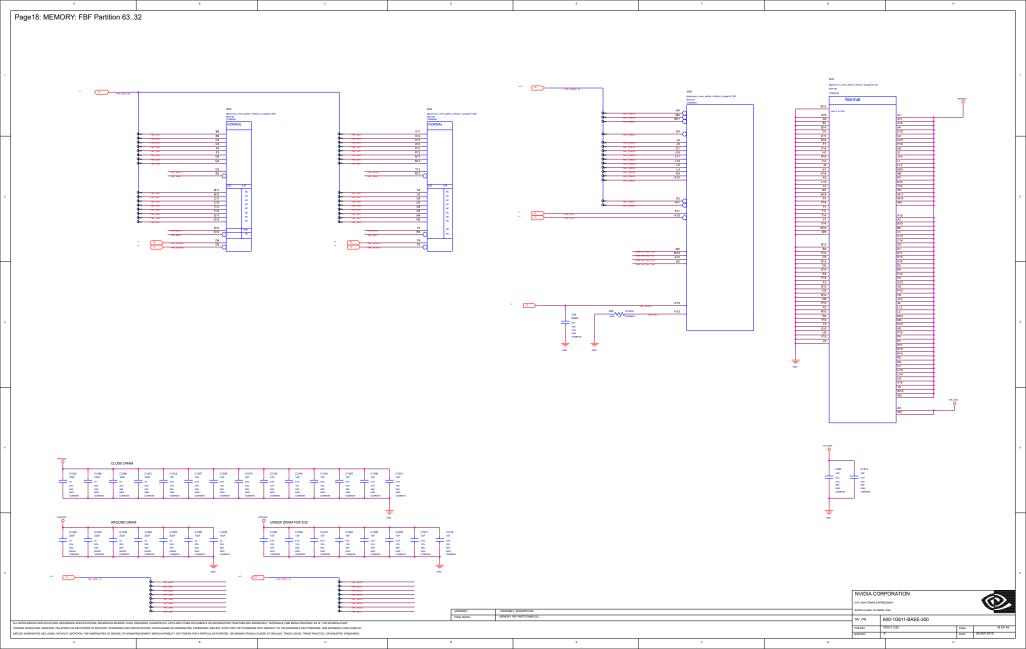


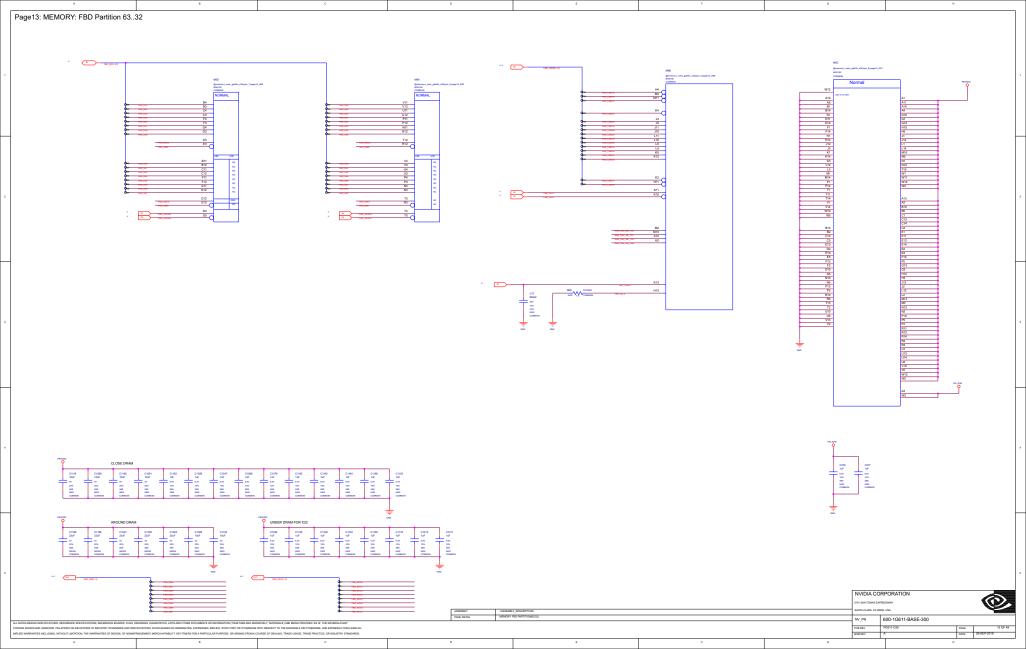


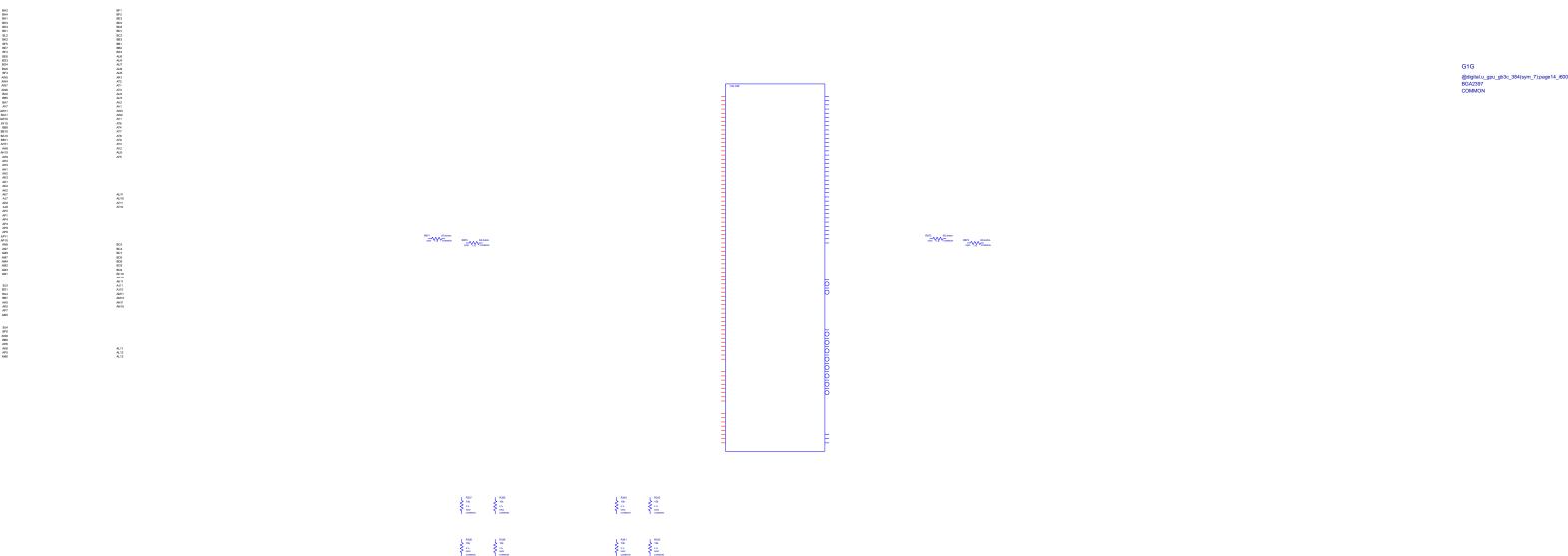


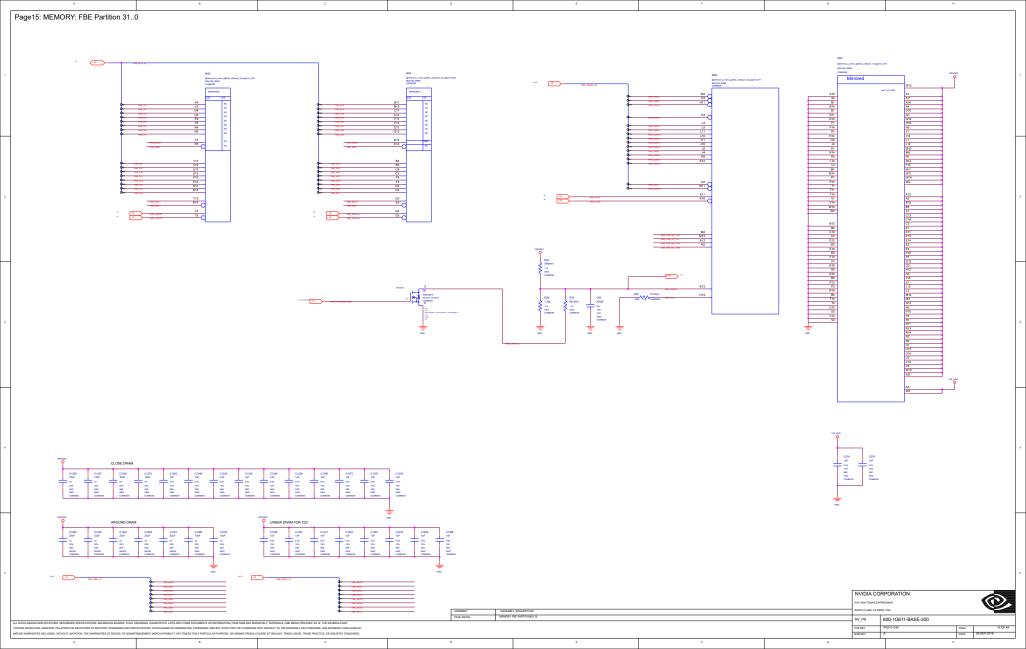


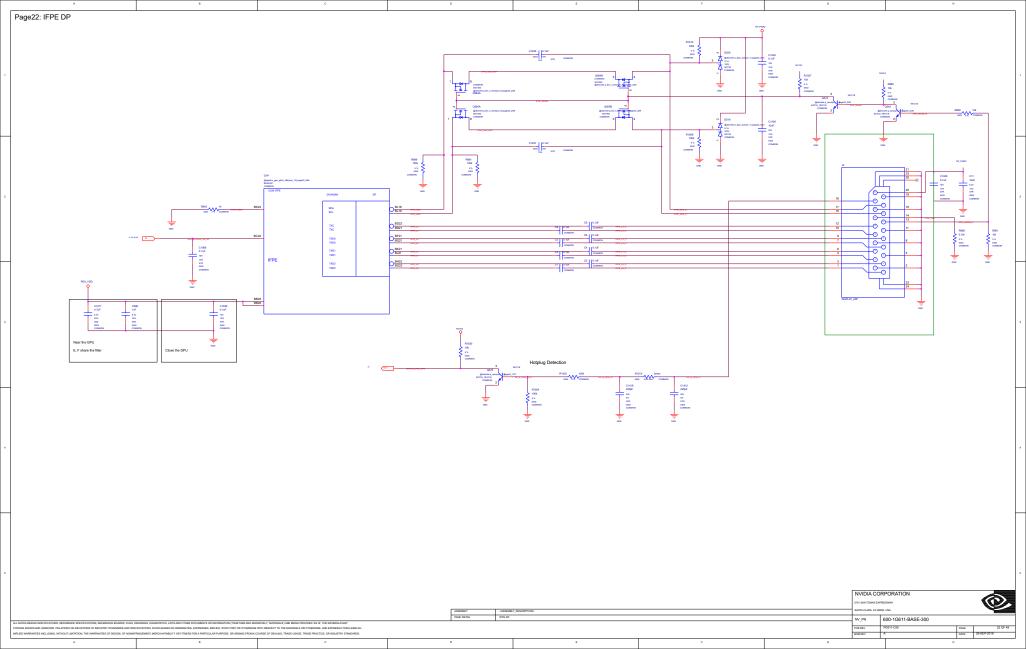


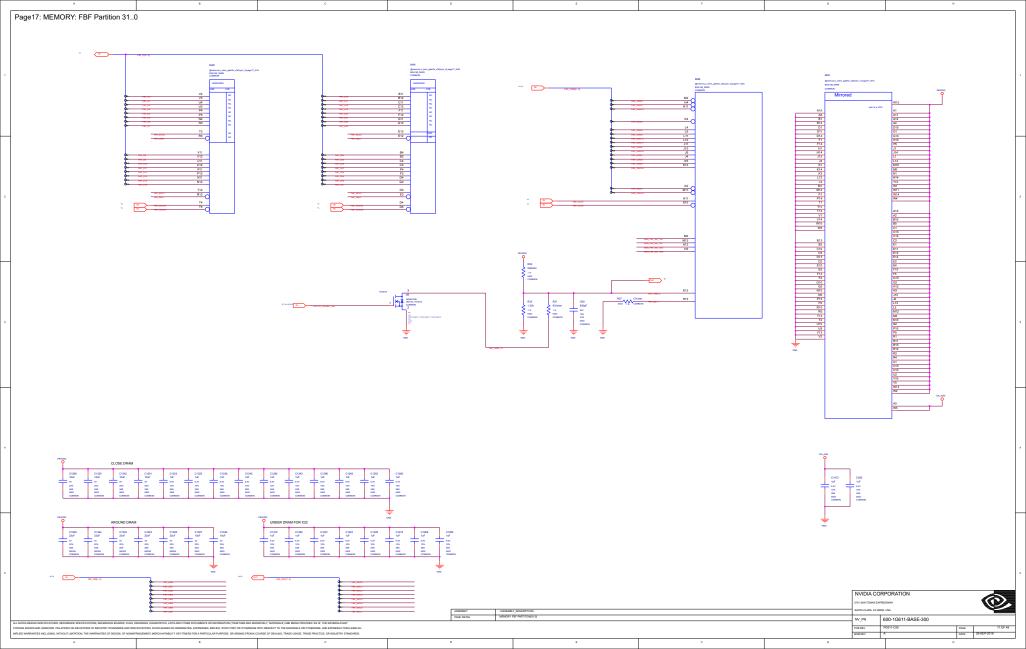


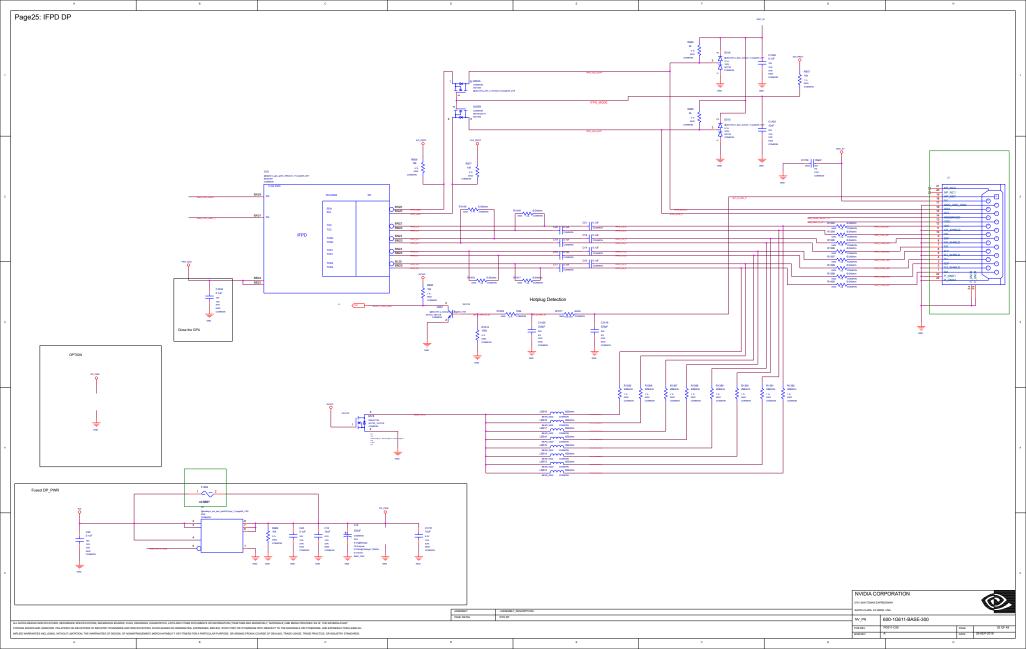


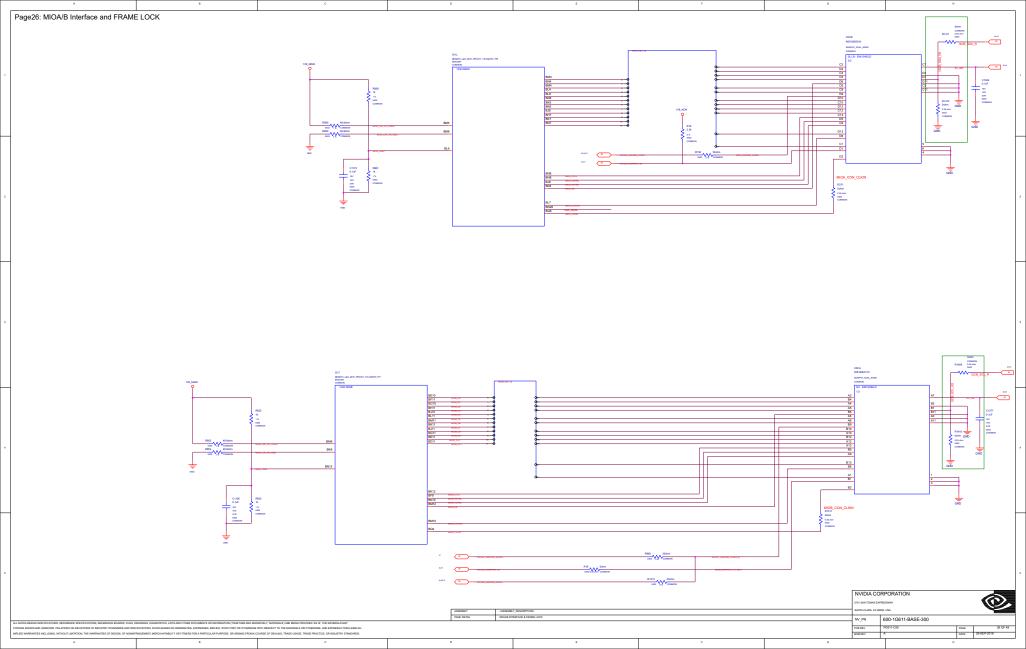


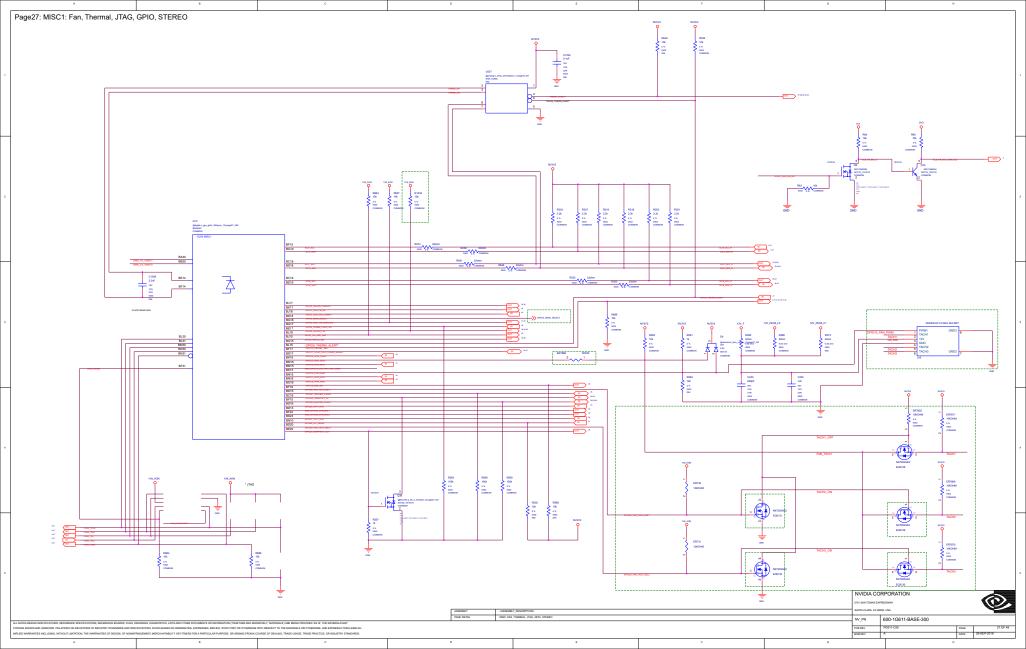


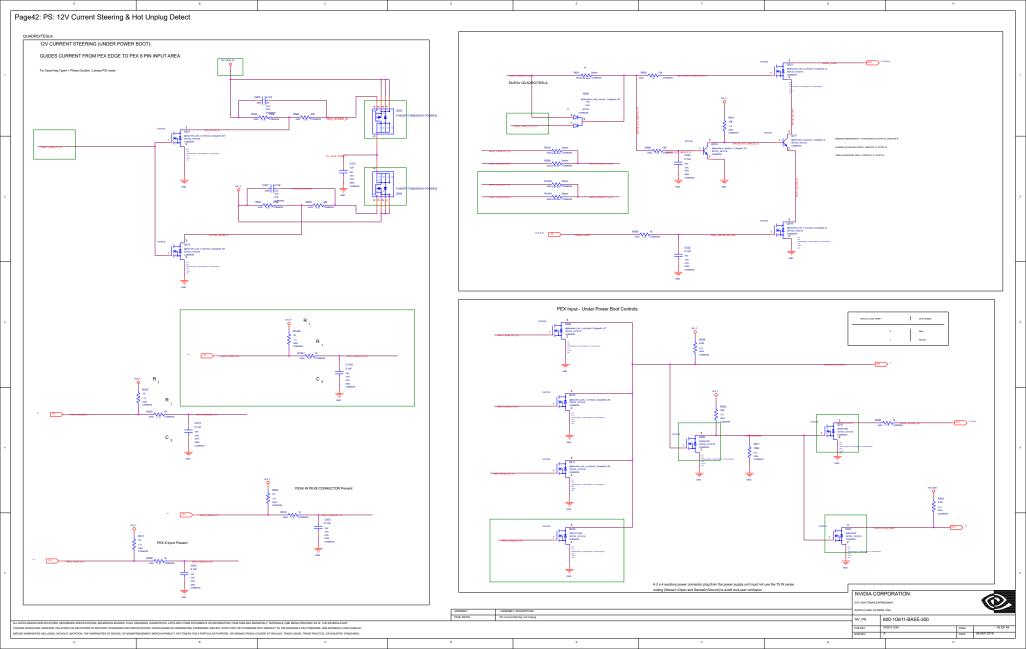


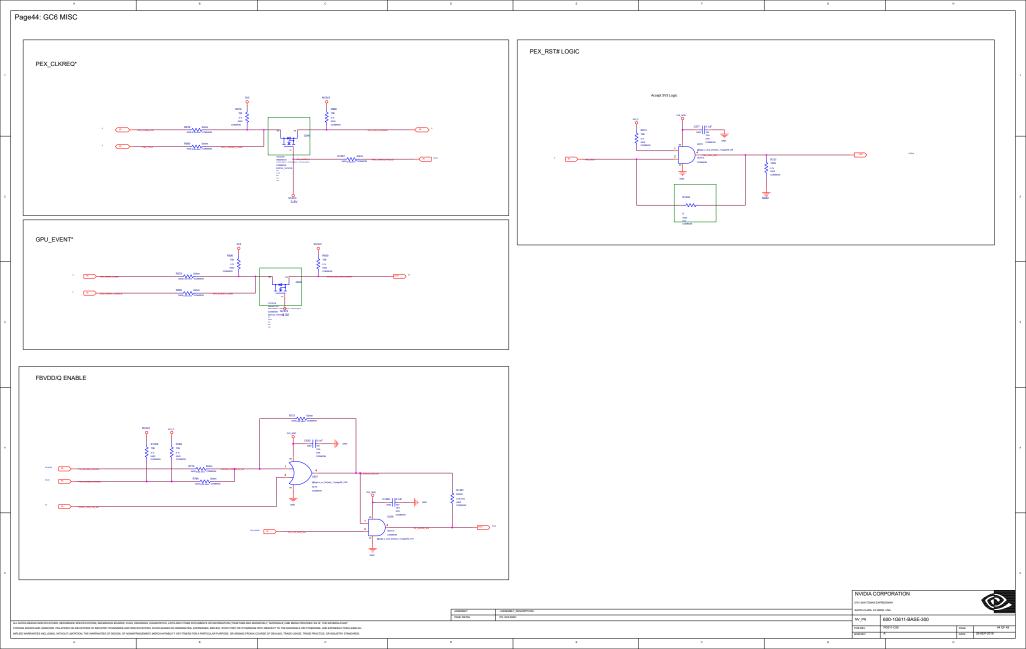


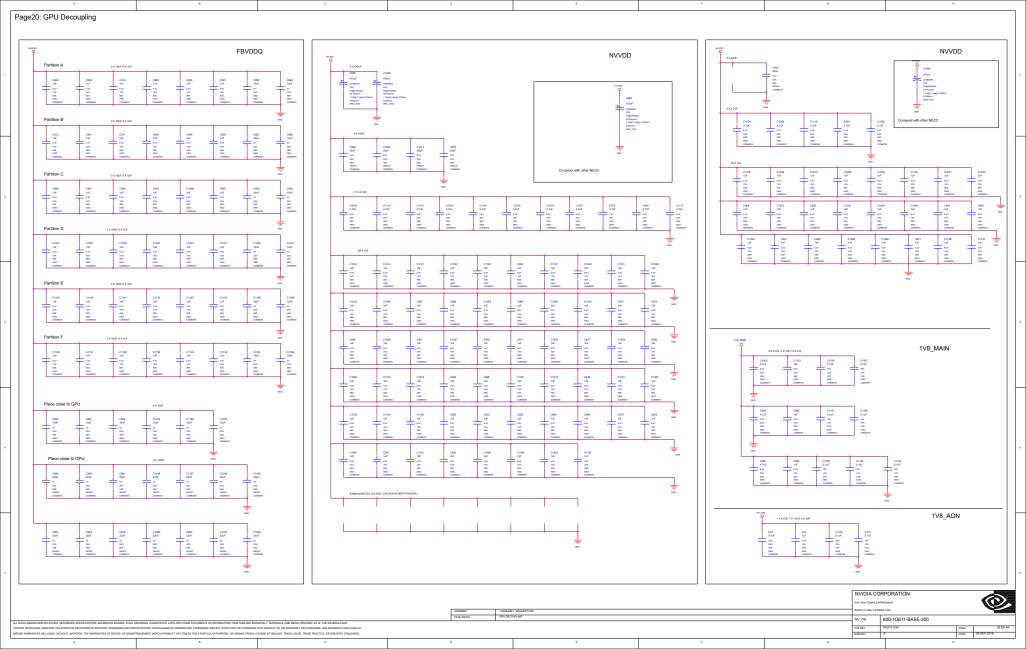


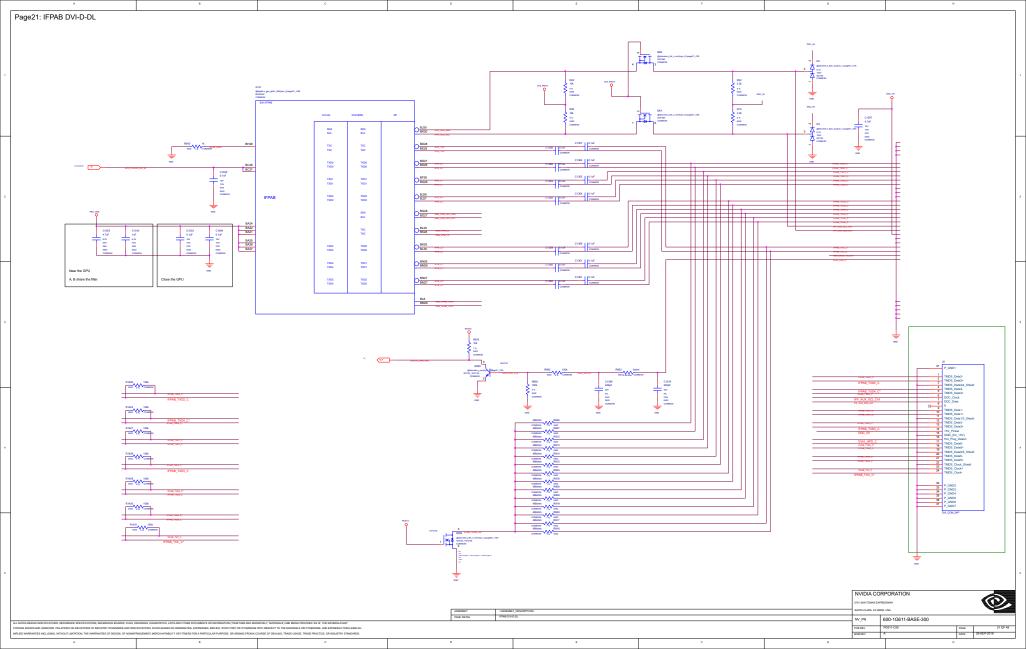


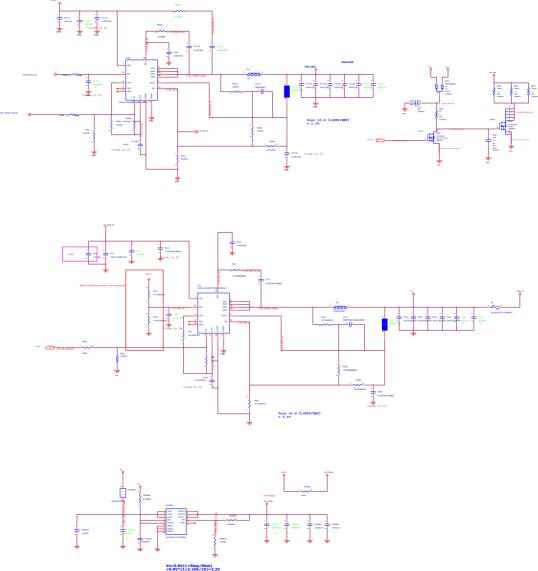


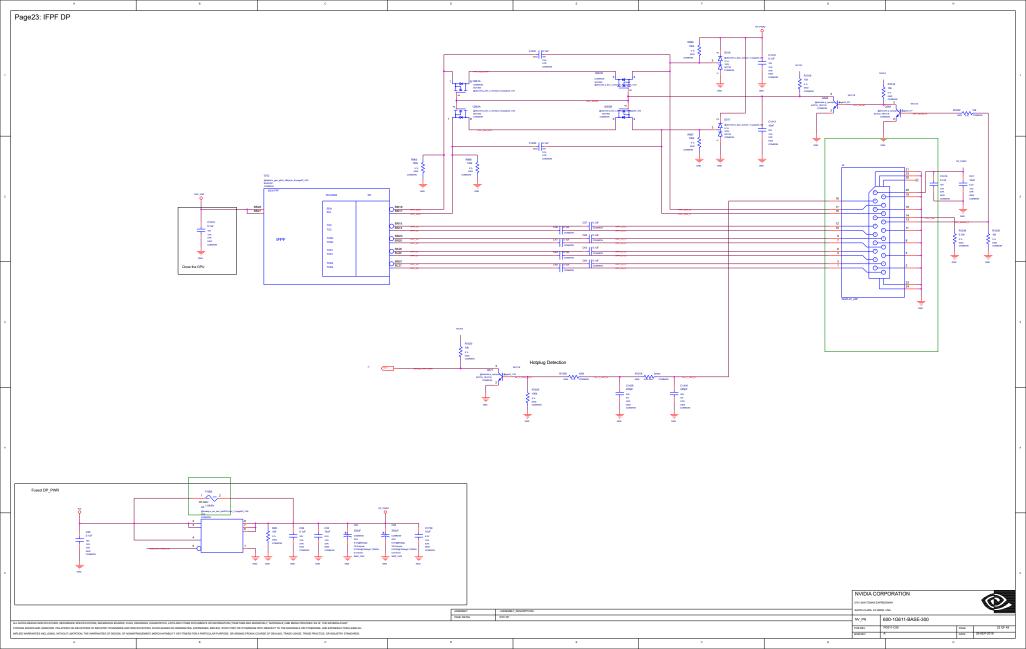


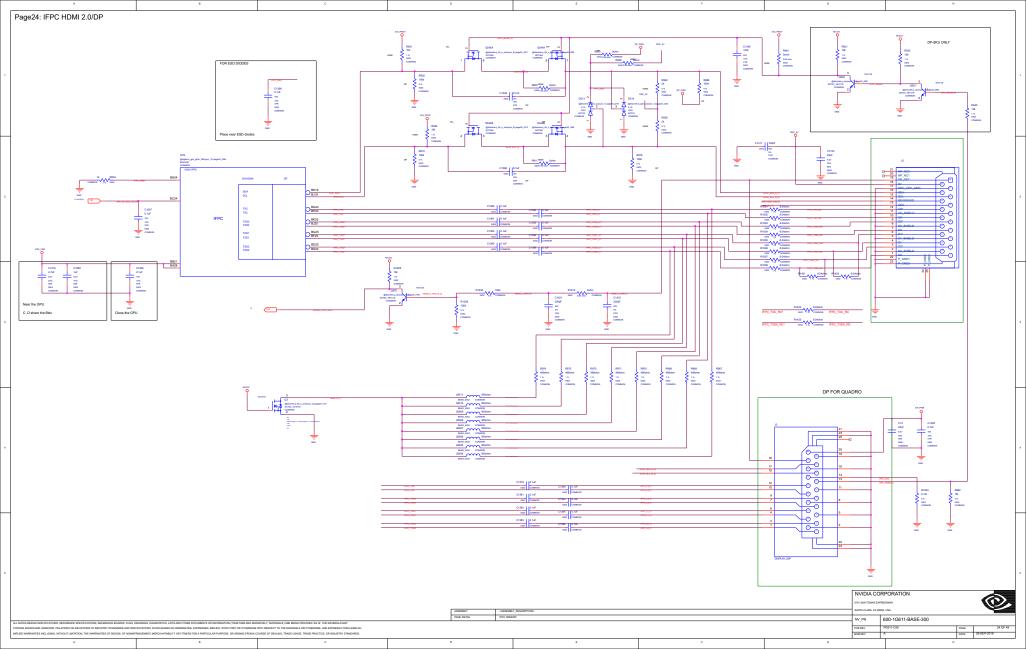


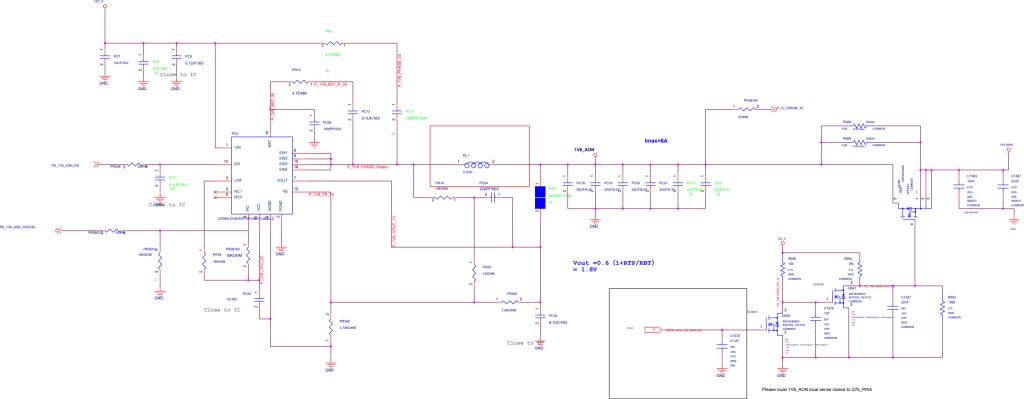


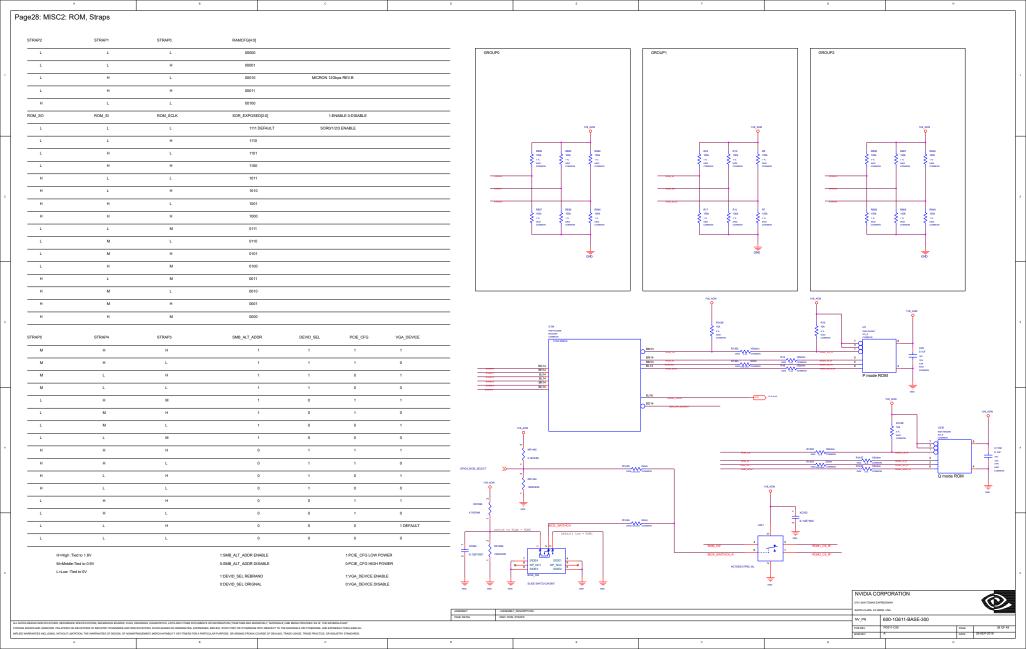


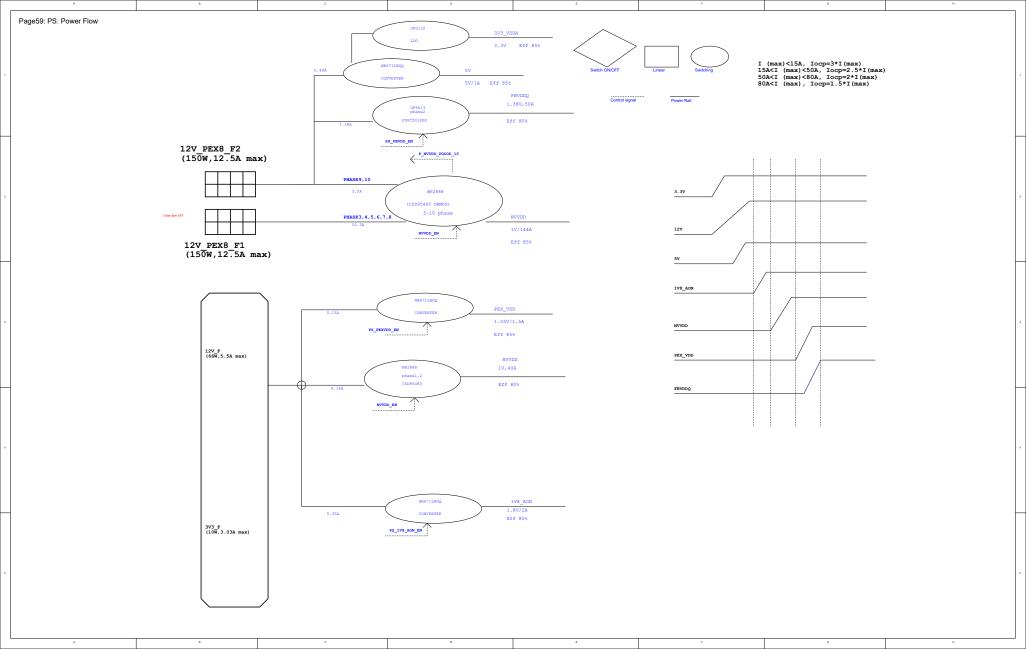


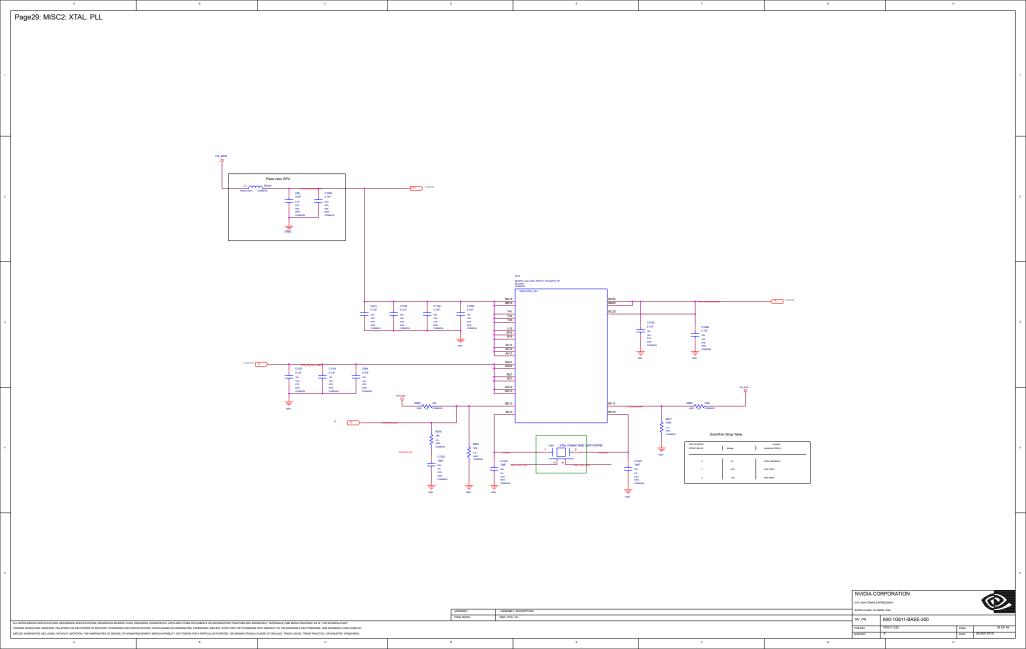


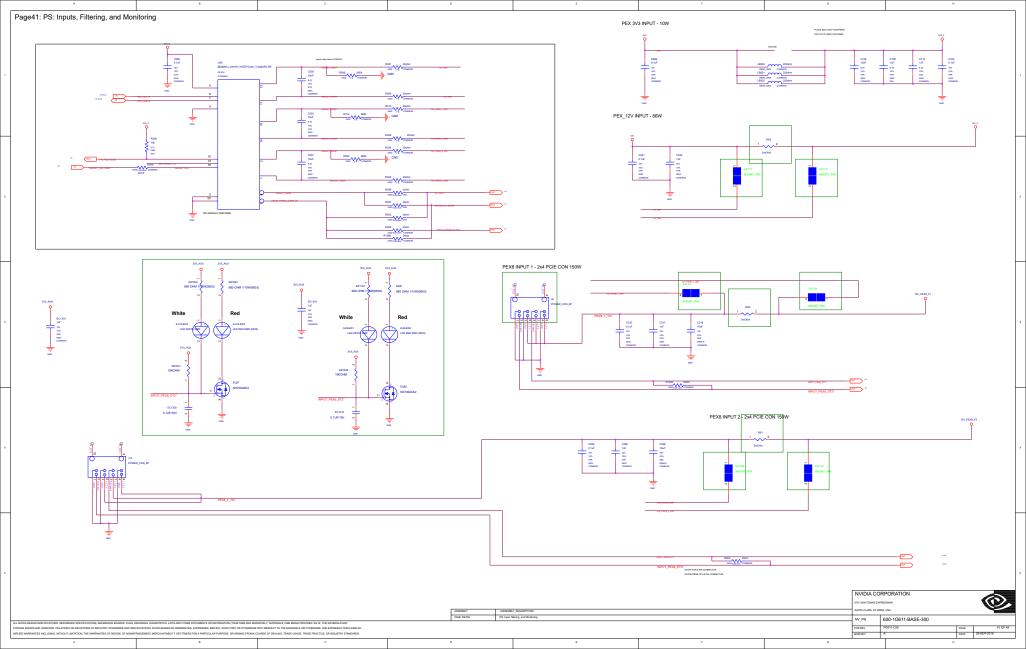


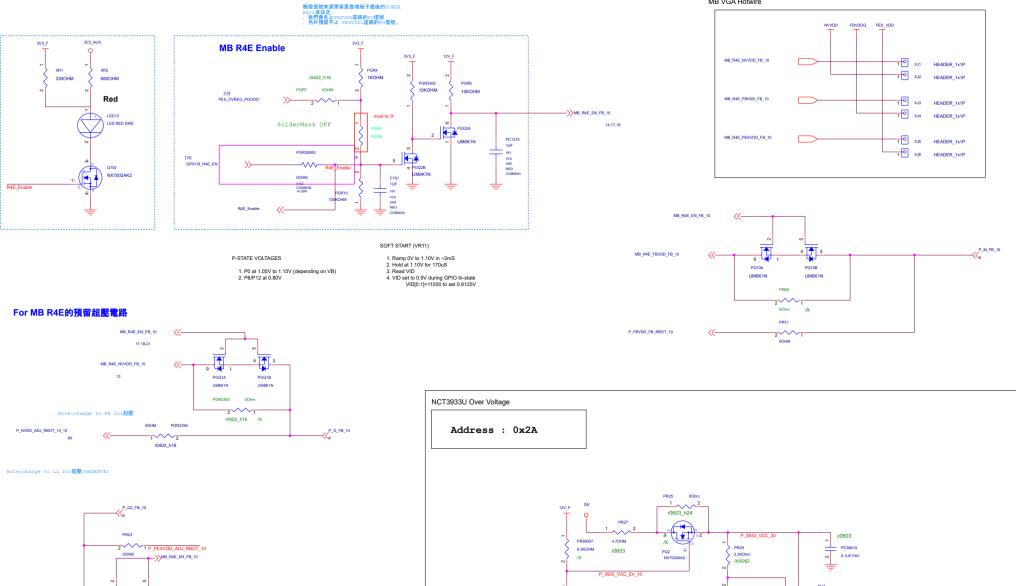










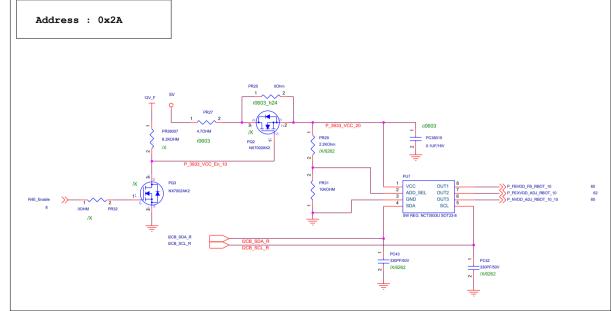


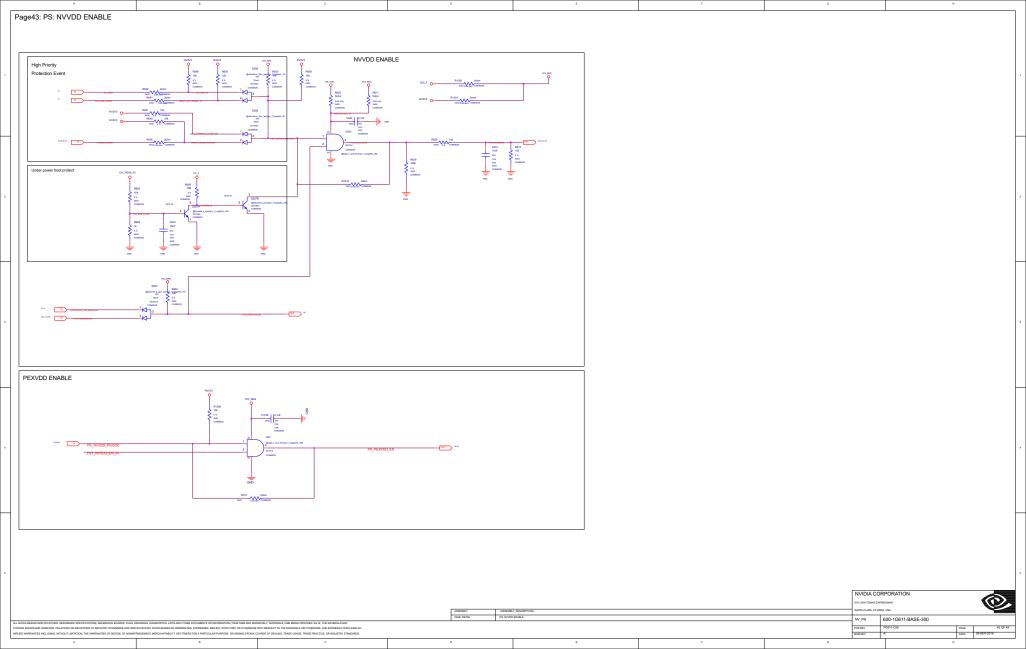
MB_R4E_PEXVDD_FB_10

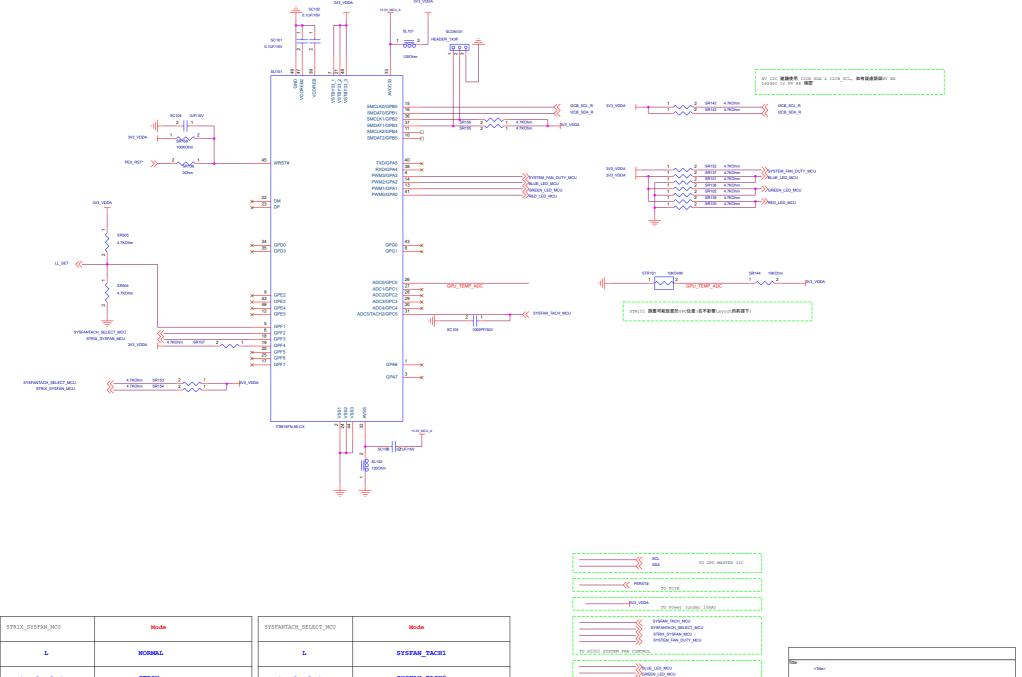
PQ23A

UM6K1N

PO23B







RED_LED_MCU

TO S0003 RGB LED

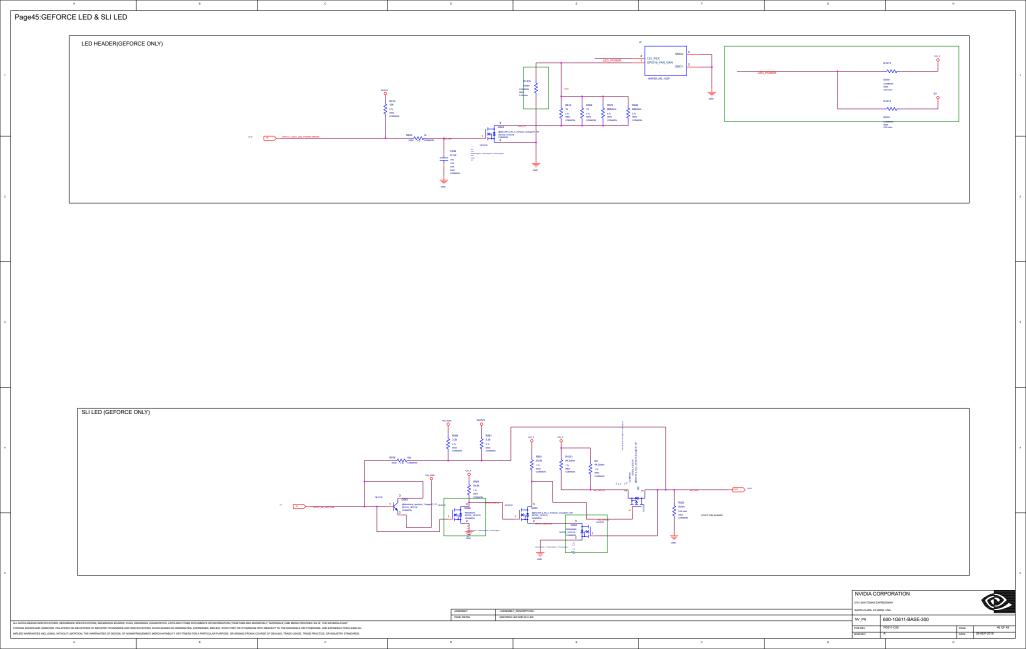
Document Number

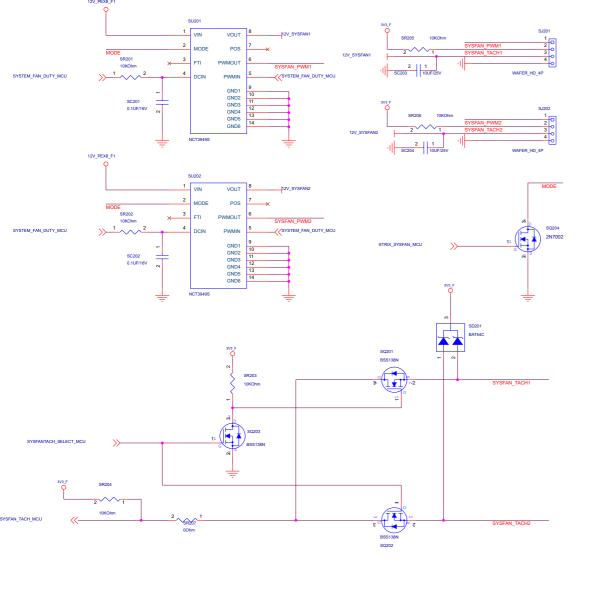
SYSFAN_TACH2

H(Default)

STRIX

H(Default)



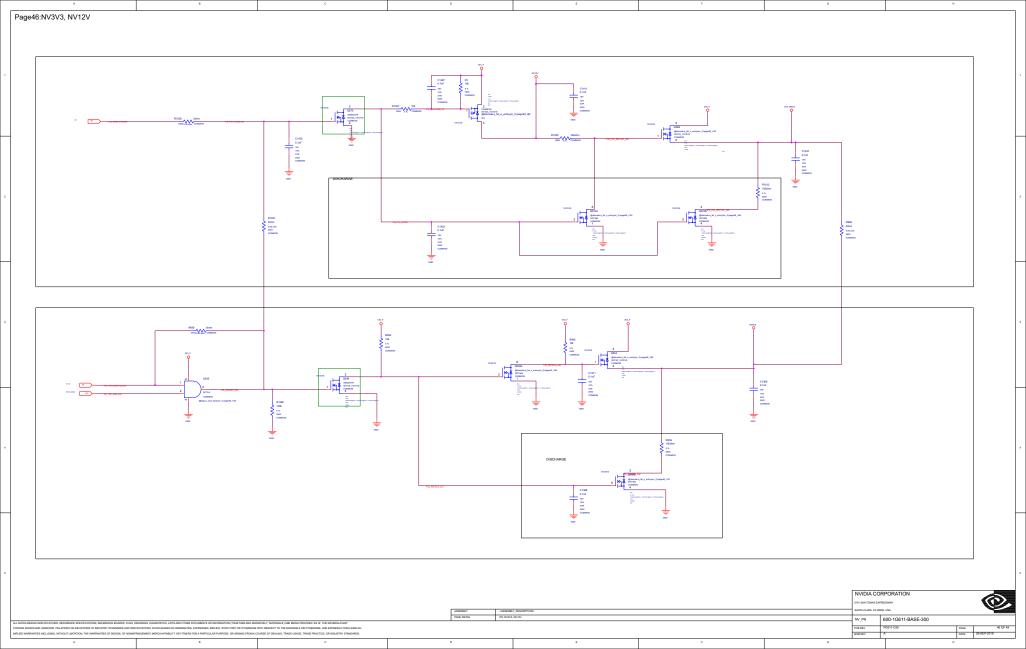


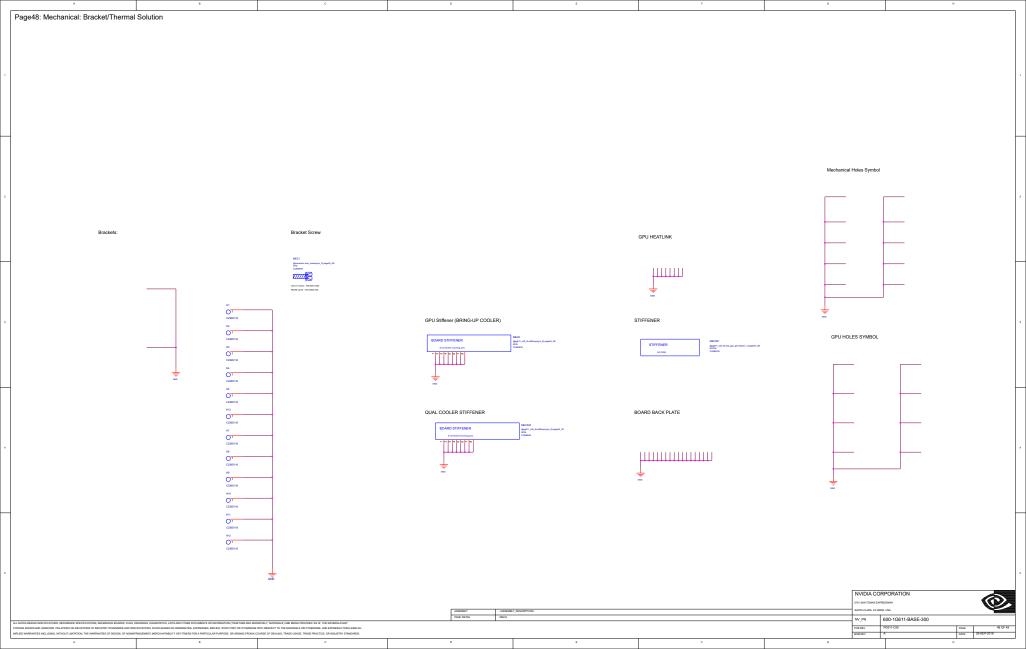


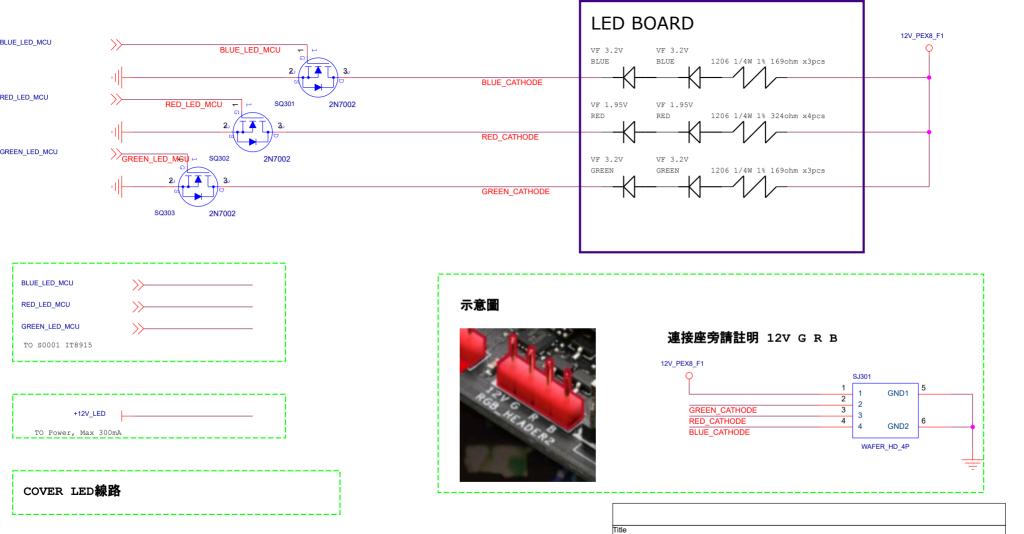
STRIX_SYSFAN_MCU	Mode
L	NORMAL
H(Default)	STRIX

SYSFANTACH_SELECT_MCU	Mode
L	SYSFAN_TACH1
H(Default)	SYSFAN_TACH2









<Title>

Date:

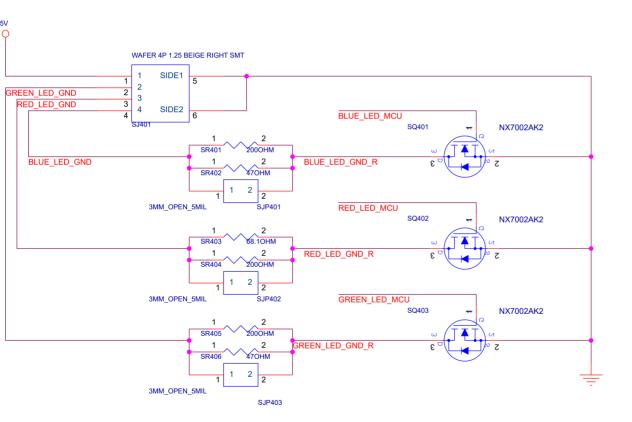
Document Number

Tuesday, August 01, 2017

Sheet

of

<RevCode>



背板ROG LED線路 TO Power BLUE_LED_MCU RED_LED_MCU

GREEN_LED_MCU

TO S0001 IT8915

