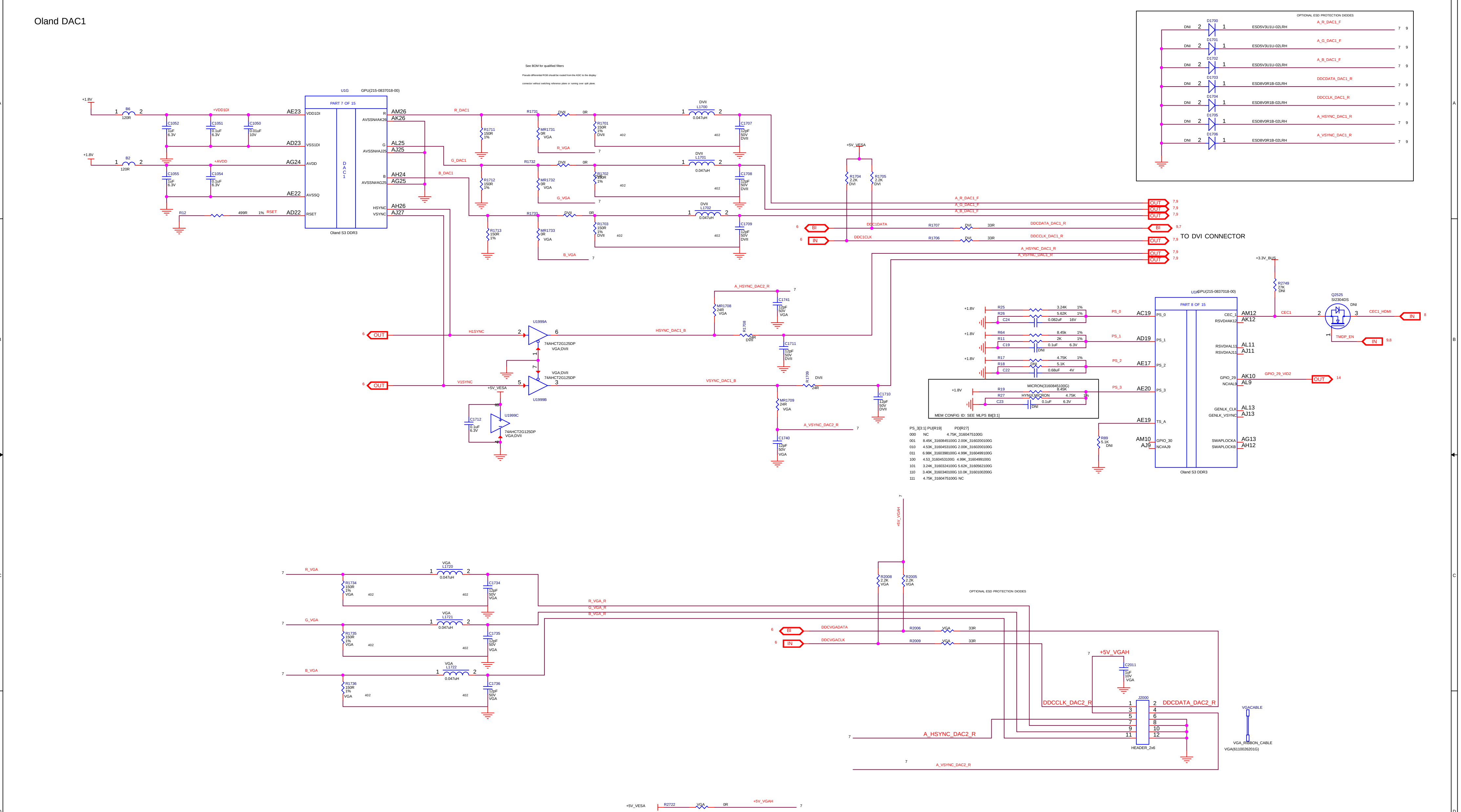
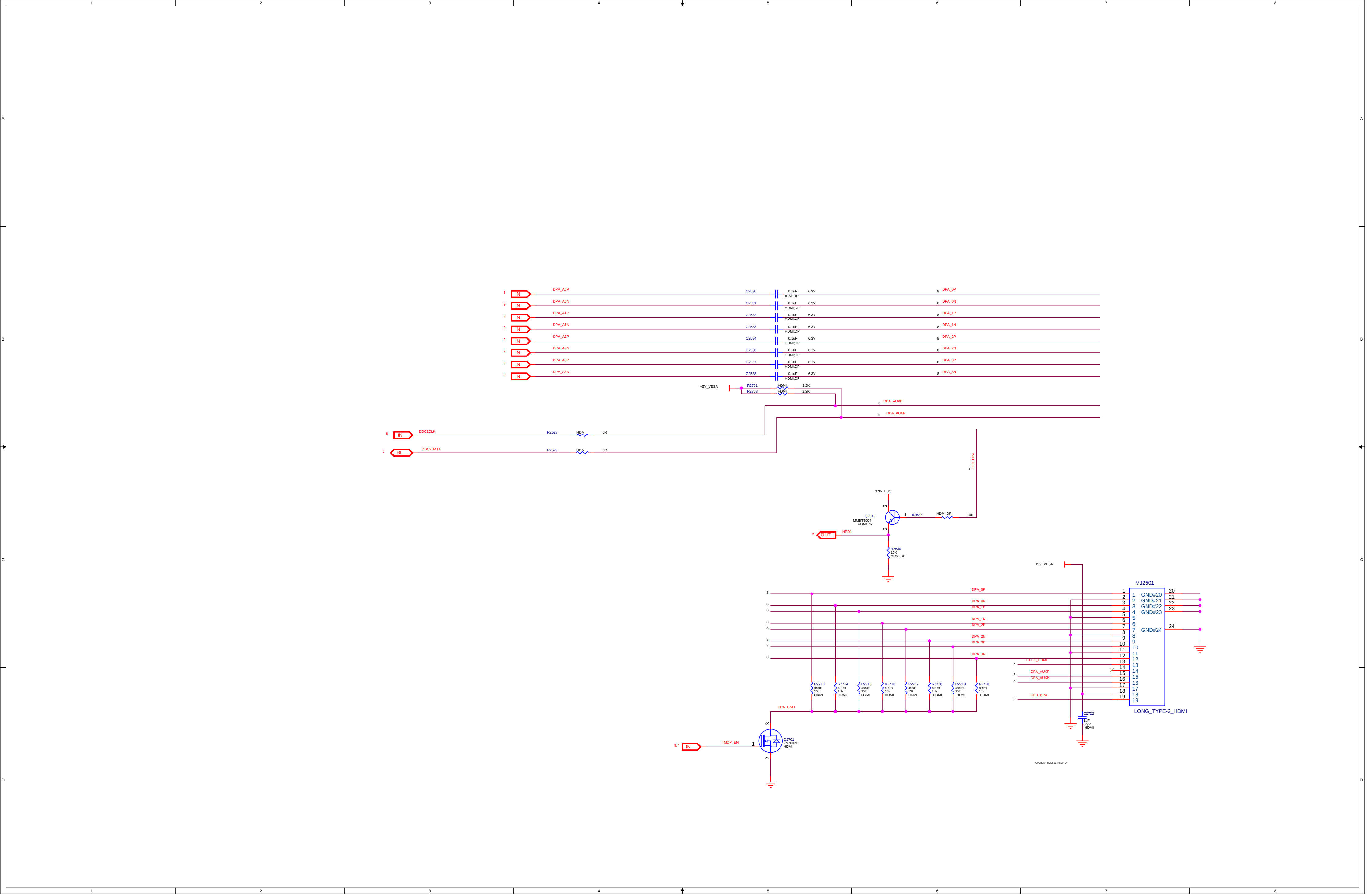
Oland DAC1

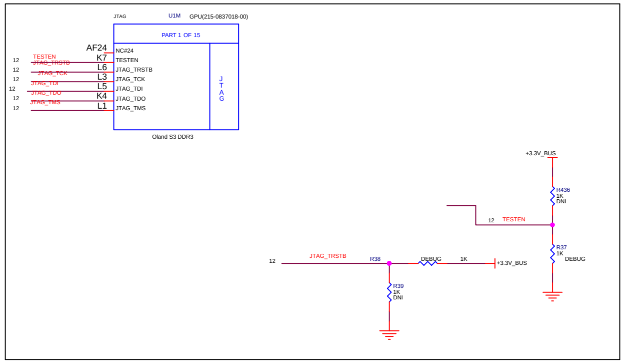


See BOM for qualified filters
Pseudo differential RGB should be routed from the ASIC to the display
connector without switching reference plane or running over split plane.
U1G
GPU(215-0837018-00)
PART 7 OF 15
DAC1
Oland S3 DDR3
+1.8V
B6
120R
B2
+VDD1DI
+AVDD
C1052
C1051
C1050
C1055
C1054
AE23
VDD1DI
AD23
VSS1DI
AG24
AVDD
AE22
AVSSQ
AD22
RSET
R12
499R
1%
AM26
AK26
AVSSN#AK26
AL25
AJ25
AVSSN#AJ25
AH24
AG25
AVSSN#AG25
AH26
HSYNC
AJ27
VSYNC
R_DAC1
G_DAC1
B_DAC1
R1711
R1712
R1713
150R
1%
R1731
R1732
R1733
MR1731
MR1732
MR1733
0R
VGA
DVII
R1701
R1702
R1703
L1700
L1701
L1702
0.047uH
C1707
C1708
C1709
12pF
50V
402
R_VGA
G_VGA
B_VGA
+5V_VESA
R1704
R1705
2.2K
DVI
A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
OUT
BI
IN
DDC1DATA
DDC1CLK
R1707
R1706
33R
DDCDATA_DAC1_R
DDCCLK_DAC1_R
TO DVI CONNECTOR
A_HSYNC_DAC1_R
A_VSYNC_DAC1_R
OPTIONAL ESD PROTECTION DIODES
D1700
D1701
D1702
D1703
D1704
D1705
D1706
DNI
ESD5V3U1U-02LRH
ESD8V0R1B-02LRH
A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
A_HSYNC_DAC1_R
A_VSYNC_DAC1_R
H1SYNC
V1SYNC
U1999A
U1999B
U1999C
74AHCT2G125DP
VGA;DVII
HSYNC_DAC1_B
VSYNC_DAC1_B
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R
MR1708
MR1709
24R
R1708
R1709
C1741
C1740
C1710
C1712
0.1uF
6.3V
U1H
GPU(215-0837018-00)
PART 8 OF 15
PS_0
PS_1
PS_2
PS_3
TS_A
GPIO_30
NC#AJ9
AC19
AD19
AE17
AE20
AE19
AM10
AJ9
R25
R26
C24
R64
R11
C19
R17
R18
C22
R19
R27
C23
3.24K
5.62K
0.082uF
8.45K
2K
4.75K
5.1K
0.68uF
MICRON(3160845100G)
HYNIX;MICRON
MEM CONFIG ID: SEE MLPS Bit[3:1]
R89
5.1K
CEC_1
RSVD#AK12
RSVD#AL11
RSVD#AJ11
GPIO_29
NC#AL9
GENLK_CLK
GENLK_VSYNC
SWAPLOCKA
SWAPLOCKB
AM12
AK12
AL11
AJ11
AK10
AL9
AL13
AJ13
AG13
AH12
CEC1
GPIO_29_VID2
+3.3V_BUS
R2749
27K
Q2525
SI2304DS
CEC1_HDMI
TMDP_EN
+5V_VGAH
R2008
R2005
DDCVGADATA
DDCVGACLK
R2006
R2009
C2011
1uF
10V
J2000
HEADER_2x6
DDCCLK_DAC2_R
DDCDATA_DAC2_R
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R
R_VGA_R
G_VGA_R
B_VGA_R
R1734
R1735
R1736
L1720
L1721
L1722
C1734
C1735
C1736
VGACABLE
VGA_RIBBON_CABLE
VGA(6110026201G)
R2722

PS_3[3:1]	PU[R19]	PD[R27]
000	NC	4.75K_3160475100G
001	8.45K_3160845100G	2.00K_3160200100G
010	4.53K_3160453100G	2.00K_3160200100G
011	6.98K_3160398100G	4.99K_3160499100G
100	4.53_3160453100G	4.99K_3160499100G
101	3.24K_3160324100G	5.62K_3160562100G
110	3.40K_3160340100G	10.0K_3160100200G
111	4.75K_3160475100G	NC


1
2
3
4
5
6
7
8
A
B
C
D
9 IN DPA_A0P C2530 0.1uF 6.3V HDMI;DP 8 DPA_0P
9 IN DPA_A0N C2531 0.1uF 6.3V HDMI;DP 8 DPA_0N
9 IN DPA_A1P C2532 0.1uF 6.3V HDMI;DP 8 DPA_1P
9 IN DPA_A1N C2533 0.1uF 6.3V HDMI;DP 8 DPA_1N
9 IN DPA_A2P C2534 0.1uF 6.3V HDMI;DP 8 DPA_2P
9 IN DPA_A2N C2536 0.1uF 6.3V HDMI;DP 8 DPA_2N
9 IN DPA_A3P C2537 0.1uF 6.3V HDMI;DP 8 DPA_3P
9 IN DPA_A3N C2538 0.1uF 6.3V HDMI;DP 8 DPA_3N
+5V_VESA
R2701 HDMI 2.2K
R2703 HDMI 2.2K
8 DPA_AUXP
8 DPA_AUXN
6 IN DDC2CLK R2528 HDMI 0R
6 BI DDC2DATA R2529 HDMI 0R
8 HPD_DPA
+3.3V_BUS
Q2513 MMBT3904 HDMI;DP
3 1 2
R2527 HDMI;DP 10K
6 OUT HPD1
R2530 10K HDMI;DP
+5V_VESA
MJ2501
LONG_TYPE-2_HDMI
GND#20 GND#21 GND#22 GND#23 GND#24
20 21 22 23 24
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
8 DPA_0P
8 DPA_0N
8 DPA_1P
8 DPA_1N
8 DPA_2P
8 DPA_2N
8 DPA_3P
8 DPA_3N
7 CEC1_HDMI
8 DPA_AUXP
8 DPA_AUXN
8 HPD_DPA
R2713 499R 1% HDMI
R2714 499R 1% HDMI
R2715 499R 1% HDMI
R2716 499R 1% HDMI
R2717 499R 1% HDMI
R2718 499R 1% HDMI
R2719 499R 1% HDMI
R2720 499R 1% HDMI
DPA_GND
C2722 1uF 6.3V HDMI
9,7 IN TMDP_EN
Q2701 2N7002E HDMI
OVERLAP HDMI WITH DP D

(19) Debug Circuits


JTAG
U1M
GPU(215-0837018-00)
PART 1 OF 15
AF24
K7
L6
L3
L5
K4
L1
NC#24
TESTEN
JTAG_TRSTB
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG
12
TESTEN
JTAG_TRSTB
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
Oland S3 DDR3
+3.3V_BUS
R436
1K
DNI
12
TESTEN
R37
1K
DEBUG
12
JTAG_TRSTB
R38
DEBUG
1K
+3.3V_BUS
R39
1K
DNI

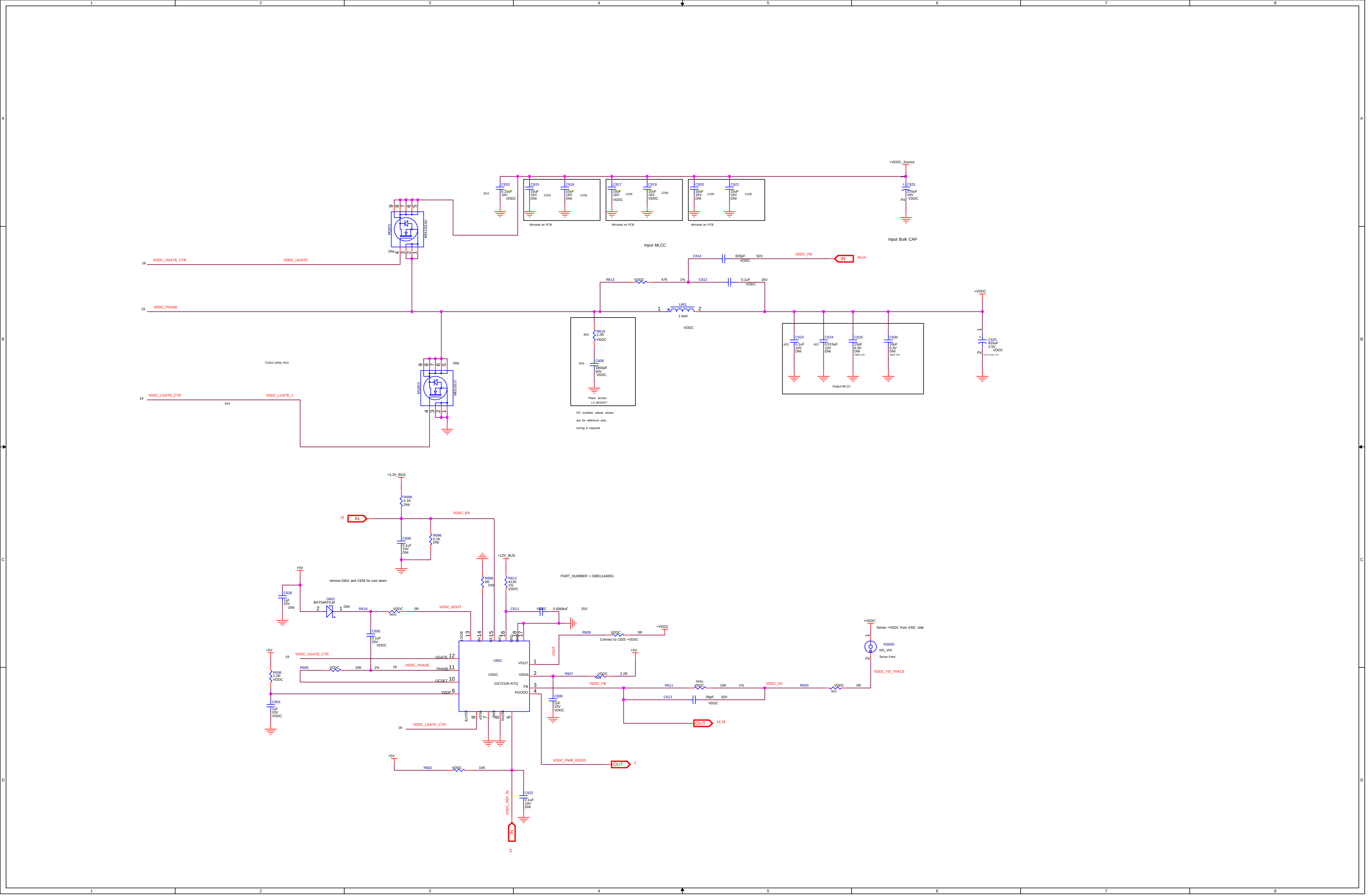

+VDDC_Source
C633 0.15uF 16V VDDC 603
C615 10uF 16V DNI 1206
C616 10uF 16V DNI 1206
C617 10uF 16V VDDC 1206
C619 10uF 16V VDDC 1206
C620 10uF 16V DNI 1206
C621 10uF 16V DNI 1206
Mirrored on PCB
Mirrored on PCB
Mirrored on PCB
Input MLCC
C631 270uF 16V VDDC
Input Bulk CAP
MQ601 MDU1514U DNI
19 VDDC_UGATE_CTR
VDDC_UGATE
19 VDDC_PHASE
TO252 DPAK PKG
MQ603 MDU1517 DNI
19 VDDC_LGATE_CTR
VDDC_LGATE_1
603
C614 820pF 50V VDDC
VDDC_FB
IN 19,14
R613 VDDC 47K 1%
C612 0.1uF 16V VDDC
L601 1.0uH VDDC
+VDDC
R619 2.2R VDDC 805
C608 1800pF 50V VDDC 603
Place across LS MOSFET
RC snubber values shown
are for reference only,
tuning is required
C623 0.1uF 10V DNI 402
C624 0.015uF 10V DNI 402
C629 10uF 6.3V DNI 0805 6.3V
C630 10uF 6.3V DNI 0805 6.3V
Output MLCC
C625 820uF 2.5V VDDC 6.3 x 9 mm, TH
+3.3V_BUS
R699 5.1K DNI
14 IN
VDDC_EN
C699 0.1uF 10V DNI
R696 5.1K DNI
+12V_BUS
R666 0R DNI
R612 412K 1% VDDC
PART_NUMBER = 2480114400G
+5V
remove D601 and C628 for cost down
C628 1uF 10V DNI
D601 BAT54KFILM DNI
R618 VDDC 0603 0R
VDDC_BOOT
C605 0.1uF 25V VDDC
C611 VDDC 0.0068uF 25V
R609 VDDC 0R
Connect to C625 +VDDC
+VDDC
VOUT
+5V
R636 2.2R VDDC
C603 1uF 10V VDDC
19 VDDC_UGATE_CTR
R605 VDDC 20K 1%
19 VDDC_PHASE
U601 VDDC GS7210A-ATQ
BOOT 13, EN 14, EN 15, TON 16, GND 18, GND 17
UGATE 12, PHASE 11, OCSET 10, VDDP 9
VOUT 1, VDDA 2, FB 3, PGOOD 4
LGATE 8, VSSP 7, GND 6, REFIN 5
R607 VDDC 805 2.2R
+5V
VDDC_FB
C606 1uF 10V VDDC
R611 RFB1 VDDC 10K 1%
VDDC_SV
R600 VDDC 603 0R
C613 56pF 50V VDDC
OUT 14,19
+VDDC
Sense +VDDC from ASIC side
NS600 NS_VIA Sense Point
VDDC_FB_TRACE
19 VDDC_LGATE_CTR
+5V
R602 VDDC 10K
VDDC_PWR_GOOD
OUT 2
C622 0.1uF 10V DNI
VDDC_REF_IN
IN 14
1 2 3 4 5 6 7 8
A B C D

TABLE OF CONTENTS

SHEET NO.	SHEET NAME
1	TOC
2	PCI-E Edge Connector
3	Oland PCIEx8 Interface
4	Oland MEM I/F CHA
5	DDR3 CHA X16
6	Oland GPIO STRAP CF PLL
7	Oland DAC
8	Oland HDMI/DP
9	Oland sDVI-I CONN
10	Oland Power&GND
11	Oland Thermal&Mech
12	Oland Debug
13	Oland Unused Modules
14	PWR SEQ
15	Sub BOM
16	0.95V
17	1.8V
18	5V
19	VDDC
20	MVDD
21	Diagram
22	REVISION HISTORY

GROUP NAME DESCRIPTION	
COMMON	INSTALLED IN MAIN BOM
NOPN	NO PN,WON'T BE IN BOM
DNI	DON'T INSTALL
INT	INTERNAL BOM, WON'T BE IN PRODUCTION BOM
GPU	GPU PN
BK	BRACKET
HS	HEATSINK OR FANSINK
BACO	BACO circuit
SUBBOM	SUBBOM PN
2ND SOURCE	
ALT	ALTERNATIVE PN(FORMAT:ALT=ALT(PN1;PN2;...)
SUB BOM	
MEM	MEMORY SUB BOM
DEBUG	DEBUG SUB BOM
POWER SUB BOM	
VDDC	VDDC SUB BOM
VDDCI	VDDCI SUB BOM
MVDD	MVDD SUB BOM
095	0.95V SUB BOM
1V8	1.8V SUB BOM

AMD - GRAPHICS
1 COMMERCE VALLEY
MARKHAM, ONTARIO, L3T 7X6

SHEET: TOC

DATE: Tue Dec 17 08:14:14 2013

REV: 1.0

SHEET NUMBER: 1 OF 22

DOCUMENT NUMBER: 105-C748xx-00A

NOTES: NOTE

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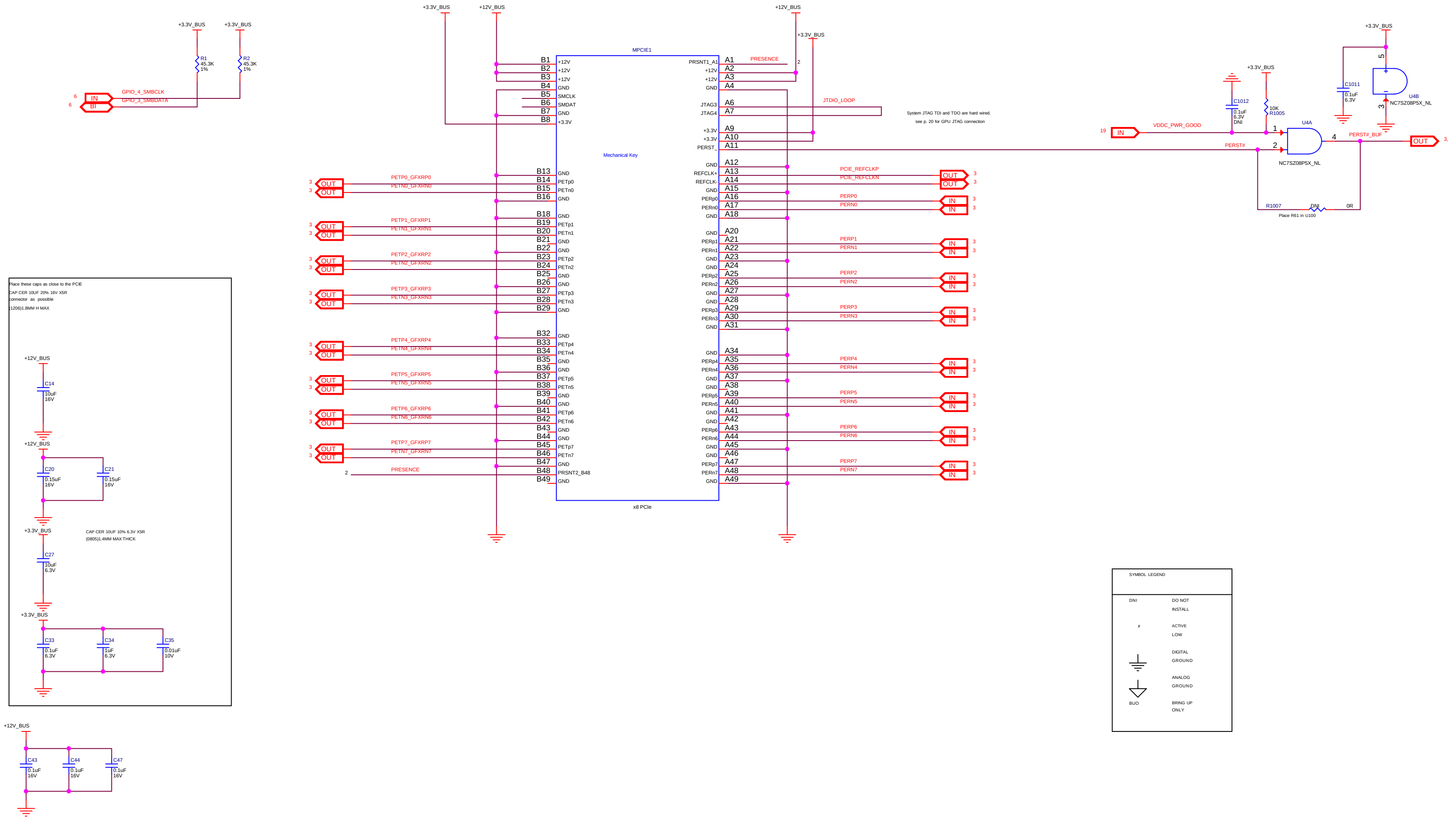
TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W

PCI-EXPRESS EDGE CONNECTOR


+3.3V_BUS
+12V_BUS
R1 45.3K 1%
R2 45.3K 1%
GPIO_4_SMBCLK
GPIO_3_SMBDATA
IN
BI
6
MPCIE1
Mechanical Key
x8 PCIe
B1 +12V
B2 +12V
B3 +12V
B4 GND
B5 SMCLK
B6 SMDAT
B7 GND
B8 +3.3V
B13 GND
B14 PETp0
B15 PETn0
B16 GND
B18 GND
B19 PETp1
B20 PETn1
B21 GND
B22 GND
B23 PETp2
B24 PETn2
B25 GND
B26 GND
B27 PETp3
B28 PETn3
B29 GND
B32 GND
B33 PETp4
B34 PETn4
B35 GND
B36 GND
B37 PETp5
B38 PETn5
B39 GND
B40 GND
B41 PETp6
B42 PETn6
B43 GND
B44 GND
B45 PETp7
B46 PETn7
B47 GND
B48 PRSNT2_B48
B49 GND
PRSNT1_A1 A1
+12V A2
+12V A3
GND A4
JTAG3 A6
JTAG4 A7
+3.3V A9
+3.3V A10
PERST_ A11
GND A12
REFCLK+ A13
REFCLK- A14
GND A15
PERp0 A16
PERn0 A17
GND A18
GND A20
PERp1 A21
PERn1 A22
GND A23
GND A24
PERp2 A25
PERn2 A26
GND A27
GND A28
PERp3 A29
PERn3 A30
GND A31
GND A34
PERp4 A35
PERn4 A36
GND A37
GND A38
PERp5 A39
PERn5 A40
GND A41
GND A42
PERp6 A43
PERn6 A44
GND A45
GND A46
PERp7 A47
PERn7 A48
GND A49
PRESENCE
2
JTDIO_LOOP
PETP0_GFXRP0
PETN0_GFXRN0
PETP1_GFXRP1
PETN1_GFXRN1
PETP2_GFXRP2
PETN2_GFXRN2
PETP3_GFXRP3
PETN3_GFXRN3
PETP4_GFXRP4
PETN4_GFXRN4
PETP5_GFXRP5
PETN5_GFXRN5
PETP6_GFXRP6
PETN6_GFXRN6
PETP7_GFXRP7
PETN7_GFXRN7
OUT
3
PCIE_REFCLKP
PCIE_REFCLKN
PERP0
PERN0
PERP1
PERN1
PERP2
PERN2
PERP3
PERN3
PERP4
PERN4
PERP5
PERN5
PERP6
PERN6
PERP7
PERN7
IN
System JTAG TDI and TDO are hard wired.
see p. 20 for GPU JTAG connection
19
VDDC_PWR_GOOD
C1012 0.1uF 6.3V DNI
10K R1005
U4A
NC7SZ08P5X_NL
PERST#
PERST#_BUF
OUT 3,
C1011 0.1uF 6.3V
U4B
NC7SZ08P5X_NL
R1007 DNI 0R
Place R61 in U100
Place these caps as close to the PCIE
CAP CER 10UF 20% 16V X5R
connector as possible
(1206)1.8MM H MAX
C14 10uF 16V
C20 0.15uF 16V
C21 0.15uF 16V
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK
C27 10uF 6.3V
C33 0.1uF 6.3V
C34 1uF 6.3V
C35 0.01uF 10V
C43 0.1uF 16V
C44 0.1uF 16V
C47 0.1uF 16V
SYMBOL LEGEND
DNI DO NOT INSTALL
# ACTIVE LOW
DIGITAL GROUND
ANALOG GROUND
BUO BRING UP ONLY

AMD - GRAPHICS
1 COMMERCE VALLEY
MARKHAM, ONTARIO, L3T 7X6

SHEET: PCI-E Edge Connector

DATE: Tue Dec 17 08:14:14 2013 REV: 1.0

SHEET NUMBER: 2 OF 22

DOCUMENT NUMBER: 105-C748xx-00A

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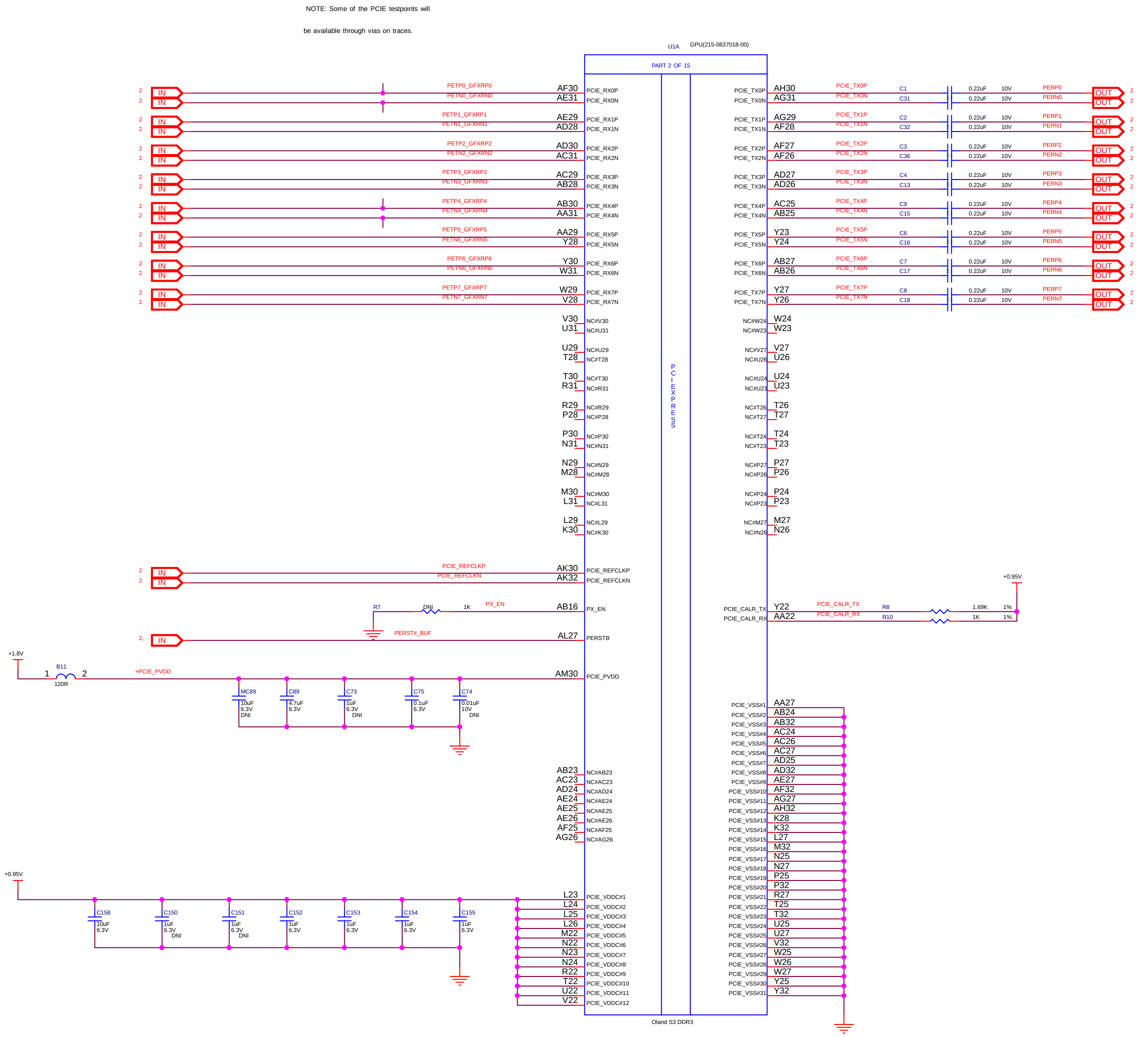
TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W

OLAND PCIe Interface

NOTE: Some of the PCIE testpoints will

be available through vias on traces.


U1A
GPU(215-0837018-00)
PART 2 OF 15
PCIEXPRESS
Oland S3 DDR3
PETP0_GFXRP0
PETN0_GFXRN0
PETP1_GFXRP1
PETN1_GFXRN1
PETP2_GFXRP2
PETN2_GFXRN2
PETP3_GFXRP3
PETN3_GFXRN3
PETP4_GFXRP4
PETN4_GFXRN4
PETP5_GFXRP5
PETN5_GFXRN5
PETP6_GFXRP6
PETN6_GFXRN6
PETP7_GFXRP7
PETN7_GFXRN7
IN
2
AF30 PCIE_RX0P
AE31 PCIE_RX0N
AE29 PCIE_RX1P
AD28 PCIE_RX1N
AD30 PCIE_RX2P
AC31 PCIE_RX2N
AC29 PCIE_RX3P
AB28 PCIE_RX3N
AB30 PCIE_RX4P
AA31 PCIE_RX4N
AA29 PCIE_RX5P
Y28 PCIE_RX5N
Y30 PCIE_RX6P
W31 PCIE_RX6N
W29 PCIE_RX7P
V28 PCIE_RX7N
V30 NC#V30
U31 NC#U31
U29 NC#U29
T28 NC#T28
T30 NC#T30
R31 NC#R31
R29 NC#R29
P28 NC#P28
P30 NC#P30
N31 NC#N31
N29 NC#N29
M28 NC#M28
M30 NC#M30
L31 NC#L31
L29 NC#L29
K30 NC#K30
PCIE_REFCLKP
PCIE_REFCLKN
AK30 PCIE_REFCLKP
AK32 PCIE_REFCLKN
R7
DNI
1K
PX_EN
AB16 PX_EN
2,
PERST#_BUF
AL27 PERSTB
+1.8V
B11
1
2
120R
+PCIE_PVDD
AM30 PCIE_PVDD
MC89 10uF 6.3V DNI
C89 4.7uF 6.3V
C73 1uF 6.3V DNI
C75 0.1uF 6.3V
C74 0.01uF 10V DNI
AB23 NC#AB23
AC23 NC#AC23
AD24 NC#AD24
AE24 NC#AE24
AE25 NC#AE25
AE26 NC#AE26
AF25 NC#AF25
AG26 NC#AG26
+0.95V
C158 10uF 6.3V
C150 1uF 6.3V DNI
C151 1uF 6.3V DNI
C152 1uF 6.3V
C153 1uF 6.3V
C154 1uF 6.3V
C155 1uF 6.3V
L23 PCIE_VDDC#1
L24 PCIE_VDDC#2
L25 PCIE_VDDC#3
L26 PCIE_VDDC#4
M22 PCIE_VDDC#5
N22 PCIE_VDDC#6
N23 PCIE_VDDC#7
N24 PCIE_VDDC#8
R22 PCIE_VDDC#9
T22 PCIE_VDDC#10
U22 PCIE_VDDC#11
V22 PCIE_VDDC#12
PCIE_TX0P AH30
PCIE_TX0N AG31
PCIE_TX1P AG29
PCIE_TX1N AF28
PCIE_TX2P AF27
PCIE_TX2N AF26
PCIE_TX3P AD27
PCIE_TX3N AD26
PCIE_TX4P AC25
PCIE_TX4N AB25
PCIE_TX5P Y23
PCIE_TX5N Y24
PCIE_TX6P AB27
PCIE_TX6N AB26
PCIE_TX7P Y27
PCIE_TX7N Y26
C1 0.22uF 10V PERP0
C31 0.22uF 10V PERN0
C2 0.22uF 10V PERP1
C32 0.22uF 10V PERN1
C3 0.22uF 10V PERP2
C36 0.22uF 10V PERN2
C4 0.22uF 10V PERP3
C13 0.22uF 10V PERN3
C9 0.22uF 10V PERP4
C15 0.22uF 10V PERN4
C6 0.22uF 10V PERP5
C16 0.22uF 10V PERN5
C7 0.22uF 10V PERP6
C17 0.22uF 10V PERN6
C8 0.22uF 10V PERP7
C18 0.22uF 10V PERN7
OUT
NC#W24 W24
NC#W23 W23
NC#V27 V27
NC#U26 U26
NC#U24 U24
NC#U23 U23
NC#T26 T26
NC#T27 T27
NC#T24 T24
NC#T23 T23
NC#P27 P27
NC#P26 P26
NC#P24 P24
NC#P23 P23
NC#M27 M27
NC#N26 N26
+0.95V
PCIE_CALR_TX Y22
PCIE_CALR_RX AA22
R8 1.69K 1%
R10 1K 1%
PCIE_VSS#1 AA27
PCIE_VSS#2 AB24
PCIE_VSS#3 AB32
PCIE_VSS#4 AC24
PCIE_VSS#5 AC26
PCIE_VSS#6 AC27
PCIE_VSS#7 AD25
PCIE_VSS#8 AD32
PCIE_VSS#9 AE27
PCIE_VSS#10 AF32
PCIE_VSS#11 AG27
PCIE_VSS#12 AH32
PCIE_VSS#13 K28
PCIE_VSS#14 K32
PCIE_VSS#15 L27
PCIE_VSS#16 M32
PCIE_VSS#17 N25
PCIE_VSS#18 N27
PCIE_VSS#19 P25
PCIE_VSS#20 P32
PCIE_VSS#21 R27
PCIE_VSS#22 T25
PCIE_VSS#23 T32
PCIE_VSS#24 U25
PCIE_VSS#25 U27
PCIE_VSS#26 V32
PCIE_VSS#27 W25
PCIE_VSS#28 W26
PCIE_VSS#29 W27
PCIE_VSS#30 Y25
PCIE_VSS#31 Y32

AMD - GRAPHICS
1 COMMERCE VALLEY
MARKHAM, ONTARIO, L3T 7X6

SHEET:	Oland PCIEx8 Interface
DATE:	Tue Dec 17 08:14:14 2013
REV:	1.0
SHEET NUMBER:	3 OF 22
DOCUMENT NUMBER:	105-C748xx-00A

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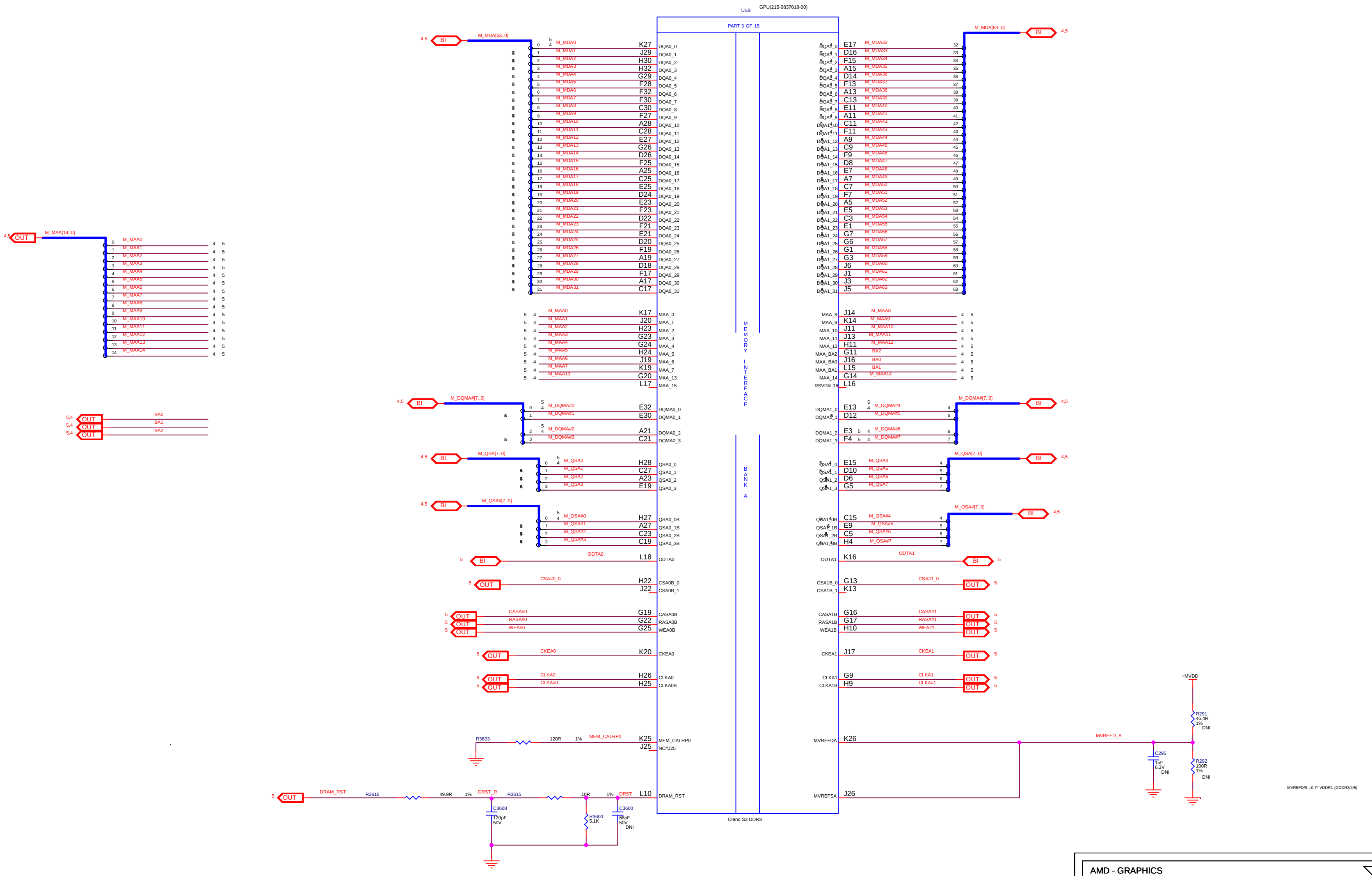
TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W

Oland S3 MEM Interface Ch A&B



U1B
GPU(215-0837018-00)
PART 3 OF 15
MEMORY INTERFACE
BANK A
Oland S3 DDR3
M_MDA[63..0]
M_MAA[14..0]
M_DQMA#[7..0]
M_QSA[7..0]
M_QSA#[7..0]
BA0
BA1
BA2
ODTA0
ODTA1
CSA#0_0
CSA#1_0
CASA#0
RASA#0
WEA#0
CASA#1
RASA#1
WEA#1
CKEA0
CKEA1
CLKA0
CLKA#0
CLKA1
CLKA#1
MEM_CALRP0
MEM_CALRP0
NC#J25
DRAM_RST
DRST_R
DRST
MVREFDA
MVREFSA
MVREFD_A
+MVDD
R3603 120R 1%
R3616 49.9R 1%
R3615 10R 1%
R3600 5.1K
C3608 120pF 50V
C3600 68pF 50V DNI
R291 46.4R 1% DNI
R292 100R 1% DNI
C295 1uF 6.3V DNI
MVREFD/S =0.7* VDDR1 (GDDR3/4/5)
BI
OUT

AMD - GRAPHICS
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MARKHAM, ONTARIO, L3T 7X6

SHEET: Oland MEM I/F CHA

DATE: Tue Dec 17 08:14:15 2013

REV: 1.0

SHEET NUMBER: 4 OF 22

DOCUMENT NUMBER: 105-C748xx-00A

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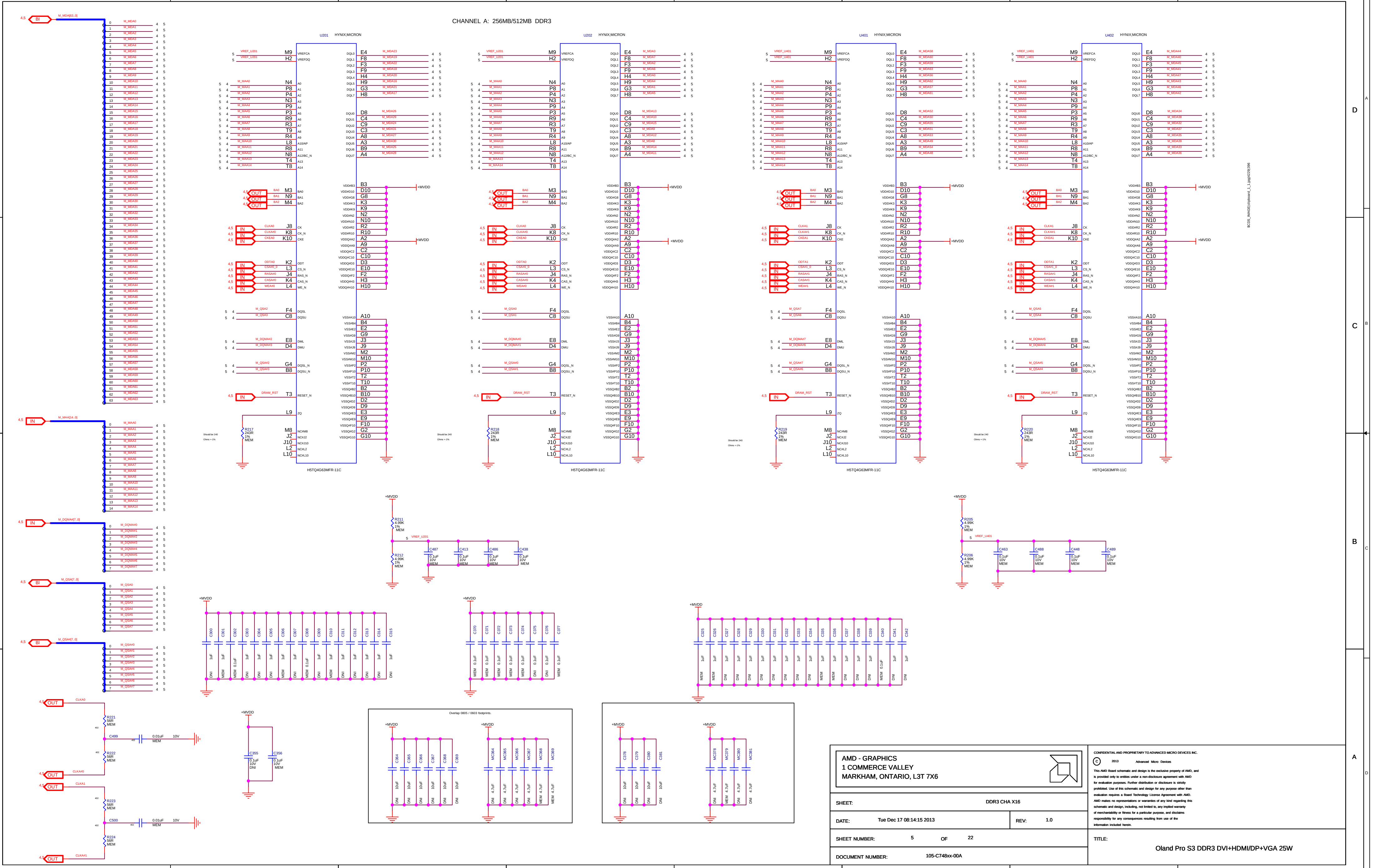
TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W


CHANNEL A: 256MB/512MB DDR3
U201
HYNIX;MICRON
U202
HYNIX;MICRON
U401
HYNIX;MICRON
U402
HYNIX;MICRON
H5TQ4G63MFR-11C
M_MDA[63..0]
M_MAA[14..0]
M_DQMA#[7..0]
M_QSA[7..0]
M_QSA#[7..0]
BI
IN
OUT
VREF_U201
VREF_U401
DRAM_RST
RESET_N
ZQ
R217
243R
1%
MEM
Should be 240
Ohms +-1%
+MVDD
R211
4.99K
R212
R205
R206
R221
56R
R222
R223
R224
C499
C500
0.01uF
10V
CLKA0
CLKA#0
CLKA1
CLKA#1
Overlap 0805 / 0603 footprints.
C364
C365
C366
C367
C368
C369
MC364
MC365
MC366
MC367
MC368
MC369
10uF
4.7uF
1uF
0.1uF
DNI
MEM

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SHEET: DDR3 CHA X16

DATE: Tue Dec 17 08:14:15 2013

REV: 1.0

SHEET NUMBER: 5 OF 22

DOCUMENT NUMBER: 105-C748xx-00A

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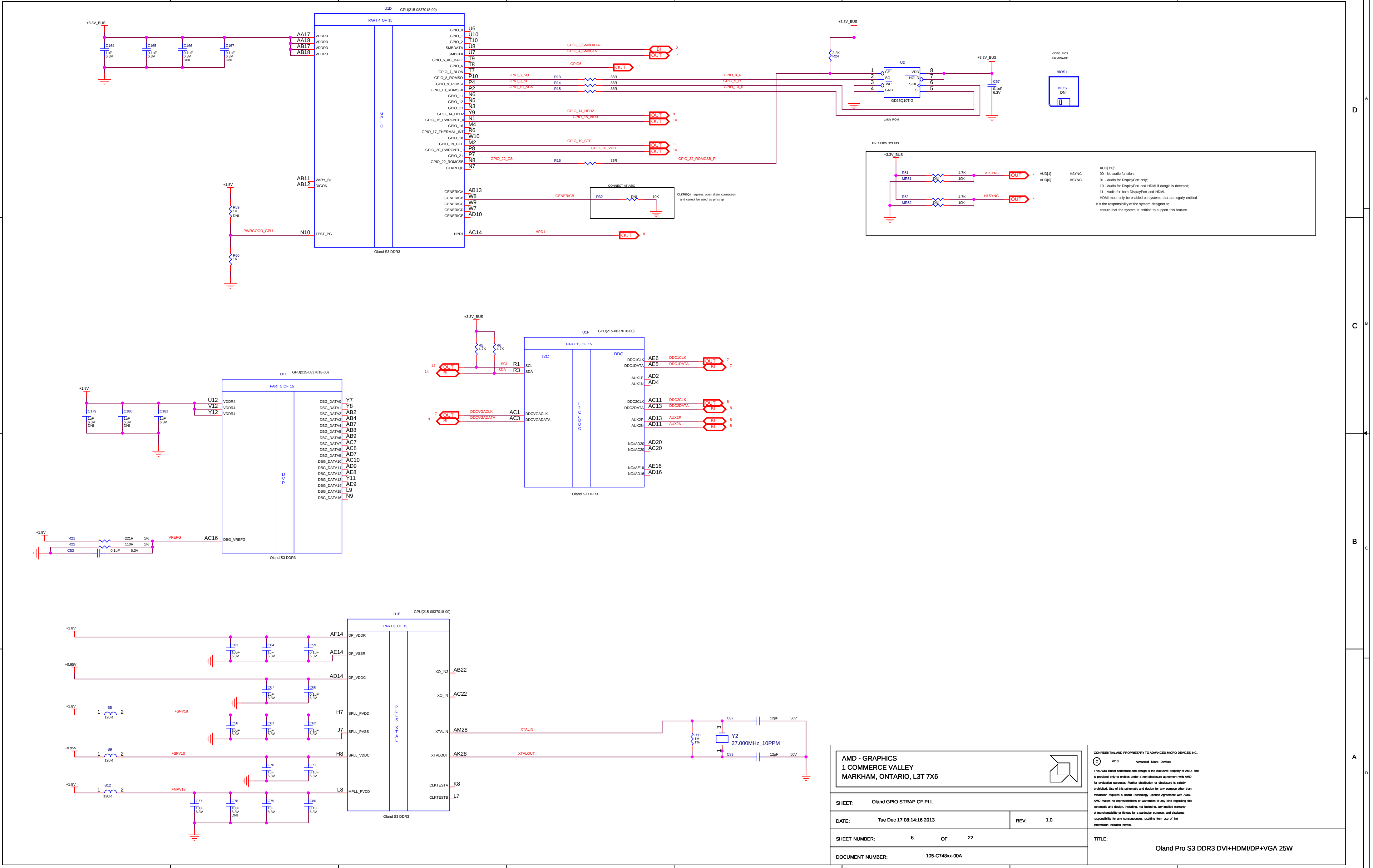
TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W


U1D
GPU(215-0837018-00)
PART 4 OF 15
GPIO
+3.3V_BUS
C164 1uF 6.3V
C165 0.1uF 6.3V
C166 0.1uF 6.3V DNI
C167 0.1uF 6.3V DNI
AA17 AA18 AB17 AB18 VDDR3
GPIO_0 U6
GPIO_1 U10
GPIO_2 T10
SMBDATA U8
SMBCLK U7
GPIO_5_AC_BATT T9
GPIO_6 T8
GPIO_7_BLON T7
GPIO_8_ROMSO P10
GPIO_9_ROMSI P4
GPIO_10_ROMSCK P2
GPIO_11 N6
GPIO_12 N5
GPIO_13 N3
GPIO_14_HPD2 Y9
GPIO_15_PWRCNTL_0 N1
GPIO_16 M4
GPIO_17_THERMAL_INT R6
GPIO_18 W10
GPIO_19_CTF M2
GPIO_20_PWRCNTL_1 P8
GPIO_21 P7
GPIO_22_ROMCSB N8
CLKREQB N7
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO6
GPIO_8_SO R13 33R GPIO_8_R
GPIO_9_SI R14 33R GPIO_9_R
GPIO_10_SCK R15 33R GPIO_10_R
GPIO_14_HPD2
GPIO_15_VID0
GPIO_19_CTF
GPIO_20_VID1
GPIO_22_CS R16 33R GPIO_22_ROMCSB_R
BI OUT
AB11 VARY_BL
AB12 DIGON
N10 TEST_PG
GENERICA AB13
GENERICB W8
GENERICC W9
GENERICD W7
GENERICE AD10
HPD1 AC14
GENERICB
CONNECT AT ASIC
R32 DNI 10K
CLKREQ# requires open drain connection, and cannot be used as pinstrap
HPD1
+1.8V
R59 1K DNI
PWRGOOD_GPU
R60 1K
Oland S3 DDR3
+3.3V_BUS
2.2K R24
U2
CE SO WP GND VDD HOLD SCK SI
GD25Q10TIG
1Mbit ROM
+3.3V_BUS
C57 0.1uF 6.3V
VIDEO BIOS FIRMWARE
BIOS1
BIOS DNI
PIN BASED STRAPS
+3.3V_BUS
R51 4.7K V1SYNC
MR51 DNI 10K
R52 4.7K H1SYNC
MR52 DNI 10K
AUD[1] HSYNC
AUD[0] VSYNC
AUD[1:0]:
00 - No audio function;
01 - Audio for DisplayPort only;
10 - Audio for DisplayPort and HDMI if dongle is detected;
11 - Audio for both DisplayPort and HDMI.
HDMI must only be enabled on systems that are legally entitled
. It is the responsibility of the system designer to
ensure that the system is entitled to support this feature
U1F
GPU(215-0837018-00)
PART 15 OF 15
I2C
DDC
I2C/DDC
+3.3V_BUS
R5 4.7K
R6 4.7K
SCL R1
SDA R3
DDC1CLK AE6
DDC1DATA AE5
AUX1P AD2
AUX1N AD4
DDC2CLK AC11
DDC2DATA AC13
AUX2P AD13
AUX2N AD11
NC#AD20 AD20
NC#AC20 AC20
NC#AE16 AE16
NC#AD16 AD16
DDCVGACLK AC1
DDCVGADATA AC3
U1C
GPU(215-0837018-00)
PART 5 OF 15
DVP
+1.8V
C179 1uF 6.3V DNI
C180 1uF 6.3V DNI
C181 1uF 6.3V
U12 V12 Y12 VDDR4
DBG_DATA0 Y7
DBG_DATA1 Y8
DBG_DATA2 AB2
DBG_DATA3 AB4
DBG_DATA4 AB7
DBG_DATA5 AB8
DBG_DATA6 AB9
DBG_DATA7 AC7
DBG_DATA8 AC8
DBG_DATA9 AD7
DBG_DATA10 AC10
DBG_DATA11 AD9
DBG_DATA12 AE8
DBG_DATA13 Y11
DBG_DATA14 AE9
DBG_DATA15 L9
DBG_DATA16 N9
DBG_VREFG AC16
R21 221R 1%
R22 110R 1%
C53 0.1uF 6.3V
VREFG
U1E
GPU(215-0837018-00)
PART 6 OF 15
PLLS XTAL
+1.8V
C63 10uF 6.3V
C64 1uF 6.3V
C59 0.1uF 6.3V
DP_VDDR AF14
DP_VSSR AE14
+0.95V
DP_VDDC AD14
C67 1uF 6.3V
C66 0.1uF 6.3V
B5 120R +SPV18
SPLL_PVDD H7
C58 10uF 6.3V
C61 1uF 6.3V
C62 0.1uF 6.3V
SPLL_PVSS J7
B9 120R +SPV10
SPLL_VDDC H8
C70 1uF 6.3V
C71 0.1uF 6.3V
B12 120R +MPV18
MPLL_PVDD L8
C77 10uF 6.3V
C78 10uF 6.3V DNI
C79 1uF 6.3V
C80 0.1uF 6.3V
XO_IN2 AB22
XO_IN AC22
XTALIN AM28
XTALOUT AK28
CLKTESTA K8
CLKTESTB L7
R31 1M 1%
Y2 27.000MHz_10PPM
C82 12pF 50V
C83 12pF 50V

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SHEET: Oland GPIO STRAP CF PLL

DATE: Tue Dec 17 08:14:16 2013 REV: 1.0

SHEET NUMBER: 6 OF 22

DOCUMENT NUMBER: 105-C748xx-00A

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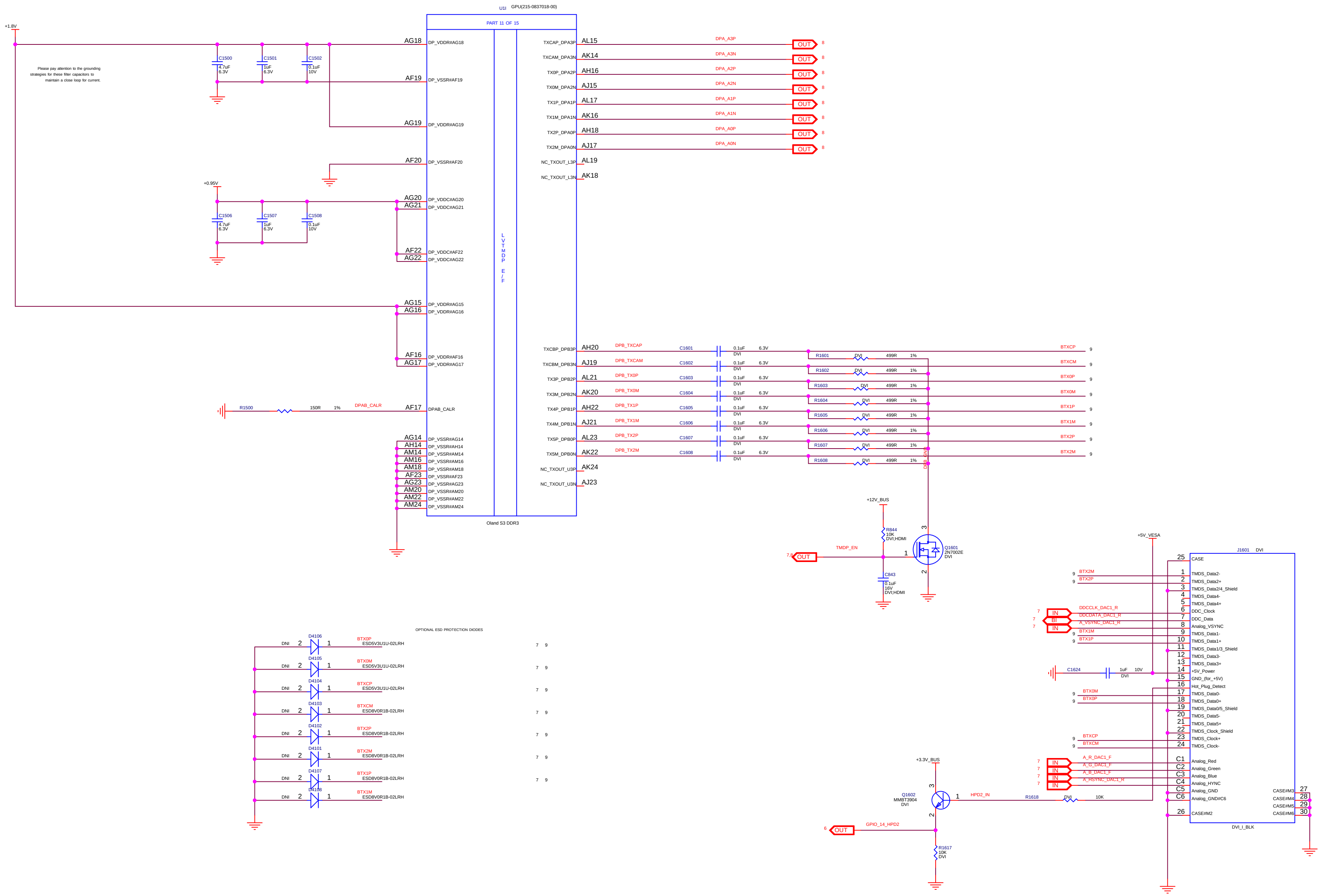
TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W


U1I GPU(215-0837018-00)
PART 11 OF 15
LVTMDP E/F
Oland S3 DDR3
+1.8V
+0.95V
Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.
C1500 4.7uF 6.3V
C1501 1uF 6.3V
C1502 0.1uF 10V
C1506 4.7uF 6.3V
C1507 1uF 6.3V
C1508 0.1uF 10V
AG18 DP_VDDR#AG18
AF19 DP_VSSR#AF19
AG19 DP_VDDR#AG19
AF20 DP_VSSR#AF20
AG20 DP_VDDC#AG20
AG21 DP_VDDC#AG21
AF22 DP_VDDC#AF22
AG22 DP_VDDC#AG22
AG15 DP_VDDR#AG15
AG16 DP_VDDR#AG16
AF16 DP_VDDR#AF16
AG17 DP_VDDR#AG17
AF17 DPAB_CALR
R1500 150R 1% DPAB_CALR
AG14 DP_VSSR#AG14
AH14 DP_VSSR#AH14
AM14 DP_VSSR#AM14
AM16 DP_VSSR#AM16
AM18 DP_VSSR#AM18
AF23 DP_VSSR#AF23
AG23 DP_VSSR#AG23
AM20 DP_VSSR#AM20
AM22 DP_VSSR#AM22
AM24 DP_VSSR#AM24
TXCAP_DPA3P AL15 DPA_A3P OUT 8
TXCAM_DPA3N AK14 DPA_A3N OUT 8
TX0P_DPA2P AH16 DPA_A2P OUT 8
TX0M_DPA2N AJ15 DPA_A2N OUT 8
TX1P_DPA1P AL17 DPA_A1P OUT 8
TX1M_DPA1N AK16 DPA_A1N OUT 8
TX2P_DPA0P AH18 DPA_A0P OUT 8
TX2M_DPA0N AJ17 DPA_A0N OUT 8
NC_TXOUT_L3P AL19
NC_TXOUT_L3N AK18
TXCBP_DPB3P AH20 DPB_TXCAP C1601 0.1uF 6.3V DVI R1601 DVI 499R 1% BTXCP 9
TXCBM_DPB3N AJ19 DPB_TXCAM C1602 0.1uF 6.3V DVI R1602 DVI 499R 1% BTXCM 9
TX3P_DPB2P AL21 DPB_TX0P C1603 0.1uF 6.3V DVI R1603 DVI 499R 1% BTX0P 9
TX3M_DPB2N AK20 DPB_TX0M C1604 0.1uF 6.3V DVI R1604 DVI 499R 1% BTX0M 9
TX4P_DPB1P AH22 DPB_TX1P C1605 0.1uF 6.3V DVI R1605 DVI 499R 1% BTX1P 9
TX4M_DPB1N AJ21 DPB_TX1M C1606 0.1uF 6.3V DVI R1606 DVI 499R 1% BTX1M 9
TX5P_DPB0P AL23 DPB_TX2P C1607 0.1uF 6.3V DVI R1607 DVI 499R 1% BTX2P 9
TX5M_DPB0N AK22 DPB_TX2M C1608 0.1uF 6.3V DVI R1608 DVI 499R 1% BTX2M 9
NC_TXOUT_U3P AK24
NC_TXOUT_U3N AJ23
+12V_BUS
R844 10K DVI;HDMI
TMDP_EN OUT 7,8
C843 0.1uF 16V DVI;HDMI
Q1601 2N7002E DVI
+5V_VESA
J1601 DVI
25 CASE
1 TMDS_Data2-
2 TMDS_Data2+
3 TMDS_Data2/4_Shield
4 TMDS_Data4-
5 TMDS_Data4+
6 DDC_Clock
7 DDC_Data
8 Analog_VSYNC
9 TMDS_Data1-
10 TMDS_Data1+
11 TMDS_Data1/3_Shield
12 TMDS_Data3-
13 TMDS_Data3+
14 +5V_Power
15 GND_(for_+5V)
16 Hot_Plug_Detect
17 TMDS_Data0-
18 TMDS_Data0+
19 TMDS_Data0/5_Shield
20 TMDS_Data5-
21 TMDS_Data5+
22 TMDS_Clock_Shield
23 TMDS_Clock+
24 TMDS_Clock-
C1 Analog_Red
C2 Analog_Green
C3 Analog_Blue
C4 Analog_HYNC
C5 Analog_GND
C6 Analog_GND#C6
26 CASE#M2
27 CASE#M3
28 CASE#M4
29 CASE#M5
30 CASE#M6
DVI_I_BLK
BTX2M BTX2P BTX1M BTX1P BTX0M BTX0P BTXCP BTXCM
DDCCLK_DAC1_R DDCDATA_DAC1_R A_VSYNC_DAC1_R
A_R_DAC1_F A_G_DAC1_F A_B_DAC1_F A_HSYNC_DAC1_R
IN BI IN IN IN IN IN
C1624 1uF 10V DVI
+3.3V_BUS
Q1602 MMBT3904 DVI
HPD2_IN
R1618 DVI 10K
GPIO_14_HPD2 OUT 6
R1617 10K DVI
OPTIONAL ESD PROTECTION DIODES
D4106 DNI BTX0P ESD5V3U1U-02LRH 7 9
D4105 DNI BTX0M ESD5V3U1U-02LRH 7 9
D4104 DNI BTXCP ESD5V3U1U-02LRH 7 9
D4103 DNI BTXCM ESD8V0R1B-02LRH 7 9
D4102 DNI BTX2P ESD8V0R1B-02LRH 7 9
D4101 DNI BTX2M ESD8V0R1B-02LRH 7 9
D4107 DNI BTX1P ESD8V0R1B-02LRH 7 9
D4108 DNI BTX1M ESD8V0R1B-02LRH

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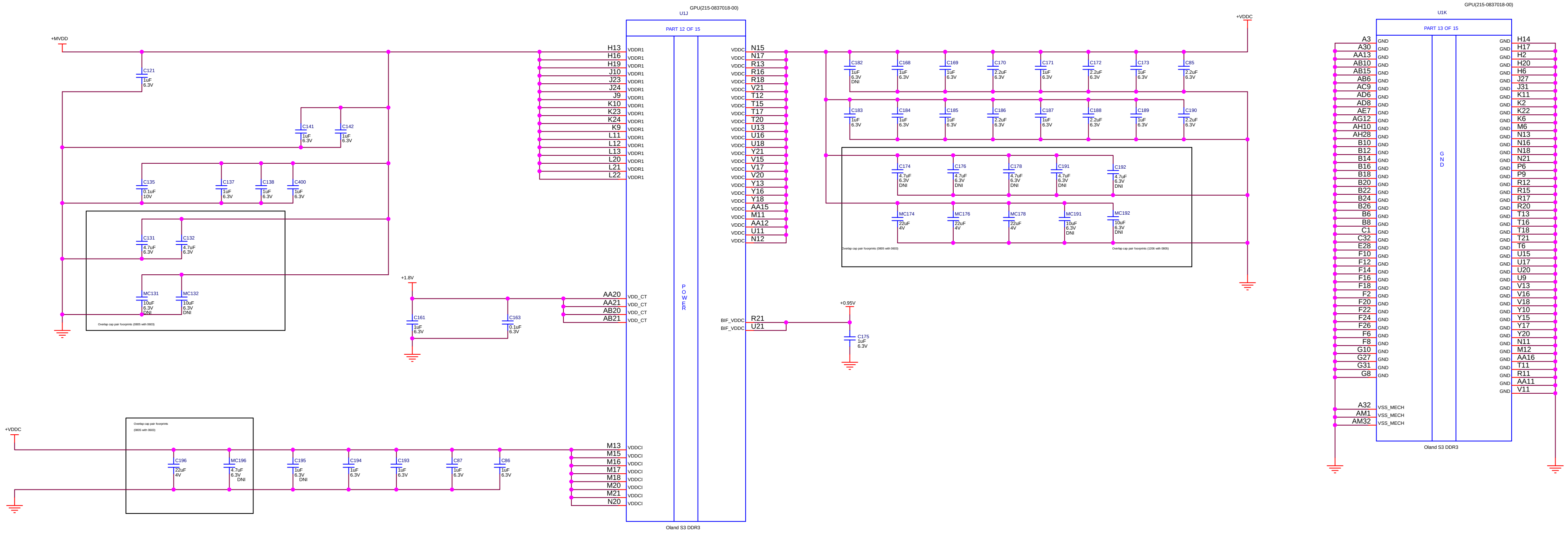
SHEET:	Oland sDVI-I CONN		
DATE:	Tue Dec 17 08:14:17 2013	REV:	1.0
SHEET NUMBER:	9	OF	22
DOCUMENT NUMBER:	105-C748xx-00A		
NOTES:	NOTE		

TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W

OLAND S3 Power & GND


+MVDD
C121 1uF 6.3V
C141 1uF 6.3V
C142 1uF 6.3V
C135 0.1uF 10V
C137 1uF 6.3V
C138 1uF 6.3V
C400 1uF 6.3V
C131 4.7uF 6.3V
C132 4.7uF 6.3V
MC131 10uF 6.3V DNI
MC132 10uF 6.3V DNI
Overlap cap pair foorprints (0805 with 0603)
+1.8V
C161 1uF 6.3V
C163 0.1uF 6.3V
GPU(215-0837018-00)
U1J
PART 12 OF 15
POWER
H13 VDDR1
H16 VDDR1
H19 VDDR1
J10 VDDR1
J23 VDDR1
J24 VDDR1
J9 VDDR1
K10 VDDR1
K23 VDDR1
K24 VDDR1
K9 VDDR1
L11 VDDR1
L12 VDDR1
L13 VDDR1
L20 VDDR1
L21 VDDR1
L22 VDDR1
AA20 VDD_CT
AA21 VDD_CT
AB20 VDD_CT
AB21 VDD_CT
M13 VDDCI
M15 VDDCI
M16 VDDCI
M17 VDDCI
M18 VDDCI
M20 VDDCI
M21 VDDCI
N20 VDDCI
VDDC N15
VDDC N17
VDDC R13
VDDC R16
VDDC R18
VDDC V21
VDDC T12
VDDC T15
VDDC T17
VDDC T20
VDDC U13
VDDC U16
VDDC U18
VDDC Y21
VDDC V15
VDDC V17
VDDC V20
VDDC Y13
VDDC Y16
VDDC Y18
VDDC AA15
VDDC M11
VDDC AA12
VDDC U11
VDDC N12
BIF_VDDC R21
BIF_VDDC U21
Oland S3 DDR3
+VDDC
C182 1uF 6.3V DNI
C168 1uF 6.3V
C169 1uF 6.3V
C170 2.2uF 6.3V
C171 1uF 6.3V
C172 2.2uF 6.3V
C173 1uF 6.3V
C85 2.2uF 6.3V
C183 1uF 6.3V
C184 1uF 6.3V
C185 1uF 6.3V
C186 2.2uF 6.3V
C187 1uF 6.3V
C188 2.2uF 6.3V
C189 1uF 6.3V
C190 2.2uF 6.3V
C174 4.7uF 6.3V DNI
C176 4.7uF 6.3V DNI
C178 4.7uF 6.3V DNI
C191 4.7uF 6.3V DNI
C192 4.7uF 6.3V DNI
MC174 22uF 4V
MC176 22uF 4V
MC178 22uF 4V
MC191 10uF 6.3V DNI
MC192 10uF 6.3V DNI
Overlap cap pair foorprints (0805 with 0603)
Overlap cap pair foorprints (1206 with 0805)
+0.95V
C175 1uF 6.3V
+VDDC
Overlap cap pair foorprints
(0805 with 0603)
C196 22uF 4V
MC196 4.7uF 6.3V DNI
C195 1uF 6.3V DNI
C194 1uF 6.3V
C193 1uF 6.3V
C87 1uF 6.3V
C86 1uF 6.3V
GPU(215-0837018-00)
U1K
PART 13 OF 15
GND
A3 GND
A30 GND
AA13 GND
AB10 GND
AB15 GND
AB6 GND
AC9 GND
AD6 GND
AD8 GND
AE7 GND
AG12 GND
AH10 GND
AH28 GND
B10 GND
B12 GND
B14 GND
B16 GND
B18 GND
B20 GND
B22 GND
B24 GND
B26 GND
B6 GND
B8 GND
C1 GND
C32 GND
E28 GND
F10 GND
F12 GND
F14 GND
F16 GND
F18 GND
F2 GND
F20 GND
F22 GND
F24 GND
F26 GND
F6 GND
F8 GND
G10 GND
G27 GND
G31 GND
G8 GND
A32 VSS_MECH
AM1 VSS_MECH
AM32 VSS_MECH
GND H14
GND H17
GND H2
GND H20
GND H6
GND J27
GND J31
GND K11
GND K2
GND K22
GND K6
GND M6
GND N13
GND N16
GND N18
GND N21
GND P6
GND P9
GND R12
GND R15
GND R17
GND R20
GND T13
GND T16
GND T18
GND T21
GND T6
GND U15
GND U17
GND U20
GND U9
GND V13
GND V16
GND V18
GND Y10
GND Y15
GND Y17
GND Y20
GND N11
GND M12
GND AA16
GND T11
GND R11
GND AA11
GND V11
Oland S3 DDR3

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SHEET: Oland Power&GND

DATE: Tue Dec 17 08:14:17 2013

REV: 1.0

SHEET NUMBER: 10 OF 22

DOCUMENT NUMBER: 105-C748xx-00A

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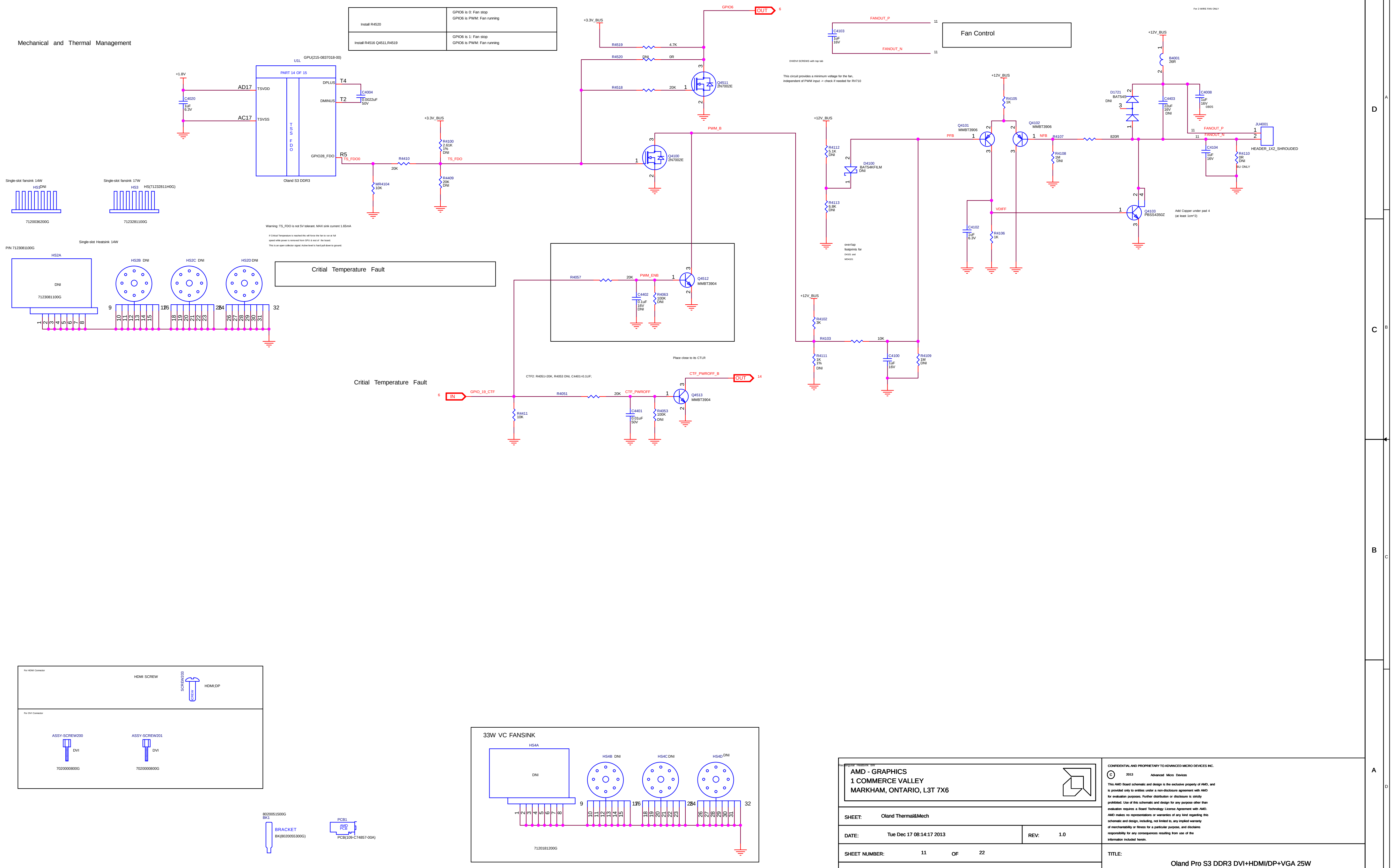
TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W

Mechanical and Thermal Management

	GPIO6
Install R4520	GPIO6 is 0: Fan stop GPIO6 is PWM: Fan running
Install R4516 Q4511,R4519	GPIO6 is 1: Fan stop GPIO6 is PWM: Fan running


U1L
GPU(215-0837018-00)
PART 14 OF 15
+1.8V
AD17
AC17
TSVDD
TSVSS
C4020
1uF
6.3V
DPLUS
DMINUS
T4
T2
C4004
0.0022uF
50V
GPIO28_FDO
R5
TS_FDO
Oland S3 DDR3
TS_FDO0
R4410
20K
MR4104
10K
+3.3V_BUS
R4100
2.61K
1%
DNI
R4409
20K
DNI
+3.3V_BUS
R4519
4.7K
R4520
DNI
0R
R4518
20K
GPIO6
OUT
6
Q4511
2N7002E
Q4100
2N7002E
PWM_B
FANOUT_P
FANOUT_N
11
C4103
1uF
16V
Fan Control
For 2-WIRE FAN ONLY
+12V_BUS
B4001
26R
D1721
BAT54S
DNI
C4403
22uF
16V
DNI
C4008
1uF
16V
0805
JU4001
HEADER_1X2_SHROUDED
C4104
1uF
16V
R4110
0R
DNI
BU ONLY
R4105
1K
Q4101
MMBT3906
Q4102
MMBT3906
PFB
NFB
R4107
820R
R4108
1M
DNI
R4112
5.1K
DNI
D4100
BAT54KFILM
DNI
R4113
6.8K
DNI
C4102
1uF
6.3V
R4106
1K
VDIFF
Q4103
PBSS4350Z
Add Copper under pad 4
(at least 1cm^2)
overlap
footprints for
D4101 and
MD4101
Single-slot fansink 14W
HS1 DNI
7120036200G
Single-slot fansink 17W
HS3
HS(7123281 1H0G)
7123281100G
Single-slot Heatsink 14W
P/N 7123081100G
HS2A
DNI
7123081100G
HS2B DNI
HS2C DNI
HS2D DNI
Critial Temperature Fault
R4057
20K
PWM_ENB
C4402
0.1uF
16V
DNI
R4063
100K
DNI
Q4512
MMBT3904
+12V_BUS
R4102
3K
R4103
10K
R4111
1K
1%
DNI
C4100
1uF
16V
R4109
1M
DNI
Place close to its CTLR
CTF2: R4051=20K, R4053 DNI, C4401=0.1UF;
Critial Temperature Fault
GPIO_19_CTF
IN
R4051
20K
CTF_PWROFF
CTF_PWROFF_B
OUT
14
R4411
10K
C4401
0.01uF
50V
R4053
100K
DNI
Q4513
MMBT3904
For HDMI Connector
HDMI SCREW
SCREW203
HDMI;DP
For DVI Connector
ASSY-SCREW200
ASSY-SCREW201
DVI
7020000800G
8020051500G
BK1
BRACKET
BK(8020055300G)
PCB1
AMD PCB
PCB(109-C74857-00A)
33W VC FANSINK
HS4A
DNI
7120181200G
HS4B DNI
HS4C DNI
HS4D DNI
Rectangular Heatsink 8W

Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board.
This is an open collector signal. Active level is hard pull down to ground.

DVI/DVI SCREWS with top tab

This circuit provides a minimum voltage for the fan,
independent of PWM input -> check if needed for RV710

AMD - GRAPHICS
1 COMMERCE VALLEY
MARKHAM, ONTARIO, L3T 7X6

SHEET: Oland Thermal&Mech

DATE: Tue Dec 17 08:14:17 2013

REV: 1.0

SHEET NUMBER: 11 OF 22

DOCUMENT NUMBER: 105-C748xx-00A

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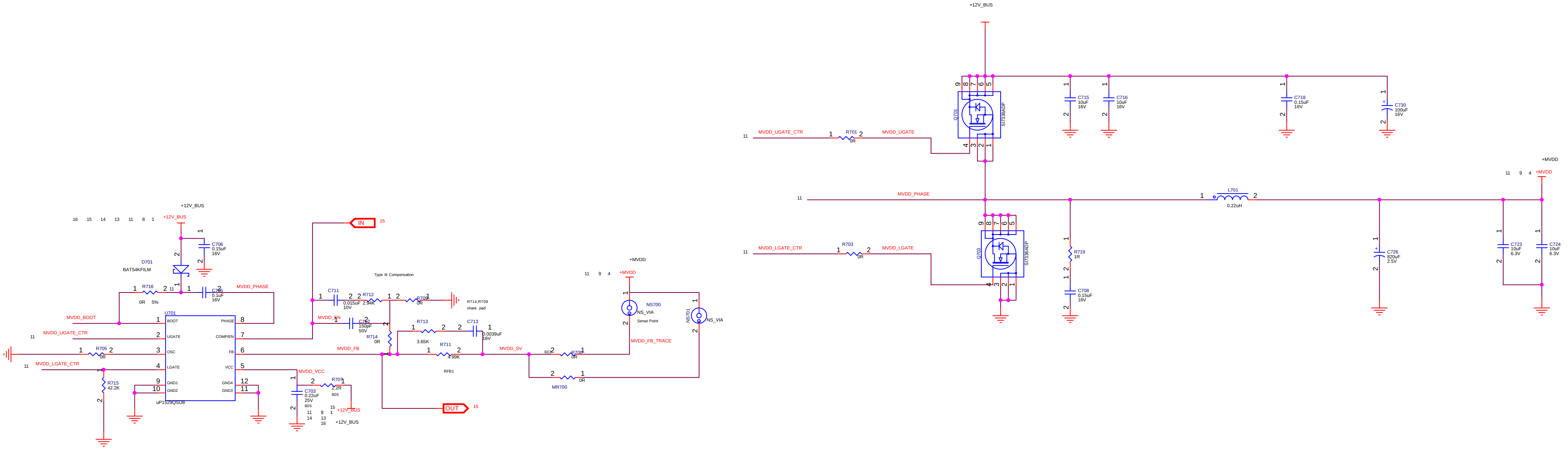
TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W


+12V_BUS
16 15 14 13 11 8 1
+12V_BUS
C706
0.15uF
16V
D701
BAT54KFILM
R716
0R 5%
C705
0.1uF
16V
MVDD_PHASE
MVDD_BOOT
11
MVDD_UGATE_CTR
R705
0R
11
MVDD_LGATE_CTR
R715
42.2K
U701
BOOT
UGATE
OSC
LGATE
GND1
GND2
PHASE
COMP/EN
FB
VCC
GND4
GND3
uP1529QSU8
MVDD_VCC
C703
0.22uF
25V
805
R707
2.2R
805
15
11 8 1
14 13
16
+12V_BUS
+12V_BUS
IN
15
Type III Compensation
C711
0.015uF
10V
R712
2.94K
R709
0R
R714,R709
share pad
MVDD_EN
C712
150pF
50V
R714
0R
R713
3.65K
C713
0.0039uF
16V
MVDD_FB
R711
4.99K
RFB1
MVDD_SV
OUT
15
603
R700
0R
MR700
0R
+MVDD
11 9 4
+MVDD
NS700
NS_VIA
Sense Point
NS701
NS_VIA
MVDD_FB_TRACE
+12V_BUS
Q701
SI7336ADP
11
MVDD_UGATE_CTR
R701
0R
MVDD_UGATE
C715
10uF
16V
C716
10uF
16V
C718
0.15uF
16V
C730
100uF
16V
11
MVDD_PHASE
L701
0.22uH
+MVDD
11 9 4
+MVDD
11
MVDD_LGATE_CTR
R703
0R
MVDD_LGATE
Q703
SI7336ADP
R719
1R
C708
0.15uF
16V
C726
820uF
2.5V
C723
10uF
6.3V
C724
10uF
6.3V

<ADDR1>
<ADDR2>
<ADDR3>

SHEET: SHEET TITLE

DATE: <CON_LAST_MODIFIED>

REV: <REV>

SHEET NUMBER: 11 OF 20

DOCUMENT NUMBER: <SCHEMATIC_NUMBER>

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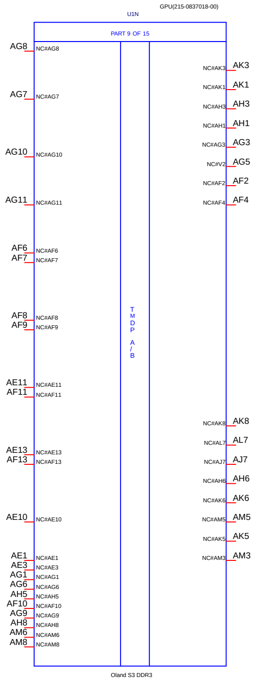
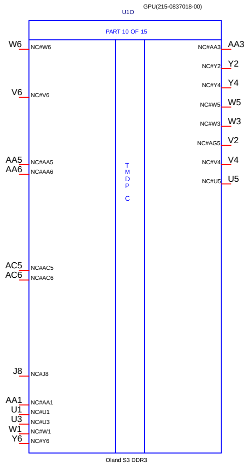
TITLE:

<TITLE>


GPU(215-0837018-00)
U1N
PART 9 OF 15
AG8 NC#AG8
AG7 NC#AG7
AG10 NC#AG10
AG11 NC#AG11
AF6 NC#AF6
AF7 NC#AF7
AF8 NC#AF8
AF9 NC#AF9
AE11 NC#AE11
AF11 NC#AF11
AE13 NC#AE13
AF13 NC#AF13
AE10 NC#AE10
AE1 NC#AE1
AE3 NC#AE3
AG1 NC#AG1
AG6 NC#AG6
AH5 NC#AH5
AF10 NC#AF10
AG9 NC#AG9
AH8 NC#AH8
AM6 NC#AM6
AM8 NC#AM8
TMDP A/B
NC#AK3 AK3
NC#AK1 AK1
NC#AH3 AH3
NC#AH1 AH1
NC#AG3 AG3
NC#V2 AG5
NC#AF2 AF2
NC#AF4 AF4
NC#AK8 AK8
NC#AL7 AL7
NC#AJ7 AJ7
NC#AH6 AH6
NC#AK6 AK6
NC#AM5 AM5
NC#AK5 AK5
NC#AM3 AM3
Oland S3 DDR3


GPU(215-0837018-00)
U1O
PART 10 OF 15
W6 NC#W6
V6 NC#V6
AA5 NC#AA5
AA6 NC#AA6
AC5 NC#AC5
AC6 NC#AC6
J8 NC#J8
AA1 NC#AA1
U1 NC#U1
U3 NC#U3
W1 NC#W1
Y6 NC#Y6
TMDP C
NC#AA3 AA3
NC#Y2 Y2
NC#Y4 Y4
NC#W5 W5
NC#W3 W3
NC#AG5 V2
NC#V4 V4
NC#U5 U5
Oland S3 DDR3

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SHEET: Oland Unused Modules

DATE: Tue Dec 17 08:14:18 2013

REV: 1.0

SHEET NUMBER: 13 OF 22

DOCUMENT NUMBER: 105-C748xx-00A

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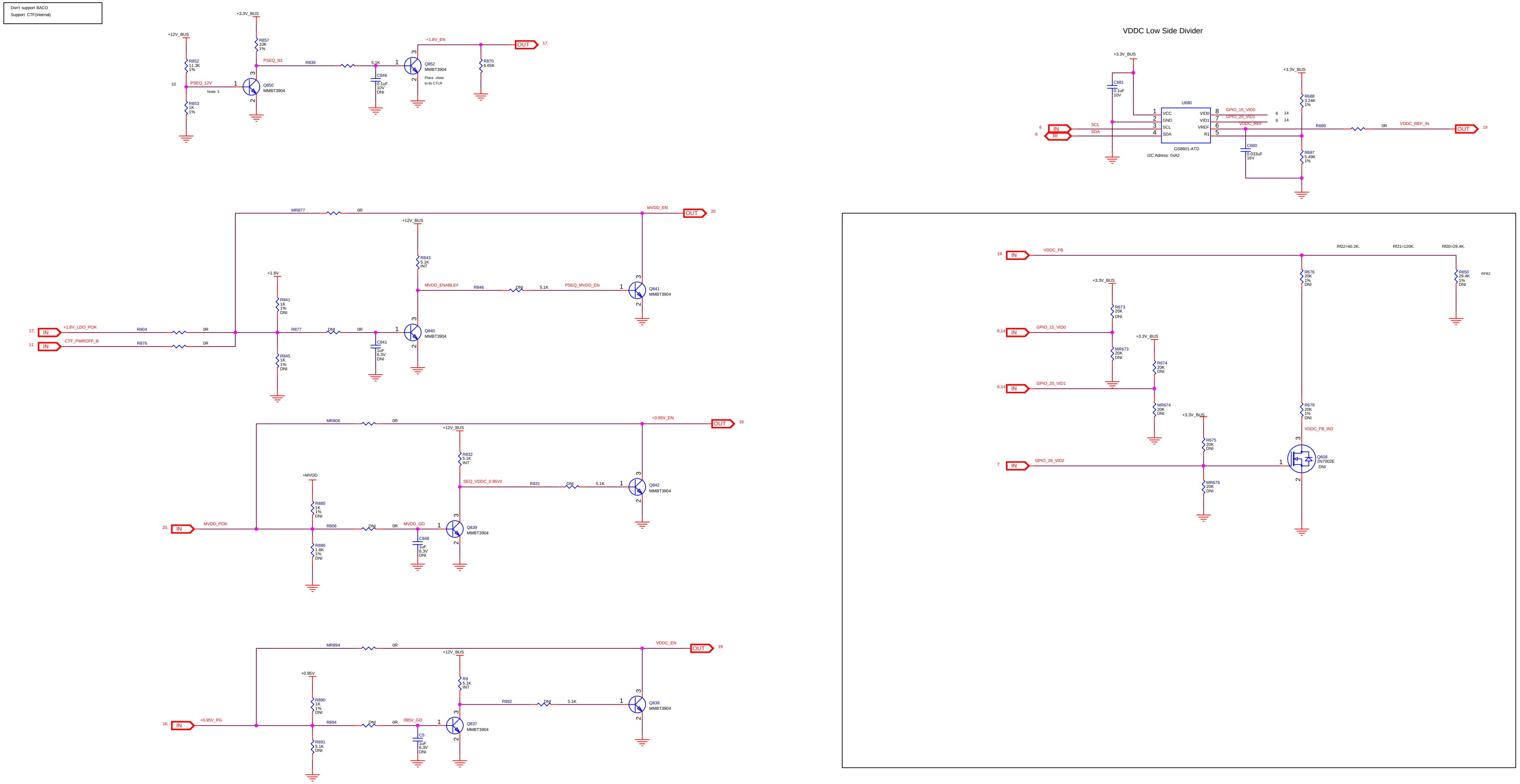
TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W

Power Management - Power Gating and Dynamic Voltage Control

POWER SEQUENCE
+1.8V-2.8ms->MVDD-3.4ms->0.95V-4.3ms->VDDC

0.95V must ramp up before VDDC

Don't support BACO
Support CTF(Internal)


+12V_BUS
R852
11.3K
1%
10
PSEQ_12V
Node 3
R853
1K
1%
+3.3V_BUS
R857
10K
1%
PSEQ_N1
Q850
MMBT3904
R839
5.1K
C846
0.1uF
10V
DNI
Q852
MMBT3904
Place close
to its CTLR
+1.8V_EN
R870
6.65K
OUT
17,
VDDC Low Side Divider
+3.3V_BUS
C681
0.1uF
10V
U680
VCC
GND
SCL
SDA
VID0
VID1
VREF
R1
GS8601-ATD
I2C Adress: 0xA2
IN
BI
SCL
SDA
6
GPIO_15_VID0
GPIO_20_VID1
6 14
VDDC_REF
C680
0.033uF
16V
R688
3.24K
1%
R687
5.49K
1%
R689
0R
VDDC_REF_IN
OUT
19
MR877
0R
MVDD_EN
OUT
20
+12V_BUS
R843
5.1K
INT
MVDD_ENABLE#
R846
DNI
5.1K
PSEQ_MVDD_EN
Q841
MMBT3904
+1.8V
R841
1K
1%
DNI
17,
IN
+1.8V_LDO_POK
R804
0R
11
CTF_PWROFF_B
R876
R877
C841
1uF
6.3V
DNI
Q840
MMBT3904
R845
1K
1%
DNI
MR806
+0.95V_EN
16
R832
5.1K
INT
SEQ_VDDC_0.95V#
R831
Q842
+MVDD
R885
20,
MVDD_POK
R806
MVDD_GD
C848
Q839
R886
1.6K
MR894
VDDC_EN
+0.95V
R890
R9
R892
Q838
16,
+0.95V_PG
R894
095V_GD
C5
Q837
R891
5.1K
VDDC_FB
Rf22=40.2K.
Rf21=120K.
Rf20=29.4K.
R676
20K
1%
DNI
R650
29.4K
RFB2
R673
6,14
MR673
R674
MR674
R675
MR675
7
GPIO_29_VID2
R679
VDDC_FB_IN3
Q608
2N7002E
DNI

AMD - GRAPHICS
1 COMMERCE VALLEY
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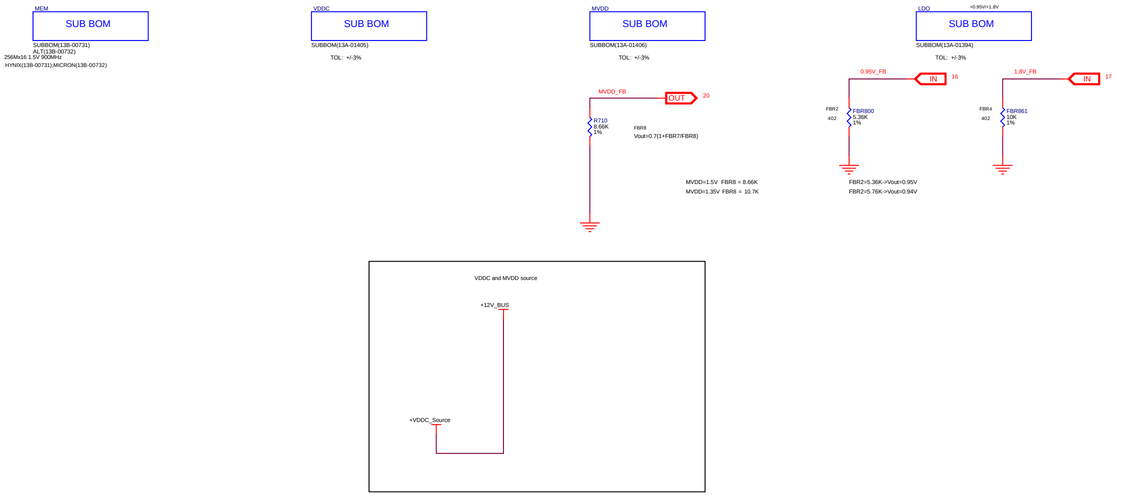
SHEET: PWR SEQ
DATE: Tue Dec 17 08:14:18 2013
REV: 1.0
SHEET NUMBER: 14 OF 22
DOCUMENT NUMBER: 105-C748xx-00A
TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W


MEM
SUB BOM
SUBBOM(13B-00731)
ALT(13B-00732)
256Mx16 1.5V 900MHz
HYNIX(13B-00731);MICRON(13B-00732)
VDDC
SUB BOM
SUBBOM(13A-01405)
TOL: +/-3%
MVDD
SUB BOM
SUBBOM(13A-01406)
TOL: +/-3%
MVDD_FB
OUT
20
R710
8.66K
1%
FBR8
Vout=0.7(1+FBR7/FBR8)
MVDD=1.5V FBR8 = 8.66K
MVDD=1.35V FBR8 = 10.7K
LDO
+0.95V/+1.8V
SUB BOM
SUBBOM(13A-01394)
TOL: +/-3%
0.95V_FB
IN
16
FBR2
402
FBR800
5.36K
1%
1.8V_FB
IN
17
FBR4
402
FBR861
10K
1%
FBR2=5.36K->Vout=0.95V
FBR2=5.76K->Vout=0.94V
VDDC and MVDD source
+12V_BUS
+VDDC_Source

AMD - GRAPHICS
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SHEET: Sub BOM

DATE: Tue Dec 17 08:14:18 2013

REV: 1.0

SHEET NUMBER: 15 OF 22

DOCUMENT NUMBER: 105-C748xx-00A

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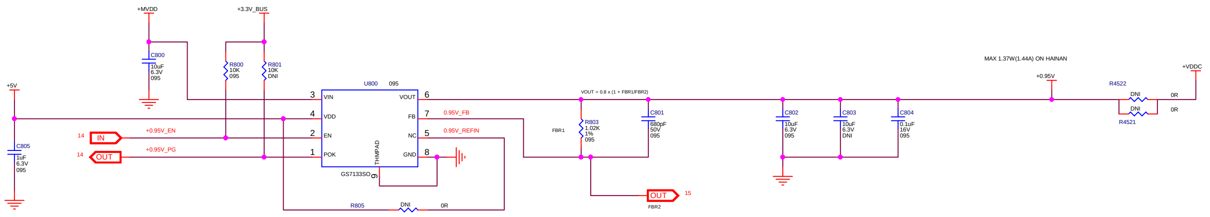
TITLE: Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W

Linear Regulators

LDO #1: Vin = +1.5V +/-2% Vout = +0.95V +/- 2%; Iout = 1.44A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling


+MVDD
+3.3V_BUS
C800
10uF
6.3V
095
R800
10K
095
R801
10K
DNI
+5V
U800 095
3 VIN
4 VDD
2 EN
1 POK
VOUT 6
FB 7
NC 5
GND 8
THMPAD
GS7133SO
9
14 IN
14 OUT
+0.95V_EN
+0.95V_PG
0.95V_FB
0.95V_REFIN
C805
1uF
6.3V
095
R805 DNI 0R
VOUT = 0.8 x (1 + FBR1/FBR2)
FBR1
R803
1.02K
1%
095
C801
680pF
50V
095
OUT 15
FBR2
C802
10uF
6.3V
095
C803
10uF
6.3V
DNI
C804
0.1uF
16V
095
MAX 1.37W(1.44A) ON HAINAN
+0.95V
R4522
DNI 0R
DNI 0R
R4521
+VDDC

$CDS_IMAGE|clipboard_3.jpg|4028|3181

AMD - GRAPHICS
1 COMMERCE VALLEY
MARKHAM, ONTARIO, L3T 7X6

SHEET: 0.95V

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REV: 1.0

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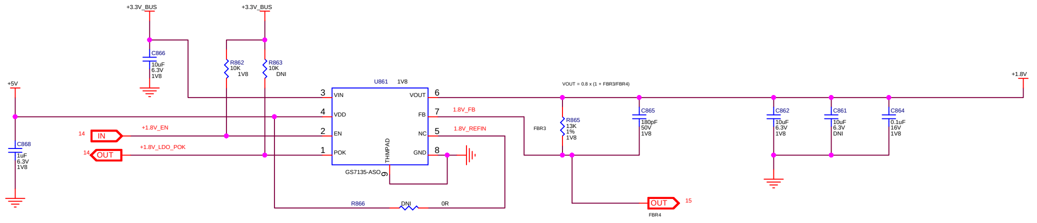
TITLE:

Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W

Linear Regulators

LDO #2: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



+3.3V_BUS
+3.3V_BUS
C866
10uF
6.3V
1V8
R862
10K
1V8
R863
10K
DNI
+5V
U861
1V8
3 VIN
4 VDD
2 EN
1 POK
VOUT 6
FB 7
NC 5
GND 8
THMPAD
9
GS7135-ASO
1.8V_FB
1.8V_REFIN
14 IN
+1.8V_EN
14 OUT
+1.8V_LDO_POK
C868
1uF
6.3V
1V8
R866
DNI
0R
VOUT = 0.8 x (1 + FBR3/FBR4)
FBR3
R865
13K
1%
1V8
C865
180pF
50V
1V8
OUT 15
FBR4
C862
10uF
6.3V
1V8
C861
10uF
6.3V
DNI
C864
0.1uF
16V
1V8
+1.8V

$CDS_IMAGE(clipboard_2.jpg|4028|3181

AMD - GRAPHICS
1 COMMERCE VALLEY
MARKHAM, ONTARIO, L3T 7X6

SHEET: 1.8V

DATE: Tue Dec 17 08:14:19 2013

REV: 1.0

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DOCUMENT NUMBER: 105-C748xx-00A

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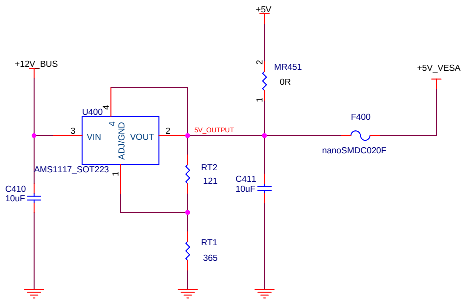
TITLE:
Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W

+5V Power


+12V_BUS
U400
4
3
VIN
4
ADJ/GND
VOUT
2
AMS1117_SOT223
1
5V_OUTPUT
C410
10uF
RT2
121
RT1
365
+5V
2
MR451
0R
1
C411
10uF
F400
nanoSMDC020F
+5V_VESA

Vout=1.25V* [1+(RT1/RT2)]

AMD - GRAPHICS
1 COMMERCE VALLEY
MARKHAM, ONTARIO, L3T 7X6

SHEET: 5V

DATE: Tue Dec 17 08:14:19 2013 REV: 1.0

SHEET NUMBER: 18 OF 22

DOCUMENT NUMBER: 105-C748xx-00A

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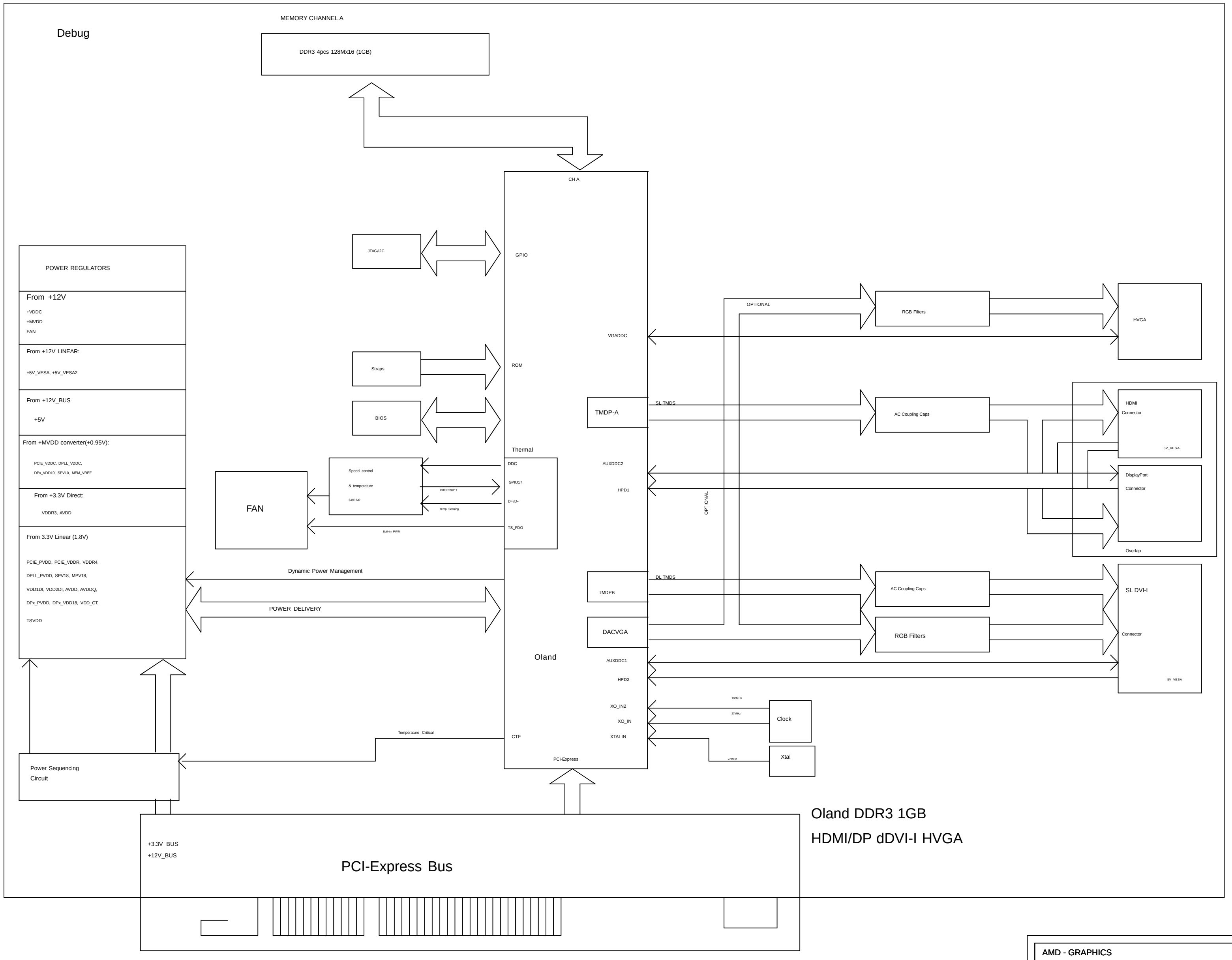
TITLE:

Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W


Debug
MEMORY CHANNEL A
DDR3 4pcs 128Mx16 (1GB)
CH A
JTAG/I2C
GPIO
Straps
ROM
BIOS
Thermal
DDC
GPIO17
D+/D-
TS_FDO
Speed control
& temperature
sense
INTERRUPT
Temp. Sensing
Built-in PWM
FAN
POWER REGULATORS
From +12V
+VDDC
+MVDD
FAN
From +12V LINEAR:
+5V_VESA, +5V_VESA2
From +12V_BUS
+5V
From +MVDD converter(+0.95V):
PCIE_VDDC, DPLL_VDDC,
DPx_VDD10, SPV10, MEM_VREF
From +3.3V Direct:
VDDR3, AVDD
From 3.3V Linear (1.8V)
PCIE_PVDD, PCIE_VDDR, VDDR4,
DPLL_PVDD, SPV18, MPV18,
VDD1DI, VDD2DI, AVDD, AVDDQ,
DPx_PVDD, DPx_VDD18, VDD_CT,
TSVDD
Dynamic Power Management
POWER DELIVERY
Power Sequencing
Circuit
Temperature Critical
CTF
Oland
PCI-Express
VGADDC
TMDP-A
SL TMDS
AUXDDC2
HPD1
OPTIONAL
TMDPB
DL TMDS
DACVGA
AUXDDC1
HPD2
XO_IN2
XO_IN
XTALIN
100MHz
27MHz
27MHz
Clock
Xtal
OPTIONAL
RGB Filters
HVGA
AC Coupling Caps
HDMI
Connector
5V_VESA
DisplayPort
Connector
Overlap
AC Coupling Caps
RGB Filters
SL DVI-I
Connector
5V_VESA
+3.3V_BUS
+12V_BUS
PCI-Express Bus

Oland DDR3 1GB

HDMI/DP dDVI-I HVGA

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SHEET:	Diagram
DATE:	Tue Dec 17 08:14:19 2013
REV:	1.0
SHEET NUMBER:	21 OF 22
DOCUMENT NUMBER:	105-C748xx-00A
TITLE:	Oland Pro S3 DDR3 DVI+HDMI/DP+VGA 25W

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SHEET NUMBER: 22 OF 22

REV: 1.0

REVISION HISTORY

ENGINEER: Tony Yang

NOTES: NOTE

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SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
1.00	00A	10/15/13	1. Initial release