PG210 B00

GP107 128b GDDR5, 75W , PCB 5.7"
DVI-D_DL (DP + DP) + HDMI (DP) + DP

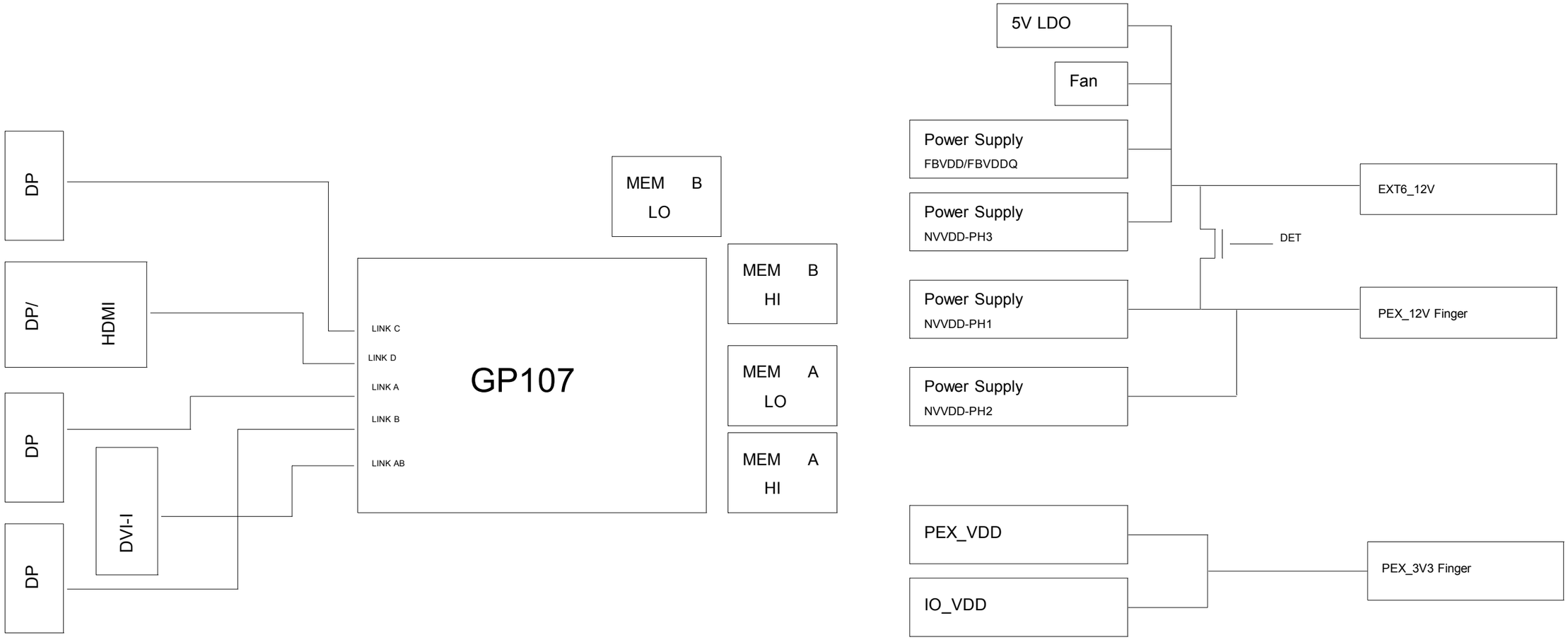
TABLE OF CONTENTS

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Table of Contents

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	1 OF 27
BOM REV	A	DATE	dd-mon-year

Block Diagram

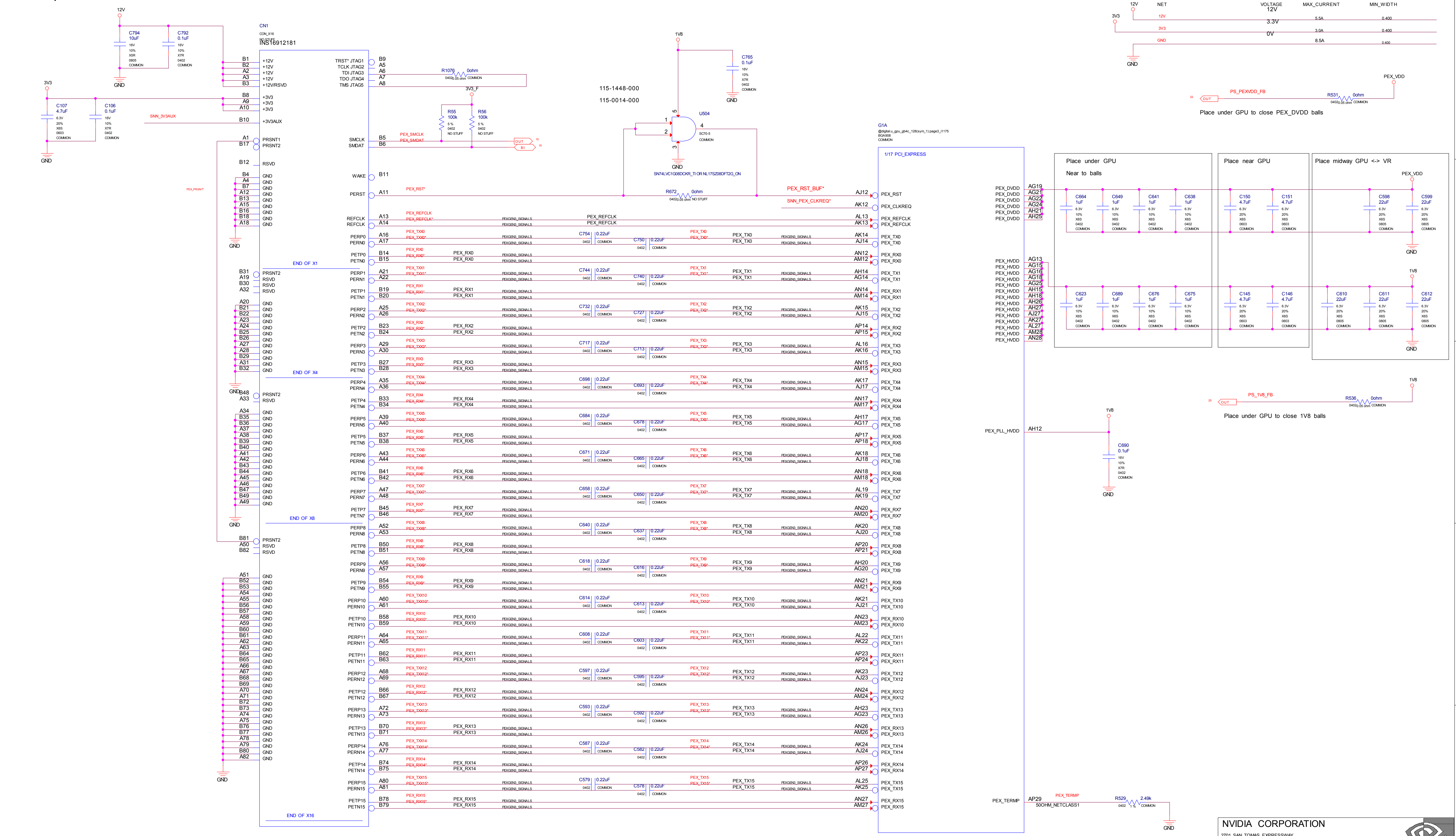


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Block Diagram

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	2 OF 27
BOM REV	A	DATE	18-DEC-2015

PCI Express

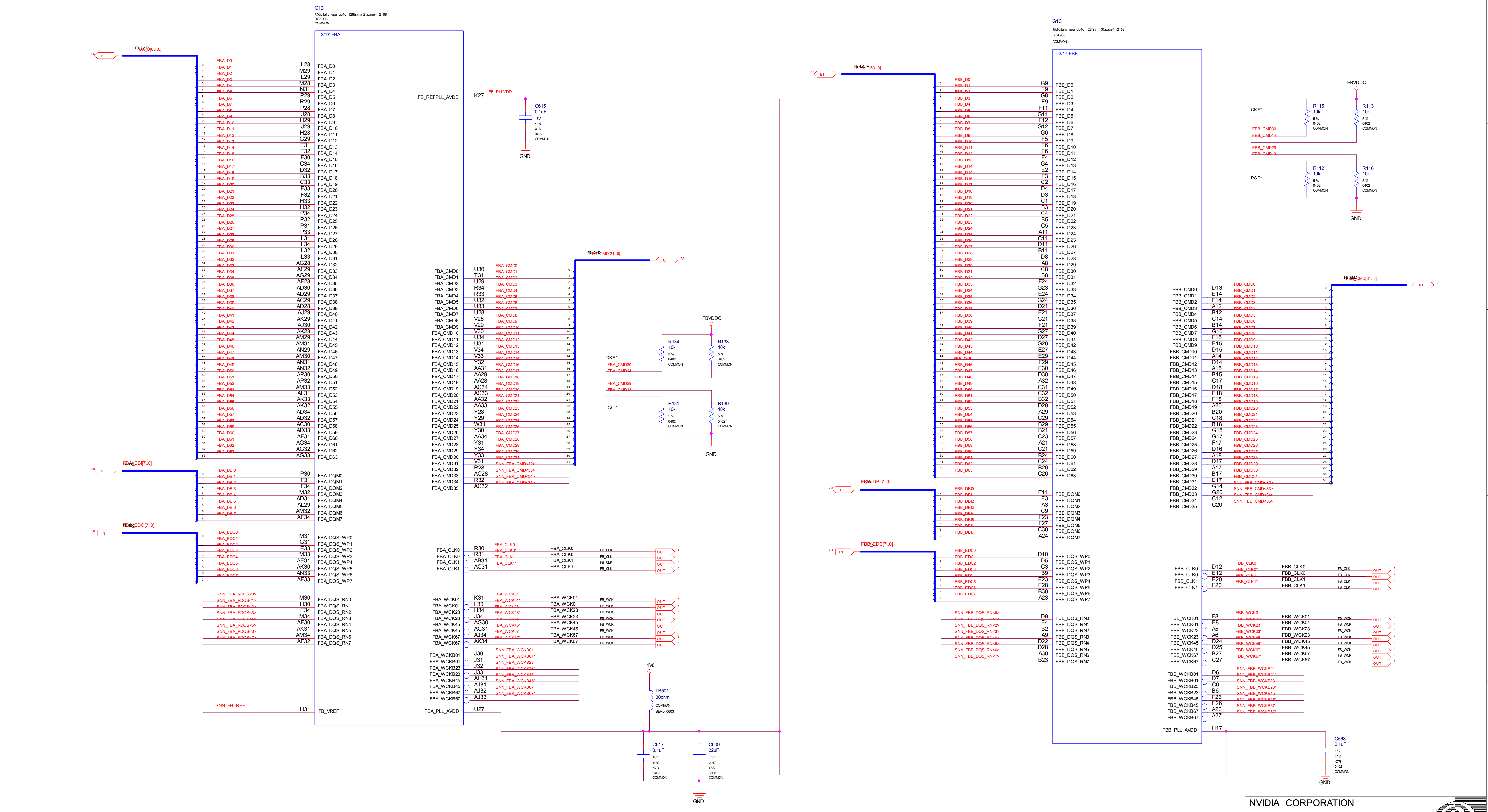


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI Express

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	3 OF 27
BOM REV	A	DATE	18-DEC-2015

MEMORY: GPU Partition A/B



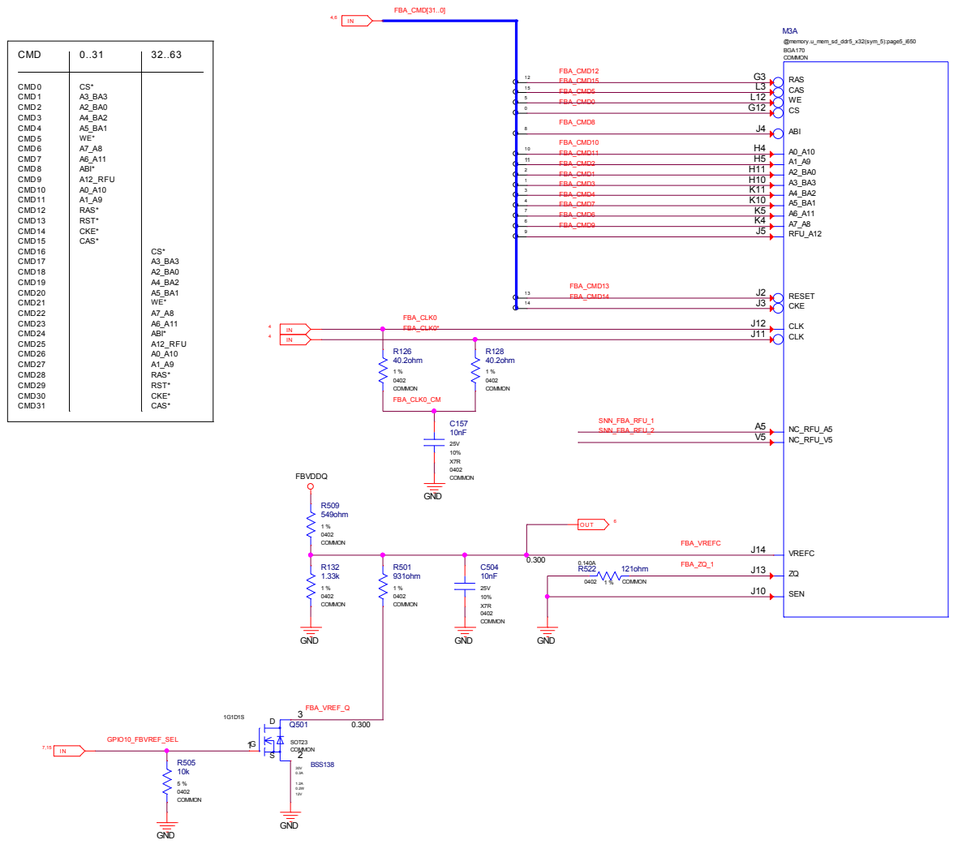
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: GPU Partition A/B

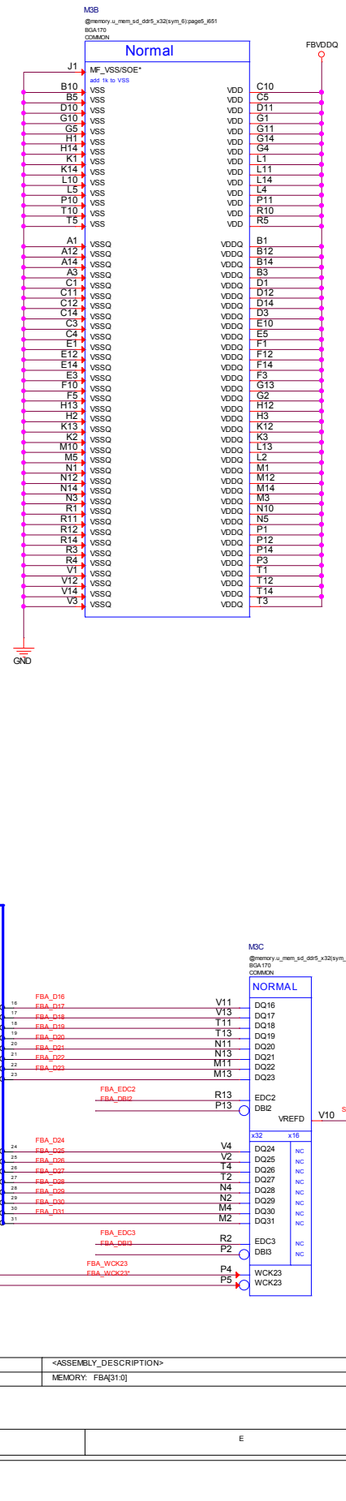
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

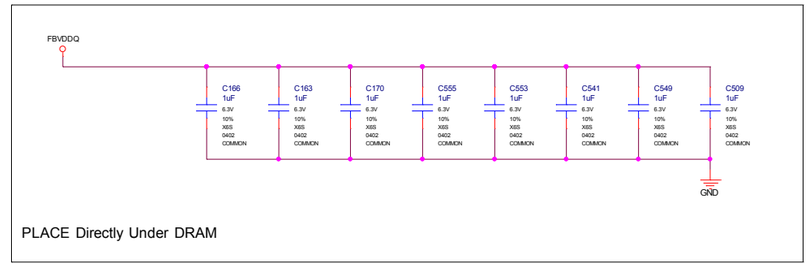
NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	4 OF 27
BOM REV	A	DATE	18-DEC-2015

MEMORY: FBA Partition 31..0

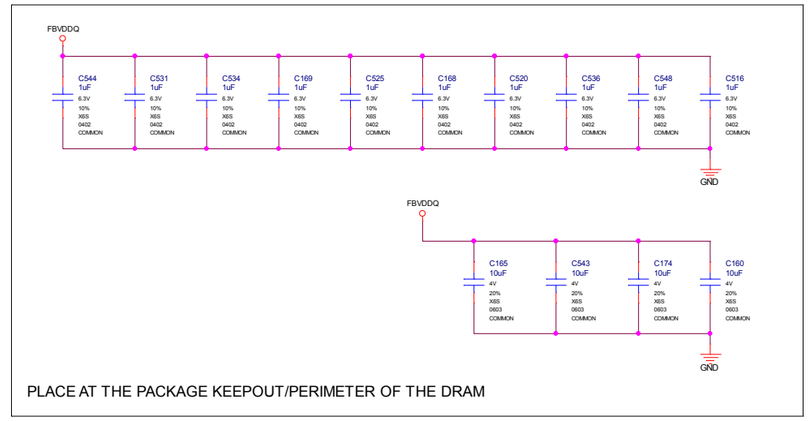
CMD	0..31	32..63
CMD 0	CS*	
CMD 1	A3_BA3	
CMD 2	A2_BA0	
CMD 3	A4_BA2	
CMD 4	A5_BA1	
CMD 5	WE*	
CMD 6	A7_A8	
CMD 7	A6_A11	
CMD 8	ABI*	
CMD 9	A12_RFU	
CMD 10	A0_A10	
CMD 11	A1_A9	
CMD 12	RAS*	
CMD 13	RST*	
CMD 14	CKE*	
CMD 15	CAS*	
CMD 16		CS*
CMD 17		A3_BA3
CMD 18		A2_BA0
CMD 19		A4_BA2
CMD 20		A5_BA1
CMD 21		WE*
CMD 22		A7_A8
CMD 23		A6_A11
CMD 24		ABI*
CMD 25		A12_RFU
CMD 26		A0_A10
CMD 27		A1_A9
CMD 28		RAS*
CMD 29		RST*
CMD 30		CKE*
CMD 31		CAS*



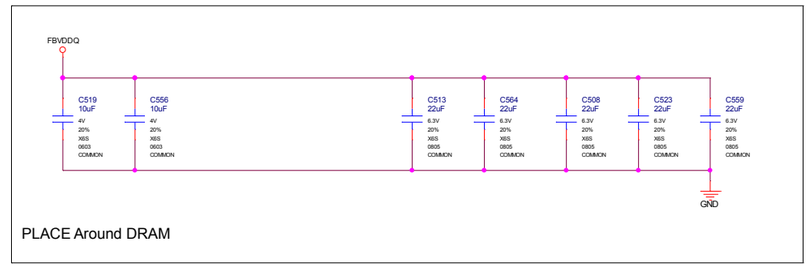




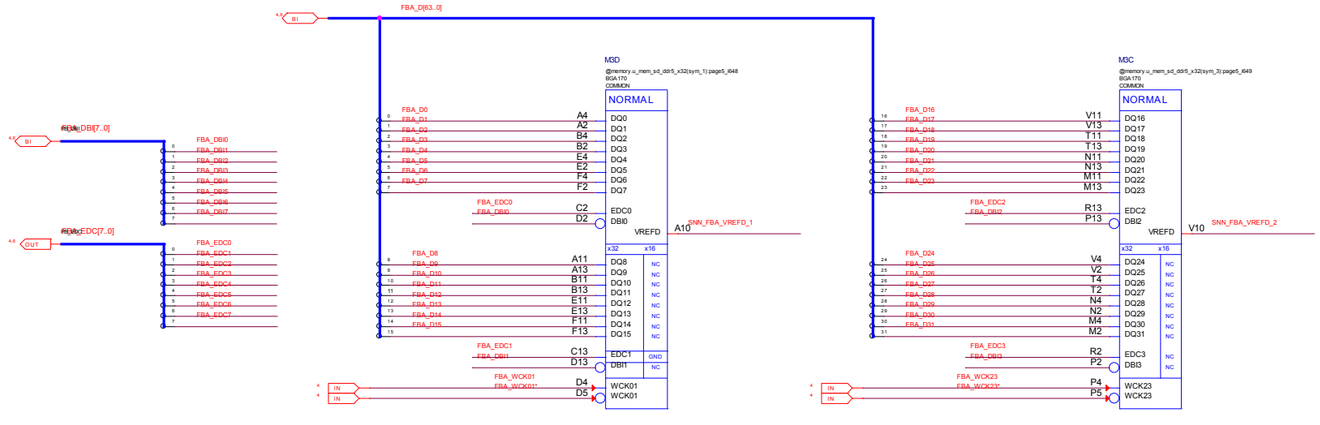
PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM



PLACE Around DRAM



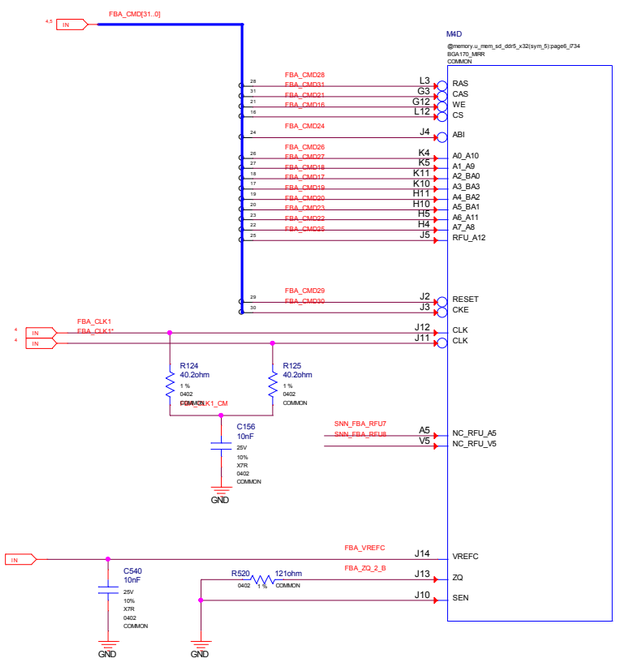
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBA[31:0]

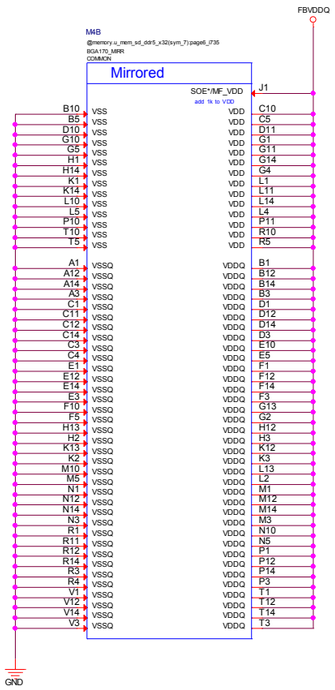
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

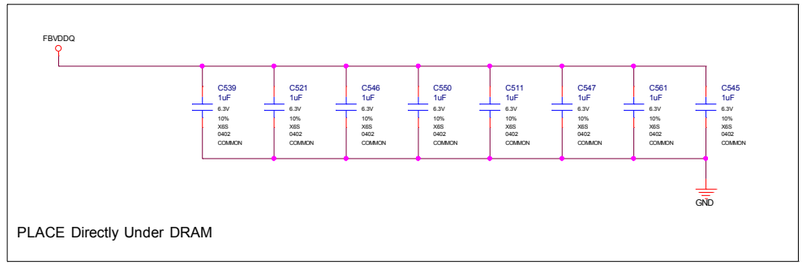
NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	5 OF 27
BOM REV	A	DATE	18-DEC-2015

MEMORY: FBA Partition 63..32

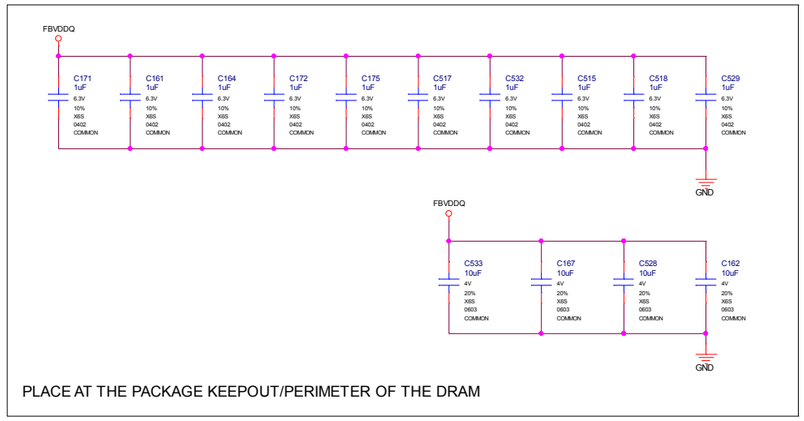
CMD	0..31	32..63
CMD 0	CS*	
CMD 1	A3_BA3	
CMD 2	A2_BA0	
CMD 3	A4_BA2	
CMD 4	A5_BA1	
CMD 5	WE*	
CMD 6	A7_A8	
CMD 7	A6_A11	
CMD 8	ABI*	
CMD 9	A12_RFU	
CMD 10	A0_A10	
CMD 11	A1_A9	
CMD 12	RAS*	
CMD 13	RST*	
CMD 14	CKE*	
CMD 15	CAS*	
CMD 16		CS*
CMD 17		A3_BA3
CMD 18		A2_BA0
CMD 19		A4_BA2
CMD 20		A5_BA1
CMD 21		WE*
CMD 22		A7_A8
CMD 23		A6_A11
CMD 24		ABI*
CMD 25		A12_RFU
CMD 26		A0_A10
CMD 27		A1_A9
CMD 28		RAS*
CMD 29		RST*
CMD 30		CKE*
CMD 31		CAS*



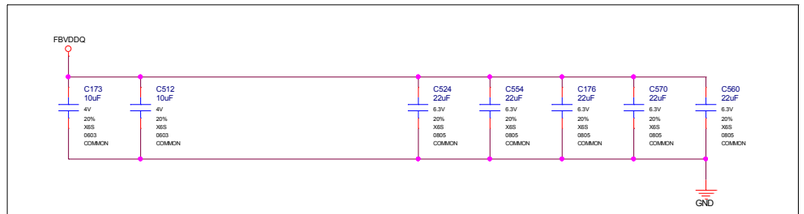




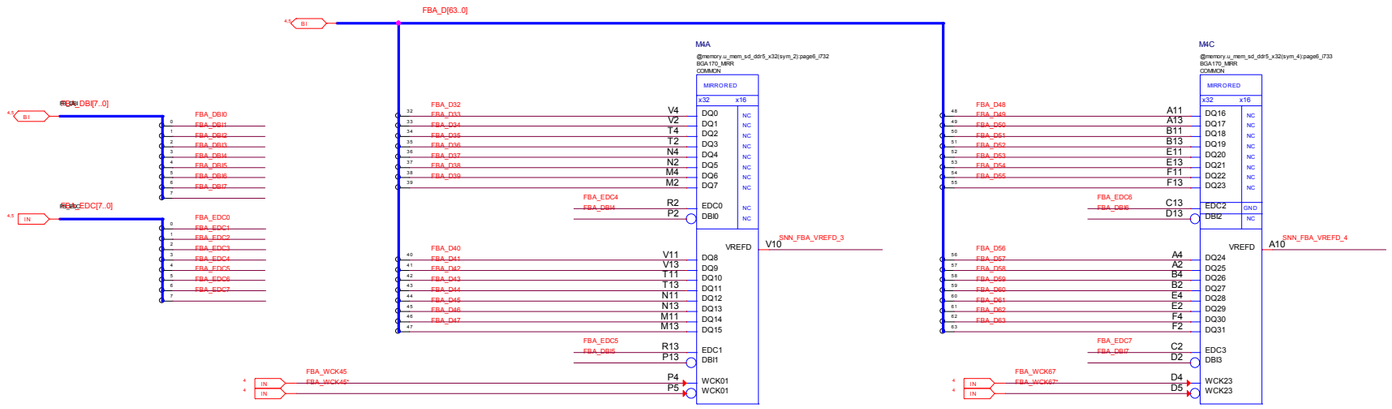
PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM



PLACE Around DRAM



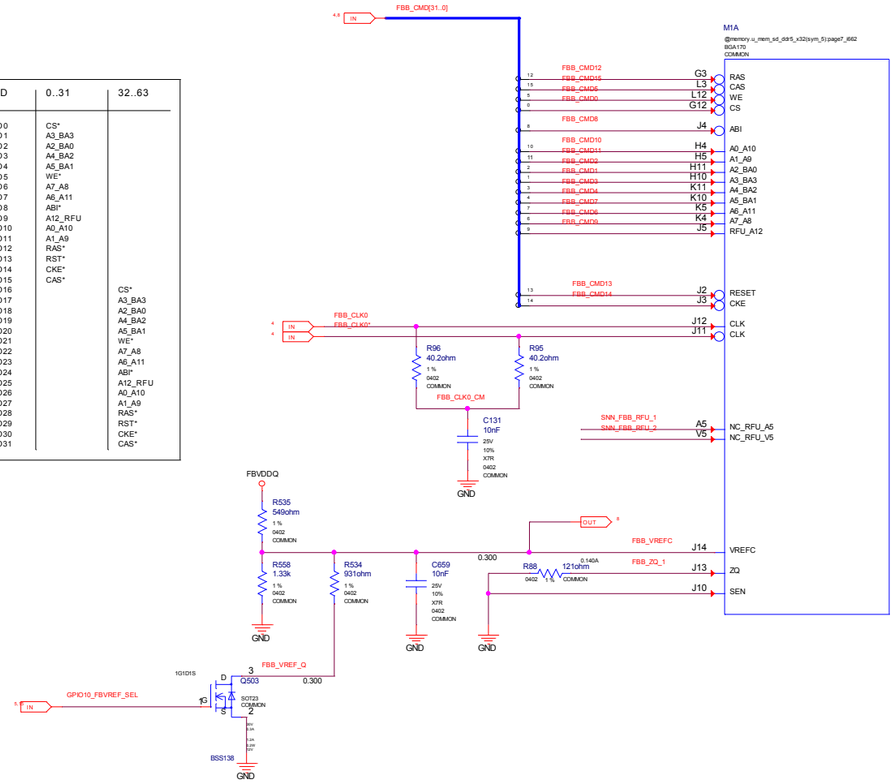
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBA[63:32]

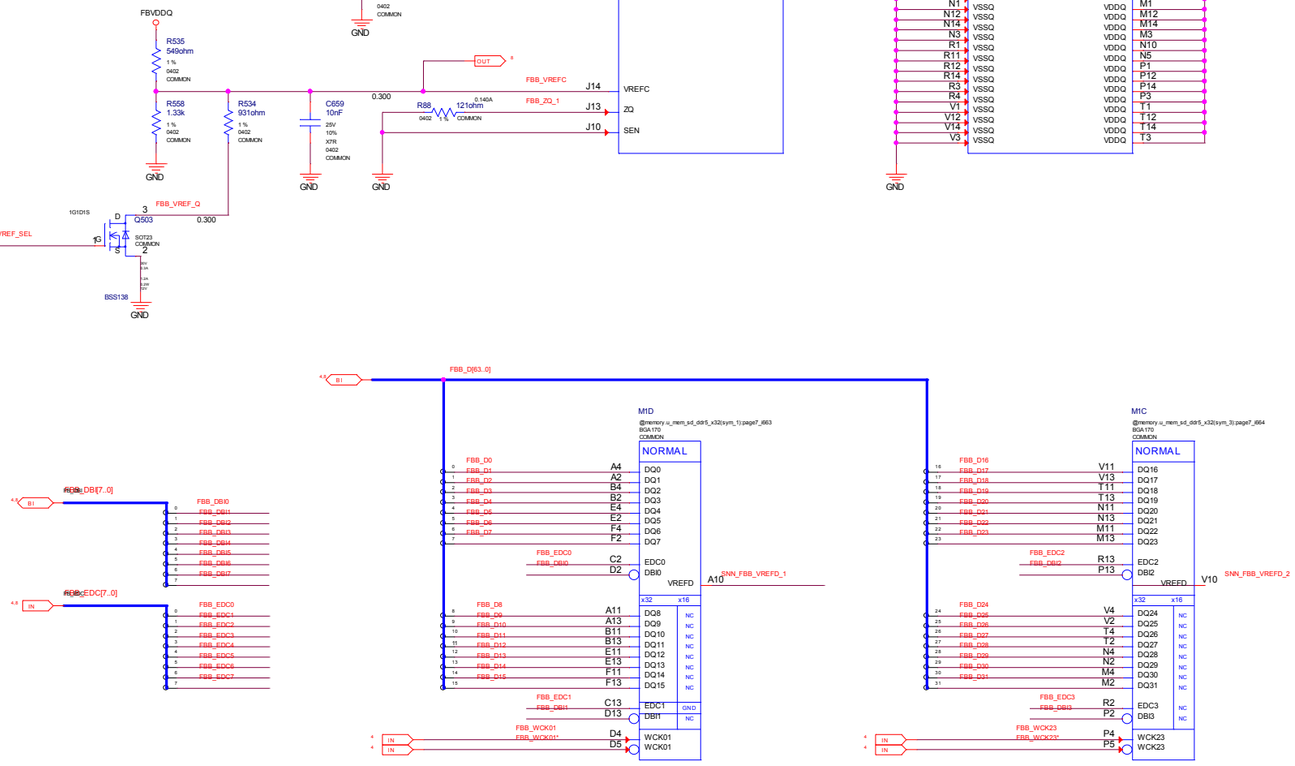
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

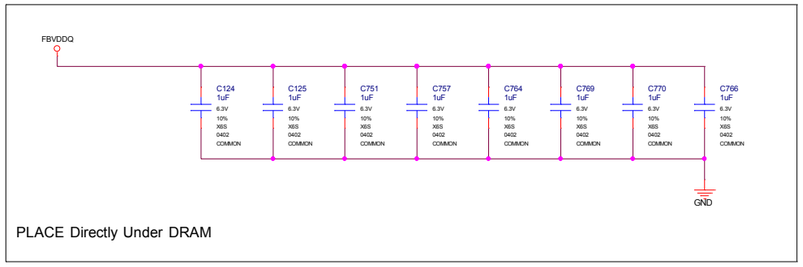
NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	6 OF 27
BOM REV	A	DATE	18-DEC-2015

MEMORY: FBB Partition 31..0

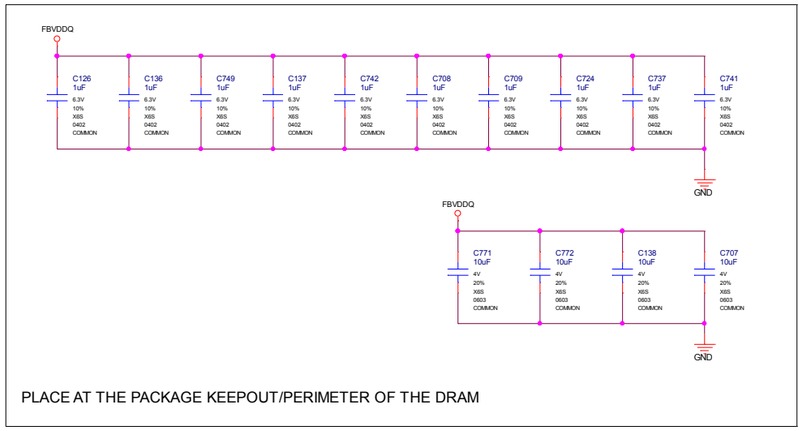
CMD	0..31	32..63
CMD0	CS*	
CMD 1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



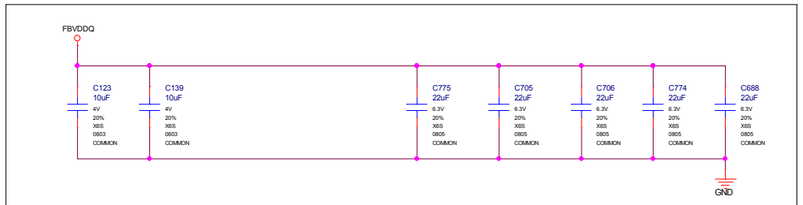




PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM



PLACE Around DRAM

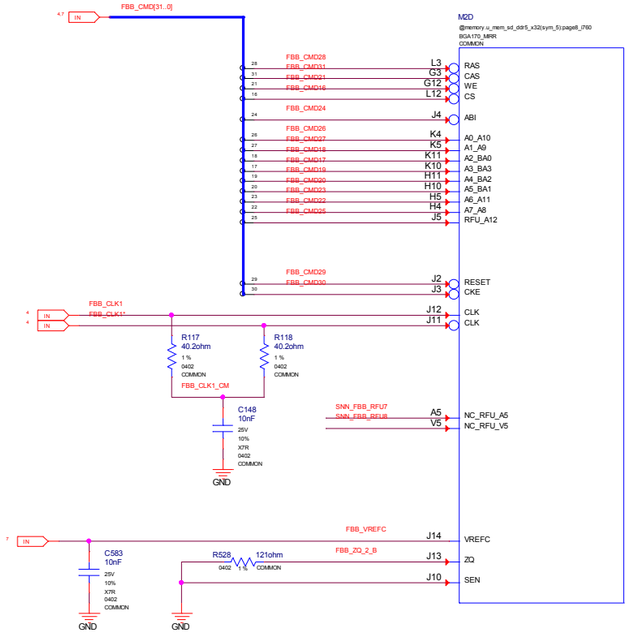
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB[31:0]

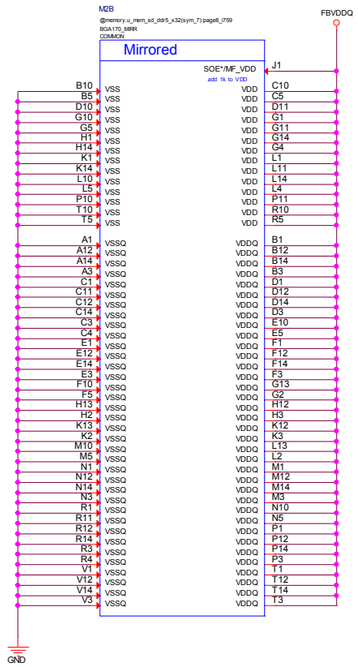
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

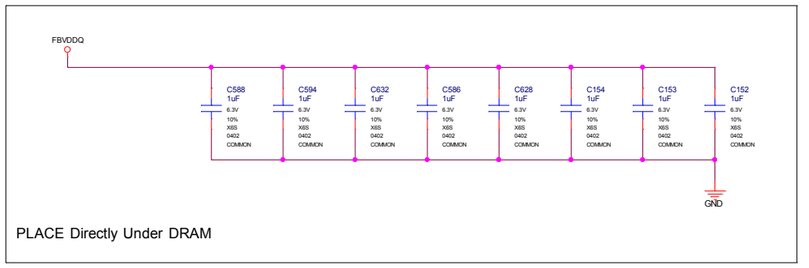
NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	7 OF 27
BOM REV	A	DATE	18-DEC-2015

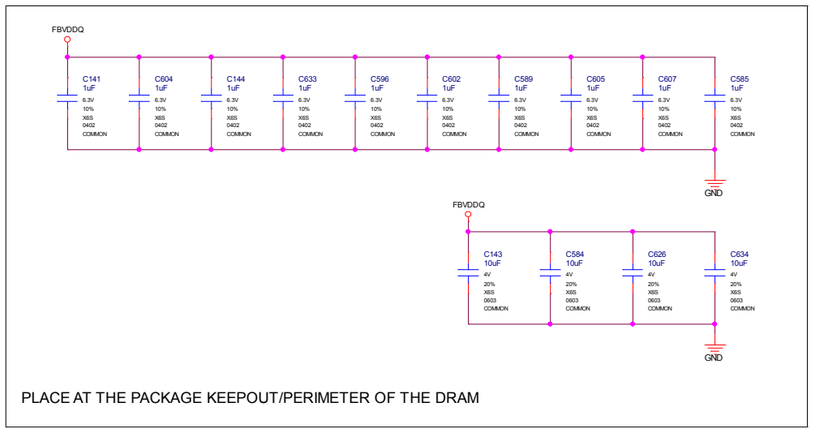
MEMORY: FBB Partition 63..32

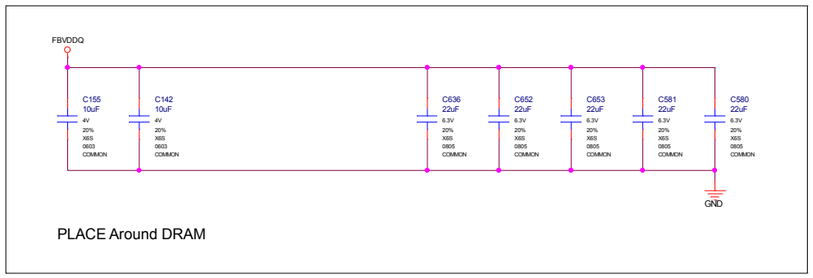
CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*









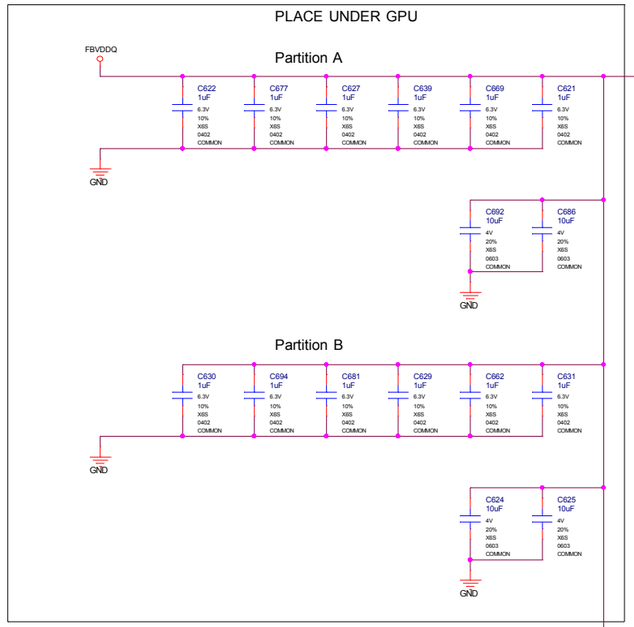


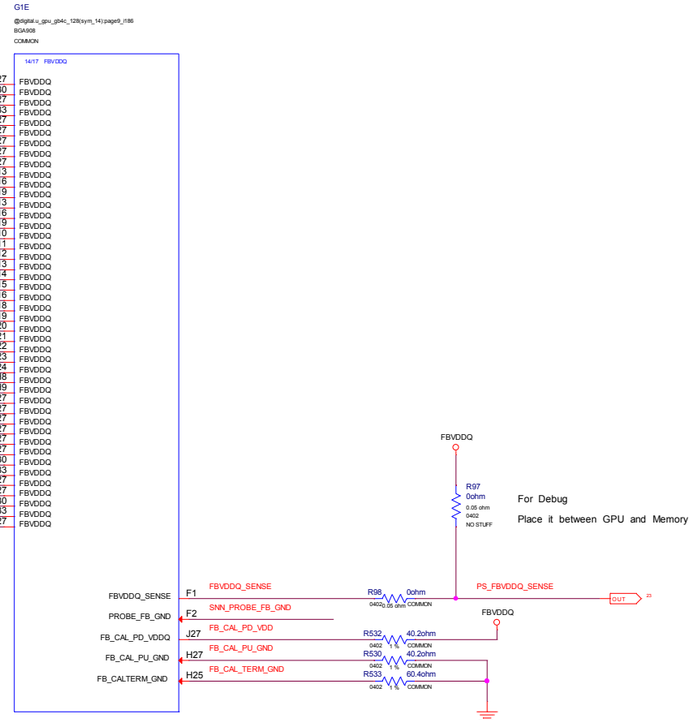
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB[63:32]

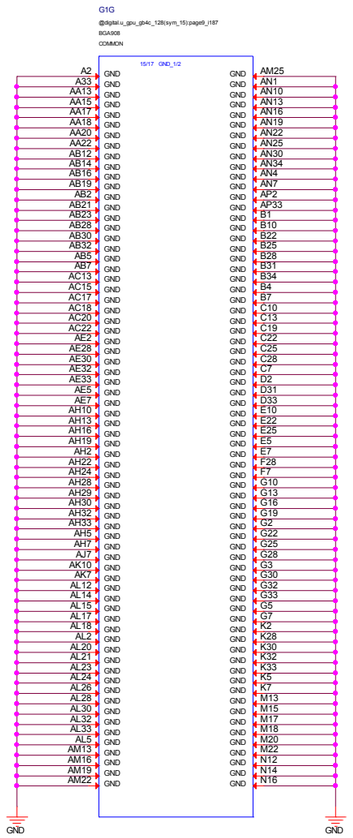
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

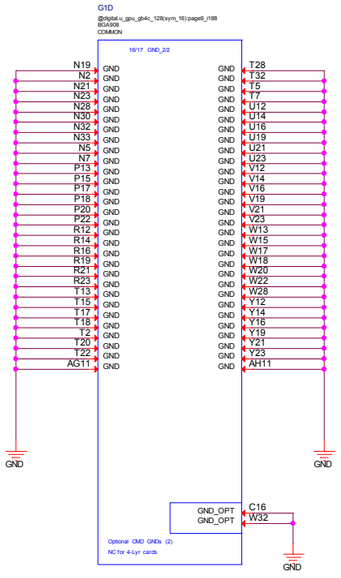
NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	8 OF 27
BOM REV	A	DATE	18-DEC-2015

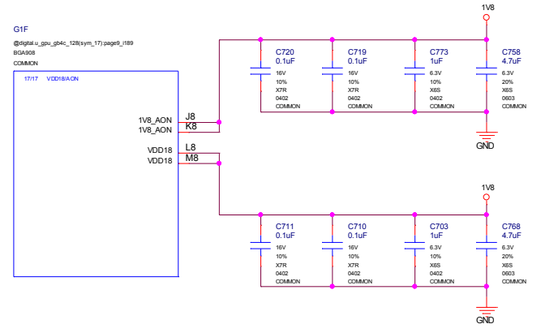
GPU FBVDDQ & 1V8 Decoupling









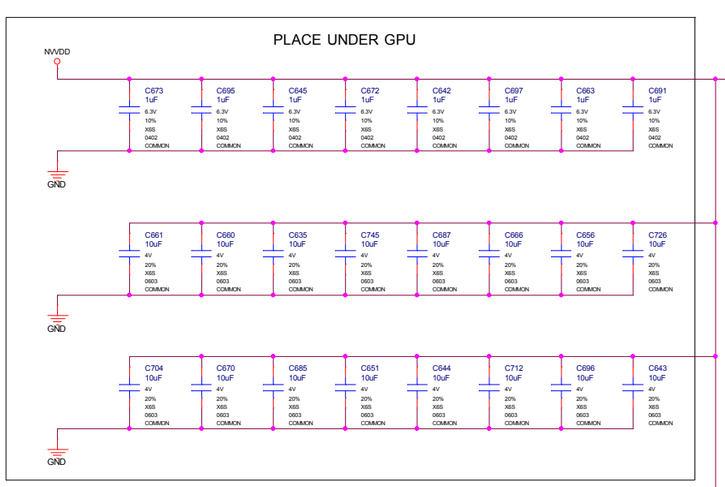


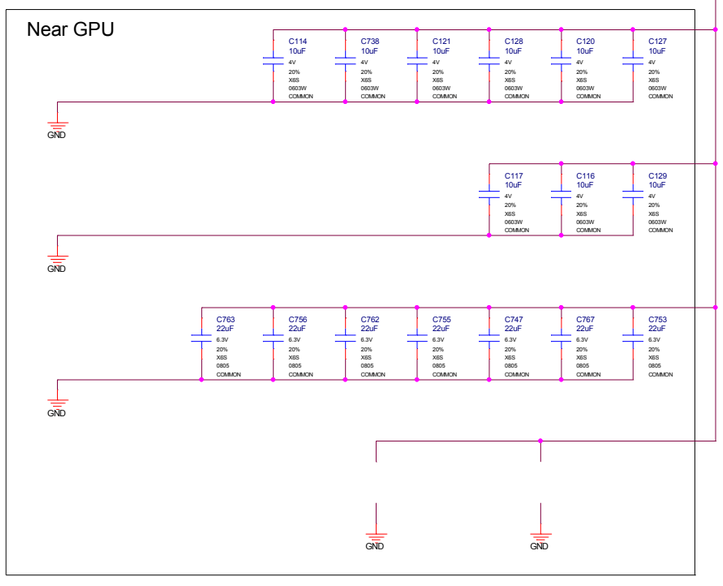
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU FBVDDQ & 1V8 Decoupling

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	9 OF 27
BOM REV	A	DATE	18-DEC-2015

GPU NVVDD & NVVDDS Decoupling

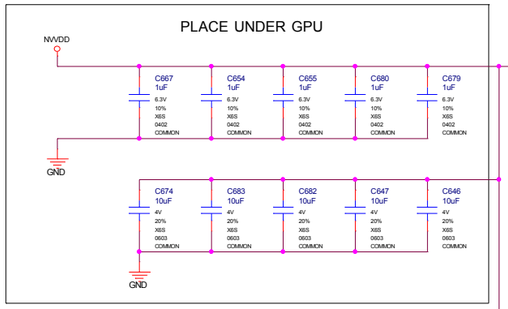


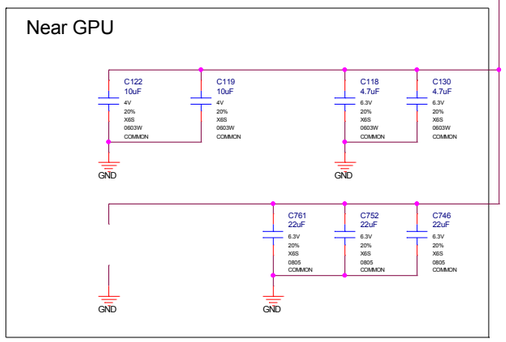


G1H
@digital-u_gpu_gb4c_128(sym_13):page10_i87
BGA/308
COMMON
13/17 NVVDD

AA14 AA21 AB13 AB15 AB17 AB18 AB20 AB22 AC12 AC16 AC19 AC23 M17 M16 M19 M23 N13 N15 N17 N18 N20 N22 P14 P21 R13 R15 R17 R18 R20 R22 T12 T16 T19 T23 U13 U15 U18 U20 U22 V13 V15 V17 V20 V22 W12 W16 W19 W23 Y13 Y15 Y17 Y18 Y20 Y22 — VDD

VDD_SENSE — L4 — GPU_NVVDD_VSENSE — 95DIFF_NETCLASS1 DP_GPU_NVDD_GNDSNS — OUT 24
GND_SENSE — L5 — GPU_NVDD_GNDSNS — 95DIFF_NETCLASS1 DP_GPU_NVDD_GNDSNS — OUT 24





G1J
@digital-u_gpu_gb4c_128(sym_8):page10_i85
BGA/308
COMMON
8/17 VDDS

AA12 AA16 AA19 AA23 AC14 AC21 M14 M21 P12 P16 P19 P23 T14 T21 U17 V18 W14 W21 — VDDS

VDDS_SENSE — U1 — GPU_NVVDDS_VSENSE — R68 0ohm 0402@0.05 0mW NO STUFF — GPU_NVVDD_VSENSE
GNDS_SENSE — U2 — GPU_NVVDDS_GNDSNS — R69 0ohm 0402@0.05 0mW NO STUFF — GPU_NVVDD_GNDSNS

G1K
@digital-u_gpu_gb4c_128(sym_9):page10_i113
BGA/308
COMMON
9/17 XVDD
CONFIGURABLE POWER CHANNELS

NVVDD

XVDD U4 U5 U6 U7 U8 V1 V2 V3 V4 V5 V6 V7 V8 W2 W3 W4 W5 W7 W8 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 AA1 AA2 AA3 AA4 AA5 AA6 AA7 AA8

1V8

G1I
@digital-u_gpu_gb4c_128(sym_4):page10_i114
BGA/308
COMMON
4/17 NC

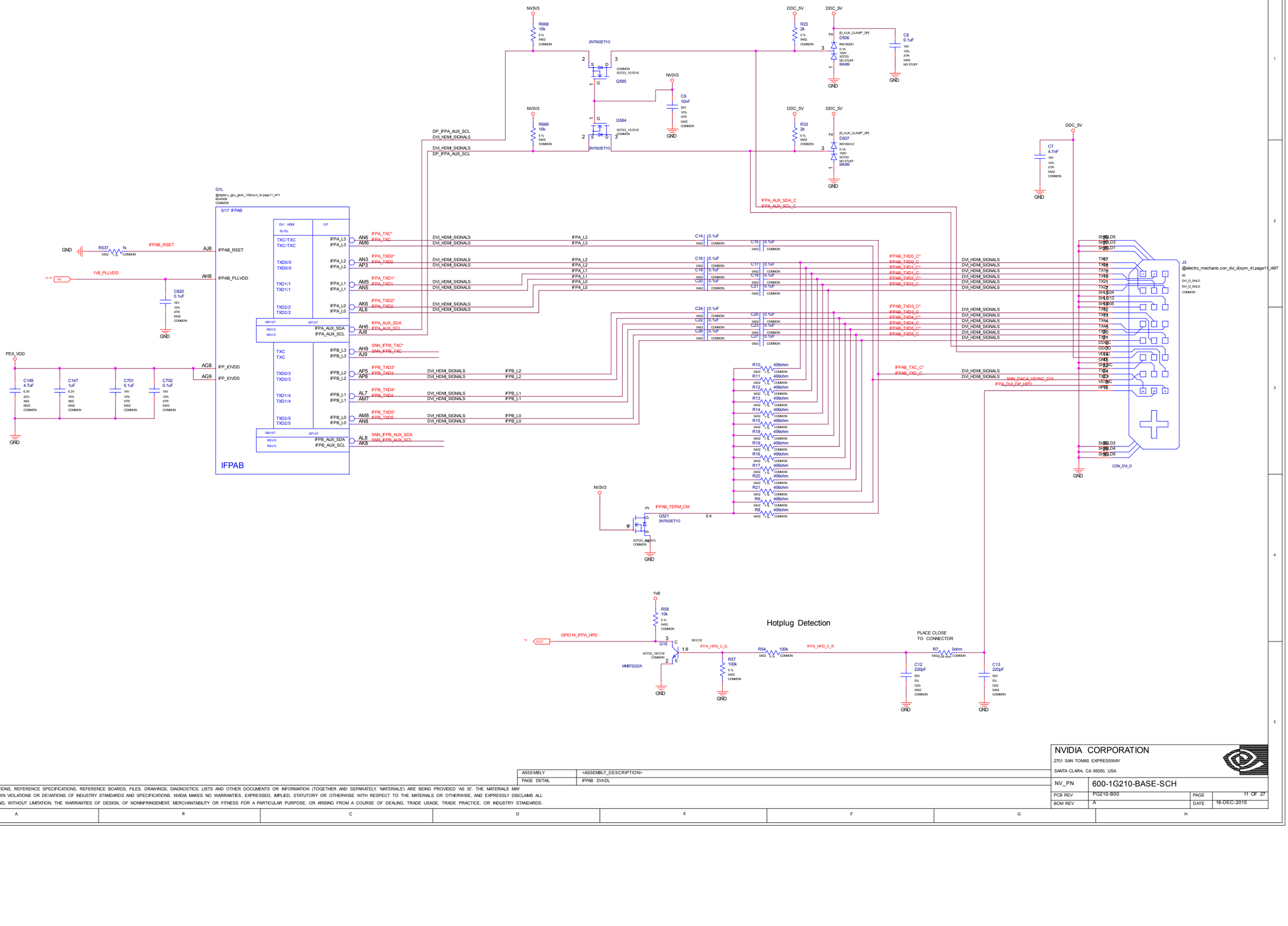
SNN_GPU_NC1	AC6	NC	GM107
SNN_GPU_NC2	AG10	NC	
	AG12	NC	PEX_SVDD_3V3
SNN_GPU_NC5	AG26	NC	PEX_PLLVDD
SNN_GPU_NC6	AG7	NC	IFPD_PLLVDD
	AJ11	NC	
	AJ26	NC	PEX_TCLK_OUT
SNN_GPU_NC9	AJ28	NC	
SNN_GPU_NC10	AJ4	NC	
	AJ5	NC	
	AK26	NC	PEX_TCLK_OUT*
SNN_GPU_NC12	AK9	NC	
SNN_GPU_NC13	AL10	NC	
SNN_GPU_NC14	AL11	NC	
SNN_GPU_NC15	AL9	NC	
SNN_GPU_NC16	AM9	NC	
SNN_GPU_NC17	AN2	NC	
SNN_GPU_NC18	AN9	NC	
SNN_GPU_NC19	AP8	NC	
SNN_GPU_NC20	C15	NC	
SNN_GPU_NC21	D19	NC	GP107/GM107 COMPATIBLE DESIGNS MUST LEAVE NC PINS FLOATING EXCEPT FOR THE CONNECTIONS SHOWN
SNN_GPU_NC22	D20	NC	
SNN_GPU_NC23	D23	NC	
SNN_GPU_NC24	D26	NC	
SNN_GPU_NC25	V32	NC	

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU NVVDD & NVVDDS DECOUPLING

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	10 OF 27
BOM REV	A	DATE	18-DEC-2015

IFPAB DVI-DL



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPAB DVI-DL

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	11 OF 27
BOM REV	A	DATE	18-DEC-2015

IFPD DP

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPD DP

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	12 OF 27
BOM REV	A	DATE	18-DEC-2015

IFPC HDMI

Hotplug Detection

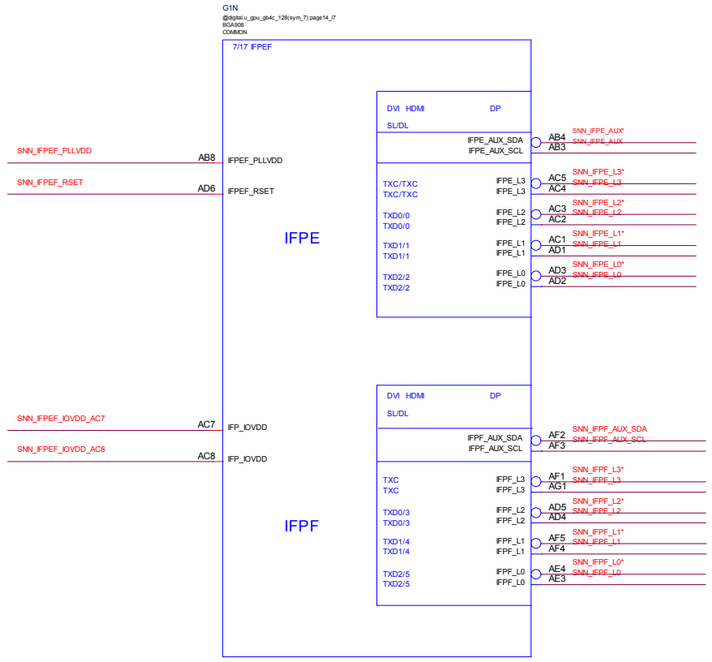
PLACE CLOSE TO CONNECTOR

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPC HDMI

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	13 OF 27
BOM REV	A	DATE	18-DEC-2015

IFPEF UNUSED



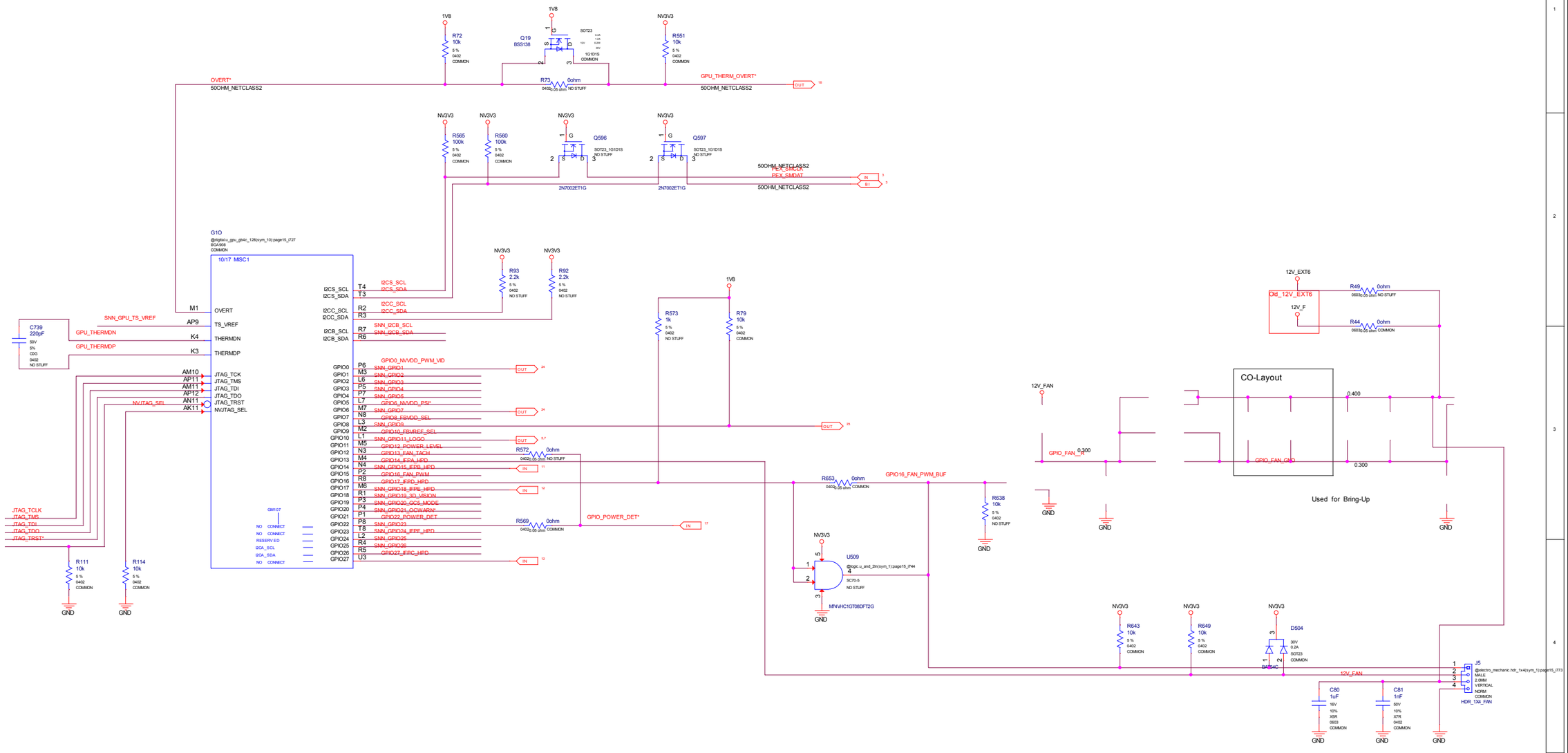
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPEF UNUSED

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	14 OF 27
BOM REV	A	DATE	18-DEC-2015

MISC1: GPIO, Fan, Thermal, JTAG

PADS FOR DEBUGGING



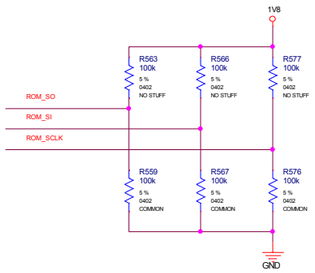
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	15 OF 27
BOM REV	A	DATE	18-DEC-2015

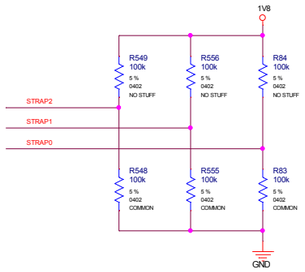
MISC2: ROM, XTAL, Straps

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

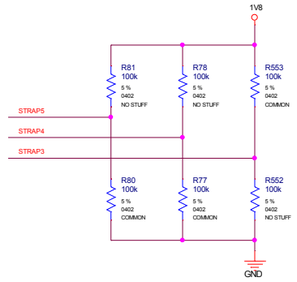


H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

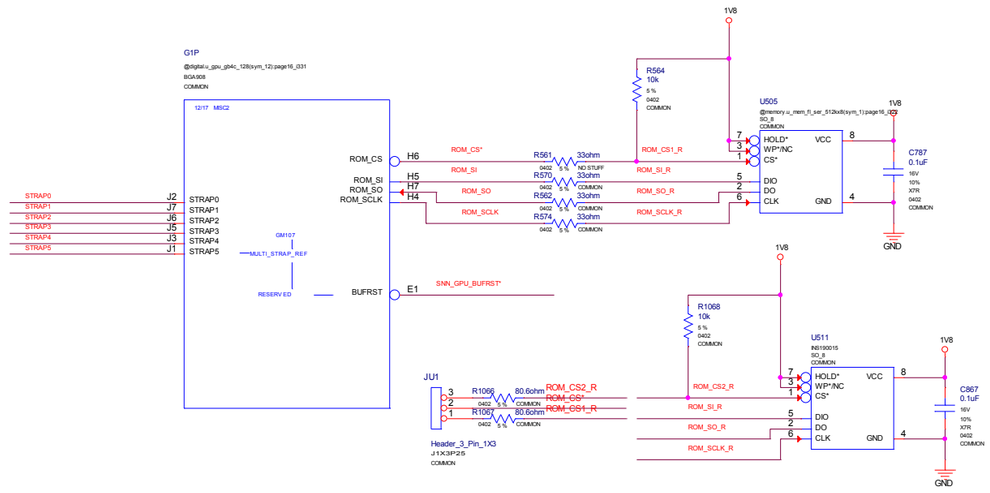


1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

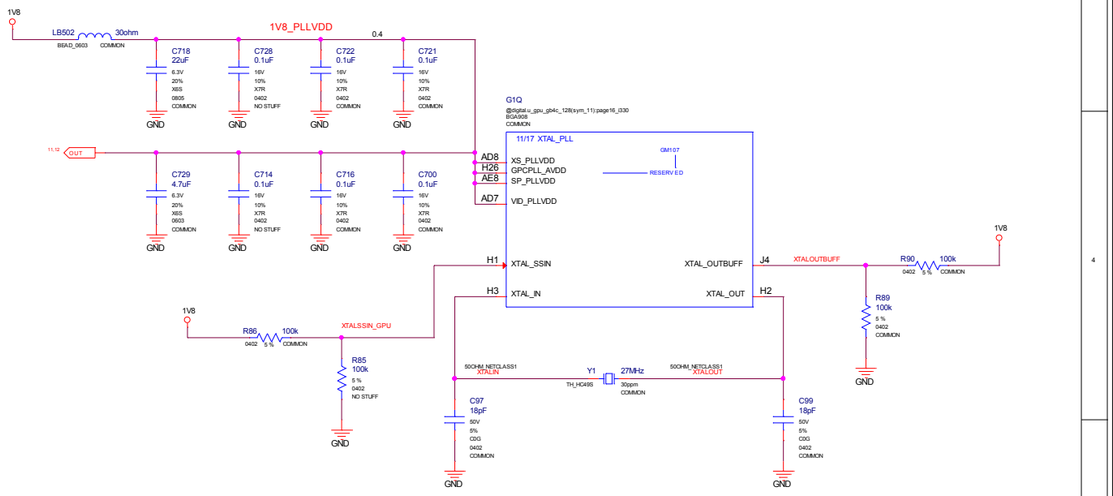
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



Smart Fan

XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



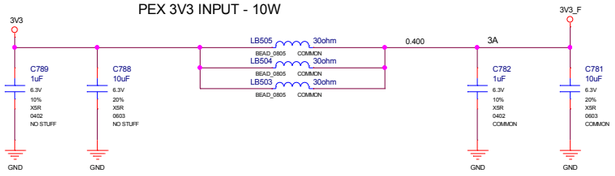
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL, Straps

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

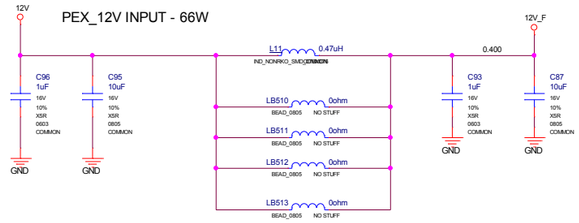
NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	16 OF 27
BOM REV	A	DATE	18-DEC-2015

Power Inputs and Filtering

PEX 3V3 INPUT - 10W

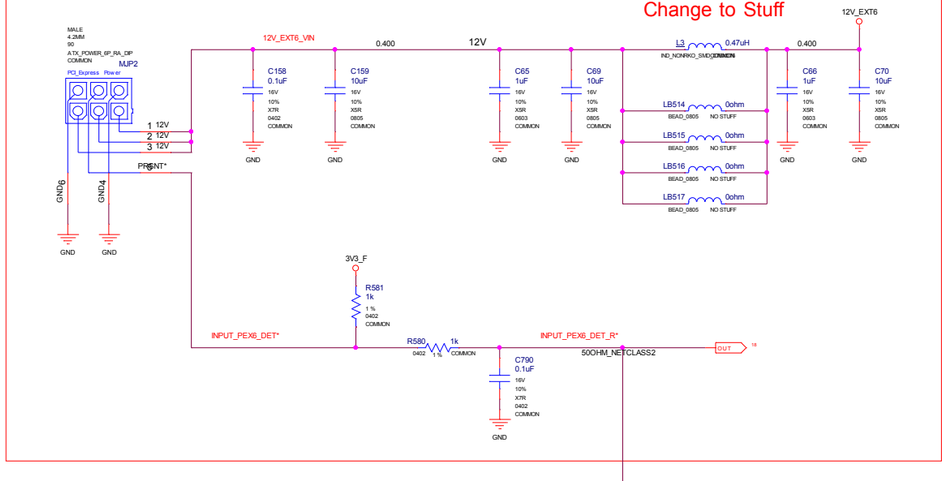


PEX_12V INPUT - 66W

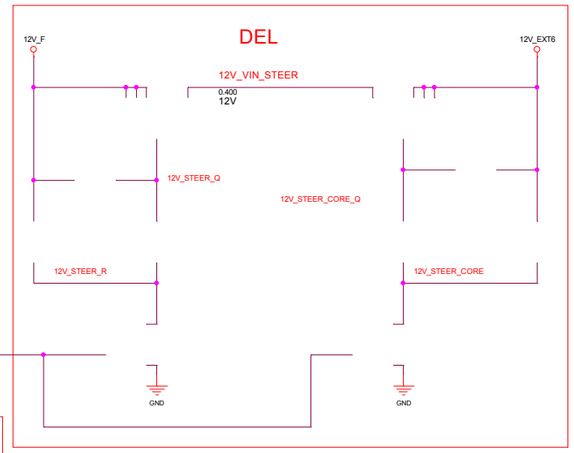


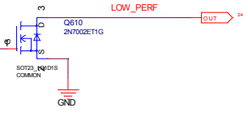
Change to NO Stuff

Change to Stuff

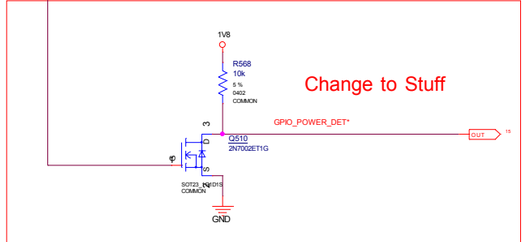


DEL





Change to Stuff

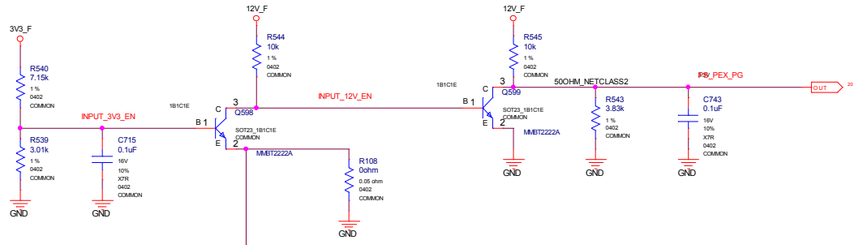


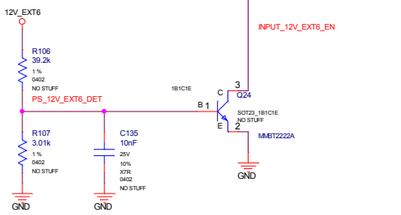
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Power Inputs and Filtering

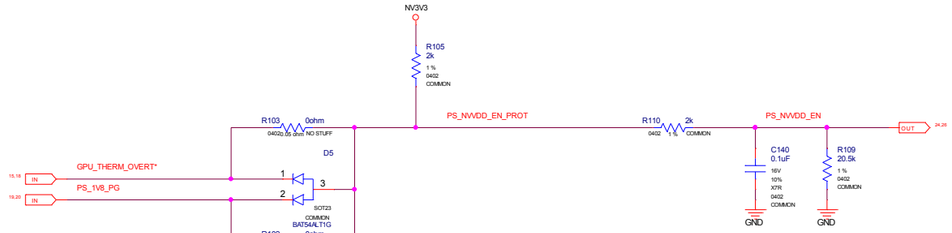
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

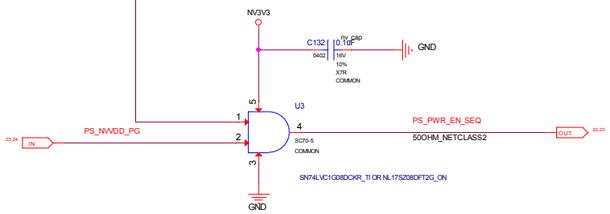
NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	17 OF 27
BOM REV	A	DATE	18-DEC-2015

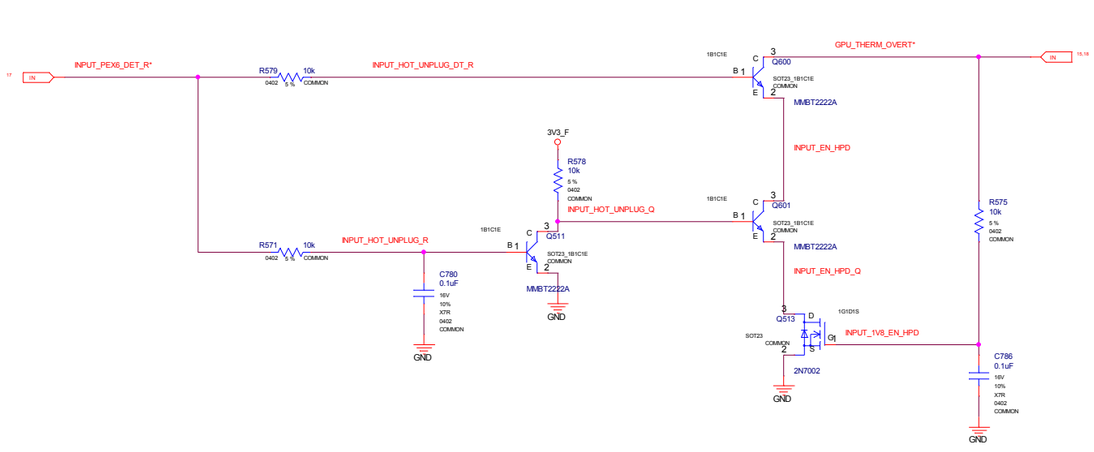
Power sequence









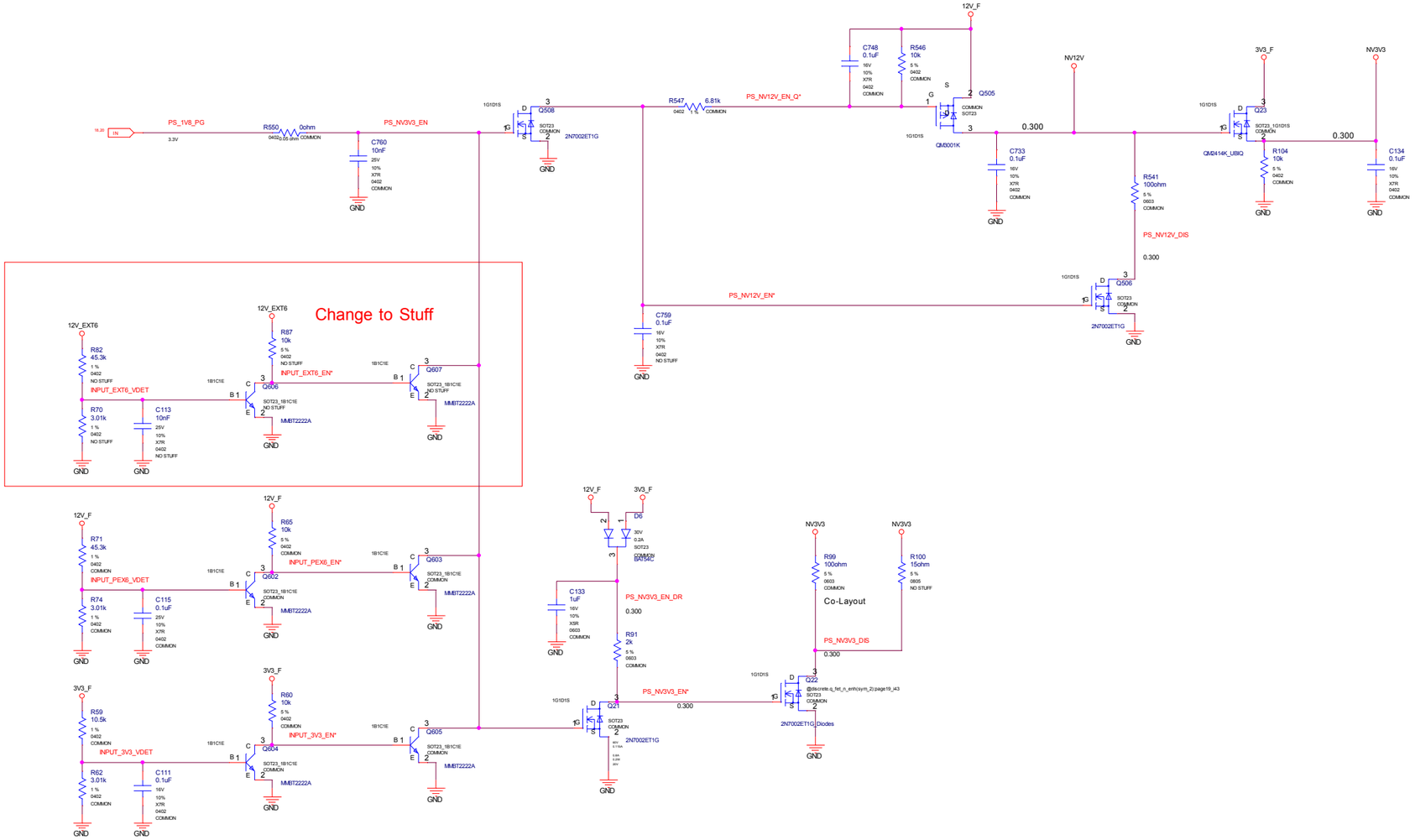


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Power Sequence

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	18 OF 27
BOM REV	A	DATE	18-DEC-2015

PS: NV3V3 & NV12V

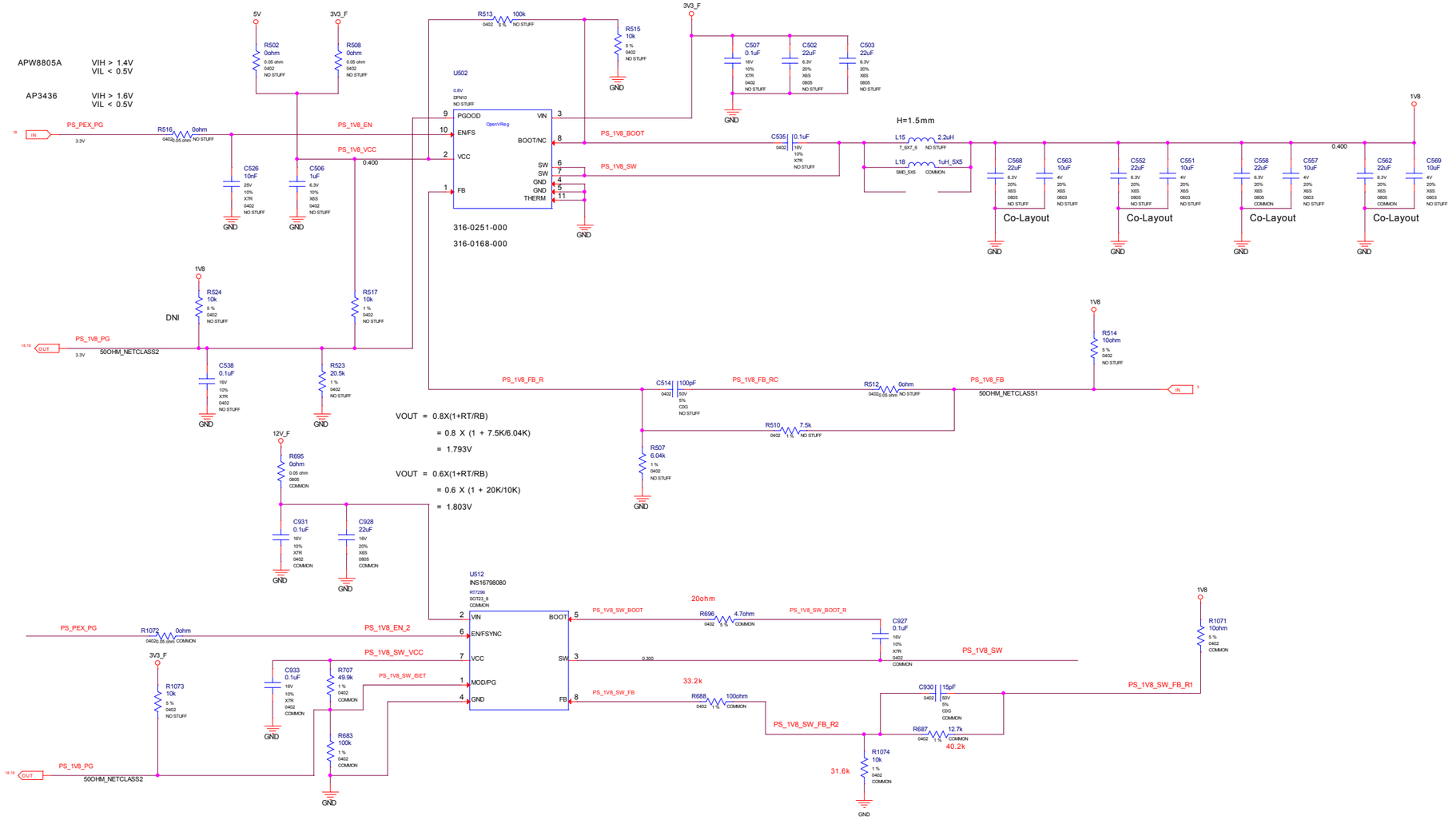


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NV3V3 & NV12V

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	19 OF 27
BOM REV	A	DATE	18-DEC-2015

PS I: 1V8

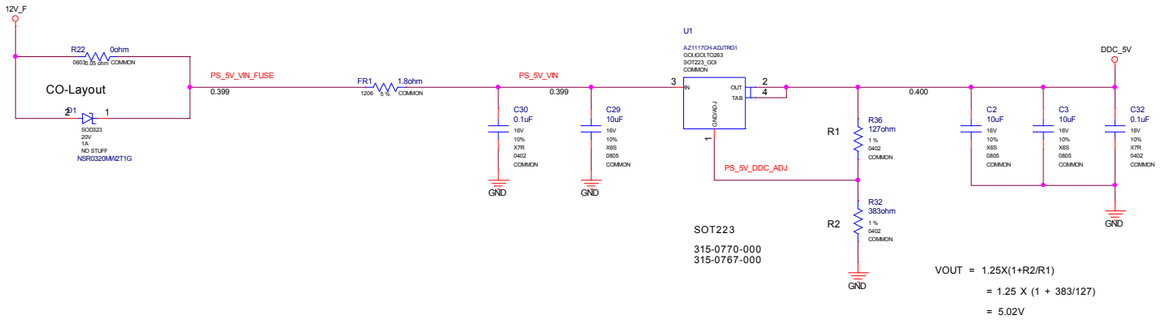


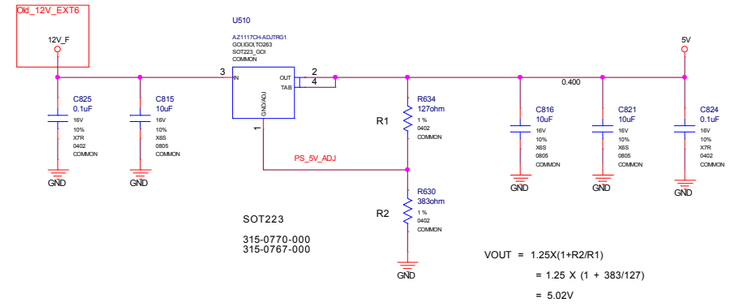
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 1V8

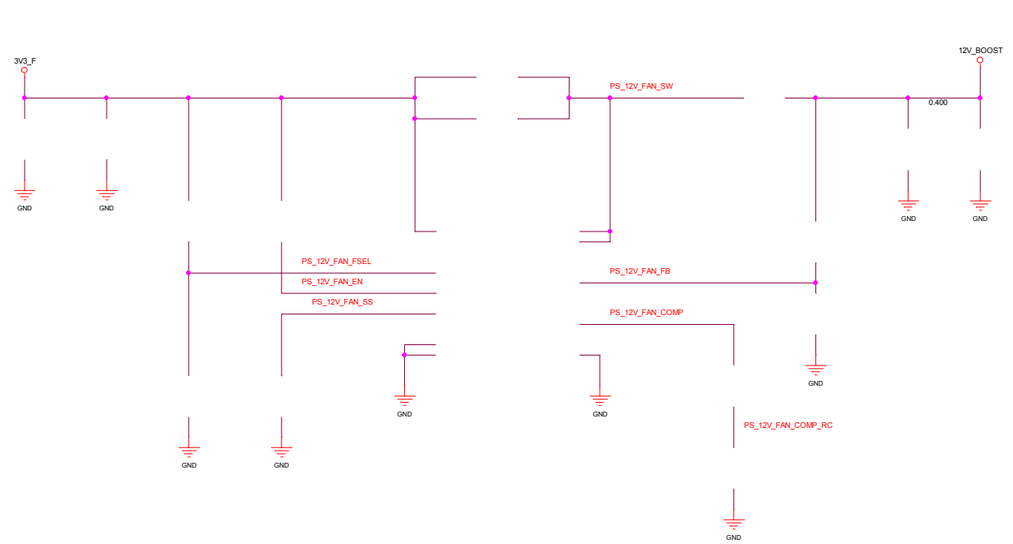
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	20 OF 27
BOM REV	A	DATE	18-DEC-2015

PSII:5V & 12V_FAN







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PSII: 5V & 12V_FAN

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	21 OF 27
BOM REV	A	DATE	18-DEC-2015

PS III: PEXVDD

uP1728 VIH > 1.5V
VIL < 0.4V

RT8071 VIH > 1.6V
VIL < 0.4V

316-0251-000
316-0168-000

130-0633-000
130-0632-000
H=1.5mm
130-0473-000
131-0699-000

VOUT = 0.8X(1+RT/RB)
= 0.8 X (1 + 7.5K/30.1K)
= 1.0V

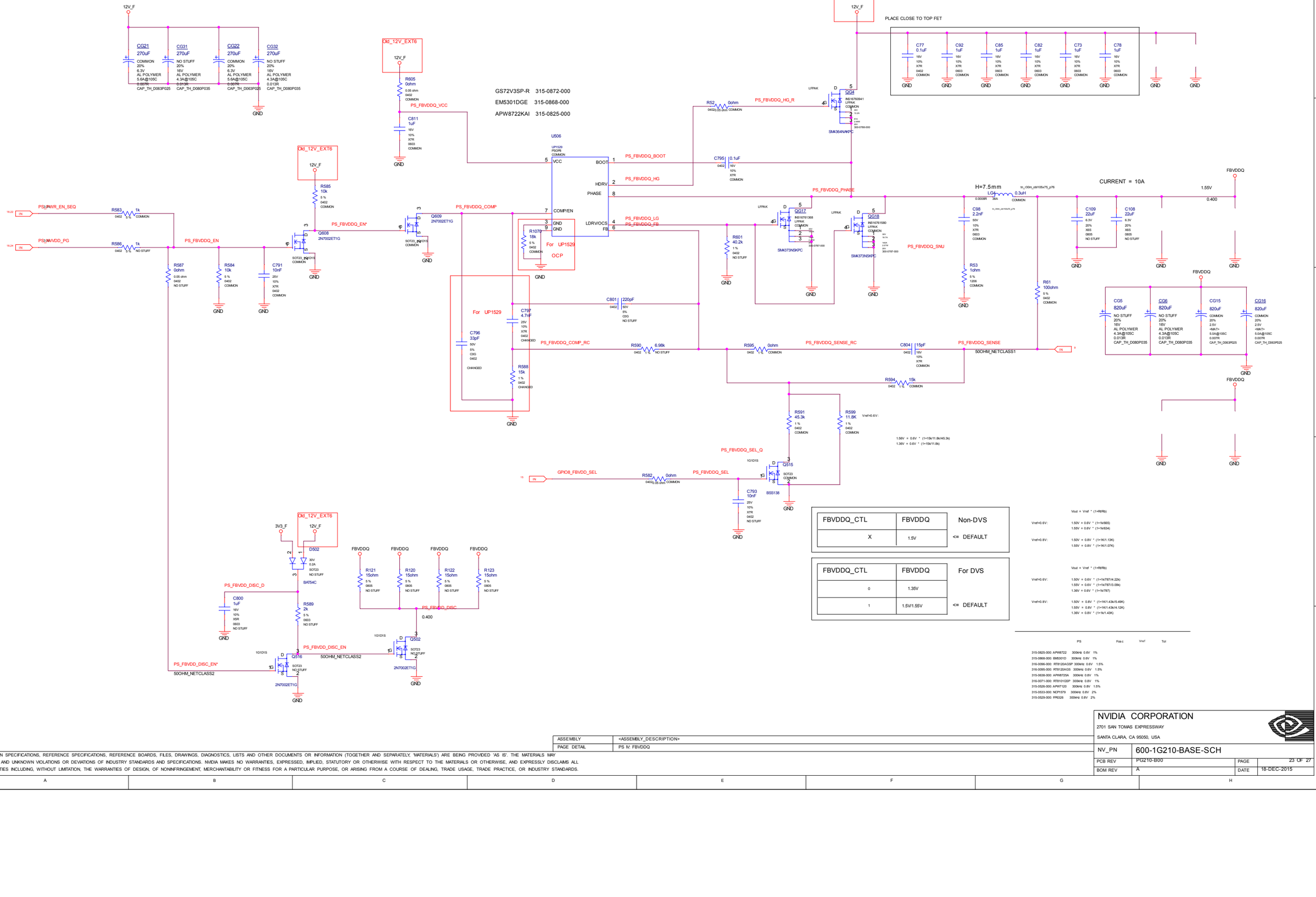
VOUT = 0.6X(1+RT/RB)
= 0.6 X (1 + 6.81K/10K)
= 1.0V

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS III: PEXVDD

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	22 OF 27
BOM REV	A	DATE	18-DEC-2015

PS IV: FBVDDQ



FBVDDQ_CTL	FBVDDQ	
X	1.5V	Non-DVS <= DEFAULT

FBVDDQ_CTL	FBVDDQ	
0	1.35V	For DVS
1	1.5V/1.55V	<= DEFAULT

Vout = Vref * (1+Rt/Rb)

Vref=0.6V:
1.50V = 0.6V * (1+1k/665)
1.55V = 0.6V * (1+1k/634)

Vref=0.8V:
1.50V = 0.8V * (1+1K/1.13K)
1.55V = 0.8V * (1+1K/1.07K)

Vout = Vref * (1+Rt/Rb)

Vref=0.6V:
1.50V = 0.6V * (1+1k/787/4.22k)
1.55V = 0.6V * (1+1k/787/3.09k)
1.36V = 0.6V * (1+1k/787)

Vref=0.8V:
1.50V = 0.8V * (1+1K/1.43k/5.49K)
1.55V = 0.8V * (1+1K/1.43k/4.12K)
1.36V = 0.8V * (1+1k/1.43K)

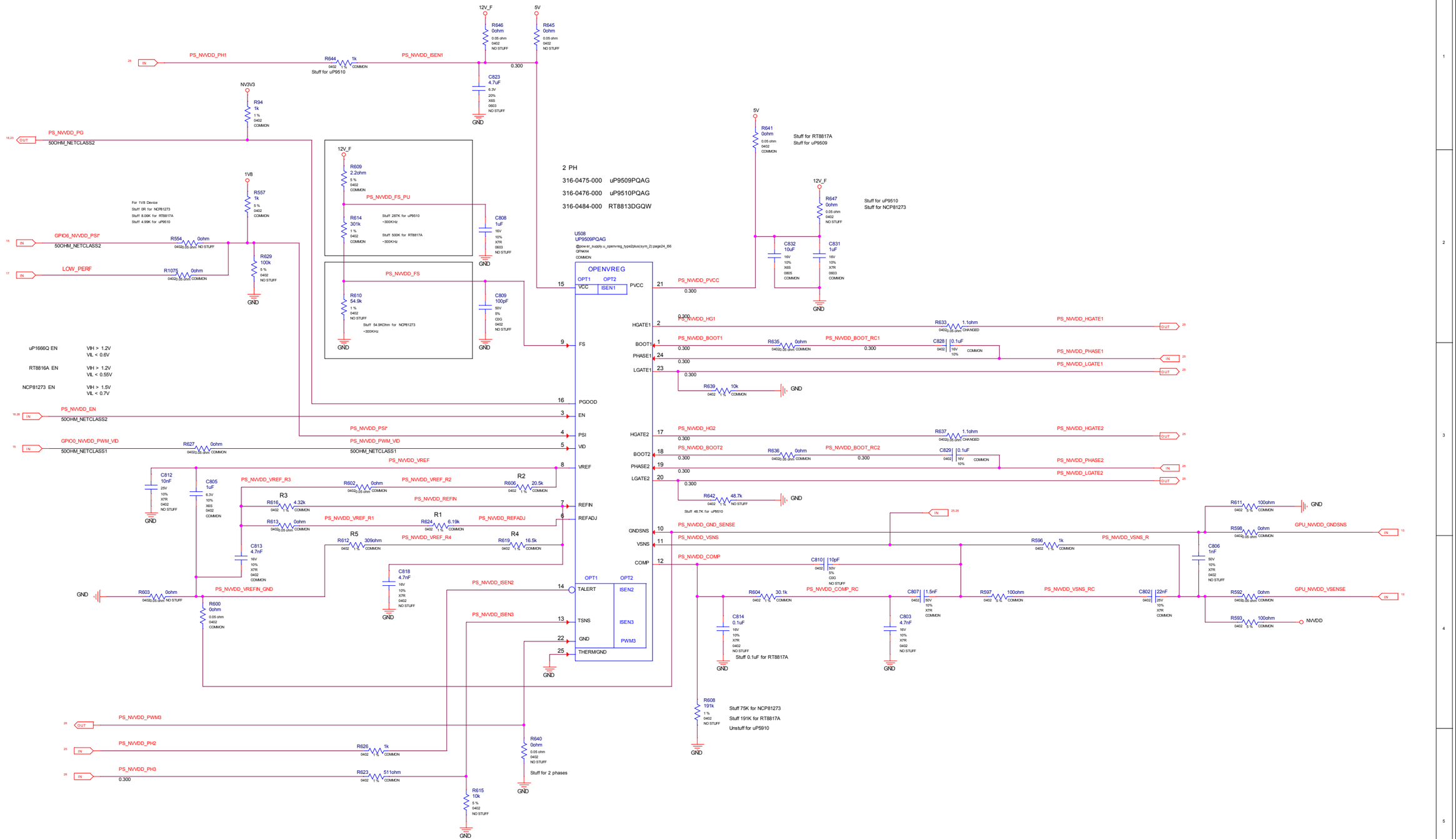
PS	Fosc	Vref	Tol
315-0825-000: APW8722	300kHz	0.6V	1%
315-0868-000: EM5301D	300kHz	0.6V	1%
316-0096-000: RT8120AGSP	300kHz	0.6V	1.5%
316-0095-000: RT8120AGS	300kHz	0.6V	1.5%
315-0638-000: APW8725A	300kHz	0.8V	1%
316-0071-000: RT8101GSP	300kHz	0.8V	1%
315-0526-000: APW7120	300kHz	0.8V	1.5%
315-0533-000: NCP1579	300kHz	0.8V	2%
315-0529-000: FR9326	300kHz	0.8V	2%

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS IV: FBVDDQ

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	23 OF 27
BOM REV	A	DATE	18-DEC-2015

PS V: NVVDD OVR2+1

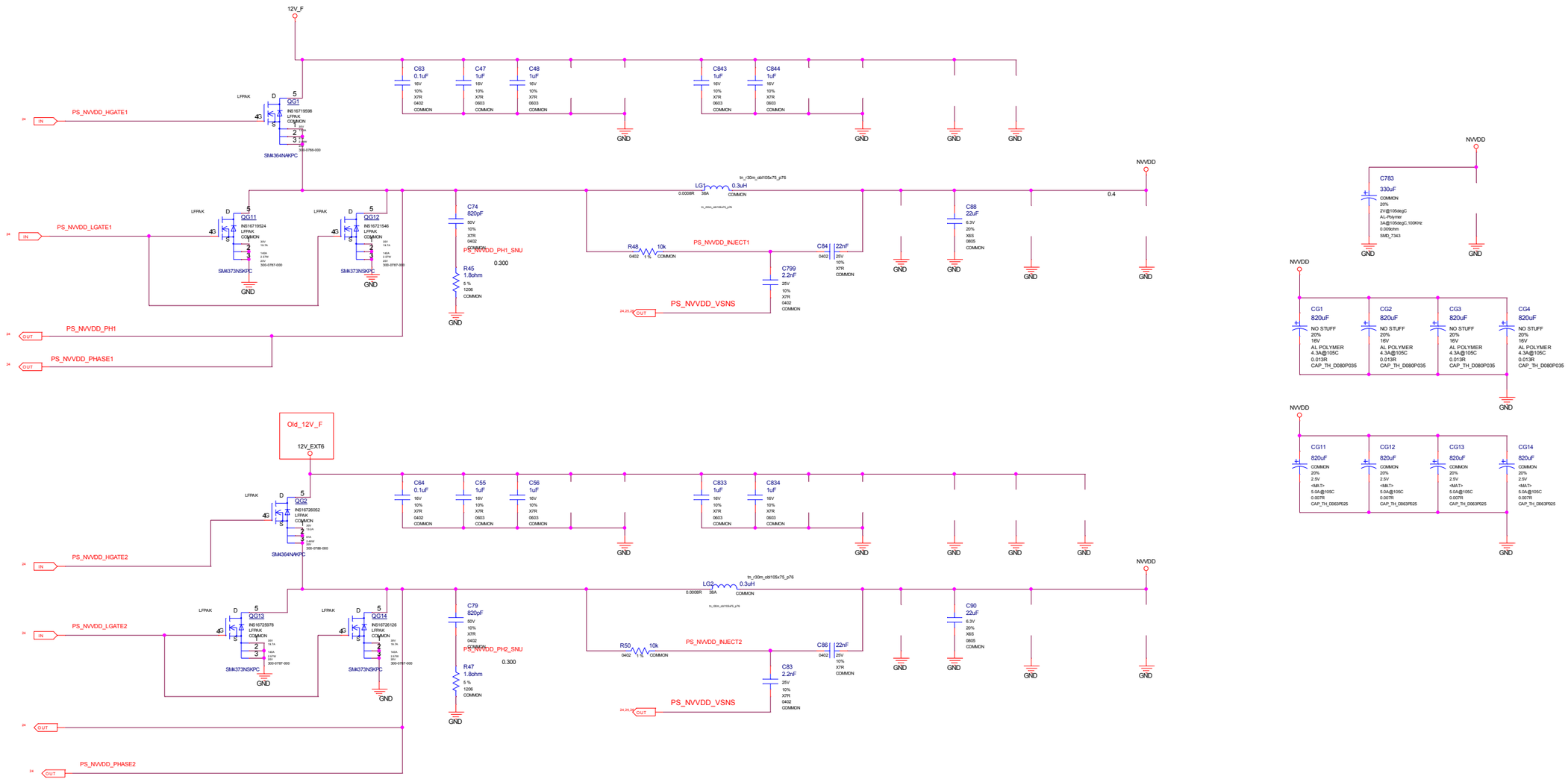


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS V: NVVDD OVR2+1

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	24 OF 27
BOM REV	A	DATE	18-DEC-2015

PS V: NVVDD Phase 1,2

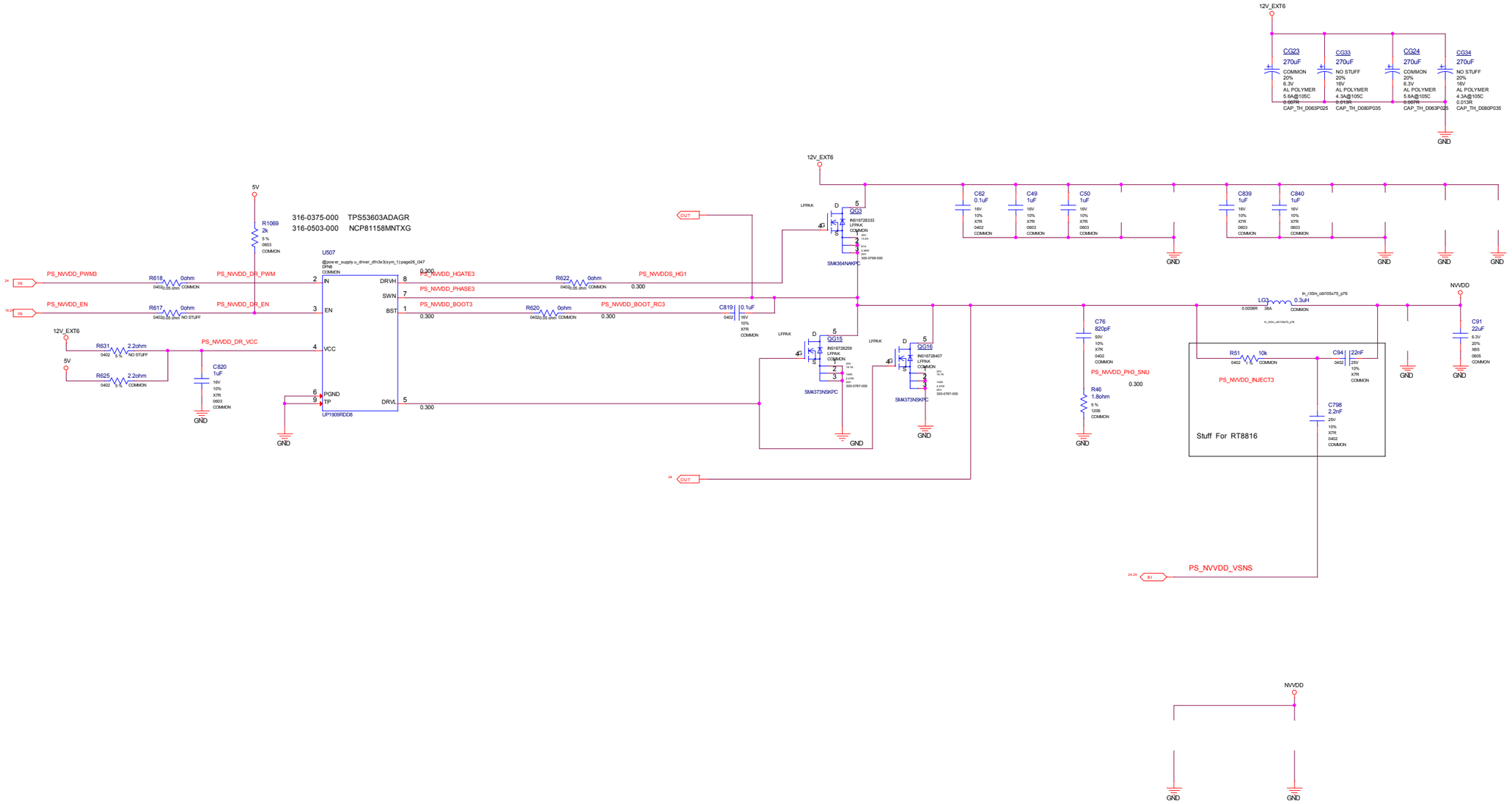


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS V: NVVDD Phase 1,2

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_P.N	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	25 OF 27
BOM REV	A	DATE	18-DEC-2015

PS V: NVVDD Phase 3

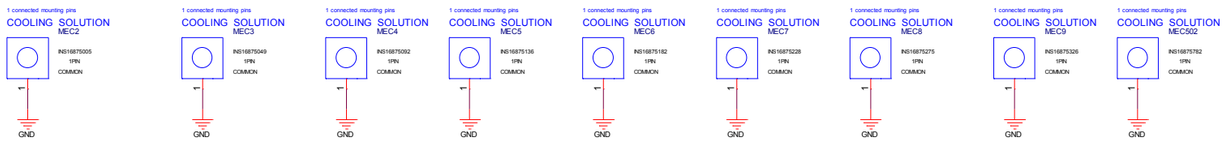


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS V: NVVDD Phase 3

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	26 OF 27
BOM REV	A	DATE	18-DEC-2015

Mechanical: Bracket/Thermal Solution



Brackets:

GPU Stiffener:

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH: Bracket/Thermal

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	27 OF 27
BOM REV	A	DATE	18-DEC-2015