


NV11, AGP4X, 4MX16 SDR SDRAM, RGB, TV DOWN.
PCI DEVICE ID 0X0=0X110 FOR NV11.

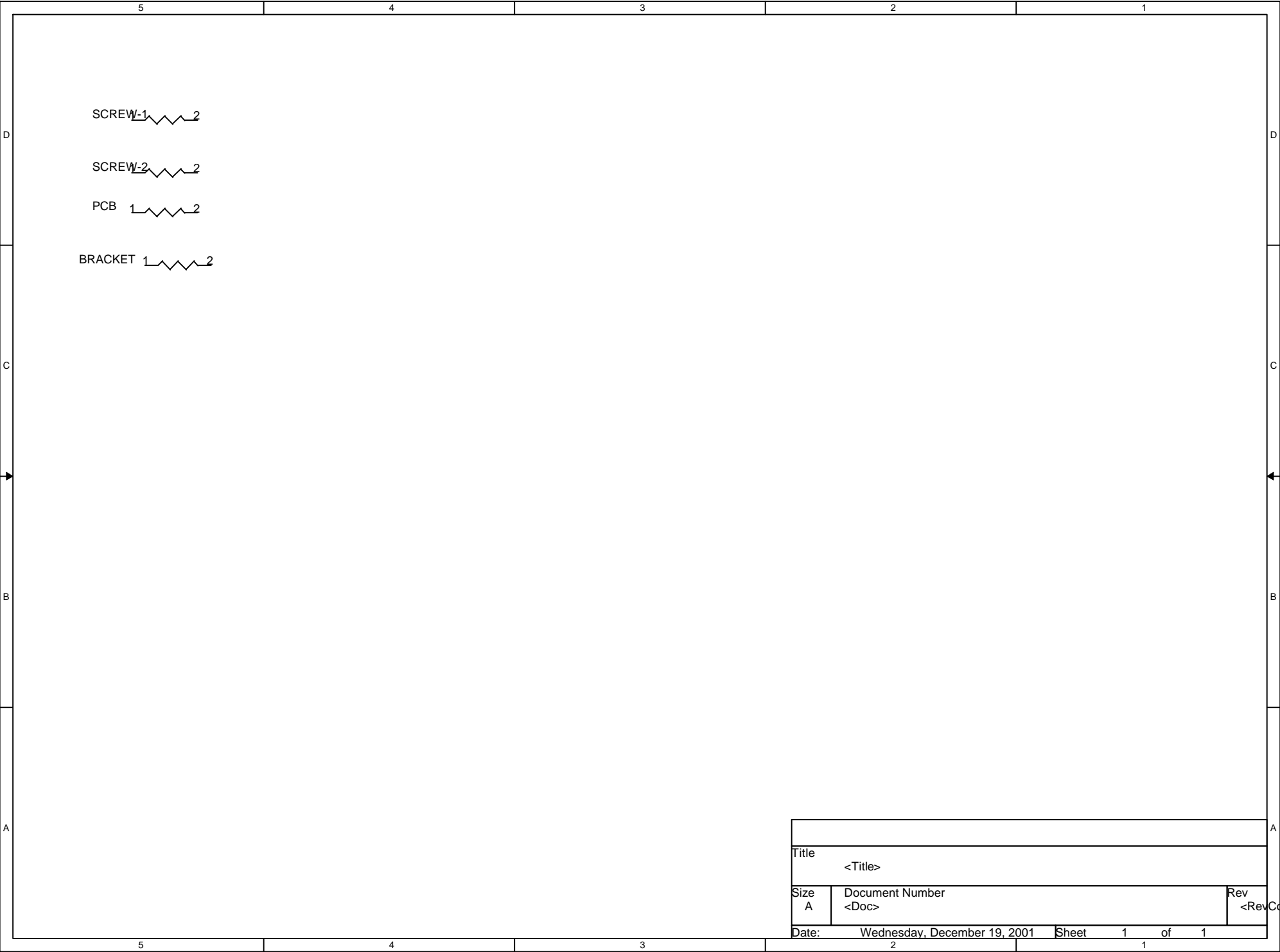
STRAPS: AGP4X, FAST WRITE ENA, ADP BIOS, NORMAL PCIAD, 14.318MHZ

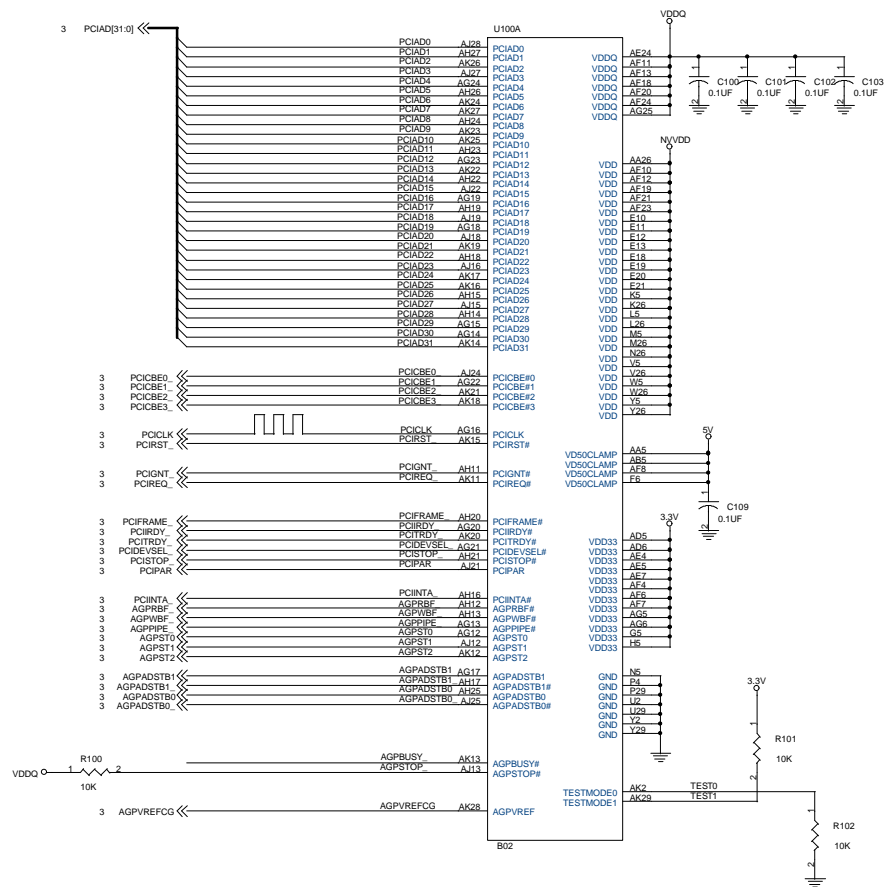
STRAP_RAM_TYPE [5:2]=0001-4MX16 SDR SDRAM

HISTORY REV. A00 BASED ON P39-C00:
A02: Added test nets for DFPDE and DFPCLK_
A02: Changed L202, L206 and L210 to 0603 MTL Inductors.
A02: Changed Rset resistor R212 to 102 ohm 1%
A02: Changed Strap Resistor R130 to No Stuff and Stuff R129

602-P0036-0000-A00

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	Size B	CAGE Code	DWG NO	Rev
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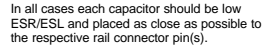
1a. NVXX HOST



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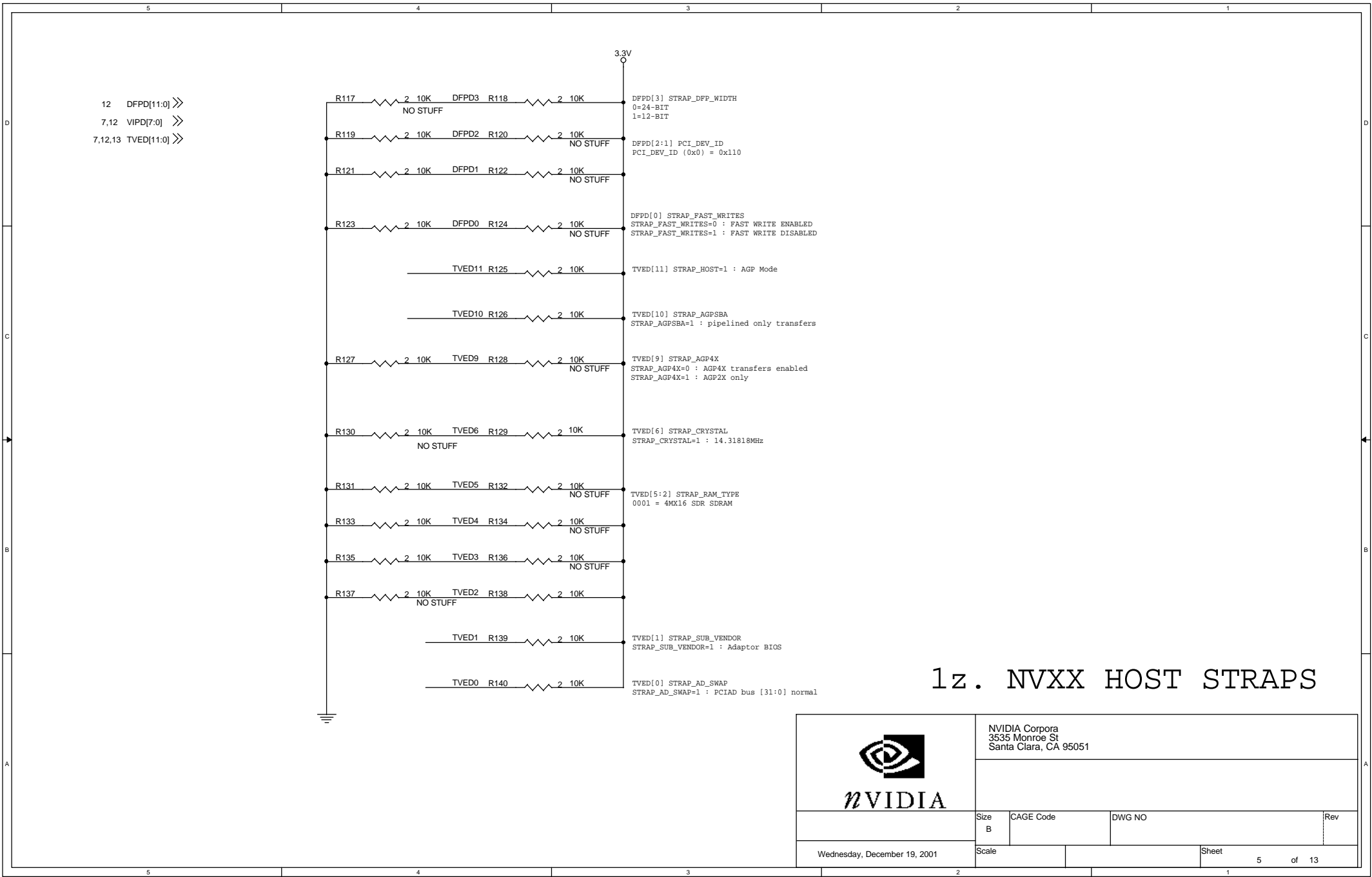
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C			
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Size C	CAGE Code	DWG NO	Rev
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A B C D E

3.3V

L211

150-220R_100MHZ

1 2

6

CDDCSCL

6

CDDCSDA

12

CACL

12

CSDA

VIPCLK

VIPCTL

12

VIPHAD0

12

VIPHAD1

12

VIPHAD2

12

VIPHAD3

12

VIPHAD4

VIPHAD0

VIPHAD1

VIPHAD2

VIPHAD3

VIPHAD4

VIPHAD5

VIPHAD6

VIPHAD7

AG7

AH5

AH6

AK5

A8

B7

A4

C4

AC3

AC4

C8

AK3

AH1

AD4

U100D

DDCSCL

DDCSDA

I2CSCL

I2CSDA

VIPCLK

VIPCTL

VIPHAD0

VIPHAD1

VIPHAD2

VIPHAD3

VIPHAD4

VIPHAD5

VIPHAD6

VIPHAD7

DACVDD

PLLVD

AK9

AK8

DACCOMP

DACVREF

DACRSET

AK11

AK10

AJ10

DACRSET

AJ9

DACGND

BUF_RST#

TVVSYNC

TVHSYNC

TVCLKOUT

TVCLKIN

XTALSIN

XTALOUT

XTALIN

XTALOUT

XTALIN

XTALOUT

XTALIN

XTALOUT

XTALIN

XTALOUT

XTALIN

XTALOUT

XTALIN

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VIPCLK

VIPD0

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VIPD2

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VIPD4

VIPD5

VIPD6

VIPD7

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VIPD1

VIPD2

VIPD3

VIPD4

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VIPD6

VIPD7

VIPD8

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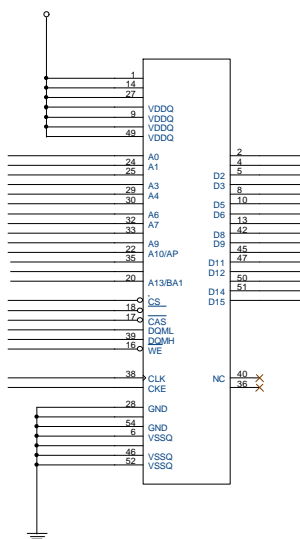
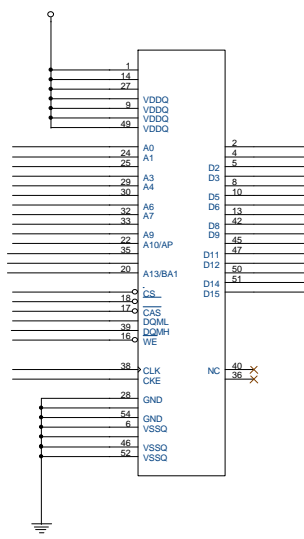
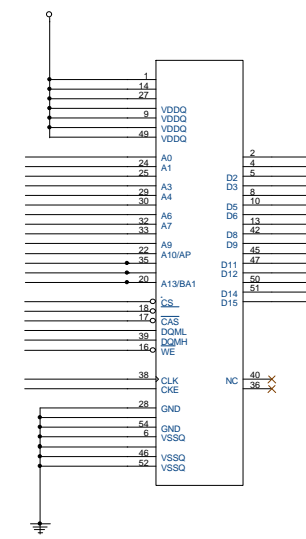
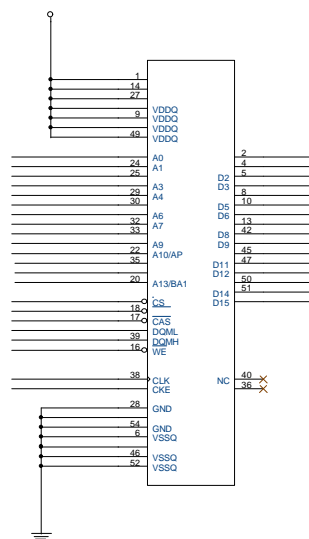
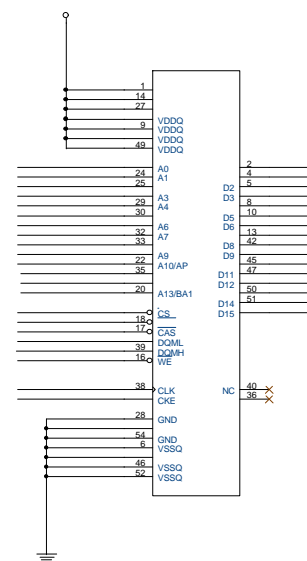
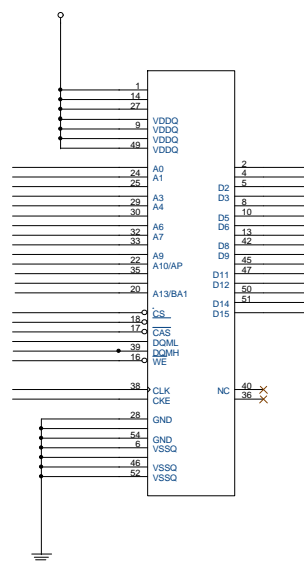
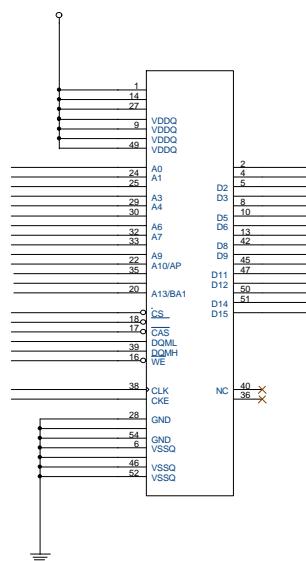
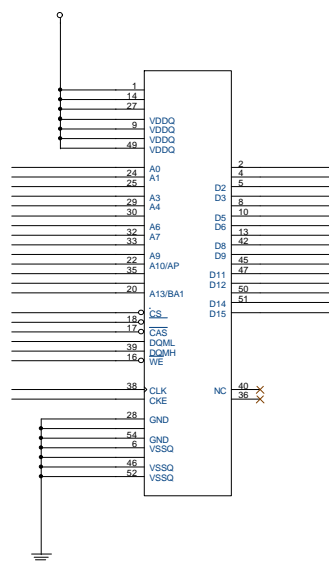
VIPD1

VIPD2

VIPD3

VIPD4

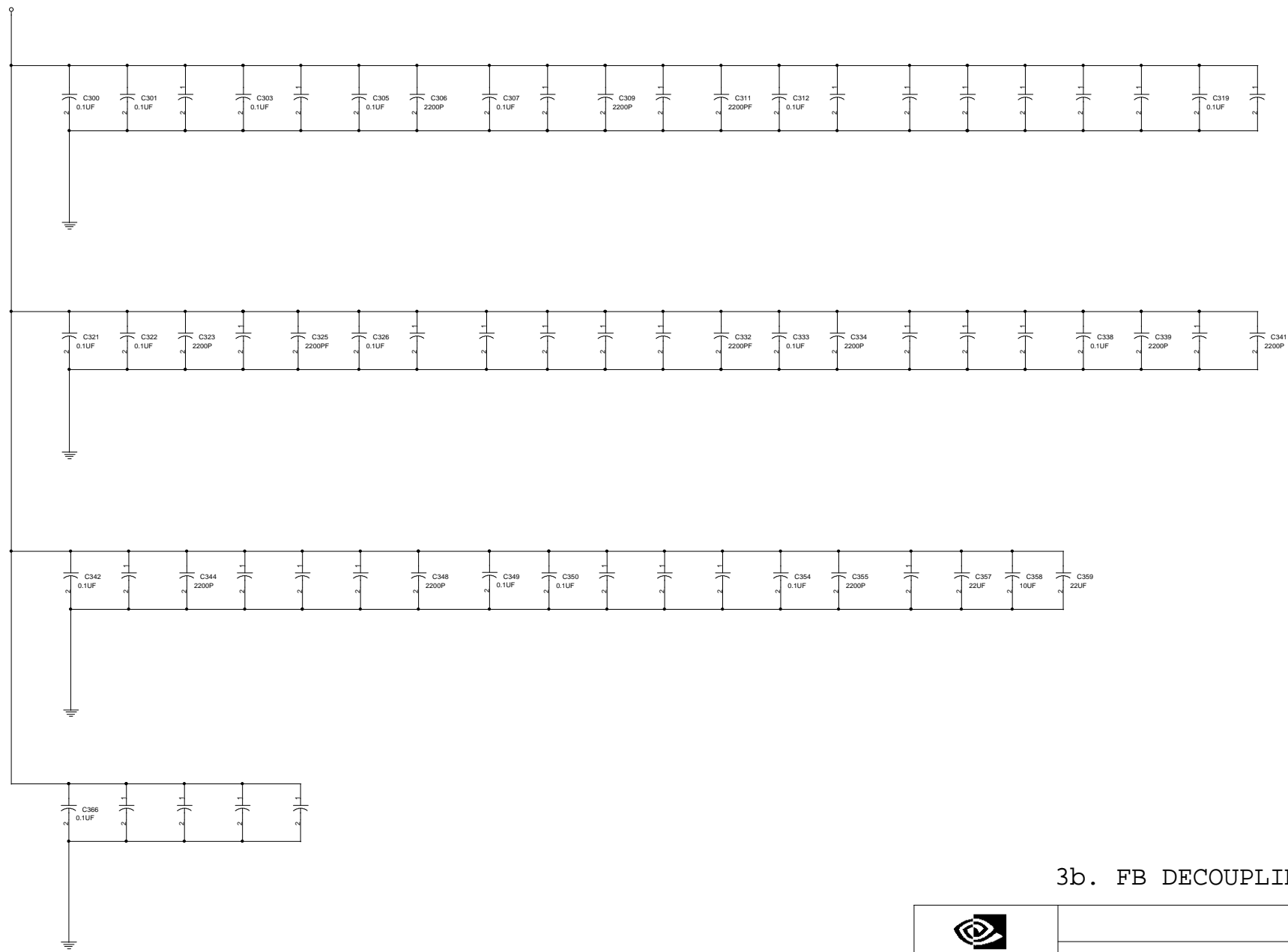
VIPD5




3c2 4MX16 SDRAM

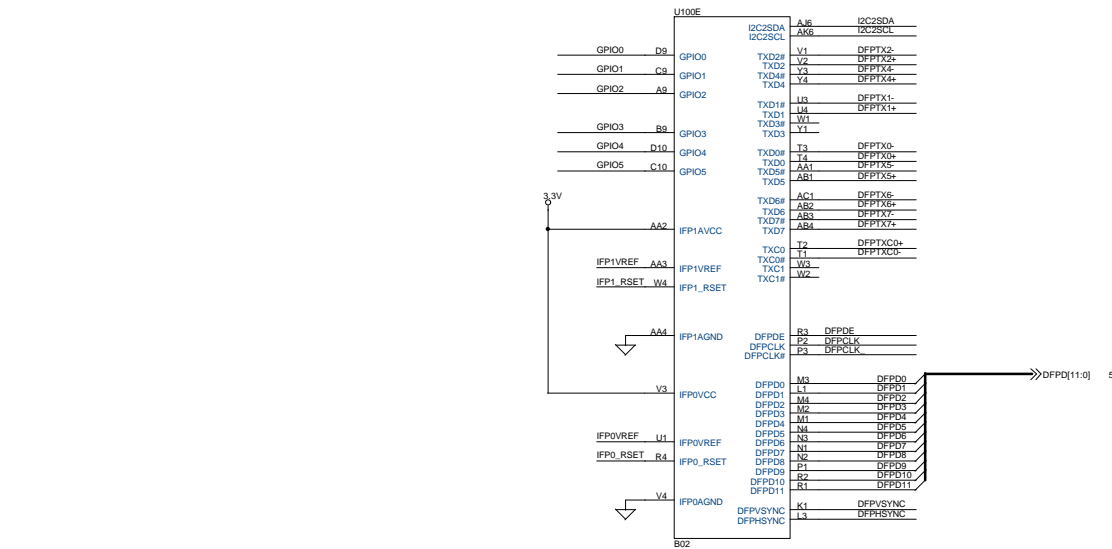


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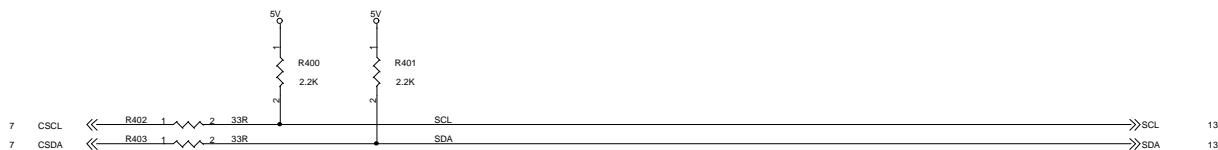
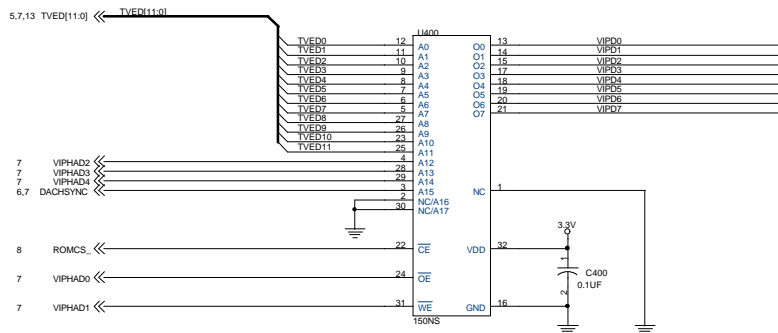


3b. FB DECOUPLING

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>>VIPD[7:0] 7



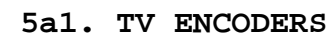
4a. ROM VIP & VIDEO IF



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