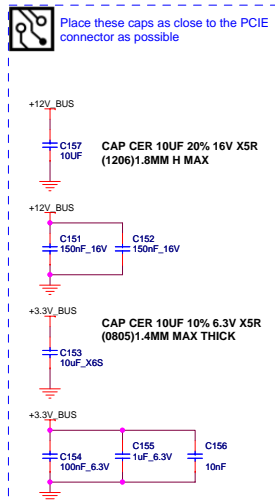




REDWOOD WOLVERINE



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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Title **RH REDWOOD GDDR5 512MB**

INC.	Advanced Micro Devices Inc. 1 Commerce Valley Drive East
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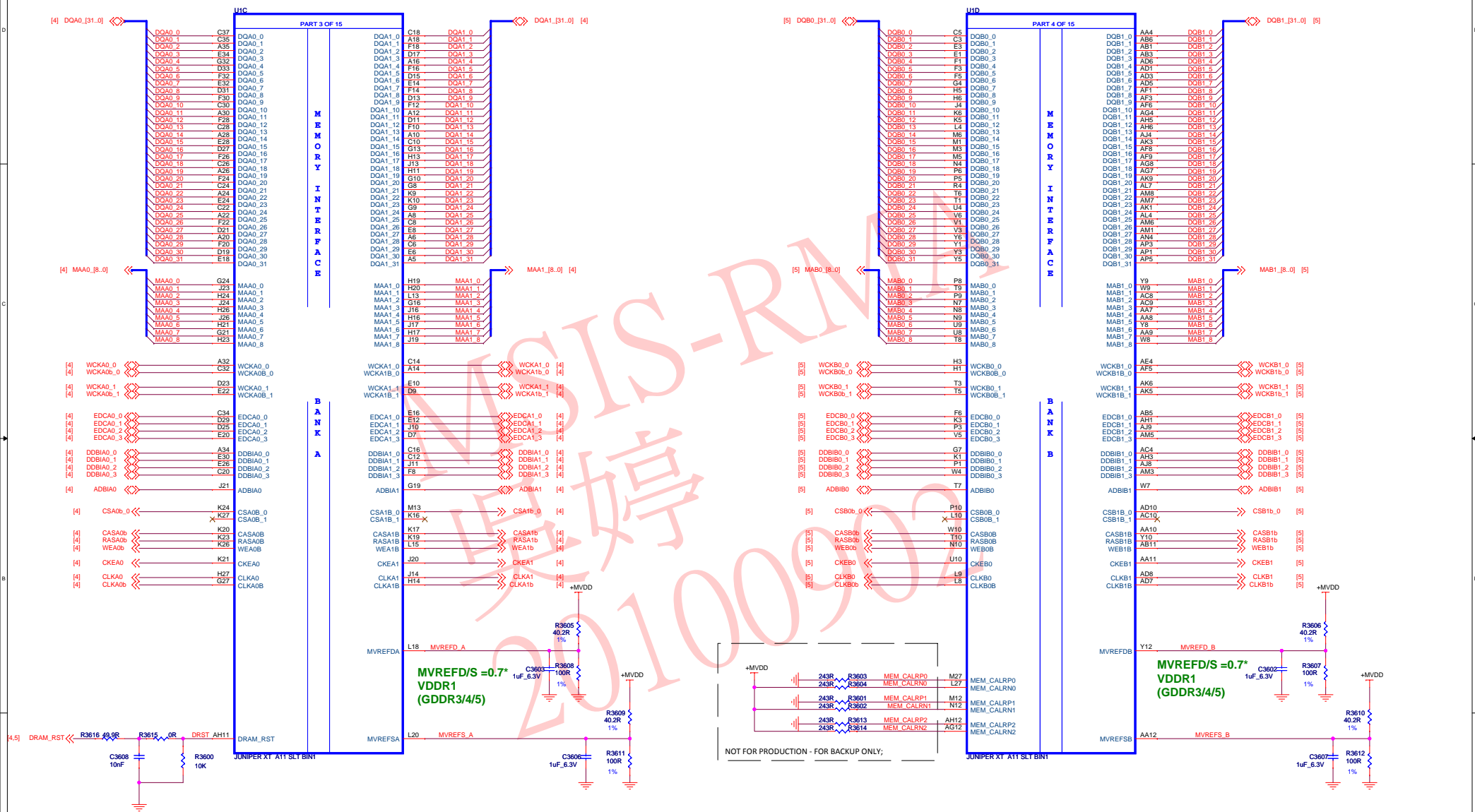


Date: Tuesday, December 29, 2009	Rev p1
Sheet 1 of 19	

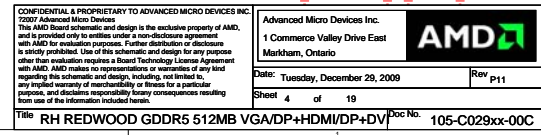
Title RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI Doi No. 105-C029xx-00C

[illegible]

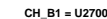
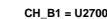
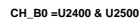
(3) REDWOOD MEM Interface Ch A&B



CH_A1 = U2300

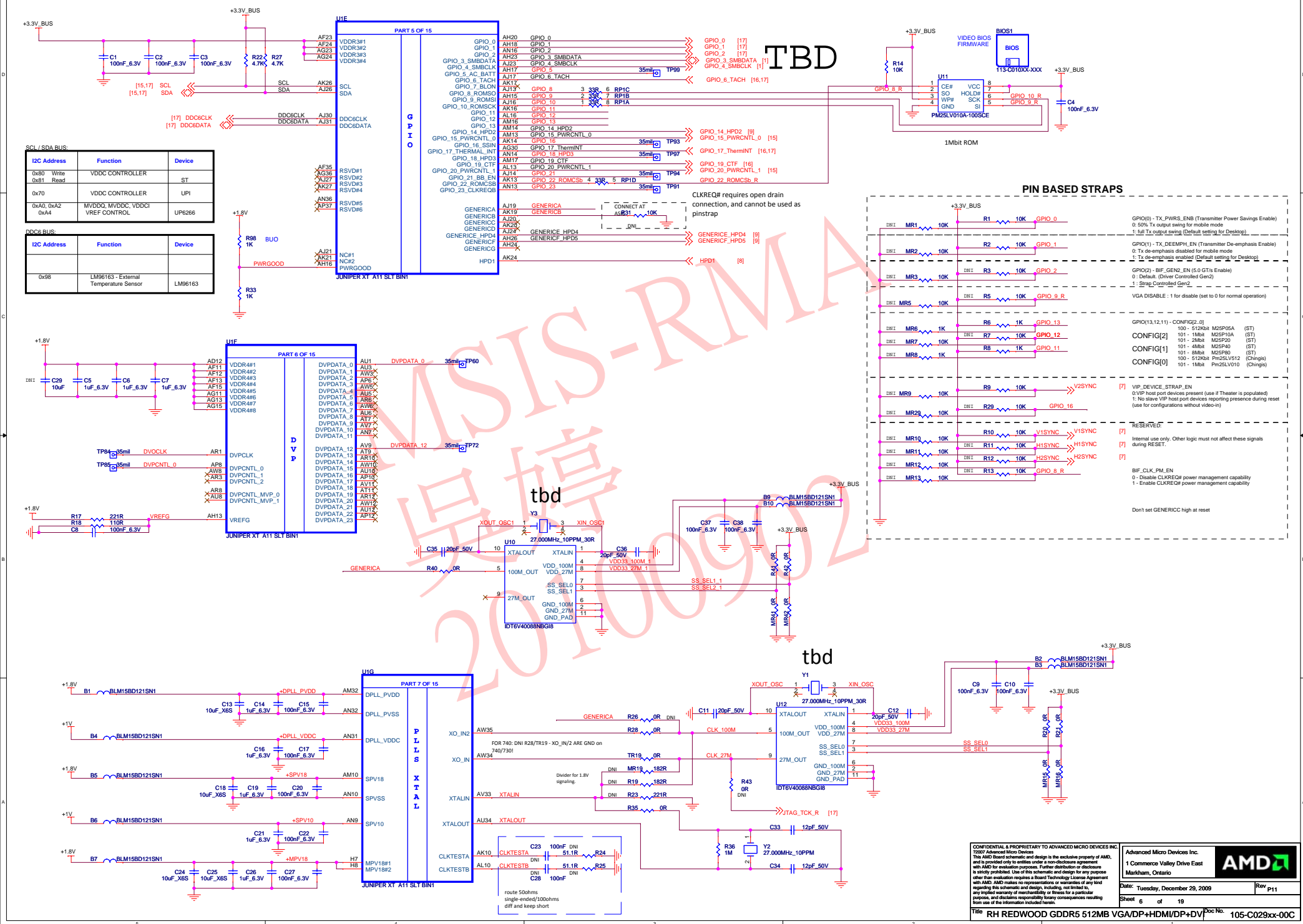


CH_B0 =U2400 & U2500

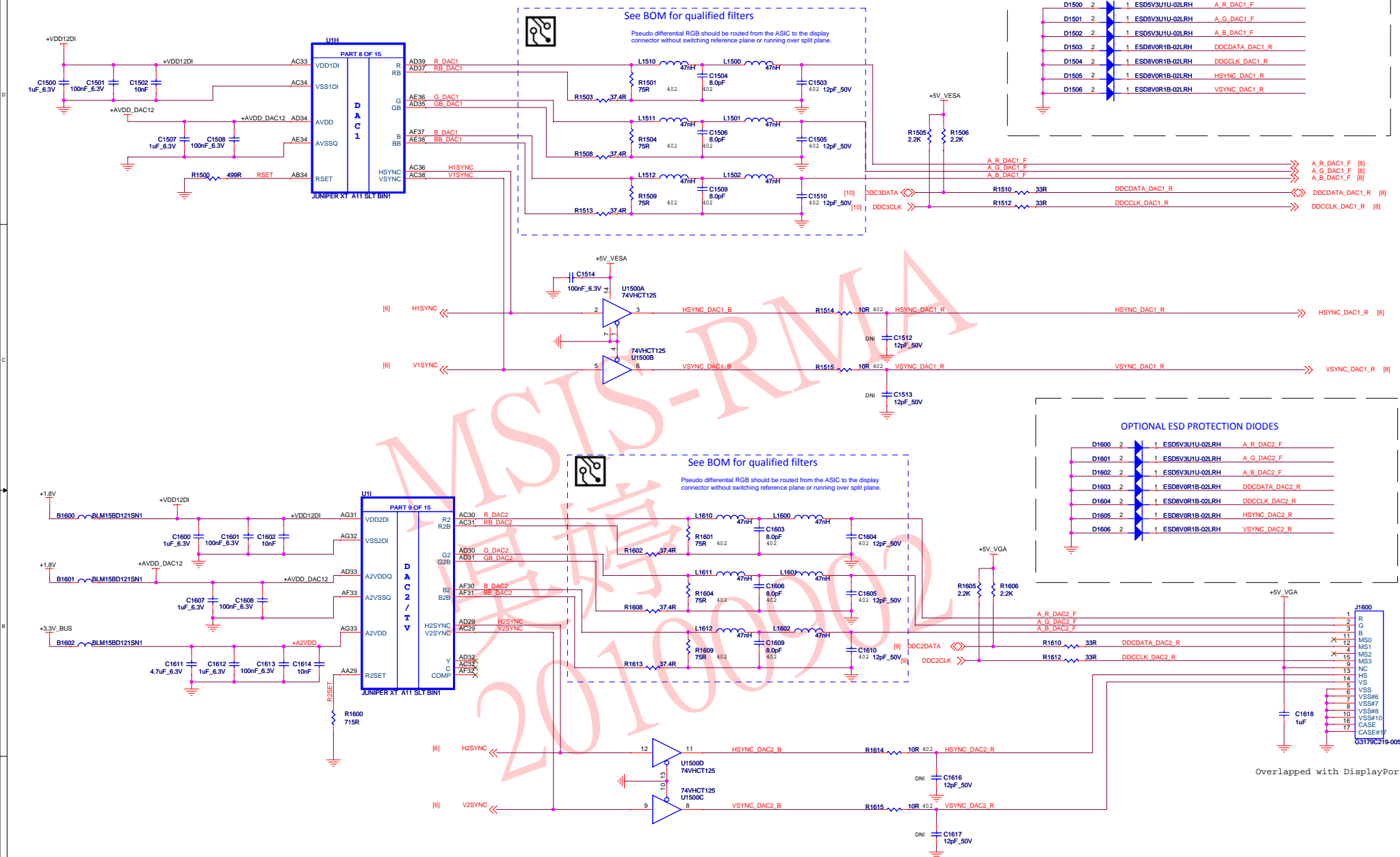


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<p>This AMD board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement.</p>	<p>1 Commerce Valley Drive East Markham, Ontario</p>
<p>This AMD board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement.</p>	<p>Date: <u>Tuesday, December 29, 2009</u> Rev <u>111</u></p>


5	4
(06) REDWOOD GPIOs Strap CF XTAL OSC	



(07) REDWOOD DAC1 and DAC2



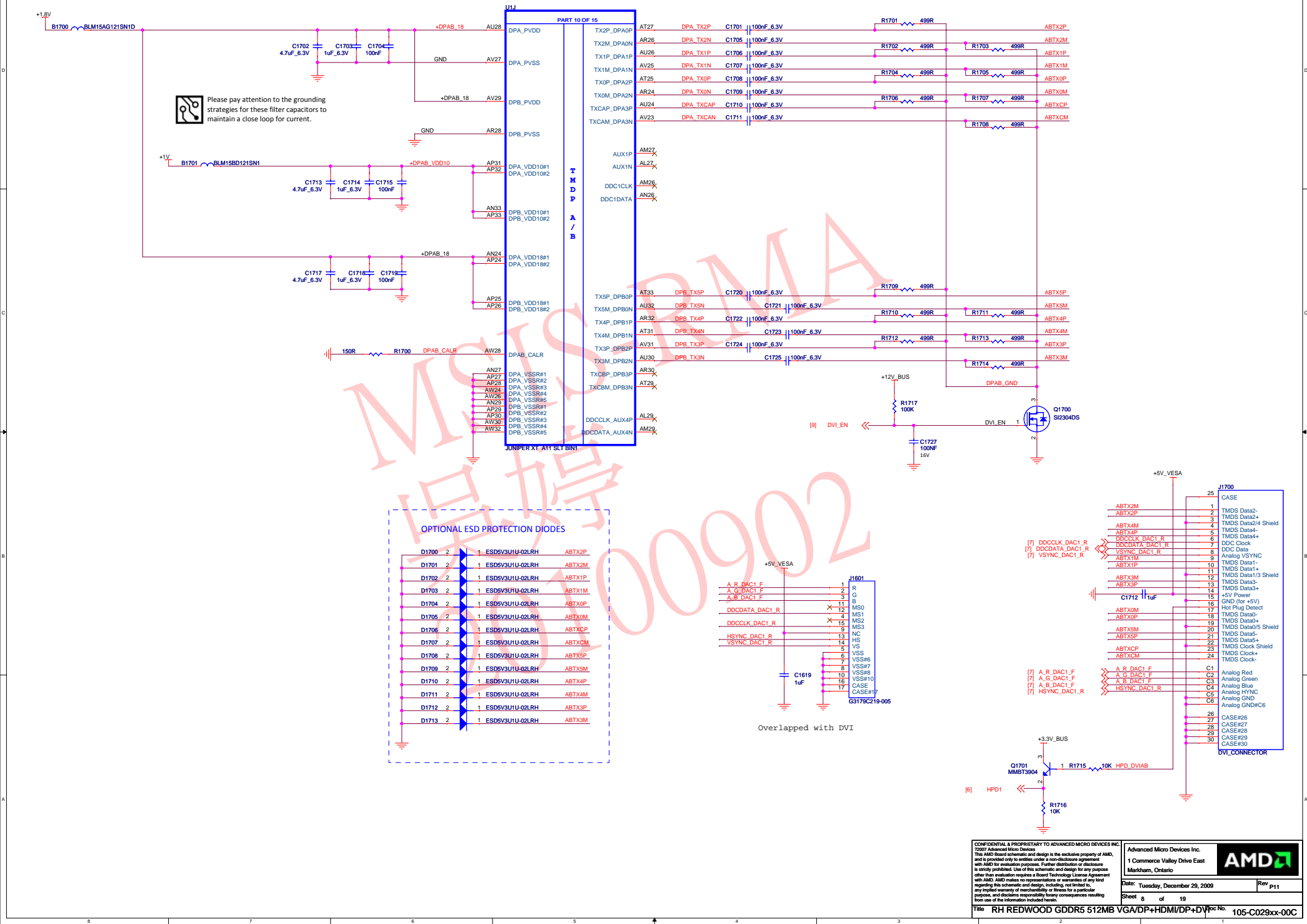
Overlapped with DisplayPort

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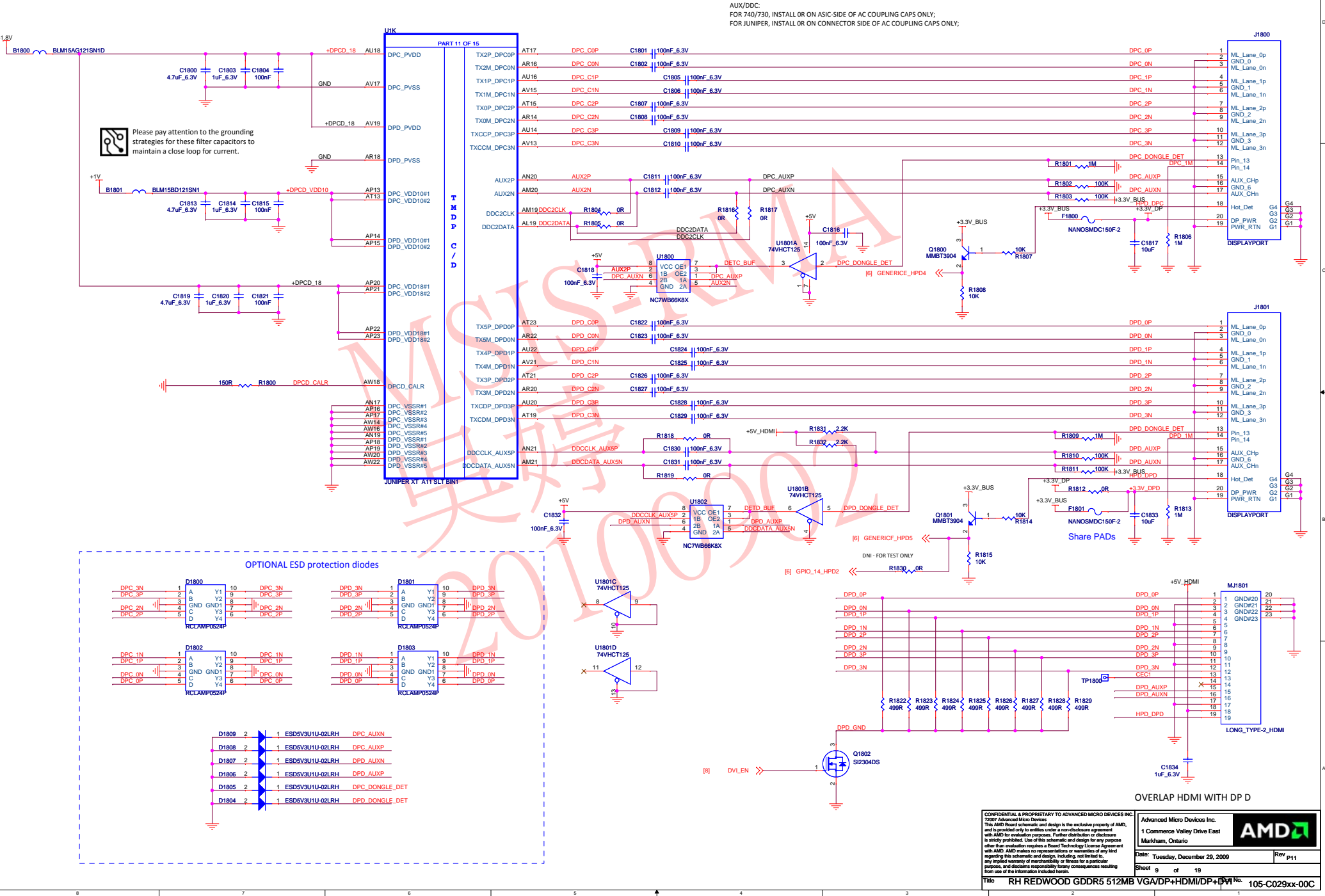
Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI	Doc No.	105-C029xx-000
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Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI	Doc No.	105-C029xx-000
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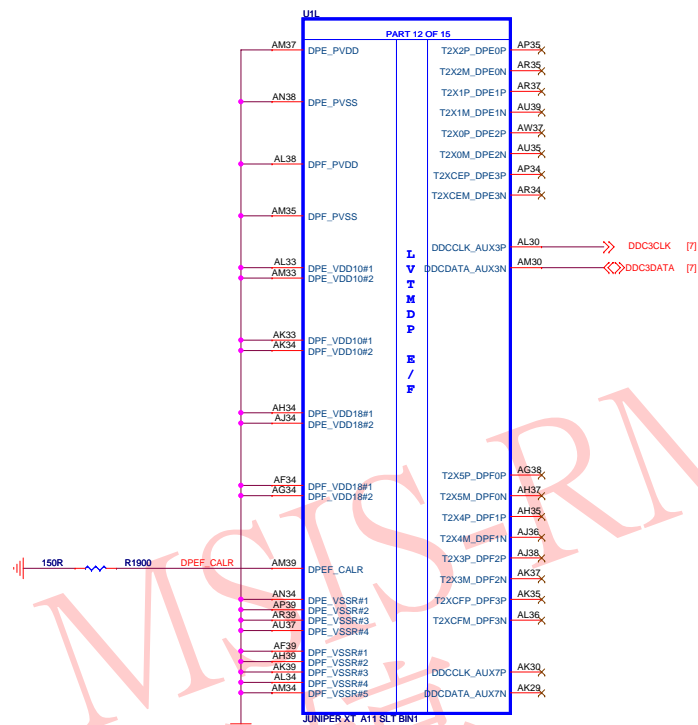
(08) REDWOOD TMDP A&B dDVI-I TOP



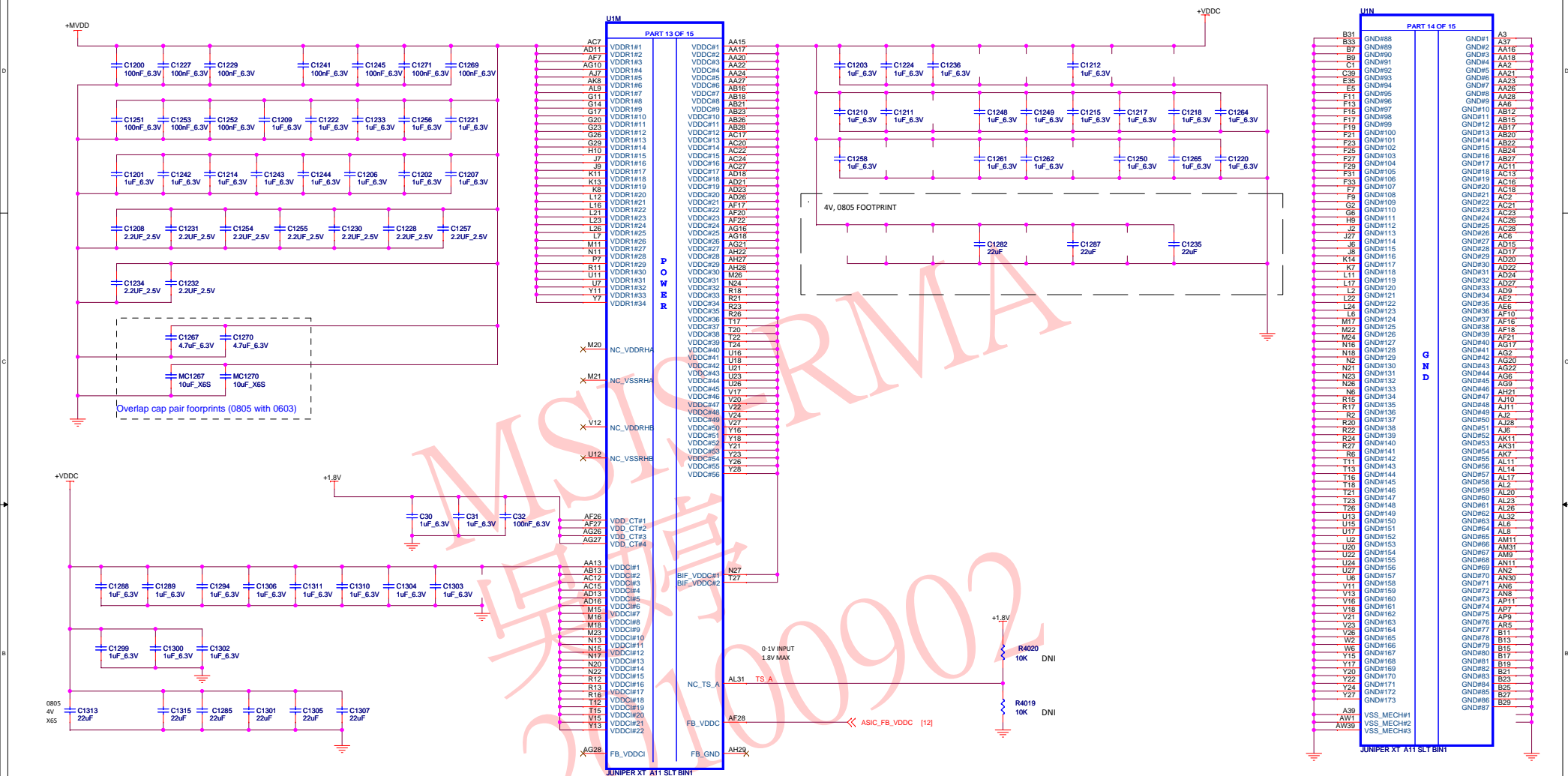
(09) REDWOOD Display Port C & Display Port/HDMI D



(10) REDWOOD LVTMDP E&F



(11) REDWOOD Power & GND



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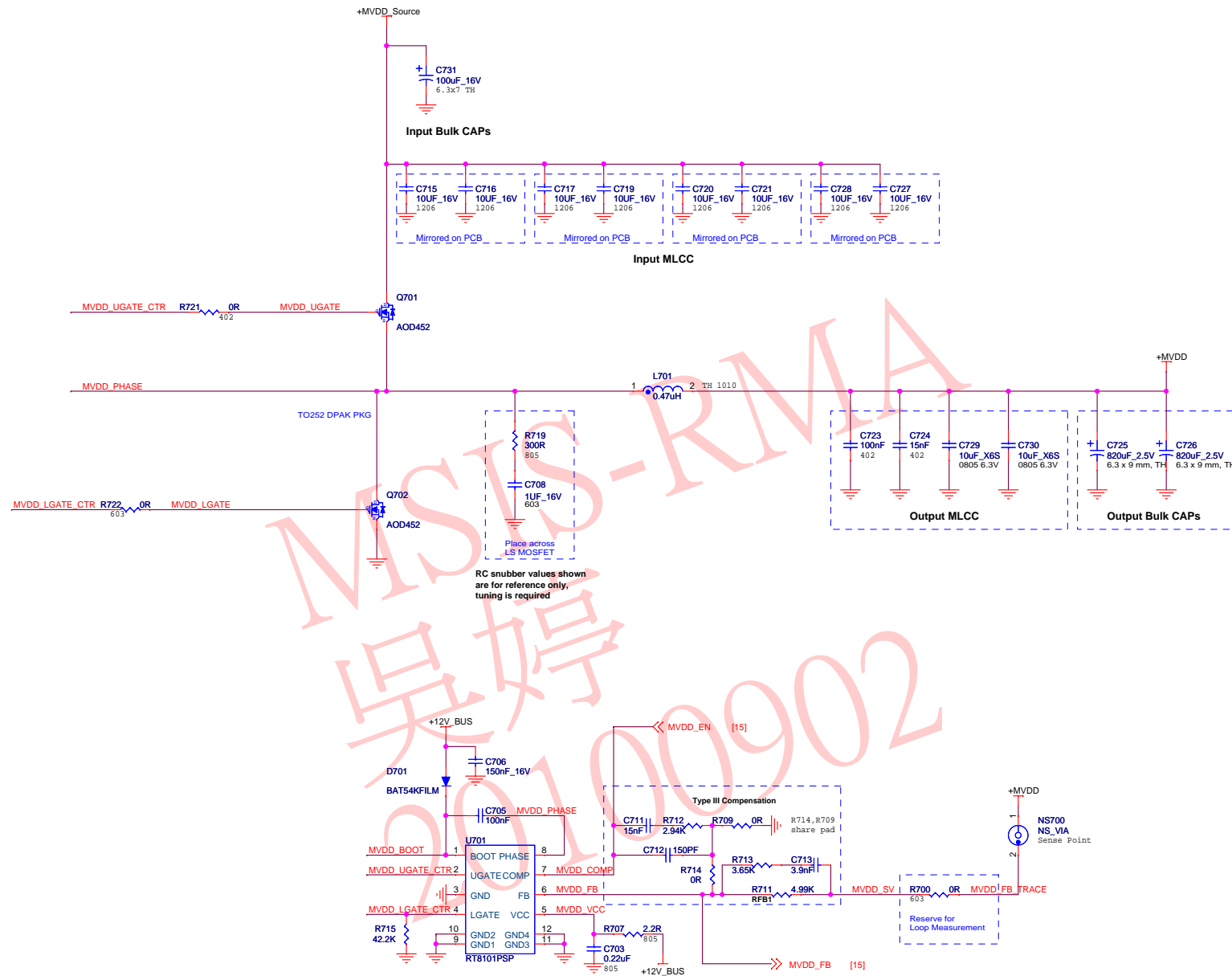
Date: Tuesday, December 29, 2009

Rev P11

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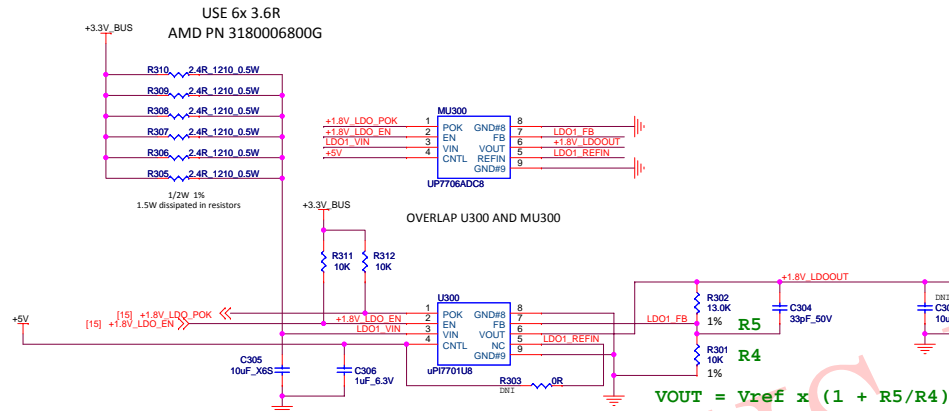
of 19

Title	RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DV	Doc No.	105-C029xx-000
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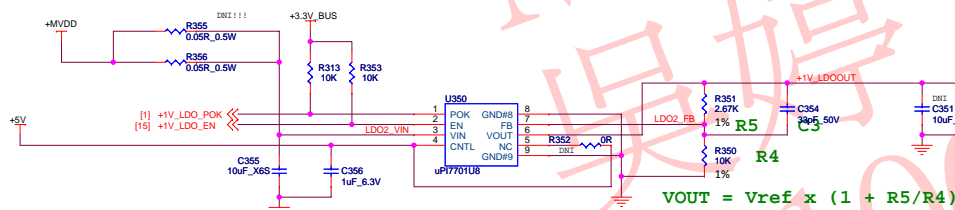


(15) Linear Regulators

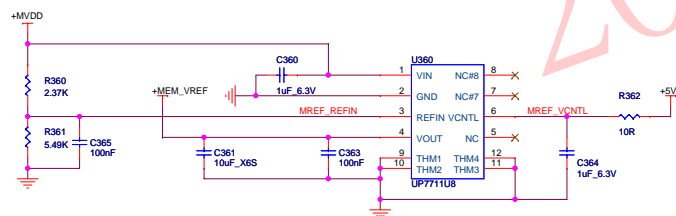
LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



Memory VREF: $V_{in} = MVDDQ$ $V_{out} = 0.7 \times MVDDQ$

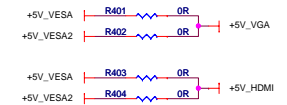
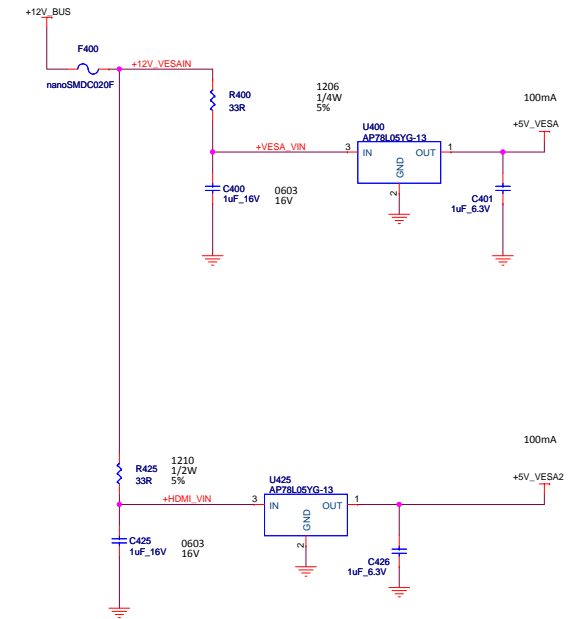


There must be one 100nF at each VREF pin
Place U360 (VIN - PIN#1) close to 10uF on MVDDQ in the middle point of memory devices

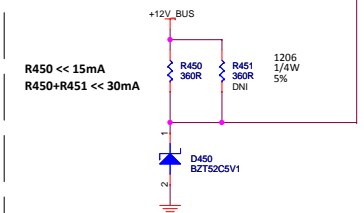
1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA

Regulators for +5V, +5V_VESA and +5V_HDMI

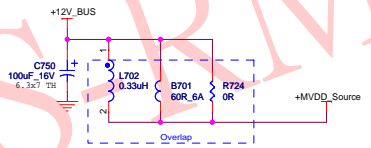
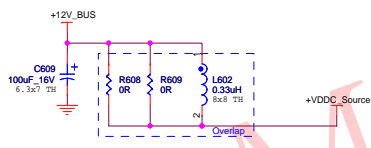
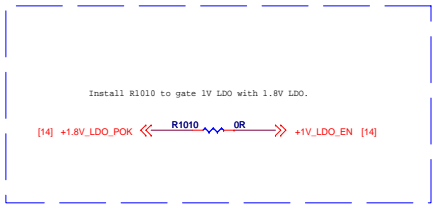
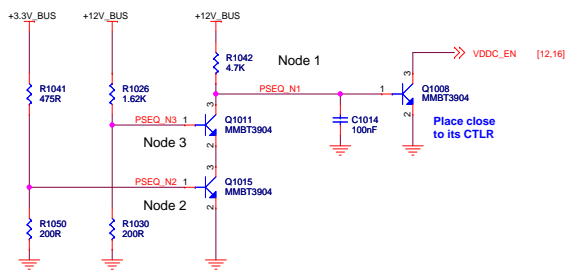


BACKUP OPTION FOR +5V REGULATOR

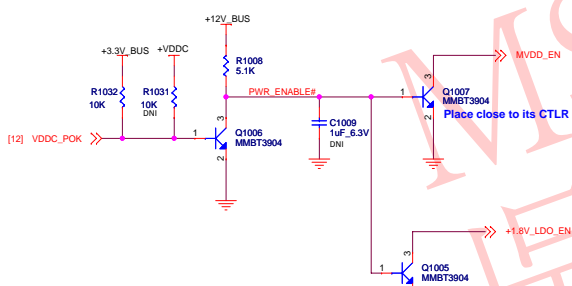


(16) Power Management - Power Gating and Dynamic Voltage Control

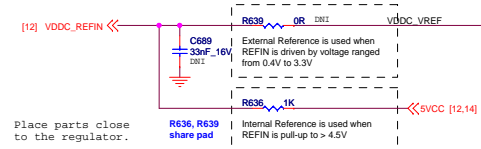
12V_BUS & 3V3_BUS POWER SEQUENCING



POWER SEQUENCING CIRCUIT

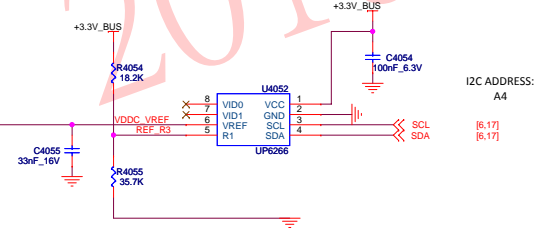


VDDC Reference Voltage Selection

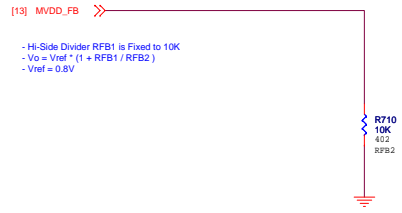


VDDC Vref Mode Selection			
Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC

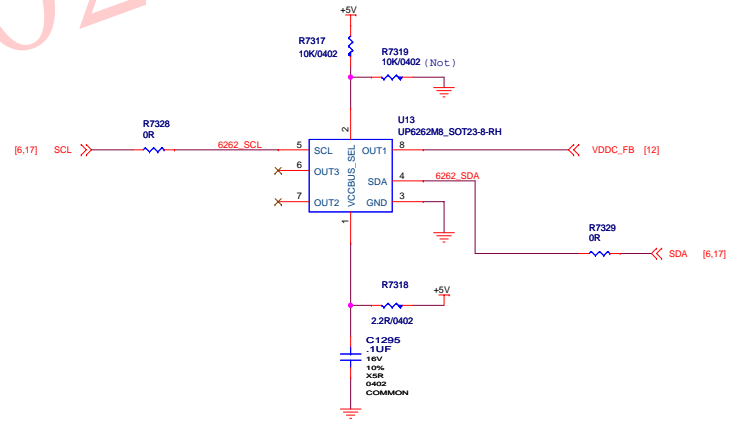
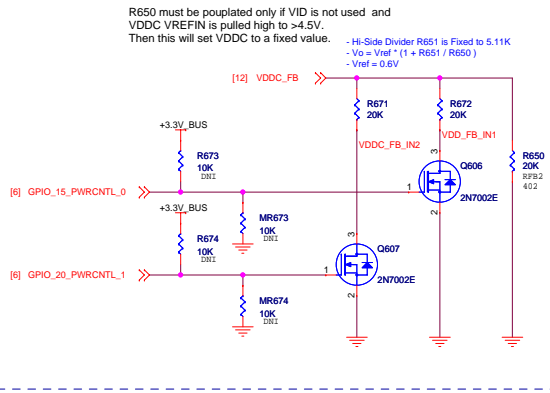
I2C VOLTAGE REFERENCE FOR VDDC (not for production)



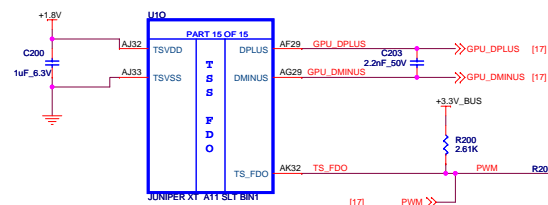
MVDD Low Side Divider



VDDC Low Side Divider

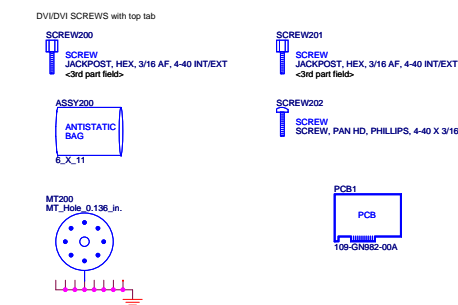
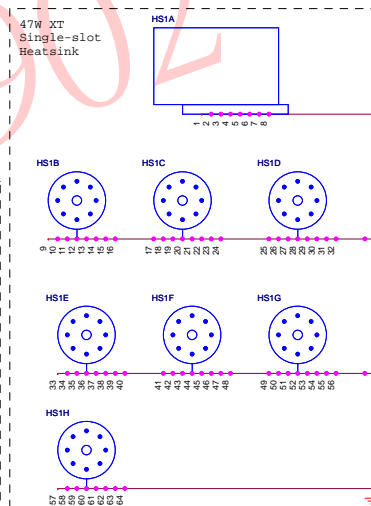
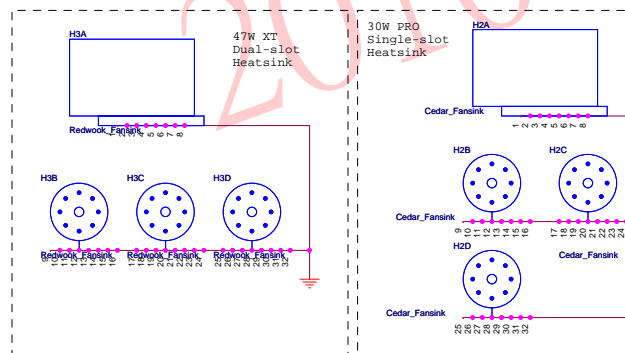
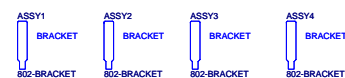
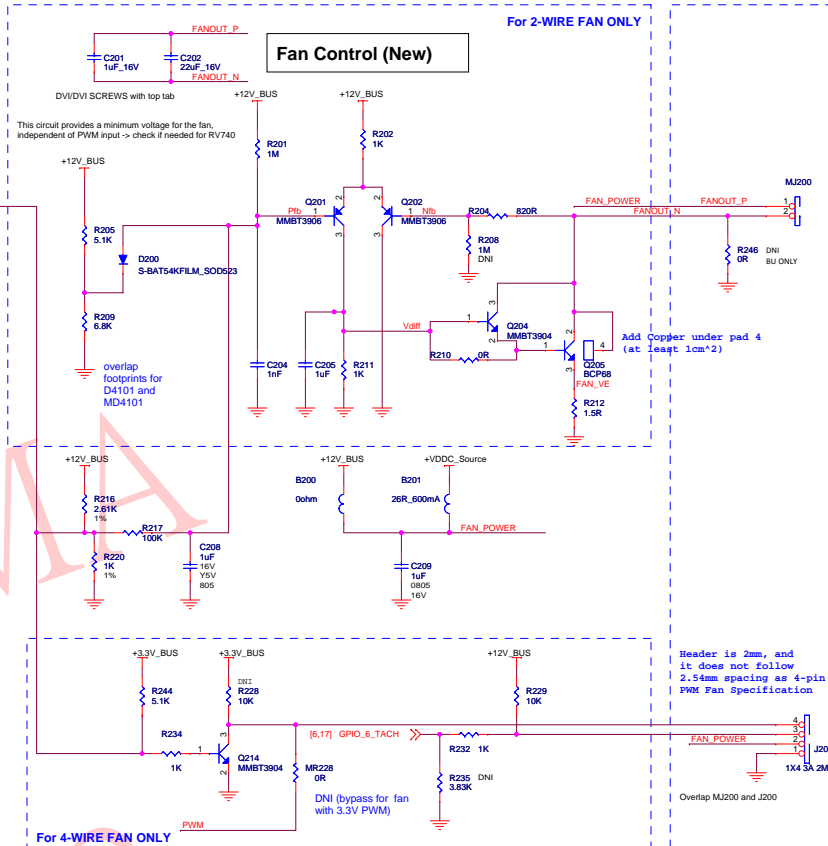
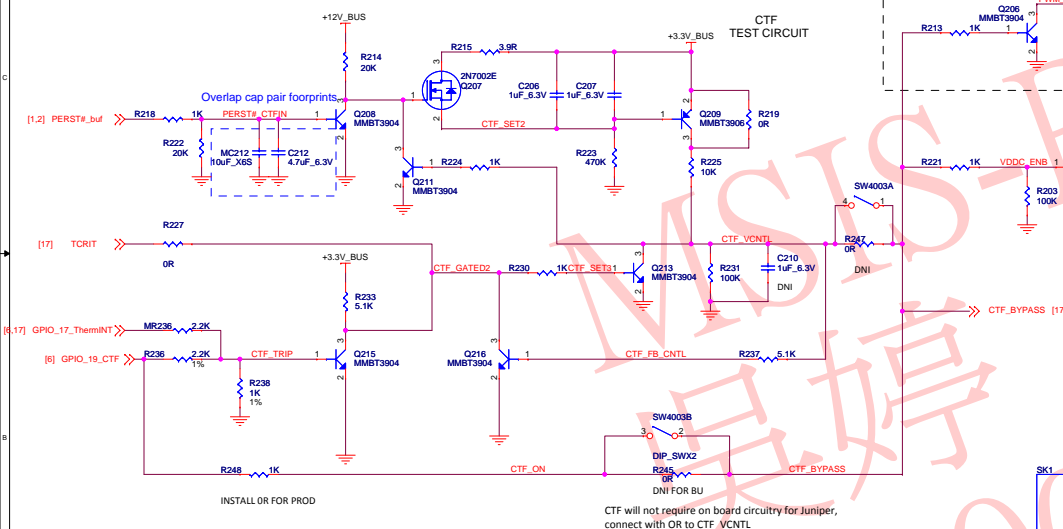



(19) Mechanical and Thermal Management



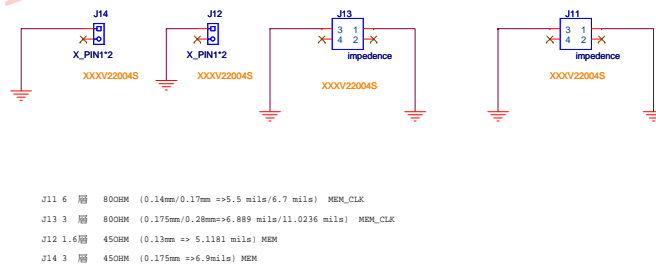
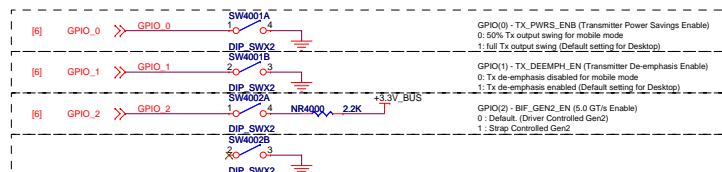
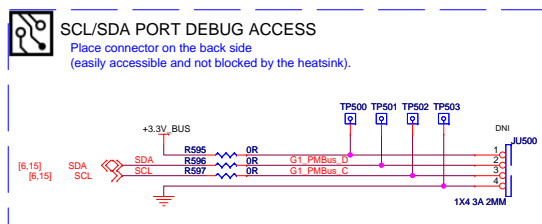
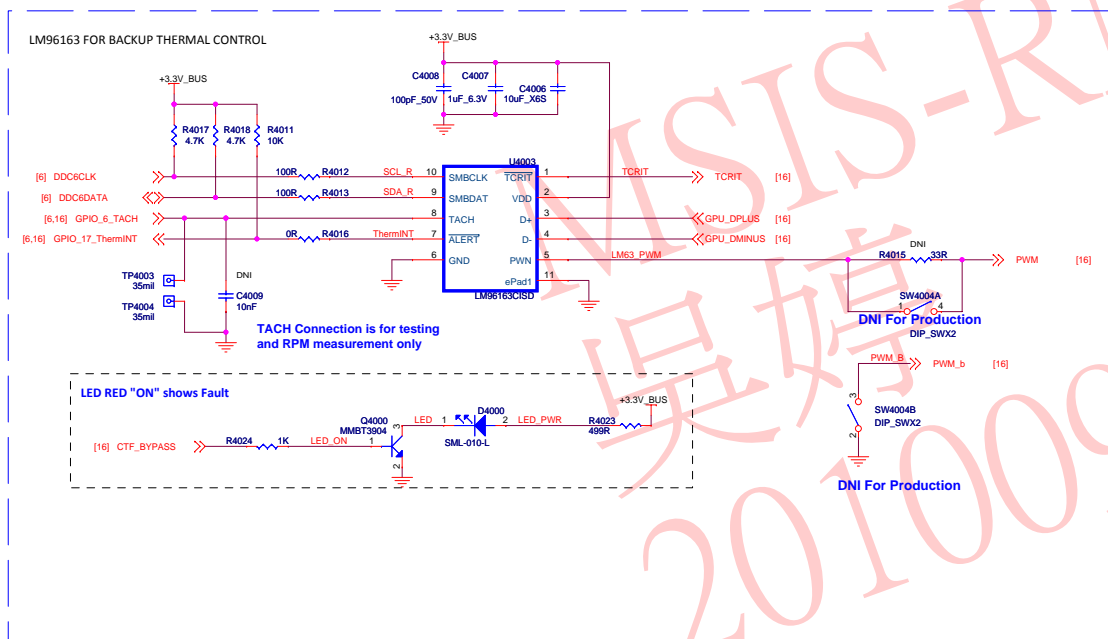
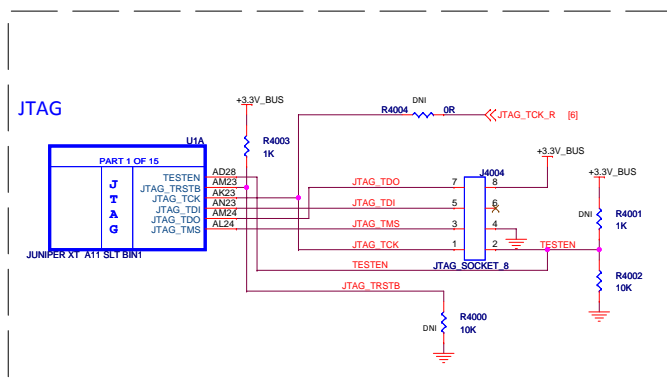
Warning: TS FDO is not 5V tolerant. MAX sink current 1.65mA

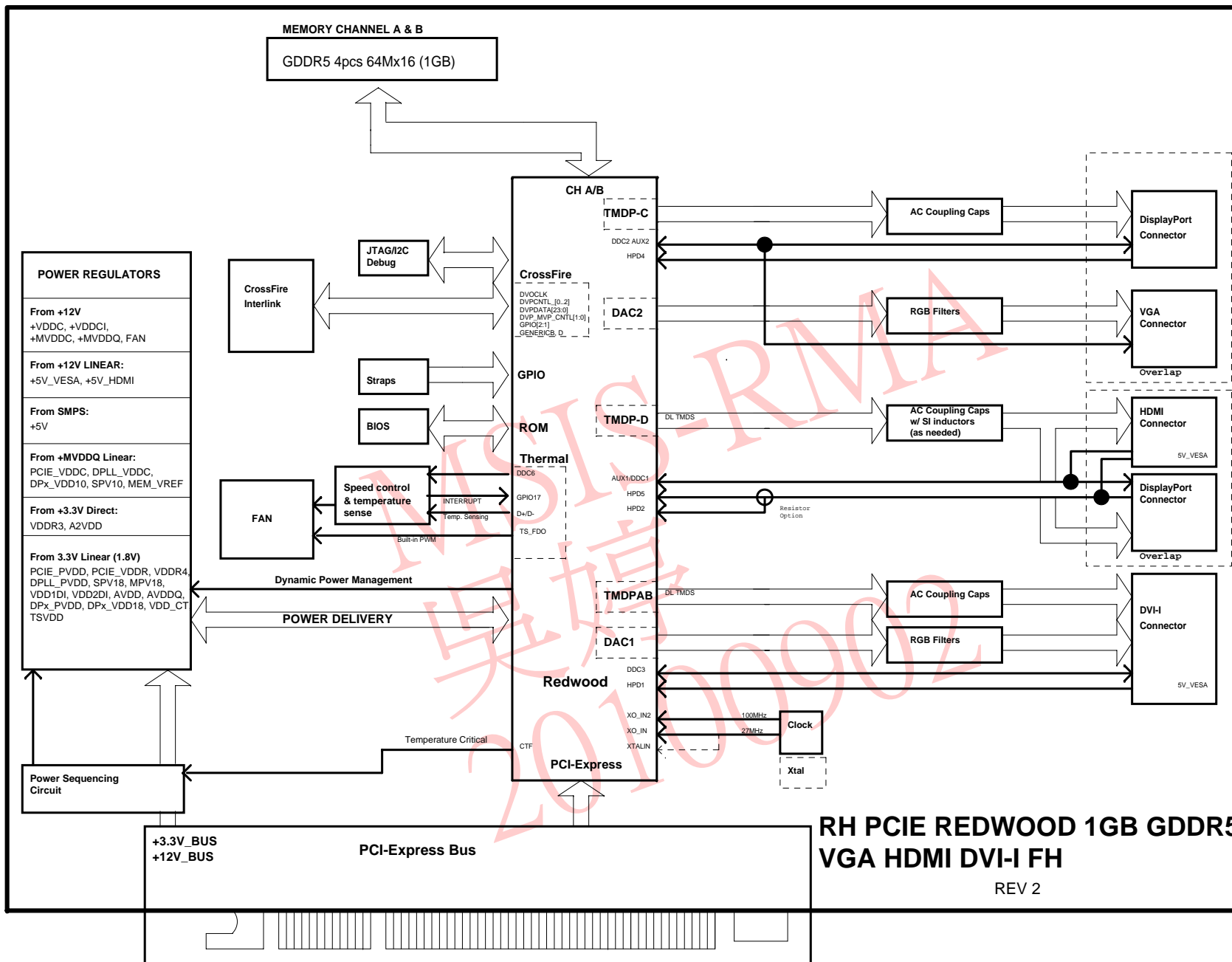
If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.



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Sheet: 16 of 19					
Title: RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVIpc No. 105-C029-001					

(19) Debug Circuits





**RH PCIE REDWOOD 1GB GDDR5
VGA HDMI DVI-I FH**
REV 2

<div>AMD</div>			Title		Schematic No.		Date:				
			RH REDWOOD GDDR5 512MB VGA/DP+HDMI/DP+DVI		105-C029xx-00C		Tuesday, December 29, 2009				
			REVISION HISTORY					NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.		Rev P11	
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION								
00	00A	2009/05/08	REDWOOD XT GDDR5 512MB - BASED ON C020 ;								
	00B	2009/10/12	1) SWAP DDC LINE TO FIX HDMI CERTIFICATE ISSUE 2) ADD ONE MORE SERIES RESISTOR ON DRAM_RST NET BASED ON SI TEAM SIMULATION RESULT 3) ADD 27MHz CLOCK TO JTAG CLK								
	00C	2009/12/02	1) ADD 1.8V I/O SHUT DOWN CIRCUIT								
	V220-4.0	2009/12/25	1)Modify Choke to SSC 2)Add POSCAP 1)Add uPI / uP6262								

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