

P361 A00 Base Design

P361-A00, G92, 8Mx32/16Mx32 GDDR3
DVI-I-DL, DVI-I-DL

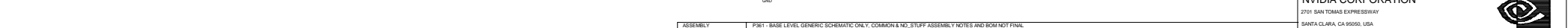
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REV	VARIANT	NUPN	ASSEMBLY
0	BASE	600-10361-base-000	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU001	600-10361-0001-000	P361 G92-280B1 1024MB GDDR3 16Mx32 DVI-I+DVI-I
2	SKU002	600-10361-0002-000	P361 G92-280B1 512MB GDDR3 16Mx32 DVI-I+DVI-I
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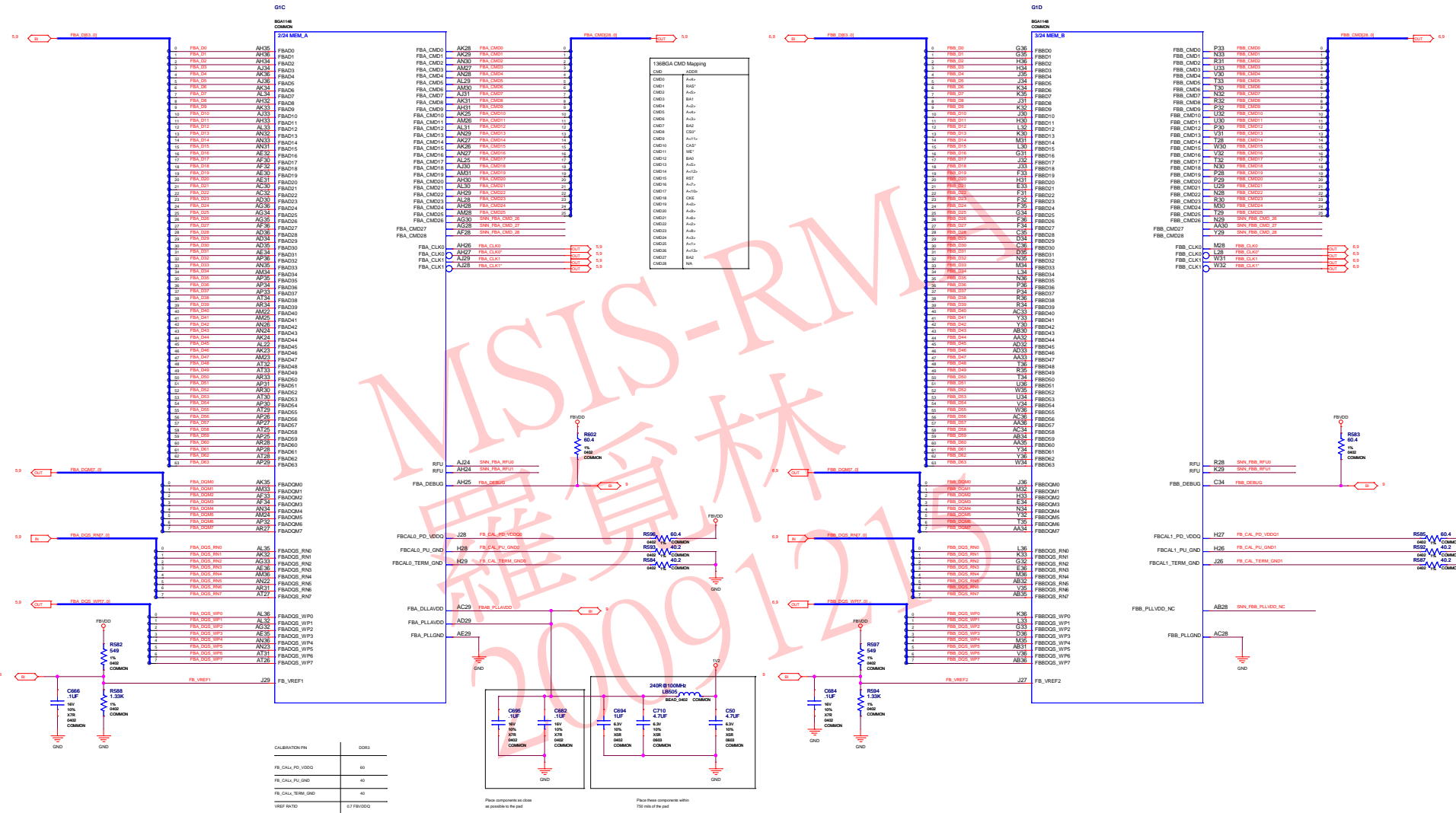
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ASSEMBLY	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: GPU Partition A/B

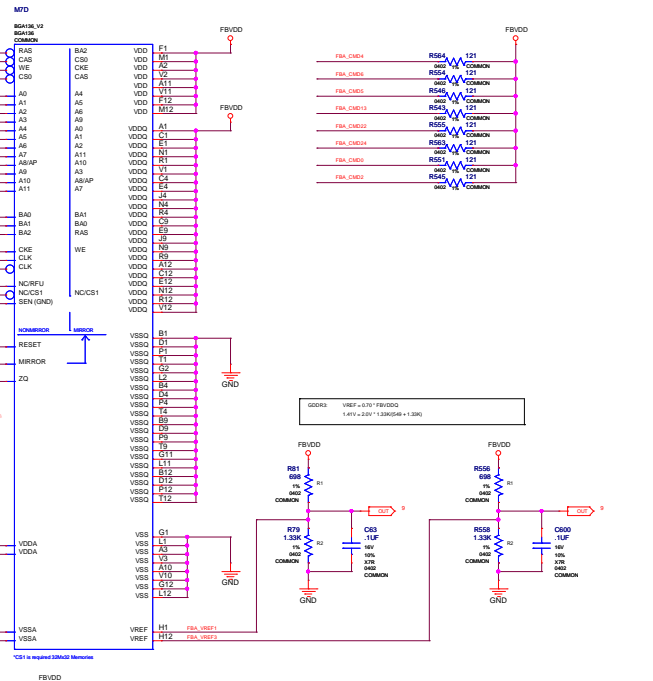
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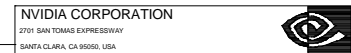
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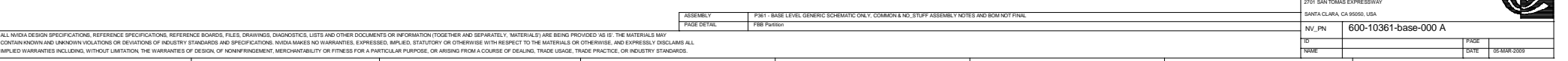


Decoupling for FBA Hi

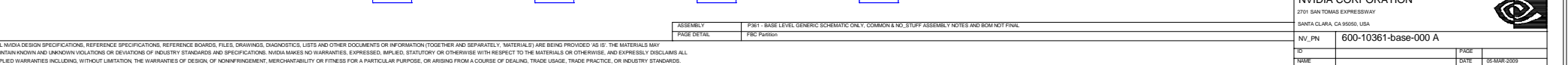


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MODE	MODE
136GBA CMD Mapping	
BA0*	CM01
CAS*	CM10
WE*	CM11
CS0*	CM08
BA2	CM07
BA0	CM12
BA1	CM03
A1-Q0	CM14
A1-Q1	CM15
A1-r	CM05
SA-Q0	CM22
SA-Q1	CM24
SA-r0	CM04
SA-r1	CM02
1A-Q0	CM04
1A-Q1	CM06
1A-r0	CM05
1A-r1	CM13
A-B0	CM21
A1-r2	CM16
A1-r3	CM23
A-B1	CM20
A1-A0	CM17
111	CM19
CHE	CM18
RST	CM15



138BGA CMD Mapping	138MAP
BA0P	CM01
BA0F	CM10
BA0E	CM11
BA0D	CM04
BA0C	CM07
BA0B	CM02
BA0A	CM03
Au0A	CM04
Au0B	CM05
Au0C	CM06
Au0D	CM07
Au0E	CM08
Au0F	CM09
Au0G	CM10
Au0H	CM11
Au0I	CM12
Au0J	CM13
Au0K	CM14
Au0L	CM15
Au0M	CM16
Au0N	CM17
Au0O	CM18
BA0P	CM01
BA0F	CM10

138BGA CMD Mapping	138MAP
BA0P	CM01
BA0F	CM10
BA0E	CM11
BA0D	CM04
BA0C	CM07
BA0B	CM02
BA0A	CM03
Au0A	CM04
Au0B	CM05
Au0C	CM06
Au0D	CM07
Au0E	CM08
Au0F	CM09
Au0G	CM10
Au0H	CM11
Au0I	CM12
Au0J	CM13
Au0K	CM14
Au0L	CM15
Au0M	CM16
Au0N	CM17
Au0O	CM18
BA0P	CM01
BA0F	CM10

Close Term MUST BE PLACED as close as possible to the BGA memory pin
Minimize STUB length!

Close Term MUST BE PLACED as close as possible to the BGA memory pin
Minimize STUB length!

C31 is required 25000 Mhz

C31 is required 25000 Mhz

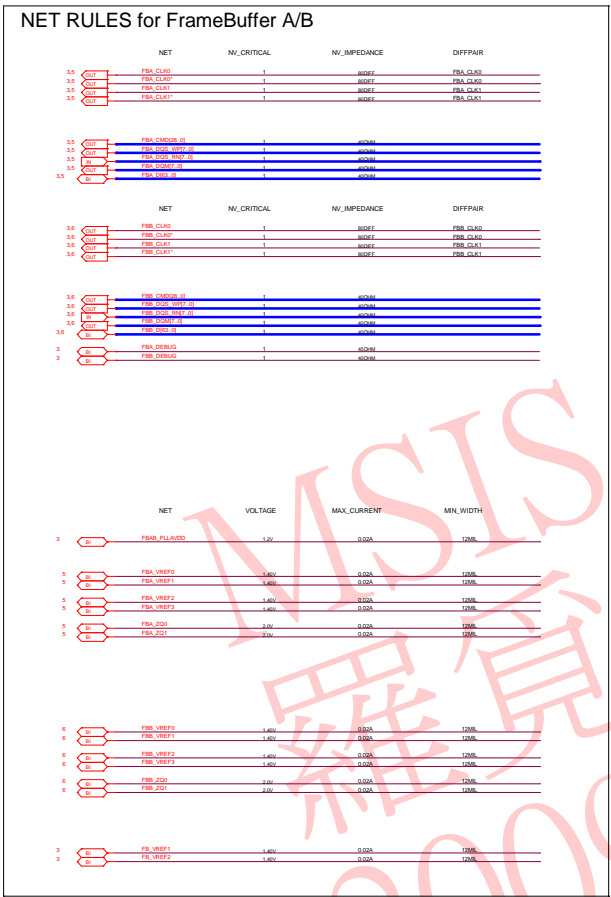
Decoupling for FBD Lo

Decoupling for FBD Hi

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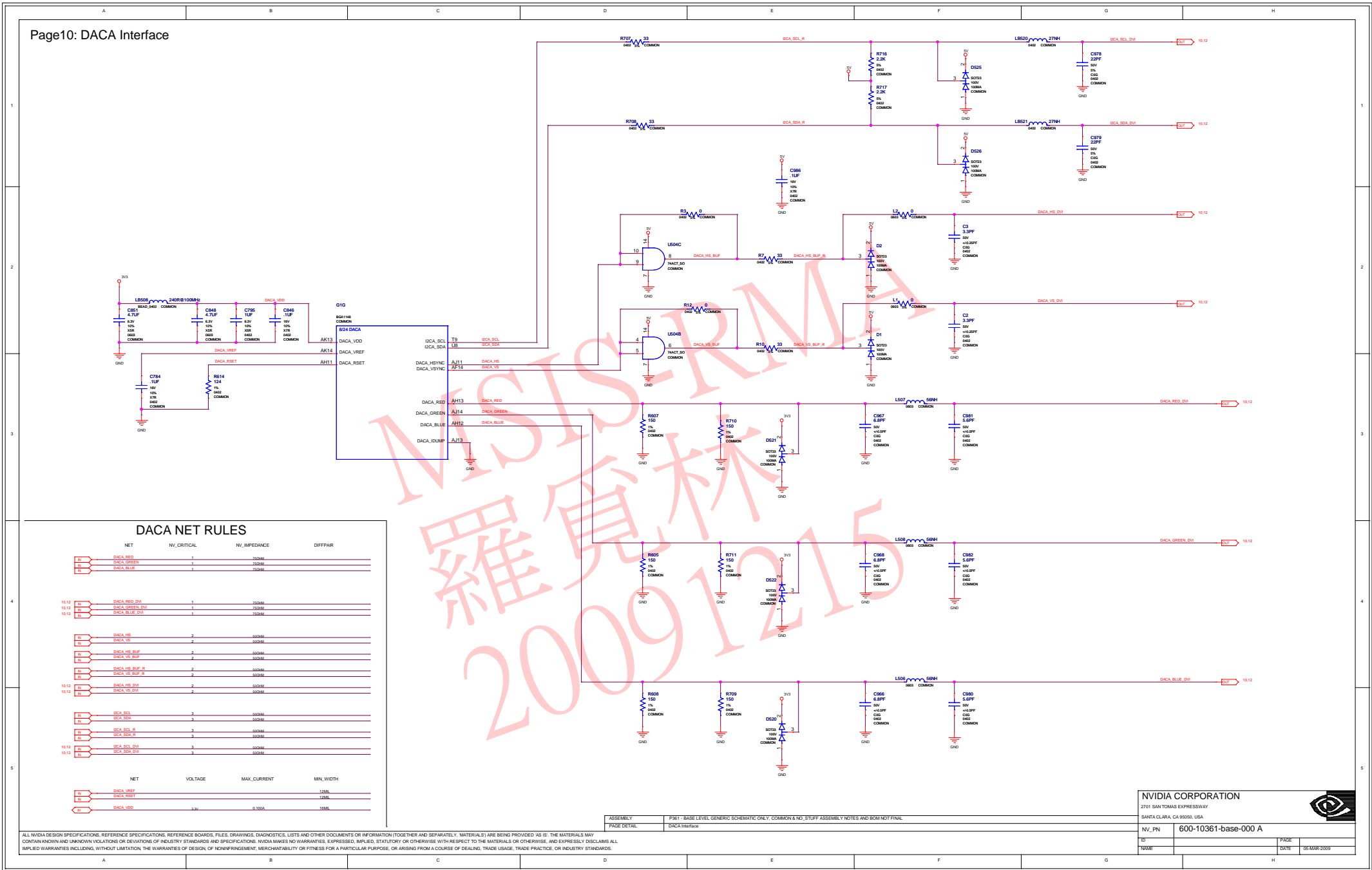
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Note: FB traces on top and bottom layers are routed with 45ohm impedance for increasing spacing.
Internal FB traces are routed with 40ohm impedance.

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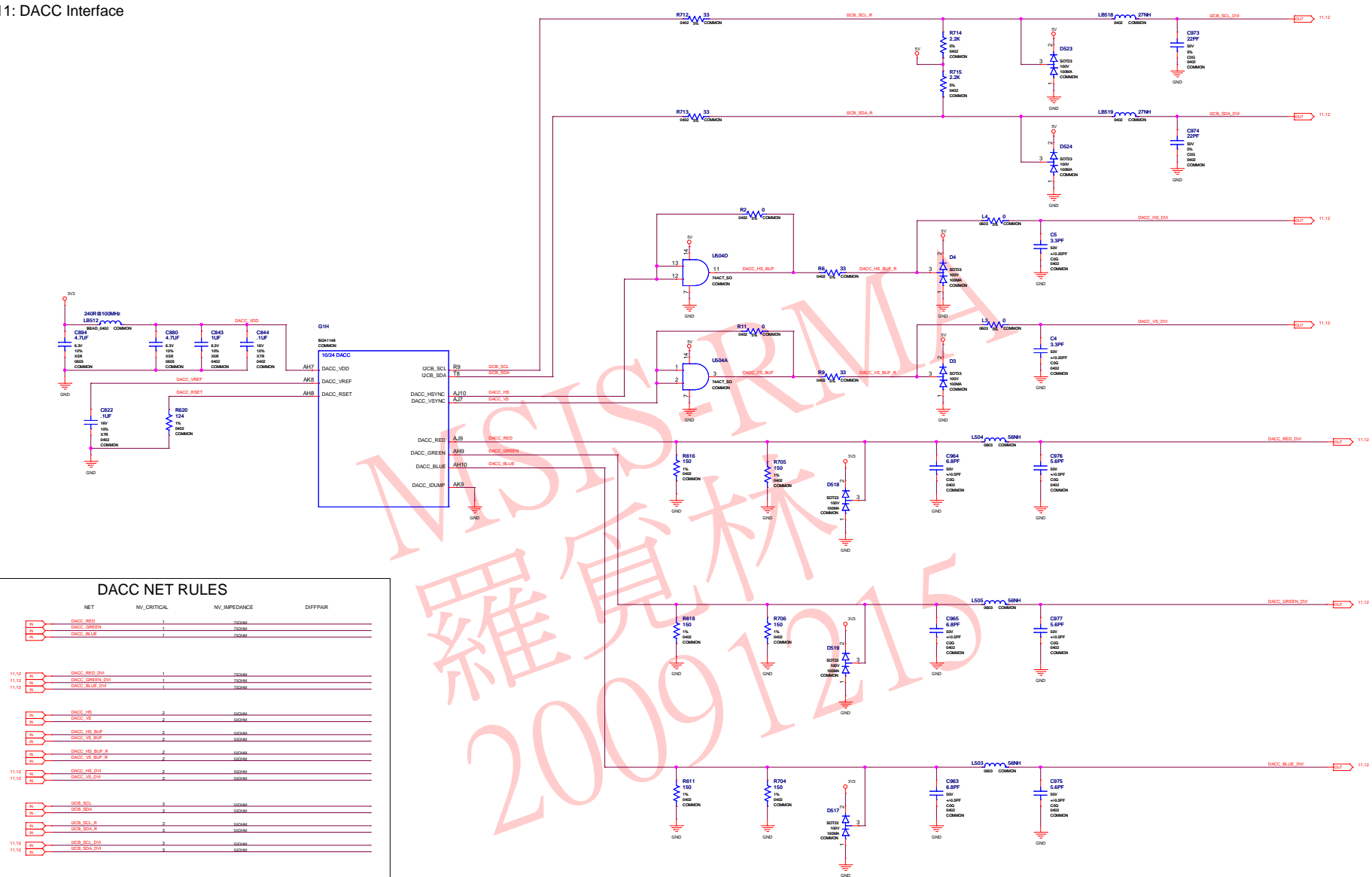
Page10: DACA Interface



DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
10.12 DACA_RED	1	750M	
10.12 DACA_GREEN	1	750M	
10.12 DACA_BLUE	1	750M	
10.12 DACA_RED_DV	1	750M	
10.12 DACA_GREEN_DV	1	750M	
10.12 DACA_BLUE_DV	1	750M	
10.12 DACA_HS	2	500M	
10.12 DACA_VS	2	500M	
10.12 DACA_HS_BUF	2	500M	
10.12 DACA_VS_BUF	2	500M	
10.12 DACA_HS_BUF_B	2	500M	
10.12 DACA_VS_BUF_B	2	500M	
10.12 DACA_HS_DV	2	500M	
10.12 DACA_VS_DV	2	500M	
10.12 DACA_SCL	3	500M	
10.12 DACA_SDA	3	500M	
10.12 DACA_SCL_B	3	500M	
10.12 DACA_SDA_B	3	500M	
10.12 DACA_SCL_DV	3	500M	
10.12 DACA_SDA_DV	3	500M	
10.12 DACA_VREF		100M	
10.12 DACA_VREF		100M	
10.12 DACA_VREF		100M	

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DACC NET RULES

	NET	NV_CRITICAL	NV_IMPEDIANCE	DIFF_PAIR
B	DACC_RED	1	100Ω	
B	DACC_GREEN	1	100Ω	
B	DACC_BLUE	1	100Ω	
11,12	DACC_RED_DN	1	100Ω	
11,12	DACC_GREEN_DN	1	100Ω	
11,12	DACC_BLUE_DN	1	100Ω	
B	DACC_HS	2	100Ω	
B	DACC_LS	2	100Ω	
B	DACC_HS_BUF	2	100Ω	
B	DACC_LS_BUF	2	100Ω	
B	DACC_HS_BUF_P	2	100Ω	
B	DACC_LS_BUF_P	2	100Ω	
11,12	DACC_HS_DN	2	100Ω	
11,12	DACC_LS_DN	2	100Ω	
B	DCB_SCL	3	100Ω	
B	DCB_SDA	3	100Ω	
B	DCB_SCL_P	3	100Ω	
B	DCB_SDA_P	3	100Ω	
11,12	DCB_SCL_DN	3	100Ω	
11,12	DCB_SDA_DN	3	100Ω	
	NET	VOLTAGE	MAX_CURRENT	MIN_LENGTH
B	DACC_HREF			120Ω
B	DACC_HREFP			120Ω
B	DACC_GND	3.3V	0.100A	100Ω

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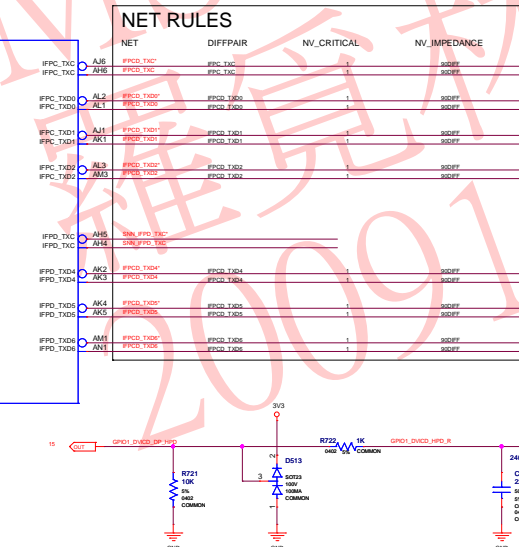
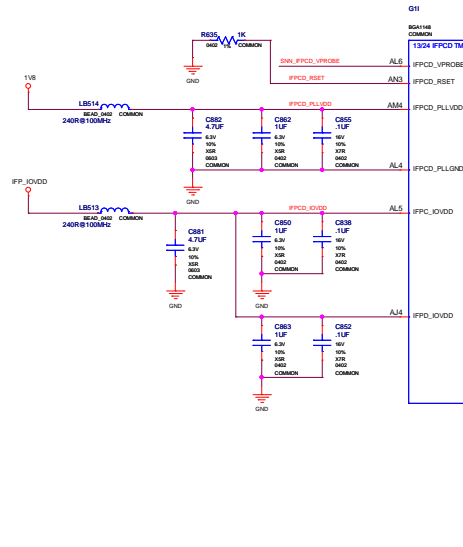
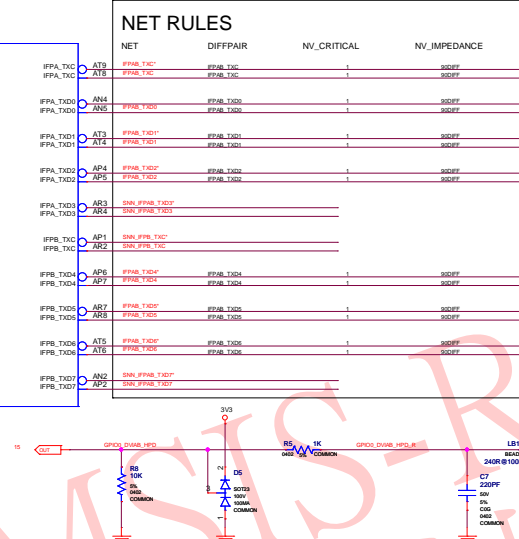
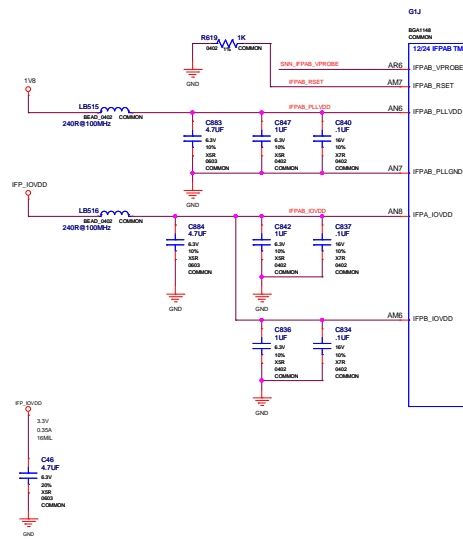
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PAGE DETAIL	DACC Interface

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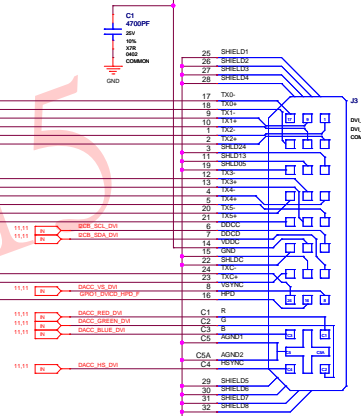
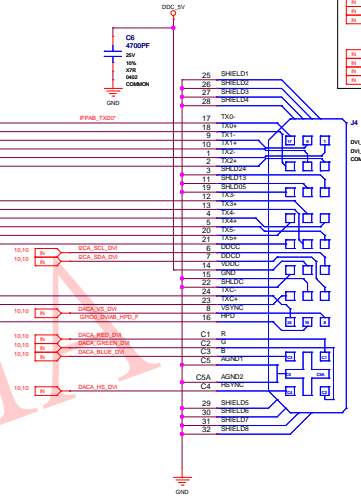
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IFPABCD NET RULES				
	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPB_RESET	IFPB_RESET			120Ω
IFPCD_RESET	IFPCD_RESET			120Ω
IFPCD_EFACD_P	IFPCD_EFACD_P	3	500Ω	
IFPCD_EFACD_N	IFPCD_EFACD_N	3	500Ω	
IFPCD_EFACD_P	IFPCD_EFACD_P	3	500Ω	
IFPCD_EFACD_N	IFPCD_EFACD_N	3	500Ω	
	NET	VOLTAGE	MAX_CURRENT	SEN_WIDTH
IFPB_PLVDD	IFPB_PLVDD	1.8V	0.25A	150MIL
IFPCD_KPDVDD	IFPCD_KPDVDD	3.3V	0.25A	150MIL
IFPCD_PLVDD	IFPCD_PLVDD	1.8V	0.25A	150MIL
IFPCD_KPLVDD	IFPCD_KPLVDD	3.3V	0.25A	150MIL



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PAGE DETAIL	IFP A/B and C/D Interface

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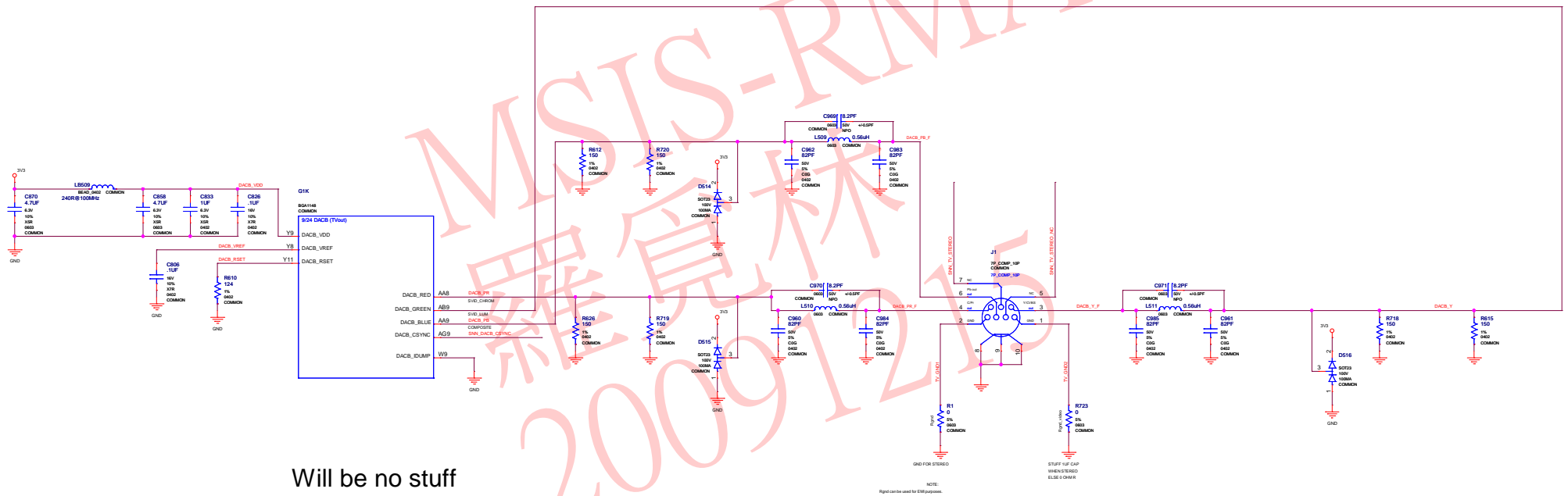
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DACB,STEREO, FL NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	DACS_PB	1	750ΩIN	
IN	DACS_Y	1	750ΩIN	
IN	DACS_PB	1	750ΩIN	
IN	DACS_PB_P	1	750ΩIN	
IN	DACS_Y_F	1	750ΩIN	
IN	DACS_PB_P	1	750ΩIN	

NET		VOLTAGE	MAX_CURRENT	MIN_WIDTH
in	TV_GND1	0.0V		125um
in	TV_GND2	0V		125um
in	DACB_VDD	3.3V	0.2A	125um
in	DACB_VREF			125um
in	DACB_RESET			125um



Will be no stuff

NOTE:
Rgnd can be used for EIM purposes

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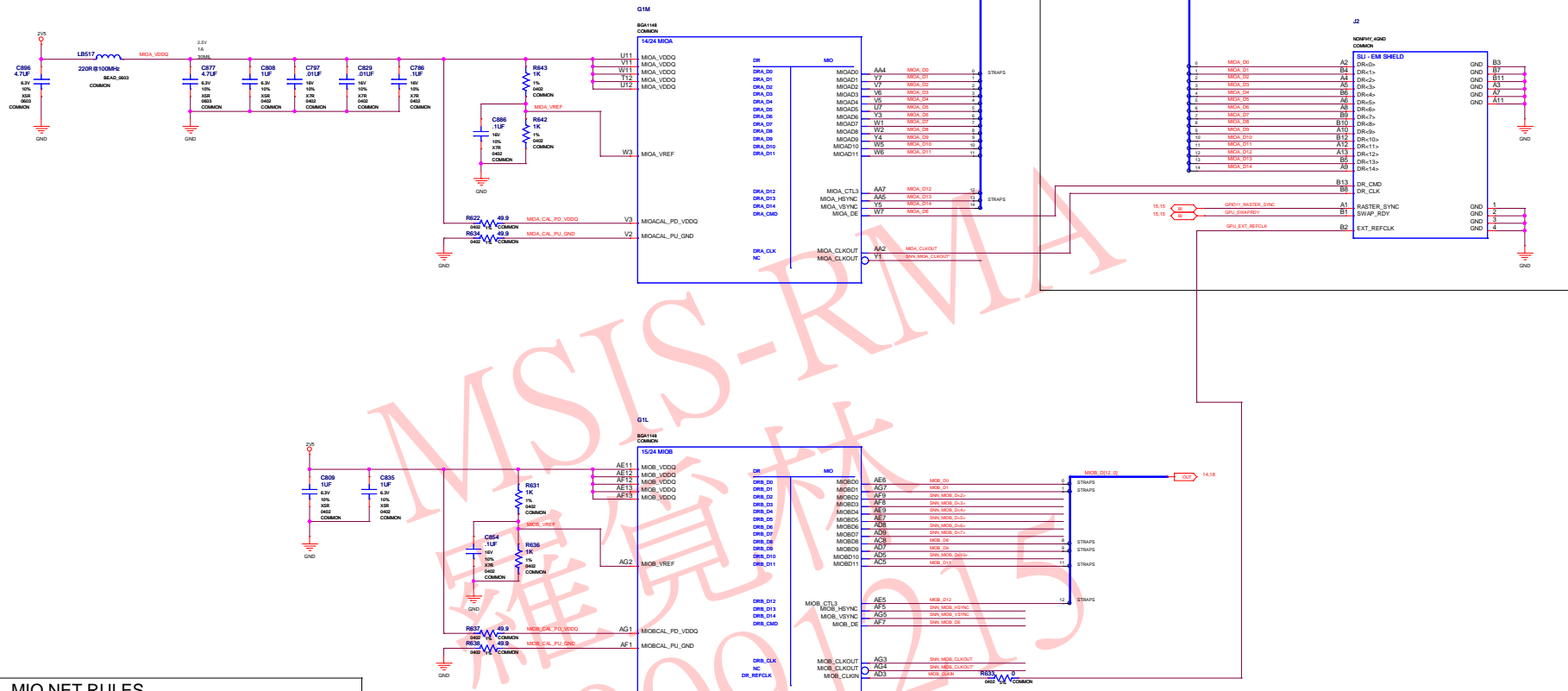
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MIO Feature Connector



MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
MIOA_MIOA_05	1	100OHM	
MIOA_MIOA_06	1	100OHM	
MIOA_MIOA_07	1	100OHM	
MIOB_MIOB_05	1	100OHM	
MIOB_MIOB_06	1	100OHM	
MIOB_MIOB_07	1	100OHM	
MIOB_MIOB_08	1	100OHM	
MIOB_MIOB_09	1	100OHM	
MIOB_MIOB_10	1	100OHM	
MIOB_MIOB_11	1	100OHM	
MIOB_MIOB_12	1	100OHM	
MIOB_MIOB_13	1	100OHM	
MIOB_MIOB_14	1	100OHM	
MIOB_MIOB_15	1	100OHM	
MIOB_MIOB_16	1	100OHM	
MIOB_MIOB_17	1	100OHM	
MIOB_MIOB_18	1	100OHM	
MIOB_MIOB_19	1	100OHM	
MIOB_MIOB_20	1	100OHM	
MIOB_MIOB_21	1	100OHM	
MIOB_MIOB_22	1	100OHM	
MIOB_MIOB_23	1	100OHM	
MIOB_MIOB_24	1	100OHM	
MIOB_MIOB_25	1	100OHM	
MIOB_MIOB_26	1	100OHM	
MIOB_MIOB_27	1	100OHM	
MIOB_MIOB_28	1	100OHM	
MIOB_MIOB_29	1	100OHM	
MIOB_MIOB_30	1	100OHM	
MIOB_MIOB_31	1	100OHM	
MIOB_MIOB_32	1	100OHM	
MIOB_MIOB_33	1	100OHM	
MIOB_MIOB_34	1	100OHM	
MIOB_MIOB_35	1	100OHM	
MIOB_MIOB_36	1	100OHM	
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MIOB_MIOB_38	1	100OHM	
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MIOB_MIOB_42	1	100OHM	
MIOB_MIOB_43	1	100OHM	
MIOB_MIOB_44	1	100OHM	
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MIOB_MIOB_46	1	100OHM	
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MIOB_MIOB_51	1	100OHM	
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MIOB_MIOB_53	1	100OHM	
MIOB_MIOB_54	1	100OHM	
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MIOB_MIOB_56	1	100OHM	
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MIOB_MIOB_60	1	100OHM	
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MIOB_MIOB_99	1	100OHM	
MIOB_MIOB_100	1	100OHM	

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ASSEMBLY: P001 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL: Multi-use (MIO) Interface

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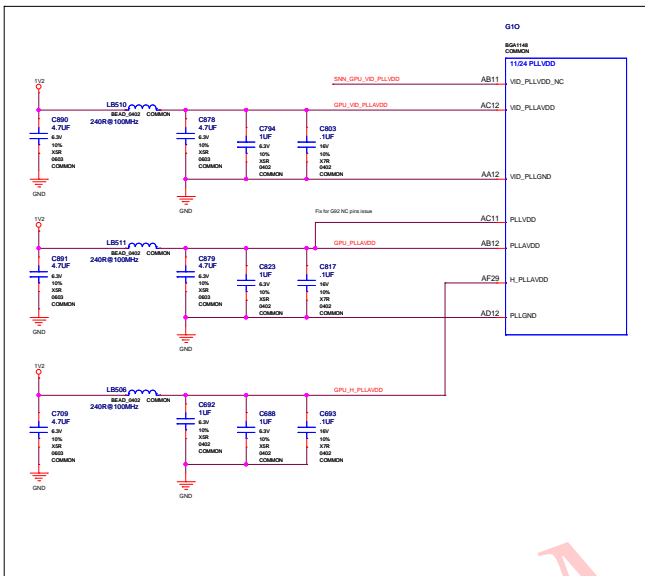
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN 600-10361-base-000 A

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NAME	DATE



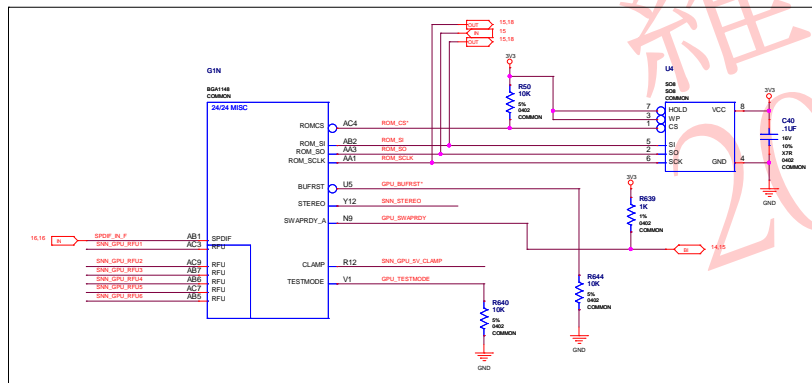
05-MAR-2009

[illegible]

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	16	ODIN_BOSS	3	500MHz	
	17	ODIN_BOSS	3	500MHz	
	18	ODIN_BOSS	3	500MHz	
15.10	19	ODIN_BOSS_W	3	500MHz	
	20	ODIN_BOSS_W	3	500MHz	
	21	ODIN_BOSS_W	3	500MHz	
15.15	22	ODIN_BOSS_W	3	500MHz	
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	290	ODIN_BOSS_W	3	500MHz	
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(BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)

[illegible]

GPIO Assignment Table

GPIO	I/O	Function
0	IN	DVI Hotplug Detect South
1	IN	DVI Hotplug Detect North
2	N/A	Not used
3	N/A	Not used
4	OUT	Fan PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fan Tach Input
8	OUT	THERMAL_OVERT*
9	N/A	Not used
10	N/A	Not used
11	OUT	RASTER (SLI) SYNC
12	N/A	Not used
13	N/A	Not used
14	N/A	Not used

ASSEMBLY	P361 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO, I2C, BIOS, PLL, and XTAL

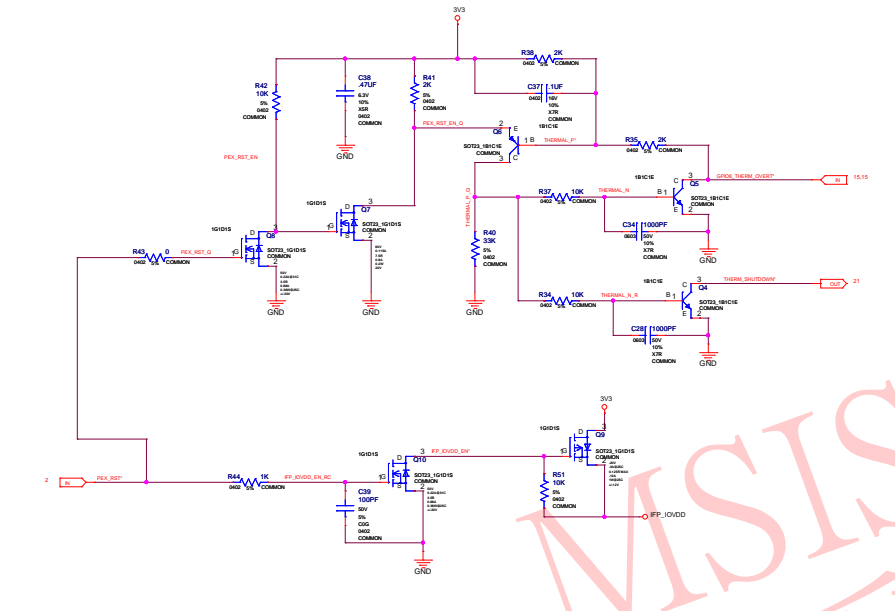
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



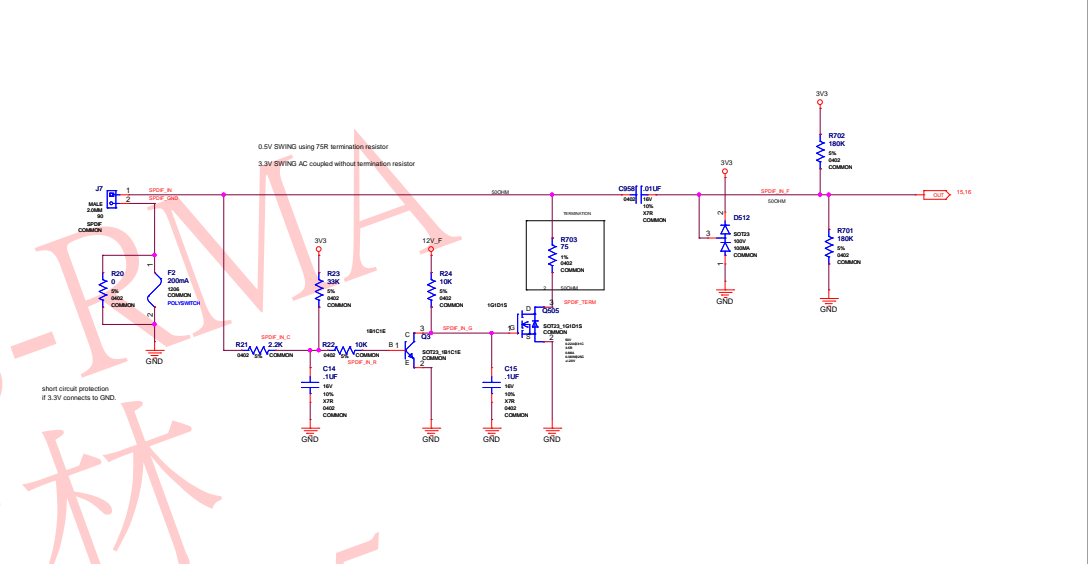
NV_PN	600-10361-base-000 A
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NAME		DATE	05-MAR-2009

THERMAL PROTECTION/TMDS BACKDRIVE

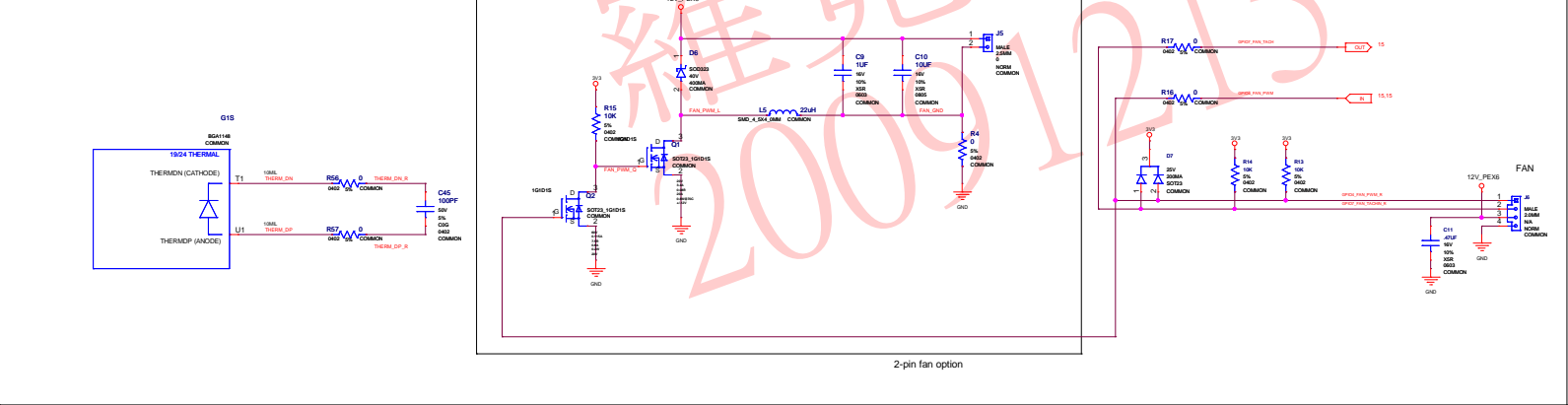


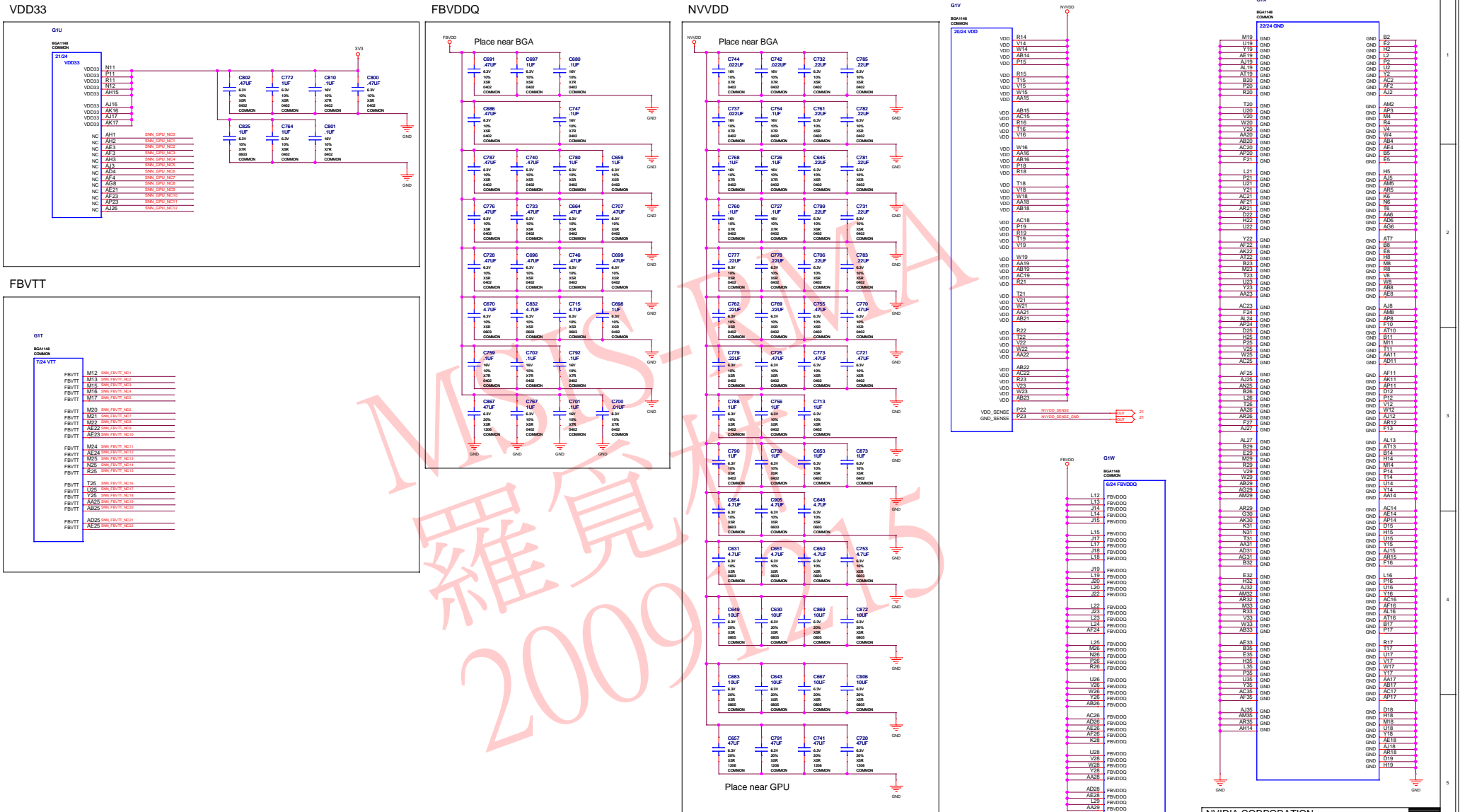
SPDIF INPUT / DETECTION



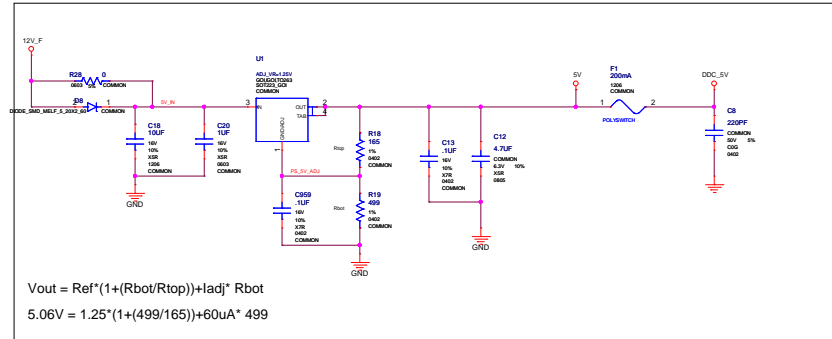
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SPDIF_N_N	50OHM	1	
SPDIF_N_G	50OHM	1	
SPDIF_N_T	50OHM	1	
SPDIF_N_E	50OHM	1	

THERMAL DIODE

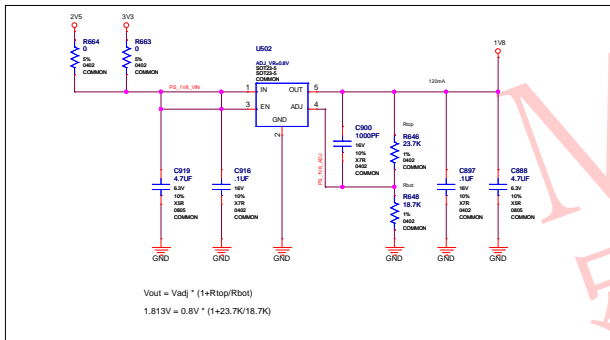




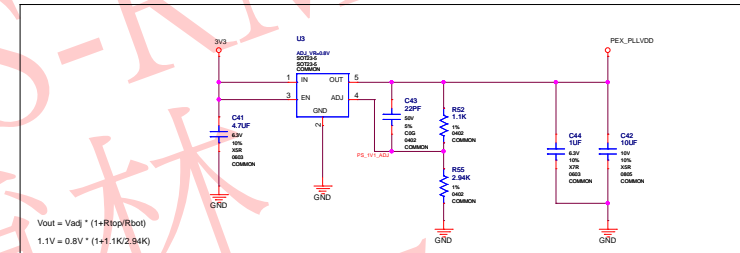
5V REGULATOR



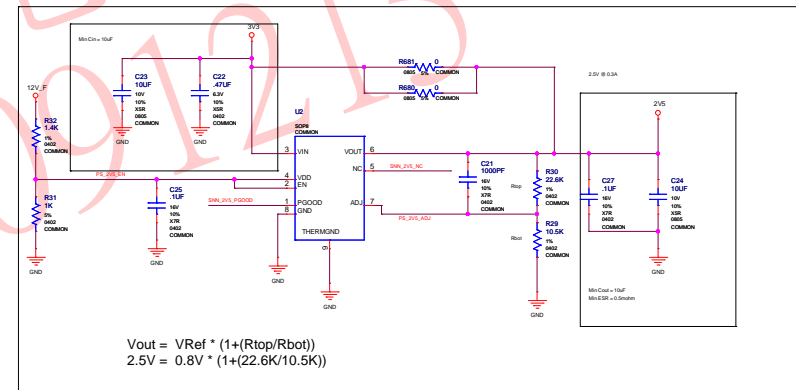
5V DDC



PEX_PLLVDD Optional



MIO_VDD 2.5V



NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	0.1A	138L	5V
5V	0.05A	138L	5V
PEX_PLLVDD	0.02A	138L	1.0V
TVS	0.02A	138L	18V
2V5	0.0A	138L	2.5V



NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
FBVDD	2500	15A	2.05V
V12	100	3A	1.2V

PEXVDD Power Supply

PEXVDD = 1.2V @ 3A

$$V_{out} = V_{in} * (1 + R_{top} / R_{bot})$$

$$1.152V = 0.8V * (1 + (1.07K / 43K))$$

FBVDD Power Supply

FBVDD = 2.05 V@ 15A

Optional

$$FBVDDQ = V_{REF} * (1 + (R_{top} / R_{bot}))$$

$$2.057V = 0.8V * (1 + (1.85K / 1.05K))$$

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ASSEMBLY	P381 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: FBVDD, PEXVDD

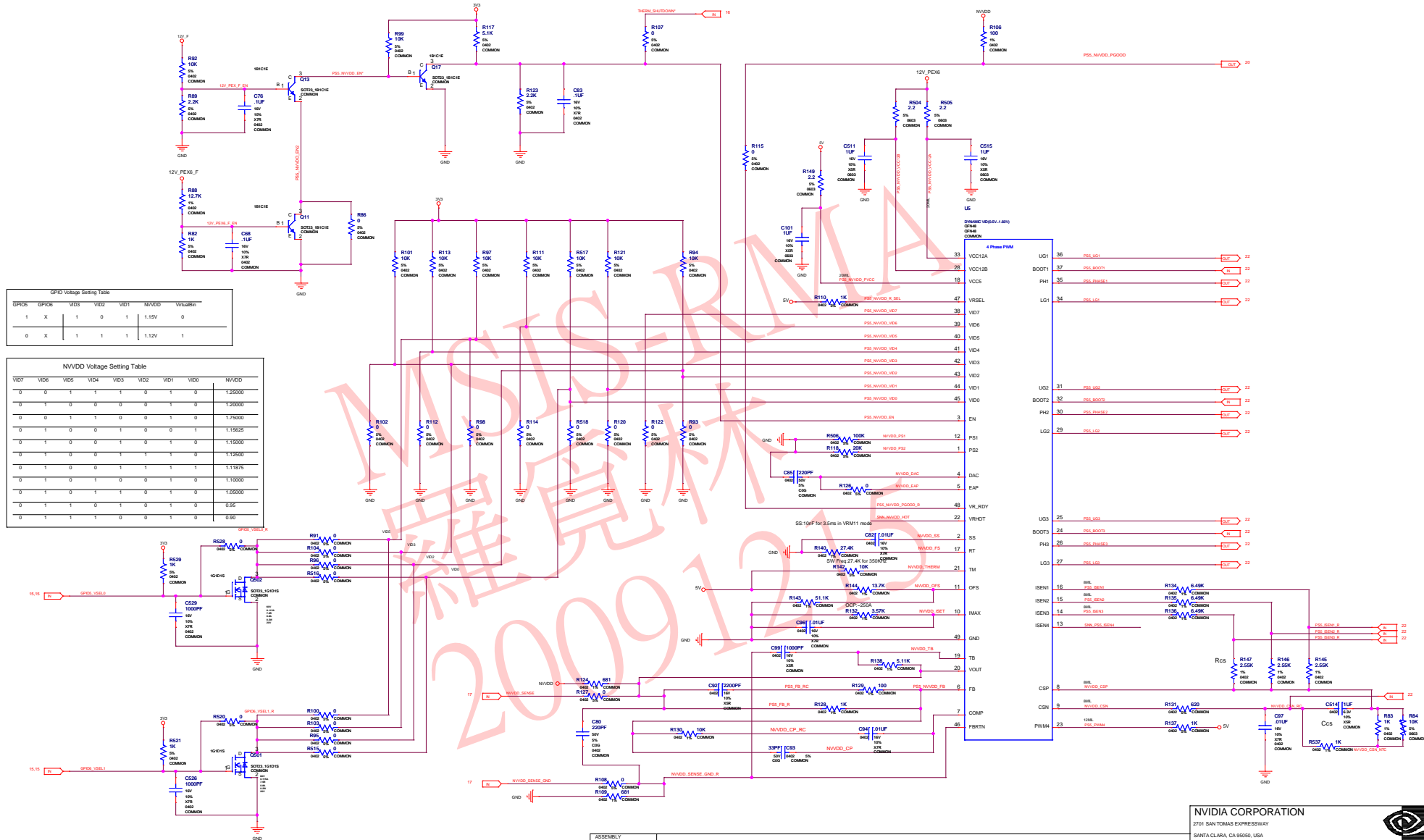
NVIDIA CORPORATION

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SANTA CLARA, CA 95050, USA

NV_PN 600-10361-base-000 A

ID	NAME	DATE	15-MAR-2005
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GPIO5	GPIO6	VID3	VID2	VID1	NVDD	VirtualBn
1	X	1	0	1	1.15V	0
0	X	1	1	1	1.12V	1

VDD1	VDD4	VDD5	VDD4	VDD3	VDD2	VDD1	VDD0	NVDD0
0	0	1	1	1	0	1	0	1.2500
0	1	0	0	0	0	1	0	1.2000
0	0	1	1	0	0	1	0	1.7500
0	1	0	0	1	0	0	1	1.1666
0	1	0	0	1	0	1	0	1.1600
0	1	0	0	1	1	1	0	1.1250
0	1	0	0	1	1	1	1	1.1167
1	0	1	0	0	0	1	0	1.1000
0	1	0	1	1	0	1	0	1.0500
0	1	1	0	1	0	1	0	0.95
0	1	1	1	0	0	1	0	0.90

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ASSEMBLY	
PAGE DETAIL	Power Supply: NVDD Regulator

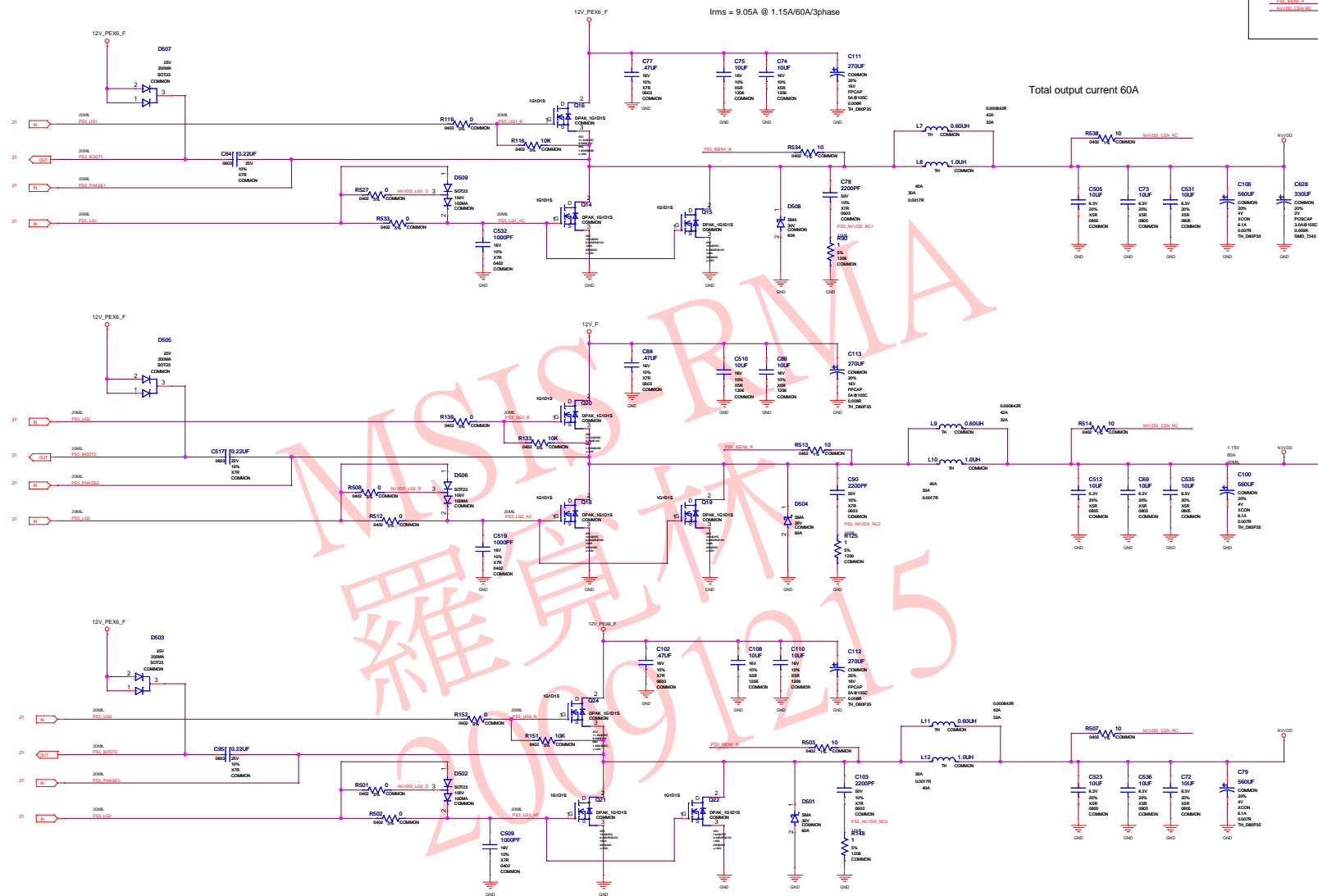
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PSS_GEN1_R	21	OUT
PSS_GEN2_R	21	OUT
PSS_GEN3_R	21	OUT
NVDD_CS1_R0	21	OUT

Total output current 60A

ASSEMBLY	
PAGE DETAIL	Power Supply: NVDD Mosfet

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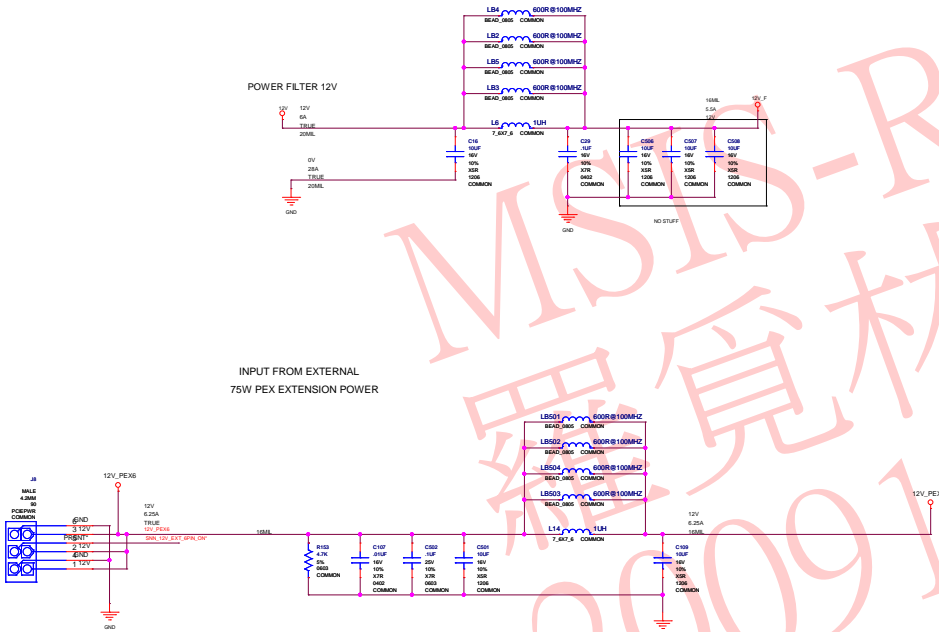
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ASSEMBLY	P001 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: Filter of 3V3, 12V, 12V_PEX6

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