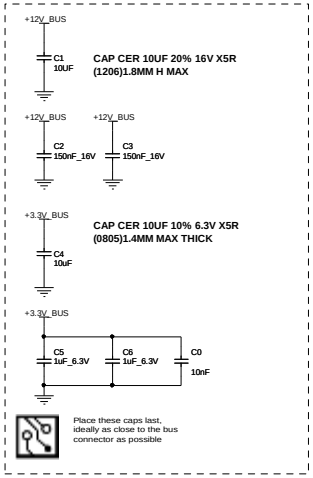
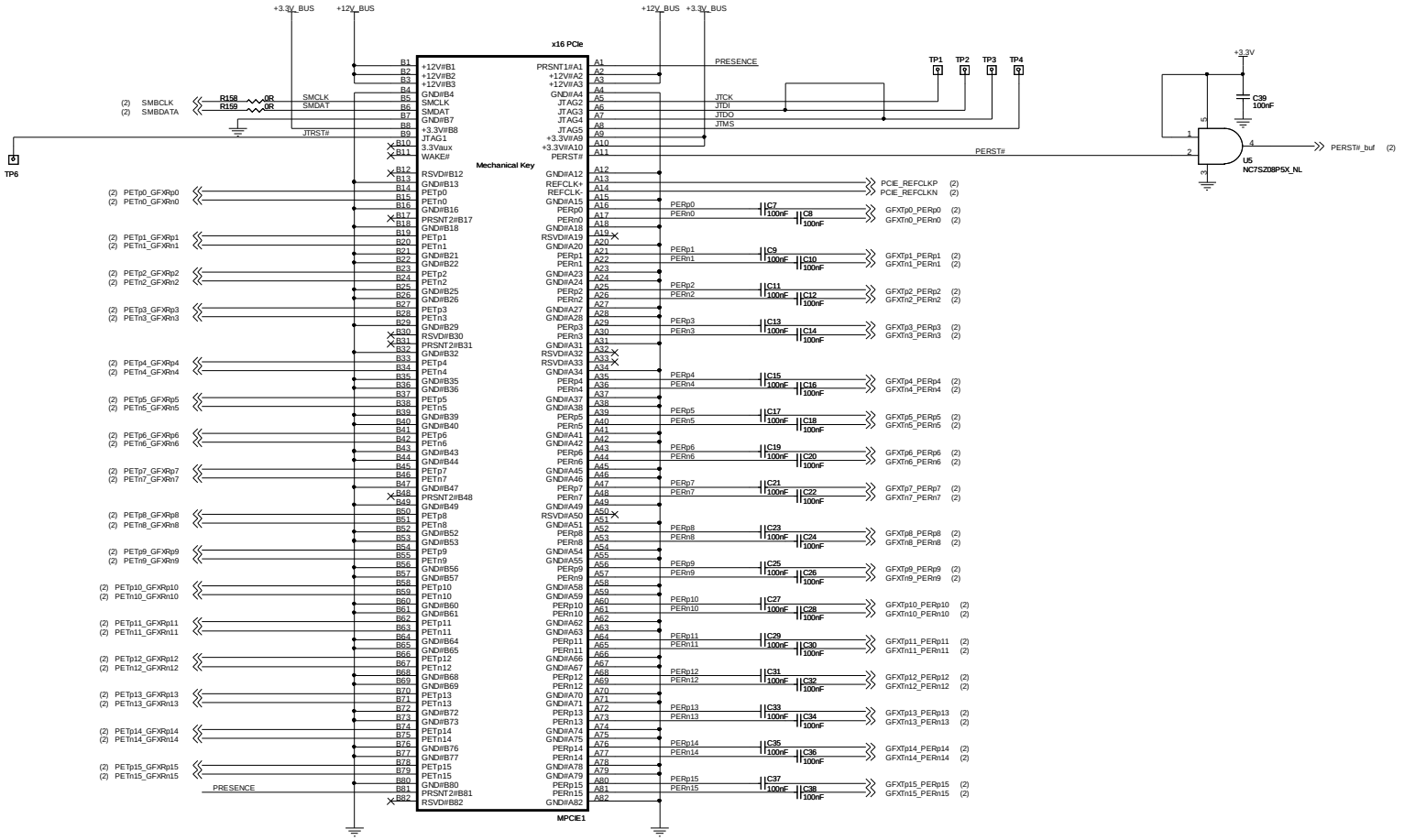
PCI-EXPRESS EDGE CONNECTOR





SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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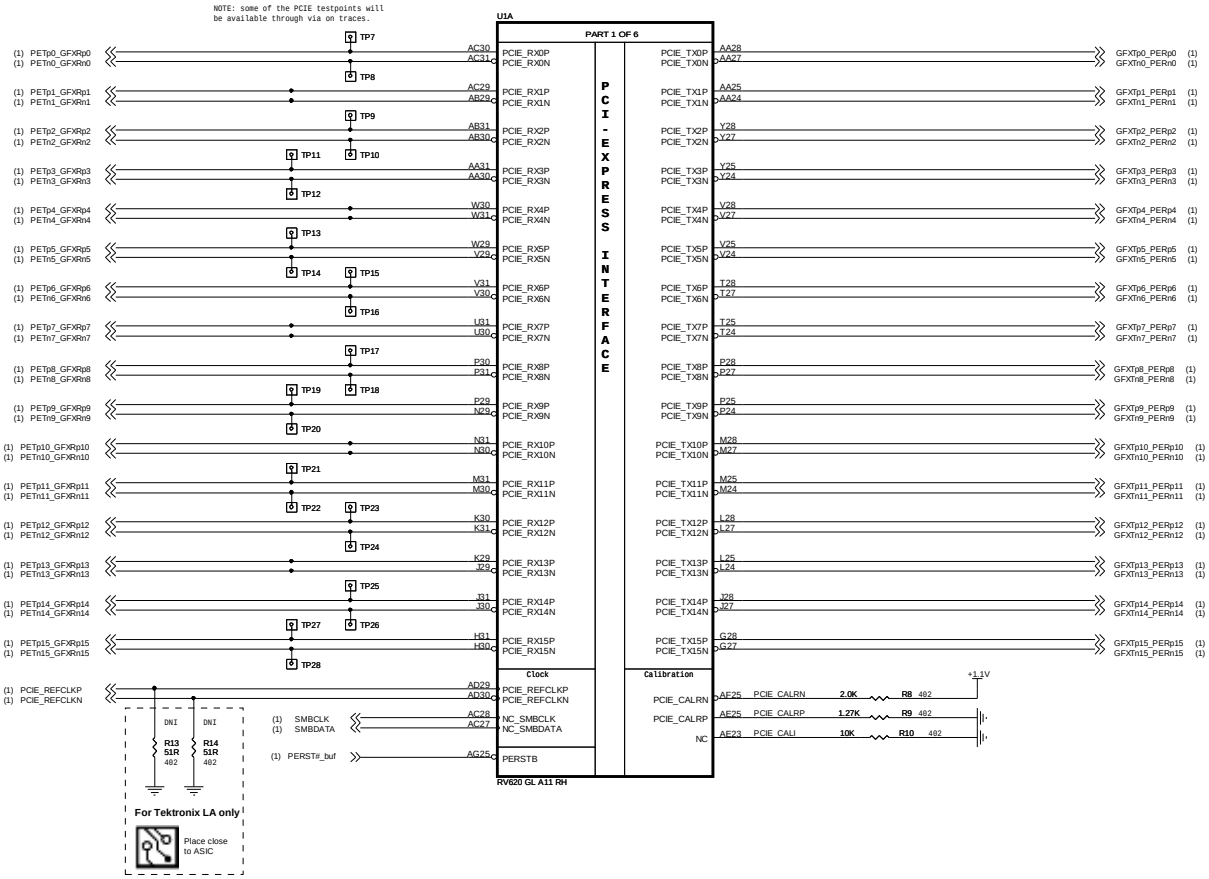

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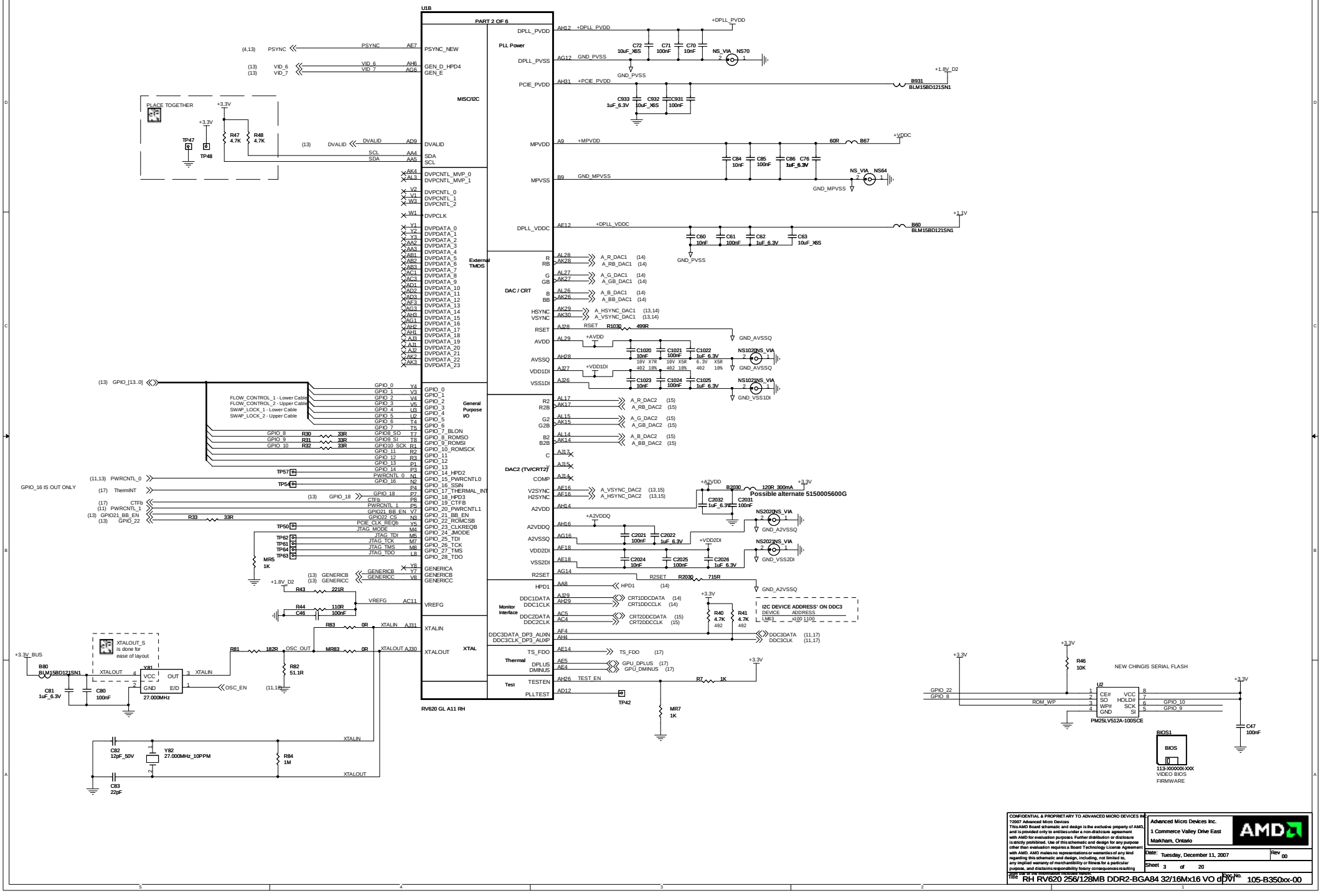

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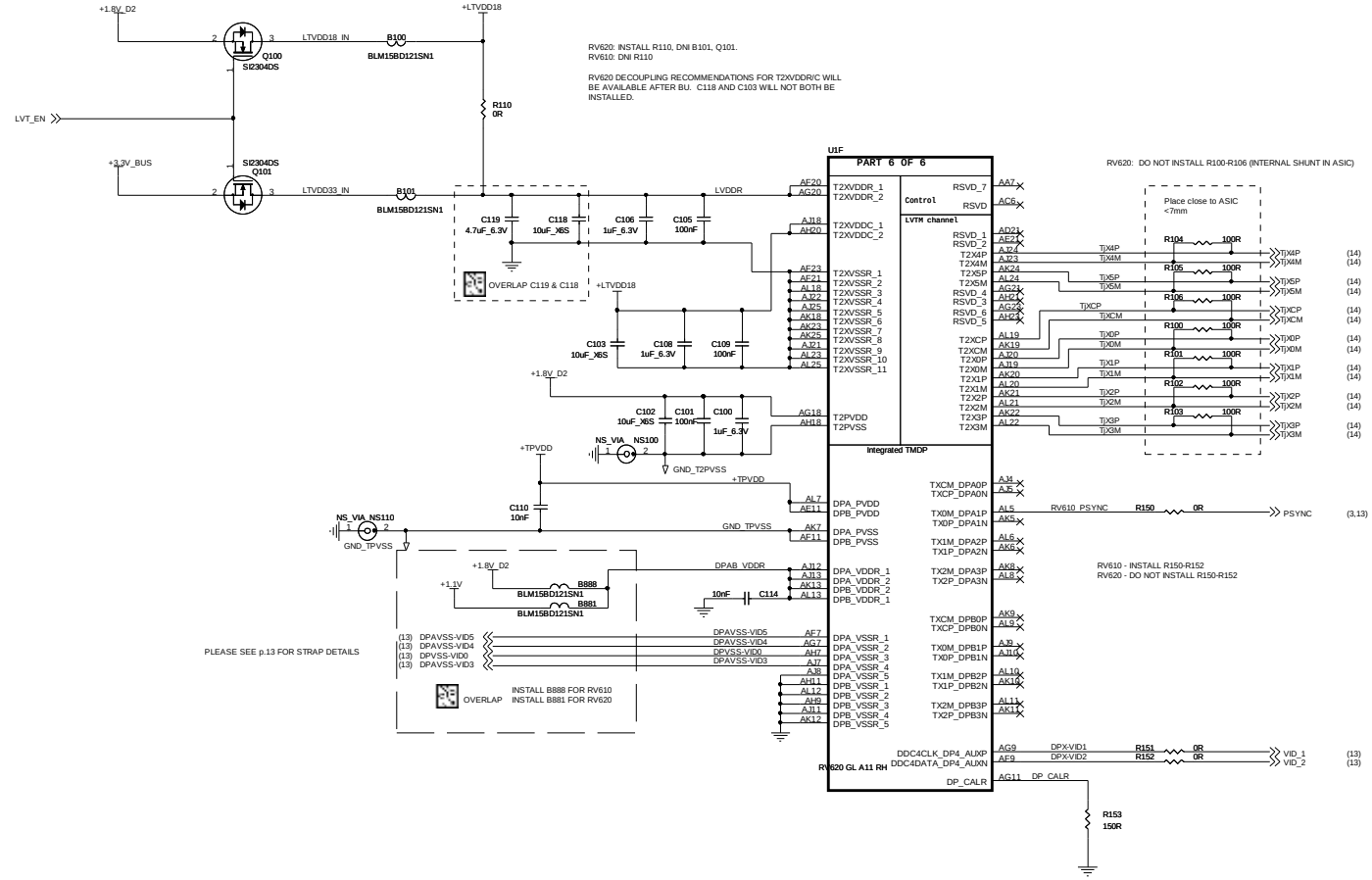

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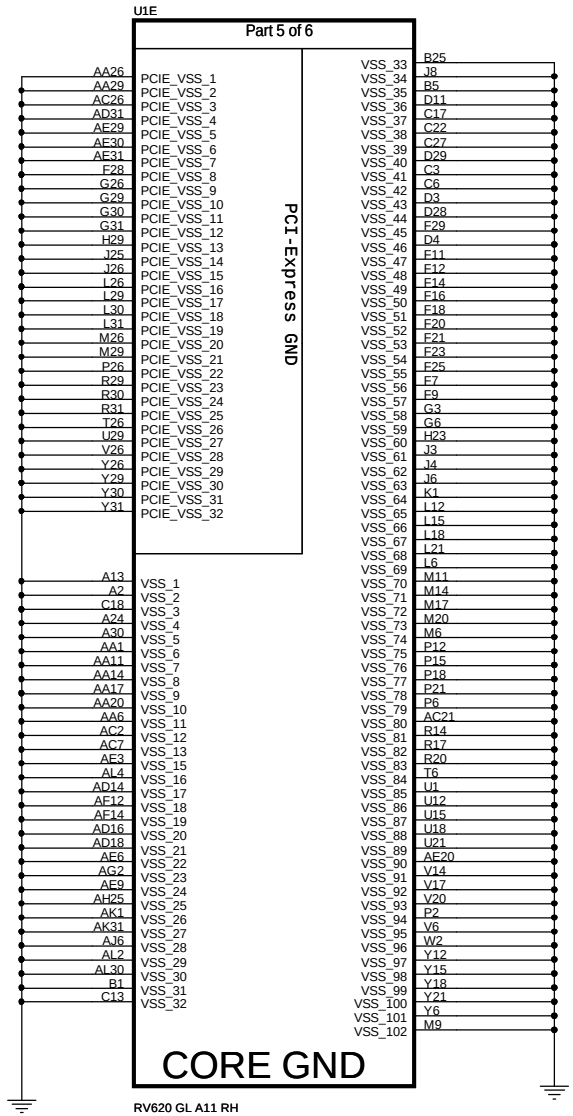

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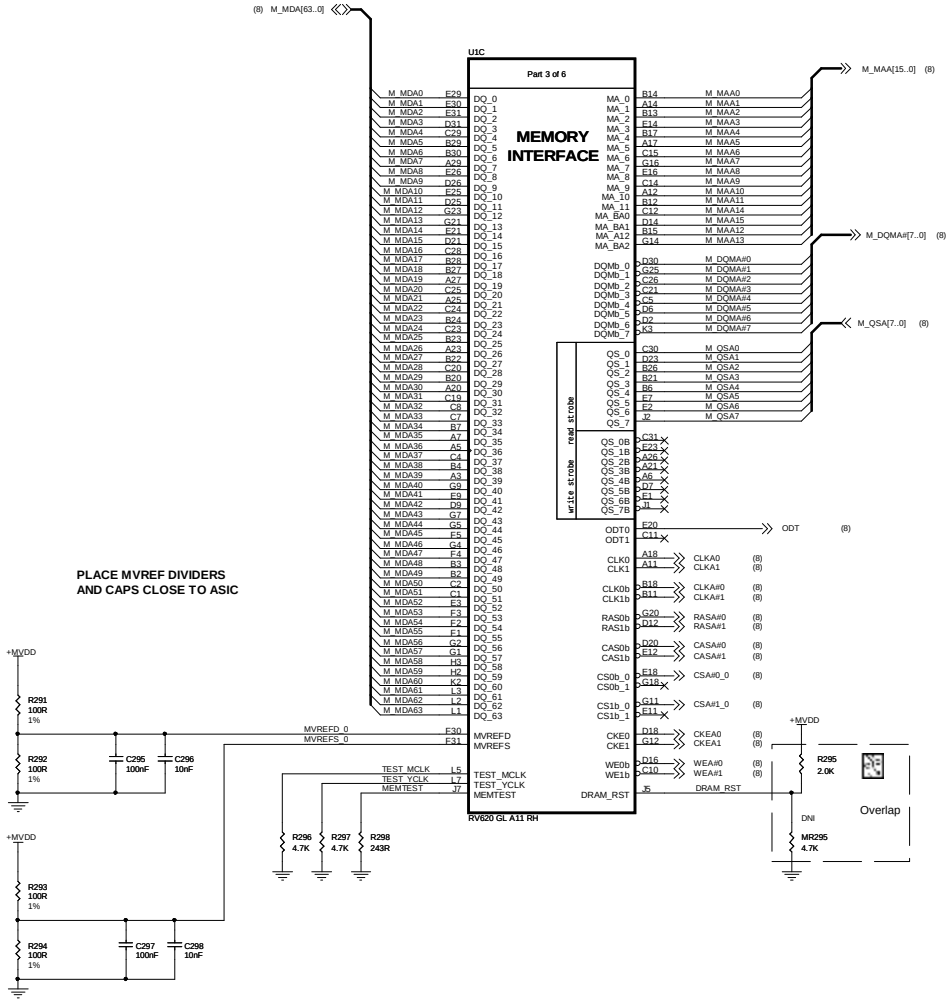

DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

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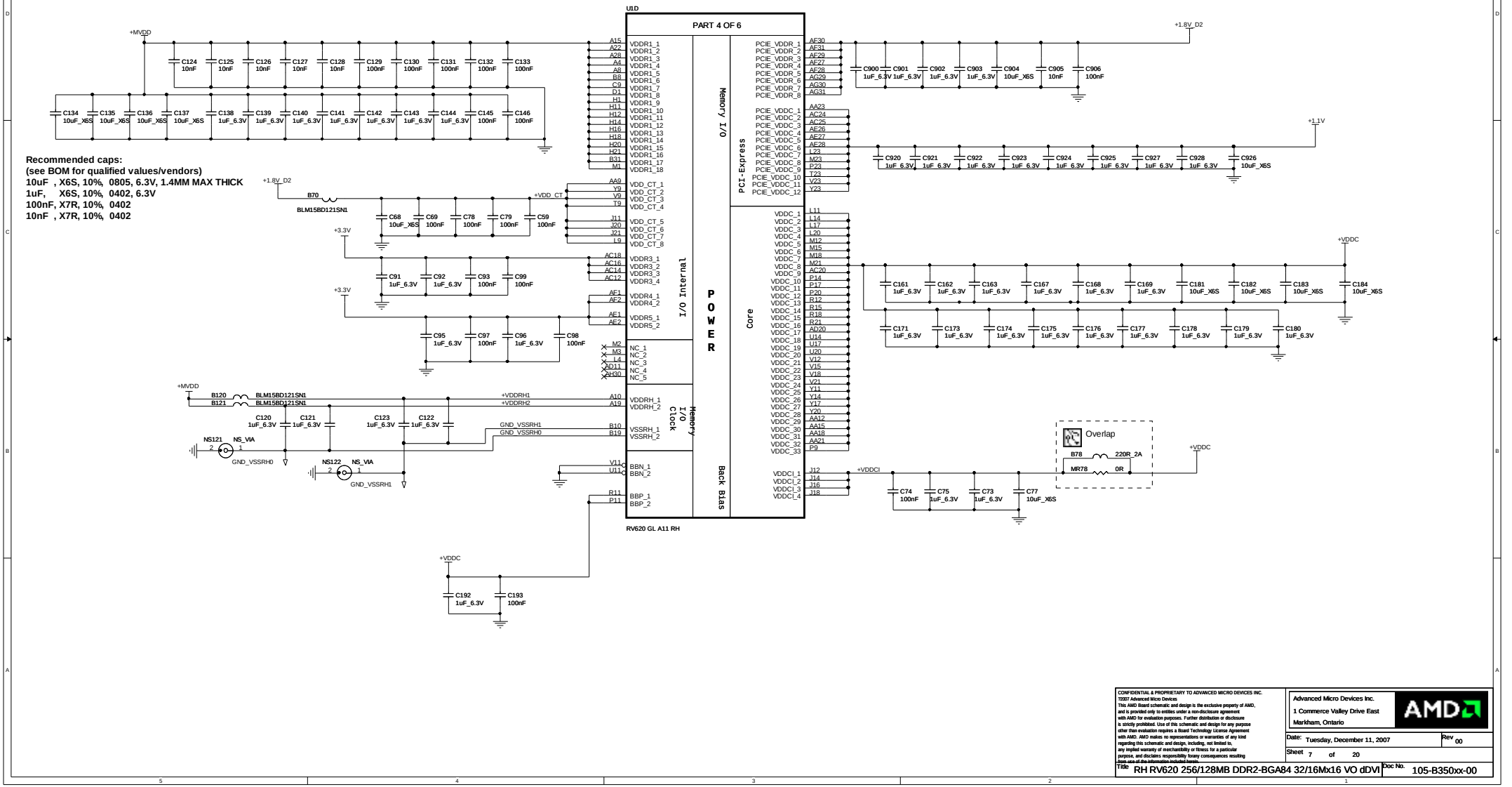

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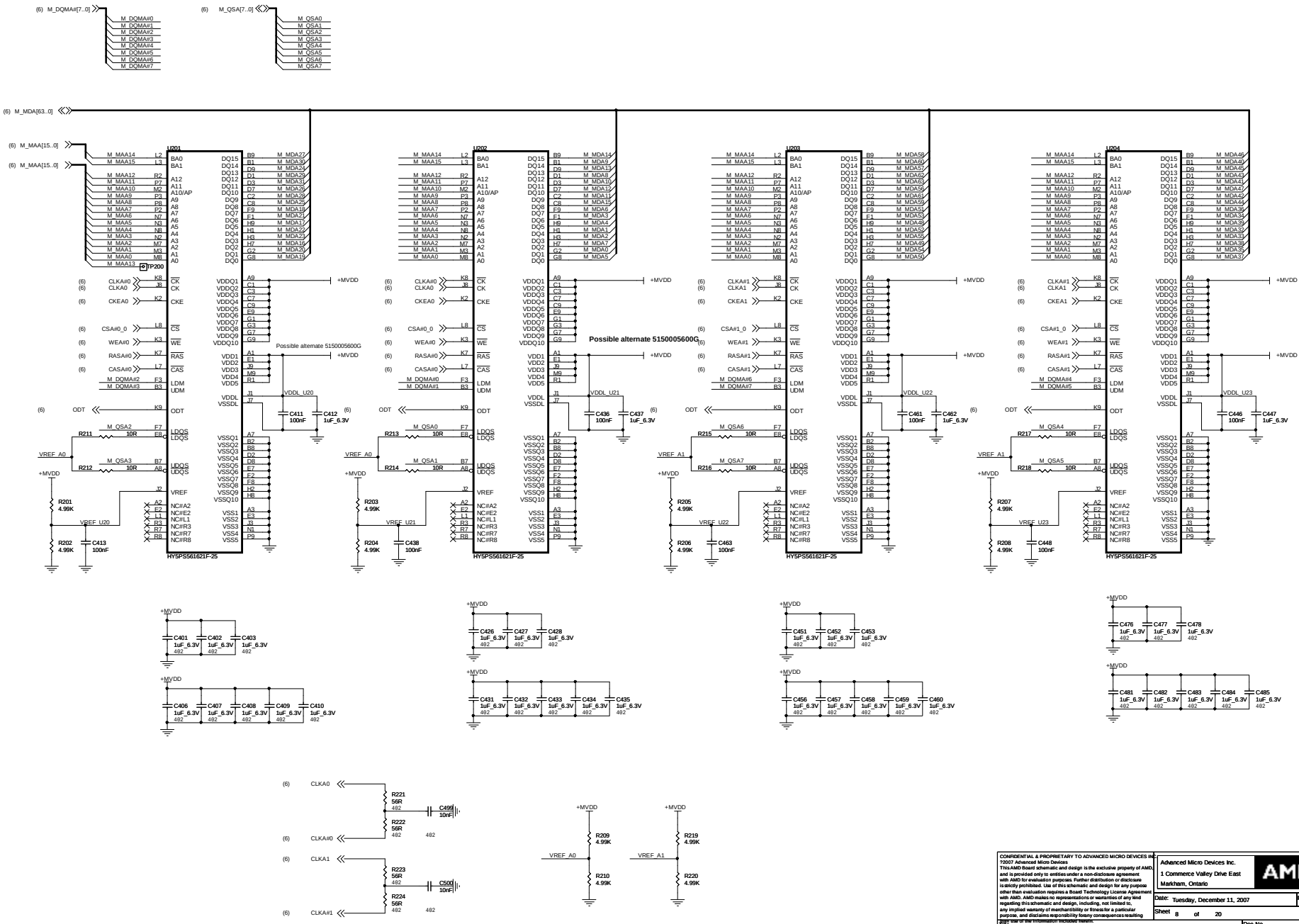
CHANNEL A: RANK 0 128MB DDR2



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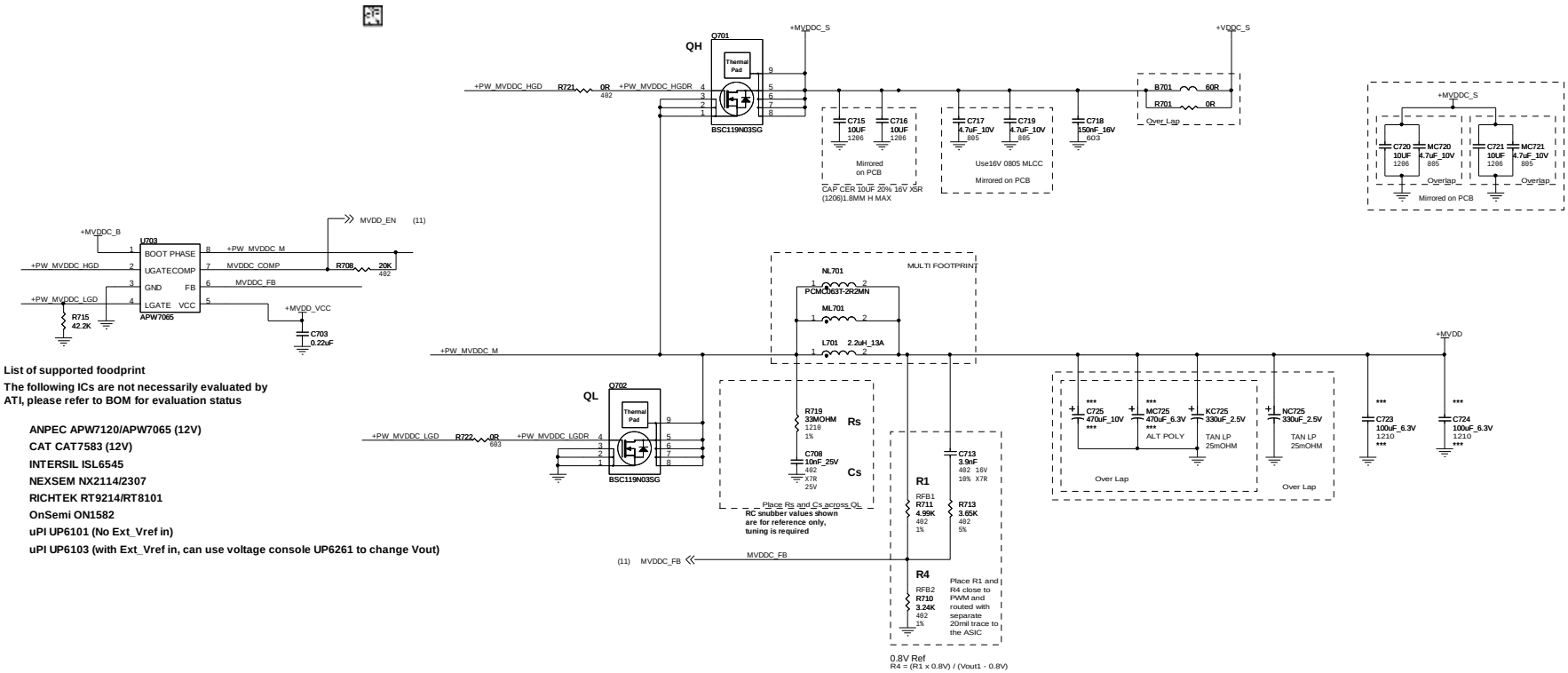
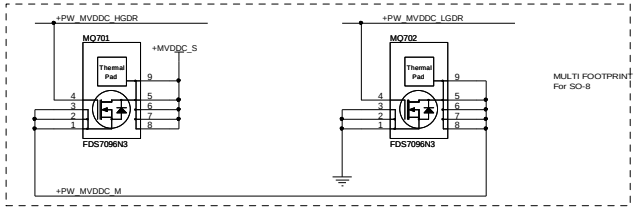


List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

- **ANPEC APW7120/APW7065 (12V)**
- **CAT CAT7583 (12V)**
- **INTERSIL ISL6545**
- **NEXSEM NX2114/2307**
- **RICHTEK RT9214/RT8101**
- **OnSemi ON1582**
- **uPI UP6101 (No Ext_Vref in)**
- **uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**



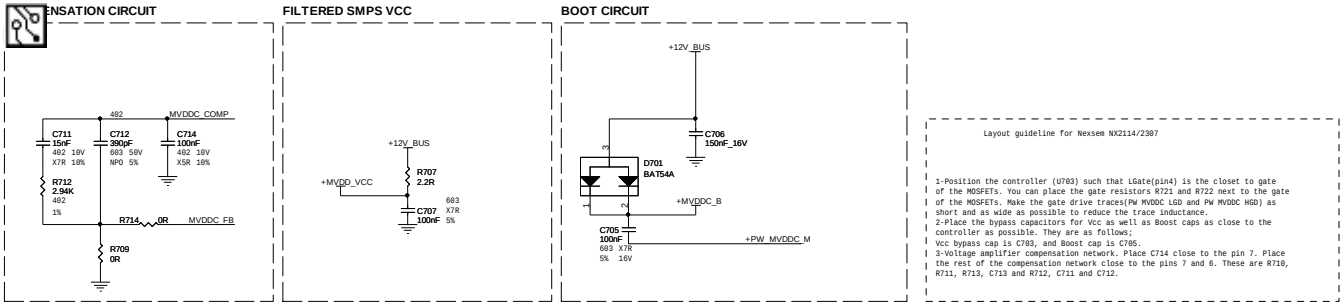
SMPS02- Regulator for MVDD

Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G
	1.8V (1.78V~1.86V)	4.99K p/n 3160499100G	3.92K p/n 3160392100G

SMPS02 Specifications

	Nominal Value	Tolerance	Adjustable range / Notes
Vin (power stage)	12V	+/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V	+2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp		
Iout	6Aavg, 8Adc_max		
Step load	3Amax		
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load		
Switching Freq.	~300kHz		TBD
Protections			



Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

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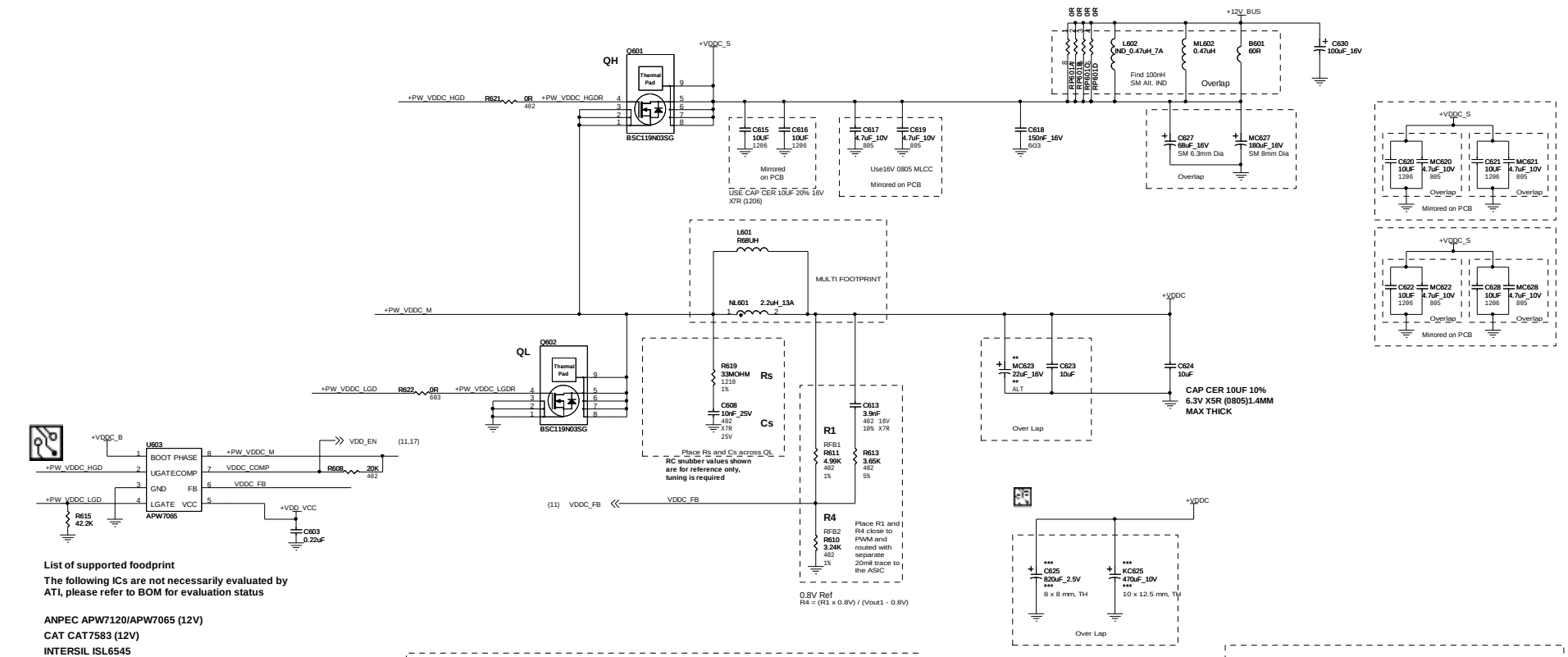

List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

ANPEC APW7120/APW7065 (12V)
CAT CAT7583 (12V)
INTERSIL ISL6545
NEXSEM NX2114/2307
RICHTEK RT9214/RT8101
OnSemi ON1582
uPI UP6101 (No Ext_Vref in)

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Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

SMPS02- Regulator for VDDC

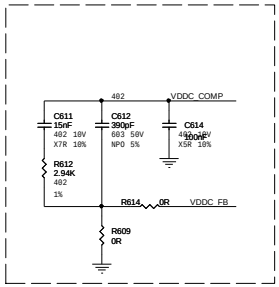
Vout = 0.9V ~ 1.1V

Part	Vout	RFB1	RFB2
0.8V Ref	1.1V (1.98V~2.08V)	200R p/n 3160200000G	511R p/n 3160511000G
	1.1V (1.10V~1.14V)	10K p/n 3160100200G	24.9K p/n 3160249200G

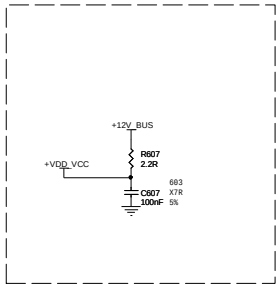
SMPS02 Specifications

	Nominal Value : Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

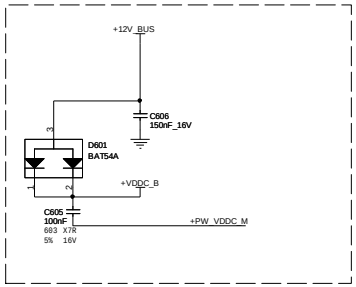
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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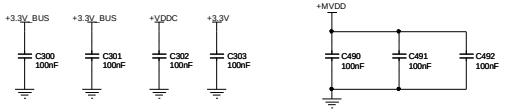
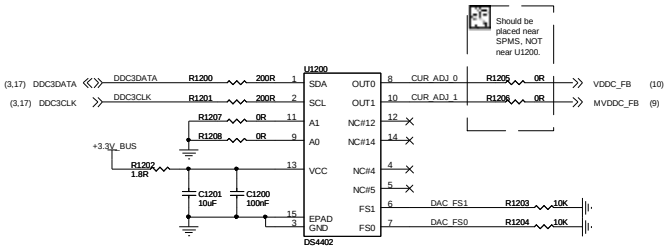
Stitching Capacitors

THESE ARE STITCHING CAPACITORS. THEIR PLACEMENT IS LAYOUT DEPENDANT.

Place C490-492 near layer transitions (top/bottom). THIS IS LAYOUT DEPENDENT.

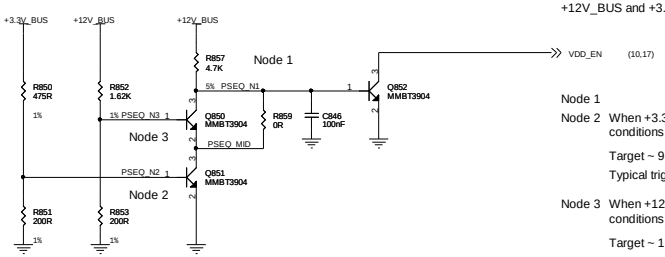


I2C control of VDDC/MVDD



Power up/down Sequencing

Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.



Node 1

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

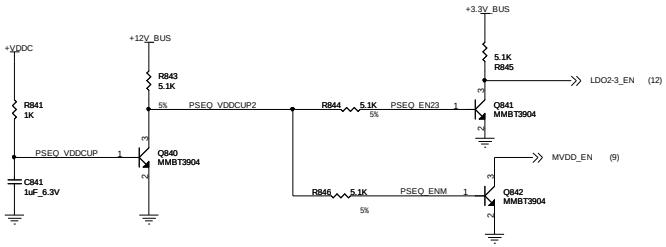
Typical trigger when +3.3V ramps above 2.2V (650mV)

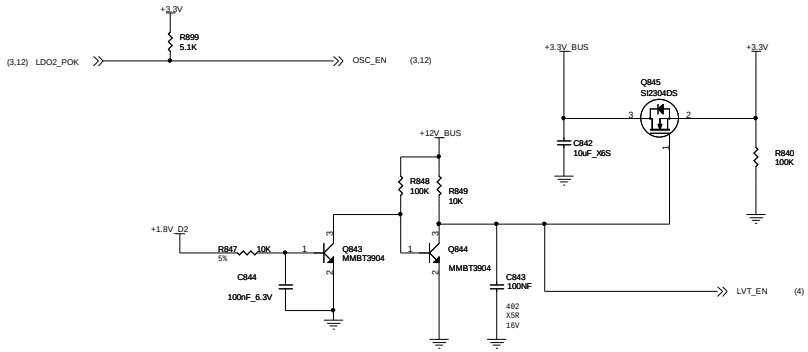
Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

When +12V_BUS ramps above min Vbe, SMPS_EN will be held low

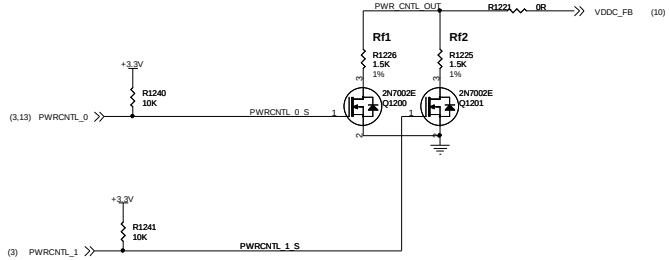




Power Play

VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=	Rf1= Rf2=	Rf1= Rf2=	
0	0				
0	1				
1	0				
1	1	1 0	1		Power-up Default



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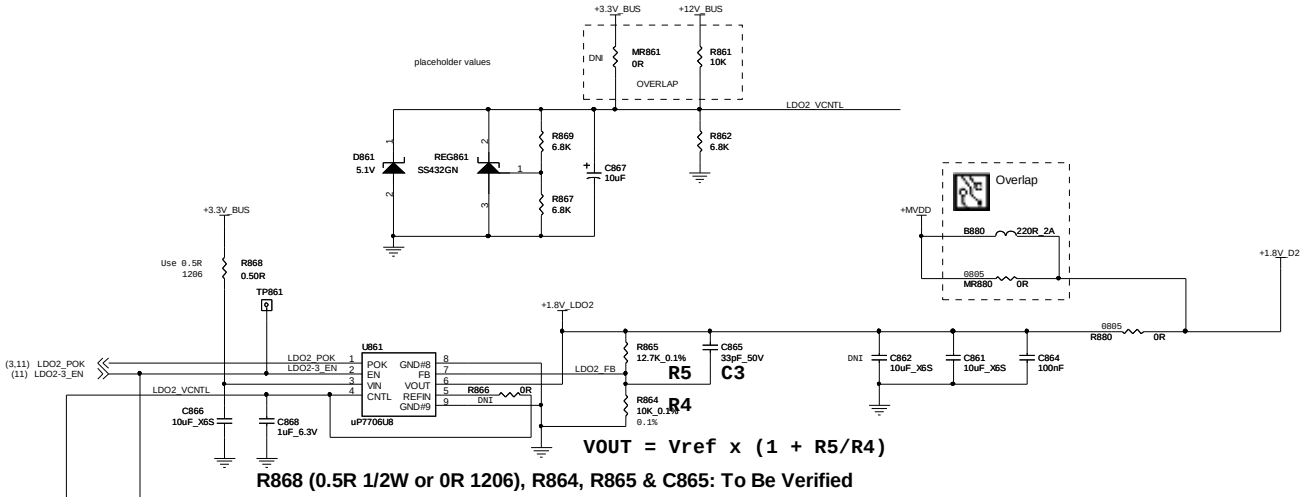
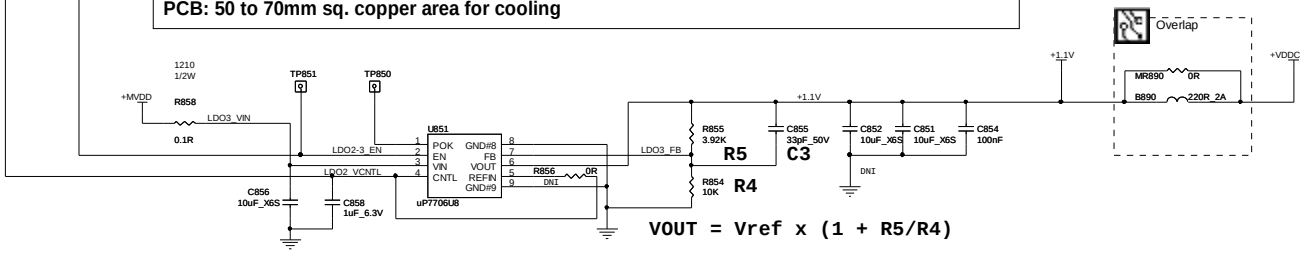
LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



VOUT = Vref x (1 + R5/R4)

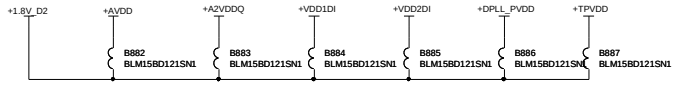
R868 (0.5R 1/2W or 0R 1206), R864, R865 & C865: To Be Verified

LDO #3: Vin = +1.4V to 2.087VMAX Vout = +1.1V +/- 2.5% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

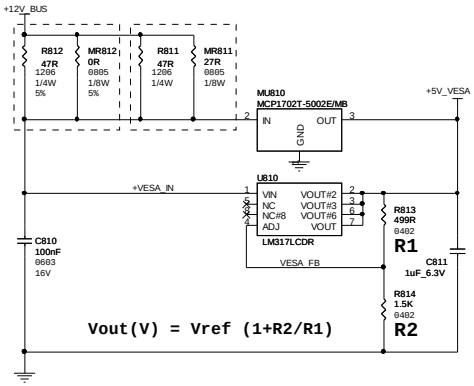


VOUT = Vref x (1 + R5/R4)

Shared Power Rails



Regulators for +5V, +5V_VESA



Vout(V) = Vref (1+R2/R1)

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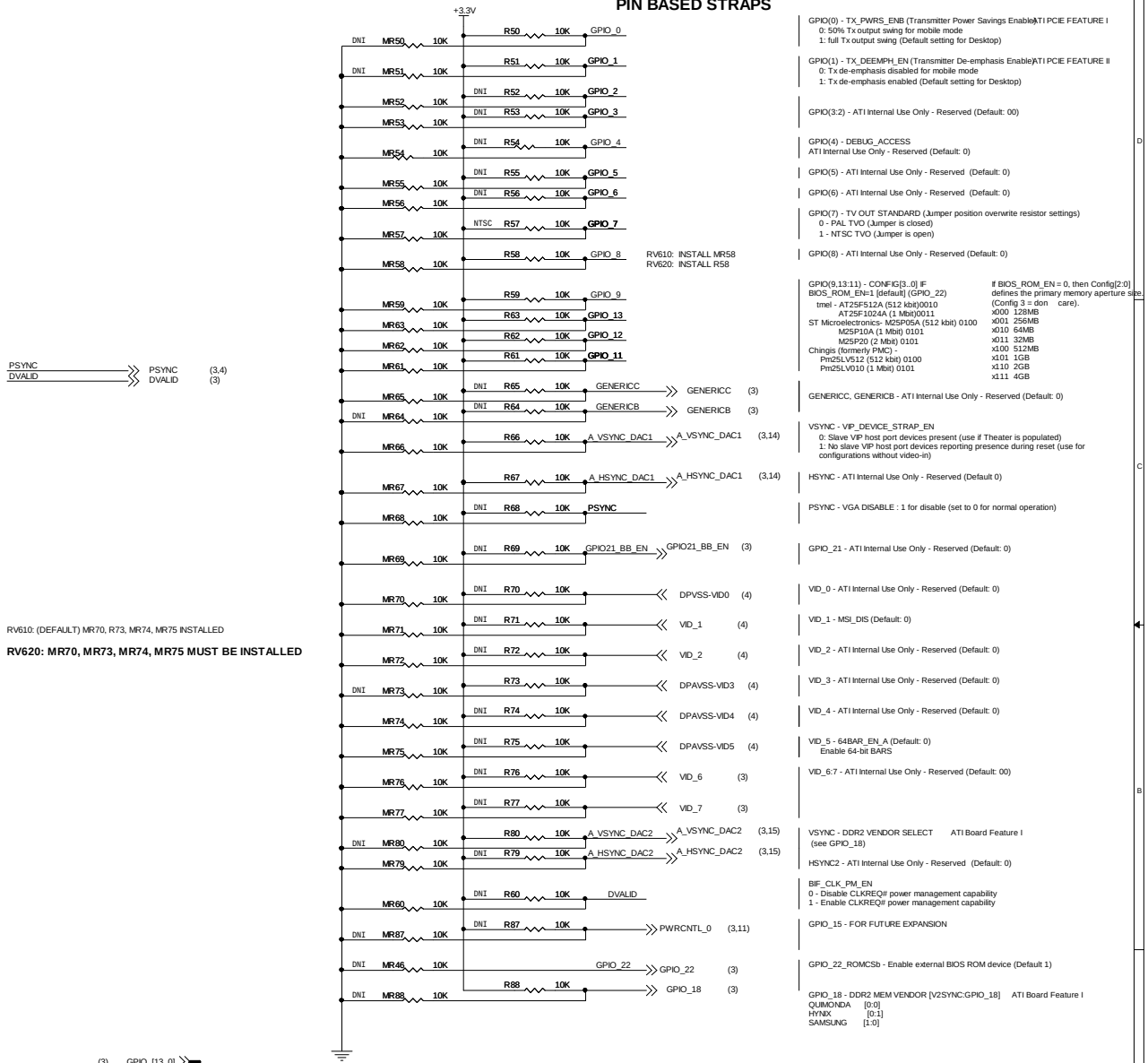
PIN BASED STRAPS



RV610: (DEFAULT) MR70, R73, MR74, MR75 INSTALLED

RV620: MR70, MR73, MR74, MR75 MUST BE INSTALLED

(3) GPIO_[13..0]

GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13

Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground High logic voltage

Signal

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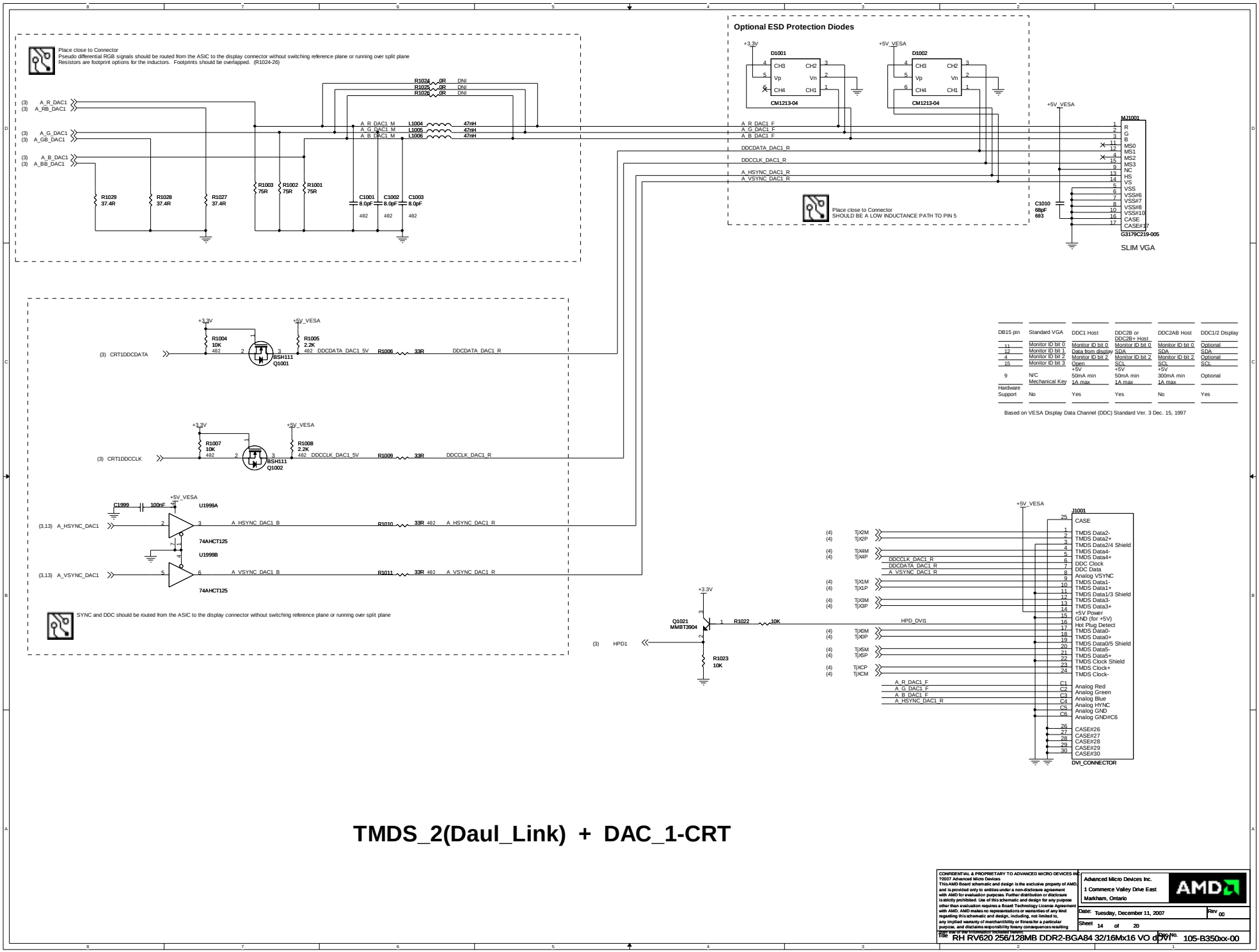

TMDS_2(Daul_Link) + DAC_1-CRT

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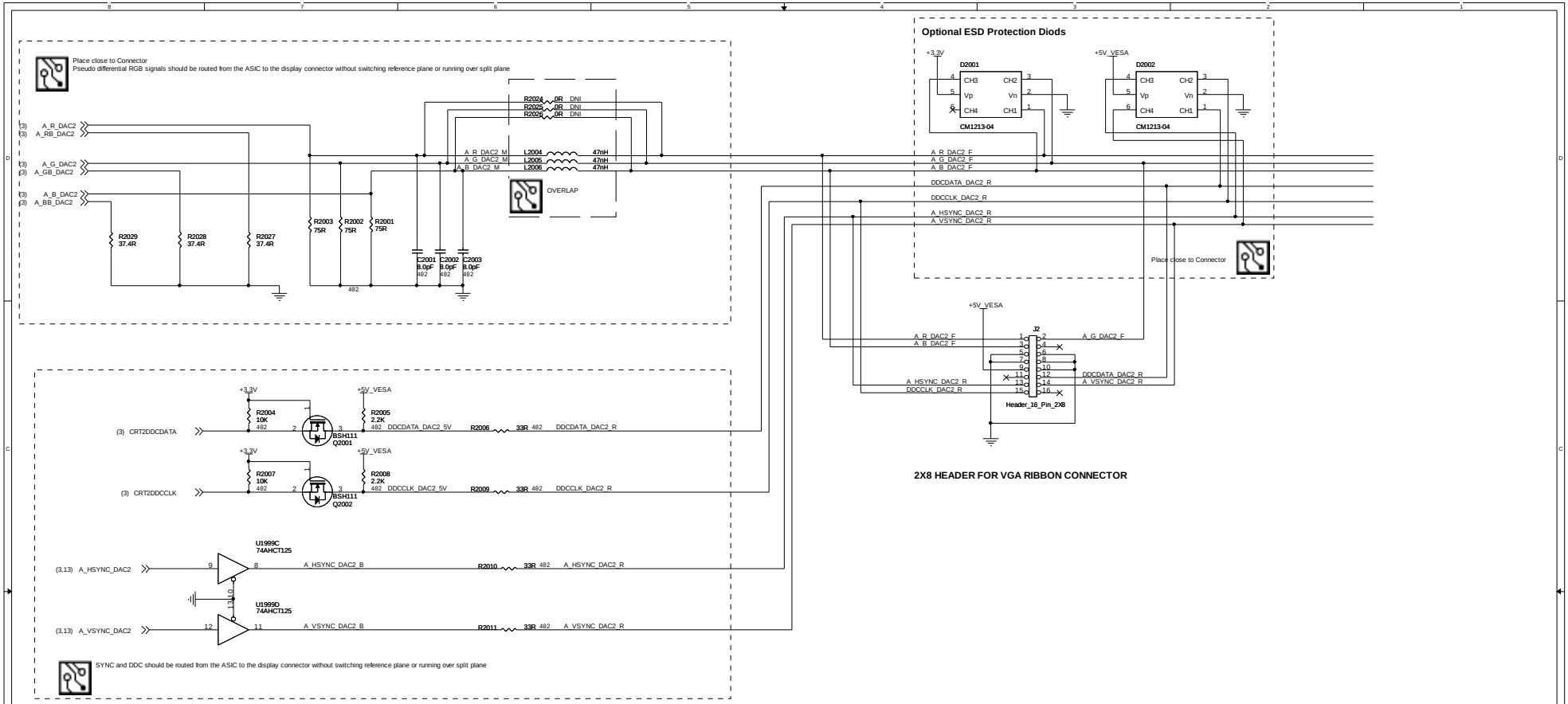

TMDS_1(Single_Link) + DAC_2-CRT

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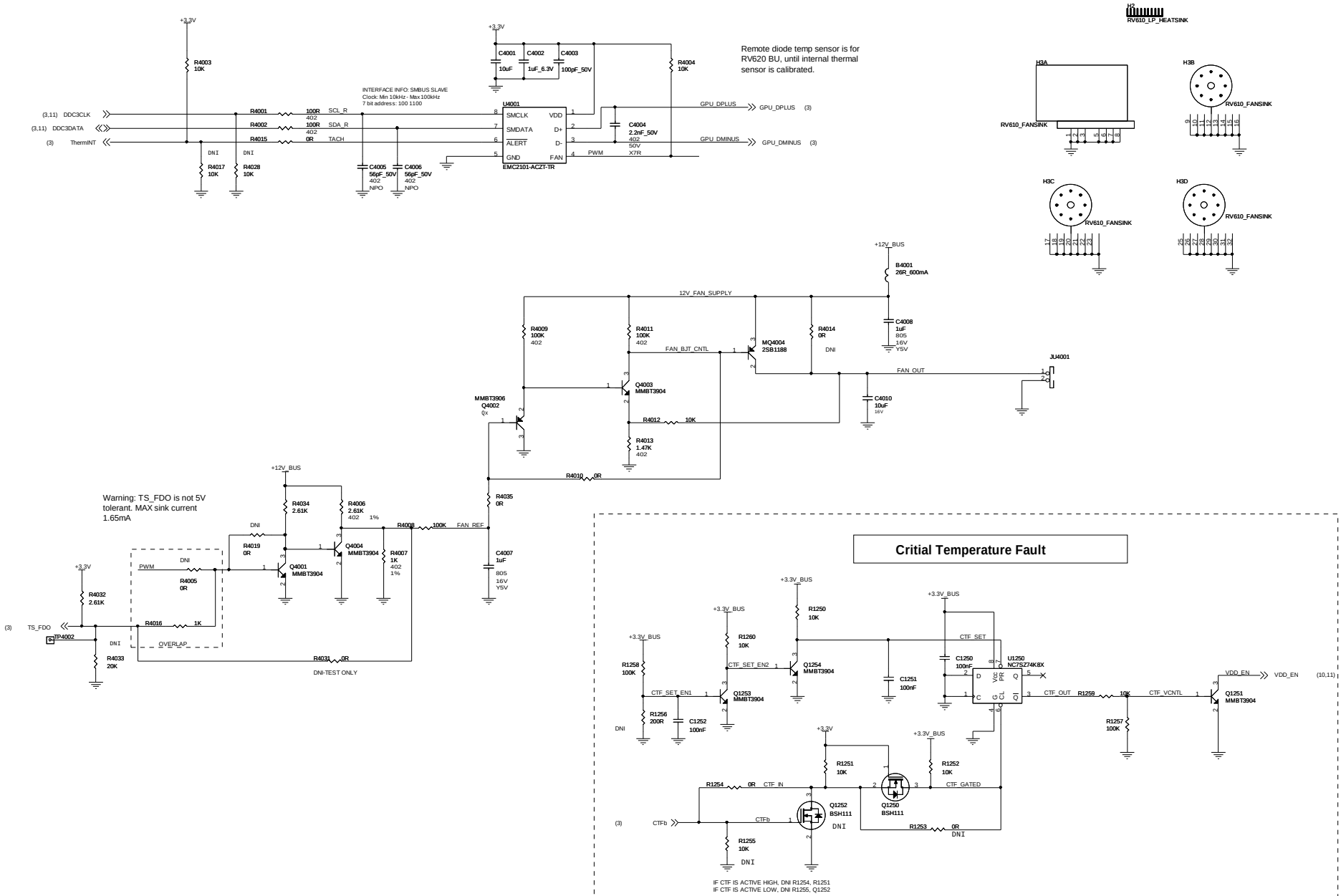

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DVI/VGA SCREWS

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW5
SCREW
SCREW, PAN HD, PHILLIPS, 4-40 X 3/16L

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY

MT1
MT_Hole_0.136_in.
DNI

MT2
MT_Hole_0.136_in_6VIA
DNI

SK1
BGA_Socket_RV620

FM1
SW_FB
NS

FM2
SW_FB
NS

FM3
SW_FB
NS

FM4
SW_FB
NS

FM5
SW_FB
NS

FM6
SW_FB
NS

ASSY1
BRACKET
8020040100G

ASSY2
BRACKET
LP
8020040400G

FM11

FM12

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Title RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI
Doc No. 105-B350xx-00

<variant_name>

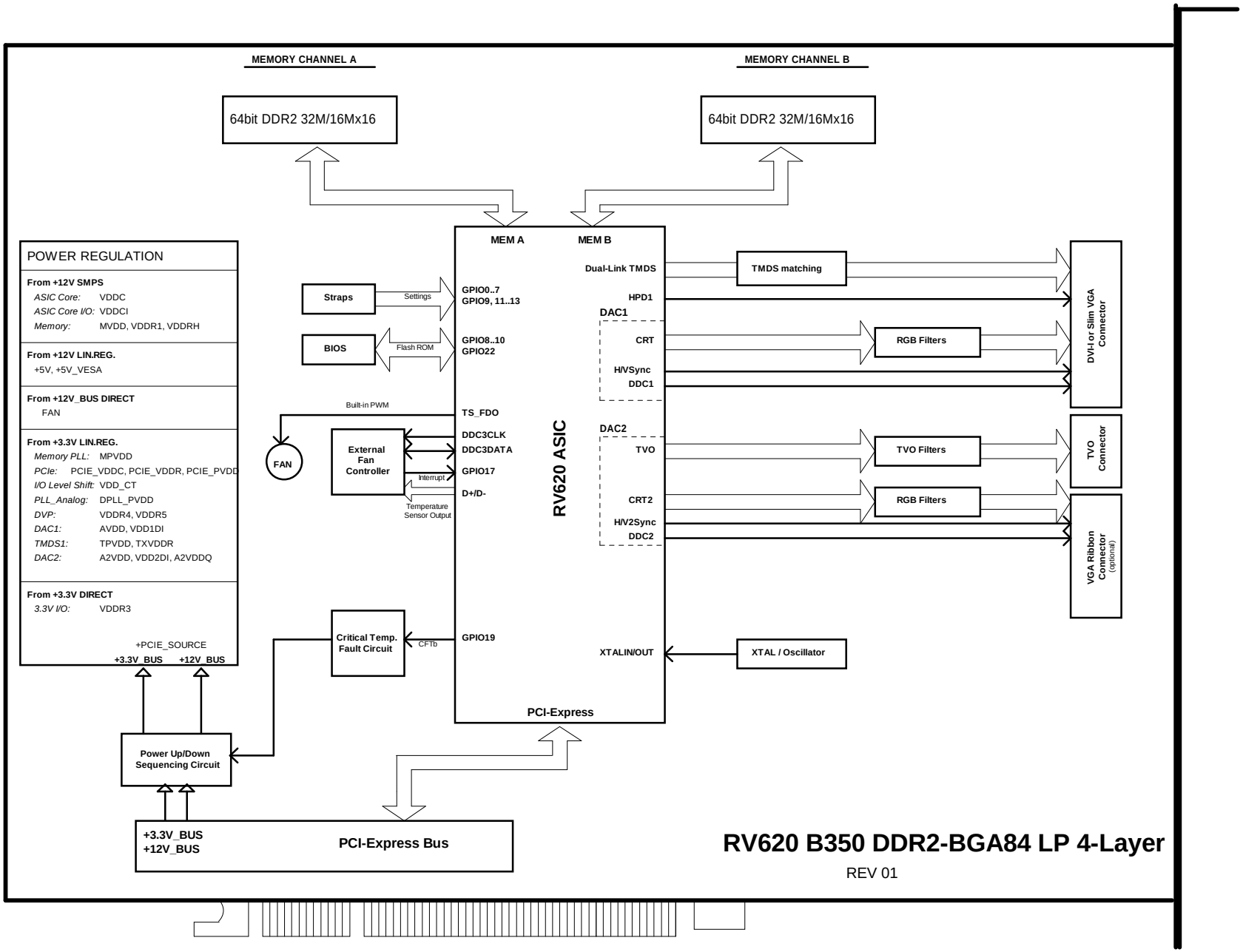
Title	Schematic No.	Date:
RH RV620 256/128MB DDR2-BGA84 32/16Mx16 VO dDVI	105-B350xx-00	**Tuesday, December 11, 2007**

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 00

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
01	00A	2007.05.07	START NEW SCHEMATIC. DERIVED FROM B170 (RV610) SCHEMATIC.
02	00A	2007.05.17	p. 4 MR155/R155 FIX SHORT
03	00A	2007.05.17	RM R7, NR7, R5, MB60, MR45, R45, R890, R1248, R1247, R1242, R1243, C853, C863; ADD R2, B890, MR890, C846; CHANGE R1022, R1023;
04	00A	2007.05.22	REMOVE GND_TXVSSR, GND_PVSS; AG23 NOW NC - WAS SCHEM MISTAKE; ADD R858 FOR BUO; R858 CHANGE TO 1210;
05	00A	2007.05.24	CTF: ADD Q1252, R1254, R1255, R1256, R1258, Q1253, Q1254, CHANGE U1250 TO SINGLE FF; UPDATE BLOCK DIAGRAM.
06	00A	2007.05.25	LVTM: ADD R110, RM R109, MR109, R108, R107;
07	00A	2007.05.28	LVTM: ADD C118, RM C104; REMOVE MR85, MR86 FOR SIMPLIFICATION;
08	00A	2007.05.28	XTALIN/OUT: LAYOUT EASEMENT; REMOVE MR108 (R849 ALREADY THERE); LVTM: ADD C119 (LOWER COST OPTION); POWER SUPPLY: REMOVE R706, MR707, R606 & MR607;
09	00A	2007.05.29	REMOVAL OF +5V: ADD R861, MR861, R862, REG861, R869, R863, R867; REMOVE MU830, U830, C830. R833, R834, C831, R832, MR832, R831, MR831; CONNECT DDC TO 5V_VESA;
010	00A	2007.05.30	CHNG C858 TO 3.3VBUS; CONNECTION TO R845 CHNG; ADD R870, MR870, C867;
011	00A	2007.05.30	REMOVE R4033; REMOVE B201-204; ADD R30-33 [PLACE NEAR ASIC]; REMOVE R3004, R3005;
012	00A	2007.05.31	REMOVE C164-C166, C170, C172 PER SIMULATION RESULTS - THESE CAPS DO NOT IMPROVE DECOUPLING. RM TP860 (LAYOUT CONSTRAINTS. ALREADY ICT TP ON THAT NET);
013	00A	2007.05.31	RM R154-R157, MR154-157 -> FUNCTIONALITY TAKEN BY EXISTING STRAPS. LAYOUT USE PLACE OF M/R154-7; ADD R7; RM MR706, MR606, B889, R863; ADD D861;
014	00A	2007.05.32	ADD SOCKET SK1
015	00A	2007.06.1	SK? CORRECTED TO SK1.
016	00B	2007.06.25	NO NETLIST CHANGES; - MOUNTING HOLES CHANGED TO 3.175mm;
017	00	2007.10.01	p. 1 - CONNECT B7 TO GND (SEE PA RV6XX H1) - REMOVE R2. IT IS ALWAYS POPULATED, NO NEED TO ZERO OHM. THIS BOARD DOES NOT SUPPORT JTAG DEBUG; p. 11 - REMOVE R839. THIS CIRCUIT IS VERIFIED, THERE IS NO NEED TO BE ABLE TO DISCONNECT IT; p. 12 - REMOVE R870 - THIS OPTION NOT USED, VCNTRL MUST BE HIGHER THAN +3.3V; - MR870 REMOVED - ALWAYS POPULATED, DO NOT NEED ZERO OHM RESISTOR OPTION; - REMOVE R860 - WAS BRING UP ONLY OPTION; p. 17 - REPLACED FAN CIRCUIT WITH ONE THAT HAS FEEDBACK: - ADD R4033, R4031, R4019, R4034, R4006, R4035, Q4004, R4035, Q40002. R4009, R4011, Q4003, R4012, R4013;
018	00	2007.12.11	P.16-Base on105-B350XX-00.DSN remove TV-OUT function: -Remove R3001-3003,C3001-3006,L3001-3003 -Remove R3006-3011,C3007-3010,J3001



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Date:	Thursday, November 29, 2007
Rev	00
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