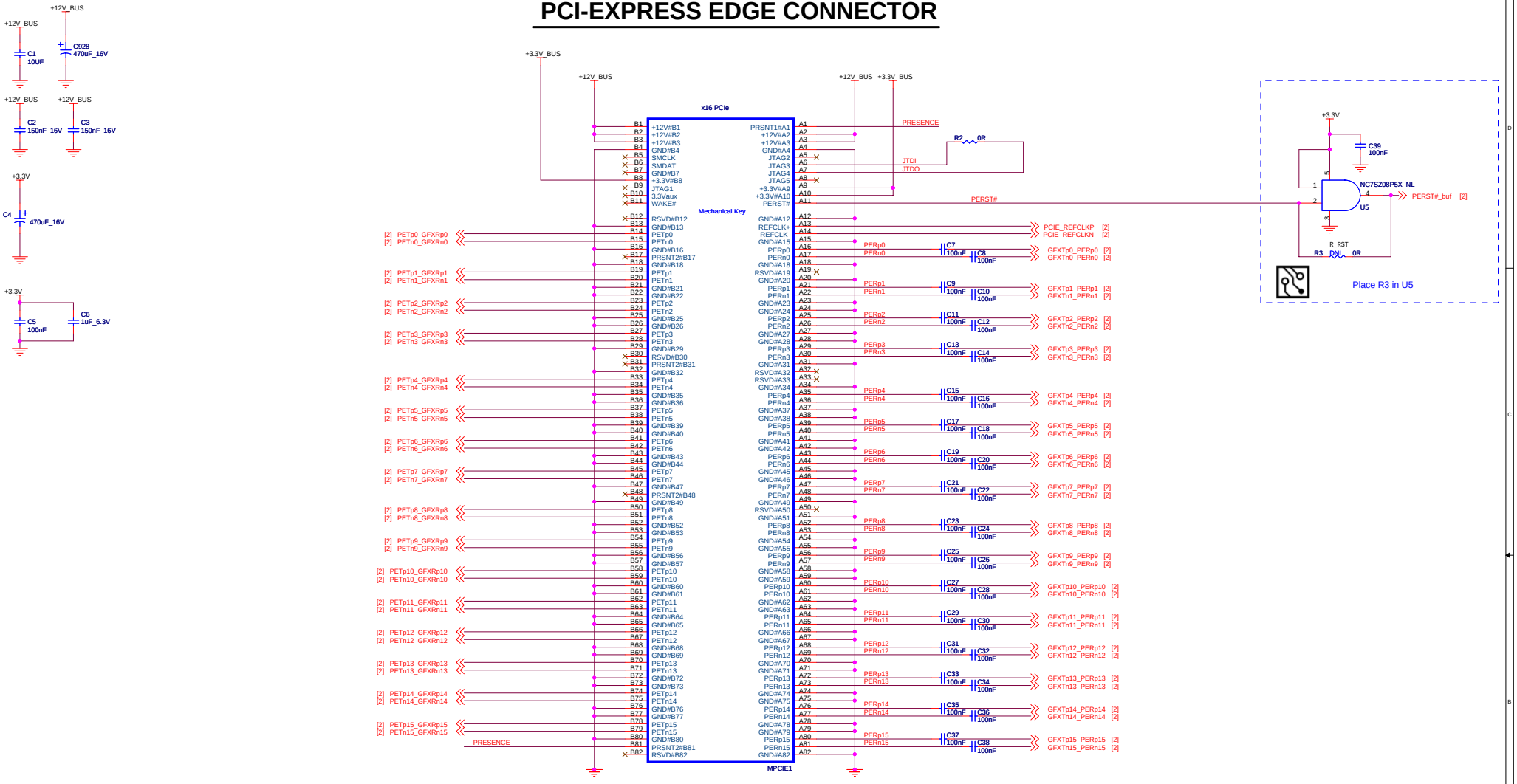
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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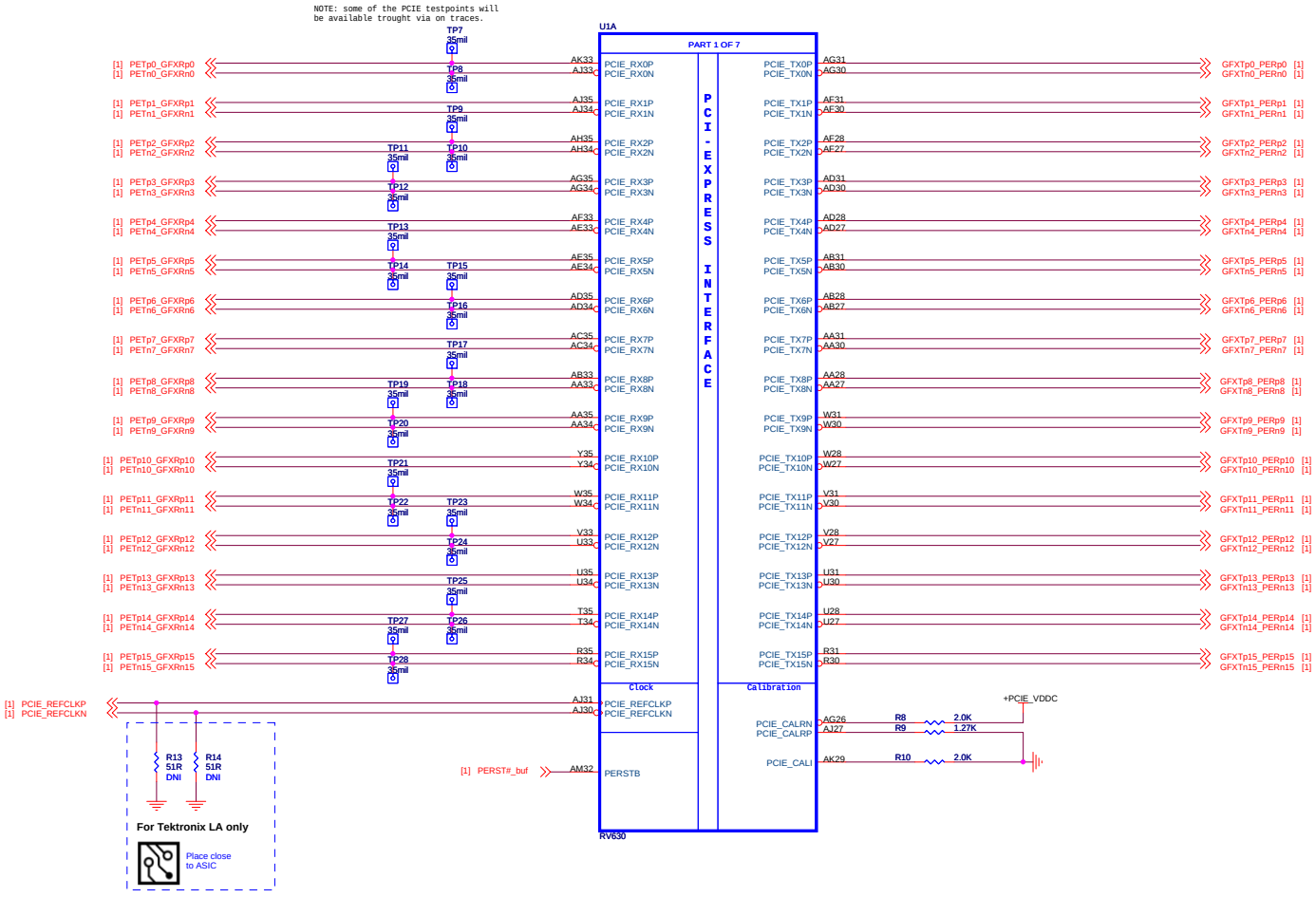
Title	RH PCIE RV630 DDR2- PCIE CONNECTOR		
Size C	Document Number 105-B149xx-00C		Rev 0.1c
Date: Wednesday, March 28, 2007		Sheet 1 of 21	



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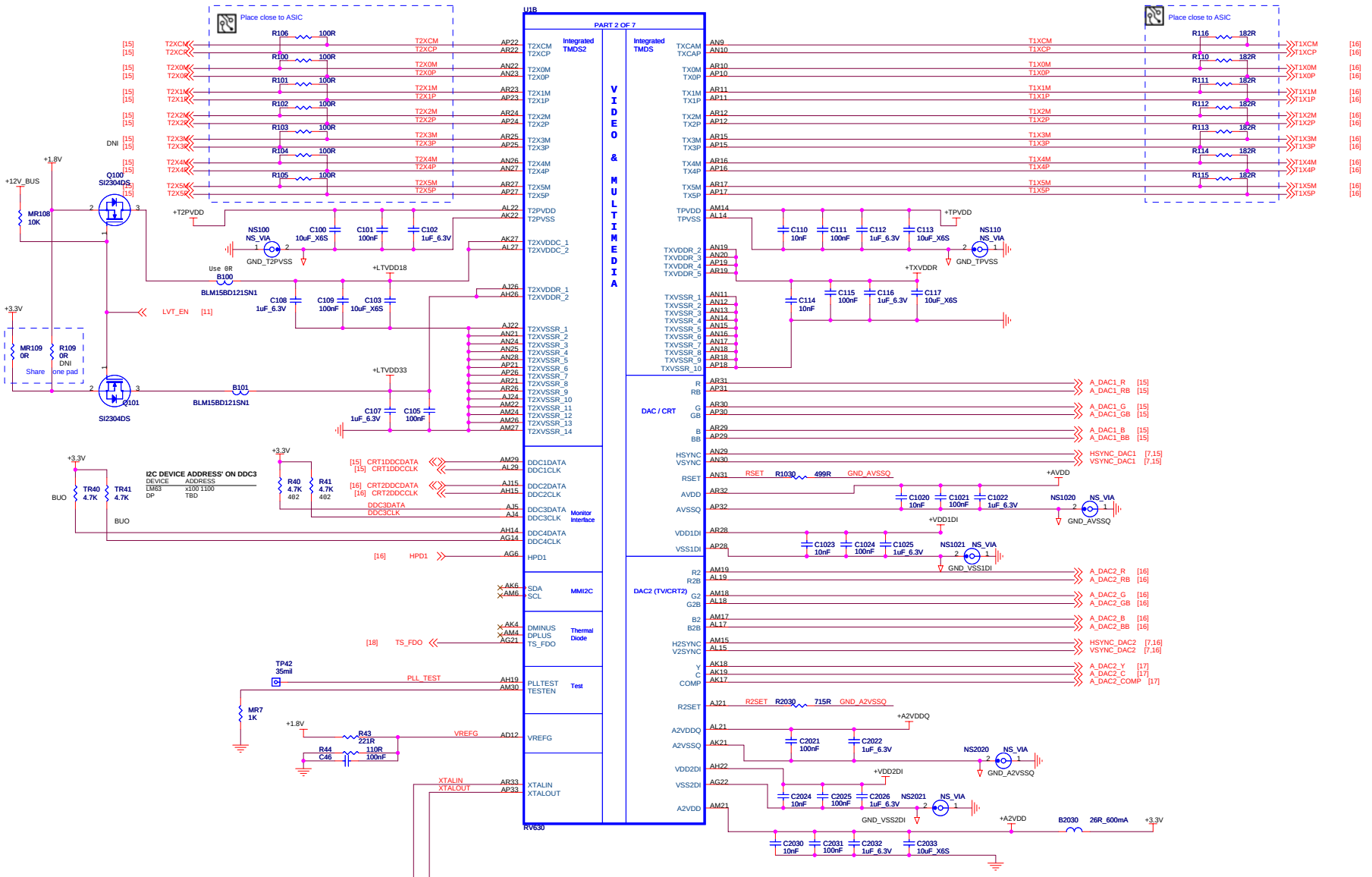
Title	RV630 DDR2- ASIC PCIE I/F		
Size C	Document Number 105-B149xx-00C		Rev 0.1c
Date: Wednesday, March 28, 2007		Sheet 2 of 21	

Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402



Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402

U1E

PART 5 OF 7

Memory I/O

PCI-Express

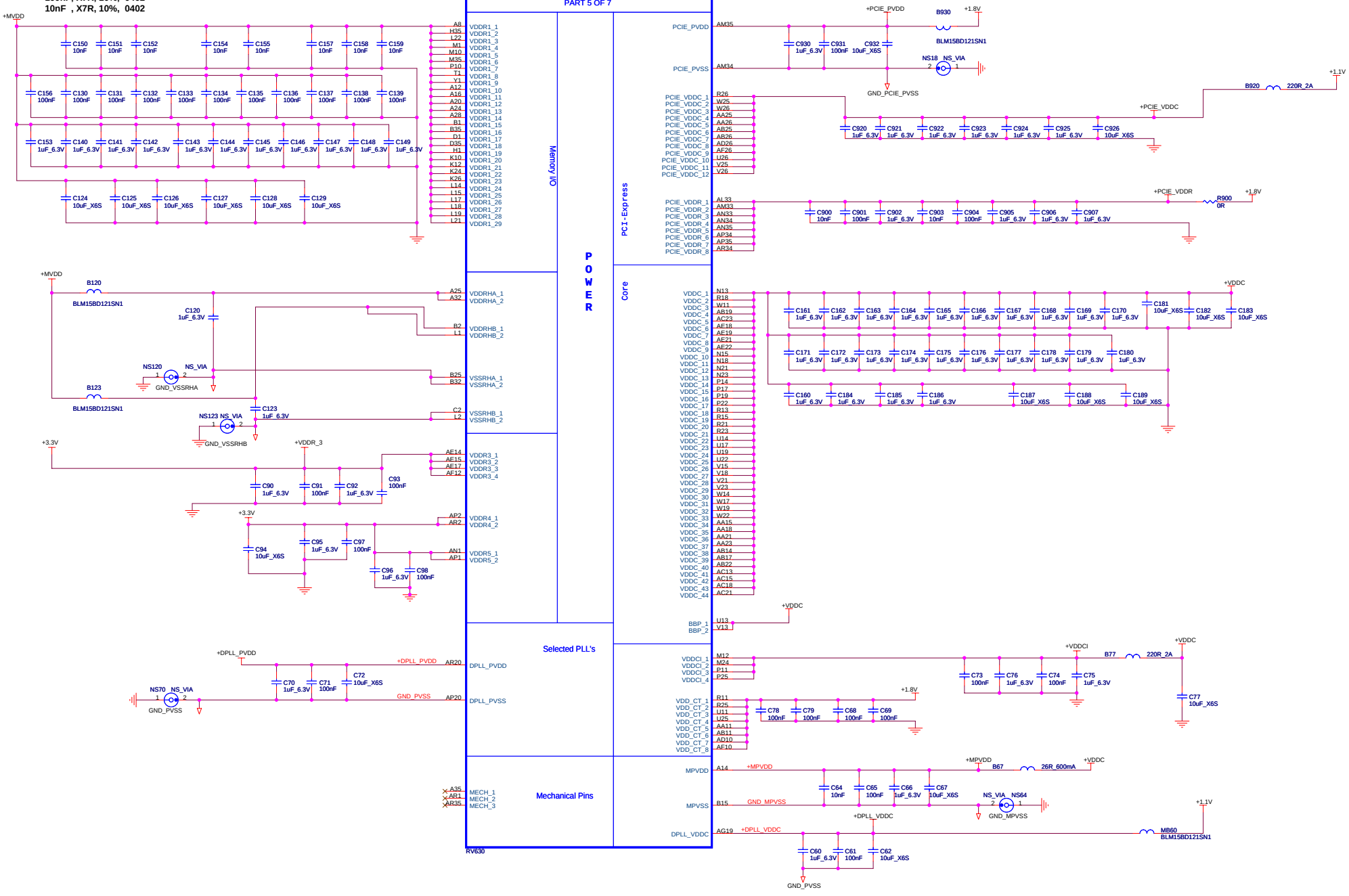
Core

Selected PLL's

Mechanical Pins

POWER

RV630



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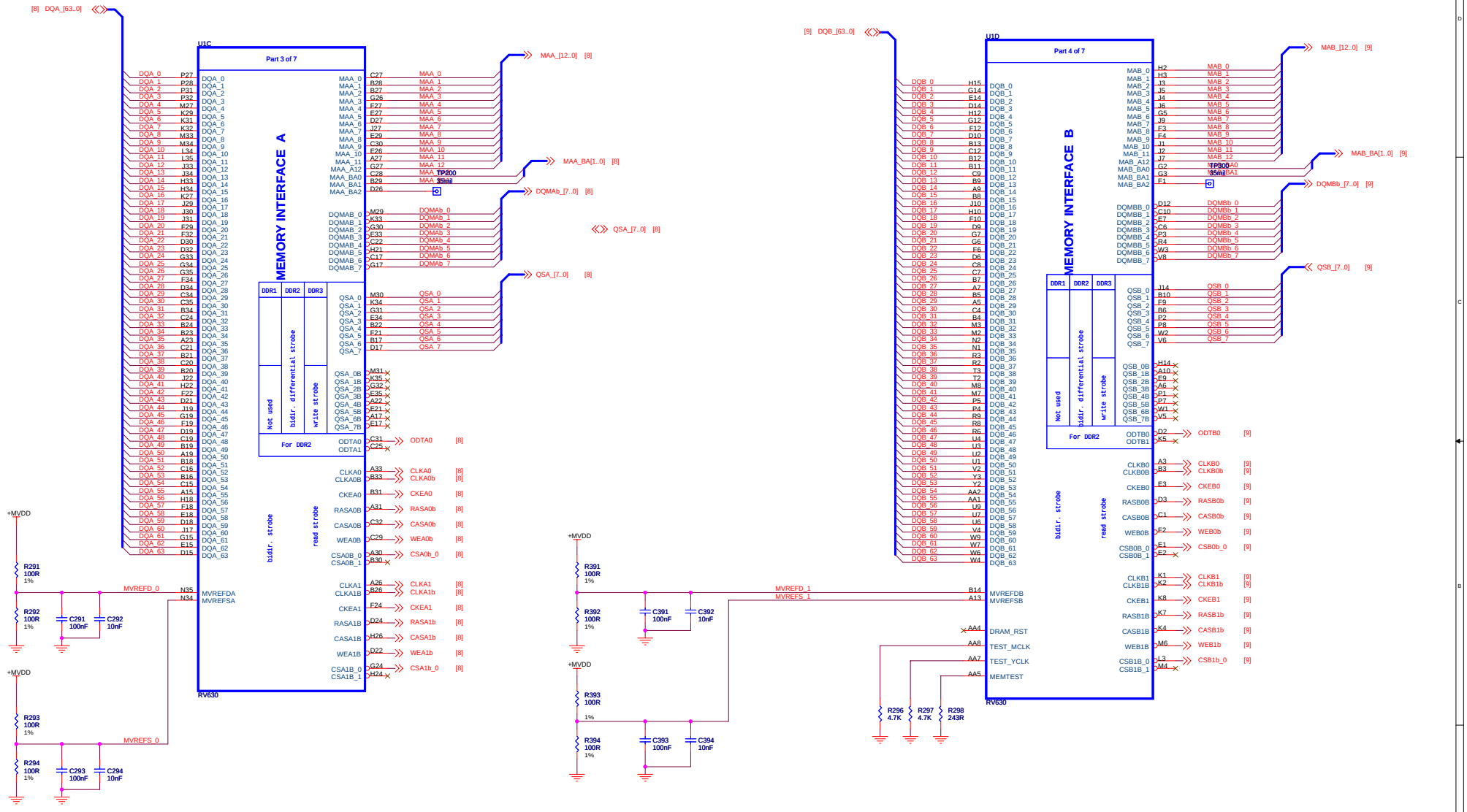
Title	RV630 DDR2- ASIC POWERS		
Size C	Document Number 105-B149xx-00C		Rev 0.1c
Date: Wednesday, March 28, 2007		Sheet 4 of 21	



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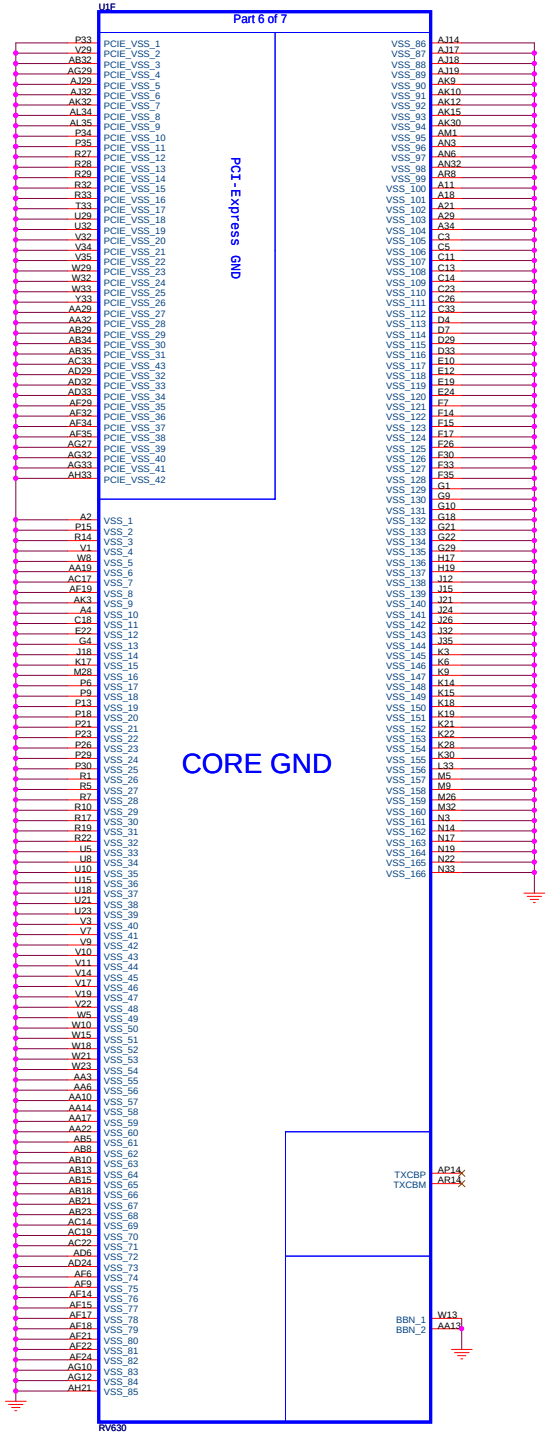
Title	RV630 DDR2- ASIC MEM		
Size C	Document Number 105-B149xx-00C		Rev 0.1c
Date: Wednesday, March 28, 2007		Sheet 5 of 21	



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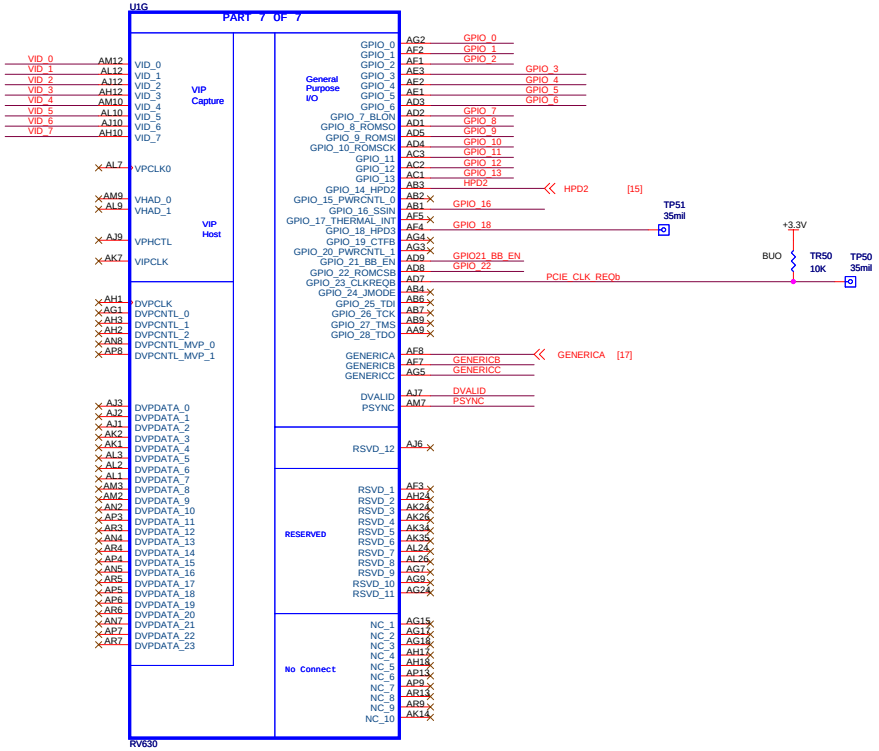
Title: RV630 DDR2- ASIC GROUNDS

Size	Document Number	Rev
C	105-B149xx-00C	0.1c

Date: Wednesday, March 28, 2007 Sheet 6 of 21



PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

ATI Internal Use Only - Reserved (Default: 00)

DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

ATI Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0]
0010 - 512Kbit AT25F512A (Atmel)
0011 - 1Mbit AT25F1024A (Atmel)
0100 - 512Kbit M25P05A (ST)
0101 - 1Mbit M25P10A (ST)
0101 - 2Mbit M25P20 (ST)
0100 - 512Kbit Pm25LV512 (Chingis)
0101 - 1Mbit Pm25LV010 (Chingis)

ATI Internal Use Only - Reserved (Default: 0)

VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

ATI Internal Use Only - Reserved

VGA DISABLE : 1 for disable (set to 0 for normal operation)

ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

MSI_DIS (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

BIF_AUDIO_EN
0 - Disable HD Audio 1- Enable HD Audio

ATI Internal Use Only - Reserved (Default: 0)

64BAR_EN_A (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

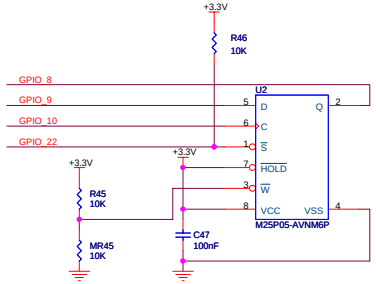
ATI Internal Use Only - Reserved (Default: 0)

MEMORY CONFIG ATI Board Feature I

VSYNC_DAC2 CHECK ATI MEMORY
GPIO18 TUNING DOCUMENT

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

Pull-Down Resistors are for BU until built-in pull-downs are verified.



113-B149XX-XXX
VIDEO BIOS
FIRMWARE

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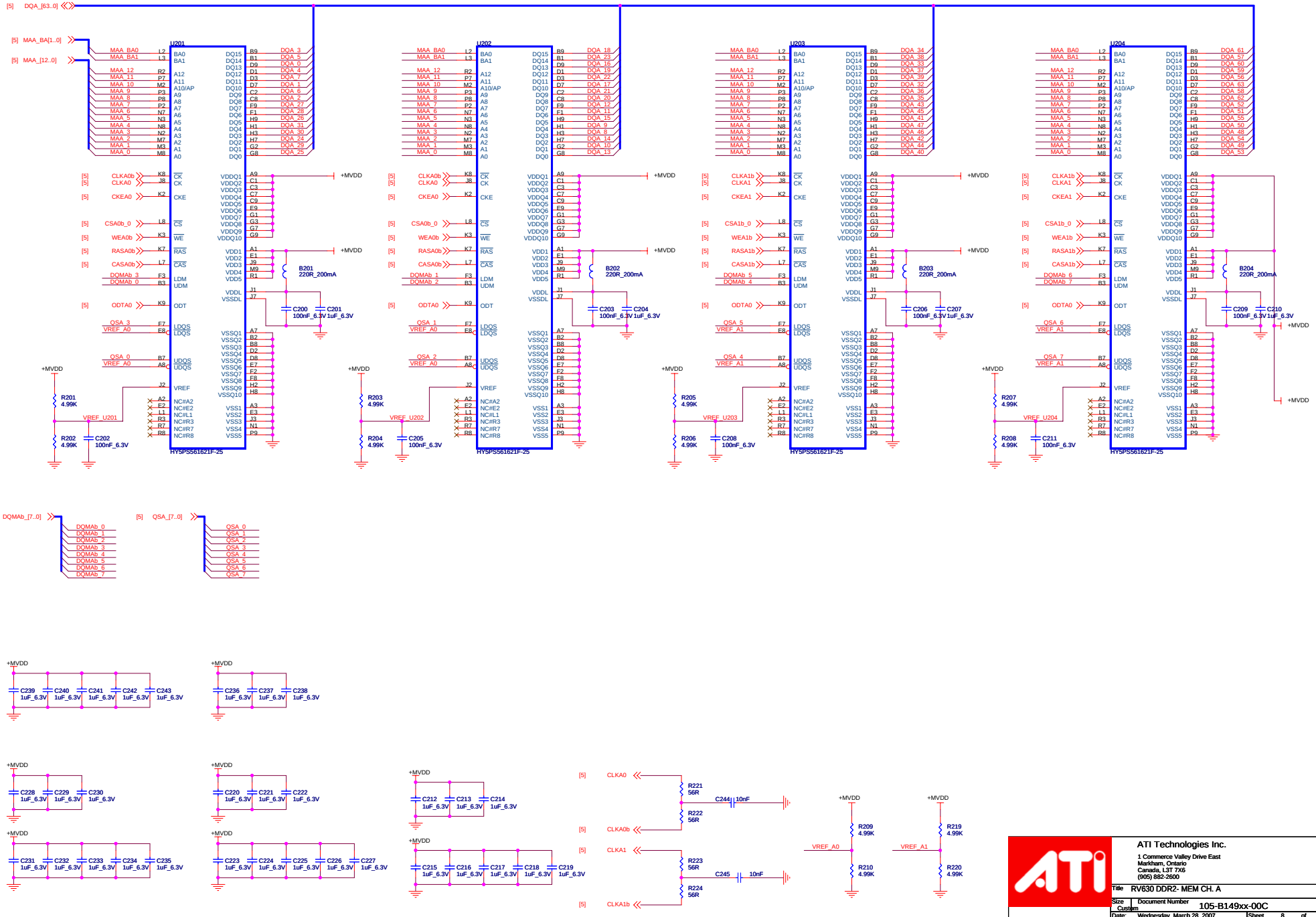
Title	RV630 DDR2- ASIC DVO-BOOT SRAPS		
Size C	Document Number 105-B149xx-00C		Rev 0.1c
Date: Wednesday, March 28, 2007		Sheet 7 of 21	

CHANNEL A: 128MB/256MB DDR2



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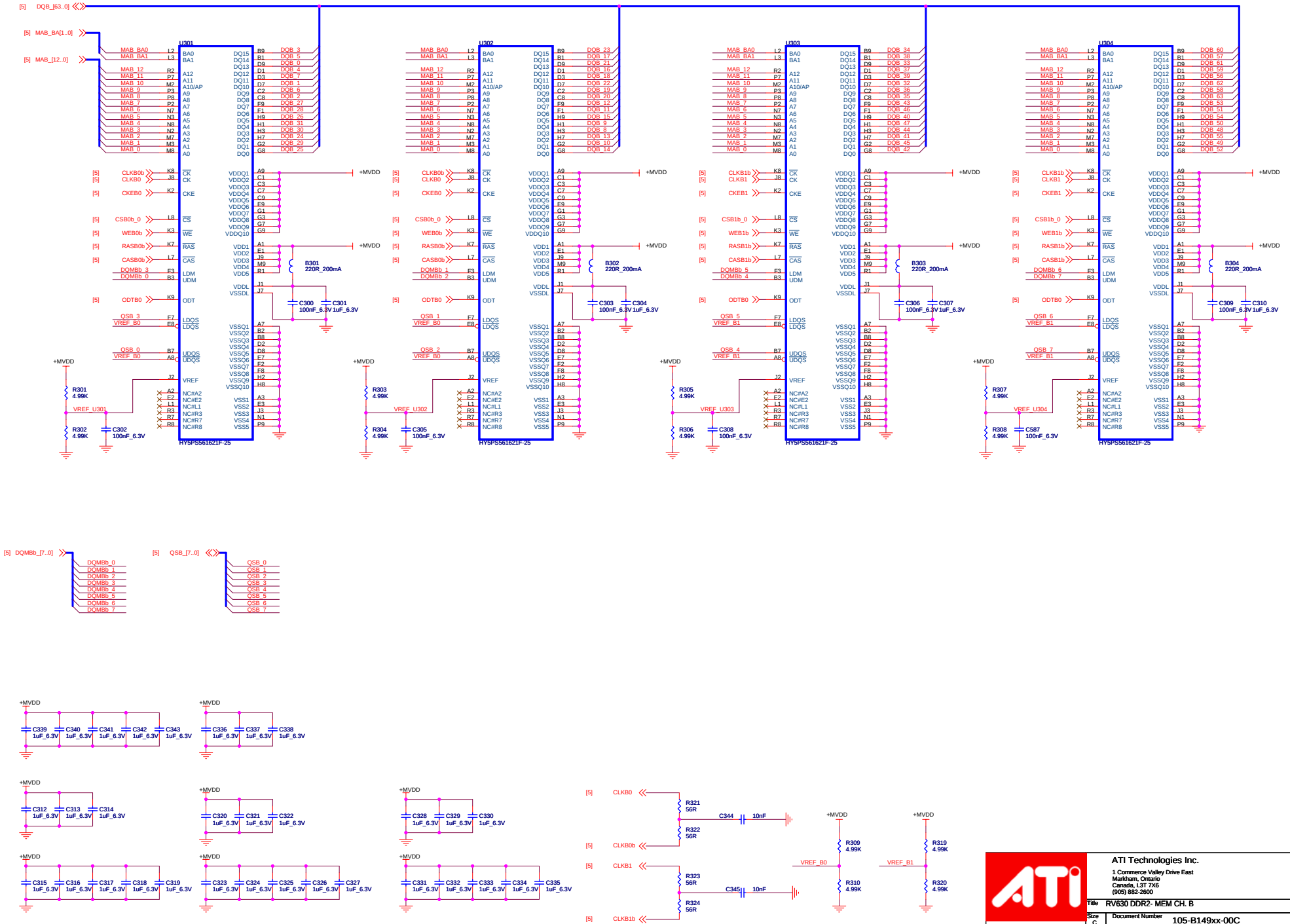
1 Commerce Valley Drive East Markham, Ontario Canada, L3T 7X6 (905) 882-2600			
Title	RV630 DDR2- MEM CH. A		
Size: Custom	Document Number: 105-B149xx-00C		Rev: 0.1c
Date: Wednesday, March 28, 2007	Sheet 8 of 21		

CHANNEL B: 128MB/256MB DDR2



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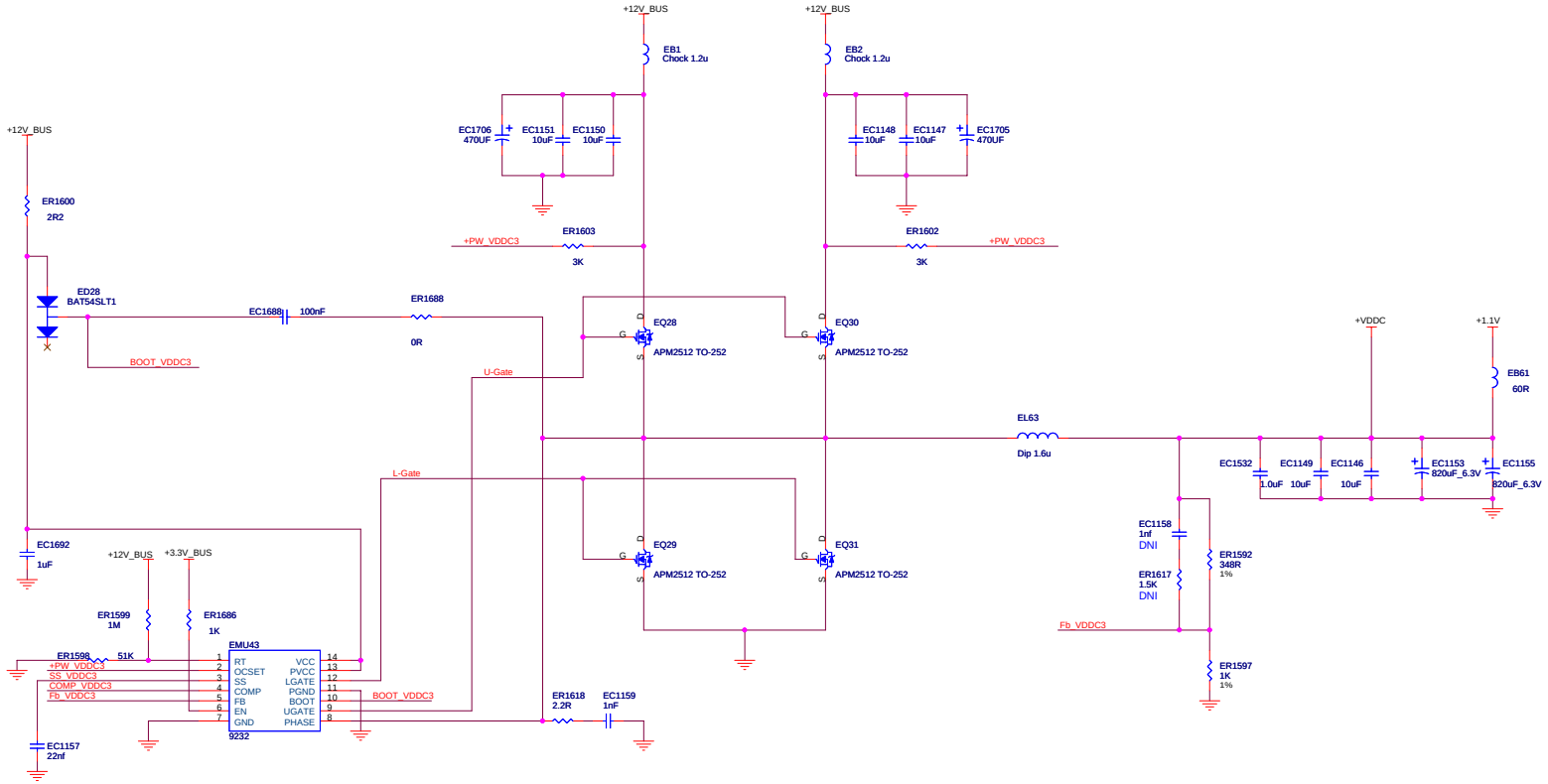
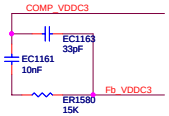
Title	RV630 DDR2- MEM CH. B	
Size C	Document Number 105-B149xx-00C	Rev 0.1c
Date: Wednesday, March 28, 2007	Sheet 9 of 21	

CORE REGULATOR VDDC



+VDDC=0.8*(1+(ER1592 / ER1597))

Compensation Circuit



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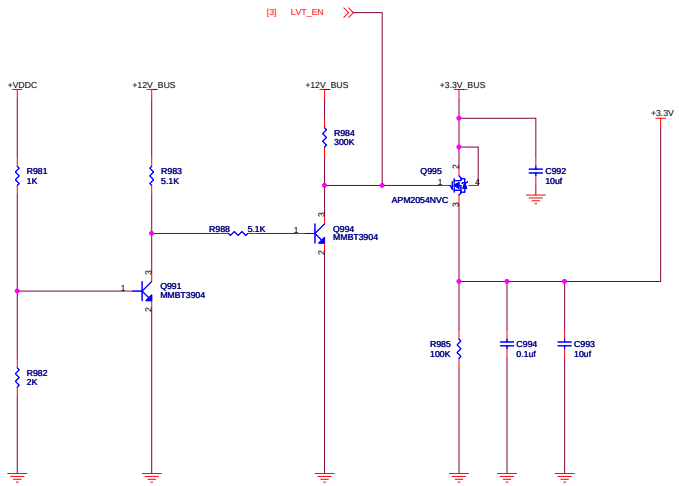
Title TR RV630 - MVDD SMPS02

Size	Document Number	Rev
Custom	105-B149xx-00C	0.1c

Date: Wednesday, March 28, 2007 Sheet 10 of 21



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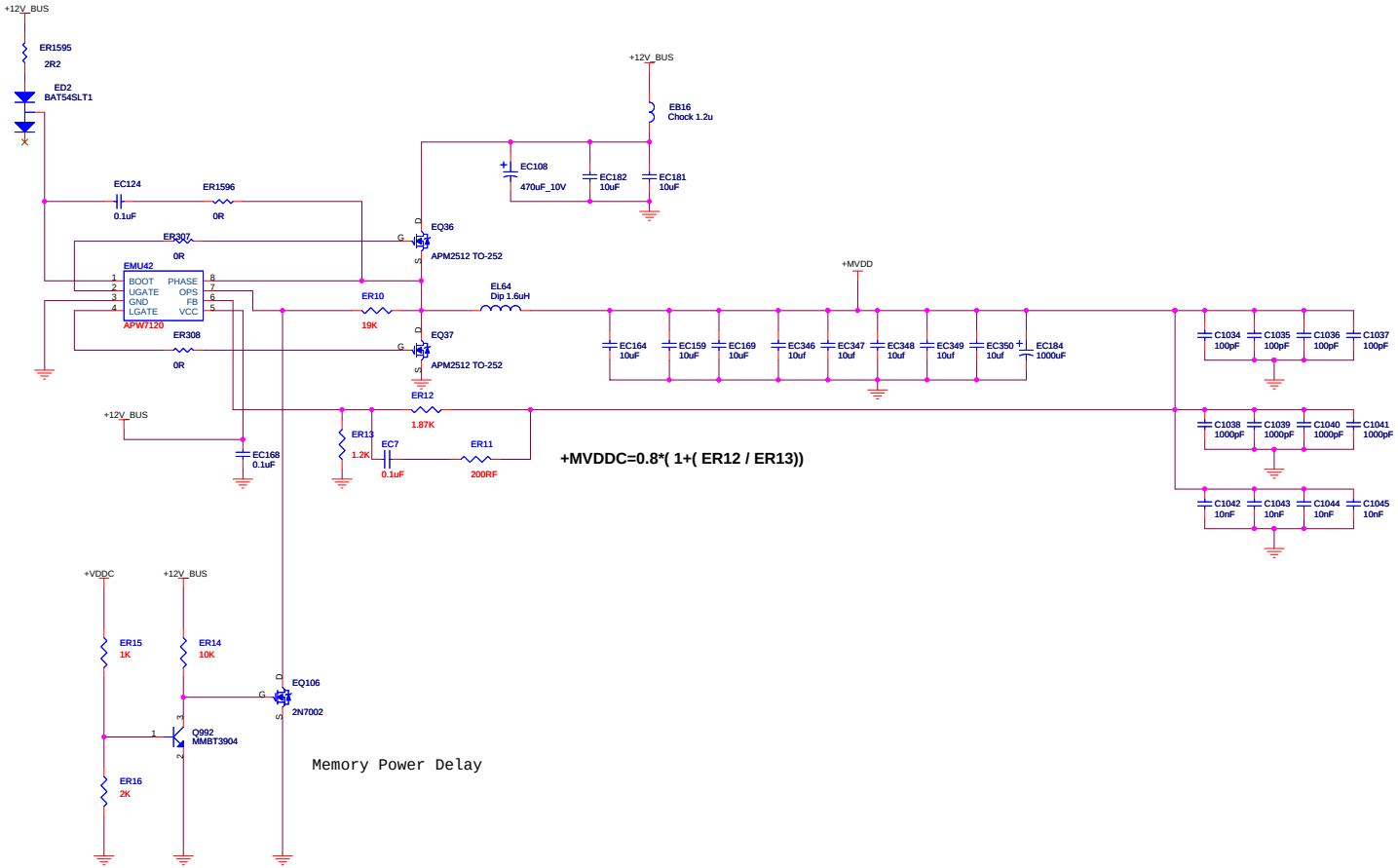
Title	RV630 DDR2- VDDC SMPS	
Size: Custom	Document Number: 105-B149xx-00C	Rev: 0.1c
Date: Wednesday, March 28, 2007	Sheet 11 of 21	



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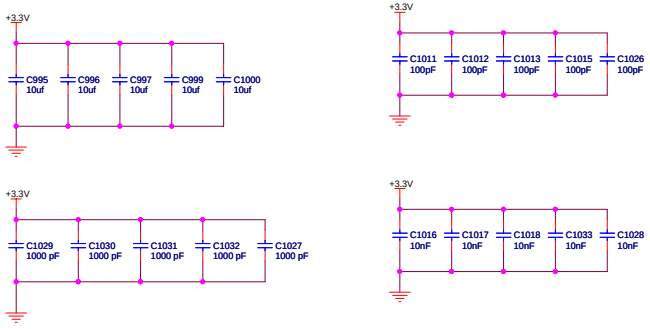
Title	TR RV630 - MVDD SMPS02	
Size: Custom	Document Number: 105-B149xx-00C	Rev: 0.1c
Date: Wednesday, March 28, 2007	Sheet 12 of 21	



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Title	RV630 DDR2- POWER MANAGMENT	
Size: C	Document Number: 105-B149xx-00C	Rev: 0.1c
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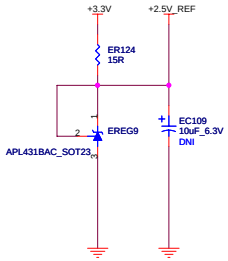
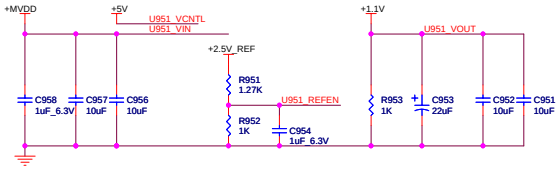
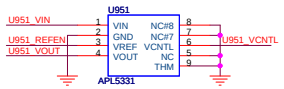
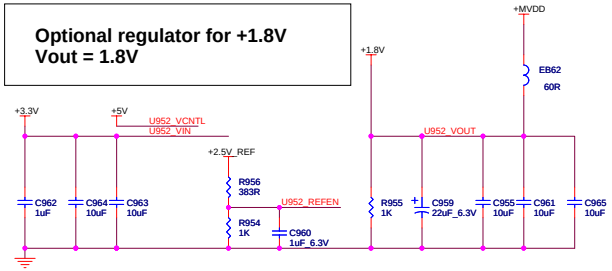


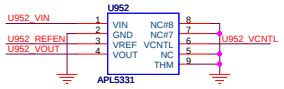
Optional regulator for +1.1V
Vout = 1.1V

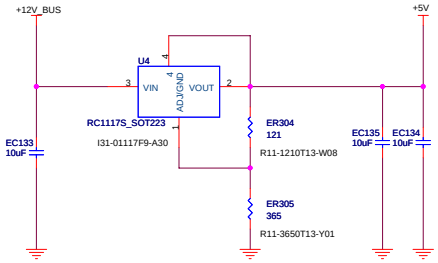




Optional regulator for +1.8V
Vout = 1.8V

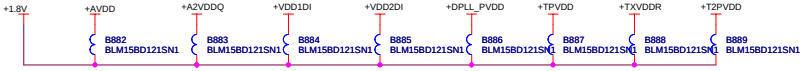






Vout=1.25V* [1+(ER305/ER304)]

Shared Power Rails



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Title	TR RV630 - Linear Regulators	
Size C	Document Number 105-B149xx-00C	Rev 0.1c
Date: Wednesday, March 28, 2007	Sheet 14 of 21	

See BOM for qualified filters

[3] A_DAC1_R — R1001 75R — C1004 8.0pF — L1001 68nH_300mA — A_R_DAC1_M — C1001 12pF_50V — L1004 36NH

[3] A_DAC1_RB — R1027 37.4R

[3] A_DAC1_G — R1002 75R — C1005 8.0pF — L1002 68nH_300mA — A_G_DAC1_M — C1002 12pF_50V — L1005 36NH

[3] A_DAC1_GB — R1028 37.4R

[3] A_DAC1_B — R1003 75R — C1006 8.0pF — L1003 68nH_300mA — A_B_DAC1_M — C1003 12pF_50V — L1006 36NH

[3] A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

+3.3V — BAT54SLT1 ED62 — BAT54SLT1 ED63 — BAT54SLT1 ED64

+5V — EF1 1.5A — +5V_VESA

MJ1001 G3179C219-005
1 R
2 G
3 B
11 MS0
12 MS1
4 MS2
15 MS3
9 NC
13 HS
14 VS
5 VSS
6 VSS#6
7 VSS#7
8 VSS#8
10 VSS#10
16 CASE
17 CASE#17

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

C1010 104pF

+5V — ED71 BAT54SLT1 — ED70 BAT54SLT1 — ED69 BAT54SLT1 — ED68 BAT54SLT1

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
Hardware	Mechanical Key	1A max	1A max	1A max	
Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

+3.3V — R1004 10K — +5V — R1005 2.2K — [3] CRT1DDCDATA — Q1001 BSH111 — DDCDATA_DAC1_5V — R1006 33R — DDCDATA_DAC1_R

+3.3V — R1007 10K — +5V — R1008 2.2K — [3] CRT1DDCCLK — Q1002 BSH111 — DDCCLK_DAC1_5V — R1009 33R — DDCCLK_DAC1_R

C1999 100nF — +5V

[3,7] HSYNC_DAC1 — U1999A SN74HCT125D — HSYNC_DAC1_B — R1010 10R — HSYNC_DAC1_R

[3,7] VSYNC_DAC1 — U1999B SN74HCT125D — VSYNC_DAC1_B — R1011 10R — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

+3.3V — Q1021 MMBT3904 — R1022 10K — HPD_DVI2 — [7] HPD2 — R1023 10K

+5V_VESA — J1001 DVI_CONNECTOR

25	CASE		
1	TMDS Data2-	[3]	T2X2M
2	TMDS Data2+	[3]	T2X2P
3	TMDS Data2/4 Shield		
4	TMDS Data4-	[3]	T2X4M
5	TMDS Data4+	[3]	T2X4P
6	DDC Clock		DDCCLK_DAC1_R
7	DDC Data		DDCDATA_DAC1_R
8	Analog VSYNC		VSYNC_DAC1_R
9	TMDS Data1-	[3]	T2X1M
10	TMDS Data1+	[3]	T2X1P
11	TMDS Data1/3 Shield		
12	TMDS Data3-	[3]	T2X3M
13	TMDS Data3+	[3]	T2X3P
14	+5V Power		
15	GND (for +5V)		
16	Hot Plug Detect		HPD_DVI2
17	TMDS Data0-	[3]	T2X0M
18	TMDS Data0+	[3]	T2X0P
19	TMDS Data0/5 Shield		
20	TMDS Data5-	[3]	T2X5M
21	TMDS Data5+	[3]	T2X5P
22	TMDS Clock Shield		
23	TMDS Clock+	[3]	T2XCP
24	TMDS Clock-	[3]	T2XCM
C1	Analog Red		A_R_DAC1_F
C2	Analog Green		A_G_DAC1_F
C3	Analog Blue		A_B_DAC1_F
C4	Analog HYNC		HSYNC_DAC1_R
C5	Analog GND		
C6	Analog GND#C6		
26	CASE#26		
27	CASE#27		
28	CASE#28		
29	CASE#29		
30	CASE#30		

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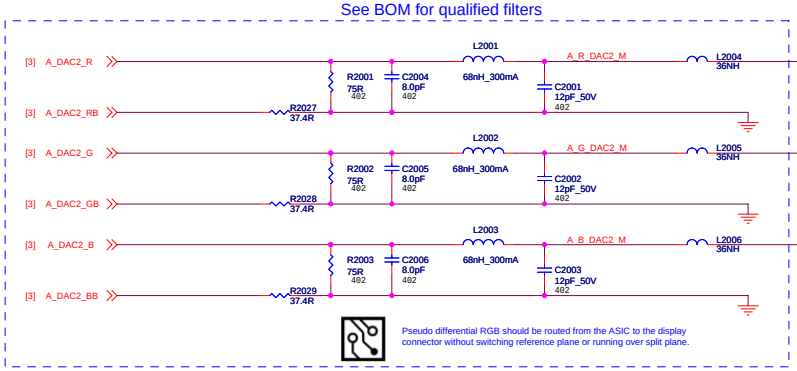
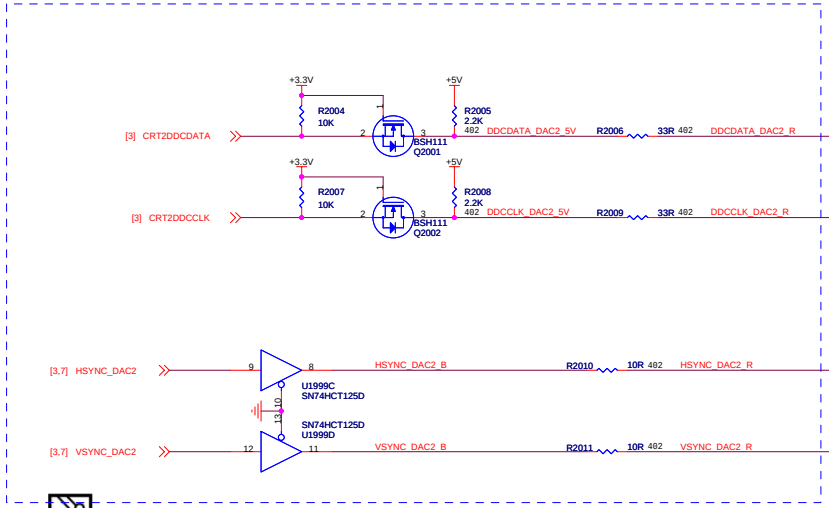
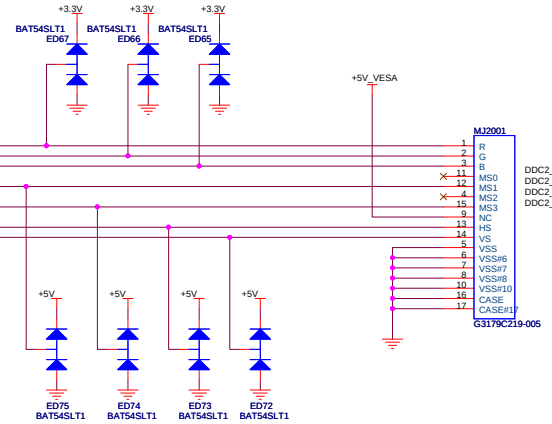
Title: RV630 DDR2- DAC1&TMDS2
Size: Custom — Document Number: 105-B149xx-00C — Rev: 0.1c
Date: Wednesday, March 28, 2007 — Sheet 15 of 21

See BOM for qualified filters

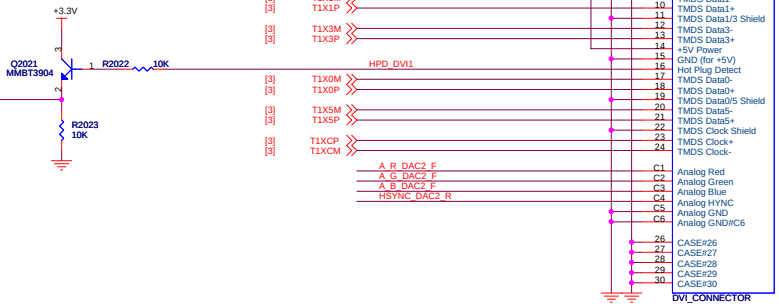






DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



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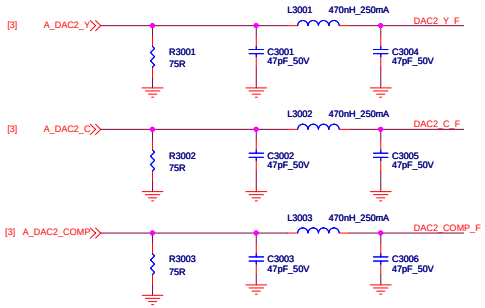
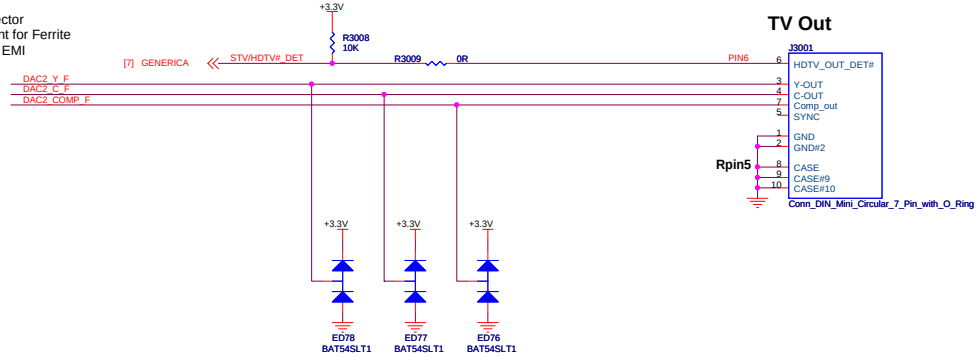
Title	RV630 DDR2-DAC2/TMDS1	
Size: Custom	Document Number: 105-B149xx-00C	Rev: 0.1c
Date: Wednesday, March 28, 2007	Sheet 16 of 21	



Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI



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Title	RV630 DDR2 - TVO	
Size: C	Document Number: 105-B149xx-00C	Rev: 0.1c
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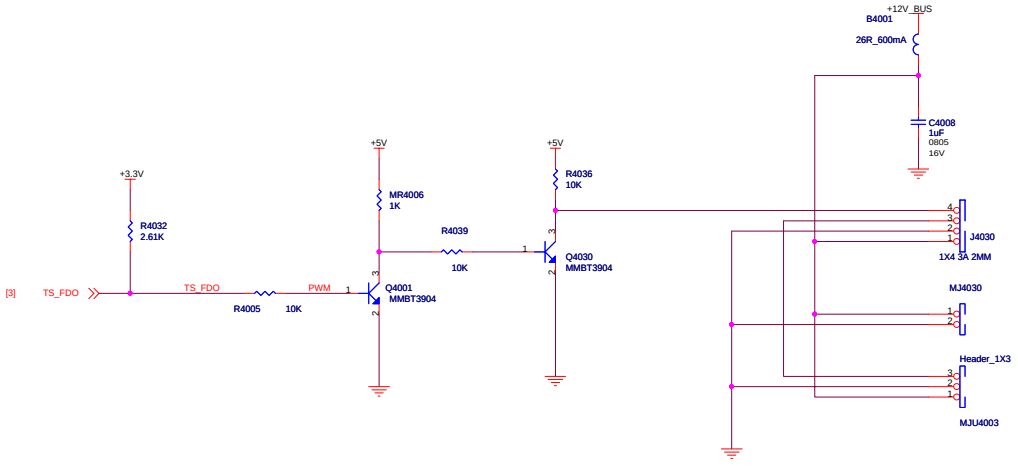

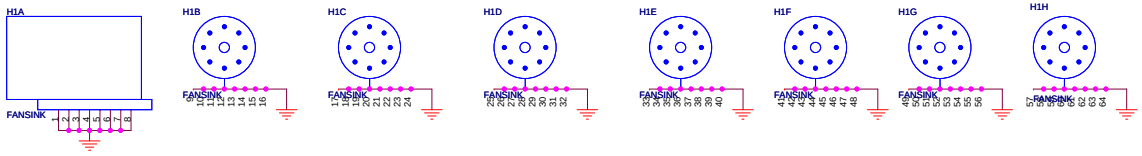

FANSINK FOR RV630 DDR2, p/n 7120033200G

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Title	RV630 DDR2-THERMAL MANAGEMENT	
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DVI/DVI SCREWS with top tab

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT

ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
ASSY-SCREW

MT1
MT_Hole_0.136_in.

MT2
MT_Hole_0.136_in_6VIA

PCB1
PCB
109-B14931-00C

ASSY1
ANTISTATIC BAG
6_X_11

ASSY2
BRACKET
8020038600G

SK1
RV410SOCKET

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM4 SW_FB
FM5 SW_FB
FM6 SW_FB

J1 X_PIN1*2
J2 X_PIN1*2
J3 X_PIN1*2
J4 X_PIN1*2
J5 X_PIN1*2
J6 X_PIN1*2
J7 X_PIN1*2
J8 X_PIN1*2
J9 X_PIN1*2

<Variant Name>

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Title	RV630 DDR2-MECHANICAL		
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<variant Name>

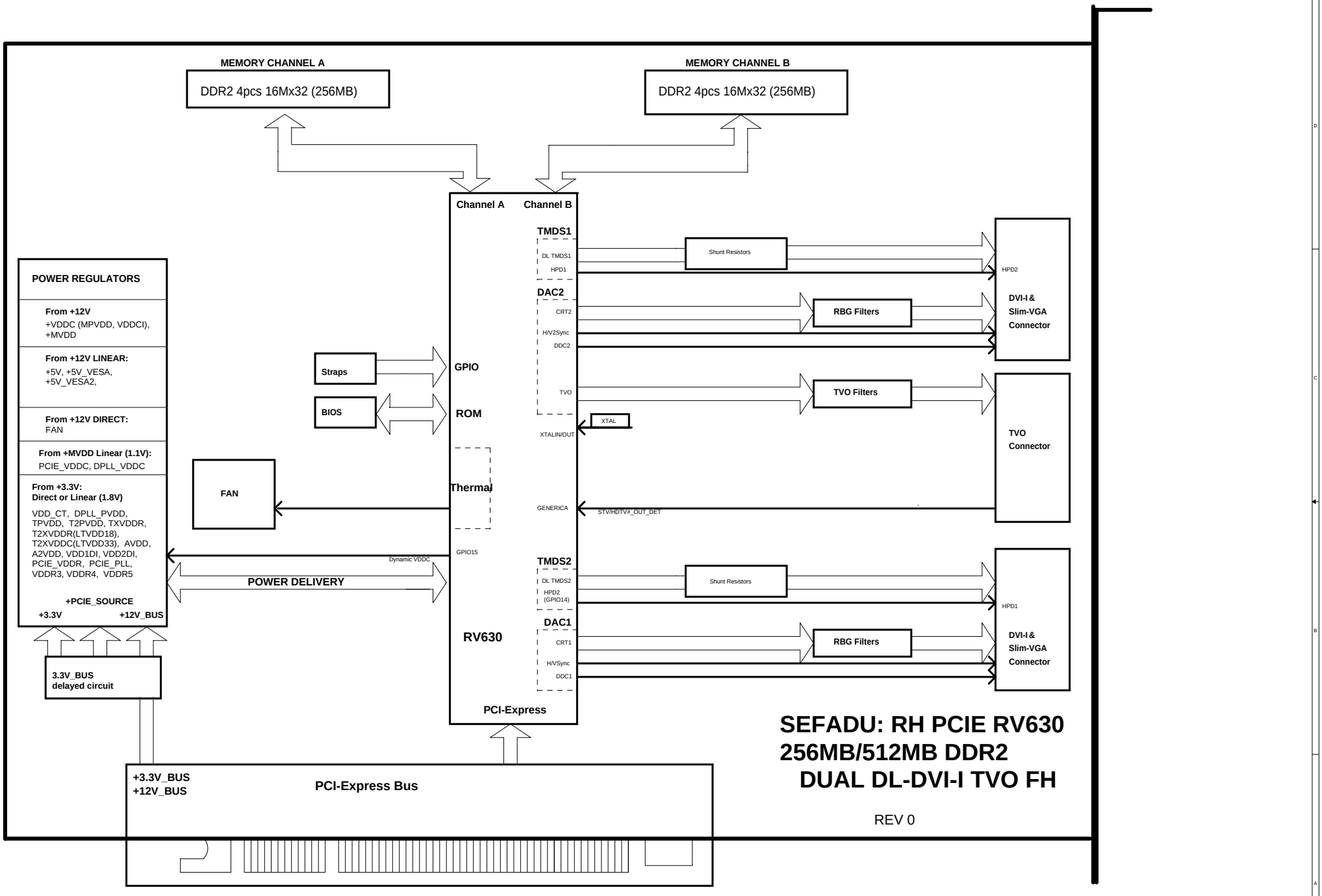
Title	Schematic No.	Date:
RV630 DDR2-REVISION HISTORY	105-B149xx-00C	Wednesday, March 28, 2007

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact ATI representative to obtain latest BOM closest to the application desired.

Rev 0.1c

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/11/17	Initial design for RV630 DDR2
00B	00B	07/01/26	THIS IS A TEST BOARD, WE WILL BASE ON THIS ONE TO DECIDE WHICH WAY WE SHOULD GO 1) CHANGING RGB CONFIGURATION FOR BOTH DAC1 AND DAC2 (PAGE 3, 14 AND 15) 2) ADD-IN Q102 AND R49 FOR VDDR3 POWER SEQUENCE CONTROL 3) CONNECT R847 TO +1.8V_D1 INSTEAD OF +1.8V_LDO2 (PAGE 13)



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Title	RV630 DDR2-BLOCK DIAGRAM	
Size: C	Document Number: 105-B149xx-00C	Rev: 0.1c
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