P977-A01: G96, GB1-128, GDDR3, DL-DVI/VGA, DL-DVI/VGA, SD/HDTV

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Page 17: SPDIF-IN, XTAL, MECHANICALS, THERMALS

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Page 19: BIOS ROM, HDCP ROM, STRAPPING OPTIONS

Page 20: POWER SUPPLY LINEARS: 5V, DDC5V, IFP PLLVDD, MIO VDD, TMDS_BACKDRIVE

Page 20: POWER SUPPLY: FBVDDQ , PEX_VDD

Page 22: POWER SUPPLY: NVVDD

REV HISTORY

Version : 0A

6/26 PAGE 16 add D701 for 4PIN FAN control protect

12/03 Memory reference: V129-4.0
Power nvdd ref : V157-1.0
Main board ref : V156-1.0

12/03 PAGE 04 ADD FBA TOP M3,M4 from V129-4.0
PAGE 05 ADD FBA BOT M5,M6 from V129-4.0
PAGE 08 ADD FBC TOP M1,M2 from V129-4.0
PAGE 09 ADD FBC BOT M7,M8 from V129-4.0

12/04 PAGE 22 SWAP power design from V157-1.0 single phase
Disable GPIO6_NVVDD_SEL function

12/08 PAGE 21 modify C108,C127,C126 footprit to 1500UF_6_3V
PAGE 22 modify C58,C500,C60 footprit to 1500UF_6_3V

12/08 PAGE 16 replace D10 from V156

12/08 modify page summary

12/10 page 22 R145.1 12V_PEX modify to 12V

12/16 page 4 & 5 & 8 & 9 swap memory bank pin request from LAYOUT

12/19 page 4 & 5 swap memory bank of M4 & M6 pin request from LAYOUT

12/22 page 22 12V change to 12V_F for good to layout

12/24 page 17 add 3 EMI solution and change 光學點footprint

12/24 page 22 change L12 L04-12A7441-M26
CHK_D2_11_5X10_8 footprint to CHK_D2_P7_4X6_2

12/24 page 21 change R511 footprint R6030 to 6030
form ME request

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10977-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10977-0001-100	G96-300, 550/800MHz 256MB 16Mx32 GDDR3 DVI+DVI+HDTV-Out
2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TABLE OF CONTENTS

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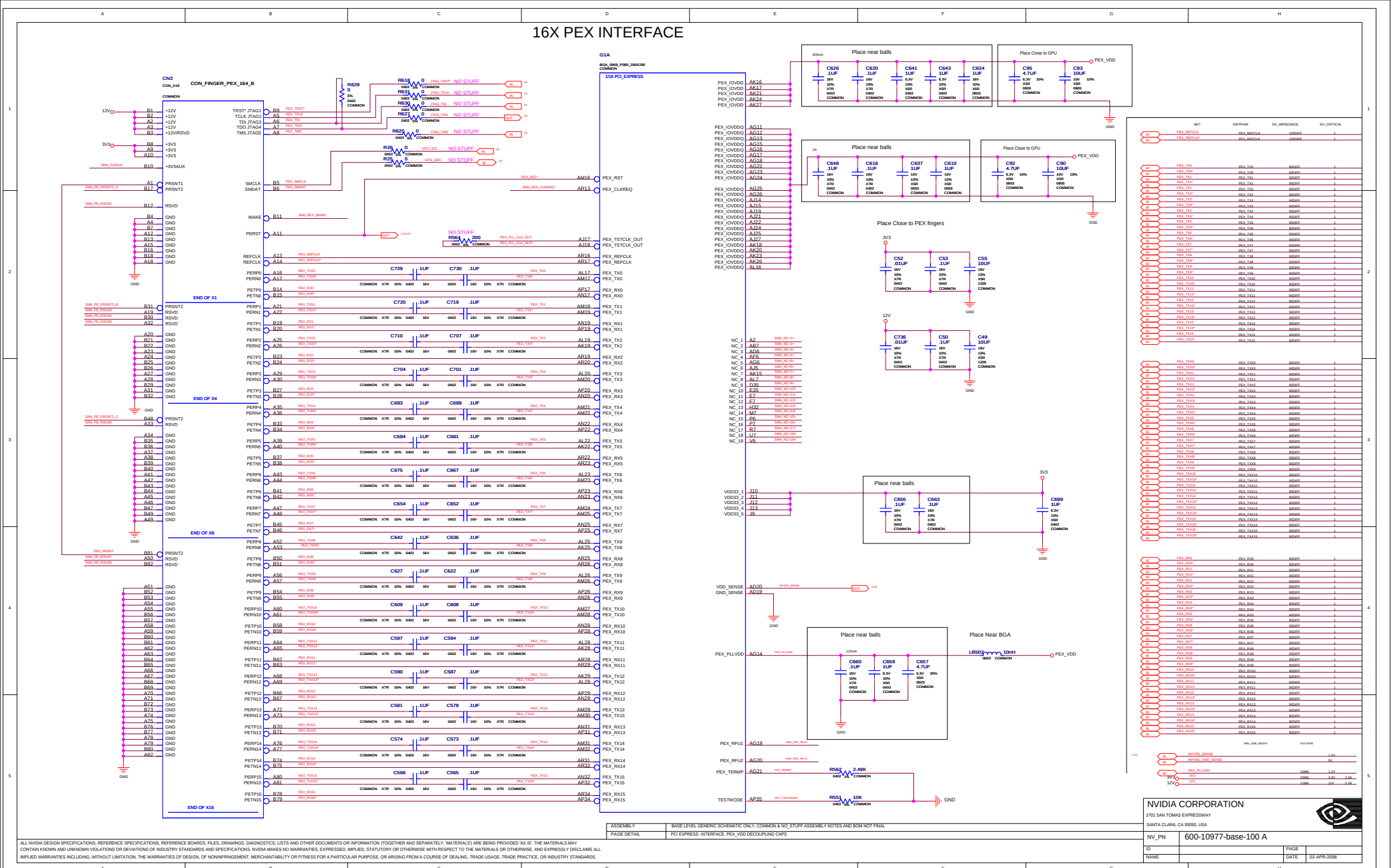
16X PEX INTERFACE



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS

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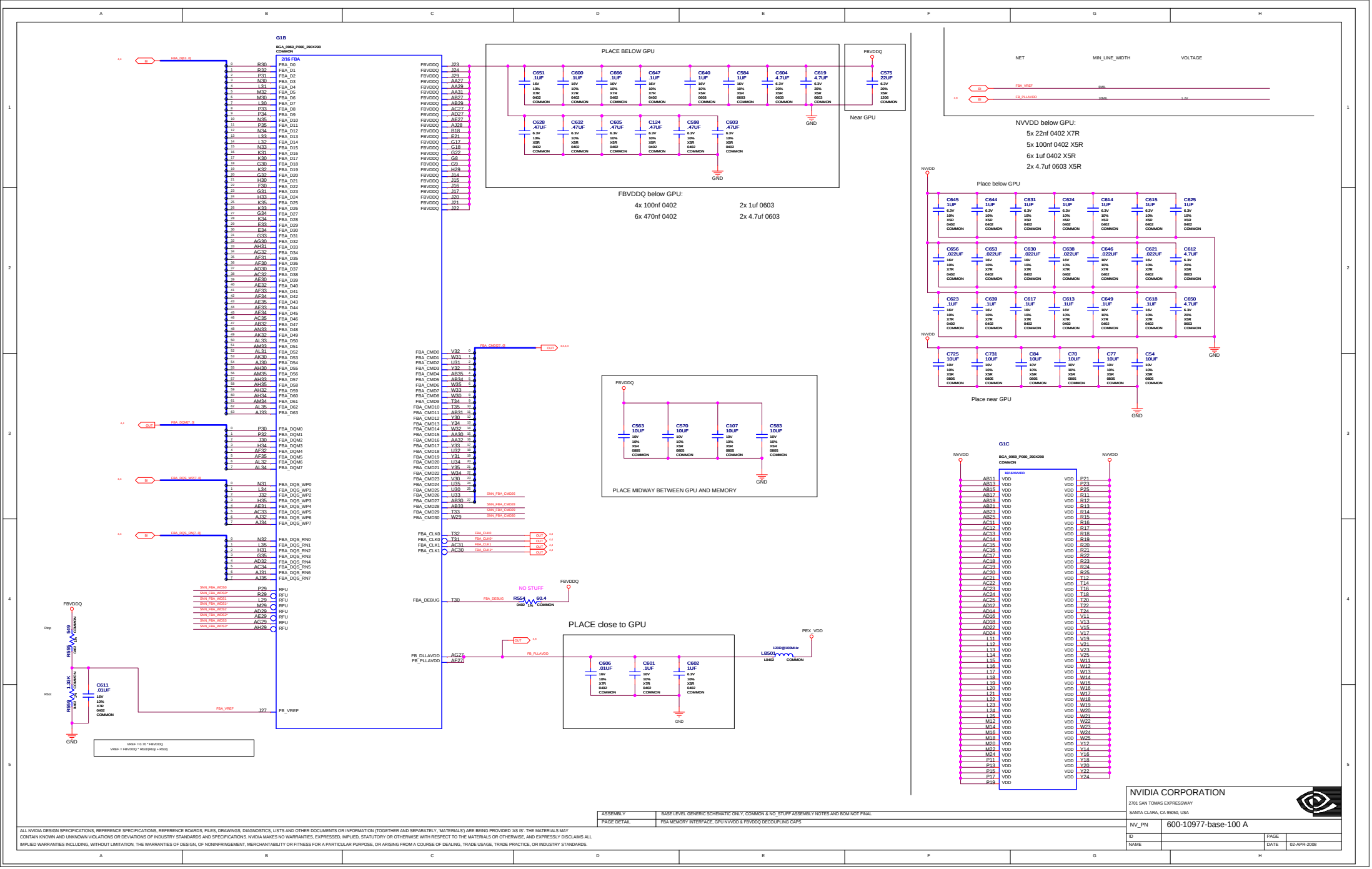
NAME		DATE	02-APR-2008



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY INTERFACE, GPU NVVDD & FBVDDQ DECOUPLING CAPS

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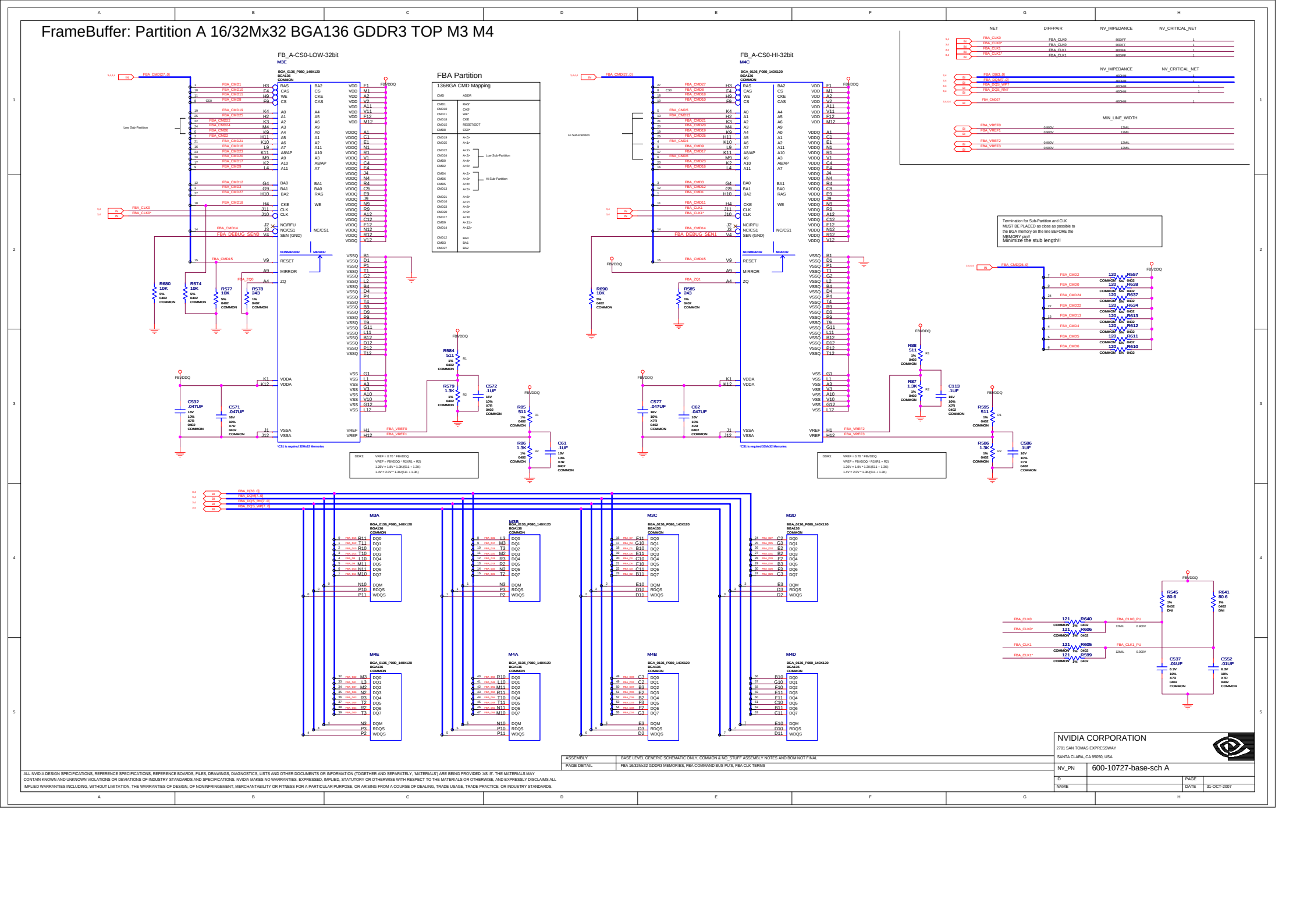
NAME		DATE	02-APR-2008

FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3 TOP M3 M4



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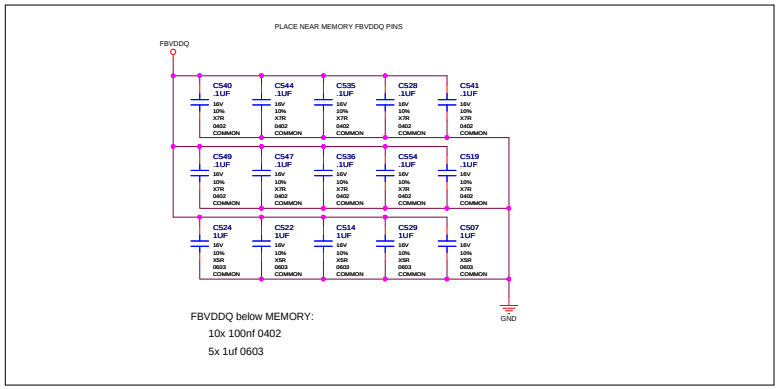
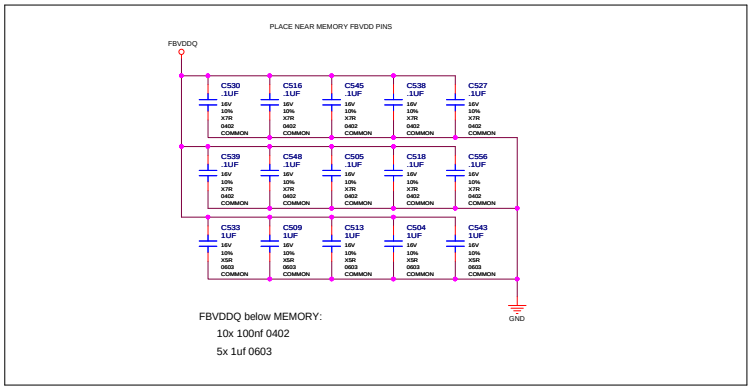
FRAME BUFFER: PARTITION A DECOUPLING

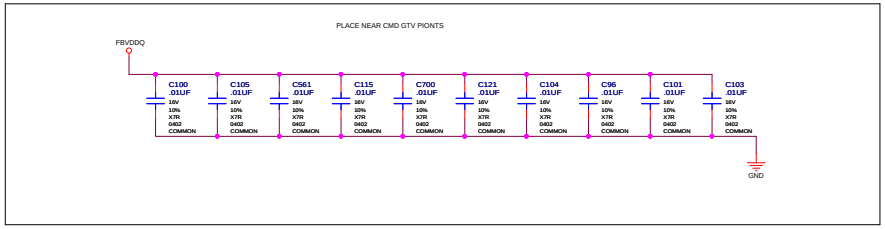
Decoupling for FBA 0..31



Decoupling for FBA 32..63



Return path coupling GND/FBVDDQ for FBA



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

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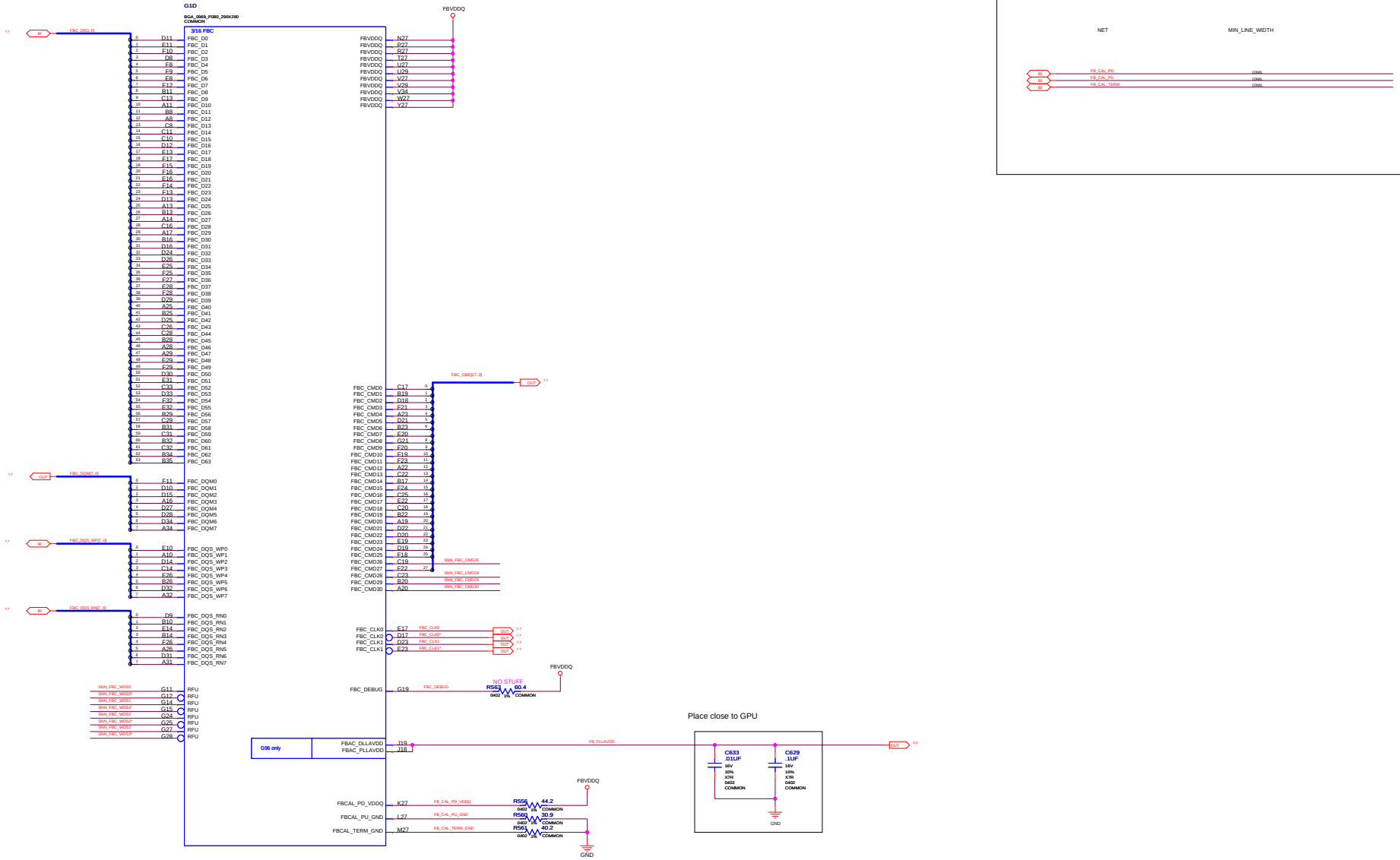
NAME		DATE	02-APR-2008



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY INTERFACE

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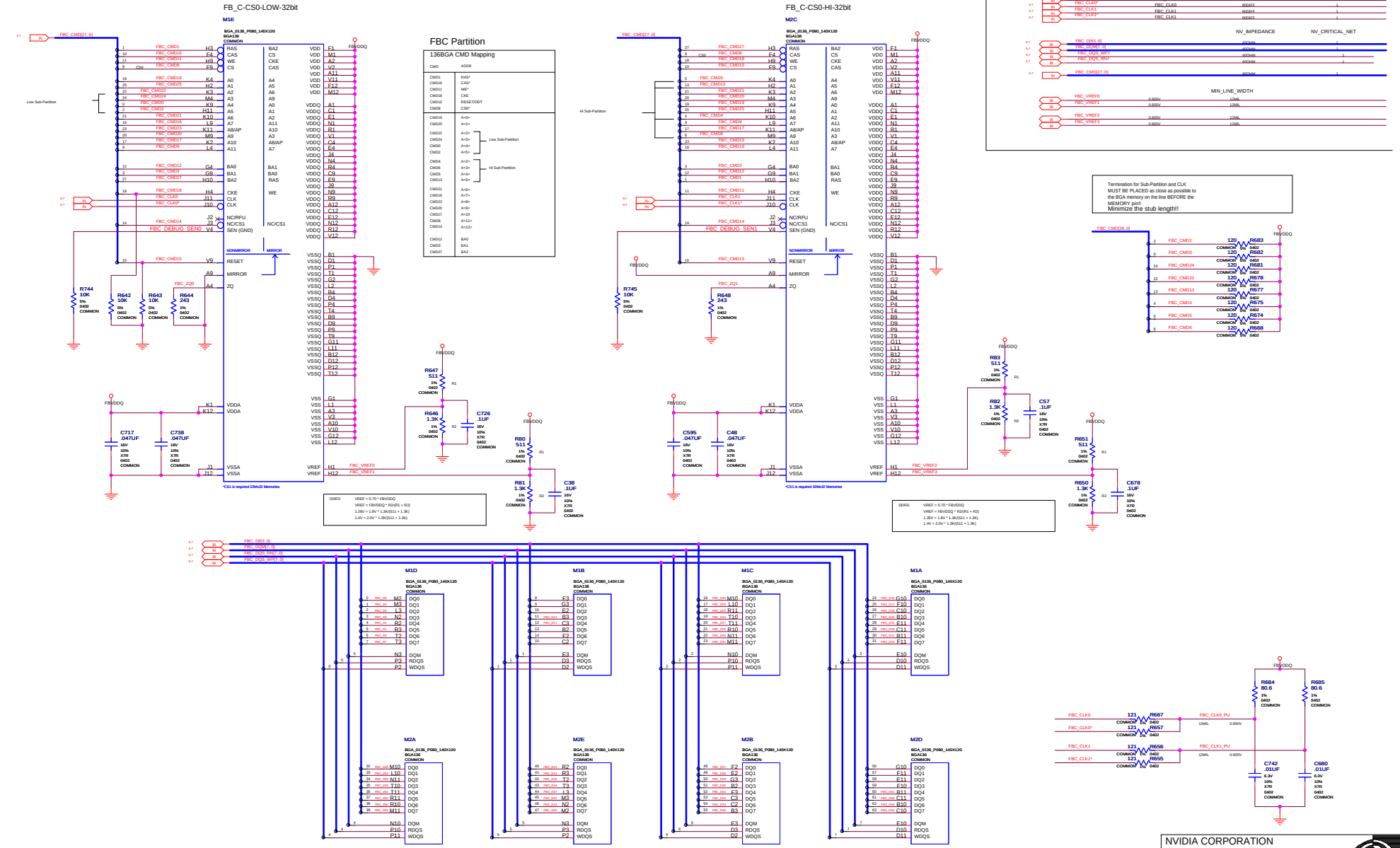
FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3 TOP M1 M2



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS PU'S, FBC CLK TERMS

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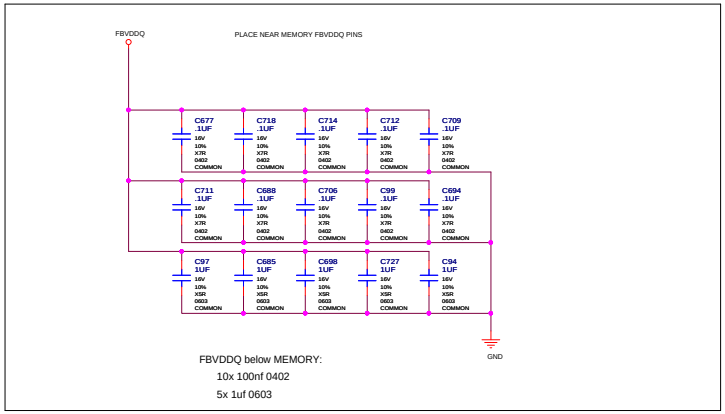
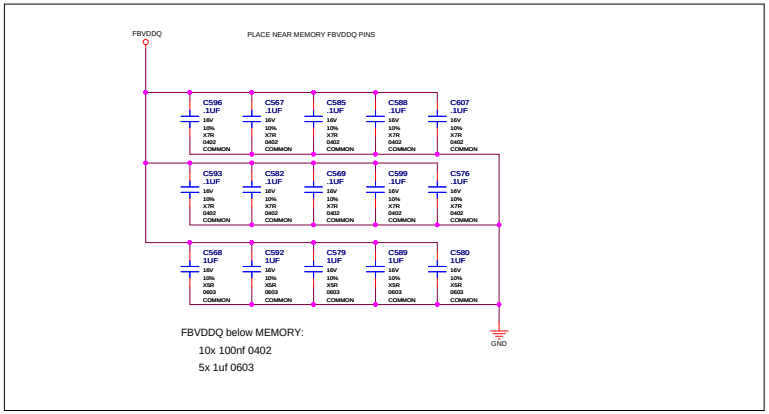
FRAMEBUFFER: PARTITION C DECOUPLING

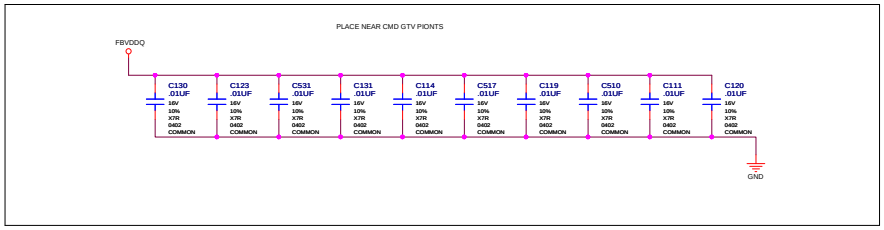
Decoupling for FBC 0..31

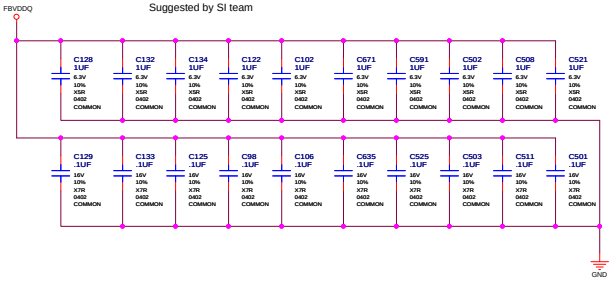


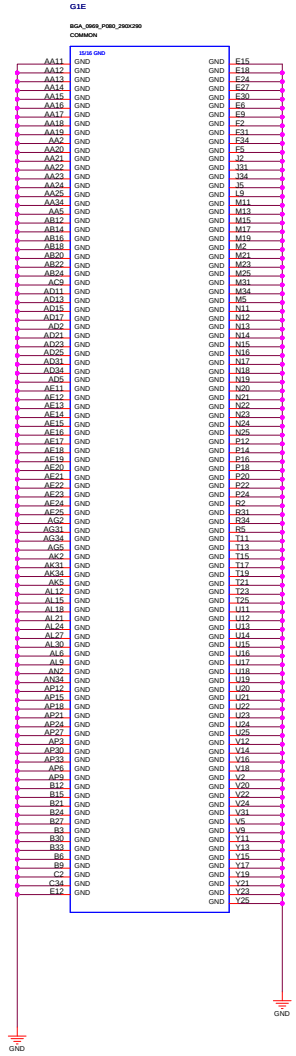
Decoupling for FBC 32..63



Return path coupling GND/FBVDDQ for FBC







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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS, GPU GND CONNECTIONS

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Primary Display (DACA), DVI-I

DACA RGB-FILTER

NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DAC_VDD			3.3V 12MIL
DACA_VREF			12MIL
DACA_RSET			12MIL
DACA_RED	1	56OHM	
DACA_GREEN	1	56OHM	
DACA_BLUE	1	56OHM	
DACA_RED_C	1	56OHM	
DACA_GREEN_C	1	56OHM	
DACA_BLUE_C	1	56OHM	
DACA_HSYNC	1	50OHM	
DACA_VSYNC	1	50OHM	
DACA_HSYNC_R	1	50OHM	
DACA_VSYNC_R	1	50OHM	
DACA_VSYNC_BUF	1	50OHM	
DACA_HSYNC_BUF	1	50OHM	
DACA_VSYNC_C	1	50OHM	
DACA_HSYNC_C	1	50OHM	
I2CA_SDA	2	50OHM	
I2CA_SCL	2	50OHM	
I2CA_SDA_R	2	50OHM	
I2CA_SCL_R	2	50OHM	
I2CA_SDA_C	2	50OHM	
I2CA_SCL_C	2	50OHM	

FOR ESD DIODES

Place near ESD diodes.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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Secondary Display (DACC), Slim DB15

DACC RGB-FILTER

NET_NAME	NV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACC_VREF			12MIL
DACC_RSET			12MIL
DACC_RED	1	50OHM	
DACC_GREEN	1	50OHM	
DACC_BLUE	1	50OHM	
DACC_RED_C	1	50OHM	
DACC_GREEN_C	1	50OHM	
DACC_BLUE_C	1	50OHM	
DACC_HSYNC	1	50OHM	
DACC_VSYNC	1	50OHM	
DACC_VSYNC_R	1	50OHM	
DACC_HSYNC_R	1	50OHM	
DACC_VSYNC_BUF	1	50OHM	
DACC_HSYNC_BUF	1	50OHM	
DACC_VSYNC_C	1	50OHM	
DACC_HSYNC_C	1	50OHM	
I2CB_SDA	2	50OHM	
I2CB_SCL	2	50OHM	
I2CB_SDA_R	2	50OHM	
I2CB_SCL_R	2	50OHM	
I2CB_SDA_C	2	50OHM	
I2CB_SCL_C	2	50OHM	

FOR ESD DIODES

5V — C13 1UF 16V 10% X5R 0603 COMMON — GND

3V3 — C785 1UF 16V 10% X5R 0603 COMMON — GND

Place near ESD diodes.

3V3 — LB12 240R@100MHz 0402 COMMON

C89 4.7UF 6.3V 10% X5R 0603 COMMON

C87 1UF 6.3V 10% X5R 0402 COMMON

C703 1UF 16V 10% X7R 0402 COMMON

C690 4700PF 25V 10% X7R 0402 COMMON

C691 1UF 16V 10% X7R 0402 COMMON

R59 124 1% 0402 COMMON

GND

DACC_VDD — AG7

DACC_VREF — AK6

DACC_RSET — AH7

G1G
BGA_0969_P080_29X29X290
COMMON
6/16 DACC

DACC_VDD
DACC_VREF
DACC_RSET

I2CB_SCL — G3
I2CB_SDA — G2

DACC_HSYNC — AM1
DACC_VSYNC — AM2

DACC_RED — AK4
DACC_GREEN — AL4
DACC_BLUE — AJ4

5V — D14 SOT23 100V 100MA COMMON

R49 33 0402 5% COMMON — I2CB_SDA_R

R5 2.2K 5% 0402 COMMON — 5V

R4 2.2K 5% 0402 COMMON

R53 33 0402 5% COMMON — I2CB_SCL_R

5V — D15 SOT23 100V 100MA COMMON

EMI filter, place close to DVI

LB1 180R@100MHz 0603 COMMON — C1 22PF 50V 5% C0G 0402 COMMON — I2CB_SDA_C — OUT

LB2 180R@100MHz 0603 COMMON — C2 22PF 50V 5% C0G 0402 COMMON — I2CB_SCL_C — OUT

5V — U505B SOIC14 COMMON

DACC_VSYNC_BUF — R654 33 0402 5% COMMON — DACC_VSYNC_R

5V — D2 SOT23 100V 100mA COMMON

EMI filter, place close to DVI

L1 27nH 0603 COMMON — C6 15PF 50V 5% C0G 0603 COMMON — DACC_VSYNC_C — OUT

5V — U505A SOIC14 COMMON

DACC_HSYNC_BUF — R671 33 0402 5% COMMON — DACC_HSYNC_R

5V — D1 SOT23 100V 100mA COMMON

L4 27nH 0603 COMMON — C9 15PF 50V 5% C0G 0603 COMMON — DACC_HSYNC_C — OUT

MIDDLE

5V_DDC

J1
N59-15R031-A43
MINIDIM15 COMMON

18	SHIELD	MEC1	16
6	GND-R	R	11
1	GND-G	G	12
2	GND_B	B	13
3	5V	HSYNC	14
8	ID2	VSYNC	15
9	GND	SCL	
4	GND		
10	GND		
5	SHIELD	MEC2	17
19			

SMN_C_MON_IDD — SDA

SMN_C_MON_IDD

GND

DACC_RED — R56 150 1% 0402 COMMON — L508 27nH 0603 COMMON — DACC_RED_C

3V3 — D511 100MA 100V SOT23 COMMON — R676 150 1% 0402 COMMON — C779 22PF 50V 5% C0G 0402 COMMON — C778 22PF 50V 5% C0G 0402 COMMON

DACC_GREEN — R57 150 1% 0402 COMMON — L509 27nH 0603 COMMON — DACC_GREEN_C

3V3 — D510 100MA 100V SOT23 COMMON — R679 150 1% 0402 COMMON — C790 22PF 50V 5% C0G 0402 COMMON — C791 22PF 50V 5% C0G 0402 COMMON

DACC_BLUE — R55 150 1% 0402 COMMON — L501 27nH 0603 COMMON — DACC_BLUE_C

3V3 — D509 100MA 100V SOT23 COMMON — R659 150 1% 0402 COMMON — C756 22PF 50V 5% C0G 0402 COMMON — C755 22PF 50V 5% C0G 0402 COMMON

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID

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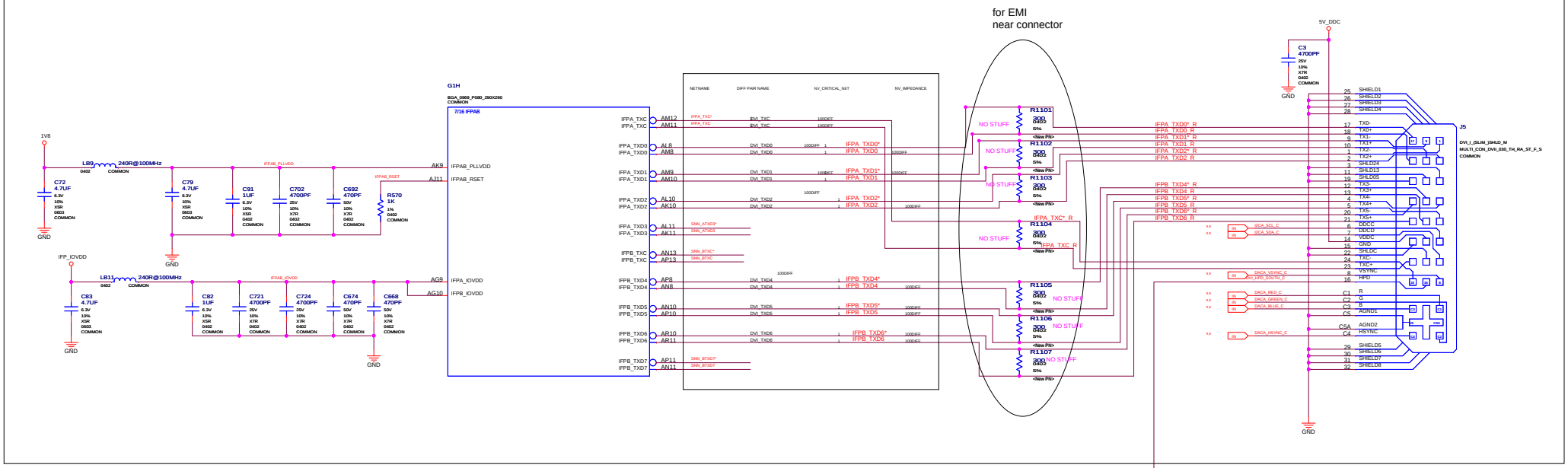
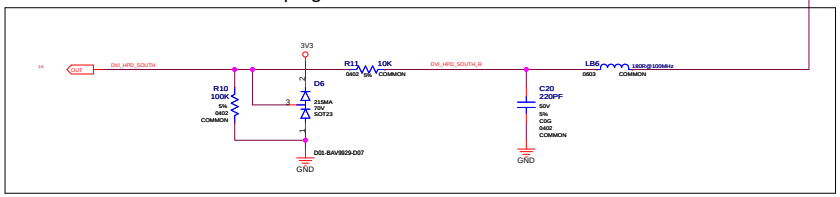
TMDS LINK: A & B



Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
IFPAB_PLLVDD	12MIL	1.8V
IFPAB_IOVDD	12MIL	3.3V
IFPABRSET	12MIL	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK A/B, DVI CONNECTOR SOUTH

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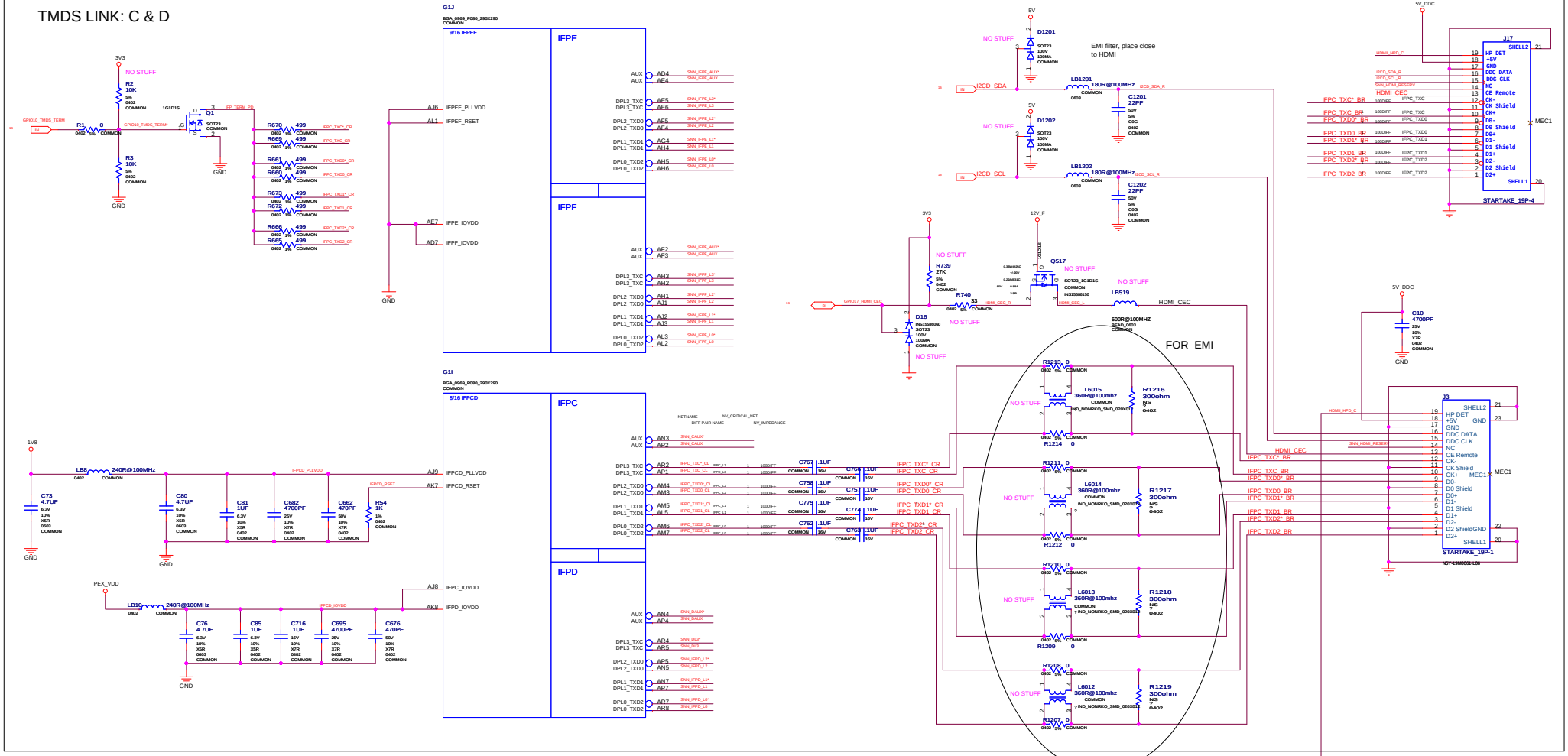
TMDS LINK: C & D



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK C/D, AC COUPLING, PD's, DVI CONNECTOR MID

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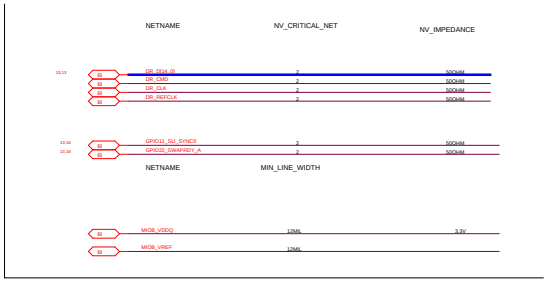
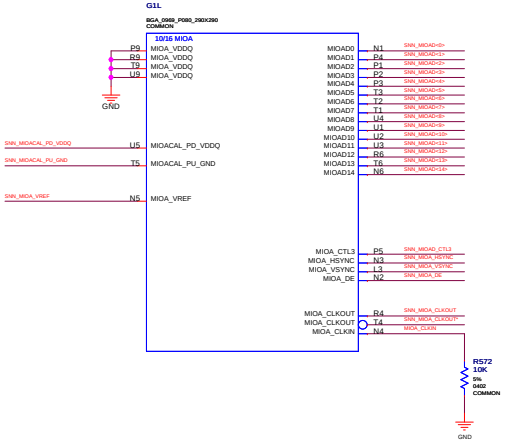
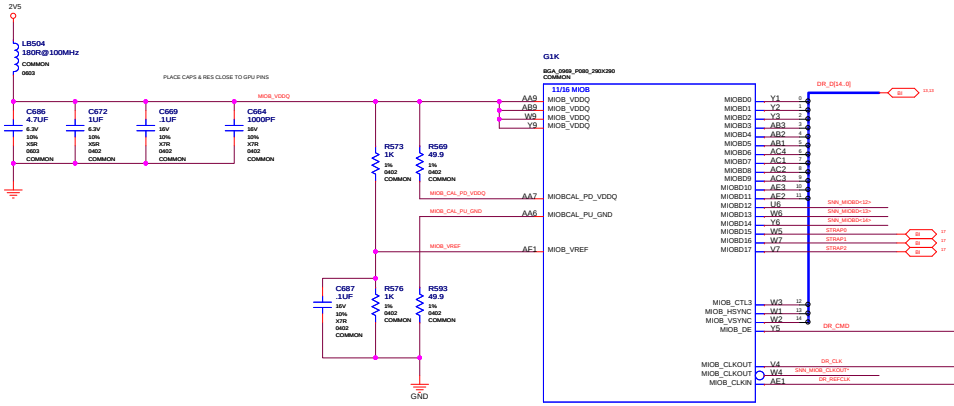
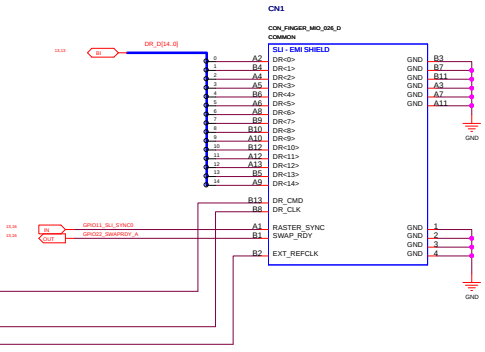
MIOA/B SLI







SLI Connector



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PAGE DETAIL	MIOA & MIOB, SLI CONNECTOR

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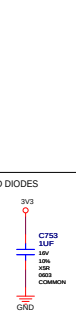
DACB: SD/HD VIDEO OUT CONNECTOR

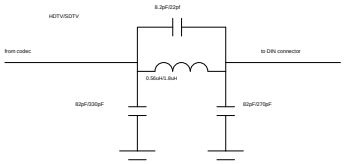
NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
OUT DACB_C_OUT		50OHM	1
OUT DACB_CVBS_OUT		50OHM	1
OUT DACB_PB_OUT		50OHM	1
BI TV_PBOUT_C		50OHM	1
BI TV_COUT_C		50OHM	1
BI TV_YOUT_C		50OHM	1
IN DACB_VREF	12MIL		
IN DACB_RSET	12MIL		

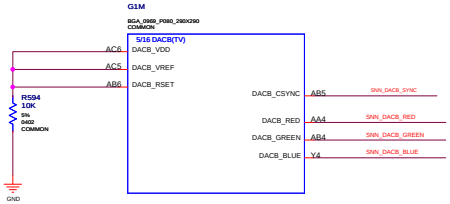
FOR ESD DIODES



Place near ESD diodes.

FILTER CIRCUIT





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, MINIDIN CONNECTOR NORTH, SD/HD VIDEO OUTPUT CONNECTOR

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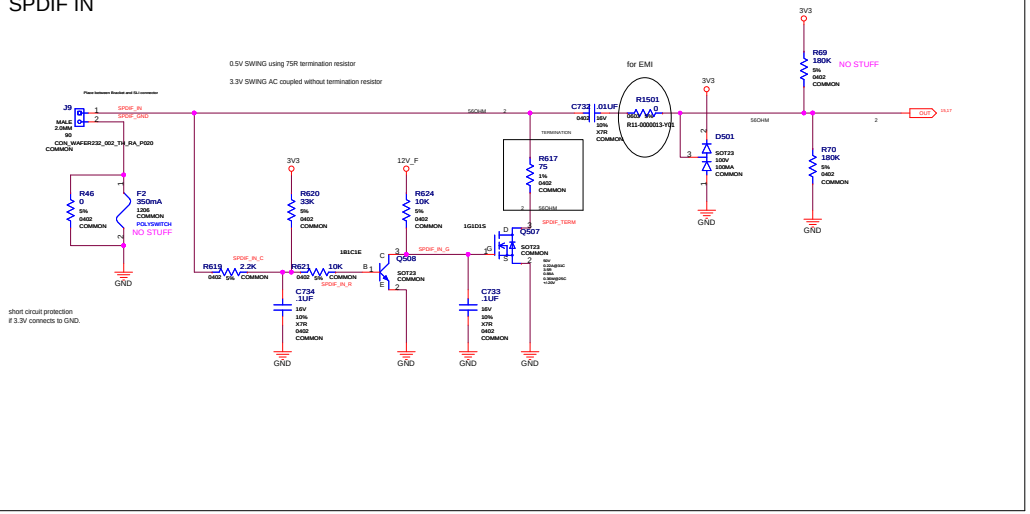
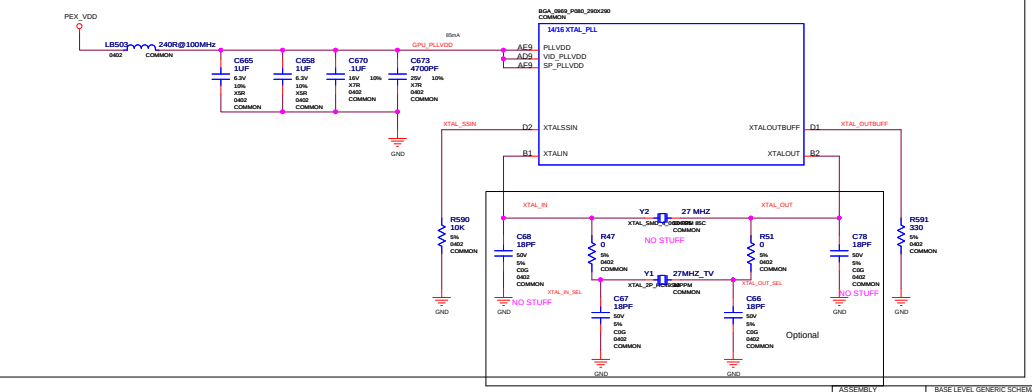
XTAL/PLLVDD/SPDIF IN

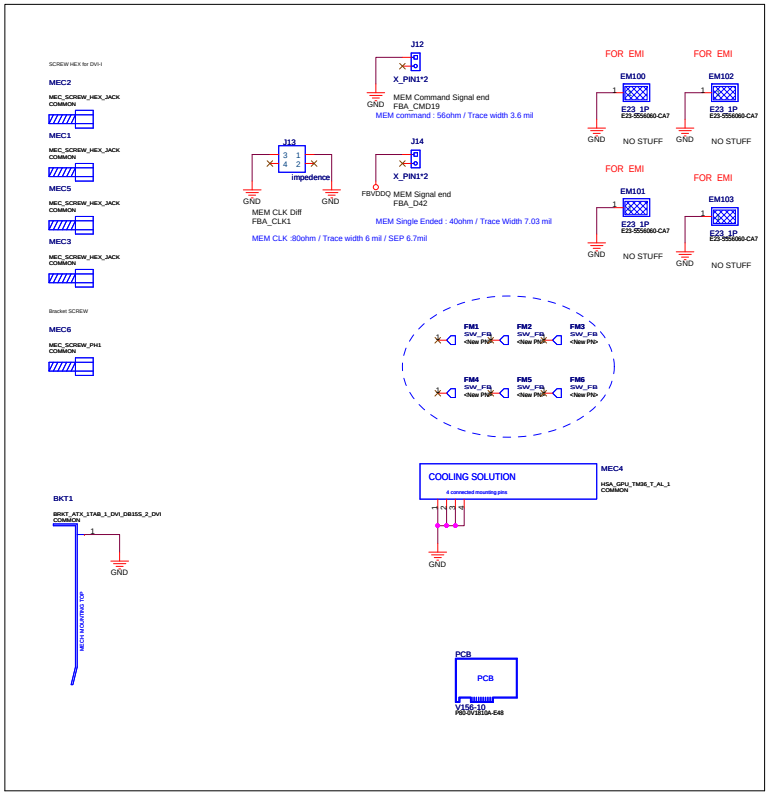
SPDIF IN

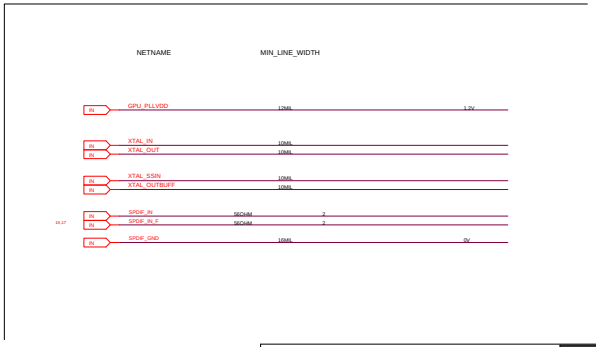


XTAL/GPU_PLLVDD



MECHANICALS & THERMALS





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF-IN, XTAL, MECHANICALS, THERMALS

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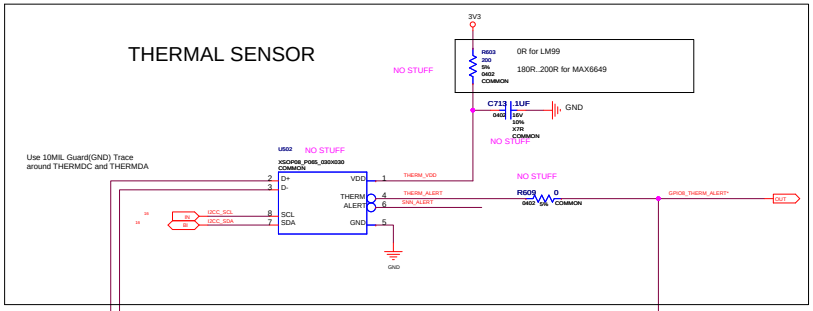
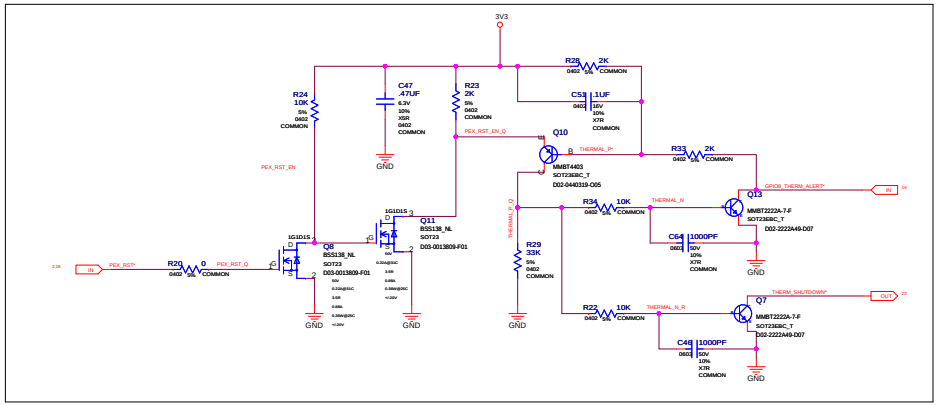
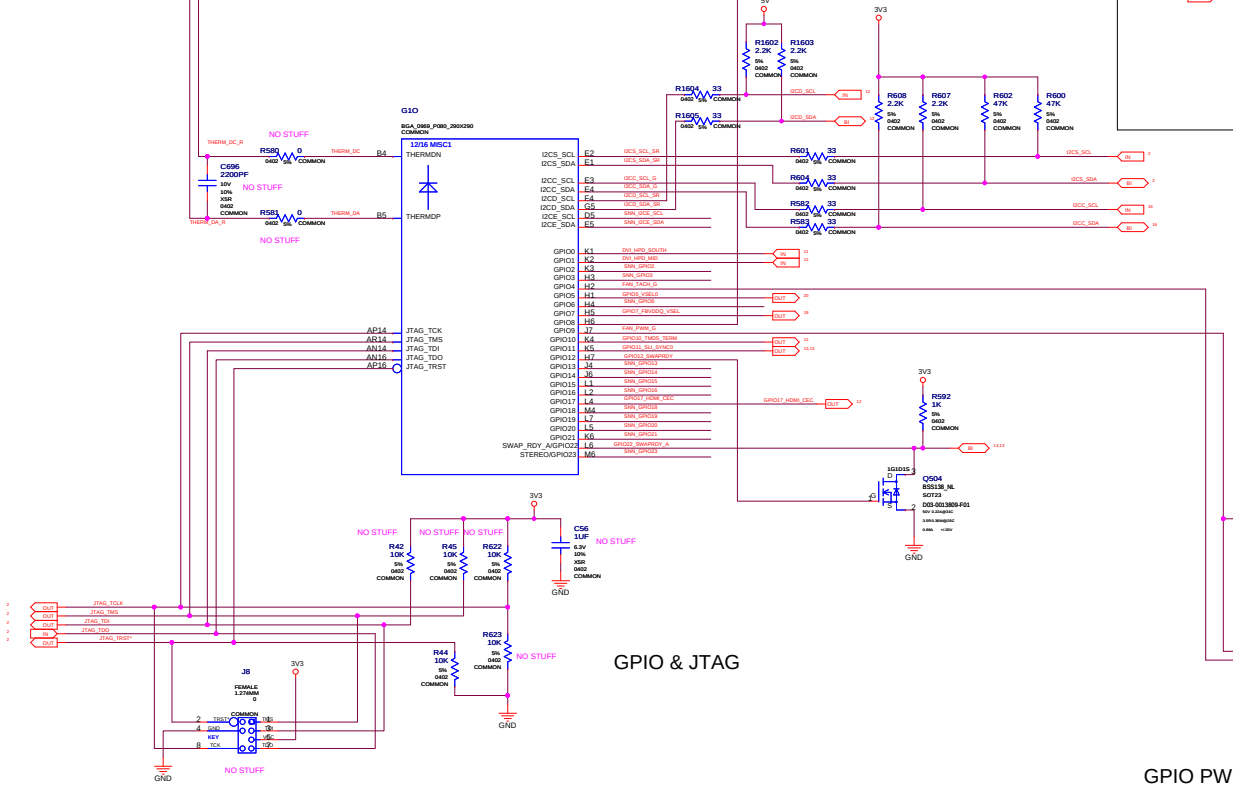
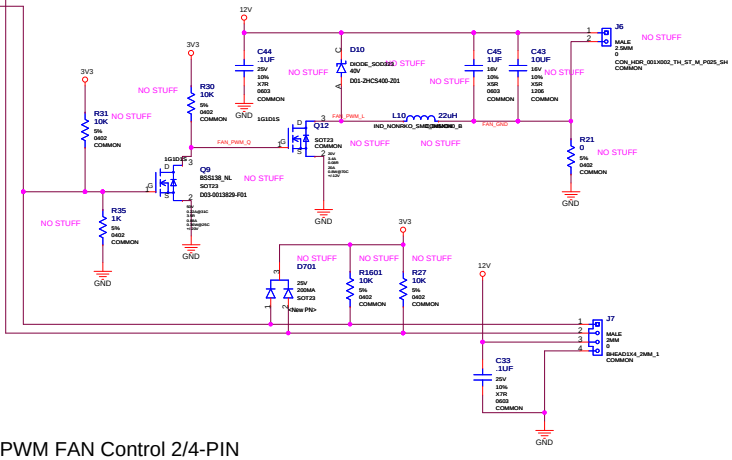
EXTERNAL THERMAL SENSOR, 4PIN FAN CONTROL, GPIO, THERMAL PROTECTION



Thermal Protection







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	EXTERNAL THERMAL SENSOR, 2/4PIN FAN CONTROL, GPIO,THERMAL PROTECTION

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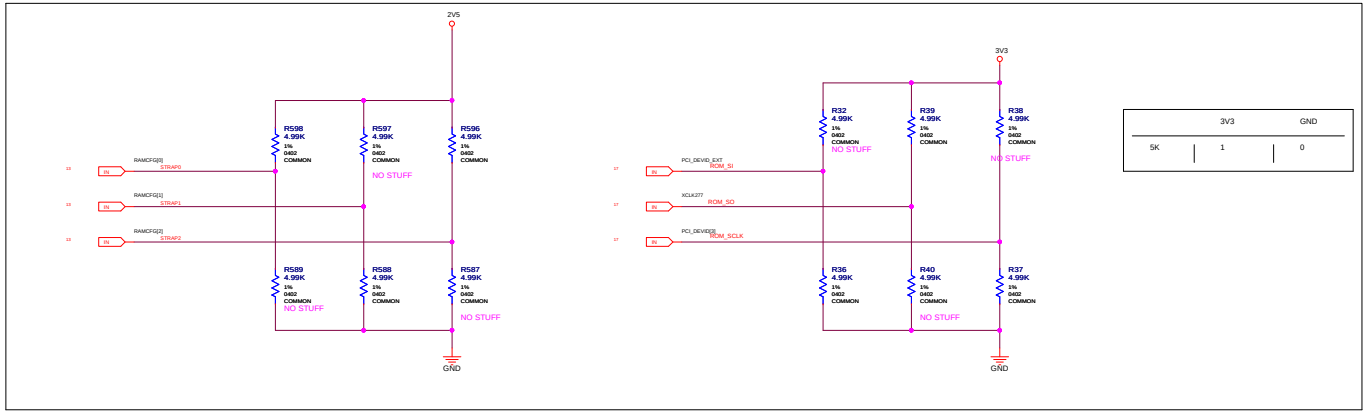
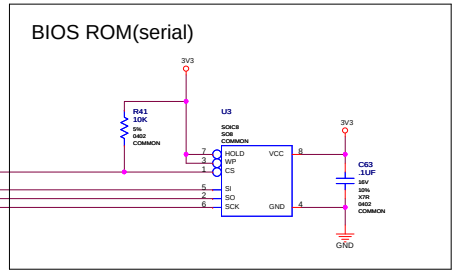
STRAPPING OPTIONS

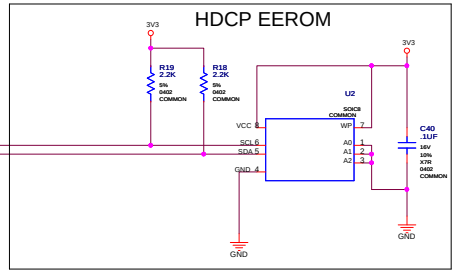
Assembly: BIOS

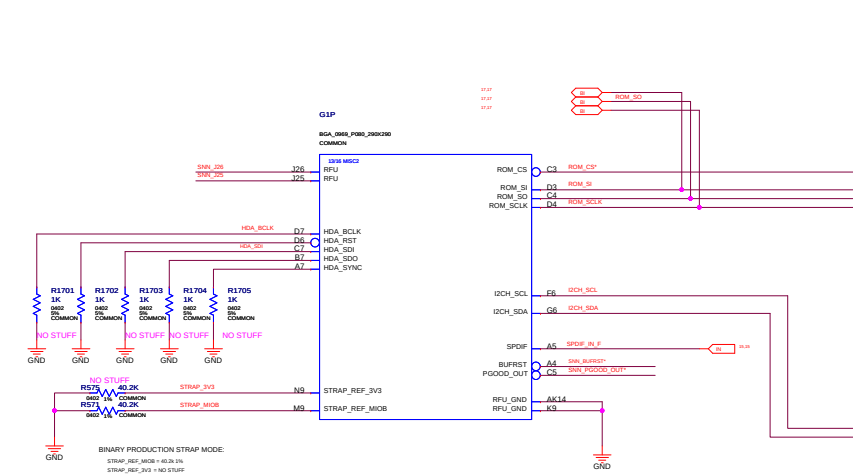


BIOS ROM(serial)



HDCP EEROM





NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
HDA_BCLK		50OHM	2
HDA_RST*		50OHM	2
HDA_SDI		50OHM	2
HDA_SDO		50OHM	2
HDA_SYNC		50OHM	2
HDA_SDI_R		50OHM	2

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

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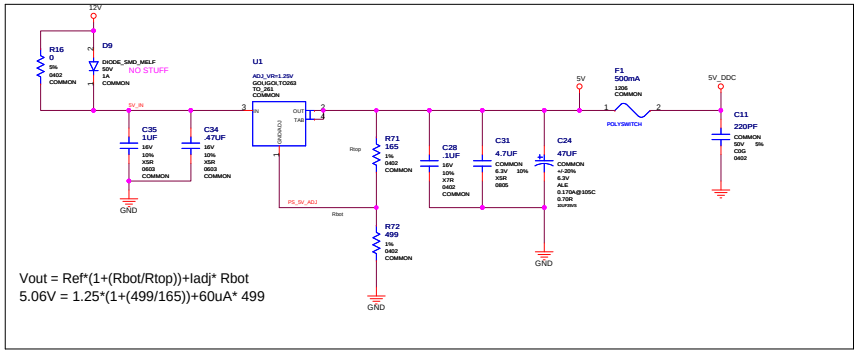
Power Supply: 5V, 5V_DDC, IFP_PLLVDD, MIOA_VDD,

TMDS BACKDRIVE

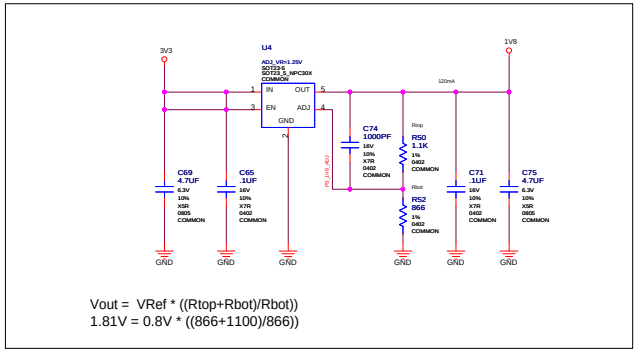
5V REGULATOR

5V DDC

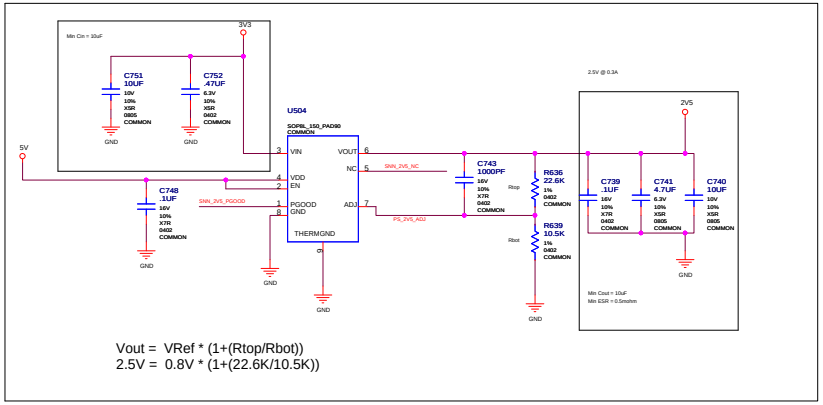


NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
5V_DDC	5V_DDC	0.1A	12Mil	5V
5V	5V	0.15A	12Mil	5V
1V8	1V8	0.12A	12Mil	1.8V
2V5	2V5	0.3A	12Mil	2.5V
GND	GND		16Mil	0
12V_F	12V_F	6A	20Mil	12V

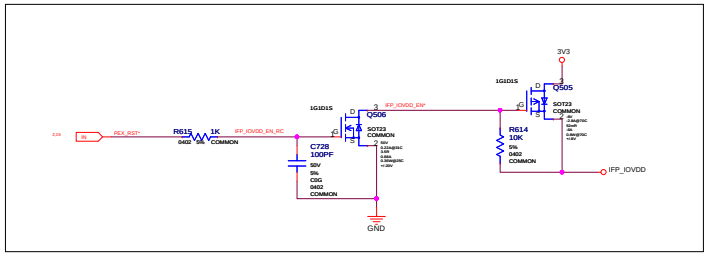
IFP PLL Supply 1.8V



MIO_VDD 2.5V



TMDS BACKDRIVE



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	5V,DDC5V,IFP PLLVDD,MIO_VDD,TMDS_BACKDRIVE

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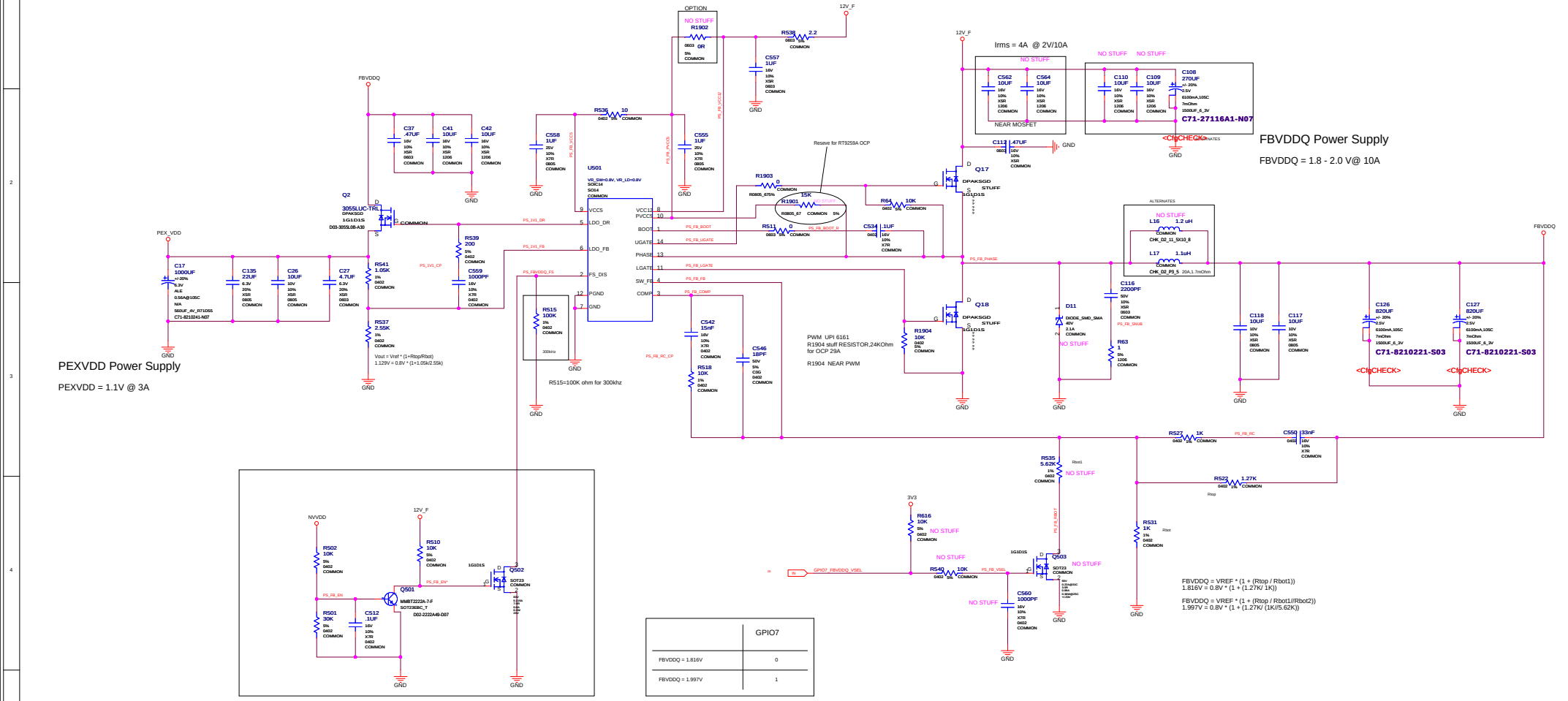
POWER SUPPLY: FBVDD/Q,PEX_VDD

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
FBVDDQ	10A	20MIL	1.8V
PEX_VDD	3A	16MIL	1.1V



PEXVDD Power Supply

PEXVDD = 1.1V @ 3A

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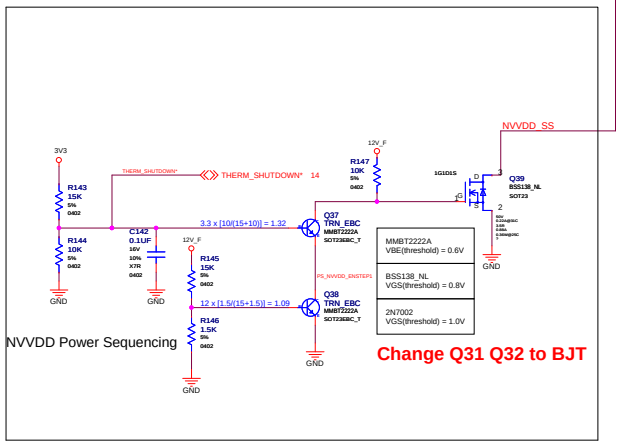
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: FBVDDQ , PEX_VDD

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10977-base-100 A		
ID		PAGE	
NAME		DATE	02-APR-2008

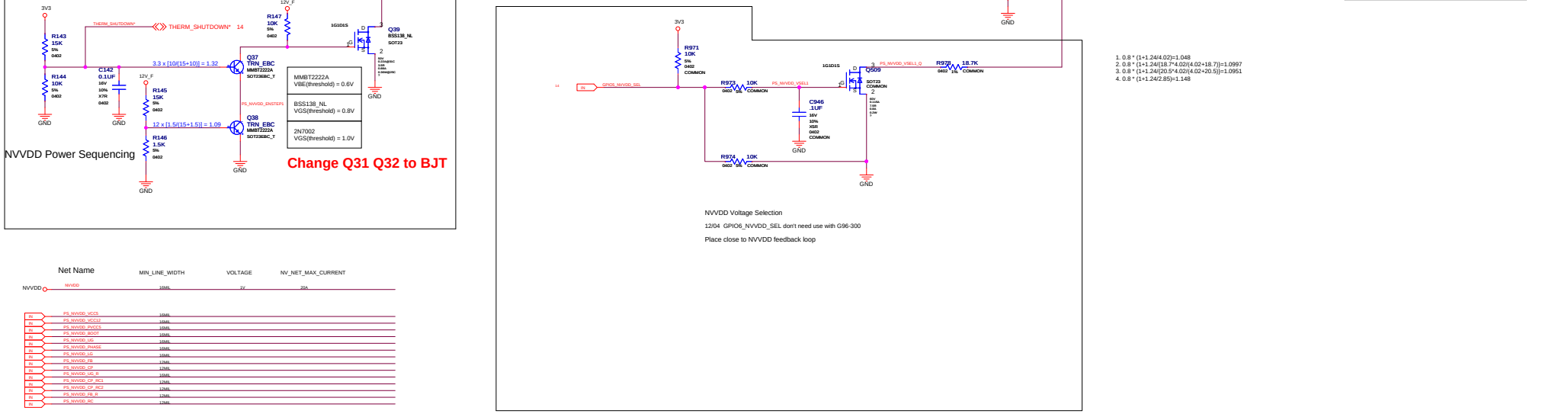
Power Supply : NVVDD



NVVDD Power Sequencing

Change Q31 Q32 to BJT

Net Name	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
NVVDD	16MIL	1V	20A
PS_NVVDD_VCCS	16MIL		
PS_NVVDD_VCC12	16MIL		
PS_NVVDD_PVCCS	16MIL		
PS_NVVDD_BOOT	16MIL		
PS_NVVDD_UG	16MIL		
PS_NVVDD_PHASE	16MIL		
PS_NVVDD_LG	16MIL		
PS_NVVDD_FB	12MIL		
PS_NVVDD_CP	12MIL		
PS_NVVDD_UG_R	16MIL		
PS_NVVDD_CP_RC1	12MIL		
PS_NVVDD_CP_RC2	12MIL		
PS_NVVDD_FB_R	12MIL		
PS_NVVDD_RC	12MIL		



NVVDD Voltage Selection

12/04 GPIO6_NVVDD_SEL don't need use with G96-300

Place close to NVVDD feedback loop

1. 0.8 * (1+1.24/4.02)=1.048
2. 0.8 * (1+1.24/(18.7*4.02/(4.02+18.7))=1.0997
3. 0.8 * (1+1.24/(20.5*4.02/(4.02+20.5))=1.0951
4. 0.8 * (1+1.24/2.85)=1.148

Title: Basenet Report
Design: p977_a00
Date: Jan 16 15:30:01 2008

Base nets and synonyms for
p977_lib.P977_A00(@p977_lib.p977_a00(sch
_1))
Base Signal Location([Zone][dir])

1V8 18.1G
2V5 18.1G
3V3 2.5G
5V 18.1G
5V_DDC 18.1G
5V_IN 18.2A
12V 2.5G
12V_F 18.1G
DACA_BLUE 9.1A<> 9.5E
DACA_BLUE_C 9.1A<> 9.5G> 11.3G<
DACA_GREEN 9.1A<> 9.4E
DACA_GREEN_C 9.1A<> 9.4G> 11.3G<
DACA_HSYNC 9.1A<> 9.3C
DACA_HSYNC_BUF 9.1A<> 9.3D
DACA_HSYNC_C 3.1F<> 5.5B
DACA_HSYNC_R 9.1A<> 9.3E
DACA_RED 9.1A<> 9.4E
DACA_RED_C 9.1A<> 9.4G> 11.3G<
DACA_RSET 9.1A< 9.3B
DACA_VDD 9.3B
DACA_VREF 9.1A< 9.3B
DACA_VSYNC 9.1A<> 9.3C
DACA_VSYNC_BUF 9.1A<> 9.3D
DACA_VSYNC_C 9.1A<> 9.3G> 11.3G<
DACA_VSYNC_R 9.1A<> 9.3E
DACB_CVBS_OUT 14.1A> 14.3F 14.4C
DACB_C_OUT 14.1A> 14.4C 14.4F
DACB_PB_OUT 14.1A> 14.4C 14.4F
DACB_RSET 14.1A< 14.3B
DACB_VDD 14.3B
DACB_VREF 14.1A< 14.3B
DACC_BLUE 10.1A<> 10.4C 10.5D
DACC_BLUE_C 10.1A<> 10.5G> 12.4G<
DACC_GREEN 10.1A<> 10.4C 10.4D
DACC_GREEN_C 10.1A<> 10.4G> 12.4G<
DACC_HSYNC 10.1A<> 10.4C
DACC_HSYNC_BUF 10.1A<> 10.3D
DACC_HSYNC_C 10.2A<> 10.3H> 12.4G<
DACC_HSYNC_R 10.1A<> 10.3E
DACC_RED 10.1A<> 10.4C 10.4D
DACC_RED_C 10.1A<> 10.4G> 12.4G<
DACC_RSET 10.1A< 10.4B
DACC_VDD 10.3B
DACC_VREF 10.1A< 10.4B
DACC_VSYNC 10.1A<> 10.4C
DACC_VSYNC_BUF 10.1A<> 10.3D
DACC_VSYNC_C 10.2A<> 10.3H> 12.4G<
DACC_VSYNC_R 10.1A<> 10.3E
DAC_VDD 9.1A<
DR_CLK 13.1G<> 13.5D
DR_CMD 13.1G<> 13.5D
DR_D<14..0> 13.1G<> 13.4D<>
13.4F<>
DR_REFCLK 13.1G<> 13.5D
DVI_HPD_MID 12.5C> 16.3D<
DVI_HPD_MID_C 12.4G
DVI_HPD_MID_R 12.5E
DVI_HPD_SOUTH 11.5C> 16.3D<
DVI_HPD_SOUTH_C 11.3G
DVI_HPD_SOUTH_R 11.5E
FAN_GND 16.4G
FAN_PWM_G 16.3C
FAN_PWM_L 16.4F
FAN_PWM_Q 16.4F
FAN_TACH_G 16.3C
FBA_CLK0 3.4D> 4.1G< 4.2A<
4.4G
FBA_CLK0* 3.4D> 4.1G< 4.2A<
4.4G
FBA_CLK0_PU 4.4H
FBA_CLK1 3.4D> 4.1G< 4.2D<
4.5G
FBA_CLK1* 3.4D> 4.1G< 4.2D<
4.5G
FBA_CLK1_PU 4.5H
FBA_CMD<0> 4.1B 4.2G
FBA_CMD<27..0> 3.2D> 4.1A< 4.1D<
4.1G> 4.2G<
FBA_CMD<1> 4.1B 4.2E
FBA_CMD<2> 4.1B 4.2G
FBA_CMD<3> 4.2B 4.2E
FBA_CMD<4> 4.1E 4.2G
FBA_CMD<5> 4.1E 4.3G
FBA_CMD<6> 4.1E 4.3G
FBA_CMD<8> 4.1B 4.1E
FBA_CMD<9> 4.1B 4.1E
FBA_CMD<10> 4.1B 4.1E

FBA_CMD<11> 4.1B 4.2E
FBA_CMD<12> 4.2B 4.2E
FBA_CMD<13> 4.1E 4.2G
FBA_CMD<14> 4.2B 4.2E
FBA_CMD<15> 4.2B 4.2E
FBA_CMD<16> 4.1B 4.1E
FBA_CMD<17> 4.1B 4.1E
FBA_CMD<18> 4.1E 4.2B
FBA_CMD<19> 4.1B 4.1E
FBA_CMD<20> 4.1B 4.1E
FBA_CMD<21> 4.1B 4.1E
FBA_CMD<22> 4.1B 4.2G
FBA_CMD<23> 4.1B 4.1E
FBA_CMD<24> 4.1B 4.2G
FBA_CMD<25> 4.1B 4.1E
FBA_CMD<27> 4.1E 4.2B
FBA_D<63..0> 3.1A<> 4.1G<> 4.4B<>
FBA_DEBUG 3.4C
FBA_DEBUG_SEN0 4.2B
FBA_DEBUG_SEN1 4.2E
FBA_DQM<7..0> 3.3A> 4.1G<> 4.4B<>
FBA_DQS_RN<7..0> 3.4A<> 4.1G<> 4.4B<>
FBA_DQS_WP<7..0> 3.3A<> 4.1G<> 4.4B<>
FBA_VREF 3.1F<> 3.5B
FBA_VREF0 4.1G<> 4.3C
FBA_VREF1 4.1G<> 4.3C
FBA_VREF2 4.1G<> 4.3F
FBA_VREF3 4.1G<> 4.3F
FBA_ZQ0 4.2B
FBA_ZQ1 4.2E
FBC_CLK0 6.4D> 7.1G< 7.2A<
7.4G
FBC_CLK0* 6.4D> 7.1G< 7.2A<
7.5G
FBC_CLK0_PU 7.4G
FBC_CLK1 6.4D> 7.1G< 7.2D<
7.5G
FBC_CLK1* 6.4D> 7.1G< 7.2D<
7.5G
FBC_CLK1_PU 7.5G
FBC_CMD<0> 7.1B 7.2G
FBC_CMD<27..0> 6.3D> 7.1A< 7.1D
7.1G< 7.2G<
FBC_CMD<1> 7.2B 7.2E
FBC_CMD<2> 7.1B 7.2G
FBC_CMD<3> 7.2B 7.2E
FBC_CMD<4> 7.1E 7.2G
FBC_CMD<5> 7.1E 7.2G
FBC_CMD<6> 7.1E 7.2G
FBC_CMD<8> 7.1B 7.1E
FBC_CMD<11> 7.1B 7.2E
FBC_CMD<12> 7.2B 7.2E
FBC_CMD<13> 7.1E 7.2G
FBC_CMD<14> 7.2B 7.2E
FBC_CMD<15> 7.2B 7.2E
FBC_CMD<16> 7.1B 7.1E
FBC_CMD<17> 7.1B 7.1E
FBC_CMD<18> 7.1E 7.2B
FBC_CMD<19> 7.1B 7.1E
FBC_CMD<20> 7.1B 7.1E
FBC_CMD<21> 7.1B 7.1E
FBC_CMD<22> 7.1B 7.2G
FBC_CMD<23> 7.1B 7.1E
FBC_CMD<24> 7.1B 7.2G
FBC_CMD<25> 7.1B 7.1E
FBC_CMD<27> 7.1E 7.2B
FBC_D<63..0> 6.1A<> 7.1G<> 7.4B<>
FBC_DEBUG 6.4C
FBC_DEBUG_SEN0 7.2B
FBC_DEBUG_SEN1 7.2E
FBC_DQM<7..0> 6.3A> 7.1G<> 7.4B<>
FBC_DQS_RN<7..0> 6.4A<> 7.1G<> 7.4B<>
FBC_DQS_WP<7..0> 6.3A<> 7.1G<> 7.4B<>
FBC_VREF0 7.1G<> 7.3C
FBC_VREF1 7.1G<> 7.3C
FBC_VREF2 7.1G<> 7.3F
FBC_VREF3 7.1G<> 7.3F
FBC_ZQ0 7.2B
FBC_ZQ1 7.2E
FBVDDQ 19.1G
FB_CAL_PD 6.1F<>
FB_CAL_PD_VDDQ 6.5C
FB_CAL_PU 6.1F<>
FB_CAL_PU_GND 6.5C
FB_CAL_TERM 6.1F<>
FB_CAL_TERM_GND 6.5C
FB_PLLAVDD 3.1F<> 3.4D> 6.4F>
GPIO5_VSEL0 16.3D> 20.4D<
GPIO7_FBVDDQ_VSEL 16.3D> 19.4D<
GPIO8_THERM_ALERT* 16.2D> 16.2H<
GPIO10_TMDS_TERM 12.1D< 16.3D>
GPIO10_TMDS_TERM* 12.1E
GPIO11_SLI_SYNC0 13.1G<> 13.4F< 16.3D>
GPIO12_SWAPRDY 16.3C

GPIO22_SWAPRDY_A 13.1G<> 13.4F>
16.4D<>
GPU_PLLVDD 15.4B 15.4G<
GPU_TESTMODE 2.5E
HDA_BCLK 17.4B 17.5A<
HDA_RST* 17.4B 17.5A<
HDA_SDI 17.4B 17.5A>
HDA_SDI_R 17.4A 17.5A>
HDA_SDO 17.4B 17.5A<
HDA_SYNC 17.4B 17.5A<
I2CA_SCL 9.1A<> 9.3C
I2CA_SCL_C 9.2A<> 9.2G> 11.3G<
I2CA_SCL_R 9.2A<> 9.2F
I2CA_SDA 9.1A<> 9.3C
I2CA_SDA_C 9.2A<> 9.2G> 11.3G<
I2CA_SDA_R 9.2A<> 9.2F
I2CB_SCL 10.2A<> 10.3C
I2CB_SCL_C 10.2A<> 10.2H> 12.3G<
I2CB_SCL_R 10.2A<> 10.2D
I2CB_SDA 10.2A<> 10.3C
I2CB_SDA_C 10.1H> 10.2A<> 12.3G<
I2CB_SDA_R 10.2A<> 10.2D
I2CC_SCL 16.2B< 16.3E<
I2CC_SCL_G 16.3C
I2CC_SDA 16.2B<> 16.3E<>
I2CC_SDA_G 16.3C
I2CH_SCL 17.4C
I2CH_SDA 17.4C
I2CS_SCL 2.1C< 16.3E<
I2CS_SCL_SR 16.3C
I2CS_SDA 2.1C<> 16.3E<>
I2CS_SDA_SR 16.3C
IFPABRSET 11.5G<>
IFPAB_IOVDD 11.3B 11.5G<>
IFPAB_PLLVDD 11.2B 11.5G<>
IFPAB_RSET 11.2B
IFPA_TXC 11.2D
IFPA_TXC* 11.2D
IFPA_TXD0 11.2D
IFPA_TXD0* 11.2D
IFPA_TXD1 11.2D
IFPA_TXD1* 11.2D
IFPA_TXD2 11.3D
IFPA_TXD2* 11.2D
IFPB_TXD4 11.3D
IFPB_TXD4* 11.3D
IFPB_TXD5 11.3D
IFPB_TXD5* 11.3D
IFPB_TXD6 11.3D
IFPB_TXD6* 11.3D
IFPCD_IOVDD 12.4B 12.5G<>
IFPCD_PLLVDD 12.3B 12.5G<>
IFPCD_RSET 12.3B
IFPC_L0 12.3D
IFPC_L0* 12.3D
IFPC_L1 12.3D
IFPC_L1* 12.3D
IFPC_L3 12.3D
IFPC_L2* 12.3D
IFPC_L3 12.3D
IFPC_L3* 12.3D
IFPC_TXC 12.1F 12.3E
IFPC_TXC* 12.1F 12.3E
IFPC_TXD0 12.1F 12.3E
IFPC_TXD0* 12.1F 12.3E
IFPC_TXD1 12.2F 12.3E
IFPC_TXD1* 12.1F 12.3E
IFPC_TXD2 12.2F 12.3E
IFPC_TXD2* 12.2F 12.3E
IFPC_TXD3 12.2F 12.4E
IFPC_TXD3* 12.2F 12.4E
IFPC_TXD4 12.2F 12.4E
IFPC_TXD4* 12.2F 12.4E
IFPC_TXD5 12.2F 12.4E
IFPC_TXD5* 12.2F 12.4E
IFPD_L0 12.4D
IFPD_L0* 12.4D
IFPD_L1 12.4D
IFPD_L1* 12.4D
IFPD_L2 12.4D
IFPD_L2* 12.4D
IFP_IOVDD_EN* 18.5B
IFP_IOVDD_EN_RC 18.5B
IFP_TERM_PD 12.1F 12.5G<>
JTAG_TCLK 2.1C< 16.4A>
JTAG_TDI 2.1C< 16.4A>
JTAG_TDO 2.1C> 16.5A<
JTAG_TMS 2.1C< 16.4A>
JTAG_TRST* 2.1C< 16.5A>
MIOA_CLKIN 13.2D
MIOB_CAL_PD_VDDQ 13.4C
MIOB_CAL_PU_GND 13.4C
MIOB_VDDQ 13.1G<> 13.4B
MIOB_VREF 13.2G<> 13.4C
NVVDD 20.1A
NVVDD_GND_SENSE 2.5G<>

NVVDD_RBOT1 20.4E
NVVDD_SENSE 2.4F> 2.5G<> 20.4H<
NVVDD_VSEL0 20.4E
PEX_PLLVDD 2.4E 2.5G<>
PEX_PLL_CLK_OUT 2.2C
PEX_PLL_CLK_OUT* 2.2C
PEX_PRSNT 2.1A 2.4A
PEX_REFCLK 2.1G<> 2.2B
PEX_REFCLK* 2.1G<> 2.2B
PEX_RST* 2.2C> 2.2C> 16.2E<
18.5A<
PEX_RST_EN 16.2F
PEX_RST_EN_Q 16.2G
PEX_RST_Q 16.2F
PEX_RX0 2.2B 2.4G<>
PEX_RX0* 2.2B 2.4G<>
PEX_RX1 2.2B 2.4G<>
PEX_RX1* 2.2B 2.4G<>
PEX_RX2 2.2B 2.4G<>
PEX_RX2* 2.3B 2.4G<>
PEX_RX3 2.3B 2.4G<>
PEX_RX3* 2.3B 2.4G<>
PEX_RX4 2.3B 2.4G<>
PEX_RX4* 2.3B 2.4G<>
PEX_RX5 2.3B 2.4G<>
PEX_RX5* 2.3B 2.4G<>
PEX_RX6 2.3B 2.4G<>
PEX_RX6* 2.3B 2.4G<>
PEX_RX7 2.3B 2.4G<>
PEX_RX7* 2.4B 2.4G<>
PEX_RX8 2.4B 2.4G<>
PEX_RX8* 2.4B 2.4G<>
PEX_RX9 2.4B 2.4G<>
PEX_RX9* 2.4B 2.4G<>
PEX_RX10 2.4B 2.4G<>
PEX_RX10* 2.4B 2.4G<>
PEX_RX11 2.4B 2.4G<>
PEX_RX11* 2.4B 2.4G<>
PEX_RX12 2.4B 2.5G<>
PEX_RX12* 2.5B 2.5G<>
PEX_RX13 2.5B 2.5G<>
PEX_RX13* 2.5B 2.5G<>
PEX_RX14 2.5B 2.5G<>
PEX_RX14* 2.5B 2.5G<>
PEX_RX15 2.5B 2.5G<>
PEX_RX15* 2.5B 2.5G<>
PEX_SMCLK 2.1B
PEX_SMDAT 2.1B
PEX_TCLK 2.1B
PEX_TDI 2.1B
PEX_TDO 2.1B
PEX_TERMP 2.5E
PEX_TMS 2.1B
PEX_TRST* 2.1B
PEX_TX0 2.1G<> 2.2D
PEX_TX0* 2.1G<> 2.2C
PEX_TX1 2.1G<> 2.2D
PEX_TX1* 2.1G<> 2.2C
PEX_TX2 2.2D 2.2G<>
PEX_TX2* 2.2C 2.2G<>
PEX_TX3 2.2G<> 2.3D
PEX_TX3* 2.2G<> 2.3C
PEX_TX4 2.2G<> 2.3D
PEX_TX4* 2.2G<> 2.3C
PEX_TX5 2.2G<> 2.3D
PEX_TX5* 2.2G<> 2.3C
PEX_TX6 2.2G<> 2.3D
PEX_TX6* 2.2G<> 2.3C
PEX_TX7 2.2G<> 2.3D
PEX_TX7* 2.2G<> 2.3C
PEX_TX8 2.2G<> 2.4D
PEX_TX8* 2.2G<> 2.4C
PEX_TX9 2.2G<> 2.4D
PEX_TX9* 2.2G<> 2.4C
PEX_TX10 2.2G<> 2.4D
PEX_TX10* 2.2G<> 2.4C
PEX_TX11 2.2G<> 2.4D
PEX_TX11* 2.2G<> 2.4C
PEX_TX12 2.2G<> 2.4C
PEX_TX12* 2.2G<> 2.4C
PEX_TX13 2.2G<> 2.5D
PEX_TX13* 2.2G<> 2.5C
PEX_TX14 2.2G<> 2.5D
PEX_TX14* 2.2G<> 2.5C
PEX_TX15 2.2G<> 2.5D
PEX_TX15* 2.2G<> 2.5C
PEX_TX0D 2.2B 2.3G<>
PEX_TX0D* 2.2B 2.3G<>
PEX_TX1D 2.2B 2.3G<>
PEX_TX1D* 2.2B 2.3G<>
PEX_TX2D 2.2B 2.3G<>
PEX_TX2D* 2.2B 2.3G<>
PEX_TX3D 2.3B 2.3G<>
PEX_TX3D* 2.3B 2.3G<>
PEX_TX4D 2.3B 2.3G<>
PEX_TX4D* 2.3B 2.3G<>

PEX_TX5 2.3B 2.3G<>
PEX_TX5* 2.3B 2.3G<>
PEX_TX6 2.3B 2.3G<>
PEX_TX6* 2.3B 2.3G<>
PEX_TX7 2.3B 2.3G<>
PEX_TX7* 2.3B 2.3G<>
PEX_TX8 2.3G<> 2.4B
PEX_TX8* 2.3G<> 2.4B
PEX_TX9 2.3G<> 2.4B
PEX_TX9* 2.3G<> 2.4B
PEX_TX10 2.3G<> 2.4B
PEX_TX10* 2.3G<> 2.4B
PEX_TX11 2.3G<> 2.4B
PEX_TX11* 2.3G<> 2.4B
PEX_TX12 2.3G<> 2.4B
PEX_TX12* 2.3G<> 2.4B
PEX_TX13 2.3G<> 2.5B
PEX_TX13* 2.3G<> 2.5B
PEX_TX14 2.3G<> 2.5B
PEX_TX14* 2.4G<> 2.5B
PEX_TX15 2.4G<> 2.5B
PEX_TX15* 2.4G<> 2.5B
PEX_VDD 19.1G
PS_1V1_CP 19.2C
PS_1V1_DR 19.2C
PS_1V1_FB 19.2C
PS_1V8_ADJ 18.3B
PS_2V5_ADJ 18.3E
PS_FBVDDQ_FS 19.2C
PS_FB_BOOT 19.2D
PS_FB_BOOT_R 19.2E
PS_FB_COMP 19.3D
PS_FB_EN 19.4B
PS_FB_EN* 19.4C
PS_FB_FB 19.2D
PS_FB_LGATE 19.2D
PS_FB_PHASE 19.2E
PS_FB_PVCC5 19.2D
PS_FB_RBOT 19.4F
PS_FB_RC 19.3G
PS_FB_RC_CP 19.3D
PS_FB_SNUB 19.3F
PS_FB_UGATE 19.2D
PS_FB_VCC5 19.2C
PS_FB_VCC12 19.2D
PS_FB_VSEL 19.4E
PS_NVVDD_BOOT1 20.1D 20.2C
PS_NVVDD_BOOT1_RC 20.1C
PS_NVVDD_BOOT2 20.1D 20.2C
PS_NVVDD_BOOT2_RC 20.3C
PS_NVVDD_CP 20.2B
PS_NVVDD_DRVH1 20.1D
PS_NVVDD_DRVH2 20.2C
PS_NVVDD_DRVL1 20.2C
PS_NVVDD_DRVL2 20.3C
PS_NVVDD_EN 20.5B
PS_NVVDD_EN* 20.4B
PS_NVVDD_EN_AND 20.5B
PS_NVVDD_FB 20.2B
PS_NVVDD_FS 20.2B
PS_NVVDD_OC 20.3C
PS_NVVDD_PGOOD 19.4B< 20.2B>
PS_NVVDD_PH1 20.2C
PS_NVVDD_PH2 20.2C
PS_NVVDD_RC 20.4G
PS_NVVDD_RC1 20.2F
PS_NVVDD_RC2 20.3F
PS_NVVDD_RC_CP 20.1B
PS_NVVDD_SS 20.2B
PS_NVVDD_VCC 20.2C
PS_NVVDD_VSEN 20.4G
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SNN_J26 17.3B
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SPDIF_TERM 15.2C
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STRAP1 13.4E<> 17.2B<
STRAP2 13.4E<> 17.2B<
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STRAP_MIOB 17.4B
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THERMAL_N_R 16.2G
THERMAL_P* 16.2G
THERMAL_P_Q 16.2G
THERM_ALERT 16.2B
THERM_DA 16.3B
THERM_DA_R 16.3A
THERM_DC 16.3B
THERM_DC_R 16.3A
THERM_SHUTDOWN* 16.2H> 20.4A<
THERM_VDD 16.2B
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TV_PBOUT_C 14.1A<> 14.4G
TV_YOUT_C 14.1A<> 14.3G
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XTAL_IN_SEL 15.5C
XTAL_OUT 15.4G< 15.5D
XTAL_OUTBUFF 15.4D 15.5G<
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Date: Jan 16 15:30:01 2008

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LB11 [11.3A]
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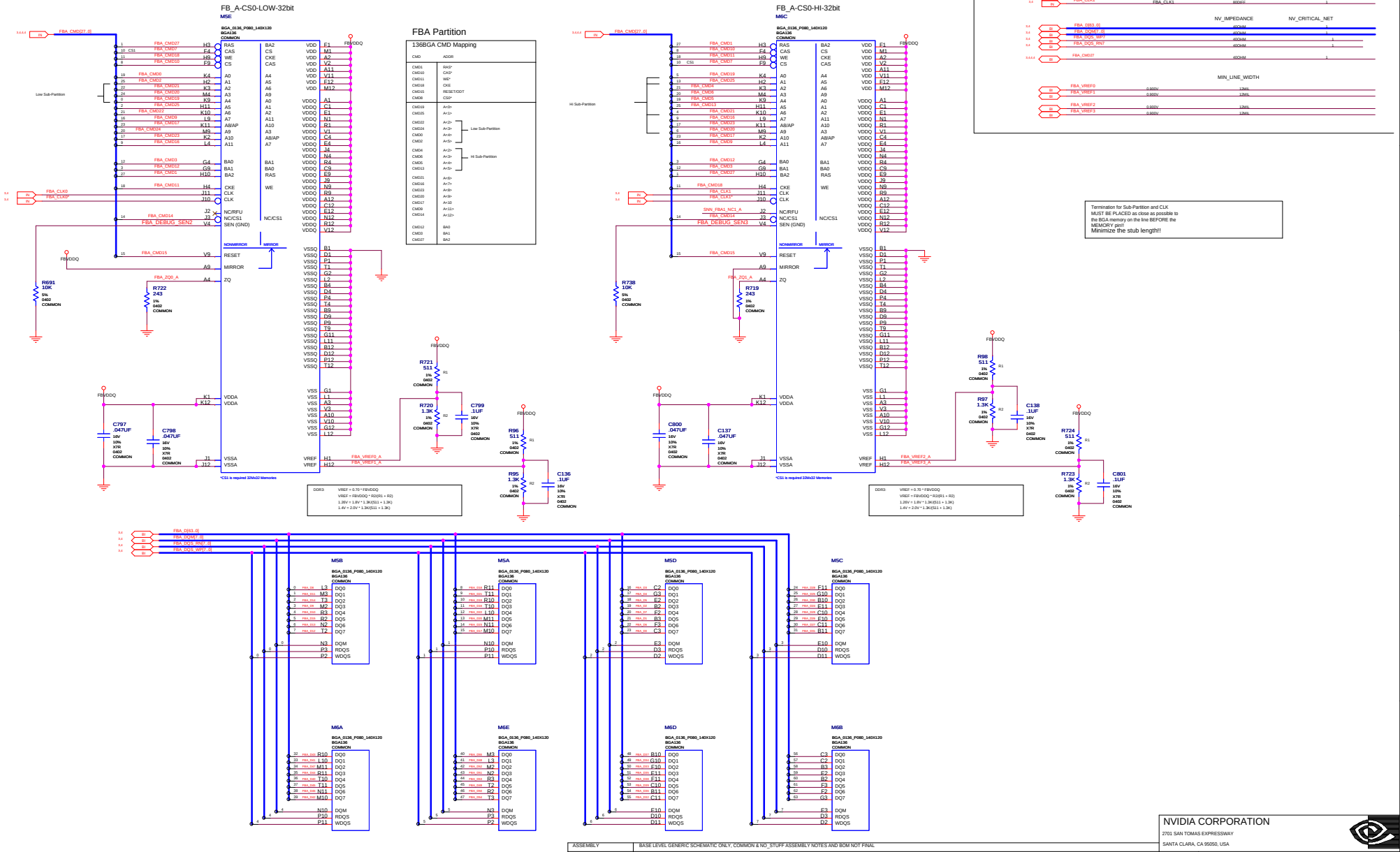

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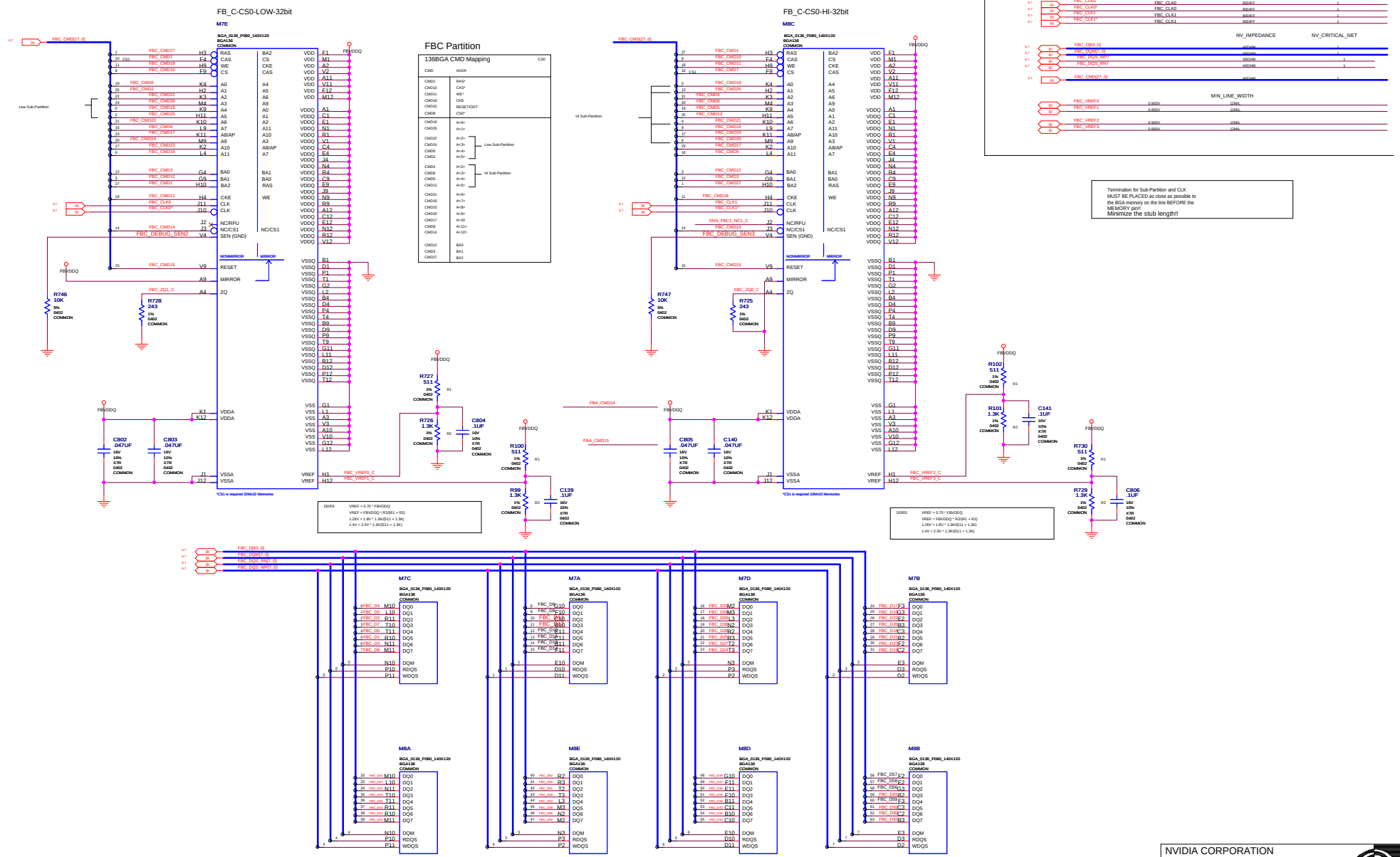

FBC Partition

136BGA CMD Mapping

CMD	ADDR	CS0
CMD1	RAS*	
CMD10	CAS*	
CMD11	WE*	
CMD18	CKE	
CMD15	RESET/ODT	
CMD8	CS0*	
CMD19	A<0>	
CMD25	A<1>	
CMD22	A<2>	Low Sub-Partition
CMD24	A<3>	
CMD0	A<4>	
CMD2	A<5>	
CMD4	A<2>	Hi Sub-Partition
CMD6	A<3>	
CMD5	A<4>	
CMD13	A<5>	
CMD21	A<6>	
CMD16	A<7>	
CMD23	A<8>	
CMD20	A<9>	
CMD17	A<10>	
CMD9	A<11>	
CMD14	A<12>	
CMD12	BA0	
CMD3	BA1	
CMD27	BA2	

DDR3: VREF = 0.70 * FBVDDQ
VREF = FBVDDQ * R2/(R1 + R2)
1.26V = 1.8V * 1.3K/(511 + 1.3K)
1.4V = 2.0V * 1.3K/(511 + 1.3K)

*CS1 is required 32Mx32 Memories

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