GA102 DT SKU P-BOARD

350W, FH Std PCB, 384b, GDDR6X x8
DP + DP + DP + HDMI/DP

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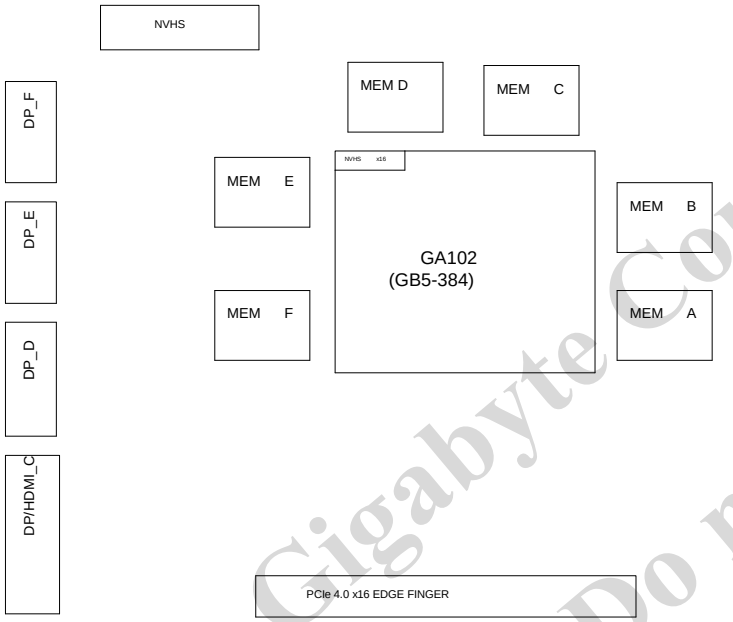

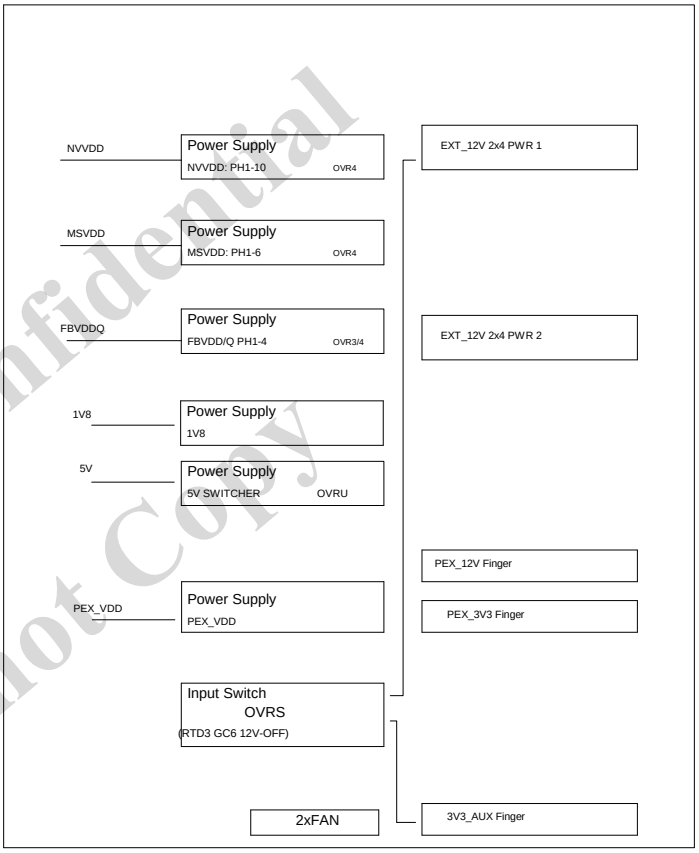

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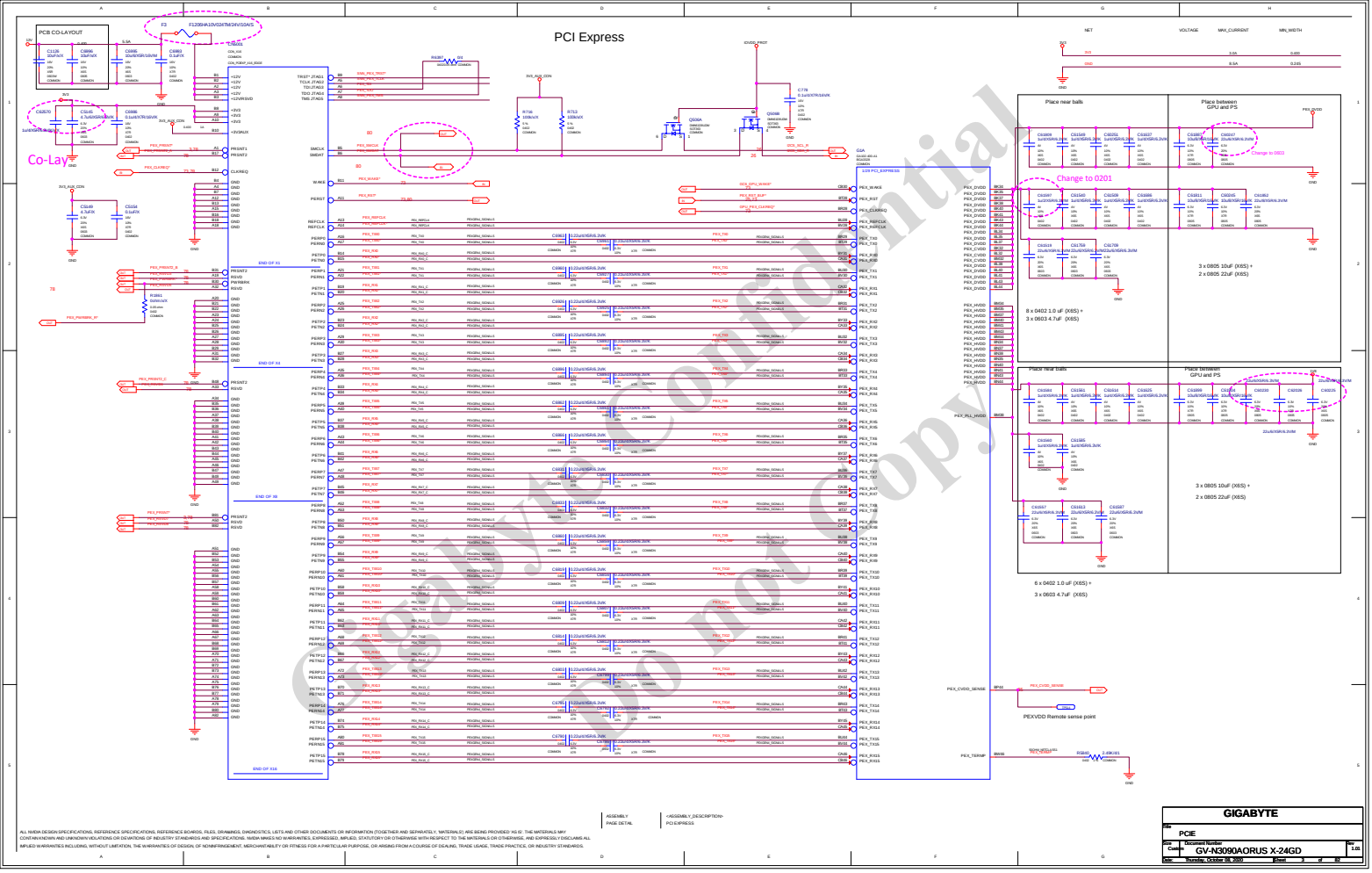

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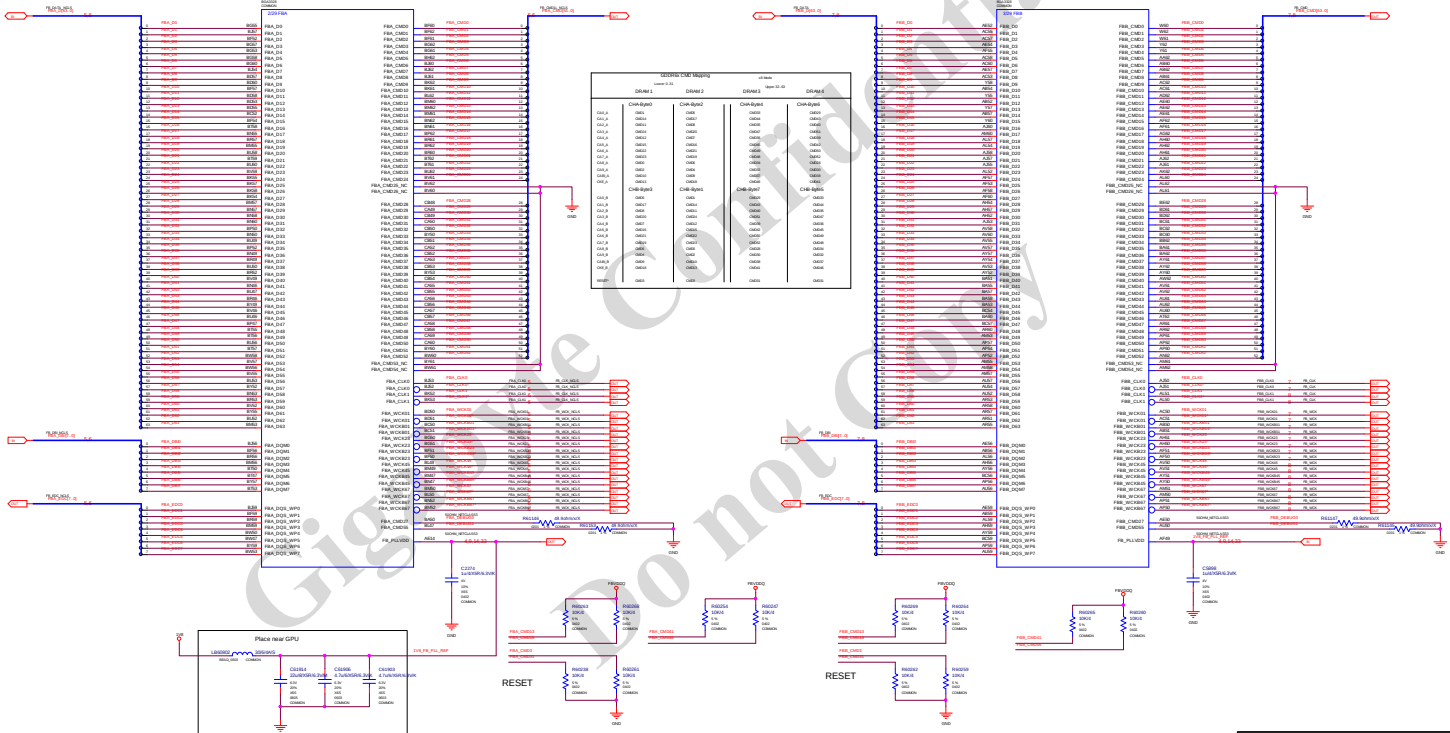

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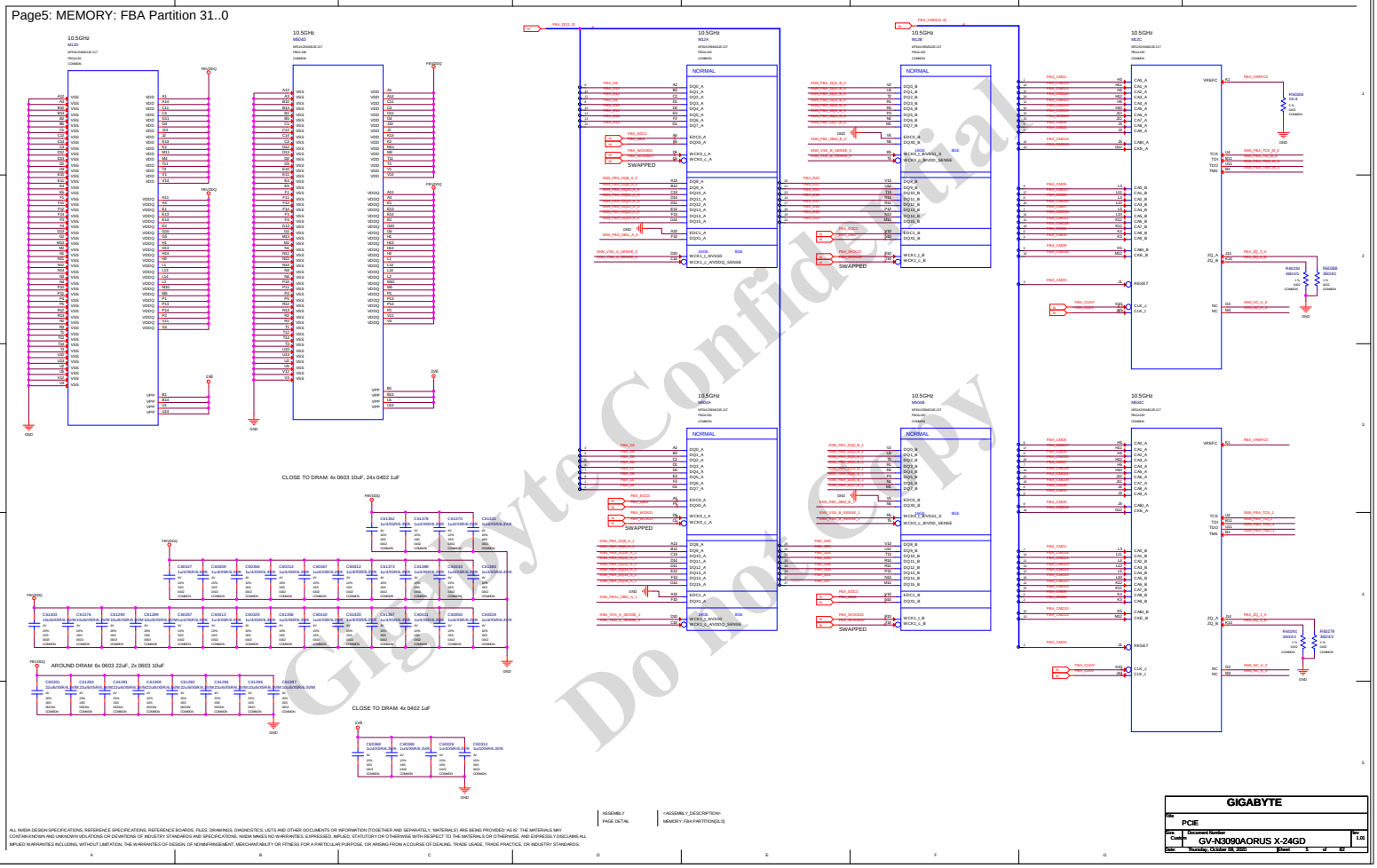

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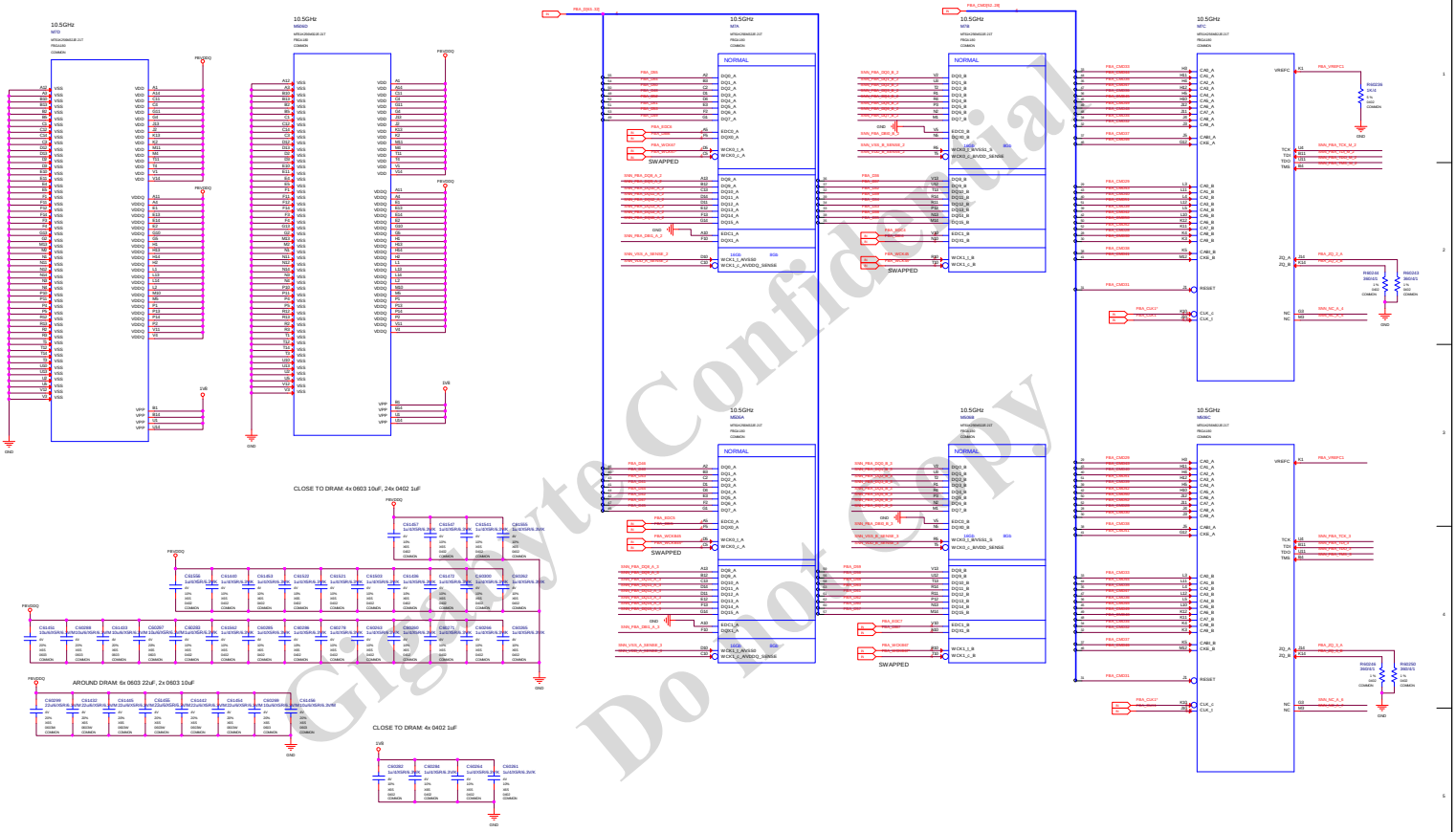

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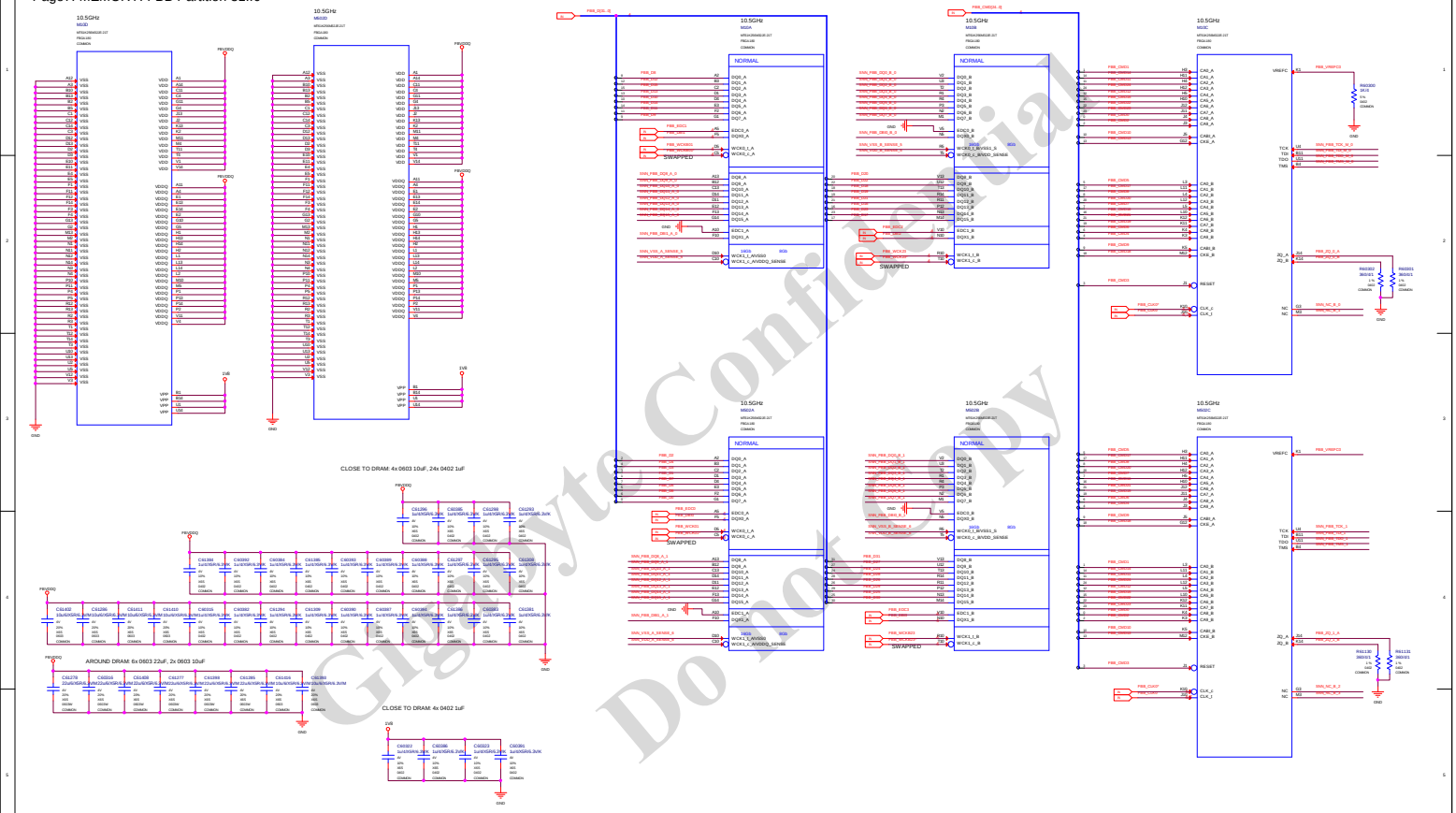

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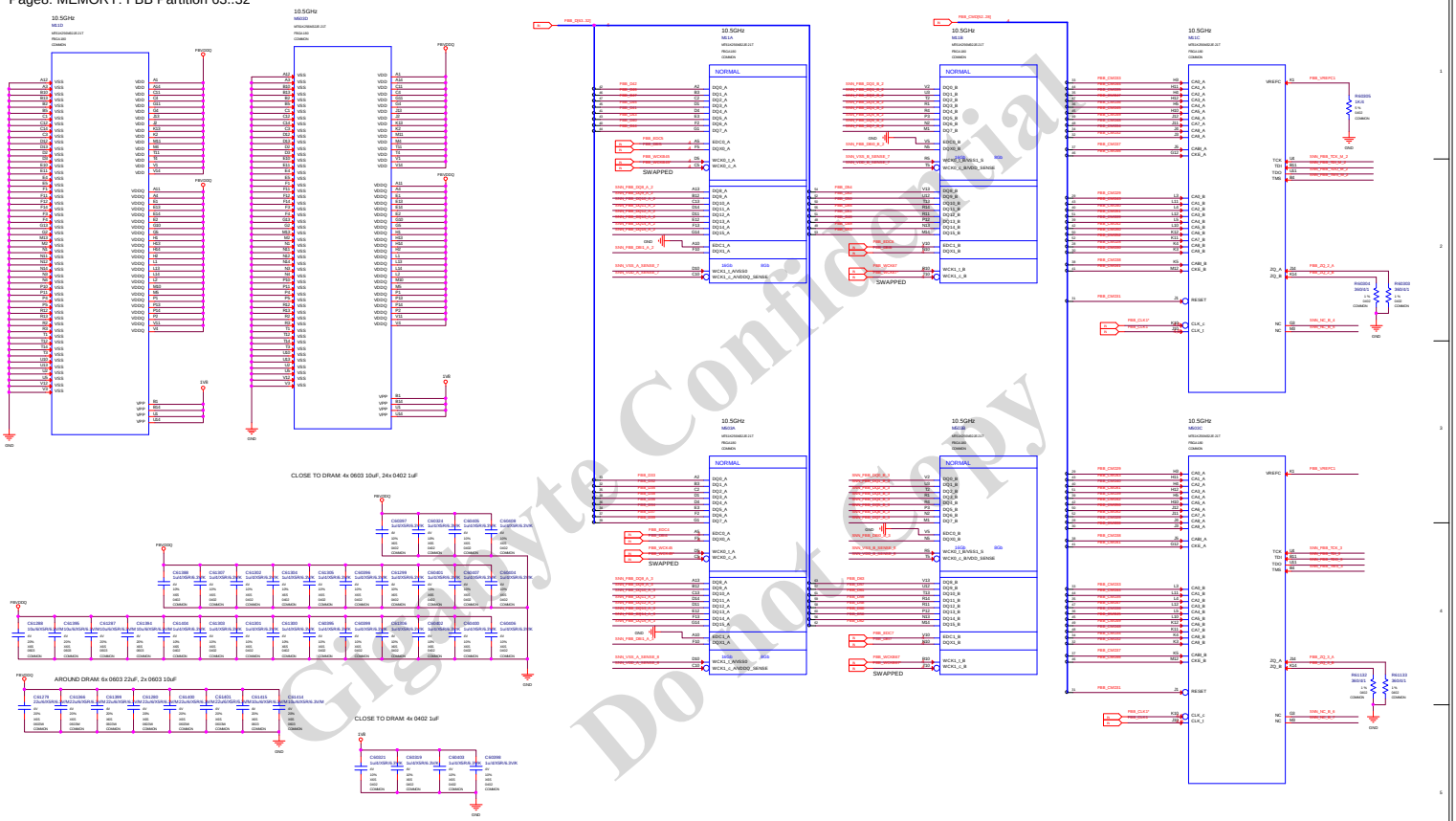

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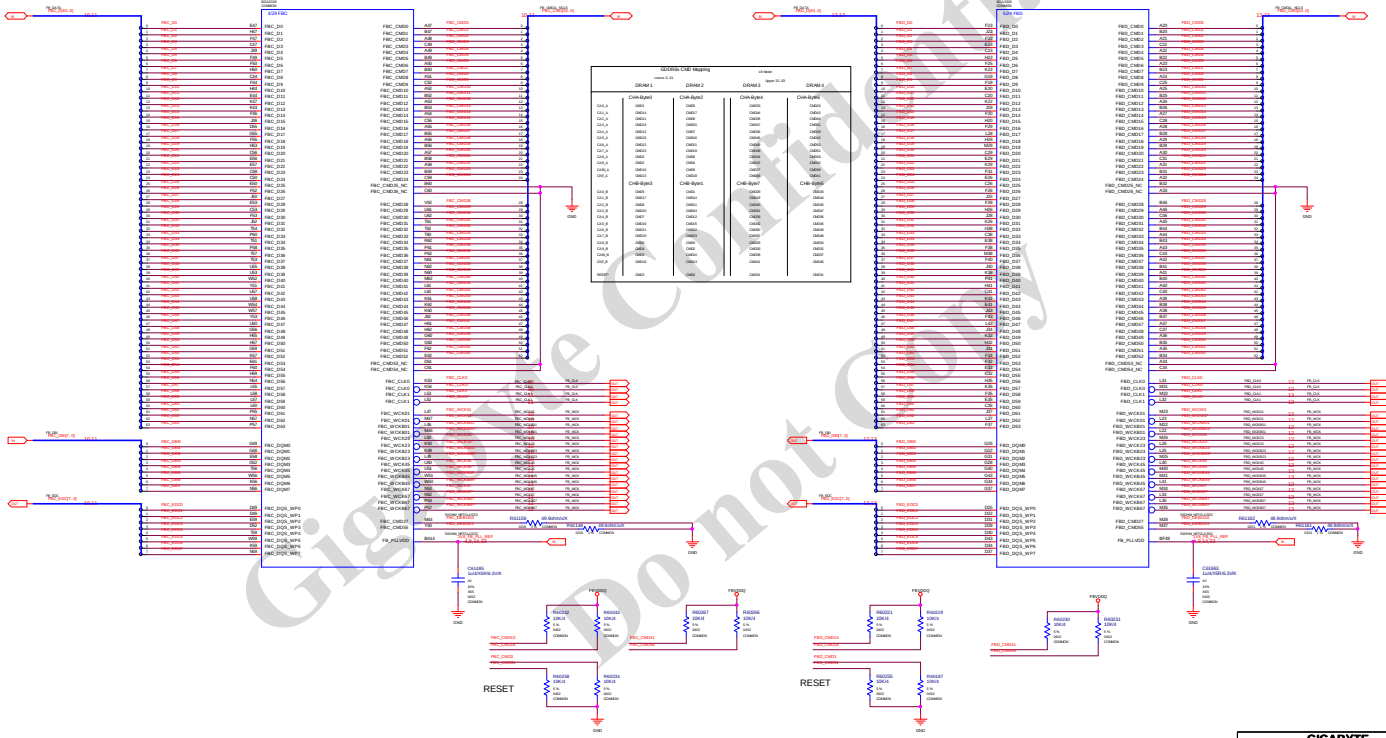

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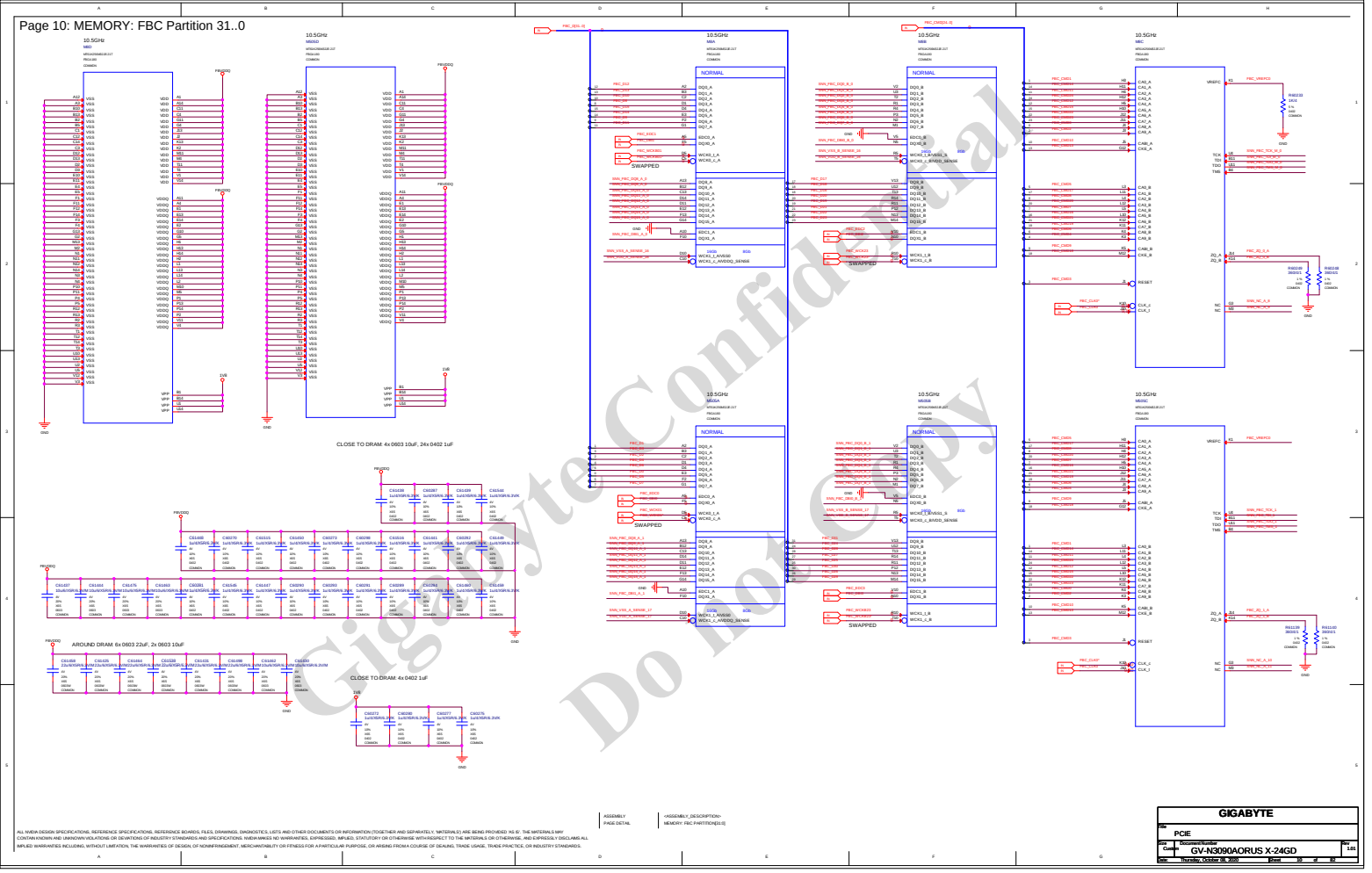

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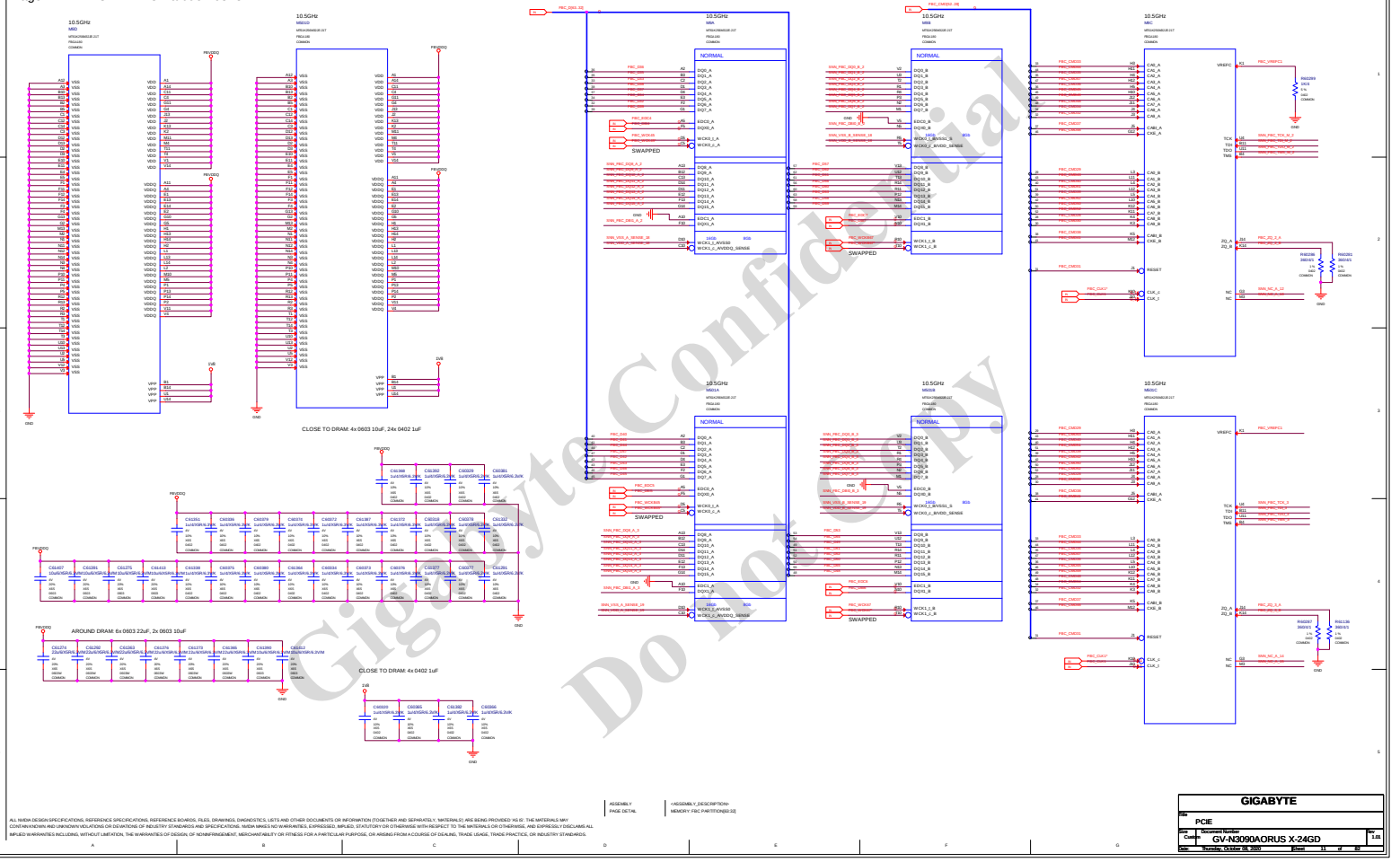

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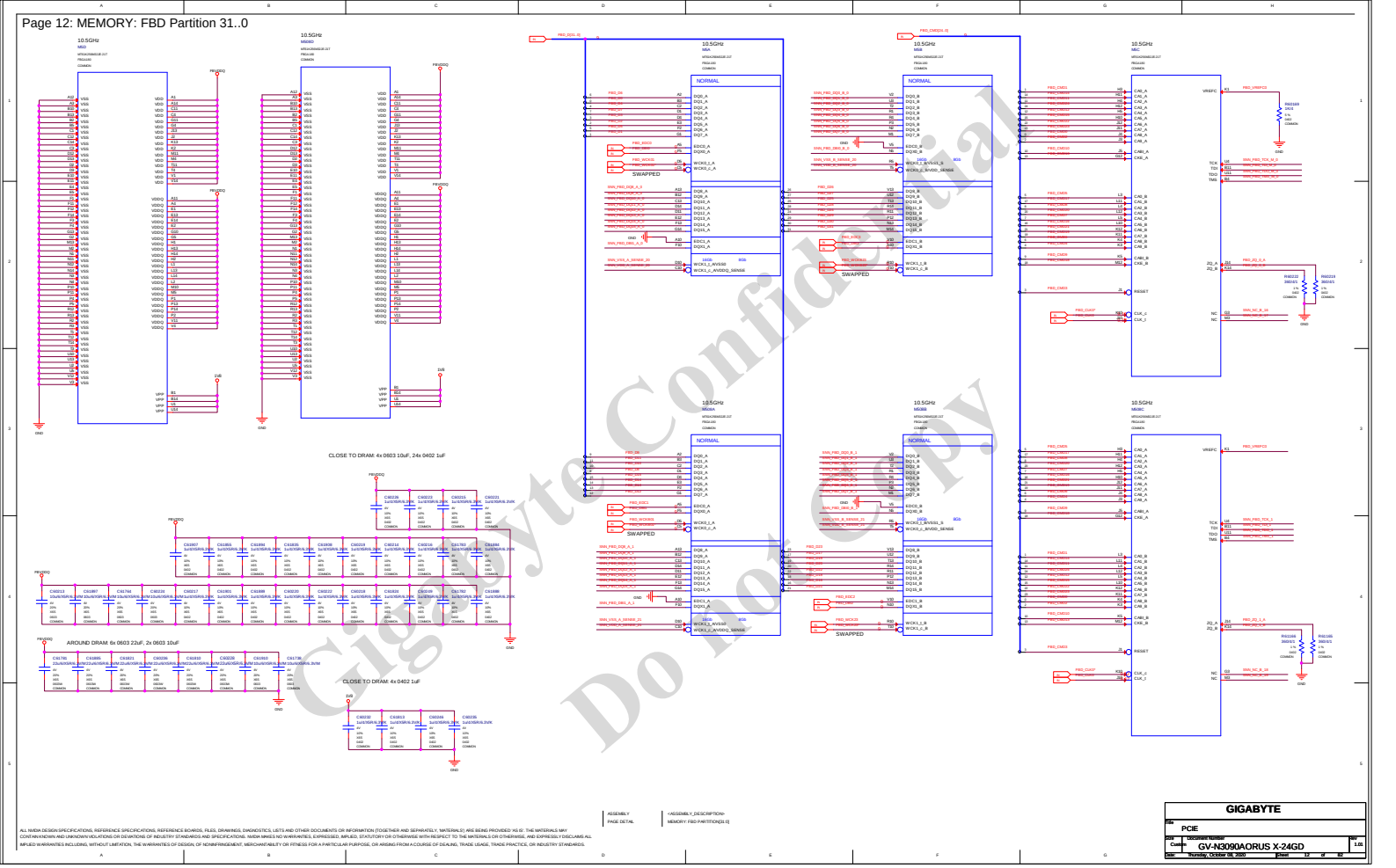

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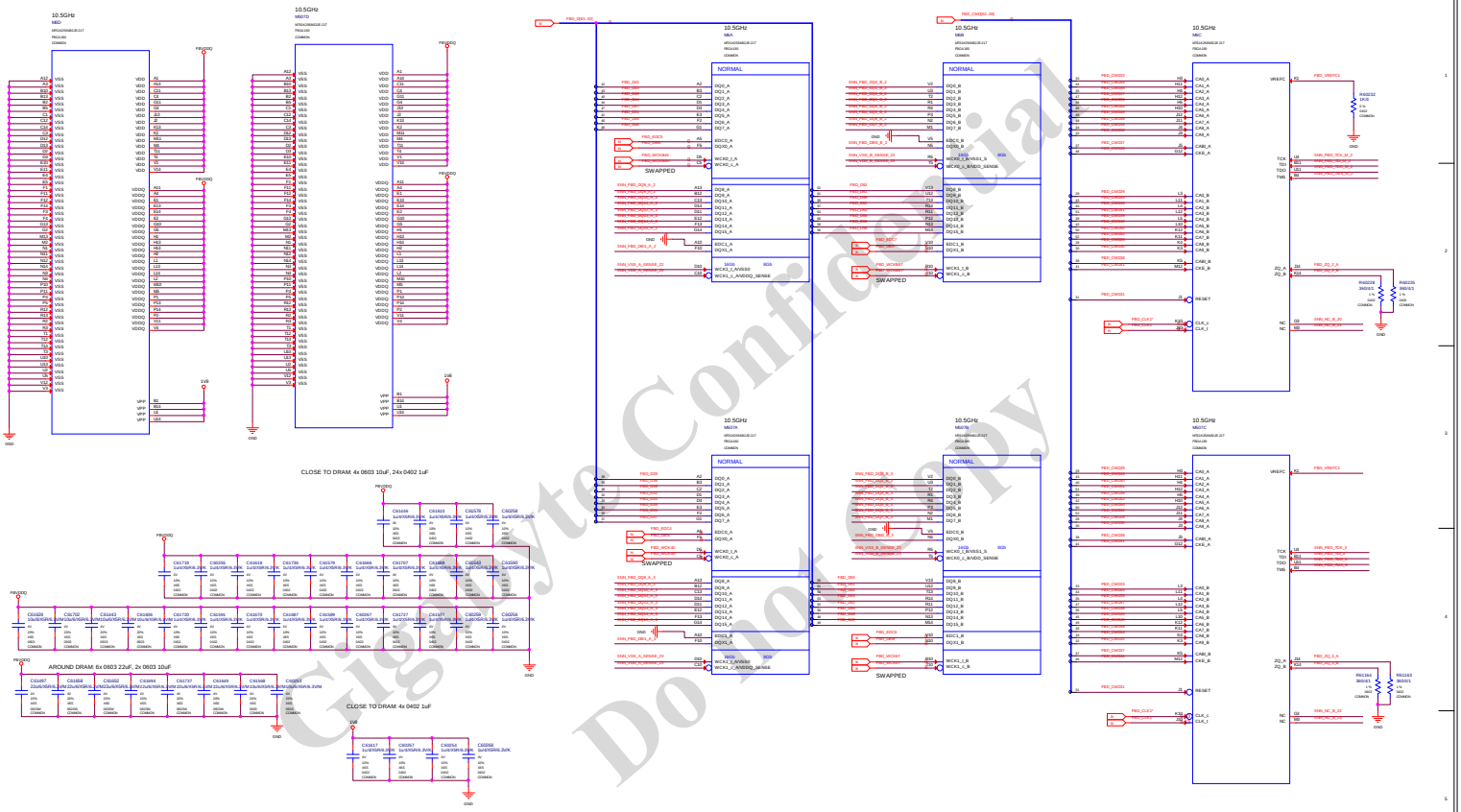

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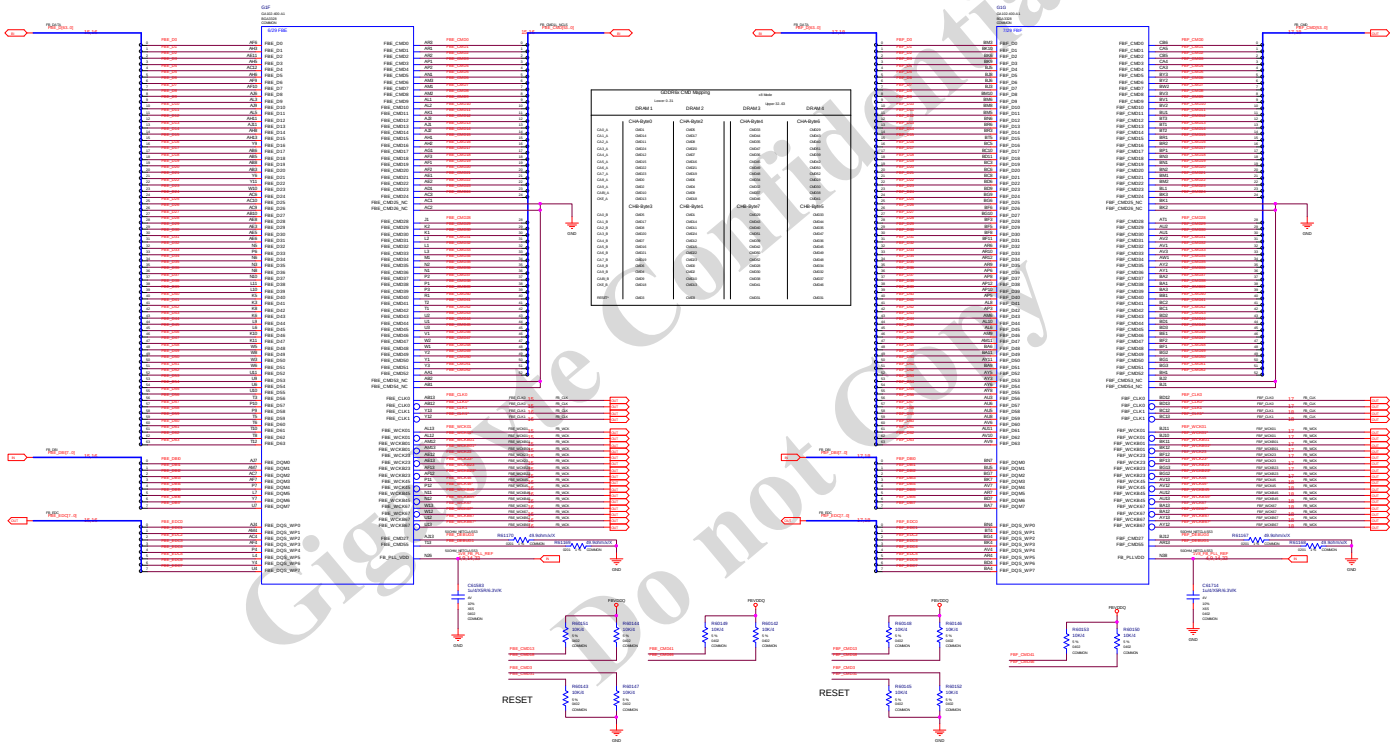

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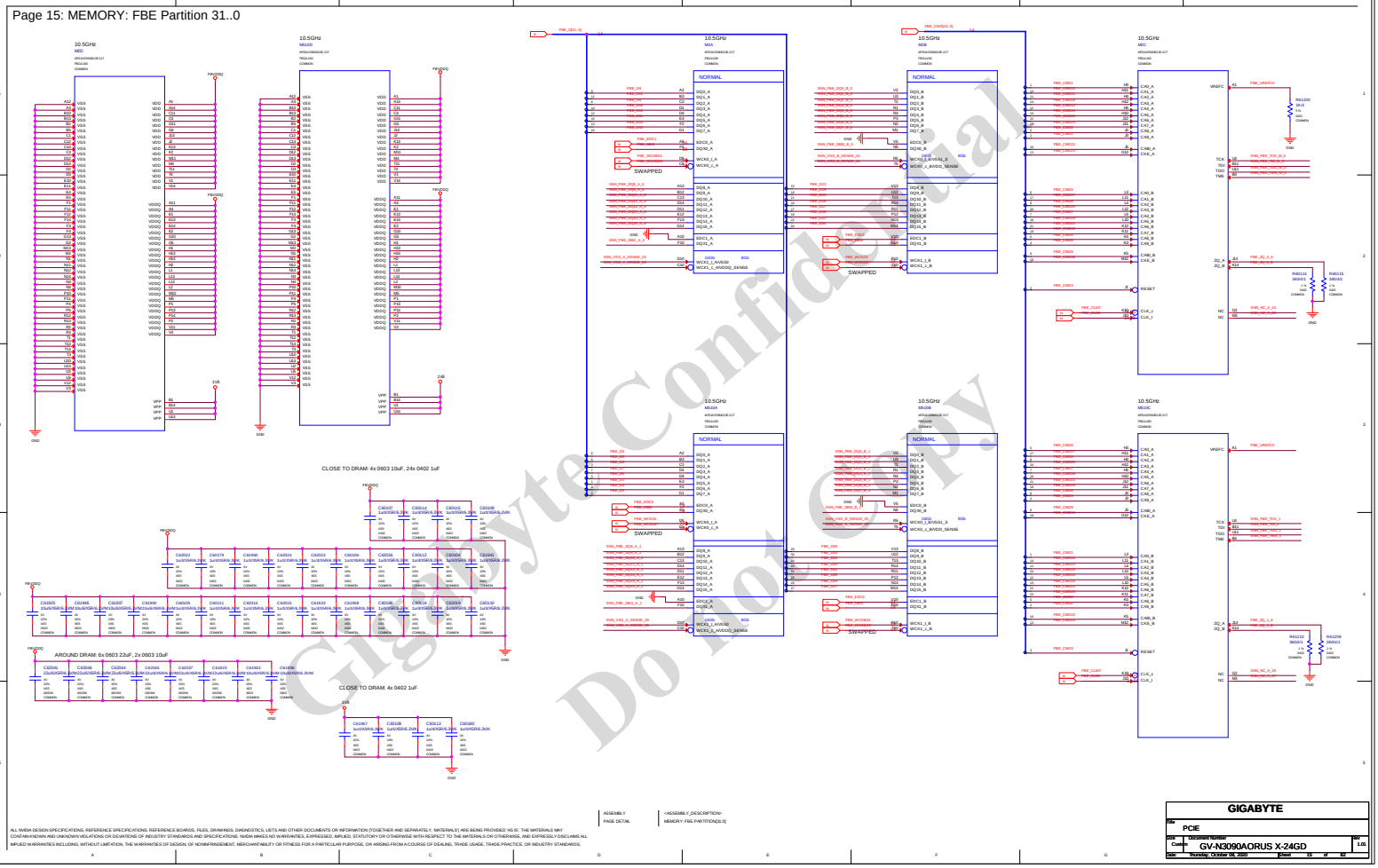

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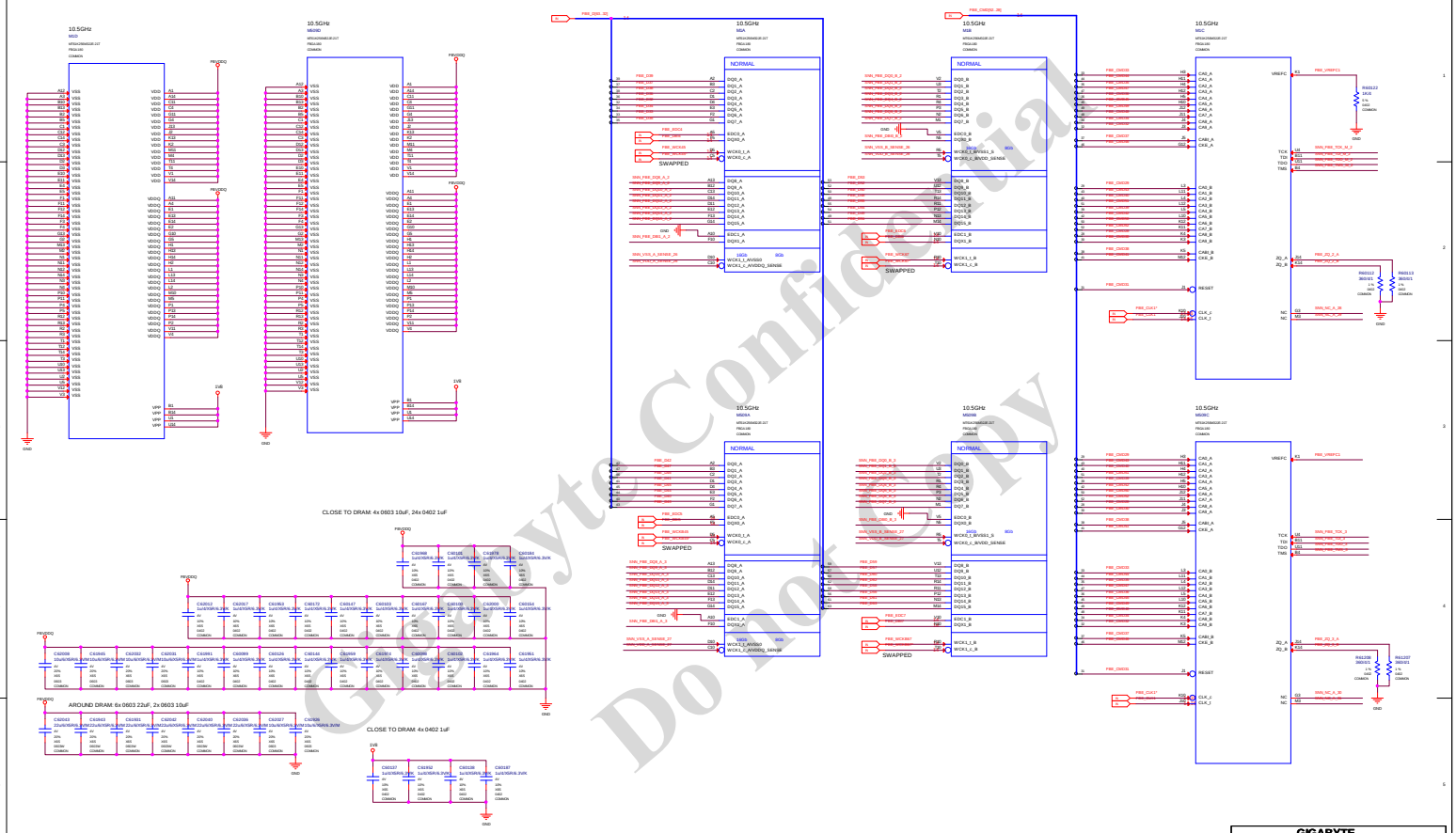

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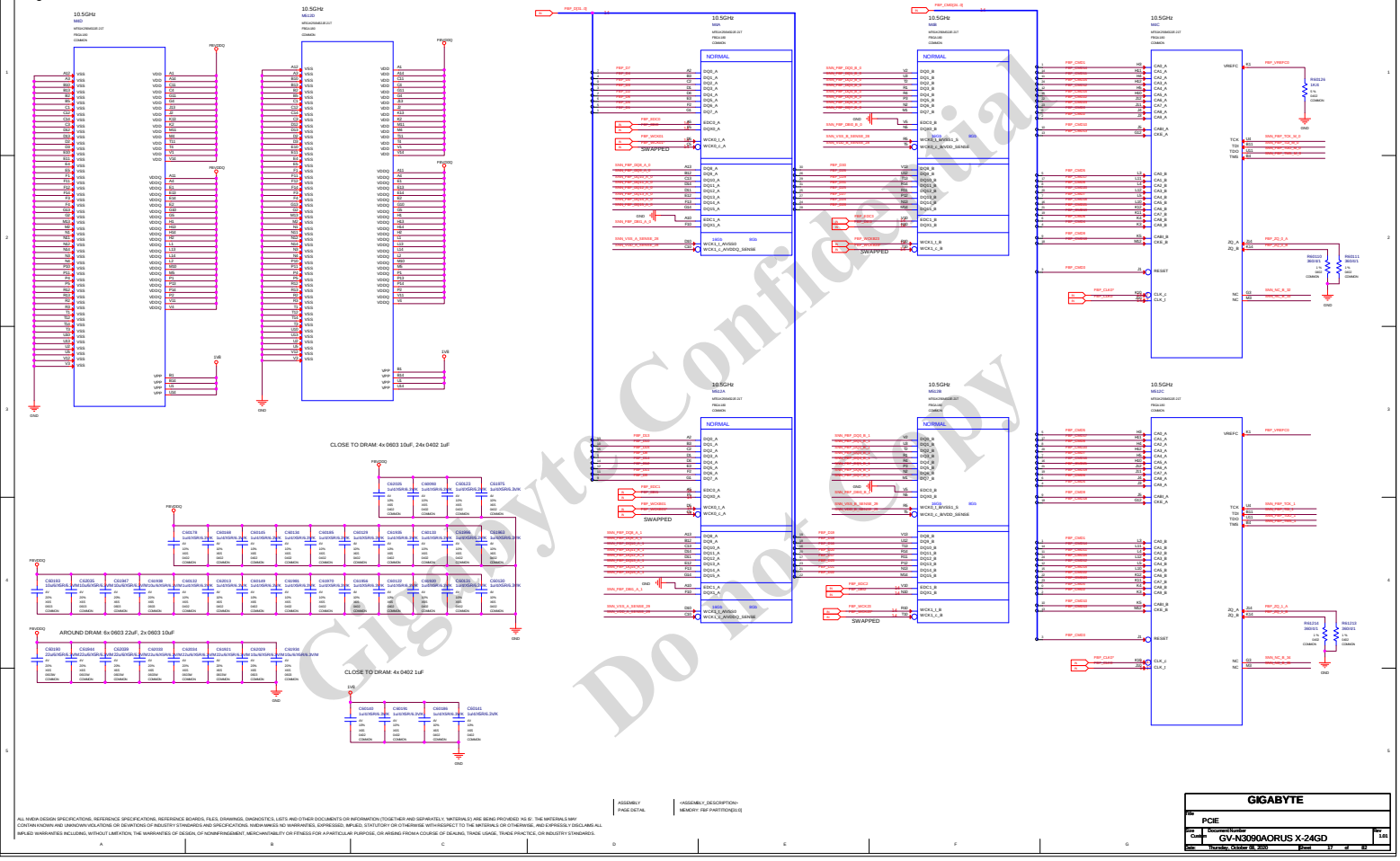

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PAGE DETAIL	MEMORY: FBF PARTITION[31:0]

GIGABYTE

Title	PCIE
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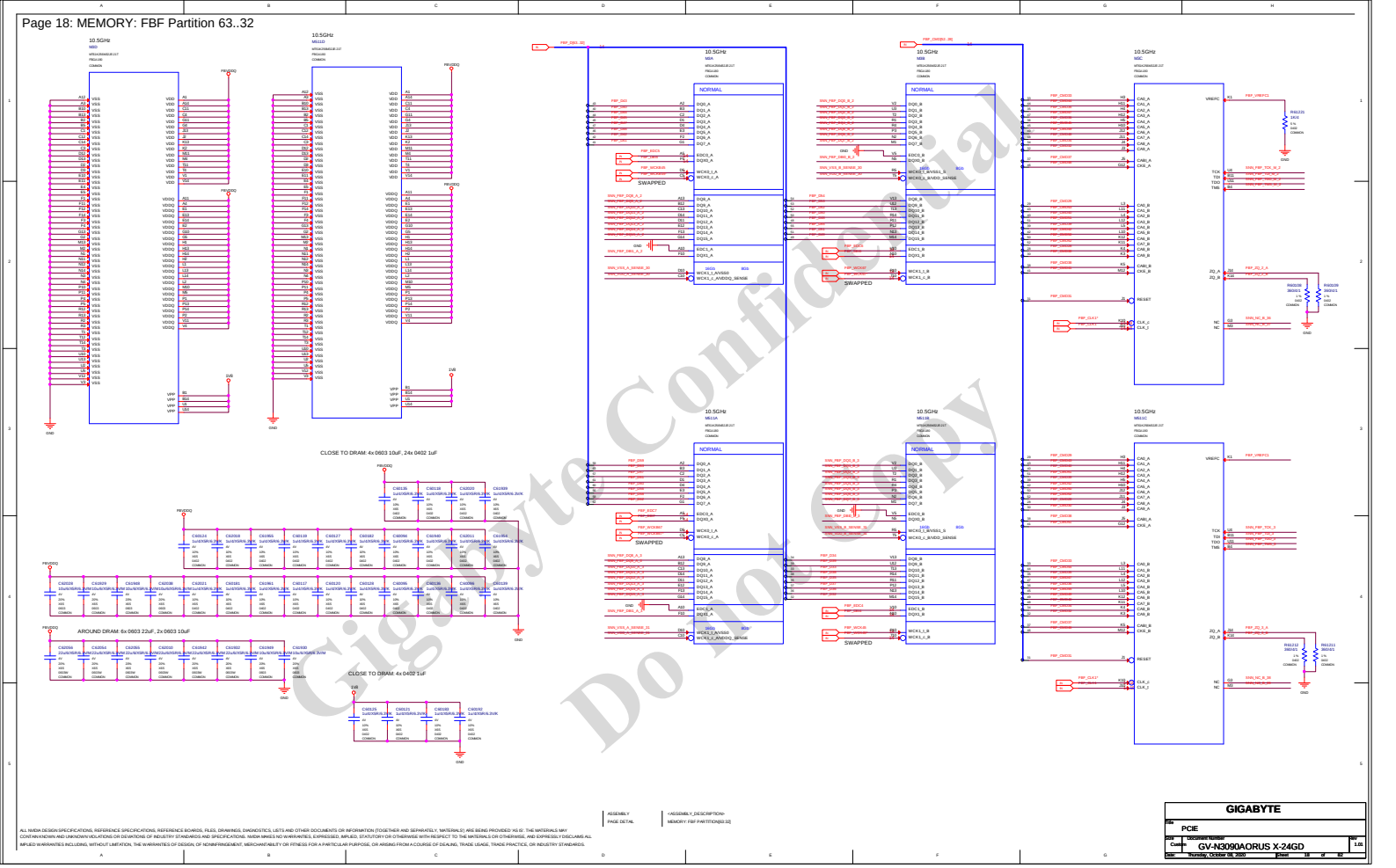
Page 18: MEMORY: FBF Partition 63..32



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ASSEMBLY
PAGE DETAIL

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GIGABYTE

File: PCIE

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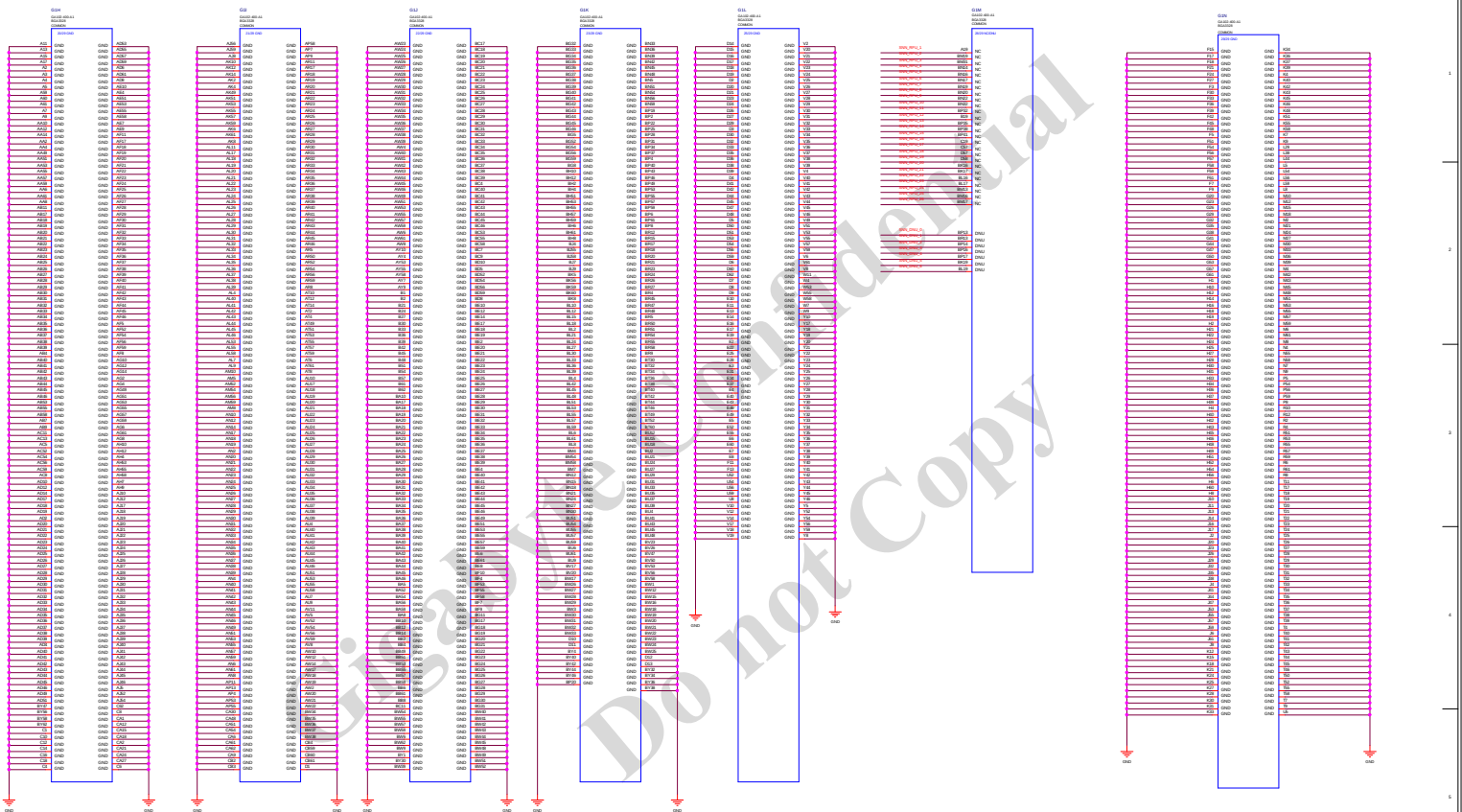
GPU GND, RFUs & RSVD



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ASSEMBLY
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GPU GND, RFUs & RSVD

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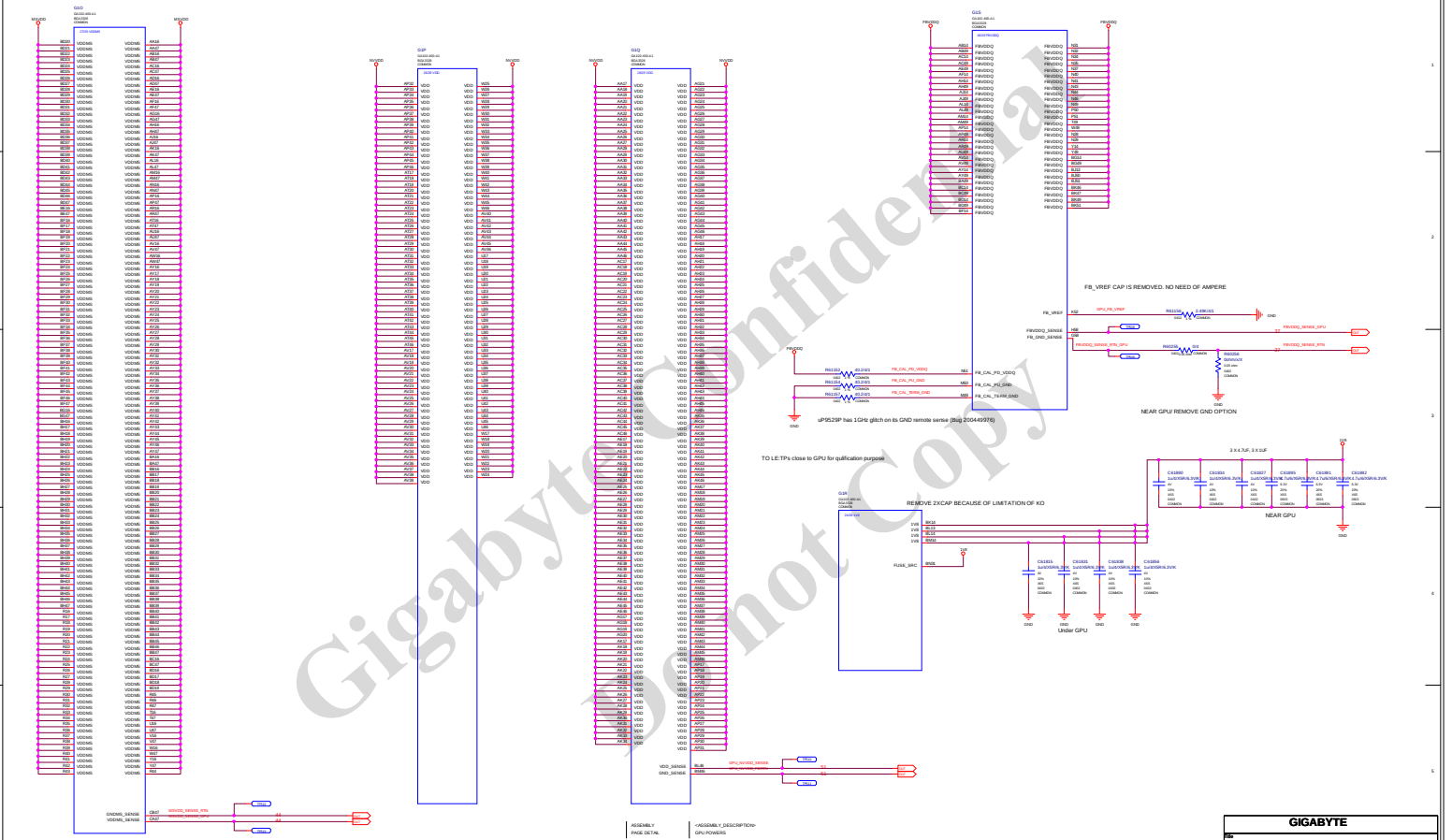
GPU PWR and GND



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PAGE DETAIL	GPU POWERS

GIGABYTE

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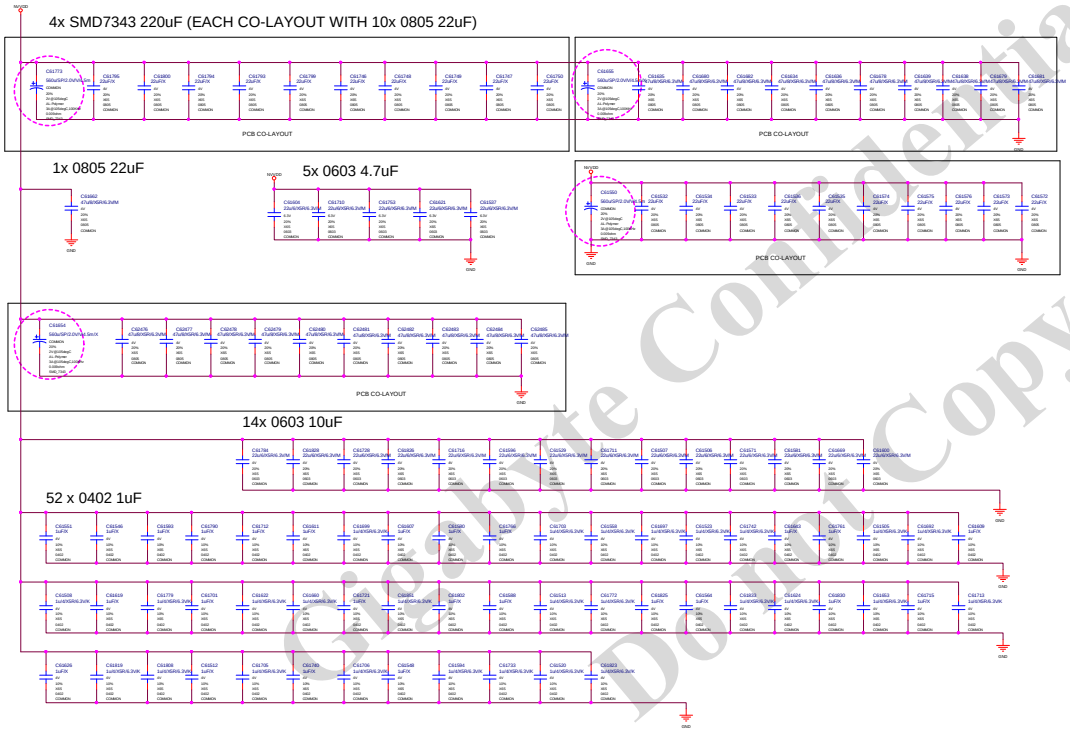
NVVDD

UNDER GPU



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ASSEMBLY
PAGE DETAIL

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GPU NVVDD DECOUPLING

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GIGABYTE			
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Code	C00000000000000		Rev 1.01
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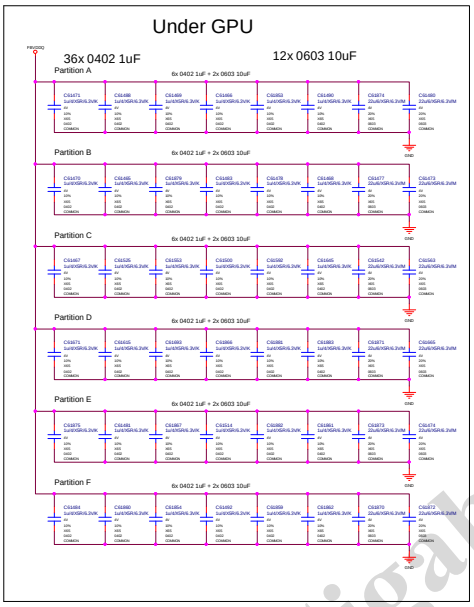
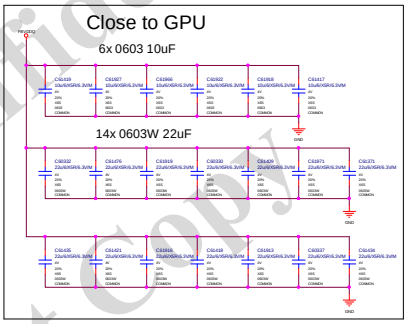
FBVDDQ





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PAGE DETAIL	GPU: FBVDD DECOUPLING

GIGABYTE		
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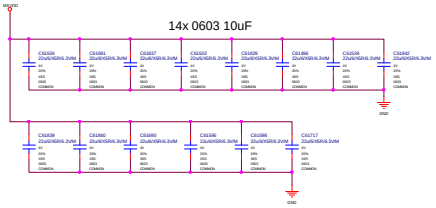
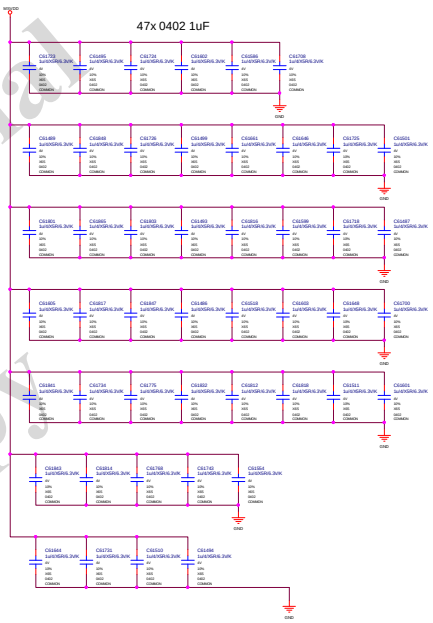
UNDER GPU

MSVDD

14x 0603 10uF

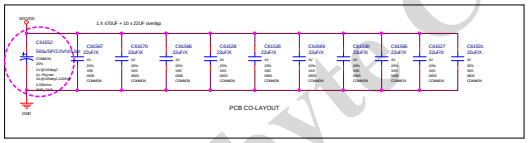


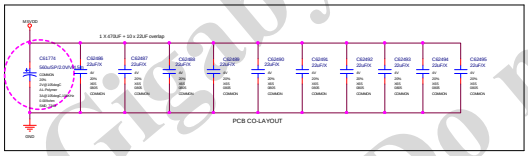
47x 0402 1uF



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)





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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU MSVDD DECOUPLING

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Size: D	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
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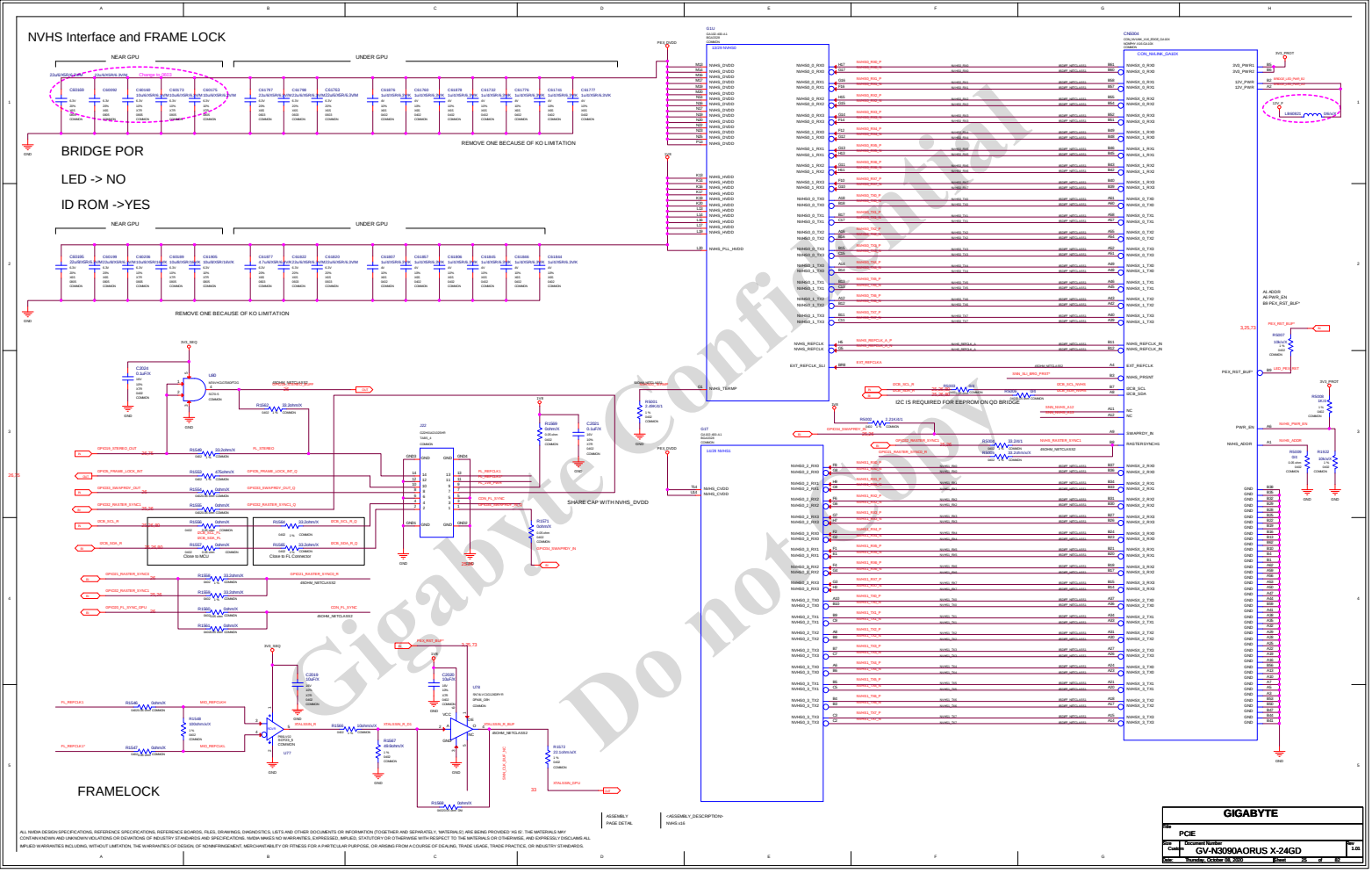

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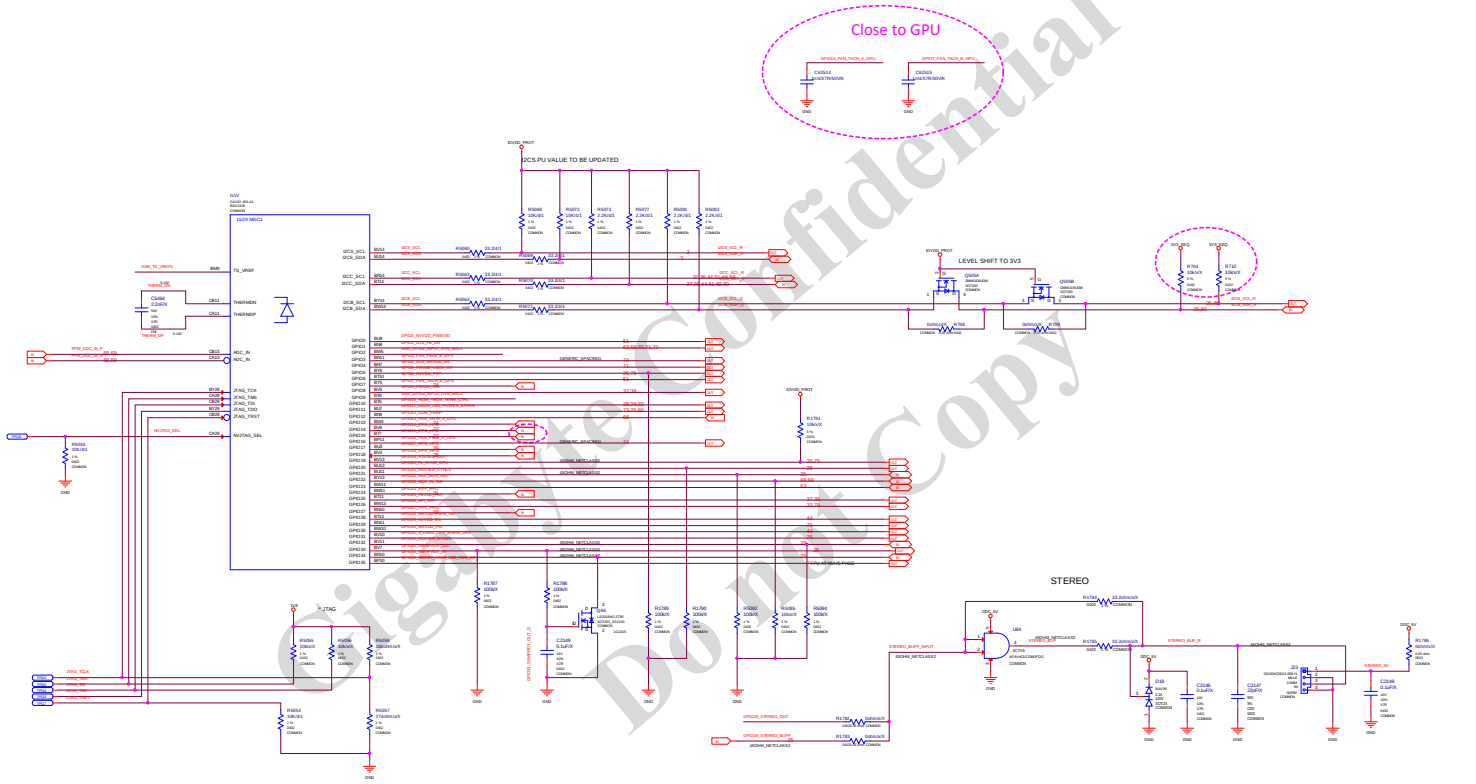
MISC1: Fan, Thermal, JTAG, GPIO, STEREO



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: THERMAL, JTAG, GPIO

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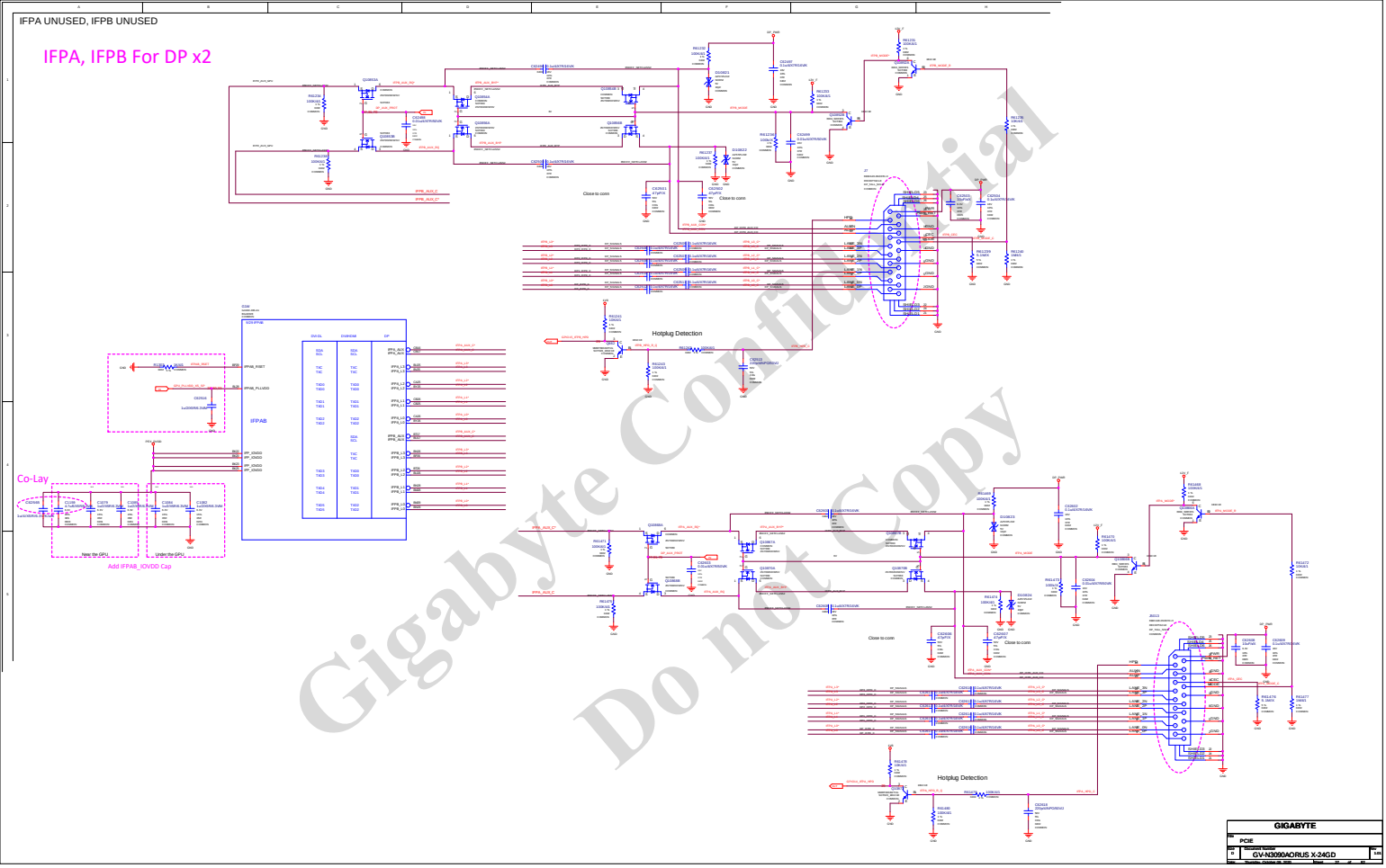
IFPA UNUSED, IFPB UNUSED

IFPA, IFPB For DP x2



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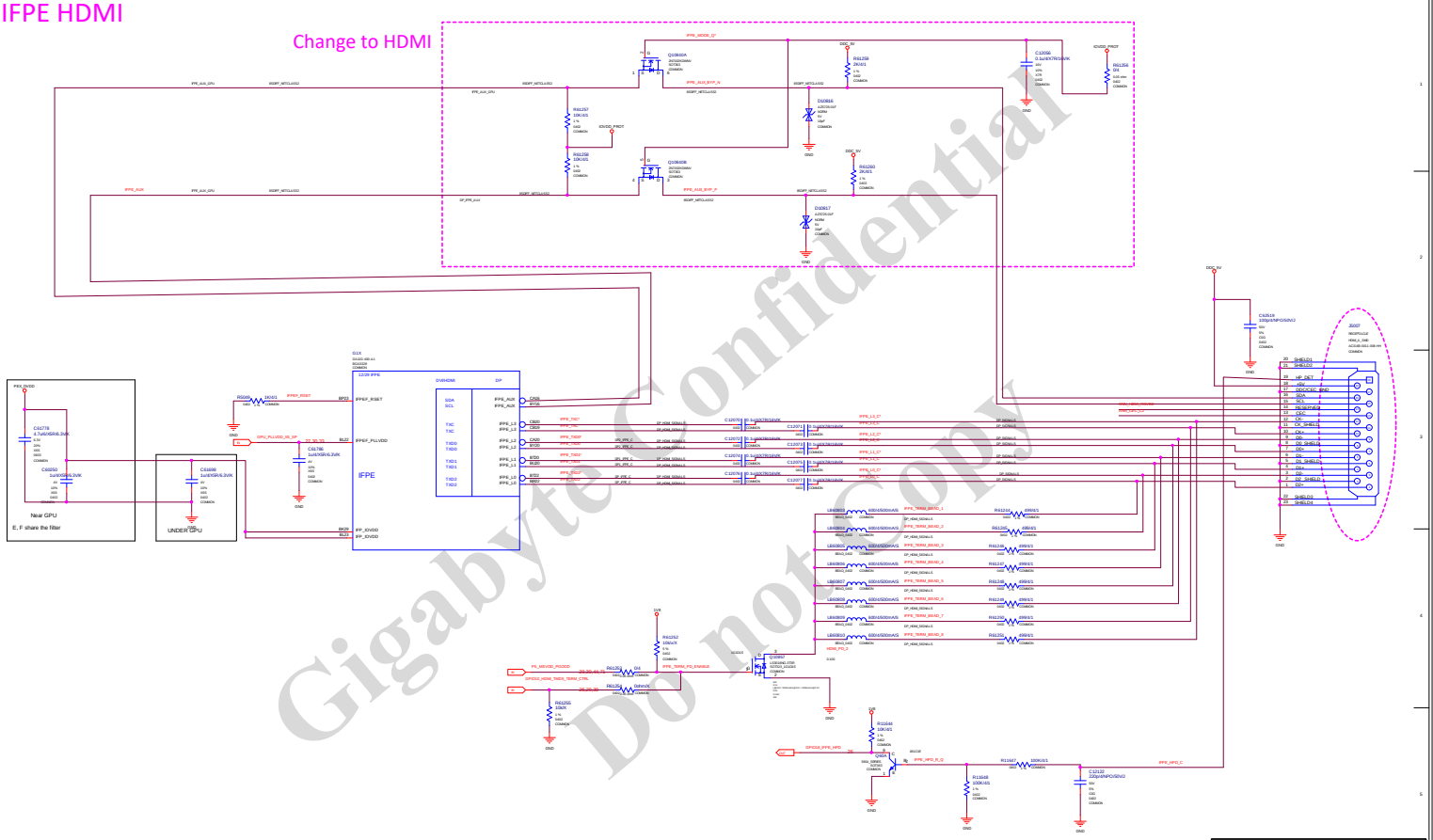
PCIE

GV-N3090AORUS X-24GD

IFPE HDMI

Change to HDMI



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PAGE DETAIL	IFPE DP

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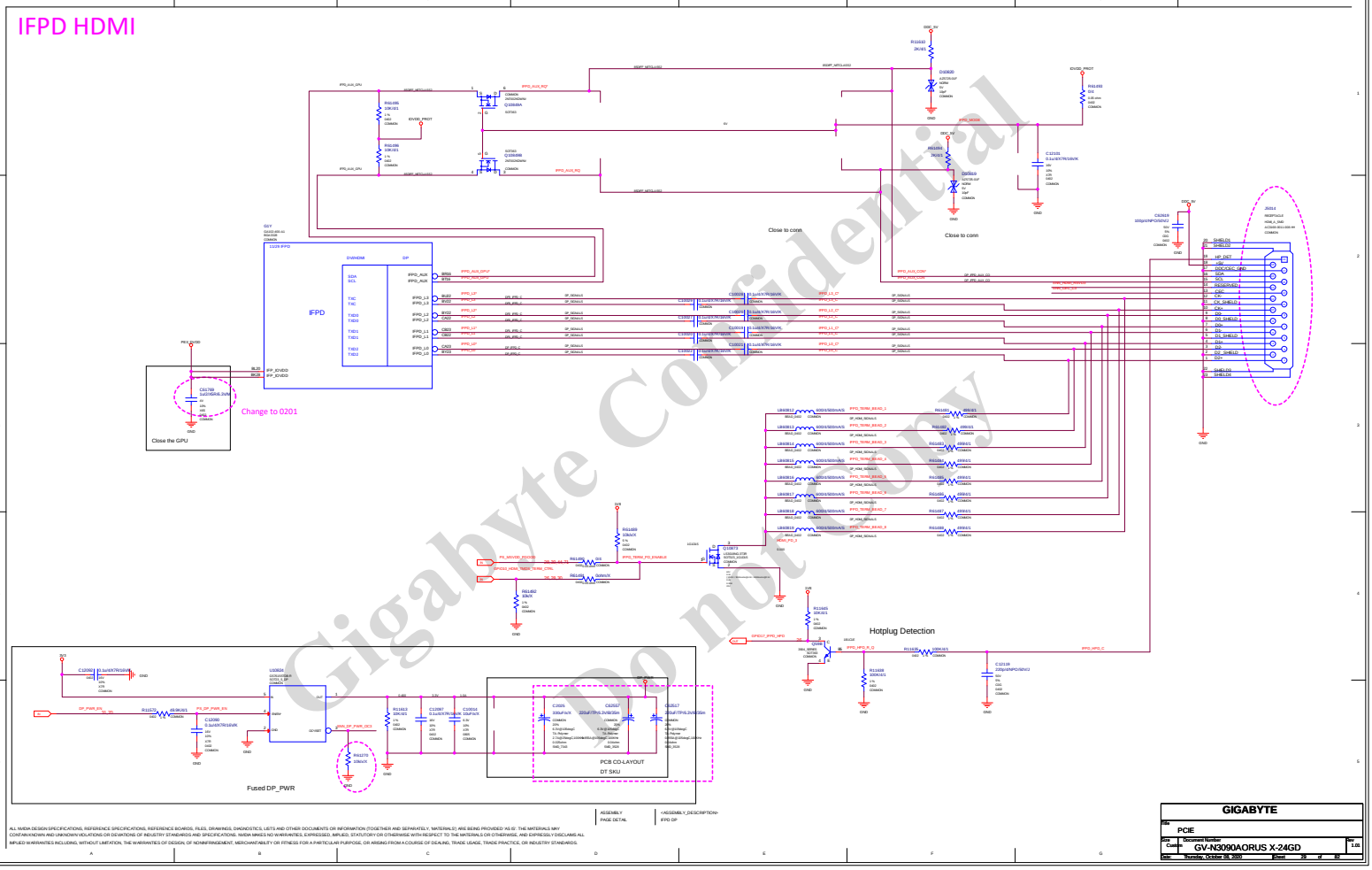

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PAGE DETAIL | IFPD DP

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Title: PCIE		
Size: C	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
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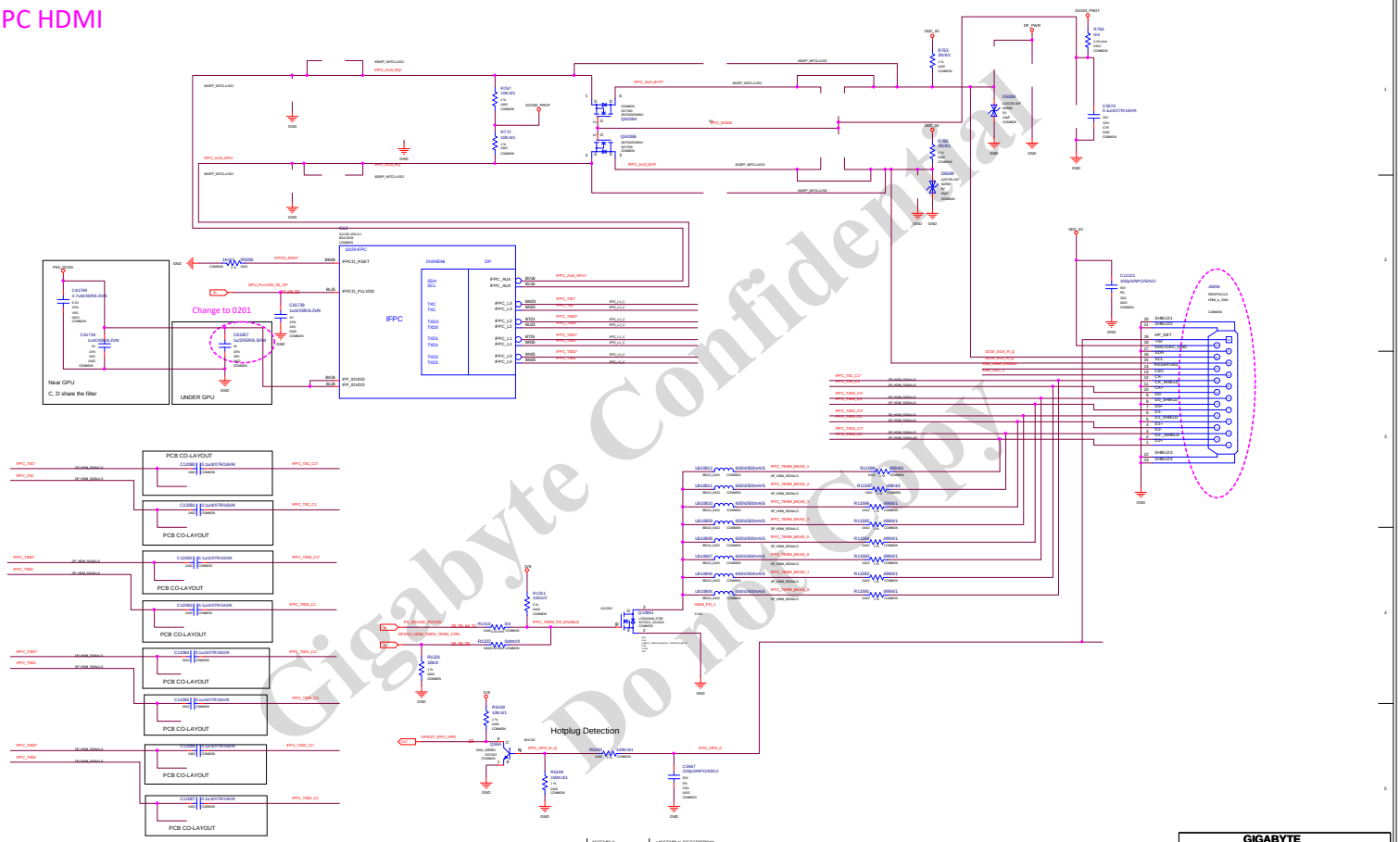
IFPC HDMI



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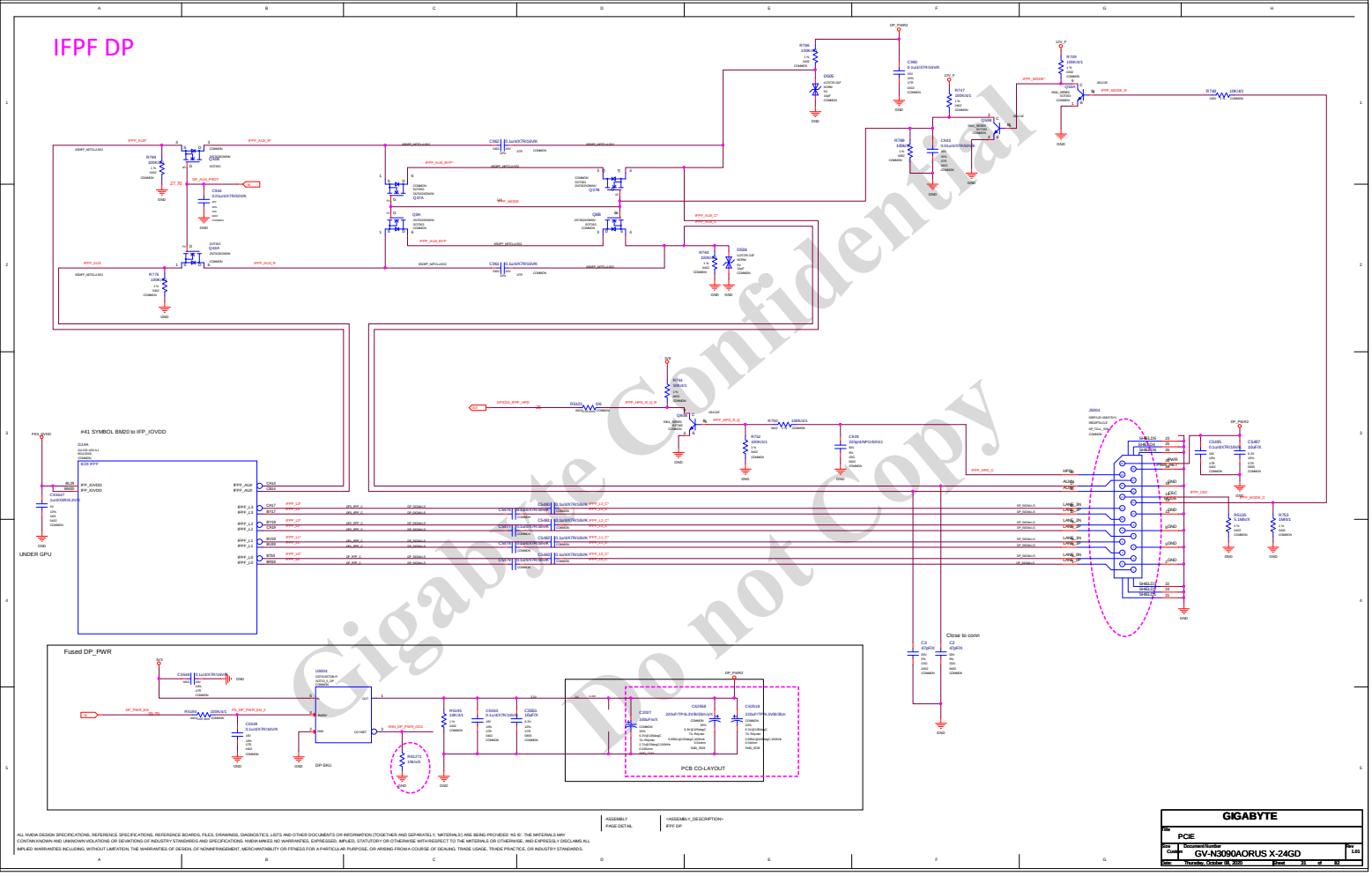

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MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb 19Gbps
L	H	L	00010	RAMCFG TBD
H	L	L	00100	RAMCFG TBD
H	L	H	00101	RAMCFG TBD
H	L	H	00101	RAMCFG MICRON 8Gb 21Gbps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0]_FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

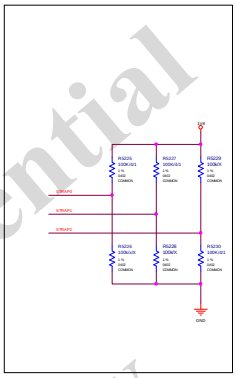
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

GROUP0



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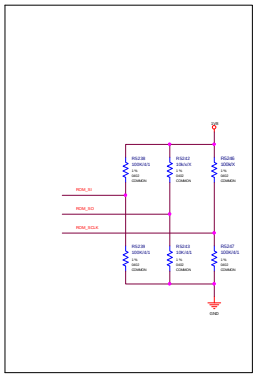

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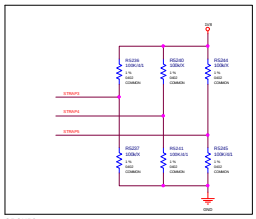

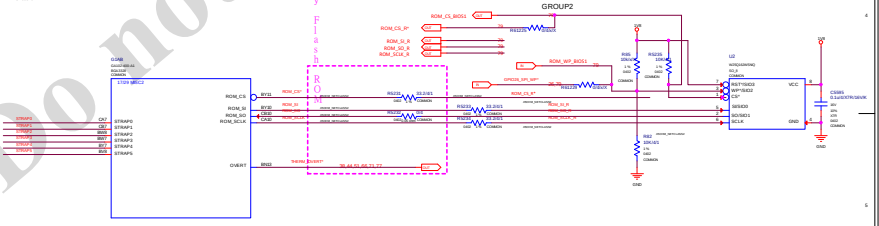

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Modify Flash ROM

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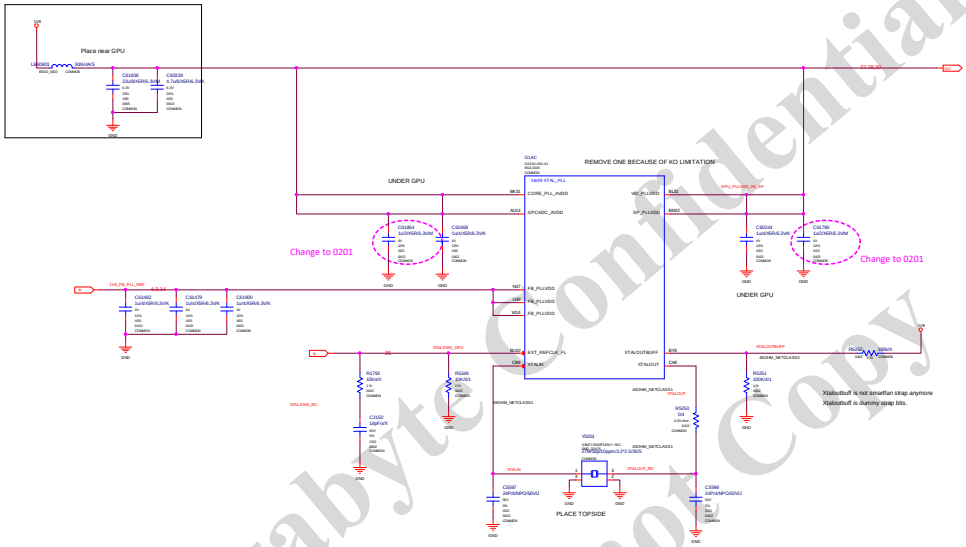
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC_ROM_STRAPS

GIGABYTE			
File: PCIE			
Size:	Document Number:		Rev:
Custom	GV-N3090AORUS X-24GD		1.01
Date: Thursday, October 08, 2020	Sheet 32 of 80		

MISC: XTAL. PLL



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PAGE DETAIL	MISC. XTAL. PLL

GIGABYTE		
Title: PCIE		
Size: C	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
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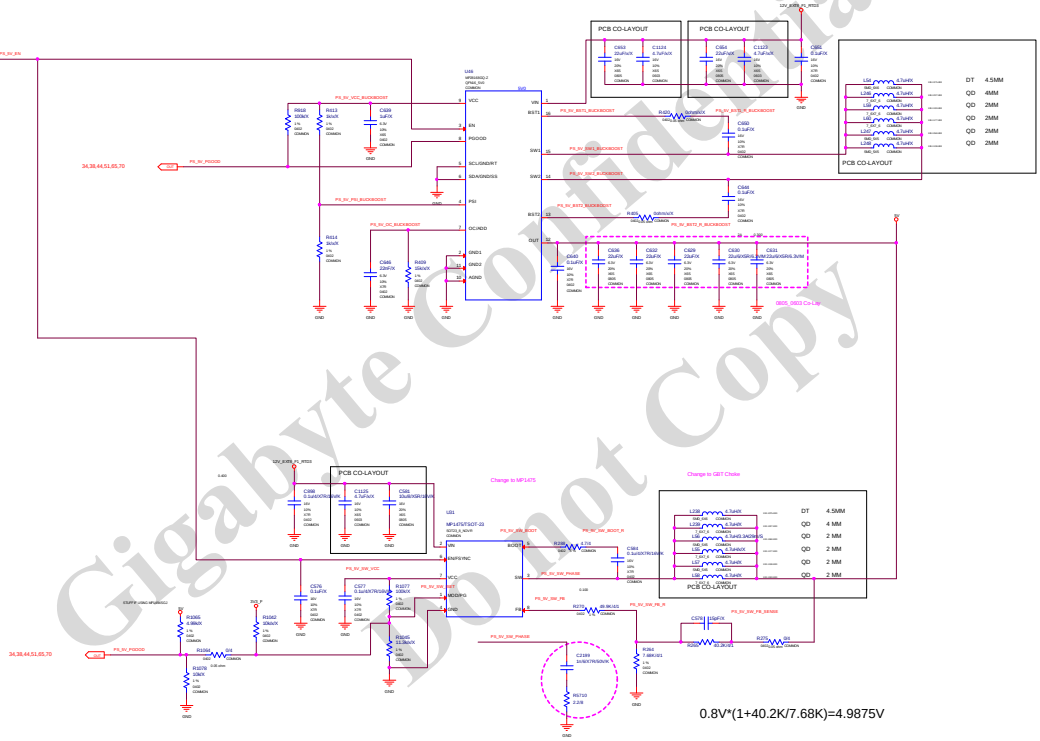
PS: 5V, 5V_BACKUP



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PAGE DETAIL	PS: 5V

Title	PCIE
Size: C	Document Number: GV-N3090AORUS X-24GD
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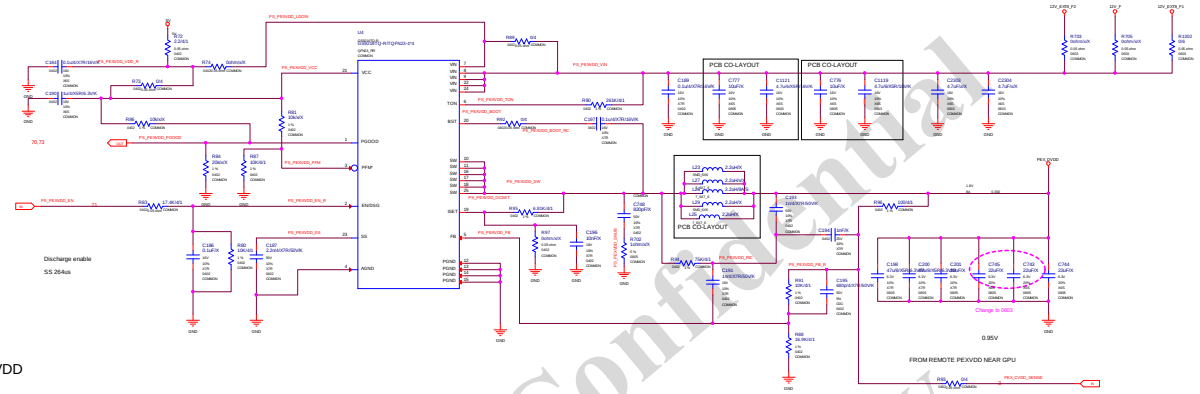
Date: Thursday, October 08, 2020	Sheet 34 of 82

PS: PEX_DVDD 1V8 Rail



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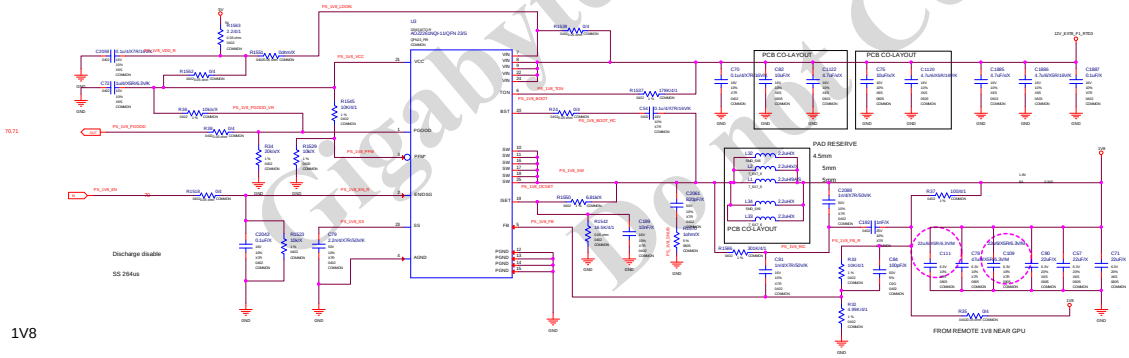

1V8

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PAGE DETAIL	PS: PEX_DVDD and 1V8

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Title	PCIE	
Size: C	Document Number: GV-N3090AORUS X-24GD	Rev: 1.0
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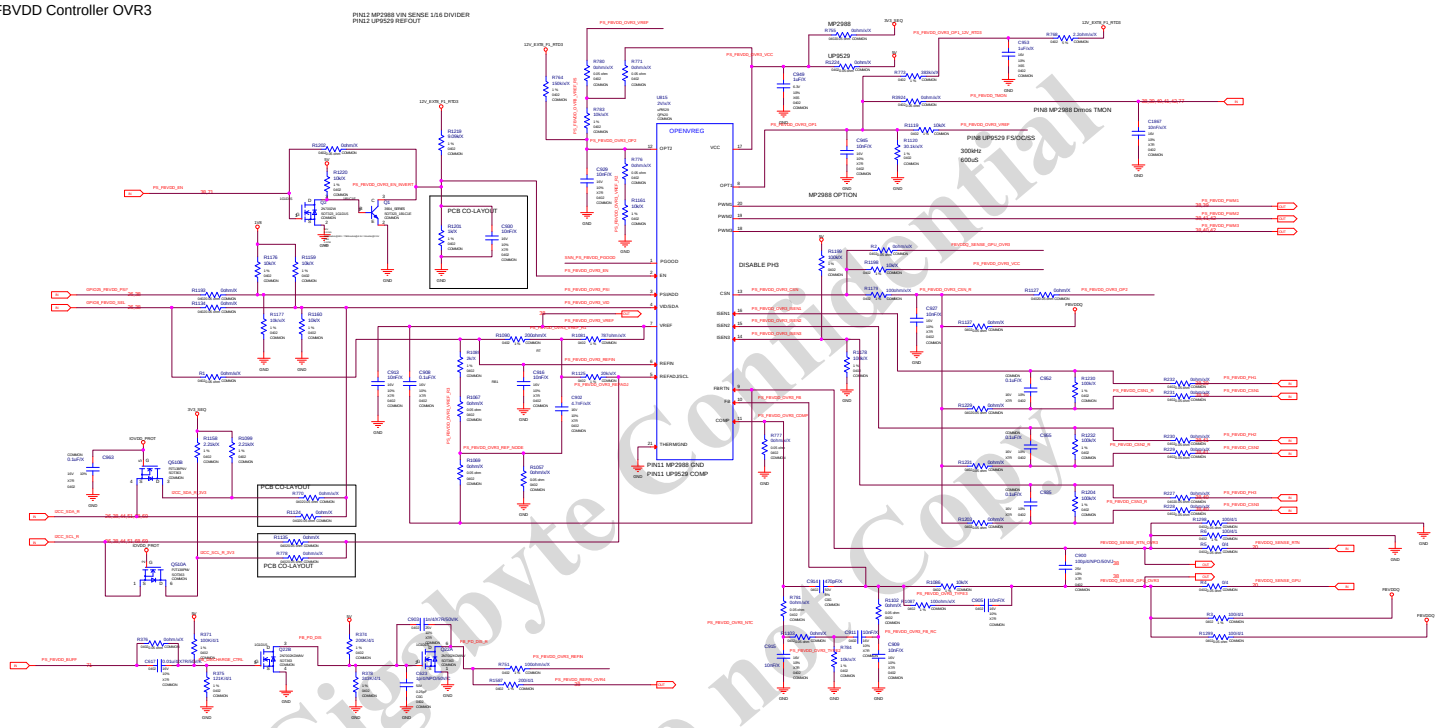
File	PCIE		
Size	Document Number		Rev
Custom	GV-N3090AORUS X-24GD		1.01
Date:	Thursday, October 08, 2020	Sheet 26 of 82	

PS: FBVDD Controller OVR3



FOR DT SKU

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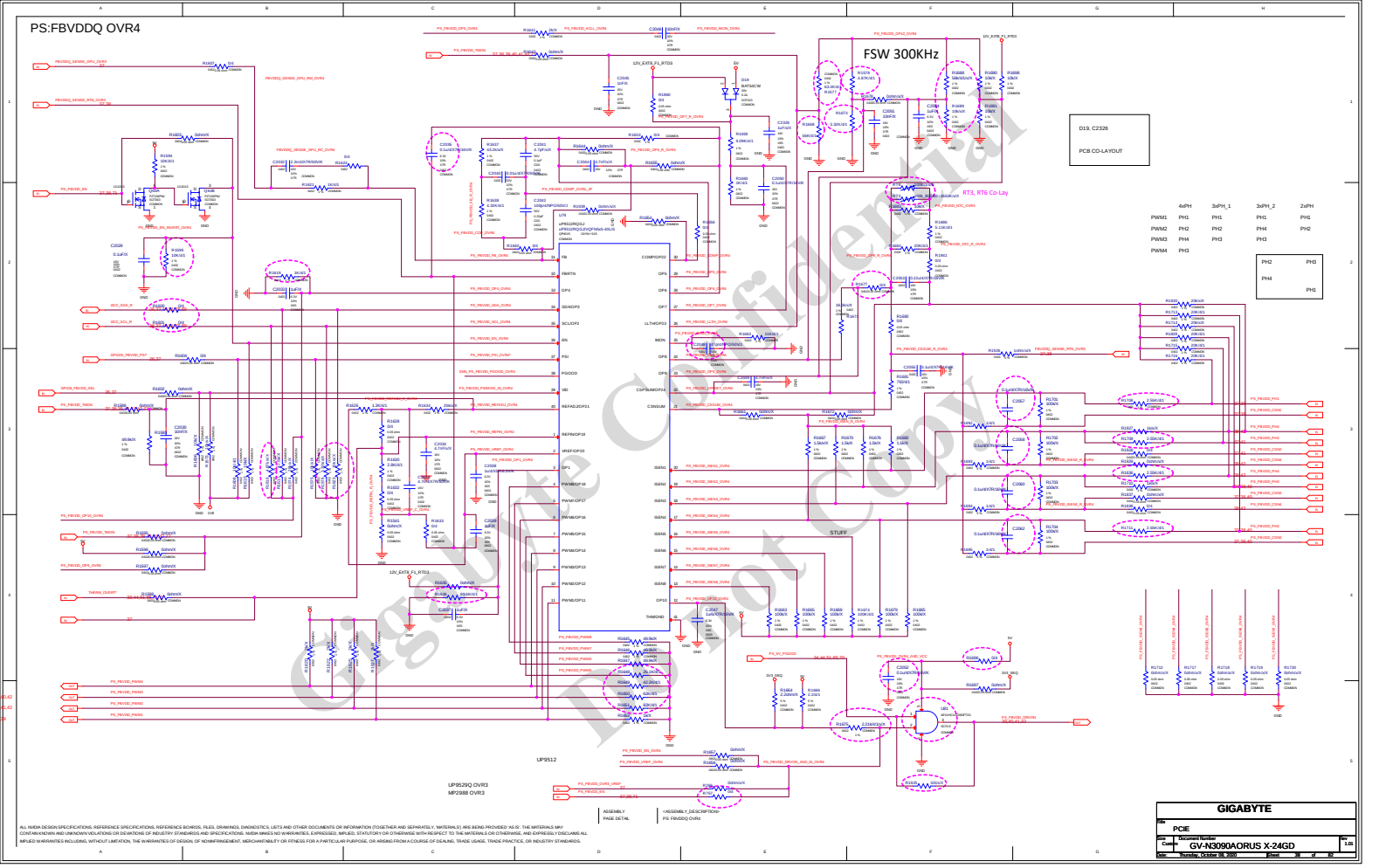
Title	PCIE		
Size	Document Number		Rev
Custom	GV-N3090AORUS X-24GD		1.01
Date:	Thursday, October 08, 2020	Sheet 37 of 82	



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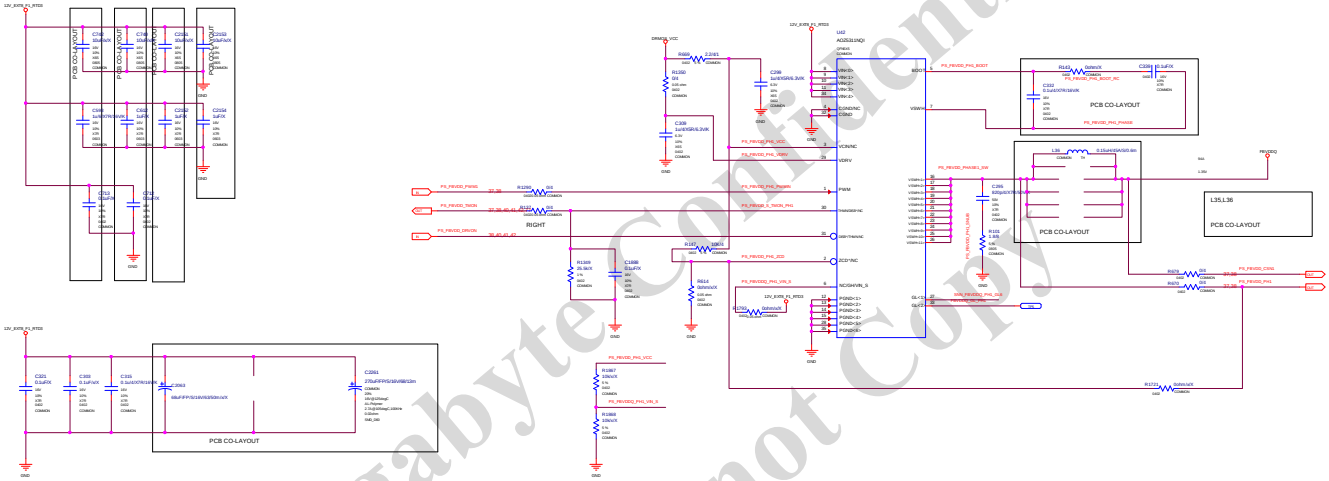
Title	PCIE
Size: C	Document Number: GV-N3090AORUS X-24GD
Rev: 1.01	
Date: Thursday, October 08, 2020	Sheet 38 of 82

PS: FBVDD PH1



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PS: FBVDD PH1

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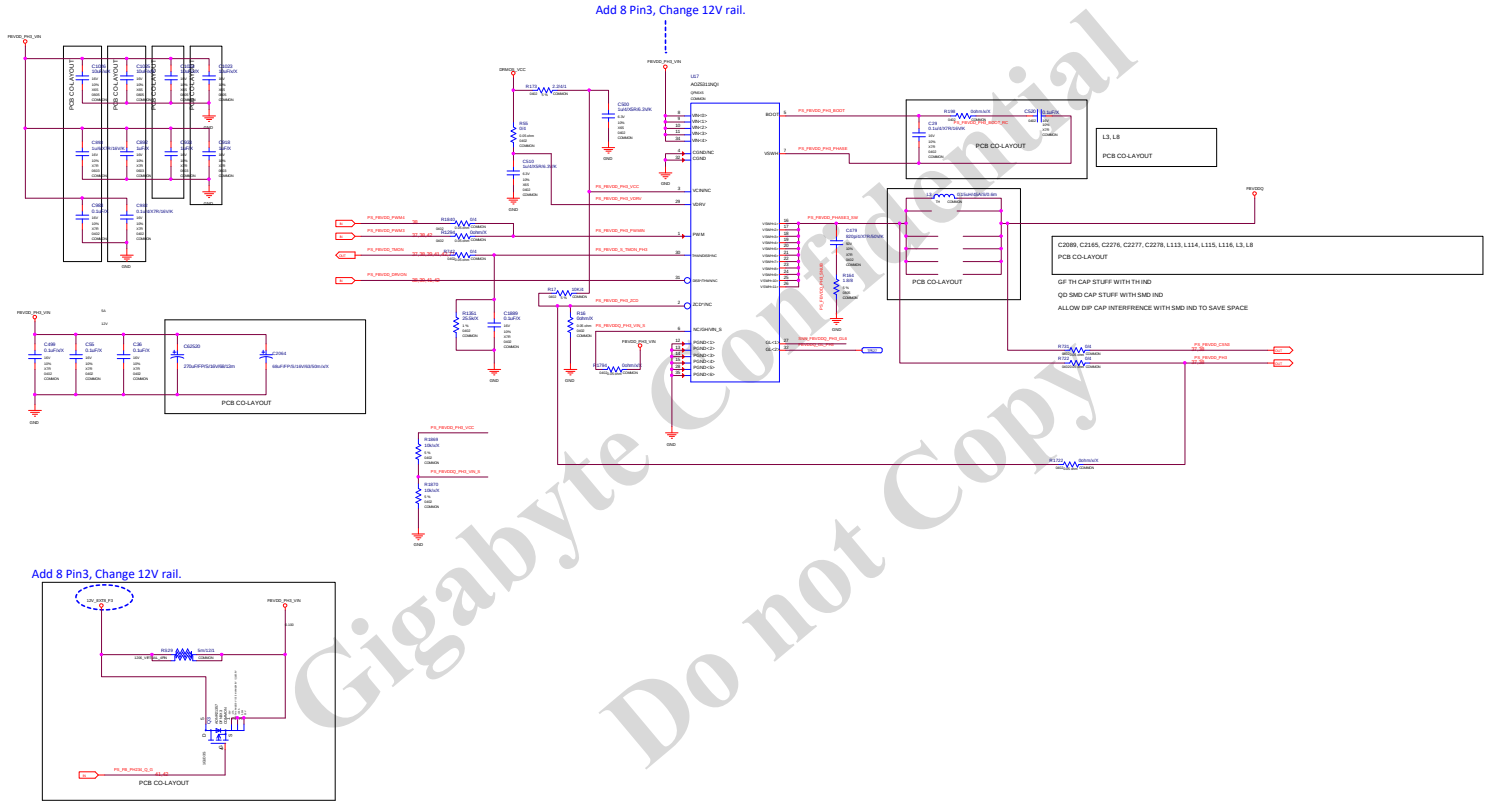
Title: PCIE		
Size: Custom	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
Date: Thursday, October 08, 2020	Sheet 39 of 82	

PS: FBVDD PH3



FBVDD PH3 INPUT ANTI-BACKDRIVE

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PS: FBVDD PH3

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GIGABYTE		
Title: PCIE		
Size: Custom	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
Date: Thursday, October 08, 2020	Sheet 40 of 82	

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PS: FBVDD PH2

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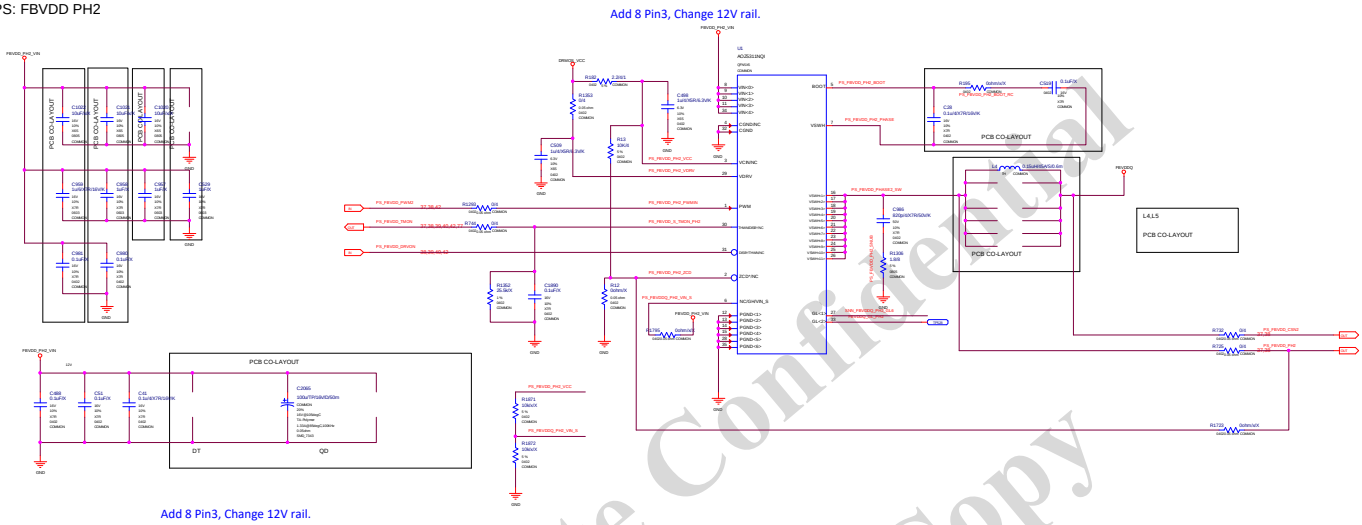

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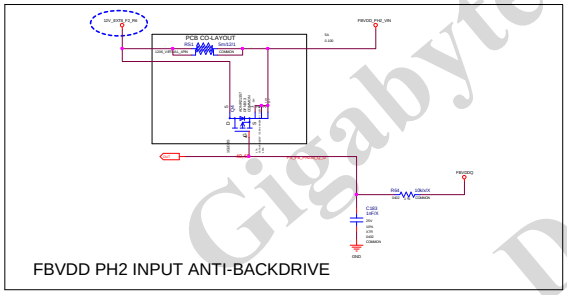

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PAGE DETAIL	PS: FBVDD PH2

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Size: C	Document Number: GV-N3090AORUS X-24GD
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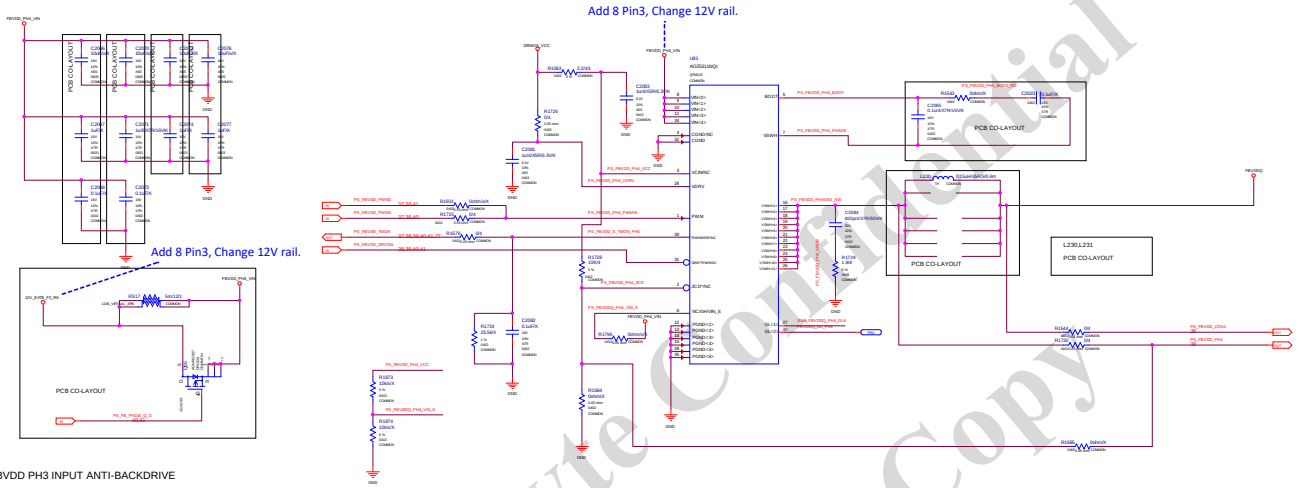
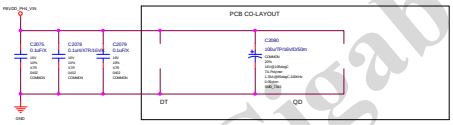
PS: FBVDD PH4



FBVDD PH3 INPUT ANTI-BACKDRIVE



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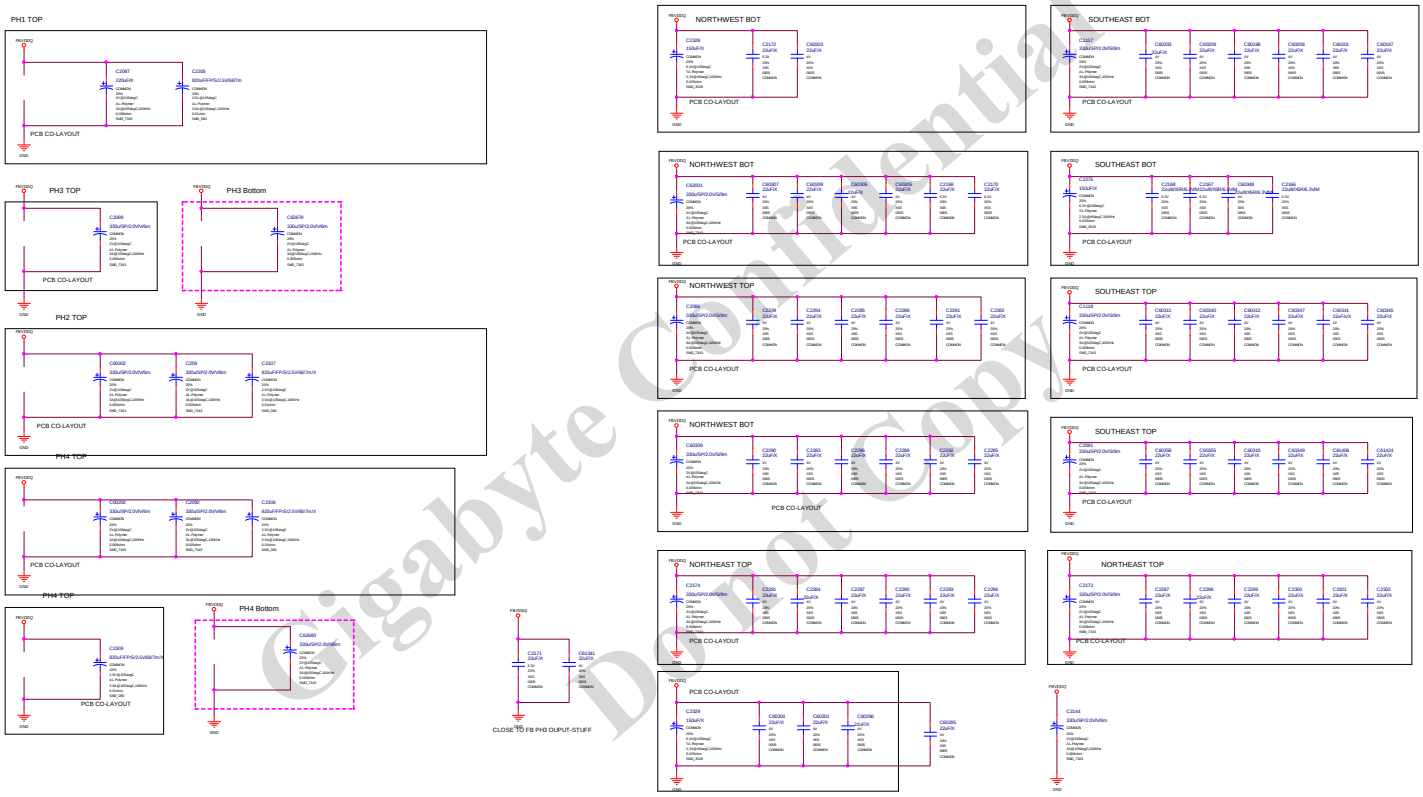
Title	PCIE	
Size: C	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
Date: Thursday, October 08, 2020	Sheet 40 of 82	

PS: FBVDD OUTPUT CAP

REFER TO PCB FOR BOM STUFFING



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PAGE DETAIL	PS: FBVDD OUTPUT CAP

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Size: C	Document Number: GV-N3090AORUS X-24GD
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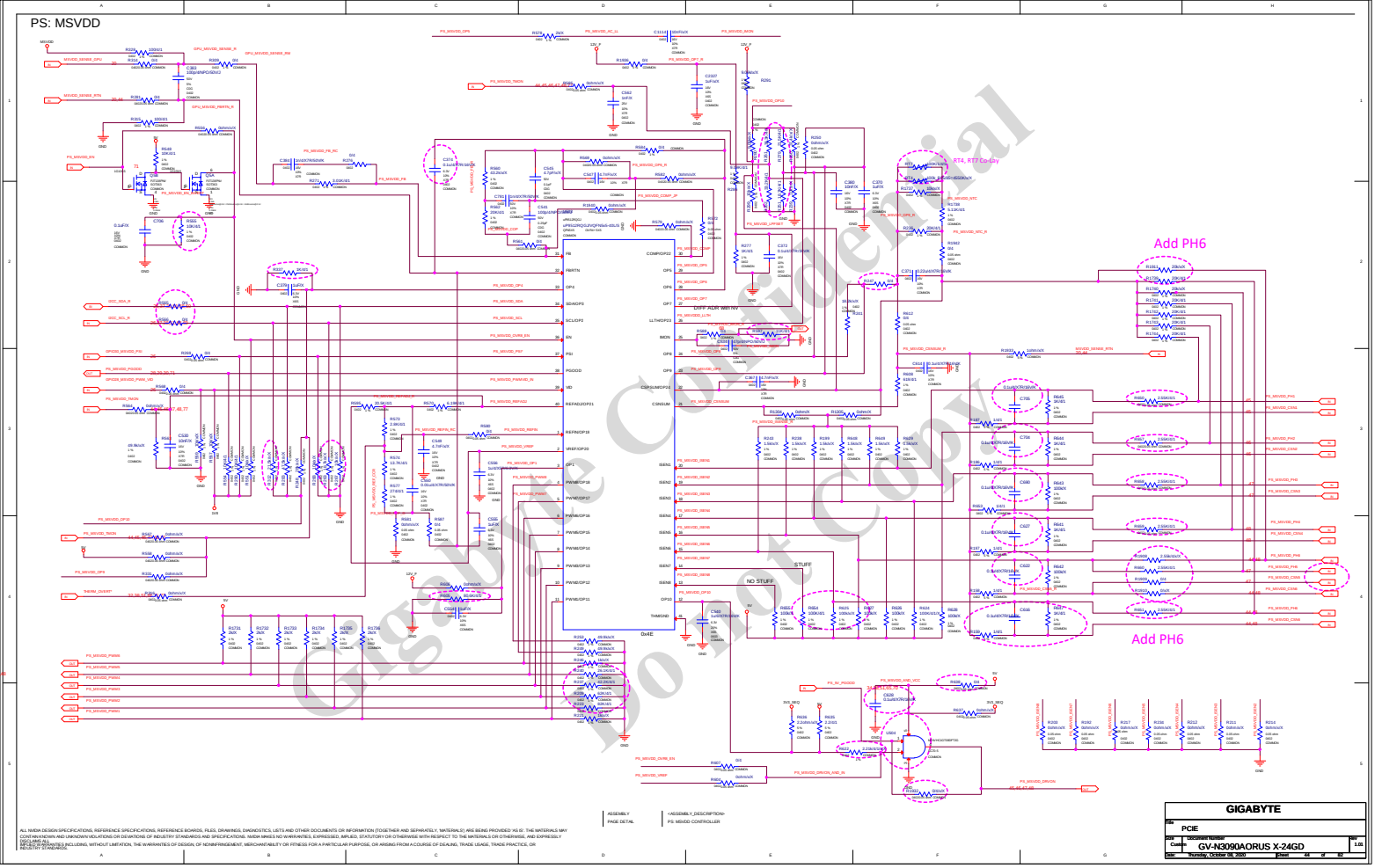
Date: Thursday, October 08, 2020	Sheet 43 of 82



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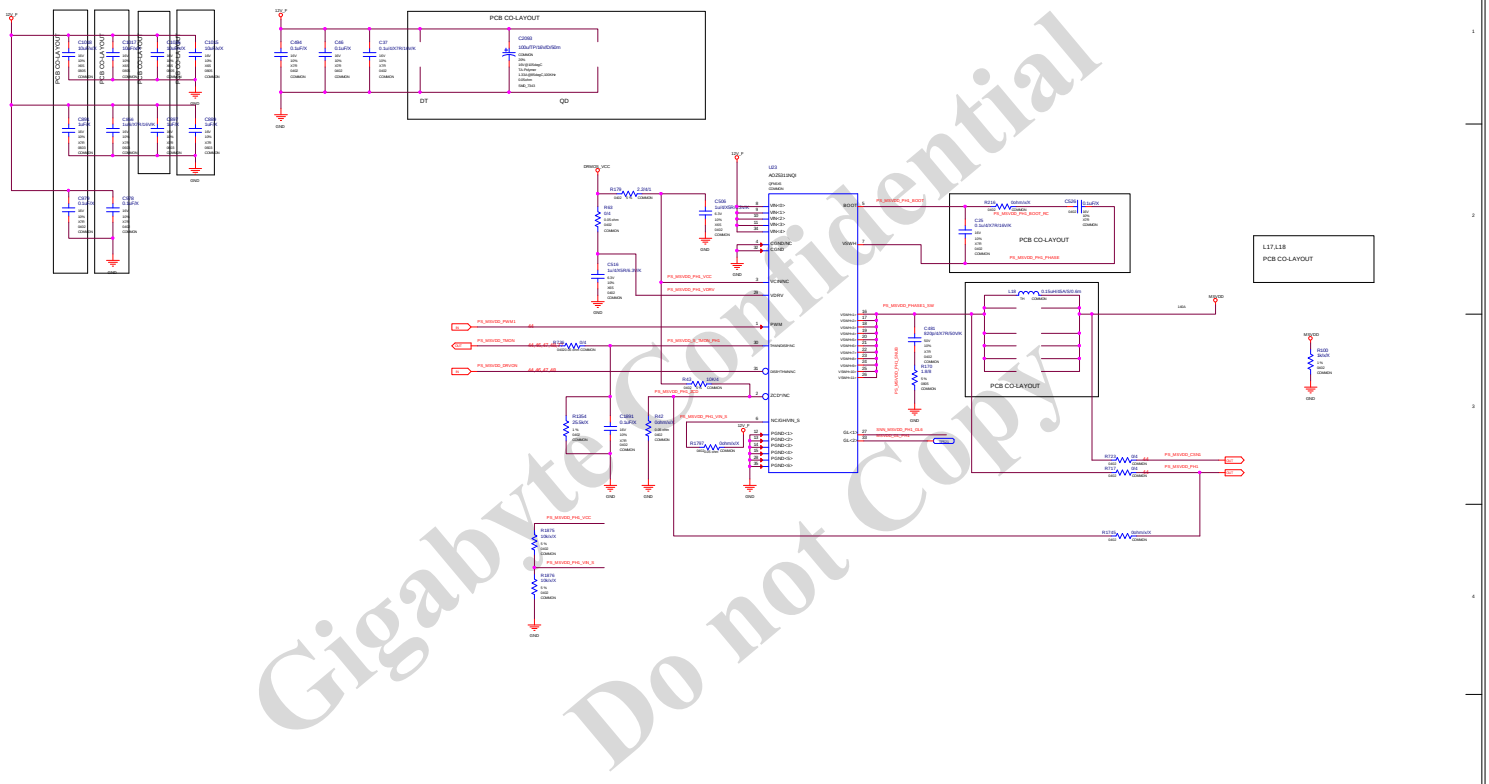
PS: MSVDD Phase 1



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Size: C	Document Number: GV-N3090AORUS X-24GD		Rev: 1.01
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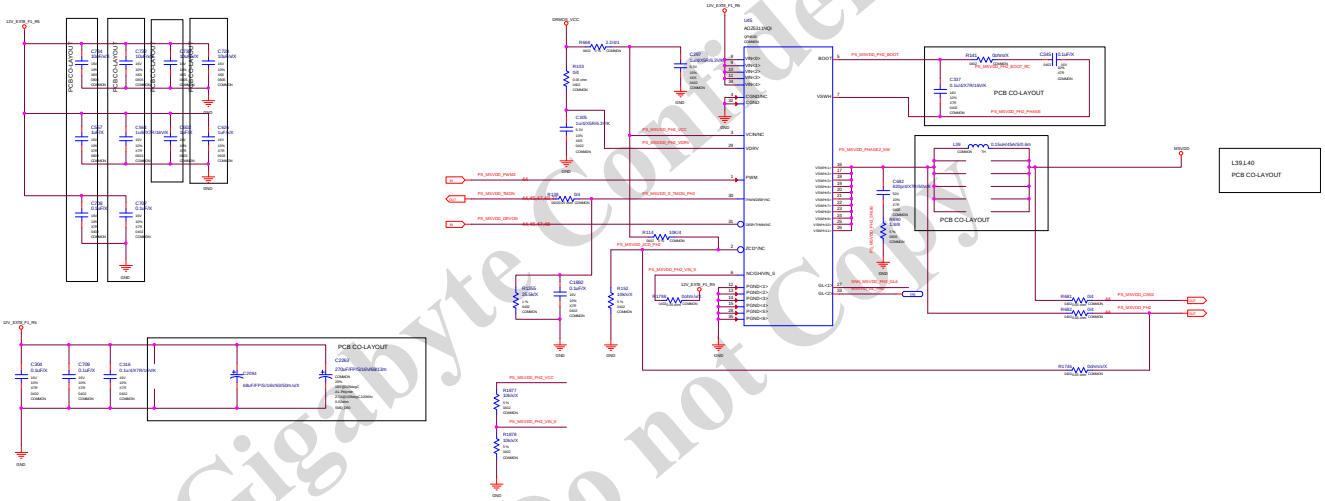
PS: MSVDD PH 2



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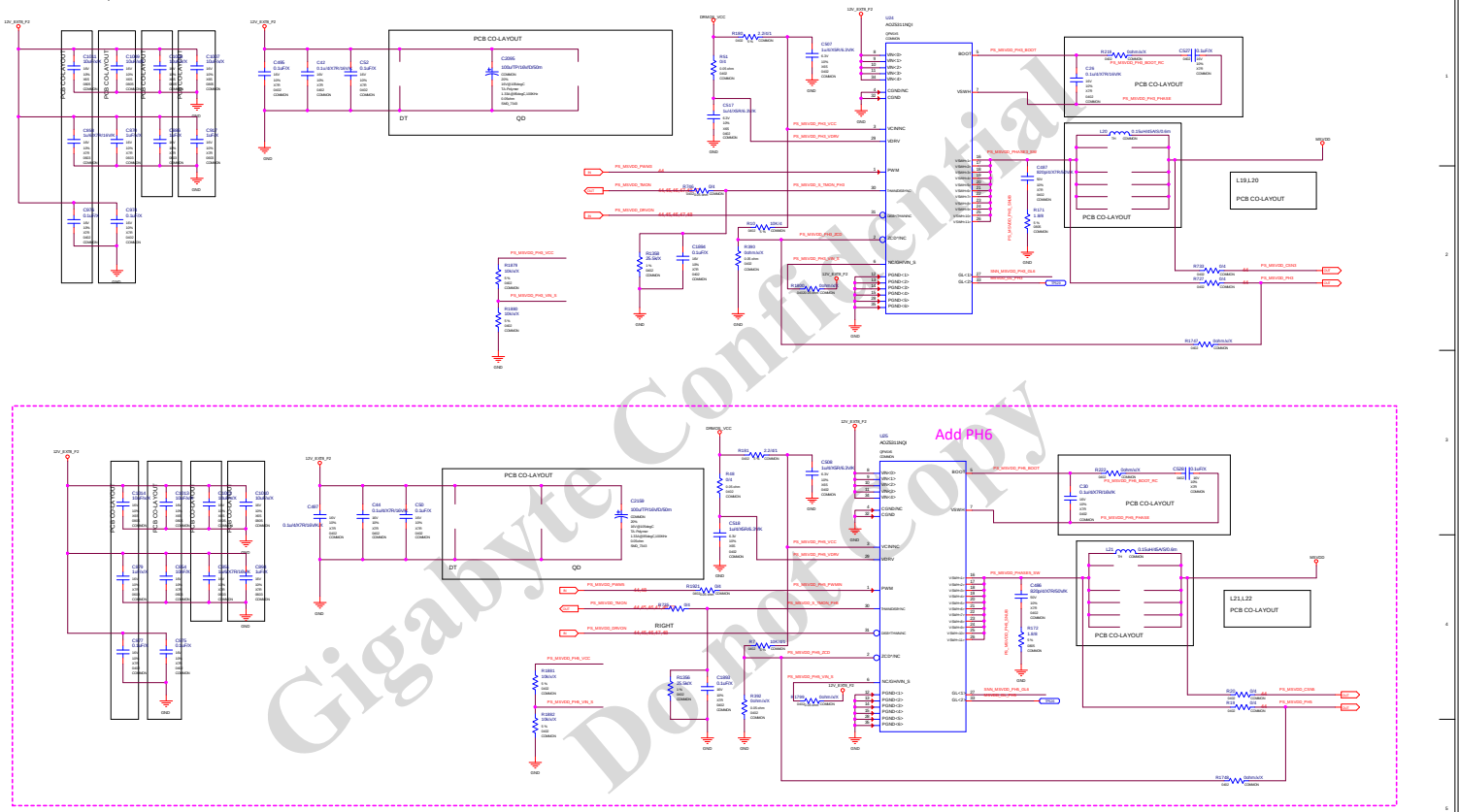
PS:MSVDD Phase 3, 5



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ASSEMBLY
PAGE DETAIL

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PS: MSVDD PH3 and PH6

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GIGABYTE	
Title	PCIE
Size	Document Number: GV-N3090AORUS X-24GD
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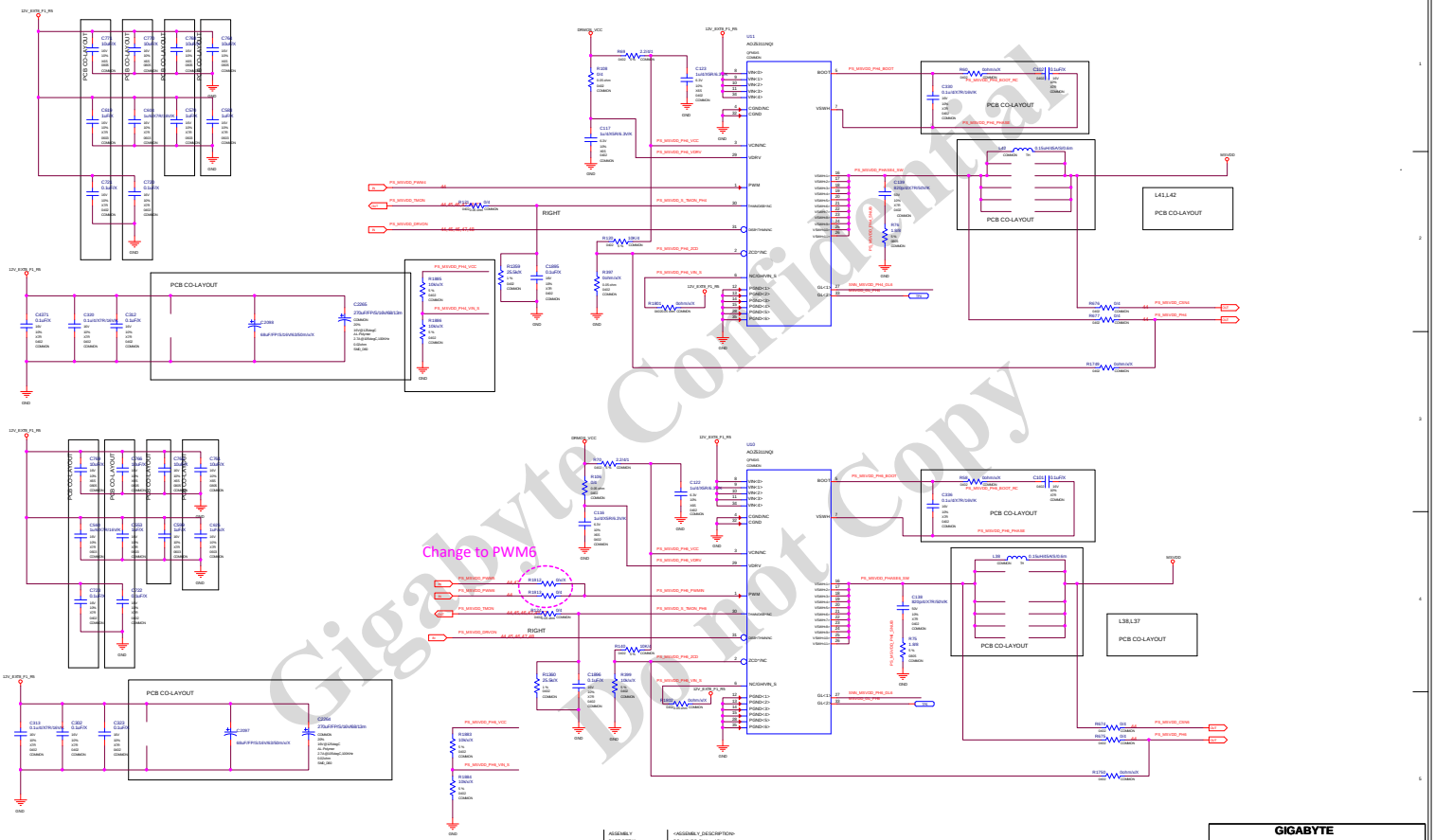
PS: MSVDD PH 4,6



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ASSEMBLY
PAGE DETAIL

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PS: MSVDD PH4 and PH6

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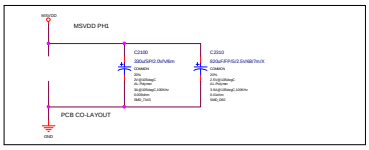
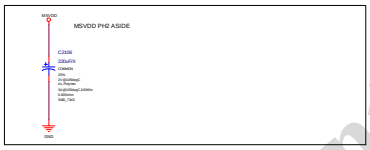
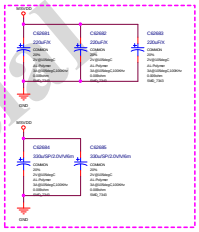
Title	PCIE		
Size	Document Number		Rev
Custom	GV-N3090AORUS X-24GD		1.0E
Date:	Thursday, October 08, 2020	Sheet 48 of 62	

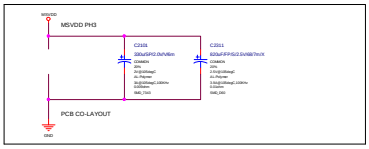
PS:MSVDD OUTPUT CAP (TOP)

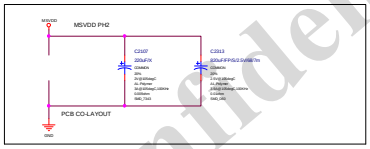
REFER TO PCB FOR BOM STUFFING

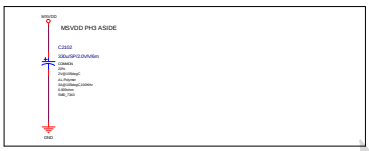


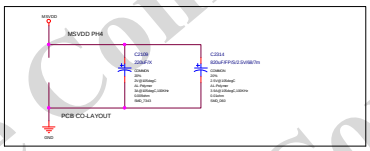


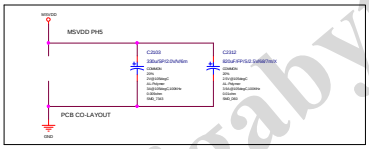


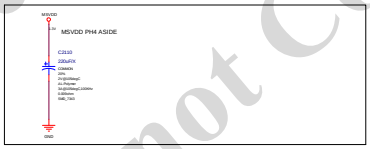


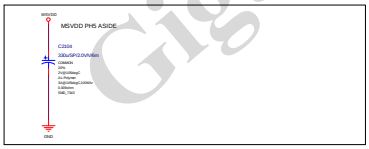


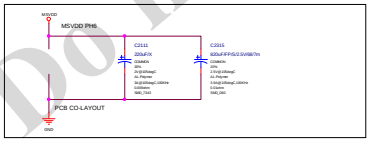


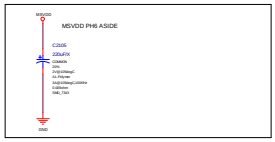












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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: MSVDD OUTPUT CAP(TOP)

GIGABYTE		
Title: PCIE		
Size: C	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
Date: Thursday, October 08, 2020	Sheet 49 of 82	

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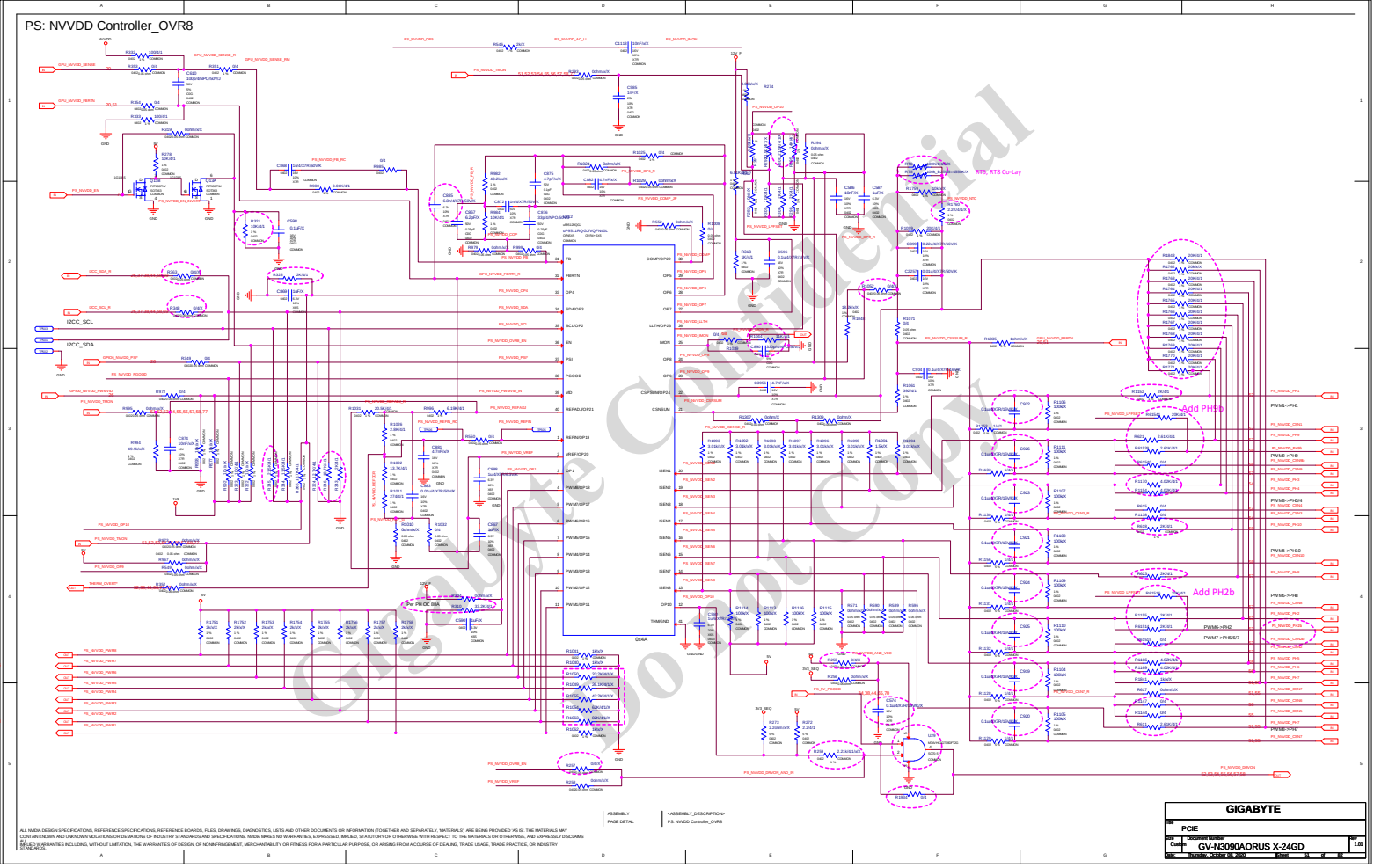
File: PCIE			
Size: D	Document Number: GV-N3090AORUS X-24GD		Rev: 1.01
Date: Thursday, October 08, 2020		Sheet 50 of 52	

PS: NVVDD Controller_OVR8



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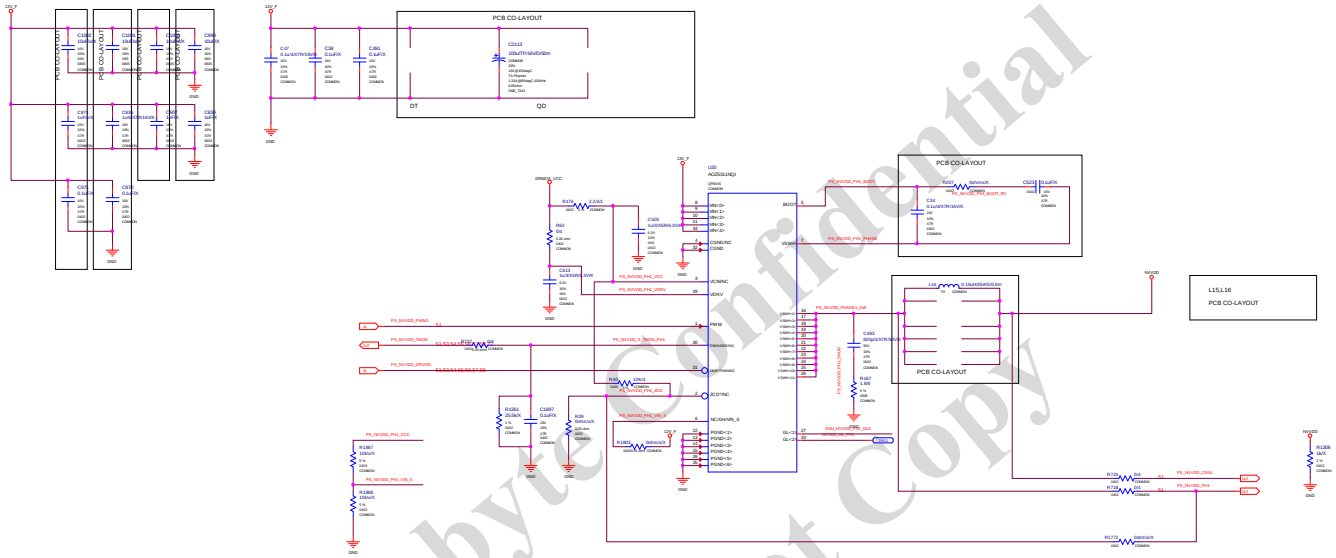
GIGABYTE			
Title	PCIE		
Size	Document Number		Rev
Custom	GV-N3090AORUS X-24GD		1.01
Date:	Thursday, October 08, 2020	Sheet 51 of 82	

PS: NVVDD Phase 1



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PAGE DETAIL	PS: NVVDD PH1 (PWM0)

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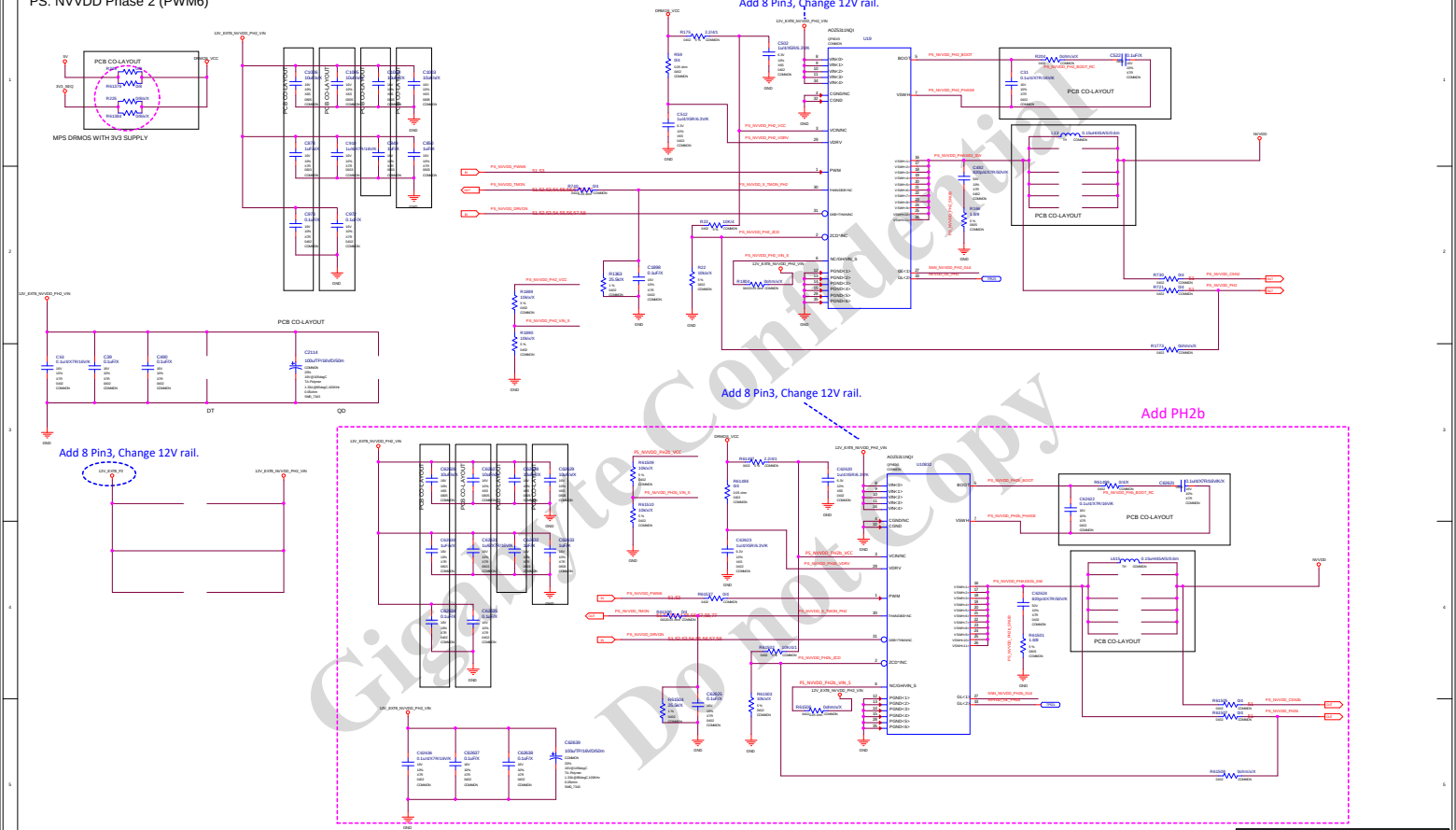
Size: C	Document Number: GV-N3090AORUS X-24GD		Rev: 1.01
Date: Thursday, October 08, 2020		Sheet 82 of 82	

PS: NVVDD Phase 2 (PWM6)

Add 8 Pin3, Change 12V rail.



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD PH2 (PWM6)

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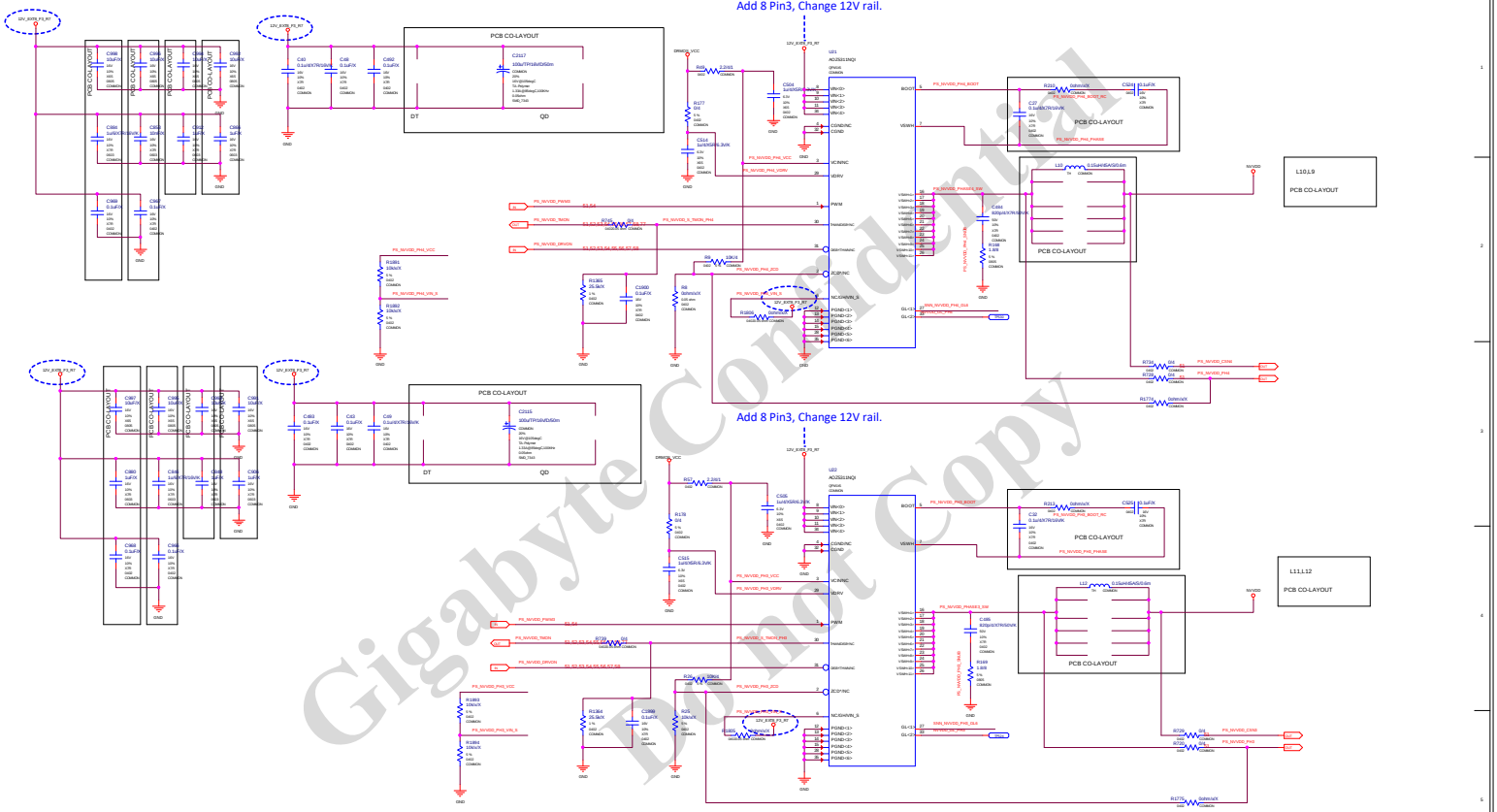
Title	PCIE	
Size: C	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
Date: Thursday, October 08, 2020	Sheet 53 of 82	

PS: NVVDD Phase 3 (PWM3), PHASE4 (PWM3)

Add 8 Pin3, Change 12V rail.



Add 8 Pin3, Change 12V rail.

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD PH3 (PWM3) and PH4 (PWM3)

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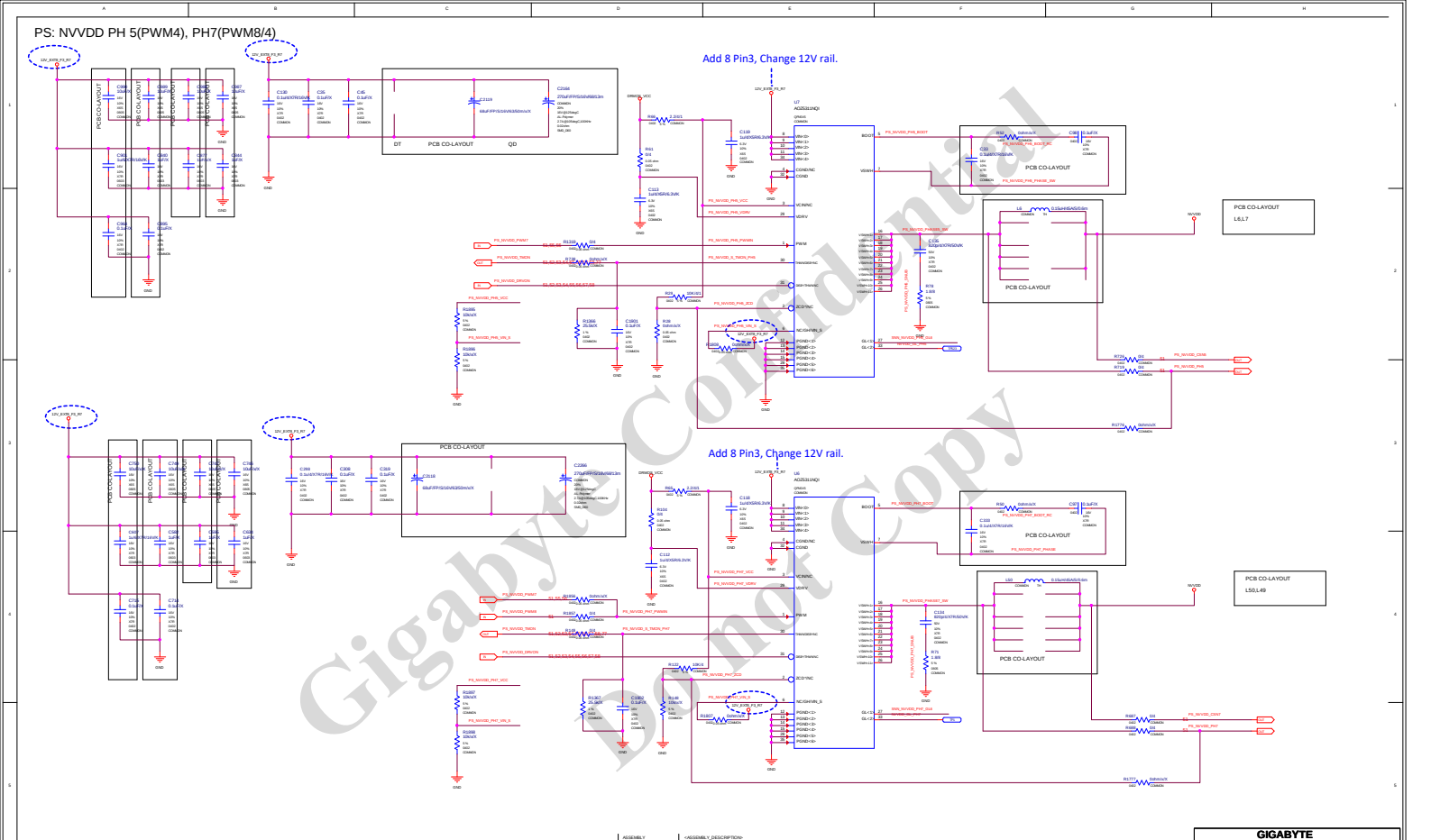
Title: PCIE		
Size: Custom	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
Date: Thursday, October 08, 2020	Sheet 64 of 82	



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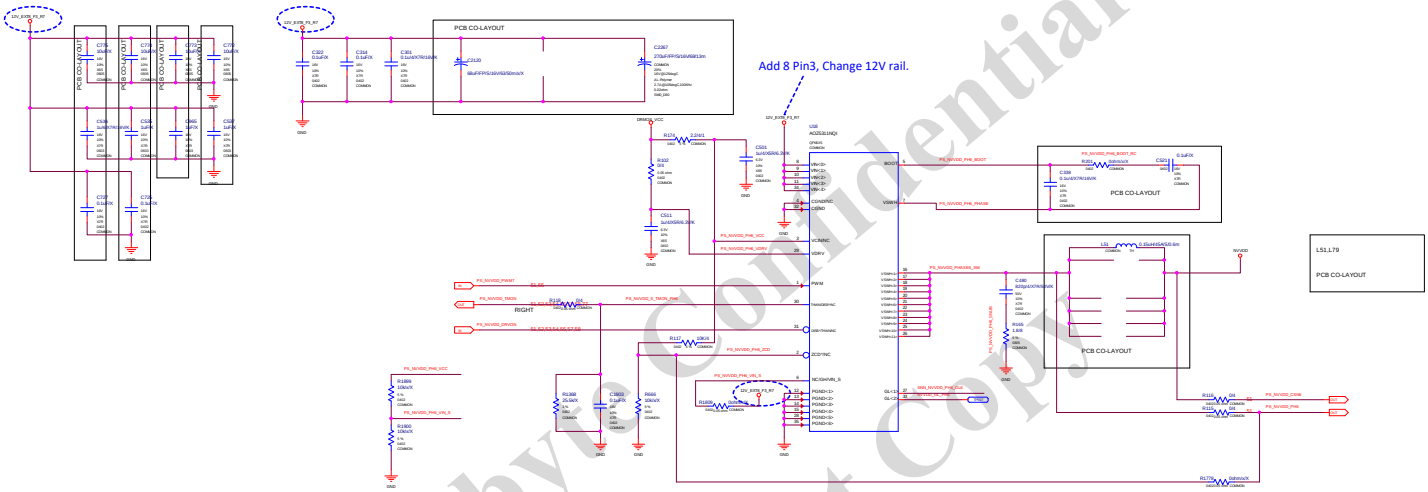
ASSEMBLY
PAGE DETAIL

<ASSEMBLY_DESCRIPTION>
PS: NVVDD PH5 (PWM4) and PH7 (PWM8)

GIGABYTE			
Title	PCIE		
Size	Document Number		Rev
Custom	GV-N3090AORUS X-24GD		1.01
Date:	Thursday, October 08, 2020	Sheet 55 of 82	

PS: NVVDD Phase 6(PWM4)



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD PH6 (PWM7)

GIGABYTE			
Title: PCIE			
Size: C	Document Number: GV-N3090AORUS X-24GD		Rev: 1.01
Date: Thursday, October 08, 2020	Sheet 56 of 82		

PS: NVVDD PH 8 (PWM5), PH 9(PWM2)

Add 8 Pin3, Change 12V rail.

Add 8 Pin3, Change 12V rail.

Add 8 Pin3, Change 12V rail.

Add 8 Pin3, Change 12V rail.

Add 8 Pin3, Change 12V rail.

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PAGE DETAIL	PS: NVVDD PH8(PWM5) and PH9(PWM2)

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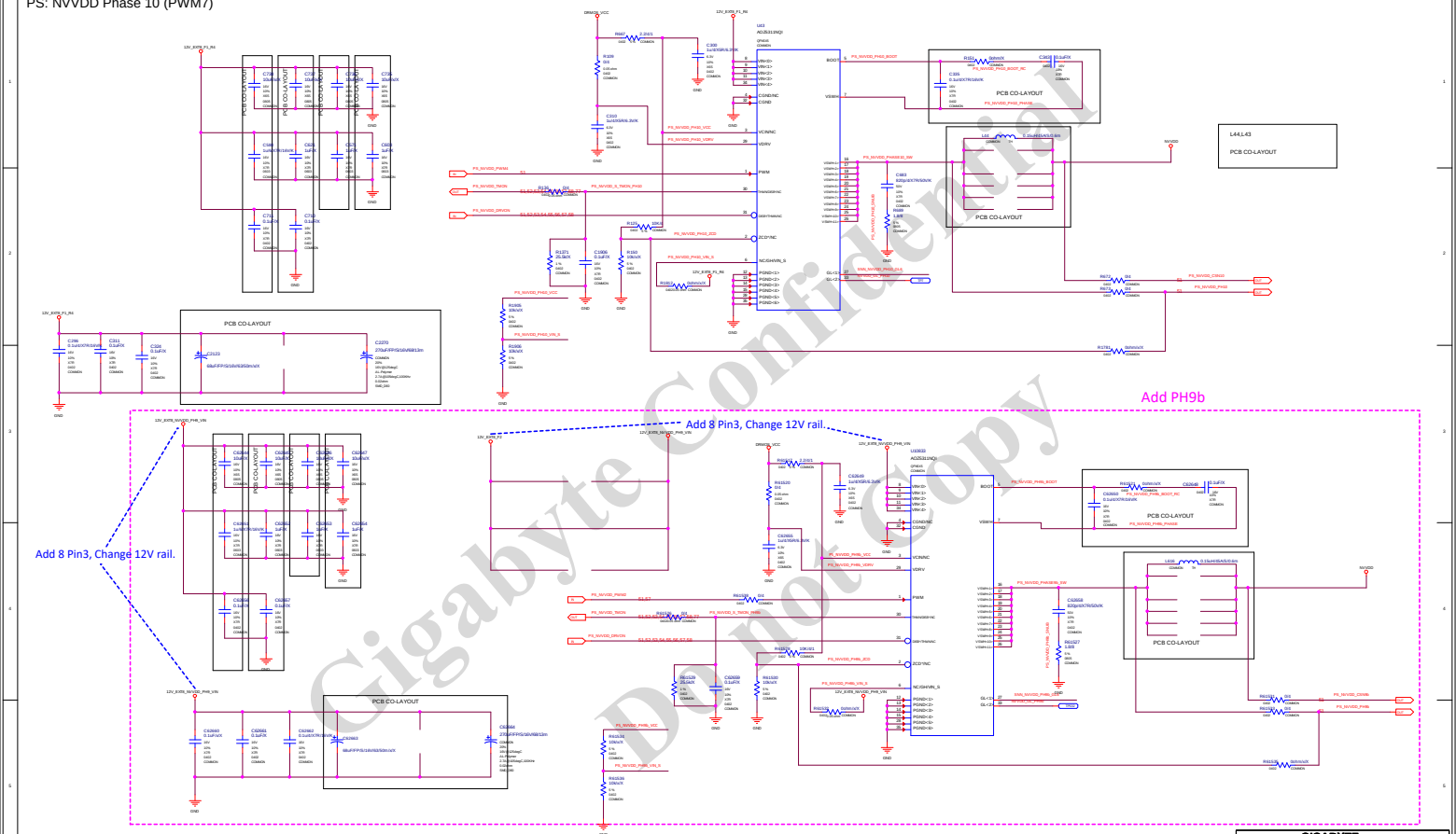
File	PCIE	
Size: C	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
Date: Thursday, October 08, 2020	Sheet 52 of 82	

PS: NVVDD Phase 10 (PWM7)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PCB CO-LAYOUT
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File: PCIE		
Size: Document Number		Rev: 1.01
Custom: GV-N3090AORUS X-24GD		
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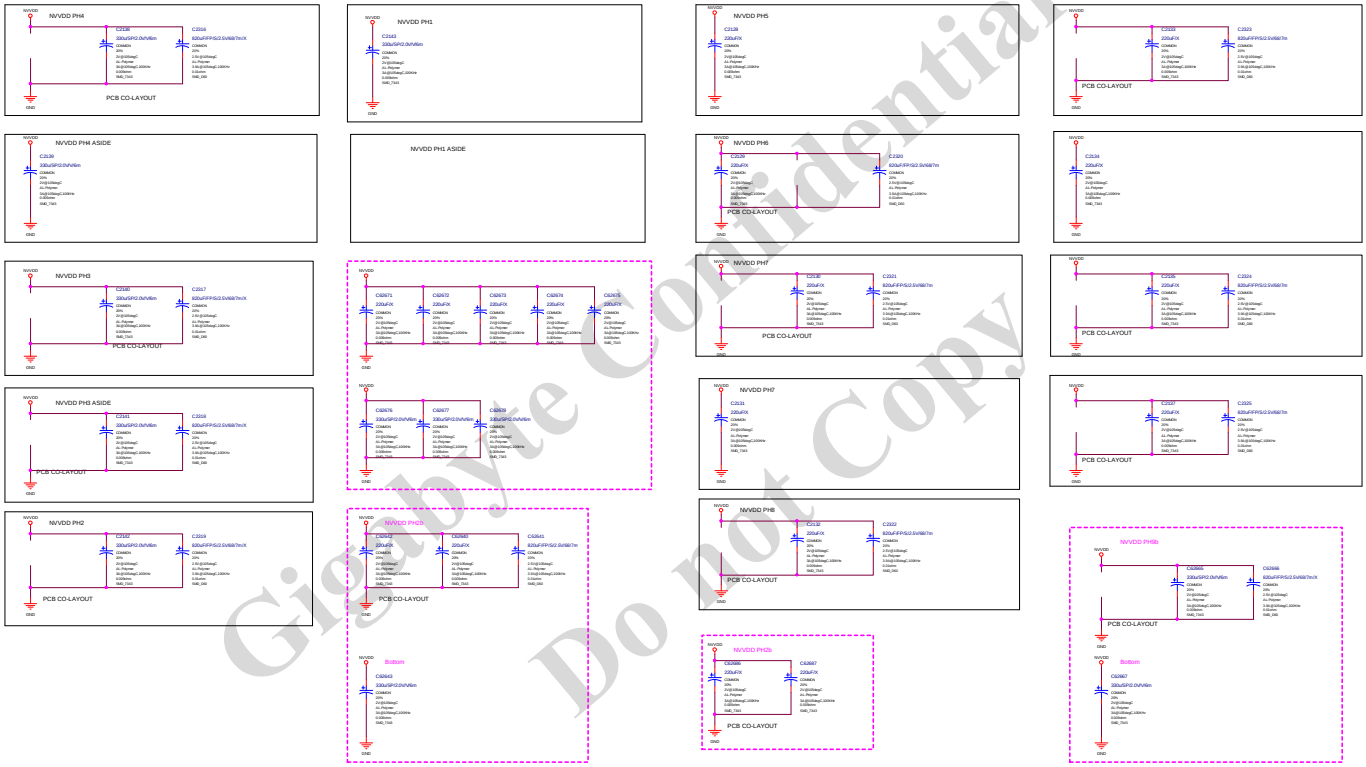
GIGABYTE			
Title	PCIE		
Size	Document Number		Rev
Custom	GV-N3090AORUS X-24GD		1.01
Date:	Thursday, October 08, 2020	Sheet 60 of 82	

PS: NVVDD OUTPUT CAP(TOP)

REFER TO PCB FOR BOM STUFFING



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD OUTPUT CAP(TOP)

GIGABYTE			
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Size: C	Document Number: GV-N3090AORUS X-24GD		Rev: 1.01
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File: PCIE			
Title: Document Number			Rev:
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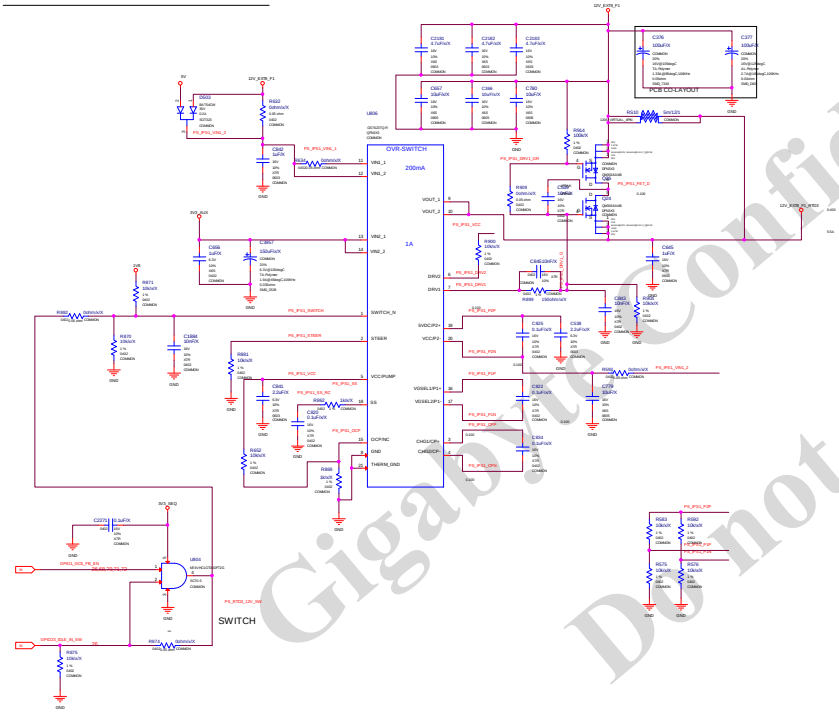
PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO23	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUT SWITCH RTD3

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Title: PCIE		
Size: C	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
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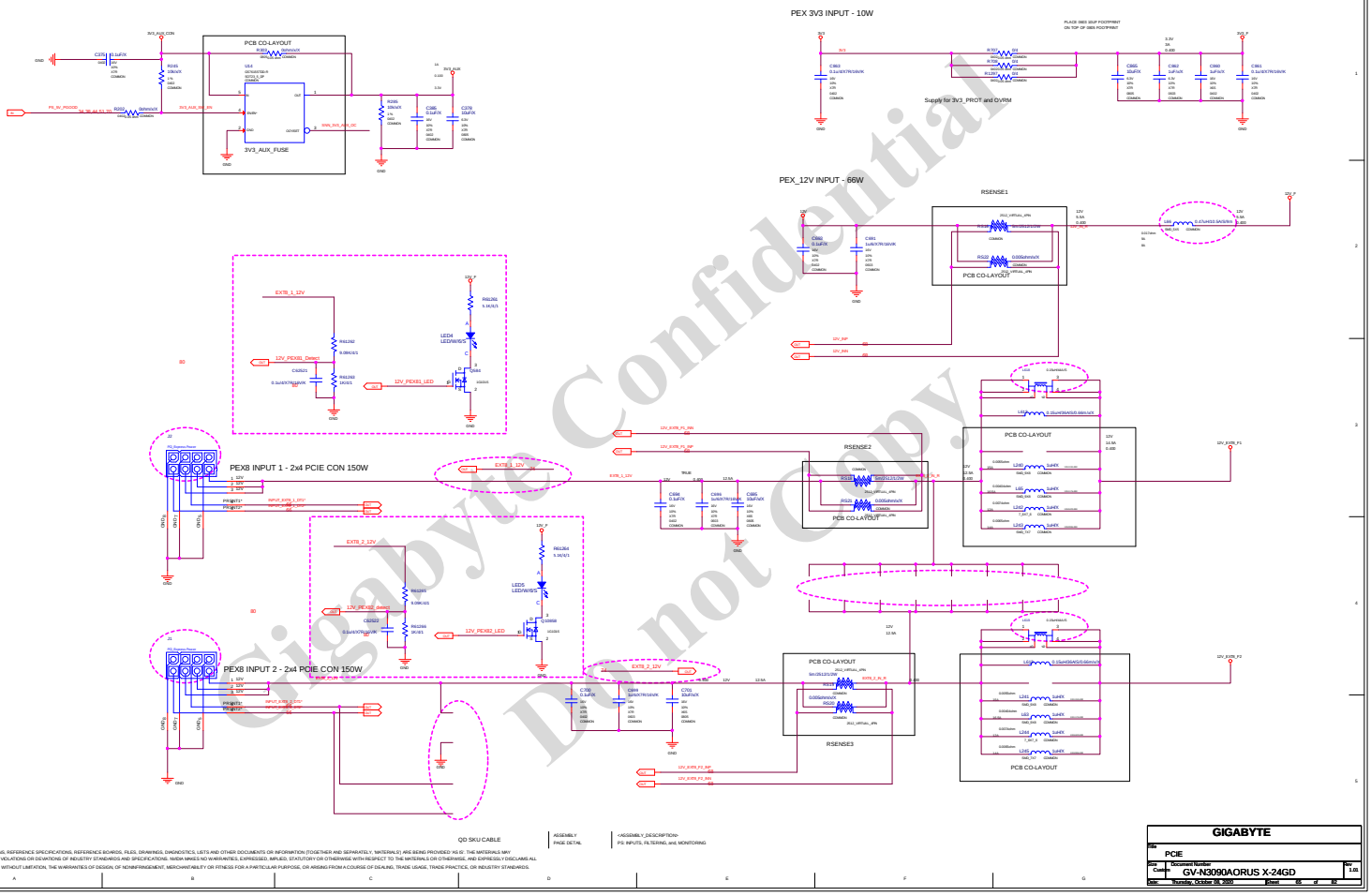
Size: D	Document Number: GV-N3090AORUS X-24GD		Rev: 1.01
Date: Thursday, October 08, 2020		Sheet 64 of 82	

PS: Inputs, Filtering, and Monitoring



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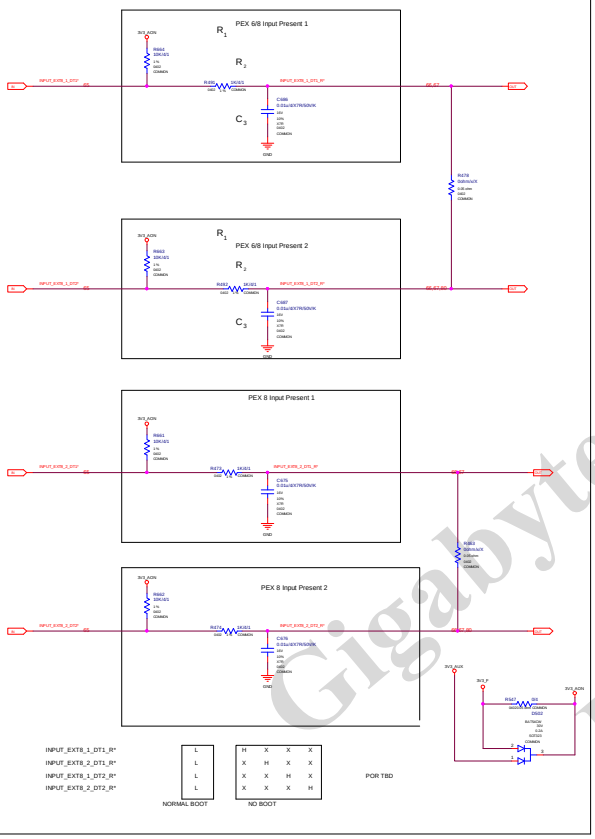
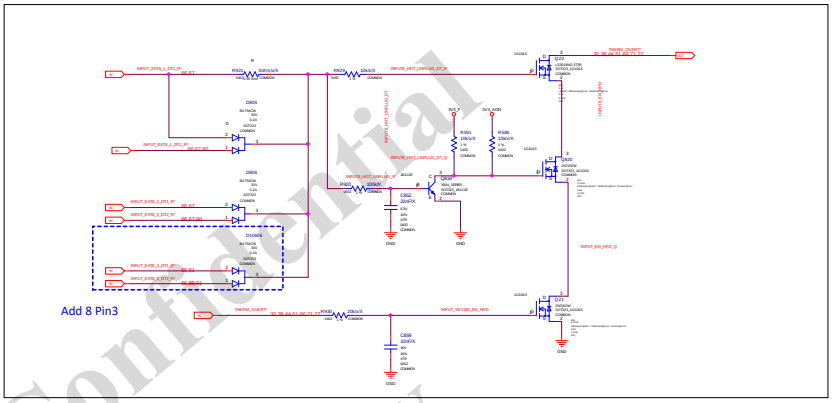
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUTS, FILTERING, and MONITORING

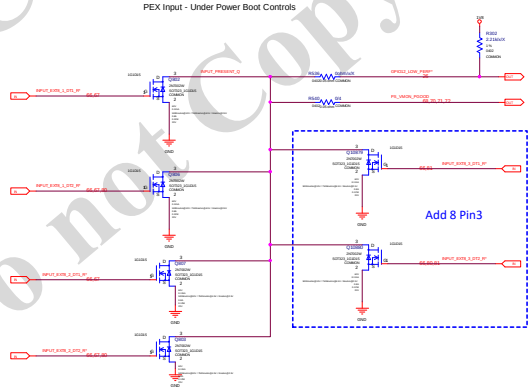
GIGABYTE

Title	PCIE	
Size: C	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
Date: Thursday, October 08, 2020	Sheet 65 of 82	

PS: 12V Current Steering & Hot Unplug Detect







A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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ASSEMBLY
PAGE DETAIL

<ASSEMBLY_DESCRIPTION>
PS: HOT UNPLUG

Title	PCIE
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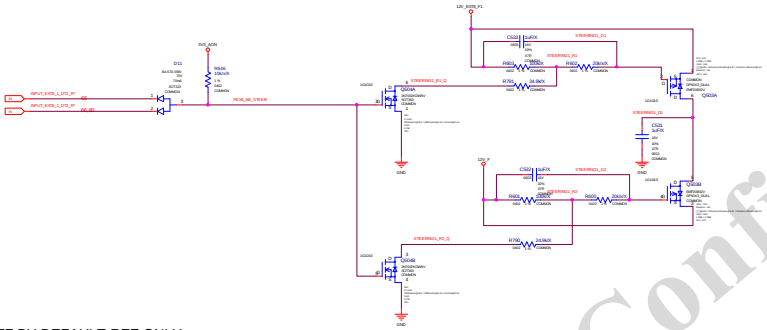
GIGABYTE

PS: Discrete Steering

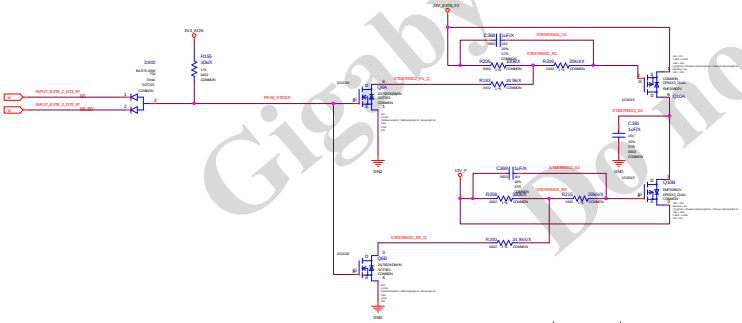
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1



NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V_EXT8_F2



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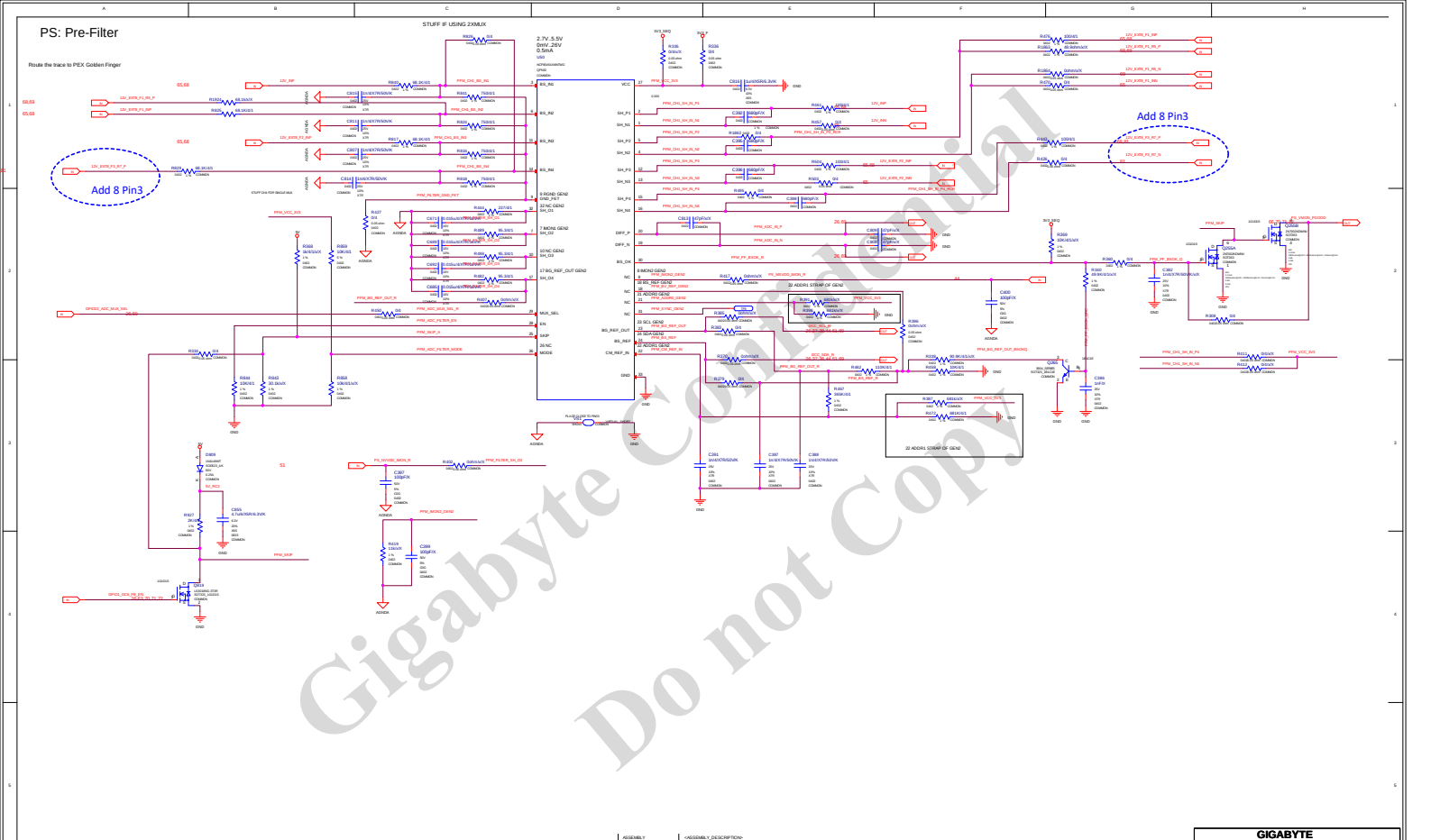
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Discrete Power Steering

GIGABYTE			
File: PCIE			
Title: Discrete Power Steering			Rev: 1.01
Custom: GV-N3090AORUS X-24GD			
Date: Thursday, October 08, 2020	Sheet 67 of 82		



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ASSEMBLY
PAGE DETAIL

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PS: PREFILTER

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GIGABYTE			
Title: PCIE			
Size: C	Document Number: GV-N3090AORUS X-24GD		Rev: 1.01
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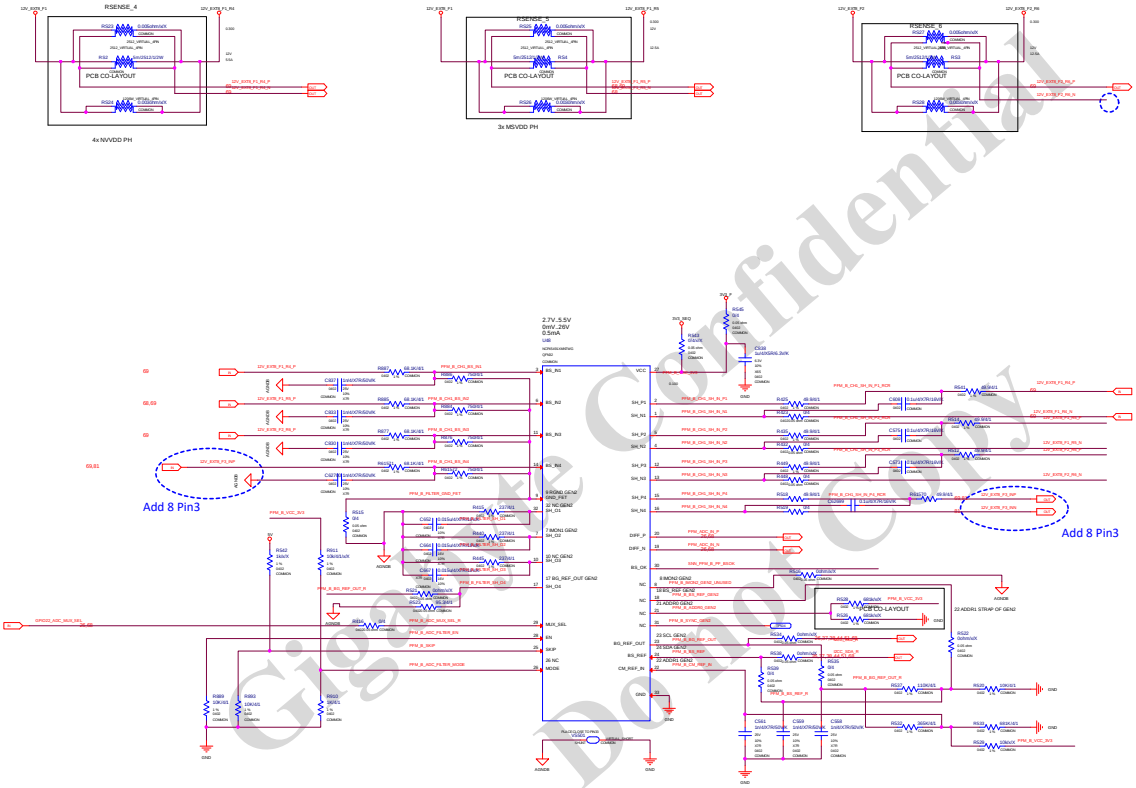
PS: Pre-Filter B



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PREFILTER B

GIGABYTE

Title	PCIE
Size: C	Document Number: GV-N3090AORUS X-24GD
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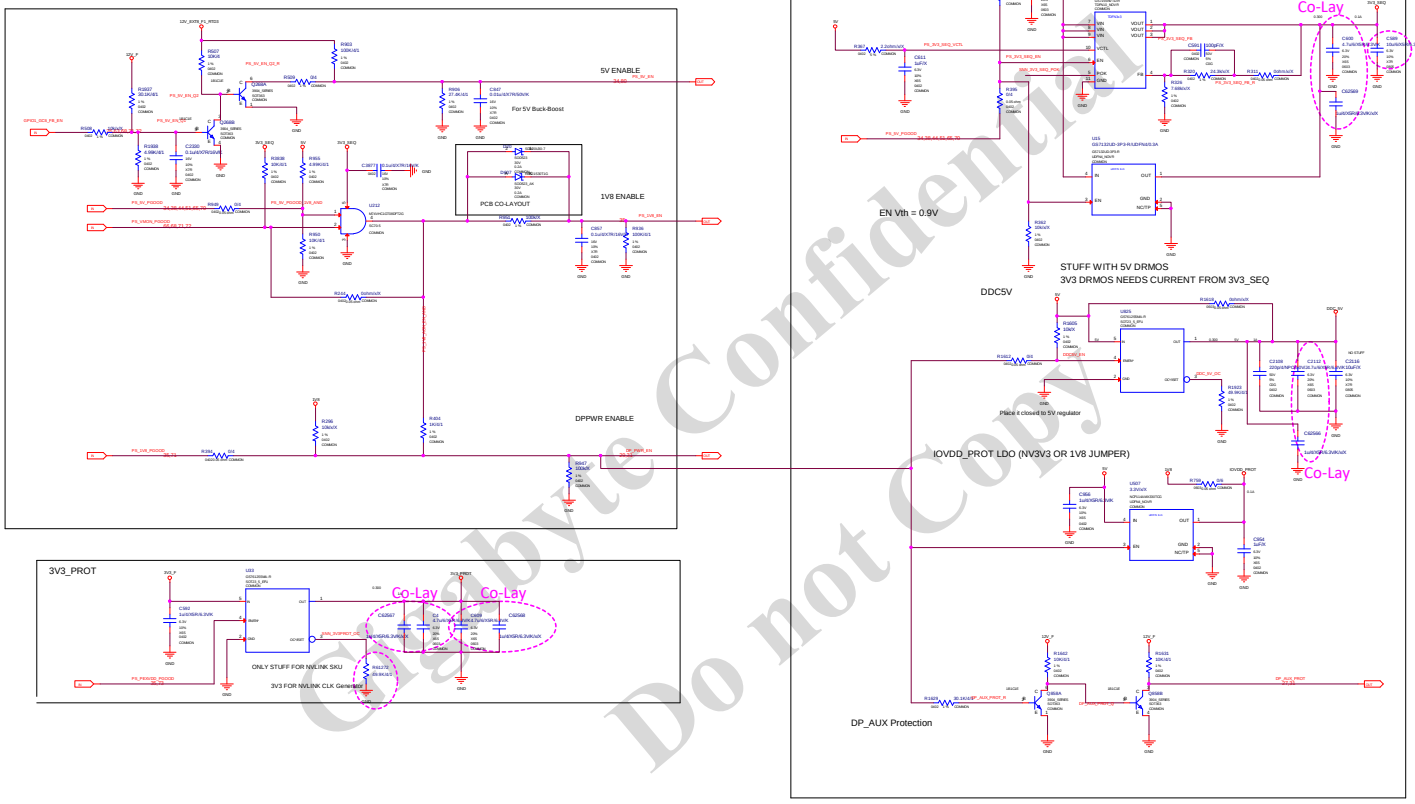
SEQUENCE:5V,1V8,3V3_SEQ ENABLE



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Sequence: 5V, 1V8, 3V3_SEQ

GIGABYTE

Title	PCIE		
Size	Document Number		Rev
Custom	GV-N3090AORUS X-24GD		1.01
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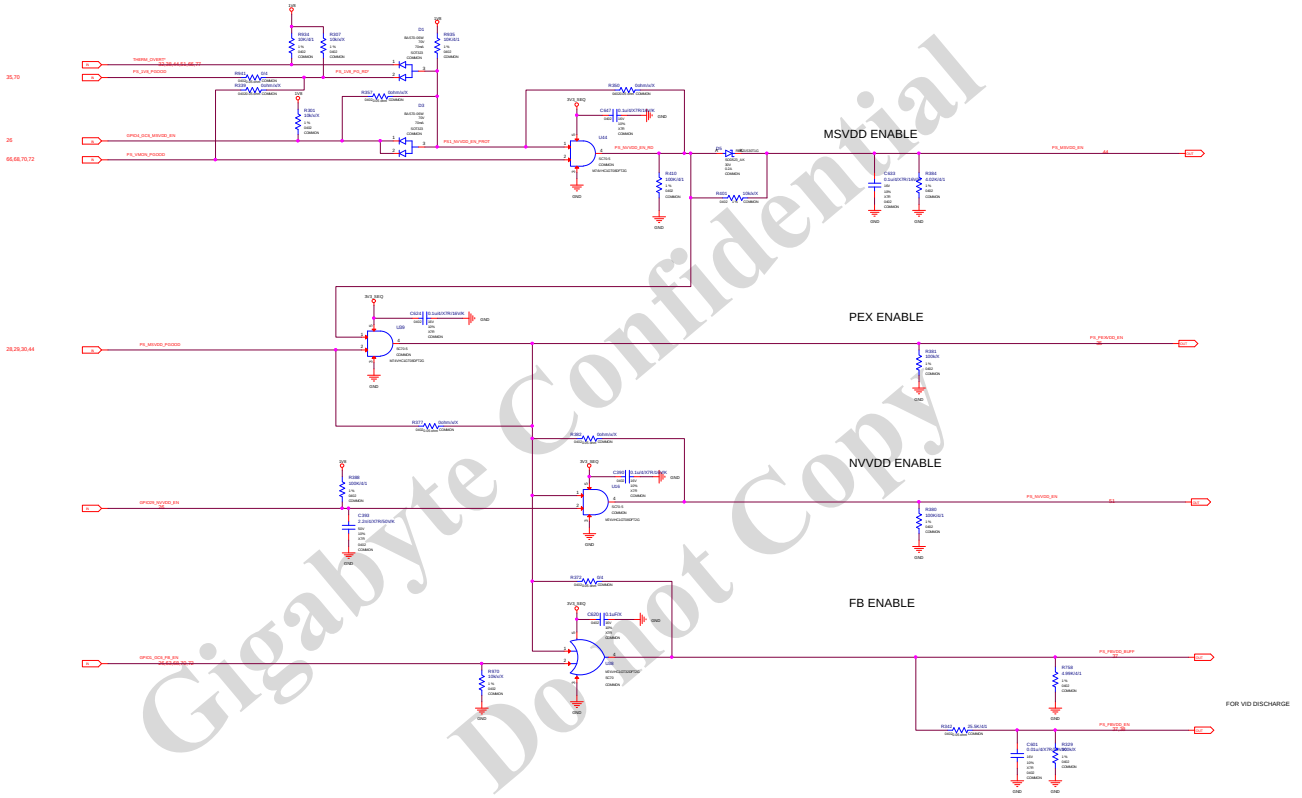
SEQUENCE:NV,PEX,FB ENABLE



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Sequence: NV, PEX, FB EN

GIGABYTE			
Title: PCIE			
Size: C	Document Number: GV-N3090AORUS X-24GD		Rev: 1.01
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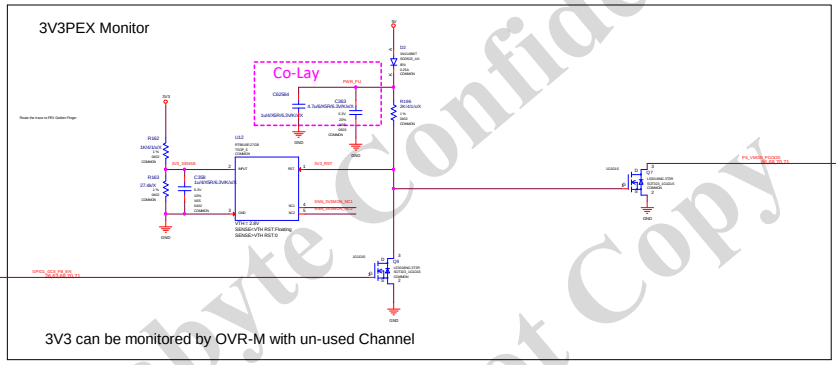
Sequence: 3V3 MONITOR



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PAGE DETAIL

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Sequence: 3V3 MONITOR

GIGABYTE		
Title: PCIE		
Size: Custom	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
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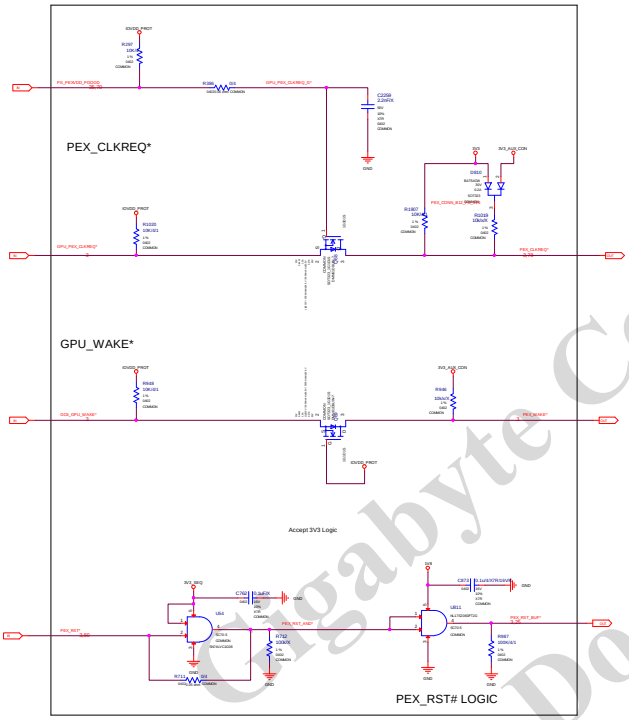
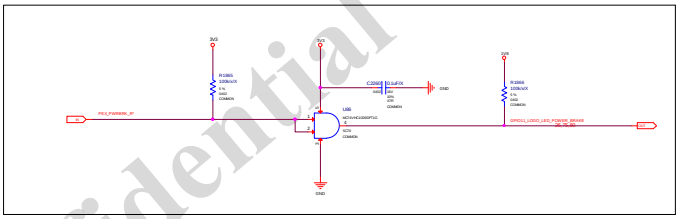
SEQUENCE:MISC





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PAGE DETAIL	Sequence: MISC

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File: PCIE		
Size: D	Document Number: Custom GV-N3090AORUS X-24GD	Rev: 1.01
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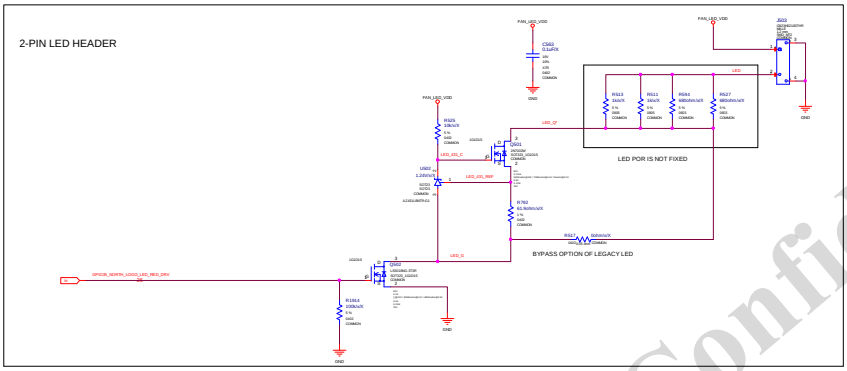
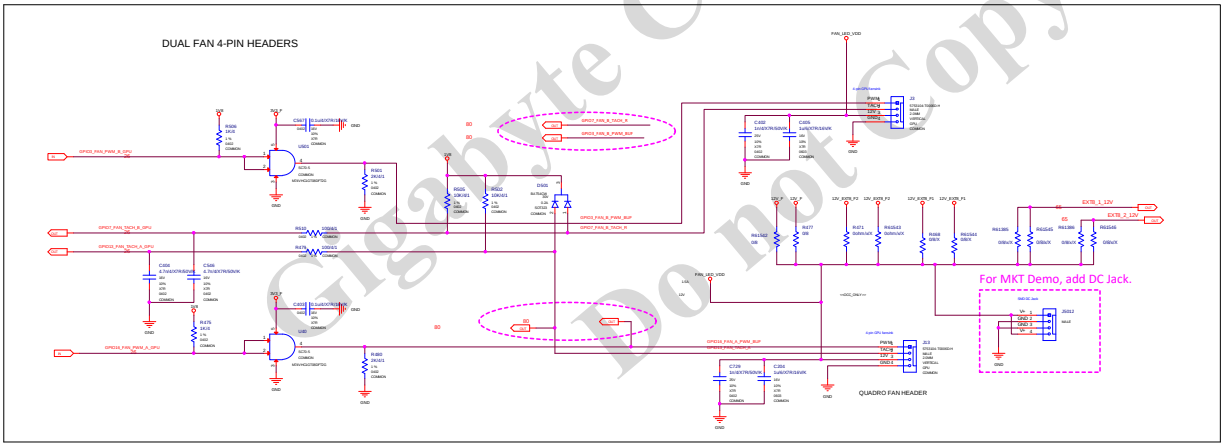
MISC: LED & FAN

2-PIN LED HEADER



DUAL FAN 4-PIN HEADERS



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: LED & FAN

GIGABYTE		
Title: PCIE		
Size: C	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
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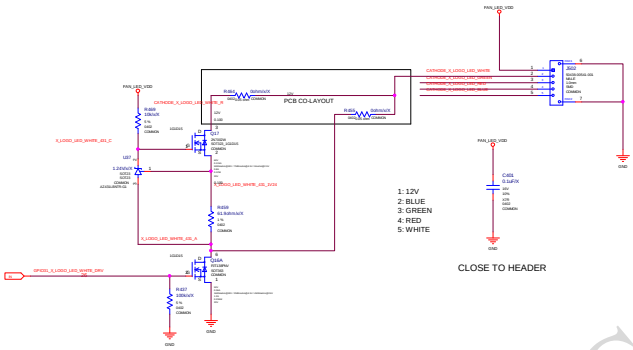
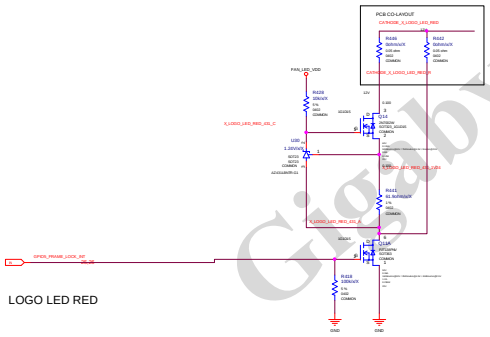
MISC: RGBW LED REF



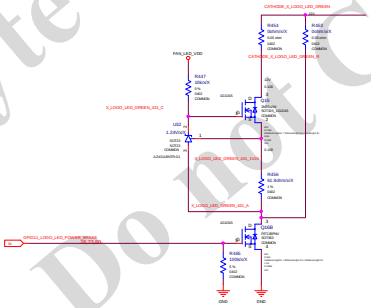
CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALINGN WITH PASH
IF ADDTIONAL POWER CONSUPTION R NEEDED, IT SHOULD BE ON LED MOD.

WHITE DRIVE

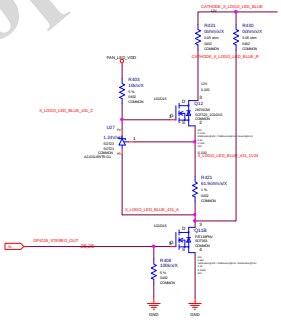


LOGO LED RED

RED DRIVE



GREEN DRIVE



BLUE DRIVE

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	RGBW LED REF

GIGABYTE		
File: PCIE		
Size:	Document Number:	Rev:
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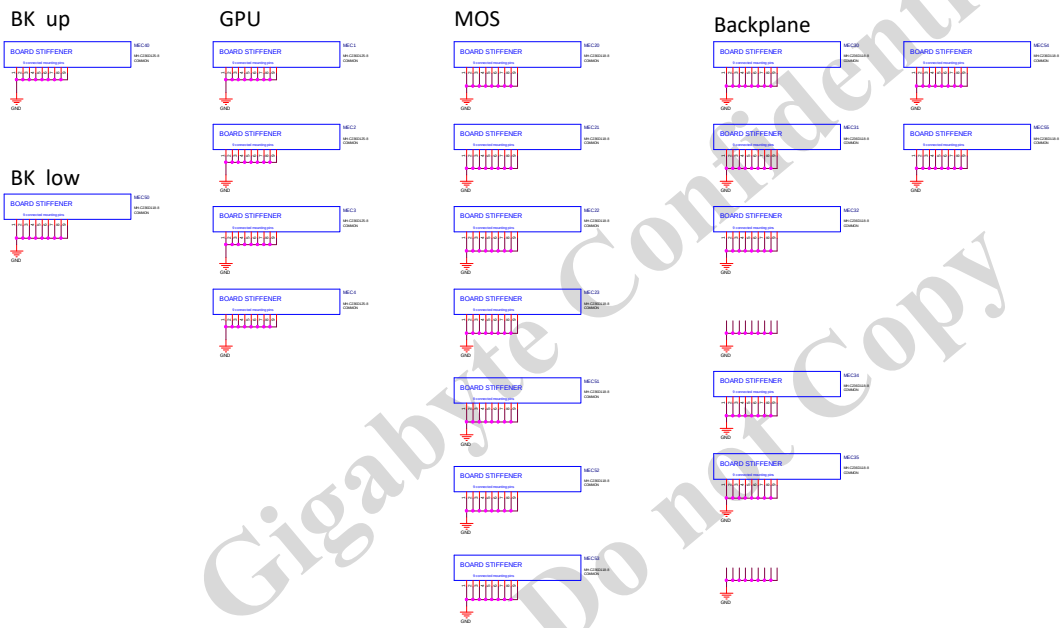
Mechanical: Mounting holes



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL MECH

GIGABYTE			
Title: PCIE			
Size: C	Document Number: GV-N3090AORUS X-24GD		Rev: 1.01
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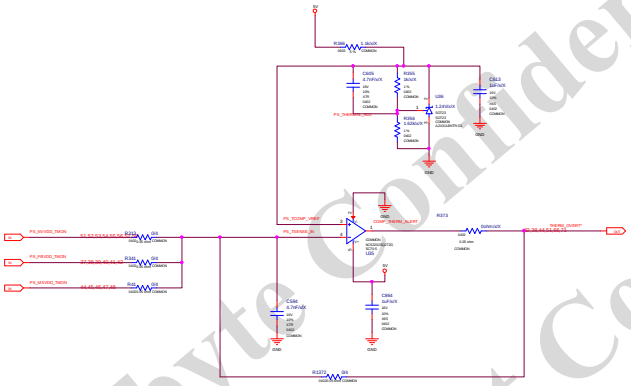
VR THERMAL PROTECTION



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	VR Thermal Protection

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Title: PCIE			
Size: C	Document Number: GV-N3090AORUS X-24GD		Rev: 1.01
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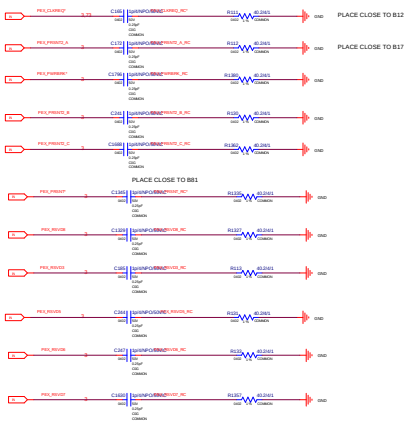
PCI TERM



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCIE TERM

GIGABYTE		
Title: PCIE		
Size: C	Document Number: GV-N3090AORUS X-24GD	Rev: 1.01
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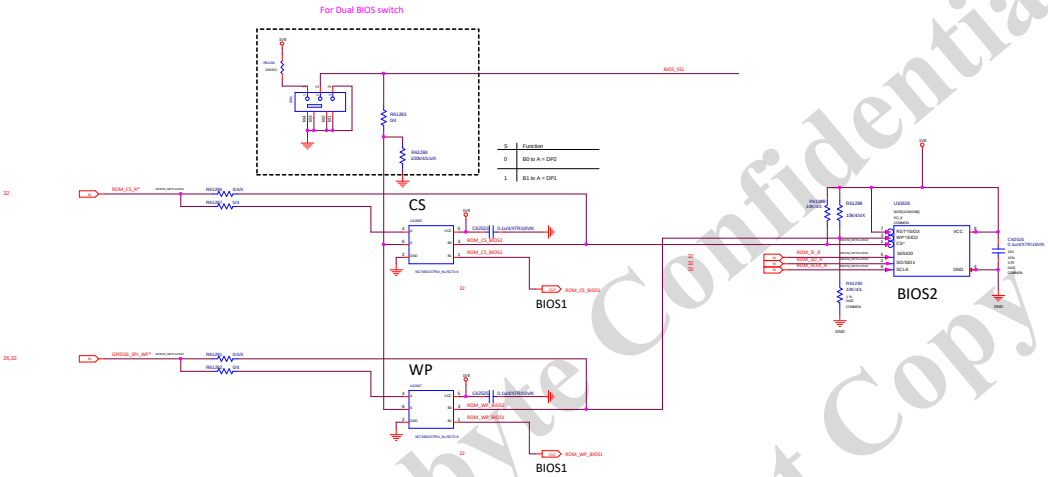
BIOS Switch



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL MCU ZERO POWER IDLE

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Title	PCIE	
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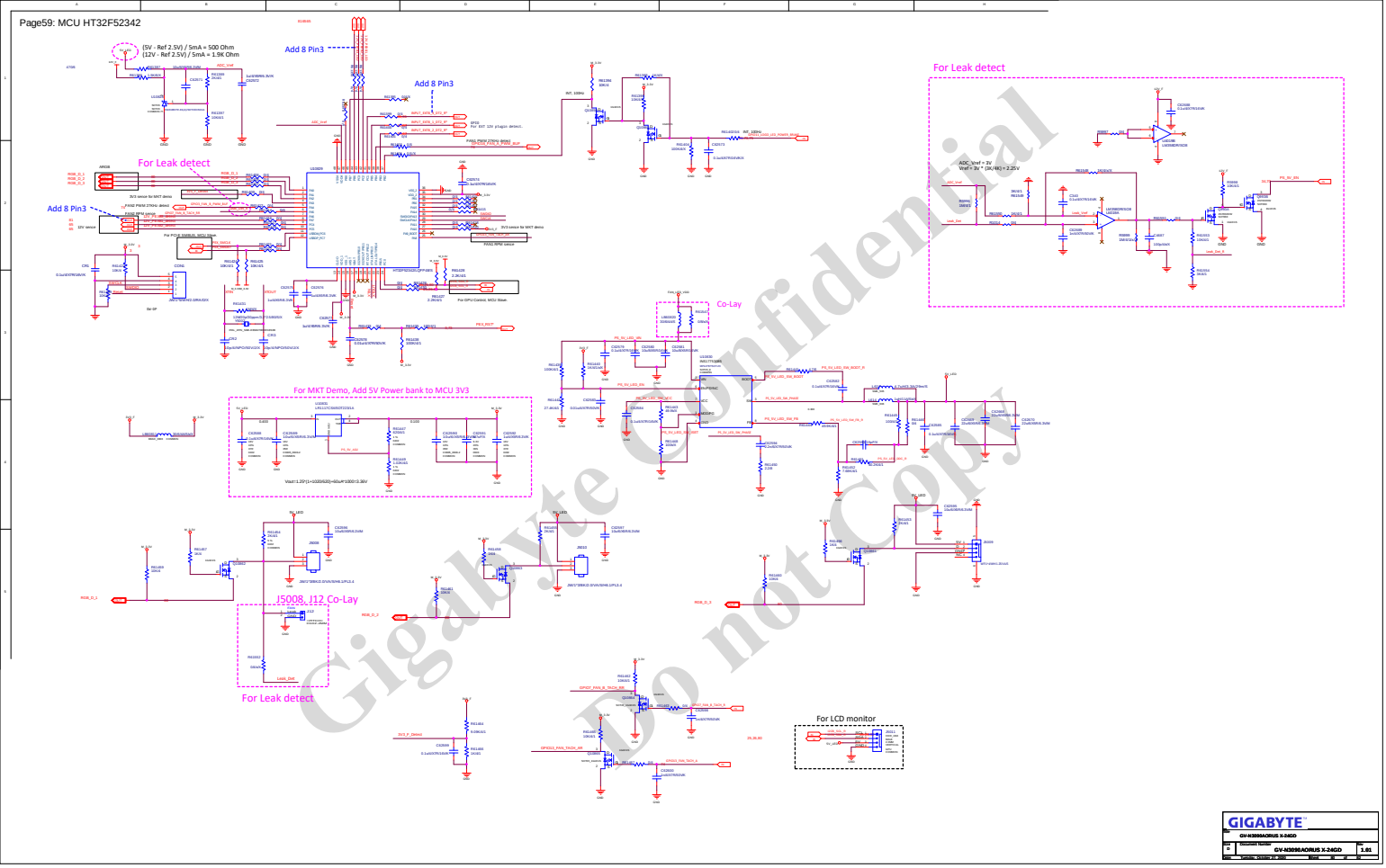

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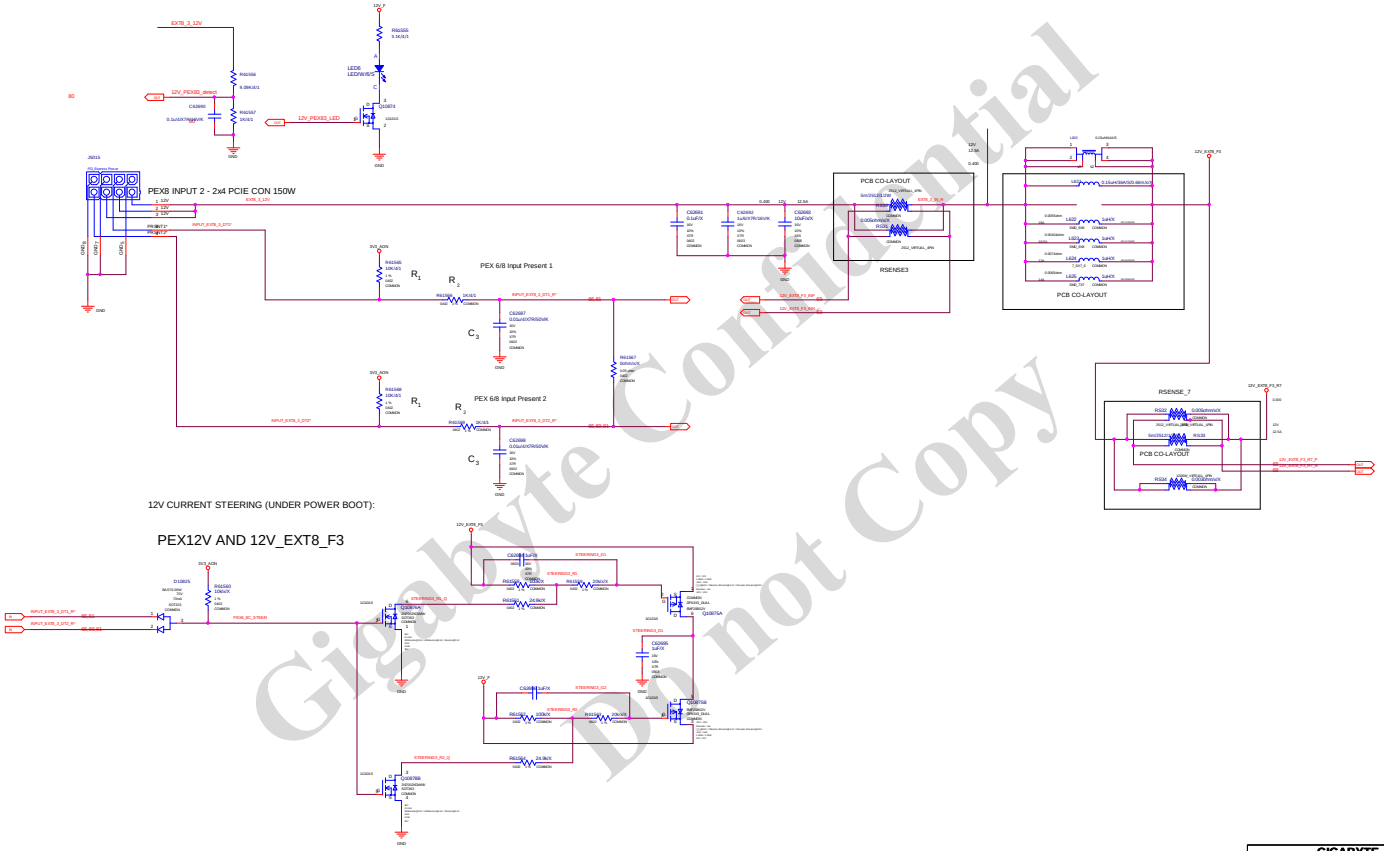

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