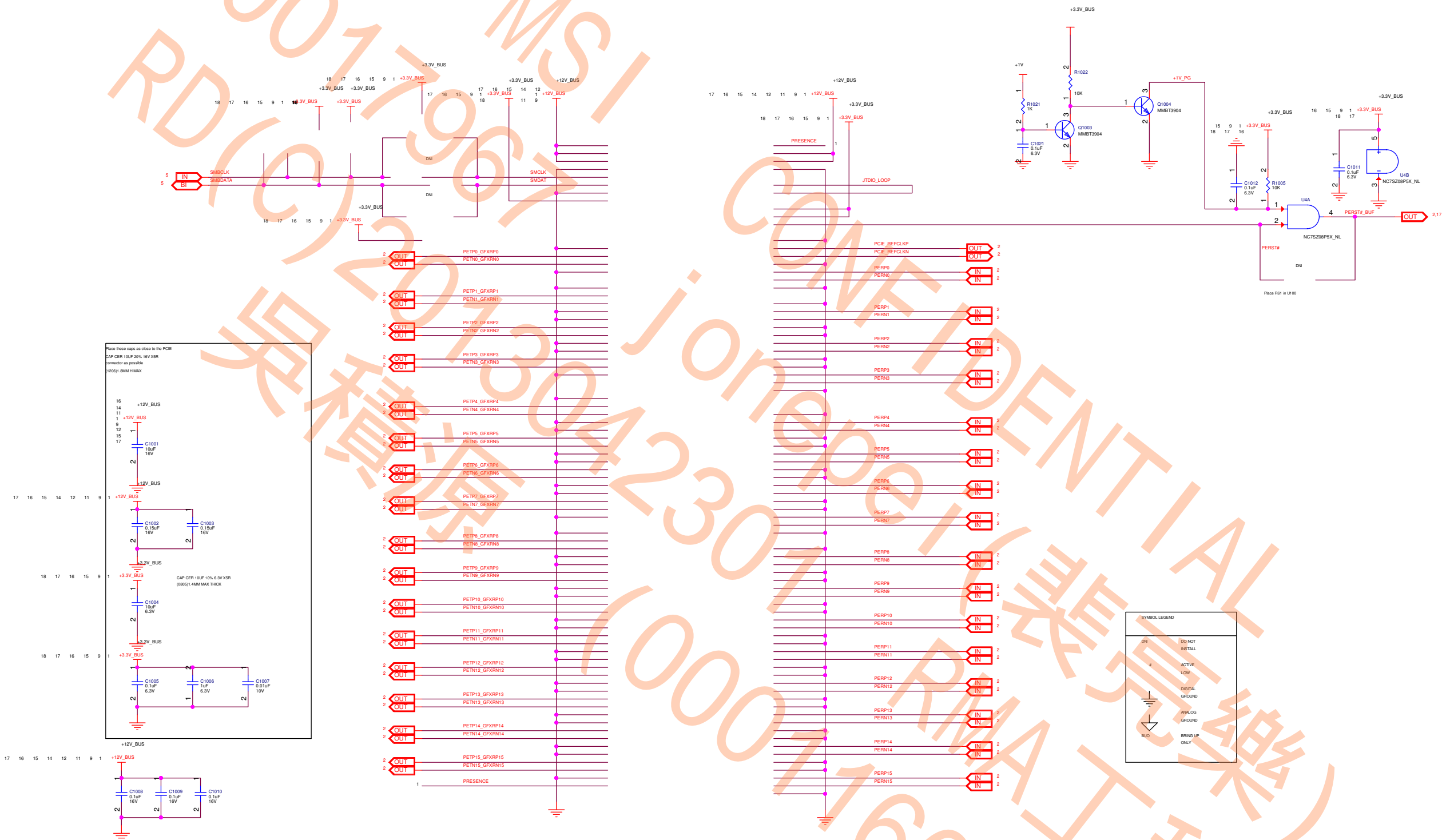

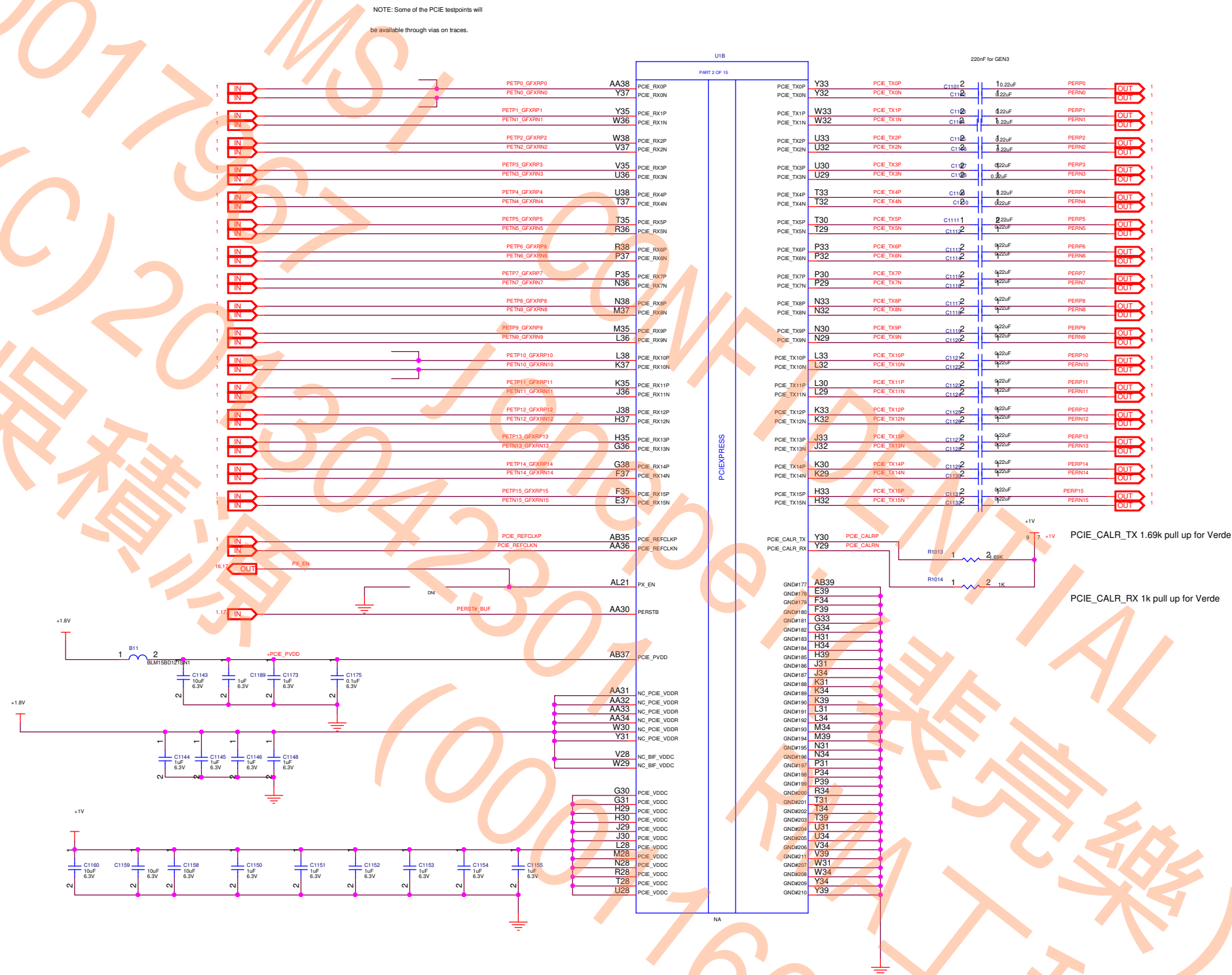



PCI-EXPRESS EDGE CONNECTOR

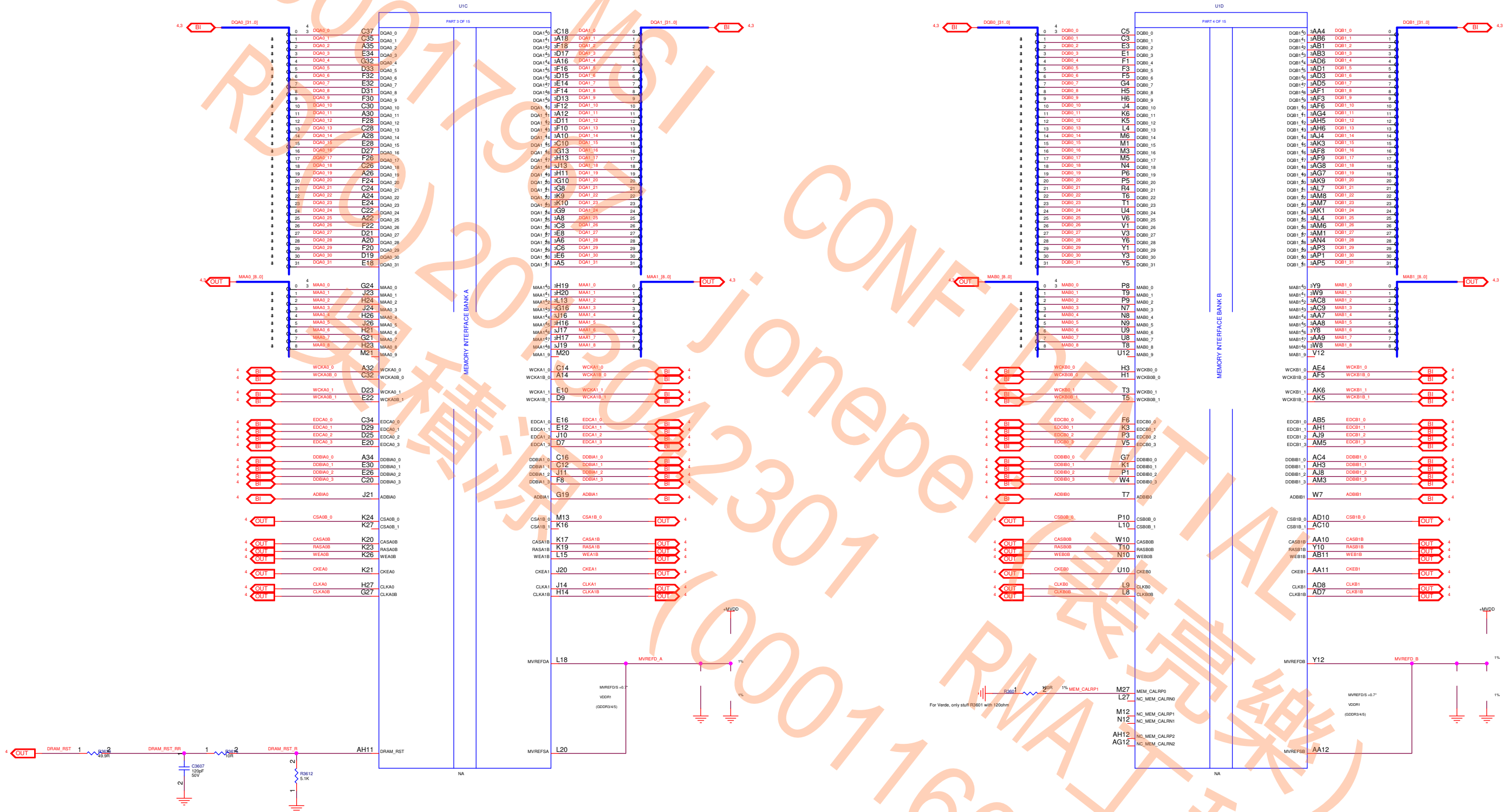


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SHEET:	PCI-E Edge Connector		
DATE:	Sun Dec 04 18:38:13 2011	REV:	15
SHEET NUMBER:	1	OF	20
DOCUMENT NUMBER:	102-C44501-00		
		TITLE:	
		TITLE	

Cape\_Verde PCIe Interface



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SHEET:	Cape Verde PCIe Interface		
DATE:	Thu Dec 01 18:14:20 2011	REV:	15
SHEET NUMBER:	2	OF	20
DOCUMENT NUMBER:	102-C44501-00		
TITLE:		TITLE	



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SHEET: Cape Verde MEMORY INTERFACE

DATE: Thu Dec 01 18:14:54 2011

REV: 15

SHEET NUMBER: 3 OF 20

DOCUMENT NUMBER: 102-C44501-00

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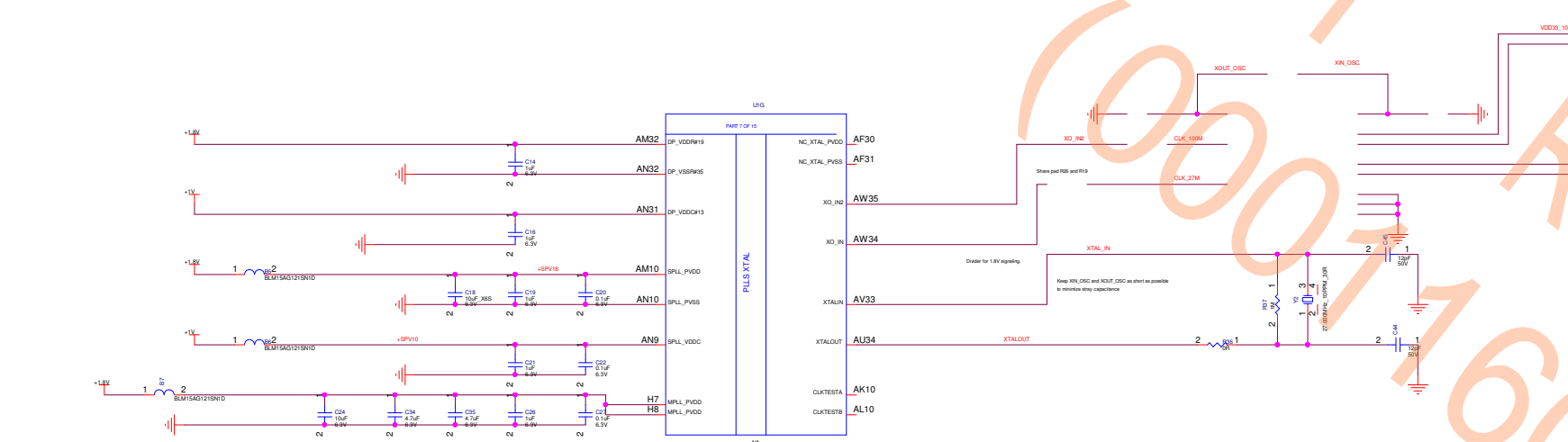
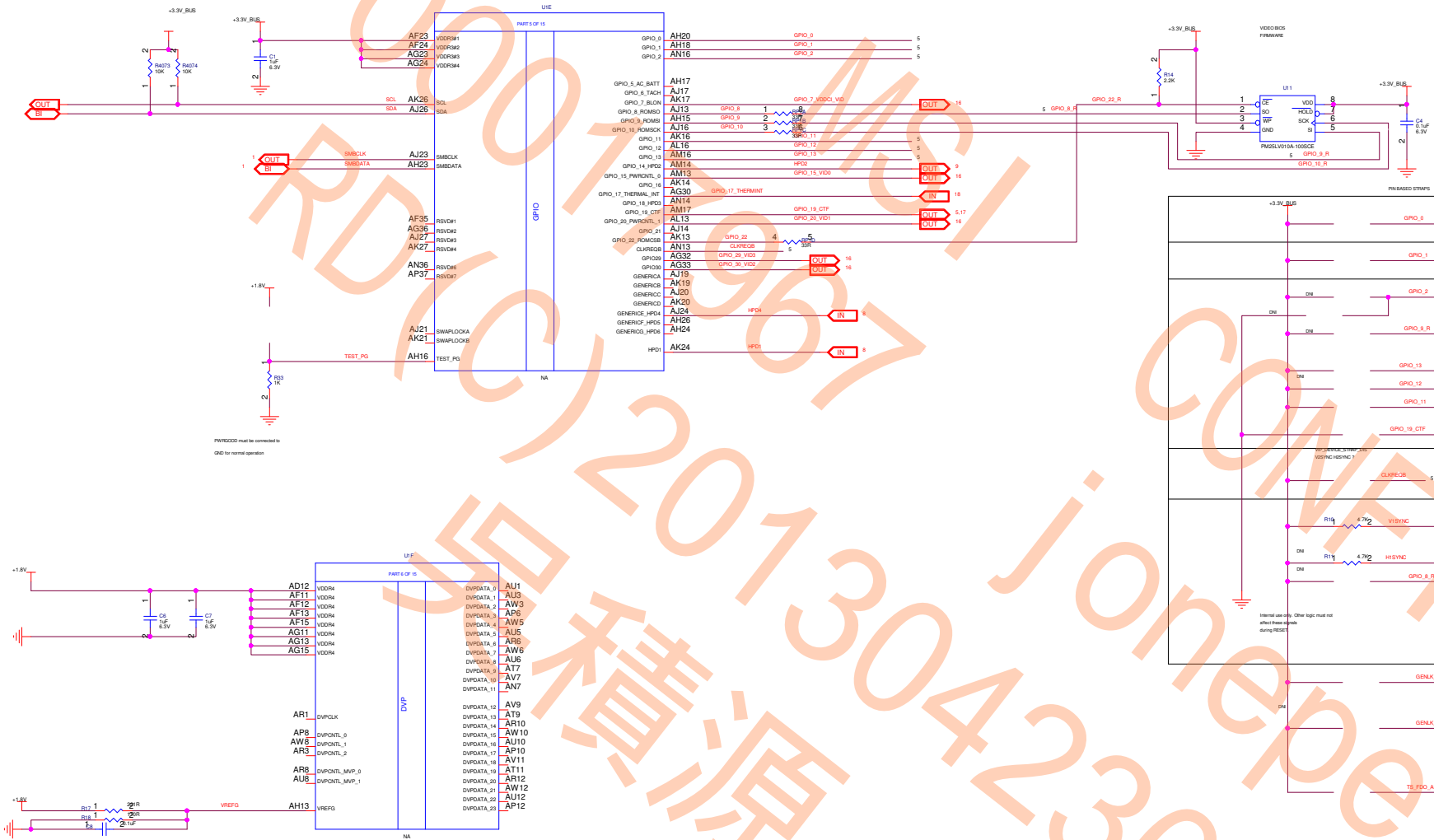
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CAPE VERDE GPIOs Strap CF XTAL OSC

PN 2280079003 for 1Mbit (PM2SLV010A-100SC/E)



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SHEET: Cap Verde GPIO STRAP OF PLL  
DATE: Wed Nov 30 19:36:12 2011  
SHEET NUMBER: 5 OF 20  
DOCUMENT NUMBER: 102-C44501-00  
NOTES: NONE

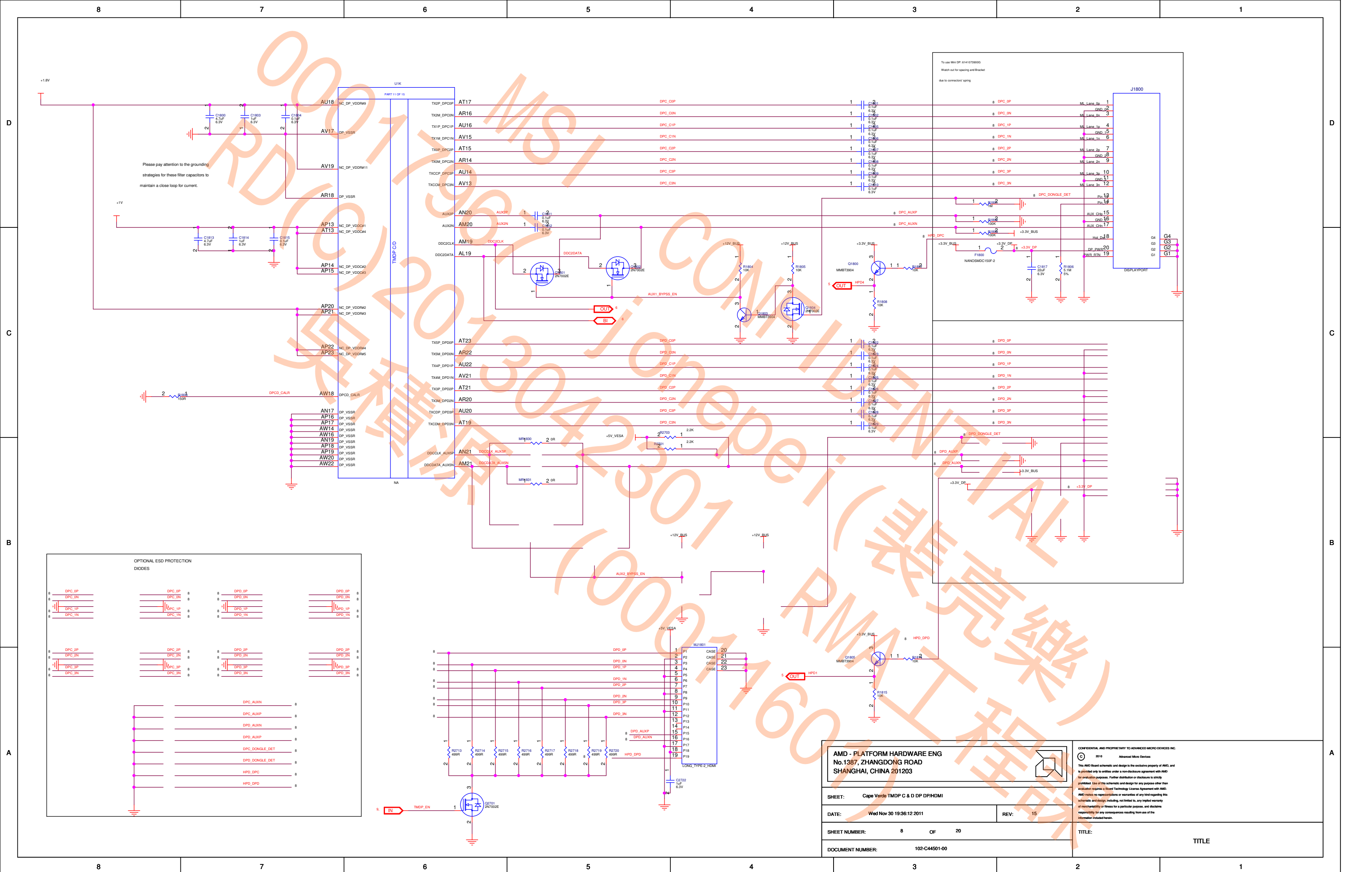
REV: 15

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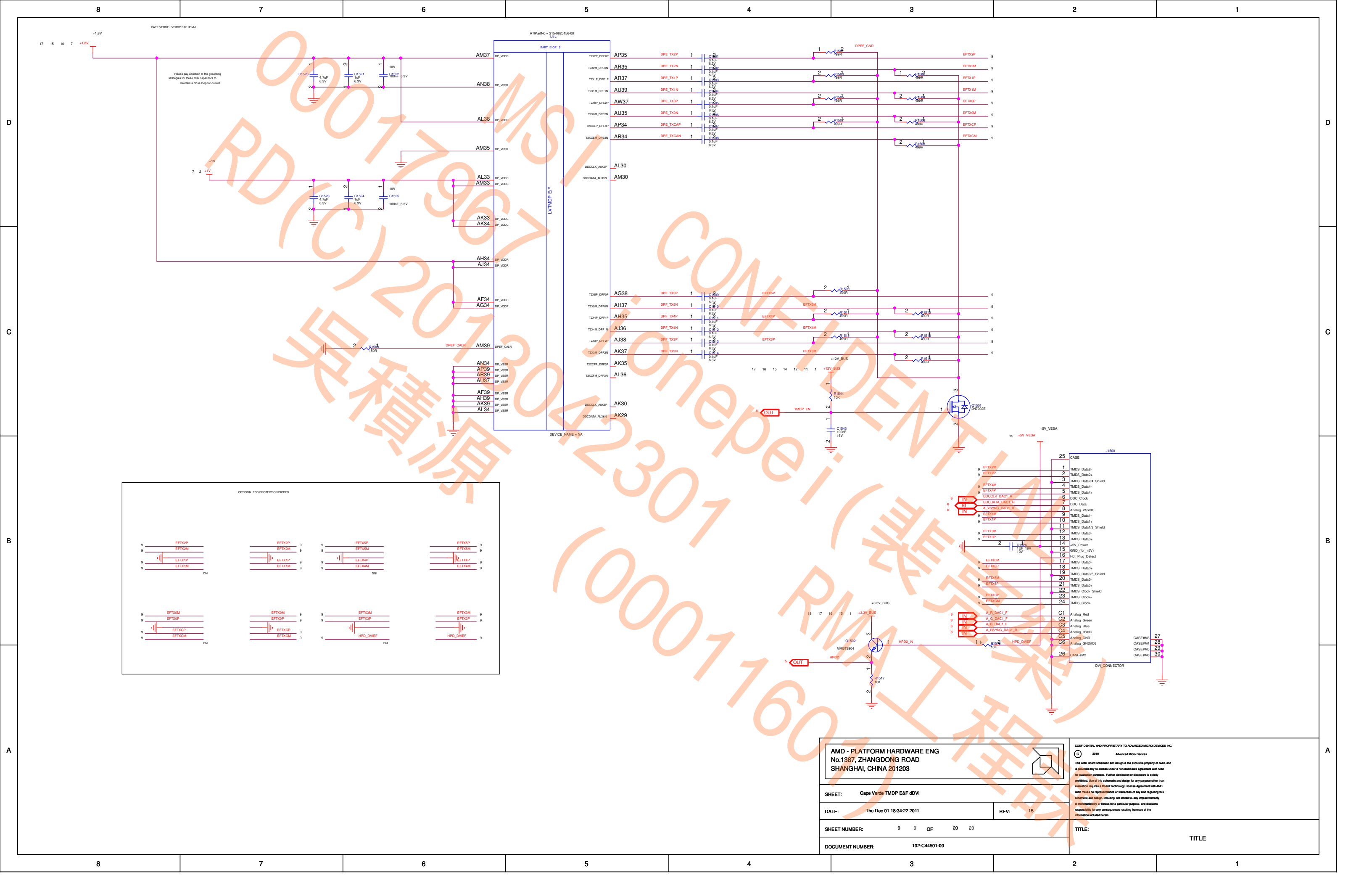
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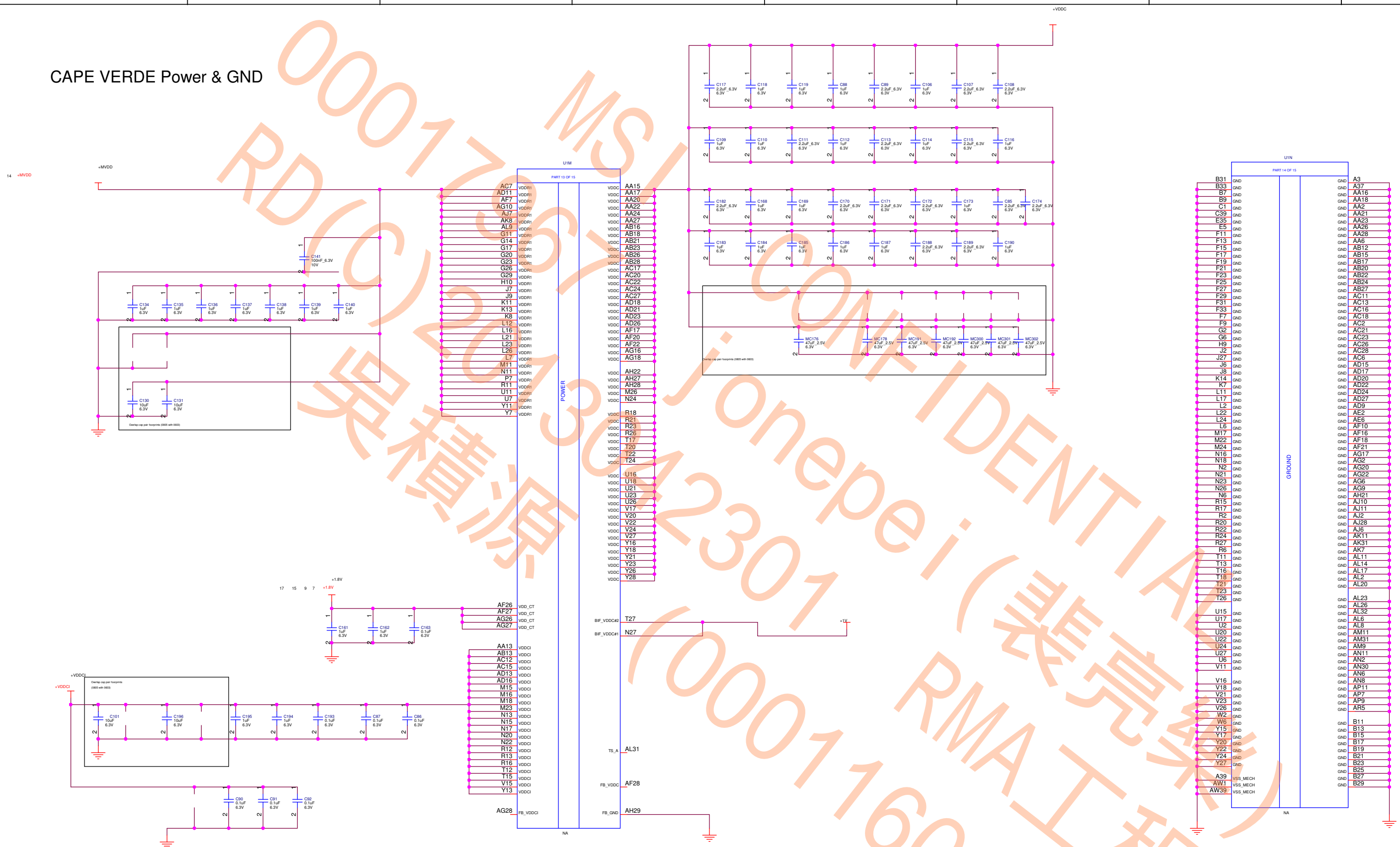








## CAPE VERDE Power & GND



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No.1387, ZHANGDONG ROAD  
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SHEET: Cape Verde Power&GND

REV: 15

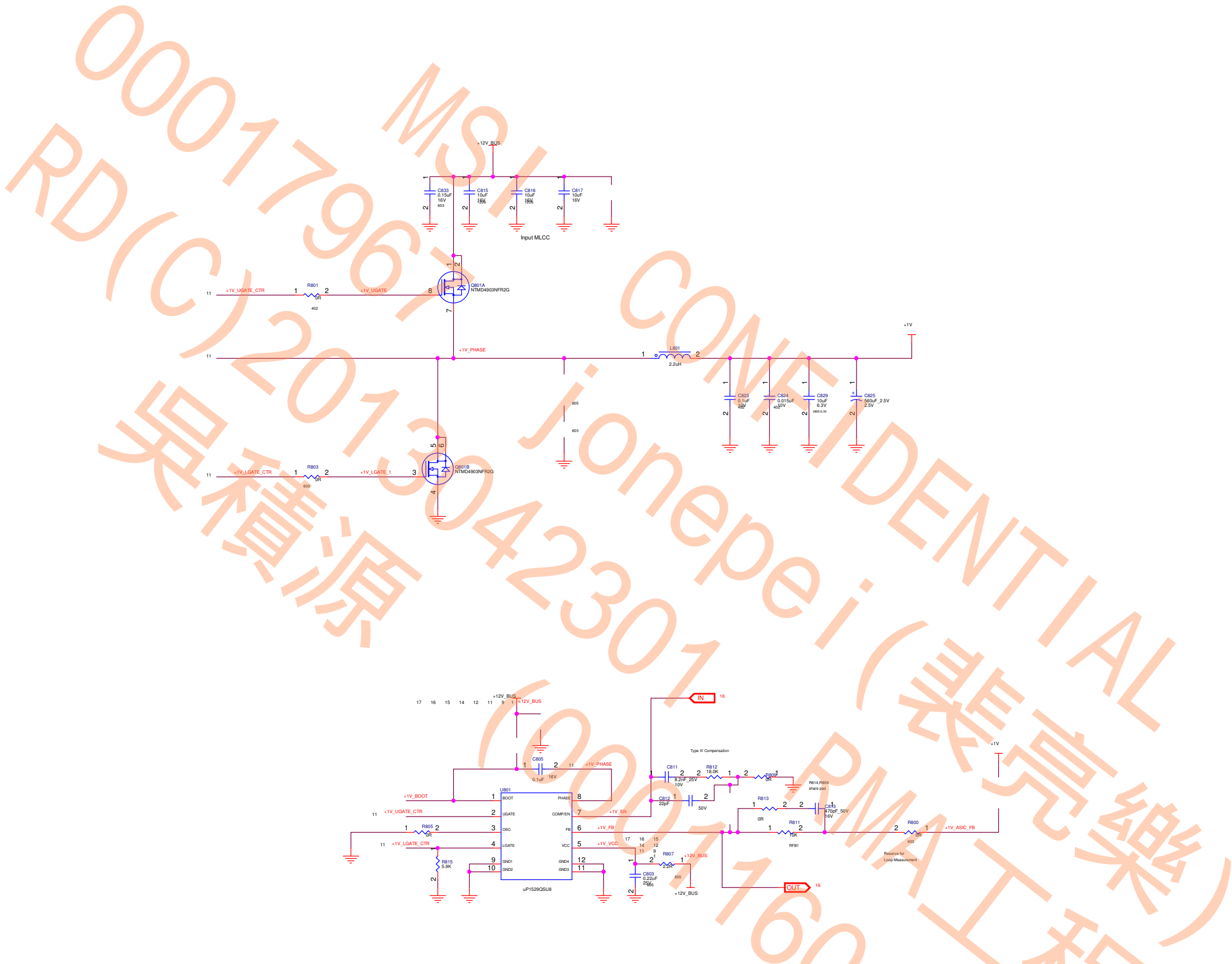
SHEET NUMBER: 10 OF 20

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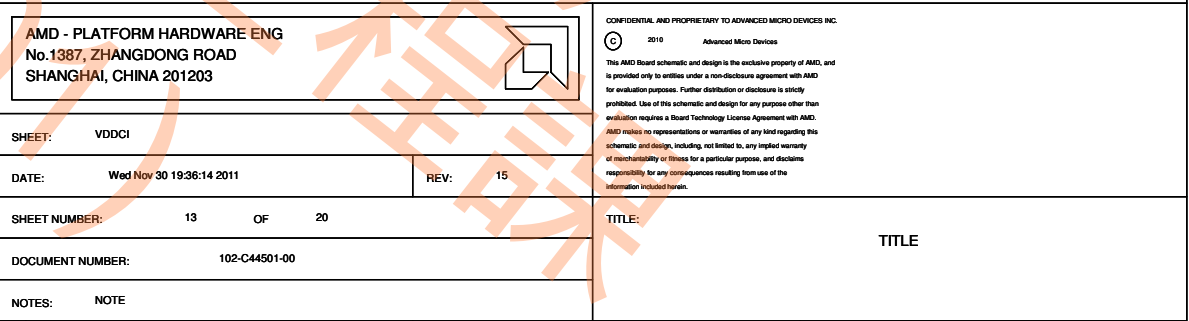
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SHEET:	0.95V REGULATOR	DATE:	Wed Nov 30 19:36:14 2011
SHEET NUMBER:	11 OF 20	REV:	15
DOCUMENT NUMBER:	102-C44501-00	TITLE:	TITLE





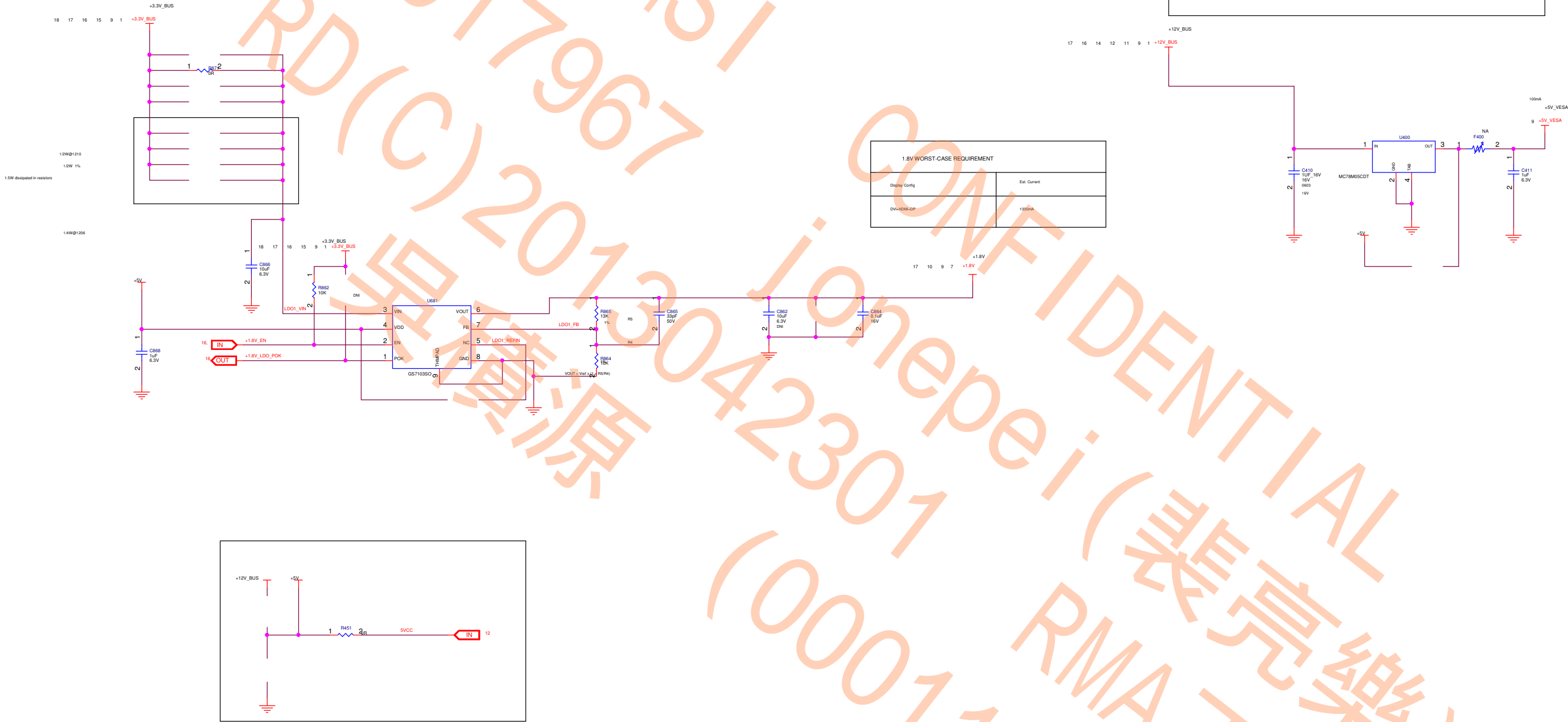




Linear Regulators

LDO #1:  
 $V_{in} = 3.00V \text{ to } 3.60V \text{ (3.3V } \pm 9\%)$   
 $V_{out} = +1.8V \text{ } \pm 2\%$   
 $I_{out} = 1.6A \text{ (TBV) RMS MAX}$   
  
PCB: 50 to 70mm sq. copper area for cooling

Regulators for +5V, +5V\_VESA and +5V\_VESA2



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SHEET: Linear Regulators

DATE: Wed Nov 30 19:36:14 2011

REV: 15

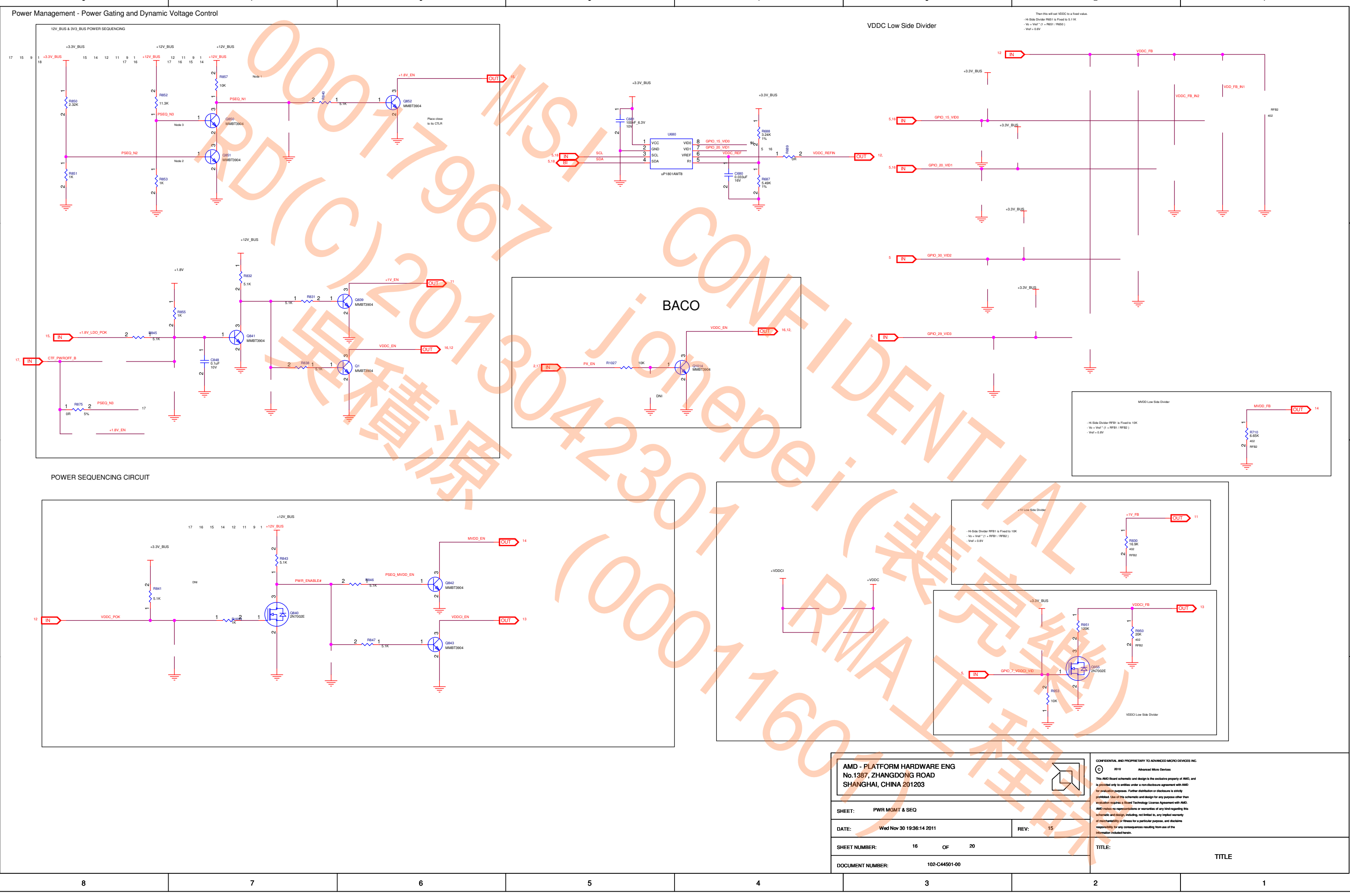
SHEET NUMBER: 15 OF 20

DOCUMENT NUMBER: 102-C44501-00

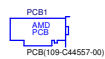
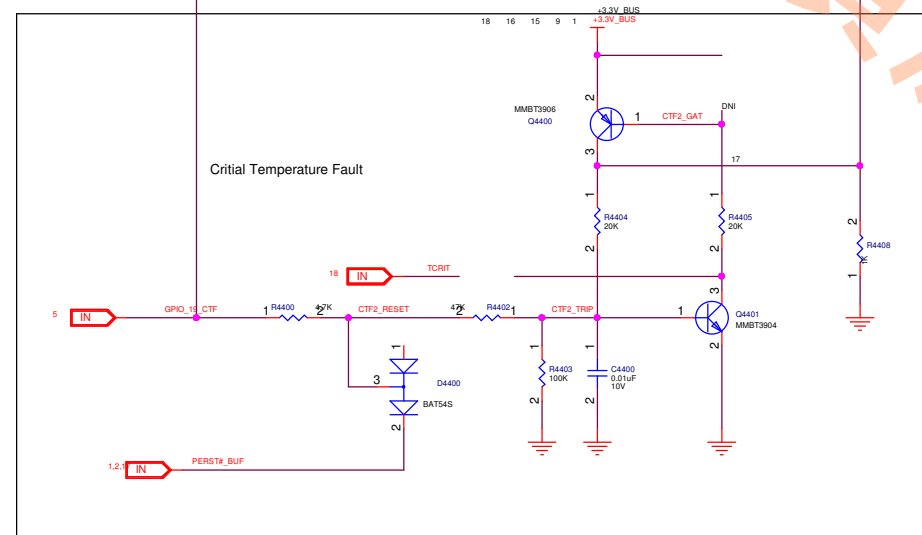
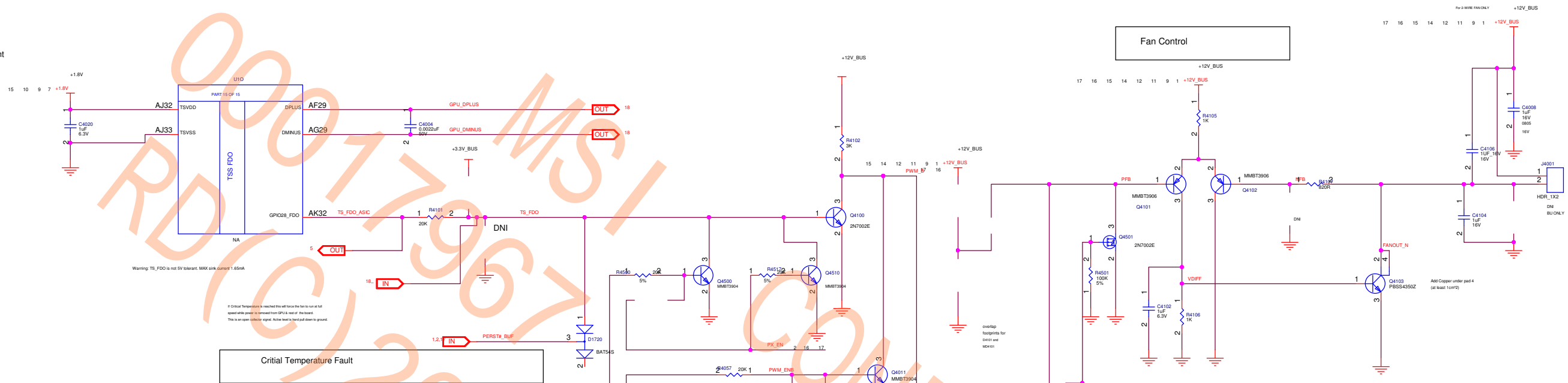
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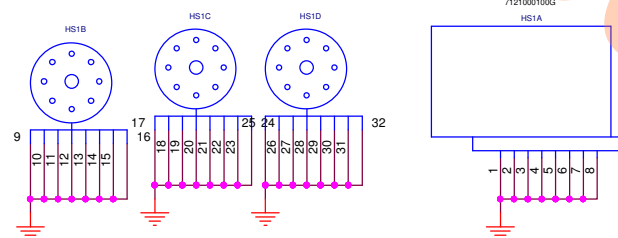
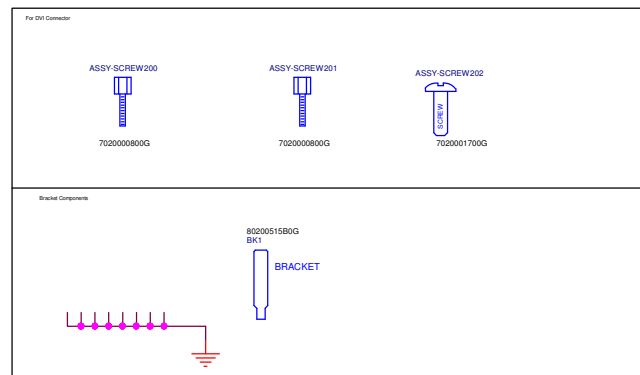
TITLE





## Mechanical and Thermal Management



Socket	60900034500G	
Bracket	80200515A0G	VGA DP DVI
Bracket	80200515C0G	DP DP DVI
Bracket	8020051500G	VGA HDMI DVI
Bracket	80200515B0G	DP HDMI DVI
Fansink	7121000100G 7122000100G 7120781200G	For 75W board

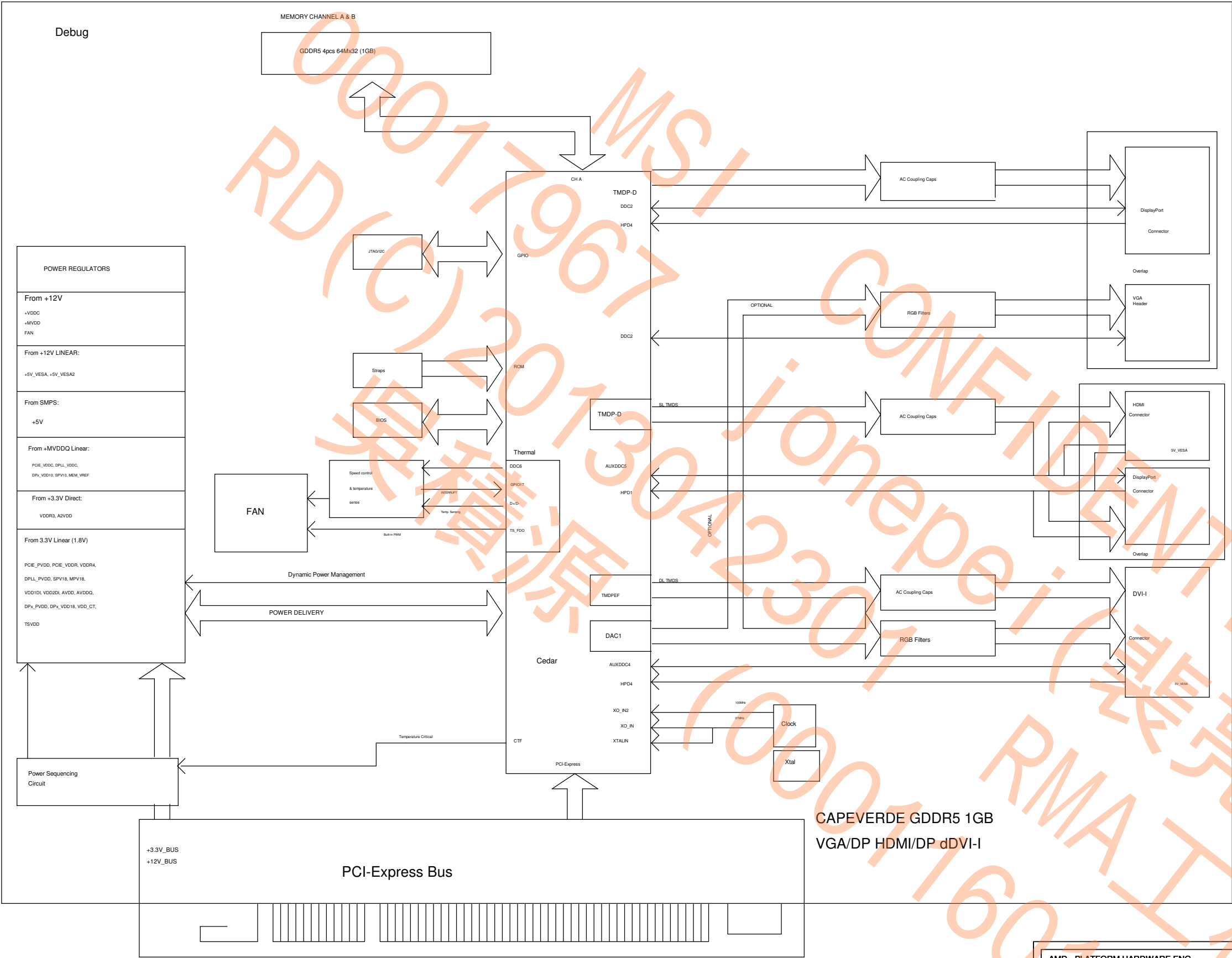


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<div>DATE RECEIVED BY:</div> <div>AMD - PLATFORM HARDWARE ENG No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203</div> <div></div>			<div>DATE RECEIVED BY:</div> <div>AMD - PLATFORM HARDWARE ENG No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203</div> <div></div>		
SHEET:      Mech/Thermal Management			SHEET:      Mech/Thermal Management		
DATE:      Thu Dec 01 15:26:18 2011			REV:      15		
SHEET NUMBER:      17      OF      20			SHEET NUMBER:      17      OF      20		
DOCUMENT NUMBER:      102-C44501-00			DOCUMENT NUMBER:      102-C44501-00		
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**A**





CAPEVERDE GDDR5 1GB  
VGA/DP HDMI/DP dDVI-I

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SHEET: BLOCK DIAGRAM					
DATE: Thu Dec 01 18:36:08 2011		REV: 15			
SHEET NUMBER: 19 19 OF 20				TITLE:	
DOCUMENT NUMBER: 102-C44501-00				TITLE	

8		7		6		5		4		3		2		1	
			TITLE CAPE VERDE PRO GDDR5 64Mx2 dDVI+HDMI+DP+DP+VGA				SCHEMATIC NO. 105-C445XX-00		DATE						
			REVISION HISTORY						NOTE: THIS SCHEMATIC REPRESENTS THE PCB. IT DOES NOT REPRESENT ANY SPECIFIC BOM. FOR SUFFICIENT OPTIONS/COMPONENT VALUES, ON PLEASE CONSULT THE PRODUCT SPECIFIC BOM. PLEASE CONTACT AMD REPRESENTATIVE TO OBTAIN LATEST BOM CLOSEST TO THE APPLICATION DESIRED.						REV P04
SCH REV	PCB REV	DATE	REVISION DESCRIPTION												
00	00A	20110711	Initial CAPE VERDE schematic.												
01	00B	20110823	1. Update bracketed OP ROM DVI to 80205515800L. 2. add GMR5154M2. 3. add GMR5154M20 to DC DAC. 4. remove BUF_VDDC.												
02	00C	20110927	1. add SAGO fan delay circuit. 2. Update 1.8V LDO symbol to 087103. 3. Remove some debug circuit.												
03	00D	20111015	1. update SAGO fan delay circuit.												
04	00	20111108	1. update C19F to 0104 08T1R1.												