### P561: G98, DDR2 MEMORY 32MX16/16Mx16/64MX16

Page 1: P561 Overview

Page 2: PCI Express Interface

Page 3: Frame Buffer Interface

Page 4: Memory 1st Bank 0..31

Page 5: Memory 1st Bank 32..63

Page 6: DACA, Slim DB15 Connector

Page 7: DACC,2x6 Header

Page 8: VIDEO CONNECTORS: MiniDIN

Page 9: TMDS Interface

Page 10: UNUSED SECTIONS FOR G98

Page 11: Straps, Mechanical Parts

Page 12: XTAL, GPIO, BIOS, FAN, JTAG, HDCP, SPDIF

Page 13: Power Supply I: NVVDD, PLLVDD

Page 14: Power Supply II: F3V3, 5V, DDC5V, FBVDDQ

Page 15: Basenet Report

Page 16: Cref Part

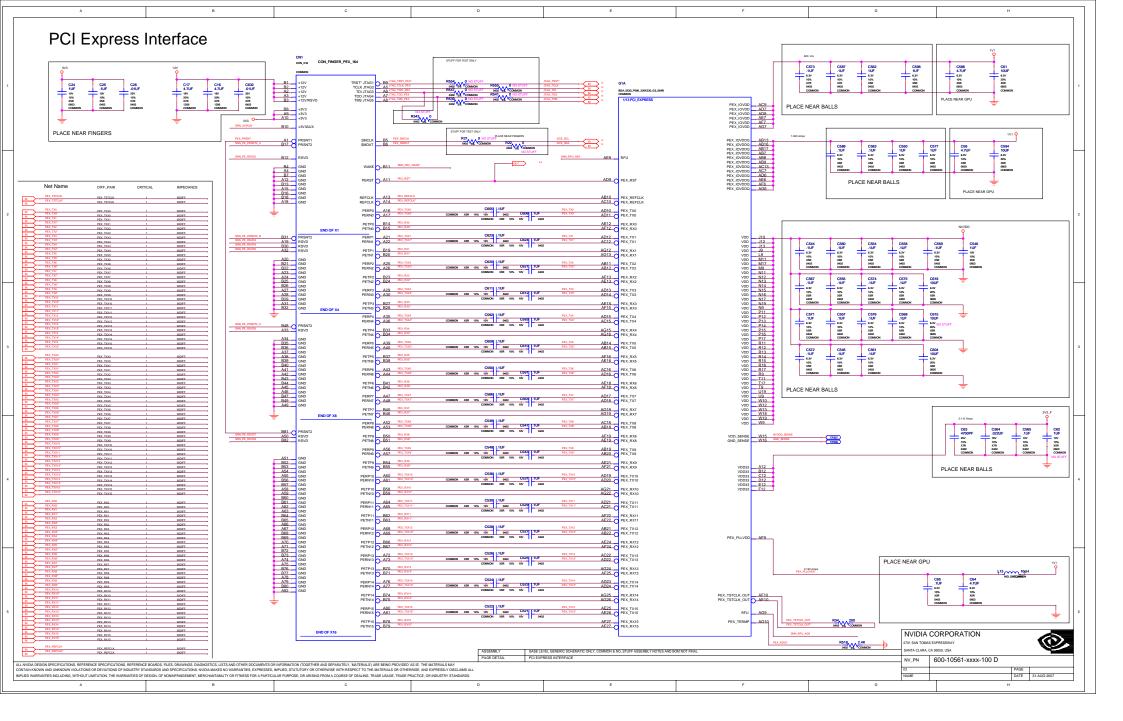
History 10	)	
96/09/27	page 08	add AV_OUT
	page 13	change Q1, Q2 to TO252
	page 14	add FBVDDQ-linear block, change U2 footprint
96/09/28	page 07	change J4 footprint
	page 12	add J7 (co-lay J6)
	page 13	add R572 for RT9259A, R570 footprint change to 0805,
		change L11, C11, C12, C31 footprint
	page 14	remove PWM block
		add D20, D21, C211, C212, C213, C214
96/10/01	page 14	add R210, R211
	page 09	add R75~R88, R63~R69, L15~L21 for DVI (EMI_solution)
96/10/02	page 12	add FAN Control Function
96/10/03	page 09	and netname (Between common Choke and DVI connector)
96/10/05	page 12	cnage Y501 (4 pin to 2 pin)
96/10/12	page 12	add L30, remove L10
96/10/12		CB:2.0 CIRCUIT DSN CAHNGE to PCB:1.0
	ONLY CHA	1 - 3
00/40/47		remove C301~~C308 ( EMI solution for FBVDDQ)
96/10/17 96/10/18		add CABLE and PCB
96/10/16	page 14	add C301~~C308 ( EMI solution for FBVDDQ)
History 20		
96/10/03 p	age 14 re	move FBVDDQ-LINNEAR block, add FBVDDQ-PWM function
		ange L15 footprint as CHK4417C_3R3S01, change C35 footprint
		hnge Y501 (4pin to 2 pin)
96/10/09 p		d FM1~~ FM6 for Fiducial Point
		dd U301~~U306 for EMI
		dd C309 for EMI
		dd C301~~C308, C310~~C312 for EMI dd L30
		move L10
		dd cable
00/10/11	Jago ac	
History 21		
	age 13 add	C11, C12 foot print C_P3_5_D8_H11_5
p	age 14 chai	nge L15 footprint, increase PHASE's line width of FBVDDQ on top plane
96/11/07 p	age 13 add	C211,C212,C213,C214

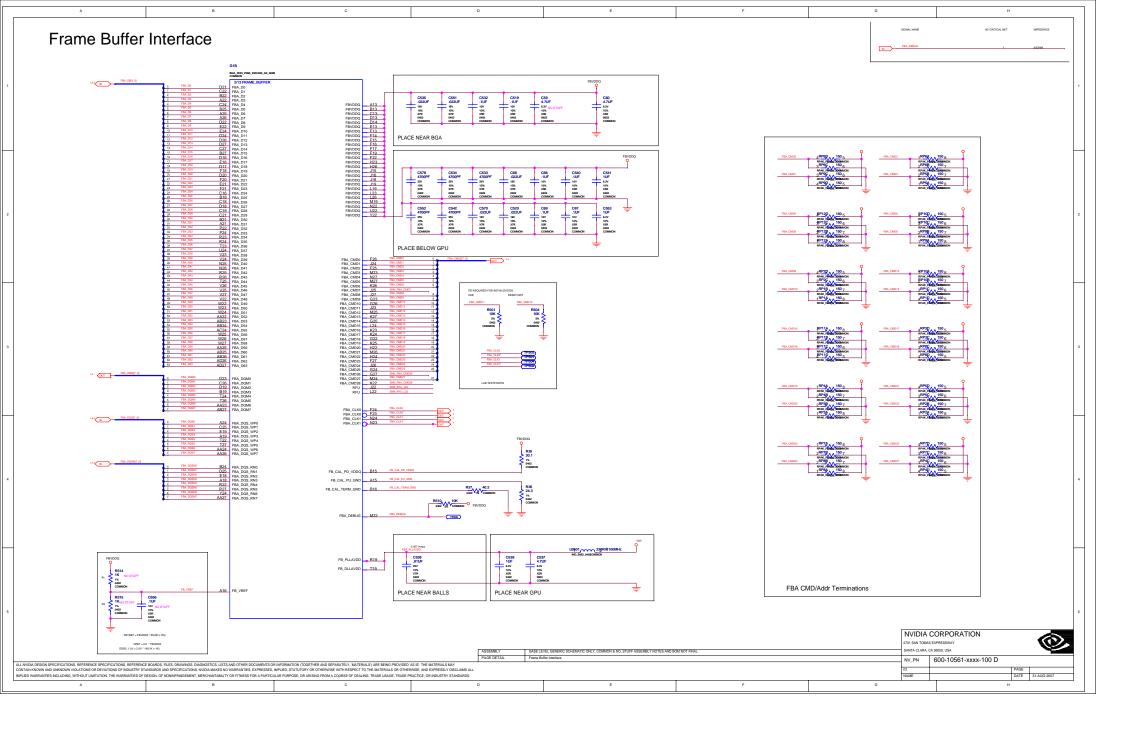
**REV HISTORY** 

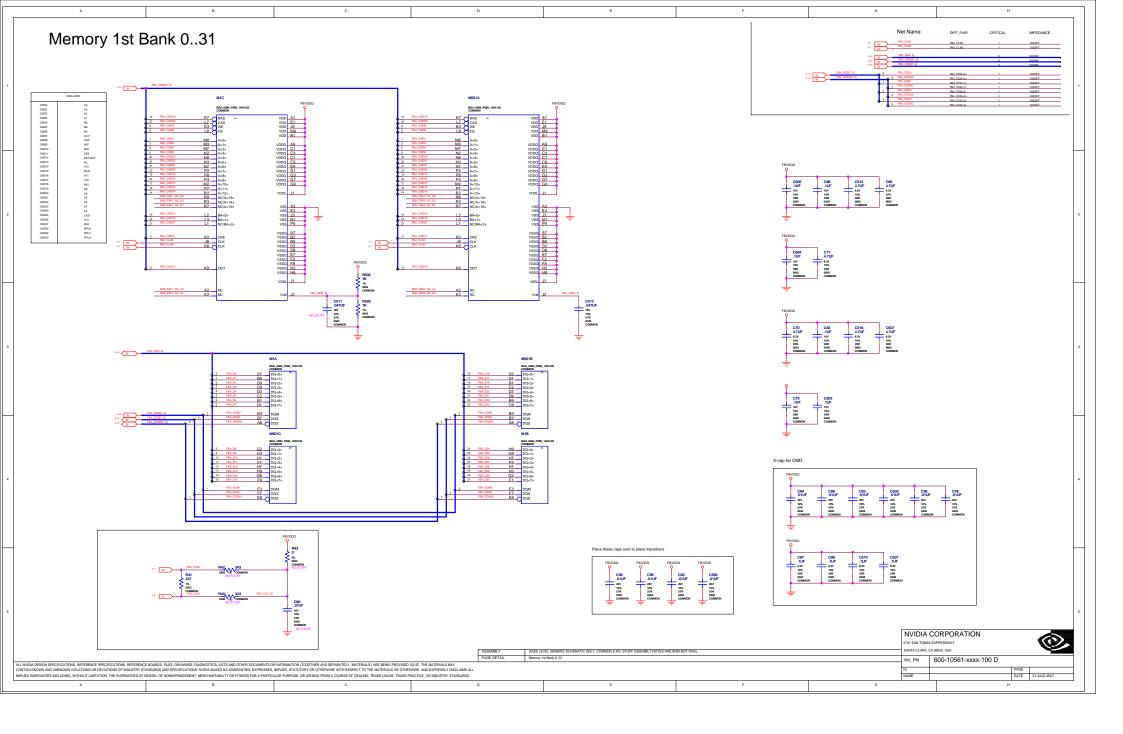
sku	VARIANT	NVPN	ASSEMBLY					
В	BASE	600-10561-xxxx-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL					
1	SKU0000	600-10561-0000-100	P561: G98-300, 64 BIT DDR2 16ftk:16 MEMORY, VGA+DVI+HDout					
2	SKU0001	600-10561-0001-100	P561: G98-300, 64 BIT DDR2 32Mx16 MEMORY, VGA+DVI+HDout					
3	SKU0997	600-10561-0997-100	P561: G98-300, 64 BIT DDR2 32MX16 MEMORY, VGA+DVI+HDDUT					
4	SKU0997	600-10561-0997-200	P561: G98-300, 64 BIT DDR2 32MX16 MEMORY, VGA+DVI+HDOUT					
5	SKU0001	600-10561-0001-200	P561: G98-300, 64 BIT DDR2 32MX16 MEMORY, VGA+DVI+HDDUT					
6	<undefined></undefined>	<undefined></undefined>						
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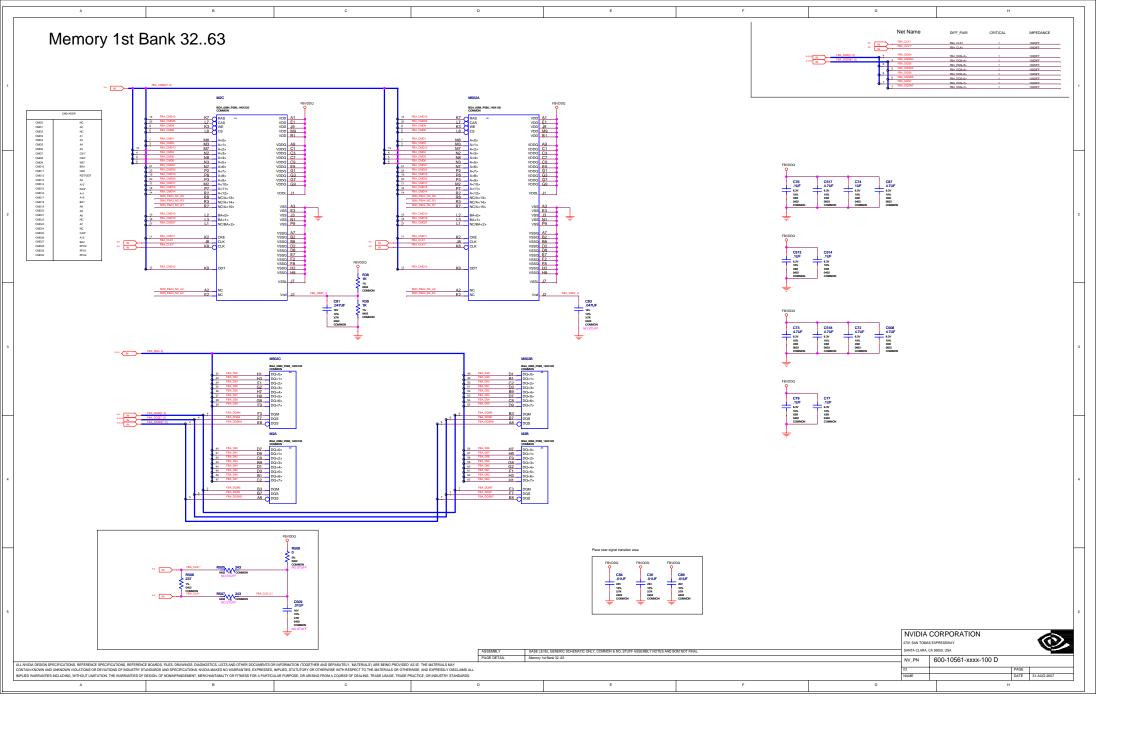
NVIDIA CORPORATION PAGE DETAIL NV\_PN 600-10561-xxxx-100 D

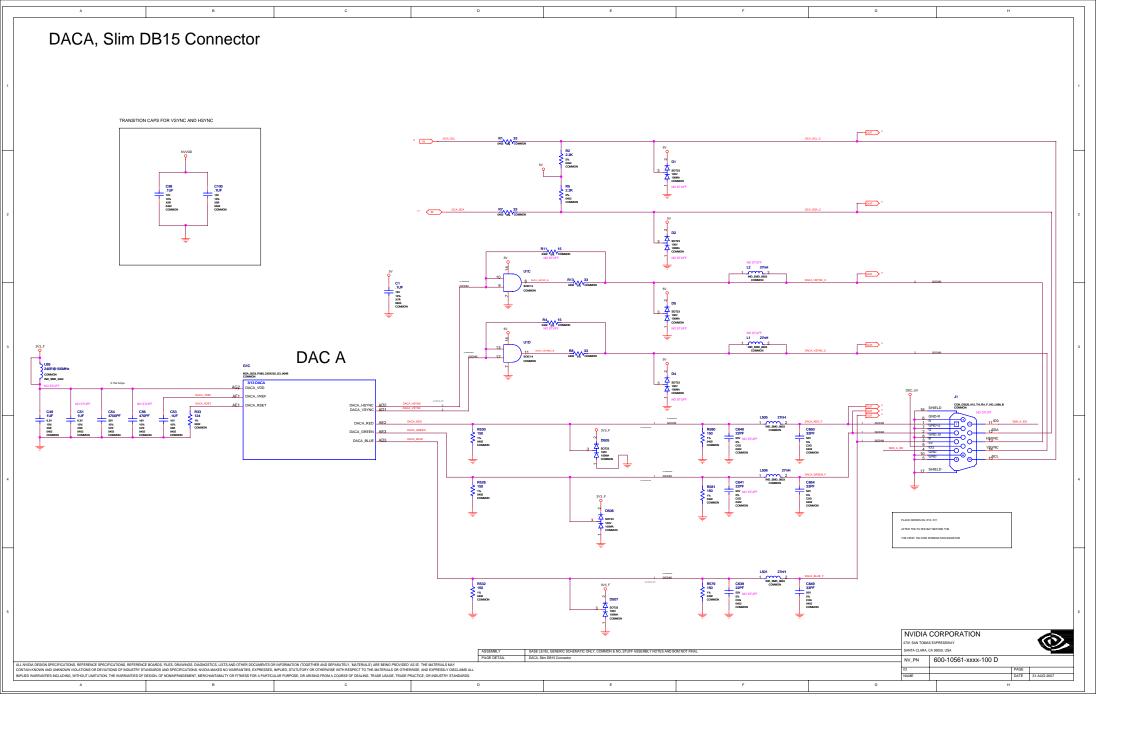
L NIVIDA DESIGNI SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FLES, DANIMINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS ON REPORTANTION (FOGETHER AND SEPARATELY, MATERIALS) ARE BERING PROVIDED AS IS: THE MATERIALS MAY ANTIAN NORMAN ADVINIONIUM WITHOUT MATERIALS ON DISCISTIFS STRANGERS AND SPECIFICATIONS. WICH AMERS AN INVASITIES, SEPARESSED, IMPLIES, STATUTION OF INTERSPECT THE MEMBERS LIGHT INTERSPECT THE MEMBERS LIGHT INTERSPECT AND SEPARATELY, MATERIALS, AND THE SEPARATELY, MATERIALS, AND THE SEPARATELY AND THE SEPARATELY OF INTERSPECT AND THE SEPARATELY AND FROM THE SEPARATELY AND THE SEPARATELY

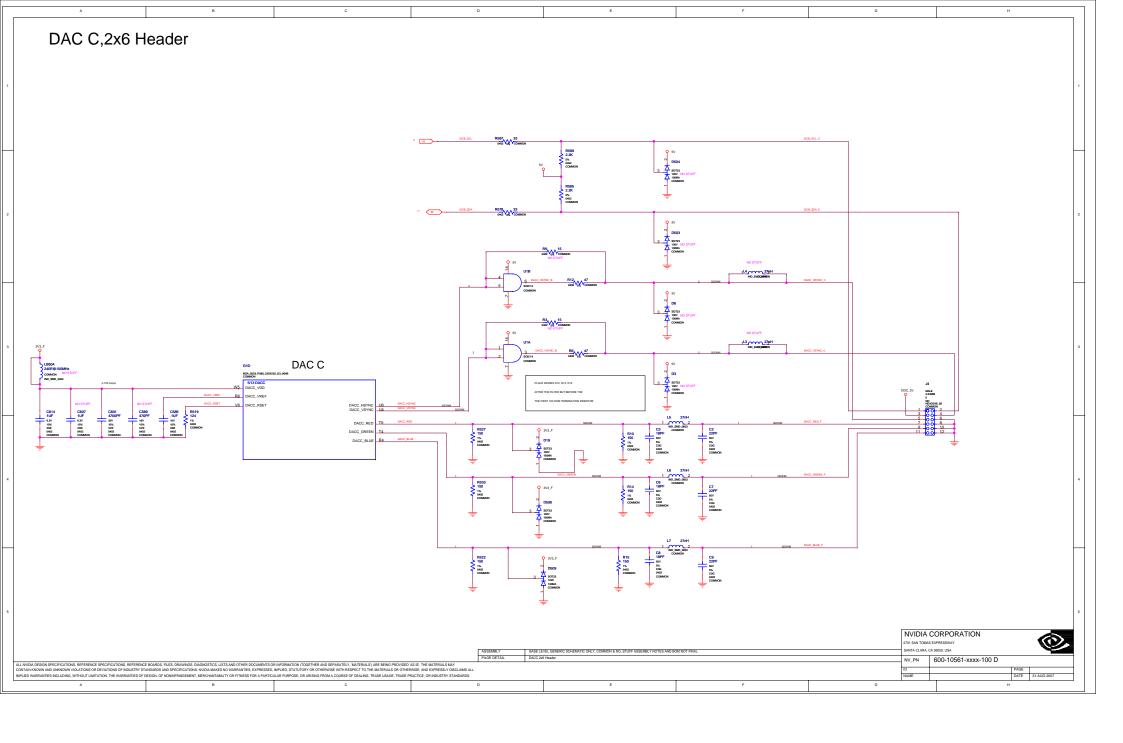


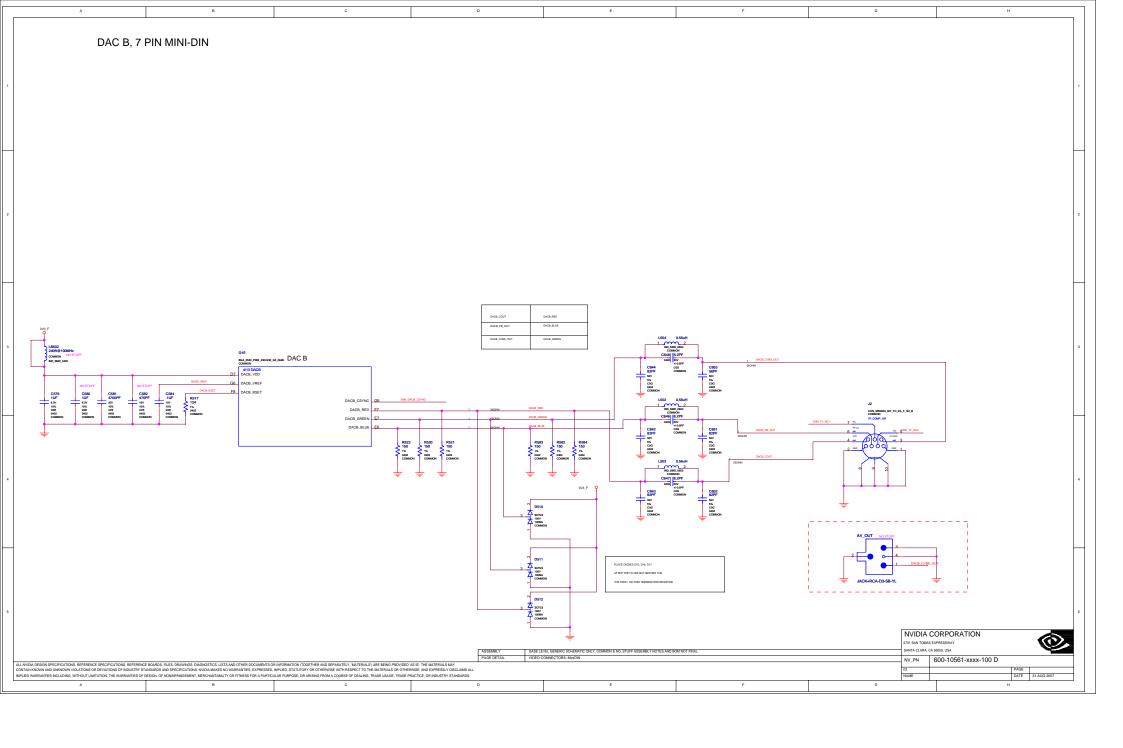


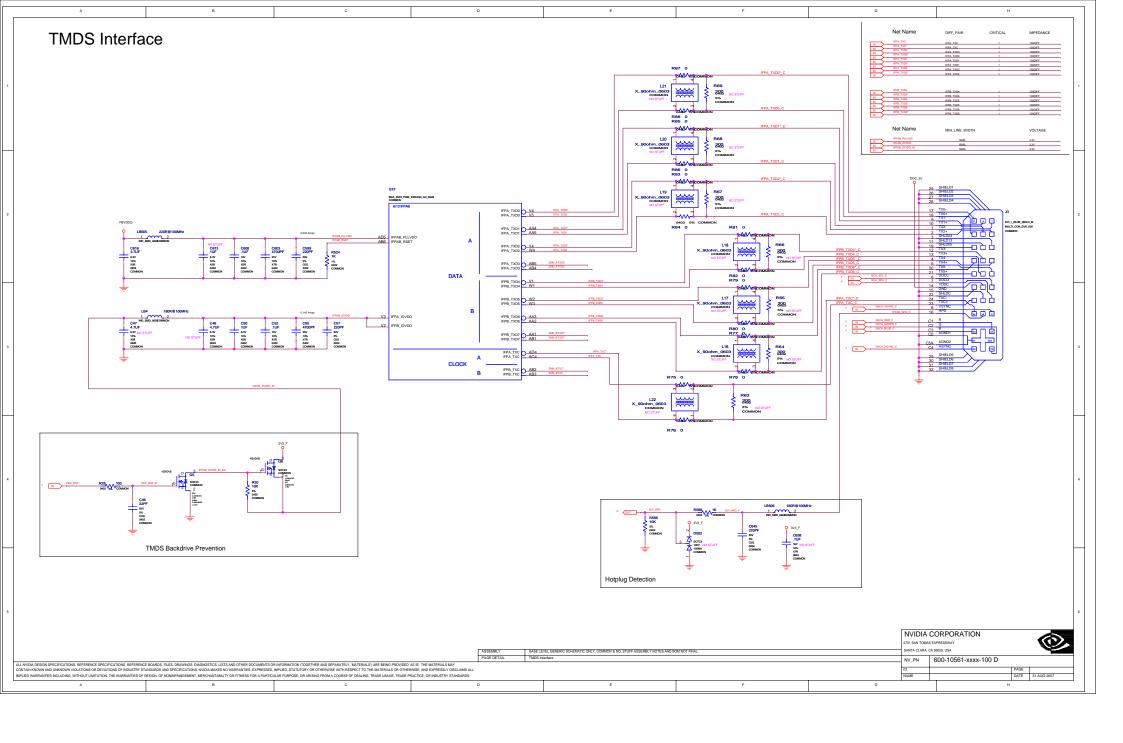


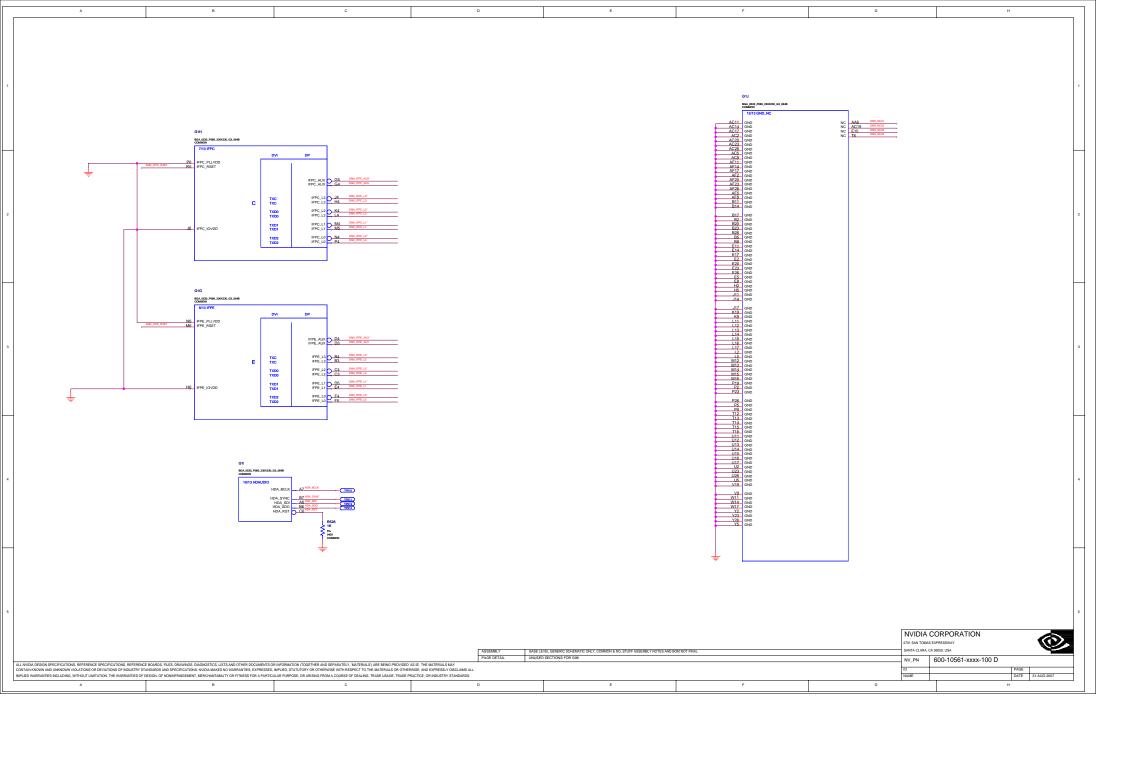




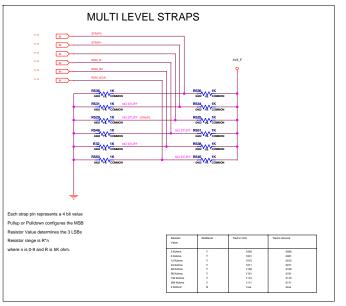














# MATILITIES MODE SEMPLO, M. (2004) (1970), e-66 SEMILITIES MODE (1970), 600 FARCTON STMUPS STMUPS SEMILITIES MODE (1970), 600 SEMILITIES MODE (1970), 600

BRINGUP BINARY MODE	STRAP_CAL_PU_GND1 ( RS11) = NO STUFF
SIGNAL	FUNCTION
STRAPIQ	3G10_PADCFG_LUT_ADR(0)
STRAP[1]	3G10_PADCFG_LUT_ADR(1)
STRAP(2)	3G10_PADCFG_LUT_ADR(2)
ROM_SCLK	3G10_PADCFG_LUT_ADR(3)
ROM_SI	SUB VENDOR
ROM SO	XCLK 277

PRODUCTION BINARY MODE	STRAP_CAL_PU_GND1 ( RS11) = 40K
SIGNAL	FUNCTION
STRAPJOJ	RAMCFG[0]
STRAP[1]	RAMCFG[1]
STRAP[2]	RAMCFG[2]
ROM_SCLK	PCI_DEVID(I)
ROM_SI	POLDEVID_EXT
ROM SO	NOLK 277

#### STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz ( MULTI LEVEL) R511= 40K, R512=40K

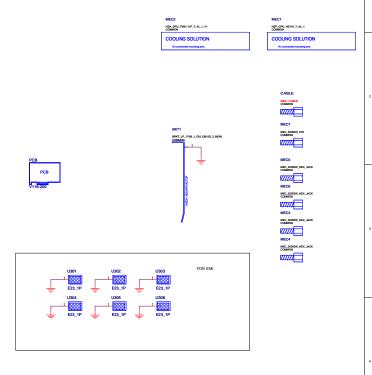
3V3_F	.	GND	PIN(SIGNAL)	FUNCTION
		5K 5K 25K 25K	STRAP(II) STRAP(II) STRAP(II) ROM, SCLK	USER[1,0] SGO_PICCEG_LUT_NOR[1,0] PCL_SENIGD_4] PCL_SENIGD_4 SCO_SENIGD_5T_SEN_VENIGOR_5LOT_CUX_CEG_PEX_PLL_DR_TERMINO
25K		45K	ROM_SI ROM_SO	RAMCFQL.0  XCLK_277, TVMCDEI[2.0]

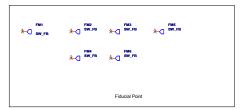
#### STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz ( BRINGUP BINARY) R511= NO STUFF, R512=NO STUFF

3V3_F	GND	PIN(SIGNAL)	FUNCTION						
9K 9K	SK SK SK SK	STRAP[0] STRAP[1] STRAP[2] ROM_SCLK ROM_S ROM_SO	SOIL PRODUCT LETT, FAMILY SOIL PRODUCTS, LETT, FAMILY						

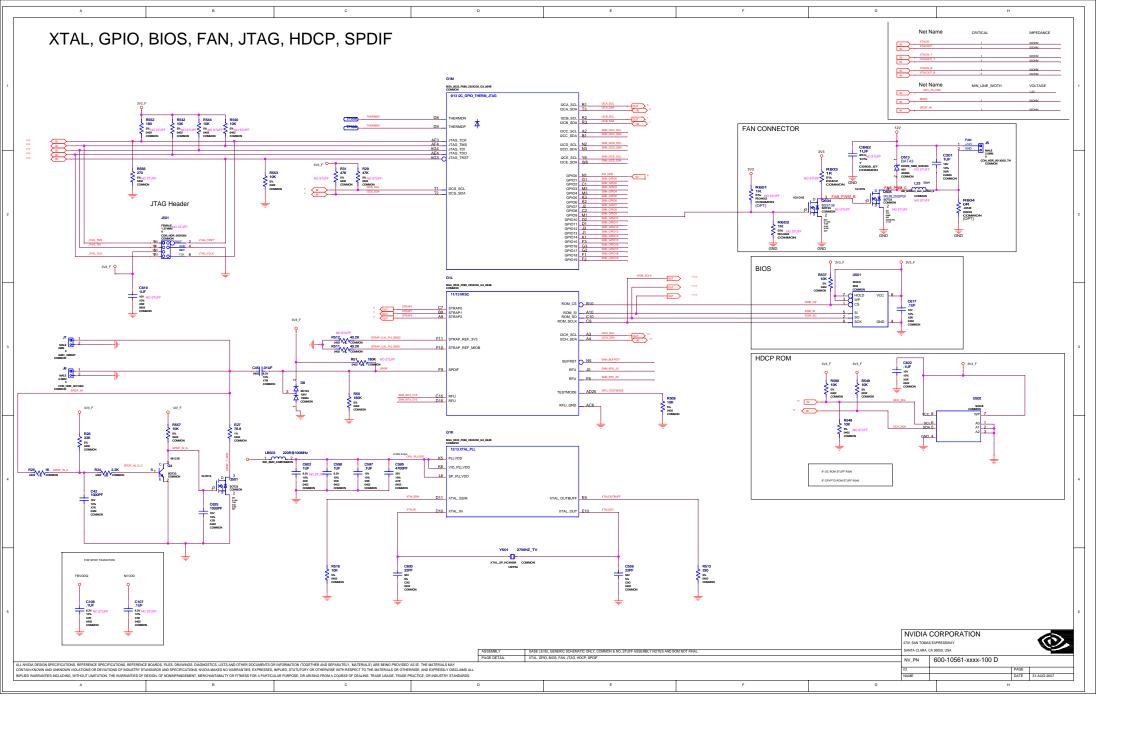
#### STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz ( PRODUCTION BINARY) R511= 40K, R512= NO STUFF

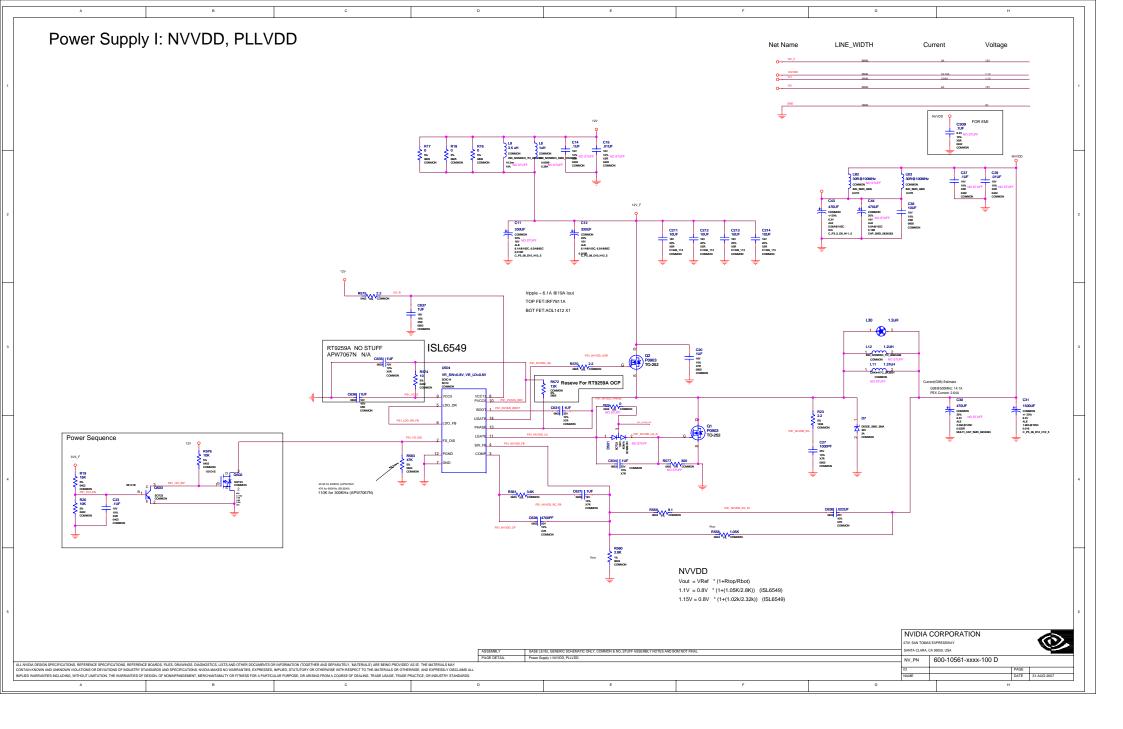
3V3_F	GND	PIN(SIGNAL)	FUNCTION
SK SK		STRAP[0]	RAMCFG[0]
SK		STRAP[1]	RAMCFG[1]
sk		STRAP[2]	RAMCFG[2]
	SK	ROM_SCLK	PCI_DEVID[3]
	SK	ROM_SI	PCI_DEVID_EXT
SK		ROM_SO	XCLK_277



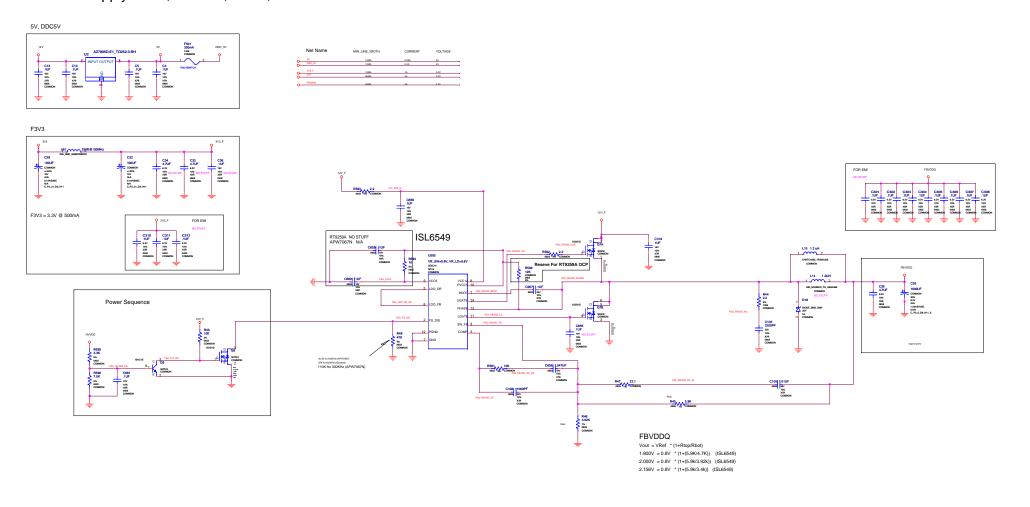


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								SANTA CLARA	CA 95050, USA 600-10561-xxxx-100 D		
	PAGE DETAIL Straps, Mechanical Parts										
CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STA	FIGUR DESIGN SPECIFICATION, REFERENCE SPECIFICATION, REFERENCE SECREPACION, SECREPACE SPECIFICATION, SEFERENCE SPECIFICAT										
LED WARRANTES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONPRINGEISMENT, MERCHANTABILITY OF RTHESS FOR A PARTICULAR PLRPPOSE, OR ARSING PROMA COURSE OF DELANG, TRADE USAGE, TRADE PRACTICE, OR INCUSTRY STANDARDS.									DATE 31-AUG-2007	007	
A	В	C	D		E	F	G		н		





## Power Supply II: 5V, DDC5V, F3V3, FBVDDQ



Title: Basenet Report
Design: p561
Date: Aug 15 1:38:59 2007 5.28 5.2C FBA\_CMD<19> 3.3C 3.3F 4.28 4.2C PS1\_12V\_EN\* 13.4B PS1\_FS\_DIS 13.4C 3.48 4.1G 4.4D PEX\_RX4 5.2B 5.2C FBA DQS<3> 3.48 4.1G 4.4D PEX RX4° 23C 2.4Ac PS1 LDO DR FB 13.4C SNN IZCE SDA 12.2E FBA\_CMD-20> 3.9C 3.3F 4.2B 4.2C 5.2B 5.2C FBA CMD<21> 3.3C 3.3G 4.2B 4.2C pd61 lib.P561(Rp561 lib.p561(sch 1) FBA DQS<6> 3.48 5.1G 5.4D PEX\_RX6\* 2.3C 2.5A PS1 NVVDD DR 13.4E SNN\_IFPC\_L0 10.2C SNN\_IFPC\_L0\* 10.2C Base Signal Location([Zone][dir] 5.2B 5.2C FBA\_DQS<7> 3.48 5.1G 5.4D 2.3C 2.5Ac PS1\_NVVDD\_FB 13.4D FBA\_CMD<23> 3.9C 3.9G 428 420 FBA\_CMD<23> 3.9C 3.4F 428 420 PEX\_RX7
PEX\_RX7\*
PEX\_RX8 PS1\_NVVDD\_LG 13.4D PS1\_NVVDD\_LG\_D 13.4E PS1\_NVVDD\_PHASE 13.3E SNN\_IFPC\_L1 10.2C SNN\_IFPC\_L1\* 10.2C SNN\_IFPC\_L2 10.2C FBA\_DQ8N<7.0> 3.4A<>4.1G<4.4A</br> 5.2B 5.2C 5.1G< 5.4A< 2.4C 2.5Ac 3V3 14.1G 3V3\_F 14.1G 5V 14.1G 12V 13.1F 12V\_F 13.1F 12V\_PS2\_R 14.2C 12V\_R 13.3C DACA\_BLUE 6.4C FBA\_CMD<24> 3.3C 3.4F 4.2B 4.2C FBA\_CMD<25> 3.3C 3.4G 4.1B 4.1C FBA\_DQSN<1> 3.48 4.1G 4.4B FBA\_DQSN<2> 3.48 4.1G 4.4D FBA\_DQSN<3> 3.48 4.1G 4.4D PEX\_RX8\* PEX\_RX9 PS1\_NVVDD\_RC 13.4F PS1\_NVVDD\_RC\_FB 13.4D SNN\_IFPC\_L2\* 10.2C SNN\_IFPC\_L3 10.2C SNN\_IFPC\_L3\* 10.2C 5.1B 5.1C PEX\_RX9\* 2.4C 2.5Ac PS1\_NVVDD\_RC\_IN 13.4F FBA CMD<27> 3.3C 3.4G 4.2B 4.2C FBA DQSN<4> 3.48 5.1G 5.46 PEX RX10 2.4C 2.5Ac PS1\_NVVDD\_UG 13.3D SNN IFPC RSET 10.2A FBA\_DQSN-55> 3.48 5.1G 5.48 FBA\_DQSN-65> 3.48 5.1G 5.4D FBA\_DQSN-7> 3.48 5.1G 5.4D PEX\_RX10° PEX\_RX11° PEX\_RX11° PS1\_NVVDD\_UGR 13.3E PS1\_PVCC5\_DRV 13.3D PS1\_VCC5 13.3C SNN\_IFPE\_AUX 10.3C SNN\_IFPE\_AUX\* 10.3C SNN\_IFPE\_L0 10.3C 5.28 5.2C 528 52C FBA\_D<0> 3.18 4.38 FBA\_D<32.0> 4.3A<> 2.4C 2.5A DACA BLUE F 6.4G> 9.3G< 3.1Ac> 4.1G< 5.3Ac FBA PLLAVDD 3.5C PEX RX12 2.4C 2.5Ac PS2 12V EN 14.4A SNN IFPE LOT 10.3C DACA\_GREEN\_F 63G> 93G-FBA\_Dx83.0> 3.1A> 4.1G< 5.3A< FBA\_Dx1> 3.1B 4.3B PEX\_RX12\* PEX\_RX13 2.4C 2.5Ac 2.5Ac 2.5C PS2\_FBVDD\_BOOT 14:3D PS2\_FBVDD\_CP 14:4D PS2\_FBVDD\_FB 14:3D SNN\_IFPE\_L1 10.3C SNN\_IFPE\_L1 10.3C SNN IFPE L2 10.3C DACA HSYNC 6.3C FBA, D-d> 3.18 4.38 FBA, D-d> 3.18 4.48 FBA D-2> 3.18 4.38 FB\_CAL\_PD\_VDDQ 3.4C PEX RX13\* 2.5A< 2.5C PS2\_FBVDD\_LG 14.3D PS2\_FBVDD\_PHASE 14.3D 14.3E 14.3F PS2\_FBVDD\_RC 14.3F DACA HSYNC B 62D PEX\_RX14 2.5A< 2.5C SNN IFPE L2\* 10.3C DACA\_HSYNC\_C 62G>93G4 DACA\_RED 64C FB\_CAL\_PU\_GND 3.4C FB\_CAL\_TERM\_GND 3.4C PEX\_RX14\* SNN\_IFPE\_L3 10.3C SNN\_IFPE\_L3 10.3C PEX\_RX15 2.5A< 2.50 SNN\_IFPE\_RSET 10.3A SNN\_NC01 10.1G SNN\_NC02 10.1G SNN\_NC03 10.1G DACA RED F 6:3G> 9:3G-FB VREF 3.5B PEX RX15\* 2.5A< 2.5C PS2 FBVDD RC FB 14.4D FB\_VREF 3.5B

GND\_SENSE 2.4F

GPU\_PLLVDD 12.1G<12.4C

GPU\_TESTMODE 12.3E PEX\_SMCLK PEX\_SMDAT PS2\_FBVDD\_RC\_IN 14.4F PS2\_FBVDD\_UG 14.3D DACA\_VSYNC 6:3C PEX\_TSTCLK 2.2Ac PS2\_FBVDD\_UGR 14:3E DACA VSYNC C 63G> 93G+ HDA\_BCLK 10.4C PEX TSTCLK\* 2.2Ac PS2\_FS\_DIS 14.3C PS2\_LDO\_DR\_FB 14.3C PS2\_NVVDD\_EN 14.4A SNN NC04 10.1G DACA\_VSYSNC\_B 6.3D DACB\_BLUE 8.4D HDA\_RST HDA\_SDI PEX\_TSTCLK\_OUT 2:5F 10.4C DACB COUT 8.4F HDA SDO PEX TX0 2.2A<2.2E PS2 PVCC5 DRV 14.3D SNN PE PRSNT2 B 2.2B HDA SYNC 10.4C DACB CVBS OUT 8:3F 8:4G PEX TX0\* 2.2A<2.2E PS2 VCC5 14.3C SNN PE PRSNT2 C 2.38 DACB\_GREEN 8.4D DACB\_PB\_OUT 8.4F FBA\_D<16> FBA\_D<16> FBA\_D<17> I2CA\_SCL 6.1D<12.1E> I2CA\_SCL\_C 6.1G>9.2G< PEX\_TX1
PEX\_TX1\*
PEX\_TX2 ROM\_CS\* 12.3E 12.3F ROM\_SCLK 11.1A<11.1 11.1A< 11.1A< 12.2F DACB RED 8.3D 3.2B 4.3D I2CA SDA 62D-0 12.1E-0 2.2A<2.2E 12.2F> 12.2F> SNN PE RSVD4 2.2B 12.2F> 12.2F> ROM SI 11.1Ac 11.1Ac 12.3F> FBA\_D<18> 328 430 328 430 PEX\_TX2\* PEX\_TX3 DACB RSET 8.38 I2CA SDA C 62G> 9.3G< 2.2A< 2.2E SNN PE RSVD5 2.2B I2CB\_SCL DACC\_BLUE\_F 7.4C 7.4E DACC\_BLUE\_F 7.4F FBA\_D<20> 3.2B 4.3D 3.2B 4.3D 12CB\_SCL\_C 7.1F PEX\_TX3\* PEX\_TX4 2.2A< 2.3E ROM\_SO 11.1Ac 11.1Ac 12.3Fs SNN\_PE\_RSVD7 2.4B SNN\_PE\_RSVD8 2.4B IZCB SDA 7.2D to 12.1E to 2.2A<2.3E 12.3F> 12.3F> 12.3F> 12.3F>
SNN\_3V3AUX 2.1B
SNN\_ATXD3 9.2E
SNN\_ATXD3\* 9.2E FBA\_D-22> FBA\_D-23> FBA\_D-24> 3.28 4.3D 3.28 4.3D PEX\_TX8\* PEX\_TX8\* SNN\_RFU\_AE9 2.2E SNN\_RFU\_AG9 2.5F SNN\_RFU\_C15 12.3C 12CB SDA C 7.2F DACC\_HSYNC 7.3C 3.2B 4.4D 12CH\_SDA 12.3E⇔ 12.3F< 2.2A< 2.3E SNN\_ATXD3\* 9.2E SNN\_A\_ID0 6.4H SNN\_A\_ID2 6.4G SNN\_BTXC 9.3E SNN\_BTXC\* 9.3E SNN\_BTXD7 9.3E DACC\_HSYNC\_B 7.2D DACC\_HSYNC\_C 7.2F DACC\_RED 7.4C 7.4E FBA\_D<26> FBA\_D<26> FBA\_D<27> FBA\_D<28> FBA\_D<29> 3.28 4.4D 3.28 4.4D 3.28 4.4D I2CS\_SCL 2.1E-> 12.2C->
I2CS\_SDA 2.1E-> 12.2C->
IFPAB\_HPD\_C 9.9G PEX\_TX8
PEX\_TX8\*
PEX\_TX7 2.2A<2.3E 2.2A<2.3E 2.2A<2.3E SNN\_RFU\_D15 12:3C SNN\_RFU\_F6 12:3E SNN\_RFU\_J5 12:3E PEX\_TX7\* PEX\_TX8 SNN\_RFU\_J22 3.3C SNN\_RFU\_J22 3.3C DACC RED F 7.4F 3.2B 4.4D IFPAB IOVDD 9.1G< 9.3C 2.2A<2.3E DACC RSET 7.38 3.2B 4.4D IFPAB IOVDD IN 9.2G< 9.3B 23A<2.4E DACC\_VREF 7.38 DACC\_VSYNC 7.9C FBA\_D<30> 3.28 4.4D 3.28 4.4D IFPAB\_IOVDD\_IN\_EN 9.48 IFPAB\_PLLVDD 9.1Gc 9.2C PEX\_TX8\* PEX\_TX9 SNN\_TV\_NC1 8.4G SNN\_TV\_NC2 8.4G DACC\_VSYNC\_B 7.3D DACC\_VSYNC\_C 7.3F FBA\_D<32> FBA\_D<33> FBA\_D<34> 3.28 5.38 3.28 5.38 3.28 5.38 #PAB\_RSET 9.2C #PA\_TXC 9.1G<9.3E 9.3G #PA\_TXC\* 9.1G<9.3E 9.3G PEX\_TX0\* PEX\_TX10\* PEX\_TX10\* SNN\_DACB\_CSYNC 8.3C SNN\_FBA1\_NC\_A2 4.3B SNN\_FBA1\_NC\_E2 4.3B SPDIF 12.1G< 12.3C SPDIF\_IN 12.1G< 12.3A 12.3A SPDIF\_IN\_C 12.4A 2.3A<2.4E 2.3A<2.4E DVI\_HPD 9.3E> 12.2E< DVI\_HPD\_F 9.3F FBA\_D<35> 3.2B 5.3B 3.2B 5.3B IFPA\_TXD0 9.1G< 9.2E 9.20 PEX\_TX11
PEX\_TX11\* 2.3A<2.4E SNN\_FBA1\_NC\_R3 4.28 SNN\_FBA1\_NC\_R7 4.28 SPDIF\_IN\_G 12.48 SPDIF\_IN\_G\_C 12.4A IFPA TXD0\* 9.1G< 9.2E 9.2 2.3A< 2.4E SNN\_FBA1\_NC\_R8 4.2B SNN\_FBA2\_NC\_A2 4.3C SNN\_FBA2\_NC\_E2 4.3C SPDIF\_T\_GND 12.4B STRAP0 11.1A< 11.1A< 12.90 FBA\_CLK0\* 3.3D 3.4D> 4.1G< FBA\_Dol0> FBA\_Dol0> 3.2B 5.3B IFPA\_TXD2 9.1G< 9.2E 9.2G PEX\_TX13 2.3A< 2.5E STRAP1 11.1Ac 11.1Ac 12.3Co 4.2A< 4.2C< 4.5B< FBA\_CLK1 3.3D 3.4D>5.1G IFPA\_TXD2\* IFPB\_TXD4 9.1G< 9.2E 9.26 9.1G< 9.2G 9.38 PEX\_TX13\* PEX\_TX14 SNN\_FBA2\_NC\_R3 4.2C SNN\_FBA2\_NC\_R7 4.2C 11 1Ac 11 1Ac 12 30 5.2A< 5.2C< 5.5B< FBA\_CLK1\* 3.3D 3.4D> 5.1G< IFPB\_TXD4\* IFPB\_TXD5 PEX\_TX14\* PEX\_TX15 FBA\_D+42> 3.28 5.48 3.28 5.48 9.1G< 9.2E 9.2G 9.1G< 9.2G 9.3E 2.3A< 2.5E SNN\_FBA2\_NC\_R8 4.2C SNN\_FBA3\_NC\_A2 5.3B STRAP\_CAL\_PU\_GND1 12:3C 2.3A< 2.5E THERMDA 3.28 5.48 3.38 5.48 3.38 5.48 IFPB\_TXD5\*
IFPB\_TXD6\*
IFPB\_TXD6\* 9.1G< 9.2G 9.3E 9.1G< 9.2G 9.3E 9.1G< 9.2G 9.3E PEX\_TXIS\* PEX\_TXXX PEX\_TXXX 23A< 25E 22C 23A< SNN\_FBA3\_NC\_F2 5.3B SNN\_FBA3\_NC\_R3 5.2B SNN\_FBA3\_NC\_R7 5.2B THERMOC XTALIN XTALIN\_B 5.2A< 5.2C< 5.5B< FBA\_CLK\_C0 4.5B FBA\_CLK\_C1 5.5B FBA\_CMD+0> 3.2C 3.2F 4.2B 4.2C FBA\_CMD+27.0> 3.2D> 4.1A< 4.1G< FBA\_D+47> 3.38 5.48 3.38 5.30 JTAG\_TCLK 2.1E-o 12.1A-c PEX\_TXX1
PEX\_TXX1\* 2.2C 2.3A< SNN\_FBA3\_NC\_R8 5.2B SNN\_FBA4\_NC\_A2 5.3C XTALIN\_T XTALOUT 12.1G< 12.1G< 12.4E FBA\_D<60>
FBA\_D<60>
FBA\_D<60>
FBA\_D<61>
FBA\_D<62>
FBA\_D<63> 3.38 5.30 SNN\_FBA4\_NC\_E2 5.3C JTAG\_TCLK\_PEX 2.1C PEX\_TXX2 2.2C 2.3A XTALOUTBUFF 12.4E FBA\_CMD<1> 3.2C 3.2F 4.1B 4.1C 3.38 5.3D JTAG\_TDI 2.1E-o 12.2A-o PEX\_TXX2\* 2.2C 2.3A< SNN\_FBA4\_NC\_R3 5.20 XTALOUT\_B 12.1Gc 3.38 5.3D 3.38 5.3D 3.38 5.3D PEX\_TXX3\* PEX\_TXX4\* PEX\_TXX4 23A< 23C SNN\_FBA4\_NC\_R7 5.2C SNN\_FBA4\_NC\_R8 5.2C SNN\_FBA\_CMD7 3.3C XTALOUT\_T 12.1Gc XTALSSIN 12.4C JTAG\_TDIO\_PEX 2.1C
JTAG\_TDO 2.1E-> 12.2A-> FBA\_D-d5-FBA\_D-d5-FBA\_D-d5-FBA\_D-d7-FBA\_D-d8-5.1B 5.1C 3.38 5.3D 12.2Ac> PEX\_TXX4\* 2.3A< 2.3C SNN\_FBA\_CMD26 3.3C FBA\_CMD-4> 32C 32F 52B 52C FBA\_CMD-6> 32C 32F 52B 52C 3.38 5.3D 3.38 5.4D JTAG\_TMS 2.1E 12.1Ac PEX\_TXXS
PEX\_TXXS 2.3A< 2.3C 2.3A< 2.3C SNN\_FBA\_CMD28 3.3C SNN\_GPI00 12.2E SNN\_GPI02 12.2E SNN\_GPI03 12.2E PEX\_TXX8\* FBA\_CMD-6> 3.2G 3.3C 5.2B 5.2C FBA\_CMD-8> 3.2G 3.3C 4.1B 4.1C 3.38 5.4D 3.38 5.4D 12.1Ac> JTAG\_TMS\_PEX 2.1C 2.3A< 2.3C 2.3C 2.4A< 12.2E 12.2E 12.2E 12.2E 12.2E 12.2E 12.2E 12.2E FBA\_D<60> FBA\_D<61> JTAG\_TRST\* 2.1E-o 12.2A-o
12.2A-o
JTAG\_TRST\_PEX\* 2.1C PEX\_TXX7\*
PEX\_TXX8\* 2.3C 2.4Ac 2.3C 2.4Ac SNN\_GPIOS SNN\_GPIOS 5.18.5.1C FBA\_CMD<br/>45> 3.2F 3.3C 4.18.4.1C 5.1B 5.1C 3.38 5.4D 2.4A< 2.4C SNN\_GPIO6 NVVDD 13.1F NVVDD\_SENSE 2.4F PEX\_PLLDVDD 2.5F PEX\_PRSNT 2.18 FBA CMD+10> 33C 33E 42B 42C PEX\_TXXXI
PEX\_TXXXI
PEX\_TXXXI SNN\_GPIO7 SNN\_GPIO8 SNN\_GPIO9 FBA\_D-62> 3.38 5.4D 246-240 528 5.2C FBA\_CMD<11> 3.3C 3.3D 4.2B 4.2C FBA\_D=63> FBA\_DEBUG 2.4A<2.4C 3.1G< 3.40 5.28 5.2C FBA\_DQM<0> 3.38 4.38 PEX\_TXX10 2.4A< 2.4C SNN\_GPIO10 FBA\_CMD<12> 3.3C 3.3D 4.2B 4.2C FBA\_DQM<7.0> 3.3A> 4.1G< 4.4A PEX\_REFCLK 2.2C 2.5Ac PEX\_TXX10" 2.4A<2.4C PEX\_TXX11 2.4A<2.4C PEX\_TXX11" 2.4A<2.4C SNN\_GPI011 SNN\_GPI012 SNN\_GPI013 528 5.2C FBA\_CMD<13> 3.2G 3.3C 5.1B 5.1C FBA\_CMD<14> 3.3C 3.3G 4.2B 4.2C FBA\_DQM<1> 3.3B 4.4B PEX\_RST\* 2.20> 2.20> 9.4A FBA\_DQM<2> 3.3B 4.3D PEX\_RST\_R 9.4A PEX\_TXX12 2.4A<2.4C SNN\_GPI014 12.2E 528 5.2C FBA\_CMD<15> 3.3C 3.3F 4.18 4.10 FBA\_DQM<3> 3.38 4.4D FBA\_DQM<4> 3.38 5.38 PEX\_RSVD PEX\_RX0 PEX\_RX0\* PEX\_TXX12\* PEX\_TXX13 2.4A< 2.4C 2.4A< 2.5C SNN\_GPI015 SNN\_GPI016 SNN\_GPI017 5.1B 5.1C FBA\_DQM<5> 3.38 5.48 2.2C 2.4Ac PEX\_TXX13\* 2.4A< 2.5C FBA CMD+16> 33C 33E 42B 42C FRA DOM/65 338 530 PFY RY1 220.244 PEX TXX14 2.44-2.50 SNN GPIO18 12.2F PEX\_RX1\*
PEX\_RX2\*
PEX\_RX2\*
PEX\_RX3 5.28 5.2C FBA\_CMD<17> 3.3C 3.3G 4.28 4.2C 5.28 5.2C PEX\_TXX15\* 2.4A<2.5C PEX\_TXX15\* 2.4A<2.5C PEX\_TXX15\* 2.4A<2.5C FBA\_DQS<0> 3.48 4.1G 4.48 SNN\_I2CC\_SCL 12.1E SNN\_I2CC\_SDA 12.1E 2.2C 2.4Ac FBA\_DQS<7.0> 3.4Ac> 4.1G< 4.4Ac> 2.2C 2.4Ac FBA\_CMD<18> 3.3C 3.3G 4.2B 4.2C 5 10 - 5 44 -230 244 PS1\_3V3\_EN 13.4A SNN\_I2CD\_SCL 12.1E NVIDIA CORPORATION 701 SAN TOMAS EXPRESSWA ANTA CLARA, CA 95050, USA BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL DAGE DETAIL «edit here to insert page detail» NV PN 600-10561-xxxx-100 D OWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS INVIDIA MAKES NO WARRANTIES EXPRESSED HIM/LED STATLITORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE AND EXPRESSLY DISCLAIMS ALL DATE 31-AUG-2007

