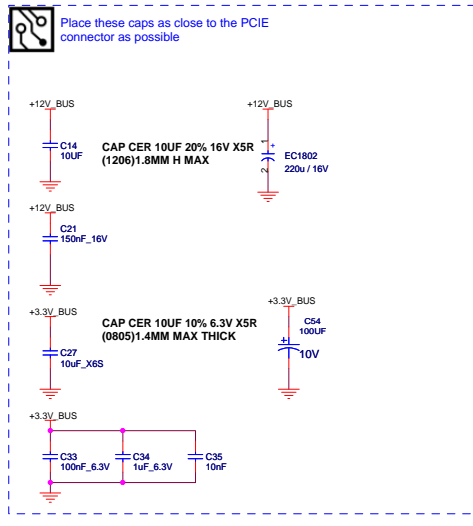
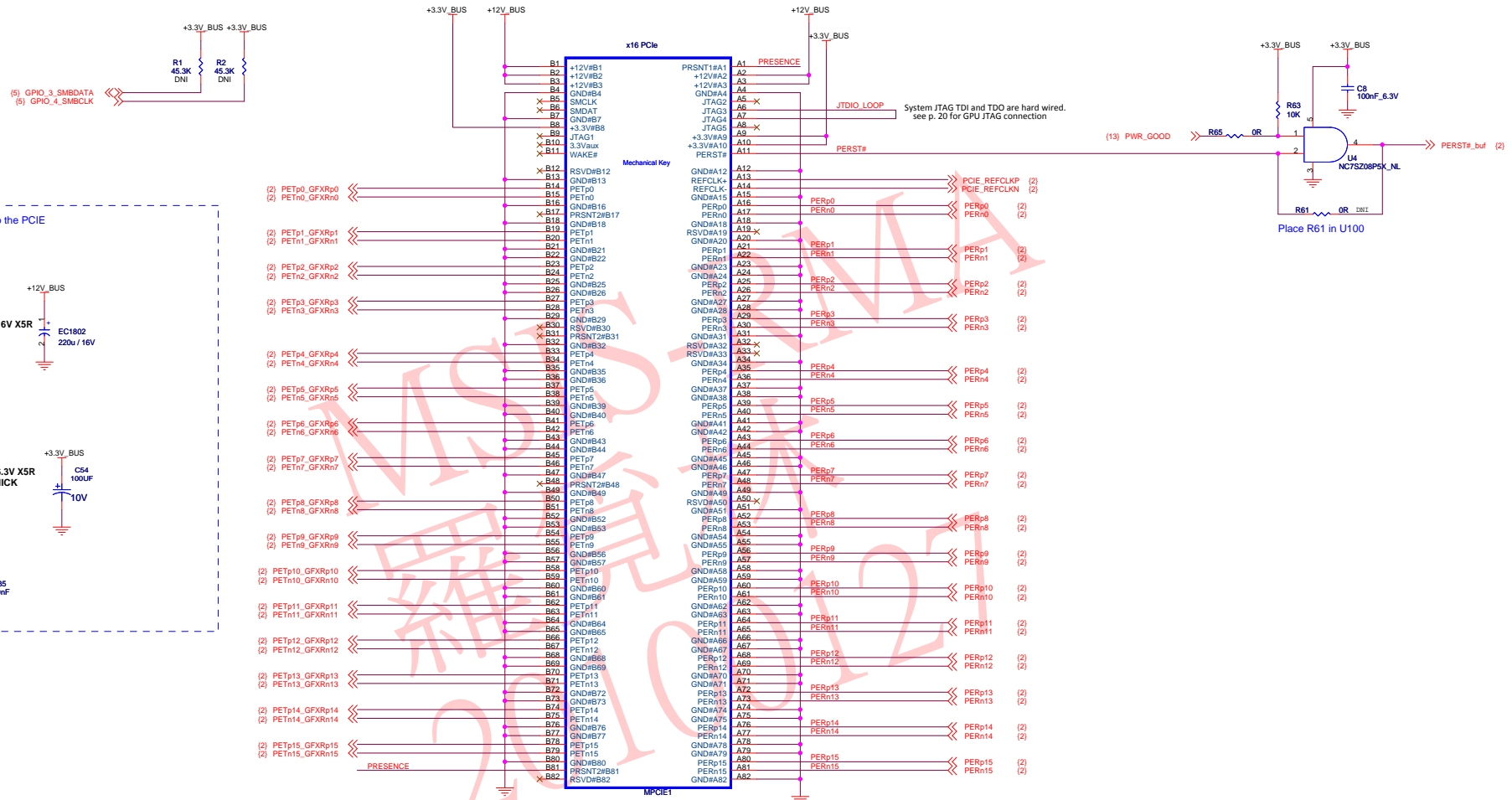


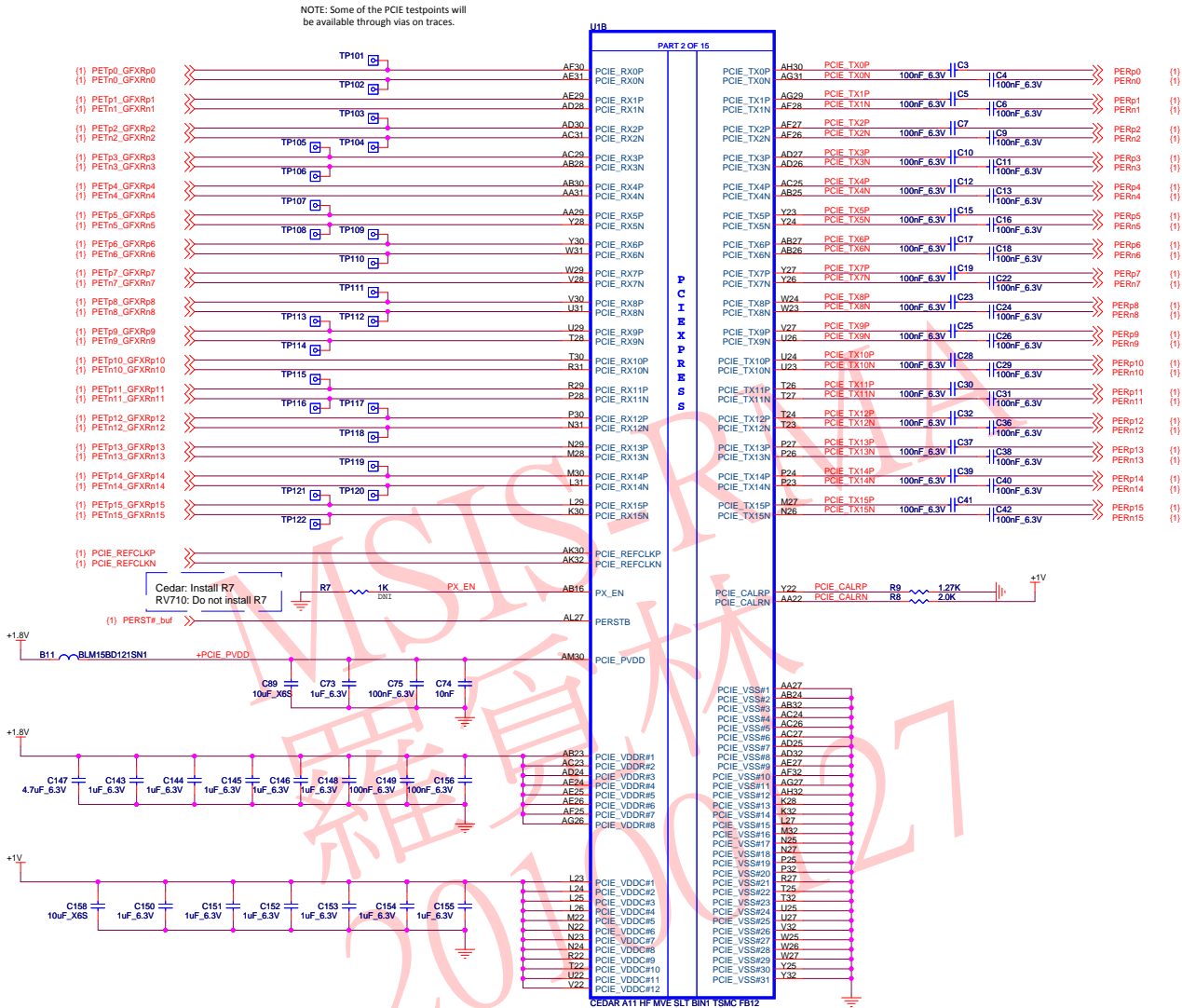
# PCI-EXPRESS EDGE CONNECTOR

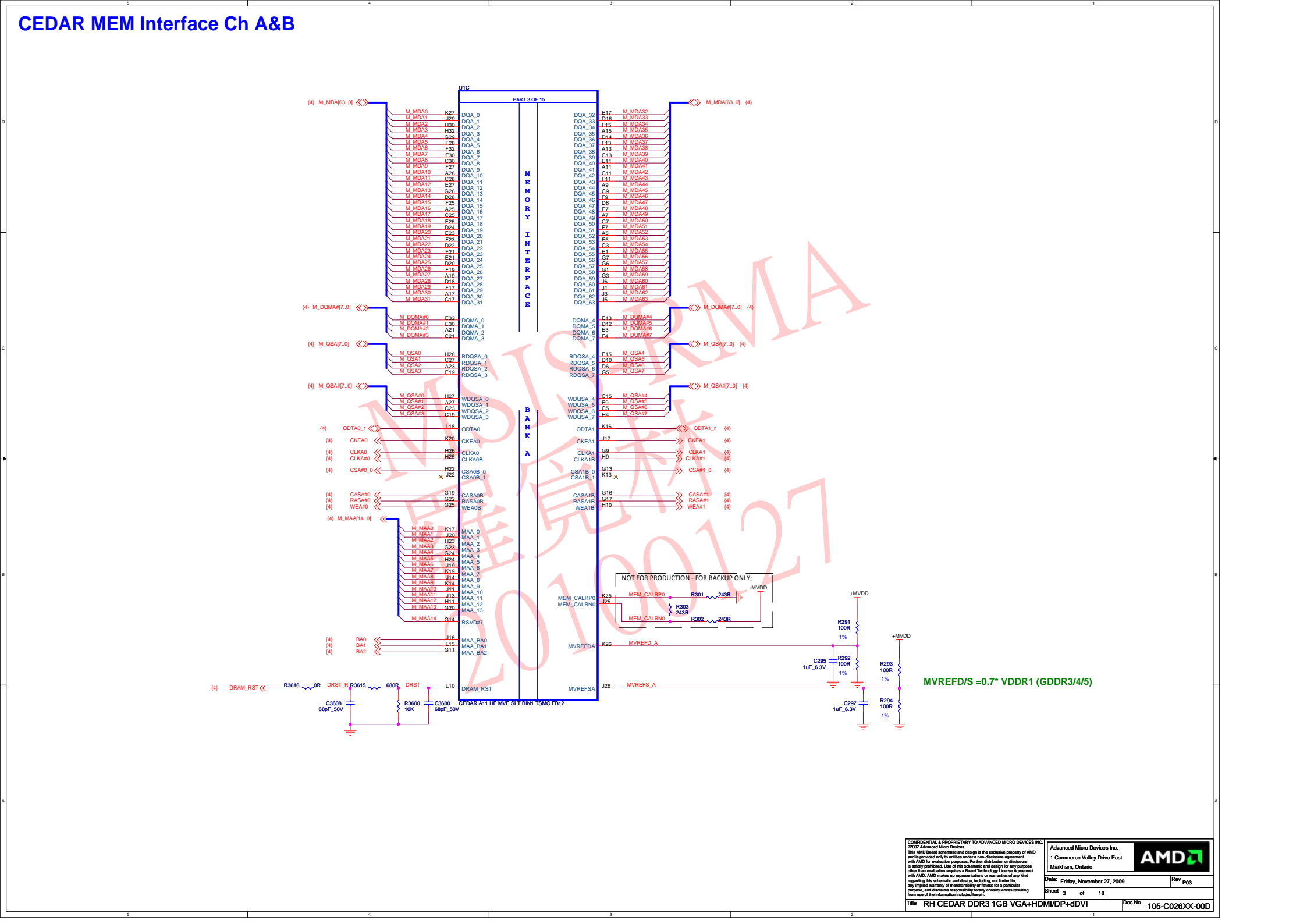
CEDAR BASS / PERCH




SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

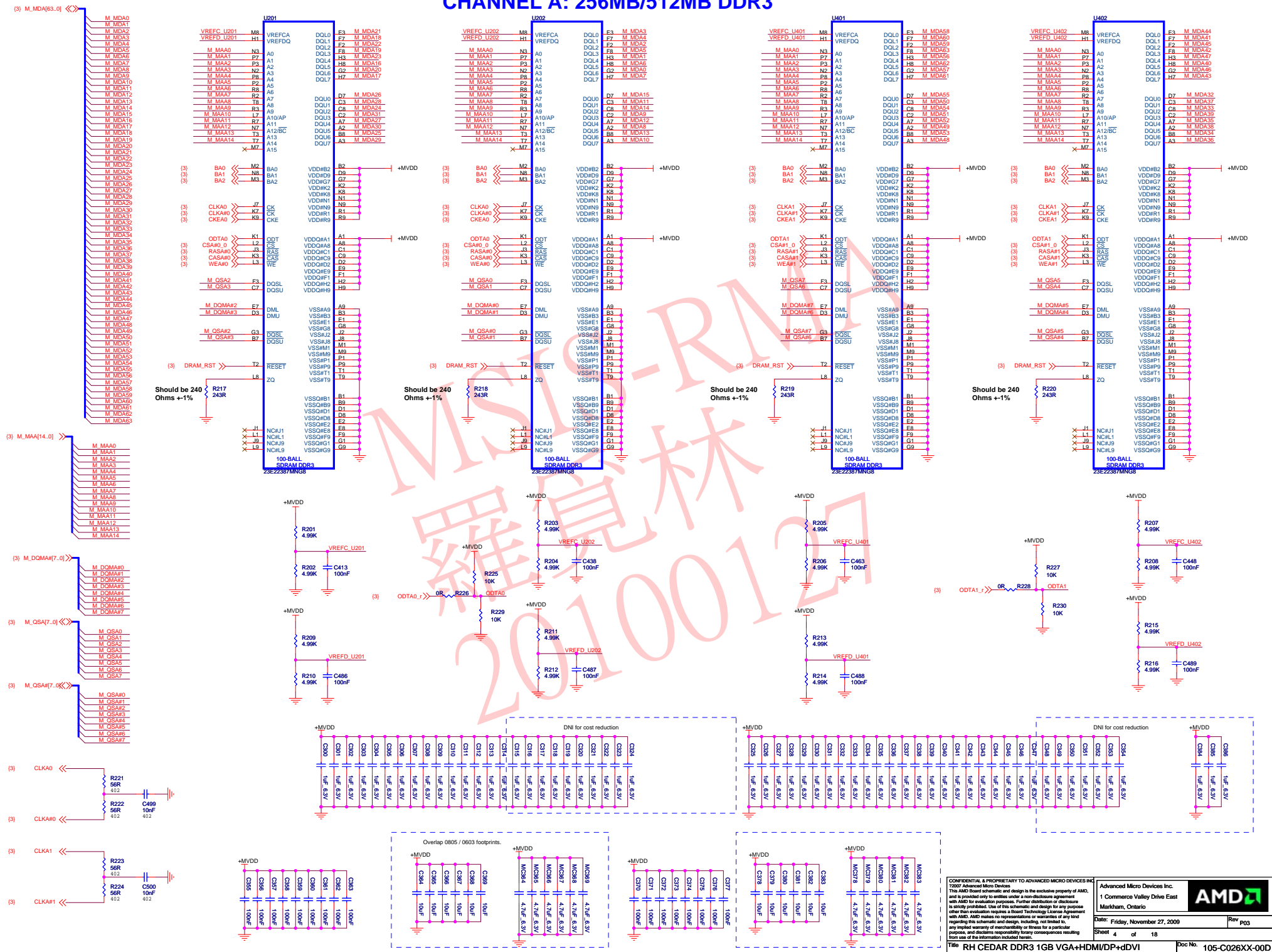
CEDAR PCIe Interface



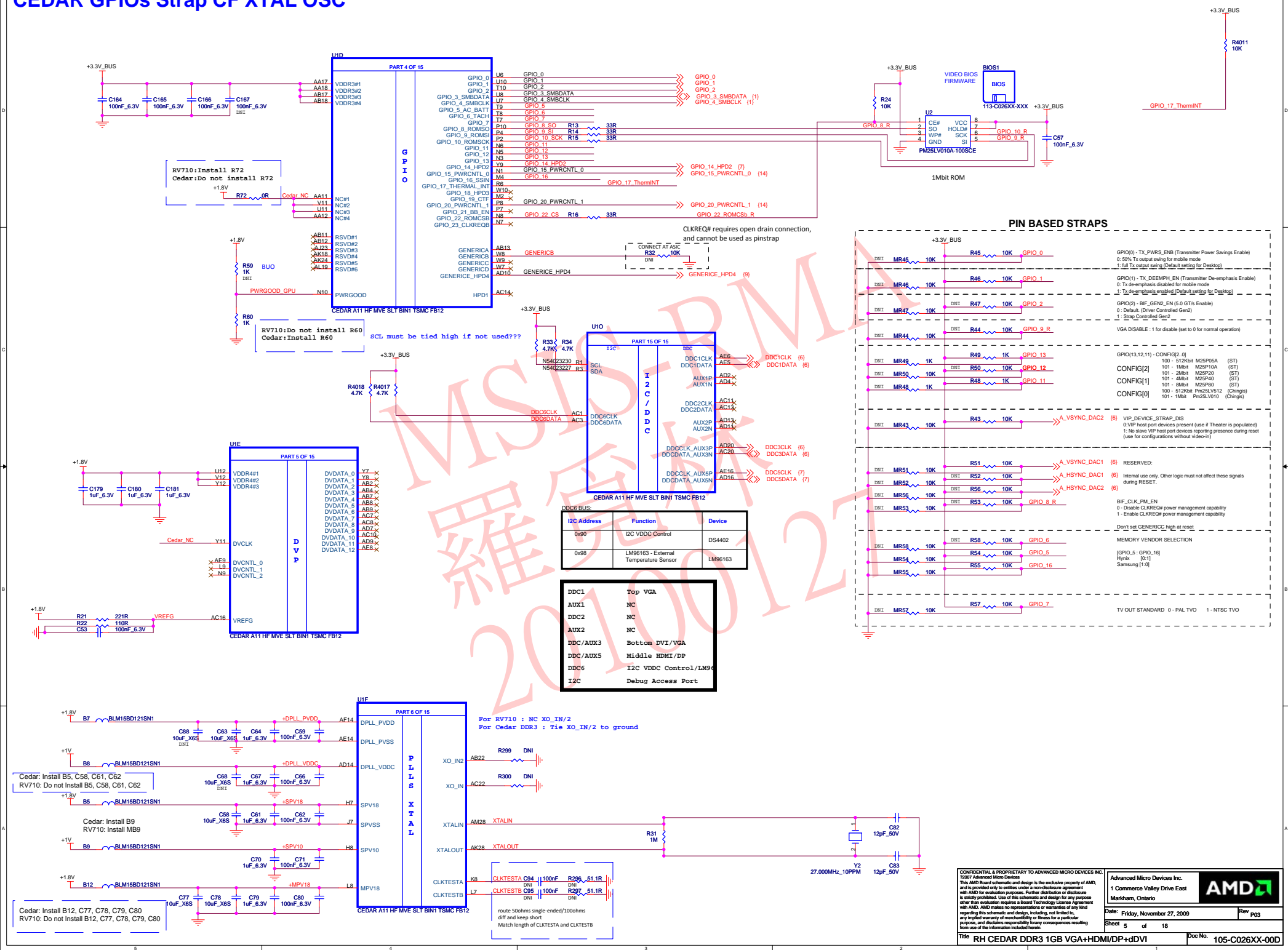
[illegible]

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Date: Friday, November 27, 2009		Rev P03	
Sheet 3	of 18		

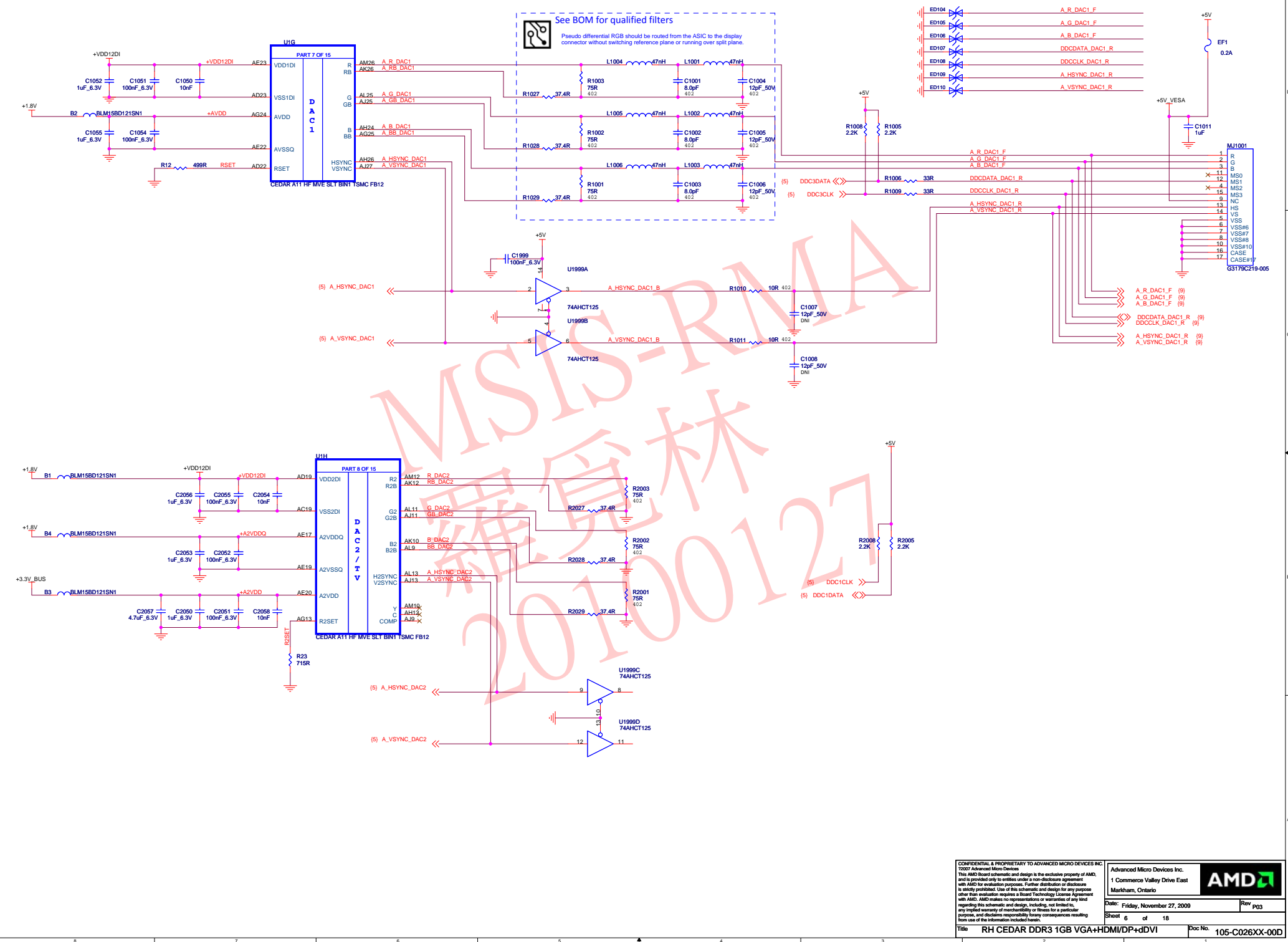
**CHANNEL A: 256MB/512MB DDR3**



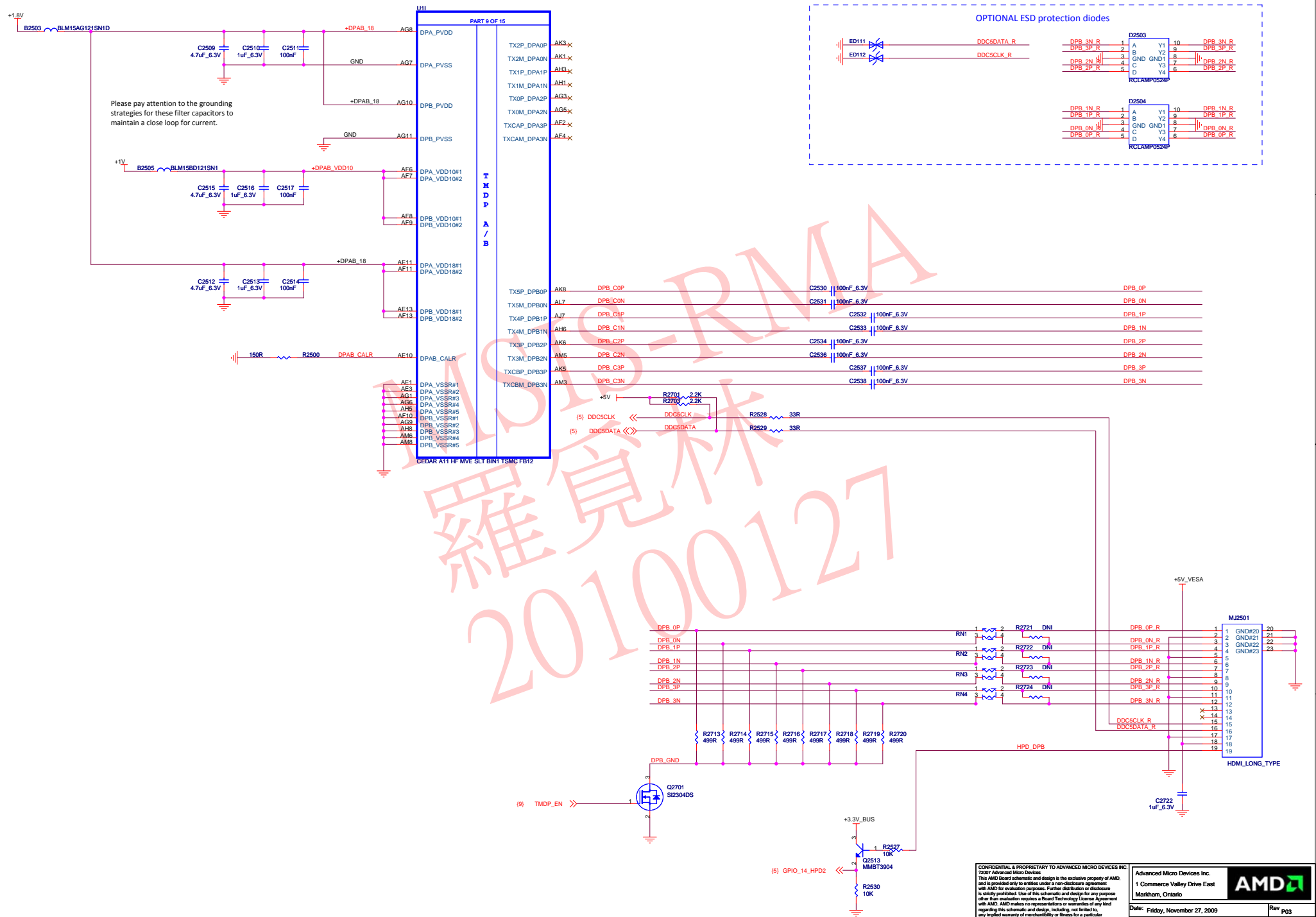
## CEDAR GPIOs Strap CF XTAL OSC



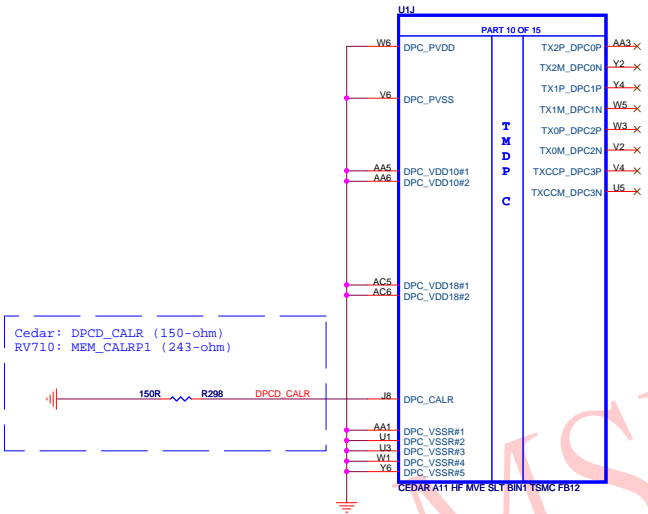
CEDAR DAC1 and DAC2



## CEDAR TMDP A&B DP/HDMI OVERLAP

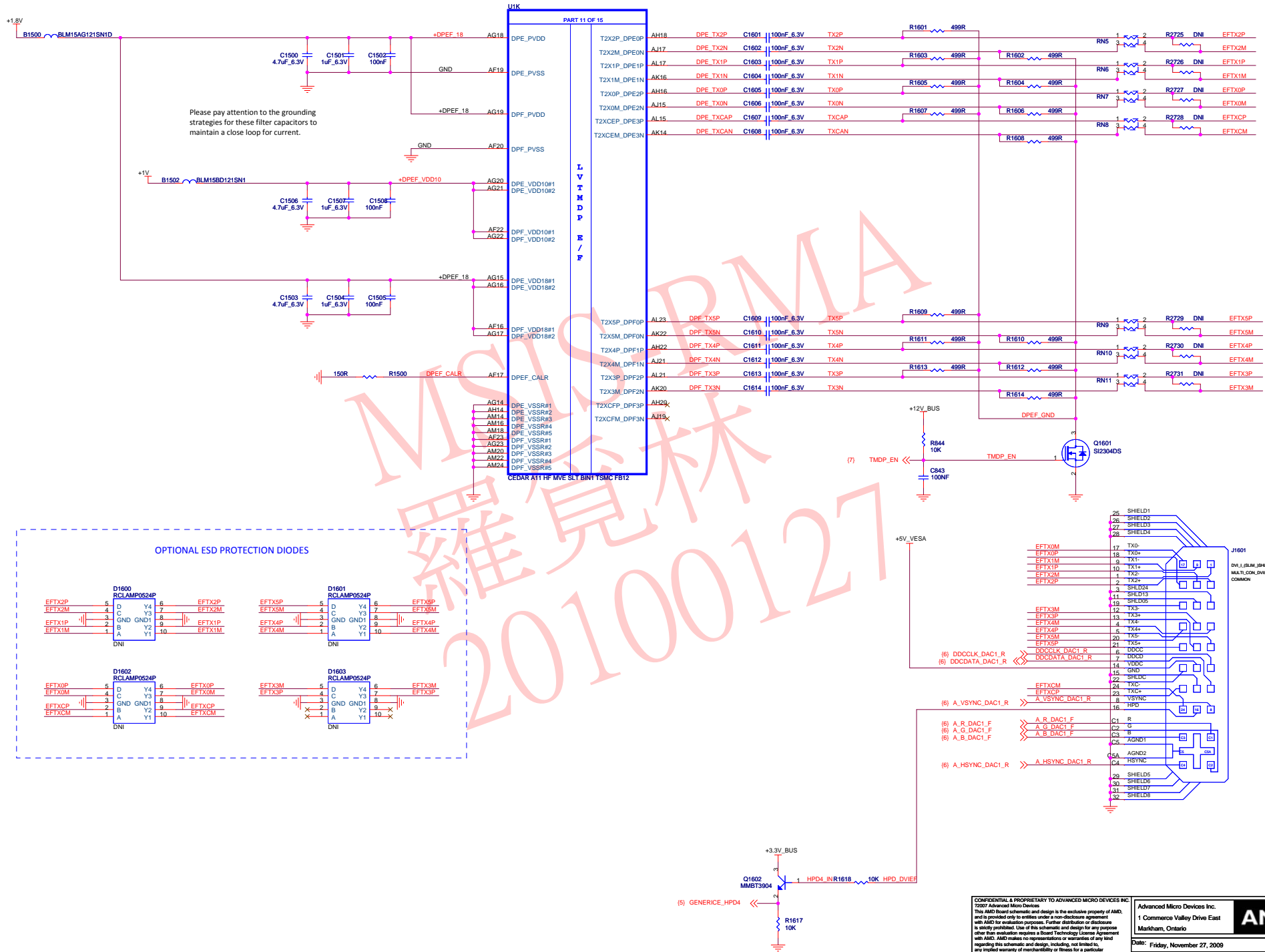


CEDAR Display Port C (Unused)

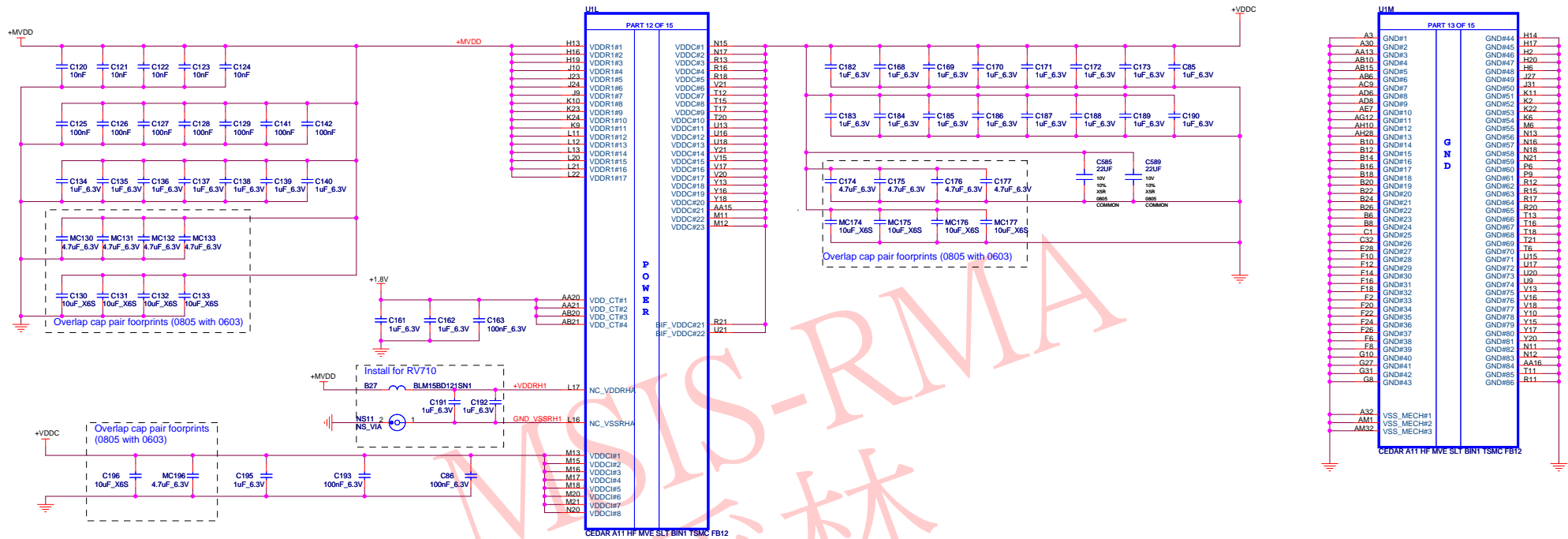




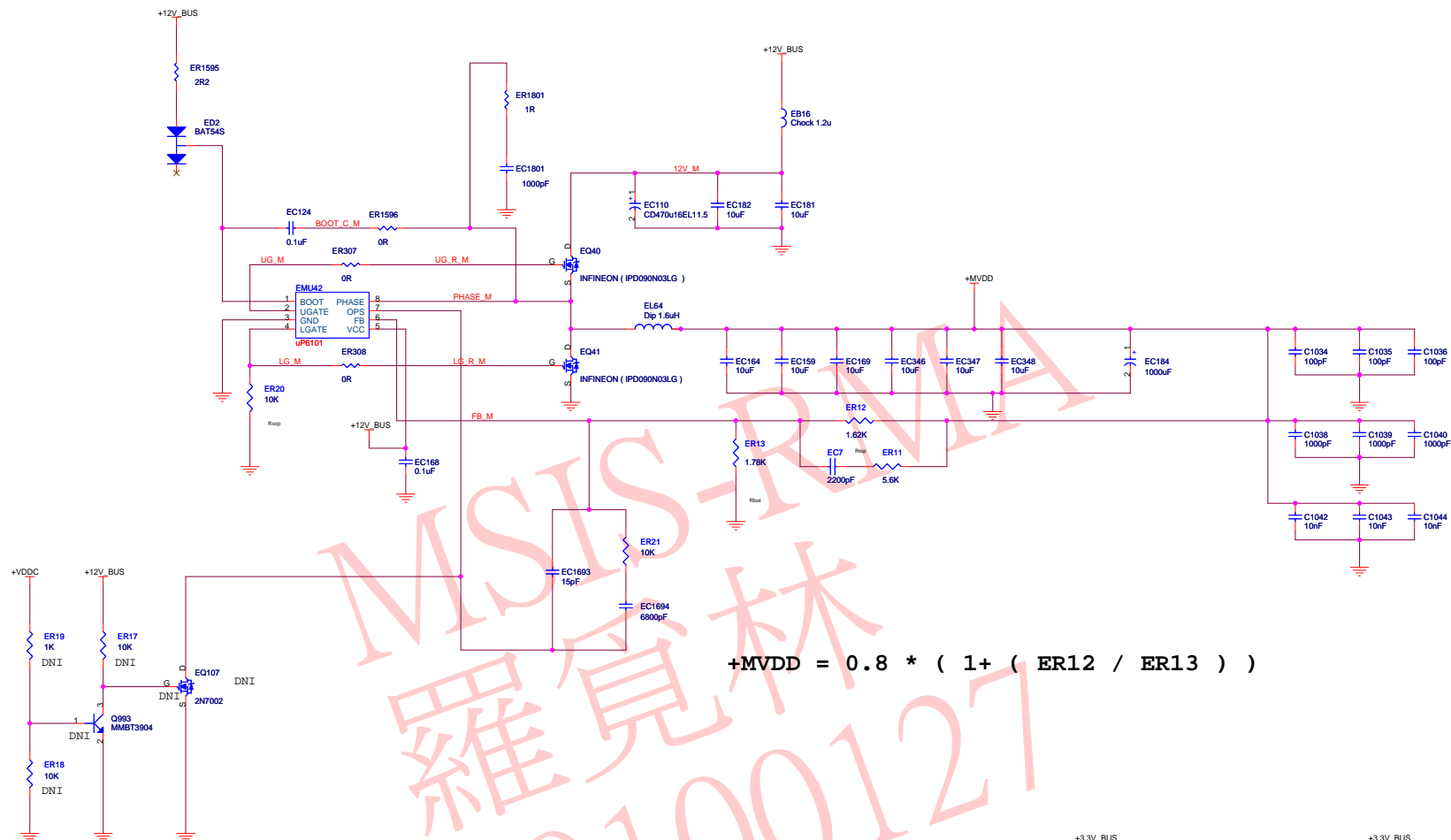
CEDAR LVTMDP E&F dDVI-I



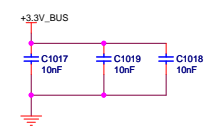
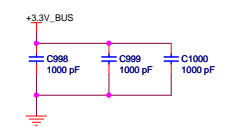
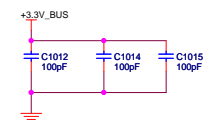
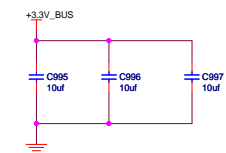
CEDAR Power & GND







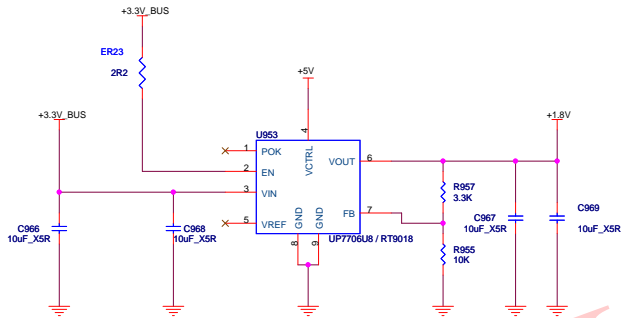
$$+MVDD = 0.8 * ( 1 + ( ER12 / ER13 ) )$$



Memory Power Seq

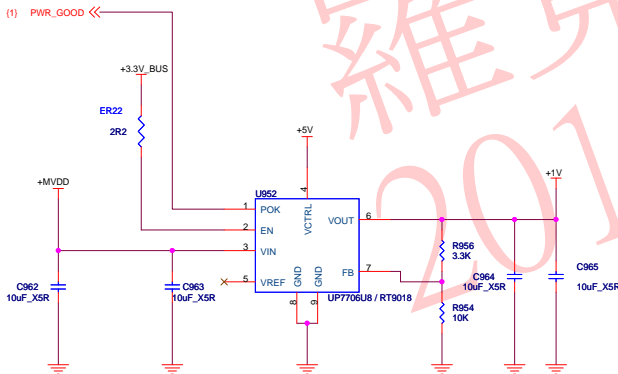
Linear Regulators

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling



$V_{out}=0.8V * ( 1+ R957 / R955 )$

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling

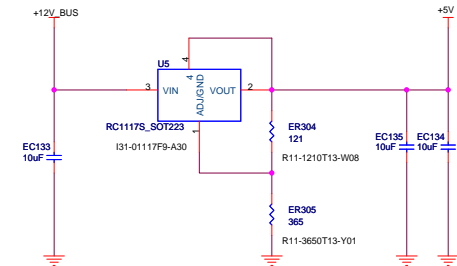


$V_{out}=0.8V * ( 1+ R956 / R954 )$

Regulators for +5V, +5V\_VESA and +5V\_VESA2

1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA



$V_{out}=1.25V* [1+(ER305/ER304) ]$

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Date: Friday, November 27, 2009  
Sheet 13 of 18

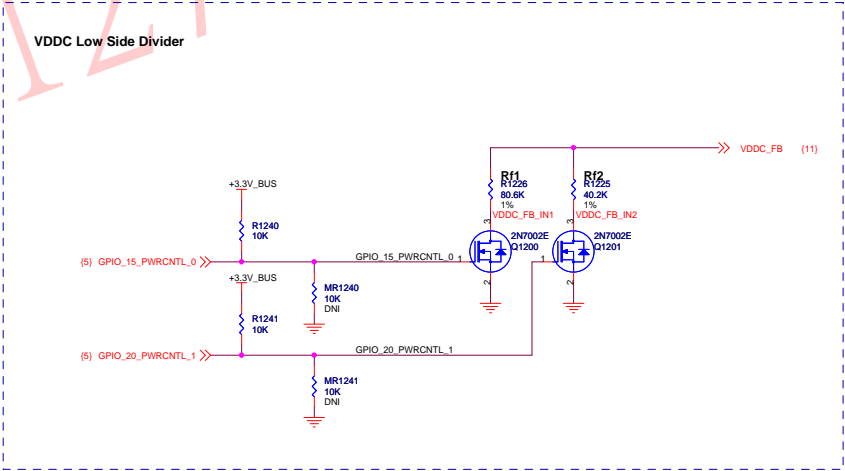
Rev P03

Title RH CEDAR DDR3 1GB VGA+HDMI/DP+dDVI

Doc No. 105-C026XX-00D

Power Management - Power Gating and Dynamic Voltage Control

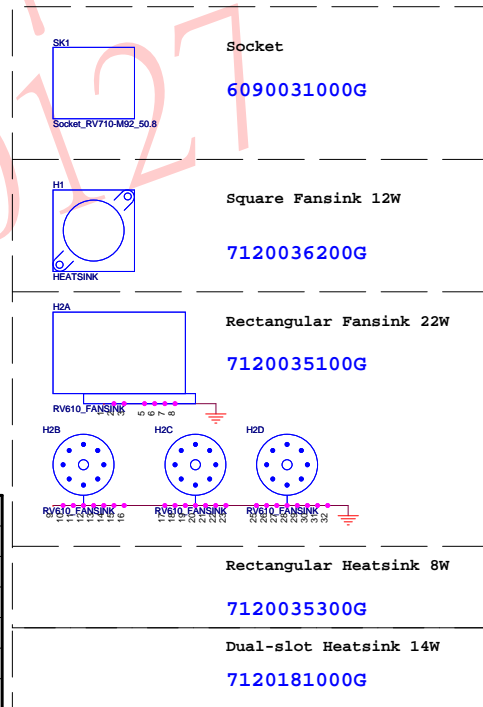
MSIS-RMA  
羅覓林  
20100127



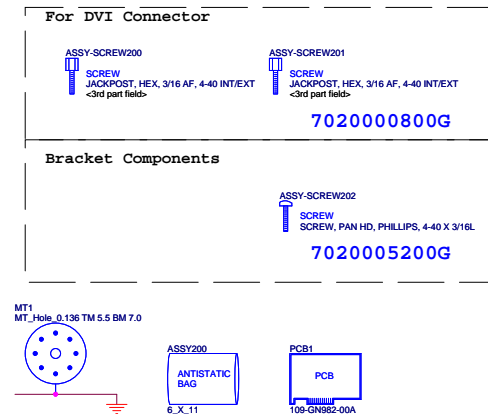
The schematic shows the U1N1 component with the following connections:

- TSVDD (AD17):** Connected to +1.8V.
- TSVSS (AC17):** Connected to ground.
- TS\_FDO (RS):** Connected to a 3.3V\_BUS supply through a network of resistors (R4100, 2.61K, R4101, 33R).
- TS\_FDO:** Connected to the PWM pin of the Q4100 MOSFET.

Figure 1 shows a schematic diagram of the power supply circuit for the MSIS-RNA. The circuit is powered by a +12V BUS. This bus is connected to a network of resistors: R4102 (2.61K, 1%), R4103 (100K), and R4111 (1K, 1%, DNI). The circuit is grounded.

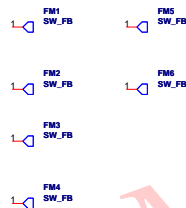
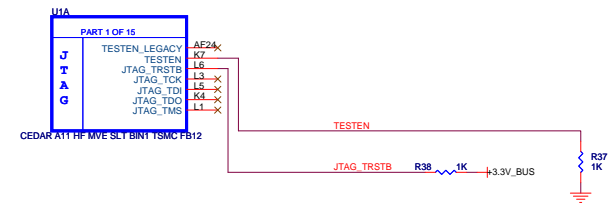


SKU		P/N	CONFIGURATION	Form Factor
	PERCH	8020051300G	DVI + DP + VGA	FH / SS
BASS		8020051400G	DVI +HDMI+ VGA	FH / SS
	PERCH	8020051600G	DVI + DP	LP / SS
BASS		80200516A0G	DVI +HDMI	LP / SS
	PERCH	8020051700G	DVI + DP + VGA	FH / DS
BASS		80200517A0G	DVI +HDMI+ VGA	FH / DS

[illegible]

(19) Debug Circuits

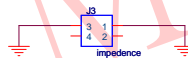
JTAG



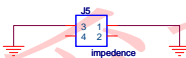
TOP  
Single end  
Address branch  
50 ohm +/- 5 ohm  
3.937 mils



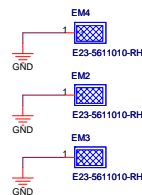
Bottom  
Single end  
Memory data  
45 ohm +/- 5 ohm  
4.724 mils



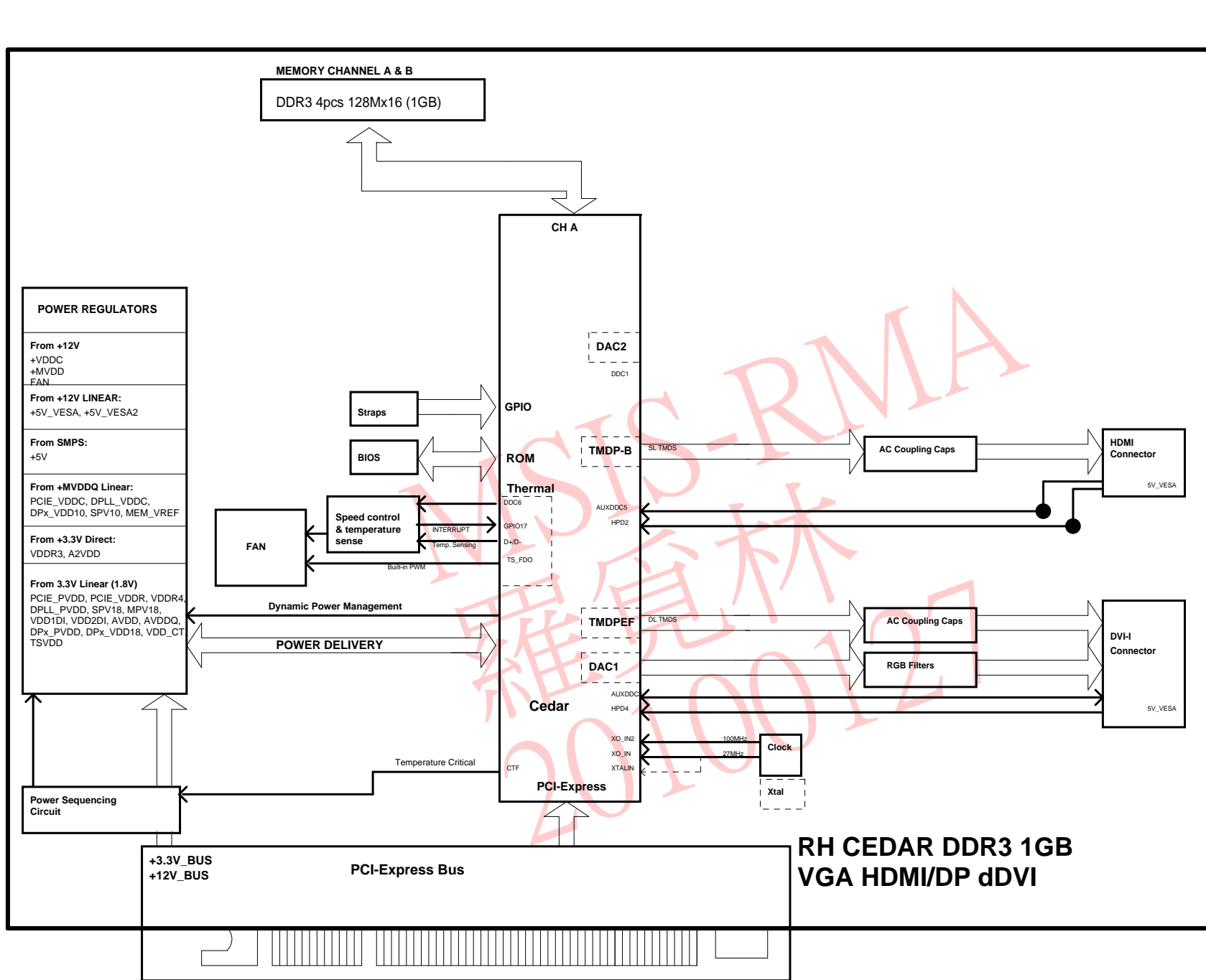
TOP  
Different  
TMDs  
100 ohm +/- 10 %  
3.897 mils / 11.850 mils



Bottom  
Different  
PEX\_PCIE  
85 ohm +/- 10 %  
4.921 mils / 6.889 mils







**RH CEDAR DDR3 1GB  
VGA HDMI/DP dDVI**

<div>AMD</div>			Title		Schematic No.		Date:				
			RH CEDAR DDR3 1GB VGA+HDMI/DP+dDVI		105-C026XX-00D		Friday, November 27, 2009				
			REVISION HISTORY					NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.		Rev P03	
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION								
00	00A	2009/03/23									
01	00B	2009/07/3									
02	00C	2009/08/12	Initial Cedar schematic								
03	00D	2009/09/24	Change DDC line configuration								

MSIS-RMA

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