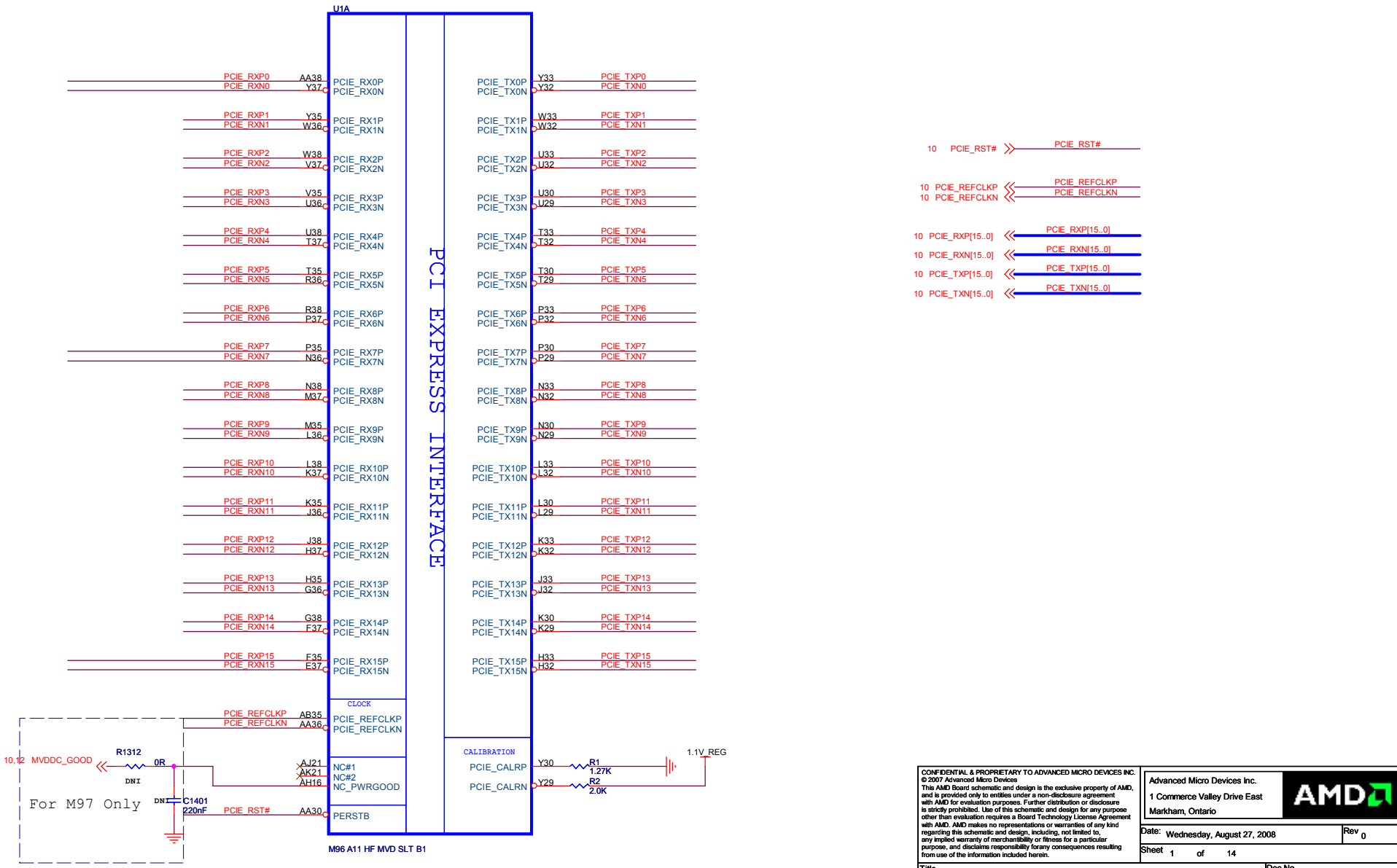

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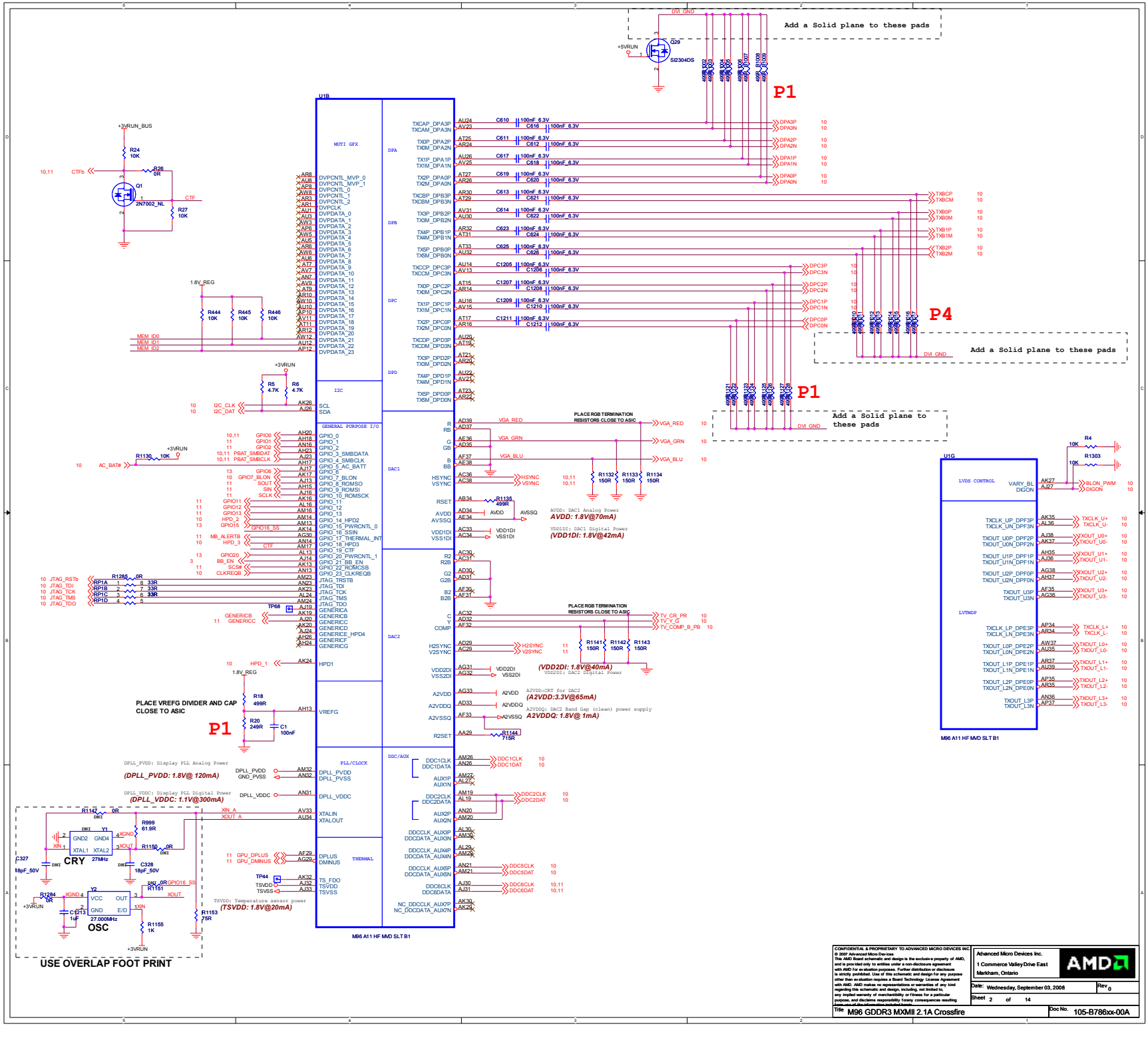
Sheet 1 of 14

Title: RH M92/M96 M package MXM2.1A DDR2

Doc No. 105-B80631-00A


Add a Solid plane to these pads
P1
P4
Add a Solid plane to these pads
Add a Solid plane to these pads
P1
PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC
USE OVERLAP FOOT PRINT
CRY
OSC
M96 A11 HF MVD SLT B1
M96 A11 HF MVD SLT B1
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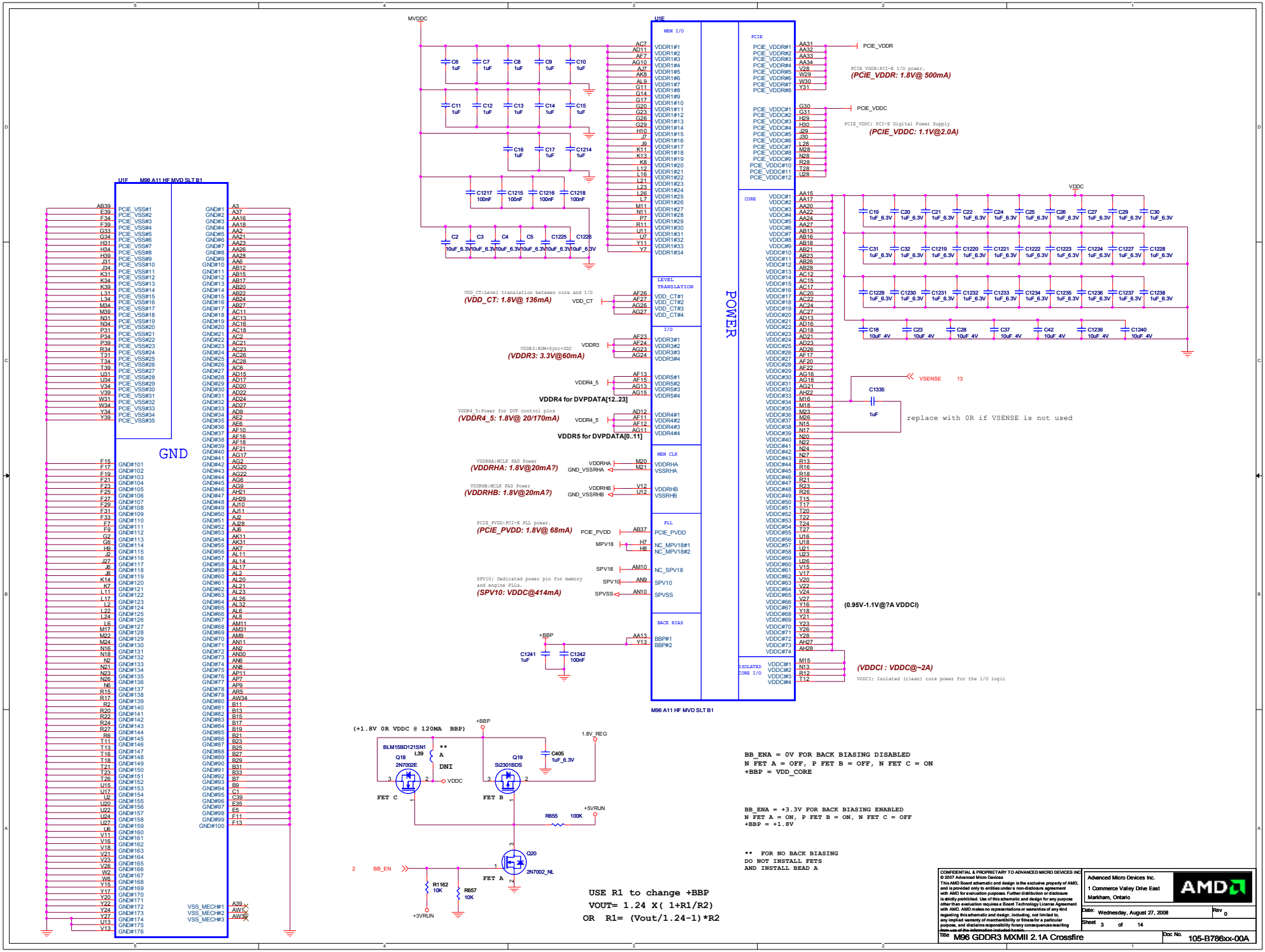
Wednesday, September 03, 2008
Sheet 2 of 14
M96 GDDR3 MXMII 2.1A Crossfire
105-B786xx-00A


U1E M96 A11 HF MVD SLT B1
MVDDC
MEM I/O
PCIE
LEVEL TRANSLATION
I/O
MEM CLK
PLL
BACK BIAS
POWER
CORE
ISOLATED CORE I/O
PCIE_VDDR
PCIE_VDDC
VDDC
VSENSE 13
C1335 1uF
replace with 0R if VSENSE is not used
(0.95V-1.1V@?A VDDCI)
(VDDCI : VDDC@~2A)
VDDCI: Isolated (clean) core power for the I/O logic
PCIE_VDDR:PCI-E I/O power.
(PCIE_VDDR: 1.8V@ 500mA)
PCIE_VDDC: PCI-E Digital Power Supply
(PCIE_VDDC: 1.1V@2.0A)
VDD_CT:Level translation between core and I/O
(VDD_CT: 1.8V@ 136mA)
VDDR3:ROM+Sync+3DC
(VDDR3: 3.3V@60mA)
VDDR4 for DVPDATA[12..23]
VDDR4_5:Power for DVP control pins
(VDDR4_5: 1.8V@ 20/170mA)
VDDR5 for DVPDATA[0..11]
VDDRHA:MCLK PAD Power
(VDDRHA: 1.8V@20mA?)
VDDRHB:MCLK PAD Power
(VDDRHB: 1.8V@20mA?)
PCIE_PVDD:PCI-E PLL power.
(PCIE_PVDD: 1.8V@ 68mA)
SPV10: Dedicated power pin for memory and engine PLLs.
(SPV10: VDDC@414mA)
+BBP
GND
M96 A11 HF MVD SLT B1
(+1.8V OR VDDC @ 120MA BBP)
BLM15BD121SN1 L39
Q18 2N7002E
FET C
Q19 SI2301BDS
FET B
C405 1uF_6.3V
1.8V_REG
R655 100K
+5VRUN
Q20 2N7002_NL
FET A
BB_EN
R1162 10K
R657 10K
+3VRUN
DNI
BB_ENA = 0V FOR BACK BIASING DISABLED
N FET A = OFF, P FET B = OFF, N FET C = ON
+BBP = VDD_CORE
BB_ENA = +3.3V FOR BACK BIASING ENABLED
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.8V
** FOR NO BACK BIASING
DO NOT INSTALL FETS
AND INSTALL BEAD A
USE R1 to change +BBP
VOUT= 1.24 X(1+R1/R2)
OR R1= (Vout/1.24-1)*R2
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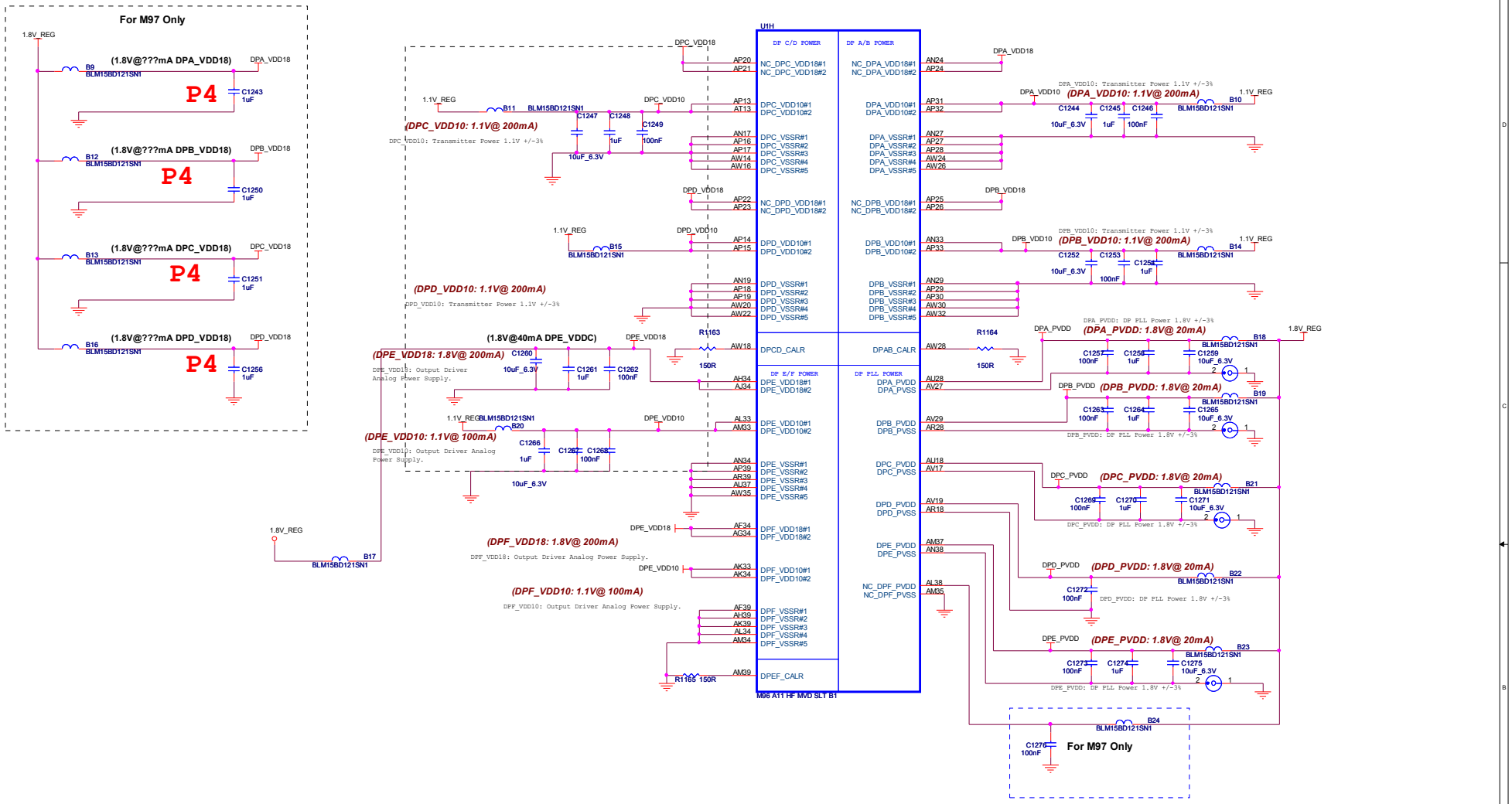
Sheet 3 of 14
Title M96 GDDR3 MXMII 2.1A Crossfire
Doc No. 105-B786xx-00A



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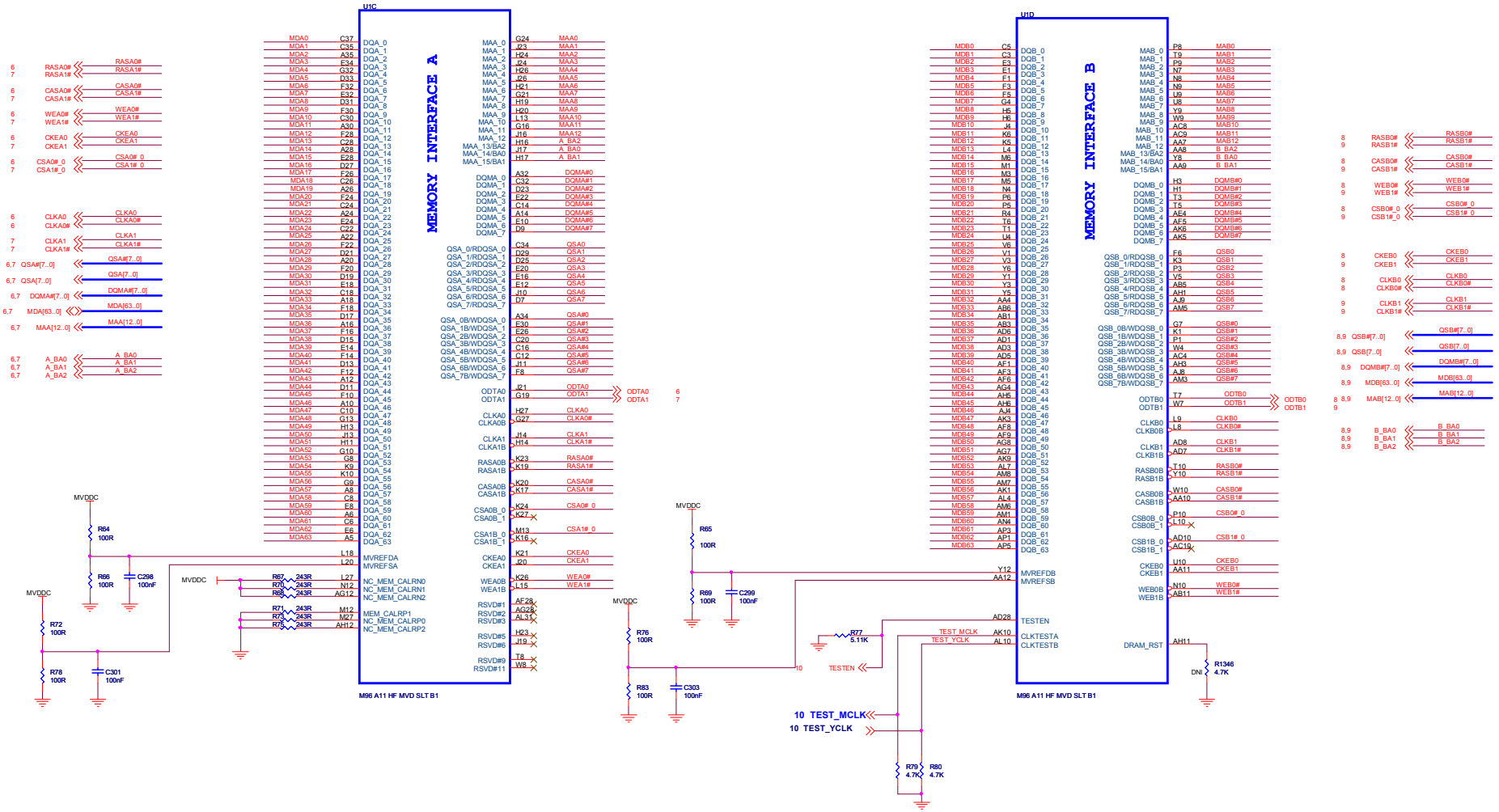
Date: Wednesday, August 27, 2008 Rev 0

Sheet 4 of 14

Title M96 GDDR3 MXMII 2.1A Crossfire

Doc No. 105-B786xx-00A



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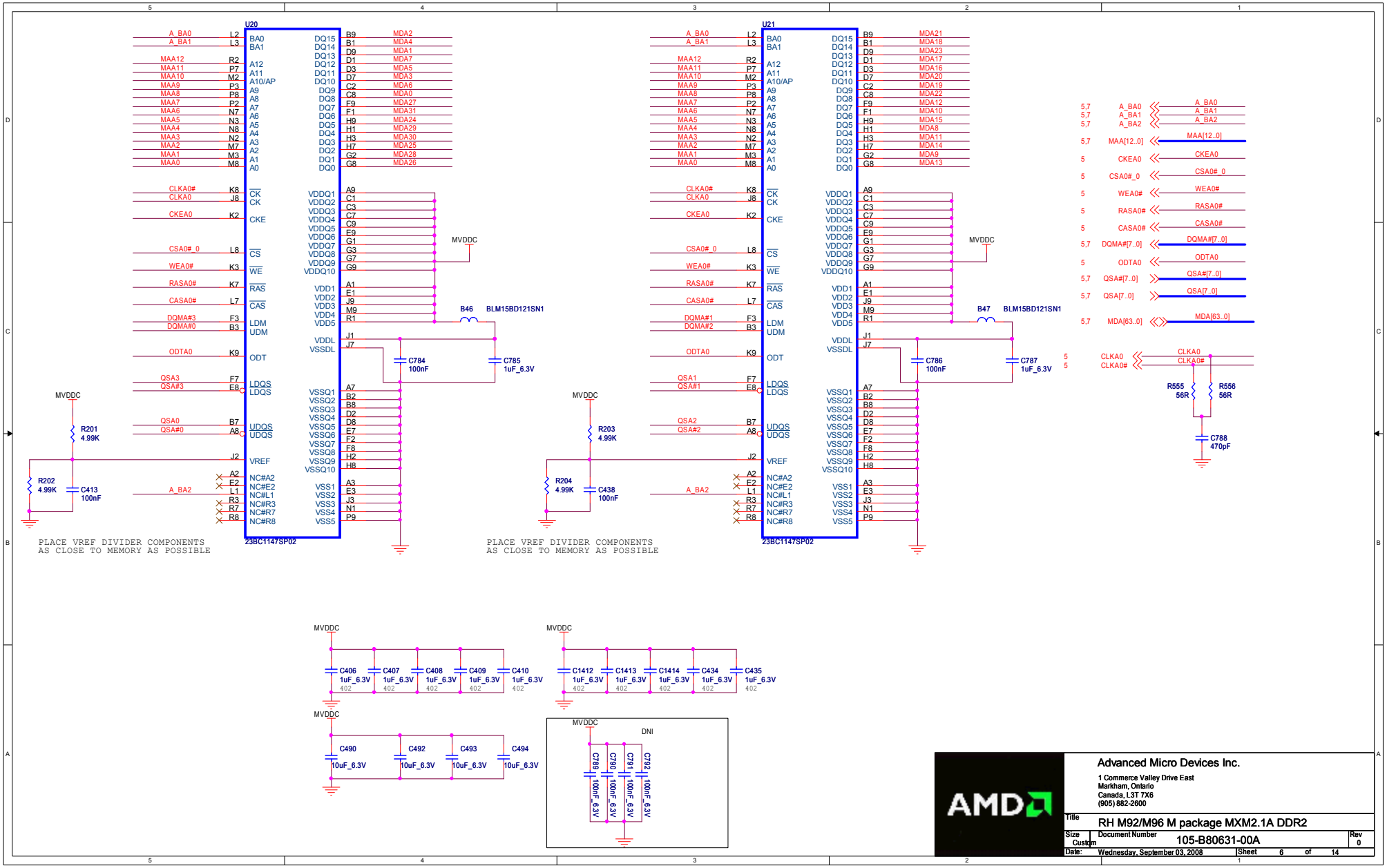
Title	RH M92/M96 M package MXM2.1A DDR2		
Size C	Document Number 105-B80631-00A		Rev 0
Date: Wednesday, August 27, 2008	Sheet 5 of 14		



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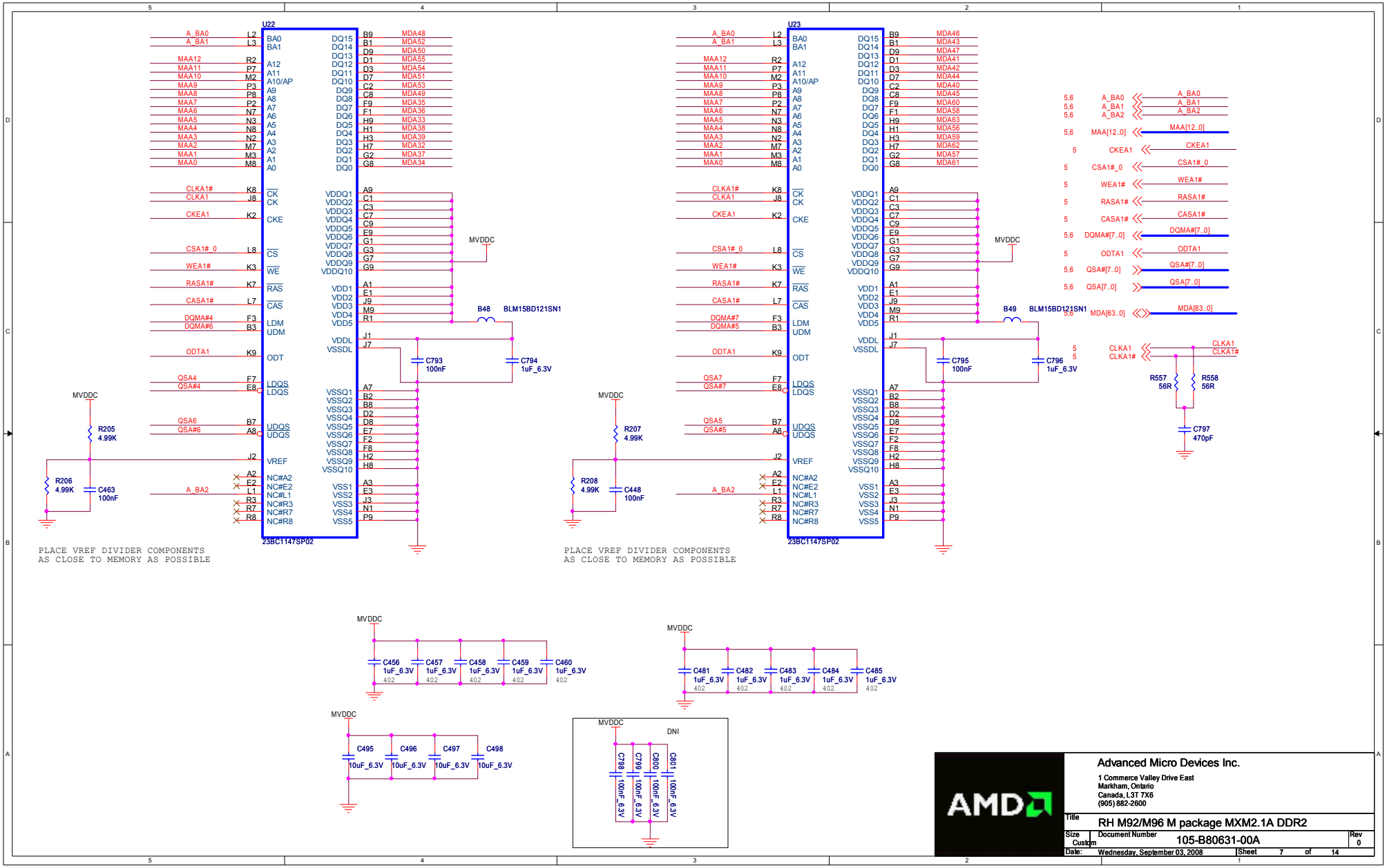
Title	RH M92/M96 M package MXM2.1A DDR2		
Size: Custom	Document Number: 105-B80631-00A		Rev: 0
Date: Wednesday, September 03, 2008	Sheet 6 of 14		



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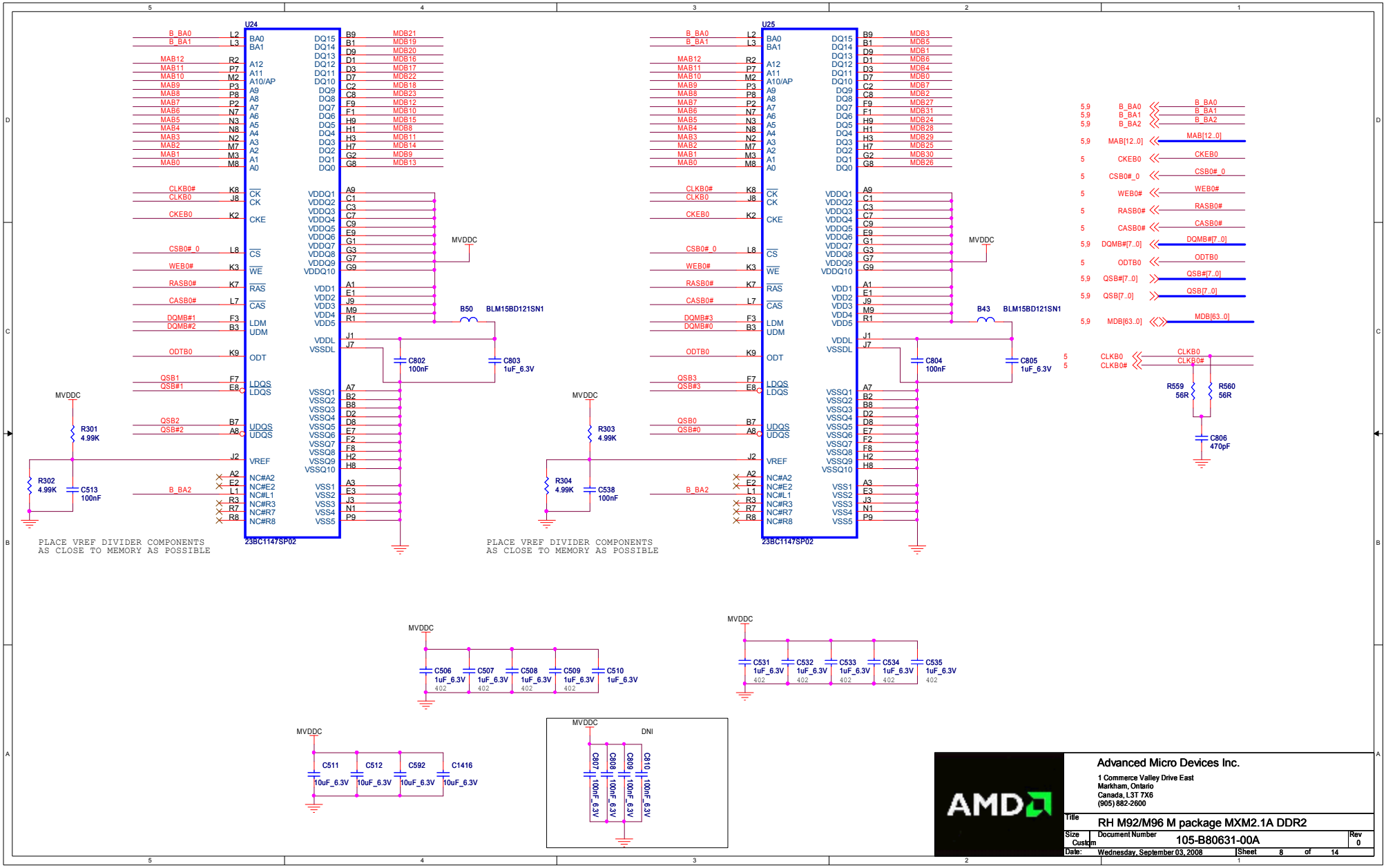
Title: RH M92/M96 M package MXM2.1A DDR2

Size: Custom | Document Number: 105-B80631-00A | Rev: 0

Date: Wednesday, September 03, 2008 | Sheet 7 of 14



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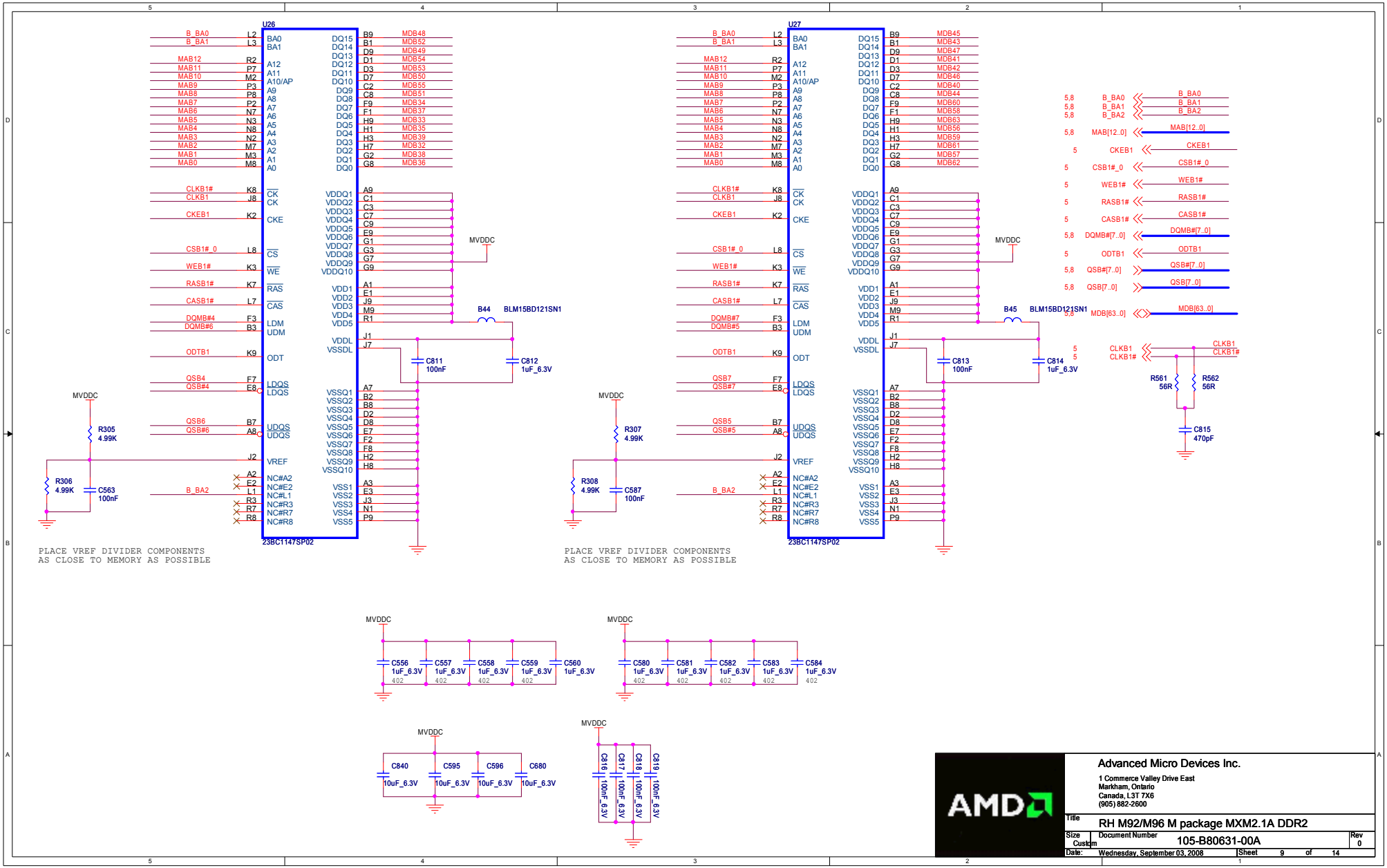
Size: Custom	Document Number: 105-B80631-00A		Rev: 0
Date: Wednesday, September 03, 2008	Sheet 8 of 14		



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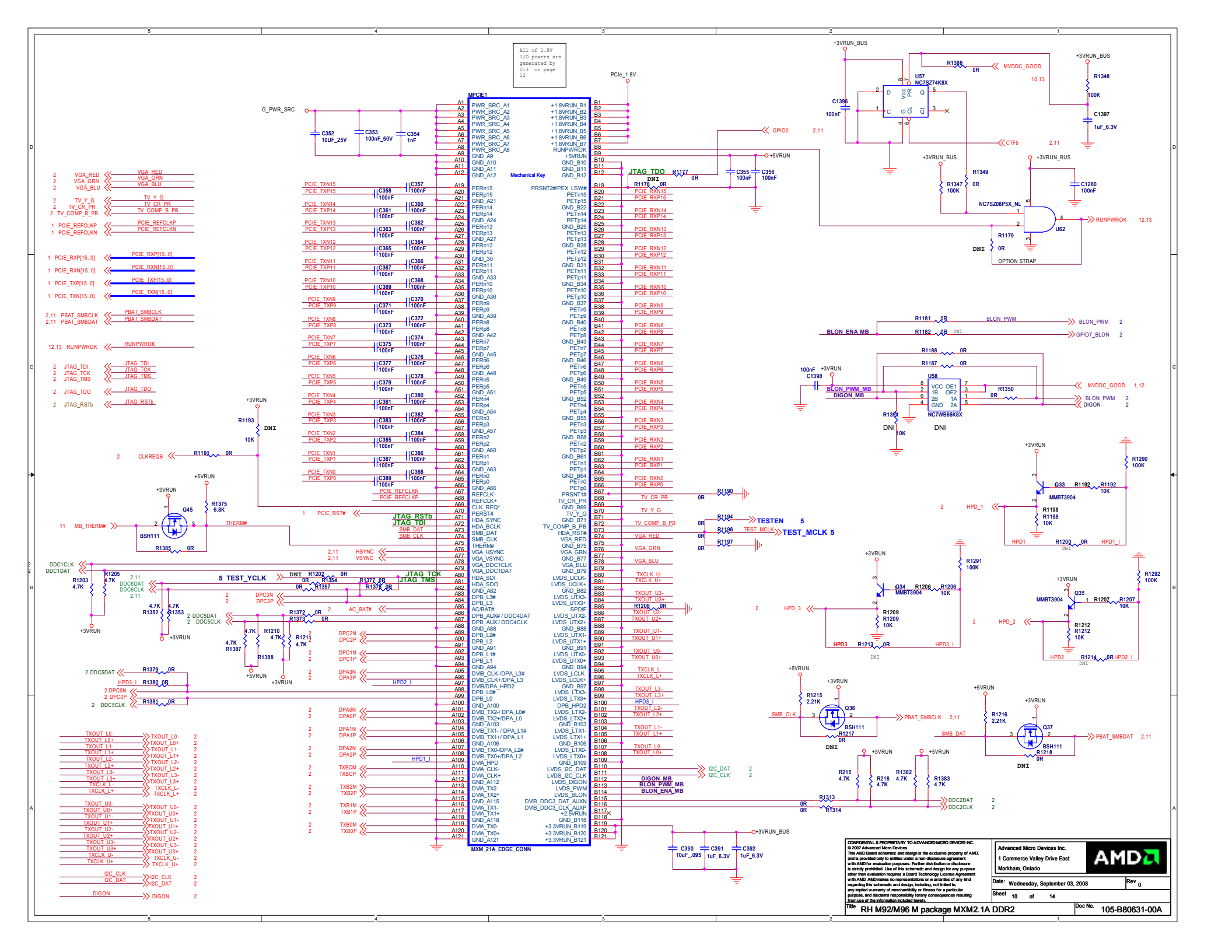
Size: Custom	Document Number: 105-B80631-00A		Rev: 0
Date: Wednesday, September 03, 2008	Sheet 9 of 14		


All of 1.8V I/O powers are generated by U13 on page 12
MPCIE1
MXM_21A_EDGE_CONN
Mechanical Key
JTAG_TDO
JTAG_RSTb
JTAG_TDI
JTAG_TCK
JTAG_TMS
SMB_DAT
SMB_CLK
TESTEN 5
TEST_MCLK 5
TEST_YCLK 5
DIGON_MB
BLON_PWM_MB
BLON_ENA_MB
OPTION STRAP
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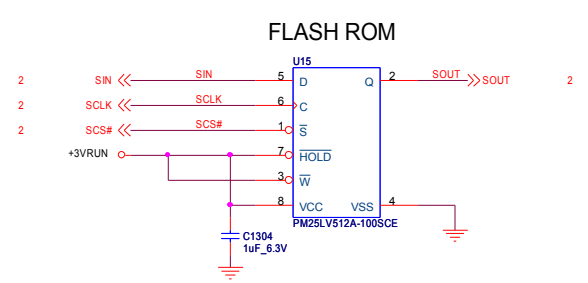
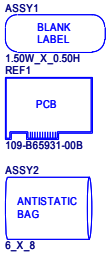
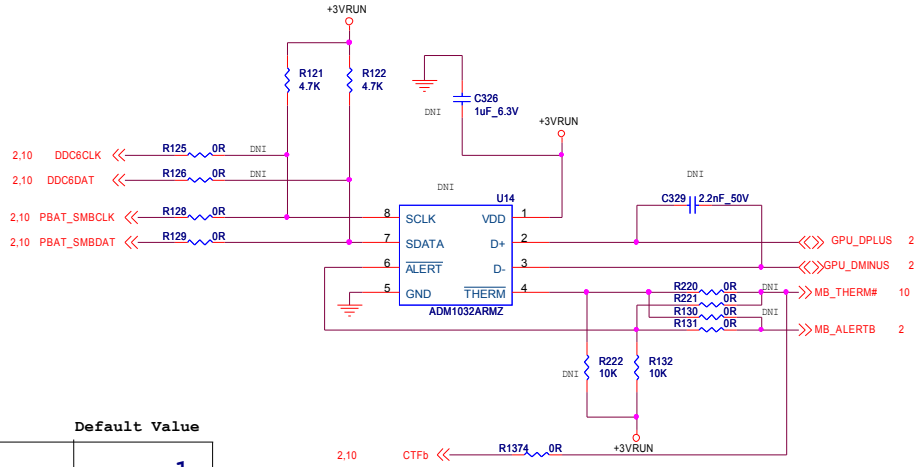
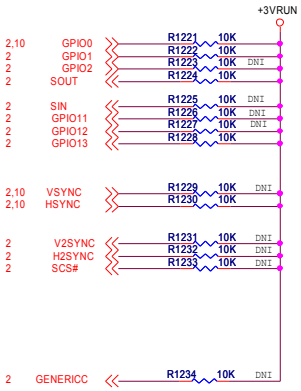
Rev 0
Sheet 10 of 14
Title RH M92/M96 M package MXM2.1A DDR2
Doc No. 105-B80631-00A









Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11	GPIO9,13,12,11 (config 3,2,1,0): a> If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM Type: b> If BIOS_ROM_EN = 0, then Config[3:0] defines the Aperture size:Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 64MB 011 = 32MB 100 = 512MB 101 = 1GB 110 = 2GB 111 = 4GB	0100
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUDIO[0]	VSYNC		1
AUD(1)	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0 – No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VIP_DEVICE_STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to '1', then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to '0', then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0

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Date: Wednesday, August 27, 2008 Rev 0

Sheet 11 of 14

Title M96 GDDR3 MXMII 2.1A Crossfire

Doc No. 105-B786xx-00A

T_ON= 1.6uS X V_Tset /(Vin-Vout)
T_OFF= 1.6uS X V_Tset / V_set

Current Ripple = 1.6uS X V_tset / L
R_esr X Cout > T_ON / 2

IO REGULATOR 1.8V @ 10A

Current Limit = 15A, V_IN= 7-24V
Imax=10A Vout= 1.8V- 1.5V
V_TSET=1.935V
F_sw= 538KHz (T_ON=0.139uSec, T_off=2.222uSec)
I_Ripple=3.1A, 20%
ESR= 9mOhms
V_ripple= I_RippleXT_OFF/Cout = 15mV

G_PWR_SRC
C1406 4.7UF_25V
C1407 4.7UF_25V
C1408 4.7UF_25V
Use OVERLAP FOOT Print
+5VRUN
C1100 100nF
C1101 1uF_6.3V
BAT54S
D5
R1100 15K
PLACE CAPS CLOSE TO AND BETWEEN UPPER FETS DRAIN AND LOWER FETS SOURCE
C1415 10UF_25V
C414 10UF_25V
Q21
BSC120N03MS_G
C416 100nF_50V
22.1R
R1240
1,10 MVDDC_GOOD
MVDDC_GOOD
R1309 47K
13 VDDC_GOOD
R1242 47K
10,13 RUNPWROK
R1243 10K
DNI
PRICE=0.29
U60
PGD
ON/SKIP
VREF
TSET
VSET
OCT
GNDP
GNDA
GND#18
GND#19
GND#20
GND#21
BST
HDR
LX
LDR
CSP
CSN
VDDA
VDDP
VIN
OZ811LN
100nF C1102
V_TSET=1.935V
R1102 20K
C1103 100nF
R1244
13 GPIO6_INV
110K
AGND
C1366 100nF
R1107 47.5K
R1105 34K
R1108 66.5K
C1107 1nF
C1104 22nF_16V
C1108 1uF_6.3V
C1109 1uF_6.3V
Vout= 2.75 X Rb /(Ra+Rb)
OR Rb= Ra / (2.75/VDDC -1)
BSC120=18.5 CENTS
Rds=14mOhms,
39A, Qg=7.2nC
Price =63Cents
DCR=10mOhm Max
Current Limit = 15A
L40 1uH_11A
MVDDC
R1103 100K
R1104 59K
C418 470uF
C419 10uF_095
R1106 51.1R
C1106 2.7nF_50V_5%
ESR=9mOhms
Price =61.7Cents
Q22
BSC042S03MS G
BSC042=27 CENTS
Rds=5.4mOhms, 93A,
Qg=17nC
AON6710=25 CENTS
,Shottkey
Rds=6.7mOhms, 19A,
Qg=29nC
C1110 22pF
C1111 1nF
BSC016=75 CENTS,
Rds=1.6mOhms, 100A, Qg=41nC
NS32
Connect all AGND together first and join with DGND with a Via at the GND pin of OUTPUT BULK CAP

1.1V (3.0A)

DNI
R1295 20K
13 VDDC_GOOD
R1294 0R
1.1V_OK
+5VRUN
U19
GND
FB
VOUT3
VOUT4
EN
POK
VCNTL
VIN
THM
APL5913KAC-TRG
1.8V_REG
R700 78.7K
R701 31.6K
C453 56pF_50V
C424 10uF_10V
C427 1uF_6.3V
1.1V_REG
C1112 10uF_6.3V
C425 10uF_6.3V
C426 10uF_6.3V

LED to indicate all Power rails are OK

+3VRUN_BUS
R1296 10K
R1270 10K
+3VRUN
NC7SZ08P5X_NL
1.1V_OK
MVDDC_GOOD
U59
R1363 390R
D7
SML-LX0603GW
Place at top-left corner

R1245 0R
DNI
+3VRUN
Q39
Si2301BDS
+3VRUN_BUS
100K R1246
10,13 MVDDC_GOOD
R1249 0R
10,13 RUNPWROK
R1250 51K
DNI
Q41
MMBT3904
C1368 100nF
DNI

1.8V_REG
47uF
C1399
NS27
NS28
NS29
MVDDC

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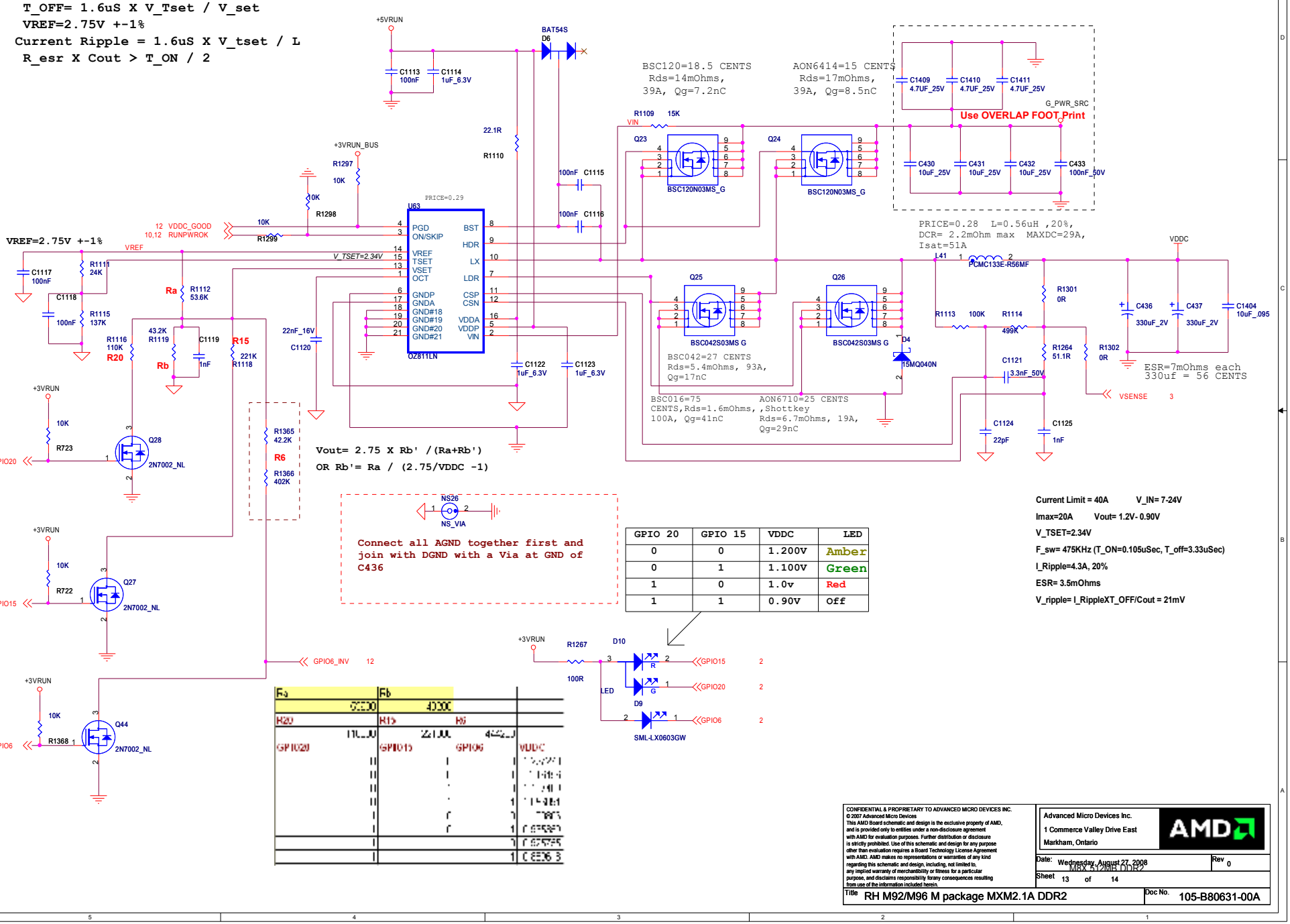
Sheet 12 of 14
Title RH M92/M96 M package MXM2.1A DDR2
Doc No. 105-B80631-00A

CORE PWM REGULATOR 0.9V/ 1.0V/ 1.05V/ 1.2V @ 20A

T_ON= 1.6uS X V_Tset /(Vin-Vout)
T_OFF= 1.6uS X V_Tset / V_set
VREF=2.75V +-1%
Current Ripple = 1.6uS X V_tset / L
R_esr X Cout > T_ON / 2



GPIO 20	GPIO 15	VDDC	LED
0	0	1.200V	Amber
0	1	1.100V	Green
1	0	1.0v	Red
1	1	0.90V	Off

Current Limit = 40A V_IN= 7-24V
Imax=20A Vout= 1.2V- 0.90V
V_TSET=2.34V
F_sw= 475KHz (T_ON=0.105uSec, T_off=3.33uSec)
I_Ripple=4.3A, 20%
ESR= 3.5mOhms
V_ripple= I_RippleXT_OFF/Cout = 21mV

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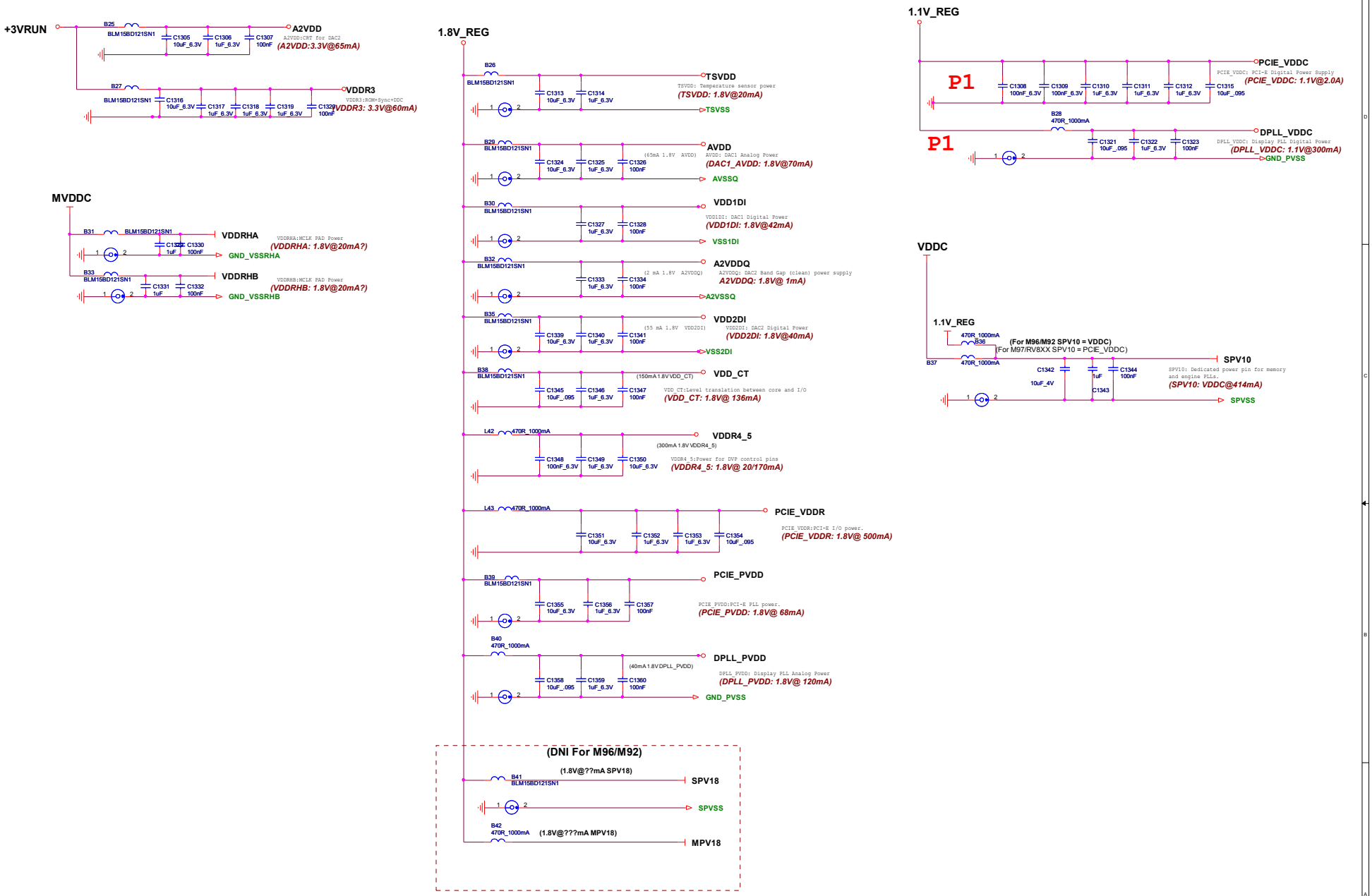
Sheet 13 of 14
Title RH M92/M96 M package MXM2.1A DDR2 Doc No. 105-B80631-00A



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Sheet 14 of 14

Title M96 GDDR3 MXMII 2.1A Crossfire

Doc No. 105-B786xx-00A