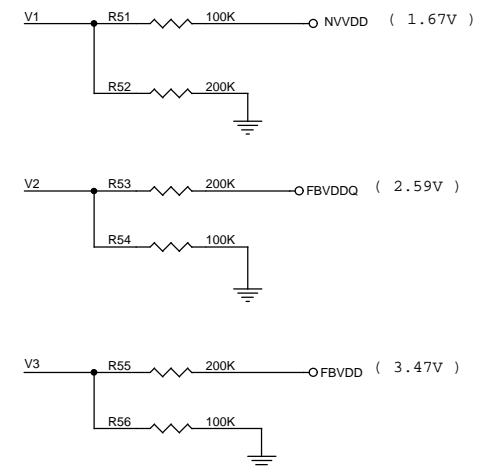
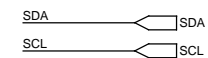


NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X
PCI DEVICE ID 0X0=0X200 FOR NV20.

NVVD SET TO: 1.52V
FBVDD SET TO: 3.47V
FBVDDQ SET TO: 2.59V

HISTORY REVISION:

- X00: Based on P50-A06
- See change list in 149- file.
 - Set FBVDDQ=2.59V
- P50-A07-X01:
- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)
- P50-A08:
- X04: - Delay PLL_VDD to come up after NVVDD.
- X05: - Added 1UF accross R257.
- X06: - Removed X04-5 above, added a switcher generated PLL delay option.
- SSENNA cap for 2nd SW changed to 1UF.
 - A05 Si, NVVDD=1.52V
- P50-A09:
- X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.
- X03: - Added option to pull up power good to 12V
- ECO1235: - Changed R841 PU to 10K (from 4.7K)
- ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction. Replaced C303,306,309 with 75ohm and no stuffed R208-210.



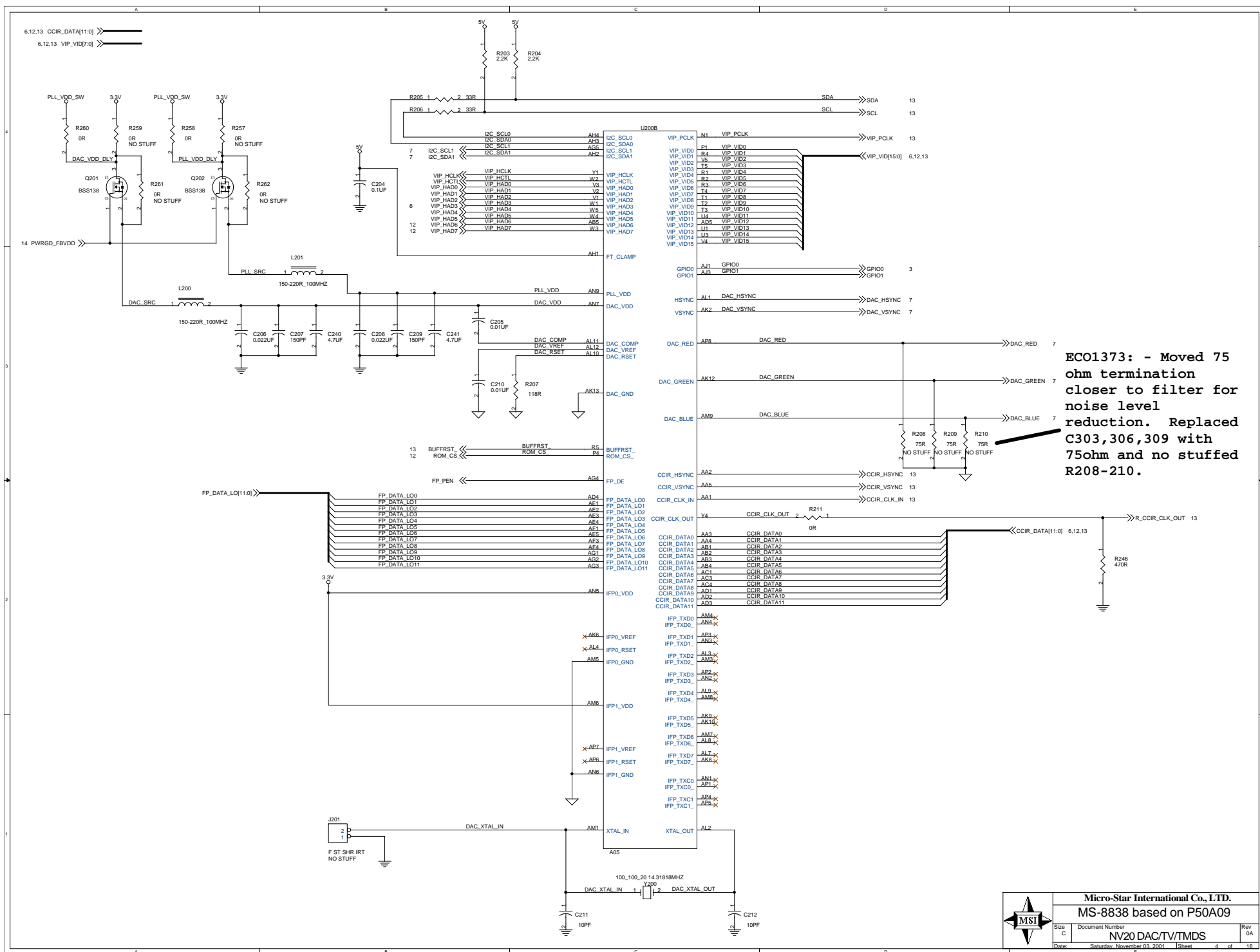
VOLTAGE SENSORING CIRCUIT



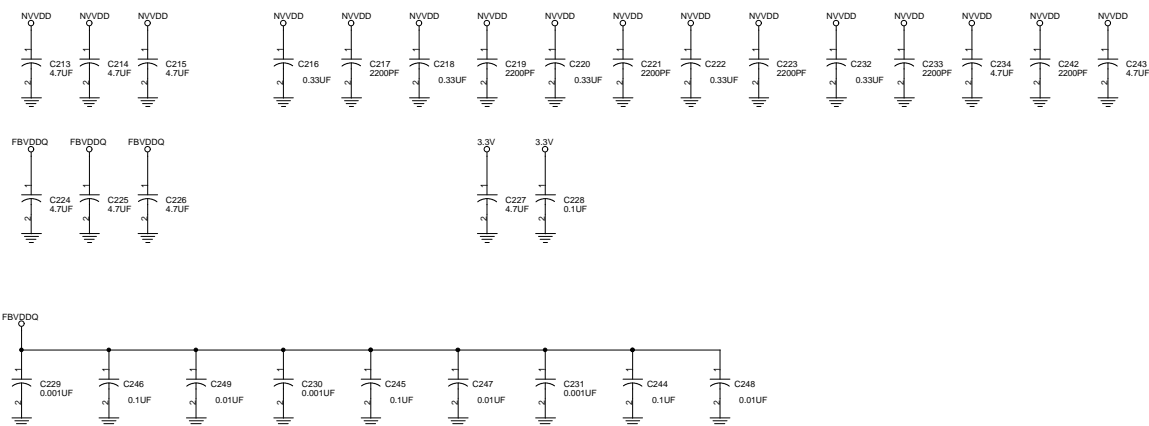
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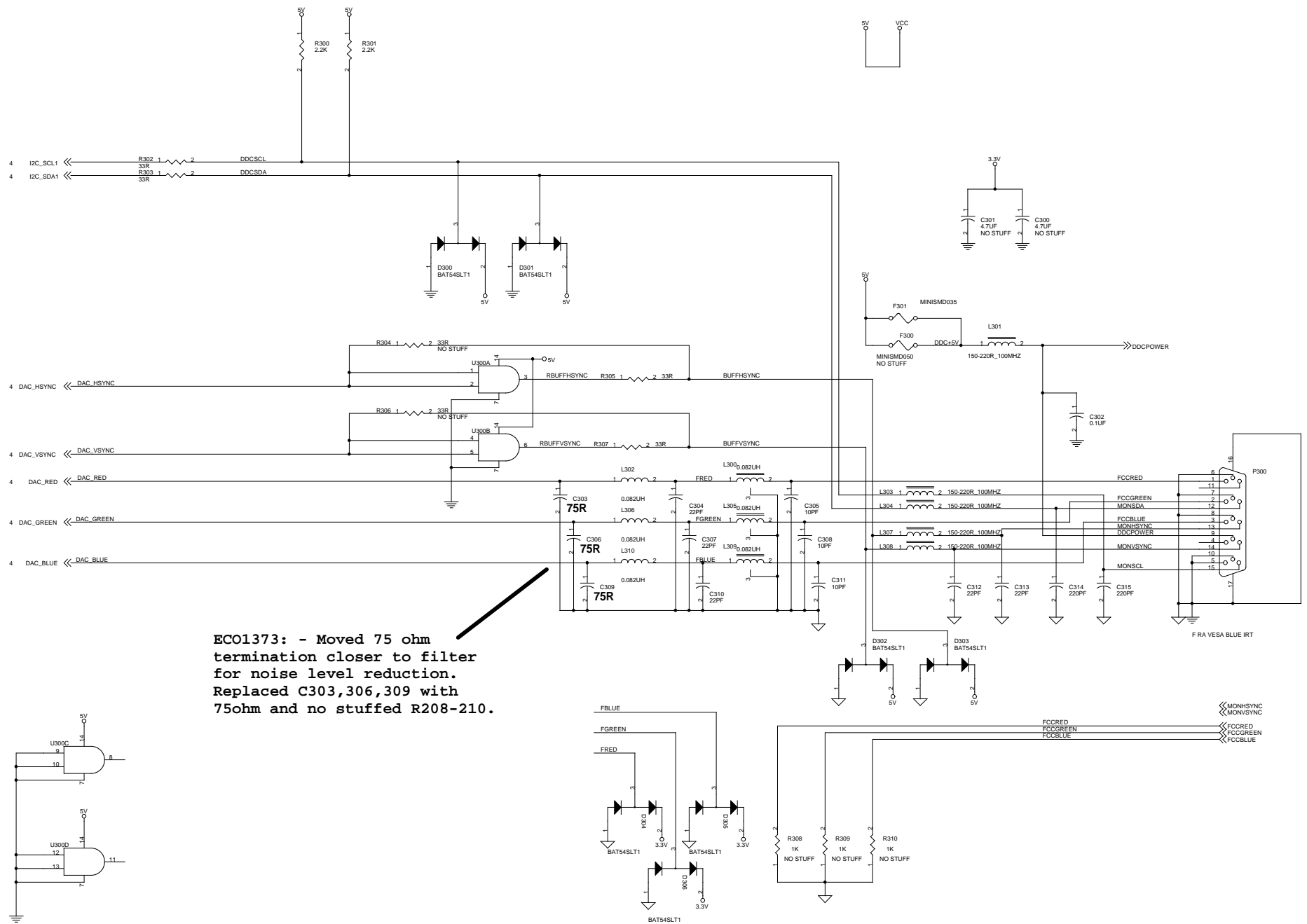




Use this for impedance controlled traces on XTAL IN/OUT







ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction. Replaced C303,306,309 with 75ohm and no stuffed R208-210.

U2000			
FBD_DATA0_A16	FBD_DATA0	FBC_DATA0	A34 FBC_DATA0
FBD_DATA1_A16	FBD_DATA1	FBC_DATA1	B33 FBC_DATA1
FBD_DATA2_A16	FBD_DATA2	FBC_DATA2	A33 FBC_DATA2
FBD_DATA3_A16	FBD_DATA3	FBC_DATA3	A32 FBC_DATA3
FBD_DATA4_A16	FBD_DATA4	FBC_DATA4	B31 FBC_DATA4
FBD_DATA5_A16	FBD_DATA5	FBC_DATA5	A30 FBC_DATA5
FBD_DATA6_A16	FBD_DATA6	FBC_DATA6	B30 FBC_DATA6
FBD_DATA7_A16	FBD_DATA7	FBC_DATA7	A29 FBC_DATA7
FBD_DATA8_A16	FBD_DATA8	FBC_DATA8	C29 FBC_DATA8
FBD_DATA9_A16	FBD_DATA9	FBC_DATA9	D28 FBC_DATA9
FBD_DATA10_A16	FBD_DATA10	FBC_DATA10	C28 FBC_DATA10
FBD_DATA11_A16	FBD_DATA11	FBC_DATA11	D27 FBC_DATA11
FBD_DATA12_A16	FBD_DATA12	FBC_DATA12	B27 FBC_DATA12
FBD_DATA13_A16	FBD_DATA13	FBC_DATA13	A27 FBC_DATA13
FBD_DATA14_A16	FBD_DATA14	FBC_DATA14	B27 FBC_DATA14
FBD_DATA15_A16	FBD_DATA15	FBC_DATA15	A27 FBC_DATA15
FBD_DATA16_A16	FBD_DATA16	FBC_DATA16	B27 FBC_DATA16
FBD_DATA17_A16	FBD_DATA17	FBC_DATA17	A21 FBC_DATA17
FBD_DATA18_A16	FBD_DATA18	FBC_DATA18	B21 FBC_DATA18
FBD_DATA19_A16	FBD_DATA19	FBC_DATA19	C20 FBC_DATA19
FBD_DATA20_A16	FBD_DATA20	FBC_DATA20	D19 FBC_DATA20
FBD_DATA21_A16	FBD_DATA21	FBC_DATA21	C19 FBC_DATA21
FBD_DATA22_A16	FBD_DATA22	FBC_DATA22	B19 FBC_DATA22
FBD_DATA23_A16	FBD_DATA23	FBC_DATA23	A19 FBC_DATA23
FBD_DATA24_A16	FBD_DATA24	FBC_DATA24	D16 FBC_DATA24
FBD_DATA25_A16	FBD_DATA25	FBC_DATA25	A18 FBC_DATA25
FBD_DATA26_A16	FBD_DATA26	FBC_DATA26	C18 FBC_DATA26
FBD_DATA27_A16	FBD_DATA27	FBC_DATA27	D16 FBC_DATA27
FBD_DATA28_A16	FBD_DATA28	FBC_DATA28	E16 FBC_DATA28
FBD_DATA29_A16	FBD_DATA29	FBC_DATA29	C17 FBC_DATA29
FBD_DATA30_A16	FBD_DATA30	FBC_DATA30	A17 FBC_DATA30
FBD_DATA31_A16	FBD_DATA31	FBC_DATA31	C16 FBC_DATA31

FBD_ADR0_D13	FBC_ADR0	D26 FBC_ADR0
FBD_ADR1_D13	FBC_ADR1	C26 FBC_ADR1
FBD_ADR2_D13	FBC_ADR2	E26 FBC_ADR2
FBD_ADR3_D13	FBC_ADR3	A26 FBC_ADR3
FBD_ADR4_D13	FBC_ADR4	D25 FBC_ADR4
FBD_ADR5_D13	FBC_ADR5	C25 FBC_ADR5
FBD_ADR6_D13	FBC_ADR6	C23 FBC_ADR6
FBD_ADR7_D13	FBC_ADR7	A23 FBC_ADR7
FBD_ADR8_D13	FBC_ADR8	D22 FBC_ADR8
FBD_ADR9_D13	FBC_ADR9	E24 FBC_ADR9
FBD_ADR10_D13	FBC_ADR10	D21 FBC_ADR10
FBD_ADR11_D13	FBC_ADR11	E18 FBC_ADR11
FBD_ADR12_D13	FBC_ADR12	C21 FBC_ADR12
FBD_ADR13_D13	FBC_ADR13	C21 FBC_ADR13

FBD_DOM0_B15	FBC_DOM0	C31 FBC_DOM0
FBD_DOM1_B15	FBC_DOM1	A28 FBC_DOM1
FBD_DOM2_B15	FBC_DOM2	E19 FBC_DOM2
FBD_DOM3_B15	FBC_DOM3	B18 FBC_DOM3

FBD_DQ0_A15	FBC_DQ0	A31 FBC_DQ0
FBD_DQ1_A15	FBC_DQ1	E27 FBC_DQ1
FBD_DQ2_A15	FBC_DQ2	A20 FBC_DQ2
FBD_DQ3_A15	FBC_DQ3	D17 FBC_DQ3

FBD_RAS_B9	FBC_RAS	C24 FBC_RAS
FBD_CAS_B9	FBC_CAS	D24 FBC_CAS
FBD_WE_B9	FBC_WE	B24 FBC_WE
FBD_CS0_B9	FBC_CS0	E22 FBC_CS0
FBD_CS1_B9	FBC_CS1	A24 FBC_CS1

FBD_CLK0_A7	FBC_CLK0	B22 FBC_CLK0
FBD_CLK1_A7	FBC_CLK1	A25 FBC_CLK1
FBD_CLK1B_A7	FBC_CLK1B	B25 FBC_CLK1B
FBD_CKE_A7	FBC_CKE	A22 FBC_CKE

U200C			
FBB_DATA0_W32	FBB_DATA0	FBA_DATA0	AM28 FBA_DATA0
FBB_DATA1_W32	FBB_DATA1	FBA_DATA1	AP29 FBA_DATA1
FBB_DATA2_W32	FBB_DATA2	FBA_DATA2	AM29 FBA_DATA2
FBB_DATA3_W32	FBB_DATA3	FBA_DATA3	AP30 FBA_DATA3
FBB_DATA4_W32	FBB_DATA4	FBA_DATA4	AP31 FBA_DATA4
FBB_DATA5_W32	FBB_DATA5	FBA_DATA5	AM31 FBA_DATA5
FBB_DATA6_W32	FBB_DATA6	FBA_DATA6	AP32 FBA_DATA6
FBB_DATA7_W32	FBB_DATA7	FBA_DATA7	AM32 FBA_DATA7
FBB_DATA8_W32	FBB_DATA8	FBA_DATA8	AP33 FBA_DATA8
FBB_DATA9_W32	FBB_DATA9	FBA_DATA9	AM33 FBA_DATA9
FBB_DATA10_W32	FBB_DATA10	FBA_DATA10	AP34 FBA_DATA10
FBB_DATA11_W32	FBB_DATA11	FBA_DATA11	AM34 FBA_DATA11
FBB_DATA12_W32	FBB_DATA12	FBA_DATA12	AP35 FBA_DATA12
FBB_DATA13_W32	FBB_DATA13	FBA_DATA13	AM35 FBA_DATA13
FBB_DATA14_W32	FBB_DATA14	FBA_DATA14	AP36 FBA_DATA14
FBB_DATA15_W32	FBB_DATA15	FBA_DATA15	AM36 FBA_DATA15
FBB_DATA16_W32	FBB_DATA16	FBA_DATA16	AP37 FBA_DATA16
FBB_DATA17_W32	FBB_DATA17	FBA_DATA17	AM37 FBA_DATA17
FBB_DATA18_W32	FBB_DATA18	FBA_DATA18	AP38 FBA_DATA18
FBB_DATA19_W32	FBB_DATA19	FBA_DATA19	AM38 FBA_DATA19
FBB_DATA20_W32	FBB_DATA20	FBA_DATA20	AP39 FBA_DATA20
FBB_DATA21_W32	FBB_DATA21	FBA_DATA21	AM39 FBA_DATA21
FBB_DATA22_W32	FBB_DATA22	FBA_DATA22	AP40 FBA_DATA22
FBB_DATA23_W32	FBB_DATA23	FBA_DATA23	AM40 FBA_DATA23
FBB_DATA24_W32	FBB_DATA24	FBA_DATA24	AP41 FBA_DATA24
FBB_DATA25_W32	FBB_DATA25	FBA_DATA25	AM41 FBA_DATA25
FBB_DATA26_W32	FBB_DATA26	FBA_DATA26	AP42 FBA_DATA26
FBB_DATA27_W32	FBB_DATA27	FBA_DATA27	AM42 FBA_DATA27
FBB_DATA28_W32	FBB_DATA28	FBA_DATA28	AP43 FBA_DATA28
FBB_DATA29_W32	FBB_DATA29	FBA_DATA29	AM43 FBA_DATA29
FBB_DATA30_W32	FBB_DATA30	FBA_DATA30	AP44 FBA_DATA30
FBB_DATA31_W32	FBB_DATA31	FBA_DATA31	AM44 FBA_DATA31

FBB_ADR0_R31	FBB_ADR0	FBA_ADR0	AL34 FBA_ADR0
FBB_ADR1_R31	FBB_ADR1	FBA_ADR1	AK34 FBA_ADR1
FBB_ADR2_R31	FBB_ADR2	FBA_ADR2	AL33 FBA_ADR2
FBB_ADR3_R31	FBB_ADR3	FBA_ADR3	AK33 FBA_ADR3
FBB_ADR4_R31	FBB_ADR4	FBA_ADR4	AL32 FBA_ADR4
FBB_ADR5_R31	FBB_ADR5	FBA_ADR5	AK32 FBA_ADR5
FBB_ADR6_R31	FBB_ADR6	FBA_ADR6	AL31 FBA_ADR6
FBB_ADR7_R31	FBB_ADR7	FBA_ADR7	AK31 FBA_ADR7
FBB_ADR8_R31	FBB_ADR8	FBA_ADR8	AL30 FBA_ADR8
FBB_ADR9_R31	FBB_ADR9	FBA_ADR9	AK30 FBA_ADR9
FBB_ADR10_R31	FBB_ADR10	FBA_ADR10	AL29 FBA_ADR10
FBB_ADR11_R31	FBB_ADR11	FBA_ADR11	AK29 FBA_ADR11
FBB_ADR12_R31	FBB_ADR12	FBA_ADR12	AL28 FBA_ADR12
FBB_ADR13_R31	FBB_ADR13	FBA_ADR13	AK28 FBA_ADR13

FBB_DOM0_V31	FBB_DOM0	FBA_DOM0	AN30 FBA_DOM0
FBB_DOM1_V31	FBB_DOM1	FBA_DOM1	AK30 FBA_DOM1
FBB_DOM2_V31	FBB_DOM2	FBA_DOM2	AL29 FBA_DOM2
FBB_DOM3_V31	FBB_DOM3	FBA_DOM3	AK29 FBA_DOM3

FBB_DQ0_V32	FBB_DQ0	FBA_DQ0	AM30 FBA_DQ0
FBB_DQ1_V32	FBB_DQ1	FBA_DQ1	AL32 FBA_DQ1
FBB_DQ2_V32	FBB_DQ2	FBA_DQ2	AK30 FBA_DQ2
FBB_DQ3_V32	FBB_DQ3	FBA_DQ3	AL31 FBA_DQ3

FBB_RAS_M33	FBB_RAS	FBA_RAS	AH31 FBA_RAS
FBB_CAS_M33	FBB_CAS	FBA_CAS	AG30 FBA_CAS
FBB_WE_M33	FBB_WE	FBA_WE	AL32 FBA_WE
FBB_CS0_M33	FBB_CS0	FBA_CS0	AK34 FBA_CS0
FBB_CS1_M33	FBB_CS1	FBA_CS1	AG31 FBA_CS1

FBB_CLK0_K32	FBB_CLK0	FBA_CLK0	AE34 FBA_CLK0
FBB_CLK1_K32	FBB_CLK1	FBA_CLK1	AK34 FBA_CLK1
FBB_CLK1B_K32	FBB_CLK1B	FBA_CLK1B	AK34 FBA_CLK1B
FBB_CKE_K32	FBB_CKE	FBA_CKE	AD31 FBA_CKE

<<FBA_DATA[31:0] 10
 <<FBB_DATA[31:0] 10
 <<FBC_DATA[31:0] 11
 <<FBD_DATA[31:0] 11

<<FBA_ADR[13:0] 10
 <<FBB_ADR[13:0] 10
 <<FBC_ADR[13:0] 11
 <<FBD_ADR[13:0] 11

<<FBA_DQS[3:0] 10
 <<FBB_DQS[3:0] 10
 <<FBC_DQS[3:0] 11
 <<FBD_DQS[3:0] 11

<<FBA_DQM[3:0] 10
 <<FBB_DQM[3:0] 10
 <<FBC_DQM[3:0] 11
 <<FBD_DQM[3:0] 11

<<FBA_RAS_ 10
 <<FBA_CAS_ 10
 <<FBA_WE_ 10
 <<FBA_CS0_ 10

<<FBA_CLK0_ 10
 <<FBA_CLK0B_ 10
 <<FBA_CLK1_ 10
 <<FBA_CKE_ 10

<<FBB_RAS_ 10
 <<FBB_CAS_ 10
 <<FBB_WE_ 10
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<<FBB_CLK0_ 10
 <<FBB_CLK0B_ 10
 <<FBB_CLK1_ 10
 <<FBB_CKE_ 10

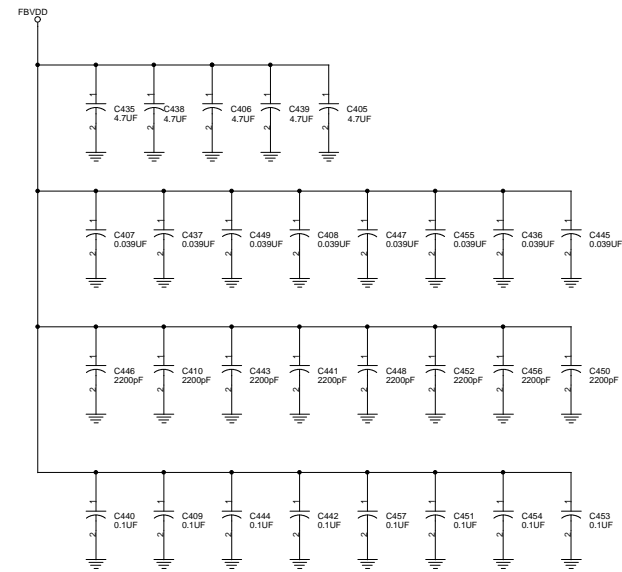
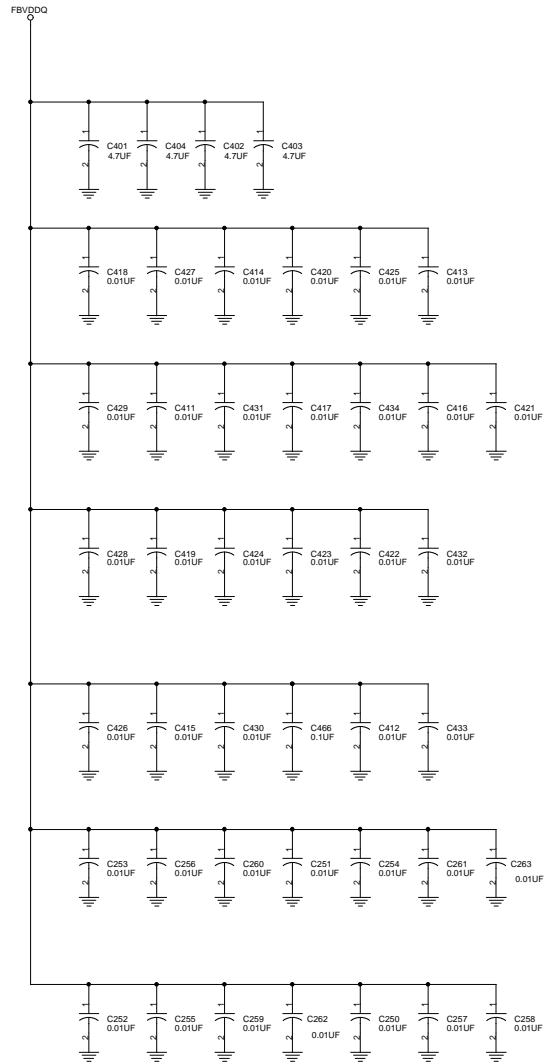
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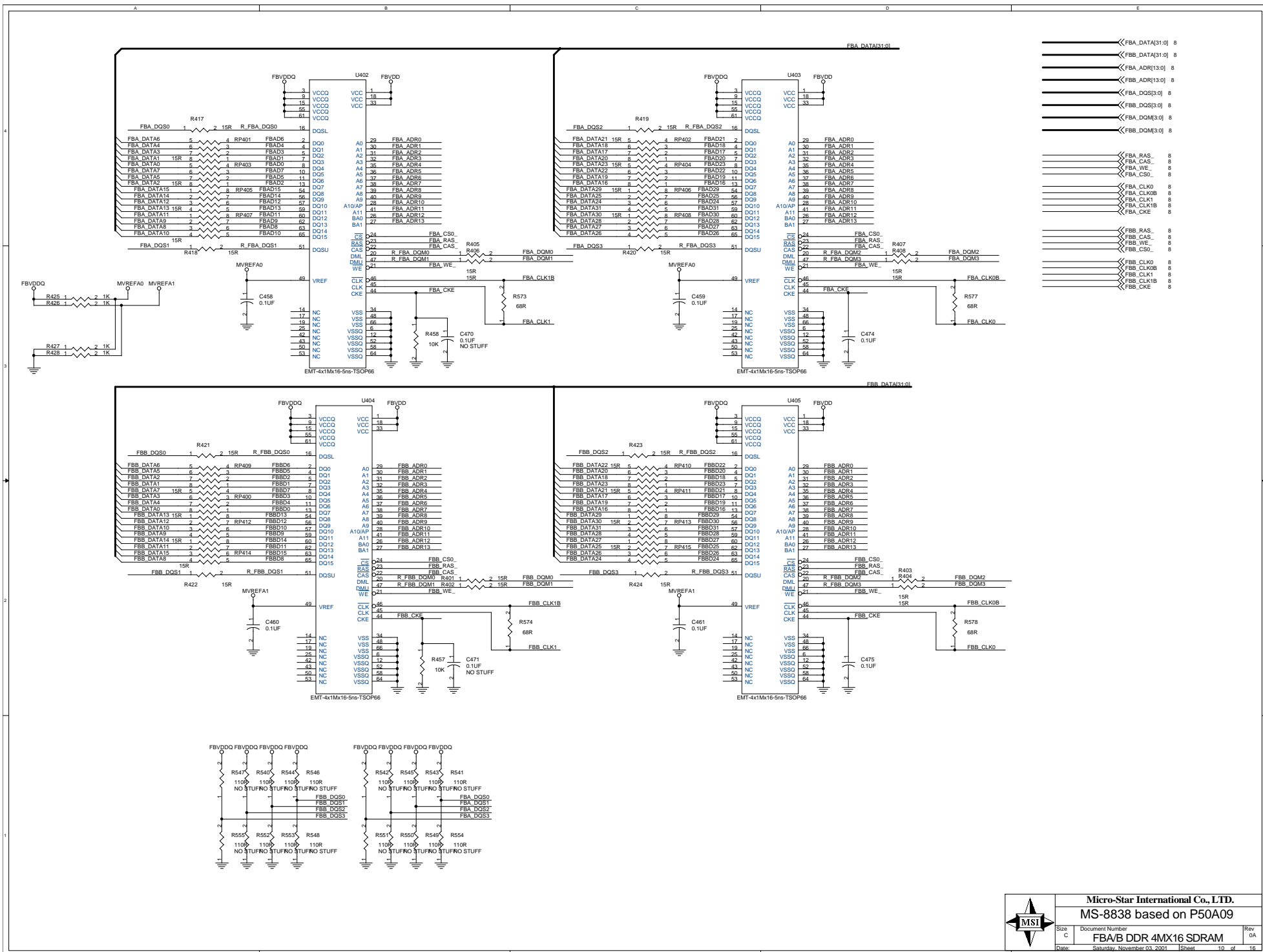
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 <<FBC_CLK0B_ 11
 <<FBC_CLK1_ 11
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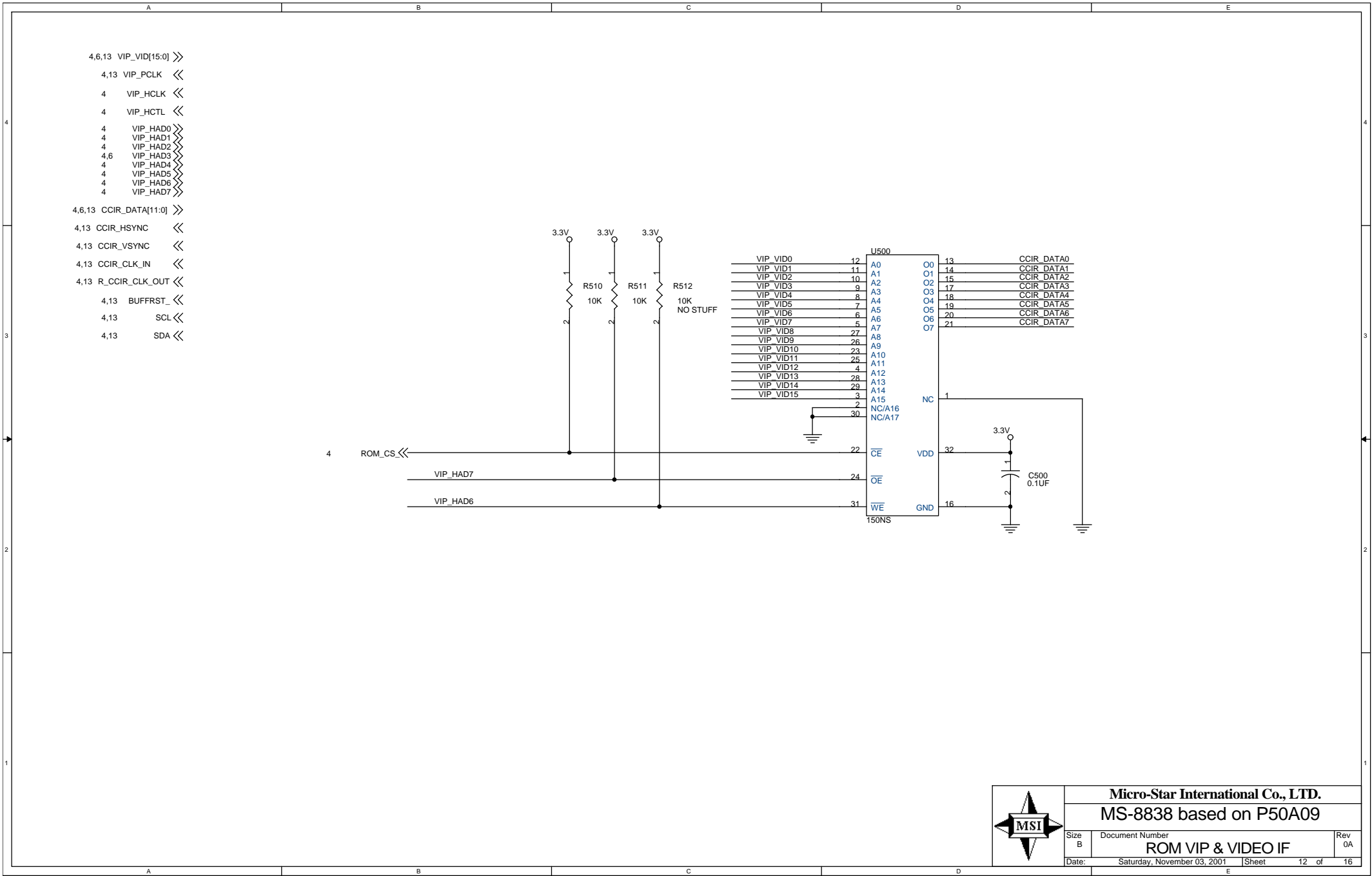
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 <<FBD_CS0_ 11

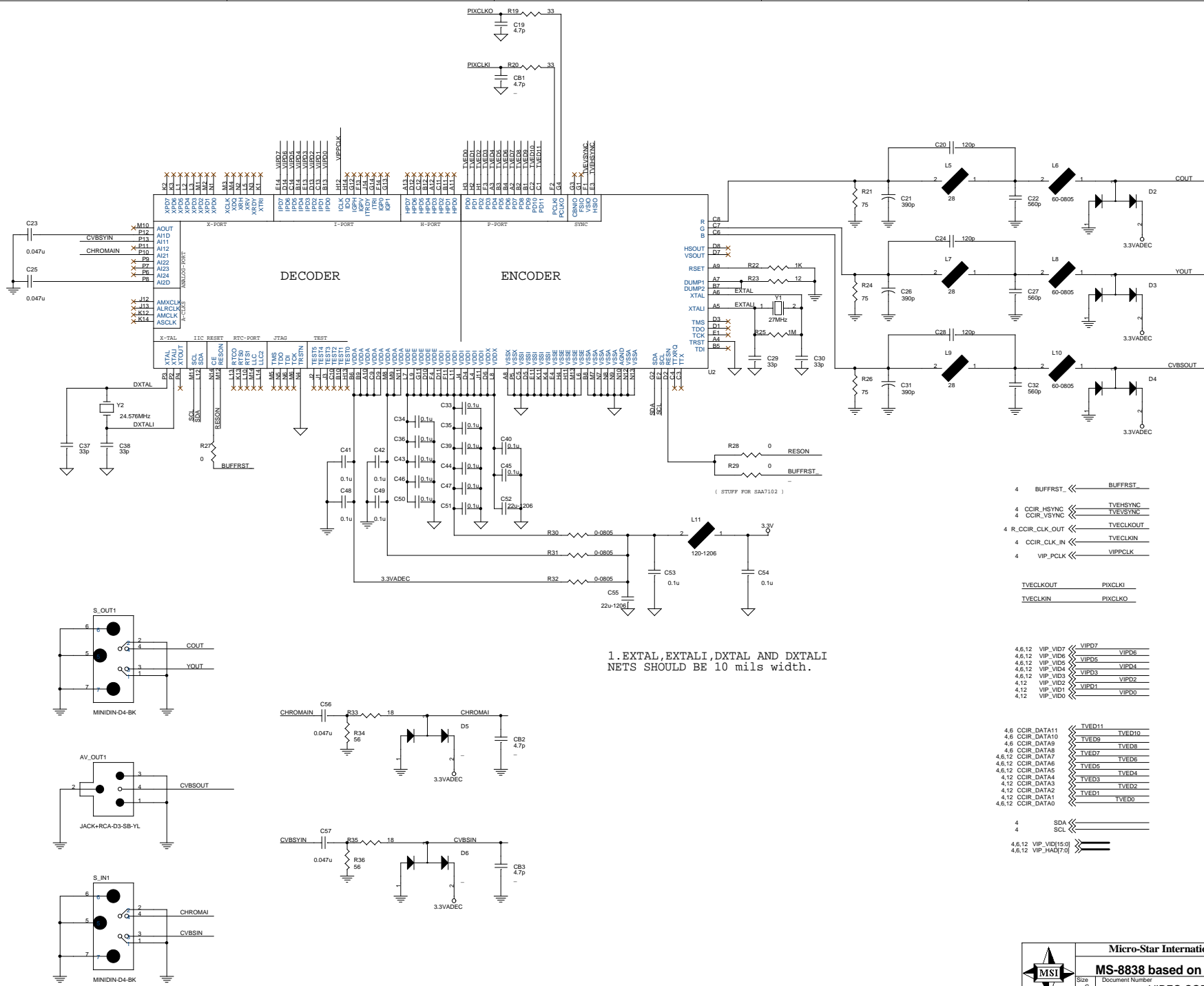
<<FBD_CLK0_ 11
 <<FBD_CLK0B_ 11
 <<FBD_CLK1_ 11
 <<FBD_CKE_ 11











1. EXTAL, EXTALI, DXTAL AND DXTALI
NETS SHOULD BE 10 mils width.

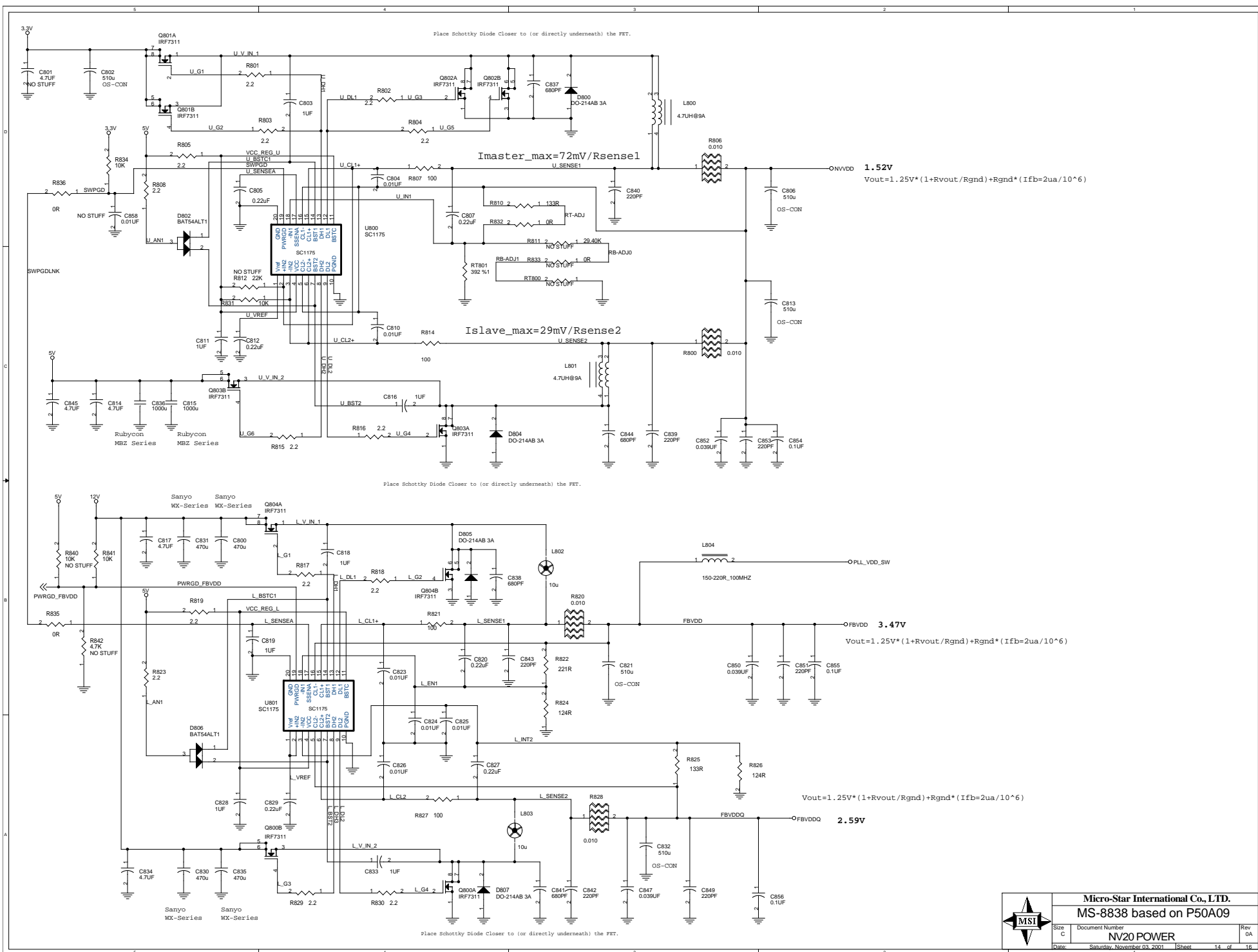
4 BUFFRST << BUFFRST
4 CCIR_HSYNC << TVEHSYNC
4 CCIR_VSYNC << TVEVSYNC
4 R_CLK_OUT << TVECLKOUT
4 CCIR_CLK_IN << TVECLKIN
4 VIP_PCLK << VIPPCLK

TVECLKOUT << PIXCLKI
TVECLKIN << PIXCLKO

4.6.12 VIP_VID7 << VIPD7
4.6.12 VIP_VID6 << VIPD6
4.6.12 VIP_VID5 << VIPD5
4.6.12 VIP_VID4 << VIPD4
4.6.12 VIP_VID3 << VIPD3
4.12 VIP_VID2 << VIPD2
4.12 VIP_VID1 << VIPD1
4.12 VIP_VID0 << VIPD0

4.6 CCIR_DATA11 << TVED11
4.6 CCIR_DATA10 << TVED10
4.6 CCIR_DATA9 << TVED9
4.6 CCIR_DATA8 << TVED8
4.6.12 CCIR_DATA7 << TVED7
4.6.12 CCIR_DATA6 << TVED6
4.6.12 CCIR_DATA5 << TVED5
4.12 CCIR_DATA4 << TVED4
4.12 CCIR_DATA3 << TVED3
4.12 CCIR_DATA2 << TVED2
4.12 CCIR_DATA1 << TVED1
4.6.12 CCIR_DATA0 << TVED0

4 SDA << SDA
4 SCL << SCL
4.6.12 VIP_VID15[0] << VIP_VID15[0]
4.6.12 VIP_HAD[7:0] << VIP_HAD[7:0]



MS-8838 based on P50A09

Rev	
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