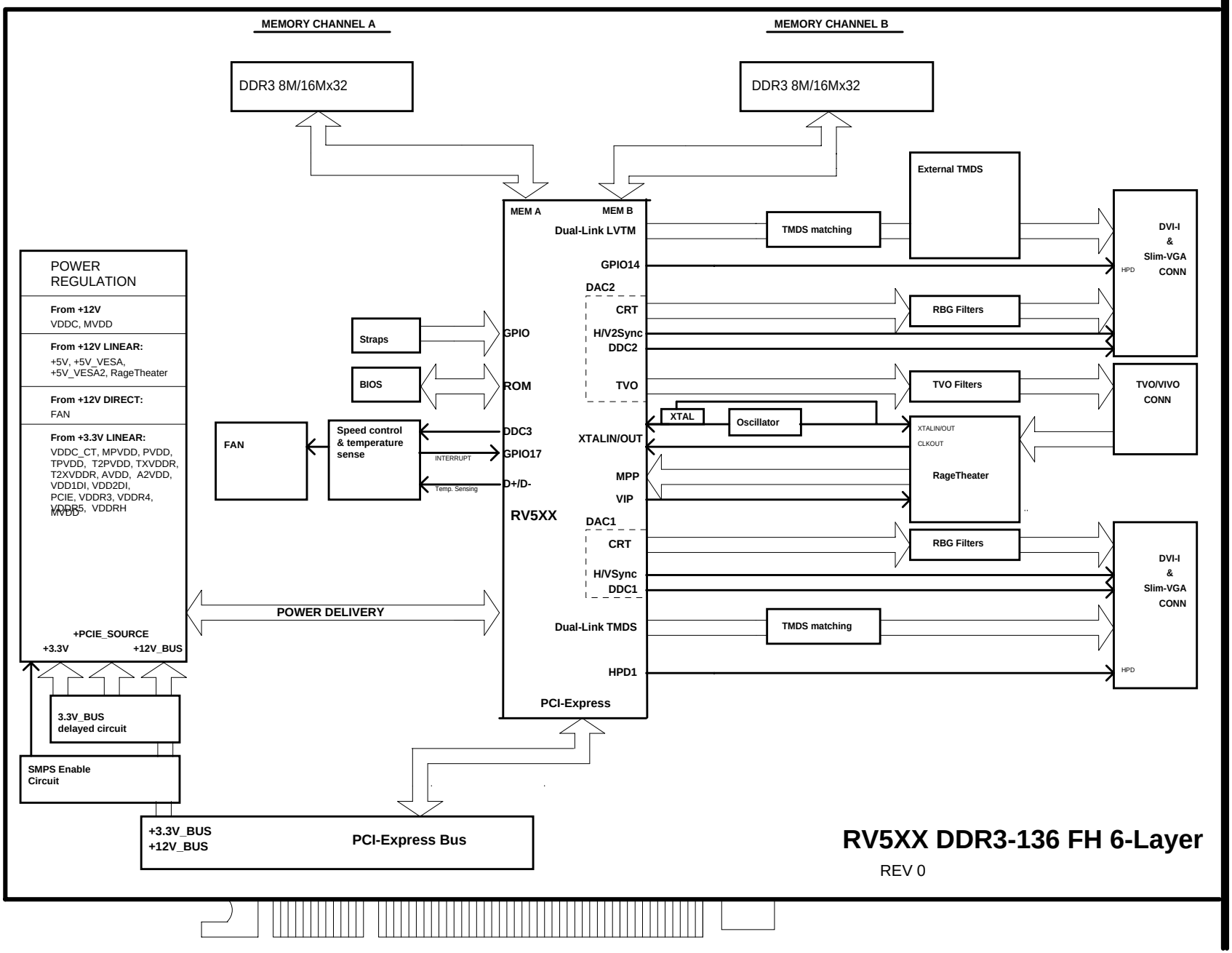
<variant Name>

Title	Schematic No.	Date:
RV530/RV515 256MB DDR3-136 Dual 2xDVI VIVO FH	105-A671xx-00	**Friday, October 07, 2005**

REVISION HISTORY

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	05/07/20	Design based on A676-00B and memory of A675-00B (pg 01) Delete redundant SMPS_EN circuits (pg 03) Remove TMDS joins and add TMDS2 terminations (pg 04) Add 1.8V option for VDDR4 and VDDR5 (pg 05) Add additional separate MVREF, QS# and address; remove ODT for DDR2 (pg 07) Add DVO port and GPIO7 for ext TMDS reset (pg 11) Change power sequence circuit for +5V and add 1.8V power supply (pg 12) Add memory based on A675-00B (pg 13) Add ext TMDS HDCP support (pg 14) Remove HPD2 option (pg 15) Add 2nd DVI connector (pg 16) Remove C3241, C3242, C3243, C3244 and C3245. Remove +MVDDC/+MVDDQ reference, use only +MVDD
1	00B	09/14/05	Added crossfire slave requirements
2	00	10/03/05	Production Release



RV5XX DDR3-136 FH 6-Layer

REV 0

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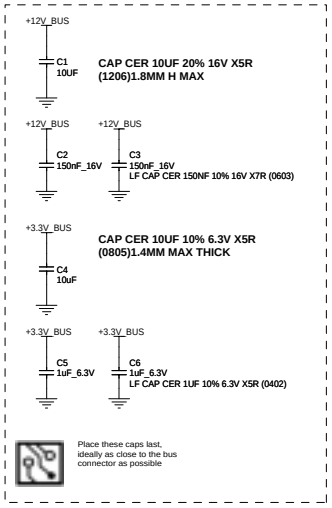
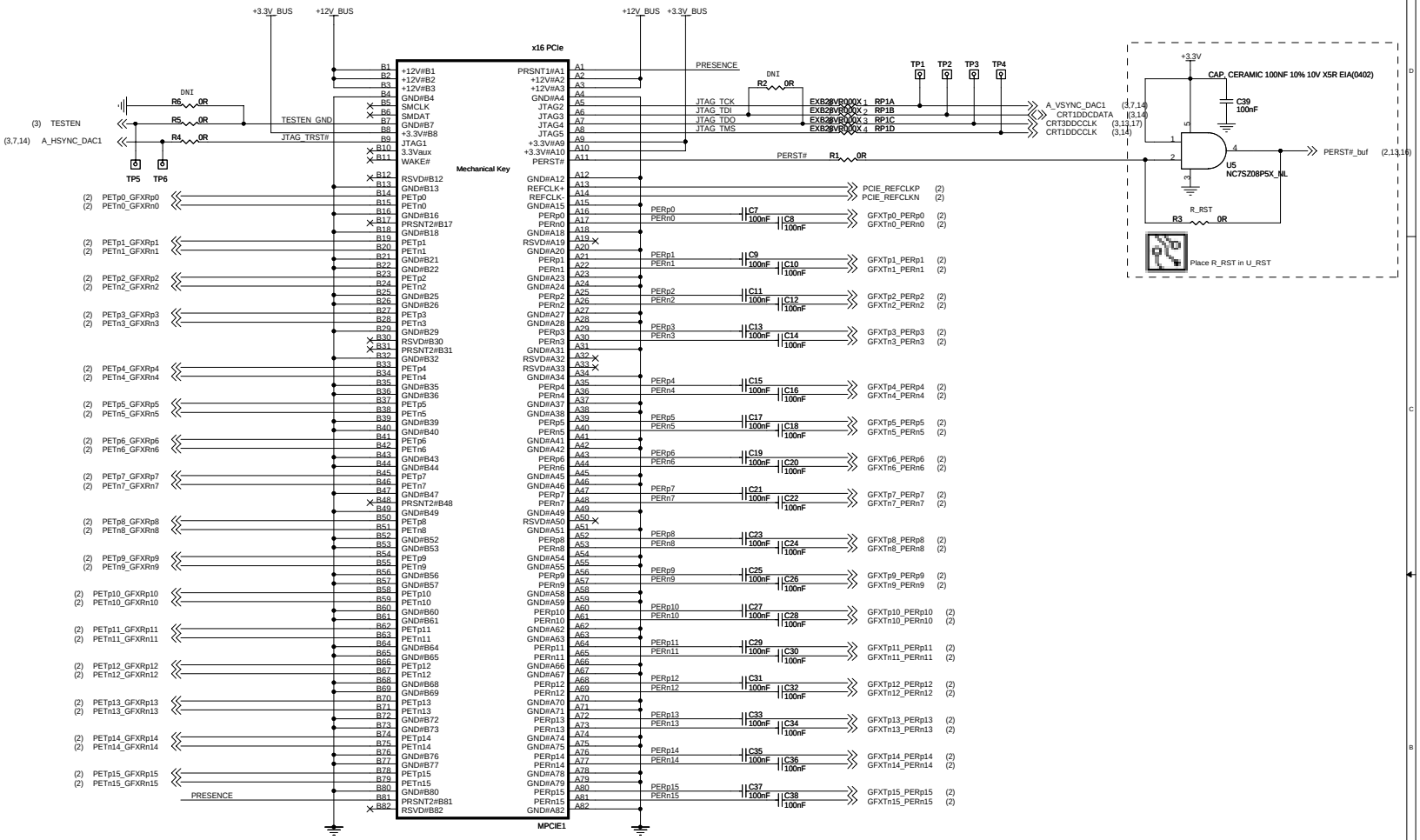
(905) 882-2600

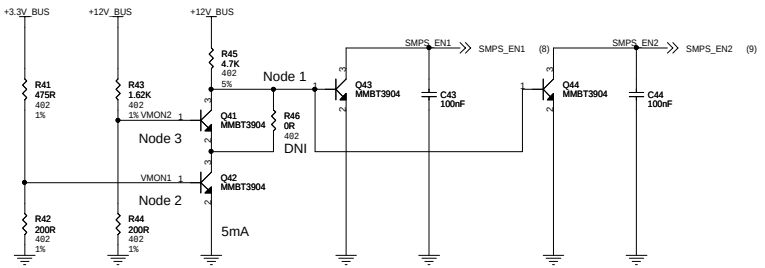
Title	RV530/RV515 256MB DDR3-136 Dual 2xDVI VIVO FH	
Size C	Document Number 105-A671xx-00	Rev 2
Date: Friday, October 07, 2005	Sheet 20 of 20	

PCI-EXPRESS EDGE CONNECTOR





POWER SEQUENCING



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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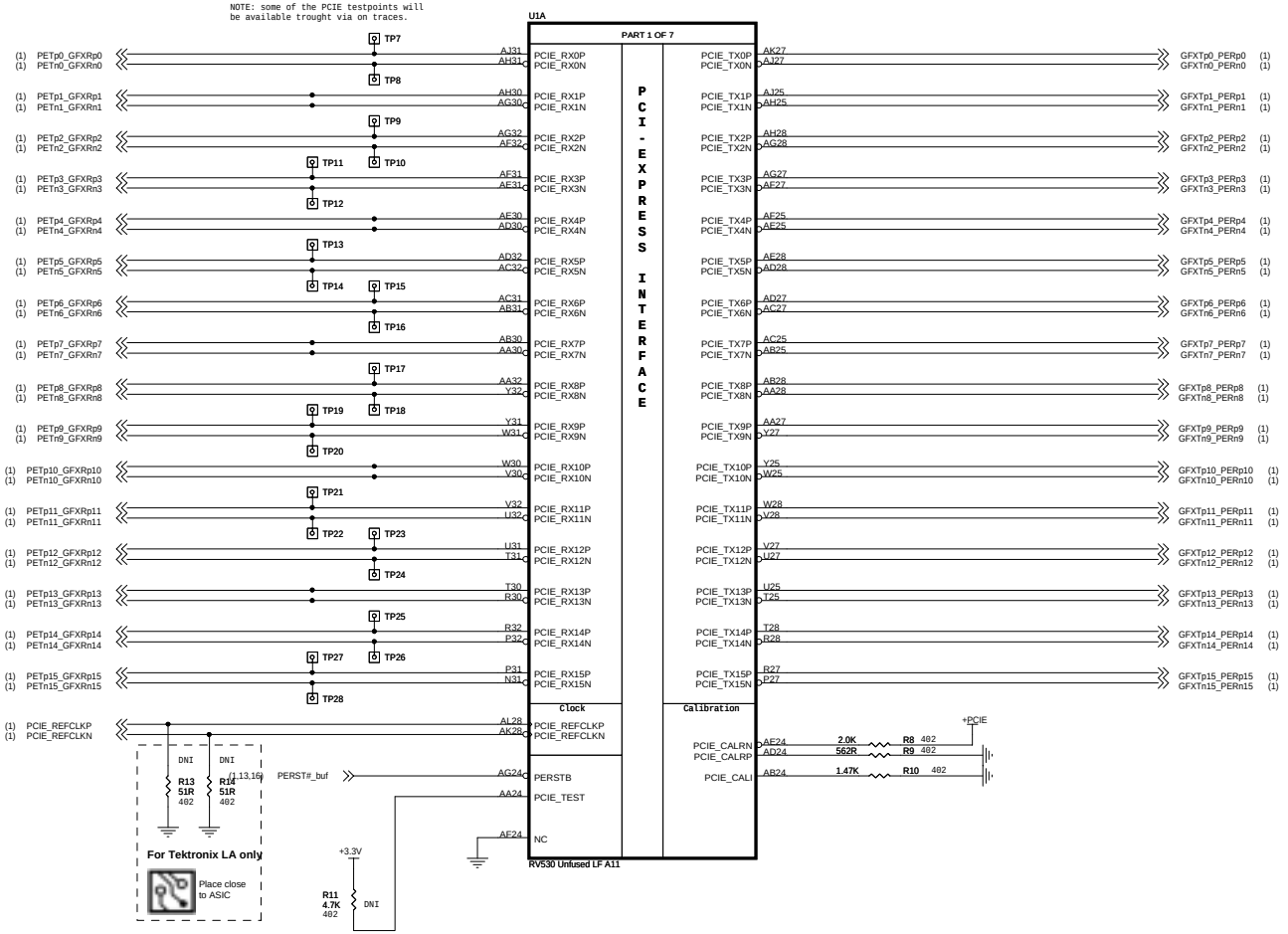
Size C	Document Number 105-A671xx-00	Rev 2
Date: Friday, October 07, 2005	Sheet 1 of 20	



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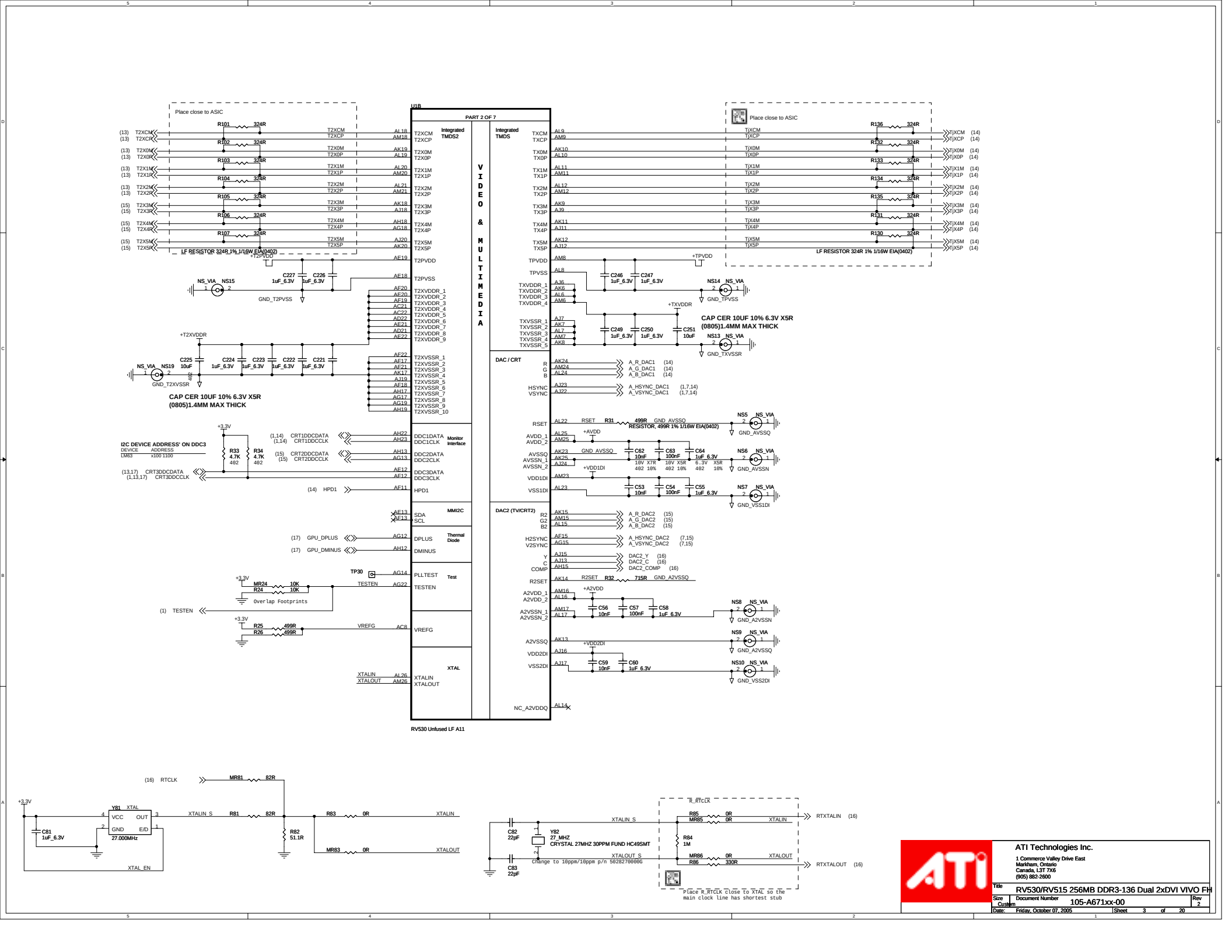
Size C	Document Number 105-A671xx-00	Rev 2
Date: Friday, October 07, 2005	Sheet 2 of 20	



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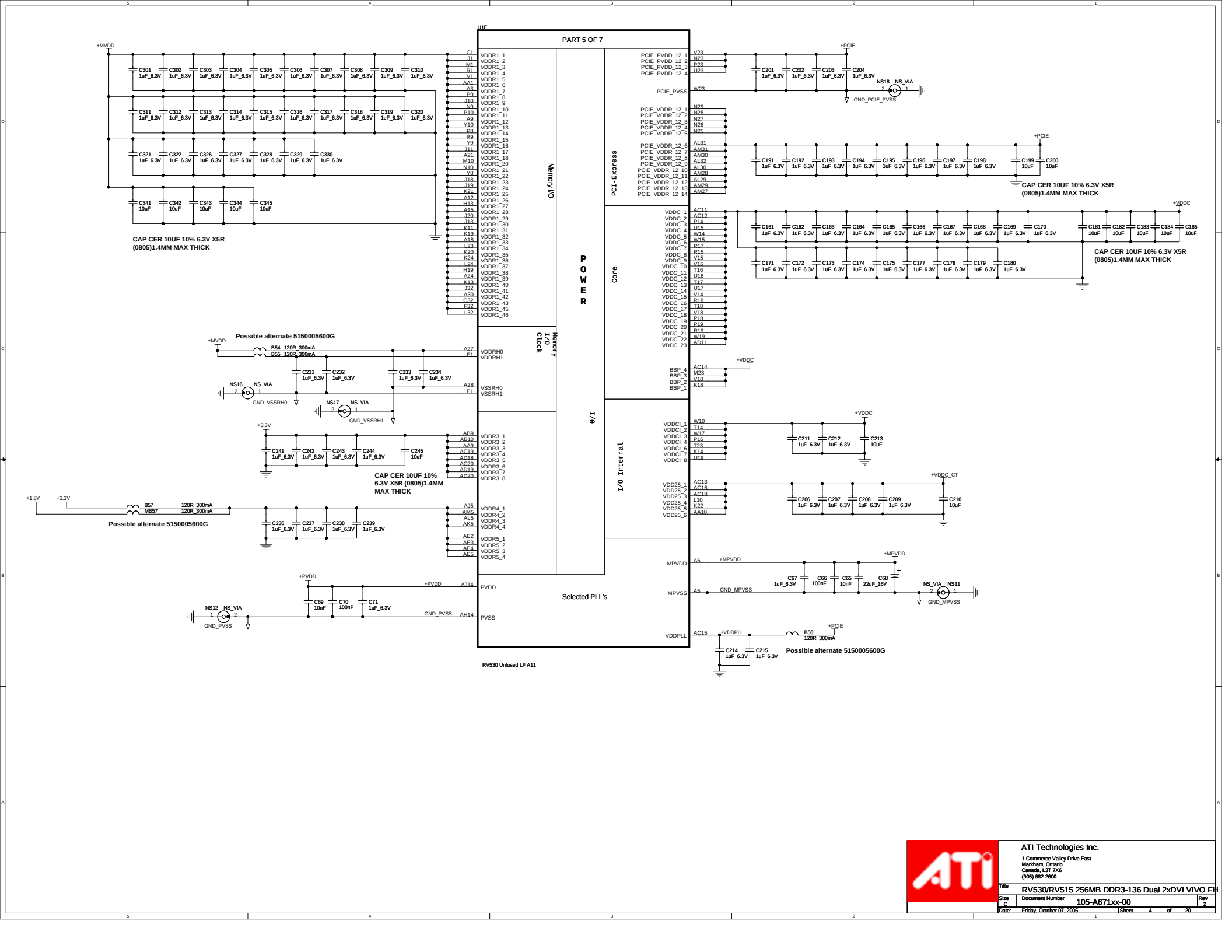
Document Number	105-A671xx-00
Rev	2
Date:	Friday, October 07, 2005
Sheet	3 of 20



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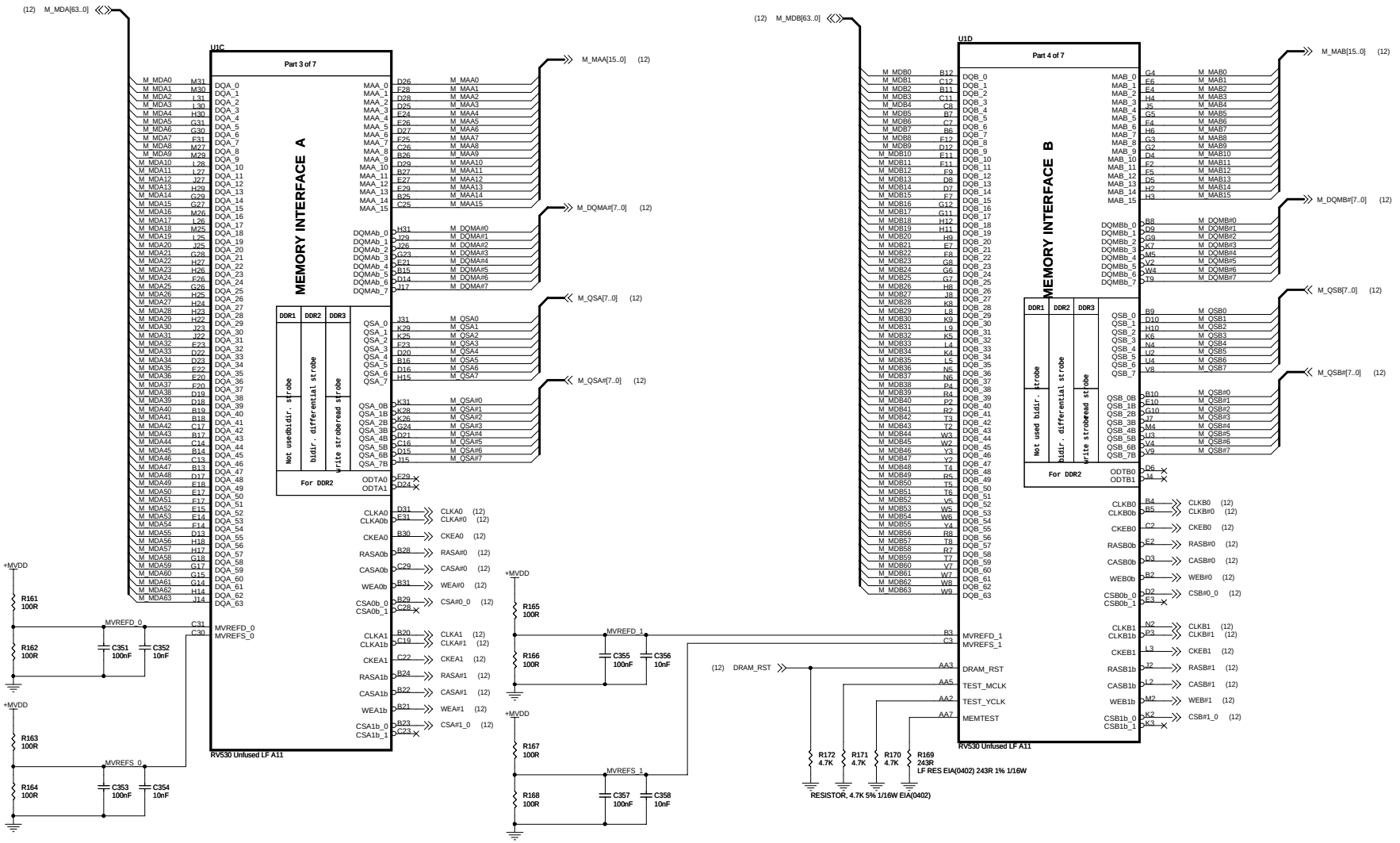
Size C	Document Number 105-A671xx-00	Rev 2
Date: Friday, October 07, 2005	Sheet 4 of 20	



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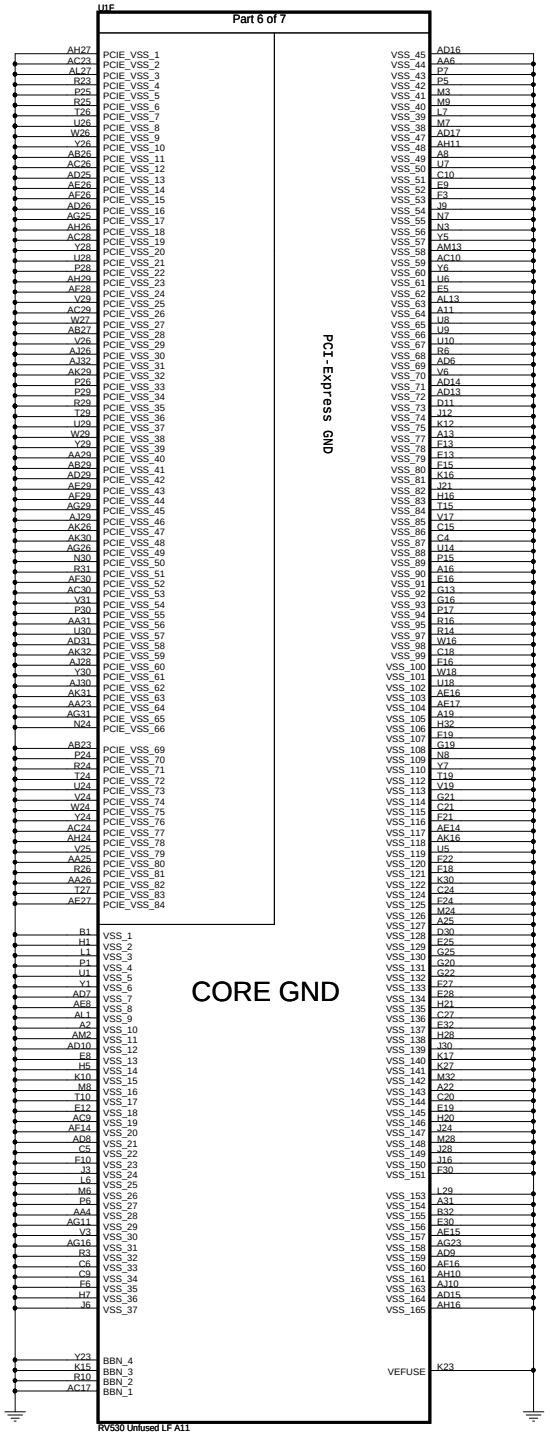
Date: Friday, October 07, 2005	Sheet 5 of 20	



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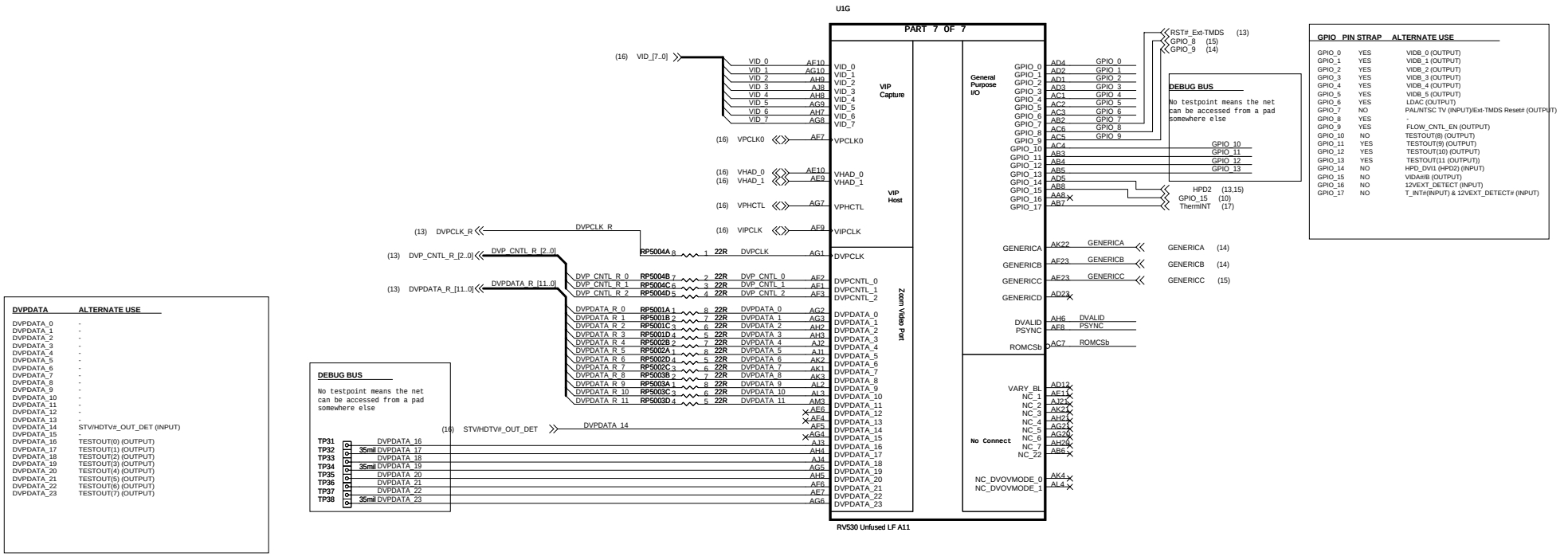
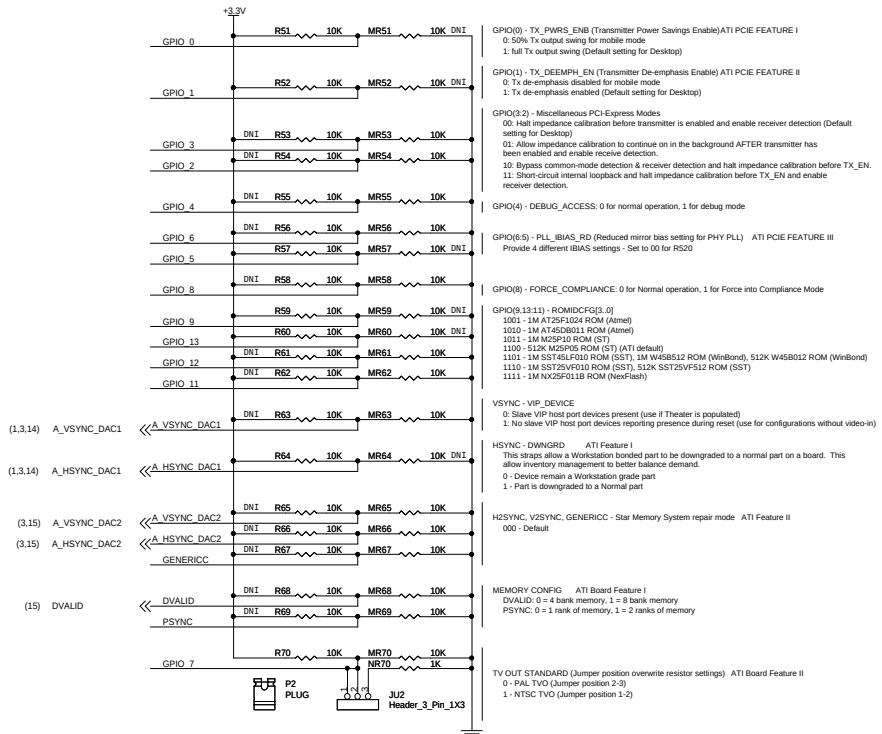
Date: Friday, October 07, 2005	Sheet 6 of 20	



PIN BASED STRAPS



GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(3:2) - Miscellaneous PCI-Express Modes
00: Hall impedance calibration before transmitter is enabled and enable receiver detection (Default setting for Desktop)
01: Allow impedance calibration to continue on in the background AFTER transmitter has been enabled and enable receive detection.
10: Bypass common-mode detection & receiver detection and halt impedance calibration before TX_EN.
11: Short-circuit internal loopback and halt impedance calibration before TX_EN and enable receiver detection.

GPIO(4) - DEBUG_ACCESS: 0 for normal operation, 1 for debug mode

GPIO(6:5) - PLL_IBIAS_RD (Reduced mirror bias setting for PHY PLL) ATI PCIE FEATURE III
Provide 4 different IBIAS settings - Set to 00 for R520

GPIO(8) - FORCE_COMPLIANCE: 0 for Normal operation, 1 for Force into Compliance Mode

GPIO(9,13:11) - ROMIDCFG[3..0]
1001 - 1M AT25F1024 ROM (Atmel)
1010 - 1M AT45DB011 ROM (Atmel)
1011 - 1M M25P10 ROM (ST)
1100 - 512K M25P05 ROM (ST) (ATI default)
1101 - 1M SST45LF010 ROM (SST), 1M W45B512 ROM (WinBond), 512K W45B012 ROM (WinBond)
1110 - 1M SST25VF010 ROM (SST), 512K SST25VF512 ROM (SST)
1111 - 1M NX25F011B ROM (NexFlash)

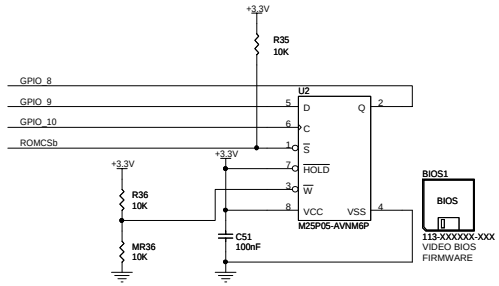
VSYNC - VIP_DEVICE
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

HSYNC - DWNGRD ATI Feature I
This straps allow a Workstation bonded part to be downgraded to a normal part on a board. This allow inventory management to better balance demand.
0 - Device remain a Workstation grade part
1 - Part is downgraded to a Normal part

H2SYNC, V2SYNC, GENERICC - Star Memory System repair mode ATI Feature II
000 - Default

MEMORY CONFIG ATI Board Feature I
DVALID: 0 = 4 bank memory, 1 = 8 bank memory
PSYNC: 0 = 1 rank of memory, 1 = 2 ranks of memory

TV OUT STANDARD (Jumper position overwrite resistor settings) ATI Board Feature II
0 - PAL TVO (Jumper position 2-3)
1 - NTSC TVO (Jumper position 1-2)



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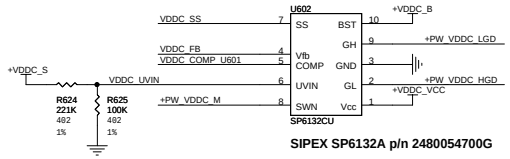
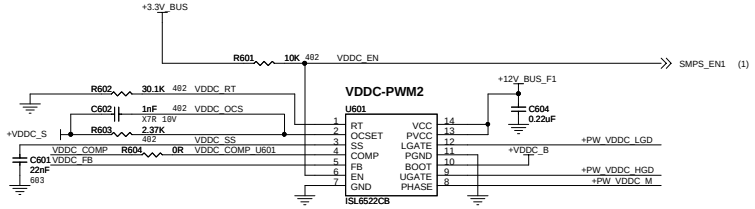
Size C	Document Number 105-A671xx-00		Rev 2
Date: Friday, October 07, 2005		Sheet 7 of 20	

VDDC-PWM1



SIPEX SP6132A p/n 2480054700G



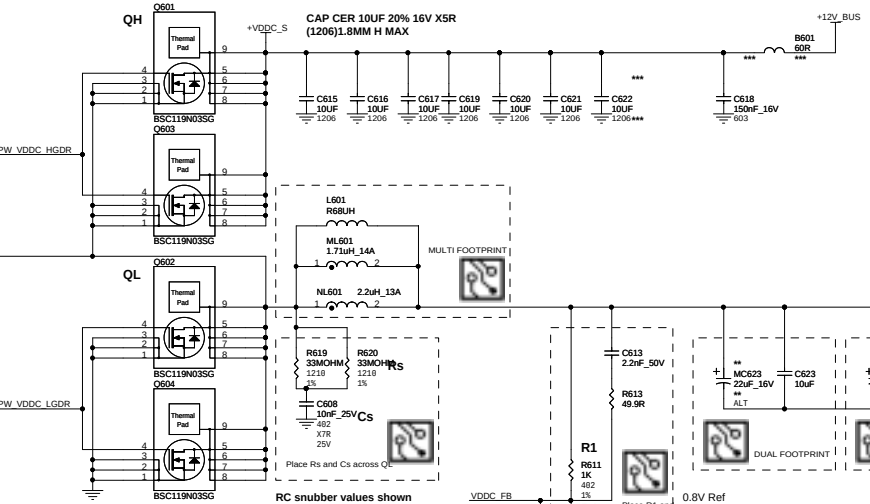
VDDC-PWM2

INTERSIL ISL6522/ISL6535

RICHTEK RT9232/RT9232A

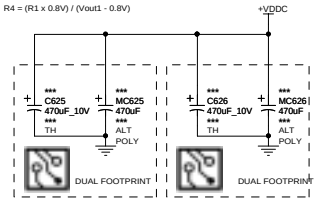
ANPEC APW7062A

ANPEC APW7062B



0.8V Ref

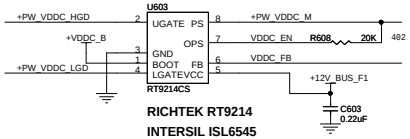
R4 = (R1 x 0.8V) / (Vout1 - 0.8V)



CAP AE 470UF 20% 10V 10x12 .5MM LOW ESR

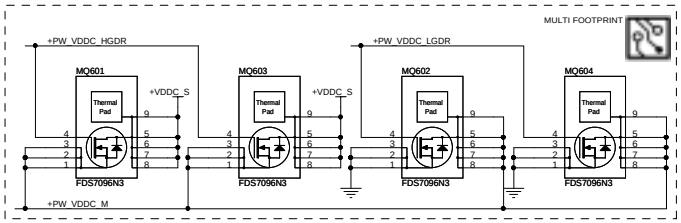
LF CAP, AL/POLY, 470UF 6.3V, LOW ESR, 8MM DIA, SMT

VDDC-PWM3

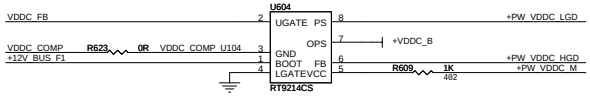


RICHTEK RT9214

INTERSIL ISL6545

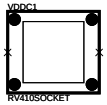


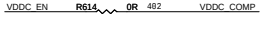
VDDC-PWM4



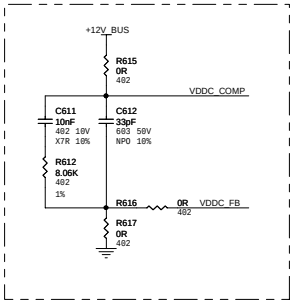
ANPEC APW7061A

This symbol is used for 103 SMPS p/n.

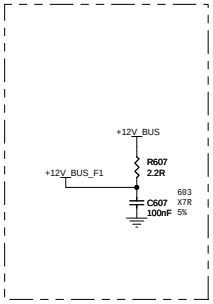




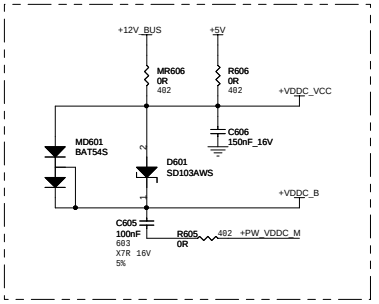
COMPENSATION CIRCUIT



FILTERED +12V_BUS



BOOT CIRCUIT



Regulator for VDDC (ASIC Core)

Vout = 1V ~ 1.3V

Part	Vout	R1	R2
0.8V Ref	1.2V	1.00K 1%	2.00K 1%
	1.25V	1.00K 1%	1.78K 1%
	1.3V	1.00K 1%	1.6K 1%

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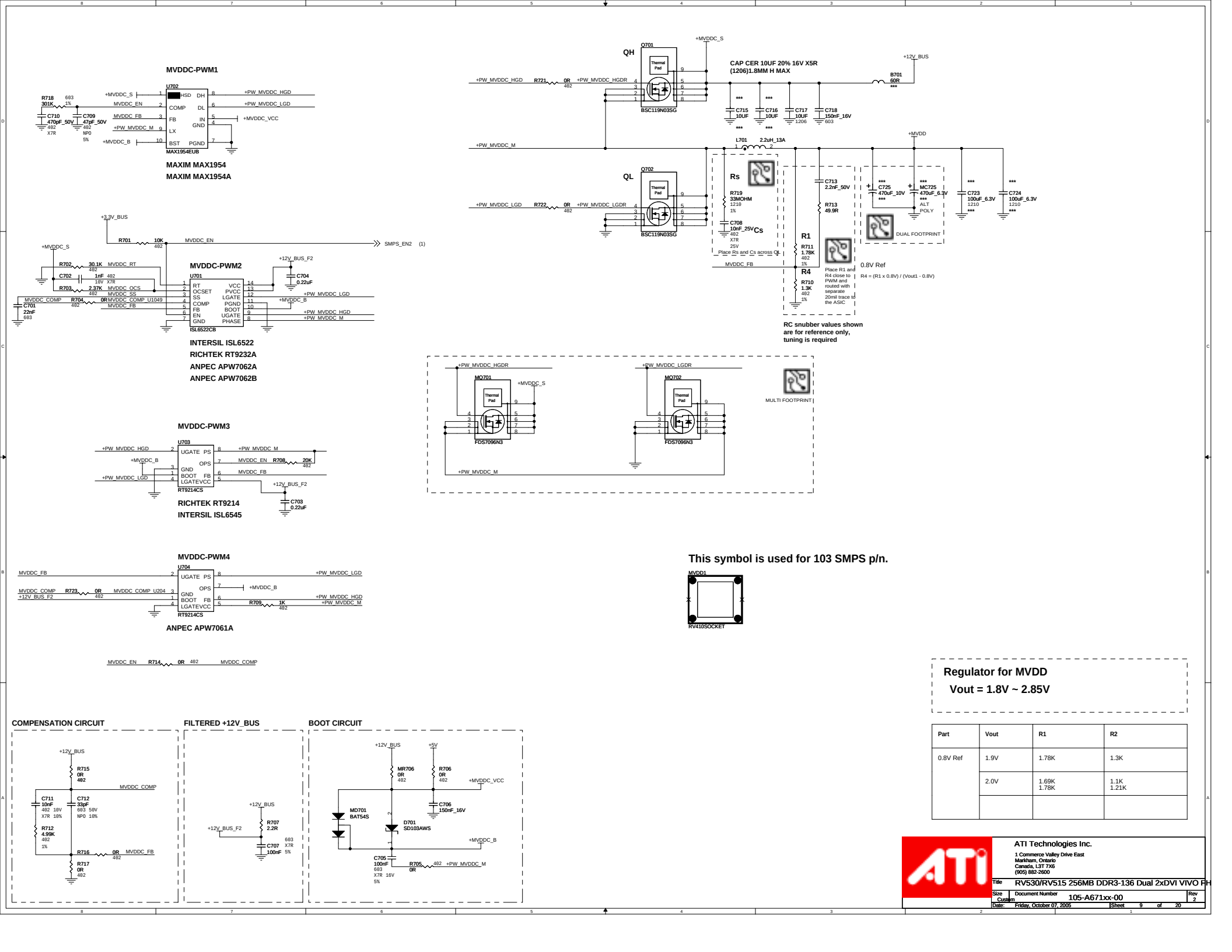
Size: Custom	Document Number: 105-A671xx-00	Rev: 2
Date: Friday, October 07, 2005	Sheet 8 of 20	



Part	Vout	R1	R2
0.8V Ref	1.9V	1.78K	1.3K
	2.0V	1.69K 1.78K	1.1K 1.21K

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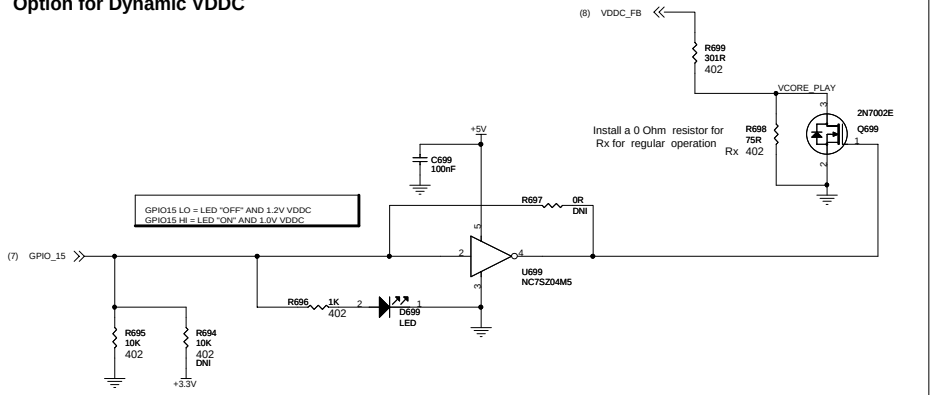
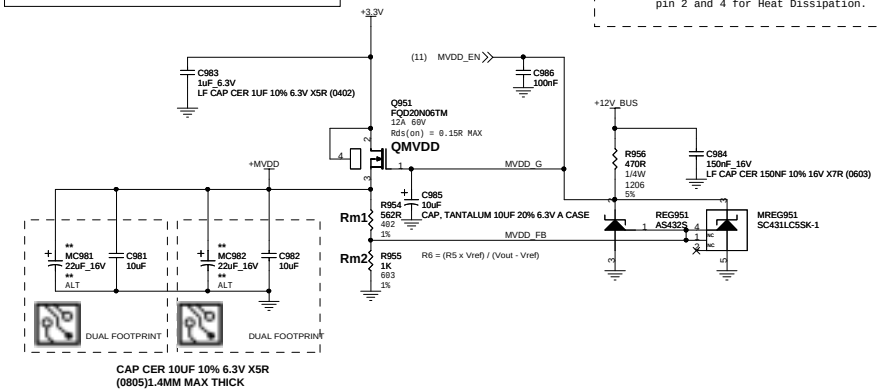
Size: Custom	Document Number: 105-A671xx-00	Rev: 2
Date: Friday, October 07, 2005	Sheet 9 of 20	

Option for Dynamic VDDC



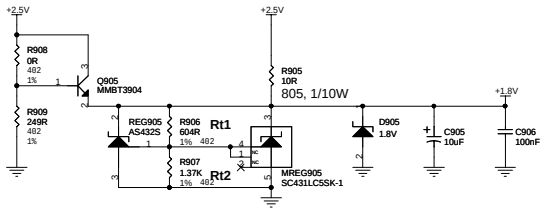
Regulator for +MVDDQ
Vout = 1.85V ~ 2.65V
Iout = 1.7A MAX
P_QMVDD = 2.5W MAX

Place Big Copper Area Under QMVDD pin 2 and 4 for Heat Dissipation.



CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

Voltage Req.	Rm1		Rm2		
2.85V					
2.55V	22.1R	316022R100G	1.1K	3240110100G	2.5V Ref.
2.5V	0R	3150000000	DNI		2.5V Ref.
2.1V min	681R	3160681000G	953R	3240953000	1.24V Ref.
2.0V min	681R	3160681000G	1.1K	3240110100G	1.24V Ref.
1.9V min, 1.94V nom.	562R	3160562000G	1K	3160100100G	1.24V Ref.



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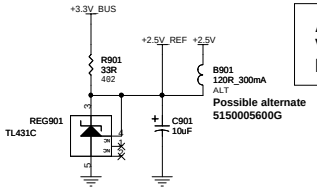
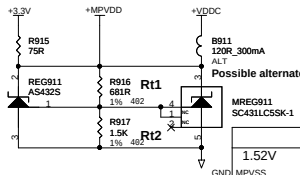
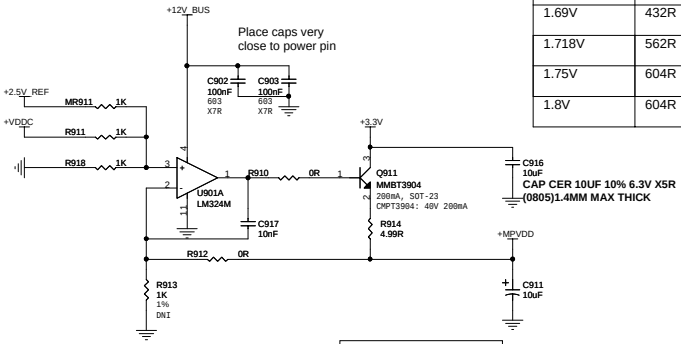
Size: Custom | Document Number: 105-A671xx-00 | Rev: 2
Date: Friday, October 07, 2005 | Sheet 10 of 20

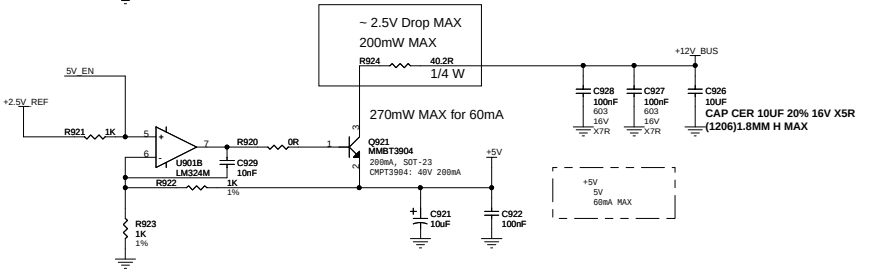
Alt regulator for +MPVDD
Vout = 1.2V (not tracking to VDDC)
Iout = 10mA MAX

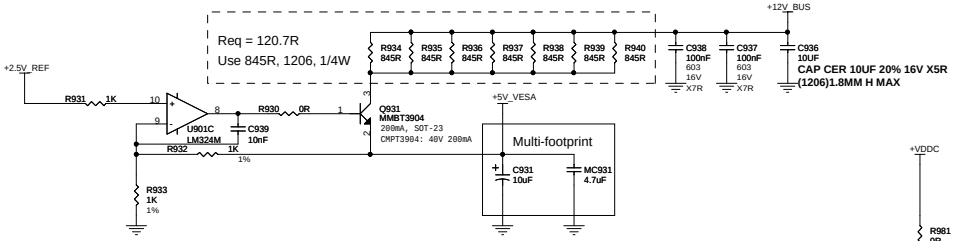


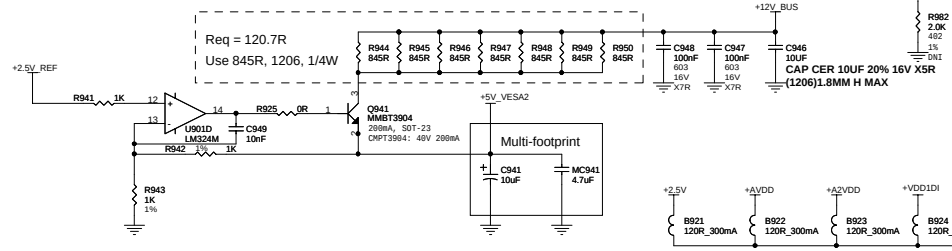


	Rt1		Rt2	
1.52V	432R	3240432000 3160432000	2.15K	3160215100
1.61V	432R	3240432000	1.5K 1.5K	3230015200 3160150100
1.69V	432R	3240432000	1.21K	3240121100
1.718V	562R	3240562000	1.5K 1.5K	3230015200 3160150100
1.75V	604R	3160604000	1.5K 1.5K	3230015200 3160150100
1.8V	604R	3160604000	1.37K	3160137100

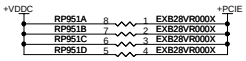


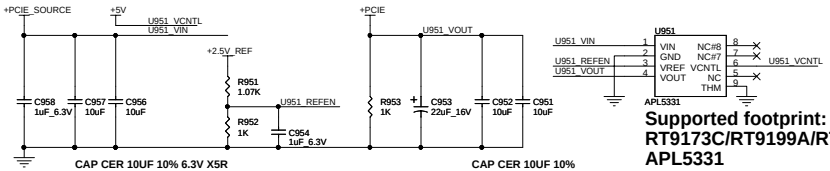






Optional regulator for +PCIE
Vout = 1.2V ~1.25V
Iout = 1.2A MAX



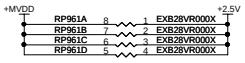


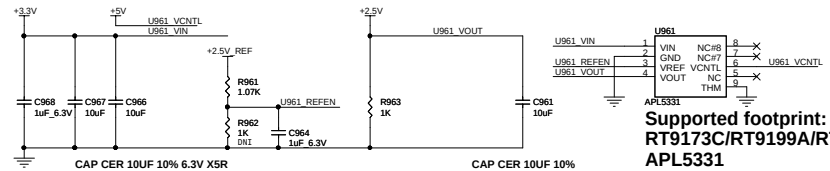
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

CAP CER 10UF 10%
6.3V X5R (0805)1.4MM
MAX THICK

Supported footprint:
RT9173C/RT9199A/RT9199
APL5331

Optional regulator for +2.5V
Vout = 2.5V
Iout = 600mA MAX



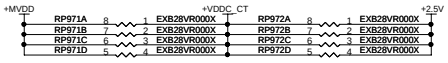


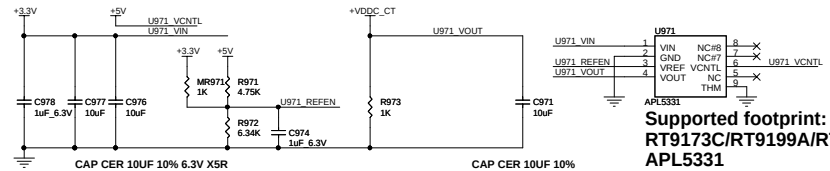
CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

CAP CER 10UF 10%
6.3V X5R (0805)1.4MM
MAX THICK

Supported footprint:
RT9173C/RT9199A/RT9199
APL5331

Optional Regulator for +VDDC_CT
Vout = 2.5V ~ 2.85V
Iout = 100mA MAX

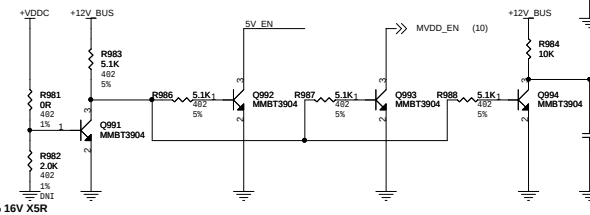


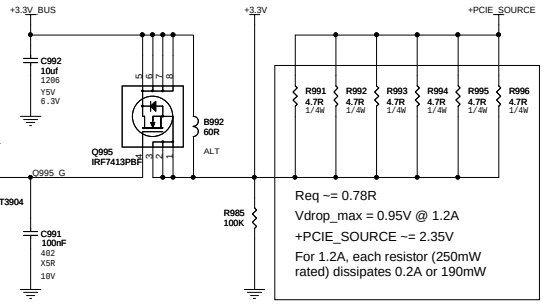


CAP CER 10UF 10% 6.3V X5R
(0805)1.4MM MAX THICK

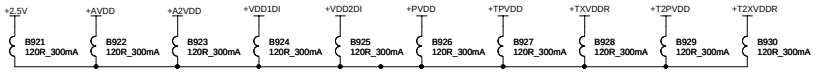
CAP CER 10UF 10%
6.3V X5R (0805)1.4MM
MAX THICK

Supported footprint:
RT9173C/RT9199A/RT9199
APL5331





Req ~= 0.78R
Vdrop_max = 0.95V @ 1.2A
+PCIE_SOURCE ~= 2.35V
For 1.2A, each resistor (250mW rated) dissipates 0.2A or 190mW



Possible alternate 5150005600G

RT9199 p/n 2480054800G (480mR RdsON Max)
RT9199A (300mR RdsON Max)
RT9173C (250mR RdsON Max)
APL5331 p/n 2480054200G (350mR MAX for 2A)

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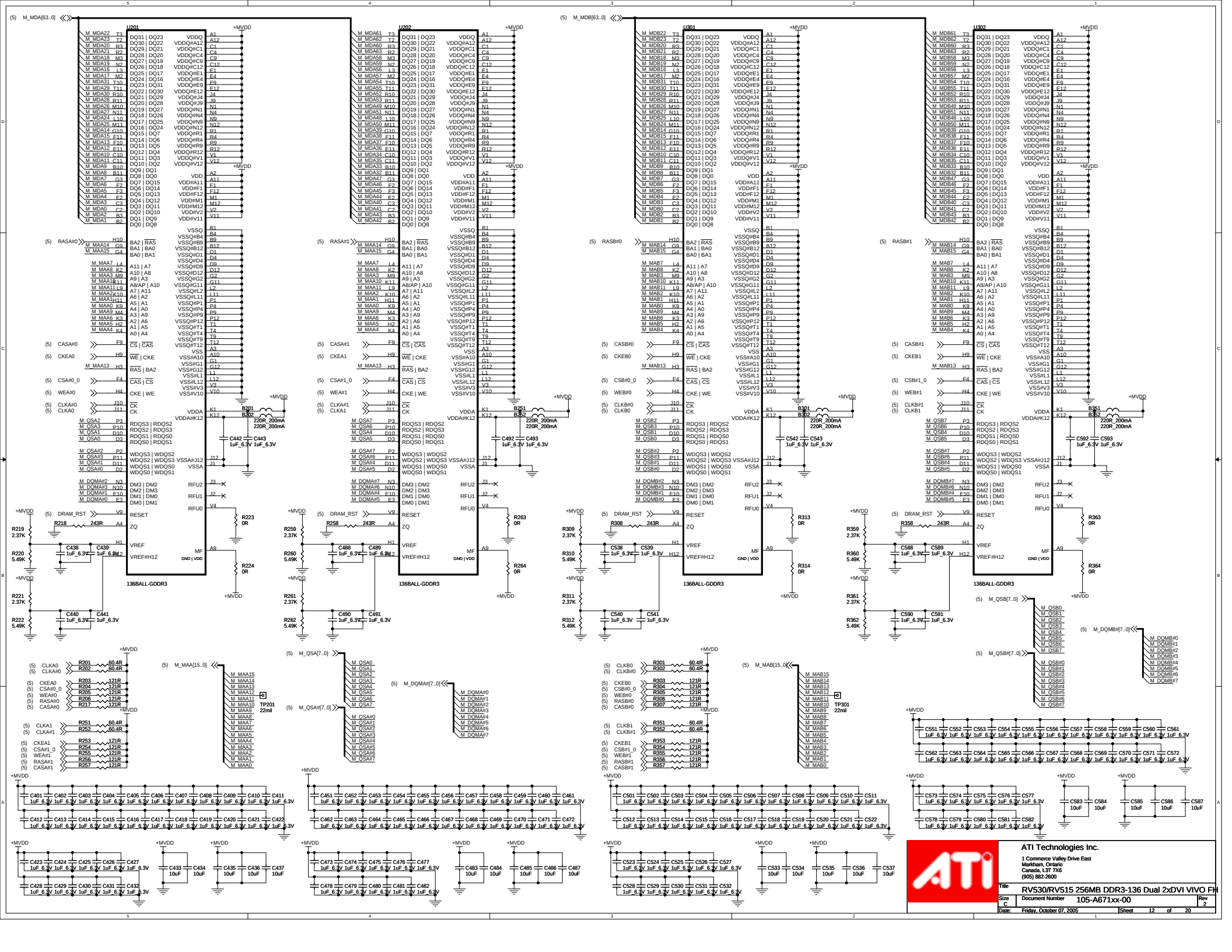
Title	RV530/RV515 256MB DDR3-136 Dual 2xDVI VIVO FH	
Size C	Document Number 105-A671xx-00	Rev 2
Date: Friday, October 07, 2005	Sheet 11 of 20	


U201
U202
U301
U302
136BALL-GDDR3
M_MDA[63..0]
M_MDB[63..0]
RASA#0
RASA#1
RASB#0
RASB#1
CASA#0
CASA#1
CASB#0
CASB#1
CKEA0
CKEA1
CKEB0
CKEB1
CSA#0_0
CSA#1_0
CSB#0_0
CSB#1_0
WEA#0
WEA#1
WEB#0
WEB#1
CLKA#0
CLKA#1
CLKB#0
CLKB#1
DRAM_RST
M_MAA[15..0]
M_MAB[15..0]
M_QSA[7..0]
M_QSB[7..0]
M_DQMA#[7..0]
M_DQMB#[7..0]
TP201
TP301
22mil
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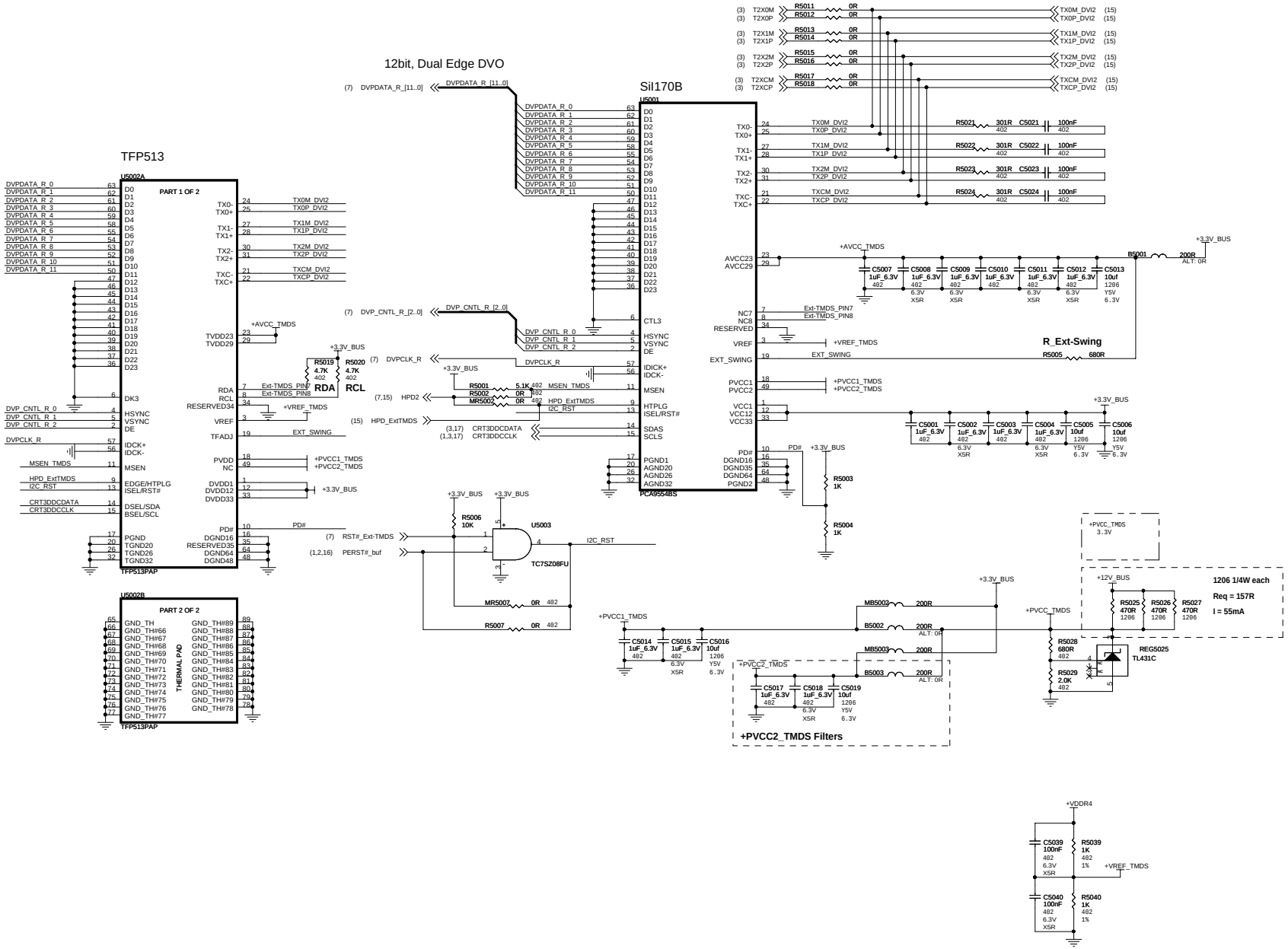
RV530/RV515 256MB DDR3-136 Dual 2xDVI VIVO FH
105-A671xx-00
Friday, October 07, 2005
12 of 20



STUFFING OPTIONS

EXT TMDS TX TO BE USED	MUST INSTALL	MUST NOT INSTALL	CAN BE REMOVED
Sil170B	Sil170B, +PVCC2_TMDS Filters R_Ext-Swing =	TFP513	RDA, RCL
TFP513	TFP513, RDA, RCL 505R <= R_Ext-Swing <= 515R	Sil170B	(Optional) +PVCC2_TMDS Filters

NOTE:
1 - Other components are to be installed.
2 - Components marked as DNI should not be installed. They should only be installed if default board settings are to be changed in which case other components may have to be adjusted accordingly.

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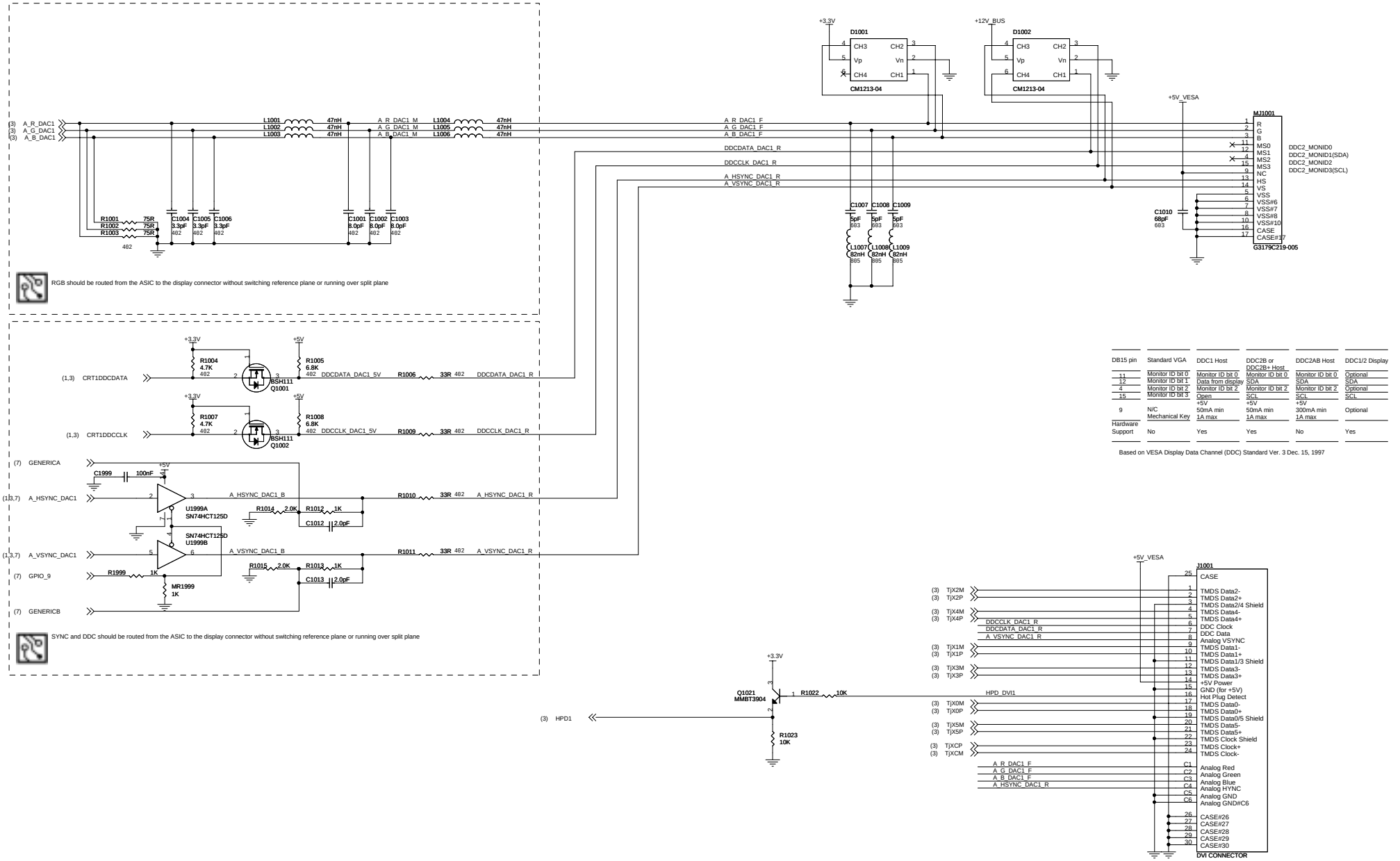
Title	RV530/RV515 256MB DDR3-136 Dual 2xDVI VIVO FH	
Size: Custom	Document Number: 105-A671xx-00	Rev: 2
Date: Friday, October 07, 2005	Sheet 13 of 20	



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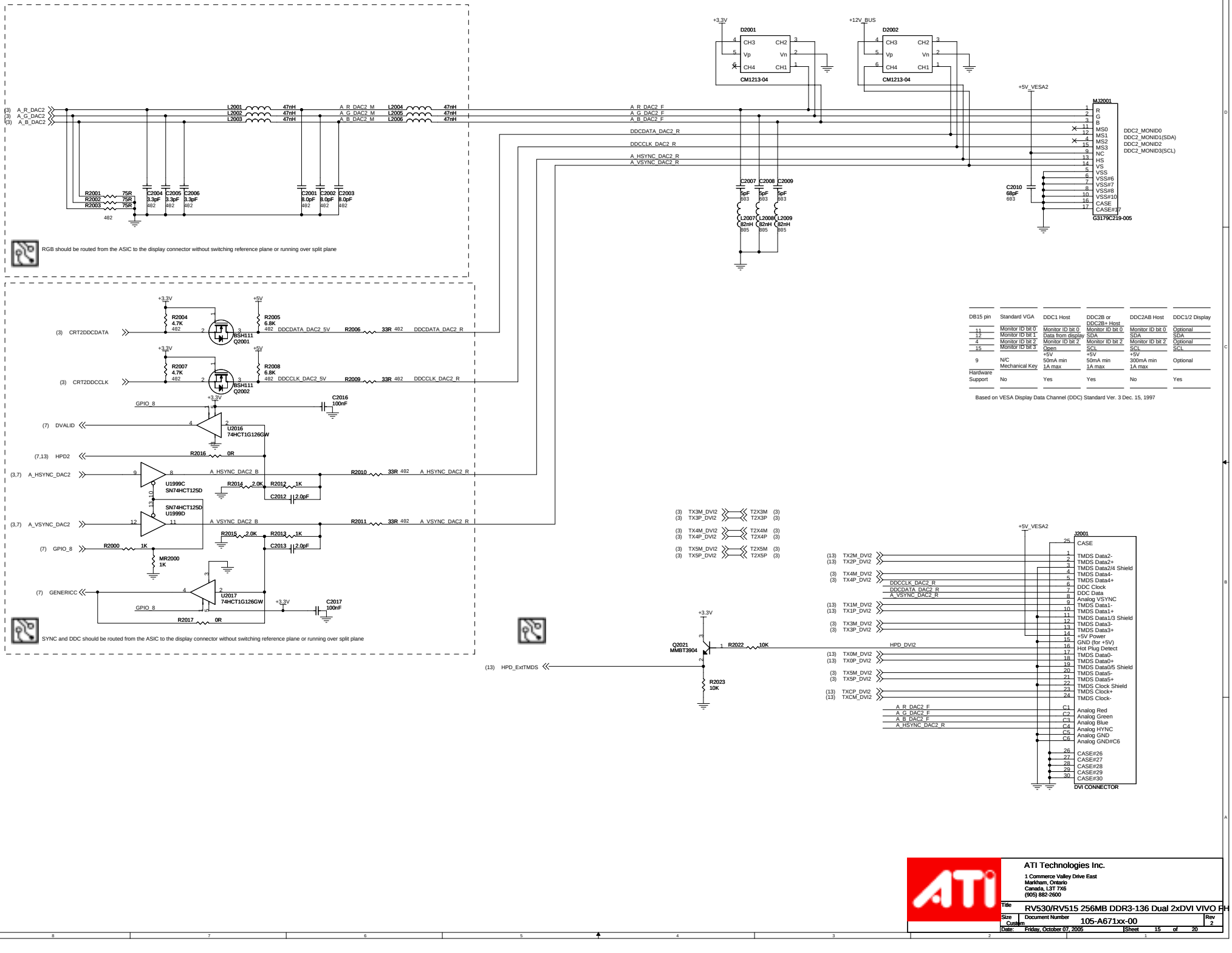
Title	RV530/RV515 256MB DDR3-136 Dual 2xDVI VIVO FH		
Size: Custom	Document Number: 105-A671xx-00		Rev: 2
Date: Friday, October 07, 2005	Sheet 14 of 20		



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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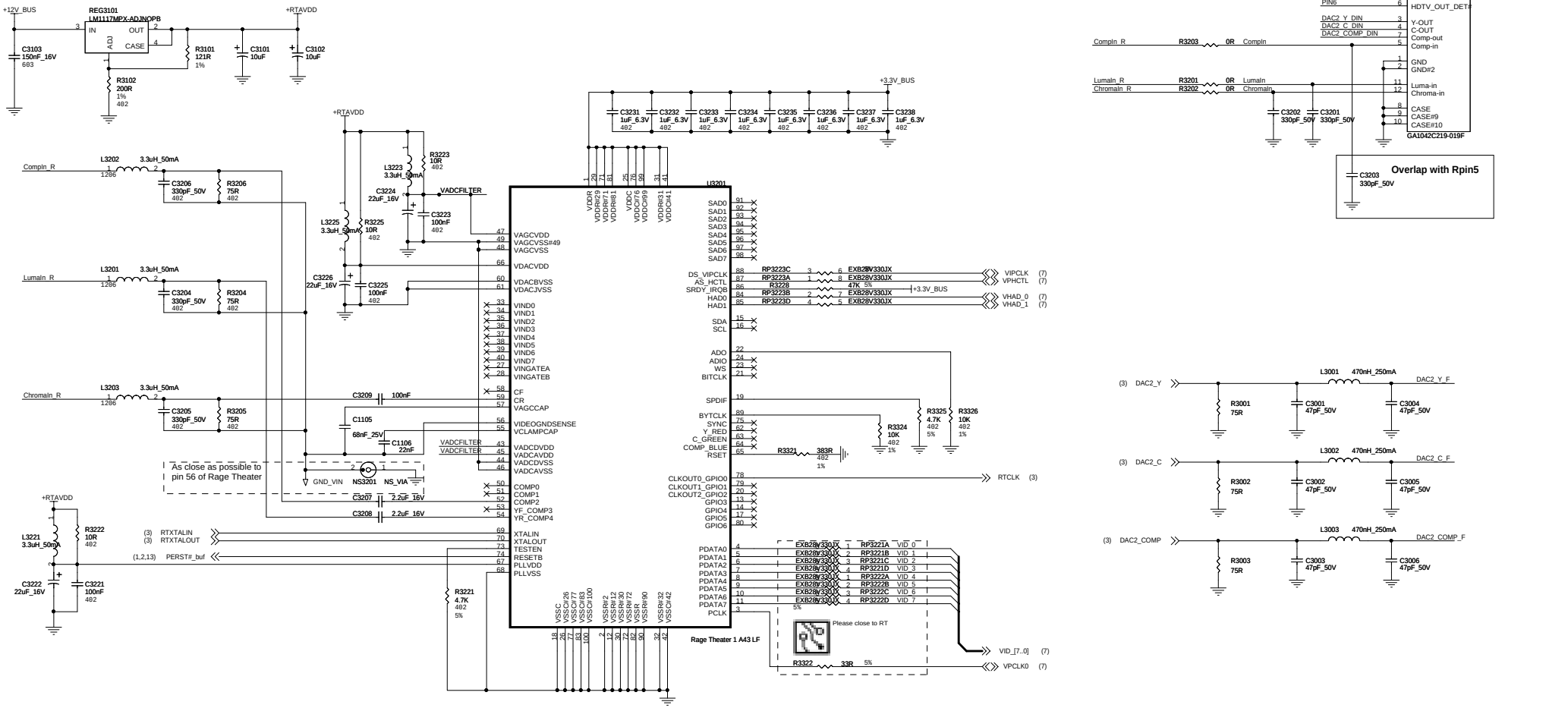
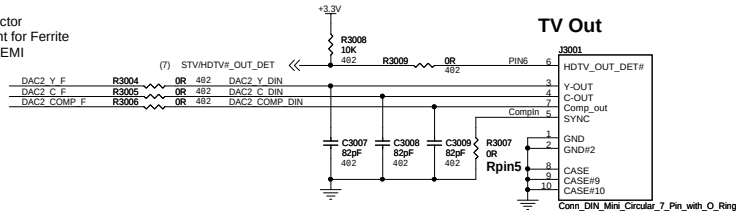
Size: Custom	Document Number: 105-A671xx-00	Rev: 2
Date: Friday, October 07, 2005	Sheet 15 of 20	

+RTAVDD
Vout = 3.3V
Iout = 125mA MAX, 80mA RMS



Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI



TV Out

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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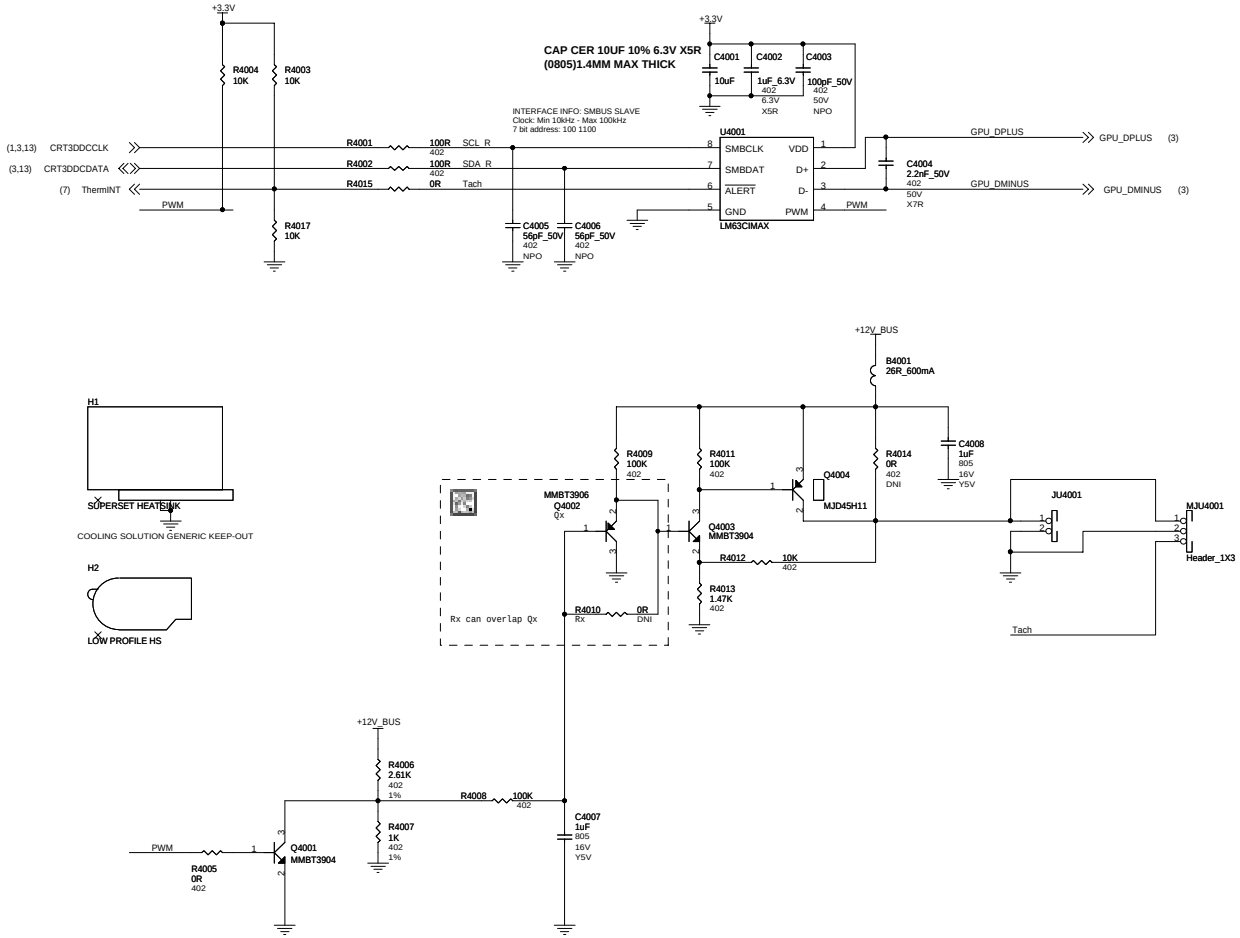
Size C	Document Number 105-A671xx-00	Rev 2
Date: Friday, October 07, 2005	Sheet 16 of 20	



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Size C	Document Number 105-A671xx-00	Rev 2
Date: Friday, October 07, 2005	Sheet 17 of 20	

DVI/VGA SCREWS

ASSY-SCREW1
SCREW
JACKSCREW
ASSY
7020000800

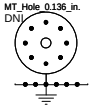
ASSY-SCREW2
SCREW
JACKSCREW
ASSY
7020000800

ASSY-SCREW5
SCREW
PAN_HEAD
7020001700

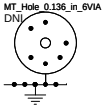
ASSY-SCREW3
SCREW
JACKSCREW
ASSY
7020000800

ASSY-SCREW4
SCREW
JACKSCREW
ASSY
7020000800

MT1
MT_Hole_0.136_in.
DNI

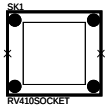


MT2
MT_Hole_0.136_in_6VIA
DNI



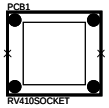
DNI

SK1



RV410SOCKET

PCB1



RV410SOCKET

<Variant Name>

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Title: RV530/RV515 256MB DDR3-136 Dual 2xDVI VIVO FH

Size	Document Number	Rev
C	105-A671xx-00	2

Date: Friday, October 07, 2005 Sheet 18 of 20