

# P2030

GK106, 2GB GDDR5, 192b mixed mode x16, x32  
Stacked DVI-I/DVI-D + HDMI/DP + DP

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1.0 Bason on P2040 modify  
PAGE 2 add 12V FUSE  
PAGE3/4/5/6/7/8/9 modify net name  
PAGE 14 Add ESD component  
PAGE 15 Add ESD componet ,change DVI component  
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PAGE 17 remove co-lay DP circuit,change HDMI component  
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PAGE 21 Add dual VBIOS circuit  
PAGE 22 PEX\_VDD/PEX\_VDD1 LDO change power switch circuit ,add 6262 circuit  
PAGE 23 FBVDDQ chane two phase power circuit  
PAGE 24 Add PEX Input power Level circuit  
PAGE 25/26/27 change nvvdd power 8 pashe power circuit  
PAGE 28 Add PEX2x3 power input circuit  
  
1.1 Bason on 1.0 modify  
PAGE 25 change nvvdd power 8 pashe power circuit

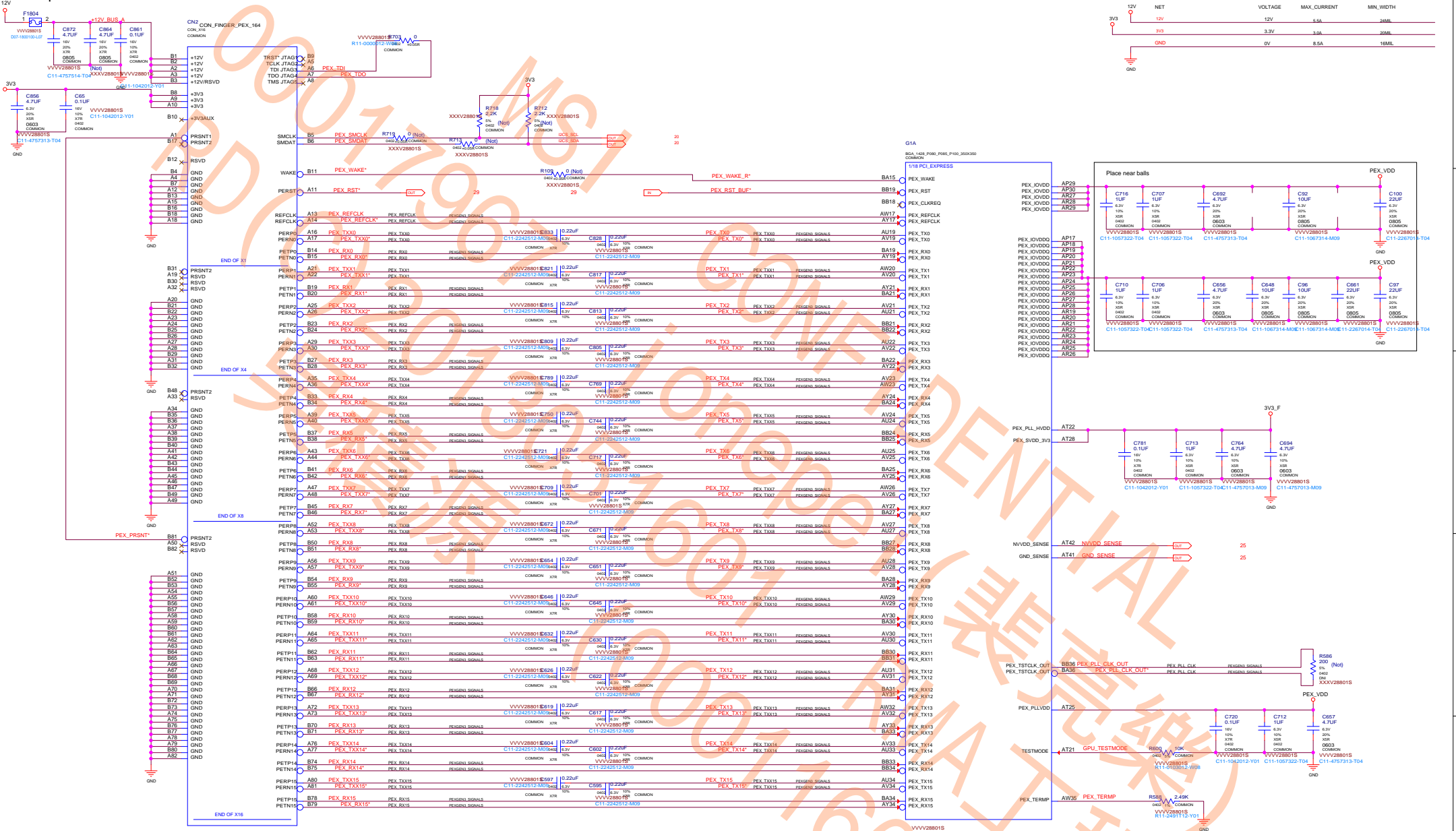
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1	SKU0000	600-12030-0000-000	GK106-400, 2048MB, GDDR5 192b Stacked DVI-I DL/DVI-D DL, HDMI, DP
2	SKU0010	600-12030-0010-000	GK106-250, 2048MB, GDDR5, 192b Stacked DVI-I DL/DVI-D, HDMI, DP
3	SKU0050	600-12030-0050-000	GK106-200, 2048MB, GDDR5, 128b Stacked DVI-I DL/DVI-D, HDMI, DP
4	SKU0060	600-52030-0060-000	GK106-875, 3072MB, GDDR5, 192b DVI-I, DP, DP Workstation
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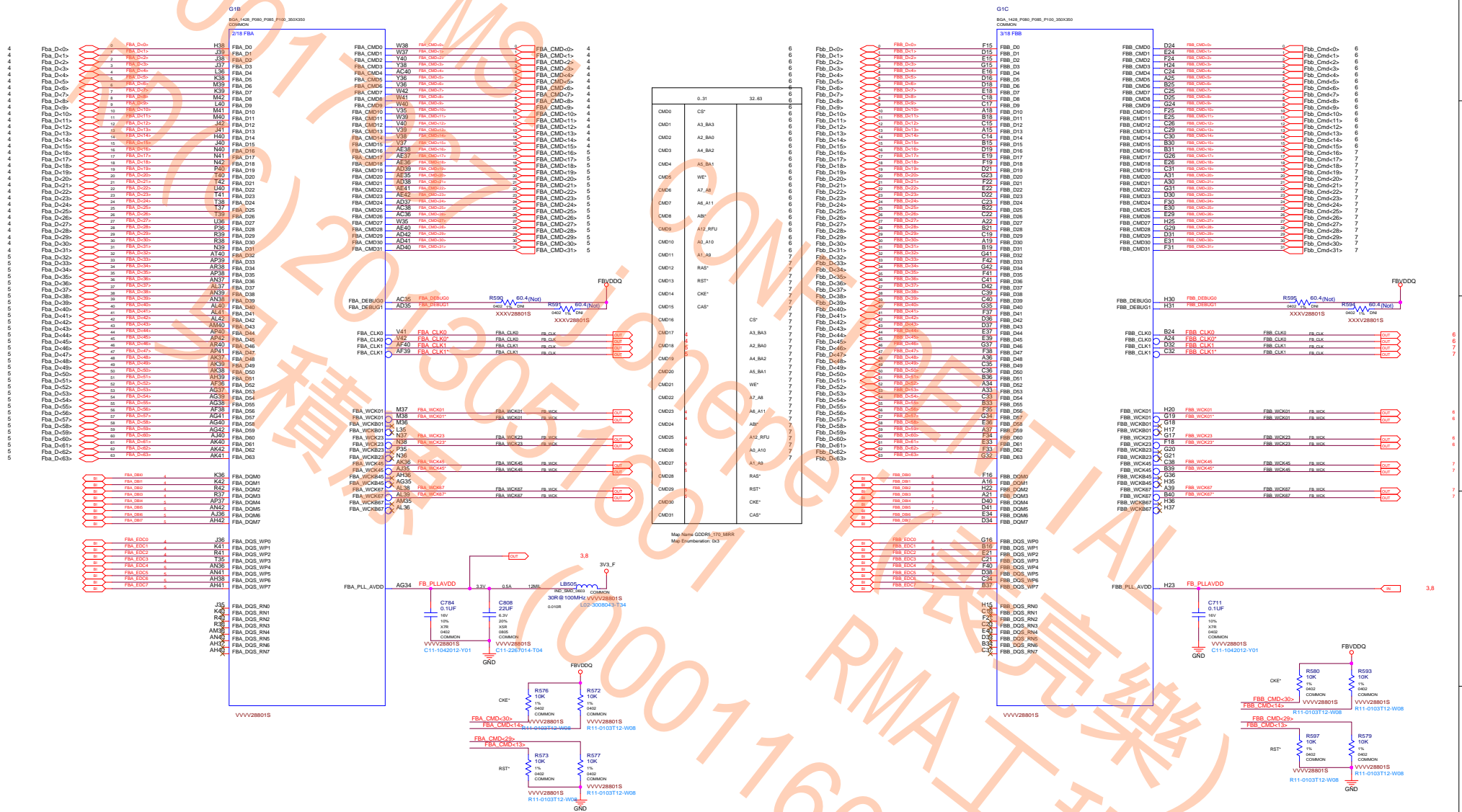
# PCI Express



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MEMORY: GPU Partition A/B



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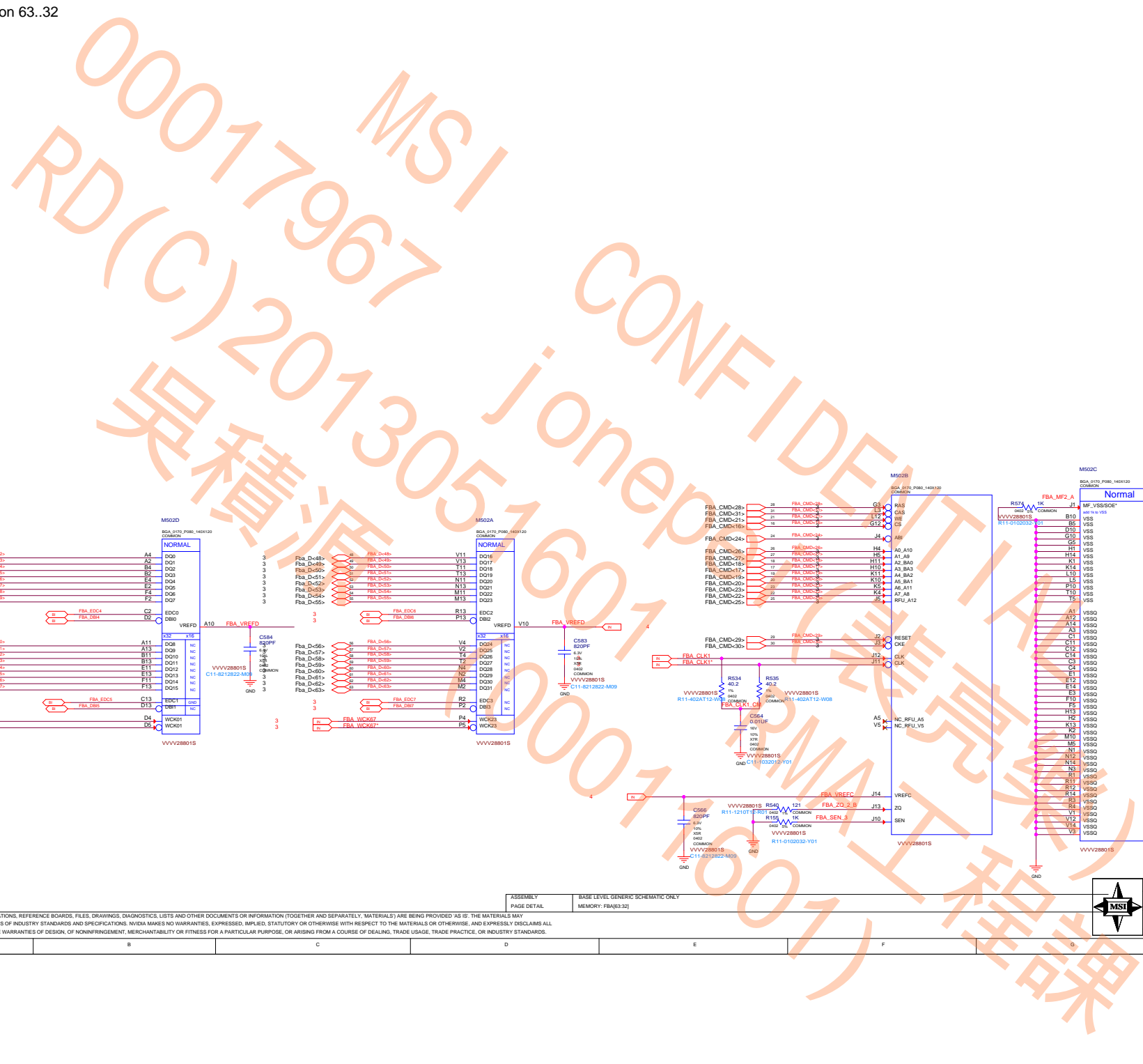
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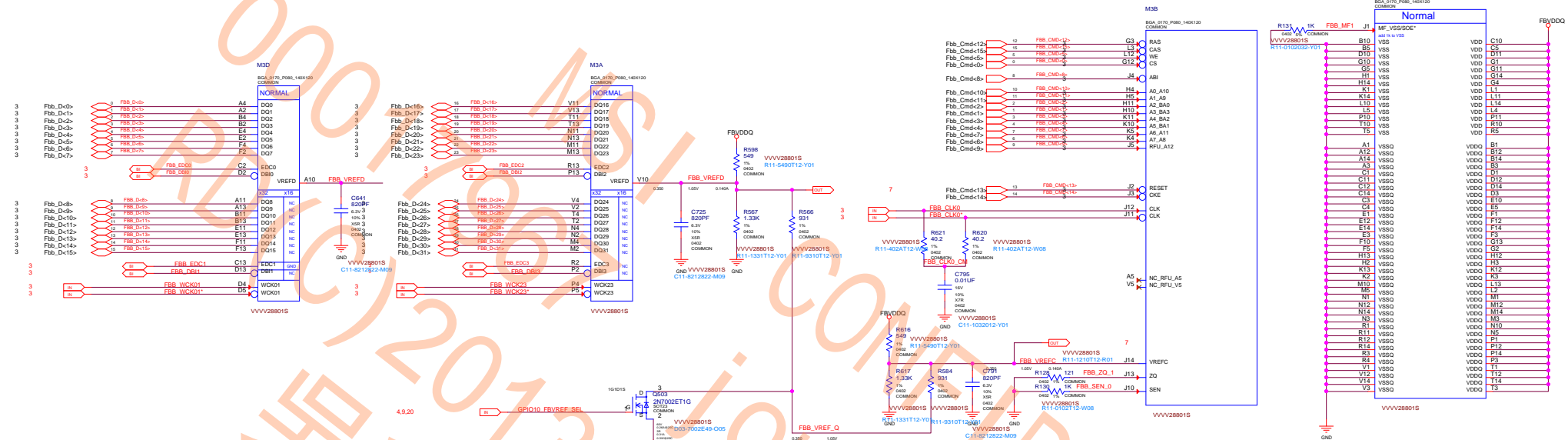
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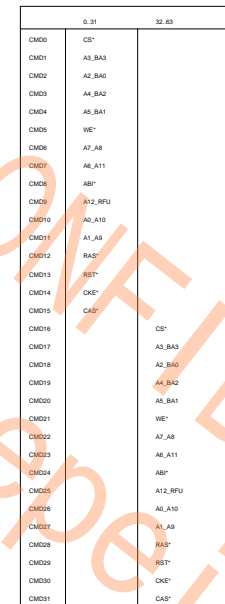
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MEMORY: FBB Partition 31..0



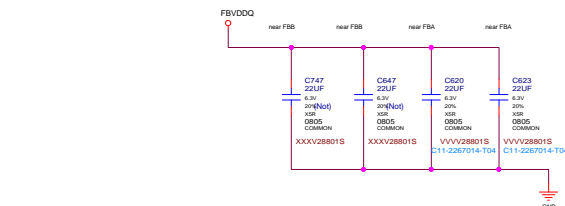
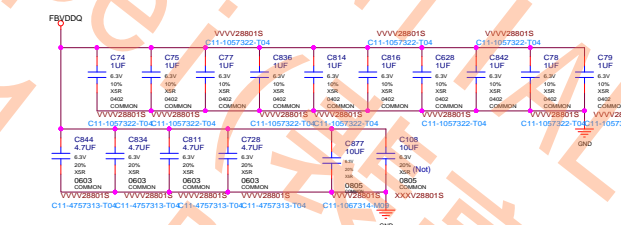
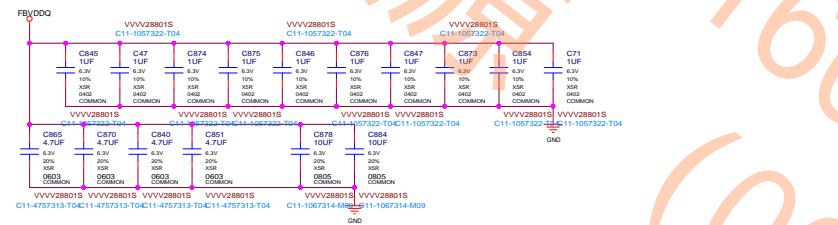
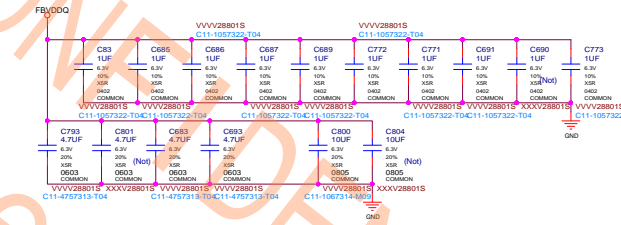
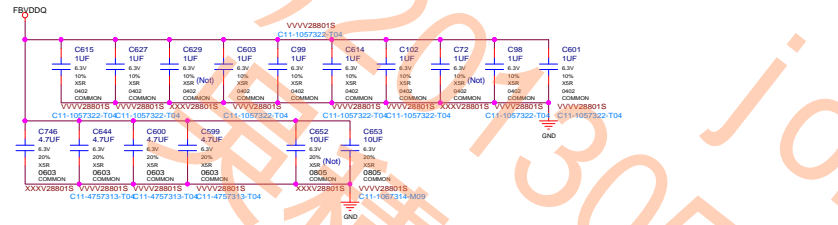
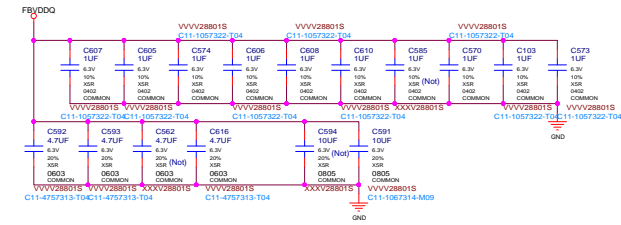
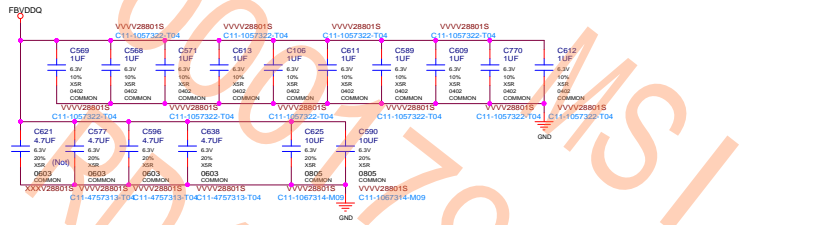












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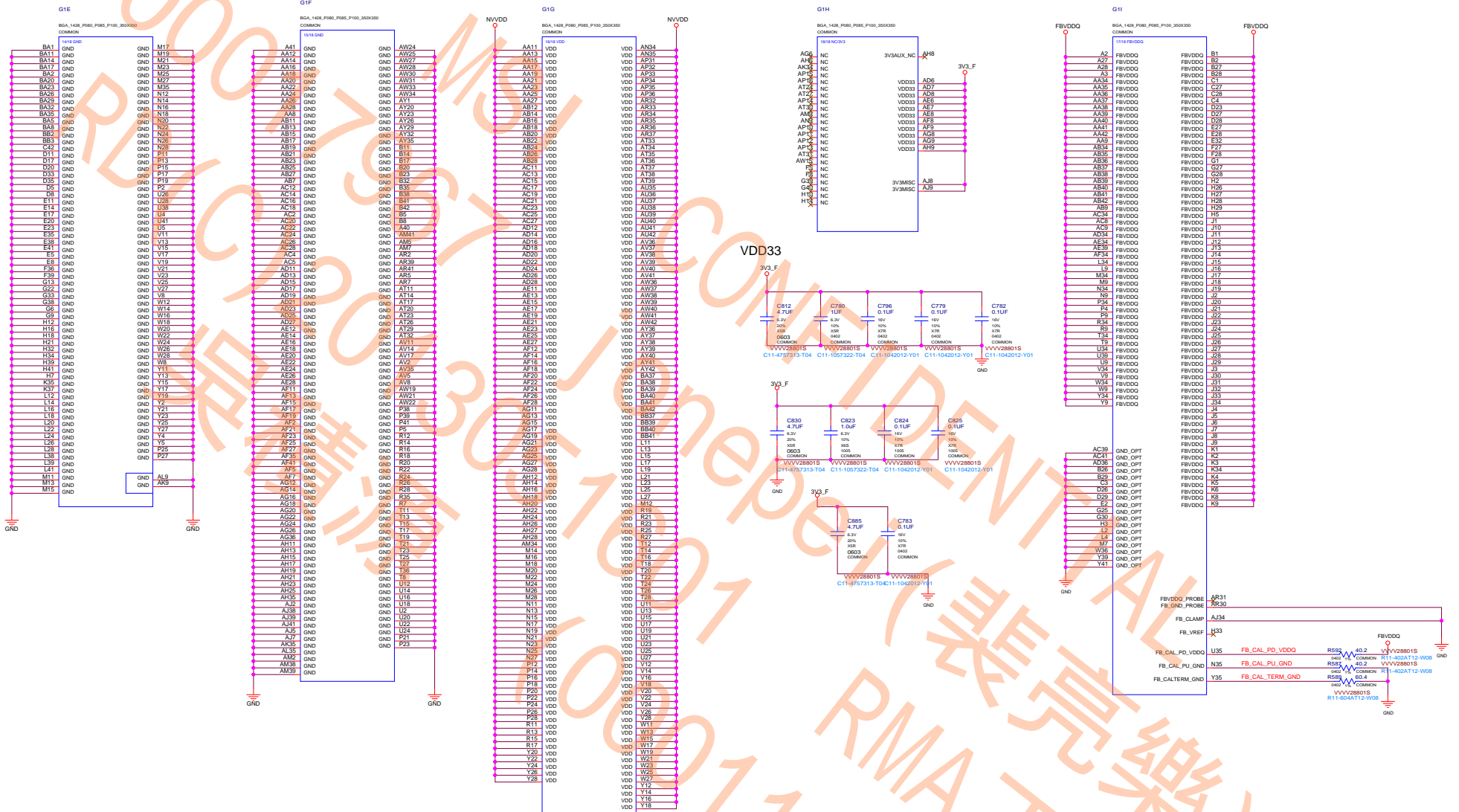
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## GPU PWR and GND



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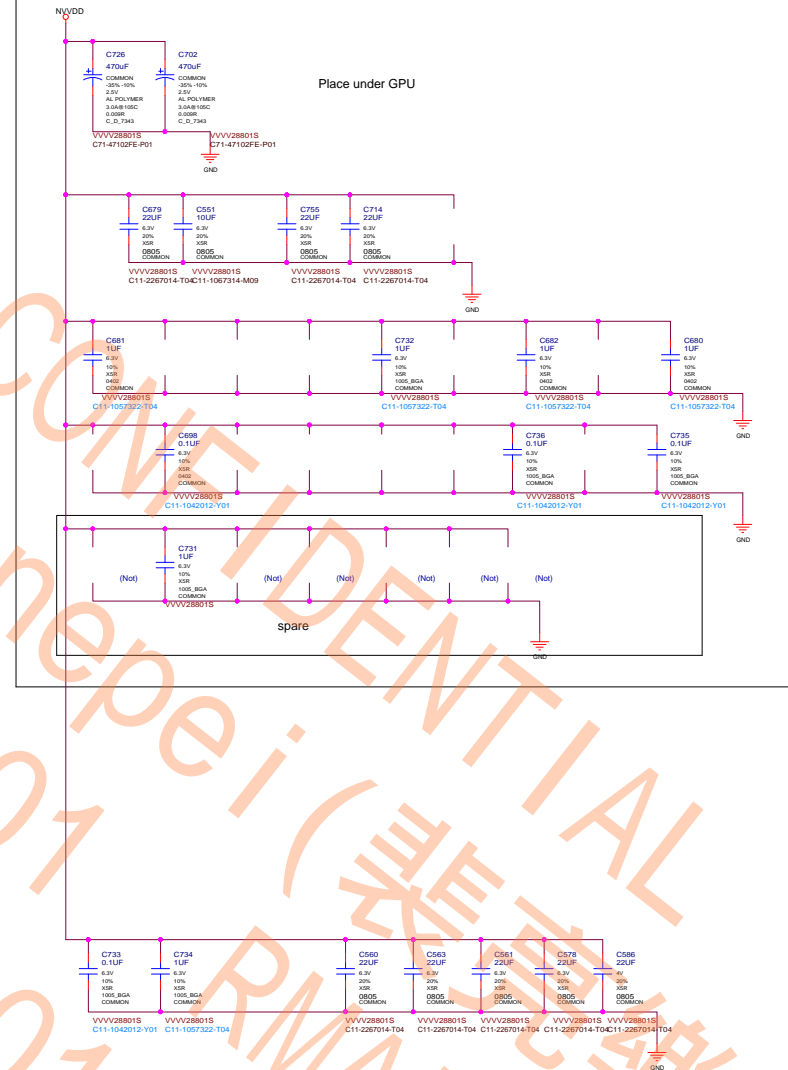
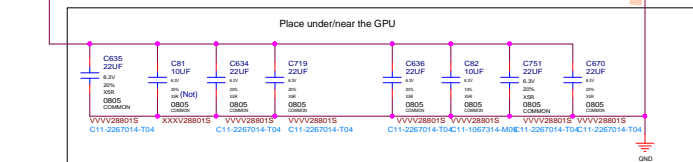
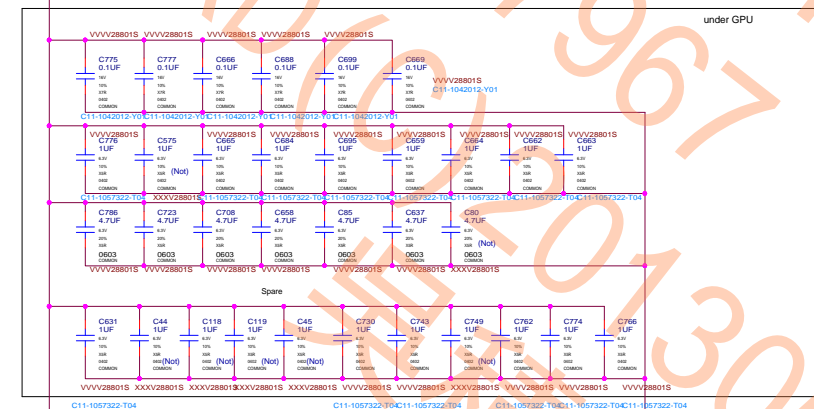
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## GPU Decoupling



	guidelines	actual
Under GPU	2x 330W 3inCh	2x 330W 3inCh
	1x 47U 1200	1x 22U 1200
	2x 22U 805	4x 22U 805
	2x 10U 805	9x 1U 402
	9x 1U 402	9x 0.1U 402
	9x 0.1U 402	
		spare sites (not studied)
		1x 7543
		27x 402
near GPU	1x 47U 1200	2x 22U
	2x 22U 805	
	2x 10U 805	spare sites (not studied)
	2x 4.7U 603	3x 805
	9x 1U 402	
	1x 0.1U 402	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU Decoupling



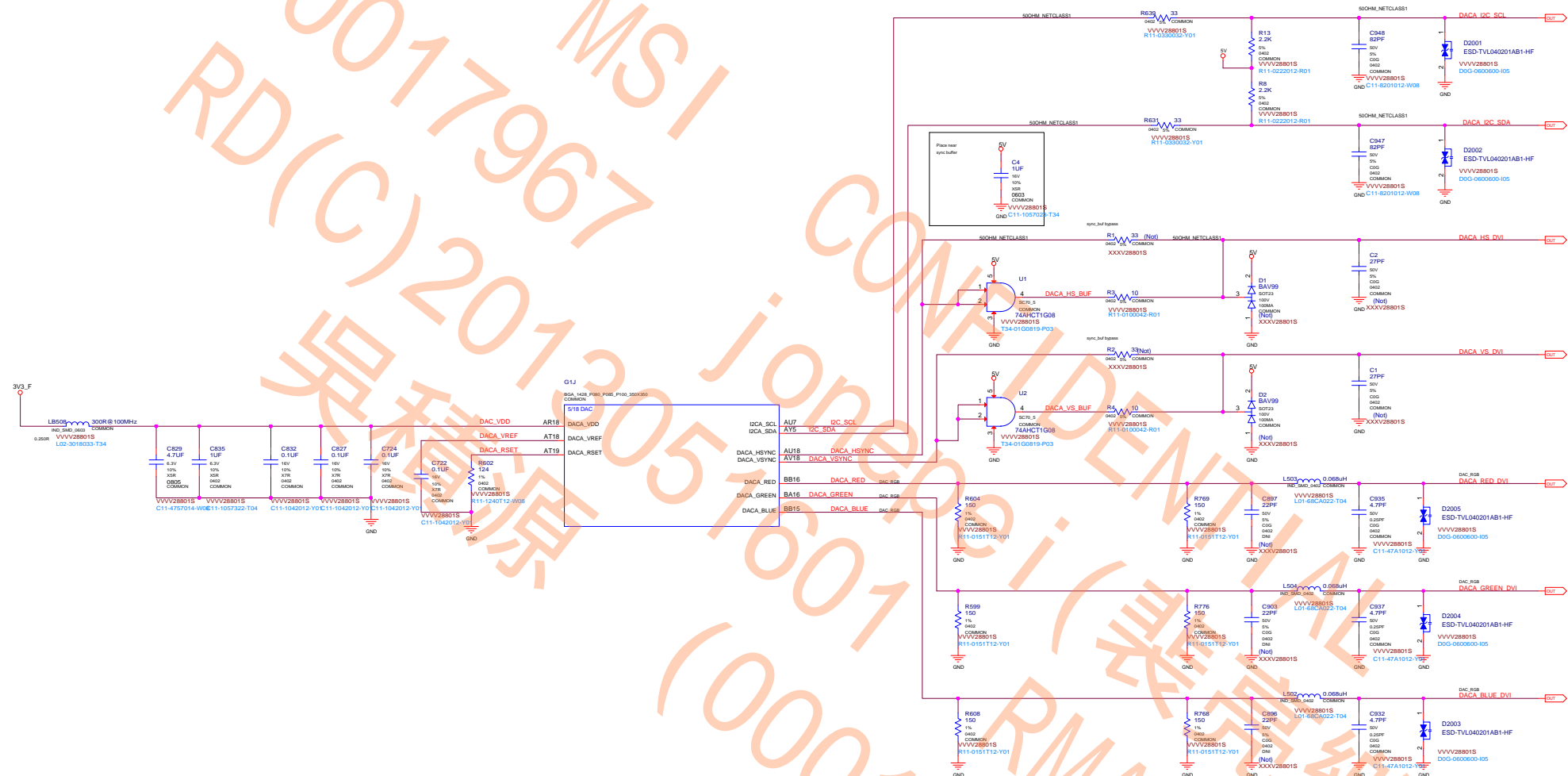
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## DACA Interface



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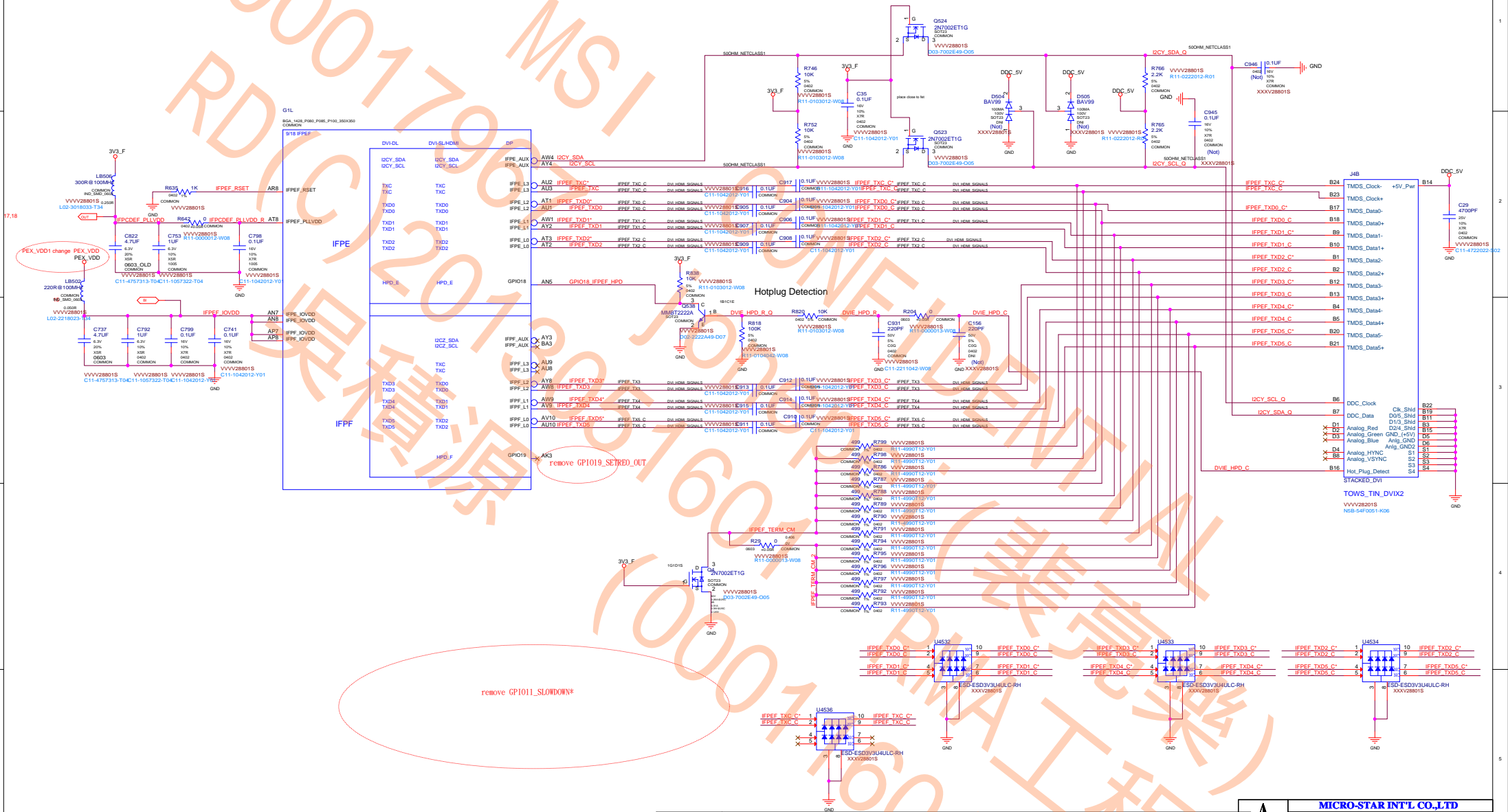
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## IFPEF DVI-D-DL



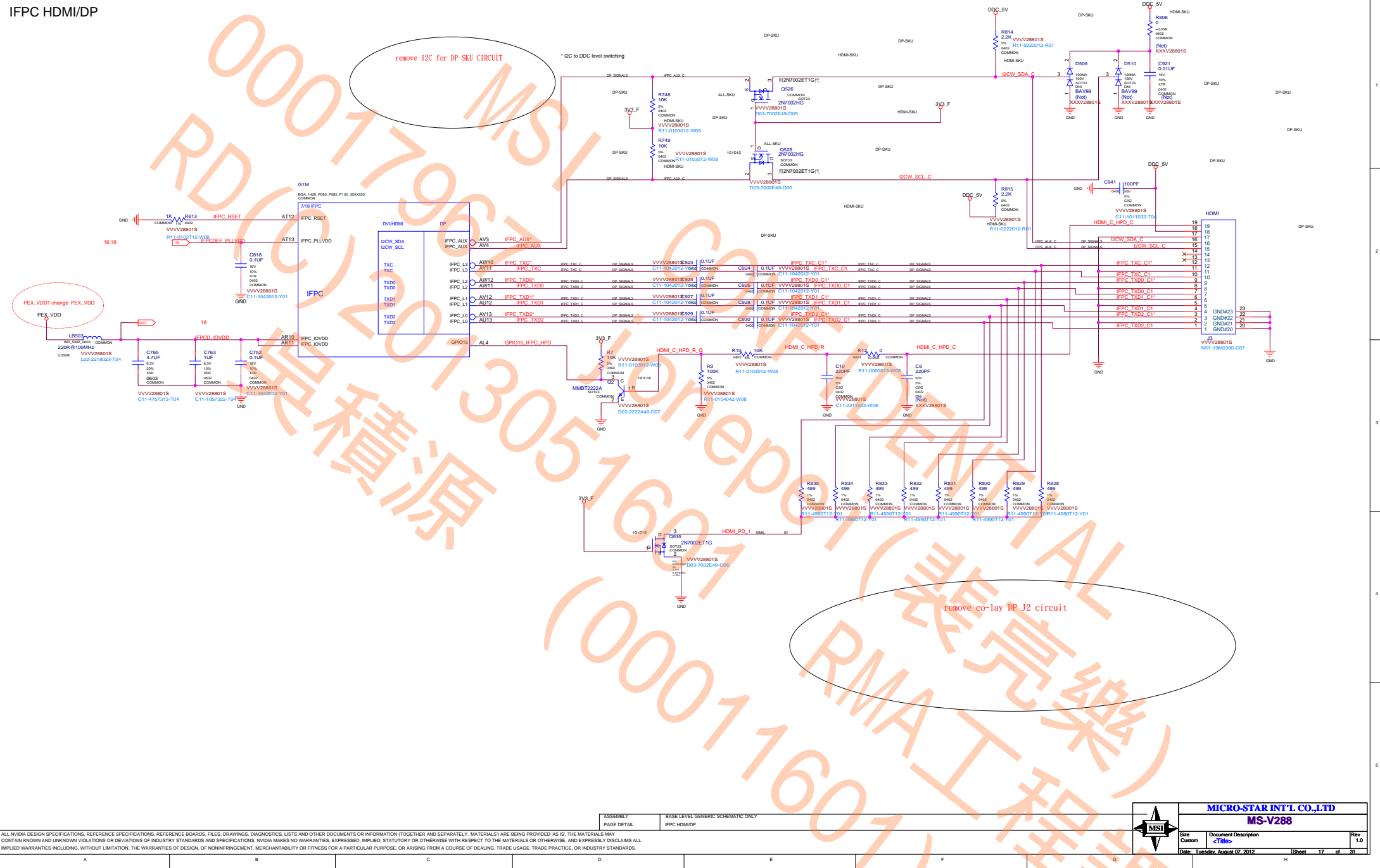
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PAGE DETAIL	IFPEF DVI-D-DL



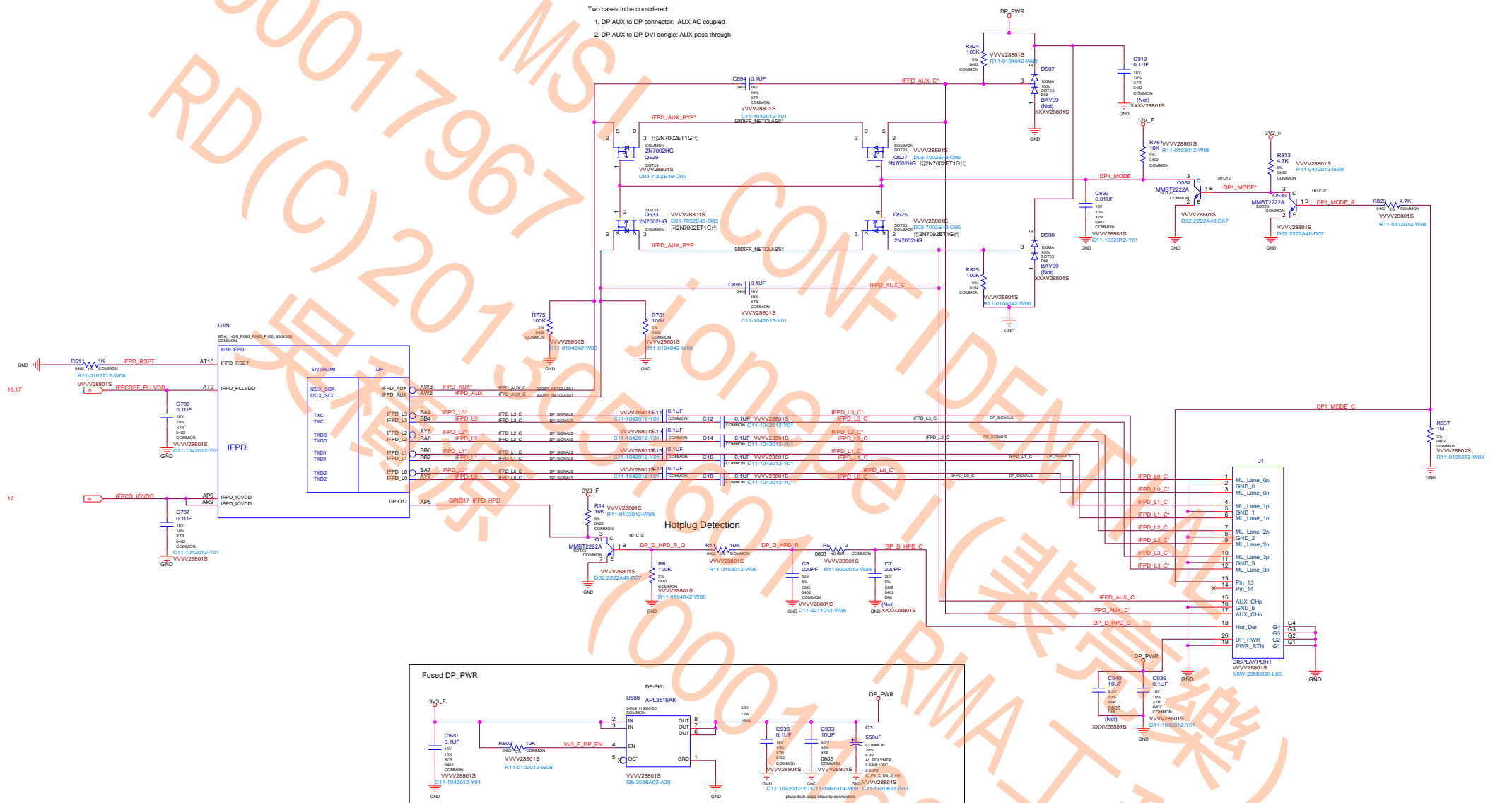
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1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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PAGE DETAIL	IFPD DP



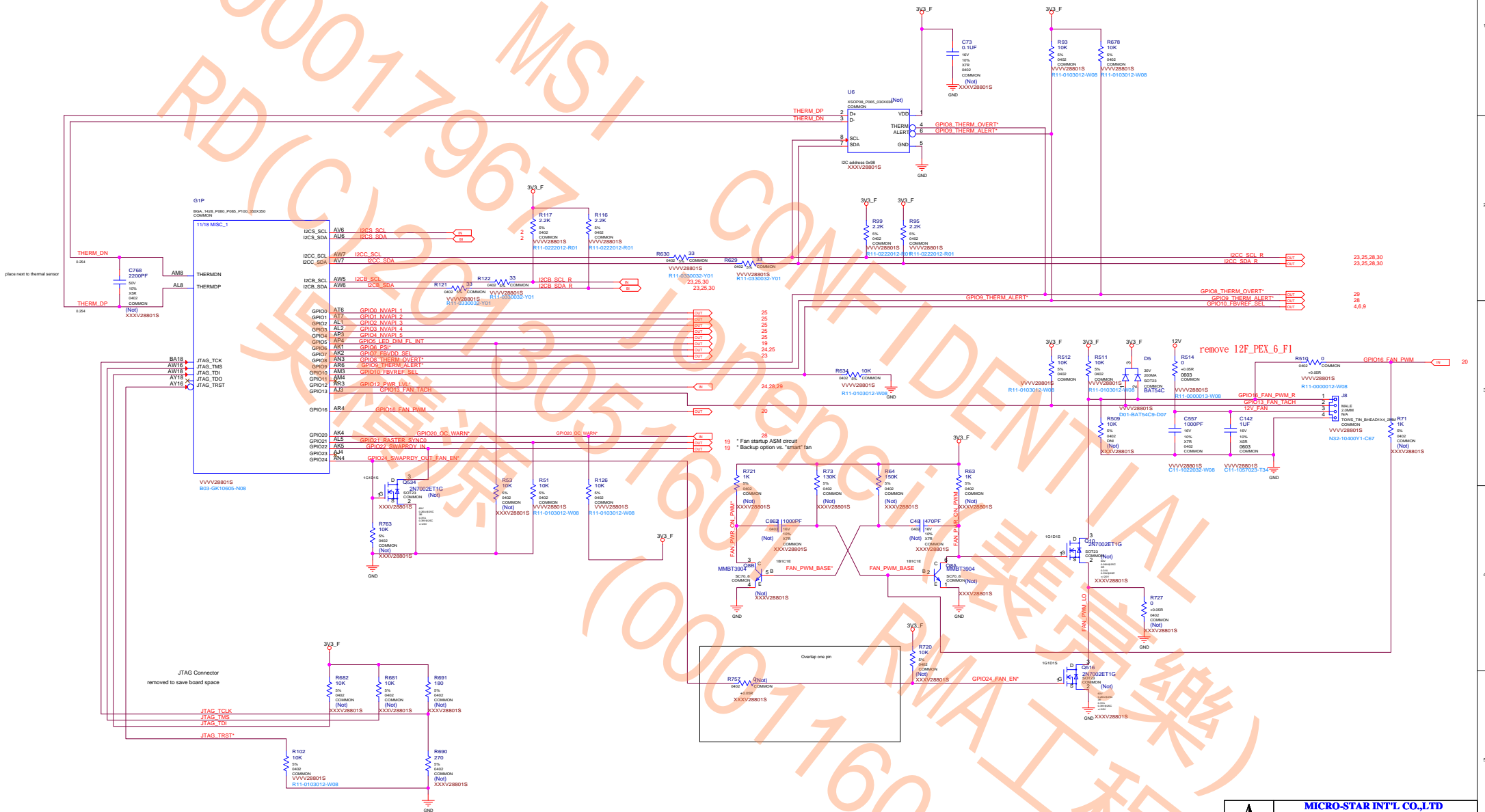
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MISC1: Fan, Thermal, JTAG, GPIO



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PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO

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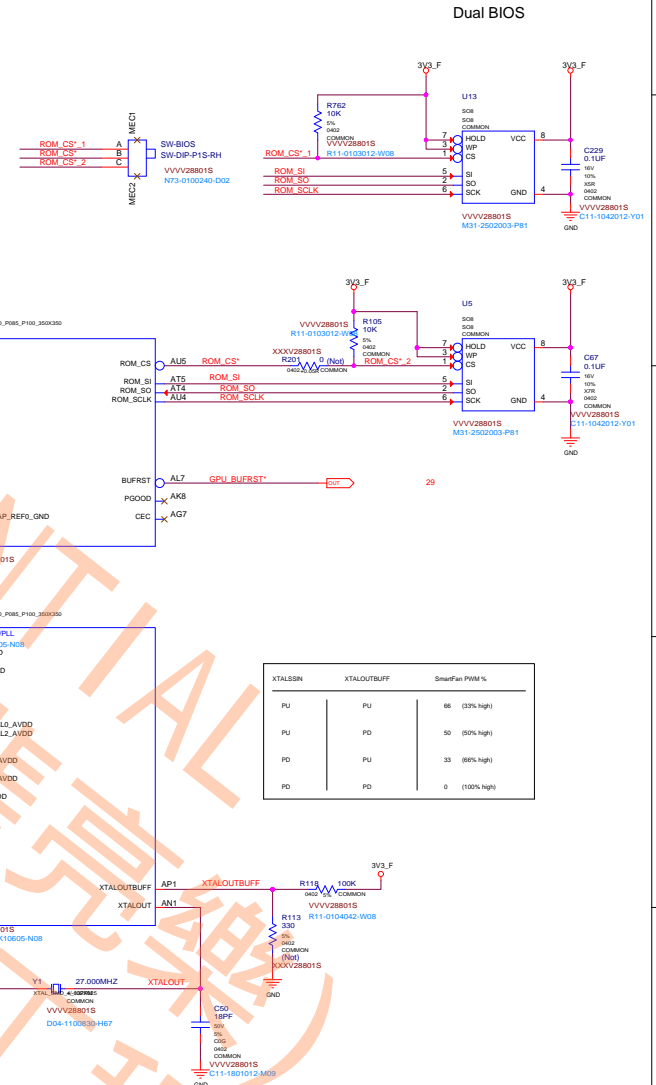
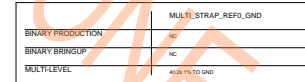
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### MISC2: ROM, XTAL, Straps

STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GPIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0000 - (0x11C0)* 0010 - (0x11C1)* 0050 - (0x11C4)* 0500 - (0x11FA)*	5K PD -400 GPU* 10K PD -250 GPU* 25K PD -225 GPU* 15K PU -875 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	*		
	PEX_SPD_CHANGE_GEN3*	1*      ENABLED*	
	PEX_MAX_SPEED*	1*      FOR GEN2/3*	45K PD*
	DP_PLL_VDD_33V*	1*      FOR 3_3V*	
	RAMCFG[3]*	0*	
	RAMCFG[2]*	1*	35K PD* 45K PD* Hybris Samsung
ROM_SI	RAMCFG[1]*	1*	
	RAMCFG[0]*	0*	
	FB[1].APERTURE_SIZE*	0*      For 128MB*	
ROM_SO	FB[0].APERTURE_SIZE*	1*      For 128MB*	30k PD*
	SMB_ALT_ADDR*	0*	
	VGA_DEVICE*	1*	
	PCI_DEVID_EXT[4]*	0*      For 0x11C0*	25K PD* 25K PD* 25K PD* 35K PU*
	SUB_VENDOR*	1*      Dedicated BIOS*	8x16: 11C0 8x16: 11C1 8x16: 11C4 8x16: 11FA
ROM_SCLK	PCI_DEVID_EXT[5]*	0*      For 0x11C0*	
	PEX_PLL_EN_TERM100*	0*      ENABLED*	

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111



XTALSSIN	XTALOUTBUFF	SmartFan PWM %
PU	PU	66 (33% high)
PU	PD	50 (50% high)
PD	PU	33 (66% high)
PD	PD	0 (100% high)

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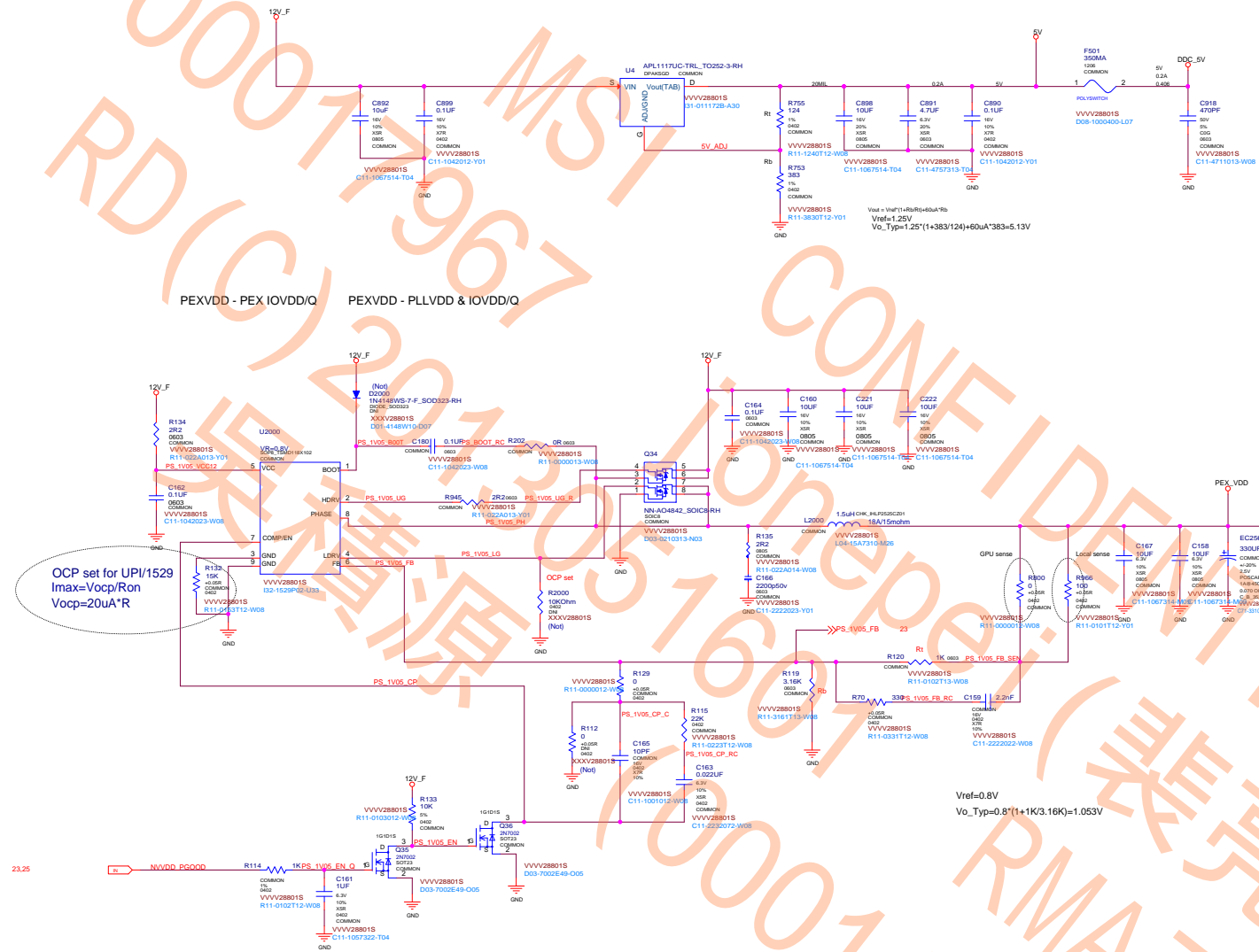
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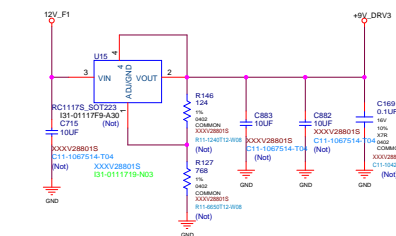
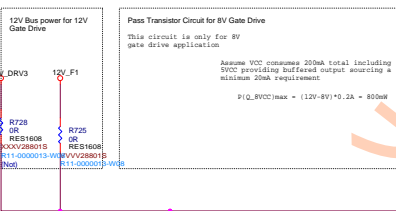
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0	1.38V
1	1.50V

$V_{out} = V_{ref} * (1 + R_{top} / (R_{bot} \parallel R_{bot1}))$   
 $V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$   
 $V_{out} = V_{ref} * (1 + R_{top} / (R_{bot} \parallel R_{bot1}))$

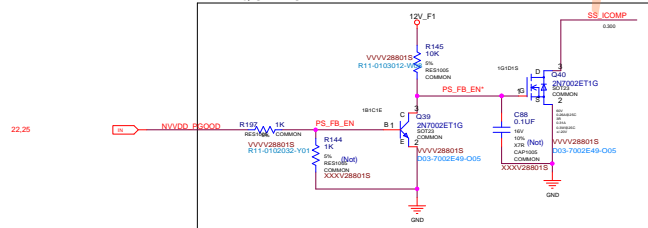
## Choosing Different Gate Drive

Gate Drive	Populate	Do Not Populate
5V Gate Drive	B631, B632	B630, B670, C660, B651, Q661
8V Gate Drive	B630, C660, B651, Q661	B631, B632, B670
12V Gate Drive	B630, C660, B670	B631, B632, B651, Q661

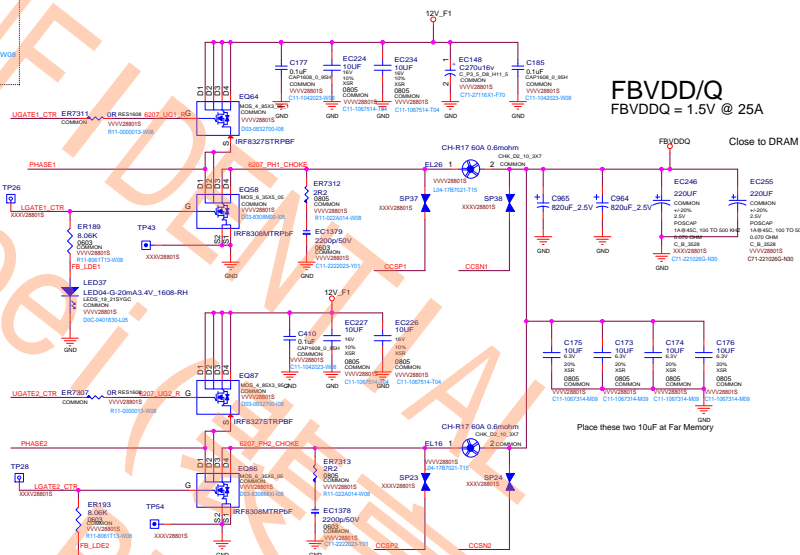
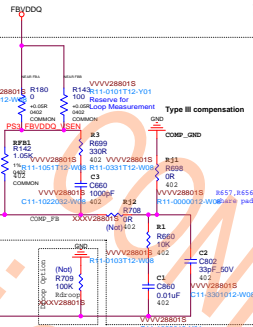
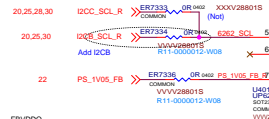


$$V_{out} = 1.25V * [1 + (R_{127} / R_{146})]$$

## FBVDDQ GATING



## SMBUS ADDRESS 0X60



FBVDDQ/Q  
 FBVDDQ = 1.5V @ 25A

Close to DRAM

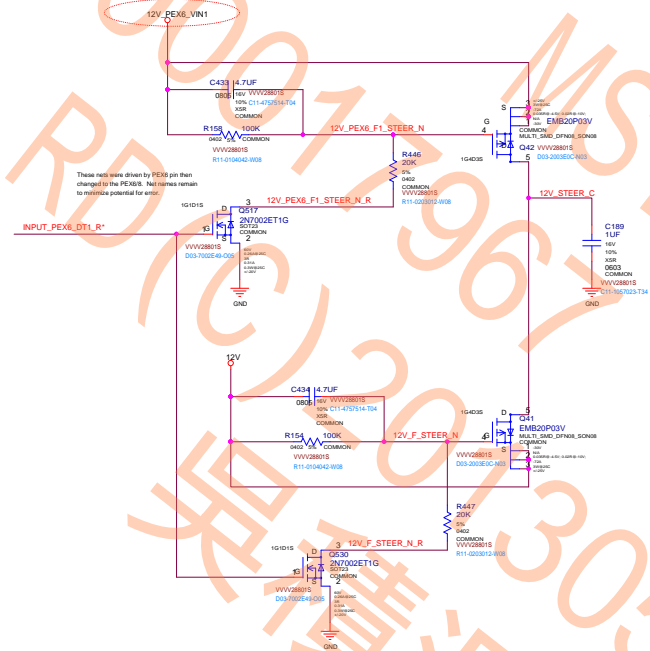
Place these two 10uF at Far Memory



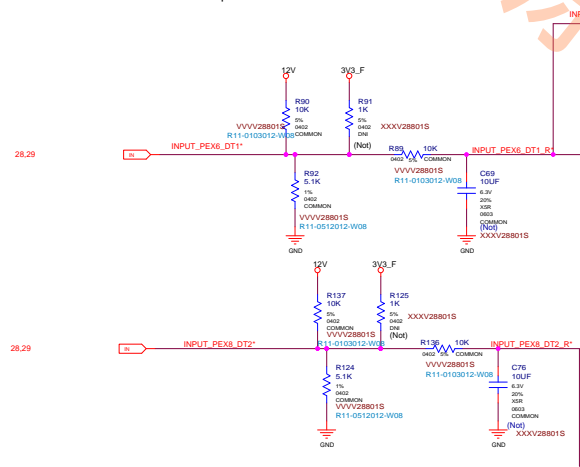
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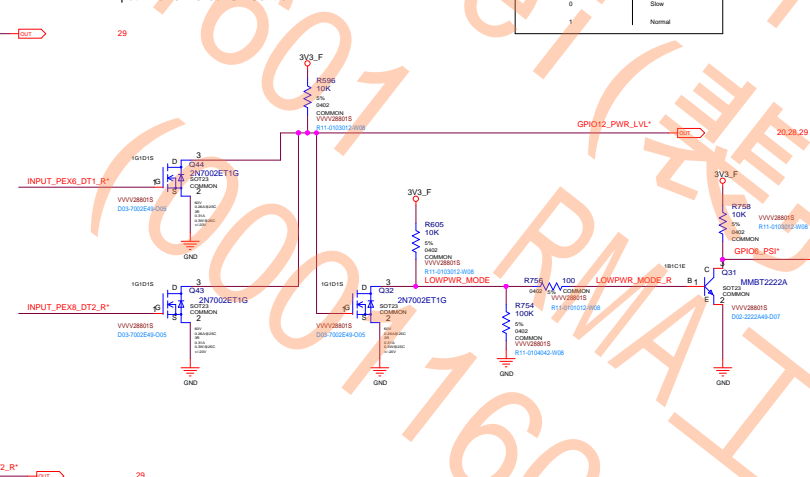
## PS: NVVDD Controller, VID and PSI



PEX Input - Power Level/PSI\* Control



PEX Input - Power Level/PSI\* Control



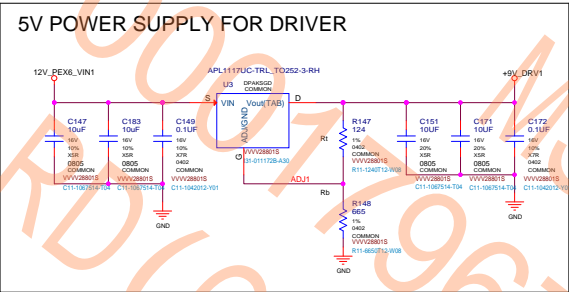
GPIO12_PWR_LVL	GPU SPEED
0	Slow
1	Normal

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVDD VID and PSI

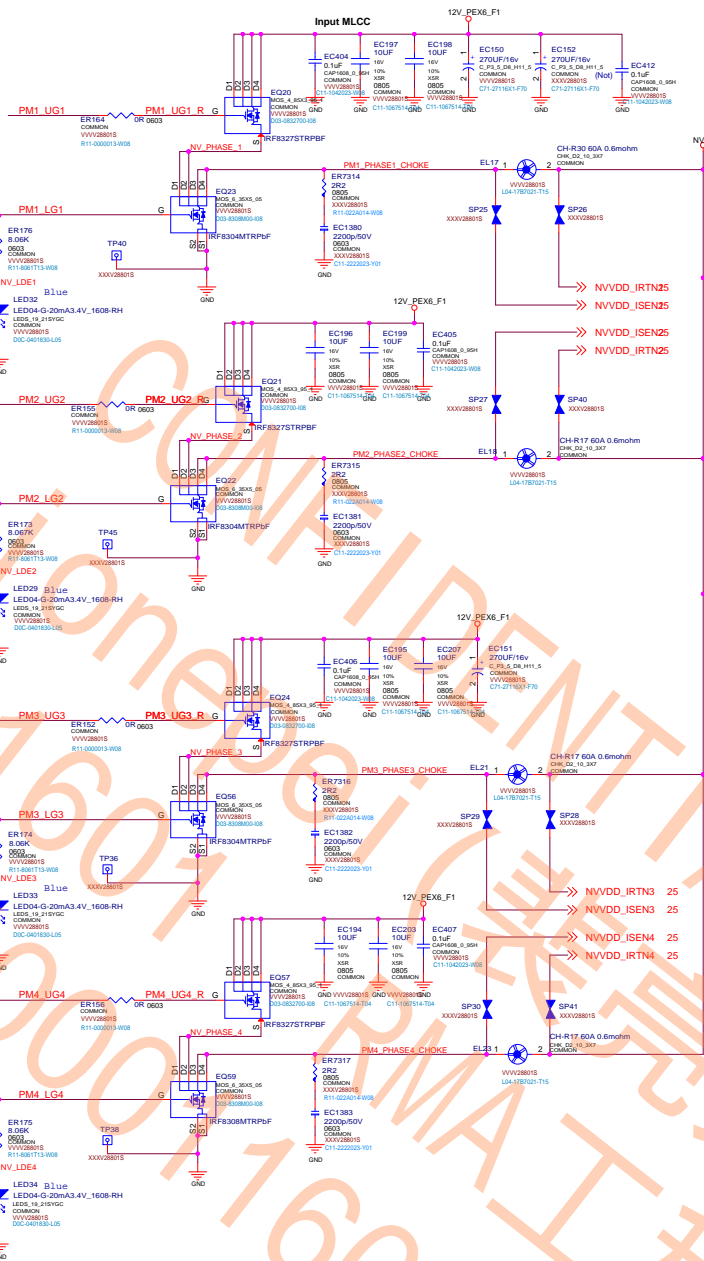
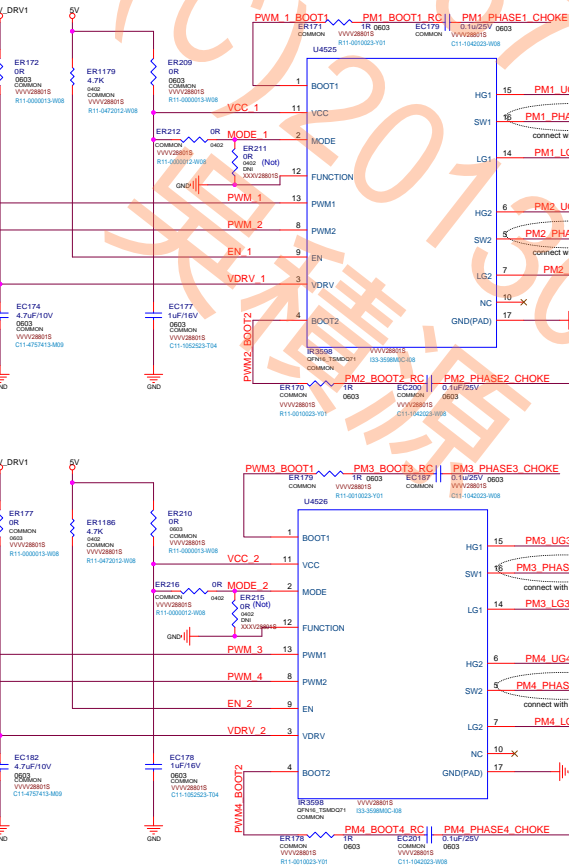
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Function	Mode	PWM Mode	Phase Mode
0	1	IR ATL	Dual
1	1	IR ATL	Double
0	0	tri-state	Dual
1	0	tri-state	Double



Output Bulk CAPs

Output Bulk CAPs



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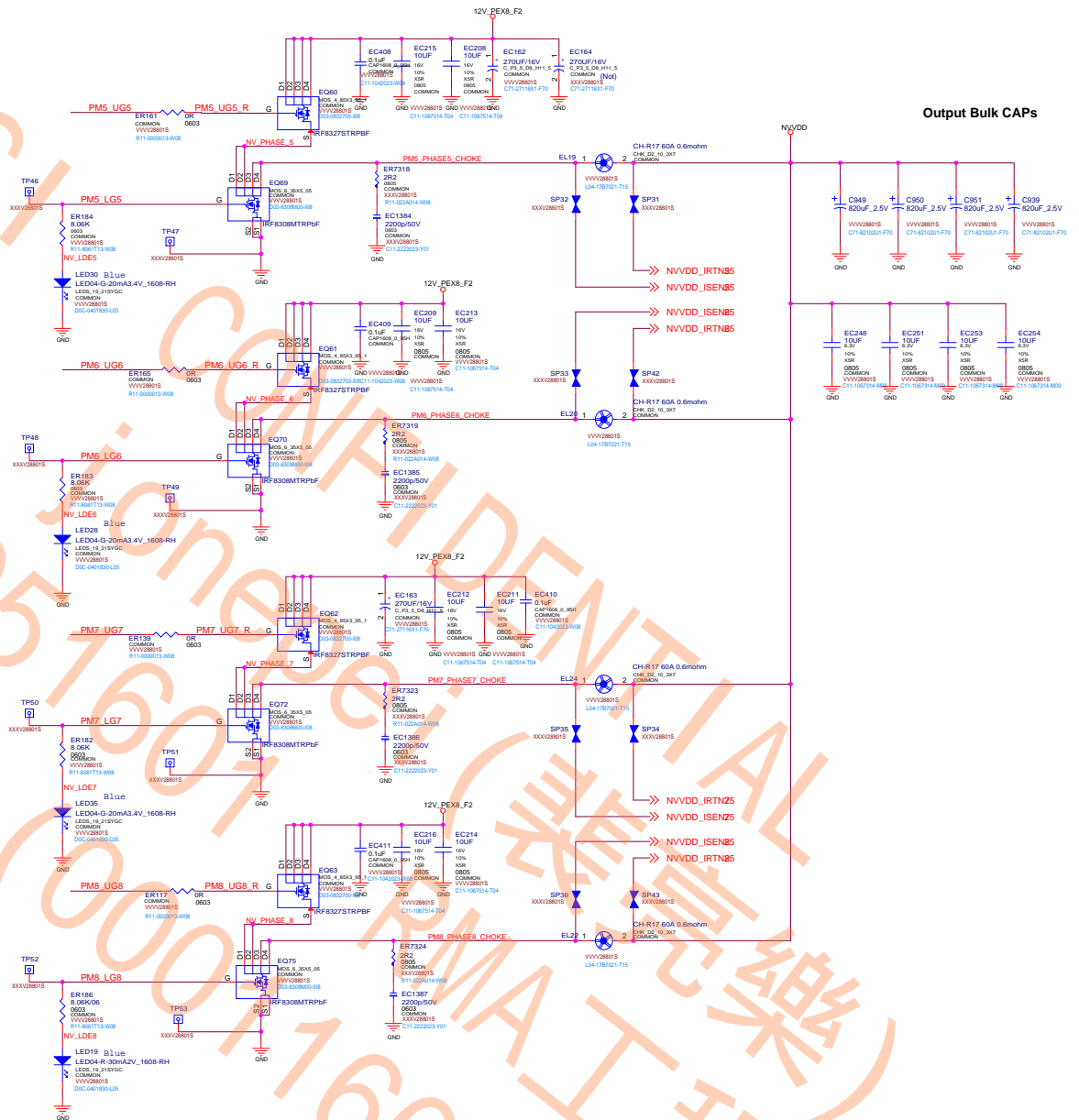
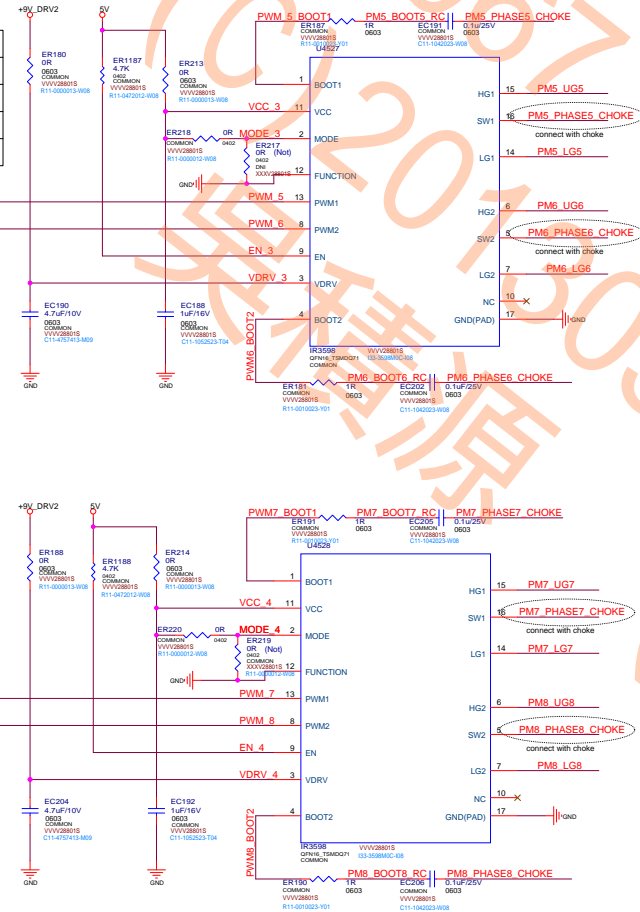
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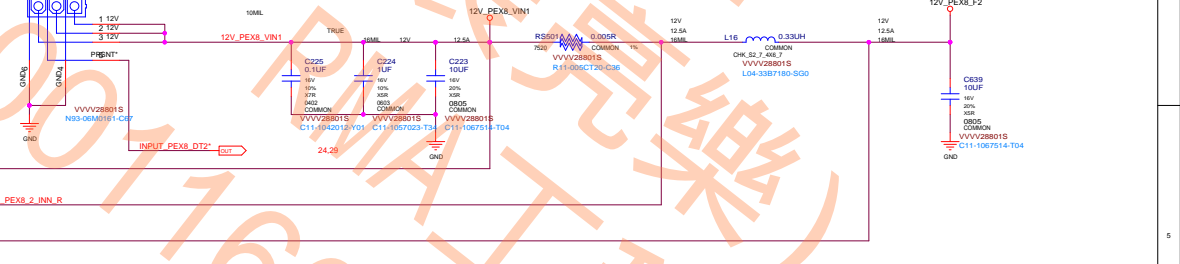
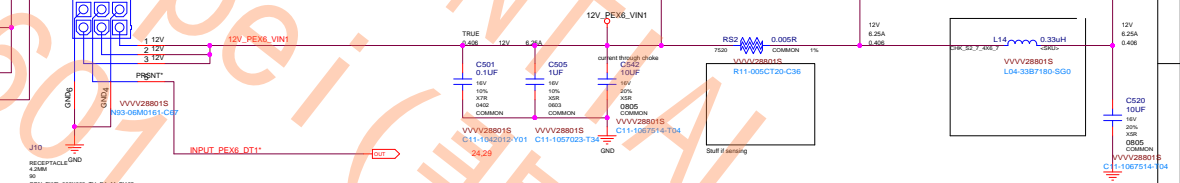
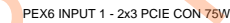
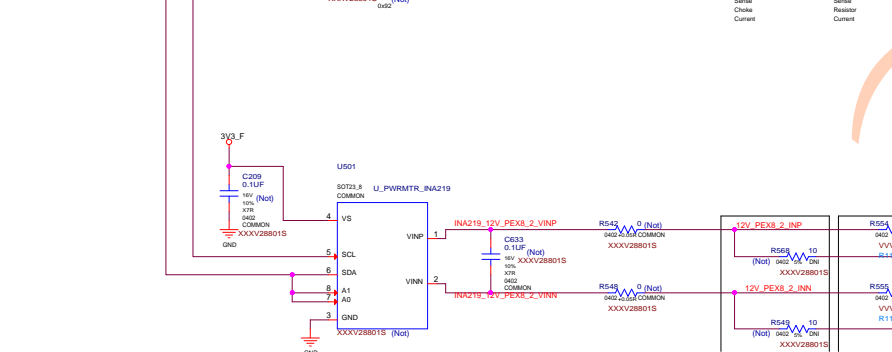
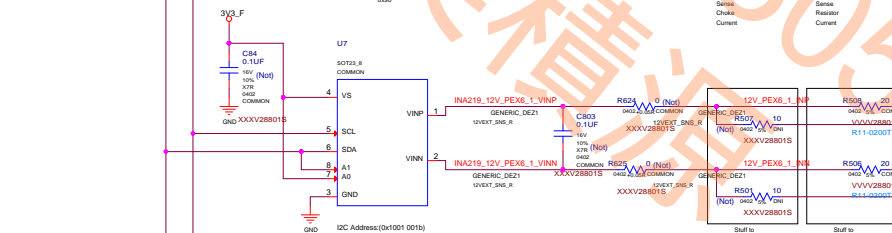
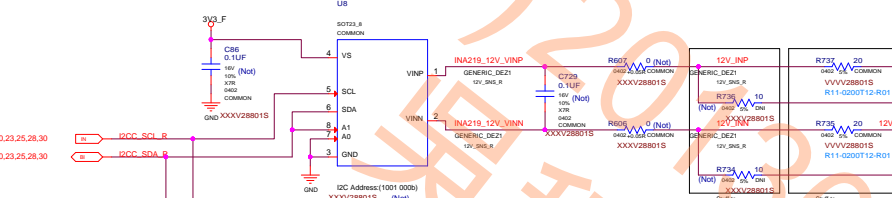
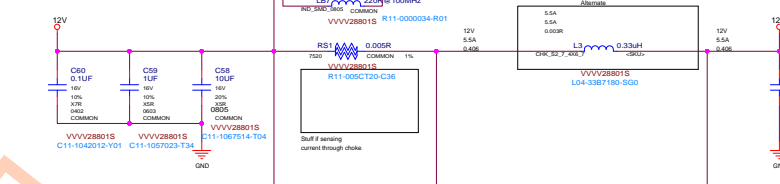
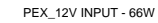
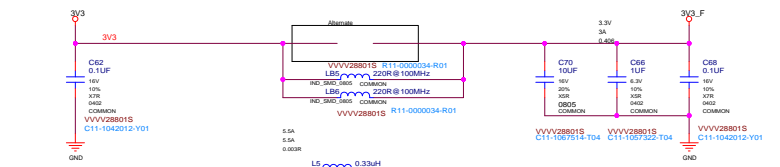
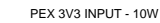
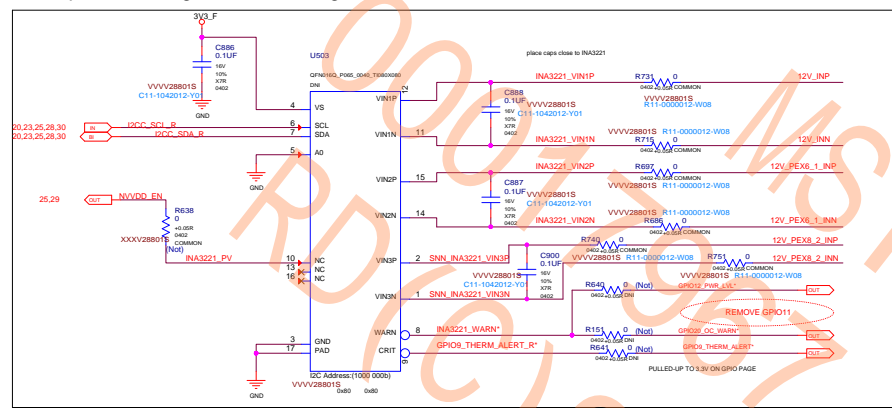


[illegible]

Function	Mode	PWM Mode	Phase Mode
0	1	IR ATL	Dual
1	1	IR ATL	Doublet
0	0	tri-state	Dual
1	0	tri-state	Doublet



## PS: Inputs, Filtering, and Monitoring



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring



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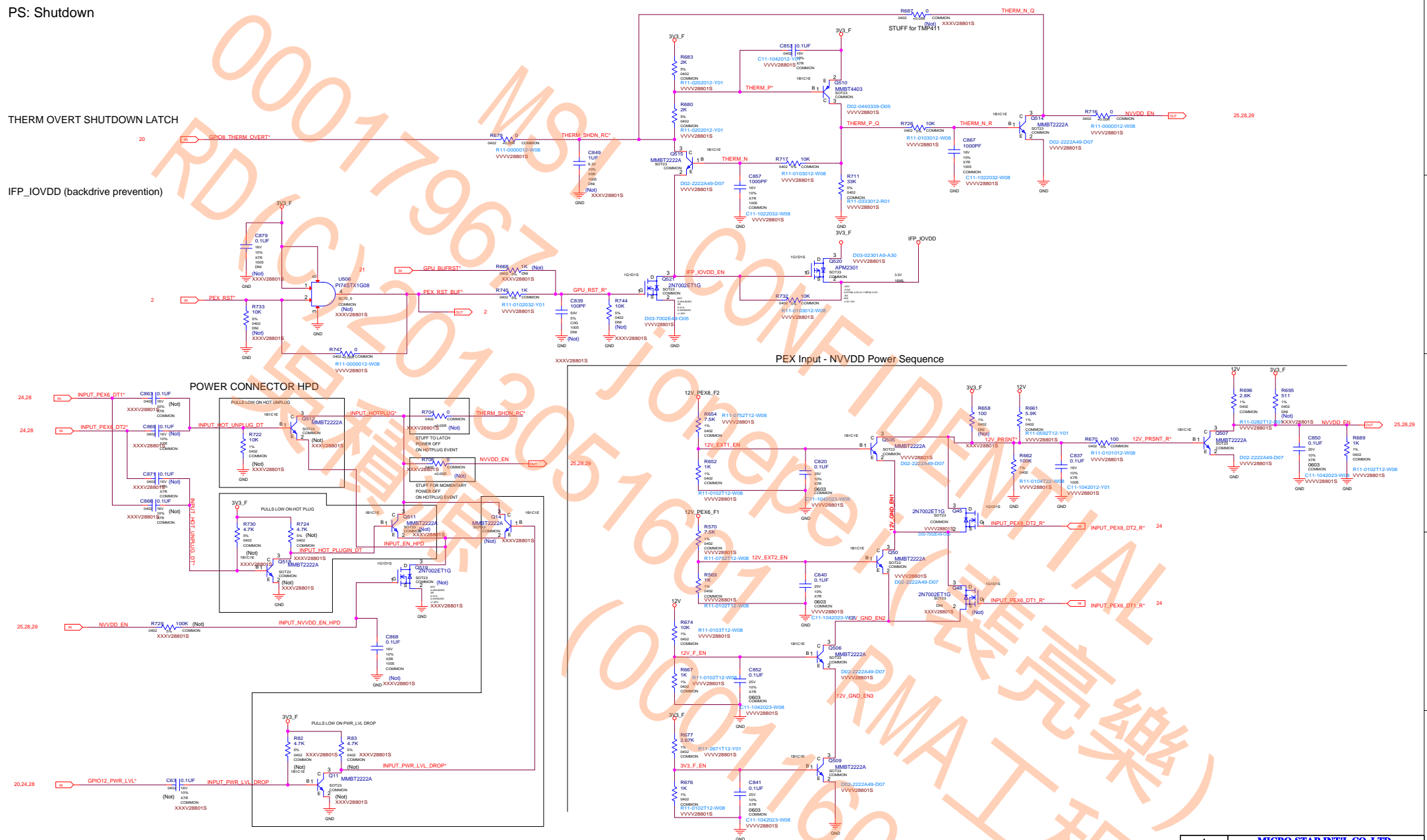
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PS: Shutdown

### THERM OVERT SHUTDOWN LATCH

IFP\_IOVDD (backdrive prevention)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Shutdown

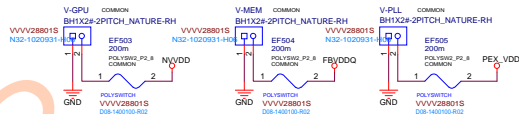
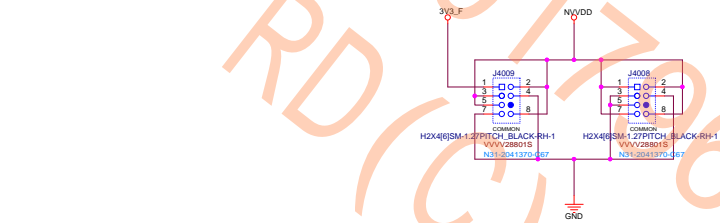


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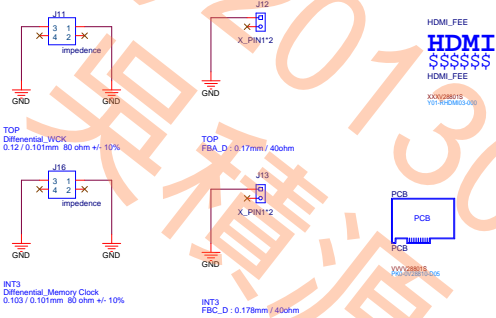
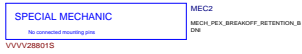
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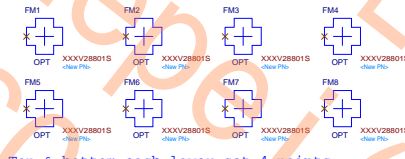
Hockey Stick



HDMI\_FEE  
HDMI\_FEE  
XXXXV28801S  
TOP 80OHMS/50%

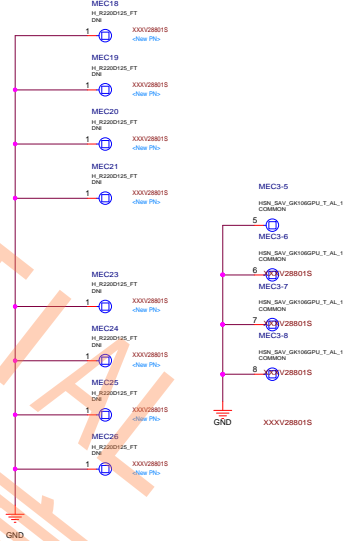


optical cross point



Top & bottom each layer set 4 points

Mechanical Holes Symbol



Bracket:



Bracket Screw



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