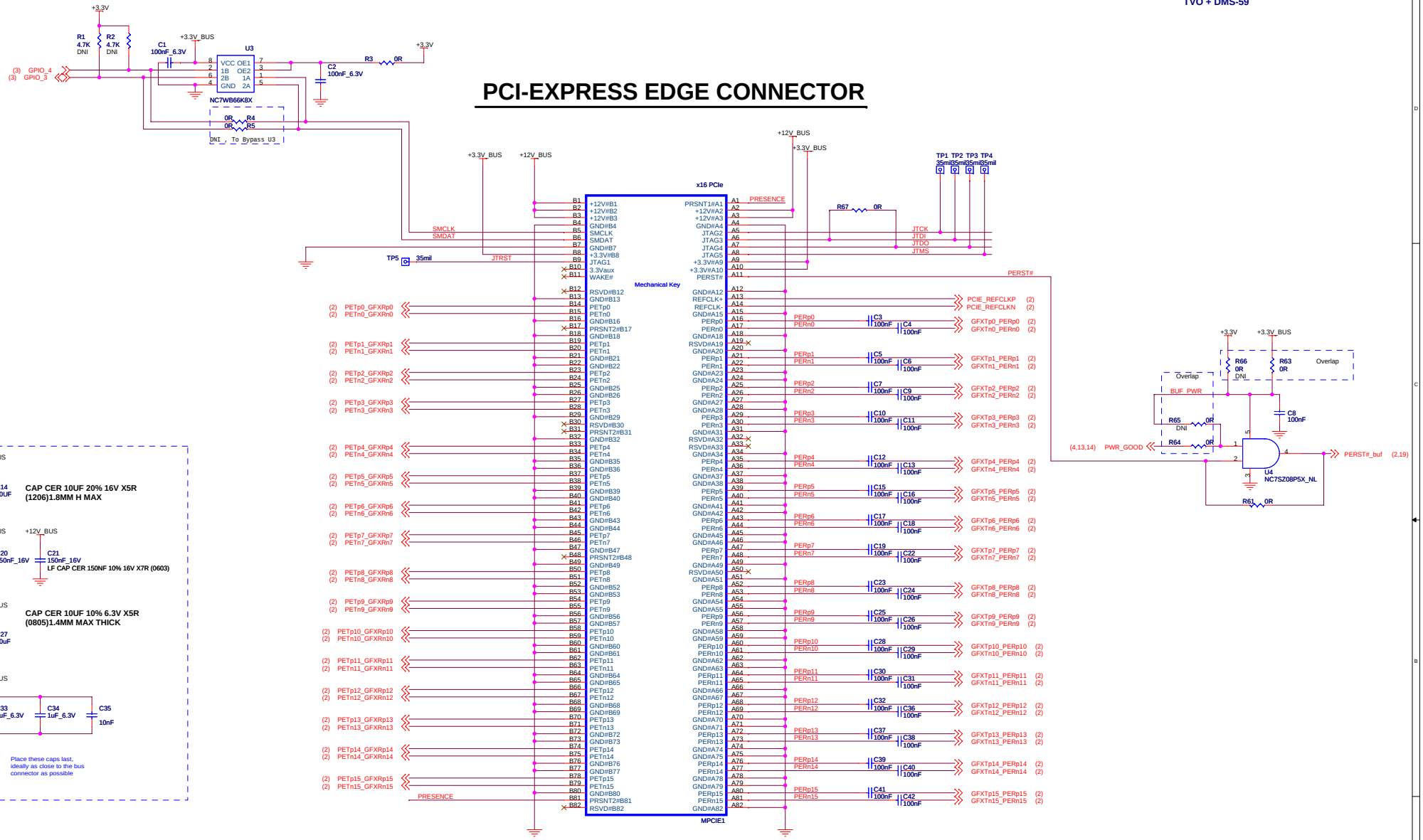
RV710

TVO + DMS-59

PCI-EXPRESS EDGE CONNECTOR



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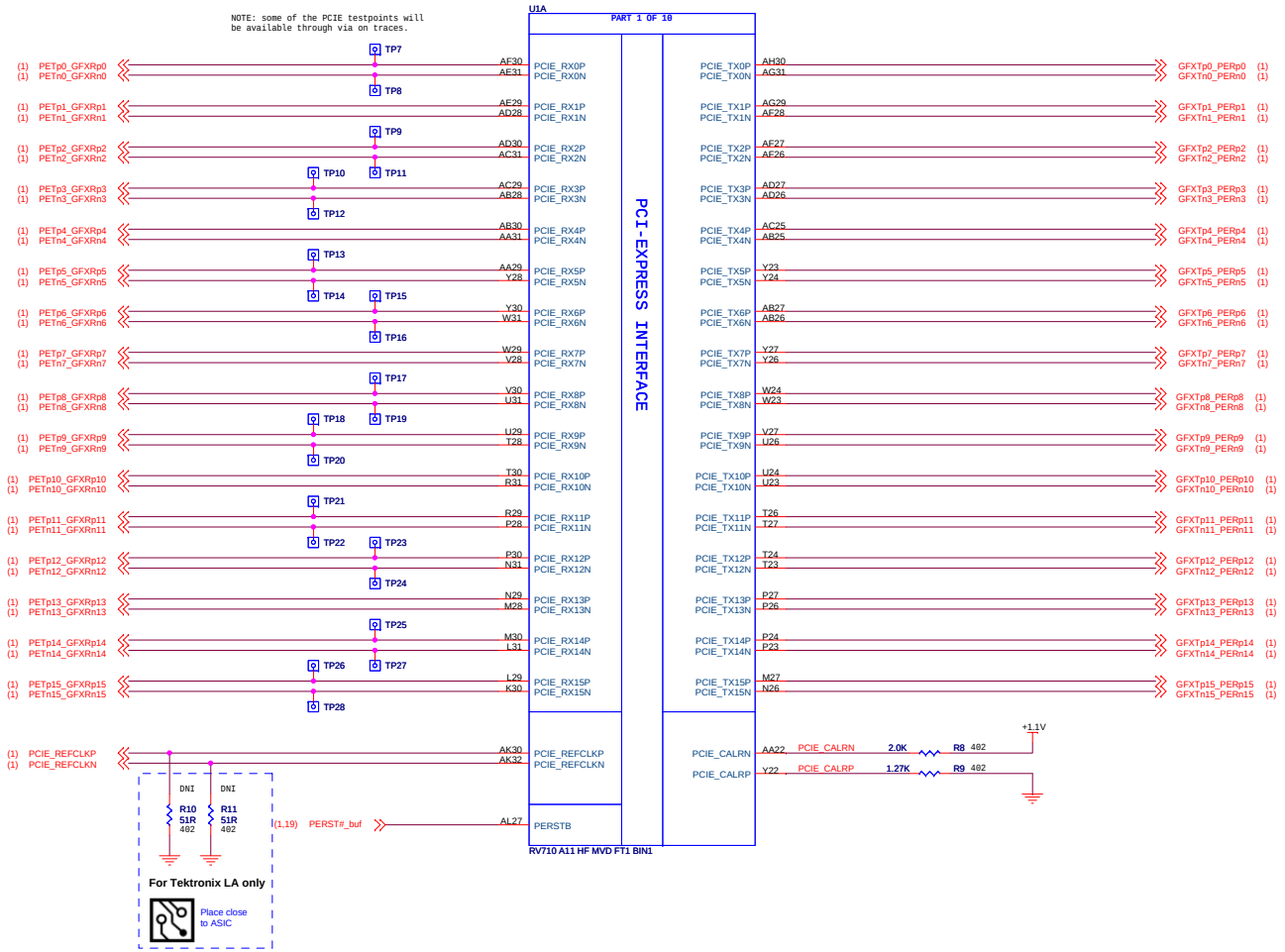

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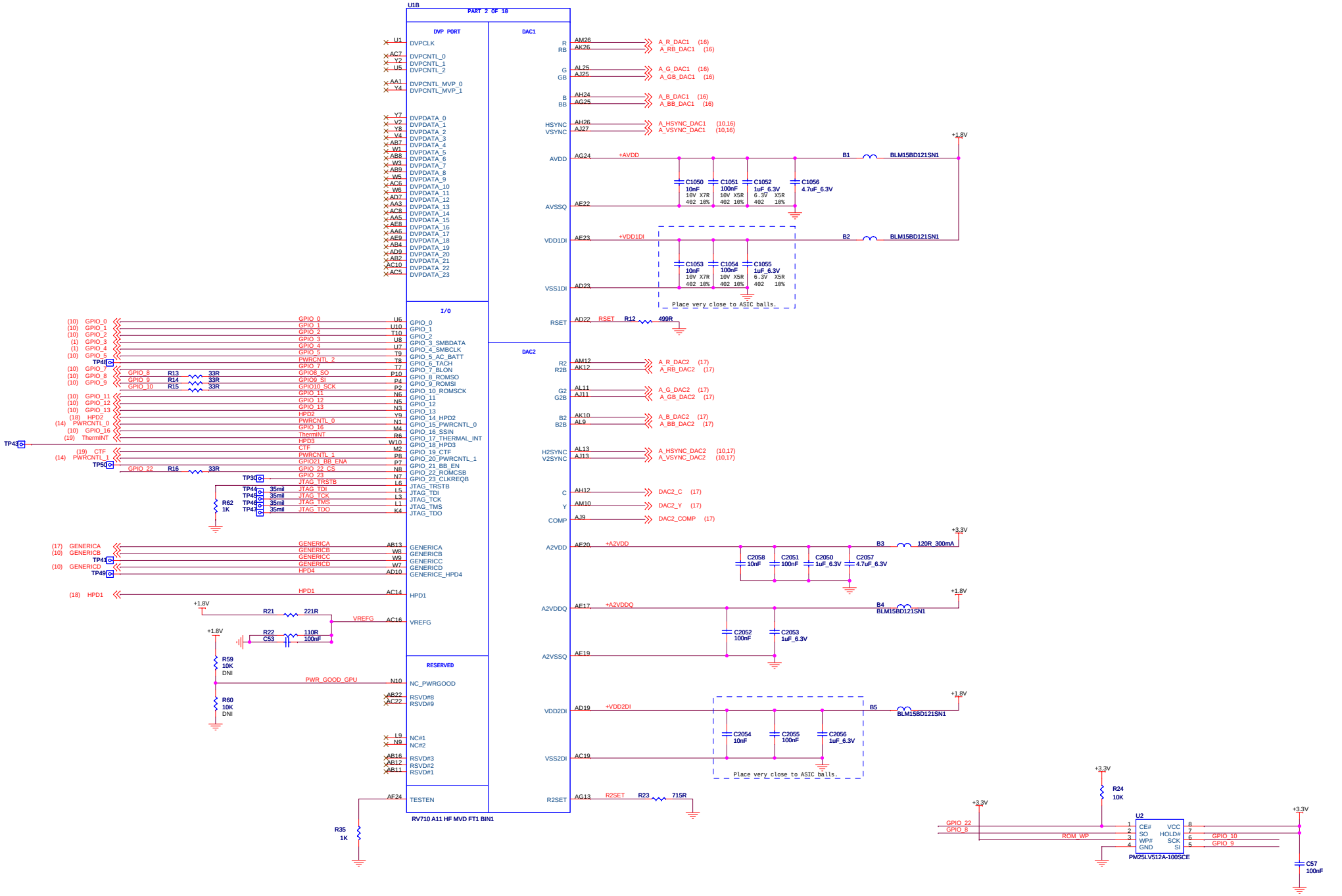
U1B
PART 2 OF 10
DVP PORT
DAC1
DAC2
I/O
RESERVED
DVPCLK
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
R
RB
G
GB
B
BB
HSYNC
VSYNC
AVDD
AVSSQ
VDD1DI
VSS1DI
RSET
R2
R2B
G2
G2B
B2
B2B
H2SYNC
V2SYNC
C
Y
COMP
A2VDD
A2VDDQ
A2VSSQ
VDD2DI
VSS2DI
R2SET
GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6_TACH
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
HPD1
VREFG
NC_PWRGOOD
RSVD#8
RSVD#9
NC#1
NC#2
RSVD#3
RSVD#2
RSVD#1
TESTEN
RV710 A11 HF MVD FT1 BIN1
A_R_DAC1 (16)
A_RB_DAC1 (16)
A_G_DAC1 (16)
A_GB_DAC1 (16)
A_B_DAC1 (16)
A_BB_DAC1 (16)
A_HSYNC_DAC1 (10,16)
A_VSYNC_DAC1 (10,16)
+1.8V
+AVDD
+VDD1DI
B1 BLM15BD121SN1
B2 BLM15BD121SN1
C1050 10nF 10V X7R 402 10%
C1051 100nF 10V X5R 402 10%
C1052 1uF_6.3V 6.3V X5R 402 10%
C1056 4.7uF_6.3V
C1053 10nF 10V X7R 402 10%
C1054 100nF 10V X5R 402 10%
C1055 1uF_6.3V 6.3V X5R 402 10%
Place very close to ASIC balls.
R12 499R
A_R_DAC2 (17)
A_RB_DAC2 (17)
A_G_DAC2 (17)
A_GB_DAC2 (17)
A_B_DAC2 (17)
A_BB_DAC2 (17)
A_HSYNC_DAC2 (10,17)
A_VSYNC_DAC2 (10,17)
DAC2_C (17)
DAC2_Y (17)
DAC2_COMP (17)
+3.3V
+A2VDD
+A2VDDQ
+VDD2DI
B3 120R 300mA
B4 BLM15BD121SN1
B5 BLM15BD121SN1
C2058 10nF
C2051 100nF
C2050 1uF_6.3V
C2057 4.7uF_6.3V
C2052 100nF
C2053 1uF_6.3V
C2054 10nF
C2055 100nF
C2056 1uF_6.3V
R23 715R
R35 1K
R21 221R
R22 110R
C53 100nF
R59 10K DNI
R60 10K DNI
R62 1K
R24 10K
U2
PM25LV512A-100SCE
C57 100nF
GPIO_22
GPIO_8
ROM_WP
GPIO_10
GPIO_9
PWR_GOOD_GPU
TP41
TP43
TP48
TP49
TP50
TP39
TP44
TP45
TP46
TP47
R13 33R
R14 33R
R15 33R
R16 33R
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
PWRCNTL_2
GPIO_7
GPIO8_SO
GPIO9_SI
GPIO10_SCK
GPIO_11
GPIO_12
GPIO_13
HPD2
PWRCNTL_0
GPIO_16
ThermINT
HPD3
CTF
PWRCNTL_1
GPIO21_BB_ENA
GPIO_22_CS
GPIO_23
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
HPD4
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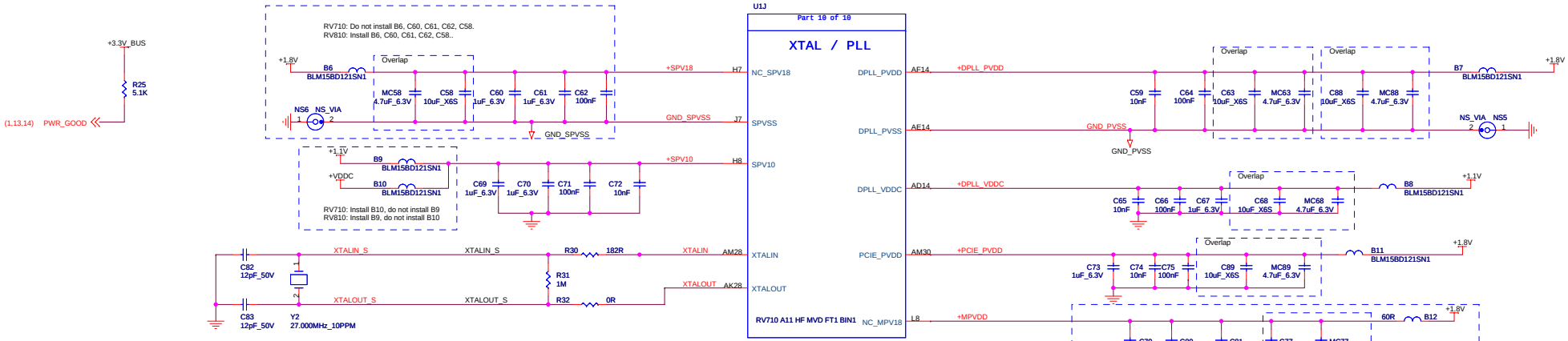
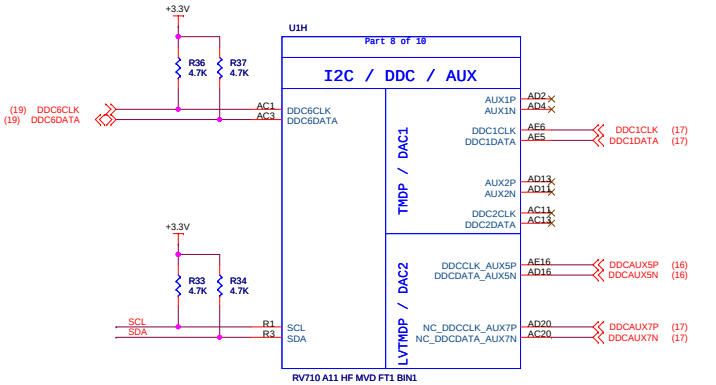


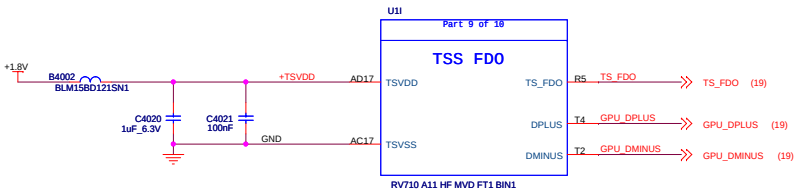
DDC6 BUS:

I2C Address	Function	Device
0x98	LM63 - External Temperature Sensor	LM63

SCL / SDA BUS:

I2C Address	Function	Device
N/A	N/A	N/A





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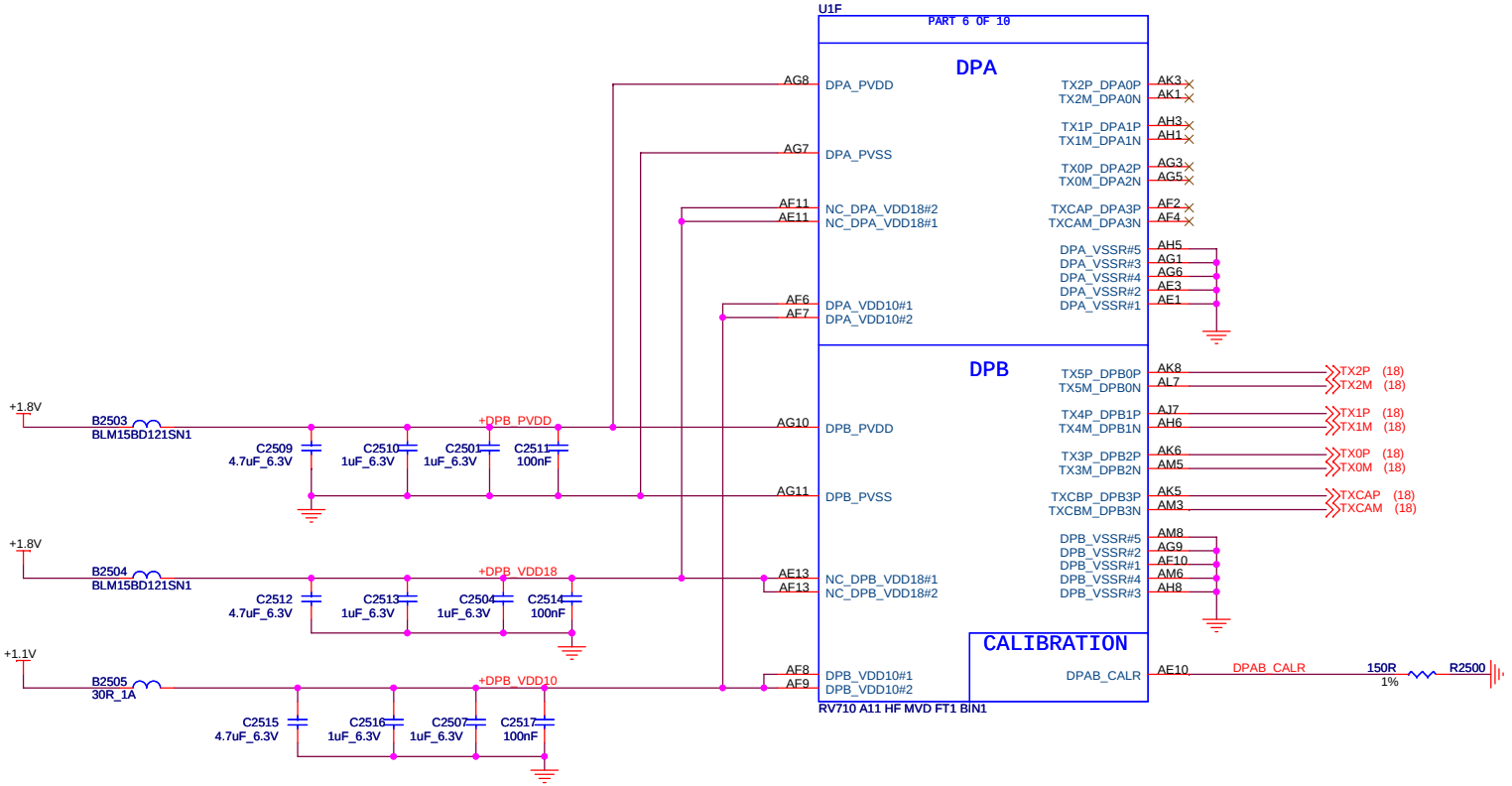
TMDP INTERFACE



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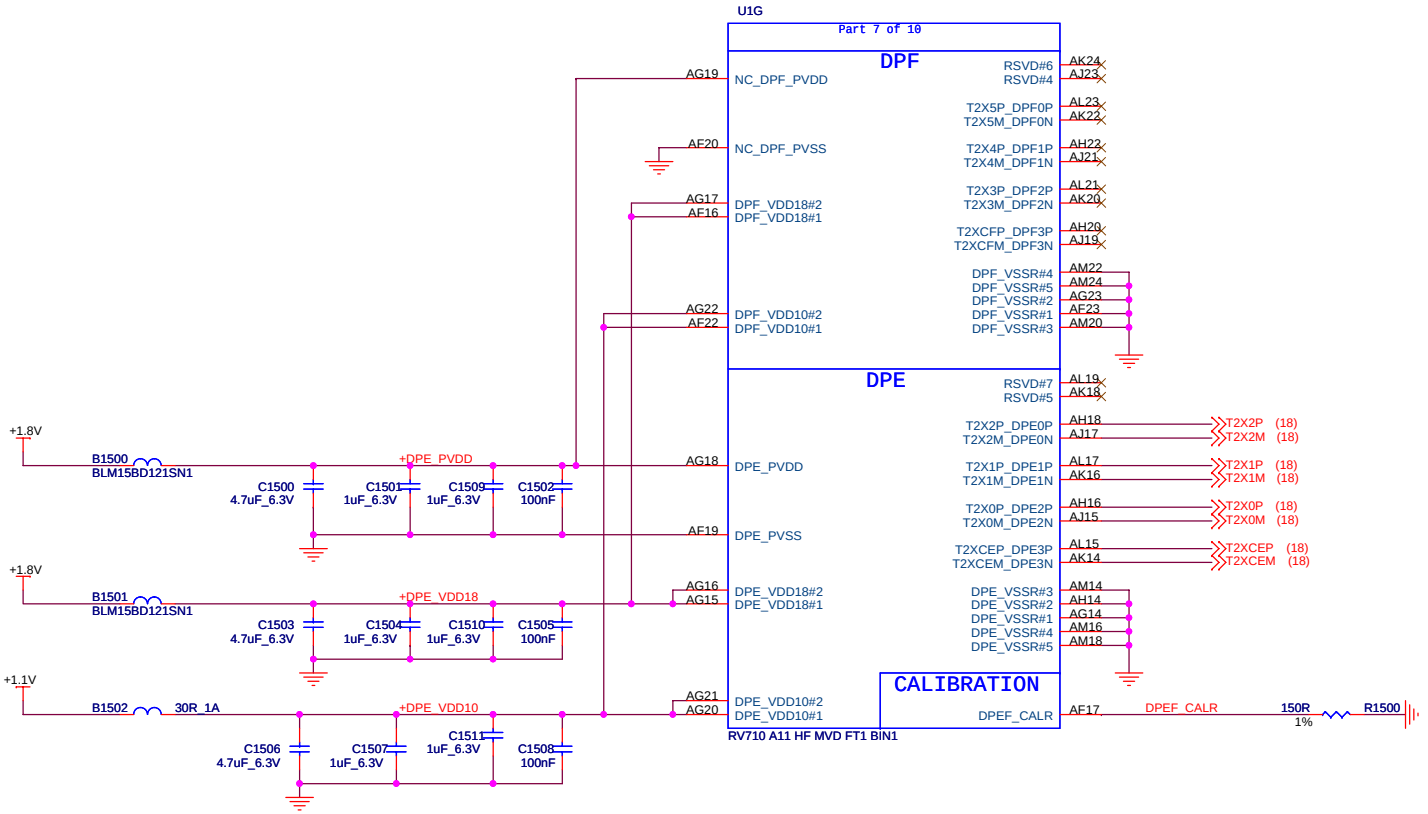
LVTMDP INTERFACE



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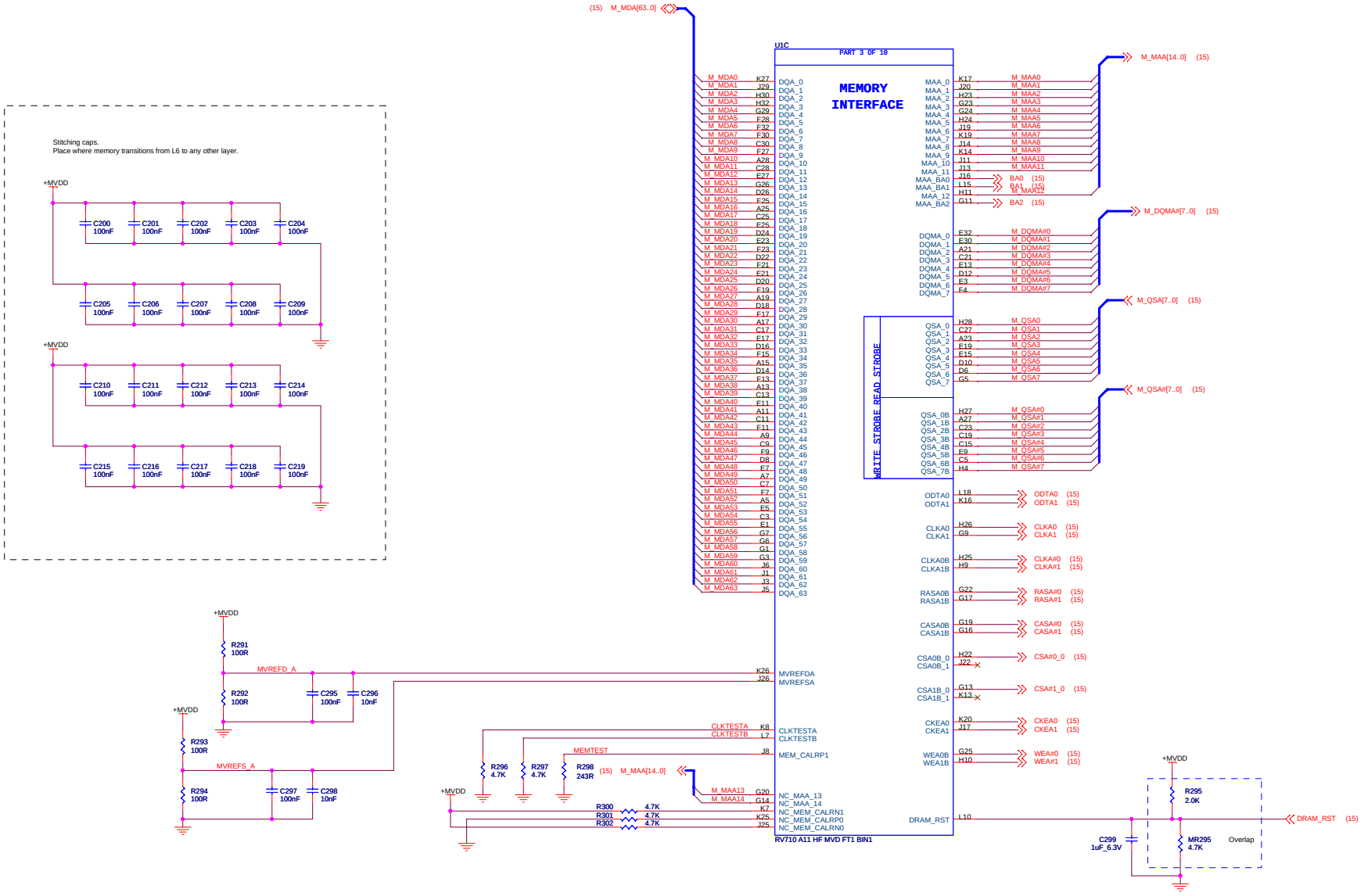
MEMORY INTERFACE



DIVIDER RESISTORS	DDR3
MVREF TO 1.8V	100R
MVREF TO GND	100R

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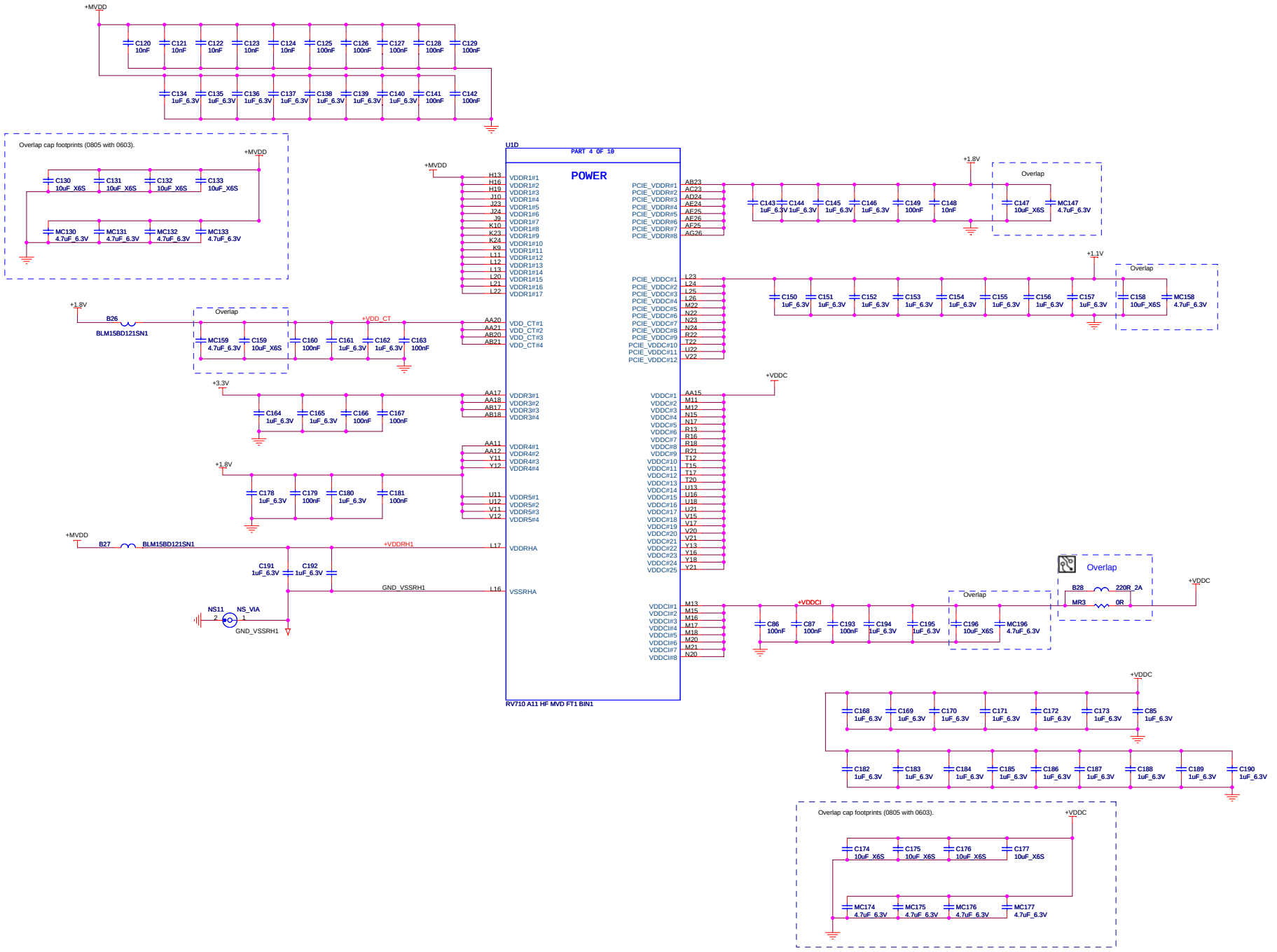

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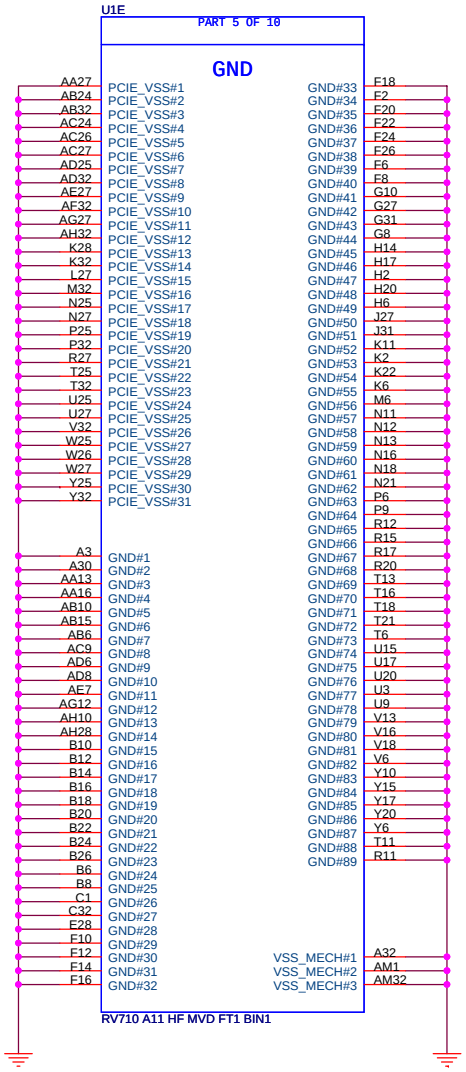

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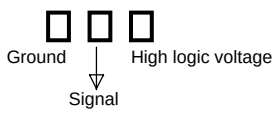
PIN BASED STRAPS

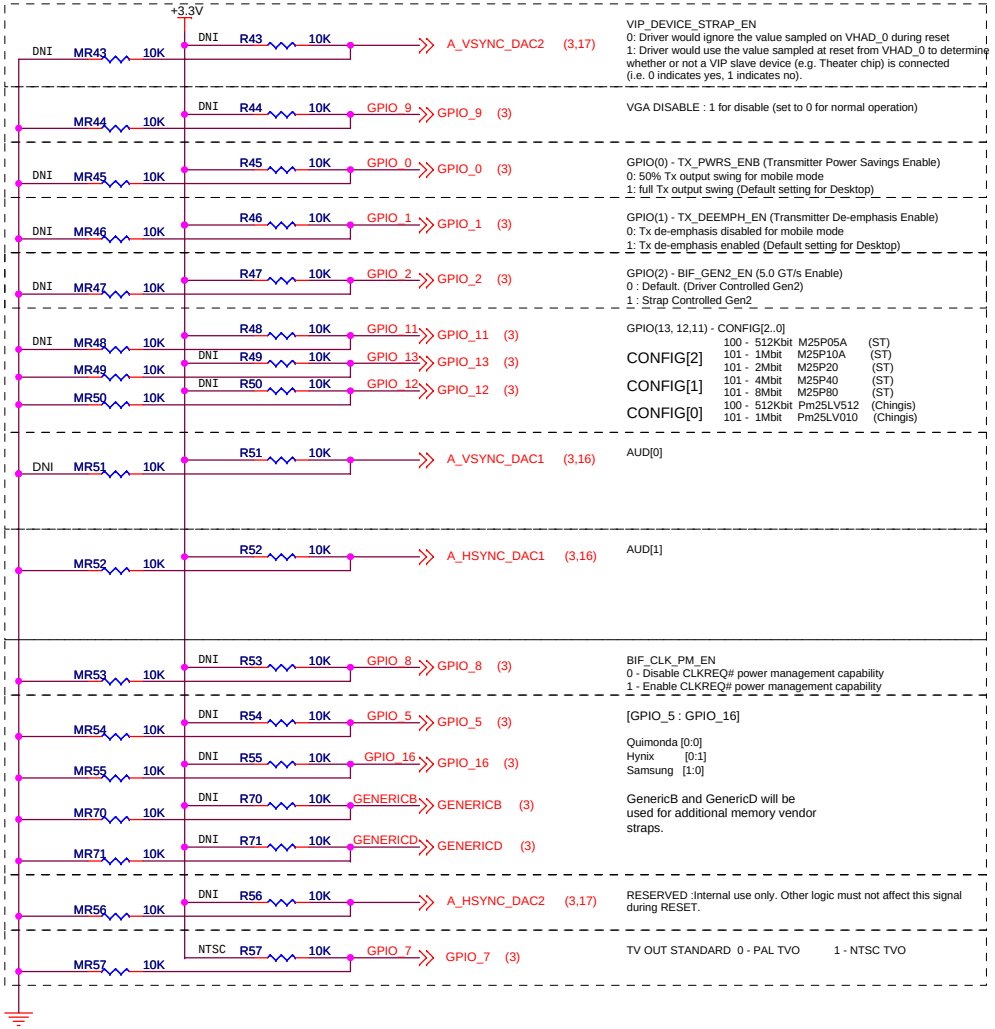
Pull-Down Resistors are for BU until built-in pull-downs are verified.

Overlap pads to save space and to prevent assembly of both resistors.

Layout



PIN BASED STRAPS



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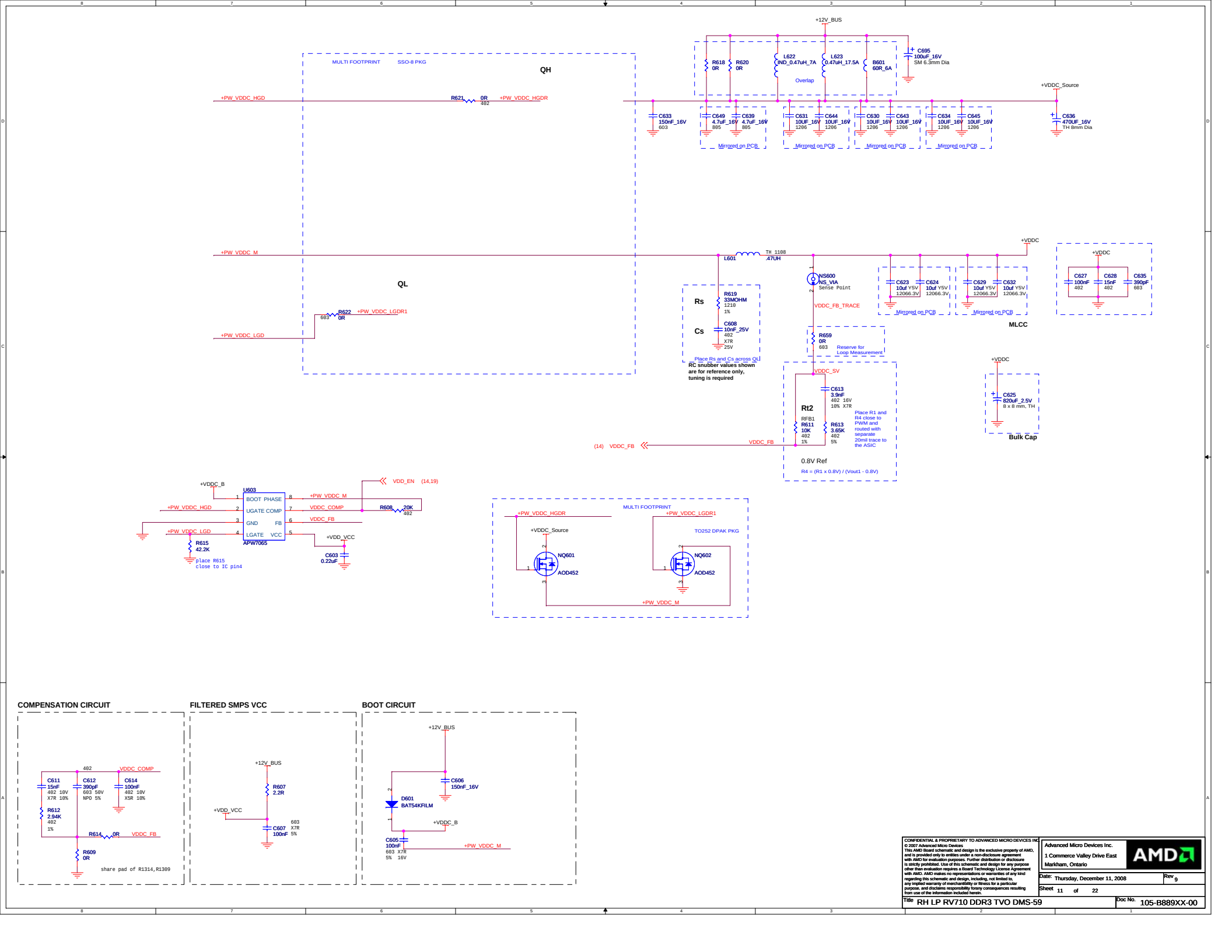

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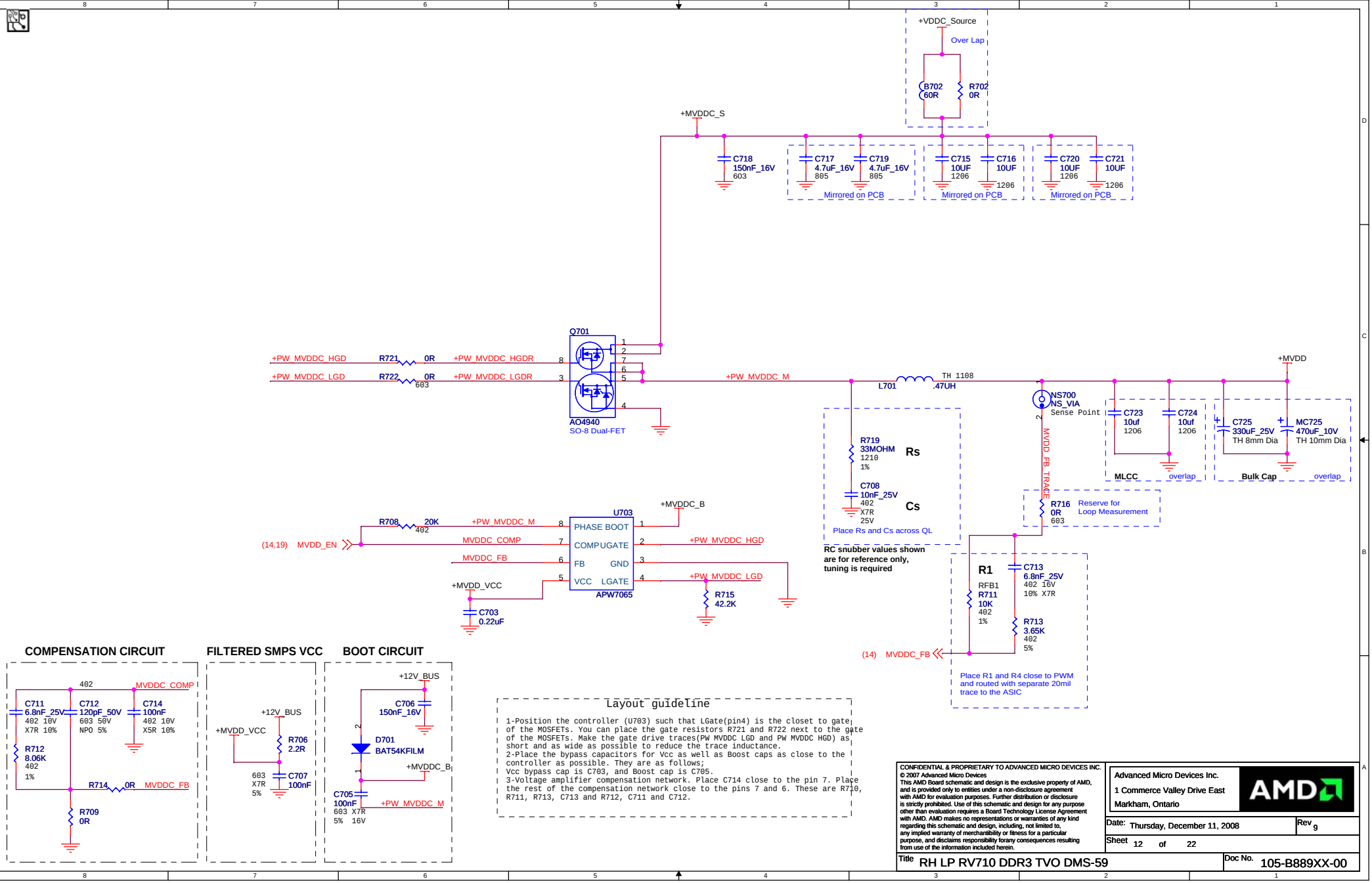

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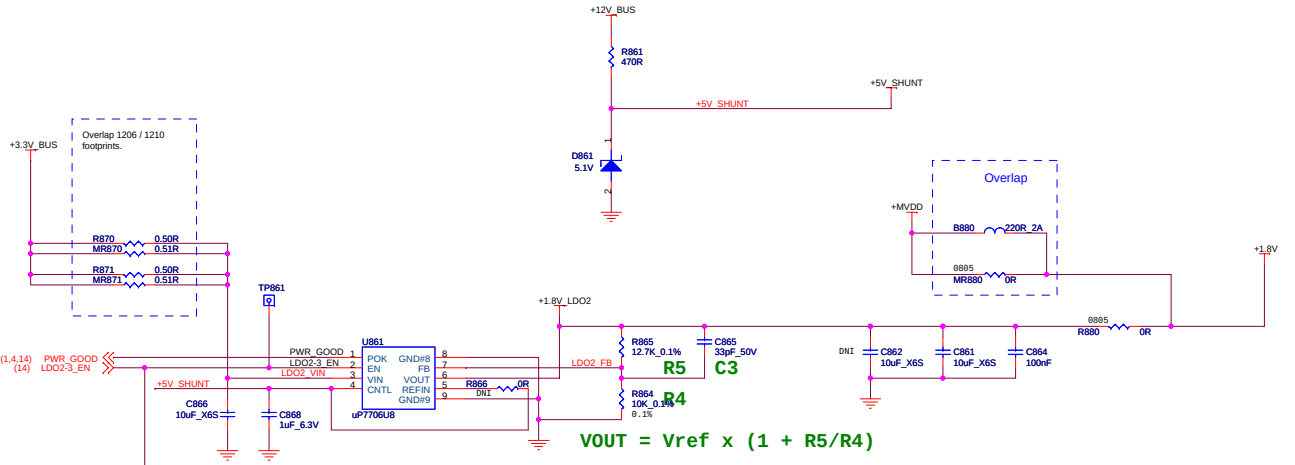
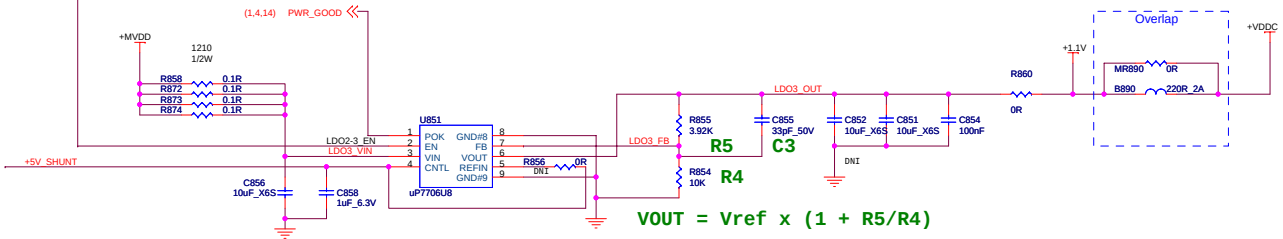
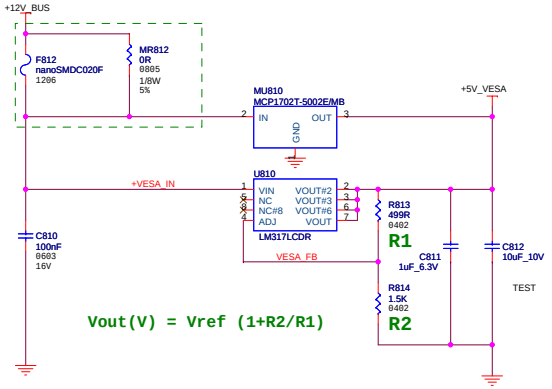
LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



LDO #3: Vin = +1.4V to 2.087VMAX Vout = +1.1V +/- 2.5% Iout = 1.4A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



Regulators for +5V_VESA



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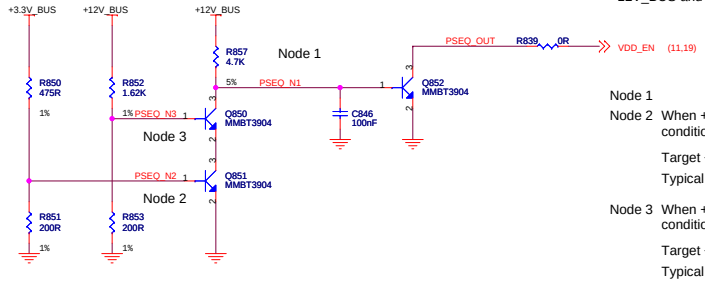
Power up/down Sequencing



Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.

Node 1

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

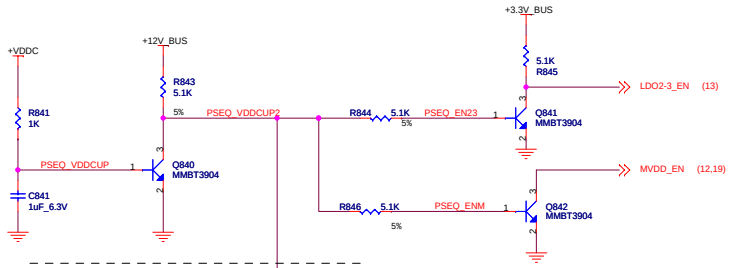
Typical trigger when +3.3V ramps above 2.2V (650mV)

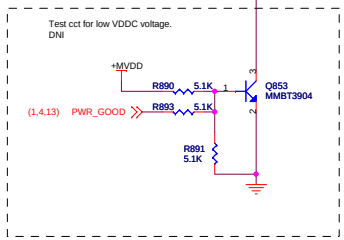
Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

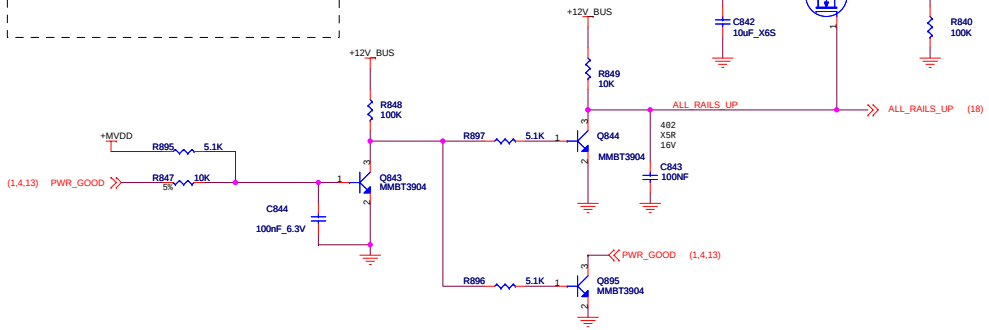
Target ~ 1.25V when +12 at min regulation (worse case)

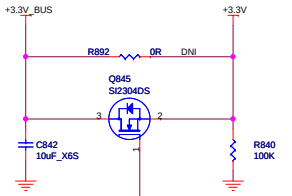
Typical trigger when +12V ramps above 10V (1.1V)

When +12V_BUS ramps above min Vbe, SMPS_EN will be held low





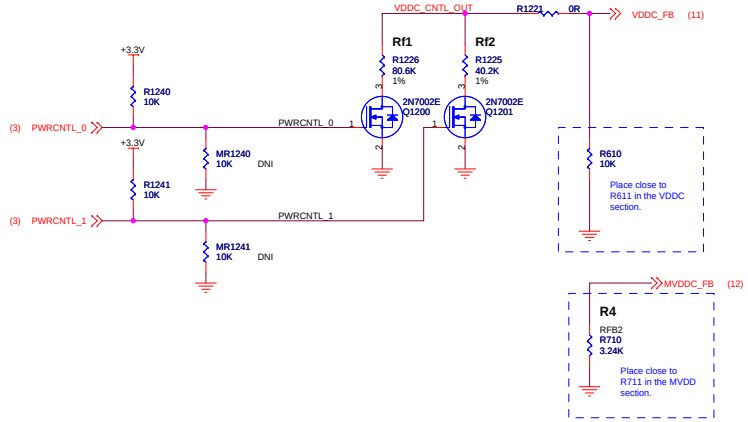




Power Play

VDDC Voltage Settings Using GPIOs

PWRCNTL_1 GPIO_20	PWRCNTL_0 GPIO_15	Output Voltage (V) Rf1= Rf2=		Rf1= Rf2=	Rf1= Rf2=	
0	0					
0	1					
1	0					
1	1	1	0	1		Power-up Default



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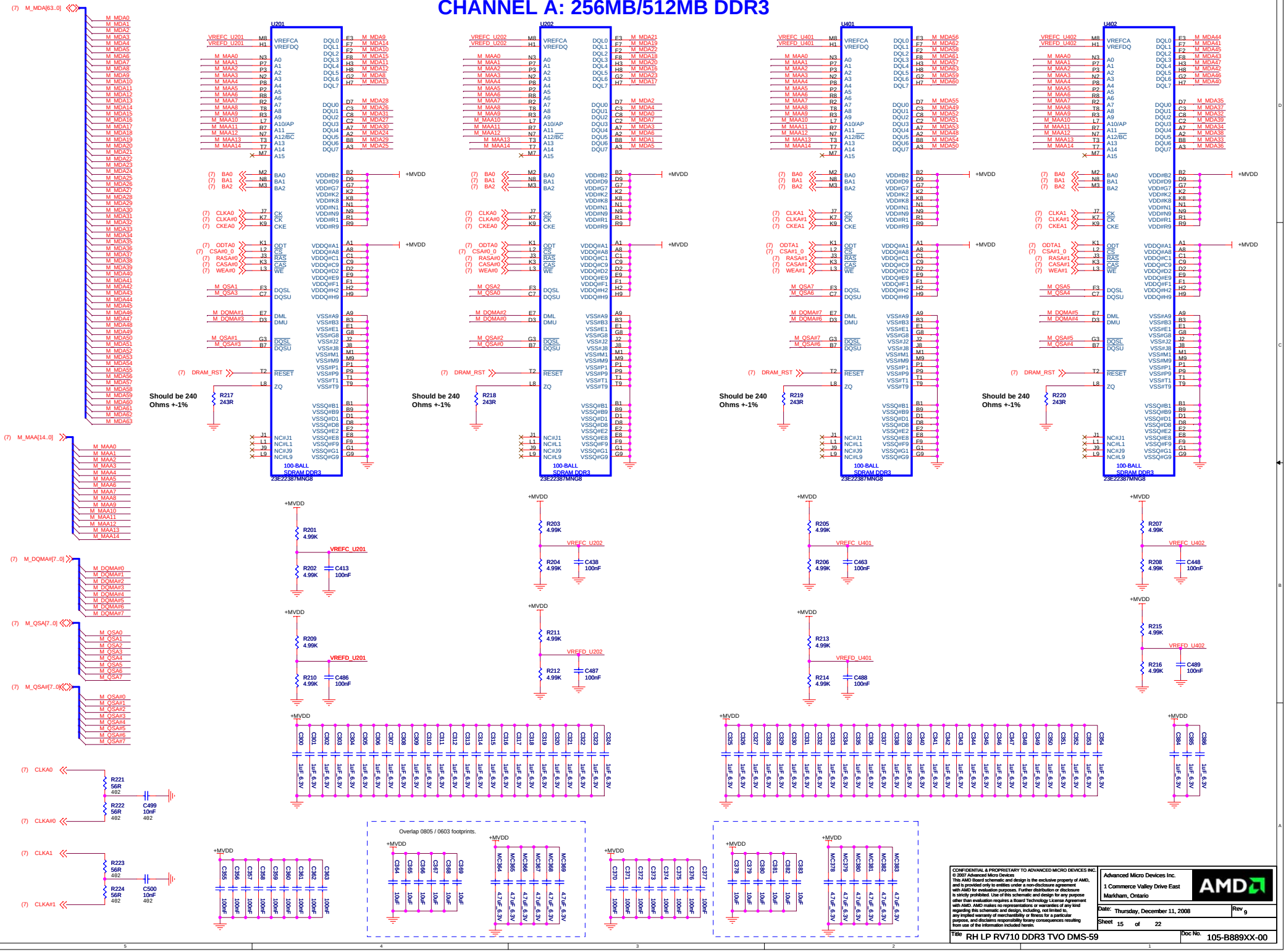
CHANNEL A: 256MB/512MB DDR3



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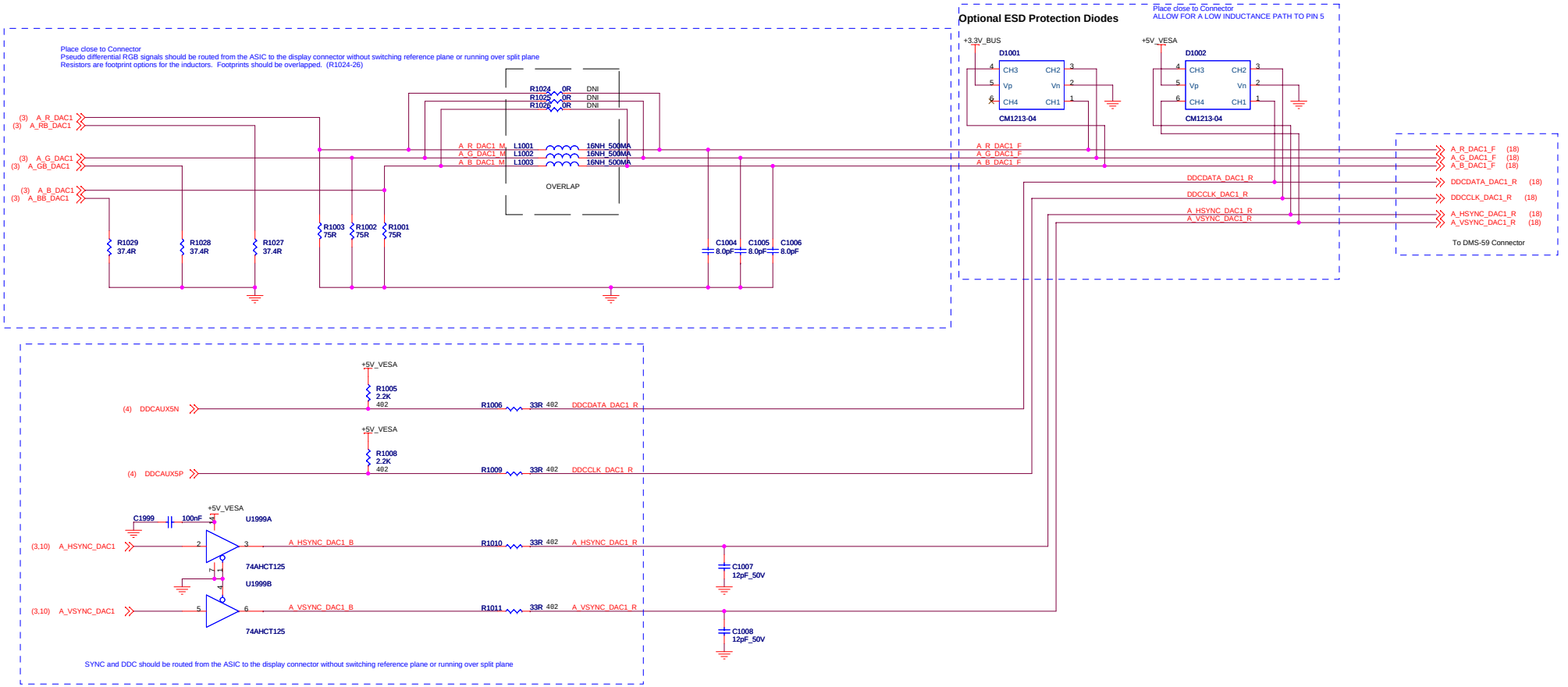
DAC 1 OUTPUT



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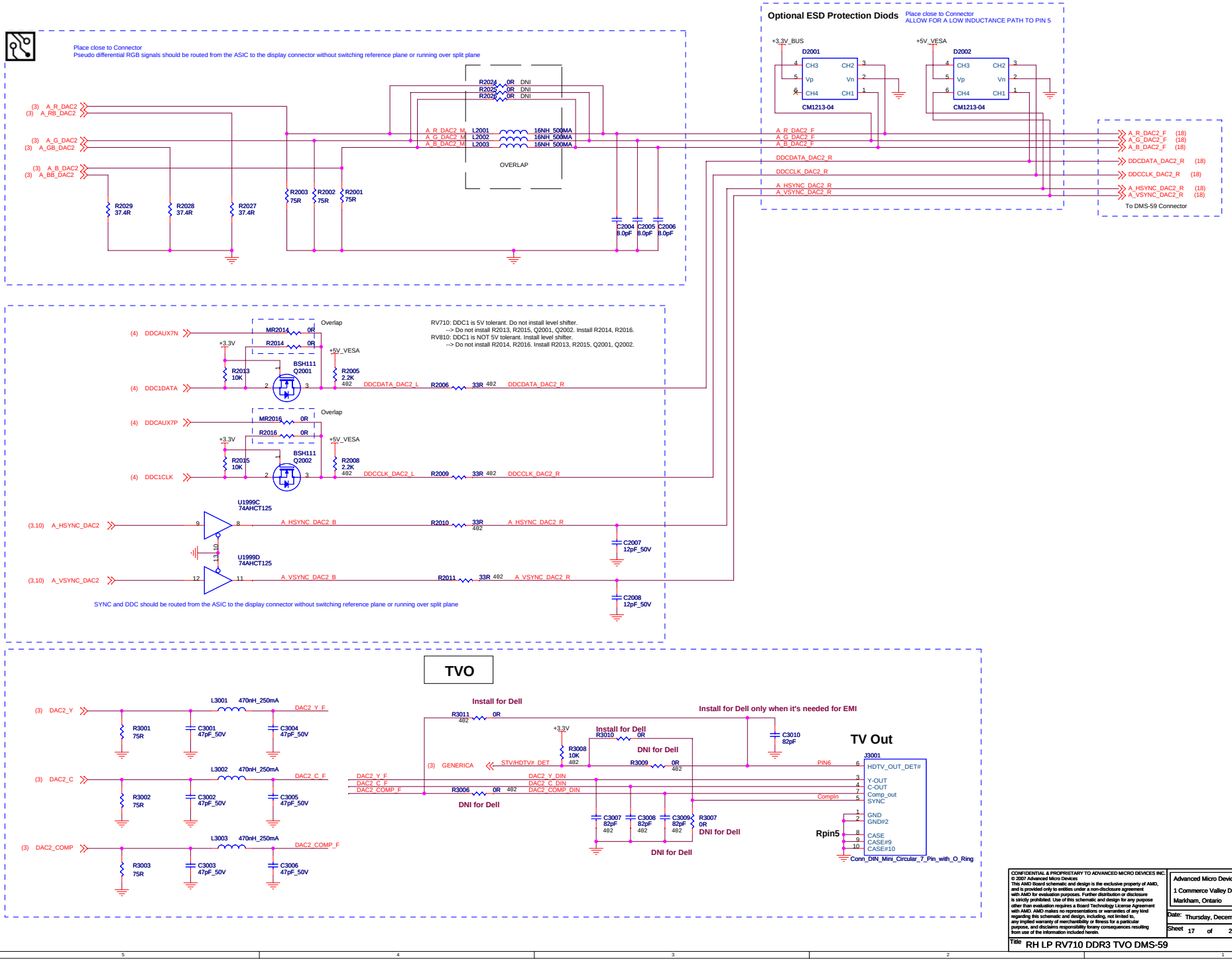
DAC 2 OUTPUT



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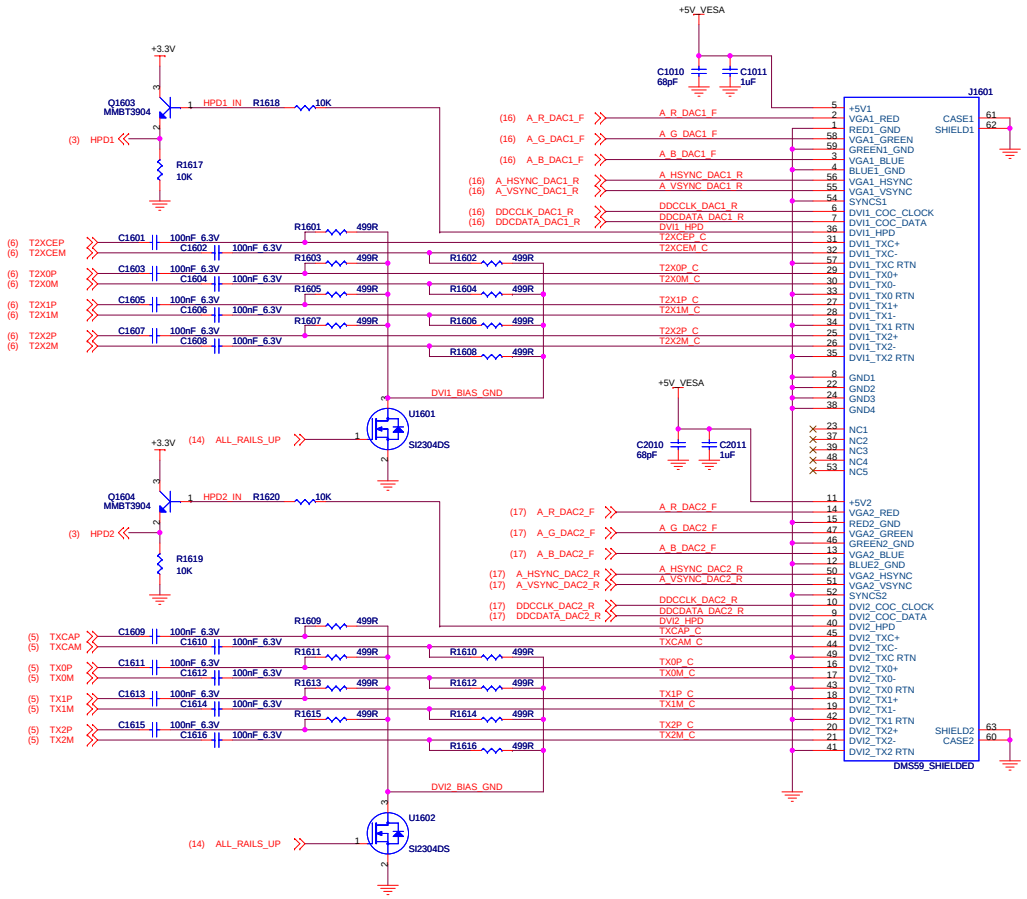
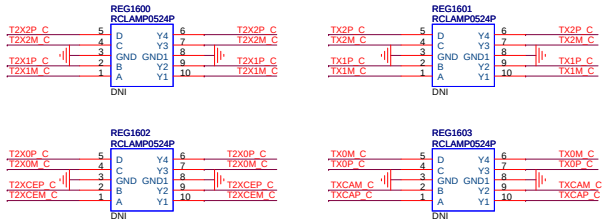
DMS-59 DPB / DPE OUTPUT



Optional ESD protection diodes



Connector 1	
Signals	Mapping
VGA:	DAC1
DVI:	Internal TMDP2
HPD:	HPD1
DDC:	DDC1
5V:	+5V_VESA

Connector 2	
Signals	Mapping
VGA:	DAC2 (TVDAC)
DVI:	Internal LVTMDS1
HPD:	HPD2
DDC:	DDC5
5V:	+5V_VESA

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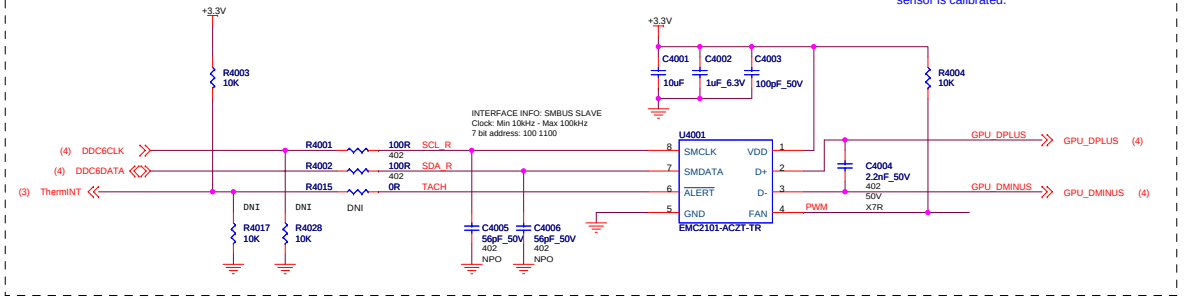
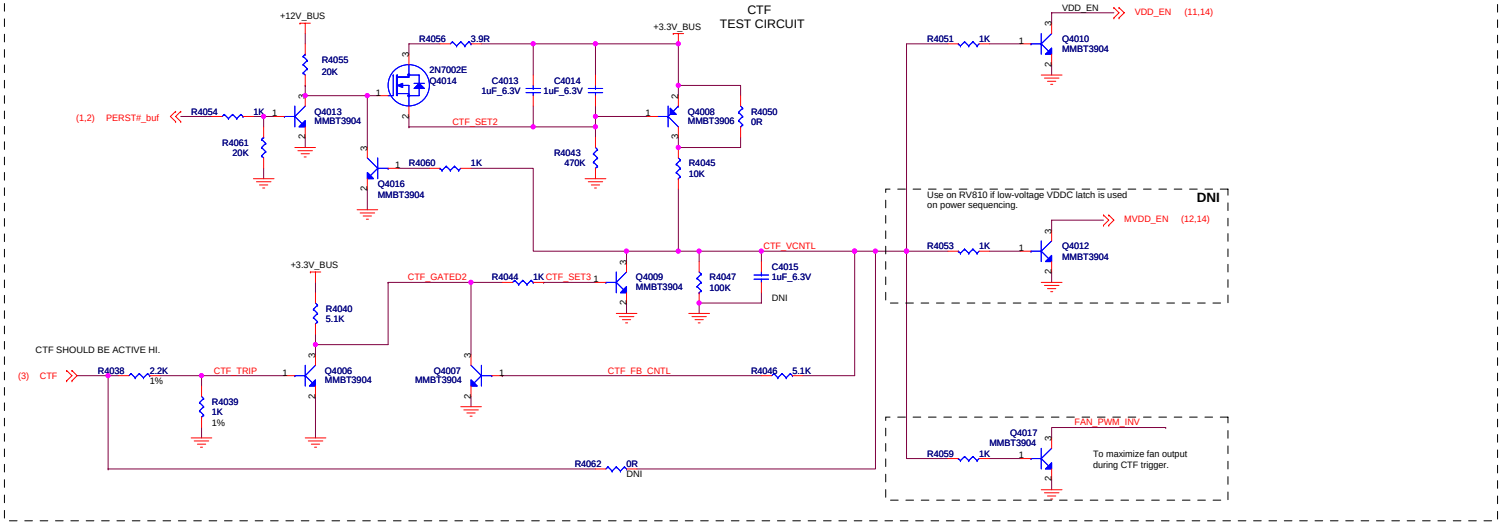
THERMAL MANAGEMENT

Remote Temperature Sensor

Remote diode temp sensor is for RV710 BU, until internal thermal sensor is calibrated.



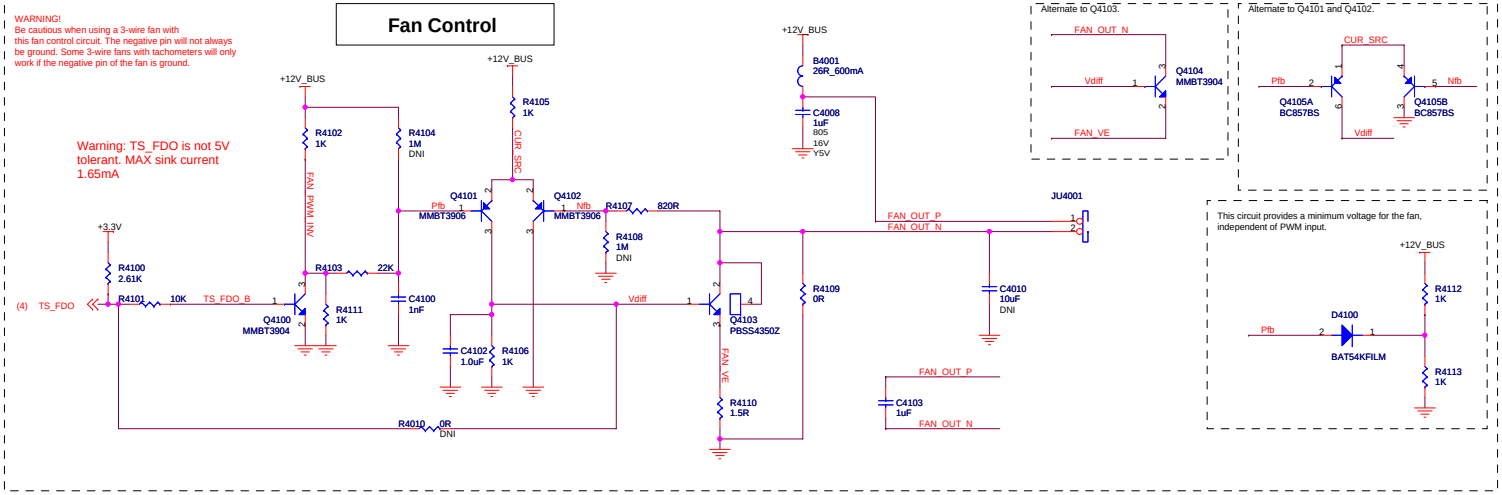
Critial Temperature Fault



Fan Control

WARNING!
Be cautious when using a 3-wire fan with this fan control circuit. The negative pin will not always be ground. Some 3-wire fans with tachometers will only work if the negative pin of the fan is ground.

Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA



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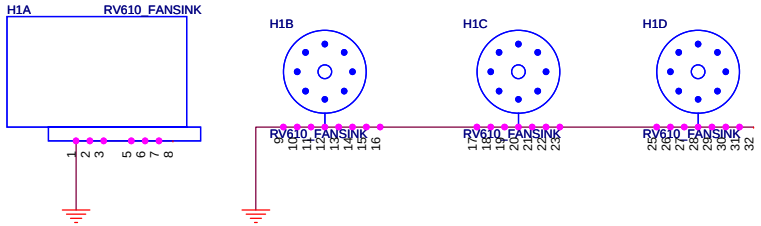

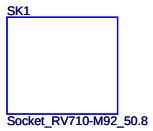

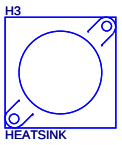

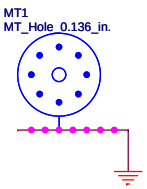

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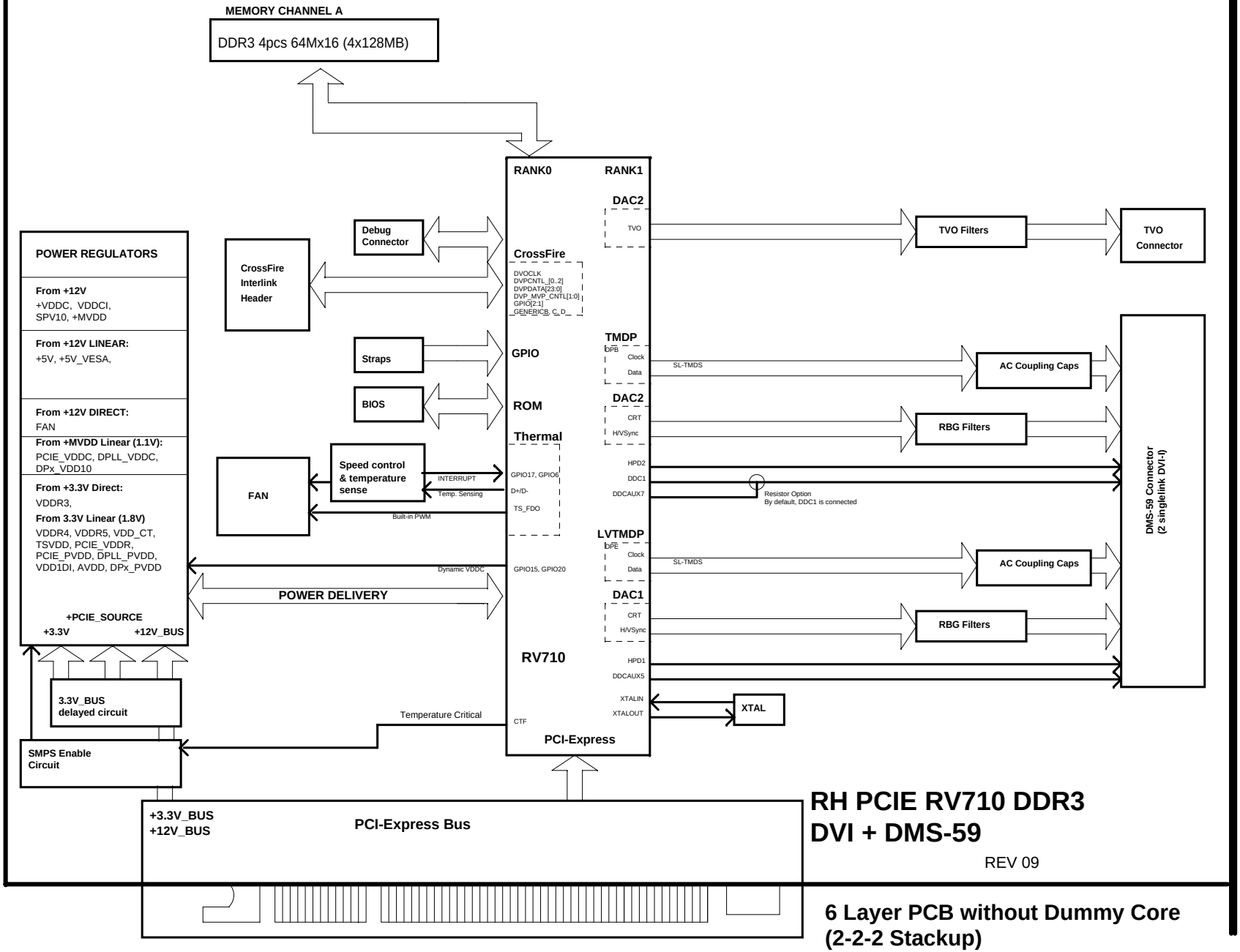

RH PCIE RV710 DDR3 DVI + DMS-59

REV 09

6 Layer PCB without Dummy Core (2-2-2 Stackup)

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Title	Schematic No.	Date:
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REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 9

RV710

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
01	00A	2008.11.11	INITIAL RELEASE OF B889 BOARD. BASED ON B754 Rev 90.
02	00A	2008.11.12	ADD R67 AS OPTION TO SHORT JTAG IO
03	00A	2008.11.13	REMOVE MT2
04	00A	2008.11.19	REMOVE MVDD GPIO VOLTAGE CONTROL OPTION
05	00A	2008.11.19	REMOVE LED AND PWR_GOOD CONNECTIONS TO CTF CIRCUIT
06	00A	2008.11.19	REMOVE MC625, PL601, NL601, ML601, R58 AND PROVIDE OPTION TO SHORT CTF TO CTF_VCNTL BY R4062
07	00A	2008.11.24	CHANGE DAC INDUCTORS TO 0603 PART, REMOVE C1001-C1003 and C2001-C2003
08	00A	2008.11.25	REMOVE R26, CHANGE MVDD FET SYMBOL
09	00A	2008.12.01	CHANGE PIN ASSIGNMENT OF D2001 AND REG1603 FOR LAYOUT