

P727-A01: G96, GB1-128, GDDR3, DL-DVI, DL-DVI/VGA, SD/HDTV

V129-12

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- Page 23: POWER SUPPLY: FBVDDQ +PEX_VDD SINGLE PHASE SWITCHER
- Page 24: POWER SUPPLY: NVVDD DUAL PHASE SWITCHER
- Page 25: POWER SUPPLY: Dynamic NVVDD

REV 1.2 HISTORY

04/01

PAGE 12.Remove J1 Slim-DSUB connector

PAGE 15.Add R761 and R762 to reserve pull down DP AUX
Change F503 and F504 footprint to 1812 size
Remove DP J8 Pin25,Pin26

PAGE 18.Change U514~U517 to EM1~EM6

PAGE 19.Add 2pin Fan control circuit

PAGE 23.Add C120,C149 10uF 1206 footprint to reserve PEX_VDD power

04/08

PAGE 22. Add R92 0805 0ohm Resistor for 3V3 bypass to 2V5 power

REV	VARIANT	NPVN	ASSEMBLY
B	BASE	600-10727-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU000	600-10727-0000-100	G96-400, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
2	SKU001	600-10727-0001-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
3	SKU002	600-10727-0002-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI
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PAGE DETAIL	TABLE OF CONTENTS

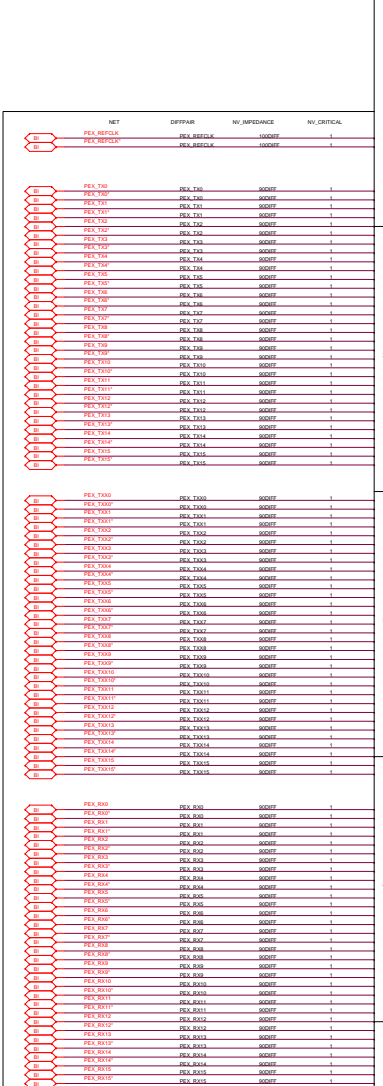
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G1A



	SIN_LIN_WIDTH	VOLTAGE
2.00	BI NVDD_SENSE	1.2V
2.00	BI NVDD_GND_SENSE	0V
	BI PEX_PLLVD	1.08V
	BI 3V3	1.70V 3.3V 3A
	BI 12V	1.28V 12V 5.5A

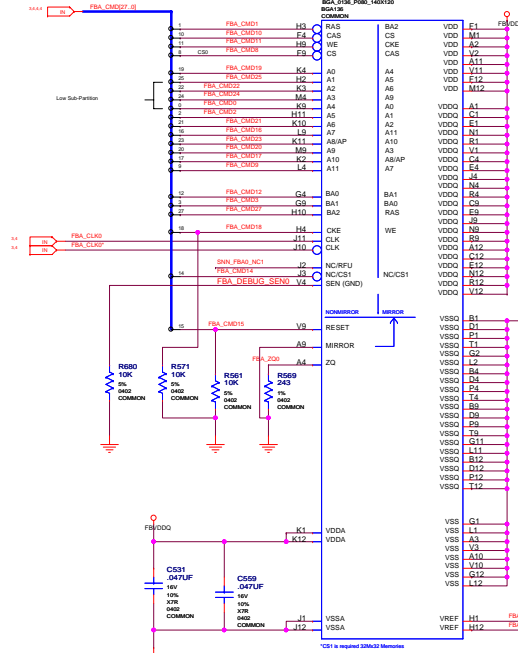
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FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3

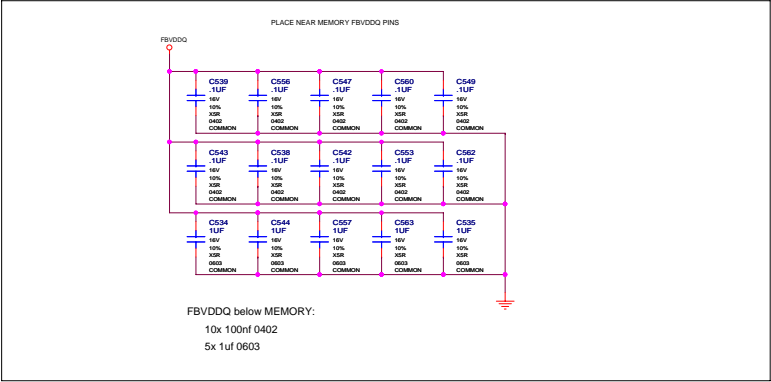
FB_A-CS0-LOW-32bit

M3E

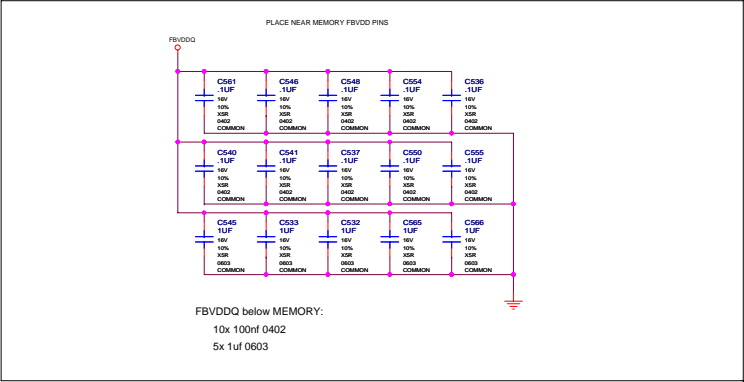


FRAME BUFFER: PARTITION A DECOUPLING

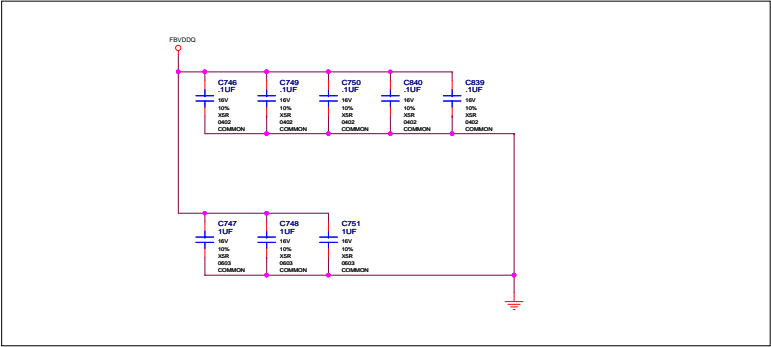
Decoupling for FBA 0..31



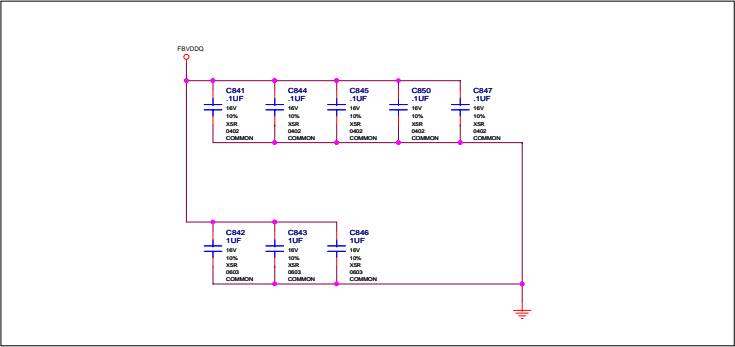
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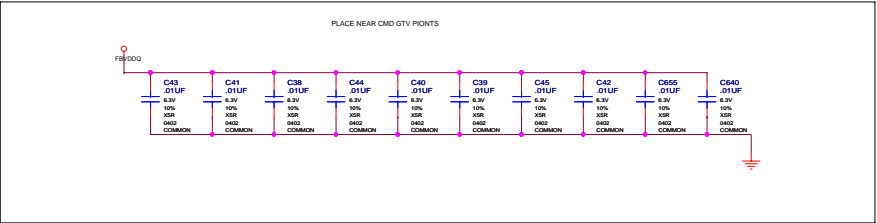
Decoupling for FBA A1 0..31



Decoupling for FBA A1 0..31



Return path coupling GND/FBVDDQ for FBA

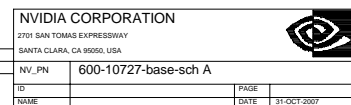
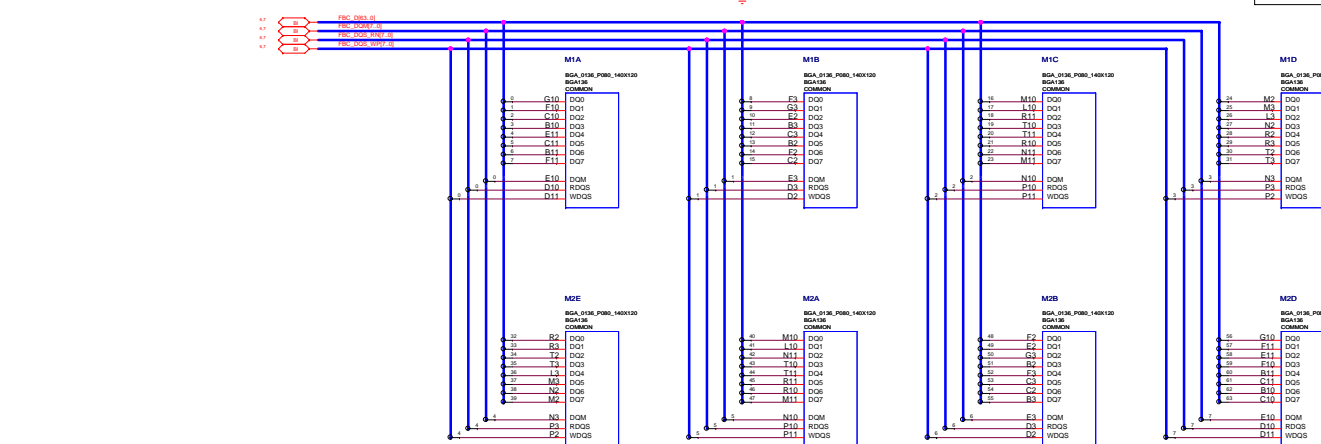


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PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

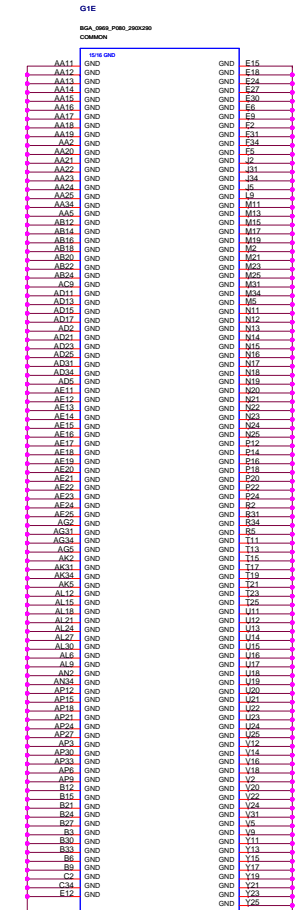
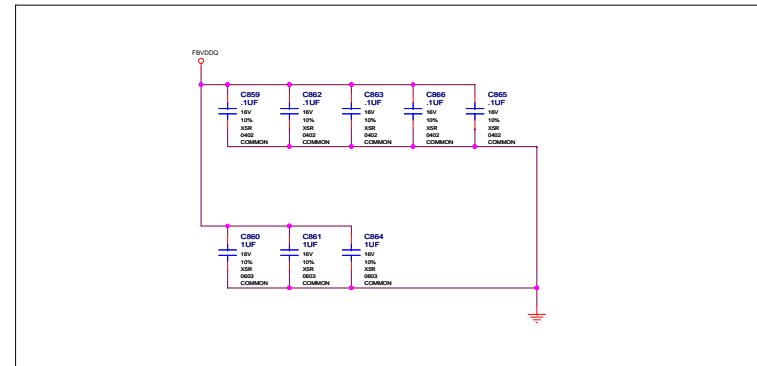
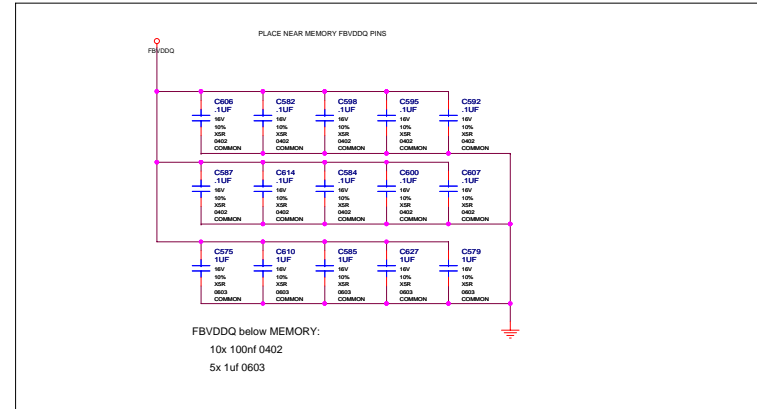
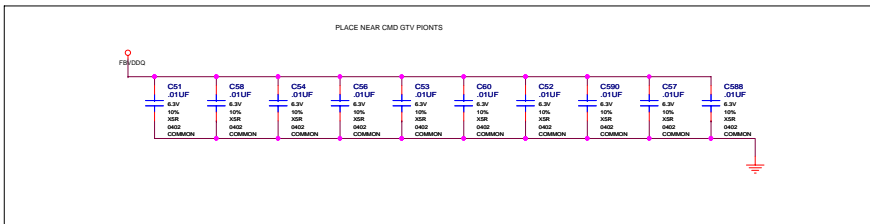
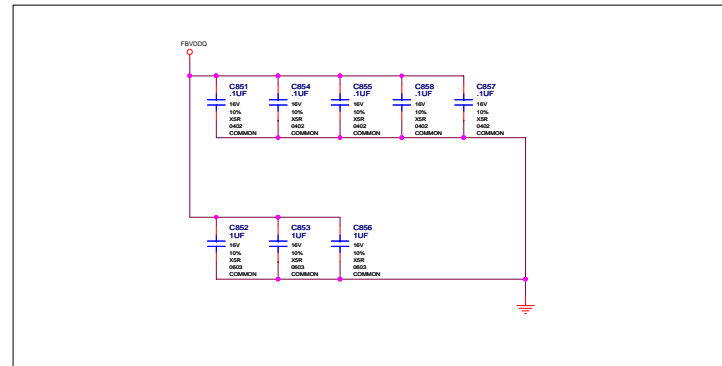
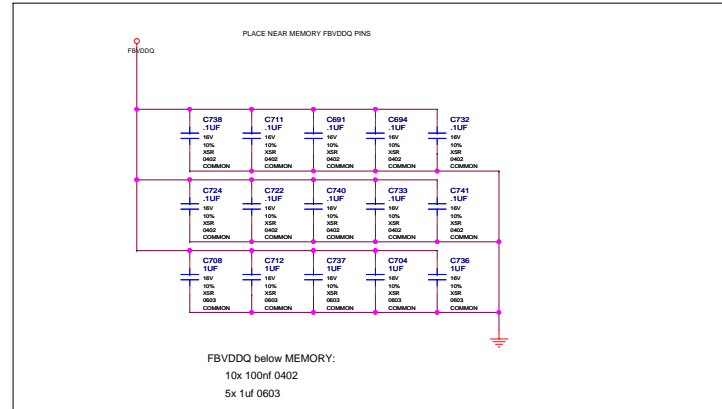
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4.7	10 FRC_C408	FRC_C408	800F	1
4.7	10 FRC_C407	FRC_C408	800F	1
4.7	10 FRC_C401	FRC_C401	800F	1
4.7	10 FRC_C401	FRC_C401	800F	1
			NV_IMPEDANCE	NV_CRITICAL_NET
4.7	10 FRC_0203_0		800H	1
4.7	10 FRC_0207_0		800H	1
4.7	10 FRC_0208_0P7		800H	1
4.7	10 FRC_0208_0M7		800H	1
4.7	10 FRC_020207_0		800H	1
			MIN_LINE_WIDTH	
10	FRC_VREF0	0.000	10M	
10	FRC_VREF1	0.000	10M	
10	FRC_VREF2	0.000	10M	
10	FRC_VREF3	0.000	10M	




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Decoupling for FBC 0..31



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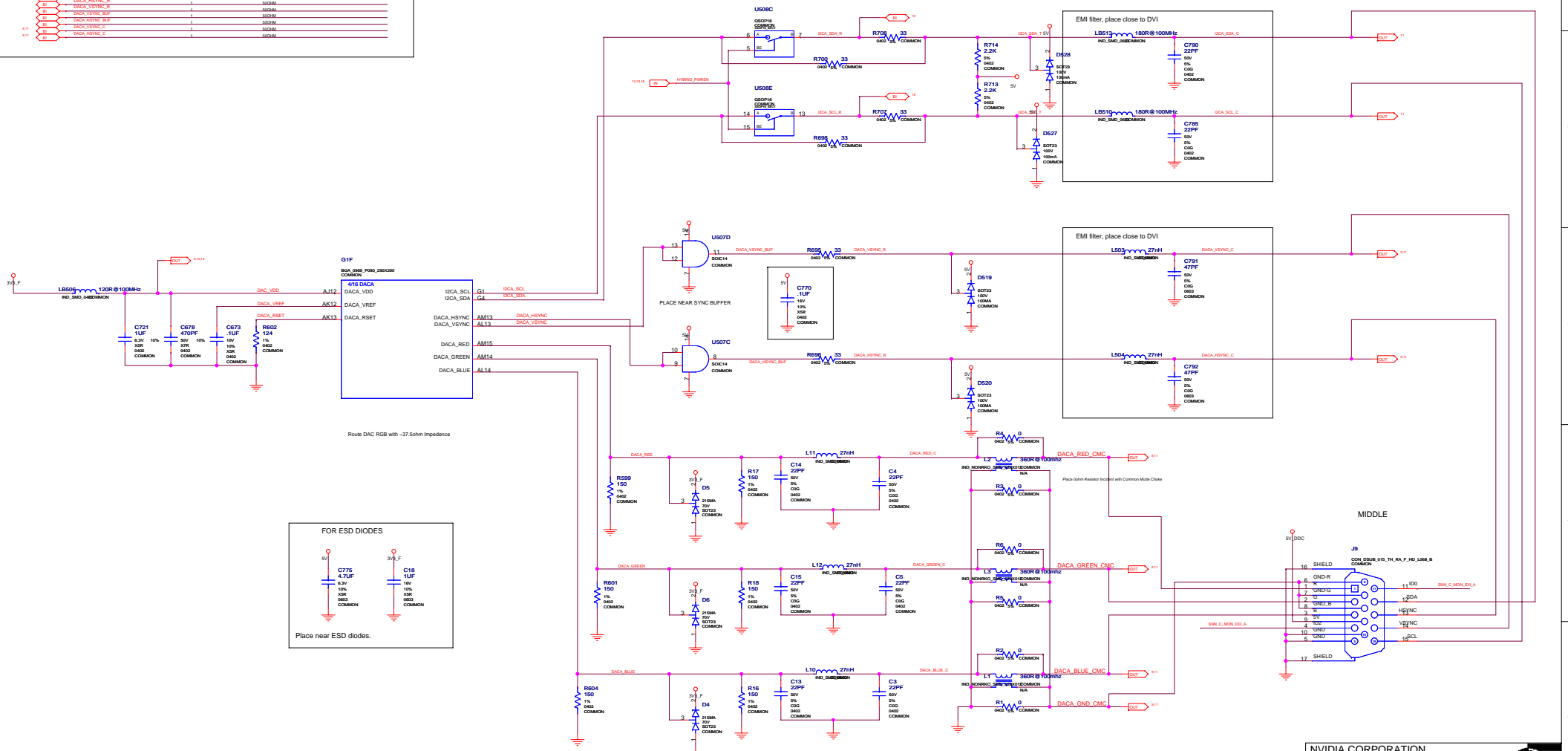
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS, GPU GND CONNECTIONS

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	NET_NAME	WV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
6.3.1.4	IN			3.30 120ML
	DATA_VDD			
	DATA_VREF			120ML
	DATA_VBIAS			120ML
	DATA_RSD	1	75OHM	
	DATA_SCREEN	1	75OHM	
	DATA_WIRE	1	75OHM	
	DATA_RSD_C	1	75OHM	
	DATA_SCREEN_C	1	75OHM	
	DATA_WIRE_C	1	75OHM	
6.3.1.5	DATA_GND_CMIC			2V 120ML
6.3.1.6	DATA_SCREEN_CMIC	1	75OHM	
6.3.1.7	DATA_WIRE_CMIC	1	75OHM	
6.3.1.8	DATA_VHYNC	1	50OHM	
	DATA_VHYNC	1	50OHM	
	DATA_VHYNC_B	1	50OHM	
	DATA_VHYNC_C	1	50OHM	
	DATA_VHYNC_BUF	1	50OHM	
	DATA_VHYNC_BUF	1	50OHM	
6.3.1.9	DATA_VHYNC_C	1	50OHM	
	DATA_VHYNC_C	1	50OHM	

Primary Display (DACA), DVI-I

DACA RGB-FILTER



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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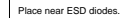


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Accession	Gene	Protein	Accession
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10.12	DACC_HSYN2_C	1	SDCHM

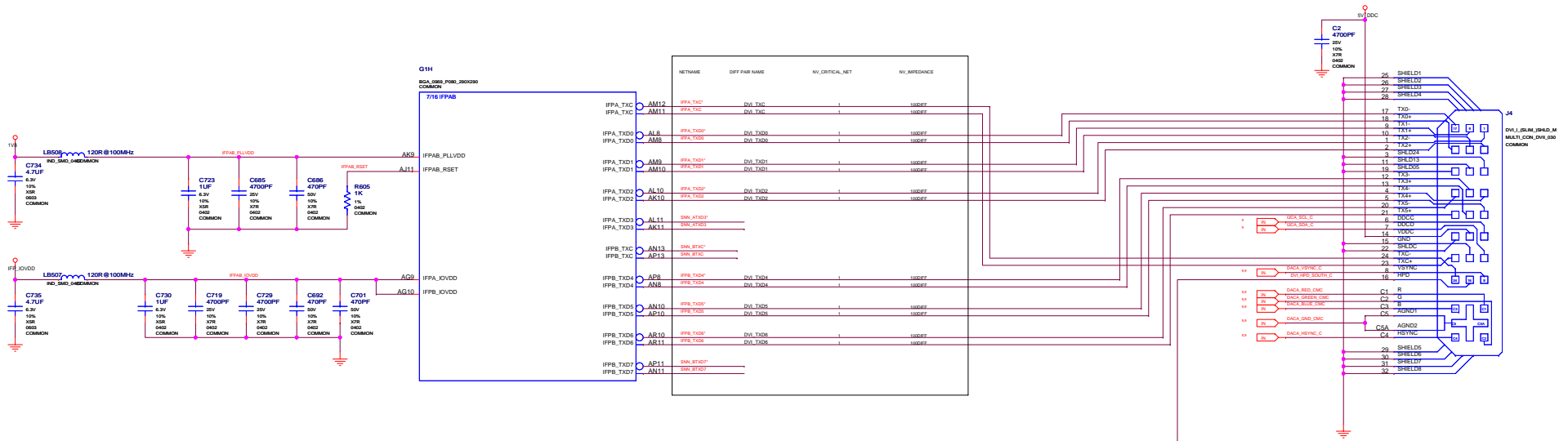


PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID
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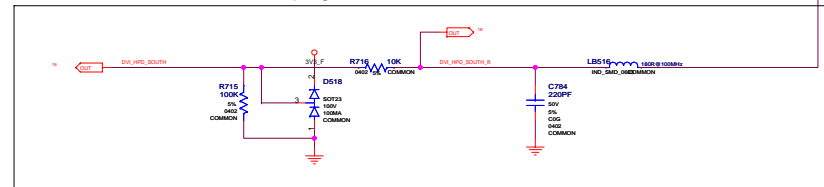
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TMDS LINK: A & B



Hotplug Detection



	NETNAME	MIN_LINE_WIDTH	VOLTAGE
SI	IFPAB_FLLVDD	12MIL	1.8V
SI	IFPAB_I0VDD	12MIL	3.3V
SI	IFPADGET	12MIL	

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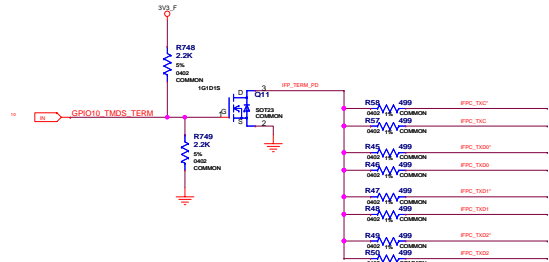


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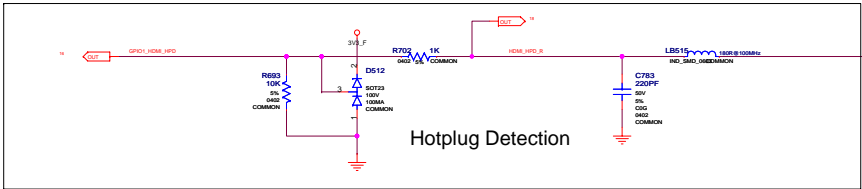
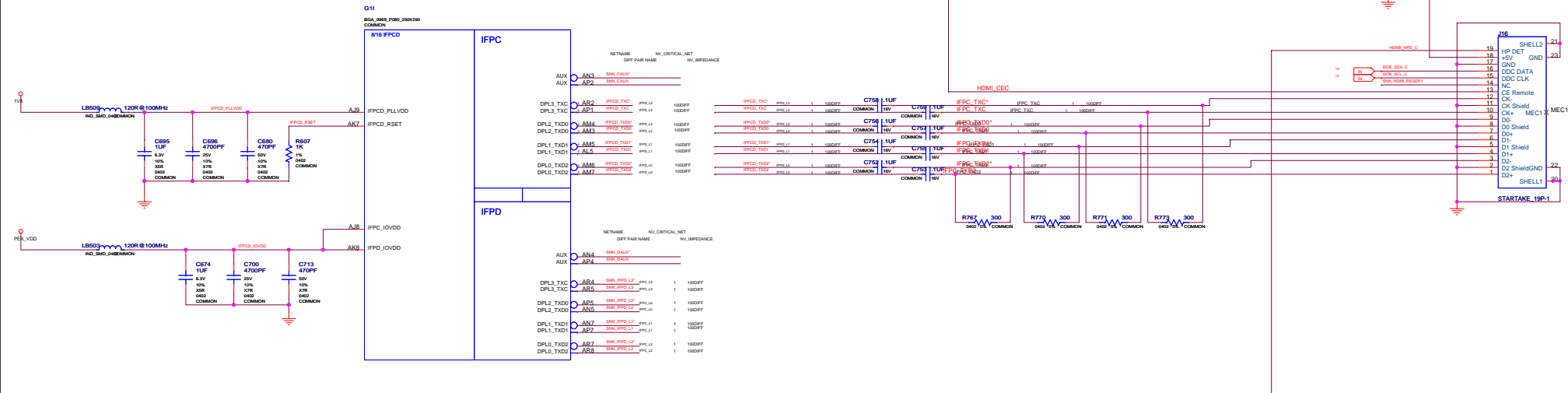
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TMDS LINK: C & D



TMDS C : HDMI



NETNAME	MIN_LENGTH	VOLTAGE
IFPCD_PLVDD	1.2MM	1.8V
IFPCD_OVDD	1.2MM	2.2V
IFPCD_TERM_PD	0.5MM	1.8V

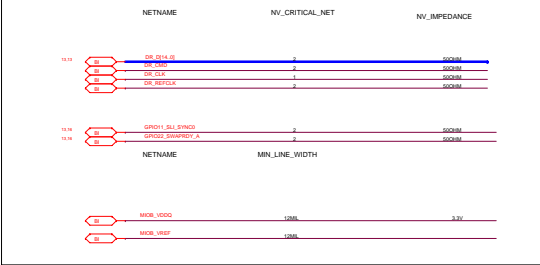
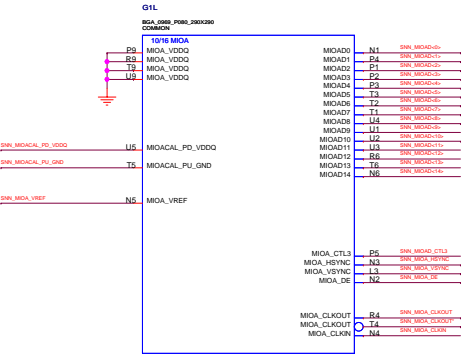
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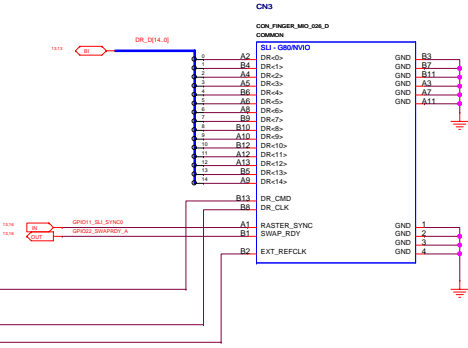
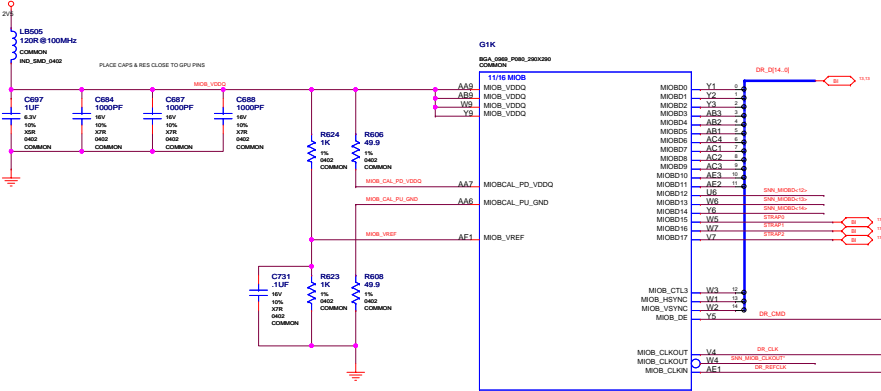
REV	DATE	DESCRIPTION
1.0	31-OCT-2007	Initial Release

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MIOA/B SLI



SLI Connector



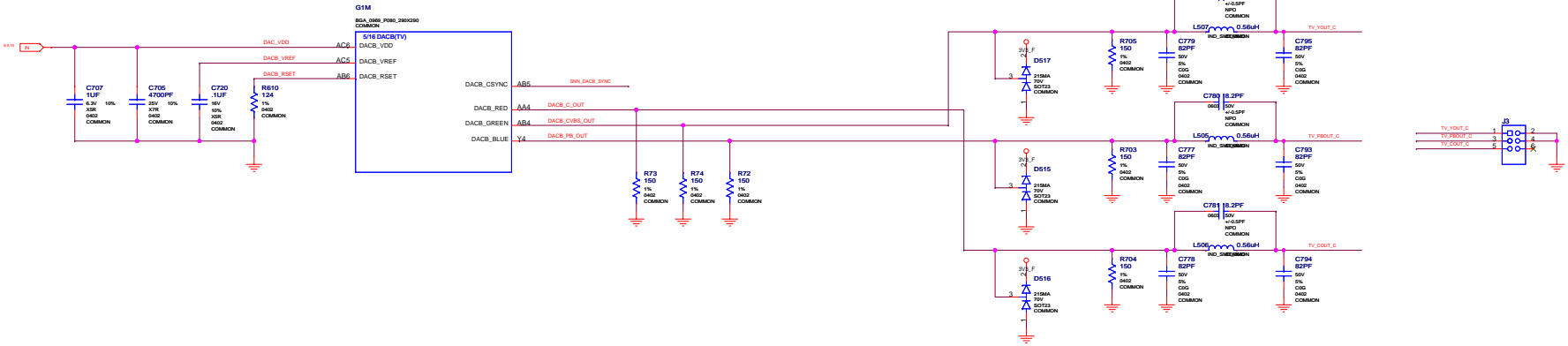
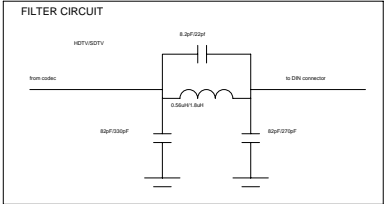
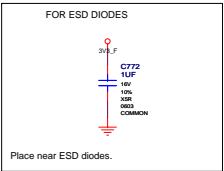
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB SLI CONNECTOR

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DACB: SD/HD VIDEO OUT CONNECTOR

NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
DACB_C_OUT		75OHM	1
DACB_CVBS_OUT		75OHM	1
DACB_PB_OUT		75OHM	1
TV_PROUT_C		75OHM	1
TV_PROUT_S		75OHM	1
TV_PROUT_E		75OHM	1
DACB_VREF	100M		
DACB_RESET	100M		



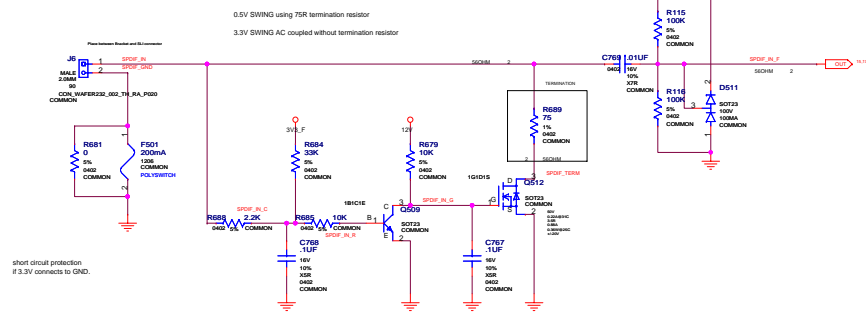
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 100FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTER, MINOR CONNECTOR NORTH, SD/HD VIDEO OUTPUT CONNECTOR

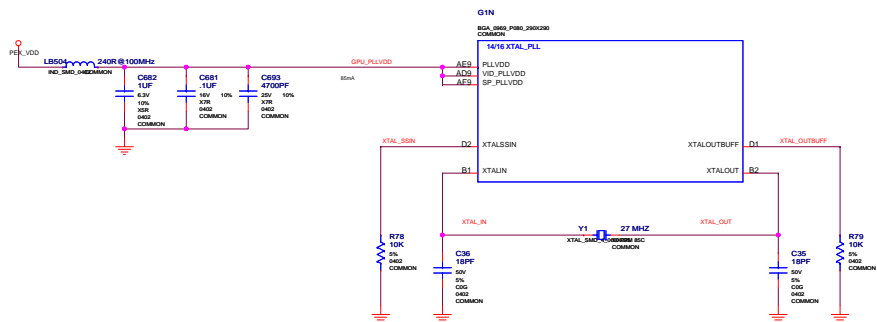
NVIDIA CORPORATION		3701 SAN TOMAS EXPRESSWAY	
		SANTA CLARA, CA 95050, USA	
NV_PN	600-10727-base-sch A	DATE	31-OCT-2007
NAME		DATE	

XTAL/PLLVD/SPDIF IN

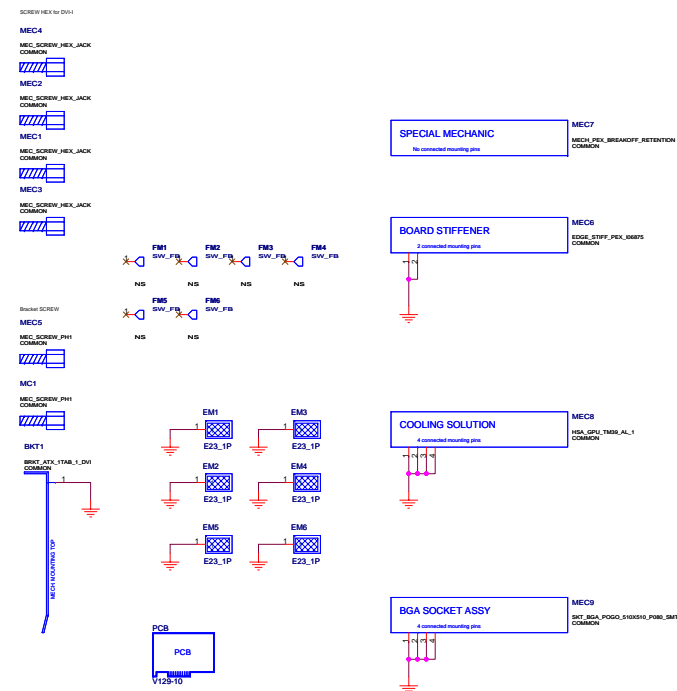
SPDIF IN



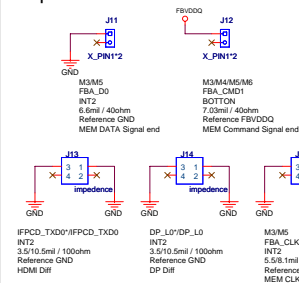
XTAL/GPU_PLLVDD



MECHANICALS & THERMALS



Impedance control line



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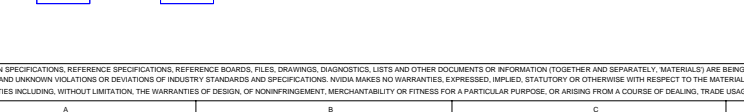
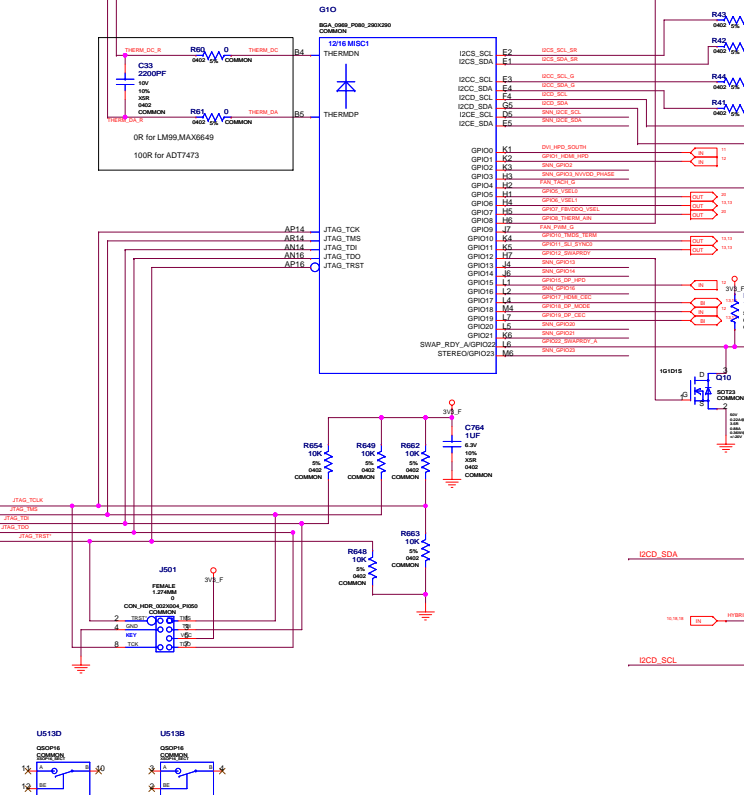
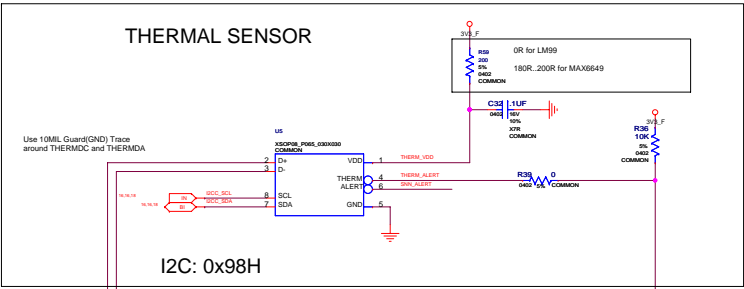
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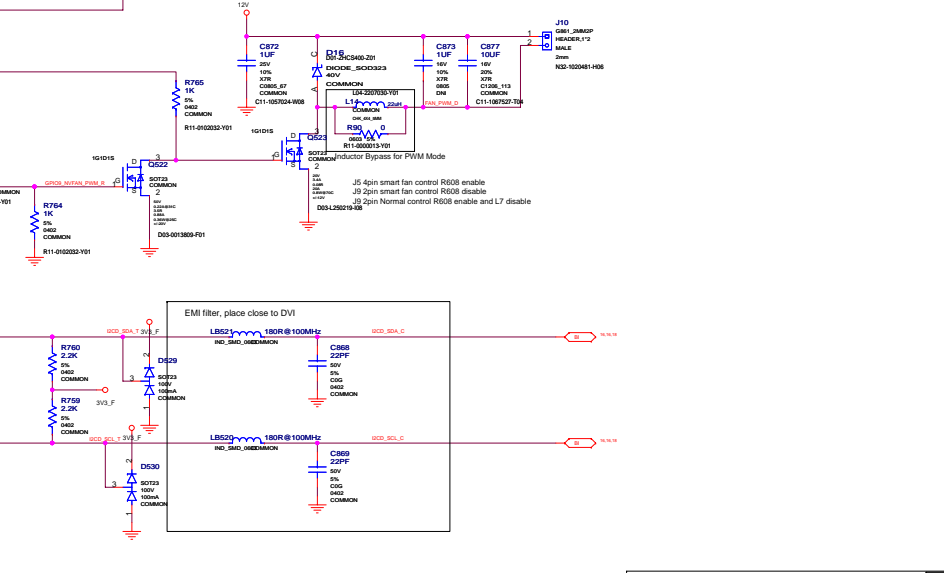
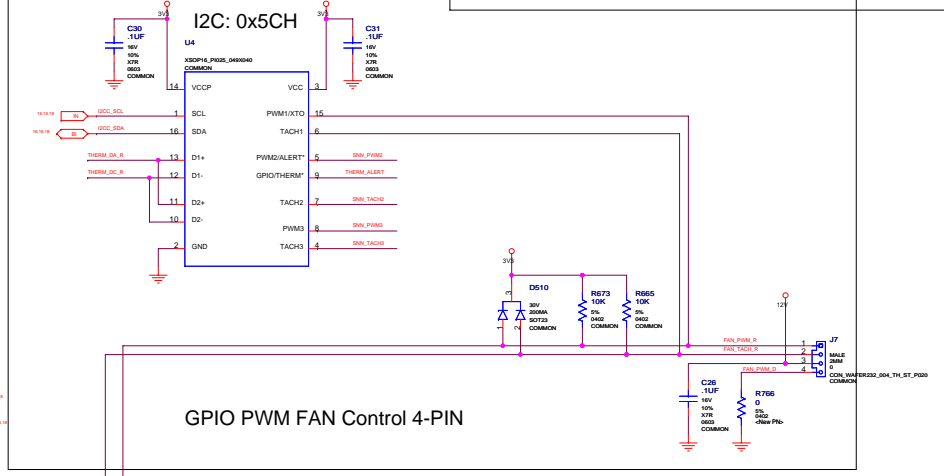
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPOD-IN, XTAL, MECHANICALS, THERMALS

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THERMAL SENSOR, FAN CONTROLLER
uses 3V3: always on.



NETNAME	MIN_LINE_WIDTH	VOLTAGE
THERM_DC	10MIL	3.3V
THERM_ALERT	10MIL	3.3V
THERM_ALERT_N	10MIL	3.3V
THERM_ALERT_N	10MIL	3.3V
THERM_ALERT_N	10MIL	3.3V
THERM_ALERT_N	10MIL	3.3V

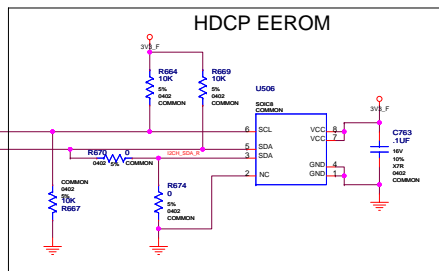
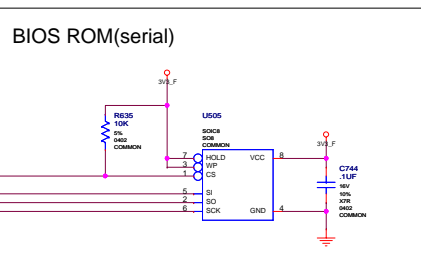
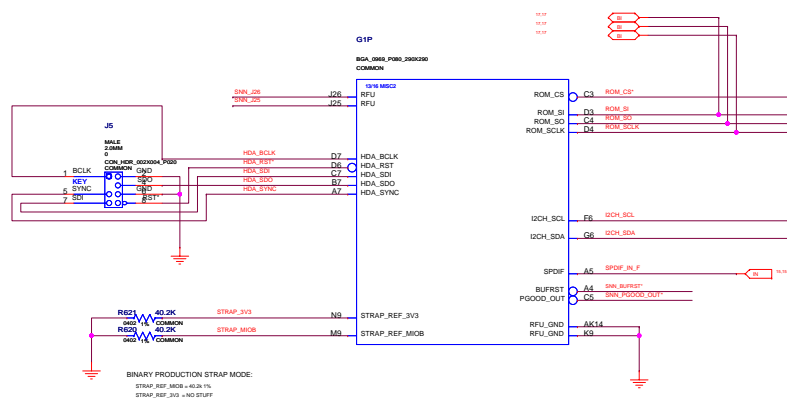
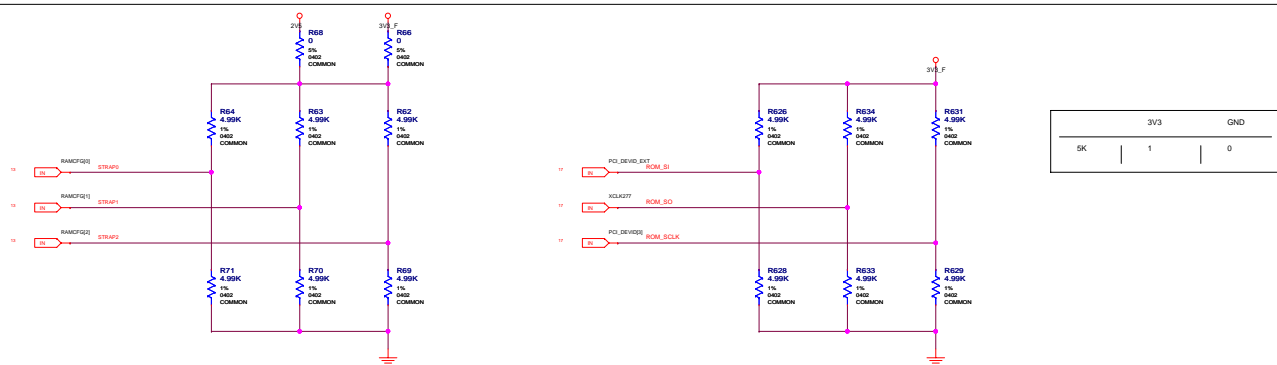
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 310FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	EXTERNAL THERMAL SENSOR, 4-PIN FAN CONTROL, GPIO

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STRAPPING OPTIONS

Assembly: BIOS



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

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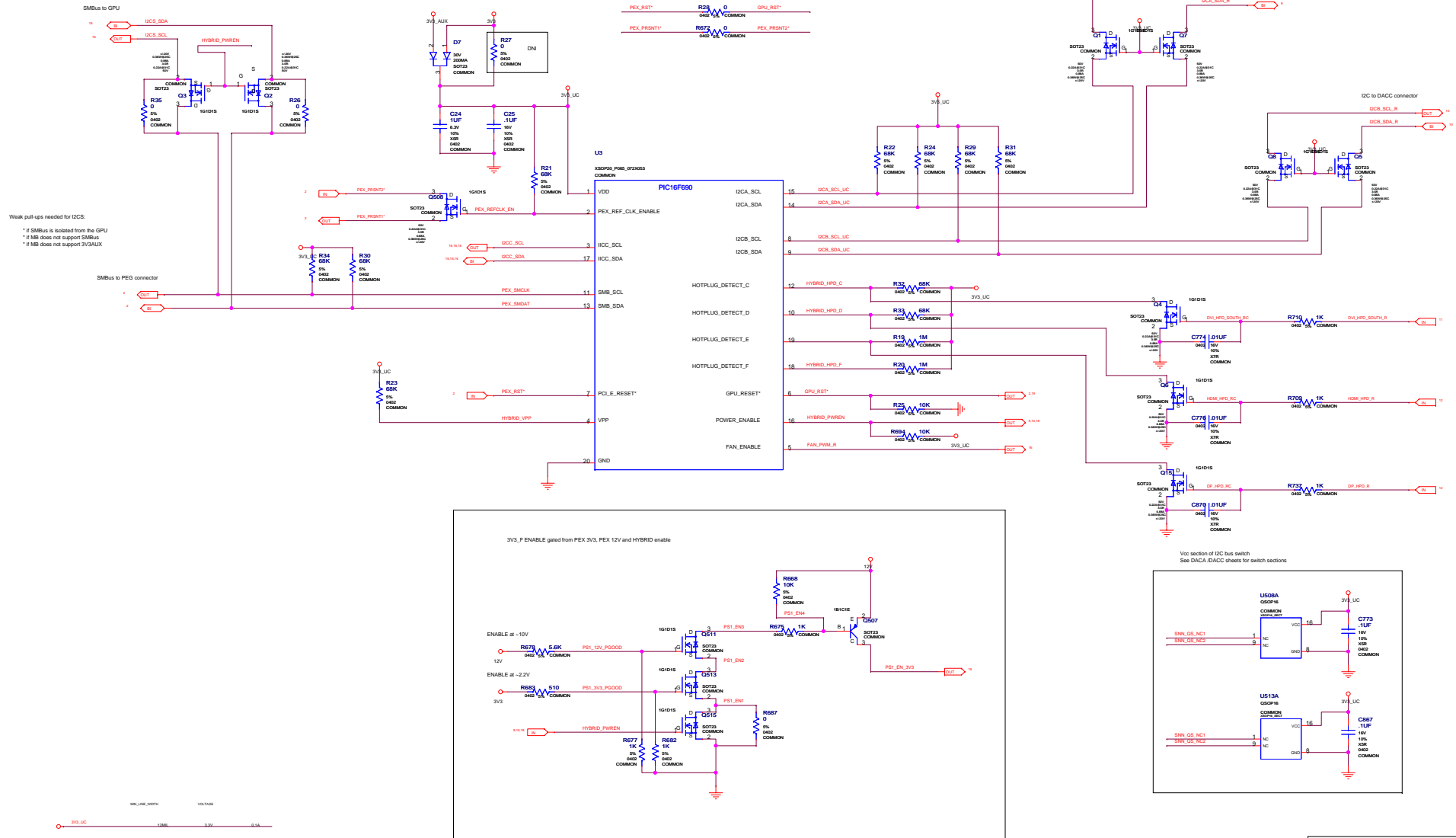
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HYBRID POWER

Per Datasheet:

Vf = 400mV at 10mA
* expected current < 2mA

Stuff only to bypass the micro-controller



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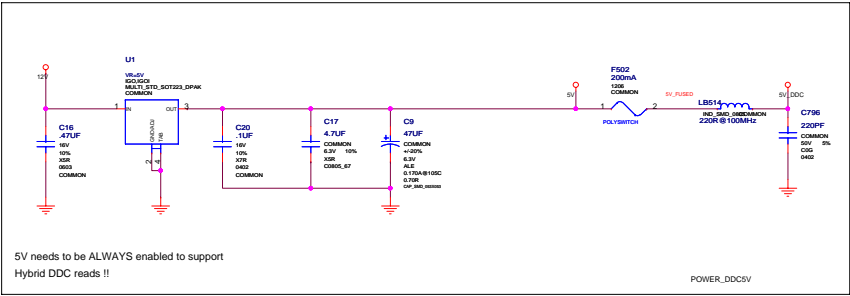
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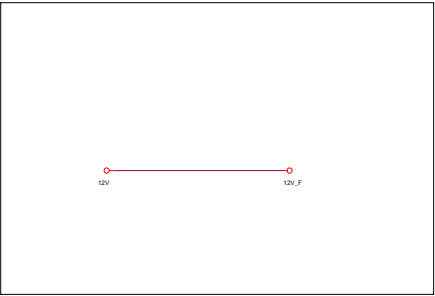
Power Supply: 5V, 5V_DDC, TMD5, MIOA_VDDQ

5V REGULATOR

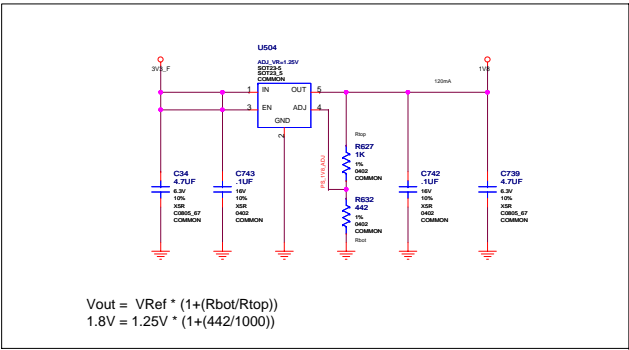


5V DDC

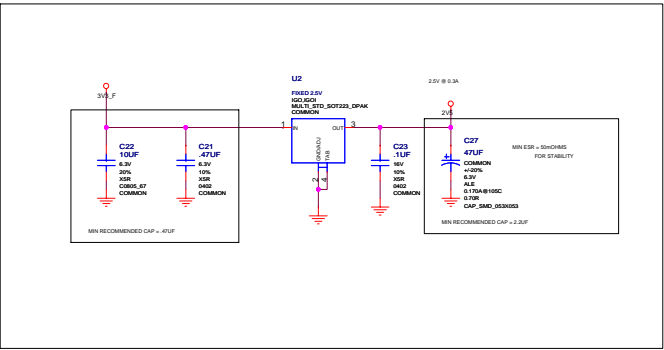
12V filter



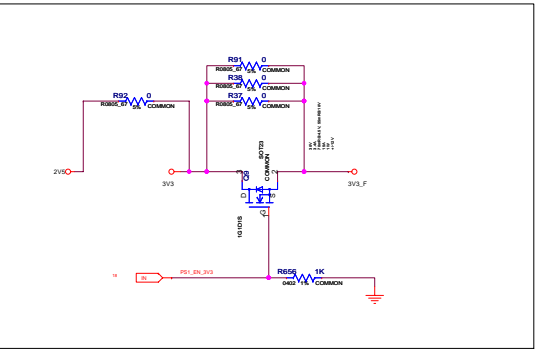
IFP PLL Supply 1.8V



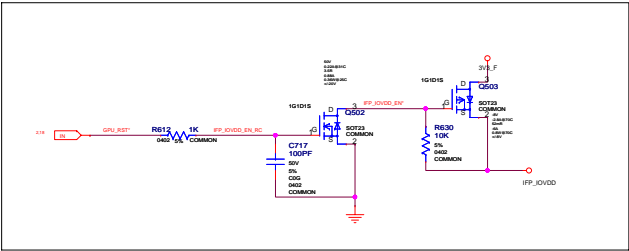
MIO_VDD 2.5V



3V3 switch



IFP_IOVDD BACKDRIVE PREVENTION



FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3

1

2

3

4

5

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FBA Partition		
136BGA CMD Mapping		
CMD	ADDR	
CMD01	BA0*	
CMD02	CAS	
CMD03	WE*	
CMD04	CS	
CMD05	BA1	
CMD06	BA2	
CMD07	BA3	
CMD08	BA4	
CMD09	BA5	
CMD10	BA6	
CMD11	BA7	
CMD12	BA8	
CMD13	BA9	
CMD14	BA10	
CMD15	BA11	
CMD16	BA12	
CMD17	BA13	
CMD18	BA14	
CMD19	BA15	
CMD20	BA16	
CMD21	BA17	
CMD22	BA18	
CMD23	BA19	
CMD24	BA20	
CMD25	BA21	
CMD26	BA22	
CMD27	BA23	

NET		DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
1	FBA_CMD01	FBA_CMD01	800PT	1
2	FBA_CMD02	FBA_CMD02	800PT	1
3	FBA_CMD03	FBA_CMD03	800PT	1
4	FBA_CMD04	FBA_CMD04	800PT	1
5	FBA_CMD05	FBA_CMD05	800PT	1
6	FBA_CMD06	FBA_CMD06	800PT	1
7	FBA_CMD07	FBA_CMD07	800PT	1
8	FBA_CMD08	FBA_CMD08	800PT	1
9	FBA_CMD09	FBA_CMD09	800PT	1
10	FBA_CMD10	FBA_CMD10	800PT	1
11	FBA_CMD11	FBA_CMD11	800PT	1
12	FBA_CMD12	FBA_CMD12	800PT	1
13	FBA_CMD13	FBA_CMD13	800PT	1
14	FBA_CMD14	FBA_CMD14	800PT	1
15	FBA_CMD15	FBA_CMD15	800PT	1
16	FBA_CMD16	FBA_CMD16	800PT	1
17	FBA_CMD17	FBA_CMD17	800PT	1
18	FBA_CMD18	FBA_CMD18	800PT	1
19	FBA_CMD19	FBA_CMD19	800PT	1
20	FBA_CMD20	FBA_CMD20	800PT	1
21	FBA_CMD21	FBA_CMD21	800PT	1
22	FBA_CMD22	FBA_CMD22	800PT	1
23	FBA_CMD23	FBA_CMD23	800PT	1
24	FBA_CMD24	FBA_CMD24	800PT	1
25	FBA_CMD25	FBA_CMD25	800PT	1
26	FBA_CMD26	FBA_CMD26	800PT	1
27	FBA_CMD27	FBA_CMD27	800PT	1
28	FBA_CMD28	FBA_CMD28	800PT	1
29	FBA_CMD29	FBA_CMD29	800PT	1
30	FBA_CMD30	FBA_CMD30	800PT	1
31	FBA_CMD31	FBA_CMD31	800PT	1
32	FBA_CMD32	FBA_CMD32	800PT	1
33	FBA_CMD33	FBA_CMD33	800PT	1
34	FBA_CMD34	FBA_CMD34	800PT	1
35	FBA_CMD35	FBA_CMD35	800PT	1
36	FBA_CMD36	FBA_CMD36	800PT	1
37	FBA_CMD37	FBA_CMD37	800PT	1
38	FBA_CMD38	FBA_CMD38	800PT	1
39	FBA_CMD39	FBA_CMD39	800PT	1
40	FBA_CMD40	FBA_CMD40	800PT	1
41	FBA_CMD41	FBA_CMD41	800PT	1
42	FBA_CMD42	FBA_CMD42	800PT	1
43	FBA_CMD43	FBA_CMD43	800PT	1
44	FBA_CMD44	FBA_CMD44	800PT	1
45	FBA_CMD45	FBA_CMD45	800PT	1
46	FBA_CMD46	FBA_CMD46	800PT	1
47	FBA_CMD47	FBA_CMD47	800PT	1
48	FBA_CMD48	FBA_CMD48	800PT	1
49	FBA_CMD49	FBA_CMD49	800PT	1
50	FBA_CMD50	FBA_CMD50	800PT	1
51	FBA_CMD51	FBA_CMD51	800PT	1
52	FBA_CMD52	FBA_CMD52	800PT	1
53	FBA_CMD53	FBA_CMD53	800PT	1
54	FBA_CMD54	FBA_CMD54	800PT	1
55	FBA_CMD55	FBA_CMD55	800PT	1
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59	FBA_CMD59	FBA_CMD59	800PT	1
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71	FBA_CMD71	FBA_CMD71	800PT	1
72	FBA_CMD72	FBA_CMD72	800PT	1
73	FBA_CMD73	FBA_CMD73	800PT	1
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76	FBA_CMD76	FBA_CMD76	800PT	1
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81	FBA_CMD81	FBA_CMD81	800PT	1
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83	FBA_CMD83	FBA_CMD83	800PT	1
84	FBA_CMD84	FBA_CMD84	800PT	1
85	FBA_CMD85	FBA_CMD85	800PT	1
86	FBA_CMD86	FBA_CMD86	800PT	1
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88	FBA_CMD88	FBA_CMD88	800PT	1
89	FBA_CMD89	FBA_CMD89	800PT	1
90	FBA_CMD90	FBA_CMD90	800PT	1
91	FBA_CMD91	FBA_CMD91	800PT	1
92	FBA_CMD92	FBA_CMD92	800PT	1
93	FBA_CMD93	FBA_CMD93	800PT	1
94	FBA_CMD94	FBA_CMD94	800PT	1
95	FBA_CMD95	FBA_CMD95	800PT	1
96	FBA_CMD96	FBA_CMD96	800PT	1
97	FBA_CMD97	FBA_CMD97	800PT	1
98	FBA_CMD98	FBA_CMD98	800PT	1
99	FBA_CMD99	FBA_CMD99	800PT	1
100	FBA_CMD100	FBA_CMD100	800PT	1

Termination for Sub-Partition and CLK MUST BE PLACED as close as possible to the BGA memory on the line BEFORE the MEMORY pin! Minimize the stub length!

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id

page

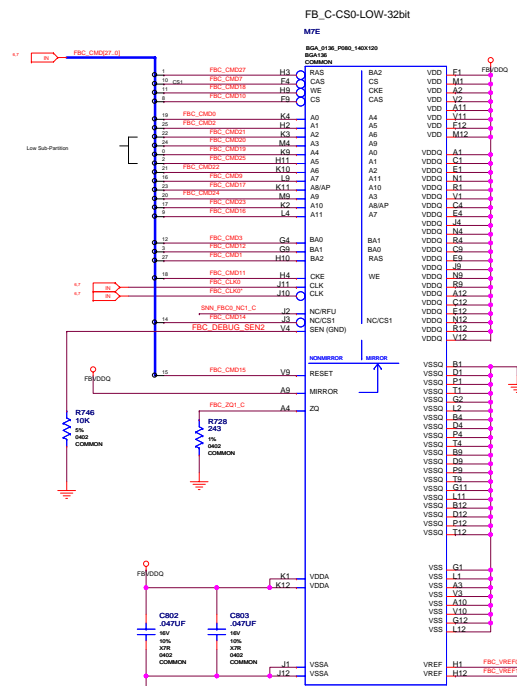
name

date

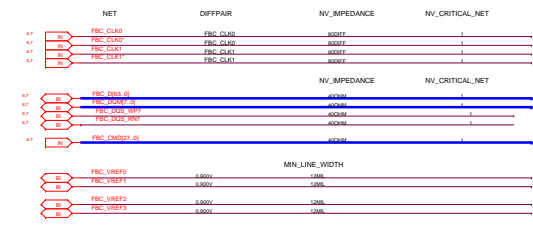
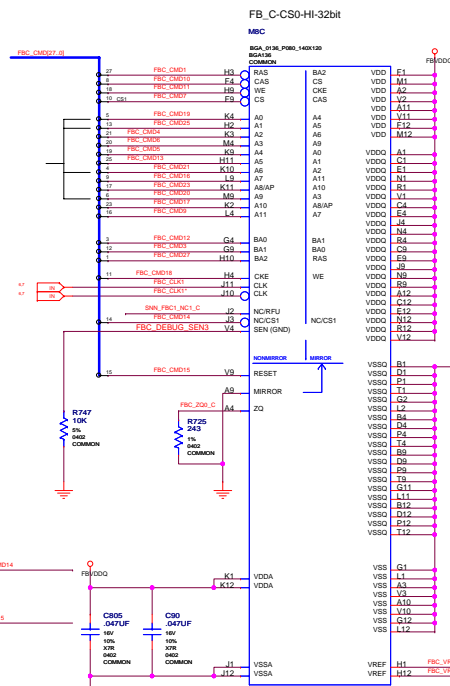
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ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL: FBA 16/32Mx32 GDDR3 MEMORIES, FBA COMMAND BUS P0/FBA CLK TERMS

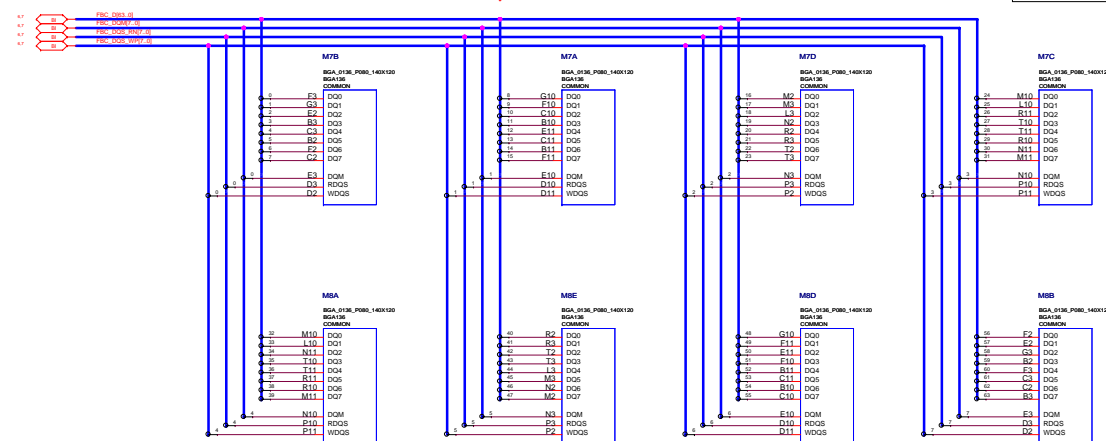
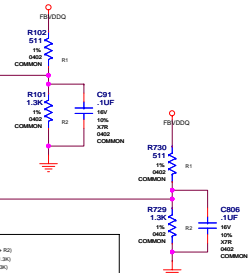
FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3



FBC Partition			CSD
CMD	ADDR		
CMD01	R40*		
CMD02	C40*		
CMD11	WE*		
CMD18	CKE		
CMD19	RESET/ODT		
CMD6	CS0*		
CMD19	A0-0		
CMD05	A0-1		
CMD04	A0-2		
CMD04	A0-3		
CMD00	A0-4		
CMD03	A0-5		
CMD04	A0-6		
CMD6	A0-6		
CMD05	A0-6		
CMD03	A0-6		
CMD21	A0-6		
CMD16	A0-7		
CMD03	A0-8		
CMD20	A0-9		
CMD17	A0-10		
CMD9	A0-11		
CMD14	A0-12		
CMD12	BA0		
CMD3	BA1		
CMD27	BA2		



Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS P/U'S, FBC CLK TERMS

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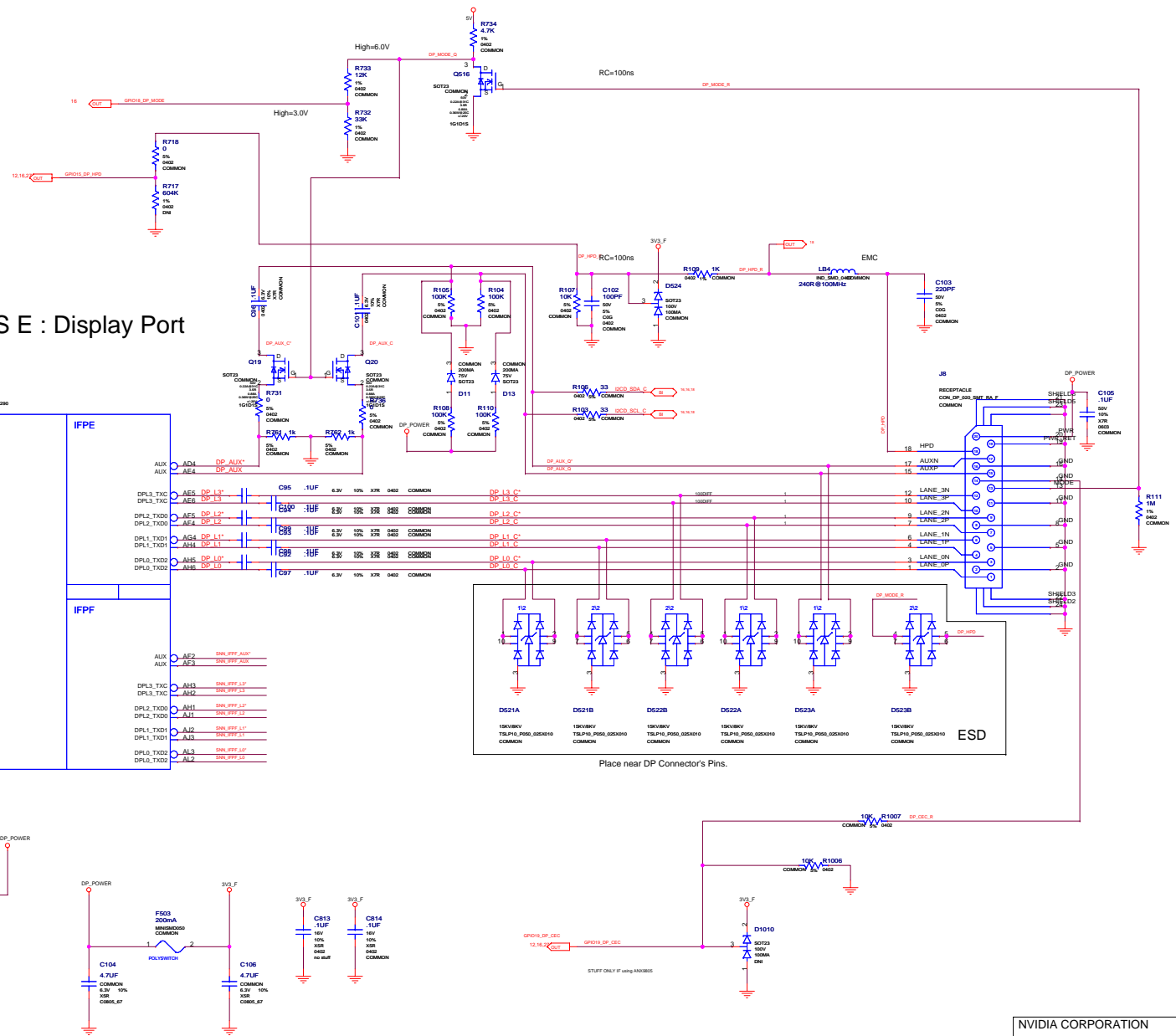


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TMDS LINK: E & F

TMDS E : Display Port



Place near DP Connector's Pins.

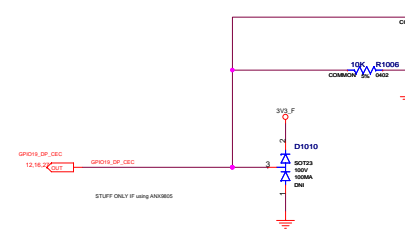
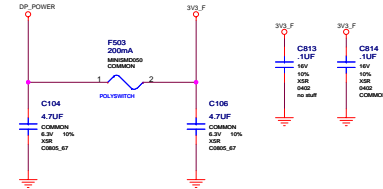
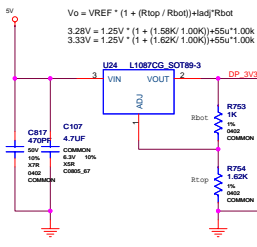
5V

$$V_O = V_{REF} * (1 + (R_{top} / R_{bot})) + I_{adj} * R_{bot}$$

$$3.28V = 1.25V * (1 + (158K / 1.00K)) + 55\mu * 1.00k$$

$$3.33V = 1.25V * (1 + (162K / 1.00K)) + 55\mu * 1.00k$$

U04 - LM333C, SO28-3



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMD5 LINK C/D, AC COUPLING, PD's, DVI CONNECTOR MID

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