

V034-1A NV44 128 MB DDR2, VGA, DVI-I, SD/HDTV

HISTORY

0A base on v001 1.1 modify  
removed TSOP-66 DDR change to BGA-84 DDR2.  
add 2nd RT9218 for FBVDD/Q.  
add APL5331 for FBVTT.  
10 removed RT9218 and VTT.  
add op+mos circuit.  
and cost down 0402 parts change to 0603.  
11 pin header change to box header for samsung request.

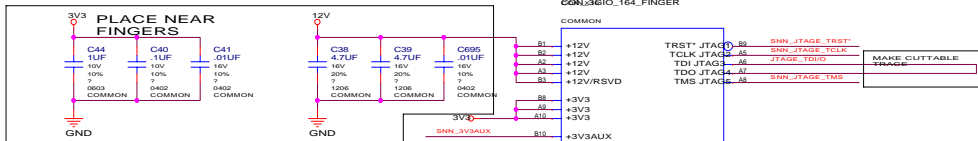
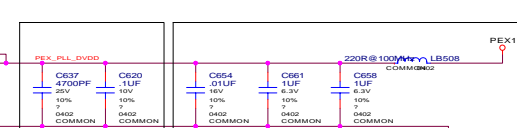
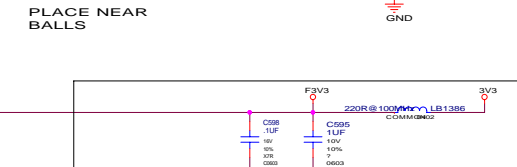
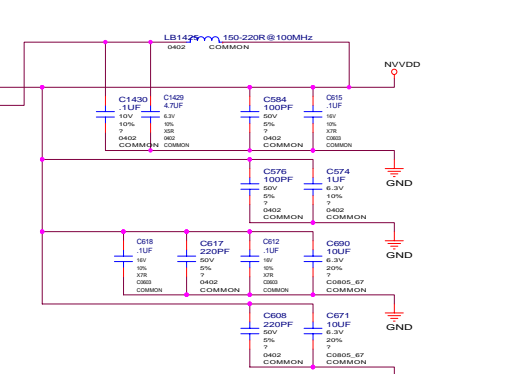
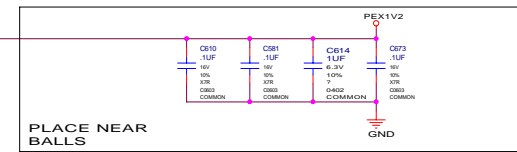
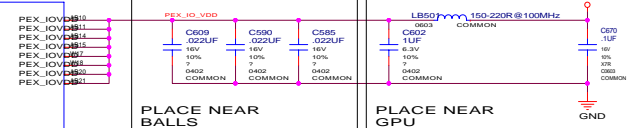
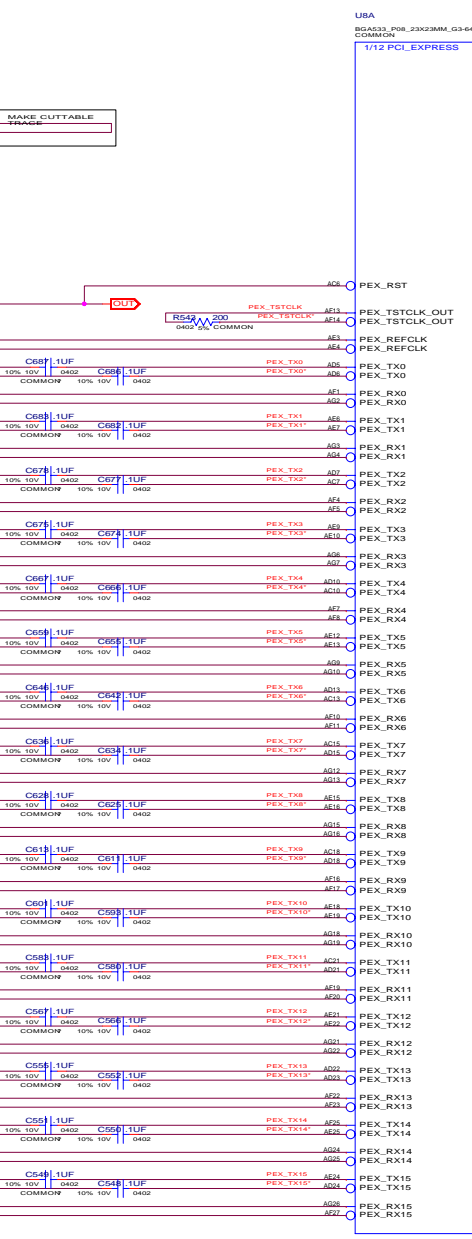
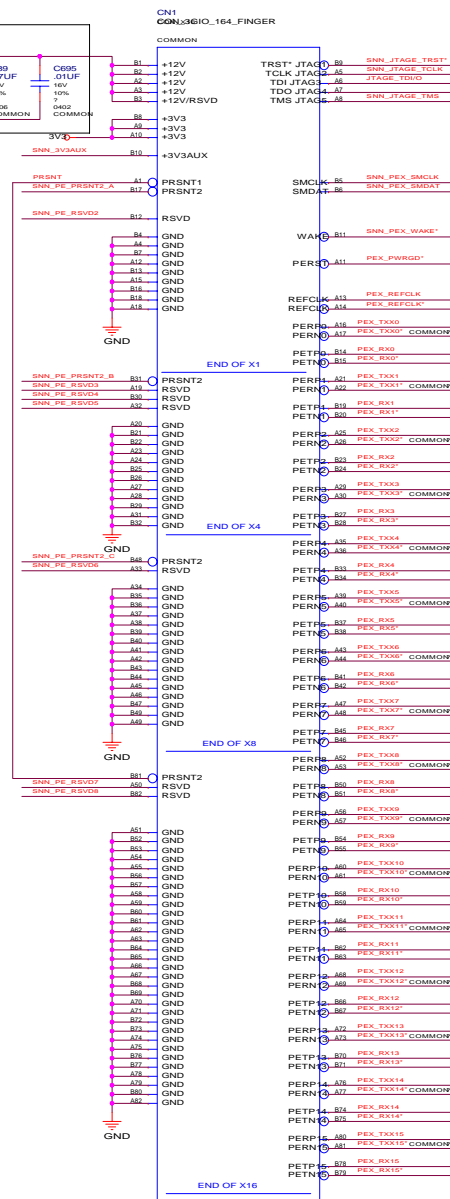
- 01. Cover page
- 02. PEX interface
- 03. GPU FB-interface
- 04. MEMORY Bit 0..31
- 05. MEMORY Bit 32..64
- 06. DAC-A, DB15 Con.
- 07. DAC-B, MUX, DB15
- 08. Internal TMDS
- 09. MIOA, MIOB
- 10. Straps
- 11. BIOS, GPIO, FAN Con.
- 12. Mini DIN
- 13. Power :NVVDD/FBVDD
- 14. Power others

A01

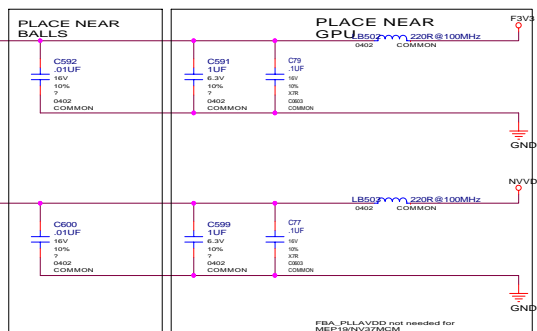
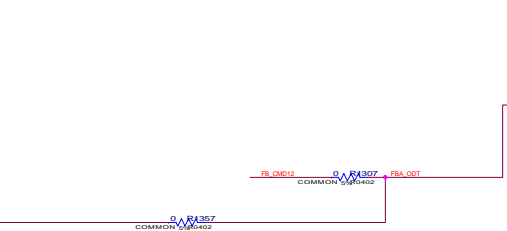
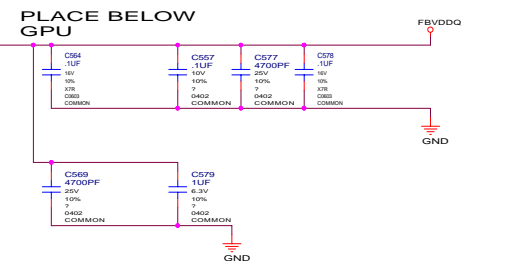
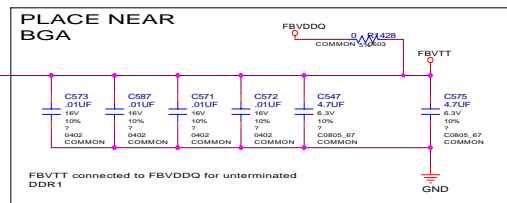
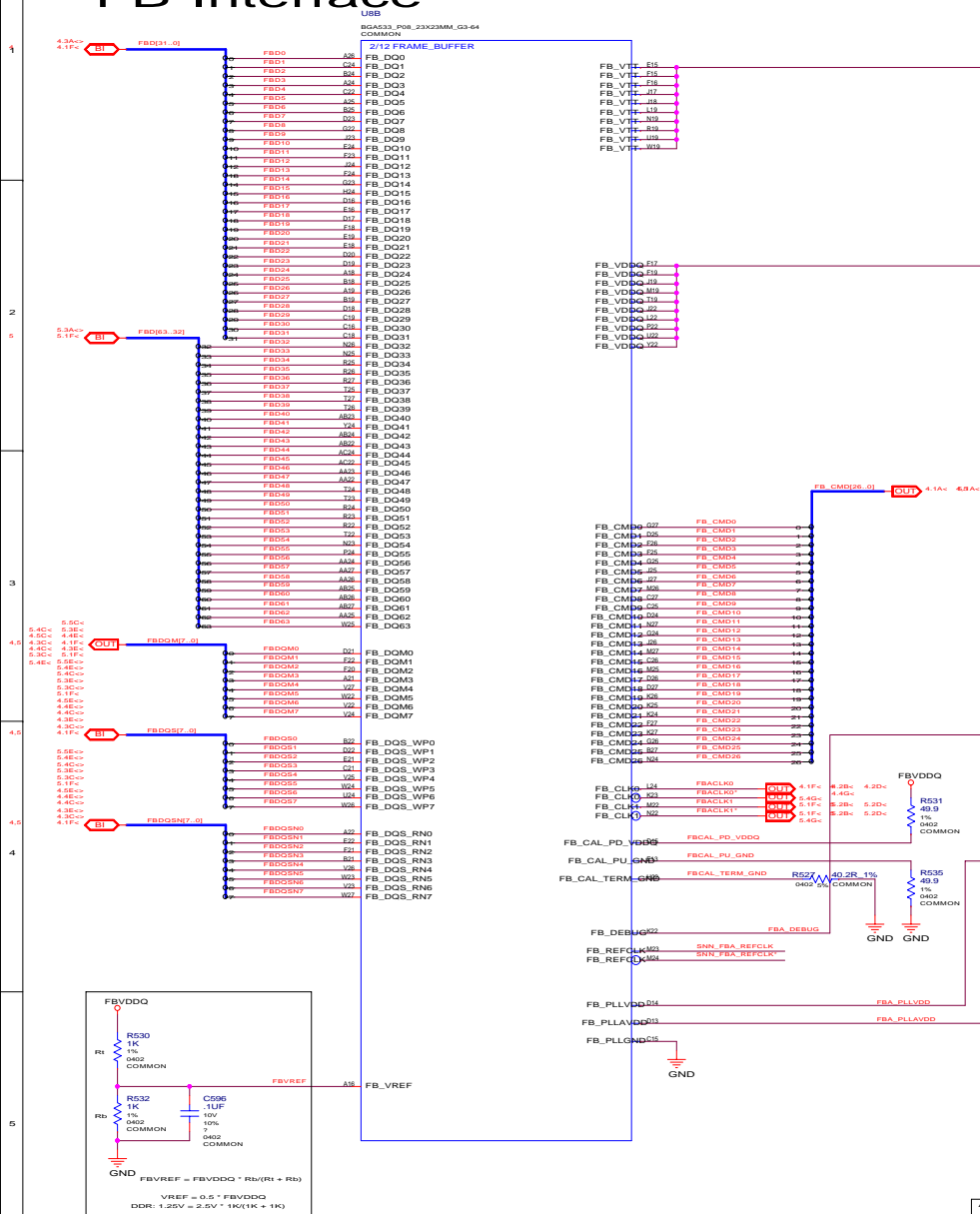
- 9/22/2004:
  - Changed TMDS\_PLLVDD to PLLVDD
  - Added bead option to PLLVDD rail of NV44
  - Changed RSET values for DACA and DACB
  - Changed DACB RSET FET to a dual package with GPIO11 control-Macrovision
  - Added F3V3 bypass to PLLVDD linear regulator
  - Changed location of R62

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10262-0000-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
1	0000	600-10262-0000-000	AND NOT FINAL
2	0001	600-10262-0001-000	<UNDEFINED>
3	0002	600-10262-0002-000	<UNDEFINED>
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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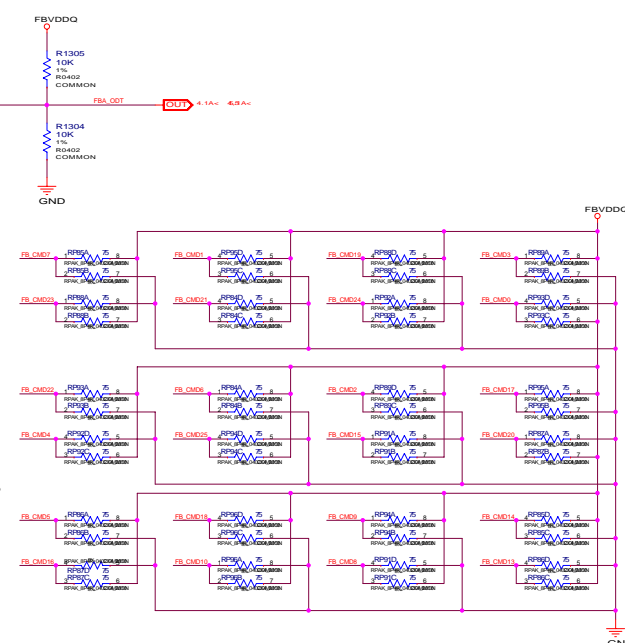
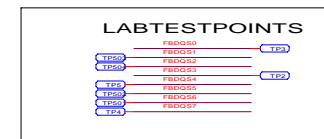
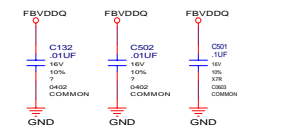
# PEX-Interface

[illegible]

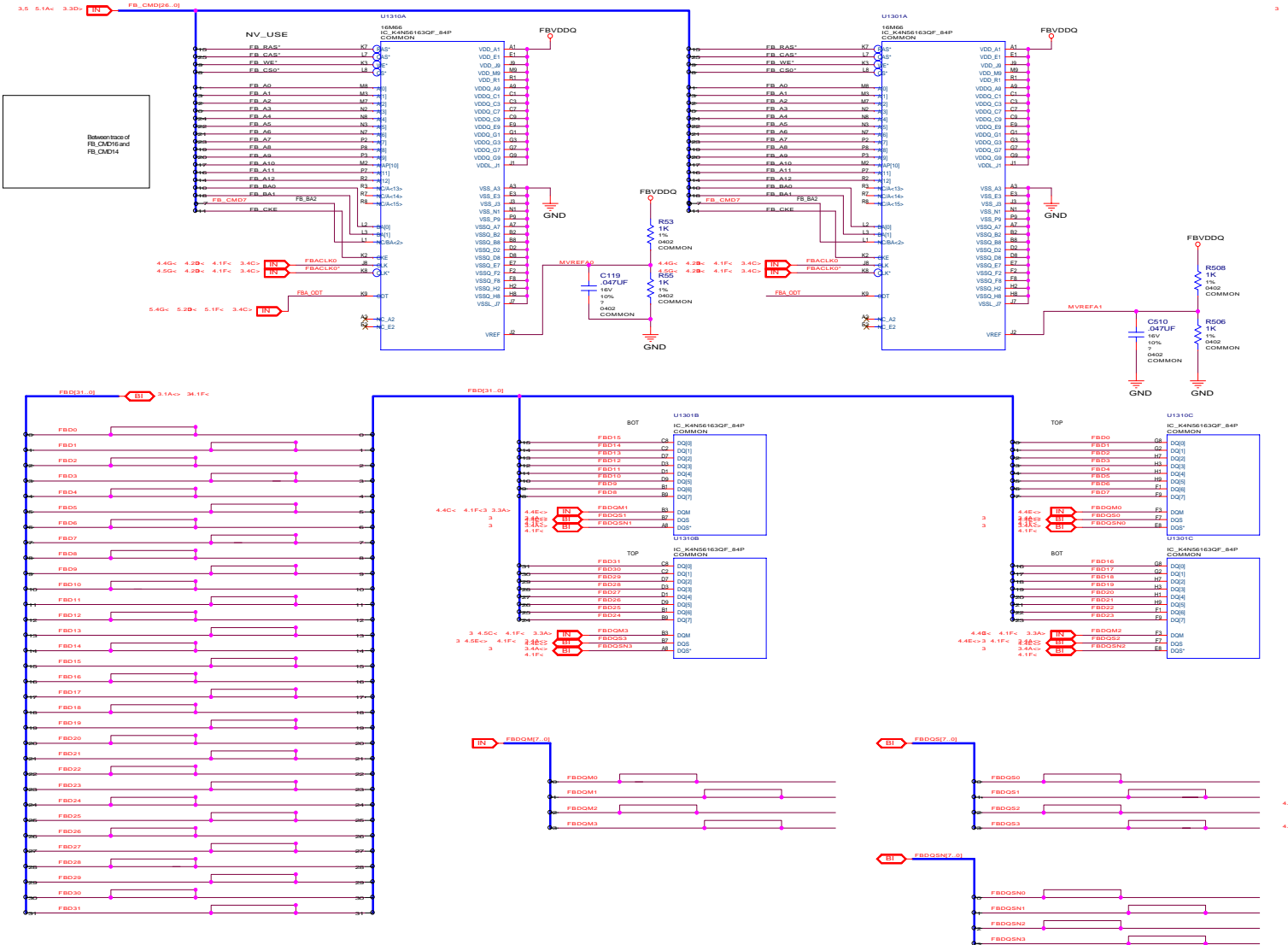
## GPU: FB-Interface



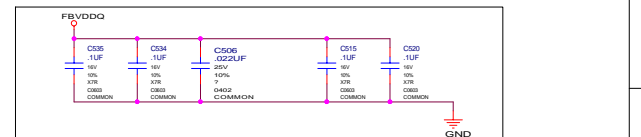
IN	Net Name	NET_SPACING_RULE
IN	FBCAL_PU_GND	1.0MIL
IN	FBCAL_TERM_GND	1.0MIL
IN	FB_DLLVDD	1.0MIL
IN	FBA_PLLAVDD	1.0MIL
IN	FBVREF	1.0MIL



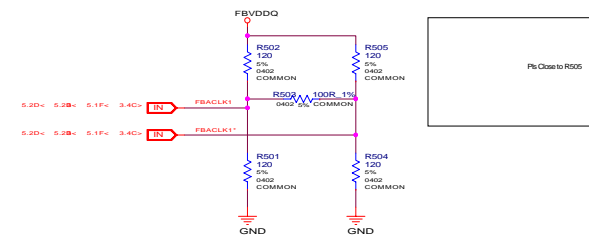
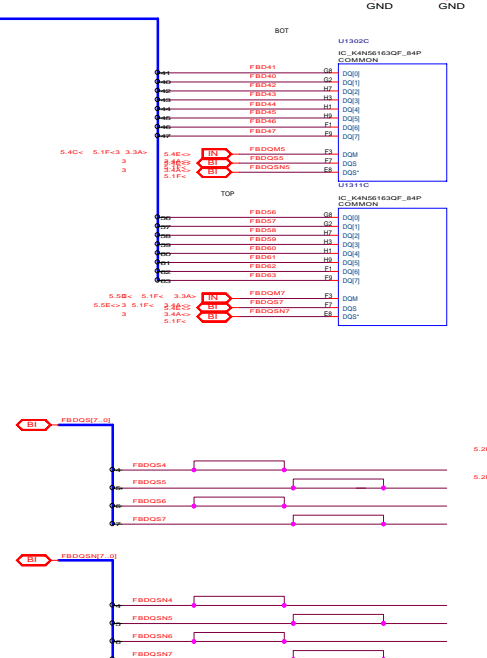
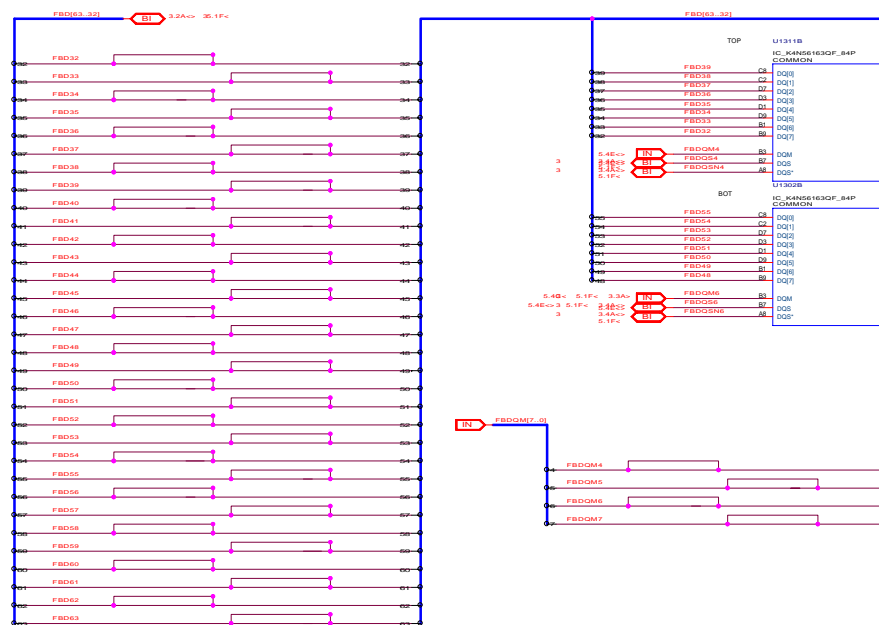
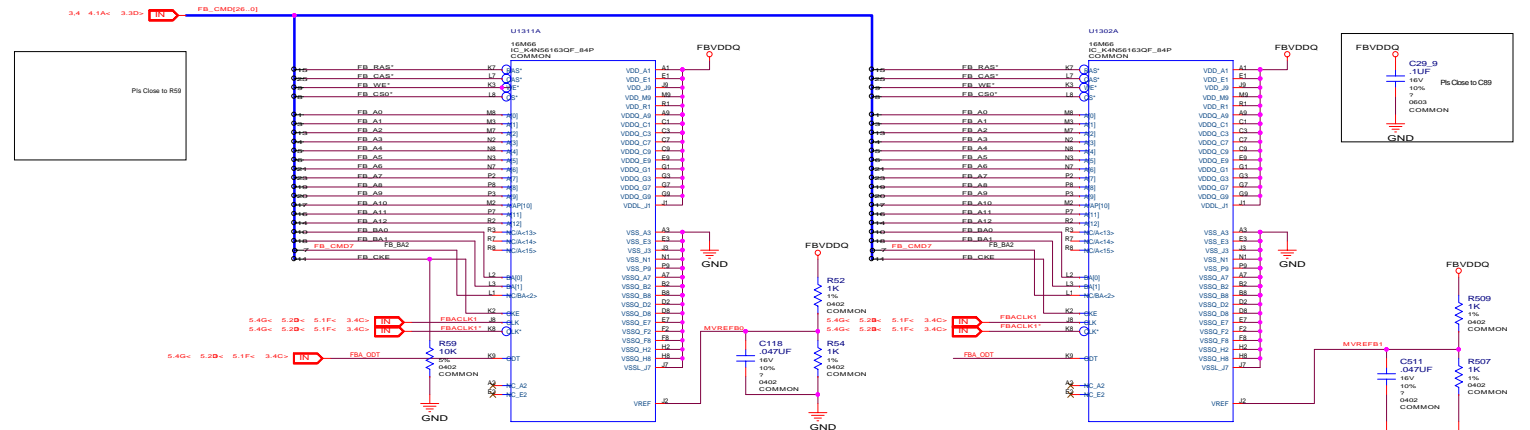
# Memory Bit 0..31



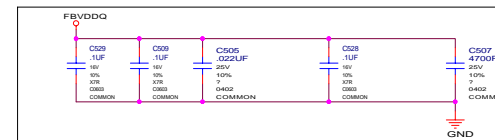
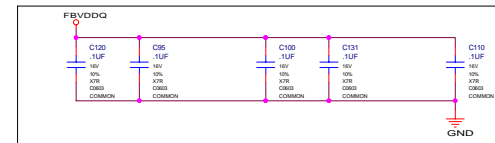
Net	Diffpair	NET_SPACING_RULE
FB_CMD7_0	FB_CMD7_0	10MIL
FB_CMD7_1	FB_CMD7_1	10MIL
FB_CMD7_2	FB_CMD7_2	10MIL
FB_CMD7_3	FB_CMD7_3	10MIL
FB_CMD7_4	FB_CMD7_4	10MIL
FB_CMD7_5	FB_CMD7_5	10MIL
FB_CMD7_6	FB_CMD7_6	10MIL
FB_CMD7_7	FB_CMD7_7	10MIL
FB_CMD7_8	FB_CMD7_8	10MIL
FB_CMD7_9	FB_CMD7_9	10MIL
FB_CMD7_10	FB_CMD7_10	10MIL
FB_CMD7_11	FB_CMD7_11	10MIL
FB_CMD7_12	FB_CMD7_12	10MIL
FB_CMD7_13	FB_CMD7_13	10MIL
FB_CMD7_14	FB_CMD7_14	10MIL
FB_CMD7_15	FB_CMD7_15	10MIL
FB_CMD7_16	FB_CMD7_16	10MIL
FB_CMD7_17	FB_CMD7_17	10MIL
FB_CMD7_18	FB_CMD7_18	10MIL
FB_CMD7_19	FB_CMD7_19	10MIL
FB_CMD7_20	FB_CMD7_20	10MIL
FB_CMD7_21	FB_CMD7_21	10MIL
FB_CMD7_22	FB_CMD7_22	10MIL
FB_CMD7_23	FB_CMD7_23	10MIL
FB_CMD7_24	FB_CMD7_24	10MIL
FB_CMD7_25	FB_CMD7_25	10MIL
FB_CMD7_26	FB_CMD7_26	10MIL
FB_CMD7_27	FB_CMD7_27	10MIL
FB_CMD7_28	FB_CMD7_28	10MIL
FB_CMD7_29	FB_CMD7_29	10MIL
FB_CMD7_30	FB_CMD7_30	10MIL
FB_CMD7_31	FB_CMD7_31	10MIL
FB_CMD7_32	FB_CMD7_32	10MIL
FB_CMD7_33	FB_CMD7_33	10MIL
FB_CMD7_34	FB_CMD7_34	10MIL
FB_CMD7_35	FB_CMD7_35	10MIL
FB_CMD7_36	FB_CMD7_36	10MIL
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FB_CMD7_95	FB_CMD7_95	10MIL
FB_CMD7_96	FB_CMD7_96	10MIL
FB_CMD7_97	FB_CMD7_97	10MIL
FB_CMD7_98	FB_CMD7_98	10MIL
FB_CMD7_99	FB_CMD7_99	10MIL
FB_CMD7_100	FB_CMD7_100	10MIL



## Memory Bit 32..63

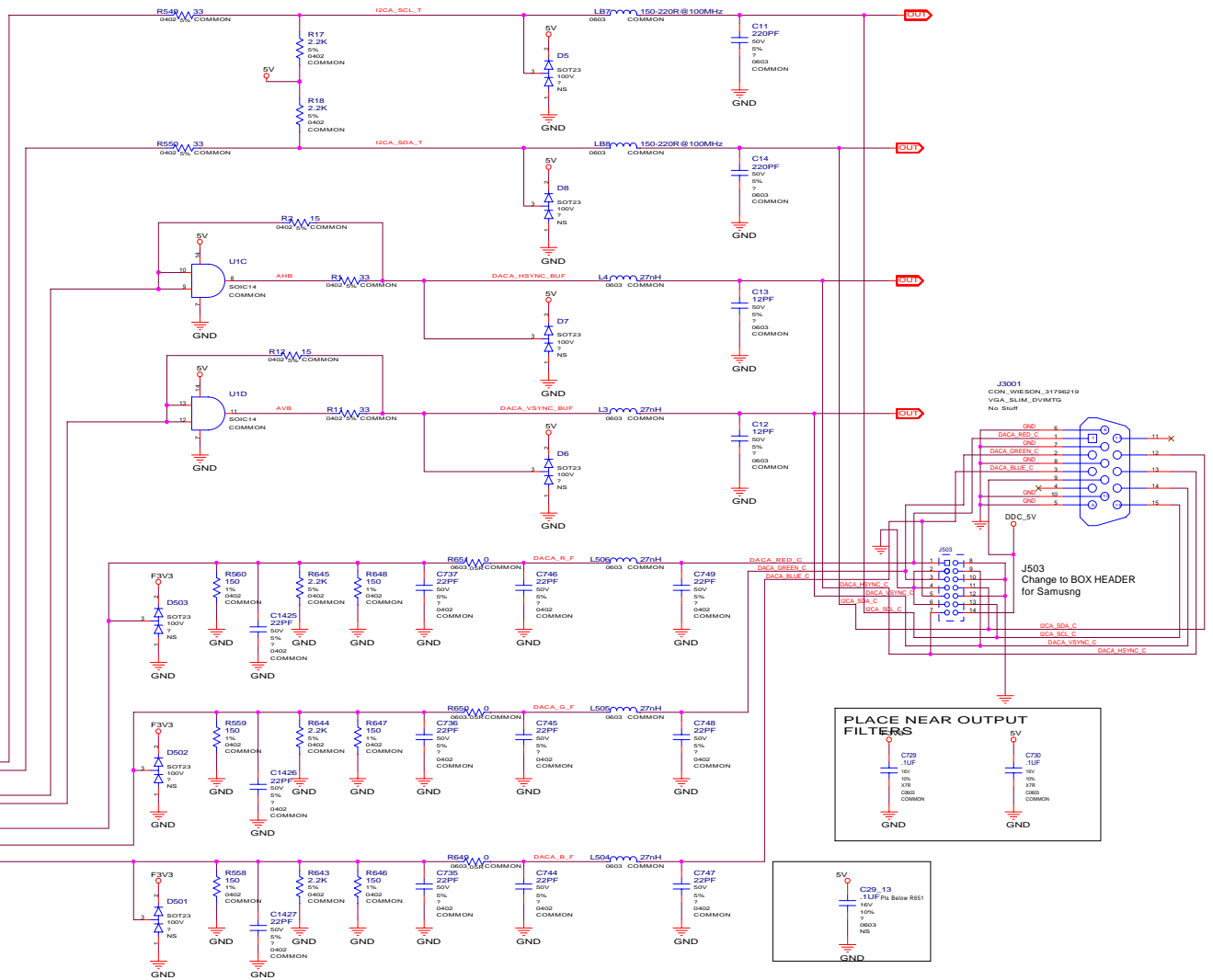
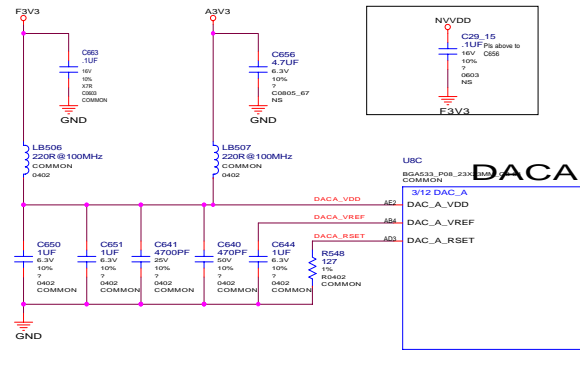
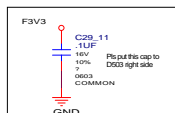
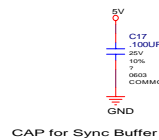


Net	Diffpair	NET_SPACING_RULE
IN	FBACKL1	25MBL
IN	FBACKL1	25MBL
IN	FRDQSR3_3I	10MBL
IN	FRDQSR7_4I	10MBL
IN	FRDQSR7_4I	10MBL
IN	FRDQSR7_4I	10MBL
IN	FRDQSR7_4I	10MBL



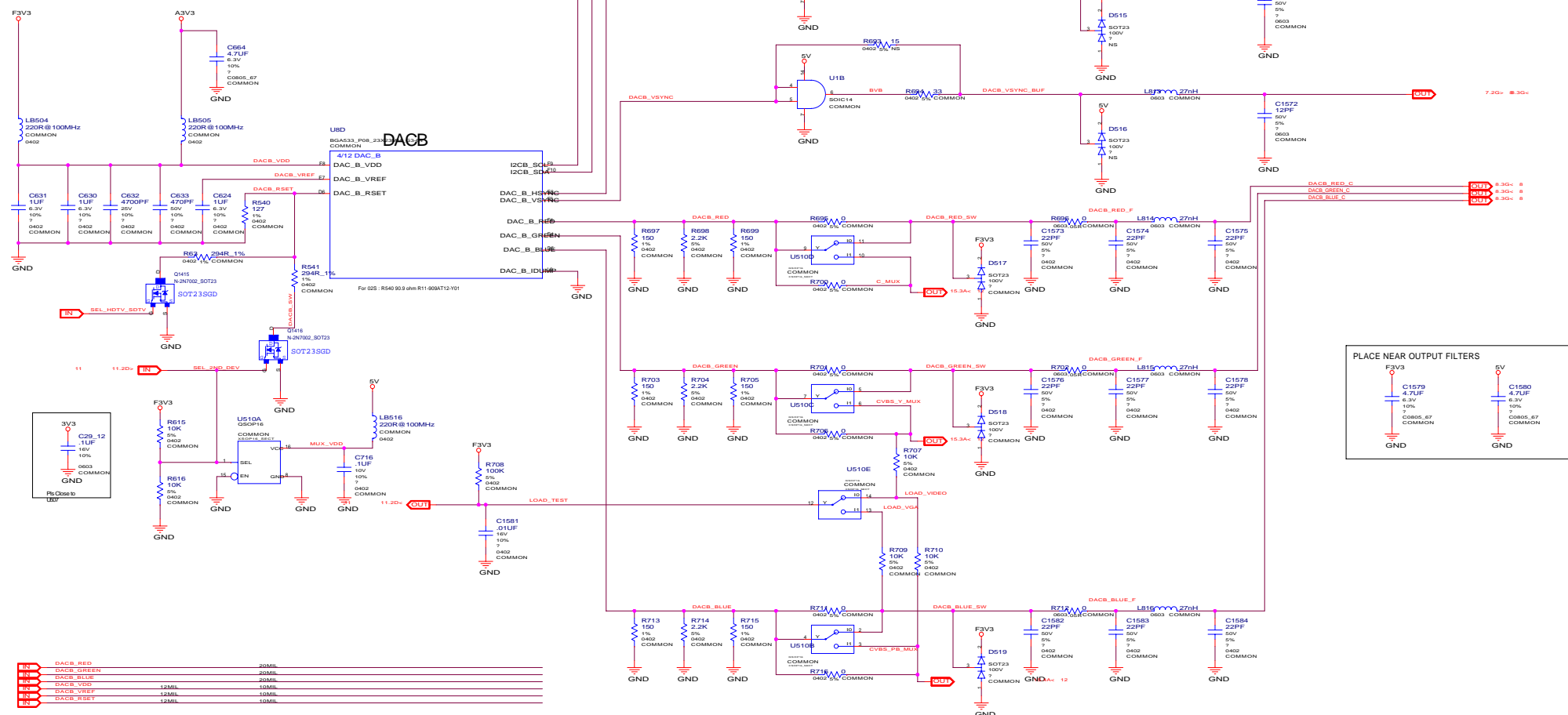
## DAC-A, DB15 Connector

Net		MIN_LINE_WIDTH=NET_SPACING_TYPE
	<b>Name</b>	
R25	DCDC_VREF	10MIL
R26	DCDC_HSVND	10MIL
R27	DCDC_VREF2	10MIL
R28	DCDC_VREF1	10MIL
R29	DCDC_GREEN	20MIL
R30	DCDC_BLUE	20MIL
R31	DCDC_VDD	12MIL
R32	DCDC_R_F	20MIL
R33	DCDC_G_F	20MIL
R34	DCDC_B_F	20MIL
R35	DCDC_RED_C	20MIL
R36	DCDC_GREEN_C	20MIL
R37	DCDC_BLUE_C	20MIL



ASSEMBLY PAGE	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM, NOT FINAL DACC, DACC, DACC, Sync
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A	B	C	D	E	F	G	H
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DAC-B, MUX,  
DB15

### PLACE NEAR OUTPUT FILTERS

Diagram illustrating the placement of electrolytic capacitors near output filters for two different voltage regulators:

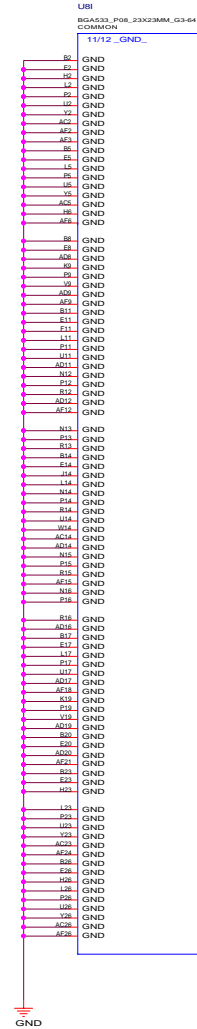
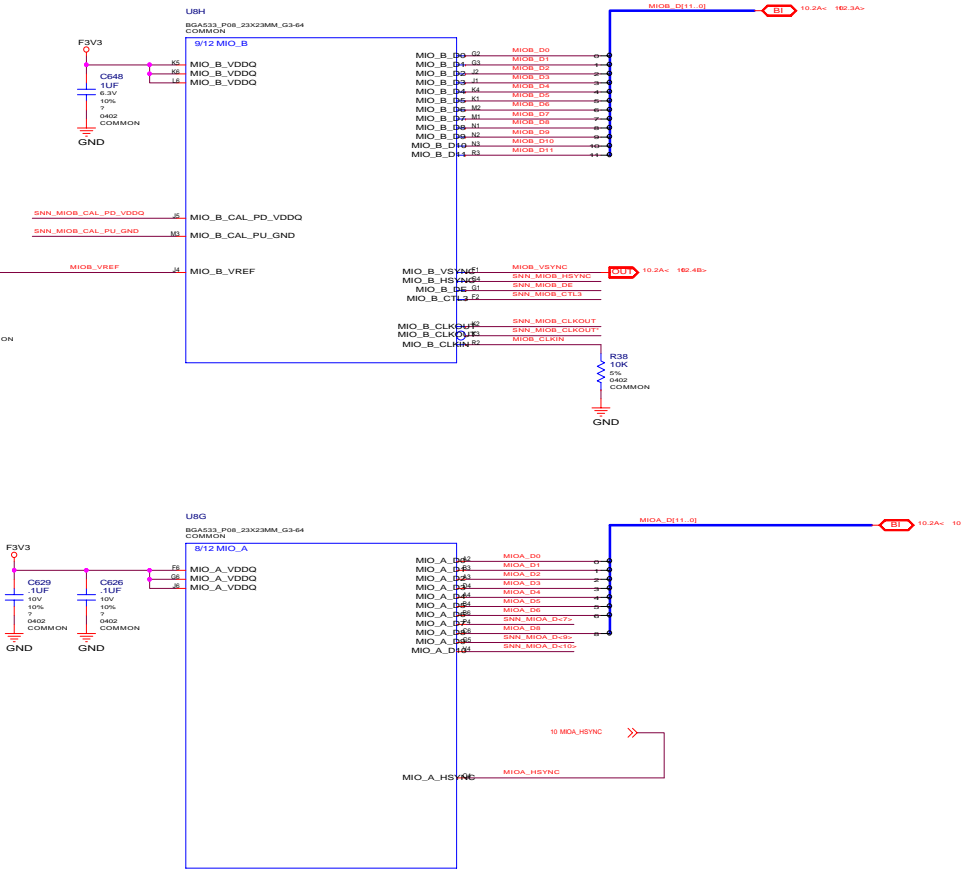
- Left Circuit (3V3):** A 3V3 regulator is connected to a 6.3V 10% electrolytic capacitor (C1579, 4.7UF) which is connected to GND. The capacitor is labeled with '7 COB05, 67 COMMON'.
- Right Circuit (5V):** A 5V regulator is connected to a 6.3V 10% electrolytic capacitor (C1580, 4.7UF) which is connected to GND. The capacitor is labeled with '7 COB05, 67 COMMON'.

IN	DACS_RED	20MIL
IN	DACS_GREEN	20MIL
IN	DACS_BLUE	20MIL
IN	DACS_VDD	12MIL
IN	DACS_VREF	10MIL
IN	DACS_RSET	10MIL





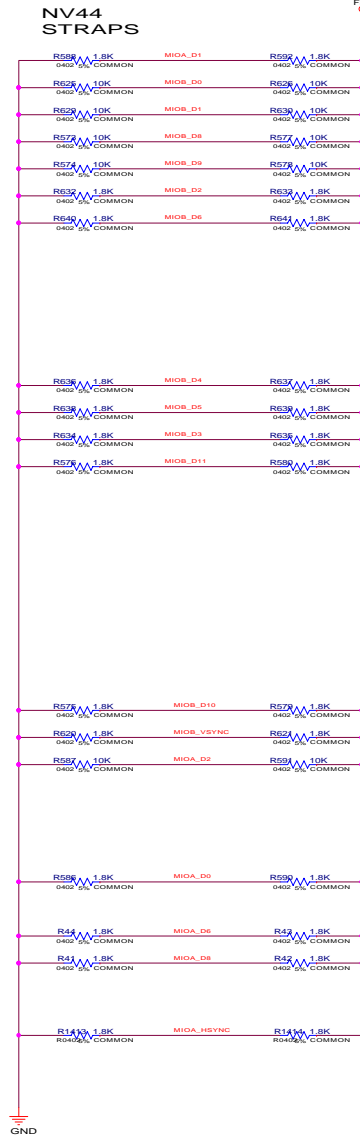
MIOA, MIOB  
Interface,  
LPC-ROM



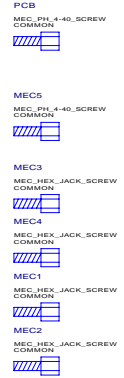
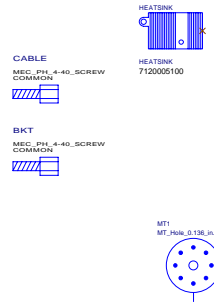
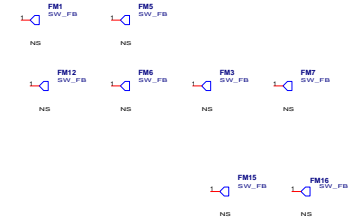
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ASSEMBLY  
PAGE  
LPC-ROM  
MIOA, MIOB Interface.

# STRAPS, Mechanical Parts

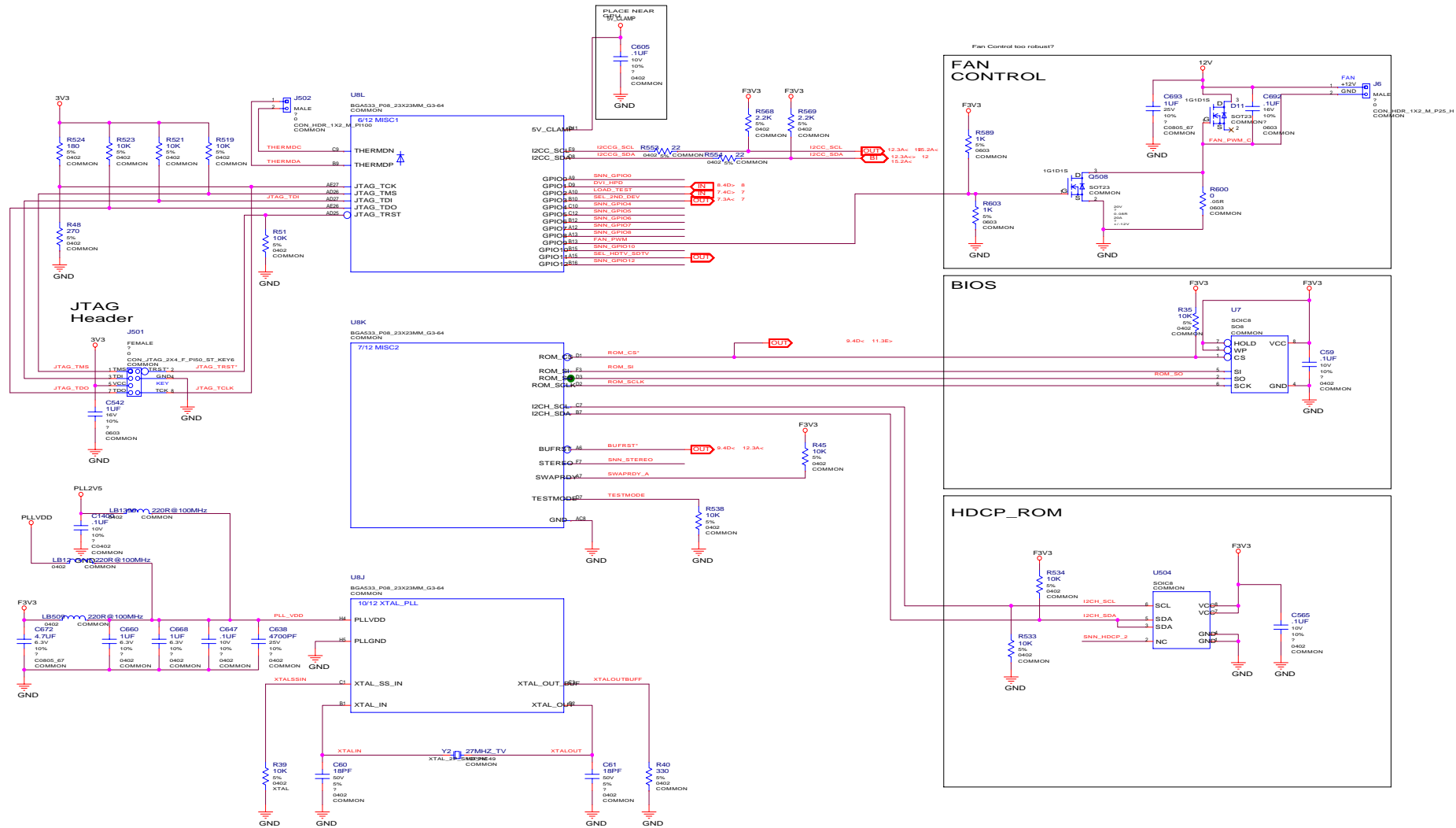


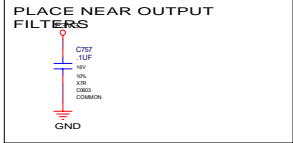
Bit	Signal	Values
00:	PCI_AD_SWAP	0 REVERSED 1 NORMAL
01:	SUBV_VENDOR	0 3.3VDC FROM 1 5.0VDC FROM
02:	RAM_CFG_0	0000 0000 0001 80Mx16DDR 0010 32GB 0011 64M 0100 160M 0101 320M 0110 640M 0111 1280M 1000 256M 1001 512M 1010 1GB 1011 2GB 1100 4GB 1101 8GB 1110 16GB 1111 RFLU
03:	RAM_CFG_1	0000 0000 0001 80Mx16DDR 0010 32GB 0011 64M 0100 160M 0101 320M 0110 640M 0111 1280M 1000 256M 1001 512M 1010 1GB 1011 2GB 1100 4GB 1101 8GB 1110 16GB 1111 RFLU
04:	RAM_CFG_2	0000 0000 0001 80Mx16DDR 0010 32GB 0011 64M 0100 160M 0101 320M 0110 640M 0111 1280M 1000 256M 1001 512M 1010 1GB 1011 2GB 1100 4GB 1101 8GB 1110 16GB 1111 RFLU
05:	RAM_CFG_3	0000 0000 0001 80Mx16DDR 0010 32GB 0011 64M 0100 160M 0101 320M 0110 640M 0111 1280M 1000 256M 1001 512M 1010 1GB 1011 2GB 1100 4GB 1101 8GB 1110 16GB 1111 RFLU
06:	CRYSTAL_0	00 13.500 Mhz 01 14.31818 10 19.200 Mhz 11 UNKNOWN
07:	TV_MODE_0	00 0FCAM 01 WFSM 10 WFSM 11 CRT
08:	TV_MODE_1	00 0FCAM 01 WFSM 10 WFSM 11 CRT
09:	AGP_30_8x	0 AGP8x 1 8XDISABLED
10:	AGP_SBA	0 SBA 1 8XDISABLED
11:	AGP_FASTWR	0 FW 1 8XDISABLED
12:	PCI_DEVID_0	1100 (default 0x00FC)
13:	PCI_DEVID_1	
20:	PCI_DEVID_2	
21:	PCI_DEVID_3	
14:	BUS_TYPE	0 PCI 1 AGP
15:	FP_IFACE	0 24BR 1 12BR (DEFAULT)
23:	FB_0	0 0M 1 64M 12550M (DEFAULT) 512M
24:	FB_1	0 0M 1 64M 12550M (DEFAULT) 512M
25:	BR	0 BRIDGE 1 BRIDGEBUS ENABLED
26:	BR_128M	BR RTS IGNORED IF BRIDGE IS ENABLED
27:	BR_AGP	
28:	BR_IO	
29:	ROM_TYPE_0	00 01 PARALLEL SERIAL_AT25F
30:	ROM_TYPE_1	SERIAL_55T40VF LPC
16:	USER_0	0000 (DEFAULT)
17:	USER_1	
18:	USER_2	
19:	USER_3	
PEX_PLL_EN_TERM100		
3GIO_PADCFG_LUT_ADDR[0]		
3GIO_PADCFG_LUT_ADDR[1]		



## XTAL, GPIO, BIOS, Fan Control, JTAG Headers

Net		NET_PHYSICAL_TYPENET_SPACING_RULE
<b>Name</b>		
<b>R1</b>	NAME	NAME
<b>R2</b>	P_LLCVDD	20MIL_TRACE
<b>R3</b>	P_LLVDD	20MIL_TRACE
<b>R4</b>	DHP_P_LLVDD	12MIL_TRACE
<b>R5</b>	DHP_P_LLVDD	12MIL_TRACE
		10MIL



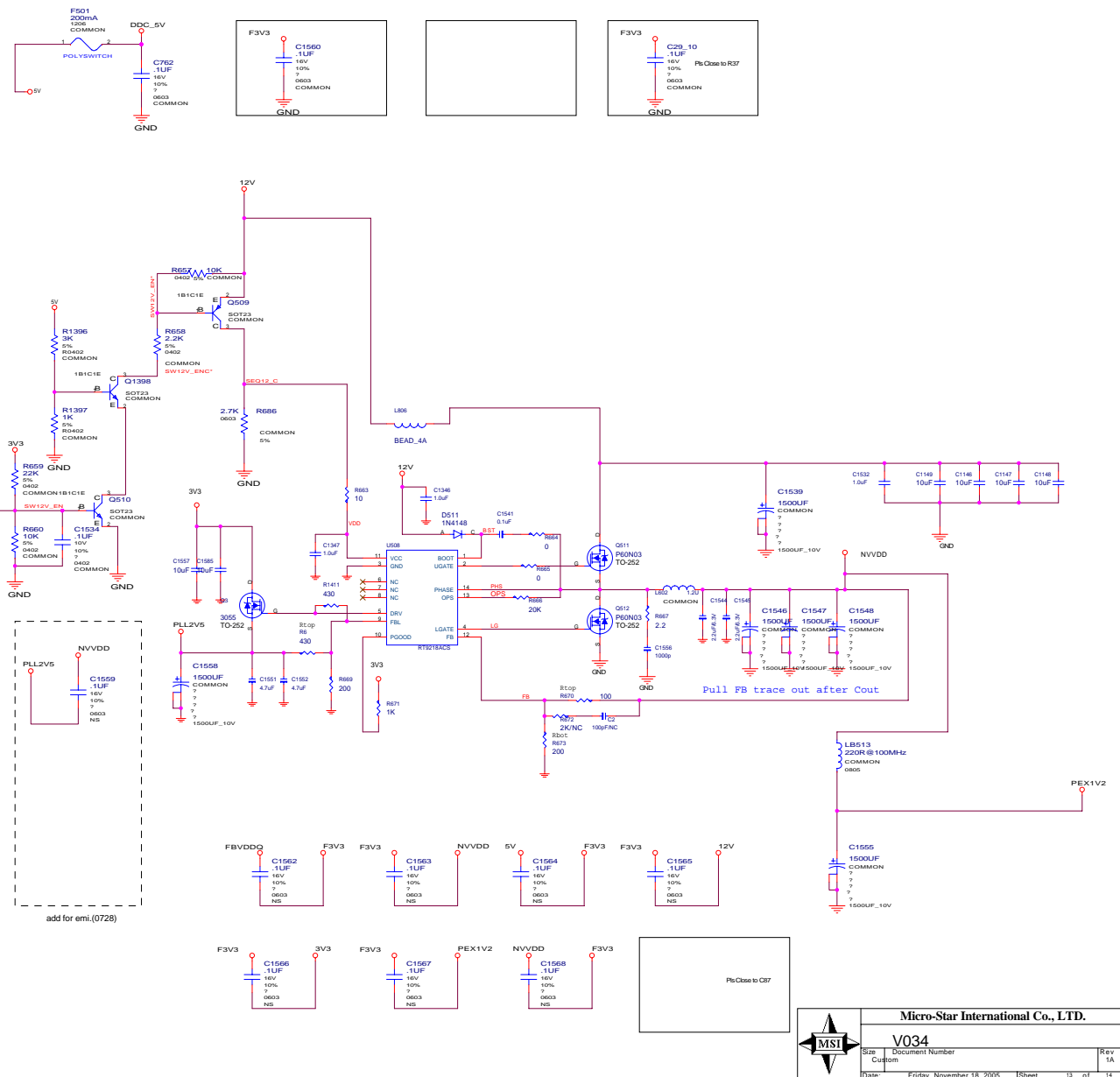


ASSEMBLY	BASE LEVEL GENERIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND
PAGE	FROM NOT FINAL
DETAIL	DRILL CONNECTORS: MiniDIN, 2x6
	HCR

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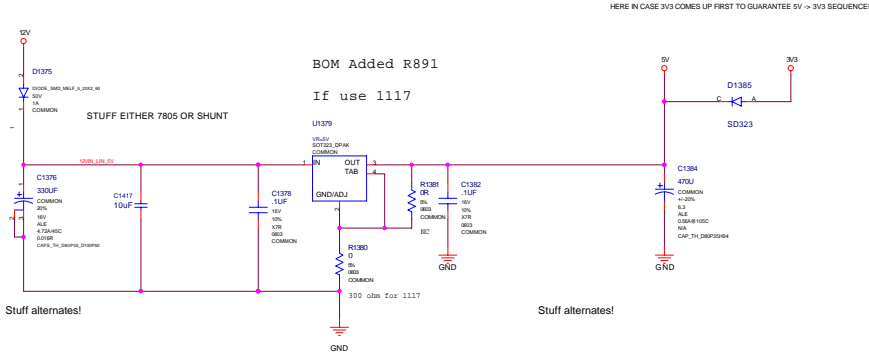
A	B	C	D	E	F	G	H
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## PowerSupplyII: 5V, DDC5V, A3V3, F3V3, TMDS\_PLLVDD



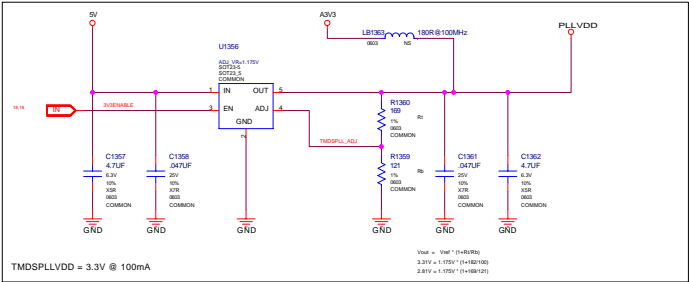
# 14 Others Power Supply (Linears)

## 5V,FBVDDQ,A3V3,3V3,TMDS\_PLLVDD,TMDS\_IOVDD,FBVTT

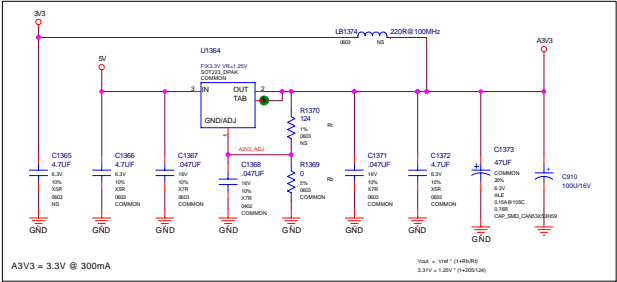


## 5V LOW COST REGULATOR

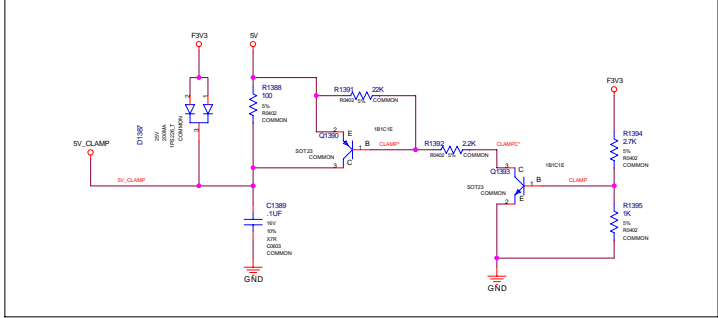
TMDS PLL Supply



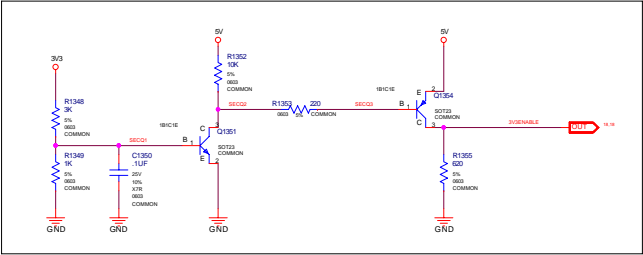
A3V3 Power Supply



5V\_CLAMP



Power Sequencing



5V and PEX3V3 UP . ALL OTHER LINEARS UP



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