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1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X200

MLB-C1

LAST\_MODIFIED=

Tue Oct 29 15:52:27 2013

REV

ECN

DESCRIPTION OF REVISION

CK APPD

A

0002535199

PRODUCTION RELEASED

2014-01-13

SCH AND BOARD PART NUMBERS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-0886	1	SCH_MLB-C1_X200	SCH1	
820-4124	1	PCBF_MLB-C1_X200	PCB1	

PDF CSA CONTENTS

			SYNC MASTER	DATE
1	1	TABLE OF CONTENTS	N/A	N/A
2	2	BLOCK DIAGRAM: SYSTEM	J85_MLB_I2	04/02/2013
3	4	BOM TABLES	J72_MLB_I1	26/2012
4	6	SOC: MAIN	N/A	04/18/2011
5	7	SOC: I/OS	N/A	05/05/2011
6	8	SOC: NAND	N/A	04/18/2011
7	9	SOC: DP,MIPI	MLB	05/04/2012
8	10	SOC: SRAM, IO PWRS	N/A	04/18/2011
9	11	SOC: VDD, SRAM, CPU, GPU PWRS	N/A	04/18/2011
10	12	SOC: MISC & ALIASES	N/A	04/11/2011
11	13	IO: TRISTAR	N/A	N/A
12	14	NAND STORAGE	MLB	05/04/2012
13	17	TOUCH: SUPPORT CKT & CONN	N/A	06/21/2010
14	18	AUDIO: HP FLEX CONN	N/A	03/31/2011
15	19	AUDIO: L81 CODEC	KAVITHA	01/18/2012
16	20	AUDIO: CS35L19A AMPS	KAVITHA	01/18/2012
17	21	BUTTON: CONN	N/A	N/A
18	22	VIDEO: EDP SUPPORT & CONN	J85_MLB_I2	05/2012
19	24	SENSOR: OSCAR	J72_MLB_I1	26/2012
20	26	CAMERA: FF-ALS CONN & FILTERS	J85_MLB_I2	03/2012

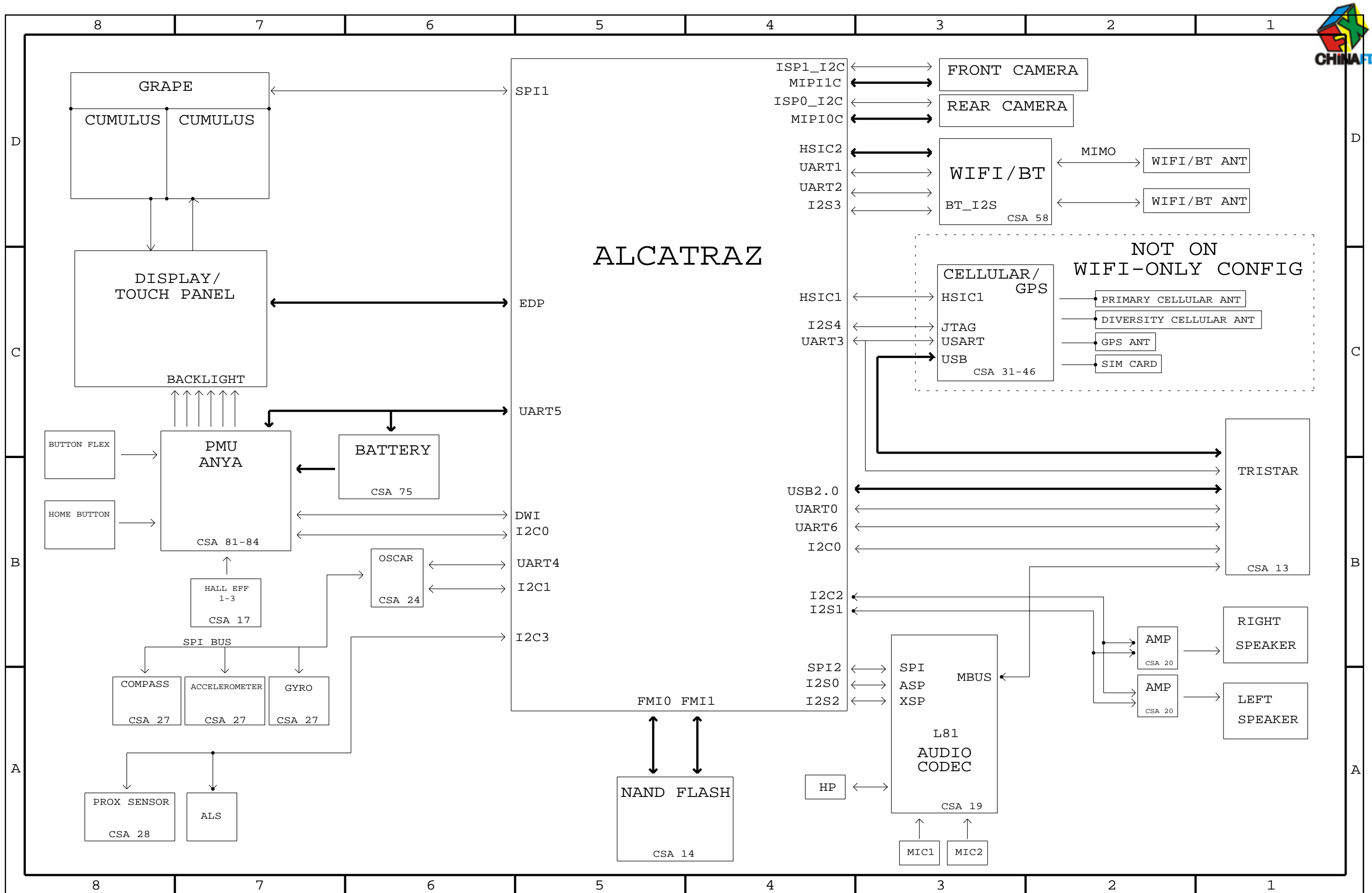
PDF CSA CONTENTS

			SYNC MASTER	DATE
21	27	SENSOR: ACCEL, COMPASS, GYRO	N/A	N/A
22	28	SENSOR: PROX	J85_MLB_I2	05/12
23	29	CAMERA: REAR CONN & FILTERS	N/A	N/A
24	30	CELL:AP INTERFACE & DEBUG CONNECTORS	J85_MLB_I2	03/2013
25	32	CELL: BASEBAND PMU (1 OF 2)	RADIO_MLB_I1	03/2013
26	33	CELL: BASEBAND PMU (2 OF 2)	RADIO_MLB_I1	03/2013
27	34	CELL: BASEBAND (1 OF 2)	RADIO_MLB_I1	03/2013
28	35	CELL: BASEBAND (2 OF 2)	RADIO_MLB_I1	03/2013
29	36	CELL: RF TRANSCEIVER (1 OF 2)	RADIO_MLB_I1	03/2013
30	37	CELL: RF TRANSCEIVER (2 OF 2)	RADIO_MLB_I1	03/2013
31	38	CELL: RX MATCHING	RADIO_MLB_I1	03/2013
32	39	CELL: RF TRANSCEIVER (3 OF 4)	RADIO_MLB_I1	03/2013
33	40	CELL: PENTABAND PA	RADIO_MLB_I1	03/2013
34	41	CELL: BAND 2/3 PAD	RADIO_MLB_I1	03/2013
35	42	CELL: BAND 7/20 PAD	RADIO_MLB_I1	03/2013
36	43	CELL: BAND 5/8 PAD	RADIO_MLB_I1	03/2013
37	44	CELL: 2G PA	RADIO_MLB_I1	03/2013
38	45	CELL: PA DCDC CONVERTER	RADIO_MLB_I1	03/2013
39	46	CELL: ASM AND HB LTE FRONT-END	RADIO_MLB_I1	03/2013
40	47	CELL: RX DIVERSITY	RADIO_MLB_I1	03/2013
41	48	CELL: GPS	RADIO_MLB_I1	03/2013
42	49	CELL: ANTENNA FEEDS	RADIO_MLB_I1	03/2013
43	57	IO: FILTERS & HOTBAR CONN	N/A	04/18/2011
44	58	WIFI/BT: MODULE	WIFI_DEV05	20/2013
45	75	POWER: BATTERY CONNECTOR	N/A	N/A
46	81	PMU: ANYA PAGE 1	J72_MLB_I1	26/2012
47	82	PMU: ANYA PAGE 2	J85_MLB_I2	03/2012
48	83	PMU: ANYA PAGE 3	J72_MLB_I1	26/2012
49	84	PMU: ANYA PAGE 4	J72_MLB_I1	26/2012
50	85	POWER: PP1V8_SW	J85_MLB_I1	26/2012
51	90	SEP: EEPROM & SOC DEBUG	J72_MLB_I1	26/2012
52	93	TEST: TP/HOLES/FIDUCIALS	J85_MLB_I2	03/12
53	94	TEST: EE TP/PP	J72_MLB_I1	26/2012
54	121	POWER: ALIASES	J72_MLB_I1	26/2012

CHINA

FDX

DRAWING





## Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:

## BOM OPTIONS

```
COMMON
ALTERNATE
16GB_PROD
32GB_PROD
64GB_PROD
128GE_PROD

DEVELOPMENT_JTAG_TAP
JTAG_DAP
MLB (WDOG TO PMU)
```

## WIFI BOM OPTIONS

ANDGATE\_TI  
FERRITE\_TY  
FERRITE\_TDK

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE

## SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BCM OPTION
339S0207	1	H6P + 1GB ELPIDA	U0652	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0208	339S0207		U0652	HYNIX DDR

## PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0656	1	IC,PMU,ANYA,D2089A1,OTFXX,FCCSP342	U8100	CRITICAL	

## FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0921	1	TOS, 19NM, PPN1.5,C,DDP,16GB	U1400	16GB
335S0922	1	TOS, 19NM, PPN1.5,C,QDP,32GB	U1400	32GB
335S0923	1	TOS, 19NM, PPN1.5,C,ODP,64GB	U1400	64GB
335S0929	1	TOS, 19NM, PPN1.5,C,12DP,64GB	U1400	96GB
335S0924	1	TOS, 19NM, PPN1.5,C,16DP,128GB	U1400	128GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0930	335S0921	16GB	U1400	HYNIX 20NM PPN1.5 16GB
335S0931	335S0922	32GB	U1400	HYNIX 20NM PPN1.5 32GB
335S0932	335S0923	64GB	U1400	HYNIX 20NM PPN1.5 64GB

## U2200

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S4272	1	IC, SLOS4P142IV, PWR SW, GREENPET3, 4A, TDPHS	U2200	

NOTE: FOLLOWING J72, U2200 USES 353S3672 FOOTPRINT (353S4272 HAS SMALLER PADS DUE TO NEW DFM RULES)

4.3UF CAP

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657		c1009,c1015...	RDAR #13988471

## MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-6207	1	FENCE,TALL,MLB,X221	PD_FENCE_MLB	CRITICAL	
806-7613	1	FENCE,RADIO,MLB,C BRD,X221	PD_CAN_RADIO	CRITICAL	

BARCODE	LABEL/EEEE	CODES
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000001	000001	000001
000002	000002	000002
000003	000003	000003
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000099	000099	000099

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	EEEE FOR 639-5393 (X200C1 GOOD)	FNJ4	CRITICAL	EEEE_X200C_GOOD
825-7639	1	EEEE FOR 639-5394 (X200C1 BETTER)	FNJ5	CRITICAL	EEEE_X200C_BETTER
825-7639	1	EEEE FOR 639-5385 (X200C1 BEST)	FNJ9	CRITICAL	EEEE_X200C_BEST
825-7639	1	EEEE FOR 639-5386 (X200C1 BEST+)	FNJH	CRITICAL	EEEE_X200C_BEST+
825-7639	1	EEEE FOR 639-5387 (X200C1 ULTIMATE)	FNJ6	CRITICAL	EEEE_X200C_ULTIMATE
825-7639	1	EEEE FOR 639-5388 (X200C1 GOOD IVS)	FNJ8	CRITICAL	EEEE_X200C_GOOD_IVS
825-7639	1	EEEE FOR 639-5389 (X200C1 BETTER IVS)	FNJF	CRITICAL	EEEE_X200C_BETTER_IVS
825-7639	1	EEEE FOR 639-5390 (X200C1 BEST IVS)	FNJC	CRITICAL	EEEE_X200C_BEST_IVS
825-7639	1	EEEE FOR 639-5391 (X200C1 BEST+ IVS)	FNJ7	CRITICAL	EEEE_X200C_BEST+_IVS
825-7639	1	EEEE FOR 639-5392 (X200C1 ULTIMATE IVS)	FNJG	CRITICAL	EEEE_X200C_ULTIMATE_IVS

## WIFI

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0223	339S0213		U5800	

GYRO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1192	1	GYRO, ST MICRO	U2720	CRITICAL	GYRO_STMICRO
338S1218	1	GYRO, INVENSENSE	U2720	CRITICAL	GYRO_INVENSENSE
132S0391	1	CAP 0.01UF 25V 0201	C2726	CRITICAL	GYRO_STMICRO
132S0288	1	CAP 0.1UF 16V 0201	C2726	CRITICAL	GYRO_INVENSENSE

338S1158 OLD GYRO - ST MICRO

OLDER INVENSENSE P/N 338S1135

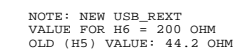
OLD INVENSENSE P/N 338S1200 (3/22/13)

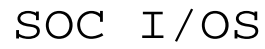
## ACCEL

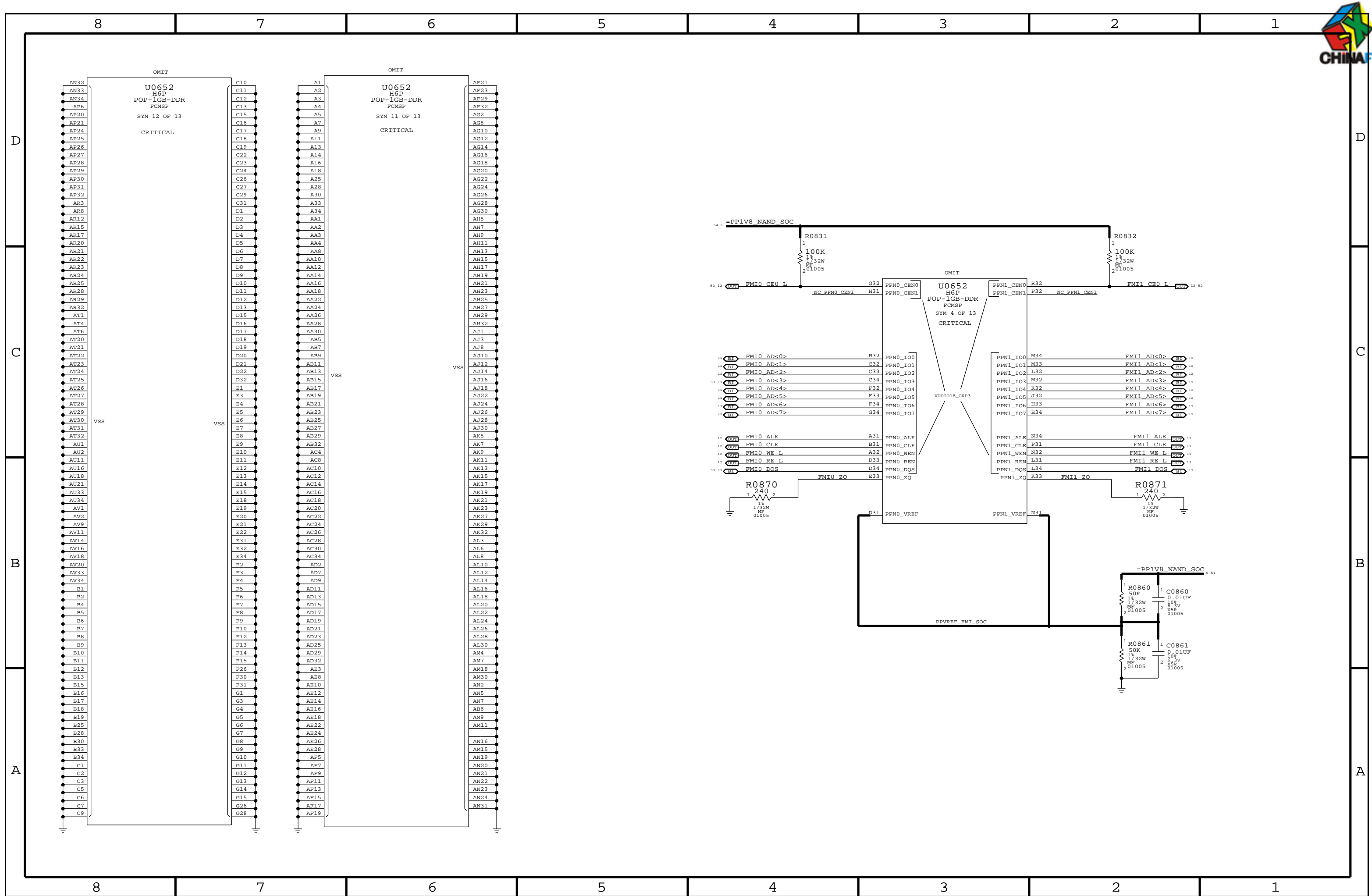
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1163	1	IC,ACCEL,3-AXIS,DIG,BMA282,1GA14	U2700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
-------------	---------------------------	------------	---------	-----------

338S1233 ST MICRO - DISQUAL'ED  
338S1114 OLD ACCEL - ST MICRO  
338S1191 OLD ACCEL - ST MICRO

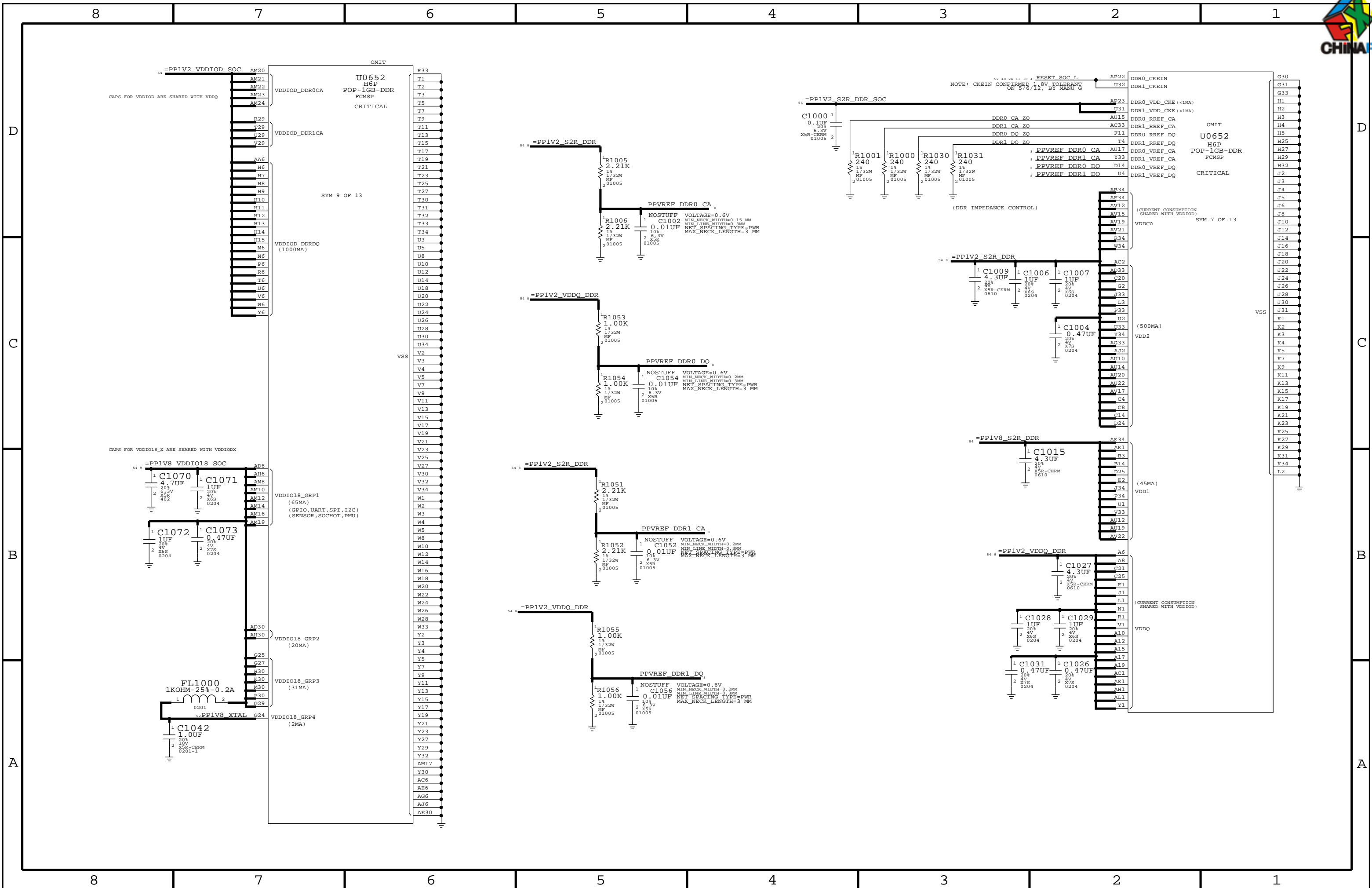




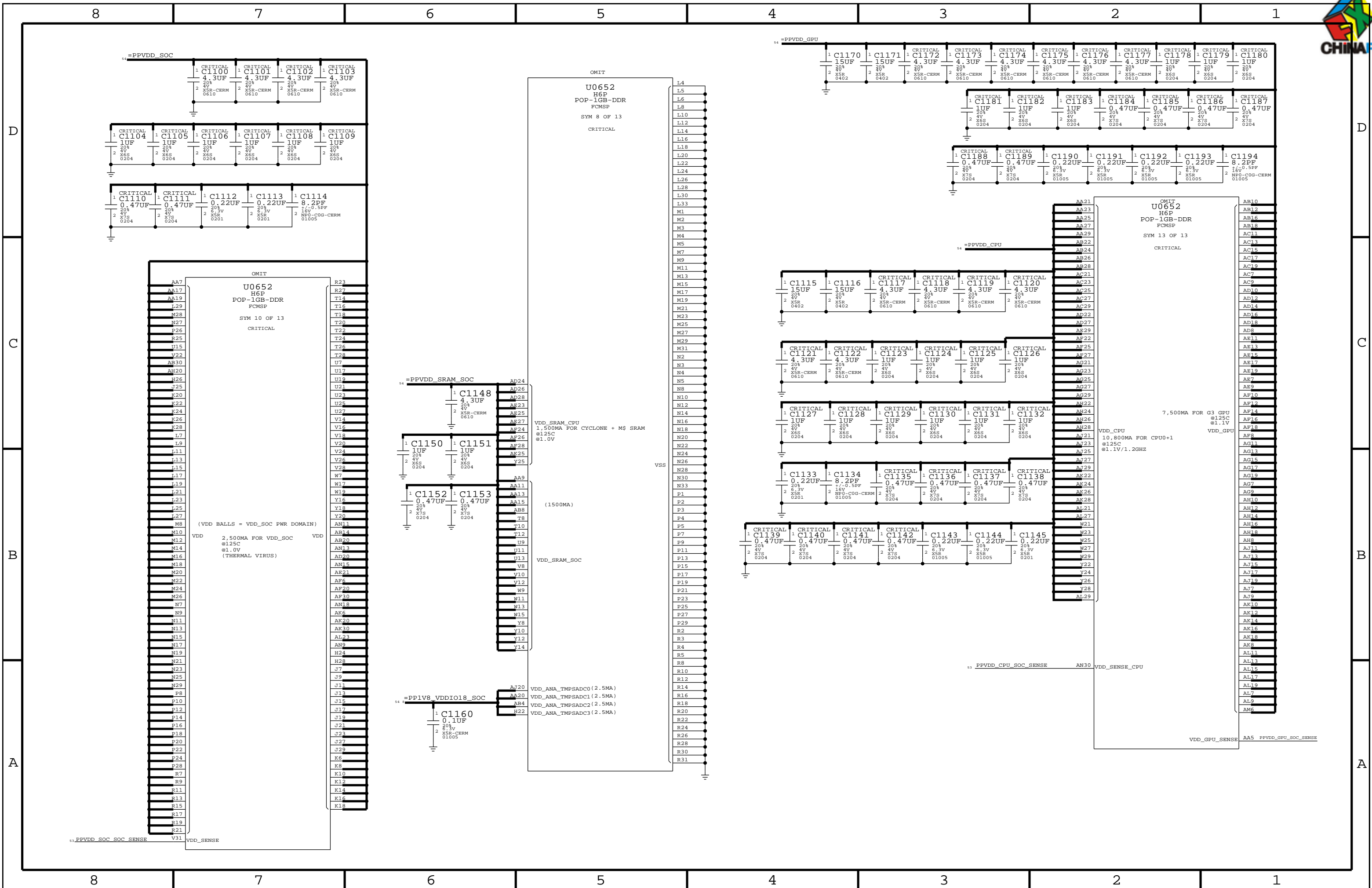


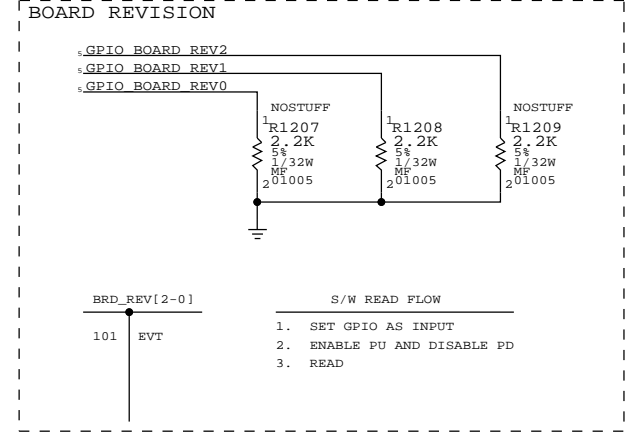
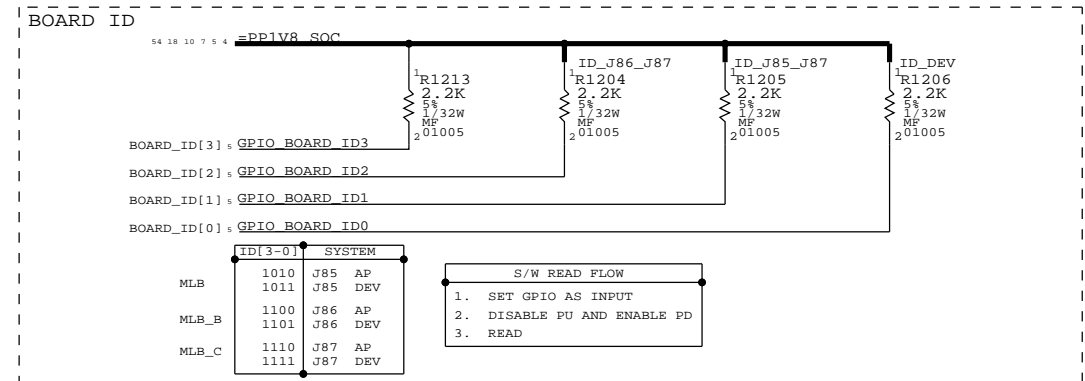
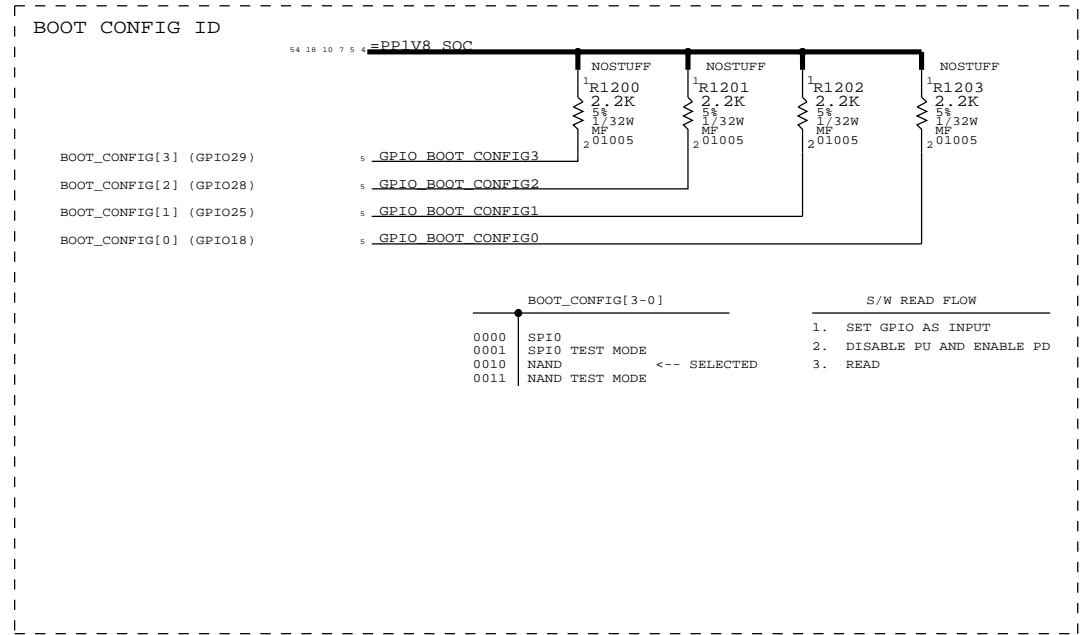
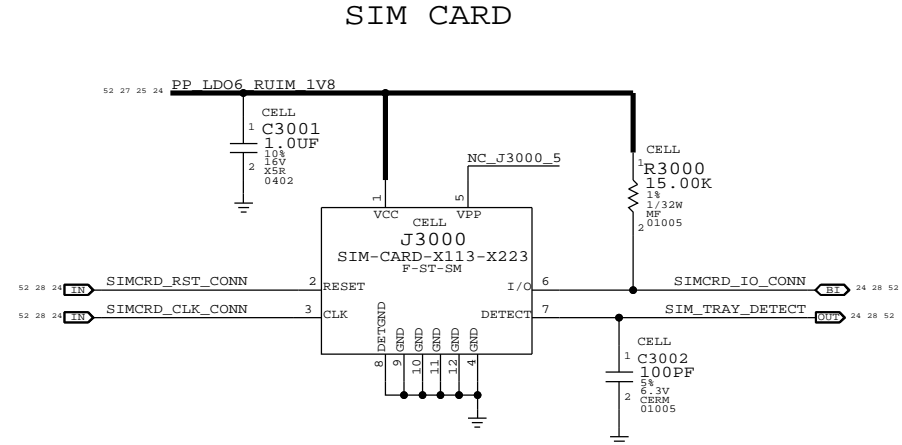
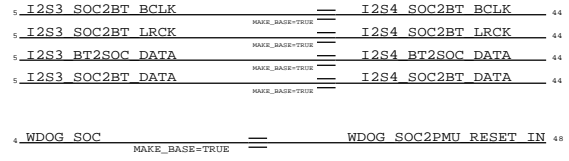
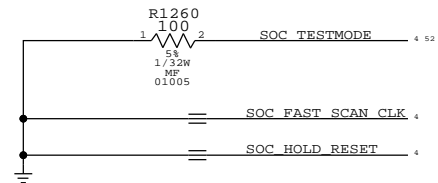
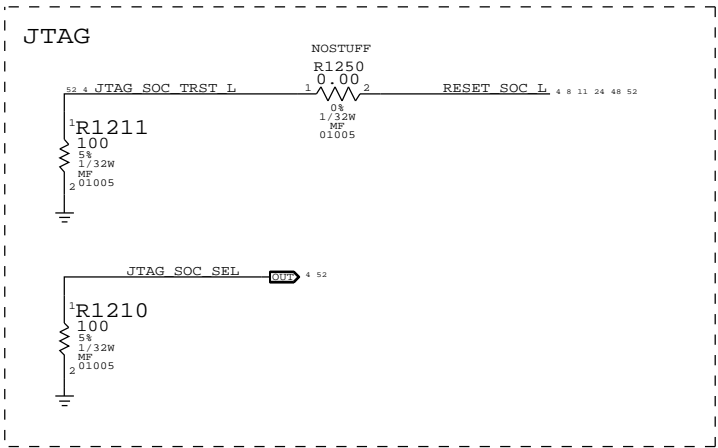








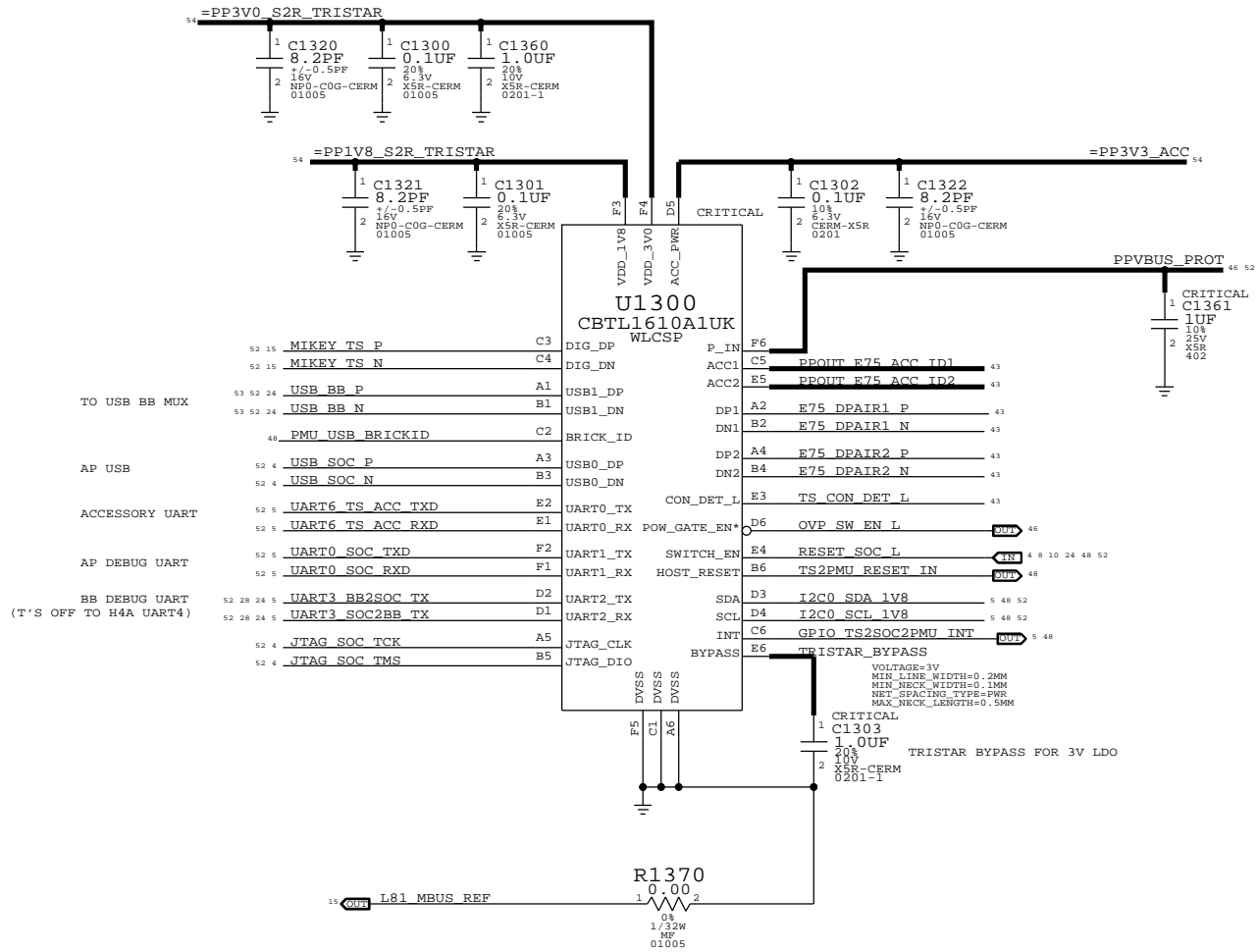


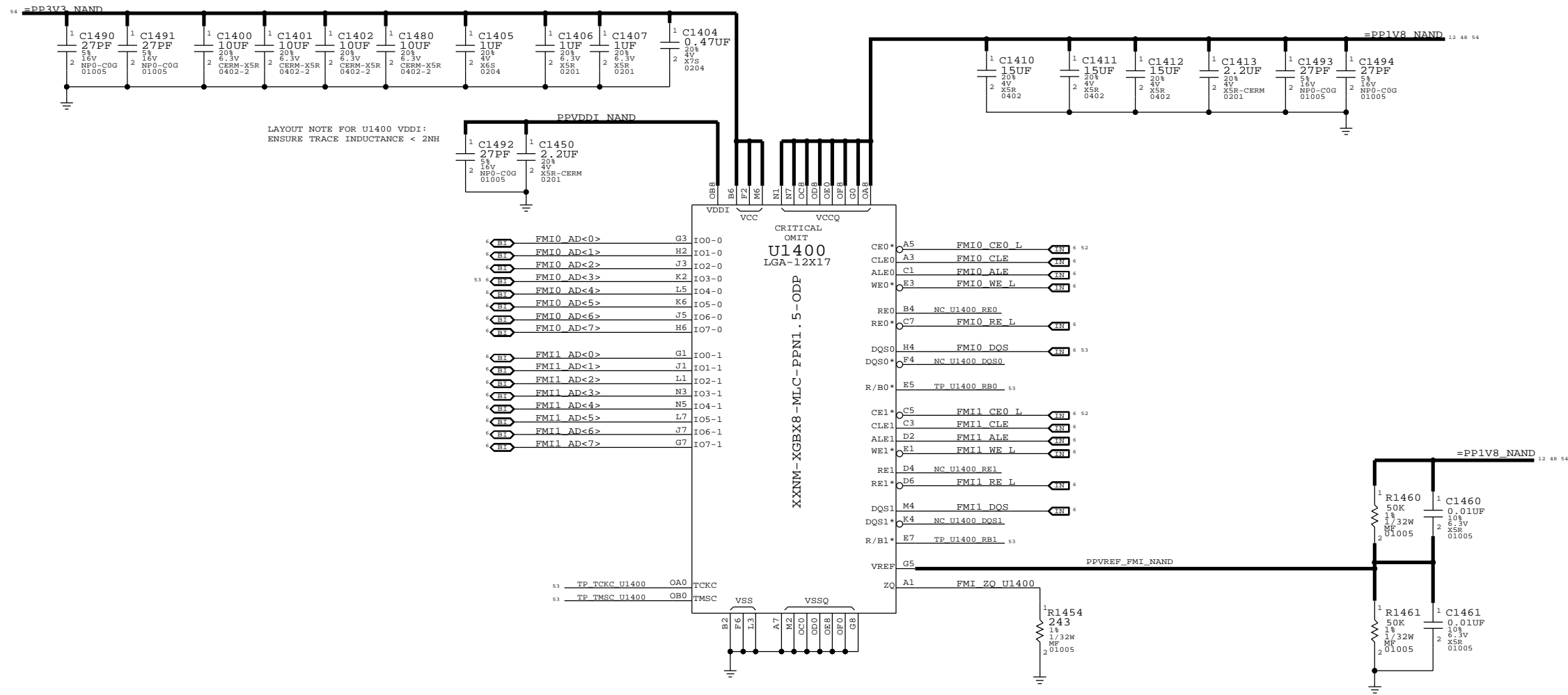


CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

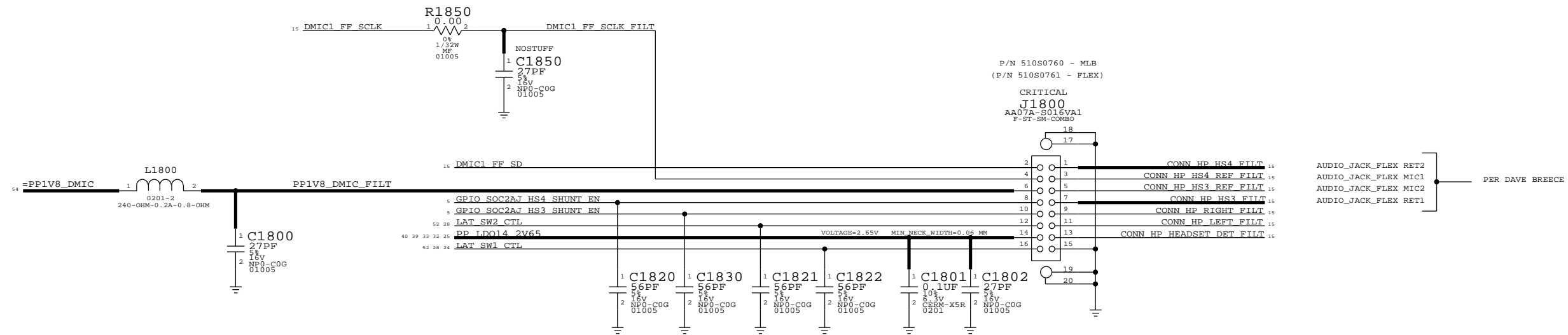
343S0658 = TRISTAR 2, A1  
998-5855 = TRISTAR 2, TC  
343S0639 = TRISTAR 2, A0  
343S0614 = TRISTAR 1

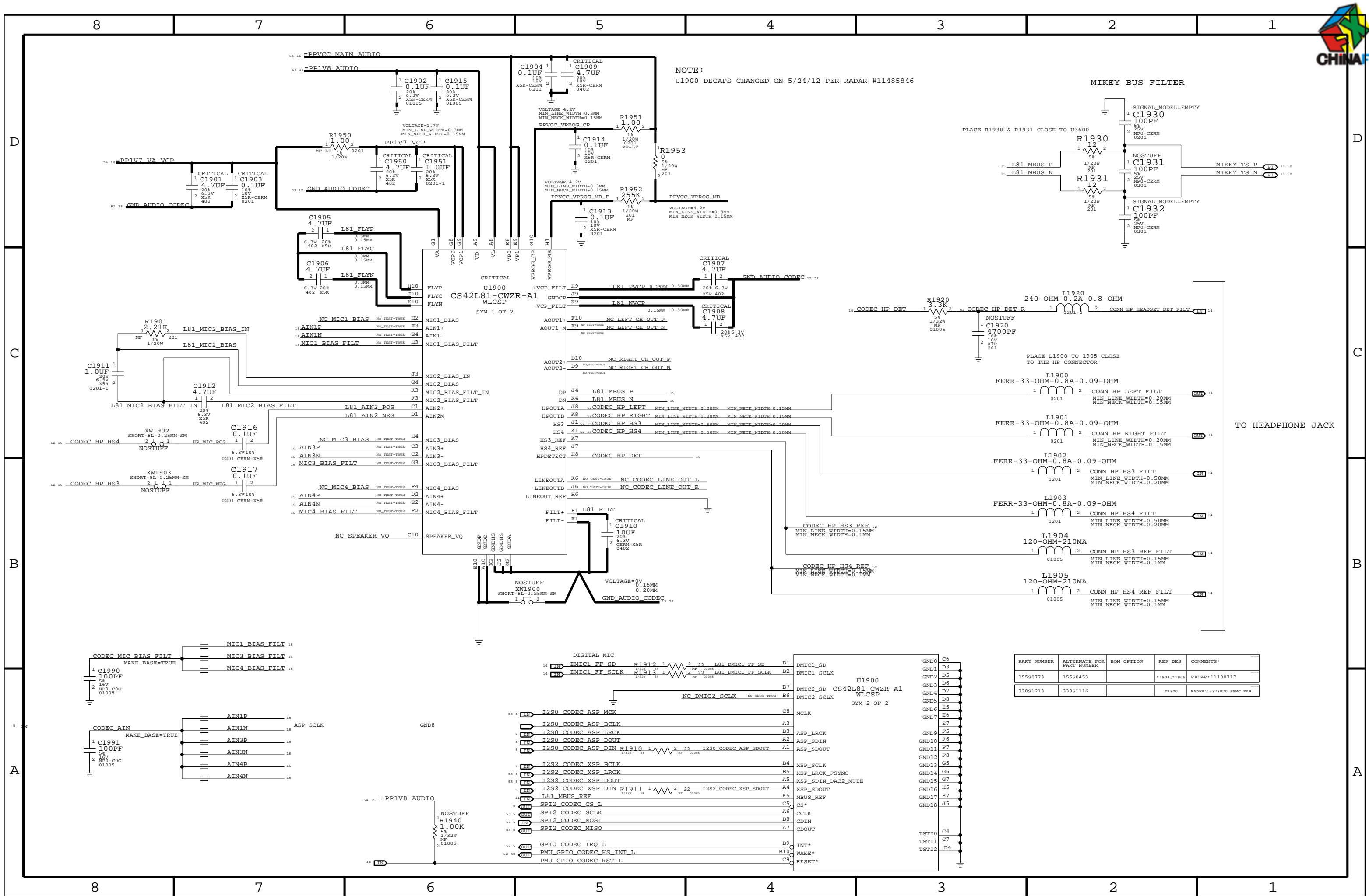
## TRISTAR







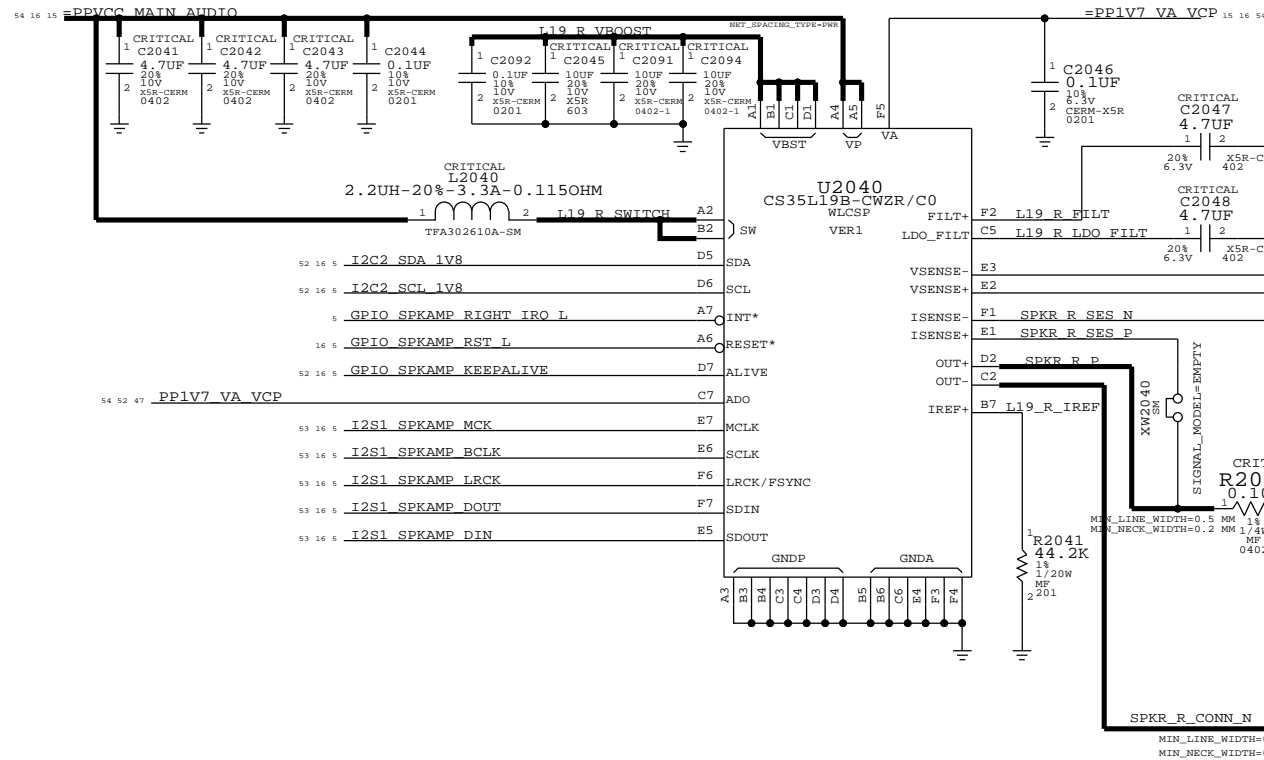






# RIGHT SPEAKER AMP

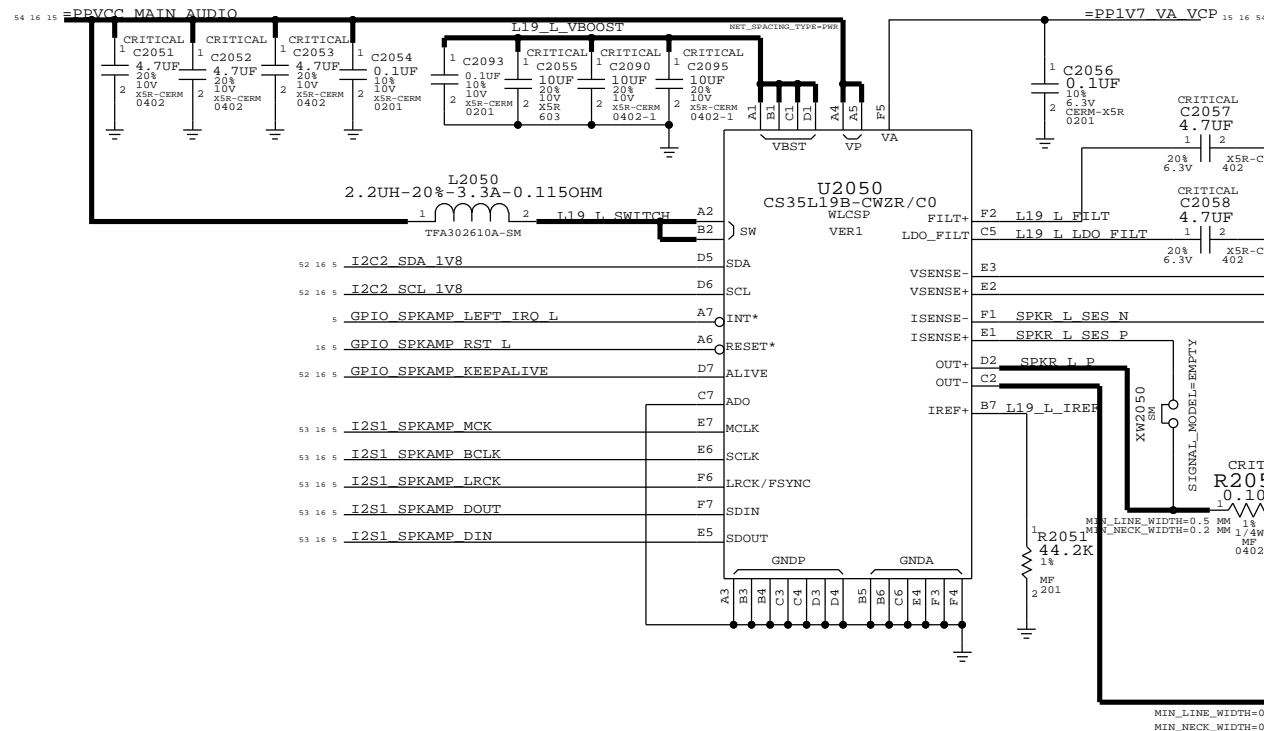
I2C ADDRESS: 1000001X



# SPEAKER CONNECTOR

# LEFT SPEAKER AMP

I2C ADDRESS: 1000000X

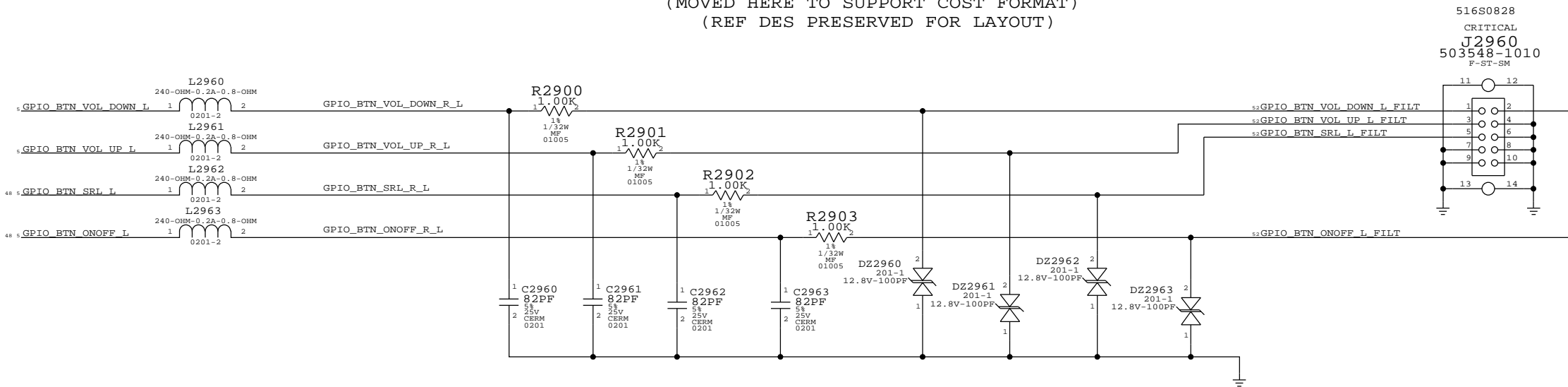


# UPDATED: DEC 13

1. ALL THE EMI/DESENSE FILTER COMPONENTS HAVE BEEN REMOVED BASED ON PERFORMANCE ON J65
2. THE CURRENT VERSION OF L19 IS B0 AND WILL CHANGE TO C0 BY MARCH 2013. C0 FIXES PROCESS ISSUES.

# BUTTON CONNECTOR

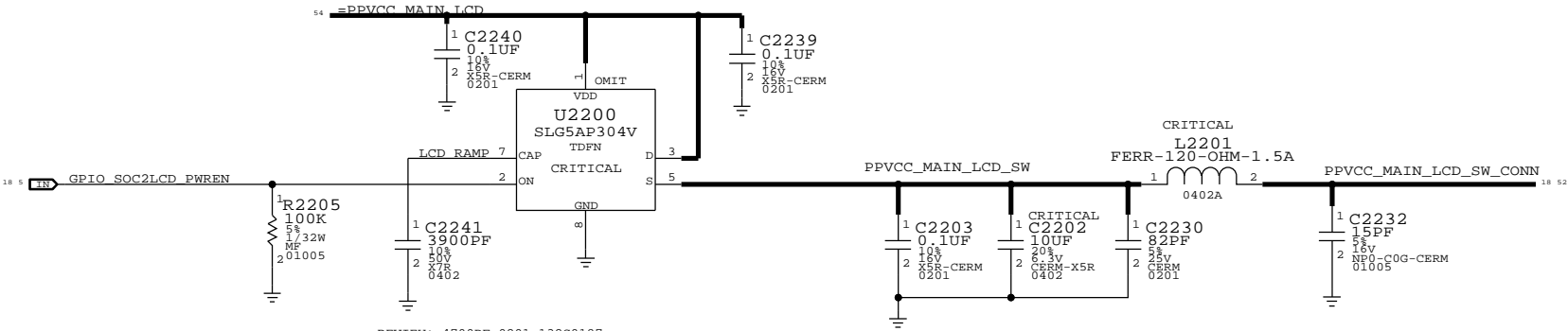
(MOVED HERE TO SUPPORT COST FORMAT)  
(REF DES PRESERVED FOR LAYOUT)



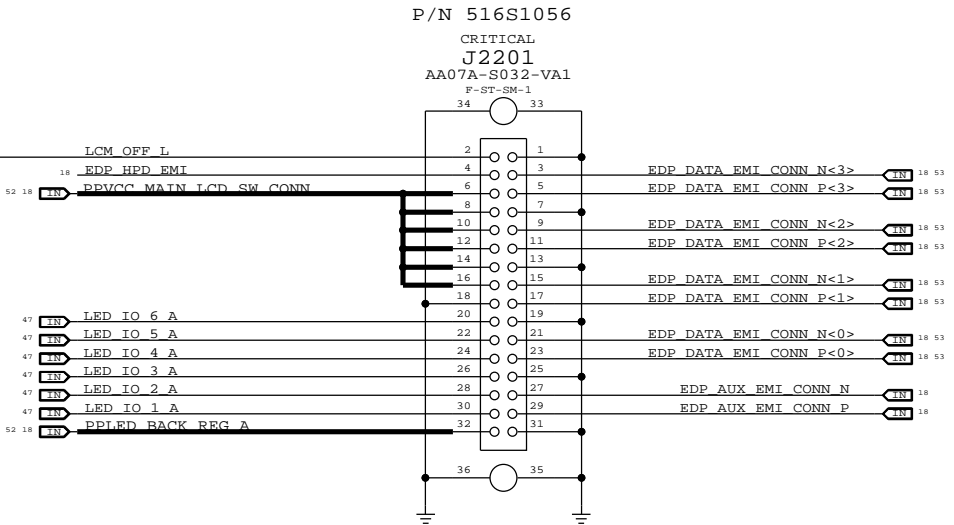


# EDP CONNECTOR SUPPORT

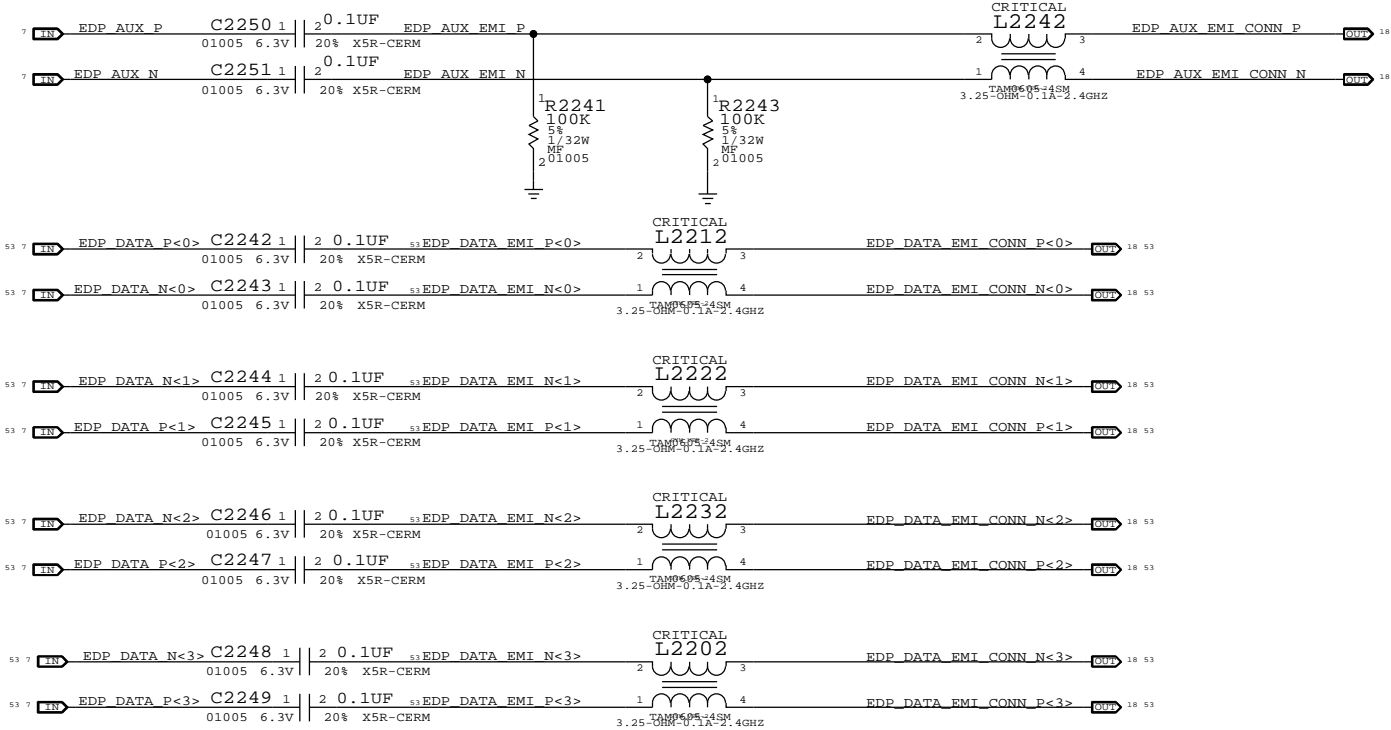
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0667	155S0583	L2242, L2810, L2811, L2812, L2813, L2814, L2710, L2711, L2712, L4030, L4031		RDAR: //PROBLEM/8616066, RDAR: //PROBLEM/9015335



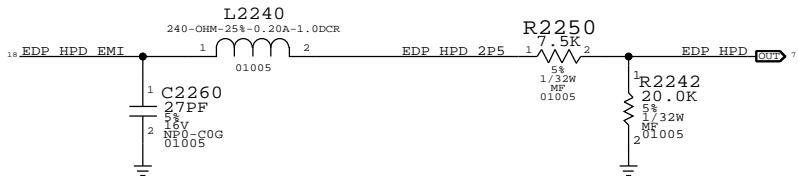
LAYOUT NOTE:  
PUT THERMAL VIAS AROUND U2200 IN CASE OF SHORTED CONDITION



REVIEW: CAN/SHOULD WE USE 132S0316, 0.1UF 20%, 01005 RDAR: //PROBLEM/12579963



REVIEW: WILL THE DISPLAY INCLUDE A VOLTAGE DIVIDER TO REDUCE THE 2.5V FROM THE TCON TO 1.8V TO THE AP? RDAR: //PROBLEM/12579981



NOTE:  
PER GREG DE MERCEY, EDP\_HP D PIN IS 2.5V TOLERANT  
HOWEVER TO BE CONSERVATIVE, DIVIDER CKT IS NOT REMOVED



C

B

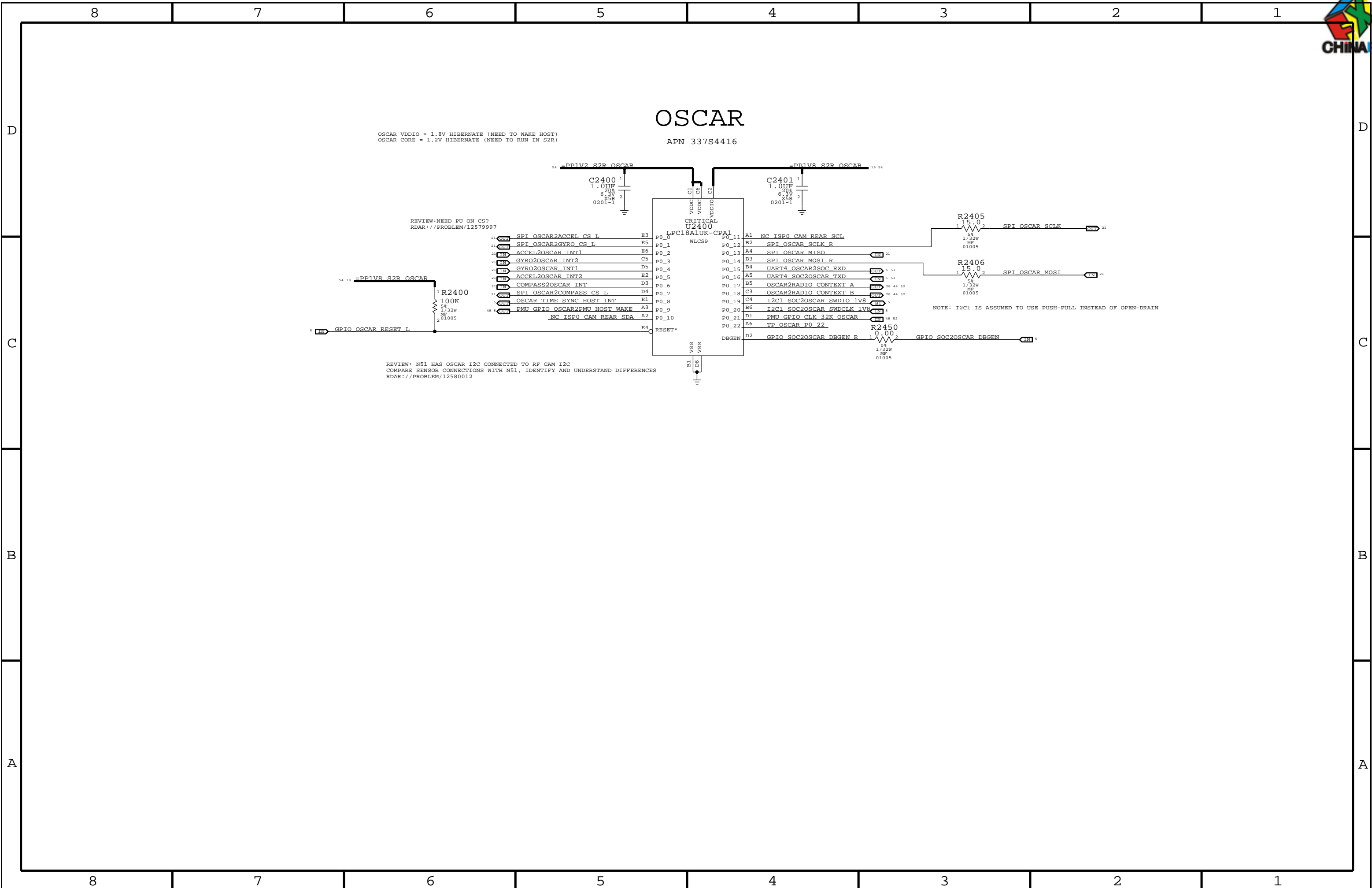
A

D

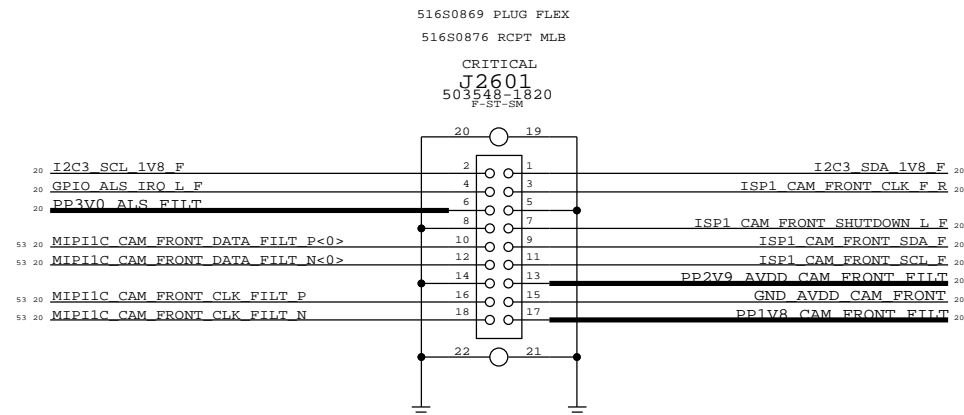
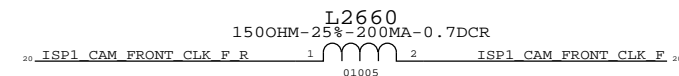
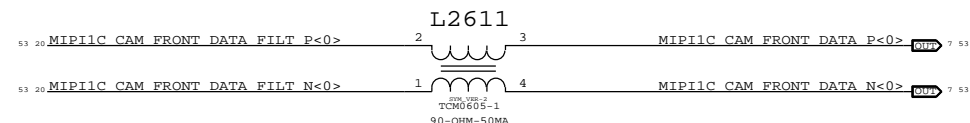
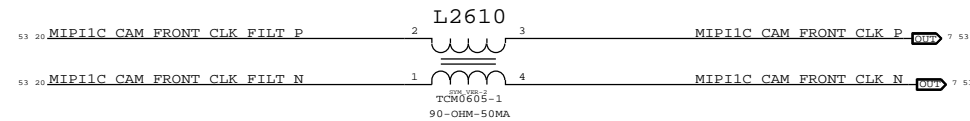
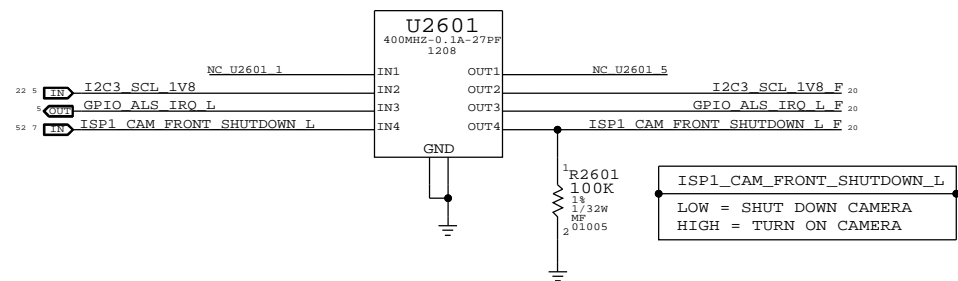
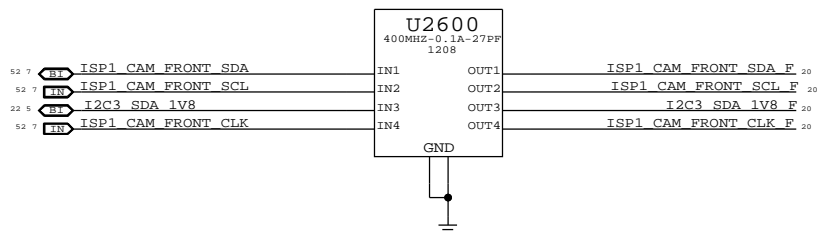
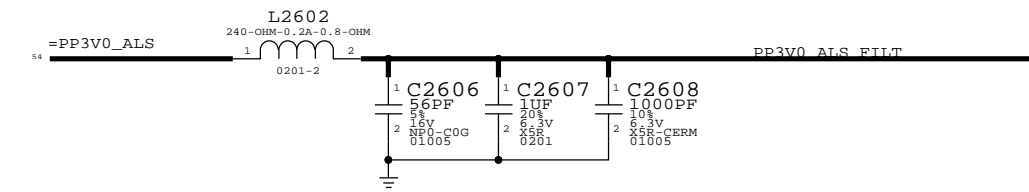
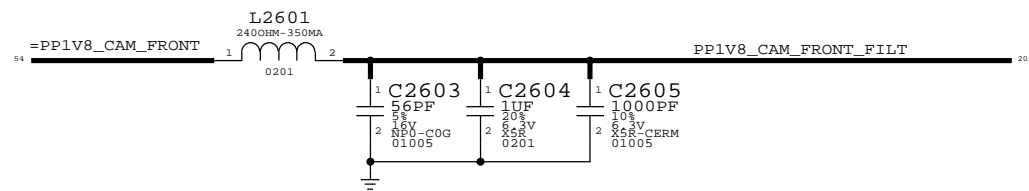
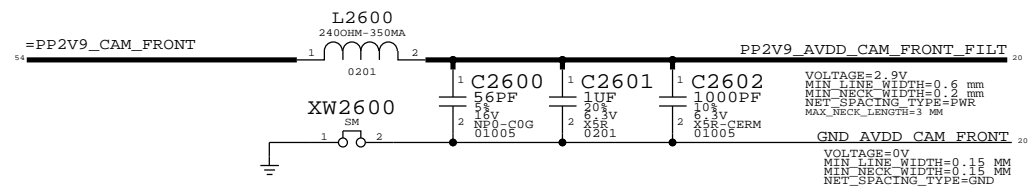
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B

A



# VGA FRONT CAMERA CONNECTOR

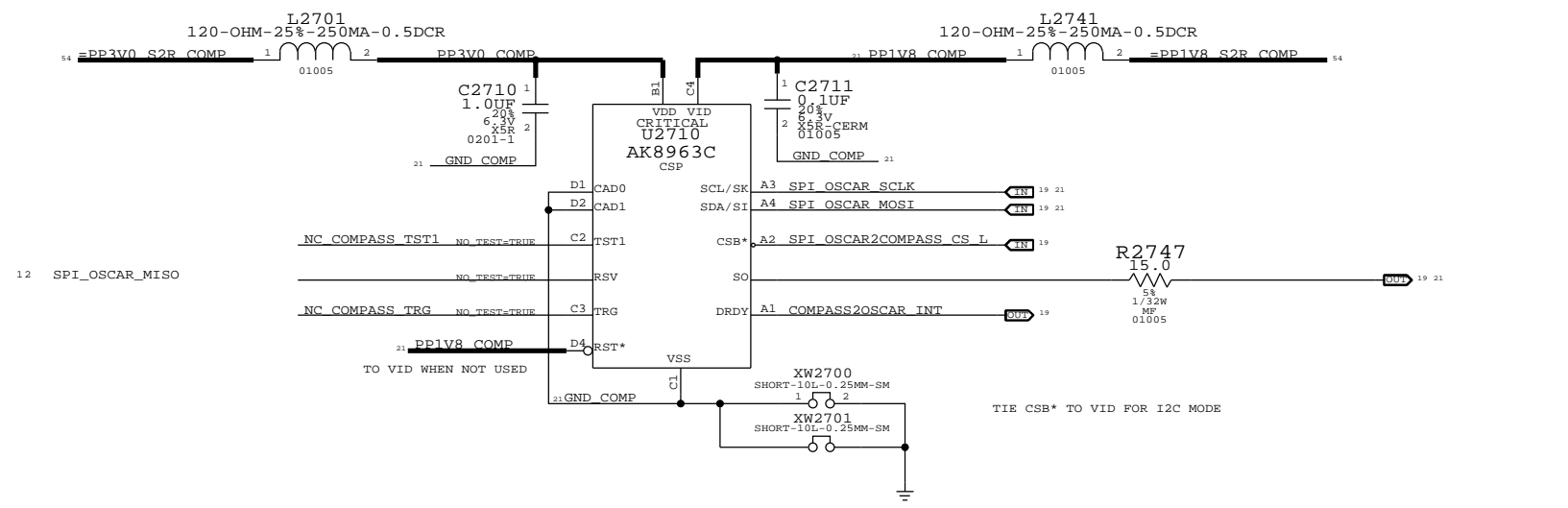
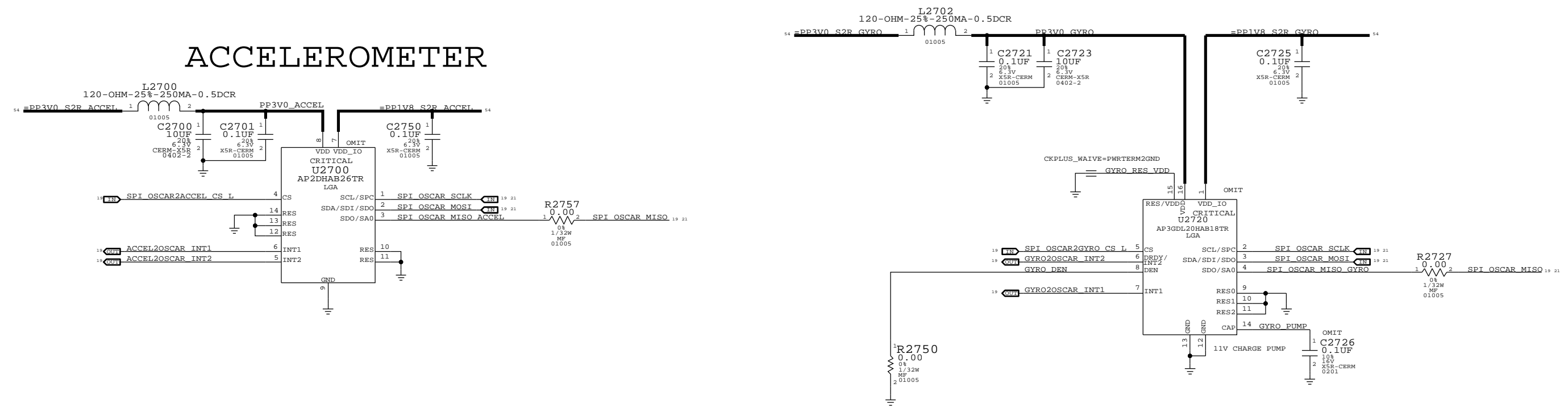




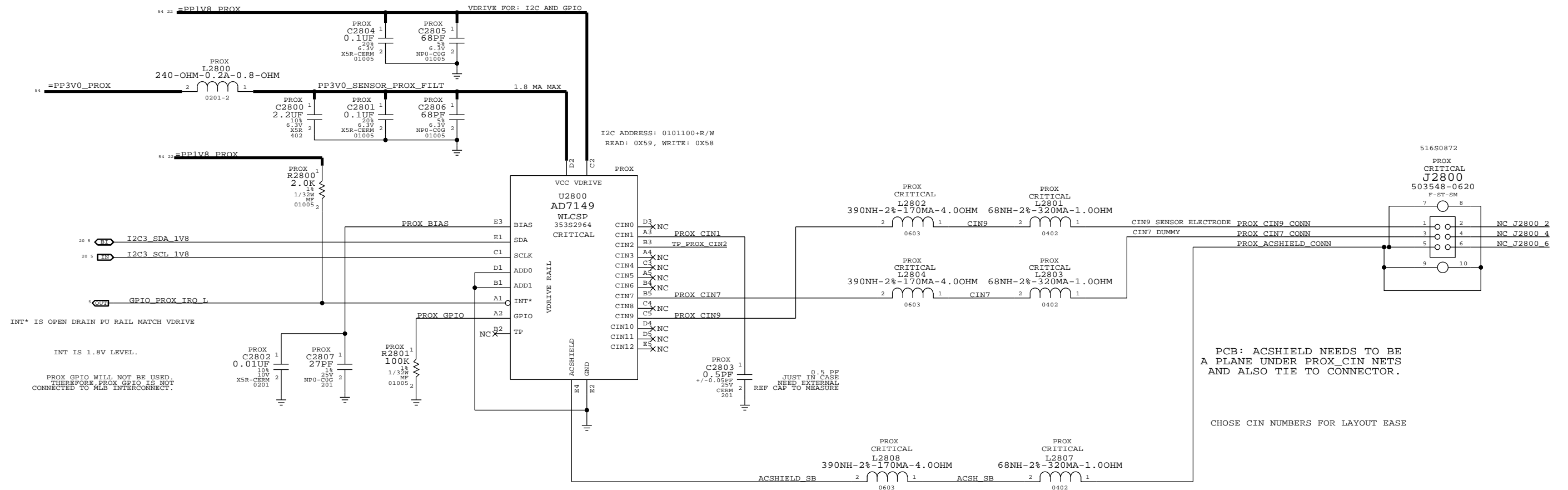
GYRO

ACCELEROMETER

COMPASS  
APN 338S1014



# PROX SENSOR



PCB: ENSURE ACSHIELD PLANE UNDER  
U3200, NO GND PLANE NEAR PROX\_CIN NETS..



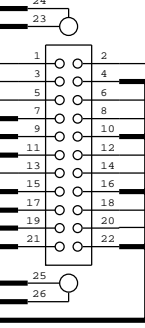


# REAR CAMERA CONNECTOR

APN: 516S0973

PLUG: 516S0974

CRITICAL  
J2950  
AA07-S022VA1  
F-ST-SM



CAM REAR VSYNC

GND CAM AVDD

GND AE AVDD

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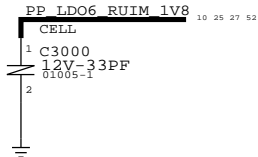
GND



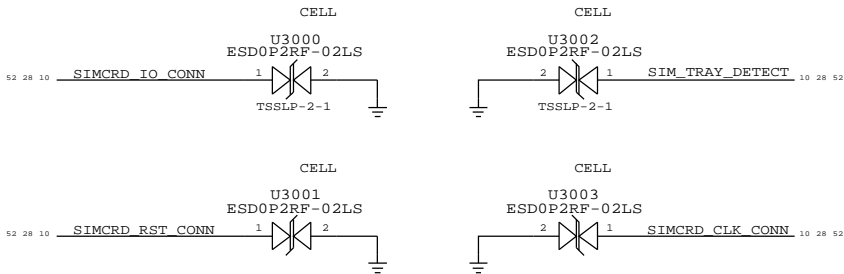
# AP INTERFACE & DEBUG CONNECTORS

## PROBE POINTS

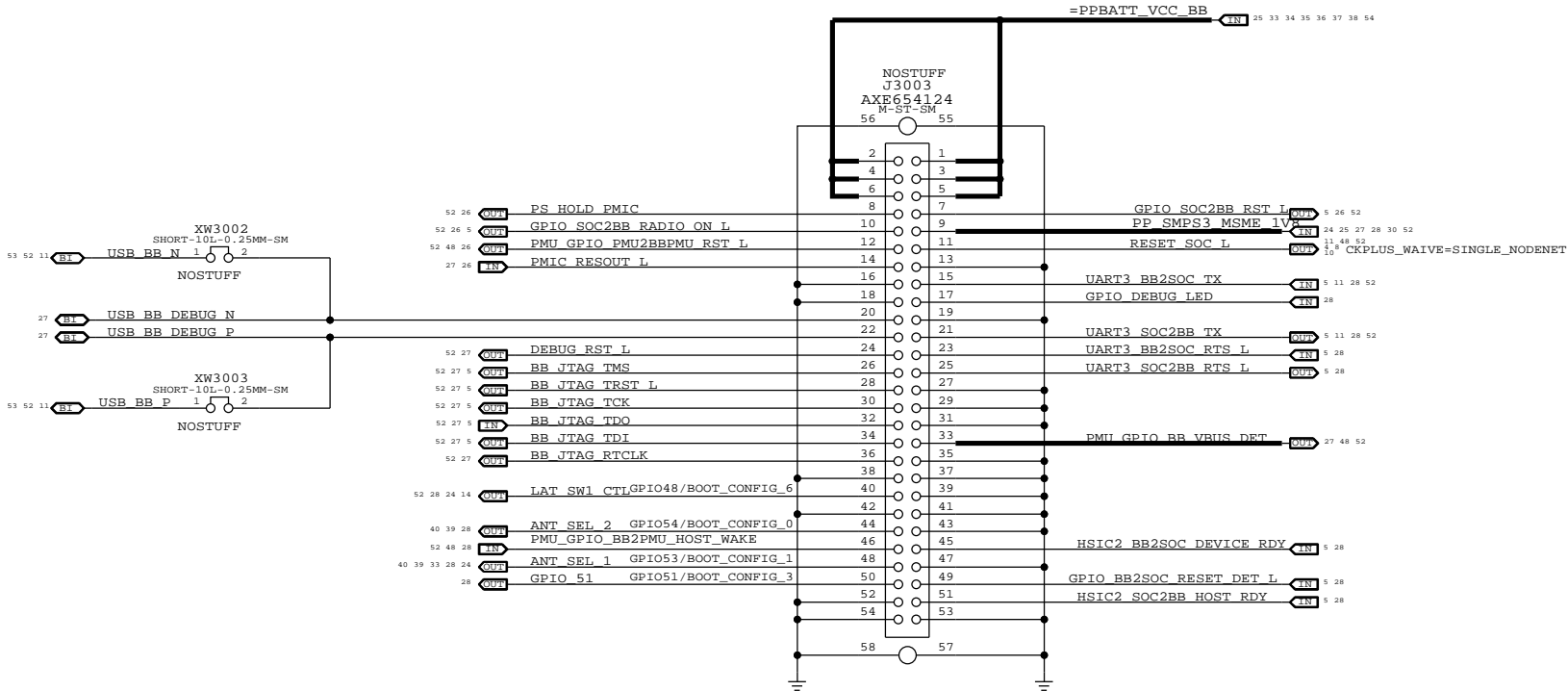
PP3000	P4MM	1	BB_ERROR_FLAG	28
PP3001	P4MM	1	SLEEP_CLK_32K	26 27
PP3002	P4MM	1	PMIC_SSBI	26 27
PP3003	P4MM	1	19P2M_MDM	26 27
PP3008	P4MM	1	WTR_SSBI_TX_GPS	28 29
PP3009	P4MM	1	WTR_SSBI_PRX_DRX	28 29
PP3010	P4MM	1	WTR_RX_ON	28 29
PP3011	P4MM	1	WTR_RF_ON	28 29
PP3012	P4MM	1	UART_WLAN2BB_LTE_COEX	28 44
PP3013	P4MM	1	UART_BB2WLAN_LTE_COEX	28 44



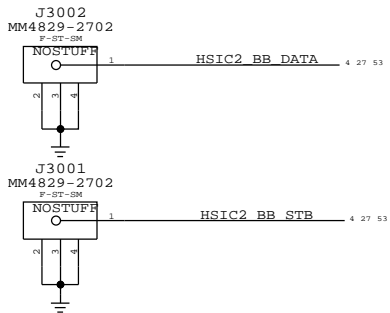
## SIM CARD ESD PROTECTION



## DEBUG CONNECTOR



BOOT OPTIONS	BOOT_CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION							
		6	5	4	3	2	1	0	
BOOT_DEFAULT_OPTION	0X00	X	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0X01	X	1	0	0	0	0	0	1
BOOT_HSIC_OPTION	0X02	X	1	0	0	0	0	1	0
BOOT_USB_OPTION	0X03	X	1	0	0	0	0	1	1
ENABLE_SAHARA_PROTOCOL	0X08	X	1	0	0	1	0	X	X





# PMU (1 OF 2)

D

D

C

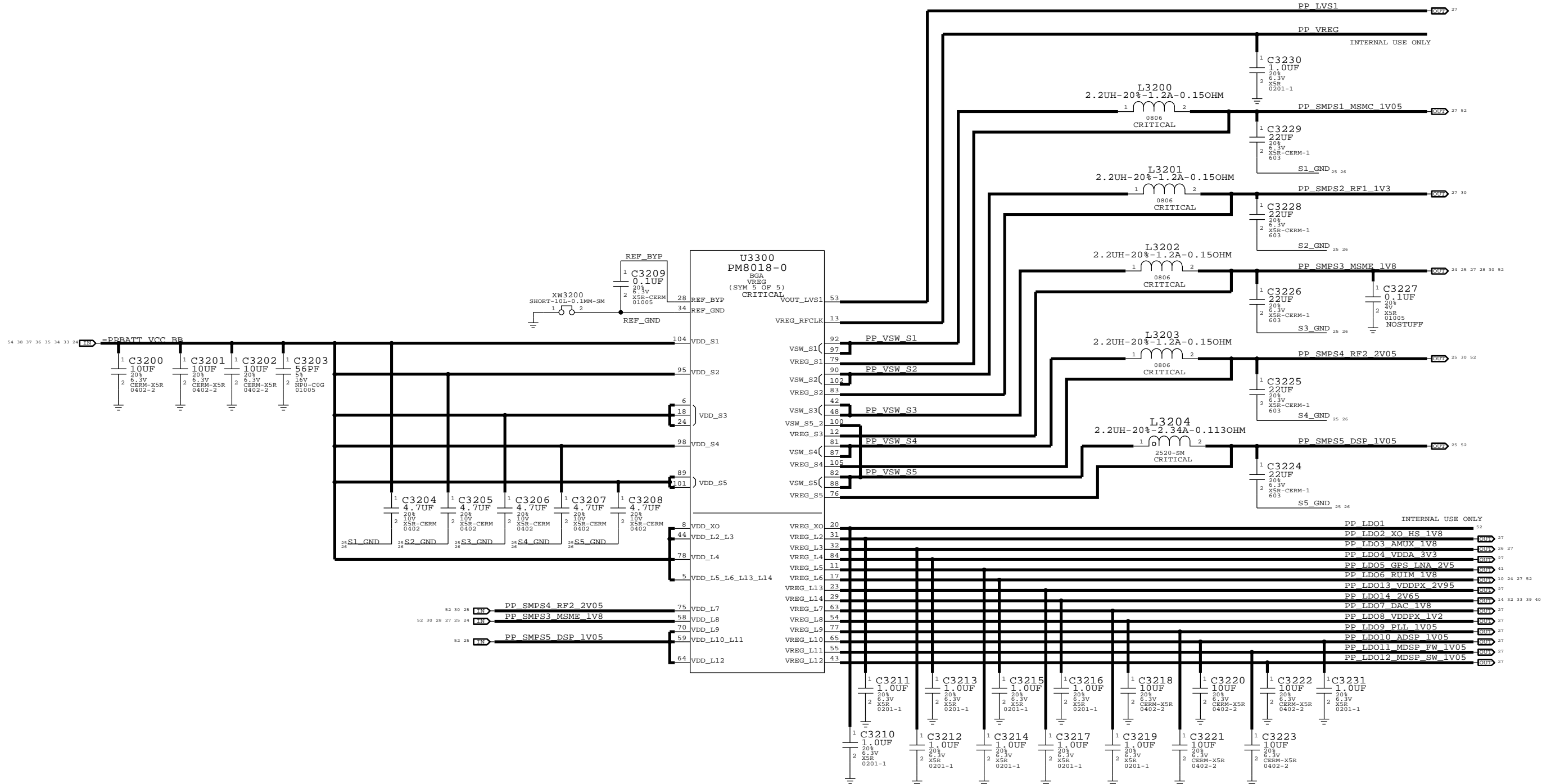
C

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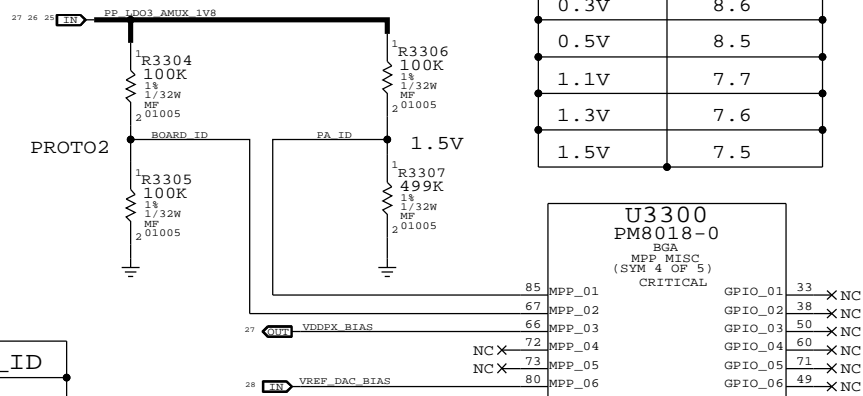
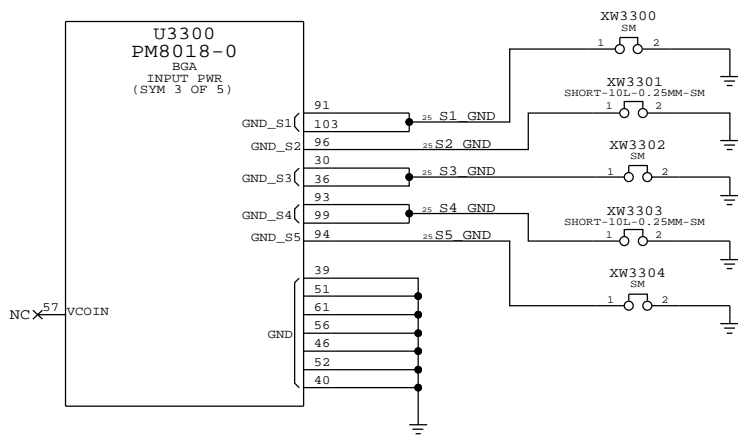
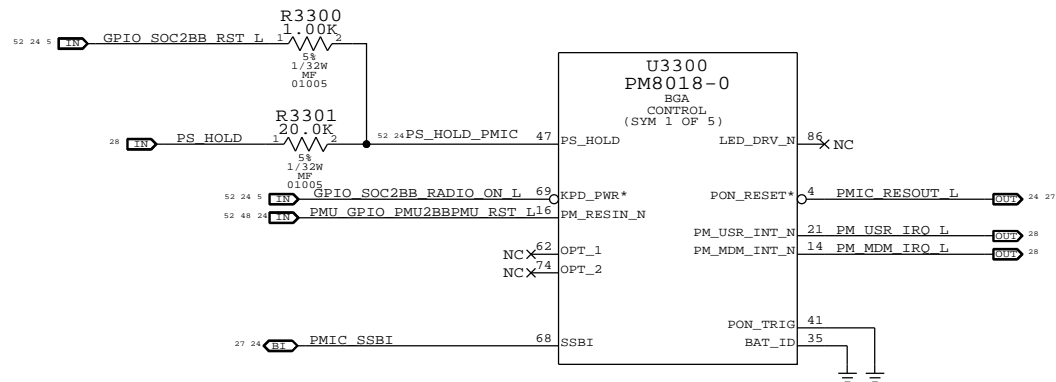


PMU ( 2 OF 2 )

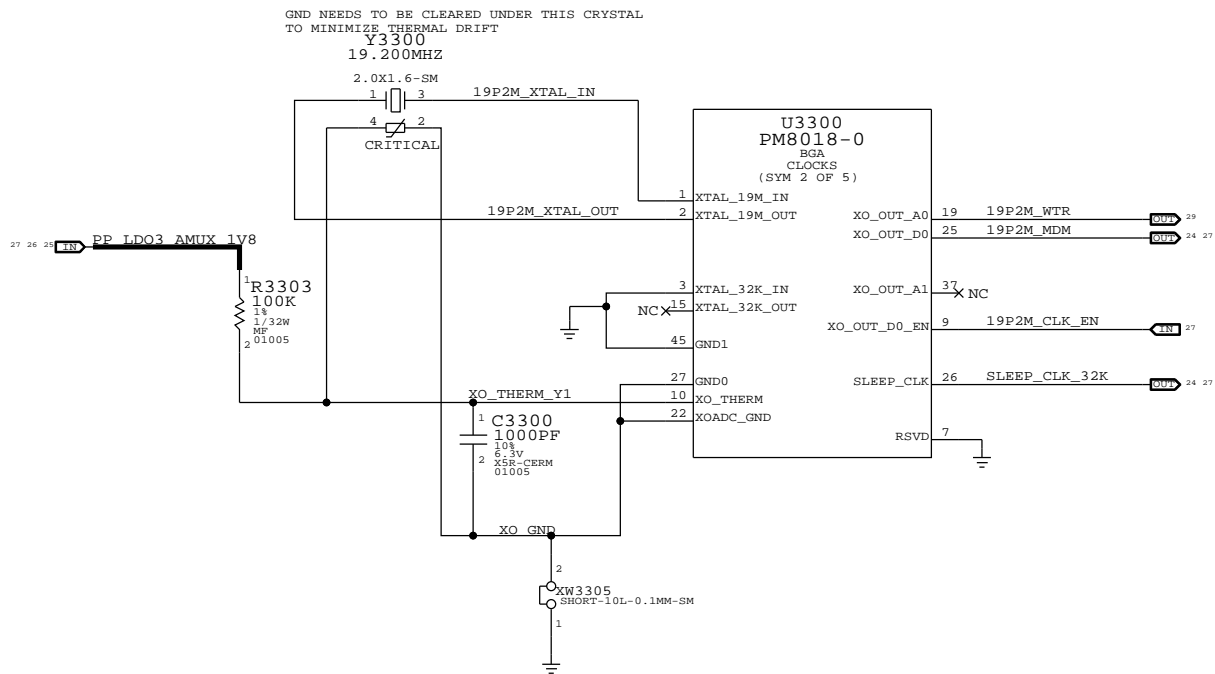
BOARD_ID	REVISION
0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT

BB GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX

PA_ID	MAV VER
0.1V	8.7
0.3V	8.6
0.5V	8.5
1.1V	7.7
1.3V	7.6
1.5V	7.5

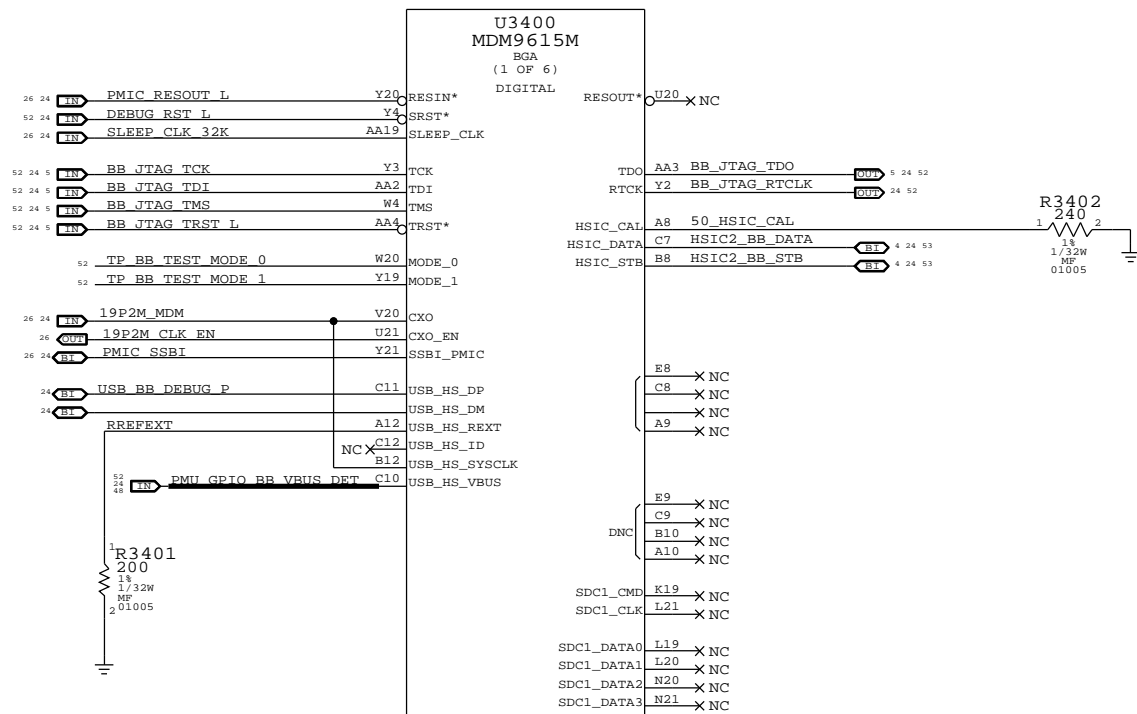
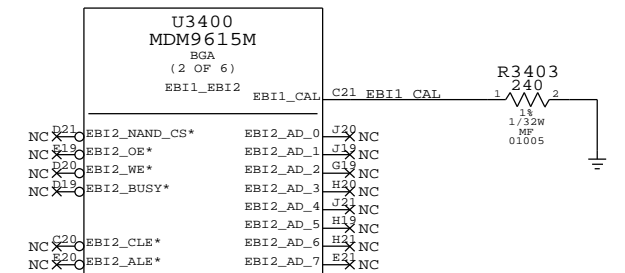
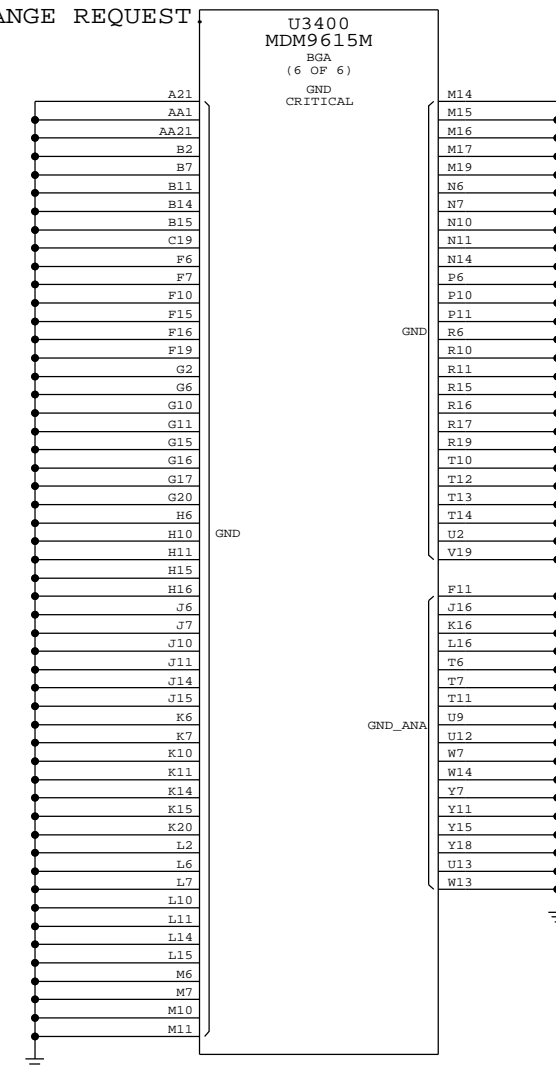
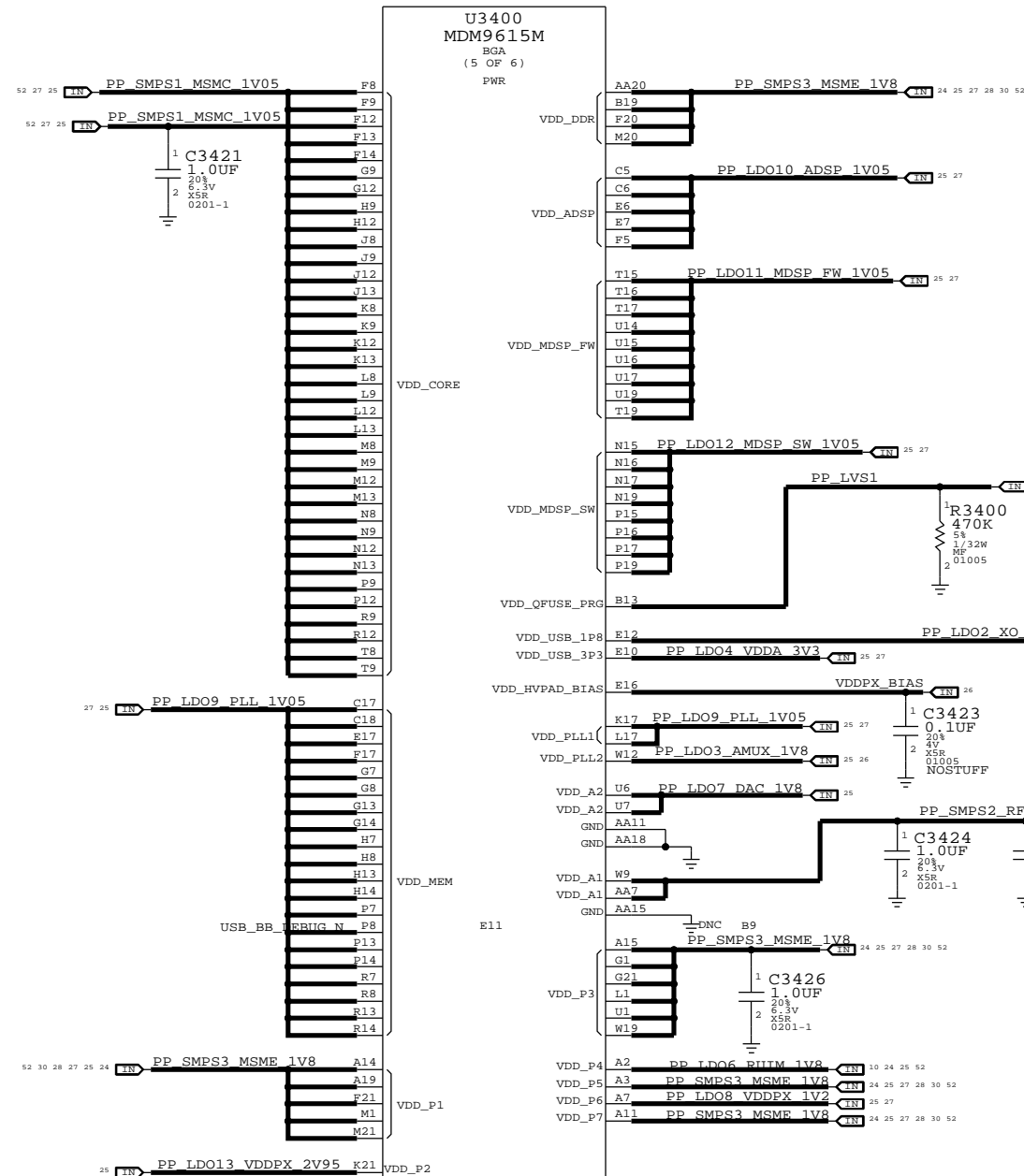


AP SECTION NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.



[illegible]

A



D

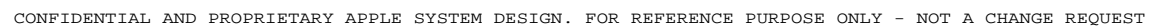
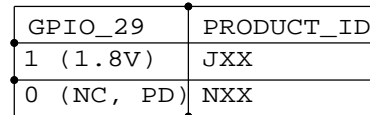
C

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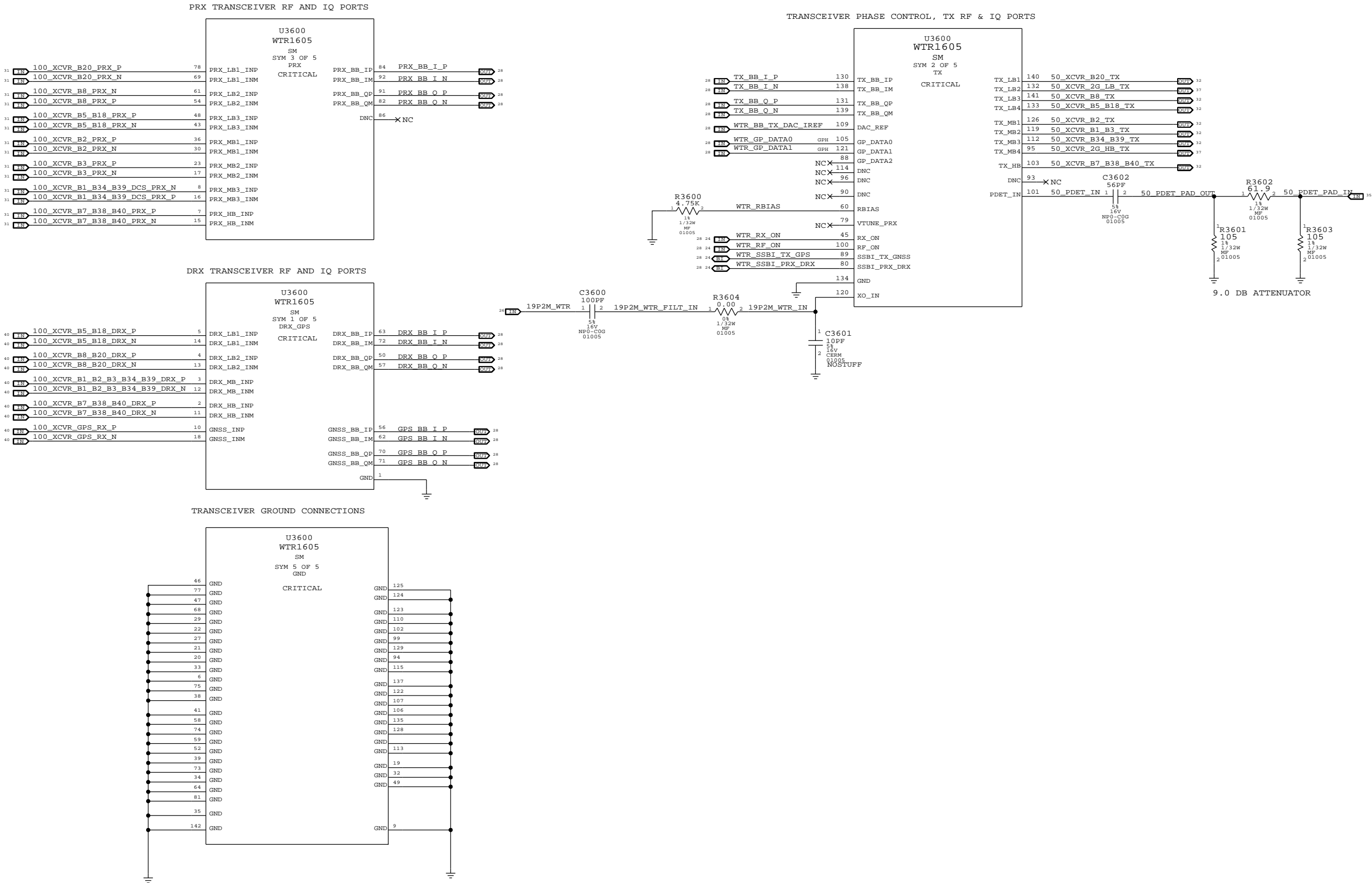


## A

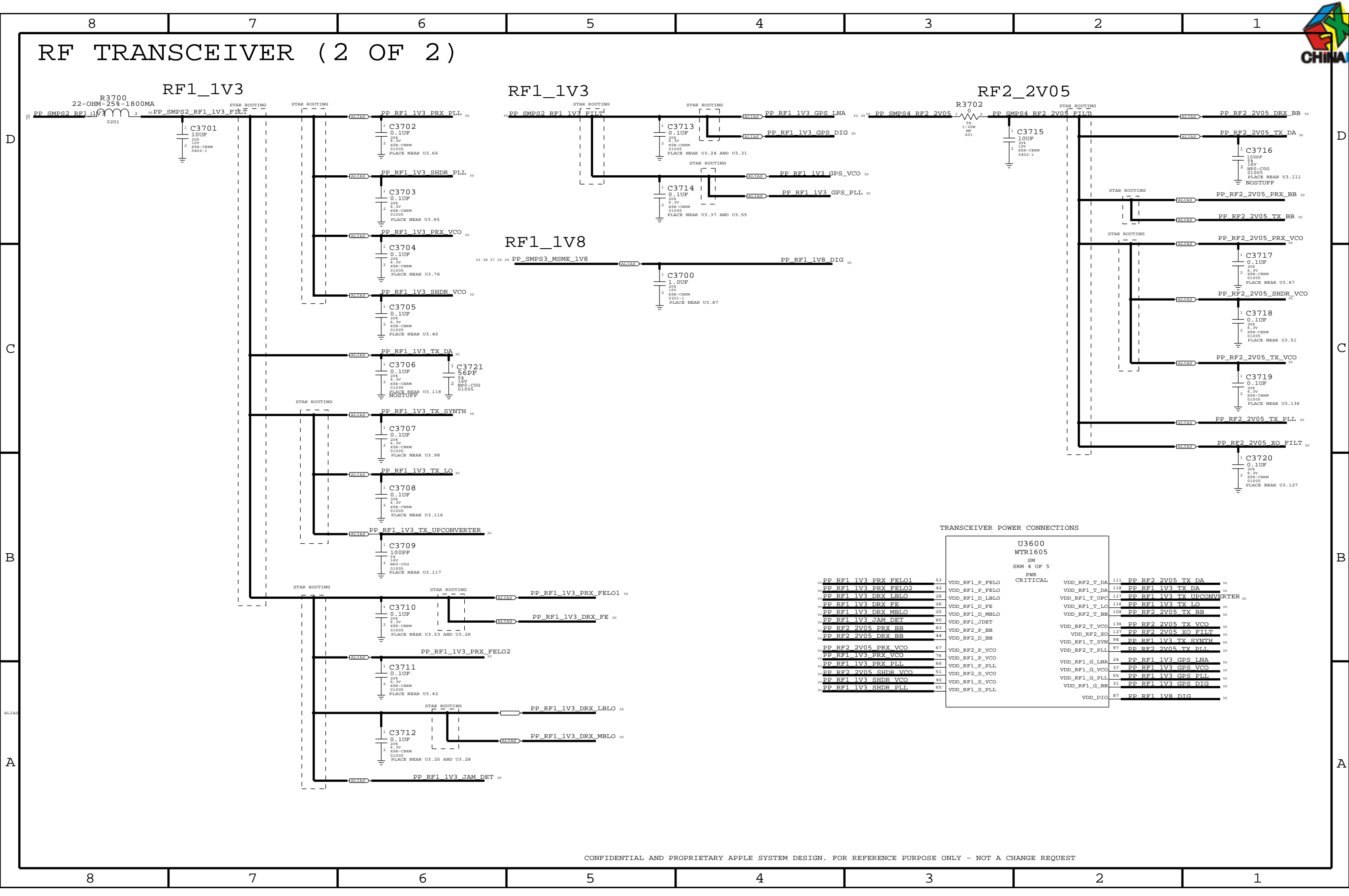




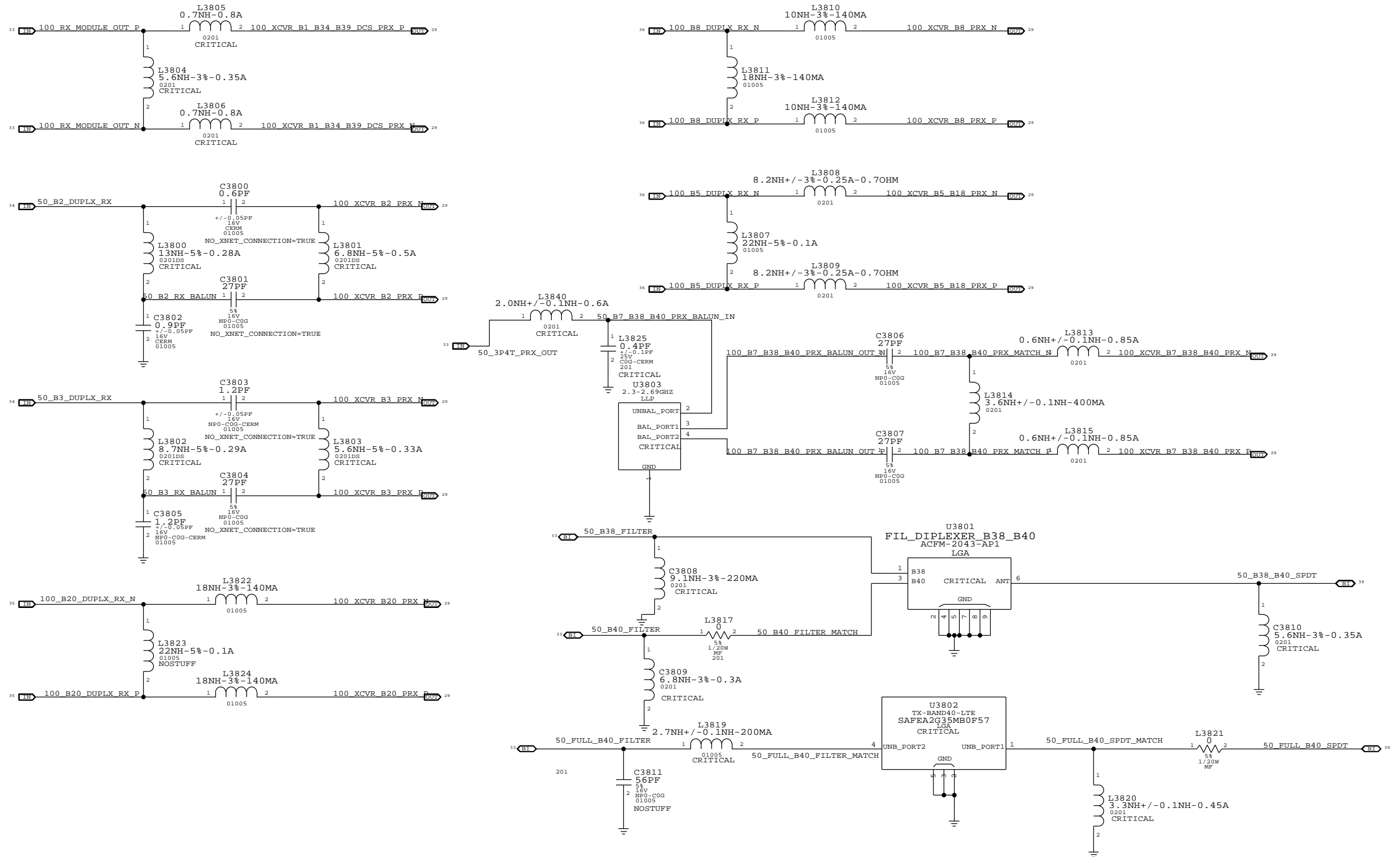
RF TRANSCEIVER (1 OF 2)





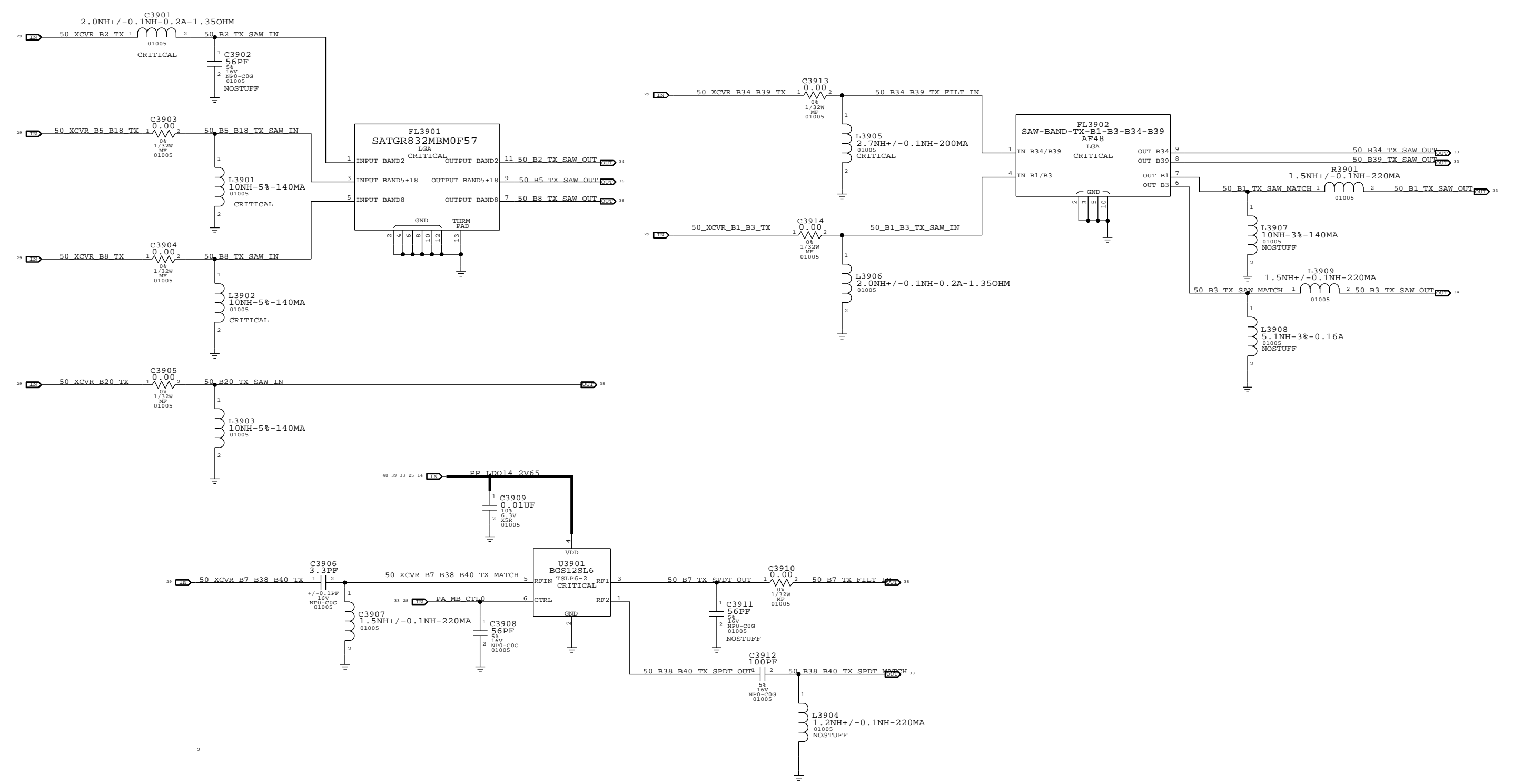


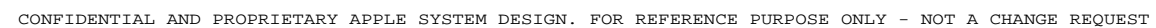
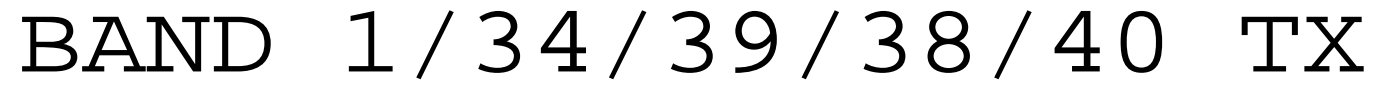
# RX MATCHING





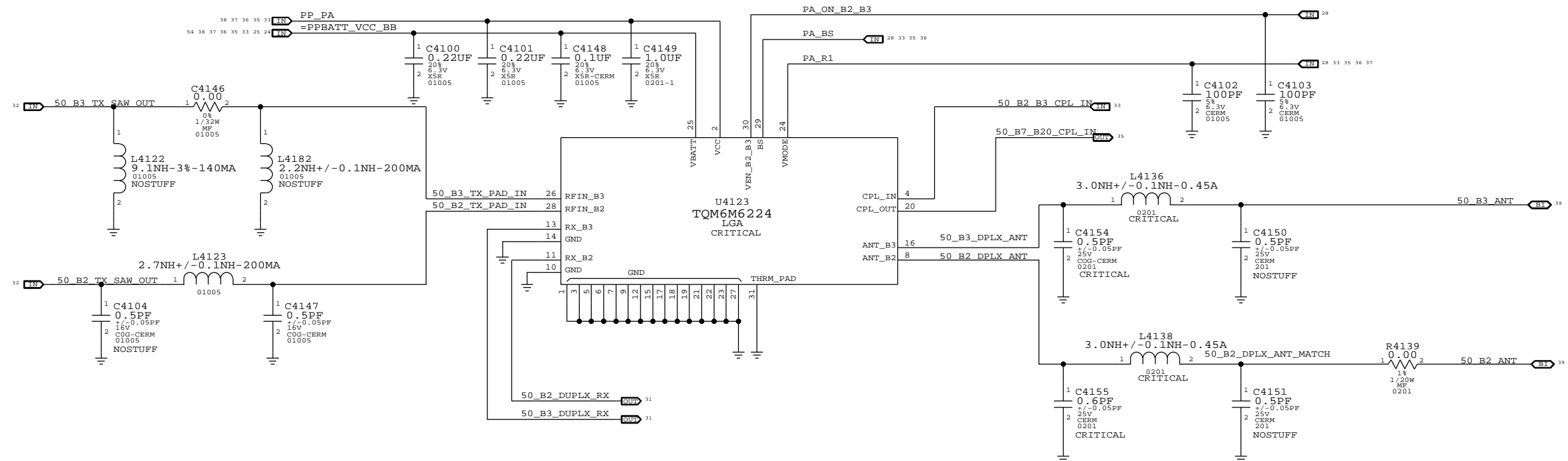
# TX INTERSTAGE FILTERS







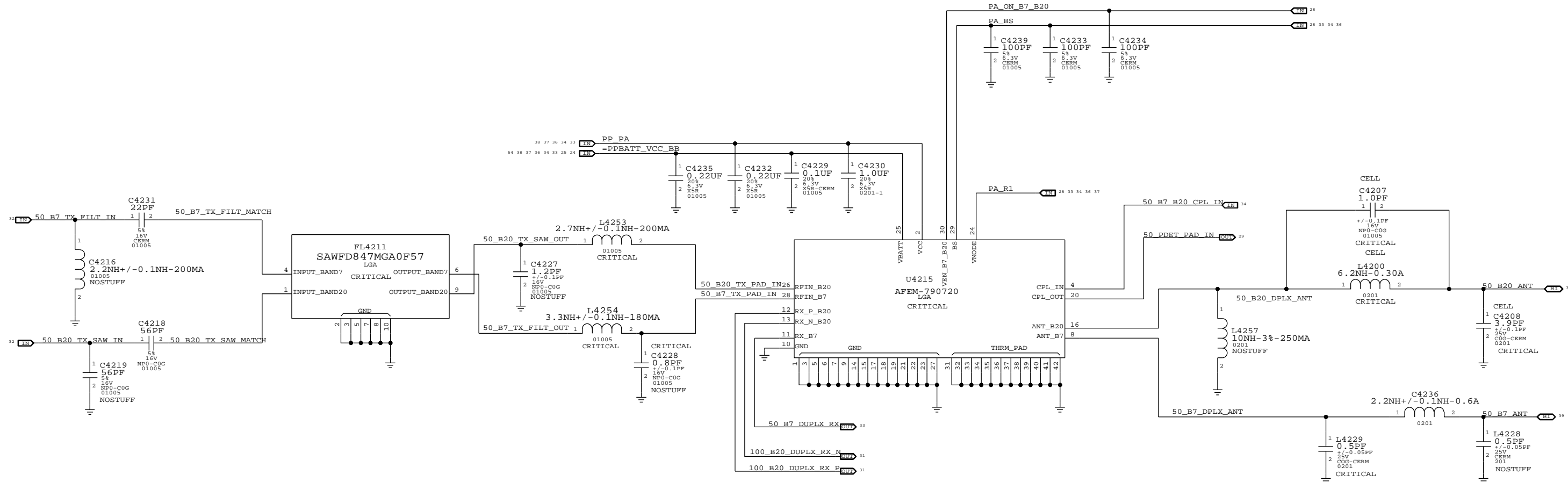
# BAND 2 / 3 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B2_B3	PA_R1
=====	=====	=====	=====	=====
OFF	X	X	0	X
B3	HPM	0	1	0
B3	LPM	0	1	1
B2	HPM	1	1	0
B2	LPM	1	1	1



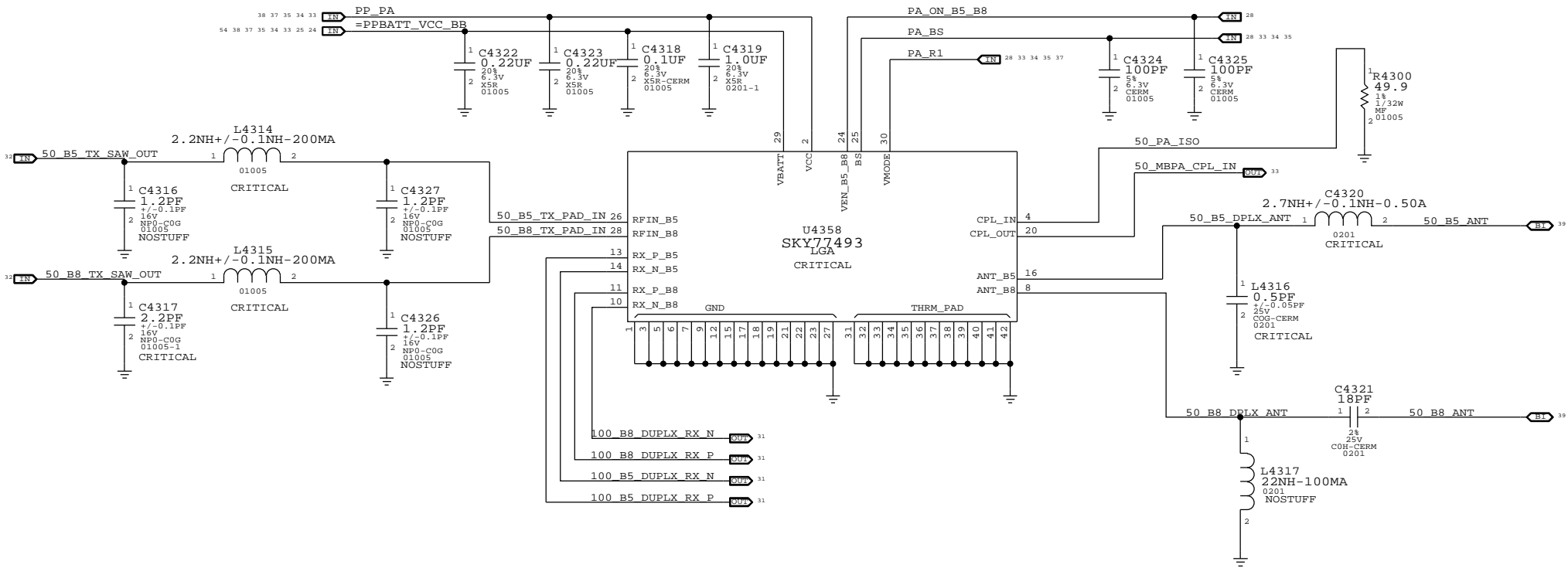
BAND 20/7 PAD



BAND	PA	POWER	MODE	PA_BS	PA_ON_B20_B7	PA_R1
OFF	X			X	0	X
B20	HPM			0	1	0
B20	LPM			0	1	1
B7	HPM			1	1	0
B7	LPM			1	1	1



BAND 5 / 8 PAD



BAND	PA	POWER	MODE	PA_BS	PA_ON_B5_B8	PA_R1
=====	=====	=====	=====	=====	=====	=====
OFF		X		X	0	X
B5		HPM		0	1	0
B5		LPM		0	1	1
B8		HPM		1	1	0
B8		LPM		1	1	1



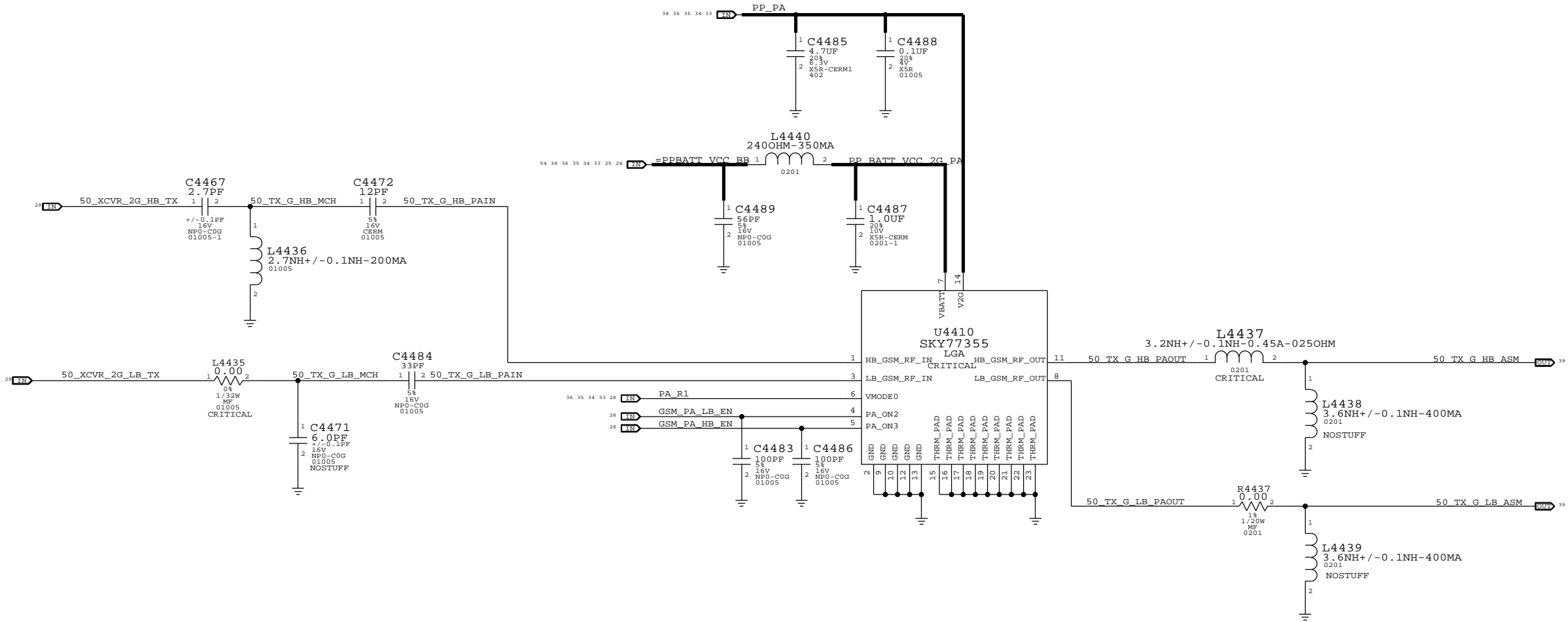


# 2G PA

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

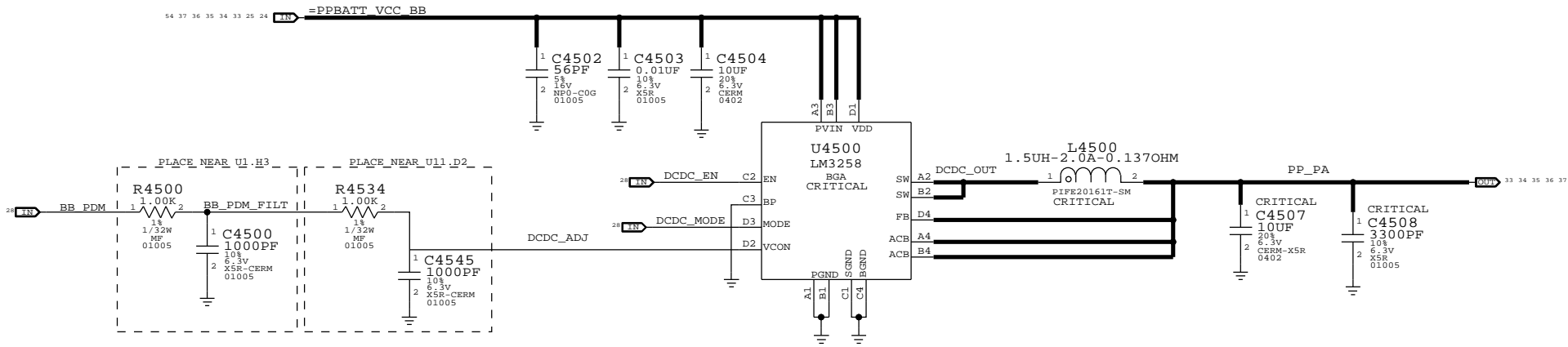
## 2G PA GAIN MODES

BAND	MODE	GAIN MODE	PA_R1	PCL RANGE
LOW BAND	GSM	ULTRA LOW	HIGH	16 TO 19
LOW BAND	GSM	LOW	HIGH	14 TO 15
LOW BAND	GSM	MEDIUM	LOW	7 TO 13
LOW BAND	GSM	HIGH	LOW	5 TO 6
HIGH BAND	GSM	ULTRA LOW	HIGH	10 TO 15
HIGH BAND	GSM	LOW	HIGH	7 TO 9
HIGH BAND	GSM	HIGH	LOW	0 TO 6
LOW BAND	EDGE	LOW	HIGH	15 TO 19
LOW BAND	EDGE	MEDIUM	LOW	10 TO 14
LOW BAND	EDGE	HIGH	LOW	8 TO 9
HIGH BAND	EDGE	LOW	HIGH	9 TO 15
HIGH BAND	EDGE	HIGH	LOW	2 TO 8



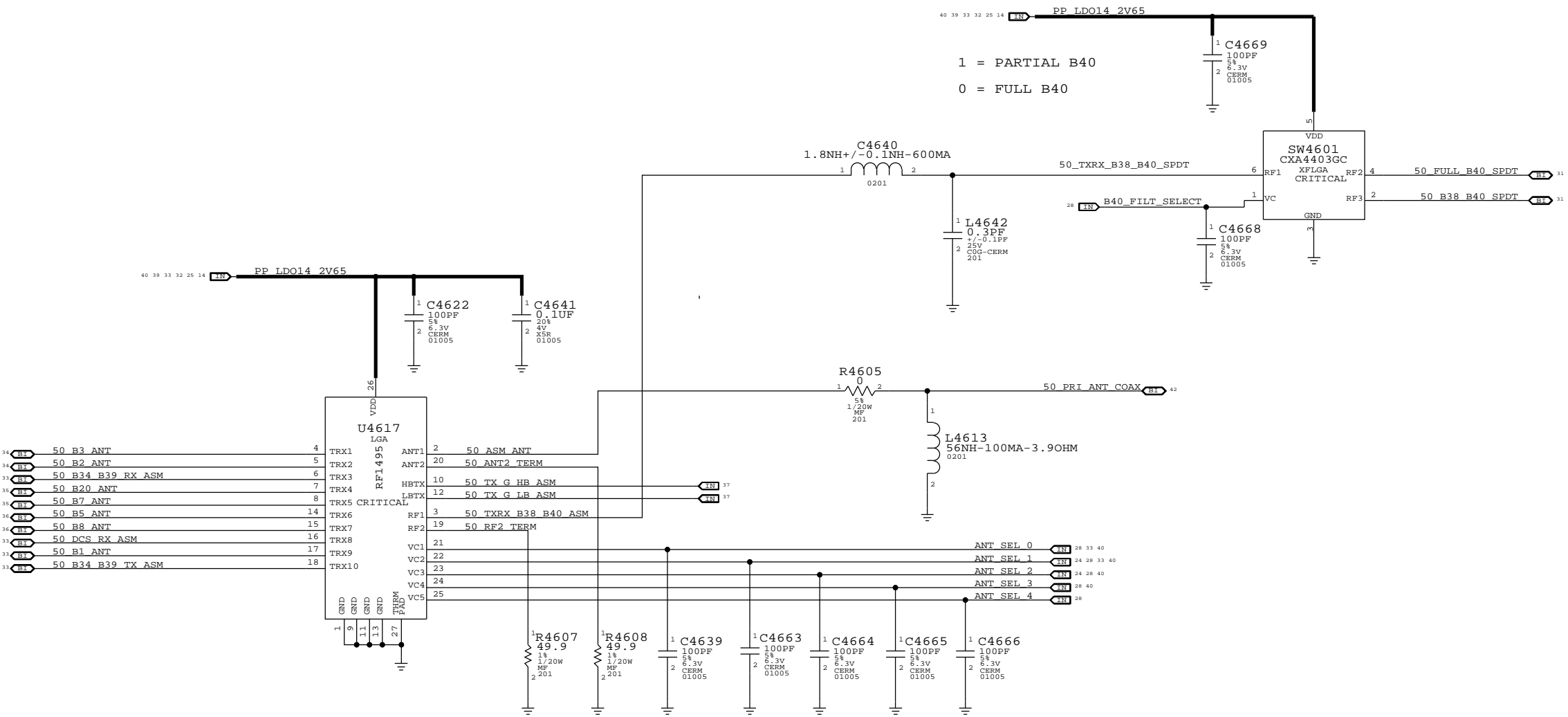


# PA DC/DC CONVERTER





# PRIMARY ASM



C

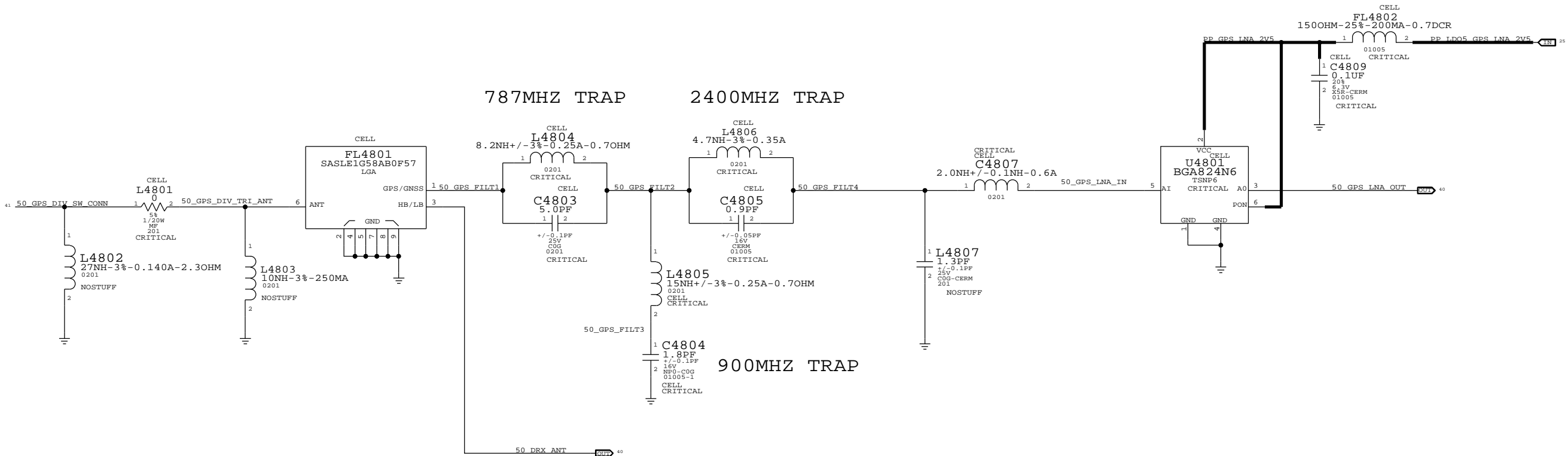
B

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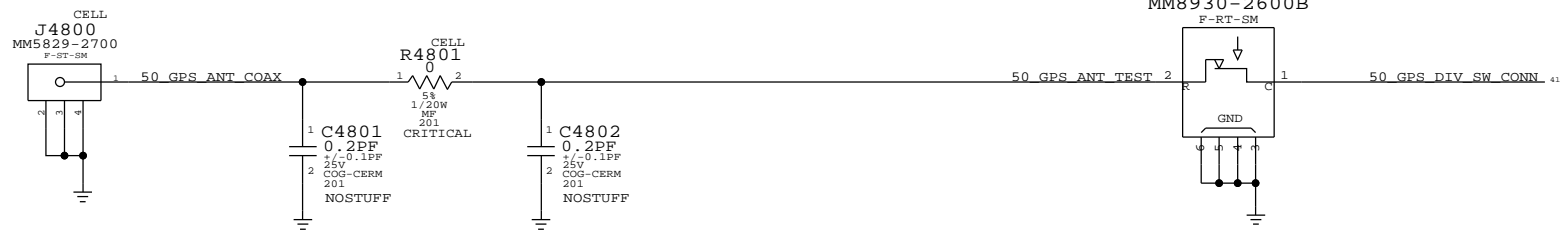


# GPS

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



## GPS\_DRX\_ANT



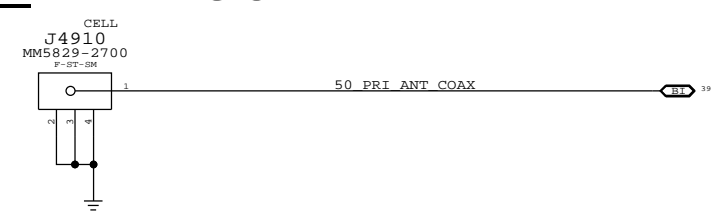
TOP MOUNT

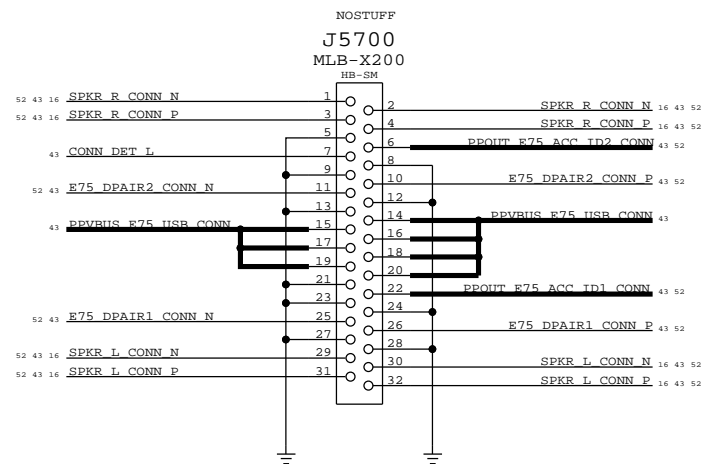
TOP MOUNT



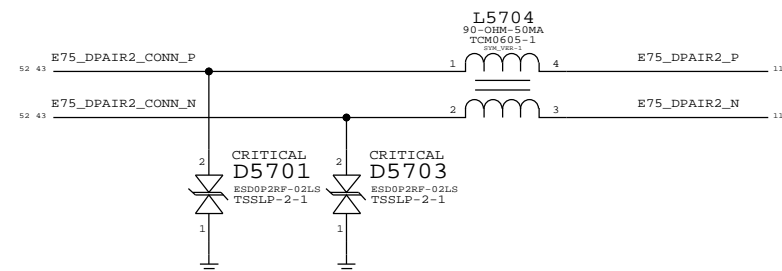
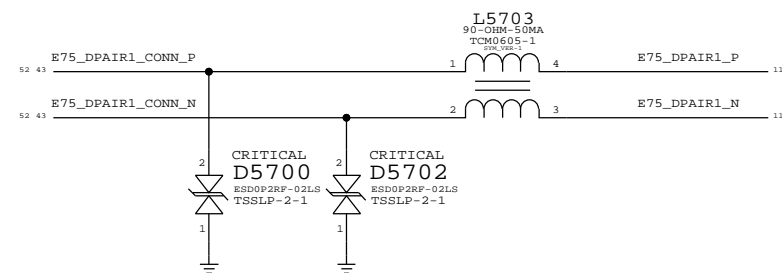
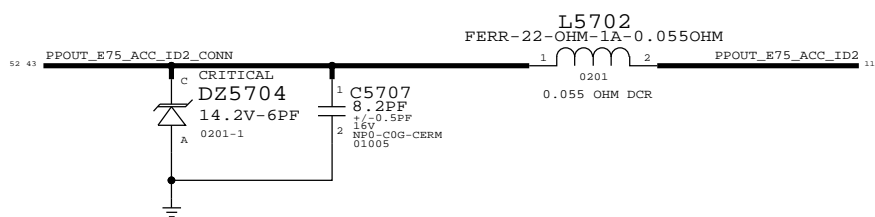
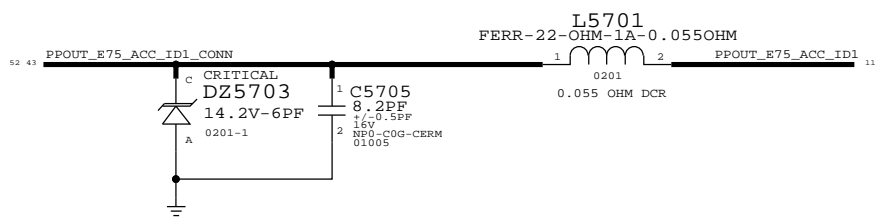
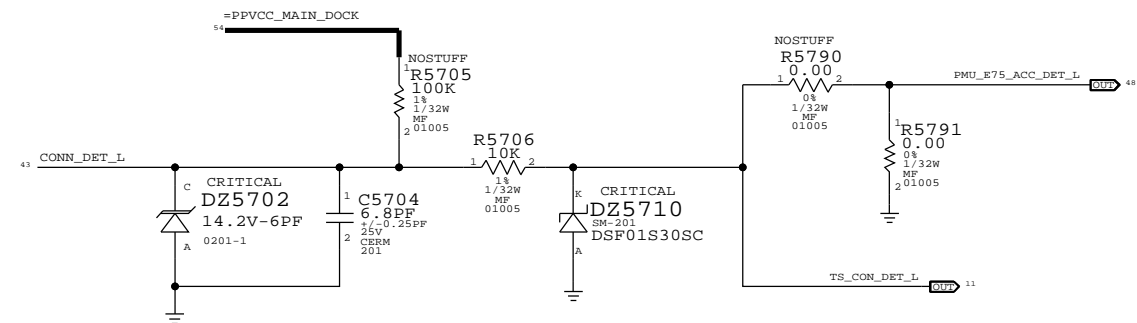
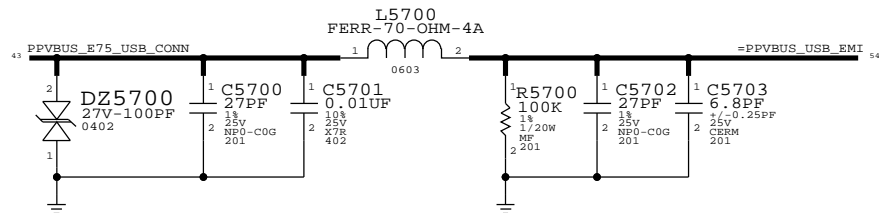
# ANTENNA FEEDS

## PRI\_ANT COAX





NOTE: SPKR\_L\_CONN\_N AND SPKR\_L\_CONN\_P WERE SWAPPED ON 5/22/12 PER RADAR #11526818

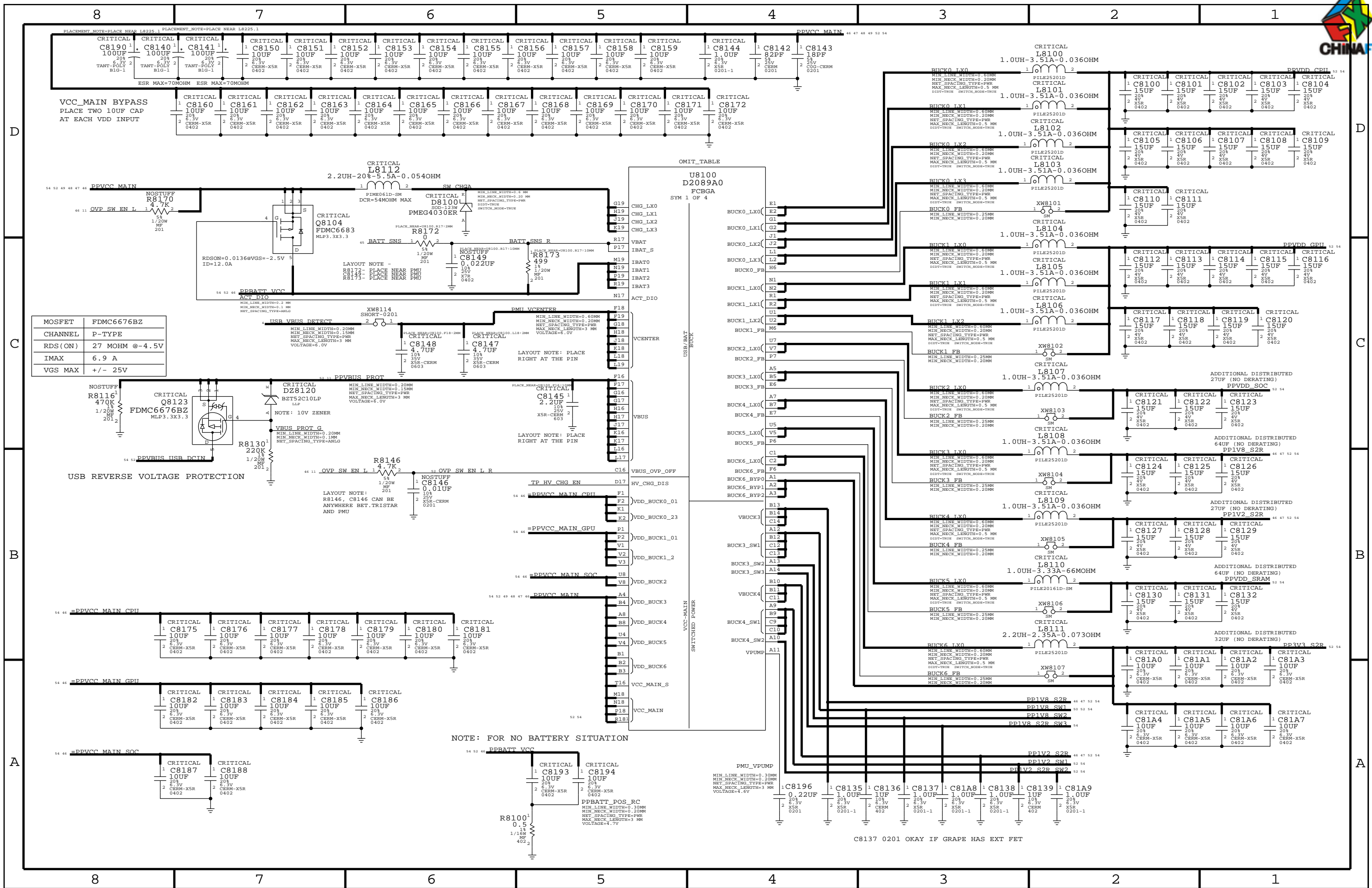


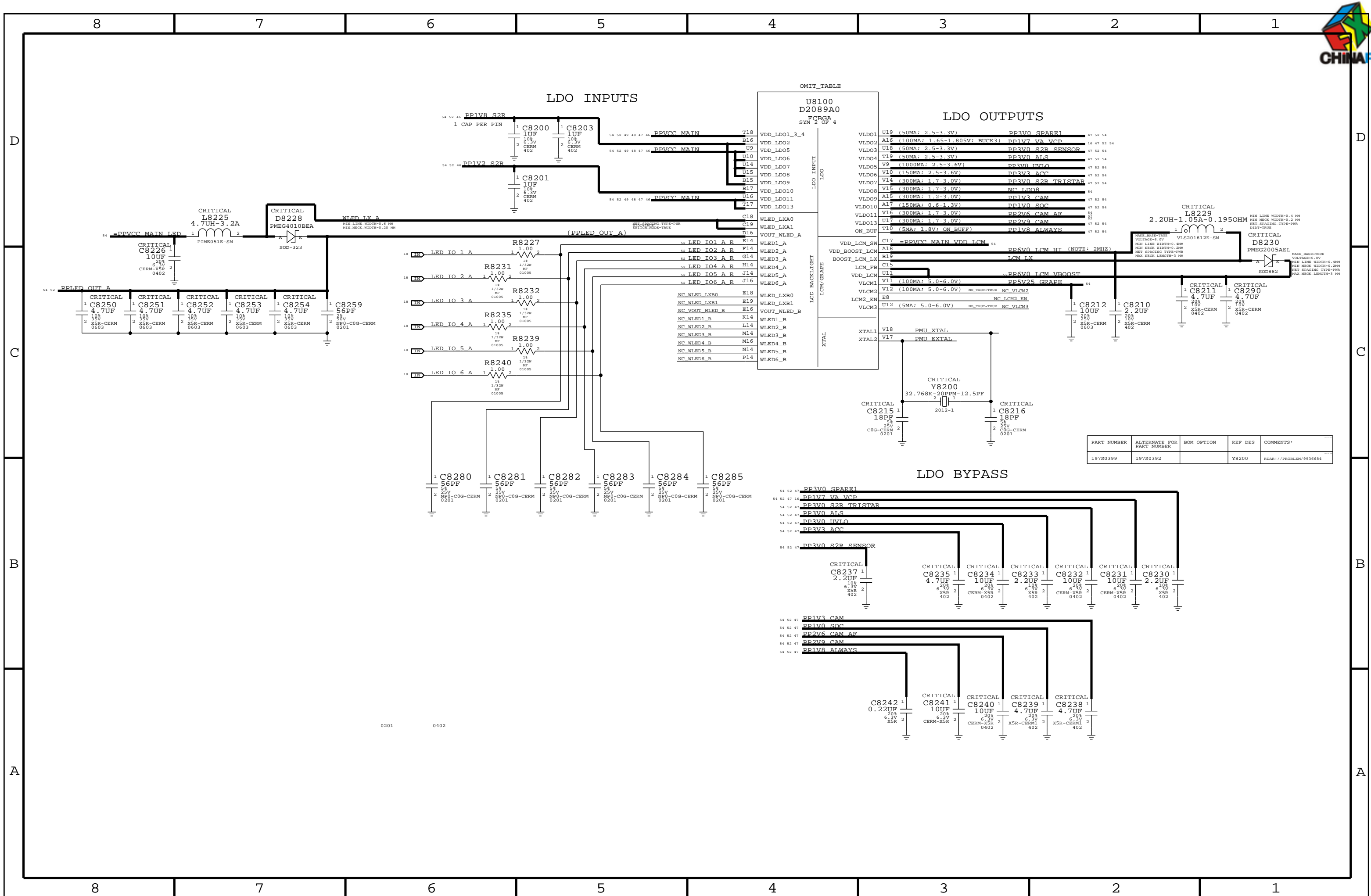


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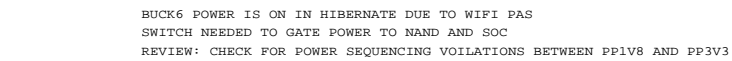






CD

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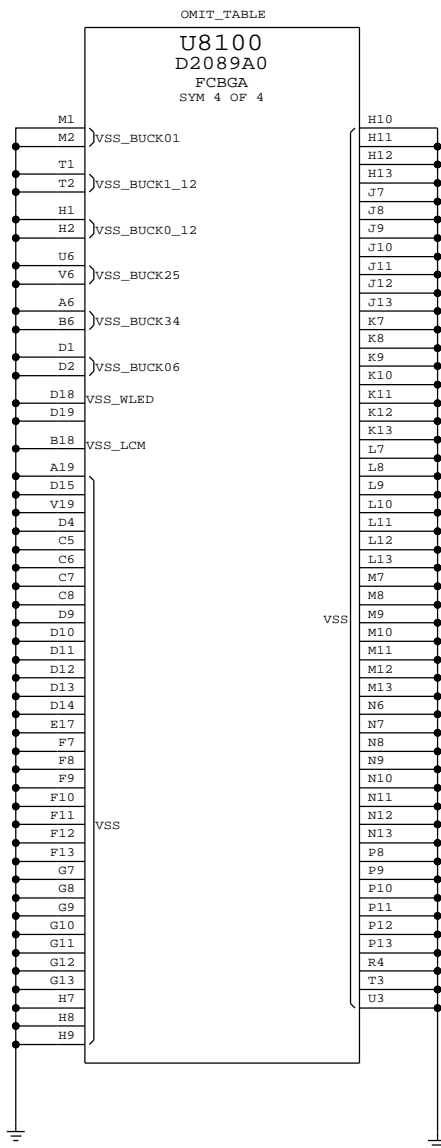
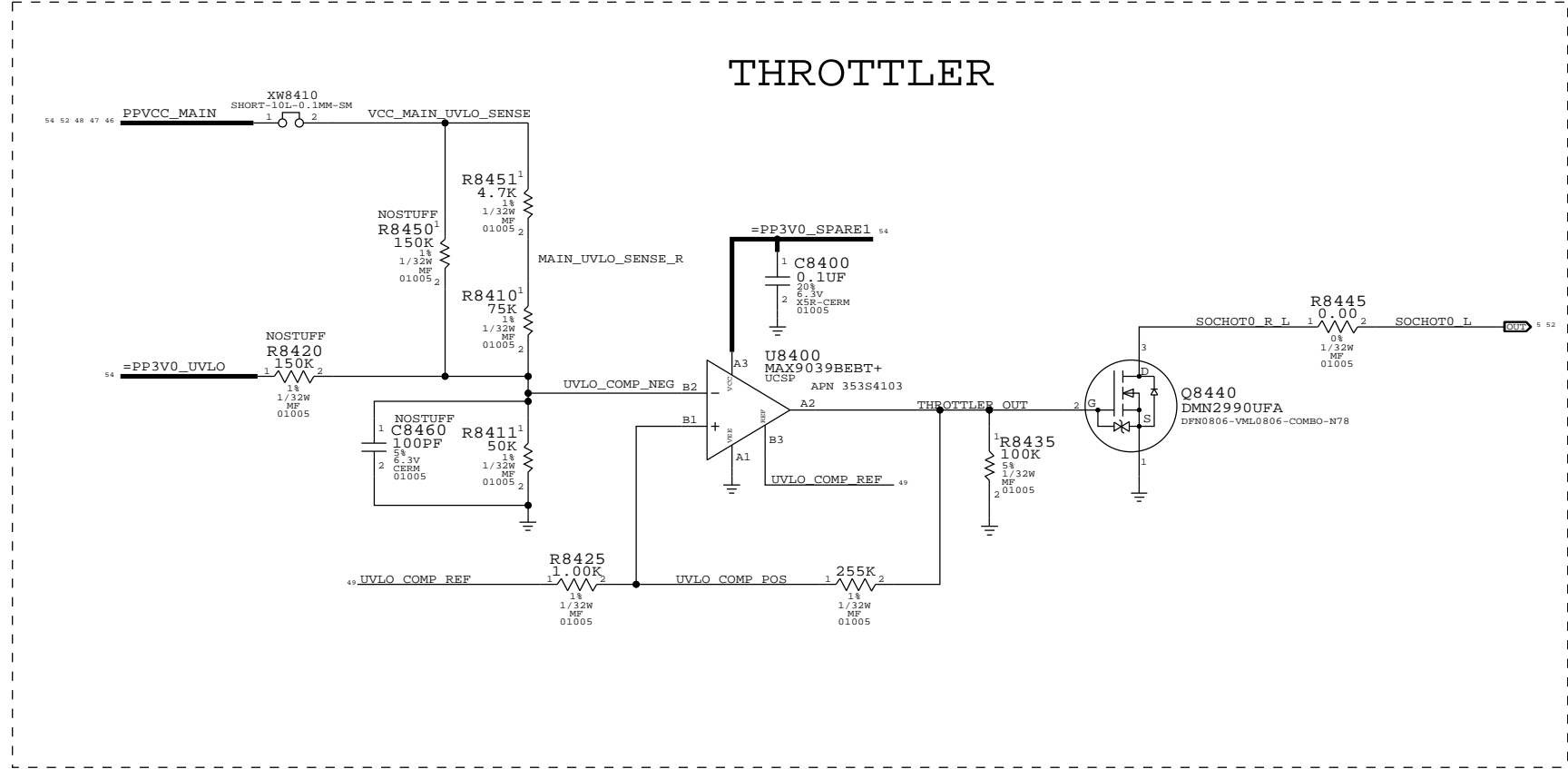
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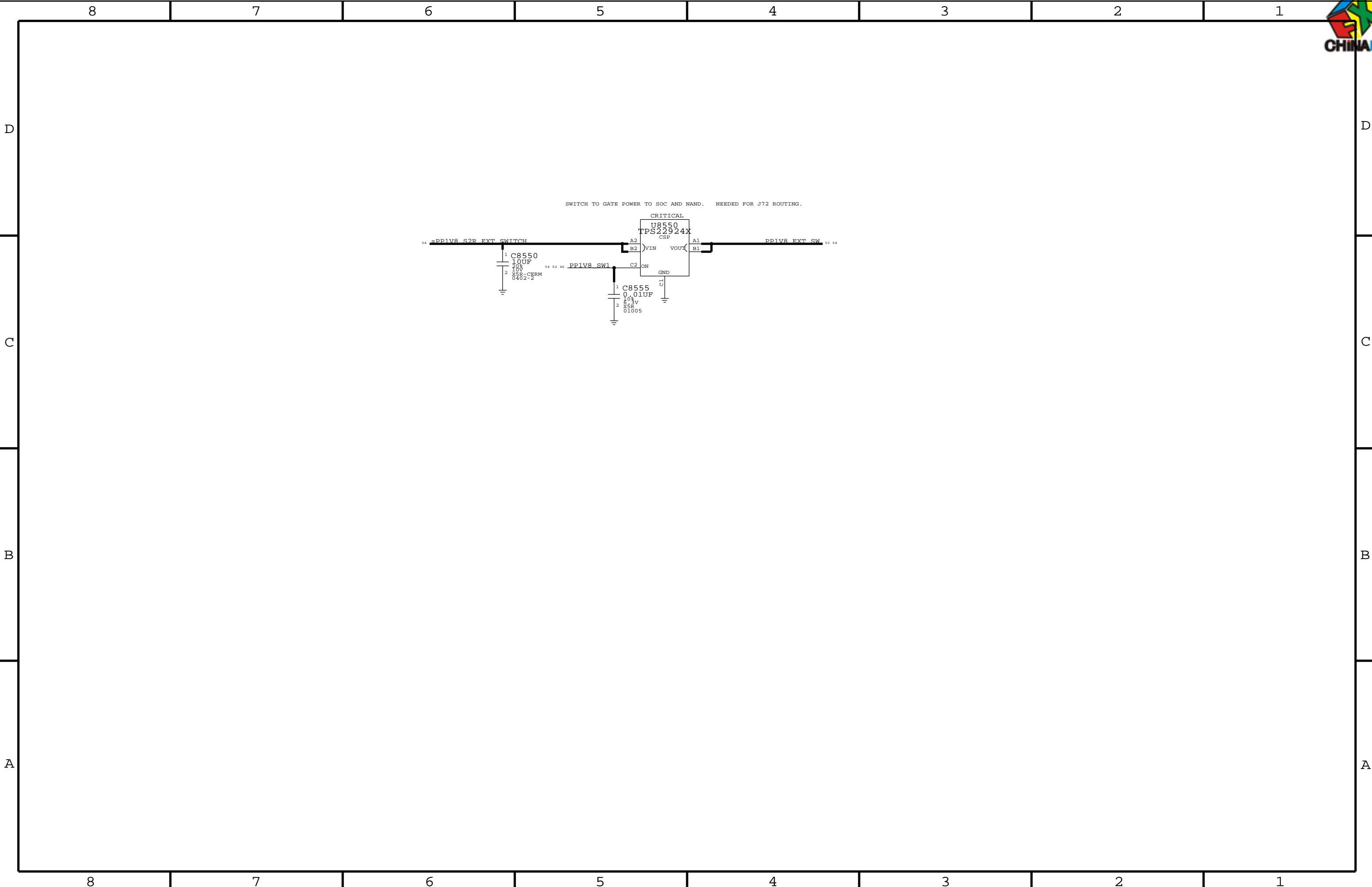
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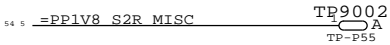


87654321

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DEBUG

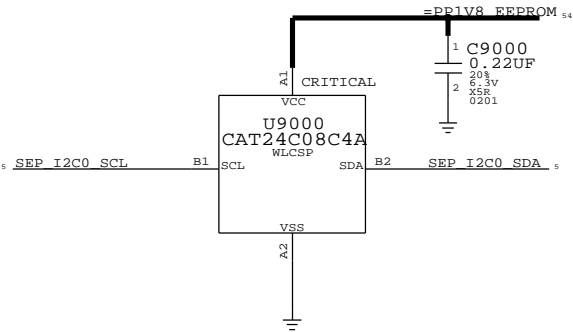


C

C

SEP EEPROM

UNPROGRAMMED P/N: 335S0894



B

B

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87654321





8	7	6	5	4	3	2	1
<div>TP9300 GPIO CODEC IRO L 5 15 A TP9304 PMU GPIO CODEC HS INT L 15 48 TP9303 BATT NTC 45 48 TP9305 PPLED OUT A 47 54 TP9396 PP3V0 UVLO 47 54 TP9397 PP3V0 SPARE1 47 54 TP9398 SOCHOT0 L 5 49 TP9312 BOARD TEMP3 P 48 A TP9313 BOARD TEMP4 P 48 TP9314 BOARD TEMP5 P 48 A TP9315 BOARD TEMP6 P 48 TP9316 BOARD TEMP7 P 48 TP9317 BOARD TEMP8 P 48 A TP9318 CLK 32K SOC2CUMULUS 5 13 TP9320 CODEC HP DET R 15 A TP9321 CODEC HP HS3 15 TP9322 CODEC HP HS3 REF 15 A TP9323 CODEC HP HS4 15 TP9324 CODEC HP HS4 REF 15 TP9325 CODEC HP LEFT 15 A TP9326 CODEC HP RIGHT 15 TP9328 DISPLAY SYNC R 13 A TP9329 DWI AP CLK 5 48 TP9330 E75 DPAIR1 CONN N 43 A TP9331 E75 DPAIR1 CONN P 43 TP9332 E75 DPAIR2 CONN N 43 A TP9333 E75 DPAIR2 CONN P 43 TP9334 FMIO CE0 L 6 12 A TP9335 FMIO CE0 L 6 12 TP9336 GND A TP9337 GND AUDIO CODEC 15 TP9338 GPIO BTN HOME FILT L 13 TP9339 GPIO BTN ONOFF L FILT 17 A TP9340 GPIO BTN SRL L FILT 17 TP9341 GPIO BTN VOL DOWN L FILT 17 A TP9342 GPIO BTN VOL UP L FILT 17 TP9343 GPIO FORCE DFU 5 A TP9344 GPIO GRAPE IRO L 5 13 TP9345 GPIO GRAPE RST L 5 13 A TP9346 GPIO SOC2BB WAKE MODEM 5 28 TP9347 GPIO SPKAMP KEEPALIVE 5 16 A TP9348 I2C0_SCL_1V8 5 11 48 TP9349 I2C0_SDA_1V8 5 11 48 A TP9350 I2C2_SCL_1V8 5 16 TP9351 I2C2_SDA_1V8 5 16 A TP9352 ISP0_CAM_REAR_CLK 7 23 TP9353 ISP0_CAM_REAR_SCL 7 23 A TP9354 ISP0_CAM_REAR_SDA 7 23 TP9355 ISP0_CAM_REAR_SHUTDOWN L 7 23 A TP9356 ISP1_CAM_FRONT_CLK 7 20 TP9357 ISP1_CAM_FRONT_SCL 7 20 A TP9358 ISP1_CAM_FRONT_SDA 7 20 TP9359 ISP1_CAM_FRONT_SHUTDOWN L 7 20 A TP9360 JTAG SOC SEL 4 10 TP9361 JTAG SOC TCK 4 11 A TP9362 JTAG SOC TDI 4 TP9363 JTAG SOC TMS 4 11 A TP9364 JTAG SOC TRST L 4 10 TP9365 JTAG WLAN SEL 44 A TP9366 OSCAR2RADIO CONTEXT A 19 28 44 TP9367 OSCAR2RADIO CONTEXT B 19 28 44 A TP9368 WLAN_TX_BLANK 28 44 TP9369 LAT_SW1_CTL 14 24 28 A TP9370 LAT_SW2_CTL 14 28 TP9371 A TP9372 LED IO1 A R 47 A TP9373 LED IO2 A R 47 TP9374 LED IO3 A R 47 A TP9375 LED IO4 A R 47 TP9376 LED IO5 A R 47 A TP9377 LED IO6 A R 47 TP9378 MIKEY_TS_N 11 15 A TP9379 MIKEY_TS_P 11 15</div>	<div>TP9380 OVP SW EN L R 46 TP9382 PMU_GPIO_BT_HOST_WAKE 44 48 TP9383 PMU_GPIO_BT_REG_ON 44 48 A TP9384 PMU_GPIO_CLK_32K_OSCAR 19 48 TP9385 PMU_GPIO_CLK_32K_WLAN 44 48 A TP9387 PMU_USB_BRICKID_R 48 TP9388 PP1V0_SOC 47 54 A TP9389 PP1V2_S2R 46 47 54 TP9390 PP1V2_S2R_SW2 46 54 A TP9391 PP1V2_SW1 46 54 TP9393 PP1V7_VA_VCP 16 47 54 A TP9395 PP1V8_ALWAYS 47 54 TP93A0 PP1V8_EXT_SW 50 54 A TP93A1 PP1V8_GRAPE_FILT 13 TP93A2 PP1V8_GRAPE_SW 13 A TP93A3 PP1V8_PLL_SOC_F 4 TP93A4 PP1V8_S2R 46 47 54 A TP93A6 PP1V8_S2R_SW3_COMP 54 TP93A7 PP1V8_SW1 46 50 54 A TP93A8 PP1V8_SW2 46 54 TP93A9 PP1V8_XTAL 8 A TP93B0 PP2V6_CAM_AF 47 54 TP93B8 PP3V0_S2R_HALL_FILT 13 TP93C0 PP3V0_S2R_SENSOR 47 54 A TP93C1 PP3V0_S2R_TRISTAR 47 54 TP93C3 PP3V3_ACC 47 54 A TP93C4 PP3V3_S2R 46 54 TP93C5 PP3V3_SW 48 54 A TP93C6 PP5V25_GRAPE_FILT 13 TP93C8 PP6V0_LCM_VBOOST 47 A TP93C9 PPBATT_VCC 46 54 TP93D0 PPLED_BACK_REG_A 18 A TP93D1 PPOUT_E75_ACC_ID1_CONN 43 TP93D2 PPOUT_E75_ACC_ID2_CONN 43 A TP93D3 PPVBUS_PROT 11 46 TP93D4 PPVBUS_USB_DCIN 46 54 A TP93D5 PPVCC_MAIN 46 47 48 49 54 TP93D6 PPVCC_MAIN_LCD_SW_CONN 18 A TP93D7 PPVDD_CPU 46 54 TP93D8 PPVDD_GPU 46 54 A TP93D9 PPVDD_SOC 46 54 TP93E0 PPVDD_SRAM 46 54</div>	<div>TP93G4 PP_SMPS4_RF2_2V05 25 30 TP93G9 SOC_TESTMODE 4 10 TP93H1 SPI1_GRAPE_CS_L 5 13 A TP93H2 SPI1_GRAPE_MISO 5 13 TP93H3 SPI1_GRAPE_MOSI 5 13 A TP93H4 SPI1_GRAPE_SCLK_R 13 TP93H5 SPKR_L_CONN_N 16 43 A TP93H6 SPKR_L_CONN_P 16 43 TP93H7 SPKR_R_CONN_N 16 43 A TP93H8 SPKR_R_CONN_P 16 43 TP93I1 TP_JTAG_SOC_TDO 4 A TP93I2 TP_JTAG_WLAN_TCK 44 TP93I3 TP_JTAG_WLAN_TRST_L 44 A TP93I4 UART0_SOC_RXD 5 11 TP93I5 UART0_SOC_TXD 5 11 A TP93I6 UART3_BB2SOC_TX 5 11 24 28 TP93I7 UART3_SOC2BB_TX 5 11 24 28 A TP93I8 UART6_TS_ACC_RXD 5 11 TP93I9 UART6_TS_ACC_TXD 5 11 A TP93J0 USB_SOC_N 4 11 TP93J1 USB_SOC_P 4 11 TP93J9 PP3V0_ALS 47 54 A TP93JA PP2V9_CAM 47 54 TP93JB PP1V3_CAM 47 54 A TP93JC PMU_GPIO_WLAN_REG_ON 44 48</div>	<div>RF TEST POINTS TP93G1 PP_SMPS1_MSMC_1V05 25 27 A TP93G2 PP_SMPS3_MSME_1V8 24 25 27 28 30 TP93G5 PP_SMPS5_DSP_1V05 25 A TP93H1 PP_LDO1 25 TP93H2 TP_BB_TEST_MODE_0 27 A TP93I0 TP_BB_TEST_MODE_1 27 TP93J0 SIMCRD_RST_CONN 10 24 28 A TP93J8 SIMCRD_CLK_CONN 10 24 28 TP93J7 SIMCRD_IO_CONN 10 24 28 A TP93J8 SIM_TRAY_DETECT 10 24 28 TP93F3 PP_LDO6_RUIM_1V8 10 24 25 27 A TP93J2 GPIO_SOC2BB_RADIO_ON_L 5 24 26 TP93J3 GPIO_SOC2BB_RST_L 5 24 26 A TP93J4 PMU_GPIO_PU2BBPMU_RST_L 24 26 48 TP9381 PMU_GPIO_BB2PMU_HOST_WAKE 24 28 48 A TP93J5 PS_HOLD_PMIC 24 26 TP9327 DEBUG_RST_L 24 27 A TP9306 BB_JTAG_RTCLK 24 27 TP9307 BB_JTAG_TCK 5 24 27 A TP9308 BB_JTAG_TDI 5 24 27 TP9309 BB_JTAG_TDO 5 24 27 A TP9310 BB_JTAG_TMS 5 24 27 TP9311 BB_JTAG_TRST_L 5 24 27 A TP93J6 USB_BB_N 11 24 53 TP93J7 USB_BB_P 11 24 53 A TP93G6 RESET_SOC_L 4 8 10 11 24 48 TP93J8 PMU_GPIO_BB_VBUS_DET 24 27 48</div>	<div>STANDOFFS: P/N 860-1657 STD9300 STDOFF-3.3X1.8R1.28H-SM STD9301 STDOFF-3.3X1.8R1.28H-SM STANDOFF: P/N 860-1683 STD9302 STDOFF-3.3X2.2R1.35H-SM-1 PLATED THROUGH HOLES DRILL SIZE: 1.1MM X 0.4MM PLATING SIZE: 1.4MM X 0.7MM SL9300 TH-NSP SL-1.1X0.4-1.4X0.7 SL9303 TH-NSP SL-1.1X0.4-1.4X0.7 SL9304 TH-NSP SL-1.1X0.4-1.4X0.7 SL9305 TH-NSP SL-1.1X0.4-1.4X0.7 MH9300 3P25R2P5 860-1688 MH9302 WASHER-BTN-MLB-X221 TH NEAR BUTTON FLEX CONN</div>			





87654321

EE CHARACTERIZATION TP

FOR FRANK (SEG)

PP9450 1 PPVDD SOC SOC SENSE PLACE\_NEAR=U0652.V31:1MM  
P4MM SN  
PP9451 1 PPVDD CPU SOC SENSE PLACE\_NEAR=U0652.AN30:1MM  
P4MM SN

NAND

PP9401 1 FMI0\_DQS PLACE\_SIDE=BOTTOM PLACE\_NEAR=U0652.D34:2MM 4 12 53  
P4MM SN  
PP9402 1 FMI0\_AD<3> PLACE\_SIDE=BOTTOM PLACE\_NEAR=U0652.C34:2MM 6 12  
P4MM SN  
PP9403 1 FMI0\_DQS PLACE\_NEAR=U0652.D34:2MM 4 12 53  
P4MM SN  
PP9410 1 TP\_TCKC\_U1400 12  
P4MM SN  
PP9411 1 TP\_TM5C\_U1400 12  
P4MM SN  
PP9412 1 TP\_U1400\_RB0 12  
P4MM SN  
PP9413 1 TP\_U1400\_RB1 12  
P4MM SN

DWI

PP9405 1 DWI\_AP\_DO PLACE\_SIDE=BOTTOM PLACE\_NEAR=U8100:2MM 5 48  
P4MM SN

AUDIO

PP9406 1 I2S0\_CODEC\_ASP\_MCK PLACE\_NEAR=U1900:2MM 5 15  
P4MM SN

PP9416 1 I2S2\_CODEC\_XSP\_LRCK PLACE\_NEAR=U1900:2MM 5 15  
P4MM SN  
PP9417 1 I2S2\_CODEC\_XSP\_DOUT PLACE\_NEAR=U1900:2MM 5 15  
P4MM SN

PP9419 1 I2S1\_SPKAMP\_MCK PLACE\_NEAR=U2040:2MM 5 16  
P4MM SN  
PP9420 1 I2S1\_SPKAMP\_BCLK PLACE\_NEAR=U2040:2MM 5 16  
P4MM SN  
PP9421 1 I2S1\_SPKAMP\_LRCK PLACE\_NEAR=U2040:2MM 5 16  
P4MM SN  
PP9422 1 I2S1\_SPKAMP\_DOUT PLACE\_NEAR=U2040:2MM 5 16  
P4MM SN  
PP9423 1 I2S1\_SPKAMP\_DIN PLACE\_SIDE=BOTTOM PLACE\_NEAR=U0652:2MM 5 16  
P4MM SN

PP9424 1 SPI2\_CODEC\_SCLK PLACE\_NEAR=U1900:2MM 5 15  
P4MM SN  
PP9425 1 SPI2\_CODEC\_MOSI PLACE\_NEAR=U1900:2MM 5 15  
P4MM SN  
PP9426 1 SPI2\_CODEC\_MISO PLACE\_SIDE=BOTTOM PLACE\_NEAR=U0652:2MM 5 15  
P4MM SN

GRAPE

OSCAR

PP9428 1 UART4\_SOC2OSCAR\_TXD PLACE\_SIDE=BOTTOM PLACE\_NEAR=U2400:2MM 5 19  
P4MM SN  
PP9429 1 UART4\_OSCAR2SOC\_RXD PLACE\_SIDE=BOTTOM PLACE\_NEAR=U0652:2MM 5 19  
P4MM SN

UART5

WIFI

PP9480 1 HSIC1\_WLAN2SOC\_DEVICE\_RDY 5 44  
P4MM SN  
PP9481 1 HSIC1\_WLAN2SOC\_REMOTE\_WAKE 5 44  
P4MM SN  
PP9482 1 PMU\_GPIO\_WLAN\_HOST\_WAKE 44 48  
P4MM SN  
PP9483 1 HSIC1\_SOC2WLAN\_HOST\_RDY 5 44  
P4MM SN

GPIO\_BT\_WAKE FUNC\_TEST=TRUE 5 44

FOR HSIC CHARACTERIZATION

PP9460 1 HSIC1\_WLAN\_DATA PLACE\_NEAR=U0652.AN33:3MM 4 44 53  
P4MM SN

PP9462 1 HSIC1\_WLAN\_DATA PLACE\_NEAR=U5800.13:3MM 4 44 53  
P4MM SN  
PP9463 1 HSIC1\_WLAN\_STB PLACE\_NEAR=U5800.14:3MM 4 44  
P4MM SN

PP9468 1 UART1\_BT2SOC\_TX PLACE\_NEAR=U0652:3MM 5 44  
P4MM SN  
PP9469 1 UART1\_SOC2BT\_TX PLACE\_NEAR=U5800:3MM 5 44  
P4MM SN

PP9471 1 UART2\_WLAN2SOC\_TX PLACE\_NEAR=U0652:3MM 5 44  
P4MM SN  
PP9472 1 UART2\_SOC2WLAN\_TX PLACE\_NEAR=U5800:3MM 5 44  
P4MM SN

BASEBAND

USB\_BB\_P FUNC\_TEST=TRUE 11 24 52  
USB\_BB\_N FUNC\_TEST=TRUE 11 24 52

FOR HSIC CHARACTERIZATION

PP9465 1 HSIC2\_BB\_STB PLACE\_NEAR=U0652.B27:3MM 4 24 27  
P4MM SN  
PP9466 1 HSIC2\_BB\_DATA PLACE\_NEAR=U3400.C7:3MM 4 24 27  
P4MM SN

PROX

HIGH SPEED, NO TEST

MIPI0C\_CAM\_REAR\_CLK\_P NO\_TEST=TRUE 7 23 53  
MIPI0C\_CAM\_REAR\_CLK\_N NO\_TEST=TRUE 7 23 53  
MIPI0C\_CAM\_REAR\_DATA\_P<0..3> NO\_TEST=TRUE 7 23 53  
MIPI0C\_CAM\_REAR\_DATA\_N<0..3> NO\_TEST=TRUE 7 23 53  
MIPI0C\_CAM\_REAR\_CLK\_FILT\_P NO\_TEST=TRUE 23  
MIPI0C\_CAM\_REAR\_CLK\_FILT\_N NO\_TEST=TRUE 23  
MIPI0C\_CAM\_REAR\_DATA\_FILT\_P<0..3> NO\_TEST=TRUE 23  
MIPI0C\_CAM\_REAR\_DATA\_FILT\_N<0..3> NO\_TEST=TRUE 23  
MIPI1C\_CAM\_FRONT\_CLK\_P NO\_TEST=TRUE 7 20 53  
MIPI1C\_CAM\_FRONT\_CLK\_N NO\_TEST=TRUE 7 20 53  
MIPI1C\_CAM\_FRONT\_DATA\_P<0> NO\_TEST=TRUE 7 20 53  
MIPI1C\_CAM\_FRONT\_DATA\_N<0> NO\_TEST=TRUE 7 20 53  
MIPI1C\_CAM\_FRONT\_CLK\_FILT\_P NO\_TEST=TRUE 20  
MIPI1C\_CAM\_FRONT\_CLK\_FILT\_N NO\_TEST=TRUE 20  
MIPI1C\_CAM\_FRONT\_DATA\_FILT\_P<0> NO\_TEST=TRUE 20  
MIPI1C\_CAM\_FRONT\_DATA\_FILT\_N<0> NO\_TEST=TRUE 20  
EDP\_DATA\_P<0..3> NO\_TEST=TRUE 7 18  
EDP\_DATA\_N<0..3> NO\_TEST=TRUE 7 18  
EDP\_DATA\_EMI\_P<0..3> NO\_TEST=TRUE 18  
EDP\_DATA\_EMI\_N<0..3> NO\_TEST=TRUE 18  
EDP\_DATA\_EMI\_CONN\_P<0..3> NO\_TEST=TRUE 18  
EDP\_DATA\_EMI\_CONN\_N<0..3> NO\_TEST=TRUE 18

1145

CAMERA

PP9440 1 MIPI1C\_CAM\_FRONT\_CLK\_P PLACE\_NEAR=U0652.AR33:3MM 7 20 53  
P4MM SN  
PP9441 1 MIPI1C\_CAM\_FRONT\_CLK\_N PLACE\_NEAR=U0652.AR34:3MM 7 20 53  
P4MM SN  
PP9442 1 MIPI1C\_CAM\_FRONT\_DATA\_P<0> PLACE\_NEAR=U0652.AT33:3MM 7 20 53  
P4MM SN  
PP9443 1 MIPI1C\_CAM\_FRONT\_DATA\_N<0> PLACE\_NEAR=U0652.AT34:3MM 7 20 53  
P4MM SN  
PP9444 1 MIPI0C\_CAM\_REAR\_CLK\_P PLACE\_NEAR=U0652.AU25:3MM 7 23 53  
P4MM SN  
PP9445 1 MIPI0C\_CAM\_REAR\_CLK\_N PLACE\_NEAR=U0652.AV25:3MM 7 23 53  
P4MM SN  
PP9446 1 MIPI0C\_CAM\_REAR\_DATA\_P<0> PLACE\_NEAR=U0652.AU27:3MM 7 23 53  
P4MM SN  
PP9447 1 MIPI0C\_CAM\_REAR\_DATA\_N<0> PLACE\_NEAR=U0652.AV27:3MM 7 23 53  
P4MM SN

87654321



# POWER CONNECTIONS

## BUCK0

52 46 PPVDD\_CPU == =PPVDD\_CPU 9  
MAKE\_BASE=TRUE

## BUCK1

52 46 PPVDD\_GPU == =PPVDD\_GPU 9  
MAKE\_BASE=TRUE

## BUCK2

52 46 PPVDD\_SOC == =PPVDD\_SOC 9  
MAKE\_BASE=TRUE

## BUCK3

52 47 46 PP1V8\_S2R == =PP1V8\_S2R\_MISC 5 51  
MAKE\_BASE=TRUE == =PP1V8\_S2R\_VDDIO\_WLAN\_BT 44  
== =PP1V8\_S2R\_TRISTAR 11  
== =PP1V8\_S2R\_DDR 8  
== =PP1V8\_S2R\_GRAPE 13  
== =PP1V8\_S2R\_EXT\_SWITCH 50  
== =PP1V8\_S2R\_REAR\_CAMERA  
== =PP1V8\_S2R\_MESA  
== =PP1V8\_S2R\_VDD\_CORE\_GPS  
== =PP1V8\_S2R\_VDD\_IO\_GPS

## BUCK3\_SW

52 50 46 PP1V8\_SW1 == =PP1V8\_AUDIO 15  
MAKE\_BASE=TRUE == =PP1V8\_DMIC 14  
== =PP1V8\_CAM\_FRONT 20  
== =PP1V8\_CAM\_REAR 23  
== =PP1V8\_PROX 22

## PP1V8\_EXT SW

52 50 46 PP1V8\_EXT SW == =PP1V8\_VDDIO18\_SOC 8 9  
MAKE\_BASE=TRUE == =PP1V8\_SOC 4 5 7 10 18  
== =PP1V8\_MIPI\_SOC 7  
== =PP1V8\_EDP\_SOC 7  
== =PP1V8\_NAND\_SOC 6  
== =PP1V8\_NAND 12 48  
== =PP1V8\_PLL\_SOC 4  
== =PP1V8\_SPKRAMP  
== =PP1V8\_EEPROM 51  
== =PP1V8\_BEACON

## PP1V8\_SW2

52 46 PP1V8\_SW2 == =PP1V8\_GRAPE 13  
MAKE\_BASE=TRUE

## PP1V8\_S2R\_SW3

46 PP1V8\_S2R\_SW3 == =PP1V8\_S2R\_GYRO 21  
MAKE\_BASE=TRUE == =PP1V8\_S2R\_ACCEL 21  
== =PP1V8\_S2R\_ OSCAR 19

## PP1V8\_S2R\_SW3 COMP

54 52 PP1V8\_S2R\_SW3 COMP == =PP1V8\_S2R\_COMP 21  
MAKE\_BASE=TRUE

PP1V8\_S2R\_SW3 SHOULD BE ON IN HIBERNATE  
CURRENTLY POWERS OSCAR AND 1.8V RAIL ON SENSOR

## BUCK4

52 47 46 PP1V2\_S2R == =PP1V2\_S2R\_DDR 8  
MAKE\_BASE=TRUE == =PP1V2\_S2R\_DDR\_SOC 8  
== =PP1V2\_S2R\_CAM\_REAR

## BUCK4\_SW

52 46 PP1V2\_SW1 == =PP1V2\_VDDO\_DDR 8  
MAKE\_BASE=TRUE == =PP1V2\_VDDIOD\_SOC 8  
== =PP1V2\_HSIC\_SOC 4

## PP1V2\_S2R\_SW2

52 46 PP1V2\_S2R\_SW2 == =PP1V2\_S2R\_ OSCAR 19  
MAKE\_BASE=TRUE  
PP1V2\_S2R\_SW2 SHOULD BE ON IN HIBERNATE  
PROVIDE 1.2V TO OSCAR

## BUCK5

52 46 PPVDD\_SRAM == =PPVDD\_SRAM\_CPU 9  
MAKE\_BASE=TRUE == =PPVDD\_SRAM\_SOC

## BUCK6

52 46 PP3V3\_S2R == =PP3V3\_S2R\_SWITCH 48  
MAKE\_BASE=TRUE == =PP3V3\_S2R\_WIFI\_PA 44

## PP3V3\_SW

52 48 PP3V3\_SW == =PP3V3\_EDP\_PU  
MAKE\_BASE=TRUE == =PP3V3\_NAND 12  
== =PP3V3\_USB\_SOC 4

## LDO1

52 47 PP3V0\_SPARE1 == =PP3V0\_SPARE1 49  
MAKE\_BASE=TRUE

## LDO2

52 47 16 PP1V7\_VA\_VCP == =PP1V7\_VA\_VCP 15 16  
MAKE\_BASE=TRUE

## LDO3

LDO3 SHOULD BE ON IN HIBERNATE  
COMPASS, ACCEL, GYRO, PROX ARE ON OSCAR  
HALL EFFECT NEEDS TO BE ON IN HIBERNATE  
52 47 PP3V0\_S2R\_SENSOR == =PP3V0\_S2R\_HALL 13  
MAKE\_BASE=TRUE == =PP3V0\_S2R\_GYRO 21  
== =PP3V0\_S2R\_ACCEL 21  
== =PP3V0\_S2R\_COMP 21

## LDO4

52 47 PP3V0\_ALS == =PP3V0\_ALS 20  
MAKE\_BASE=TRUE == =PP3V0\_PROX 22  
== =PP3V0\_HP\_ALS  
== =PP3V0\_IO\_ALS  
SHOULD IO ALS POWER HERE?

## LDO5

52 47 PP3V0\_UVLO == =PP3V0\_UVLO 49  
MAKE\_BASE=TRUE

## LDO6

52 47 PP3V3\_ACC == =PP3V3\_ACC 11  
MAKE\_BASE=TRUE

## LDO7

LDO7 SHOULD BE ON IN HIBERNATE  
52 47 PP3V0\_S2R\_TRISTAR == =PP3V0\_S2R\_TRISTAR 11  
MAKE\_BASE=TRUE

## LDO8

47 NC\_LDO8 NO\_TEST=TRUE == =NC\_LDO8  
MAKE\_BASE=TRUE

## LDO9

BACKUP RAIL. CAN BE BOOSTED TO MEET  
1.1V MIN ON CAMERA IF NEEDED.  
52 47 PP1V3\_CAM == =PP1V3\_CAM\_FRONT  
MAKE\_BASE=TRUE == =PP1V3\_CAM\_REAR 23

## LDO10

52 47 PP1V0\_SOC == =PP1V0\_USB\_SOC 4  
MAKE\_BASE=TRUE == =PP1V0\_MIPI\_SOC 7  
== =PP1V0\_EDP\_PAD\_DVDD\_SOC 7

## LDO11

52 47 PP2V6\_CAM\_AF == =PP2V6\_CAM\_REAR\_AF 23  
MAKE\_BASE=TRUE

## LDO13

52 47 PP2V9\_CAM == =PP2V9\_CAM\_FRONT 20  
MAKE\_BASE=TRUE == =PP2V9\_CAM\_REAR 23

## VLCM1

47 PP5V25\_GRAPE == =PP5V25\_GRAPE 13  
MAKE\_BASE=TRUE

## CHARGER MAIN

52 49 48 47 46 PPVCC\_MAIN == =PPVCC\_MAIN\_AUDIO 15 16  
MAKE\_BASE=TRUE == =PPVCC\_MAIN\_LED 47  
== =PPVCC\_MAIN\_DOCK 43  
== =PPVCC\_MAIN\_DEV  
== =PPVCC\_MAIN\_CPU 46  
== =PPVCC\_MAIN\_GPU 46  
== =PPVCC\_MAIN\_SOC 46  
== =PPVCC\_MAIN\_GRAPE 13  
== =PPVCC\_MAIN\_LCD 18  
== =PPVCC\_MAIN\_NAVAJO  
== =PPVCC\_MAIN\_VDD\_LCM 47  
== =PPVCC\_MAIN\_WLAN 44  
== =PPVCC\_MAIN\_GPS

## BATTERY

52 46 PPBATT\_VCC == =PPBATT\_POS\_CONN 45  
MAKE\_BASE=TRUE == =PPBATT\_VCC\_BB 24 25 33 34 35 36 37 38  
== =PPBATT\_AUDIO

## USB POWER INPUT

52 46 PPVBUS\_USB\_DCIN == =PPVBUS\_USB\_EMI 43  
MAKE\_BASE=TRUE

## ON\_BUF

52 47 PP1V8\_ALWAYS == =PP1V8\_ALWAYS 5  
MAKE\_BASE=TRUE

## BACKLIGHT BOOST

52 47 PPLED\_OUT\_A == =PPLED\_REG\_A 18  
MAKE\_BASE=TRUE