

V207-10

P672: GT215-128bit, 32Mx32 GDDR5

DL-DVI, VGA, HDMI

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V207 20 pcb change list

Page 2 : Add EC1802 for 12V input

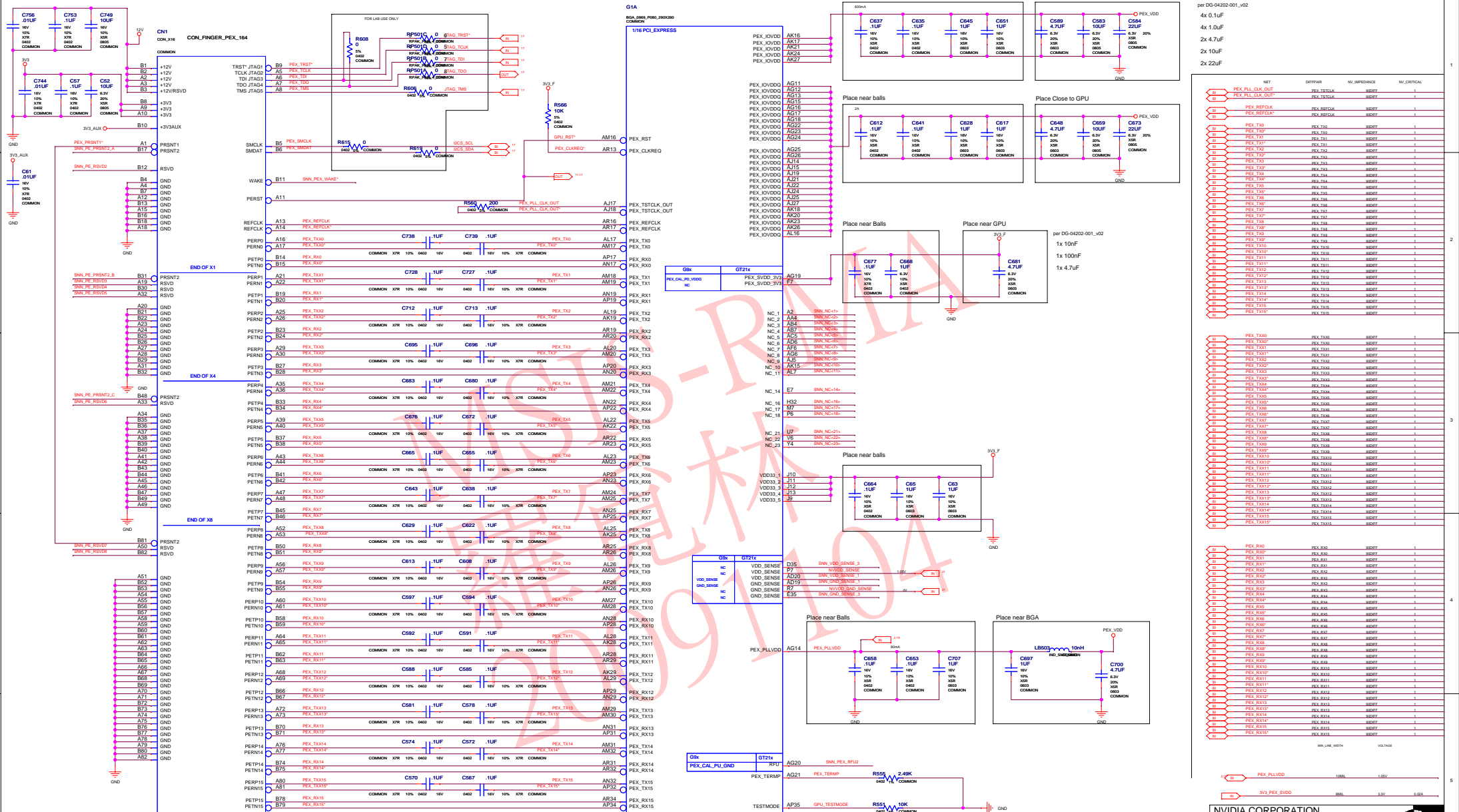
MSIS-RMA

羅覓林

20091104


REV	VARIANT	NVPN	ASSEMBLY
0	BASE	600-10672-base-100	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SRU001	600-10672-0001-100	GT215-400, 500/1375MHz, 512MB, 32Mx32, BGA175, 18000MHz, GDDR5, DVI-VGA/HDMI
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PEX x16 INTERFACE

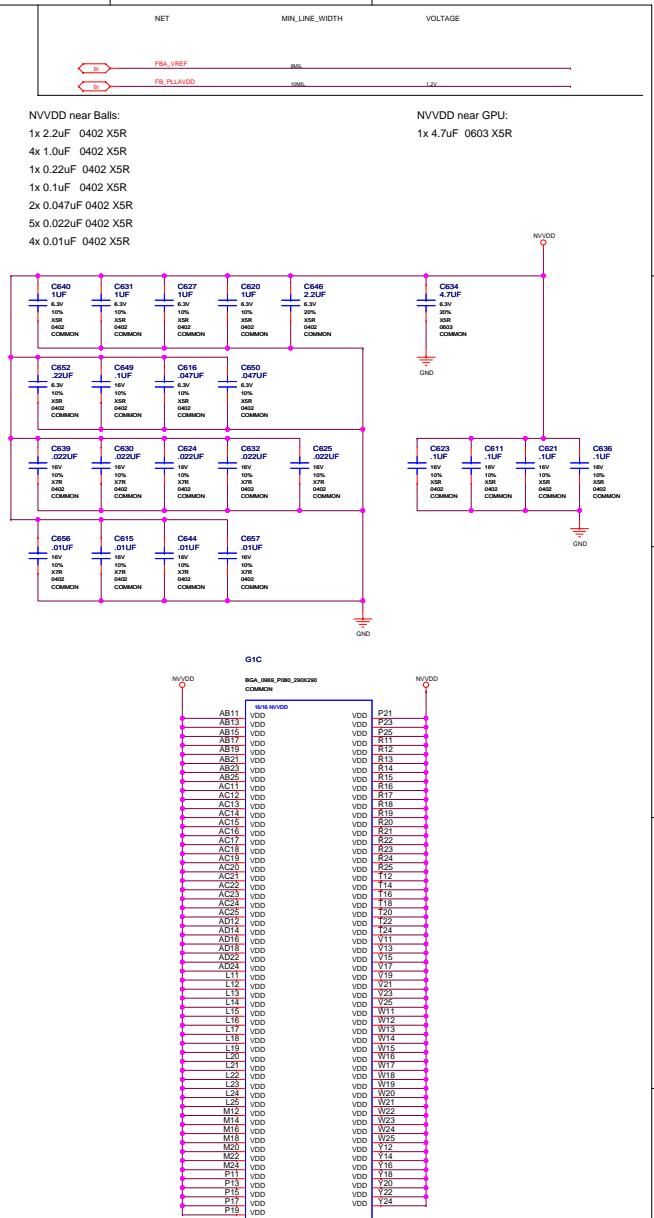
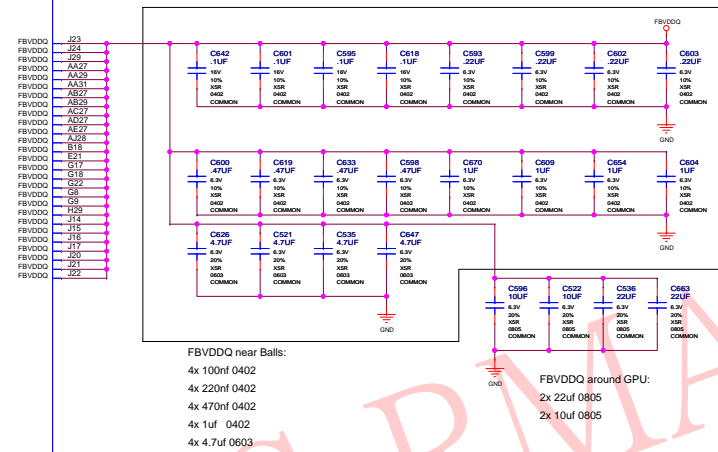
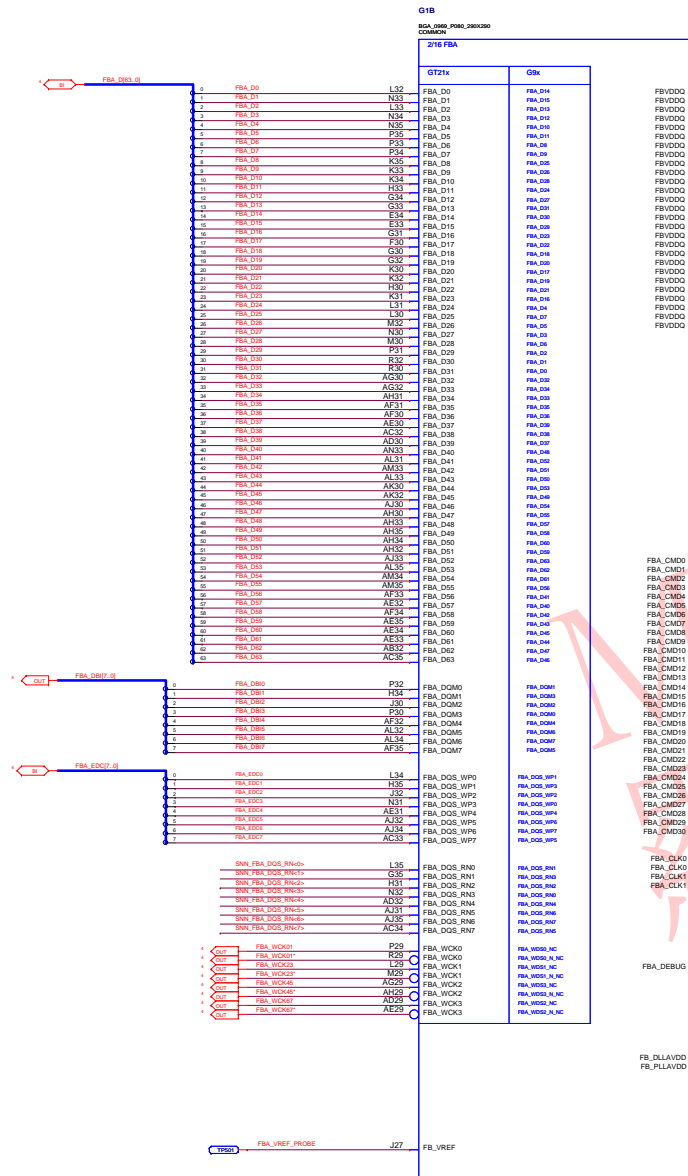


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS

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NV_PN		600-10672-base-100 A	
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MEMORY Partition A - GPU, FBVDD/Q & NVVDD DECOUPLING



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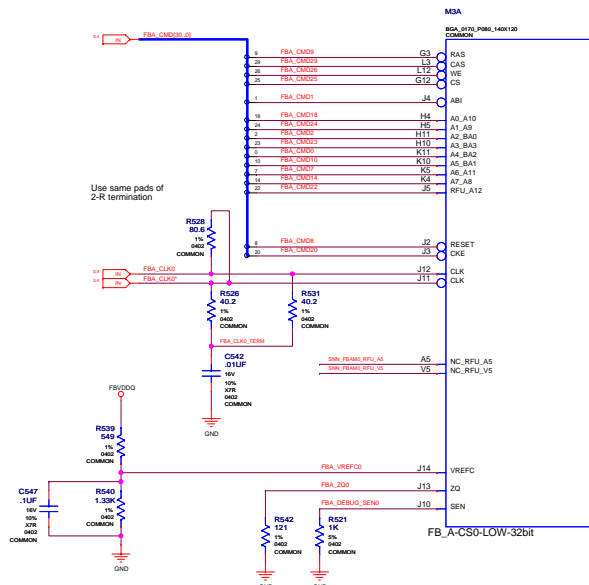
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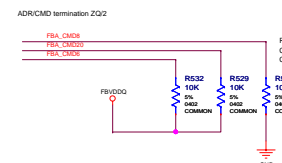
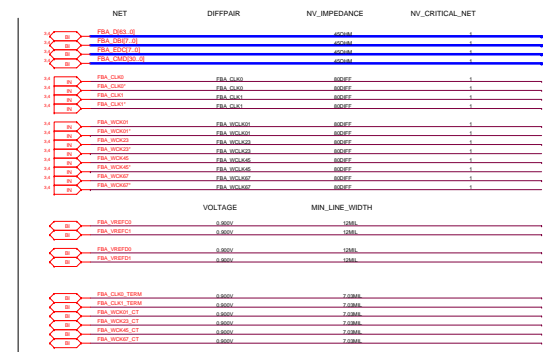
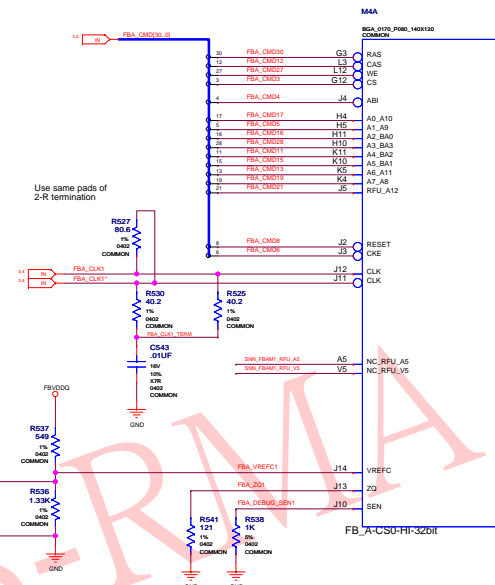
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY INTERFACE, GPU NVVDD & FBVDDQ DECOUPLING CAPS

FBA MEMORY INTERFACE, GPU NVDD & FBVDDQ DECOUPLING CAPS

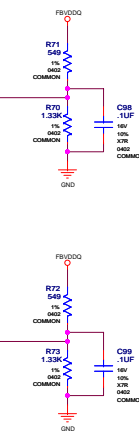
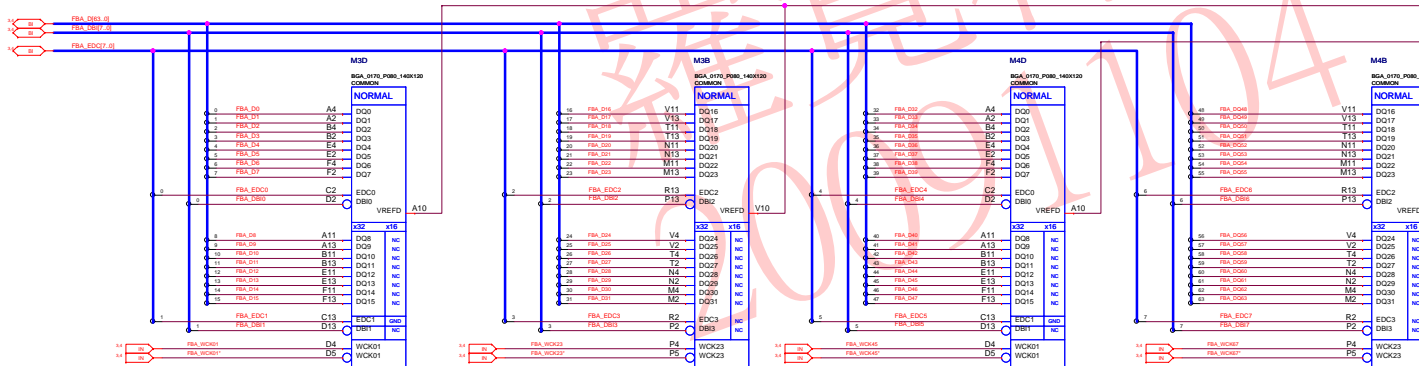
MEMORY Partition A



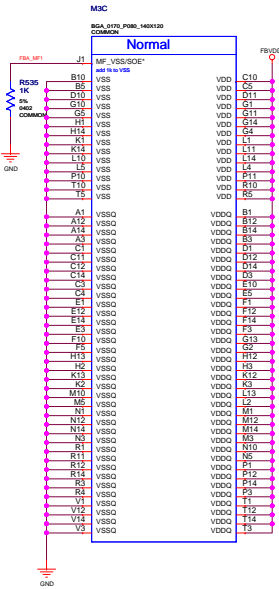
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CM00	A4, B42	
CM01	AB ¹	
CM02	A2, B40	
CM03		C5 ¹
CM04		AB ¹
CM05		A1, A2
CM06		CK ²
CM07	A6, A11	
CM08	R5 ¹	R5 ¹
CM09	R4 ²	
CM10	A5, BA1	
CM11		A4, BA2
CM12		CA ²
CM13		AB, A11
CM14	A7, AB	
CM15		AB, BA1
CM16		A2, BA0
CM17		A0, A10
CM18	A4, A10	
CM19		A7, AB
CM20	CK ²	
CM21		A12, RFU
CM22	A12, RFU	
CM23	A1, BA3	
CM24	A1, A9	
CM25	C0 ¹	
CM26	WE ²	
CM27		WE ²
CM28		
CM29	CA ²	
CM30		BA3



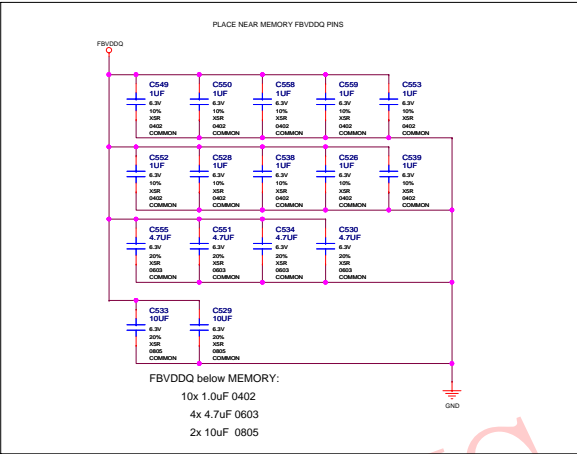
!!! Place all WCK termination inline instead at the memory near end (<50ps ~300MIL from DRAM pin) !!!



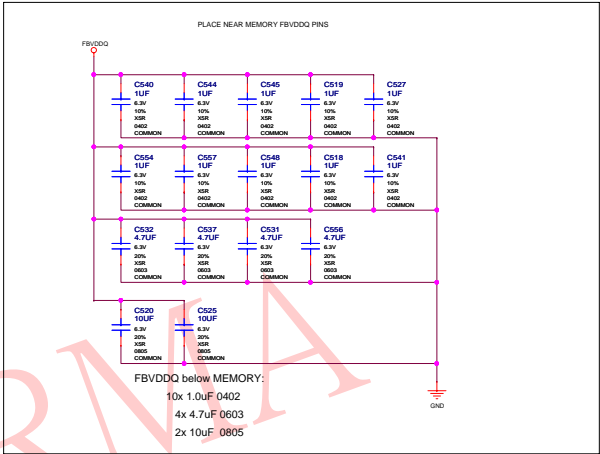
MEMORY Partition A - Decoupling



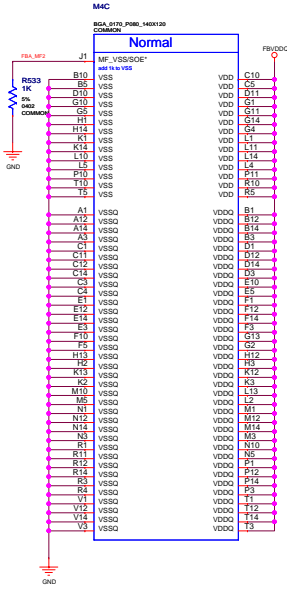
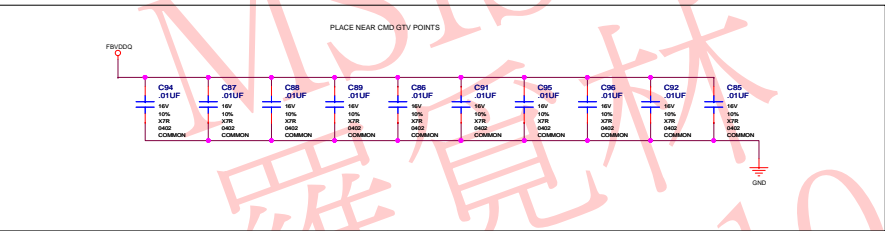
Decoupling for FBA 0..31



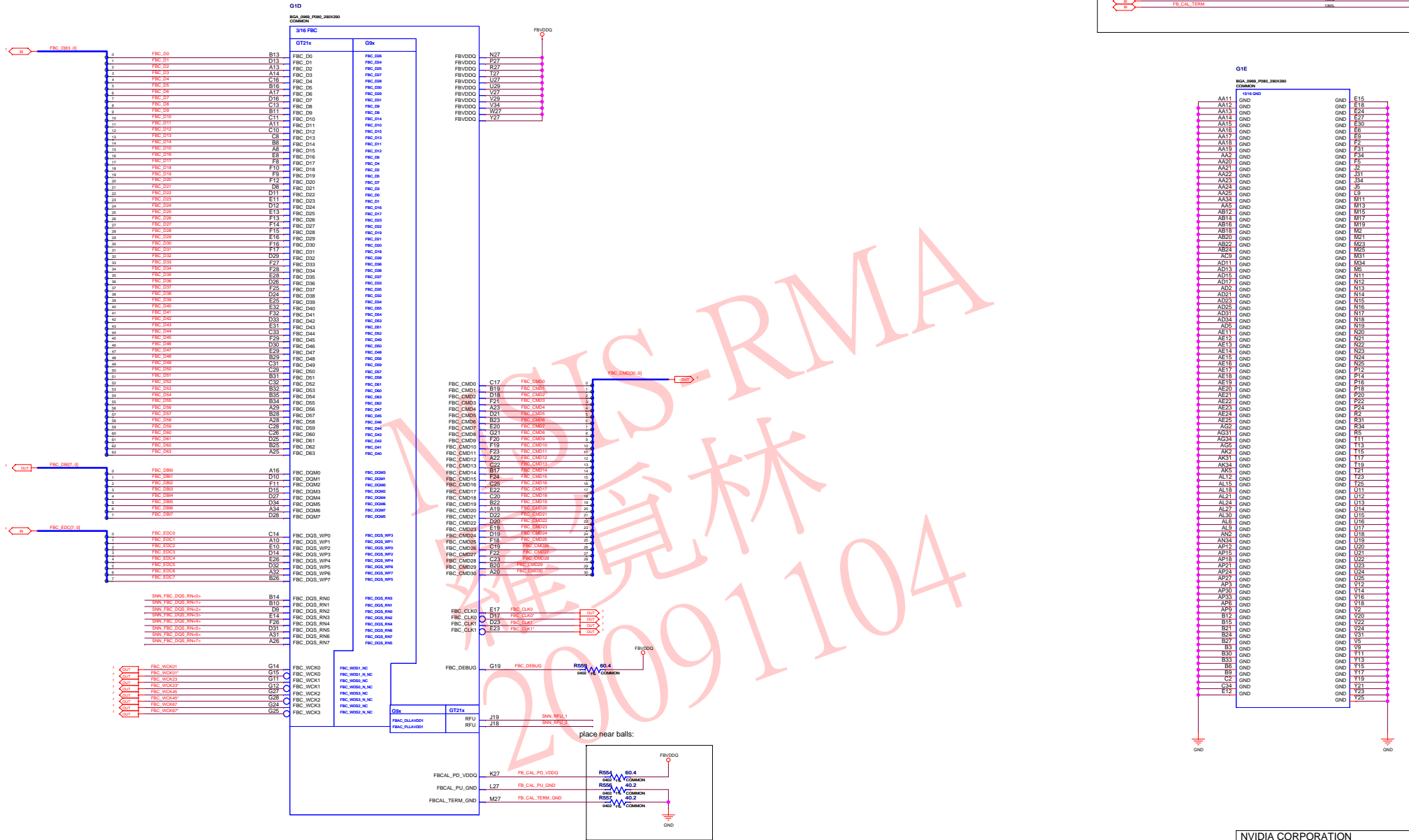
Decoupling for FBA 32..63



Return path coupling GND/FBVDDQ for FBA



MEMORY Partition C - GPU



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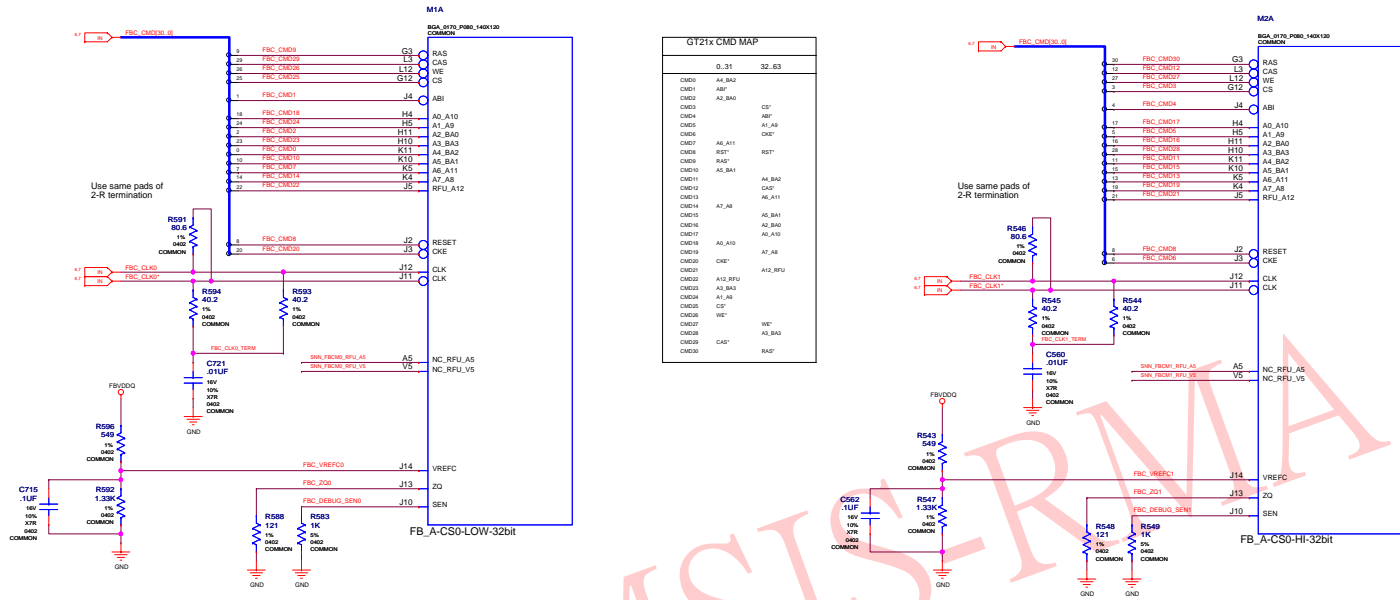


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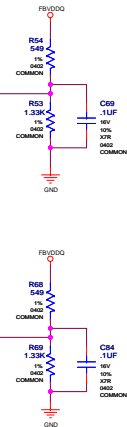
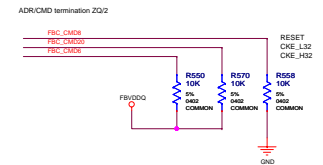
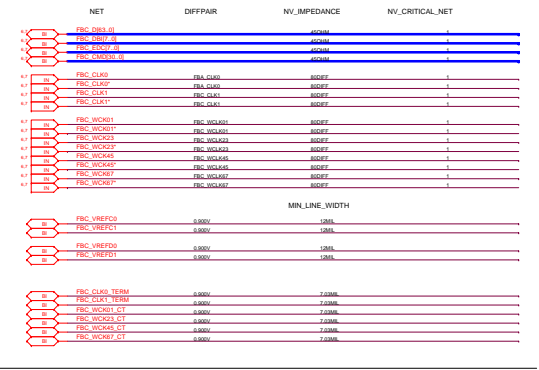
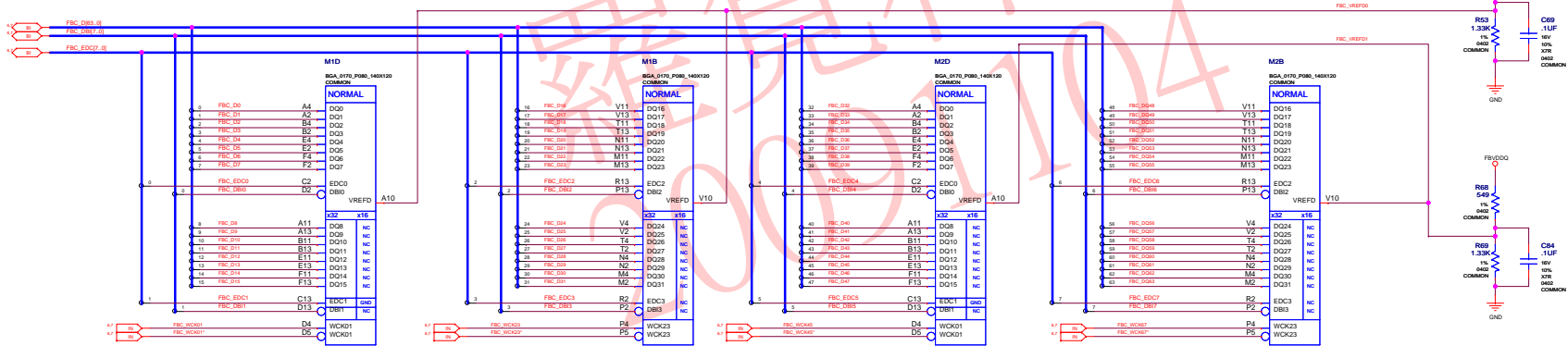
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MEMORY Partition C



!!! Place all WCK termination inline instead at the memory near end (<50ps ~300MIL from DRAM pin)!!!



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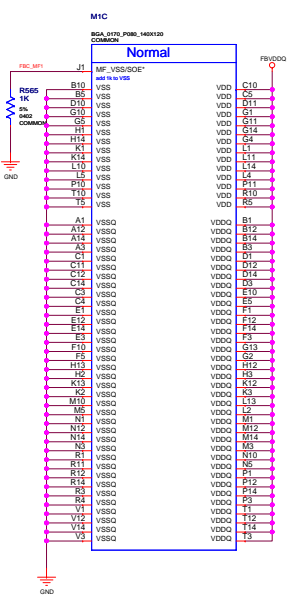


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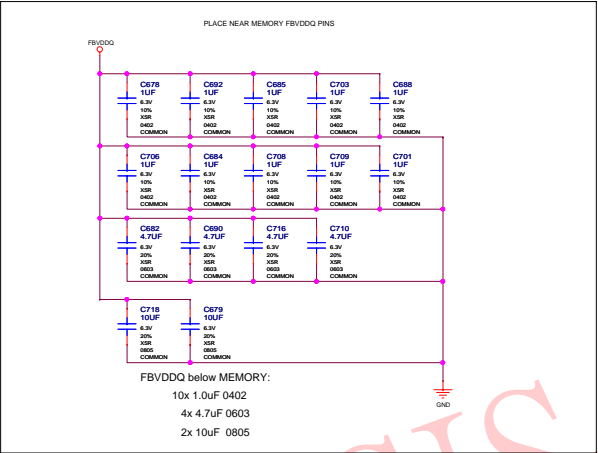
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NAME	DATE 01-JUL-2009

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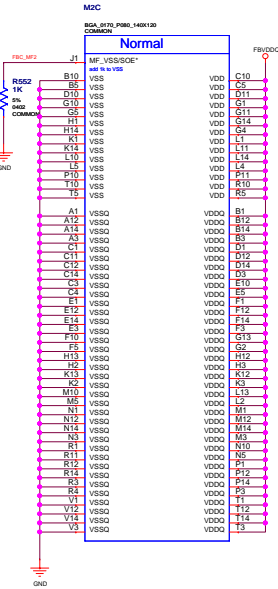
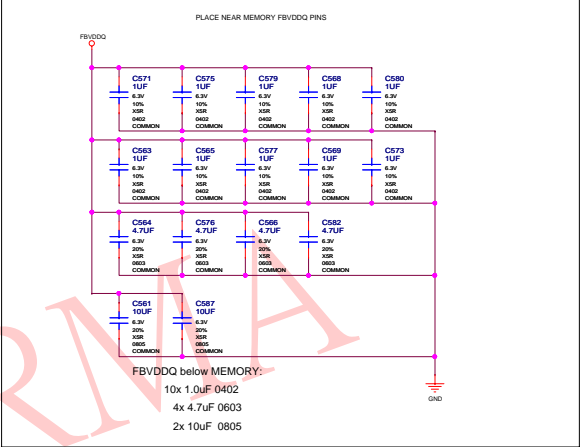
MEMORY PARTITION C DECOUPLING



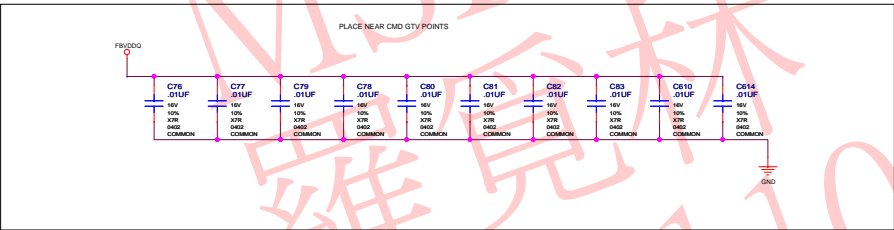
Decoupling for FBC 0.31



Decoupling for FBC 32.63



Return path coupling GND/FBVDDQ for FBC



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Primary Display (DACA), DVI-I (South)



	NET_NAME	IV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
15	DACA_VDD			3.2V 100M
16	DACA_VREF			100M
17	DACA_RESET			100M
18	DACA_RED	I	1000M	
19	DACA_GREEN	I	1000M	
20	DACA_BLUE	I	1000M	
21	DACA_RED_C	I	1000M	
22	DACA_GREEN_C	I	1000M	
23	DACA_BLUE_C	I	1000M	
24	DACA_HSYNC	I	1000M	
25	DACA_HSYNC_E	I	1000M	
26	DACA_HSYNC_E	I	1000M	
27	DACA_HSYNC_BUF	I	1000M	
28	DACA_HSYNC_BUF	I	1000M	
29	DACA_HSYNC_C	I	1000M	
30	DACA_HSYNC_C	I	1000M	

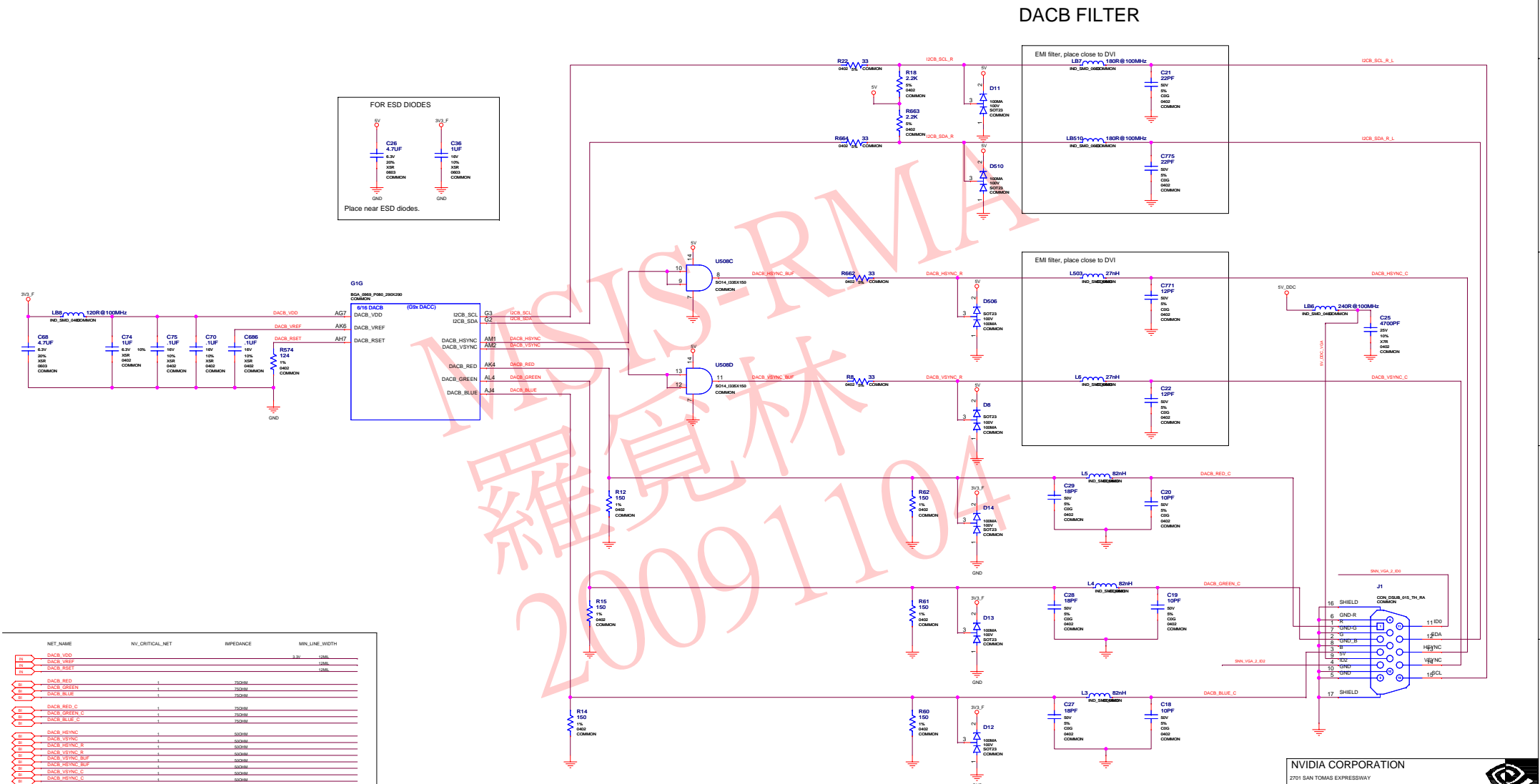
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA (PRIMARY DVI-I)

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Secondary Display (DACB), VGA (Mid)



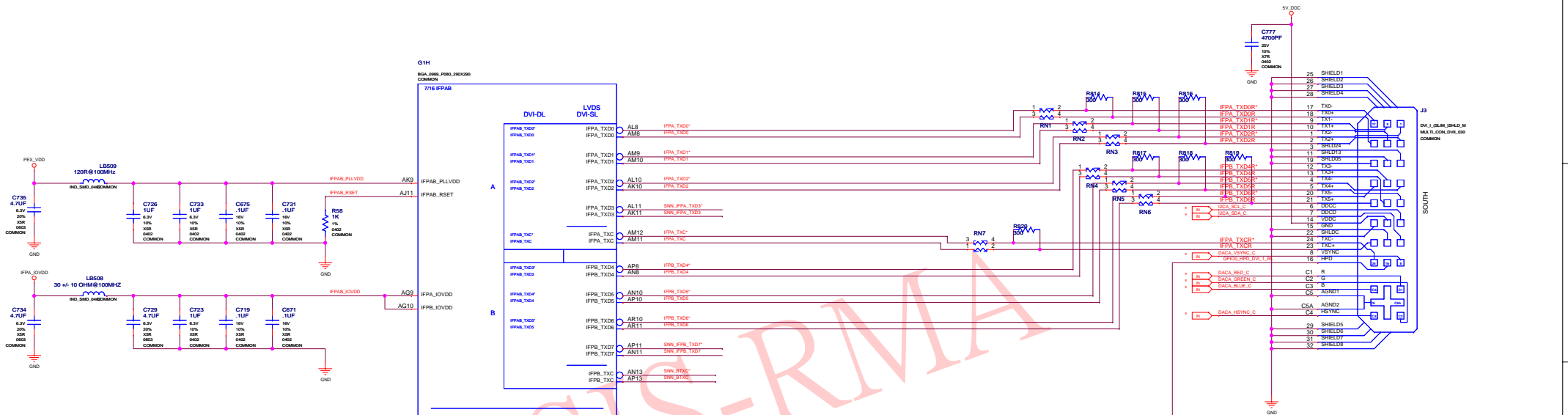
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2	DACB_VREF			100M
3	DACB_PSET			100M
4	DACB_RED	I	7500M	
5	DACB_GREEN	I	7500M	
6	DACB_BLUE	I	7500M	
7	DACB_RED_C	I	7500M	
8	DACB_GREEN_C	I	7500M	
9	DACB_BLUE_C	I	7500M	
10	DACB_HYSTING	I	5000M	
11	DACB_VSTING	I	5000M	
12	DACB_HYSTING_R	I	5000M	
13	DACB_VSTING_R	I	5000M	
14	DACB_HYSTING_BUF	I	5000M	
15	DACB_VSTING_BUF	I	5000M	
16	DACB_VSTING_C	I	5000M	
17	DACB_HYSTING_C	I	5000M	

[illegible]

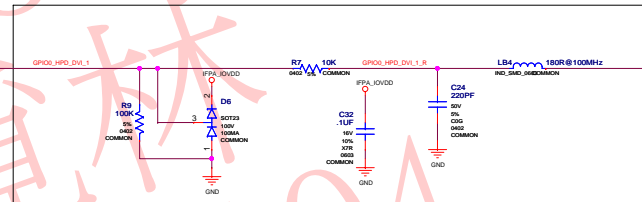
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB (SECONDARY VGA)

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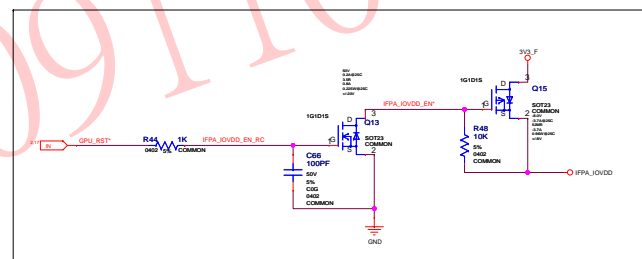
LINK A/B: TMDS, Primary DVI-I DL (South)



HOTPLUG DETECTION



IFP_IOVDD BACKDRIVE PREVENTION



	NETNAME	DEF PART NAME	NO. CRITICAL NET	NO. REFERENCE
10	IFPA_T0C1	F738_T0C1	1	10007
10	IFPA_T0C2	F738_T0C2	1	10007
10	IFPA_T0D0	F738_T0D0	1	10007
10	IFPA_T0D1	F738_T0D1	1	10007
10	IFPA_T0D11	F738_T0D1	1	10007
10	IFPA_T0D2	F738_T0D2	1	10007
10	IFPA_T0D21	F738_T0D2	1	10007
10	IFPA_T0D22	F738_T0D2	1	10007
10	IFPA_T0D23	F738_T0D2	1	10007
10	IFPA_T0D4	F738_T0D4	1	10007
10	IFPA_T0D41	F738_T0D4	1	10007
10	IFPA_T0D50	F738_T0D50	1	10007
10	IFPA_T0D51	F738_T0D51	1	10007
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10	IFPA_T0V9	F738_T0V9	1	10007
10	IFPA_T0W0	F738_T0W0	1	10007
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10	IFPA_T0W2	F738_T0W2	1	10007
10	IFPA_T0W3	F738_T0W3	1	

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PAGE DETAIL	TMD5 LINK A/B: DVI-I (SOUTH)

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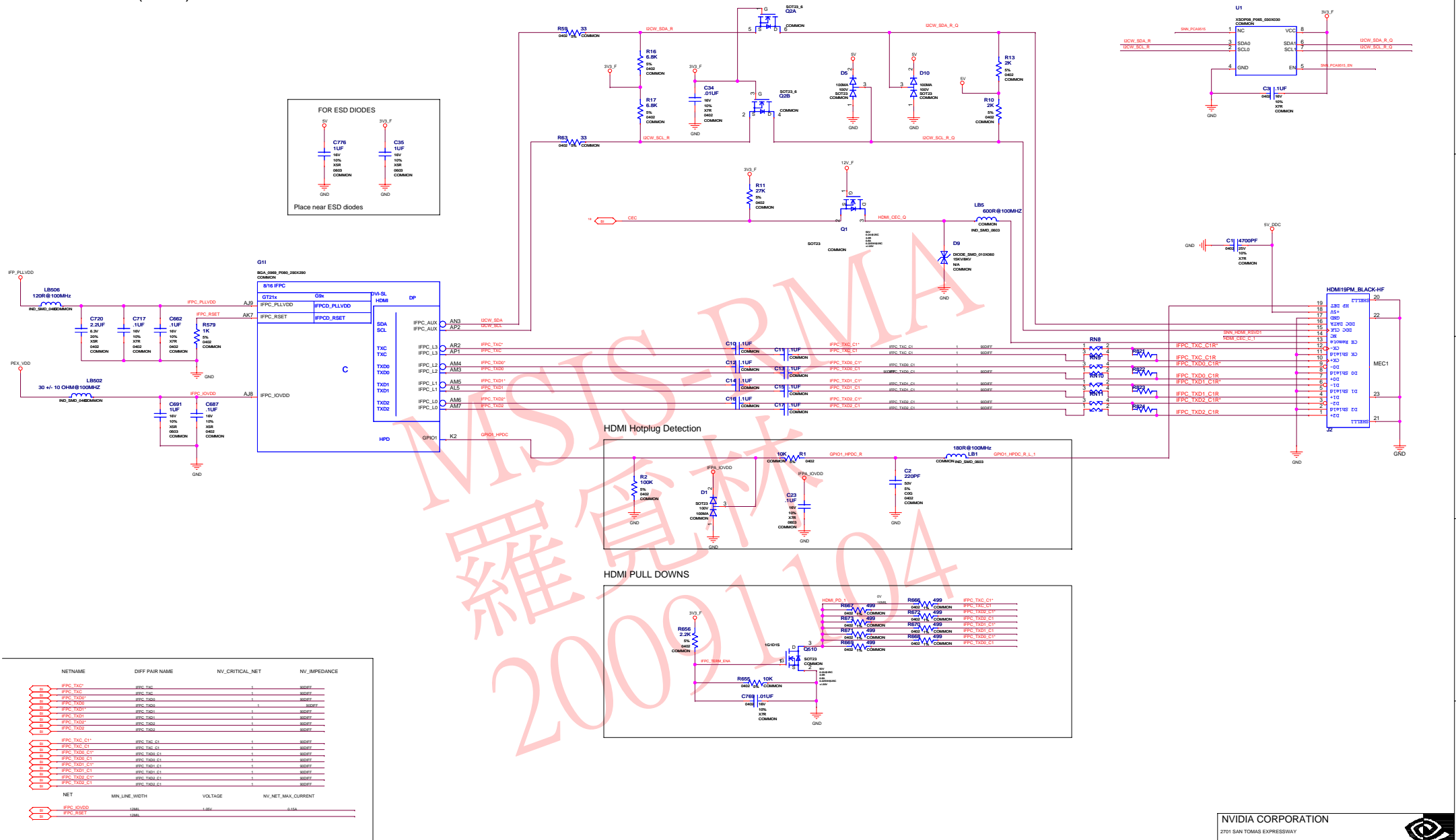
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LINK C: HDMI (North)



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NV_PN	600-10672-base-100 A
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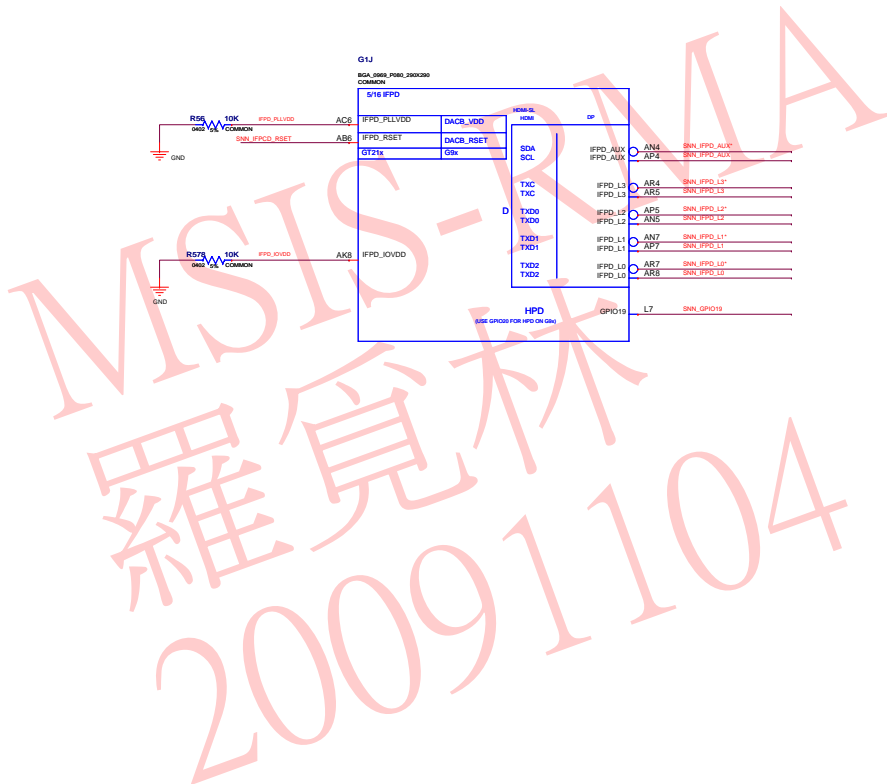
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The diagram shows a horizontal beam of total length \$L\$. A vertical line at the left end represents a support. A horizontal force \$H\$ is applied at the right end, pointing to the left. The beam is divided into two segments by the support.

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PAGE DETAIL	LINK C: HDMI (NORTH)

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A



A

3

C

P

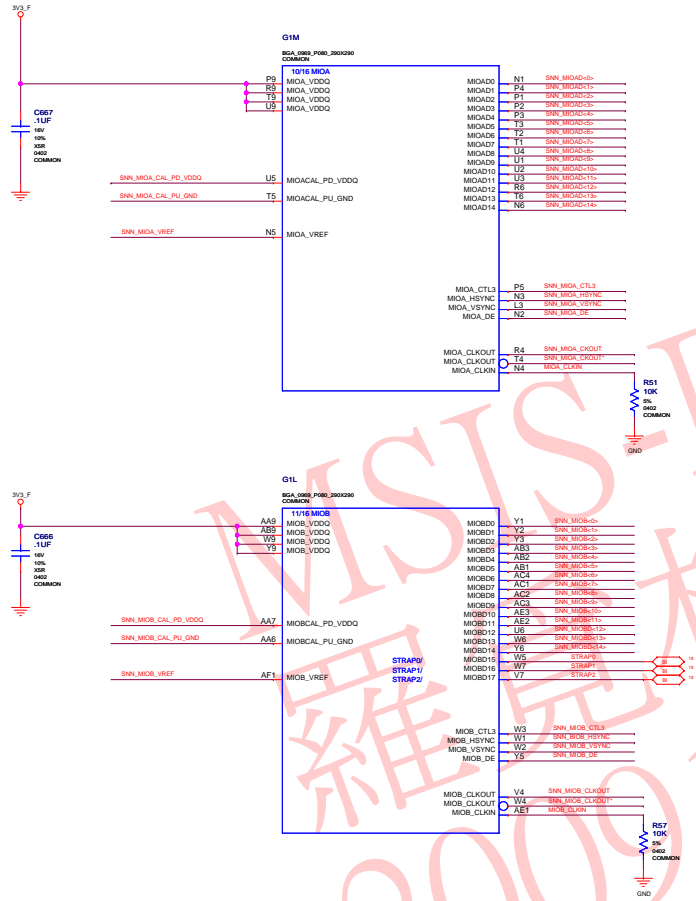
3

F

Q

[illegible]

MIOA/B UNUSED



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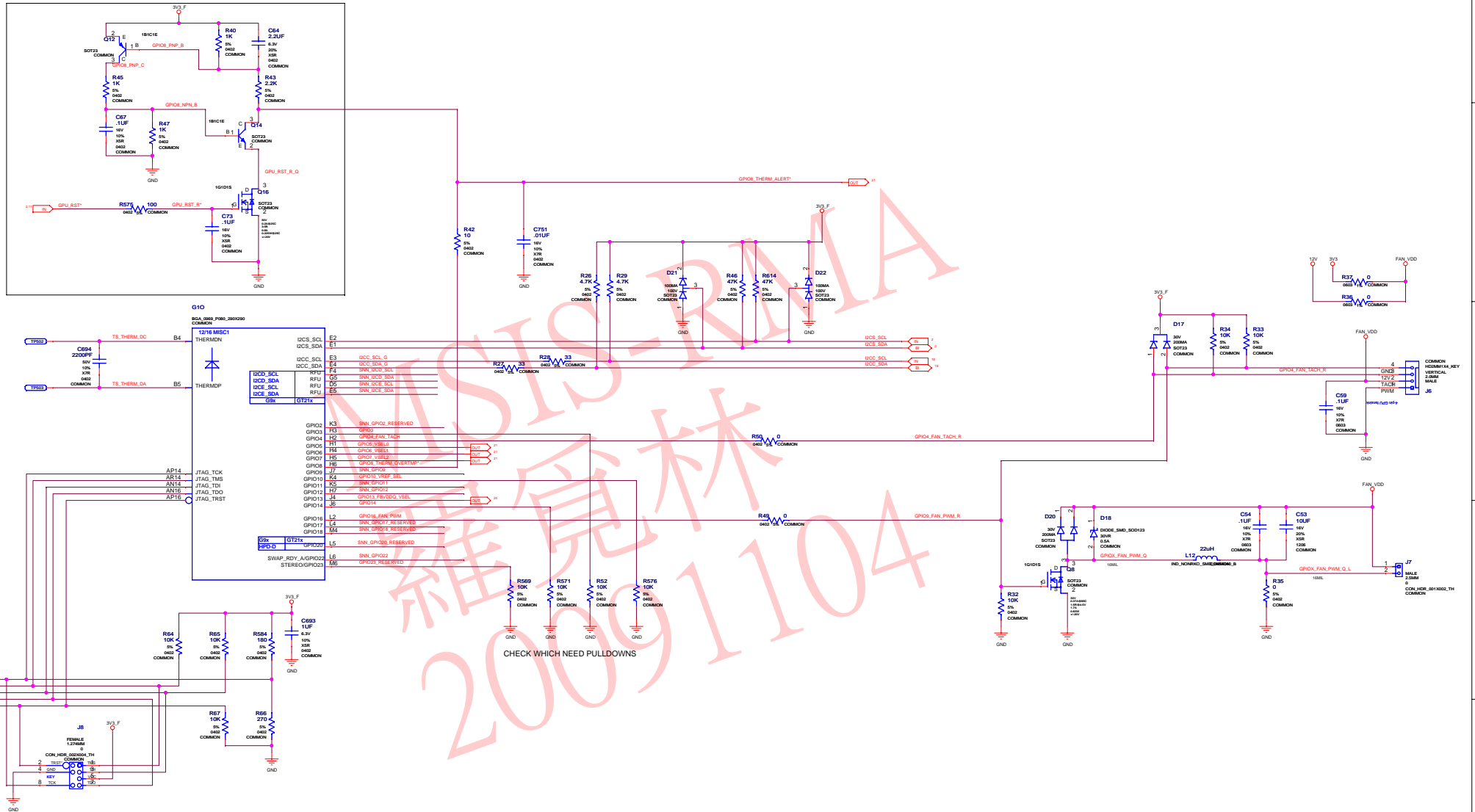
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THERM ALERT, FAN CONTROL, GPIO & JTAG

THERM ALERT LATCH



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PAGE DETAIL	FAN CONTROL, THERMAL ALERT, GPIO, JTAG

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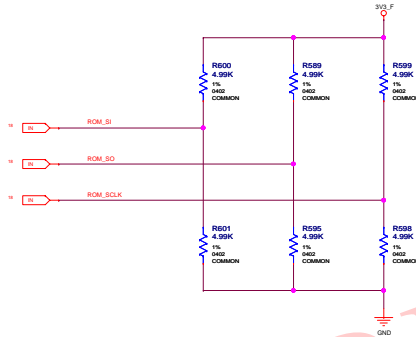
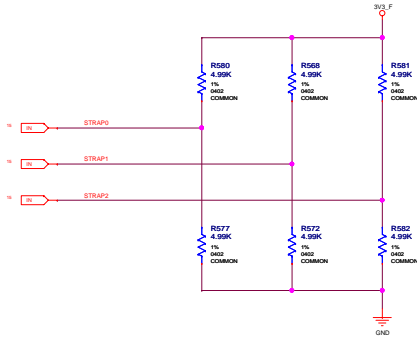
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STRAPPING, VBIOS, INFOROM

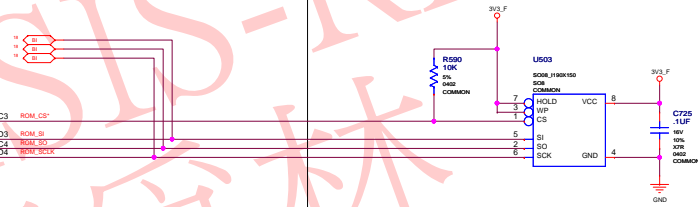
STRAPPING OPTIONS



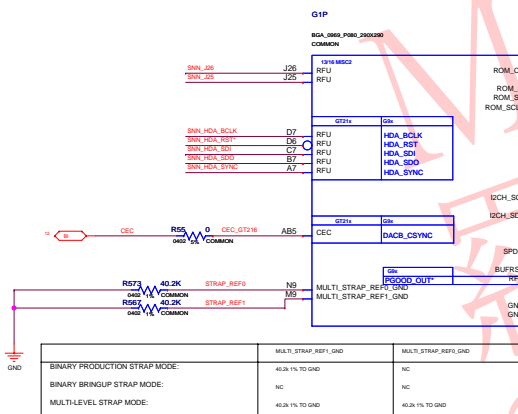
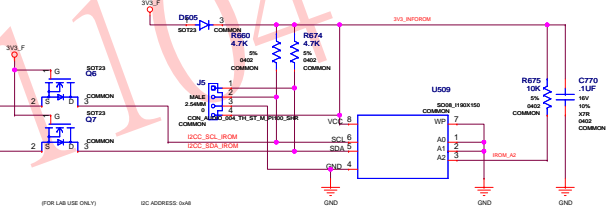
STRAP[3:0] = 0x8 (GPIO_PADCFG DSKTOP default plus 0x8)
STRAP[3:0] = 0x8 (PCL_DEVID = 0xCAB)
ROM_SQ[0] = 1 (VGA Device Enable)
ROM_SQ[1] = 0 (SMB_ALT_ADDR, default (1GPU))
ROM_SQ[2] = 0 (FB apert. size 256MB, default)
ROM_SQ[3] = 0 (XCLK_417, default)
ROM_SCLQ[0] = 0 (PEX_PLL_EN_TERM100 disabled, default)
ROM_SCLQ[1] = 1 (SLT_CLK_CFG, default)
ROM_SCLQ[2] = 1 (VBIOS RM present, default)
ROM_SCLQ[3] = 0 (PCL_DEVID[4] = 0)

ROM_SQ[3:0] = RAMCFG[3:0]
0x0001 Qimonda 128-bit, GDDR5
0x0010 Hynix 128-bit, GDDR5
0x0011 Samsung 128-bit, GDDR5

BIOS ROM(serial)



INFOROM



FBVDDQ Power Supply 1.35-1.50V@15A

[illegible]

	GPIO13
FBVDDQ = 1.35V	0
FBVDDQ = 1.55V	1

$$\begin{aligned} \text{FBVDDQ} &= \text{VREF} * (1 + (\text{Rtop} / \text{Rbot})) \\ 1.358\text{V} &= 0.8\text{V} * (1 + (698 / 1\text{K})) \end{aligned}$$

$$\begin{aligned} \text{FBVDDQ} &= \text{VREF} * (1 + (\text{Rtop} / \text{Rbot} \parallel \text{Rbot1})) \\ 1.548\text{V} &= 0.8\text{V} * (1 + (698 / (1\text{K} \parallel 2.94\text{K}))) \end{aligned}$$

NET		MIN_LEN_WIDTH	VOLTAGE	IN_NET_MAX_CURRENT
RVDD0	RVDD0	120kΩ	1.8V	60A
RVDD0	RVDD0	200kΩ	1.8V	30A
PEX_VDD0	PEX_VDD0	200kΩ	1.05V	30A
PS_FB_BOOT	PS_FB_BOOT	120kΩ		
PS_FB_BOOT_A	PS_FB_BOOT_A	120kΩ		
PS_FB_USATE	PS_FB_USATE	120kΩ		
PS_FB_USATE_B	PS_FB_USATE_B	120kΩ		
PS_FB_PHASE	PS_FB_PHASE	200kΩ		50A
PS_FB_USATE	PS_FB_USATE	120kΩ		
PS_FB_VCC12	PS_FB_VCC12	120kΩ	12V	
PS_FB_VCC3	PS_FB_VCC3	120kΩ	3V	
PS_FB_VVCC5	PS_FB_VVCC5	120kΩ	5V	
PS_V12_DR	PS_V12_DR	120kΩ		
PS_V12_FB	PS_V12_FB	120kΩ		
PS_V12_BC	PS_V12_BC	120kΩ		
PS_FB	PS_FB	120kΩ		
PS_FB_FB	PS_FB_FB	120kΩ		
PS_FB_SVFLY	PS_FB_SVFLY	120kΩ		
PS_FB	PS_FB	120kΩ		
PS_FB_VO	PS_FB_VO	120kΩ		
PS_FB_SNB	PS_FB_SNB	120kΩ		
PS_FB_COMP	PS_FB_COMP	120kΩ		
PS_FB_SC_CP	PS_FB_SC_CP	120kΩ		
PS_FB_E	PS_FB_E	120kΩ		
PS_FB_C	PS_FB_C	120kΩ		

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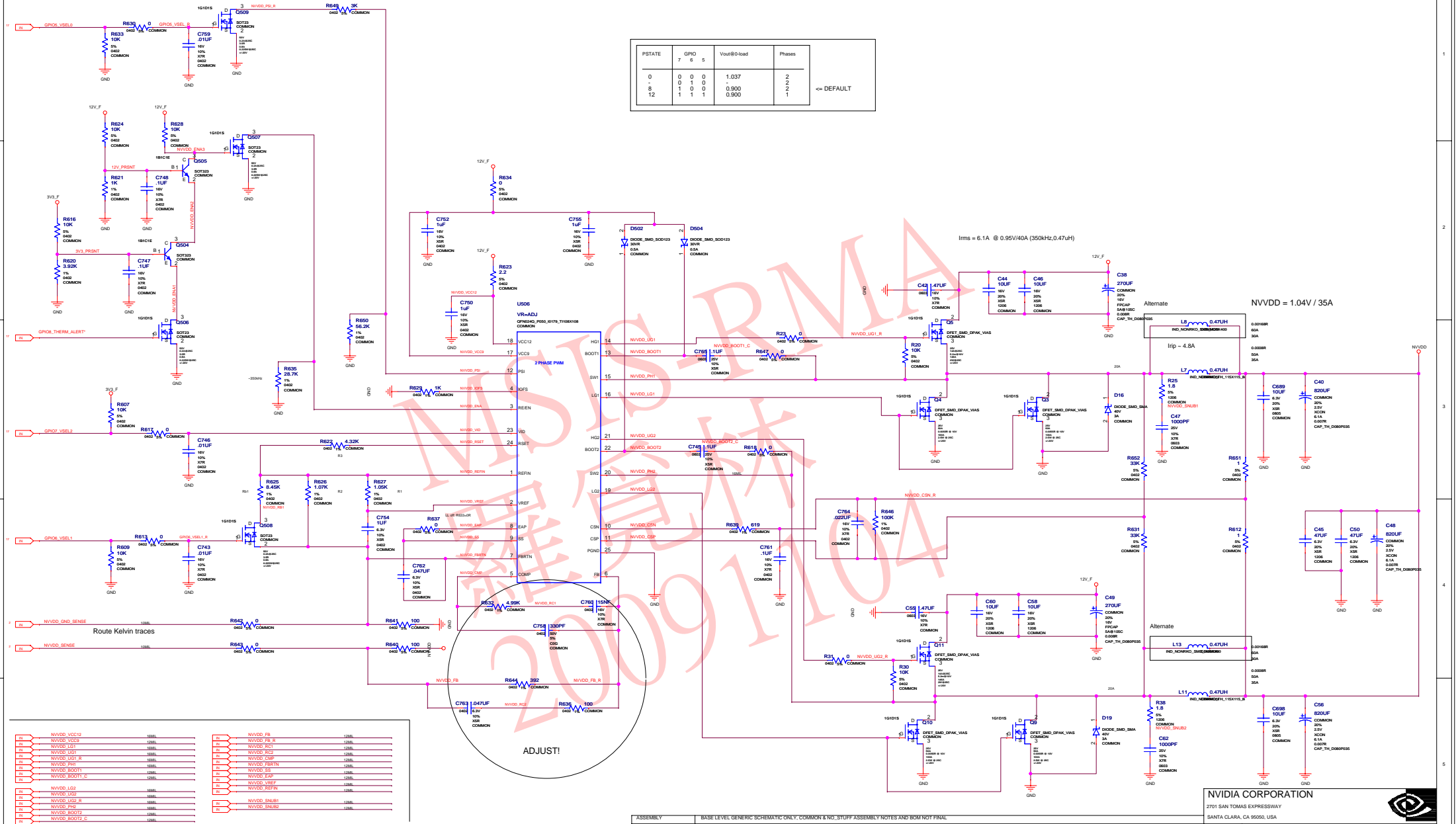
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBVDDQ SINGLE PHASE SWITCHER, PEX_VDD LINEAR

POWER SUPPLY: NVVDD DUAL-PHASE SWITCHER

NVVDD Power Supply 35A@1.04V



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NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

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