P636: G98, DDR2 MEMORY 64MX16/32MX16

Page 1: P636 Overview

Page 2: PCI EXPRESS INTERFACE

Page 3: Frame Buffer Interface

Page 4: Memory 1st Bank 0..31

Page 5: Memory 1st Bank 32..63

Page 6: DACA, VGA FOR DVI-I

Page 7: DACC,2x6 Header

Page 8: DACB, UNUSED

Page 9: TMDS Interface

Page 10: UNUSED PARTS FOR G98 AND GND

Page 11: Straps, Mechanical Parts

Page 12: XTAL, GPIO, BIOS, FAN, JTAG, HDCP

Page 13: Power Supply: NVVDD, 1V1

Page 14: Power Supply : 5V, FBVDDQ

Page 15: THERMAL LATCH CIRCUIT

Page 16: BACKUP DECOUPLING CAPS

Page 17: NET REPORT

Page 18: COMPONENT REPORT

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10636-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0001	600-10636-0001-000	P636: G98-459-U2, 256MB DDR2 500MHZ, DVI+VGA
2	SKU0002	600-10636-0002-000	P636: G98-459-U2, 512MB DDR2 500MHZ, DVI+VGA
3	SKU0003	600-10636-0003-000	P636: G98-459-U2, 512MB DDR2 400MHZ, DVI+VGA
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	P636 Overview

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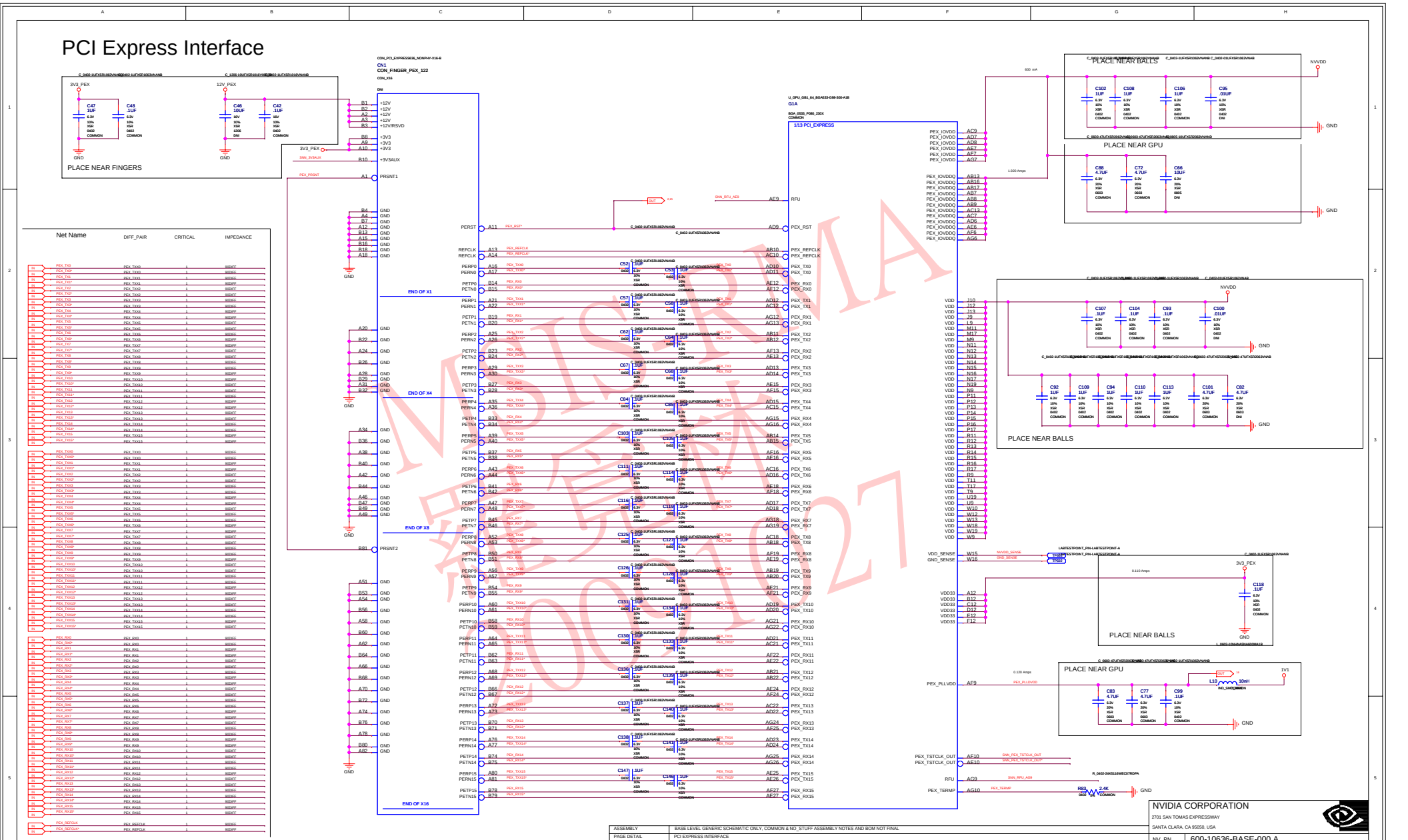
NV_PN	600-10636-BASE-000 A		
ID		PAGE	
NAME		DATE	23-JUL-2009

PCI Express Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS INTERFACE

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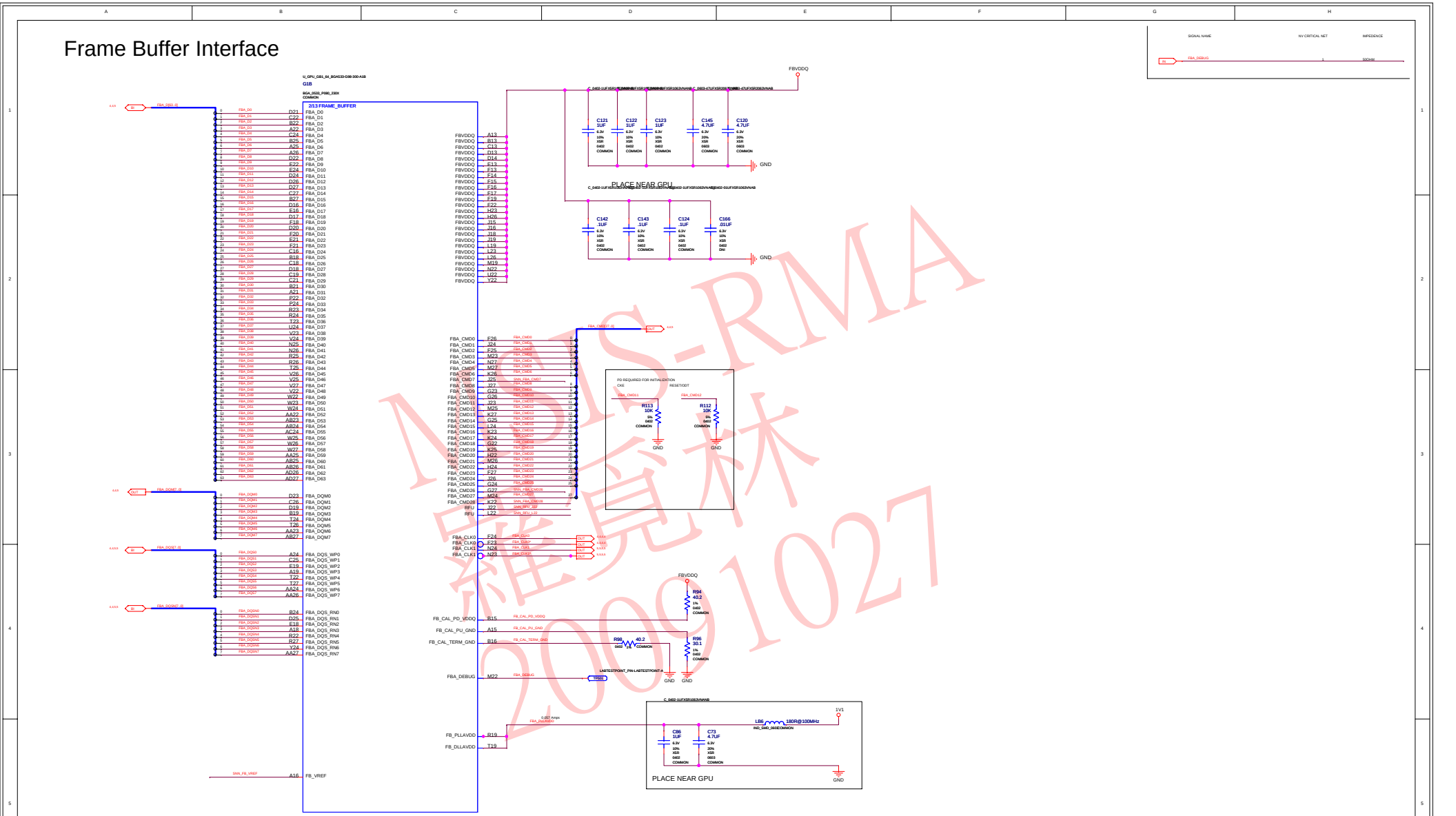
Frame Buffer Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Frame Buffer Interface

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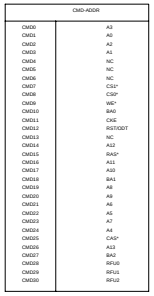
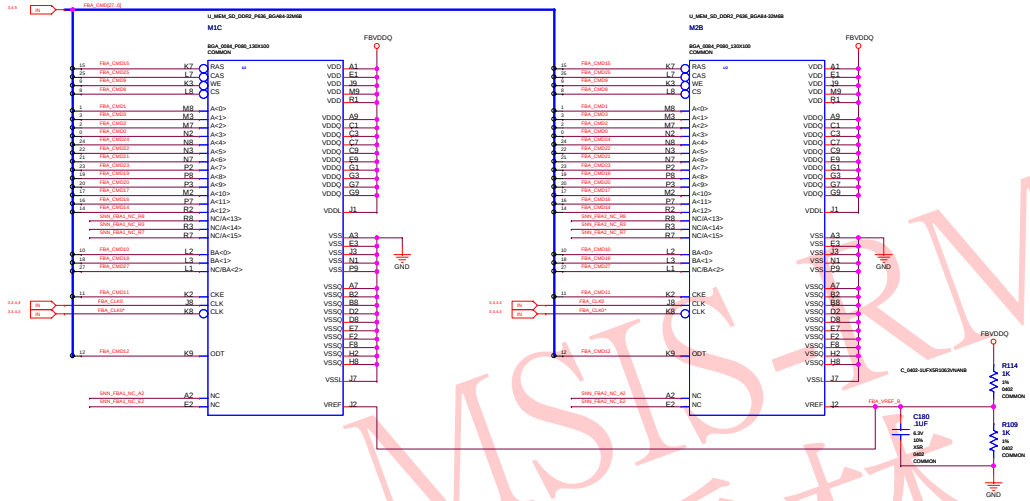
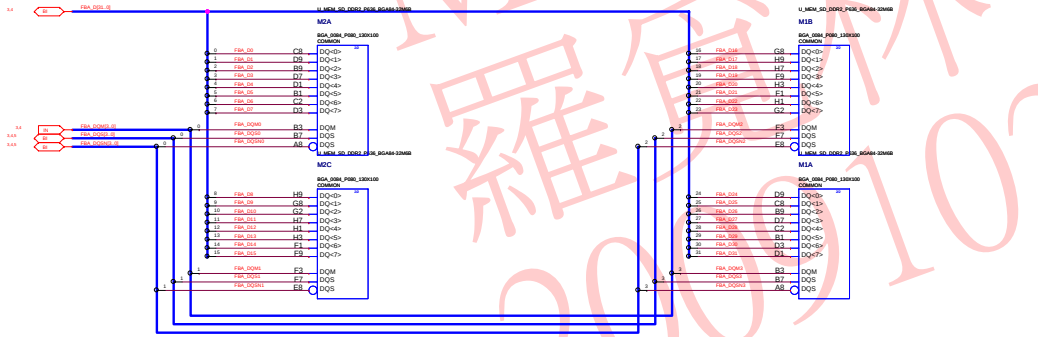
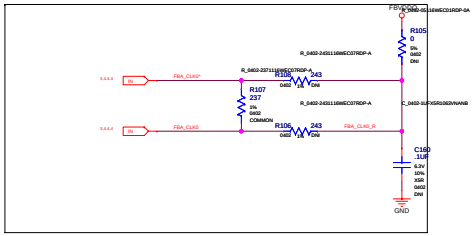
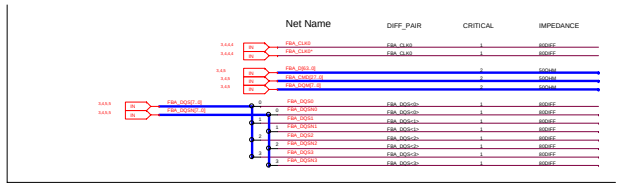
Memory 1st Bank 0..31

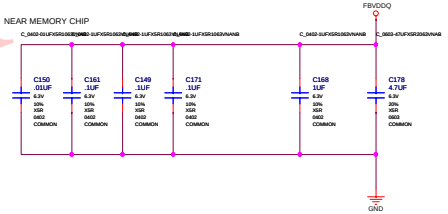


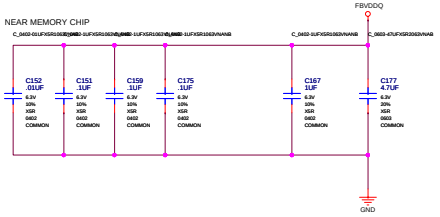












ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Memory 1st Bank 0..31

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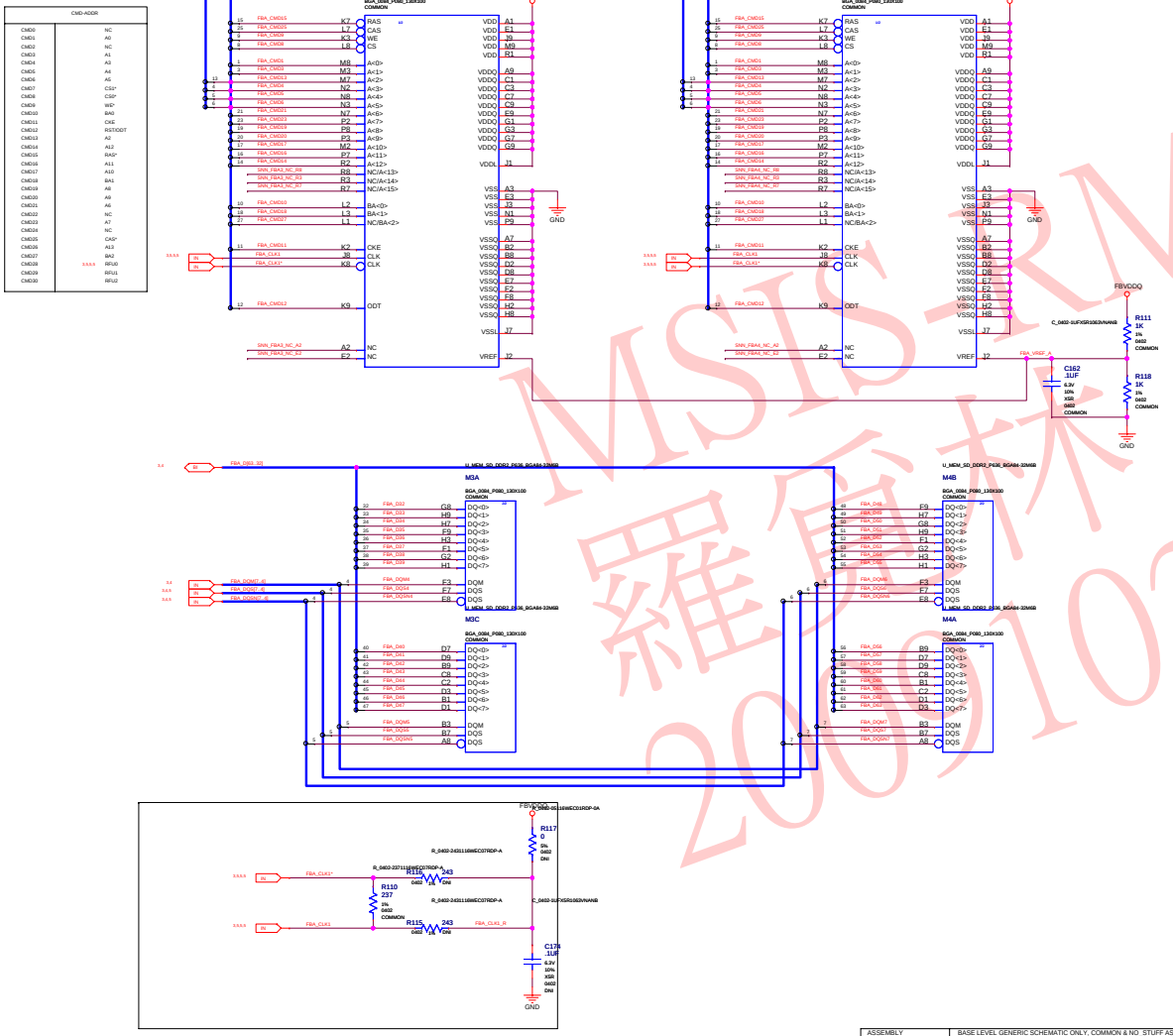
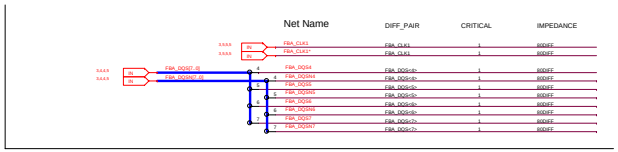
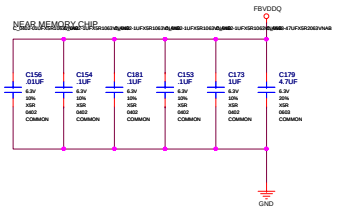
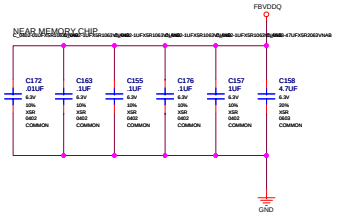
ID		PAGE	
NAME		DATE	23-JUL-2009

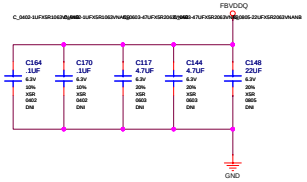
Memory 1st Bank 32..63











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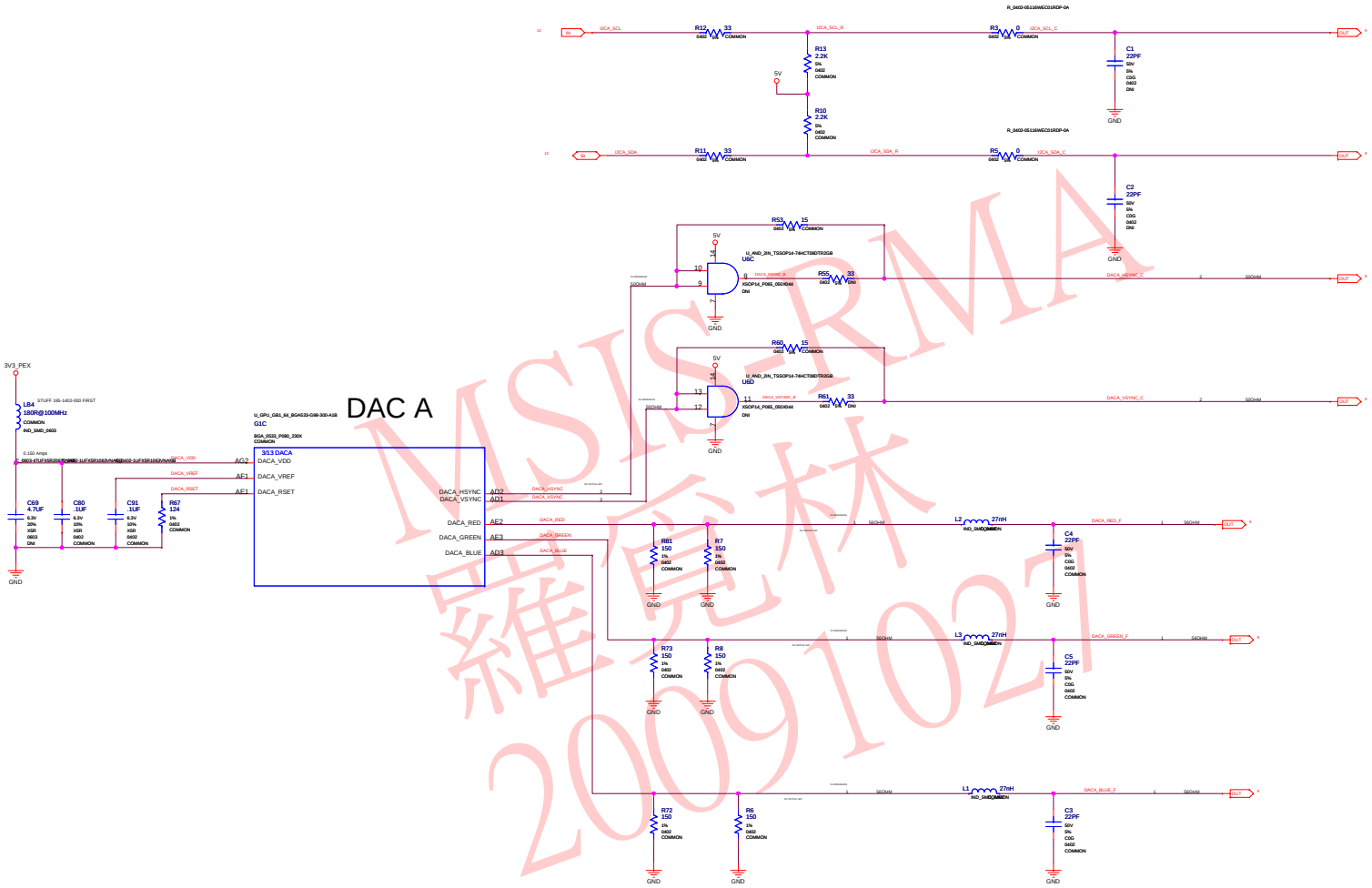
DACA,VGA FOR DVI-I



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PAGE DETAIL	DACA_VGA FOR DVI-I

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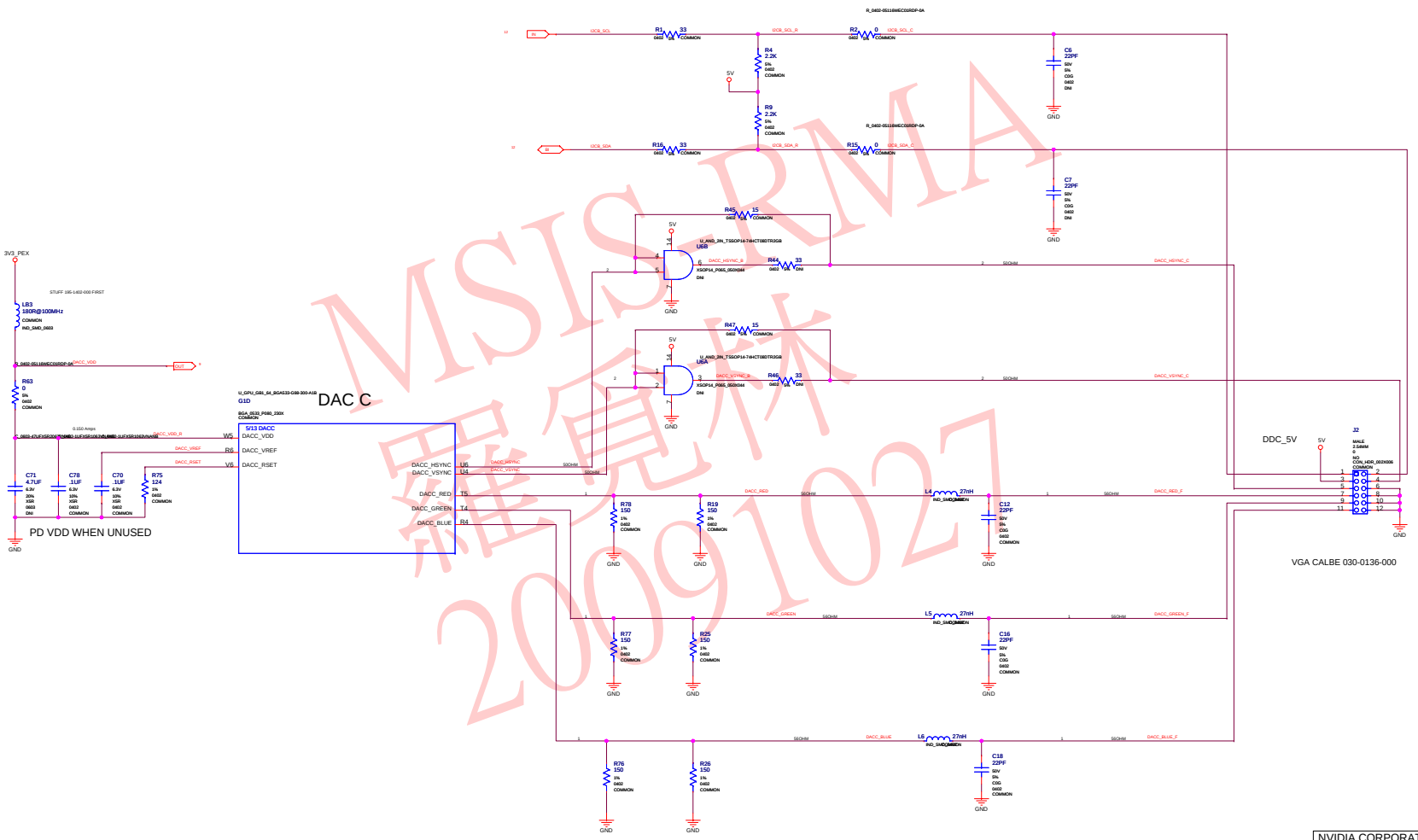
DACC,2x6 Header



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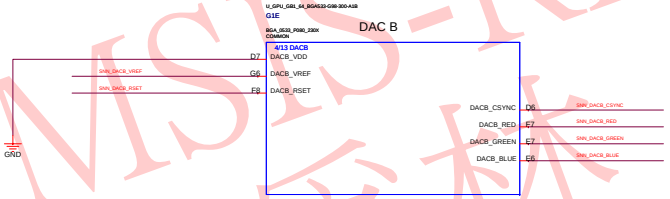
DACB,UNUSED



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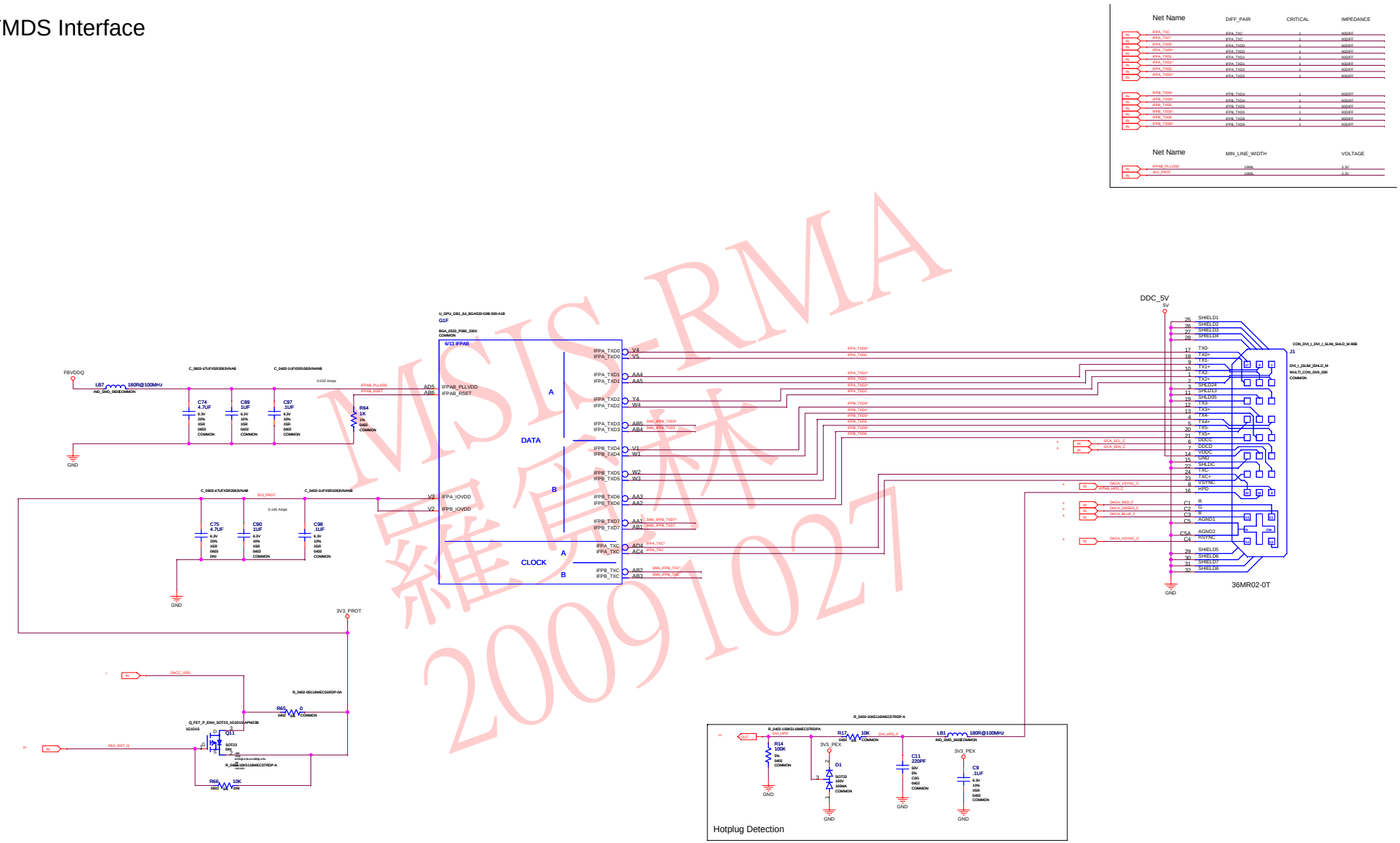
TMDS Interface



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PAGE DETAIL	TMDS Interface

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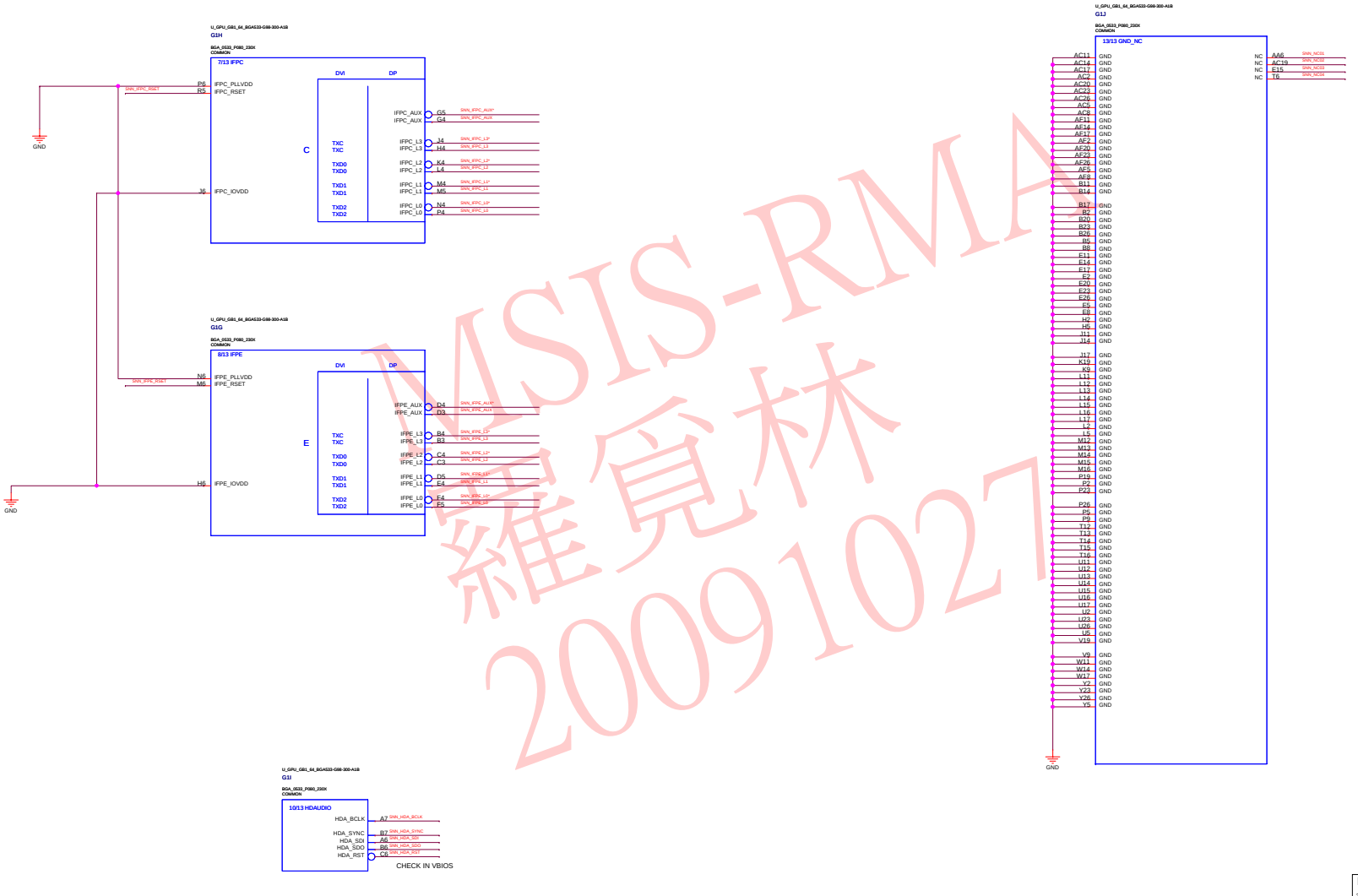
UNUSED PARTS FOR G98 AND GND



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PAGE DETAIL	UNUSED PARTS FOR G98 AND GND

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ID		PAGE	
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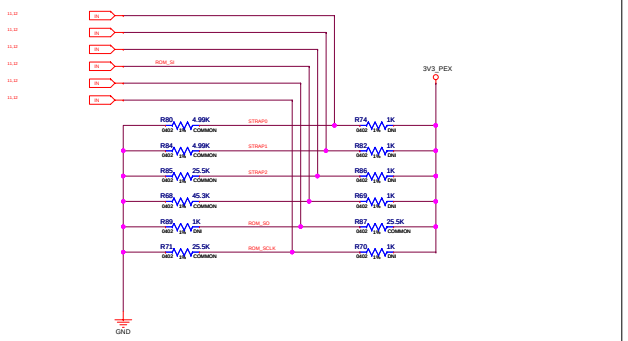
Straps, Mechanical Parts

MULTI LEVEL STRAPS



Each strap pin represents a 4 bit value

Pullup or Pulldown configures the MSB

Resistor Value determines the 3 LSBs

Resistor range is R*n

where n is 0-9 and R is 5K ohm.

RESValue	MultiLevel	TiedToVcc	TiedToGround
5 K ohms	Y	1000	0000
10 K ohms	Y	1001	0001
15 K ohm	Y	1010	0010
20 K ohms	Y	1011	0011
25 K ohms	Y	1100	0100
30 K ohms	Y	1101	0101
35 K ohms	Y	1110	0110
45 K ohms	Y	1111	0111

MULTI LEVEL MODE

STRAP_CAL_PU_GND0 (RS12) = 40K
STRAP_CAL_PU_GND1 (RS11) = 40K

SIGNAL	FUNCTION
STRAP[0]	USER[3..0]
STRAP[1]	3GIO_PADCFG_LUT_ADR[3..0]
STRAP[2]	PCI_DEVID[3..0]
ROM_SCLK	PCI_DEVID_EXT, SUB_VENDOR, SLOT_CLK_CFG, PEX_PLL_EN_TERM100
ROM_SI	RAMCFG[3..0]
ROM_SO	XCLK_277, TVMODE[2..0]

STRAP SETTINGS FOR HYNIX 32Mx16 DDR2 500MHz (MULTI LEVEL) R511= 40K, R512=40K

3V3_PEX	GND	PIN(SIGNAL)	FUNCTION
	5K	STRAP[0]	USER[3..0]
	5K	STRAP[1]	3GIO_PADCFG_LUT_ADR[3..0]
	25K	STRAP[2]	PCI_DEVID[3..0]
	25K	ROM_SCLK	PCI_DEVID_EXT, SUB_VENDOR, SLOT_CLK_CFG, PEX_PLL_EN_TERM100
	45K	ROM_SI	RAMCFG[3..0]
2SK		ROM_SO	XCLK_277, TVMODE[2..0]

STRAPS

1. SUB VENDOR = 1 (ROM PRESENT
   = 0 (NO ROM PRESENT)

2. DEVICE ID FOR G80-64 = 0x00E4
   A) PCI_DEV_ID = [3..0] LSB = 0100
   B) PCI_DEVID_EXT = [1] 4TH BIT = 0

3. 3GIO_PADCFG_LUT_ADR[3..0] = 0000

4. TVMODE[2..0] = 001

5. RAMCFG[3..0] = 0000 64Mx16 DDR2 64 BIT HYNIX
   = 0001 64Mx16 DDR2 64 BIT SAMSUNG Q-DIE
   = 0010 64Mx16 DDR2 64 BIT QIMONDA
   = 0011 64Mx16 DDR2 64 BIT SAMSUNG E-DIE
   = 0100 32Mx16 DDR2 64 BIT NANYA
   = 0101 32Mx16 DDR2 64 BIT SAMSUNG
   = 0110 32Mx16 DDR2 64 BIT QIMONDA
   = 0111 32Mx16 DDR2 64 BIT HYNIX

6. USER[3..0] = 0000

NOT READY YET

COOLING SOLUTION
No connected mounting pins

HEATSINKK8_P83S-HEATSINKK8RB
MEC1
HSP_GRU_HS122_T
COMMON

NOT READY YET

BRACKET6M_ATX_1X_NO-BRKT_ATX_0
BKT1
BRKT_ATX_STAB_1_DVI_2
COMMON

MEC2
MEC_SCREW_HEX_JACK
COMMON

MEC3
MEC_SCREW_HEX_JACK
COMMON

MEC4 MOUNT HEX CONNECTOR

FM1 SW_FID <New Pin>
FM2 SW_FID <New Pin>
FM3 SW_FID <New Pin>
FM4 SW_FID <New Pin>
FM5 SW_FID <New Pin>
FM6 SW_FID <New Pin>

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Straps, Mechanical Parts

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ID		PAGE	
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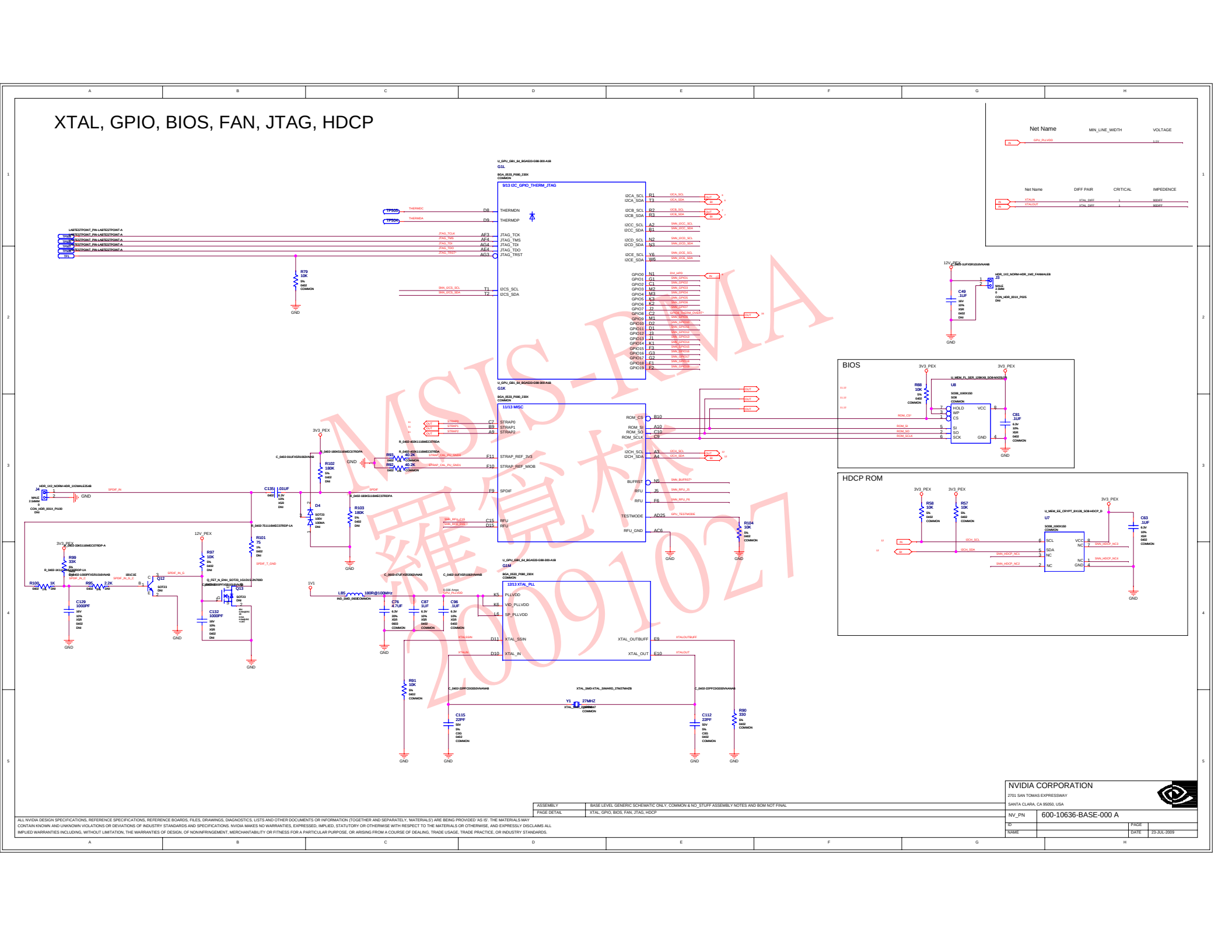
XTAL, GPIO, BIOS, FAN, JTAG, HDCP



Power Supply: NVVDD, 1V1

Net Name	LINE_WIDTH	Current	Voltage
NVVDD	16MIL	16.74A	1.1V
1V1	16MIL	2.64A	1.1V
12V_PEX	16MIL	4A	12V
GND	16MIL		0V

UPI6103:315-0524-000, 300KHZ
APW7165:315-0460-000, 300KHZ
UPI6101:315-0462-000, 300KHZ
NCP1579:XXX-XXXX-XXX, 275KHZ
L6726A: XXX-XXXX-XXX, 270KHZ

RMS 5.7A

STUFF 042-0071-000 OR MLCCS

STUFF WHEN NCP1579/L6276A

Power Sequence

<0.3V OFF -- UPI6103
<0.6V OFF -- APW7165
<0.3V OFF -- NCP1579
<0.4V OFF -- L6726A
OD ON

1.1V@15A

STUFF WHEN L6727

0OHM WHEN UPI6103

APW: 15PF, 12.7K
UPI: 47PF, 12.7K
NCP: XXPF, XXXXK
L6726: XXPF, XXXXK
L6727: XXPF, XXXXK

TRANSISTOR->MOSFET

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD, 1V1

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NV_PN	600-10636-BASE-000 A		
ID		PAGE	
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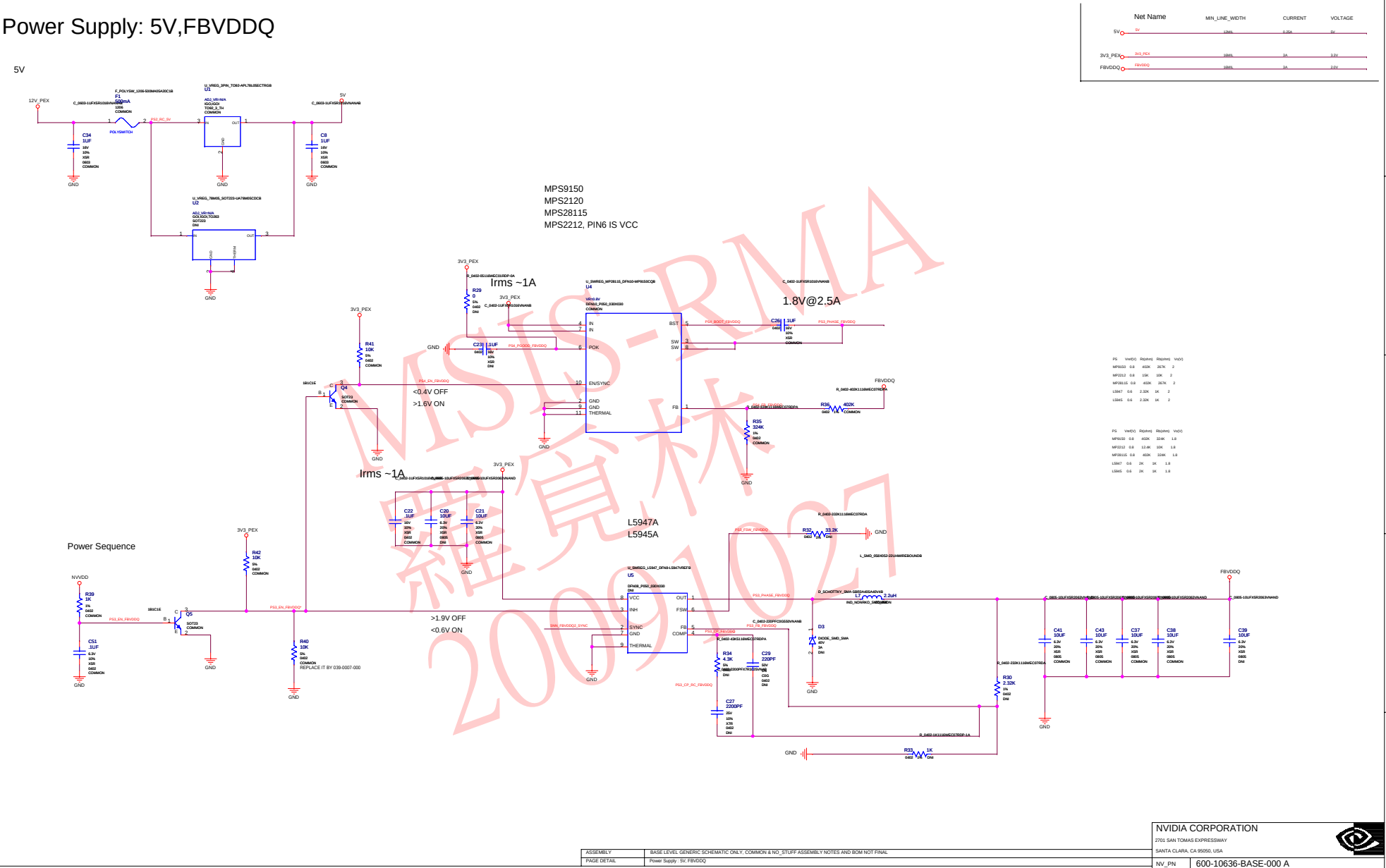
Power Supply: 5V,FBVDDQ



Net Name | MIN_LINE_WIDTH | CURRENT | VOLTAGE

5V | 12MIL | 0.25A | 5V

3V3_PEX | 10MIL | 3A | 3.3V

FBVDDQ | 10MIL | 3A | 2.5V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply : 5V, FBVDDQ

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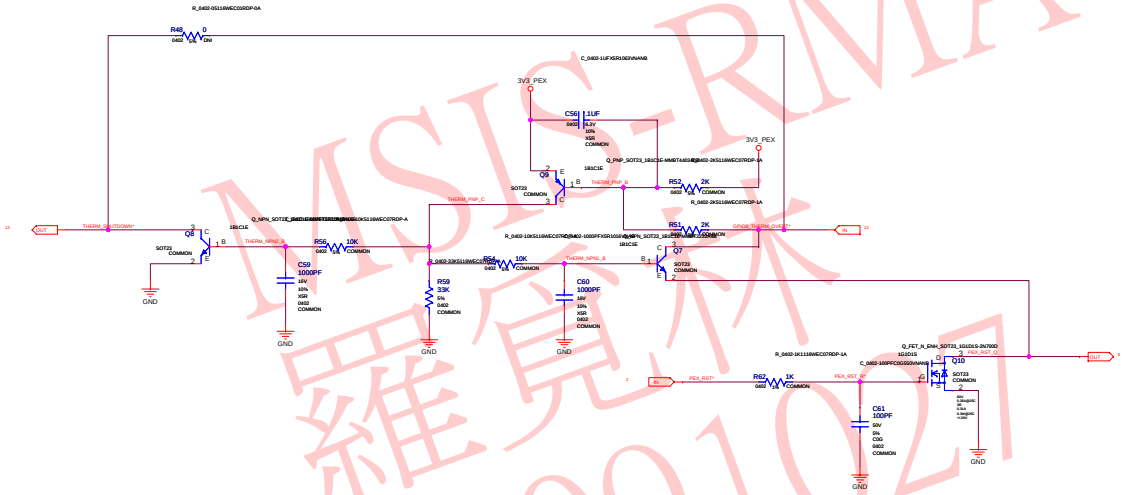
THERMAL LATCH CIRCUIT



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PAGE DETAIL	THERMAL LATCH CIRCUIT

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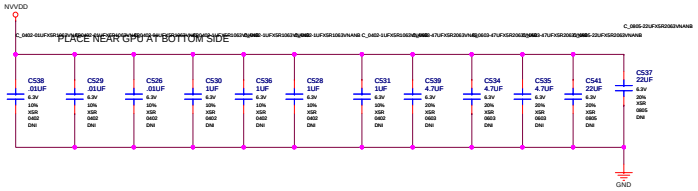
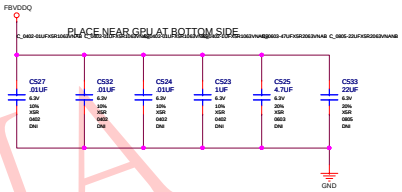
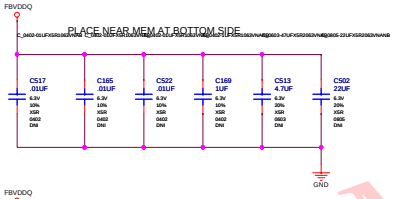
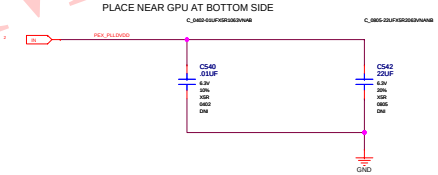
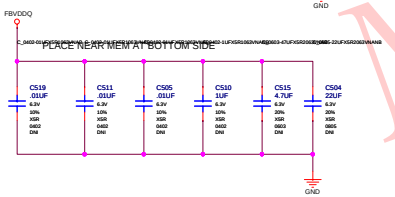
BACKUP DECOUPLING CAPS

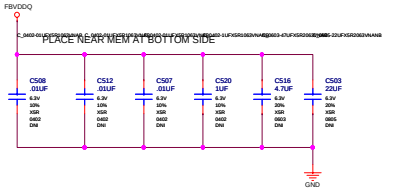


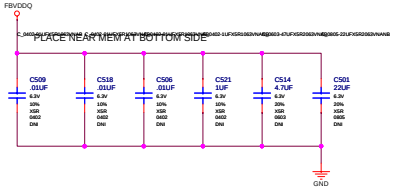












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PAGE DETAIL	BACKUP DECOUPLING CAPS

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Title: Basenet Report
Design: p636
Date: Jul 10 17:01:46 2009

Base nets and synonyms for
p636_lib.P636(@p636_lib.p636(sch_1))
Base Signal Location(Zone)[dir]

1V1 13.1F
3V3_PEX 14.1G
3V3_PROT 9.1G< 9.3B
5V 14.1G
12V_PEX 13.1F
DACA_BLUE 6.3C
DACA_BLUE_F 6.4F> 9.3G<
DACA_GREEN 6.3C
DACA_GREEN_F 6.4F> 9.3G<
DACA_HSYNC 6.3C
DACA_HSYNC_B 6.2D
DACA_HSYNC_C 6.2G> 9.3G<
DACA_RED 6.3C
DACA_RED_F 6.3F> 9.3G<
DACA_RSET 6.3B
DACA_VDD 6.3B
DACA_VREF 6.3B
DACA_VSYNC 6.3C
DACA_VSYNC_C 6.3G> 9.3G<
DACA_VSYSNC_B 6.3D
DACC_BLUE 7.4C 7.5E
DACC_BLUE_F 7.5F
DACC_GREEN 7.4C 7.4E
DACC_GREEN_F 7.4F
DACC_HSYNC 7.3C
DACC_HSYNC_B 7.2D
DACC_HSYNC_C 7.2F
DACC_RED 7.4C 7.4E
DACC_RED_F 7.4F
DACC_RSET 7.3B
DACC_VDD 7.3B> 9.4A<
DACC_VDD_R 7.3B
DACC_VREF 7.3B
DACC_VSYNC 7.3C
DACC_VSYNC_B 7.3D
DACC_VSYNC_C 7.3F
DVI_HPD 9.5E> 12.2E<
DVI_HPD_F 9.5F
FBA_CLK0 3.3D< 4.1G< 4.2A<
4.2C< 4.5B<
FBA_CLK0* 3.4D> 4.1G< 4.2A<
4.2C< 4.5B<
FBA_CLK0_R 4.5B
FBA_CLK1 3.4D< 5.1G< 5.2A<
5.2C< 5.5B<
FBA_CLK1* 3.4D> 5.1G< 5.2A<
5.2C< 5.5B<
FBA_CLK1_R 5.5B
FBA_CMD<0> 3.2C 4.2B 4.2C
FBA_CMD<1> 3.2D< 4.1A< 4.1G<
5.1A<
FBA_CMD<1> 3.2C 4.1B 4.1C 5.1B
5.1C
FBA_CMD<2> 3.2C 4.1B 4.1C
FBA_CMD<3> 3.2C 4.1B 4.1C 5.1B
5.1C
FBA_CMD<4> 3.2C 5.2B 5.2C
FBA_CMD<5> 3.2C 5.2B 5.2C
FBA_CMD<6> 3.3C 5.2B 5.2C
FBA_CMD<8> 3.3C 4.1B 4.1C 5.1B
5.1C
FBA_CMD<9> 3.3C 4.1B 4.1C 5.1B
5.1C
FBA_CMD<10> 3.3C 4.2B 4.2C 5.2B
5.2C
FBA_CMD<11> 3.3C 3.3D 4.2B 4.2C
5.2B 5.2C
FBA_CMD<12> 3.3C 3.3D 4.2B 4.2C
5.2B 5.2C
FBA_CMD<13> 3.3C 5.1B 5.1C
FBA_CMD<14> 3.3C 4.2B 4.2C 5.2B
5.2C
FBA_CMD<15> 3.3C 4.1B 4.1C 5.1B
5.1C
FBA_CMD<16> 3.3C 4.2B 4.2C 5.2B
5.2C
FBA_CMD<17> 3.3C 4.2B 4.2C 5.2B
5.2C
FBA_CMD<18> 3.3C 4.2B 4.2C 5.2B
5.2C
FBA_CMD<19> 3.3C 4.2B 4.2C 5.2B
5.2C
FBA_CMD<20> 3.3C 4.2B 4.2C 5.2B
5.2C
FBA_CMD<21> 3.3C 4.2B 4.2C 5.2B
5.2C
FBA_CMD<22> 3.3C 4.2B 4.2C
FBA_CMD<23> 3.3C 4.2B 4.2C 5.2B
5.2C
FBA_CMD<24> 3.3C 4.2B 4.2C
FBA_CMD<25> 3.3C 4.1B 4.1C 5.1B
5.1C
FBA_CMD<27> 3.3C 4.2B 4.2C 5.2B
5.2C
FBA_DQ<0> 3.1B 4.3B
FBA_DQ<31..0> 4.3A<>
3.1A<> 4.1G<
FBA_DQ<63..0> 3.1A<> 4.1G<
5.3A<>
FBA_DQ<1> 3.1B 4.3B
FBA_DQ<2> 3.1B 4.3B
FBA_DQ<3> 3.1B 4.3B
FBA_DQ<4> 3.1B 4.3B
FBA_DQ<5> 3.1B 4.3B
FBA_DQ<6> 3.1B 4.3B
FBA_DQ<7> 3.1B 4.3B
FBA_DQ<8> 3.1B 4.4B
FBA_DQ<9> 3.1B 4.4B
FBA_DQ<10> 3.1B 4.4B
FBA_DQ<11> 3.1B 4.4B
FBA_DQ<12> 3.1B 4.4B
FBA_DQ<13> 3.1B 4.4B
FBA_DQ<14> 3.1B 4.4B
FBA_DQ<15> 3.2B 4.4B
FBA_DQ<16> 3.2B 4.3D
FBA_DQ<17> 3.2B 4.3D
FBA_DQ<18> 3.2B 4.3D
FBA_DQ<19> 3.2B 4.3D
FBA_DQ<20> 3.2B 4.3D
FBA_DQ<21> 3.2B 4.3D
FBA_DQ<22> 3.2B 4.3D
FBA_DQ<23> 3.2B 4.3D
FBA_DQ<24> 3.2B 4.4D
FBA_DQ<25> 3.2B 4.4D
FBA_DQ<26> 3.2B 4.4D
FBA_DQ<27> 3.2B 4.4D
FBA_DQ<28> 3.2B 4.4D
FBA_DQ<29> 3.2B 4.4D
FBA_DQ<30> 3.2B 4.4D
FBA_DQ<31> 3.2B 4.4D
FBA_DQ<32> 3.2B 5.3B
FBA_DQ<63..32> 3.1A<> 4.1G<
5.3A<>
FBA_DQ<33> 3.2B 5.3B
FBA_DQ<34> 3.2B 5.3B
FBA_DQ<35> 3.2B 5.3B
FBA_DQ<36> 3.2B 5.3B
FBA_DQ<37> 3.2B 5.3B
FBA_DQ<38> 3.2B 5.3B
FBA_DQ<39> 3.2B 5.3B
FBA_DQ<40> 3.2B 5.4B
FBA_DQ<41> 3.2B 5.4B
FBA_DQ<42> 3.2B 5.4B
FBA_DQ<43> 3.2B 5.4B
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FBA_DQ<45> 3.2B 5.4B
FBA_DQ<46> 3.3B 5.4B
FBA_DQ<47> 3.3B 5.4B
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FBA_DQ<49> 3.3B 5.3D
FBA_DQ<50> 3.3B 5.3D
FBA_DQ<51> 3.3B 5.3D
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FBA_DQ<57> 3.3B 5.4D
FBA_DQ<58> 3.3B 5.4D
FBA_DQ<59> 3.3B 5.4D
FBA_DQ<60> 3.3B 5.4D
FBA_DQ<61> 3.3B 5.4D
FBA_DQ<62> 3.3B 5.4D
FBA_DQ<63> 3.3B 5.4D
FBA_DEBUG 3.1G< 3.4C
FBA_DQM<0> 3.3B 4.3B
FBA_DQM<3..0> 4.4A<
5.2A> 4.1G<
FBA_DQM<7..0> 3.3A> 4.1G<
5.4A<
FBA_DQM<1> 3.3B 4.4B
FBA_DQM<2> 3.3B 4.3D
FBA_DQM<3> 3.3B 4.4D
FBA_DQM<4> 3.3B 5.3B
FBA_DQM<7..4> 3.3A> 4.1G<
5.4A<
FBA_DQM<5> 3.3B 5.4B
FBA_DQM<6> 3.3B 5.3D
FBA_DQM<7> 3.3B 5.4D
FBA_DQS<0> 3.4B 4.1G 4.4B
FBA_DQS<3..0> 4.4A<>
3.4A<> 4.1G< 5.1G<
FBA_DQS<7..0> 3.4A<> 4.1G< 5.1G<
5.4A<

FBA_DQS<1> 3.4B 4.1G 4.4B
FBA_DQS<2> 3.4B 4.1G 4.4D
FBA_DQS<3> 3.4B 4.1G 4.4D
FBA_DQS<4> 3.4B 5.1G 5.4B
FBA_DQS<7..4> 3.4A<> 4.1G< 5.1G<
5.4A<
FBA_DQS<5> 3.4B 5.1G 5.4B
FBA_DQS<6> 3.4B 5.1G 5.4D
FBA_DQS<7> 3.4B 5.1G 5.4D
FBA_DQSN<0> 3.4B 4.1G 4.4B
FBA_DQSN<3..0> 4.4A<>
3.4A<> 4.1G< 5.1G<
FBA_DQSN<7..0> 3.4A<> 4.1G< 5.1G<
5.4A<
FBA_DQSN<1> 3.4B 4.1G 4.4B
FBA_DQSN<2> 3.4B 4.1G 4.4D
FBA_DQSN<3> 3.4B 4.1G 4.4D
FBA_DQSN<4> 3.4B 5.1G 5.4B
FBA_DQSN<7..4> 3.4A<> 4.1G< 5.1G<
5.4A<
FBA_DQSN<5> 3.4B 5.1G 5.4B
FBA_DQSN<6> 3.4B 5.1G 5.4D
FBA_DQSN<7> 3.4B 5.1G 5.4D
FBA_PLLAVDD 3.5C
FBA_VREF_A 5.3E
FBA_VREF_B 4.3E
FBVDDQ 14.1G
FB_CAL_PD_VDDQ 3.4C
FB_CAL_PU_GND 3.4C
FB_CAL_TERM_GND 3.4C
GND_SENSE 2.4F
GPIO8_THERM_OVERT* 12.2F> 15.2E<
GPU_PLLVDD 12.1G< 12.4C
GPU_TESTMODE 12.3E
I2CA_SCL 6.1C< 12.1E>
I2CA_SCL_C 6.1G> 9.3G<
I2CA_SCL_R 6.1E
I2CA_SDA 6.2C<> 12.1E<>
I2CA_SDA_C 6.2G> 9.3G<
I2CA_SDA_R 6.1E
I2CB_SCL 7.1D< 12.1E>
I2CB_SCL_C 7.1E
I2CB_SCL_R 7.1E
I2CB_SDA 7.2D<> 12.1E<>
I2CB_SDA_C 7.2E
I2CB_SDA_R 7.2E
I2CH_SCL 12.3E> 12.3F<
I2CH_SDA 12.3E<> 12.3F>
IFPAB_HPD_C 9.3G
IFPAB_PLLVDD 9.1G> 9.3C
IFPAB_RSET 9.3C
IFPA_TXC 9.1G< 9.4D
IFPA_TXC* 9.1G< 9.3D
IFPA_TXD0 9.1G< 9.2E
IFPA_TXD0* 9.1G< 9.2E
IFPA_TXD1 9.1G< 9.3E
IFPA_TXD1* 9.1G< 9.3E
IFPA_TXD2 9.1G< 9.3E
IFPA_TXD2* 9.1G< 9.3E
IFPB_TXD4 9.1G< 9.3E
IFPB_TXD4* 9.1G< 9.3E
IFPB_TXD5 9.1G< 9.3E
IFPB_TXD5* 9.1G< 9.3E
IFPB_TXD6 9.1G< 9.3E
IFPB_TXD6* 9.1G< 9.3E
JTAG_TCLK 12.1C
JTAG_TDI 12.1C
JTAG_TDO 12.2C
JTAG_TMS 12.1C
JTAG_TRST* 12.2C
NVVDD 13.1F
NVVDD_SENSE 2.4F
PEX_PLLDVDD 2.4H> 16.2E<
PEX_PRSNT 2.1B
PEX_REFCLK 2.2C 2.5A<
PEX_REFCLK* 2.2C 2.5A<
PEX_RST* 2.2D> 2.2D> 15.2D<
PEX_RST_Q 9.5A< 15.2E>
PEX_RST_R* 15.2E
PEX_RX0 2.2C 2.4A<
PEX_RX0* 2.2C 2.4A<
PEX_RX1 2.2C 2.4A<
PEX_RX1* 2.2C 2.4A<
PEX_RX2 2.2C 2.4A<
PEX_RX2* 2.2C 2.4A<
PEX_RX3 2.3C 2.4A<
PEX_RX3* 2.3C 2.4A<
PEX_RX4 2.3C 2.4A<
PEX_RX4* 2.3C 2.4A<
PEX_RX5 2.3C 2.5A<
PEX_RX5* 2.3C 2.5A<
PEX_RX6 2.3C 2.5A<
PEX_RX6* 2.3C 2.5A<
PEX_RX7 2.3C 2.5A<
PEX_RX7* 2.3C 2.5A<
PEX_RX8 2.4C 2.5A<

PEX_RX8* 2.4C 2.5A<
PEX_RX9 2.4C 2.5A<
PEX_RX9* 2.4C 2.5A<
PEX_RX10 2.4C 2.5A<
PEX_RX10* 2.4C 2.5A<
PEX_RX11 2.4C 2.5A<
PEX_RX11* 2.4C 2.5A<
PEX_RX12 2.4C 2.5A<
PEX_RX12* 2.4C 2.5A<
PEX_RX13 2.5A< 2.5C
PEX_RX13* 2.5A< 2.5C
PEX_RX14 2.5A< 2.5C
PEX_RX14* 2.5A< 2.5C
PEX_RX15 2.5A< 2.5C
PEX_RX15* 2.5A< 2.5C
PEX_TERMP 2.5F
PEX_TX0 2.2A< 2.2E
PEX_TX0* 2.2A< 2.2E
PEX_TX1 2.2A< 2.2E
PEX_TX1* 2.2A< 2.2E
PEX_TX2 2.2A< 2.2E
PEX_TX2* 2.2A< 2.2E
PEX_TX3 2.3A< 2.3E
PEX_TX3* 2.3A< 2.3E
PEX_TX4 2.3A< 2.3E
PEX_TX4* 2.3A< 2.3E
PEX_TX5 2.3A< 2.3E
PEX_TX5* 2.3A< 2.3E
PEX_TX6 2.3A< 2.3E
PEX_TX6* 2.3A< 2.3E
PEX_TX7 2.2A< 2.3E
PEX_TX7* 2.2A< 2.3E
PEX_TX8 2.3A< 2.4E
PEX_TX8* 2.3A< 2.4E
PEX_TX9 2.3A< 2.4E
PEX_TX9* 2.3A< 2.4E
PEX_TX10 2.3A< 2.4E
PEX_TX10* 2.3A< 2.4E
PEX_TX11 2.3A< 2.4E
PEX_TX11* 2.3A< 2.4E
PEX_TX12 2.3A< 2.4E
PEX_TX12* 2.3A< 2.4E
PEX_TX13 2.3A< 2.5E
PEX_TX13* 2.3A< 2.5E
PEX_TX14 2.3A< 2.5E
PEX_TX14* 2.3A< 2.5E
PEX_TX15 2.3A< 2.5E
PEX_TX15* 2.3A< 2.5E
PEX_TX0 2.2C 2.3A<
PEX_TX0* 2.2C 2.3A<
PEX_TX1 2.3C 2.3A<
PEX_TX1* 2.2C 2.3A<
PEX_TX2 2.2C 2.3A<
PEX_TX2* 2.2C 2.3A<
PEX_TX3 2.3A< 2.3C
PEX_TX3* 2.3A< 2.3C
PEX_TX4 2.3A< 2.3C
PEX_TX4* 2.3A< 2.3C
PEX_TX5 2.3A< 2.3C
PEX_TX5* 2.3A< 2.3C
PEX_TX6 2.3A< 2.3C
PEX_TX6* 2.3C 2.4A<
PEX_TX7 2.3C 2.4A<
PEX_TX7* 2.3C 2.4A<
PEX_TX8 2.4A< 2.4C
PEX_TX8* 2.4A< 2.4C
PEX_TX9 2.4A< 2.4C
PEX_TX9* 2.4A< 2.4C
PEX_TX10 2.4A< 2.4C
PEX_TX10* 2.4A< 2.4C
PEX_TX11 2.4A< 2.4C
PEX_TX11* 2.4A< 2.4C
PEX_TX12 2.4A< 2.4C
PEX_TX12* 2.4A< 2.4C
PEX_TX13 2.4A< 2.5C
PEX_TX13* 2.4A< 2.5C
PEX_TX14 2.4A< 2.5C
PEX_TX14* 2.4A< 2.5C
PEX_TX15 2.4A< 2.5C
PEX_TX15* 2.4A< 2.5C
PSI_BOOT_NVVDD 13.3D
PSI_BOOT_RC_NVVDD 13.3E
PS1_CP 13.3C
PS1_FB_NVDD 13.4D
PS1_FB_RC_NVVDD 13.4E
PS1_UG_NVDD 13.3D
PSI_PHASE_NVDD 13.3D
PS1_RC_12V 13.3C
PS1_RC_NVDD 13.3F
PS1_UG_NVDD 13.3D
PS1_UG_R_NVDD 13.3D
PS1_VSEN_NVDD 13.4F
PS2_RC_5V 14.1B
PS3_CP_FBVDDQ 14.4E
PS3_CP_RC_FBVDDQ 14.4E
PS3_EN_FBVDDQ 14.4A

PS3_EN_FBVDDQ* 14.4B
PS3_FB_FBVDDQ 14.4E
PS3_FSW_FBVDDQ 14.3E
PS3_PHASE_FBVDDQ 14.2E 14.4E
PS4_BOOT_FBVDDQ 14.2D
PS4_EN_FBVDDQ 14.2C
PS4_FB_FBVDDQ 14.3D
PS4_RVDDQ_FBVDDQ 14.2D
ROM_CS* 12.3E 12.3F
ROM_SCLK 11.1A< 11.1A< 12.2F>
12.2F> 12.2F>
ROM_SI 11.1A< 11.1A< 12.3F>
12.3F> 12.3F>
ROM_SO 11.1A< 11.1A< 12.3F>
12.3F> 12.3F>
SNN_3V3AUX 2.1B
SNN_BUFRST* 12.3E
SNN_DACB_BLUE 6.3E
SNN_DACB_CSYNC 6.3E
SNN_DACB_GREEN 6.3E
SNN_DACB_RED 6.3E
SNN_DACB_RSET 6.3C
SNN_DACB_VREF 6.3C
SNN_FBA1_NC_A2 4.3B
SNN_FBA1_NC_E3 4.2B
SNN_FBA1_NC_R3 4.2B
SNN_FBA1_NC_R7 4.2B
SNN_FBA1_NC_R8 4.2B
SNN_FBA2_NC_A2 4.3C
SNN_FBA2_NC_E3 4.3C
SNN_FBA2_NC_R3 4.2C
SNN_FBA2_NC_R7 4.2C
SNN_FBA2_NC_R8 4.2C
SNN_FBA3_NC_A2 5.3B
SNN_FBA3_NC_E3 5.3B
SNN_FBA3_NC_R3 5.2B
SNN_FBA3_NC_R7 5.2B
SNN_FBA3_NC_R8 5.2B
SNN_FBA4_NC_A2 5.3C
SNN_FBA4_NC_E3 5.3C
SNN_FBA4_NC_R3 5.2C
SNN_FBA4_NC_R7 5.2C
SNN_FBA4_NC_R8 5.2C
SNN_FBA_CMD7 3.3C
SNN_FBA_CMD26 3.3C
SNN_FBA_CMD28 3.3C
SNN_FBVDDQ_SYNC 14.4D
SNN_FB_VREF 3.5B
SNN_GPIO1 12.2E
SNN_GPIO2 12.2E
SNN_GPIO3 12.2E
SNN_GPIO4 12.2E
SNN_GPIO5 12.2E
SNN_GPIO6 12.2E
SNN_GPIO7 12.2E
SNN_GPIO9 12.2E
SNN_GPIO10 12.2E
SNN_GPIO11 12.2E
SNN_GPIO12 12.2E
SNN_GPIO13 12.2E
SNN_GPIO14 12.2E
SNN_GPIO15 12.2E
SNN_GPIO16 12.2E
SNN_GPIO17 12.2E
SNN_GPIO18 12.2E
SNN_GPIO19 12.2E
SNN_GPU_SPDIF 12.3C
SNN_HDA_BCLK 10.5C
SNN_HDA_RST 10.5C
SNN_HDA_SDI 10.5C
SNN_HDA_SDO 10.5C
SNN_HDA_SYNC 10.5C
SNN_HDCP_NC 12.4G
SNN_I2CC_SCL 12.1E
SNN_I2CC_SDA 12.1E
SNN_I2CD_SCL 12.1E
SNN_I2CD_SDA 12.1E
SNN_I2CE_SCL 12.2E
SNN_I2CE_SDA 12.2E
SNN_I2CS_SCL 12.2C
SNN_I2CS_SDA 12.2C
SNN_IFPB_TXC 9.4D
SNN_IFPB_TXC* 9.4D
SNN_IFPB_TXD3 9.3D
SNN_IFPB_TXD3* 9.3D
SNN_IFPB_TXD7 9.3D
SNN_IFPB_TXD7* 9.3D
SNN_IFPC_AUX 10.2C
SNN_IFPC_AUX* 10.2C
SNN_IFPC_L0 10.2C
SNN_IFPC_L0* 10.2C
SNN_IFPC_L1 10.2C
SNN_IFPC_L1* 10.2C
SNN_IFPC_L2 10.2C
SNN_IFPC_L2* 10.2C
SNN_IFPC_L3 10.2C

SNN_IFPC_L3* 10.2C
SNN_IFPC_RSET 10.1A
SNN_IFPE_AUX 10.3C
SNN_IFPE_AUX* 10.3C
SNN_IFPE_L0 10.3C
SNN_IFPE_L0* 10.3C
SNN_IFPE_L1 10.3C
SNN_IFPE_L1* 10.3C
SNN_IFPE_L2 10.3C
SNN_IFPE_L2* 10.3C
SNN_IFPE_L3 10.3C
SNN_IFPE_L3* 10.3C
SNN_IFPE_RSET 10.3A
SNN_NC01 10.1G
SNN_NC02 10.1G
SNN_NC03 10.1G
SNN_NC04 10.1G
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SNN_PEX_SMDAT 2.1C
SNN_PEX_TCLK 2.1C
SNN_PEX_TDI 2.1C
SNN_PEX_TDO 2.1C
SNN_PEX_TMS 2.1C
SNN_PEX_TRST* 2.1C
SNN_PEX_TSTCLK_OUT 2.5F
SNN_PEX_TSTCLK_OUT 2.5F
*
SNN_PEX_WAKE* 2.2C
SNN_PE_PRSNT2_A 2.1B
SNN_PE_PRSNT2_B 2.2B
SNN_PE_PRSNT2_C 2.3B
SNN_PE_RSVD2 2.2B
SNN_PE_RSVD3 2.2B
SNN_PE_RSVD4 2.2B
SNN_PE_RSVD5 2.2B
SNN_PE_RSVD6 2.3B
SNN_PE_RSVD7 2.4B
SNN_PE_RSVD8 2.4B
SNN_RFU_AE9 2.2E
SNN_RFU_AG9 2.5F
SNN_RFU_C15 12.3C
SNN_RFU_D15 12.3C
SNN_RFU_F6 12.3E
SNN_RFU_J5 12.3E
SNN_RFU_J22 3.3C
SNN_RFU_L22 3.3C
STRAP3 11.1A< 11.1A< 12.3C>
STRAP1 11.1A< 11.1A< 12.3C>
STRAP2 11.1A< 11.1A< 12.3C>
STRAP_CAL_PU_GND6 12.3C
STRAP_CAL_PU_GND1 12.3C
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NV_PN	600-10636-BASE-000 A		
ID		PAGE	
NAME	<ENGINEER>	DATE	23-JUL-2009

Title: Cref Part Report
Design: p636
Date: Jul 10 17:01:46 2009

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