P393-A01 Base Design

P393-A01, G92, 8Mx32/16Mx32 GDDR3 (800/1000 MHz),
DVI-I-DL, DVI-I-DL/DisplayPort, HDTVout/Stereo

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V117-0D Base on P393
1.page 10 DAC-A Co-lay slim D-sub with DVI
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3.page 17 Modify SPIDF in circuit and co-lay MAX6649 circuit with ATD7473
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5.page 22 Modify 1V2 and FBVDD power circuit.
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SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10393-base-100	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU_DT_0000	600-10393-0000-100	P393 G92-300 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
2	SKU_DT_0002	600-10393-0002-100	P393 G92-200 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
3	SKU_WS_0500	600-50393-0500-100	P393 G92-875 512MB GDDR3 16Mx32 DVI-I+DP+STEREO
4	SKU_WS_0501	600-50393-0501-100	P393 G92-850 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
5	SKU_DT_0004	600-10393-0004-100	P393 G92-270 512MB GDDR3 16Mx32 DVI-I+DVI-I+HDTV
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Overview

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SUMMARY
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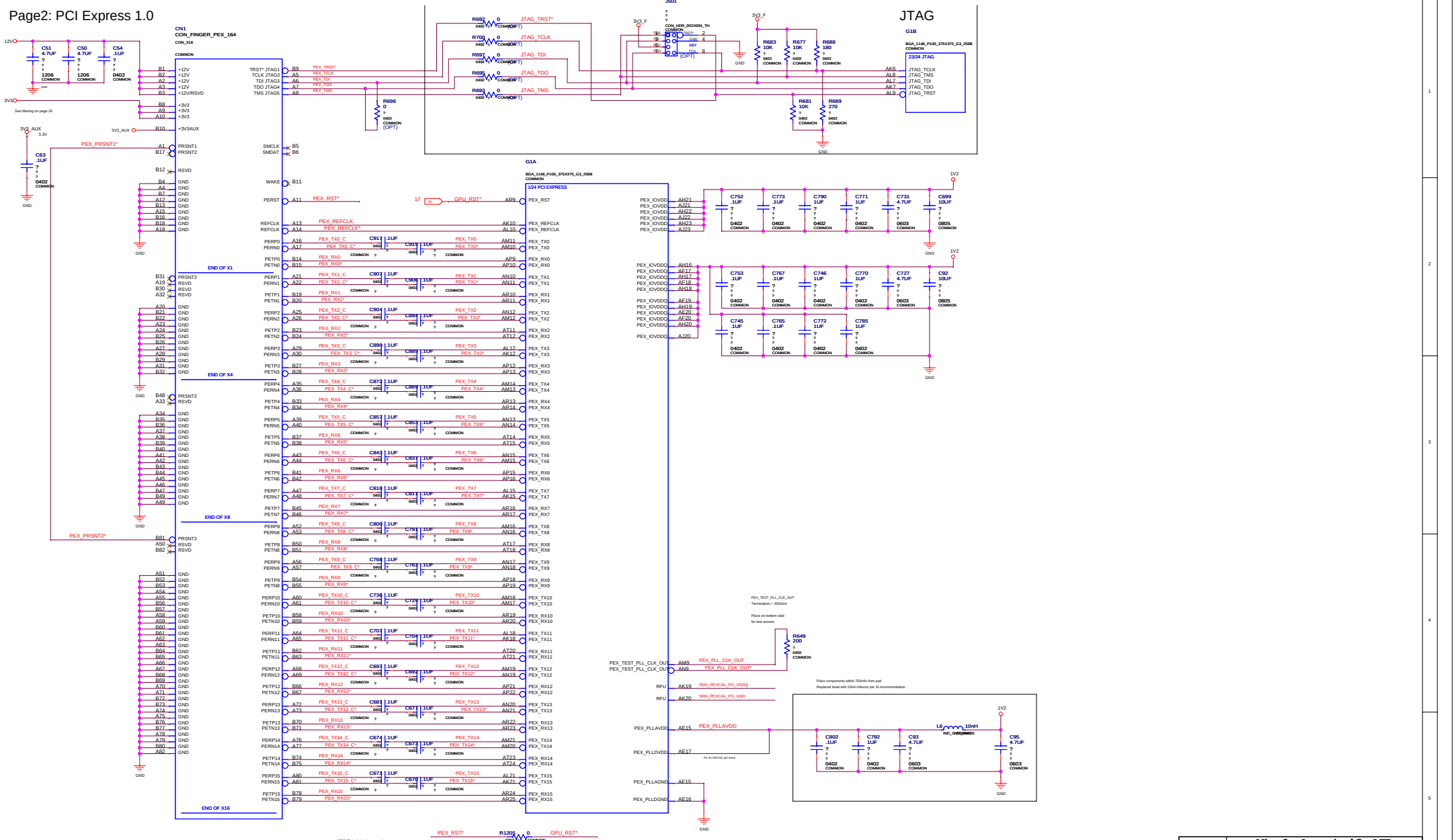
Page2: PCI Express 1.0



ASSEMBLY	P303 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI Express 1.0

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PCI Express 1.0

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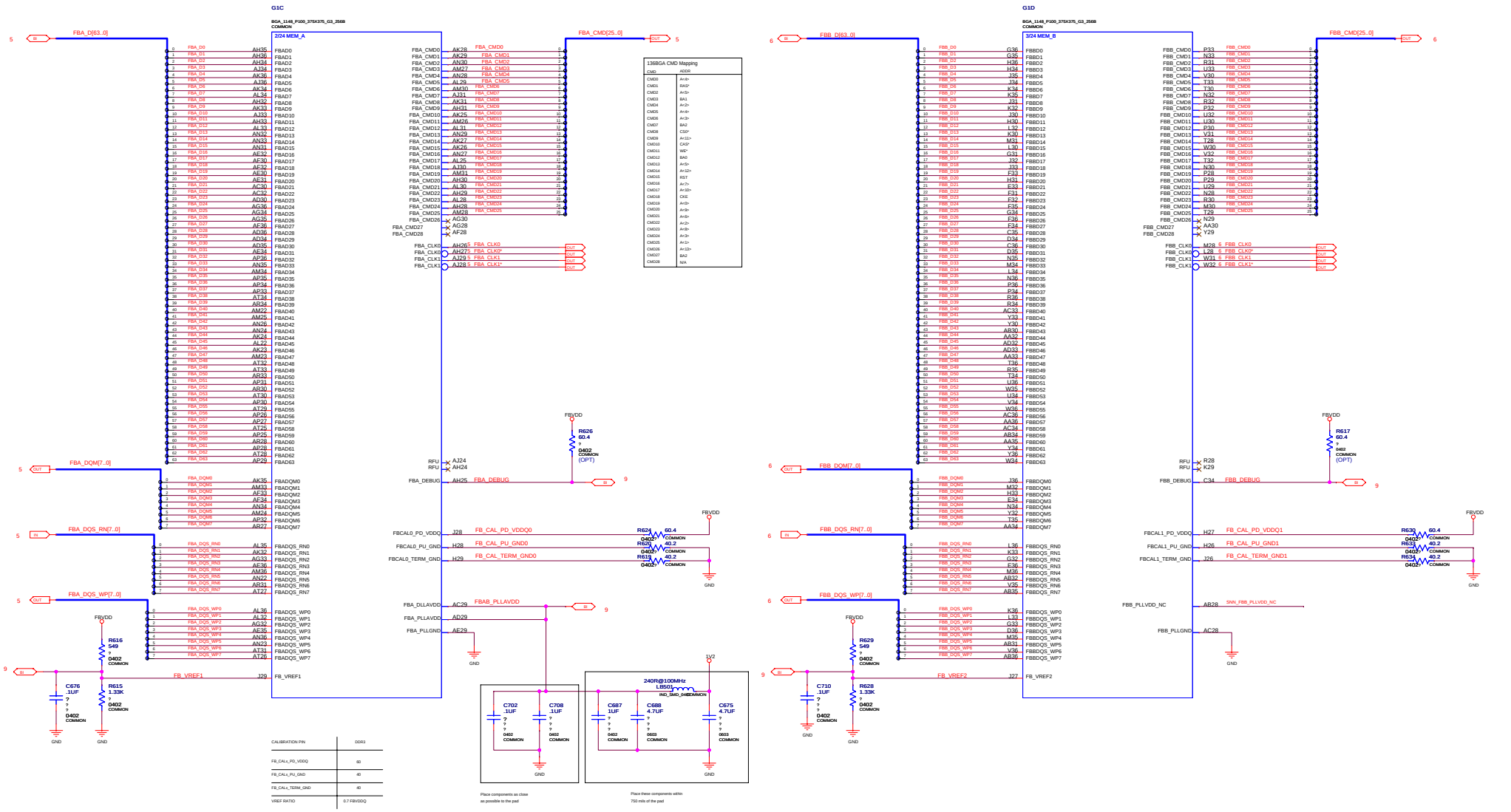
Page3: MEMORY: GPU Partition A/B



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: GPU Partition A/B

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MEMORY: GPU Partition A/B

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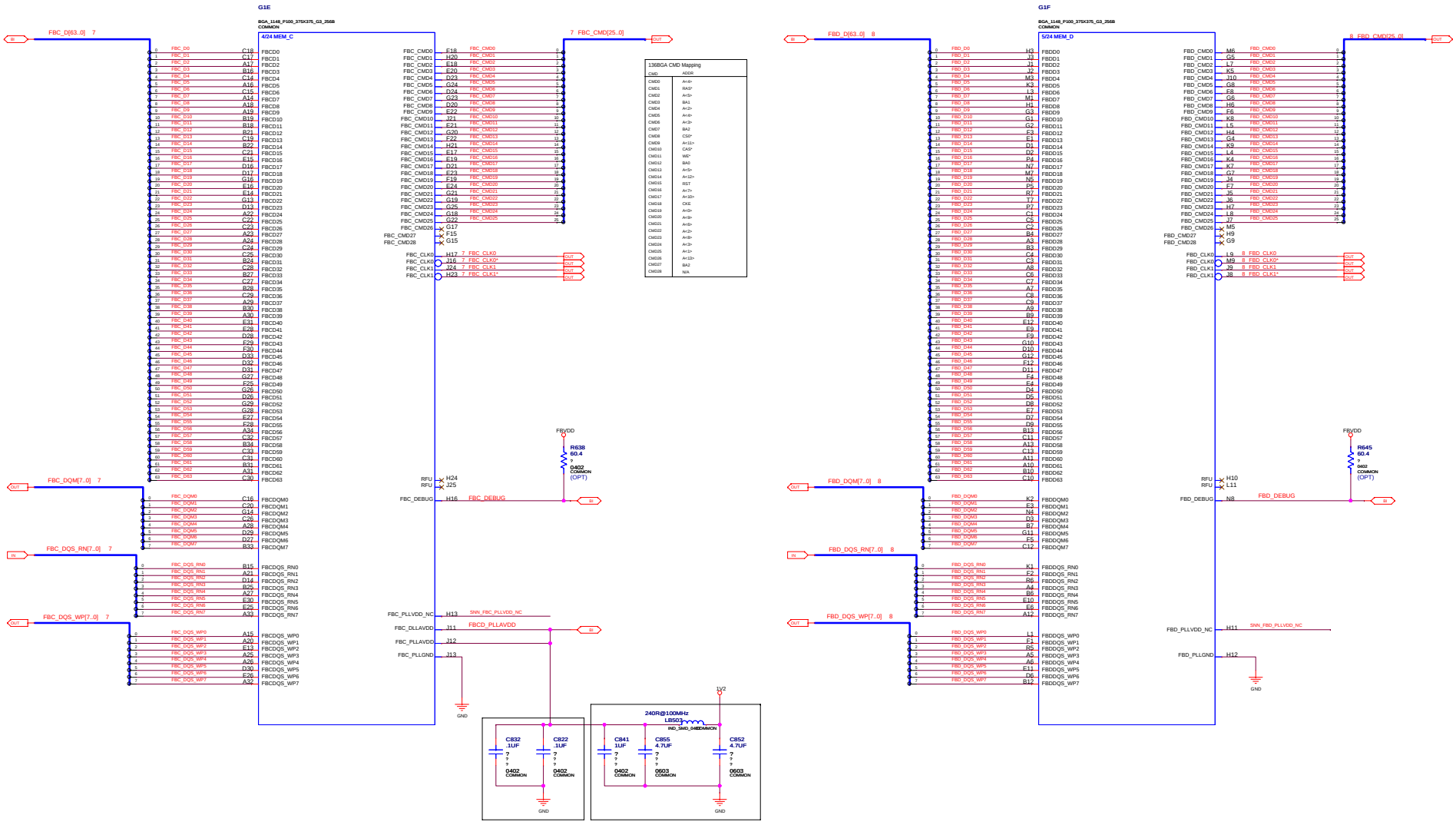
Page4: MEMORY: GPU Partition C/D



ASSEMBLY: P383 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: MEMORY: GPU Partition C/D

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MEMORY: GPU Partition C/D

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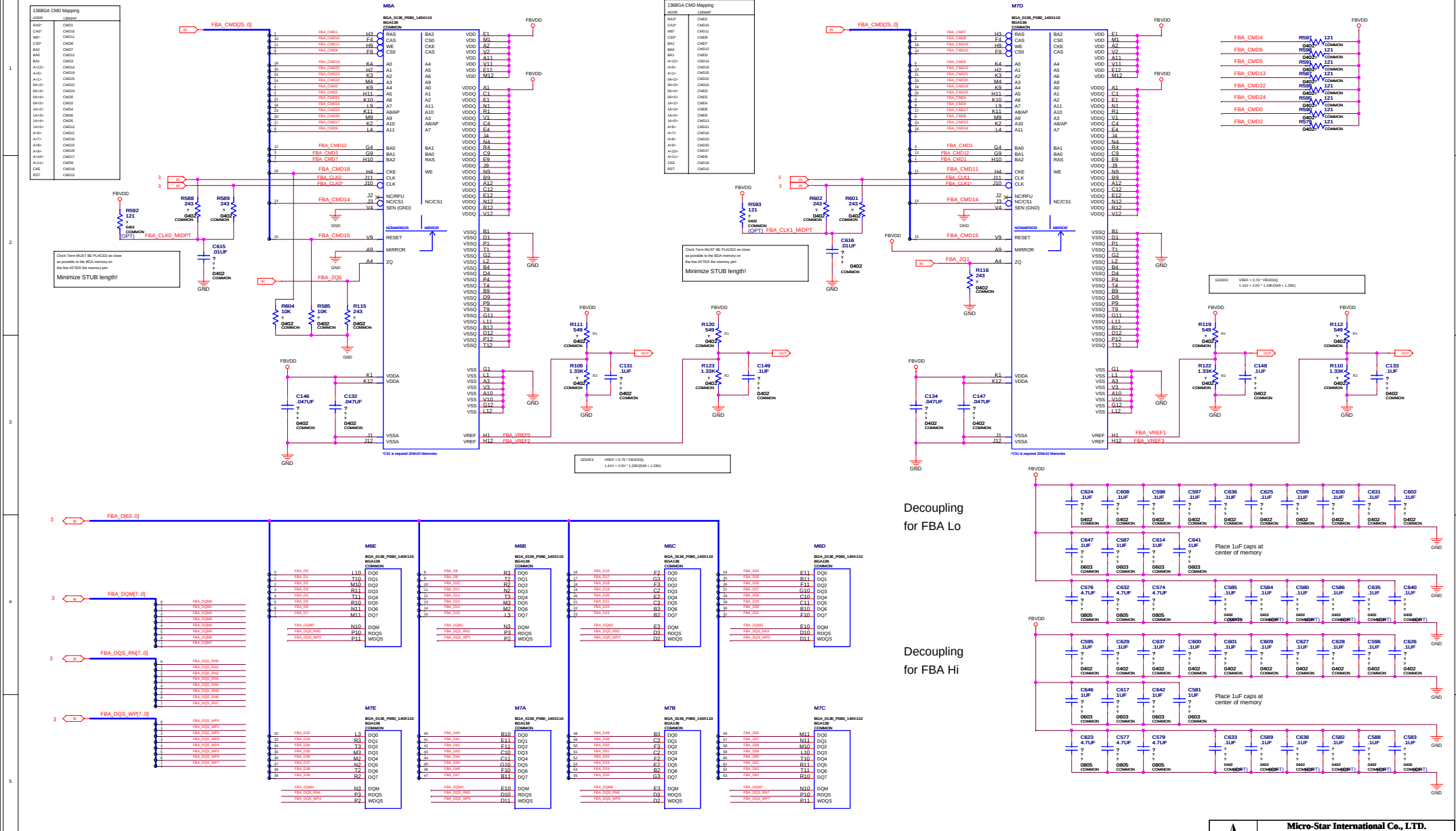
Page5: FBA Partition



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PAGE DETAIL	FBA Partition

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FBA Partition

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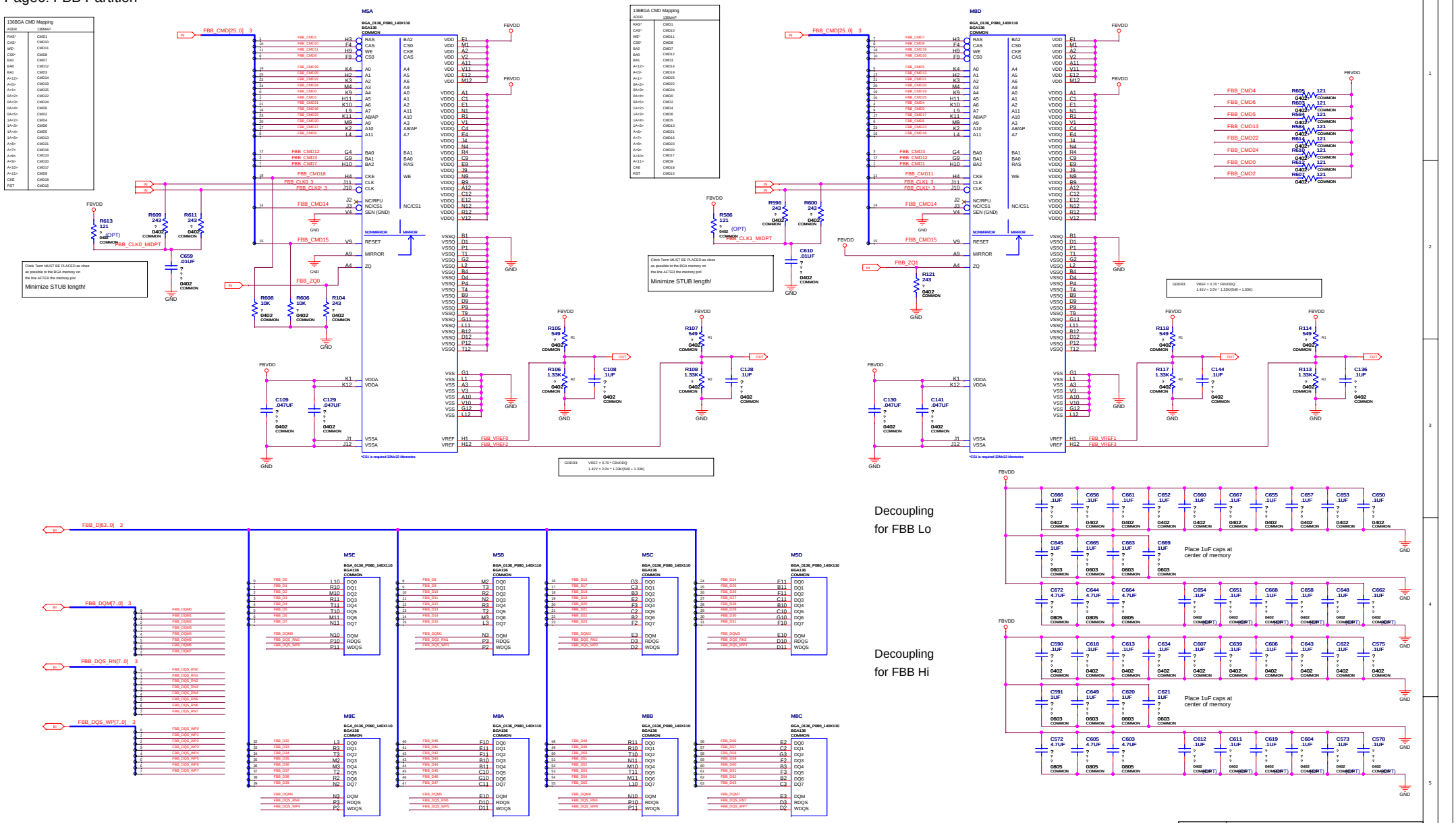
Page6: FBB Partition



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PAGE DETAIL: FBB Partition

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FBB Partition

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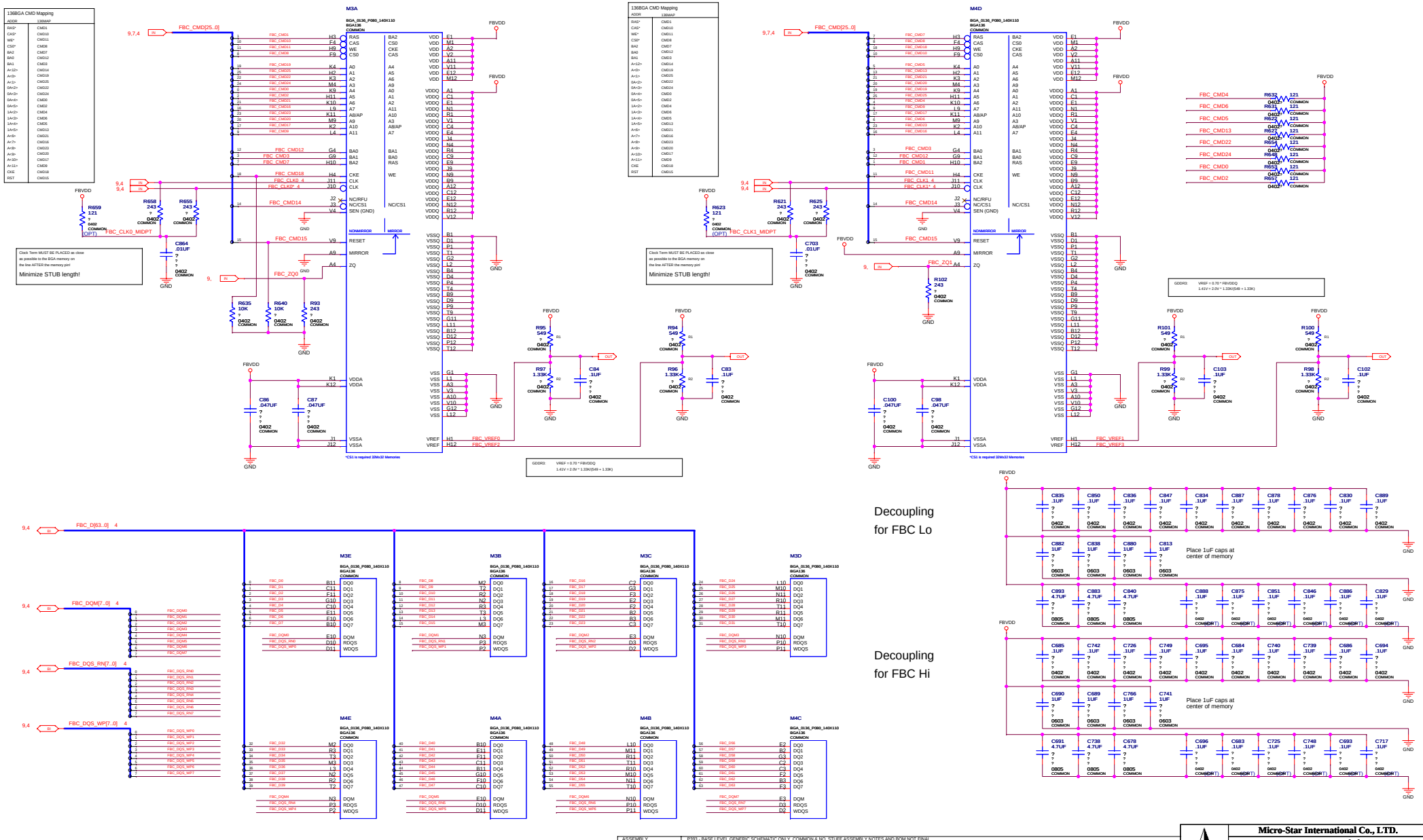
Page7: FBC Partition



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FBC Partition

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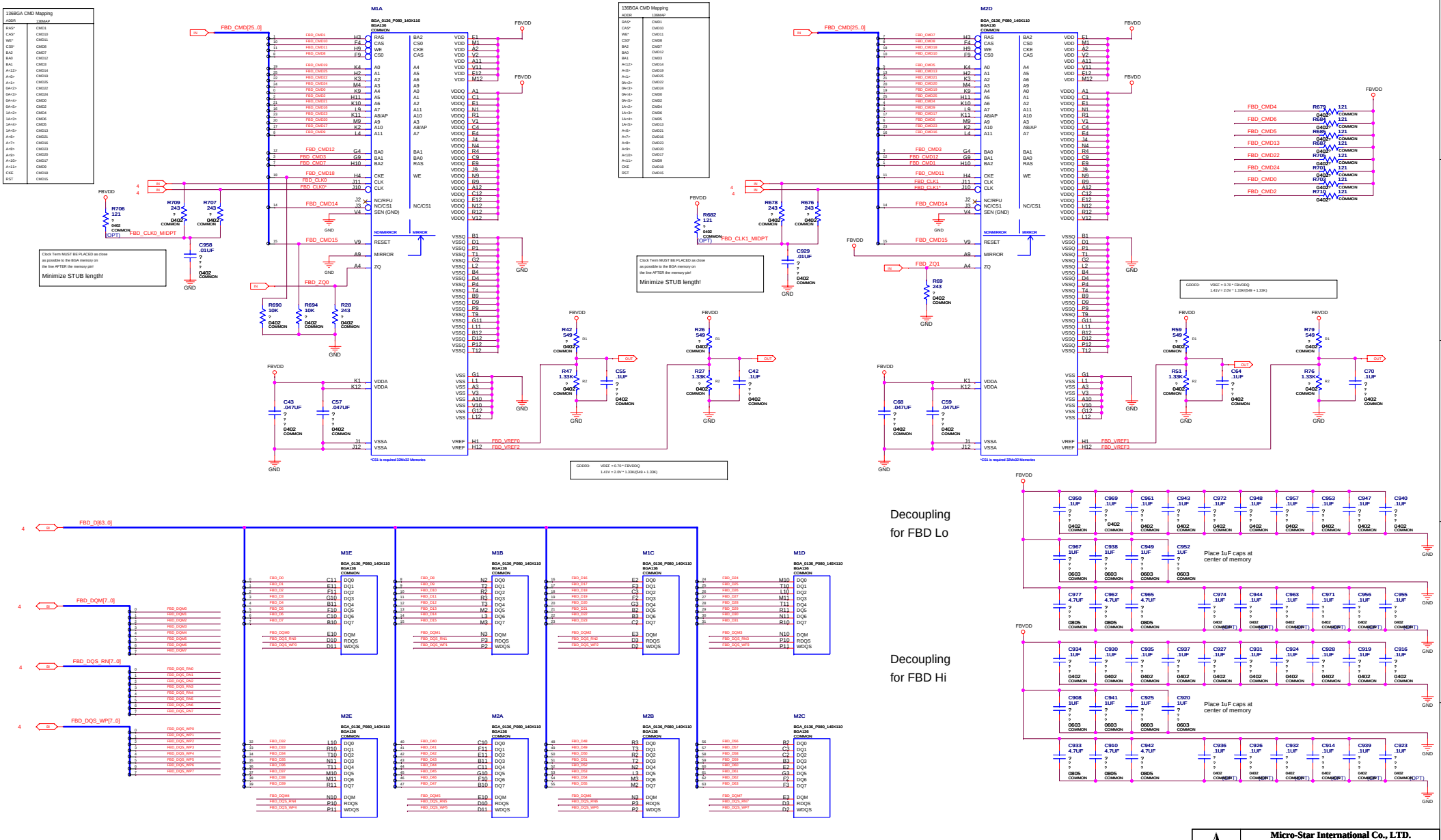
Page8: FBD Partition



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PAGE DETAIL: FBD Partition

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FBD Partition

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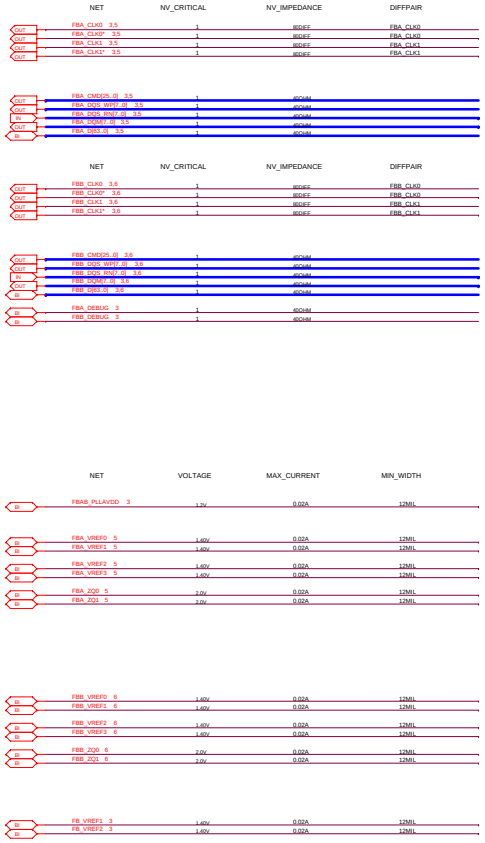
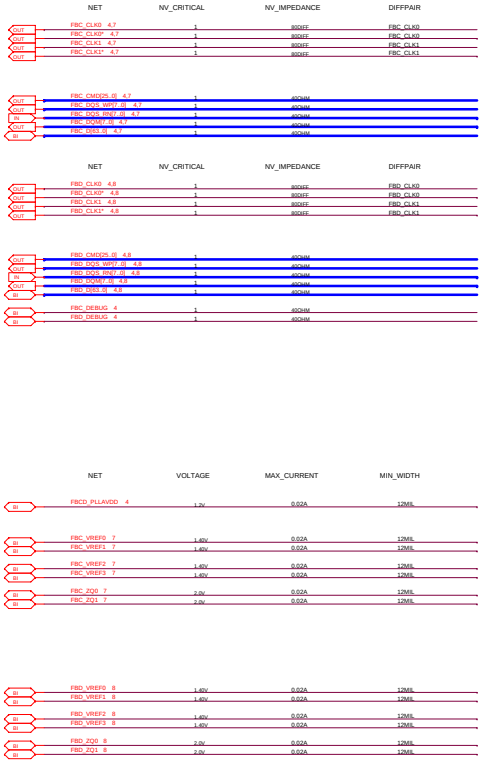
Page9: FrameBuffer Net Rules

NET RULES for FrameBuffer A/B



NET RULES for FrameBuffer C/D



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FrameBuffer Net Rules

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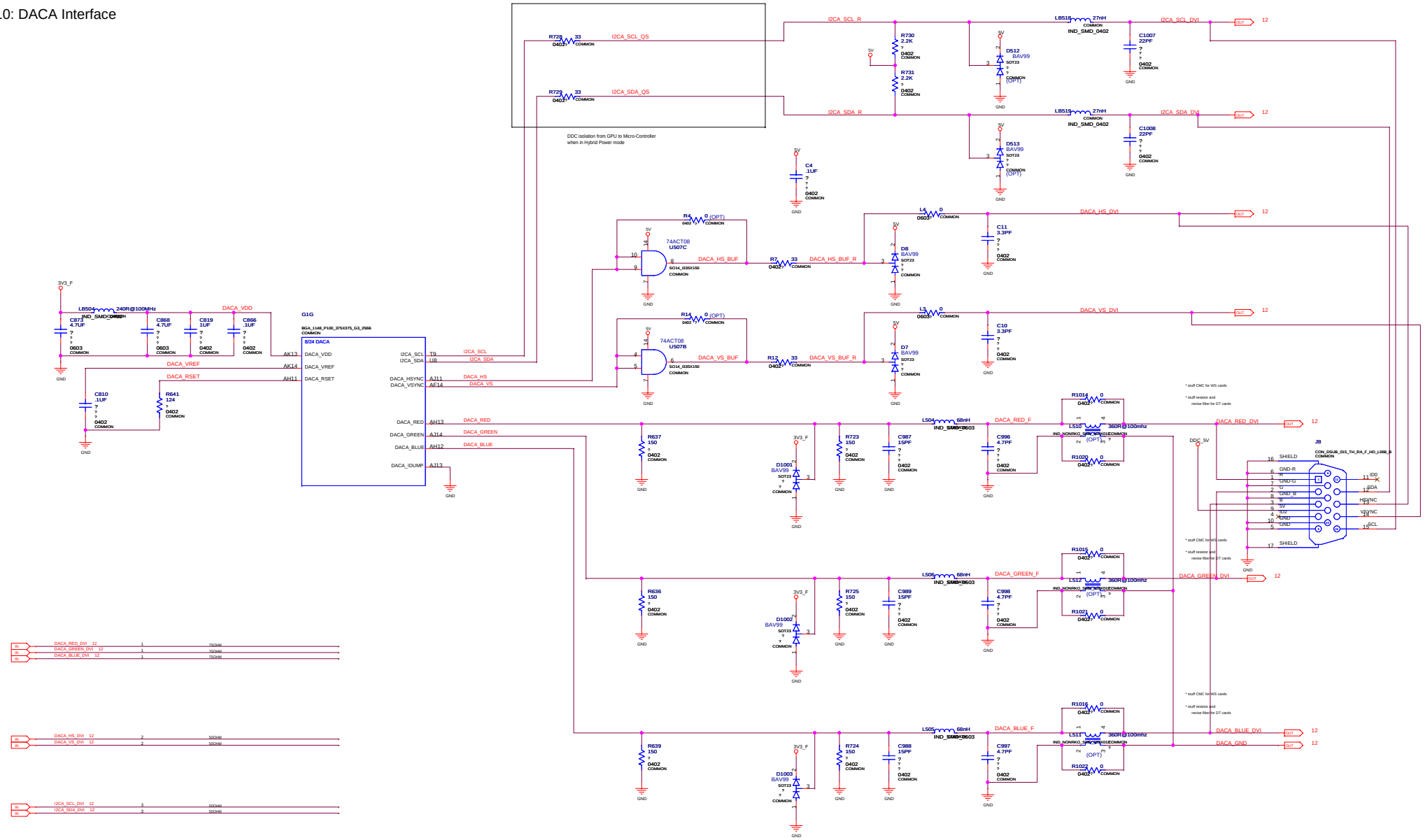
Page10: DACA Interface



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA Interface

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DACA Interface

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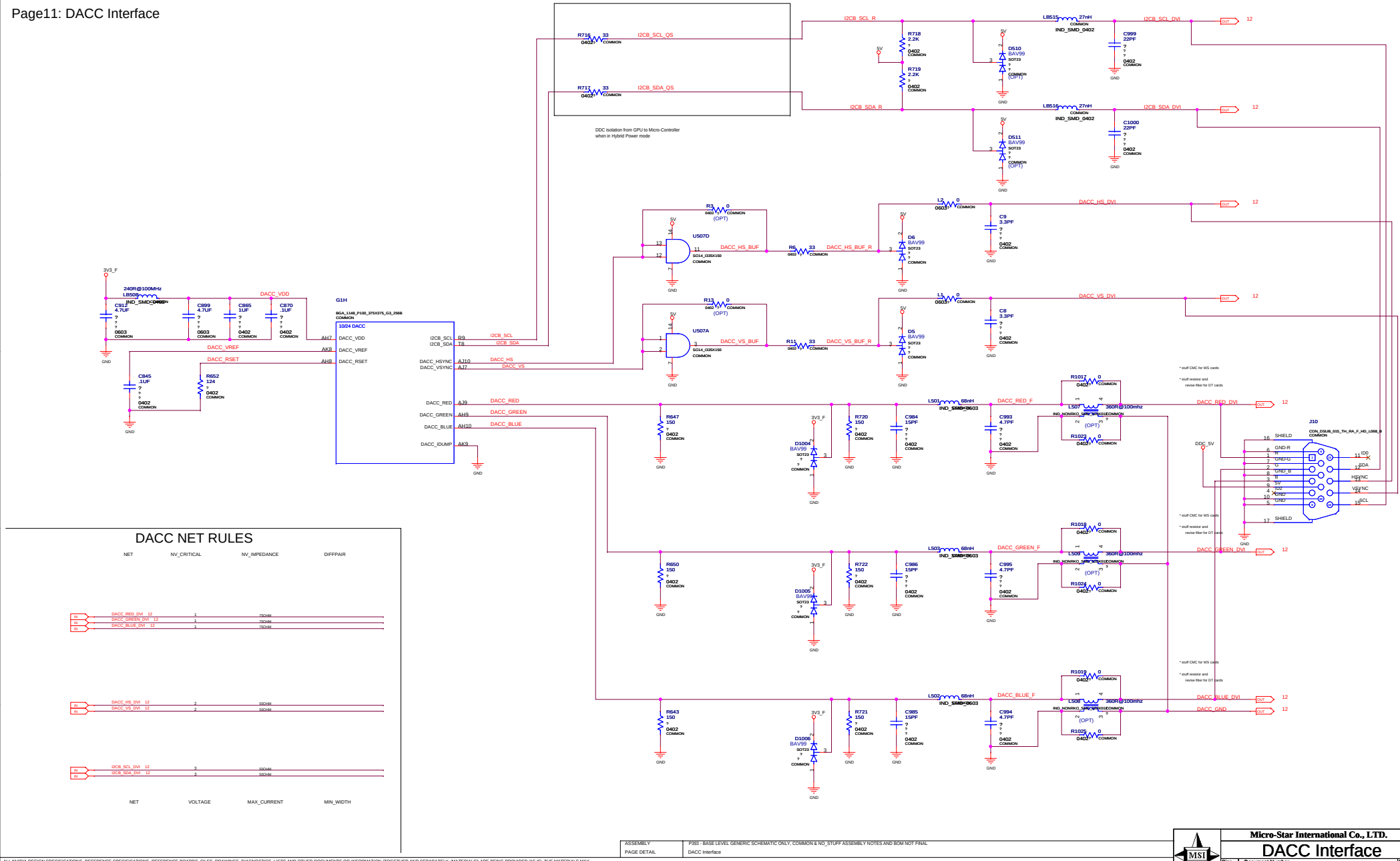
Page11: DACC Interface



DACC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACC_RED_DVI 12	1	75OHM	
DACC_GREEN_DVI 12	1	75OHM	
DACC_BLUE_DVI 12	1	75OHM	
DACC_HS_DVI 12	2	50OHM	
DACC_VS_DVI 12	2	50OHM	
I2CB_SCL_DVI 12	3	50OHM	
I2CB_SDA_DVI 12	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC Interface

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DACC Interface

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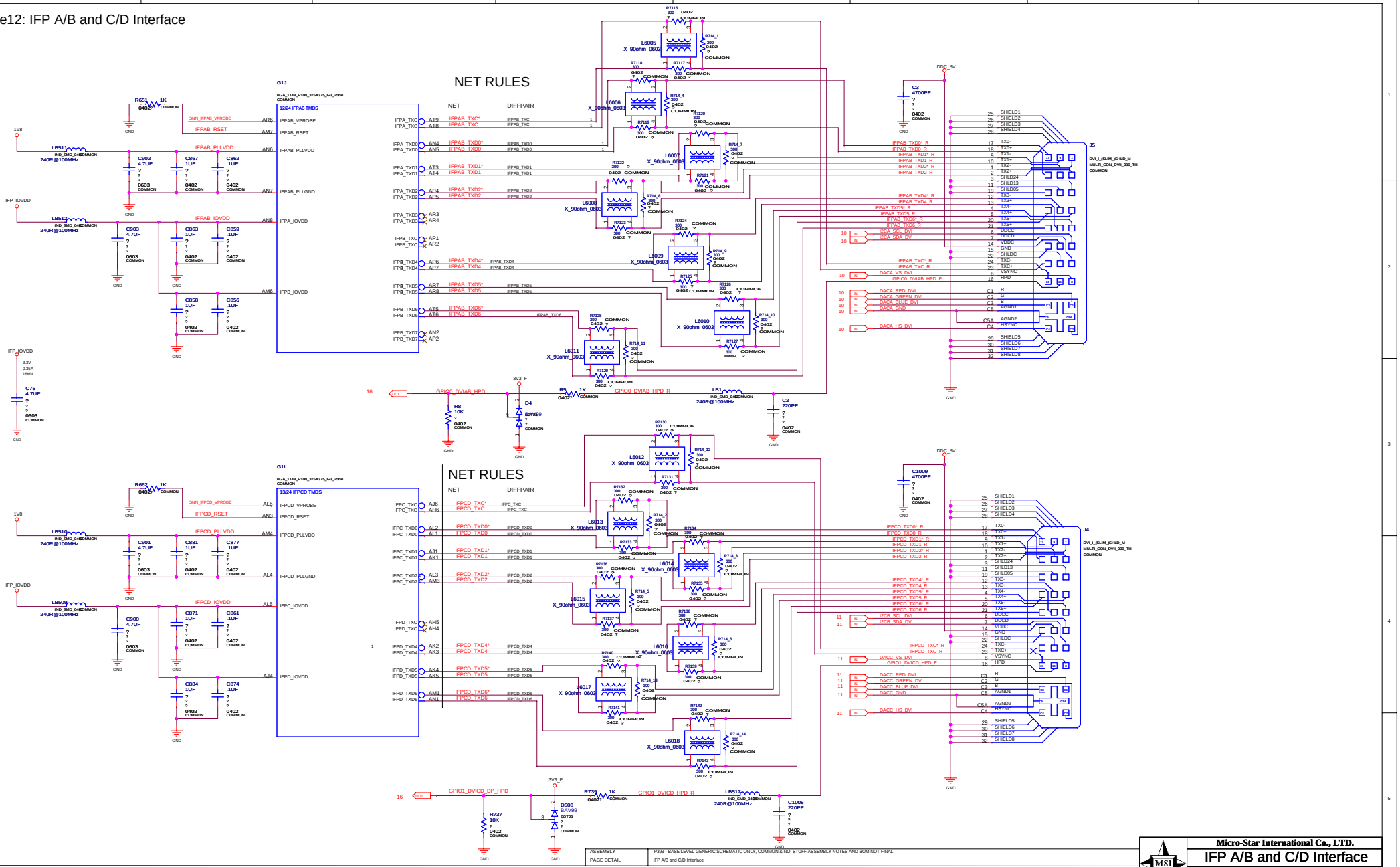
Page12: IFP A/B and C/D Interface



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IFP A/B and C/D Interface

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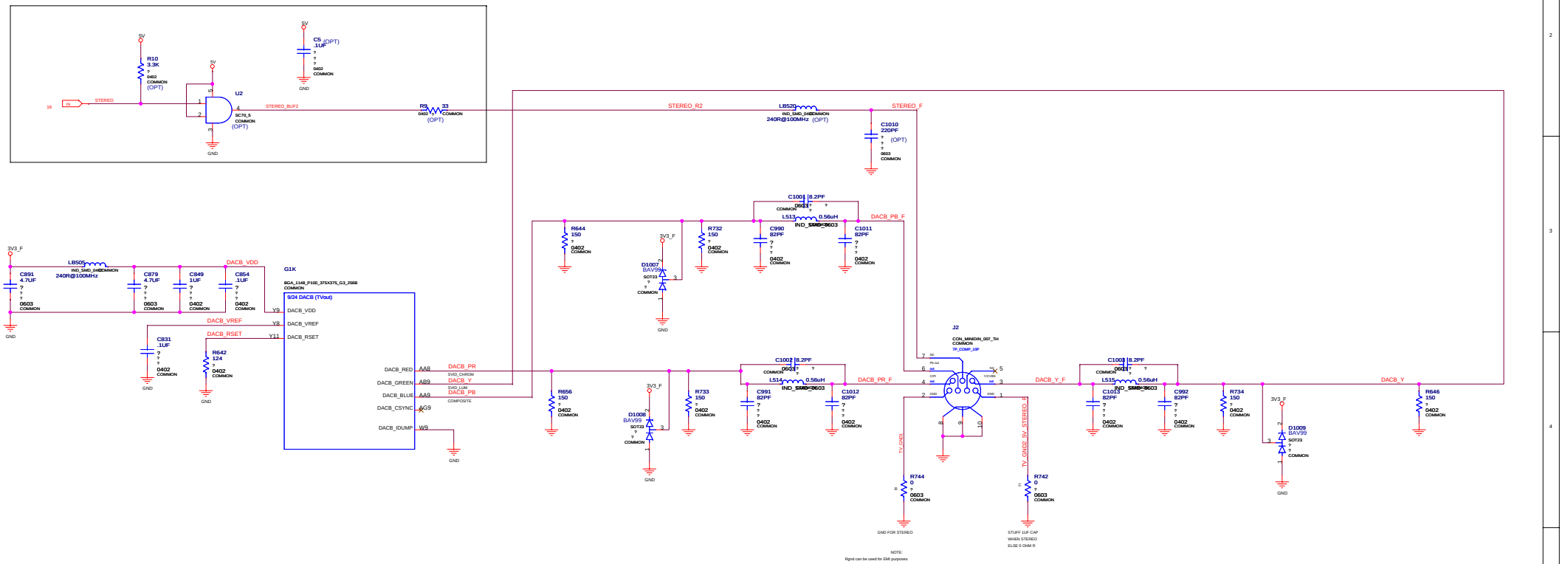
Page13: DACB and Stereo Interface

DACB,STEREO, FL NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR

Stereo



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB and Stereo Interface

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DACB and Stereo Interface

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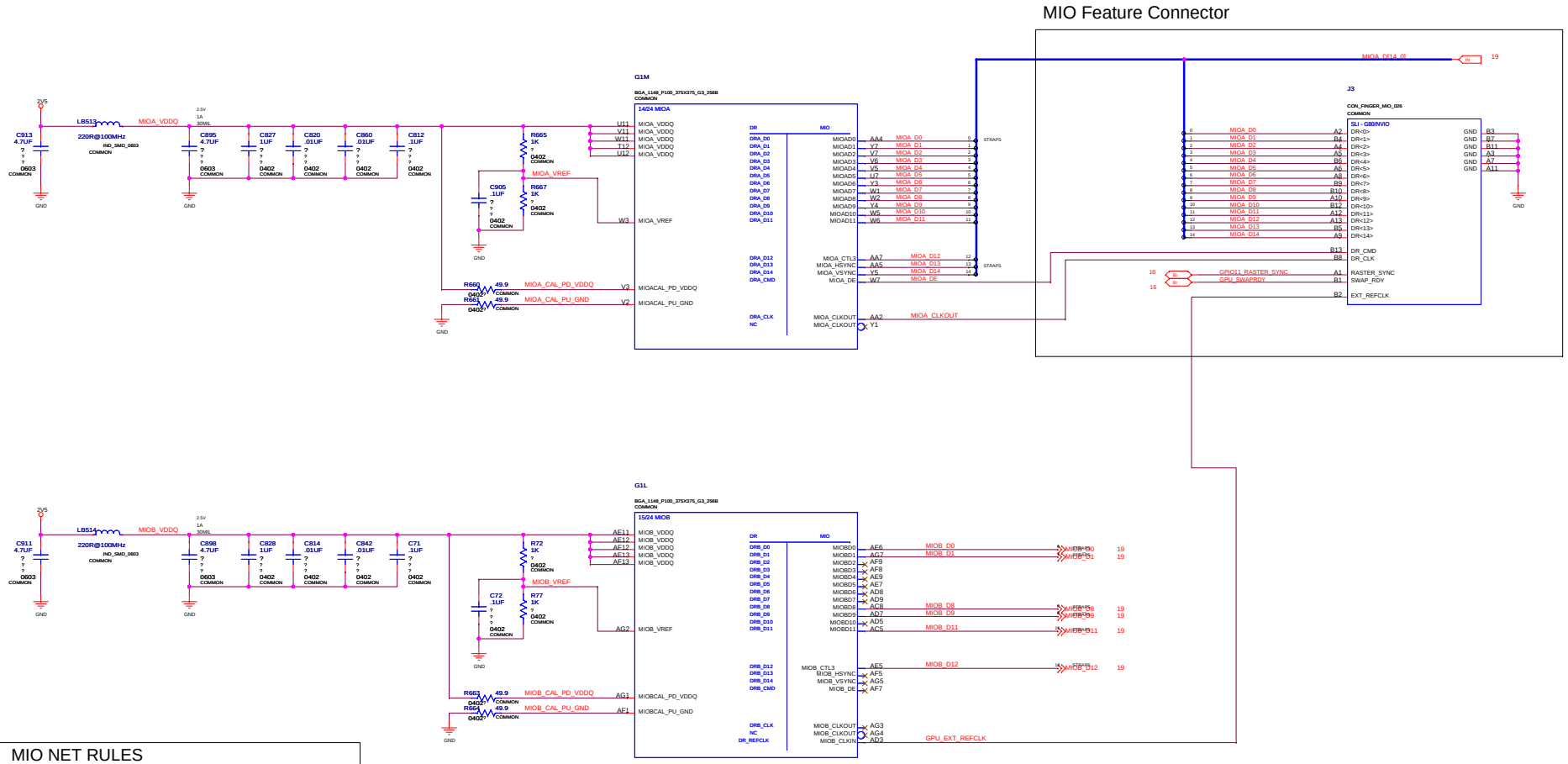
Page14: Multi-use IO(MIO) Interface



MIO NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
MIOA_D[14..0]_19	1	60OHM	

ASSEMBLY: P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: Multi-use IO(MIO) Interface

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Multi-use IO(MIO) Interface

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Page15: Display Port (Analogix ANX9802/ANX9805)

* I2C keeper circuit removed

* ANX9805 support

pin 76 - GPIO3 to DP mode, from pin 13, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 74 - GPIO2, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 73 - CEC support via FET and pull-up, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 71 - SPDIF1 - tie to GND, input select 0/1 through internal register

pin 70 - SPDIF0 - support for Audio input, grounded on ANX9802
- place GND resistor away from ANX device if needed

pin 68 - NC - tie to GND

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display Port

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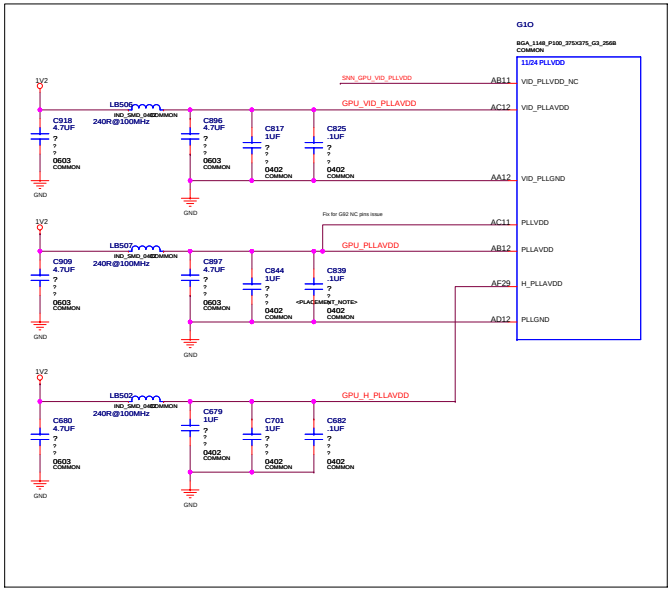
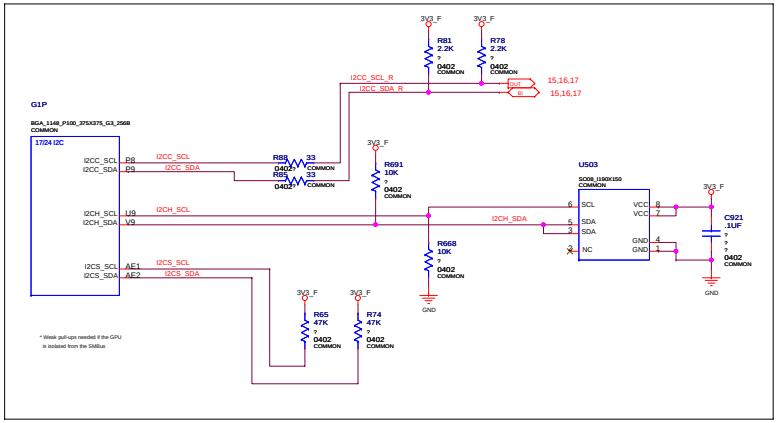
Page16: MISC: GPIO, I2C, BIOS, PLL, and XTAL

PLLVDD/VID_PLLVDD

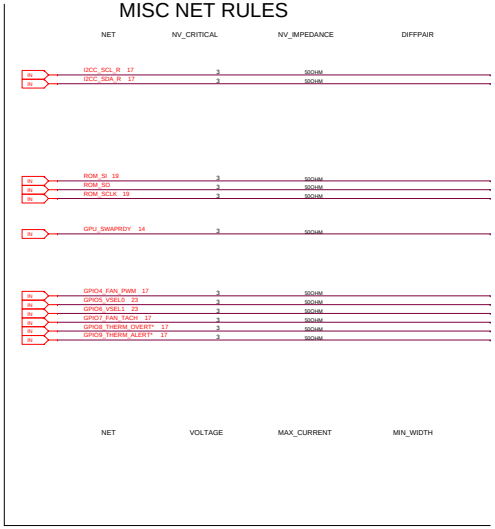


I2CC / I2CH(+ HDCP ROM) / I2CS

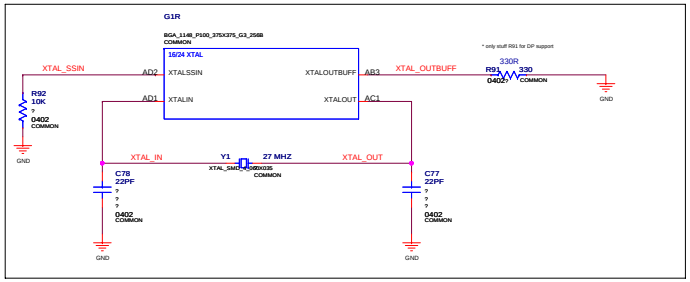


I2CS isolation for Hybrid Power

MISC NET RULES

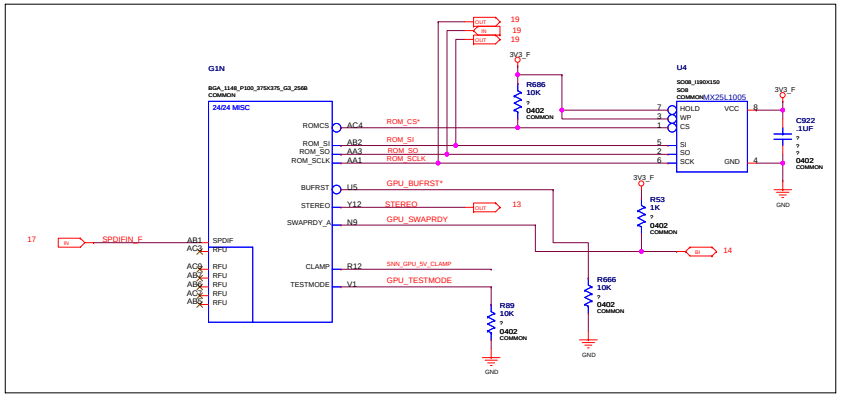


XTAL

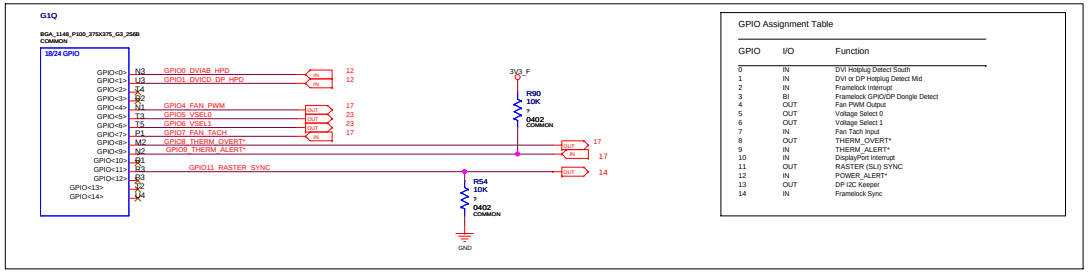


ROM / MISC

(BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)



GPIO



GPIO Assignment Table

GPIO	I/O	Function
0	IN	DVI Hotplug Detect South
1	IN	DVI or DP Hotplug Detect Mid
2	IN	Framelock Interrupt
3	BI	Framelock GPIO/DP Dongle Detect
4	OUT	Fan PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fan Tach Input
8	OUT	THERM_OVERT*
9	IN	THERM_ALERT*
10	IN	DisplayPort Interrupt
11	OUT	RASTER (SLI) SYNC
12	IN	POWER_ALERT*
13	OUT	DP I2C Keeper
14	IN	Framelock Sync

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC: GPIO, I2C, BIOS, PLL, and XTAL

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GPIO, I2C, BIOS, PLL, and XTAL

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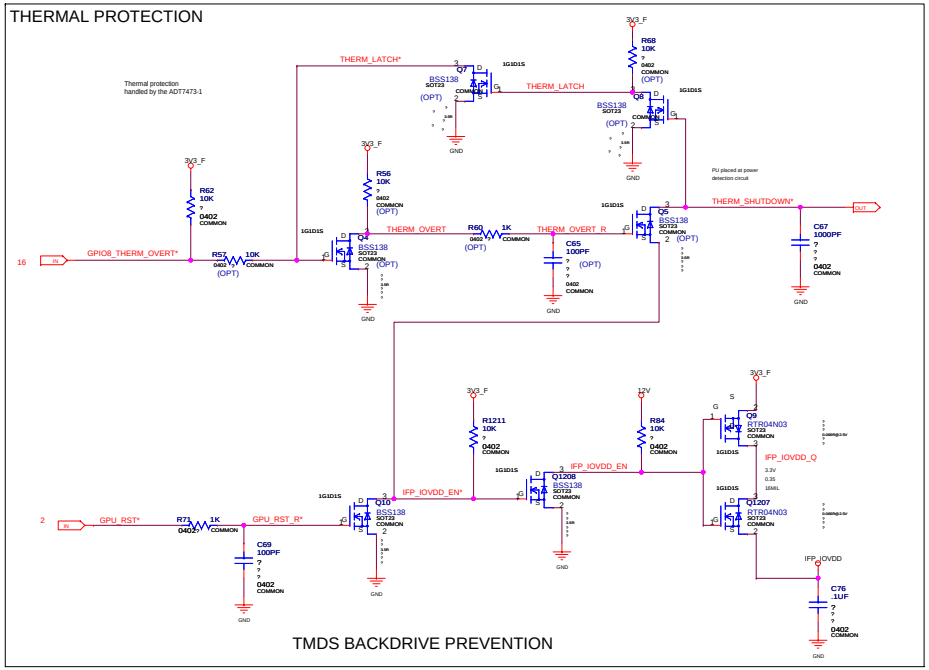
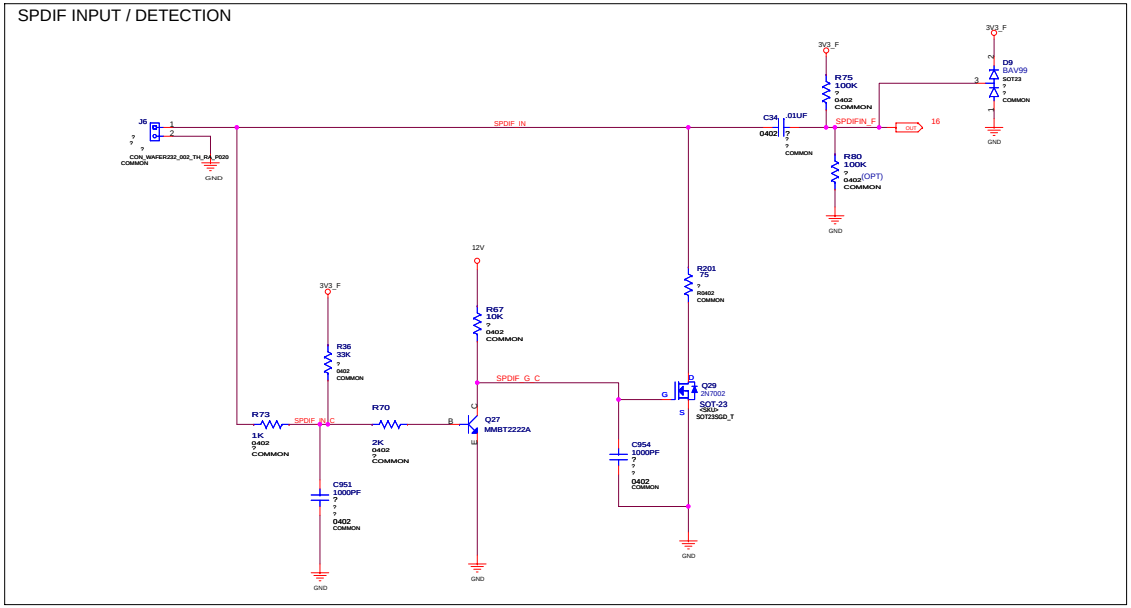
Page17: Thermal Control/Protection and SPDIF Input

NET	IMPEDANCE	NV_CRITICAL_NET	MIN_LINE_WIDTH
SPDIFIN_F	55OHM		1

THERMAL PROTECTION

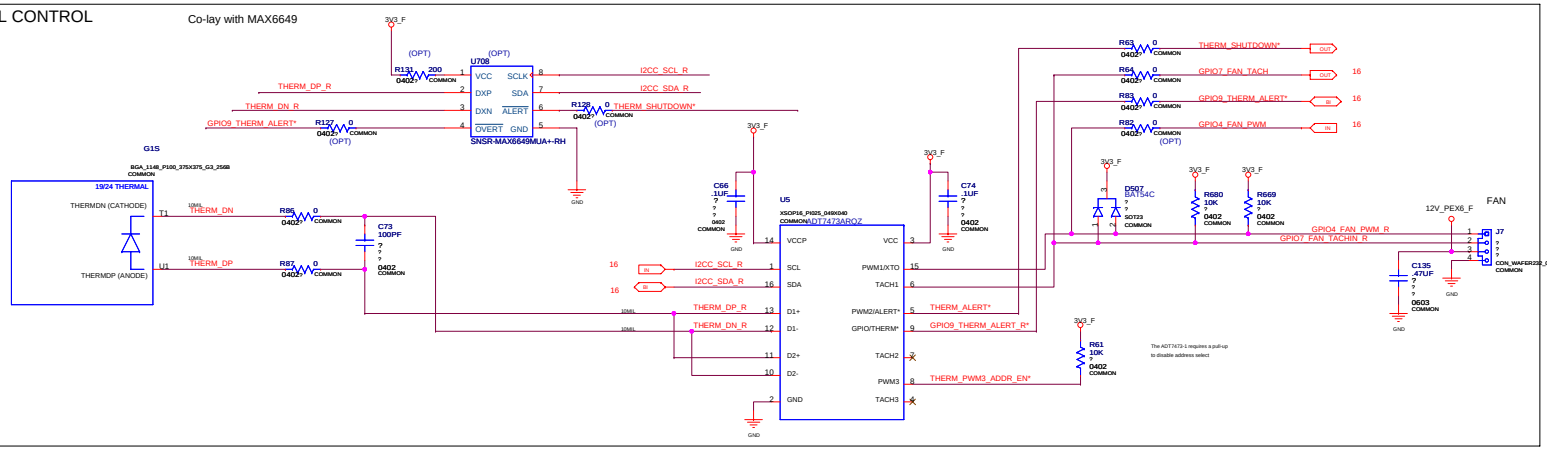


SPDIF INPUT / DETECTION



THERMAL CONTROL

Co-lay with MAX6649



The FAN connector needs to move as follows for mechanical / ID support:

* move -43mils in Y
* move +43mils in X

Stuffing possibilities for thermal control and protection:

2) ADT7473 is COMMON
GPIO4 is not used.
GPIO7 is the tach input from the fan
GPIO9 is the thermal alert for GPU slowdown.
With a newer version of the ADT chip, PWM2 can optionally be used for shutdown

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Thermal Control/Protection and SPDIF Input

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Thermal Control/Protection and SPDIF Input

Size	Document Number	Rev
Custom	MS-V117	<FevCode>

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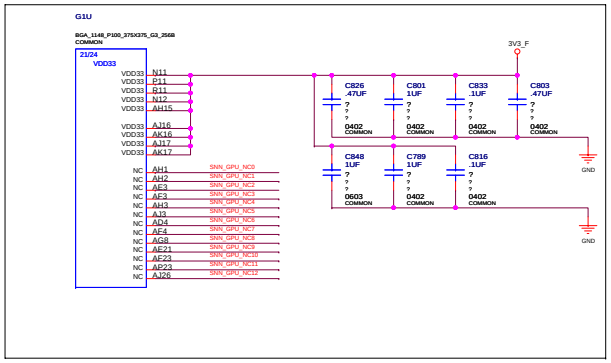
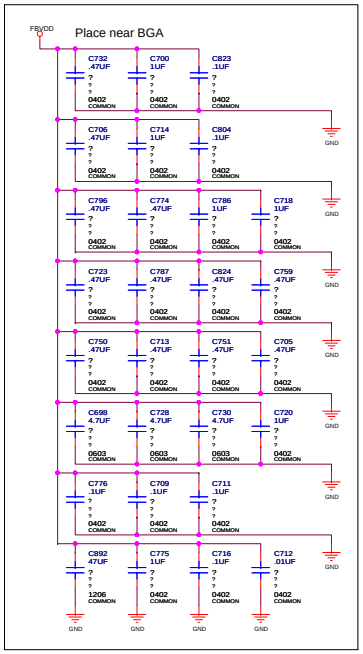
Page18: Power/GND and Decoupling

VDD33

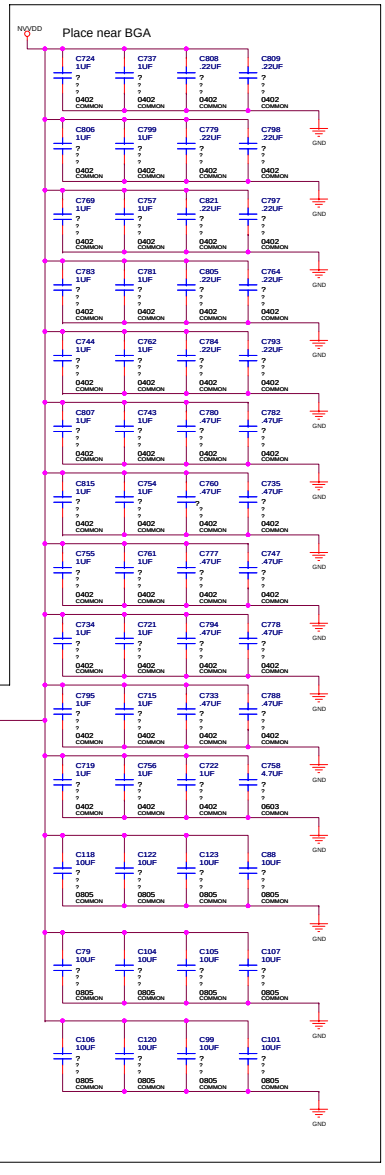


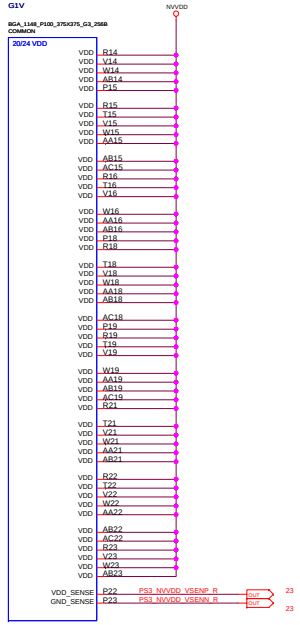
FBVTT

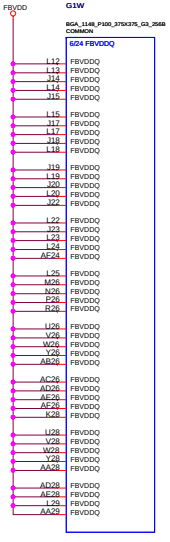
FBVDDQ

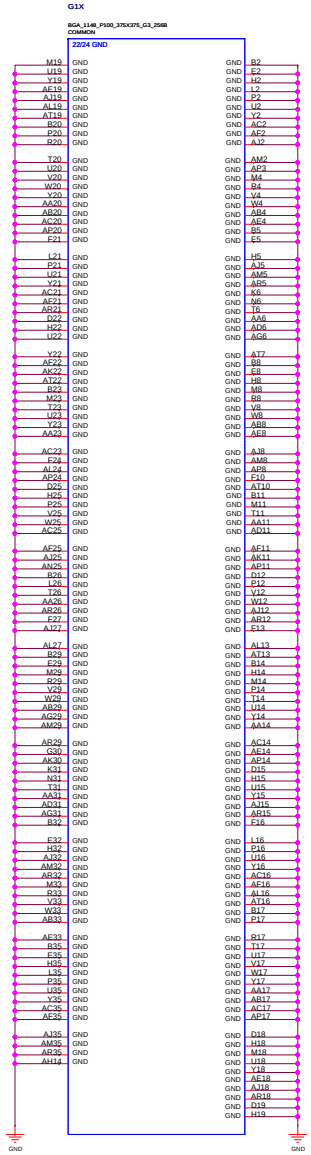


NVVDD









NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
PS3_NVVDD_VSENP_R 23	1	60OHM	NVVDD_SENSE
PS3_NVVDD_VSENN_R 23	1	60OHM	NVVDD_SENSE

ASSEMBLY: P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: Power/GND and Decoupling

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Power/GND and Decoupling

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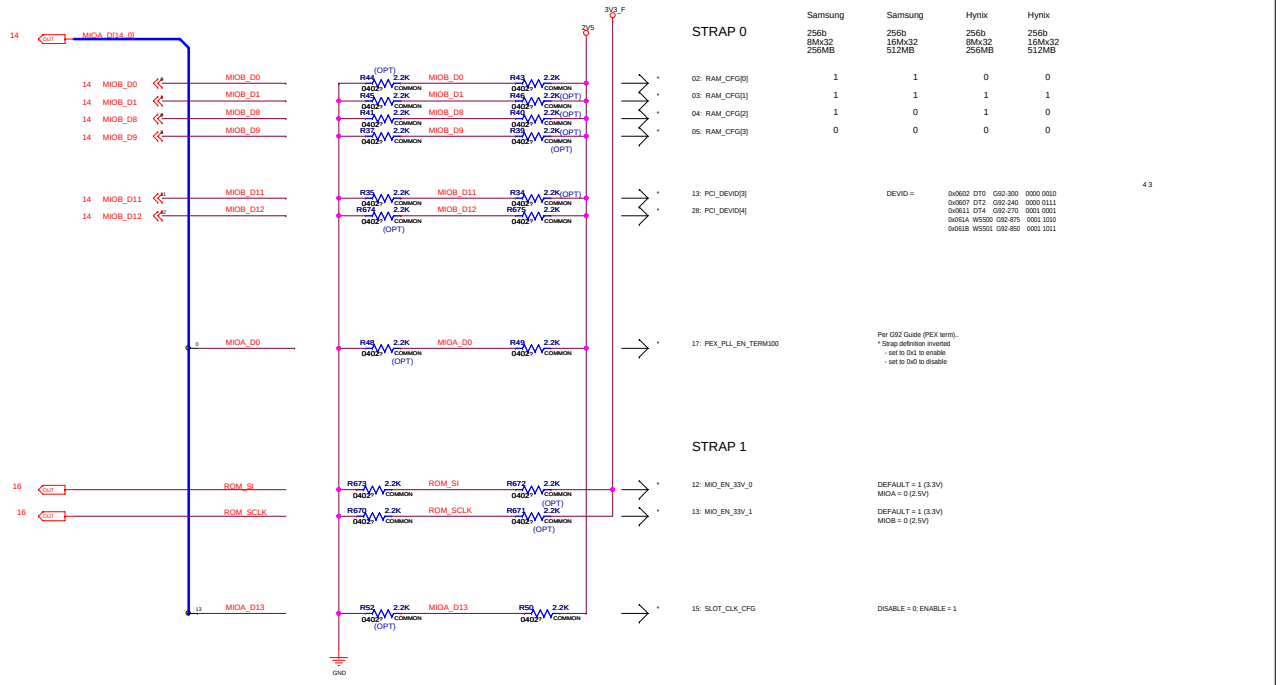
Page19: Configuration Straps and Mechanical

STRAPS



STRAP 0

	Samsung 256b 8Mx32 256MB	Samsung 256b 16Mx32 512MB	Hynix 256b 8Mx32 256MB	Hynix 256b 16Mx32 512MB
02: RAM_CFG[0]	1	1	0	0
03: RAM_CFG[1]	1	1	1	1
04: RAM_CFG[2]	1	0	1	0
05: RAM_CFG[3]	0	0	0	0

13: PCI_DEVID[3], 28: PCI_DEVID[4] — DEVID =

0x0602 DT0	G92-300	0000 0010	
0x0607 DT2	G92-240	0000 0111	
0x0611 DT4	G92-270	0001 0001	
0x061A WS500	G92-875	0001 1010	
0x061B WS501	G92-850	0001 1011	

17: PEX_PLL_EN_TERM100 — Per G92 Guide (PEX term)..
* Strap definition inverted
- set to 0x1 to enable
- set to 0x0 to disable

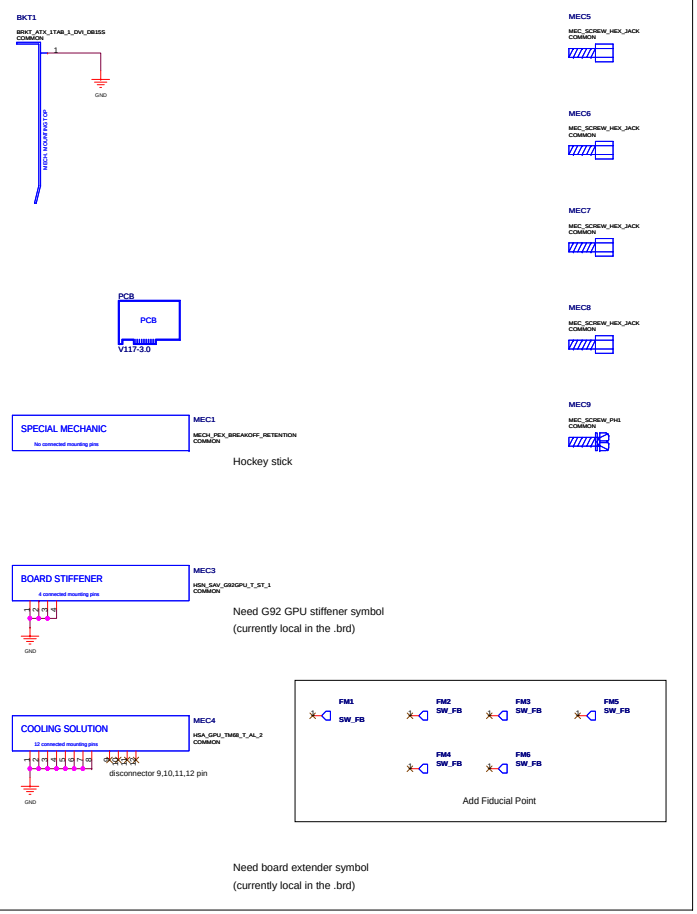
STRAP 1

12: MIO_EN_33V_0 — DEFAULT = 1 (3.3V) MIOA = 0 (2.5V)

13: MIO_EN_33V_1 — DEFAULT = 1 (3.3V) MIOB = 0 (2.5V)

15: SLOT_CLK_CFG — DISABLE = 0; ENABLE = 1

MECHANICAL



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Configuration Straps and Mechanical

Micro-Star International Co., LTD.

Straps and Mechanical

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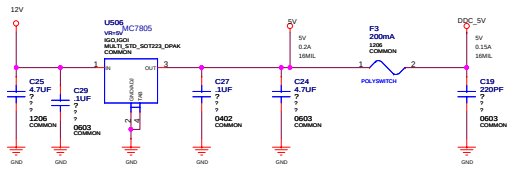
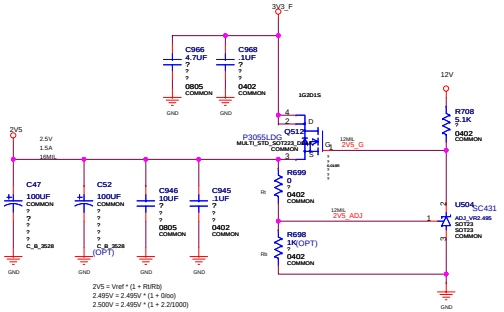
Date: Friday, December 14, 2007 Sheet 19 of 27

Page20: Power Supply: 5V, 2V5,

5V and DDC5V Supply



2V5 Supply



DEL 5V STEREO Supply

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 5V, STEREO_5V, 2V5, DP_PWR

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5V, 2V5,

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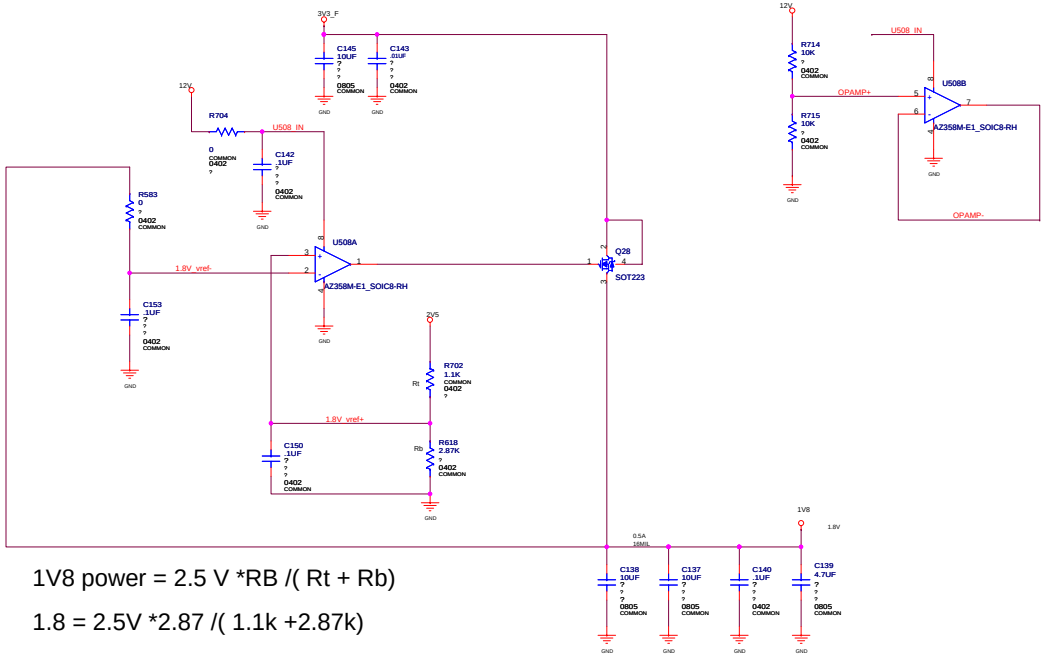
Page21: Power Supply: 1V8



1V8 power = 2.5 V *RB /(Rt + Rb)

1.8 = 2.5V *2.87 /(1.1k +2.87k)

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: 1V2, 1V8

Micro-Star International Co., LTD.

1V8

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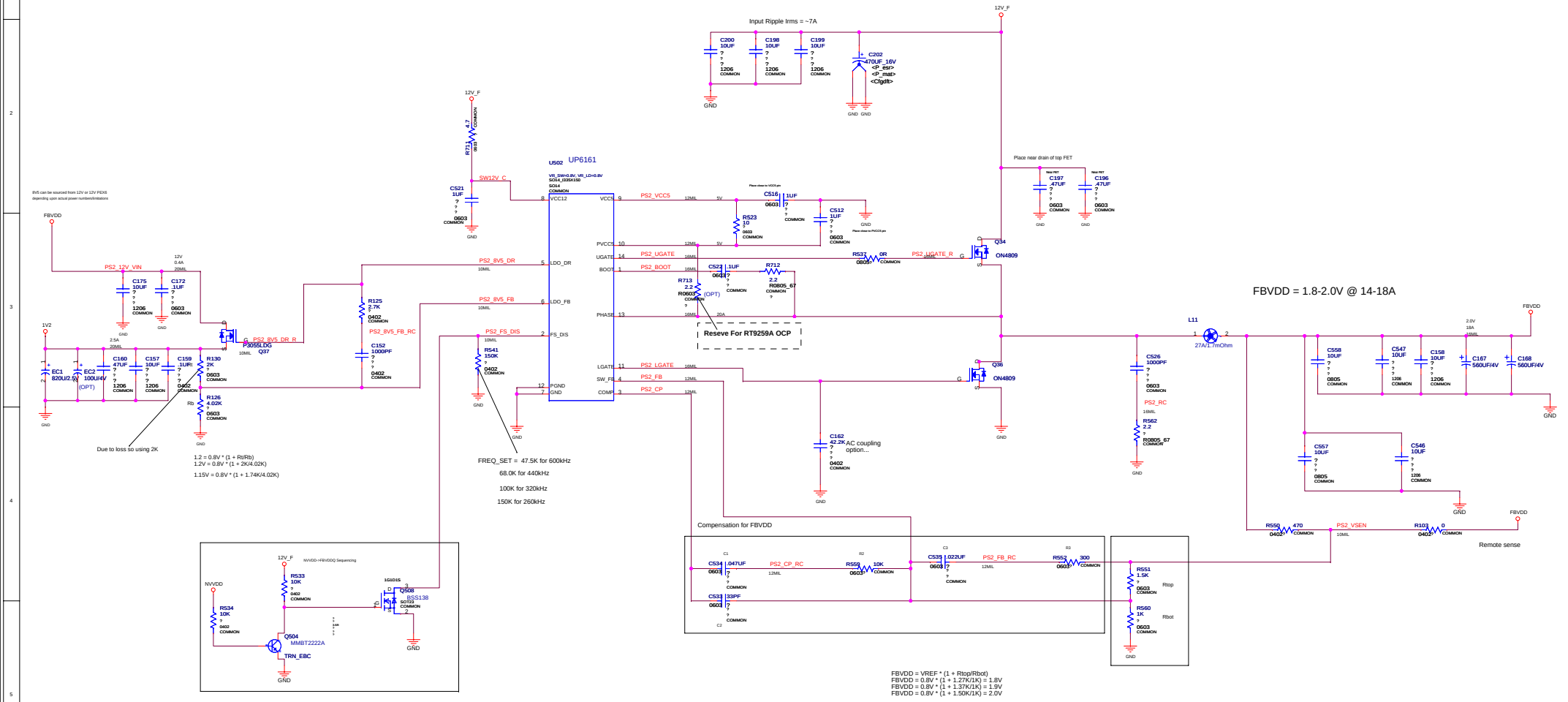
Date: Friday, December 14, 2007 Sheet 21 of 27

Page22: Combined FBVDD/VDDQ, 1V2



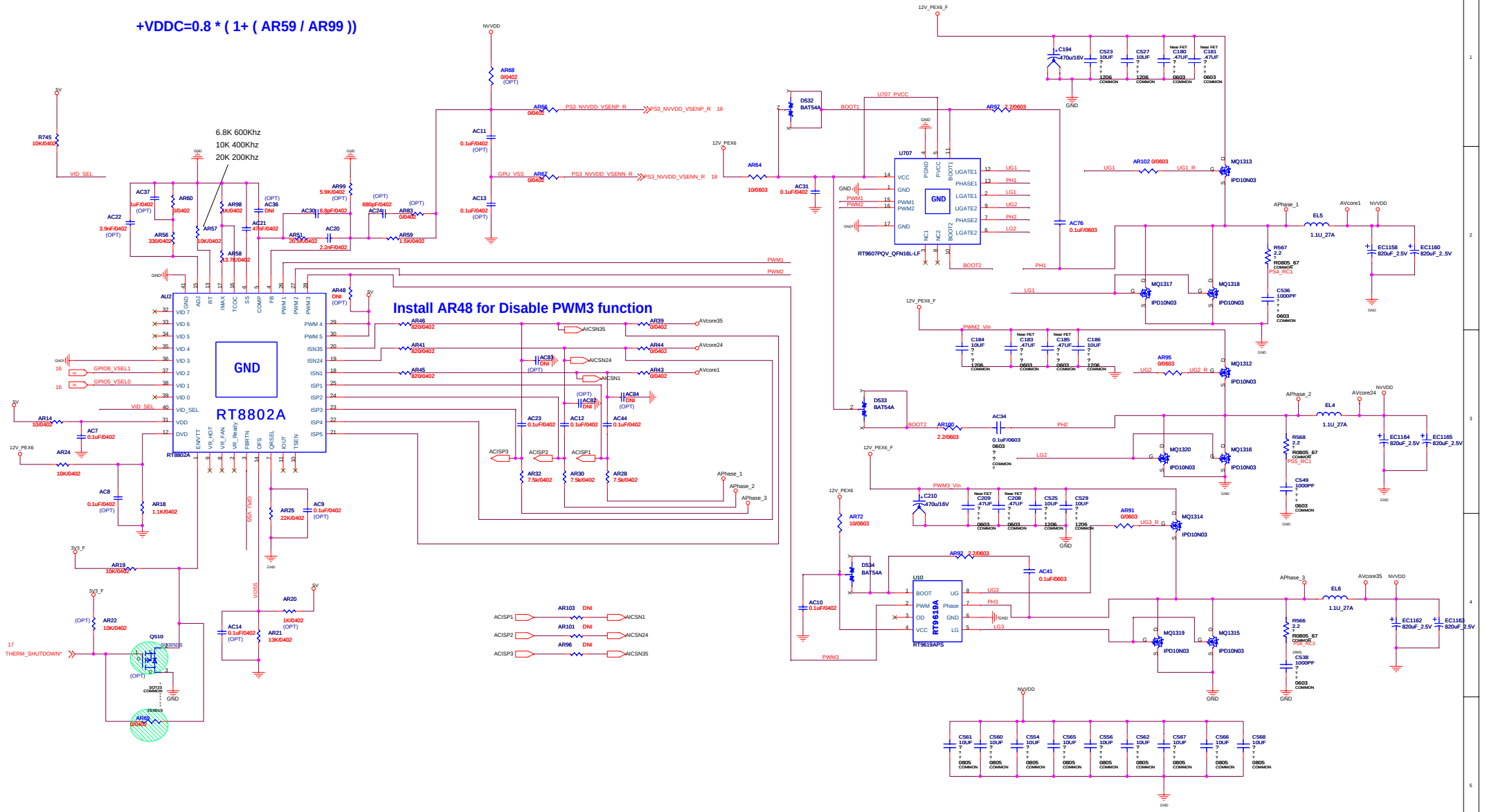
ASSEMBLY: P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: Power Supply: FBVDDIQ, 8V5

Micro-Star International Co., LTD.	
FBVDD/VDDQ, 1V2	
Size: Custom	Document Number: MS-V117
Rev: <FevCode>	
Date: Tuesday, December 18, 2007	Sheet 22 of 27

Page23: Power Supply: NVVDD Regulator

+VDDC=0.8 * (1+ (AR59 / AR99))



ASSEMBLY: P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: Power Supply: NVVDD Regulator

Micro-Star International Co., LTD.

NVVDD

Size: Custom | Document Number: V117 | Rev: <FevCode>

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Page24: Power Supply: NVVDD Phase 2, 3

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 1 & 2

MSI

Micro-Star International Co., LTD.

<Title>

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Custom	<Doc>	<FevCode>

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Page25: Power Supply: NVVDD Phase 1

ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVVDD Phase 3

Micro-Star International Co., LTD.

<Title>

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Custom	<Doc>	<FevCode>

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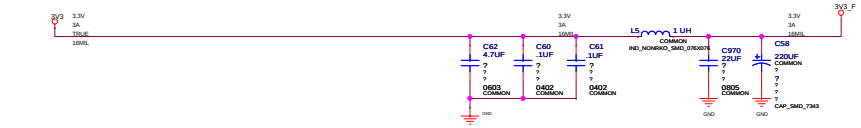
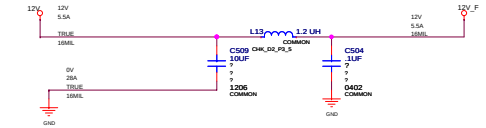
Page26: Power Supply: Filter/Detection of 3V3,12V,12V_PEX

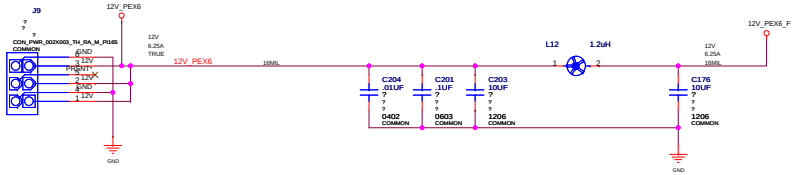
POWER FILTER 3.3V



POWER FILTER 12V



INPUT FROM EXTERNAL
75W PEX EXTENSION POWER



ASSEMBLY	P393 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: Filter/Detection of 3V3, 12V, 12V_PEX6

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3V3,12V,12V_PEX

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Page27: Power Supply: Hybrid Power

Weak pull-ups needed for I2CS:

* if SMBus is isolated from the GPU
* if MB does not support SMBus
* if MB does not support 3V3AUX

ASSEMBLY	P393 : BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: Hybrid Power

Micro-Star International Co., LTD.
<Title>
Size: Custom | Document Number: <Doc> | Rev: <FevCode>
Date: Friday, December 14, 2007 | Sheet 27 of 27