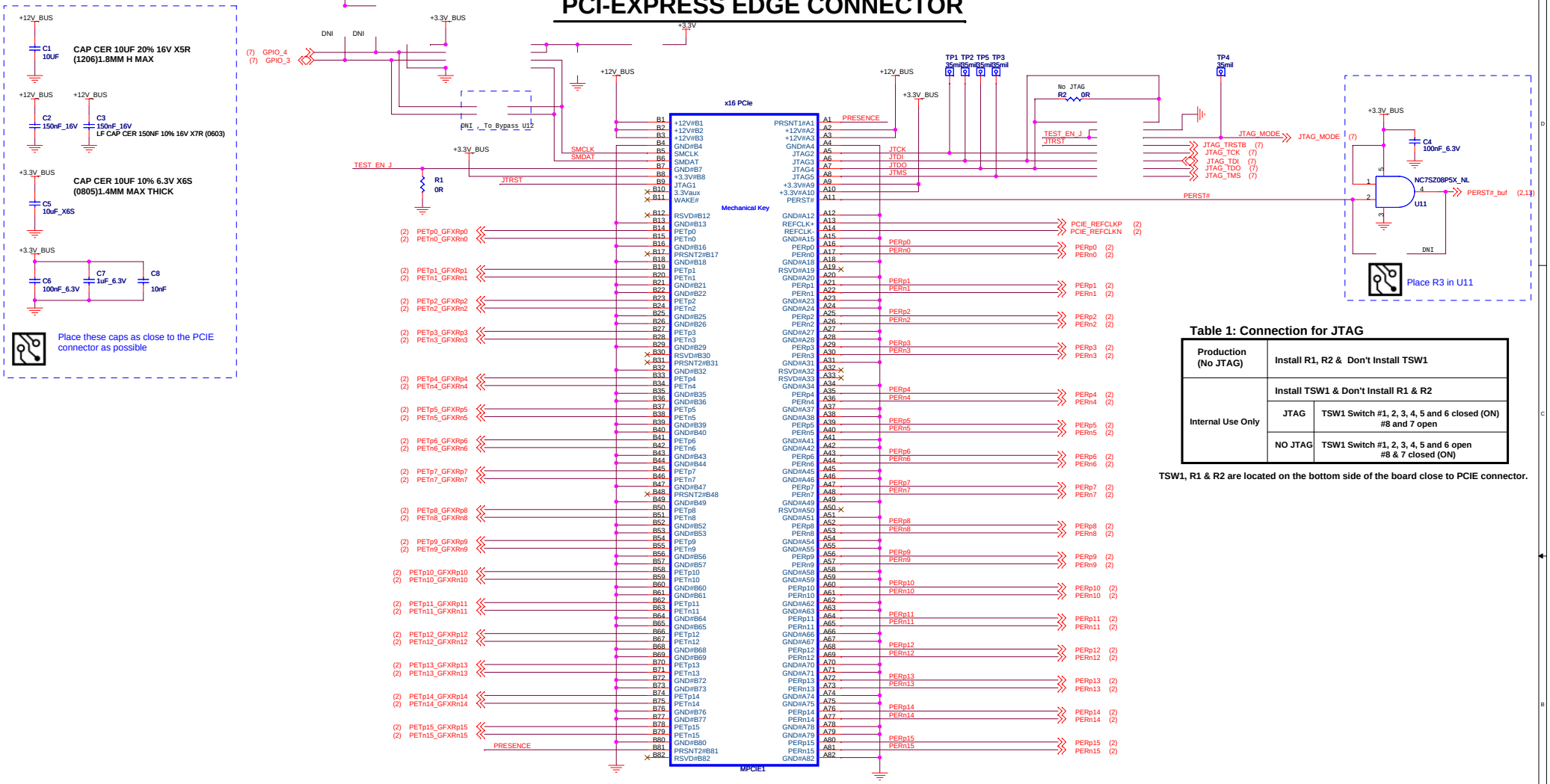
# PCI-EXPRESS EDGE CONNECTOR




## Table 1: Connection for JTAG

| | | |
|---|---|---|
| Production (No JTAG) | Install R1, R2 & Don't Install TSW1 | |
| Internal Use Only | Install TSW1 & Don't Install R1 & R2 | |
| | JTAG | TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open |
| | NO JTAG | TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON) |

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

| SYMBOL LEGEND | |
|---|---|
| DNI | DO NOT INSTALL |
| # | ACTIVE LOW |
| | DIGITAL GROUND |
| | ANALOG GROUND |
| BUO | BRING UP ONLY |



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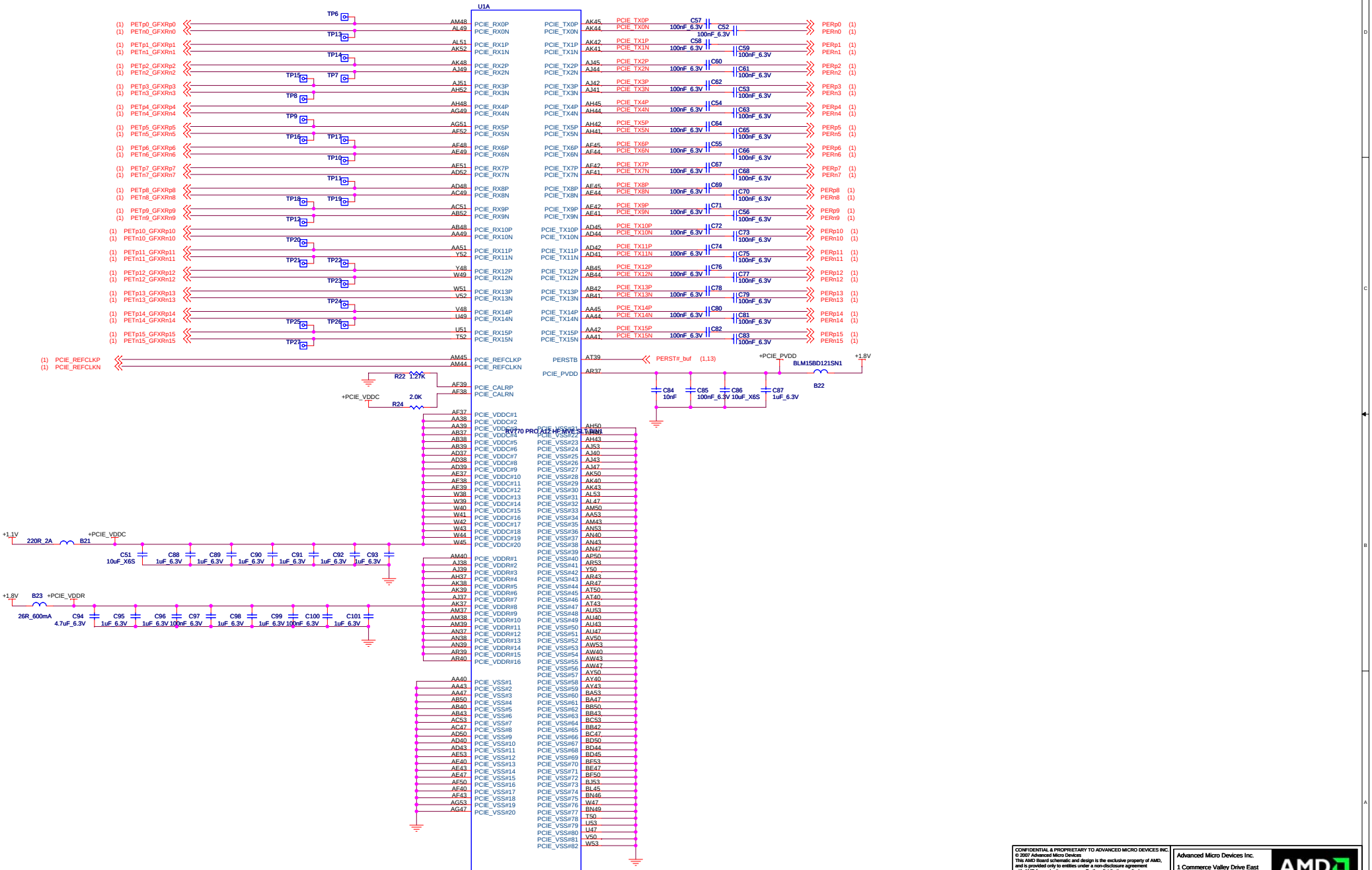
NOTE: some of the PCIE testpoints will
be available trought via on traces.



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| | |
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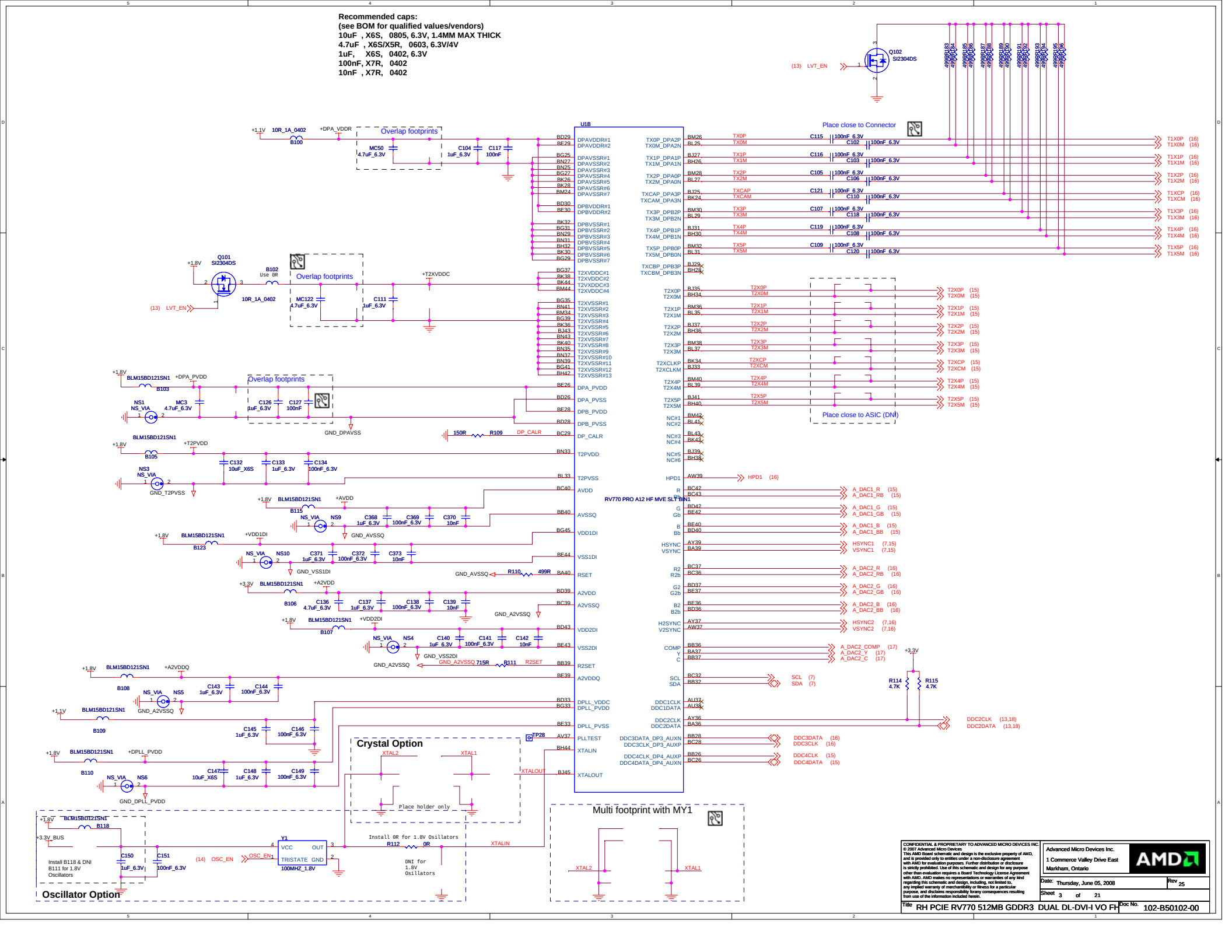
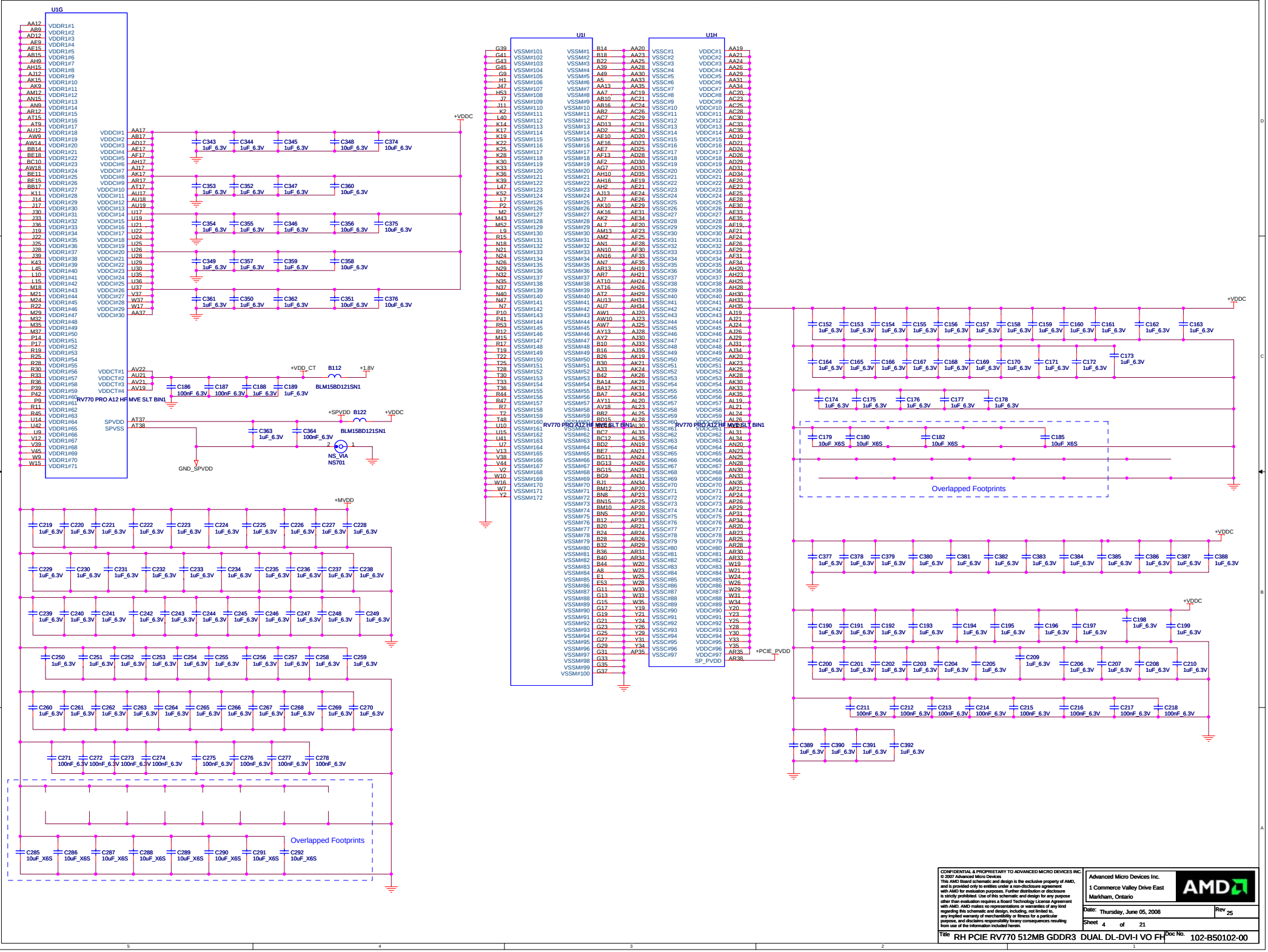
**Recommended caps:**
**(see BOM for qualified values/vendors)**
**10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK**
**4.7uF , X6S/X5R, 0603, 6.3V/4V**
**1uF, X6S, 0402, 6.3V**
**100nF, X7R, 0402**
**10nF , X7R, 0402**



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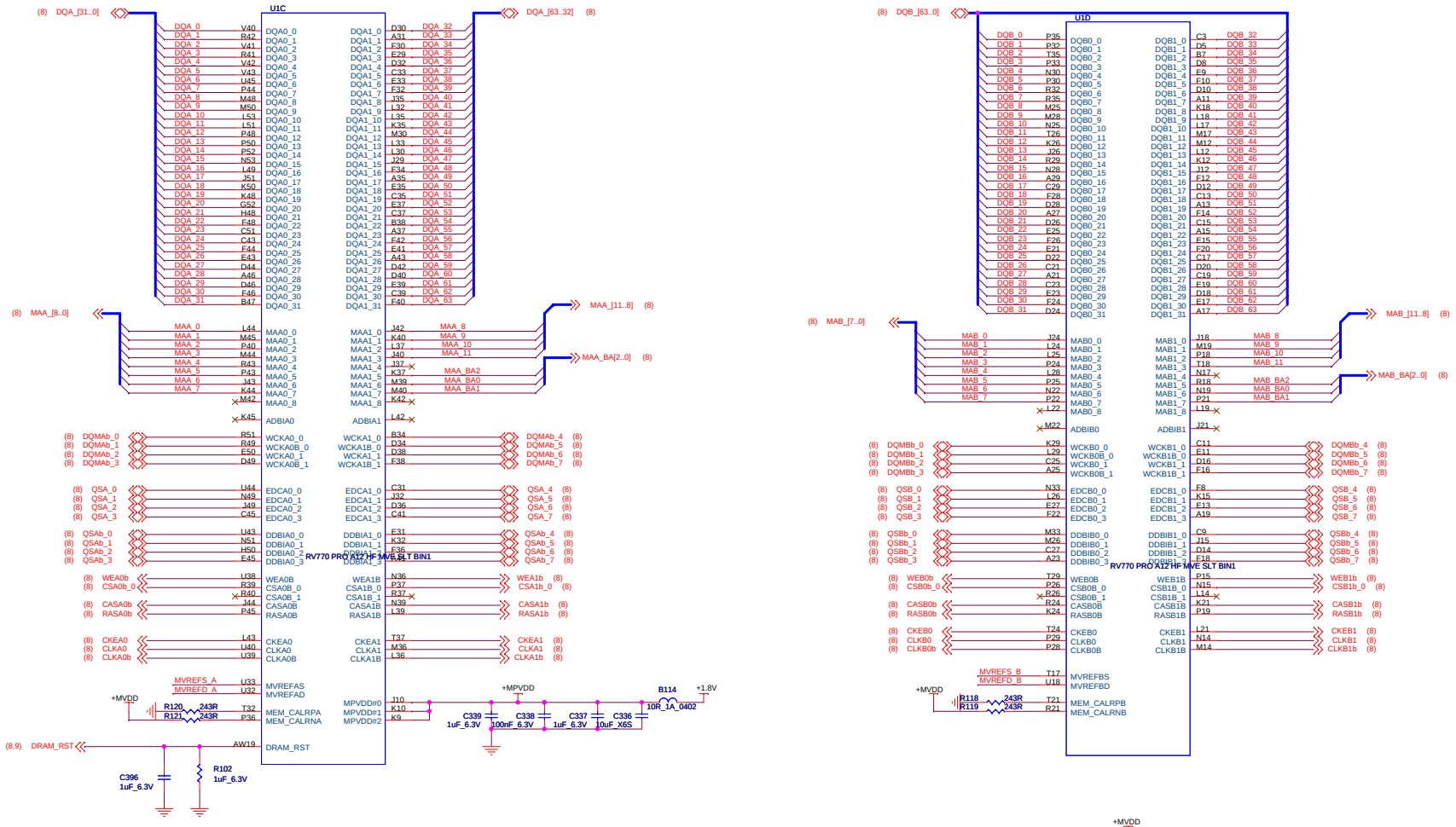


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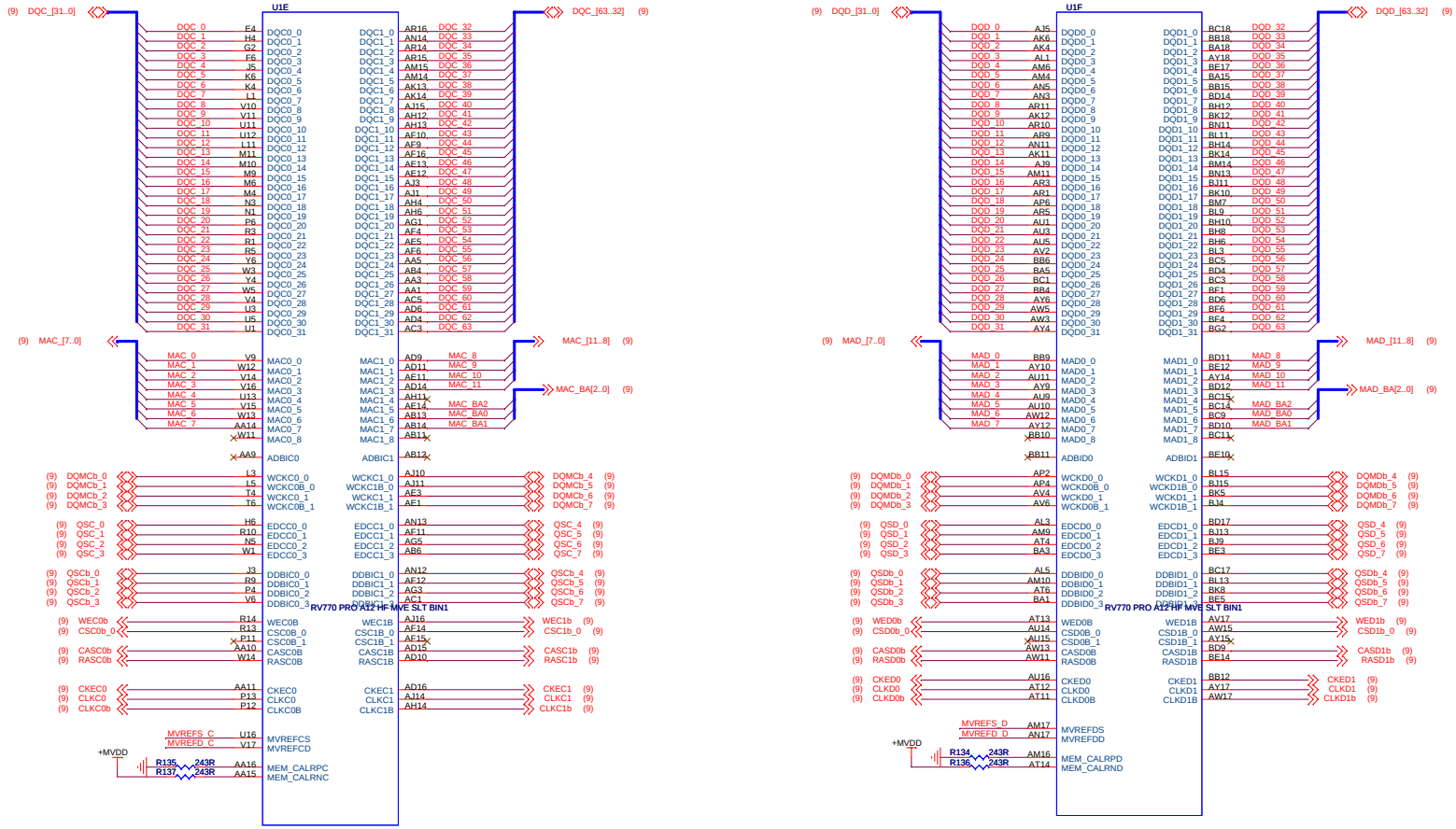
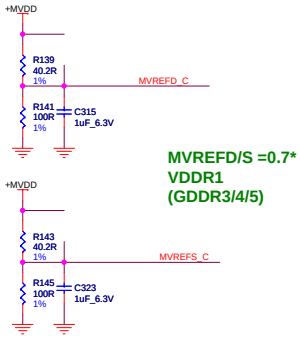
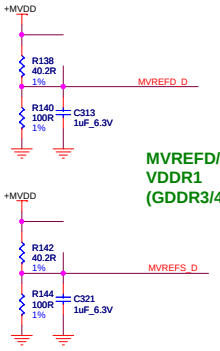









MVREFD/S =0.7*
VDDR1
(GDDR3/4/5)




MVREFD/S =0.7*
VDDR1
(GDDR3/4/5)



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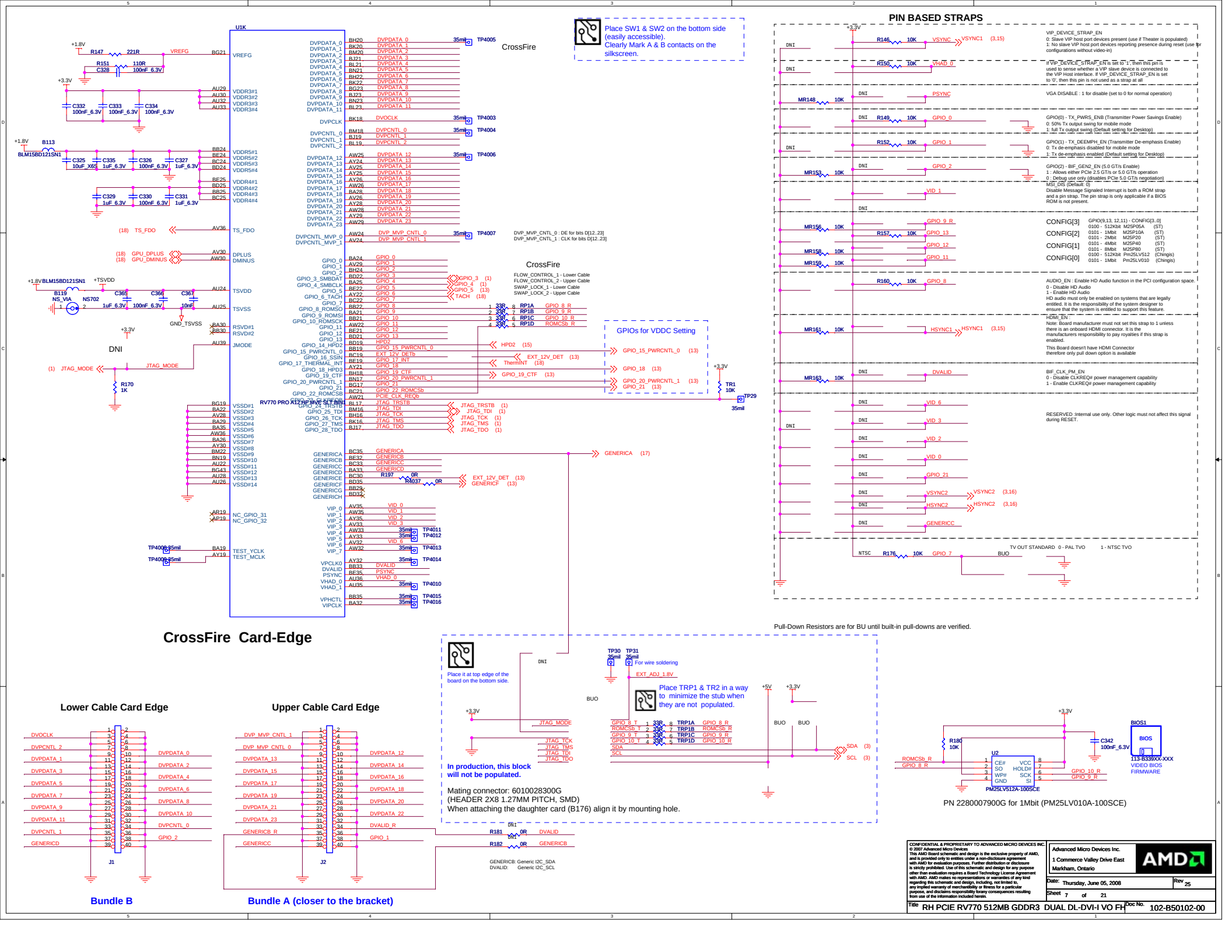
PIN BASED STRAPS
CrossFire Card-Edge
Lower Cable Card Edge
Upper Cable Card Edge
Bundle B
Bundle A (closer to the bracket)
Pull-Down Resistors are for BU until built-in pull-downs are verified.
In production, this block will not be populated.
Mating connector: 6010028300G
(HEADER 2X8 1.27MM PITCH, SMD)
When attaching the daughter card (B176) align it by mounting hole.
PN 2280007900G for 1Mbit (PM25LV010A-100SCE)
CrossFire
GPIOs for VDDC Setting
Place SW1 & SW2 on the bottom side (easily accessible).
Clearly Mark A & B contacts on the silkscreen.
Place it at top edge of the board on the bottom side.
Place TRP1 & TR2 in a way to minimize the stub when they are not populated.
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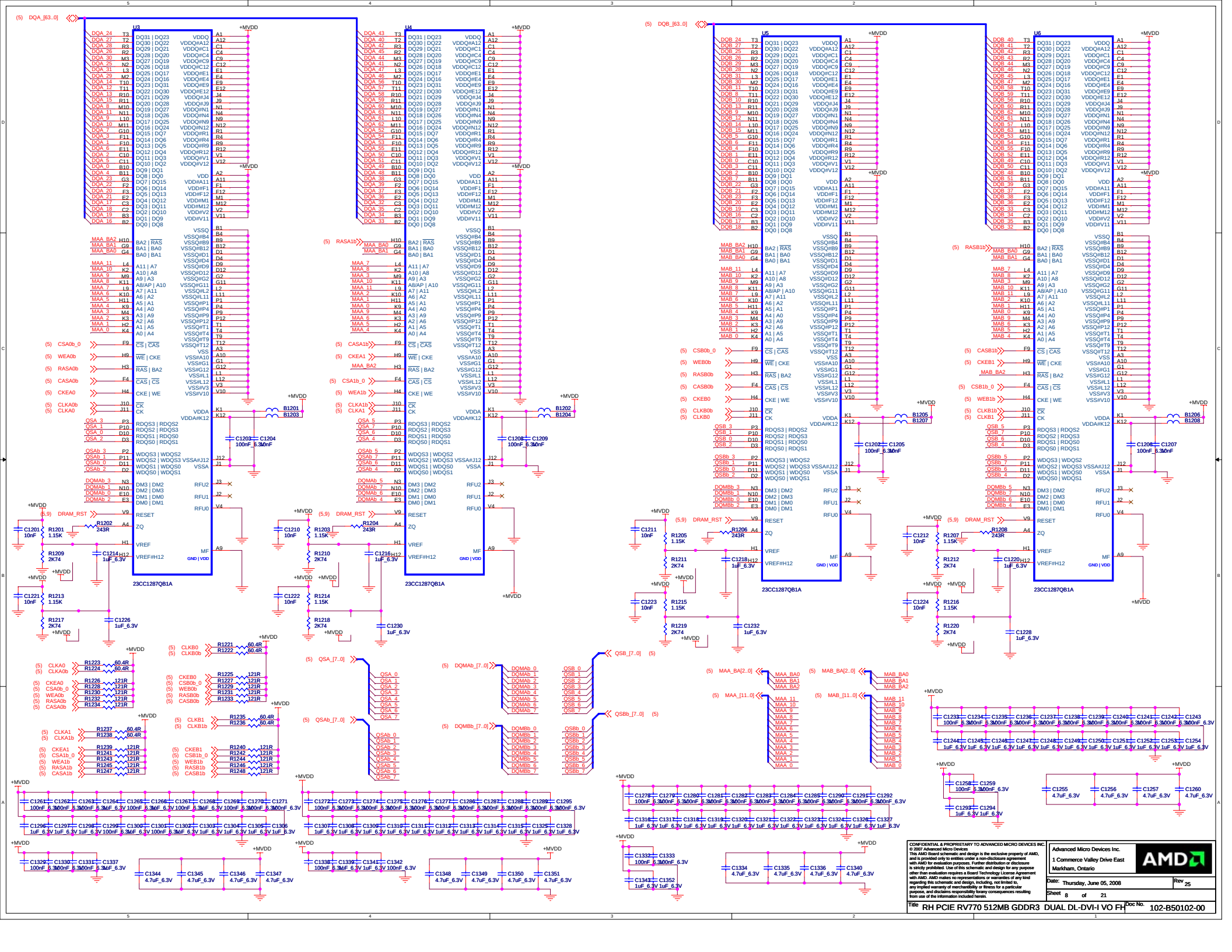


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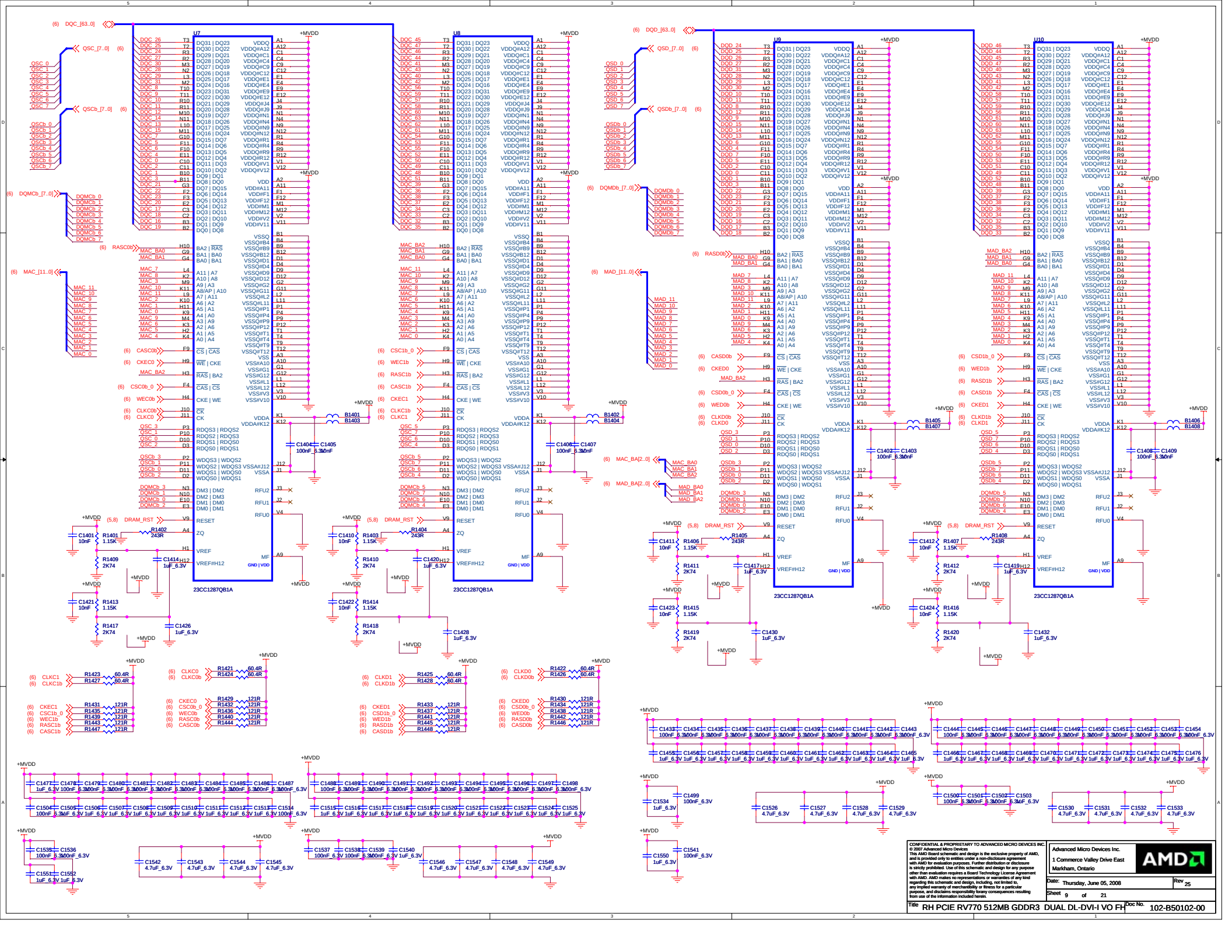




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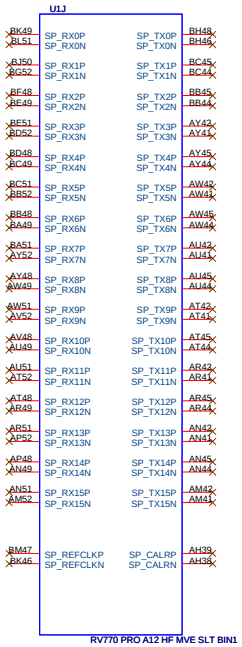




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## Input Bulk CAPs

+VDDC_Source / +VDDC_ExtSource

MC623 470UF_16V TH 8mm Dia — TH 10x12.5mm — Overlap
MC626 470UF_16V TH 8mm Dia — TH 10mm Dia — Overlap
MC630 470UF_16V TH 8mm Dia — TH 10x12.5mm — Overlap
MC637 470UF_16V TH 8mm Dia — TH 10mm Dia — Overlap
MC636 470UF_16V TH 8mm Dia — TH 10x12.5mm
MC657 470UF_16V TH 8mm Dia — TH 10mm Dia — Overlap

## Choosing Different Gate Drive

| Gate Drive | Populate | Do Not Populate |
|---|---|---|
| 5V Gate Drive | R631, R632 | R630, R670, C660, R661, Q661 |
| 8V Gate Drive | R630, C660, R661, Q661 | R631, R632, R670 |
| 12V Gate Drive | R630, C660, R670 | R631, R632, R661, Q661 |

Reserved for ARIES-II — +12V_EXT — VCC2

Overlap the footprints for MR655 and C655

PGND Option — Current Compensation — Css if current comp. not used — C655 100nF_25V — SS_ICOMP

VDDC_REFIN — VDDC_REFIN (13)

VDDC_FB — VDDC_FB (13) — FB_S

+VDDC — NS600 NS_VIA — VDDC_FB_TRACE

Type III compensation: R3 R653 10K — COMP_GND — Rj1 — C3 C653 4.7NF_50V — Rj2 R656 0R — R1 R652 40.2K — C2 C651 150pF — C1 C652 4.7NF_50V — COMP_FB

Droop Option — Rdroop

12V Bus power for 12V Gate Drive — +12V_BUS — 402

Pass Transistor Circuit for 8V Gate Drive
This circuit is only for 8V gate drive application
Assume VCC consumes 200mA total including 5VCC providing buffered output sourcing a minimum 20mA requirement
P(Q_8VCC)max = (12V-8V)*0.2A = 800mW
+12V_BUS — R661 10K — SI2304DS Q661 — VCCDRV

OPTIONAL — UGATE2 — 0R R611 — C612 1uF — PHASE2 — LGATE2 — 0R R613

U601 uPI6201BQ: UGATE2, BOOT2, REFOUT/POK, REFINEN, SSI/COMP, FB, PHASE2, LGATE2, VCCDRV/DROOP, VCC, LGATE1, PHASE1, PGND, PGND26, PGND27, PGND28, PGND29, UGATE1, BOOT1, 5VCC, AGND, BUSEN, CSP1, COMP/DROOP, RT, IOUT/IMAX/DROOP, CSP2, CSN2, CSN1

R_RT 402 R655 30.1K — Iout — Iout (13) — C638 1nF 402 10V X5R — Rdroop — CSP2 — CSN2 — CSN1

VDDC_FB_TRACE — DNI

C694 1UF_16V X7R 603 — 1206 X5R 16V — LGATE1 — 0R R603 — PHASE1 — C602 1uF — UGATE1 — 0R R601 — OPTIONAL

C660 1uF_6.3V 402 6.3V Y5V — 402 10V X5R

PH2_ENb — PH2_ENb (13)
- When +12V_EXT=ON, PH2_ENb=Low, Phase 2 Enabled
- When +12V_EXT=OFF, PH2_ENb=Hi , Phase 2 Disabled

Populate - For 5V Gate Drive application
Remove - For 8V or 12V Gate Drive application
5VCC

5VCC (13,14)
5VCC applied externally or generated internally from the IC, must be in regulation before IC start soft-start sequence.

1. For 5V Gate Drive application:
External filtered +5V_EXT is applied to this pin.
2. For 8V or 12V Gate Drive application:
+5VCC is generated internally and this is an output with 20mA minimum current capability

(13) VDDC_EN — R685 0R — share pad — VCCDRV — SS_ICOMP — VDDC_REFIN
VDDC PWM Whole Chip Enable

+12V_BUS — L621 IND_0.47uH_7A — DUAL FOOTPRINT — C690 100uF_16V TH 6x7mm
C632 4.7uF_16V 805 — C633 4.7uF_16V 805 — C621 10UF_16V 1206 — C622 10UF_16V 1206 — C600 150nF_16V 603 — +VDDC_Source
C635 4.7uF_16V 805 — C634 4.7uF_16V 805 — C640 10UF_16V 1206 — C663 10UF_16V 1206
Mirrored on PCB

+12V_EXT — C695 100uF_16V TH 6x7mm — L622 IND_0.47uH_7A — DUAL FOOTPRINT — +VDDC_ExtSource
C639 150nF_16V 603
C625 10UF_16V 1206 — C624 10UF_16V 1206 — C627 4.7uF_16V 805 — C628 4.7uF_16V 805
C665 10UF_16V 1206 — C664 10UF_16V 1206 — C629 4.7uF_16V 805 — C631 4.7uF_16V 805
Mirrored on PCB

Q601 BSC120N03LSG — Q602 BSC120N03LSG — UGATE1 — PHASE1
L601 PCMB103T-R47MS — L602 PCMB103T-R47MS — Overlap — +VDDC
L611 PCMB103T-R47MS — L612 PCMB103T-R47MS
Q612 BSC120N03LSG — Q611 BSC120N03LSG — UGATE2 — PHASE2
Q603 BSC042N03LSG — Q604 BSC042N03LSG — LGATE1
Q613 BSC042N03LSG — Q614 BSC042N03LSG — LGATE2
R604 4.32K 1/10W 0603 — C604 100nF X7R — R605 1.47K — C605 100nF_6.3V
R614 4.32K 1/10W 0603 — C614 100nF X7R — C615 100nF_6.3V — R615 1.47K
FB_S — CSP1 — CSN1 — CSN2 — CSP2
Place across Q613, Q614 — 805 — 603
RC snubber values shown are for reference only, tuning is required

+VDDC — 2.5V, 9mR SP/POSCAP, SMT 7343 2MM H — Mirrored on PCB

C641 820uF_2.5V — C642 820uF_2.5V — C643 820uF_2.5V — C644 820uF_2.5V — 8 x 8 mm, TH
Place seperately

R696 300R 805

C645 10uf Y5V 12066.3V — C646 10uf Y5V 12066.3V — C647 10uf Y5V 12066.3V — C648 10uf Y5V 12066.3V

C661 15nF 402 603 — C650 15nF 402 603



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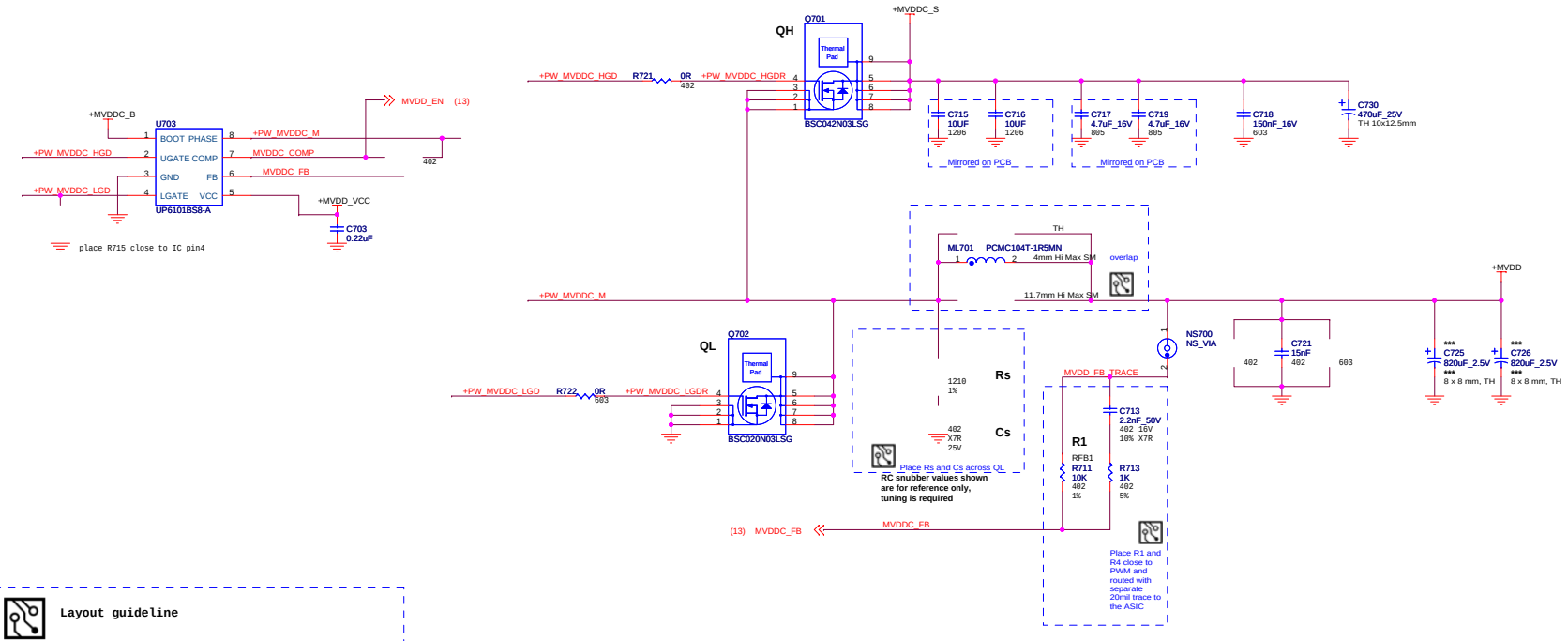
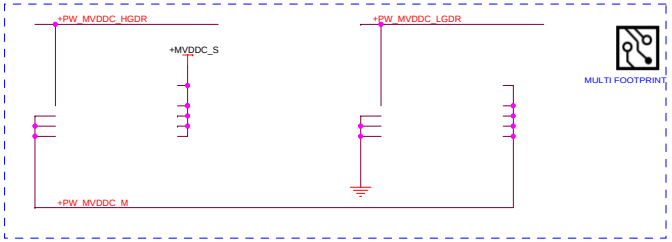
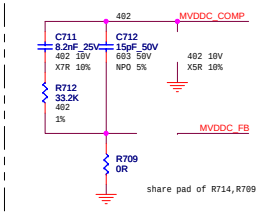



## Layout guideline

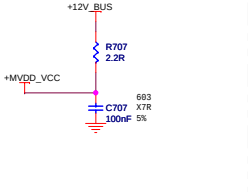
1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



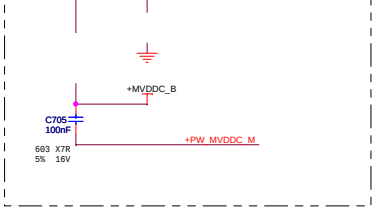

### COMPENSATION CIRCUIT




### FILTERED SMPS VCC




### BOOT CIRCUIT



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## 12V_EXT Connector

VDDC_EN is open collector and it is deactivated (pulled down to ground) when: EN_INTb =1 OR EN_Tb =1 OR (EN_EXTb =1 AND SENSE_GND_PIN=0)

Overlap MC1603 and C1603

## Phase Control Support

## 4-bit VID for VDDC Setting

(bit 5 is fixed to zero VID4=0)

Place all parts close to the regulator that uses the voltage reference. R1673 & R1674 can be placed close to GPU for easy access to +3.3V.

R1687 & R1688 must be selected to limit MAX ref voltage to MAX VDDC.

See BOM for qualified values.

External Reference is used when REFIN is driven by voltage ranged from 0.4V to 3.3V

Internal Reference is used when REFIN is pull-up to > 4.5V

R636, R639 share pad

**Table 4 VDDC Vref Mode Selection**

| Vref Mode | R636 | R639/C659 | Vref (V) |
|---|---|---|---|
| Internal | Populate | NC | 0.6 |
| External | NC | Populate | set by VID IC (U1220) |

## Power up Sequencing

## AUX plug Enforcment option (BUO not for production)

## 12V AUX Power up Fault Support

## 12V/3.3V Bonding

## Bypass Switch (not for production)

Red LED On, shows 12V AUX fault

## AUX Hot Plug/ Unplug Fault supprt

## Critical Temperature Support

Red LED On, shows critical temperature fault

Bypass Switch (not for production)

## MVDD Input Option Circuit

## VDDC Transient Test Circuit

For testing only, not intended for production

## 10x Buffered VDDC Output Current Monitoring

Temp Comp

For testing only, not intended for production

## 16-bit ADC for voltage & current read back

Install only R1270 or MR1270

Connect to +VDDC & +MVDD at the ASIC

For testing only, not intended for production

See BOM for qualified config.

**Table 5 PTC Themal Protection**

| PTC | THEM_PRT |
|---|---|
| >= Themal shutdown temp (R>=4.7K) | Low |
| < Themal shutdown temp (R < 4.7K) | Hi |

- Place PTC1, PTC2 close to VDDC MOSFET
- Place PTC3, PTC4 close to MVDD

**Table 2: VDDC Enable/Shutdown**

| | |
|---|---|
| EN_INTb asserted (0) when: | +12V_BUS & +3.3V_BUS are passed the threshold limit set by the voltage dividers |
| EN_EXTb asserted (0) when: | External cable plugged in, and +12V_EXT is passed the threshold limit set by the voltage divider |
| EN_Tb | This will be cleared at power-up, and will be set when Critical Temperature is reached |
| EXT_12V_DET (Active High) | On rising edge of LDO_EN, condition of PH2_EN is latched to determine the status of EXT cable. |

## VDDC Low Side Divider

R650 must be pouplated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.

- VDDC Hi-Side Divider R651 is Fixed to 5.11K
- Vo = Vref * (1 + R651 / R650 )
- Vref = 0.6V

## PTC Comparator Solution

Overlap Pad of R1653/MR1653

Overlap Pad of R1666/MR1666

Overlap Pad of R1686/MR1686

Place caps very close to power pin

## 12V_BUS & 12V_EXT Input Switch Circuit

FDS6675, -10A, -30V, SO-8 (2020002200G)
Alt. FDS7779Z, -16A, -30V, SO-8 (2020013800G)

Put copper area under Q1230/1231 for heat dissipation.

**Table 3**

| 0: OFF / 1: ON | | | 0: OFF / 1: ON | | | | Status |
|---|---|---|---|---|---|---|---|
| 12V_BUS | 12V_EXT | EXT_12V_DET | Q1 | Q2 | | | |
| | | | | | | | No Power, No boot |
| 0 | 0 | NA | NA | NA | | | |
| 1 | 0 | 0 | 1 | 1 | | | Board is Powered by 12V_BUS, action taken by software |
| 0 | 1 | NA | 0 | 0 | | | No 12V_BUS, No boot |
| 1 | 1 | 1 | 0 | 0 | | | Boot up in normal condition |



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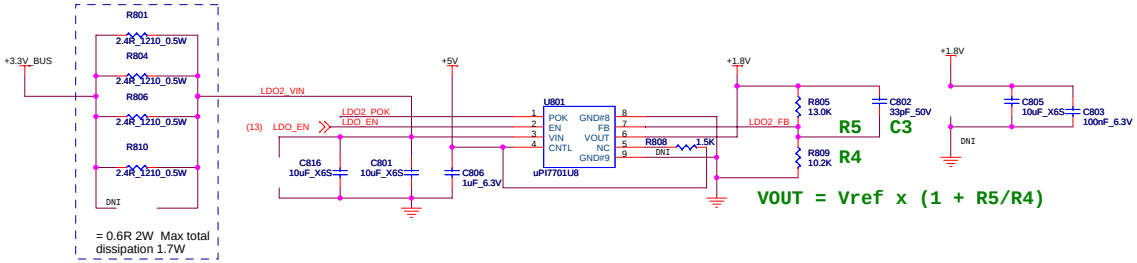
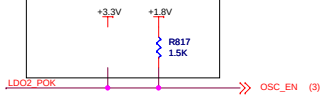
**LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 1.7A (TBV) RMS MAX**

**PCB: Min 70mm sq. copper area for cooling**



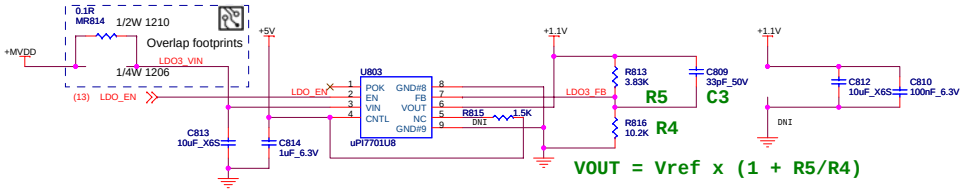

Install R817 if Y1 is a 1.8V Device

Install R807 if Y1 is a 3.3V Device

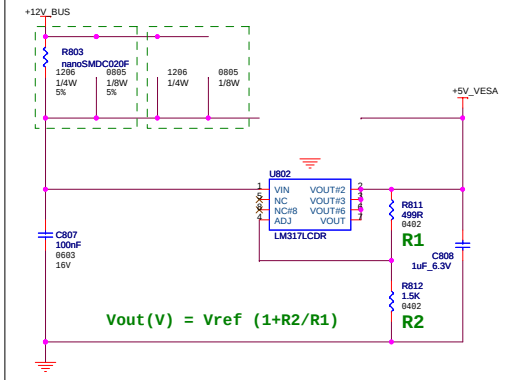


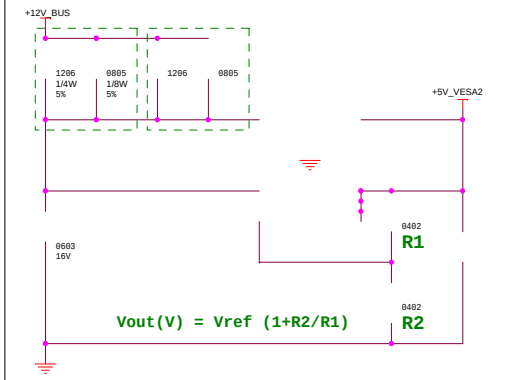

**LDO #3: Vin = +1.50V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX**

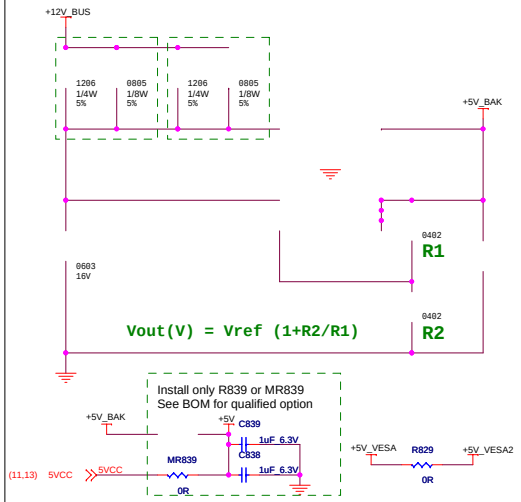
**PCB: Min 70mm sq. copper area for cooling**




## Regulators for +5V, +5V_VESA and +5V_VESA2



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See BOM for qualified filters

(3) A_DAC1_R — L1001 47nH — R1001 75R 402 — 402 — 402
(3) A_DAC1_RB — R1027 37.4R
(3) A_DAC1_G — L1002 47nH — R1002 75R 402 — 402 — 402
(3) A_DAC1_GB — R1028 37.4R
(3) A_DAC1_B — L1003 47nH — R1003 75R 402 — 402 — 402
(3) A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

L100x and ML100x footprints are overlapped

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

For ESD Protection

+3.3V
+5V_VESA
+5V_VESA
603

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

(3) DDC4DATA — +5V — R1005 2.2K — DDCDATA_DAC1_5V — R1006 33R 402 — DDCDATA_DAC1_R
(3) DDC4CLK — +5V — R1008 2.2K — DDCCLK_DAC1_5V — R1009 33R 402 — DDCCLK_DAC1_R

C1999 100nF 6.3V +5V
(3,7) HSYNC1 — U1999A 74VHC125 — HSYNC_DAC1_B — R1010 10R 402 — HSYNC_DAC1_R
(3,7) VSYNC1 — U1999B 74VHC125 — VSYNC_DAC1_B — R1011 10R 402 — VSYNC_DAC1_R

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

| DB15 pin | Standard VGA | DDC1 Host | DDC2B or DDC2B+ Host | DDC2AB Host | DDC1/2 Display |
|---|---|---|---|---|---|
| 11 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Optional |
| 12 | Monitor ID bit 1 | Data from display | SDA | SDA | SDA |
| 4 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Optional |
| 15 | Monitor ID bit 3 | Open | SCL | SCL | SCL |
| | | +5V | +5V | +5V | |
| 9 | N/C | 50mA min | 50mA min | 300mA min | Optional |
| | Mechanical Key | 1A max | 1A max | 1A max | |
| Hardware Support | No | Yes | Yes | No | Yes |

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

+3.3V
Q1021 MMBT3904
R1022 10K
R1023 10K
(7) HPD2
HPD_DVI2

(3) T2X2M
(3) T2X2P
(3) T2X4M
(3) T2X4P
DDCCLK_DAC1_R
DDCDATA_DAC1_R
VSYNC_DAC1_R
(3) T2X1M
(3) T2X1P
(3) T2X3M
(3) T2X3P
(3) T2X0M
(3) T2X0P
(3) T2X5M
(3) T2X5P
(3) T2XCP
(3) T2XCM
A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
HSYNC_DAC1_R

+5V_VESA

J1001 DVI_CONNECTOR

| | | | |
|---|---|---|---|
| 25 | CASE | | |
| 1 | TMDS Data2- | C1 | Analog Red |
| 2 | TMDS Data2+ | C2 | Analog Green |
| 3 | TMDS Data2/4 Shield | C3 | Analog Blue |
| 4 | TMDS Data4- | C4 | Analog HYNC |
| 5 | TMDS Data4+ | C5 | Analog GND |
| 6 | DDC Clock | C6 | Analog GND#C6 |
| 7 | DDC Data | | |
| 8 | Analog VSYNC | 26 | CASE#26 |
| 9 | TMDS Data1- | 27 | CASE#27 |
| 10 | TMDS Data1+ | 28 | CASE#28 |
| 11 | TMDS Data1/3 Shield | 29 | CASE#29 |
| 12 | TMDS Data3- | 30 | CASE#30 |
| 13 | TMDS Data3+ | | |
| 14 | +5V Power | | |
| 15 | GND (for +5V) | | |
| 16 | Hot Plug Detect | | |
| 17 | TMDS Data0- | | |
| 18 | TMDS Data0+ | | |
| 19 | TMDS Data0/5 Shield | | |
| 20 | TMDS Data5- | | |
| 21 | TMDS Data5+ | | |
| 22 | TMDS Clock Shield | | |
| 23 | TMDS Clock+ | | |
| 24 | TMDS Clock- | | |



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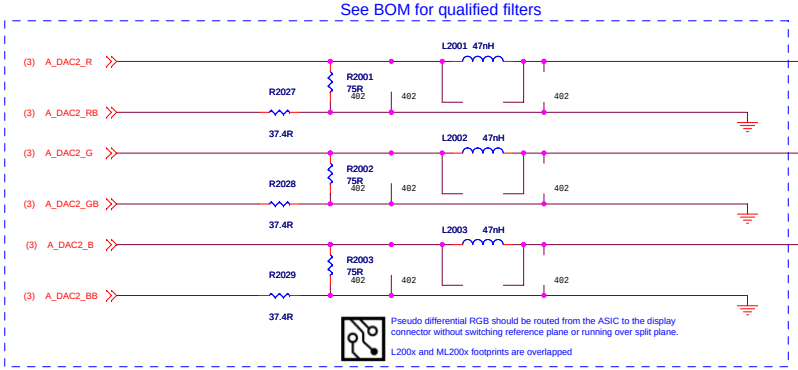
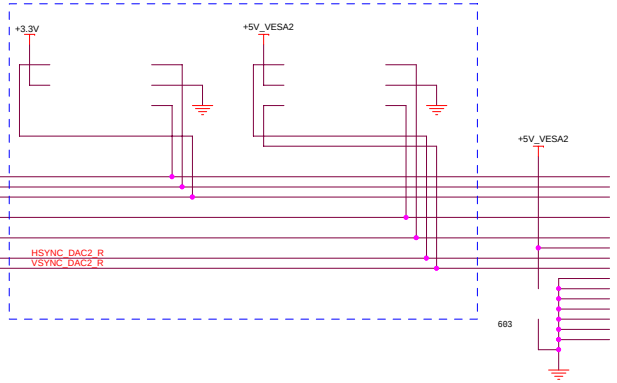
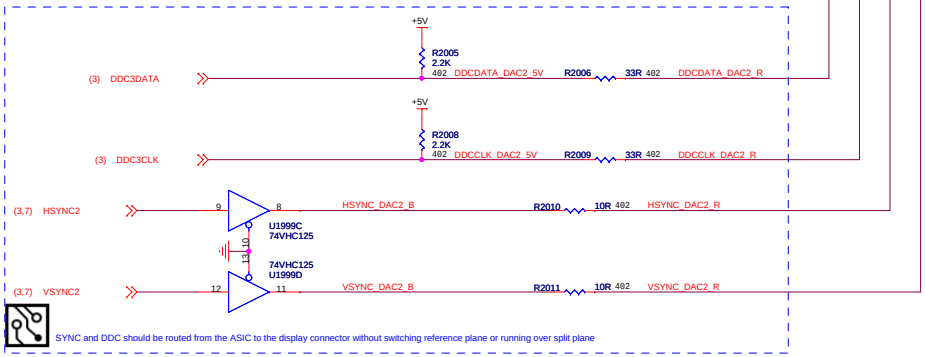
See BOM for qualified filters

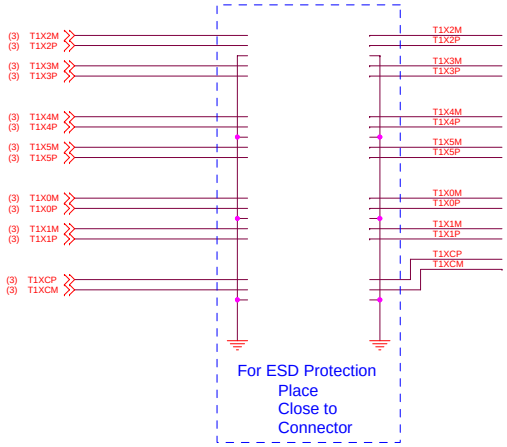


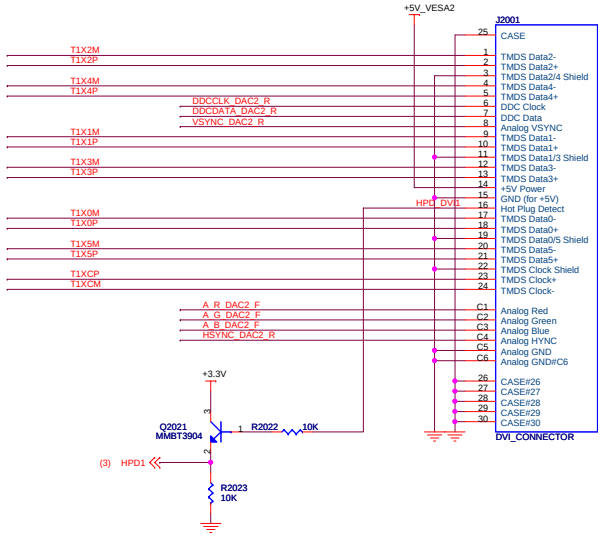




| DB15 pin | Standard VGA | DDC1 Host | DDC2B or DDC2B+ Host | DDC2AB Host | DDC1/2 Display |
|---|---|---|---|---|---|
| 11 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Monitor ID bit 0 | Optional |
| 12 | Monitor ID bit 1 | Data from display | SDA | SDA | SDA |
| 4 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Monitor ID bit 2 | Optional |
| 15 | Monitor ID bit 3 | Open | SCL | SCL | SCL |
| 9 | N/C | +5V 50mA min 1A max | +5V 50mA min 1A max | +5V 300mA min 1A max | Optional |
| Hardware Support | Mechanical Key | No | Yes | Yes | No | Yes |

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



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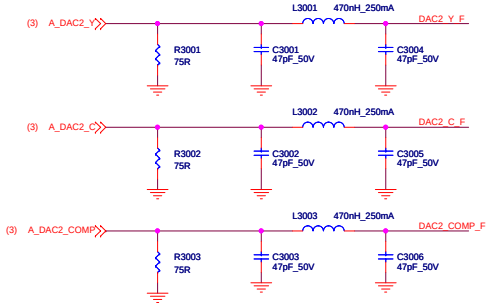


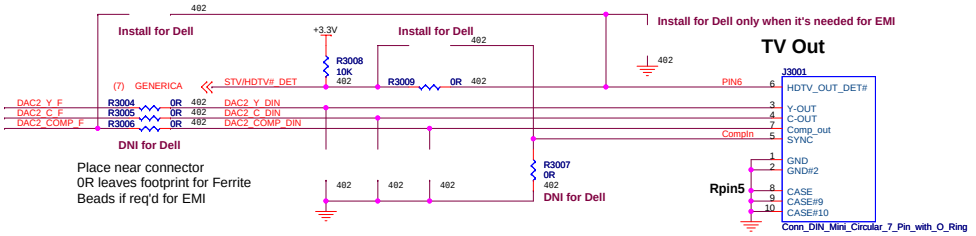


- 4-pin Svideo MiniDIN P/N 6070001000G



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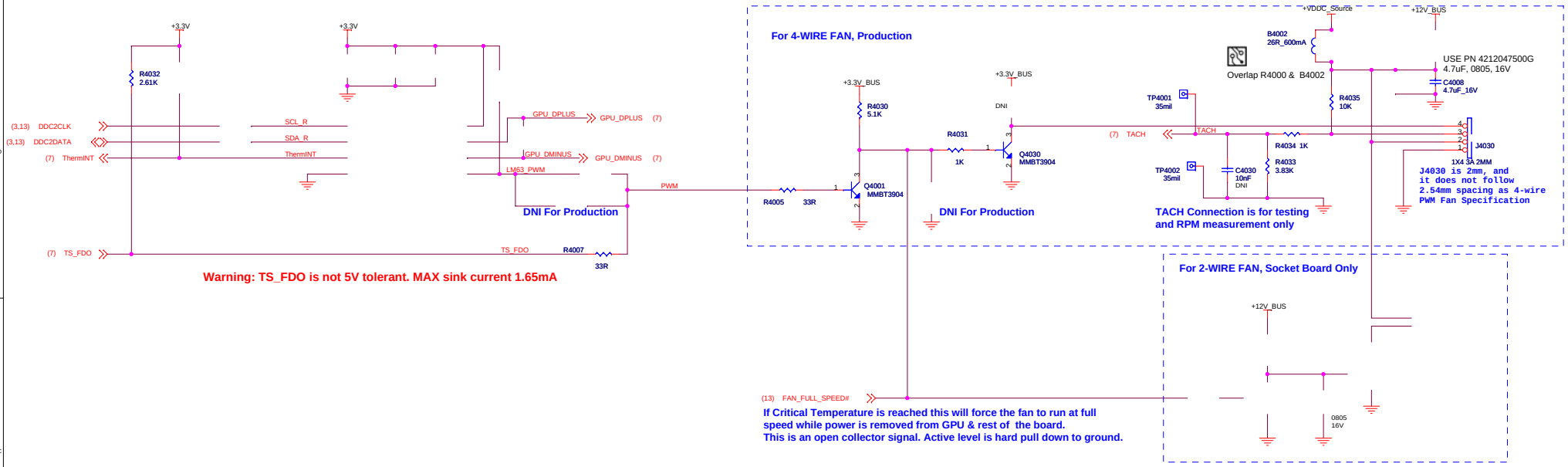


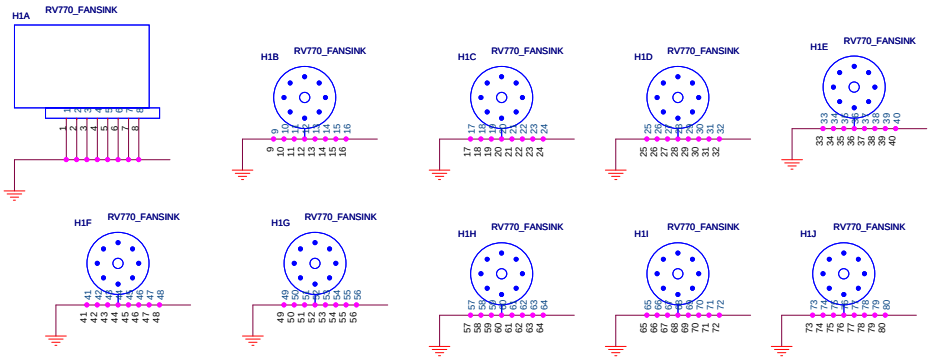




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ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY1
ANTISTATIC
BAG
0

BKT1: DS, DVI - DIN - DVI

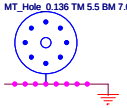
BKT2
BRACKET
8020038600G

VDDC1

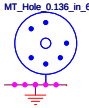
MVDD1

TPC1

MT1
MT_Hole_0.136 TM 5.5 BM 7.0



MT2
MT_Hole_0.136_in_6VIA



PCB1
PCB
109-B50131-00

# PCIE 12V/3.3V Power up Bonding support



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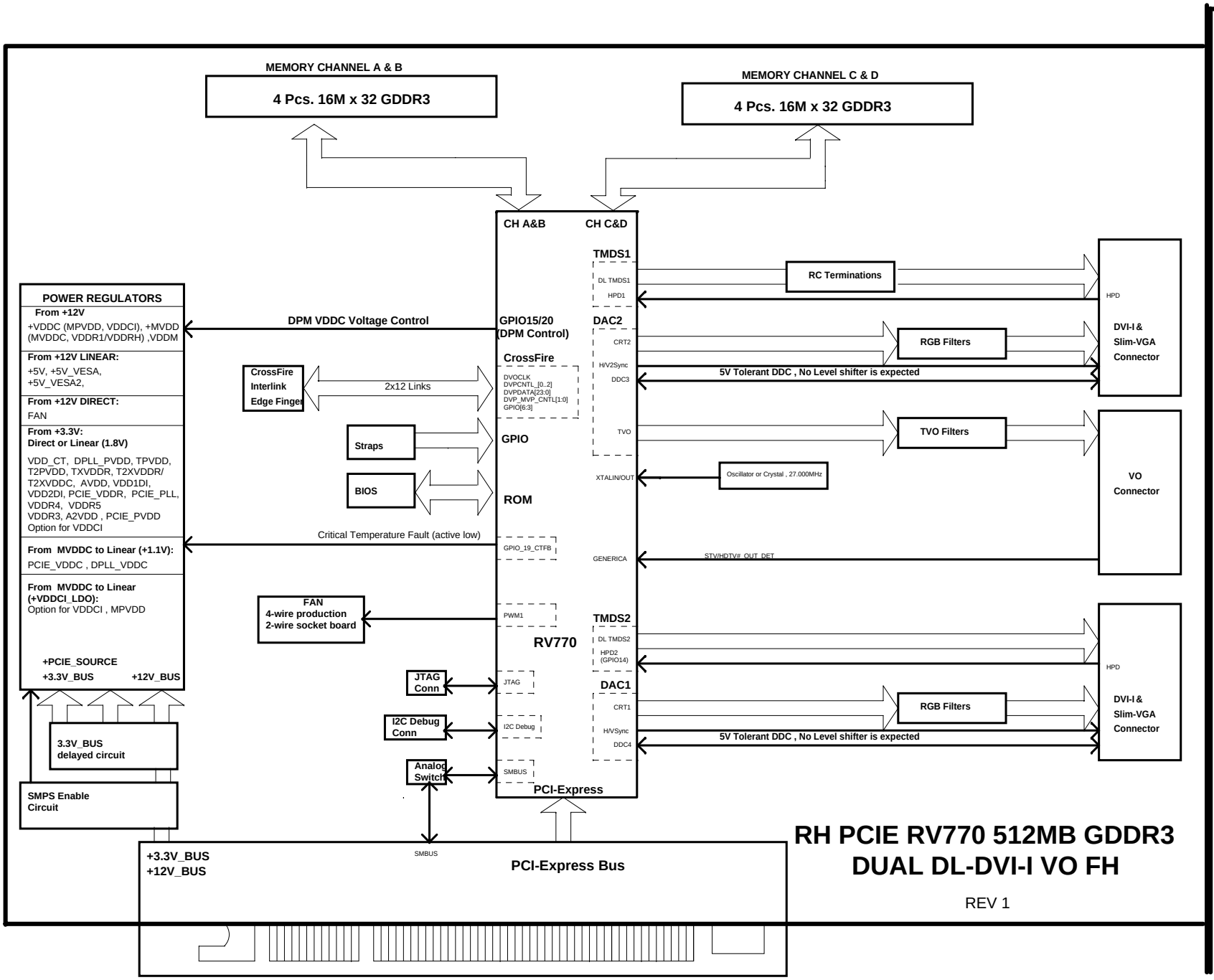
| Title | Schematic No. | Date: |
|---|---|---|
| RH PCIE RV770 512MB GDDR3 DUAL DL-DVI-I VO FH | 102-B50102-00 | Thursday, June 05, 2008 |

# REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
**For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.**
**Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 25

| Sch Rev | PCB Rev | Date | REVISION DESCRIPTION |
|---|---|---|---|
| 0 | 00A | 07/10/11 | Initial design for RV770 GDDR3 |
| 1 | 00B | 08/02/25 | Improvement:<br>1) Add 1 uF CAP on memory reset, Pg5<br>2) MVDDC current leakage board workaround; Pg13<br>3) MVDD Themal Protection, Pg 13<br>4) Improvement on Hot Plug protection Pg13<br>5) 12V_BUS & 12V_EXT Input Switch Circuit Page 13 |
| 2 | 00 | 08/03/27 | 1.Correct PTC comparator power connection.<br>2. Add Fuse NF1200 on page 13 |



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