GA102 DT SKU P-BOARD

350W, FH Std PCB, 384b, GDDR6X x8
DP + DP + DP + HDMI/DP

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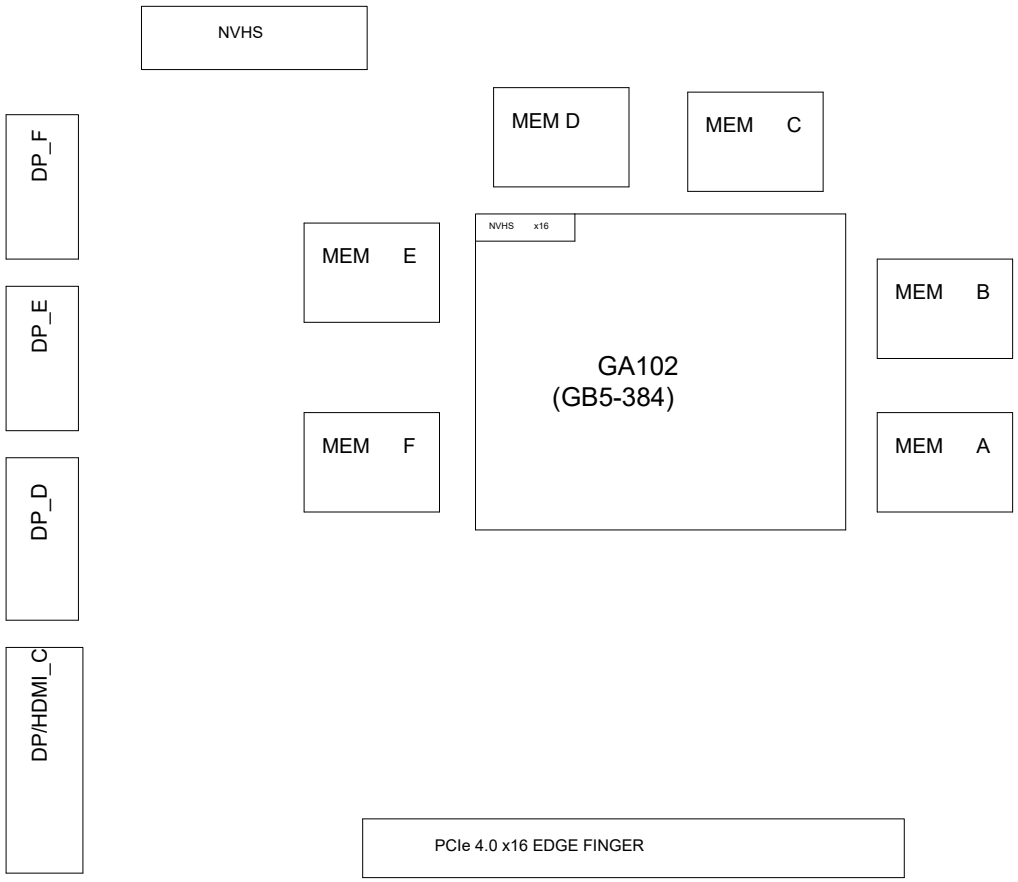
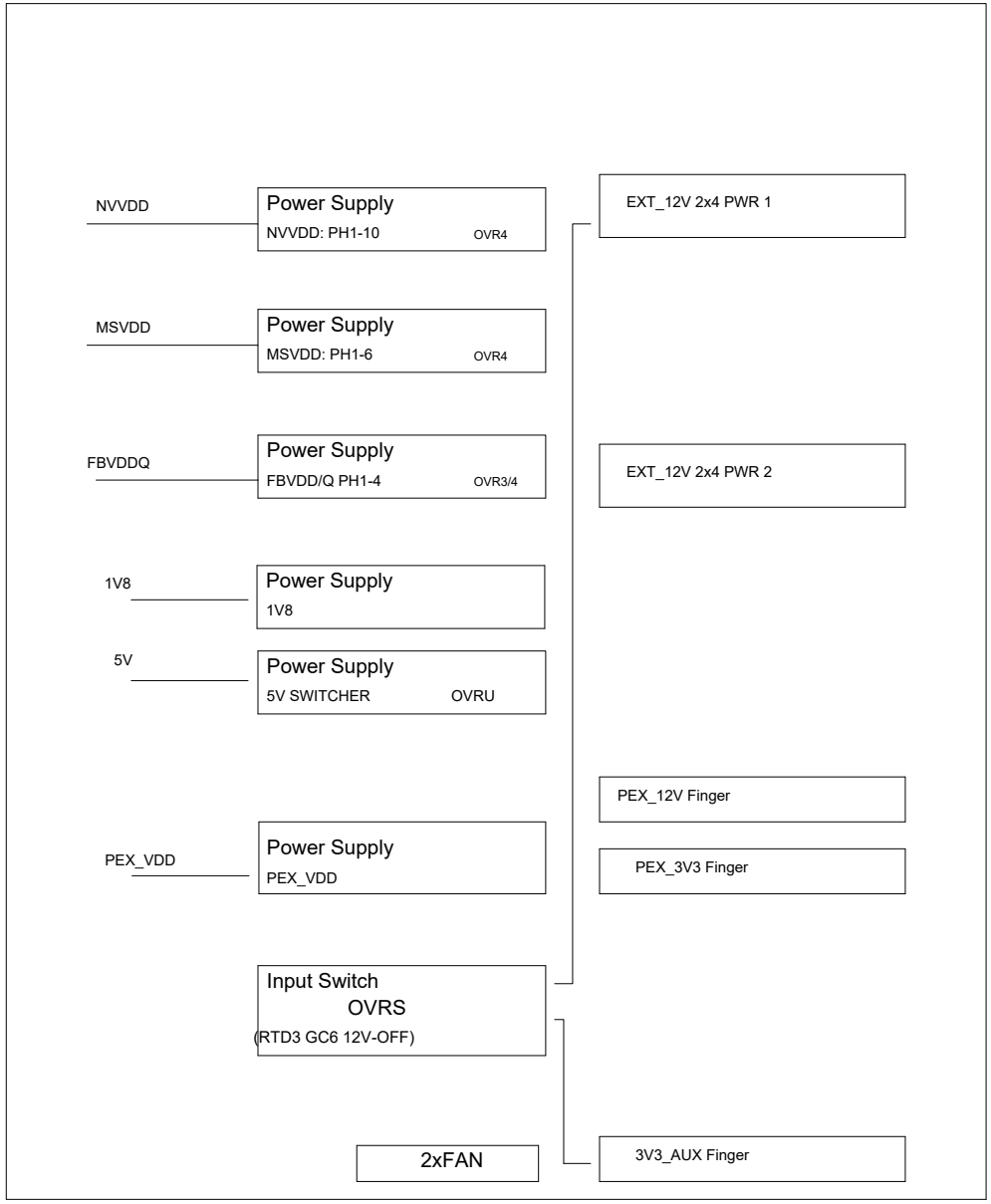
Block Diagram





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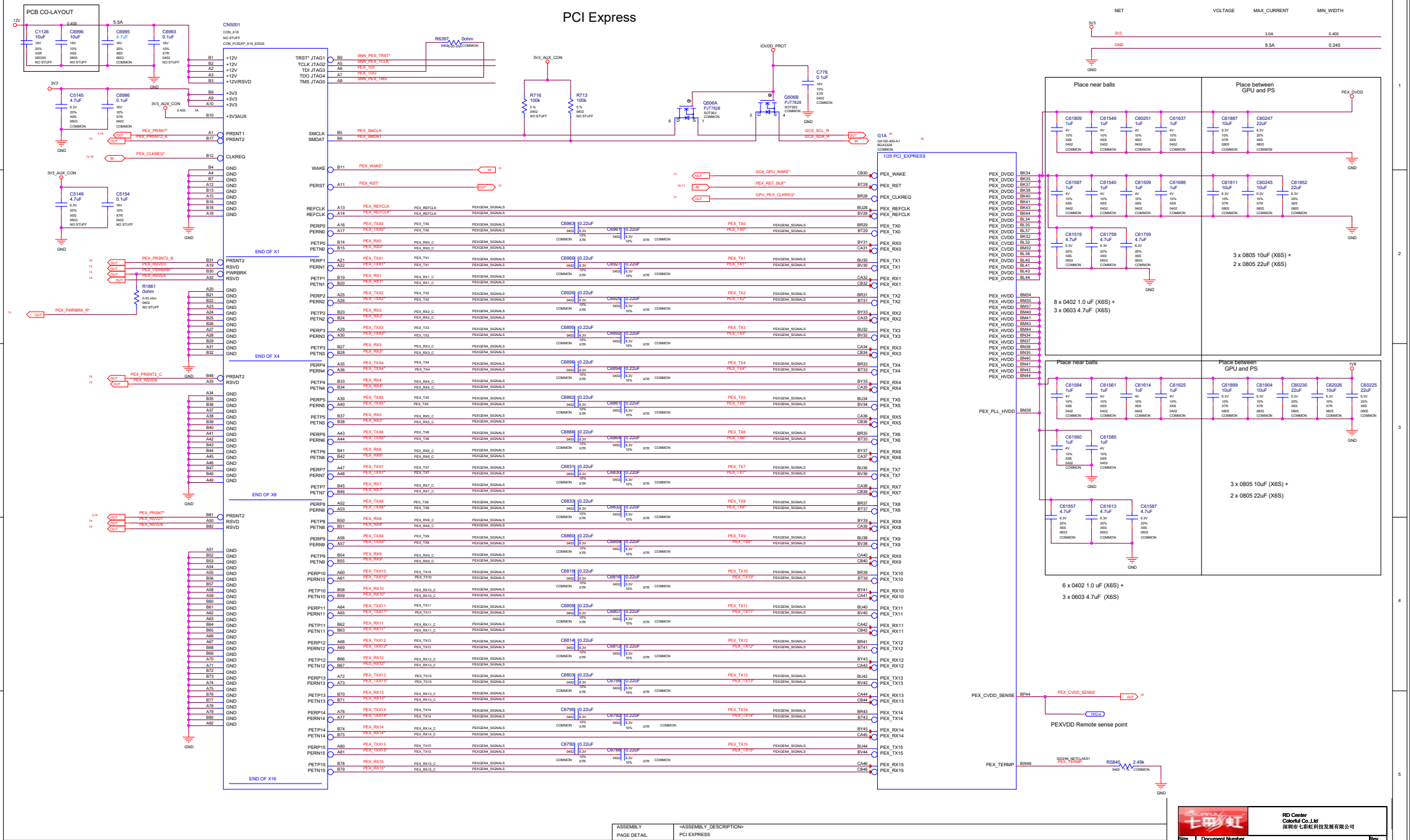
PCI Express



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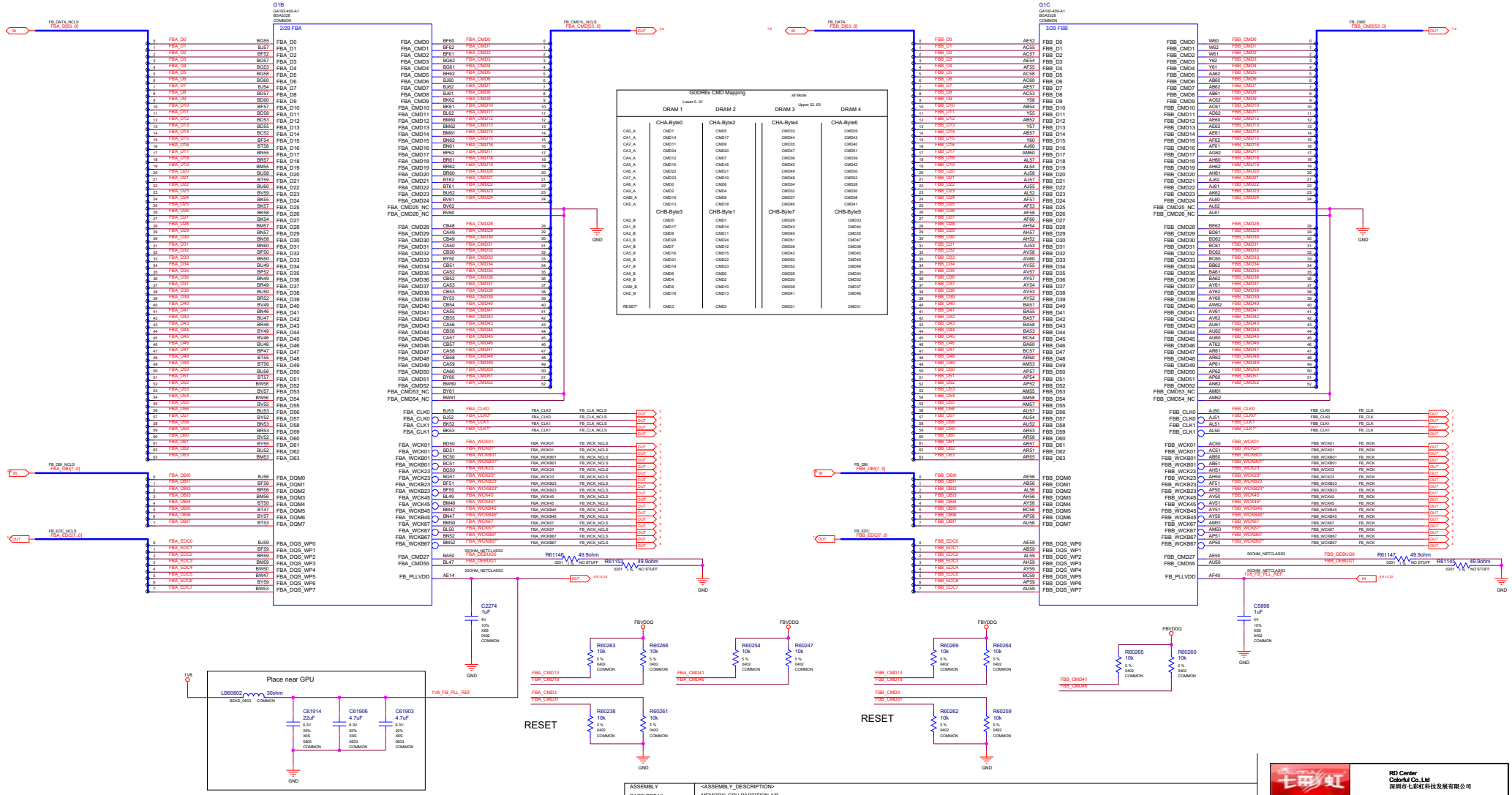
MEMORY: GPU Partition A/B



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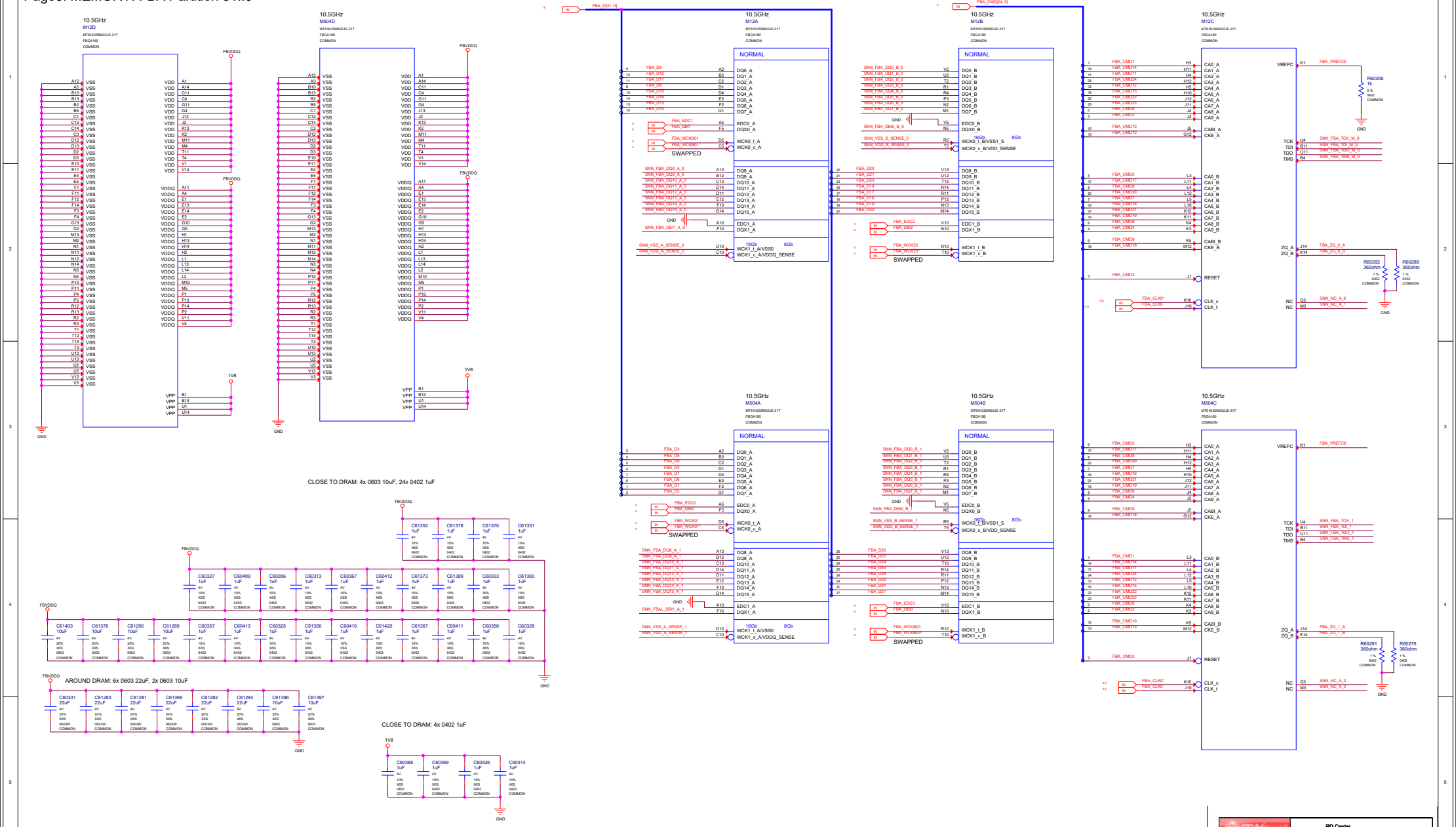

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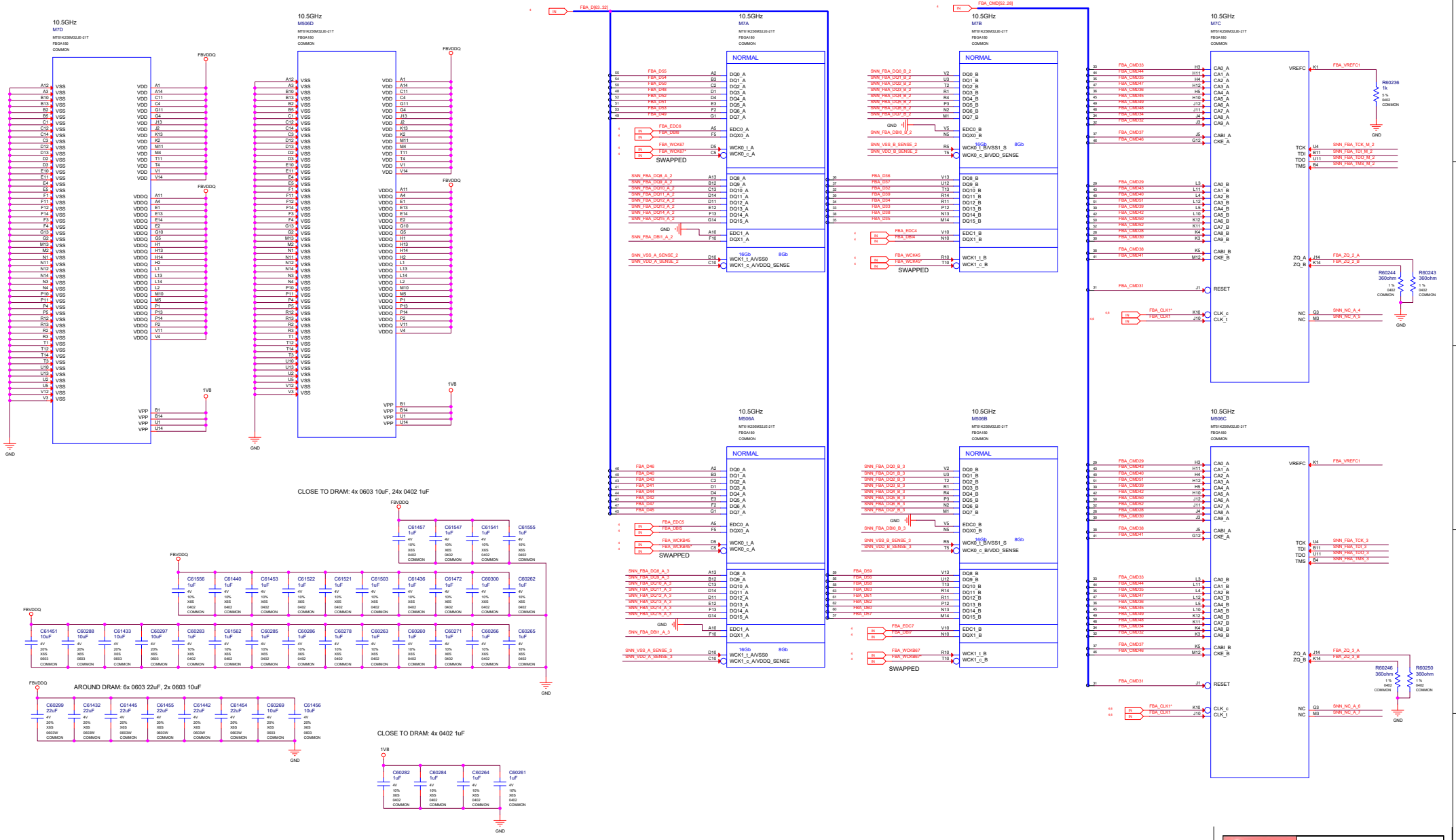

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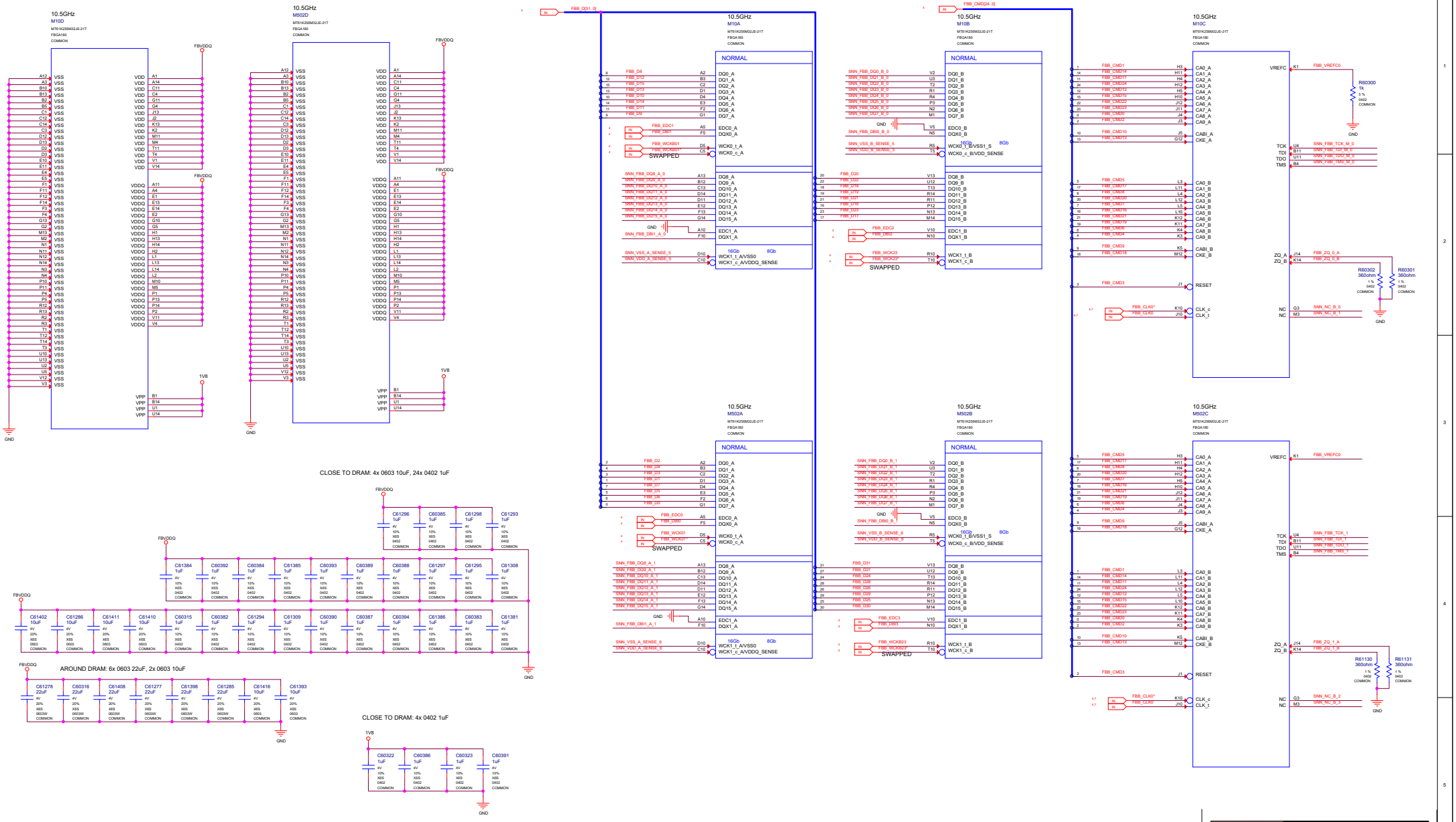

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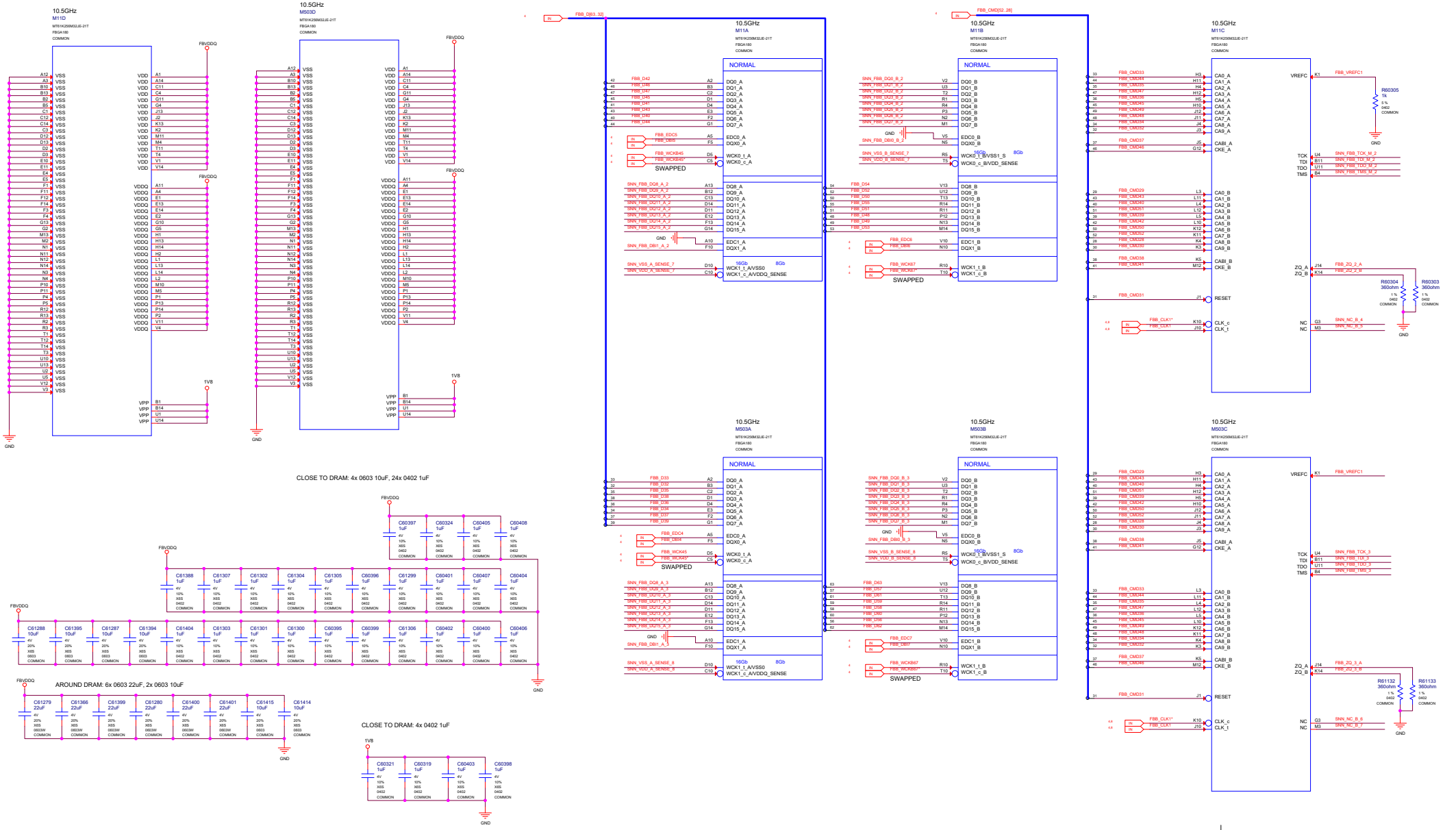

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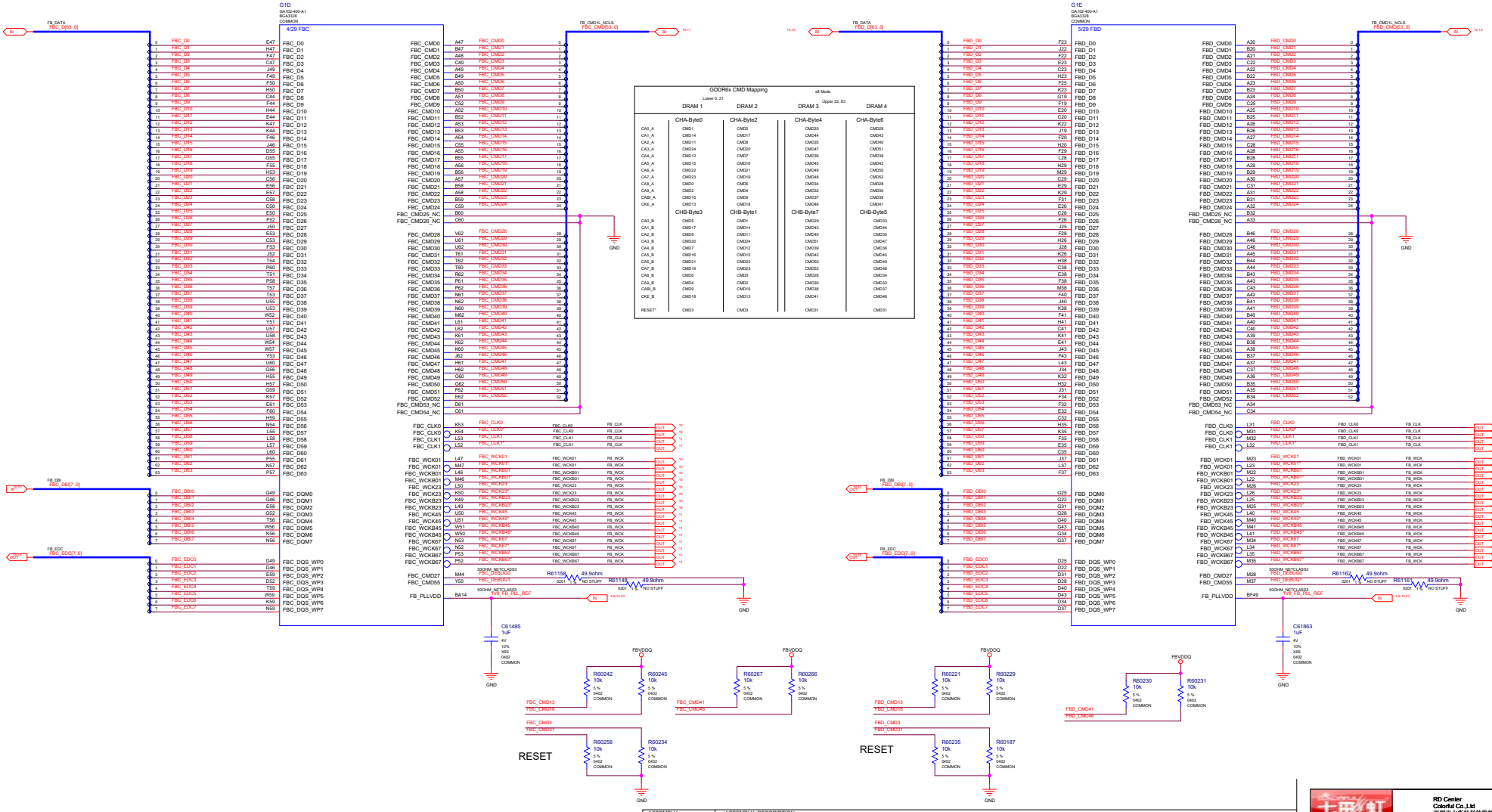
MEMORY: GPU Partition C/D



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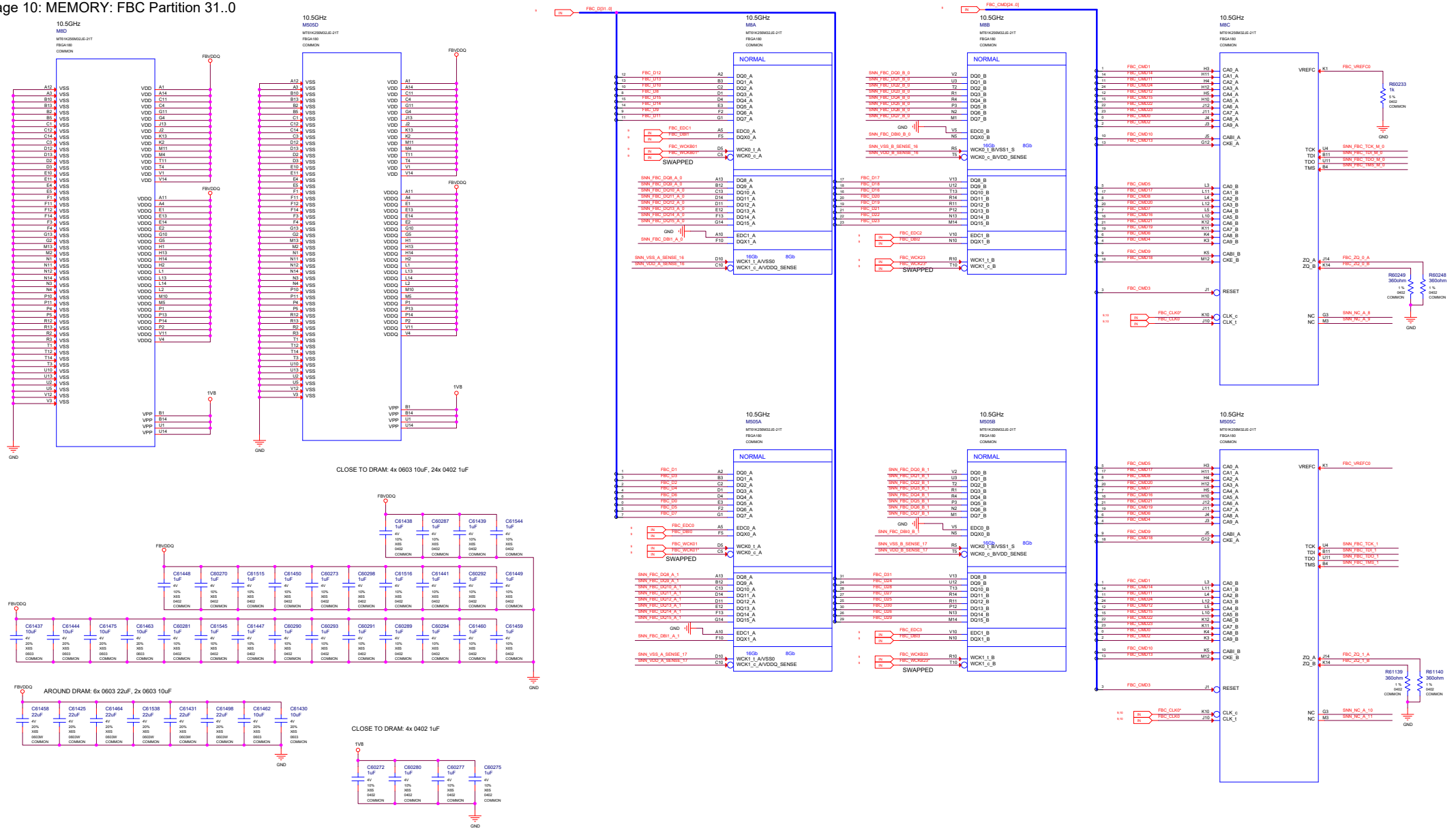

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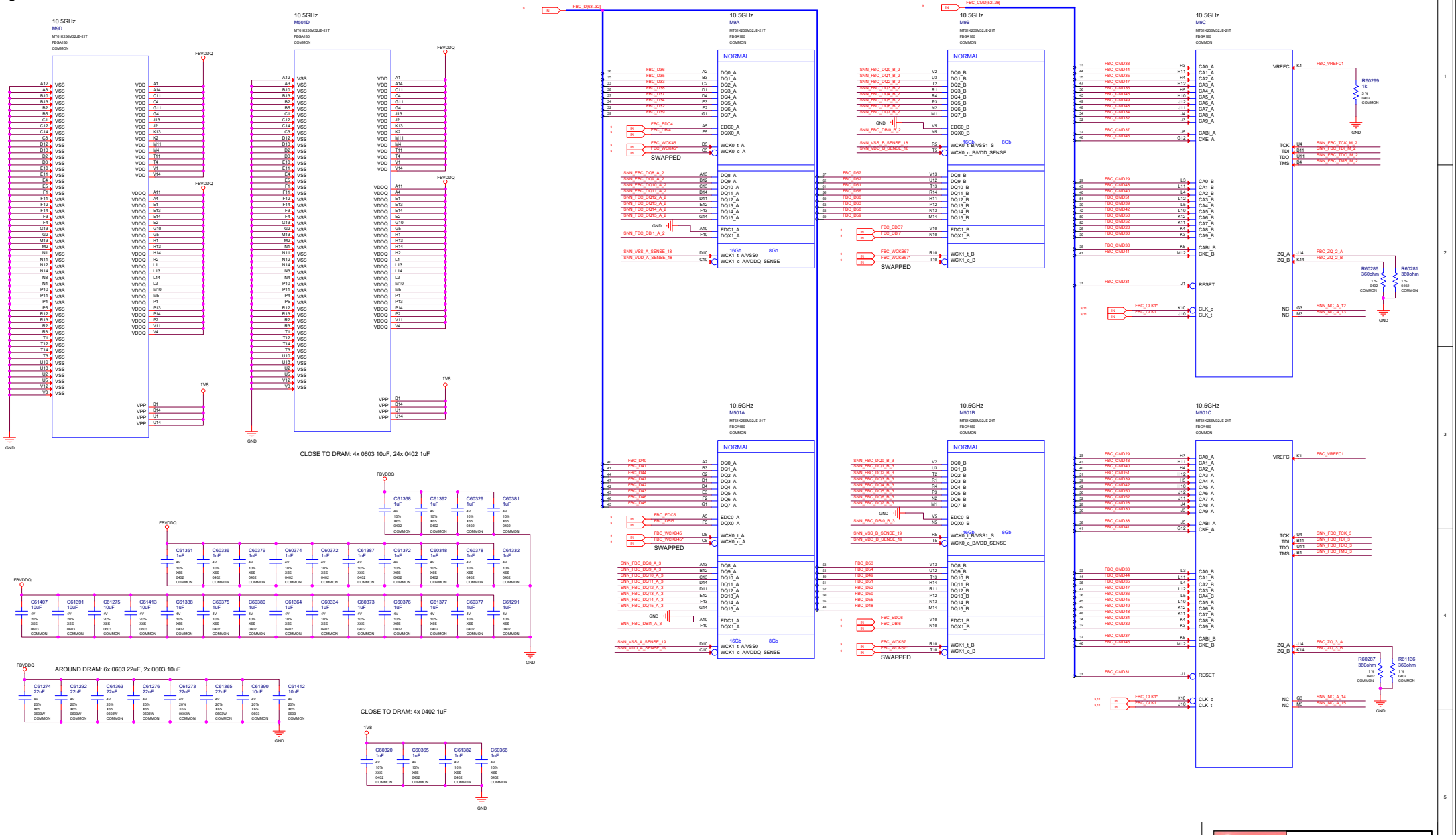

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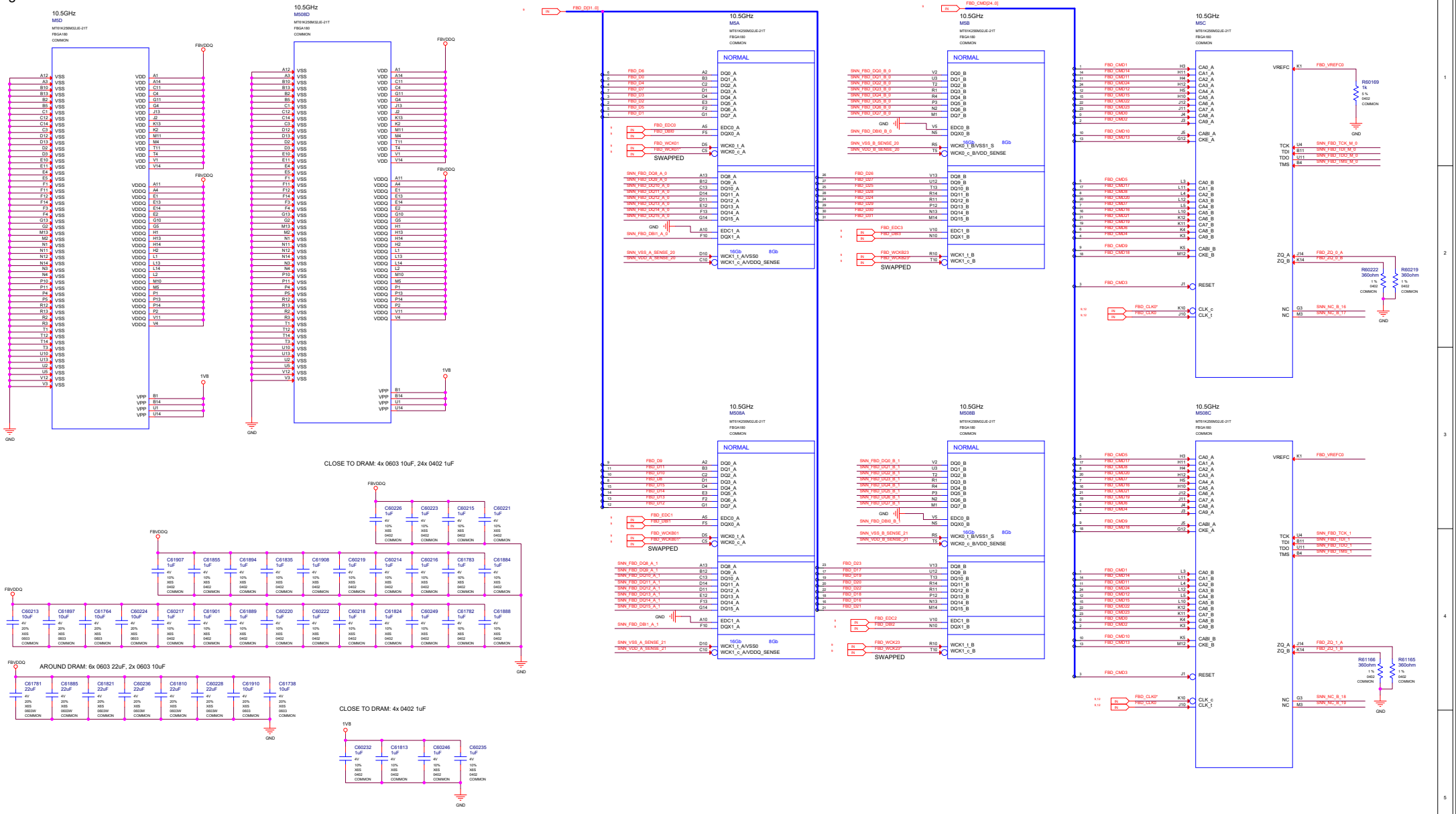

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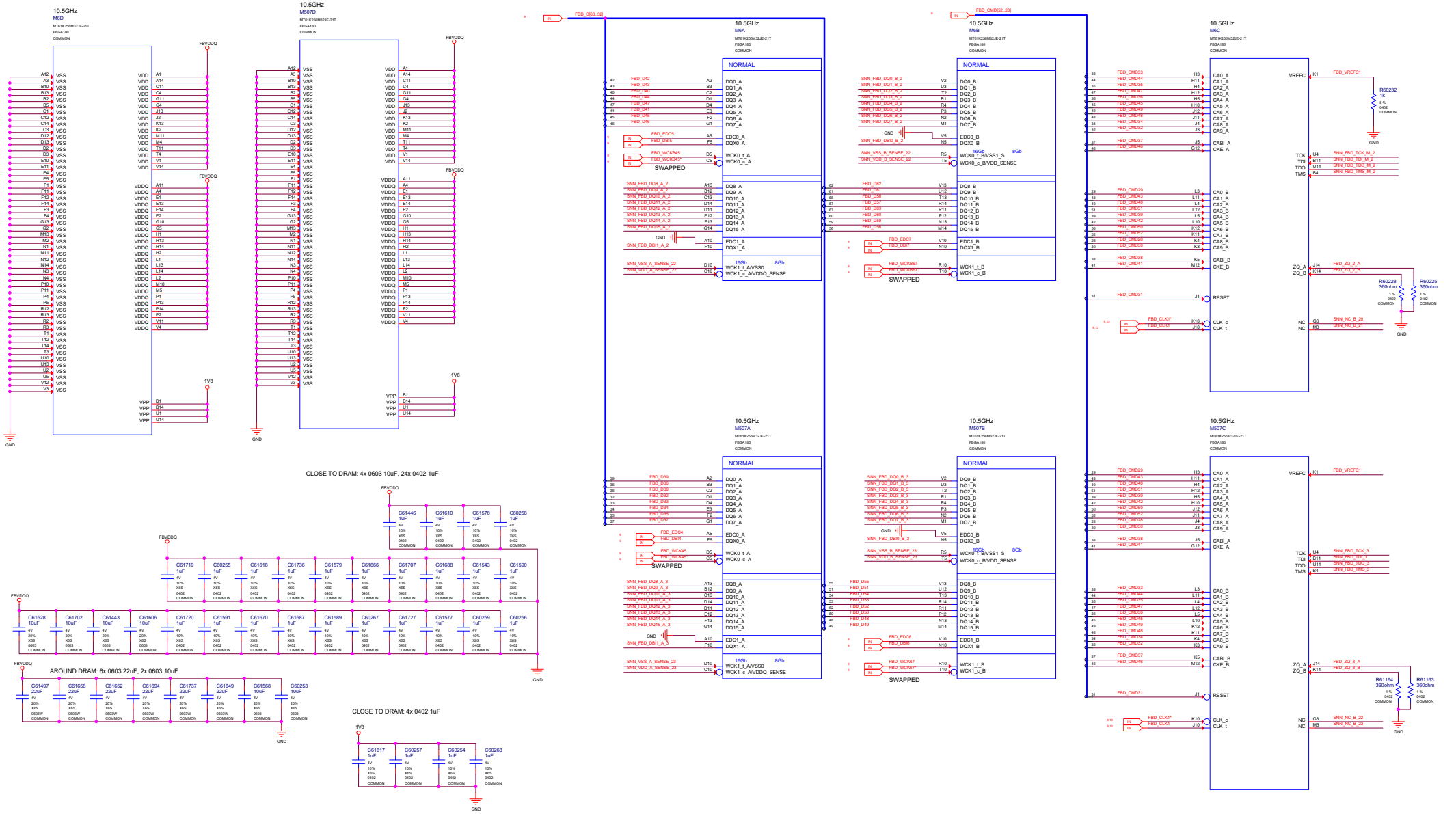

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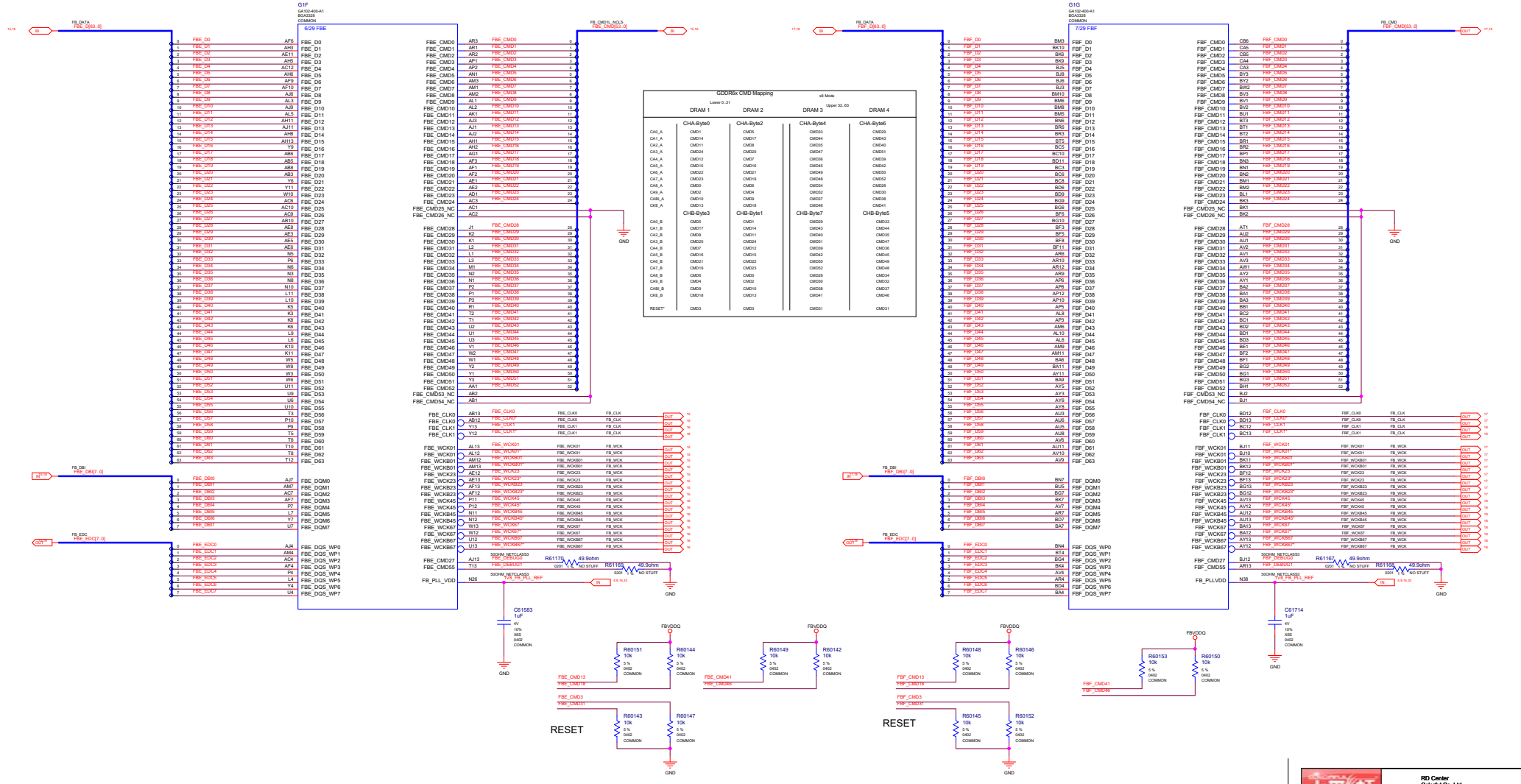
MEMORY: GPU Partition E/F



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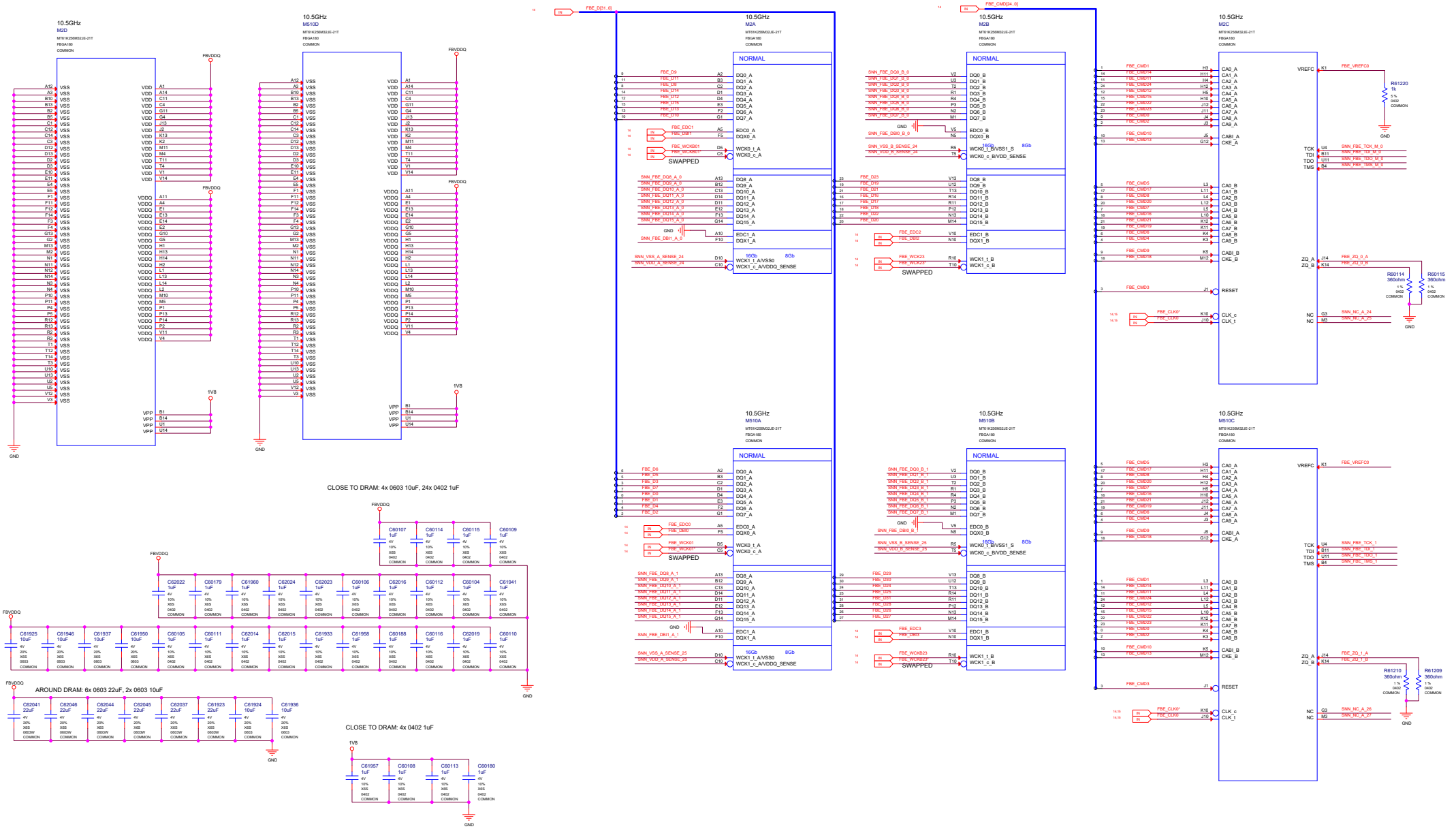

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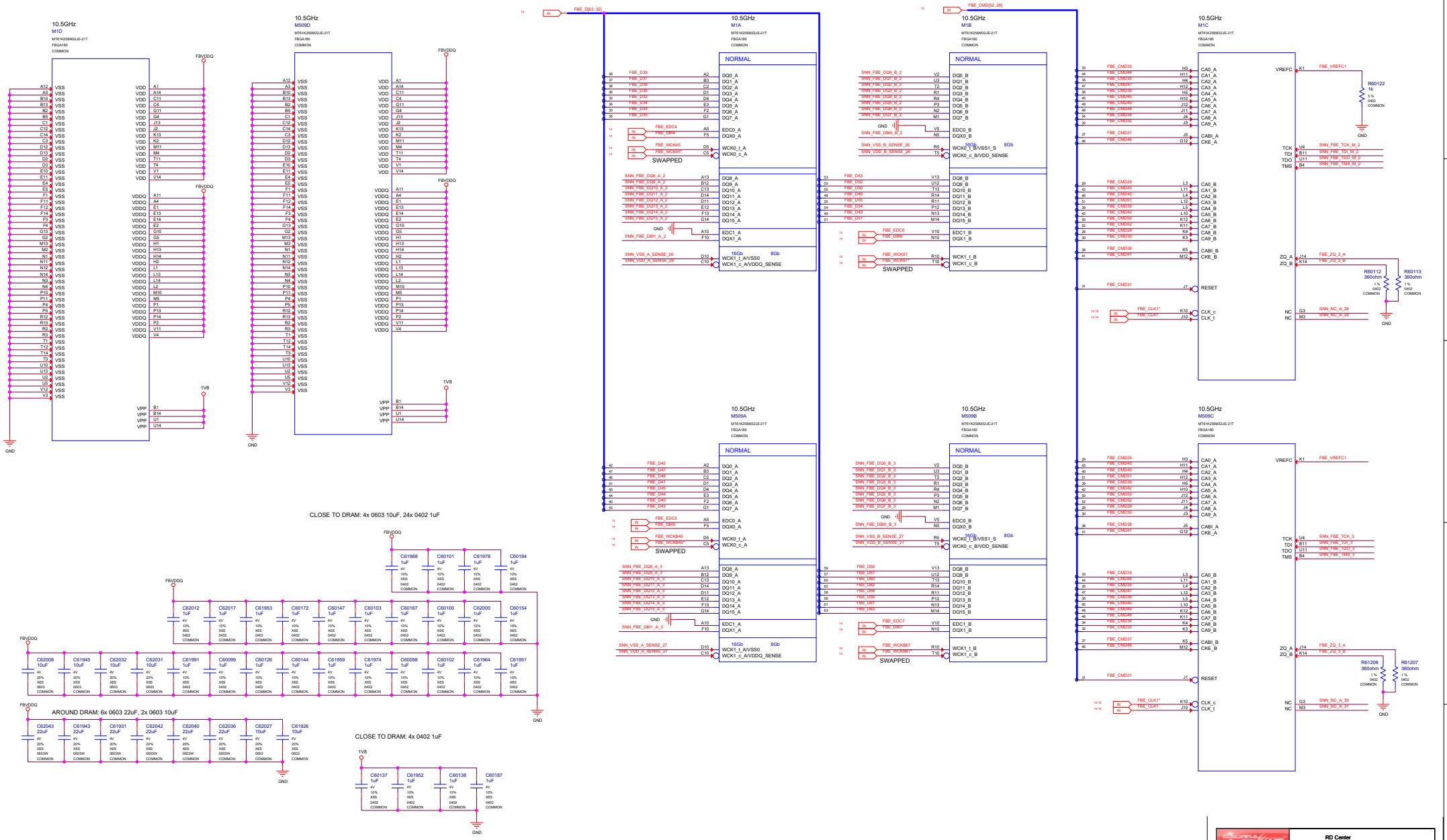

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Page 17: MEMORY: FBF Partition 31..0

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBF PARTITION[31:0]

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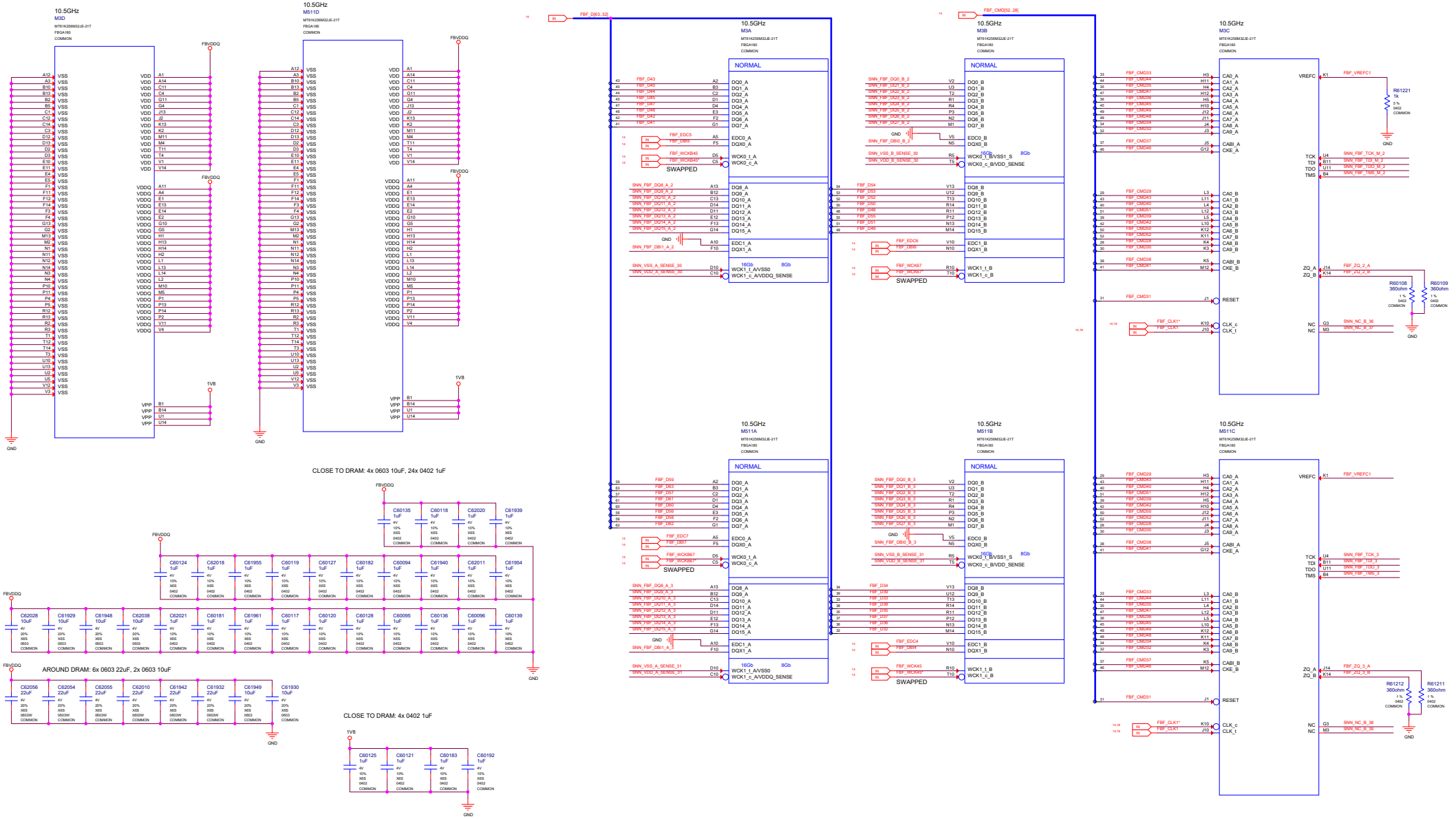
Page 18: MEMORY: FBF Partition 63..32



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PAGE DETAIL	MEMORY: FBF PARTITION[63:32]

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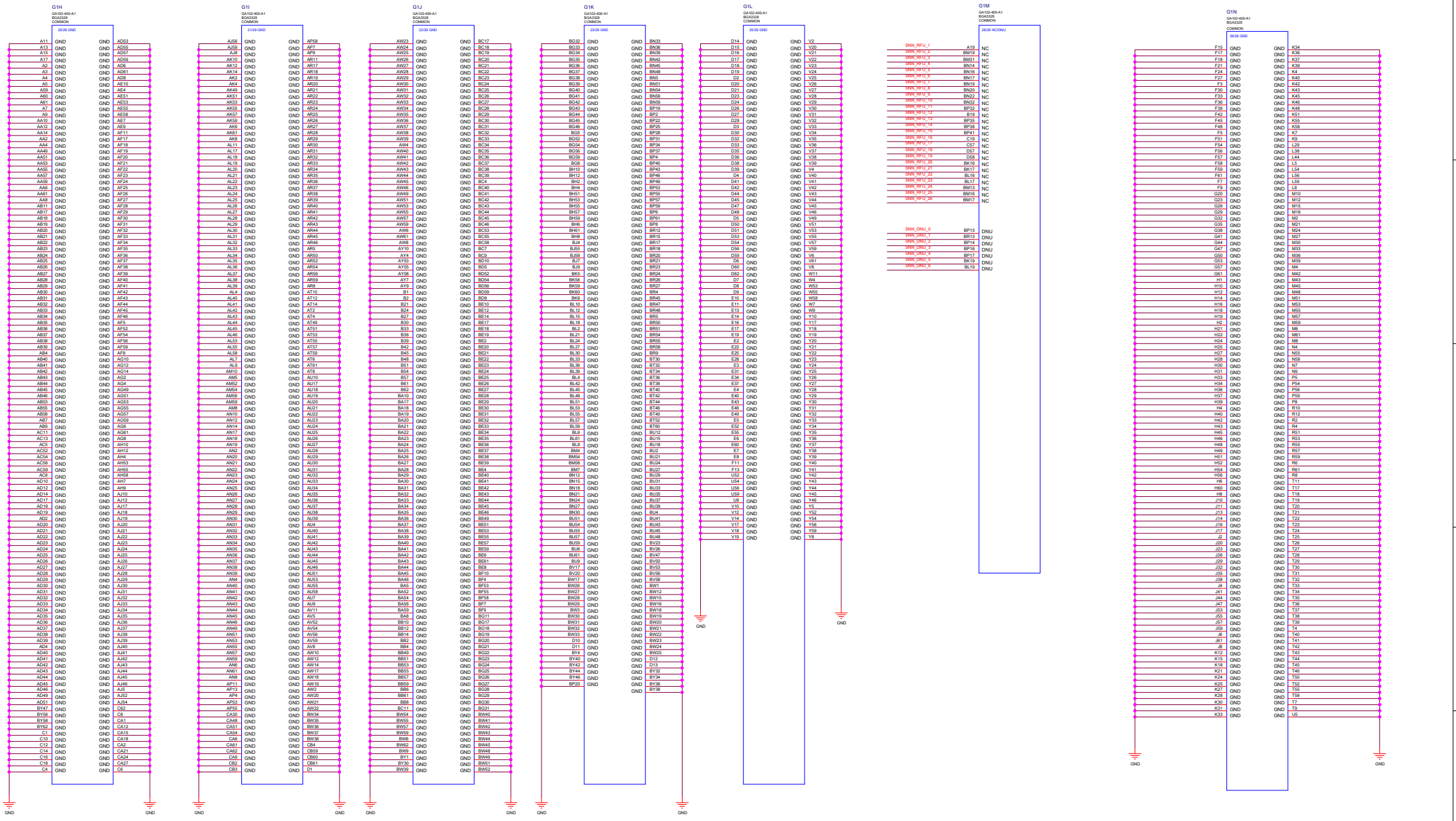
GPU GND, RFUs & RSVD



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU GND, RFUs & RSVD

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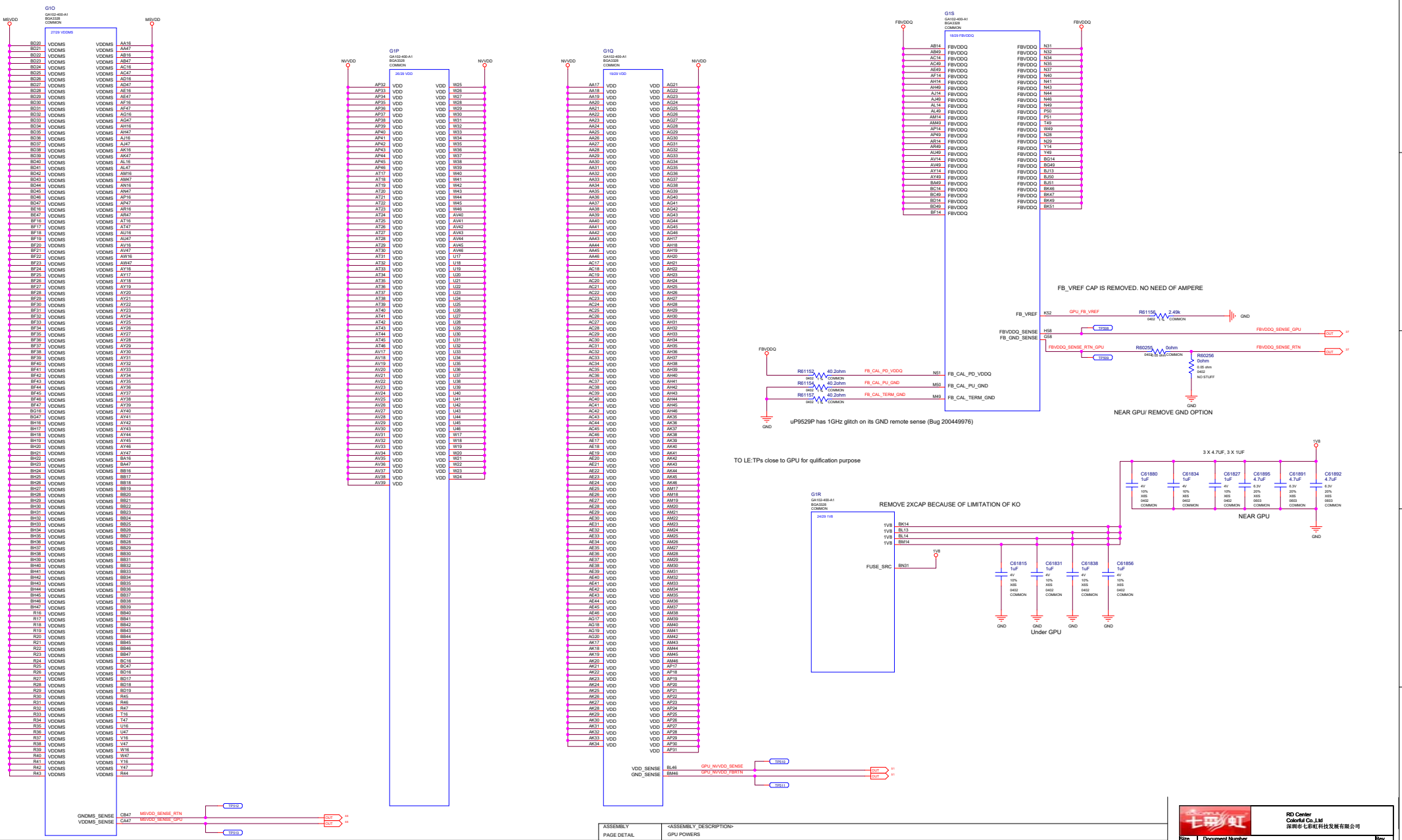
GPU PWR and GND



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU POWERS

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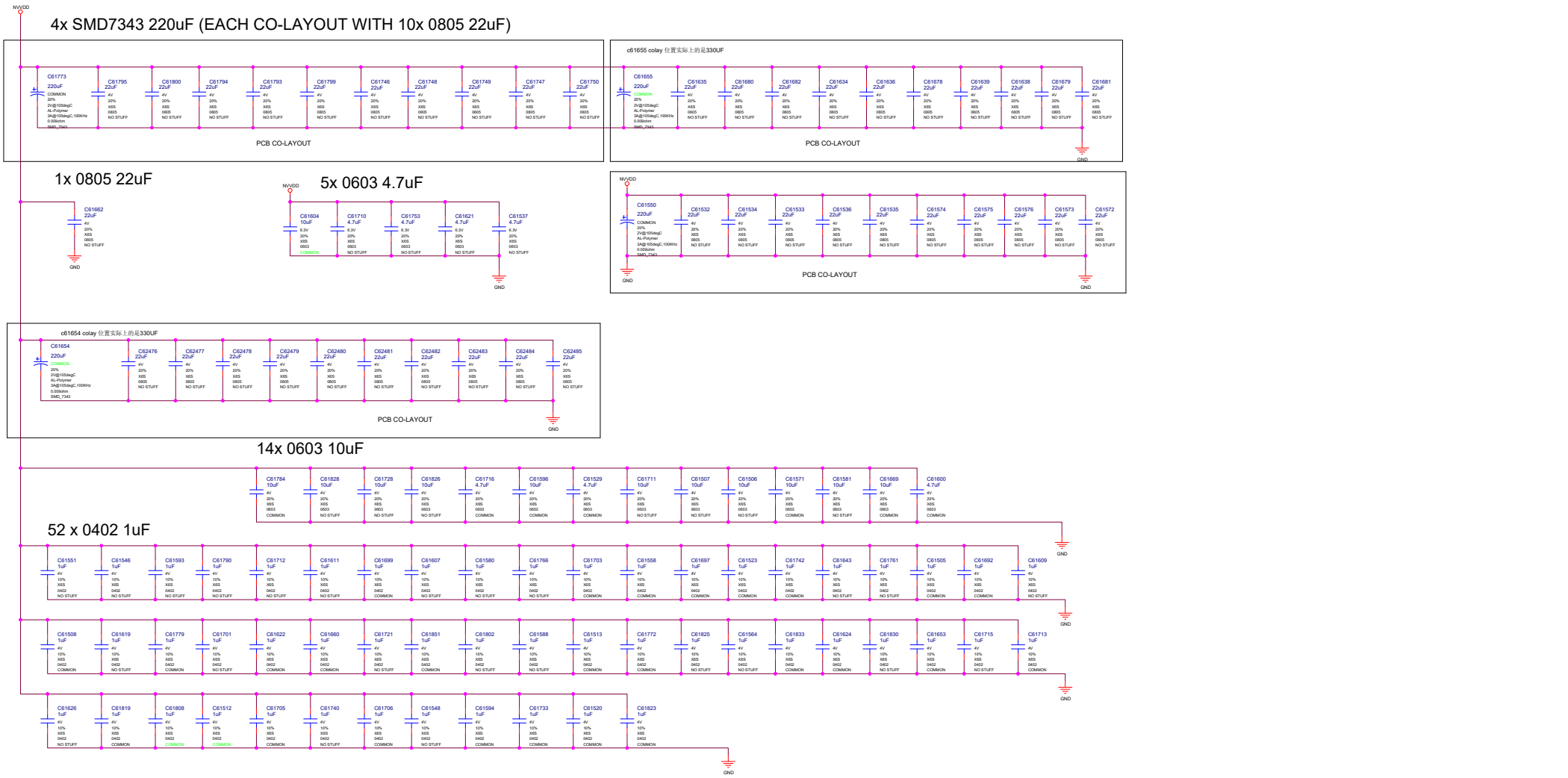
NVVDD

UNDER GPU



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU: NVVDD DECOUPLING

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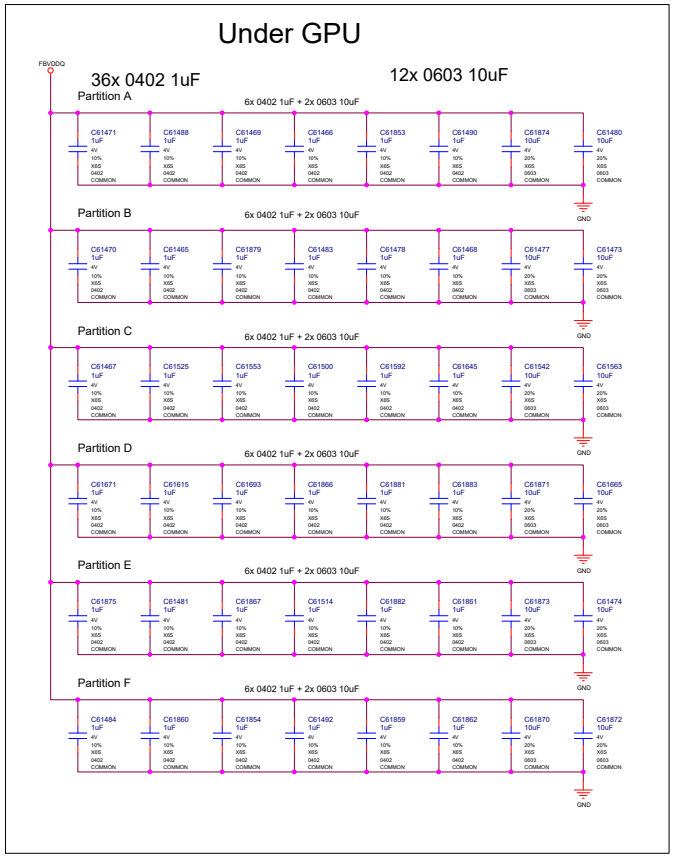
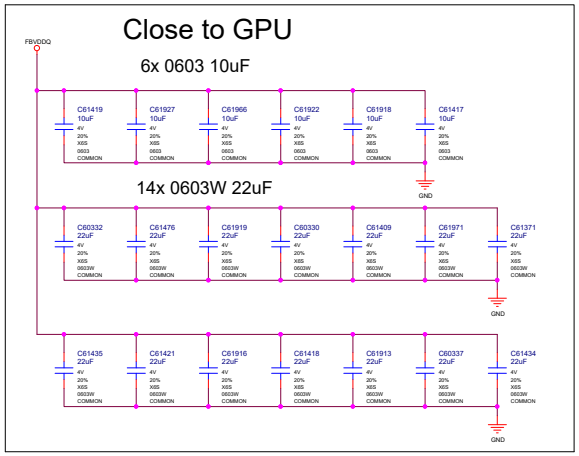
FBVDDQ





ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU: FBVDD DECOUPLING

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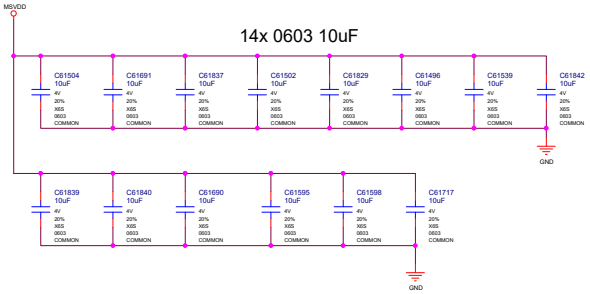
Page 23: GPU: MSVDD DECOUPLING

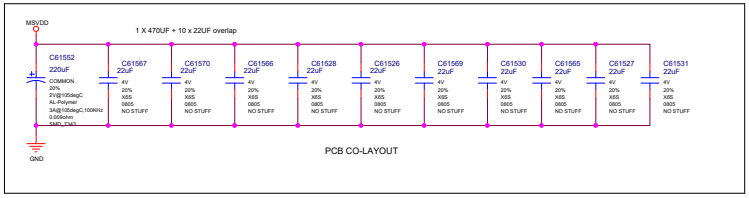
UNDER GPU

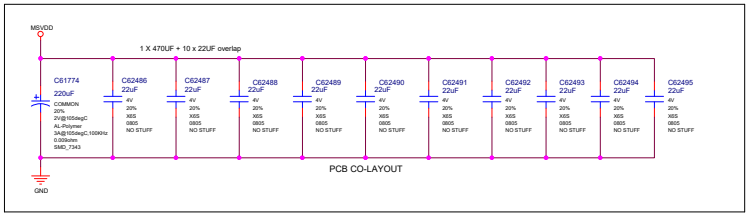
MSVDD

14x 0603 10uF

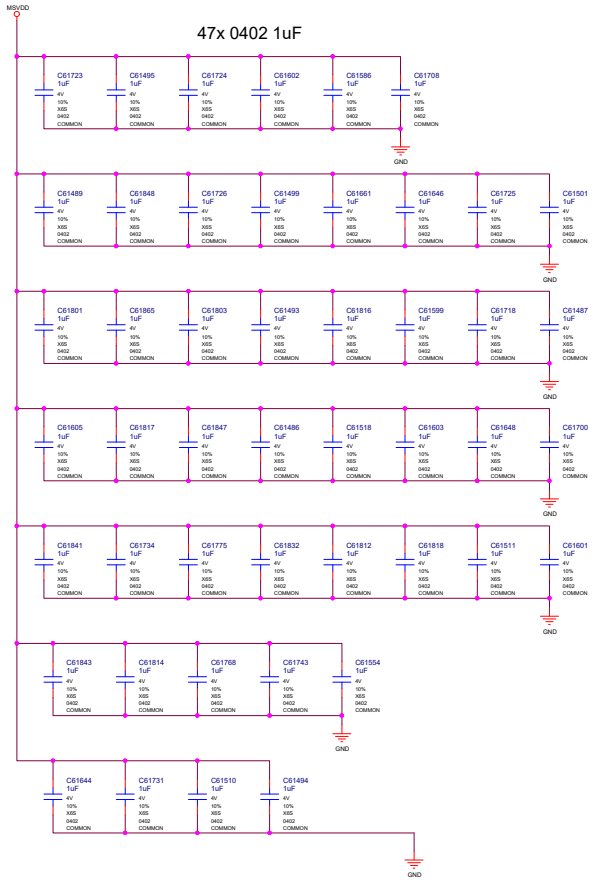


2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)





47x 0402 1uF



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU: MSVDD DECOUPLING

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	BLANK

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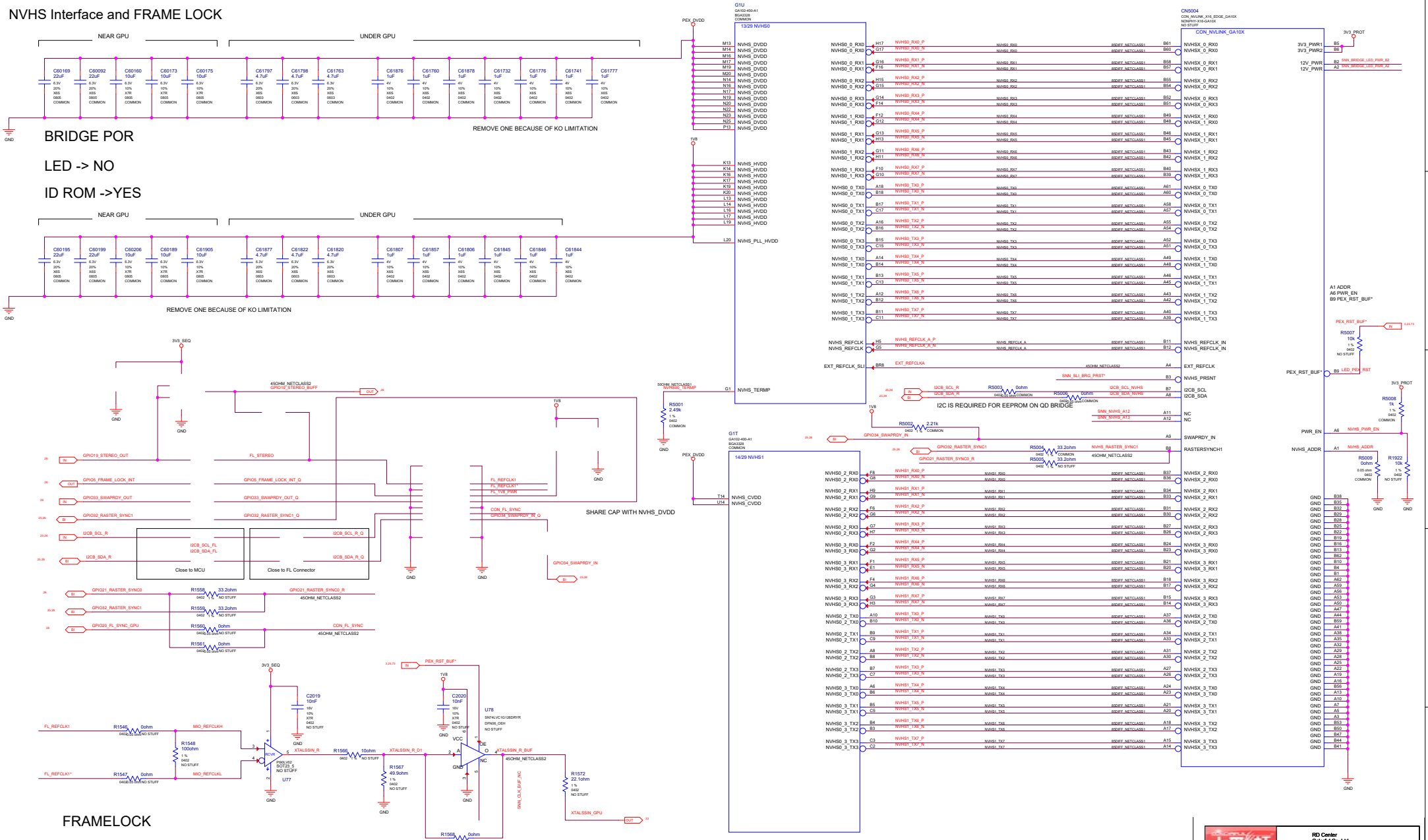
NVHS Interface and FRAME LOCK



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	NVHS x16

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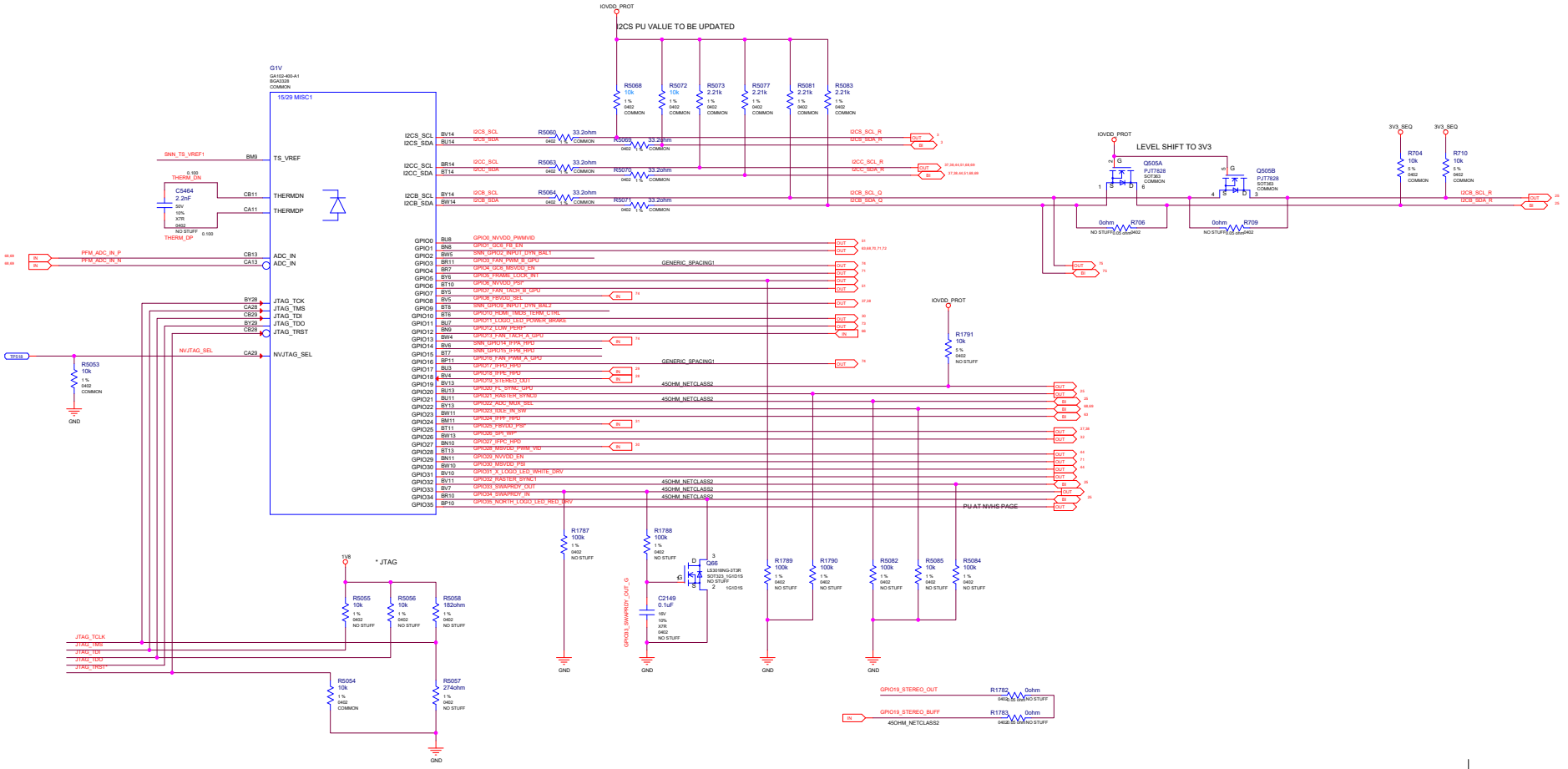
MISC1: Fan, Thermal, JTAG, GPIO, STEREO



ASSEMBLY <ASSEMBLY_DESCRIPTION>

PAGE DETAIL MISC: THERMAL, JTAG, GPIO

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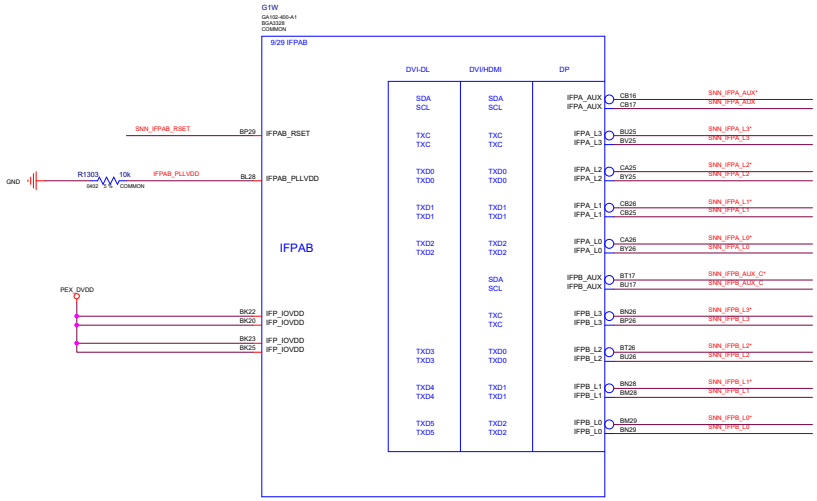
IFPA UNUSED, IFPB UNUSED



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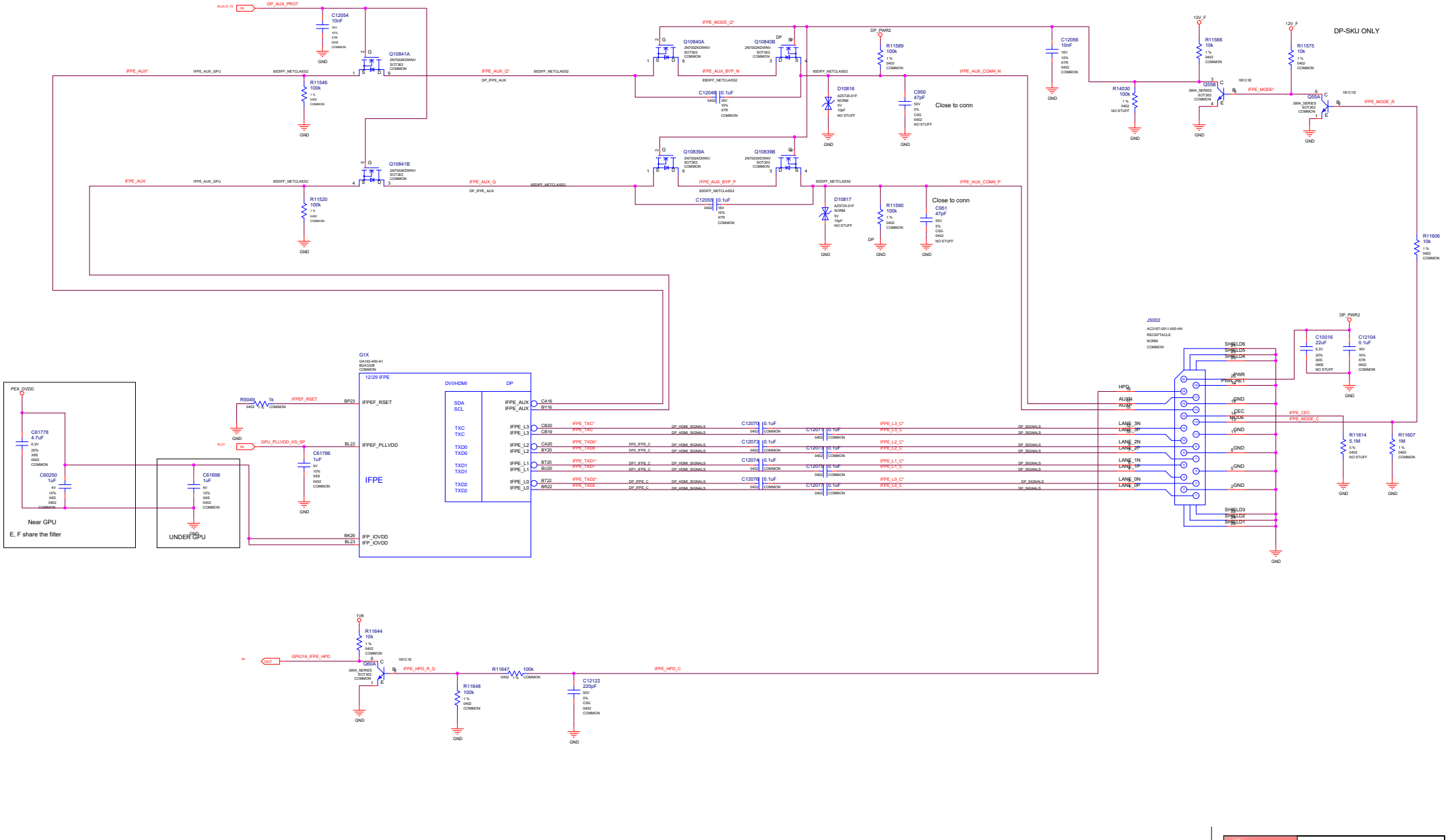
IFPE DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPE DP

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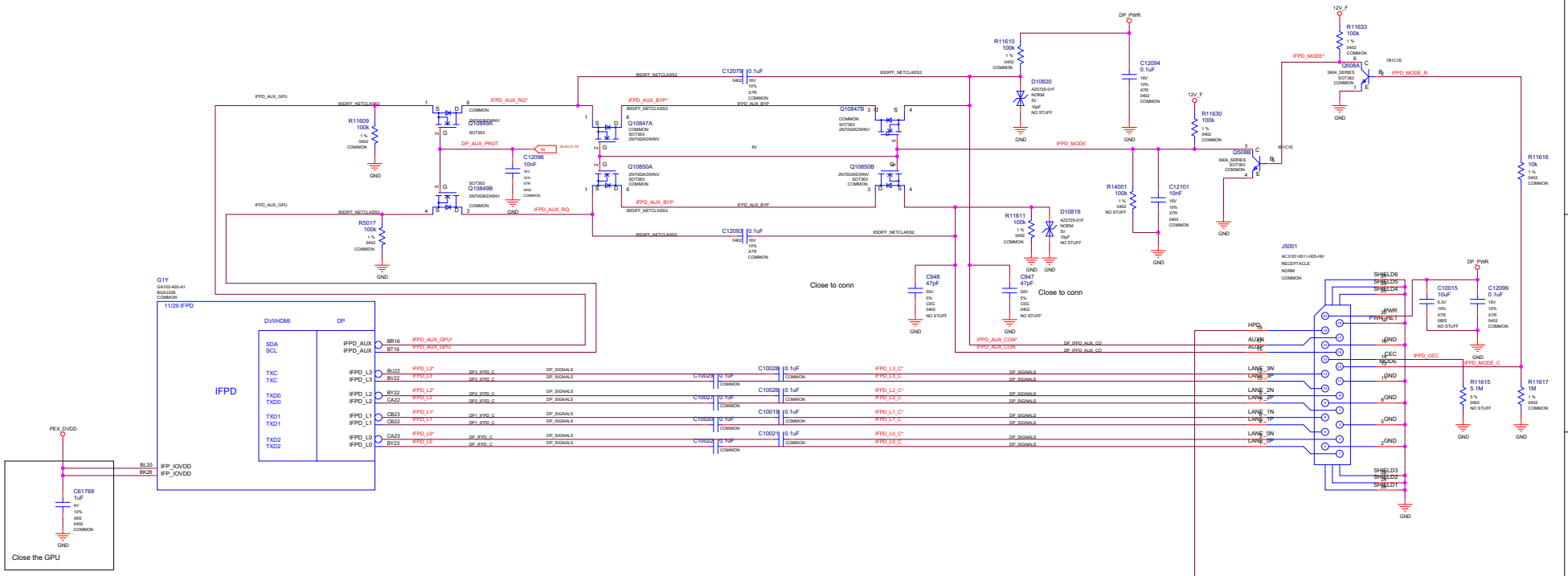
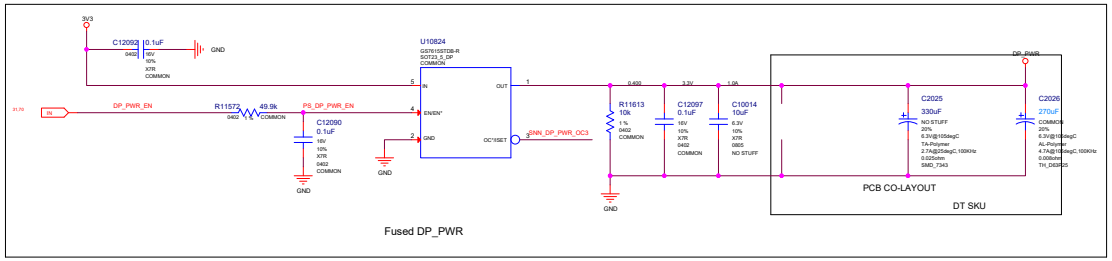
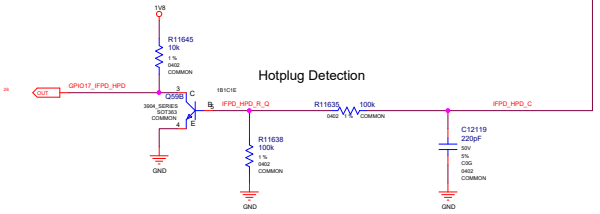
IFPD DP







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPD DP

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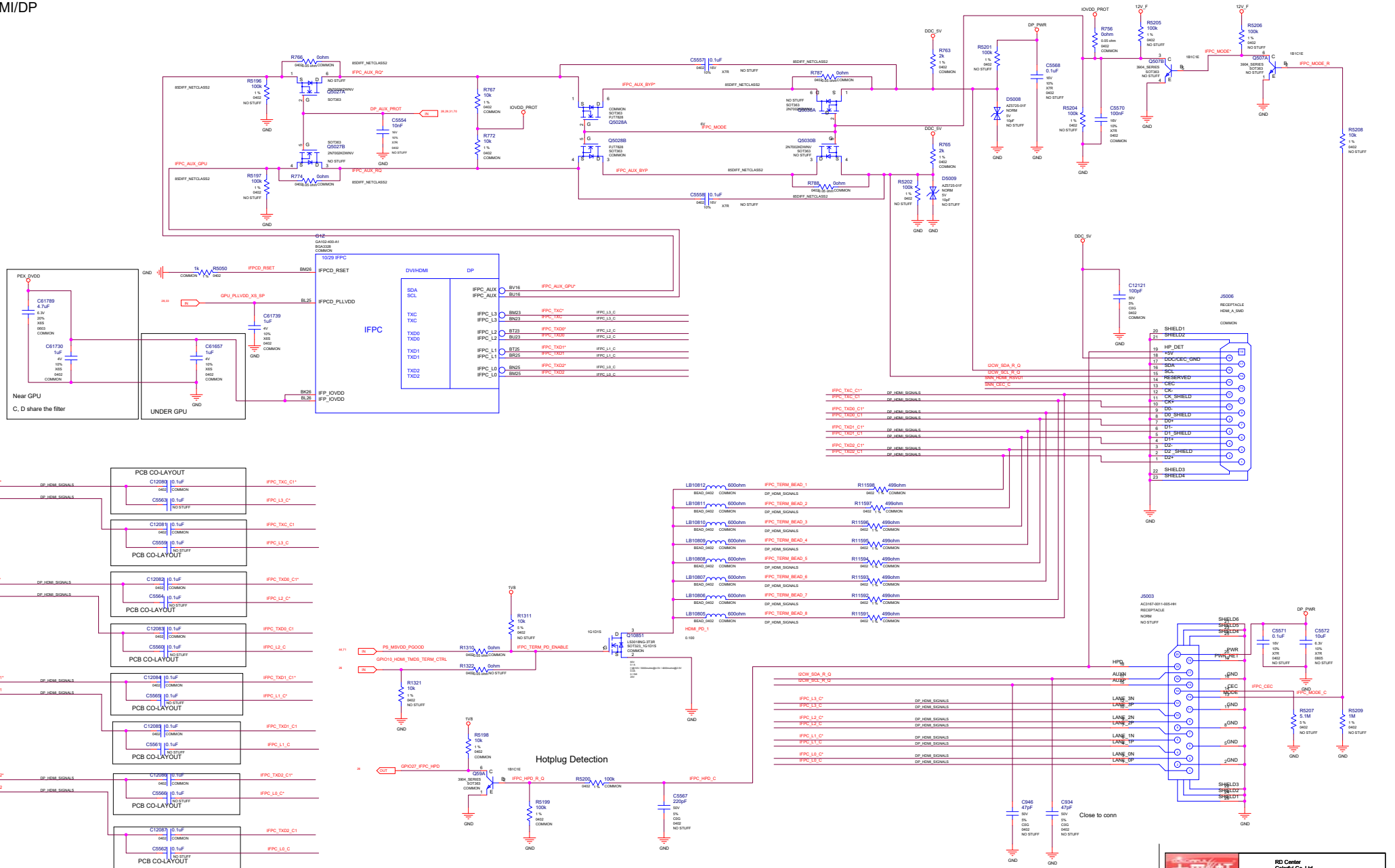
IFPC HDMI/DP



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PAGE DETAIL	IFPC HDMI/DP

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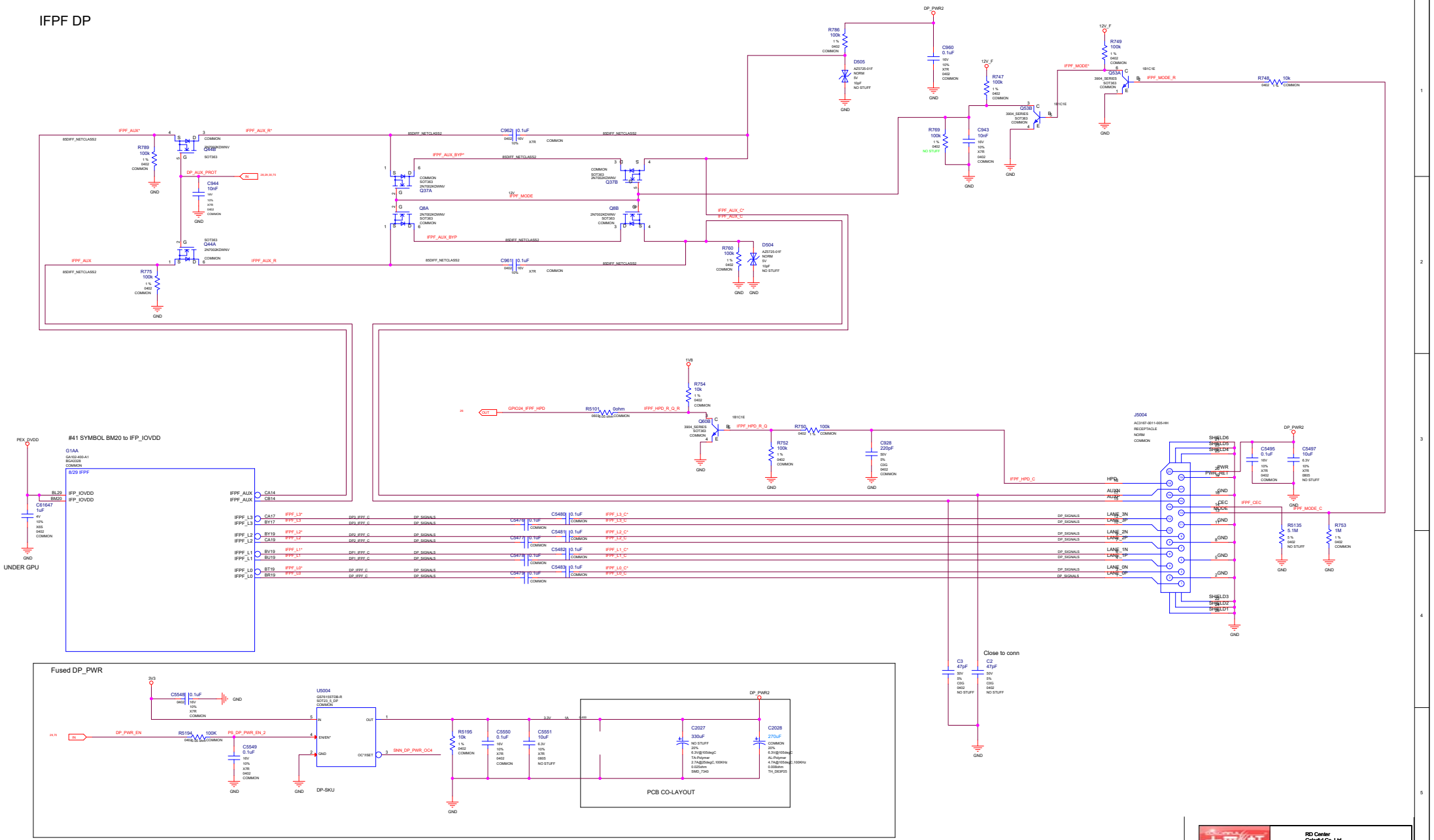
IFPF DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPF DP

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MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb 19Gbps
L	H	L	00010	RAMCFG TBD
H	L	L	00100	RAMCFG TBD
H	L	L	00101	RAMCFG TBD
H	L	H	00101	RAMCFG MICRON 8Gb 21Gbps

DEFAULT

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

DEFAULT

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
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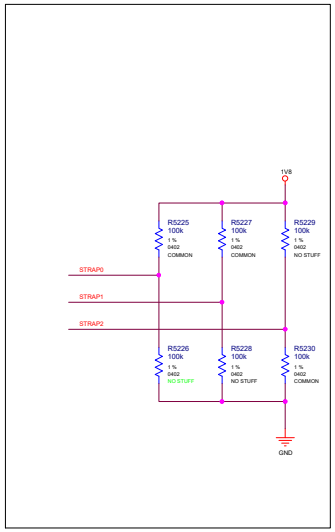
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

GROUP0



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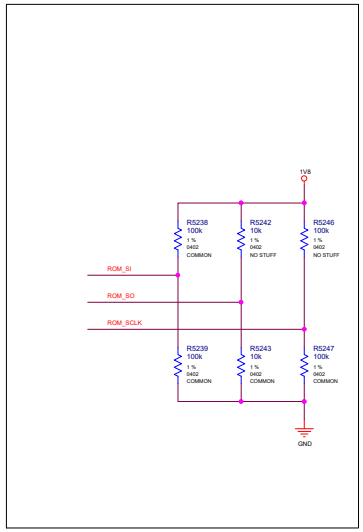

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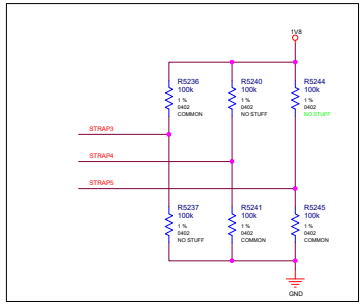

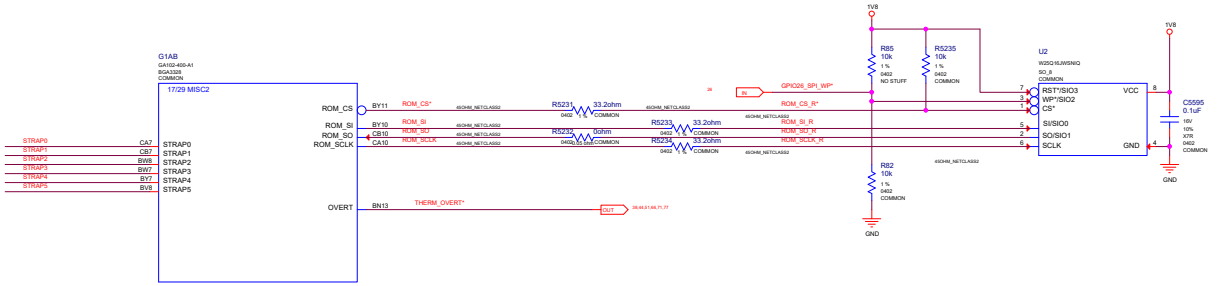

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PAGE DETAIL	MISC. ROM, STRAPS

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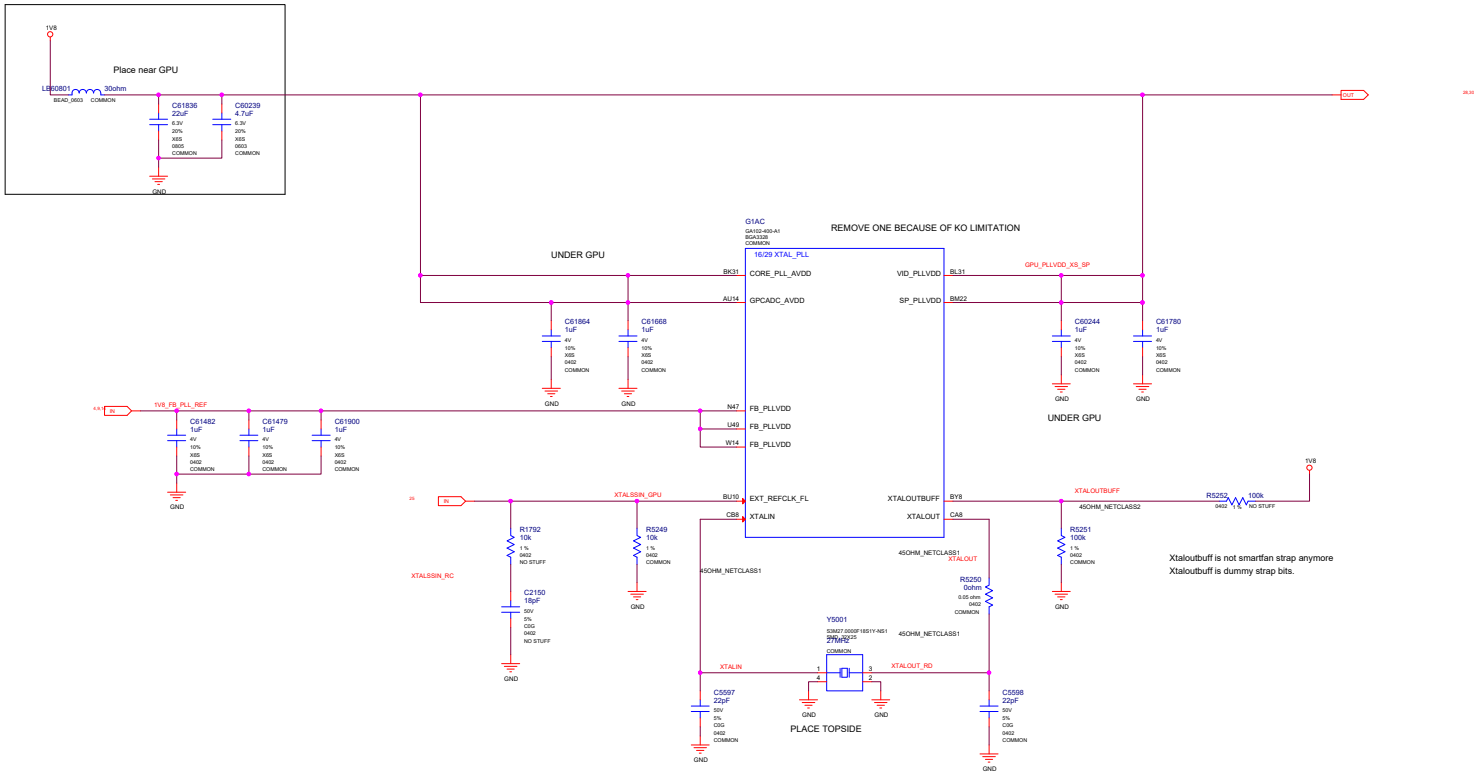
MISC: XTAL. PLL



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PAGE DETAIL	MISC. XTAL. PLL

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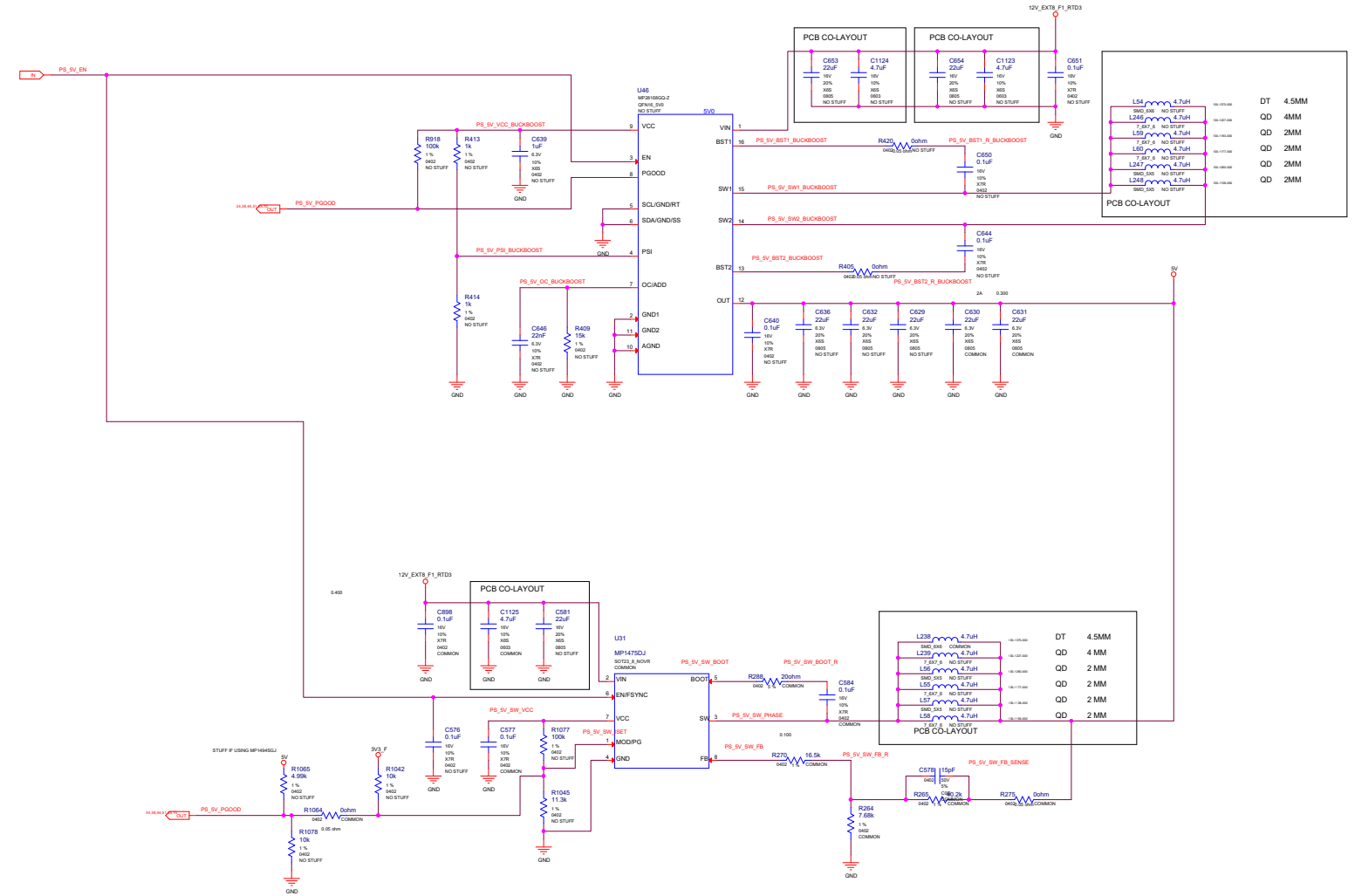
PS: 5V, 5V_BACKUP



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PAGE DETAIL	PS: 5V

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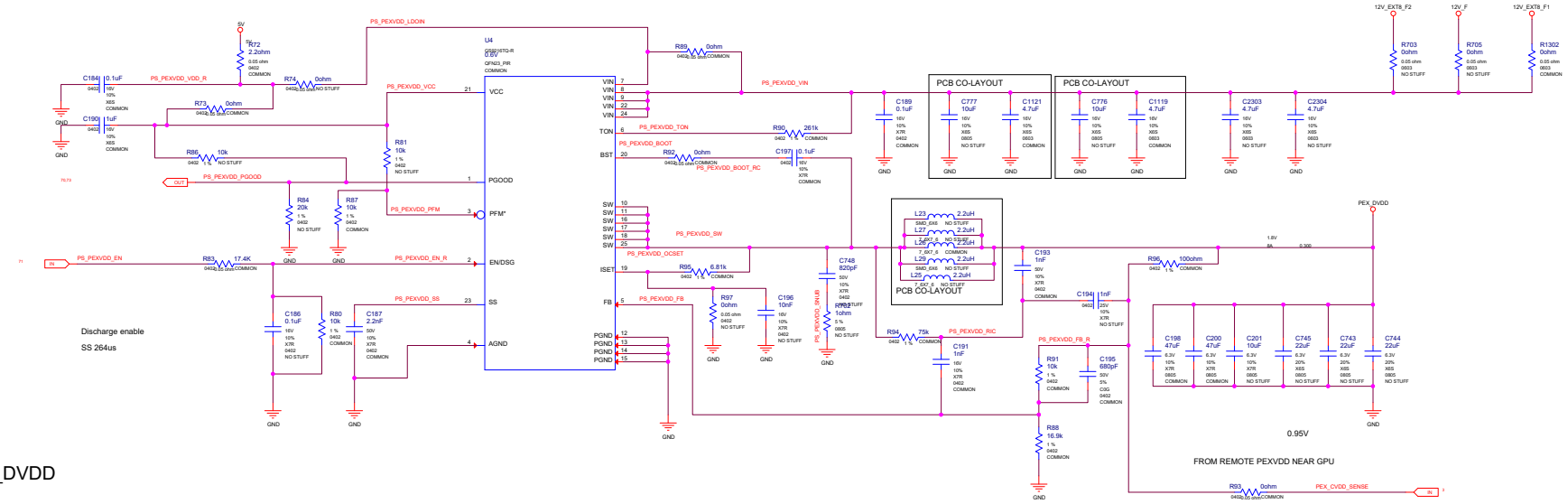
PS: PEX_DVDD 1V8 Rail



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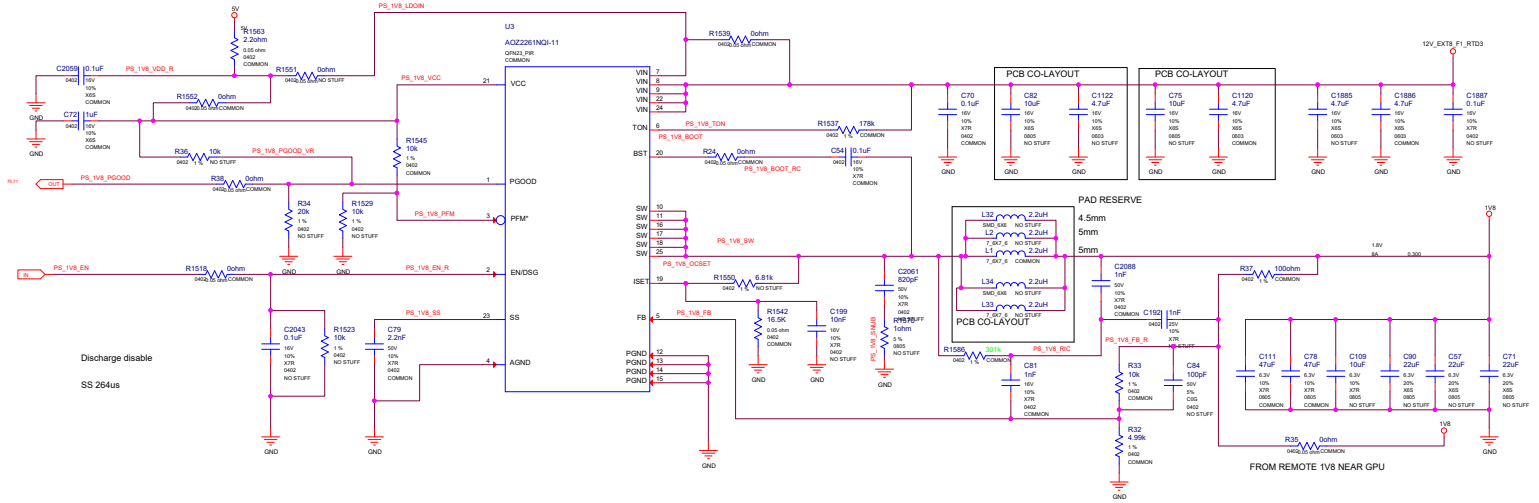

1V8

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PAGE DETAIL	PS: PEX_DVDD and 1V8

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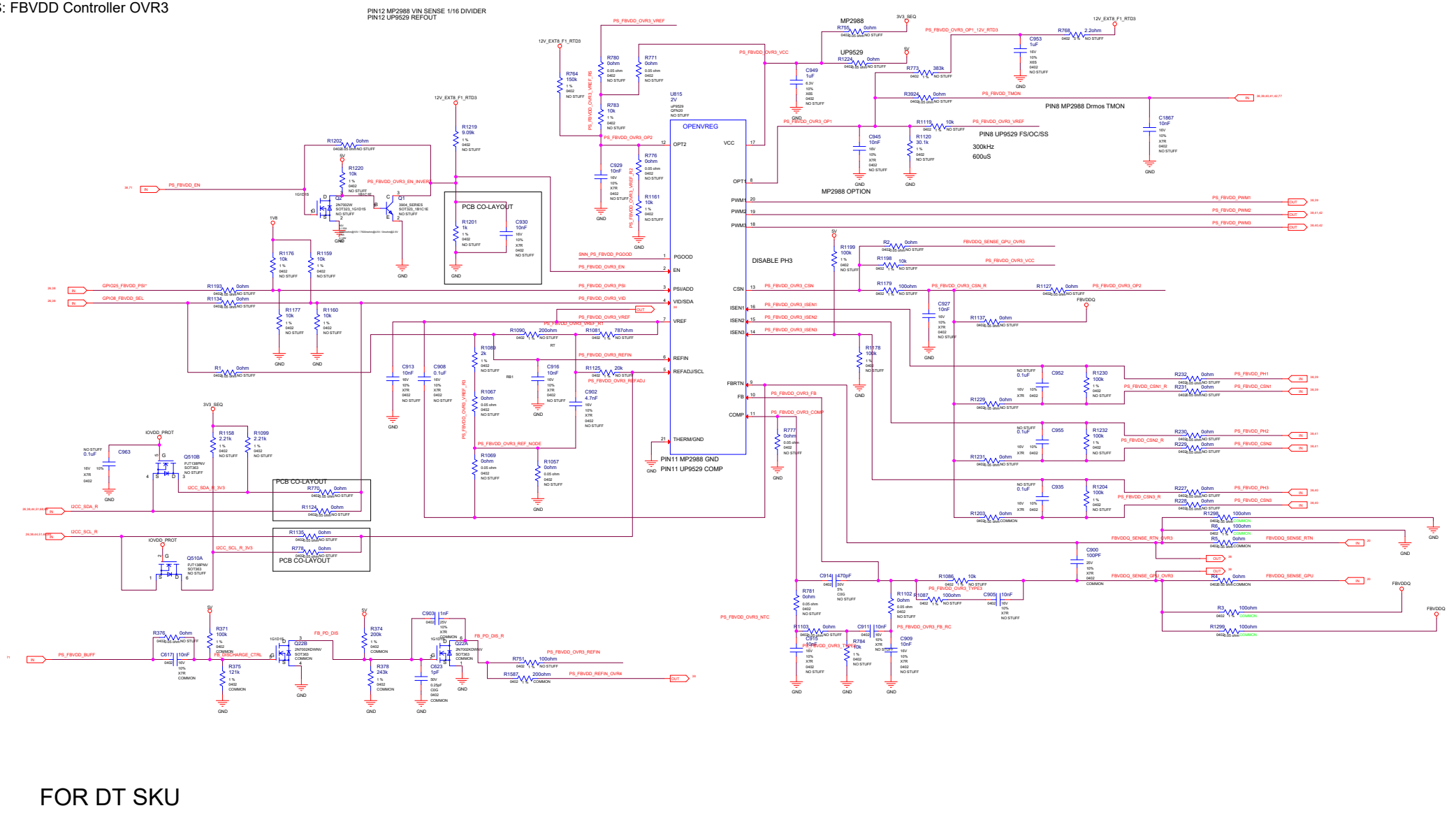
PS: FBVDD Controller OVR3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PIN12 UP9529 REFOUT
MP2988
UP9529
OPENVREG
MP2988 OPTION
PIN8 MP2988 Drmos TMON
PIN8 UP9529 FS/OC/SS
300kHz
600uS
DISABLE PH3
PIN11 MP2988 GND
PIN11 UP9529 COMP
PCB CO-LAYOUT
PCB CO-LAYOUT
PCB CO-LAYOUT
PS_FBVDD_EN
PS_FBVDD_OVR3_EN_INVERT
PS_FBVDD_OVR3_VREF
PS_FBVDD_OVR3_OP1
PS_FBVDD_OVR3_OP2
PS_FBVDD_OVR3_VCC
PS_FBVDD_TMON
PS_FBVDD_PWM1
PS_FBVDD_PWM2
PS_FBVDD_PWM3
PS_FBVDD_OVR3_PSI
PS_FBVDD_OVR3_VID
PS_FBVDD_OVR3_REFIN
PS_FBVDD_OVR3_REFADJ
PS_FBVDD_OVR3_FB
PS_FBVDD_OVR3_COMP
PS_FBVDD_OVR3_CSN
PS_FBVDD_OVR3_ISEN1
PS_FBVDD_OVR3_ISEN2
PS_FBVDD_OVR3_ISEN3
PS_FBVDD_OVR3_NTC
PS_FBVDD_OVR3_FB_RC
PS_FBVDD_OVR3_REFIN_OVR4
PS_FBVDD_BUFF
PS_DISCHARGE_CTRL
FB_PD_DIS
FB_PD_DIS_R
I2CC_SDA_R
I2CC_SCL_R
I2CC_SDA_R_3V3
I2CC_SCL_R_3V3
IOVDD_PROT
GPIO25_FBVDD_PSI*
GPIO8_FBVDD_SEL
PS_FBVDD_OVR3_CSN_R
PS_FBVDD_OVR3_ISEN1_R
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PS_FBVDD_OVR3_OP2
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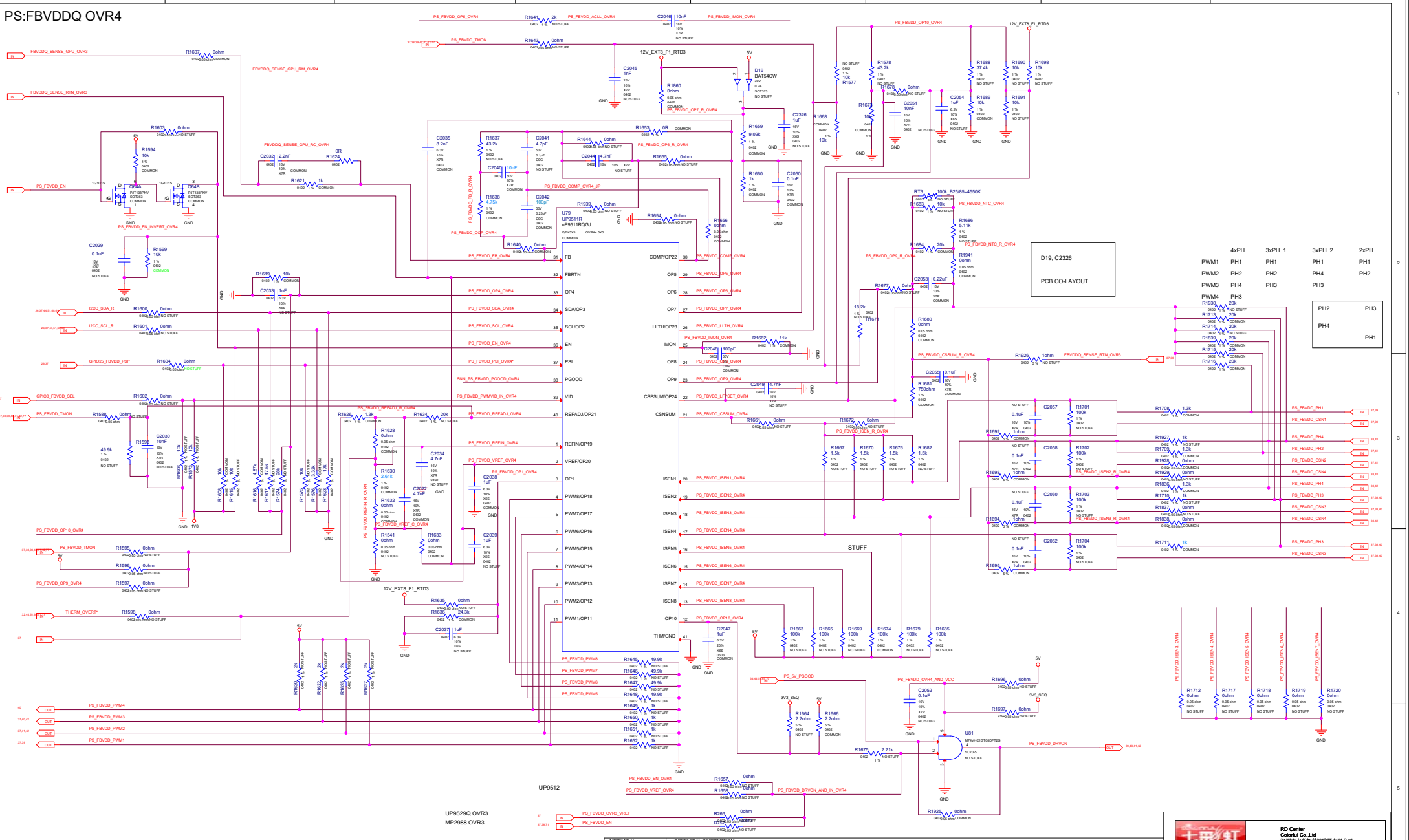
PS:FBVDDQ OVR4



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PAGE DETAIL PS: FBVDDQ OVR4

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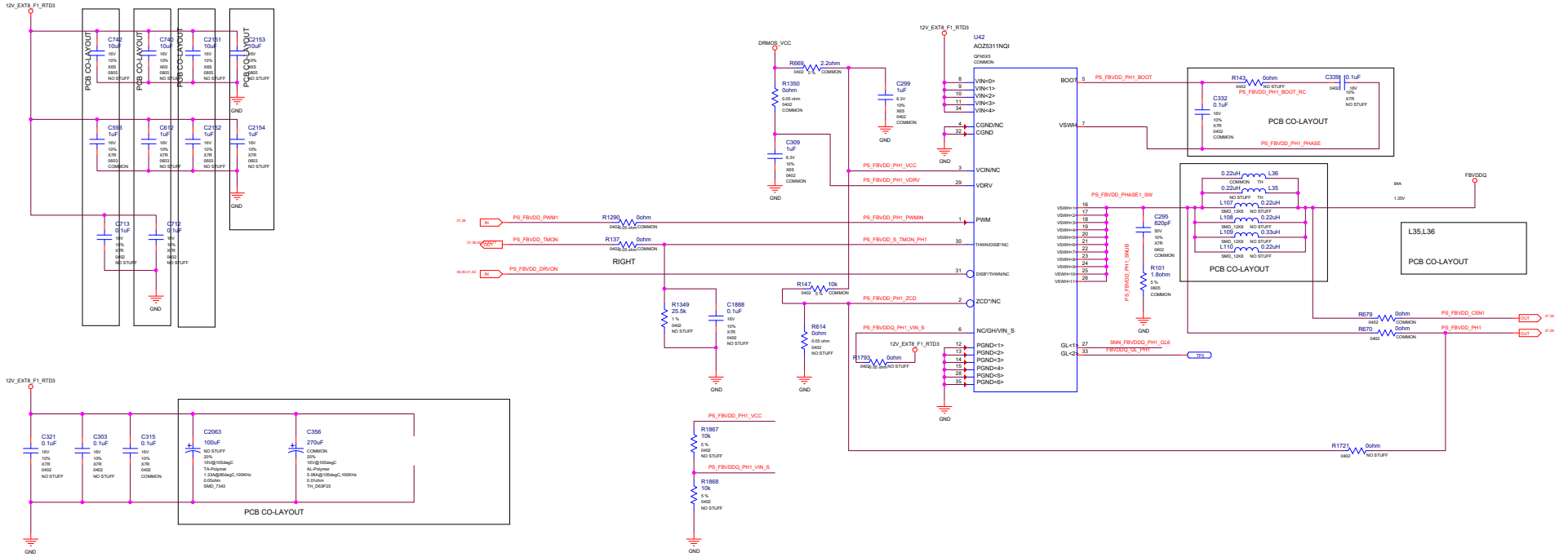
PS: FBVDD PH1



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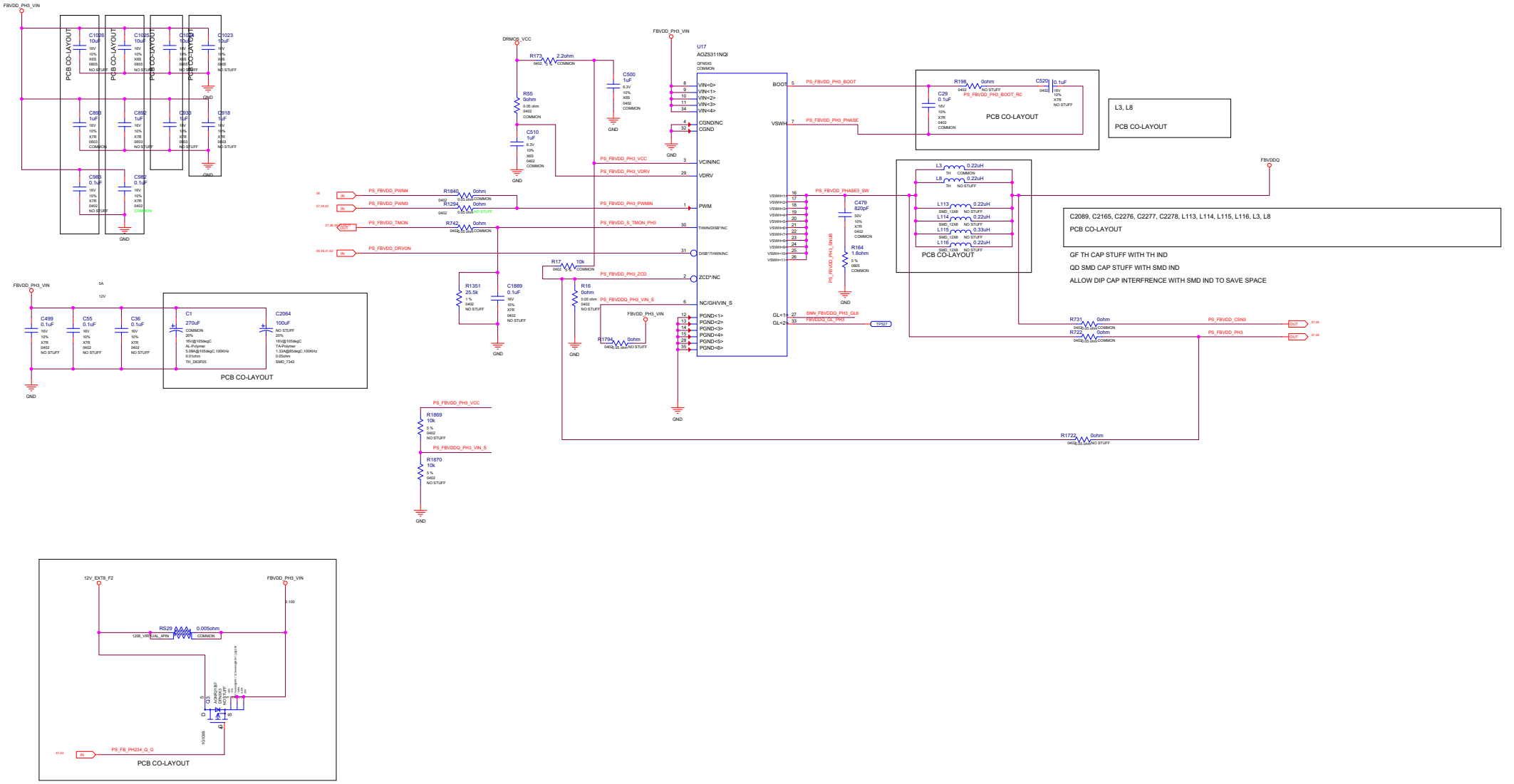
PS: FBVDD PH3



FBVDD PH3 INPUT ANTI-BACKDRIVE

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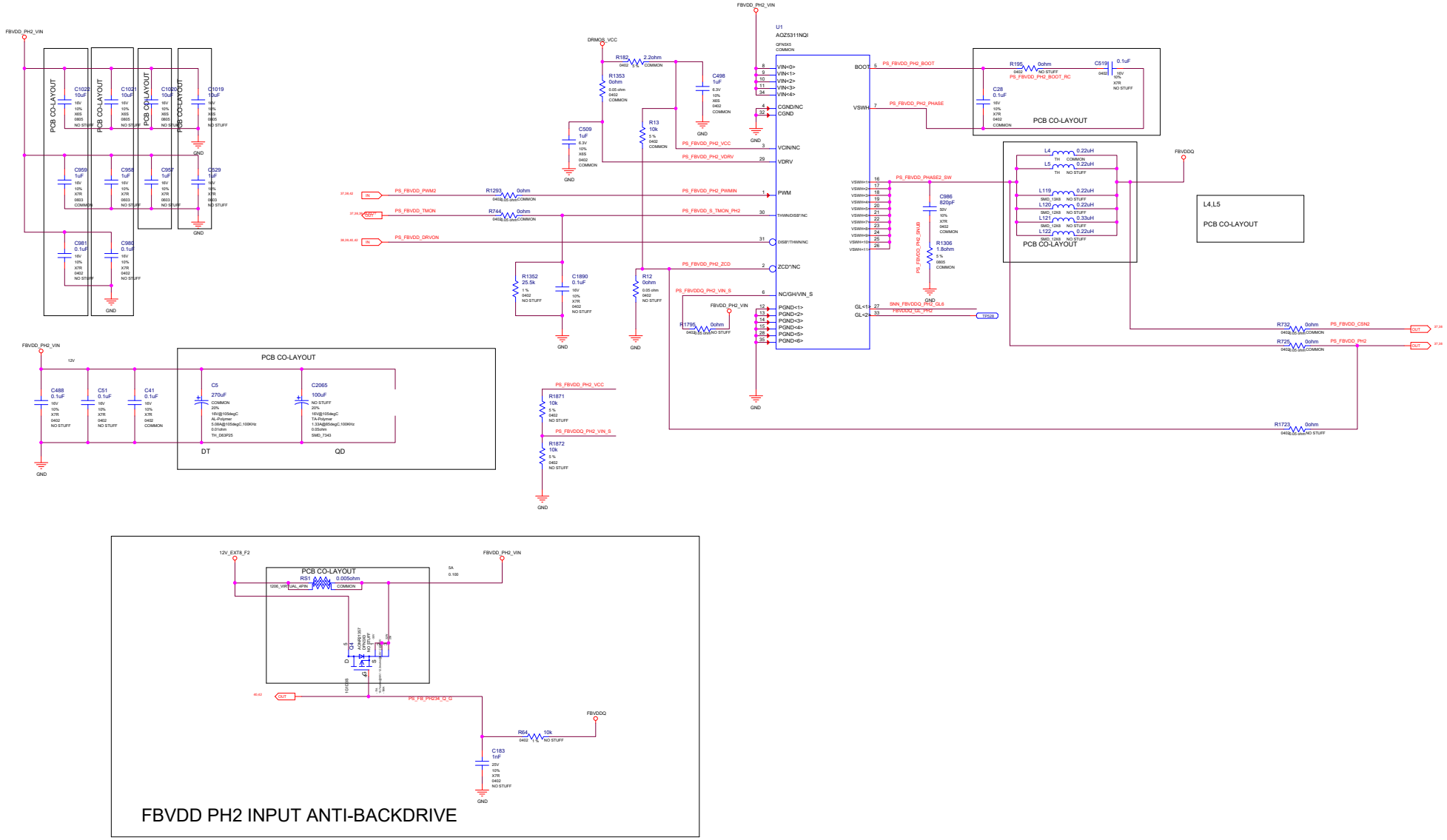
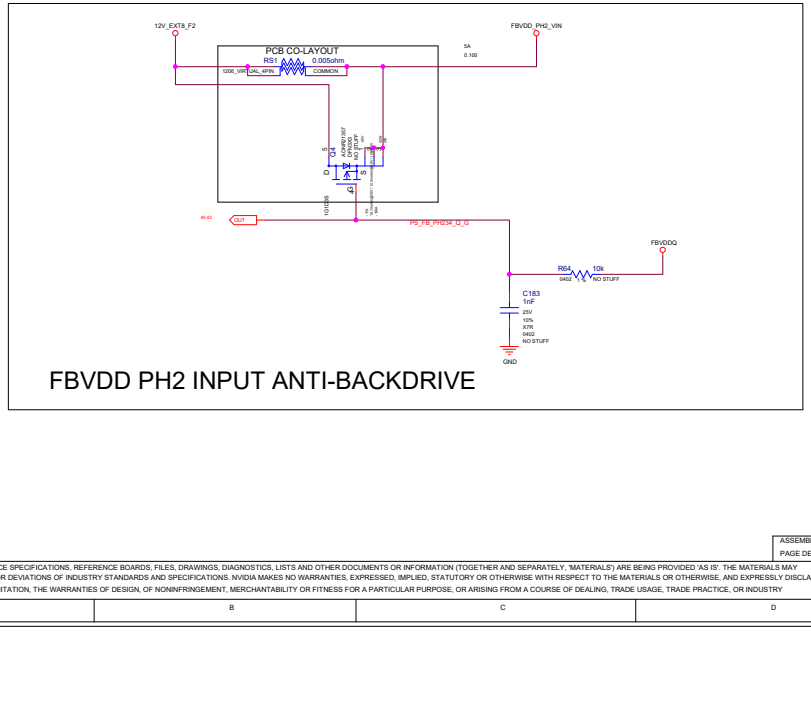
PS: FBVDD PH2





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PAGE DETAIL	PS: FBVDD PH2

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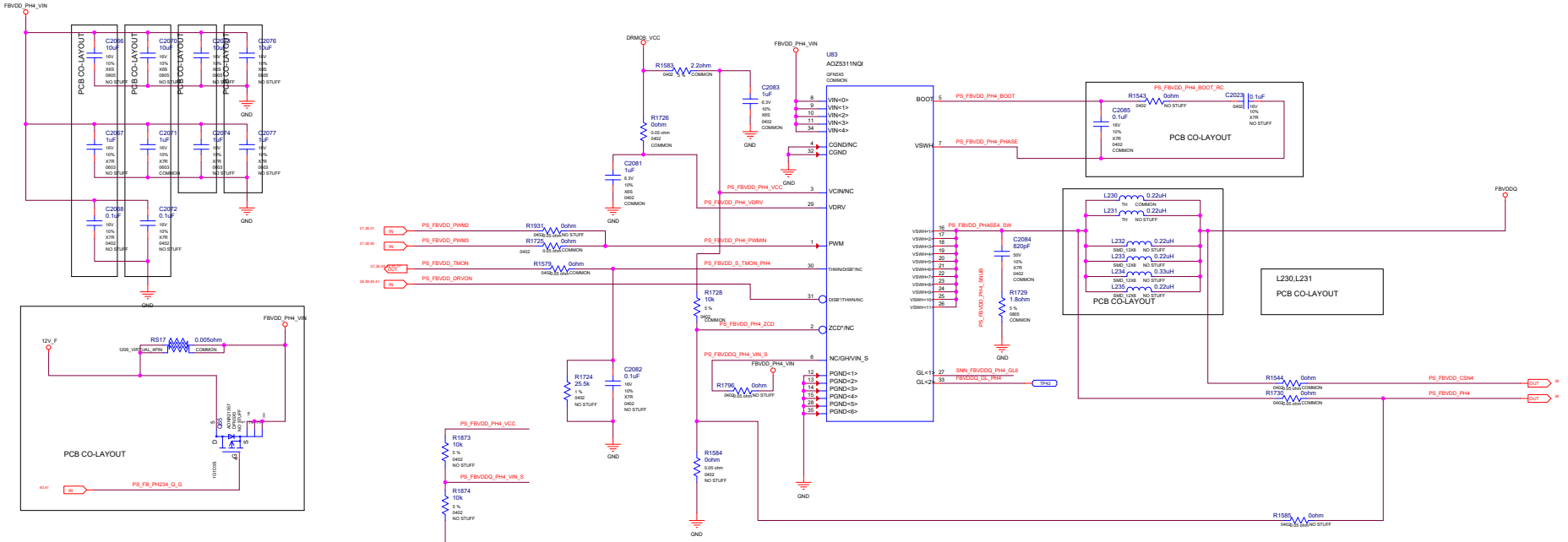
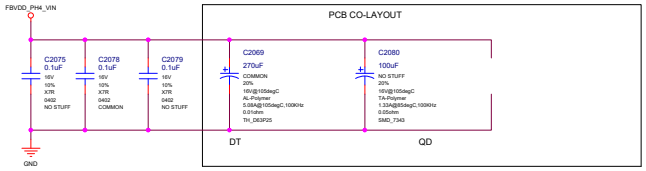
PS: FBVDD PH4



FBVDD PH3 INPUT ANTI-BACKDRIVE



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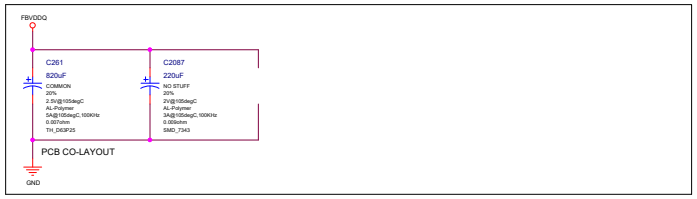
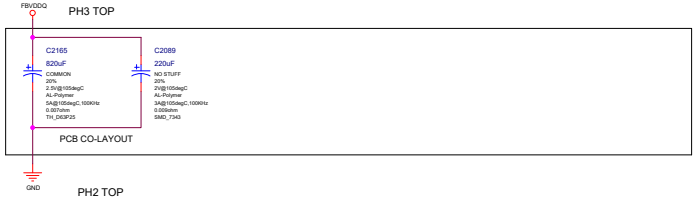
PS: FBVDD OUTPUT CAP

REFER TO PCB FOR BOM STUFFING

PH1 TOP



PH3 TOP



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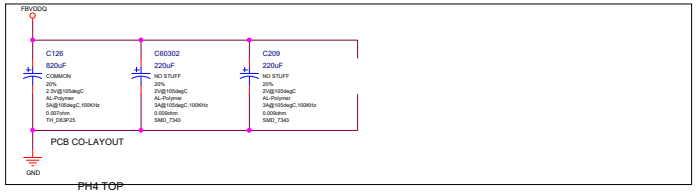

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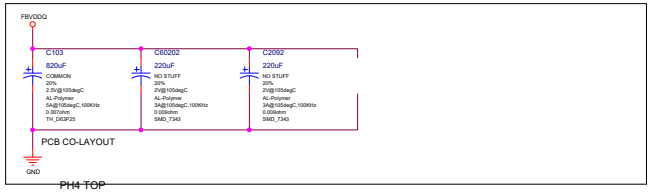

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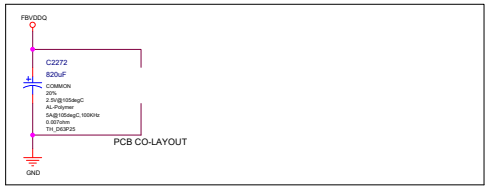

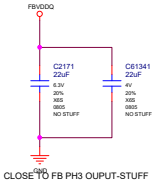

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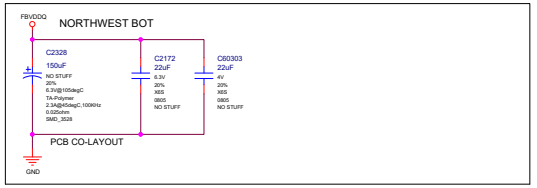

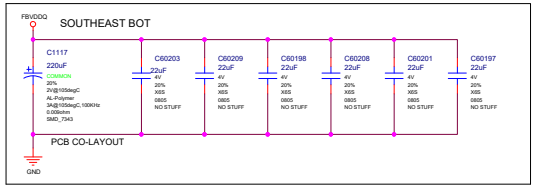

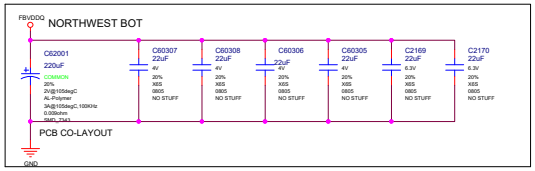

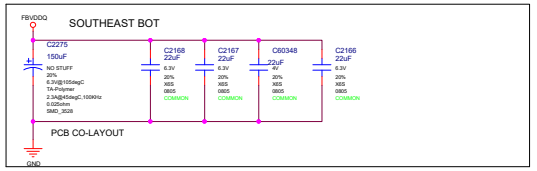

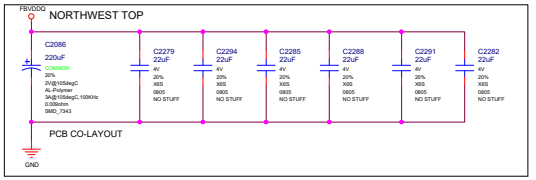

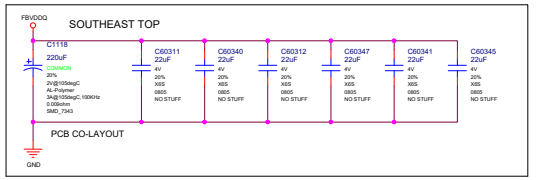

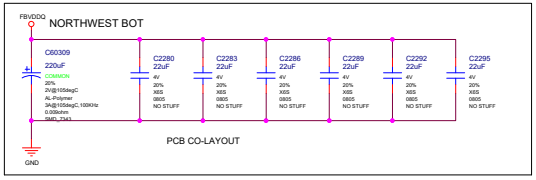

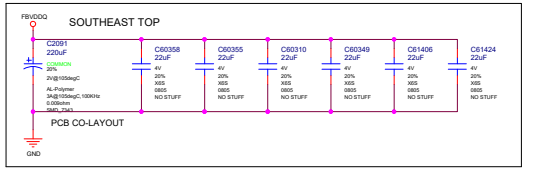

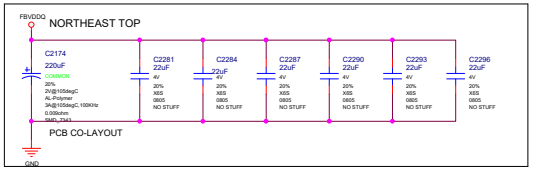

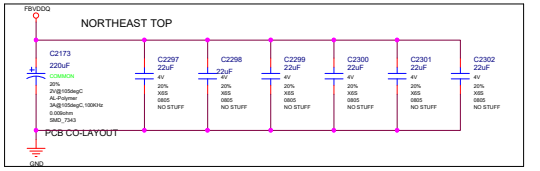

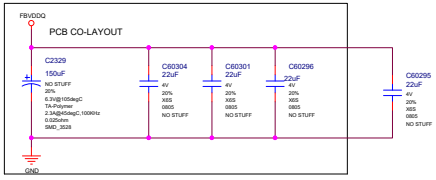

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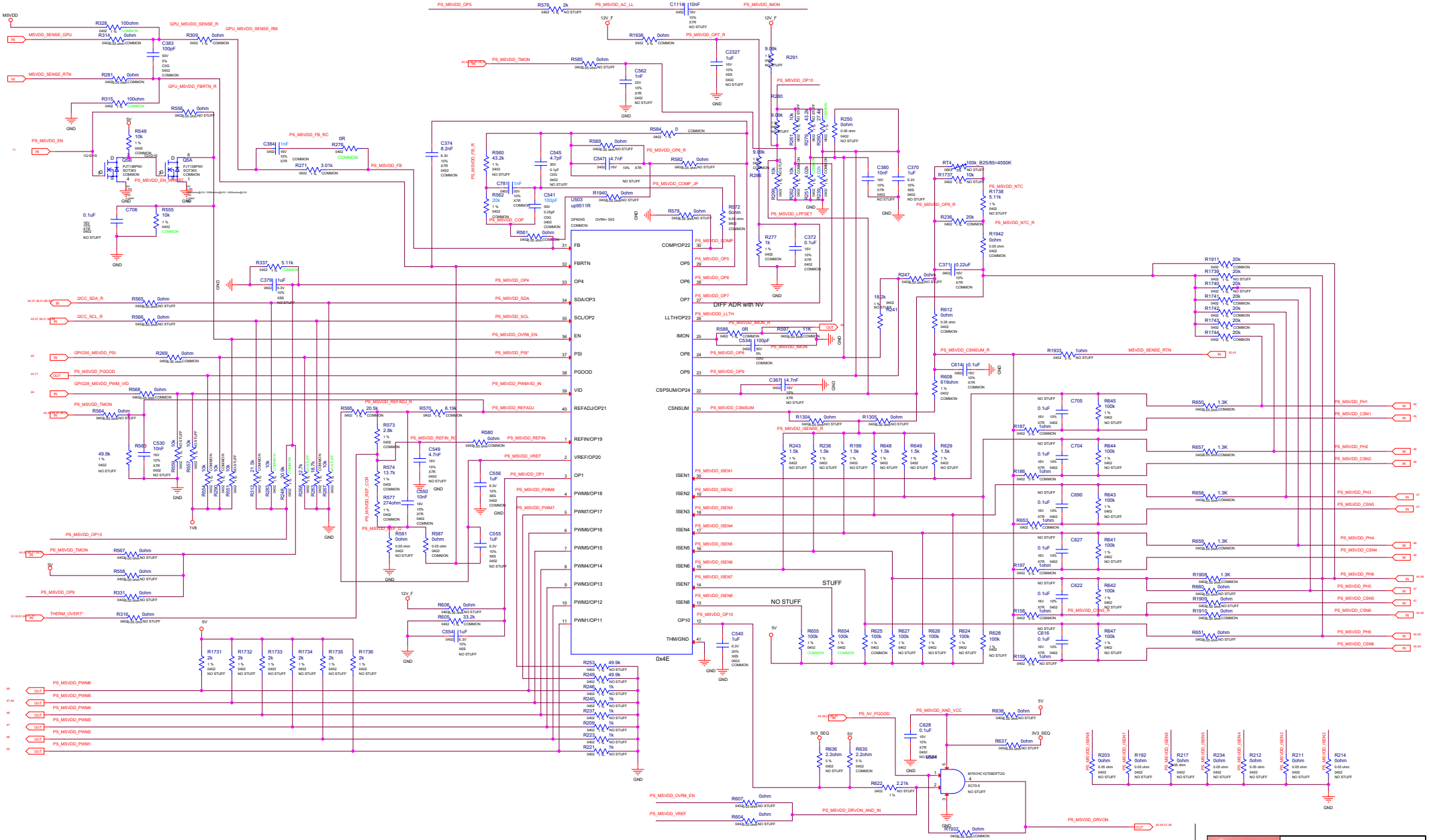
PS: MSVDD



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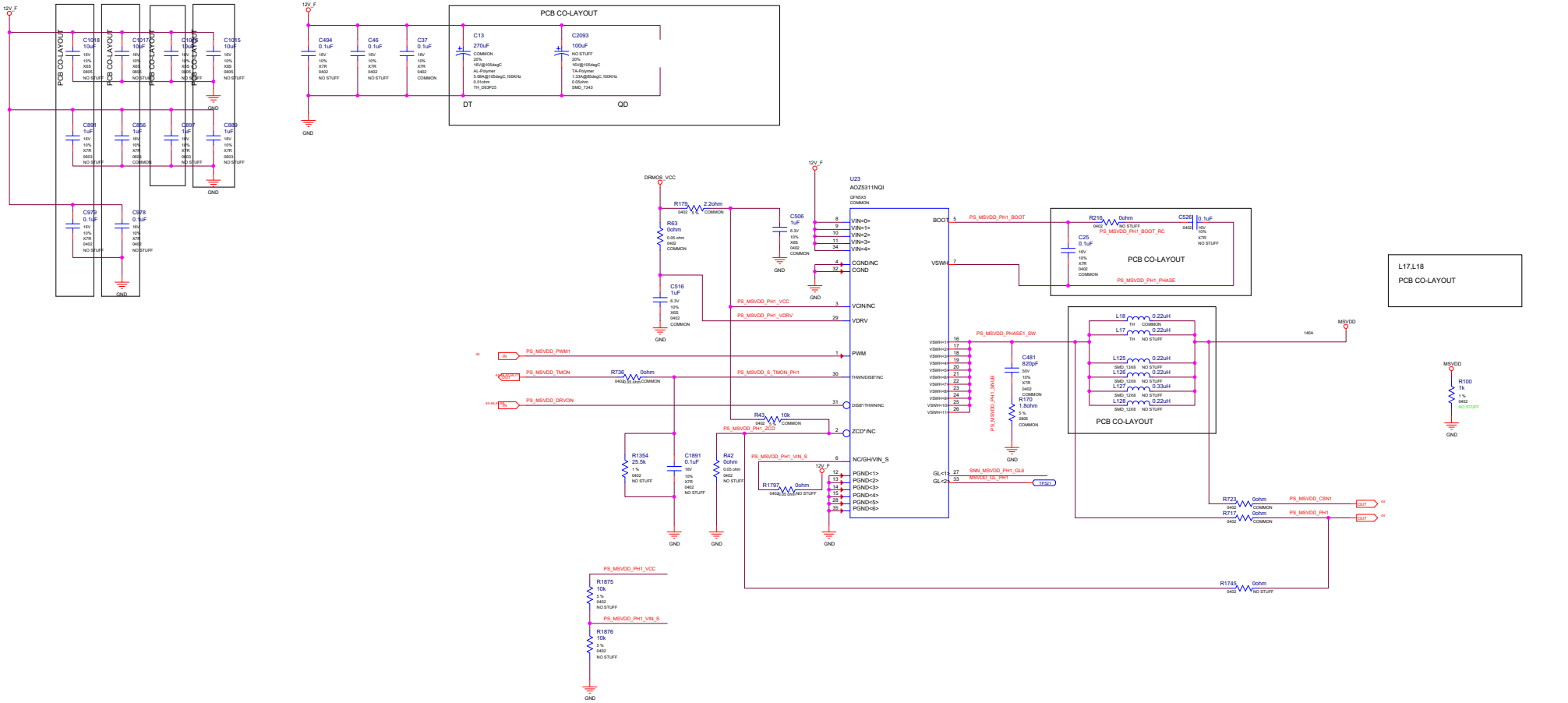
PS: MSVDD Phase 1



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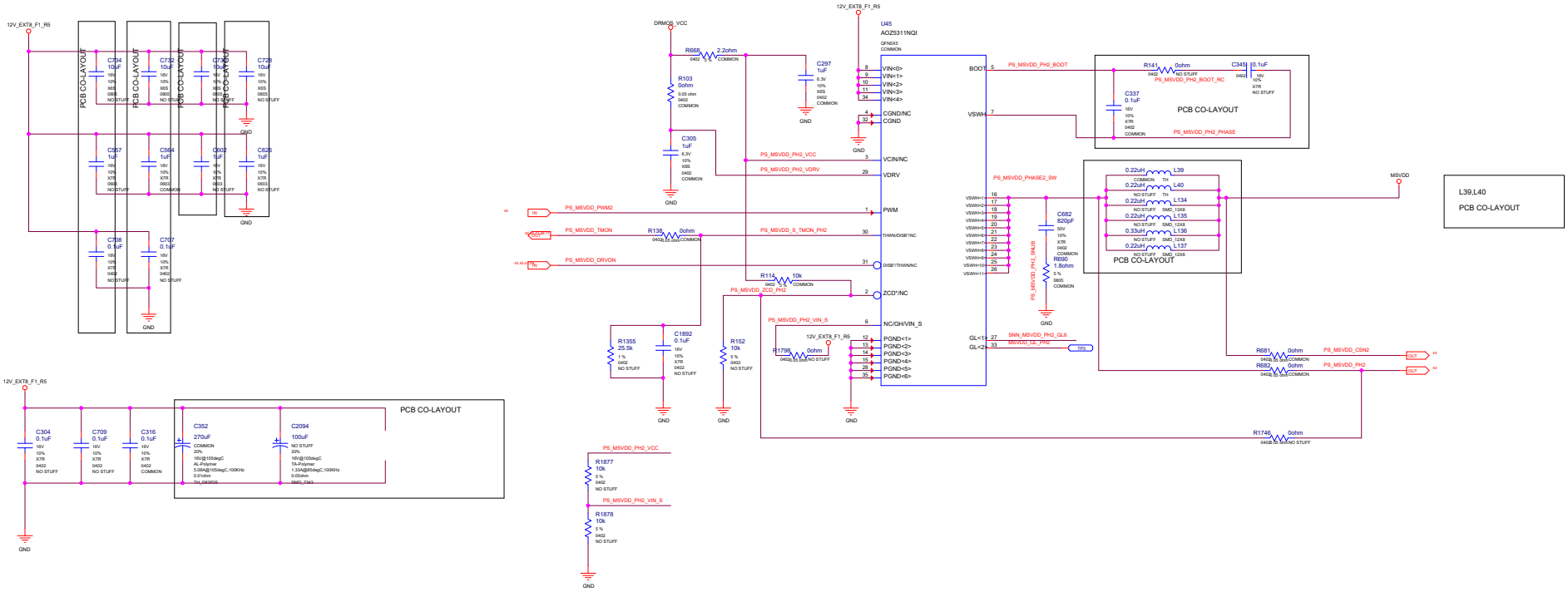
PS: MSVDD PH 2



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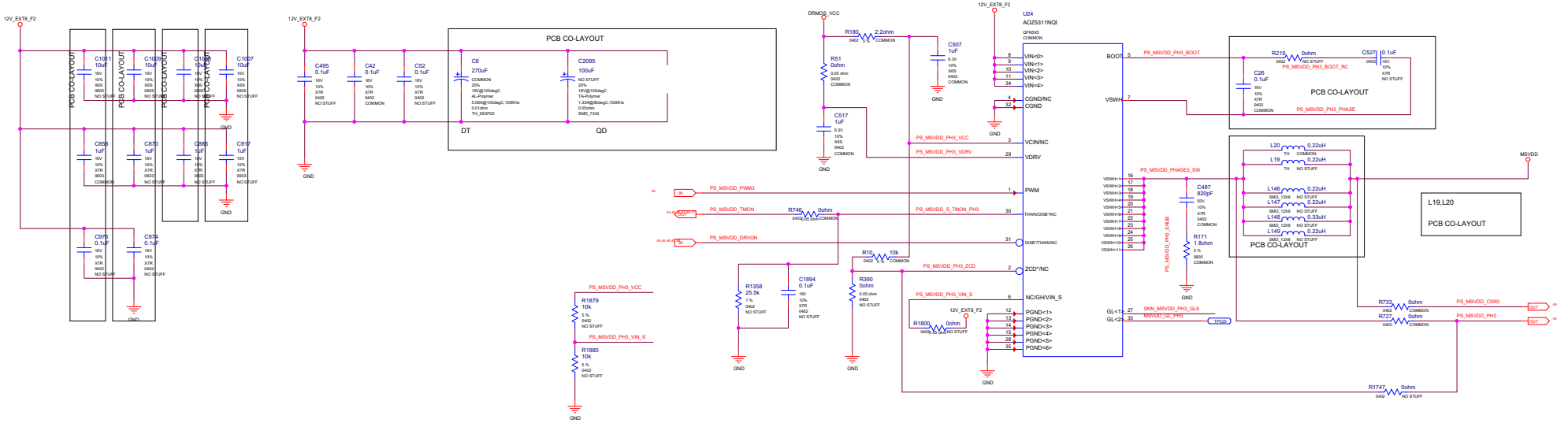

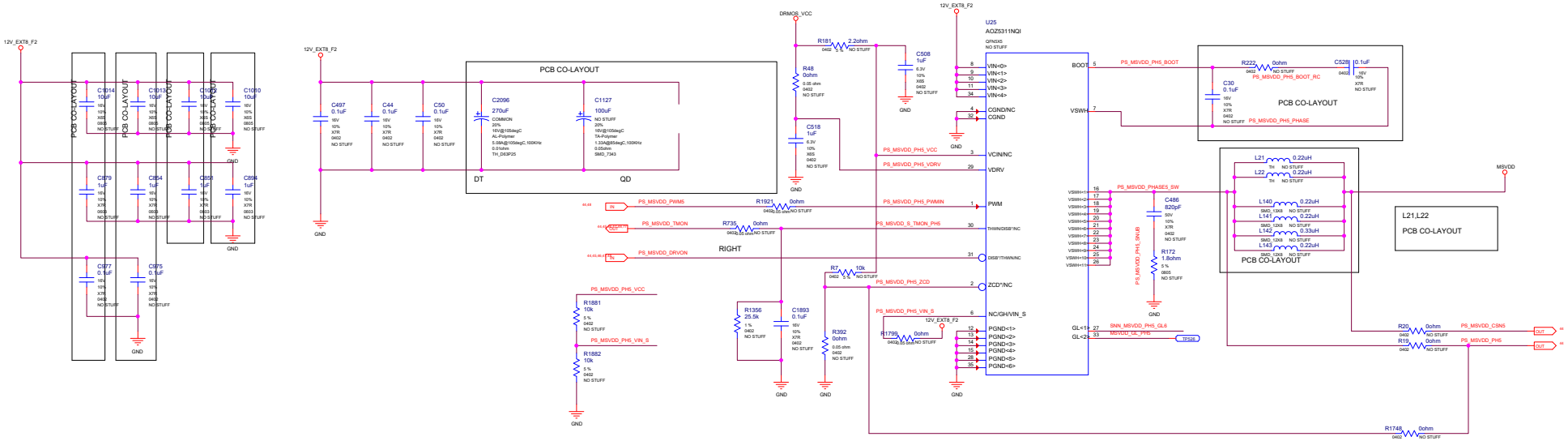

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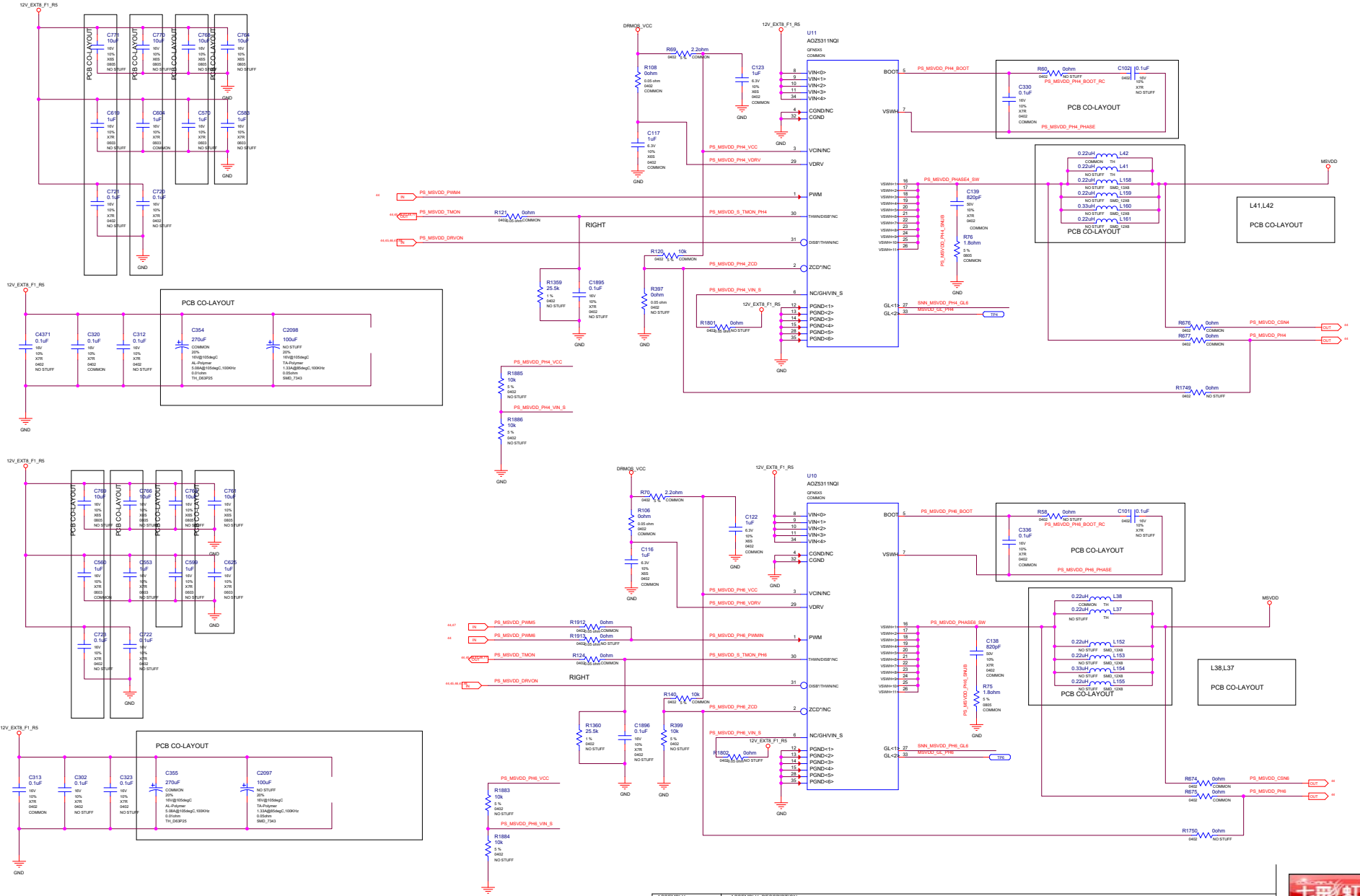

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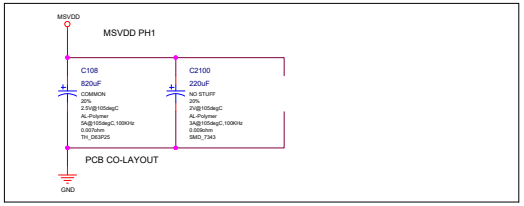
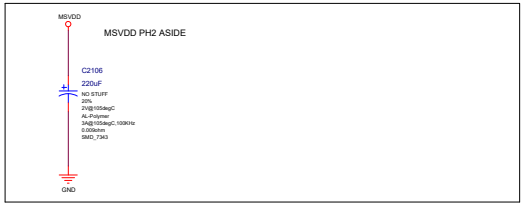
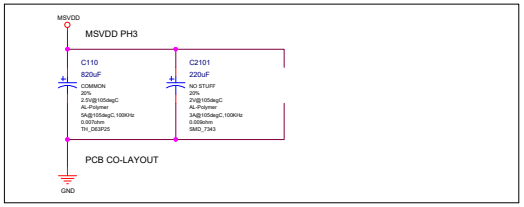
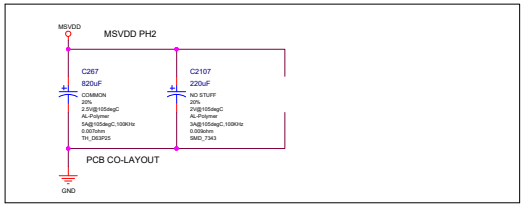
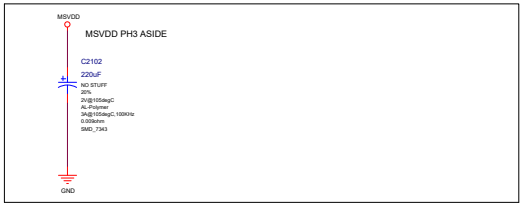
REFER TO PCB FOR BOM STUFFING

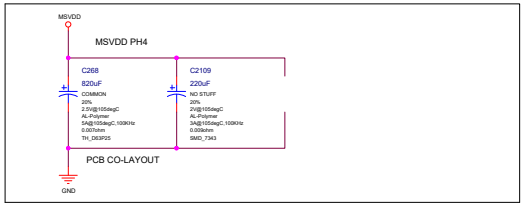


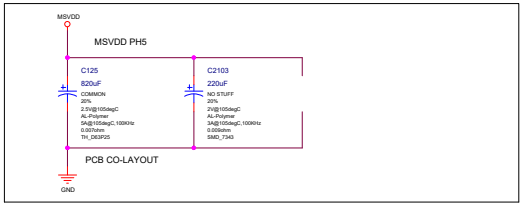


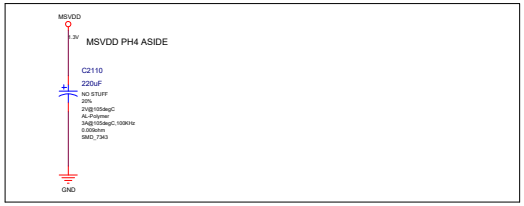


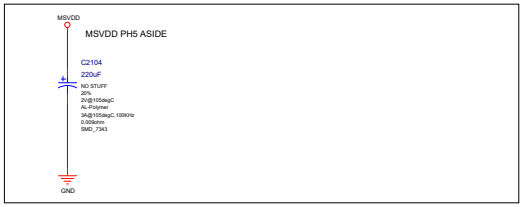


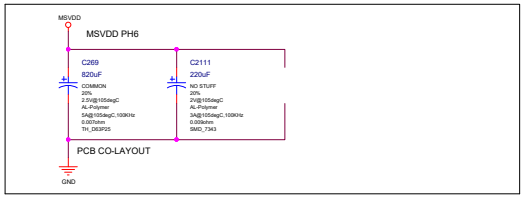


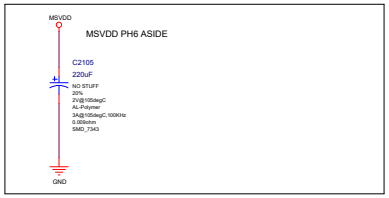












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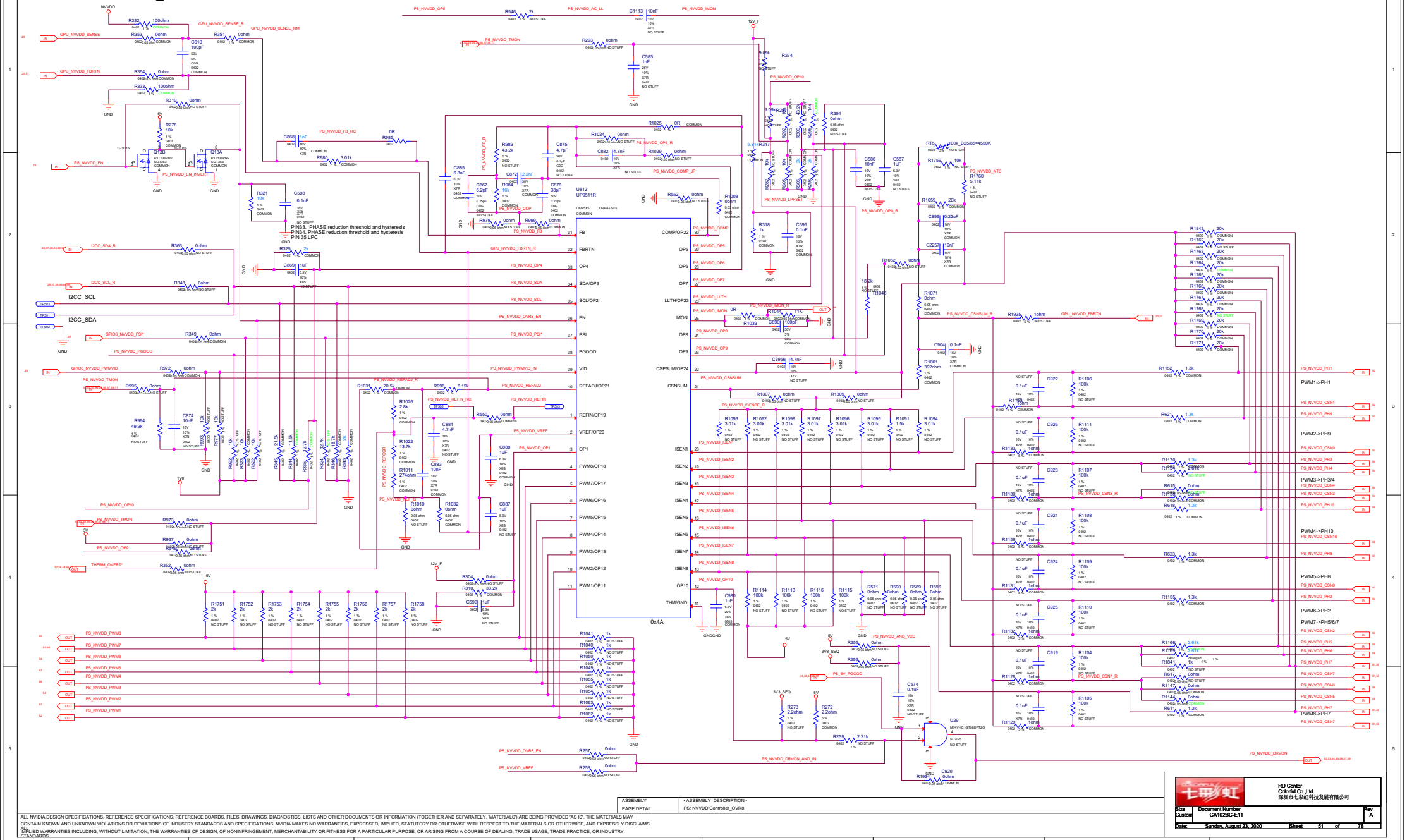
PS: NVVDD Controller_OVR8



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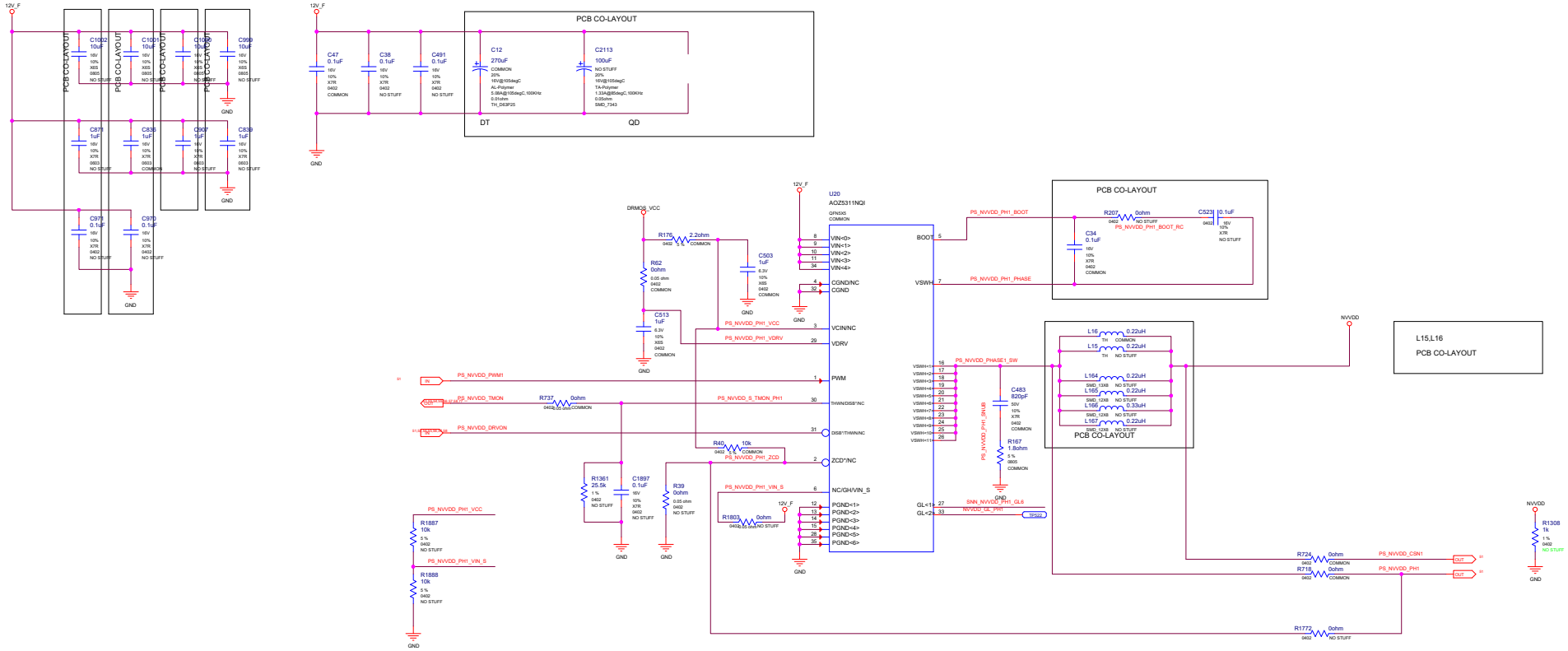
PS: NVVDD Phase 1



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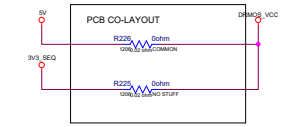

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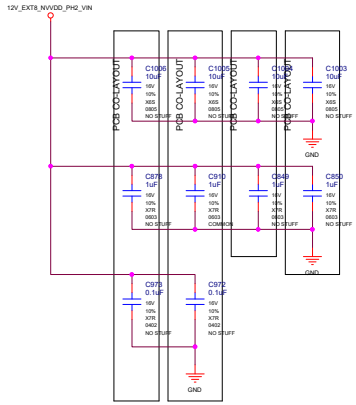

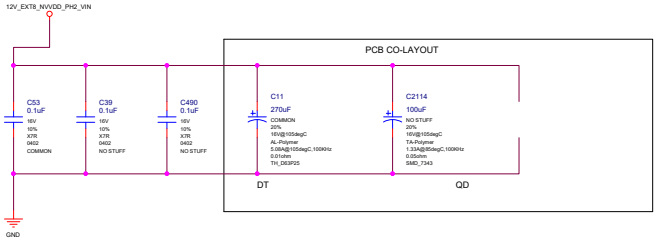

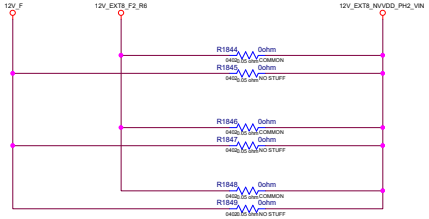

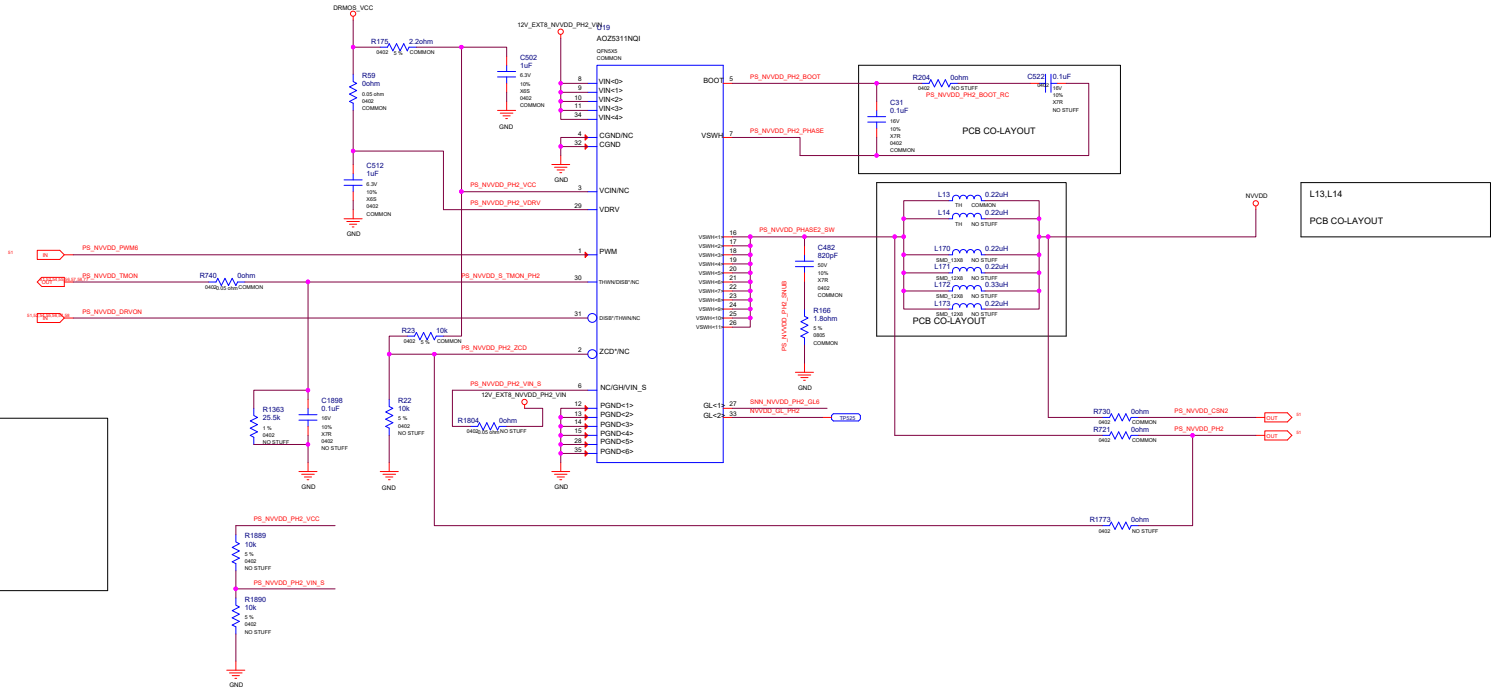

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PAGE DETAIL	PS: NVVDD PH2 (PWM6)

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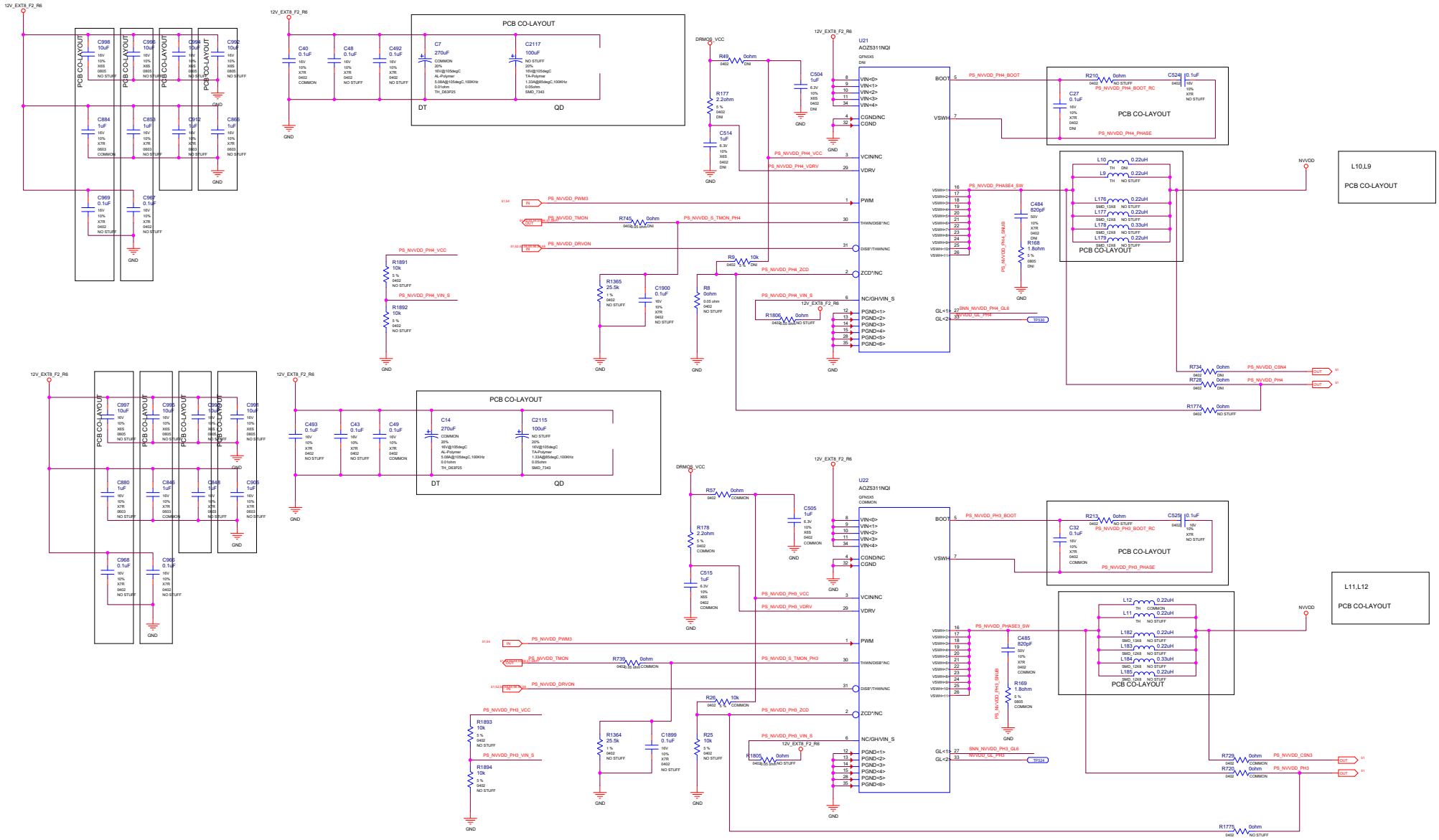
PS: NVVDD Phase 3 (PWM3), PHASE4 (PWM3)



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PAGE DETAIL	PS: NVVDD PH3 (PWM3) and PH4 (PWM3)

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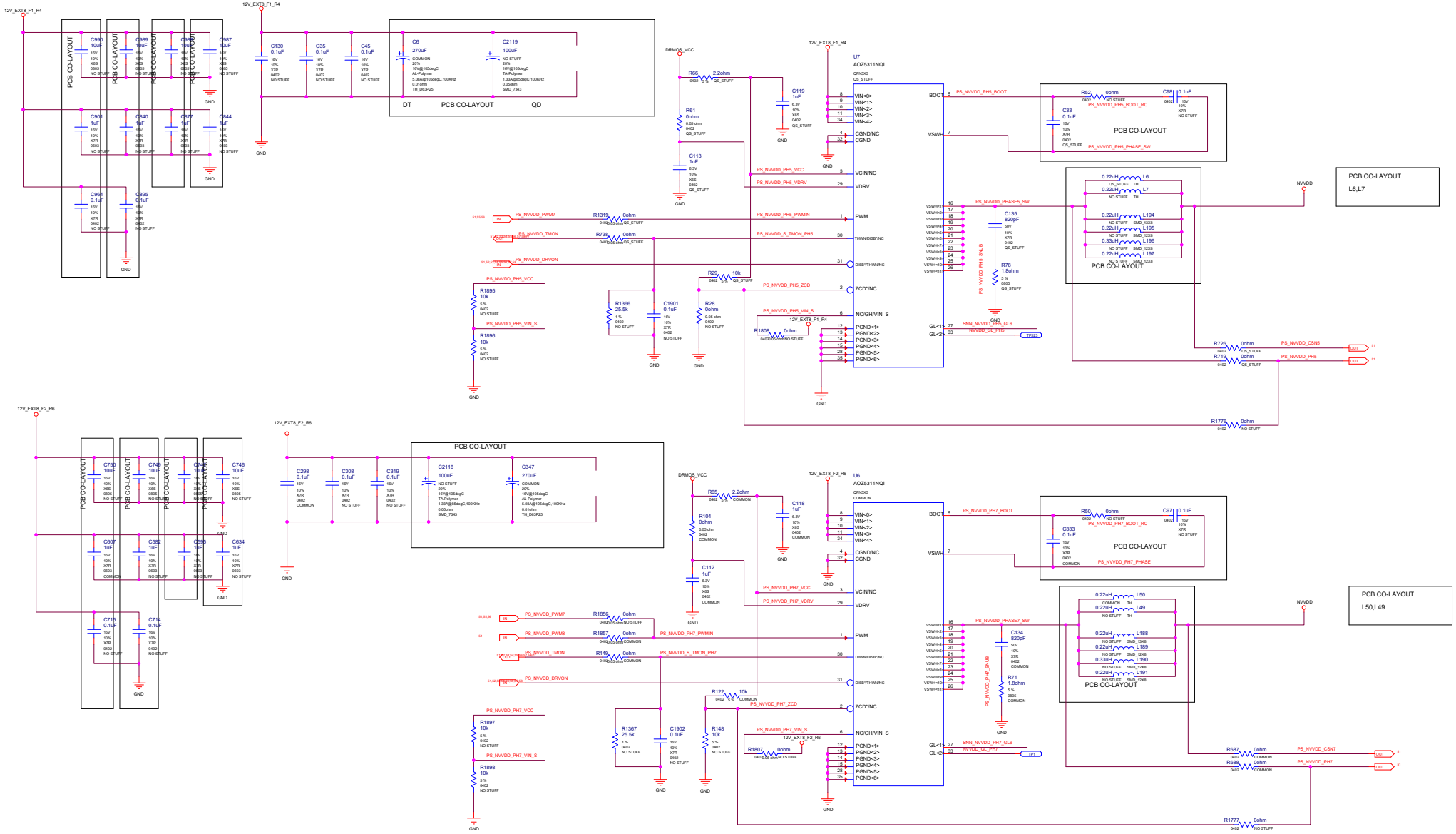
PS: NVVDD PH 5(PWM4), PH7(PWM8/4)



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PAGE DETAIL	PS: NVVDD PH5 (PWM7) and PH7 (PWM8)

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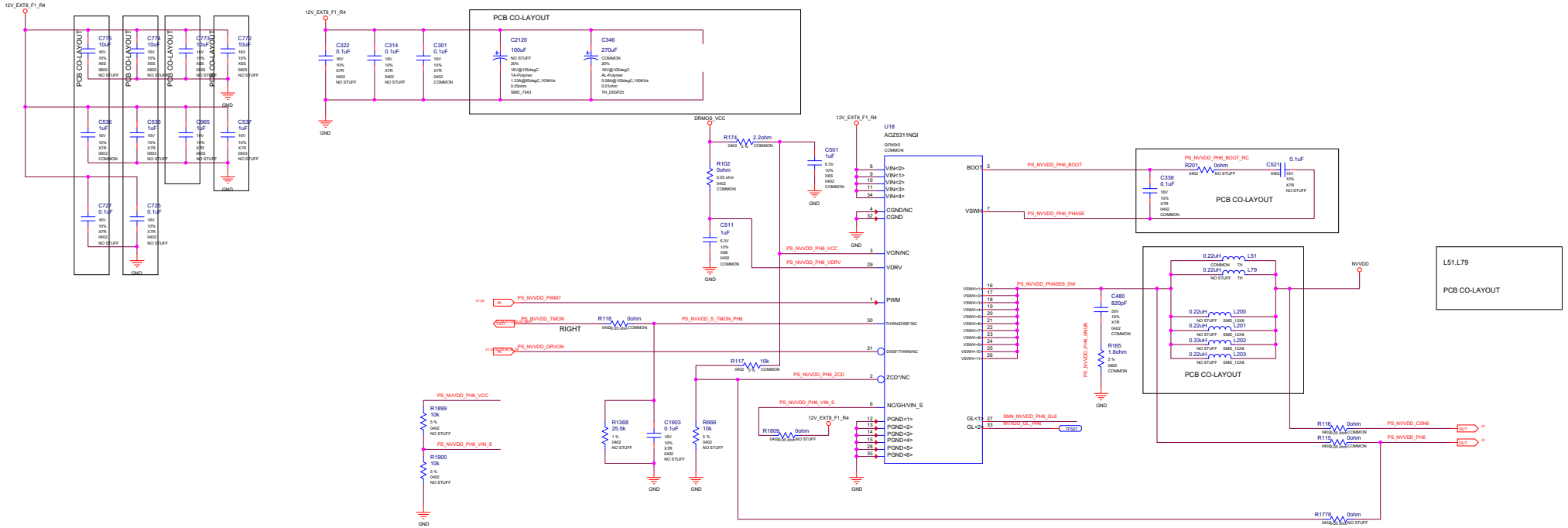
PS: NVVDD Phase 6(PWM4)



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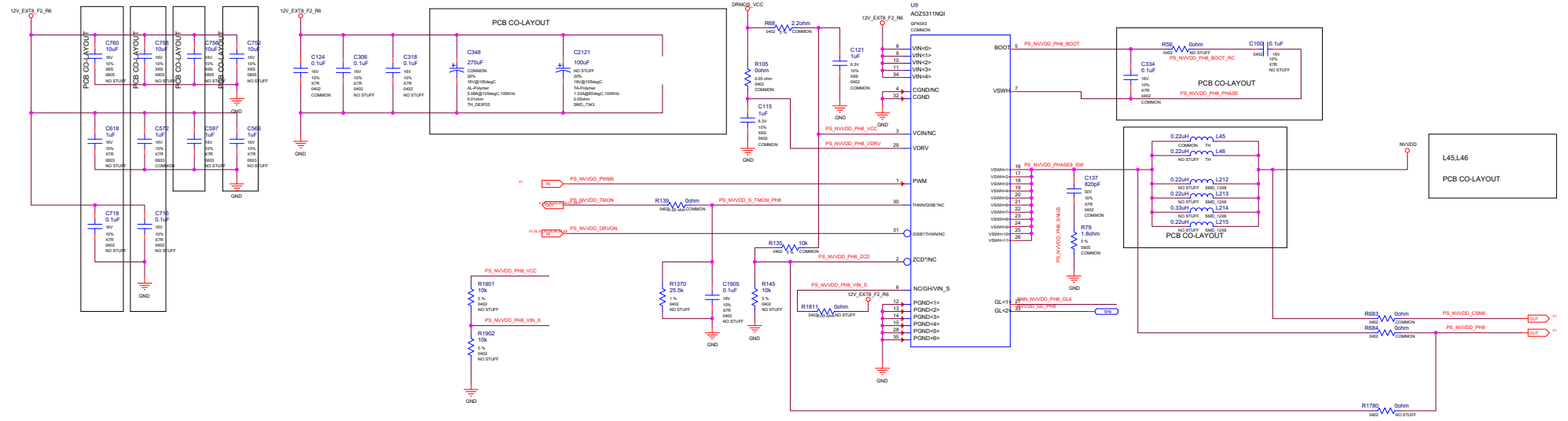
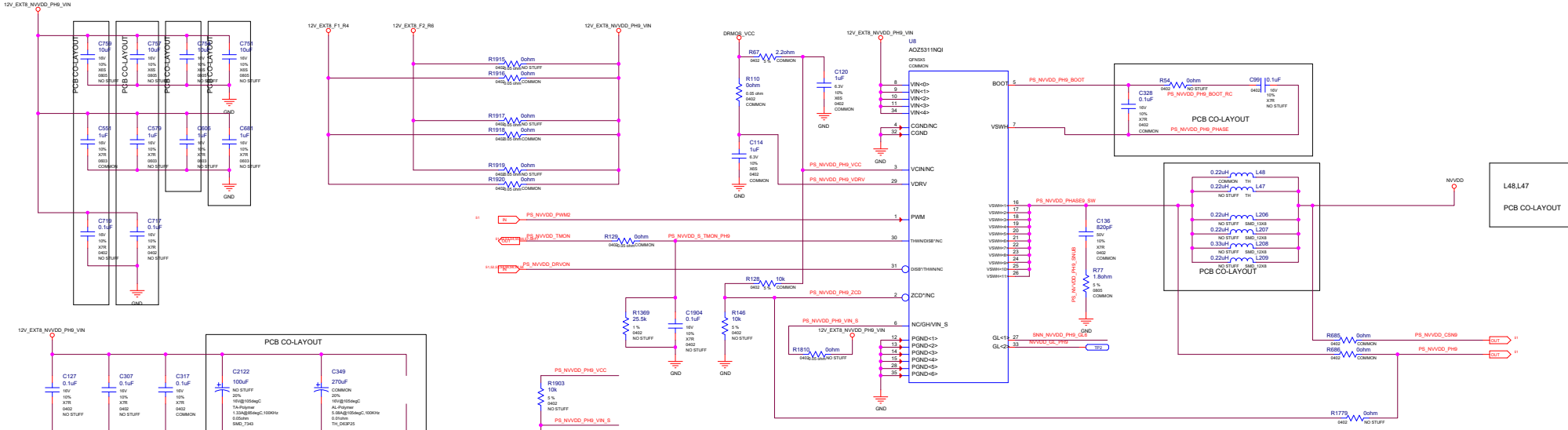
PS: NVVDD PH 8 (PWM5), PH 9(PWM2)





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PAGE DETAIL	PS: NVVDD PH8(PWM5) and PH9(PWM2)

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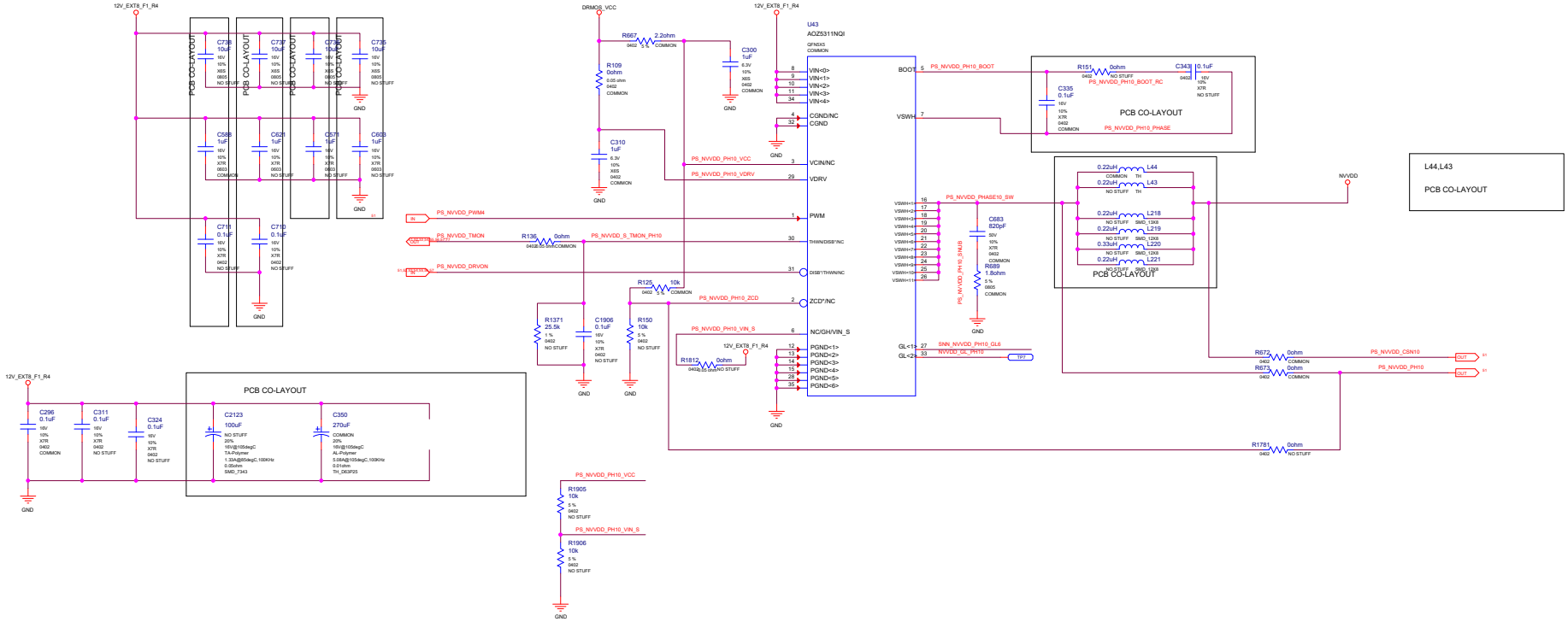
PS: NVVDD Phase 10 (PWM4)



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PAGE DETAIL	PS: NVVDD PH10 (PWM4)

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PAGE DETAIL	Colayout Notes

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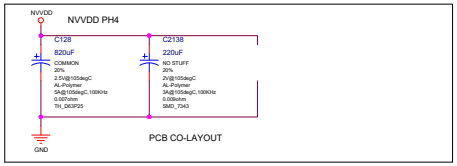
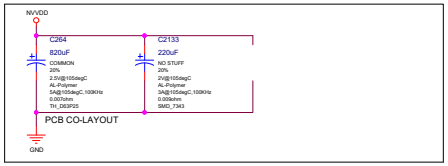
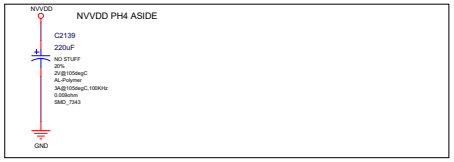
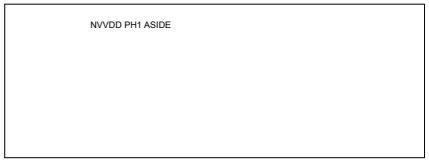
PS: NVVDD OUTPUT CAP(TOP)

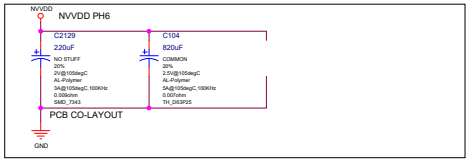
REFER TO PCB FOR BOM STUFFING

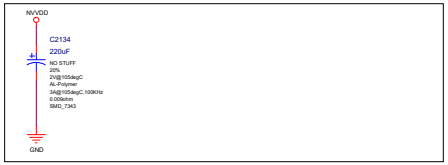


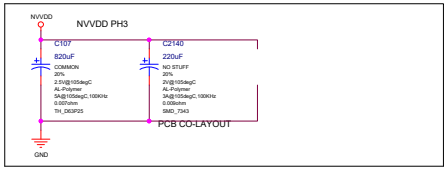


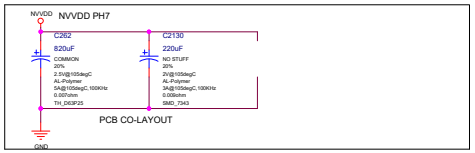


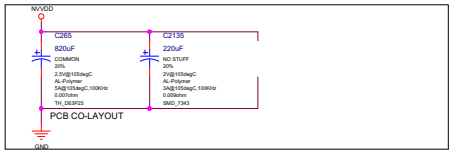


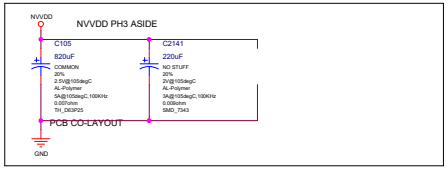


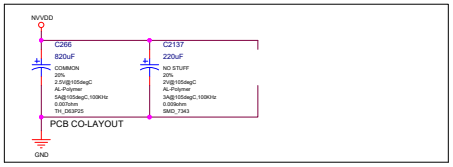


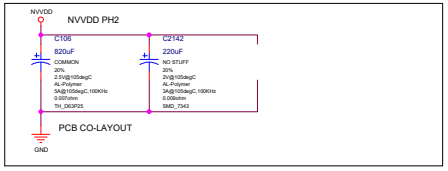


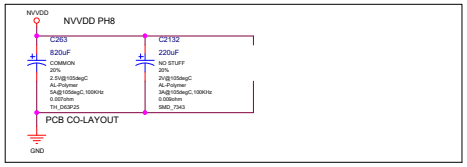












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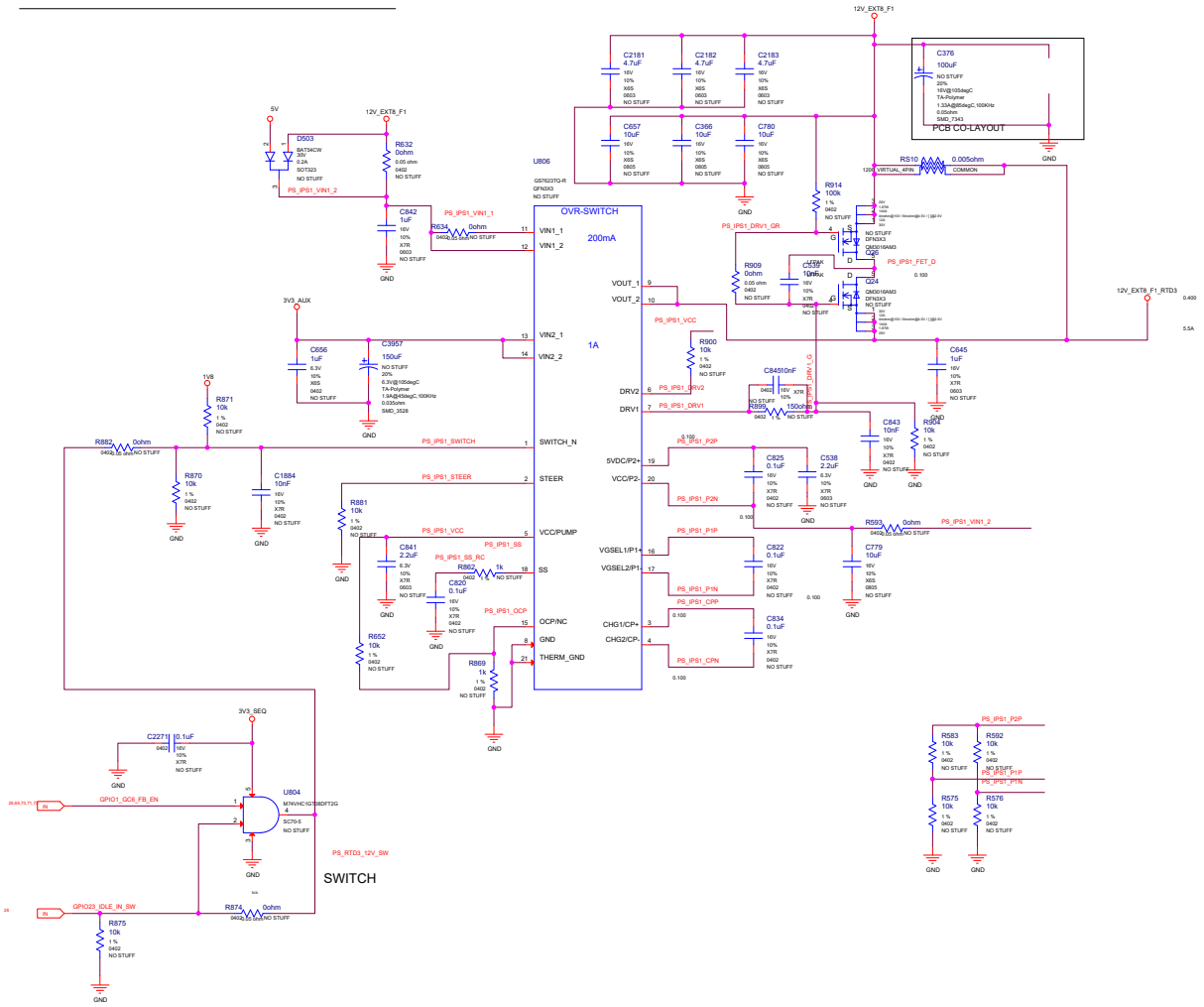
PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO23	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



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PAGE DETAIL PS: INPUT SWITCH RTD3

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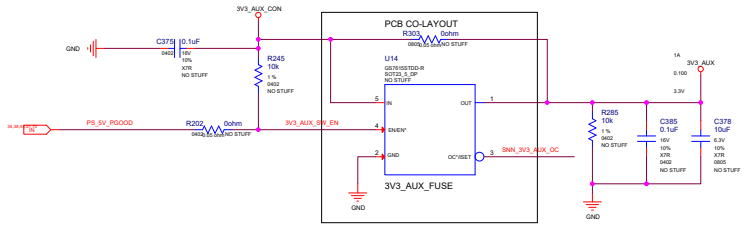
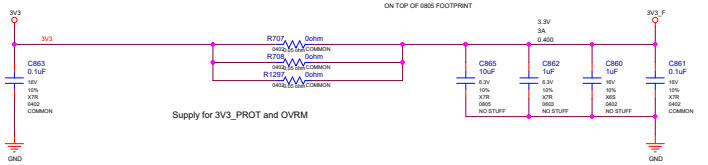
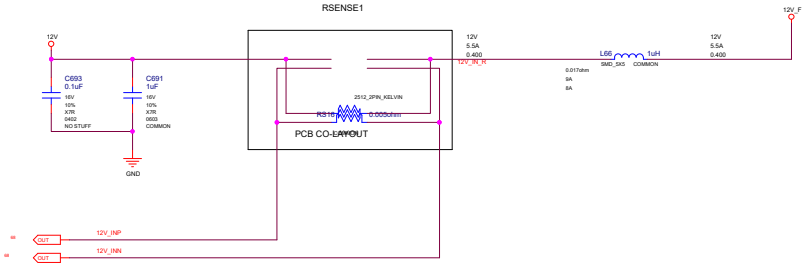
PS: Inputs, Filtering, and Monitoring



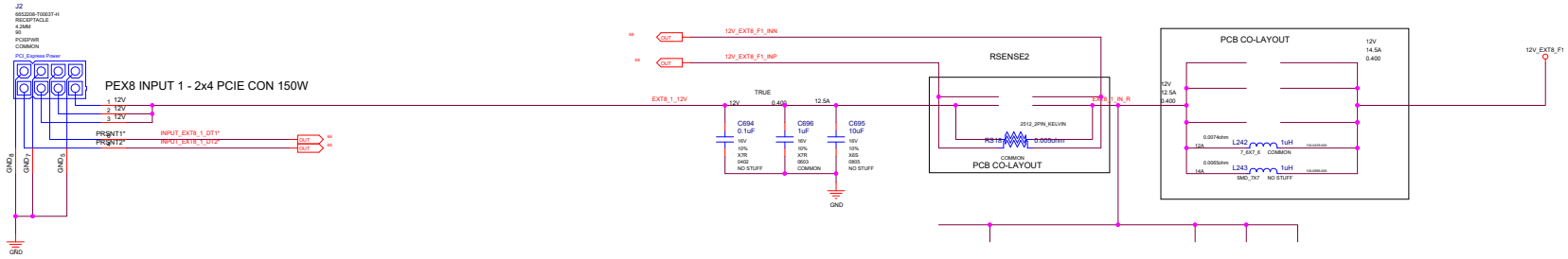
PEX 3V3 INPUT - 10W



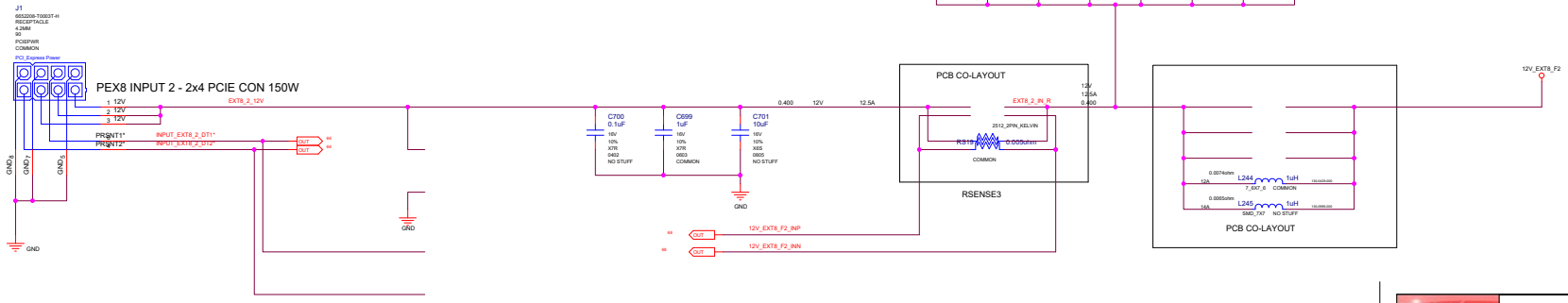
PEX_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



QD SKU CABLE

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PAGE DETAIL	PS: INPUTS, FILTERING, and, MONITORING

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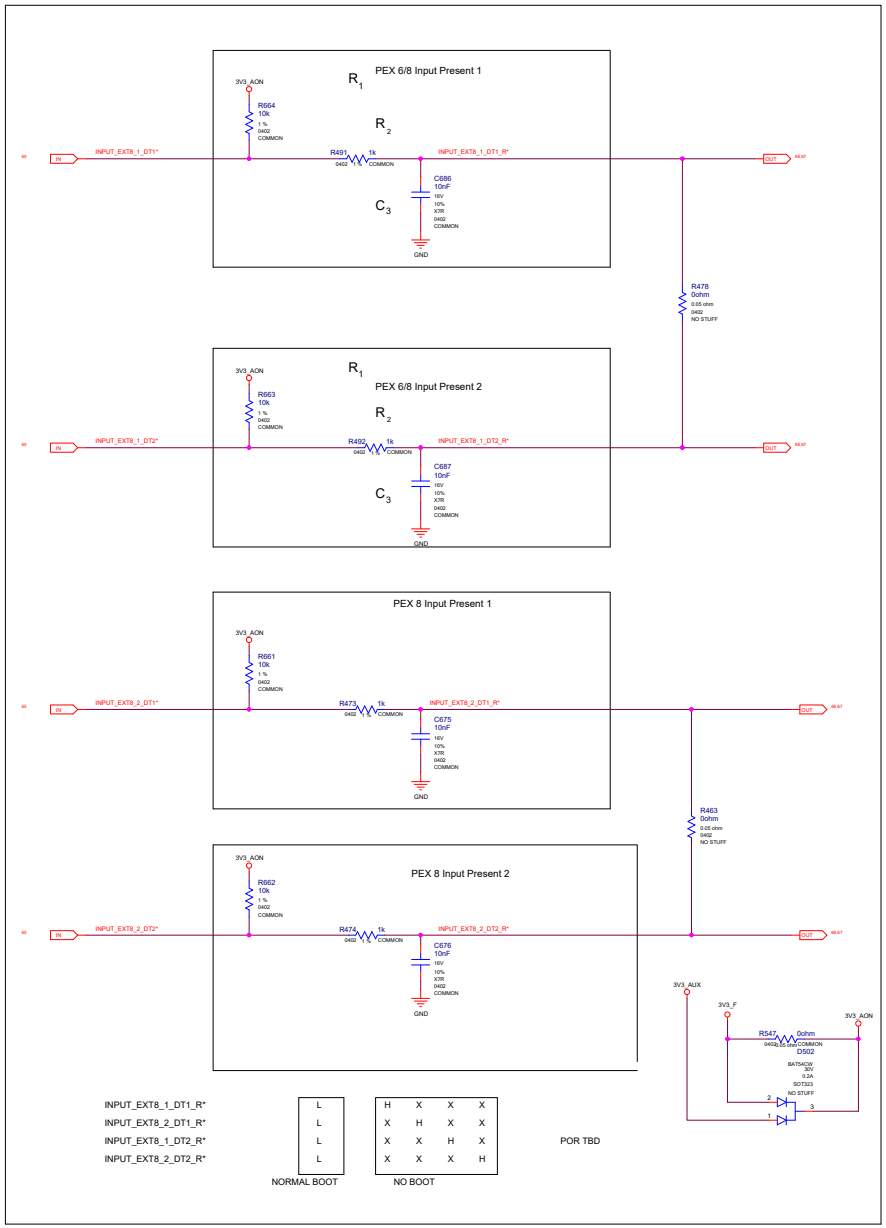
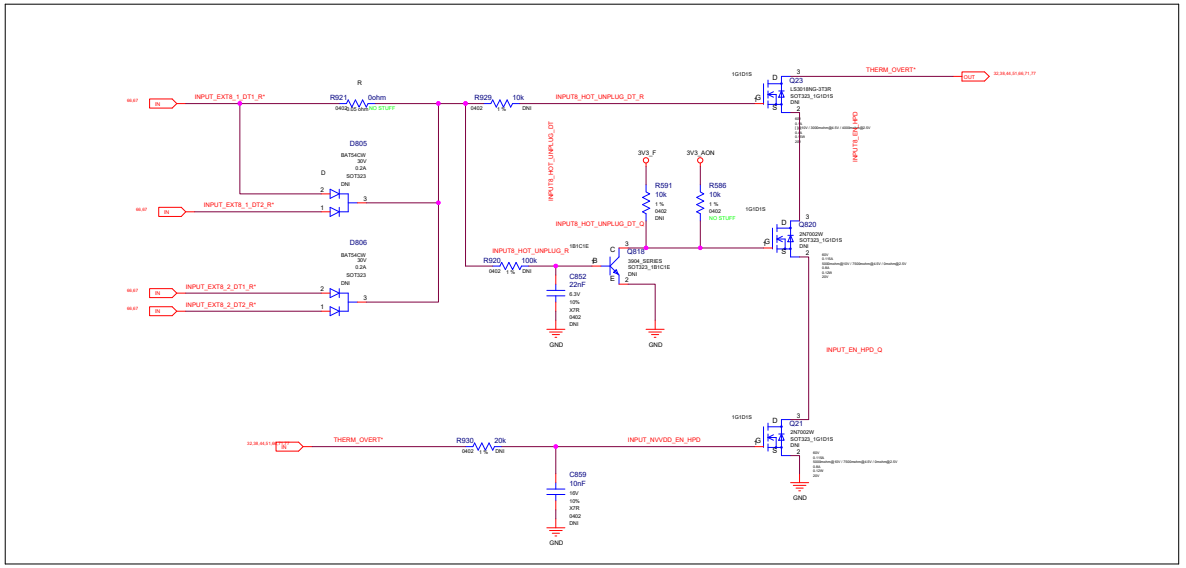
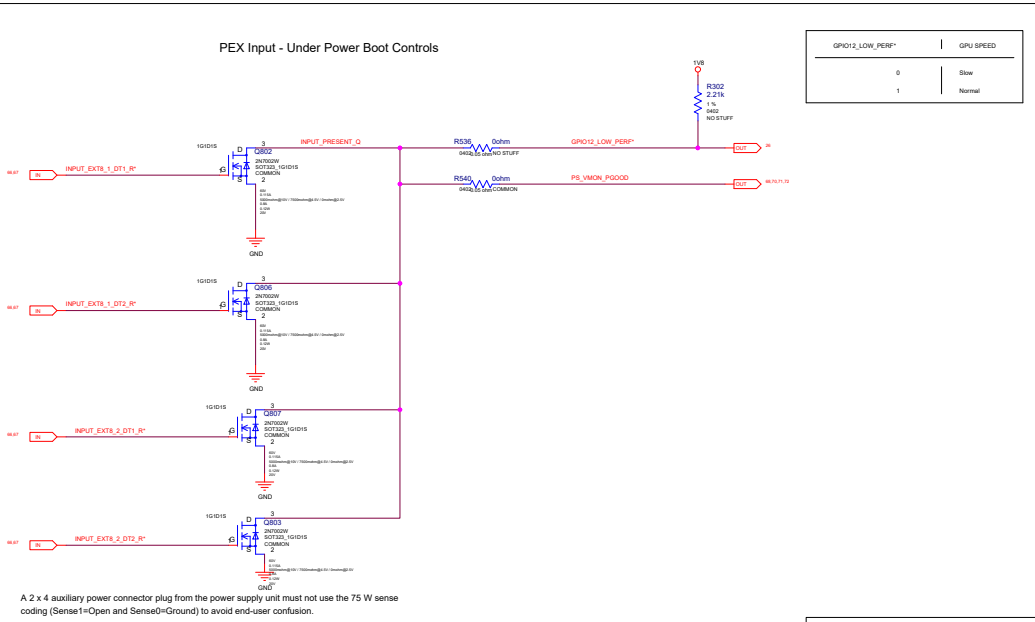
PS: 12V Current Steering & Hot Unplug Detect







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PAGE DETAIL	PS: HOT UNPLUG

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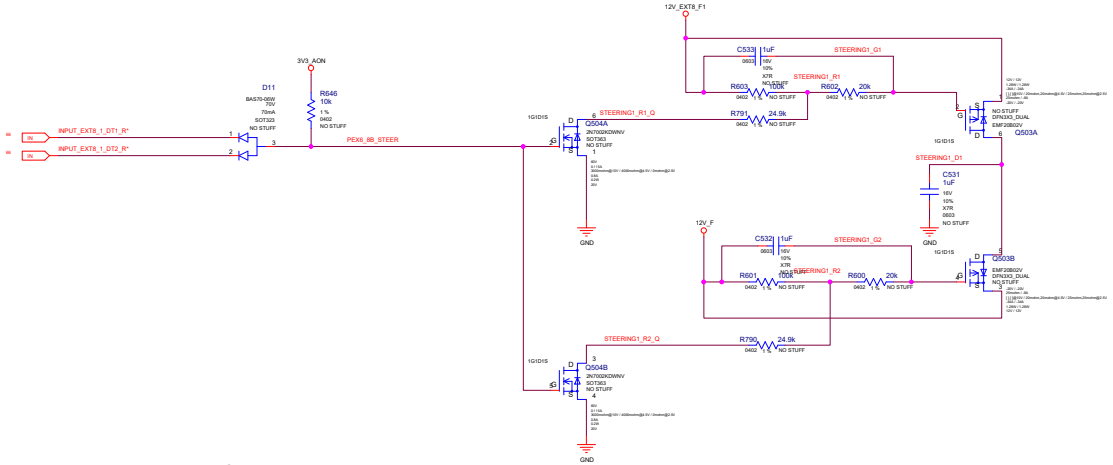
PS: Discrete Steering

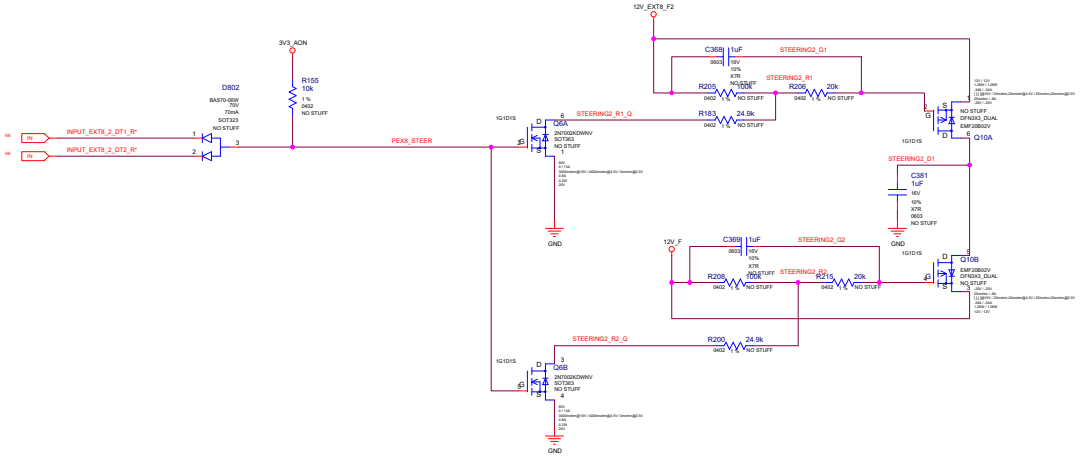
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1



NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V_EXT8_F2



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Discrete Power Steering

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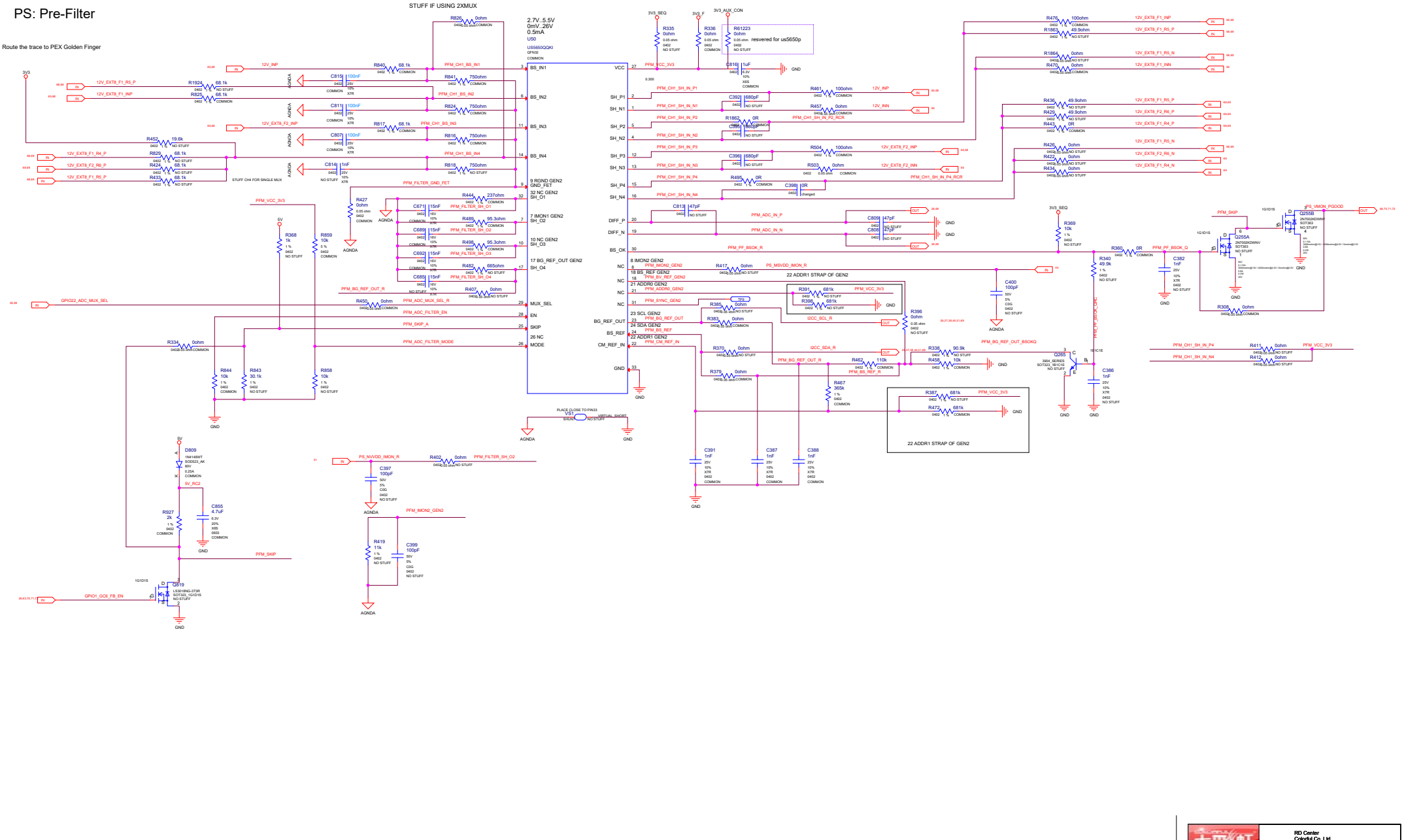
PS: Pre-Filter

Route the trace to PEX Golden Finger



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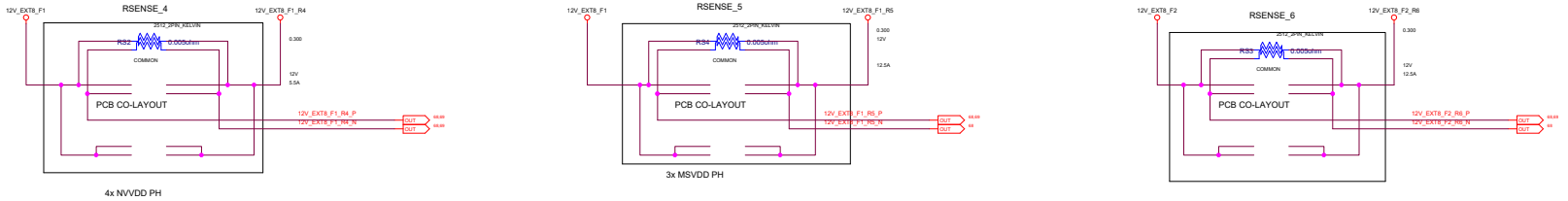
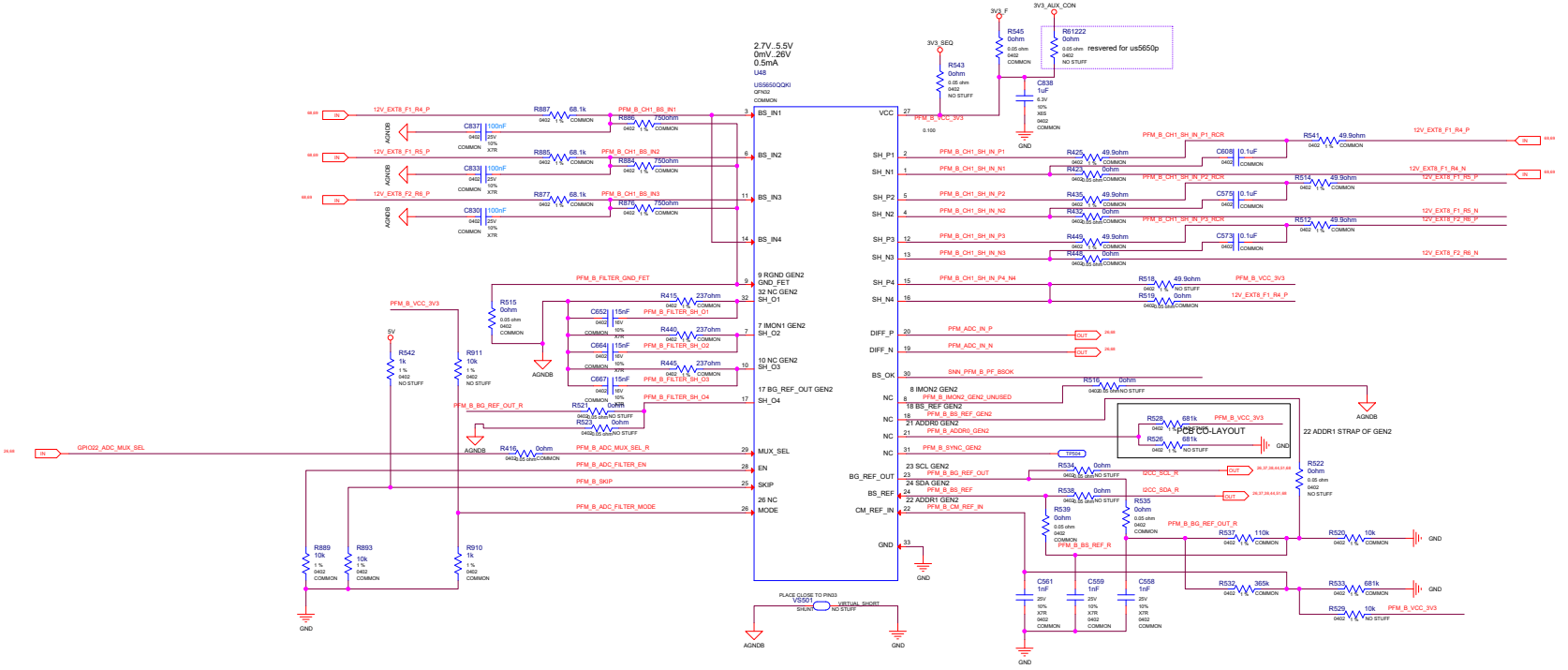
PS: Pre-Filter B





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PAGE DETAIL	PS: PREFILTER B

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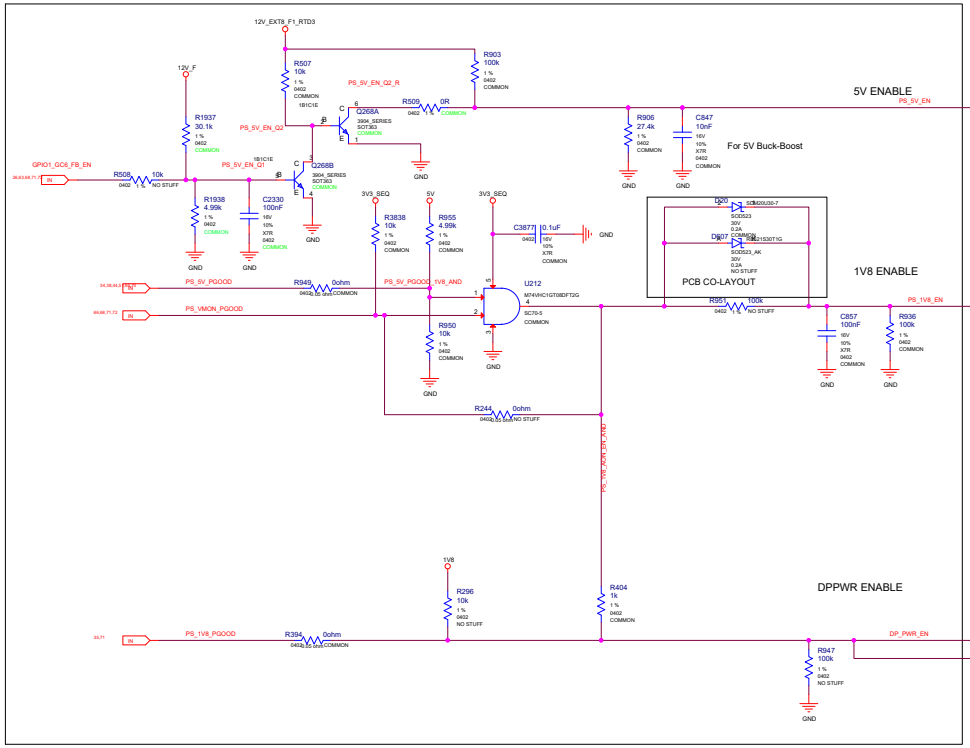

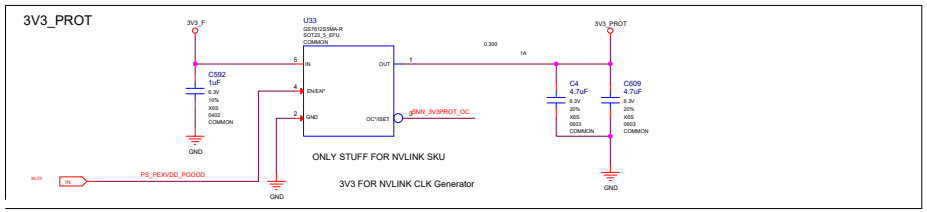

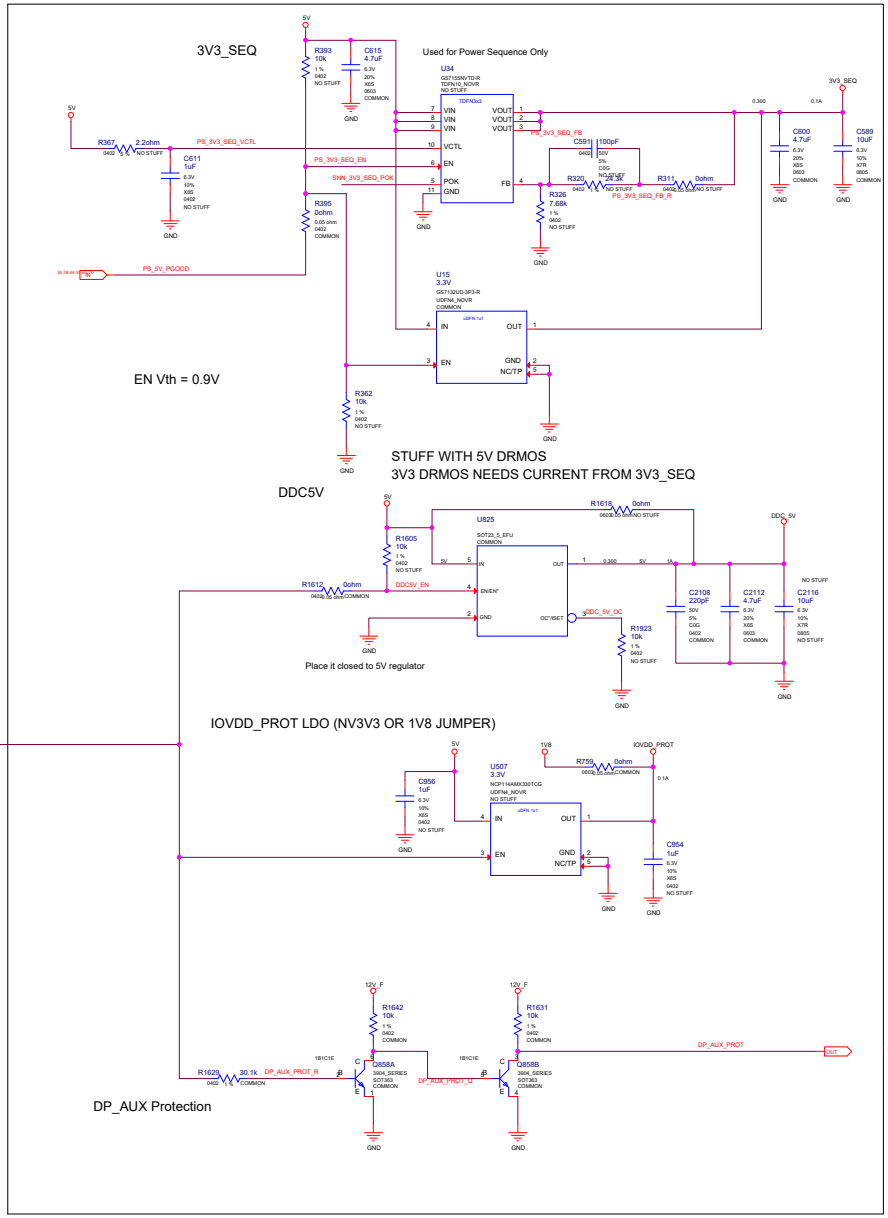

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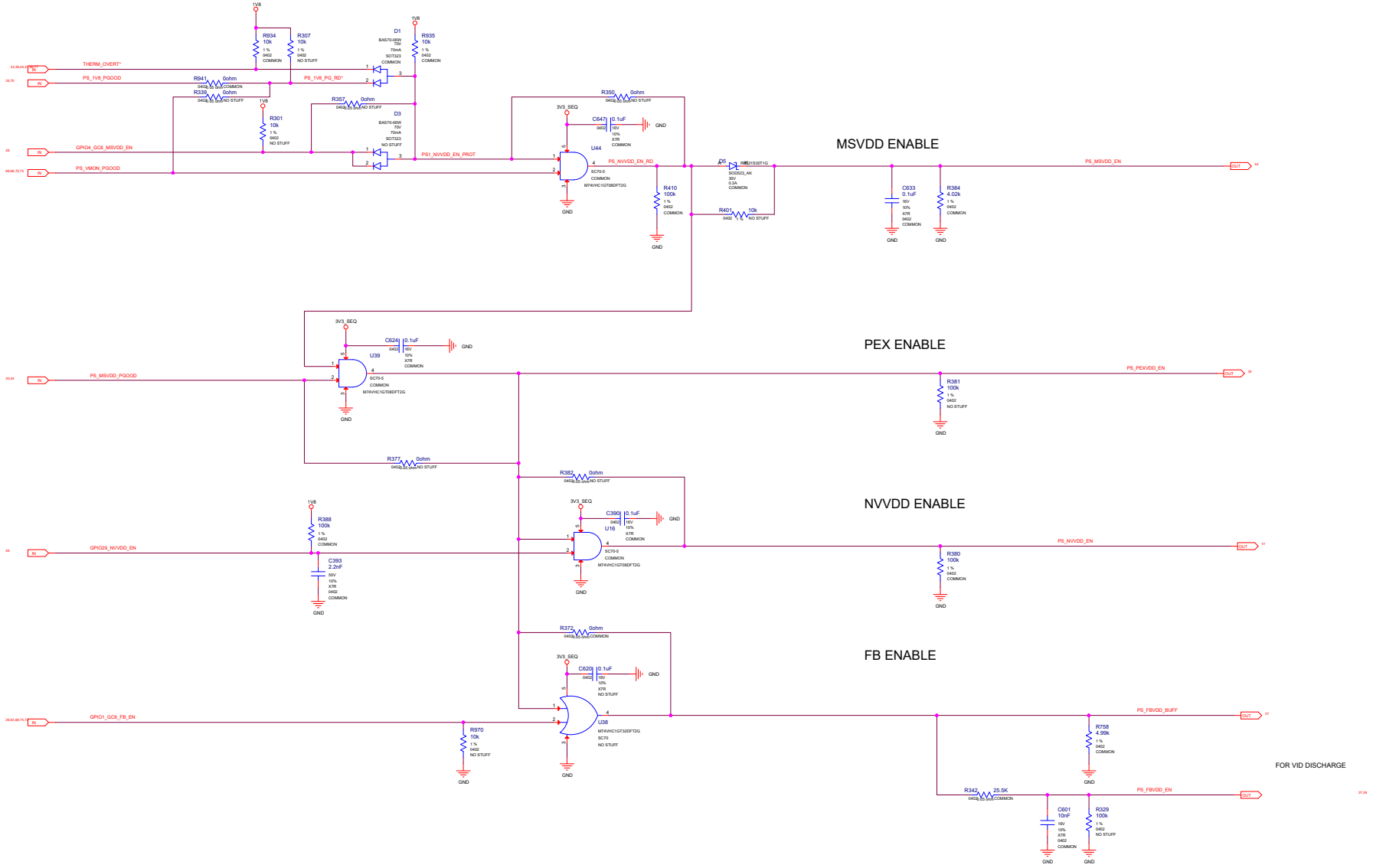
SEQUENCE:NV,PEX,FB ENABLE



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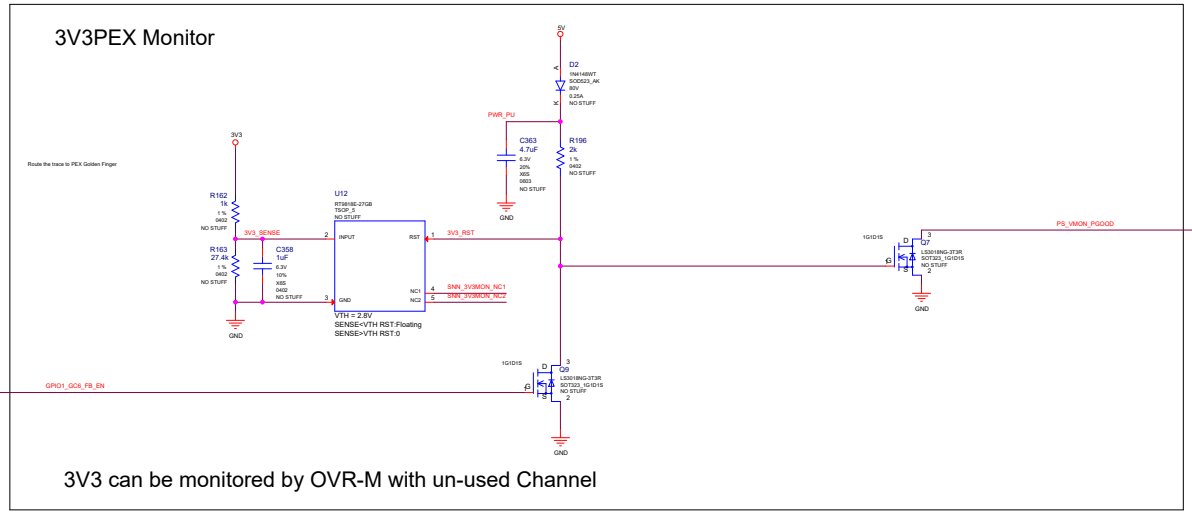
Sequence: 3V3 MONITOR



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PAGE DETAIL	Sequence: 3V3 MONITOR

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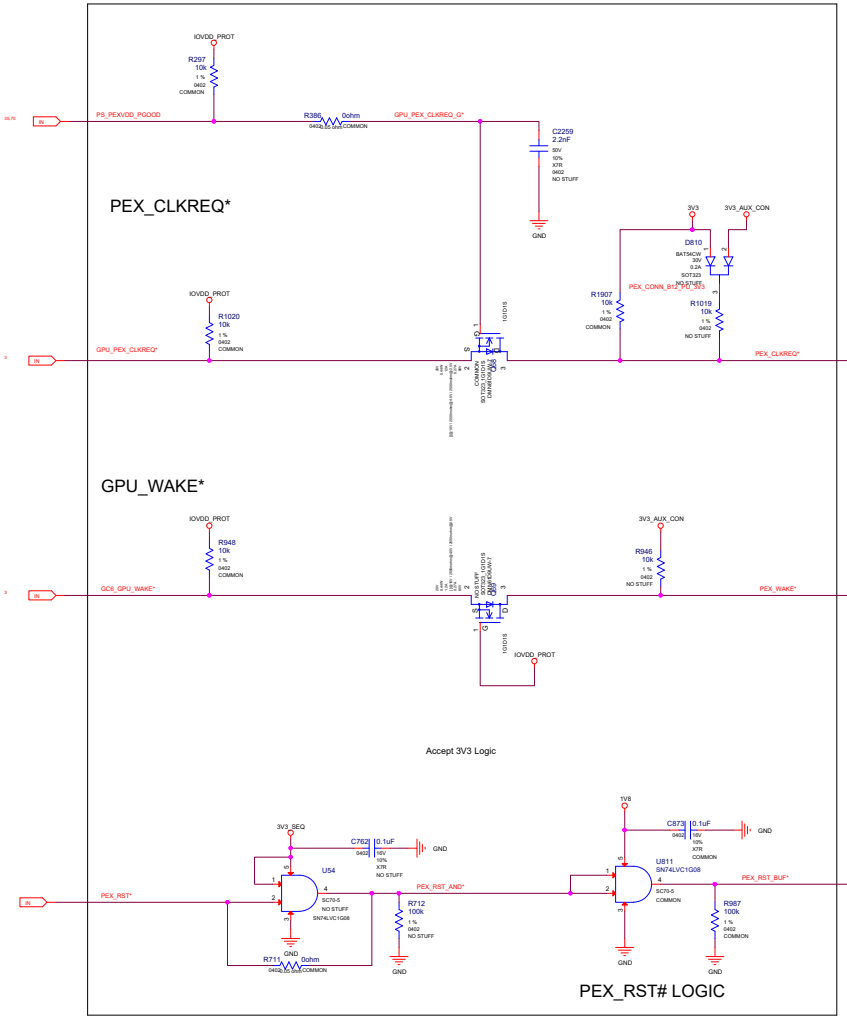
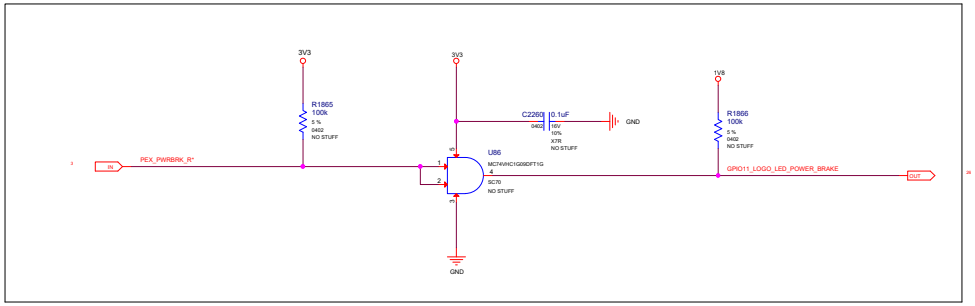
SEQUENCE:MISC





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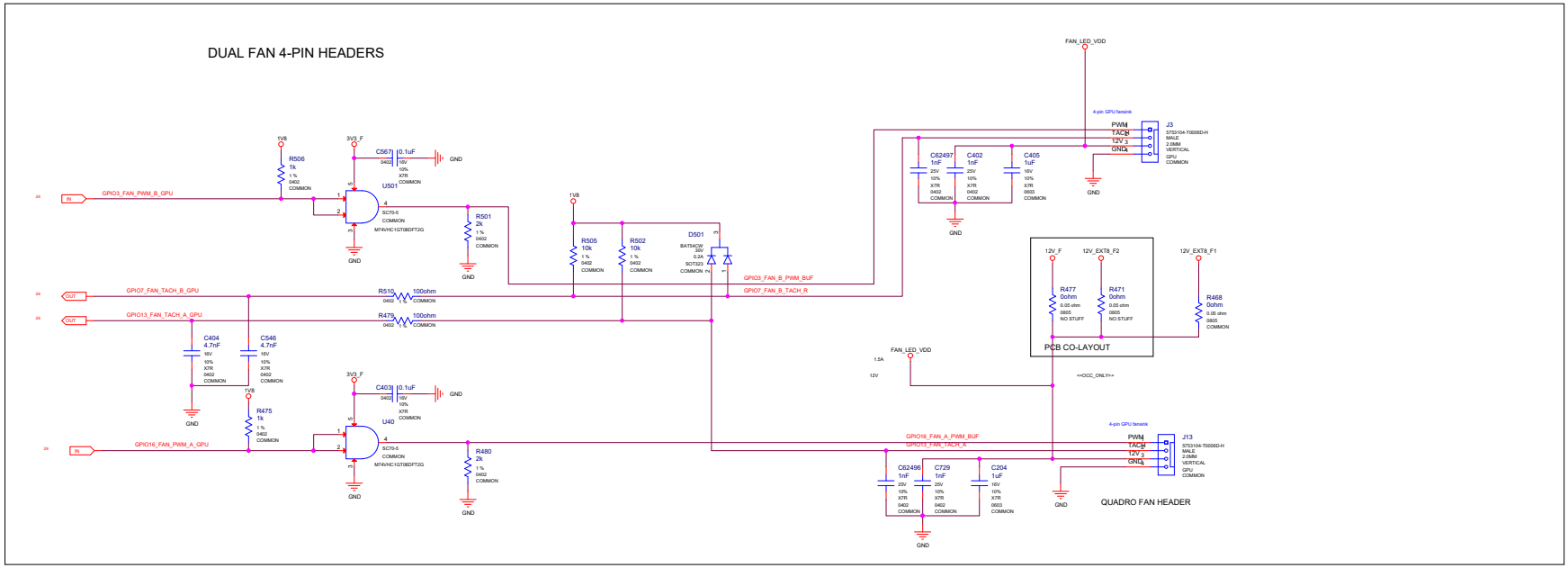
MISC: LED & FAN



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PAGE DETAIL	MISC: LED & FAN

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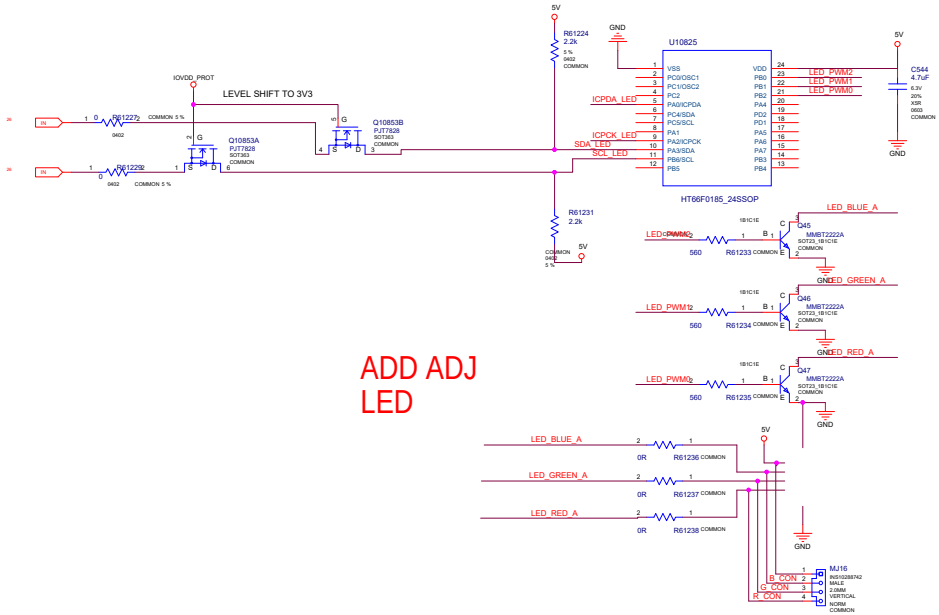
MISC: RGBW LED REF



ADD ADJ LED

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	RGBW LED REF

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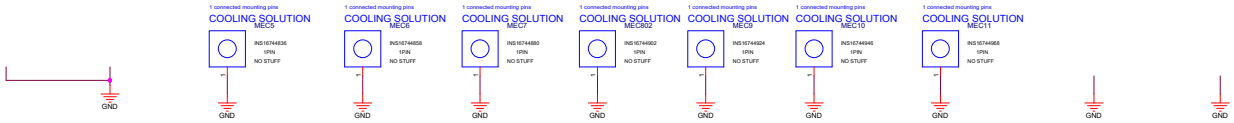
Mechanical: Mounting holes



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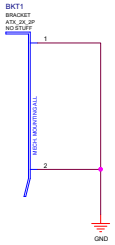

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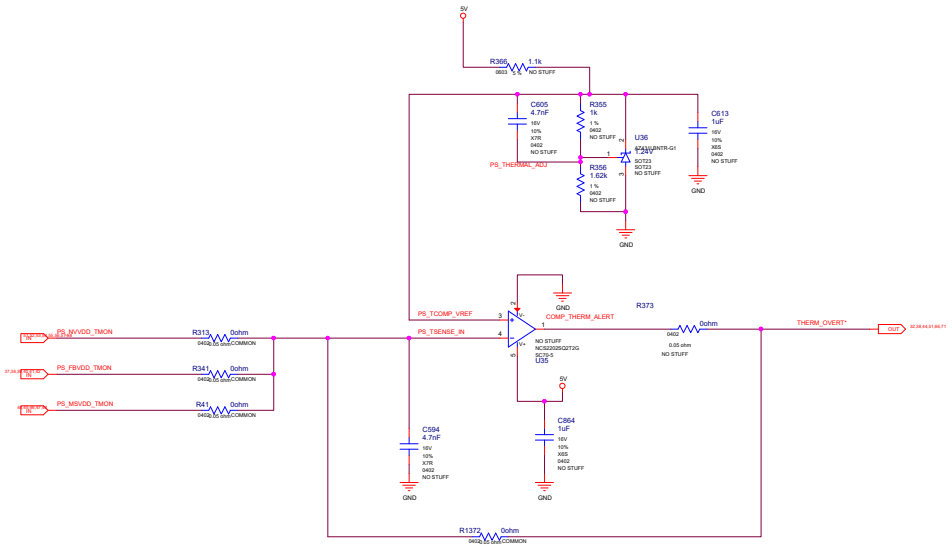
VR THERMAL PROTECTION



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	VR Thermal Protection

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PCI TERM

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCIE TERM

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