PG413 A00

GP104 - 8GB GDDR5X, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

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MS-V336

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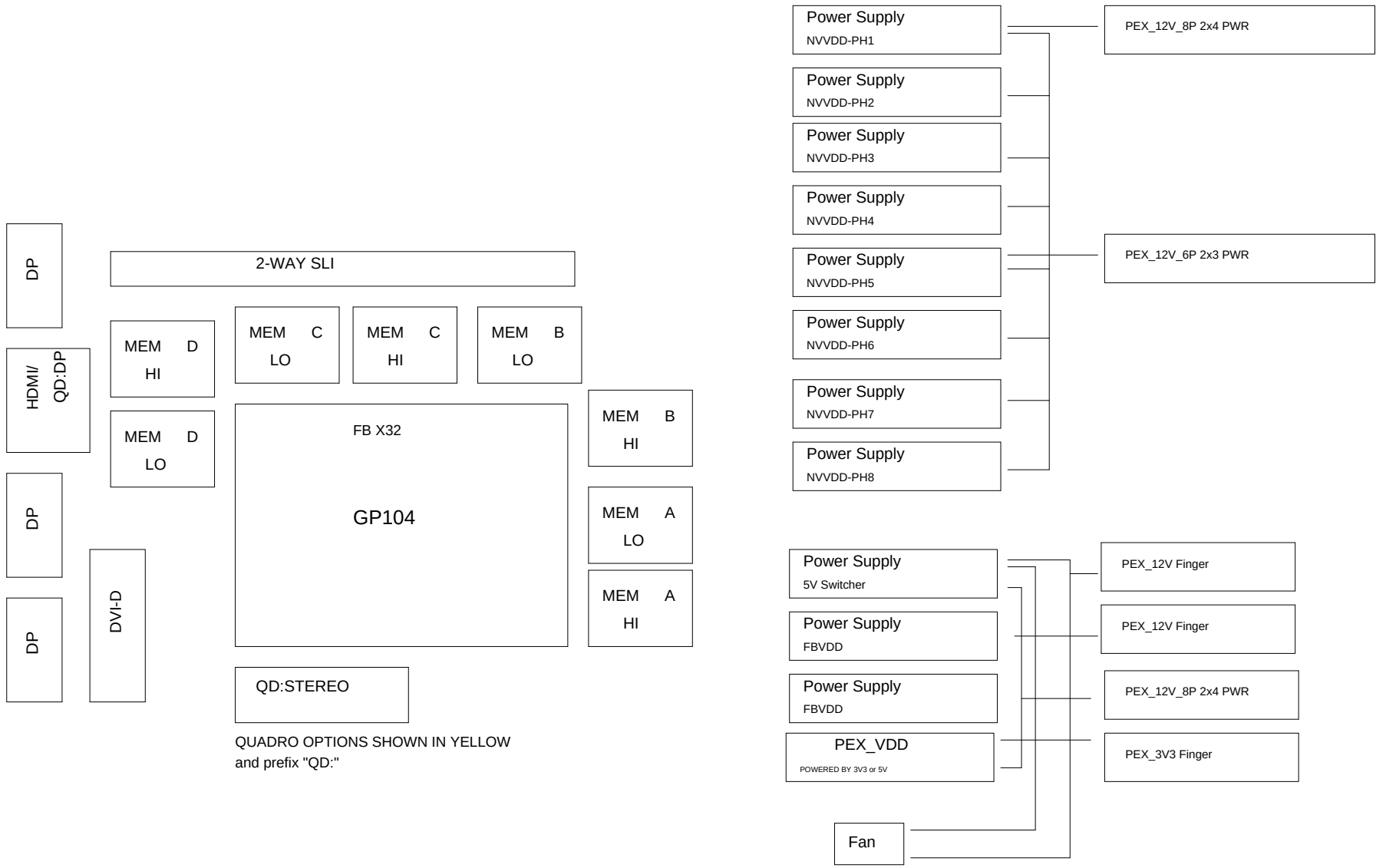

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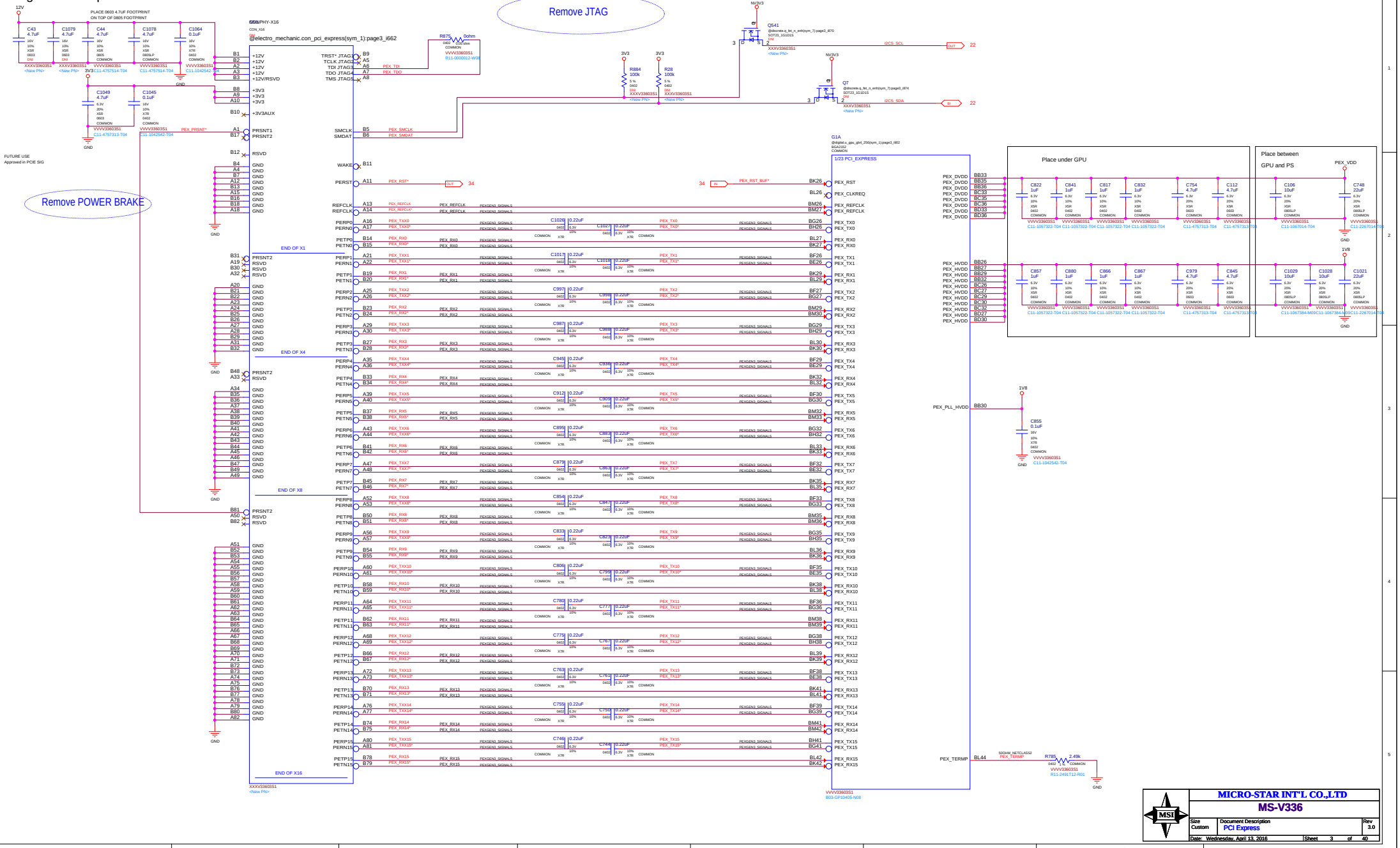
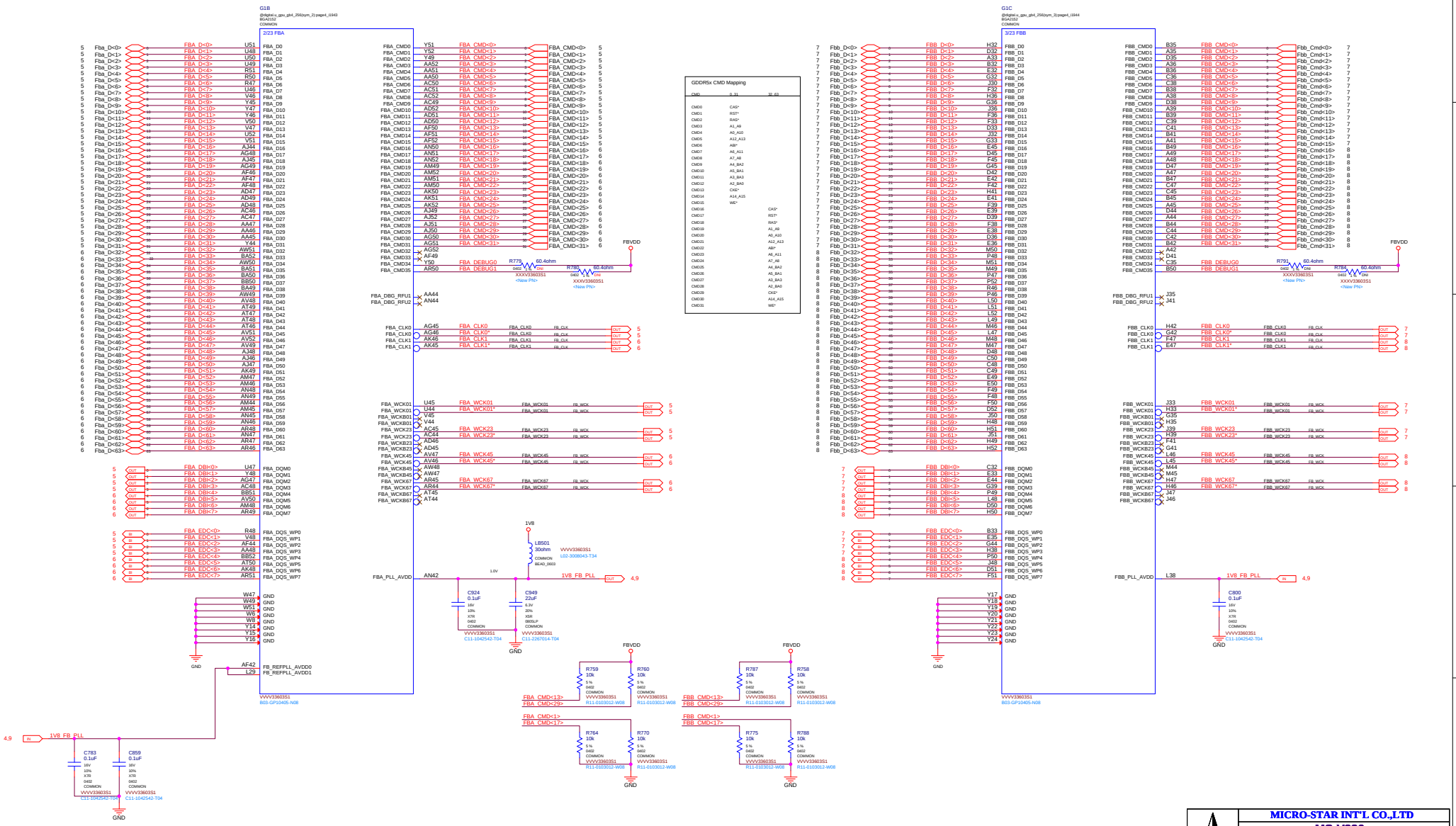


Page4: MEMORY: GPU Partition A/B



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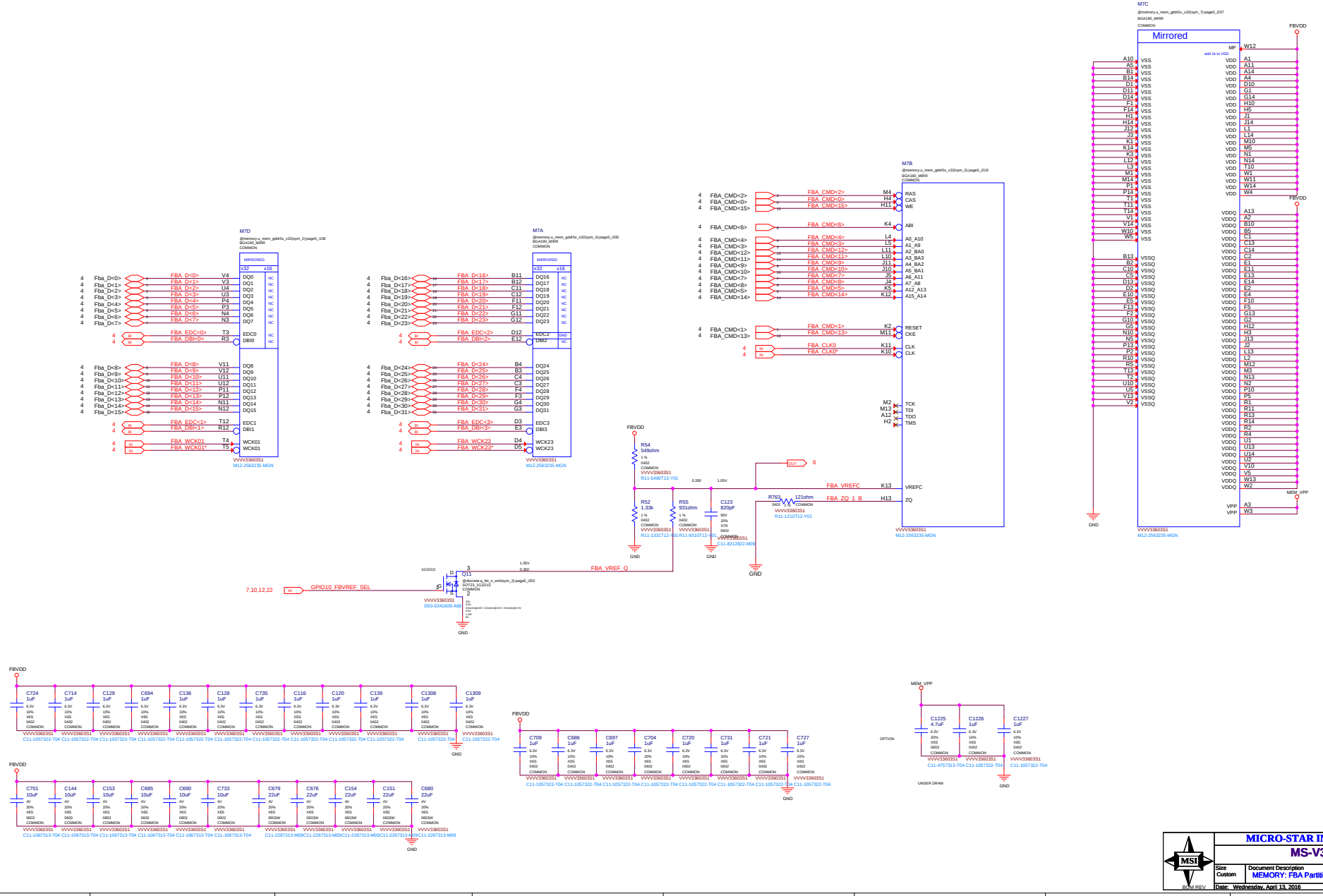

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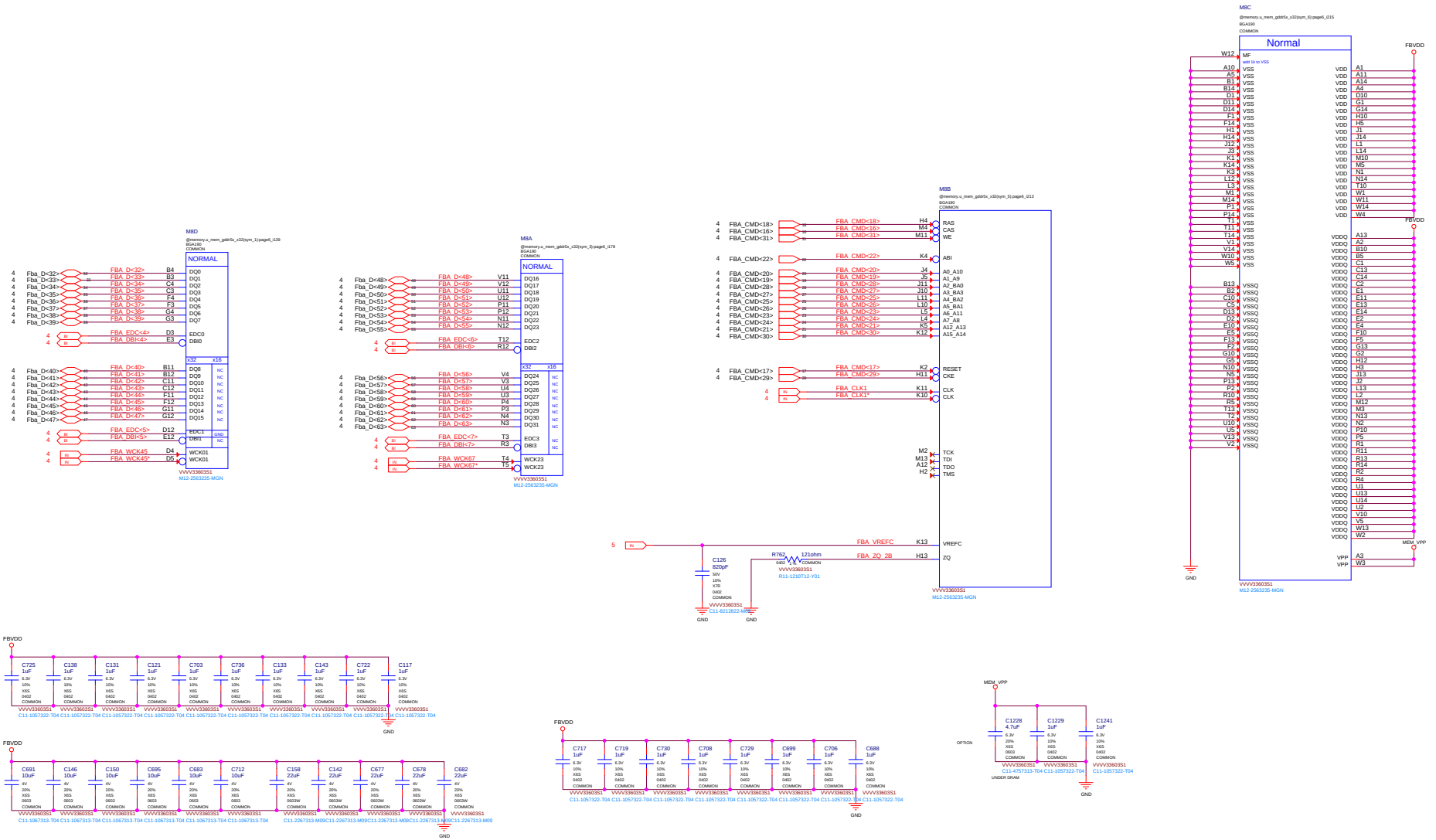

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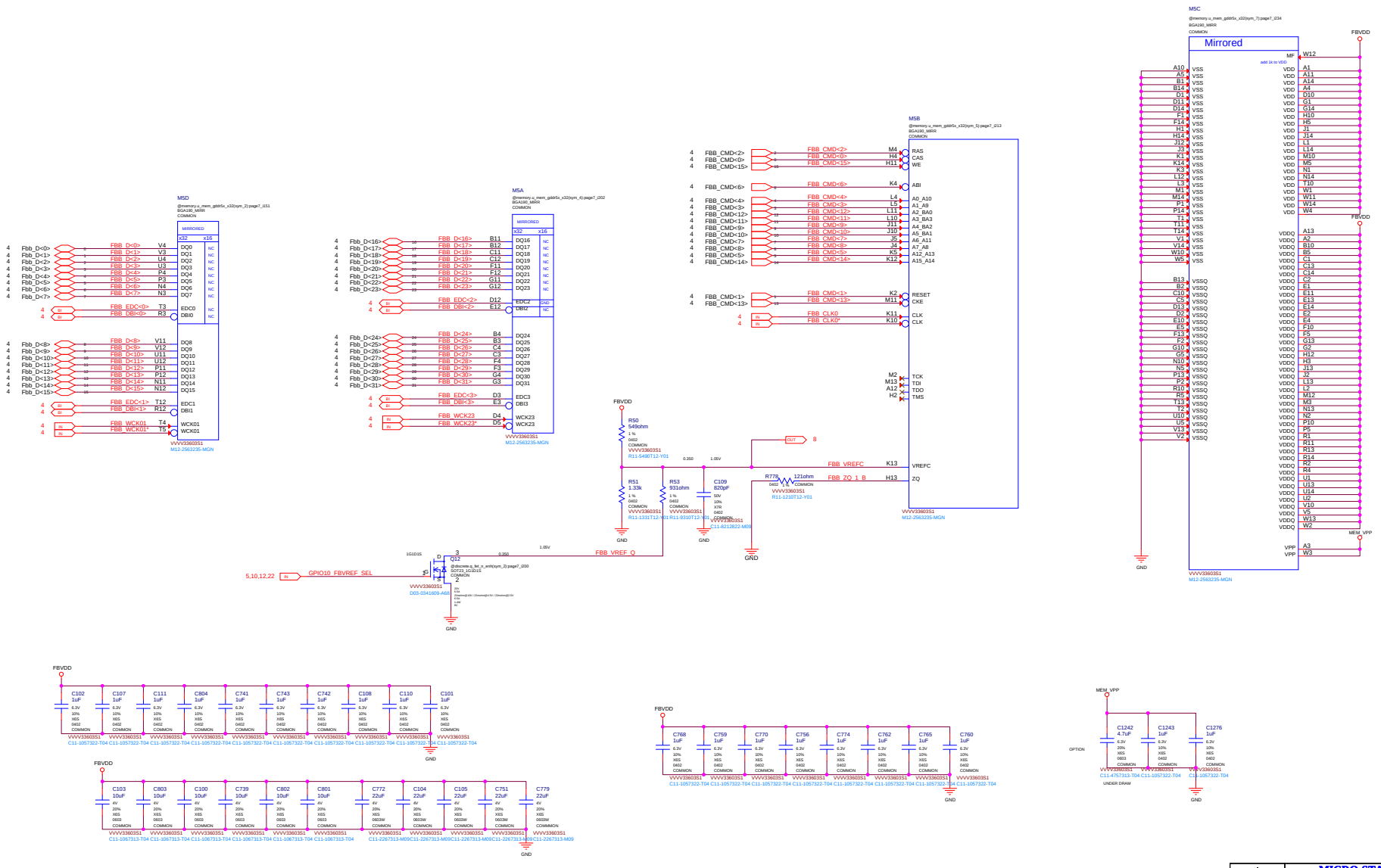

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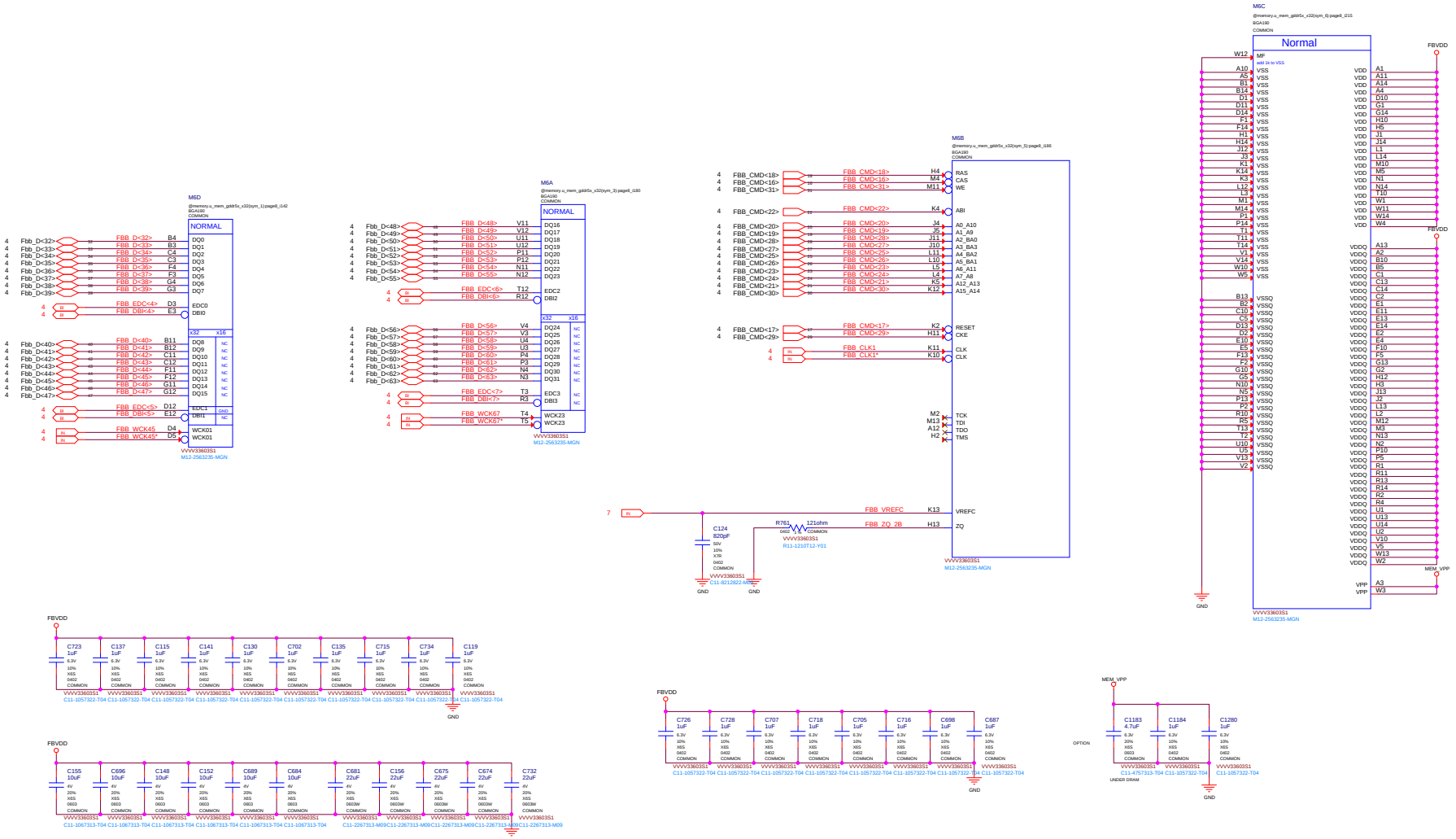

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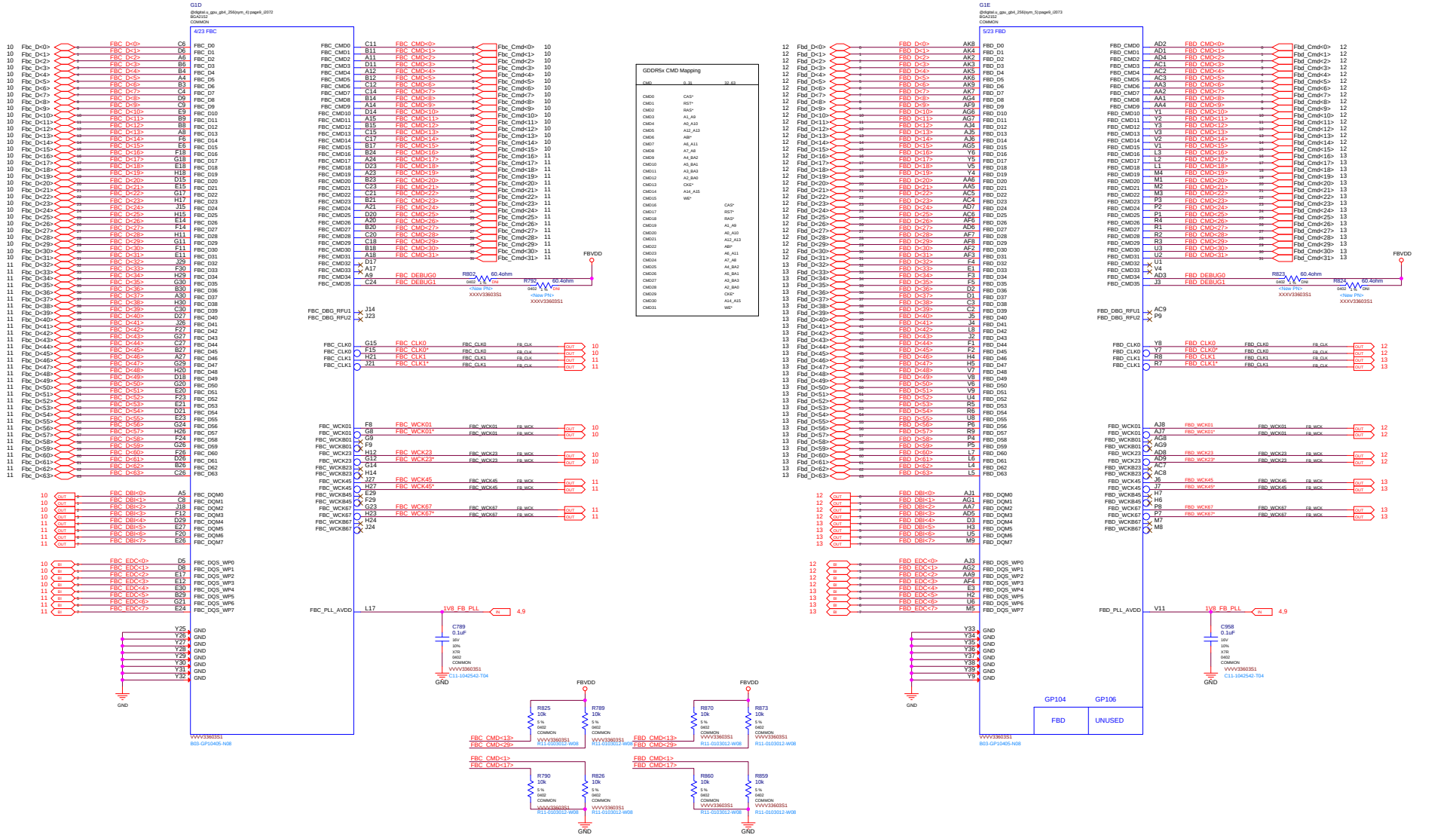
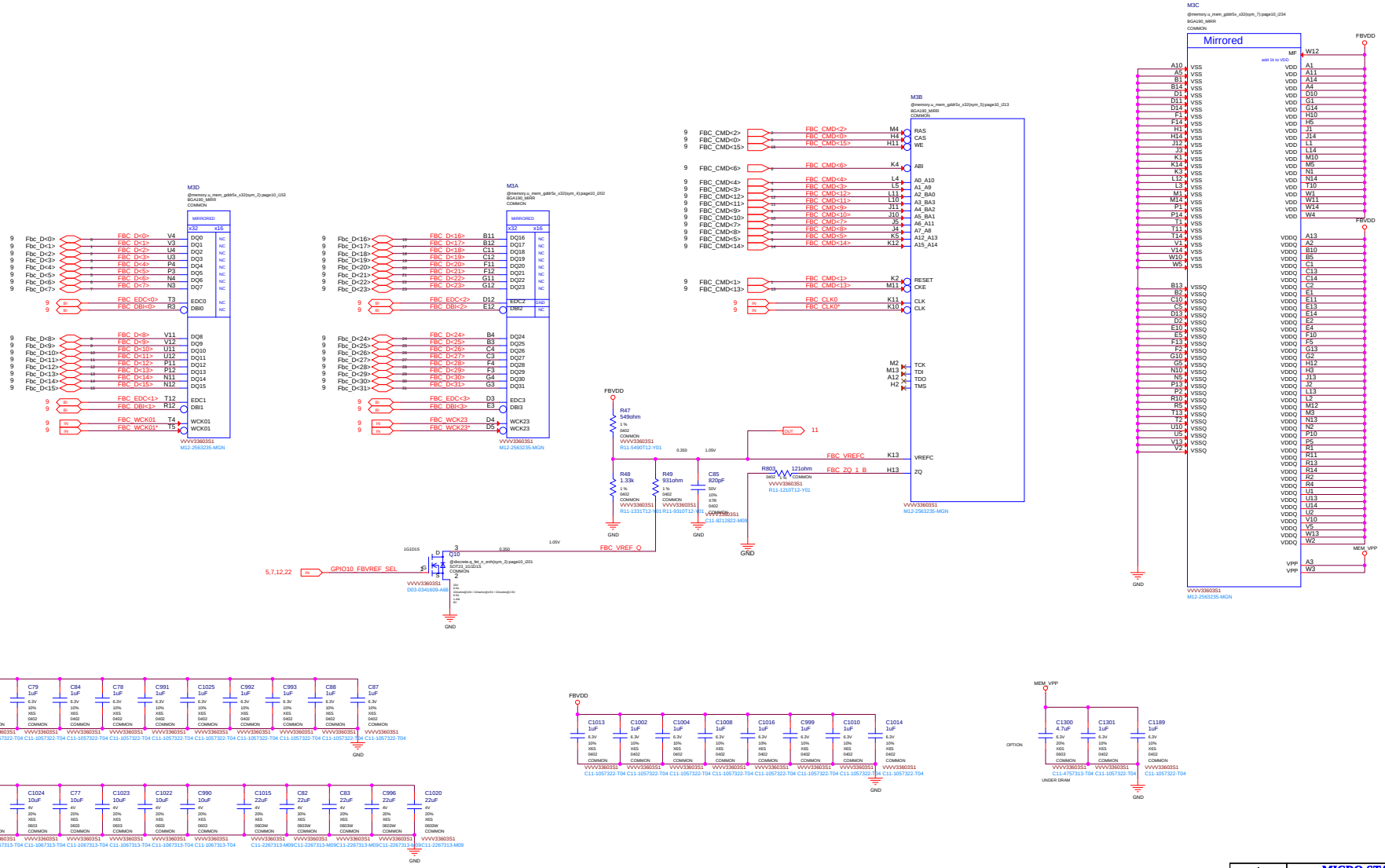


Page10: MEMORY: FBC Partition 31..0



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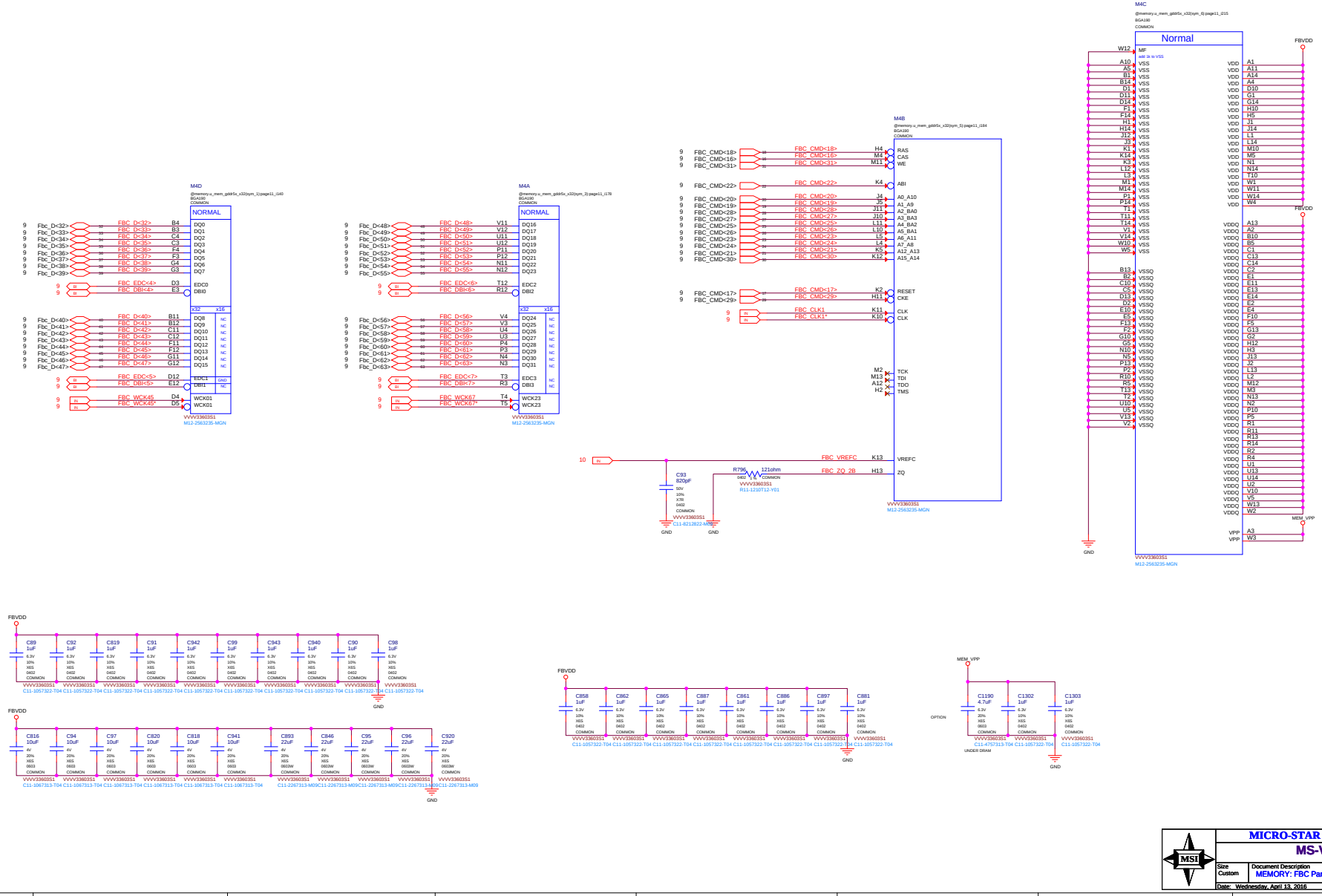

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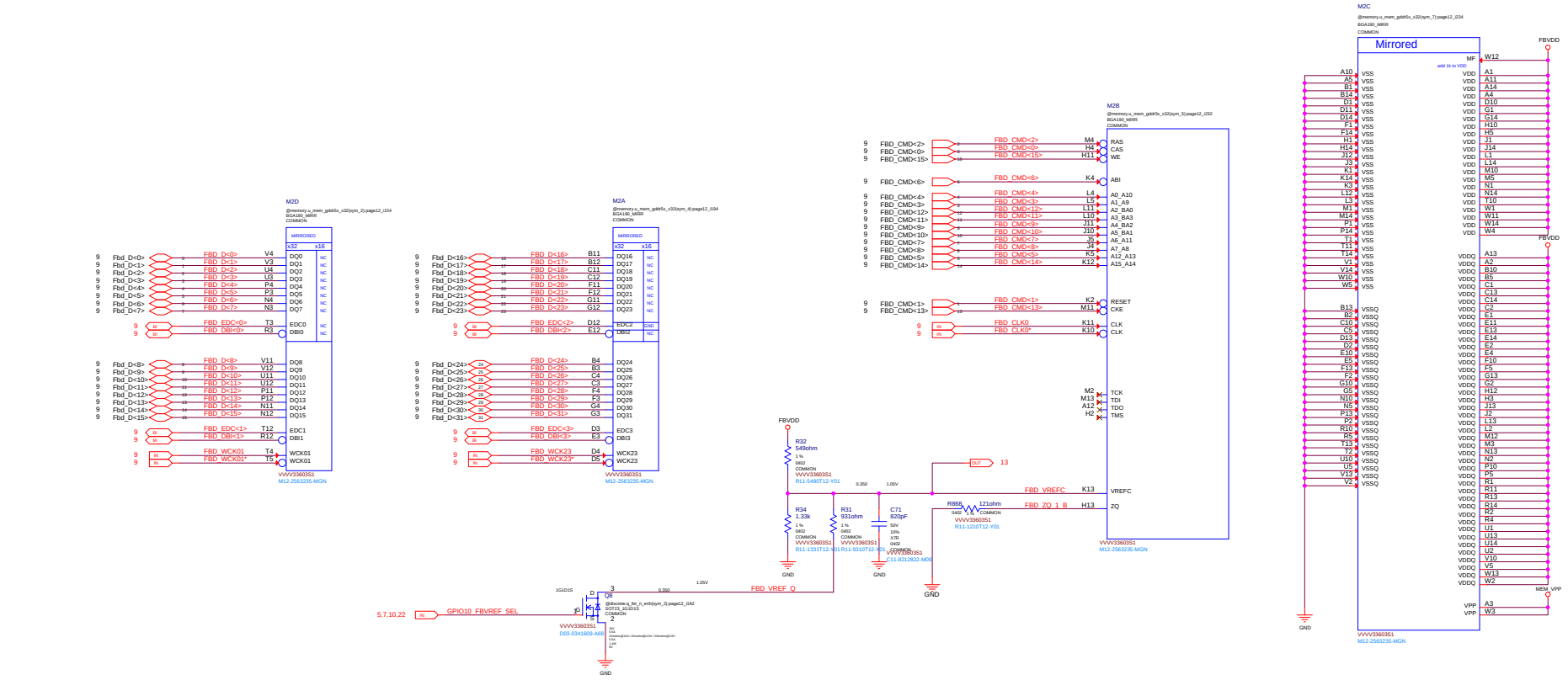

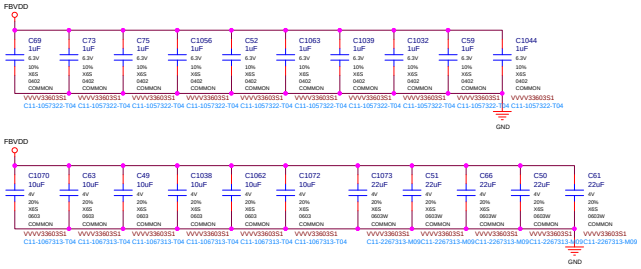

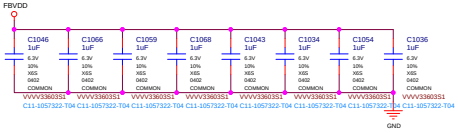

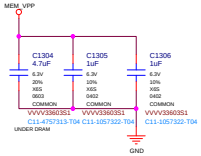

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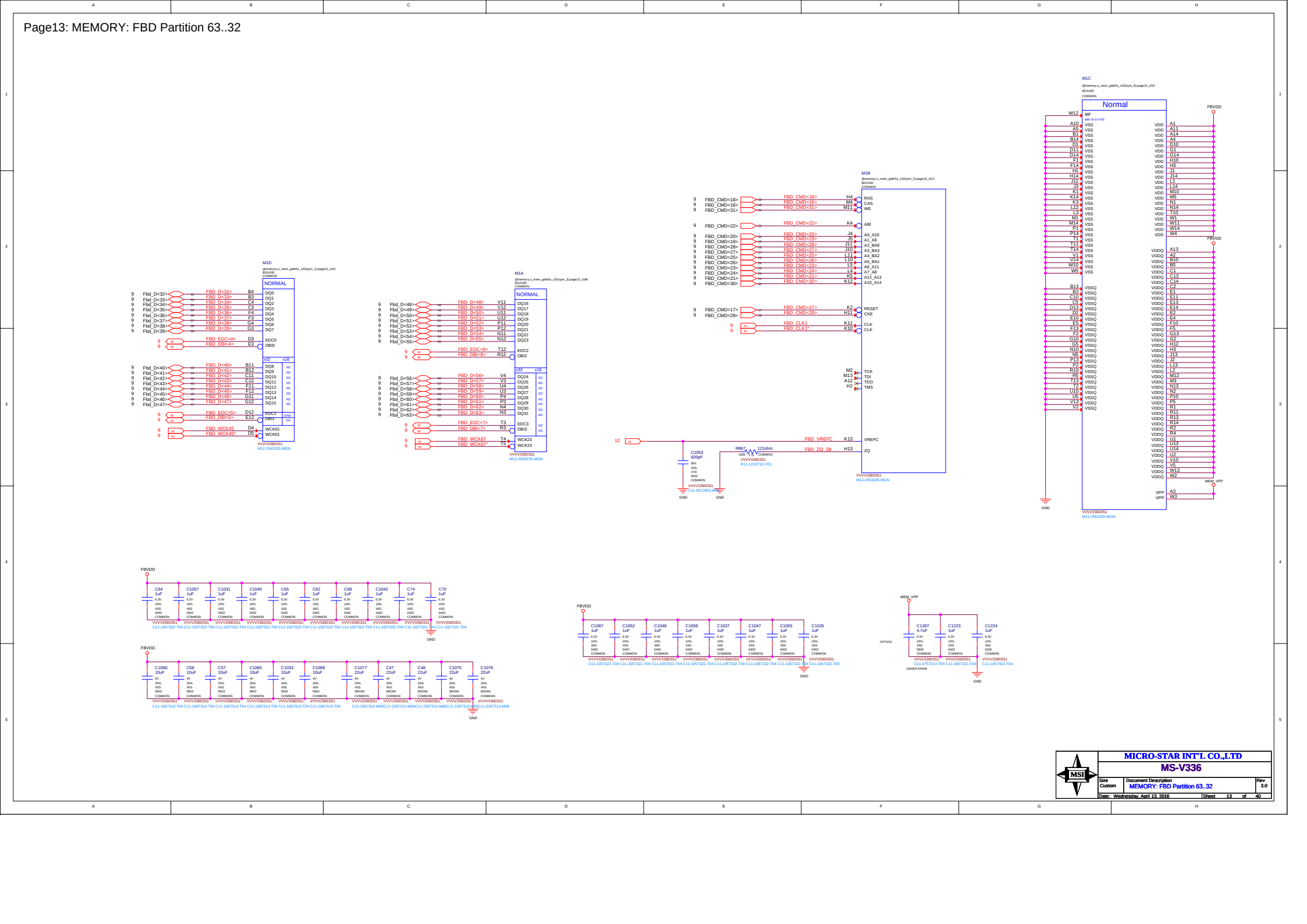
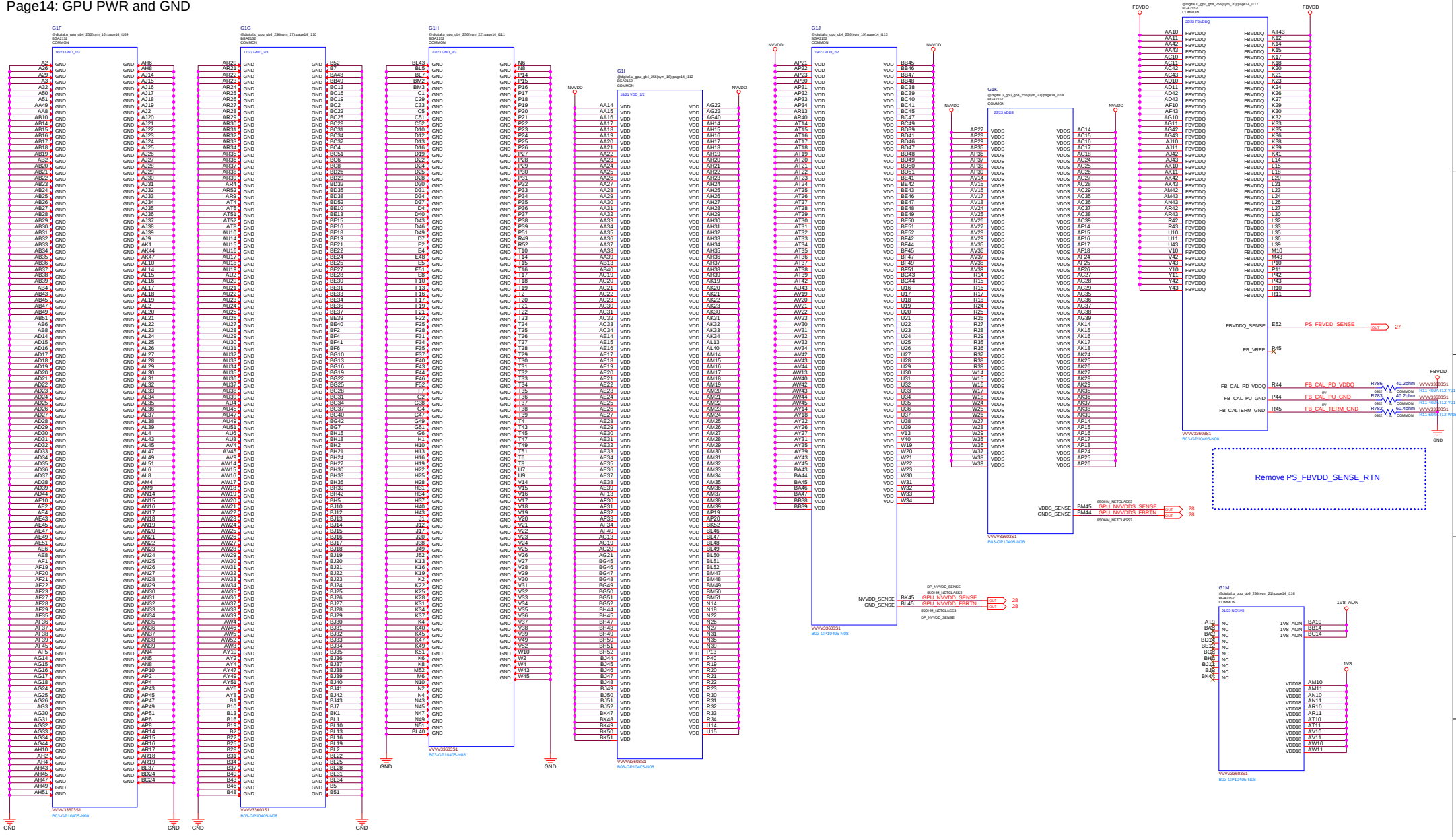


Page14: GPU PWR and GND



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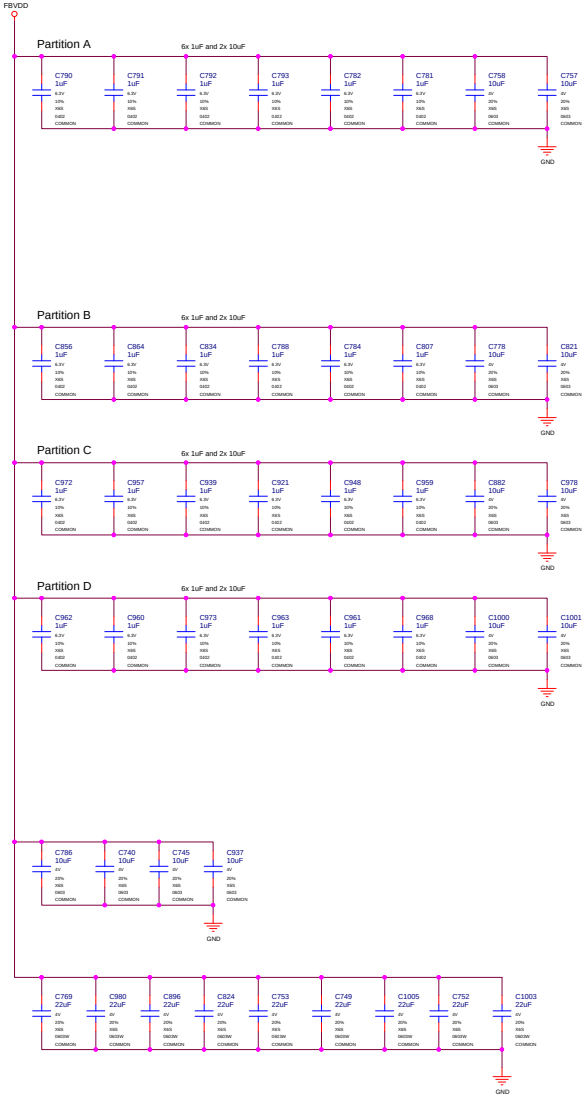
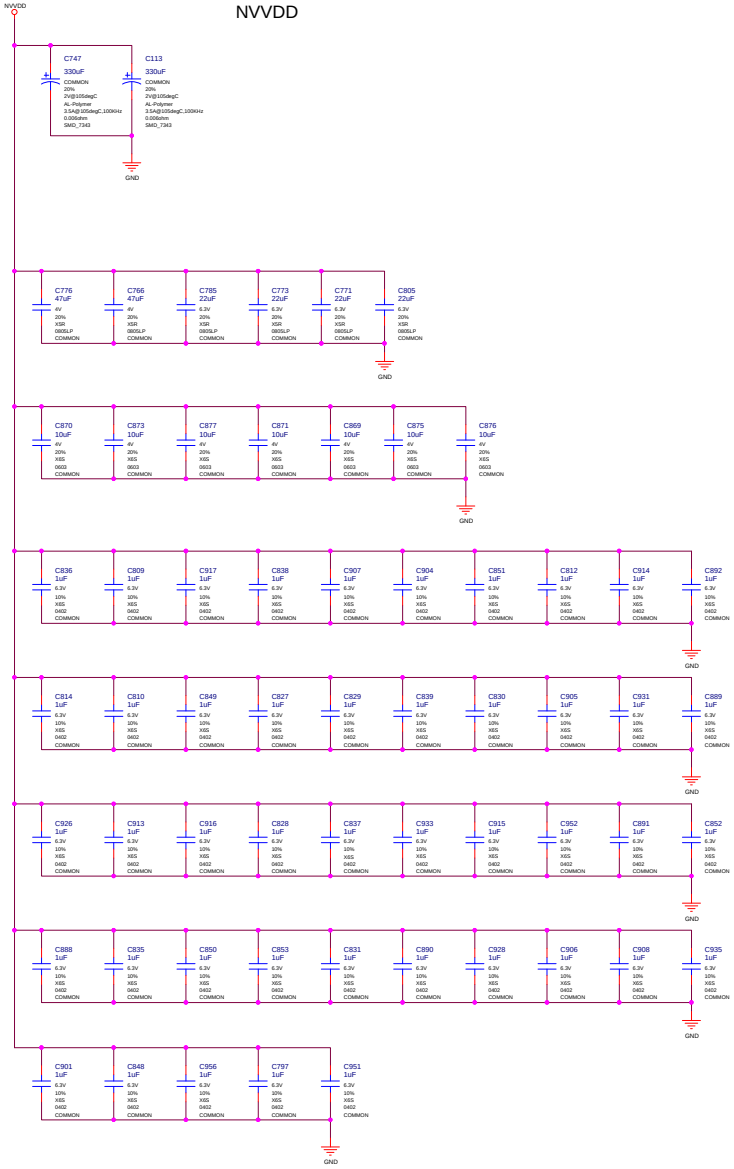
Page15: GPU Decoupling

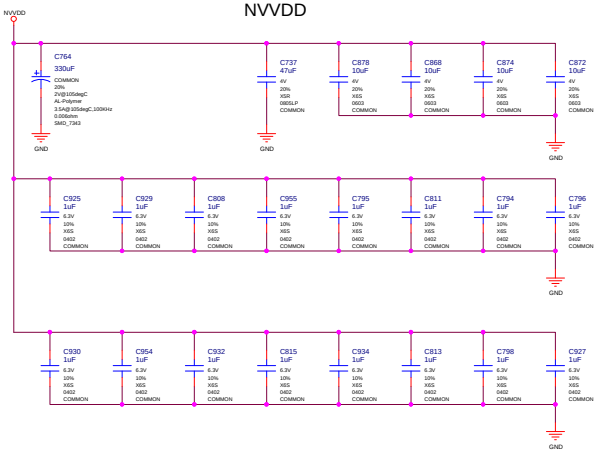
FBVDD

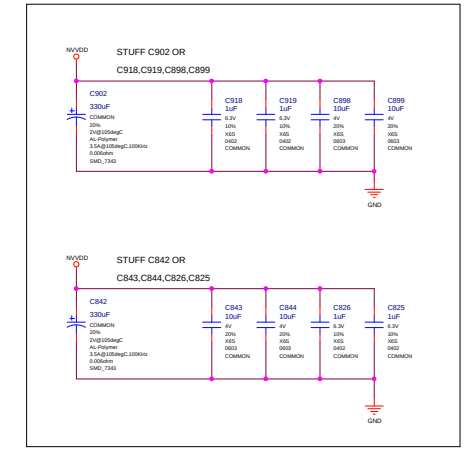


NVVDD

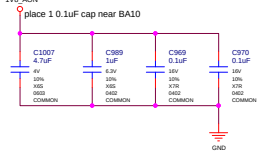


NVVDD



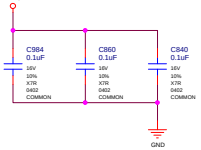


1V8_AON



place 1 0.1uf cap for BB14 and BC14 to share

VDD18



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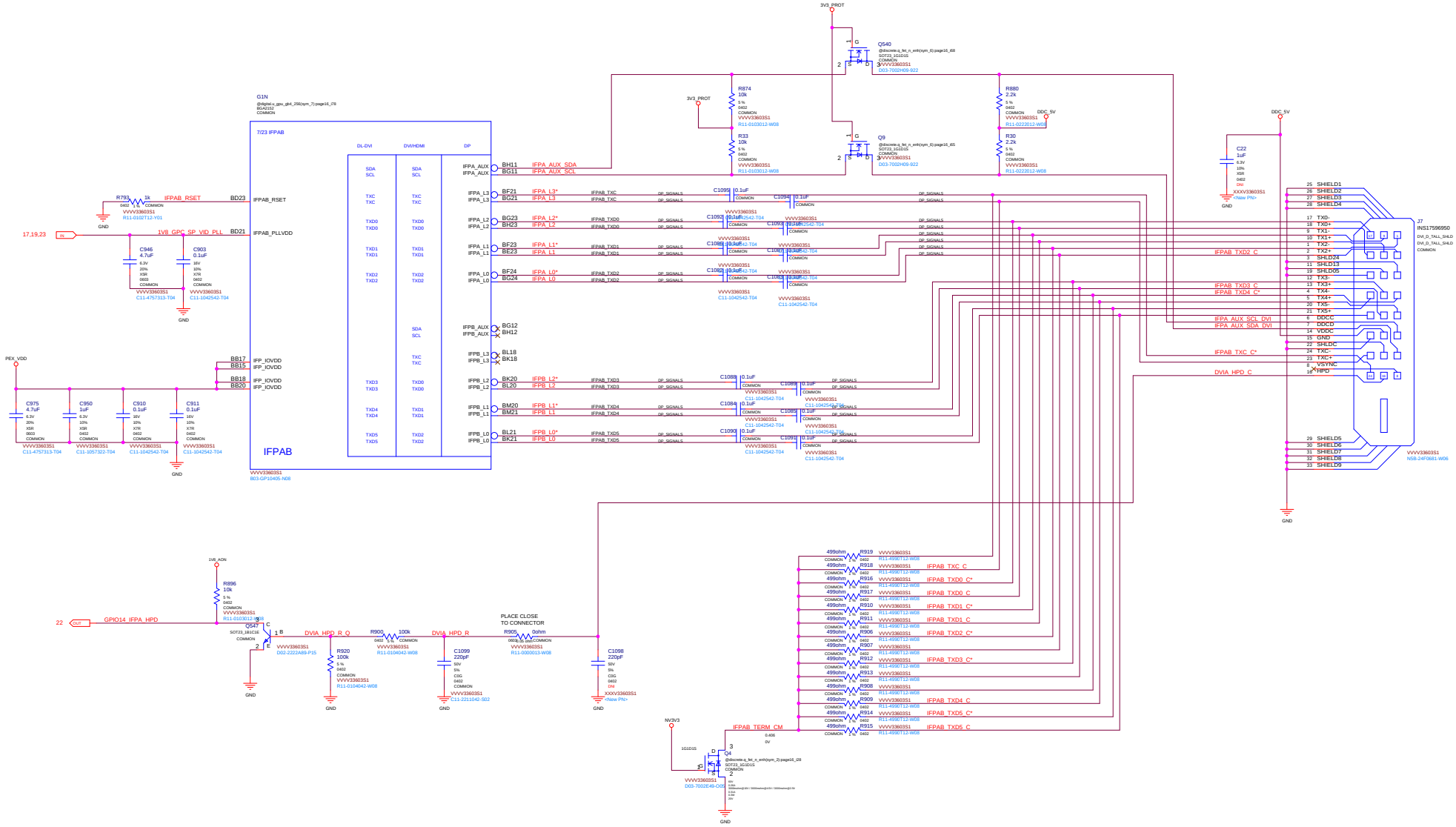
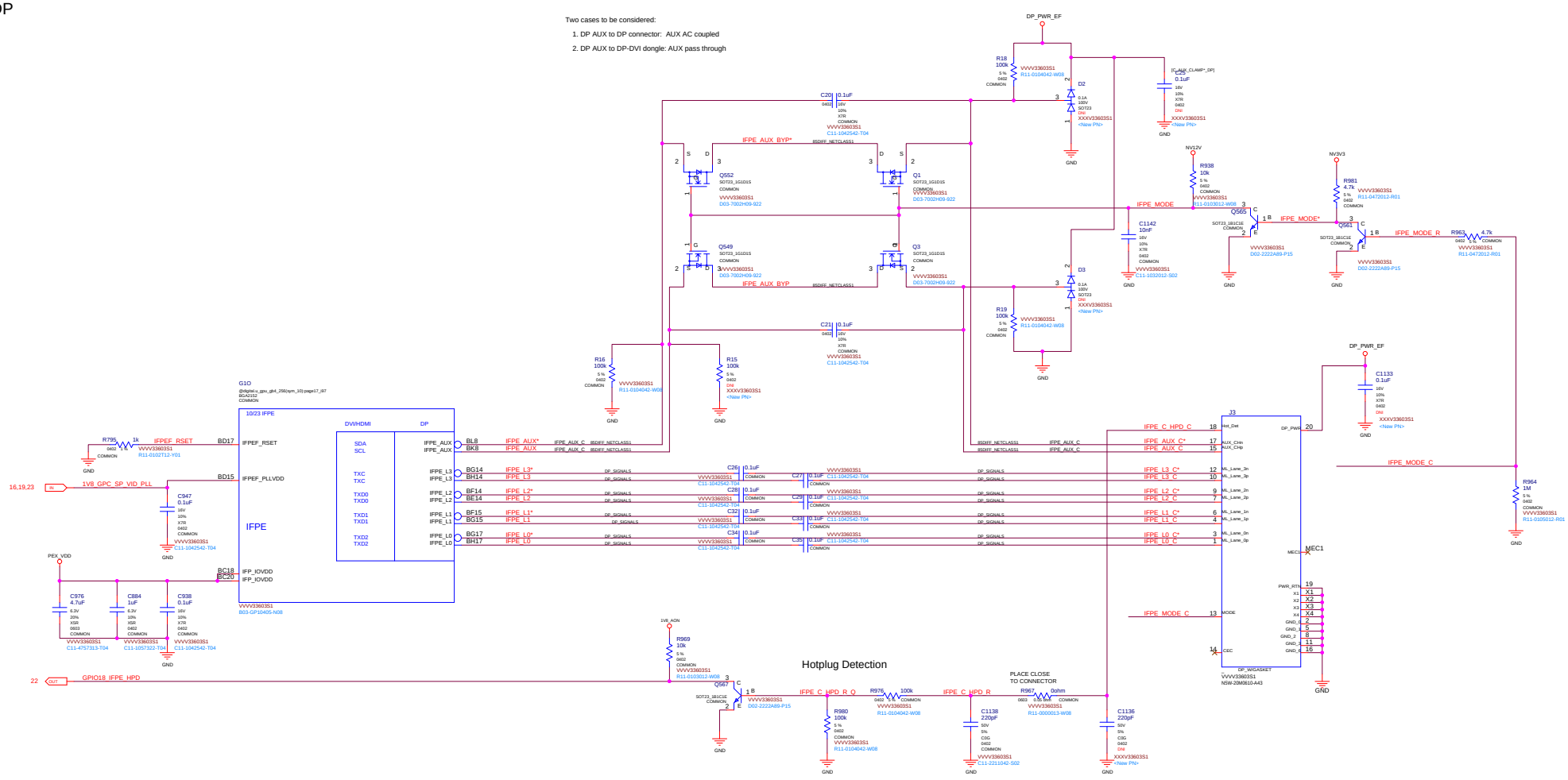
Page16: IFPAB DVI-D-DL

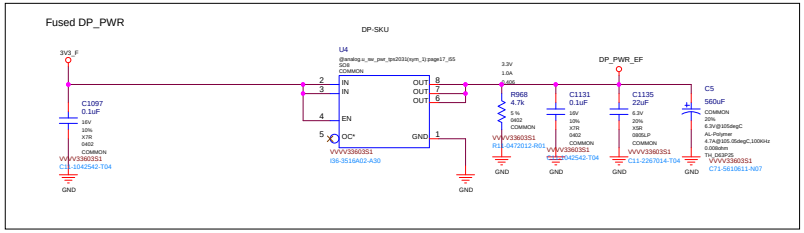


Page17: IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through





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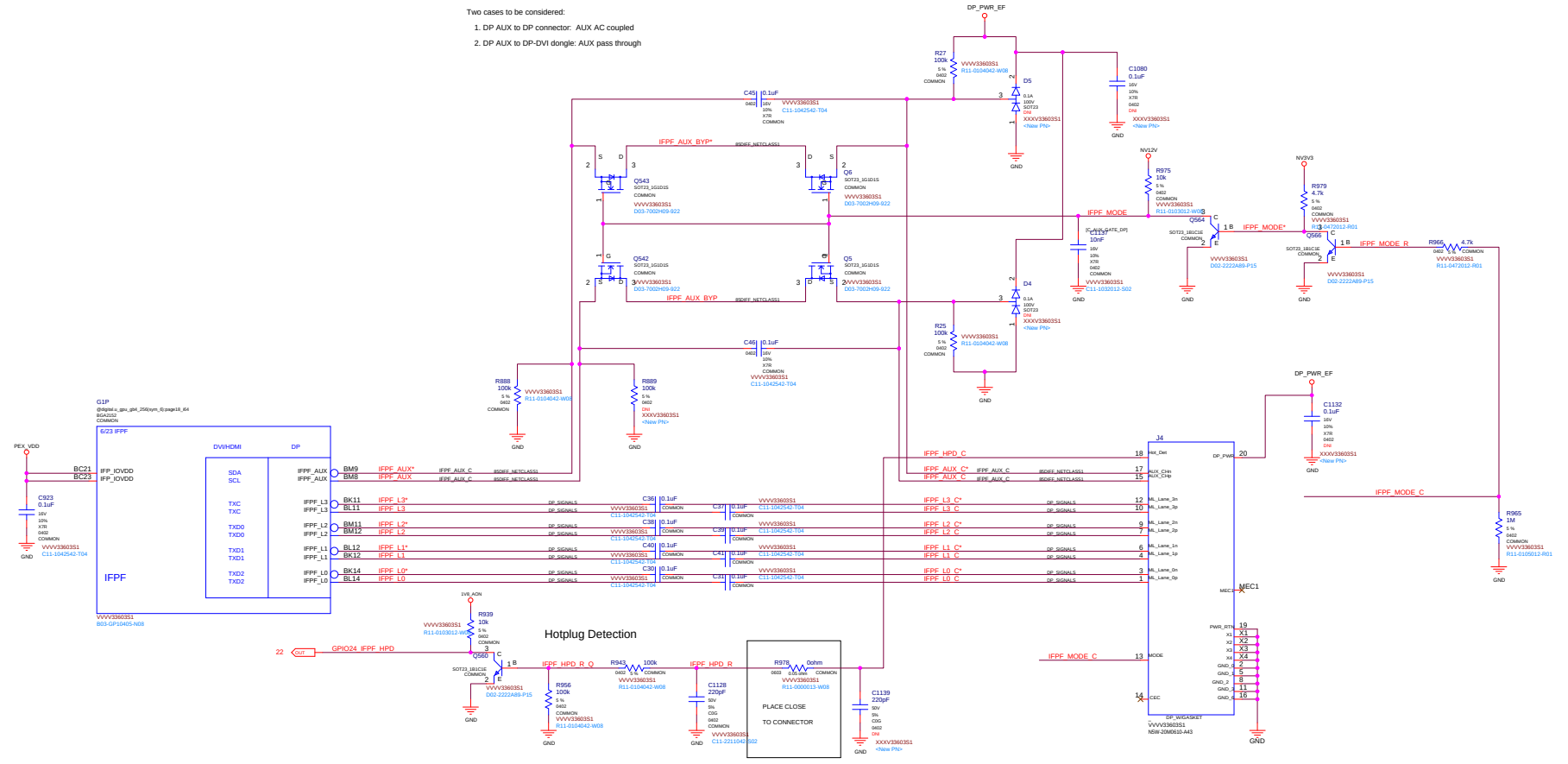
Page18: IFPF DP



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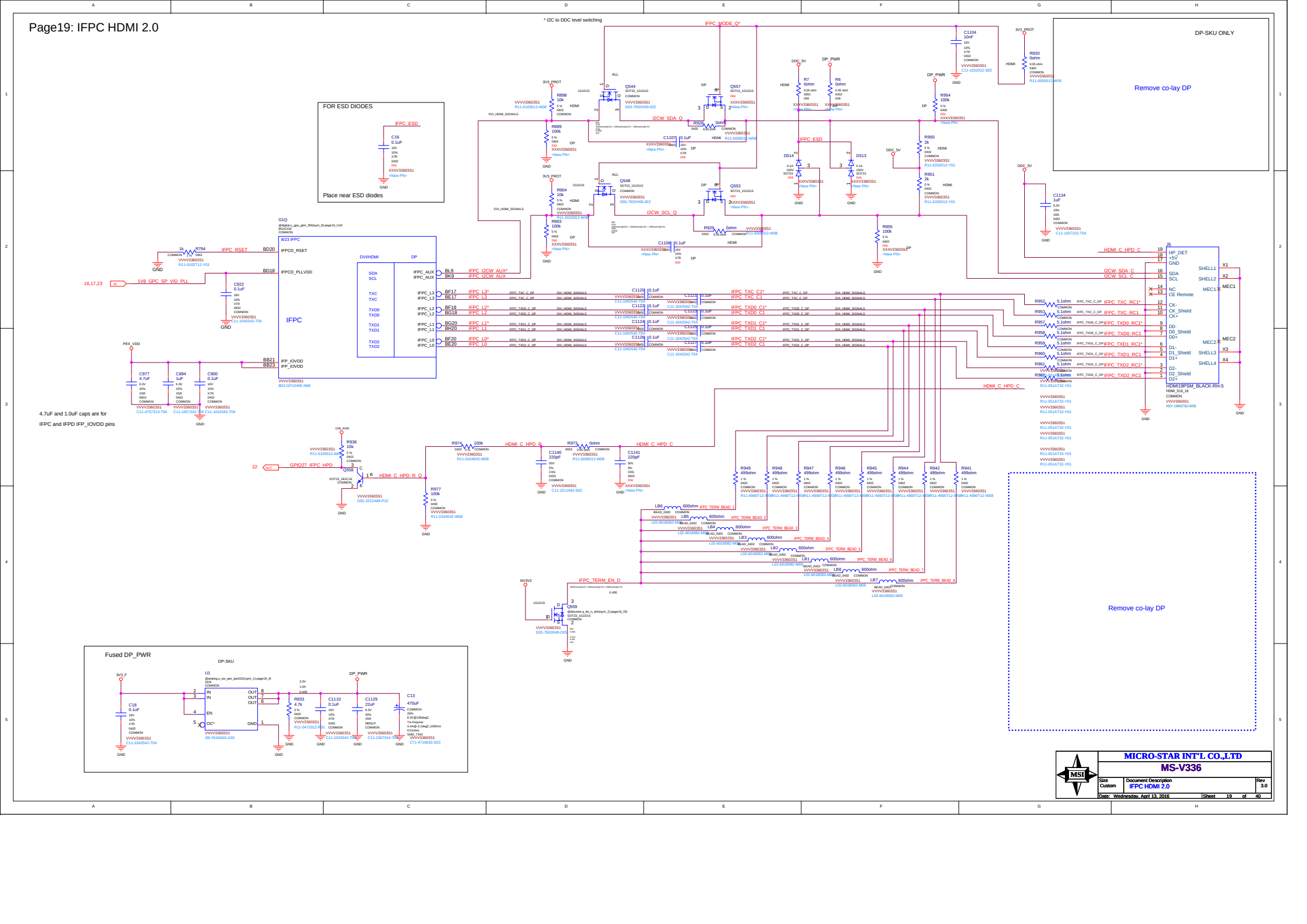
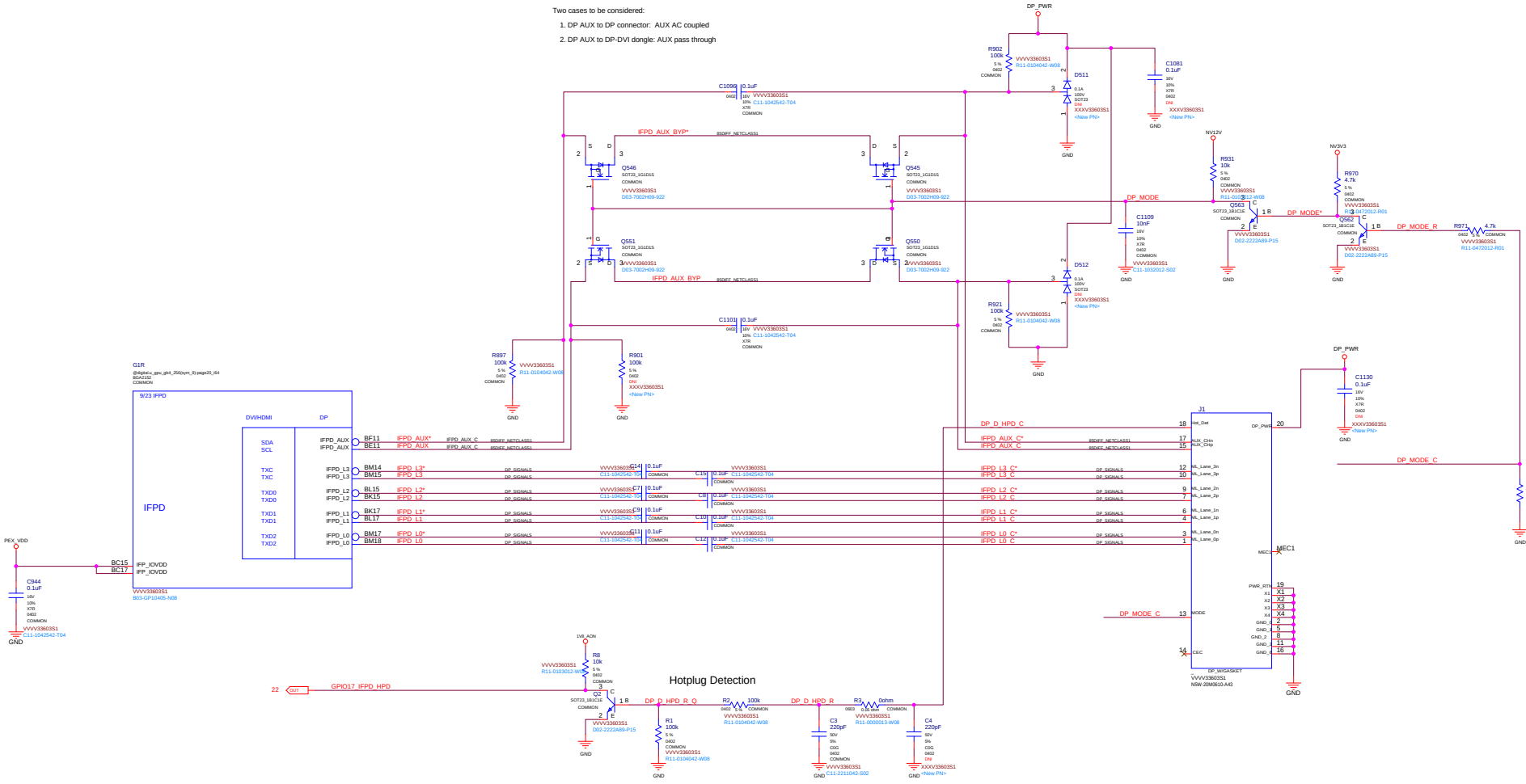
Page19: IFPC HDMI 2.0



Page20: IFPD DP



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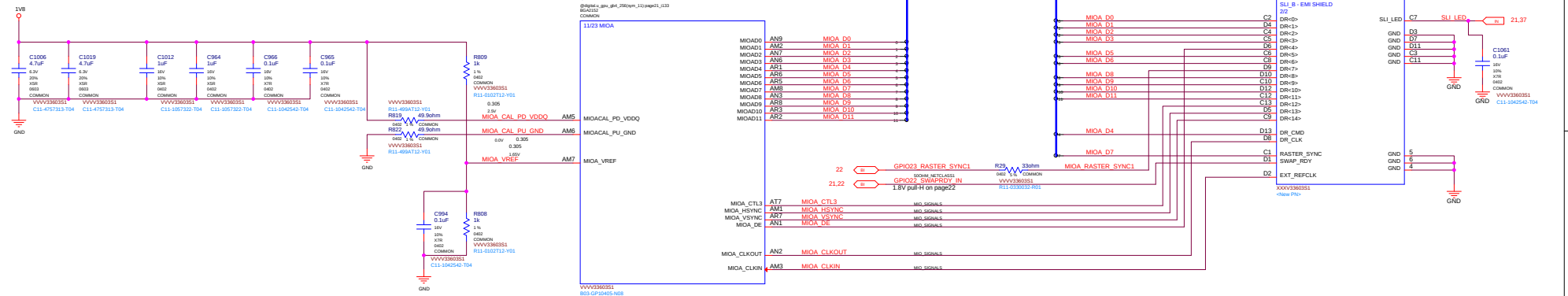
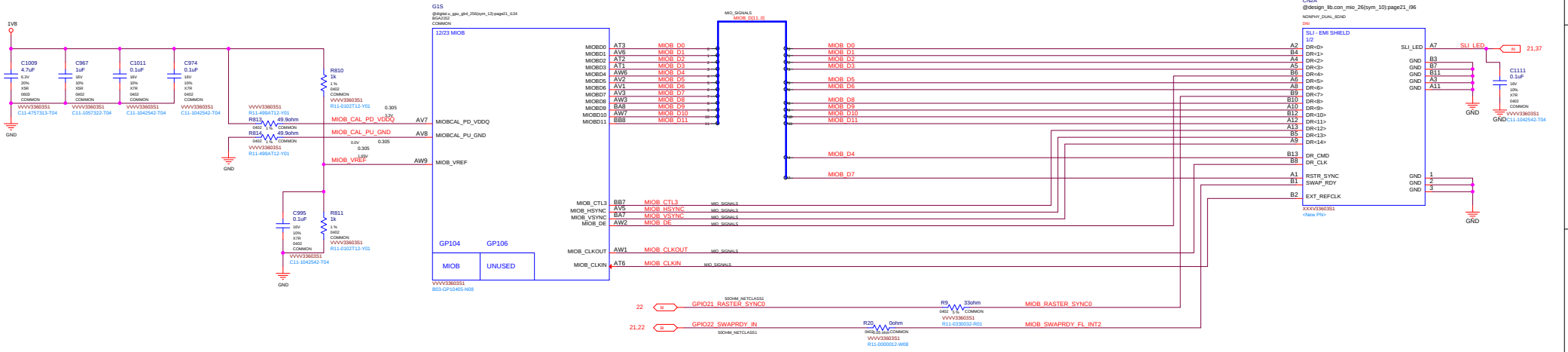
Page21: MIOA/B Interface





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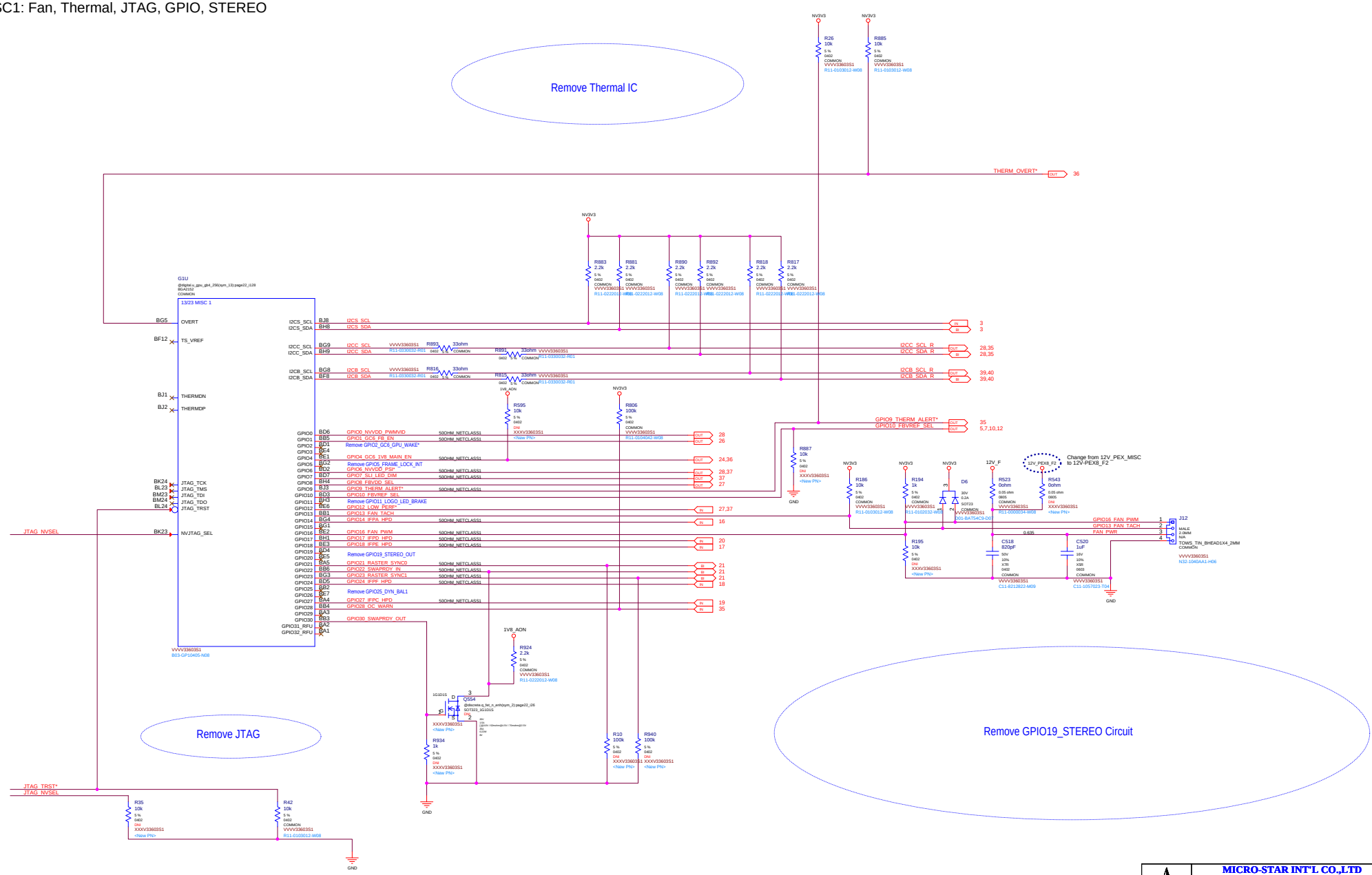
Page22: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



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Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

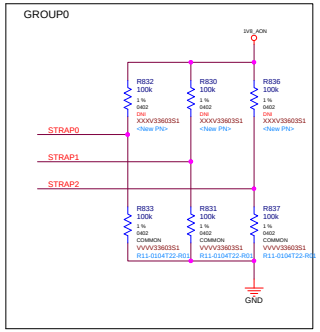
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

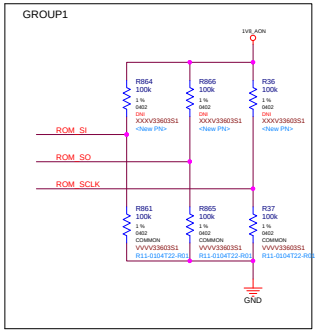
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

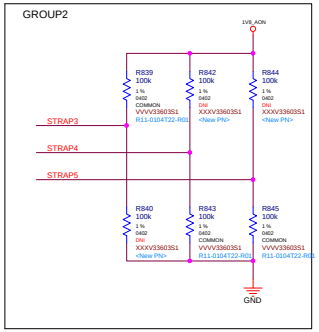
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

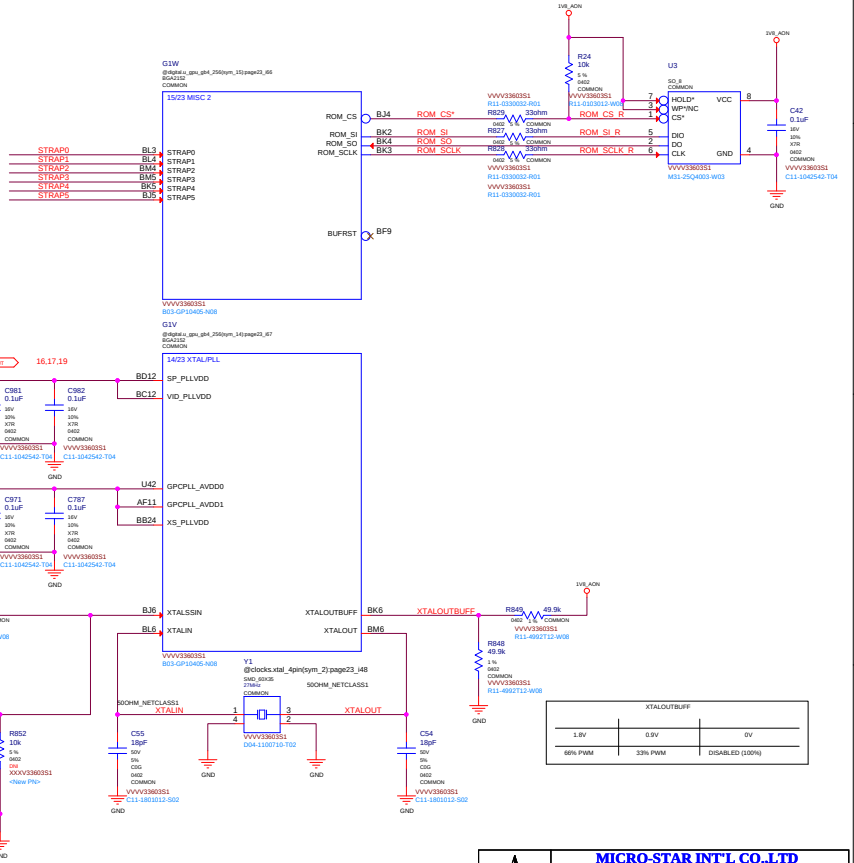
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







CFG[3:0]	Config Width	Vendor
0000	256Mx32 256-bit	Micron
0001	Reserved	
0010	Reserved	
0011	Reserved	
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	



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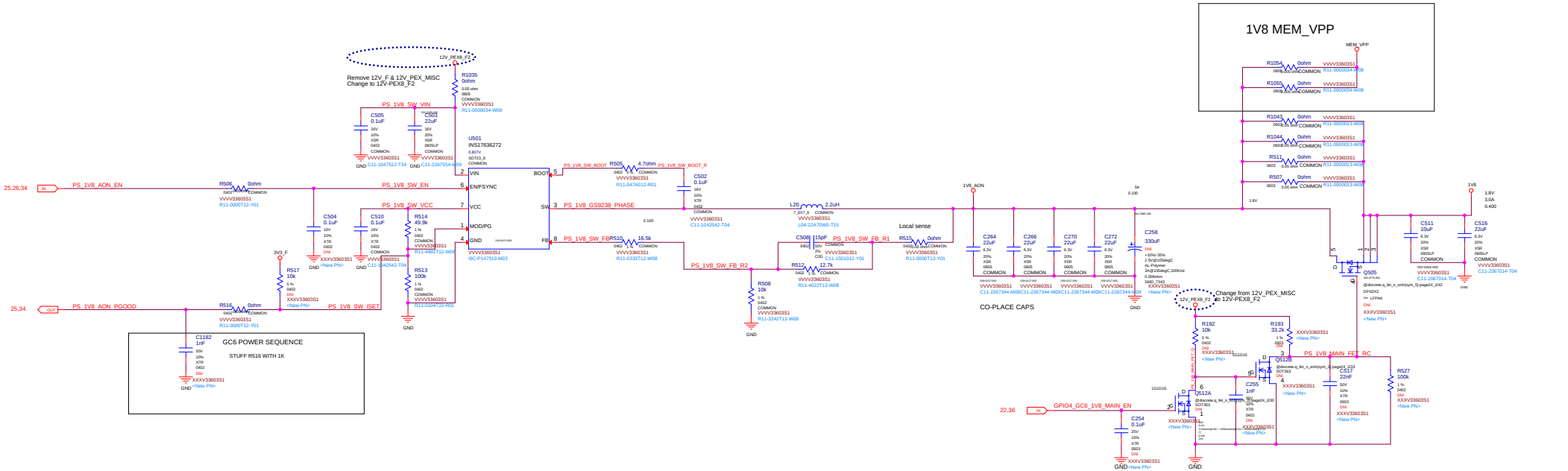
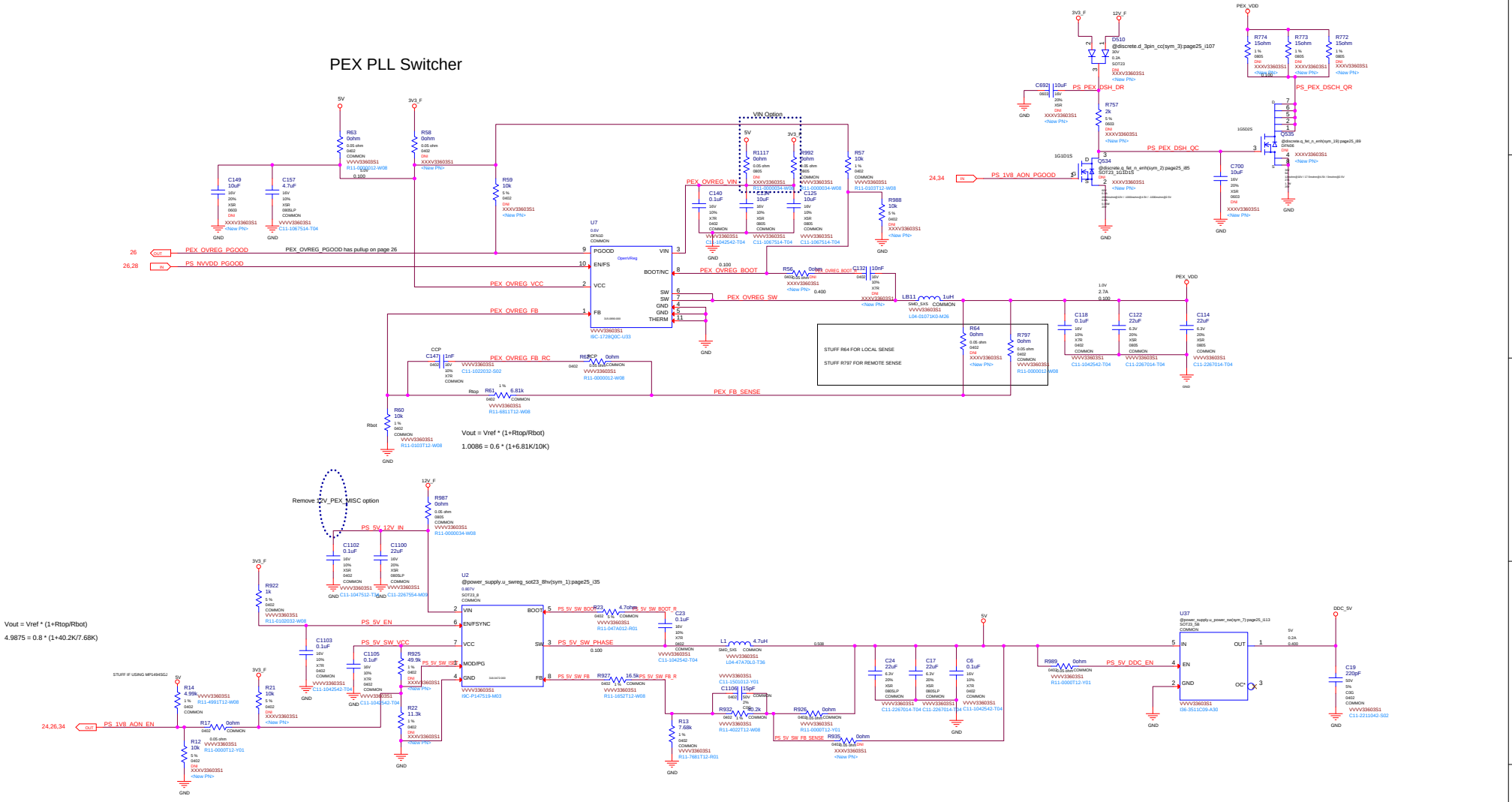
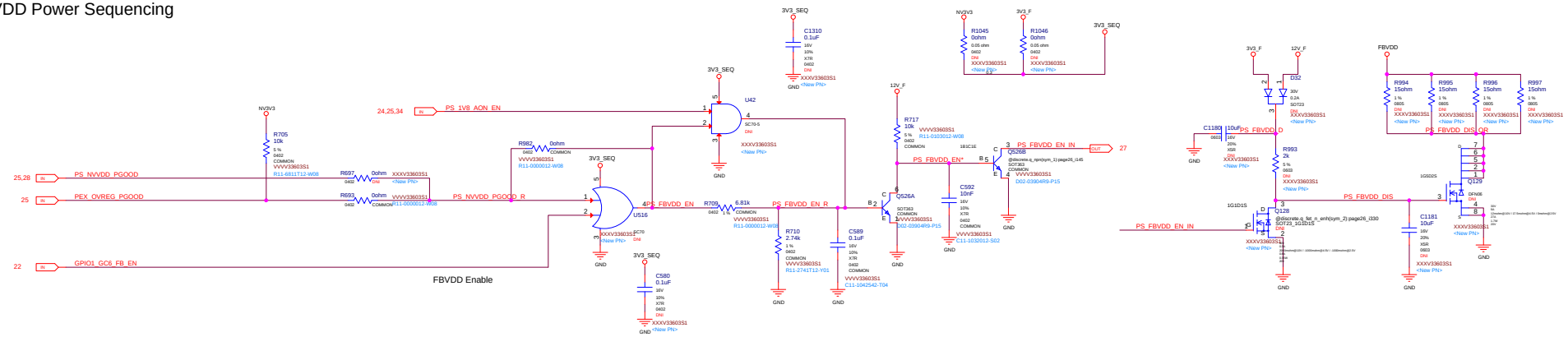
Page24: PS: 1V8, 1V8_AON



Page25: PS: 5V, PEX_VDD



Page26: PS: FBVDD Power Sequencing



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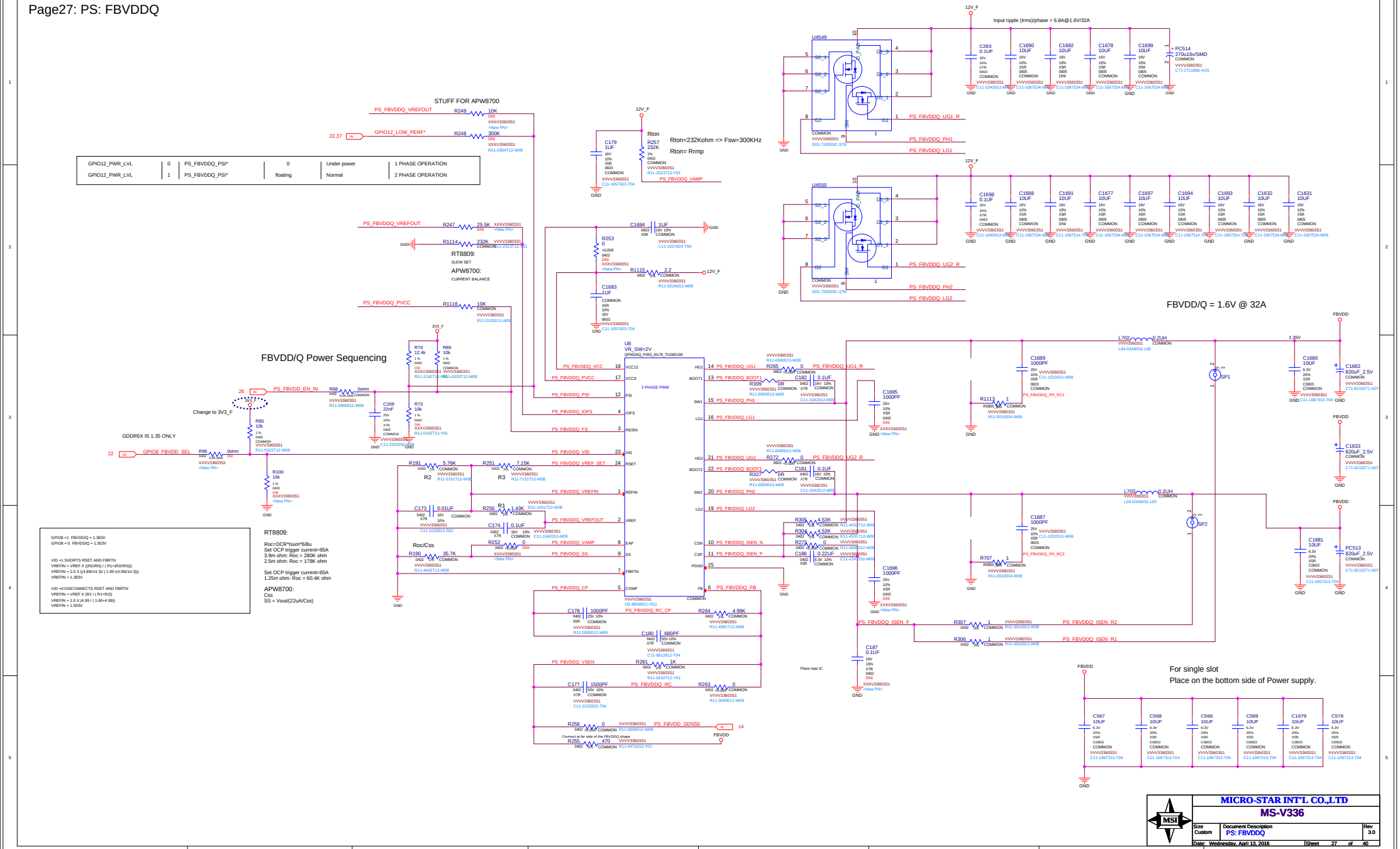
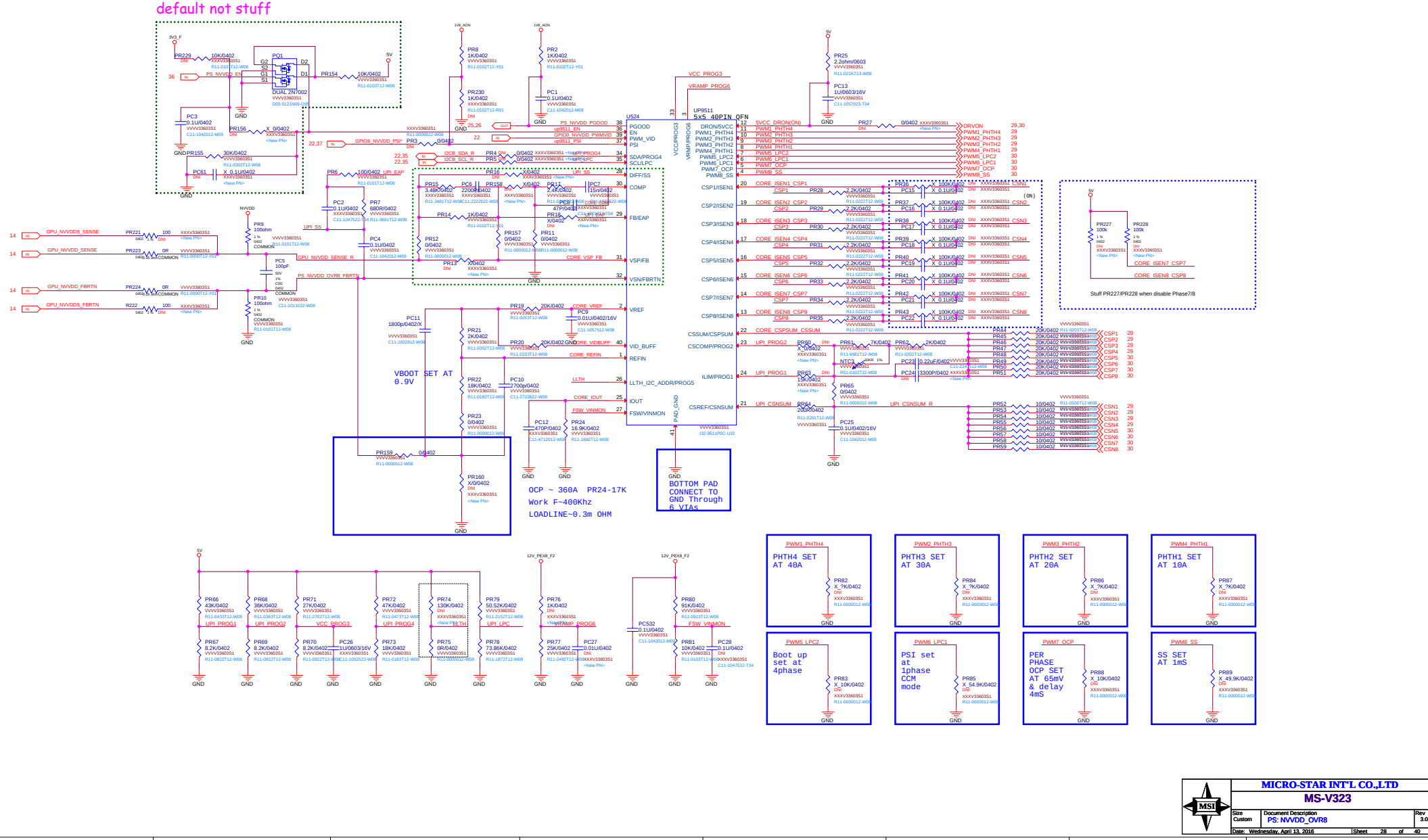
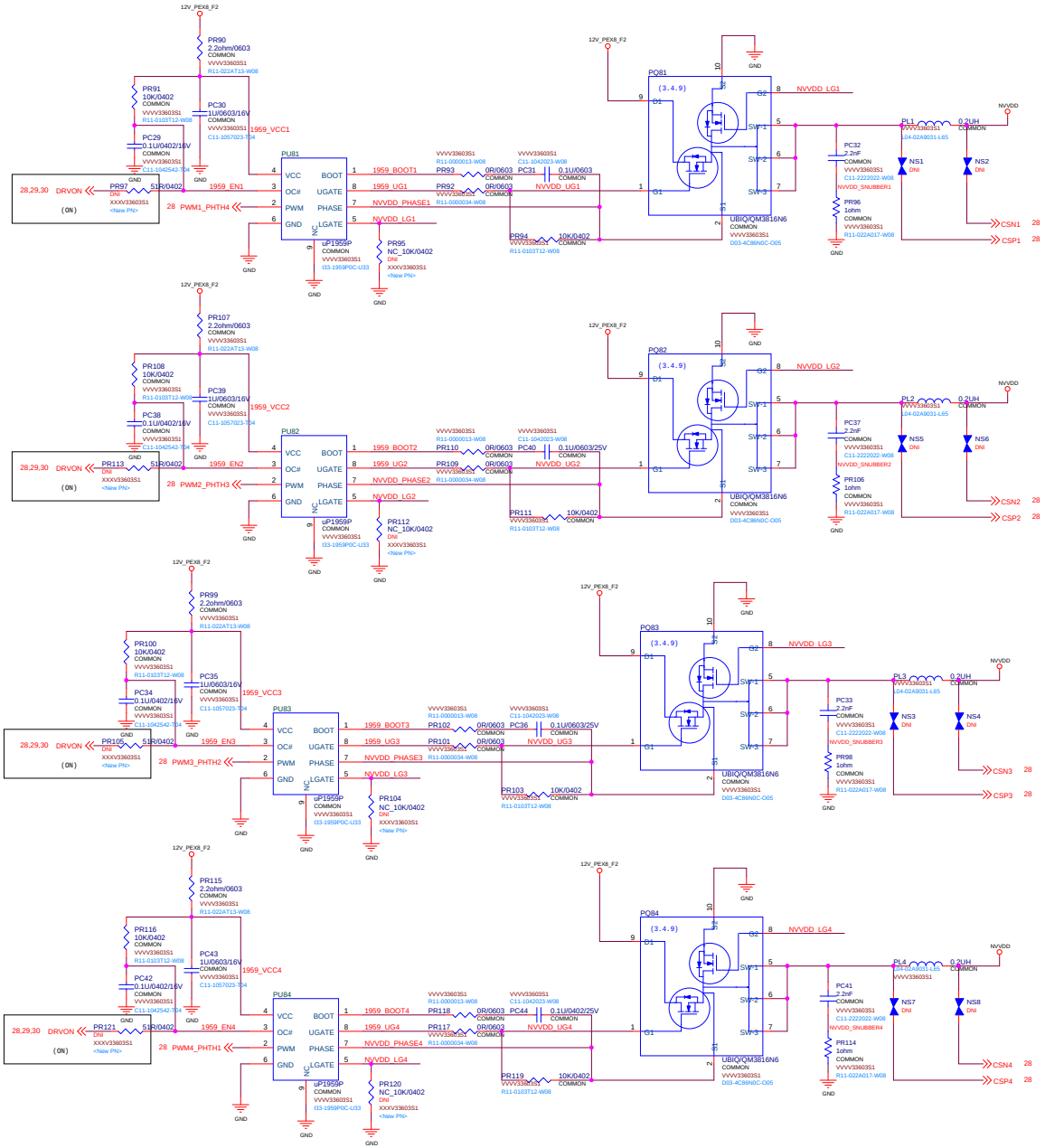
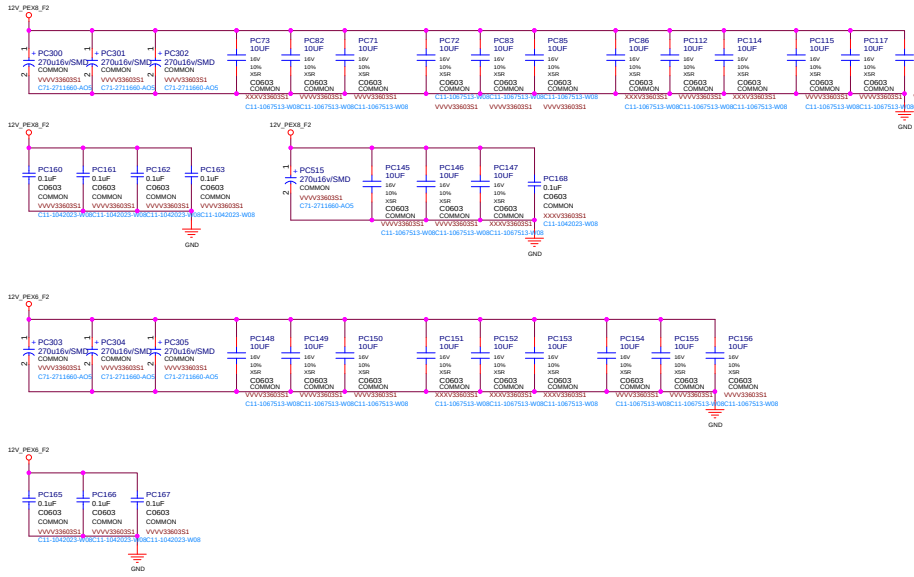
Page27: PS: FBVDDQ



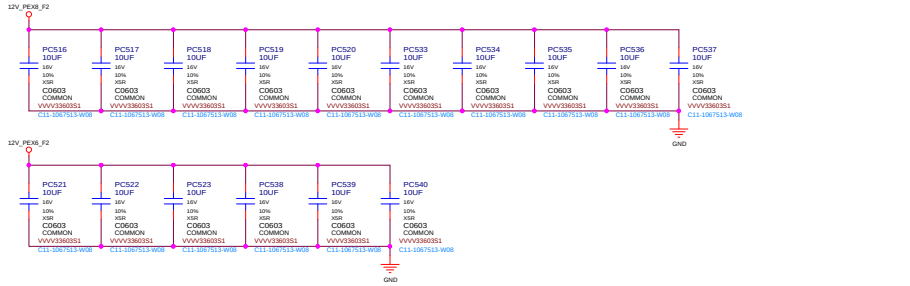

default not stuff
U524
UP9511
5x5 40PIN QFN
PGOOD
EN
PWM_VID
PSI
SDA/PROG4
SCL/LPC
DIFF/SS
COMP
FB/EAP
VSP/FB
VSN/FBRTN
VREF
VID_BUFF
REFIN
LLTH_I2C_ADDR/PROG5
IOUT
FSW/VINMON
CSSUM/CSPSUM
CSCOMP/PROG2
ILIM/PROG1
CSREF/CSNSUM
PAD_GND
VBOOT SET AT 0.9V
OCP ~ 360A PR24-17K
Work F~400Khz
LOADLINE~0.3m OHM
BOTTOM PAD CONNECT TO GND Through 6 VIAs
PWM1_PHTH4
PHTH4 SET AT 40A
PWM2_PHTH3
PHTH3 SET AT 30A
PWM3_PHTH2
PHTH2 SET AT 20A
PWM4_PHTH1
PHTH1 SET AT 10A
PWM5_LPC2
Boot up set at 4phase
PWM6_LPC1
PSI set at 1phase CCM mode
PWM7_OCP
PER PHASE OCP SET AT 65mV & delay 4mS
PWM8_SS
SS SET AT 1mS
Stuff PR227/PR228 when disable Phase7/8
MICRO-STAR INT'L CO.,LTD
MS-V323
PS: NVVDD_OVR8
Wednesday, April 13, 2016



EXT_12V Input CAP



EXT_12V Input CAP(Backup)



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V336	
Size: Custom	Document Description: PS: NVVDD Phase 1-4	Rev: 3.0
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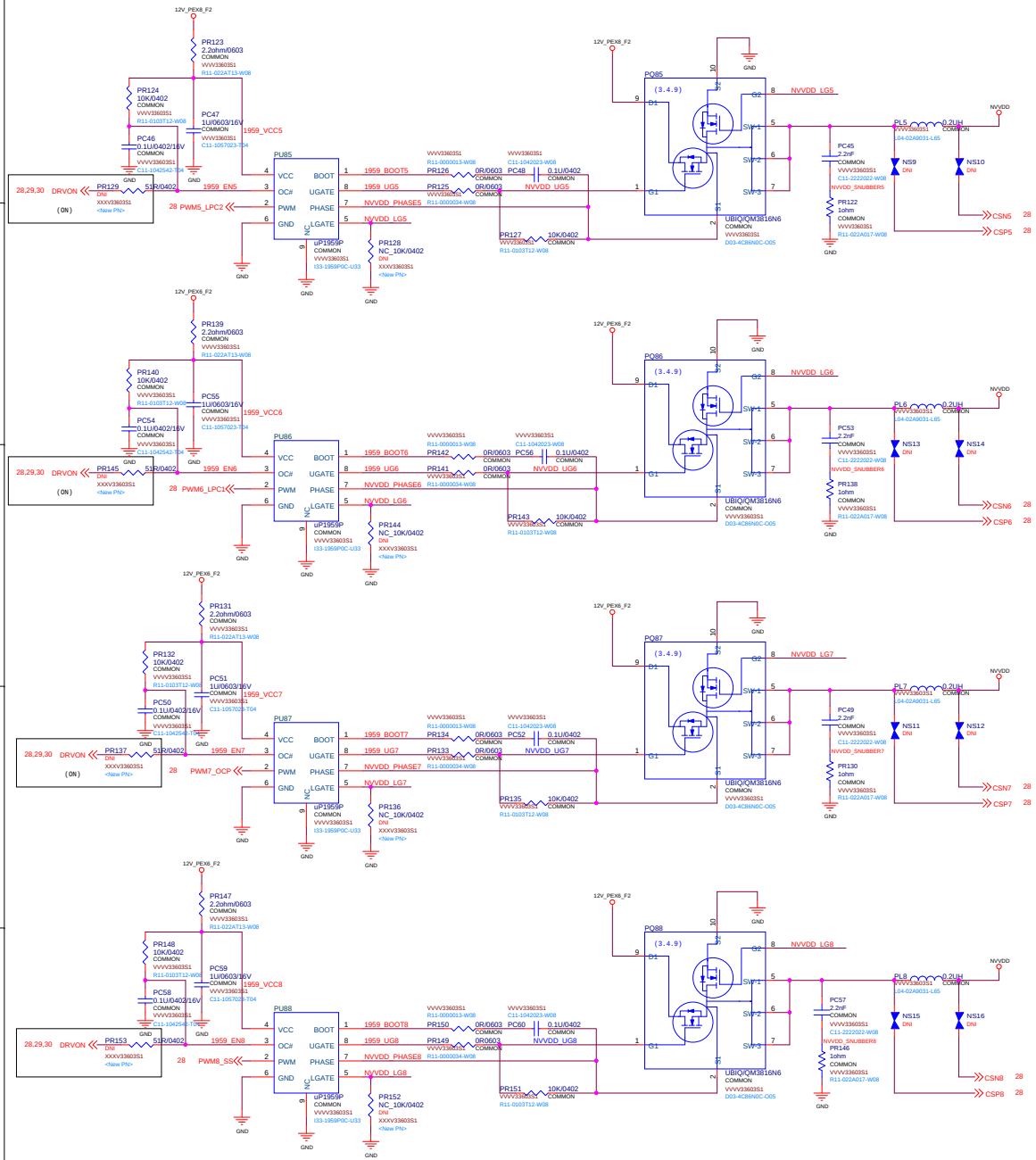
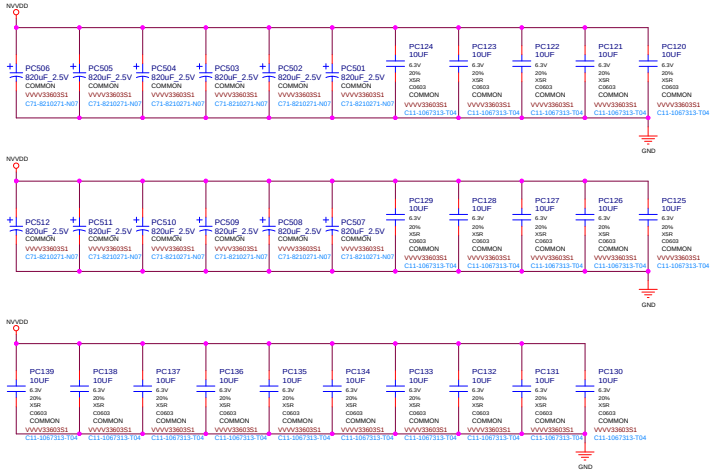
Page30: PS: NVVDD Phase 5-8



NVVDD Output CAP



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MS-V336		
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Page31: PS: Blank Page

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MS-V336	
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Page32: PS: Dynamic Power Balance Phases

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Page33: PS: Dynamic Power Balance Logic

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MS-V336	
Size: Custom	Document Description: PS: Dynamic Power Balance Logic
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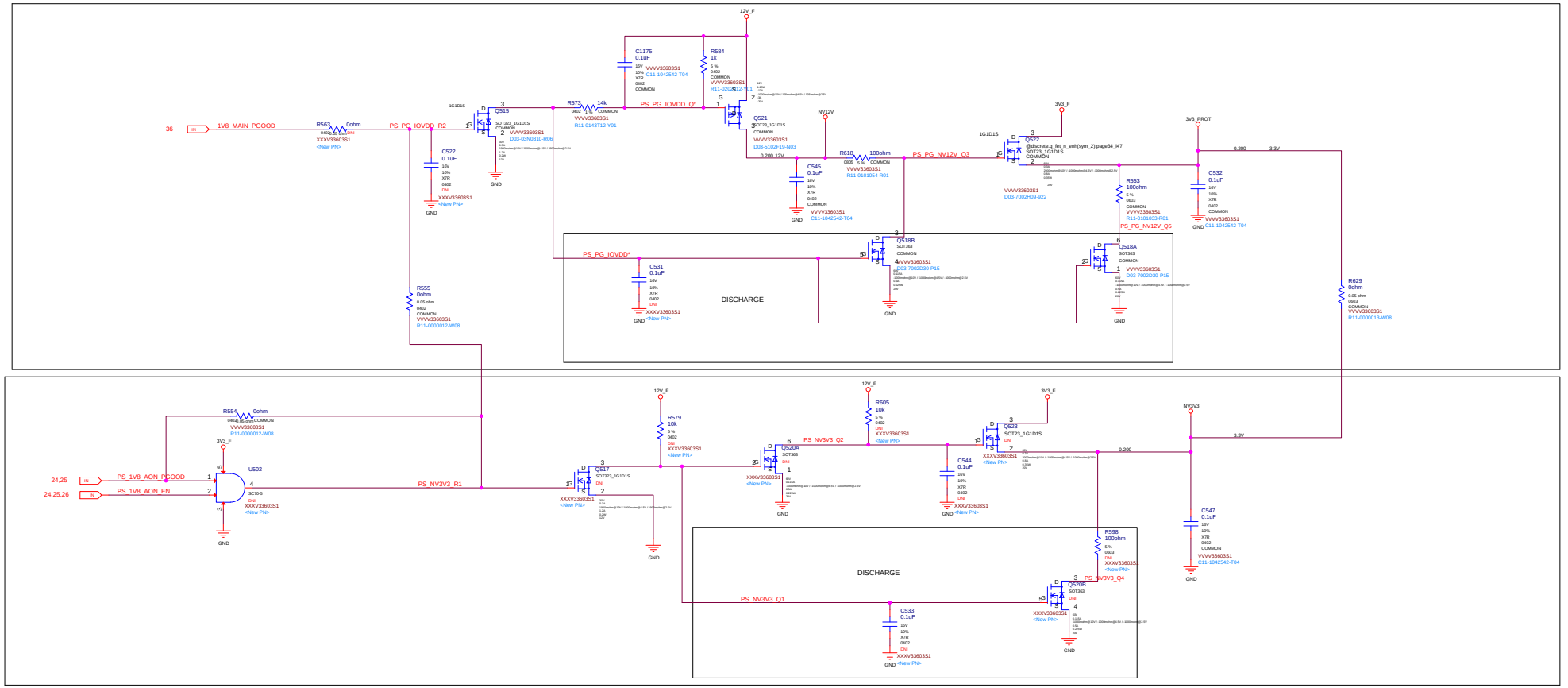
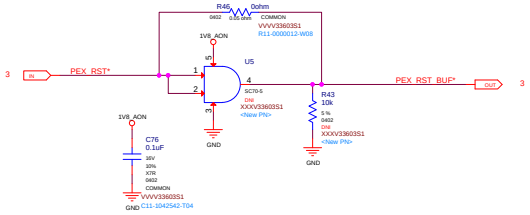
Page34:PS: NV3V3, NV12V





Remove

MICRO-STAR INT'L CO.,LTD		
MS-V336		
Size: Custom	Document Description: PS: NV3V3, NV12V	Rev: 3.0
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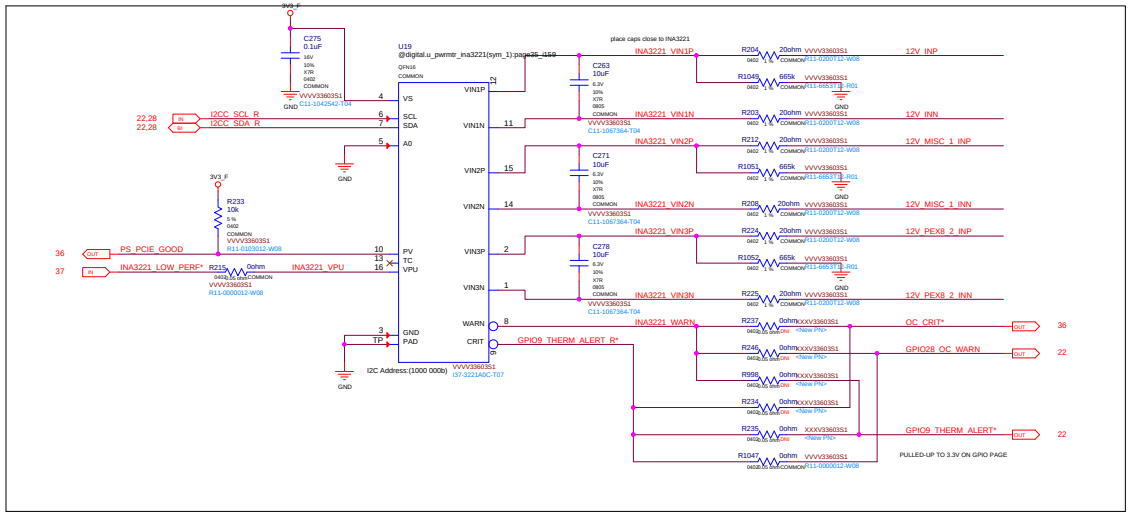
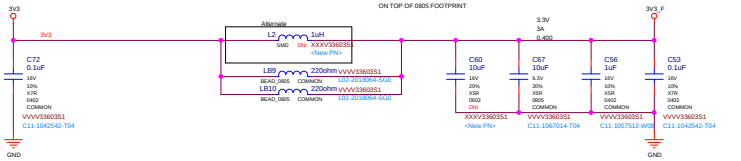
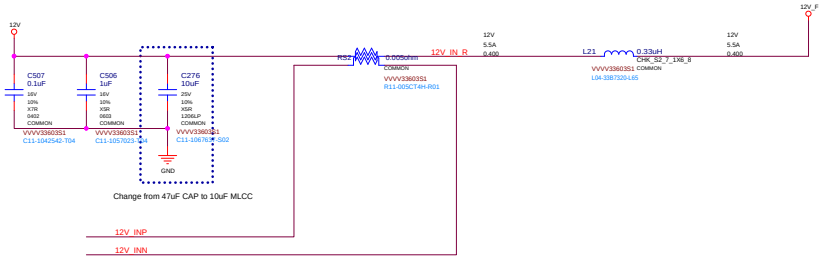
Page35: PS: Inputs, Filtering, and Monitoring

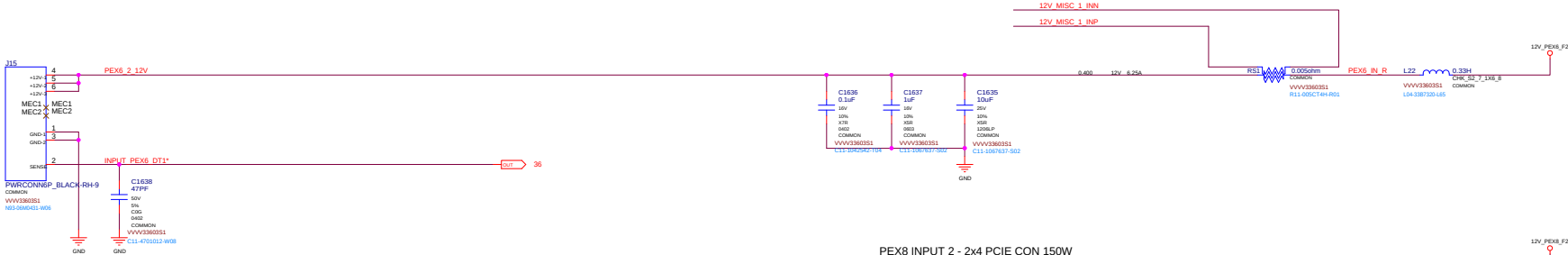


PEX 3V3 INPUT - 10W

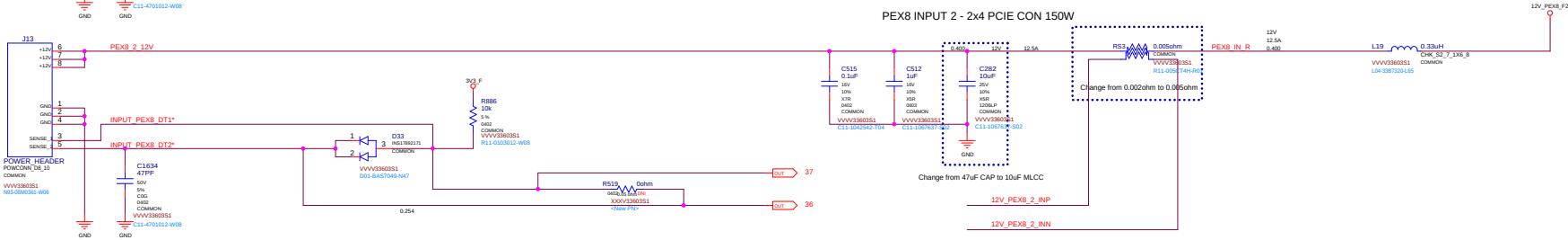


PEX_12V INPUT - 66W





PEX8 INPUT 2 - 2x4 PCIE CON 150W



STUFF FOR 6-PIN CONNECTOR
OR REVERSE CPU 8-PIN CONNECTOR

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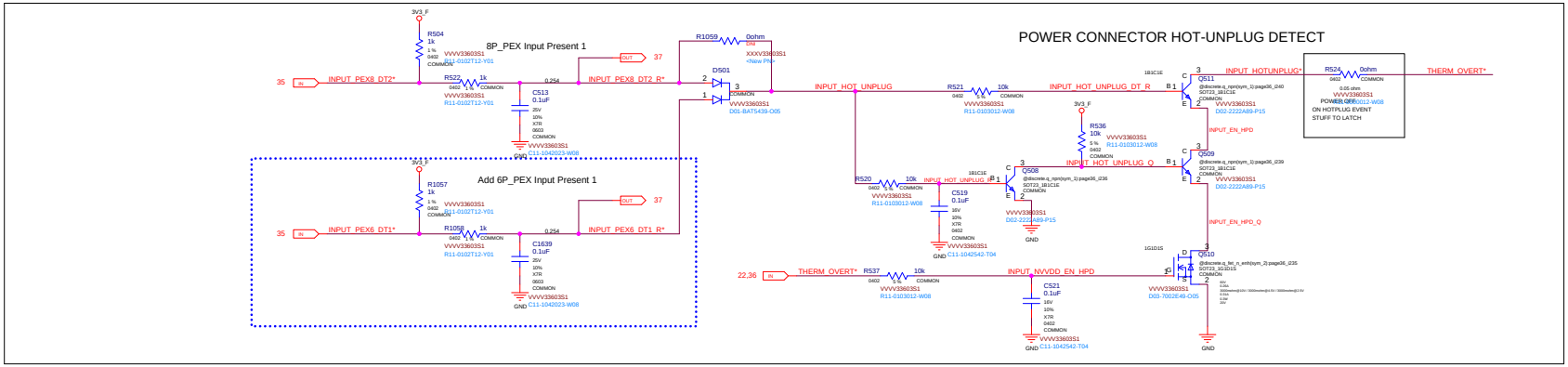
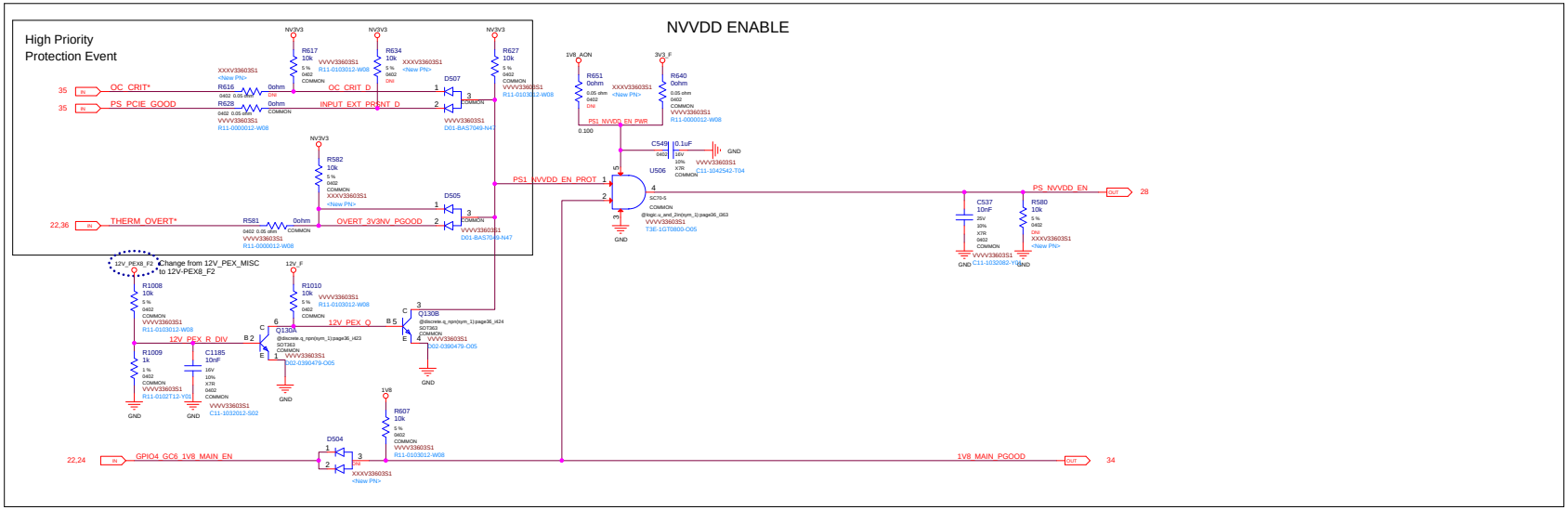
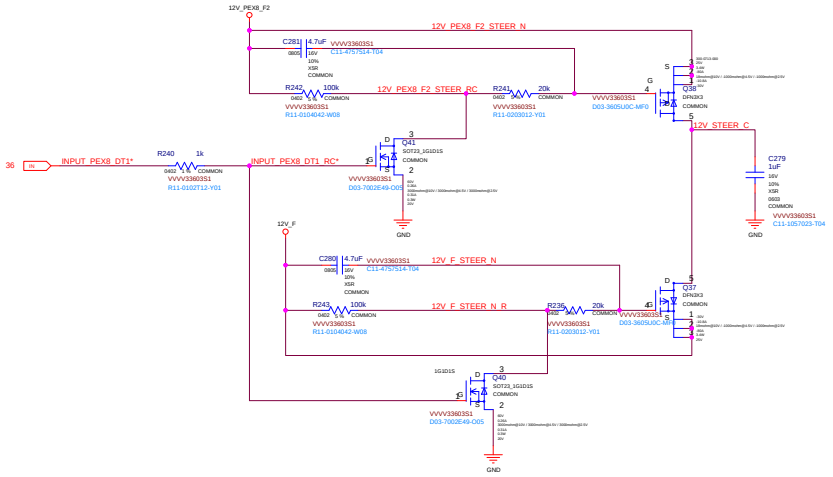

8P_PEX Input Present 1
Add 6P_PEX Input Present 1
POWER CONNECTOR HOT-UNPLUG DETECT
INPUT_PEX8_DT2*
INPUT_PEX8_DT2_R*
INPUT_PEX6_DT1*
INPUT_PEX6_DT1_R*
INPUT_HOT_UNPLUG
INPUT_HOT_UNPLUG_DT_R
INPUT_HOT_UNPLUG_Q
INPUT_HOTUNPLUG*
THERM_OVERT*
INPUT_EN_HPD
INPUT_EN_HPD_Q
INPUT_NVDD_EN_HPD
POWER OFF ON HOTPLUG EVENT
STUFF TO LATCH

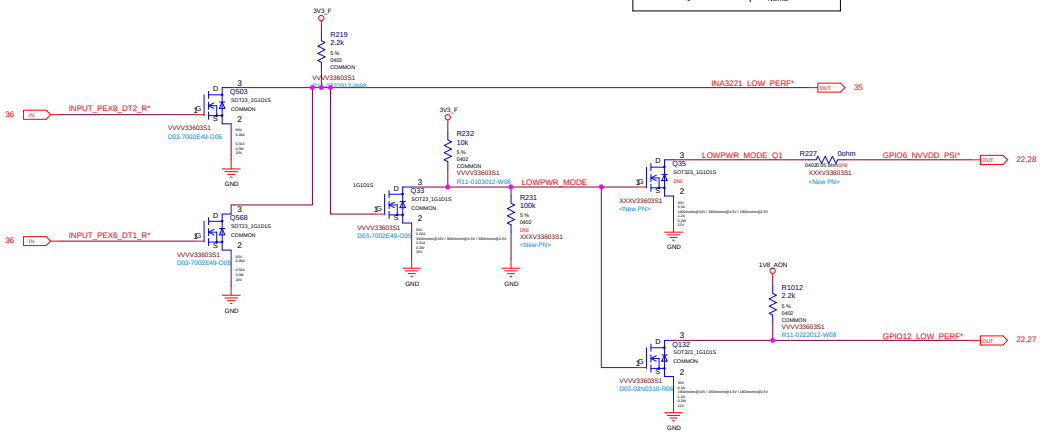

High Priority
Protection Event
NVDD ENABLE
OC_CRIT*
PS_PCIE_GOOD
THERM_OVERT*
OC_CRIT_D
INPUT_EXT_PRSNT_D
OVERT_3V3NV_PGOOD
PS1_NVDD_EN_PROT
PS1_NVDD_EN_PWR
PS_NVDD_EN
12V_PEX8_F2
Change from 12V_PEX_MISC
to 12V-PEX8_F2
12V_PEX_R_DIV
12V_PEX_Q
GPIO4_GC6_1V8_MAIN_EN
1V8_MAIN_PGOOD

Page37: PS: 12V Current Steering, PSI Control, and LED

PEX Input - 12V Current Steering FETs



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

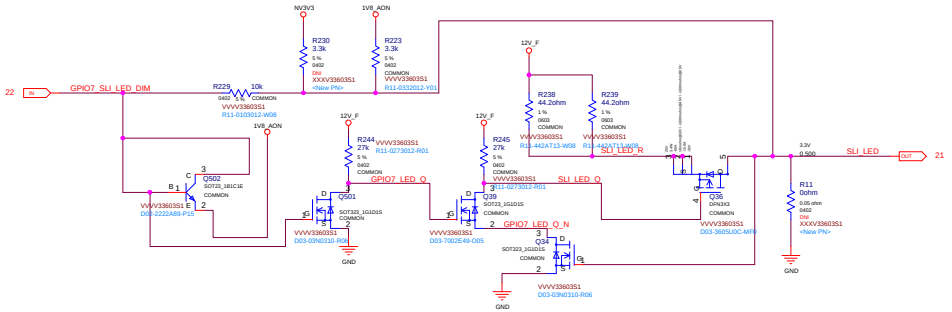
Remove POWER BRAKE

GeForce Logo LED

LED HEADER
(C0MM0N)

Remove Logo LED

SLI LED (GEFORCE ONLY)



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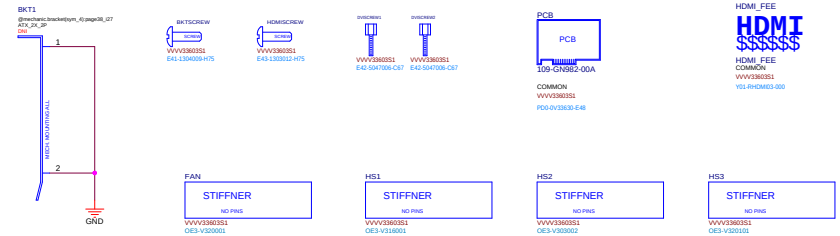
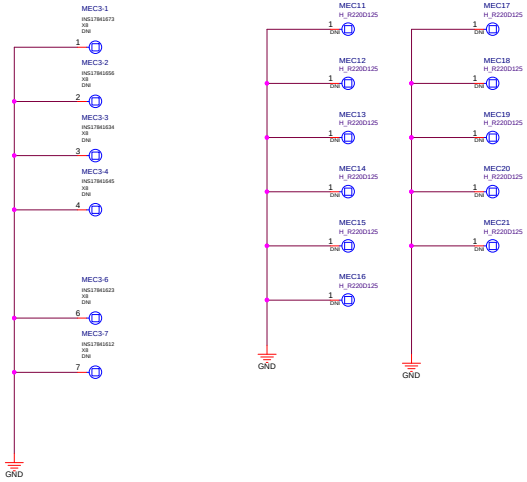
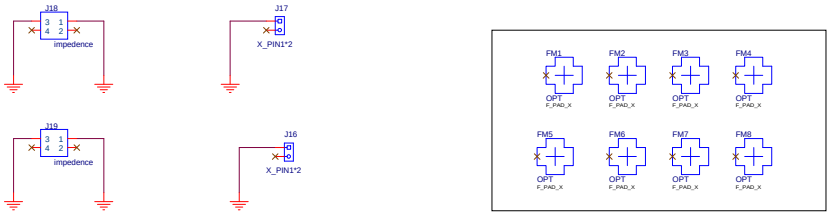
Page38: Mechanical: Bracket/Thermal Solution

Brackets:



GPU Stiffner





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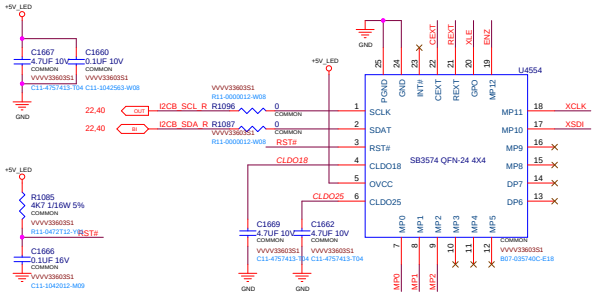
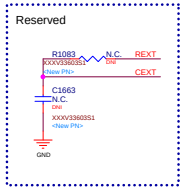
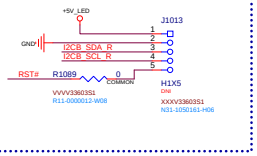
Page39: LED_CONTROLLER_ENE3574



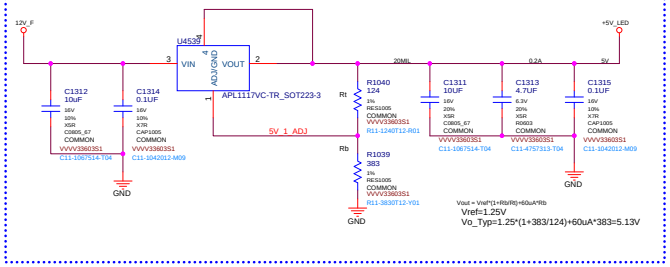
Reserved



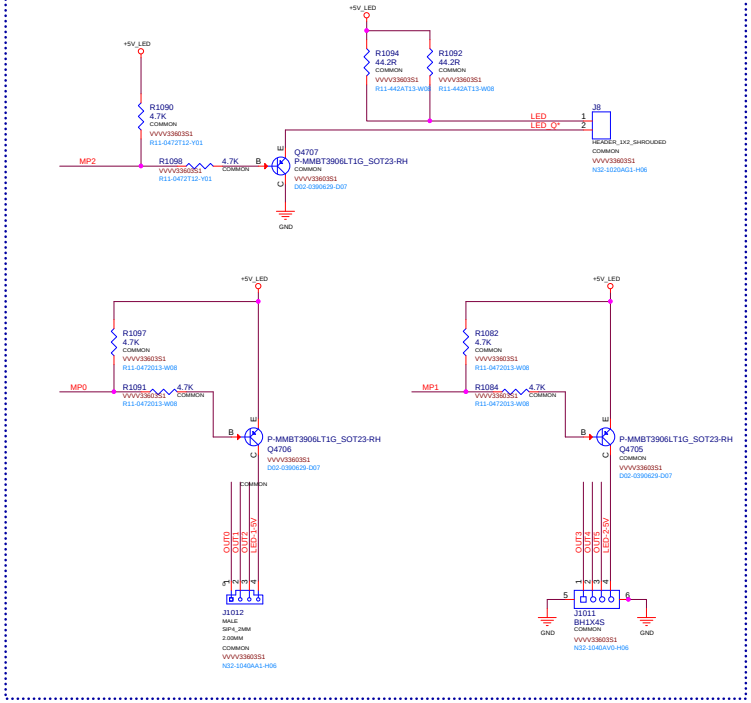
Firmware Programming

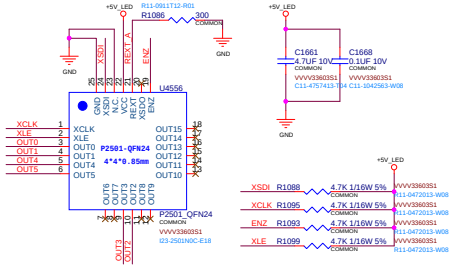


Regulators for +5V_LED



LED Connector





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Page40: VOLTAGE SUPERVISOR

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