P71, NV17, 4Mx16 SDR, 64MB, RGB, TV-out, video capture, AGP4X

PCI DEVICE ID 0X0=0X171 FOR NV17-128D.

NVIDIA

HISTORY:

X00: Adapted from P70, with memory from P60

X24: 1) Added FB clock terminators.

X26: 1) Changed LFH to new pinout.

X30: 1) Removed cap on FBACKE.
2) Changed FB clock terminators to 0402 packages.

X42: 1) Swapped power supply FETs

X45: 1) Added R606 in 12V supply to U600

X46: 1) Changed AGPSTOP pullup to 3.3V
2) Added linear regulator (U602) for frame buffer rail

X50: 1) Changed from integrated to discrete video filters

X51: 1) Removed linear regulator (U602) for frame buffer rail
2) Many BOM edits to reflect new BOM generation scheme

X52: 1) New heatsink part number.
2) Change all FB clock terminators to 200 ohms (R210-R217)

X54: 1) NVPN edits to synchronize schematic with Agile BOM.

This schematic is not the source for the netlist - the A01 netlist was used for the A04 PCB. This schematic should be used to go forward if A05 is necessary. It has the correct AGPSTOP pullup voltage, as well as many BOM edits for the new BOM generation scheme.

PAGE OVERVIEW

Stuff Option	Meaning
COMMON	Common to all assemblies
NO STUFF	Not normally present in any assembly
VIDCAP	Video Capture
RGB_PROT	RGB Protection diodes on primary DAC outputs
LFH	Second DAC channel goes to LFH connector
TV	Second DAC channel goes to S Video connector as TV out
1117	Fixed 1117 linear regulator for A3.3V
1117_ADJ	Adjustable 1117 linear regulator for A3.3V
NO_1117	Take A3.3V from system 3.3V
64B5N	64 Bit, 5 nS frame buffer
64B6N	64 Bit, 6 nS frame buffer
128B5N	128 Bit, 5 nS frame buffer
128B6N	128 Bit, 6 nS frame buffer
DESK	Desktop system
WKST	Workstation system
WKSTL	Workstation Lite system
MEM33	Frame buffer voltage is AGP 3.3V
MEM30	Frame buffer voltage is independently regulated

MS-8873 BASE ON P71-A04 Modify

1. Page 1 add RE1 and CE1 for EMI funcion.
2. Page 6 L301~L304 and L319~L321 pad size change to 0603 type. Change P300 VGA conector to stand D-SUB.
3. Remove original P71-A04 page 7 Dual DAC, 2nd VGA.
4. Page 7 remove DVI location and net function.remove U823,R1030,C885,R1031,R1032 and C419.
   L400.1,L403.1,L405.1,L406.1,L409.1 connect to A3.3V.
5. Page 8 add U100.AG3,U100.AG2 and U100.AG5 bypass cap. (for EMI function).
   Remove SAA7113 function.
   Remove U100.A7,U100.C2,U100.C4,U100.B4 net.
   Add AV-out & S-out function and remove P500,D505,D506,C883,C884,L602,L603
   Remove Decoupling U500 parts and I2C(R1033~R1036) function.
6. Page 9 L600 & L601 SMD type change to Dip type.
   Location Q1 vendor change to AOS4800 and Add C623 & C607 1000u Dip(C623 & C607 no stuff).
7. Page 10 R704~R719 & R726~R733 pad size change to 0603 type.
   Add PLCC32 bios (Location U1000,R1000,C1000),
   Change default ROMTYPE from 01 to 00
   Remove C700 & R748 (follow P70 original design)
8. Page 6 P300.16 & P300.17 connect to GND.
   U300.1,U300.2,U300.9,U300.10 pin connect to GND.
   L305,L307 and L308 0805 size change to 0603.
9. Page 8 AV_OUT and S_OUT GND change to CGND.

MS-8873 Ver:100 base on MS-8873 Ver:00A Modify (EMI solution)

1. Short CGND and GND by copper plan .
2. A3.3V add bypass CAP. CE2 102P .

MS-8873 Ver:200 base onMS-8873 Ver:100 Modify

1. Page 2 . Add a schmitt-trigger circuit (U1) for M/B compability .

P71-A06 base on P71-A04 Modify

1. Add a PCI Reset ,DFF circuit in Page 2
   Including U101,R1042,R1044,R1046,C887 parts

2. Add a NVVDD Power Sequencer circuit in Page 10
   Including D805,Q803,Q804,R1039,R1040 parts

140-10071-0000-xxx
602-10071-0000-xxx

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MS-8873 BASE ON P71-A04	
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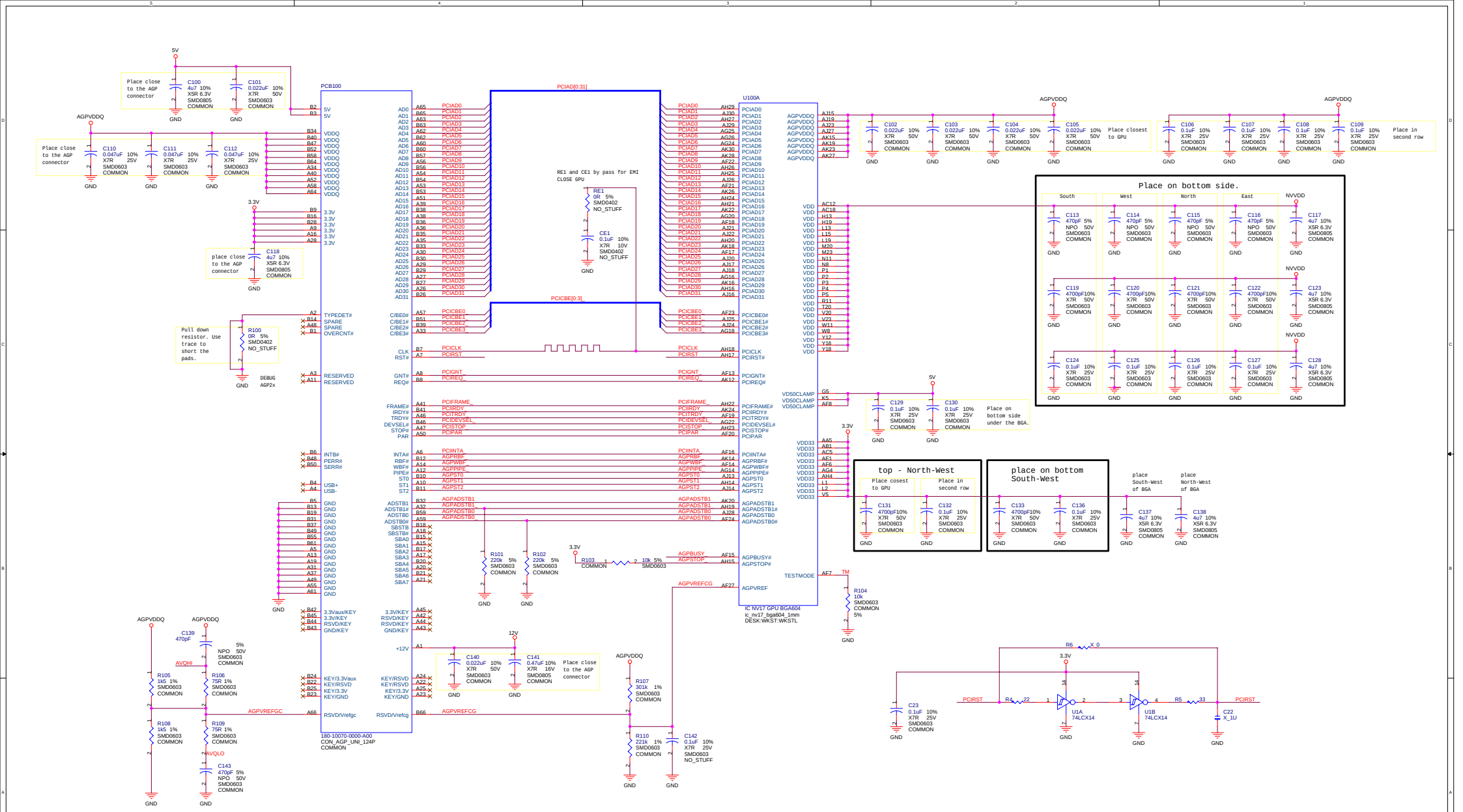
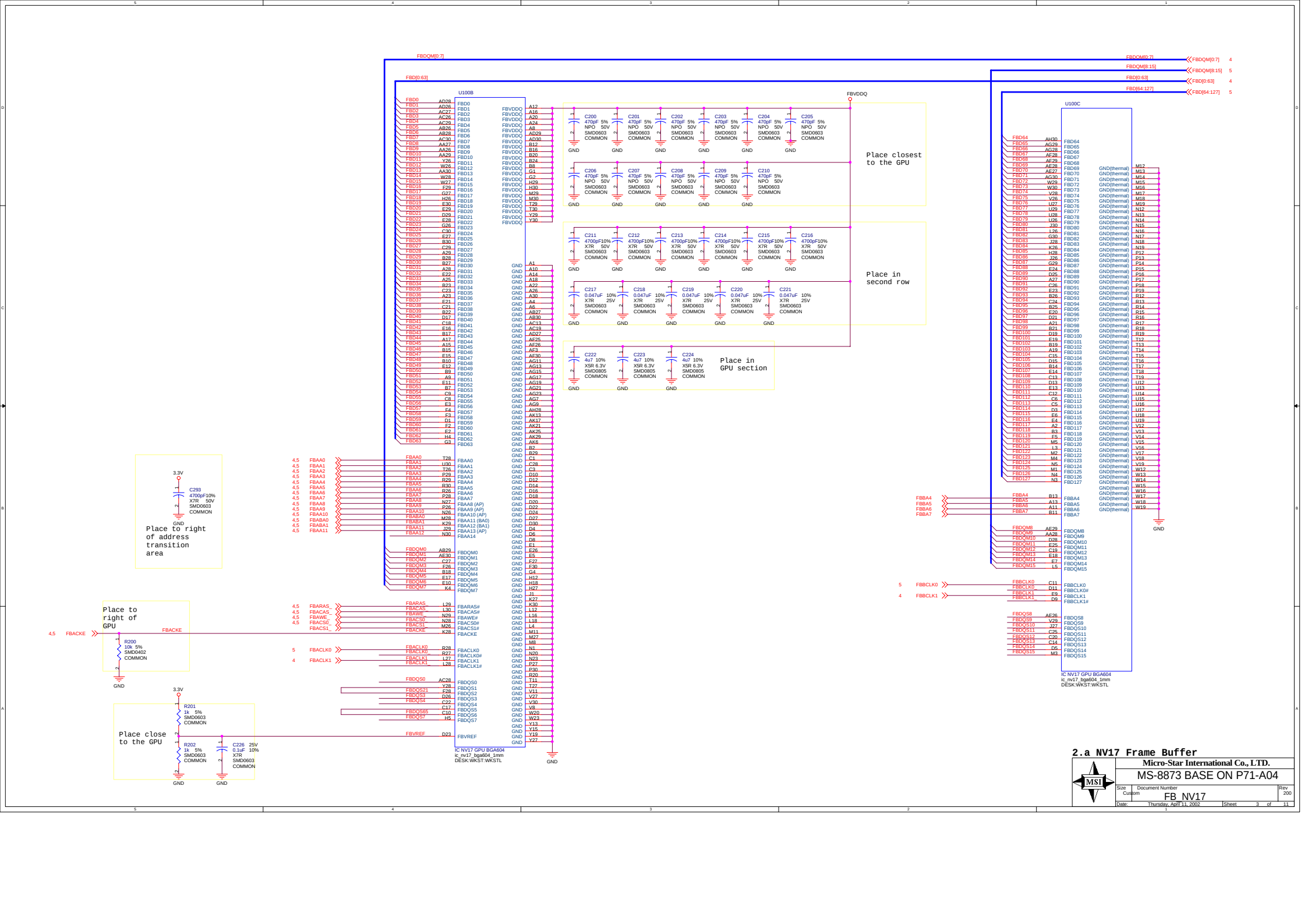

PCB100
U100A
PCIAD[0:31]
PCICBE[0:3]
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WKST:WKSTL
180-10070-0000-A00
CON_AGP_UNI_124P
COMMON
RE1 and CE1 by pass for EMI
CLOSE GPU
Place on bottom side.
top - North-West
place on bottom
South-West
Place close to the AGP connector
Pull down resistor. Use trace to short the pads.
Place close to GPU
Place in second row
Place on bottom side under the BGA.
place South-West of BGA
place North-West of BGA
1. AGP interface, core decoupling
Micro-Star International Co., LTD.
MS-8873 BASE ON P71-A04
AGP
Thursday, April 11, 2002



2.a NV17 Frame Buffer

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Size: Custom	Document Number: FB_NV17
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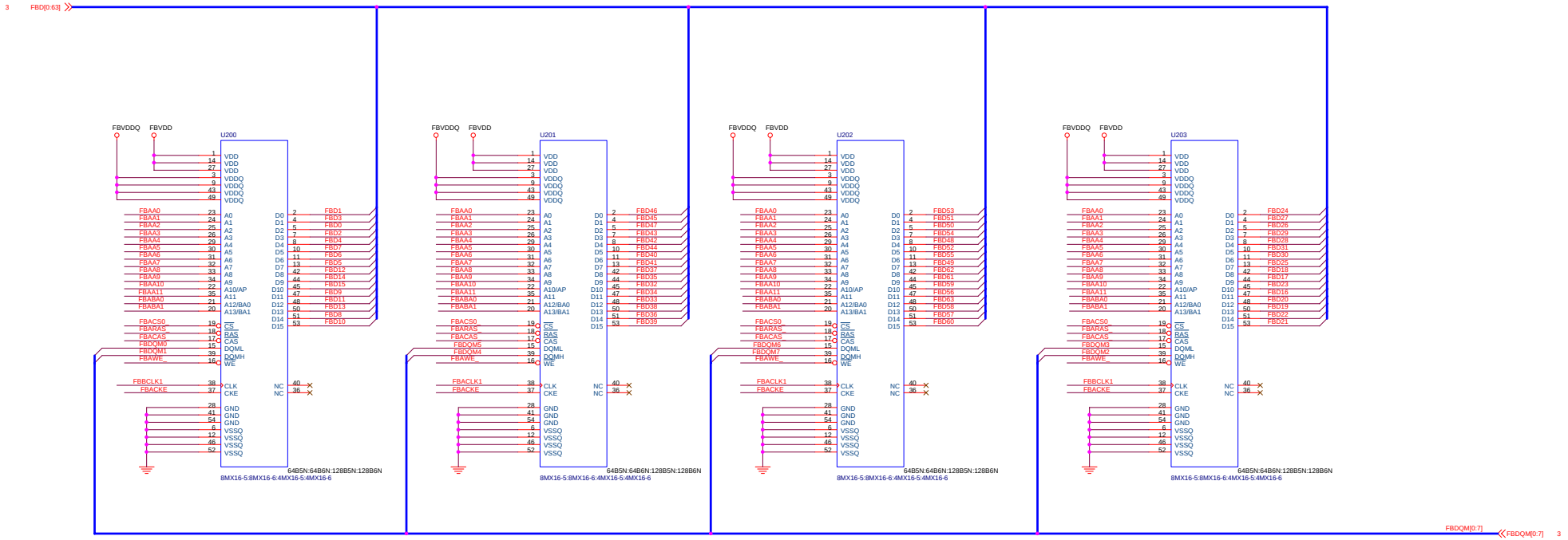

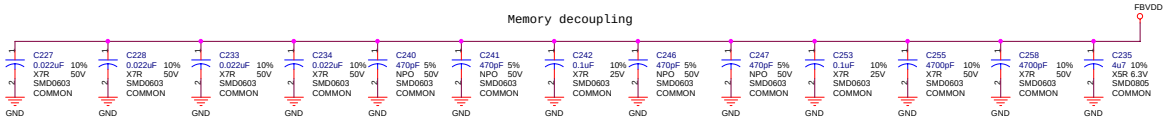

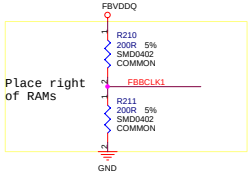

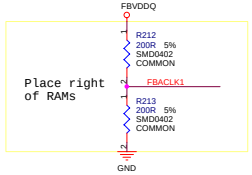

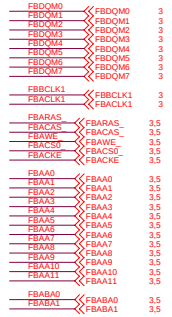

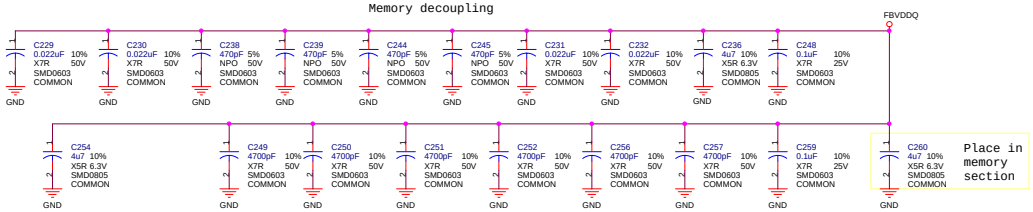

2.b Frame Buffer 0..63

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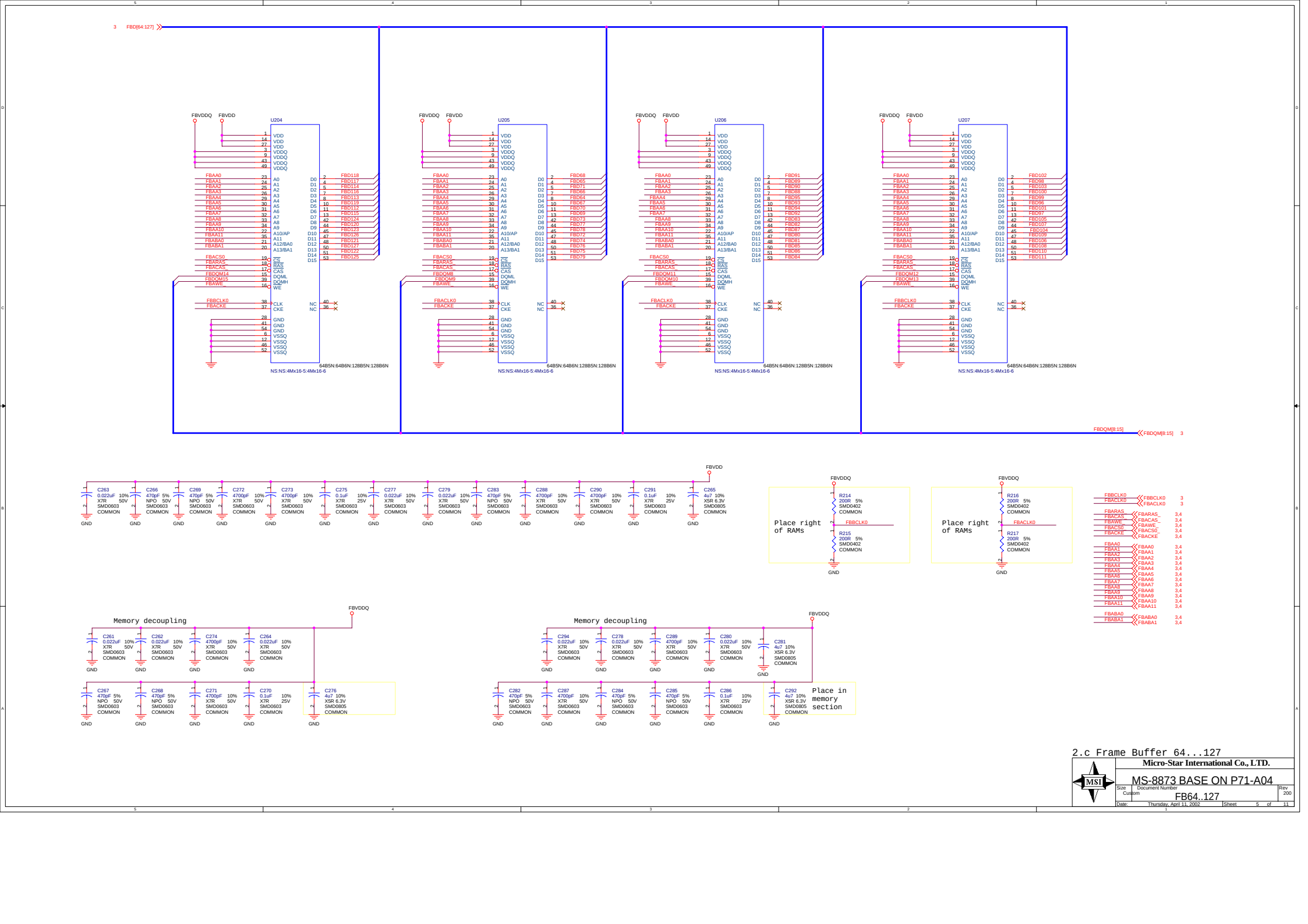
FBD[64:127]
U204
U205
U206
U207
FBVDDQ
FBVDD
64B5N:64B6N:128B5N:128B6N
NS:NS:4Mx16-5:4Mx16-6
FBDQM[8:15]
FBCLK0
FBACKE
FBAA0
FBABA0
FBACS0
FBARAS_
FBACAS_
FBDQM14
FBDQM15
FBAWE_
Memory decoupling
Place right of RAMs
Place in memory section
R214 200R 5% SMD0402 COMMON
R215 200R 5% SMD0402 COMMON
R216 200R 5% SMD0402 COMMON
R217 200R 5% SMD0402 COMMON
2.c Frame Buffer 64...127
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FB64..127
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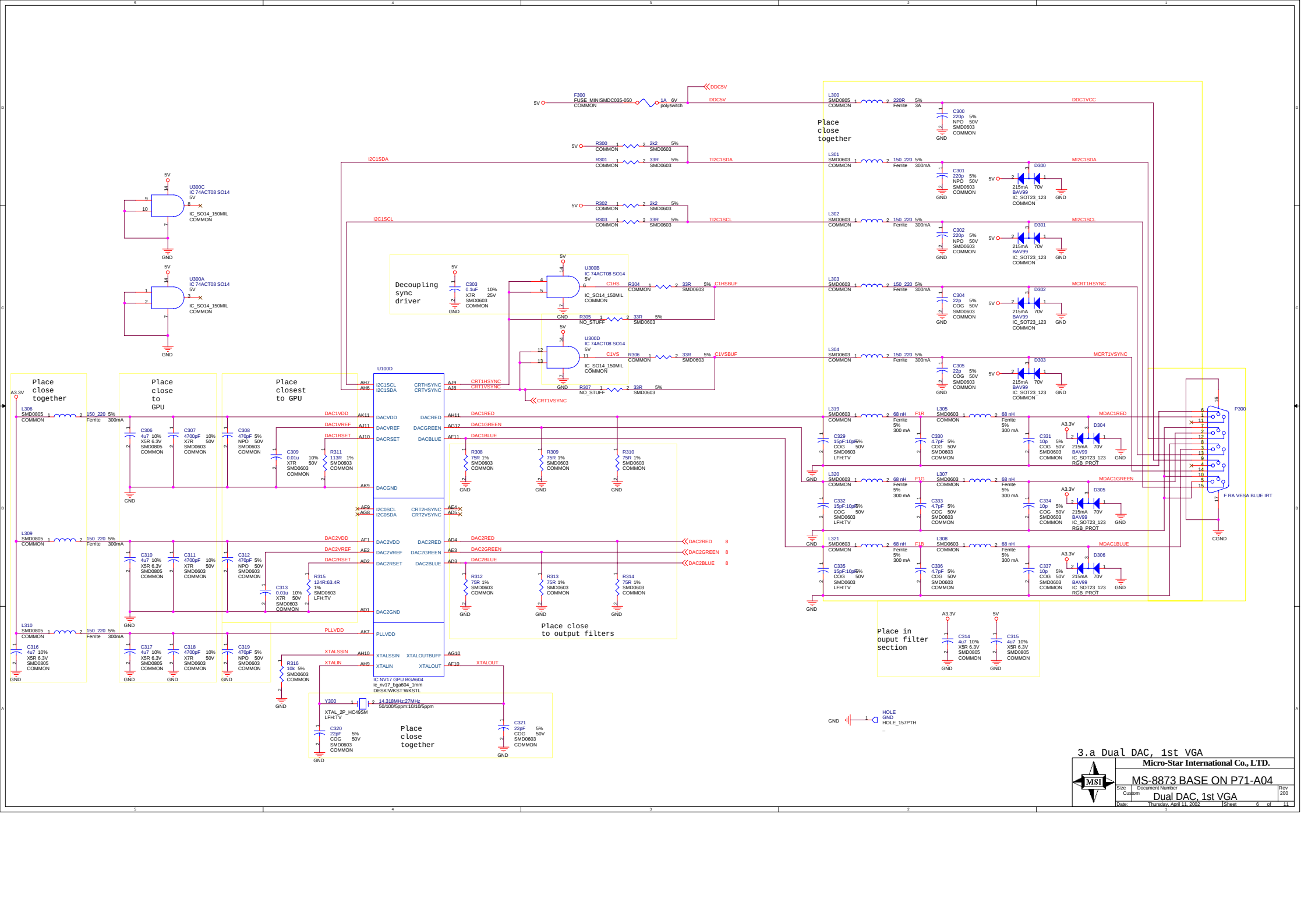
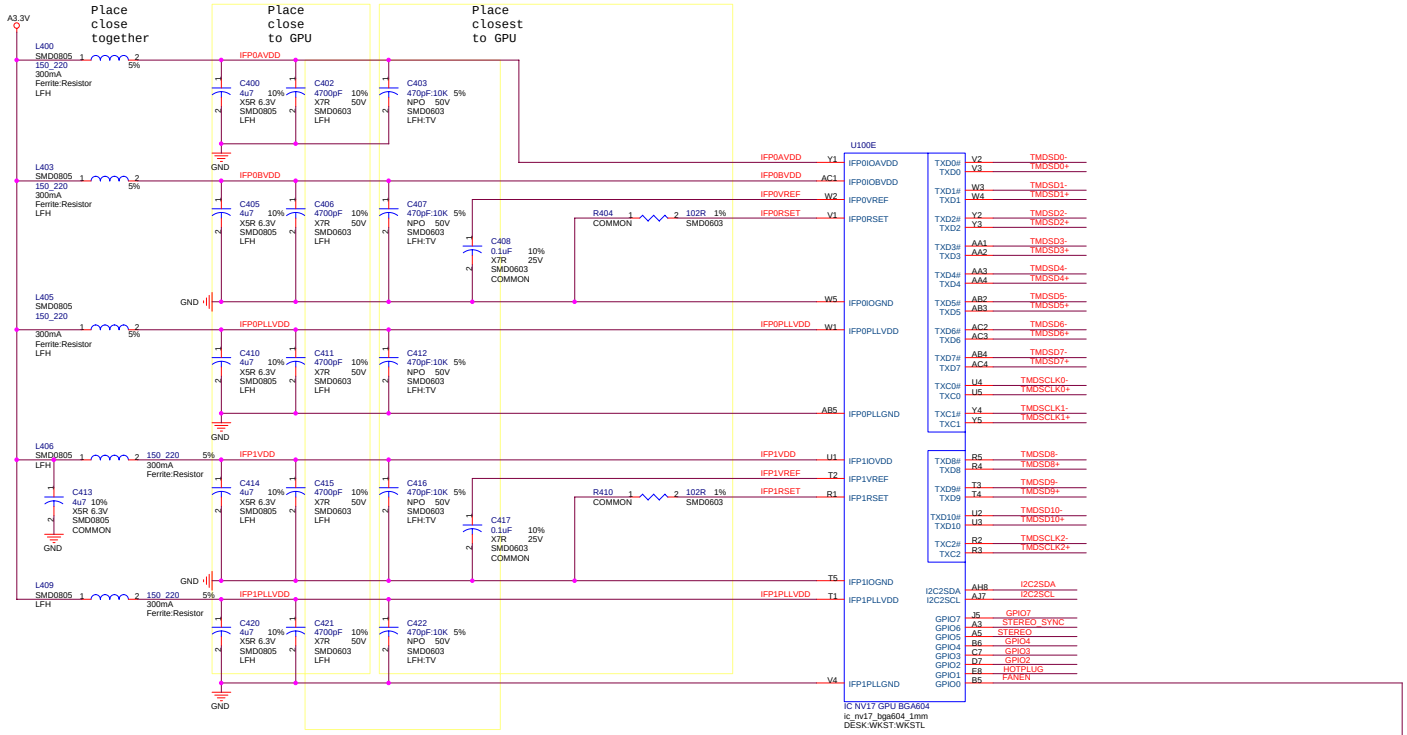

Place close together
Place close to GPU
Place closest to GPU
Decoupling sync driver
Place close to output filters
Place in ouput filter section
Place close together
U100D
IC NV17 GPU BGA604
ic_nv17_bga604_1mm
DESK:WKST:WKSTL
U300A IC 74ACT08 SO14
U300B IC 74ACT08 SO14
U300C IC 74ACT08 SO14
U300D IC 74ACT08 SO14
IC_SO14_150MIL COMMON
F300 FUSE_MINISMDC035-050 COMMON
DDC5V
DDC1VCC
I2C1SDA
I2C1SCL
TI2C1SDA
TI2C1SCL
MI2C1SDA
MI2C1SCL
MCRT1HSYNC
MCRT1VSYNC
C1HSBUF
C1VSBUF
CRT1HSYNC
CRT1VSYNC
DAC1VDD
DAC1VREF
DAC1RSET
DAC1RED
DAC1GREEN
DAC1BLUE
DAC2VDD
DAC2VREF
DAC2RSET
DAC2RED
DAC2GREEN
DAC2BLUE
PLLVDD
XTALSSIN
XTALIN
XTALOUT
P300
F RA VESA BLUE IRT
Y300 14.318MHz:27MHz 50/100/5ppm:10/10/5ppm
XTAL_2P_HC49SM LFH:TV
HOLE GND HOLE_157PTH
3.a Dual DAC, 1st VGA
Micro-Star International Co., LTD.
MS-8873 BASE ON P71-A04
Dual DAC, 1st VGA
Thursday, April 11, 2002



SCREW-1

SCREW-2

heatsink

Passive
HEATSINK_NV10
COMMON

PCB

Bracket

4. Panel

MSI	Micro-Star International Co., LTD.	
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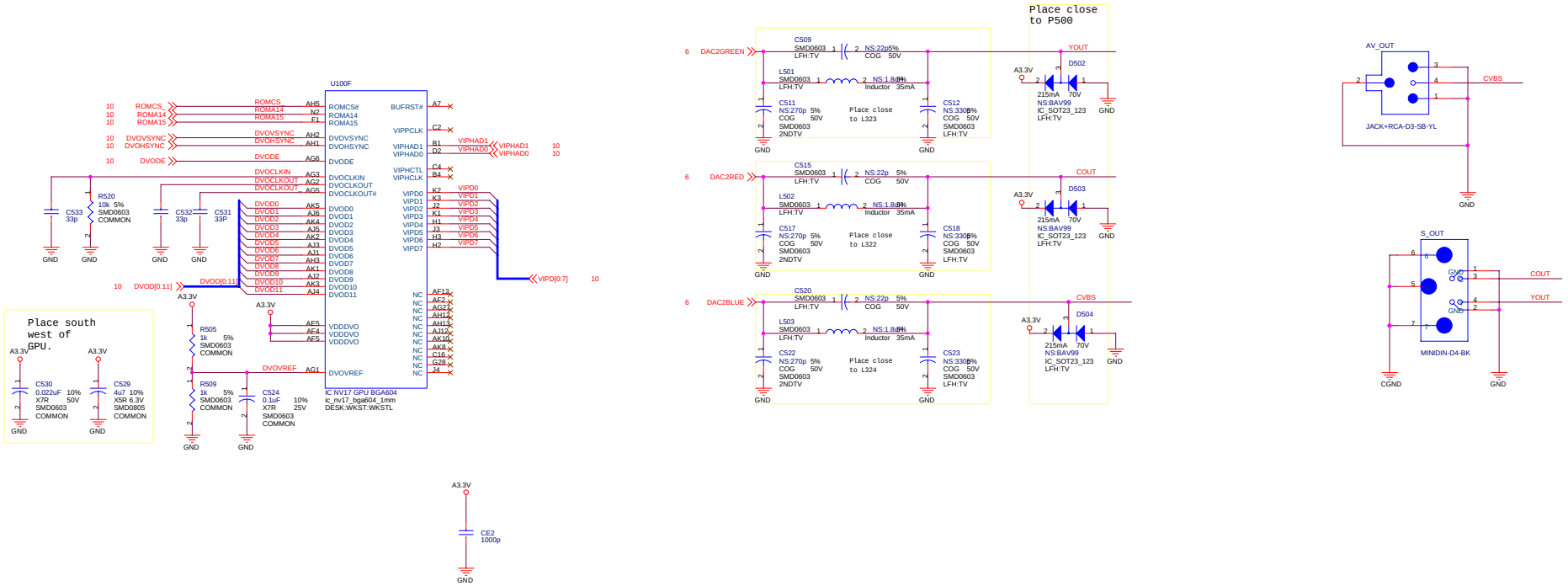

5. TV out,video capture,stereo

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Size: Custom	Document Number: TV out, video capture, stereo	Rev: 200
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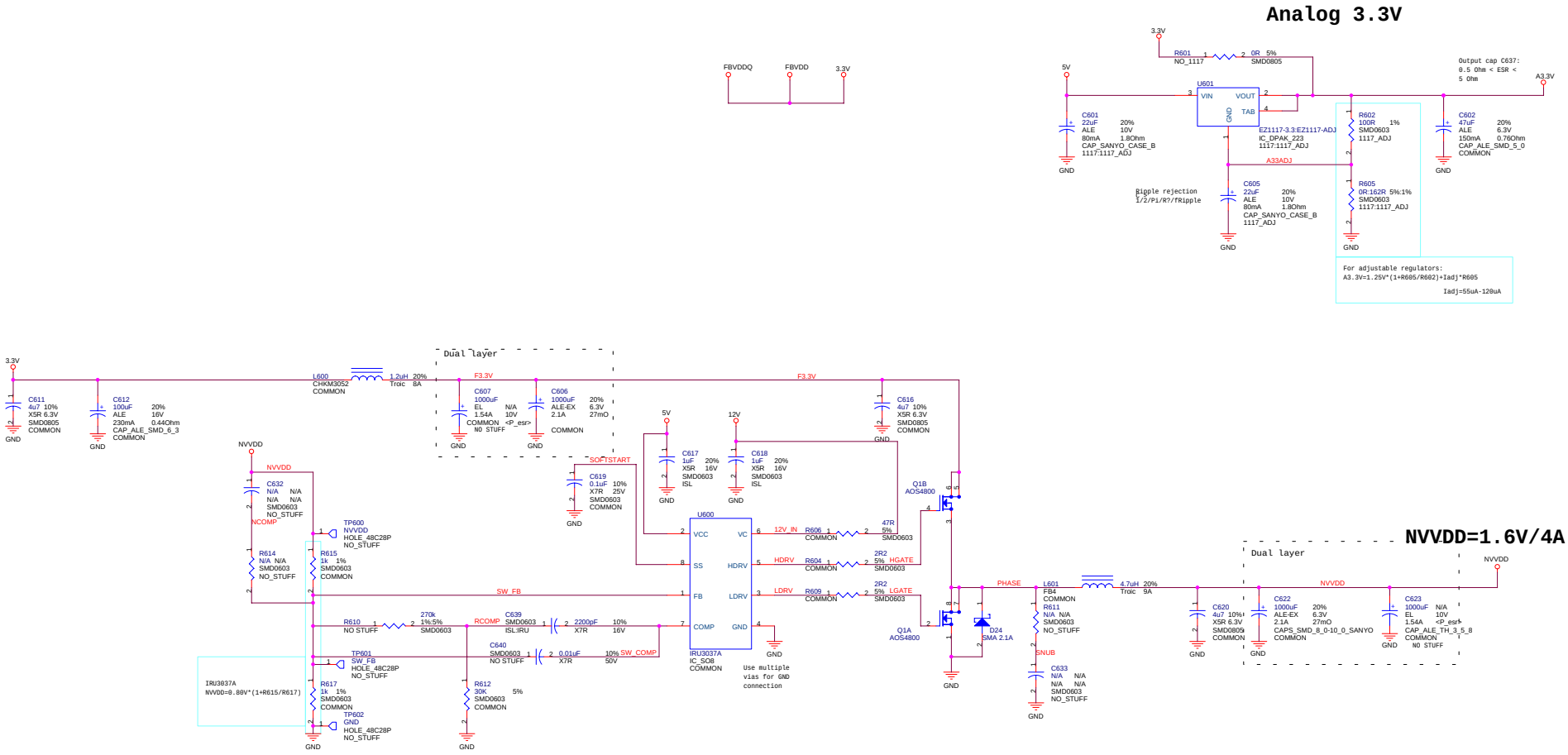

6. Power supply

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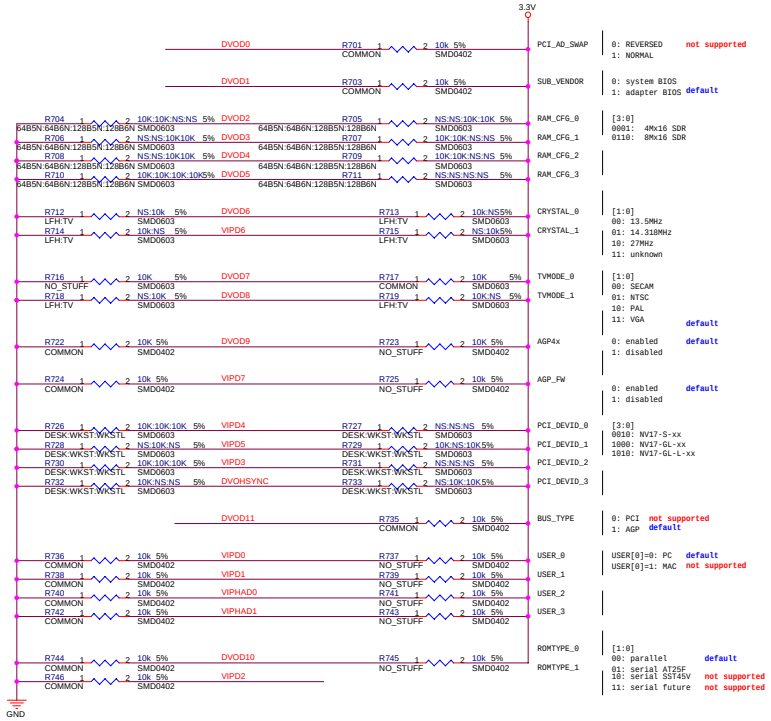

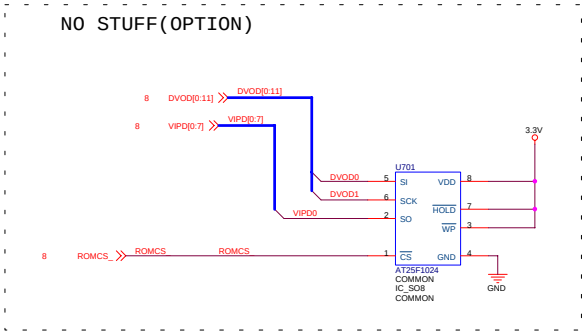

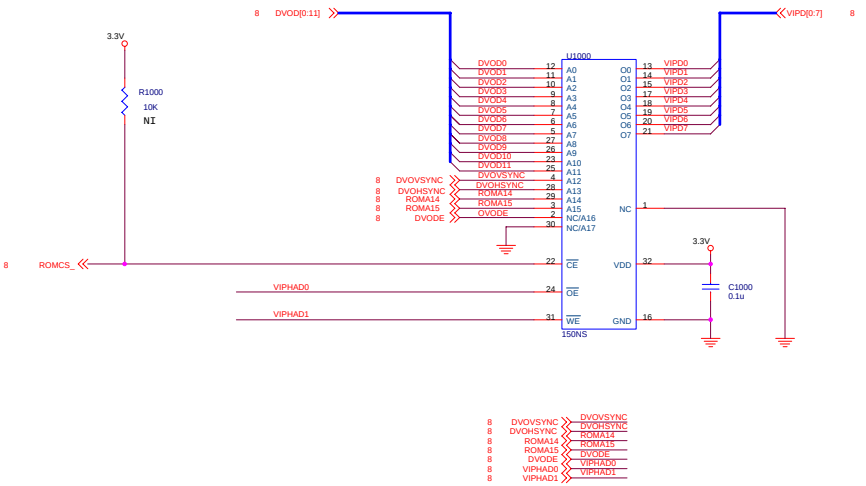

7. BIOS, Strapping

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MS-8873 BASE ON P71-A04	
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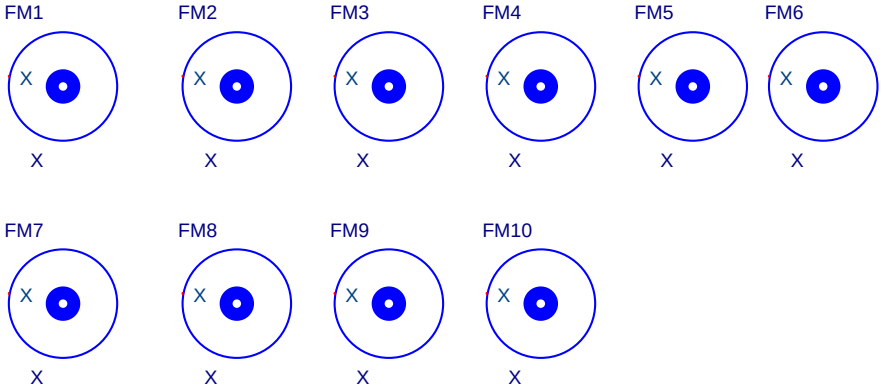

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