

PG411 A01

GP104 - 8GB GDDR5, 256b, 256Mx32
Tall DVI-D + DP + DP + HDMI + DP

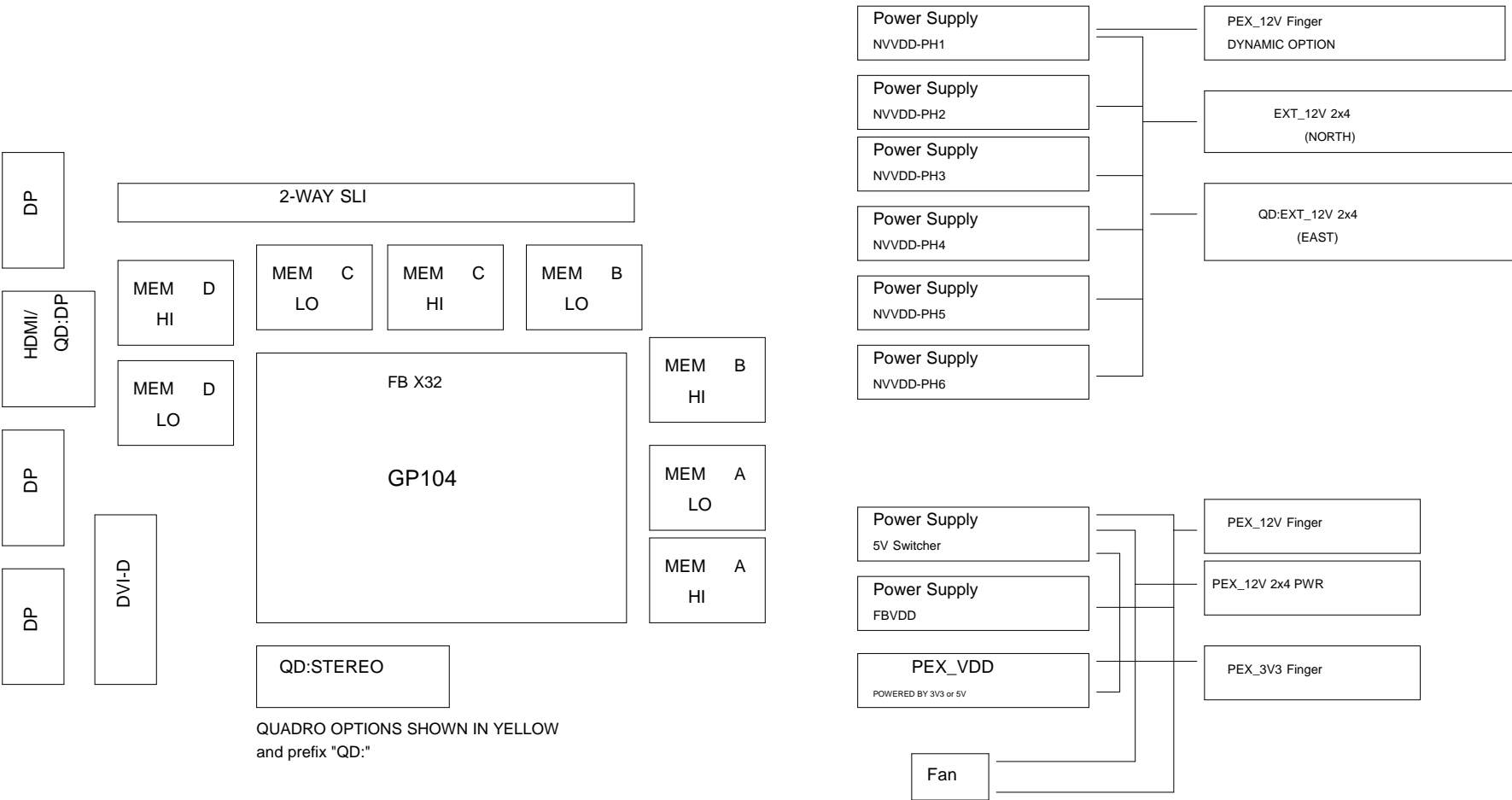
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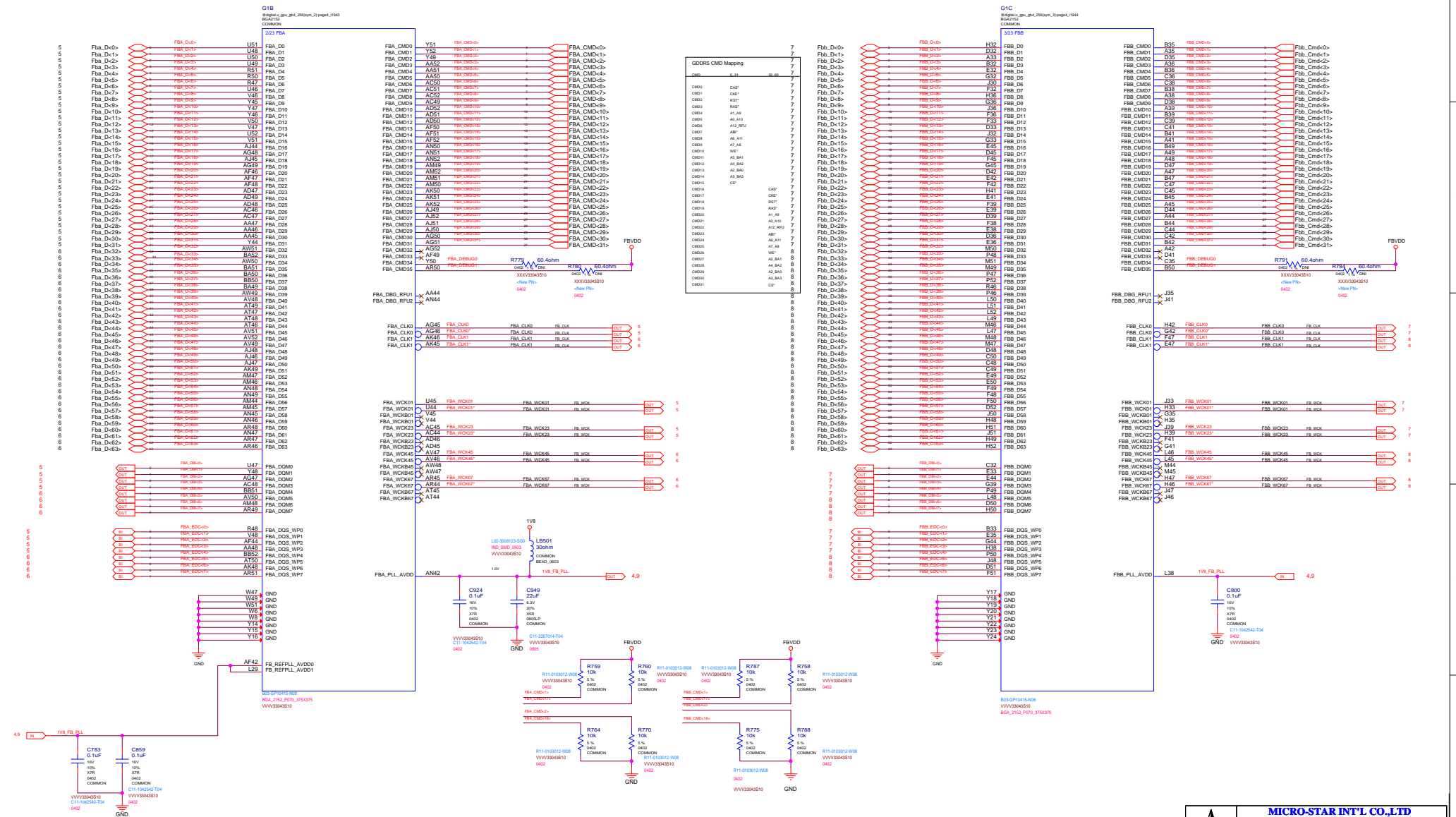


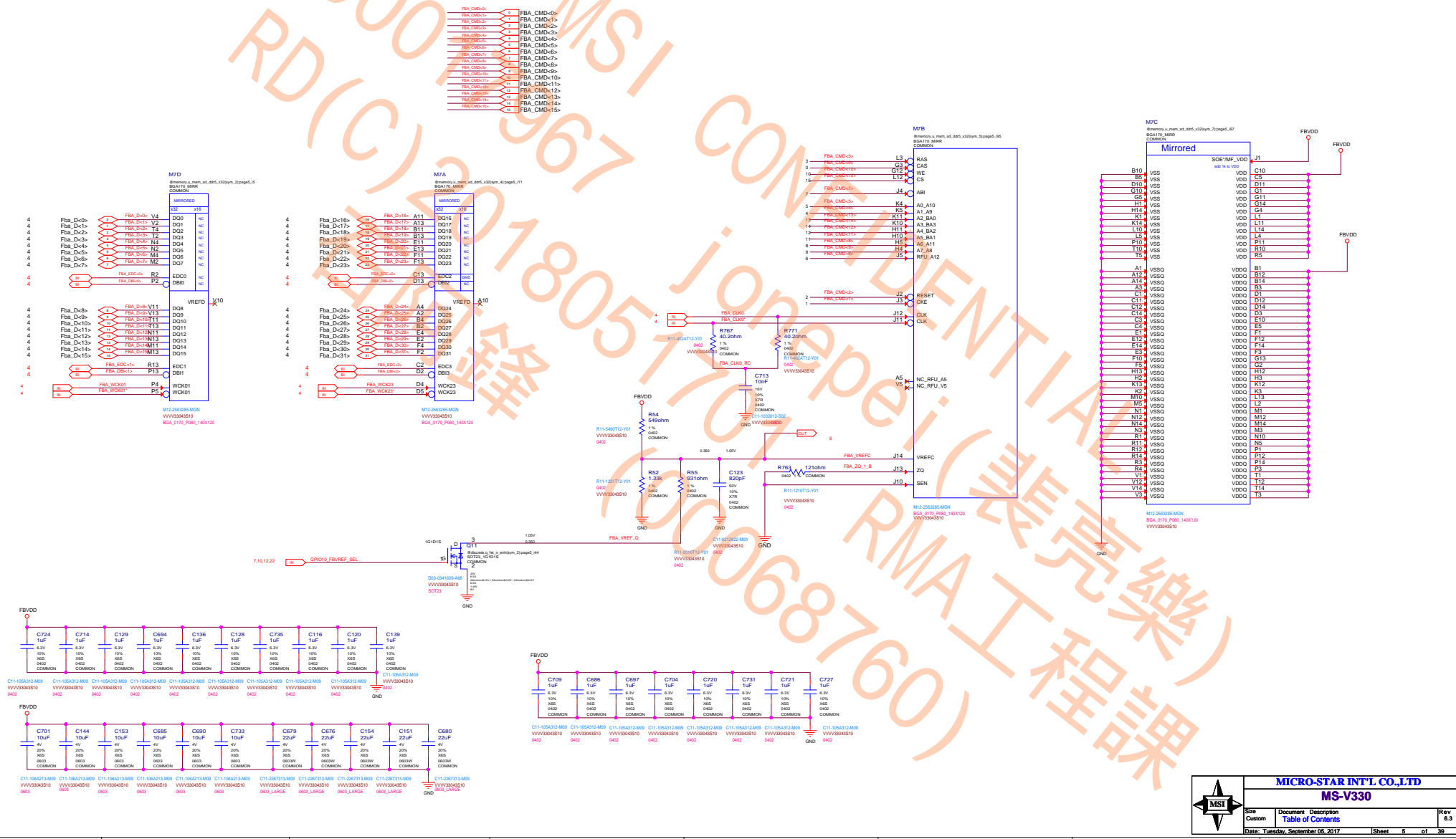
QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

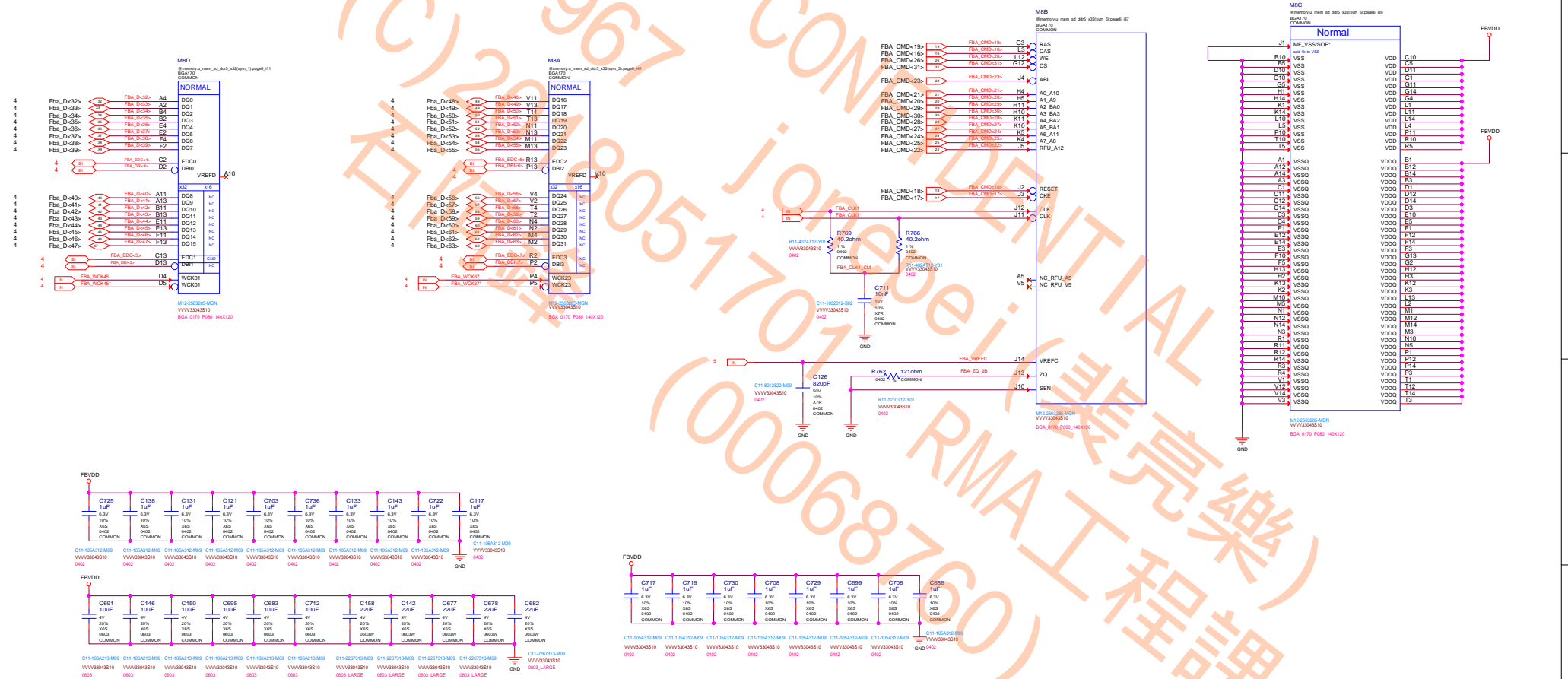
Remove POWER BRAKE

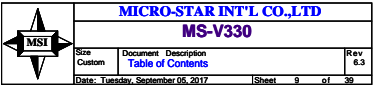


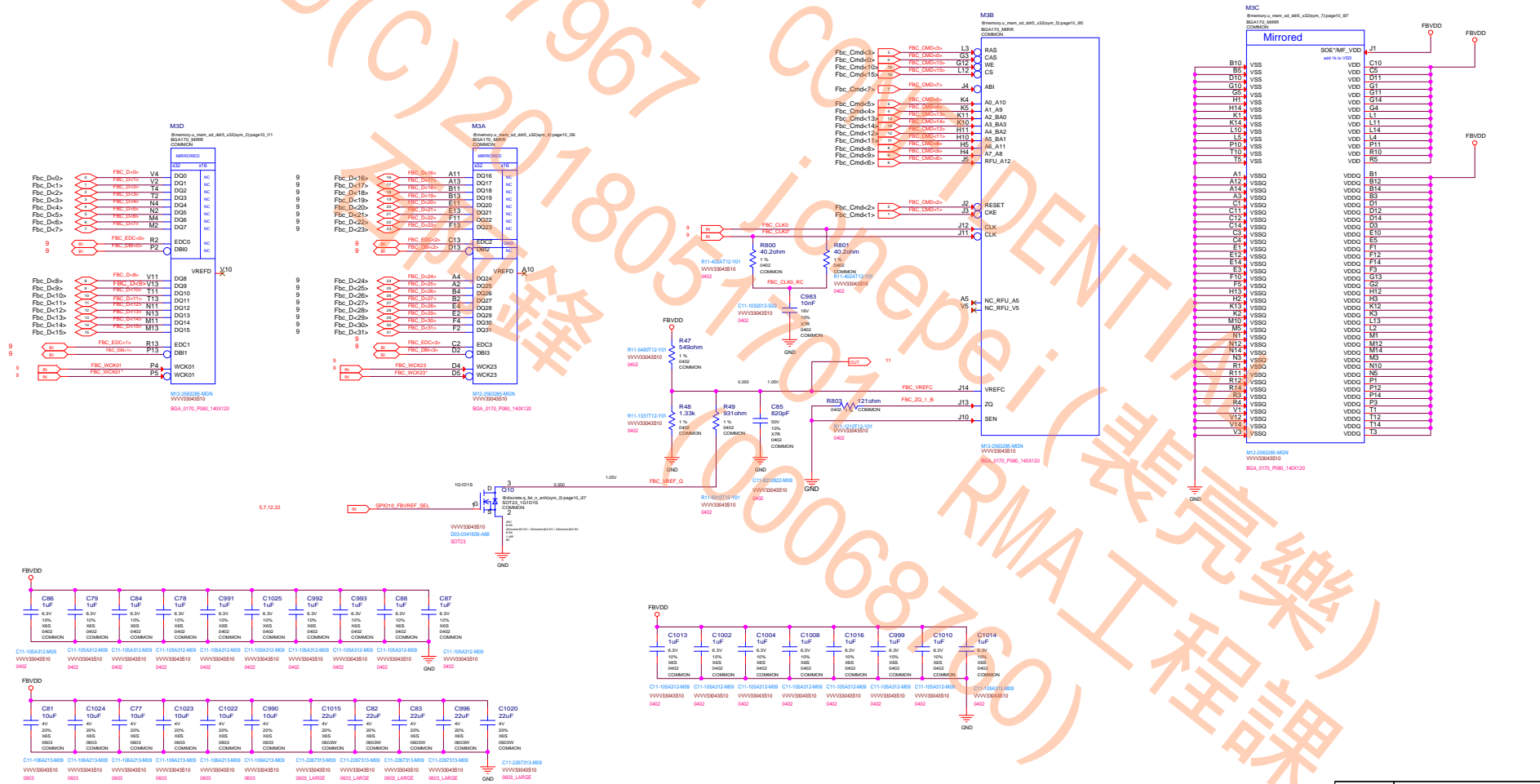
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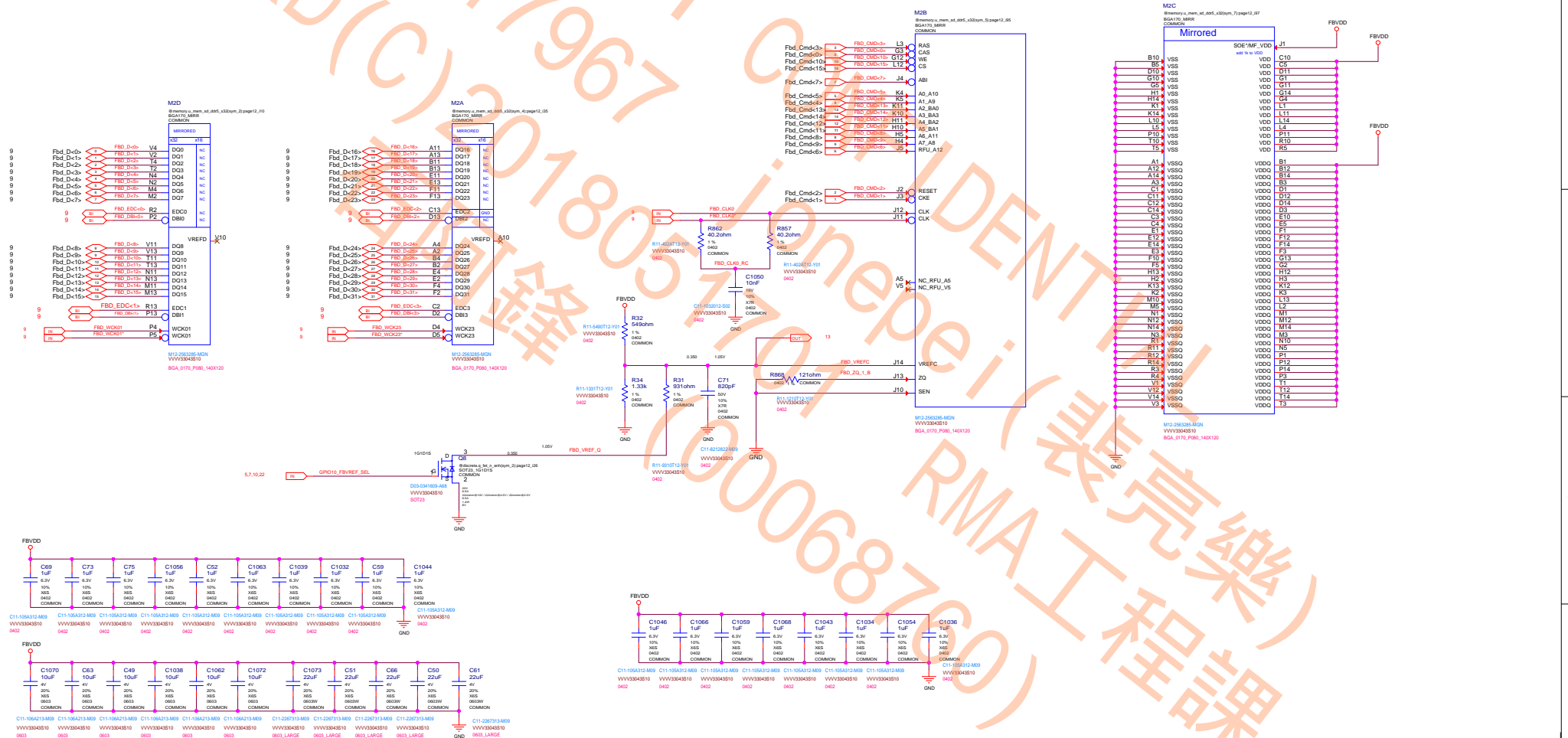


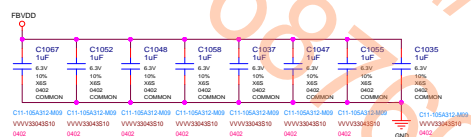
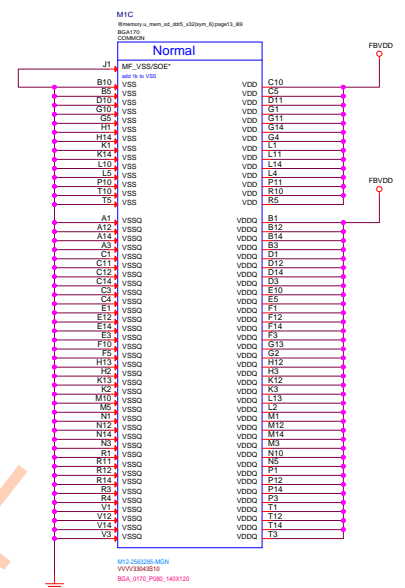


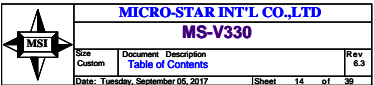




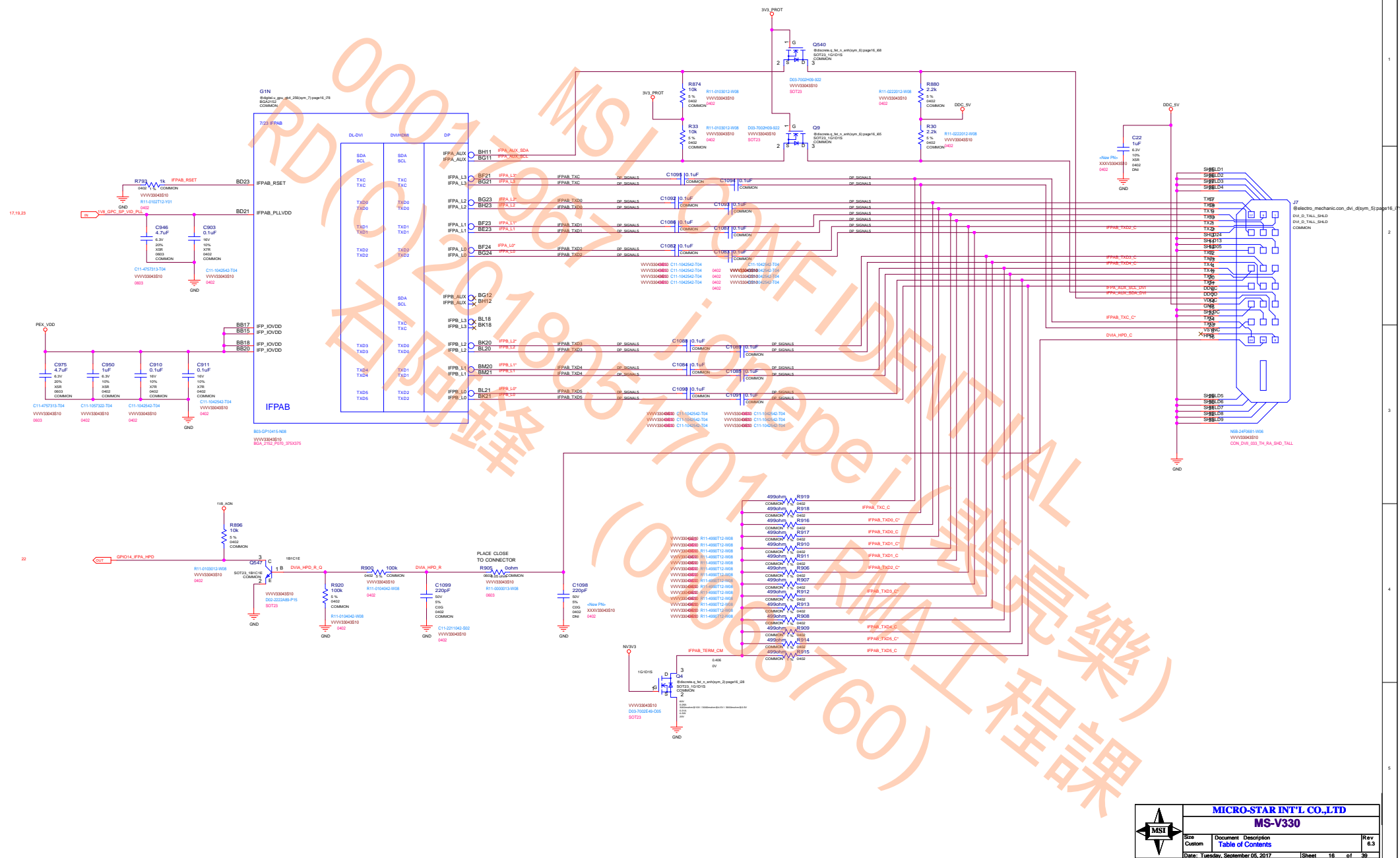




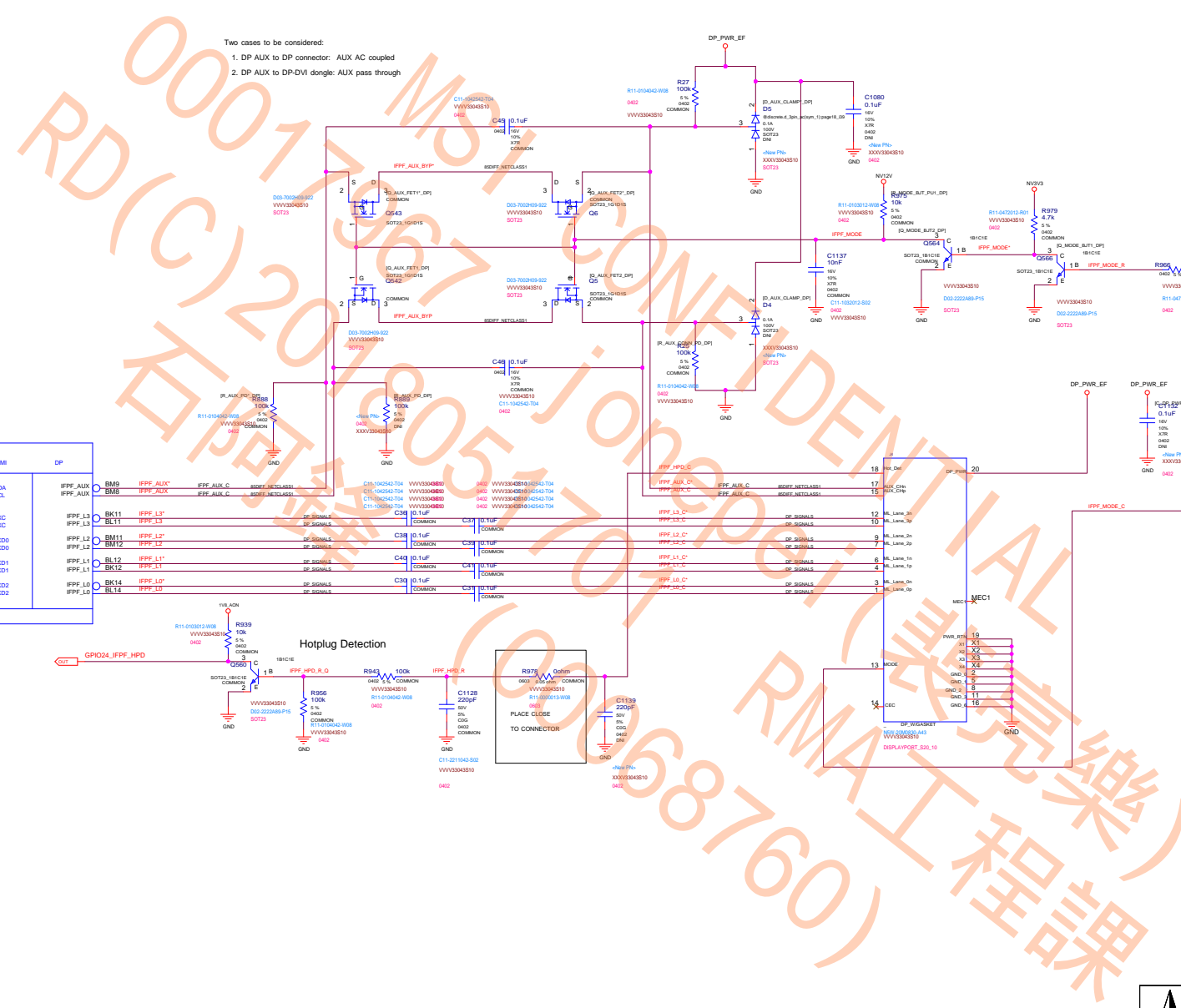


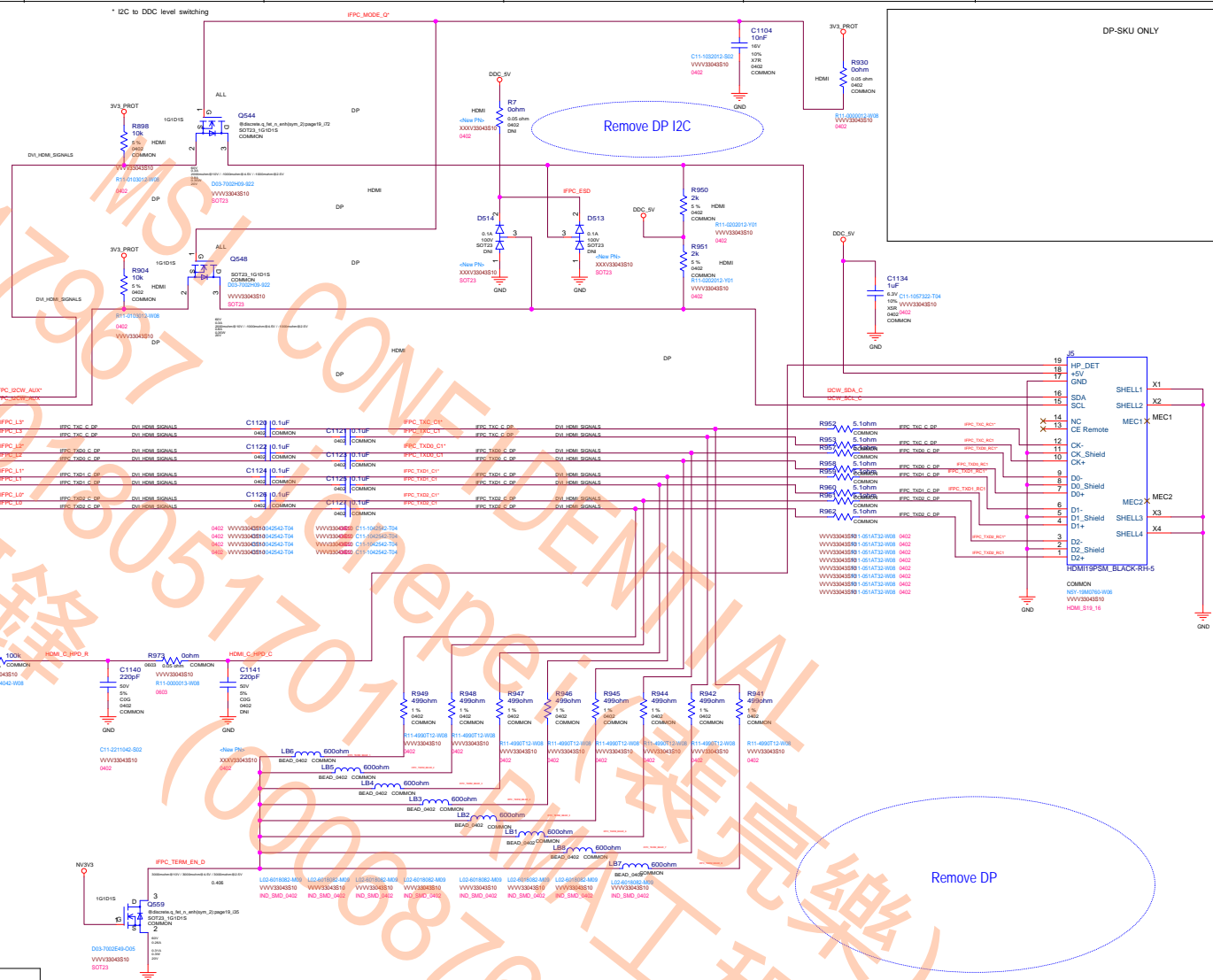
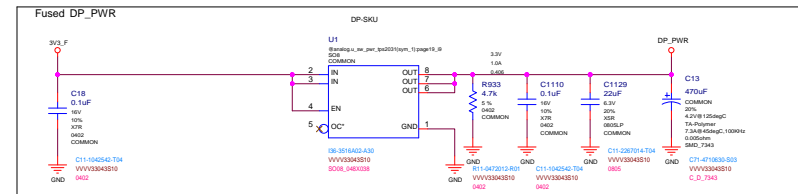




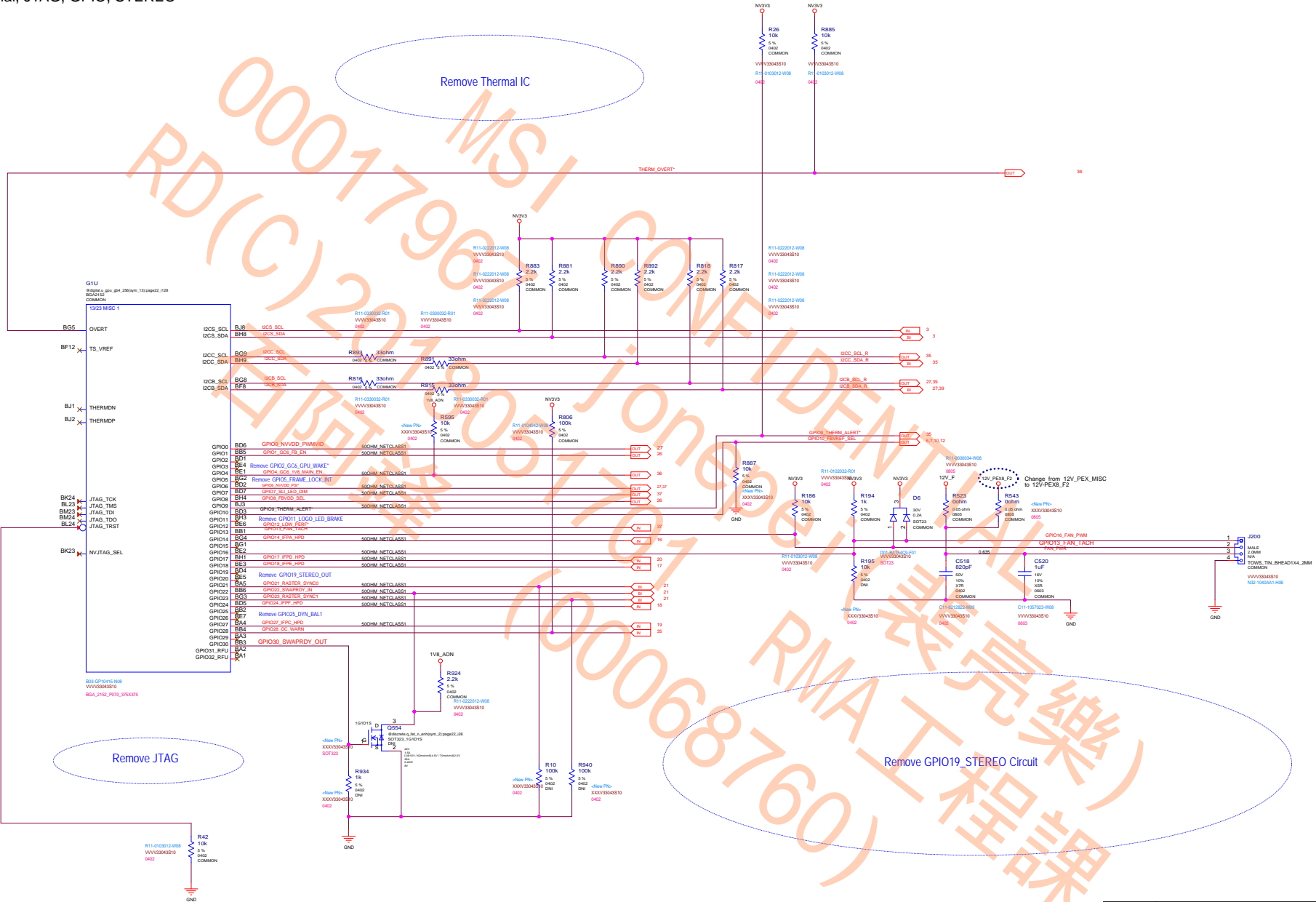


1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through





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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	M	0001
H	H	M	0000

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	0	1	1
M	L	L	1	0	1	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	L	M	1	0	0	1
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	1 DEFAULT

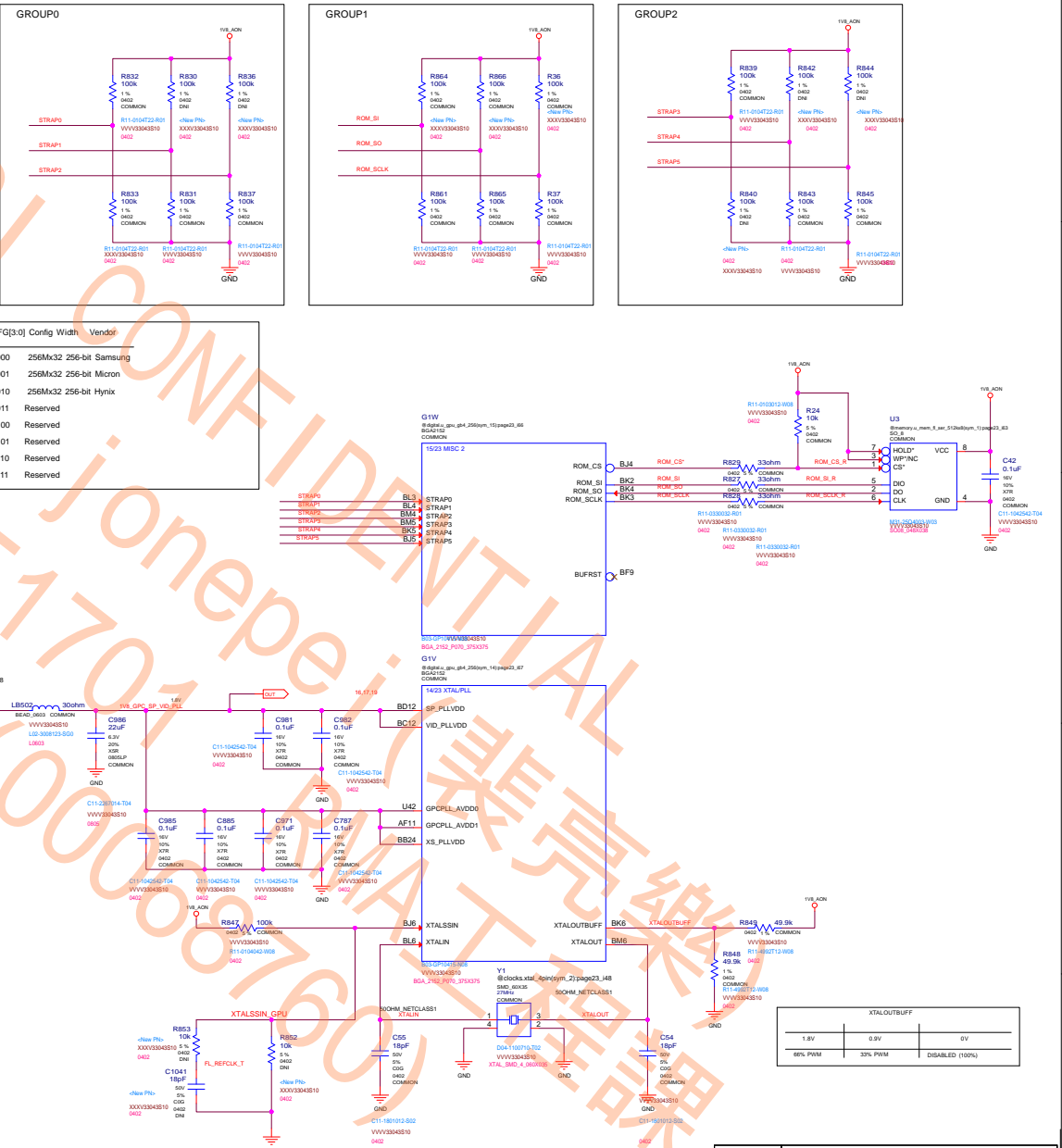
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

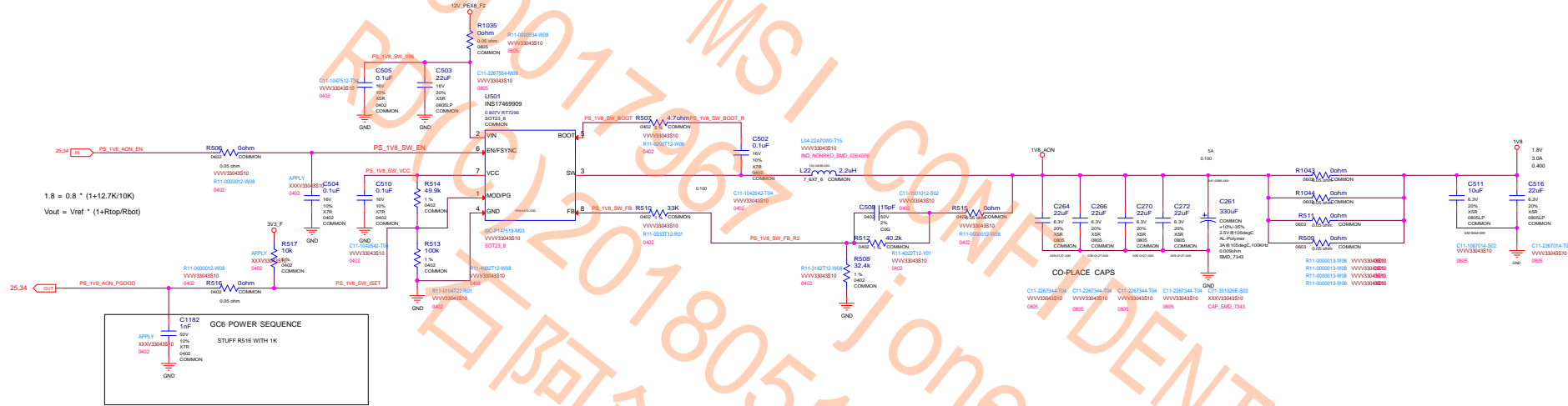
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

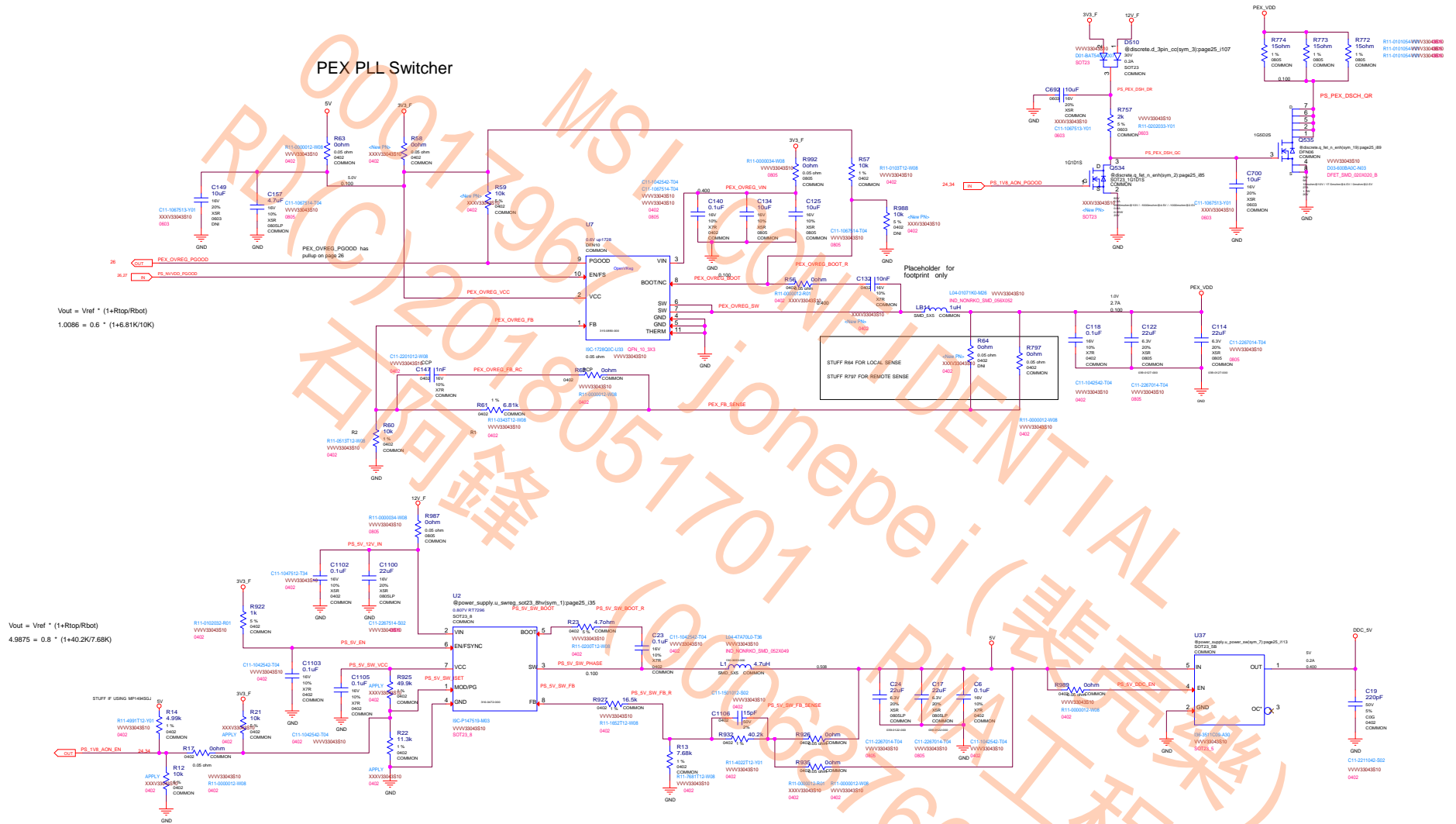
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



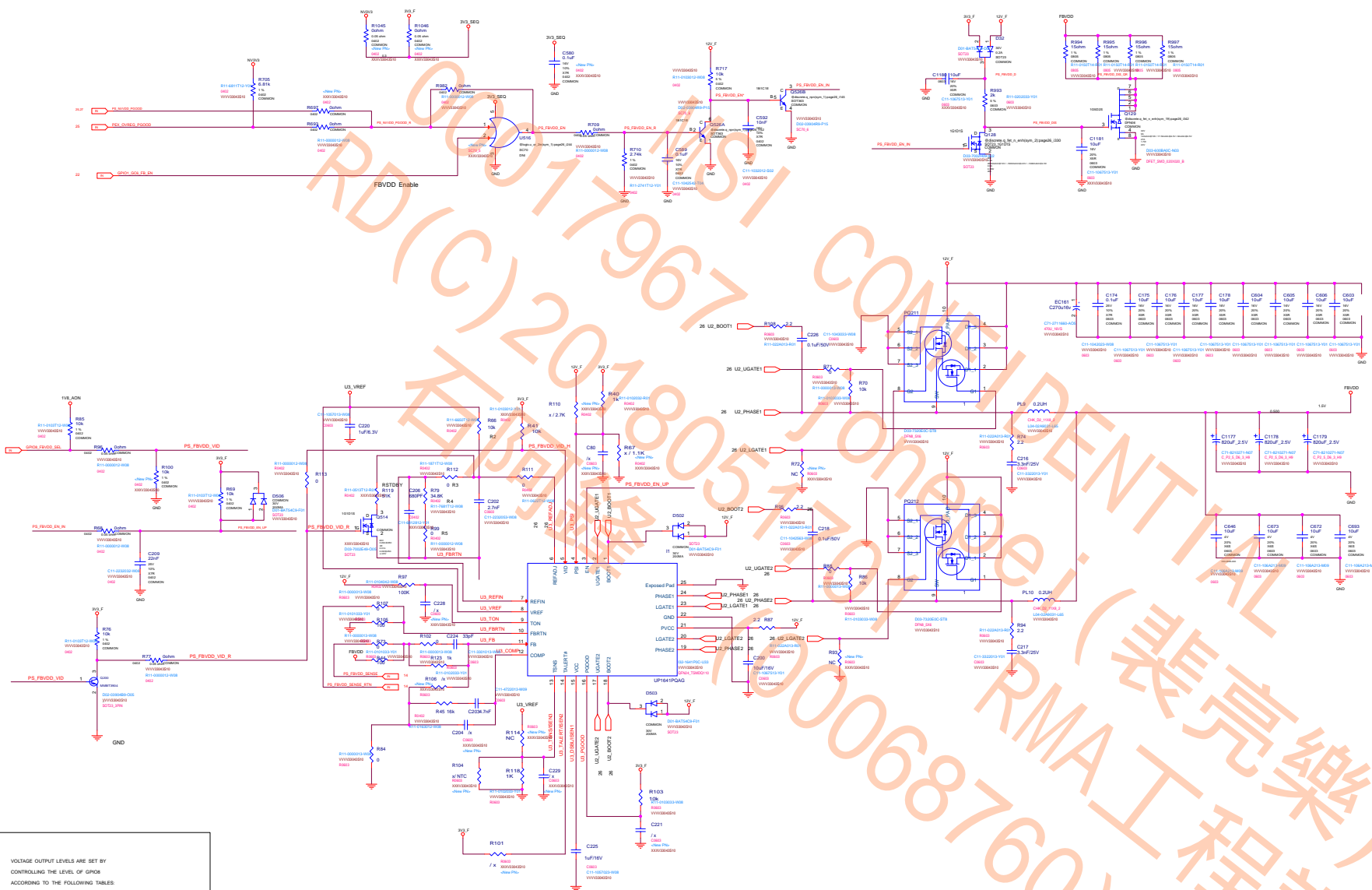


PEX PLL Switcher



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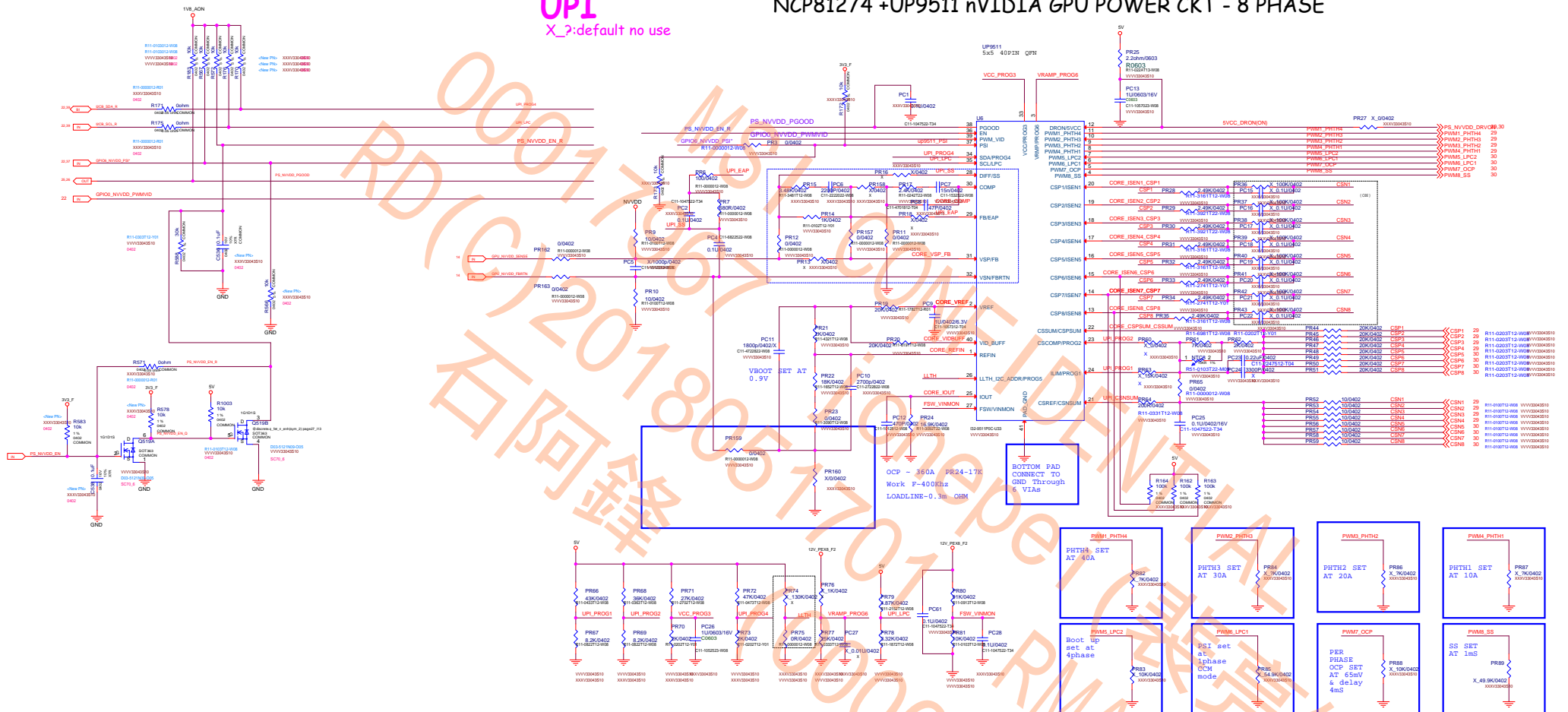


VOLTAGE OUTPUT LEVELS ARE SET BY CONTROLLING THE LEVEL OF GPIO8 ACCORDING TO THE FOLLOWING TABLES:

SAMSUNG K4G1325FC-HC28


GPIO8 LEVEL	FBVDD OUTPUT VOLTAGE
0	1.35V
1	1.55V

NCP81274 +UP9511 nVIDIA GPU POWER CKT - 8 PHASE



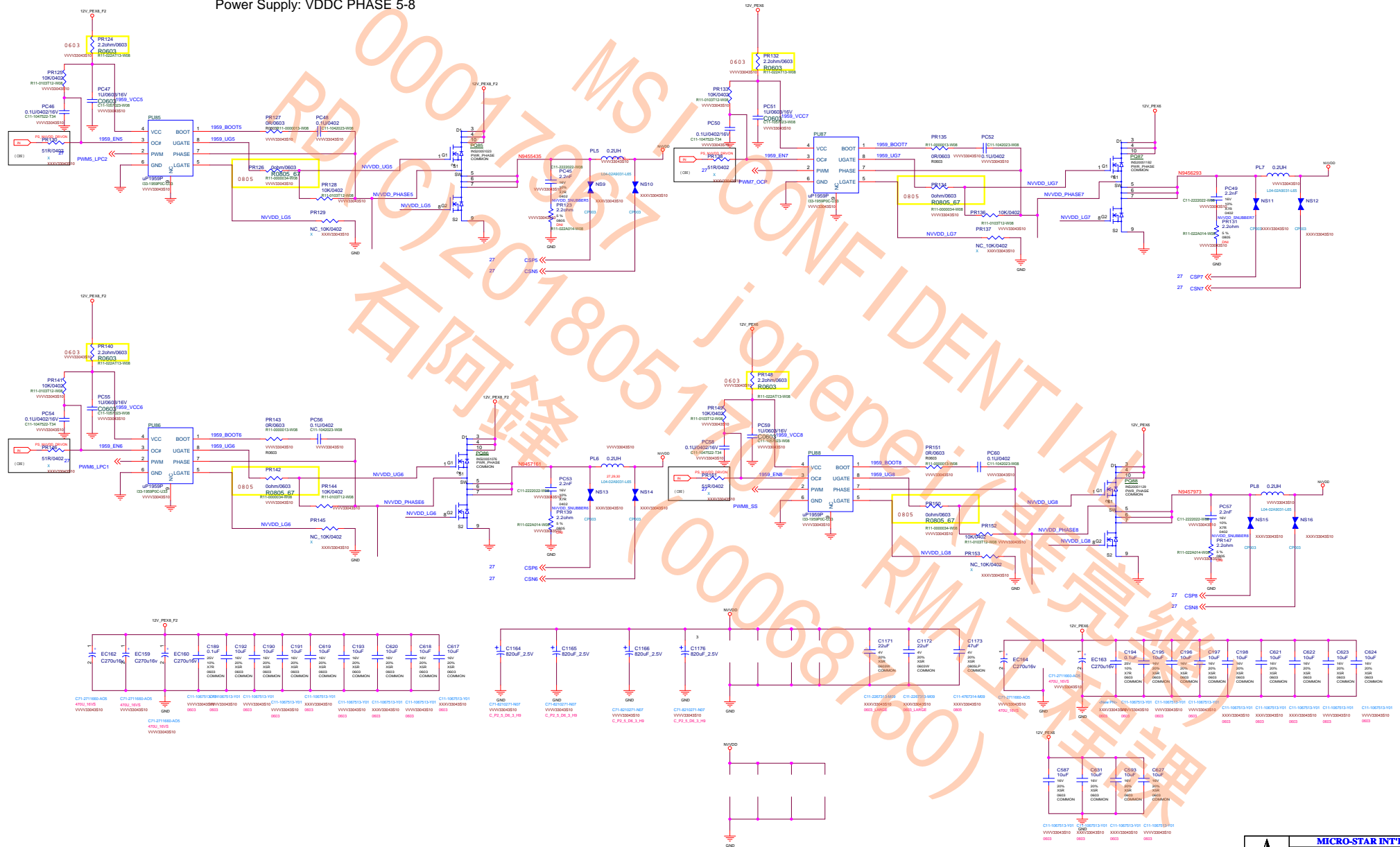
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石阿鋒 (00068760)

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Power Supply: VDDC PHASE 5-8







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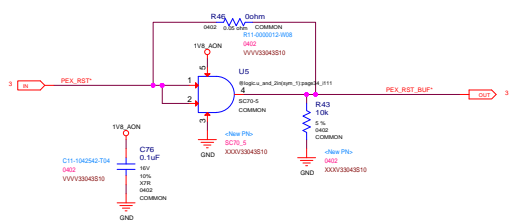
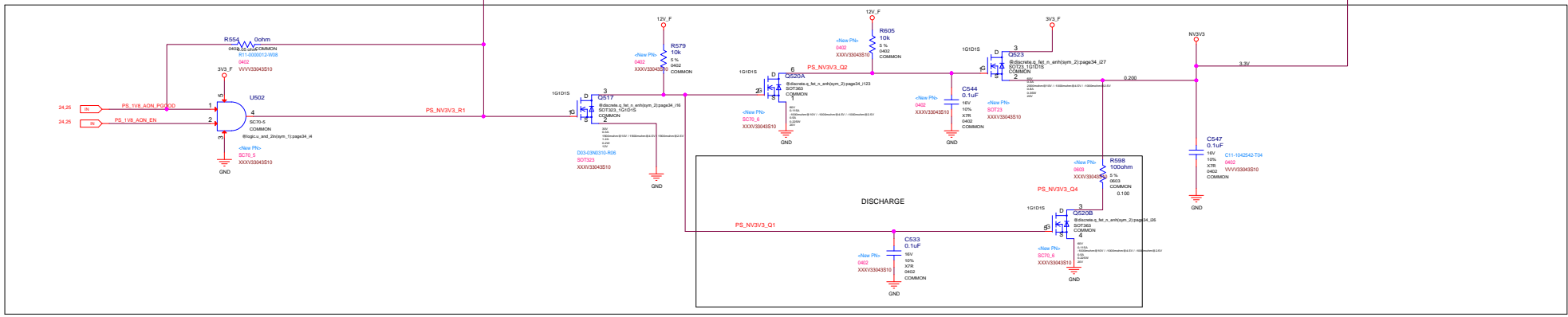
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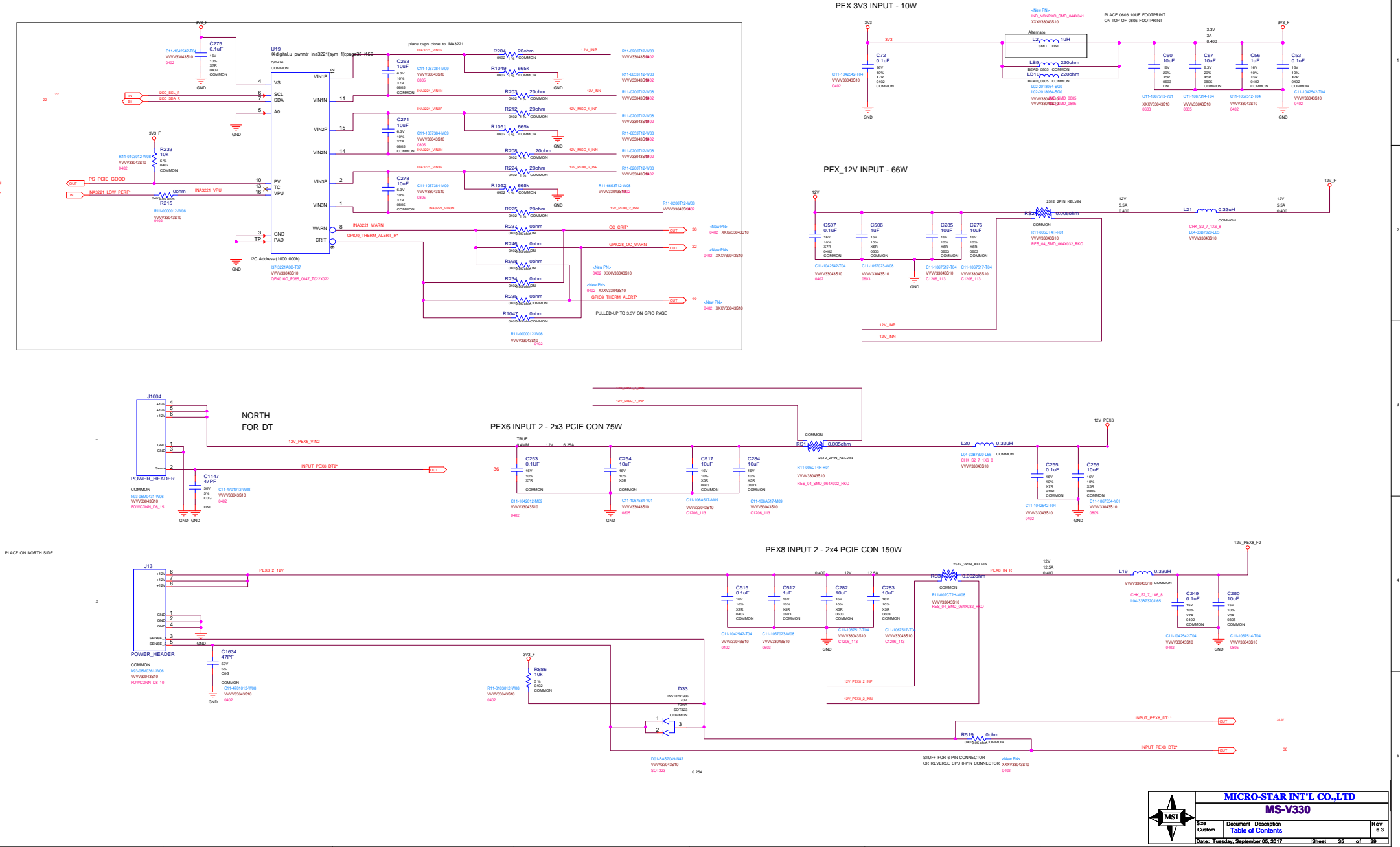


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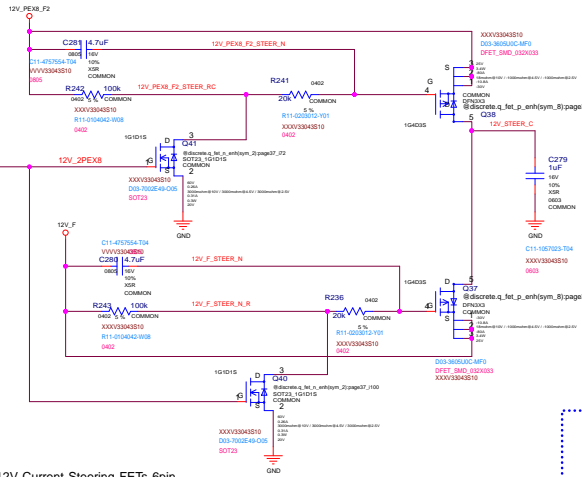
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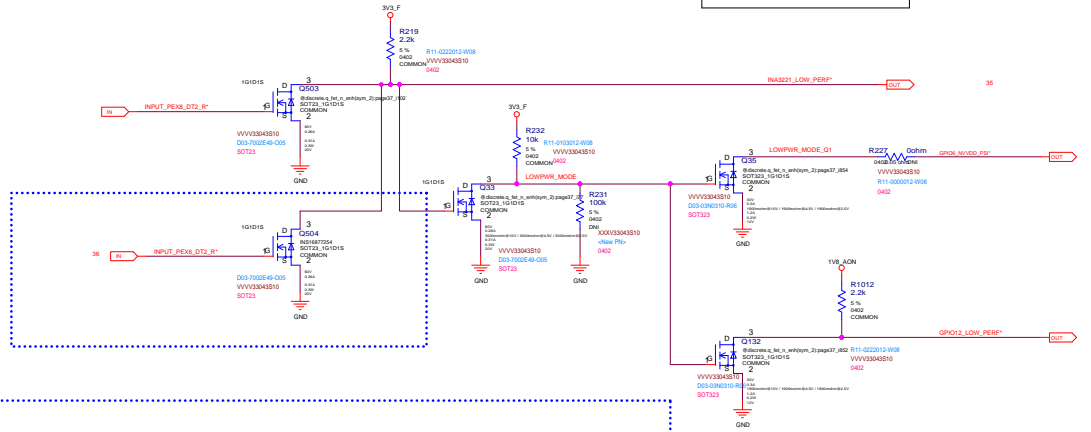






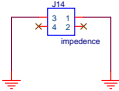
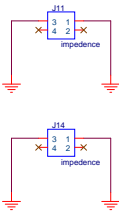
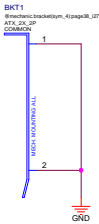
Remove POWER BRAKE

POWER BRAKE

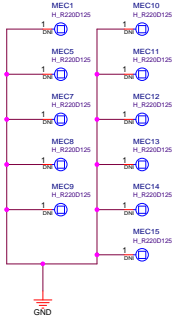
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Brackets:



Mechanical Holes Symbol



GPU Stiffner

