P615-A01,G96-GB1-128,MXM-III,512/256MB GDDR3(32/16Mx32),LVDS,HDMI,DP,VGA,HD AUDIO

MXM 2.1A SPECIFICATION COMPLIANT

Table of Contents

SKU	VARIANT	NVPN	ASSEMBLY
B	Base	600-10615-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY
1	SKU0001	600-10615-0001-000	NB9E-GE G96 650MHz, 512MB(128bit) GDDR3 32Mx32, LVDS,HDMI,TV,DP,HD_AUDIO
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PAGE OVERVIEW

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10615-0001-100 A		
ID	design	PAGE	1 OF 19
NAME	dhao	DATE	18-SEP-2007

PCI EXPRESS

CN1
CON_MXM_HE_EDGE
NONPHY-HE
NONPHY-HE
COMMON

1/2 PCI-Express, Power

3V3_RUN
C3 .1UF 16V 10% X7R 0402 COMMON
C4 .1UF 16V 10% X7R 0402 COMMON
238 3V3RUN (1.5A)

1V8_RUN
C75 .1UF 16V 10% X7R 0402 COMMON
2 1V8RUN (3.5A)

PWR_SRC
C541 .1UF 25V 10% X7R 0603 COMMON
C501 .1UF 25V 10% X7R 0603 COMMON
C542 .1UF 25V 10% X7R 0603 COMMON
1 PWR_SRC (14A)

2V5_RUN
C11 .1UF 16V 10% X7R 0402 COMMON
234 2V5RUN (0.5A)

5V_RUN
C79 .1UF 16V 10% X7R 0402 COMMON
18 5VRUN (0.5A)

17 20 41 44 47 50 53 56 59 62 65 68 71 74 77 80 83 86 89 92 95 98 101 104 107 110 113 116 119 122 125 128 131 138 142 150 154 158 163 164 175 176 181 182 187 188 194 199 205 206 211 212 218 223 229 235 236 241 E2 GND

R79 0 5% 0402 COMMON

R74 0 0402 5% NO STUFF

NO STUFF FOR PRODUCTION
Place to the bottom side for test usage.
R564 100 0402 5% NO STUFF

CLK_REQ	137	PEX_CLKREQ*											
PEX_RST	139												
PEX_REFCLK	135												
PEX_REFCLK	133												
PEX_RX0	129	PEX_TX0_C	PEX_TX0_C	90DIFF	1	C661 .1UF 0402 16V 10% X7R COMMON							
PEX_RX0	127	PEX_TX0_C*	PEX_TX0_C	90DIFF	1		C655 .1UF 0402 16V 10% X7R COMMON						
PEX_TX0	132												
PEX_TX0	130												
PEX_RX1	123	PEX_TX1_C	PEX_TX1_C	90DIFF	1	C650 .1UF 0402 16V 10% X7R COMMON							
PEX_RX1	121	PEX_TX1_C*	PEX_TX1_C	90DIFF	1		C642 .1UF 0402 16V 10% X7R COMMON						
PEX_TX1	126												
PEX_TX1	124												
PEX_RX2	117	PEX_TX2_C	PEX_TX2_C	90DIFF	1	C639 .1UF 0402 16V 10% X7R COMMON							
PEX_RX2	115	PEX_TX2_C*	PEX_TX2_C	90DIFF	1		C631 .1UF 0402 16V 10% X7R COMMON						
PEX_TX2	120												
PEX_TX2	118												
PEX_RX3	111	PEX_TX3_C	PEX_TX3_C	90DIFF	1	C627 .1UF 0402 16V 10% X7R COMMON							
PEX_RX3	109	PEX_TX3_C*	PEX_TX3_C	90DIFF	1		C621 .1UF 0402 16V 10% X7R COMMON						
PEX_TX3	114												
PEX_TX3	112												
PEX_RX4	105	PEX_TX4_C	PEX_TX4_C	90DIFF	1	C619 .1UF 0402 16V 10% X7R COMMON							
PEX_RX4	103	PEX_TX4_C*	PEX_TX4_C	90DIFF	1		C614 .1UF 0402 16V 10% X7R COMMON						
PEX_TX4	108												
PEX_TX4	106												
PEX_RX5	99	PEX_TX5_C	PEX_TX5_C	90DIFF	1	C611 .1UF 0402 16V 10% X7R COMMON							
PEX_RX5	97	PEX_TX5_C*	PEX_TX5_C	90DIFF	1		C607 .1UF 0402 16V 10% X7R COMMON						
PEX_TX5	102												
PEX_TX5	100												
PEX_RX6	93	PEX_TX6_C	PEX_TX6_C	90DIFF	1	C602 .1UF 0402 16V 10% X7R COMMON							
PEX_RX6	91	PEX_TX6_C*	PEX_TX6_C	90DIFF	1		C596 .1UF 0402 16V 10% X7R COMMON						
PEX_TX6	96												
PEX_TX6	94												
PEX_RX7	87	PEX_TX7_C	PEX_TX7_C	90DIFF	1	C592 .1UF 0402 16V 10% X7R COMMON							
PEX_RX7	85	PEX_TX7_C*	PEX_TX7_C	90DIFF	1		C590 .1UF 0402 16V 10% X7R COMMON						
PEX_TX7	90												
PEX_TX7	88												
PEX_RX8	81	PEX_TX8_C	PEX_TX8_C	90DIFF	1	C587 .1UF 0402 16V 10% X7R COMMON							
PEX_RX8	79	PEX_TX8_C*	PEX_TX8_C	90DIFF	1		C582 .1UF 0402 16V 10% X7R COMMON						
PEX_TX8	84												
PEX_TX8	82												
PEX_RX9	75	PEX_TX9_C	PEX_TX9_C	90DIFF	1	C580 .1UF 0402 16V 10% X7R COMMON							
PEX_RX9	73	PEX_TX9_C*	PEX_TX9_C	90DIFF	1		C573 .1UF 0402 16V 10% X7R COMMON						
PEX_TX9	78												
PEX_TX9	76												
PEX_RX10	69	PEX_TX10_C	PEX_TX10_C	90DIFF	1	C570 .1UF 0402 16V 10% X7R COMMON							
PEX_RX10	67	PEX_TX10_C*	PEX_TX10_C	90DIFF	1		C569 .1UF 0402 16V 10% X7R COMMON						
PEX_TX10	72												
PEX_TX10	70												
PEX_RX11	63	PEX_TX11_C	PEX_TX11_C	90DIFF	1	C568 .1UF 0402 16V 10% X7R COMMON							
PEX_RX11	61	PEX_TX11_C*	PEX_TX11_C	90DIFF	1		C566 .1UF 0402 16V 10% X7R COMMON						
PEX_TX11	66												
PEX_TX11	64												
PEX_RX12	57	PEX_TX12_C	PEX_TX12_C	90DIFF	1	C565 .1UF 0402 16V 10% X7R COMMON							
PEX_RX12	55	PEX_TX12_C*	PEX_TX12_C	90DIFF	1		C562 .1UF 0402 16V 10% X7R COMMON						
PEX_TX12	60												
PEX_TX12	58												
PEX_RX13	51	PEX_TX13_C	PEX_TX13_C	90DIFF	1	C561 .1UF 0402 16V 10% X7R COMMON							
PEX_RX13	49	PEX_TX13_C*	PEX_TX13_C	90DIFF	1		C559 .1UF 0402 16V 10% X7R COMMON						
PEX_TX13	54												
PEX_TX13	52												
PEX_RX14	45	PEX_TX14_C	PEX_TX14_C	90DIFF	1	C555 .1UF 0402 16V 10% X7R COMMON							
PEX_RX14	43	PEX_TX14_C*	PEX_TX14_C	90DIFF	1		C553 .1UF 0402 16V 10% X7R COMMON						
PEX_TX14	48												
PEX_TX14	46												
PEX_RX15	39	PEX_TX15_C	PEX_TX15_C	90DIFF	1	C552 .1UF 0402 16V 10% X7R COMMON							
PEX_RX15	37	PEX_TX15_C*	PEX_TX15_C	90DIFF	1		C551 .1UF 0402 16V 10% X7R COMMON						
PEX_TX15	42												
PEX_TX15	40												

PRSNT1 134
PEX_LSW 38 PEX_PRSNT* R94 0 0402 5% COMMON PEX_PRSNT_R* OUT 19.4A<

LOW: Low Swing Mode
Floating: Stand Mode

G1
696-400-A1 DT
BGA969
COMMON

1/16 PCI_EXPRESS

PEX_RST	AM16	PEX_RST											
PEX_CLKREQ	AR13	PEX_CLKREQ											
PEX_TSTCLK_OUT	AJ17	PEX_TSTCLK_OUT	90DIFF	1	PEX_TCLK	PEX_PLL_CLK_OUT							
PEX_TSTCLK_OUT	AJ18	PEX_TSTCLK_OUT*	90DIFF	1	PEX_TCLK	PEX_PLL_CLK_OUT*							
PEX_REFCLK	AR16	PEX_REFCLK	100DIFF	1	PEX_RCLK	PEX_REFCLK							
PEX_REFCLK	AR17	PEX_REFCLK*	100DIFF	1	PEX_RCLK	PEX_REFCLK*							
PEX_TX0	AL17	PEX_TX0	90DIFF	1	PEX_TX0	PEX_TX0							
PEX_TX0	AM17	PEX_TX0*	90DIFF	1	PEX_TX0	PEX_TX0*							
PEX_RX0	AP17	PEX_RX0	90DIFF	1	PEX_RX0	PEX_RX0							
PEX_RX0	AN17	PEX_RX0*	90DIFF	1	PEX_RX0	PEX_RX0*							
PEX_TX1	AM18	PEX_TX1	90DIFF	1	PEX_TX1	PEX_TX1							
PEX_TX1	AM19	PEX_TX1*	90DIFF	1	PEX_TX1	PEX_TX1*							
PEX_RX1	AN19	PEX_RX1	90DIFF	1	PEX_RX1	PEX_RX1							
PEX_RX1	AP19	PEX_RX1*	90DIFF	1	PEX_RX1	PEX_RX1*							
PEX_TX2	AL19	PEX_TX2	90DIFF	1	PEX_TX2	PEX_TX2							
PEX_TX2	AK19	PEX_TX2*	90DIFF	1	PEX_TX2	PEX_TX2*							
PEX_RX2	AR19	PEX_RX2	90DIFF	1	PEX_RX2	PEX_RX2							
PEX_RX2	AR20	PEX_RX2*	90DIFF	1	PEX_RX2	PEX_RX2*							
PEX_TX3	AL20	PEX_TX3	90DIFF	1	PEX_TX3	PEX_TX3							
PEX_TX3	AM20	PEX_TX3*	90DIFF	1	PEX_TX3	PEX_TX3*							
PEX_RX3	AP20	PEX_RX3	90DIFF	1	PEX_RX3	PEX_RX3							
PEX_RX3	AN20	PEX_RX3*	90DIFF	1	PEX_RX3	PEX_RX3*							
PEX_TX4	AM21	PEX_TX4	90DIFF	1	PEX_TX4	PEX_TX4							
PEX_TX4	AM22	PEX_TX4*	90DIFF	1	PEX_TX4	PEX_TX4*							
PEX_RX4	AN22	PEX_RX4	90DIFF	1	PEX_RX4	PEX_RX4							
PEX_RX4	AP22	PEX_RX4*	90DIFF	1	PEX_RX4	PEX_RX4*							
PEX_TX5	AL22	PEX_TX5	90DIFF	1	PEX_TX5	PEX_TX5							
PEX_TX5	AK22	PEX_TX5*	90DIFF	1	PEX_TX5	PEX_TX5*							
PEX_RX5	AR22	PEX_RX5	90DIFF	1	PEX_RX5	PEX_RX5							
PEX_RX5	AR23	PEX_RX5*	90DIFF	1	PEX_RX5	PEX_RX5*							
PEX_TX6	AL23	PEX_TX6	90DIFF	1	PEX_TX6	PEX_TX6							
PEX_TX6	AM23	PEX_TX6*	90DIFF	1	PEX_TX6	PEX_TX6*							
PEX_RX6	AP23	PEX_RX6	90DIFF	1	PEX_RX6	PEX_RX6							
PEX_RX6	AN23	PEX_RX6*	90DIFF	1	PEX_RX6	PEX_RX6*							
PEX_TX7	AM24	PEX_TX7	90DIFF	1	PEX_TX7	PEX_TX7							
PEX_TX7	AM25	PEX_TX7*	90DIFF	1	PEX_TX7	PEX_TX7*							
PEX_RX7	AN25	PEX_RX7	90DIFF	1	PEX_RX7	PEX_RX7							
PEX_RX7	AP25	PEX_RX7*	90DIFF	1	PEX_RX7	PEX_RX7*							
PEX_TX8	AL25	PEX_TX8	90DIFF	1	PEX_TX8	PEX_TX8							
PEX_TX8	AK25	PEX_TX8*	90DIFF	1	PEX_TX8	PEX_TX8*							
PEX_RX8	AR25	PEX_RX8	90DIFF	1	PEX_RX8	PEX_RX8							
PEX_RX8	AR26	PEX_RX8*	90DIFF	1	PEX_RX8	PEX_RX8*							
PEX_TX9	AL26	PEX_TX9	90DIFF	1	PEX_TX9	PEX_TX9							
PEX_TX9	AM26	PEX_TX9*	90DIFF	1	PEX_TX9	PEX_TX9*							
PEX_RX9	AP26	PEX_RX9	90DIFF	1	PEX_RX9	PEX_RX9							
PEX_RX9	AN26	PEX_RX9*	90DIFF	1	PEX_RX9	PEX_RX9*							
PEX_TX10	AM27	PEX_TX10	90DIFF	1	PEX_TX10	PEX_TX10							
PEX_TX10	AM28	PEX_TX10*	90DIFF	1	PEX_TX10	PEX_TX10*							
PEX_RX10	AN28	PEX_RX10	90DIFF	1	PEX_RX10	PEX_RX10							
PEX_RX10	AP28	PEX_RX10*	90DIFF	1	PEX_RX10	PEX_RX10*							
PEX_TX11	AL28	PEX_TX11	90DIFF	1	PEX_TX11	PEX_TX11							
PEX_TX11	AK28	PEX_TX11*	90DIFF	1	PEX_TX11	PEX_TX11*							
PEX_RX11	AR28	PEX_RX11	90DIFF	1	PEX_RX11	PEX_RX11							
PEX_RX11	AR29	PEX_RX11*	90DIFF	1	PEX_RX11	PEX_RX11*							
PEX_TX12	AK29	PEX_TX12	90DIFF	1	PEX_TX12	PEX_TX12							
PEX_TX12	AL29	PEX_TX12*	90DIFF	1	PEX_TX12	PEX_TX12*							
PEX_RX12	AP29	PEX_RX12	90DIFF	1	PEX_RX12	PEX_RX12							
PEX_RX12	AN29	PEX_RX12*	90DIFF	1	PEX_RX12	PEX_RX12*							
PEX_TX13	AM29	PEX_TX13	90DIFF	1	PEX_TX13	PEX_TX13							
PEX_TX13	AM30	PEX_TX13*	90DIFF	1	PEX_TX13	PEX_TX13*							
PEX_RX13	AN31	PEX_RX13	90DIFF	1	PEX_RX13	PEX_RX13							
PEX_RX13	AP31	PEX_RX13*	90DIFF	1	PEX_RX13	PEX_RX13*							
PEX_TX14	AM31	PEX_TX14	90DIFF	1	PEX_TX14	PEX_TX14							
PEX_TX14	AM32	PEX_TX14*	90DIFF	1	PEX_TX14	PEX_TX14*							
PEX_RX14	AR31	PEX_RX14	90DIFF	1	PEX_RX14	PEX_RX14							
PEX_RX14	AR32	PEX_RX14*	90DIFF	1	PEX_RX14	PEX_RX14*							
PEX_TX15	AN32	PEX_TX15	90DIFF	1	PEX_TX15	PEX_TX15							
PEX_TX15	AP32	PEX_TX15*	90DIFF	1	PEX_TX15	PEX_TX15*							
PEX_RX15	AR34	PEX_RX15	90DIFF	1	PEX_RX15	PEX_RX15							
PEX_RX15	AP34	PEX_RX15*	90DIFF	1	PEX_RX15	PEX_RX15*							

PEX_IOVDD AK16 AK17 AK21 AK24 AK27

PEX_IOVDDQ AG11 AG12 AG13 AG15 AG16 AG17 AG18 AG22 AG23 AG24 AG25 AG26 AJ14 AJ15 AJ19 AJ21 AJ22 AJ24 AJ25 AJ27 AK18 AK20 AK23 AK26 AL16

CLOSE TO BALLS

PEX_VDD
C606 .1UF 16V 10% X7R 0402 COMMON
C624 .1UF 16V 10% X7R 0402 COMMON
C622 1UF 6.3V 10% X5R 0402 COMMON
C597 1UF 6.3V 10% X7R 0603 COMMON
C589 4.7UF 6.3V 10% X5R 0603 COMMON
C708 4.7UF 6.3V 10% X5R 0603 COMMON
C645 10UF 6.3V 20% X5R 0805 COMMON
C560 .1UF 16V 10% X7R 0402 COMMON
C571 .1UF 16V 10% X7R 0402 COMMON
C610 1UF 6.3V 10% X5R 0402 COMMON
C73 1UF 6.3V 10% X7R 0603 COMMON
GND

NC_1 A2 SNN_NC<1>
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NC_3 AD6 SNN_NC<3>
NC_4 AF6 SNN_NC<4>
NC_5 AG6 SNN_NC<5>
NC_6 AJ5 SNN_NC<6>
NC_7 AK15 SNN_NC<7>
NC_8 AL7 SNN_NC<8>
NC_9 D35 SNN_NC<9>
NC_10 E35 SNN_NC<10>
NC_11 E7 SNN_NC<11>
NC_12 F7 SNN_NC<12>
NC_13 H32 SNN_NC<13>
NC_14 M7 SNN_NC<14>
NC_15 P6 SNN_NC<15>
NC_16 P7 SNN_NC<16>
NC_17 R7 SNN_NC<17>
NC_18 U7 SNN_NC<18>
NC_19 V6 SNN_NC<19>

3V3_RUN
VDD33_1 J10
VDD33_2 J11
VDD33_3 J12
VDD33_4 J13
VDD33_5 J9
C660 .1UF 16V 10% X7R 0402 COMMON
C641 1UF 6.3V 10% X5R 0402 COMMON
GND

VDD_SENSE AD20 NVVDD_SENSE OUT 2.5G<> 17.4H<
GND_SENSE AD19 NVVDD_GND_SENSE OUT 2.5G<> 17.4H<

L<750mil
DP_PWR_VDD
PEX_PLLVDD AG14 PEX_PLLVDD
C634 .01UF 16V 10% X7R 0402 COMMON
C706 .1UF 16V 10% X7R 0402 COMMON
C670 1UF 6.3V 10% X5R 0402 COMMON
C663 4.7UF 6.3V 10% X5R 0603 COMMON
L501 10nH 0603 COMMON
C707 10UF 6.3V 20% X5R 0805 COMMON
GND

PEX_VDD 17.4H< 17.4H<
PEX_RFU1 AG19 PEX_CAL_PD_VDDQ R560 2.49K 0402 1% COMMON
PEX_RFU2 AG20 PEX_CAL_PU_GND R559 2.49K 0402 1% COMMON
PEX_TERMP AG21 PEX_TERMP R558 2.49K 0402 1% COMMON
TESTMODE AP35 GPU_TESTMODE R92 1K 0402 5% COMMON
GND

		MIN_LINE_WIDTH	VOLTAGE
BI	NVVDD_SENSE	10MIL	1.0V
BI	NVVDD_GND_SENSE	10MIL	0V
BI	PEX_PLLVDD	10MIL	1.1V

SOURCE_PWR_NET	VOLTAGE	MAX_CURRENT	MIN_LINE_WIDTH
PWR_SRC	22V	16.0A	24MIL
1V8_RUN	1.8V	3.5A	24MIL
2V5_RUN	2.5V	0.5A	16MIL
3V3_RUN	3.3V	1.5A	16MIL
5V_RUN	5V	0.5A	16MIL

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10615-0001-100 A		
ID	design	PAGE	2 OF 19
NAME	dhao	DATE	18-SEP-2007

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS

GPU MEMORY INTERFACE: PARTITION A

G1
G96-400-A1 DT
BGA969
COMMON

2/16 FBA

FBA_D0	R30	0 FBA_D<0>
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FBA_D2	P31	2 FBA_D<2>
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FBA_D4	L31	4 FBA_D<4>
FBA_D5	M32	5 FBA_D<5>
FBA_D6	M30	6 FBA_D<6>
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FBA_D8	P33	8 FBA_D<8>
FBA_D9	P34	9 FBA_D<9>
FBA_D10	N35	10 FBA_D<10>
FBA_D11	P35	11 FBA_D<11>
FBA_D12	N34	12 FBA_D<12>
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FBA_D57	AH33	57 FBA_D<57>
FBA_D58	AH35	58 FBA_D<58>
FBA_D59	AH32	59 FBA_D<59>
FBA_D60	AH34	60 FBA_D<60>
FBA_D61	AM34	61 FBA_D<61>
FBA_D62	AL35	62 FBA_D<62>
FBA_D63	AJ33	63 FBA_D<63>

4.4F> 4.4A<> BI FBA_D<63..0>

FBA_DQM0	P30	0 FBA_DQM<0>
FBA_DQM1	P32	1 FBA_DQM<1>
FBA_DQM2	J30	2 FBA_DQM<2>
FBA_DQM3	H34	3 FBA_DQM<3>
FBA_DQM4	AF32	4 FBA_DQM<4>
FBA_DQM5	AF35	5 FBA_DQM<5>
FBA_DQM6	AL32	6 FBA_DQM<6>
FBA_DQM7	AL34	7 FBA_DQM<7>

4.4F> 4.4A<> BI FBA_DQM<7..0>

FBA_DQS_WP0	N31	0 FBA_DQS_WP<0>
FBA_DQS_WP1	L34	1 FBA_DQS_WP<1>
FBA_DQS_WP2	J32	2 FBA_DQS_WP<2>
FBA_DQS_WP3	H35	3 FBA_DQS_WP<3>
FBA_DQS_WP4	AE31	4 FBA_DQS_WP<4>
FBA_DQS_WP5	AC33	5 FBA_DQS_WP<5>
FBA_DQS_WP6	AJ32	6 FBA_DQS_WP<6>
FBA_DQS_WP7	AJ34	7 FBA_DQS_WP<7>

4.5A<> 4.4F> BI FBA_DQS_WP<7..0>

FBA_DQS_RN0	N32	0 FBA_DQS_RN<0>
FBA_DQS_RN1	L35	1 FBA_DQS_RN<1>
FBA_DQS_RN2	H31	2 FBA_DQS_RN<2>
FBA_DQS_RN3	G35	3 FBA_DQS_RN<3>
FBA_DQS_RN4	AD32	4 FBA_DQS_RN<4>
FBA_DQS_RN5	AC34	5 FBA_DQS_RN<5>
FBA_DQS_RN6	AJ31	6 FBA_DQS_RN<6>
FBA_DQS_RN7	AJ35	7 FBA_DQS_RN<7>

4.4F< 4.4A<> IN FBA_DQS_RN<7..0>

RFU	P29	SNN_FBA_WDS0
RFU	R29	SNN_FBA_WDS0*
RFU	L29	SNN_FBA_WDS1
RFU	M29	SNN_FBA_WDS1*
RFU	AD29	SNN_FBA_WDS2
RFU	AE29	SNN_FBA_WDS2*
RFU	AG29	SNN_FBA_WDS3
RFU	AH29	SNN_FBA_WDS3*

FBVDDQ	J23	
FBVDDQ	J24	
FBVDDQ	J29	
FBVDDQ	AA27	
FBVDDQ	AA29	
FBVDDQ	AA31	
FBVDDQ	AB27	
FBVDDQ	AB29	
FBVDDQ	AC27	
FBVDDQ	AD27	
FBVDDQ	AE27	
FBVDDQ	AJ28	
FBVDDQ	B18	
FBVDDQ	E21	
FBVDDQ	G17	
FBVDDQ	G18	
FBVDDQ	G22	
FBVDDQ	G8	
FBVDDQ	G9	
FBVDDQ	H29	
FBVDDQ	J14	
FBVDDQ	J15	
FBVDDQ	J16	
FBVDDQ	J17	
FBVDDQ	J20	
FBVDDQ	J21	
FBVDDQ	J22	

FBVDDQ

C574 .1UF 16V 10% X7R 0402 COMMON
C629 .1UF 16V 10% X7R 0402 COMMON
C595 .1UF 16V 10% X7R 0402 COMMON
C506 1UF 6.3V 10% X7R 0603 COMMON
C524 1UF 6.3V 10% X7R 0603 COMMON
C535 4.7UF 6.3V 10% X5R 0603 COMMON
C623 .1UF 16V 10% X7R 0402 COMMON
C572 .1UF 16V 10% X7R 0402 COMMON
C575 .1UF 16V 10% X7R 0402 COMMON
C539 1UF 6.3V 10% X7R 0603 COMMON
C540 1UF 6.3V 10% X7R 0603 COMMON
C526 4.7UF 6.3V 10% X5R 0603 COMMON
GND

FBA_CMD<27..0> OUT 4.1A< 4.4F<

FBA_CMD0	V32	FBA_CMD<0>	0
FBA_CMD1	W31	FBA_CMD<1>	1
FBA_CMD2	U31	FBA_CMD<2>	2
FBA_CMD3	Y32	FBA_CMD<3>	3
FBA_CMD4	AB35	FBA_CMD<4>	4
FBA_CMD5	AB34	FBA_CMD<5>	5
FBA_CMD6	W35	FBA_CMD<6>	6
FBA_CMD7	W33	SNN_FBA_CMD7	
FBA_CMD8	W30	FBA_CMD<8>	8
FBA_CMD9	T34	FBA_CMD<9>	9
FBA_CMD10	T35	FBA_CMD<10>	10
FBA_CMD11	AB31	FBA_CMD<11>	11
FBA_CMD12	Y30	FBA_CMD<12>	12
FBA_CMD13	Y34	FBA_CMD<13>	13
FBA_CMD14	W32	FBA_CMD<14>	14
FBA_CMD15	AA30	FBA_CMD<15>	15
FBA_CMD16	AA32	FBA_CMD<16>	16
FBA_CMD17	Y33	FBA_CMD<17>	17
FBA_CMD18	U32	FBA_CMD<18>	18
FBA_CMD19	Y31	FBA_CMD<19>	19
FBA_CMD20	U34	FBA_CMD<20>	20
FBA_CMD21	Y35	FBA_CMD<21>	21
FBA_CMD22	W34	FBA_CMD<22>	22
FBA_CMD23	V30	FBA_CMD<23>	23
FBA_CMD24	U35	FBA_CMD<24>	24
FBA_CMD25	U30	FBA_CMD<25>	25
FBA_CMD26	U33	SNN_FBA_CMD26	
FBA_CMD27	AB30	FBA_CMD<27>	27
FBA_CMD28	AB33	SNN_FBA_CMD28	
FBA_CMD29	T33	SNN_FBA_CMD29	
FBA_CMD30	W29	SNN_FBA_CMD30	

FBA_CLK0	T32	FBA_CLK0	OUT 4.2A< 4.4F<
FBA_CLK0	T31	FBA_CLK0*	OUT 4.2A< 4.4F<
FBA_CLK1	AC31	FBA_CLK1	OUT 4.2D< 4.4F<
FBA_CLK1	AC30	FBA_CLK1*	OUT 4.2D< 4.4F<

FBA_DEBUG T30 FBA_DEBUG R546 40.2 0402 1% "NO STUFF" FBVDDQ

FB_DLLAVDD AG27
FB_PLLAVDD AF27 FB_PLLAVDD OUT 3.5G<> 6.5G<>

LOW PERF: VREF = 0.50 * FBVDDQ

HIGH PERF: VREF = 0.70 * FBVDDQ

VREF = FBVDDQ * Rbot/(Rtop + Rbot)

VREF	RTop	RBot	FBVDDQ	PERF MODE	GPIO10
0.77V	549	1k33 || 931	1.55V	Low	High
0.90V	549	1k32 || 931	1.8V	Low	High
1.09V	549	1k33	1.55V	High	Low
1.26V	549	1k33	1.8V	High	Low

FBVDDQ
R553 549 1% 0402 COMMON Rtop
FB_VREF1 J27 FB_VREF
R555 Rbot1 931 1% 0402 COMMON
R554 1.33K 1% 0402 COMMON Rbot
C576 .01UF 16V 10% X7R 0402 COMMON
GND
FBAC_VREF_CTL 3
1G1D1S Q504 NTS4001NT1G SOT323_1G1D1S COMMON
MAX_VOLTAGE=30V CONT DRAIN_CURRENT=215MA MAX_CURRENT=600MA MAX_WATTAGE=150MW V_BE_SS=+/-20V
14.3G> 7.1H< 4.1H< IN GPIO10_FB_VREF_SW
GND

NET	MIN_LINE_WIDTH	VOLTAGE
3.4F> 6.5C< BI FB_PLLAVDD	10MIL	1.1V
BI FB_VREF1	12MIL	1.26V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	FBA MEMORY INTERFACE & FBVDDQ DECOUPLING CAPS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10615-0001-100 A		
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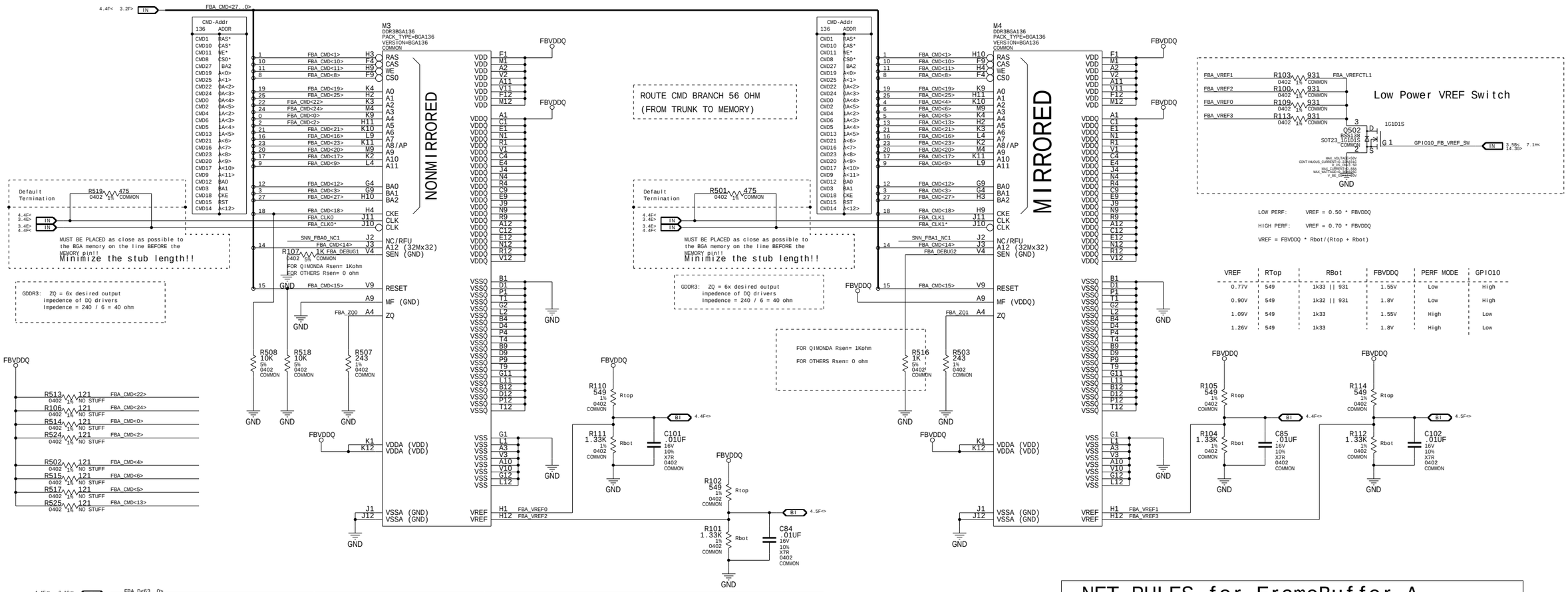
NAME	dhao	DATE	18-SEP-2007

FRAME BUFFER PARTITION A



NET RULES for FrameBuffer A

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBA_CLK0	1	80DIFF	FBA_CLK0
FBA_CLK0*	1	80DIFF	FBA_CLK0
FBA_CLK1	1	80DIFF	FBA_CLK1
FBA_CLK1*	1	80DIFF	FBA_CLK1
FBA_DQS_WP<7..0>	1	50OHM	
FBA_DQS_RN<7..0>	1	50OHM	
FBA_DQM<7..0>	1	50OHM	
FBA_D<63..0>	1	50OHM	
FBA_CMD<27..0>	1	50OHM	

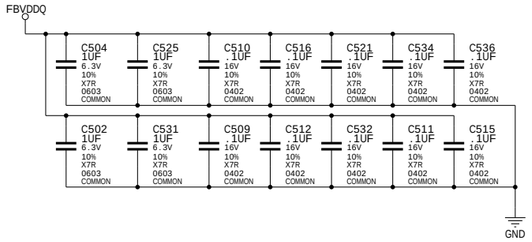
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBA_VREF0	1.26V	0.02A	12MIL
FBA_VREF1	1.26V	0.02A	12MIL
FBA_VREF2	1.26V	0.02A	12MIL
FBA_VREF3	1.26V	0.02A	12MIL
FBA_ZQ0	1.26V	0.02A	12MIL
FBA_ZQ1	1.26V	0.02A	12MIL

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FRAME BUFFER A MEMORIES

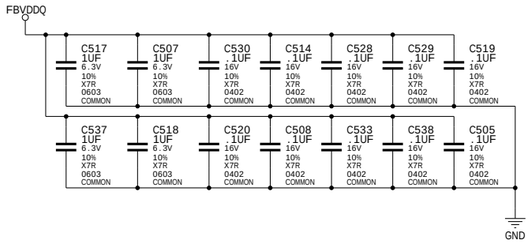
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10615-0001-100 A		
ID	design	PAGE	4 OF 19
NAME	dhao	DATE	12-JAN-2007

FRAME BUFFER: PARTITION A DECOUPLING

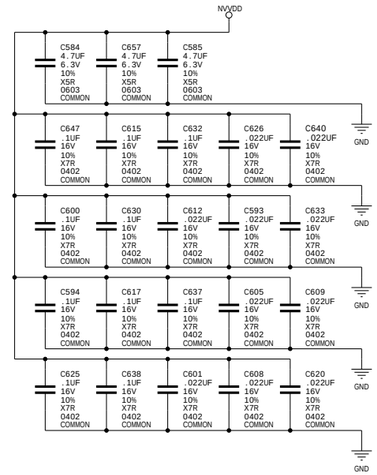


Decoupling for M3



Decoupling for M4

NVVDD POWER AND DECOUPLING



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	FBA & NVVDD DECOUPLING CAPS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10615-0001-100 A		
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GPU MEMORY INTERFACE: PARTITION C

NET	MIN_LINE_WIDTH
FB_CAL_PD_VDDQ	10MIL
FB_CAL_PU_GND	10MIL
FB_CAL_TERM_GND	10MIL

7.4F<> 7.4A<> B1 FBC_D<63..0>

G1
G96-400-A1 DT
BGA969
COMMON

3/16 FBC

0	FBC_D<0>	D11	FBC_D0
1	FBC_D<1>	E11	FBC_D1
2	FBC_D<2>	F10	FBC_D2
3	FBC_D<3>	D8	FBC_D3
4	FBC_D<4>	F8	FBC_D4
5	FBC_D<5>	F9	FBC_D5
6	FBC_D<6>	E8	FBC_D6
7	FBC_D<7>	F12	FBC_D7
8	FBC_D<8>	B11	FBC_D8
9	FBC_D<9>	C13	FBC_D9
10	FBC_D<10>	A11	FBC_D10
11	FBC_D<11>	B8	FBC_D11
12	FBC_D<12>	A8	FBC_D12
13	FBC_D<13>	C8	FBC_D13
14	FBC_D<14>	C11	FBC_D14
15	FBC_D<15>	C10	FBC_D15
16	FBC_D<16>	D12	FBC_D16
17	FBC_D<17>	E13	FBC_D17
18	FBC_D<18>	F17	FBC_D18
19	FBC_D<19>	F15	FBC_D19
20	FBC_D<20>	F16	FBC_D20
21	FBC_D<21>	E16	FBC_D21
22	FBC_D<22>	F14	FBC_D22
23	FBC_D<23>	F13	FBC_D23
24	FBC_D<24>	D13	FBC_D24
25	FBC_D<25>	A13	FBC_D25
26	FBC_D<26>	B13	FBC_D26
27	FBC_D<27>	A14	FBC_D27
28	FBC_D<28>	C16	FBC_D28
29	FBC_D<29>	A17	FBC_D29
30	FBC_D<30>	B16	FBC_D30
31	FBC_D<31>	D16	FBC_D31
32	FBC_D<32>	D24	FBC_D32
33	FBC_D<33>	D26	FBC_D33
34	FBC_D<34>	E25	FBC_D34
35	FBC_D<35>	F25	FBC_D35
36	FBC_D<36>	F27	FBC_D36
37	FBC_D<37>	E28	FBC_D37
38	FBC_D<38>	F28	FBC_D38
39	FBC_D<39>	D29	FBC_D39
40	FBC_D<40>	A25	FBC_D40
41	FBC_D<41>	B25	FBC_D41
42	FBC_D<42>	D25	FBC_D42
43	FBC_D<43>	C26	FBC_D43
44	FBC_D<44>	C28	FBC_D44
45	FBC_D<45>	B28	FBC_D45
46	FBC_D<46>	A28	FBC_D46
47	FBC_D<47>	A29	FBC_D47
48	FBC_D<48>	E29	FBC_D48
49	FBC_D<49>	F29	FBC_D49
50	FBC_D<50>	D30	FBC_D50
51	FBC_D<51>	E31	FBC_D51
52	FBC_D<52>	C33	FBC_D52
53	FBC_D<53>	D33	FBC_D53
54	FBC_D<54>	F32	FBC_D54
55	FBC_D<55>	E32	FBC_D55
56	FBC_D<56>	B29	FBC_D56
57	FBC_D<57>	C29	FBC_D57
58	FBC_D<58>	B31	FBC_D58
59	FBC_D<59>	C31	FBC_D59
60	FBC_D<60>	B32	FBC_D60
61	FBC_D<61>	C32	FBC_D61
62	FBC_D<62>	B34	FBC_D62
63	FBC_D<63>	B35	FBC_D63

7.4F> 7.4A<> B1 FBC_DQM<7..0>

0	FBC_DQM<0>	F11	FBC_DQM0
1	FBC_DQM<1>	D10	FBC_DQM1
2	FBC_DQM<2>	D15	FBC_DQM2
3	FBC_DQM<3>	A16	FBC_DQM3
4	FBC_DQM<4>	D27	FBC_DQM4
5	FBC_DQM<5>	D28	FBC_DQM5
6	FBC_DQM<6>	D34	FBC_DQM6
7	FBC_DQM<7>	A34	FBC_DQM7

7.5A<> 7.4F> B1 FBC_DQS_WP<7..0>

0	FBC_DQS_WP<0>	E10	FBC_DQS_WP0
1	FBC_DQS_WP<1>	A10	FBC_DQS_WP1
2	FBC_DQS_WP<2>	D14	FBC_DQS_WP2
3	FBC_DQS_WP<3>	C14	FBC_DQS_WP3
4	FBC_DQS_WP<4>	E26	FBC_DQS_WP4
5	FBC_DQS_WP<5>	B26	FBC_DQS_WP5
6	FBC_DQS_WP<6>	D32	FBC_DQS_WP6
7	FBC_DQS_WP<7>	A32	FBC_DQS_WP7

7.4F< 7.4A<> B1 FBC_DQS_RN<7..0>

0	FBC_DQS_RN<0>	D9	FBC_DQS_RN0
1	FBC_DQS_RN<1>	B10	FBC_DQS_RN1
2	FBC_DQS_RN<2>	E14	FBC_DQS_RN2
3	FBC_DQS_RN<3>	B14	FBC_DQS_RN3
4	FBC_DQS_RN<4>	F26	FBC_DQS_RN4
5	FBC_DQS_RN<5>	A26	FBC_DQS_RN5
6	FBC_DQS_RN<6>	D31	FBC_DQS_RN6
7	FBC_DQS_RN<7>	A31	FBC_DQS_RN7

SNN_FBC_WDS0	G11	RFU
SNN_FBC_WDS0*	G12	RFU
SNN_FBC_WDS1	G14	RFU
SNN_FBC_WDS1*	G15	RFU
SNN_FBC_WDS2	G24	RFU
SNN_FBC_WDS2*	G25	RFU
SNN_FBC_WDS3	G27	RFU
SNN_FBC_WDS3*	G28	RFU

FBVDDQ

FBVDDQ	N27
FBVDDQ	P27
FBVDDQ	R27
FBVDDQ	T27
FBVDDQ	U27
FBVDDQ	U29
FBVDDQ	V27
FBVDDQ	V29
FBVDDQ	V34
FBVDDQ	W27
FBVDDQ	Y27

FBC_CMD<27..0> OUT 7.1A< 7.4F<

FBC_CMD0	C17	FBC_CMD<0>	0
FBC_CMD1	B19	FBC_CMD<1>	1
FBC_CMD2	D18	FBC_CMD<2>	2
FBC_CMD3	F21	FBC_CMD<3>	3
FBC_CMD4	A23	FBC_CMD<4>	4
FBC_CMD5	D21	FBC_CMD<5>	5
FBC_CMD6	B23	FBC_CMD<6>	6
FBC_CMD7	E20	SNN_FBC_CMD7	
FBC_CMD8	G21	FBC_CMD<8>	8
FBC_CMD9	F20	FBC_CMD<9>	9
FBC_CMD10	F19	FBC_CMD<10>	10
FBC_CMD11	F23	FBC_CMD<11>	11
FBC_CMD12	A22	FBC_CMD<12>	12
FBC_CMD13	C22	FBC_CMD<13>	13
FBC_CMD14	B17	FBC_CMD<14>	14
FBC_CMD15	F24	FBC_CMD<15>	15
FBC_CMD16	C25	FBC_CMD<16>	16
FBC_CMD17	E22	FBC_CMD<17>	17
FBC_CMD18	C20	FBC_CMD<18>	18
FBC_CMD19	B22	FBC_CMD<19>	19
FBC_CMD20	A19	FBC_CMD<20>	20
FBC_CMD21	D22	FBC_CMD<21>	21
FBC_CMD22	D20	FBC_CMD<22>	22
FBC_CMD23	E19	FBC_CMD<23>	23
FBC_CMD24	D19	FBC_CMD<24>	24
FBC_CMD25	F18	FBC_CMD<25>	25
FBC_CMD26	C19	SNN_FBC_CMD26	
FBC_CMD27	F22	FBC_CMD<27>	27
FBC_CMD28	C23	SNN_FBC_CMD28	
FBC_CMD29	B20	SNN_FBC_CMD29	
FBC_CMD30	A20	SNN_FBC_CMD30	

NET_NAME

FBC_CLK0	E17	FBC_CLK0	OUT 7.2A< 7.4F<
FBC_CLK0	D17	FBC_CLK0*	OUT 7.2A< 7.4F<
FBC_CLK1	D23	FBC_CLK1	OUT 7.2D< 7.4F<
FBC_CLK1	E23	FBC_CLK1*	OUT 7.2D< 7.4F<

FBVDDQ

FBC_DEBUG G19 FBC_DEBUG R561 40.2 0402 1% NO STUFF

L<750mil

G96 only	FBAC_DLLAVDD	J19	FB_PLLAVDD
	FBAC_PLLAVDD	J18	

CLOSE TO BALLS <100 mil

C613 .1UF 16V 10% X7R 0402 COMMON
C577 .1UF 16V 10% X7R 0402 COMMON
C618 2.2UF 6.3V 20% X5R 0402 COMMON
C583 4.7UF 6.3V 10% X5R 0603 COMMON
GND

IN 3.4F> 3.5G<>

PEX_VDD
240R@100MHz BEAD_0402 LB501 COMMON

FBVDDQ

FBCAL_PD_VDDQ	K27	FB_CAL_PD_VDDQ	R552	44.2 0402 1% COMMON
FBCAL_PU_GND	L27	FB_CAL_PU_GND	R556	30.9 0402 1% COMMON
FBCAL_TERM_GND	M27	FB_CAL_TERM_GND	R557	40.2 0402 1% COMMON

GND

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	FBC MEMORY INTERFACE

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	602-10615-0001-100 A		
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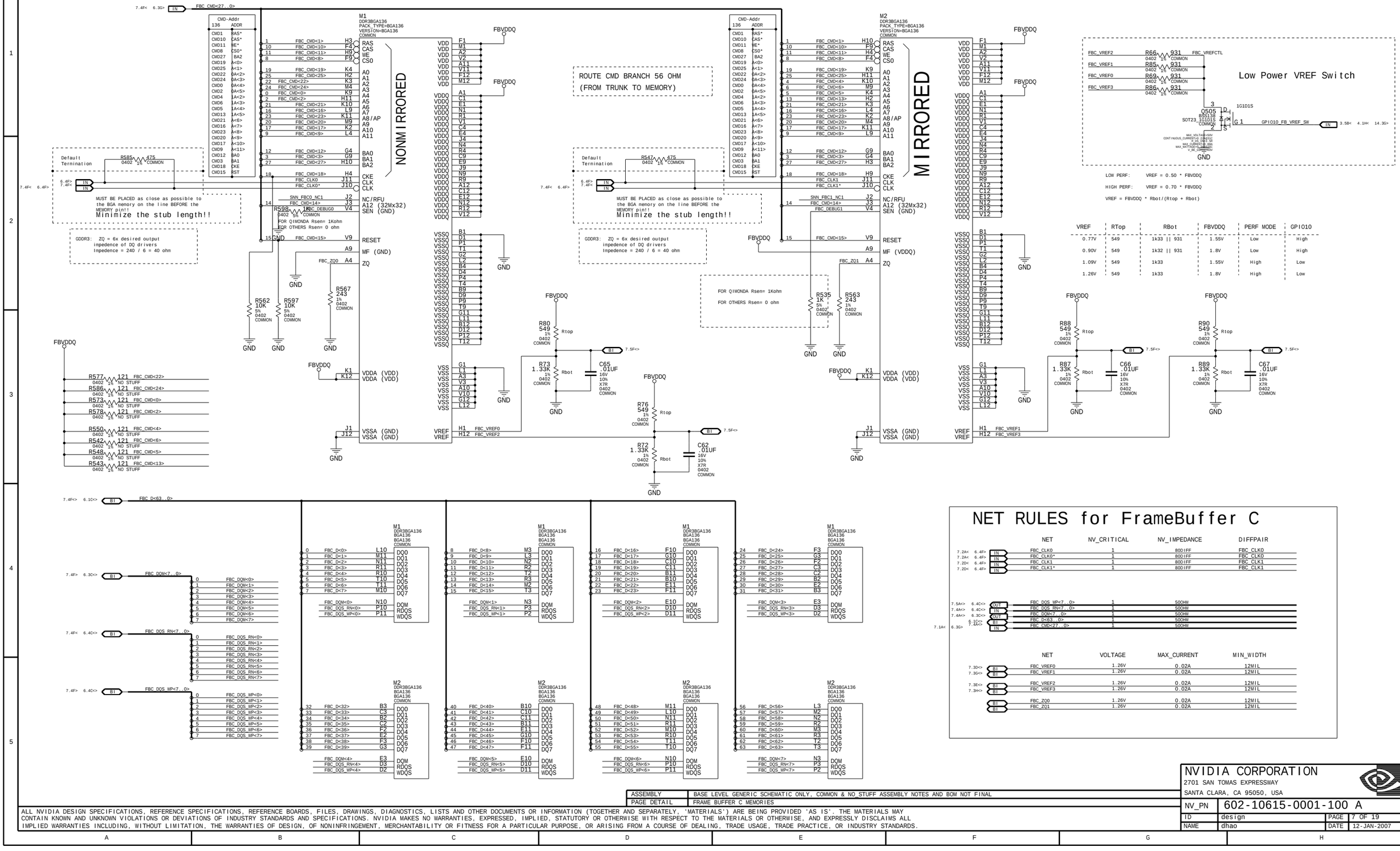
FRAME BUFFER PARTITION C



NET RULES for FrameBuffer C

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBC_CLK0	1	80DIFF	FBC_CLK0
FBC_CLK0*	1	80DIFF	FBC_CLK0
FBC_CLK1	1	80DIFF	FBC_CLK1
FBC_CLK1*	1	80DIFF	FBC_CLK1

NET	NV_CRITICAL	NV_IMPEDANCE
FBC_DQS_WP<7..0>	1	50OHM
FBC_DQS_RN<7..0>	1	50OHM
FBC_DQM<7..0>	1	50OHM
FBC_D<63..0>	1	50OHM
FBC_CMD<27..0>	1	50OHM

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBC_VREF0	1.26V	0.02A	12MIL
FBC_VREF1	1.26V	0.02A	12MIL
FBC_VREF2	1.26V	0.02A	12MIL
FBC_VREF3	1.26V	0.02A	12MIL
FBC_ZQ0	1.26V	0.02A	12MIL
FBC_ZQ1	1.26V	0.02A	12MIL

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FRAME BUFFER C MEMORIES

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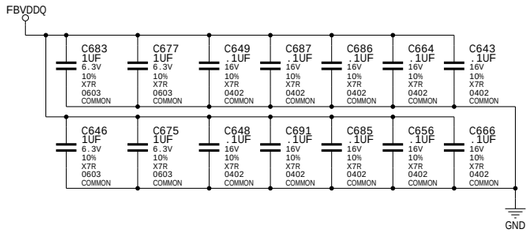
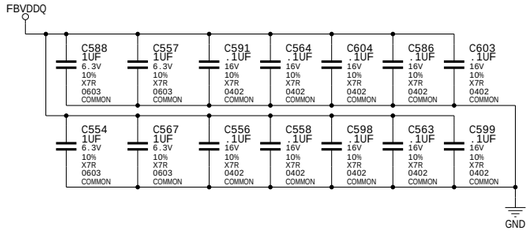
NAME	dhao	DATE	12-JAN-2007

FRAMEBUFFER: PARTITION C DECOUPLING

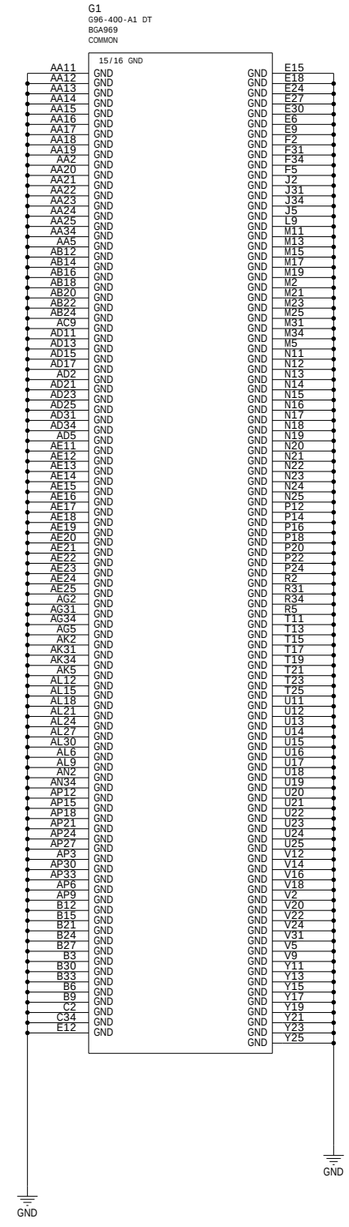


Decoupling for M1



Decoupling for M2

NVVDD GROUND



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	FBC DECOUPLING CAPS, GPU GND CONNECTIONS

NVIDIA CORPORATION
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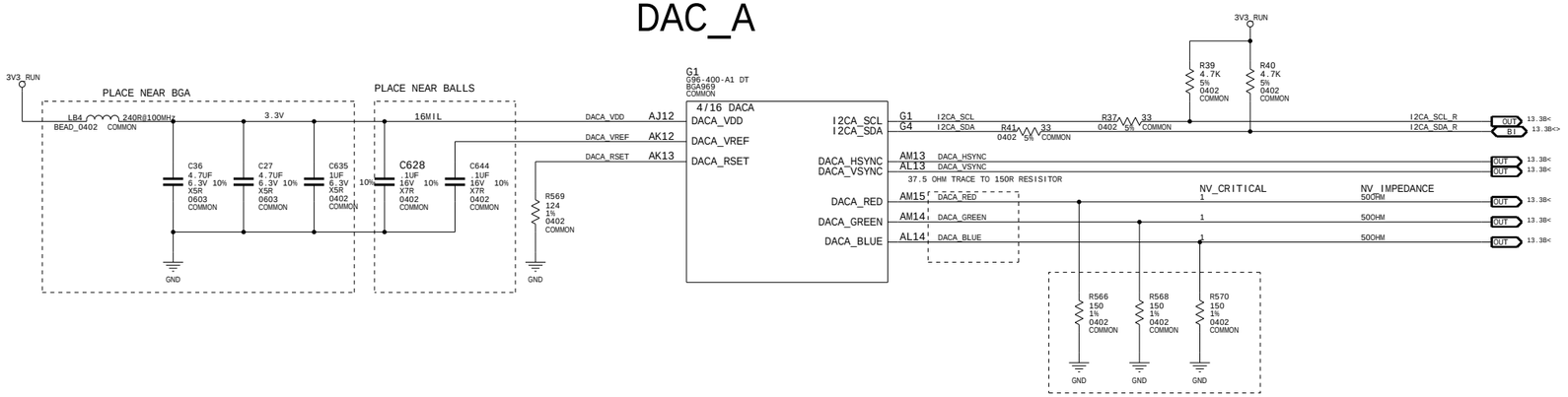
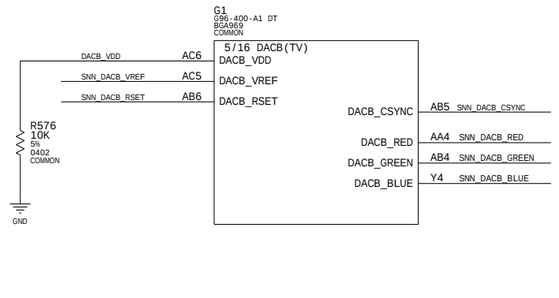
DAC_A

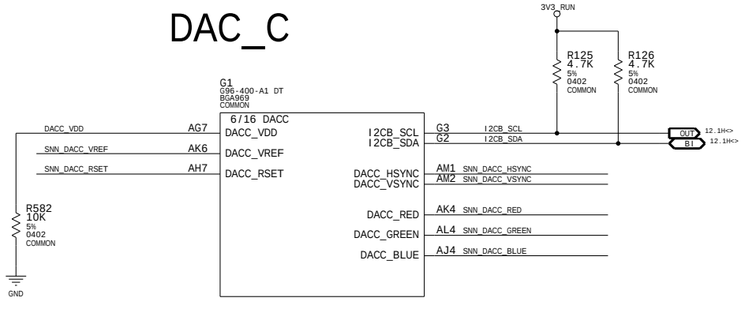


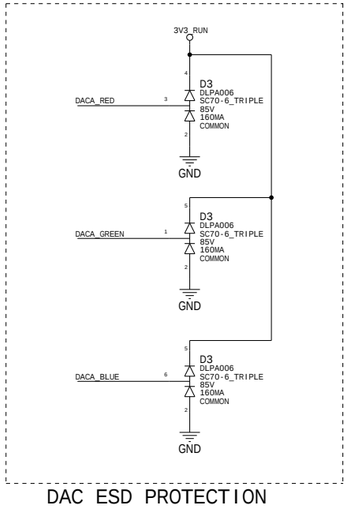
Place close to GPU

DAC_B



DAC_C





DAC ESD PROTECTION

ASSEMBLY	
PAGE_DETAIL	DAC A/B

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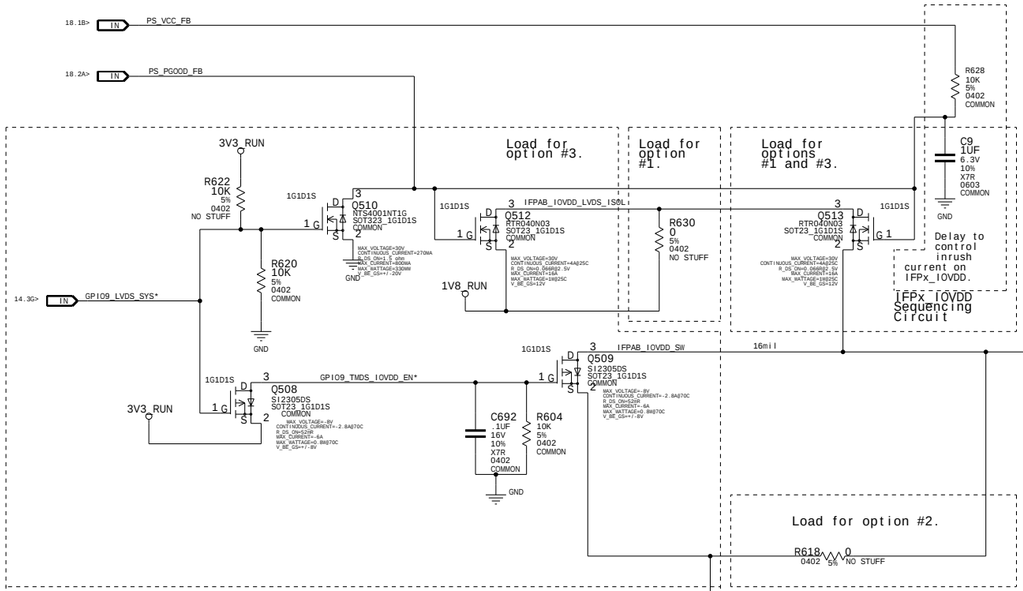
LVDS/TMDS(link A&B)

Loading options for IFPAB outputs

Option #1) IFPAB outputs to LVDS only.
Option #2) IFPAB outputs to DVI-C only.
Option #3) Controlled with GPIO9, IFPAB dynamically outputs to LVDS or DVI-C.



(LVDS CONSTRAINTS)

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
IFPA_TXD0*	IFPATXD0	1	100DIFF
IFPA_TXD0	IFPATXD0	1	100DIFF
IFPA_TXD1*	IFPATXD1	1	100DIFF
IFPA_TXD1	IFPATXD1	1	100DIFF
IFPA_TXD2*	IFPATXD2	1	100DIFF
IFPA_TXD2	IFPATXD2	1	100DIFF
IFPA_TXD3*	IFPATXD3	1	100DIFF
IFPA_TXD3	IFPATXD3	1	100DIFF
IFPB_TXD4*	IFPBTXD4	1	100DIFF
IFPB_TXD4	IFPBTXD4	1	100DIFF
IFPB_TXD5*	IFPBTXD5	1	100DIFF
IFPB_TXD5	IFPBTXD5	1	100DIFF
IFPB_TXD6*	IFPBTXD6	1	100DIFF
IFPB_TXD6	IFPBTXD6	1	100DIFF
IFPB_TXD7*	IFPBTXD7	1	100DIFF
IFPB_TXD7	IFPBTXD7	1	100DIFF
IFPA_TXC*	IFPATXC	1	100DIFF
IFPA_TXC	IFPATXC	1	100DIFF
IFPB_TXC*	IFPBTXC	1	100DIFF
IFPB_TXC	IFPBTXC	1	100DIFF

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	LVDS/TMDS OPTION (LINK A/B)

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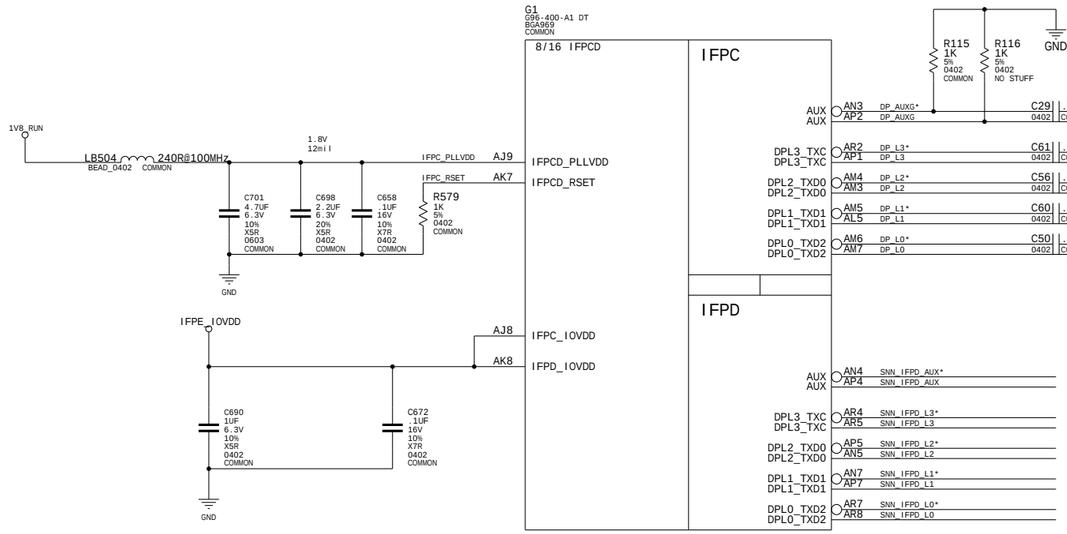
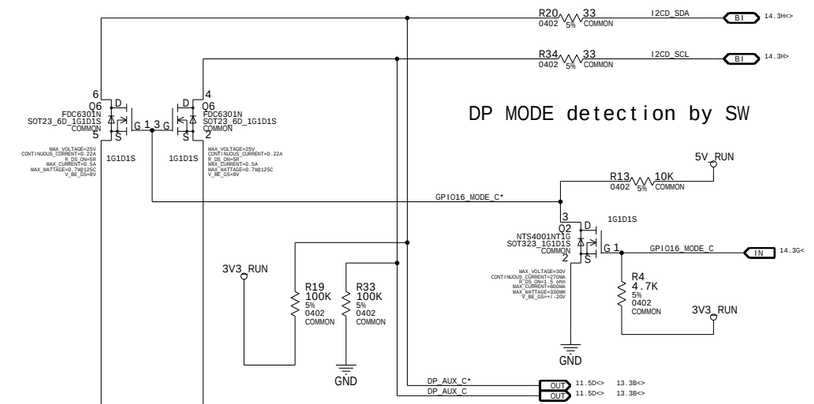
DP(link C)





(DP CONSTRAINTS)

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
DP_AUX*	DP_AUX	1	100DIFF
DP_AUX	DP_AUX	1	100DIFF
DP_AUXG_R*	DP_AUX1	1	100DIFF
DP_AUXG_R	DP_AUX1	1	100DIFF
DP_L3*	DP_L3	1	100DIFF
DP_L3	DP_L3	1	100DIFF
DP_L2*	DP_L2	1	100DIFF
DP_L2	DP_L2	1	100DIFF
DP_L1*	DP_L1	1	100DIFF
DP_L1	DP_L1	1	100DIFF
DP_L0*	DP_L0	1	100DIFF
DP_L0	DP_L0	1	100DIFF

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
DP_AUX_C*	DP_AUX_C	1	100DIFF
DP_AUX_C	DP_AUX_C	1	100DIFF
DP_L3_C*	DPL3C	1	100DIFF
DP_L3_C	DPL3C	1	100DIFF
DP_L2_C*	DPL2C	1	100DIFF
DP_L2_C	DPL2C	1	100DIFF
DP_L1_C*	DPL1C	1	100DIFF
DP_L1_C	DPL1C	1	100DIFF
DP_L0_C*	DPL0C	1	100DIFF
DP_L0_C	DPL0C	1	100DIFF

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DISPLAY PORT (LINK C)

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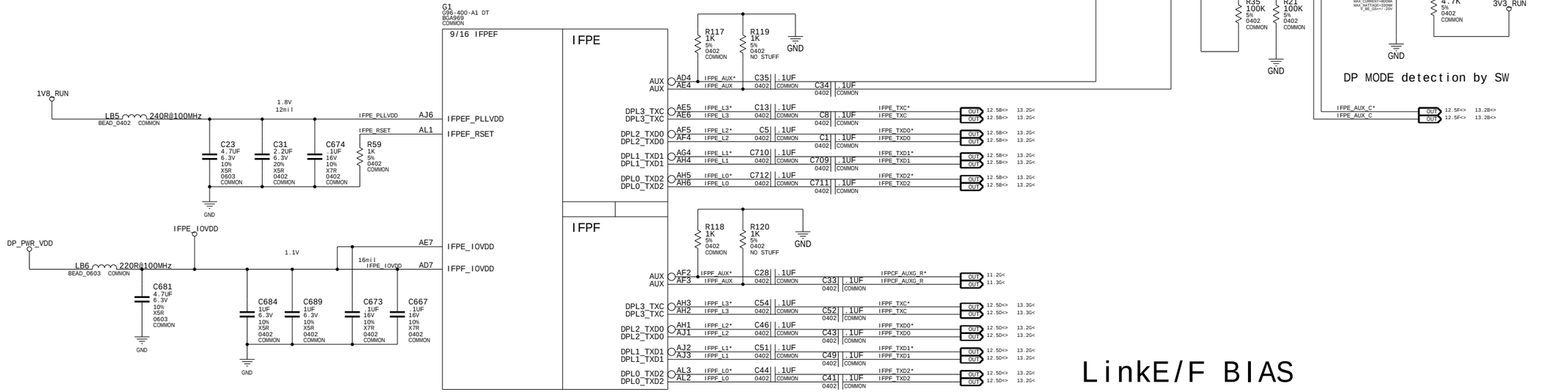
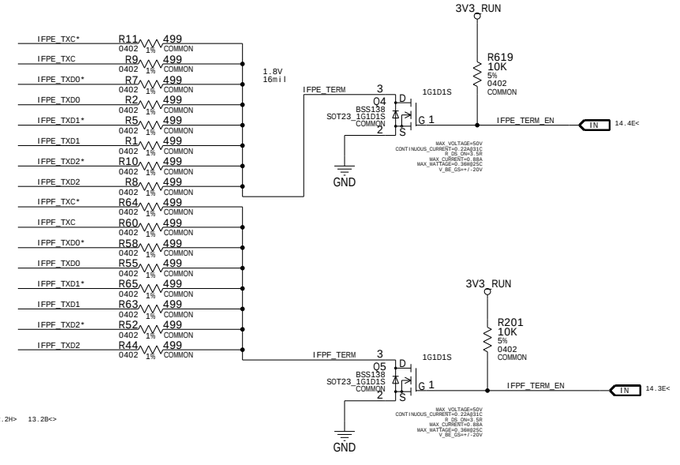
HDMI/DP OPTION (LINK E)



TMDS (LINK F)



LinkE/F BIAS

(TMDS/HDMI/DP OPTION CONSTRAINTS)

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
IFPE_L3*	IFPE_L3	1	100DIFF
IFPE_L3	IFPE_L3	1	100DIFF
IFPE_L2*	IFPE_L2	1	100DIFF
IFPE_L2	IFPE_L2	1	100DIFF
IFPE_L1*	IFPE_L1	1	100DIFF
IFPE_L1	IFPE_L1	1	100DIFF
IFPE_L0*	IFPE_L0	1	100DIFF
IFPE_L0	IFPE_L0	1	100DIFF
IFPE_TXC*	IFPETXC	1	100DIFF
IFPE_TXC	IFPETXC	1	100DIFF
IFPE_TXD0*	IFPETXD0	1	100DIFF
IFPE_TXD0	IFPETXD0	1	100DIFF
IFPE_TXD1*	IFPETXD1	1	100DIFF
IFPE_TXD1	IFPETXD1	1	100DIFF
IFPE_TXD2*	IFPETXD2	1	100DIFF
IFPE_TXD2	IFPETXD2	1	100DIFF

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
IFPF_L3*	IFPF_L3	1	100DIFF
IFPF_L3	IFPF_L3	1	100DIFF
IFPF_L2*	IFPF_L2	1	100DIFF
IFPF_L2	IFPF_L2	1	100DIFF
IFPF_L1*	IFPF_L1	1	100DIFF
IFPF_L1	IFPF_L1	1	100DIFF
IFPF_L0*	IFPF_L0	1	100DIFF
IFPF_L0	IFPF_L0	1	100DIFF
IFPF_TXC*	IFPFTXC	1	100DIFF
IFPF_TXC	IFPFTXC	1	100DIFF
IFPF_TXD0*	IFPFTXD0	1	100DIFF
IFPF_TXD0	IFPFTXD0	1	100DIFF
IFPF_TXD1*	IFPFTXD1	1	100DIFF
IFPF_TXD1	IFPFTXD1	1	100DIFF
IFPF_TXD2*	IFPFTXD2	1	100DIFF
IFPF_TXD2	IFPFTXD2	1	100DIFF

NET NAME	DIFFPAIR	NV_CRITICAL_NET	NV_IMPEDANCE
IFPE_AUX*	IFPE_AUX	1	100DIFF
IFPE_AUX	IFPE_AUX	1	100DIFF
IFPE_AUXG_R*	IFPE_AUXG_R	1	100DIFF
IFPE_AUXG_R	IFPE_AUXG_R	1	100DIFF
IFPE_AUX_C*	IFPE_AUX_C	1	100DIFF
IFPE_AUX_C	IFPE_AUX_C	1	100DIFF
IFPF_AUX*	IFPF_AUX	1	100DIFF
IFPF_AUX	IFPF_AUX	1	100DIFF

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	HDMI/DP OPTION (LINK E), TMDS (LINK F)

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MXM CONNECTOR

CN1
CON_MXM_HE_EDGE
(NON)PHY(-X16,-HE)
NONPHY-HE
COMMON

2/2 IO - LVDS,DVI,DP,VGA,TV

14.3H<	OUT	DVIA_HPD	217	DVI_A_HPD	
12.5F<> 12.2H>	BI	IFPE_AUX_C	232	DDCB_SCLK	
12.5F<> 12.2H>	BI	IFPE_AUX_C*	230	DDCB_SDATA	
14.4H<	OUT	DVIBC_HPD	193	DVI_B_C_HPD	
		SNN_TV_Y	140	TV_Y	HDTV_Y
		SNN_TV_C	136	TV_C	HDTV_Pr
		SNN_TV_CVBS	144	TV_CVBS	HDTV_Pb
9.1G>	IN	DACA_VSYNC	153	VSYNC	
9.1G>	IN	DACA_HSYNC	151	HSYNC	
9.1G>	IN	DACA_RED	148	VGA_RED	
9.1G>	IN	DACA_GREEN	152	VGA_GRN	
9.1G>	IN	DACA_BLUE	156	VGA_BLU	
9.1G>	IN	I2CA_SCL_R	155	DDCA_SCLK	
9.1G<>	BI	I2CA_SDA_R	157	DDCA_SDATA	
14.3H<	OUT	GPIO1_DP_HPD	200	DP_HPD	
11.5D<> 11.2H>	BI	DP_AUX_C*	171	DP_AUX	
11.5D<> 11.2H>	BI	DP_AUX_C	173	DP_AUX	
14.3G>	IN	GPIO3_PPEN	224	LVDS_PPEN	
14.3G>	IN	GPIO4_BLEN	228	LVDS_BLEN	
14.3G>	IN	GPIO2_BL_PWM	226	LVDS_BL_BRGHT	
16.5G< 14.3H> 14.2A<	IN	I2CC_SCL_R	222	DDCC_SCLK	
16.5G> 14.3H> 14.2A<	BI	I2CC_SDA_R	220	DDCC_SDATA	
14.5A<>	BI	SMB_DATA	145	SMB_DAT	
14.5A<	OUT	SMB_CLK	147	SMB_CLK	
14.2G>	IN	THERM_ALERT*	149	THERM	
18.4B< 17.3A< 10.3A<	OUT	MOBILE_RUNPWROK	16	RUNPWROK	
14.3G<	OUT	GPIO12_AC_DET	169	AC/BATT*	
16.2E<	OUT	SPDIF	170	SPDIF	
16.1A<	OUT	HDA_BCLK	143	HDA_BCLK	
16.2A<	OUT	HDA_SYNC	141	HDA_SYNC	
16.2A<	OUT	HDA_SDO	161	HDA_SDO	
16.1A>	IN	HDA_SDI	159	HDA_SDI	
16.1A<	OUT	HDA_RST*	146	HDA_RST	

DVI_A_CLK	219	IFPE_TXC*	12.2F> 12.5B<>
DVI_A_CLK	221	IFPE_TXC	12.2F> 12.5B<>
DVI_A_TX0	237	IFPE_TXD0*	12.2F> 12.5B<>
DVI_A_TX0	239	IFPE_TXD0	12.2F> 12.5B<>
DVI_A_TX1	231	IFPE_TXD1*	12.2F> 12.5B<>
DVI_A_TX1	233	IFPE_TXD1	12.2F> 12.5B<>
DVI_A_TX2	225	IFPE_TXD2*	12.3F> 12.5B<>
DVI_A_TX2	227	IFPE_TXD2	12.3F> 12.5B<>

DP_A / DVI-B

DP_A_L0	DVI_B_TX2	201	IFPF_TXD2* 12.3F> 12.5D<>
DP_A_L0	DVI_B_TX2	203	IFPF_TXD2 12.3F> 12.5D<>
DP_A_L1	DVI_B_TX1	207	IFPF_TXD1* 12.3F> 12.5D<>
DP_A_L1	DVI_B_TX1	209	IFPF_TXD1 12.3F> 12.5D<>
DP_A_L2	DVI_B_TX0	213	IFPF_TXD0* 12.3F> 12.5D<>
DP_A_L2	DVI_B_TX0	215	IFPF_TXD0 12.3F> 12.5D<>
DP_A_L3	DVI_B_CLK	189	IFPF_TXC* 12.3F> 12.5D<>
DP_A_L3	DVI_B_CLK	191	IFPF_TXC 12.3F> 12.5D<>
DP_B_L0		195	DP_L0_C* 11.3G> 11.5D<>
DP_B_L0		197	DP_L0_C 11.3G> 11.5D<>
DP_B_L1		183	DP_L1_C* 11.3G> 11.5D<>
DP_B_L1		185	DP_L1_C 11.3G> 11.5D<>
DP_B_L2		177	DP_L2_C* 11.3G> 11.5D<>
DP_B_L2		179	DP_L2_C 11.3G> 11.5D<>
DP_B_L3		165	DP_L3_C* 11.3G> 11.5D<>
DP_B_L3		167	DP_L3_C 11.3G> 11.5D<>
LVDS_UTX0		186	IFPB_TXD4 10.2H> 10.5B<>
LVDS_UTX0		184	IFPB_TXD4* 10.2H> 10.5B<>
LVDS_UTX1		180	IFPB_TXD5 10.2H> 10.5B<>
LVDS_UTX1		178	IFPB_TXD5* 10.2H> 10.5B<>
LVDS_UTX2		174	IFPB_TXD6 10.2H> 10.5B<>
LVDS_UTX2		172	IFPB_TXD6* 10.2H> 10.5B<>
LVDS_UTX3		168	IFPB_TXD7 10.3H> 10.5B<>
LVDS_UTX3		166	IFPB_TXD7* 10.2H> 10.5B<>
LVDS_UCLK		162	IFPB_TXC 10.2H> 10.5B<>
LVDS_UCLK		160	IFPB_TXC* 10.2H> 10.5B<>
LVDS_LTX0		216	IFPA_TXD0 10.1H> 10.4B<>
LVDS_LTX0		214	IFPA_TXD0* 10.1H> 10.4B<>
LVDS_LTX1		210	IFPA_TXD1 10.2H> 10.4B<>
LVDS_LTX1		208	IFPA_TXD1* 10.2H> 10.4B<>
LVDS_LTX2		204	IFPA_TXD2 10.2H> 10.5B<>
LVDS_LTX2		202	IFPA_TXD2* 10.2H> 10.5B<>
LVDS_LTX3		198	IFPA_TXD3 10.2H> 10.5B<>
LVDS_LTX3		196	IFPA_TXD3* 10.2H> 10.5B<>
LVDS_LCLK		192	IFPA_TXC 10.1H> 10.5B<>
LVDS_LCLK		190	IFPA_TXC* 10.1H> 10.5B<>

3V3_RUN

D501 BAT54C 30V 200MA SOT23 COMMON

D9 BAT54C 30V 200MA SOT23 COMMON

R91 1K 0402 5% COMMON

C70 470PF 50V 10% X7R 0402 COMMON

C55 .01UF 0402 16V 10% X7R COMMON

NV_IMPEDANCE=56OHM
NV_CRITICAL_NET=2
SPDIF_MXM

GND

3V3_RUN

D8 DLPA006 160MA 85V SC70-6_TRIPLE COMMON — I2CA_SDA_R
D8 DLPA006 160MA 85V SC70-6_TRIPLE COMMON — DP_AUX_C*
D10 DLPA006 160MA 85V SC70-6_TRIPLE COMMON — IFPE_AUX_C*
D8 DLPA006 160MA 85V SC70-6_TRIPLE COMMON — DP_AUX_C
D10 DLPA006 160MA 85V SC70-6_TRIPLE COMMON — I2CA_SCL_R
D10 DLPA006 160MA 85V SC70-6_TRIPLE COMMON — IFPE_AUX_C

GND

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MXM CONNECTOR

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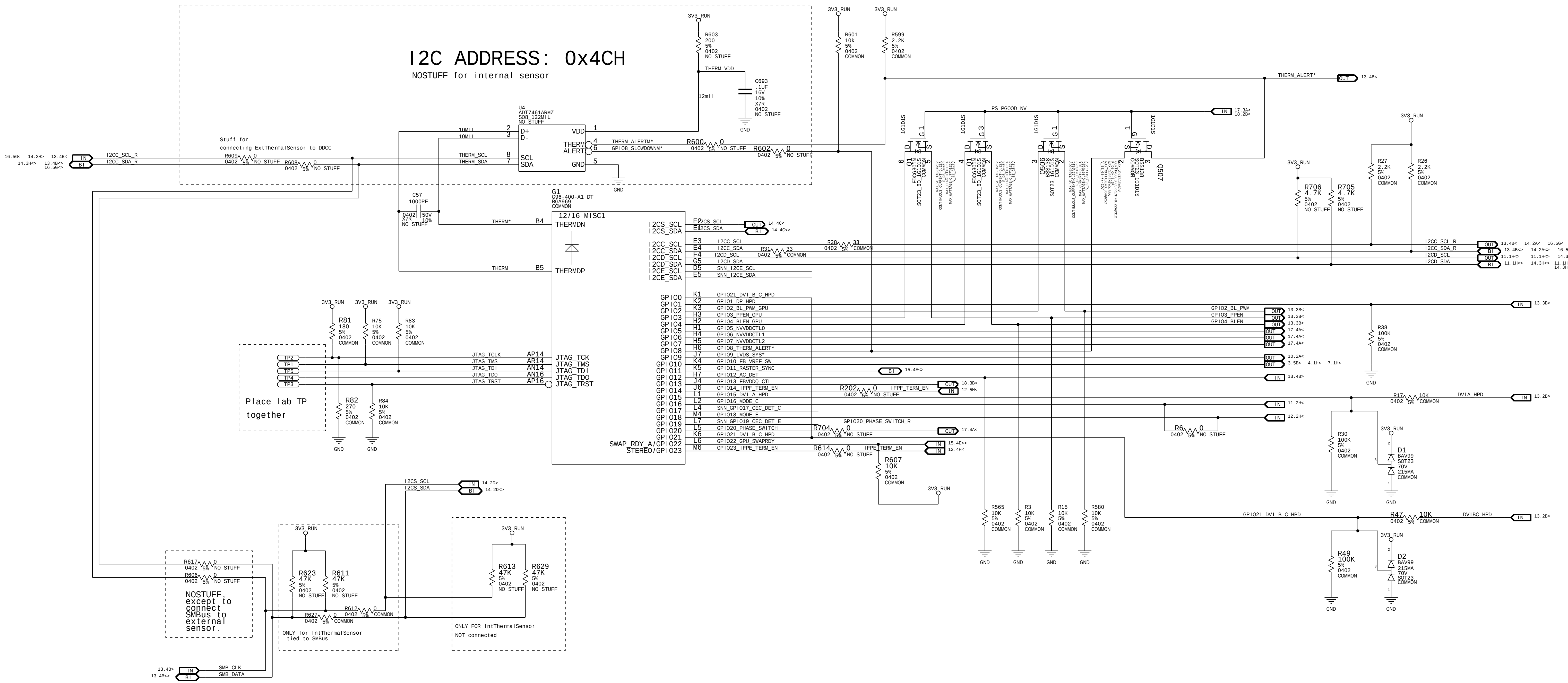
GPIO, TEMP SENSOR, JTAG



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPIO, JTAG, TEMP SENSOR

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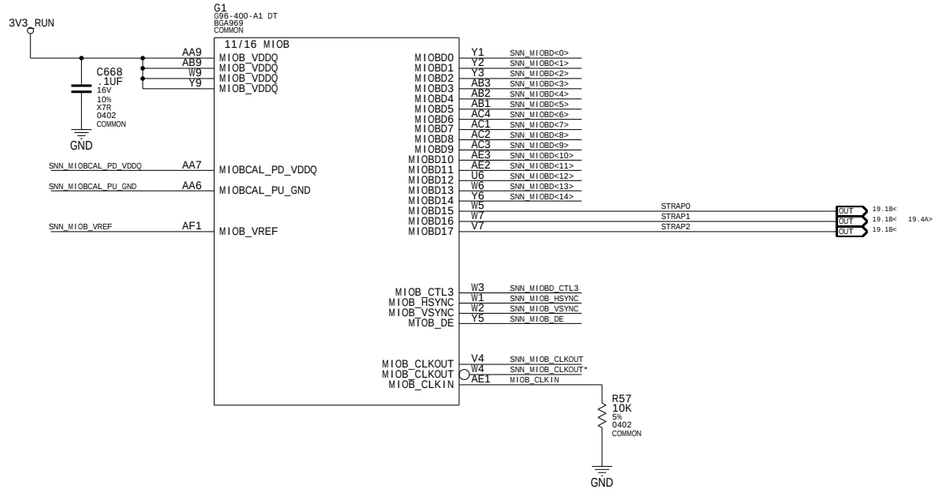
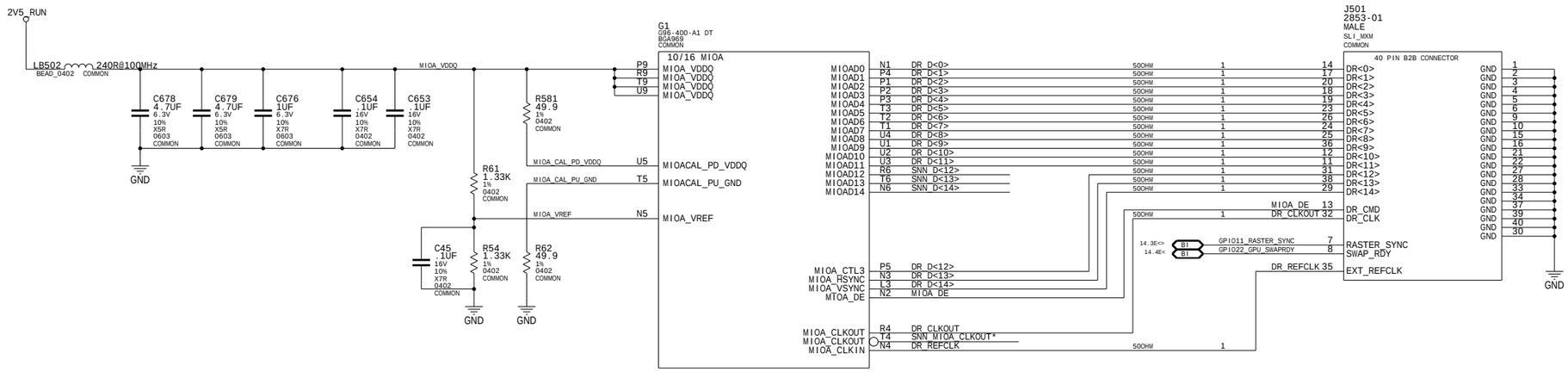
MIOA/B

NETNAME	MIN_LINE_WIDTH	
B1 MIOB_VDDQ	12MIL	3.3V

(MIOB CONSTRAINTS)





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MIO A/B, STRAPPING OPTIONS

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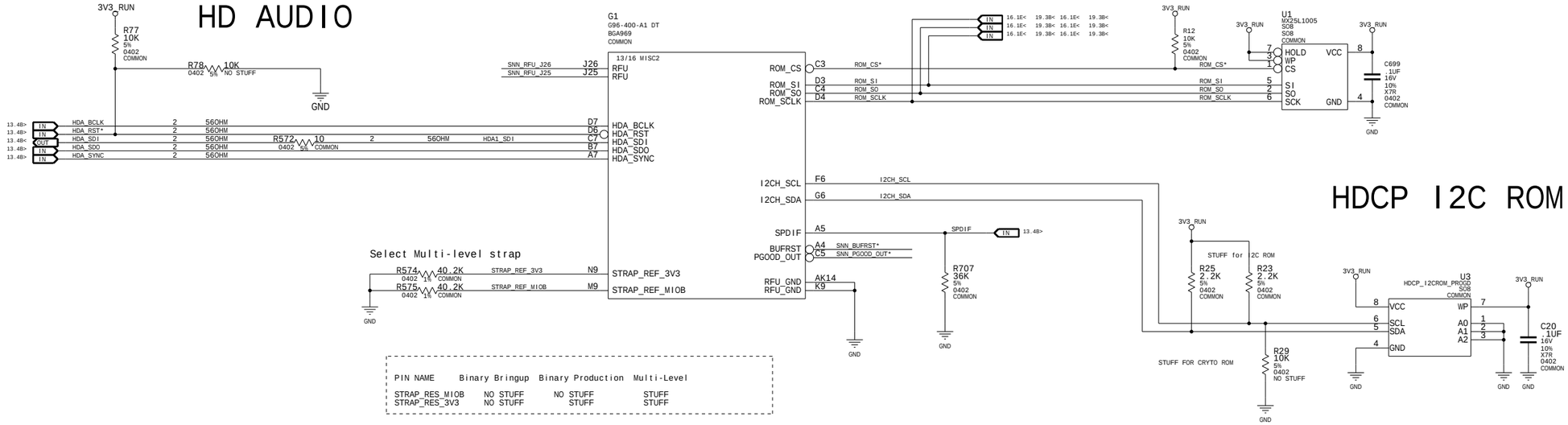
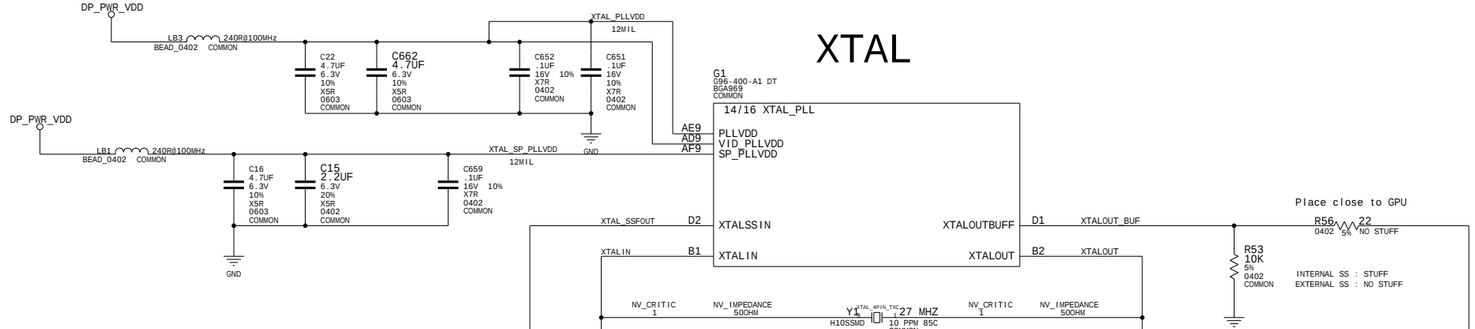
HD AUDIO



VBIOS ROM

HDCP I2C ROM

XTAL



SPREAD

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	VBIOS, HDCP/I2C ROM, XTAL, SPREAD SPECTRUM, HD AUDIO

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NVVDD POWER SUPPLY

NET	VOLTAGE	CURRENT	LINE_WIDTH
NVVDD	1.00V	30A	20MIL
PS_PHASE1_NV		15A	16MIL
PS_PHASE2_NV		15A	16MIL
PS_UGATE1_NV			20MIL
PS_BOOT1_NV			20MIL
PS_LGATE1_NV			20MIL
PS_CSP1			16MIL
PS_CSN1			16MIL
PS_UGATE2_NV			20MIL
PS_BOOT2_NV			20MIL
PS_LGATE2_NV			20MIL
PS_CSP2			16MIL
PS_CSN2			16MIL
PS_DROOP_NV			16MIL
PS_VDD_CREF_NV			16MIL
PS_VDD_DROOP_NV			16MIL
PS_VDD_ISLEW_NV			20MIL
PS_VDD_V5FILT			20MIL

Iout_peak_to_peak = 37.4 A
(Iout_max=30A; Vin=7.5V; Vout=1.0V; F=300KHz)

Iout_peak_to_peak = 39.2A
(Iout_max=30A; Vin=22V; Vout=1.0V; F=300KHz)

Iin_rms = 7.4A
(Iout_max=30A; Vin=7.5V; Vout=1.0V)

Iin_rms = 9.2A
(Iout_max=30A; Vin=22V; Vout=1.0V)

NO STUFF Q503 AND R527	
VID<3..0>	NVVDD
0 0 0 0	1.250
0 0 0 1	1.225
0 0 1 0	1.200
0 0 1 1	1.175
0 1 0 0	1.150
0 1 0 1	1.125
0 1 1 0	1.100
0 1 1 1	1.075
1 0 0 0	1.050
1 0 0 1	1.025
1 0 1 0	1.000
1 0 1 1	0.975
1 1 0 0	0.950
1 1 0 1	0.925
1 1 1 0	0.900
1 1 1 1	0.875

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	NVVDD POWER SUPPLY

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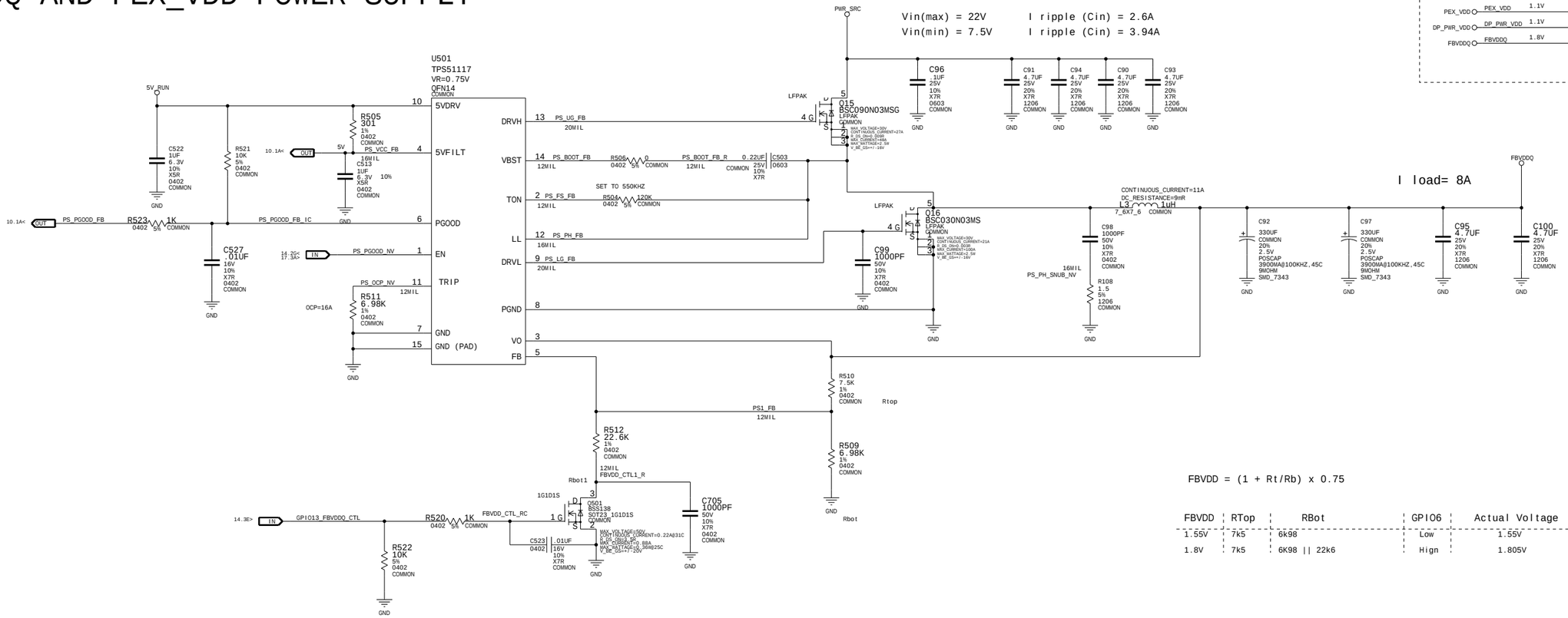
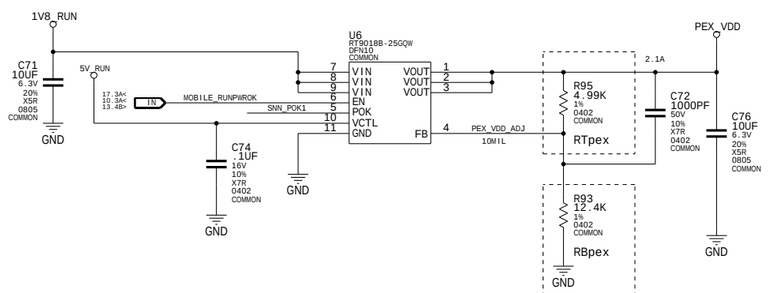
FBVDDQ AND PEX_VDD POWER SUPPLY

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
PEX_VDD	1.1V	12MIL	2.1A
DP_PWR_VDD	1.1V	12MIL	1.2A
FBVDDQ	1.8V	20MIL	8A



FBVDD	RTop	RBot	GPIO6	Actual Voltage
1.55V	7k5	6k98	Low	1.55V
1.8V	7k5	6K98 || 22k6	Hign	1.805V

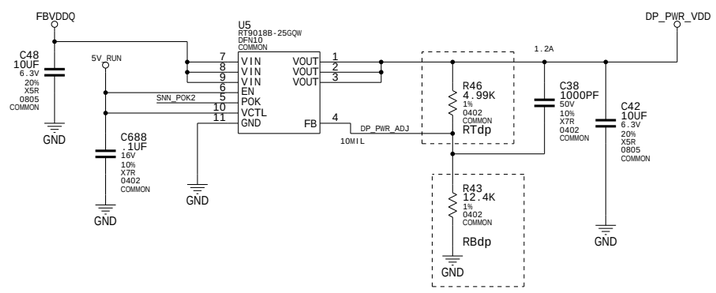
PEXVDD Regulator



1.1=0.8*[1+(4k99/12k4)]

PEXVDD=0.8*[1+(RTpex/RBpex)]

DP_IOVDD Regulator



1.1=0.8*[1+(4k99/12k4)]

DP_IOVDD=0.8*[1+(RTpex/RBpex)]

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	FBVDDQ AND PEXVDD POWER SUPPLY

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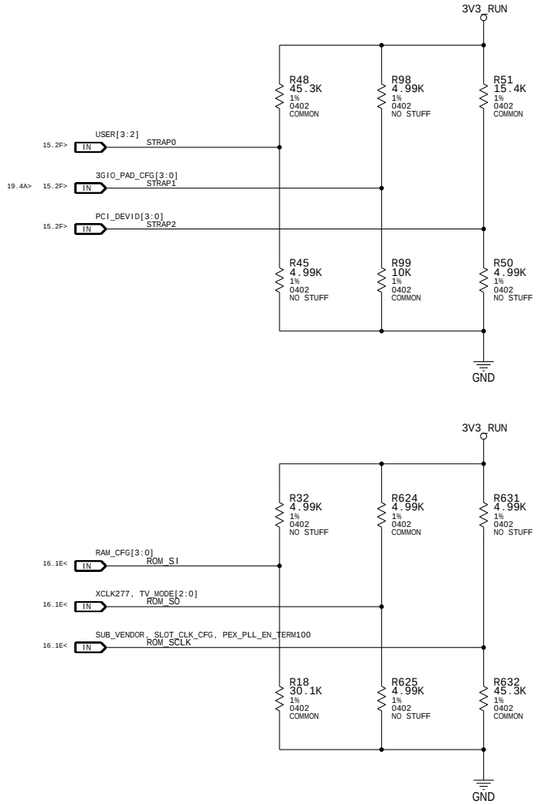
STRAPPING OPTIONS



	3V3	GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

STRAP0

USER_BIT0
USER_BIT1
USER_BIT2
USER_BIT3

0xF: 45K PU (unused)

STRAP1

3GIO_PADCFG_LUT_ADR0
3GIO_PADCFG_LUT_ADR1
3GIO_PADCFG_LUT_ADR2
3GIO_PADCFG_LUT_ADR3

0x0: Desktop default (normal swing) - 5k PD
0x1: Mobile default (low swing) - 10k PD
acc. to //hw/tesla_g98b/manuals/dev_ext_devices.ref

STRAP2

PCI_DEVID_0
PCI_DEVID_1
PCI_DEVID_2
PCI_DEVID_3

all 4 bits set by HW strapping
0x064A: 15K PU (NB9E-GE)

ROM_SO

TV_MODE_BIT0
TV_MODE_BIT1
TV_MODE_BIT2
XCLK_277

0x0: NTSC-M
5K PU
1: PCI-E GEN2

ROM_SI

RAM_CFG_0
RAM_CFG_1
RAM_CFG_2
RAM_CFG_3

256 MB (4pcs. 16Mx32)

RAM_CFG[3:0]	Definitions
0000	Reserved
0001	Qimonda
0010	Hynix
0011	Samsung

512 MB (4pcs. 32Mx32)

RAM_CFG[3:0]	Definitions
0100	25k PD Reserved
0101	30k PD Qimonda
0110	35k PD Hynix
0111	45k PD Samsung

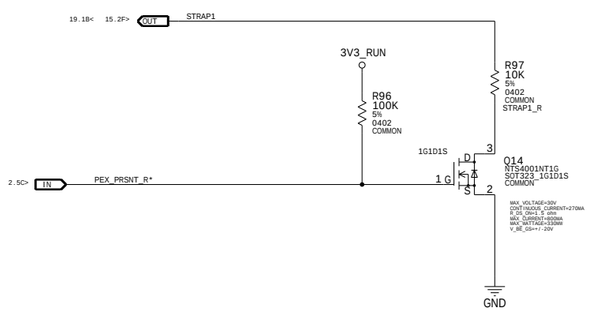
ROM_SCLK

PCI_DEVID_EXT
SUB_VENDOR
SLOT_CLK_CONFIG
PEX_PLL_EN_TERM100

0:
1: SUB_VENDOR BIOS
1:
1: TERM100 ENABLED

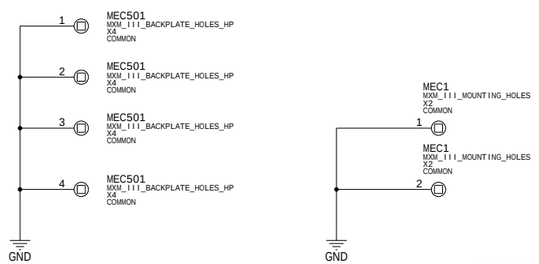
30K PD

PEX SWING LEVEL



PEX_PRSNT2_R	R_STRAP1	3_GIO_PADCFG_LUT<3..0>
GND	10k	0x1 MOBILE_DEFAULT
FLOAT	5k (10k || 10k)	0x0 DESKTOP_DEFAULT

MECHANICAL



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PEX SWING LEVEL, MECHANICAL

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