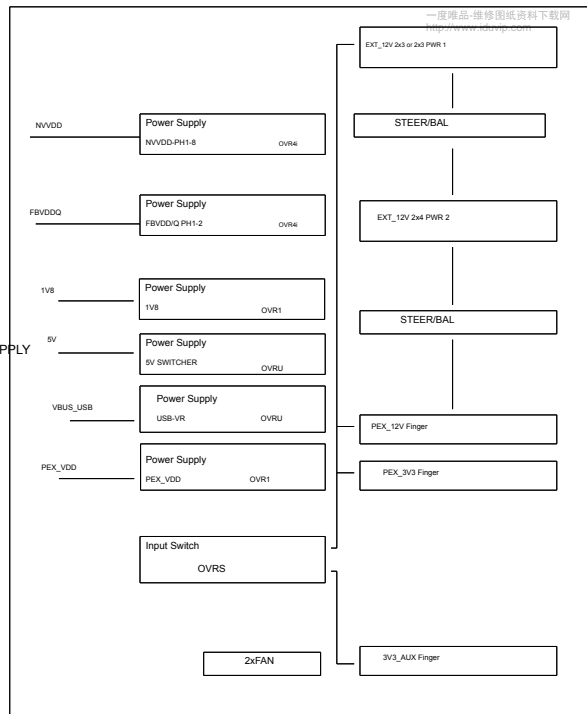


TALL DP + DP + DP + HDMI/DP + USB

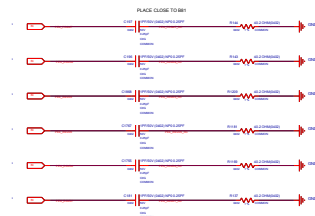
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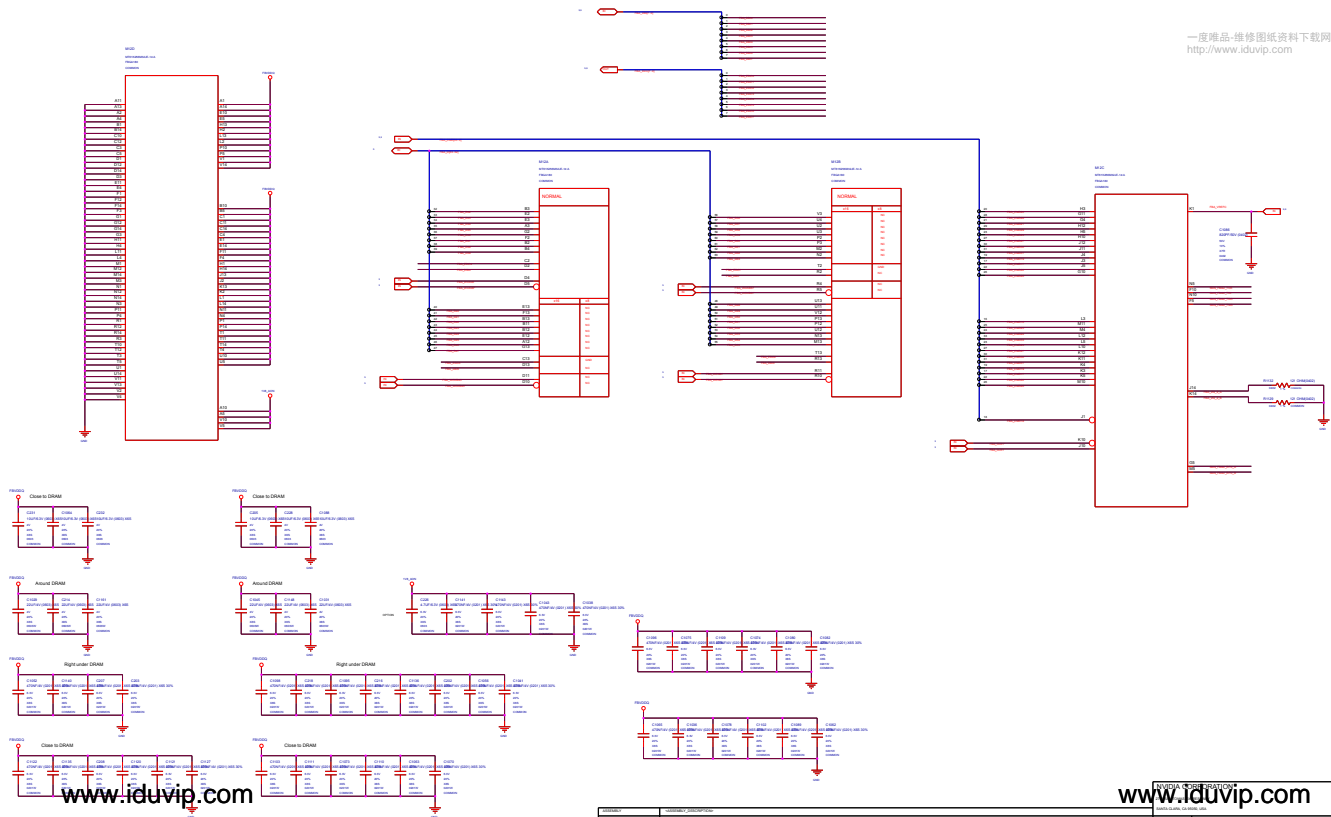
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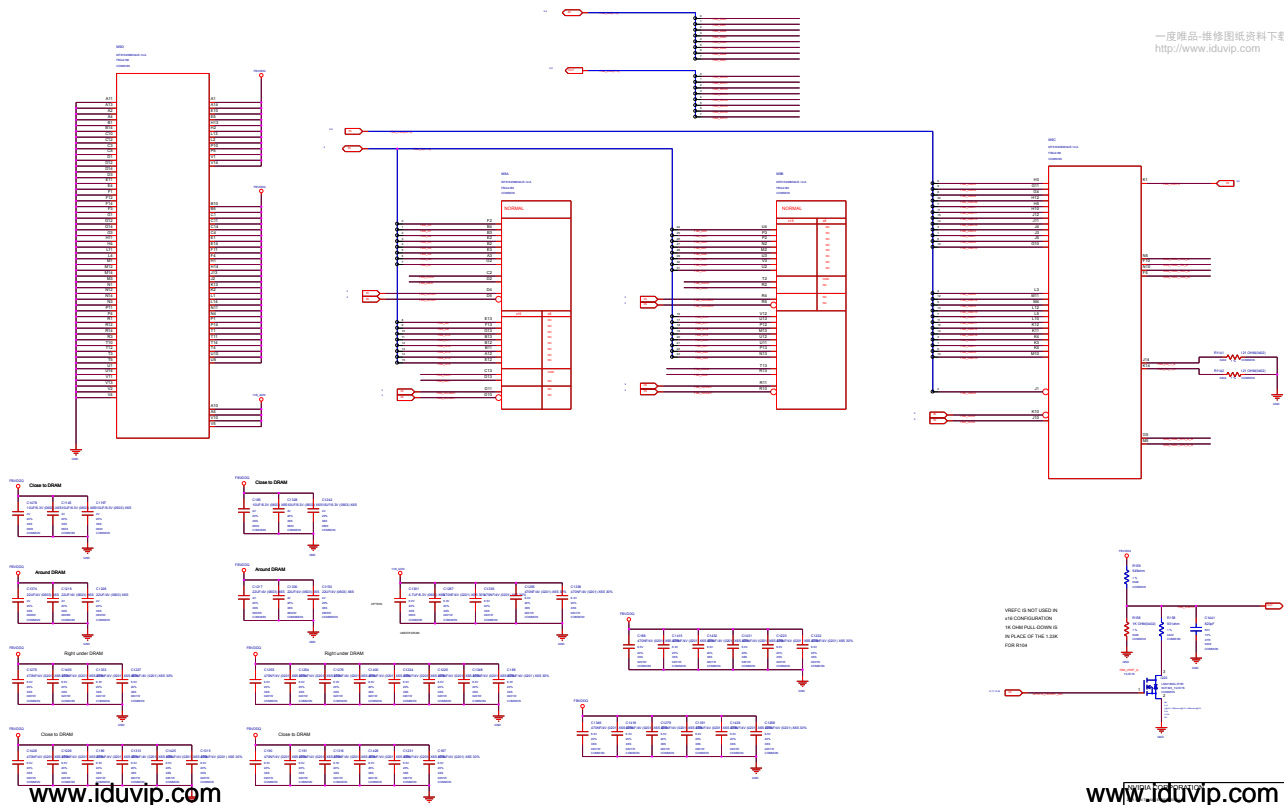


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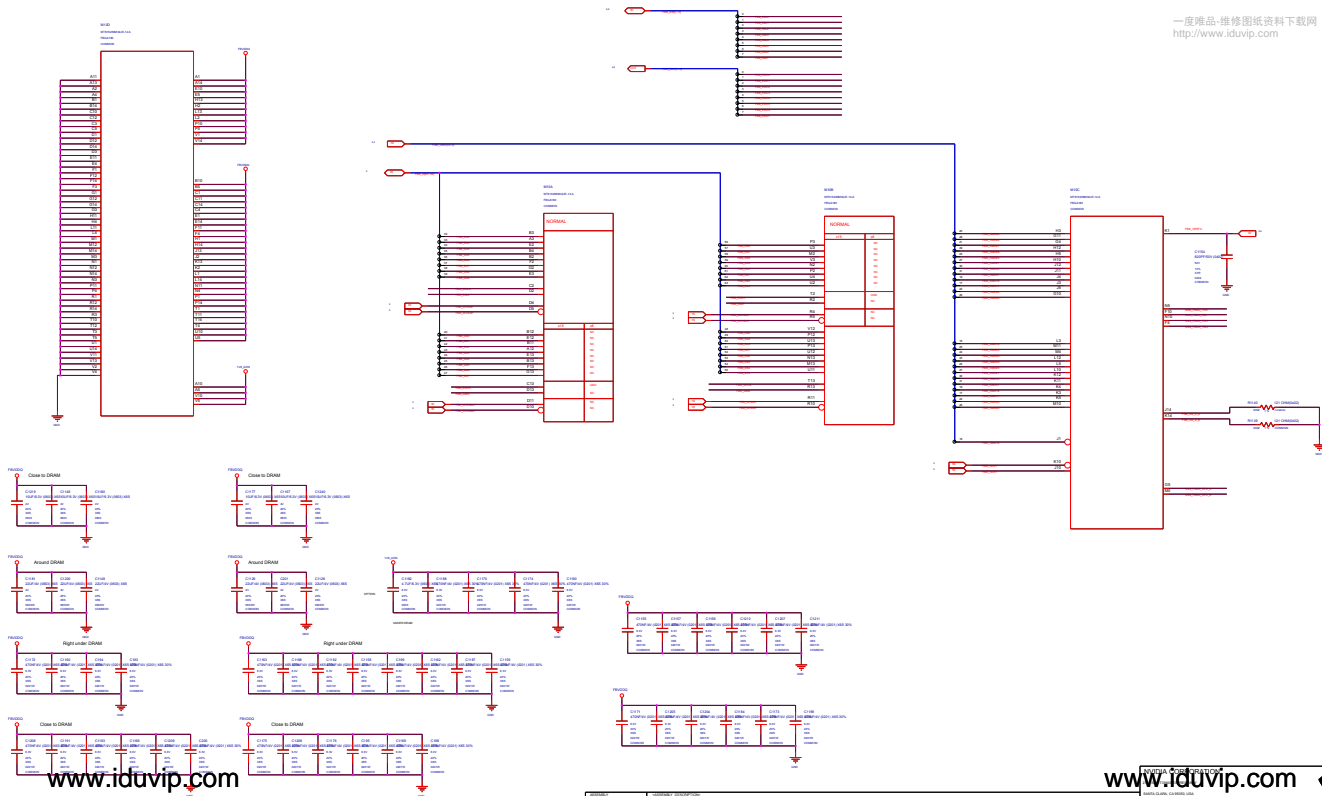
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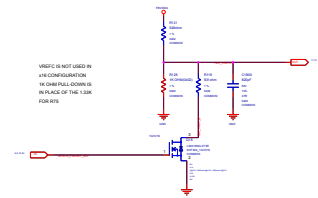
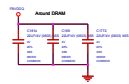
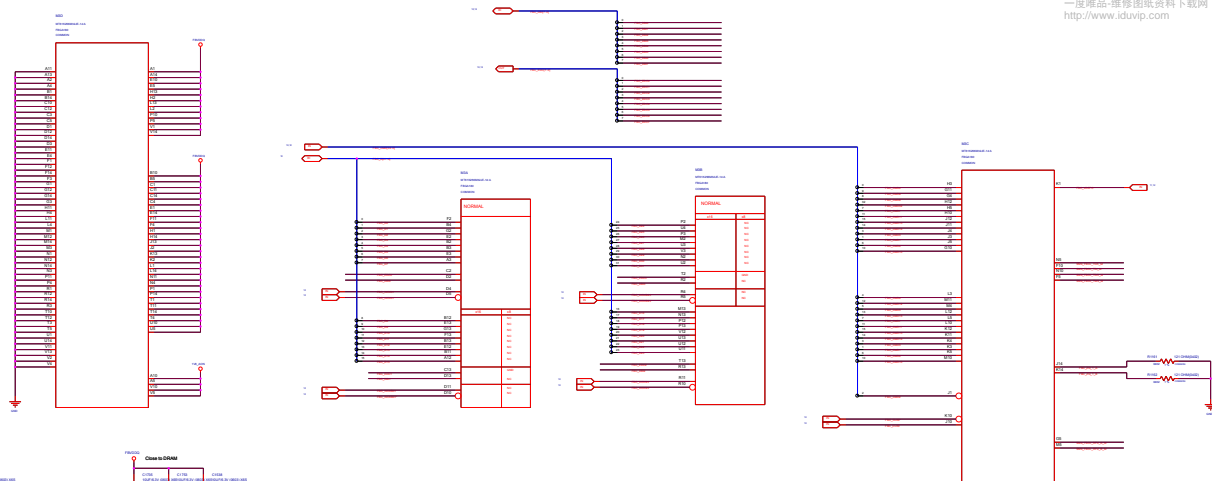


MEMORY	MEMORY PARTITION 63_32
Model 63_32	Model 63_32
Part No.	805-1G180-BASE-200
Rev. 1.0	Rev. 1.0
Part No.	805-1G180-BASE-200

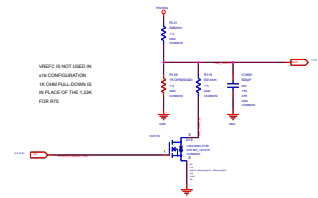
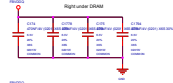
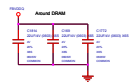
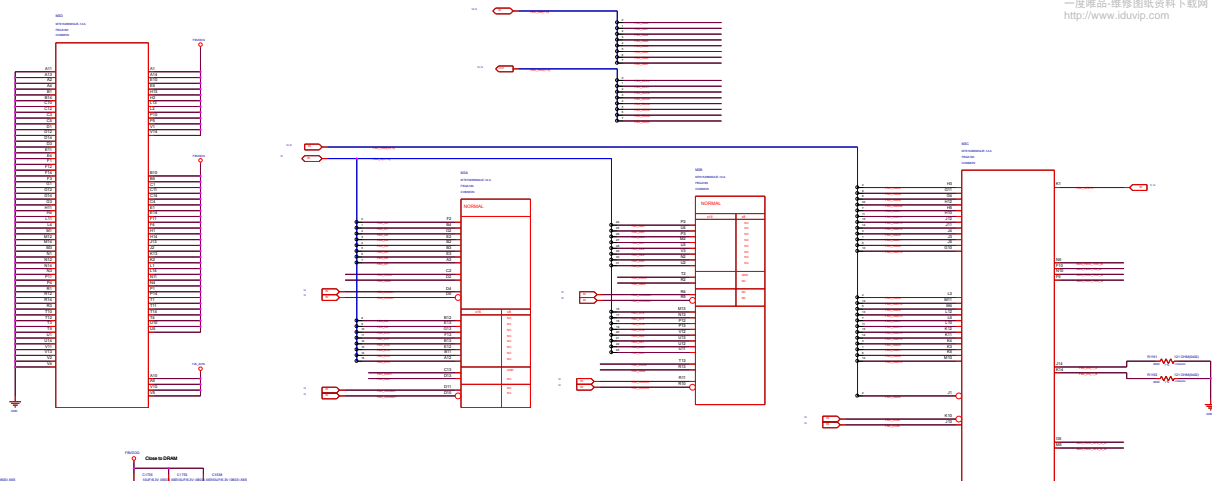


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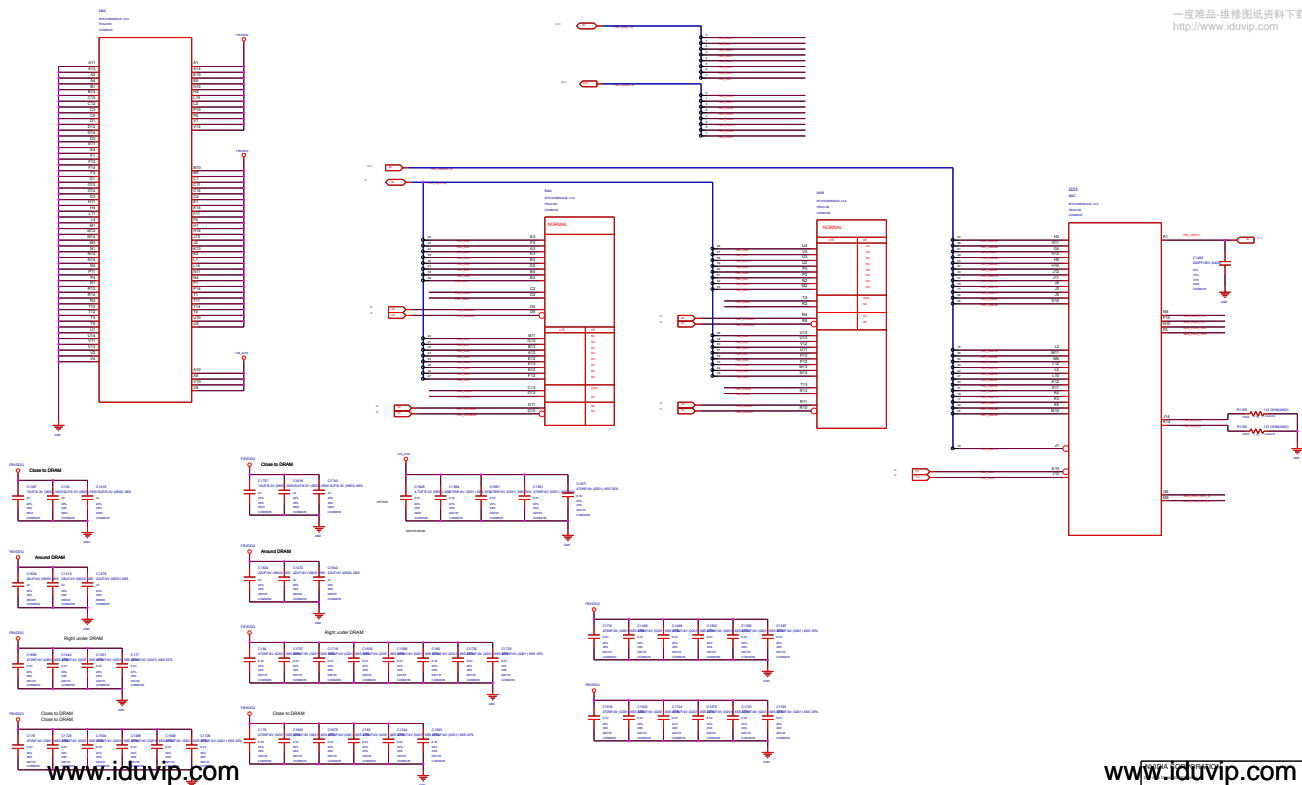


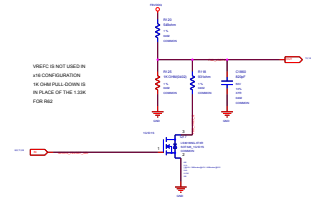
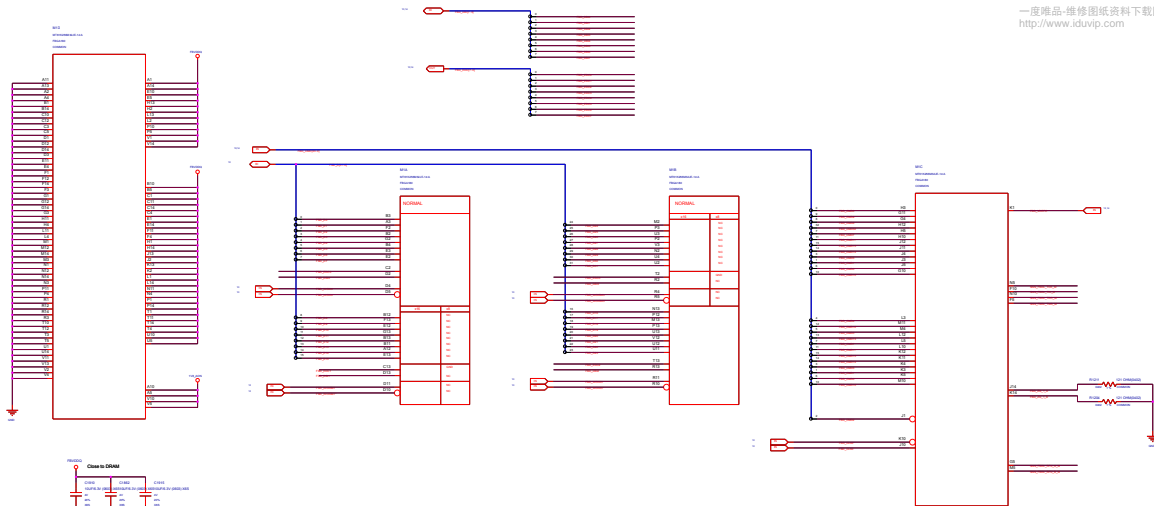


VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.23K
FOR R7H.



VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.23K
FOR R7H.





VREFC IS NOT USED;
x16 CONFIGURATION
1K OHM PULL-DOWN
IN PLACE OF THE 1.2K
FOR R62;



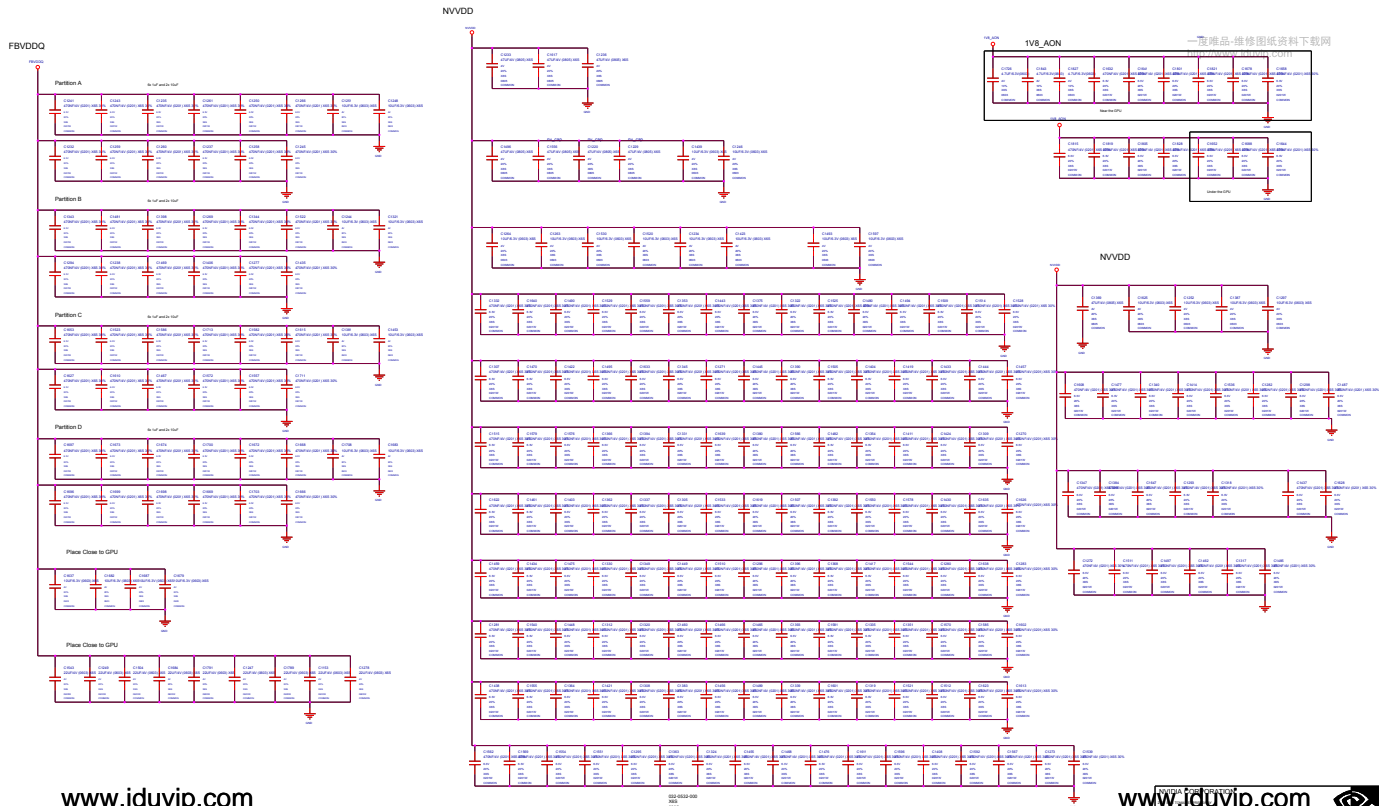




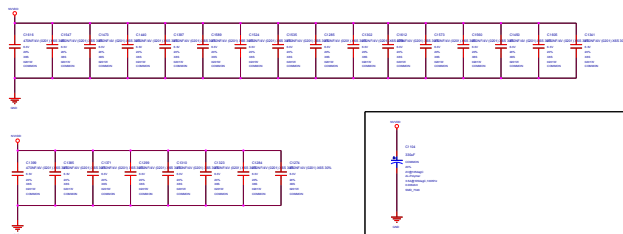
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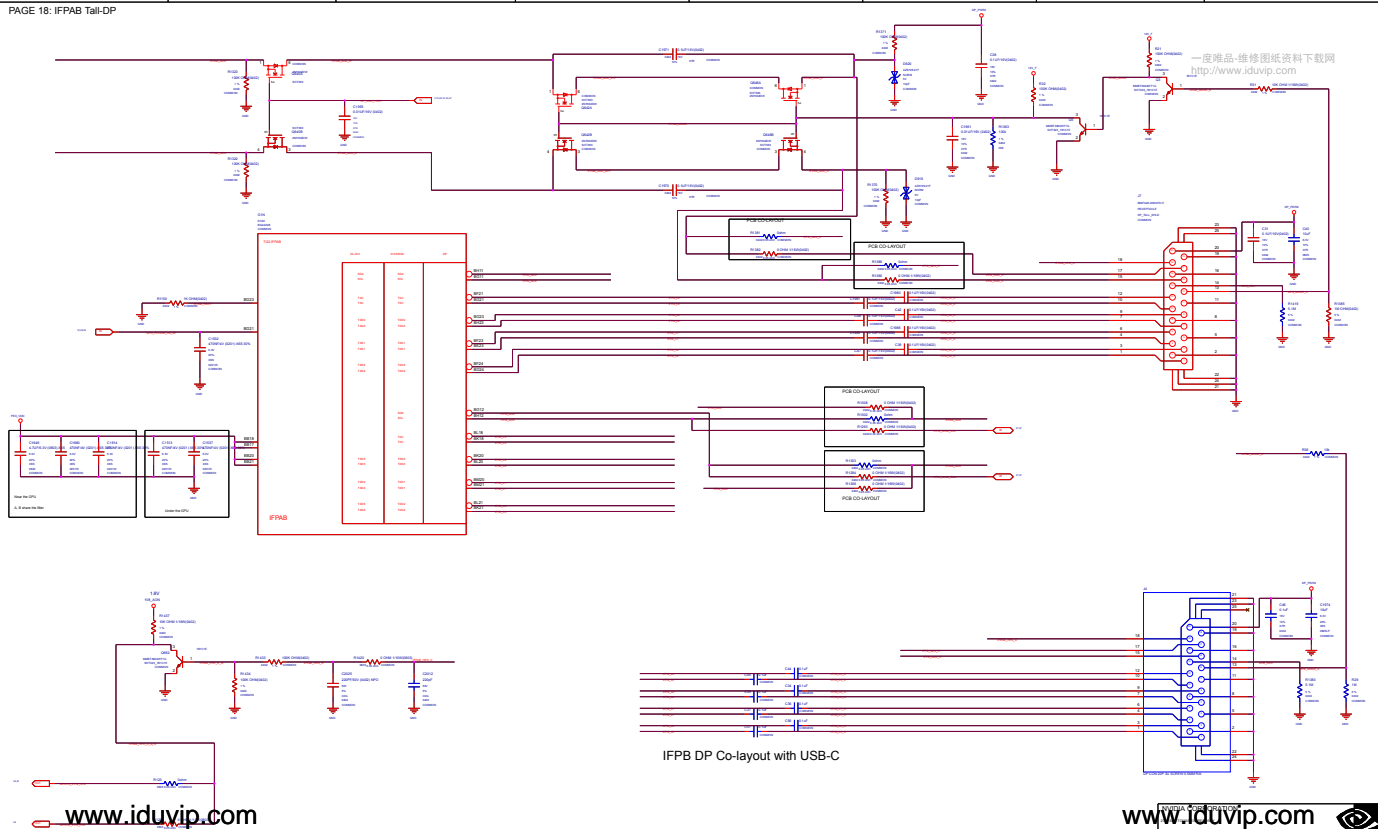


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NVIDIA CORPORATION							
10070 CLARA, CA 95000, USA							
INV_PN	600-1G180-BASE-200						
PCB date	PCB180-802	Part	10 of 24				
Order date	JA	DATE	20F-JUNE-2018				



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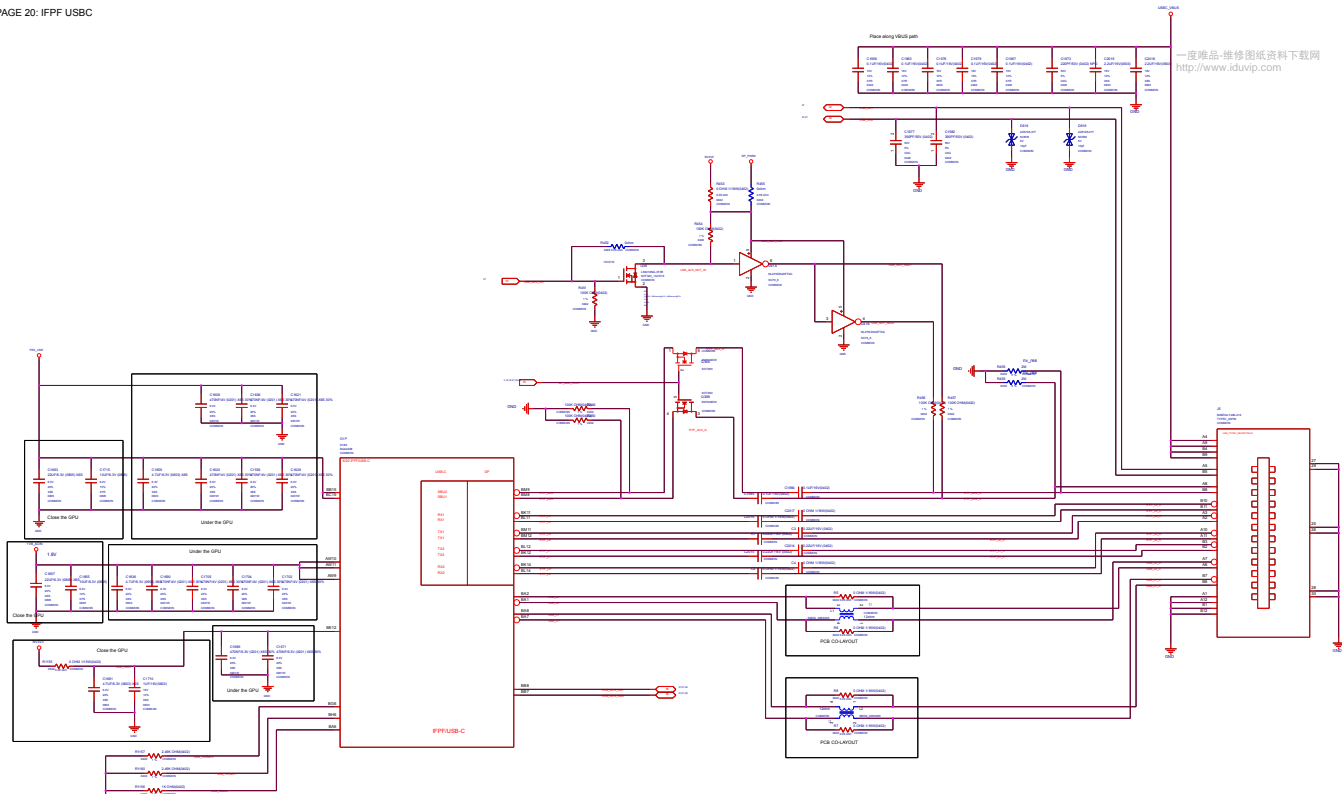


REVISION	REVISION DESCRIPTION
1.0	1.000 1000 1000

NVIDIA CORPORATION			
NVIDIA LOGO			
MODEL	650-10180-BASE 200	REV	1.000 1000 1000
DATE	1.000 1000 1000	REV	1.000 1000 1000
DATE	1.000 1000 1000	REV	1.000 1000 1000

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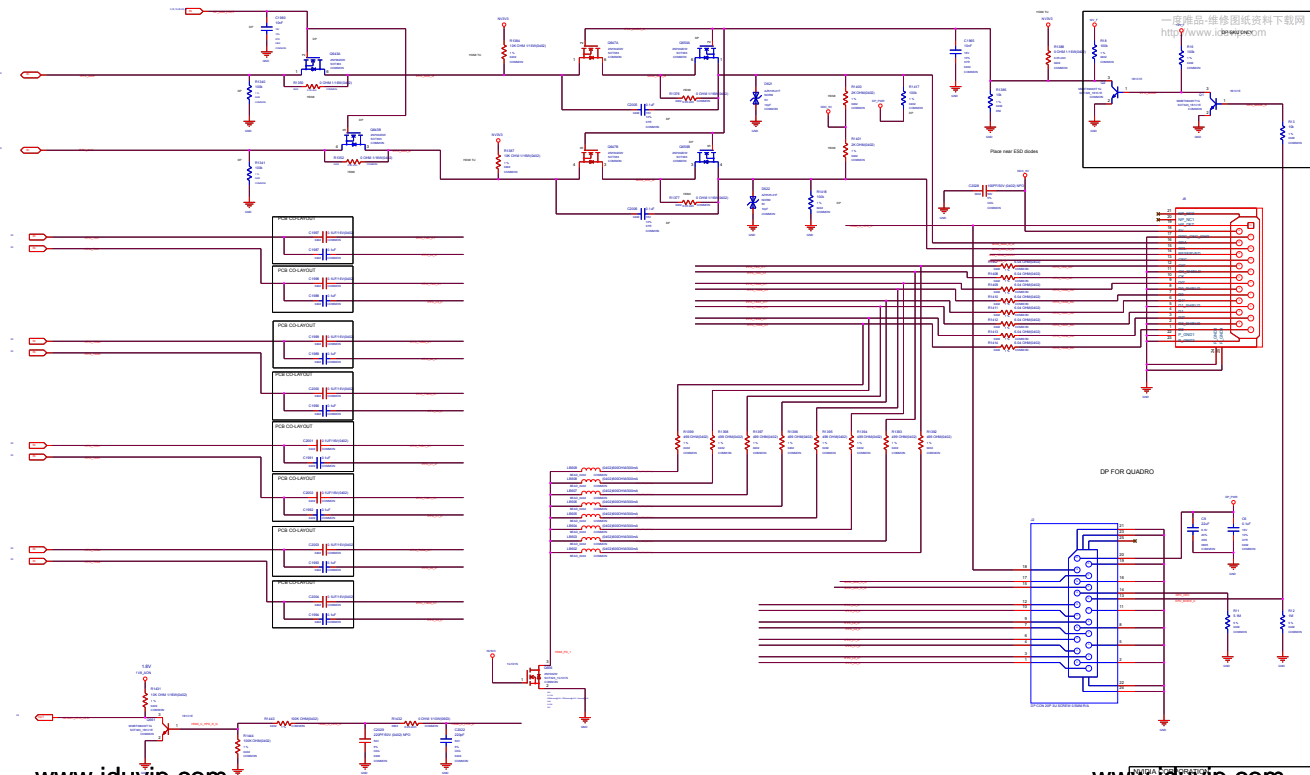
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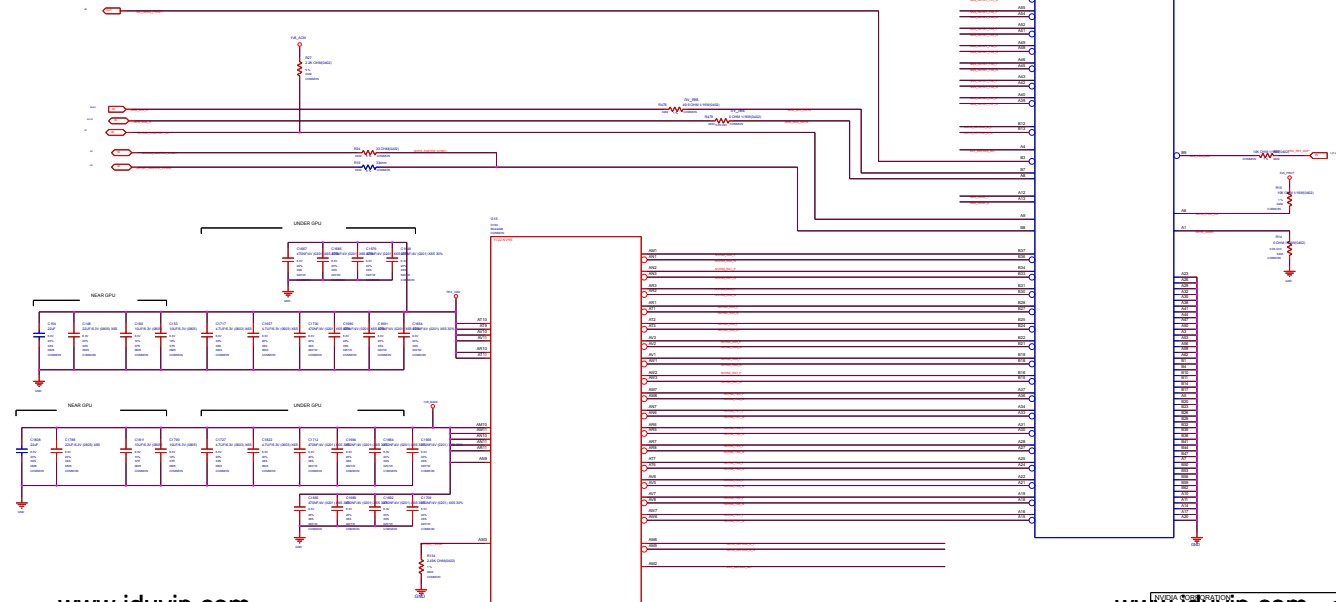
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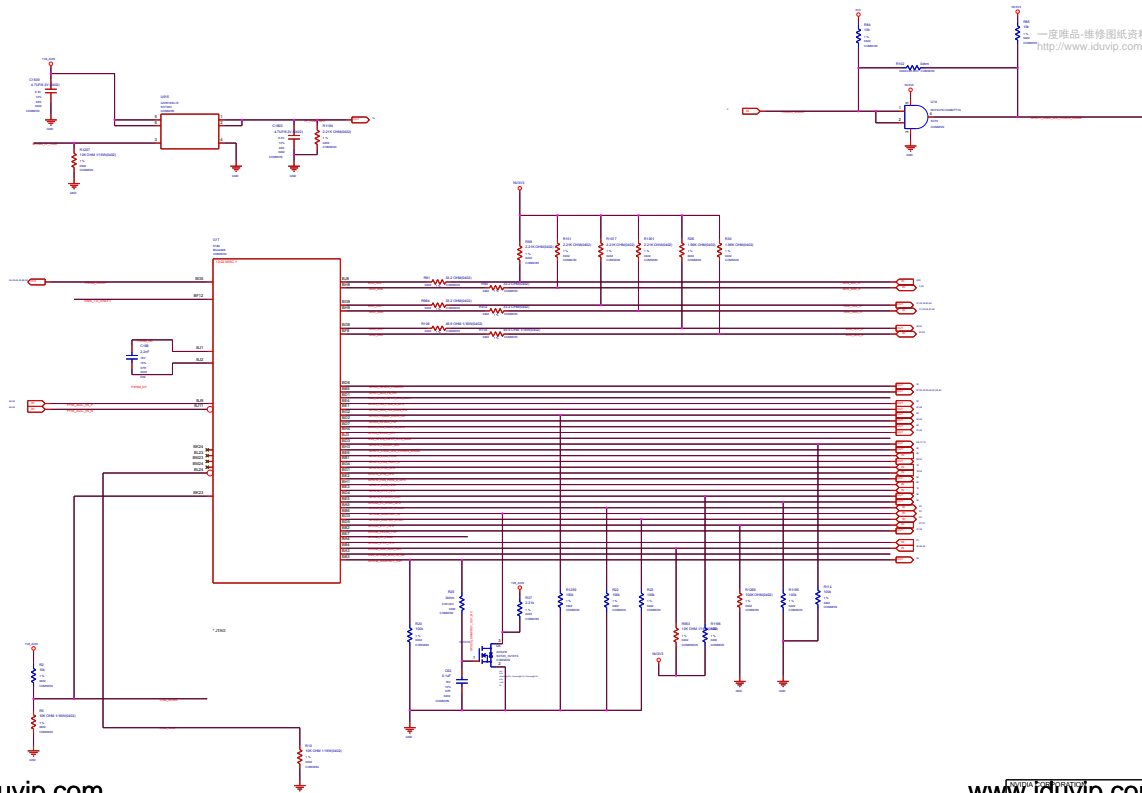
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ASSEMBLY	ASSEMBLY DESCRIPTION	ITEM LOCATION, QUANTITY, ETC.
BASE SERIAL	BASE INTERFERENCE	

REV. P/N	600-1G180-BASE-200		
DESCRIPTION	REVISION	DATE	BY/APP. NO.
600-1G180	A	03/03/2014	

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NY_PN	000-1G180-BASE-200		
FILE NO	PG 180-002	AGE	21 OF 31
ACCOUNT	A	AGE	27-000-000

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H=High -Tied to 1.8V
M=Medium -Tied to 0.9V
L=Low -Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFGH (6)	RAMCFG TSD	DEFAULT
L	L	L	0000	RAMCFG TSD	
L	L	H	0001	RAMCFG TSD	
L	H	L	0010	RAMCFG TSD	
L	H	H	0011	RAMCFG TSD	
H	H	L	0110	RAMCFG TSD	
H	H	H	0111	RAMCFG TSD	

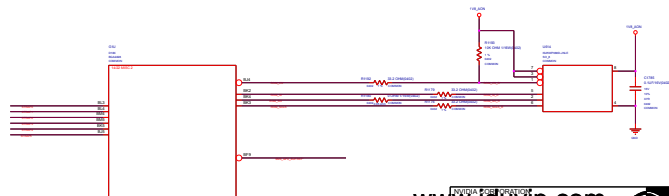
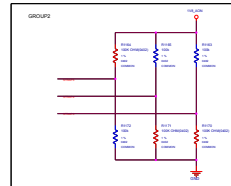
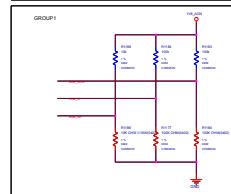
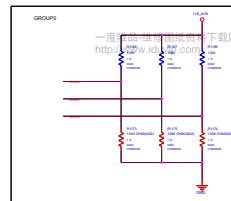
ROM_S0	ROM_S1	ROM_SCLX	DUMPP12 (LFS_OVERT)	1 ENABLE 0 DISABLE	DEFAULT
L	L	L	X001	FS_OVERT ENABLE	
L	L	M	X000	FS_OVERT DISABLE	

STRAPS	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default

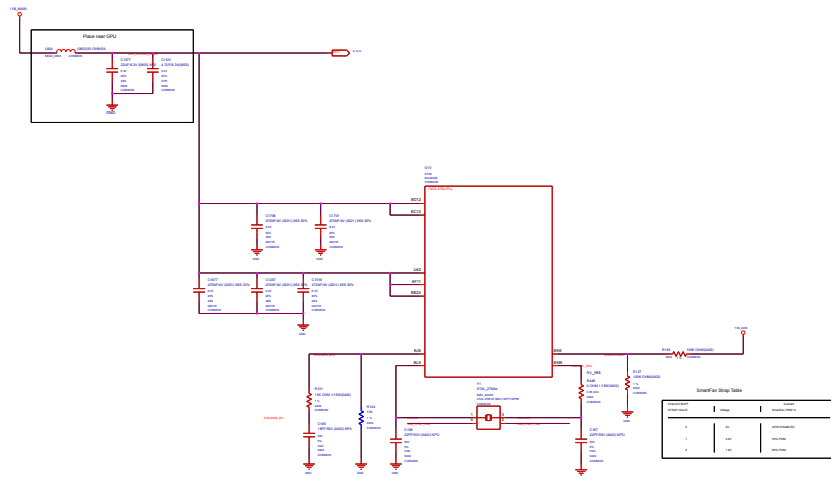
RAMCFGH (6)	DENSITY	WIDTH	VENDOR
0000	8Gb	256-Gb	Samsung
0001	8Gb	256-Gb	Micron
0010	8Gb	256-Gb	Hynix
0110	16Gb	256-Gb	Samsung
0111	16Gb	256-Gb	Samsung

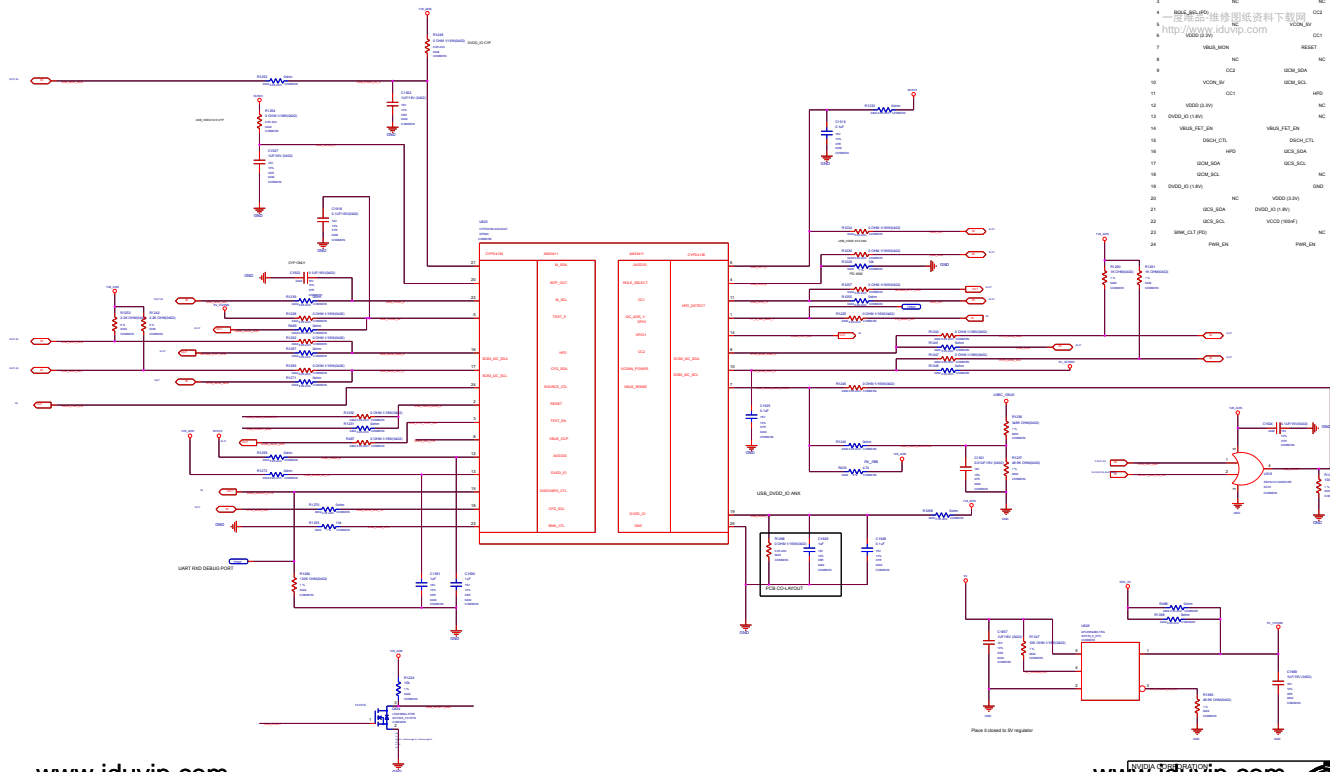


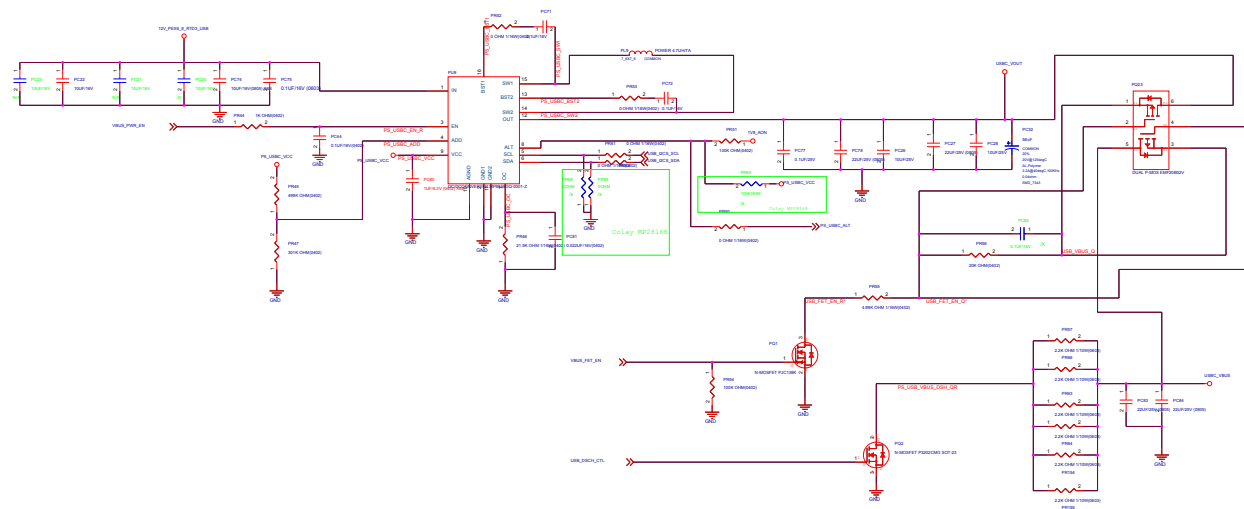
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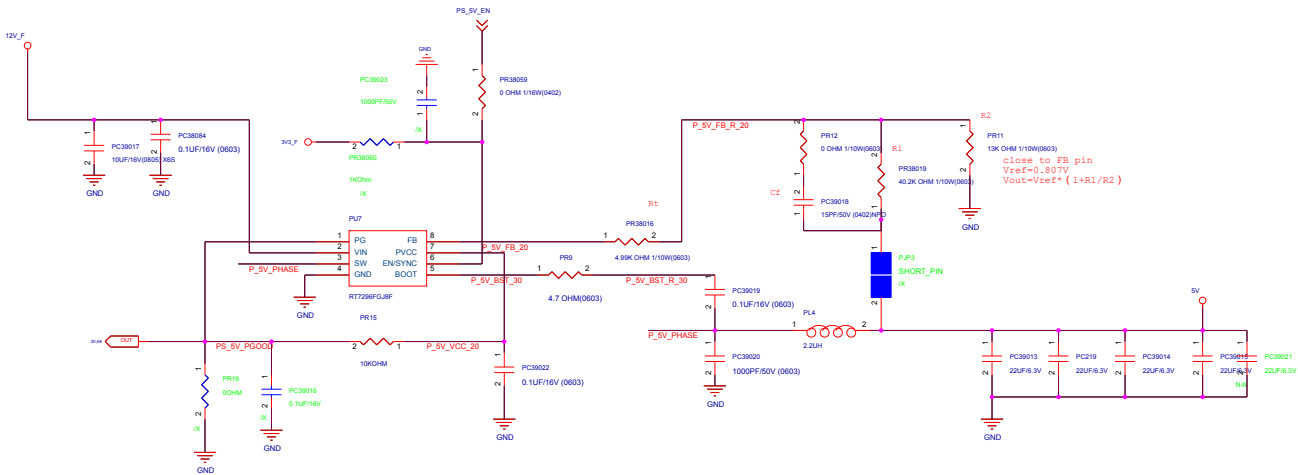
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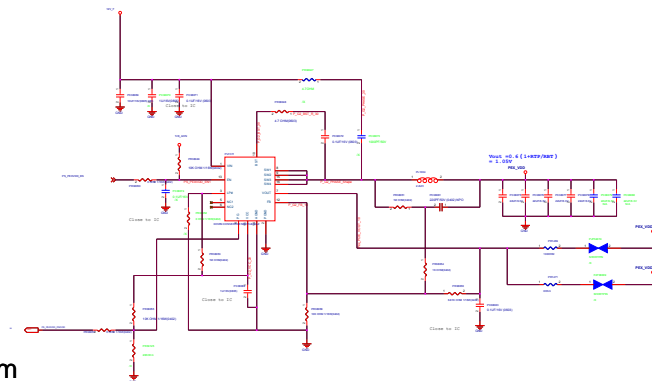
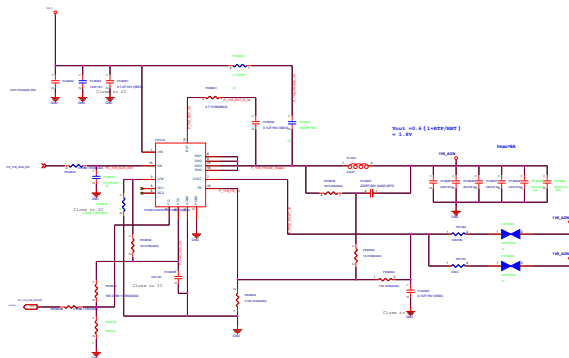




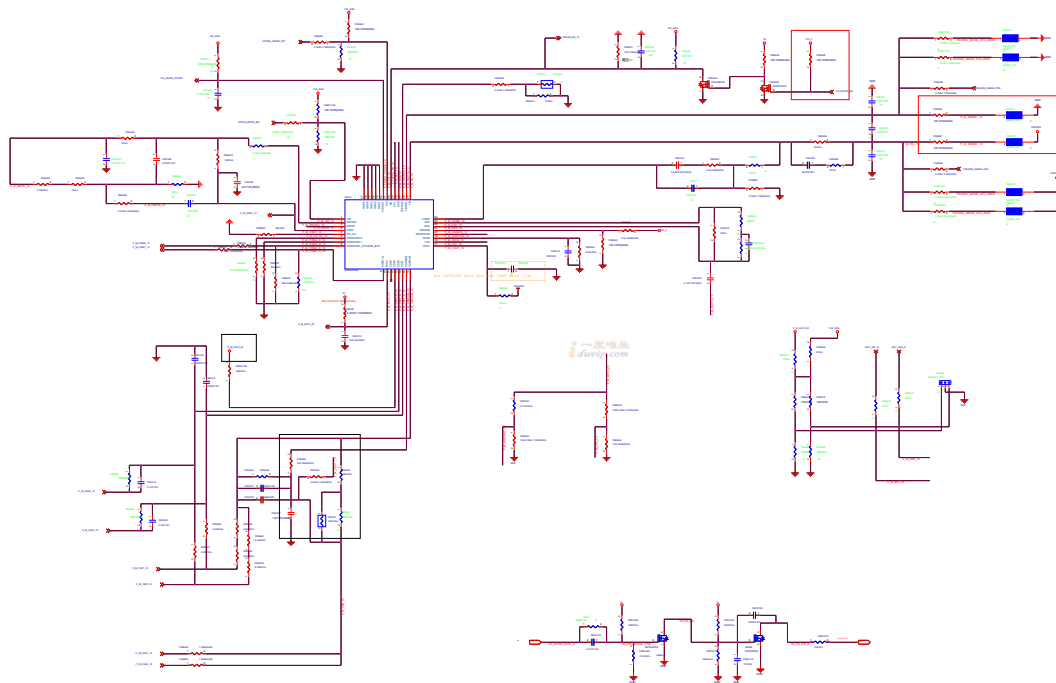


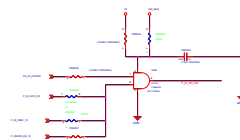
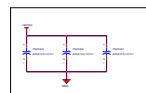
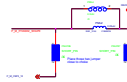
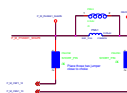
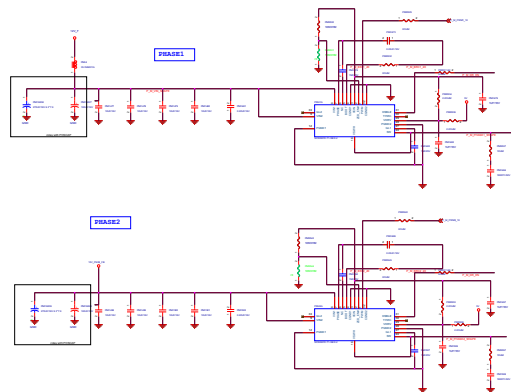


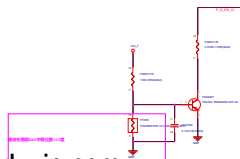
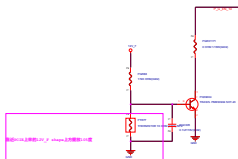


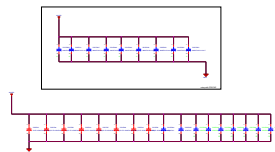
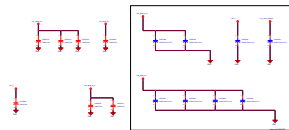
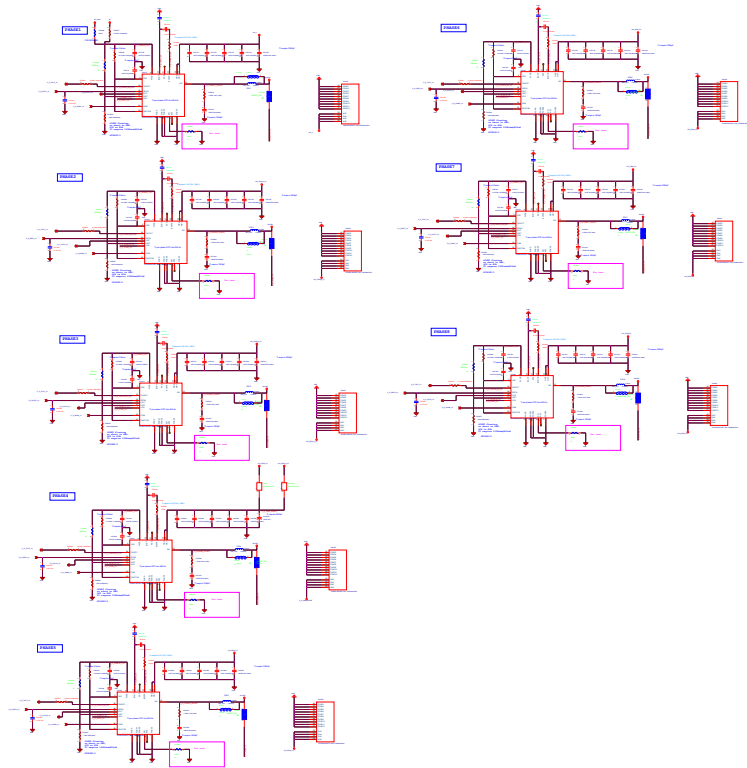


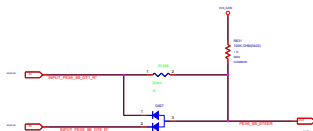
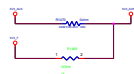
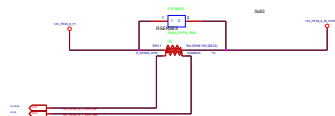
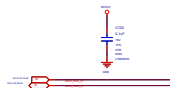
图例	说明
1	2
3	4



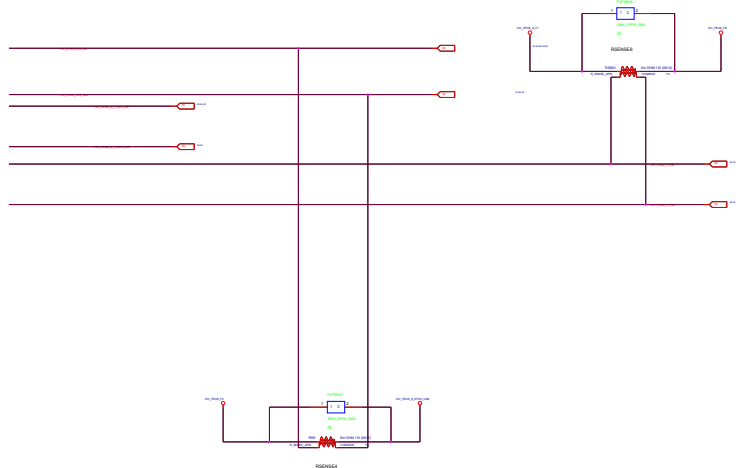








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PROPERTY	PROPERTY DESCRIPTION
FILE NAME	FILE NAME DESCRIPTION

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SUNDAE ELECTRONICS, INC.

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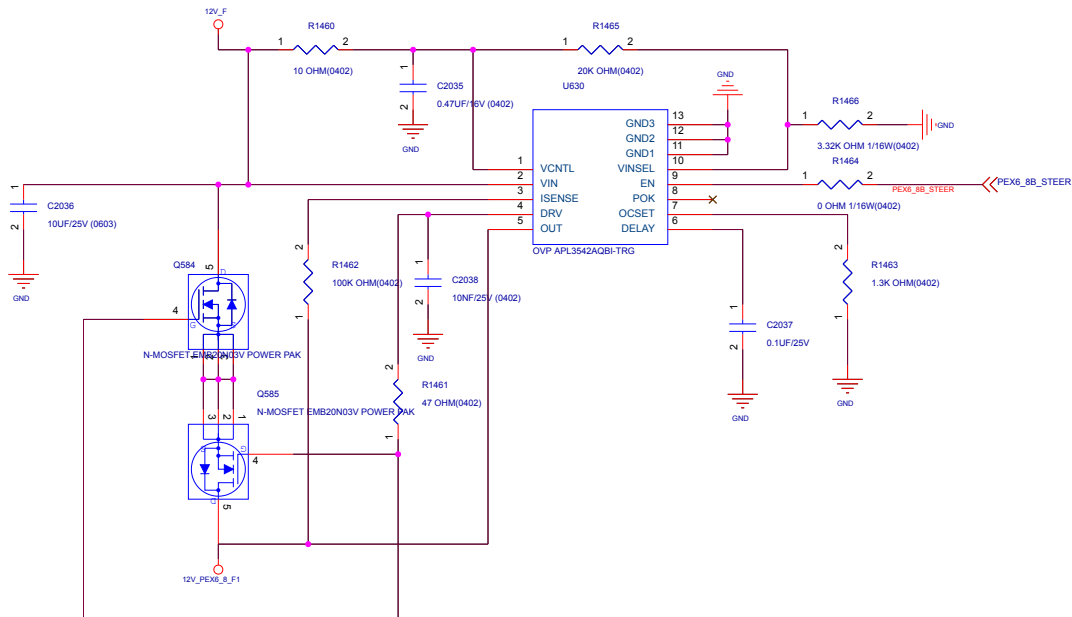
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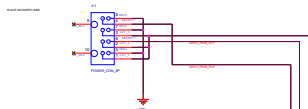
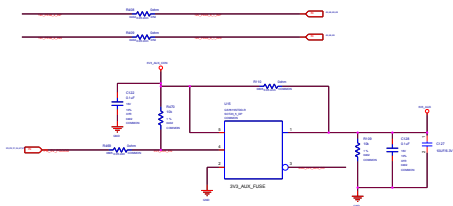
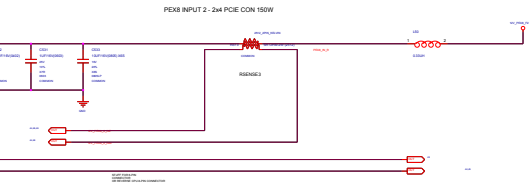
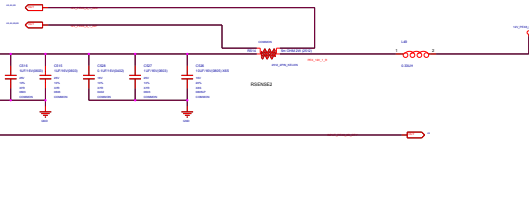
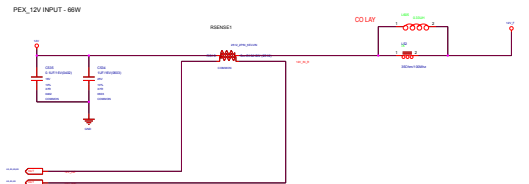
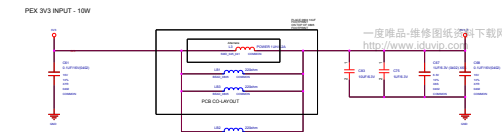
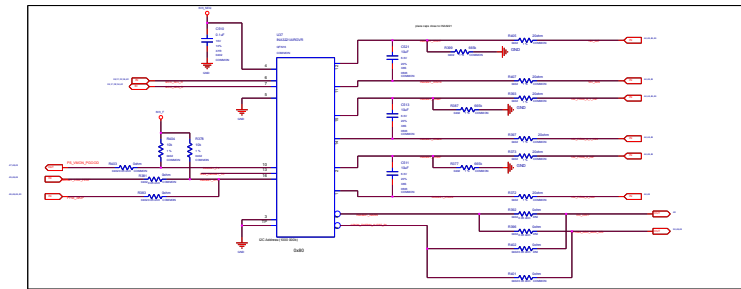
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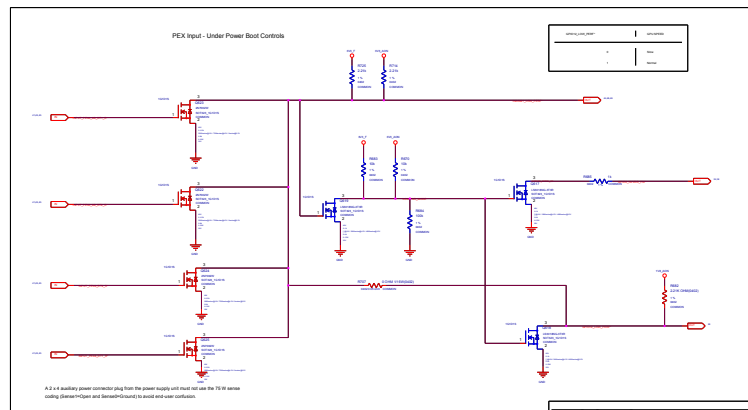
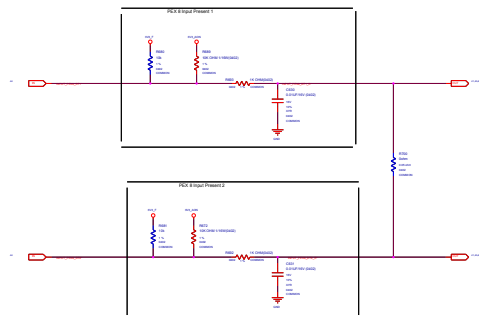
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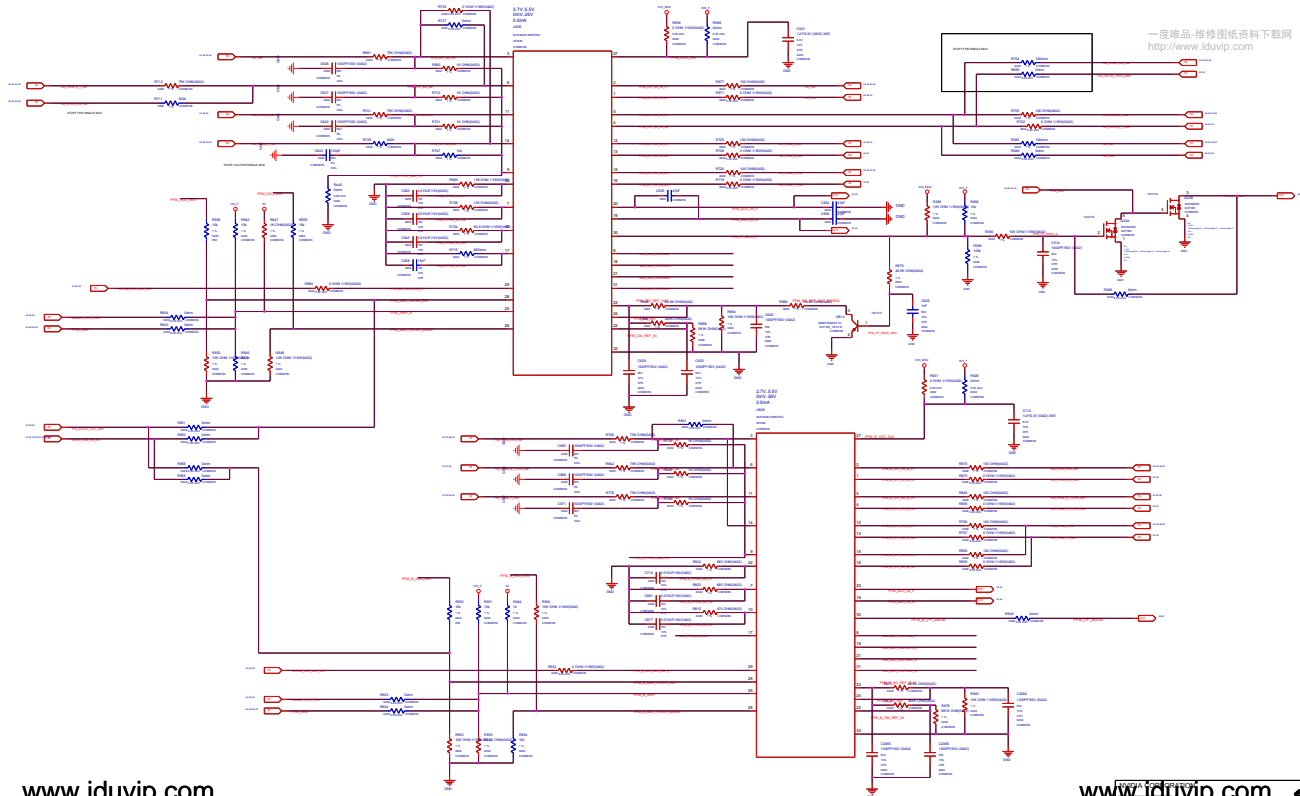
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A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense=Open and Sense=Ground) to avoid end-user confusion.

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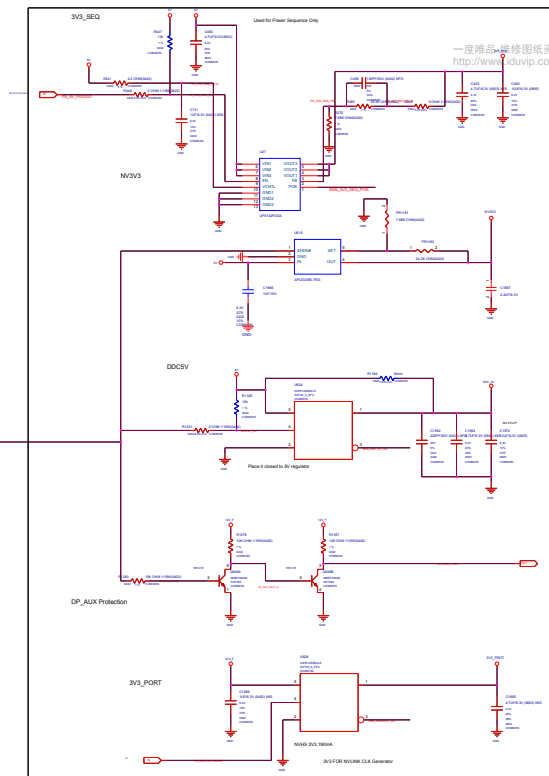
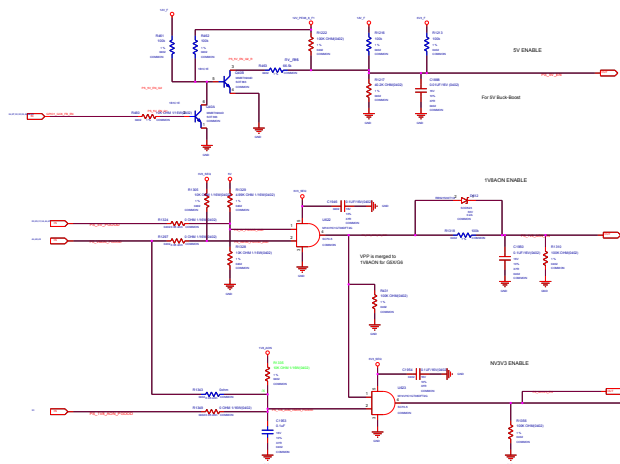
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INSTRUMENT	PERFORMANCE INFORMATION REPORT	
INSTRUMENT #	PERFORMANCE INFORMATION REPORT	



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SANTA CLARA, CALIFORNIA, USA					
NV_PN		600-1G180-BASE-200			
PCB REV	Footprint Size	PAGE	SEE CDP 34		
ORDER NO.	Q	DATE	20-JUNE-2015		



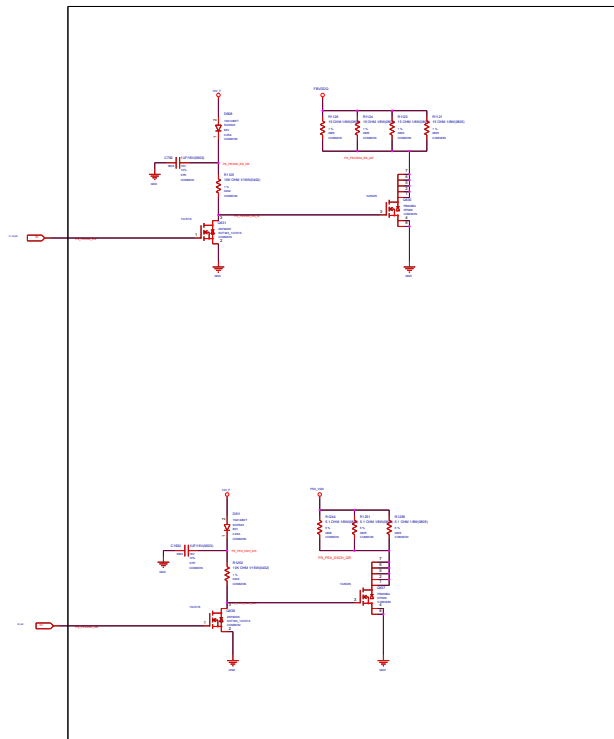
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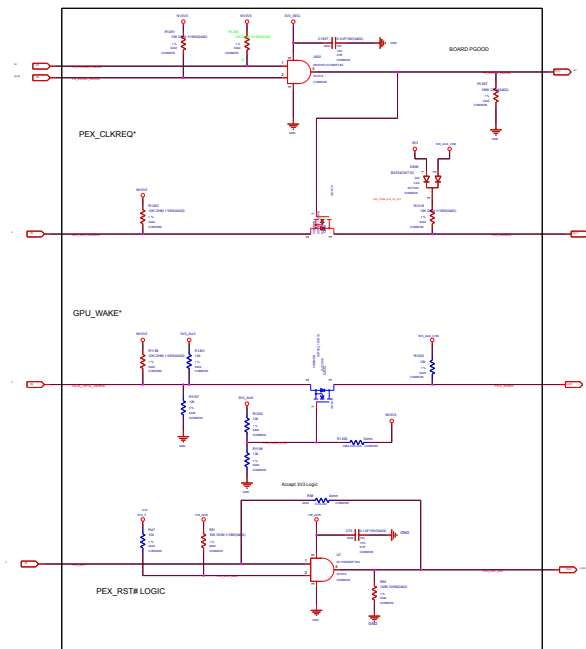
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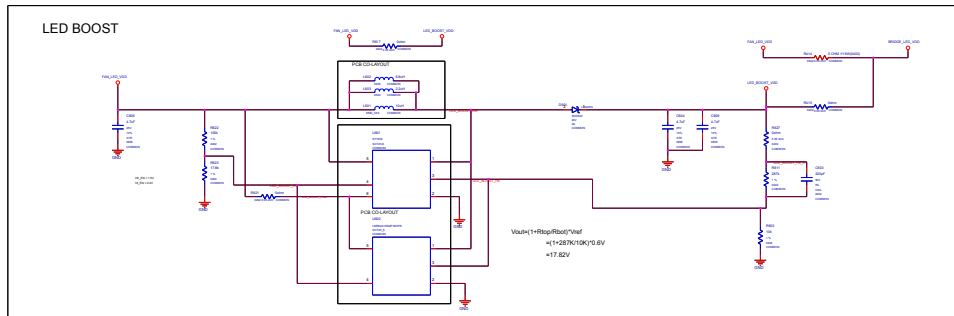
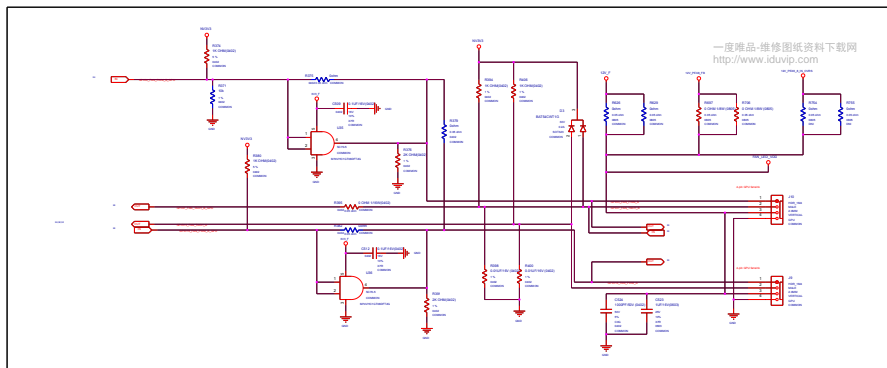
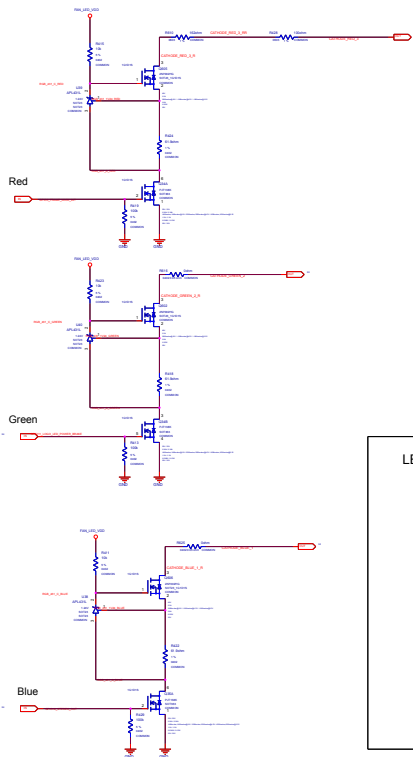


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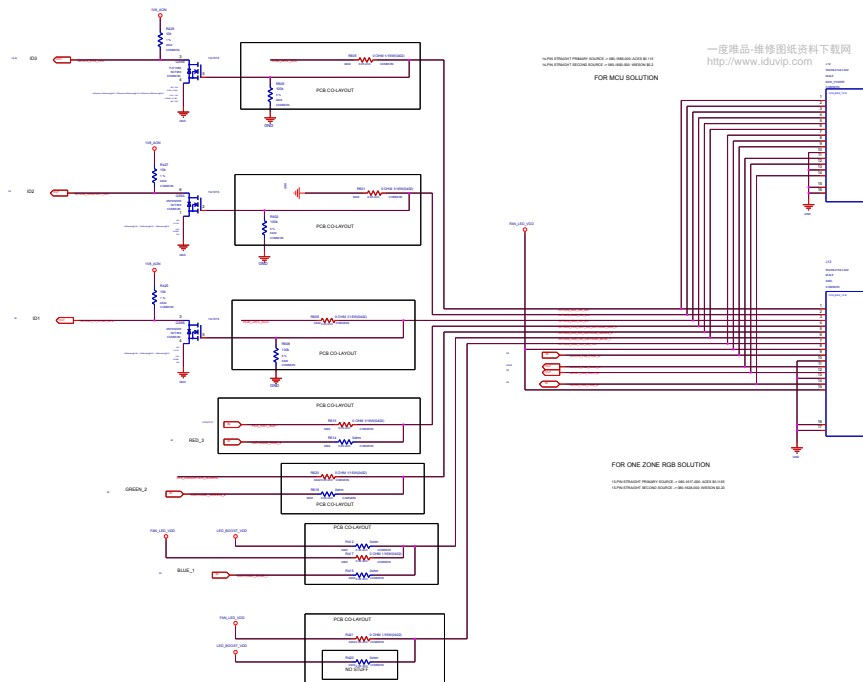
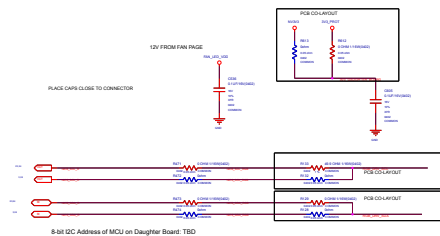


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ISSUE SERIAL	ISSUE TIME	ISSUE DATE





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