

PG210 B00

GP107 128b GDDR5, 75W , PCB 5.7"  
DVI-D\_DL (DP + DP) + HDMI (DP) + DP

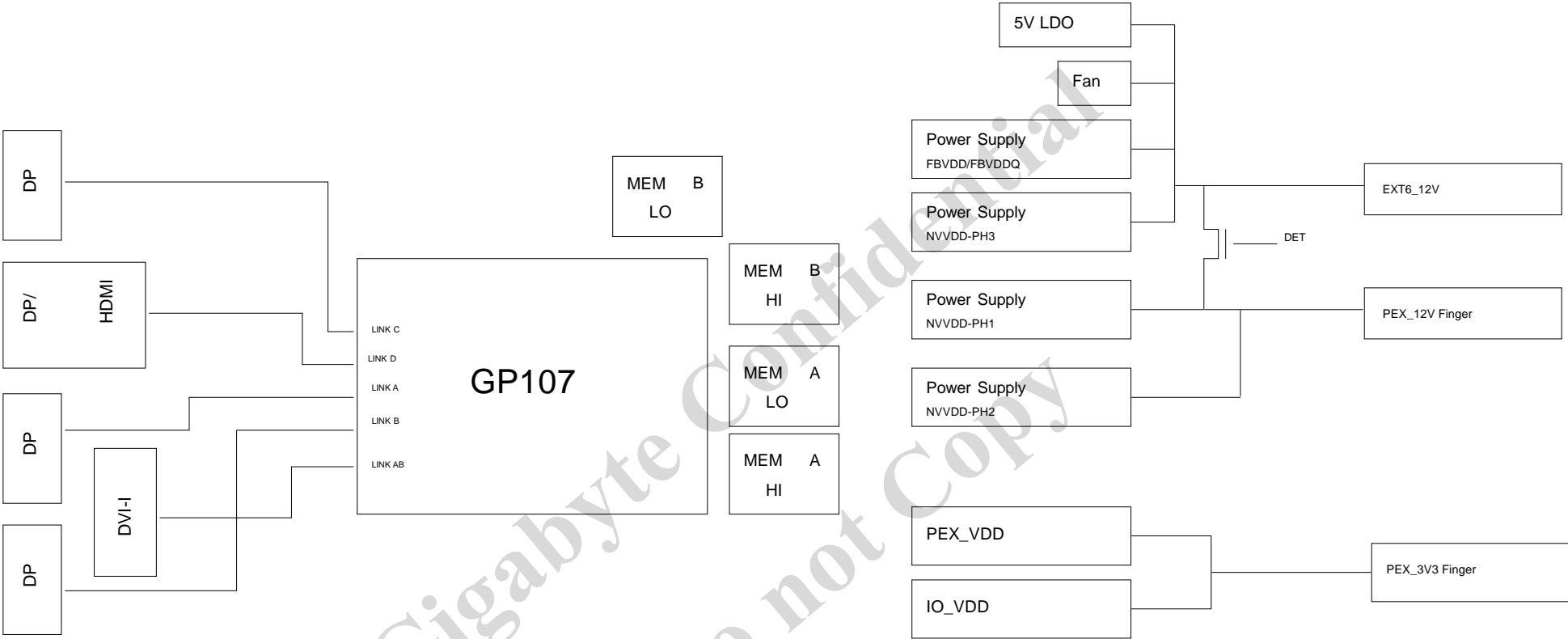
TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	MEMORY: GPU Partition A/B
5	MEMORY: FBA[31:0]
6	MEMORY: FBA[63:32]
7	MEMORY: FBB[31:0]
8	MEMORY: FBB[63:32]
9	GPU FBVDDQ & 1V8 Decoupling
10	GPU NVVDD & NVVDDS DECOUPLING
11	IFPAB DVI-DL
12	IFPD DP
13	IFPC HDMI
14	IFPEF UNUSED
15	MISC1: Fan, Thermal, JTAG, GPIO
16	MISC2: ROM, XTAL, Straps
17	Power Inputs and Filtering
18	Power Sequence
19	PS: NV3V3 & NV12V
20	PSI: 1V8
21	PSII: 5V & 12V_FAN
22	PS III: PEXVDD
23	PS IV: FBVDDQ
24	PS V: NVVDD OVR2+1
25	PS V: NVVDD Phase 1,2

Page	Description
26	PS V: NVVDD Phase 3
27	MECH: Bracket/Thermal

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Block Diagram

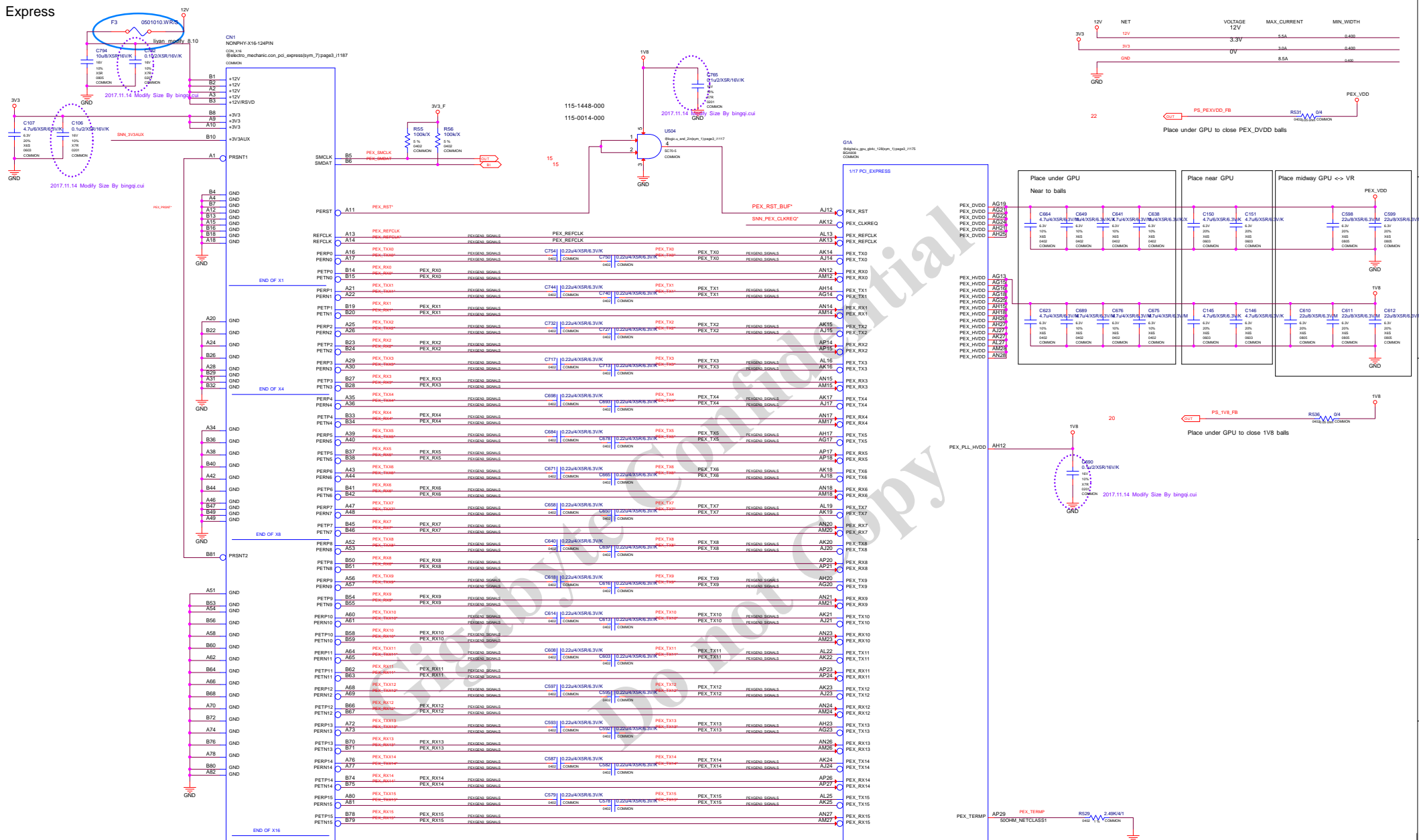


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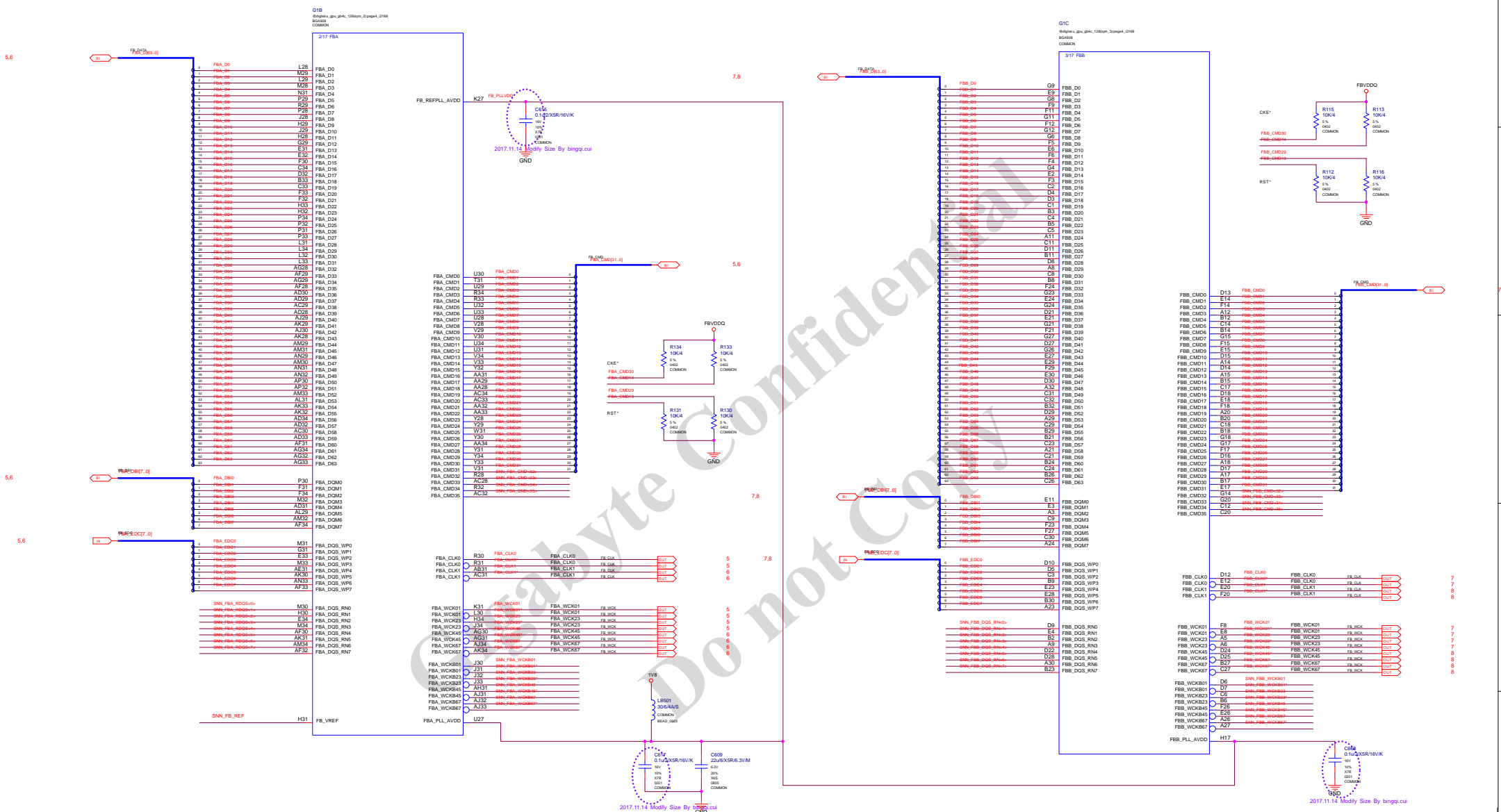
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Title			
Block Diagram			
Size	Document Number	Rev	
Custom	GV-N10600C-2GD	1.11	
Date:	Monday, January 29, 2018	Sheet	2 of 28

# PCI Express



# MEMORY: GPU Partition A/B



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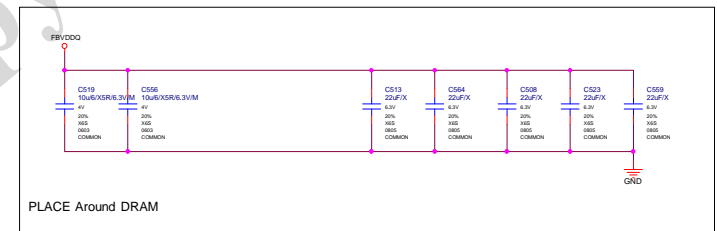
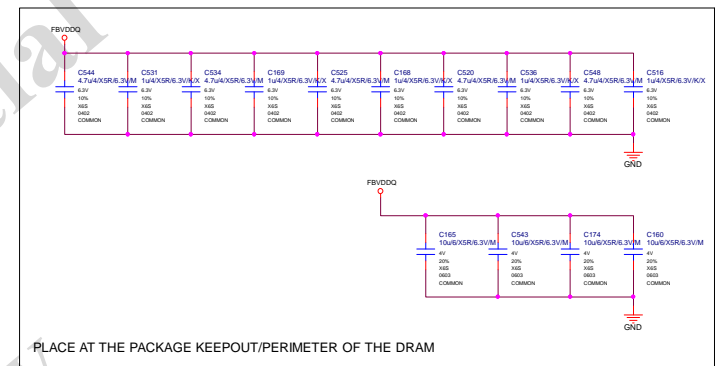
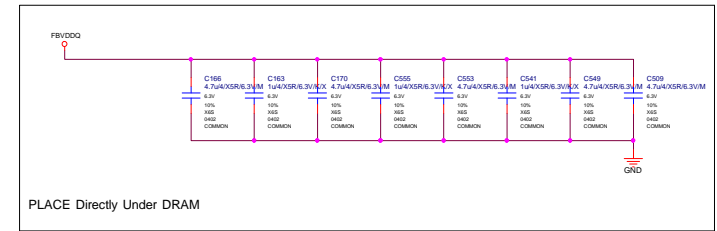
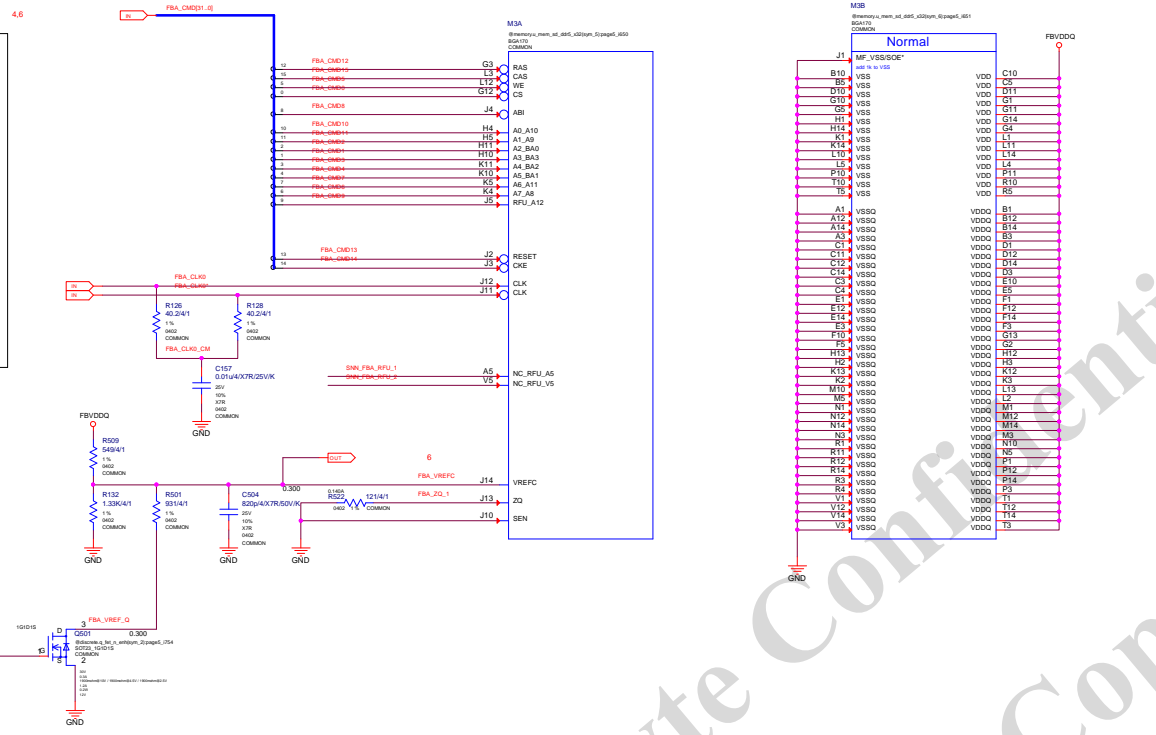
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MEMORY: GPU Partition A/B

File	MEMORY_GPU Partition A_B	Rev	1.11
Size	Document Number		
Customer	CW-NV-N1660C-2D0		
Date	Monday, January 29, 2018	Sheet	4 of 28

MEMORY: FBA Partition 31..0

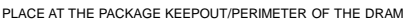
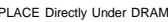
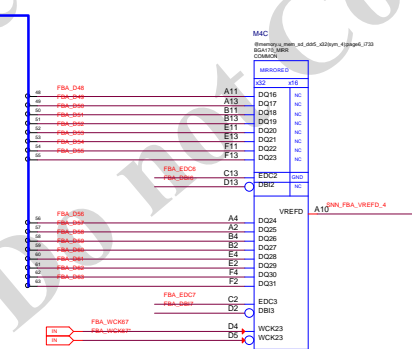
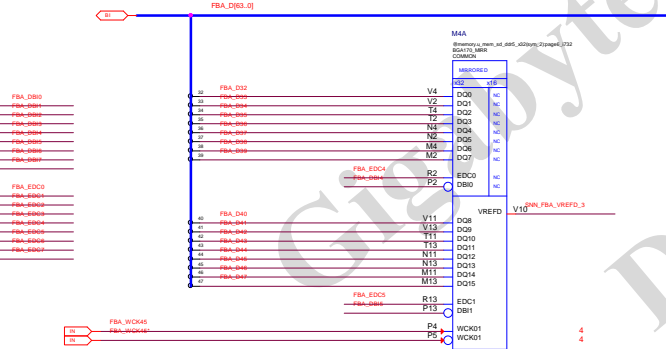
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CMD0	CS*	
CMD1	A3..BA3	
CMD2	A2..BA2	
CMD3	A4..BA2	
CMD4	A6..BA1	
CMD5	WE*	
CMD6	A7	
CMD7	AE..A11	
CMD8	AB1*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A0	
CMD12	RA5*	
CMD13	RS1*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3..BA3
CMD18		A2..BA0
CMD19		A4..BA2
CMD20		A6..BA1
CMD21		WE*
CMD22		A7
CMD23		AE..A11
CMD24		AB1*
CMD25		A12..RFU
CMD26		A0..A10
CMD27		A1..A0
CMD28		RA5*
CMD29		RS1*
CMD30		CKE*
CMD31		CAS*



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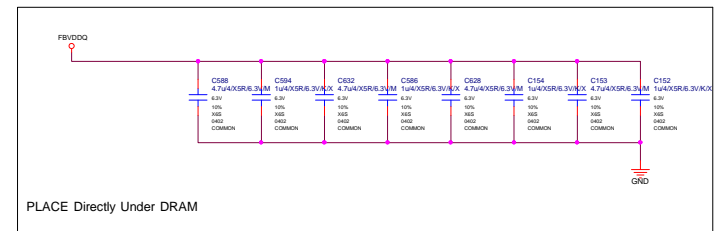
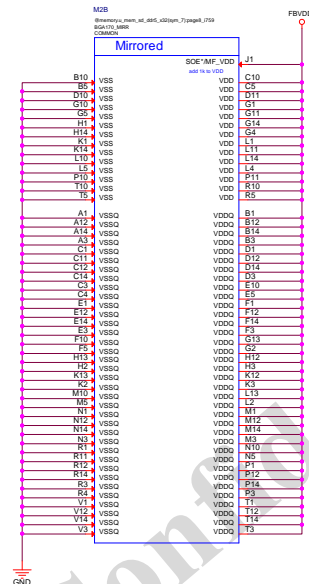
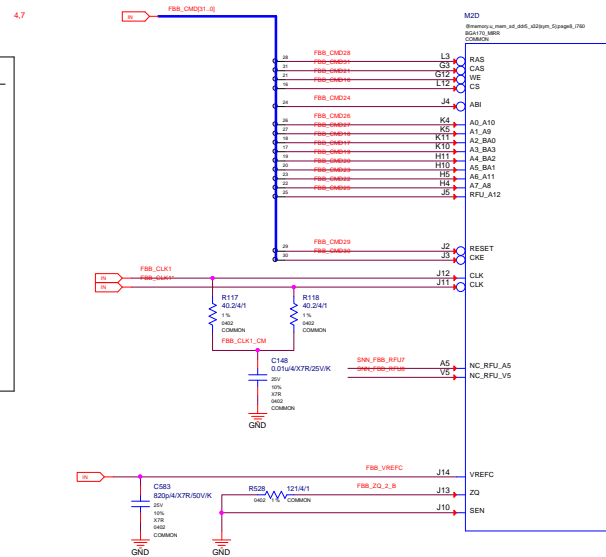
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Date:	Monday, January 26, 2015	Sheet	5 of 26

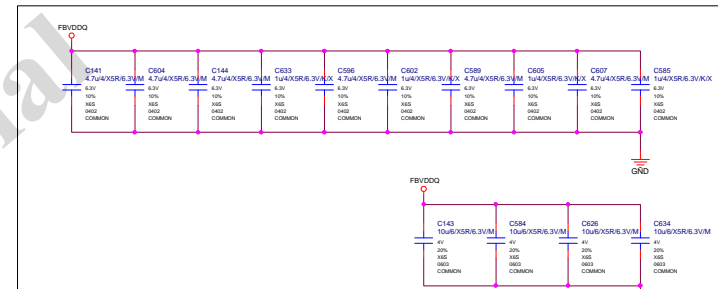
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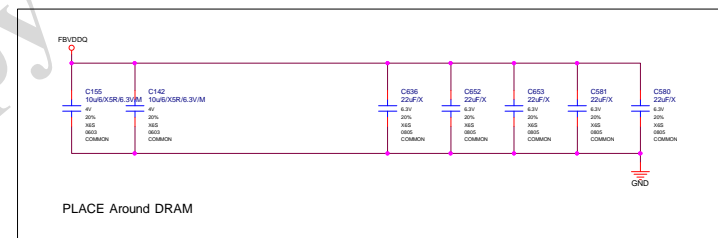
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CMD4	AE..BA1	
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CMD6	A7..AB	
CMD7	AB*, AE..A11	
CMD8	A12..RFU	
CMD9	A0..A10	
CMD11	A1..AB	
CMD12	RA*	
CMD13	RS†	
CMD14	CW*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3..BA3
CMD18		A2..BA0
CMD19		A4..BA2
CMD20		AE..BA1
CMD21		WE*
CMD22		A7..AB
CMD23		AB*, AE..A11
CMD24		A12..RFU
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CMD29		RS†
CMD30		CW*
CMD31		CAS*



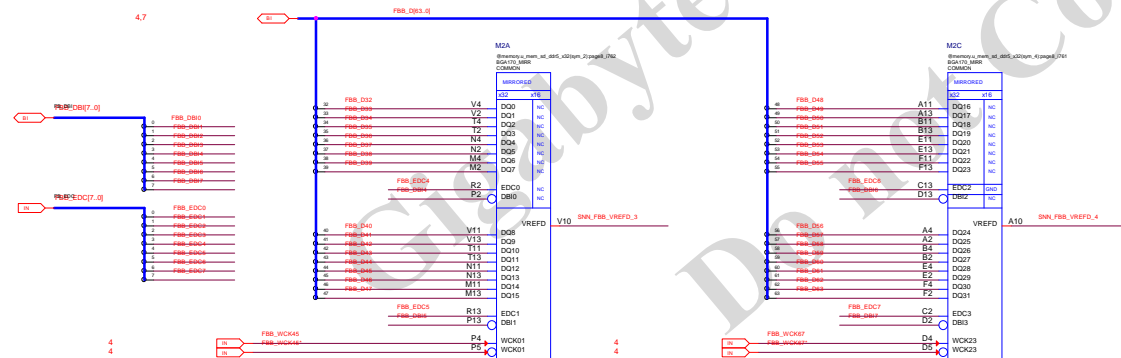
PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM

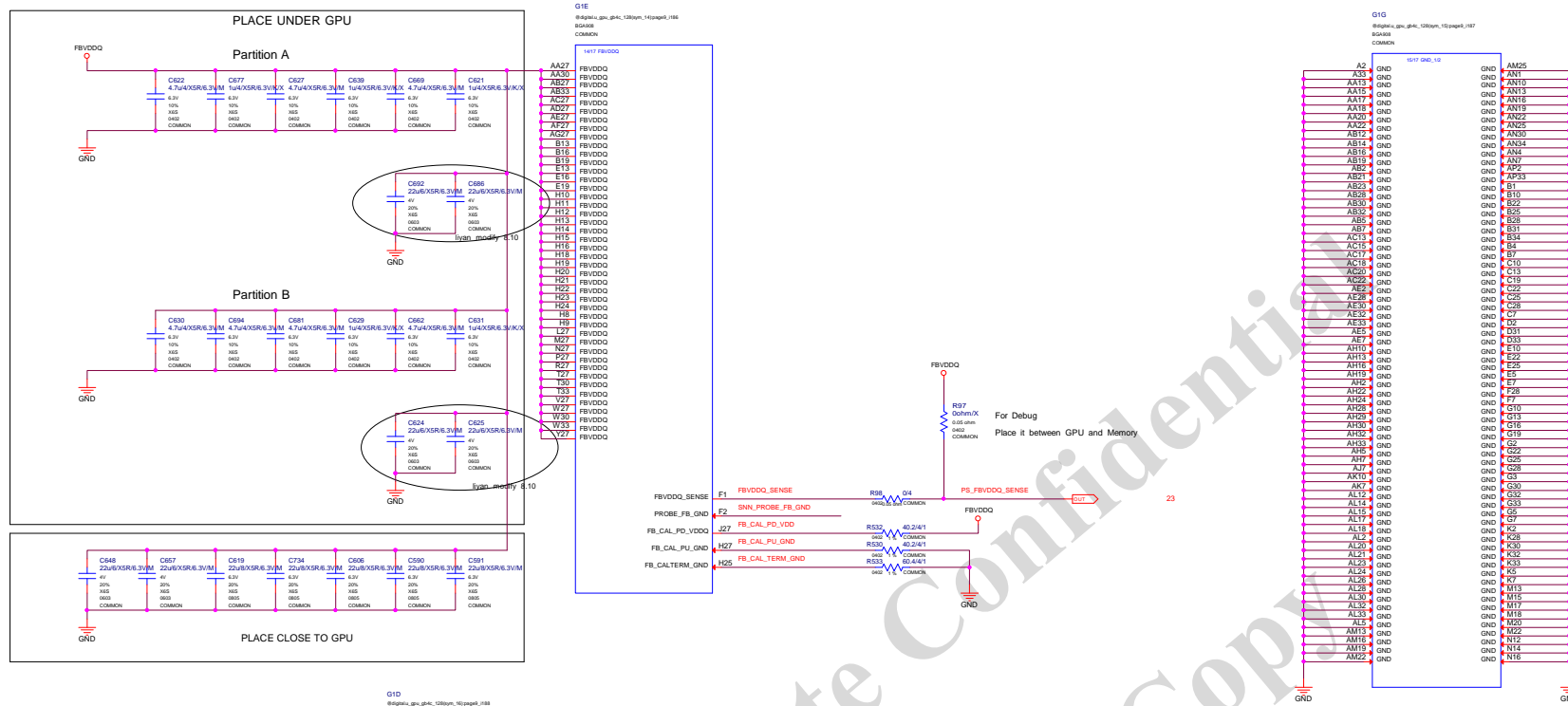


PLACE Around DRAM





## GPU FBVDDQ & 1V8 Decoupling



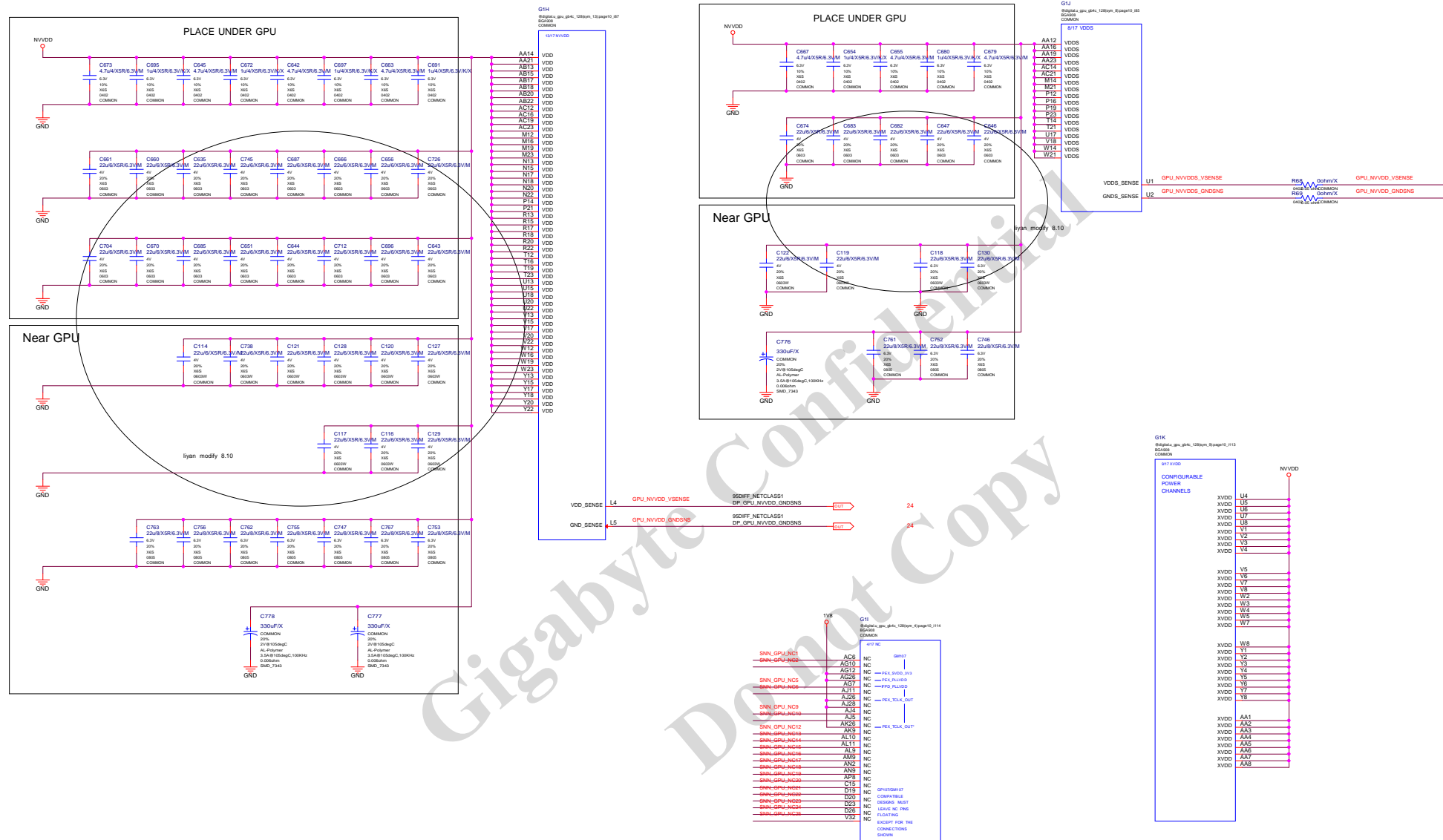
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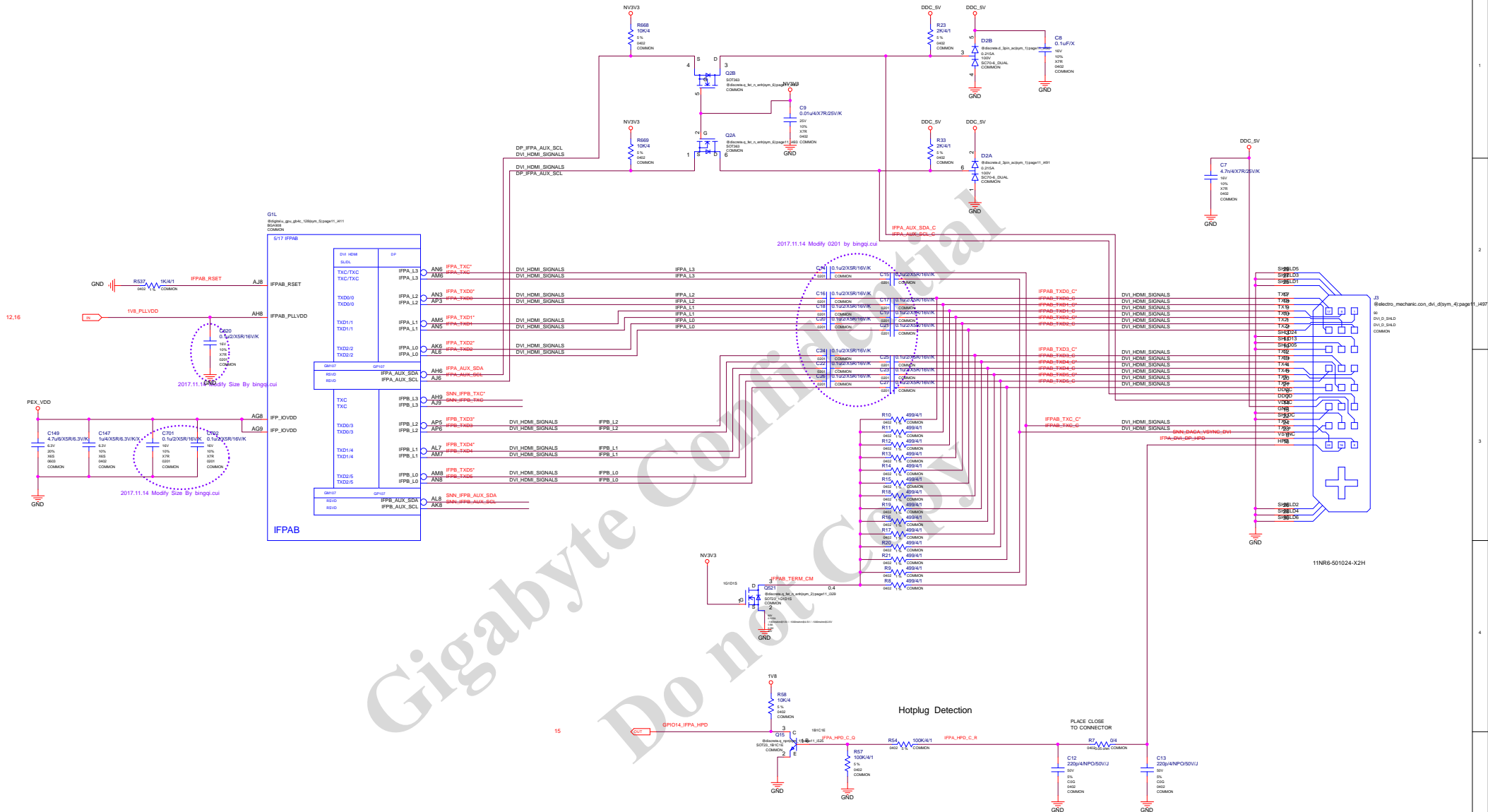
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GPU FBVDDQ & 1V8 Decoupling

Title		
GPU FBVDDQ & 1V8 Decoupling		
Size	Document Number	Rev
Cust#	GV-N1050C-2GD	1.11
Date:	Monday, January 29, 2018	Sheet 9 of 28

## GPU NVVDD & NVVDDS Decoupling



# IFPAB DVI-DL

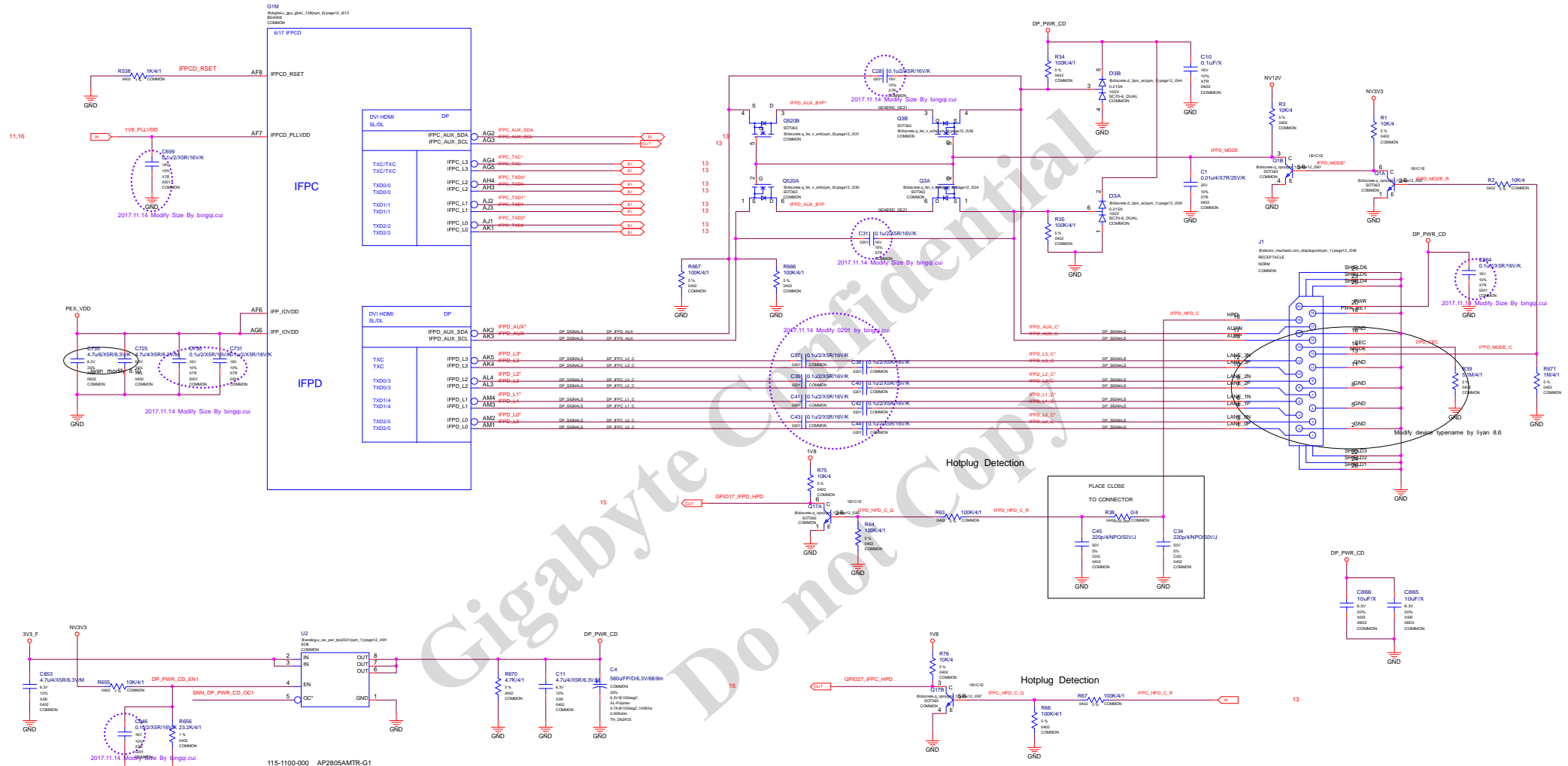


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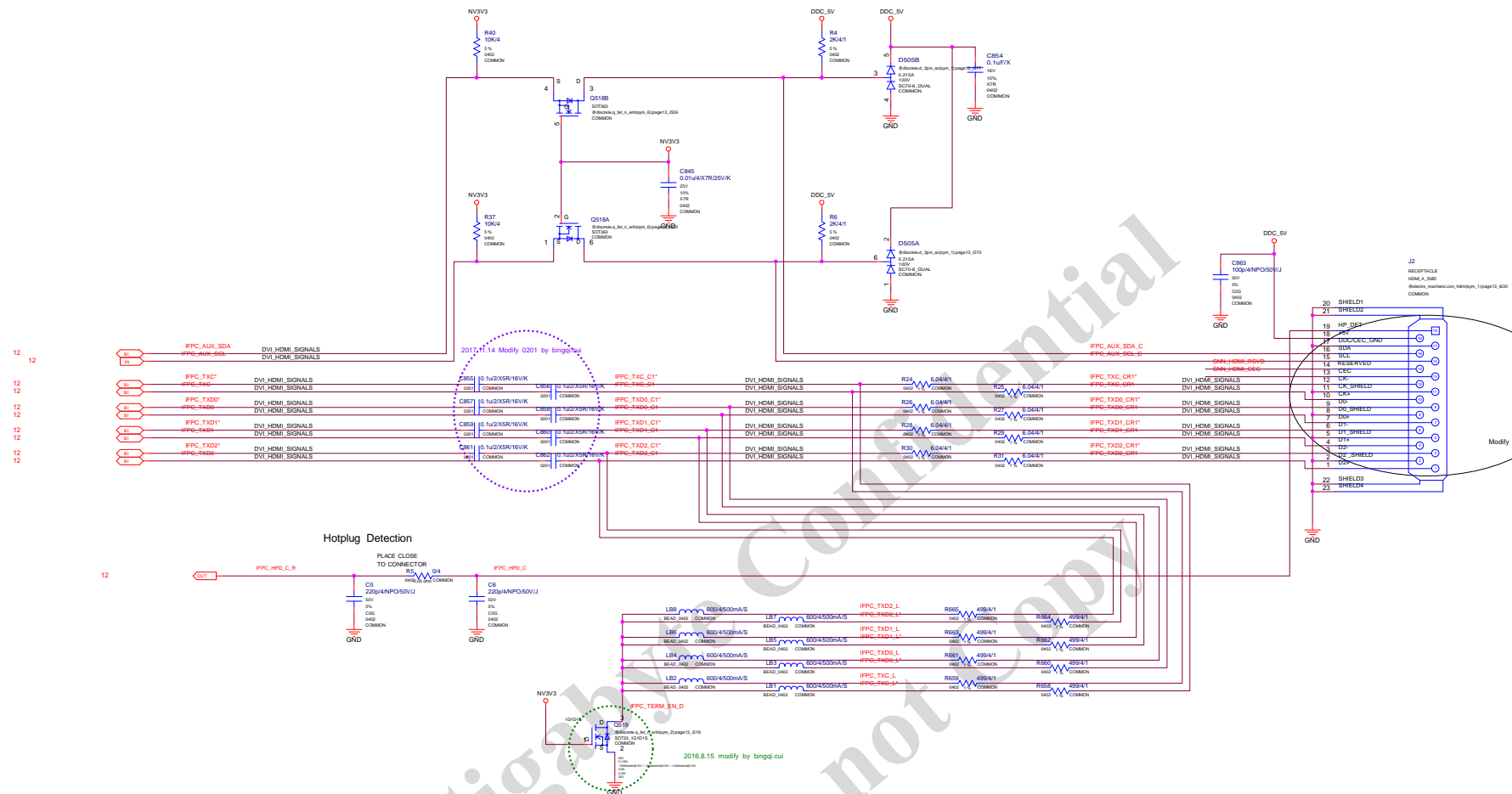
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IFPAB DVI-DL

File	GPU NVDDO & NVDDOS Decoupling
Doc	Document Number
Customer	CW-N1050C-2GD
Date	Monday, January 29, 2018
Sheet	11 of 28
Rev	1.11



## IFPC HDMI



Modify device typename by liyan 8.6

## Hotplug Detection

PLACE CLOSE

IFPC\_HPD\_C\_R

IFPC\_HPD\_C

IFPC\_TERM\_EN\_D

2016.8.15 modify by bingqi.cui

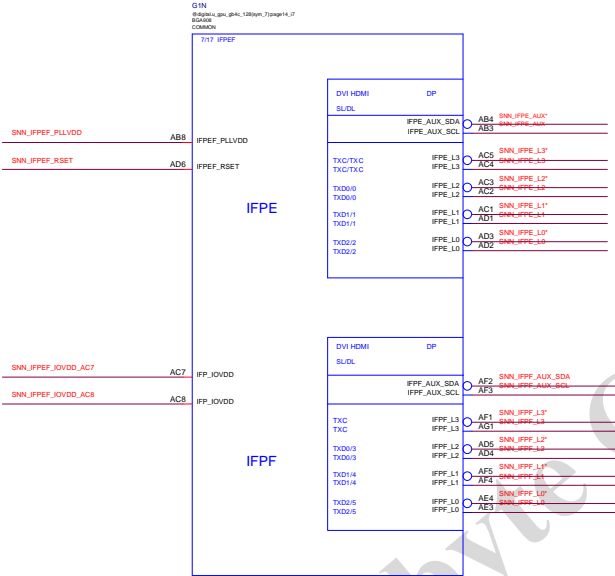
IFPC HDMI

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PAGE DETAIL

Title			
IFPC HDMI			
Size	Document Number	Rev	
Custm	GV-N1050C-2GD	1.11	
Date:	Monday, January 29, 2018	Sheet	13 of 28

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IFPEF UNUSED



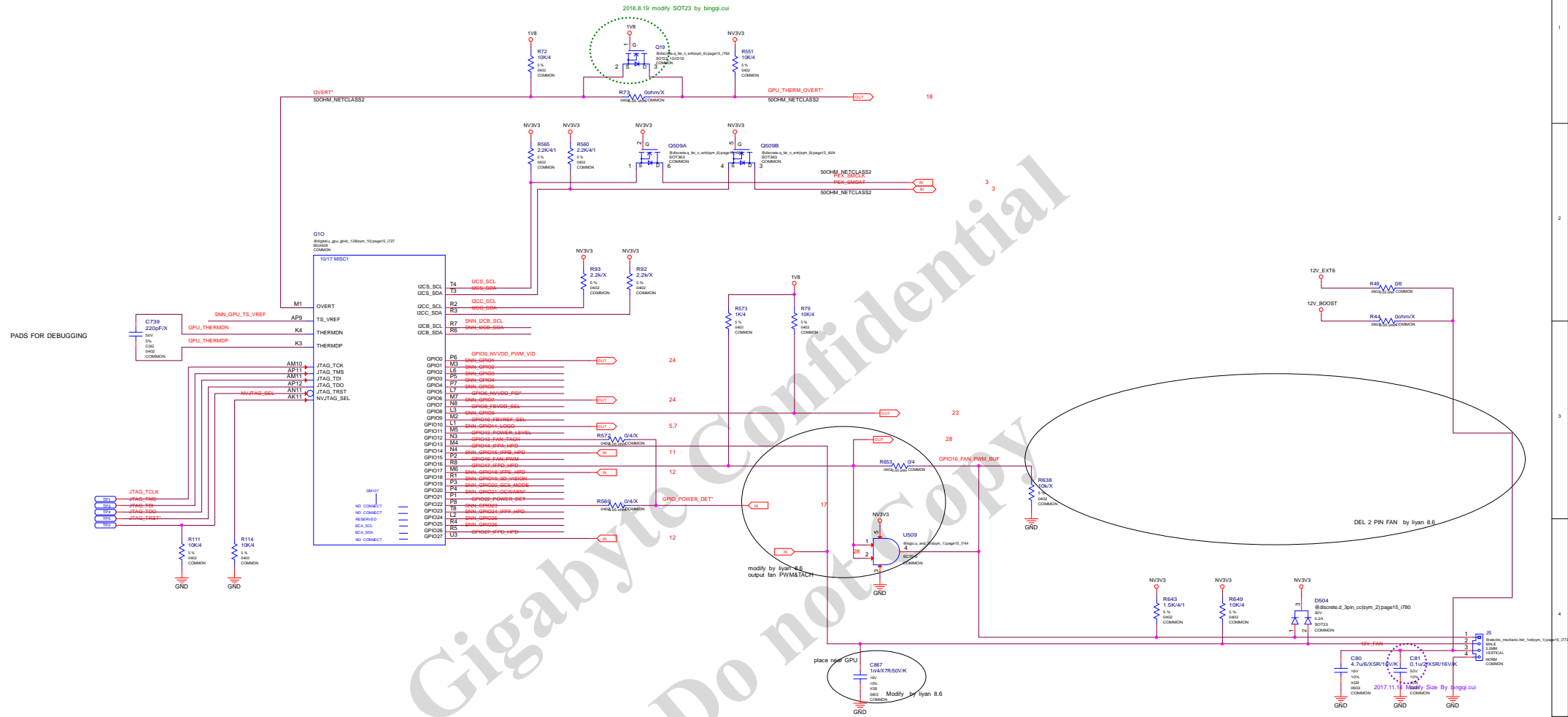
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Title		
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Doc	Document Number	Rev
Cust	2V-N1050C-2GD	1.11
Date	Monday, January 29, 2018	Sheet 14 of 28

MISC1: GPIO, Fan, Thermal, JTAG



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PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO

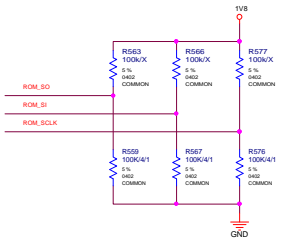
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GPIO, Fan, Thermal, JT4G			
Size	Document Number	Rev	
Cust#	GV-N10500C-2GD	1.11	
Date:	Monday, January 29, 2018	Sheet	15 of 28

MISC2: ROM, XTAL, Straps

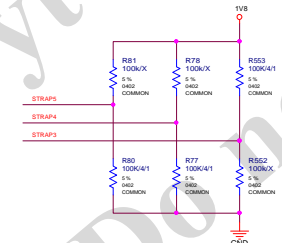
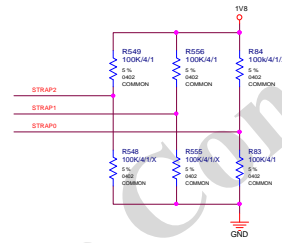
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L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	0000 Samsung B-Die 8Gb 256Mx32
L	L	H	0001 Micron F-Die 8Gb 256Mx32
L	H	L	0010 Hynix M-Die 8Gb 256Mx32
L	H	H	0011
H	H	L	0110 Hynix A-Die 4Gb 128Mx32
H	H	H	0111 Samsung E-Die 4Gb 128Mx32
L	L	M	1000 Micron B-Die 4Gb 128Mx32
L	M	L	1001

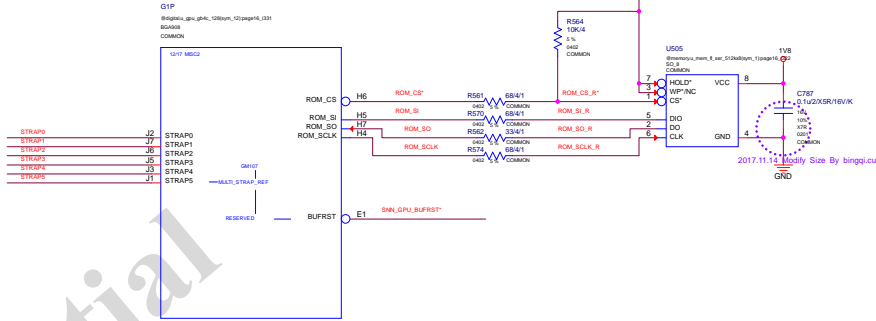
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	0
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0



H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

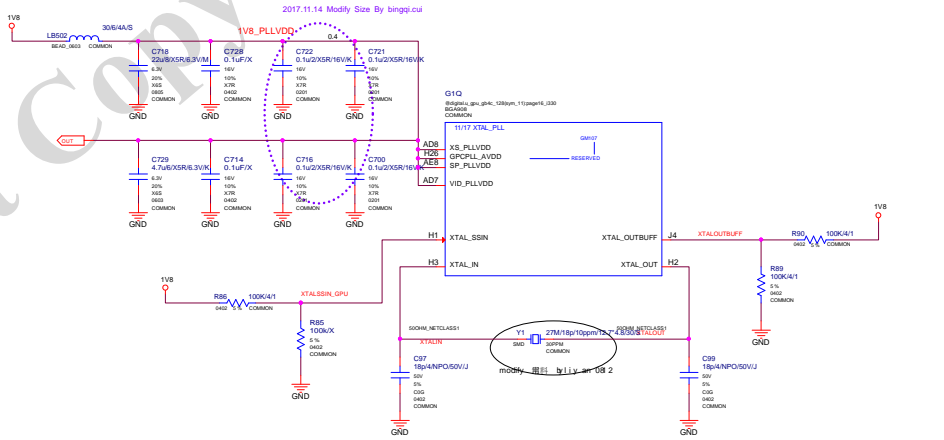


1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



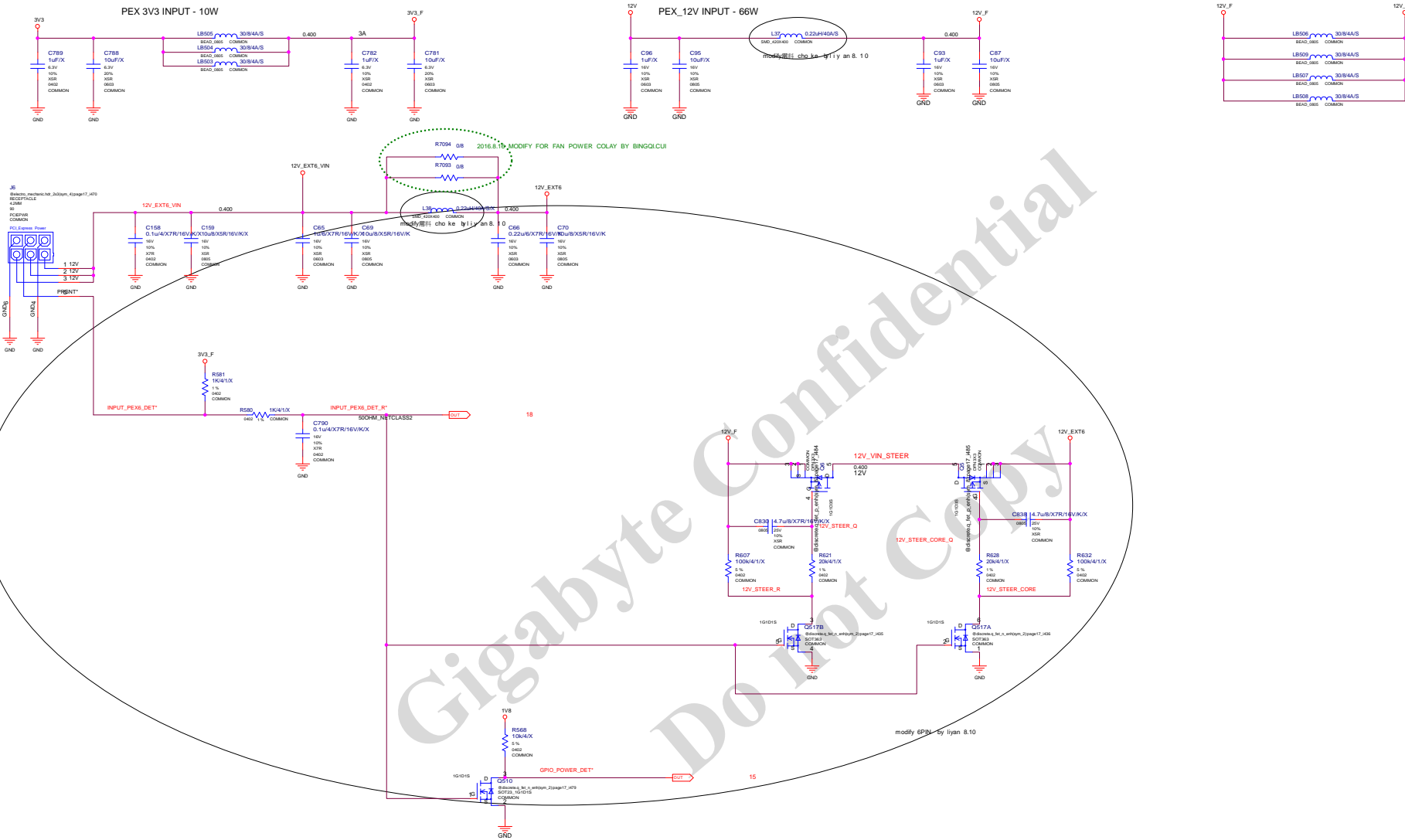
Smart Fan

XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM





## Power Inputs and Filtering



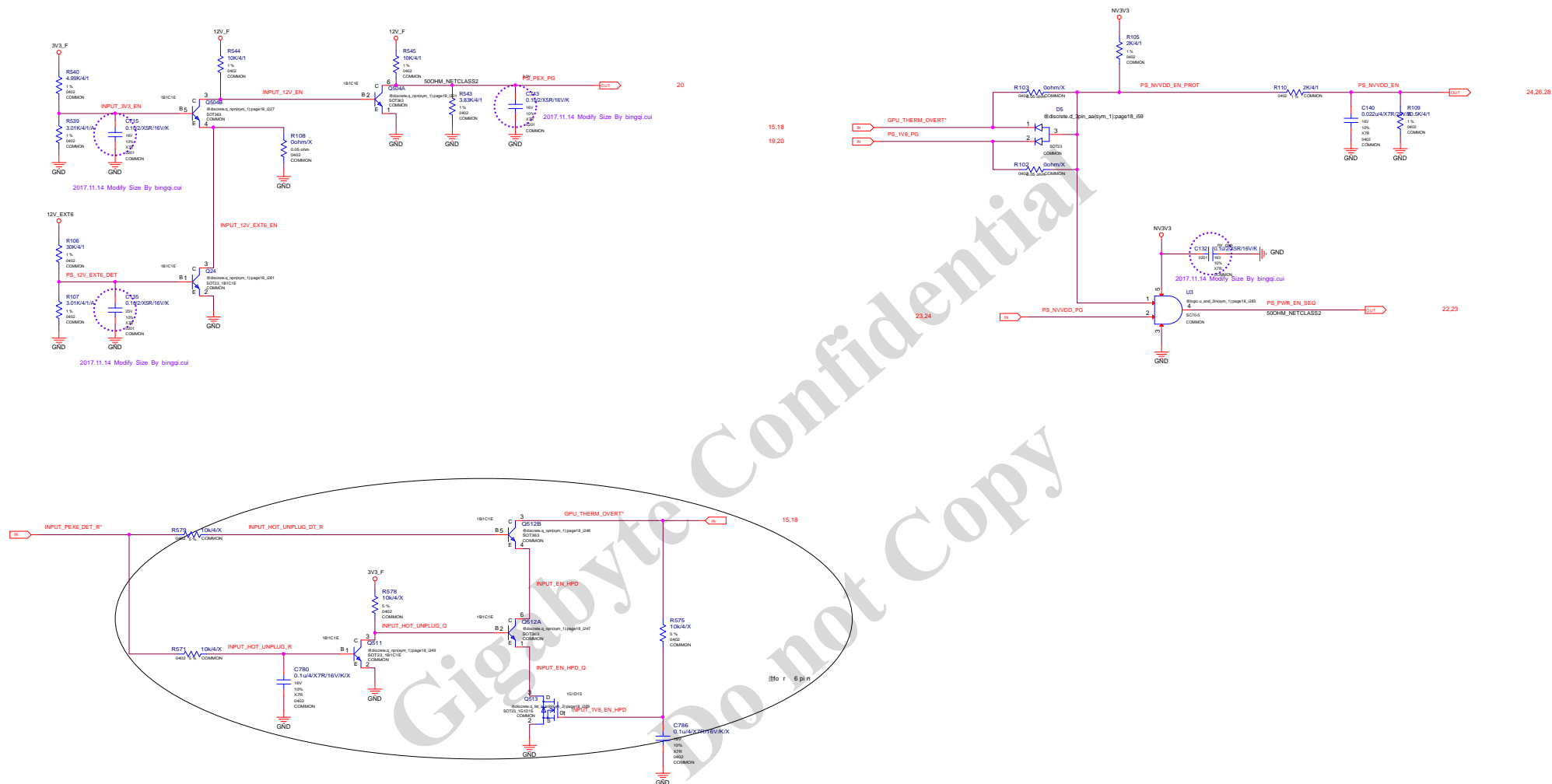
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ASSEMBLY  
PAGE DETAIL

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Power Inputs and Filtering

Title			
Power Inputs and Filtering			
Size	Document Number	Rev	
Customer	GV-N10500C-2GD	1.11	
Date:	Tuesday, January 30, 2018	Sheet	17 of 28

## Power sequence



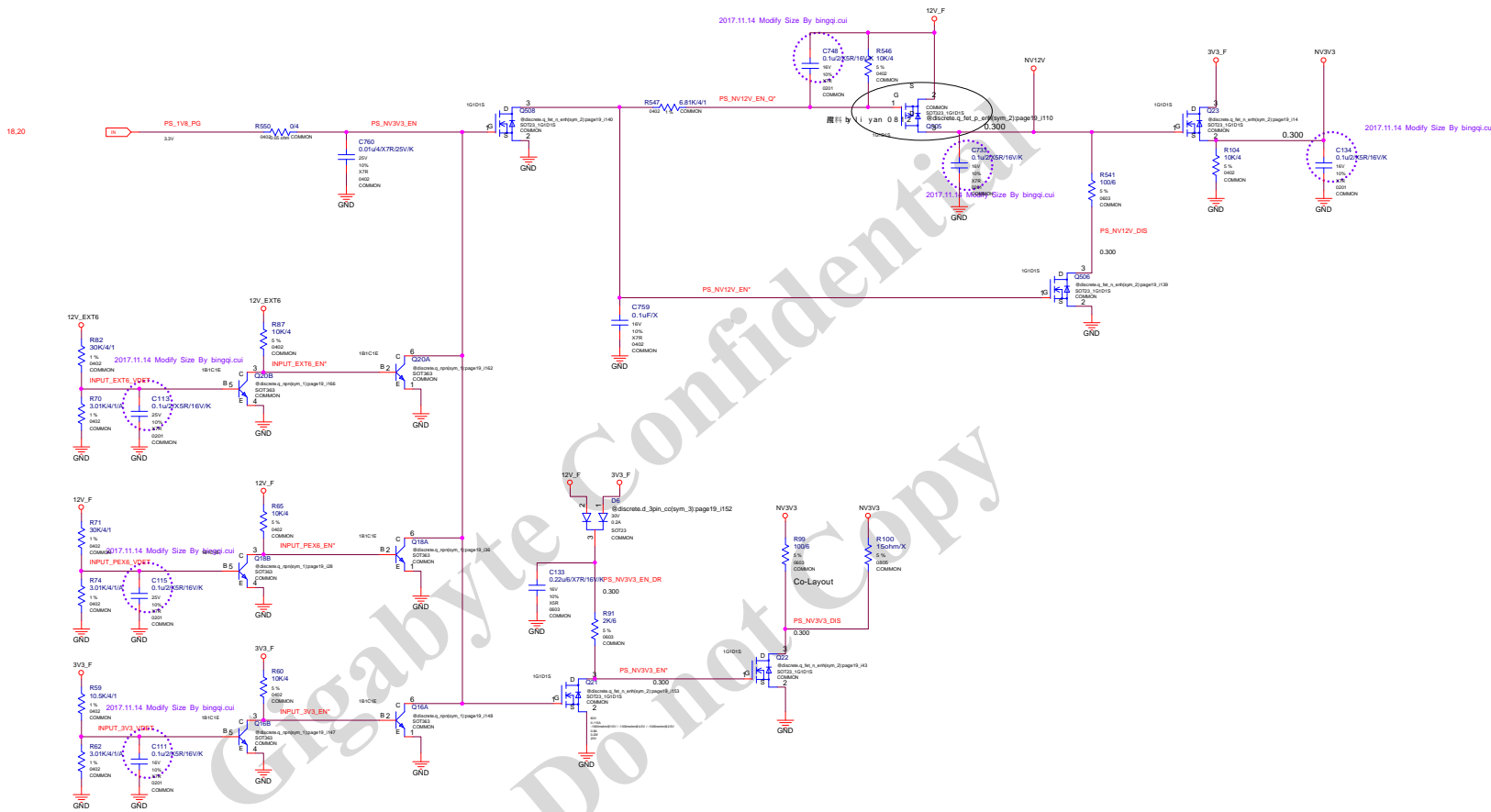
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ASSEMBLY  
PAGE DETAIL

Power Sequence

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Power sequence			
Size	Document Number		Rev
Custom	GV-N1050C-2GD		1.1
Date:	Monday, January 26, 2015	Sheet 18 of 28	

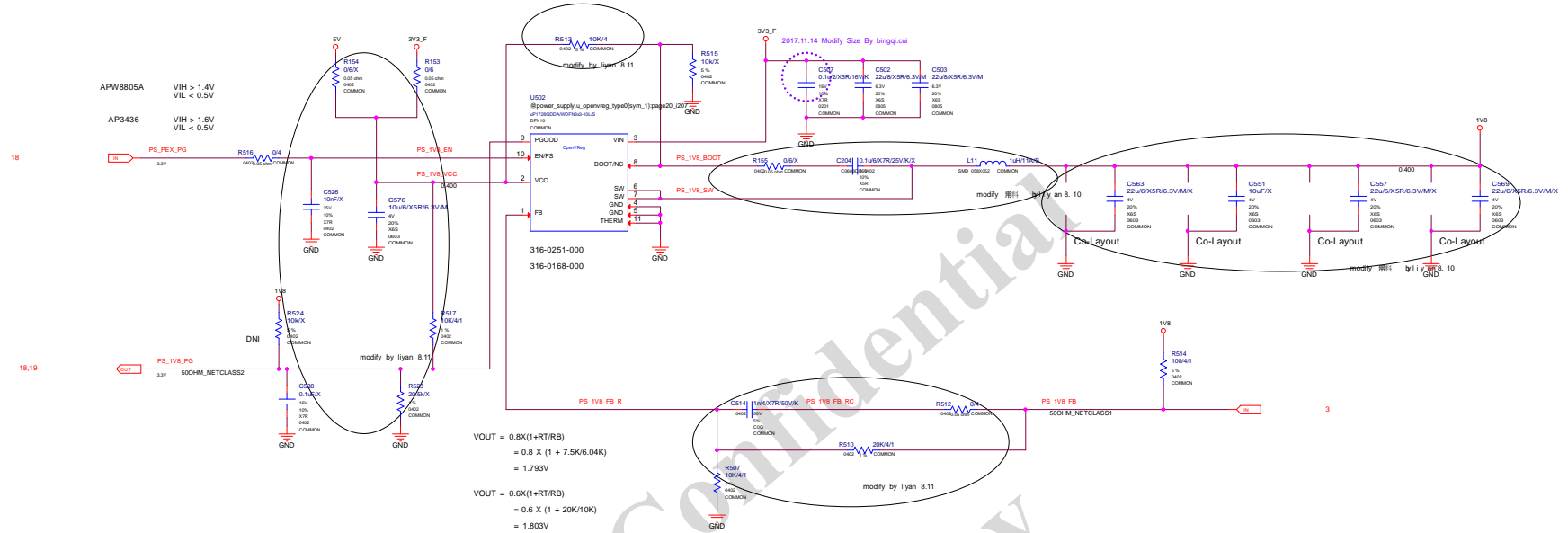
PS: NV3V3 & NV12V



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ASSEMBLY  
PAGE DETAIL  
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PS: NV3V3 & NV12V

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NV3V3 & NV12V		
Doc	Document Number	Rev
Cust	Customer Number	1.11
Date	Monday, January 29, 2018	Sheet 18 of 28

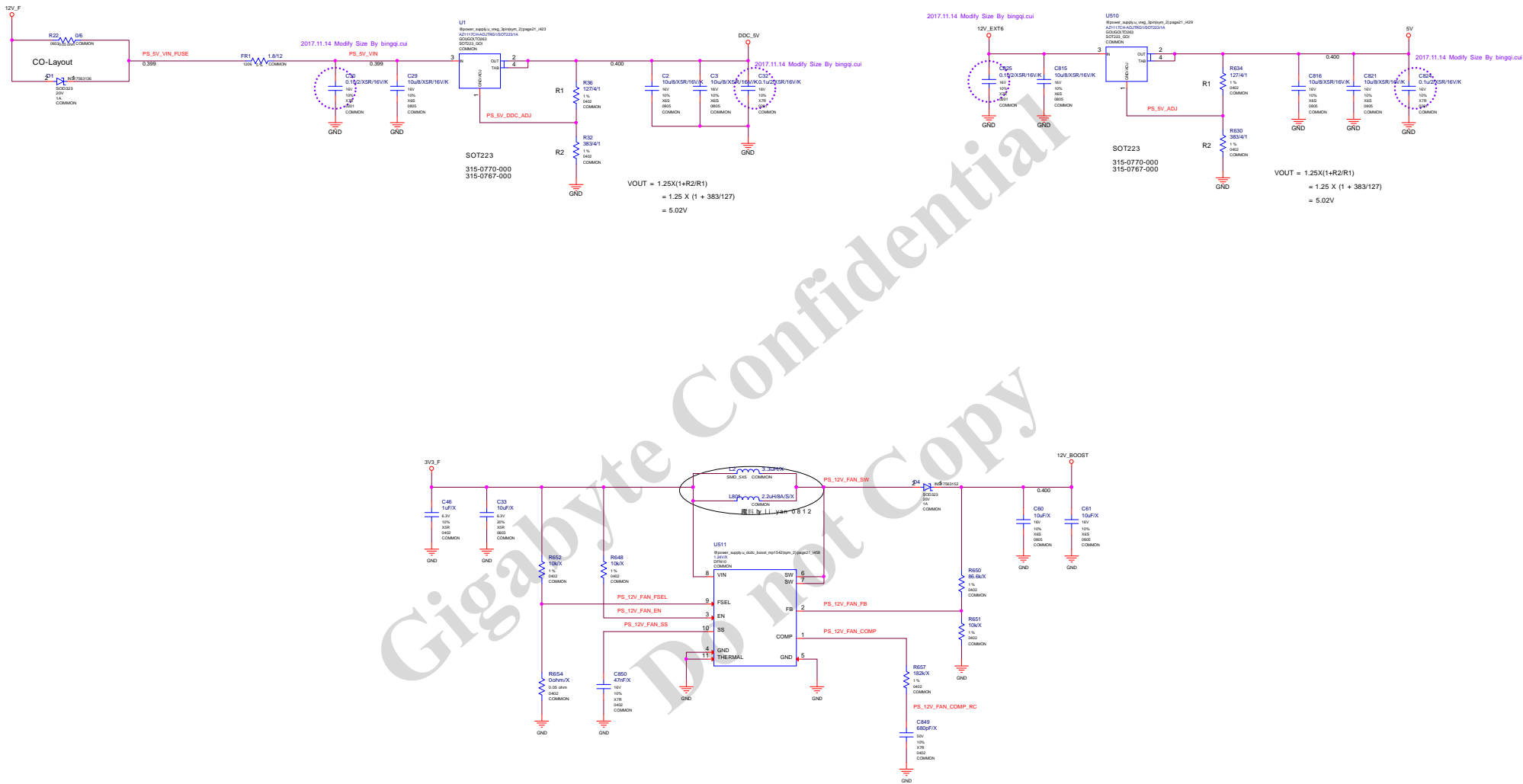


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PSI: 1V8

Title			
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Size	Document Number		Rev
Customer	GV-N1050C-2GD		1.11
Date:	Monday, January 29, 2018	Sheet	20 of 28

PSII:5V & 12V\_FAN

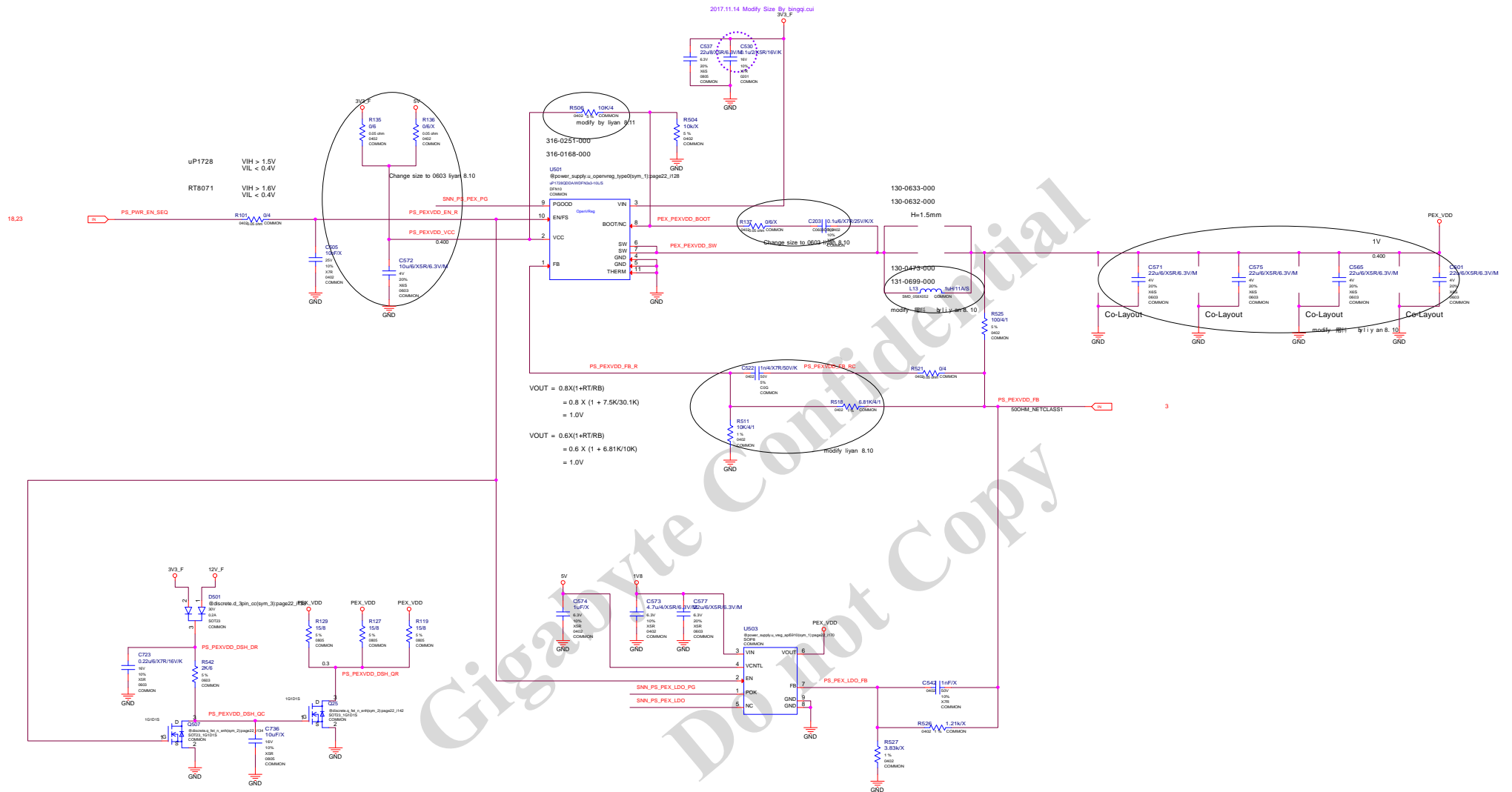


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PSII: 5V & 12V\_FAN

Title		5V & 12V_FAN
Size	Document Number	1.11
Date	Monday, January 25, 2018	Sheet 21 of 28

## PS III: PEXVDD



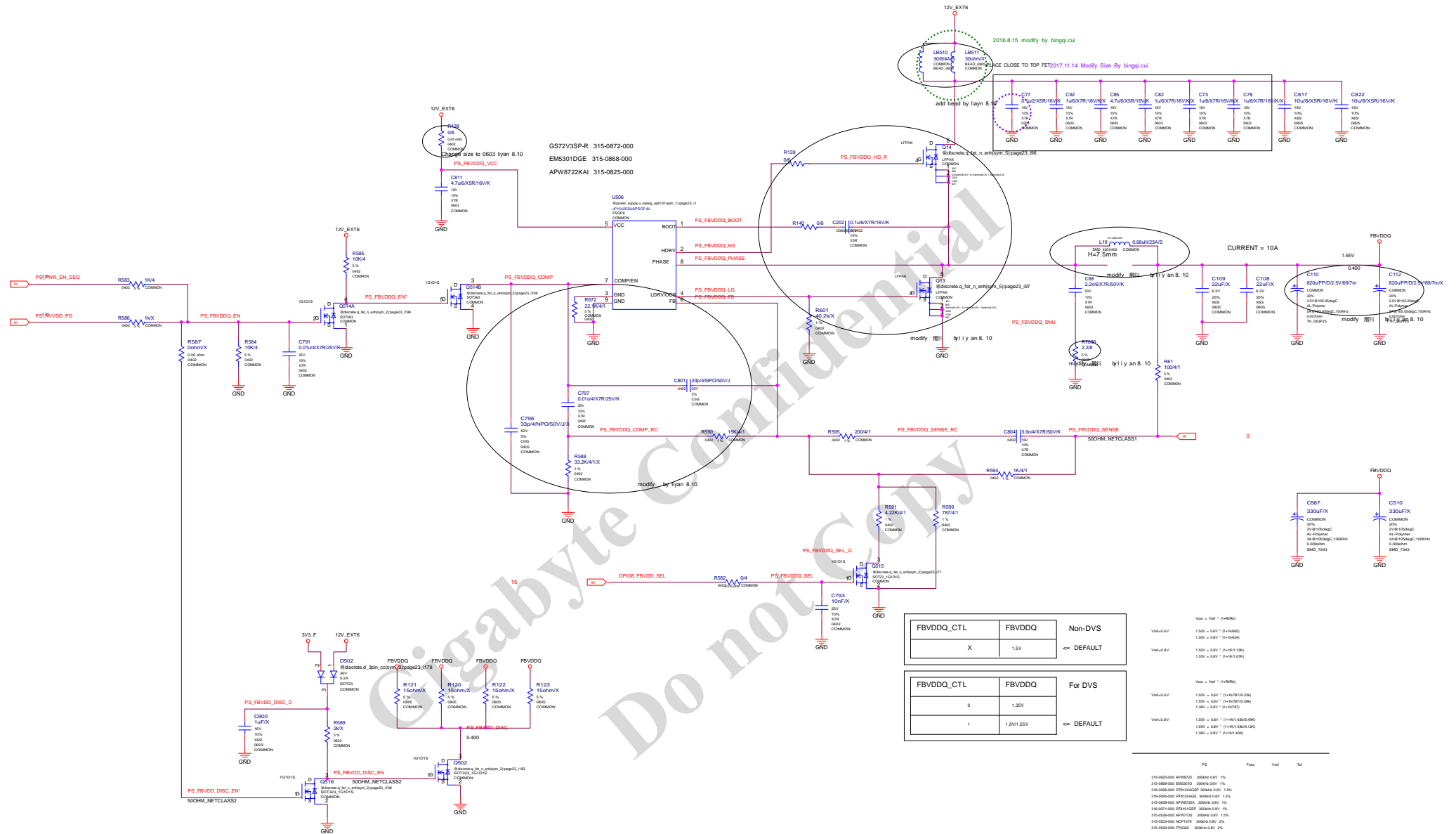
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PS III: PEXVDD

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PEXVDD			
Size	Document Number		Rev
Customer	GV-N1050OC-2GD		1.11
Date:	Monday, January 29, 2018	Sheet	22 of 28

## PS IV: FBVDDQ



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PAGE DETAIL	PS IV: FBVDDQ

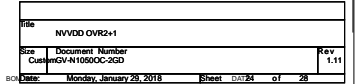
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FBVDDQ_CTL	FBVDDQ	For DVS
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1	1.5V/1.55V	=< DEFAULT

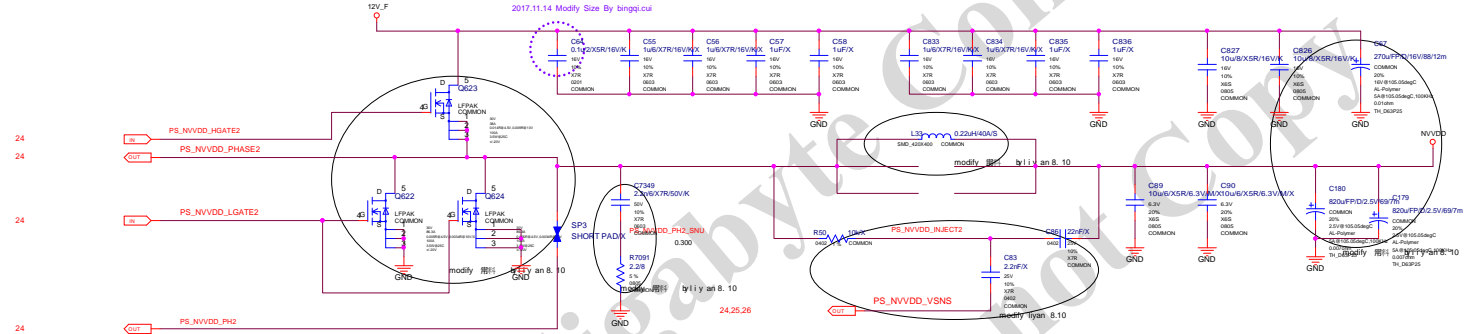
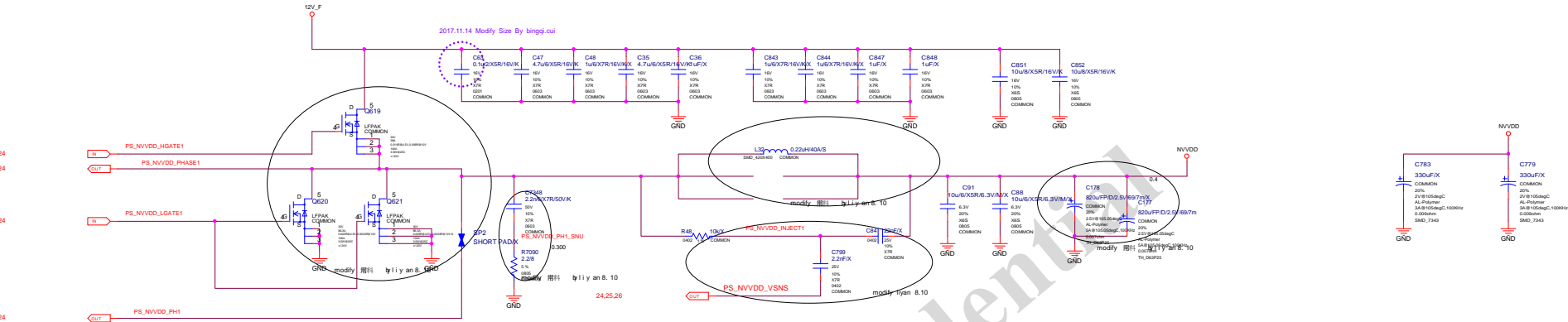
	$\text{Vint} = \text{Vint} * (\text{+N0R01})$
Vint0.0V	$1.00\text{V} = 0.0\text{V} * (\text{+N0R00})$ $1.00\text{V} = 0.0\text{V} * (\text{+N0R00})$
Vint0.1V	$1.00\text{V} = 0.0\text{V} * (\text{+N0R1130})$ $1.00\text{V} = 0.0\text{V} * (\text{+N0R1130})$
	$\text{Vint} = \text{Vint} * (\text{+N0R01})$
Vint0.2V	$1.00\text{V} = 0.0\text{V} * (\text{+N0R7074220})$ $1.00\text{V} = 0.0\text{V} * (\text{+N0R7074220})$ $1.00\text{V} = 0.0\text{V} * (\text{+N0R707})$
Vint0.3V	$1.00\text{V} = 0.0\text{V} * (\text{+N0R43005490})$ $1.00\text{V} = 0.0\text{V} * (\text{+N0R43005490})$ $1.00\text{V} = 0.0\text{V} * (\text{+N0R4300})$

Title			
FBVDDQ			
Size	Document Number		Rev
Customer	GV-N1050OC-2GD		1.11
Date:	Monday, January 29, 2018	Sheet	23 of 28





PS V: NVVDD Phase 1,2



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ASSEMBLY PAGE DETAIL  
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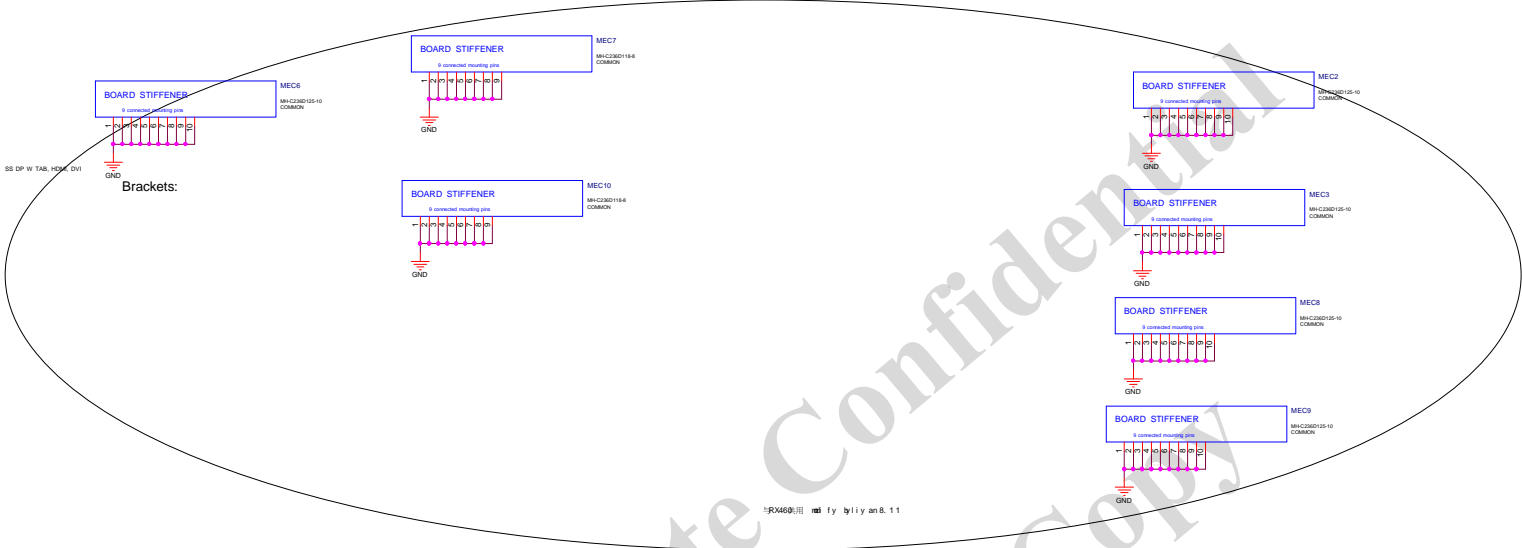
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Size	Document Number	Rev	1,11
Cust	Doc#	Rev	10860C-90D
Date:	Monday, January 29, 2018	Sheet	25 of 28



ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	PS V: NWDO Phase 3

Title			
NVVDD Phase 3			
Size	Document Number	Rev	
Customer	GV-N1050CC-2GD	1.11	
Date:	Monday, January 29, 2018	Sheet	28 of 28

Mechanical: Bracket/Thermal Solution



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ASSEMBLY  
PAGE DETAIL

ASSEMBLY DESCRIPTION  
MECH: Bracket/Thermal

Title		
Bracket/Thermal Solution		
Doc	Document Number	Rev
Customer	2V-N1050C-2GD	1.11
Date:	Monday, January 29, 2018	Sheet 27 of 28

