

V091-20 Bason on P402-A02 DESIGN -- G84/G86, 600/700 128/256 MB DDR3, VGA, DVI-I, SD/HDTV

REV	VARIANT	NVPN	ASSEMBLY
0	BASE	600-10402-0aaa-ich	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10402-0000-200	G84-300, 600/700MHz 256MB 18Mx32 BGA135 GDDR3 DVI+HDTV+Out
2	SKU0010	600-10402-0010-200	G84-400-600/700MHz 256/128 MB 18Mx32 BGA135 GDDR3 DVI+VGA_HDTV+Out
3	SKU0020	600-10402-0020-200	G84-875, 600/700MHz 256MB 18Mx32 BGA135 GDDR3 DVI+HDTV+Out
4	SKU0100	600-10402-0100-200	G84-300, 600/700MHz 256MB 18Mx32 BGA135 GDDR3 DVI+HDTV+Out
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Page 20: POWER SUPPLY: 5V, TMDSIOVDD, PEX1V2 AND FBVDDQ SWITCHER  
Page 21: POWER SUPPLY: SINGLE PHASE NVVDD, NVVDD SET CONTROL

V091-20

1. Page 20, 21 Modify FBVDDQ and NVVDD power circuit  
2. Page 19 co-layout TMDS\_PLLVDD power circuit  
3. Page 11, 12 add EMI TMDS circuit  
4. Page 16 fan 2pin modify 3pin

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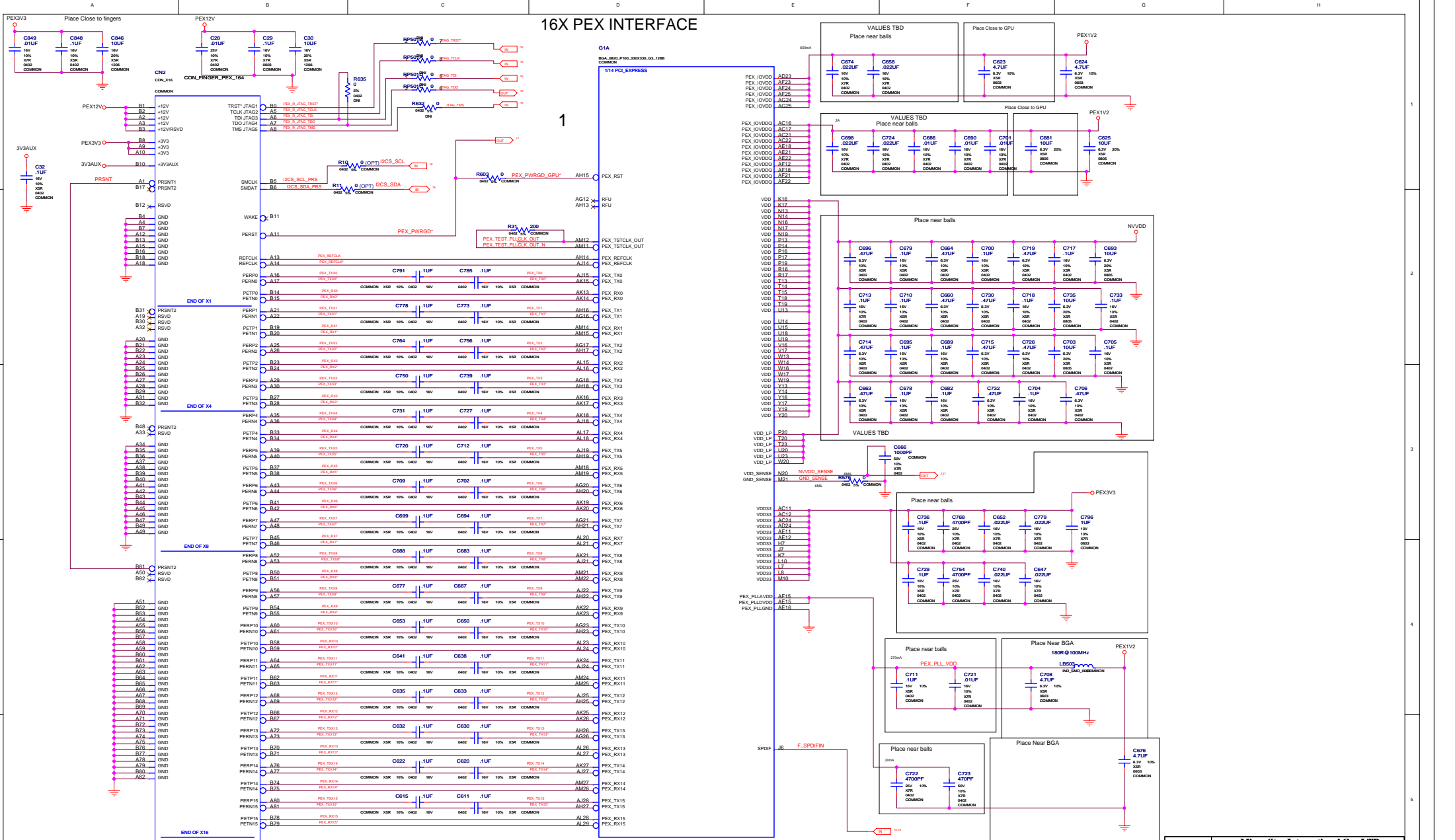
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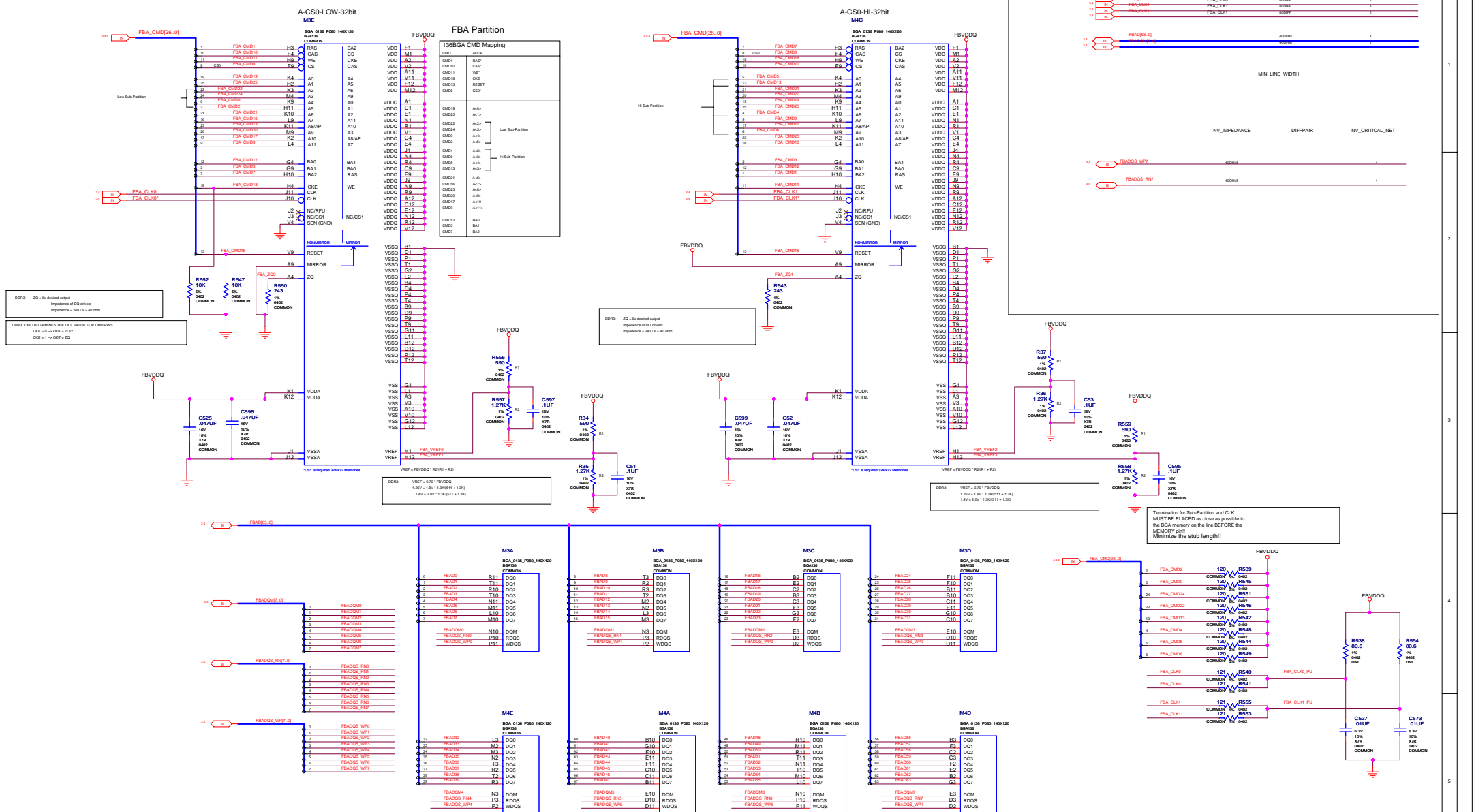
Date: Wednesday, April 05, 2006 Sheet: 1 of 1

# 16X PEX INTERFACE



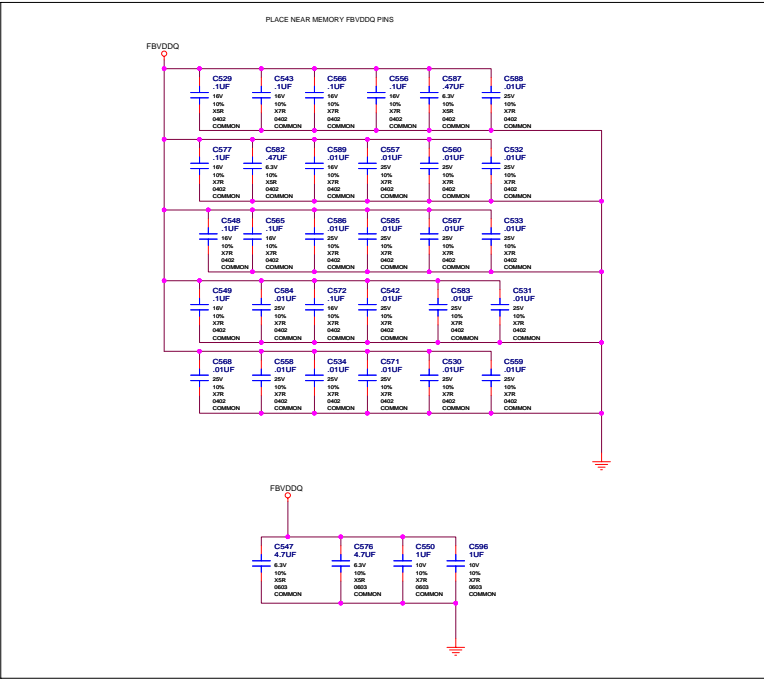


Framebuffer: Partition A 8Mx32 BGA136 DDR3

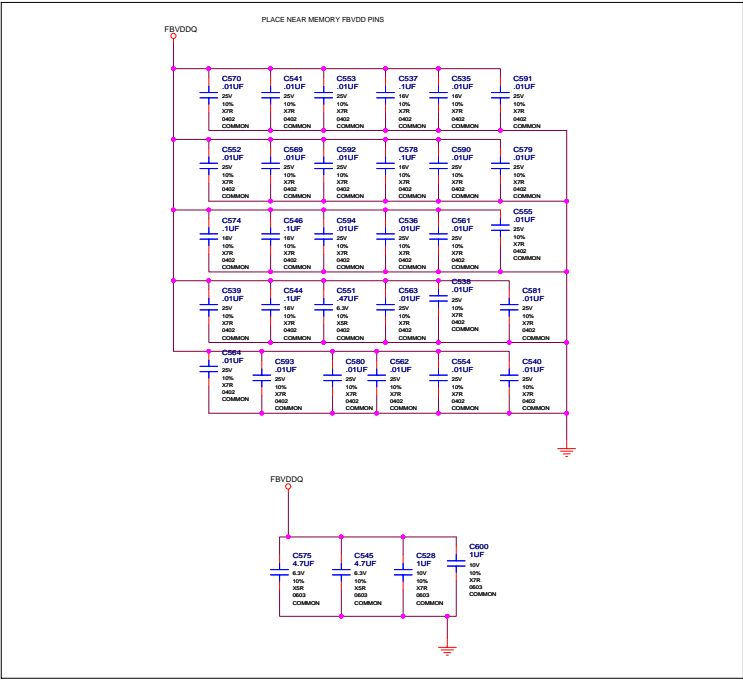


FRAME BUFFER: PARTITION A DECOUPLING

Decoupling for FBA 0..31




Decoupling for FBA 32..63



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ASSEMBLY PAGE DETAIL  
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FBA MEMORY FBVDDQ DECOUPLING CAPS

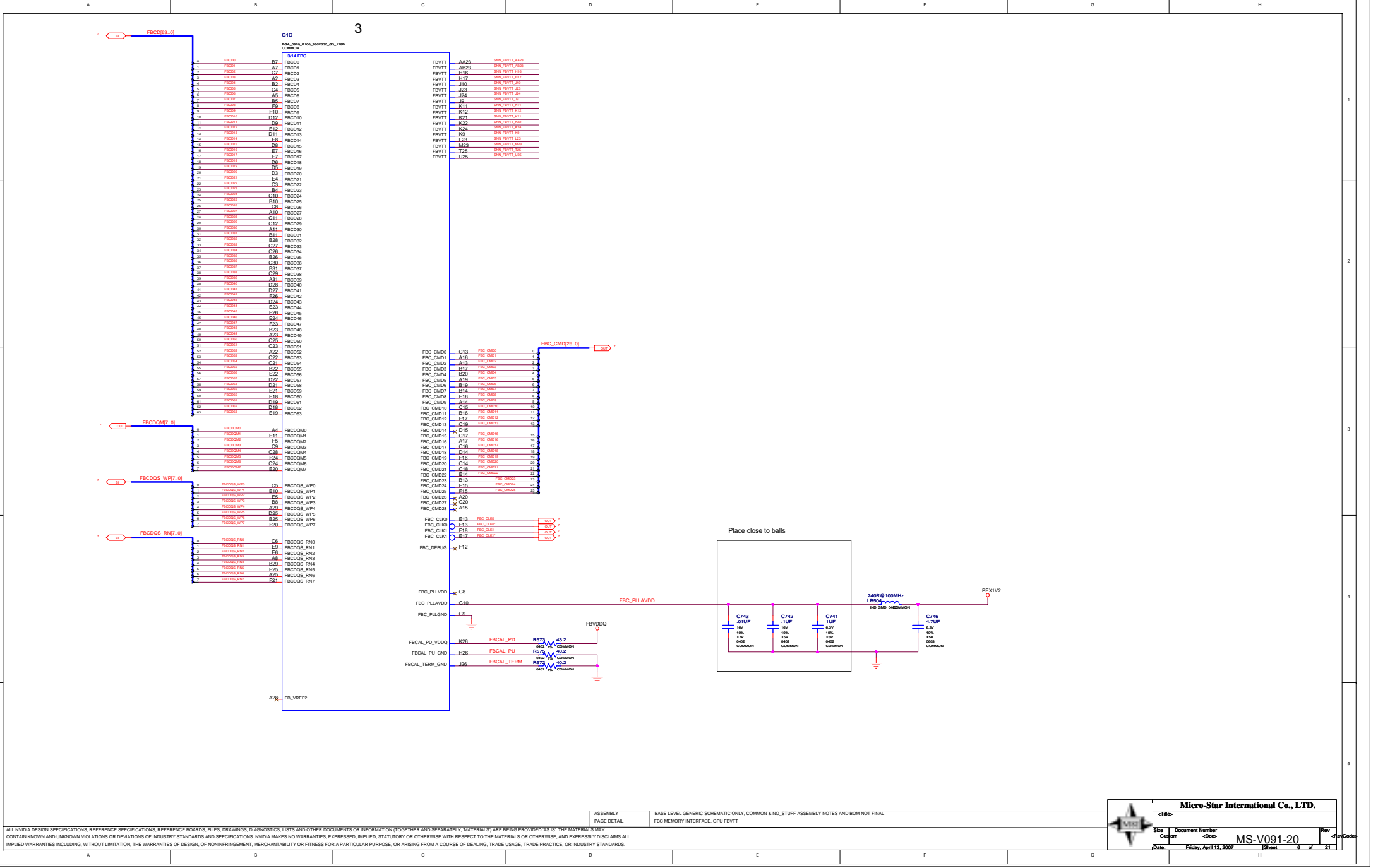


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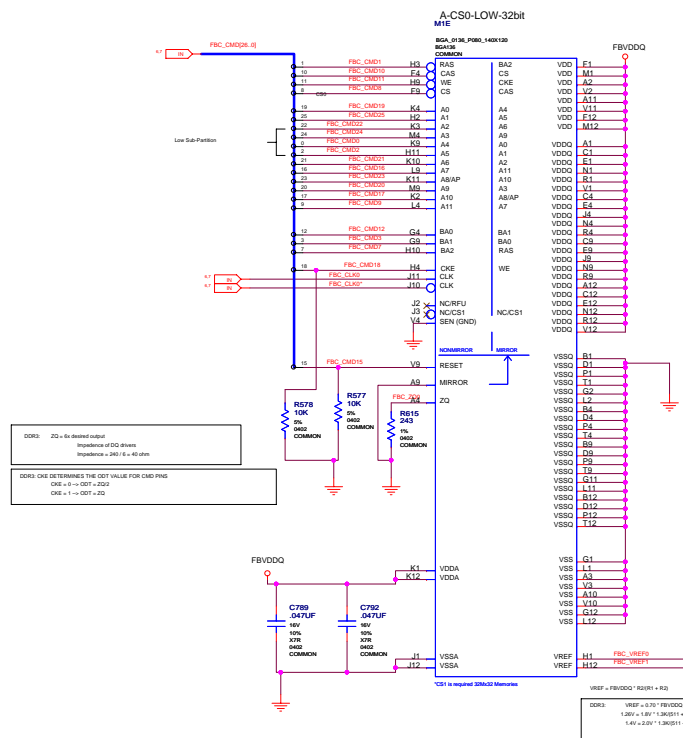
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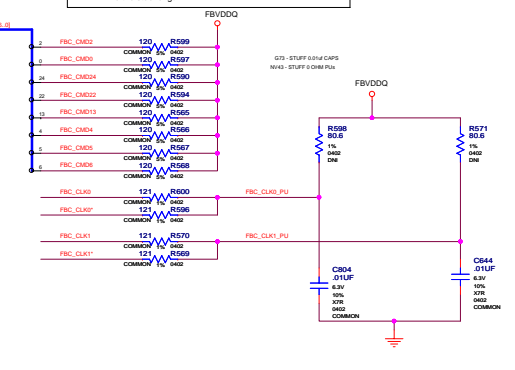
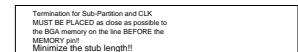
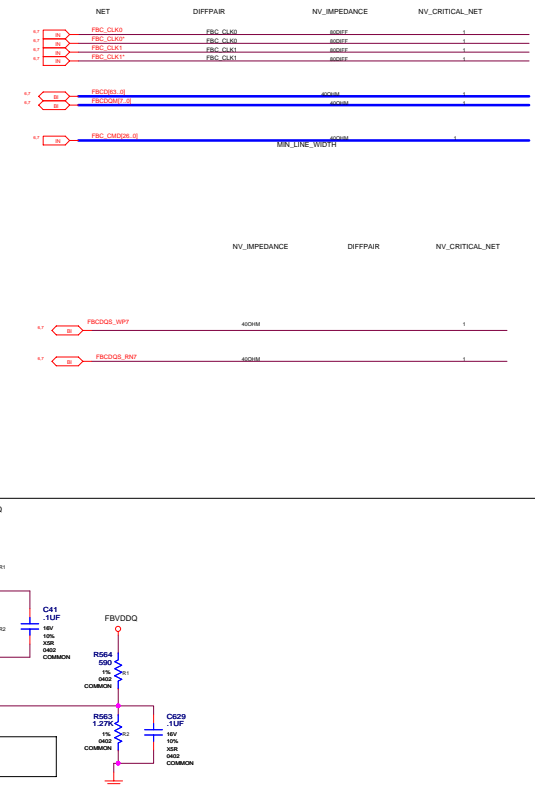
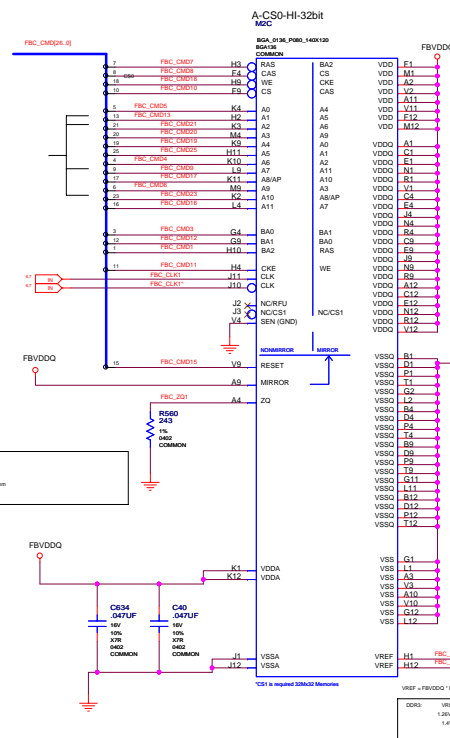
Date Monday, April 16, 2007 Sheet 6 of 21



FRAMEBUFFER: PARTITION C 8Mx32 BGA136 DDR3



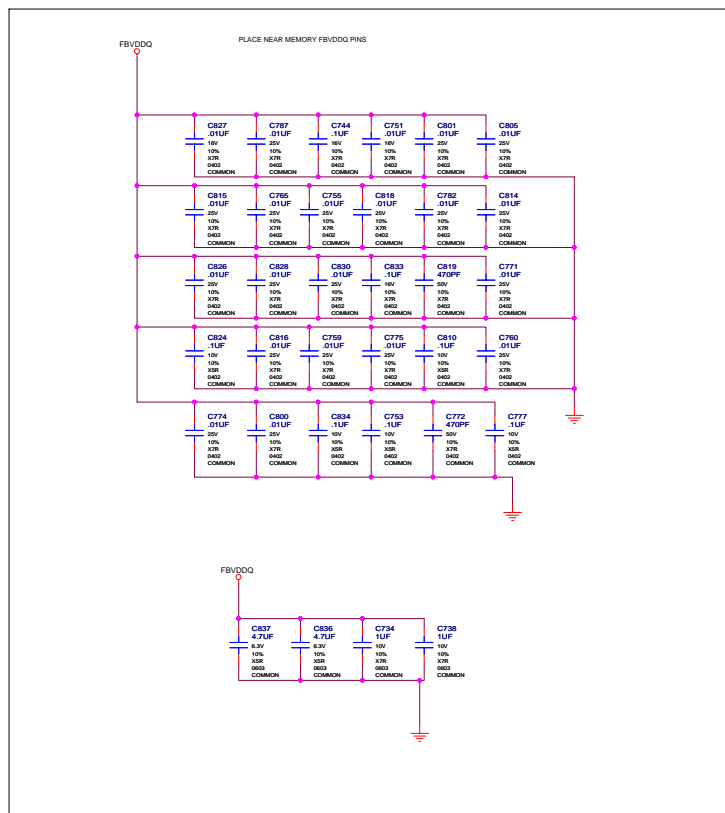
1366GA CMD Mapping	
CMD	ADDR
CMD1	BA0*
CMD10	CAS*
CMD11	WE*
CMD18	OE
CMD19	RESET
CMD8	CS*
CMD19	A-0
CMD20	A-1
CMD22	A-2
CMD24	A-3
CMD28	A-4
CMD2	A-5
CMD4	A-6
CMD5	A-7
CMD6	A-8
CMD13	A-9
CMD21	A-10
CMD26	A-11
CMD23	A-8
CMD29	A-10
CMD17	A-11
CMD9	A-11
CMD12	BA0
CMD3	BA1
CMD7	BA2



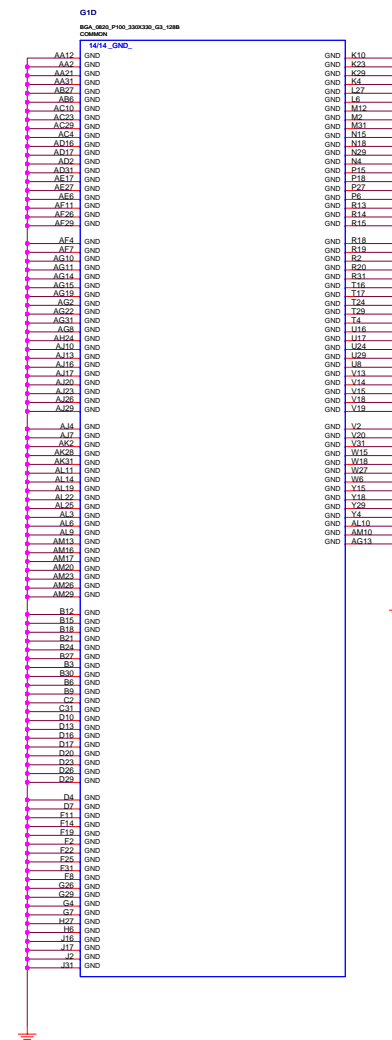
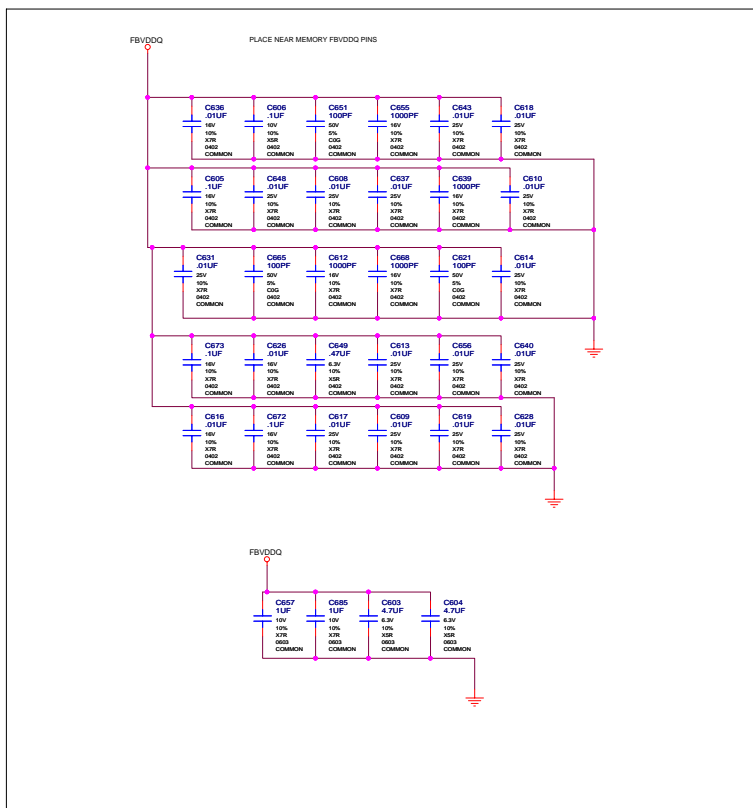
## FRAMEBUFFER: PARTITION C DECOUPLING

14

## Decoupling for FBC 0..31



## Decoupling for FBC 32..63



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS, GPU GND CONNECTIONS



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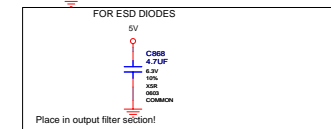
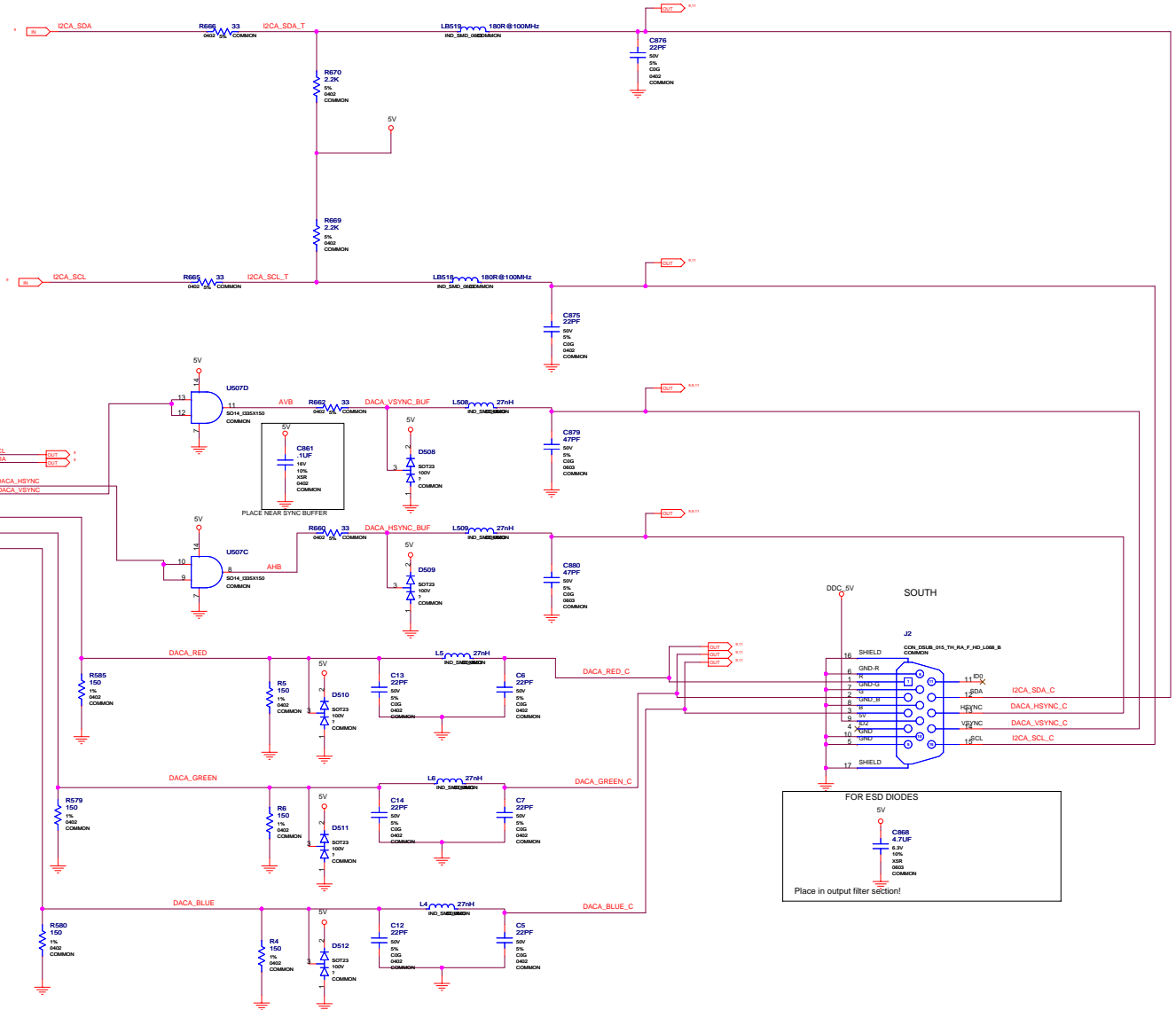
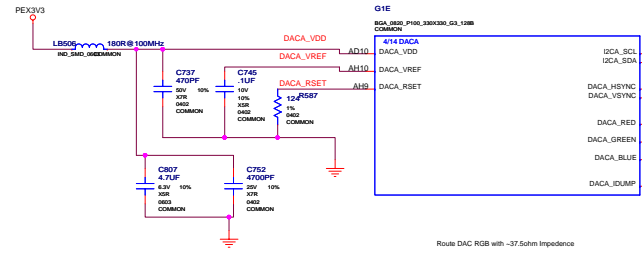
Date: Monday, April 16, 2007 Sheet 8 of 21

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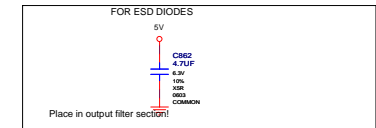
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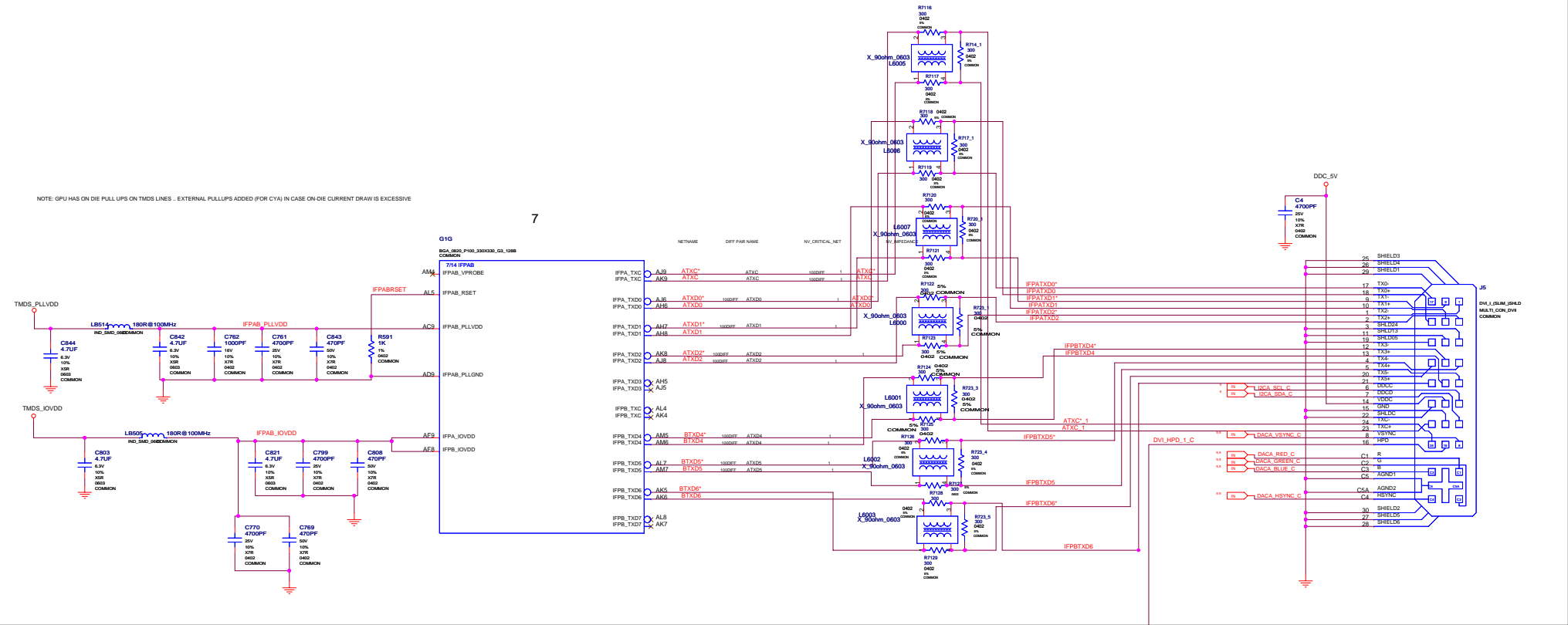
## DACC RGB-FILTER



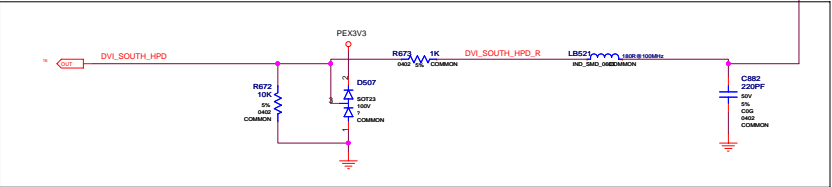
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Date:	Thursday, April 12, 2007	Sheet	10 of 21

INTERNAL TMDS .. LINK A & B

NOTE: GPU HAS ON DIE PULL UPS ON TMDS LINES - EXTERNAL PULLUPS ADDED (FOR CIVA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE



Hotplug Detection

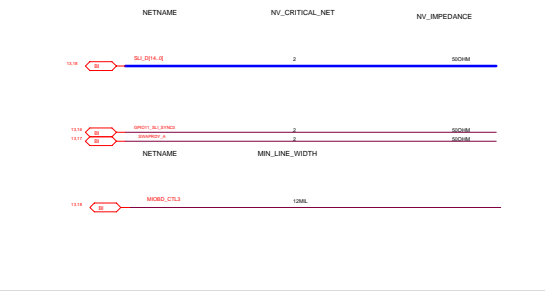
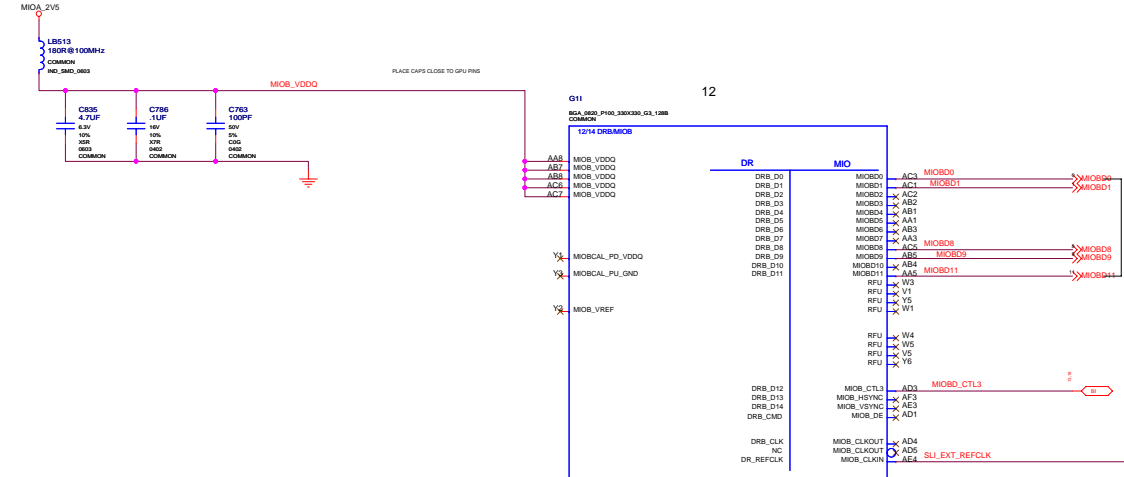


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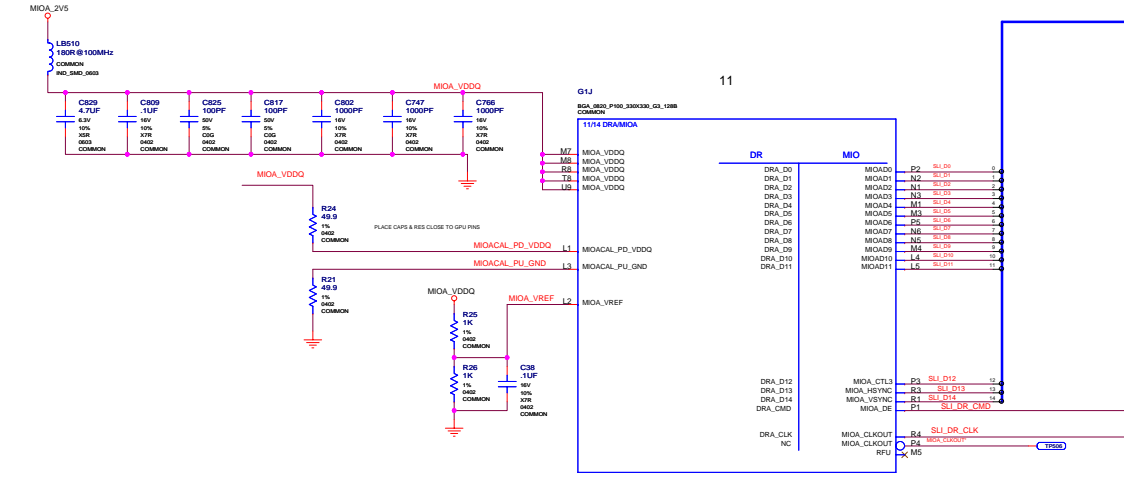
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MAX LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL  
TMDS LINK A/B & P/LA, TMDS IO BACKDRIVE PREVENTION/DVI CONNECTOR SOUTH



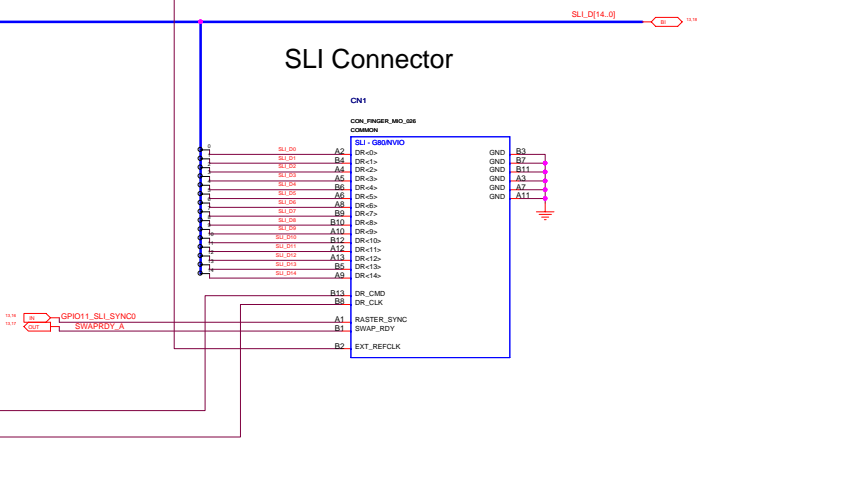
G3 VIP/MIOB



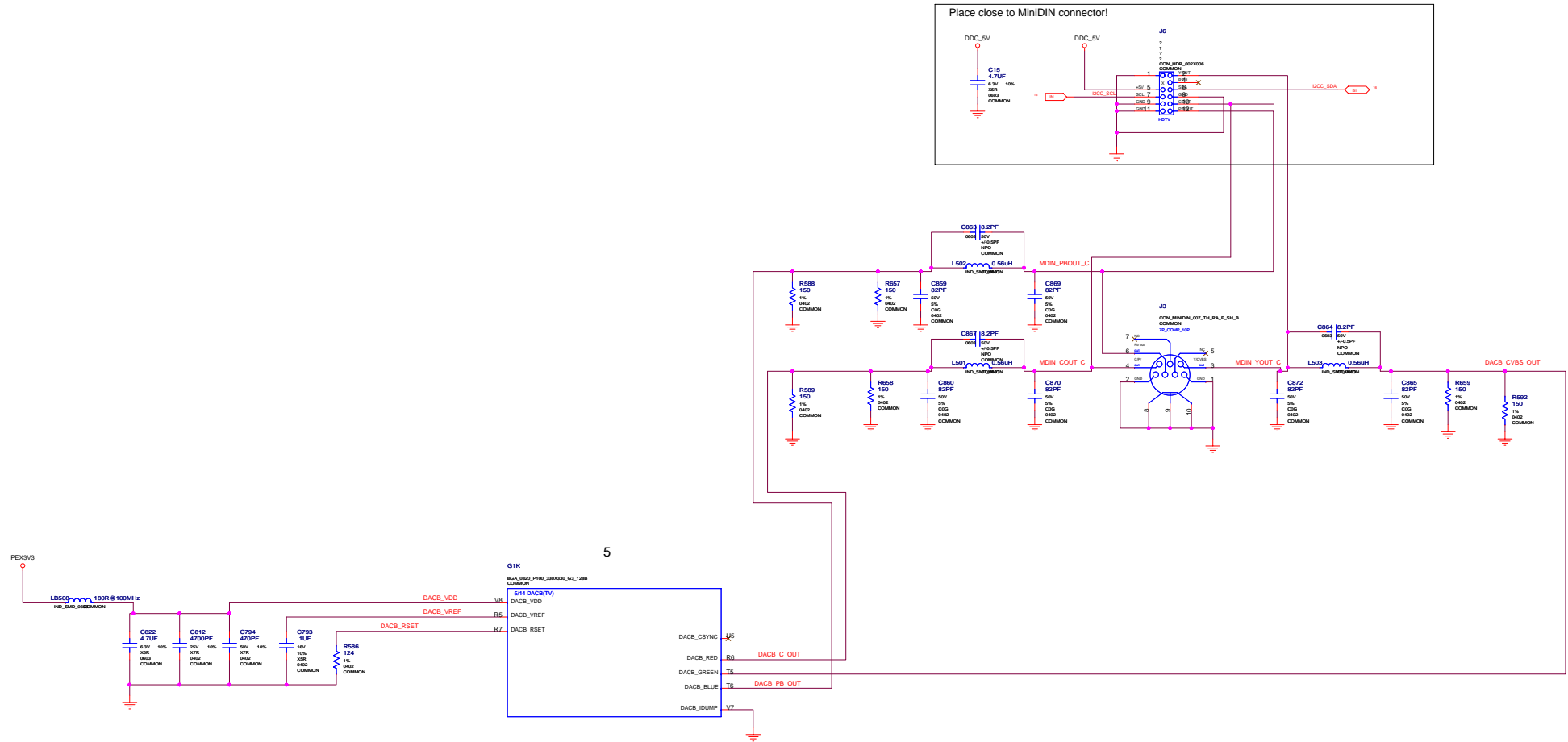
G3 MIOA



SLI Connector



## DACB .. MiniDIN VIDEO OUT CONNECTOR



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, MINIDIN CONNECTOR NORTH, COMPONENT VIDEO OUTPUT CONNECTOR



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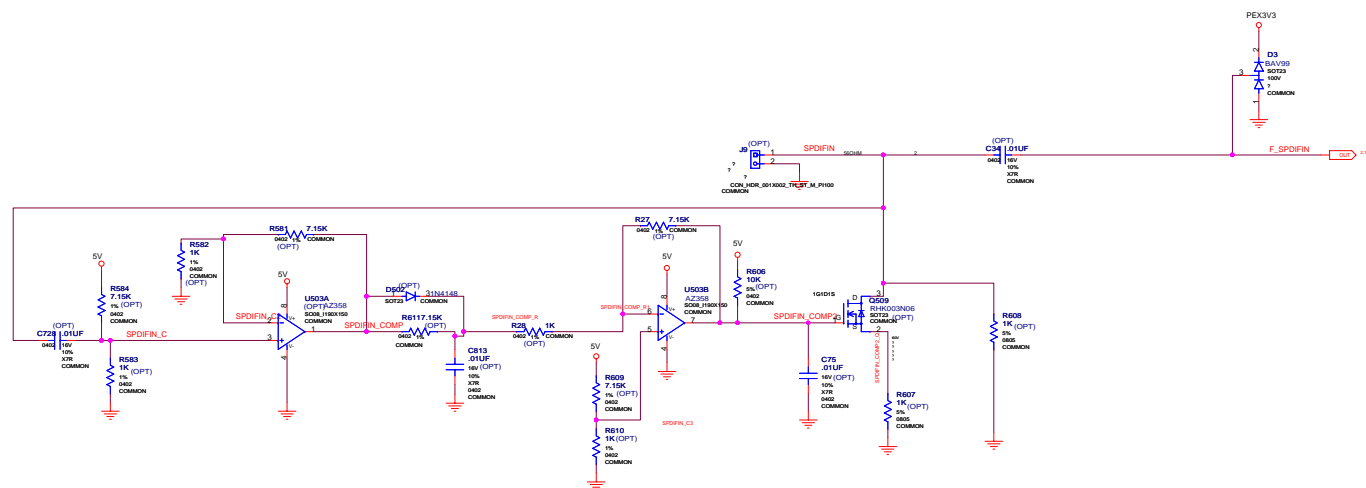
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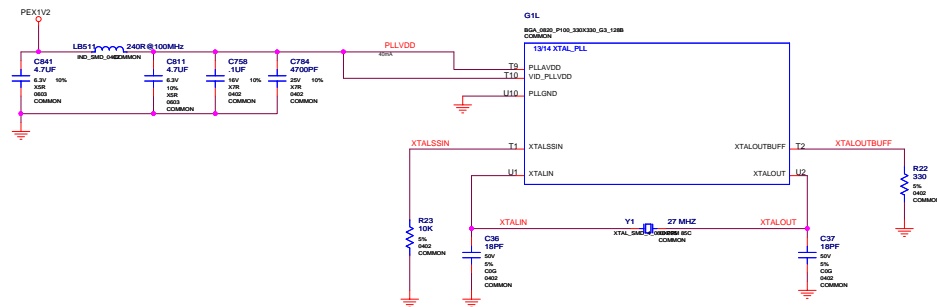
## XTAL/PLLVDD/SPDIF IN

## SPDIF IN

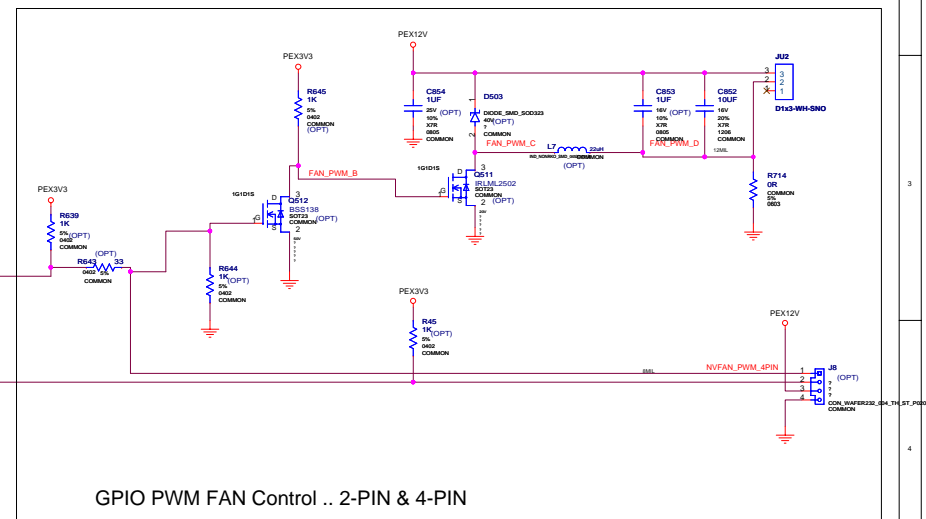


## XTAL/PLLVDD

13



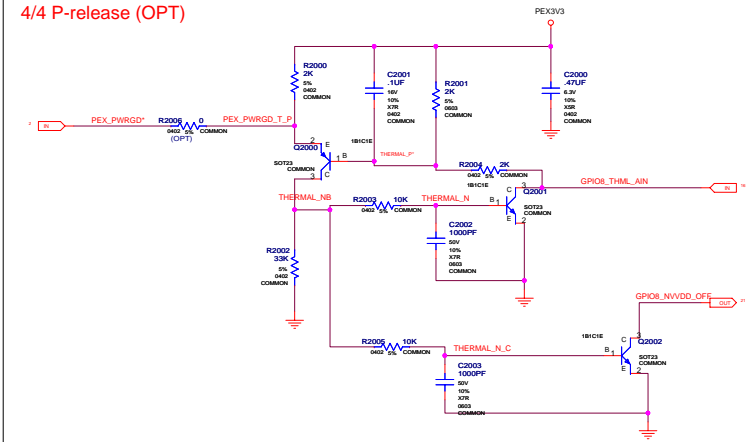
2.15 IN F\_SPOFIN SECHM 2



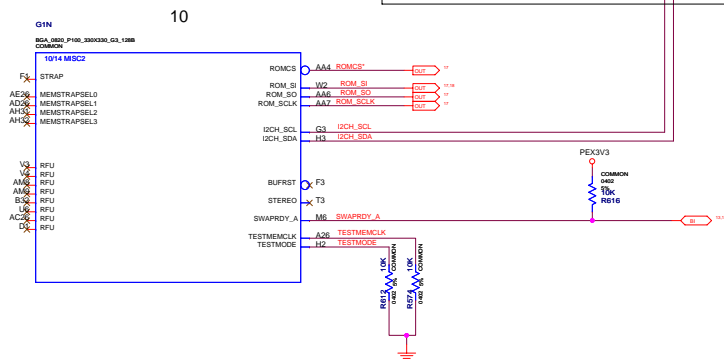
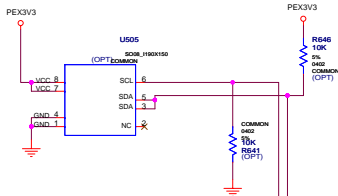
GPIO	IO	FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	DVI SOUTH HOTPLUG DET
2	IN/OUT	RESERVED
3	IN	OSM THERMAL ODS IN
4	IN	FAN TACH
5	OUT	NRVDD VOLTAGE SELECT 0
6	OUT	NRVDD VOLTAGE SELECT 1
7	OUT	RESERVED
8	IN	THERMAL ALERT IN
9	OUT	PWM FAN
10	OUT	RESERVED
11	OUT	SU-11VDD
12	OUT	RESERVED
13	IN	RESERVED
14	IN	RESERVED



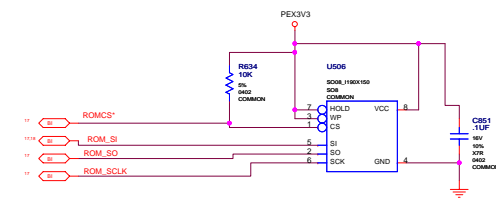
## Thermal Protection



## HDCP ROM (serial)



## BIOS ROM(serial)

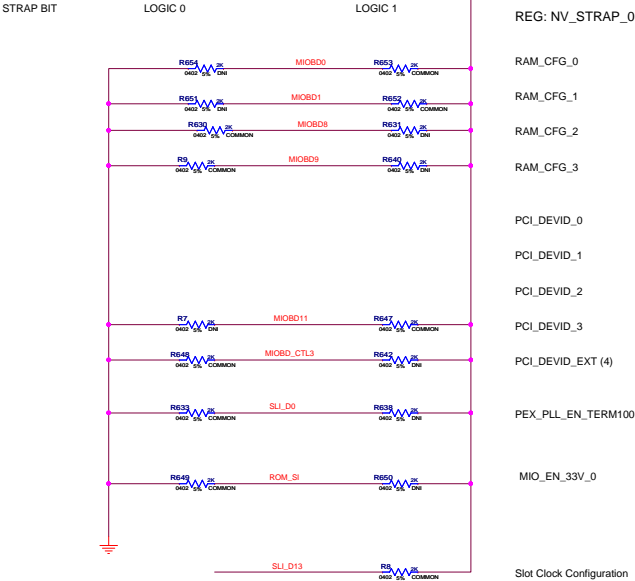
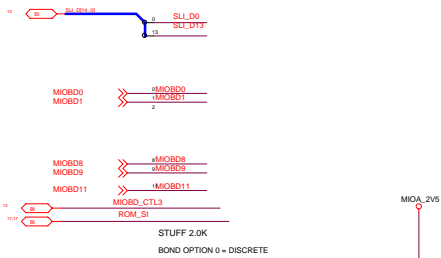


SRAM MAPPING	
ROM	NW4/G73
SO	ROM_SO
SI	ROM_SI
SCK	ROM_SCK
CS*	ROM_CS*

BIOS, Straps, Misc

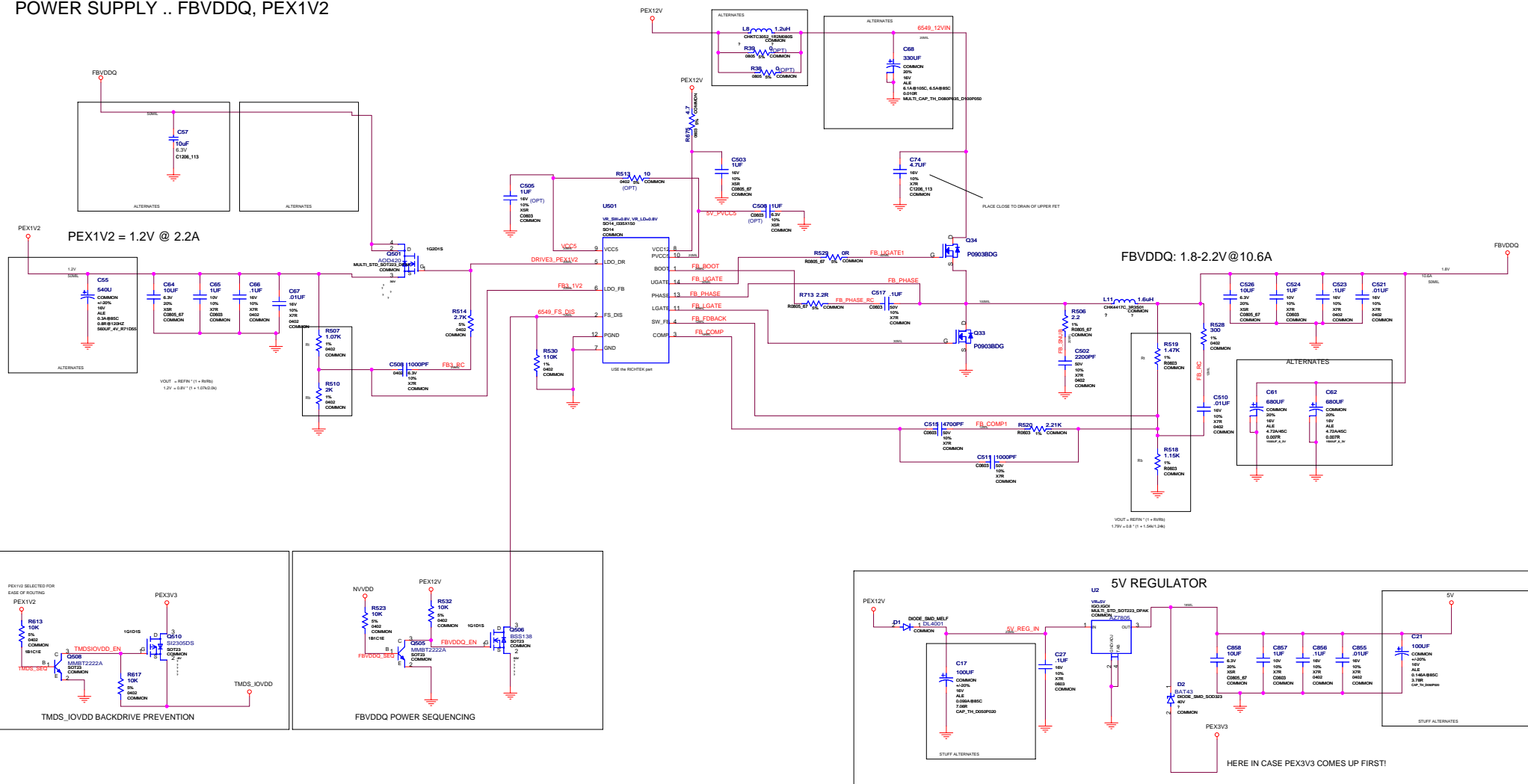
STRAPS

Assembly: BIOS





## POWER SUPPLY .. FBVDDQ, PEX1V2



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: 5V, TMSIOVDD, PEX1V2 AND FBVDDQ SWITCHER



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