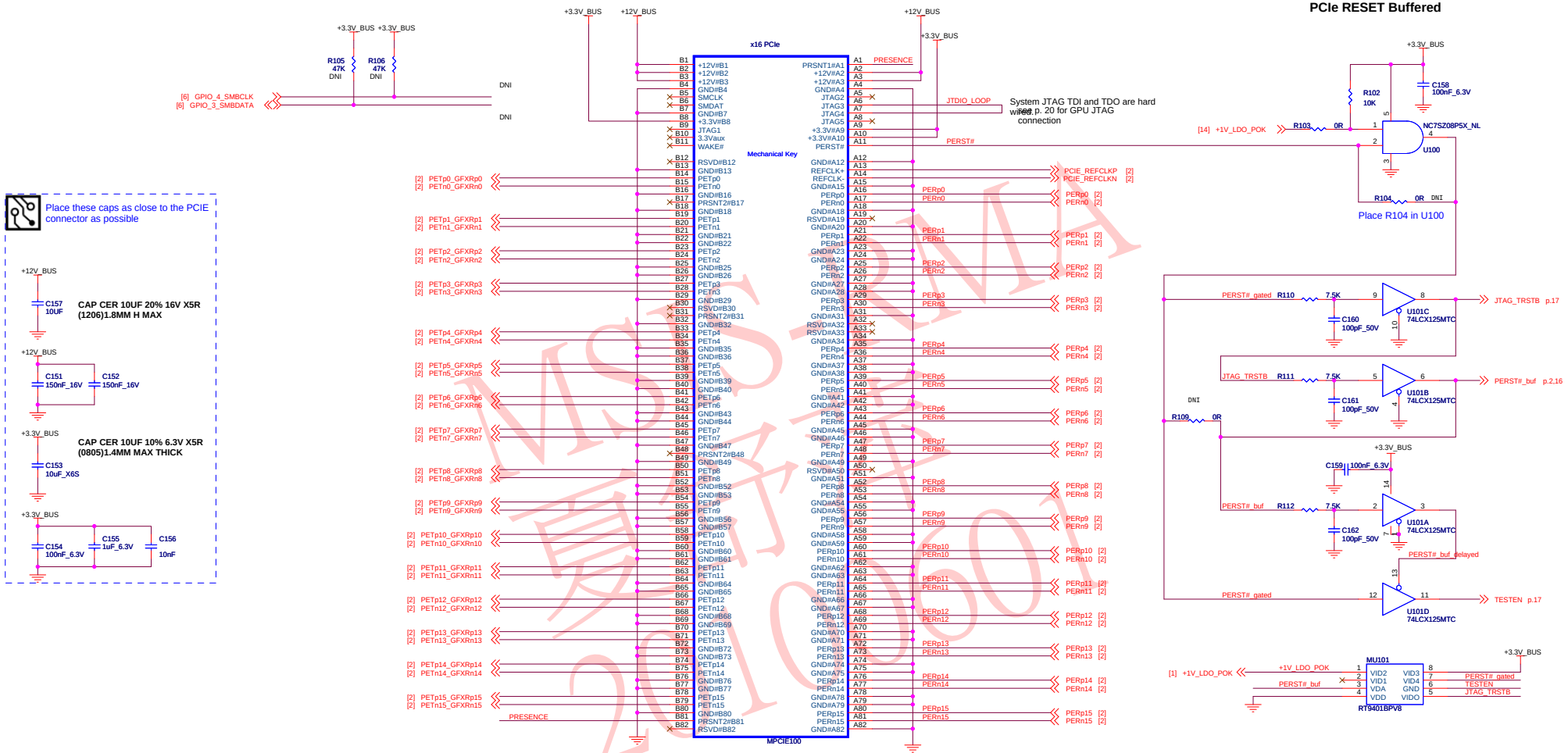
PCI-EXPRESS EDGE CONNECTOR

REDWOOD
WOLVERINE



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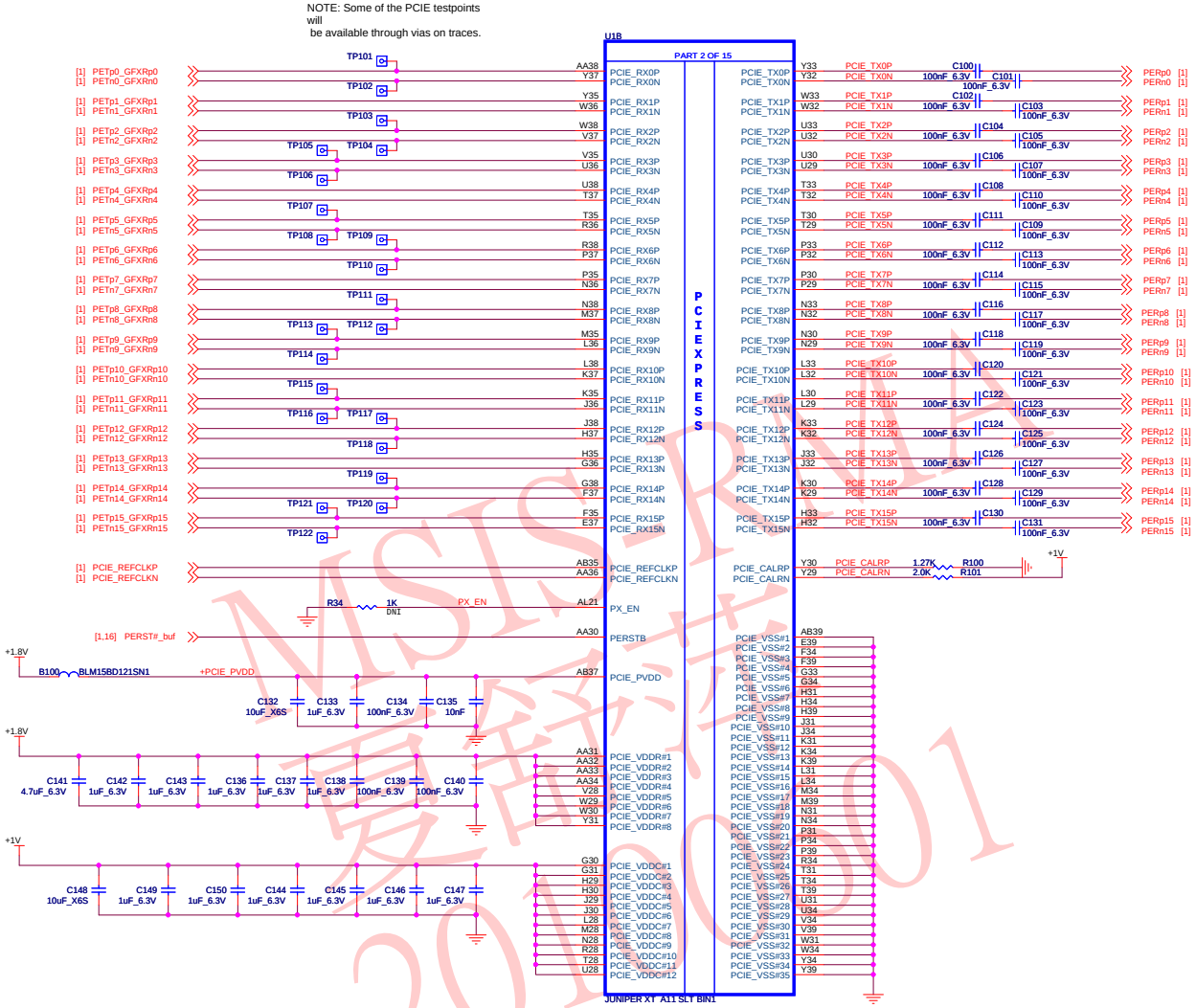
(2) REDWOOD PCIe Interface



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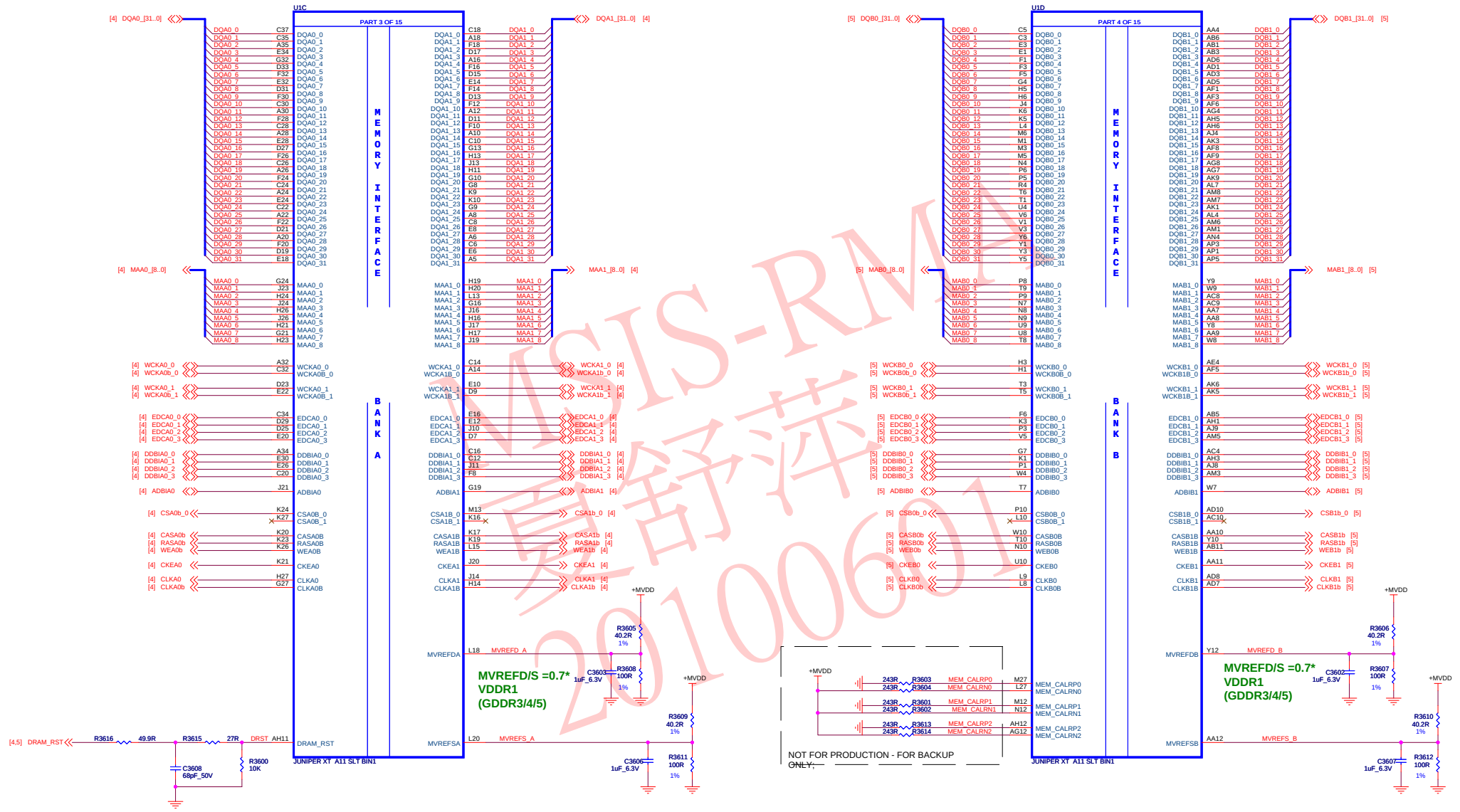
(3) REDWOOD MEM Interface Ch A&B



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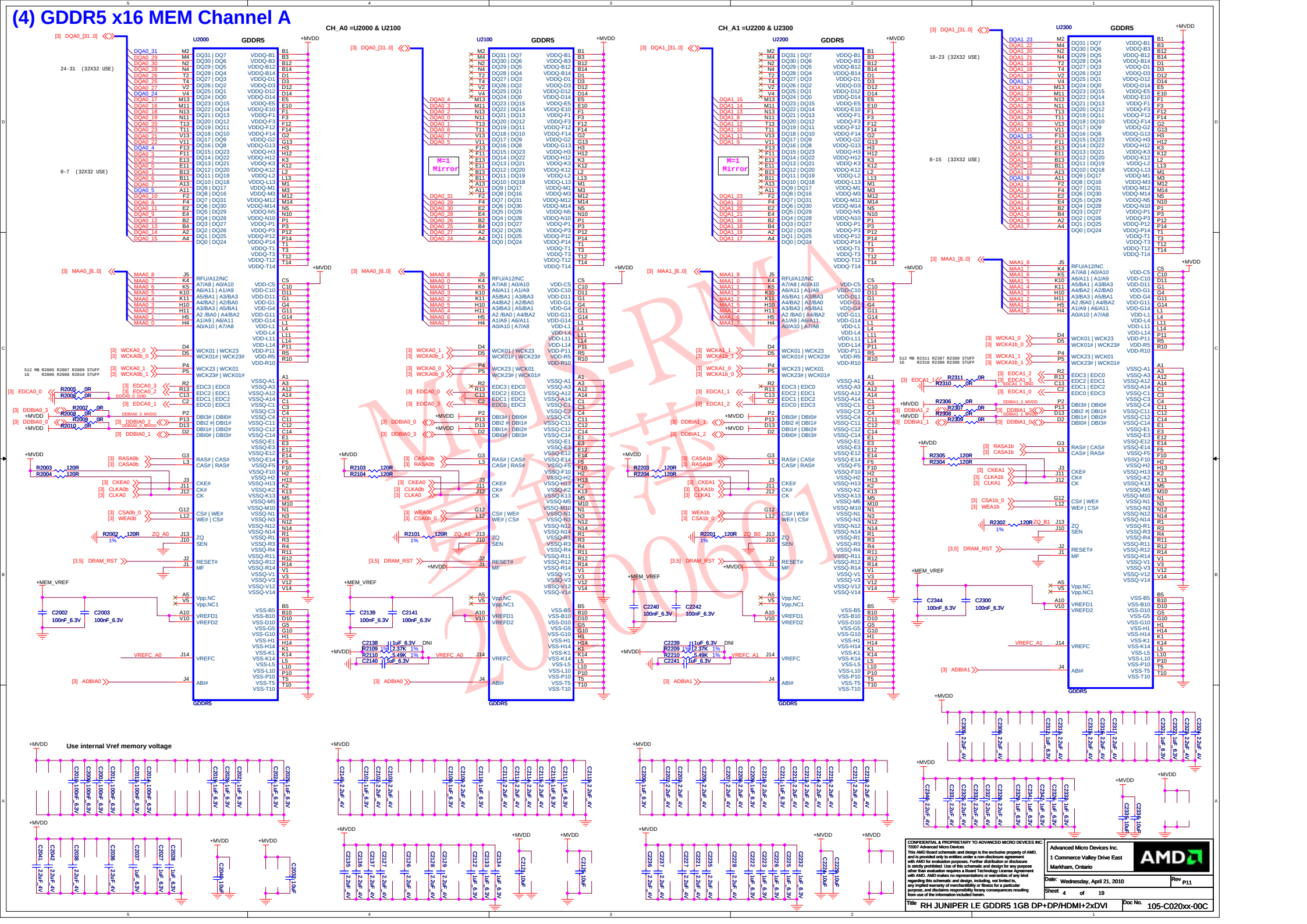
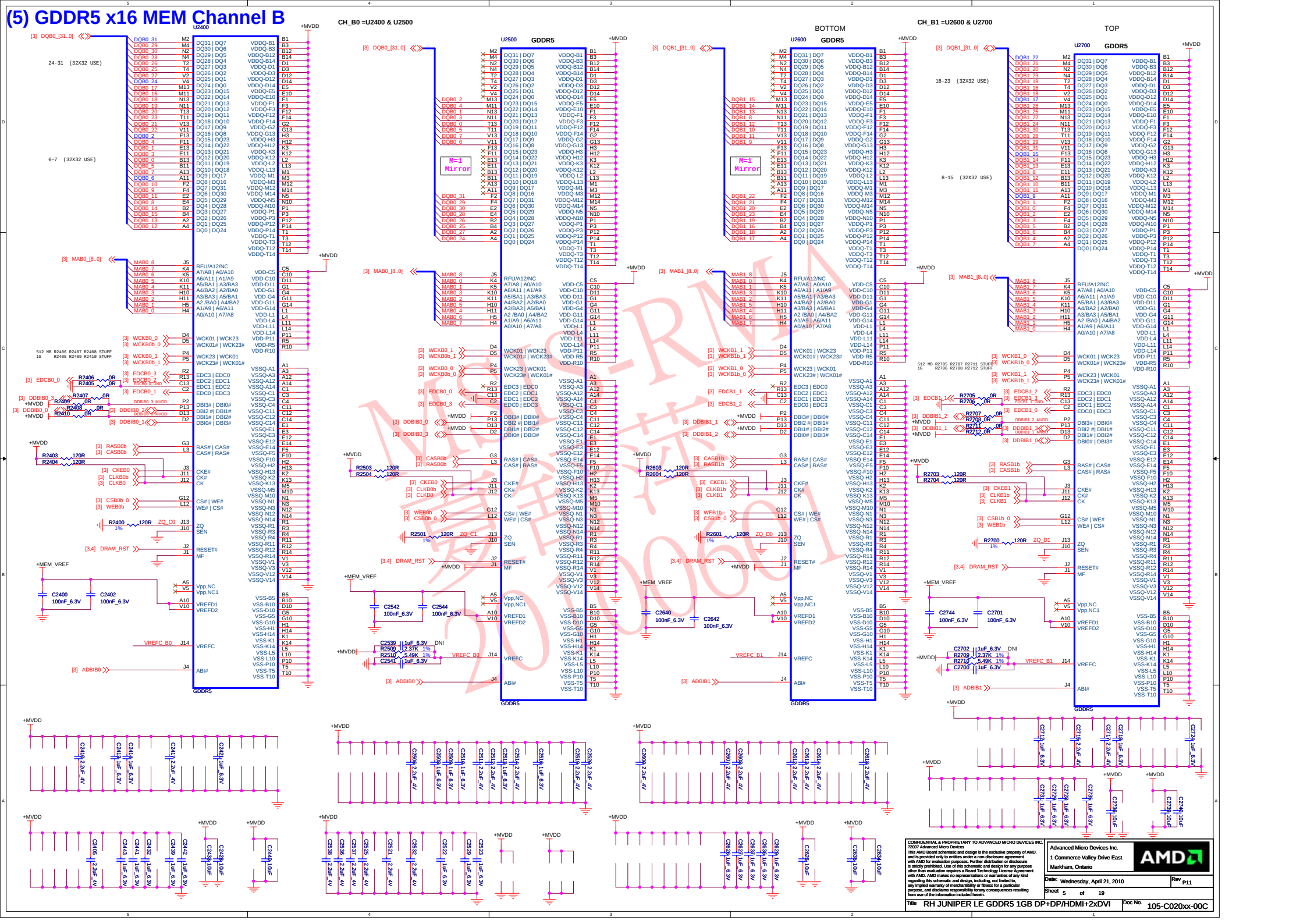
(4) GDDR5 x16 MEM Channel A



(5) GDDR5 x16 MEM Channel B



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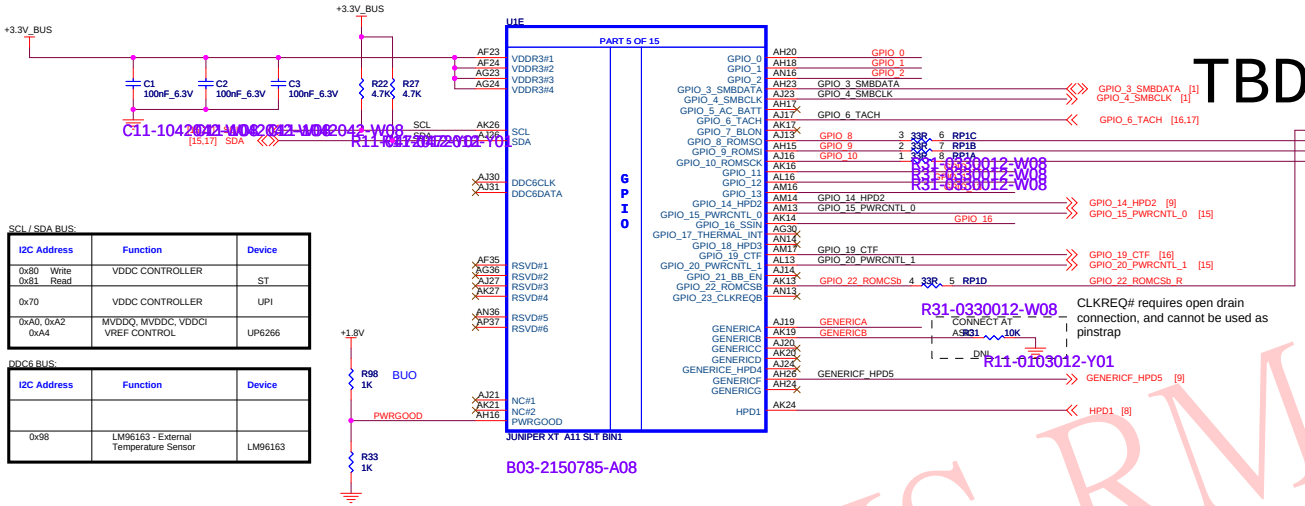
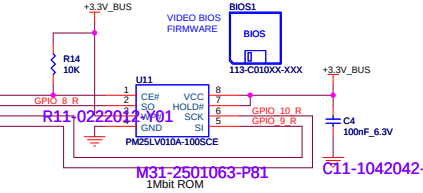
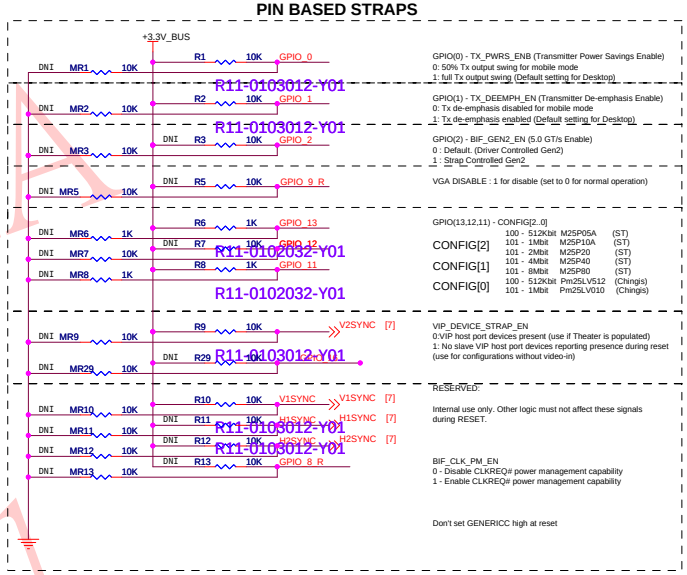
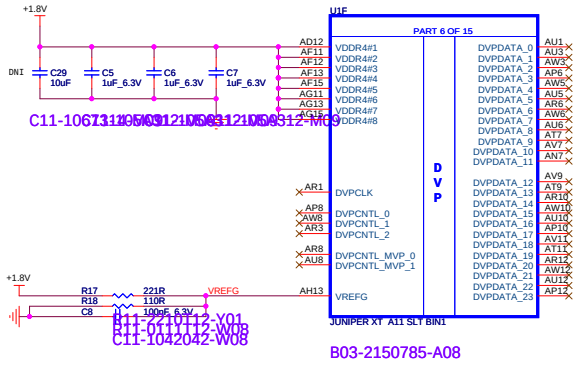
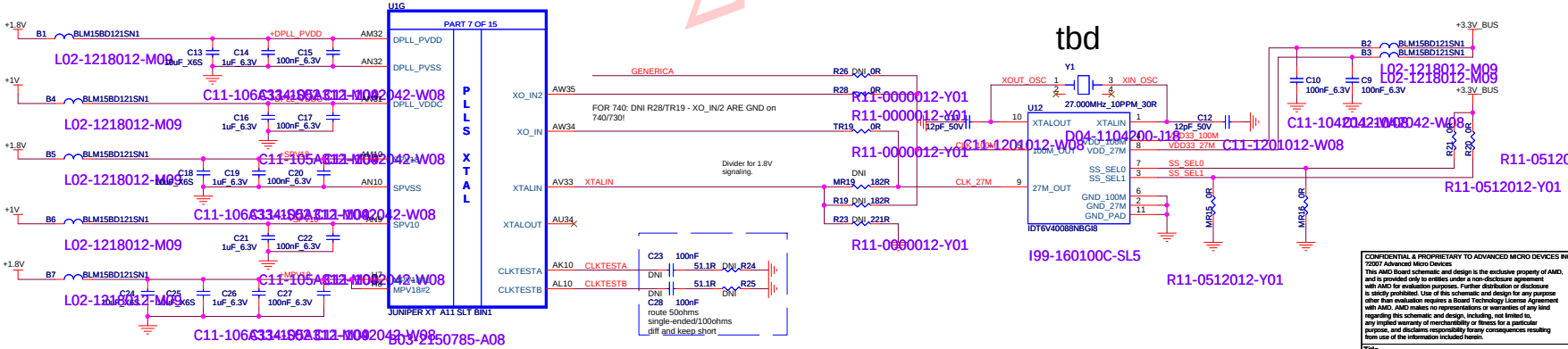
(06) REDWOOD GPIOs Strap CF XTAL OSC











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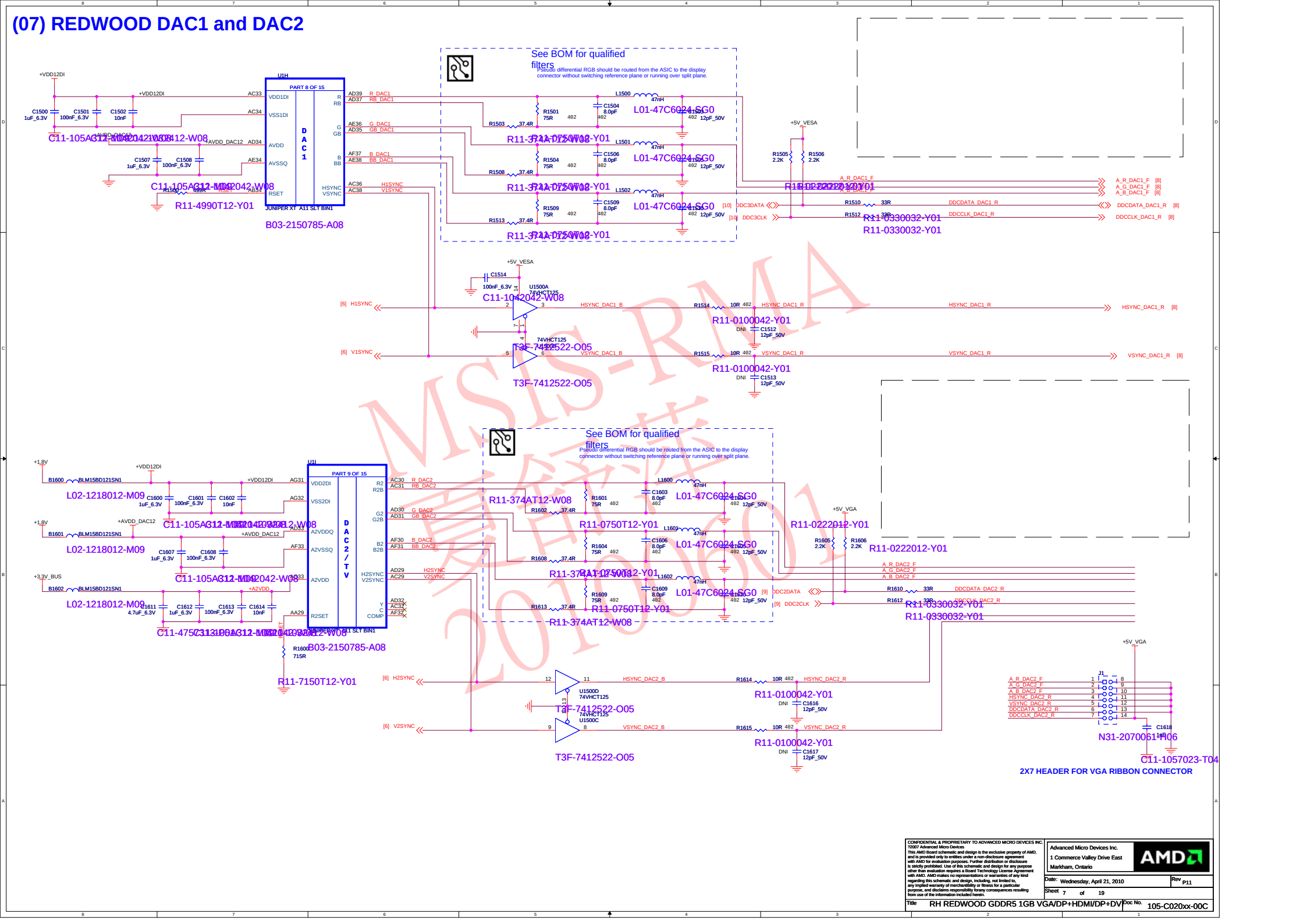
(07) REDWOOD DAC1 and DAC2



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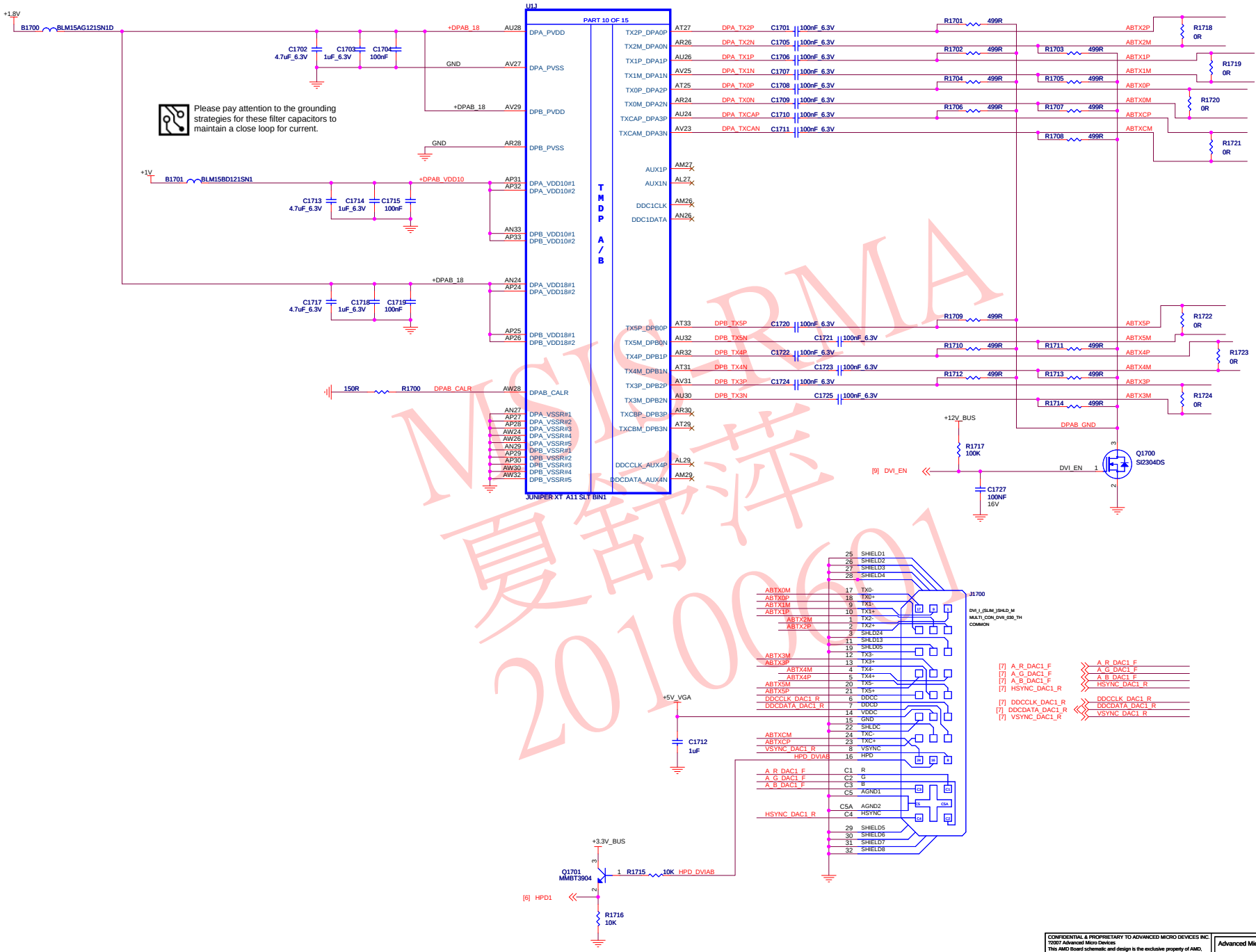
(08) REDWOOD TMDP A&B dDVI-I TOP



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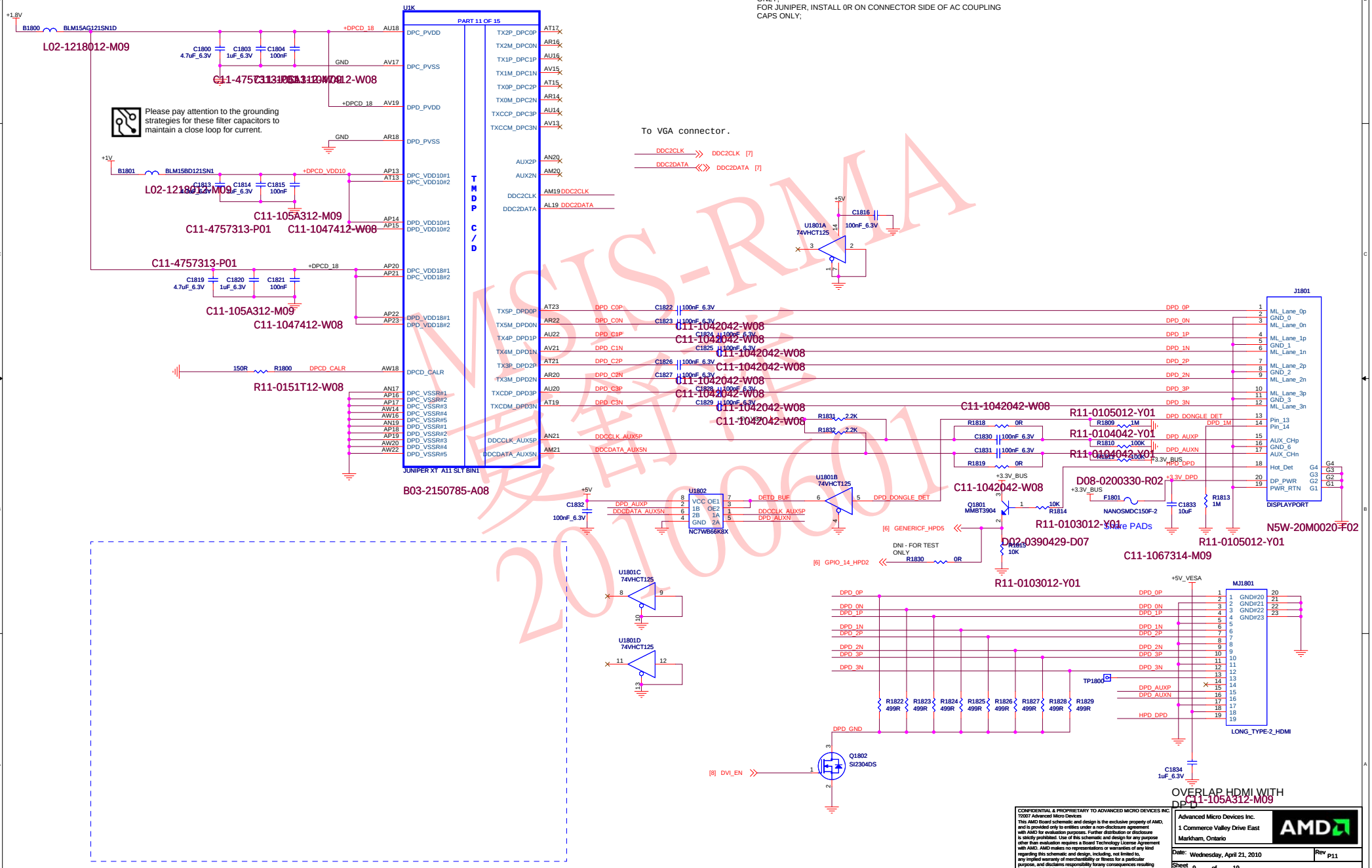
(09) REDWOOD Display Port C & Display Port/HDMI D



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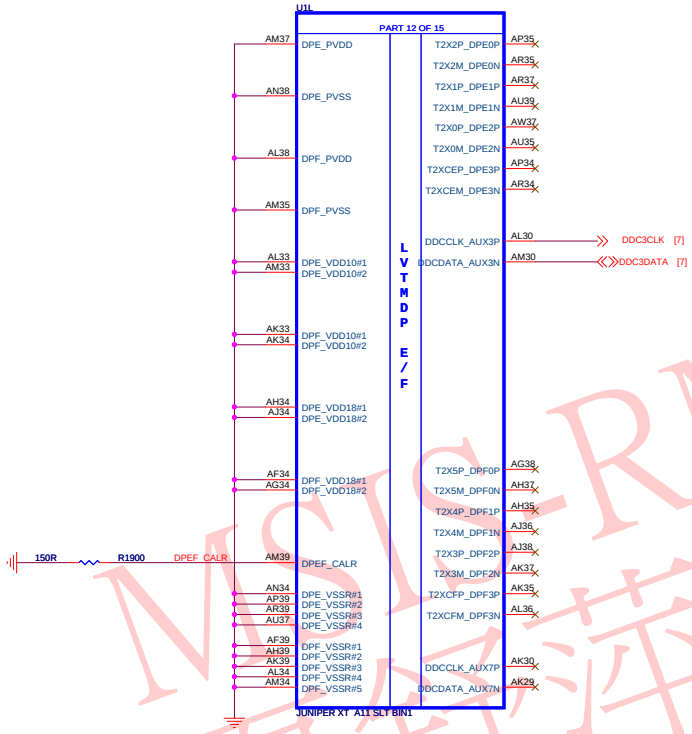
(10) REDWOOD LVTMDP E&F



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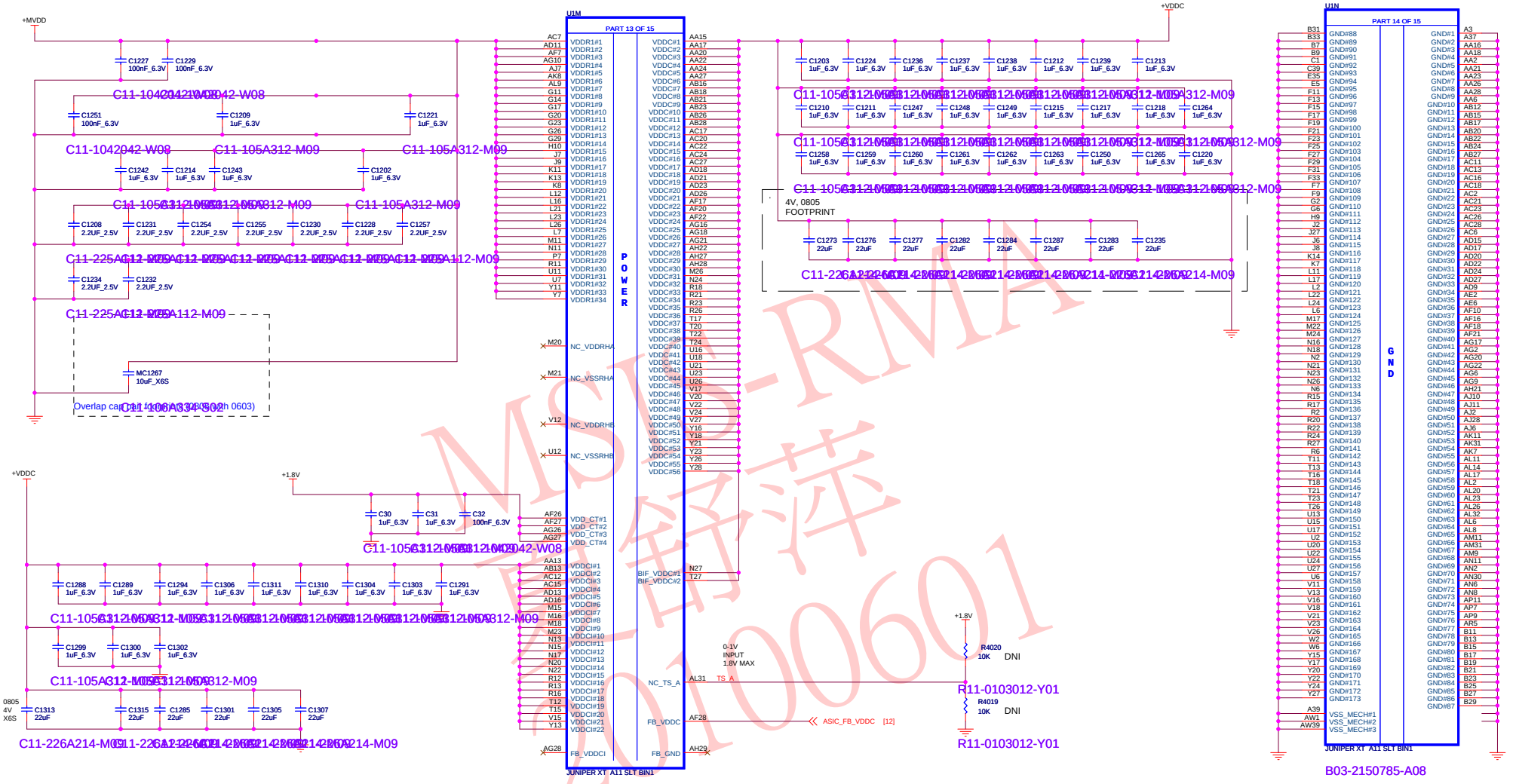
(11) REDWOOD Power & GND



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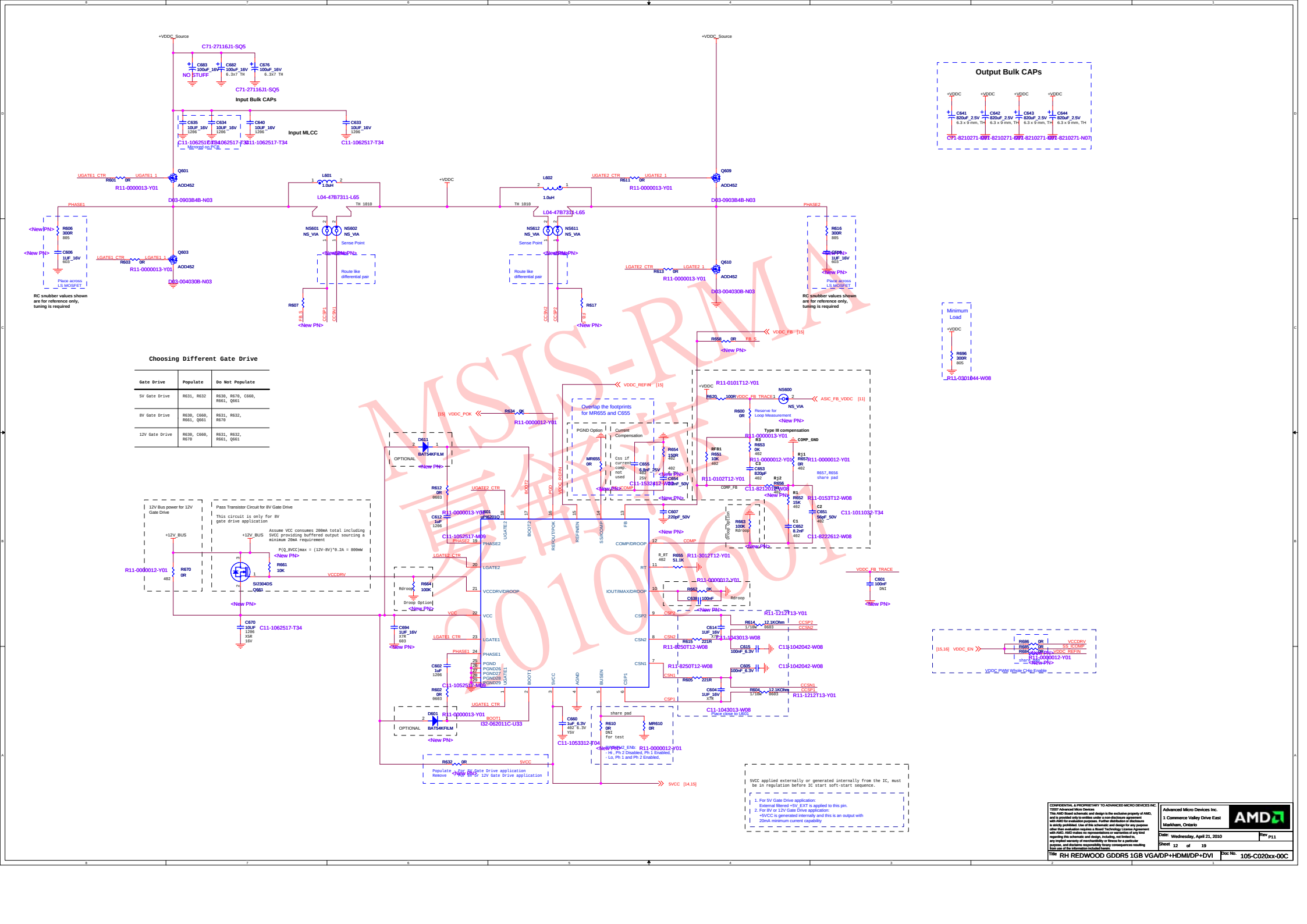
Output Bulk CAPs
Minimum Load
Input Bulk CAPs
Input MLCC
Choosing Different Gate Drive
Gate Drive | Populate | Do Not Populate
5V Gate Drive | R631, R632 | R630, R670, C660, R661, Q661
8V Gate Drive | R630, C660, R661, Q661 | R631, R632, R670
12V Gate Drive | R630, C660, R670 | R631, R632, R661, Q661
RC snubber values shown are for reference only, tuning is required
Sense Point
Route like differential pair
Overlap the footprints for MR655 and C655
Pass Transistor Circuit for 8V Gate Drive
This circuit is only for 8V gate drive application
12V Bus power for 12V Gate Drive
Droop Option
PGND Option
Current Compensation
Type III compensation
share pad
5VCC applied externally or generated internally from the IC, must be in regulation before IC start soft-start sequence.
1. For 5V Gate Drive application: External filtered +5V_EXT is applied to this pin.
2. For 8V or 12V Gate Drive application: +5VCC is generated internally and this is an output with 20mA minimum current capability
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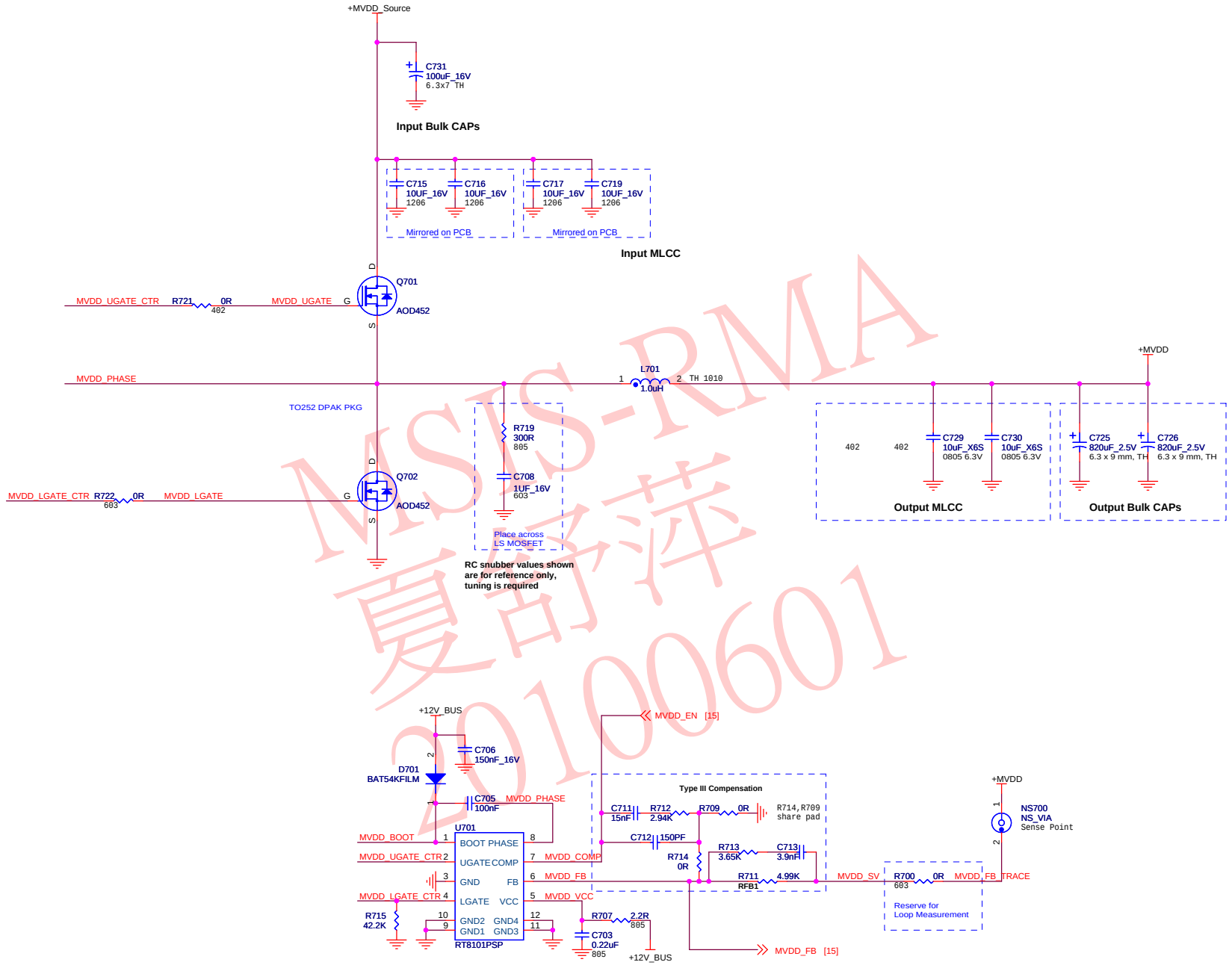

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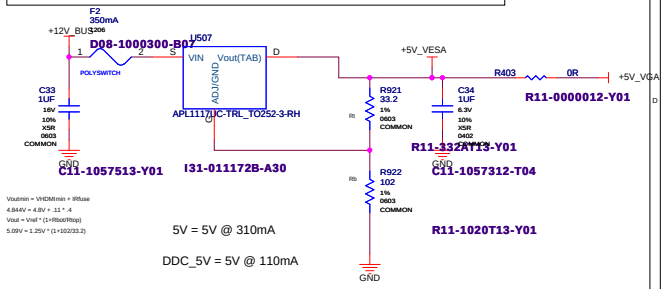
(15) Linear Regulators

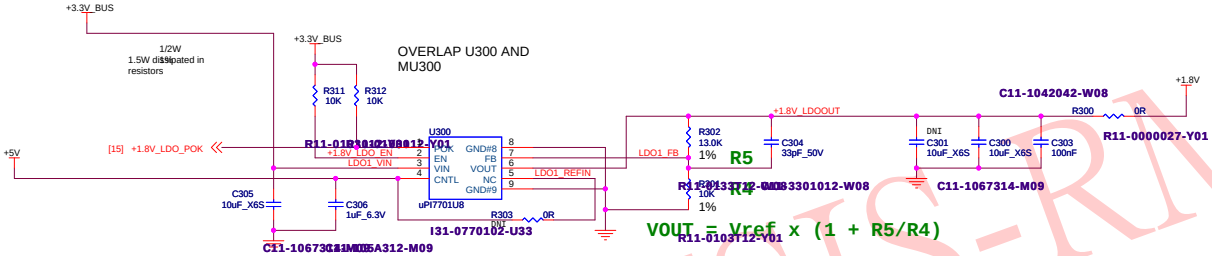
Regulators for +5V, +5V_VESA and +5V_HDMI



LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

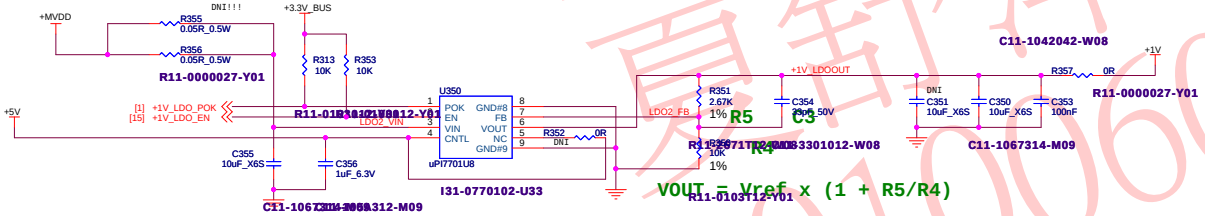
USE 6x 3.6R
AMD PN
3180006800G

1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

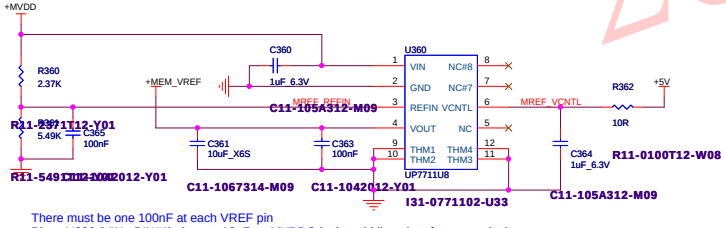


LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA



Memory VREF: Vin = MVDDQ Vout = 0.7xMVDDQ



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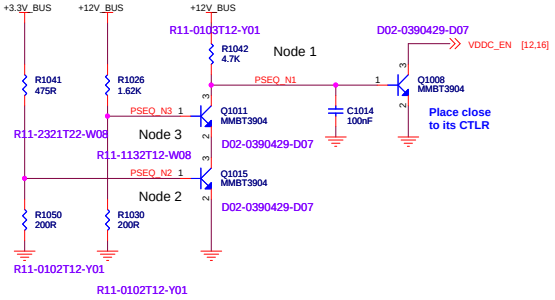
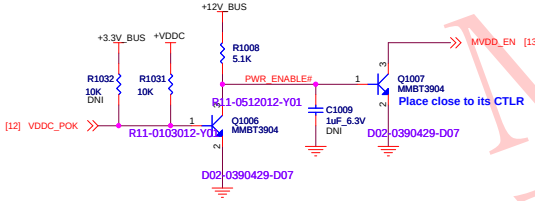
(16) Power Management - Power Gating and Dynamic Voltage Control

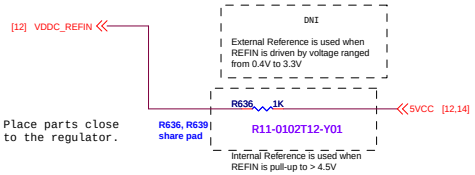
12V_BUS & 3V3_BUS POWER SEQUENCING



POWER SEQUENCING CIRCUIT

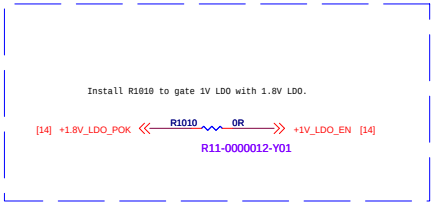


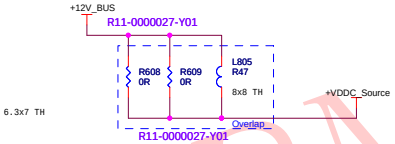
VDDC Reference Voltage Selection

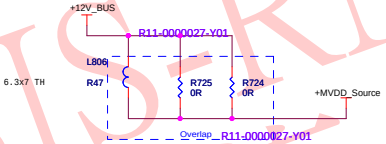


VDDC Vref Mode Selection

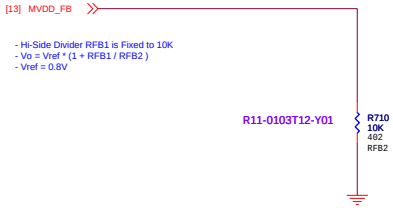
Vref Mode	R636	R639/C689	Vref (V)
Internal	Populate	DNI	0.6
External	DNI	Populate	set by VID IC





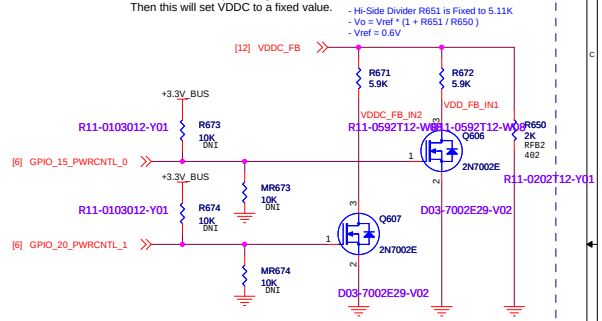


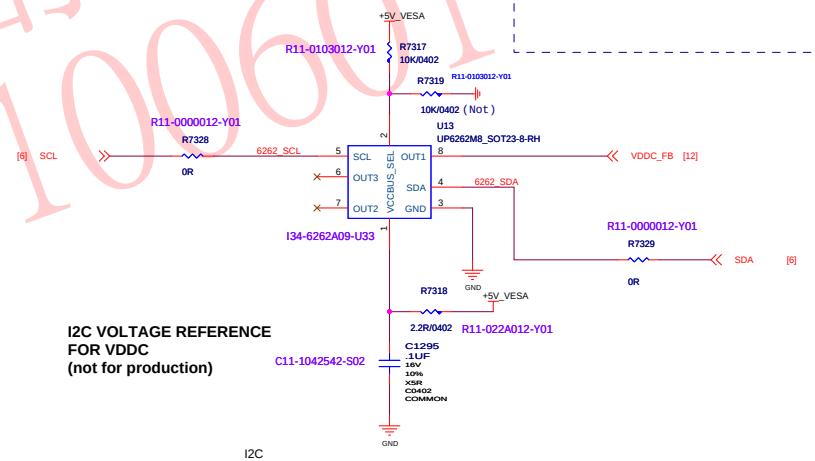
MVDD Low Side Divider



VDDC Low Side Divider

R650 must be poulated only if VID is not used and VDDC VREFIN is pulled high to >4.5V. Then this will set VDDC to a fixed value.





I2C VOLTAGE REFERENCE FOR VDDC (not for production)

I2C ADDRESS: A4

I2C ADDRESS: A4

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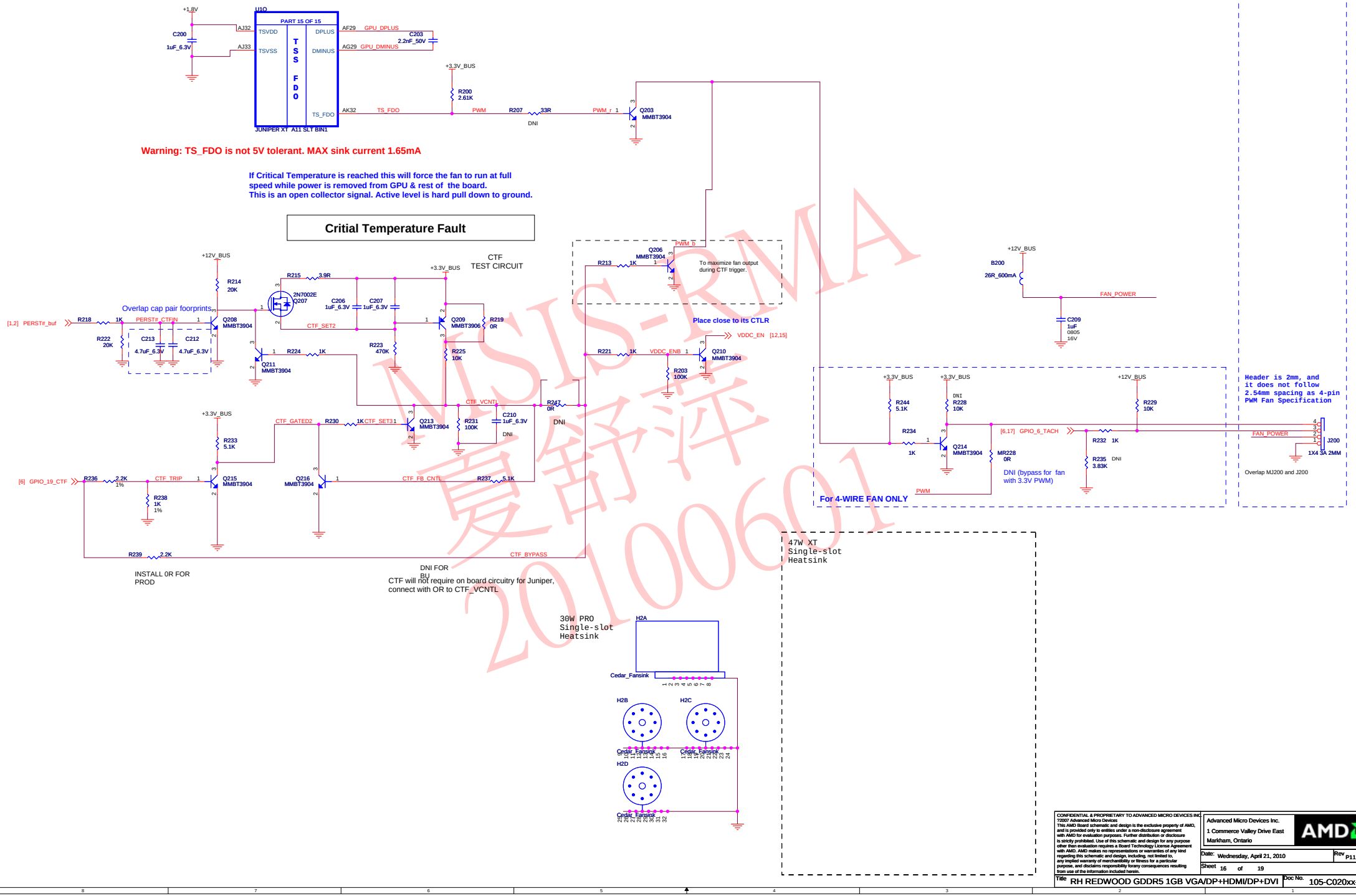
(19) Mechanical and Thermal Management



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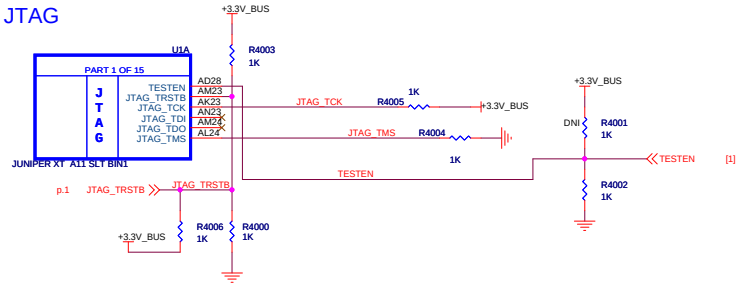
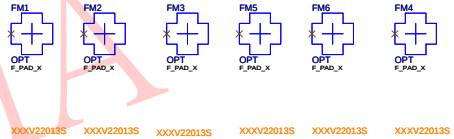
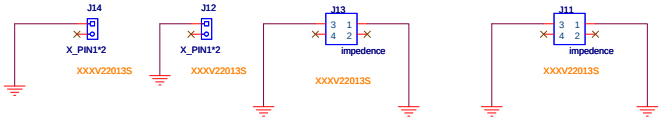
(19) Debug Circuits

JTAG



LM96163 FOR BACKUP THERMAL CONTROL





J11 8 層 MEM_CLK 80OHM 5.118/7.4803

J13 1 層 TMDS 100 OHM 3.98/11.77

J12 1層 45OHM 5.118/ 12 MEM DATA

J14 8 層 45OHM 5.118/ 12 MEM ADD

SCL/SDA PORT DEBUG ACCESS

Place connector on the back side
(easily accessible and not blocked by the heatsink).

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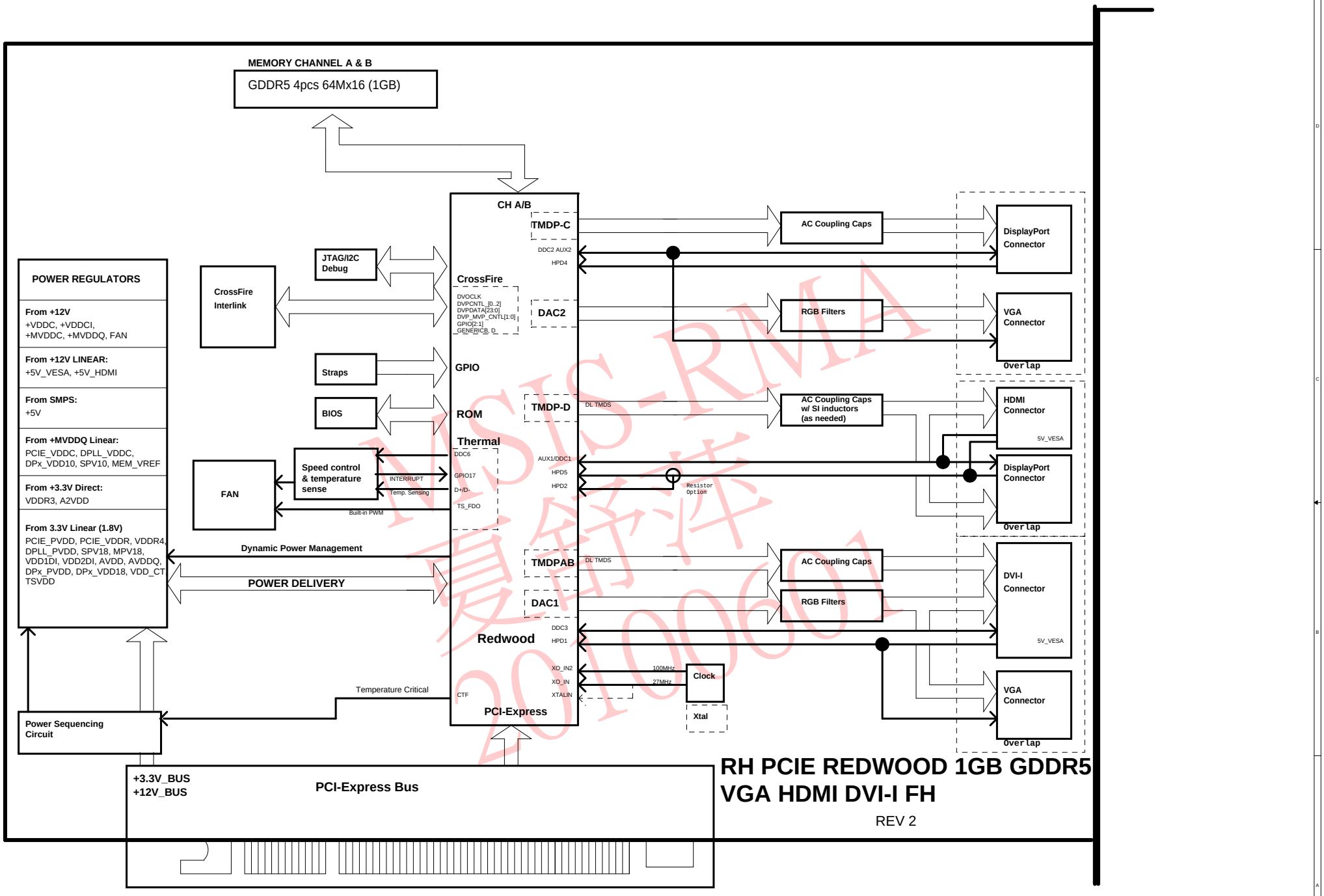

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Title	Schematic No.	Date:
RH REDWOOD GDDR5 1GB VGA/DP+HDMI/DP+DVI	105-C020xx-00C	Wednesday, April 21, 2010

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev P11

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
00	00A	2009/05/08	
01	00B	2009/08/20	
02	00C	2009/09/28	REDWOOD XT GDDR5 1GB - Initial Release