

P727-A01: G96, GB1-128, GDDR3, DL-DVI, DL-DVI/VGA, SD/HDTV

V129-122

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- Page 22: POWER SUPPLY LINEARS: 5V, DDC5V, IFP PLLVDD, IFP IOVDD, MIO VDD, 3V3 FILTER, 12V FILTER
- Page 23: POWER SUPPLY: FBVDDQ +PEX_VDD SINGLE PHASE SWITCHER
- Page 24: POWER SUPPLY: NVVDD DUAL PHASE SWITCHER
- Page 25: POWER SUPPLY: Dynamic NVVDD

REV 1.2 HISTORY

04/01

PAGE 12.Remove J1 Slim-DSUB connector

PAGE 15.Add R761 and R762 to reserve pull down DP AUX
Change F503 and F504 footprint to 1812 size
Remove DP J8 Pin25,Pin26

PAGE 18.Change U514~U517 to EM1~EM6

PAGE 19.Add 2pin Fan control circuit

PAGE 23.Add C120,C149 10uF 1206 footprint to reserve PEX_VDD power

04/08

PAGE 22. Add R92 0805 0ohm Resistor for 3V3 bypass to 2V5 power

REV 1.21 HISTORY

06/04

PAGE 20.Add R774 10K pull down resistor for HDA issue

REV 1.22 HISTORY

07/16

PAGE 22. Reverse Diode at 5V regulator input side to prevent Leakage to 12V

PAGE 22. Reverse CAP SOLID for A2V5

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10727-0000-001	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKJ0000	600-10727-0000-100	G96-A01, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
2	SKJ0001	600-10727-0001-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
3	SKJ0002	600-10727-0002-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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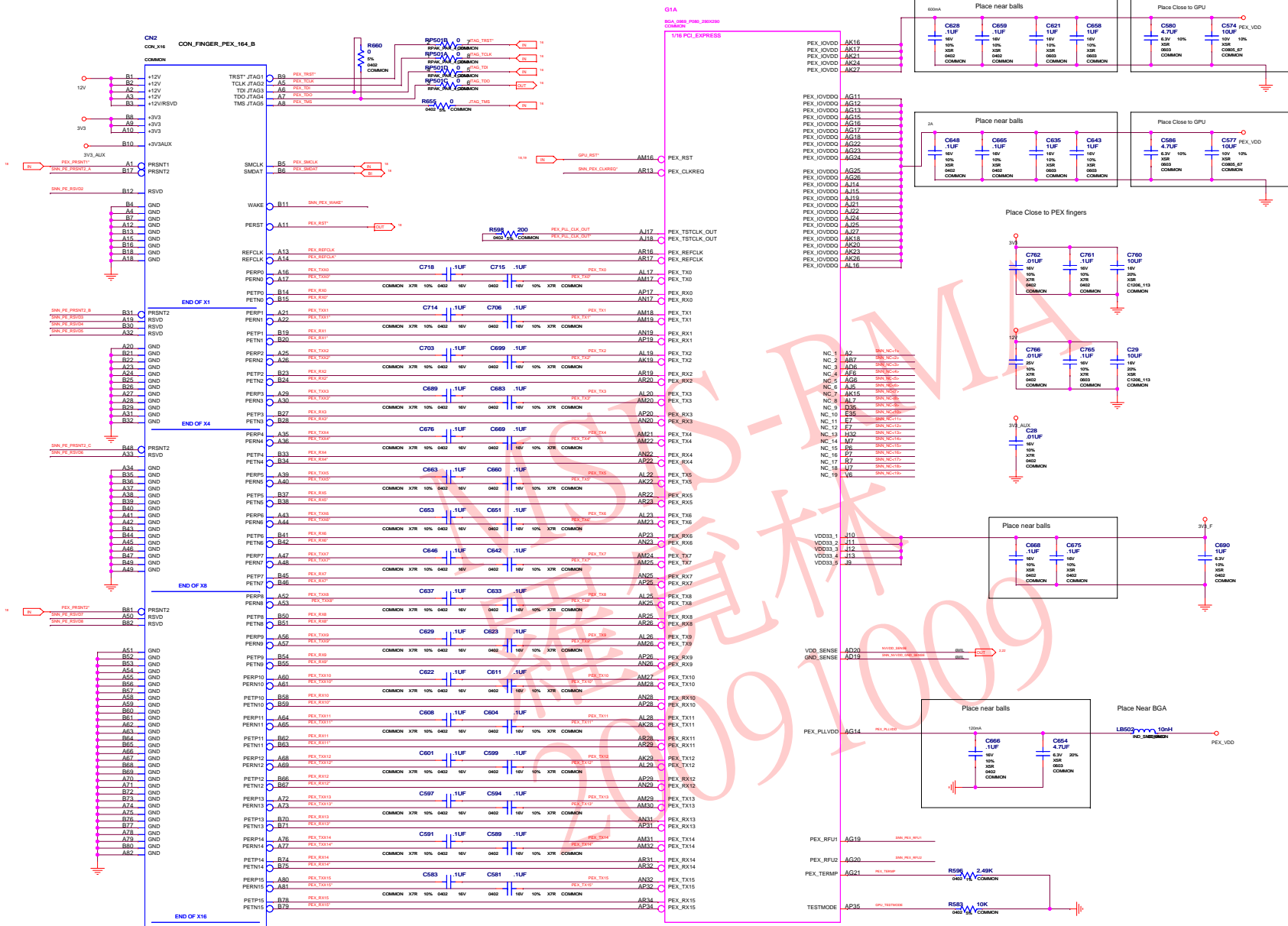
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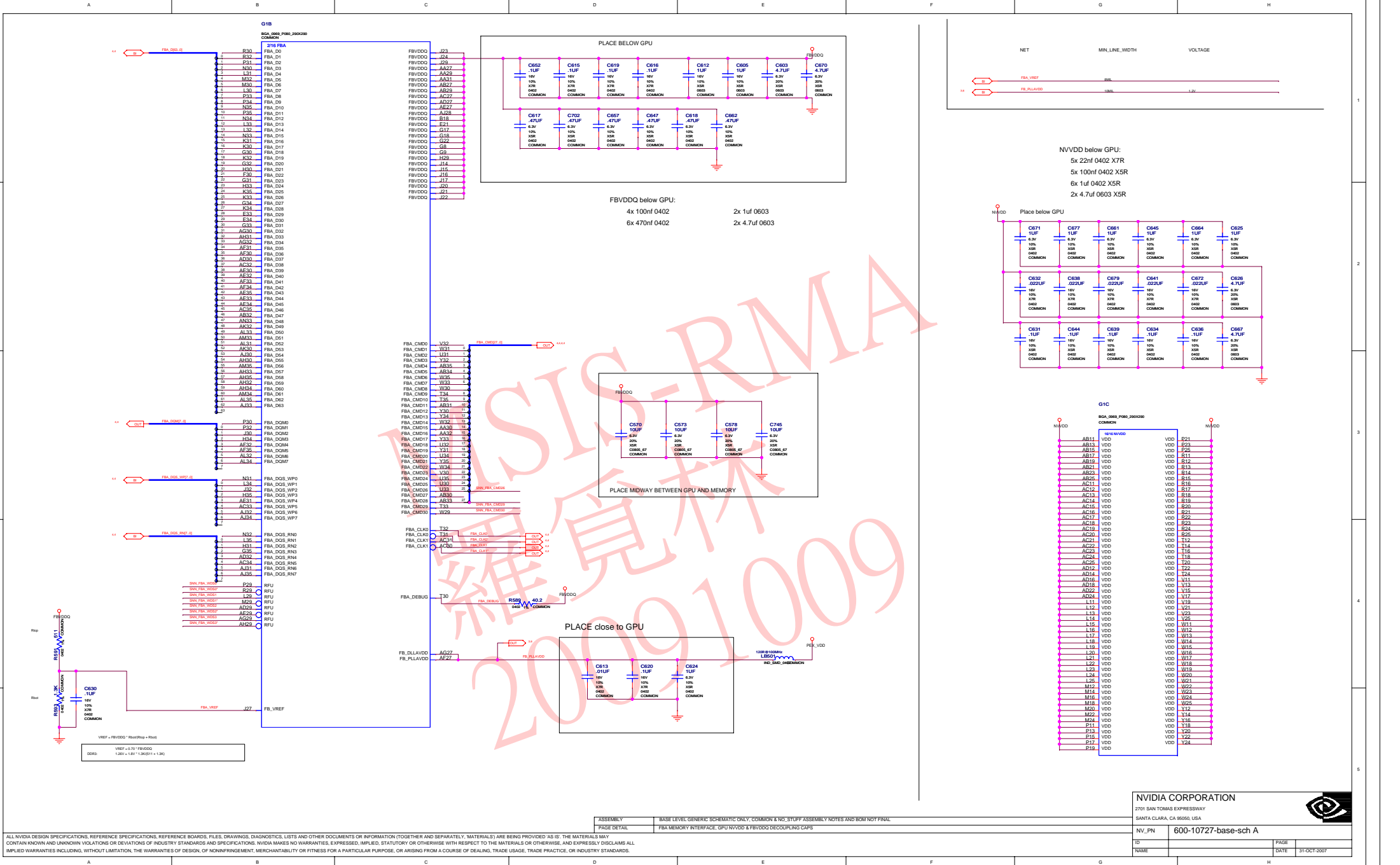
16X PEX INTERFACE



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PEX12	PEX13	PEX14	PEX15
PEX16	PEX17	PEX18	PEX19
PEX20	PEX21	PEX22	PEX23
PEX24	PEX25	PEX26	PEX27
PEX28	PEX29	PEX30	PEX31
PEX32	PEX33	PEX34	PEX35
PEX36	PEX37	PEX38	PEX39
PEX40	PEX41	PEX42	PEX43
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PEX60	PEX61	PEX62	PEX63
PEX64	PEX65	PEX66	PEX67
PEX68	PEX69	PEX70	PEX71
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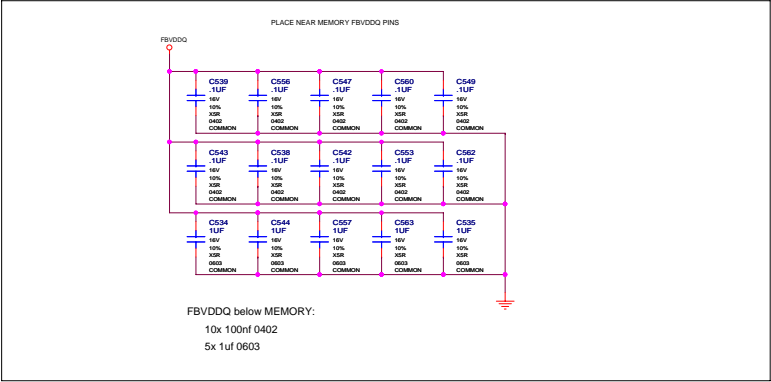
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ASSEMBLY NAME LEVEL: GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE: DETAIL FBVDDQ/FBVDD DECOUPLING CAPS

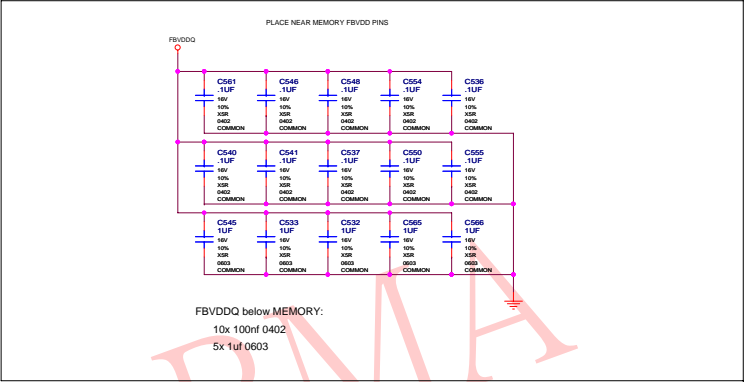
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FRAME BUFFER: PARTITION A DECOUPLING

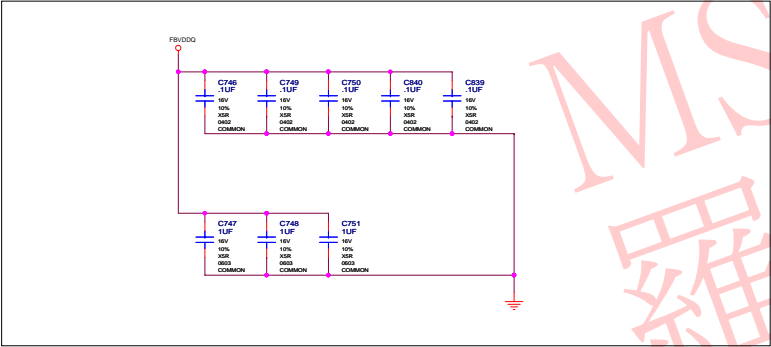
Decoupling for FBA 0..31



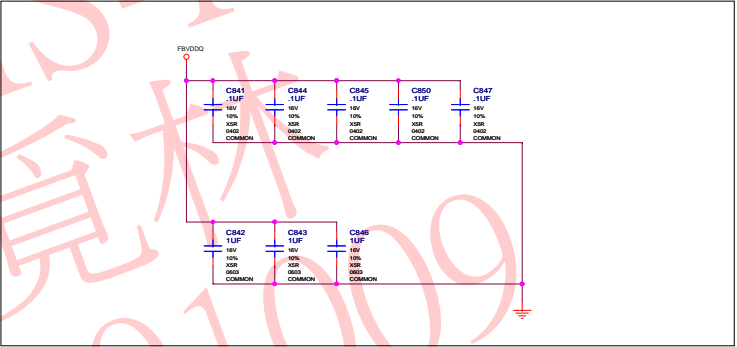
Decoupling for FBA 32..63



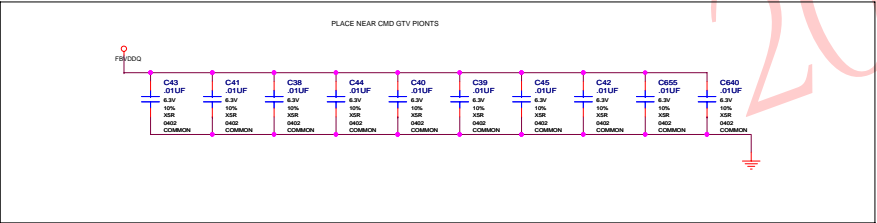
Decoupling for FBA A1 0..31



Decoupling for FBA A1 0..31



Return path coupling GND/FBVDDQ for FBA

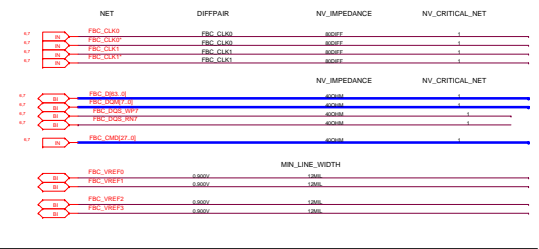
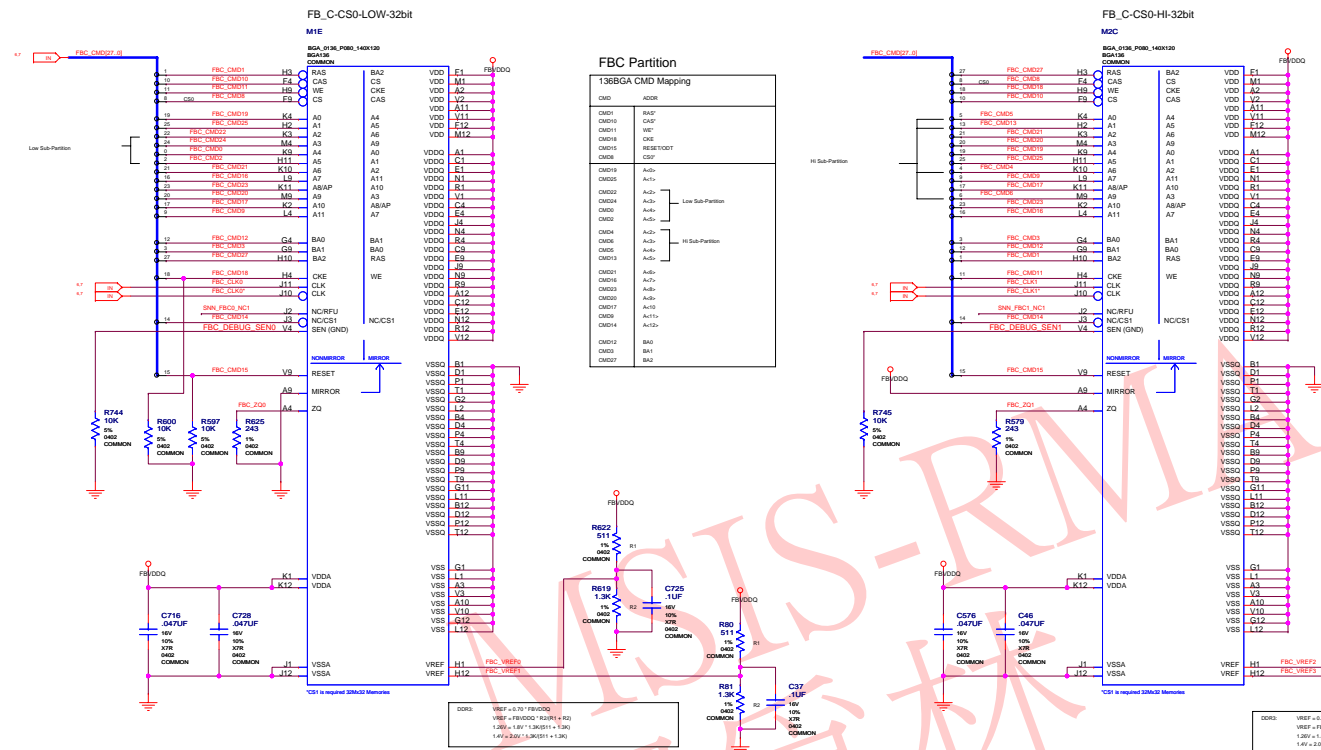


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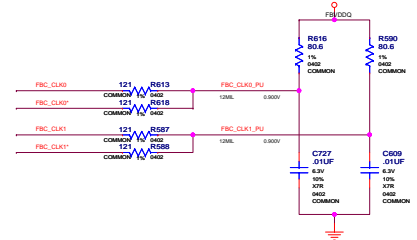
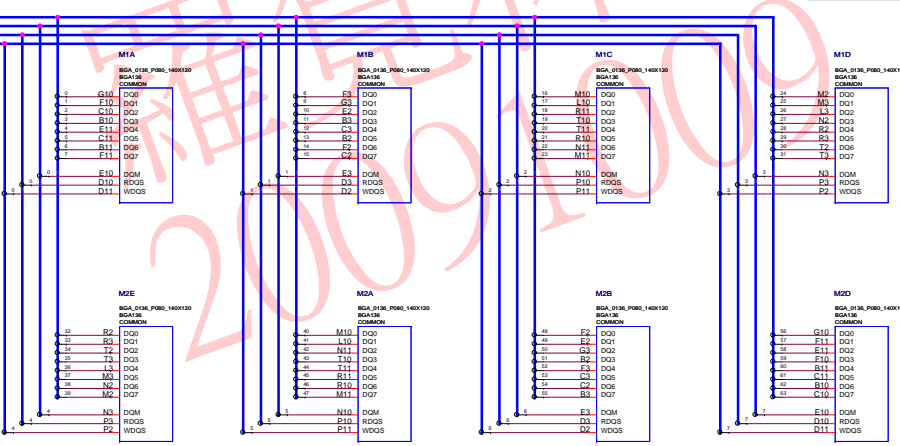
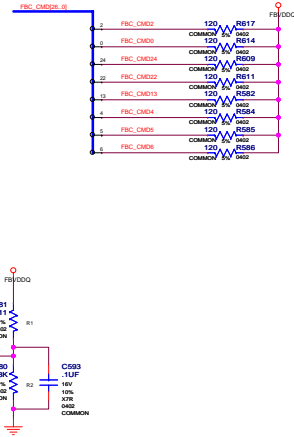
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FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3



Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!



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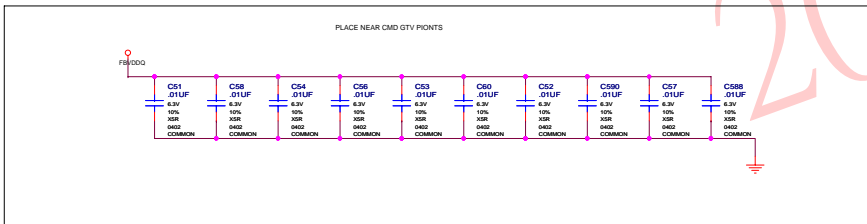
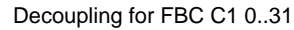


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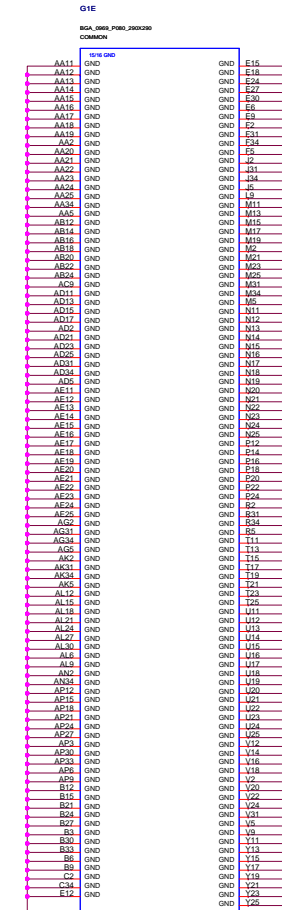
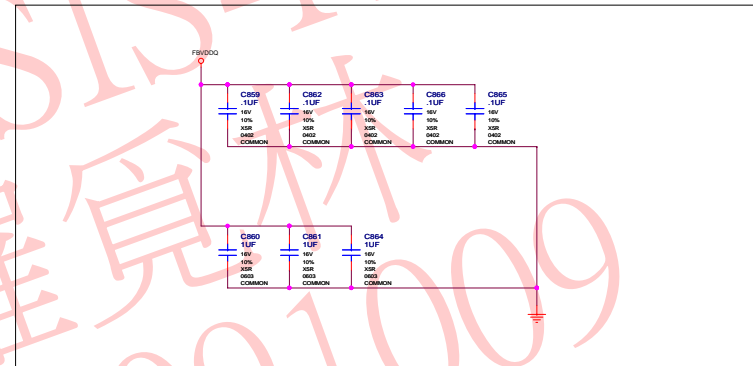
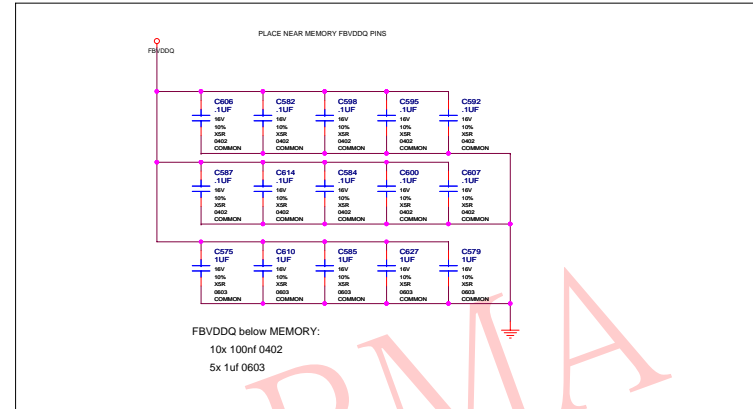
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS PU'S, FBC CLK TERMS

[illegible]

Decoupling for FBC 0..31



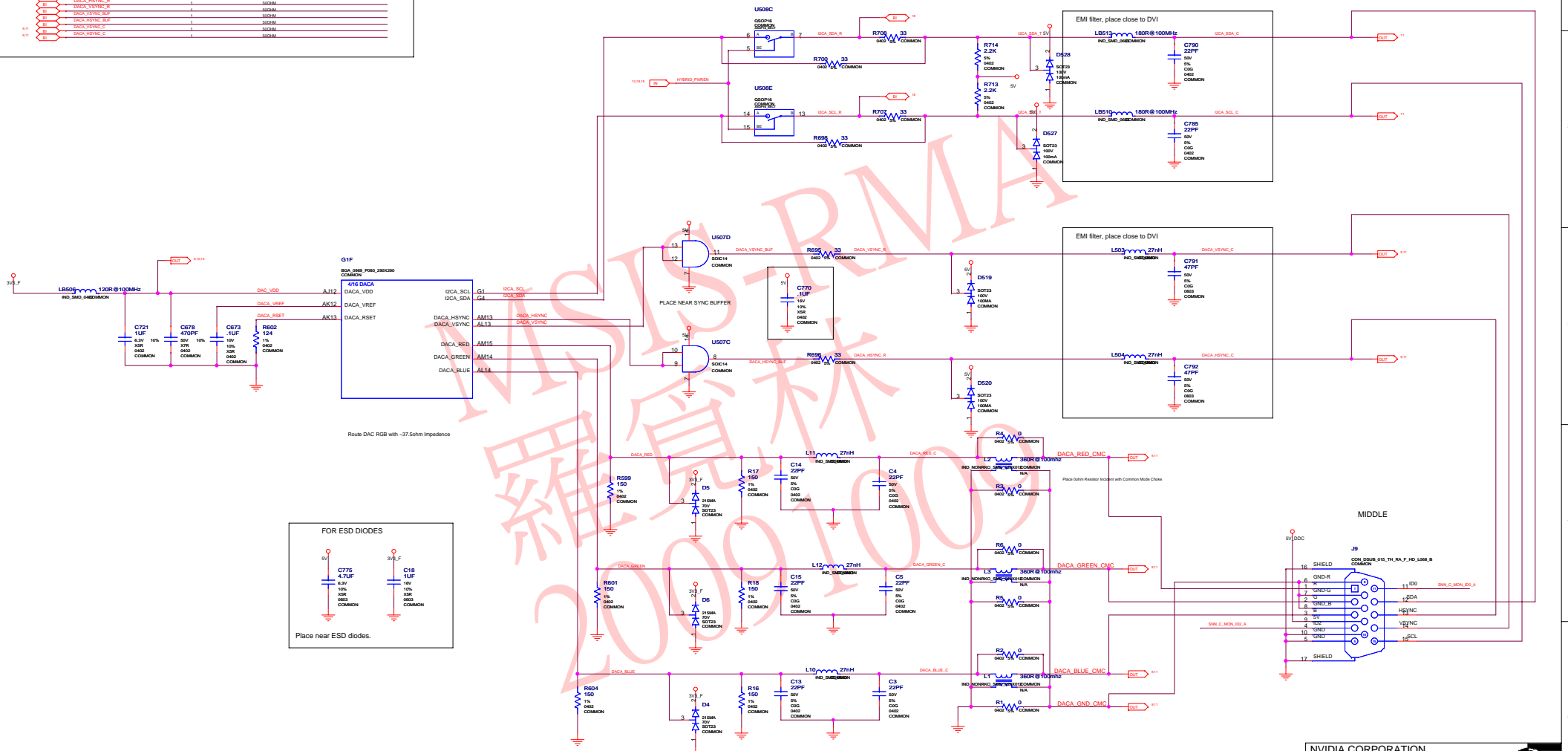
Decoupling for FBC C1 32..63



	NET_NAME	WV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
6.3.1.4	IN			3.30 120M
	DATA_VDD			
IN	DATA_VREF			120M
IN	DATA_VBIAS			120M
	DATA_RSD	1	75OHM	
IN	DATA_GREEN	1	75OHM	
IN	DATA_BLUE	1	75OHM	
	DATA_RSD_C	1	75OHM	
IN	DATA_GREEN_C	1	75OHM	
IN	DATA_BLUE_C	1	75OHM	
6.3.1.5	DATA_GND_CMIC			0V 120M
6.3.1	DATA_GND_CMIC	1	75OHM	
6.3.1	DATA_GREEN_CMIC	1	75OHM	
6.3.1	DATA_BLUE_CMIC	1	75OHM	
	DATA_VTNC	1	50OHM	
	DATA_VTNC_R	1	50OHM	
	DATA_VTNC_R	1	50OHM	
	DATA_VTNC_R	1	50OHM	
	DATA_VTNC_BUF	1	50OHM	
6.3.1	DATA_VTNC_BUF	1	50OHM	
6.3.1	DATA_VTNC_C	1	50OHM	
	DATA_VTNC_C	1	50OHM	

Primary Display (DACA), DVI-I

DACA RGB-FILTER



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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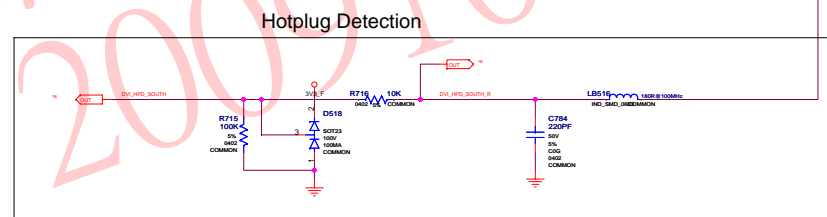
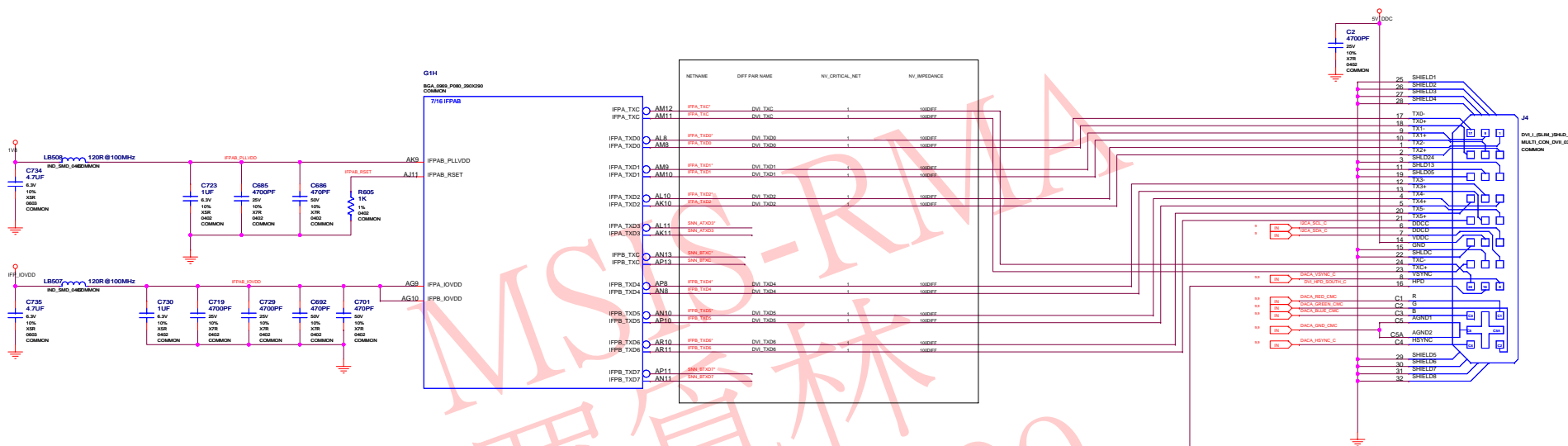


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TMDS LINK: A & B



	NETNAME	MIN_LINE_WIDTH	VOLTAGE
SI	FFAB_ILVDD	120u	1.8V
SI	FFAB_ICVDD	120u	3.3V
SI	FFABISSET	120u	

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	IV_1
	ID

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	IV_1
	ID

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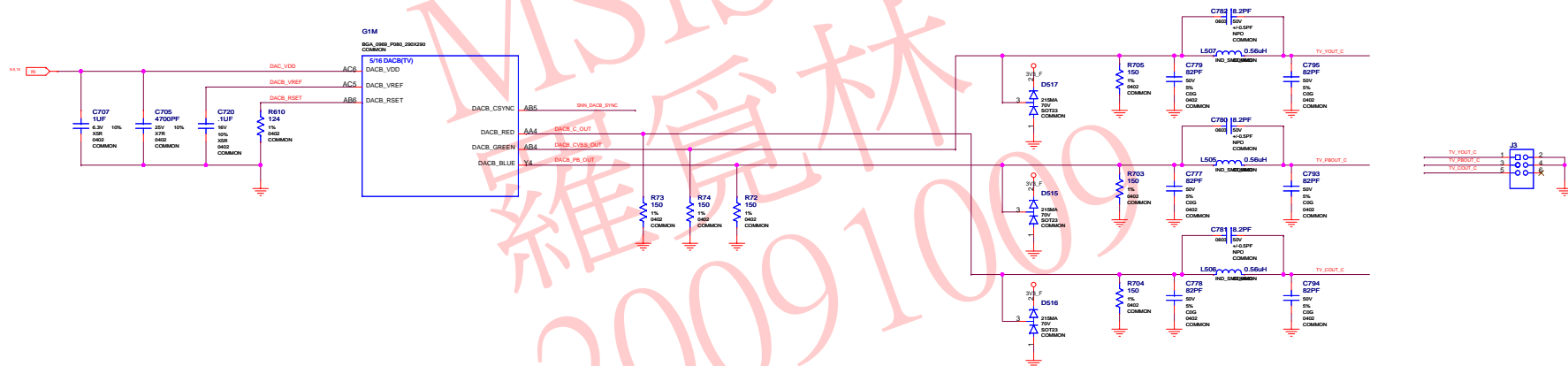
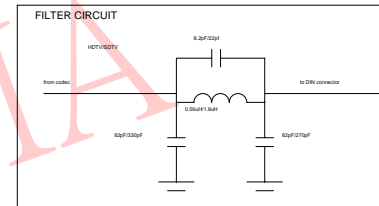
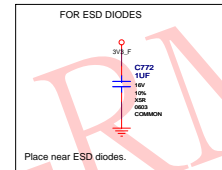
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DACB: SD/HD VIDEO OUT CONNECTOR

	NET_NAME	MIN_LINE_WIDTH	NY_IMPEDANCE	NY_CRESTAL_NET
Q11	DACB_C_OUT		750HM	1
Q12	EDOTD_CIN1_COUT		750HM	1
Q13	WACB_PIE_COUT		750HM	1
Q14				
Q1	TV_PICOUT_C		750HM	1
Q2	TV_PICIN_C		750HM	1
Q3	TV_PICOUT_C		750HM	1
Q4				
Q5	DACB_VREF	100M		
Q6	DACB_VREF	100M		



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, MINIDIN CONNECTOR NORTH, SD/HD VIDEO OUTPUT CONNECTOR

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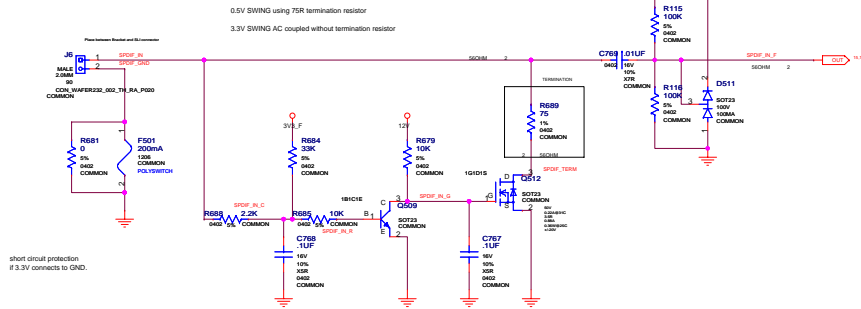


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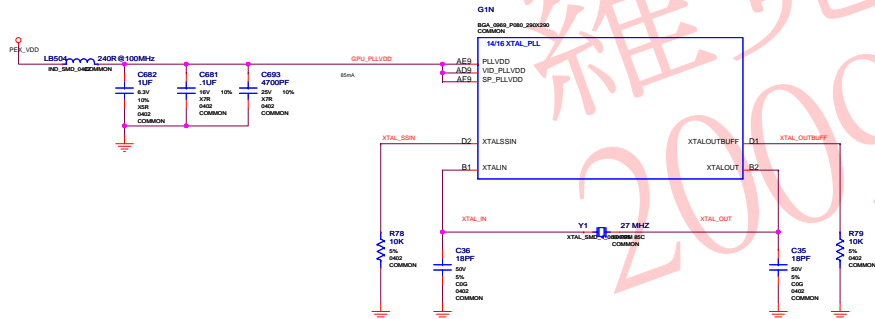
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XTAL/PLLVDD/SPDIF IN

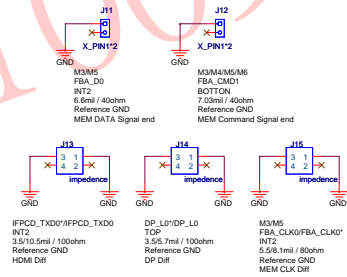
SPDIF IN



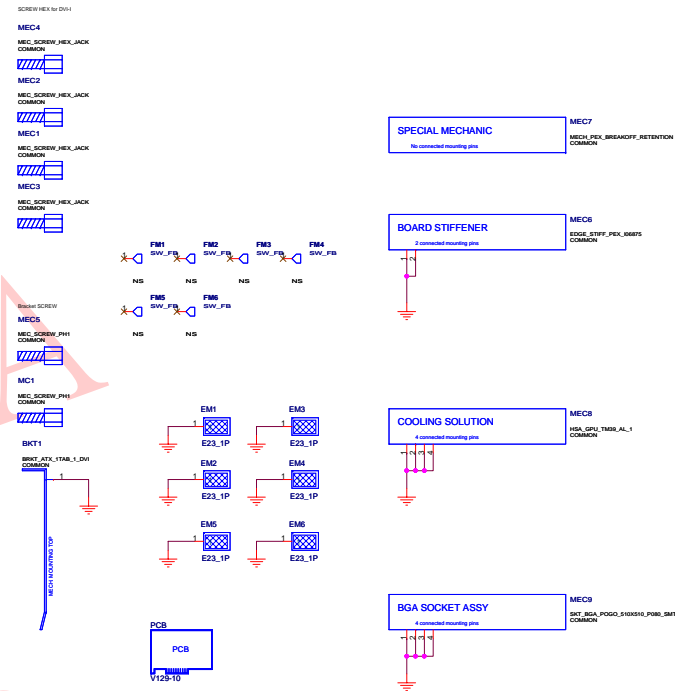
XTAL/GPU_PLLVDD



Impedance control line



MECHANICALS & THERMALS



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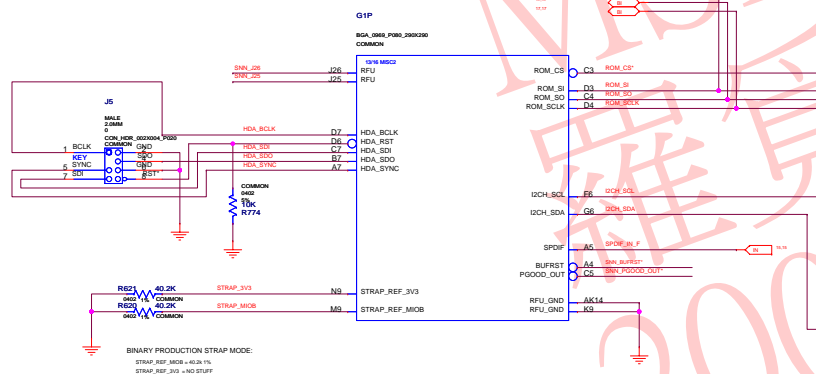
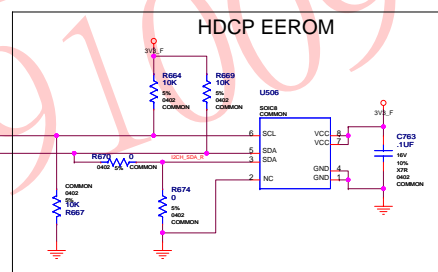
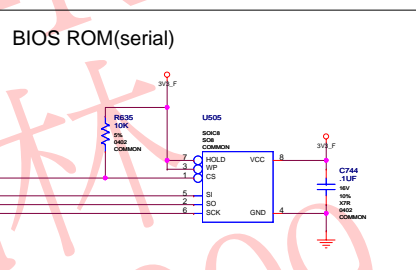
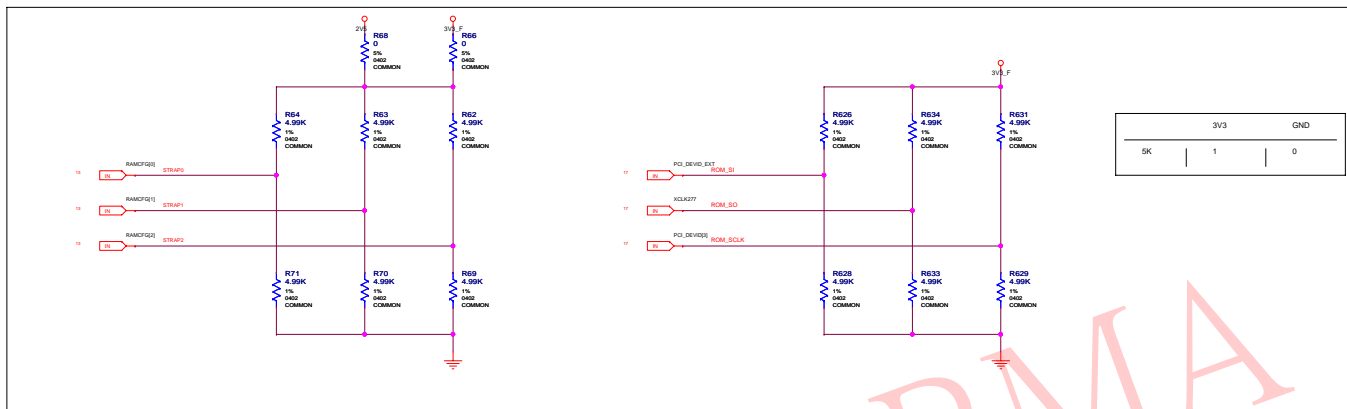
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF-IN, XTAL, MECHANICALS, THERMALS

STRAPPING OPTIONS

Assembly: BIOS



	NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
OUT	HDA_BCLK		50Ω(1M)	2
OUT	HDA_FSI1		50Ω(1M)	2
OUT	HDA_SCK		50Ω(1M)	2
OUT	HDA_SDIO		50Ω(1M)	2
OUT	HDA_SSPIC		50Ω(1M)	2

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

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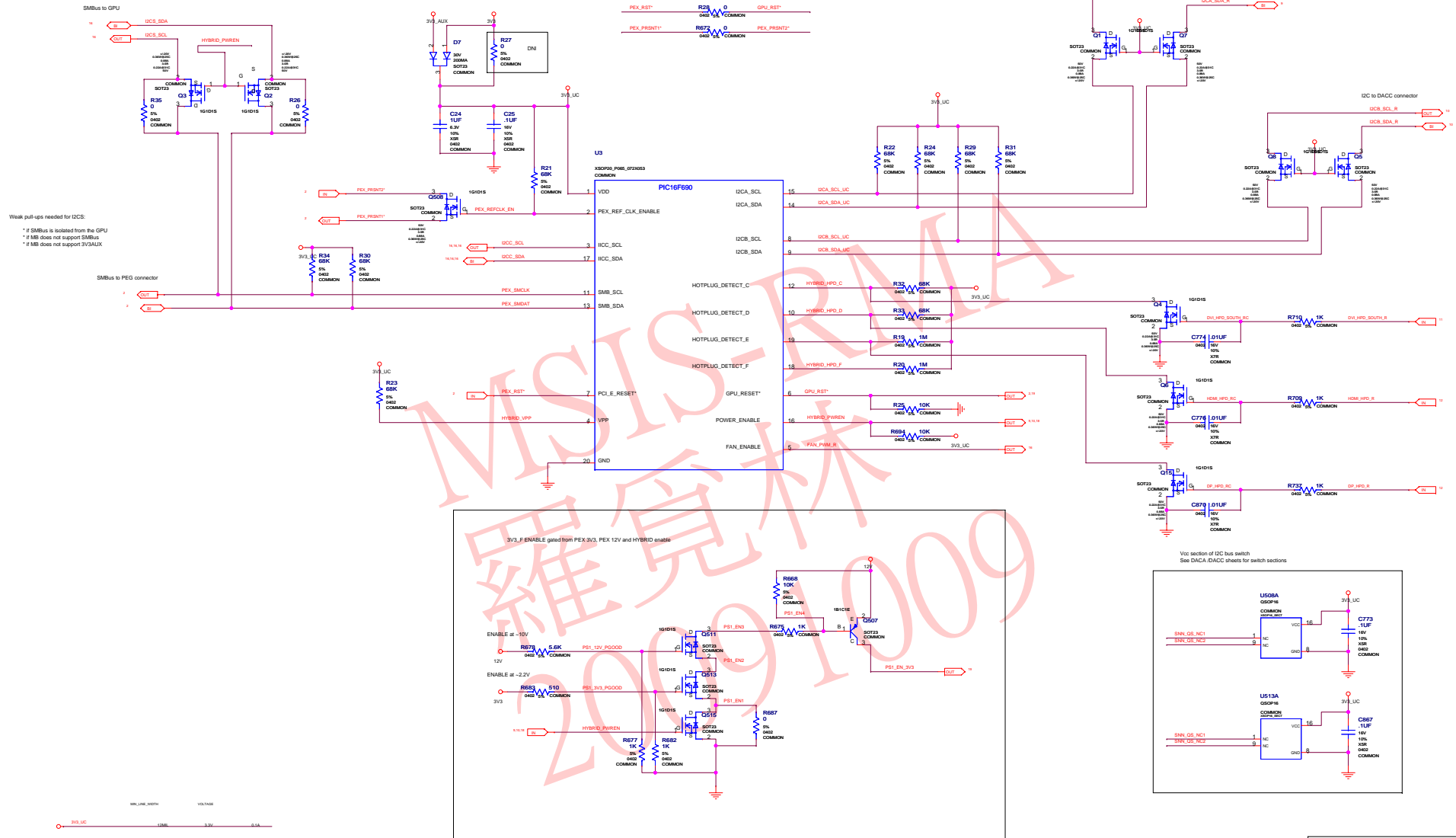
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HYBRID POWER

Per Datasheet:

Vf = 400mV at 10mA
* expected current < 2mA

Stuff only to bypass the micro-controller



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	HYBRID POWER CIRCUIT

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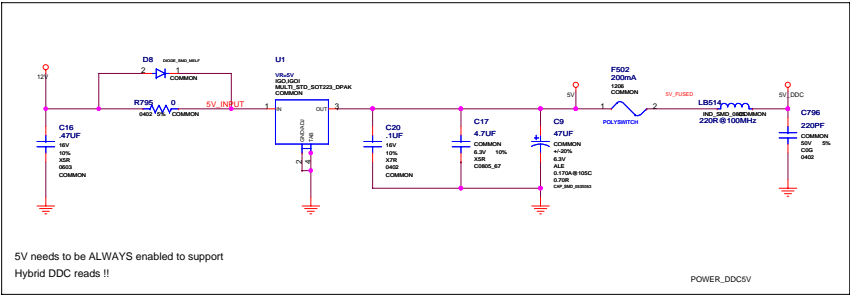
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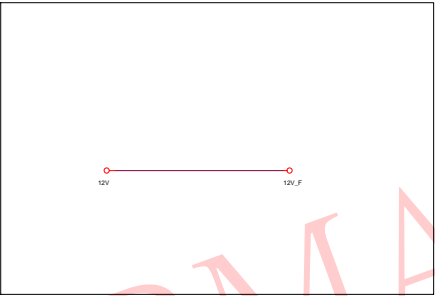
Power Supply: 5V, 5V_DDC, TMDS, MIOA_VDDQ

5V REGULATOR

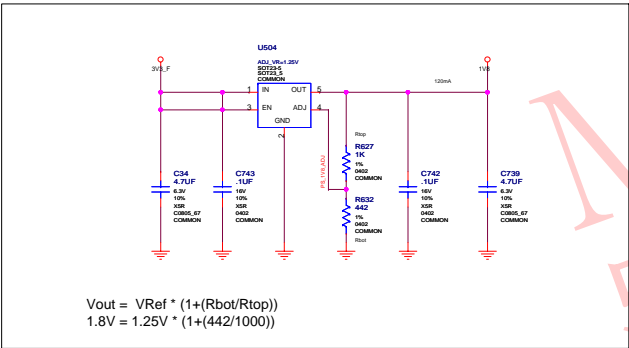


5V DDC

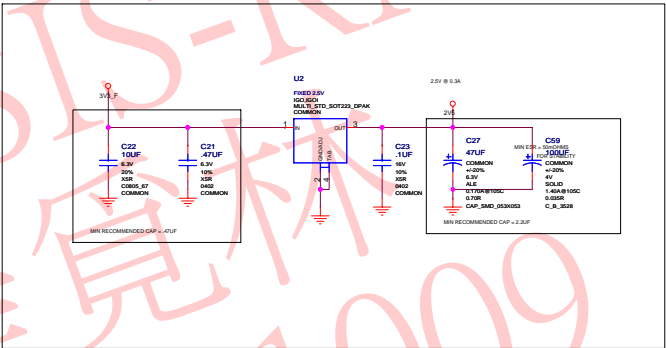
12V filter



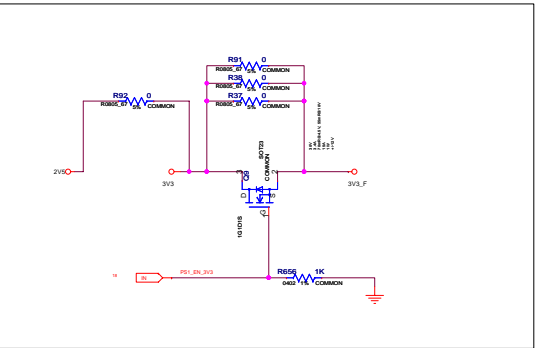
IFP PLL Supply 1.8V



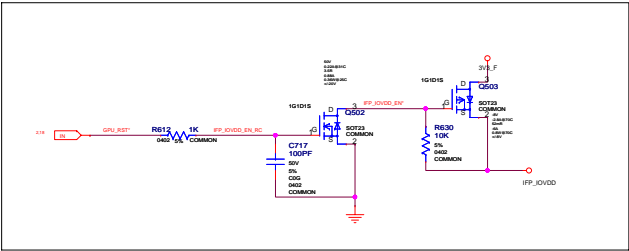
MIO_VDD 2.5V



3V3 switch



IFP_IOVDD BACKDRIVE PREVENTION



NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
5V_FUSED	0.1A	120µm	5V
5V_DDC	0.1A	120µm	5V
5V	0.1A	120µm	5V
PL1_V16_ADJ	0.1A	120µm	1.8V
1V8	0.1A	120µm	1.8V
2V5	0.1A	120µm	2.5V
3V3	0.1A	120µm	3V
3V3_F	0.1A	120µm	3.3V
12V_F	0.1A	200µm	12V

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 3100FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY LINEARS: 5V, DDC5V, IFPPLLVD, IFP10VDD, MIO_VDD, 3V3 FILTER, 12V FILTER

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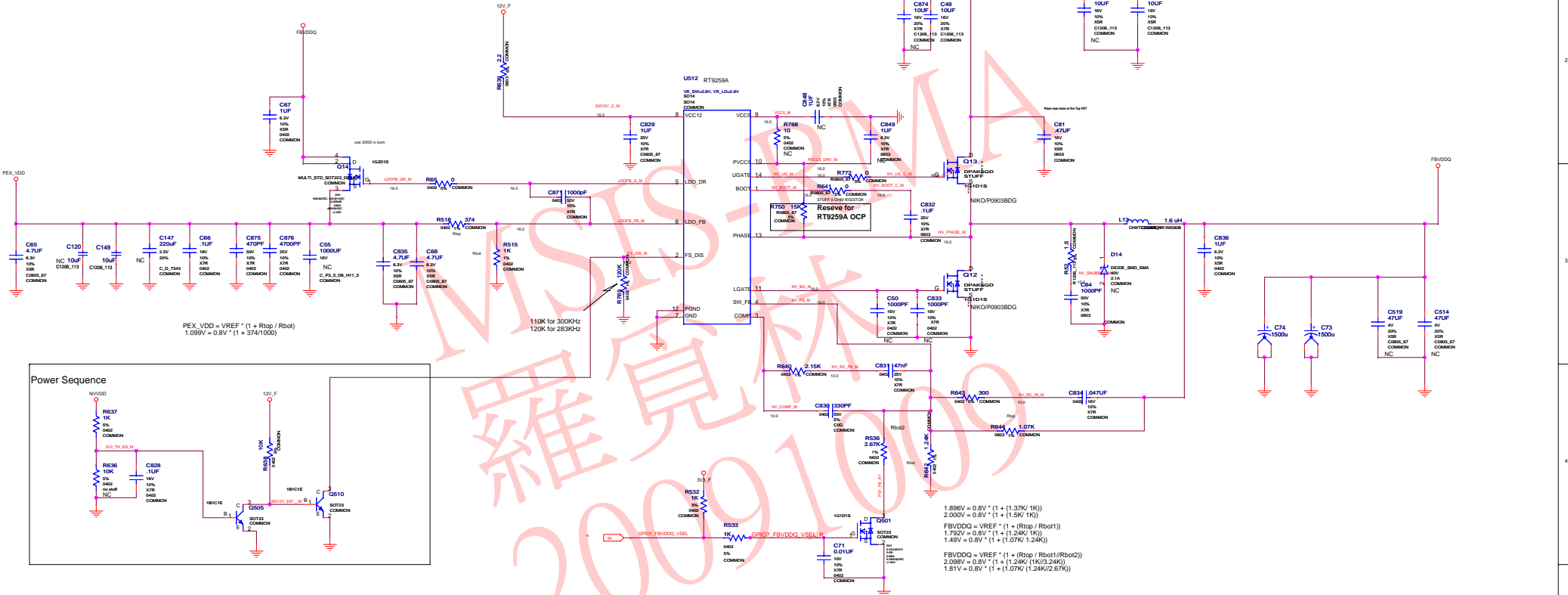
POWER SUPPLY: FBVDD/Q

NET	MIN_LENGTH	VOLTAGE	MAX_CURRENT
FBVDDQ	12000	1.2V	1.5A
PRE_F0_B00T_0	12000		
PRE_F0_B00T_1	12000		
PRE_F0_B00T_2	12000		
PRE_F0_B00T_3	12000		
PRE_F0_B00T_4	12000		
PRE_F0_B00T_5	12000		
PRE_F0_B00T_6	12000		
PRE_F0_B00T_7	12000		
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PRE_F0_B00T_9	12000		
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PRE_F0_B00T_11	12000		
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PRE_F0_B00T_97	12000		
PRE_F0_B00T_98	12000		
PRE_F0_B00T_99	12000		
PRE_F0_B00T_100	12000		

FBVDDQ: 1.2mil internal plane
500 mil wide from VRM to MEM
3inch from VRM to farthest MEM

FBVDDQ: 1.8-2.0V @ 9A

FBVDD/Q decap near VRM:
1x 47uF 1206
1x 1500uF ALE/OSCON



FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3

1

2

3

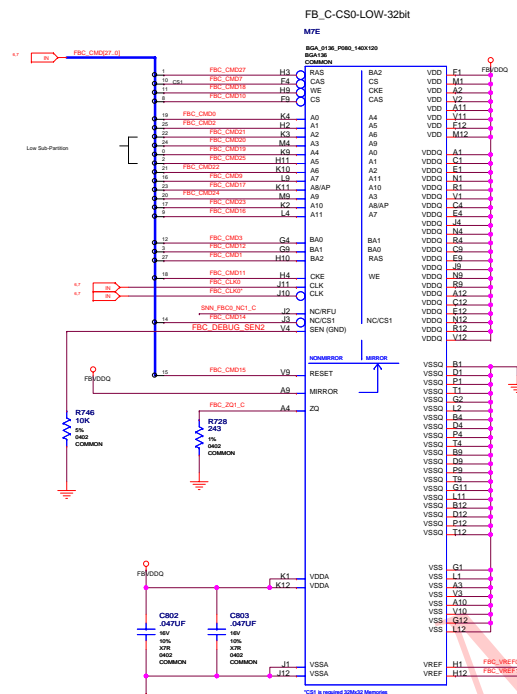
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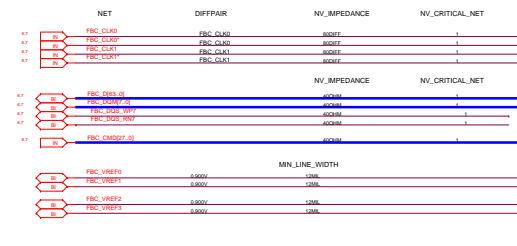
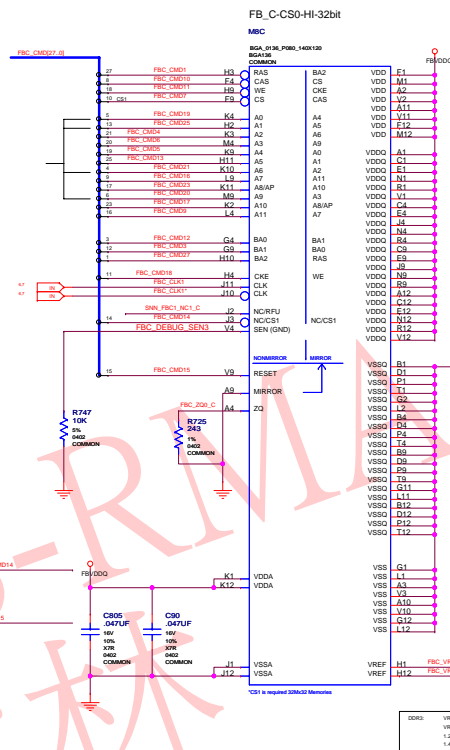
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136BGA CMD Mapping	
QMC	ADDR
QMC01	BA0*
QMC02	BA1*
QMC03	BA2*
QMC04	BA3*
QMC05	BA4*
QMC06	BA5*
QMC07	BA6*
QMC08	BA7*
QMC09	BA8*
QMC10	BA9*
QMC11	BA10*
QMC12	BA11*
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QMC545	BA544*
QMC546	BA545*

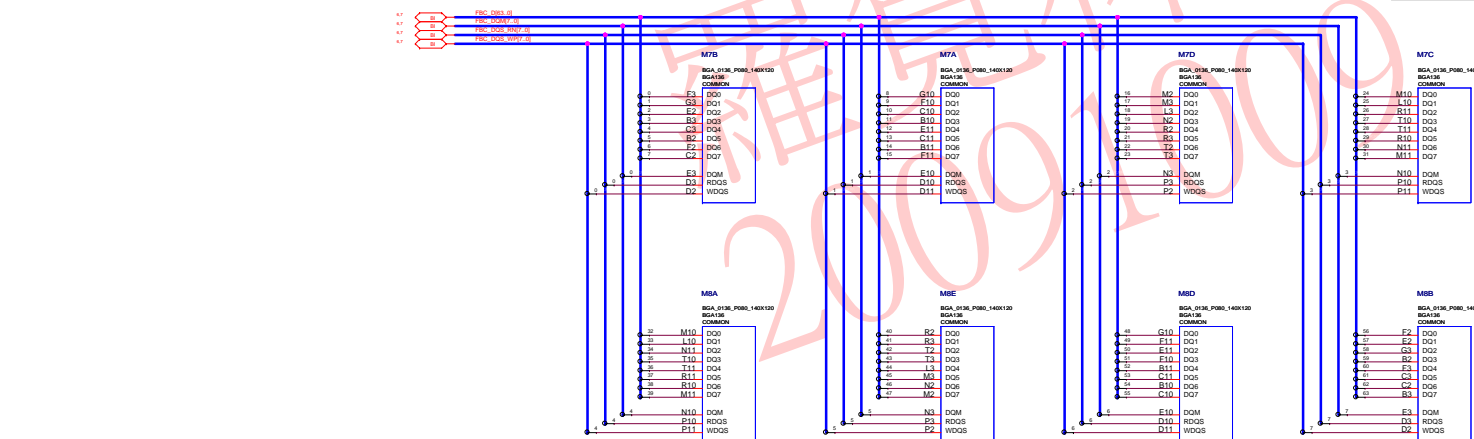
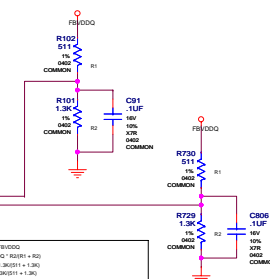
FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3




FBC Partition			CSD
CMD	ADDR		
CMD1	R4D*		
CMD2	CAC*		
CMD11	WE*		
CMD18	CSE		
CMD15	RESET/IO0*		
CMD6	CSD		
CMD19	Ar0*		
CMD25	Ar1*		
CMD3	Ar2*		
CMD24	Ar3*		Line Sub-Partition
CMD0	Ar4*		
CMD2	Ar5*		
CMD4	Ar6*		
CMD6	Ar7*		HS Sub-Partition
CMD5	Ar8*		
CMD13	Ar9*		
CMD21	Ar0*		
CMD16	Ar1*		
CMD3	Ar2*		
CMD0	Ar3*		
CMD17	Ar4*		
CMD5	Ar11*		
CMD14	Ar12*		
CMD12	BA0		
CMD3	BA1		
CMD27	BA2		



Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!

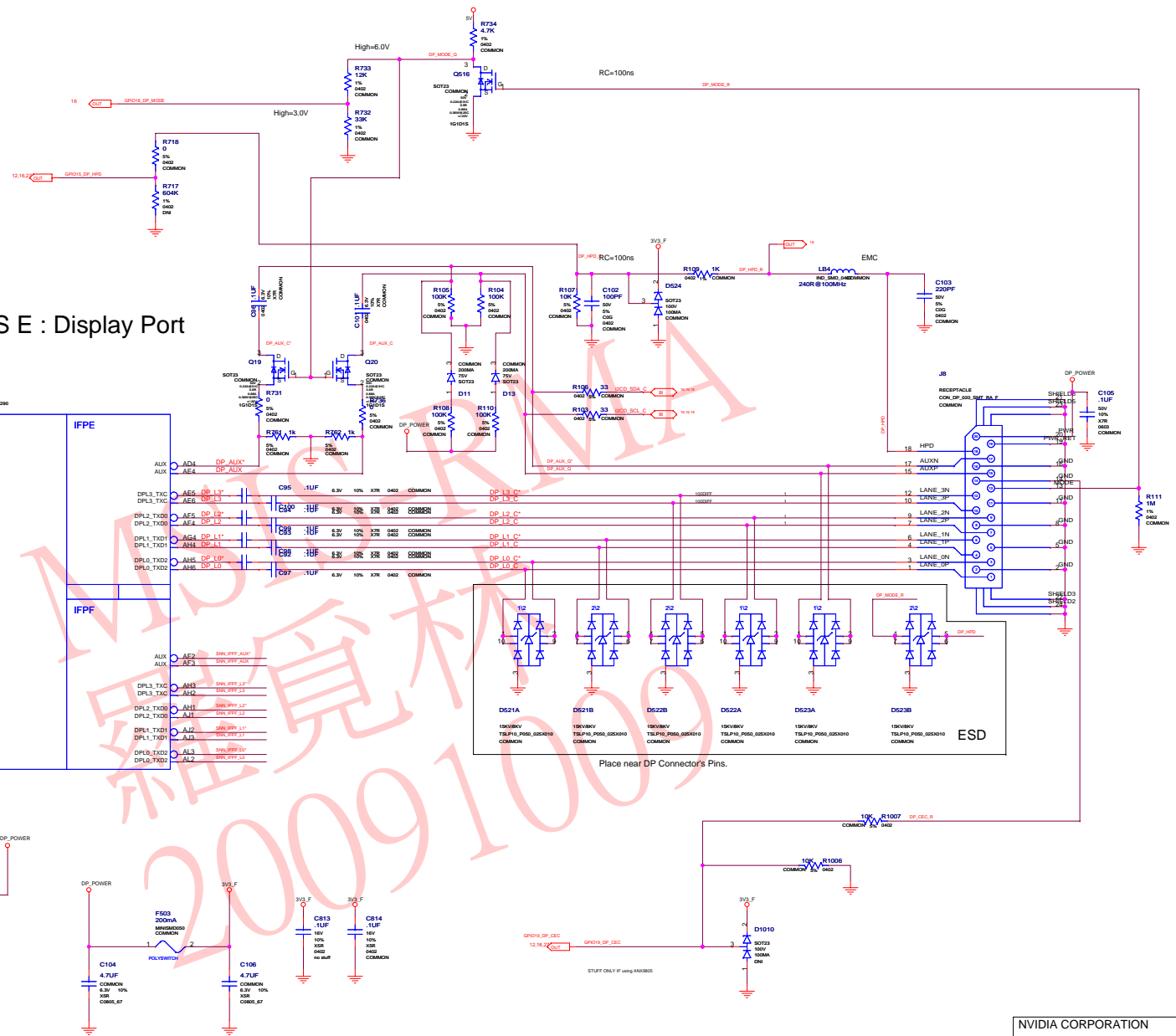


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TMDS LINK: E & F

TMDS E : Display Port



$$V_o = V_{REF} * (1 + (R_{top} / R_{bot})) + I_{adj} * R_{bot}$$

$$3.28V = 1.25V * (1 + (1.58K / 1.00K)) + 55\mu * 1.00K$$

$$3.33V = 1.25V * (1 + (1.62K / 1.00K)) + 55\mu * 1.00K$$

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMD5 LINK C/D, AC COUPLING, PD's, DVI CONNECTOR MID

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