

G94-P545-A01 - GDDR3, DVI/VGA + DVI/VGA + HDTV/SDTV-Out

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	800-10545-000-100	PS46 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SRU010	800-10545-010-100	Q04-400 600MHz/1000MHz 512MB 18MAJ32 BGA138 GDDR3, DVI+DL+DVI+DL+HDTV-Out (Bring Up SRU)
2	SRU020	800-10545-020-100	Q04-400 600MHz/1000MHz 512MB 18MAJ32 BGA138 GDDR3, DVI+DL+DVI+DL+HDTV-Out
3	SRU010	800-10545-010-100	Q04-300 500MHz/800MHz 512MB 18MAJ32 BGA138 GDDR3, DVI+DL+DVI+DL+HDTV-Out
4	SRU020	800-10545-020-100	Q04-200 500MHz/800MHz 384MB 18MAJ32 BGA138 GDDR3, DVI+DL+DVI+DL+HDTV-Out
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V127-0A Base on P545

- 1.PAGE18: ADD Display port circuit  
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10.PAGE 17 CO-LAYOUT HDIM CONNECT  
11.PAGE 15 remove J2 D\_SUB SLIM CONNECT  
12.PAGE 29 ADD CH7322 circuit

V127-20 Base on V127-0A

- 1.PAGE30 .CO-LAYOUT RT9258 circuit

V127-0C Base on V127-20

- 1.PAGE18 remove Display port co-lay circuit  
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PAGE DETAIL	Overview

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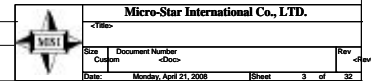
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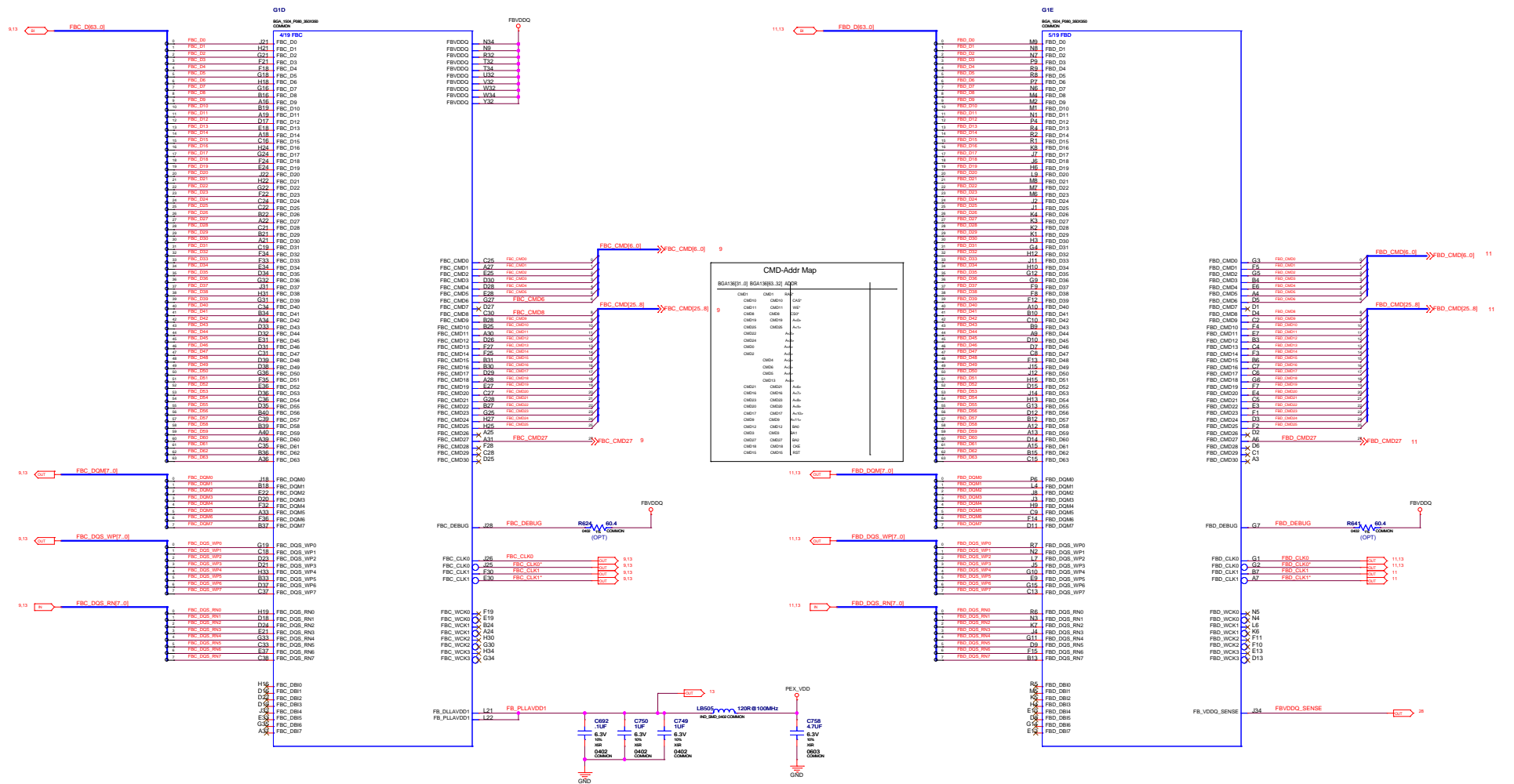
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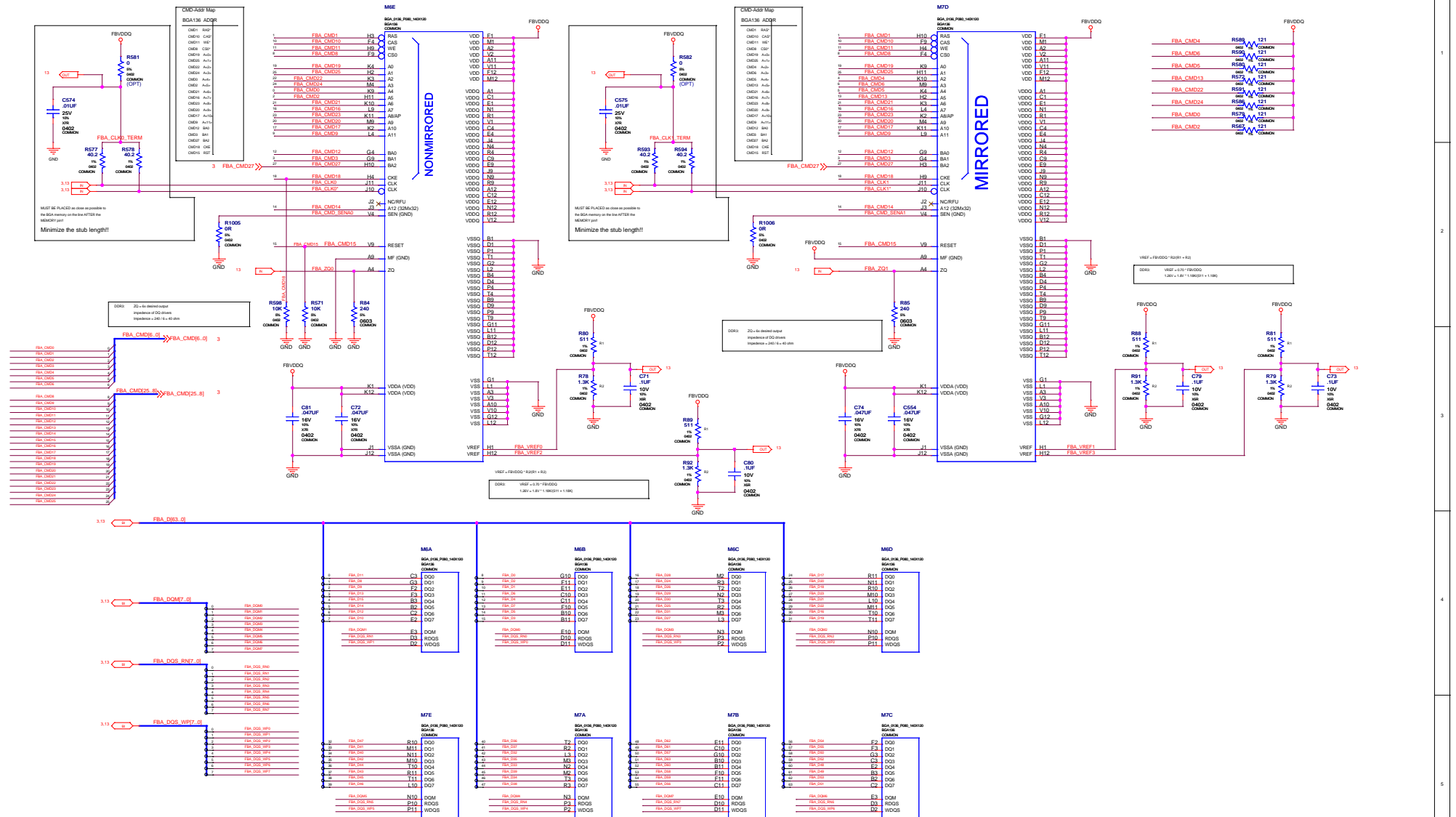
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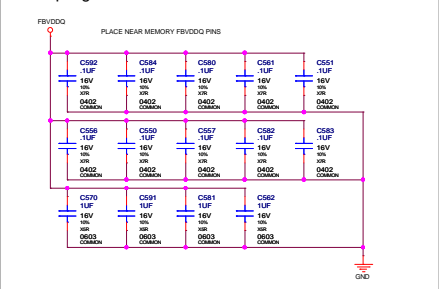


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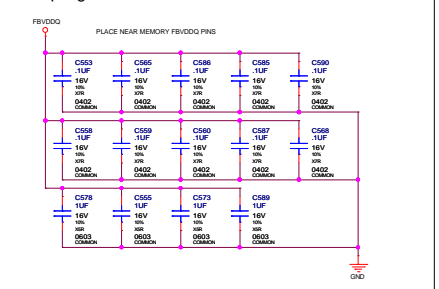
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PS4 BASE 'LEVEL' GENERIC SCHEMATIC ONLY, COMMON I/O, STUFF ASSEMBLY NOTES AND BOARD NOT FRILL  
MEMORY: GPU Partition C/D



Decoupling for FBA 31..0



Decoupling for FBA 63..32



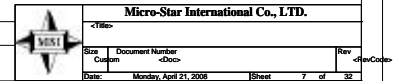
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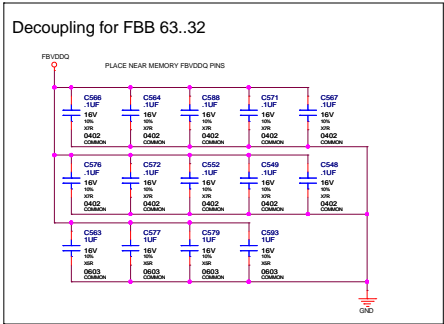
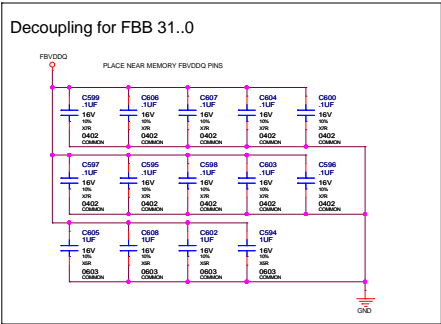
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FBA Partition Decoupling



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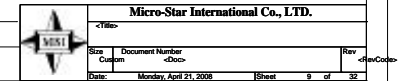
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FBB Partition Decoupling



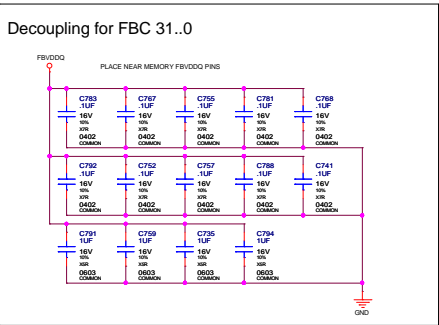
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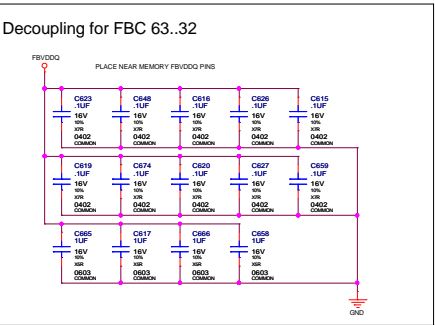




Decoupling for FBC 31..0



Decoupling for FBC 63..32



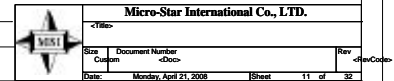
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FBC Partition Decoupling

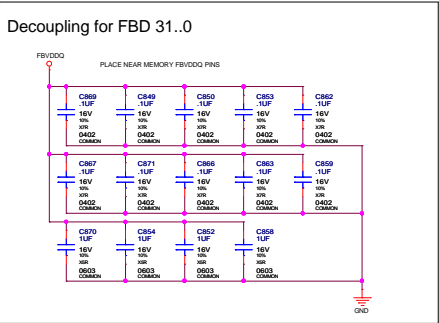


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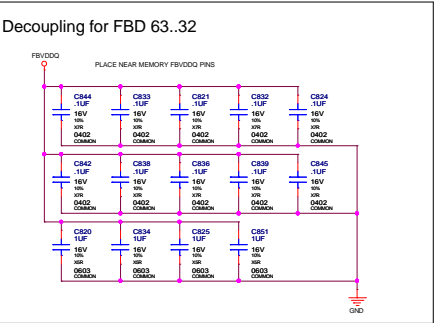
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Decoupling for FBD 31..0



Decoupling for FBD 63..32



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PS40 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL  
FBD Partition Decoupling



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NET RULES for FBA and FBB

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
3.5	FBA_CLK0	1	FBA_CLK0
3.5	FBA_CLK0P	1	FBA_CLK0
5	FBA_CLK0_TERM	1	NOAM
3.5	FBA_CLK1	1	FBA_CLK1
3.5	FBA_CLK1P	1	FBA_CLK1
5	FBA_CLK1_TERM	1	NOAM

NET	NV_CRITICAL_NET	IMPEDANCE
3.5	FBA_DQS_W0P_0	NOAM
3.5	FBA_DQS_W0P_1	NOAM
3.5	FBA_DQS_W0P_2	NOAM
3.5	FBA_DQS_W0P_3	NOAM

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
3.7	FBB_CLK0	1	FBB_CLK0
3.7	FBB_CLK0P	1	FBB_CLK0
7	FBB_CLK0_TERM	1	NOAM
3.7	FBB_CLK1	1	FBB_CLK1
3.7	FBB_CLK1P	1	FBB_CLK1
7.15	FBB_CLK1_TERM	1	NOAM

NET	NV_CRITICAL_NET	IMPEDANCE
3.7	FBB_DQS_W0P_0	NOAM
3.7	FBB_DQS_W0P_1	NOAM
3.7	FBB_DQS_W0P_2	NOAM
3.7	FBB_DQS_W0P_3	NOAM

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
3	FB_PLA000	1.0V	0.02A
3	FB_VREF	1.0V	0.02A
5	FB_VREF0	1.0V	0.02A
5	FB_VREF1	1.0V	0.02A
5	FB_VREF2	1.0V	0.02A
5	FB_VREF3	1.0V	0.02A
5	FBA_Z00	1.0V	0.02A
5	FBA_Z01	1.0V	0.02A
7	FB_VREF0	1.0V	0.02A
7	FB_VREF1	1.0V	0.02A
7	FB_VREF2	1.0V	0.02A
7	FB_VREF3	1.0V	0.02A
7	FBB_Z00	1.0V	0.02A
7	FBB_Z01	1.0V	0.02A

NET RULES for FBC and FBD

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
4.9	FBC_CLK0	1	FBC_CLK0
4.9	FBC_CLK0P	1	FBC_CLK0
9	FBC_CLK0_TERM	1	NOAM
4.9	FBC_CLK1	1	FBC_CLK1
4.9	FBC_CLK1P	1	FBC_CLK1
9	FBC_CLK1_TERM	1	NOAM

NET	NV_CRITICAL_NET	IMPEDANCE
4.9	FBC_DQS_W0P_0	NOAM
4.9	FBC_DQS_W0P_1	NOAM
4.9	FBC_DQS_W0P_2	NOAM
4.9	FBC_DQS_W0P_3	NOAM

NET	NV_CRITICAL_NET	IMPEDANCE	DIFFPAIR
4.11	FBD_CLK0	1	FBD_CLK0
4.11	FBD_CLK0P	1	FBD_CLK0
11	FBD_CLK0_TERM	1	NOAM
3.7	FBD_CLK1	1	FBD_CLK1
3.7	FBD_CLK1P	1	FBD_CLK1
7.15	FBD_CLK1_TERM	1	NOAM

NET	NV_CRITICAL_NET	IMPEDANCE
4.11	FBD_DQS_W0P_0	NOAM
4.11	FBD_DQS_W0P_1	NOAM
4.11	FBD_DQS_W0P_2	NOAM
4.11	FBD_DQS_W0P_3	NOAM

NET	MIN_LINE_WIDTH	VOLTAGE	NV_NET_MAX_CURRENT
4	FB_PLA000	1.0V	0.02A
9	FBC_VREF0	1.0V	0.02A
9	FBC_VREF1	1.0V	0.02A
9	FBC_VREF2	1.0V	0.02A
9	FBC_VREF3	1.0V	0.02A
9	FBC_Z00	1.0V	0.02A
9	FBC_Z01	1.0V	0.02A
11	FBD_VREF0	1.0V	0.02A
11	FBD_VREF1	1.0V	0.02A
11	FBD_VREF2	1.0V	0.02A
11	FBD_VREF3	1.0V	0.02A
11	FBD_Z00	1.0V	0.02A
11	FBD_Z01	1.0V	0.02A

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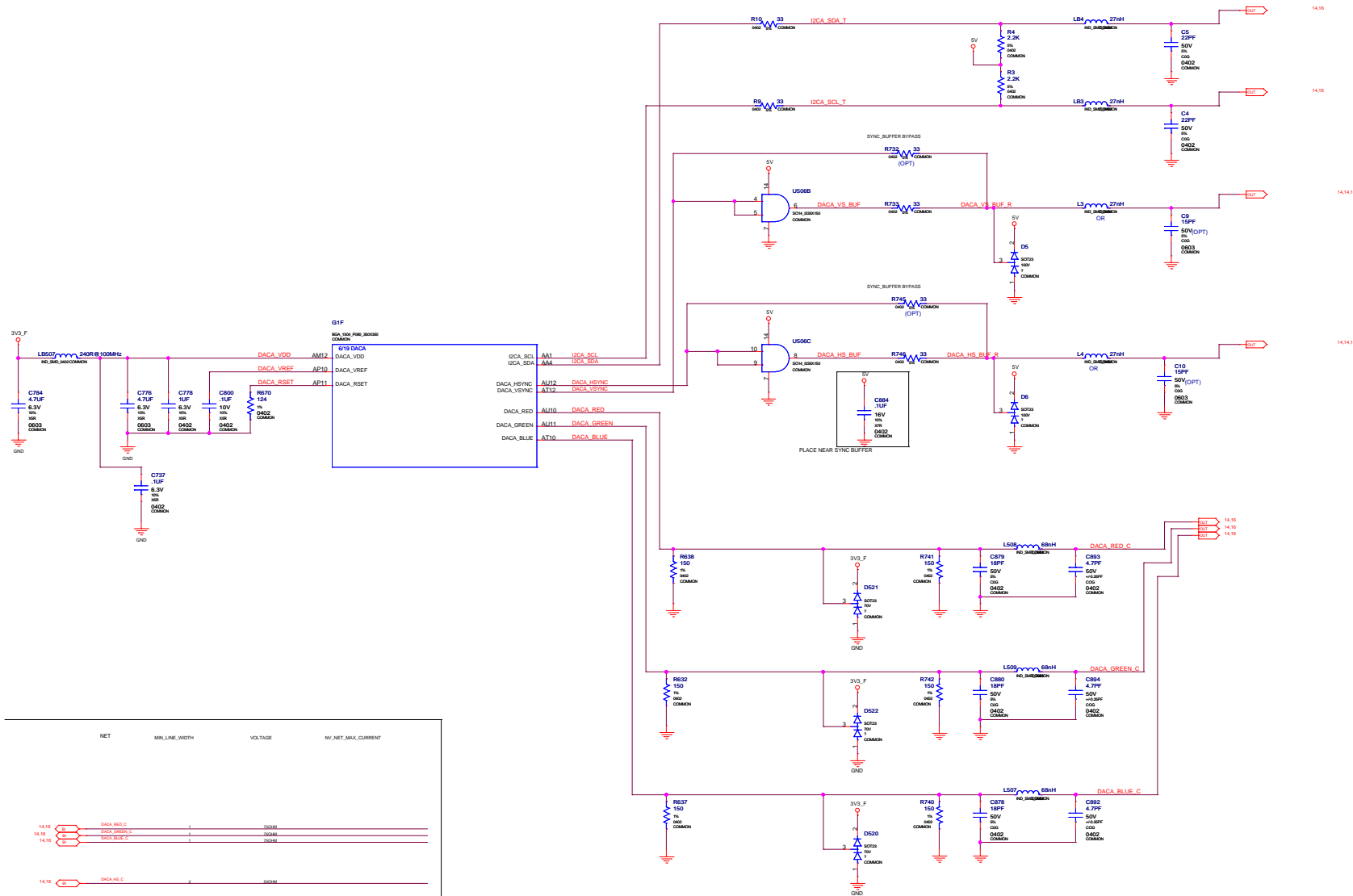
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FB Net Properties



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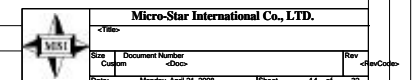
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## DACA RGB-FILTER

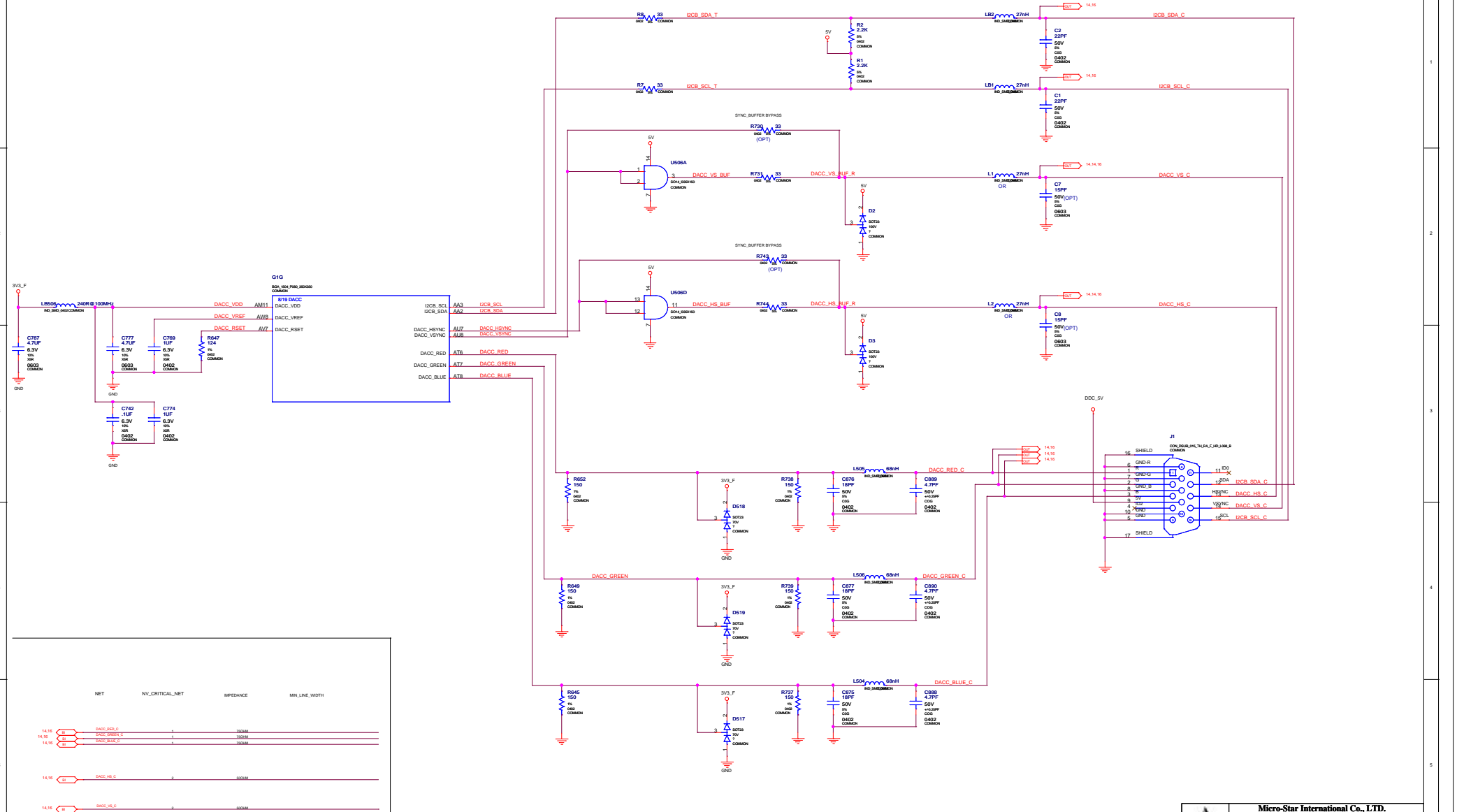


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14.10	DHCA_WG_0	2	200mV	
14.10	DHCA_WG_0	2	200mV	

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## DACC RGB-FILTER



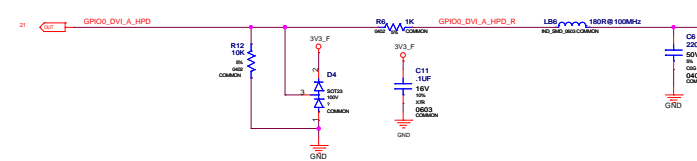
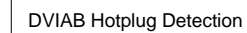
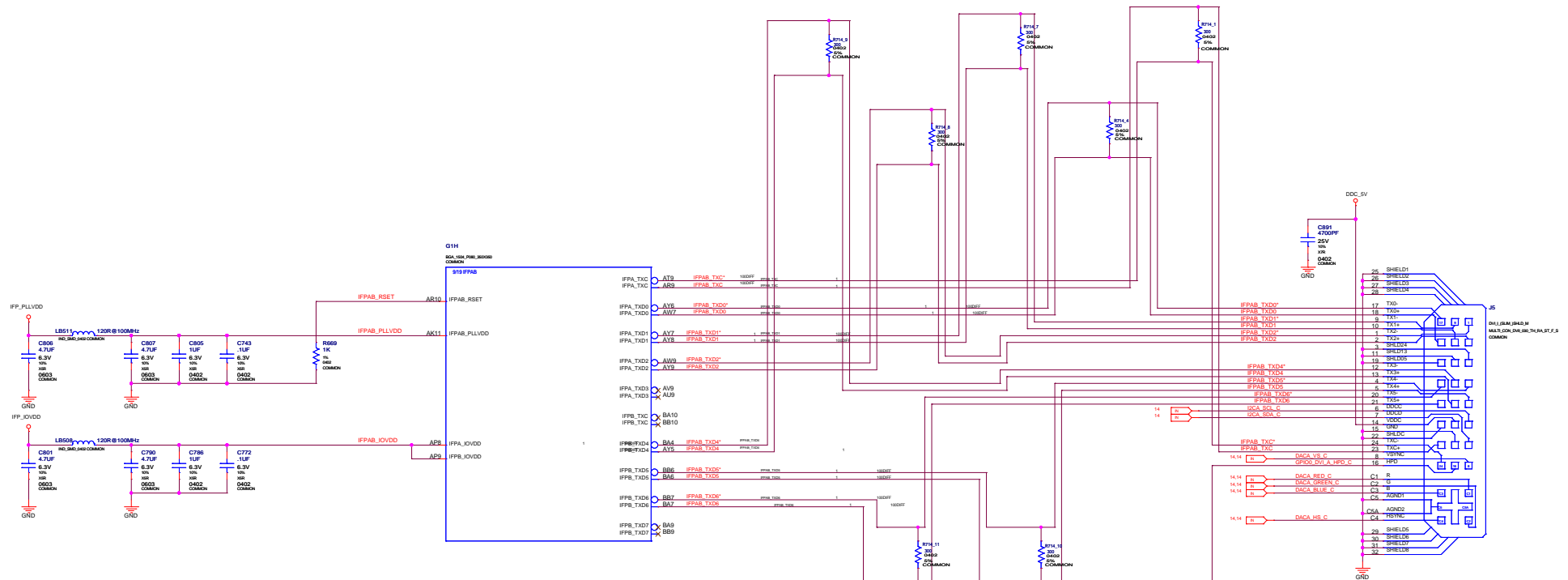
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PAGE DETAIL	DACC Interface



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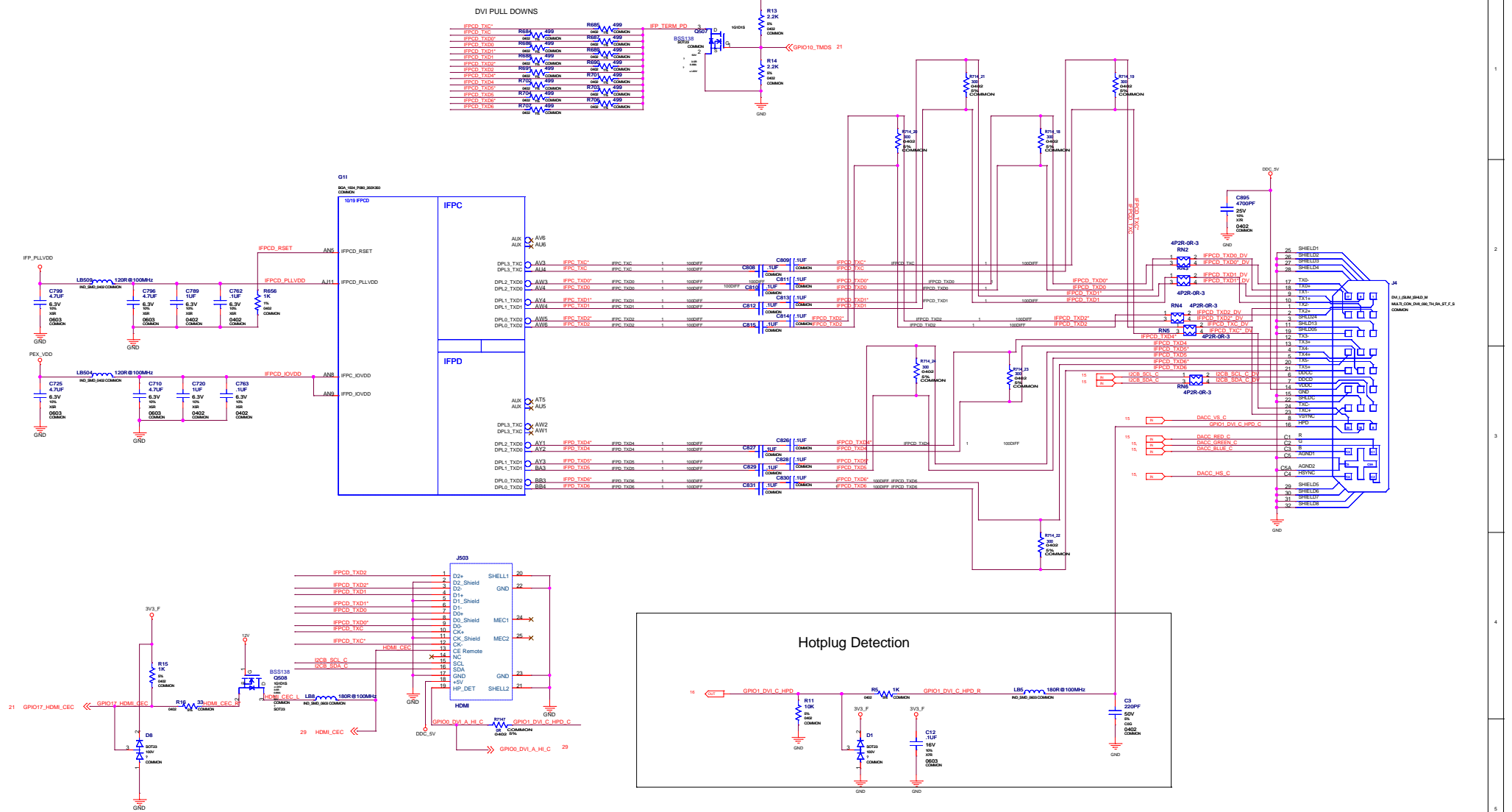
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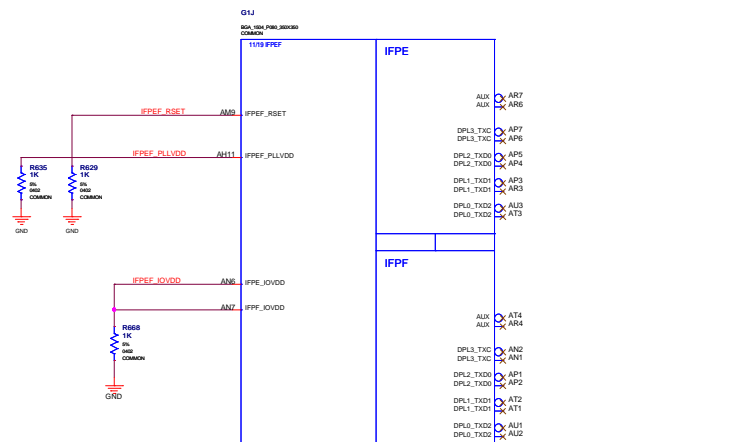


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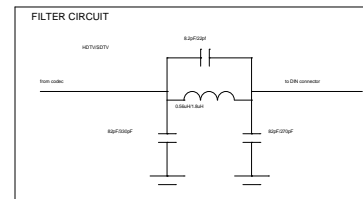
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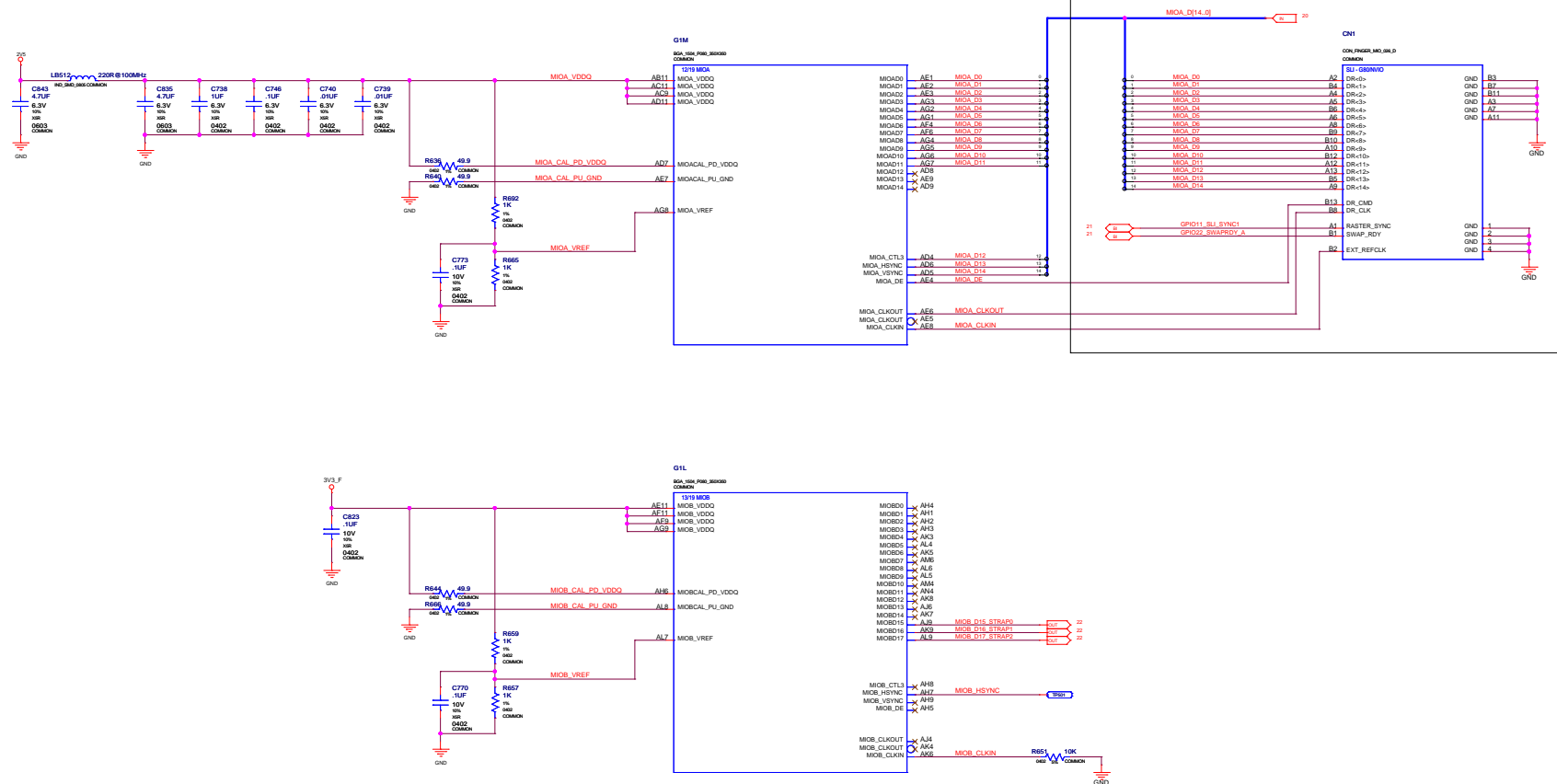


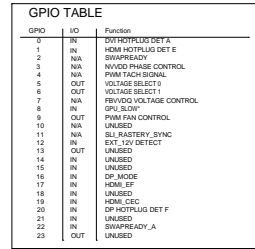
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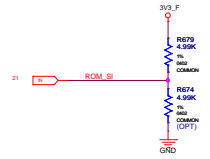


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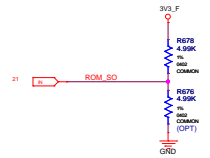


## Page22: Strap Configuration

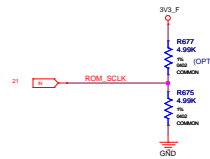


STRAP PIN	STRAP NAME
ROM_SI	PCI_DEVID_EXT

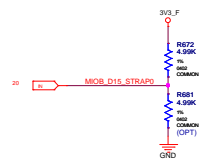
3V3		GND	
5K	1	0	0



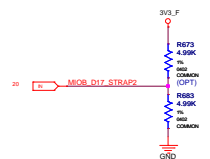
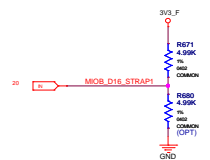
STRAP PIN	STRAP NAME
ROM_SO	SLOT_CLK_CFG



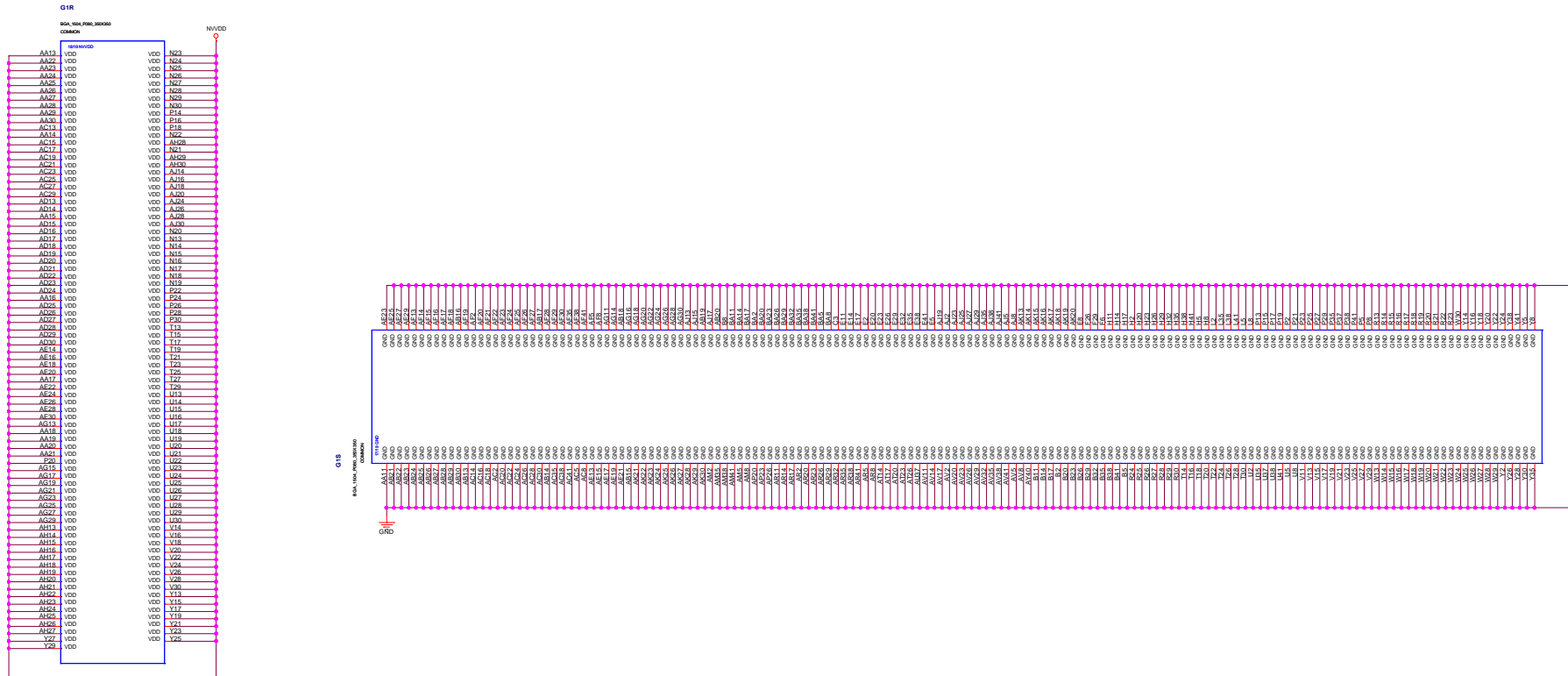
STRAP PIN	STRAP NAME
ROM_SCLK	PCI_DEVID[3]

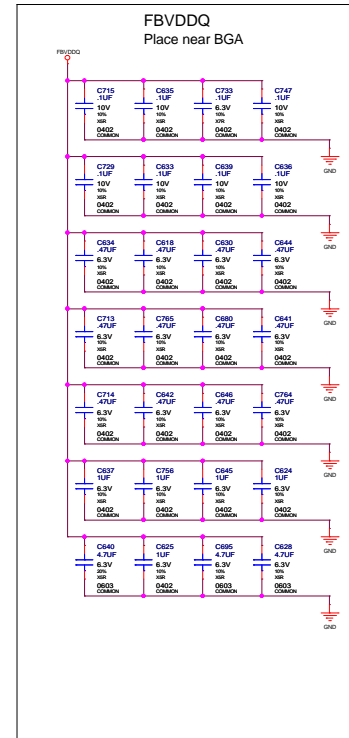
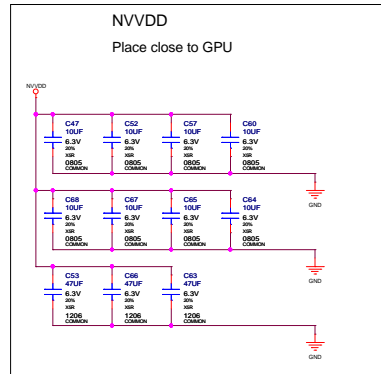
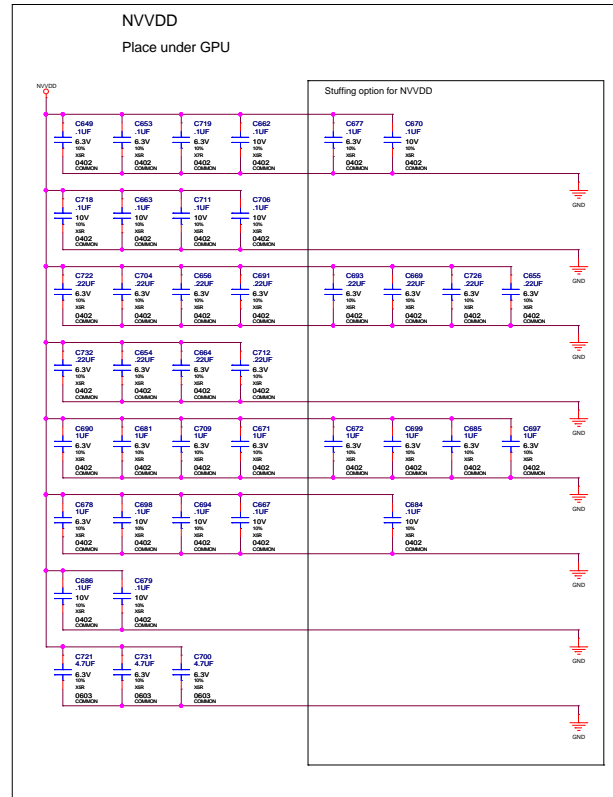


<b>STRAP PIN</b>	<b>STRAP NAME</b>	
STRAP0	RAMCFG0	
		* RAMCFG[2:0]
		256MB (8Mx32)
		101 --- 256-bit Omron 110 --- 256-bit Hynix 111 --- 256-bit Samsung
		512MB (16Mx32)
		001 --- 256-bit Omron 010 --- 256-bit Hynix 011 --- 256-bit Samsung
		1024MB (32Mx32)
		101 --- 256-bit Hynix 110 --- 256-bit Hynix 111 --- 256-bit Samsung
		* VBIOSS will be defined on a per SKU basis.
<b>STRAP PIN</b>	<b>STRAP NAME</b>	
STRAP1	RAMCFG1	
<b>STRAP PIN</b>	<b>STRAP NAME</b>	
STRAP2	RAMCFG2	

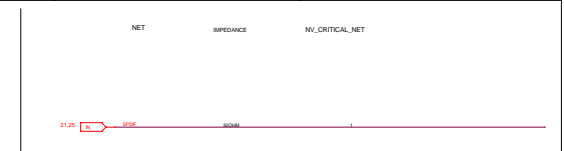


SGLA - SGLA PUBLI - SERVIZIO COORDINATO	
1	INIZIARE
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC
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100	NC

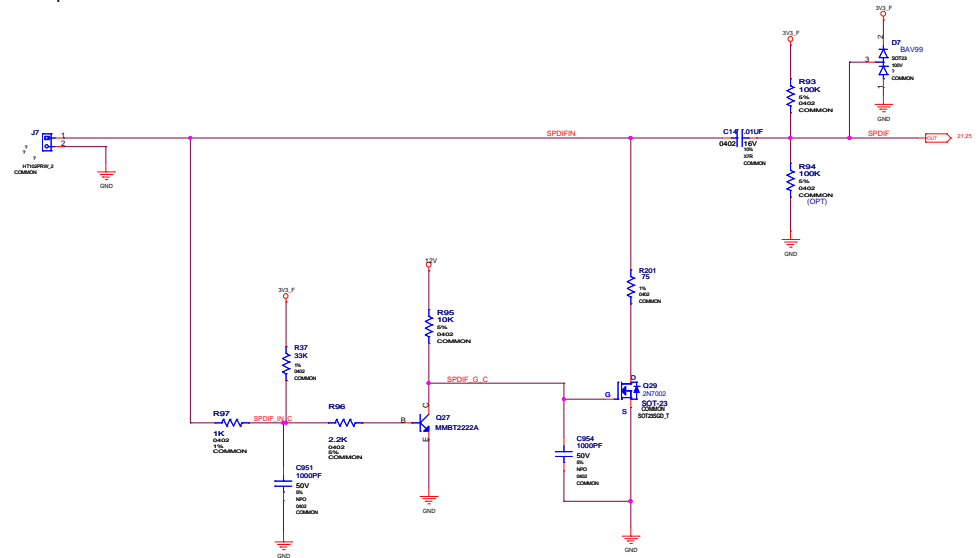




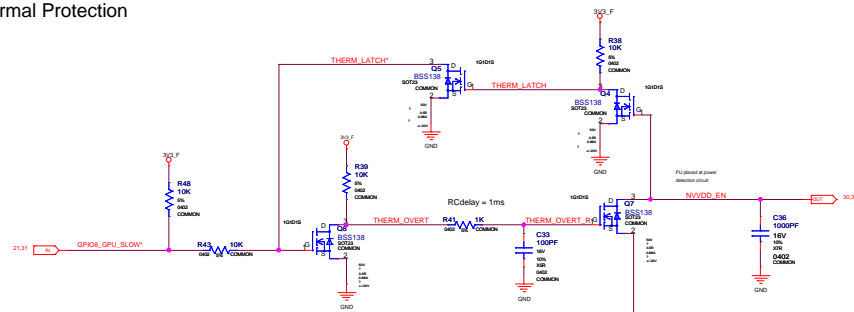




## SPDIF Input

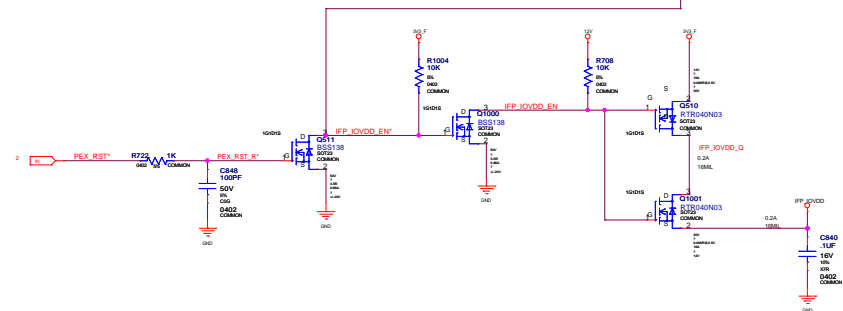


## Thermal Protection

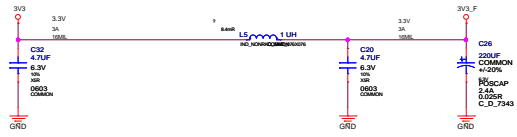


## IFP\_IOVDD Backdrive Prevention

Stuffing possibilities for thermal control and protection:



3V3\_F = 3.3V @ 2.5A



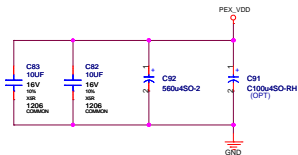
12V\_F = 12V @ 5.5A



12V\_EXT\_F = 12V @ 6.25A

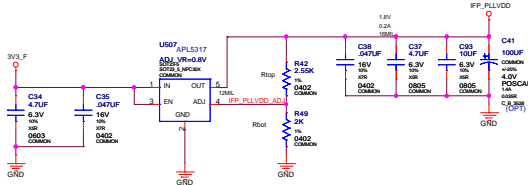
[illegible]

	GPIO12
EMERGENCY MODE (VUV_EXT present)	0
150W POWER MODE (VUV_EXT NOT present)	1



### IFP\_PLLVDD Power Supply

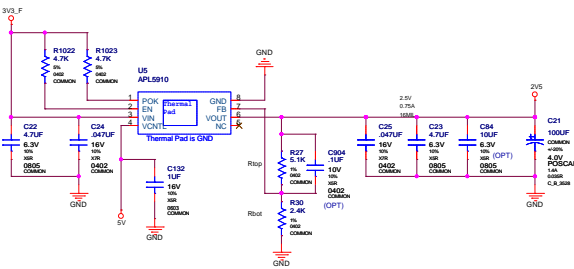
IFP\_PLLVDD = 1.8V @ 200mA



$$\text{IFP\_PLLVDD} = \text{VREF} * (1 + (\text{Rtop} / \text{Rbot}))$$
$$1.82\text{V} = 0.8\text{V} * (1 + (2.5\text{K} / 2\text{K}))$$

### 2V5 Power Supply

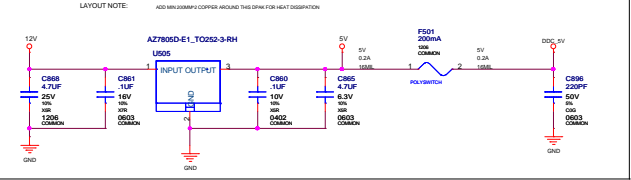
2V5 = 2.5V @ 750mA



$$2\text{V5} = \text{VREF} * (1 + (\text{Rtop} / \text{Rbot}))$$
$$2.5\text{V} = 0.8\text{V} * (1 + (5.1\text{K} / 2\text{K}))$$

### 5V and DDC\_5V Power Supply

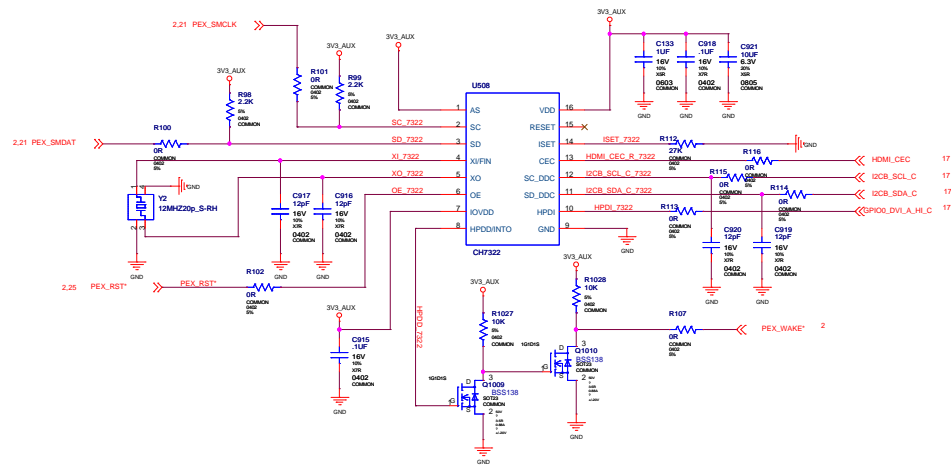
DDC\_5V = 5V @ 200mA



ASSEMBLY PAGE DETAIL PS40 BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NC STUFF ASSEMBLY NOTES AND BOM NOT FINAL PS II: IFP\_VDD, IFP\_PLLVDD, 2V5, 5V, and DDC\_5V Power Supply

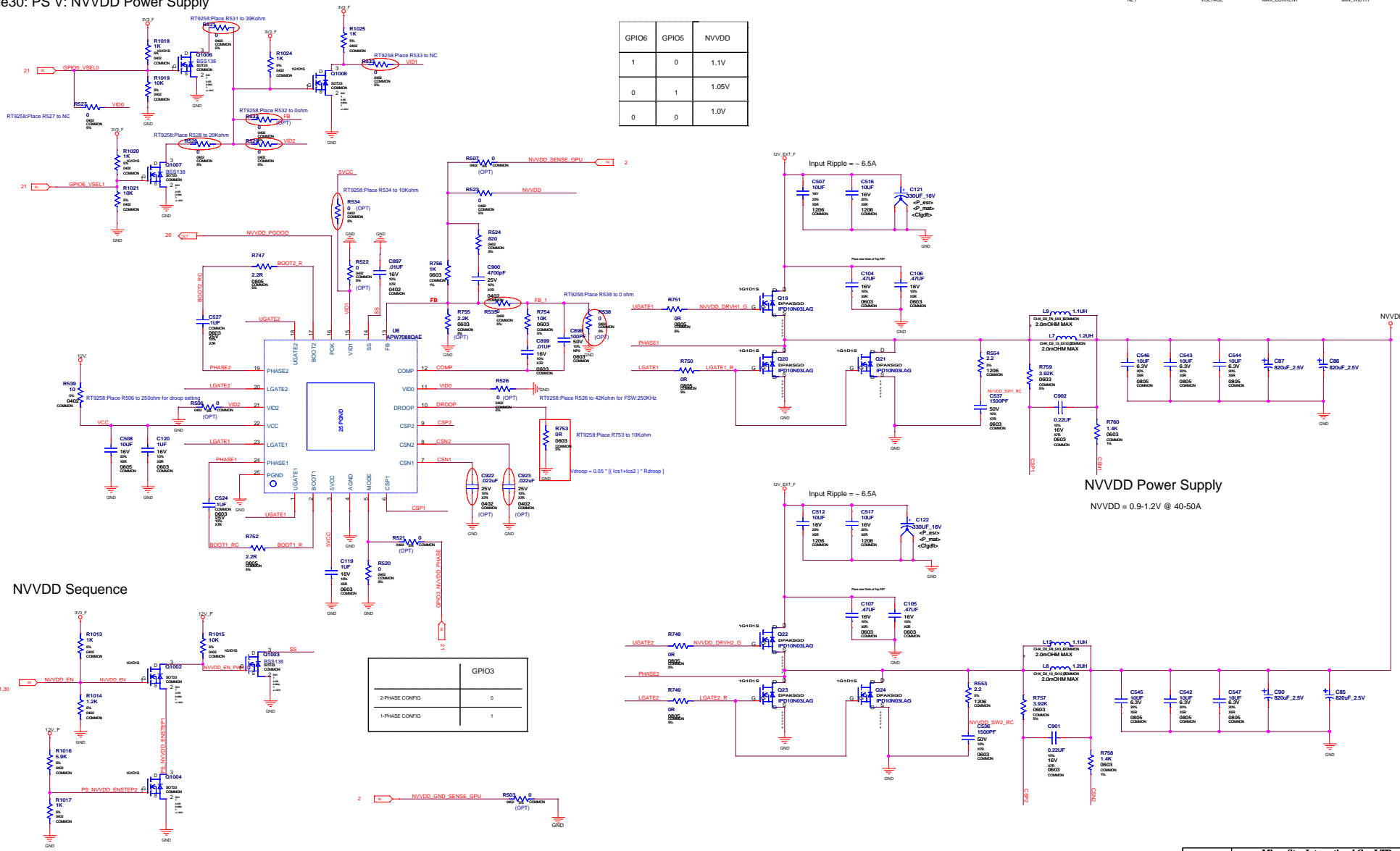
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NVDD Voltage Select		
NVDD range 0.80V-1.40V		
Regulator: ADP7025		
Control via NV_GPCLKV_NV_VSEL2[1:0]		
VID	NVDD	Q94
6 5 4 2 1 0	Vout	
0 1 1 1 0 0	0.80V	
0 1 1 0 1 0	0.85V	
0 1 1 0 0 0	0.90V	
0 1 0 1 1 0	0.95V	
0 1 0 1 0 0	1.00V	=> Default
0 1 0 0 1 0	1.05V	=> Voltage1
0 1 0 0 0 0	1.10V	
0 0 1 1 1 0	1.15V	=> Voltage2
0 0 1 1 0 0	1.20V	
0 0 1 0 1 0	1.25V	
0 0 1 0 0 0	1.30V	
0 0 0 1 1 0	1.35V	
0 0 0 1 0 0	1.40V	

GPI06	GPI05	NVDD
1	0	1.1V
0	1	1.05V
0	0	1.0V



**NVVDD Power Supply**  
NVVDD = 0.9-1.2V @ 40-50A

	GPIO3
2-PHASE CONFIG	0
1-PHASE CONFIG	1

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PAGE DETAIL	PS V: NVCC Power Supply

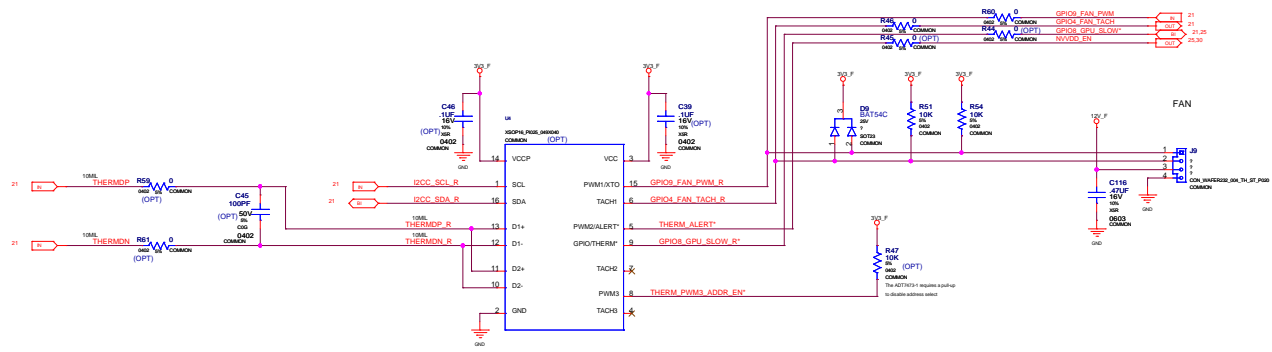
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ADT7473 External Fan/Thermal Control



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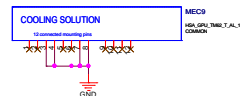
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PAGE DETAIL  
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Thermal Diode and Fan Control



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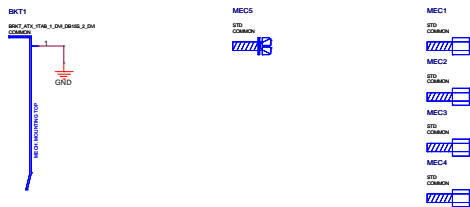
Thermal



Mechanical



Bracket



FOR EMI



FOR EMI



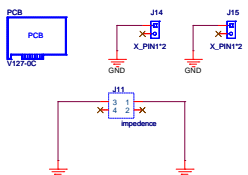
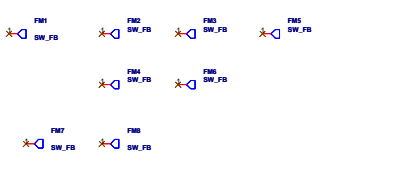
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