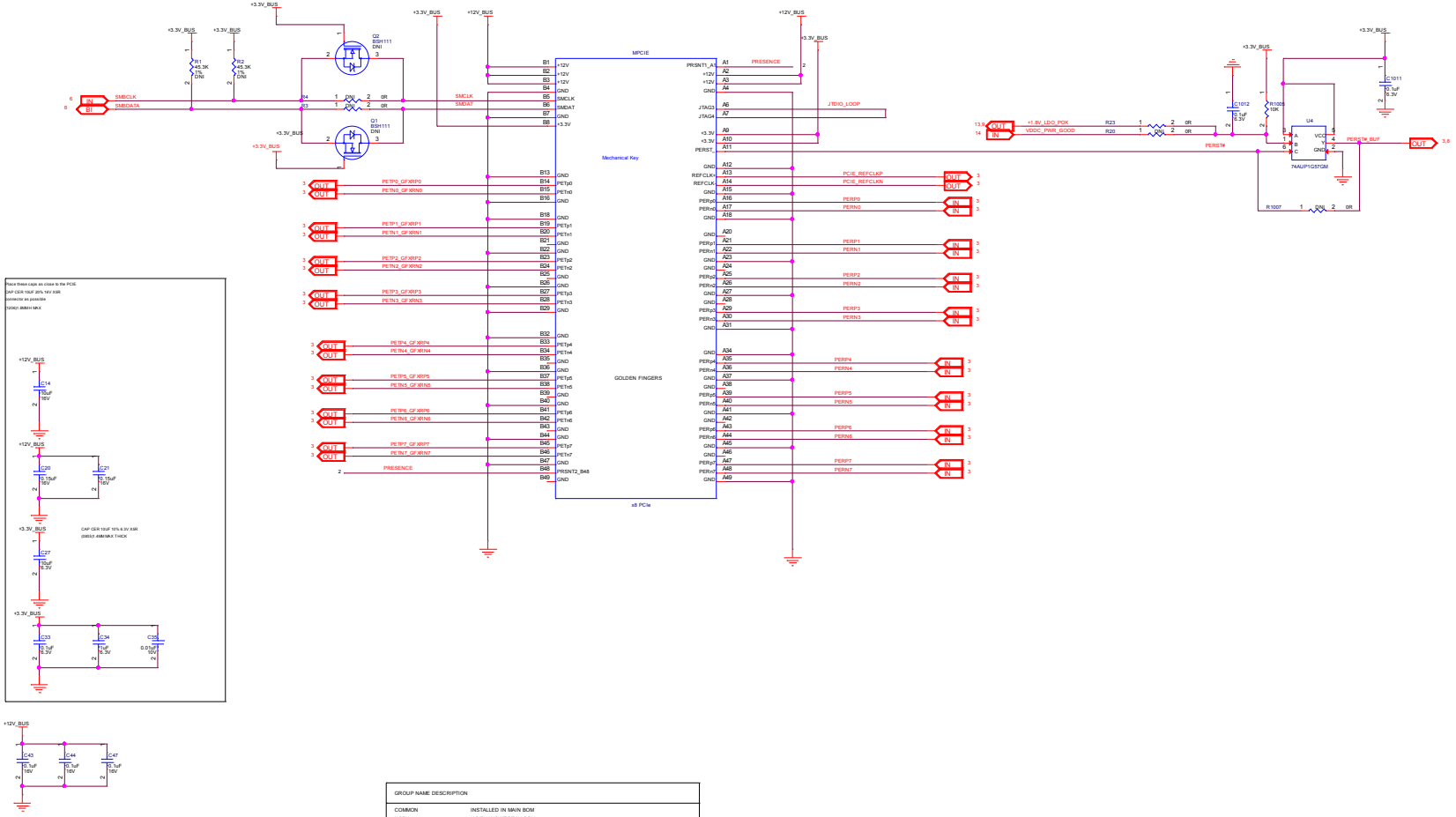
TABLE OF CONTENTS

GROUP NAME	DESCRIPTION
COMMON	INSTALLED IN MAIN BOM
NOPN	NO PN,WON'T BE IN BOM
DNI	DON'T INSTALL
INT	INTERNAL BOM, WON'T BE IN PRODUCTION BOM
GPU	GPU PN
BK	BRACKET
HS	HEATSINK OR FANSINK
BACO	BACO circuit
SUBBOM	SUBBOM PN
2ND SOURCE	
ALT	ALTERNATIVE PN(FORMAT:ALT=ALT[PN1;PN2;...)
SUB BOM	
MEM	MEMORY SUB BOM
DEBUG	DEBUG SUB BOM
POWER SUB BOM	
VDDC	VDDC SUB BOM
VDDCI	VDDCI SUB BOM
MVDD	MVDD SUB BOM
095	0.95V SUB BOM
1V8	1.8V SUB BOM

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET:	TOC AND BOM GROUP
DATE:	Thu Feb 04 02:22:45 2016
REV:	1.0
SHEET NUMBER:	1 OF 17
DOCUMENT NUMBER:	105_D03400_00A
NOTES:	NOTE
TITLE:	BANKS DT

PCI-EXPRESS EDGE CONNECTOR



GROUP NAME	DESCRIPTION
COMMON	INSTALLED IN MAIN BOM
NOPN	NO PN,WON'T BE IN BOM
DNI	DON'T INSTALL
INT	INTERNAL BOM, WON'T BE IN PRODUCTION BOM
GPU	GPU PN
SUBBOM	SUBBOM PN
2ND SOURCE	
ALT	ALTERNATIVE PN(FORMAT:ALT+ALT(PN1;PN2;...))
POWER SUB BOM	
VDDC	VDDC SUB BOM
MVDD	MVDD SUB BOM
095	0.95V SUB BOM
1V8	1.8V SUB BOM
DEBUG	DEBUG SUB BOM

SYMBOL LEGEND

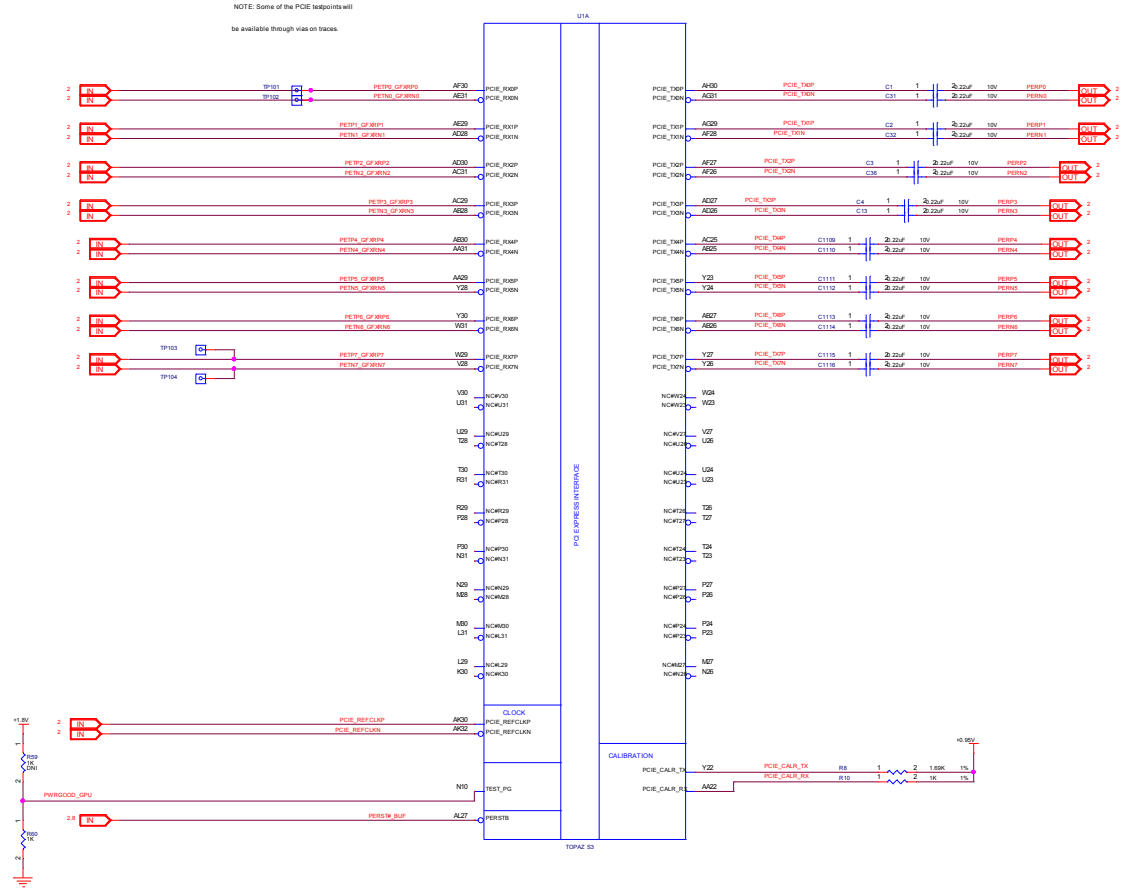
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
EUO	BRING UP ONLY

LED GREEN "ON" shows PX_EN

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

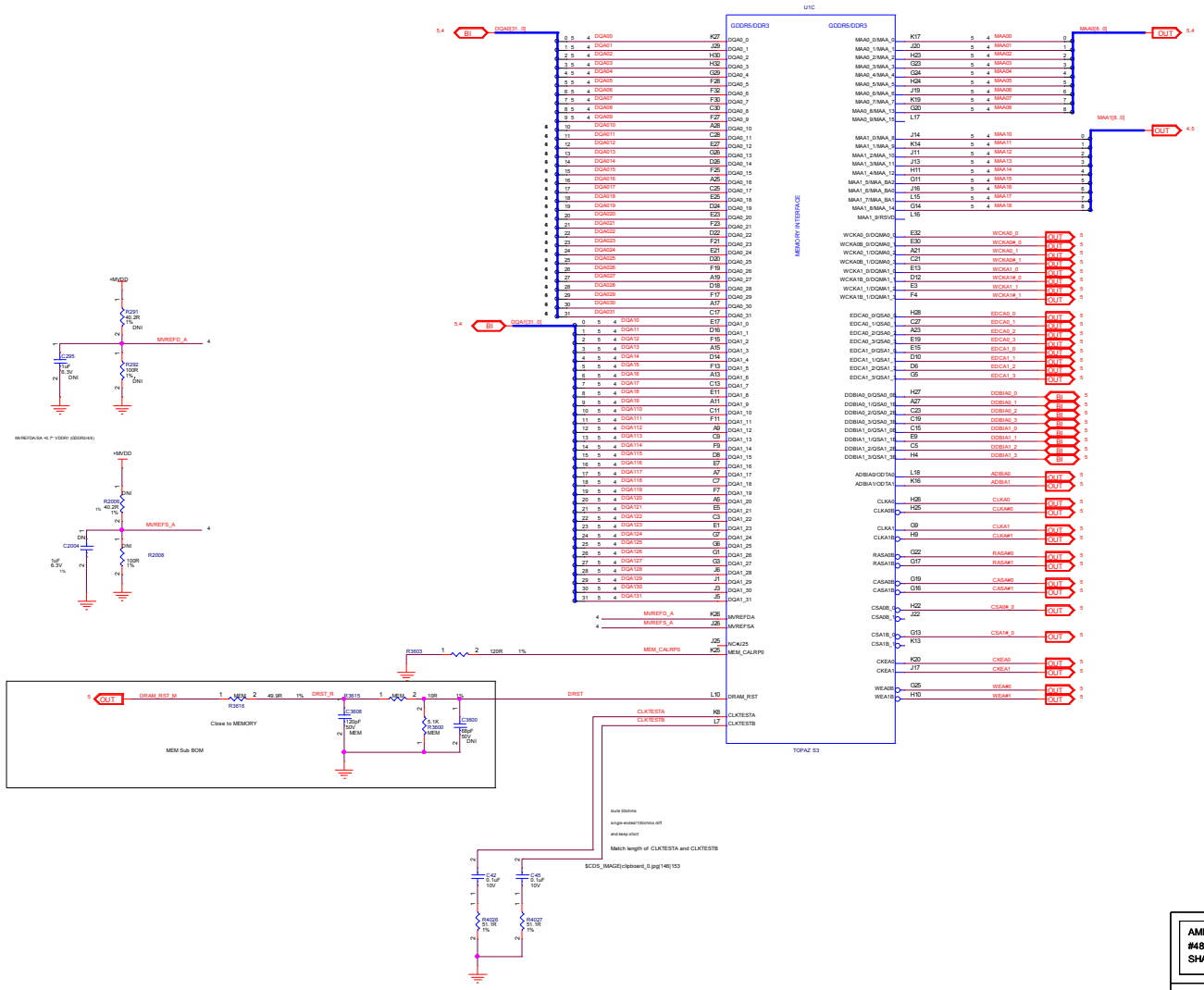
SHEET:	PCI-E Edge Connector		
DATE:	Thu Feb 04 02:22:45 2016	REV:	1.0
SHEET NUMBER:	2 OF 17		
DOCUMENT NUMBER:	105_D03400_00A		
TITLE:	BANKS DT		

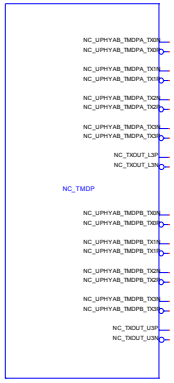
PCIe Interface



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. © 2016 Advanced Micro Devices This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.
SHEET: PCIEx8 Interface	
DATE: Thu Feb 04 02:22:46 2016	REV: 1.0
SHEET NUMBER: 3 OF 17	TITLE: BANKS DT
DOCUMENT NUMBER: 105_D03400_00A	

MEM Interface Ch A

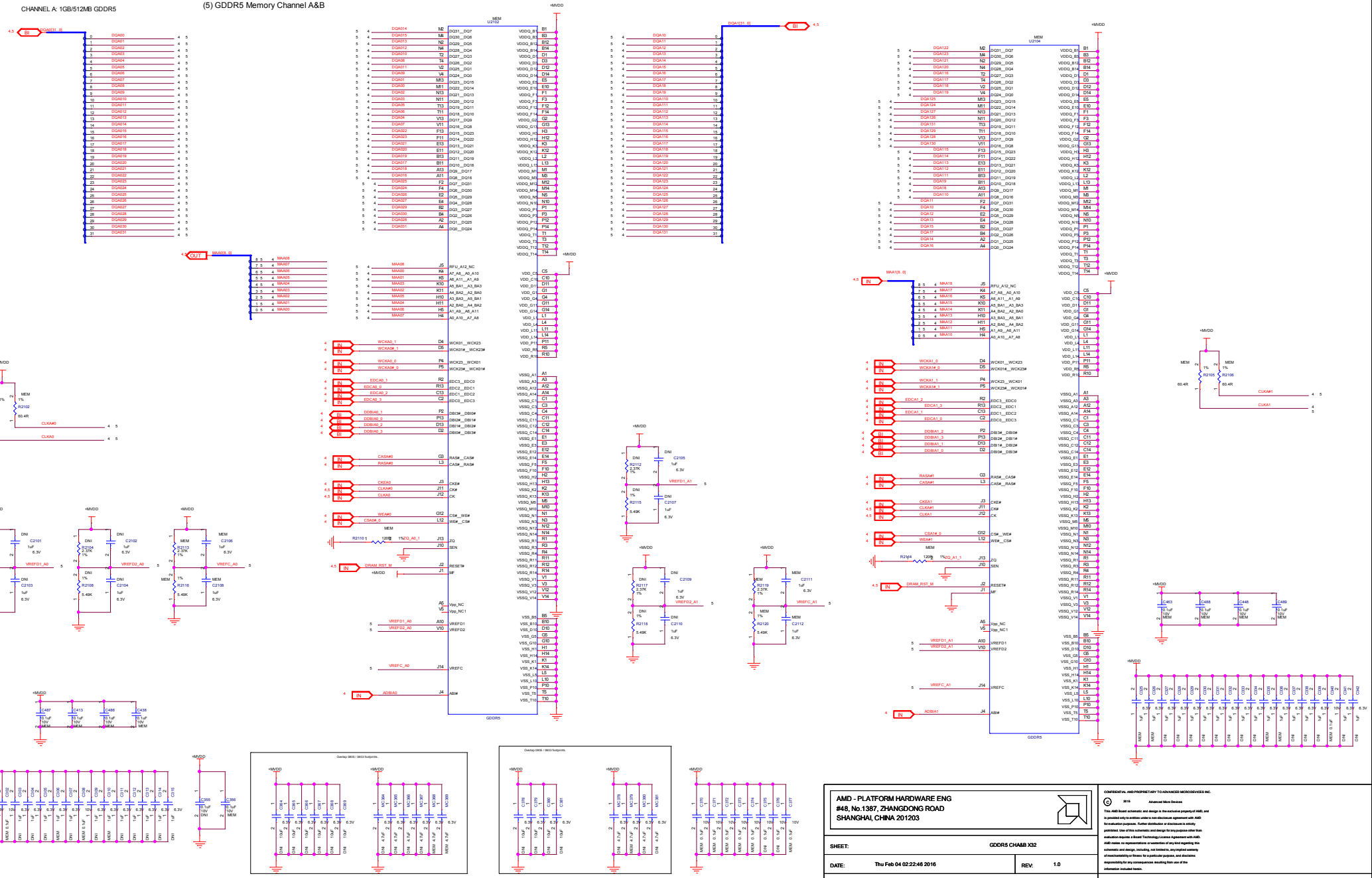




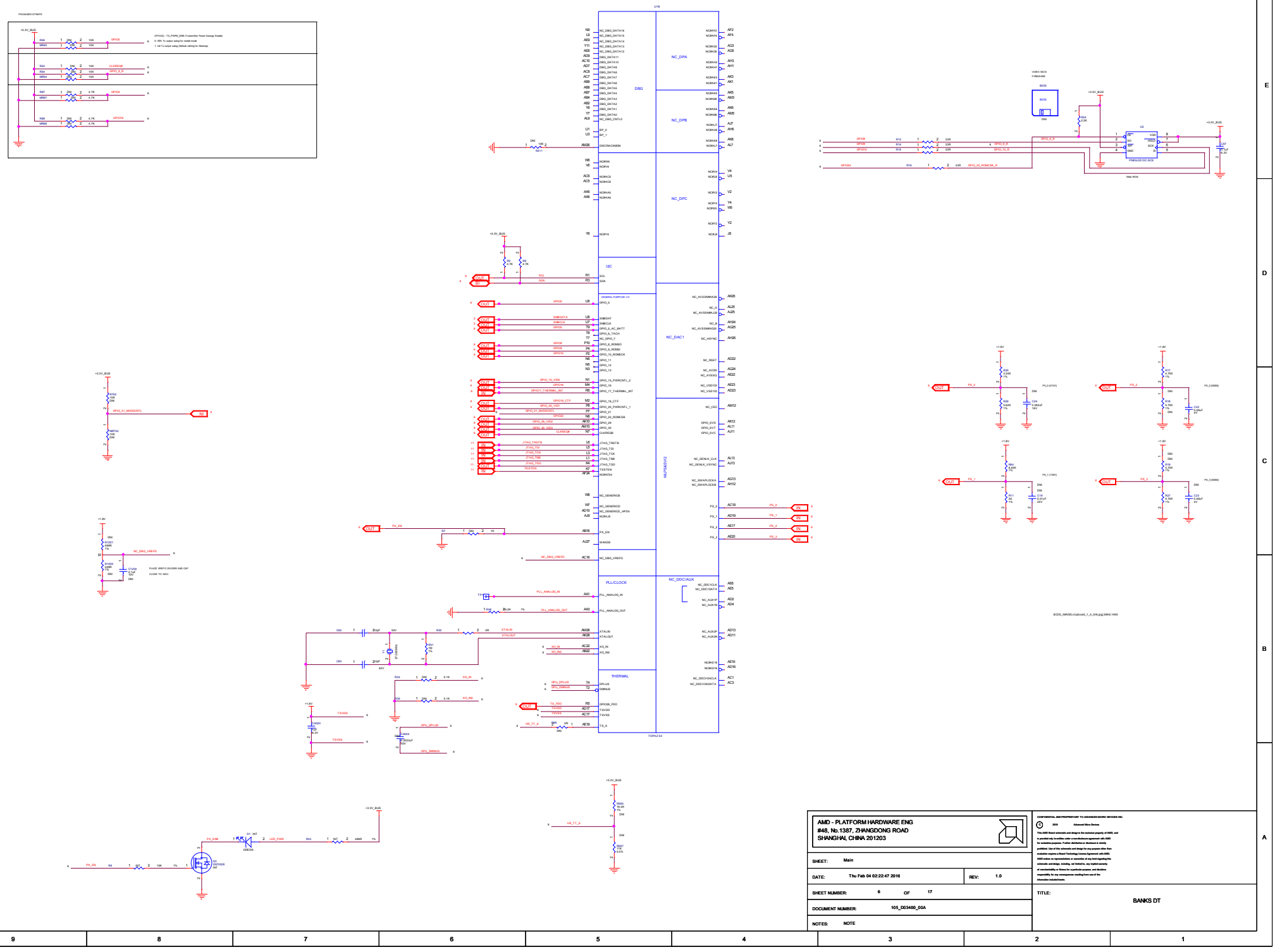
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: MEM Interface	
DATE: Thu Feb 04 02:22:46 2016	REV: 1.0
SHEET NUMBER: 4 OF 17	TITLE: BANKS DT
DOCUMENT NUMBER: 105_D03400_00A	

CHANNEL A: 1GB/512MB GDDR5

(5) GDDR5 Memory Channel A&B



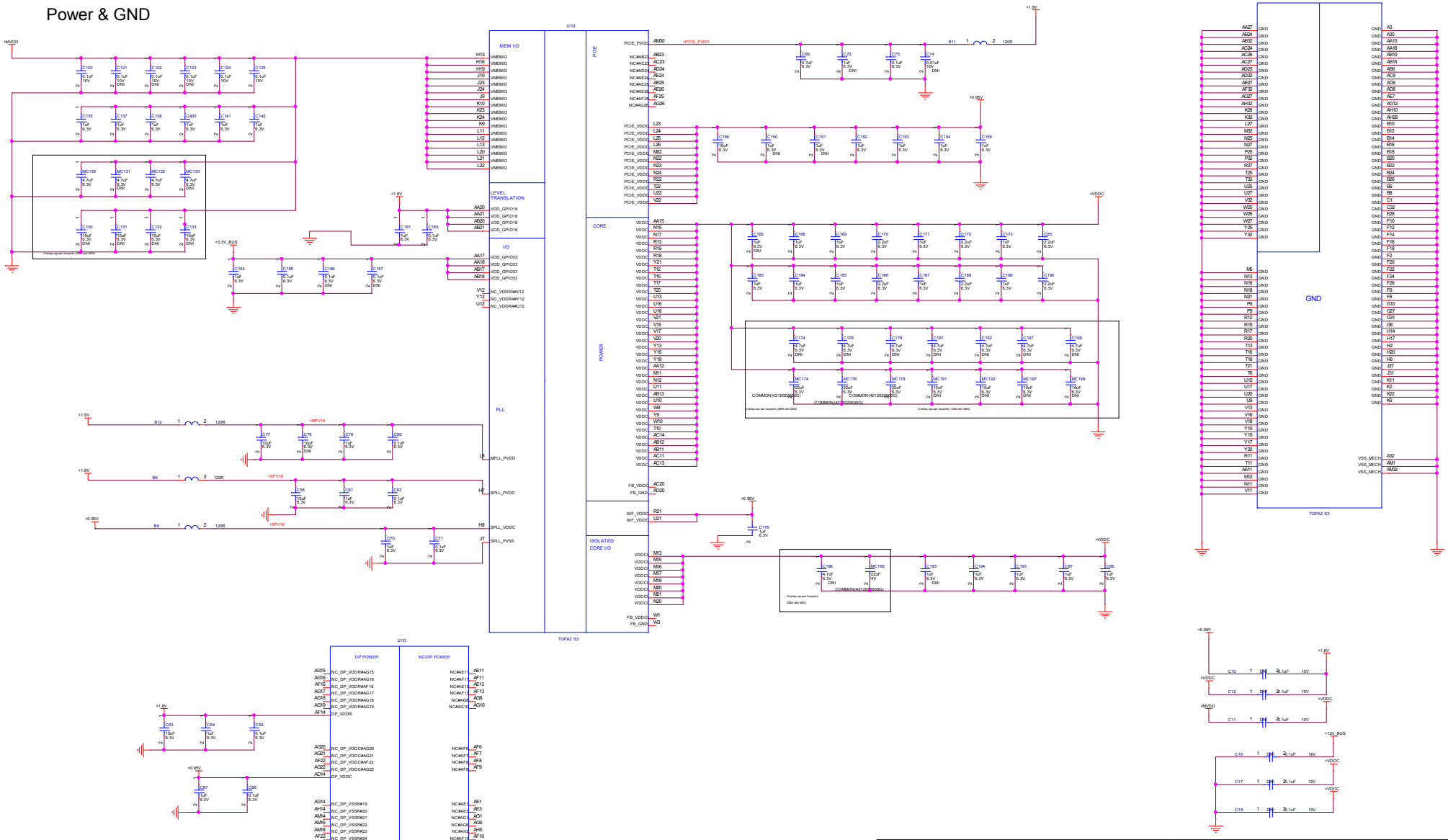
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET:	GDDR5 CHA&B X32
DATE: Thu Feb 04 02:22:46 2016	REV: 1.0
SHEET NUMBER: 5 OF 17	TITLE: BANKS DT
DOCUMENT NUMBER: 105_D03400_00A	



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: Main	
DATE: Thu Feb 04 02:22:47 2016	REV: 1.0
SHEET NUMBER: 6 OF 17	
DOCUMENT NUMBER: 105_D03400_00A	
NOTES: NOTE	

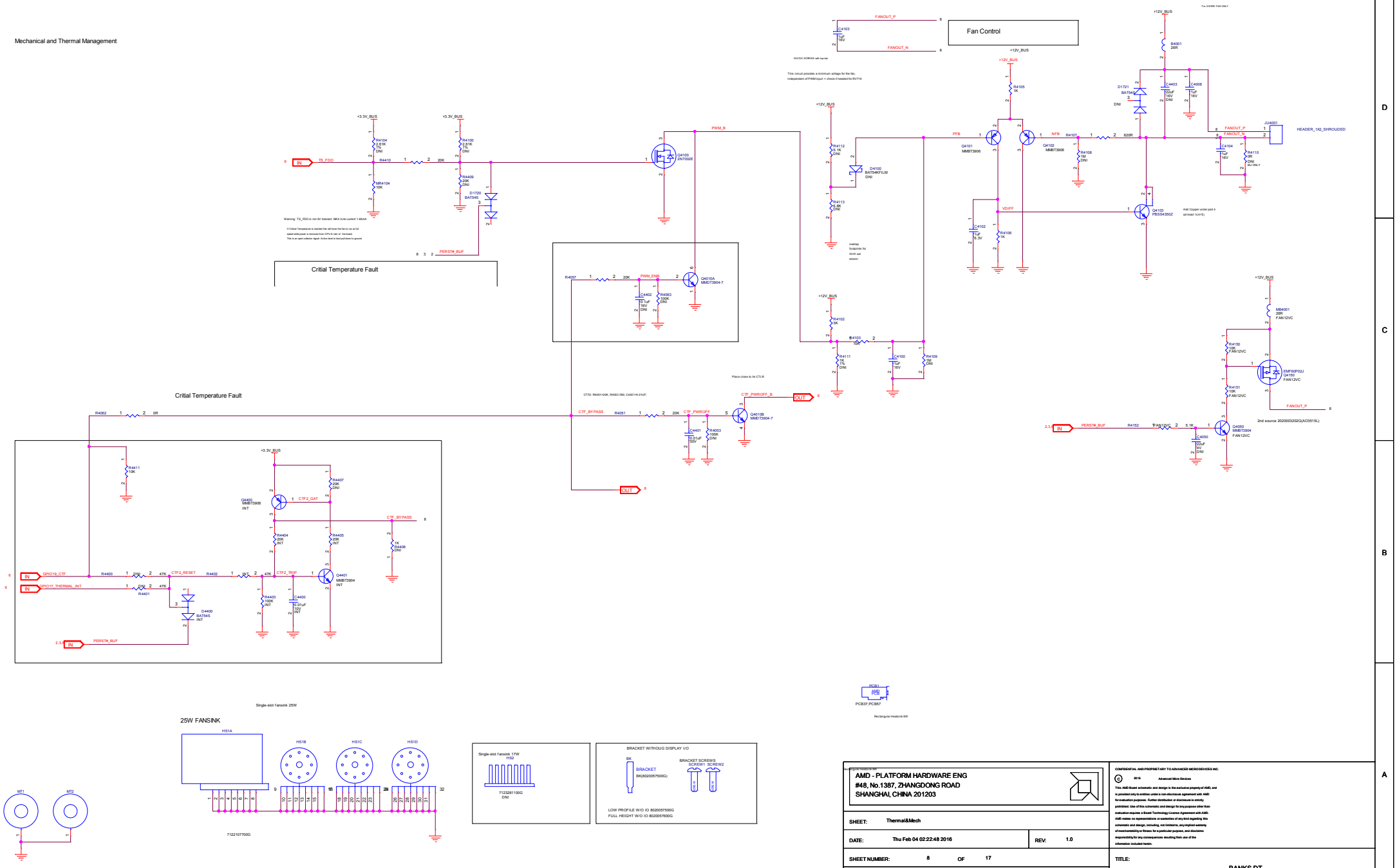
TITLE: BANKS DT

Power & GND



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: Power&GND	
DATE: Thu Feb 04 02:22:47 2016	REV: 1.0
SHEET NUMBER: 7 OF 17	
DOCUMENT NUMBER: 105_D03400_00A	TITLE: BANKS DT

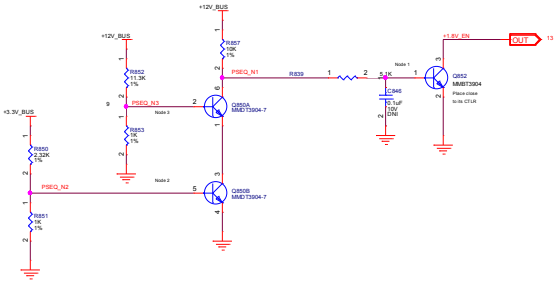
Mechanical and Thermal Management

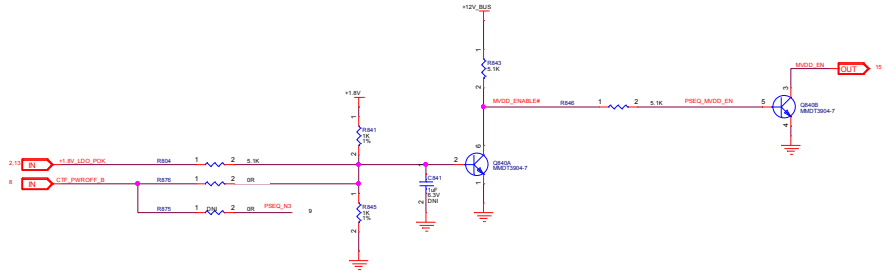


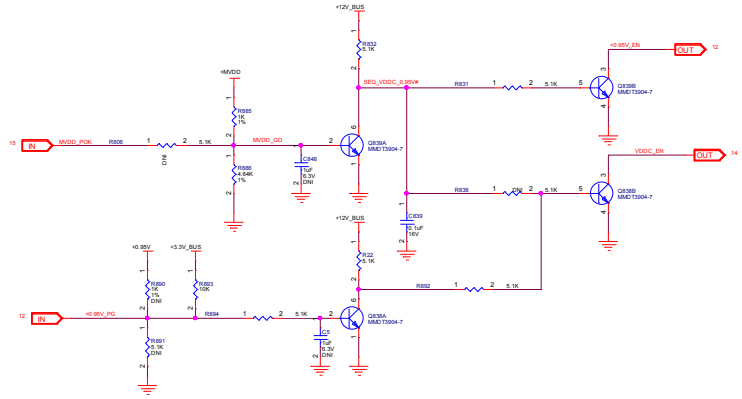
Power Management - Power Gating and Dynamic Voltage Control

POWER SEQUENCE
+1.8V->MVDD->0.95V->VDDC
0.95V must ramp up before VDDC

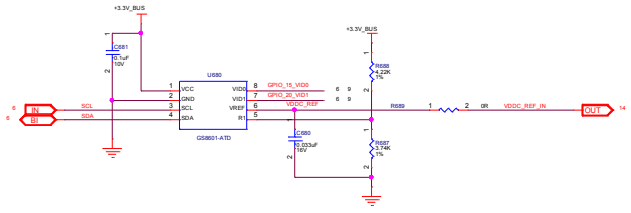
Don't support BACO
Support CTF(Internal)





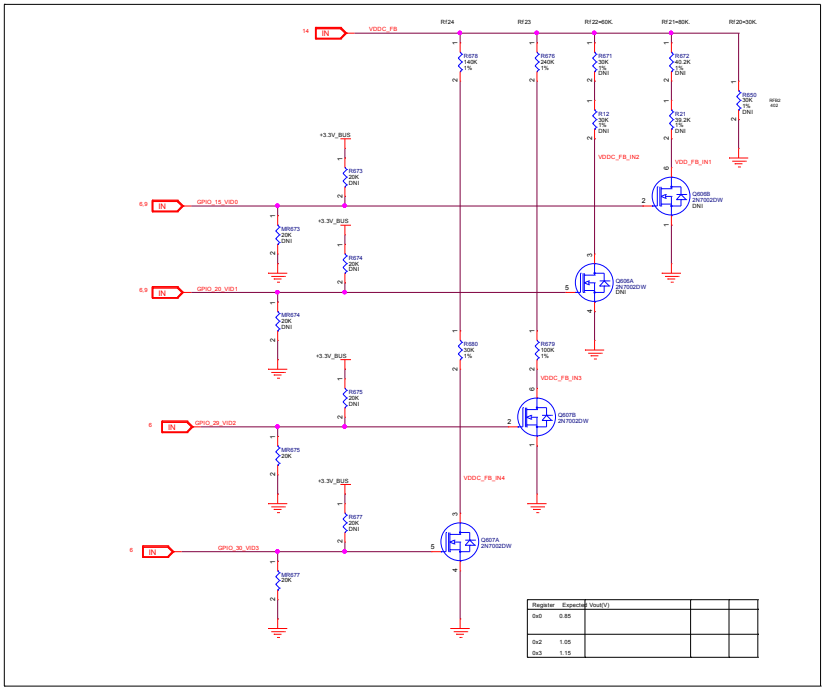


VDDC Low Side Divider



R688=3.24K,R687=5.49K; BOOT UP VDDC=1V; VR1/VCC=5.49/(3.24+5.49)=62.8%

R688=4.22K,R687=3.74K; BOOT UP VDDC=0.9V; VR1/VCC=3.74/(4.22+3.74)=46.9%



Register	Expected Vout(V)		
0x0	0.85		
0x2	1.05		
0x3	1.15		

AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203			
SHEET:	PWR SEQ		
DATE:	Thu Feb 04 02:22:48 2016	REV:	1.0
SHEET NUMBER:	9 OF 17		
DOCUMENT NUMBER:	105_D03400_00A	TITLE:	BANKS DT

MEM

SUB BOM

SUBBOM(13B-00999)
ALT(13B-00732)
256Mx32 1.35V 1125MHZ
MICRON(13B-00966)

VDDC

SUB BOM

SUBBOM(13A-01832)

TOL: +/-3%

MVDD

SUB BOM

SUBBOM(13A-01836)

TOL: +/-3%

LDO

+0.95V/+1.8V

SUB BOM

SUBBOM(13A-01834)

TOL: +/-3%

0.95V_FB — IN — 12

FBR2 402 — FBR800 5.36K 1% — 2

1.8V_FB — IN — 13

FBR4 402 — FBR861 10K 1% — 2

FBR2=5.36K->Vout=0.95V

FBR2=5.76K->Vout=0.94V

MVDD_FB_GR — OUT — 15

FBR702 1.43K 1% — 2

FBR8 402

Vout=0.8(1+FBR7/FBR8)

FBR7020 0R — 2

MVDD=1.5V FBR8 = 1.13K

MVDD=1.35V FBR8 = 1.43K

VDDC and MVDD source

+12V_BUS

FBR8 0R DNI — 2

FBR6 0R DNI — 2

L611 0.47UH

Bott Thk

Overlap

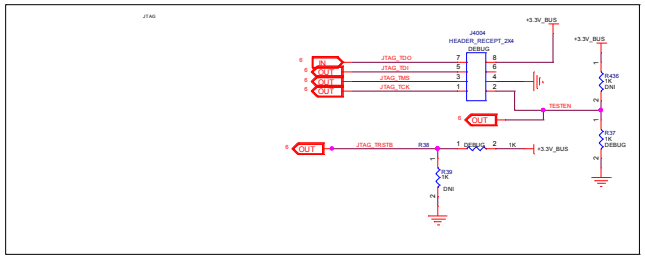
+VDDC_Source

AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203			
SHEET:	Sub BOM		
DATE:	Thu Feb 04 02:22:48 2016	REV:	1.0
SHEET NUMBER:	10 OF 17		
DOCUMENT NUMBER:	105_D03400_00A		
NOTES:	NOTE		

TITLE:

BANKS DT

Debug Circuits



AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Debug

DATE: Thu Feb 04 02:22:48 2016 REV: 1.0

SHEET NUMBER: 11 OF 17

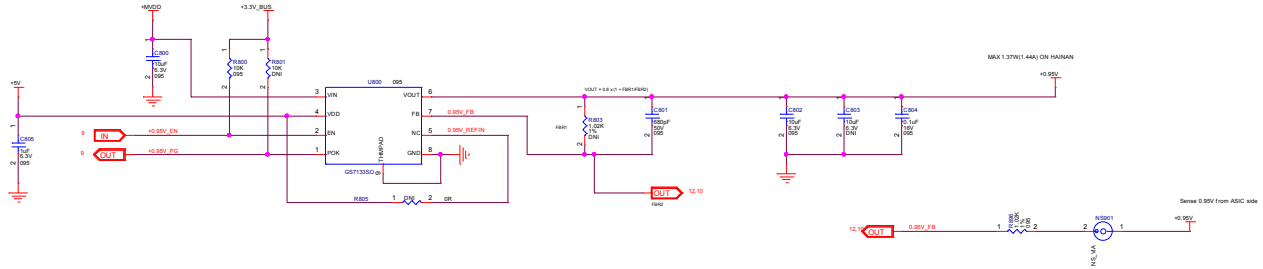
DOCUMENT NUMBER: 105_D03400_00A

TITLE: BANKS DT

Linear Regulators

LDO #1: Vin = +1.5V +/-2% Vout = +0.95V +/- 2%; Iout = 1.44A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



COMPRESSED IMAGE

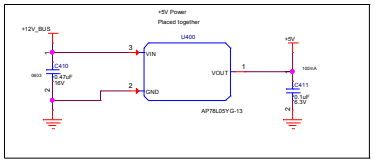
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: 0.95V	
DATE: Thu Feb 04 02:22:48 2016	REV: 1.0
SHEET NUMBER: 12 OF 17	
DOCUMENT NUMBER: 105_D03400_00A	
NOTES: NOTE	

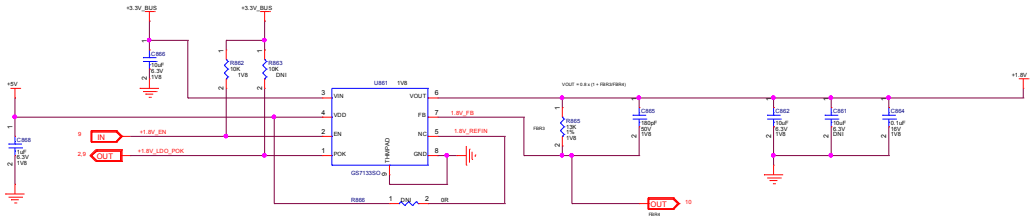
TITLE: BANKS DT

Linear Regulators

LDO #2: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX

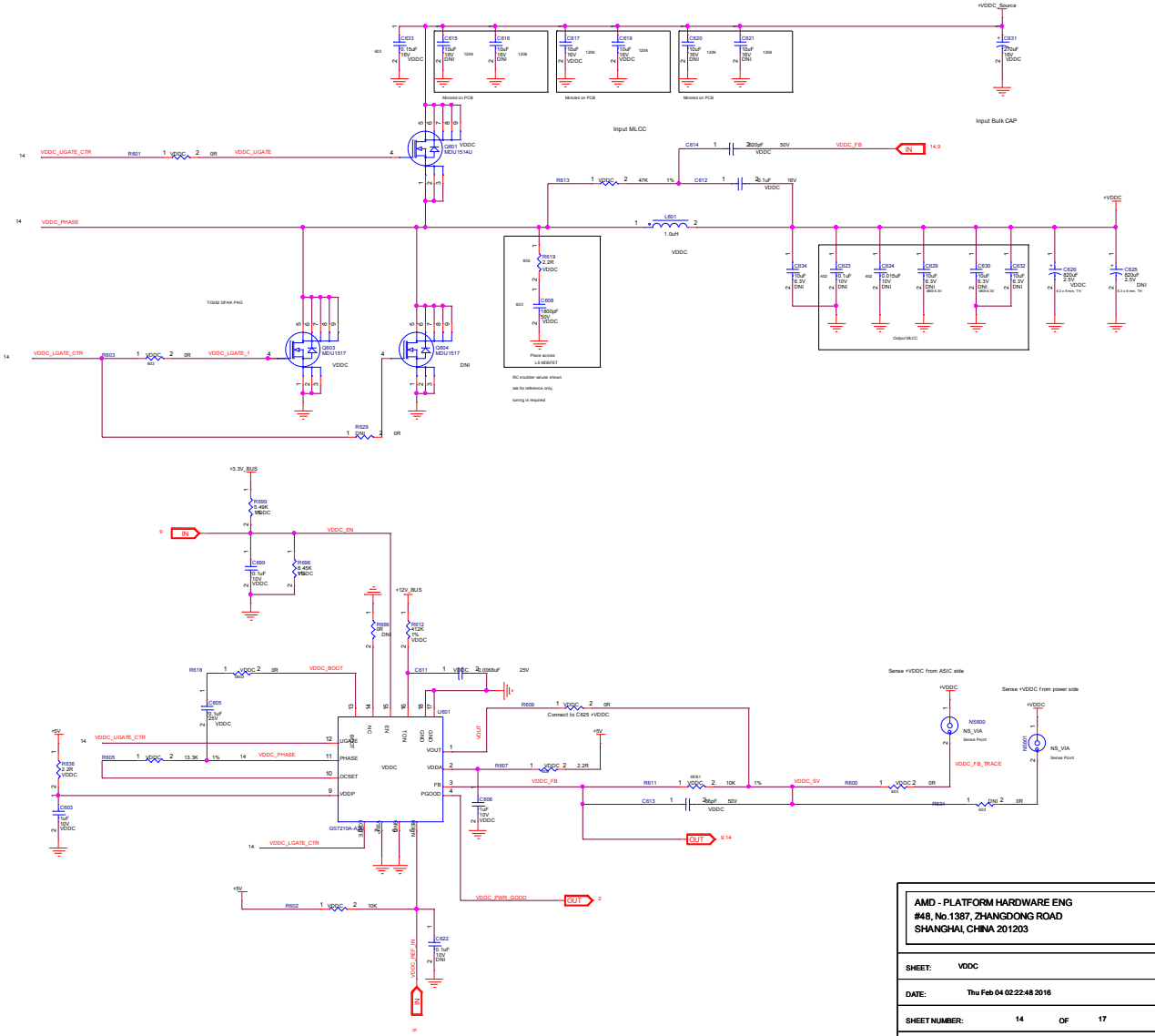
PCB: 50 to 70mm sq. copper area for cooling





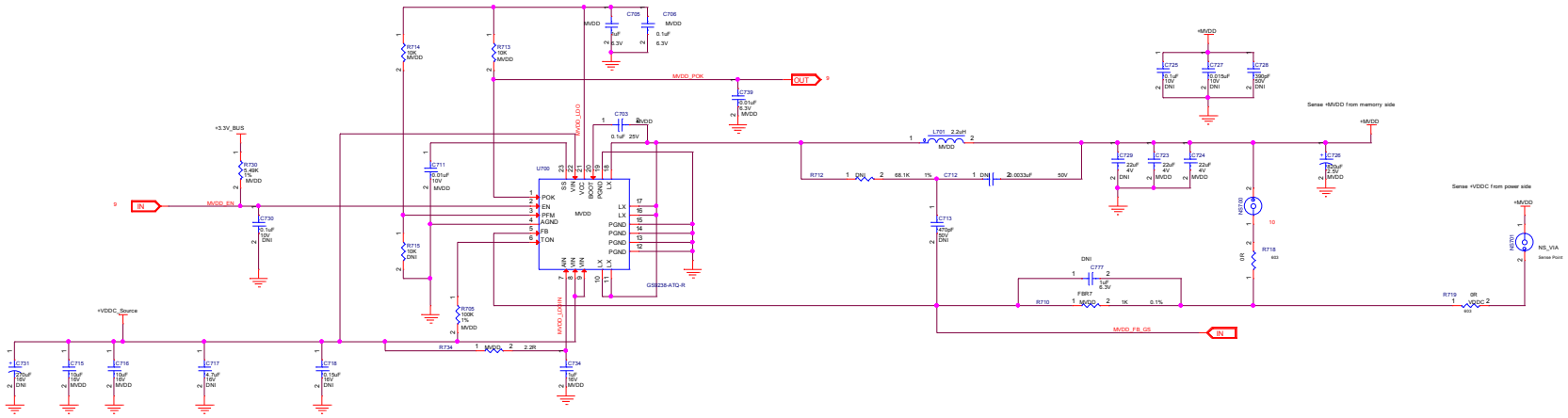
AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET:	1.8V
DATE:	Thu Feb 04 02:22:48 2016
REV:	1.0
SHEET NUMBER:	13 OF 17
DOCUMENT NUMBER:	105_D03400_00A
TITLE:	BANKS DT

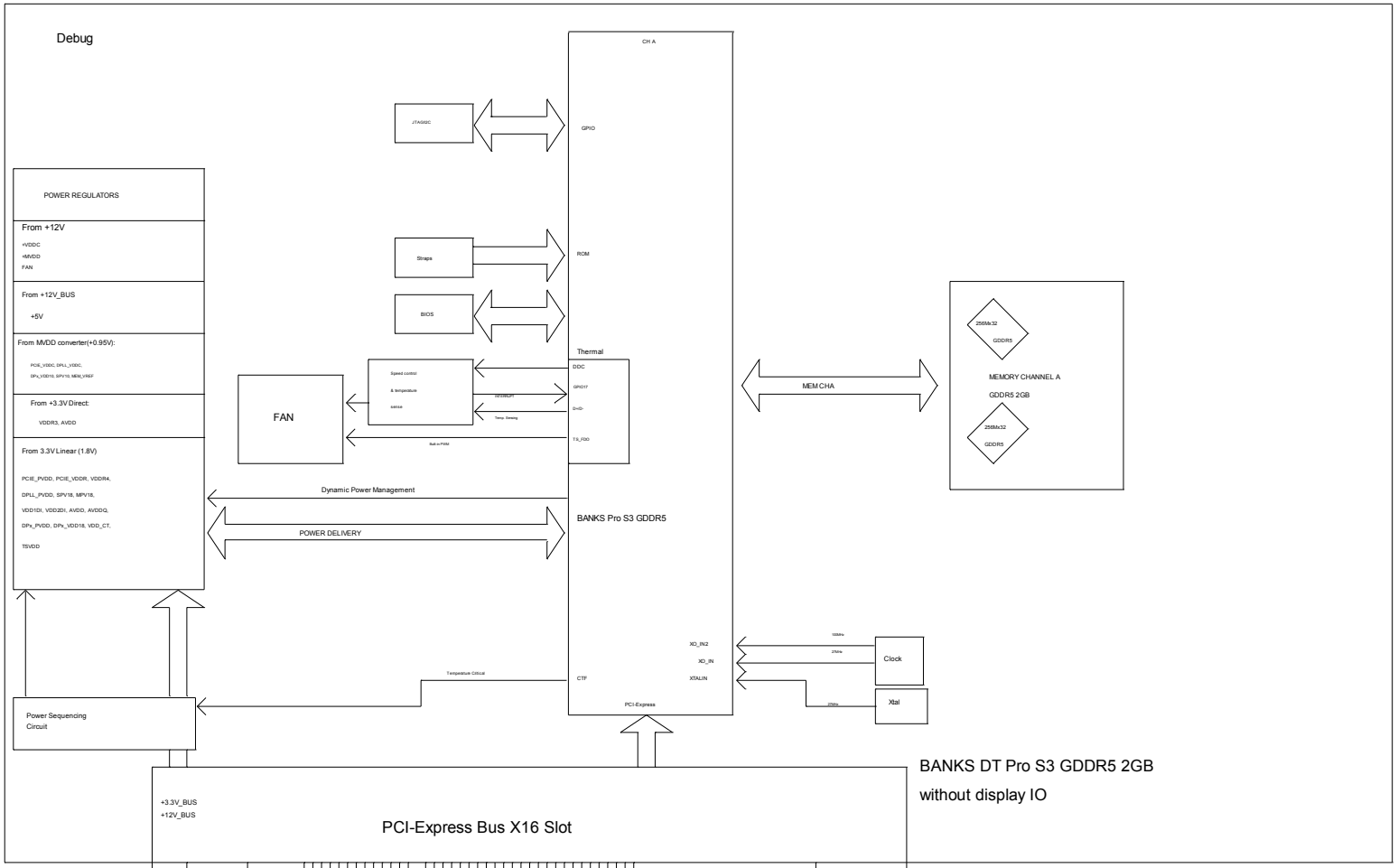


AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: VDDC	
DATE: Thu Feb 04 02:22:48 2016	REV: 1.0
SHEET NUMBER: 14 OF 17	
DOCUMENT NUMBER: 105_D03400_00A	TITLE: BANKS DT

Regulator for MVDD



AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: MVDD	
DATE: Thu Feb 04 02:22:49 2016	REV: 1.0
SHEET NUMBER: 15 OF 17	
DOCUMENT NUMBER: 105_D03400_00A	TITLE: BANKS DT



BANKS DT Pro S3 GDDR5 2GB

without display IO

Banks Pro S3 GDDR5 Power

0.95V(Measued)	TDP=16W	14W
VDDC	16.2A	13.05A
VDDCI	1.1A	1A
1.35V	TDP=16W	14W
MVDD(FOR SUN)	1.05A	1.01A
MVDD(2Pcs MEM)	2A	2A
VDDR1	0.77A	0.62A
3.3V	TDP=16W	14W
VDDR3	0.05A	0.05A
0.95V	TDP=16W	14W
+0.95V	0.79A	0.78A
BIF_VDDC	0.6A	0.59A
1.8V	TDP=16W	14W
+1.8V	0.1A	0.1A

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET:	Diagram
DATE:	Thu Feb 04 02:22:49 2016
REV:	1.0
SHEET NUMBER:	16 OF 17
DOCUMENT NUMBER:	105_D03400_00A
TITLE:	BANKS DT

AMD

TITLE: BANKS DT

DOCUMENT NUMBER: 105_D03400_00A

DATE: Thu Feb 04 02:22:49 2016

SHEET NUMBER: 17 OF 17

REV: 1.0

REVISION HISTORY

ENGINEER: BILLY DENG

NOTES: NOTE

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
1.00	00A	01/11/16	1. Initial release