P363-A01 SKU0000

P363-A01, G92, 8Mx32/16Mx32 GDDR3 (800/1000 MHz), DVI-I-DL, DVI-I-DL

Table of Contents:

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10363-base-100	P363 - BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-10363-0000-100	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
2	SKU0050	600-10363-0050-100	P363 G92-289 512MB GDDR3 16Mx32 DVI-I+DVI-I
3	SKU0058	600-10363-0058-100	P363 G92-288 512MB GDDR3 16Mx32 DVI-I+DVI-I
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	Overview

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
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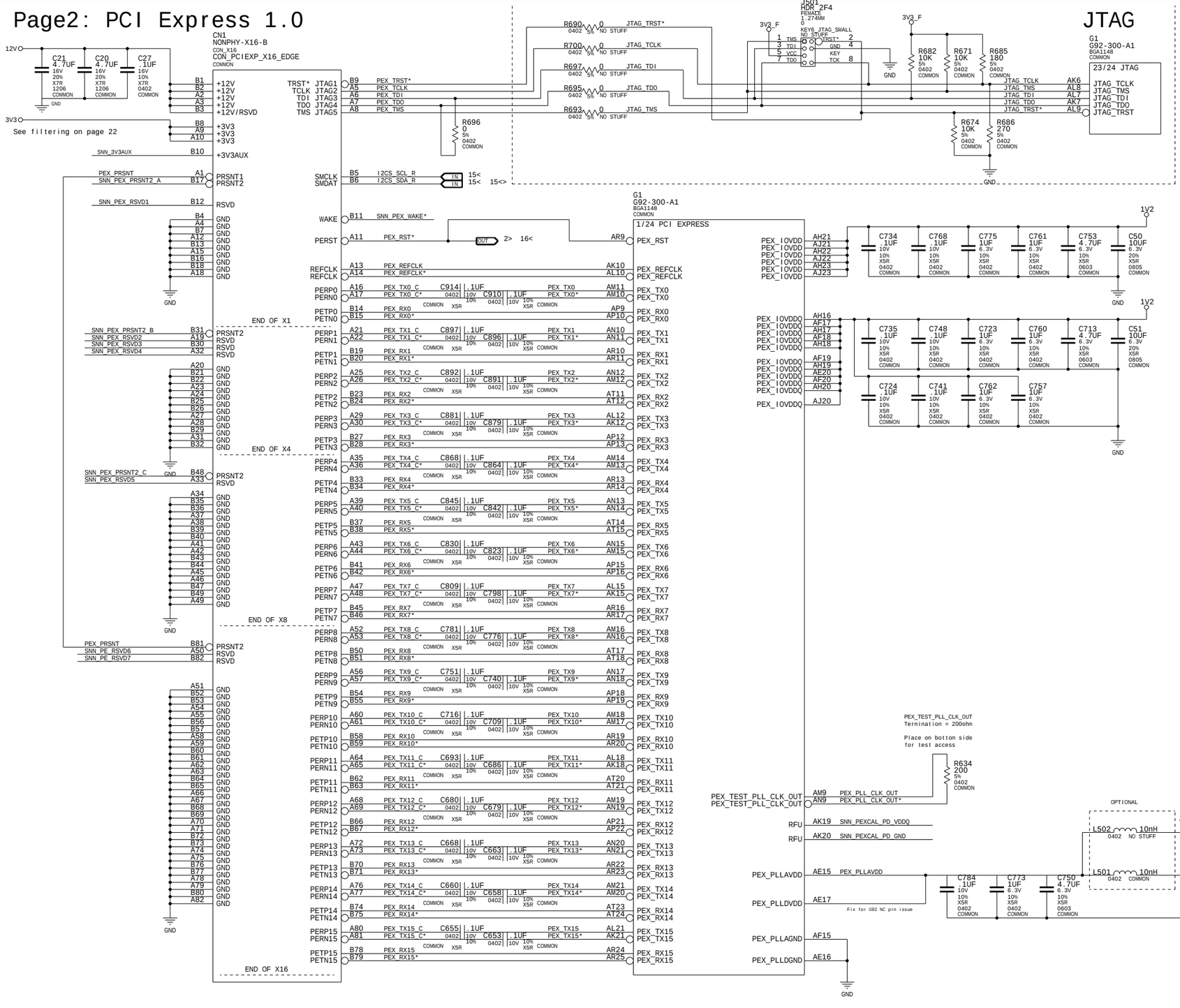
Page2: PCI Express 1.0



PEX NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
PEX_REFCLK	1	90DIFF	PEX_REFCLK
PEX_REFCLK*	1	90DIFF	PEX_REFCLK
PEX_TX0_C	1	90DIFF	PEX_TX0_C
PEX_TX0_C*	1	90DIFF	PEX_TX0_C
PEX_TX1_C	1	90DIFF	PEX_TX1_C
PEX_TX1_C*	1	90DIFF	PEX_TX1_C
PEX_TX2_C	1	90DIFF	PEX_TX2_C
PEX_TX2_C*	1	90DIFF	PEX_TX2_C
PEX_TX3_C	1	90DIFF	PEX_TX3_C
PEX_TX3_C*	1	90DIFF	PEX_TX3_C
PEX_TX4_C	1	90DIFF	PEX_TX4_C
PEX_TX4_C*	1	90DIFF	PEX_TX4_C
PEX_TX5_C	1	90DIFF	PEX_TX5_C
PEX_TX5_C*	1	90DIFF	PEX_TX5_C
PEX_TX6_C	1	90DIFF	PEX_TX6_C
PEX_TX6_C*	1	90DIFF	PEX_TX6_C
PEX_TX7_C	1	90DIFF	PEX_TX7_C
PEX_TX7_C*	1	90DIFF	PEX_TX7_C
PEX_TX8_C	1	90DIFF	PEX_TX8_C
PEX_TX8_C*	1	90DIFF	PEX_TX8_C
PEX_TX9_C	1	90DIFF	PEX_TX9_C
PEX_TX9_C*	1	90DIFF	PEX_TX9_C
PEX_TX10_C	1	90DIFF	PEX_TX10_C
PEX_TX10_C*	1	90DIFF	PEX_TX10_C
PEX_TX11_C	1	90DIFF	PEX_TX11_C
PEX_TX11_C*	1	90DIFF	PEX_TX11_C
PEX_TX12_C	1	90DIFF	PEX_TX12_C
PEX_TX12_C*	1	90DIFF	PEX_TX12_C
PEX_TX13_C	1	90DIFF	PEX_TX13_C
PEX_TX13_C*	1	90DIFF	PEX_TX13_C
PEX_TX14_C	1	90DIFF	PEX_TX14_C
PEX_TX14_C*	1	90DIFF	PEX_TX14_C
PEX_TX15_C	1	90DIFF	PEX_TX15_C
PEX_TX15_C*	1	90DIFF	PEX_TX15_C
PEX_RX0	1	90DIFF	PEX_RX0
PEX_RX0*	1	90DIFF	PEX_RX0
PEX_RX1	1	90DIFF	PEX_RX1
PEX_RX1*	1	90DIFF	PEX_RX1
PEX_RX2	1	90DIFF	PEX_RX2
PEX_RX2*	1	90DIFF	PEX_RX2
PEX_RX3	1	90DIFF	PEX_RX3
PEX_RX3*	1	90DIFF	PEX_RX3
PEX_RX4	1	90DIFF	PEX_RX4
PEX_RX4*	1	90DIFF	PEX_RX4
PEX_RX5	1	90DIFF	PEX_RX5
PEX_RX5*	1	90DIFF	PEX_RX5
PEX_RX6	1	90DIFF	PEX_RX6
PEX_RX6*	1	90DIFF	PEX_RX6
PEX_RX7	1	90DIFF	PEX_RX7
PEX_RX7*	1	90DIFF	PEX_RX7
PEX_RX8	1	90DIFF	PEX_RX8
PEX_RX8*	1	90DIFF	PEX_RX8
PEX_RX9	1	90DIFF	PEX_RX9
PEX_RX9*	1	90DIFF	PEX_RX9
PEX_RX10	1	90DIFF	PEX_RX10
PEX_RX10*	1	90DIFF	PEX_RX10
PEX_RX11	1	90DIFF	PEX_RX11
PEX_RX11*	1	90DIFF	PEX_RX11
PEX_RX12	1	90DIFF	PEX_RX12
PEX_RX12*	1	90DIFF	PEX_RX12
PEX_RX13	1	90DIFF	PEX_RX13
PEX_RX13*	1	90DIFF	PEX_RX13
PEX_RX14	1	90DIFF	PEX_RX14
PEX_RX14*	1	90DIFF	PEX_RX14
PEX_RX15	1	90DIFF	PEX_RX15
PEX_RX15*	1	90DIFF	PEX_RX15
PEX_TX0	1	90DIFF	PEX_TX0
PEX_TX0*	1	90DIFF	PEX_TX0
PEX_TX1	1	90DIFF	PEX_TX1
PEX_TX1*	1	90DIFF	PEX_TX1
PEX_TX2	1	90DIFF	PEX_TX2
PEX_TX2*	1	90DIFF	PEX_TX2
PEX_TX3	1	90DIFF	PEX_TX3
PEX_TX3*	1	90DIFF	PEX_TX3
PEX_TX4	1	90DIFF	PEX_TX4
PEX_TX4*	1	90DIFF	PEX_TX4
PEX_TX5	1	90DIFF	PEX_TX5
PEX_TX5*	1	90DIFF	PEX_TX5
PEX_TX6	1	90DIFF	PEX_TX6
PEX_TX6*	1	90DIFF	PEX_TX6
PEX_TX7	1	90DIFF	PEX_TX7
PEX_TX7*	1	90DIFF	PEX_TX7
PEX_TX8	1	90DIFF	PEX_TX8
PEX_TX8*	1	90DIFF	PEX_TX8
PEX_TX9	1	90DIFF	PEX_TX9
PEX_TX9*	1	90DIFF	PEX_TX9
PEX_TX10	1	90DIFF	PEX_TX10
PEX_TX10*	1	90DIFF	PEX_TX10
PEX_TX11	1	90DIFF	PEX_TX11
PEX_TX11*	1	90DIFF	PEX_TX11
PEX_TX12	1	90DIFF	PEX_TX12
PEX_TX12*	1	90DIFF	PEX_TX12
PEX_TX13	1	90DIFF	PEX_TX13
PEX_TX13*	1	90DIFF	PEX_TX13
PEX_TX14	1	90DIFF	PEX_TX14
PEX_TX14*	1	90DIFF	PEX_TX14
PEX_TX15	1	90DIFF	PEX_TX15
PEX_TX15*	1	90DIFF	PEX_TX15
PEX_PLL_CLK_OUT	1	90DIFF	PEX_PLL_CLK_OUT
PEX_PLL_CLK_OUT*	1	90DIFF	PEX_PLL_CLK_OUT
PEX_RST*	3	50OHM	
PEX_TRST*	3	50OHM	
PEX_TCLK	3	50OHM	
PEX_TDI	3	50OHM	
PEX_TDO	3	50OHM	
PEX_TMS	3	50OHM	
JTAG_TCLK	3	50OHM	
JTAG_TMS	3	50OHM	
JTAG_TDI	3	50OHM	
JTAG_TDO	3	50OHM	
JTAG_TRST*	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
PEX_PLLAVDD	1.2V	0.25A	12MIL
PEX_PLLDVDD	1.2V	0.10A	12MIL

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	PCI Express 1.0

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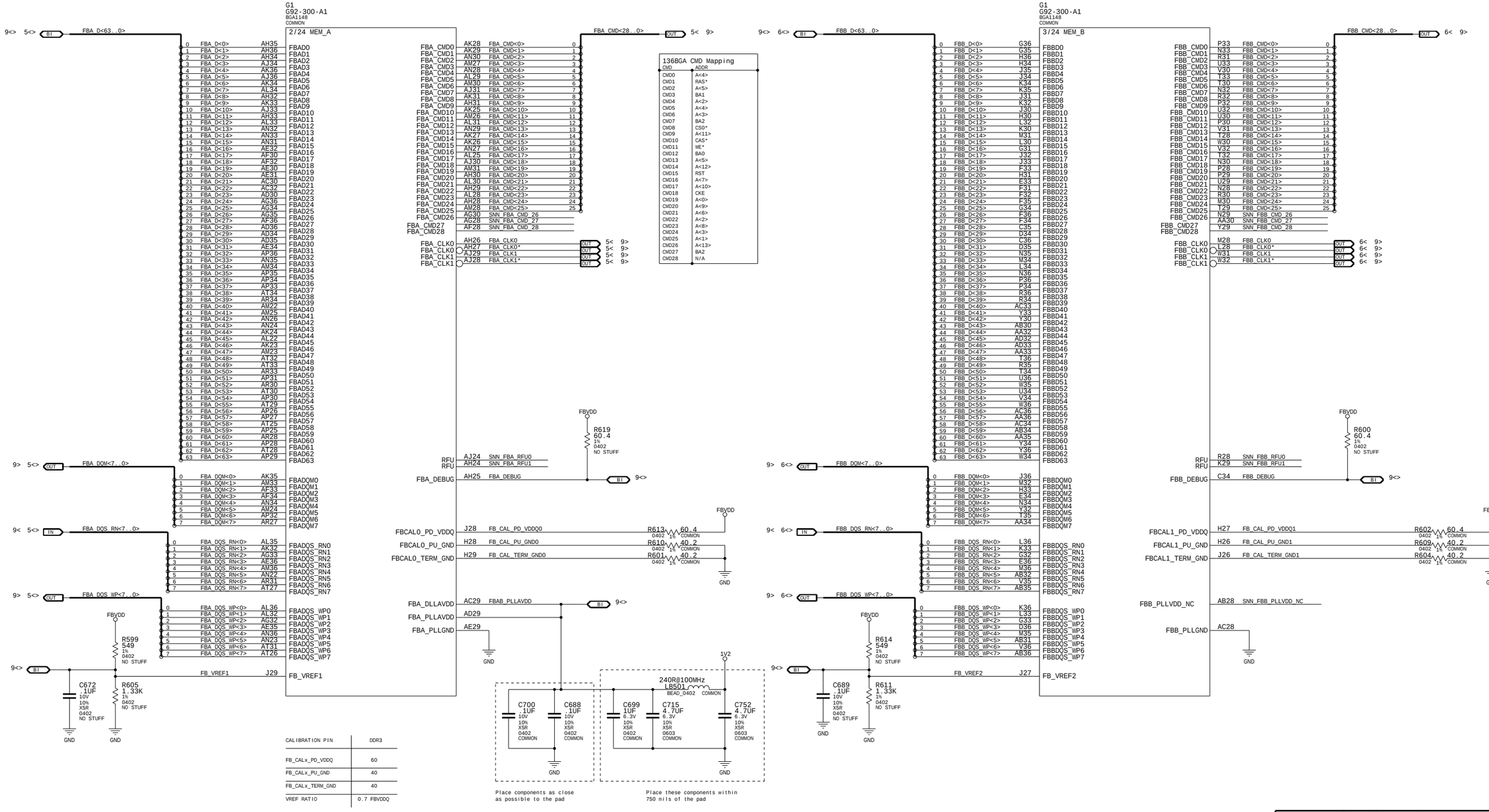
Page3: MEMORY: GPU Partition A/B



ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	MEMORY: GPU Partition A/B

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Page4: MEMORY: GPU Partition C/D

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	MEMORY: GPU Partition C/D

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Page5: FBA Partition

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

M6 / M7
DDR3BGA136
PACK_TYPE=BGA136_V2
VERSION=BGA136
CHANGED

*CS1 is required 32Mx32 Memories

Clock Term MUST BE PLACED as close as possible to the BGA memory on the line AFTER the memory pin!
Minimize STUB length!

GDDR3: VREF = 0.70 * FBVDDQ
1.41V = 2.0V * 1.33K/(549 + 1.33K)

Decoupling for FBA Lo

Decoupling for FBA Hi

Place 1uF caps at center of memory

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	FBA Partition

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Page6: FBB Partition

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

M5 / M8 DDR3BGA136, PACK_TYPE=BGA136_V2, VERSION=BGA136 CHANGED

Clock Term MUST BE PLACED as close as possible to the BGA memory on the line AFTER the memory pin!
Minimize STUB length!

*CS1 is required 32Mx32 Memories

GDDR3: VREF = 0.70 * FBVDDQ
1.41V = 2.0V * 1.33K/(549 + 1.33K)

Decoupling for FBB Lo

Place 1uF caps at center of memory

Decoupling for FBB Hi

Place 1uF caps at center of memory

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	FBB Partition

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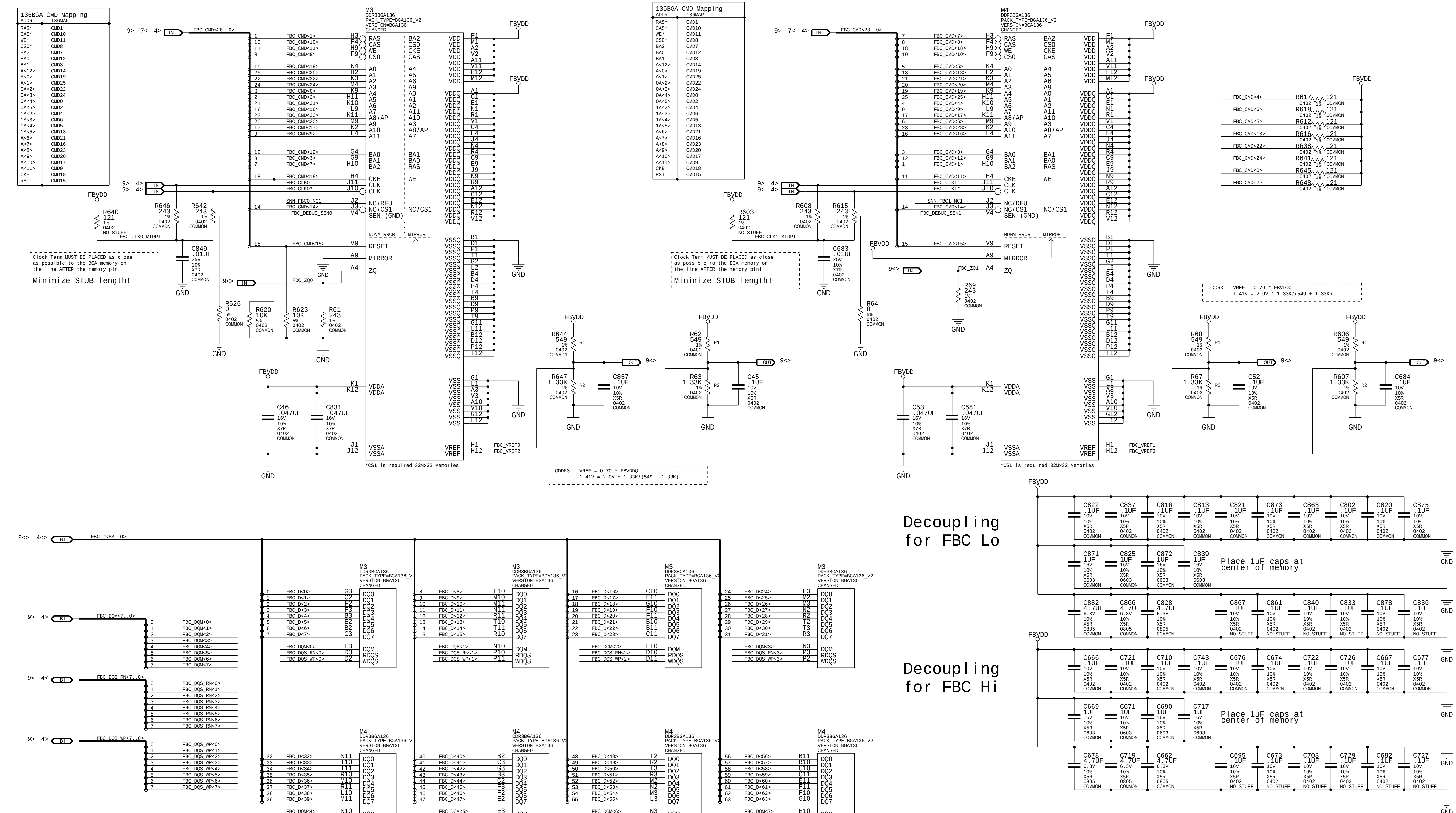
Page7: FBC Partition



ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	FBC Partition

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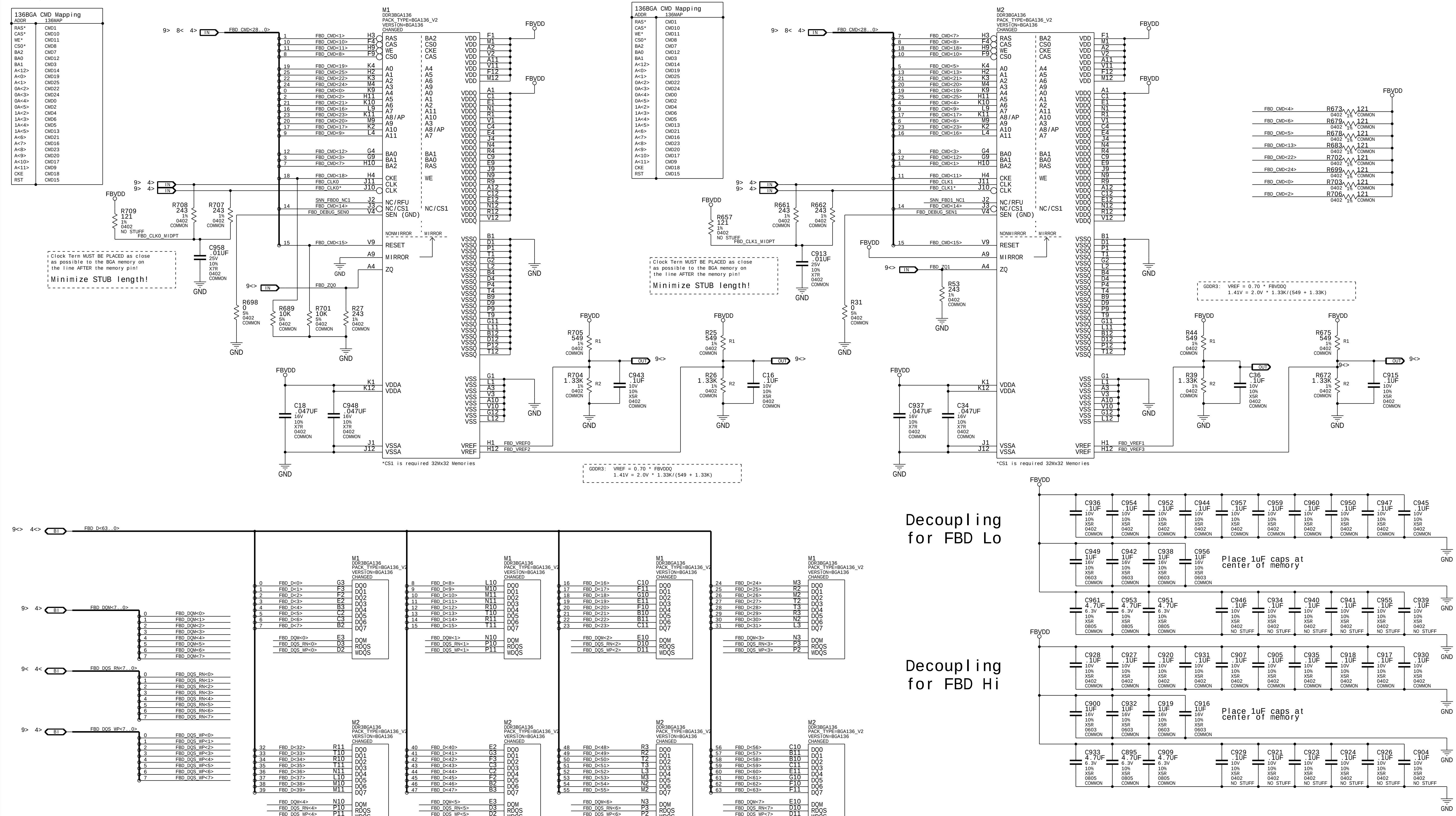
Page8: FBD Partition



136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

136BGA CMD Mapping

ADDR	136MAP
RAS*	CMD1
CAS*	CMD10
WE*	CMD11
CS0*	CMD8
BA2	CMD7
BA0	CMD12
BA1	CMD3
A<12>	CMD14
A<0>	CMD19
A<1>	CMD25
0A<2>	CMD22
0A<3>	CMD24
0A<4>	CMD0
0A<5>	CMD2
1A<2>	CMD4
1A<3>	CMD6
1A<4>	CMD5
1A<5>	CMD13
A<6>	CMD21
A<7>	CMD16
A<8>	CMD23
A<9>	CMD20
A<10>	CMD17
A<11>	CMD9
CKE	CMD18
RST	CMD15

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	FBD Partition

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Page9: FrameBuffer Net Rules

NET RULES for FrameBuffer A/B

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
5< 3>	OUT	FBA_CLK0	1	80DIFF	FBA_CLK0
5< 3>	OUT	FBA_CLK0*	1	80DIFF	FBA_CLK0
5< 3>	OUT	FBA_CLK1	1	80DIFF	FBA_CLK1
5< 3>	OUT	FBA_CLK1*	1	80DIFF	FBA_CLK1
5< 3>	OUT	FBA_CMD<28..0>	1	40OHM	
5<> 3>	OUT	FBA_DQS_WP<7..0>	1	40OHM	
5<> 3<	IN	FBA_DQS_RN<7..0>	1	40OHM	
5<> 3>	OUT	FBA_DQ<7..0>	1	40OHM	
5<> 3<>	BI	FBA_D<63..0>	1	40OHM	

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
6< 3>	OUT	FBB_CLK0	1	80DIFF	FBB_CLK0
6< 3>	OUT	FBB_CLK0*	1	80DIFF	FBB_CLK0
6< 3>	OUT	FBB_CLK1	1	80DIFF	FBB_CLK1
6< 3>	OUT	FBB_CLK1*	1	80DIFF	FBB_CLK1
6< 3>	OUT	FBB_CMD<28..0>	1	40OHM	
6<> 3>	OUT	FBB_DQS_WP<7..0>	1	40OHM	
6<> 3<	IN	FBB_DQS_RN<7..0>	1	40OHM	
6<> 3>	OUT	FBB_DQ<7..0>	1	40OHM	
6<> 3<>	BI	FBB_D<63..0>	1	40OHM	
3<>	BI	FBA_DEBUG	1	45OHM	
3<>	BI	FBB_DEBUG	1	40OHM	

		NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
3<>	BI	FBAB_PLLAVDD	1.2V	0.02A	12MIL
5>	BI	FBA_VREF0	1.40V	0.02A	12MIL
5>	BI	FBA_VREF1	1.40V	0.02A	12MIL
5>	BI	FBA_VREF2	1.40V	0.02A	12MIL
5>	BI	FBA_VREF3	1.40V	0.02A	12MIL
5<	BI	FBA_ZQ0	2.0V	0.02A	12MIL
5<	BI	FBA_ZQ1	2.0V	0.02A	12MIL
6>	BI	FBB_VREF0	1.40V	0.02A	12MIL
6>	BI	FBB_VREF1	1.40V	0.02A	12MIL
6>	BI	FBB_VREF2	1.40V	0.02A	12MIL
6>	BI	FBB_VREF3	1.40V	0.02A	12MIL
6<	BI	FBB_ZQ0	2.0V	0.02A	12MIL
6<	BI	FBB_ZQ1	2.0V	0.02A	12MIL
3<>	BI	FB_VREF1	1.40V	0.02A	12MIL
3<>	BI	FB_VREF2	1.40V	0.02A	12MIL

NET RULES for FrameBuffer C/D

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
7< 4>	OUT	FBC_CLK0	1	80DIFF	FBC_CLK0
7< 4>	OUT	FBC_CLK0*	1	80DIFF	FBC_CLK0
7< 4>	OUT	FBC_CLK1	1	80DIFF	FBC_CLK1
7< 4>	OUT	FBC_CLK1*	1	80DIFF	FBC_CLK1
7< 4>	OUT	FBC_CMD<28..0>	1	40OHM	
7<> 4>	OUT	FBC_DQS_WP<7..0>	1	40OHM	
7<> 4<	IN	FBC_DQS_RN<7..0>	1	40OHM	
7<> 4>	OUT	FBC_DQ<7..0>	1	40OHM	
7<> 4<>	BI	FBC_D<63..0>	1	40OHM	

		NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
8< 4>	OUT	FBD_CLK0	1	80DIFF	FBD_CLK0
8< 4>	OUT	FBD_CLK0*	1	80DIFF	FBD_CLK0
8< 4>	OUT	FBD_CLK1	1	80DIFF	FBD_CLK1
8< 4>	OUT	FBD_CLK1*	1	80DIFF	FBD_CLK1
8< 4>	OUT	FBD_CMD<28..0>	1	40OHM	
8<> 4>	OUT	FBD_DQS_WP<7..0>	1	40OHM	
8<> 4<	IN	FBD_DQS_RN<7..0>	1	40OHM	
8<> 4>	OUT	FBD_DQ<7..0>	1	40OHM	
8<> 4<>	BI	FBD_D<63..0>	1	40OHM	
4<>	BI	FBC_DEBUG	1	40OHM	
4<>	BI	FBD_DEBUG	1	40OHM	

		NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
4<>	BI	FBCD_PLLAVDD	1.2V	0.02A	12MIL
7>	BI	FBC_VREF0	1.40V	0.02A	12MIL
7>	BI	FBC_VREF1	1.40V	0.02A	12MIL
7>	BI	FBC_VREF2	1.40V	0.02A	12MIL
7>	BI	FBC_VREF3	1.40V	0.02A	12MIL
7<	BI	FBC_ZQ0	2.0V	0.02A	12MIL
7<	BI	FBC_ZQ1	2.0V	0.02A	12MIL
8>	BI	FBD_VREF0	1.40V	0.02A	12MIL
8>	BI	FBD_VREF1	1.40V	0.02A	12MIL
8>	BI	FBD_VREF2	1.40V	0.02A	12MIL
8>	BI	FBD_VREF3	1.40V	0.02A	12MIL
8<	BI	FBD_ZQ0	2.0V	0.02A	12MIL
8<	BI	FBD_ZQ1	2.0V	0.02A	12MIL

Note: FB traces on top and bottom layers are routed with 45ohm impedance for increasing spacing.
Internal FB traces are routed with 40ohm impedance.

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	FrameBuffer Net Rules

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Page10: DACA Interface

DACA NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	DACA_RED	1	75OHM	
IN	DACA_GREEN	1	75OHM	
IN	DACA_BLUE	1	75OHM	
12< 10> IN	DACA_RED_DVI	1	75OHM	
12< 10> IN	DACA_GREEN_DVI	1	75OHM	
12< 10> IN	DACA_BLUE_DVI	1	75OHM	
IN	DACA_HS	2	50OHM	
IN	DACA_VS	2	50OHM	
IN	DACA_HS_BUF	2	50OHM	
IN	DACA_VS_BUF	2	50OHM	
IN	DACA_HS_BUF_R	2	50OHM	
IN	DACA_VS_BUF_R	2	50OHM	
12< 10> IN	DACA_HS_DVI	2	50OHM	
12< 10> IN	DACA_VS_DVI	2	50OHM	
IN	I2CA_SCL	3	50OHM	
IN	I2CA_SDA	3	50OHM	
IN	I2CA_SCL_R	3	50OHM	
IN	I2CA_SDA_R	3	50OHM	
12< 10> IN	I2CA_SCL_DVI	3	50OHM	
12< 10> IN	I2CA_SDA_DVI	3	50OHM	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	DACA_VREF			12MIL
IN	DACA_RSET			12MIL
BI	DACA_VDD	3.3V	0.100A	16MIL

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	DACA Interface

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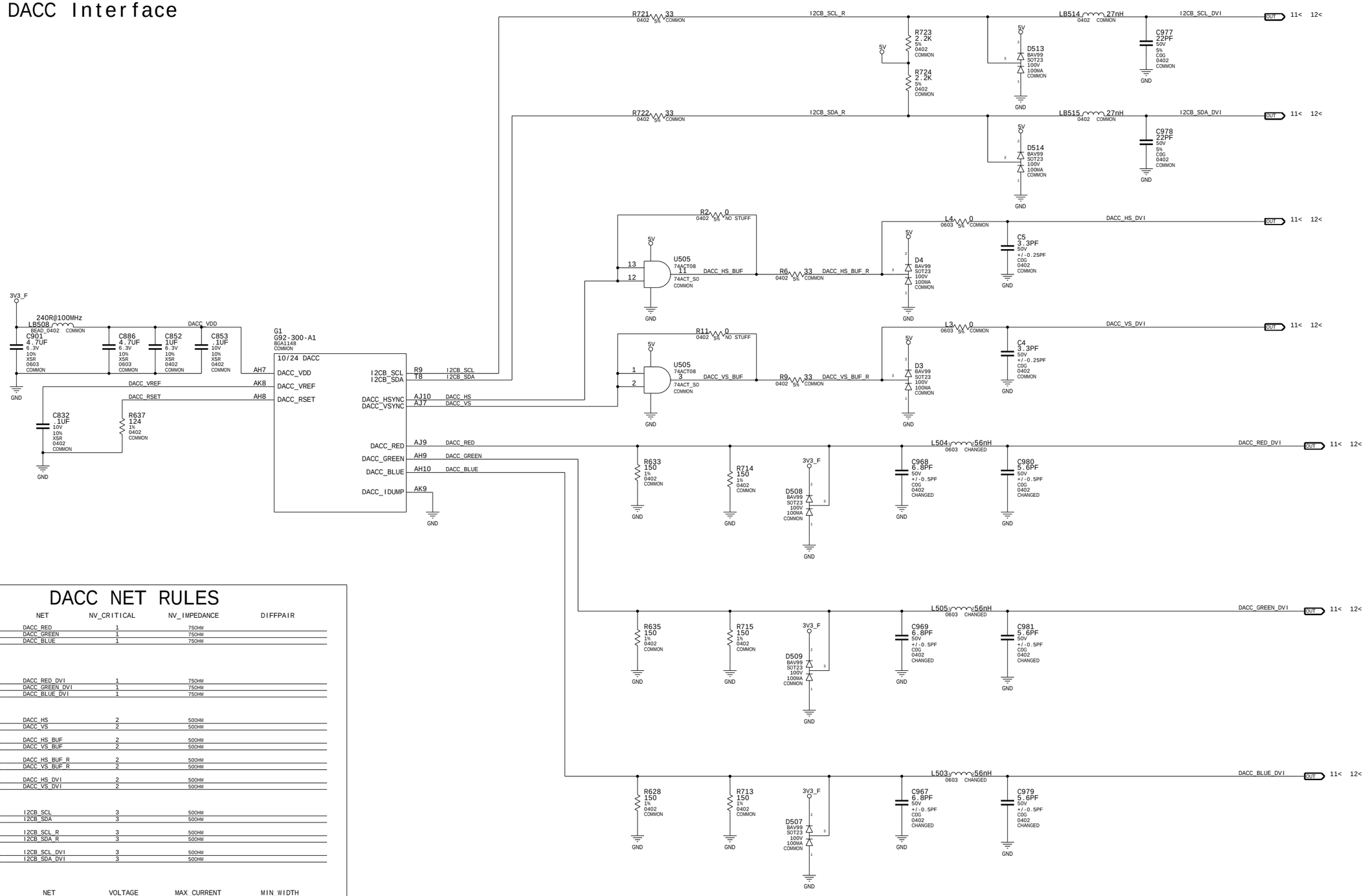
Page11: DACC Interface



DACC NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	DACC_RED	1	75OHM	
IN	DACC_GREEN	1	75OHM	
IN	DACC_BLUE	1	75OHM	
12< 11> IN	DACC_RED_DVI	1	75OHM	
12< 11> IN	DACC_GREEN_DVI	1	75OHM	
12< 11> IN	DACC_BLUE_DVI	1	75OHM	
IN	DACC_HS	2	50OHM	
IN	DACC_VS	2	50OHM	
IN	DACC_HS_BUF	2	50OHM	
IN	DACC_VS_BUF	2	50OHM	
IN	DACC_HS_BUF_R	2	50OHM	
IN	DACC_VS_BUF_R	2	50OHM	
12< 11> IN	DACC_HS_DVI	2	50OHM	
12< 11> IN	DACC_VS_DVI	2	50OHM	
IN	I2CB_SCL	3	50OHM	
IN	I2CB_SDA	3	50OHM	
IN	I2CB_SCL_R	3	50OHM	
IN	I2CB_SDA_R	3	50OHM	
12< 11> IN	I2CB_SCL_DVI	3	50OHM	
12< 11> IN	I2CB_SDA_DVI	3	50OHM	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	DACC_VREF			12MIL
IN	DACC_RSET			12MIL
BI	DACC_VDD	3.3V	0.100A	16MIL

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	DACC Interface

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Page12: IFP A/B and C/D Interface

IFPABCD NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RSET			12MIL
IFPCD_RSET			12MIL
GPIO0_DVIAB_HPD_F	3	50OHM	
GPIO0_DVIAB_HPD_R	3	50OHM	
GPIO1_DVICD_HPD_F	3	50OHM	
GPIO1_DVICD_HPD_R	3	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_PLLVDD	1.8V	0.03A	16MIL
IFPAB_IOVDD	3.3V	0.09A	16MIL
IFPCD_PLLVDD	1.8V	0.03A	16MIL
IFPCD_IOVDD	3.3V	0.09A	16MIL

NET RULES

NET	DIFFPAIR	NV_CRITICAL	NV_IMPEDANCE
IFPA_TXC*	IFPAB_TXC	1	90DIFF
IFPA_TXC	IFPAB_TXC	1	90DIFF
IFPA_TXD0*	IFPAB_TXD0	1	90DIFF
IFPA_TXD0	IFPAB_TXD0	1	90DIFF
IFPA_TXD1*	IFPAB_TXD1	1	90DIFF
IFPA_TXD1	IFPAB_TXD1	1	90DIFF
IFPA_TXD2*	IFPAB_TXD2	1	90DIFF
IFPA_TXD2	IFPAB_TXD2	1	90DIFF
SNN_IFPAB_TXD3*			
SNN_IFPAB_TXD3			
SNN_IFPB_TXC*			
SNN_IFPB_TXC			
IFPB_TXD4*	IFPAB_TXD4	1	90DIFF
IFPB_TXD4	IFPAB_TXD4	1	90DIFF
IFPB_TXD5*	IFPAB_TXD5	1	90DIFF
IFPB_TXD5	IFPAB_TXD5	1	90DIFF
IFPB_TXD6*	IFPAB_TXD6	1	90DIFF
IFPB_TXD6	IFPAB_TXD6	1	90DIFF
SNN_IFPAB_TXD7*			
SNN_IFPAB_TXD7			

NET RULES

NET	DIFFPAIR	NV_CRITICAL	NV_IMPEDANCE
IFPC_TXC*	IFPC_TXC	1	90DIFF
IFPC_TXC	IFPC_TXC	1	90DIFF
IFPC_TXD0*	IFPCD_TXD0	1	90DIFF
IFPC_TXD0	IFPCD_TXD0	1	90DIFF
IFPC_TXD1*	IFPCD_TXD1	1	90DIFF
IFPC_TXD1	IFPCD_TXD1	1	90DIFF
IFPC_TXD2*	IFPCD_TXD2	1	90DIFF
IFPC_TXD2	IFPCD_TXD2	1	90DIFF
SNN_IFPD_TXC*			
SNN_IFPD_TXC			
IFPD_TXD4*	IFPCD_TXD4	1	90DIFF
IFPD_TXD4	IFPCD_TXD4	1	90DIFF
IFPD_TXD5*	IFPCD_TXD5	1	90DIFF
IFPD_TXD5	IFPCD_TXD5	1	90DIFF
IFPD_TXD6*	IFPCD_TXD6	1	90DIFF
IFPD_TXD6	IFPCD_TXD6	1	90DIFF

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	IFP A/B and C/D Interface

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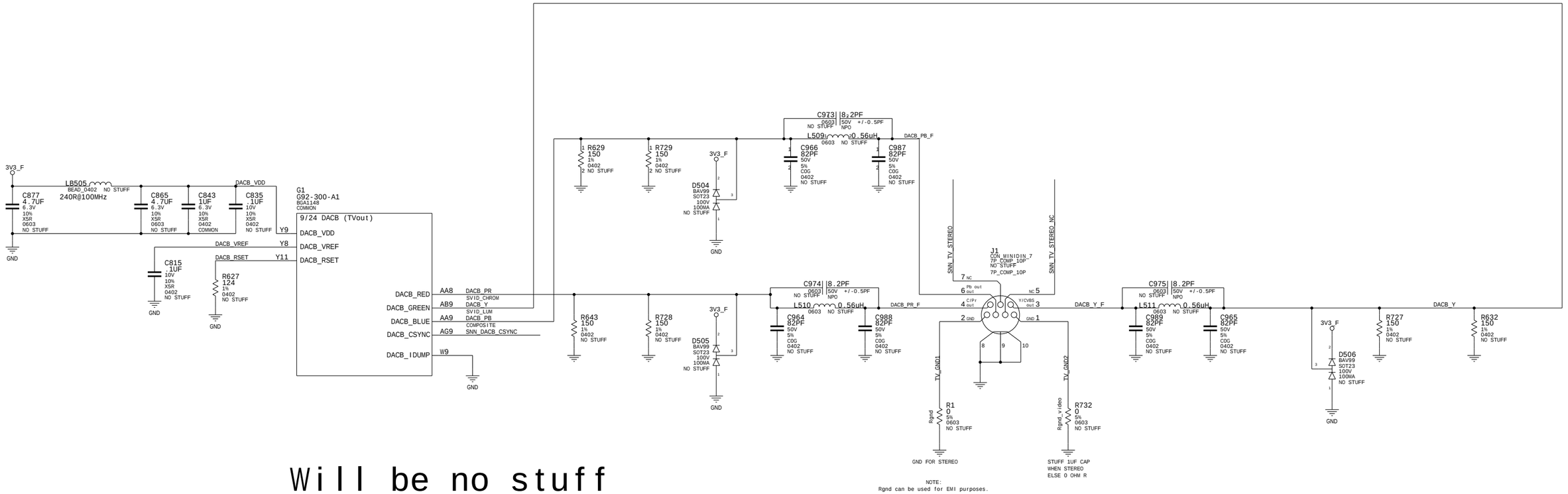
Page13: DACB Interface

DACB,STEREO, FL NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	DACB_PR	1	75OHM	
IN	DACB_Y	1	75OHM	
IN	DACB_PB	1	75OHM	
IN	DACB_PR_F	1	75OHM	
IN	DACB_Y_F	1	75OHM	
IN	DACB_PB_F	1	75OHM	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	TV_GND1	0.0V		12MIL
IN	TV_GND2	0V		12MIL
IN	DACB_VDD	3.3V	0.2A	12MIL
IN	DACB_VREF			12MIL
IN	DACB_RSET			12MIL



NOTE:
Rgnd can be used for EMI purposes.

Will be no stuff

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	DACB Interface

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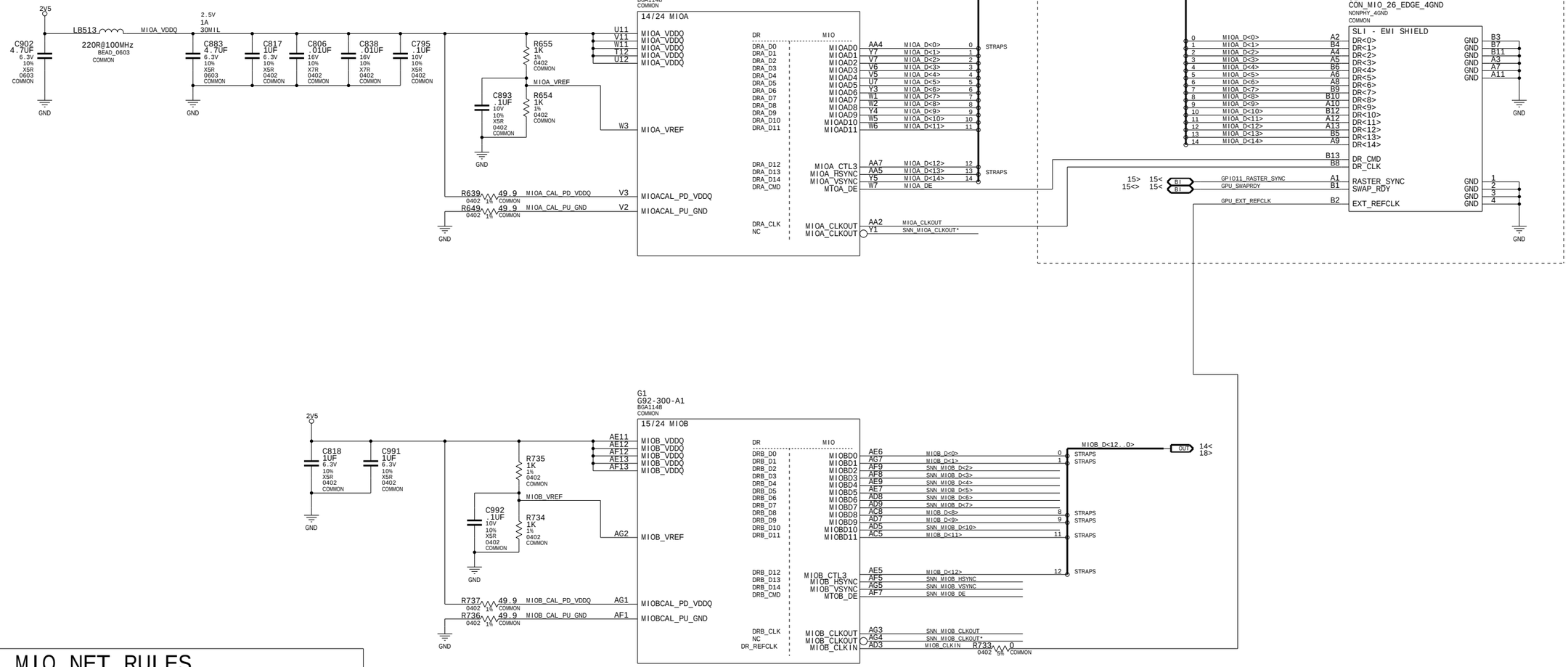
Page14: Multi-use IO(MIO) Interface

MIO Feature Connector



MIO NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
18> 14< IN	MIOA_D<14..0>	1	50OHM	
IN	MIOA_CLKOUT	1	50OHM	
IN	MIOA_DE	1	50OHM	
18> 14> IN	MIOB_D<12..0>	1	50OHM	
IN	MIOB_CLKIN	1	50OHM	
IN	GPU_EXT_REFCLK	1	50OHM	

	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN	MIOA_VREF	1.25V		12MIL
IN	MIOACAL_PD_VDDQ			12MIL
IN	MIOACAL_PU_GND			12MIL
IN	MIOB_VREF	1.25V		12MIL
IN	MIOBCAL_PD_VDDQ			12MIL
IN	MIOBCAL_PU_GND			12MIL

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	Multi-use IO(MIO) Interface

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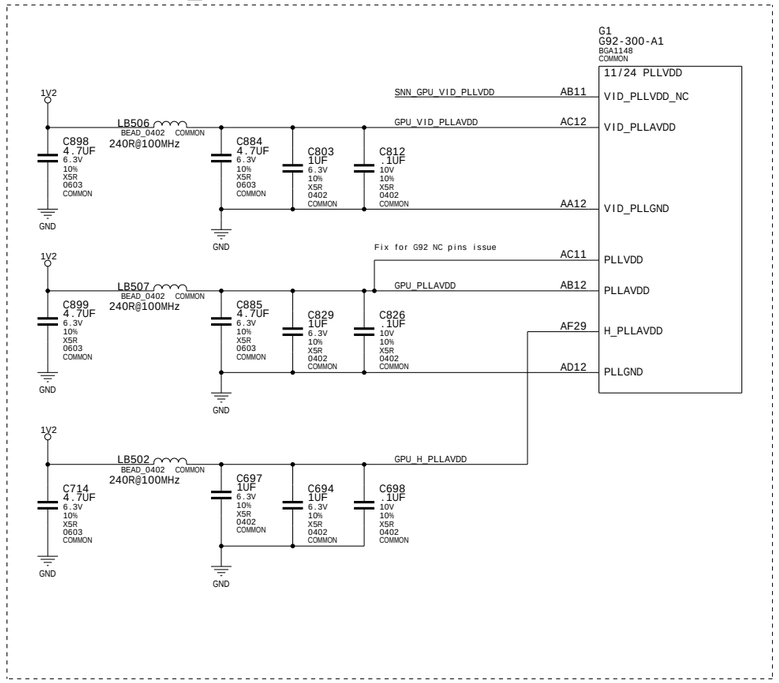
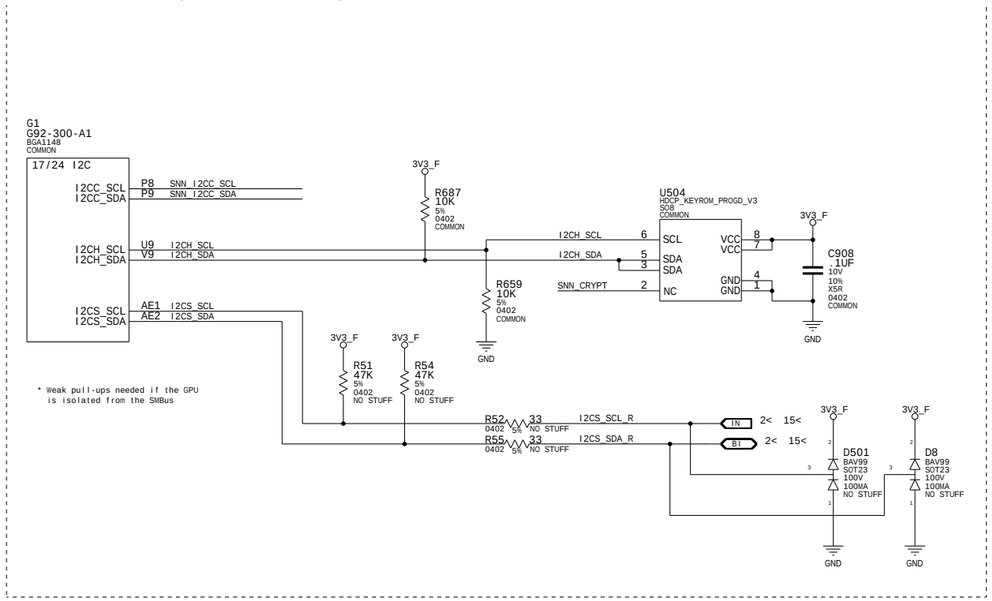
Page15: MISC: GPIO, I2C, BIOS, PLL, and XTAL

PLLVDD/VID_PLLVDD



I2CC / I2CH(+ HDCP ROM) / I2CS

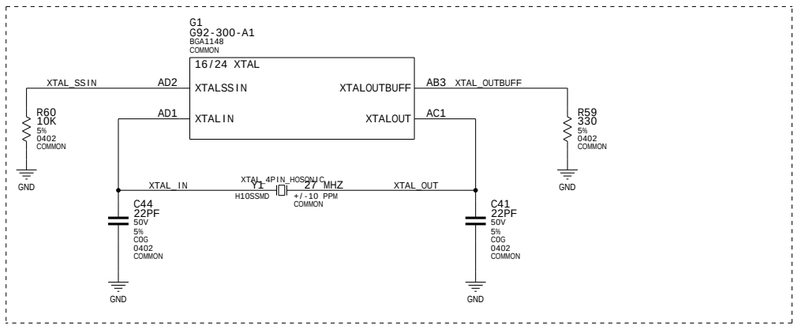


MISC NET RULES

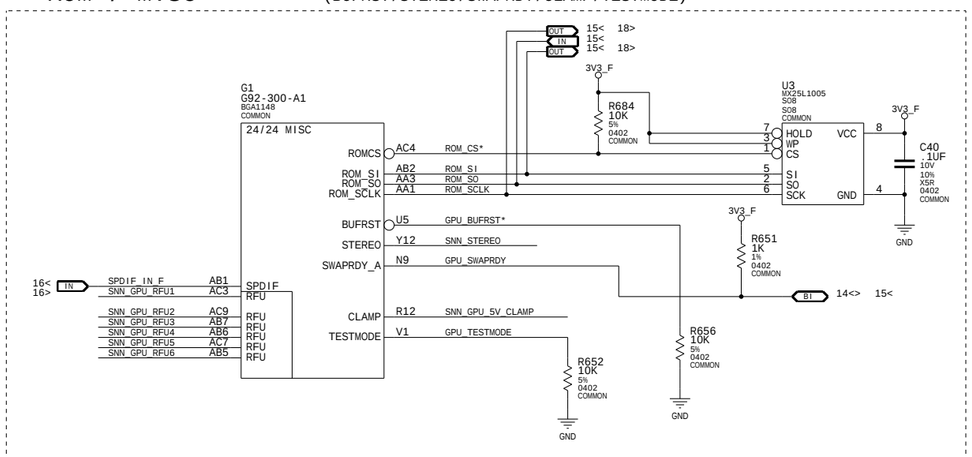
NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
I2CH_SCL	3	50OHM	
I2CH_SDA	3	50OHM	
I2CS_SCL	3	50OHM	
I2CS_SDA	3	50OHM	
I2CS_SCL_R	3	50OHM	
I2CS_SDA_R	3	50OHM	
ROM_CS*	3	50OHM	
ROM_SI	3	50OHM	
ROM_SO	3	50OHM	
ROM_SCLK	3	50OHM	
GPU_SWAPRDY	3	50OHM	
GPU_TESTMODE	3	50OHM	
GPIO0_DVI_A_HPD	3	50OHM	
GPIO1_DVI_C_HPD	3	50OHM	
GPIO4_FAN_PWM	3	50OHM	
GPIO5_VSEL0	3	50OHM	
GPIO6_VSEL1	3	50OHM	
GPIO7_FAN_TACH	3	50OHM	
GPIO8_THERM_OVERT*	3	50OHM	
GPIO11_RASTER_SYNC	3	50OHM	
XTAL_SSIN	1	50OHM	
XTAL_IN	1	50OHM	
XTAL_OUT	1	50OHM	
XTAL_OUTBUFF	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
GPU_VID_PLLVDD	1.2V	0.05A	12MIL
GPU_VID_PLLAVDD	1.2V	0.05A	12MIL
GPU_PLLVDD	1.2V	0.05A	12MIL
GPU_PLLAVDD	1.2V	0.05A	12MIL
GPU_H_PLLAVDD	1.2V	0.05A	12MIL

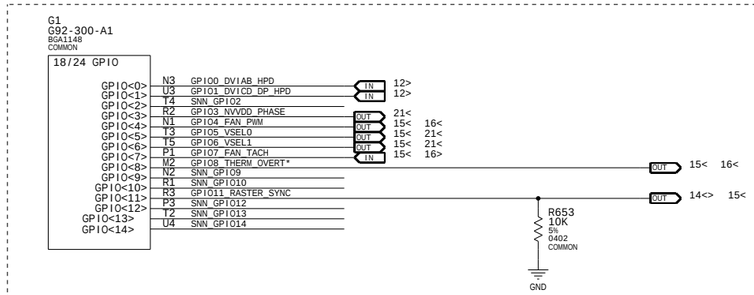
XTAL



ROM / MISC (BUFRST/STEREO/SWAPRDY/CLAMP/TESTMODE)



GPIO



GPIO Assignment Table

GPIO	I/O	Function
0	IN	DVI Hotplug Detect South
1	IN	DVI Hotplug Detect Nouth
2	N/A	Framelock Interrupt
3	OUT	Select Phase number of NVVDD
4	OUT	Fan PWM Output
5	OUT	Voltage Select 0
6	OUT	Voltage Select 1
7	IN	Fan Tach Input
8	OUT	THERM_OVERT*
9	N/A	Not used
10	N/A	Not used
11	OUT	RASTER (SLI) SYNC
12	N/A	Not used
13	N/A	Not used
14	N/A	Not used

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	MISC: GPIO, I2C, BIOS, PLL, and XTAL

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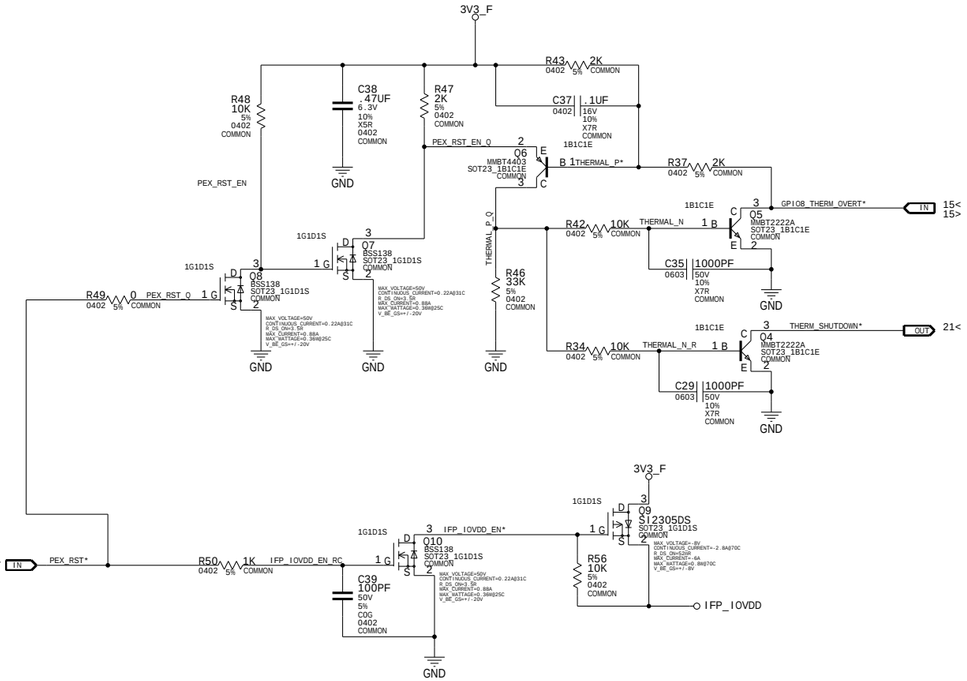
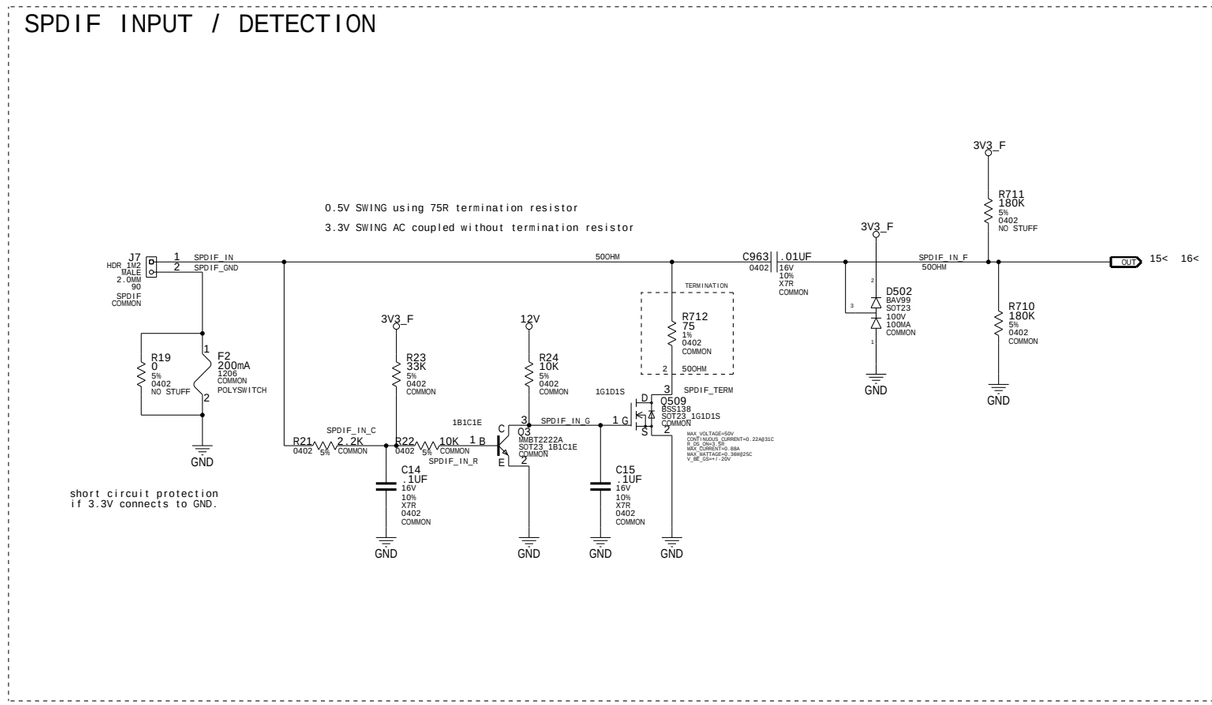
Page16: Thermal Control/Protection and SPDIF Input

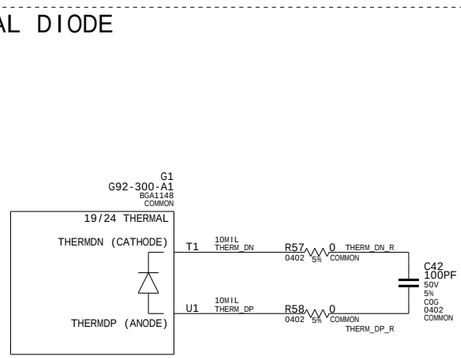
THERMAL PROTECTION/TMDS BACKDRIVE

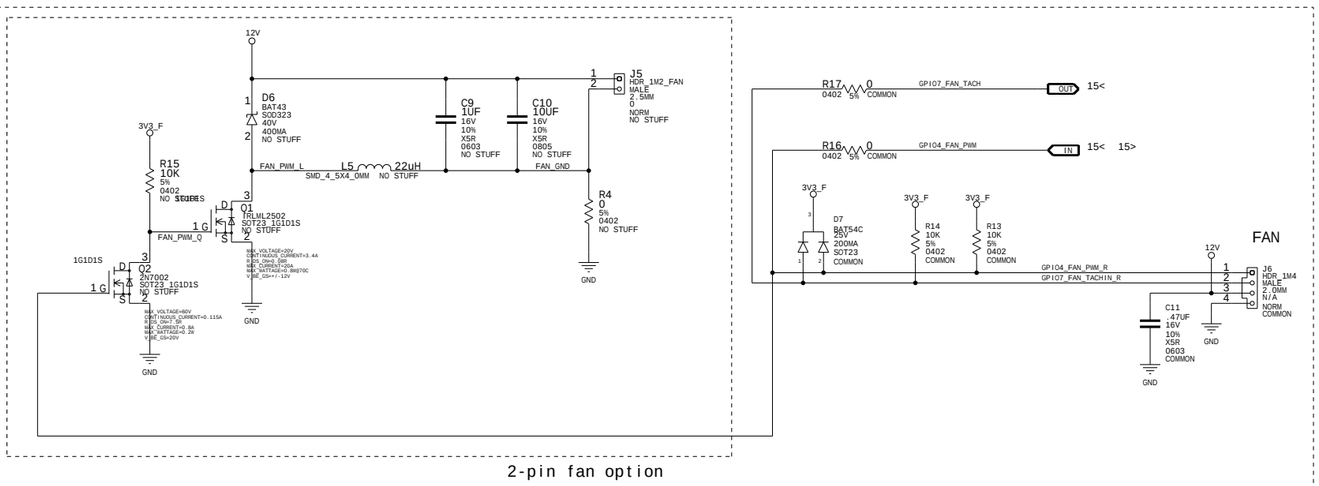


SPDIF INPUT / DETECTION



THERMAL DIODE





NET	IMPEDANCE	NV_CRITICAL_NET	MIN_LINE_WIDTH
SPDIF_IN	50OHM	1	
SPDIF_IN_C	50OHM	1	
SPDIF_IN_R	50OHM	1	
SPDIF_IN_G	50OHM	1	
SPDIFIN_TERM	50OHM	1	
SPDIF_IN_F	50OHM	1	

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	Thermal Control/Protection and SPDIF Input

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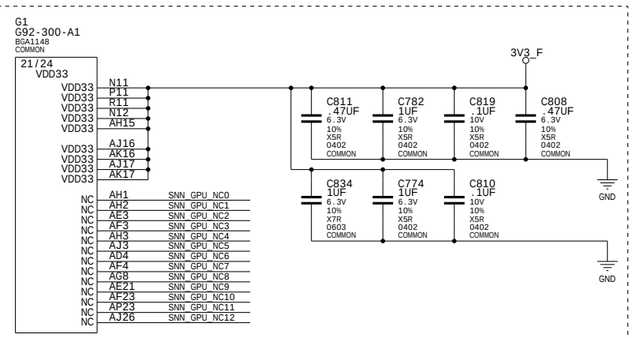
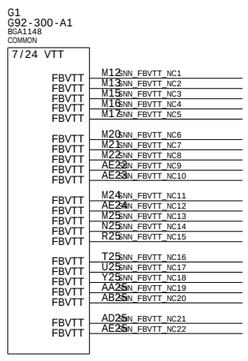
Page17: Power/GND and Decoupling

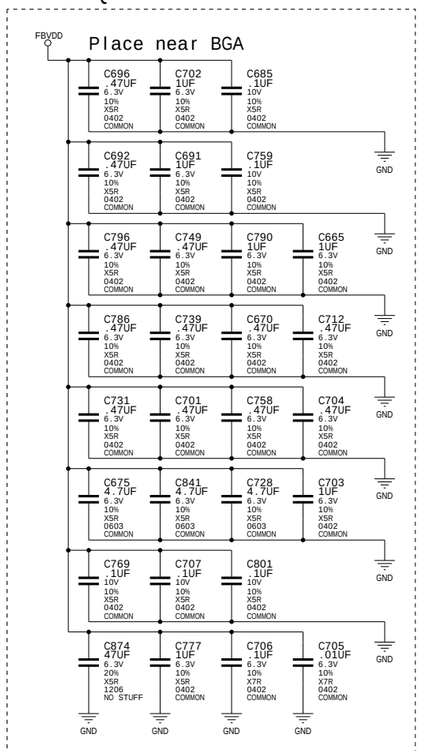
VDD33



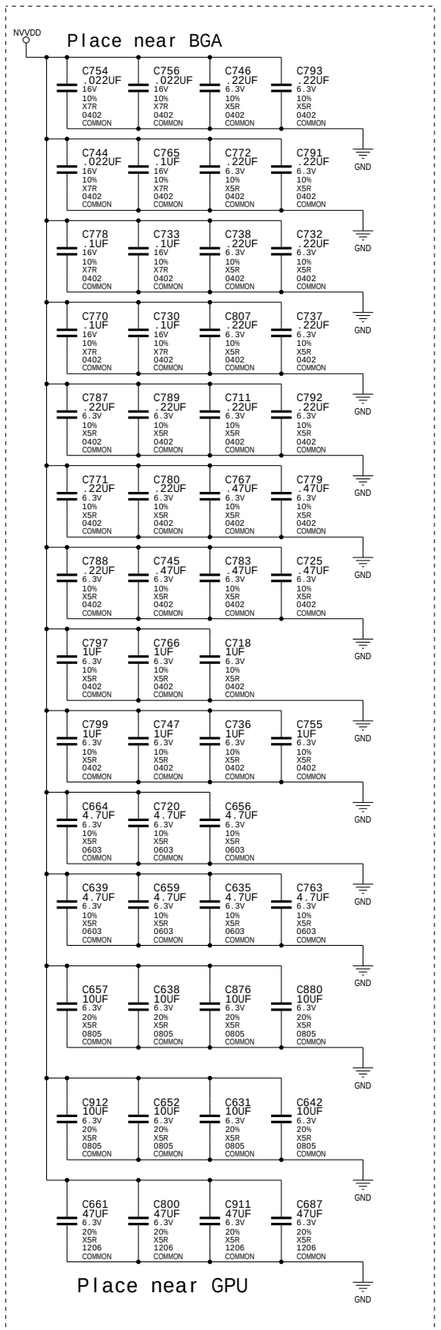
FBVTT

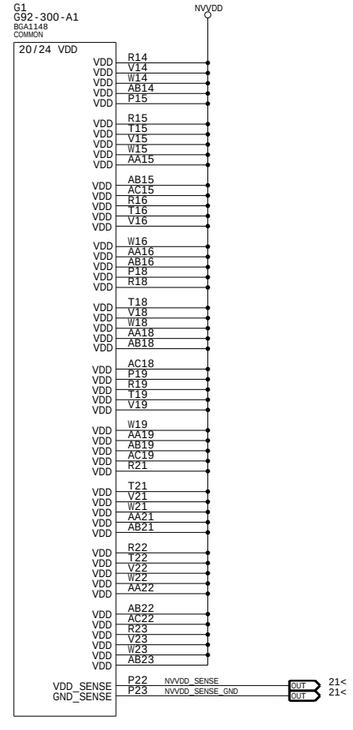


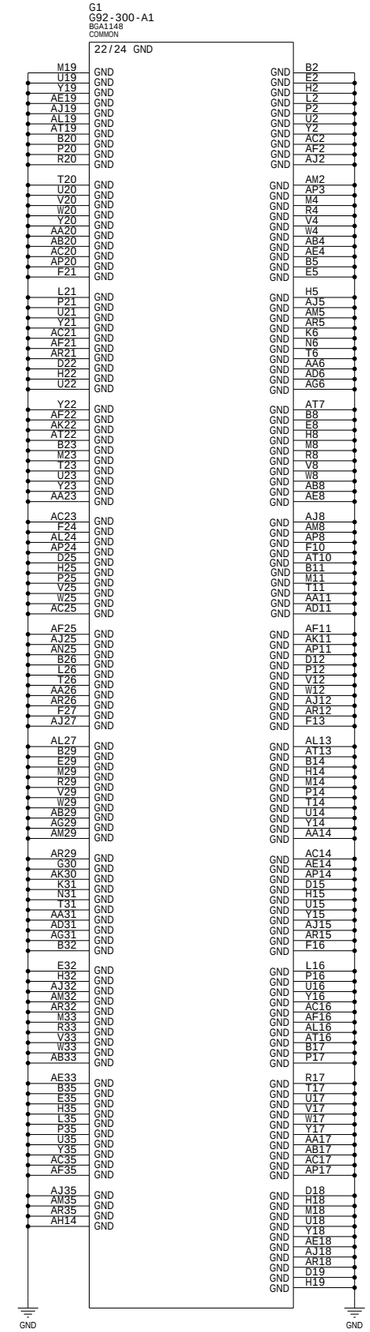
FBVDDQ



NVVDD







ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	Power/GND and Decoupling

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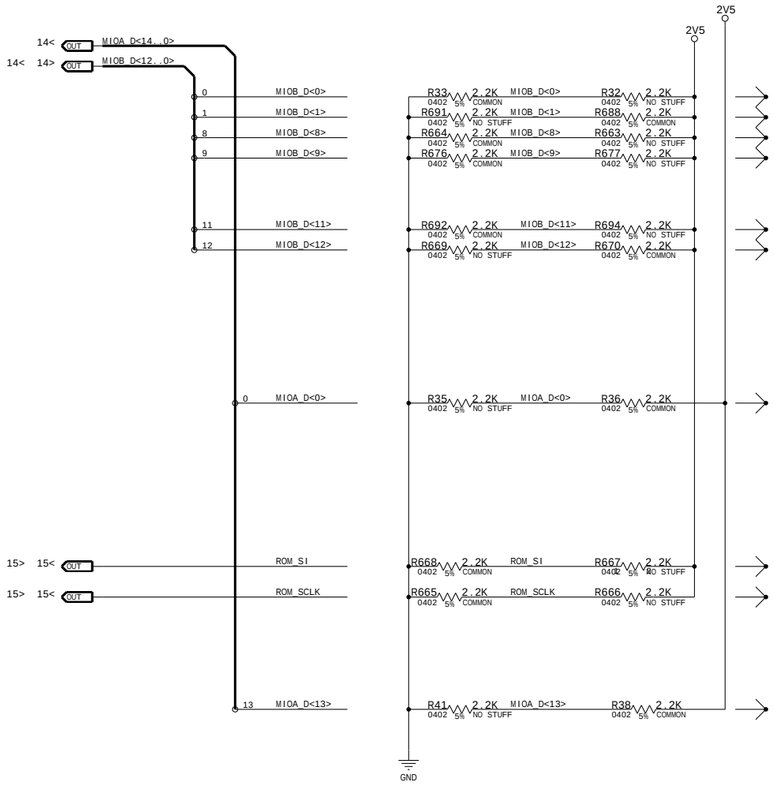
Page18: Configuration Straps and Mechanical

STRAPS



STRAP 0

		Samsung	Samsung	Hynix	Hynix	Qimonda
		256b 8Mx32 256MB	256b 16Mx32 512MB	256b 8Mx32 256MB	256b 16Mx32 512MB	256b 16Mx 32 521MB
* 02:	RAM_CFG[0]	1	1	0	0	1
* 03:	RAM_CFG[1]	1	1	1	1	0
* 04:	RAM_CFG[2]	1	0	1	0	0
* 05:	RAM_CFG[3]	0	0	0	0	0

4 3

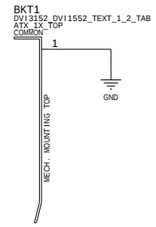
* 13:	PCI_DEVID[3]	DEVID =	0x0614	DT0	G92-279	0001 0100
* 28:	PCI_DEVID[4]		0x0614	DT50	G92-289	0001 0100

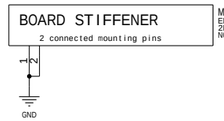
* 17:	PEX_PLL_EN_TERM100	Per G92 Guide (PEX term).. * Strap definition inverted - set to 0x1 to enable - set to 0x0 to disable

STRAP 1

* 12:	MIO_EN_33V_0	DEFAULT = 1 (3.3V) MIOA = 0 (2.5V)
* 13:	MIO_EN_33V_1	DEFAULT = 1 (3.3V) MIOB = 0 (2.5V)
* 15:	SLOT_CLK_CFG	DISABLE = 0; ENABLE = 1

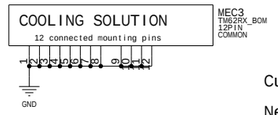
MECHANICAL





Top edge stiffener

Hockey stick



Currently it's a preliminary symbol.

New fansink will be updated to BOM.

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	Configuration Straps and Mechanical

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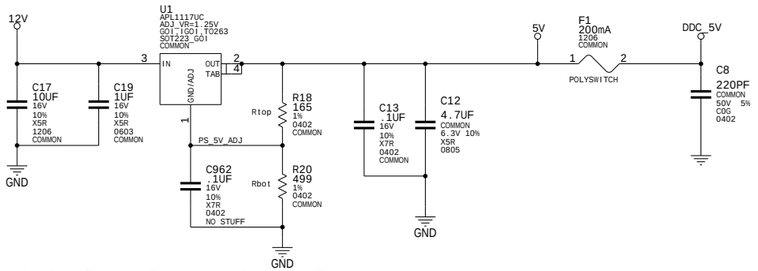
Page 19:Power Supply: 5V, 5V_DDC, 1v8, 2V5,PEX_PLLVDD Option

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
DDC_5V	DDC_5V	0.1A	12MIL	5V
5V	5V	0.15A	12MIL	5V
PEX_PLLVDD	PEX_PLLVDD	0.12A	12MIL	1.1V
1V8	1V8	0.12A	12MIL	1.8V
2V5	2V5	0.8A	12MIL	2.5V

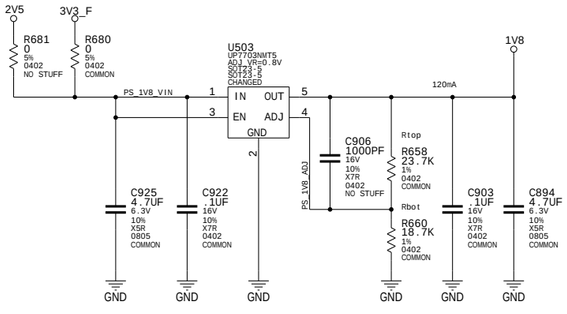
5V REGULATOR

5V DDC



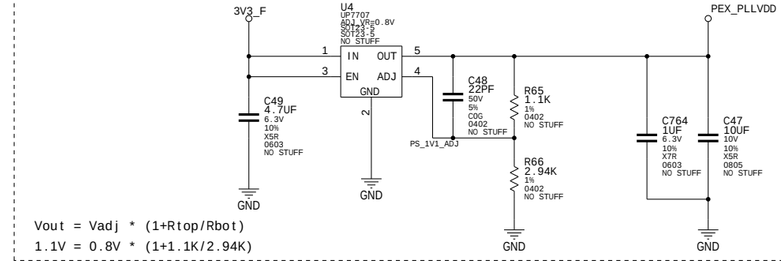
Vout = Ref*(1+(Rbot/Rtop))+Iadj* Rbot
5.06V = 1.25*(1+(499/165))+60uA* 499

IFP PLL Supply 1.8V



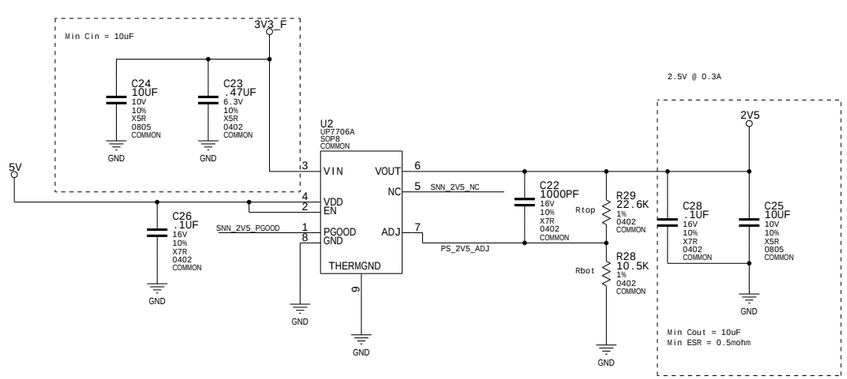
Vout = Vadj * (1+Rtop/Rbot)
1.813V = 0.8V * (1+23.7K/18.7K)

PEX_PLLVDD Optional



Vout = Vadj * (1+Rtop/Rbot)
1.1V = 0.8V * (1+1.1K/2.94K)

MIO_VDD 2.5V



Vout = VRef * (1+(Rtop/Rbot))
2.5V = 0.8V * (1+(22.6K/10.5K))

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	Power Supply: 5V, STEREO_5V, 2V5, DP_PWR

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NV_PN	600-10363-0000-100 A		
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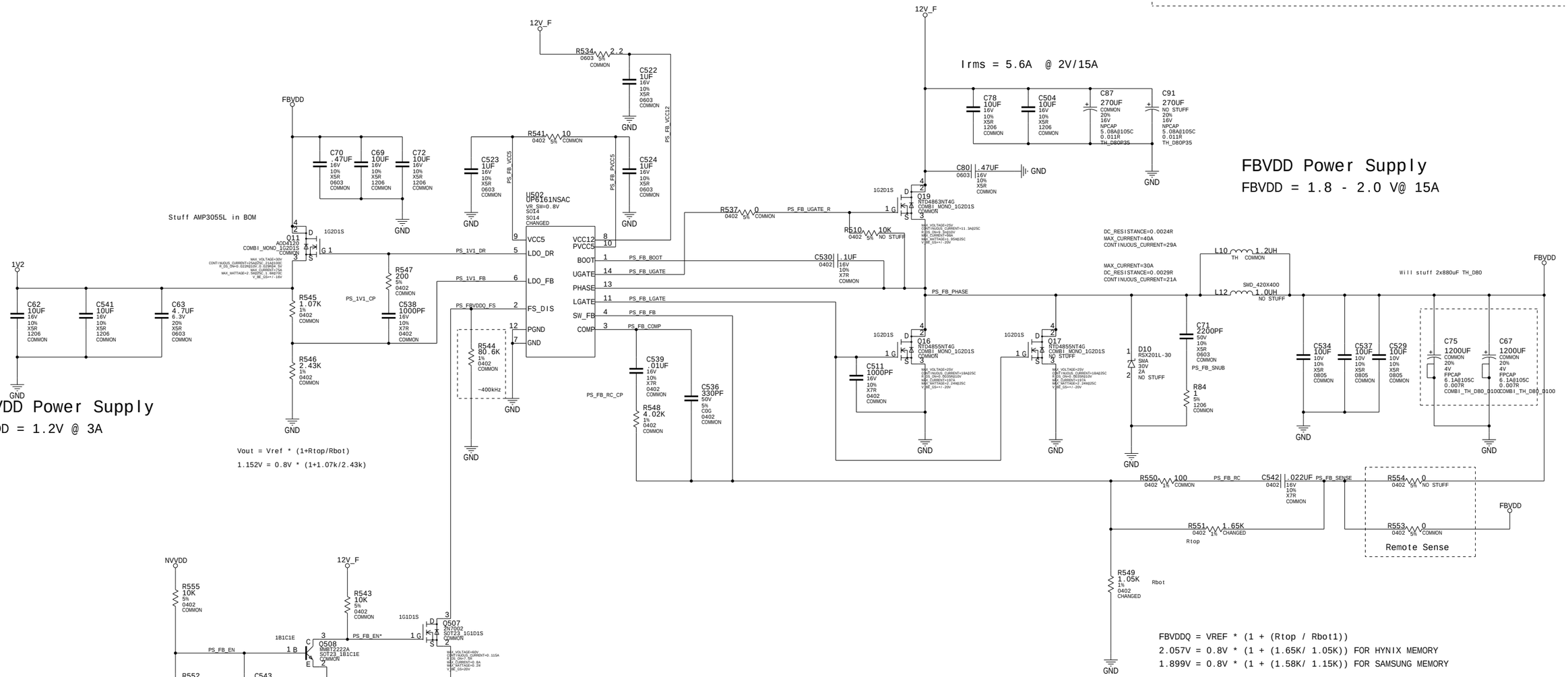
Page20:POWER SUPPLY: FBVDD,PEX_VDD

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
FBVDD	15A	20MIL	1.9V
1V2	3A	16MIL	1.1V



ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	Power Supply: FBVDD/Q, 8V5

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Page21:POWER SUPPLY: NVVDD

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
NVVDD	60A	20MIL	1.1V

Irms = 11.4A @ 1.05V/60A/Two phase

NVVDD Power Supply

NVVDD = 1.05-1.1V @ 55-60A

300KHz per phase

NVVDD ENABLE

NVVDD = 0.6 * (1 + Rtop/Rbot)

GPIO6	GPIO5	NVVDD
0	0	0.95V (Low perfmode)
1	0	1.05V (VB0)
1	1	1.10V (VB1)

ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	Power Supply: NVVDD Regulator

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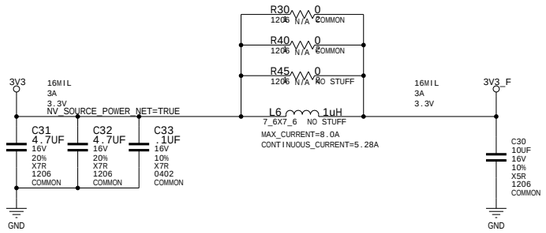
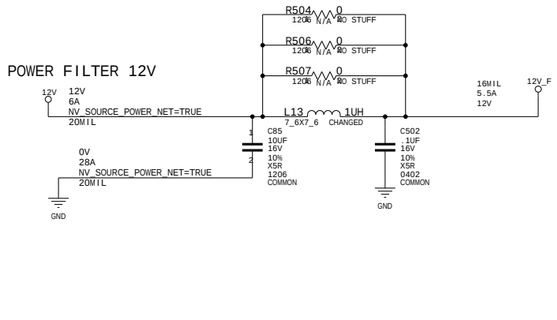
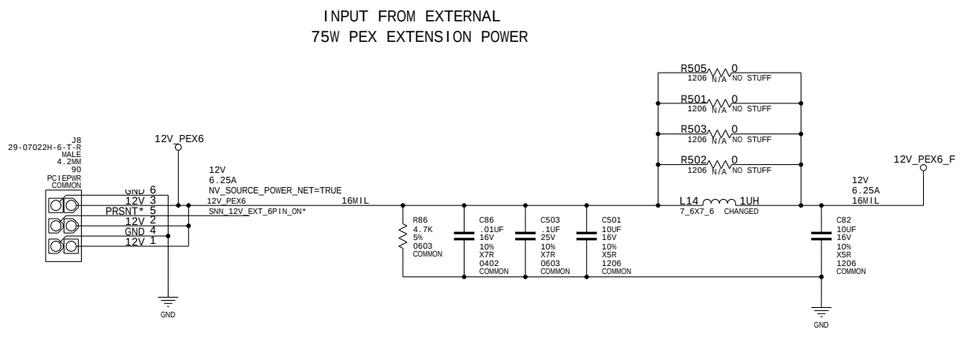
Page22: Power Supply: Filter of 12V,12V_PEX6,3V3







ASSEMBLY	P363 G92-279 512MB GDDR3 16Mx32 DVI-I+DVI-I
PAGE DETAIL	Power Supply: Filter of 3V3, 12V, 12V_PEX6

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