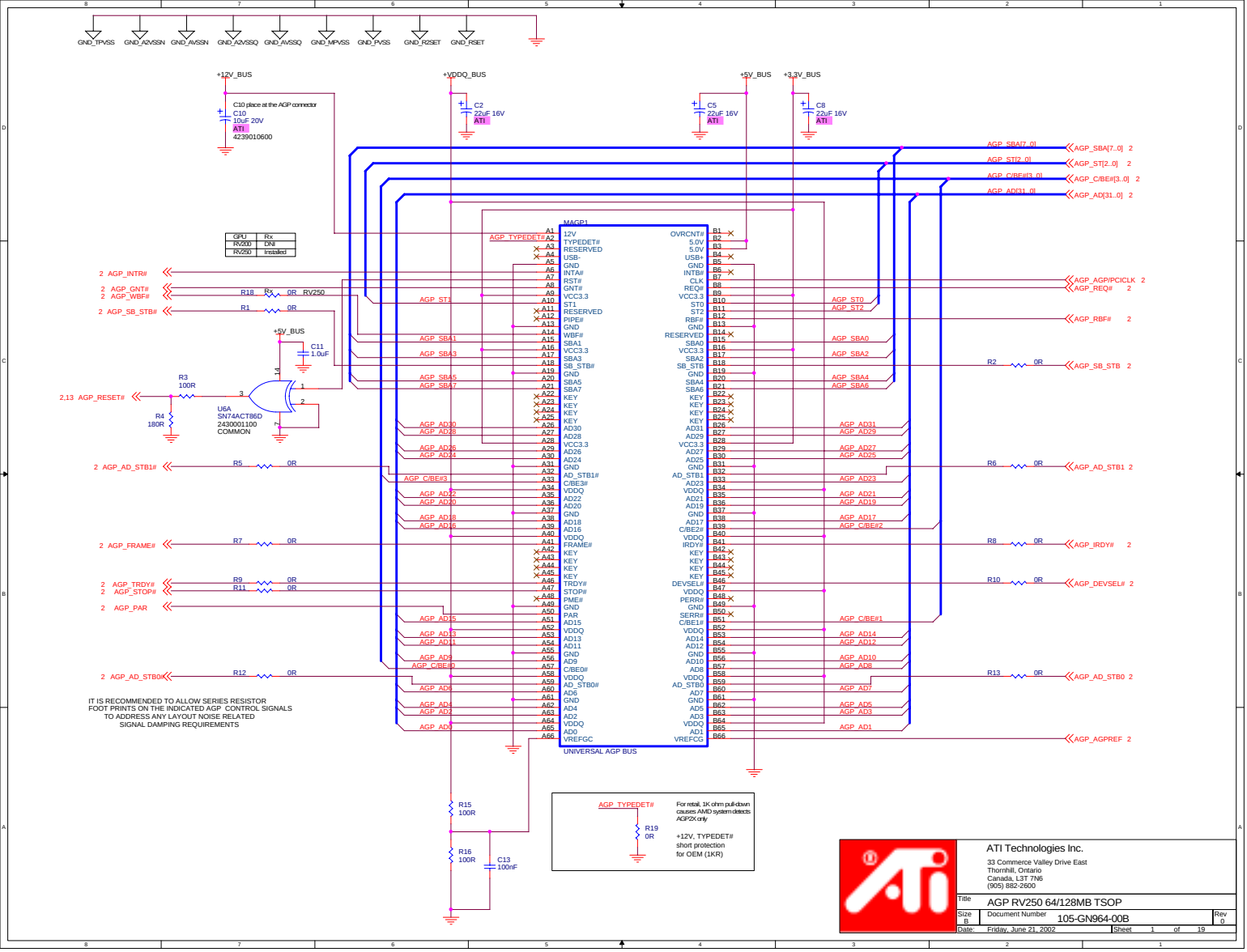

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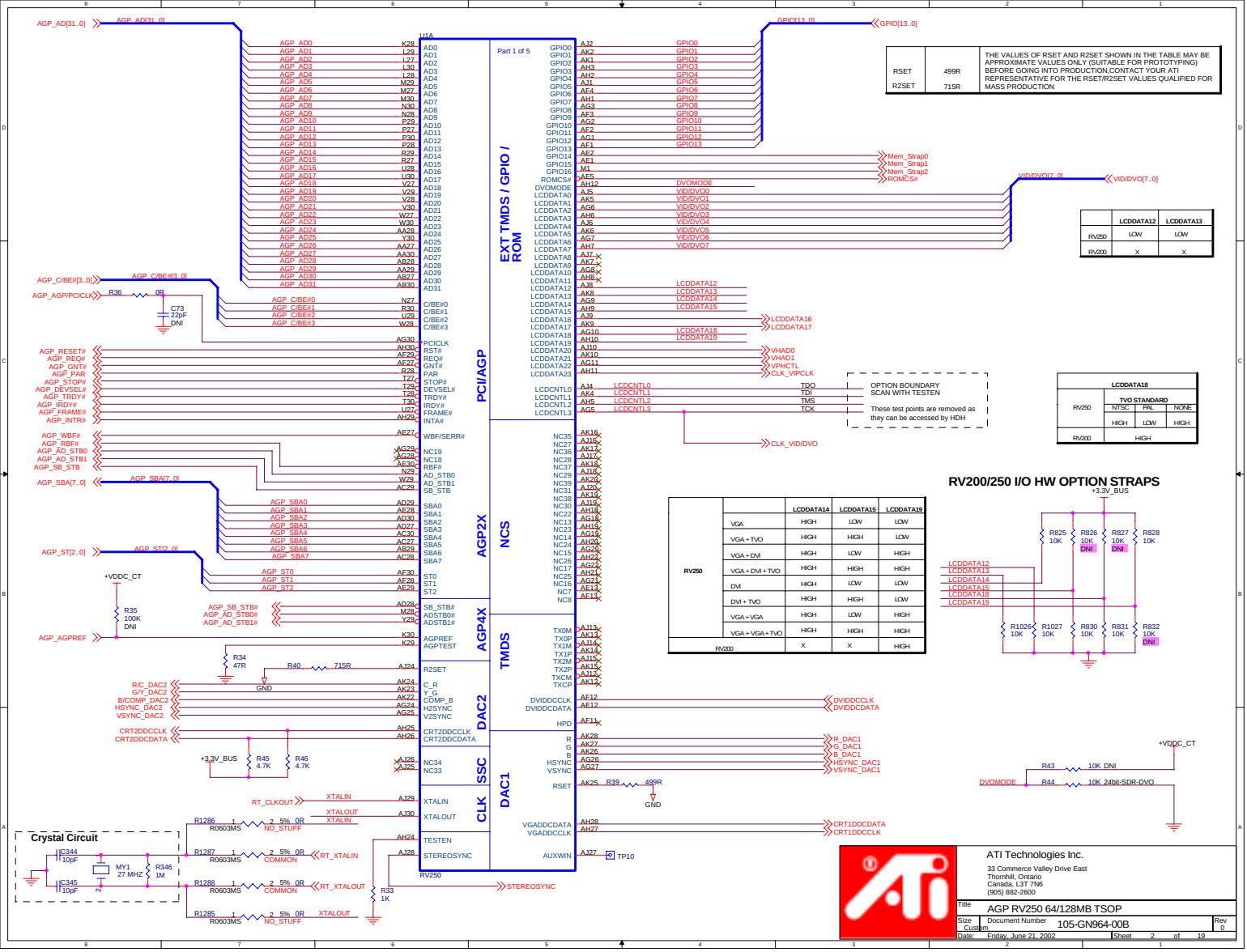
Title	AGP RV250 64/128MB TSOP	
Size B	Document Number 105-GN964-00B	Rev 0
Date: Friday, June 21, 2002	Sheet 1 of 19	


U1A
Part 1 of 5
PCI/AGP
AGP2X
NCS
AGP4X
TMDS
DAC2
SSC
CLK
DAC1
EXT TMDS / GPIO / ROM
RV250
RV200
RSET 499R
R2SET 715R
THE VALUES OF RSET AND R2SET SHOWN IN THE TABLE MAY BE APPROXIMATE VALUES ONLY (SUITABLE FOR PROTOTYPING) BEFORE GOING INTO PRODUCTION,CONTACT YOUR ATI REPRESENTATIVE FOR THE RSET/R2SET VALUES QUALIFIED FOR MASS PRODUCTION
OPTION BOUNDARY SCAN WITH TESTEN
These test points are removed as they can be accessed by HDH
RV200/250 I/O HW OPTION STRAPS
Crystal Circuit
ATI Technologies Inc.
33 Commerce Valley Drive East
Thornhill, Ontario
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(905) 882-2600
Title AGP RV250 64/128MB TSOP
Size Custom
Document Number 105-GN964-00B
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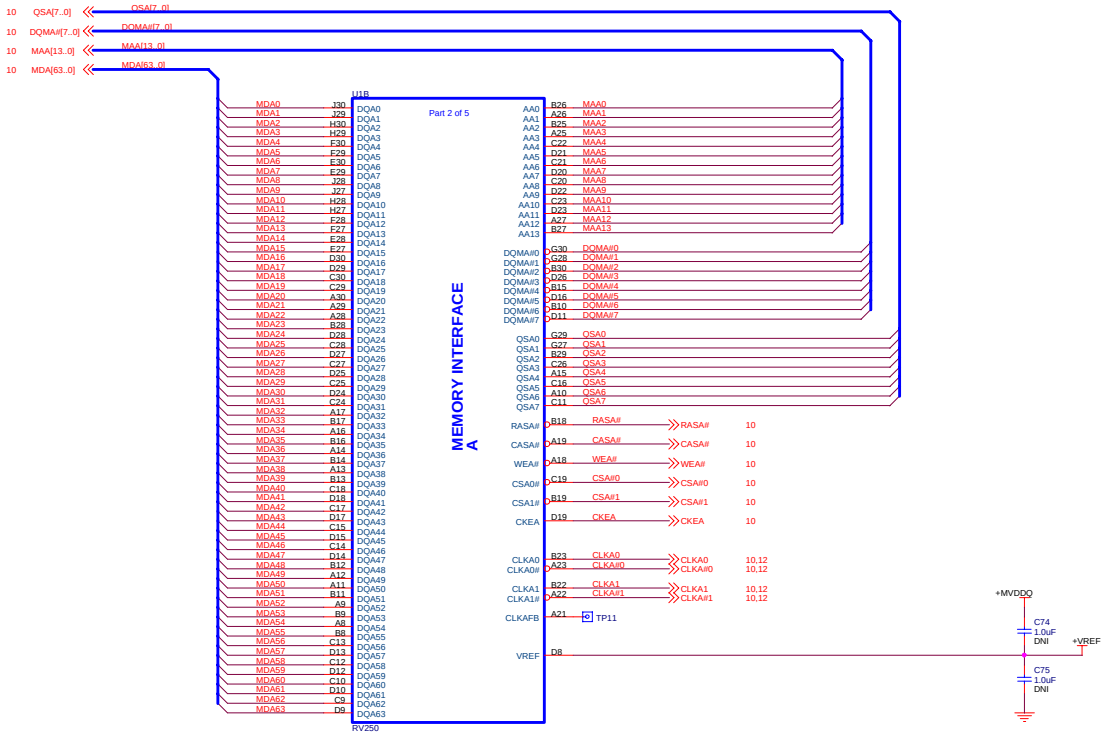
MEMORY CHANNEL A



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Title	AGP RV250 64/128MB TSOP		
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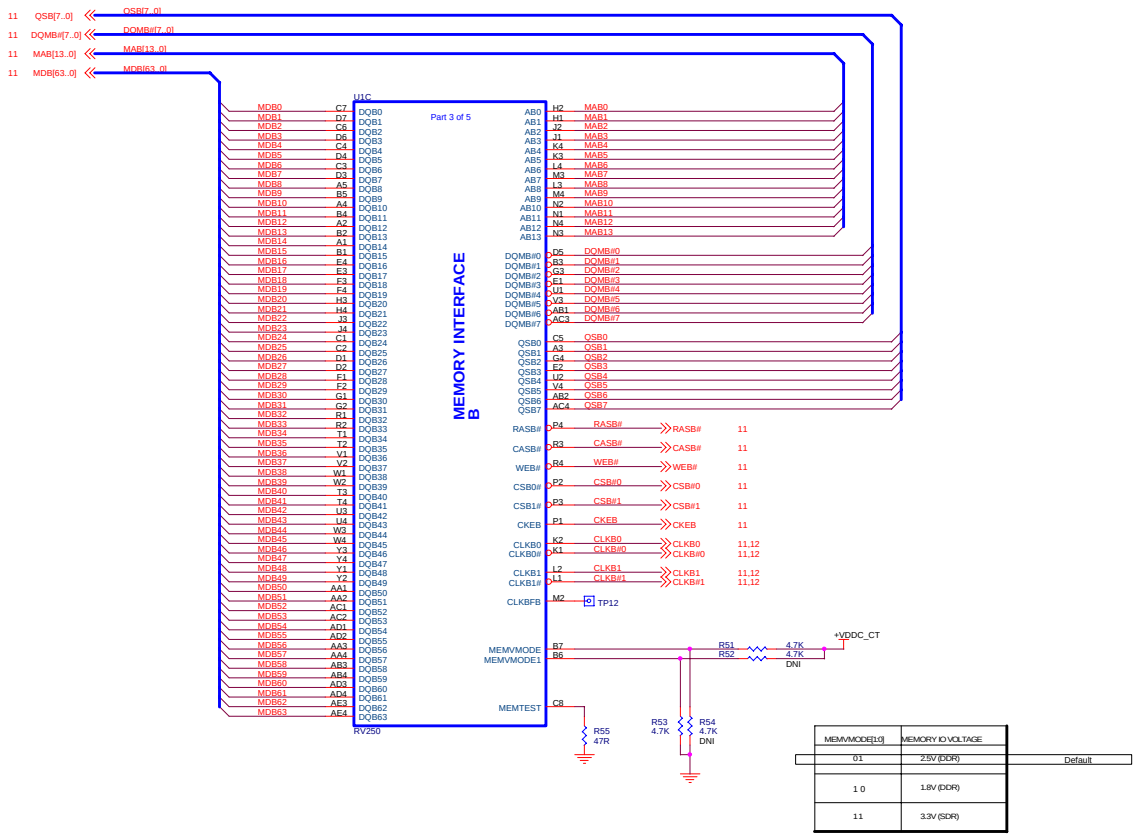
MEMORY CHANNEL B



MEMVMODE[1:0]	MEMORY IO VOLTAGE	
0 1	2.5V (DDR)	Default
1 0	1.8V (DDR)	
1 1	3.3V (SDR)	

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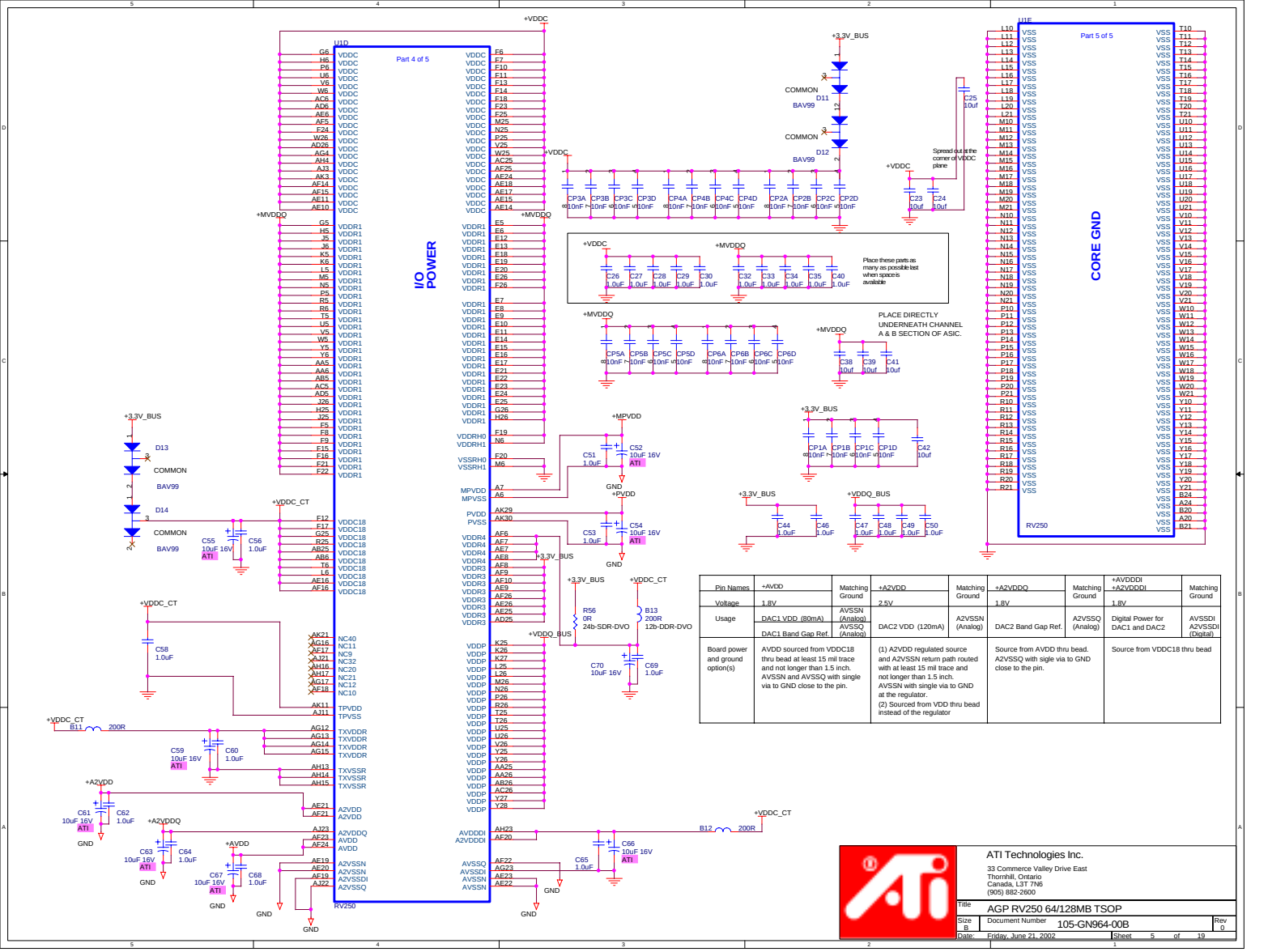

Pin Names	+AVDD	Matching Ground	+A2VDD	Matching Ground	+A2VDDQ	Matching Ground	+AVDDDI +A2VDDDI	Matching Ground
Voltage	1.8V		2.5V		1.8V		1.8V	
Usage	DAC1 VDD (80mA)	AVSSN (Analog)	DAC2 VDD (120mA)	A2VSSN (Analog)	DAC2 Band Gap Ref.	A2VSSQ (Analog)	Digital Power for DAC1 and DAC2	AVSSDI A2VSSDI (Digital)
	DAC1 Band Gap Ref.	AVSSQ (Analog)						
Board power and ground option(s)	AVDD sourced from VDDC18 thru bead at least 15 mil trace and not longer than 1.5 inch. AVSSN and AVSSQ with single via to GND close to the pin.		(1) A2VDD regulated source and A2VSSN return path routed with at least 15 mil trace and not longer than 1.5 inch. AVSSN with single via to GND at the regulator. (2) Sourced from VDD thru bead instead of the regulator		Source from AVDD thru bead. A2VSSQ with sigle via to GND close to the pin.		Source from VDDC18 thru bead	

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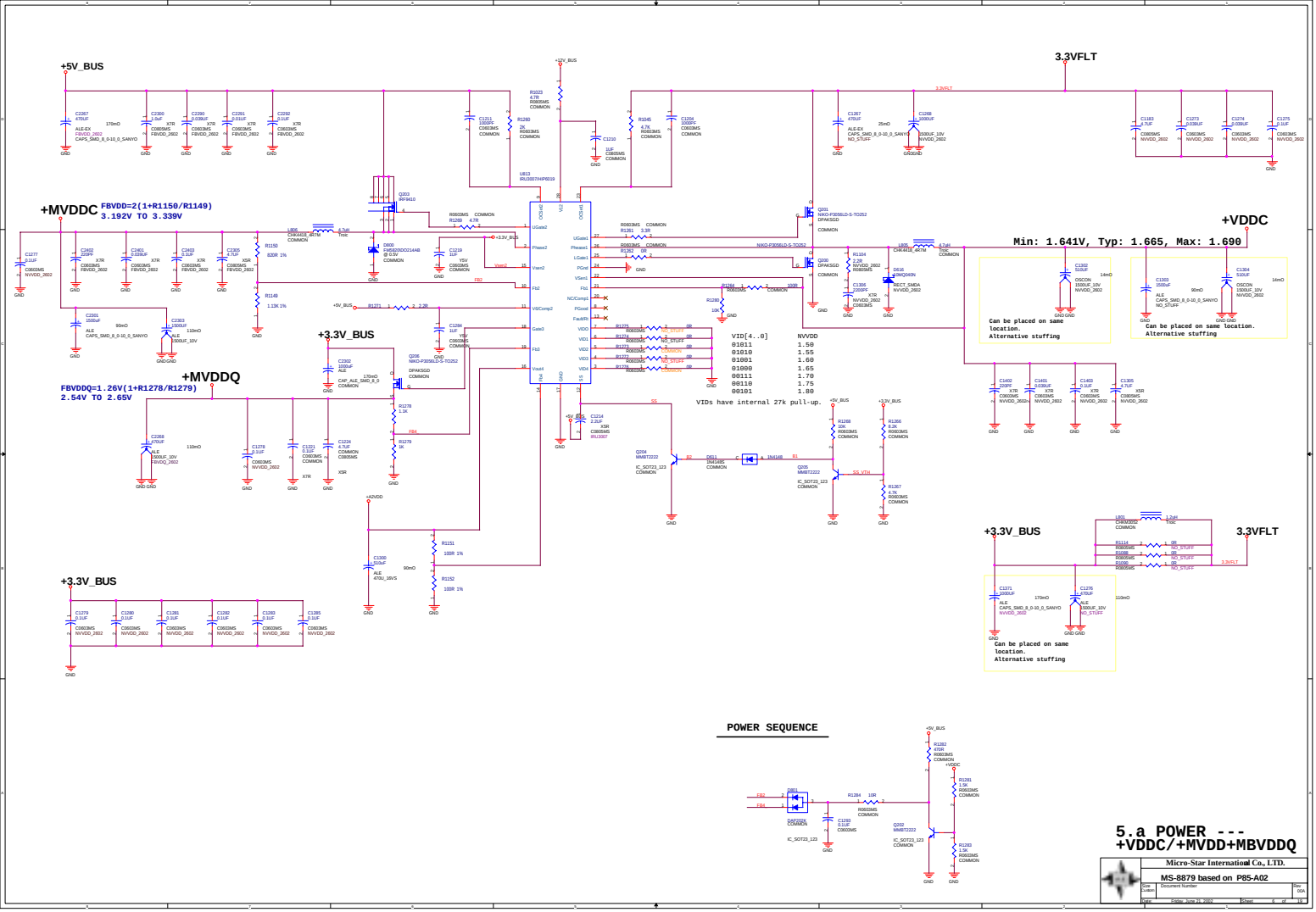
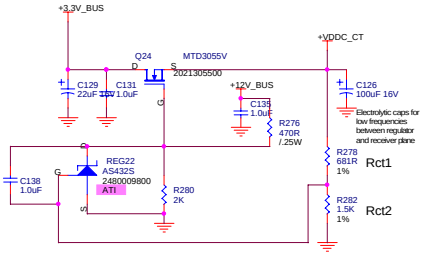

+5V_BUS
3.3VFLT
+MVDDC
FBVDD=2(1+R1150/R1149)
3.192V TO 3.339V
+VDDC
Min: 1.641V, Typ: 1.665, Max: 1.690
Can be placed on same location.
Alternative stuffing
+3.3V_BUS
+MVDDQ
FBVDDQ=1.26V(1+R1278/R1279)
2.54V TO 2.65V
VID[4..0] NVDD
01011 1.50
01010 1.55
01001 1.60
01000 1.65
00111 1.70
00110 1.75
00101 1.80
VIDs have internal 27k pull-up.
POWER SEQUENCE
5.a POWER ---
+VDDC/+MVDD+MBVDDQ
Micro-Star International Co., LTD.
MS-8879 based on P85-A02

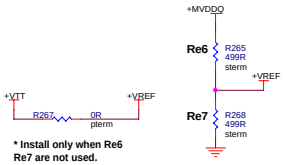
Regulator for VDDC_CT (Core Transform) and AVDD/A2VDDQ/AVDDDI/A2VDDDI TXVDDR, LVDDRx

Vin = 3.3V AGP
Vout = 1.8V
Iout = 350mA + 100mA + 50mA = 500mA MAX
Iout = 600mA MAX (with PVDD/TPVDD)

	Rct1		Rct2	
1.8V	681R	3240681000	1.5K	3230015200
1.9V	536R	3240536000	1K	3240100100



Vref Voltage



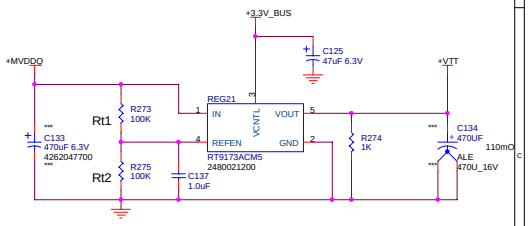
*** Install only when Re6 Re7 are not used.**

Use localized Vref on the memory page

Regulator for VTT (Termination)

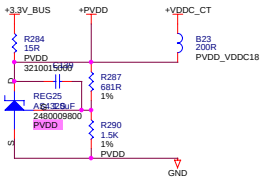
Vin = MVDDQ
Vout = 1.25V
Iout = 2000mA MAX
Iout = 750mA Est. MAX

	Rt1		Rt2	
1.25V	1K	3240100100	1K	3240100100
1.3V	1.0K	3240100100	1.02K	3240102100



Regulator for PVDD (R200 PLLs) and optional TPVDD (TMDS PLLs)

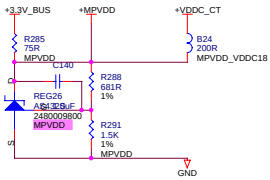
Vin = 3.3V AGP
Vout = +1.8V
Iout = 25mA MAX (PVDD only)
Iout = 100mA MAX (PVDD + TPVDD)
(Optional)



If PVDD and TPVDD are used from the same regulator, Rr must be change to 15R P/N3210015000 to provide enough current.

Regulator for MPVDD (Memory PLLs)

Vin = 3.3V AGP
Vout = +1.8V
Iout = 10mA MAX



AVDD/A2VDDQ (1st DAC & 2nd DAC Band Gap)

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Title	AGP RV250 64/128MB BGA	
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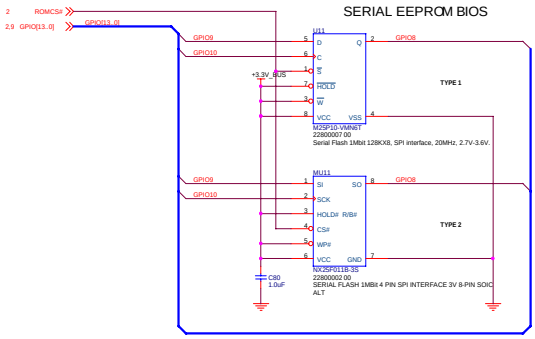

<Variant Name>

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Title: AGP RV250 64/128MB TSOP

Size: C | Document Number: 105-GN964-00B | Rev: 0

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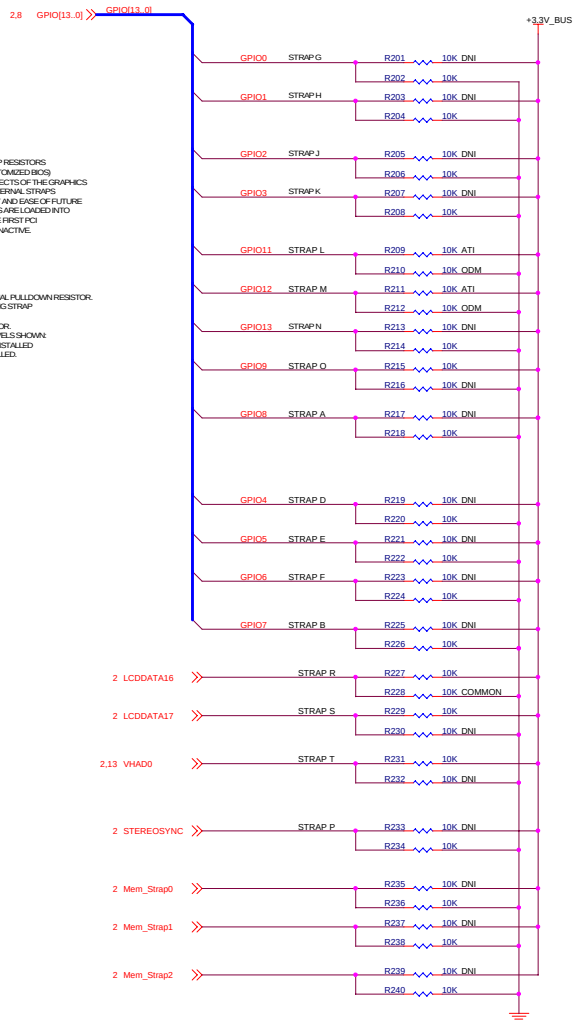
OPTION STRAPS



NOTE: THE M7
SUPPORTS THE USE OF STRAP RESISTORS
(AS AN ALTERNATIVE TO CUSTOMIZED BIOS)
TO CONFIGURE CERTAIN ASPECTS OF THE GRAPHICS
SUBSYSTEM. THE USE OF EXTERNAL STRAPS
PROVIDES ADDED FLEXIBILITY AND EASE OF FUTURE
UPGRADE. STRAPPED VALUES ARE LOADED INTO
INTERNAL REGISTERS ON THE FIRST PCI
COMMAND AFTER RESET# IS INACTIVE.

NOTE:

THE I/O BUFFERS USE INTERNAL PULLDOWN RESISTOR.
THIS DICTATES THE FOLLOWING STRAP
CONFIGURATION:
STRAP TO VCC VIA 10K RESISTOR.
THIS PROVIDES THE LOGIC LEVELS SHOWN:
'0' WHEN 10K RESISTOR NOT INSTALLED
'1' WHEN 10K RESISTOR INSTALLED.

STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM **1011 - Serial M25P10 ROM (ST), chip IDis from ROM** 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1001
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000 (internal pull-down)
VGA_DISABLE	GPIO(7)	**0 - VGA controller capabilliity enableed.** 1 - The device will not be recognized as the systemis VGA controller.	0
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select **00 - single function device.** 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	00
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

<Variant Name>

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Title	AGP RV250 64/128MB TSOP	
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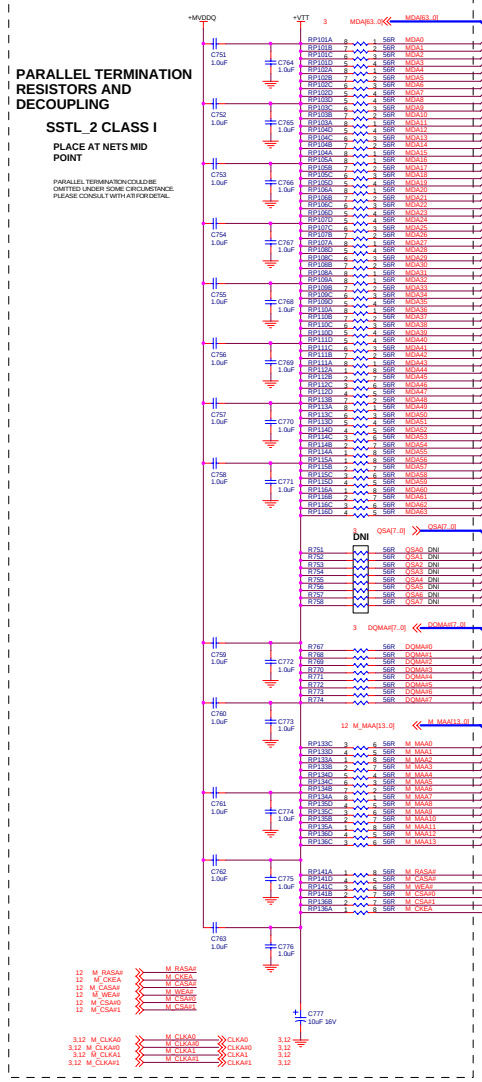
TERMINATION FOR MEMORY CHANNEL A

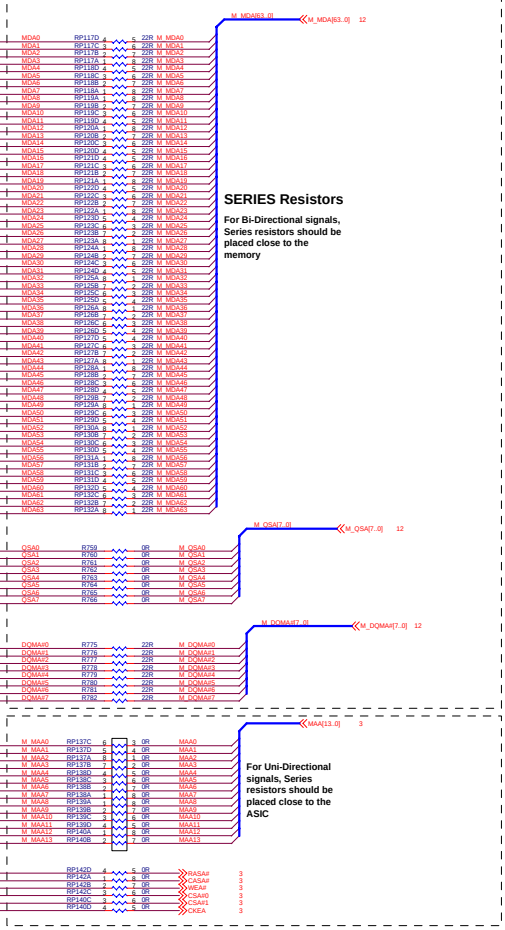
PARALLEL TERMINATION RESISTORS AND DECOUPLING

SSTL_2 CLASS I

PLACE AT NETS MID POINT

PARALLEL TERMINATION COULD BE OMITTED UNDER SOME CIRCUMSTANCE. PLEASE CONSULT WITH ATI FOR DETAIL.





SERIES Resistors

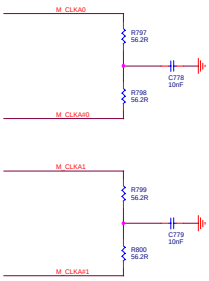
For Bi-Directional signals, Series resistors should be placed close to the memory

For Uni-Directional signals, Series resistors should be placed close to the ASIC

CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



Symbol change 56R instead of 121R

<Variant Name>

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Title	AGP RV250 64/128MB TSOP	
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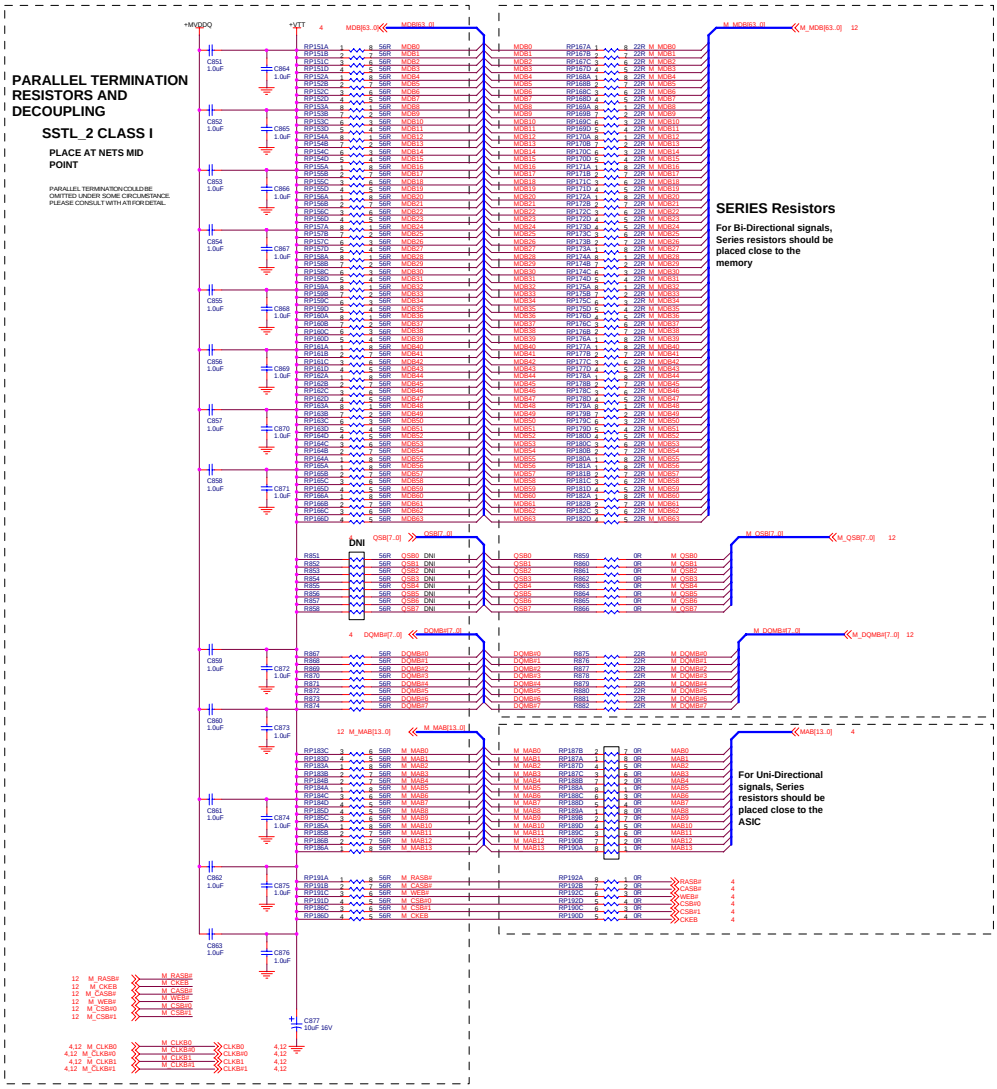
TERMINATION FOR MEMORY CHANNEL B

PARALLEL TERMINATION RESISTORS AND DECOUPLING

SSTL_2 CLASS I

PLACE AT NETS MID POINT

PARALLEL TERMINATION COULD BE OMITTED UNDER SOME CIRCUMSTANCE. PLEASE CONSULT WITH ATI FOR DETAIL.



SERIES Resistors

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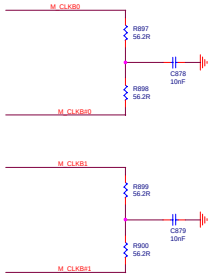

There are two standard Terminations that are supported by for DDR memory. Series or Parallel. Please consult design guide for performance impacts.

<Variant Name>

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Title	AGP RV250 64/128MB TSOP		
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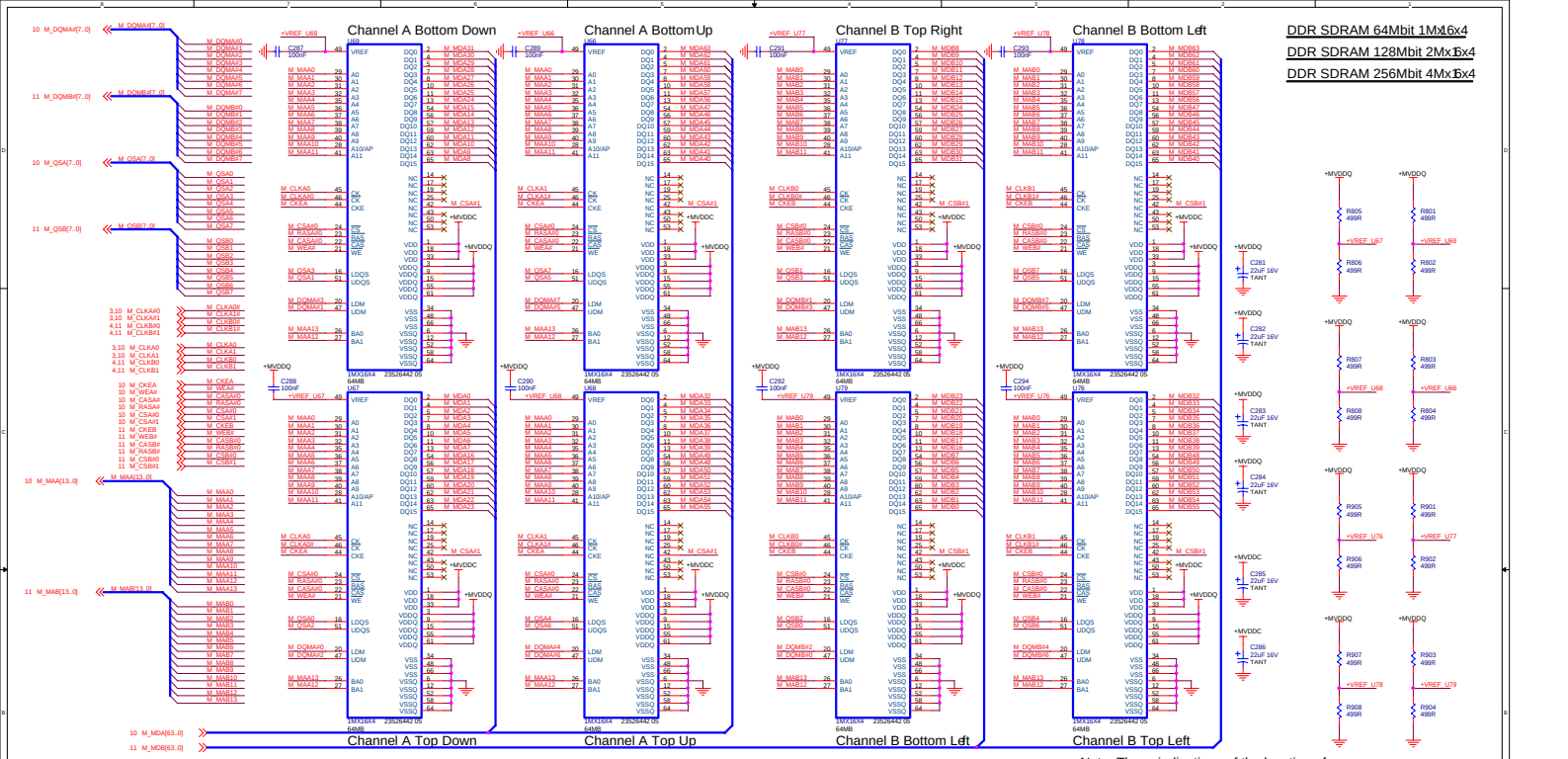
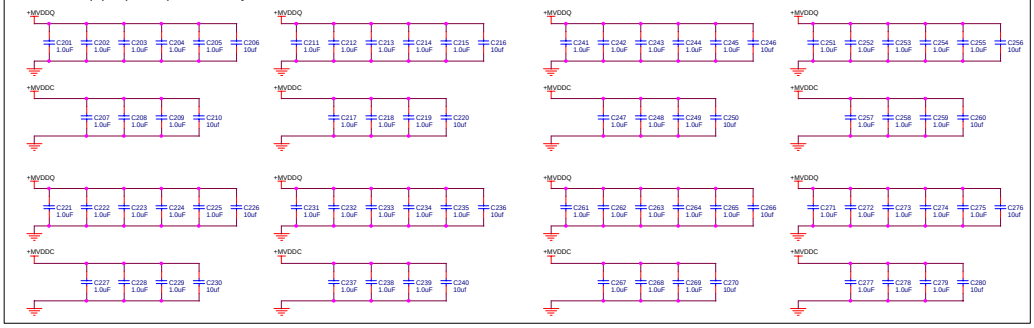


Note: These indications of the location of the memory for the solder side (bottom) are looking thru from the component side.

Put 1 1uF cap per power pin of memory



Part number for 8Mx16?

DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

<Variant Name>

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Layout Guide line of T HEATER

#1 : C385 and C386 have to be placed as close as possible to the pins of Rage THEATER

#2 : C397 should be placed close to J2

OPTIONAL +3.3V REGULATOR

+5V_BUS REG1 3.3V IN OUT CASE ADJ RVDD +3.3V_BUS

C374 100nF C373 100uF R376 0R

+3.3V_BUS

C565 100nF C375 100nF C376 100nF C377 100nF C378 22uF

U12

R1094 10R B76 3.3uH C926 47uF C927 100nF

R1095 10R B17 3.3uH C381 47uF C382 100nF

R1096 10R B77 3.3uH C928 47uF C929 100nF

R1097 10R B21 3.3uH C393 47uF C394 100nF

R1098 10R B34 3.3uH C399 47uF C400 100nF

RVDD PLLVDD

VAGCVDD VAGCVSS VAGCVSS VDACVDD VDACABVSS VDACJVSS VIND0 VIND1 VIND2 VIND3 VIND4 VIND5 VIND6 VIND7 VINGATEA VINGATEB CF CR VAGCCAP VIDEOGNDSENSE VCLAMPCAP VADCDVDD VADCAVDD VADCDVSS VADCAVSS COMP0 COMP1 COMP2 YF_COMP3 YR_COMP4 XTALIN XTALOUT TESTEN RESETB PLLVDD PLLVSS

CR C889 2.2uF C924 16pFX7R C925 22nF

C43 2.2uF YR C890 2.2uF

RT_XTALIN RT_XTALOUT AGP_RESETB CompR L28 3.3uH C891 330pF C892 330pF R1065 75.0R 1%

R392 3K3

VSSC VSSC VSSC VSSC VSSC VSSR VSSR VSSR VSSR VSSR VSSR VSSR VSSC VSSC

RAGE THEATER

SAD0 SAD1 SAD2 SAD3 SAD4 SAD5 SAD6 SAD7

DS_VIPCLK AS_HCTL SRDY_IRQB HAD0 HAD1 SDA SCL ADO ADIO WS BITCLK SPDIF BYTCLK SYNC V_RED C_GREEN COMP_BLUE RSET CLKOUT0_GPIO0 CLKOUT1_GPIO1 CLKOUT2_GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 PDATA0 PDATA1 PDATA2 PDATA3 PDATA4 PDATA5 PDATA6 PDATA7 PCLK

R195 10K R196 10K CLK_VIPCLK 2

R549 47K R197 10K +3.3V_BUS

R198 10K VHAD0 2,9 R199 10K VHAD1 2

R380 4.7K "DNI" +3.3V_BUS L0C1 R381 10K

MPPEN SPDIF R382 10K

R375 75.0R R377 75.0R R378 75.0R R384 10K

R140 107 R RT_CLKOUT 2

R139 150R

RP193A RP194A 33R VIDIDVO0 VIDIDVO1 VIDIDVO2 VIDIDVO3 VIDIDVO4 VIDIDVO5 VIDIDVO6 VIDIDVO7

VIDIDVO7..0 VIDIDVO[7..0] 2

R389 33R CLK_VIDIDVO 2

PLACE AS CLOSE TO THE RAGE THEATRE AS POSSIBLE.

TV-OUT

YR L8 3.3uH YRIN R1063 75.0R 1% C885 330pF C886 330pF

CR L9 3.3uH CRIN R1064 75.0R 1% C887 330pF C888 330pF

Y/R L4 1.8uH R379 75.0R 1% C383 82pF C384 82pF Luma_F Chroma_F Comp_F

C/G L2 1.8uH R383 75.0R 1% C387 82pF C388 82pF R508 0R

COMP/B L3 1.8uH R385 75.0R 1% C391 82pF C392 82pF COMP1

CVBS

14,15 G/Y_DAC2_F Luma Rm6 Rm1 R501 R891 0R TVO_ONLY 120R TVO_CRT Q91 2N7002E TVO_CRT Qm1 Rm7 R504 1.5K TVO_CRT Y/R

CREATE DUAL FOOTPRINT FOR BEAD 0603/0805

14,15 R/C_DAC2_F Chroma Rm8 Rm2 R502 R892 0R TVO_ONLY 120R TVO_CRT Q92 2N7002E TVO_CRT Qm2 Rm9 R505 1.5K TVO_CRT C/G

CREATE DUAL FOOTPRINT FOR BEAD 0603/0805

14,15 B/COMP_DAC2_F Comp Rm10 Rm3 R503 R893 0R TVO_ONLY 120R TVO_CRT Q93 2N7002E TVO_CRT Qm3 Rm11 R506 1.5K TVO_CRT COMP/B

CREATE DUAL FOOTPRINT FOR BEAD 0603/0805

	Install	DNI
VIDEO-OUT&CRT2	Rm1,Rm2,Rm3,Qm1,Qm2, Qm3,Rm7,Rm8,Rm11,Rm12, Cm1,Cm2,Rm13,Rm14,Dm1	Rm6,Rm8,Rm10, Cm3,Cm4,Cm5
VIDEO-OUT ONLY	Rm6,Rm8,Rm10, Cm3,Cm4,Cm5	Rm1,Rm2,Rm3,Qm1,Qm2, Qm3,Rm7,Rm9,Rm11,Rm12, Cm1,Rm13,Rm14,Dm1,Cm2

Cm1 C508 100nF TVO_CRT

+5V_BUS U7A SN74AC786D 24300011 00 COMMON

Dm1 BAV99 TVO_CRT D91

15 VSYNC_DAC2_B R507 0R TVO_CRT Rm14 C507 47nF TVO_CRT Cm2 R510 5.1M TVO_CRT Rm13 Rm12 R509 10K TVO_CRT

Layout Guide line of T HEATER

#1 : C27 and C28 have to be placed as close as possible to the respective pins of Rage THEATER

#2 : VINGND should be seperated from Digital or Chassis Ground and have no loops

#3 : VINGND should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

Chroma_F R520 0R Comp_F R521 0R CRIN R522 0R

P500 9-pin:4-pin:9-pin:3-pin CDN_S_VIDEO_9P_STD VIVO:TV_OUT:VIDCAP:STEREO_OUT

RS19 0R Luma_F CVBSYIN R513 0R YRIN R514 0R CompR

GND

CRIN YRIN P501 9-pin:4-pin:9-pin:3-pin CDN_S_VIDEO_9P_STD VIVO:TV_OUT:VIDCAP:STEREO_OUT

GND

R523 0R CompR

AV_IN JACK+RCA-D3-SB-YL CompR

J2A CD-D1x4-BK-SBTJ CRIN CompR YRIN C20 22pF C21 22pF C22 22pF

AV_OUT JACK+RCA-D3-SB-YL Comp_F

ATI Technologies Inc.

33 Commerce Valley Drive East
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(905) 882-260 0

File	Daughter Card RT1 VIVO	
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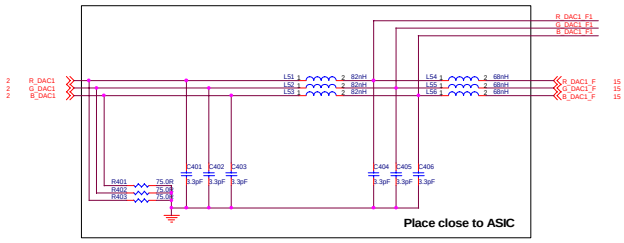
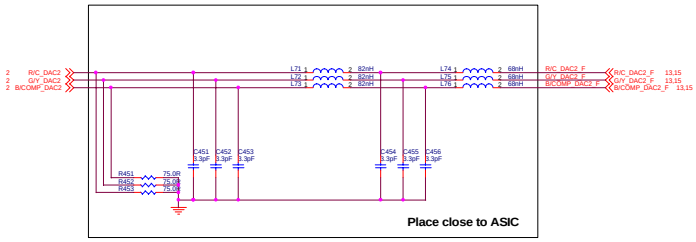
Date: Friday, June 21, 2002	Sheet 13 of 19	

PRIMARY CRT



SECONDARY CRT



<Variant Name>

ATI Technologies Inc.
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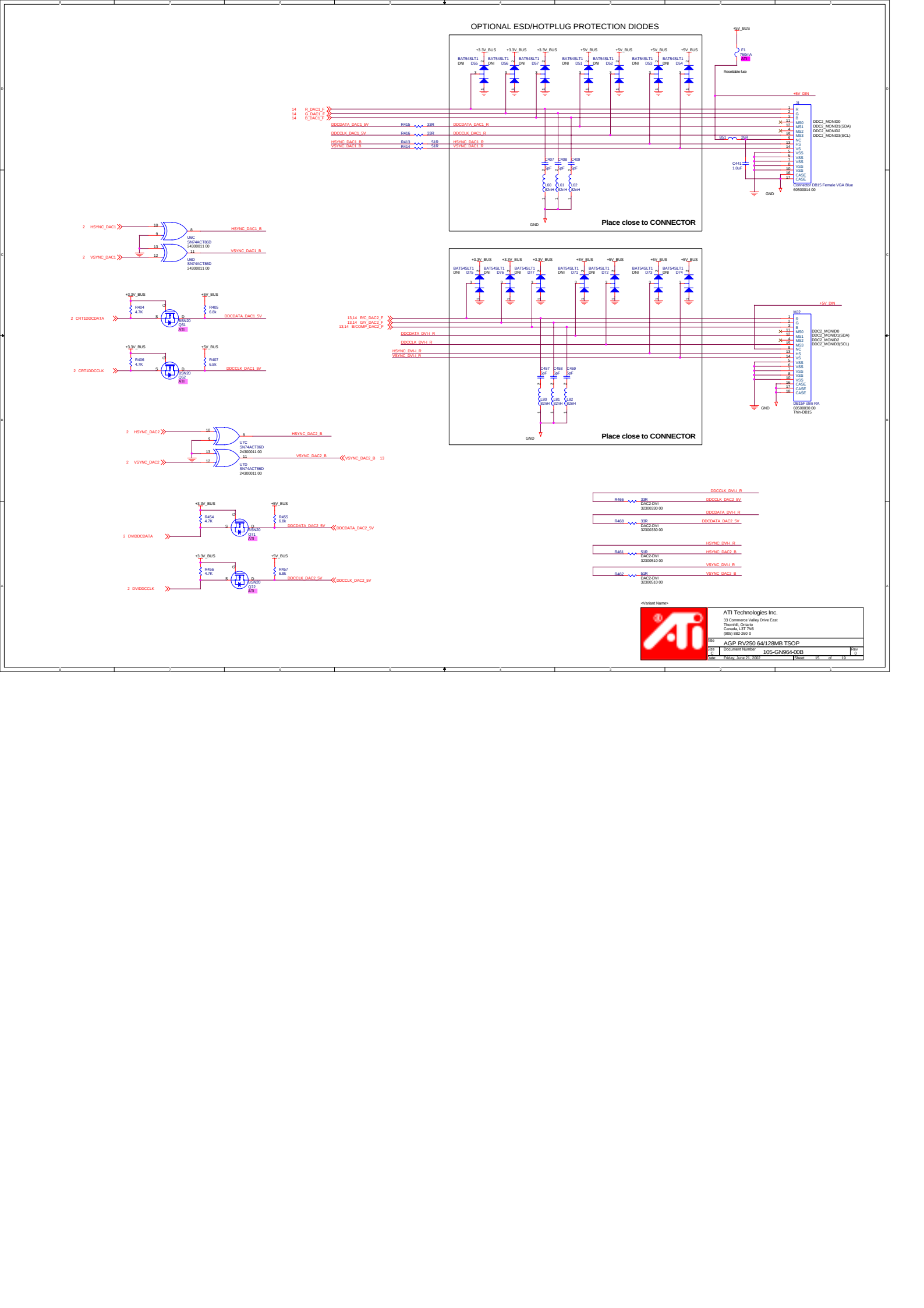
Title	AGP RV250 64/128MB TSOP	
Size: C	Document Number: 105-GN964-00B	Rev: 0
Date: Friday, June 21, 2002	Sheet 14 of 19	


OPTIONAL ESD/HOTPLUG PROTECTION DIODES
+5V_BUS
F1
750mA
ATI
Resettable fuse
+5V_DIN
+3.3V_BUS
BAT54SLT1
DNI
D55
D56
D57
D51
D52
D53
D54
R_DAC1_F
G_DAC1_F
B_DAC1_F
DDCDATA_DAC1_5V
DDCCLK_DAC1_5V
HSYNC_DAC1_B
VSYNC_DAC1_B
R415
R416
R413
R414
33R
51R
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R
C407
C408
C409
5pF
L60
L61
L62
82nH
GND
Place close to CONNECTOR
J1
DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)
BS1
C441
1.0uF
Connector DB15 Female VGA Blue
60500014 00
HSYNC_DAC1
VSYNC_DAC1
U6C
U6D
SN74ACT86D
24300011 00
R404
R405
R406
R407
4.7K
6.8k
CRT1DDCDATA
CRT1DDCCLK
DDCDATA_DAC1_5V
DDCCLK_DAC1_5V
Q51
Q52
RSN20
D55
D56
D57
D51
D52
D53
D54
13,14 R/C_DAC2_F
13,14 G/Y_DAC2_F
13,14 B/COMP_DAC2_F
DDCDATA_DVI-I_R
DDCCLK_DVI-I_R
HSYNC_DVI-I_R
VSYNC_DVI-I_R
C457
C458
C459
L80
L81
L82
J12
DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)
DB15F slim RA
60500030 00
Thin DB15
HSYNC_DAC2
VSYNC_DAC2
U7C
U7D
HSYNC_DAC2_B
VSYNC_DAC2_B
R454
R455
R456
R457
DVIDDCDATA
DVIDDCCLK
DDCDATA_DAC2_5V
DDCCLK_DAC2_5V
Q71
Q72
R466
R468
R461
R462
DDCCLK_DVI-I_R
DDCCLK_DAC2_5V
DDCDATA_DVI-I_R
DDCDATA_DAC2_5V
HSYNC_DVI-I_R
HSYNC_DAC2_B
VSYNC_DVI-I_R
VSYNC_DAC2_B
DAC2-DVI
32300330 00
32300510 00
<Variant Name>
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(905) 882-260 0
Title
AGP RV250 64/128MB TSOP
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0
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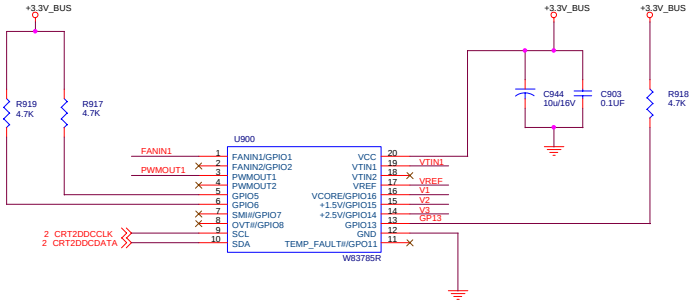
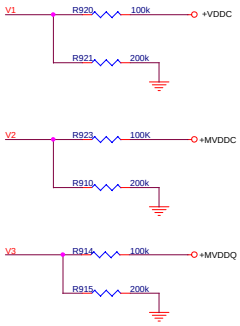
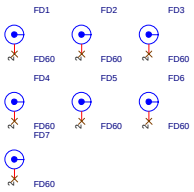
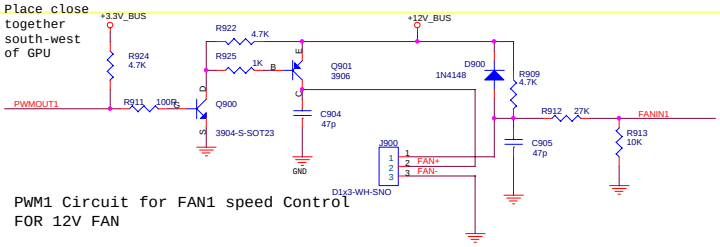
19







Place close together south-west of GPU



PWM1 Circuit for FAN1 speed Control
FOR 12V FAN

VOLTAGE SENSORING CIRCUIT

TEMPERATURE SENSORING CIRCUIT

<Variant Name>

ATI Technologies Inc.
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Title	AGP RV250 64/128MB BGA	
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