NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X

PCI DEVICE ID 0X0=0X200 FOR NV20.

NVVDD SET TO: 1.52V
FBVDD SET TO: 3.47V
FBVDDQ SET TO: 2.59V

HISTORY REVISION:

X00: Based on P50-A06
- See change list in 149- file.
- Set FBVDDQ=2.59V

P50-A07-X01:

- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

P50-A08:

X04: - Delay PLL_VDD to come up after NVVDD.

X05: - Added 1UF accross R257.

X06: - Removed X04-5 above, added a switcher generated PLL delay option.
- SSENA cap for 2nd SW changed to 1UF.
- A05 Si, NVVDD=1.52V

P50-A09:

X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.

X03: - Added option to pull up power good to 12V

ECO1235: - Changed R841 PU to 10K (from 4.7K)

ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction.
Replaced C303,306,309 with 75ohm and no stuffed R208-210.

{Item}\t{Quantity}\t{Reference}\t{Source Package} {USR DFINE} {Value}\t{Assembly}
{Assembly}{Source Package} {Value}{PN}{AVL1}{AVL2}{AVL3}{AVL4}{AVL5}

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MS-8822 based on P50A09

Size	Document Number	Rev
C	TOP PAGE	2.0

Date: Friday, June 08, 2001 Sheet 1 of 16

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Friday, June 08, 2001
Sheet	1 of 1

P300-1
4.7UF

P300-2
4.7UF

HEATSINK
4.7UF

BRACKET
4.7UF

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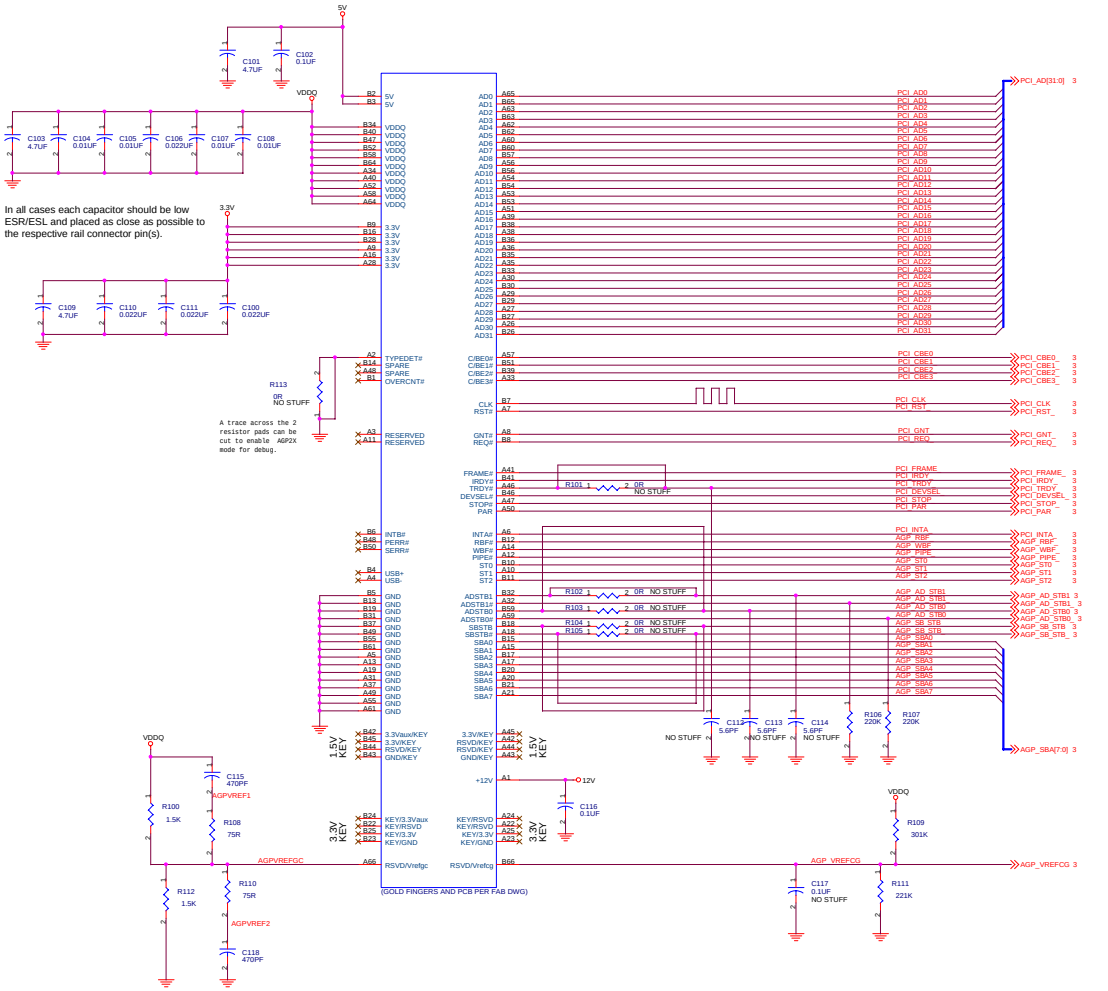
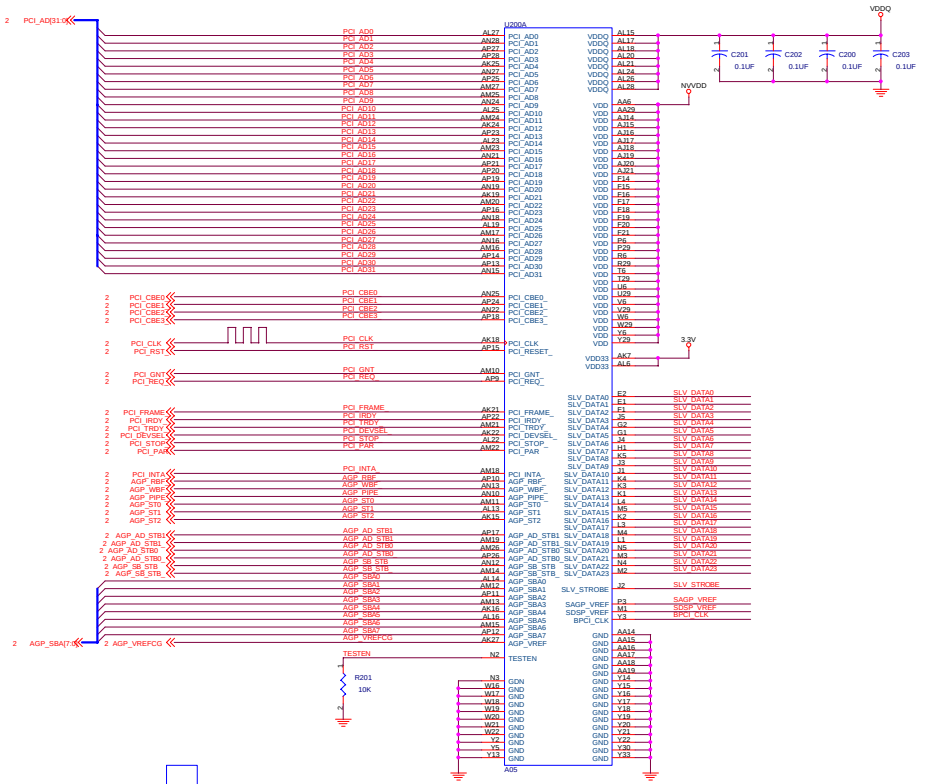
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, June 08, 2001	Sheet 1 of 1	



Micro-Star International Co., LTD.	
MS-8822 based on P50A09	
Size: C	Document Number: BUS I/O
Rev: 2.0	
Date: Friday, June 08, 2001	Sheet 2 of 16



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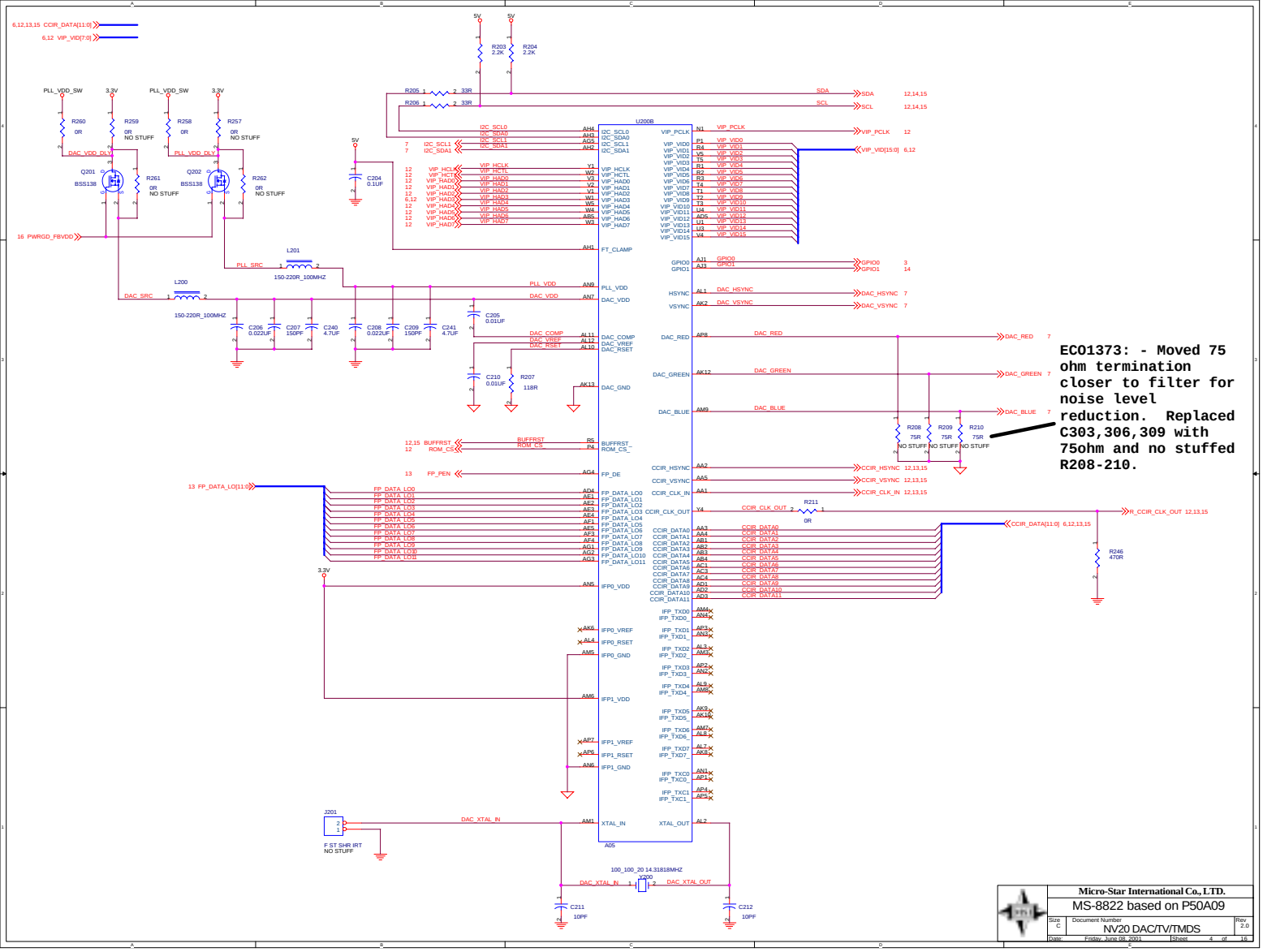
Size: C	Document Number: NV20 HOST
Rev: 2.0	
Date: Friday, June 08, 2001	Sheet 3 of 16



ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction. Replaced C303,306,309 with 75ohm and no stuffed R208-210.

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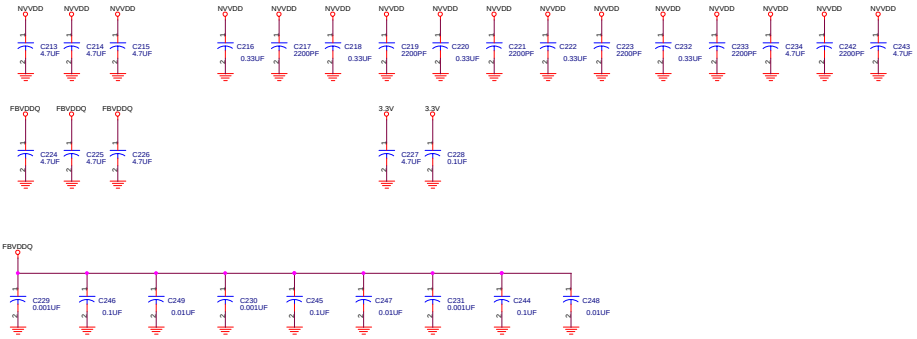
MS-8822 based on P50A09	
Size: C	Document Number: NV20 DAC/TV/TMDS
Rev: 2.0	
Date: Friday, June 08, 2001	Sheet 4 of 16

Use thick (non-impedance controlled) traces on XTALIN/OUT



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MS-8822 based on P50A09			
Size: C	Document Number: NV20 DECOUPLING		Rev: 2.0
Date: Friday, June 08, 2001	Sheet 5 of 16		

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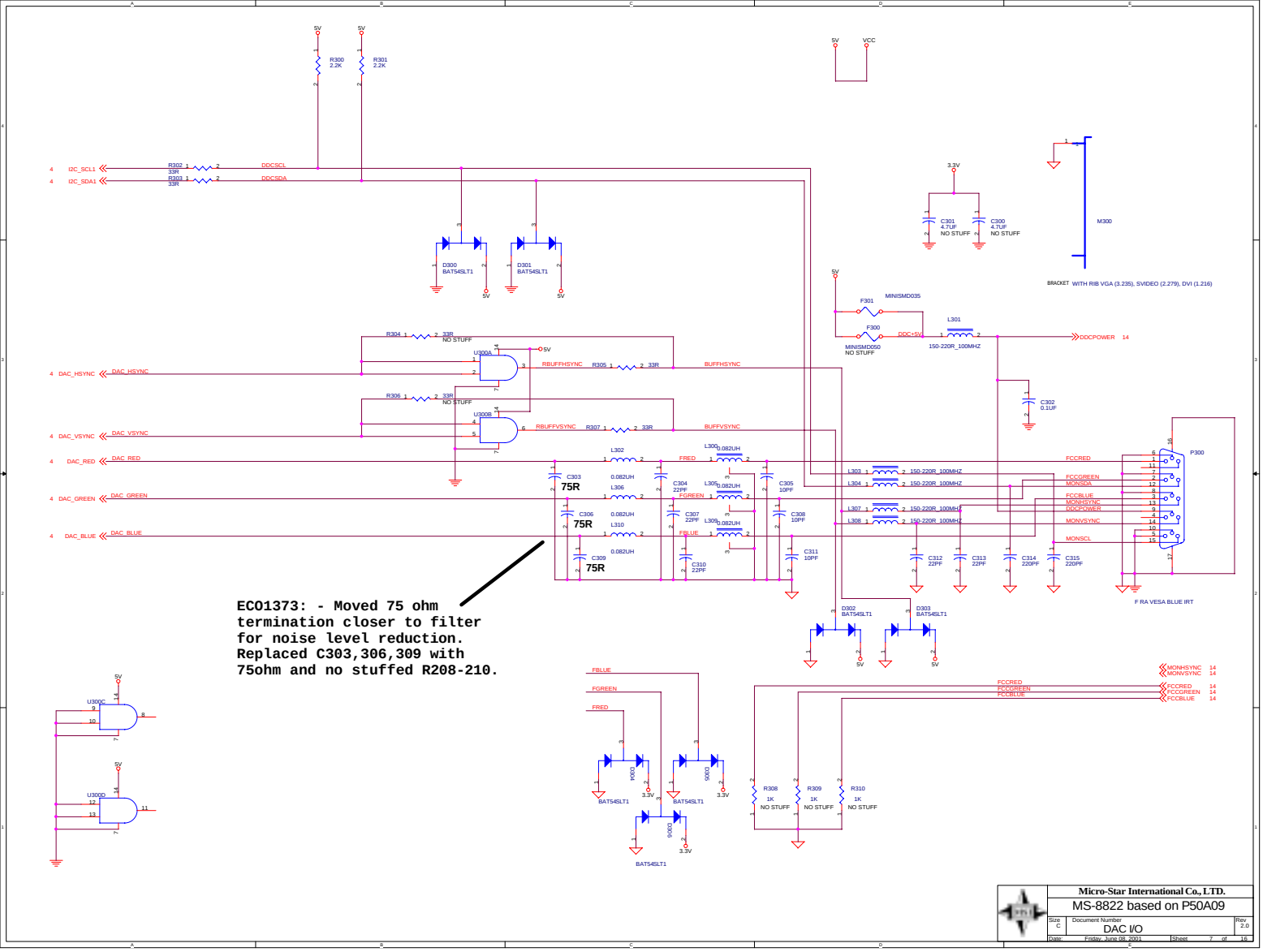
MS-8822 based on P50A09			
Size: C	Document Number: NV20 HOST STRAPS		Rev: 2.0
Date: Friday, June 08, 2001	Sheet 6 of 16		



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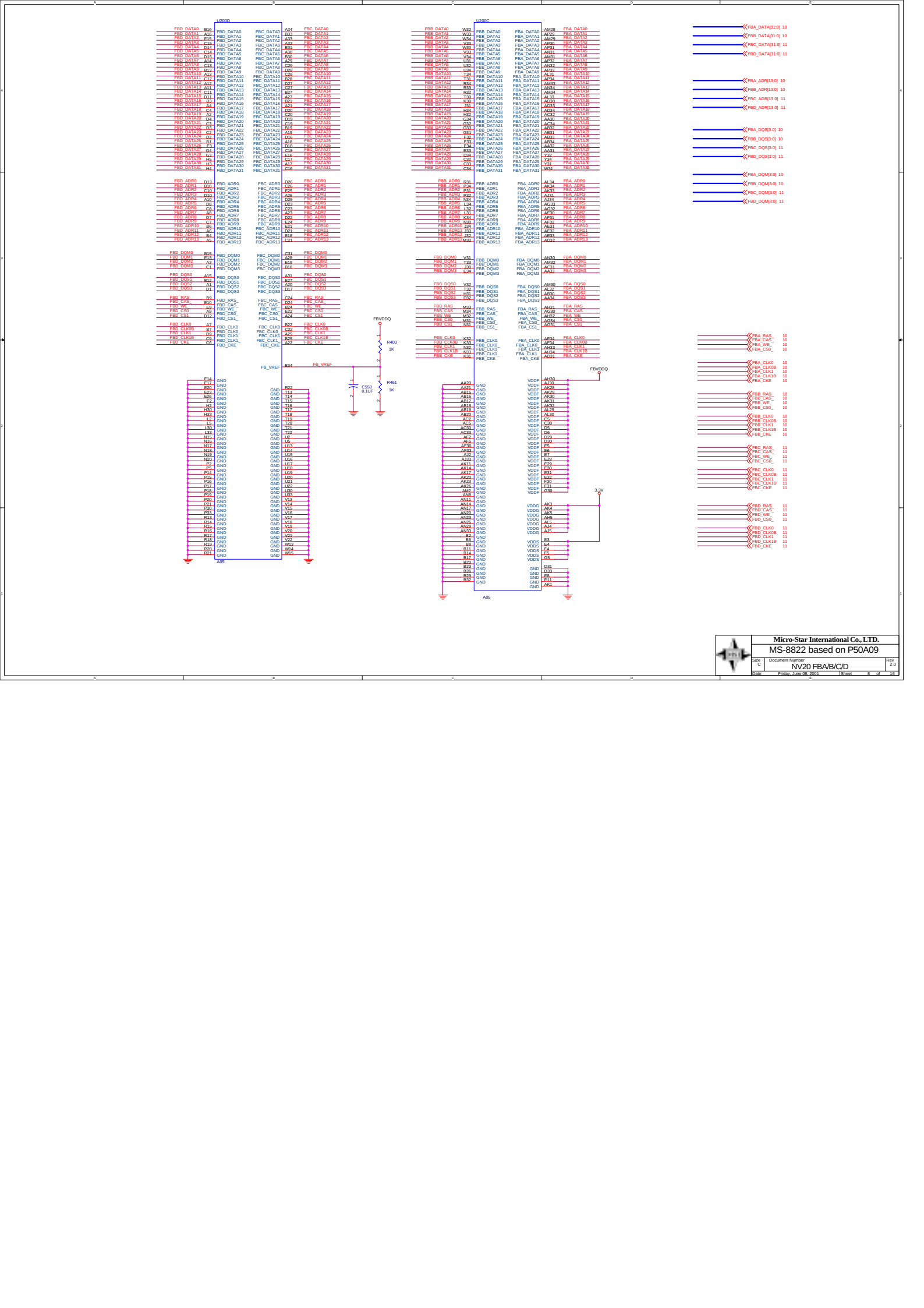
Rev: 2.0	
Date: Friday, June 08, 2001	Sheet 7 of 16



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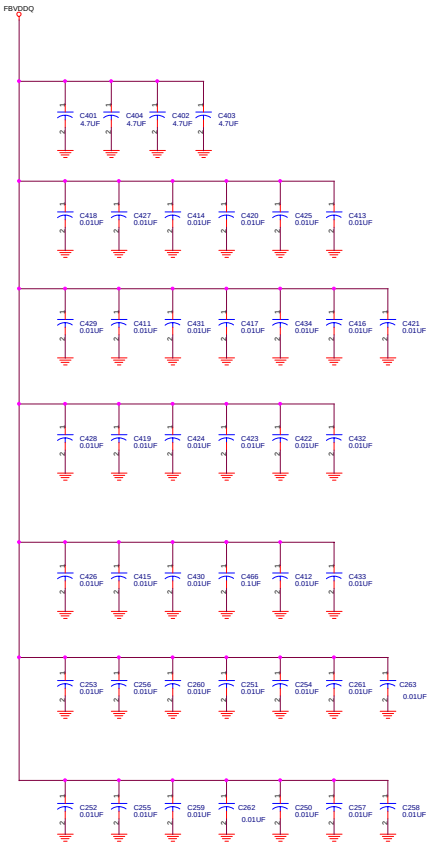
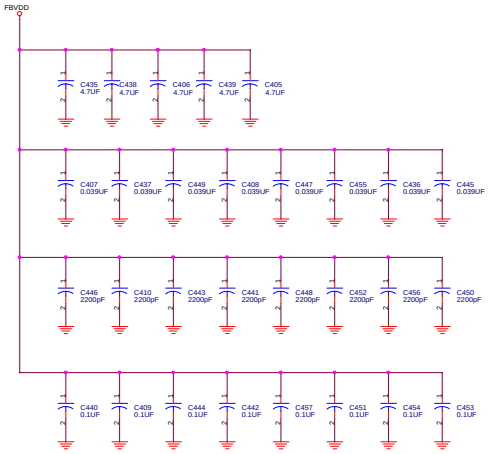
Date: Friday, June 08, 2001	Sheet 8 of 16	





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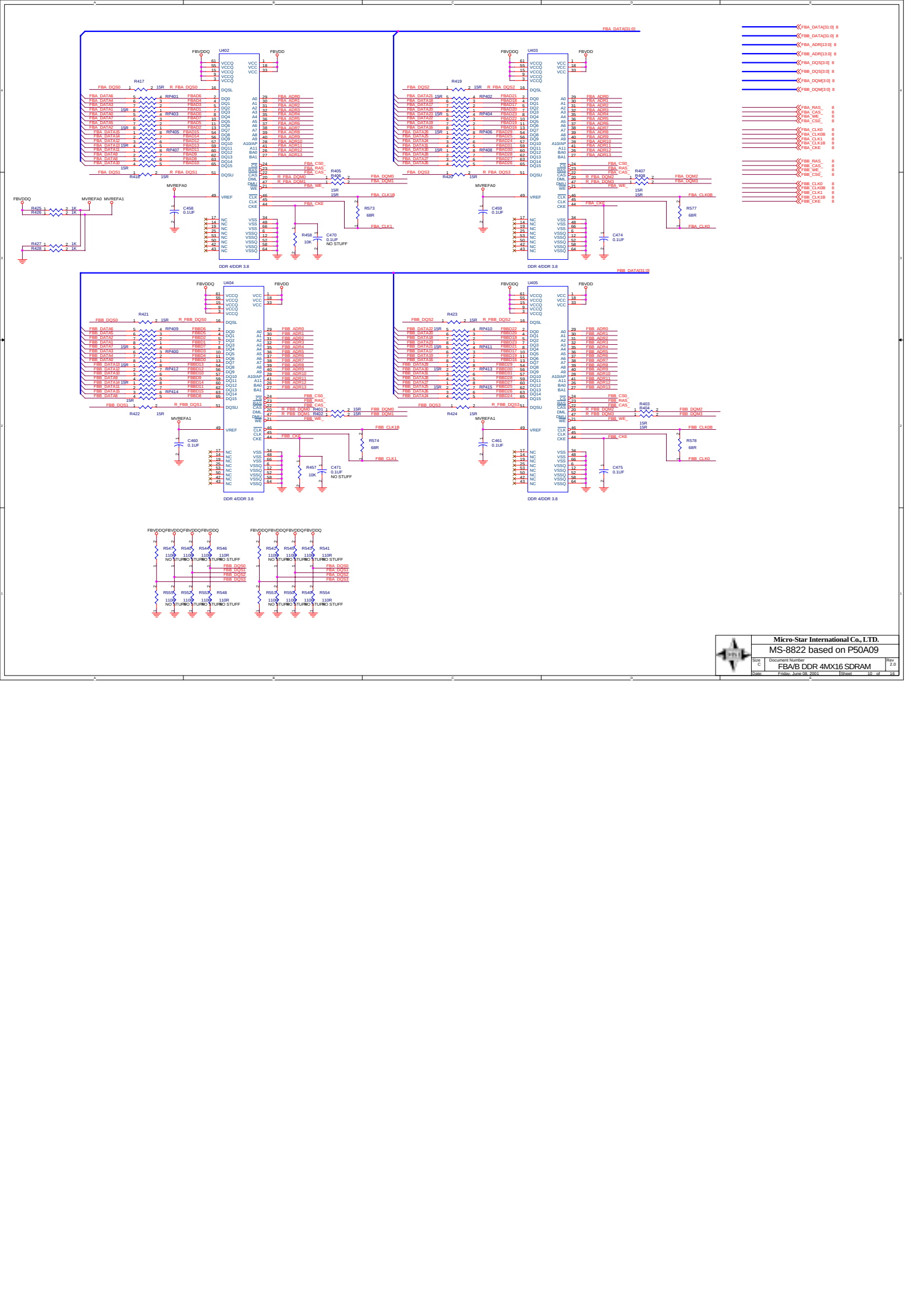
Date: Friday, June 08, 2001	Sheet 9 of 16	


FBA_DATA[31:0] 8
FBB_DATA[31:0] 8
FBA_ADR[13:0] 8
FBB_ADR[13:0] 8
FBA_DQS[3:0] 8
FBB_DQS[3:0] 8
FBA_DQM[3:0] 8
FBB_DQM[3:0] 8
FBA_RAS_ 8
FBA_CAS_ 8
FBA_WE_ 8
FBA_CS0_ 8
FBA_CLK0 8
FBA_CLK0B 8
FBA_CLK1 8
FBA_CLK1B 8
FBA_CKE 8
FBB_RAS_ 8
FBB_CAS_ 8
FBB_WE_ 8
FBB_CS0_ 8
FBB_CLK0 8
FBB_CLK0B 8
FBB_CLK1 8
FBB_CLK1B 8
FBB_CKE 8
U402
U403
U404
U405
DDR 4/DDR 3.8
MVREFA0
MVREFA1
FBVDDQ
FBVDD
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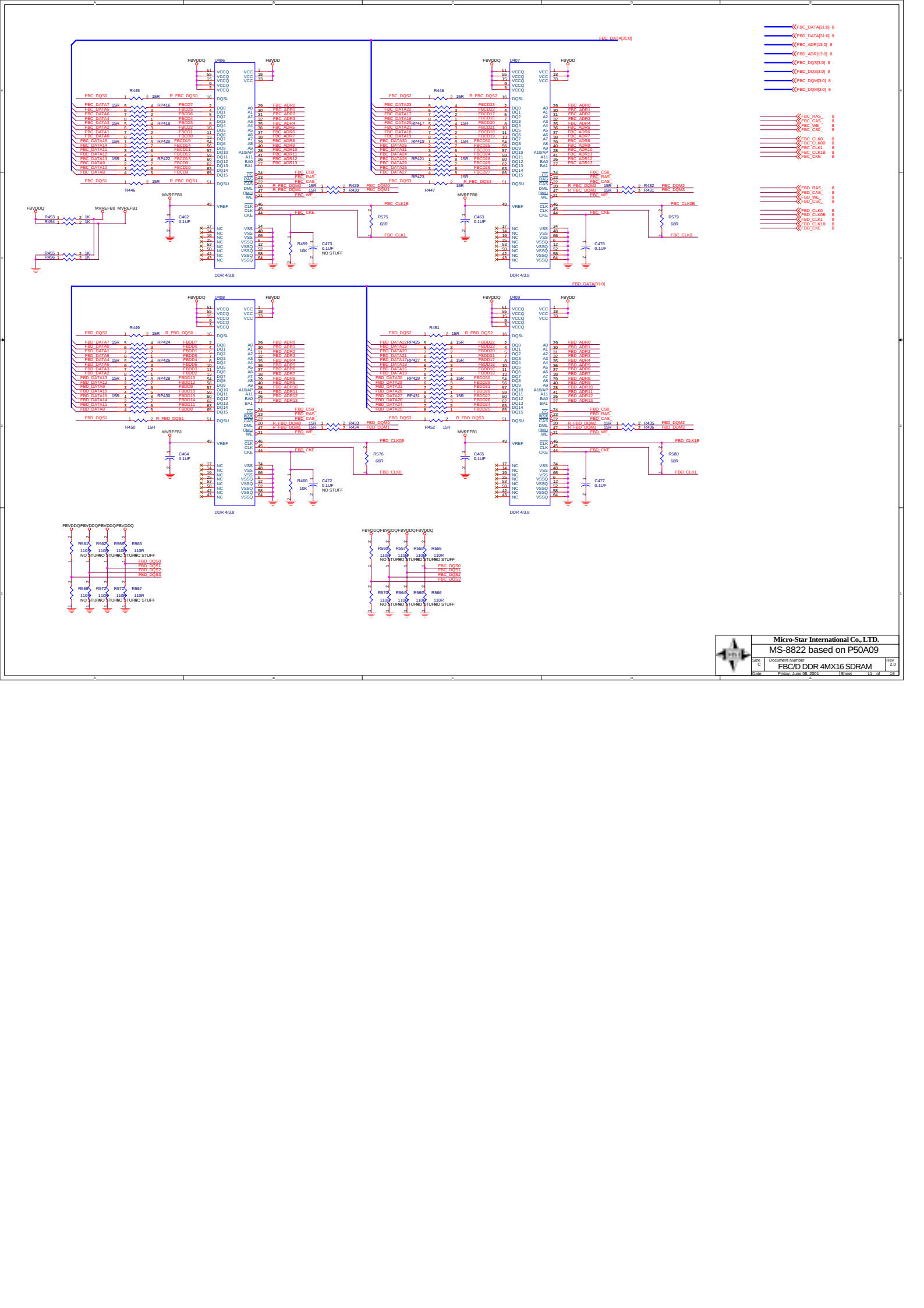
MS-8822 based on P50A09
FBA/B DDR 4MX16 SDRAM
Size C
Document Number
Rev 2.0
Date: Friday, June 08, 2001
Sheet 10 of 16



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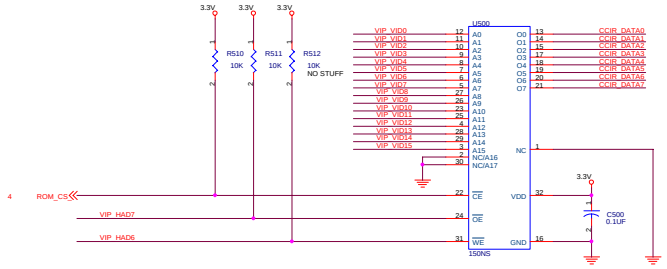
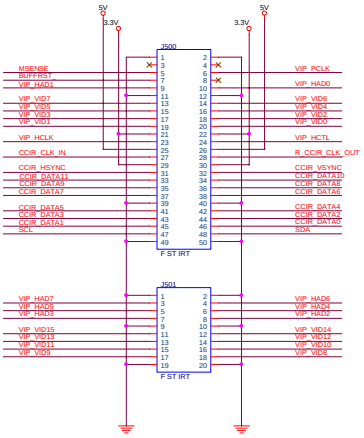
MS-8822 based on P50A09	
Size: C	Document Number: FBC/D DDR 4MX16 SDRAM
Rev: 2.0	
Date: Friday, June 08, 2001	Sheet: 11 of 16

4,6 VIP_VID[15:0]
4 VIP_PCLK
4 VIP_HCLK
4 VIP_HCTL
4 VIP_HAD0
4 VIP_HAD1
4 VIP_HAD2
4,6 VIP_HAD3
4 VIP_HAD4
4 VIP_HAD5
4 VIP_HAD6
4 VIP_HAD7
4,6,13,15 CCIR_DATA[11:0]
4,13,15 CCIR_HSYNC
4,13,15 CCIR_VSYNC
4,13,15 CCIR_CLK_IN
4,13,15 R_CCIR_CLK_OUT
4,15 BUFFRST_
4,14,15 SCL
4,14,15 SDA





Micro-Star International Co., LTD.			
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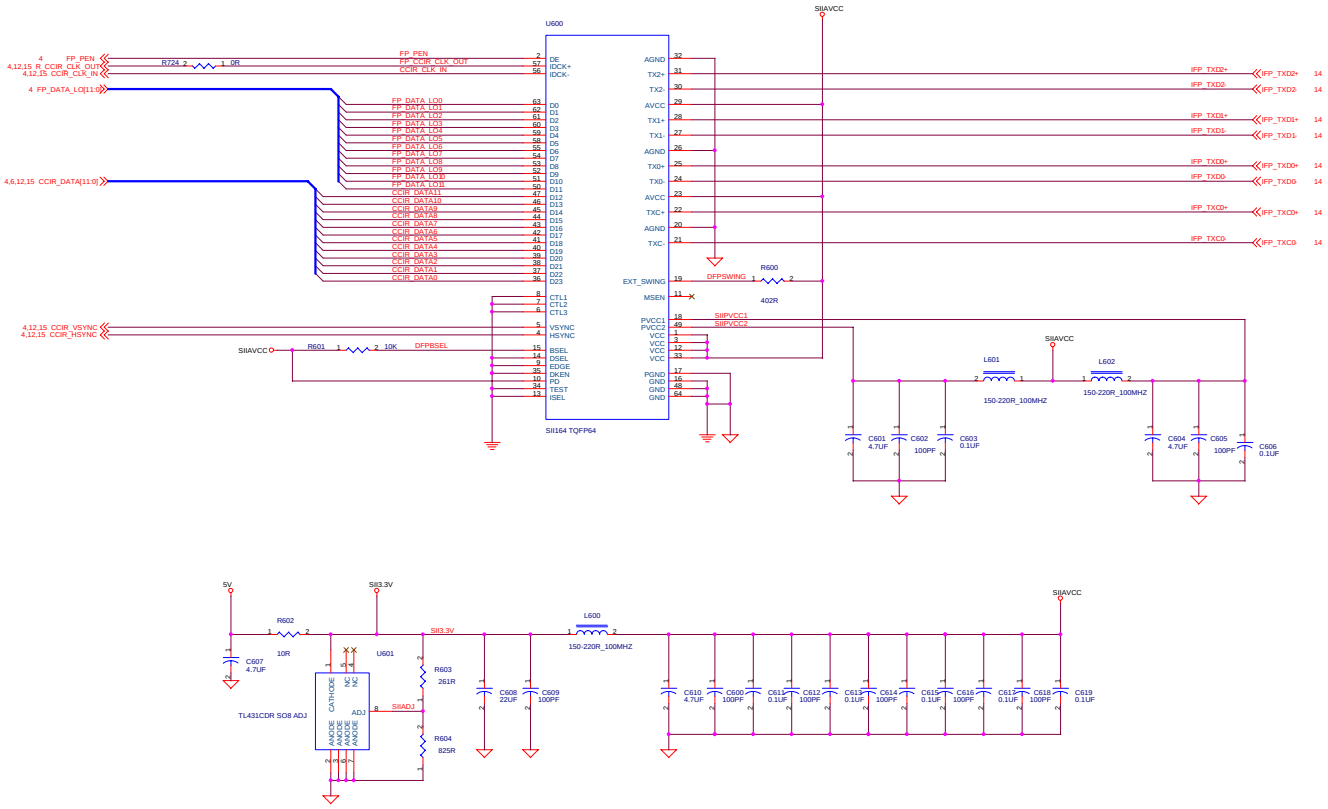
Size C	Document Number ROM VIP & VIDEO IF		Rev 2.0
Date: Friday, June 08, 2001		Sheet 12 of 16	



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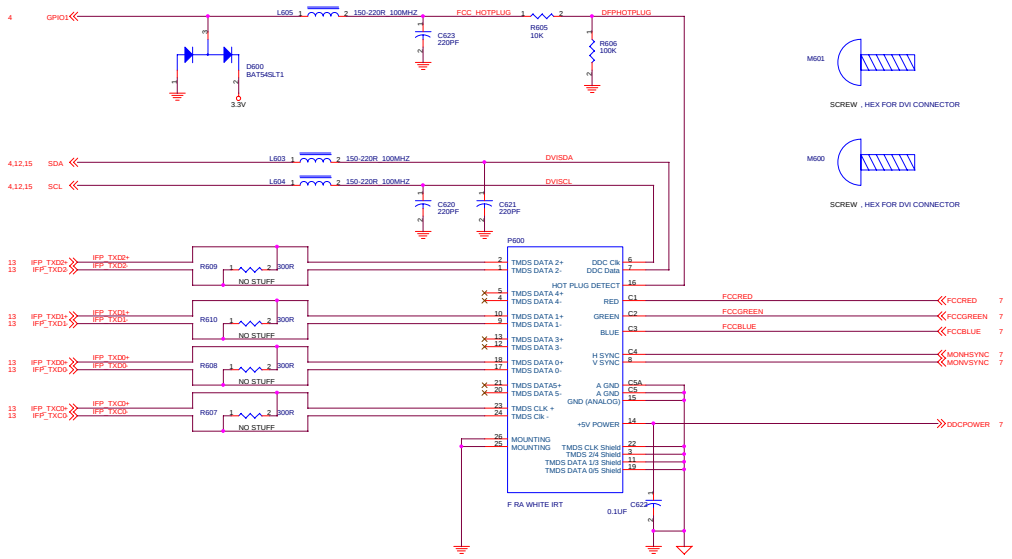
MS-8822 based on P50A09		
Size: C	Document Number: EXTERNAL DFP/DVI	Rev: 2.0
Date: Friday, June 08, 2001	Sheet: 13 of 16	



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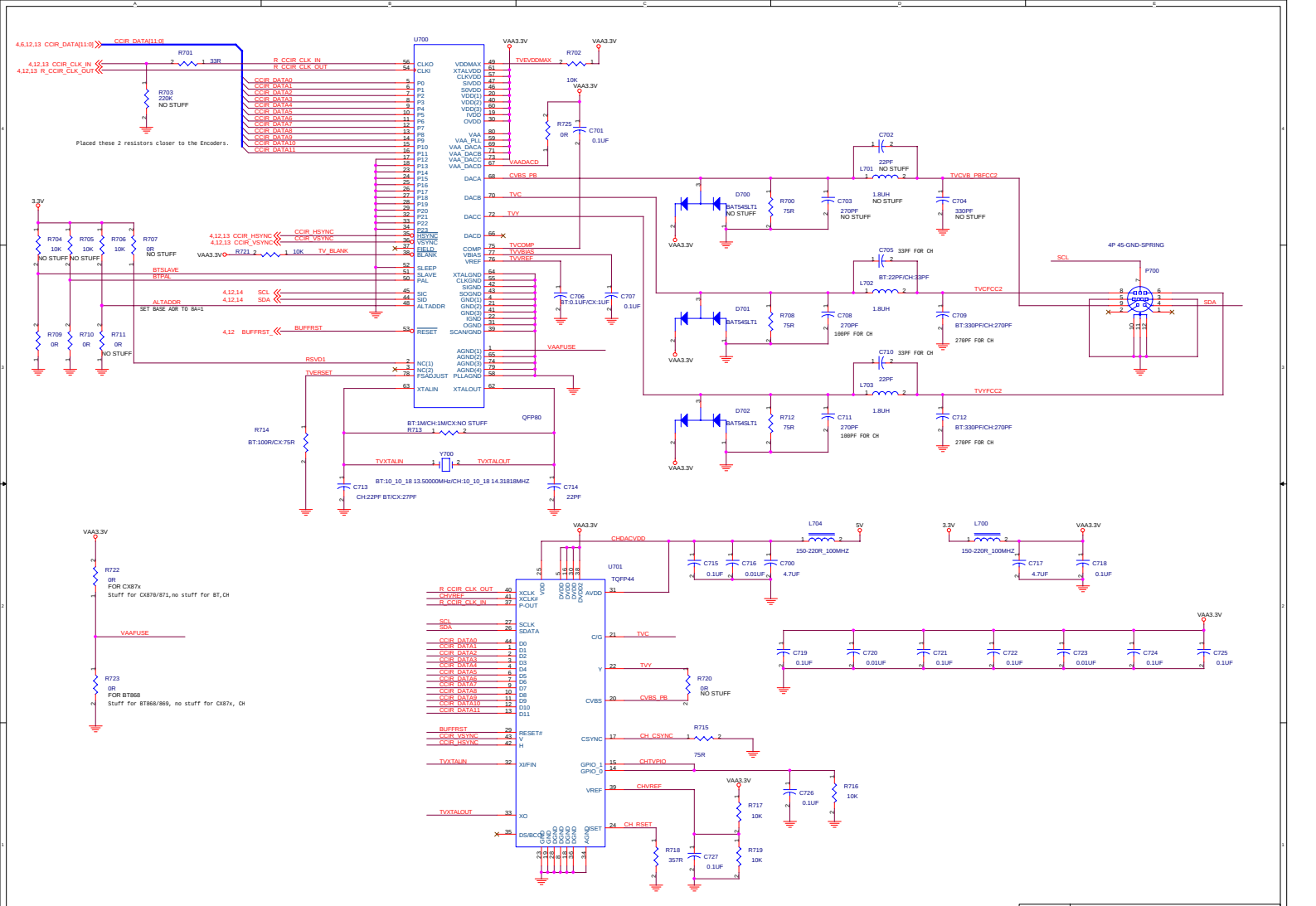
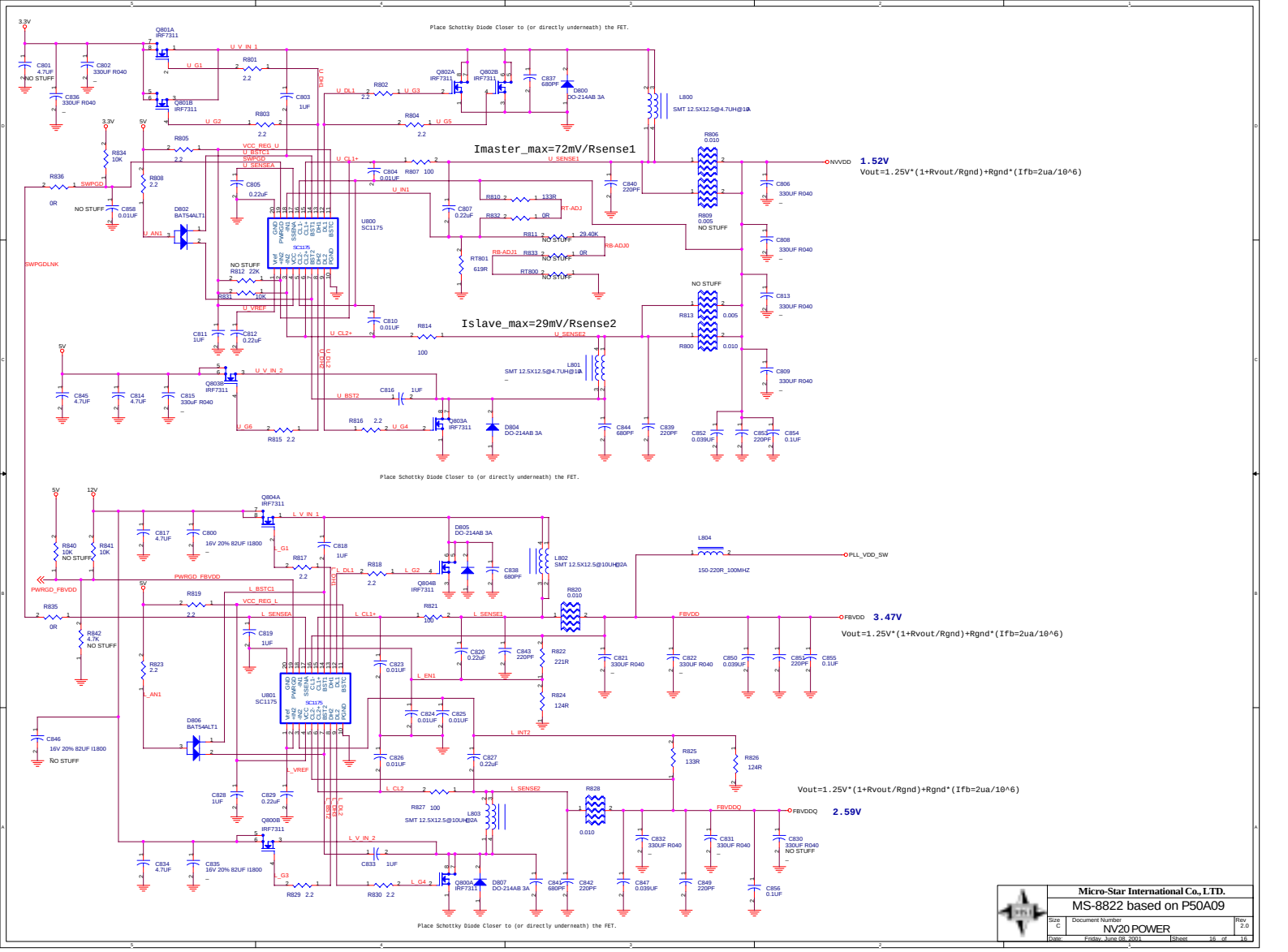
Size: C	Document Number: DVI-I I/O		Rev: 2.0
Date: Friday, June 08, 2001	Sheet 14 of 16		



Parts for Chrontel CH7007/8



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MS-8822 based on P50A09	
Size: C	Document Number: NV20 POWER
Rev: 2.0	
Date: Friday, June 08, 2001	Sheet 16 of 16