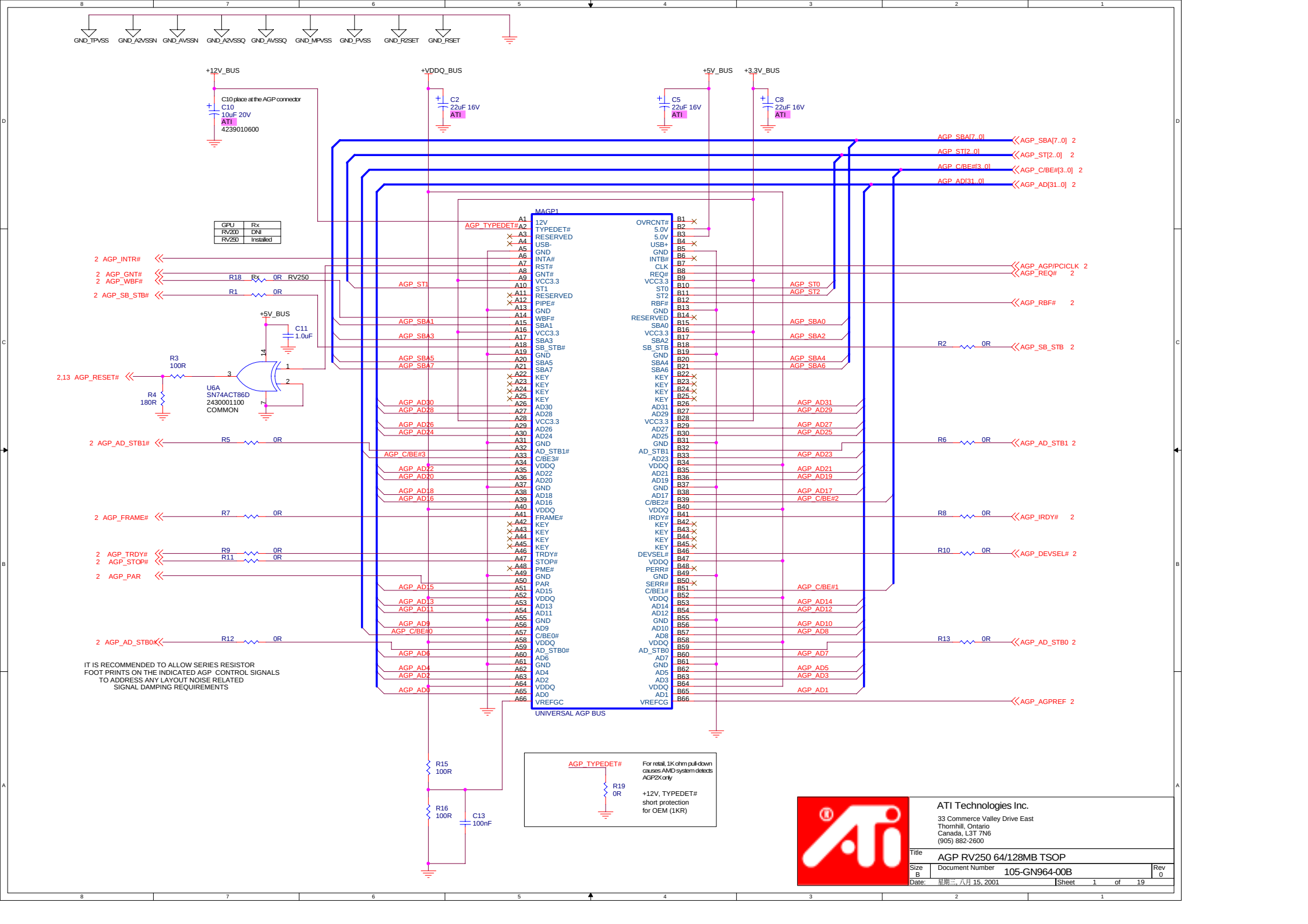
GND_TPVSS
GND_A2VSSN
GND_AVSSN
GND_A2VSSQ
GND_AVSSQ
GND_MPVSS
GND_PVSS
GND_R2SET
GND_RSET
+12V_BUS
C10 place at the AGP connector
C10
10uF 20V
ATI
4239010600
+VDDQ_BUS
C2
22uF 16V
ATI
+5V_BUS
C5
22uF 16V
ATI
+3.3V_BUS
C8
22uF 16V
ATI
GPU | Rx
RV200 | DNI
RV250 | Installed
MAGP1
12V
TYPEDET#
RESERVED
USB-
GND
INTA#
RST#
GNT#
VCC3.3
ST1
RESERVED
PIPE#
GND
WBF#
SBA1
VCC3.3
SBA3
SB_STB#
GND
SBA5
SBA7
KEY
KEY
KEY
KEY
KEY
AD30
AD28
VCC3.3
AD26
AD24
GND
AD_STB1#
C/BE3#
VDDQ
AD22
AD20
GND
AD18
AD16
VDDQ
FRAME#
KEY
KEY
KEY
KEY
KEY
TRDY#
STOP#
PME#
GND
PAR
AD15
VDDQ
AD13
AD11
GND
AD9
C/BE0#
VDDQ
AD_STB0#
AD6
GND
AD4
AD2
VDDQ
AD0
VREFGC
OVRCNT#
5.0V
5.0V
USB+
GND
INTB#
CLK
REQ#
VCC3.3
ST0
ST2
RBF#
GND
RESERVED
SBA0
VCC3.3
SBA2
SB_STB
GND
SBA4
SBA6
KEY
KEY
KEY
KEY
KEY
AD31
AD29
VCC3.3
AD27
AD25
GND
AD_STB1
AD23
VDDQ
AD21
AD19
GND
AD17
C/BE2#
VDDQ
IRDY#
KEY
KEY
KEY
KEY
KEY
DEVSEL#
VDDQ
PERR#
GND
SERR#
C/BE1#
VDDQ
AD14
AD12
GND
AD10
AD8
VDDQ
AD_STB0
AD7
GND
AD5
AD3
VDDQ
AD1
VREFCG
UNIVERSAL AGP BUS
AGP_SBA[7..0]
AGP_ST[2..0]
AGP_C/BE#[3..0]
AGP_AD[31..0]
AGP_SBA[7..0] 2
AGP_ST[2..0] 2
AGP_C/BE#[3..0] 2
AGP_AD[31..0] 2
AGP_AGP/PCICLK 2
AGP_REQ# 2
AGP_RBF# 2
AGP_SB_STB 2
AGP_AD_STB1 2
AGP_IRDY# 2
AGP_DEVSEL# 2
AGP_AD_STB0 2
AGP_AGPREF 2
2 AGP_INTR#
2 AGP_GNT#
2 AGP_WBF#
2 AGP_SB_STB#
2,13 AGP_RESET#
2 AGP_AD_STB1#
2 AGP_FRAME#
2 AGP_TRDY#
2 AGP_STOP#
2 AGP_PAR
2 AGP_AD_STB0#
R18 Rx 0R RV250
R1 0R
R2 0R
R3 100R
R4 180R
R5 0R
R6 0R
R7 0R
R8 0R
R9 0R
R10 0R
R11 0R
R12 0R
R13 0R
C11 1.0uF
U6A
SN74ACT86D
2430001100
COMMON
IT IS RECOMMENDED TO ALLOW SERIES RESISTOR
FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS
TO ADDRESS ANY LAYOUT NOISE RELATED
SIGNAL DAMPING REQUIREMENTS
R15 100R
R16 100R
C13 100nF
AGP_TYPEDET#
R19 0R
For retail, 1K ohm pull-down causes AMD system detects AGP2X only
+12V, TYPEDET# short protection for OEM (1KR)
ATI Technologies Inc.
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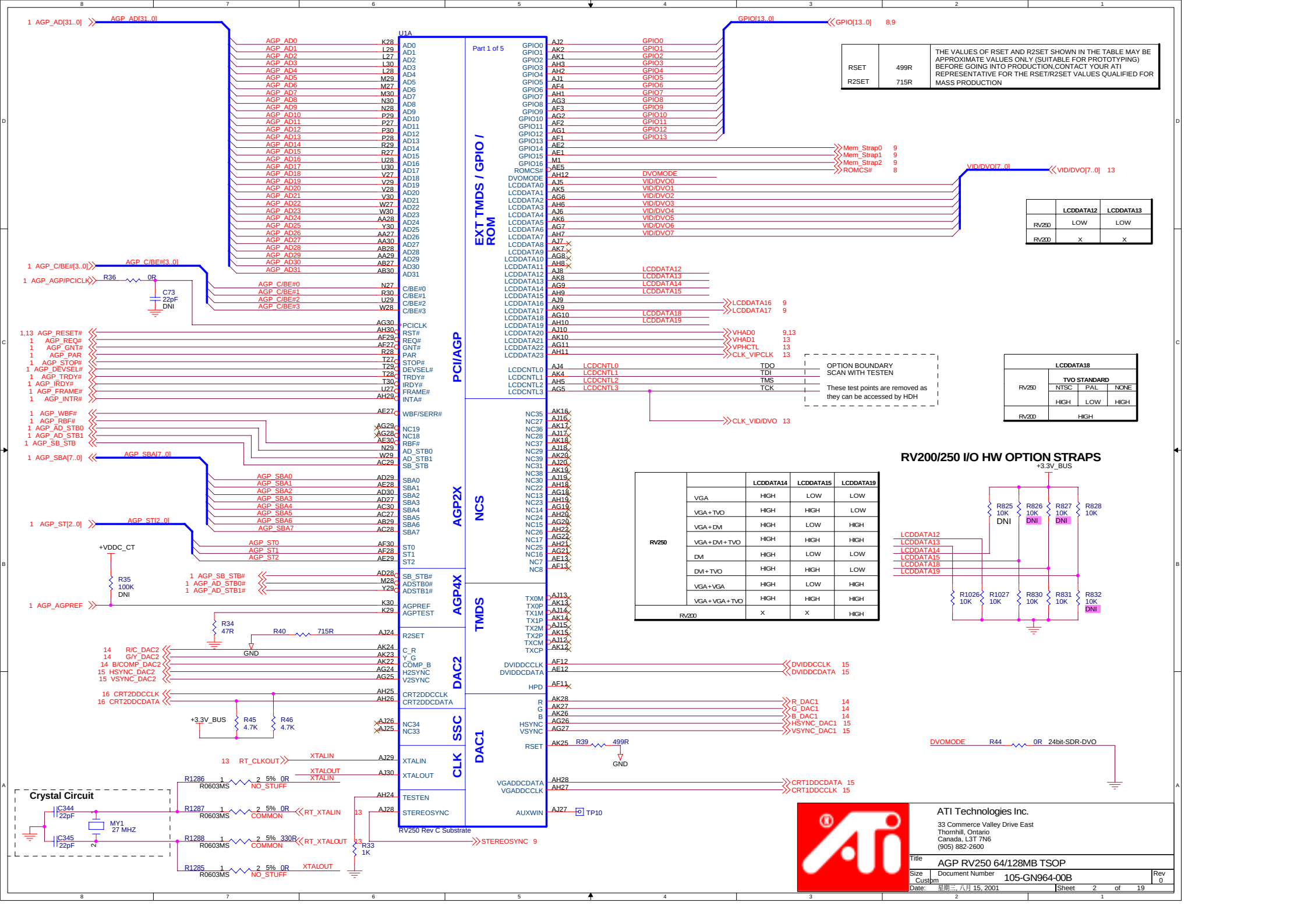
Thornhill, Ontario
Canada, L3T 7N6
(905) 882-2600
Title
AGP RV250 64/128MB TSOP
Size B
Document Number 105-GN964-00B
Rev 0
Date: 星期三, 八月 15, 2001
Sheet 1 of 19


U1A
Part 1 of 5
PCI/AGP
AGP2X
NCS
AGP4X
TMDS
DAC2
SSC
CLK
DAC1
EXT TMDS / GPIO / ROM
RV250 Rev C Substrate
AGP_AD[31..0]
AGP_C/BE#[3..0]
AGP_SBA[7..0]
AGP_ST[2..0]
GPIO[13..0]
VID/DVO[7..0]
RSET 499R
R2SET 715R
THE VALUES OF RSET AND R2SET SHOWN IN THE TABLE MAY BE APPROXIMATE VALUES ONLY (SUITABLE FOR PROTOTYPING) BEFORE GOING INTO PRODUCTION,CONTACT YOUR ATI REPRESENTATIVE FOR THE RSET/R2SET VALUES QUALIFIED FOR MASS PRODUCTION
OPTION BOUNDARY SCAN WITH TESTEN
These test points are removed as they can be accessed by HDH
RV200/250 I/O HW OPTION STRAPS
+3.3V_BUS
Crystal Circuit
MY1 27 MHZ
ATI Technologies Inc.
33 Commerce Valley Drive East
Thornhill, Ontario
Canada, L3T 7N6
(905) 882-2600
Title AGP RV250 64/128MB TSOP
Size Custom
Document Number 105-GN964-00B
Rev 0
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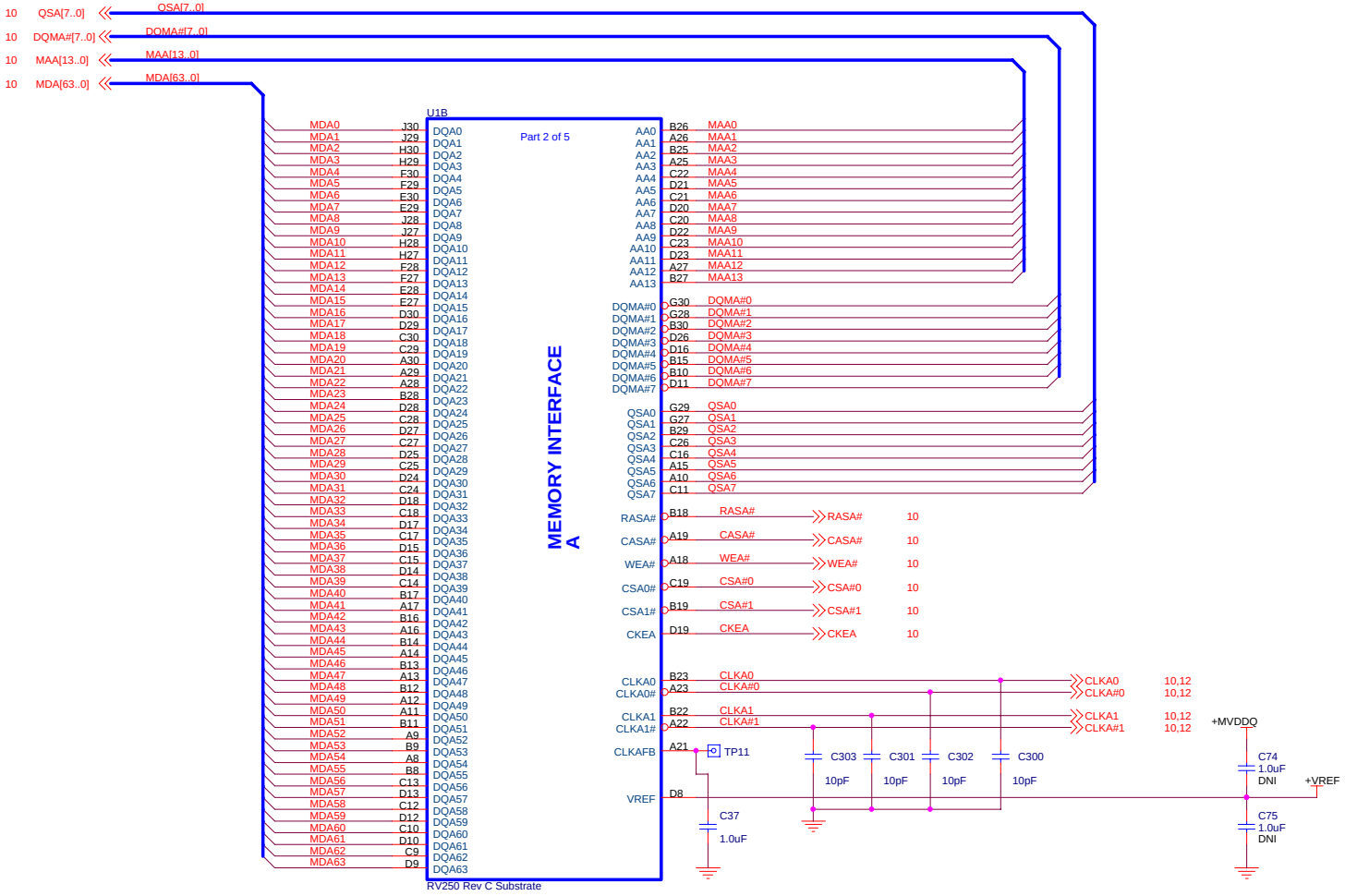
Sheet 2 of 19

MEMORY CHANNEL A



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Title	AGP RV250 64/128MB TSOP	
Size: Custom	Document Number: 105-GN964-00B	Rev: 0
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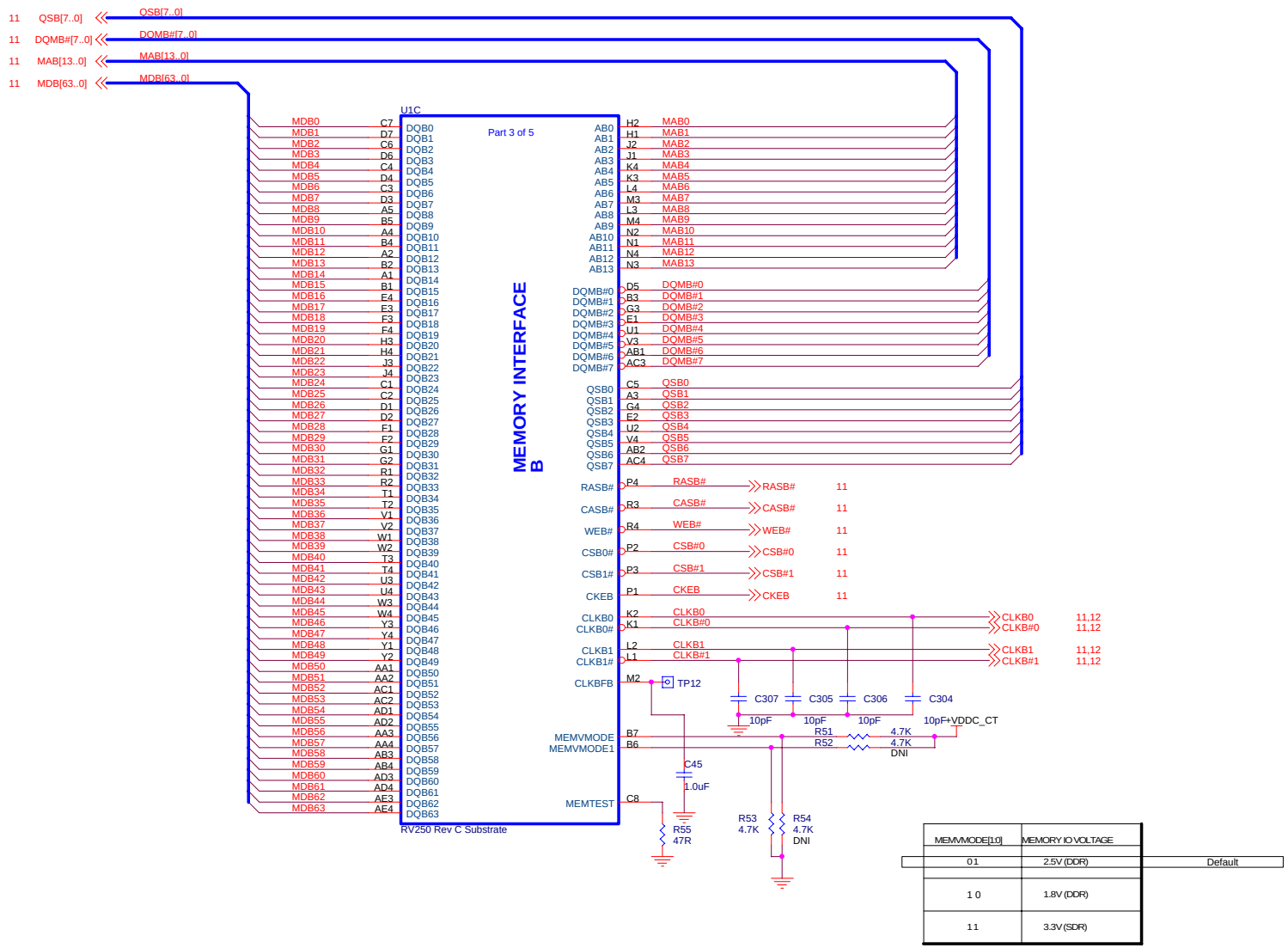
MEMORY CHANNEL B



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Title	AGP RV250 64/128MB TSOP	
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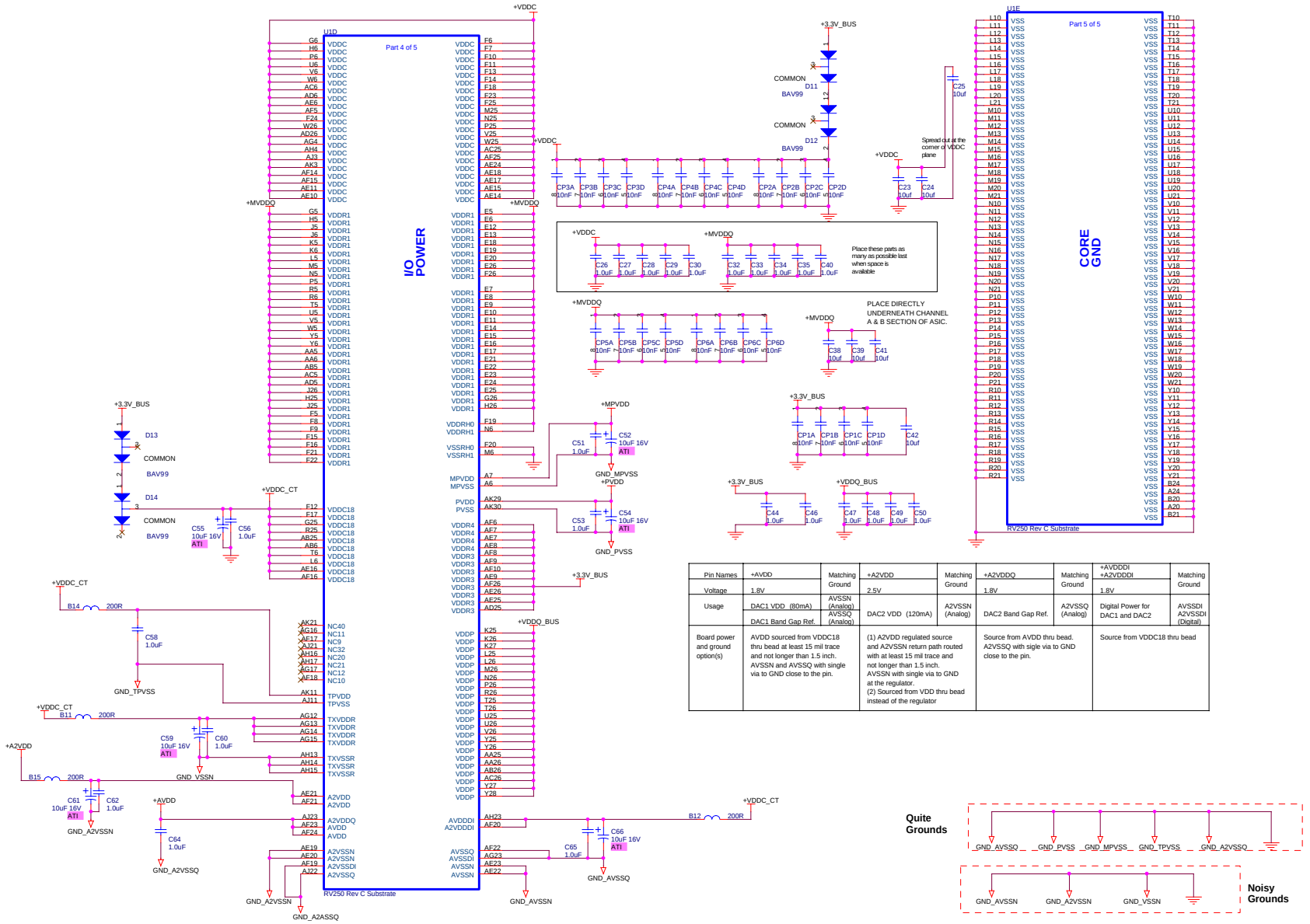

Pin Names	+AVDD	Matching Ground	+A2VDD	Matching Ground	+A2VDDQ	Matching Ground	+AVDDDI +A2VDDDI	Matching Ground
Voltage	1.8V		2.5V		1.8V		1.8V	
Usage	DAC1 VDD (80mA)	AVSSN (Analog)	DAC2 VDD (120mA)	A2VSSN (Analog)	DAC2 Band Gap Ref.	A2VSSQ (Analog)	Digital Power for DAC1 and DAC2	AVSSDI A2VSSDI (Digital)
	DAC1 Band Gap Ref.	AVSSQ (Analog)						
Board power and ground option(s)	AVDD sourced from VDDC18 thru bead at least 15 mil trace and not longer than 1.5 inch. AVSSN and AVSSQ with single via to GND close to the pin.		(1) A2VDD regulated source and A2VSSN return path routed with at least 15 mil trace and not longer than 1.5 inch. AVSSN with single via to GND at the regulator. (2) Sourced from VDD thru bead instead of the regulator		Source from AVDD thru bead. A2VSSQ with sigle via to GND close to the pin.		Source from VDDC18 thru bead	

Quite Grounds

GND_AVSSQ GND_PVSS GND_MPVSS GND_TPVSS GND_A2VSSQ

GND_AVSSN GND_A2VSSN GND_VSSN

Noisy Grounds

The following grounds should be routed back to their respective regulators and then tied directly to the ground plane with one via: GND_PVSS, GND_MPVSS, GND_TPVSS, and GND_A2VSSN. The other ground pins (GND_AVSSN, GND_A2VSSQ, GND_RSET, GND_R2SET) should be tied to the ground plane directly through one via as close to the pins as possible without connecting to anything else. If space is an issue it is possible to use one via for two adjacent pins.

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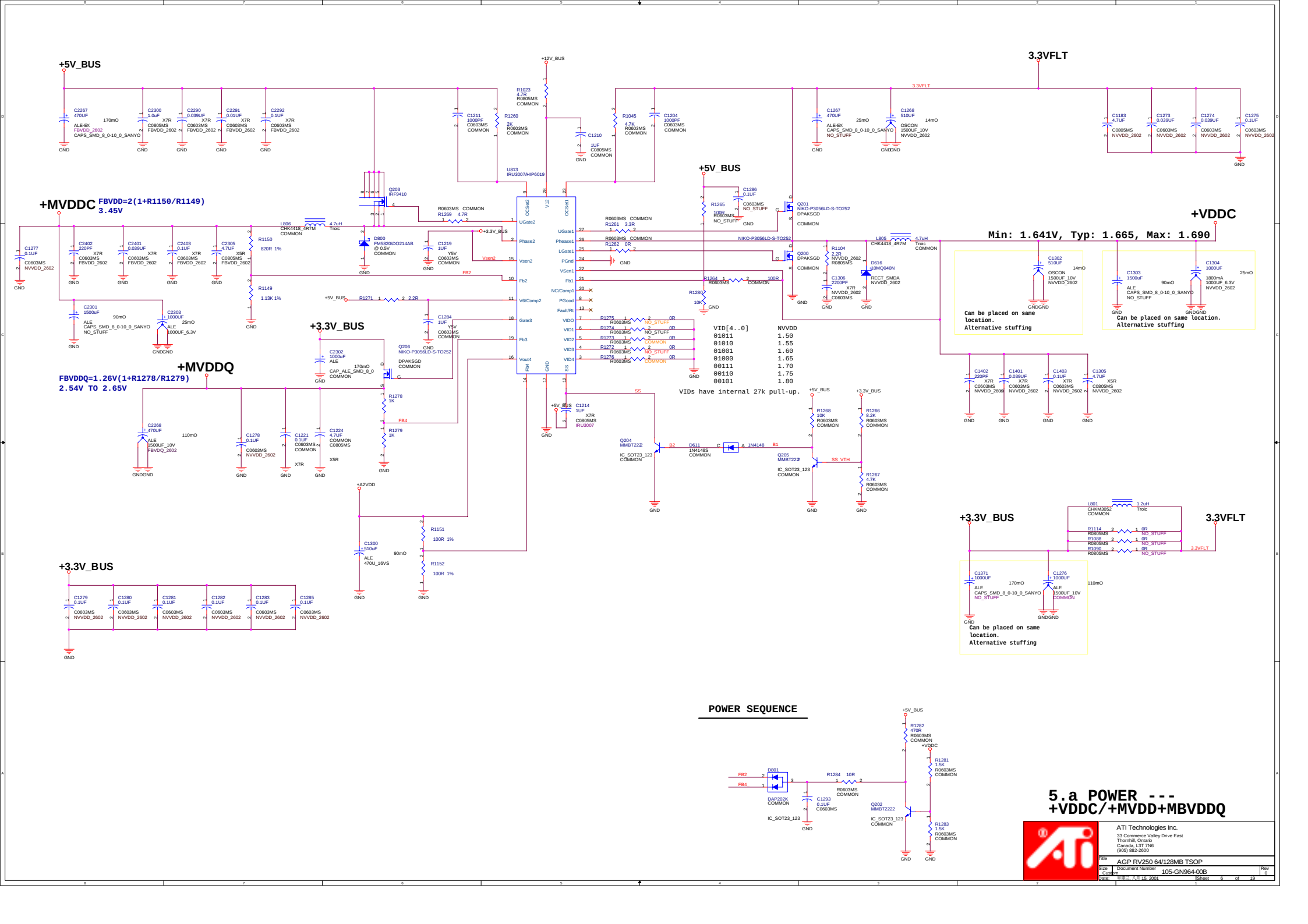
+5V_BUS
+12V_BUS
3.3VFLT
+MVDDC
FBVDD=2(1+R1150/R1149)
3.45V
+MVDDQ
FBVDDQ=1.26V(1+R1278/R1279)
2.54V TO 2.65V
+3.3V_BUS
+A2VDD
+VDDC
Min: 1.641V, Typ: 1.665, Max: 1.690
Can be placed on same location.
Alternative stuffing
U813
IRU3007/HIP6019
VID[4..0] NVVDD
01011 1.50
01010 1.55
01001 1.60
01000 1.65
00111 1.70
00110 1.75
00101 1.80
VIDs have internal 27k pull-up.
POWER SEQUENCE
5.a POWER --- +VDDC/+MVDD+MBVDDQ
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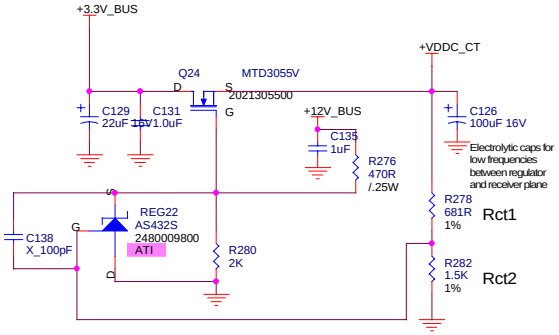
AGP RV250 64/128MB TSOP
105-GN964-00B

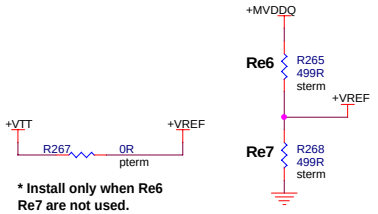
Regulator for VDDC_CT (Core Transform) and AVDD/A2VDDQ/AVDDDI/A2VDDDI TXVDDR, LVDDRx

Vin = 3.3V AGP
Vout = 1.8V
Iout = 350mA + 100mA + 50mA = 500mA MAX
Iout = 600mA MAX (with PVDD/TPVDD)

	Rct1		Rct2	
1.8V	681R	3240681000	1.5K	3230015200
1.9V	536R	3240536000	1K	3240100100



Vref Voltage



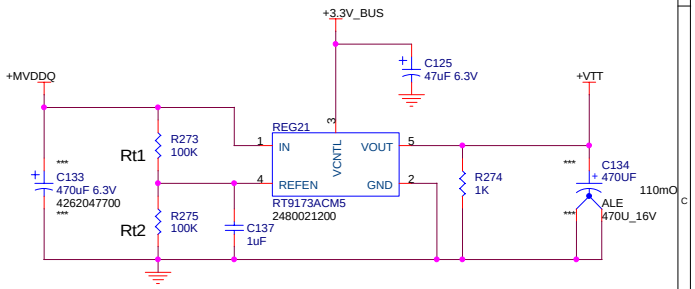
*** Install only when Re6 Re7 are not used.**

Use localized Vref on the memory page

Regulator for VTT (Termination)

Vin = MVDDQ
Vout = 1.25V
Iout = 2000mA MAX
Iout = 750mA Est. MAX

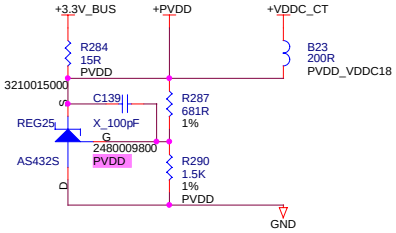
	Rt1		Rt2	
1.25V	1K	3240100100	1K	3240100100
1.3V	1.0K	3240100100	1.02K	3240102100



Regulator for PVDD (R200 PLLs) and optional TPVDD (TMDS PLLs)

Vin = 3.3V AGP
Vout = +1.8V
Iout = 25mA MAX (PVDD only)
Iout = 100mA MAX (PVDD + TPVDD)

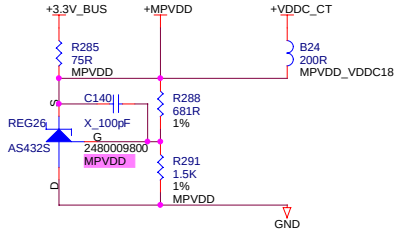
(Optional)



If PVDD and TPVDD are used from the same regulator, Rr must be change to 15R P/N3210015000 to provide enough current.

Regulator for MPVDD (Memory PLLs)

Vin = 3.3V AGP
Vout = +1.8V
Iout = 10mA MAX



AVDD/A2VDDQ (1st DAC & 2nd DAC Band Gap)

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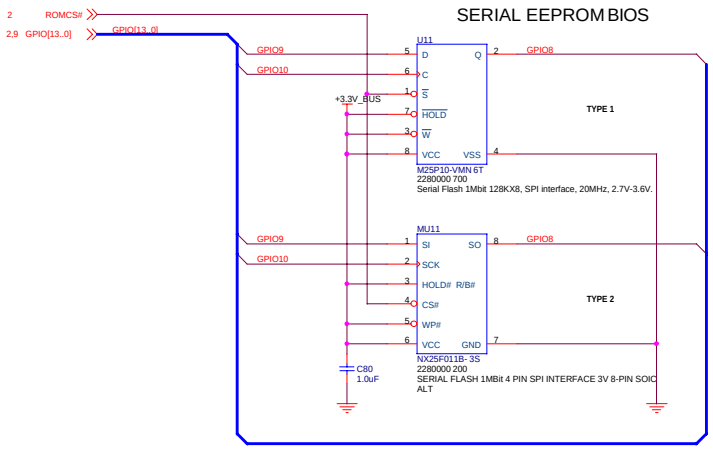
Title	AGP RV250 64/128MB BGA	
Size B	Document Number 105-GN964-00B	Rev 0
Date: 星期三, 八月 15, 2001	Sheet 7 of 19	



<Variant Name>

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Title: AGP RV250 64/128MB TSOP

Size: C | Document Number: 105-GN964-00B | Rev: 0

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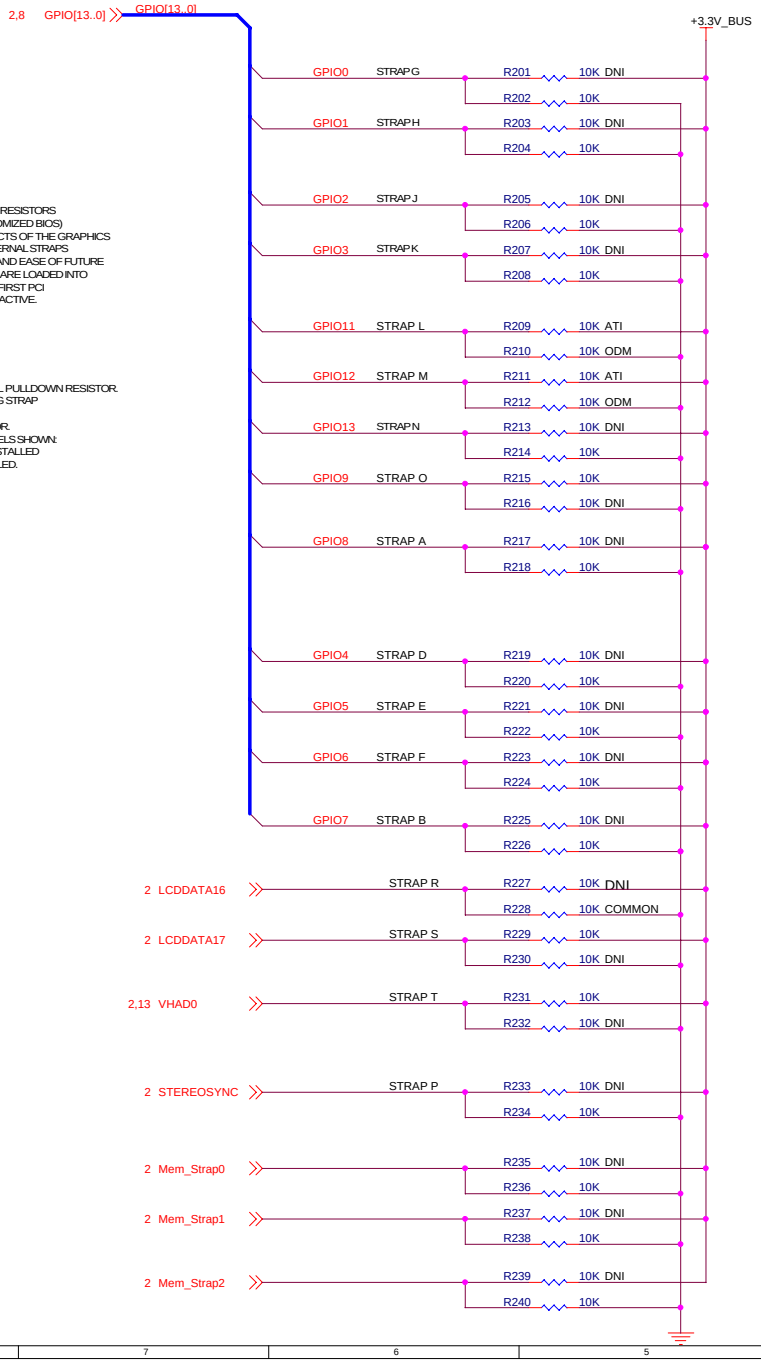
OPTION STRAPS



NOTE: THE M7
SUPPORTS THE USE OF STRAP RESISTORS
(AS AN ALTERNATIVE TO CUSTOMIZED BIOS)
TO CONFIGURE CERTAIN ASPECTS OF THE GRAPHICS
SUBSYSTEM. THE USE OF EXTERNAL STRAPS
PROVIDES ADDED FLEXIBILITY AND EASE OF FUTURE
UPGRADE. STRAPPED VALUES ARE LOADED INTO
INTERNAL REGISTERS ON THE FIRST PCI
COMMAND AFTER RESET# IS INACTIVE.

NOTE:

THE I/O BUFFERS USE INTERNAL PULLDOWN RESISTOR.
THIS DICTATES THE FOLLOWING STRAP
CONFIGURATION:
STRAP TO VCC VIA 10K RESISTOR.
THIS PROVIDES THE LOGIC LEVELS SHOWN:
'0' WHEN 10K RESISTOR NOT INSTALLED
'1' WHEN 10K RESISTOR INSTALLED.

STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM **1011 - Serial M25P10 ROM (ST), chip IDis from ROM** 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1001
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000 (internal pull-down)
VGA_DISABLE	GPIO(7)	**0 - VGA controller capabillity enableed.** 1 - The device will not be recognized as the systemis VGA controller.	0
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select **00 - single function device.** 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	00
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

<Variant Name>

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Title: AGP RV250 64/128MB TSOP

Size: B | Document Number: 105-GN964-00B | Rev: 0

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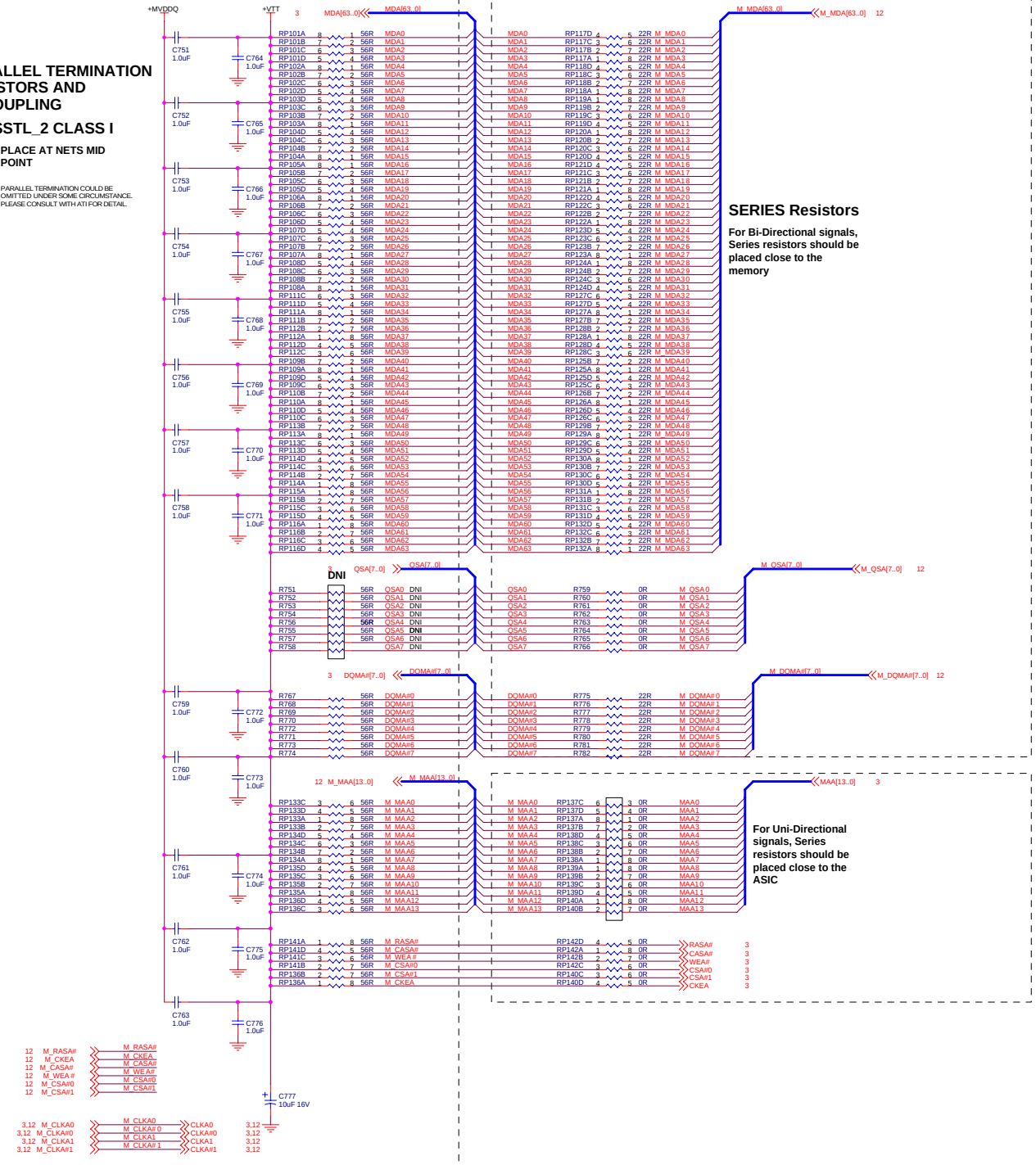
TERMINATION FOR MEMORY CHANNEL A

PARALLEL TERMINATION RESISTORS AND DECOUPLING

SSTL_2 CLASS I

PLACE AT NETS MID POINT

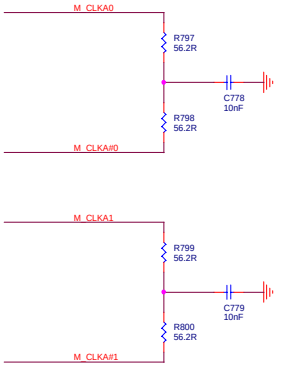
PARALLEL TERMINATION COULD BE OMITTED UNDER SOME CIRCUMSTANCE. PLEASE CONSULT WITH ATI FOR DETAIL.



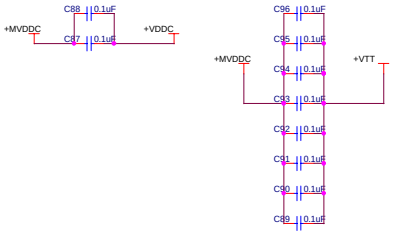
CLOCK terminations

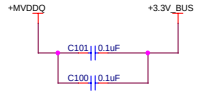
Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



Symbol change 56R instead of 121R





<Variant Name>

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Title	AGP RV250 64/128MB TSOP	
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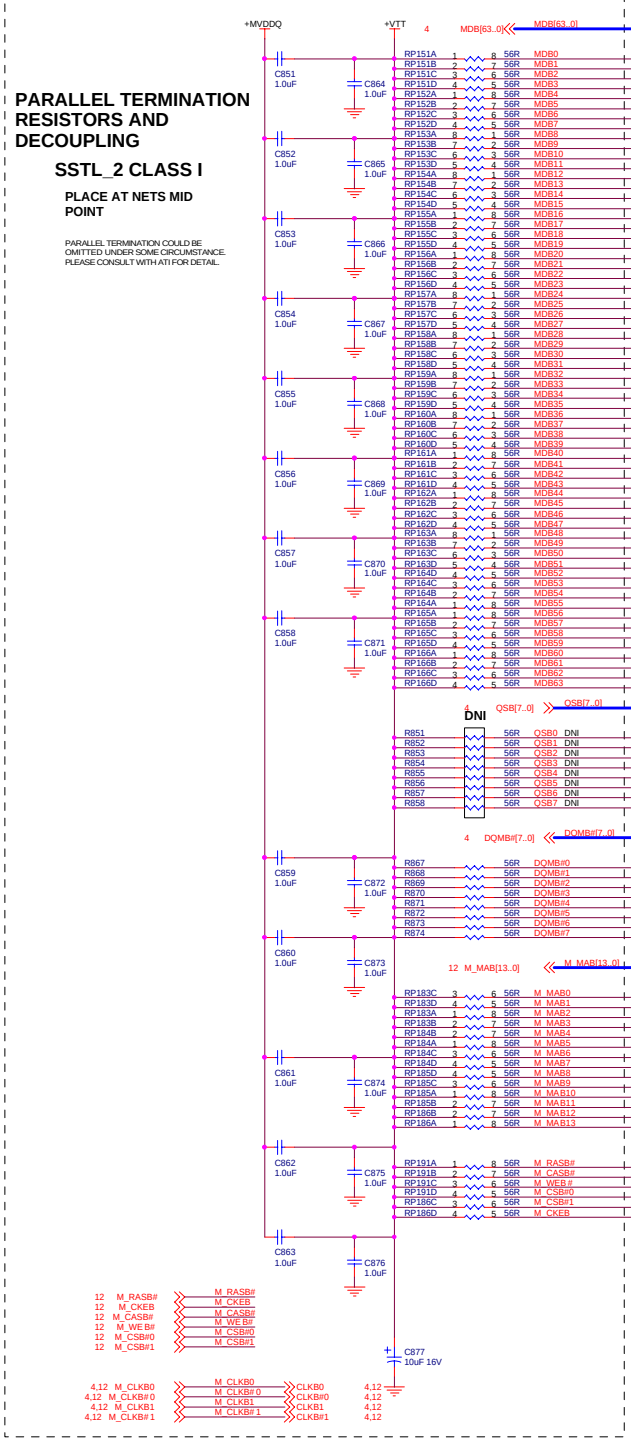
TERMINATION FOR MEMORY CHANNEL B

PARALLEL TERMINATION RESISTORS AND DECOUPLING

SSTL_2 CLASS I

PLACE AT NETS MID POINT

PARALLEL TERMINATION COULD BE OMITTED UNDER SOME CIRCUMSTANCE. PLEASE CONSULT WITH ATI FOR DETAIL.



SERIES Resistors

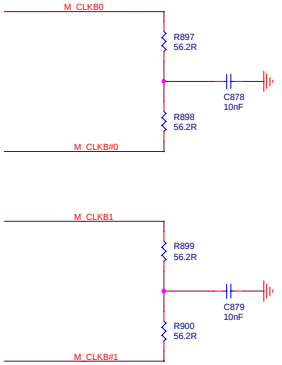
For Bi-Directional signals, Series resistors should be placed close to the memory

For Uni-Directional signals, Series resistors should be placed close to the ASIC

CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



There are two standard Terminations that are supported by for DDR memory. Series or Parallel. Please consult design guide for performance impacts.

<Variant Name>

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Title	AGP RV250 64/128MB TSOP	
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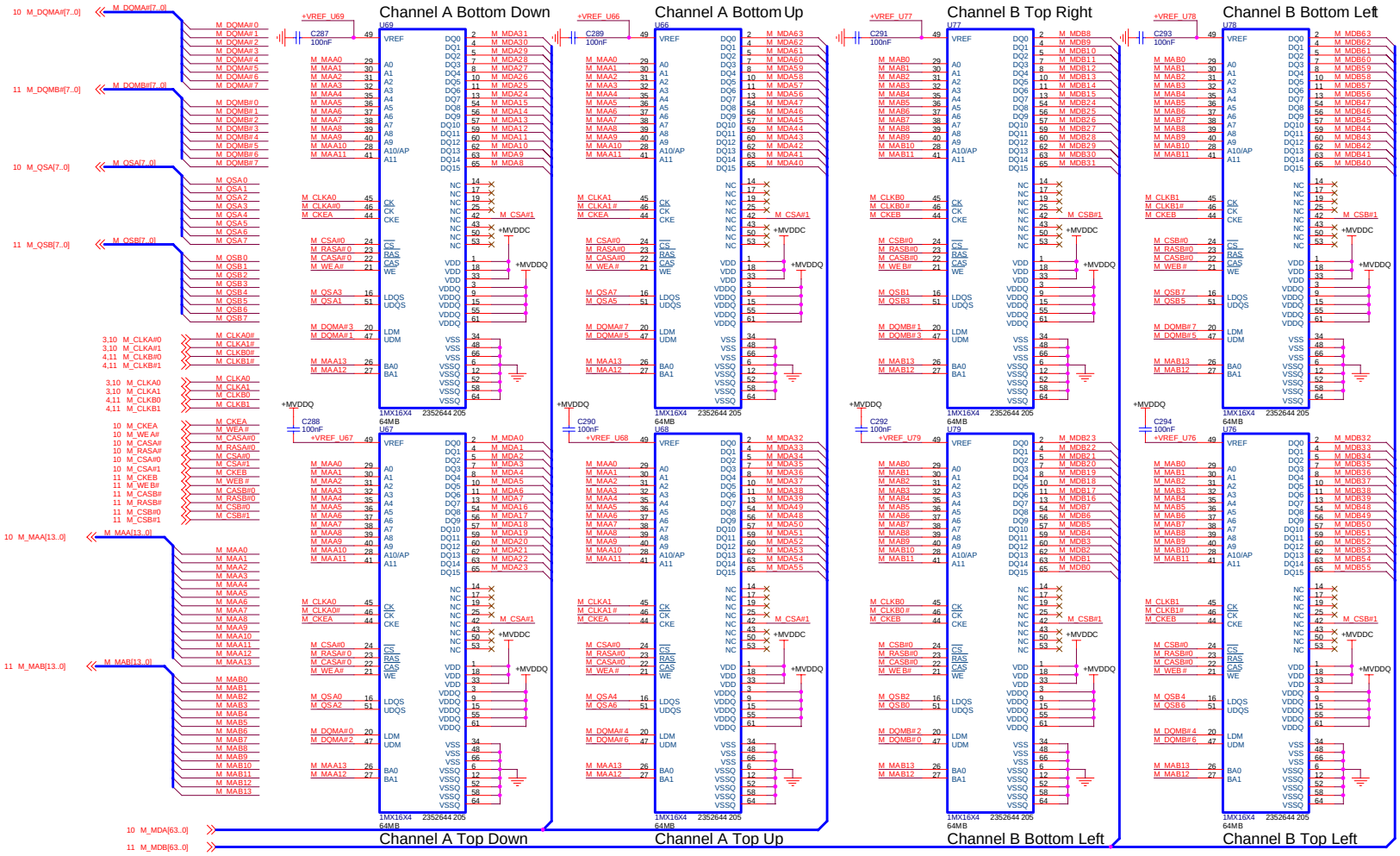

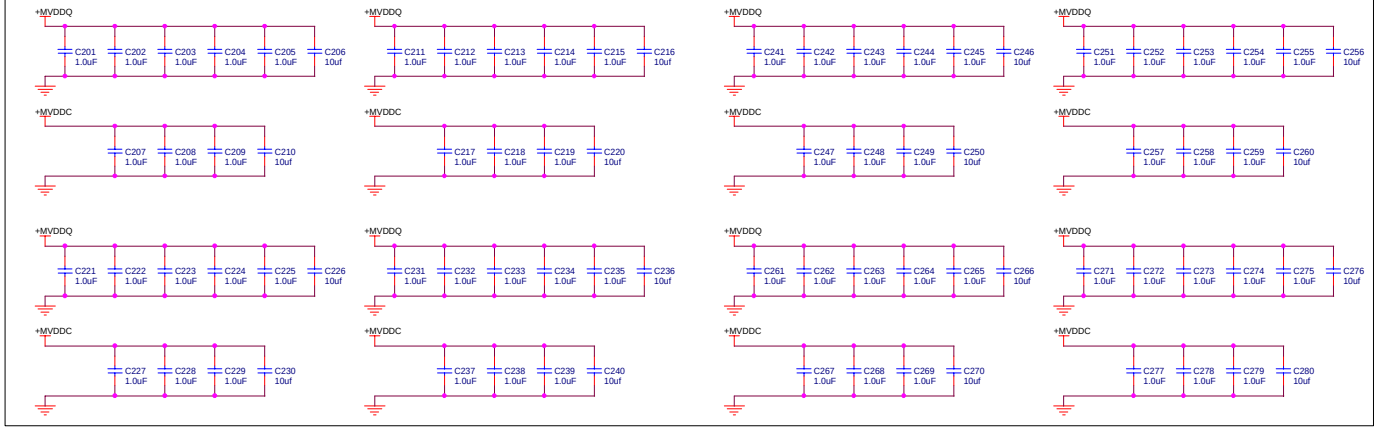

Part number for 8Mx16?

DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

<Variant Name>

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Layout Guide line of THEATER

#1 : C385 and C386 have to be placed as close as possible to the pins of Rage THEATER

#2 : C397 should be placed close to J2

OPTIONAL +3.3V REGULATOR

+5V_BUS REG1 3.3V RVDD +3.3V_BUS

IN OUT ADJ CASE

C374 100nF C373 100uF R376 0R

+3.3V_BUS

C565 100nF C375 100nF C376 100nF C377 100nF C378 22uF

U12

RAGE THEATER

VDDR VDDR VDDR VDDR VDDC VDDC VDDC VDDR VDDC

SAD0 SAD1 SAD2 SAD3 SAD4 SAD5 SAD6 SAD7

DS_VIPCLK AS_HCTL SRDY_IRQB HAD0 HAD1

SDA SCL

ADO ADIO WS BITCLK

SPDIF

BYTCLK SYNC Y_RED C_GREEN COMP_BLUE RSET

CLKOUT0_GPIO0 CLKOUT1_GPIO1 CLKOUT2_GPIO2 GPIO3 GPIO4 GPIO5 GPIO6

PDATA0 PDATA1 PDATA2 PDATA3 PDATA4 PDATA5 PDATA6 PDATA7 PCLK

VAGCVDD VAGCVSS VAGCVSS VDACVDD VDACBVSS VDACJVSS VIND0 VIND1 VIND2 VIND3 VIND4 VIND5 VIND6 VIND7 VINGATEA VINGATEB CF CR VAGCCAP VIDEOGNDSENSE VCLAMPCAP VADCDVDD VADCAVDD VADCDVSS VADCAVSS COMP0 COMP1 COMP2 YF_COMP3 YR_COMP4 XTALIN XTALOUT TESTEN RESETB PLLVDD PLLVSS

VSSC VSSC VSSC VSSC VSSC VSSR VSSR VSSR VSSR VSSR VSSR VSSC VSSC

CLK_VIPCLK VPHCTL VHAD0 VHAD1 R195 R196 R197 R198 33R

R380 4.7K DNI +3.3V_BUS R381 10K L0C1 MPPEN SPDIF R382 10K

R139 220R RT_CLKOUT 2

R374 383R R384 10K R140 150 R

VID/DVO[7..0] VID/DVO[7..0] 2

RP193A RP194A VID/DVO0 VID/DVO1 VID/DVO2 VID/DVO3 VID/DVO4 VID/DVO5 VID/DVO6 VID/DVO7

R389 33R CLK_VID/DVO 2

PLACE AS CLOSE TO THE RAGE THEATRE AS POSSIBLE.

RVDD B21 3.3uH R1092 10R C393 47uF C394 100nF

CR C889 2.2uF C924 68nF/X7R C925 22nF

C43 2.2uF YR C890 2.2uF

2 RT_XTALIN 2 RT_XTALOUT

1,2 AGP_RESET#

CompR L28 3.3uH C891 330pF C892 330pF R1065 75.0R 1%

RVDD R109B 10R B34 3.3uH C399 47uF C400 100nF

R392 3K3

TV-OUT

YR L8 3.3uH YRIN R1063 75.0R 1% C885 330pF C886 330pF

CR L9 3.3uH CRIN R1064 75.0R 1% C887 330pF C888 330pF

VGND

Y/R L4 1.8uH R379 75.0R 1% C383 82pF C384 82pF Luma_F Chroma_F Comp_F

C/G L2 1.8uH R383 75.0R 1% C387 82pF C388 82pF R508 0R

COMP/B L3 1.8uH COMP1 R385 75.0R 1% C391 82pF C392 82pF

14,15 G/Y_DAC2_F Luma

CREATE DUAL FOOTPRINT FOR BEAD 0603/0805

Rm6 R501 0R TVO_ONLY Bm1 B91 120R TVO_CRT

Q91 2N7002E TVO_CRT Qm1 Rm7 R504 1.5K TVO_CRT Y/R

14,15 R/C_DAC2_F Chroma

CREATE DUAL FOOTPRINT FOR BEAD 0603/0805

Rm8 R502 0R TVO_ONLY Bm2 B92 120R TVO_CRT

Q92 2N7002E TVO_CRT Qm2 Rm9 R505 1.5K TVO_CRT C/G

14,15 B/COMP_DAC2_F Comp

CREATE DUAL FOOTPRINT FOR BEAD 0603/0805

Rm10 R503 0R TVO_ONLY Bm3 B93 120R TVO_CRT

Q93 2N7002E TVO_CRT Qm3 Rm11 R506 1.5K TVO_CRT COMP/B

Cm1

Dm1 BAV99 TVO_CRT D91

R507 0R TVO_CRT Rm14 C507 47nF TVO_CRT Cm2 R510 5.1M TVO_CRT Rm13

15 VSYNC_DAC2_B

+5V_BUS C508 100nF TVO_CRT

U7A SN74ACT86D 2430001 100 COMMON

Rm12 R509 10K TVO_CRT

	Install	DNI
VIDEO-OUT&CRT2	Bm1,Bm2,Bm3,Qm1,Qm2, Qm3,Rm7,Rm9,Rm11,Rm12, Cm1,Cm2,Rm13,Rm14,Dm1	Rm6,Rm8,Rm10, Cm3,Cm4,Cm5
VIDEO-OUT ONLY	Rm6,Rm8,Rm10, Cm3,Cm4,Cm5	Bm1,Bm2,Bm3,Qm1,Qm2, Qm3,Rm7,Rm9,Rm11,Rm12, Cm1,Rm13,Rm14,Dm1,Cm2

Layout Guide line of THEATER

#1 : C27 and C28 have to be placed as close as possible to the respective pins of Rage THEATER

#2 : VINGND should be seperated from Digital or Chassis Ground and have no loops

#3 : VINGND should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

Chroma_F R520 0R Comp_F R521 0R CRIN R522 0R R519 0R Luma_F

CVBSYIN R513 0R YRIN R514 0R CompR

P500 9-pin:4-pin:9-pin:3-pin CON_S_VIDEO_9P_STD VIVO:TV_OUT:VIDCAP:STEREO_OUT

CGND

CRIN YRIN P501 9-pin:4-pin:9-pin:3-pin CON_S_VIDEO_9P_STD VIVO:TV_OUT:VIDCAP:STEREO_OUT

R523 0R CompR

AV_IN CompR JACK+RCA-D3-SB-YL

JA CRIN CompR YRIN CD-D1x4-BK-SBTJ C20 22pF C21 22pF C22 22pF

AV_OUT Comp_F JACK+RCA-D3-SB-YL

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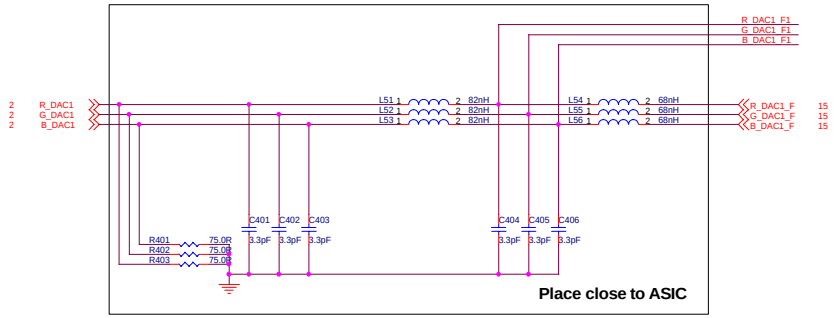
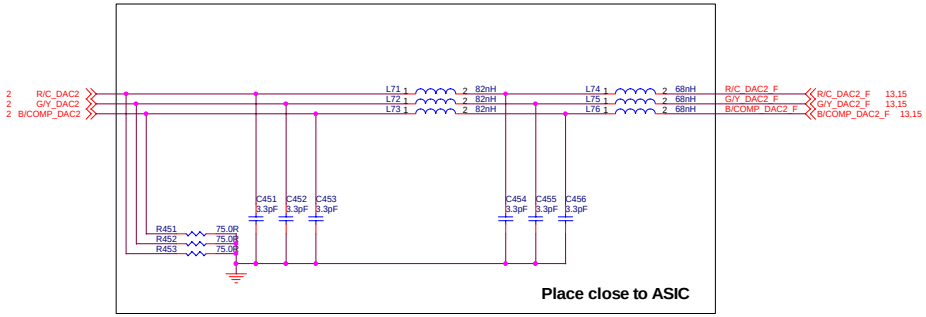
PRIMARY CRT



SECONDARY CRT



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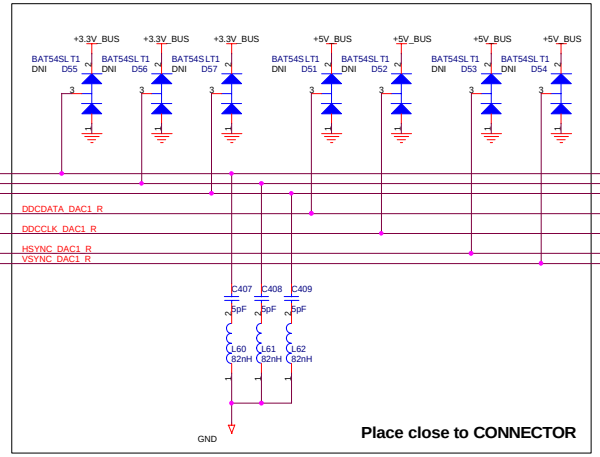
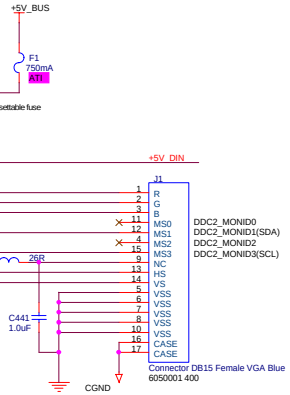
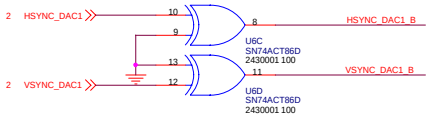
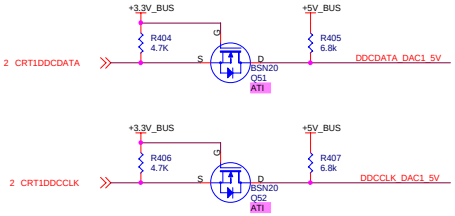
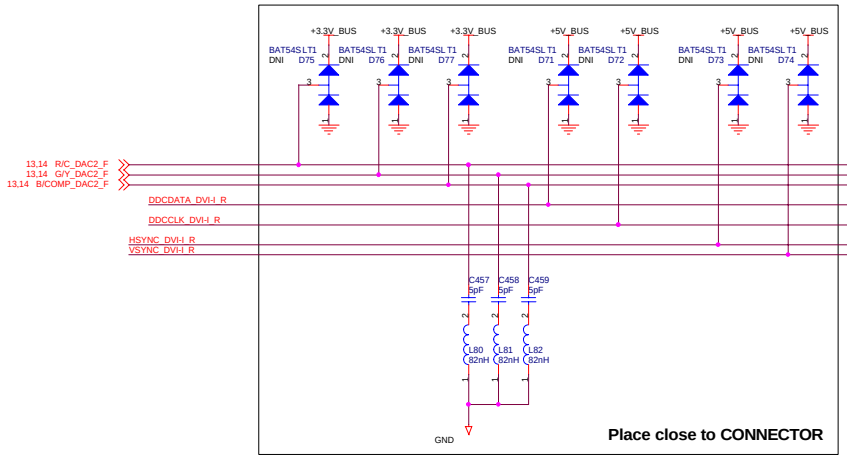
OPTIONAL ESD/HOTPLUG PROTECTION DIODES

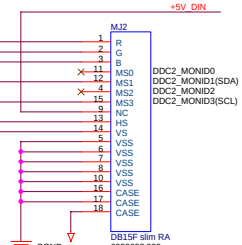


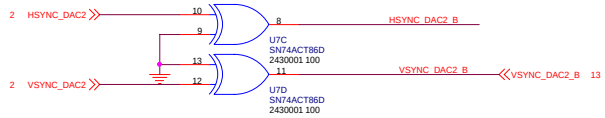


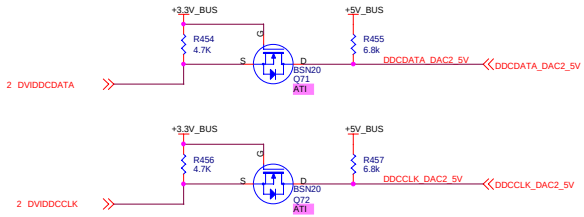


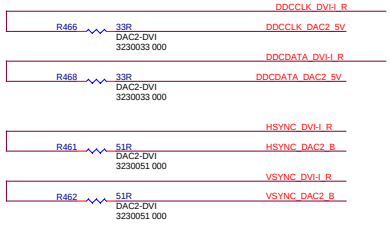












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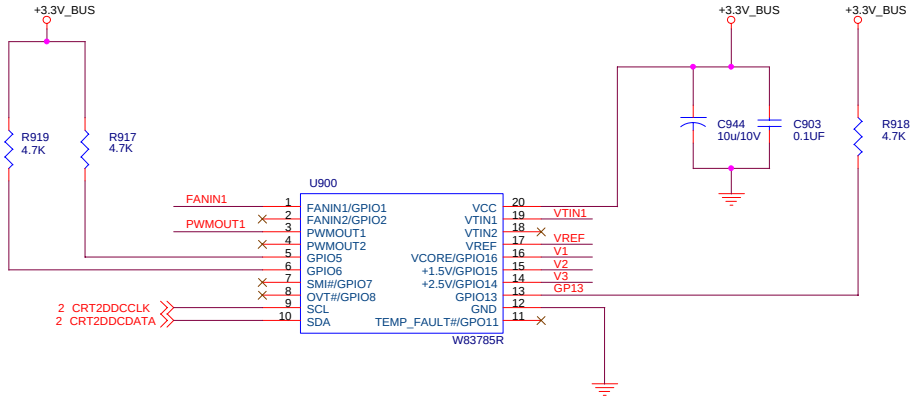
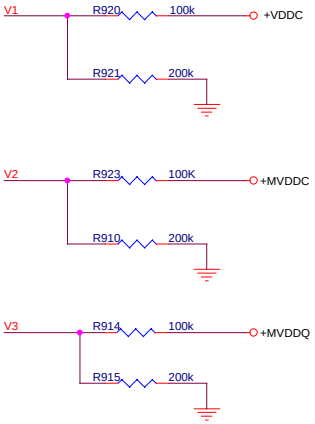
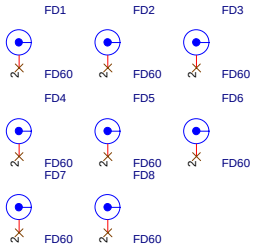
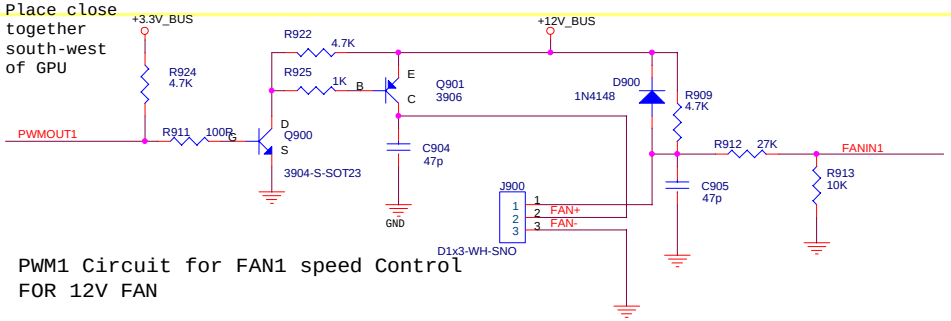




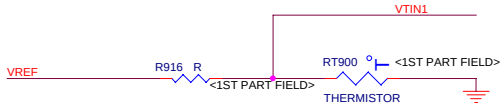


Place close together south-west of GPU



PWM1 Circuit for FAN1 speed Control
FOR 12V FAN

VOLTAGE SENSORING CIRCUIT



TEMPERATURE SENSORING CIRCUIT

<Variant Name>

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33 Commerce Valley Drive East
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(905) 882-2600

Title	AGP RV250 64/128MB BGA	
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