


- History
- 1. add L18 with co-aly res. (11/8)
  - 2. Remove USB power sense(11/11)
  - 3. Remove 5V pwrn ic option(11/12)
  - 4. Remove PTC and FBVDDQ PH2 INPUT OPTION (11/14)
  - 5. Remove 1V8\_MAIN output option parts(11/14)
  - 6. Remove J15 and parts(11/16)
  - 7. Remove Input Power Balancing Switcher(11/16)
  - 8. add MLCC cap. on page 16(12/11)

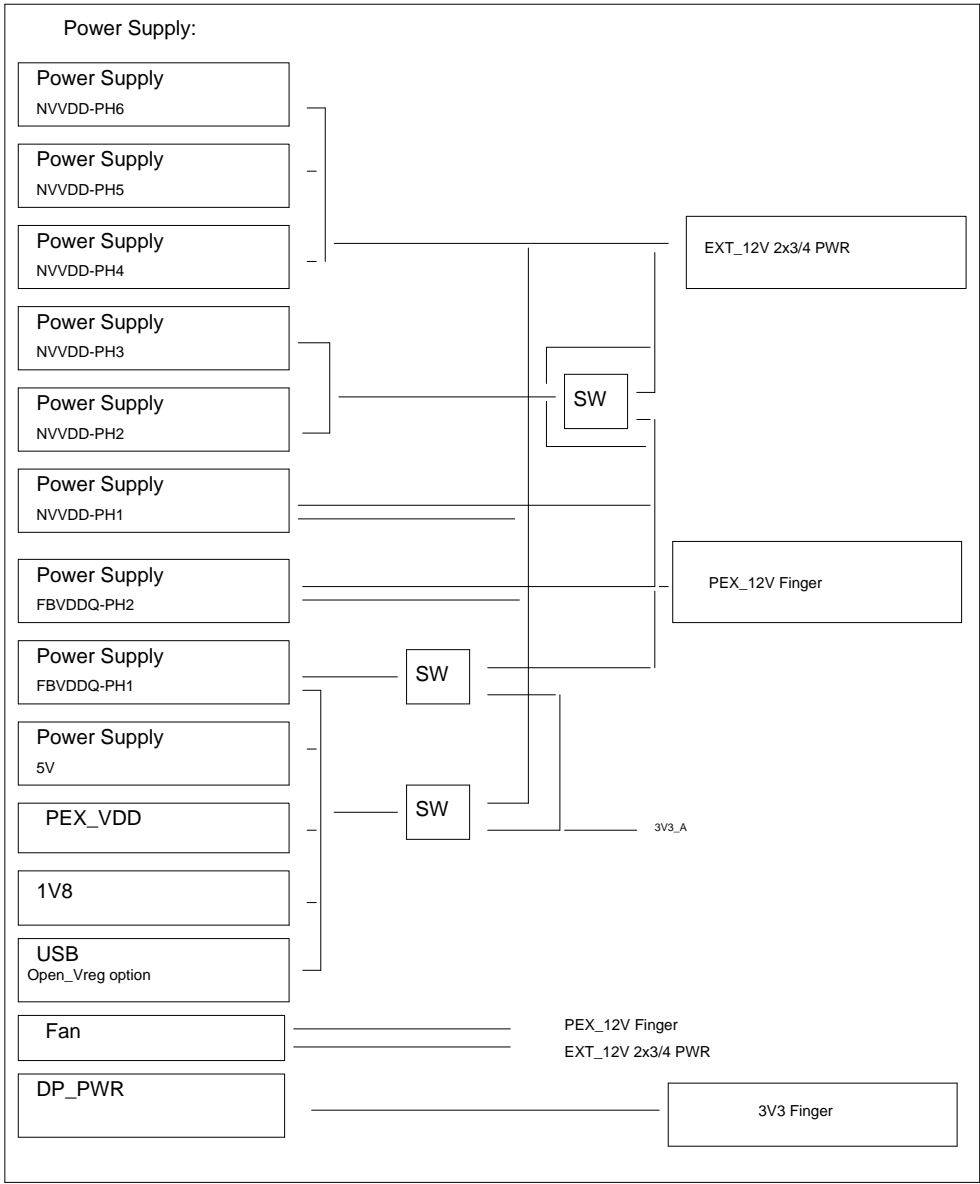
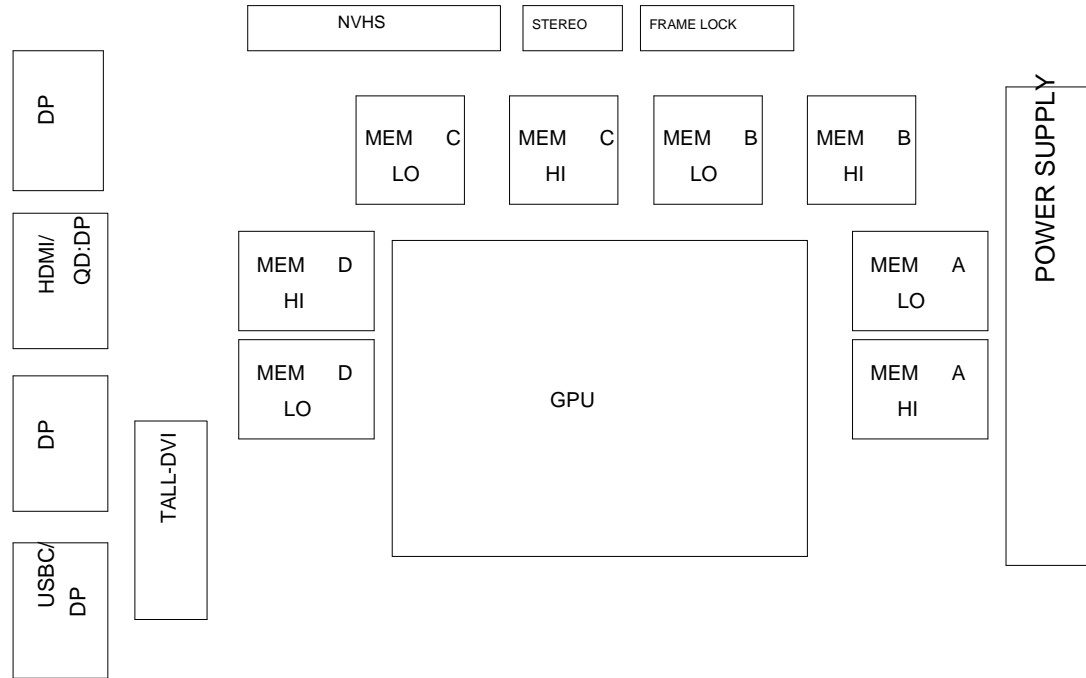
PG160-B02 8GB GDDR6, 256b, X16  
DP + DP + HDMI/DP + DP

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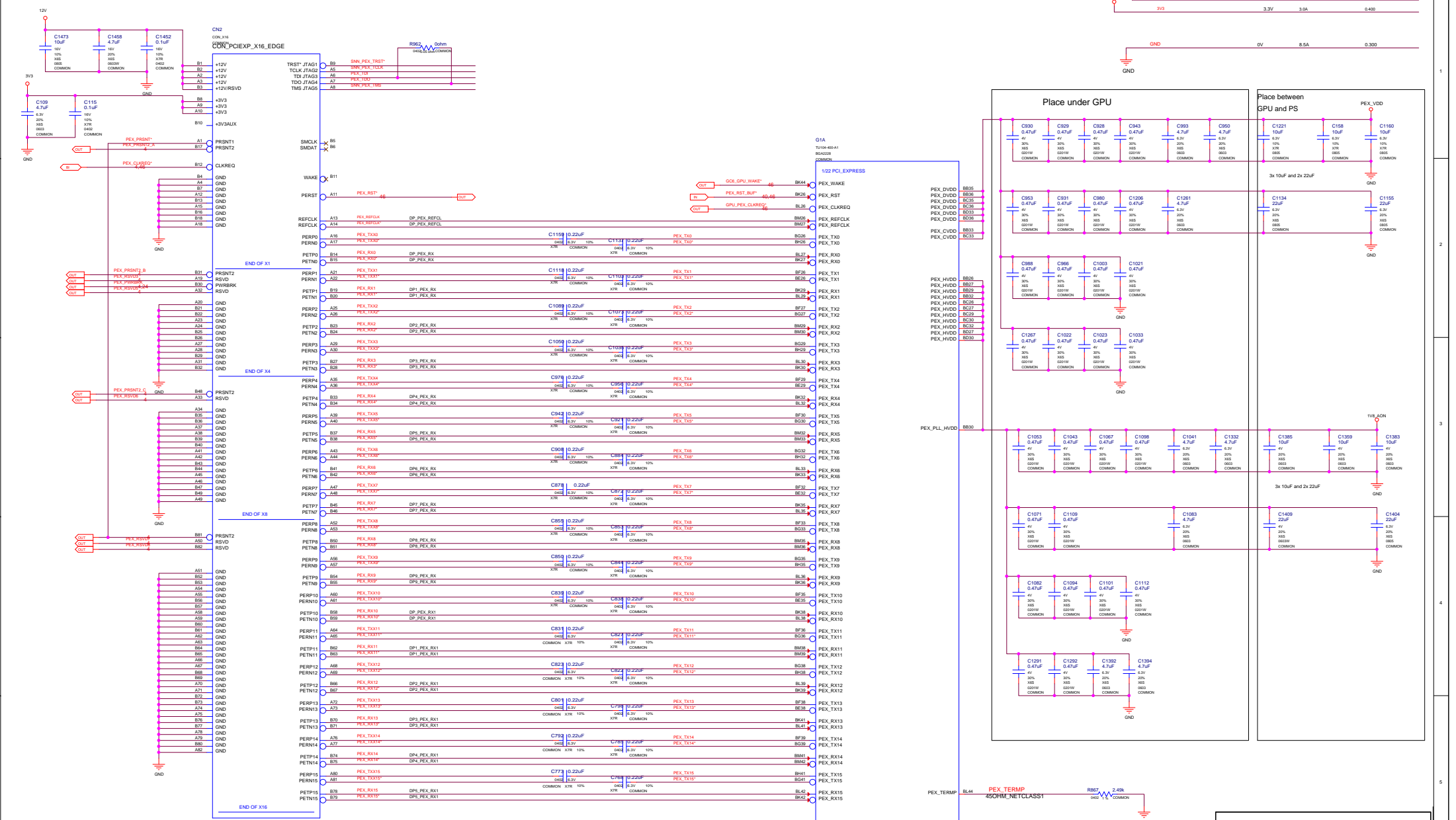


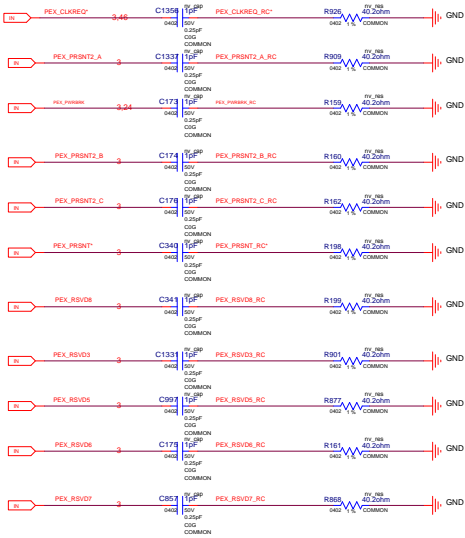
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Custom		A
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Block Diagram

Title			
Block Diagram			
Size	Module Name:		Rev
Custom			A
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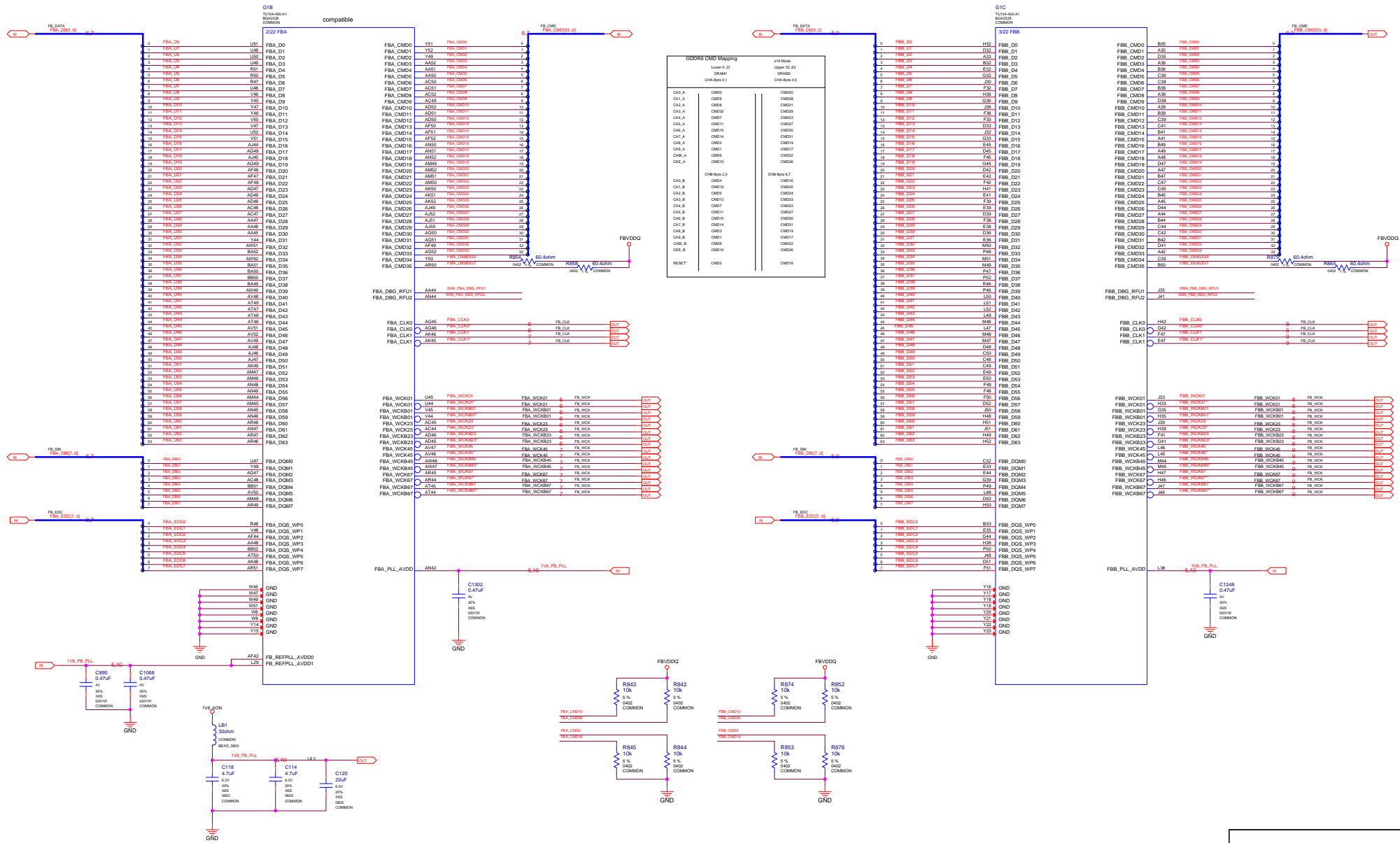




PCIE RC TERM

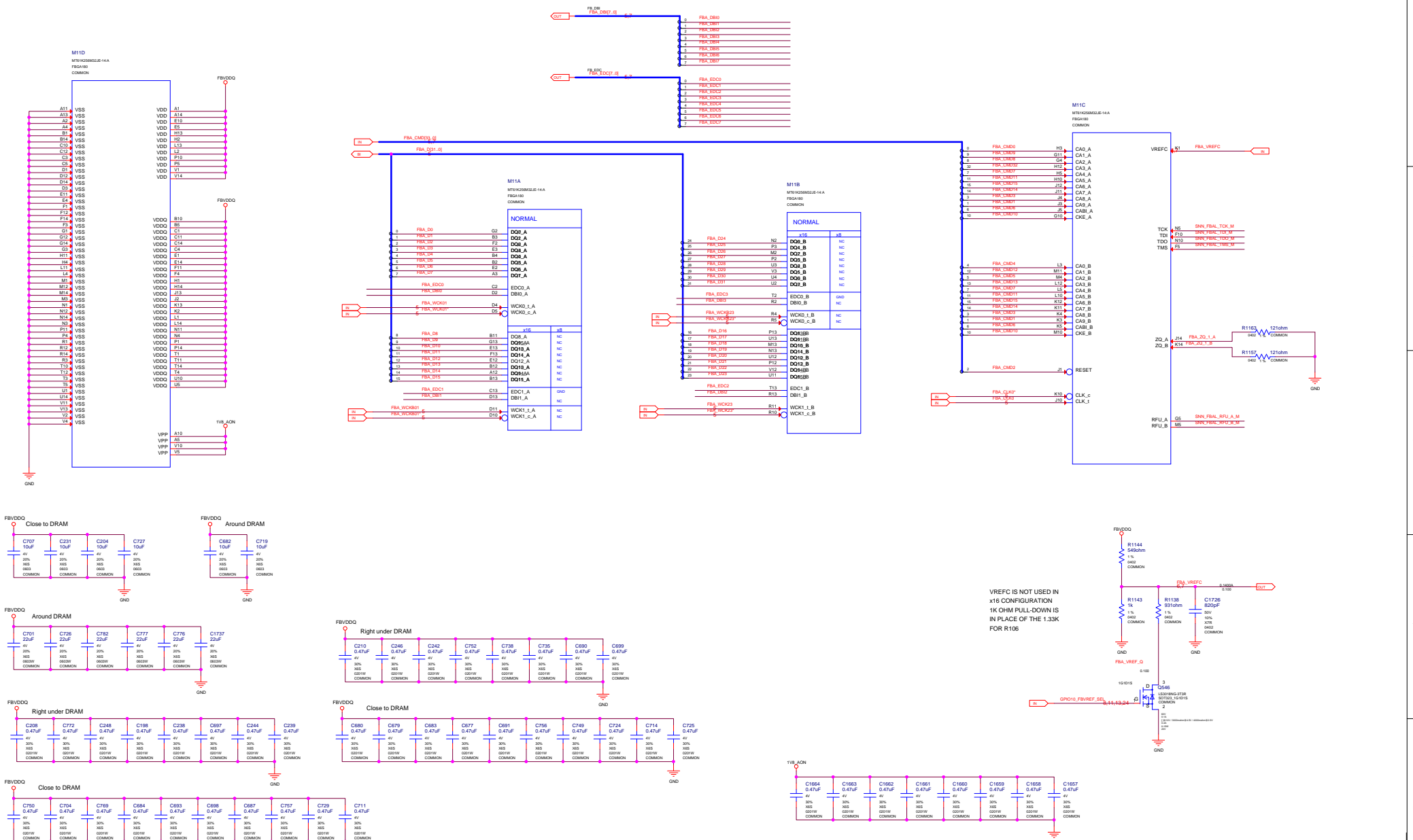


Title		
PCIE RC TERM		
Size	Module Name:	Rev
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MEMORY: GPU FB\_AB

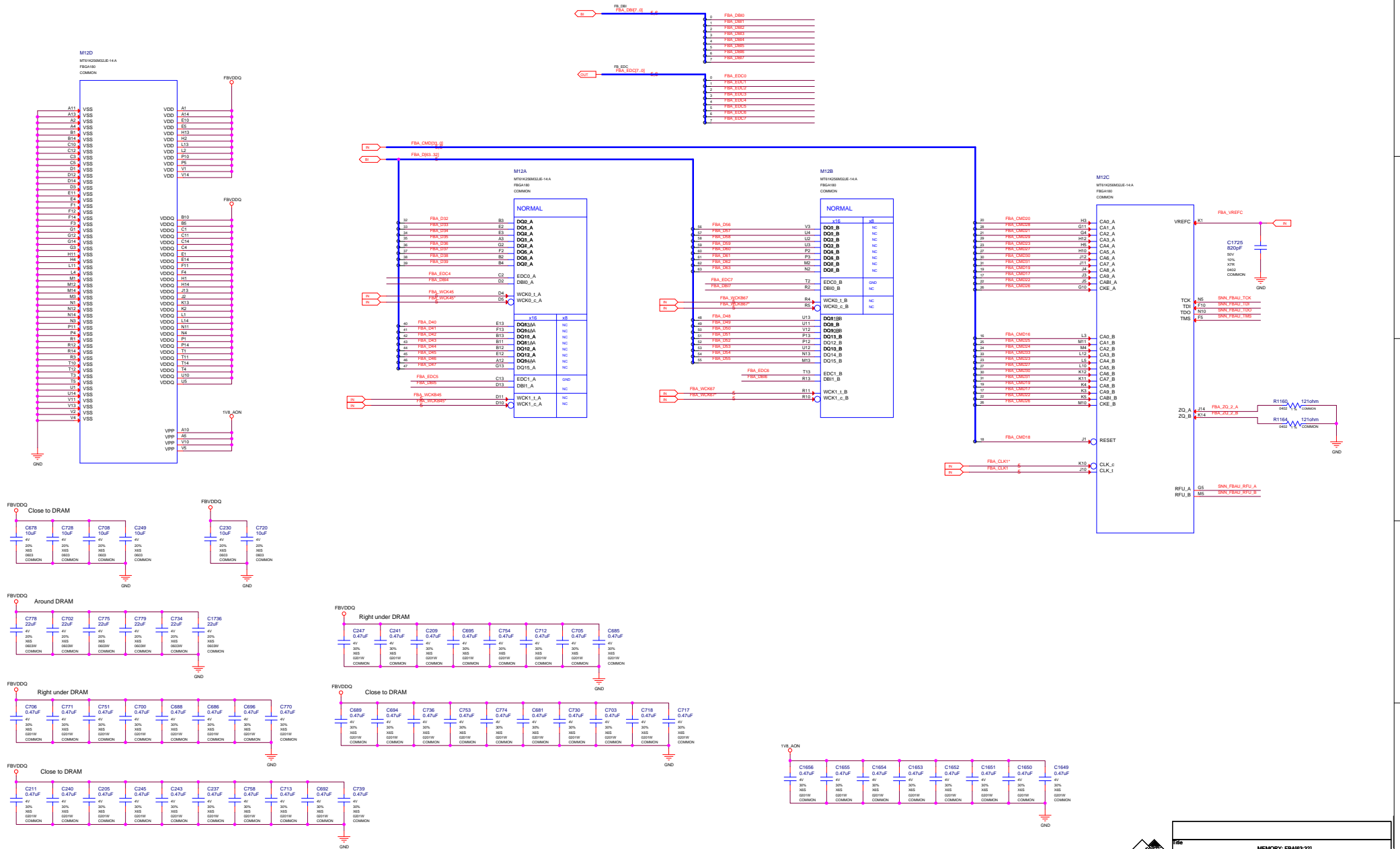
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	Size	Module Name:	Rev
	Custom		A
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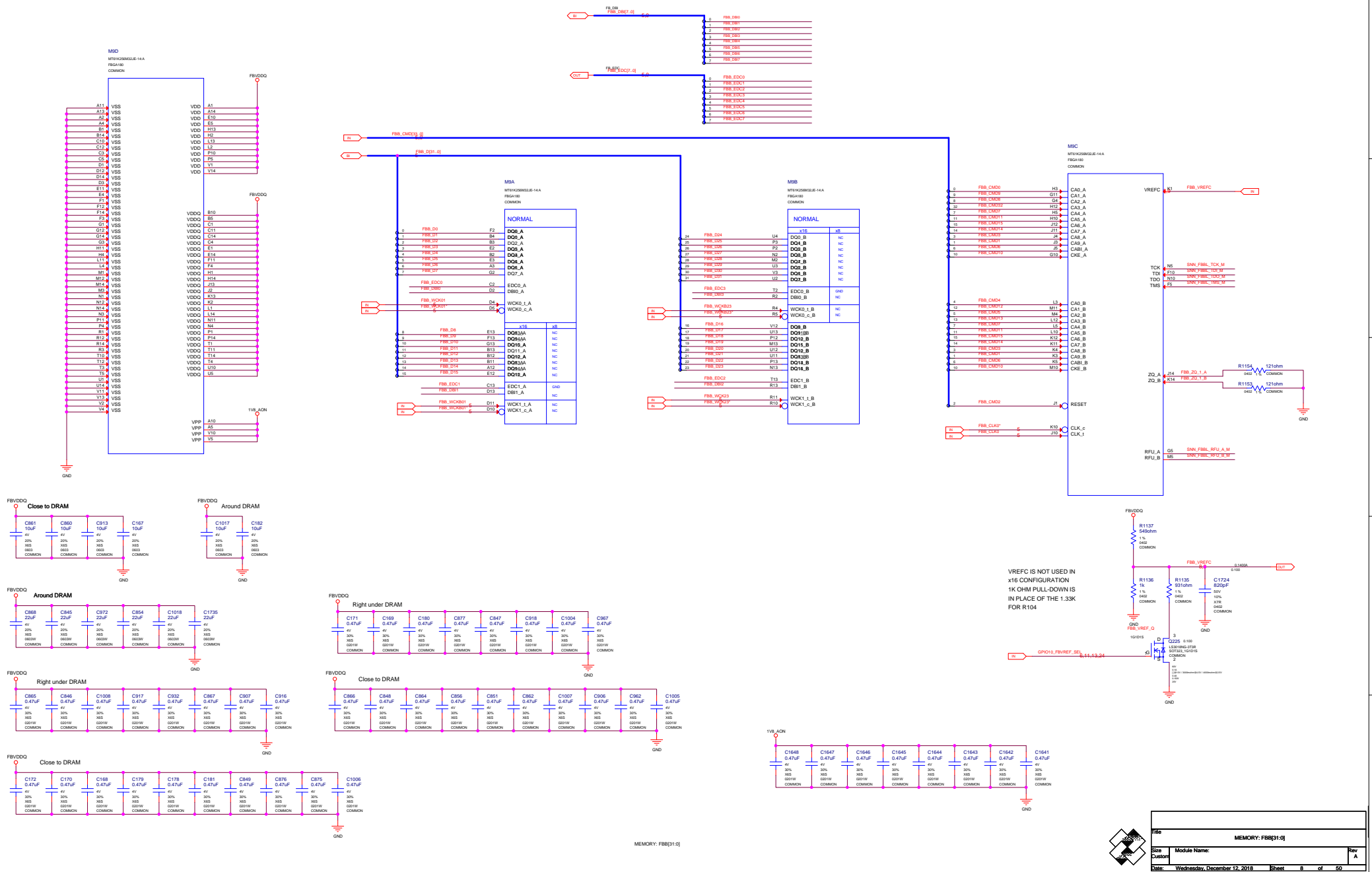


MEMORY: FBA[31:0]

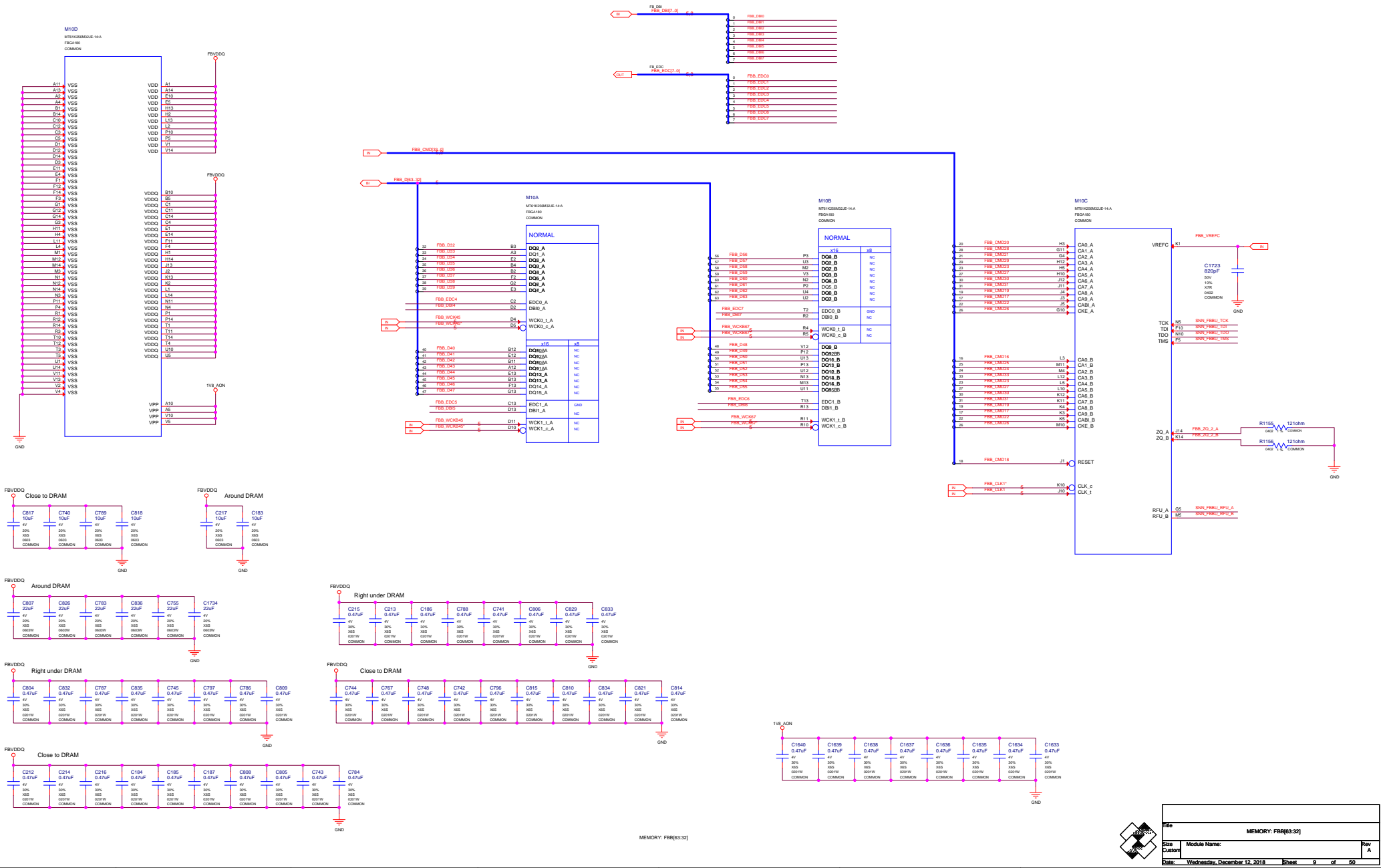


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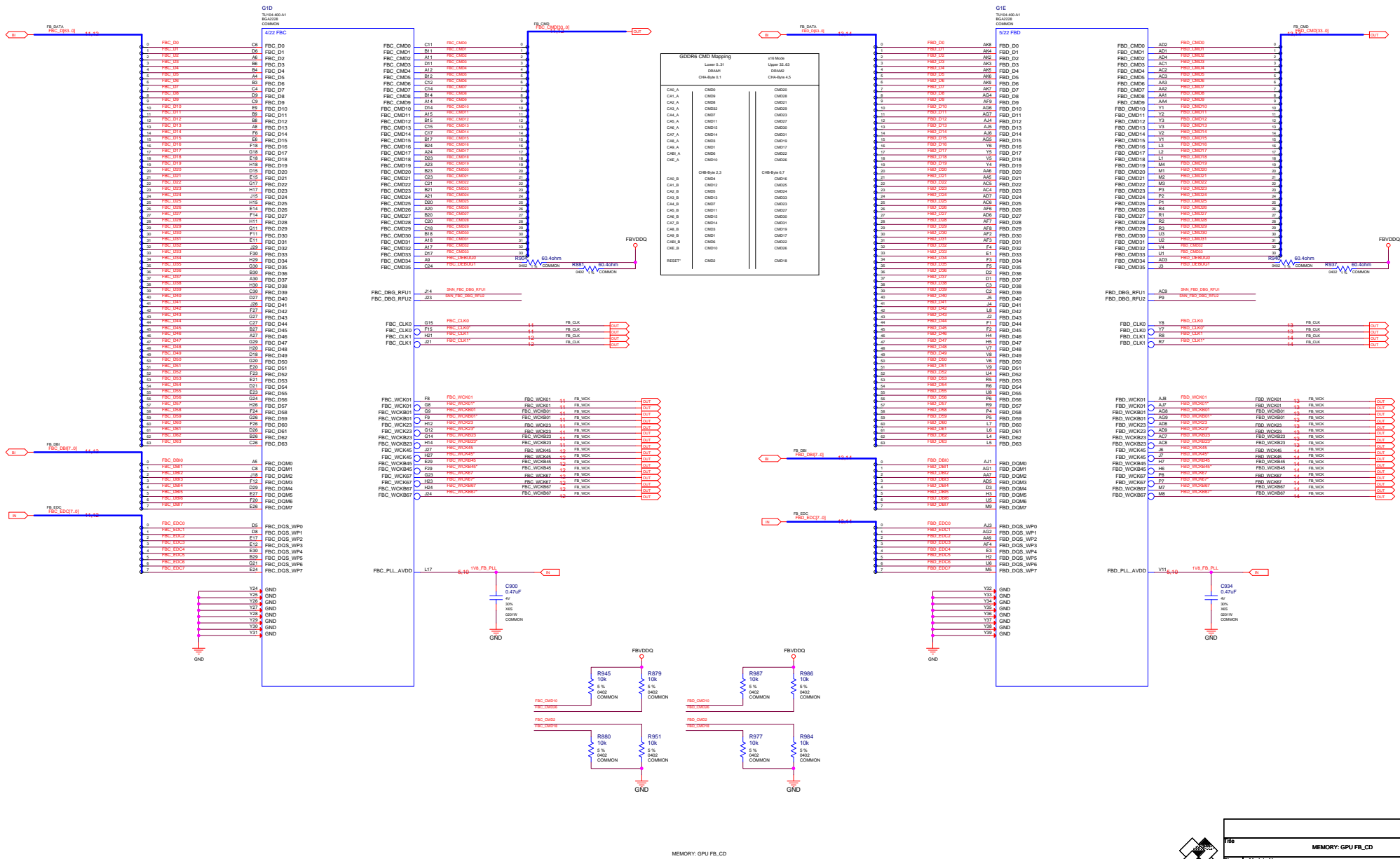




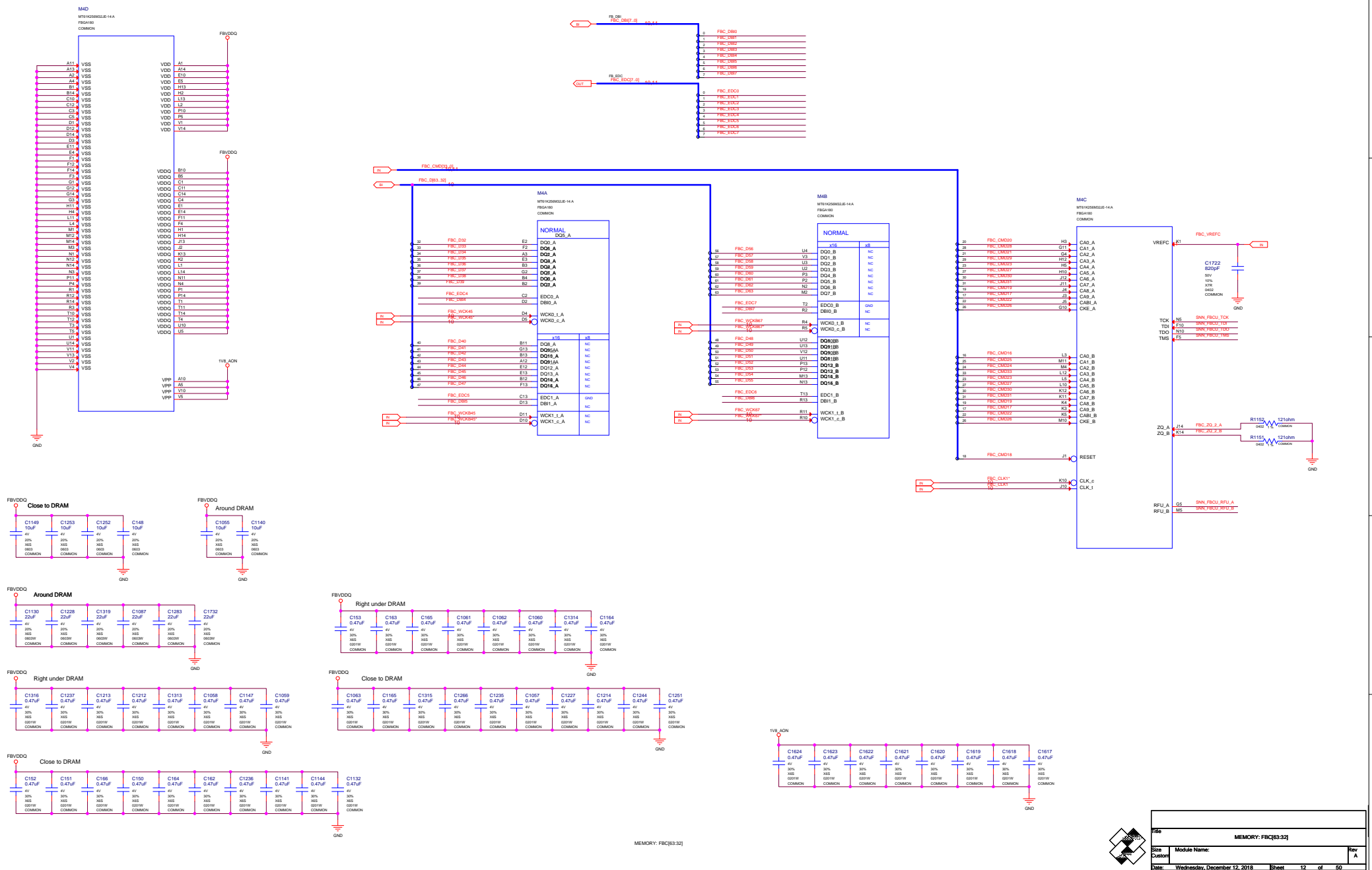


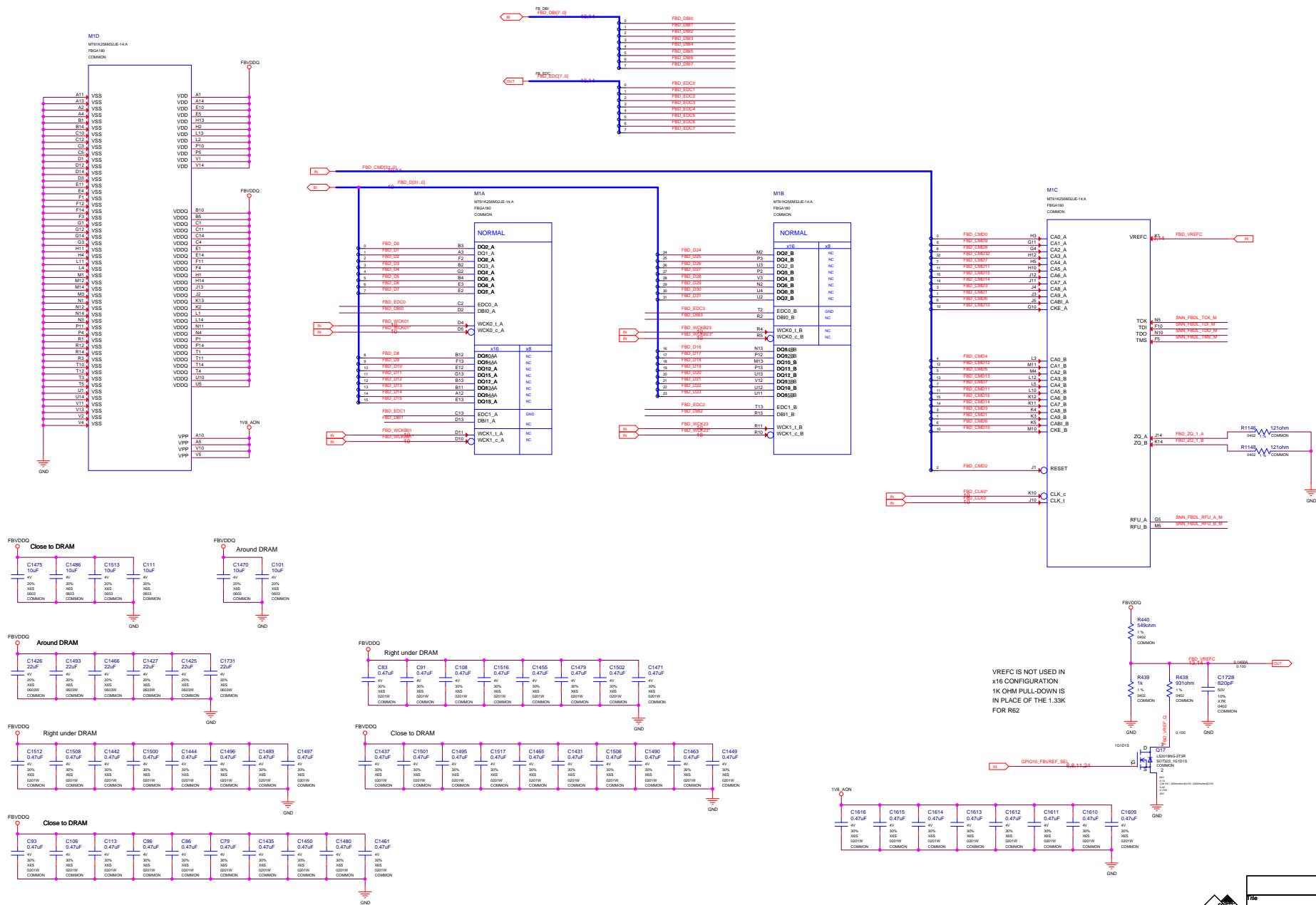
MEMORY: FBB[63..32]

Title			MEMORY: FBB[63..32]		
Size			Module Name:		
Custom			Rev A		
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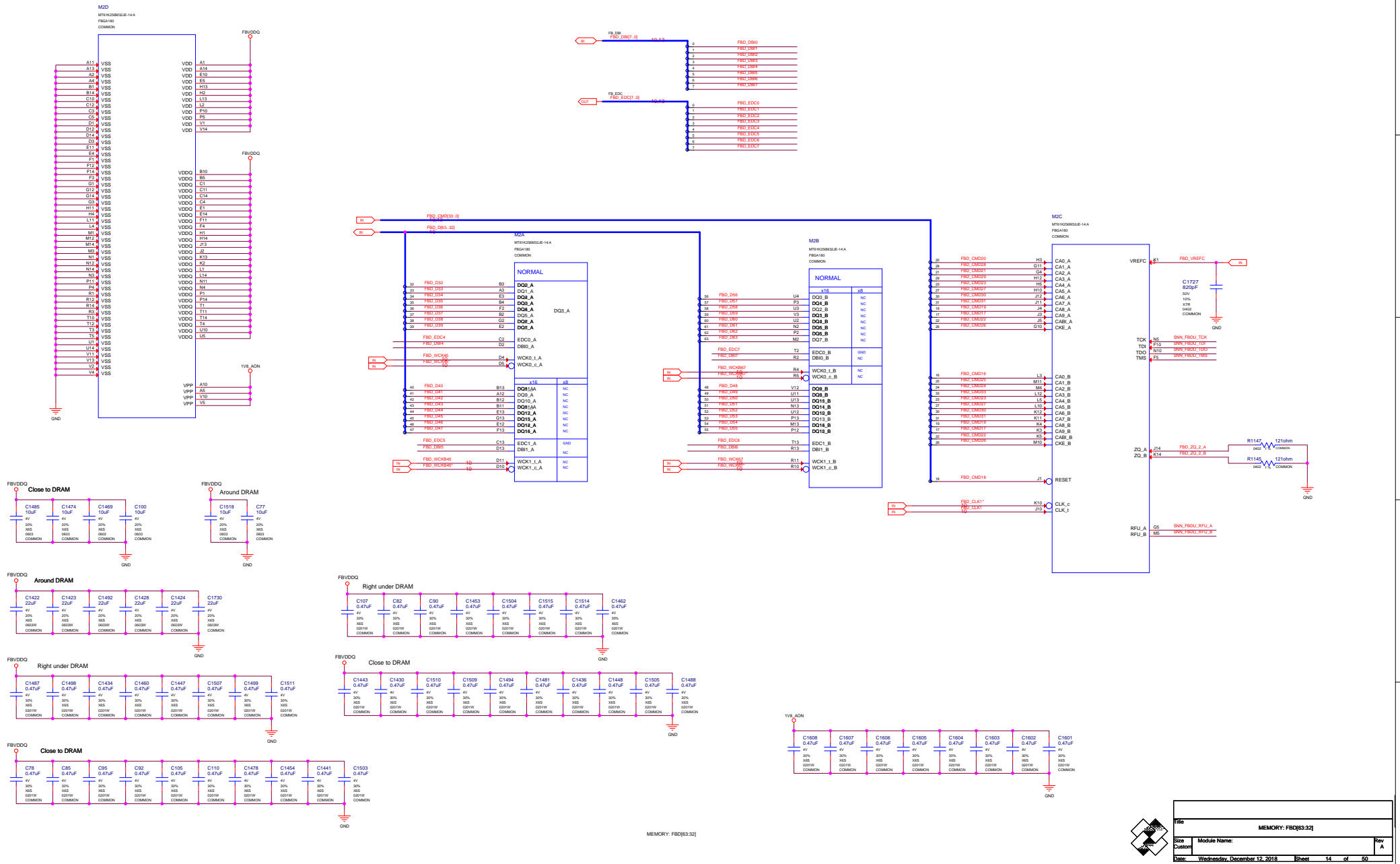


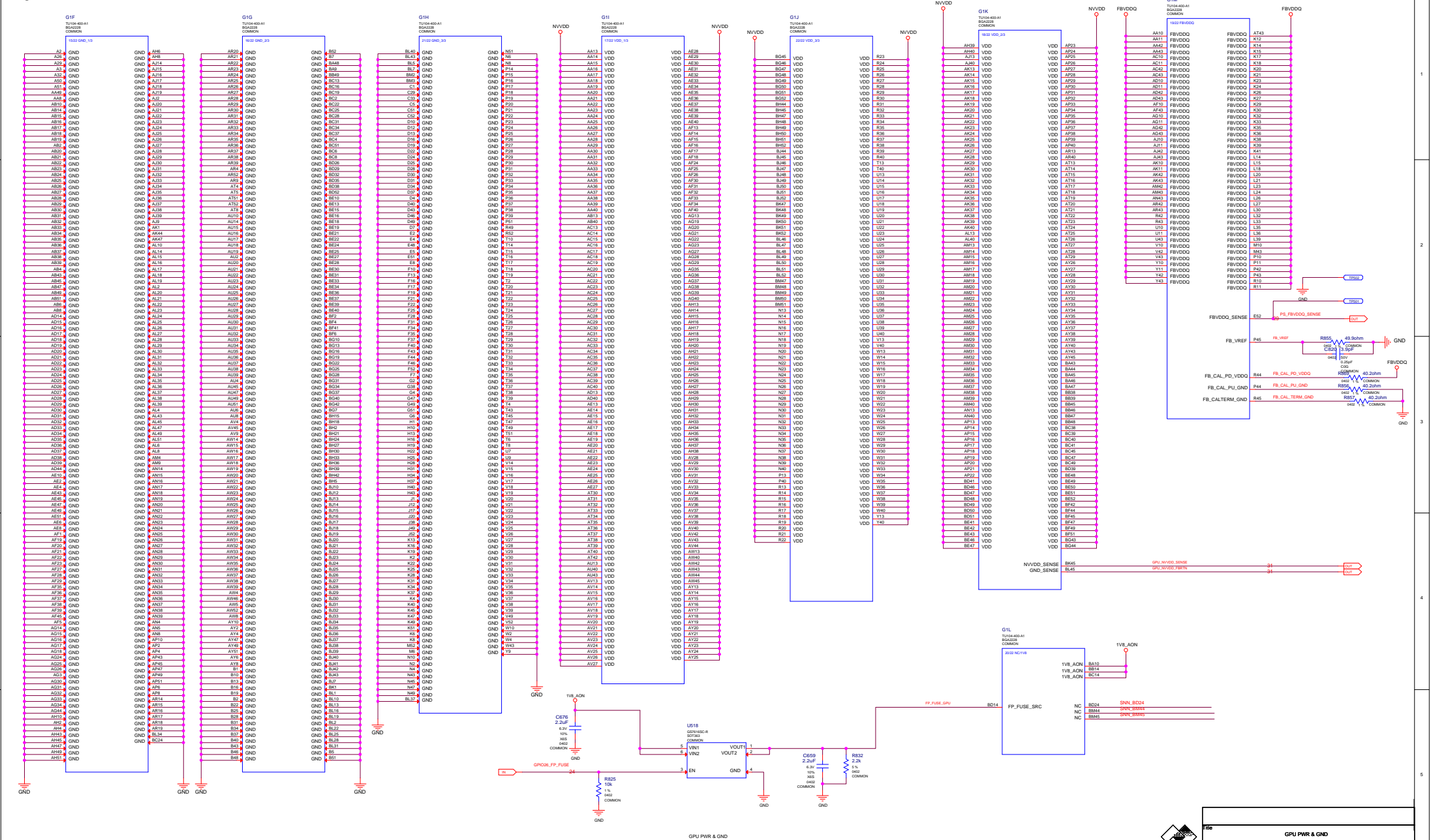
MEMORY: FBD[31:0]

VREFC IS NOT USED IN  
x16 CONFIGURATION  
1K OHM PULL-DOWN IS  
IN PLACE OF THE 1.33K  
FOR R62

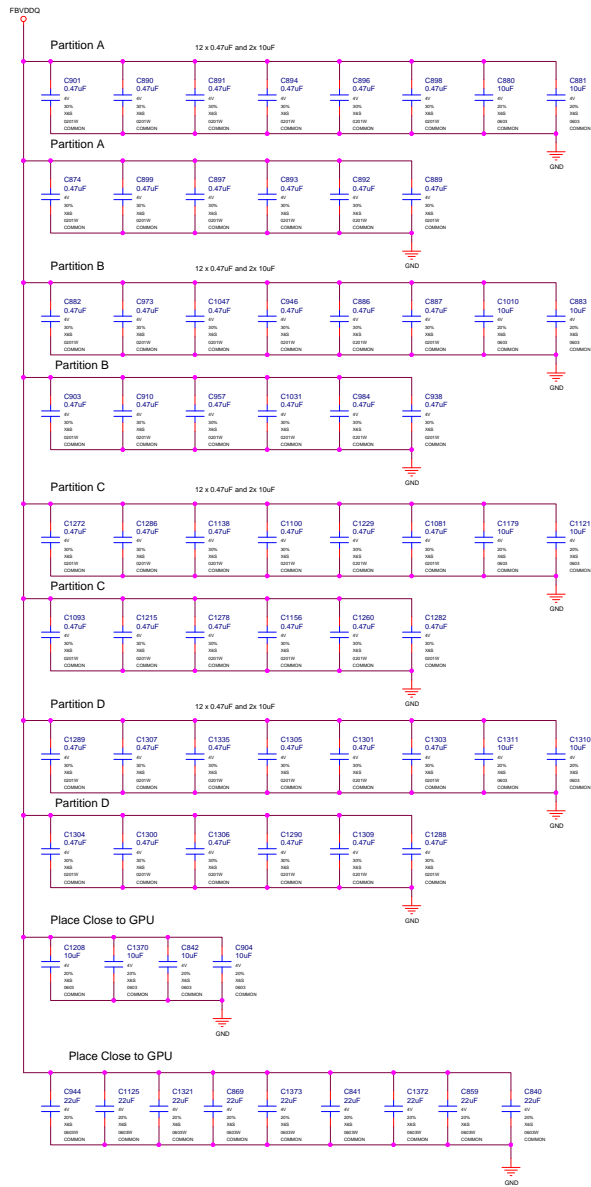


Title			
MEMORY: FBD[31:0]			
Size	Module Name:		Rev
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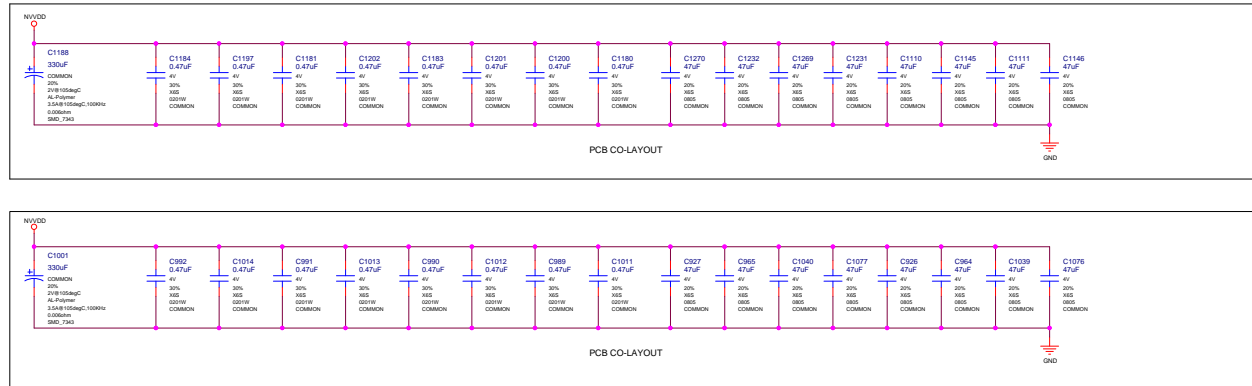




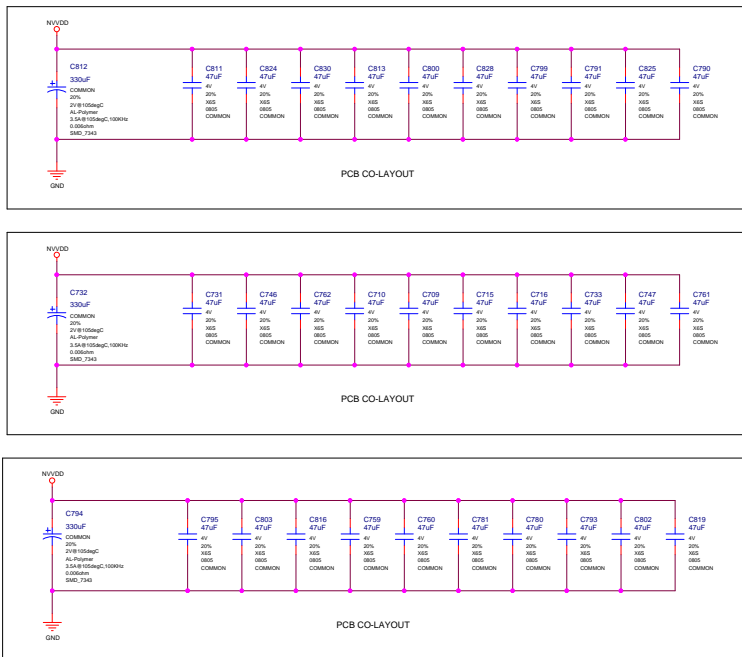
## FBVDDQ



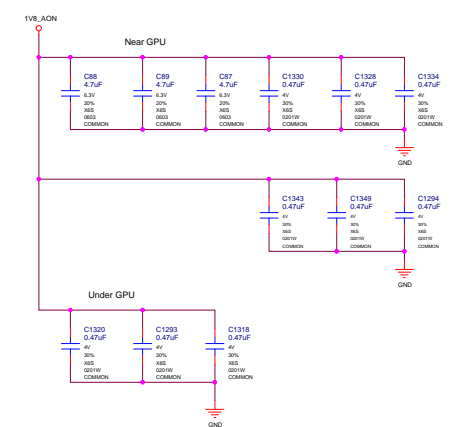
## Under GPU



## Near GPU



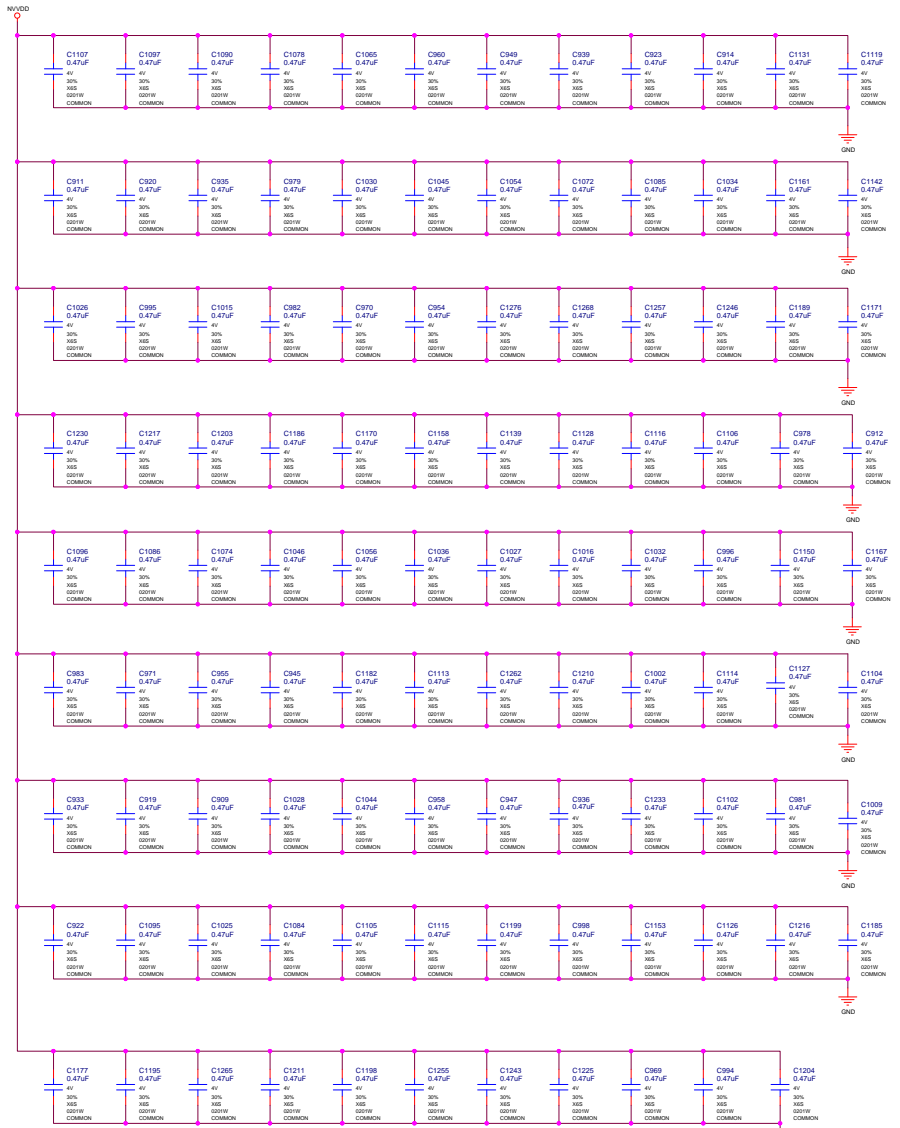
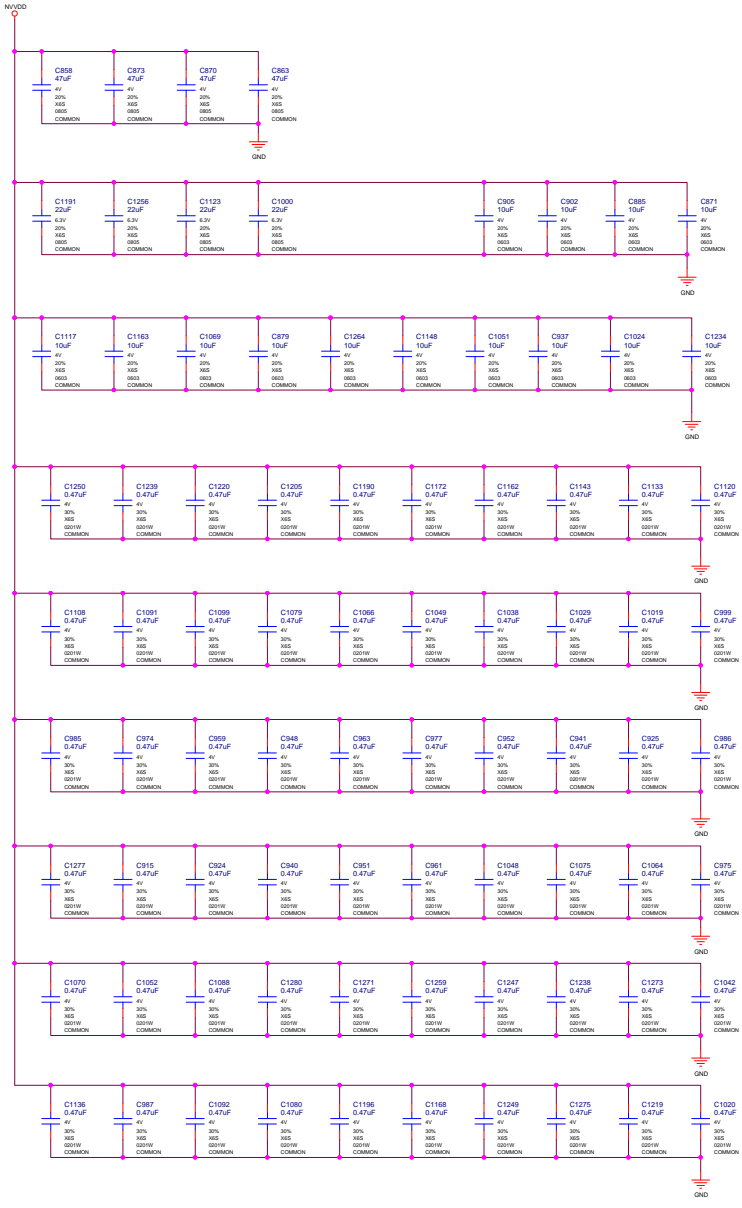
## 1V8\_AON




Title		
GPU Decoupling		
Size	Module Name:	Rev
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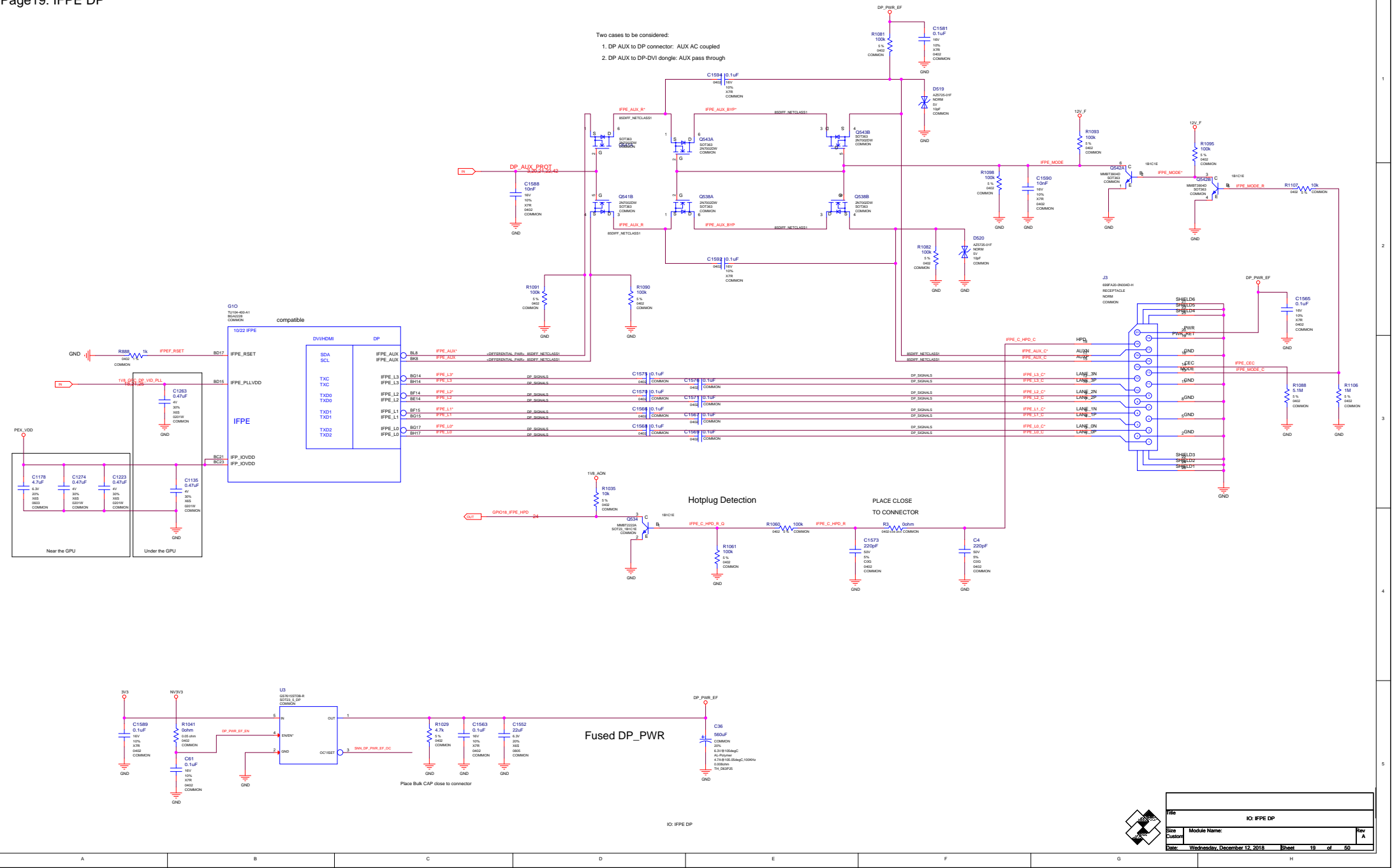
NVDD




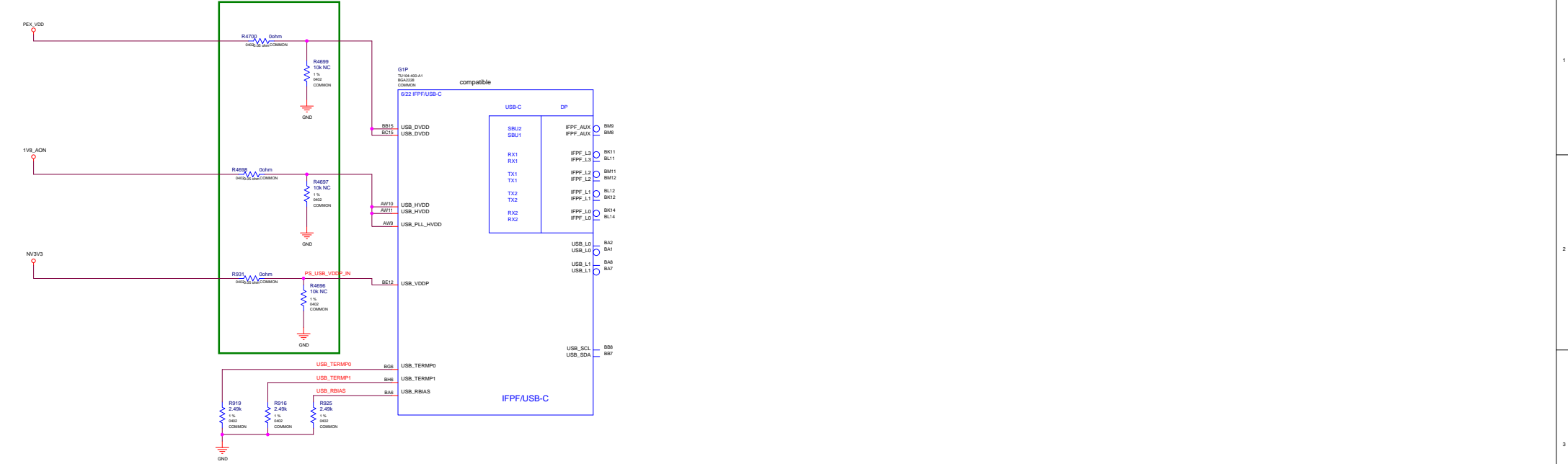
GPU Decoupling2

	File		GPU Decoupling2	
	Size	Module Name:	Rev A	
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	Title		
	IO: IFPE DP		
	Size	Module Name:	Rev
	Custom		A
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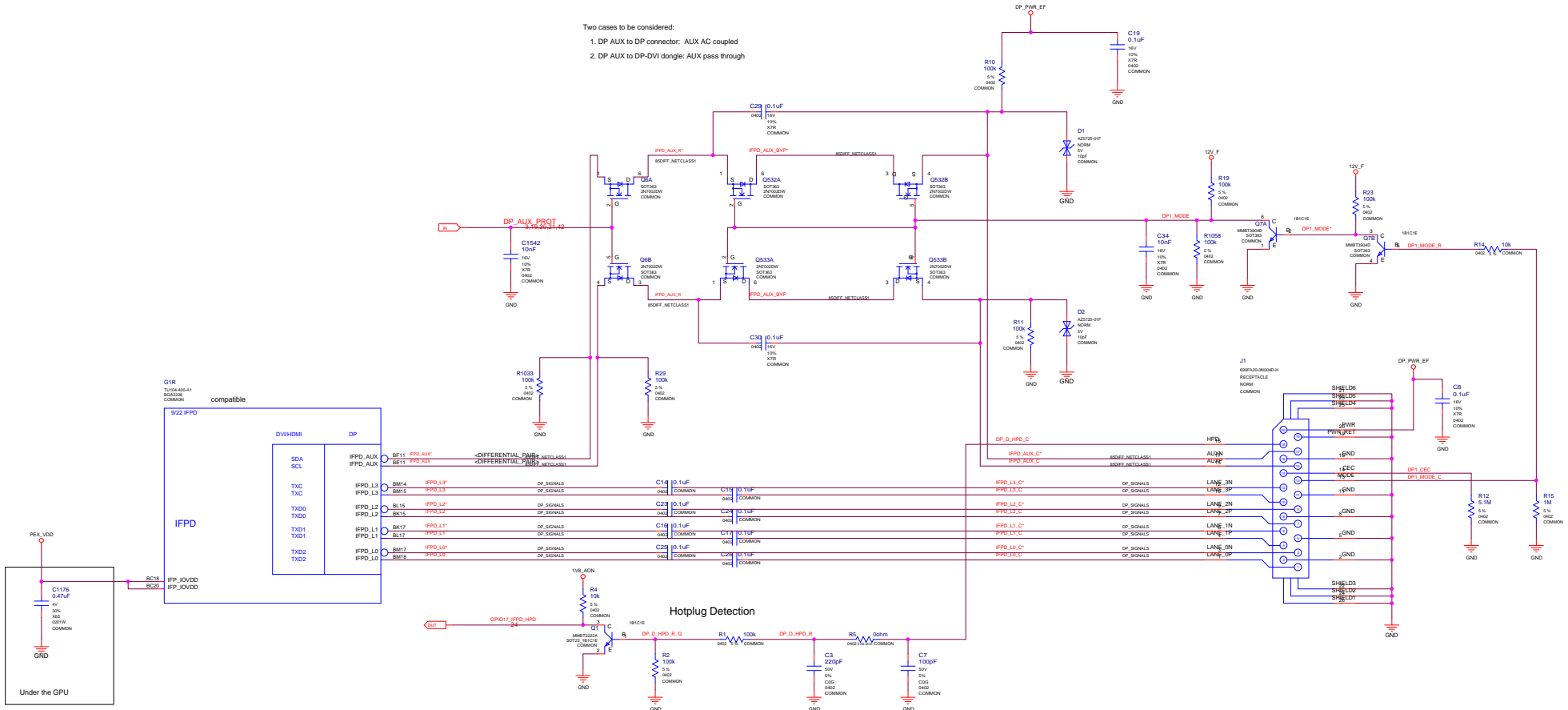


IO: IFPF USB-C

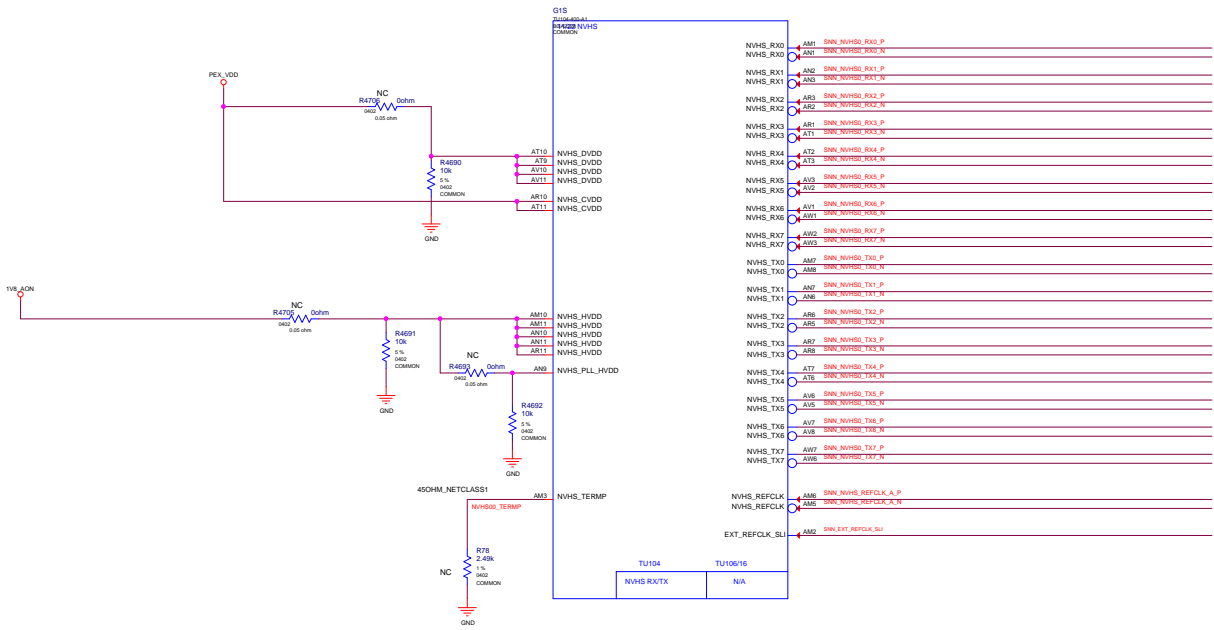
File		IO: IFPF USB-C	
Size	Custom	Module Name:	Rev A
Date:	Wednesday, December 12, 2018	Sheet	20 of 50



Two cases to be considered:  
1. DP AUX to DP connector: AUX AC coupled  
2. DP AUX to DP-DVI dongle: AUX pass through



File		IO: IFPD DP
Size	Module Name:	Rev A
Custom		
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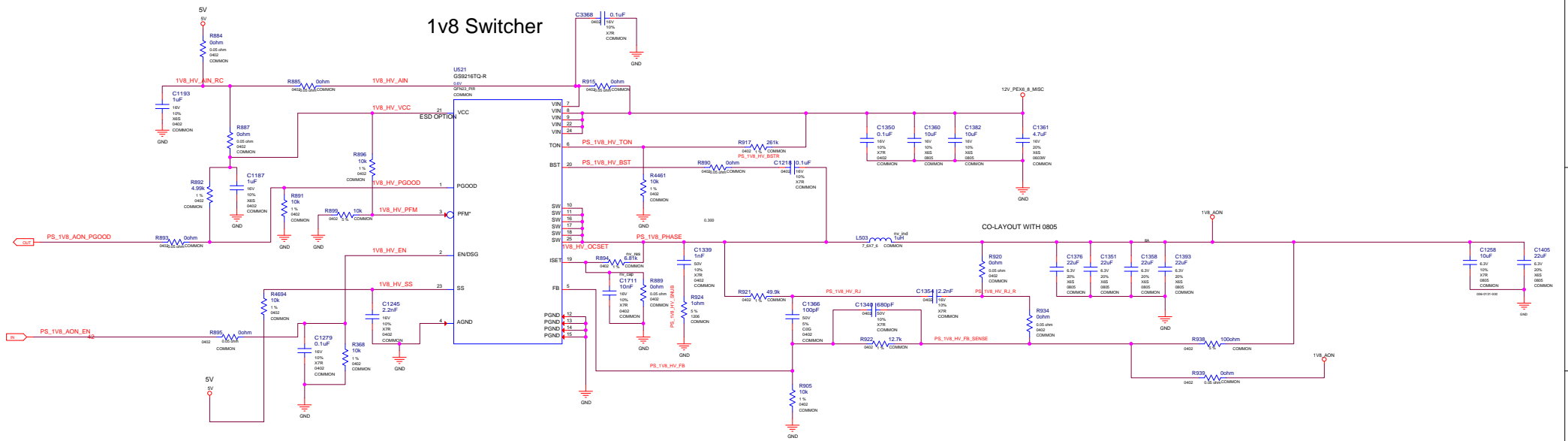
IO: NVHS Interface and Frame Lock

Title			
IO: NVHS Interface and Frame Lock			
Size	Module Name:		Rev
Custom			A
Date:	Wednesday, December 12, 2018	Sheet	23 of 50





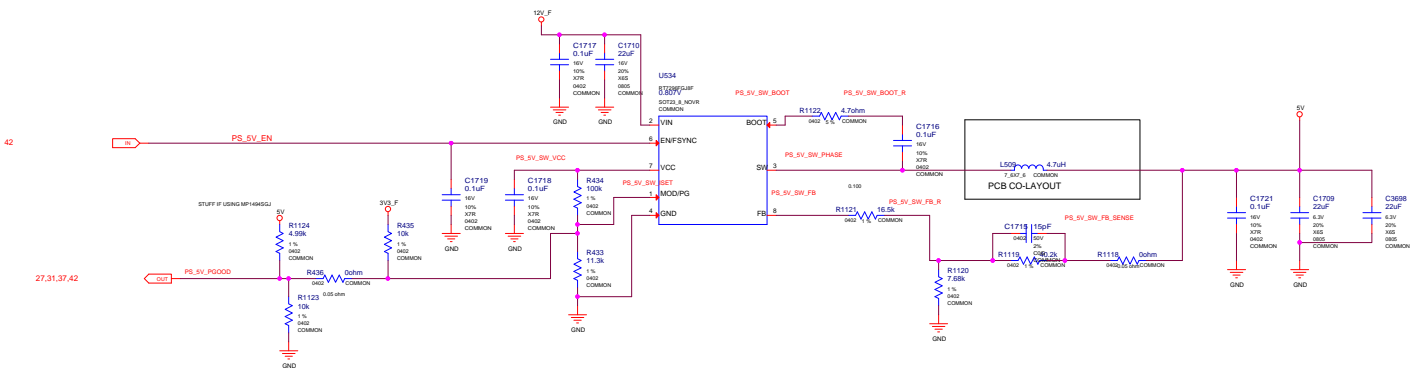




PS: 1V8\_PLL, 1V8\_AON



Title			
PS: 1V8_PLL, 1V8_AON			
Size	Module Name:		Rev
Custom			A
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File		PS: 5V
Size	Module Name:	Rev A
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## PEX Switcher



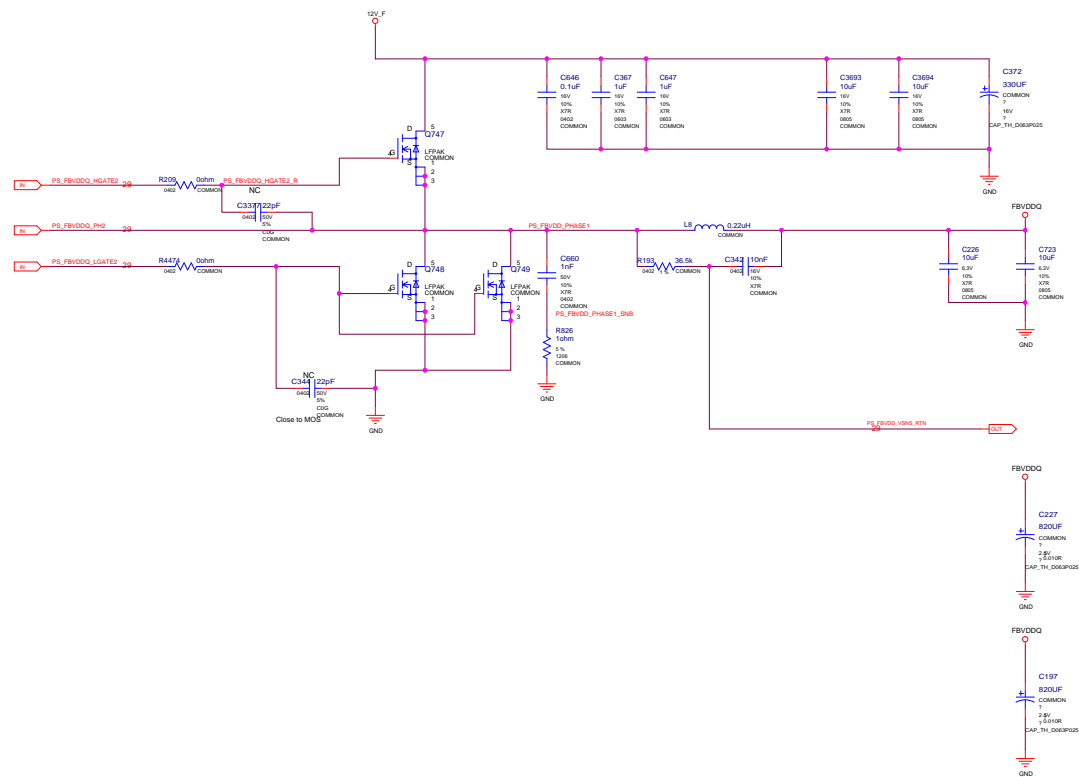
PS: PEXVDD



Title			
PS: PEXVDD			
Size	Module Name:		Rev
Customr			A
Date:	Wednesday, December 12, 2018	Sheet	28 of 50



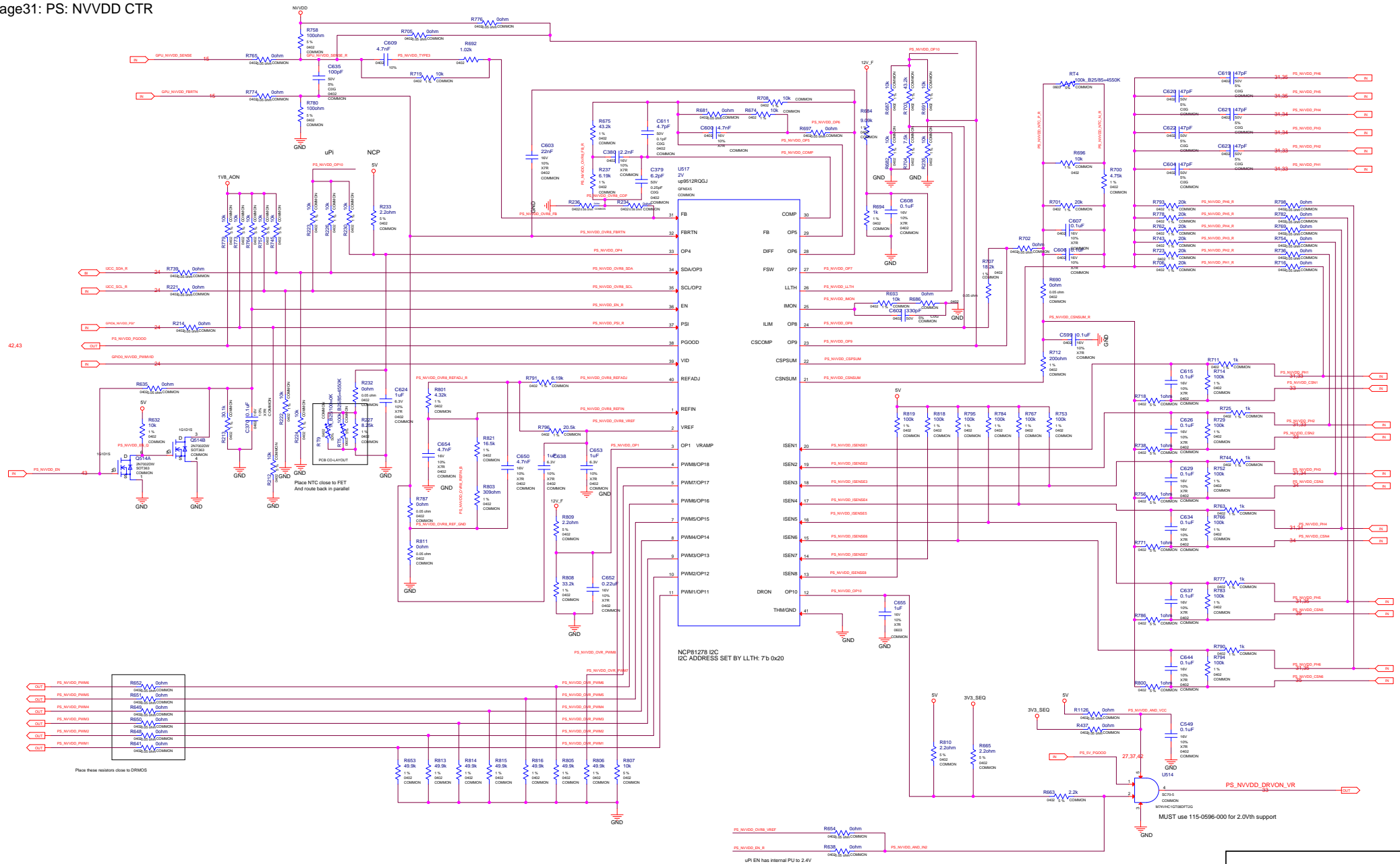
Title			PS: FBVDDQ		
Size Custom	Module Name:				Rev A
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PS: FBVDDQ PH2



Title		
PS: FBVDDQ PH2		
Size	Module Name:	Rev
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PS: NVVDD Controller



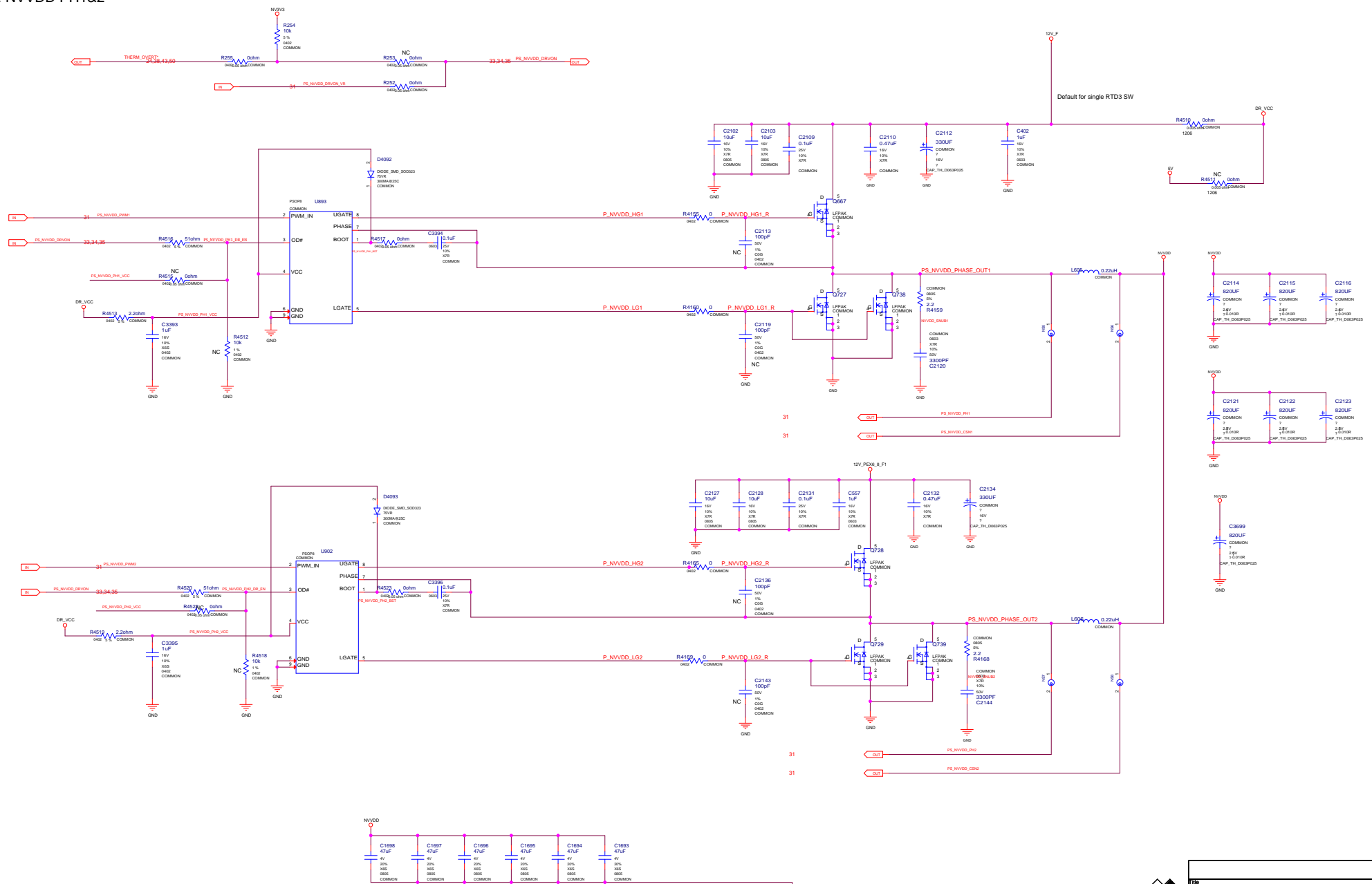
Title		PS: NVDD Controller	
Size	Module Name:	Rev A	
Custom			
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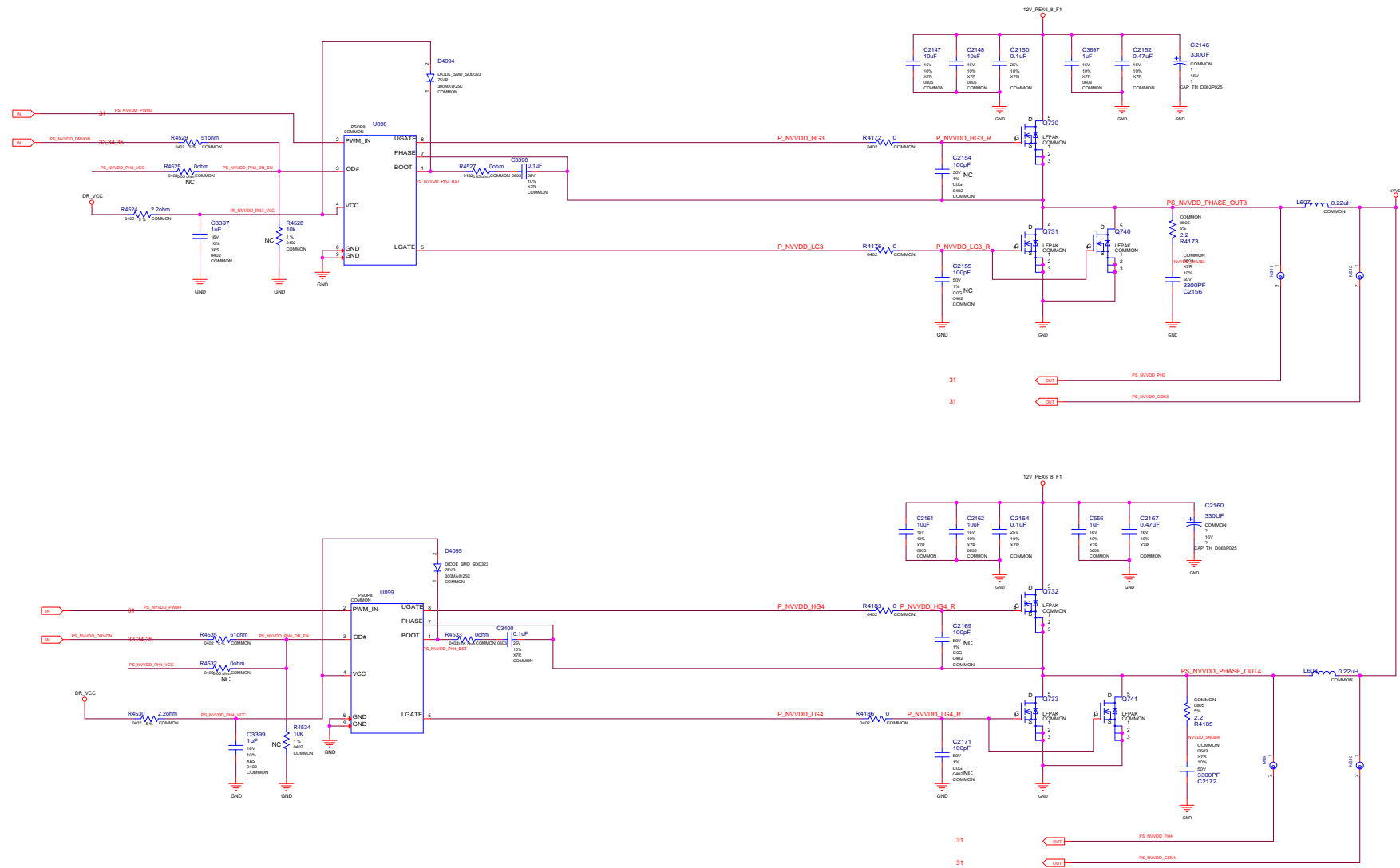
PS: NVVDD Controller OVR3i



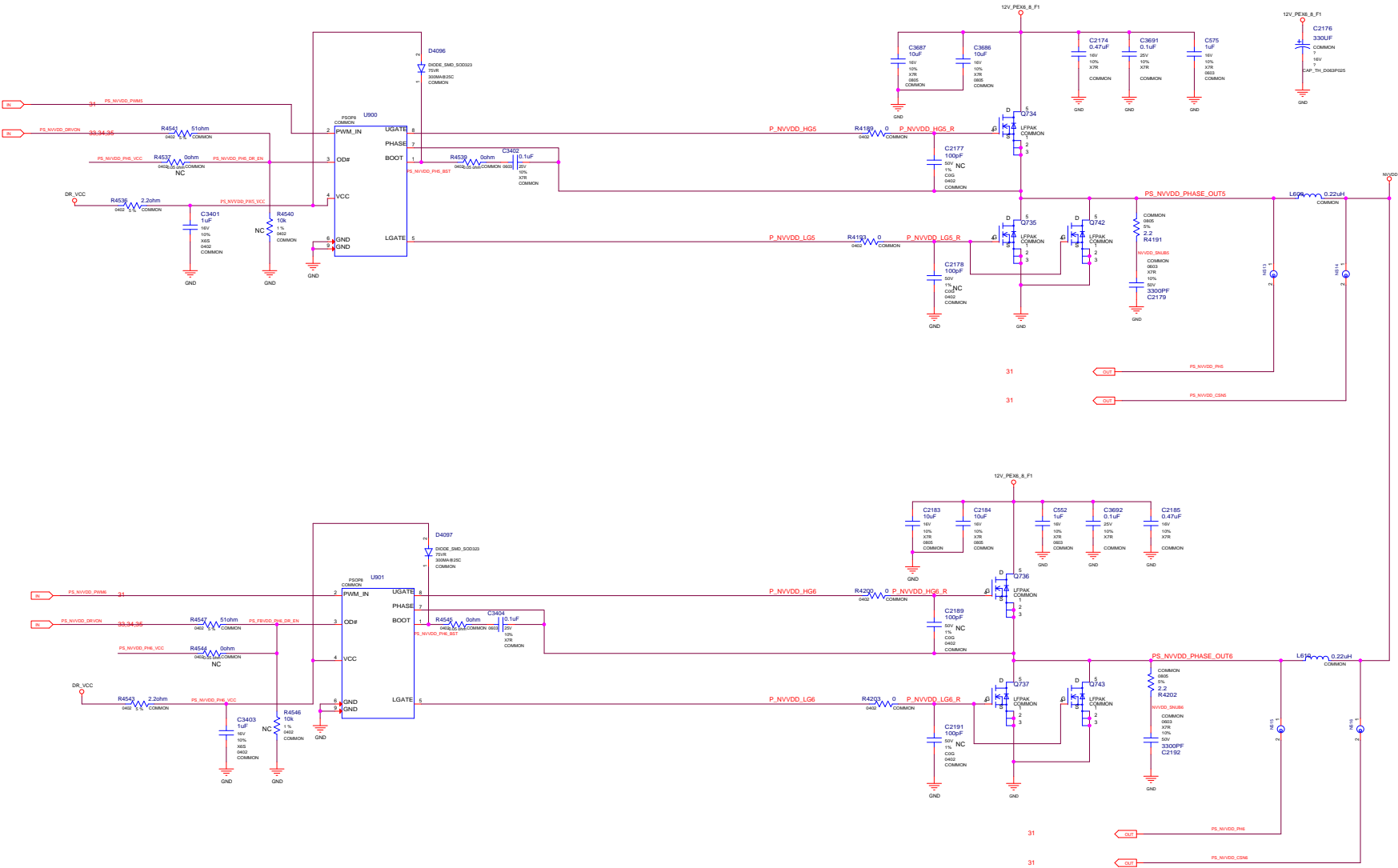
Title		
PS: NVVDD Controller OVR3i		
Size	Module Name:	Rev
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Title			PS: NVVDD Phase 3,4
Size	Custom	Module Name:	
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		Rev	A



PS: NVVDD Phase 5,6

Title		PS: NVVDD Phase 5,6	
Size	Custom	Module Name:	Rev A
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Title		
PS: Input Power Balancing Switcher		
Size	Module Name:	Rev
Custom		A
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Title		
PS: Type-C BuckBoost		
Size	Module Name:	Rev
Custom		A
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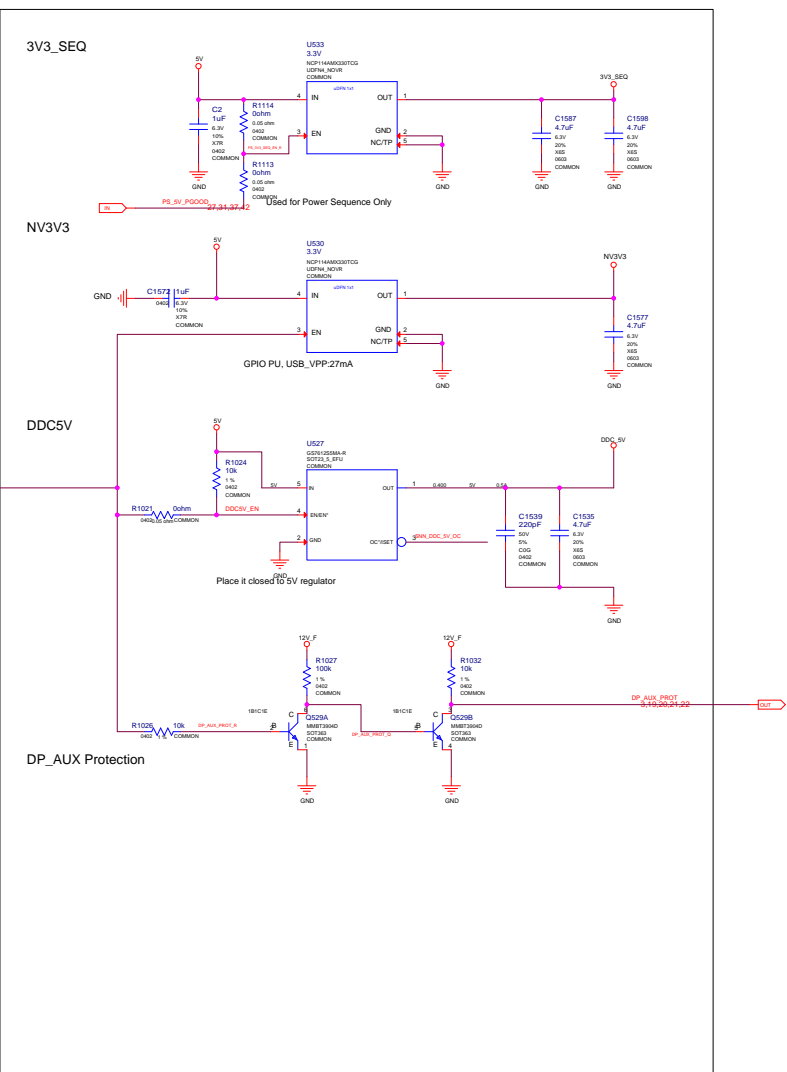
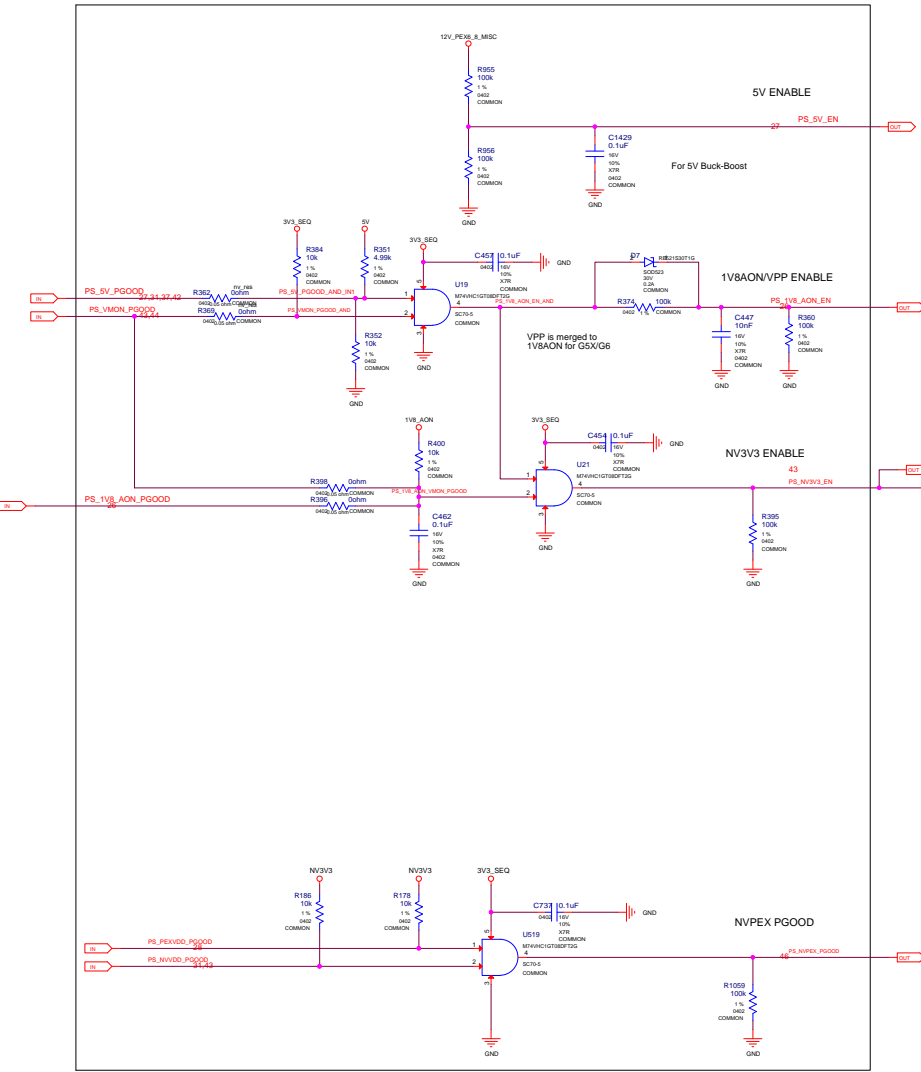


Title		
PD PPC		
Size	Module Name:	Rev
Custom		A
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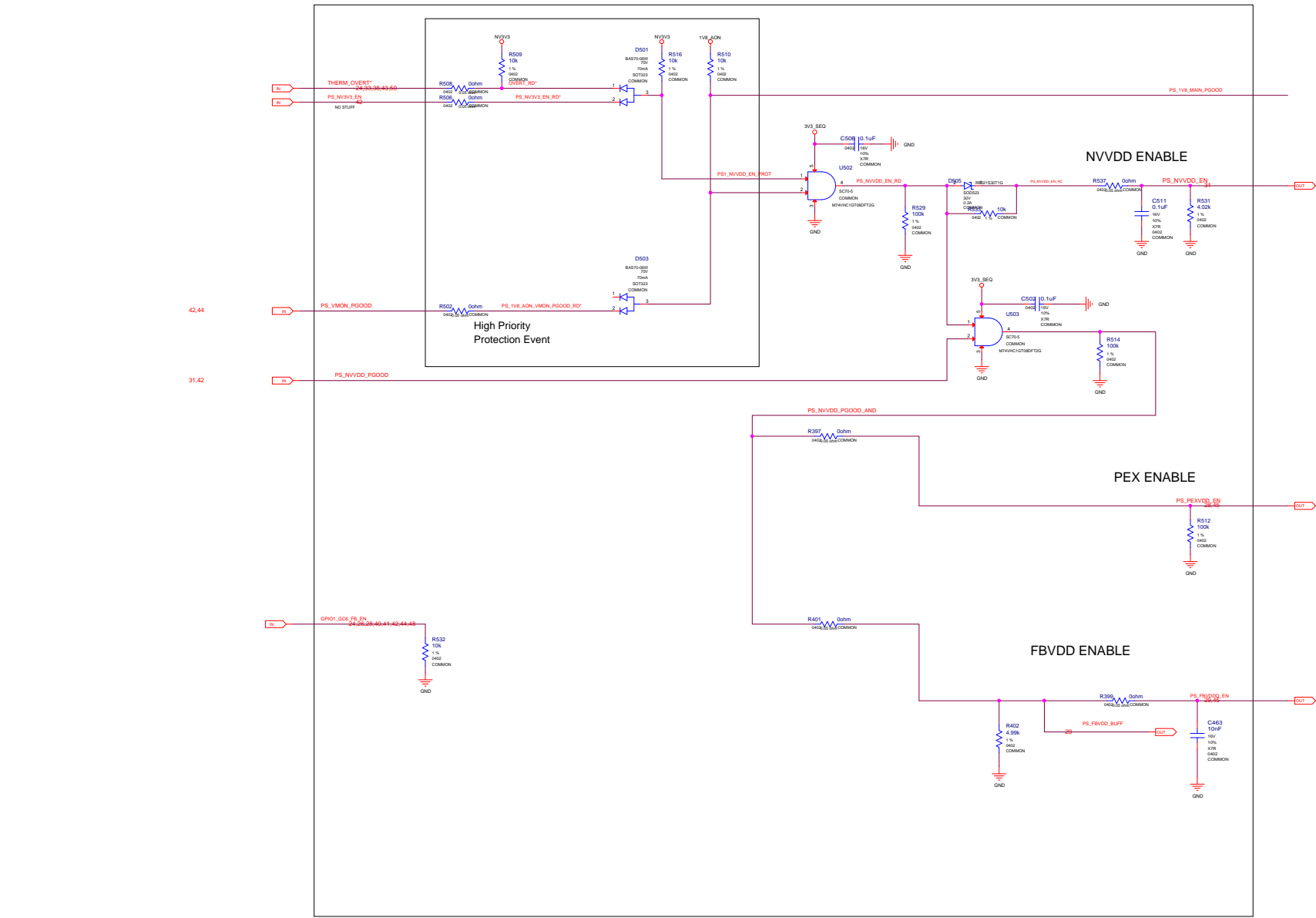


File		
PS: 12V & 3V3_A SWITCHER		
Size	Module Name:	Rev
Custom		A
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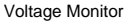
SEQ: 5V, 1V8, NV3V3 ENABLE

Title			SEQ: 5V, 1V8, NV3V3 ENABLE
Size	Module Name:	Rev	A
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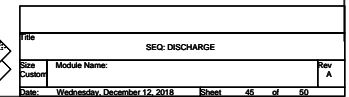
SEQ: NV, PEX, FB ENABLE

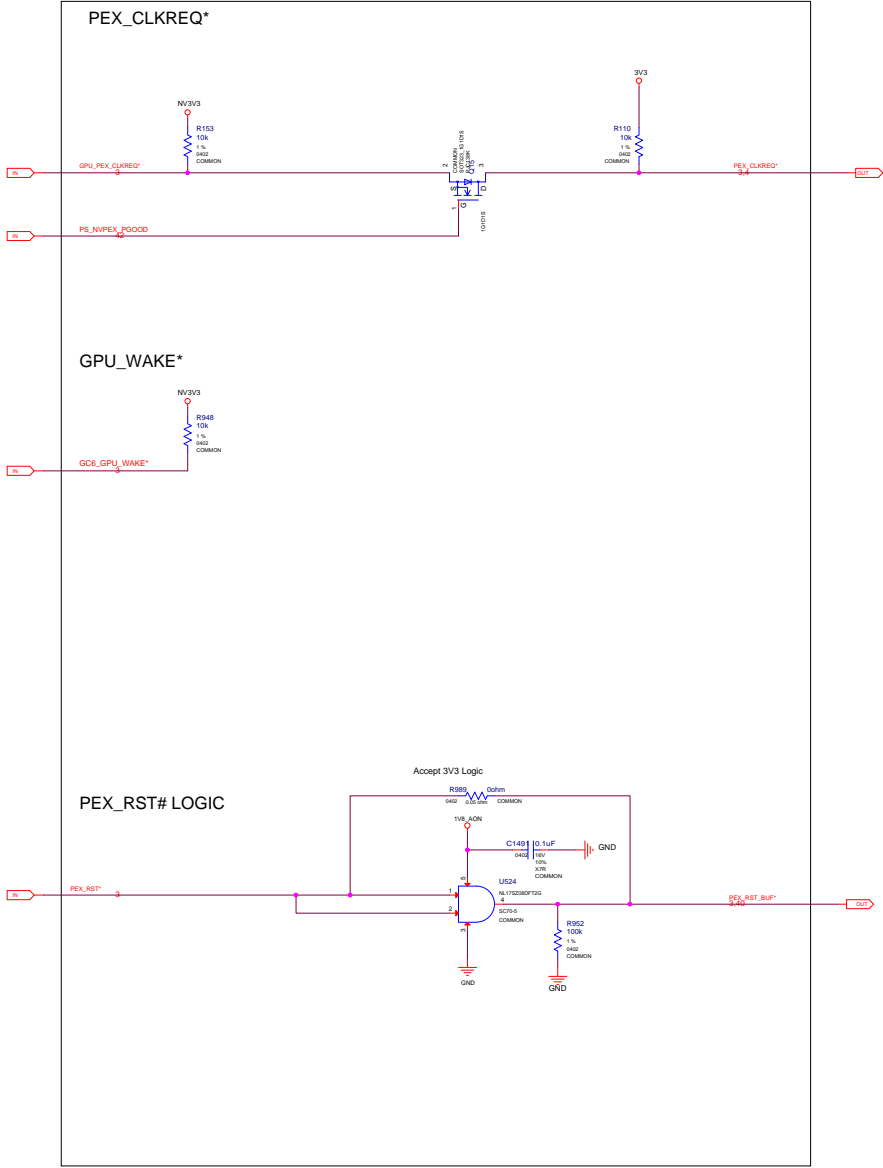
Title		SEQ: NV, PEX, FB ENABLE
Size	Module Name:	Rev A
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Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
CS_VMON_PGOOD	OPEN-DRAIN	Floating(f) once both 3V3 and 12V reach Vth
GS6_FB_EN	INPUT	Indicator for RTD3/G06 residence. Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(PVU) or Pre-filter(SKIP)
PS_PF_BSKQ	INPUT	From INA3221(PVU) or Pre-filter(BS_OK)

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A





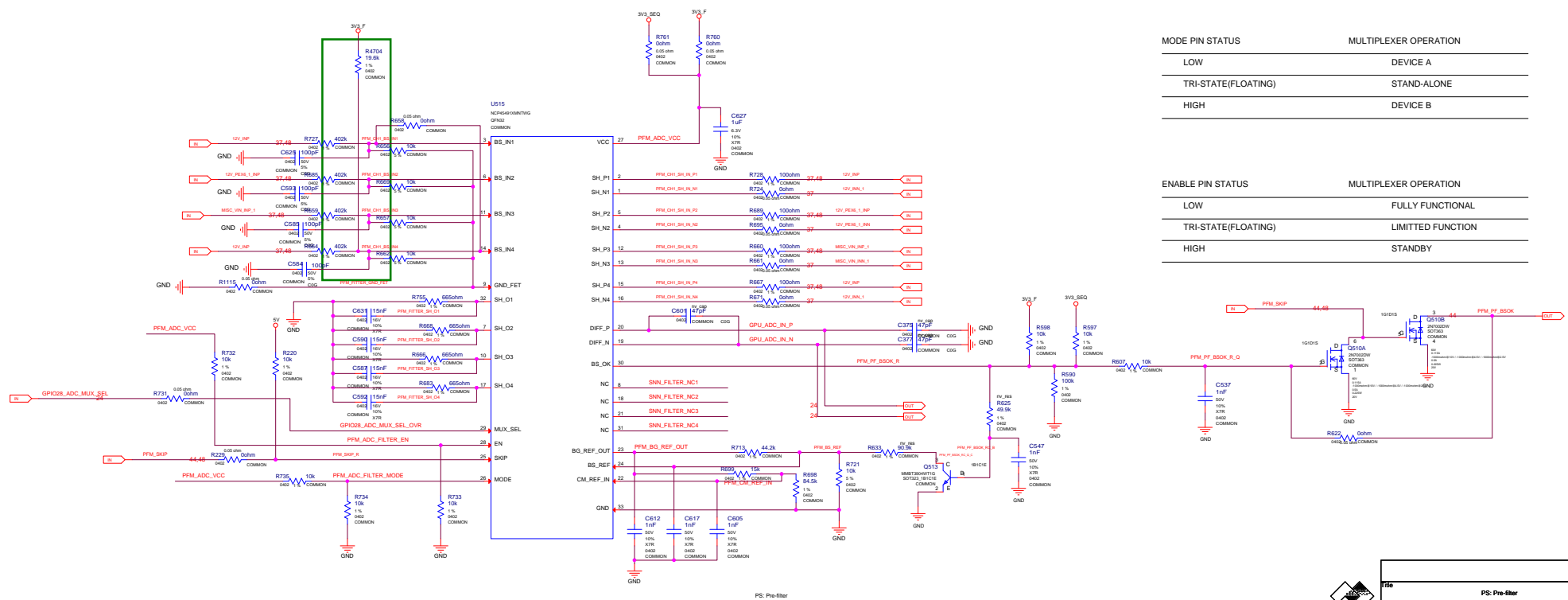
SEQ MISC



Title		SEQ MISC
Size	Module Name:	Rev A
Custom		
Date: Wednesday, December 12, 2018		Sheet 46 of 50



A	B	C	D	E	F	G	H
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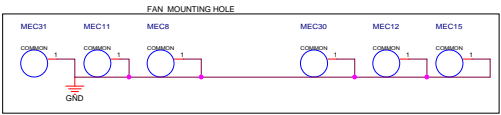
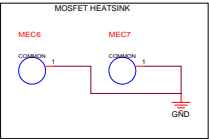
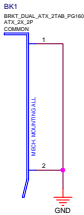


MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY



Brackets:



BACK STIFFENER:



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PTC

Title	
PTC	
Size	Module Name:
Custom	
Date:	Wednesday, December 12, 2018
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Rev	A