PG165-A00

TU116 6GB GDDR5, 192b, X32
DVI-D + DP + HDMI

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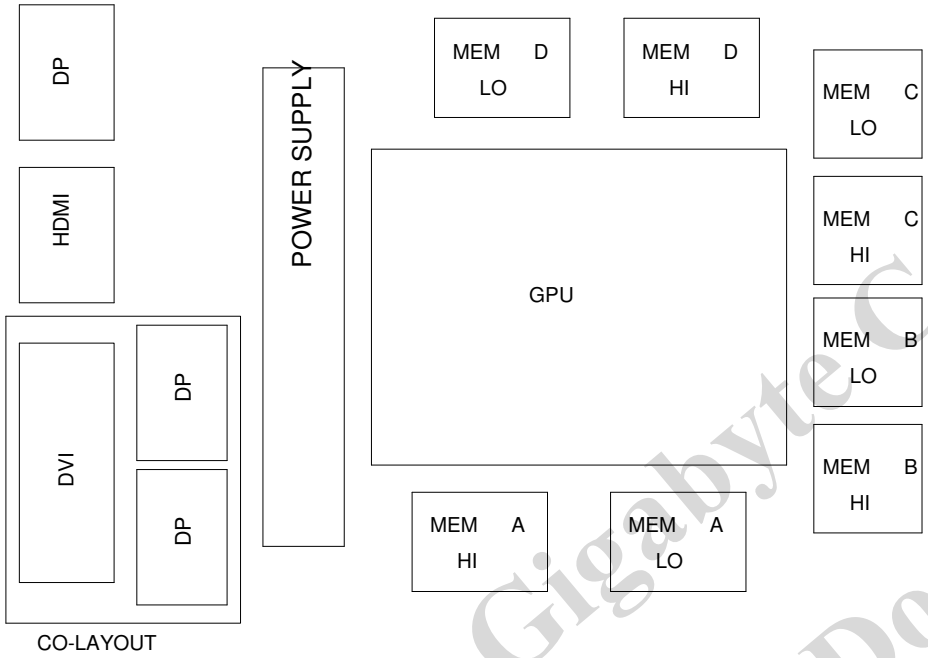

Power Supply:

- Power Supply NVVDD-PH6
- Power Supply NVVDD-PH5
- Power Supply NVVDD-PH4
- Power Supply NVVDD-PH3
- Power Supply NVVDD-PH2
- Power Supply NVVDD-PH1
- Power Supply FBVDDQ-PH2
- Power Supply FBVDDQ-PH1
- Power Supply 5V
- PEX_VDD
- 1V8
- Fan
- DP_PWR

EXT_12V 8PIN PWR

PEX_12V Finger

PEX_3V3 FINGER

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Block Diagram

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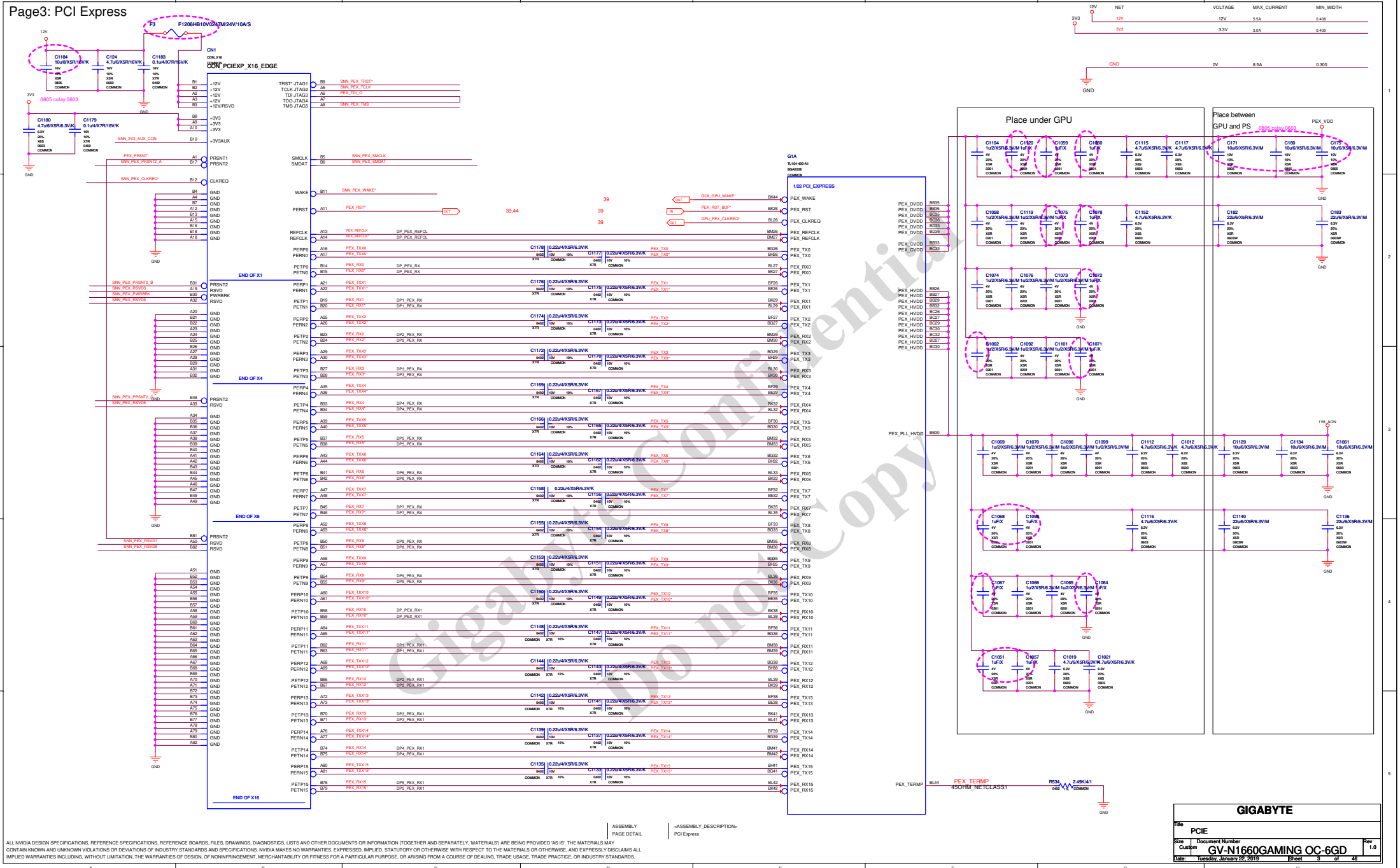

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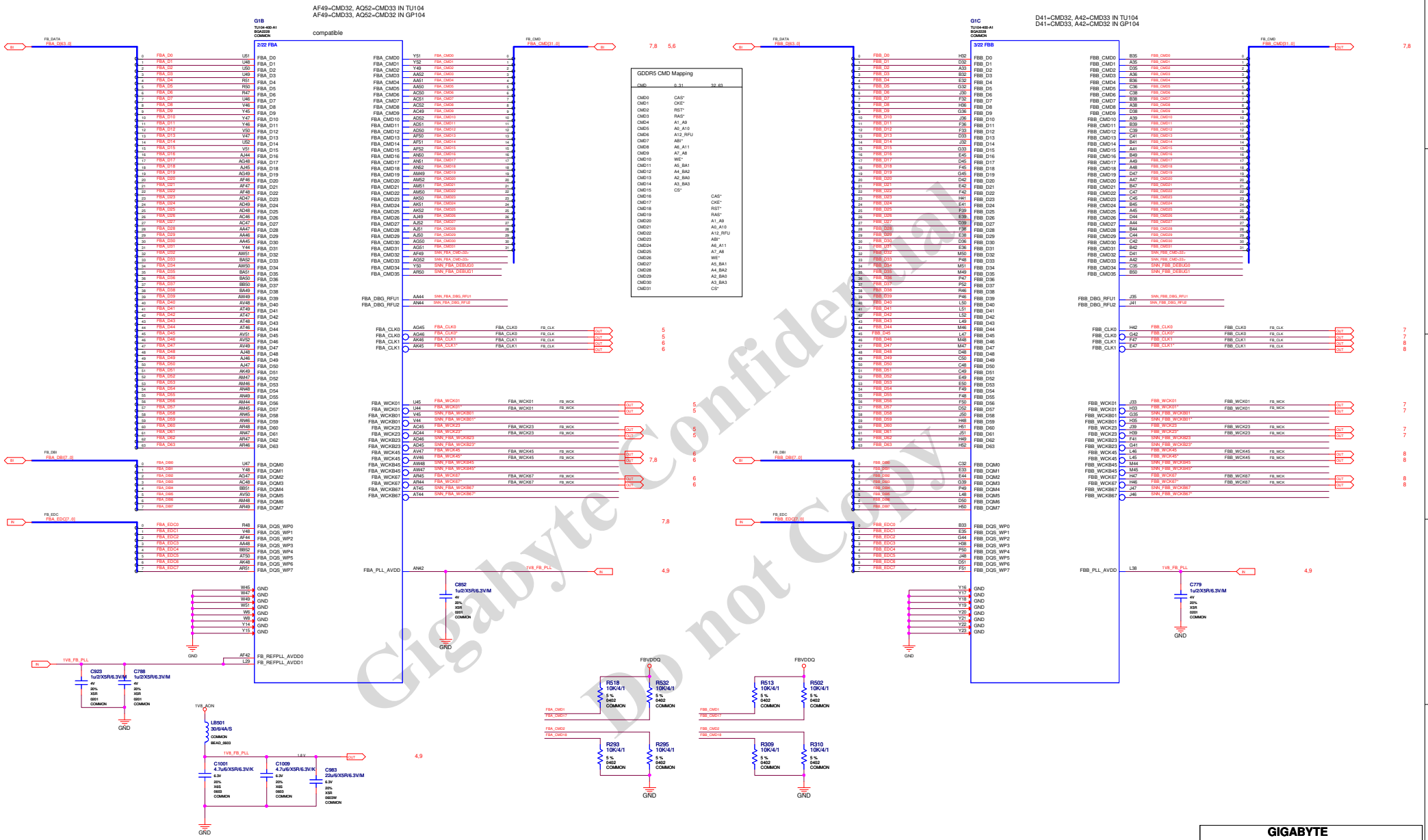
Page4: MEMORY: GPU Partition A/B



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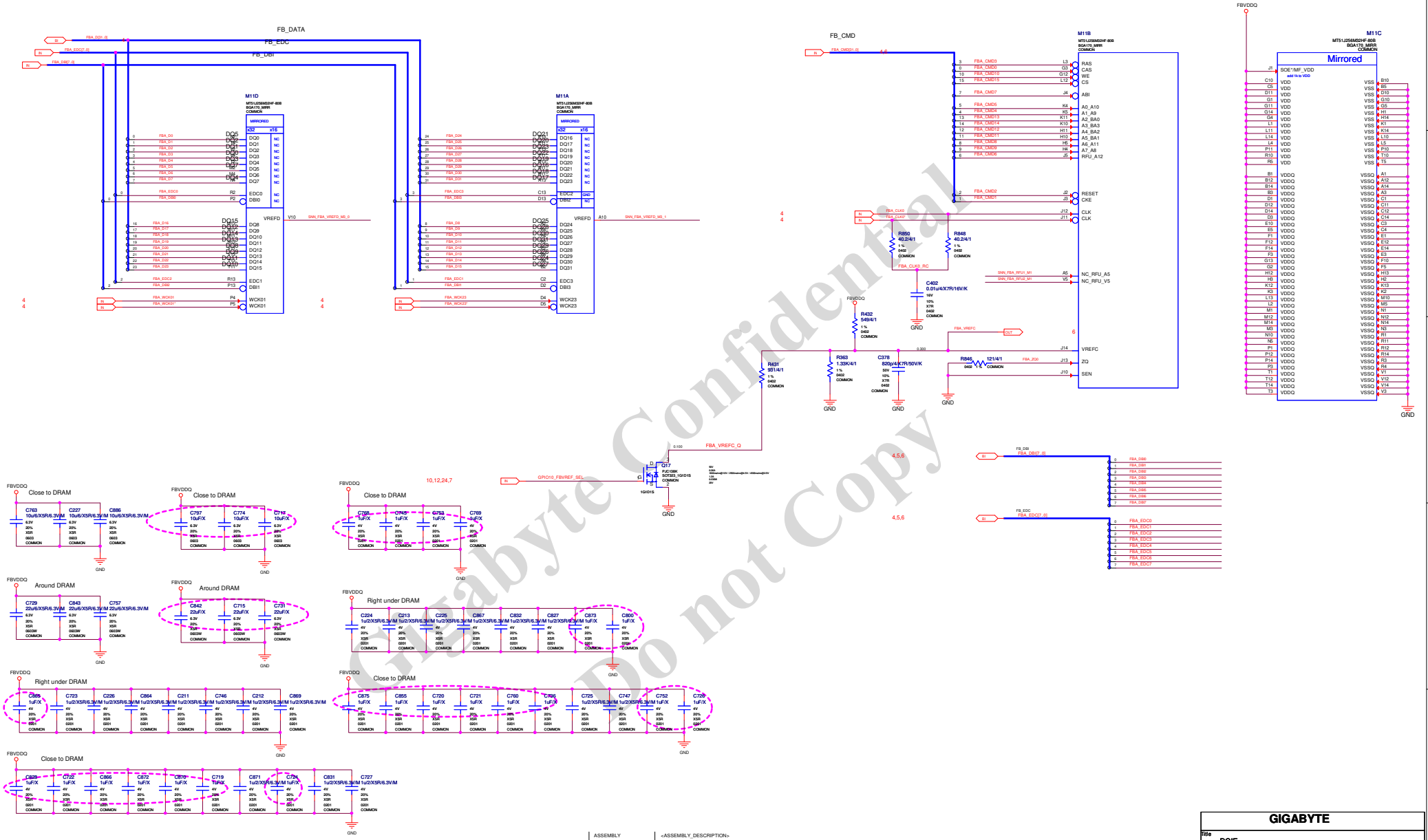

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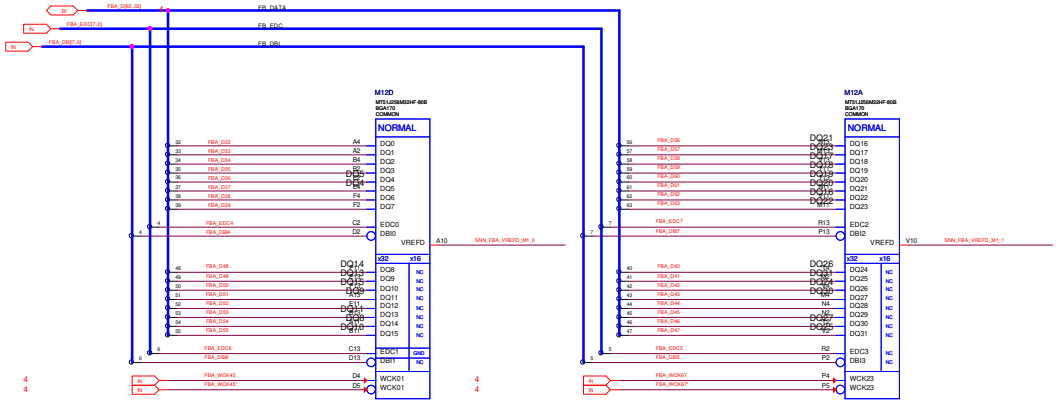

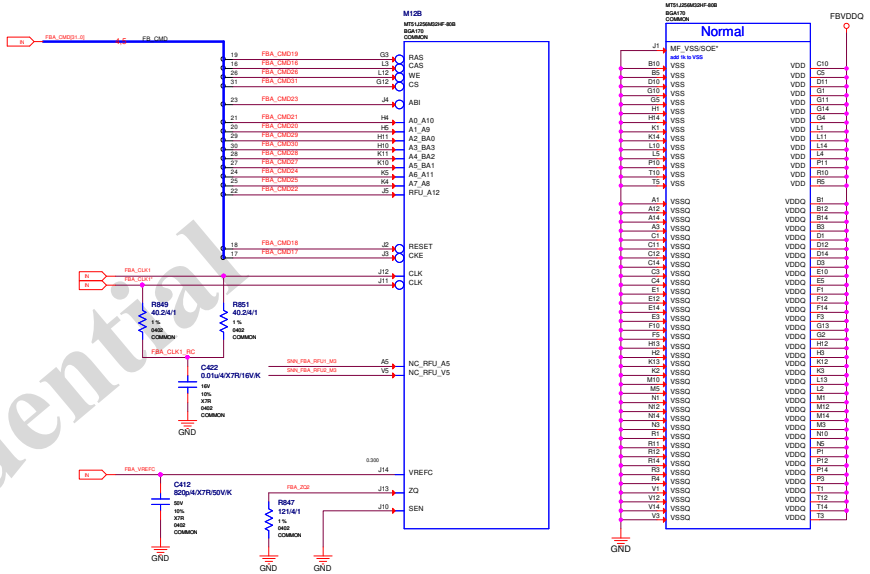

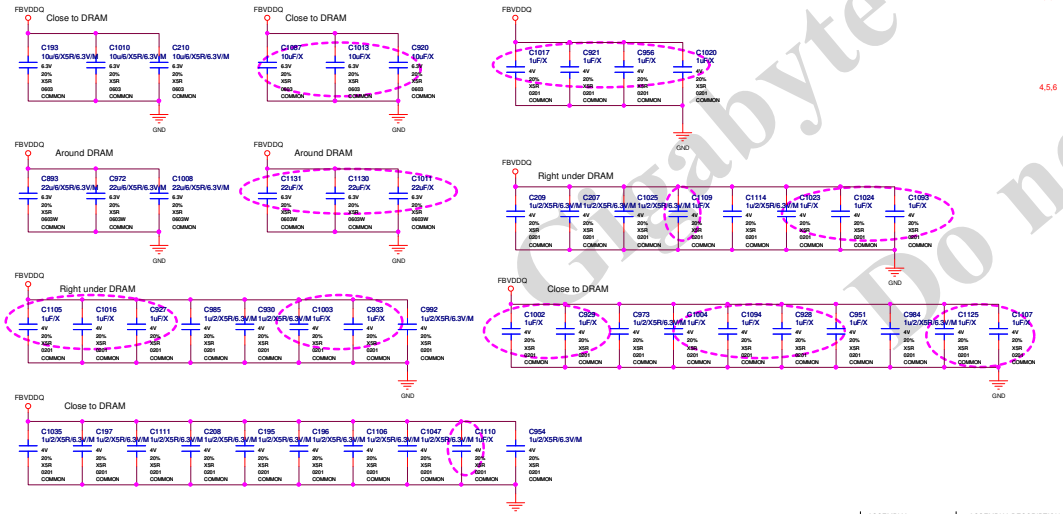

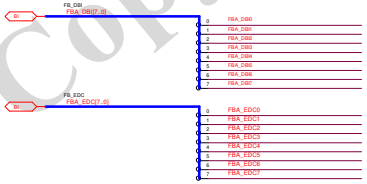

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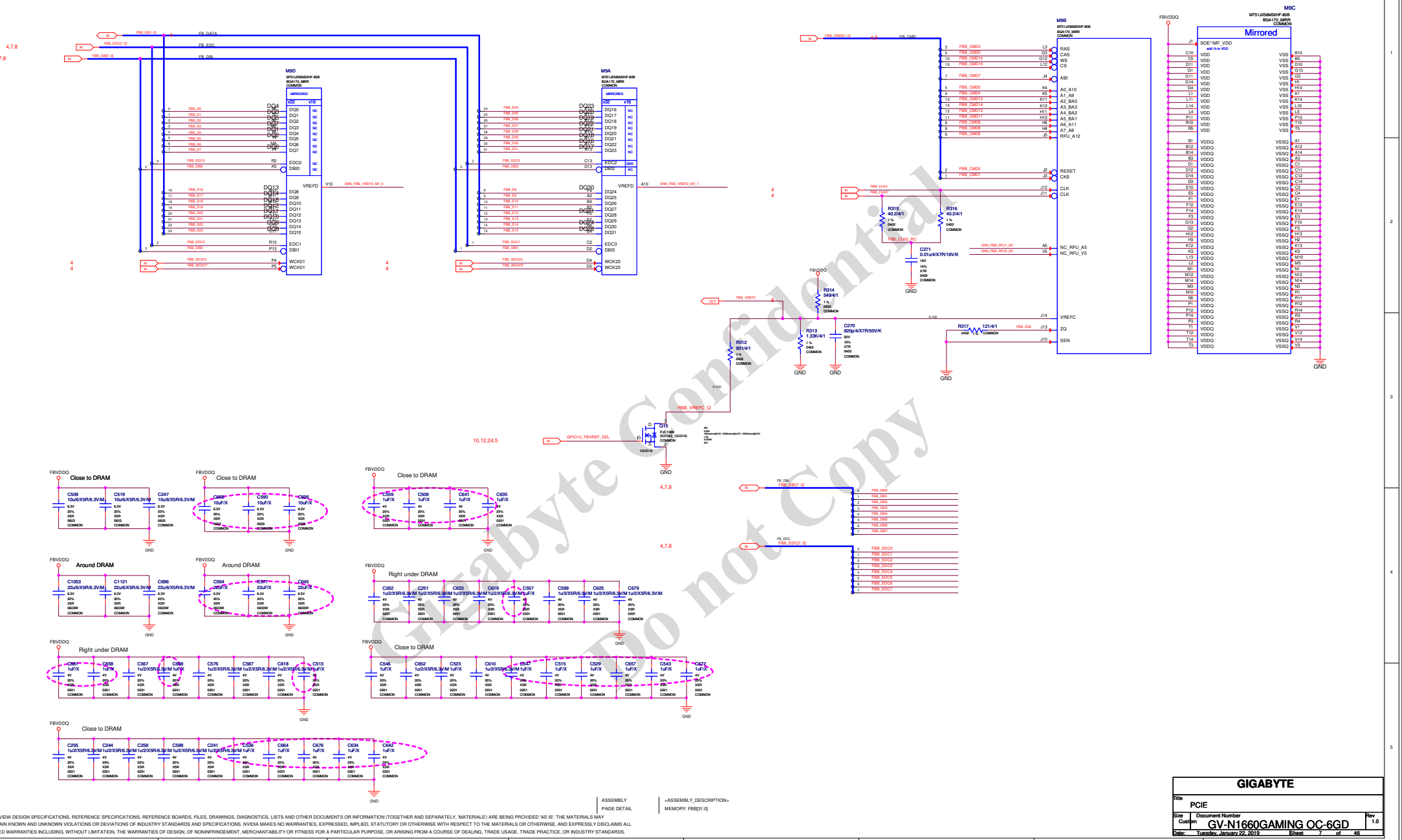
Page7: MEMORY: FBB Partition 31..0



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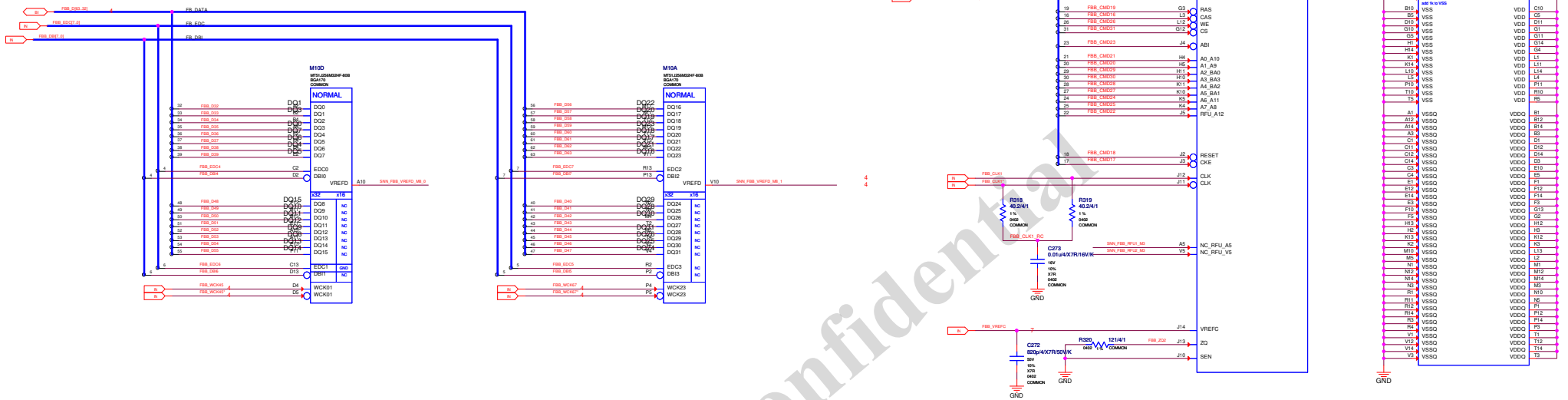

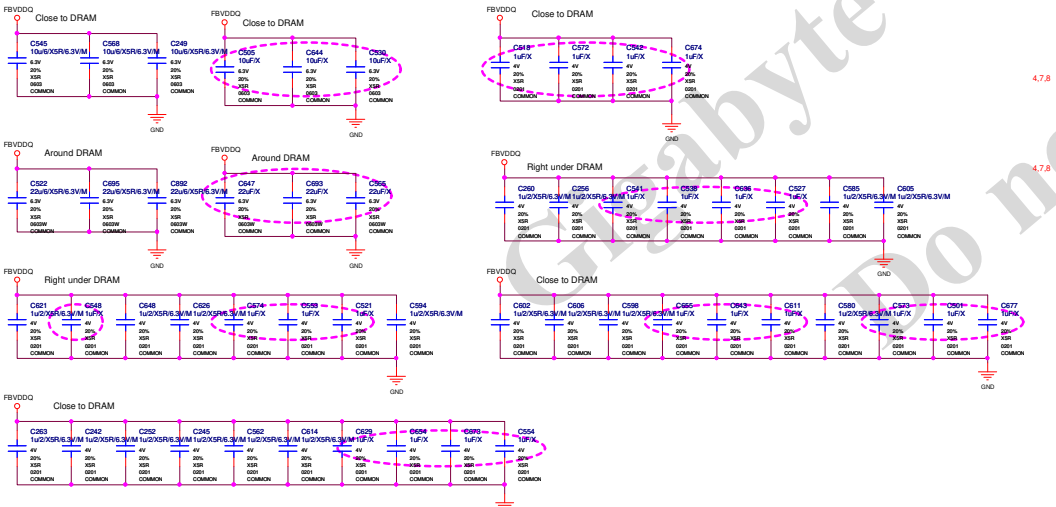

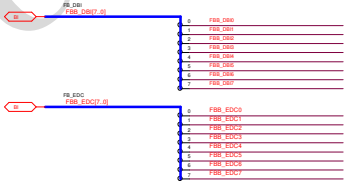

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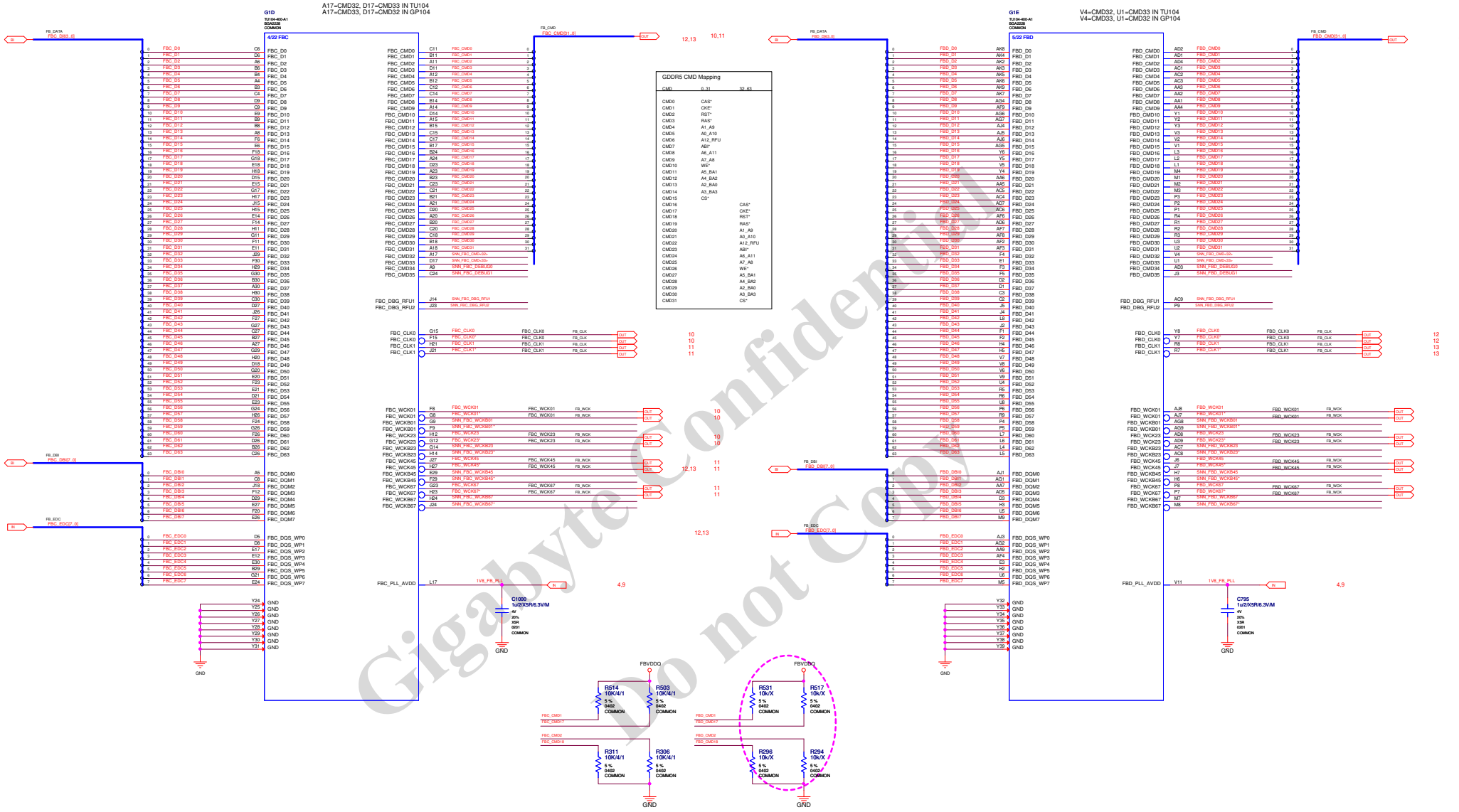

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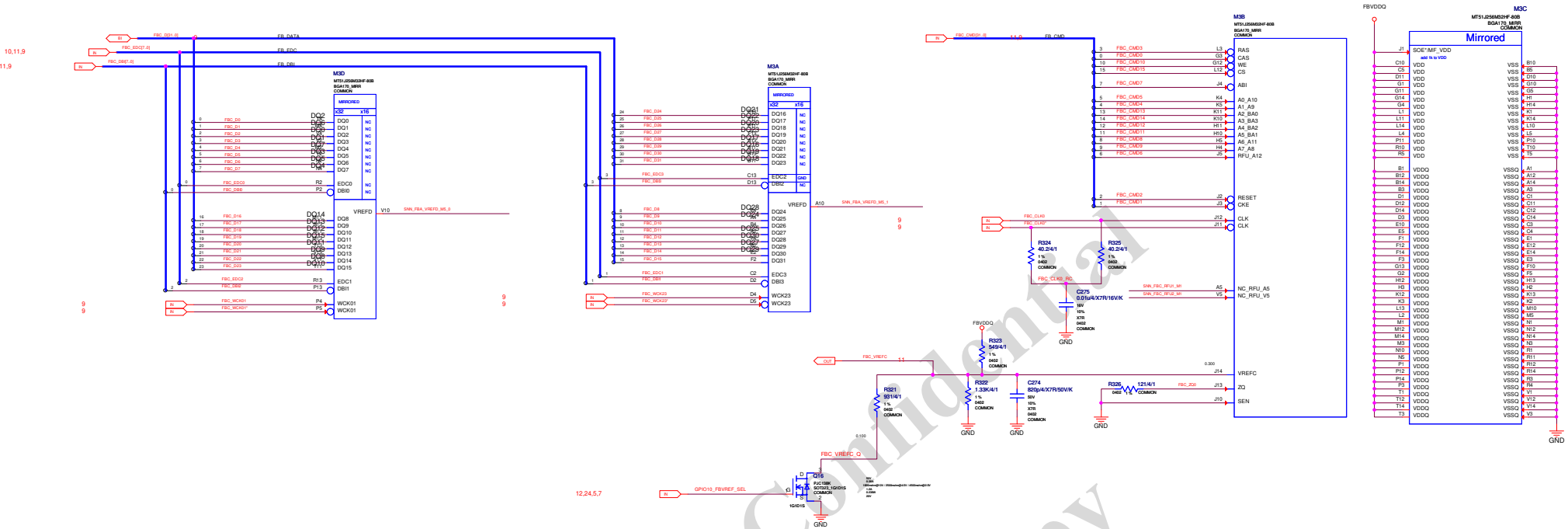

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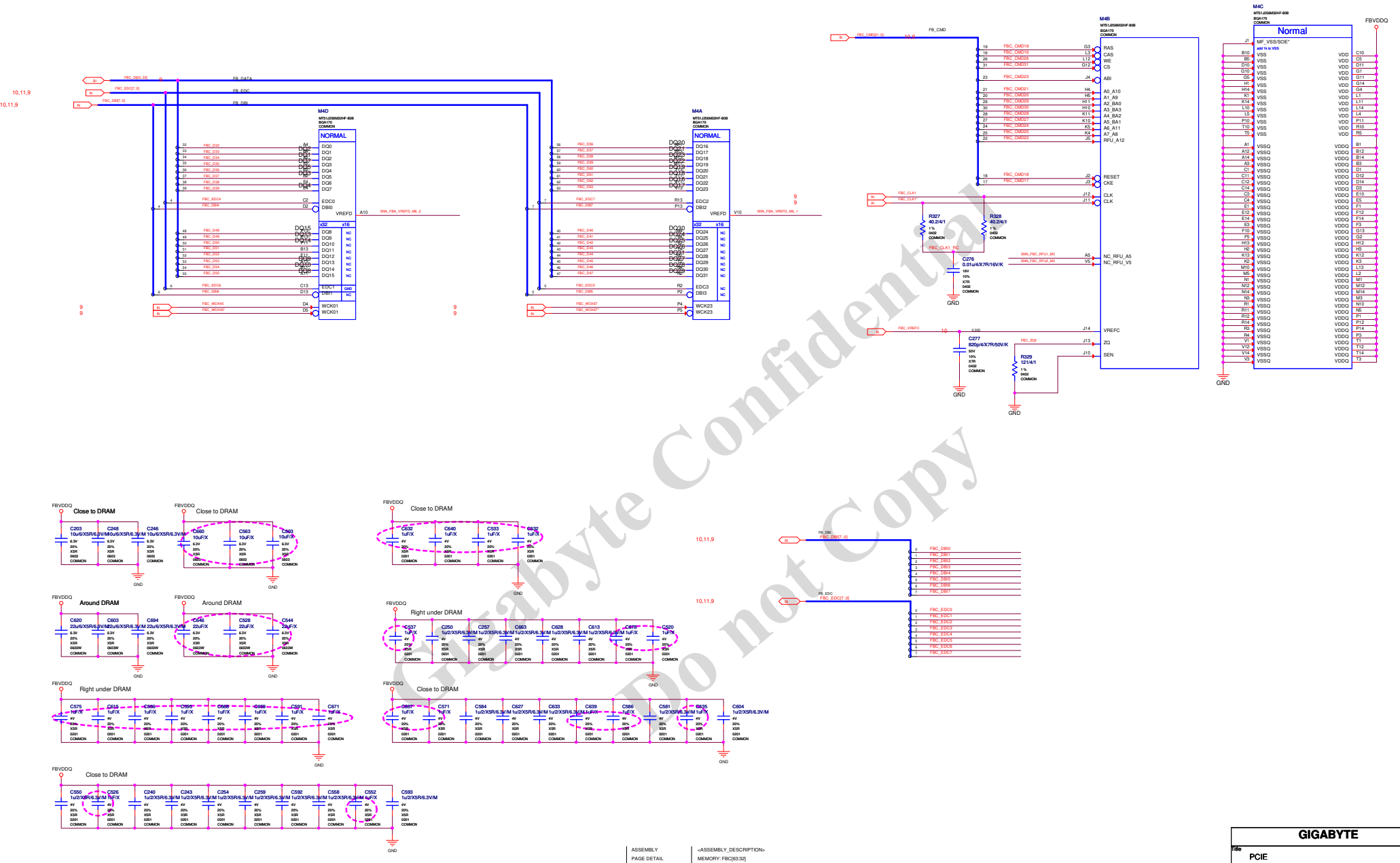

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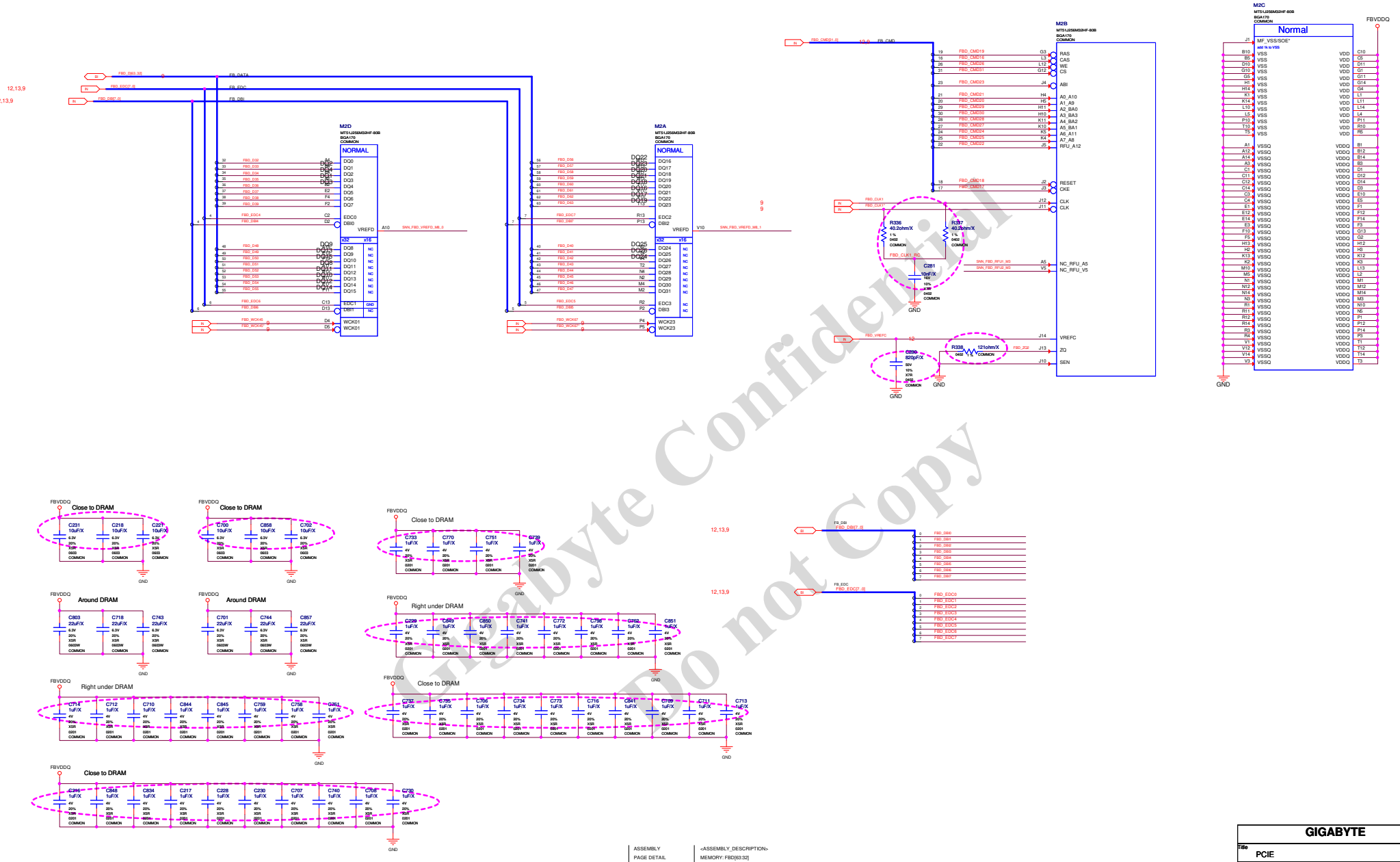

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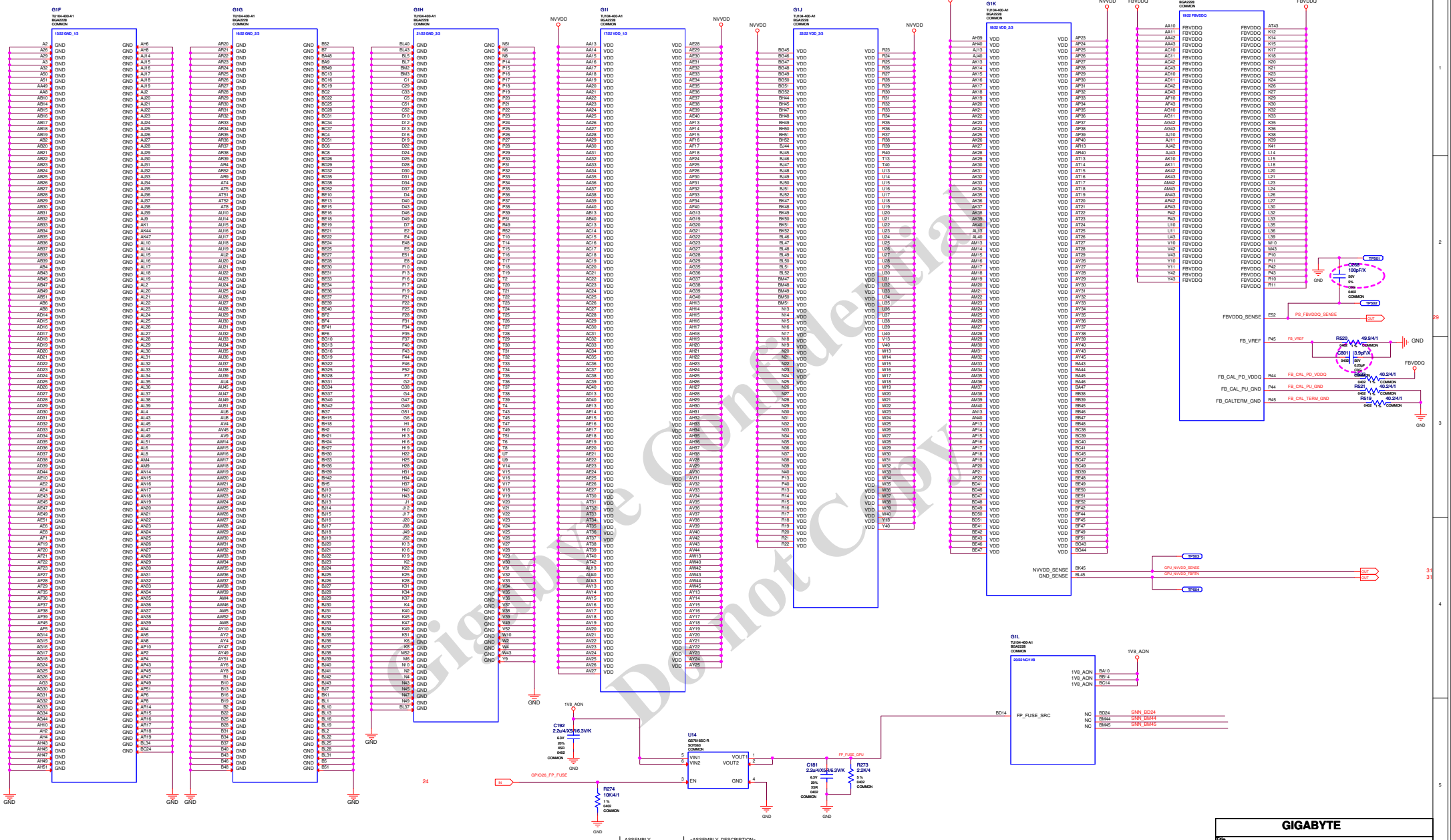
Page14: GPU PWR and GND



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Page15: GPU DECOUPLING 1

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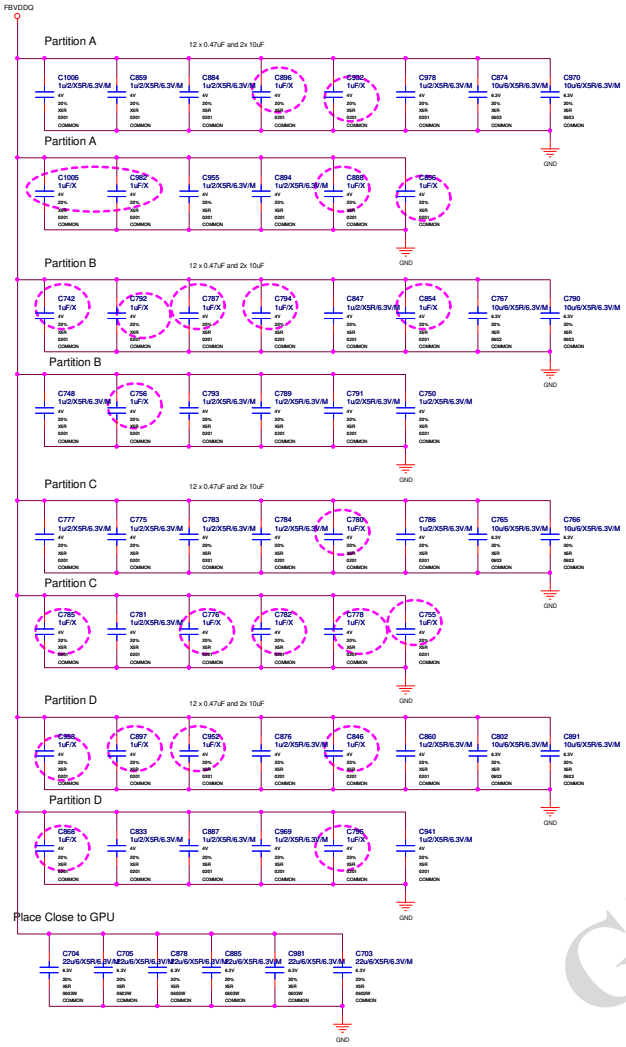

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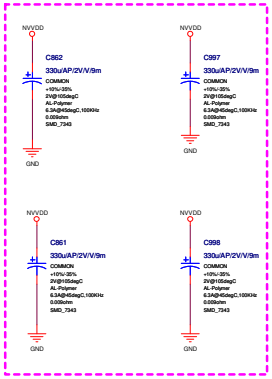

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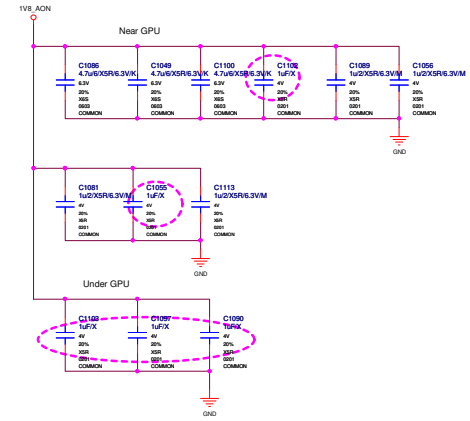

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PAGE DETAIL | GPU DECOUPLING 1

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GIGABYTE

Title: PCIE		
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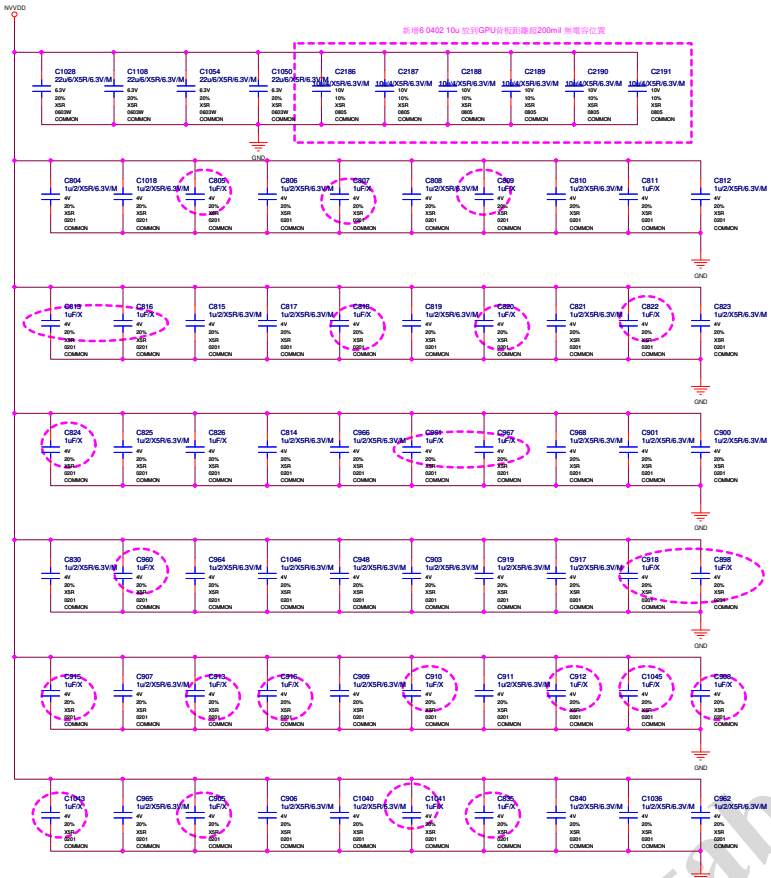
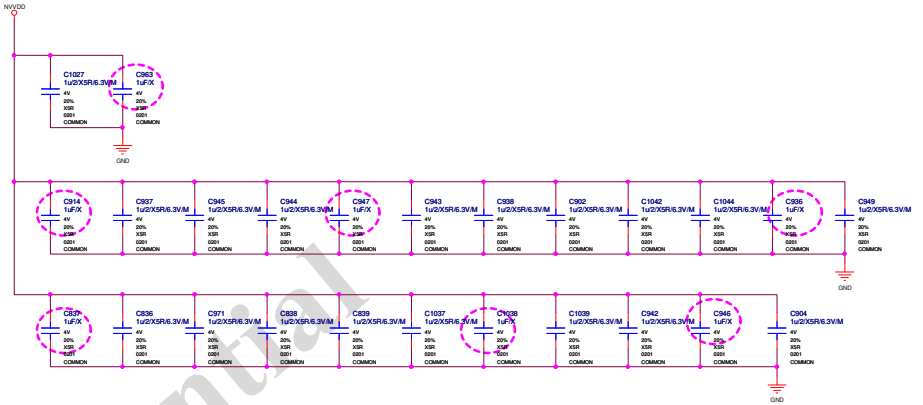
Page16: GPU DECOUPLING 2

NVVDD





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PAGE DETAIL

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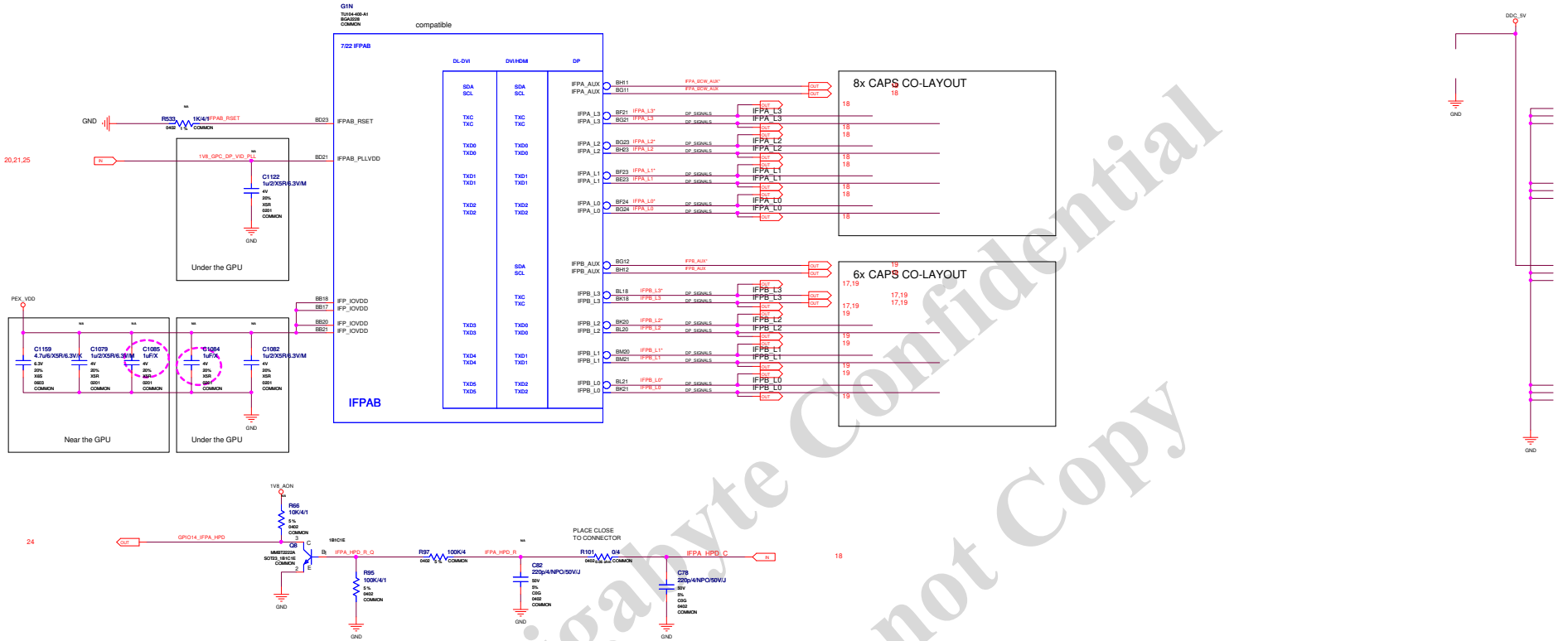
Page17: IFPAB DVI-D-DL



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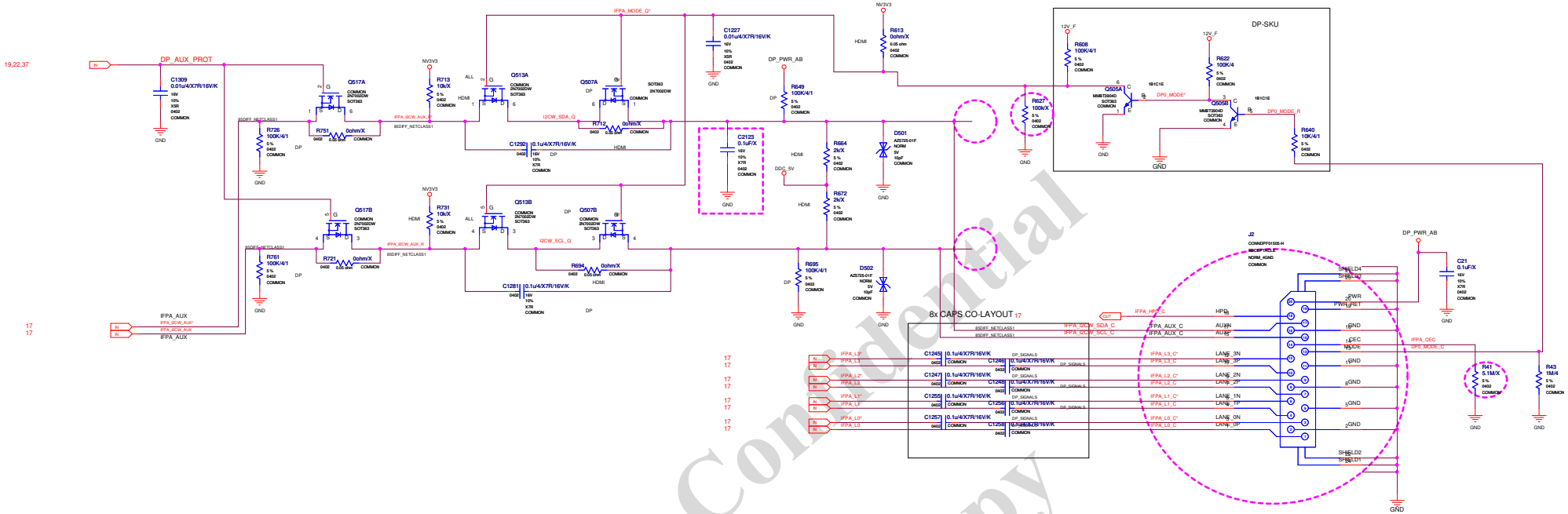
Page18: IFPA DP



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Size: Custom	Document Number: GV-N1660GAMING OC-6GD	Rev: 1.0
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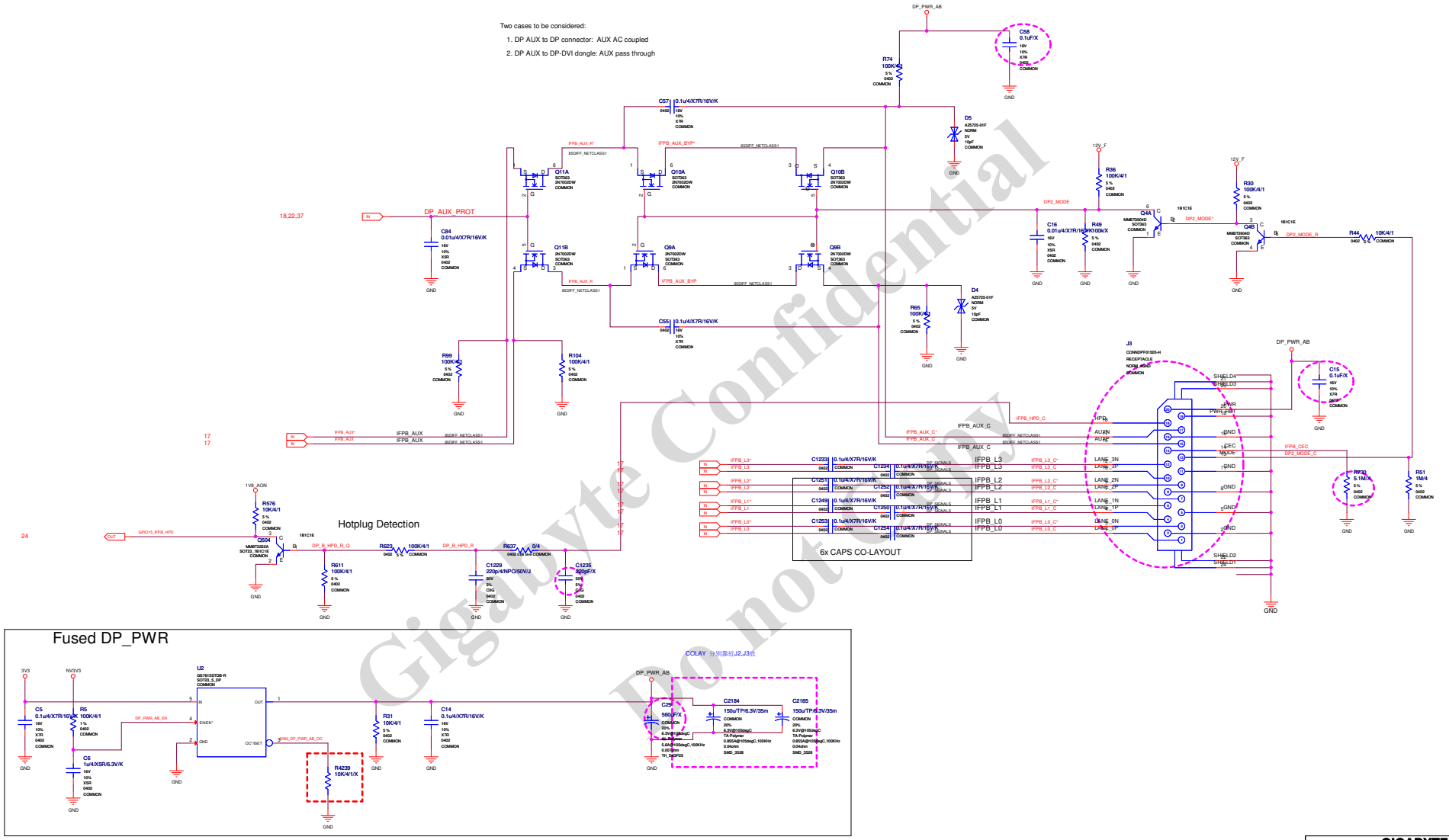

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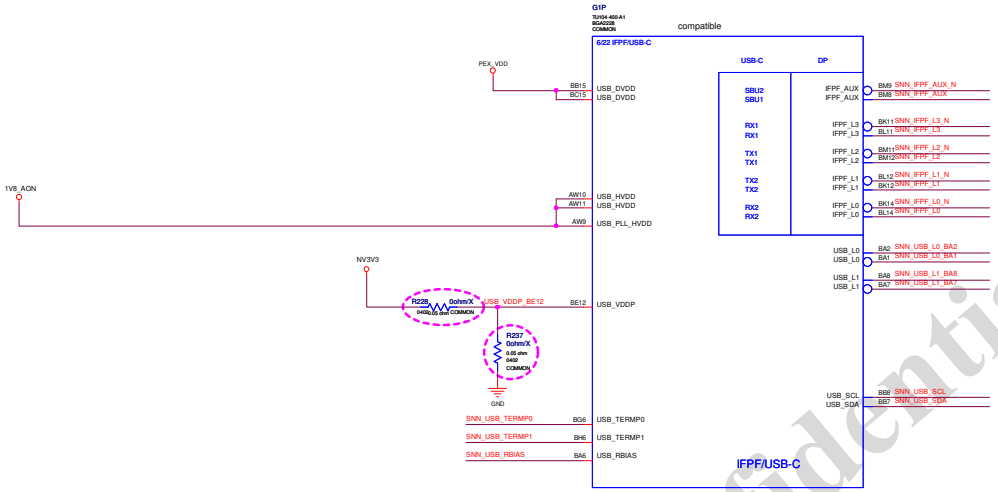
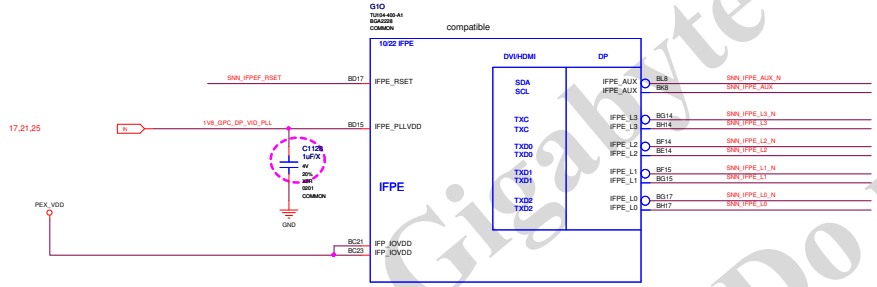
Page20: IFPE & IFPF NC





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IO: IFPE & IFPF NC

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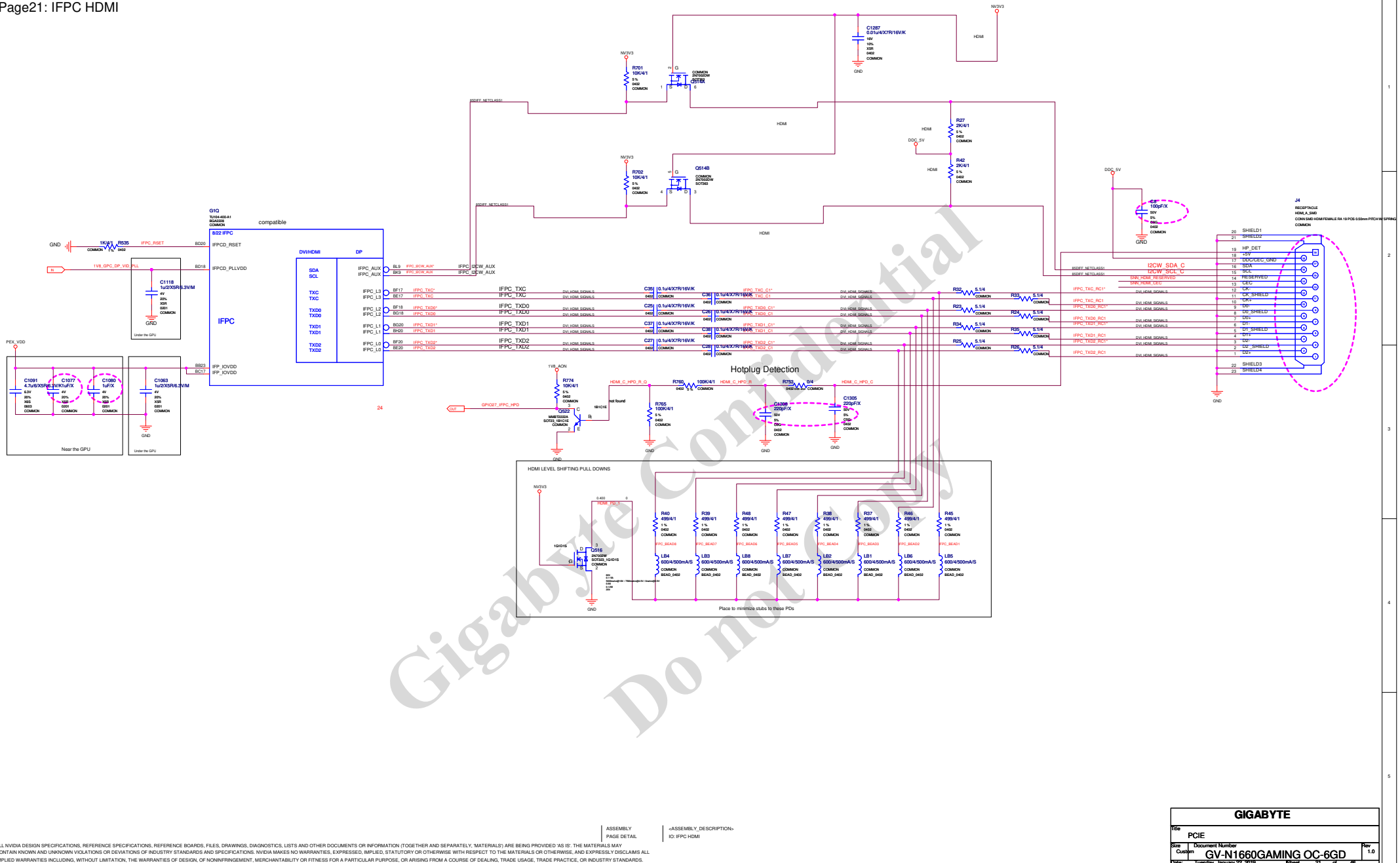
Page21: IFPC HDMI



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PAGE DETAIL	IO: IFPC HDMI

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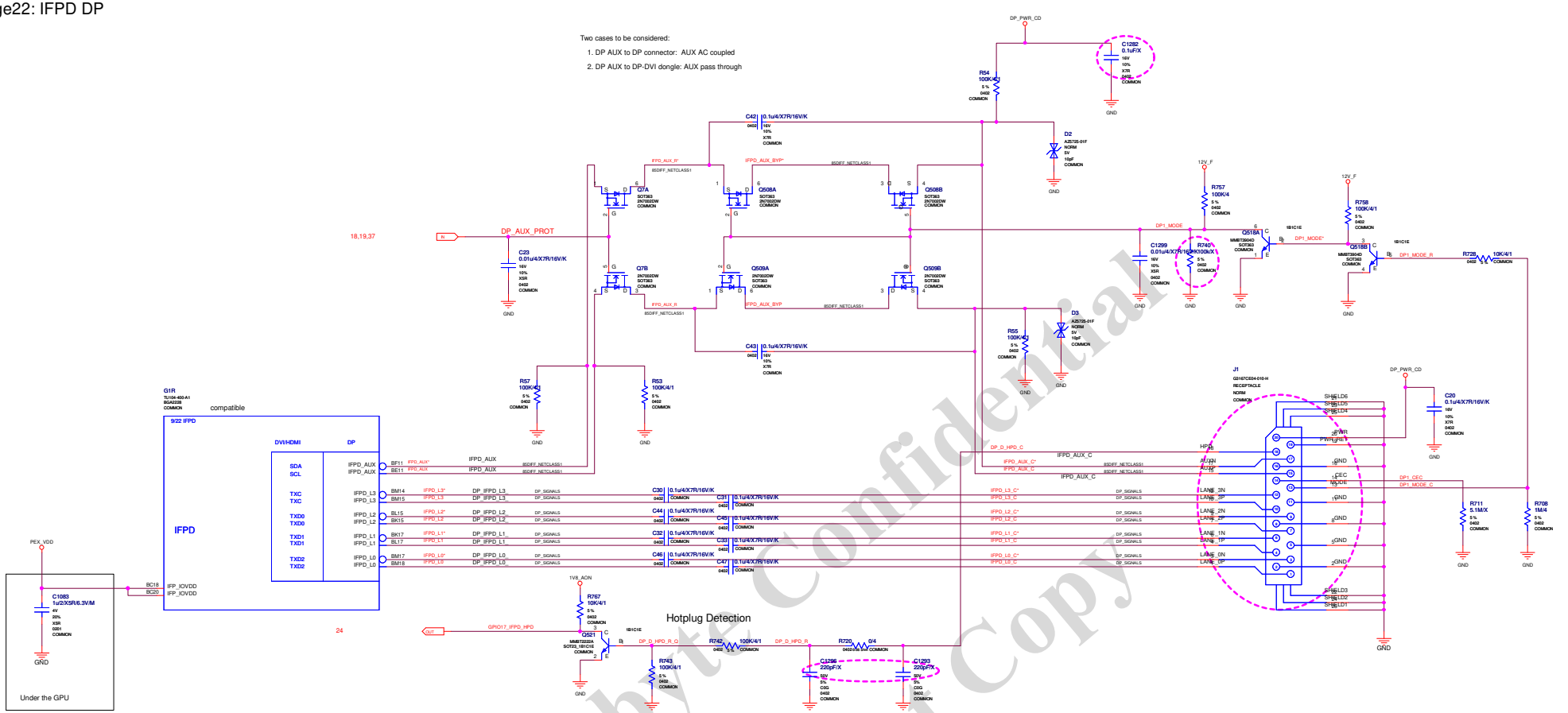
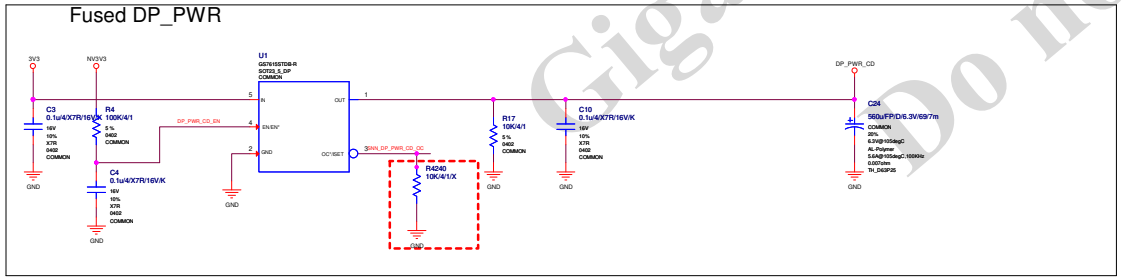
Page22: IFPD DP





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PAGE DETAIL

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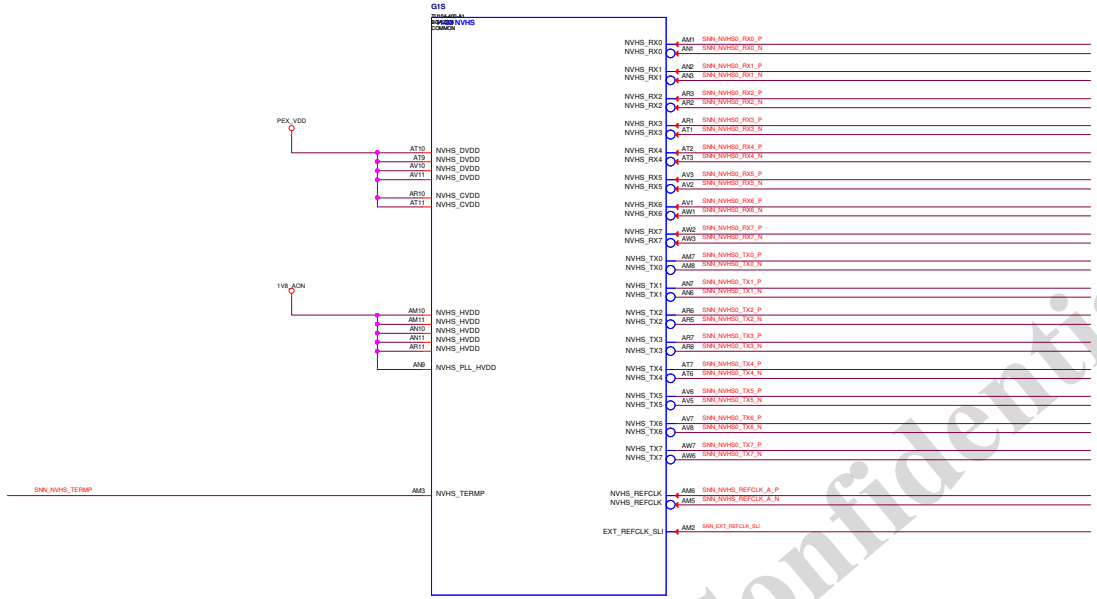
Page23: NVHS INTERFACE AND FRAME LOCK



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL IO: NVHS INTERFACE AND FRAME LOCK

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Title: PCIE		
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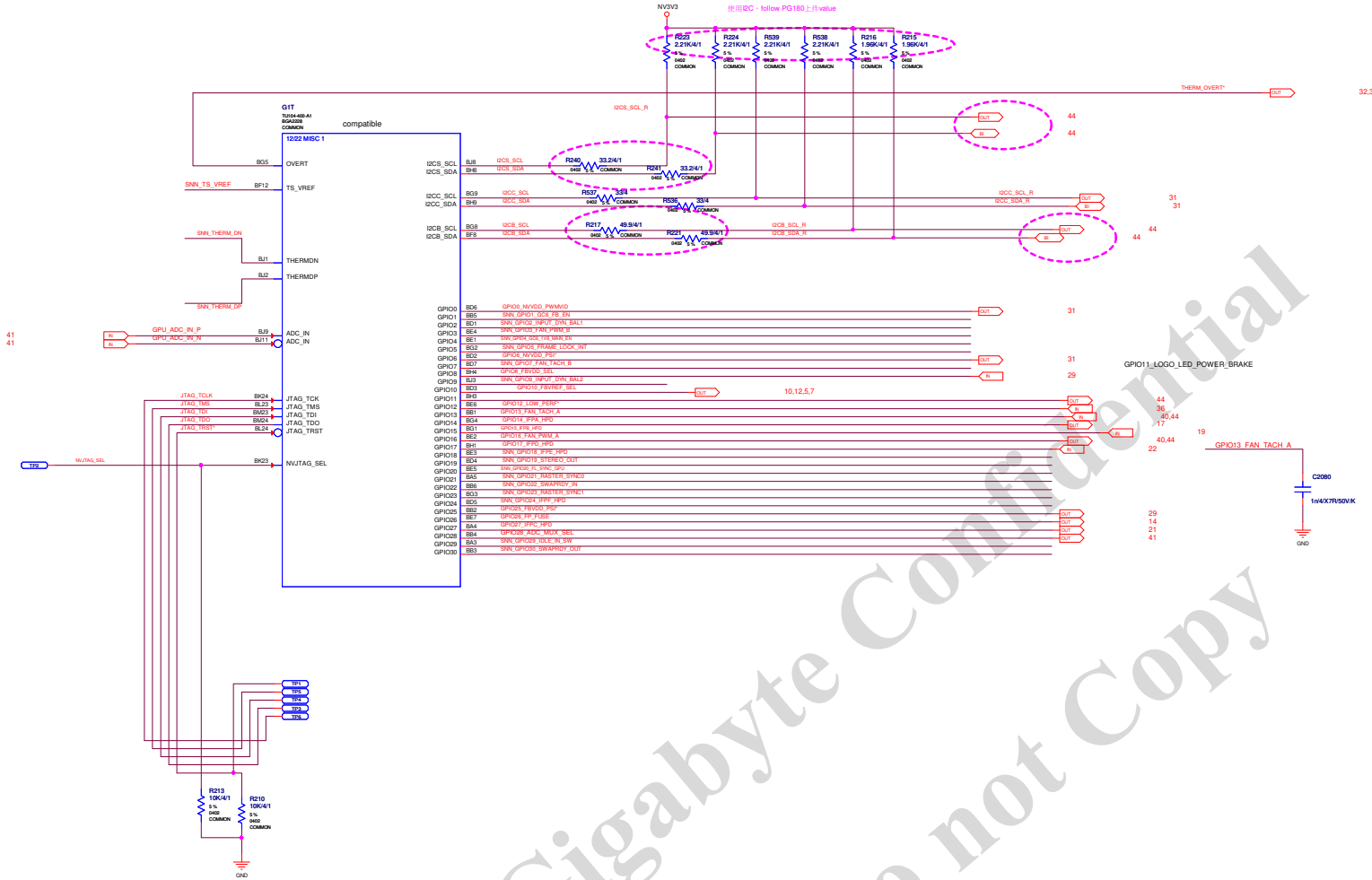
Page24: MISC1: JTAG, GPIO, ADC, I2C, OVERT



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: JTAG,GPIO,ADC,I2C,OVERT

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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung 8Gb 256Mx32 K4G80325FC-HC25
L	L	H	0001	Micron 8Gb 256Mx32 MT51J256M32HF-80:B
L	H	L	0010	Hynix 8Gb 256Mx32 H5GC8H24AJR-R2C
L	H	H	0011	Hynix 8Gb 256Mx32 H5GQ8H24MJR-R4C
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

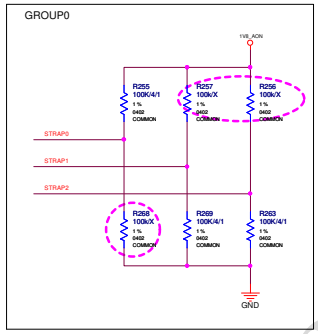
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

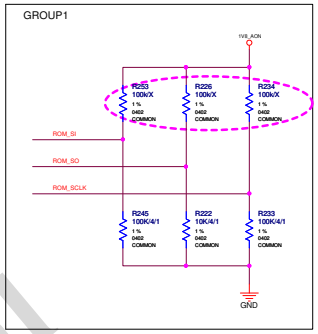
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

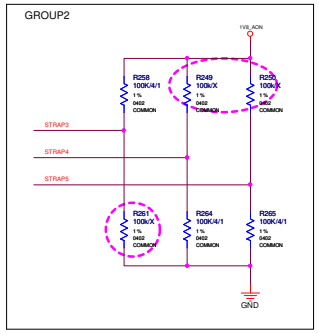
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

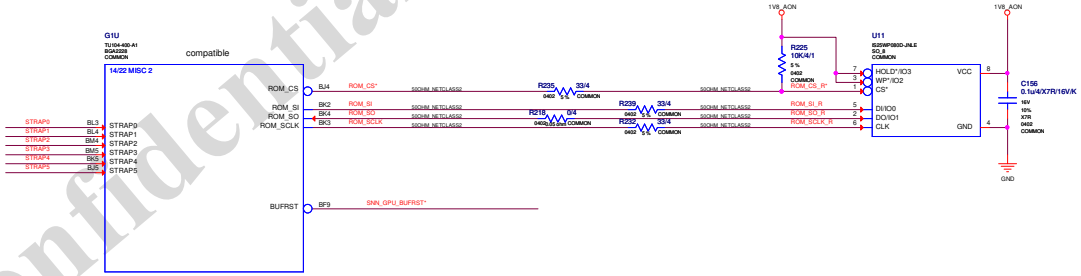
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

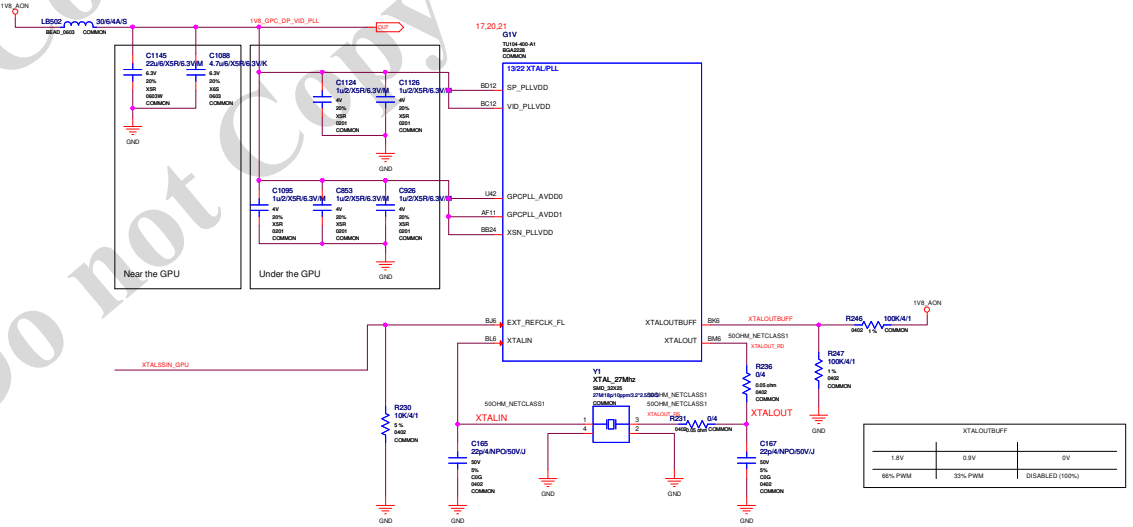
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE











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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL MISC2: ROM, XTAL,STRAPS

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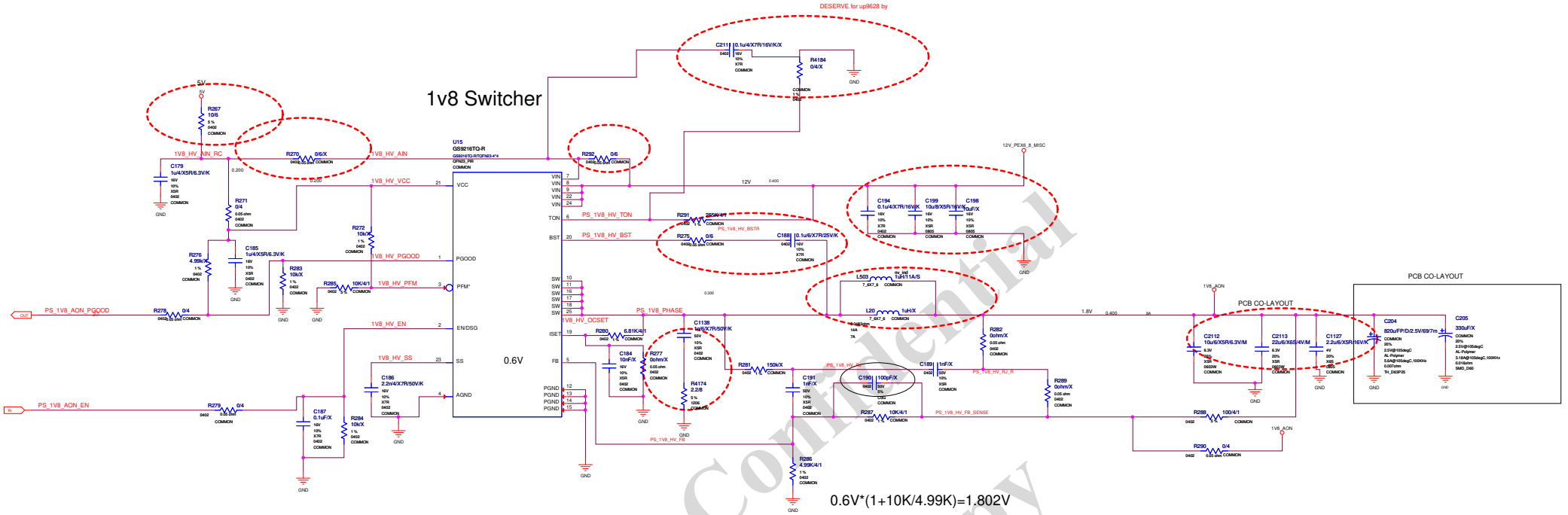
Page27: PS: 1V8_AON



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Title: PCIE

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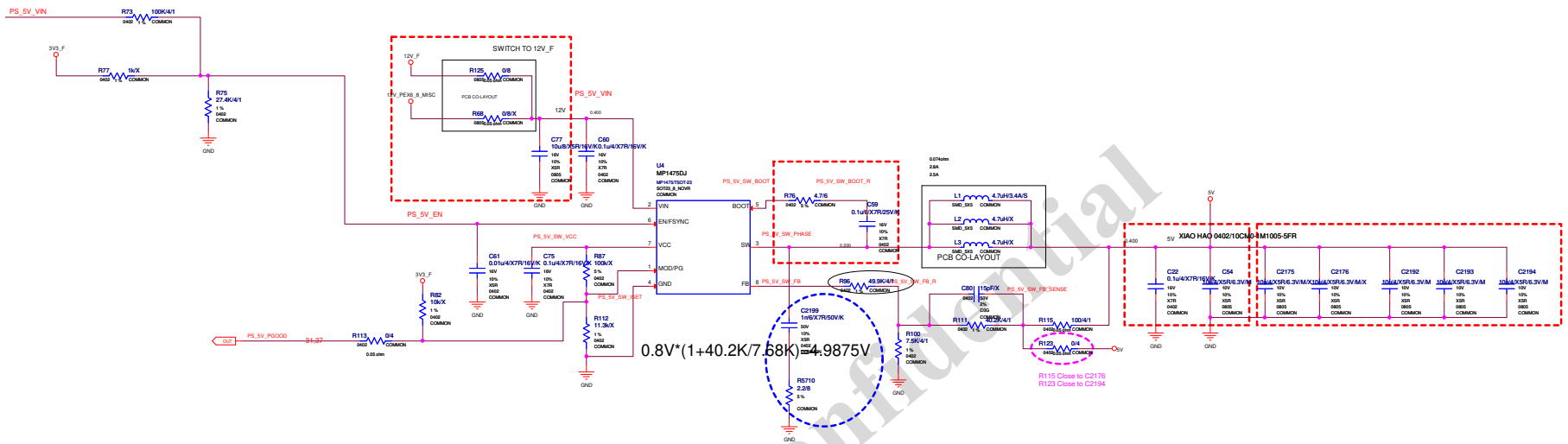

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Title: PCIE		
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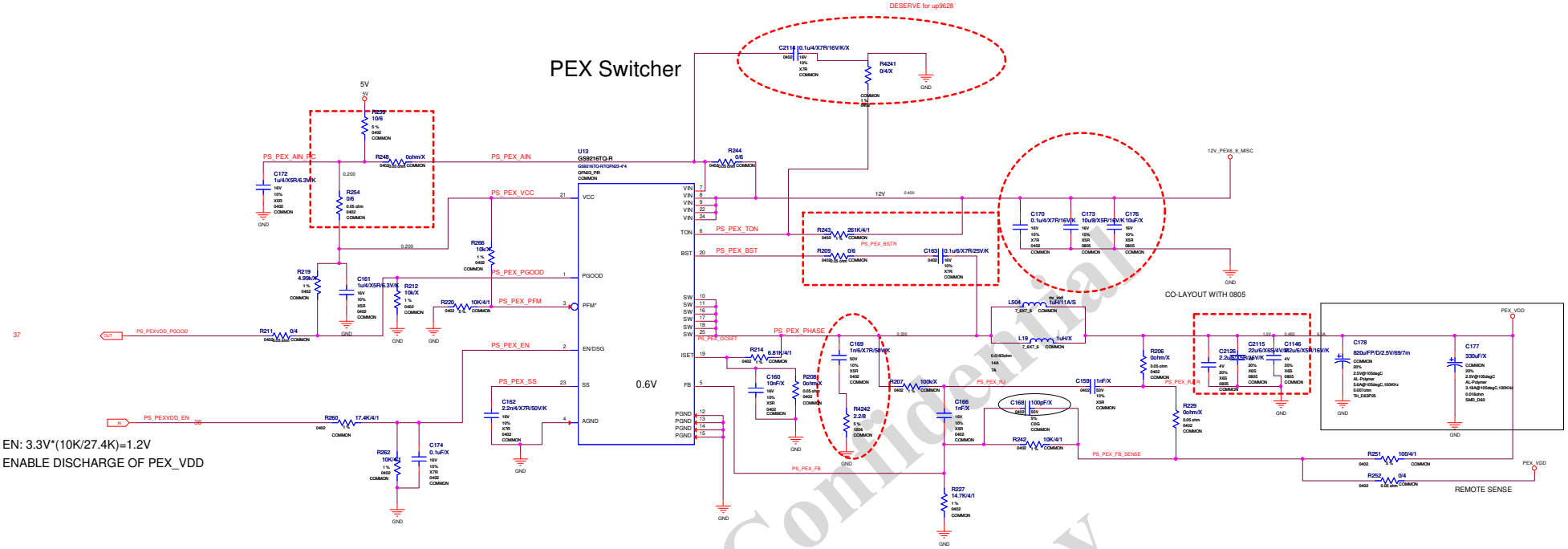

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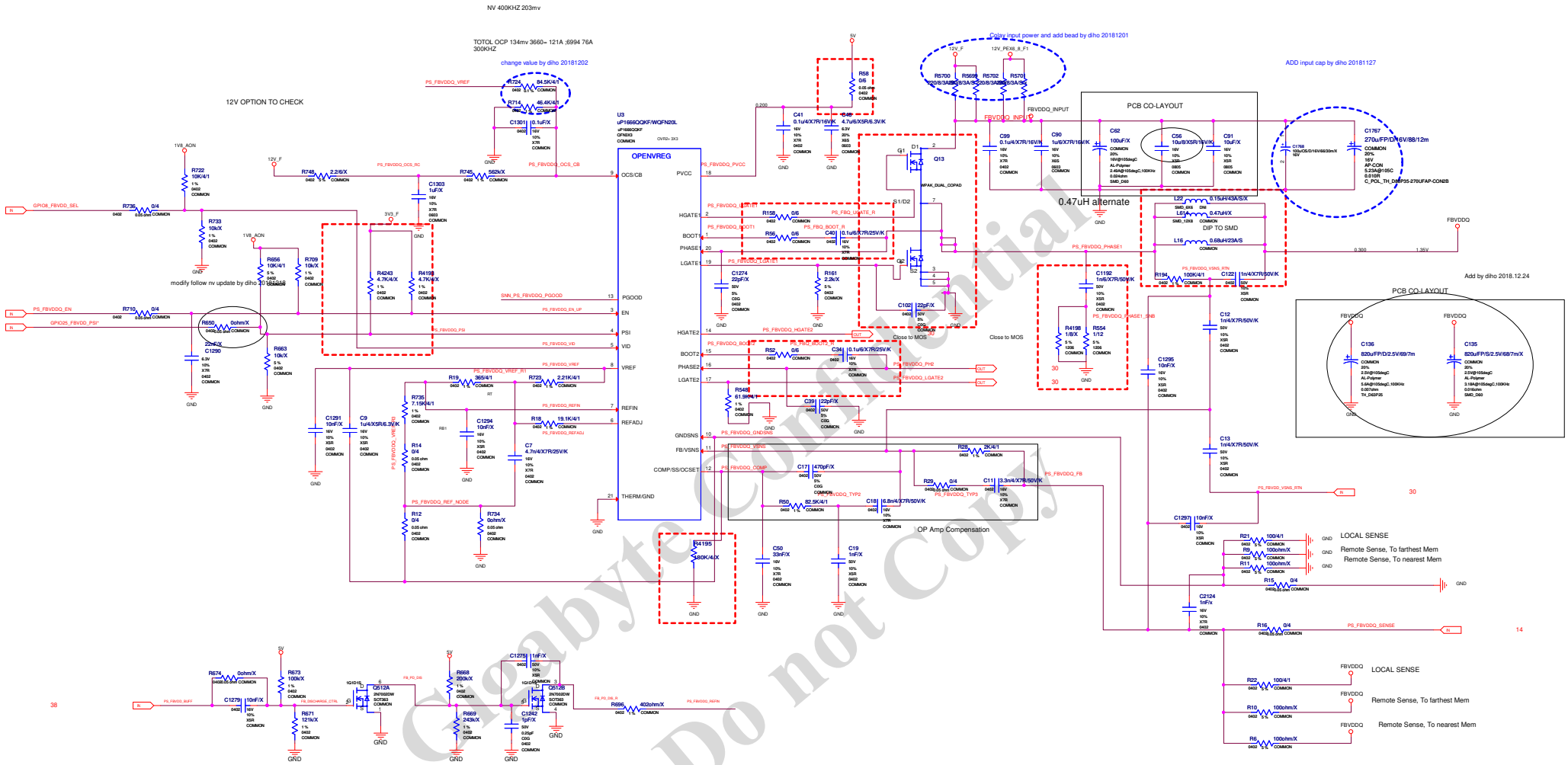
Page30: PS: FBVDDQ



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ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: FBVDDQ

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Title	PCIE
Size	Custom
Document Number	GV-N1660GAMING OC-6GD
Rev	1.0
Date:	Tuesday, January 22, 2019
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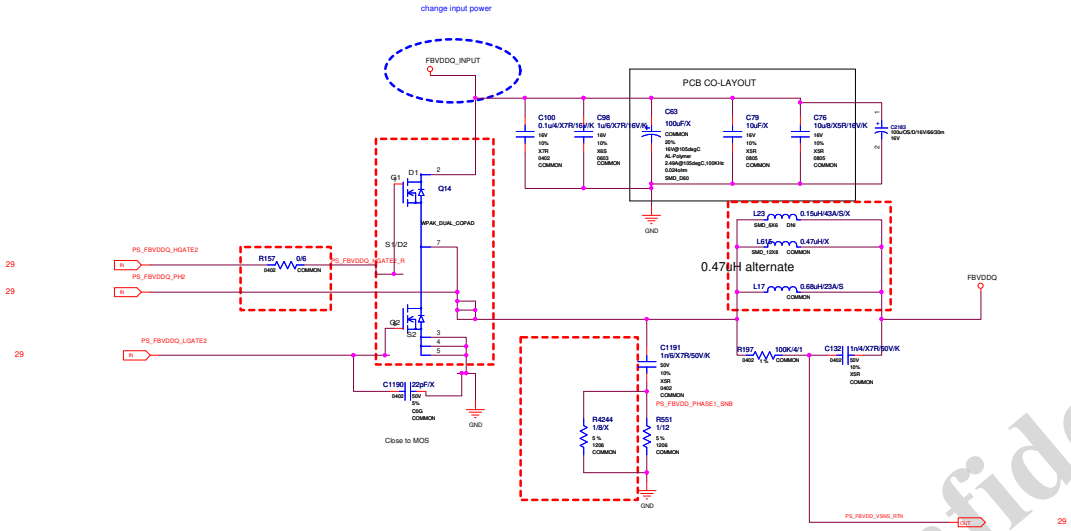

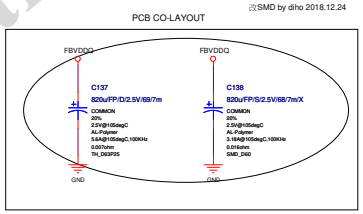

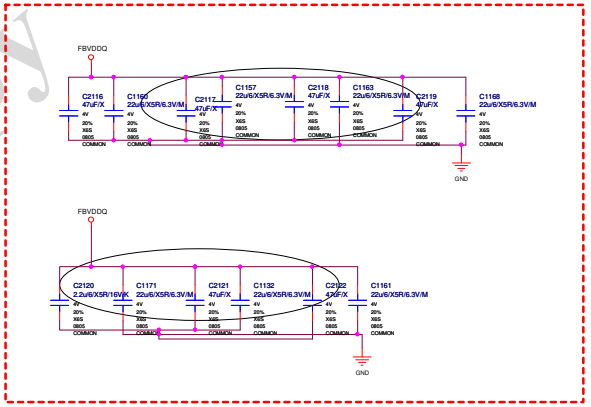

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Title: PCIE		
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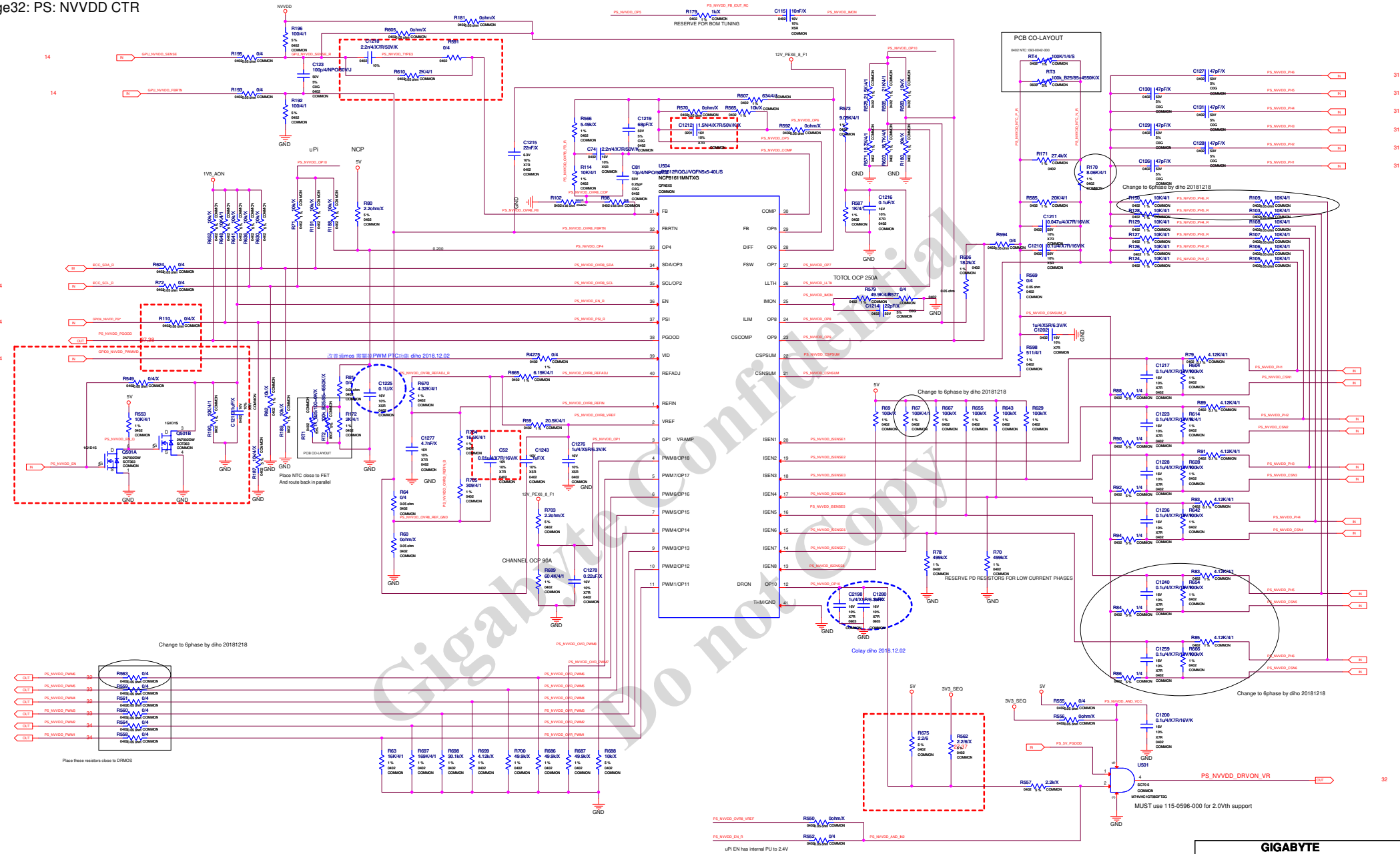
Page32: PS: NVVDD CTR



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PAGE DETAIL	PS: NVVDD Controller

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Size: Custom	Document Number: GV-N1660GAMING OC-6GD	Rev: 1.0
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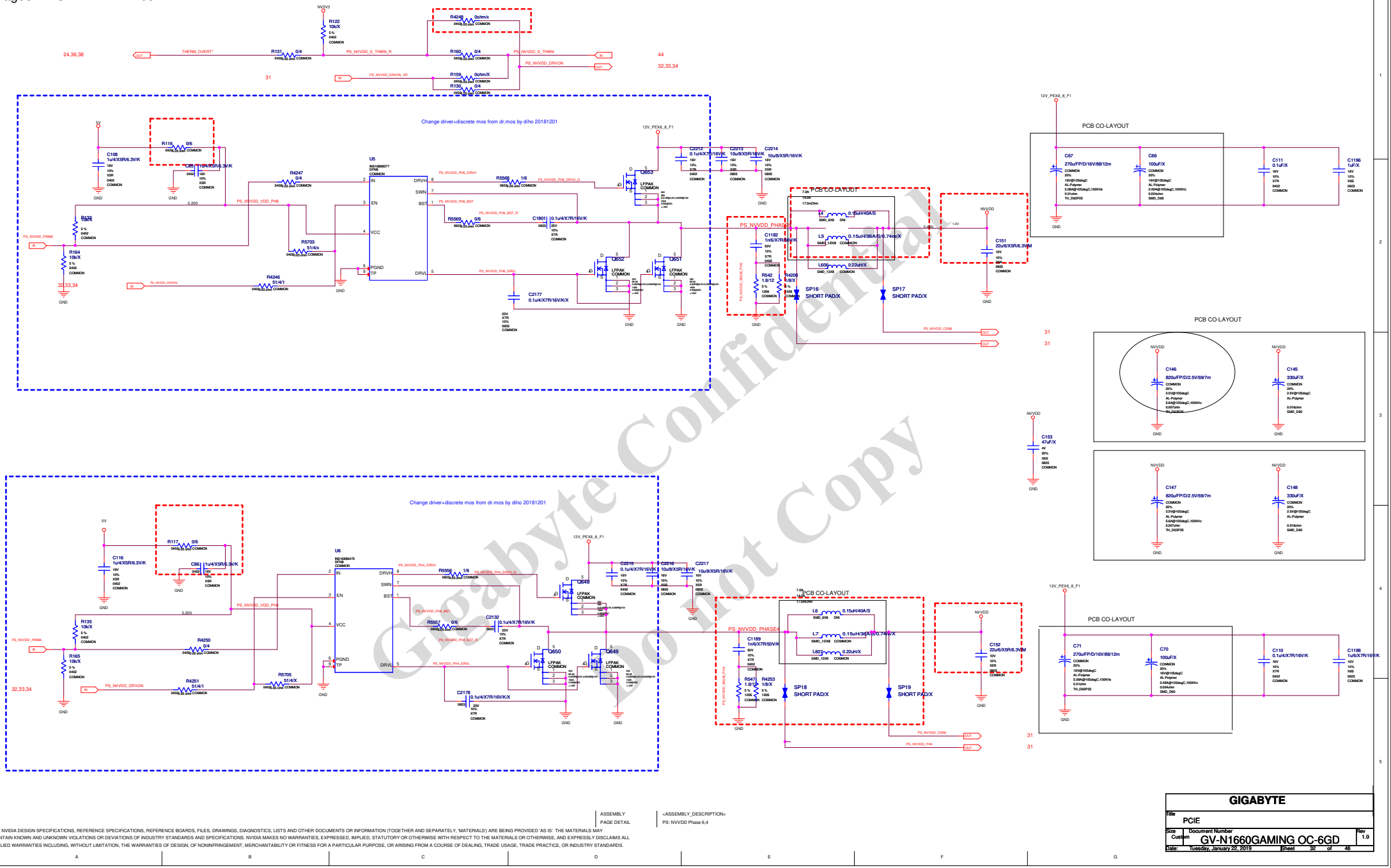
Page34: PS: NVVDD PH6&4



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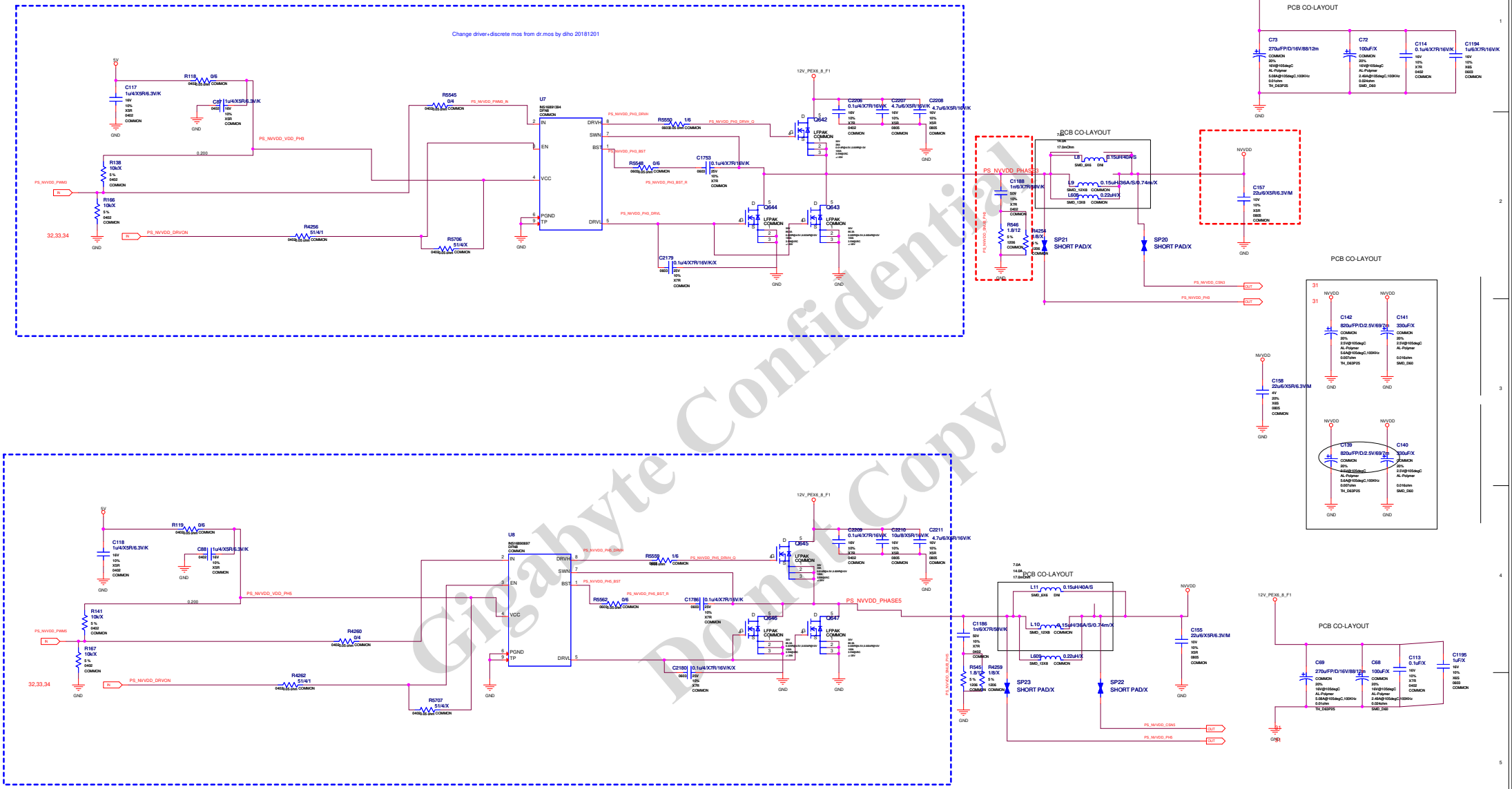
Page35: PS: NVVDD PH3&5



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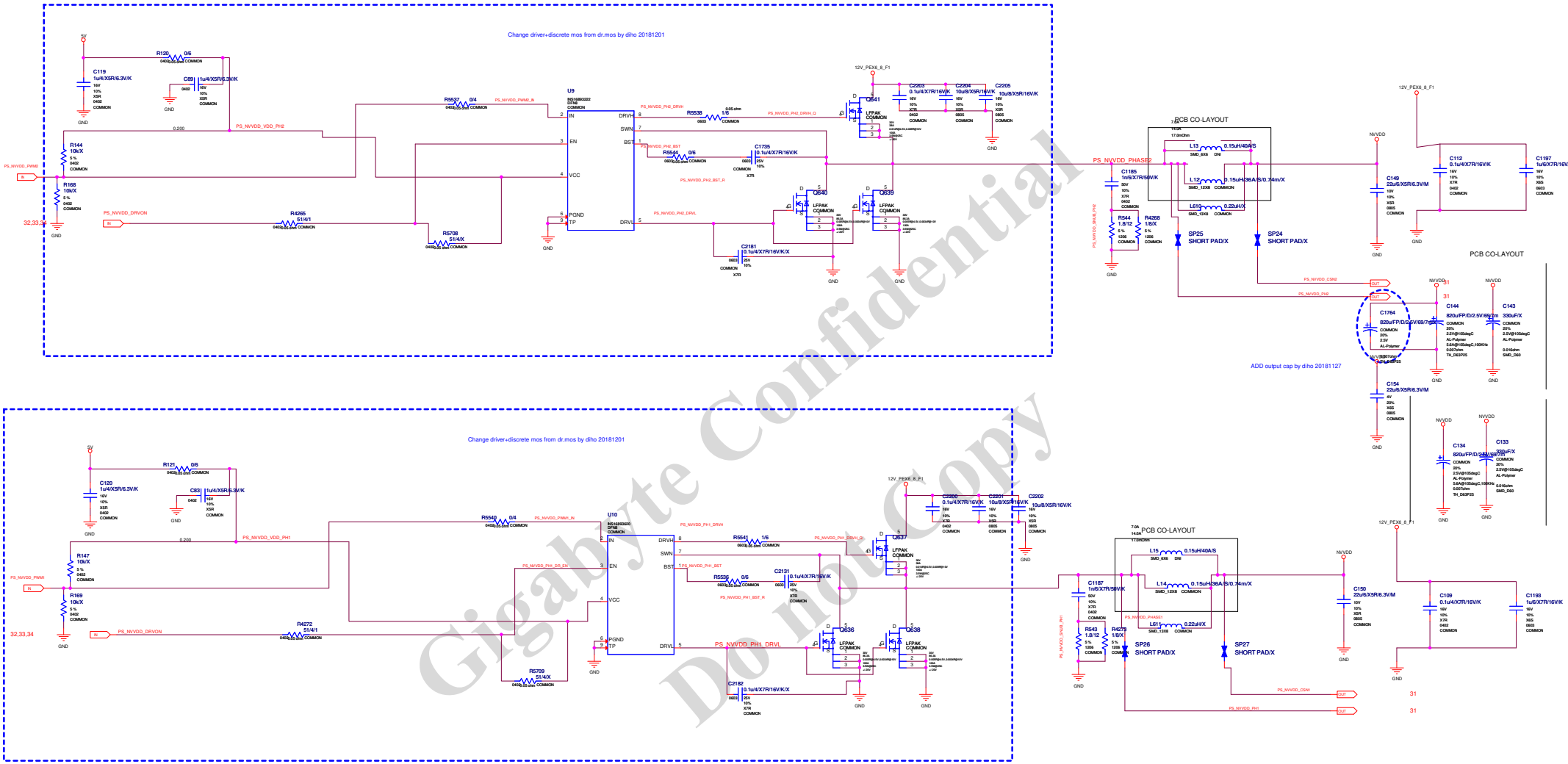

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PAGE DETAIL	PS: NVVDD Phase 2,1

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Title: PCIE		
Size: Custom	Document Number: GV-N1660GAMING OC-6GD	Rev: 1.0
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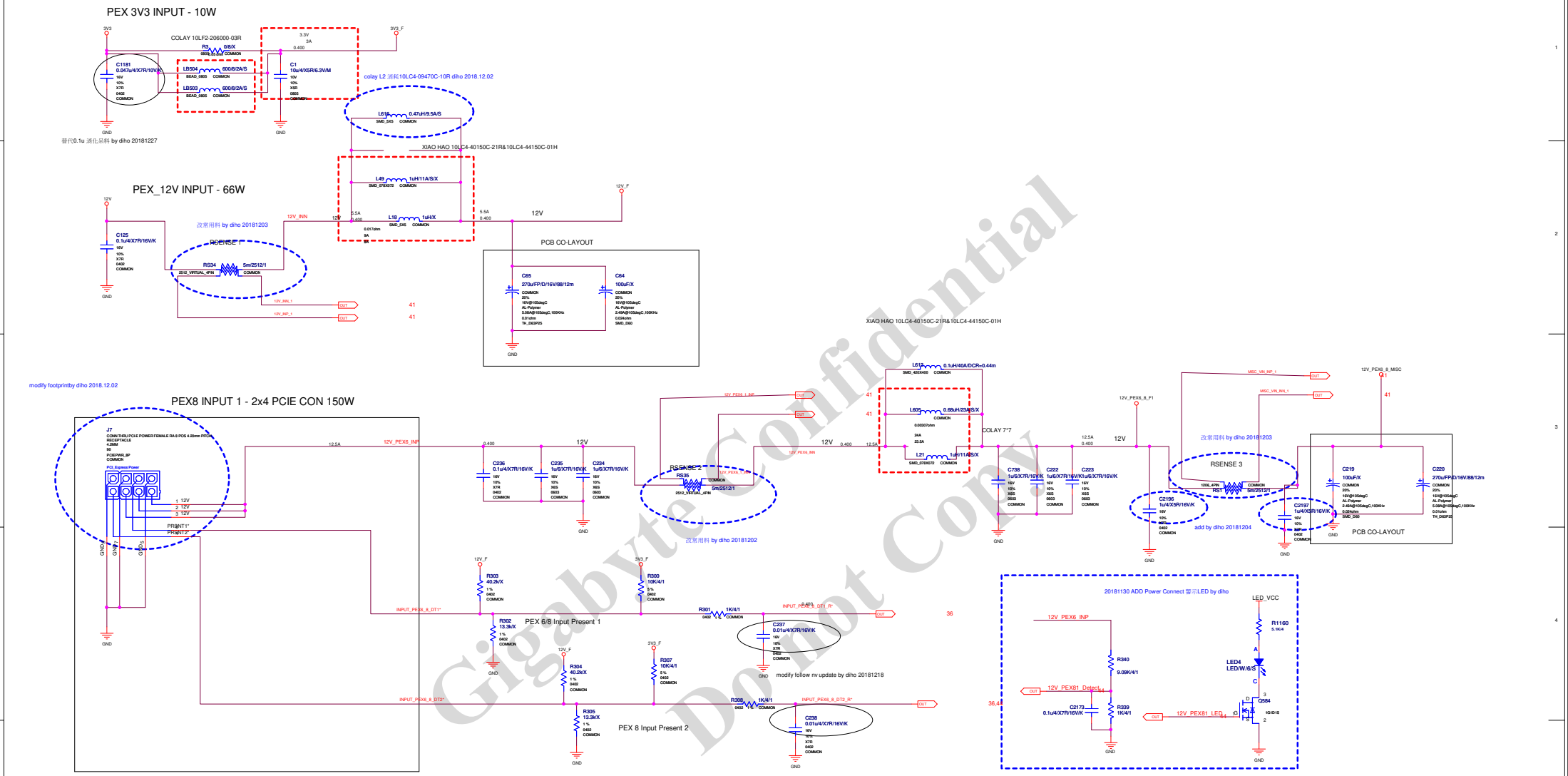
Page38: PS: Inputs, Filtering, and Monitoring



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PS: Input, Filtering, and Monitoring

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Title: PCIE

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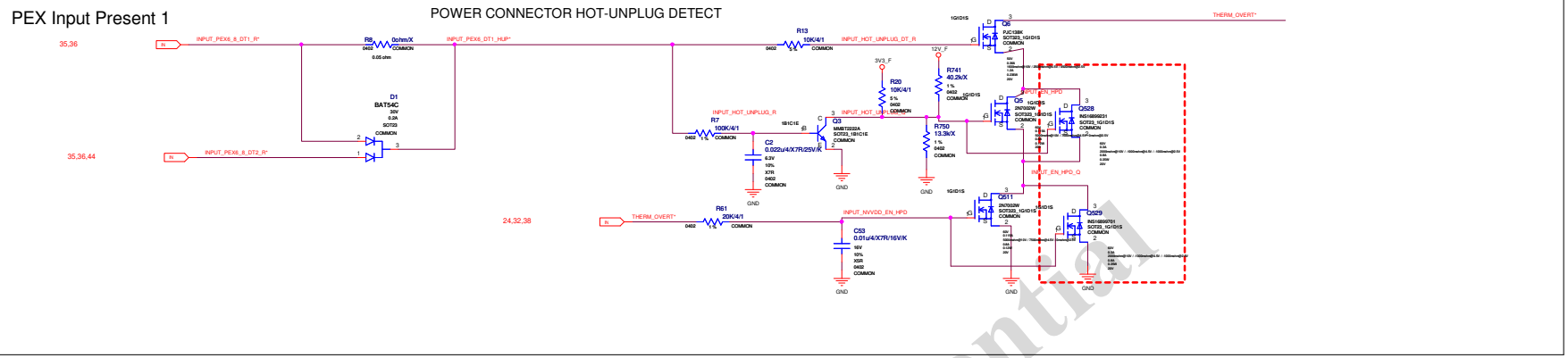
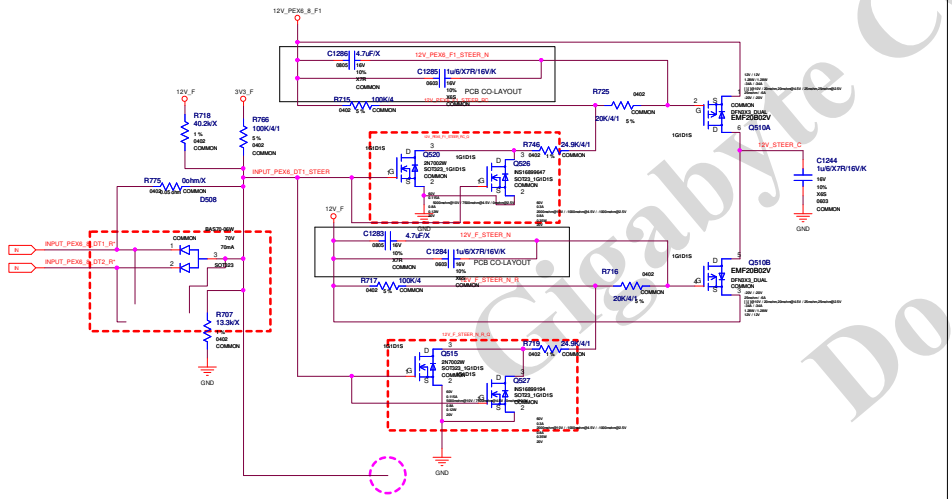
Page39: PS: HOT-UNPLUG, UNDER POWER BOOT, CURRENT STEERING

PEX Input Present 1

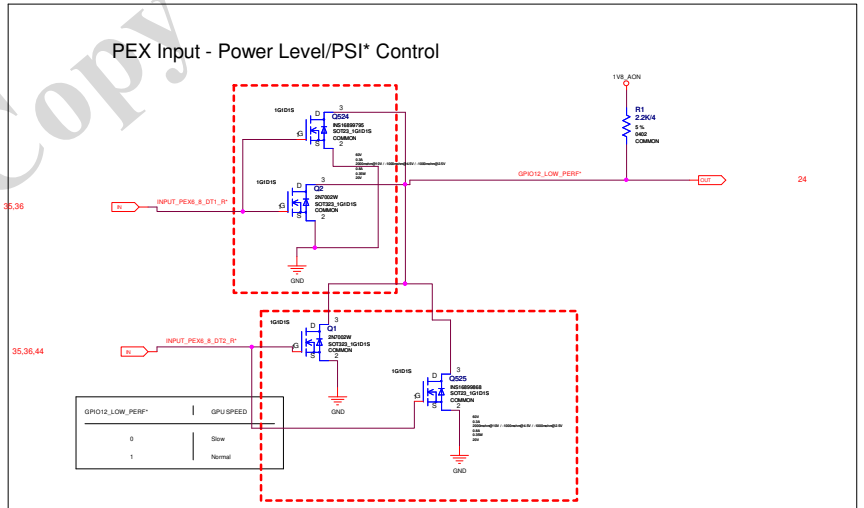


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



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ASSEMBLY
PAGE DETAIL

<ASSEMBLY_DESCRIPTION>
PS: STEERING, UPB & HOT-UNPLUG

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Title: PCIE		
Size: Custom	Document Number: GV-N1660GAMING OC-6GD	Rev: 1.0
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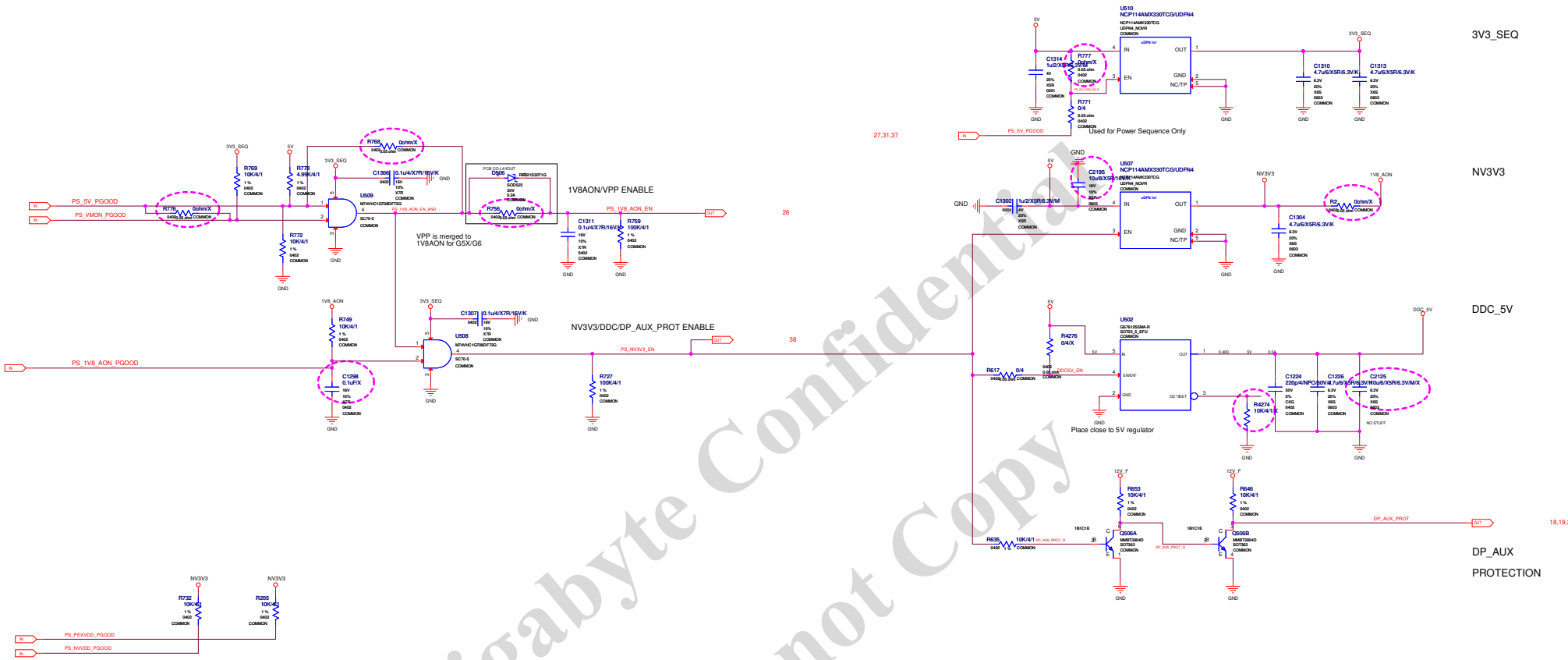
Page37: SEQ:1V8_AON, 3V3_SEQ, NV3V3, DDC_5V, DP_AUX_PROT



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PAGE DETAIL	SEQ: 1V8_AON, 3V3_SEQ, NV3V3, DDC_5V, DP_AUX_PROT

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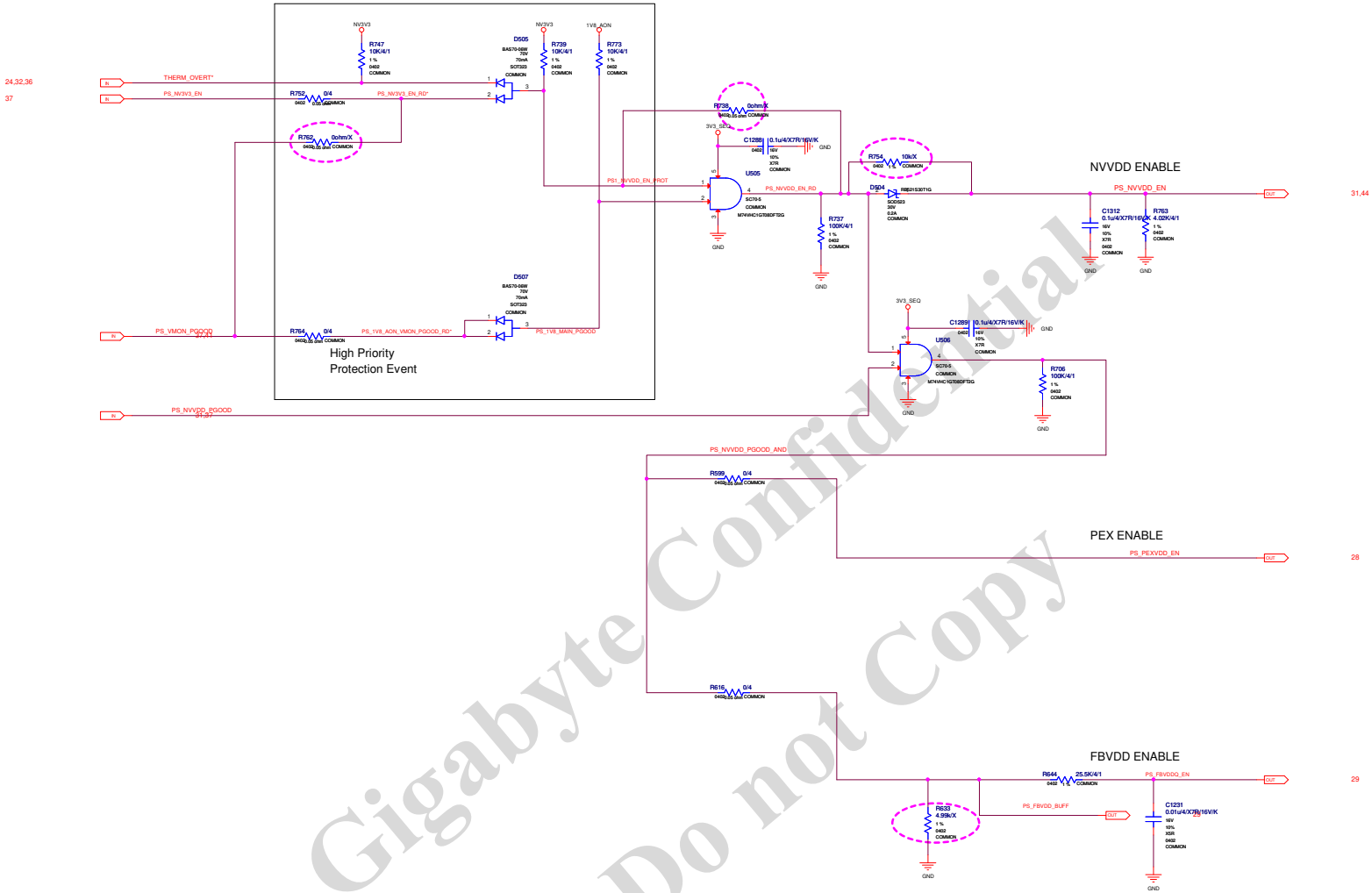
Page38: SEQ:NVVDD, PEX, FBVDDQ ENABLE



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NVVDD, PEX, FBVDDQ ENABLE

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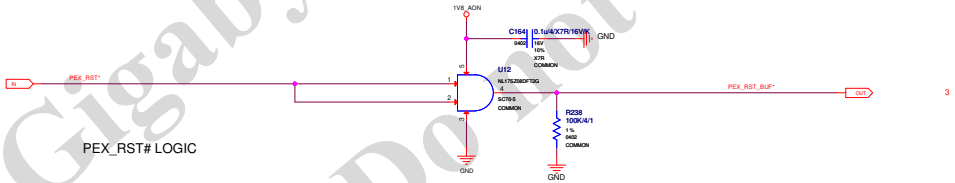
PU ON GPU SIDE
NC ON GOLD FINGER SIDE

PU ON GPU SIDE
NC ON GOLD FINGER SIDE



PEX_RST# LOGIC

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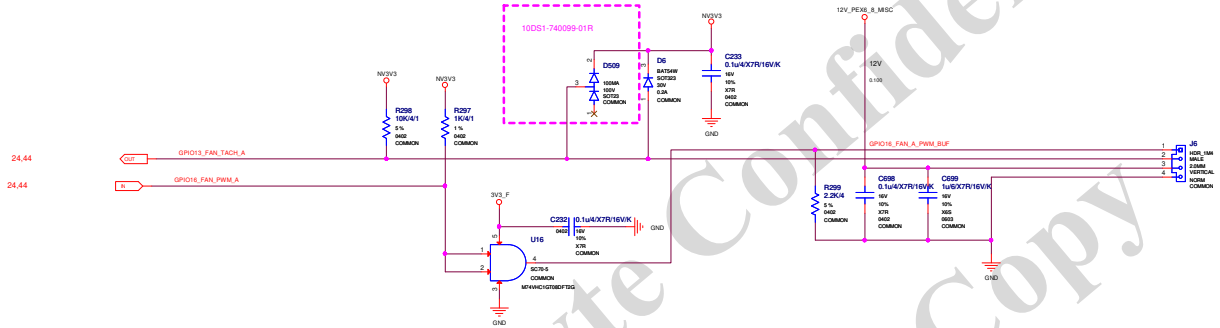
Page40: FAN



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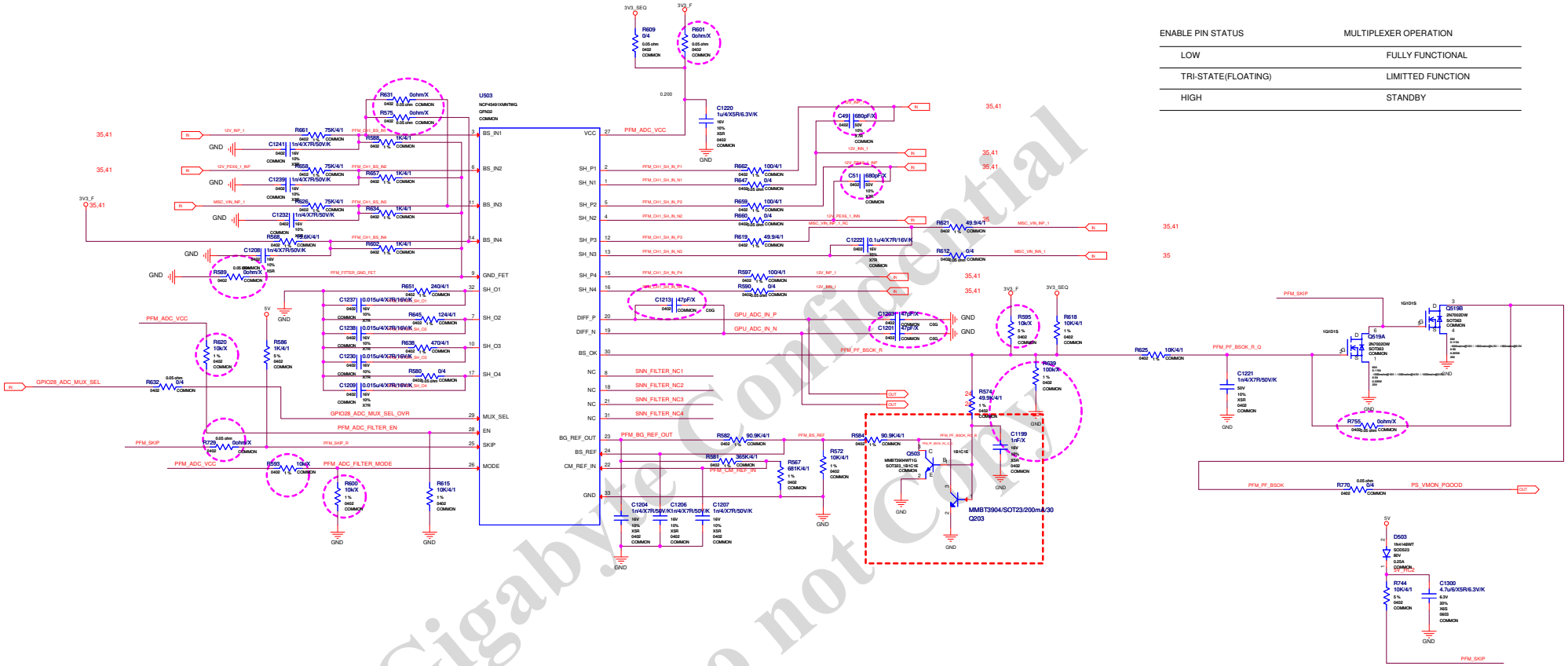
MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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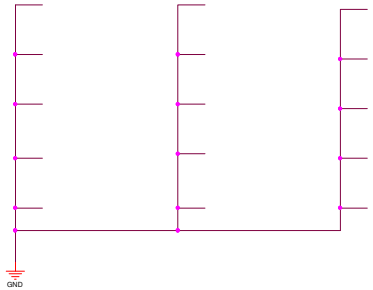
Brackets:

MOUNTING HOLES FOR HS:



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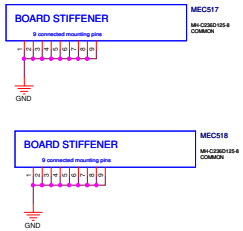

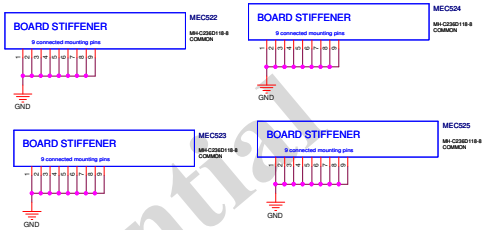

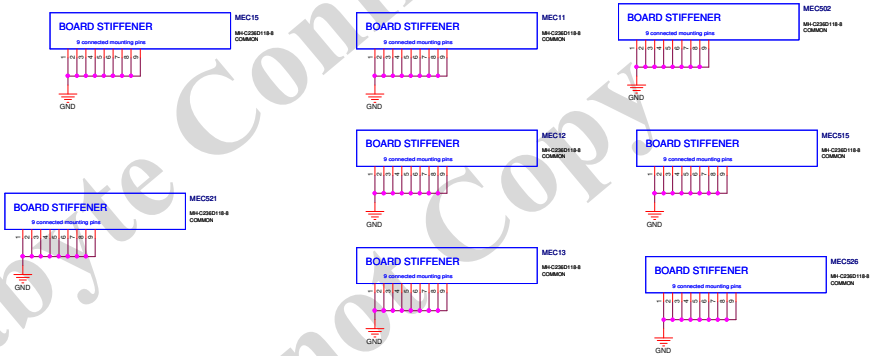

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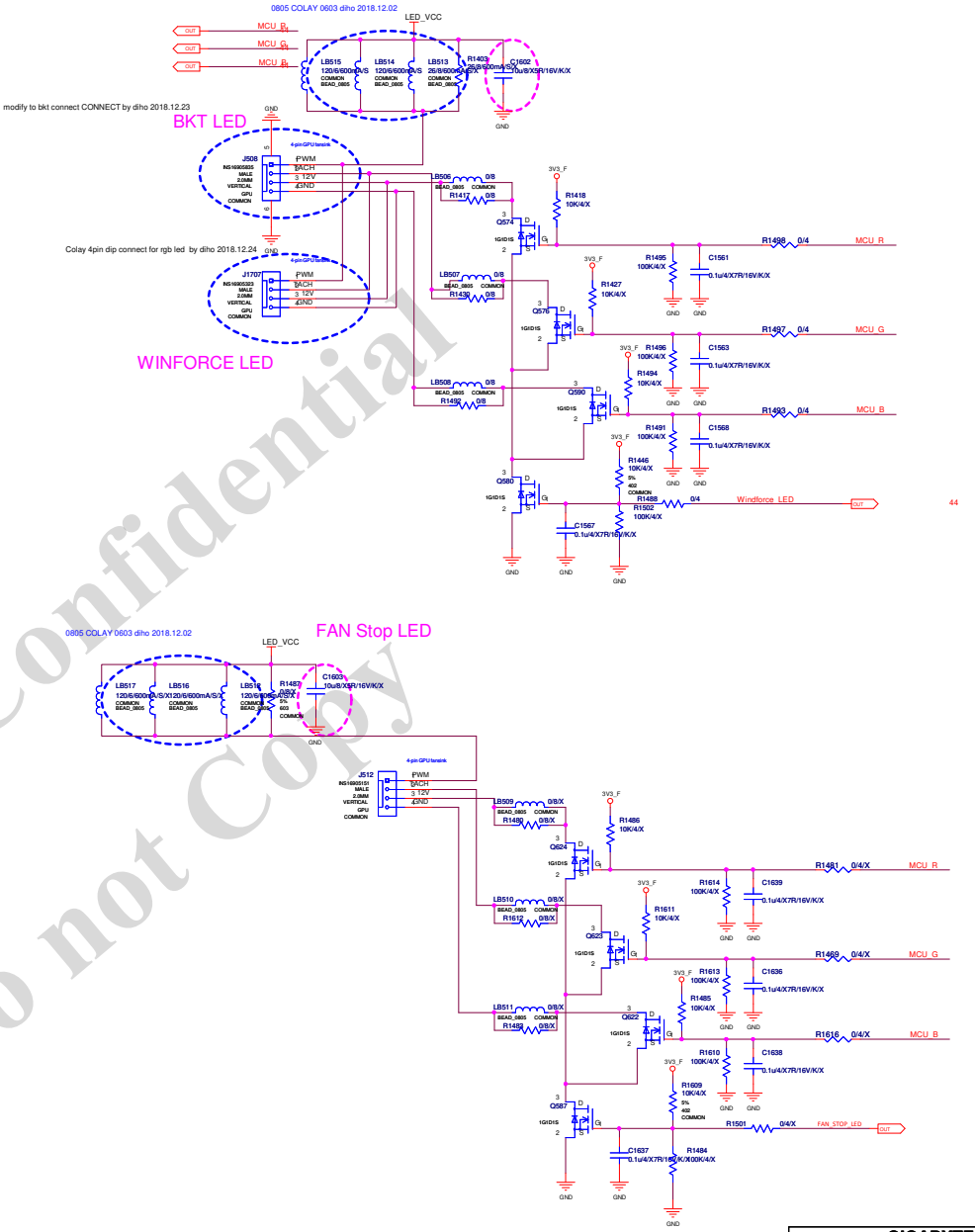
Page40: LED_LED



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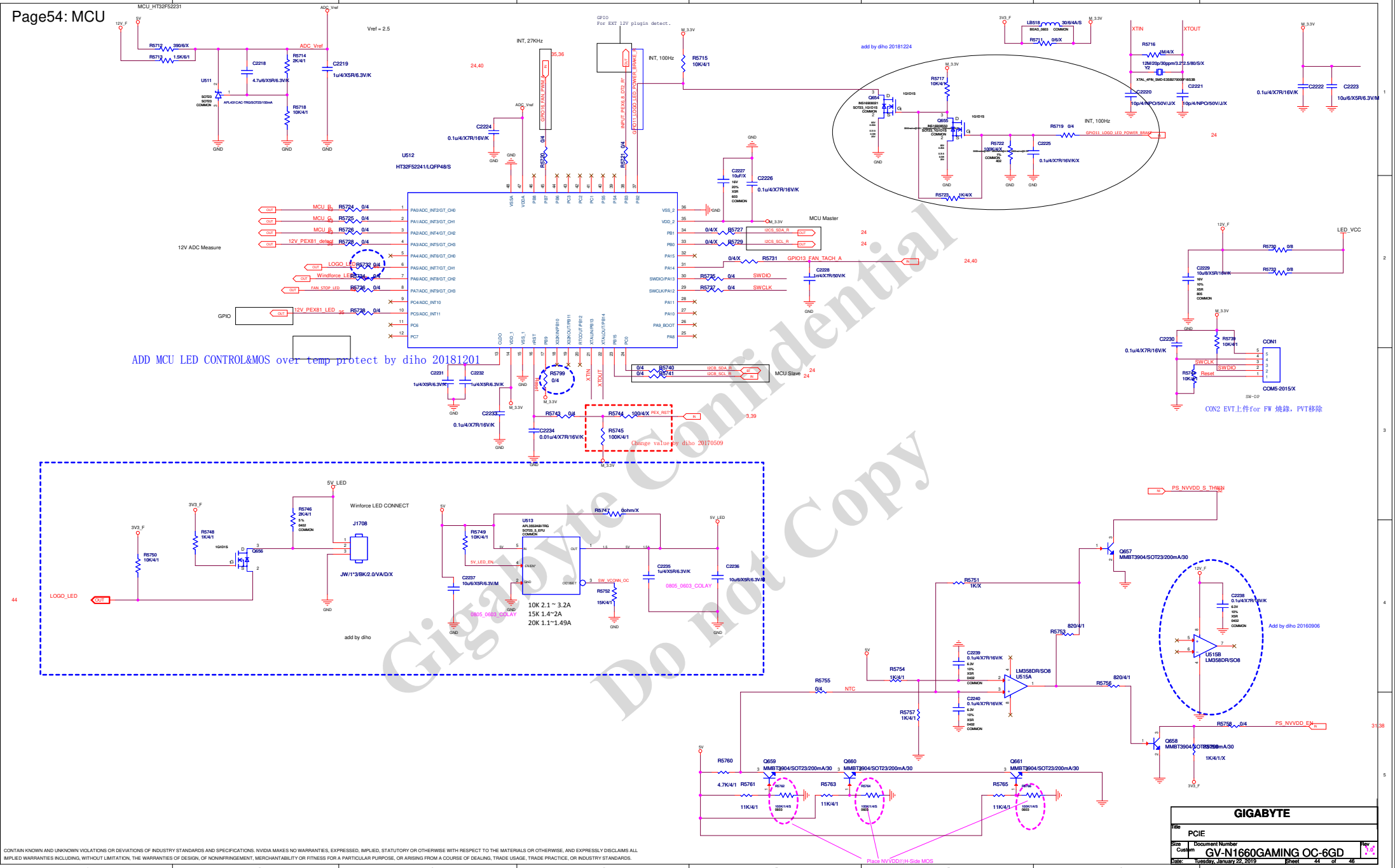
Page54: MCU



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