P216-A02 DESIGN -- NV43, 128 MB DDR3, VGA, DVI-I, SD/HDTV, VIVO

PAGE SUMMARY:

dev	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10216-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	000	602-10216-0000-200	NV43-U 500/500MHz 128MB DDR3 8MX32 DVI+VGA+HDTVOUT
2	001	602-10216-0001-200	NV43-U 500/500MHZ 128MB DDR3 8MX32 DVI+VGA+HDMVO
3	002	602-10216-0002-200	NV43-U 350/350MHZ 128MB DDR3 8MX32 DVI+VGA+HDTVOUT
4	003	602-10216-0003-200	NV43-U 400/400MHZ 128MB DDR3 8MX32 DVI+VGA+HDTVOUT
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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X01

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TABLE OF CONTENTS & REVISION HISTORY

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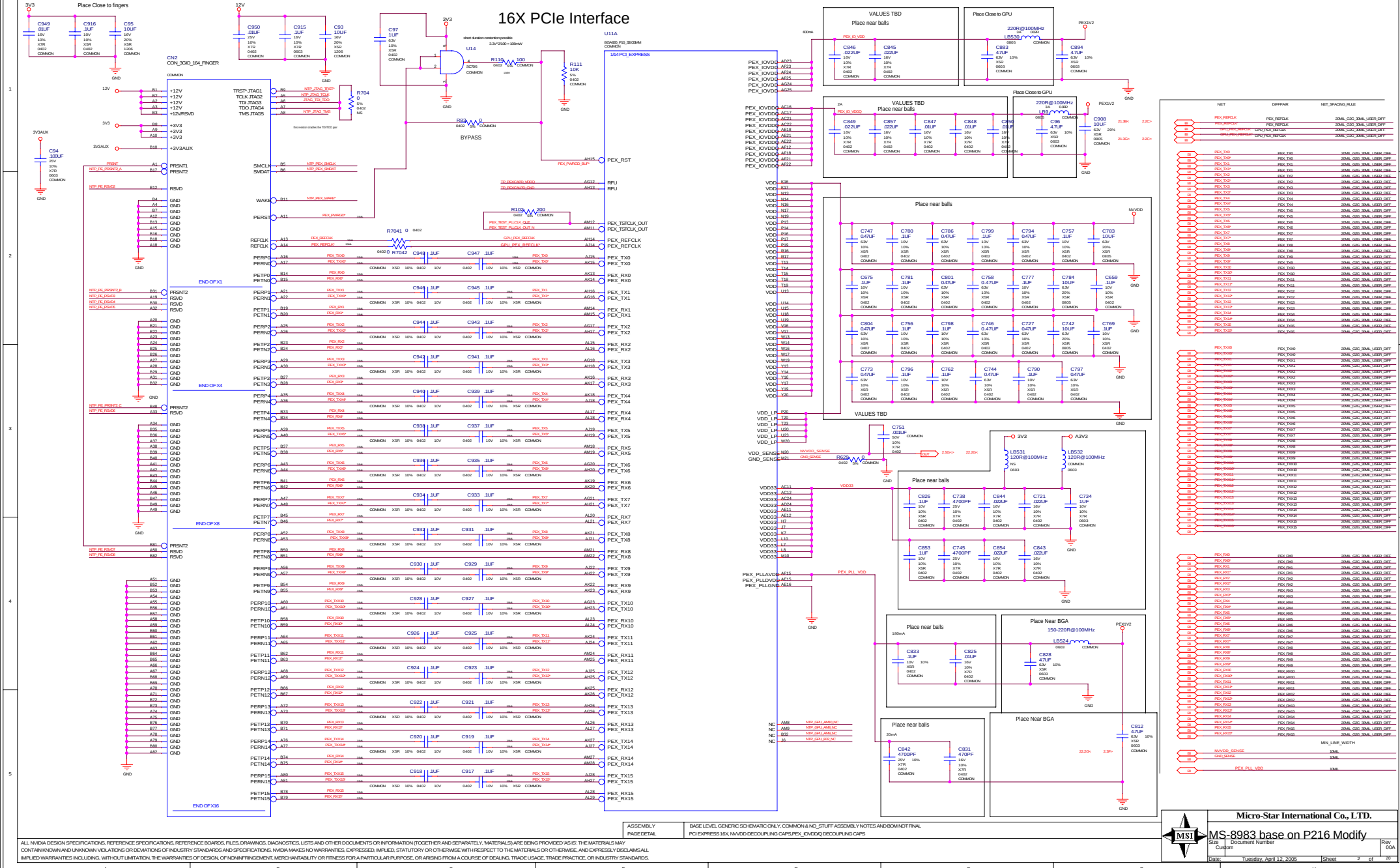
16X PCIe Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PCI EXPRESS 16X, NVVDD DECOUPLING CAPS,PEX_IOVDDQ DECOUPLING CAPS

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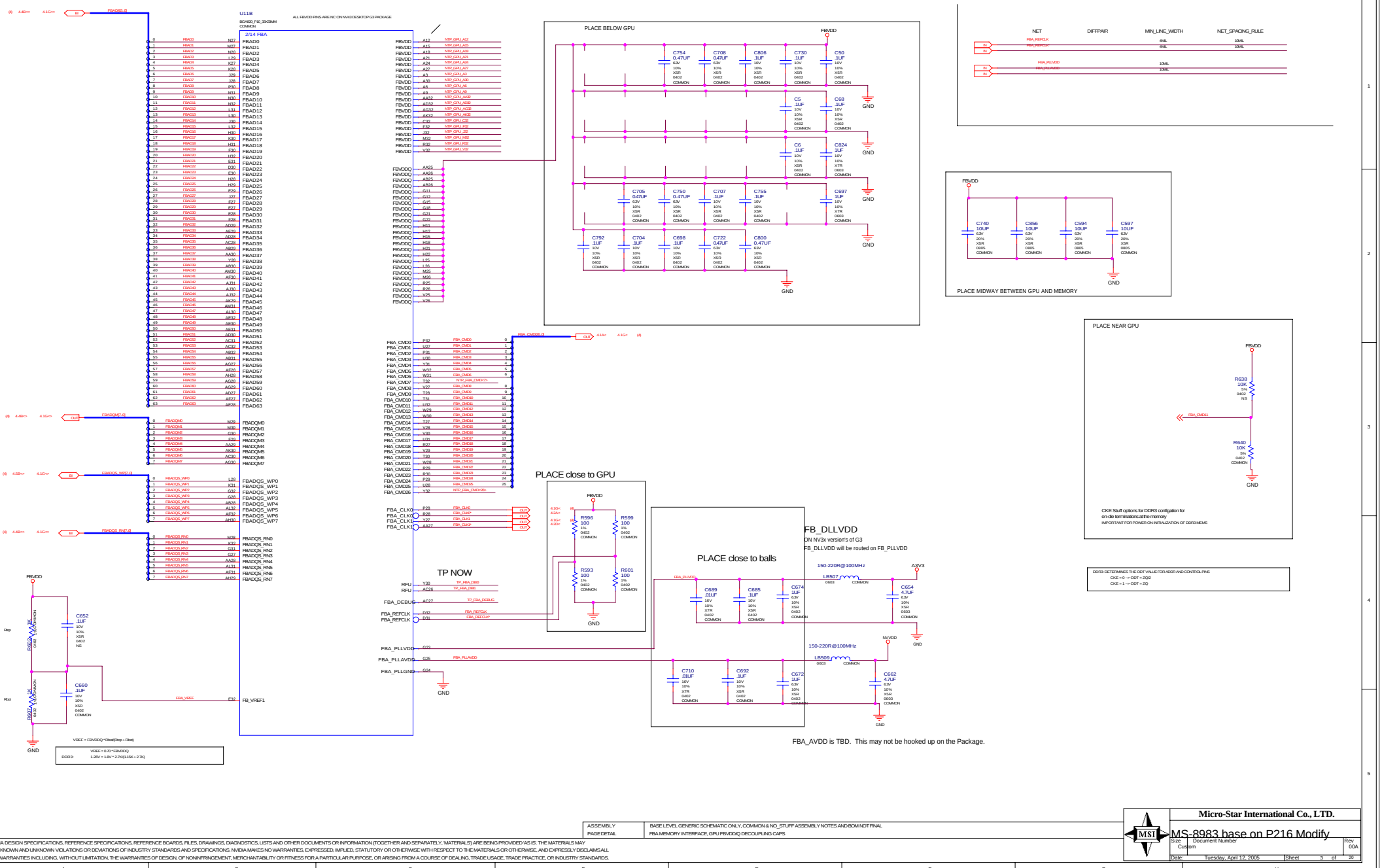

NET	DIFFPAIR	MIN_LINE_WIDTH	NET_SPACING_RULE
FBA_REFCLK		4MIL	10MIL
FBA_REFCLK#		4MIL	10MIL
FBA_PLLVDD		10MIL	
FBA_PLLAVDD		10MIL	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY INTERFACE, GPU FBVDDQ DECOUPLING CAPS

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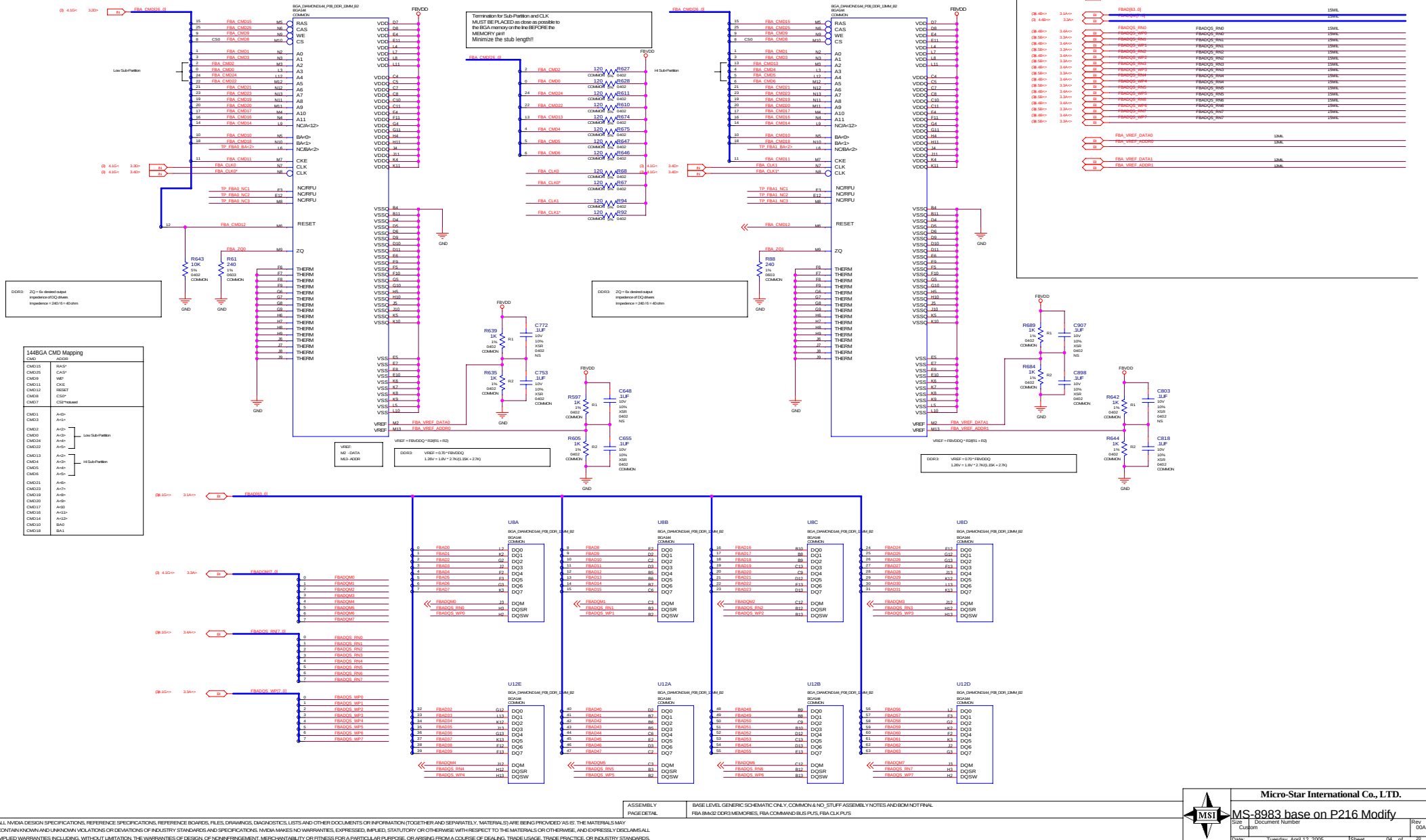
5 FrameBuffer: Partition A 8Mx32 BGA144 DDR3



ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: FBA 8Mx32 DDR3 MEMORIES, FBA COMMAND BUS PUS, FBA CLK PUS

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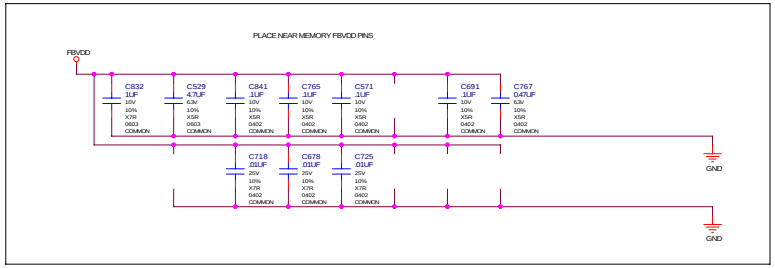
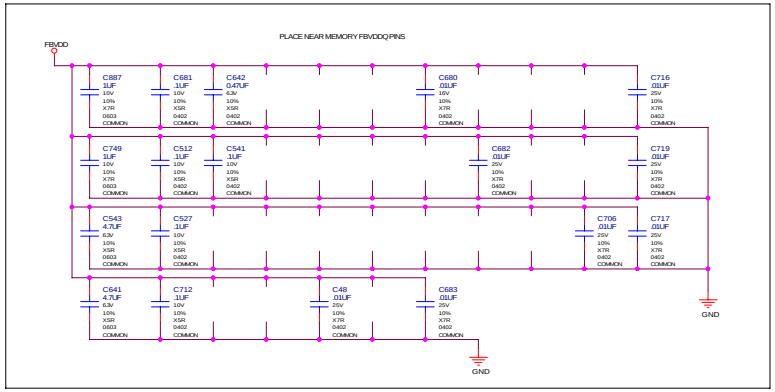
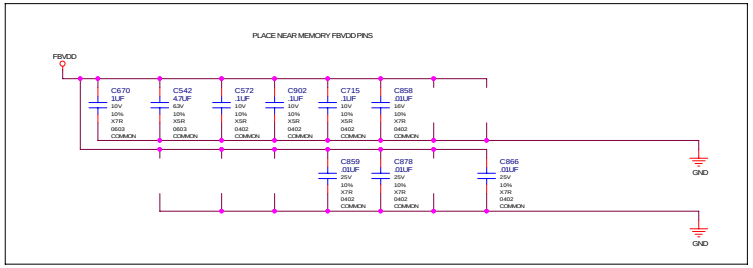
FRAME BUFFER: PARTITION A DECOUPLING

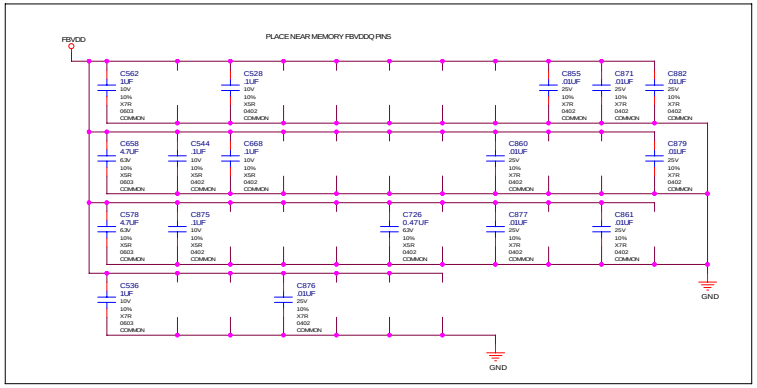
Decoupling for FBA 0..31





Decoupling for FBA 32..63





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

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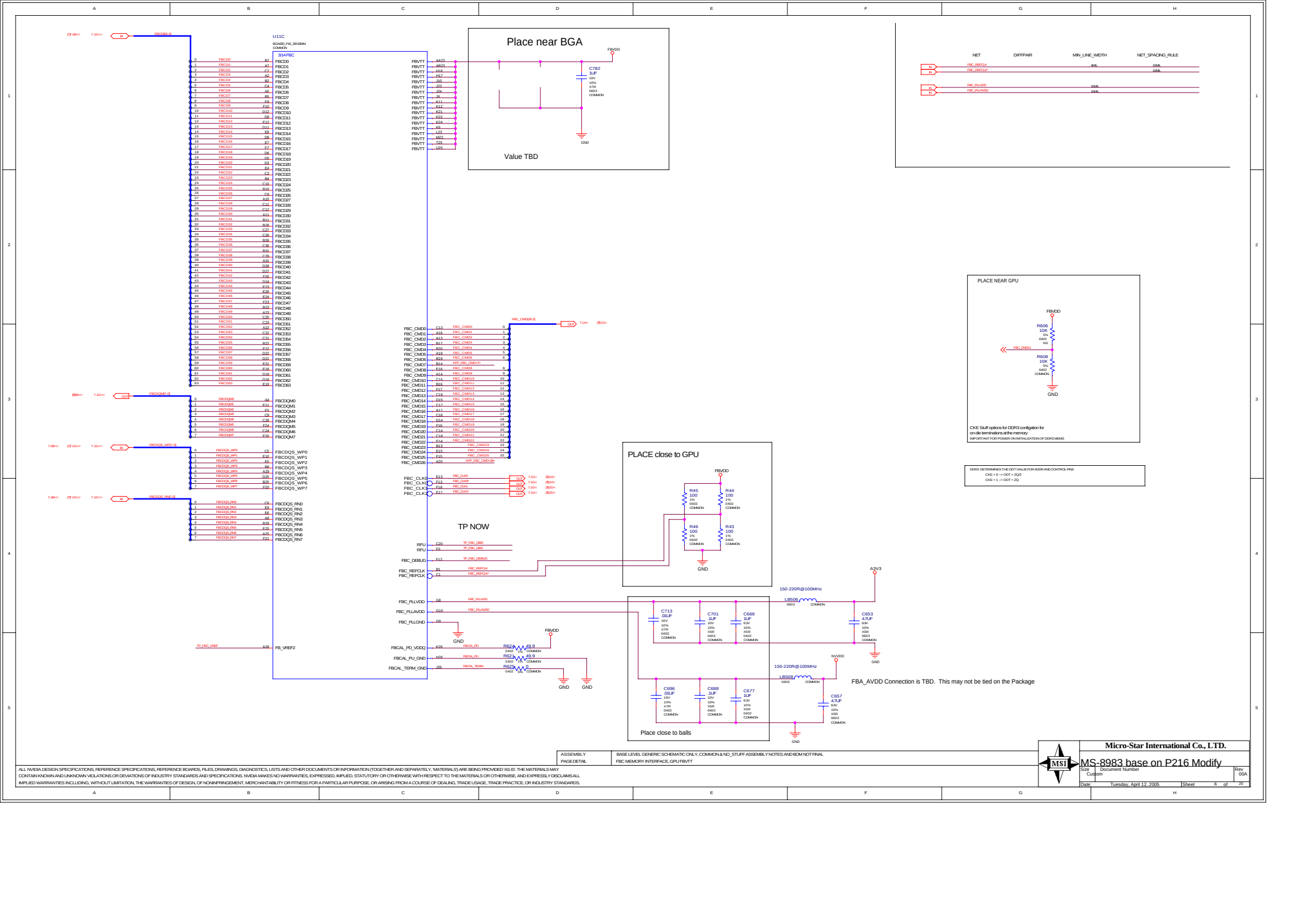

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY INTERFACE, GPU FBVTT

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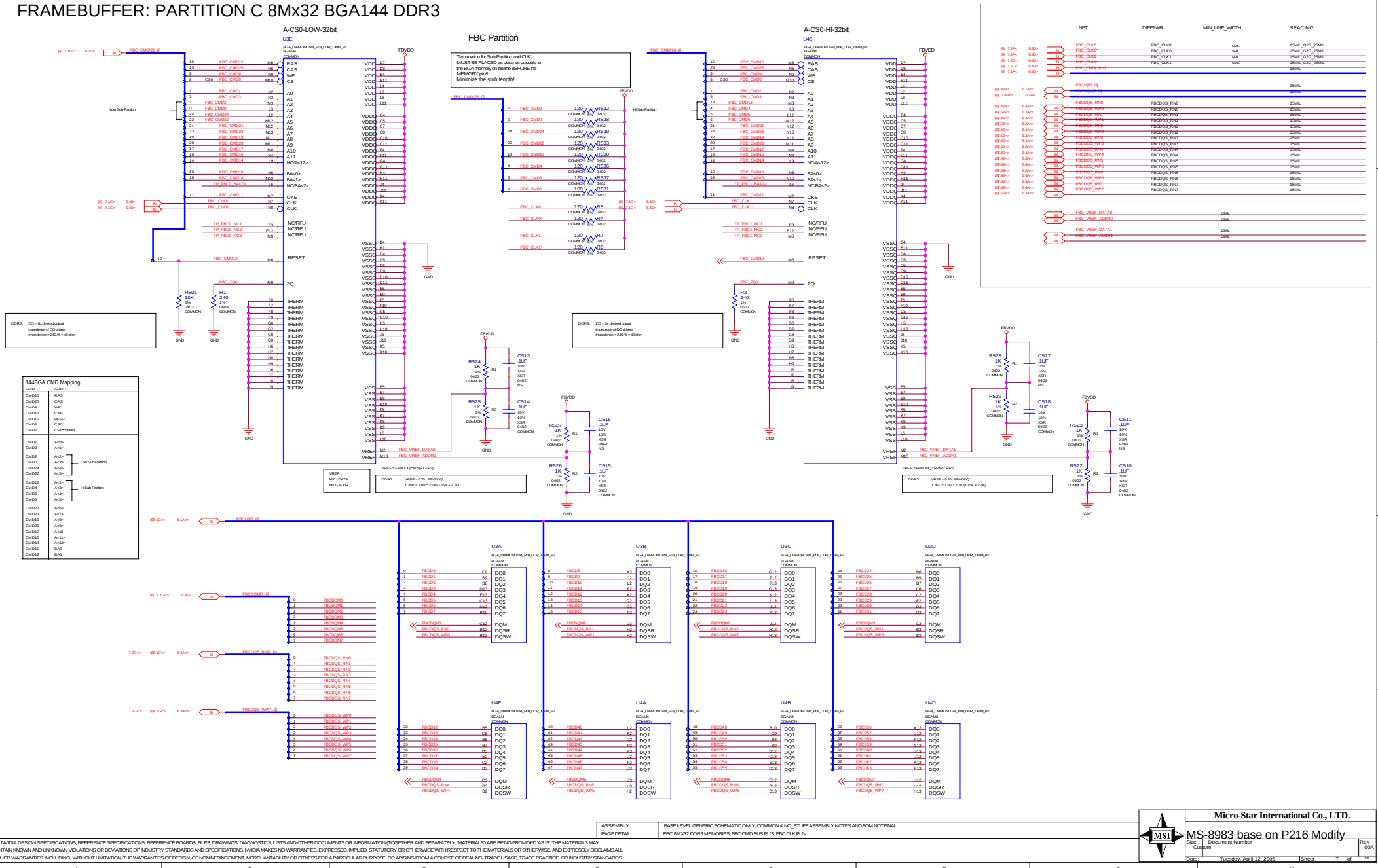
FRAMEBUFFER: PARTITION C 8Mx32 BGA144 DDR3



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 8MX32 DDR3 MEMORIES, FBC CMD BUS PUS, FBC CLK PUs

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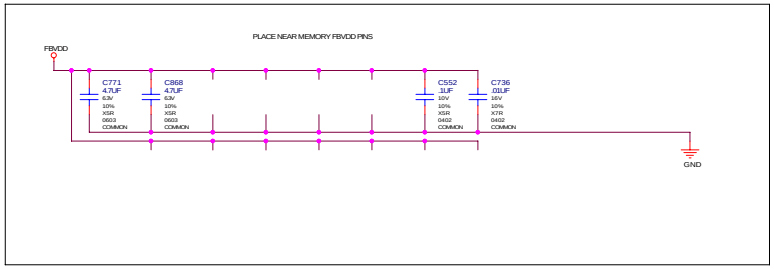
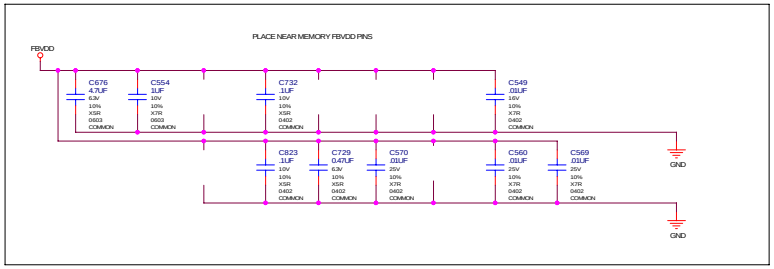
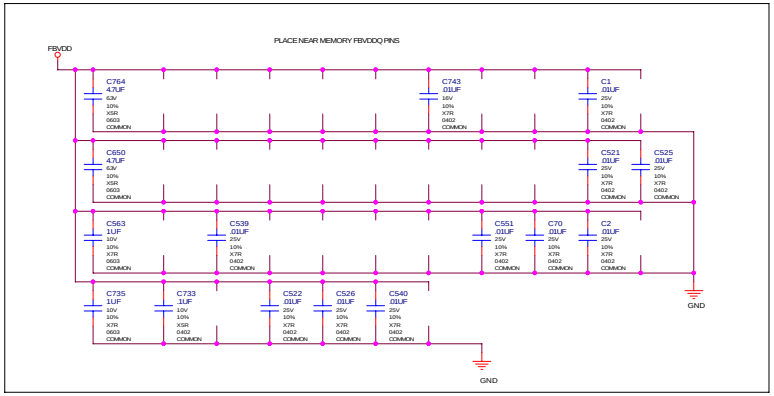
FRAMEBUFFER: PARTITION C DECOUPLING

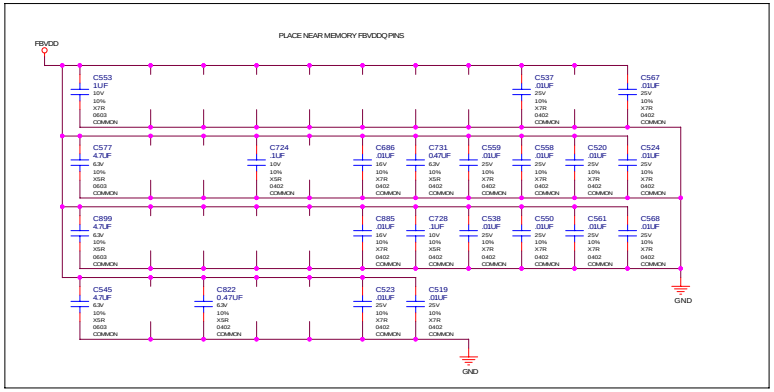
Decoupling for FBC 0..31

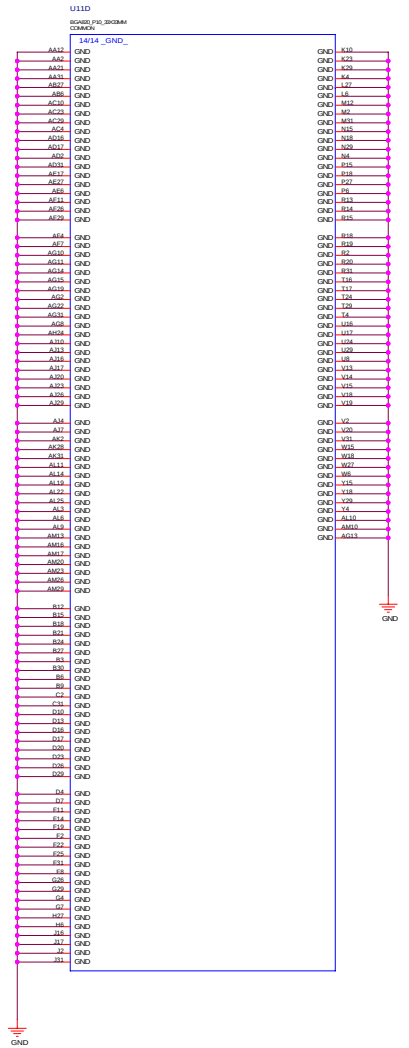


Decoupling for FBC 32..63









ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDD/Q DECOUPLING CAPS, GPU GND CONNECTIONS

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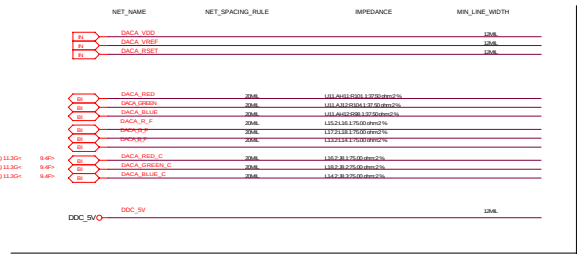
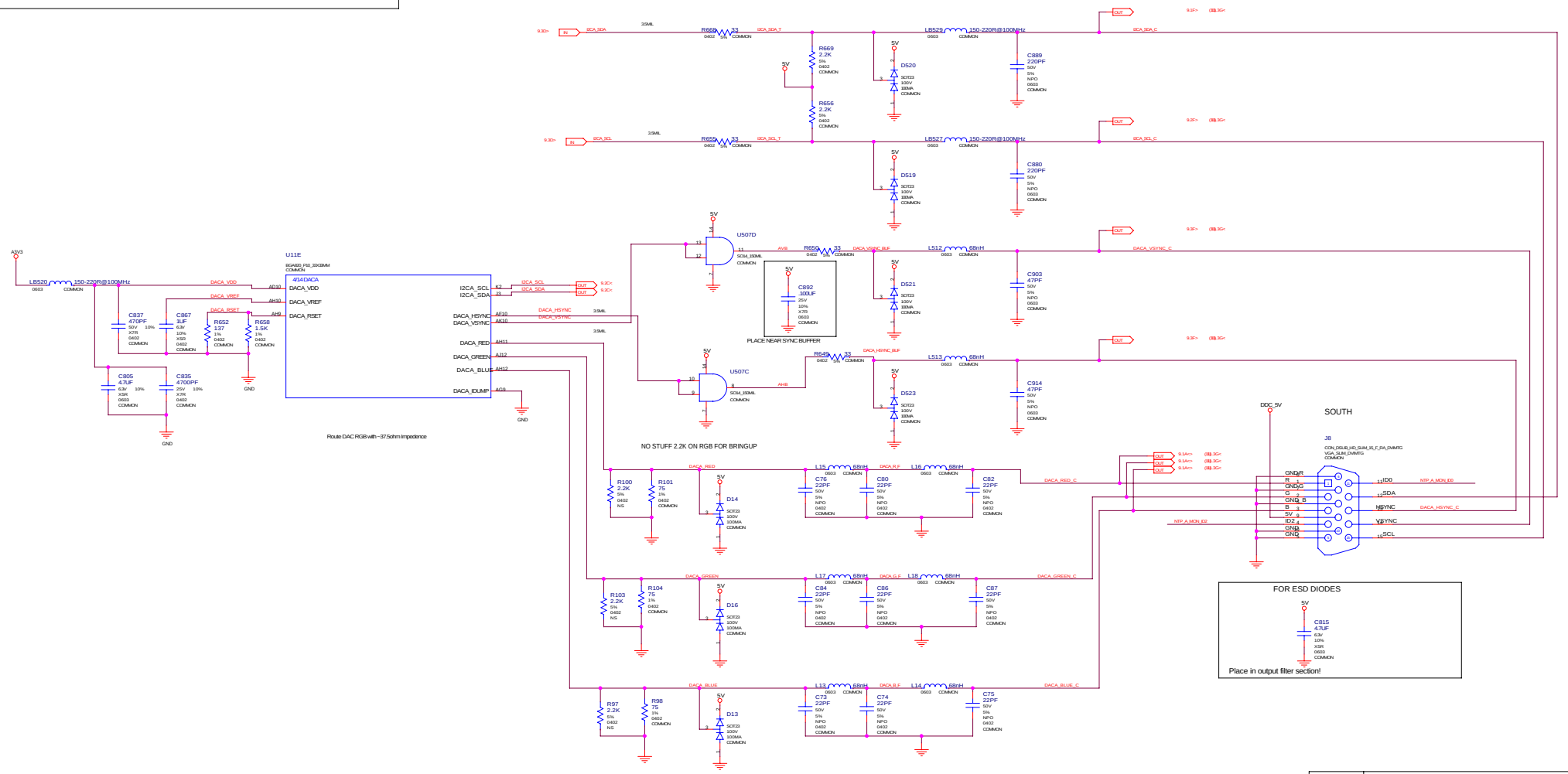
Primary Display (DACA), Slim DB15

DACA RGB-FILTER





ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL

PAGE DETAIL: DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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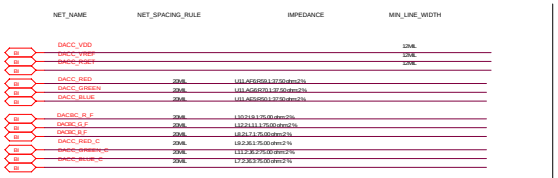
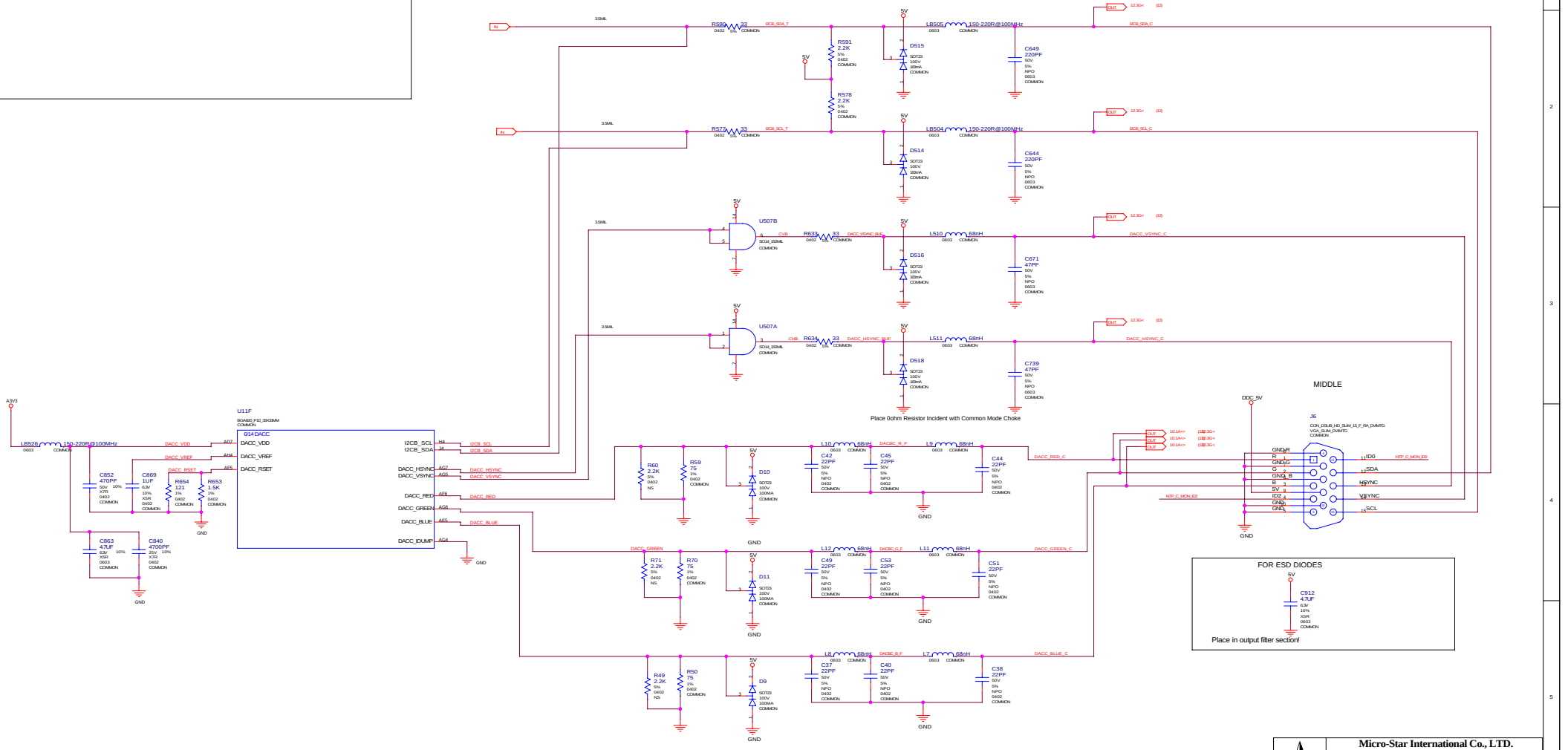
Secondary Display (DACC), Slim DB15

DACC RGB-FILTER





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MID

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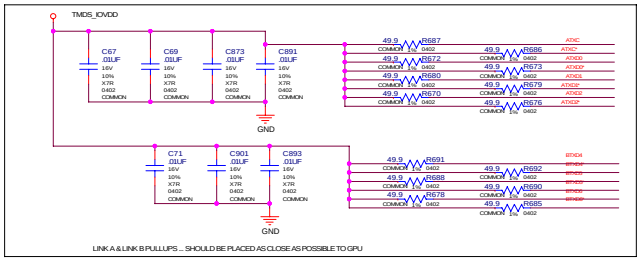
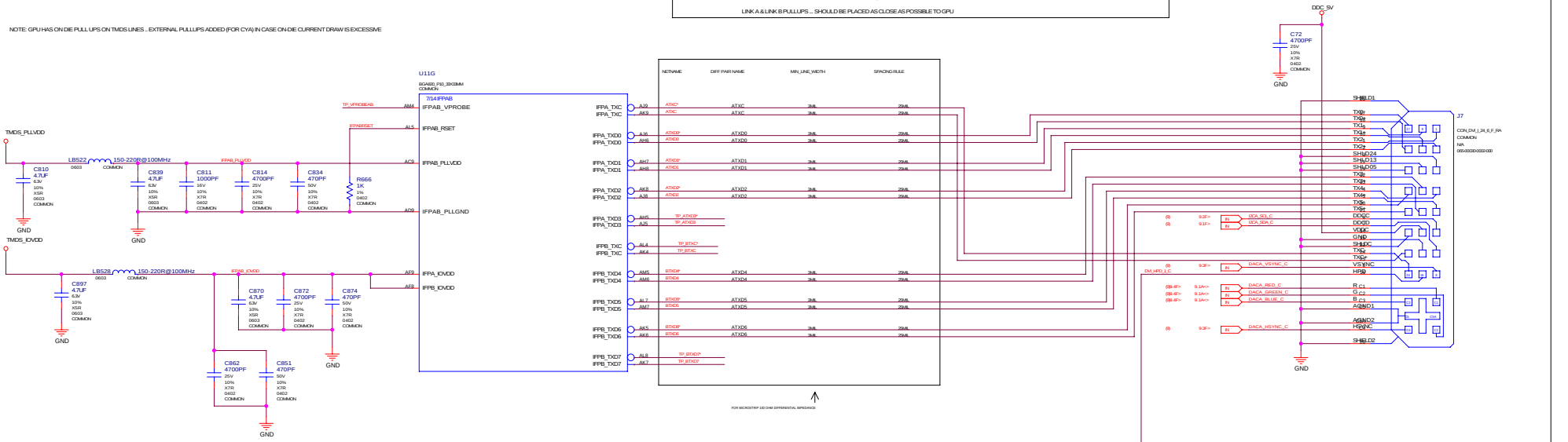
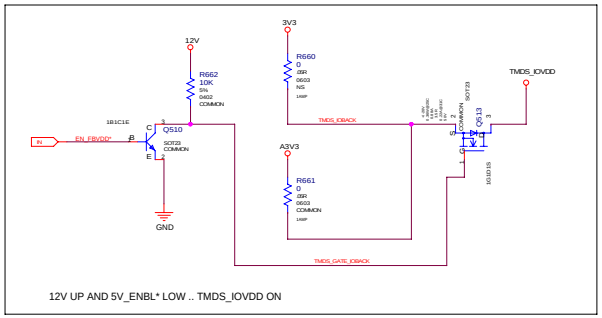
INTERNAL TMDS .. LINK A & B



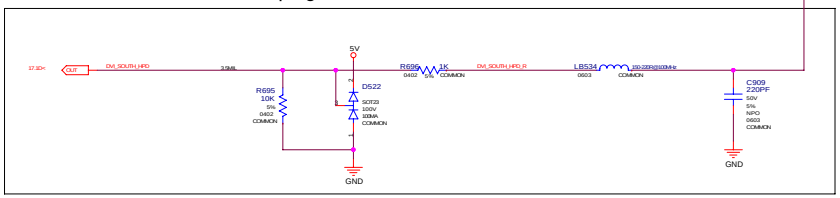
NOTE: GPU HAS ON DIE PULL UPS ON TMDS LINES .. EXTERNAL PULLUPS ADDED (FOR CYA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE

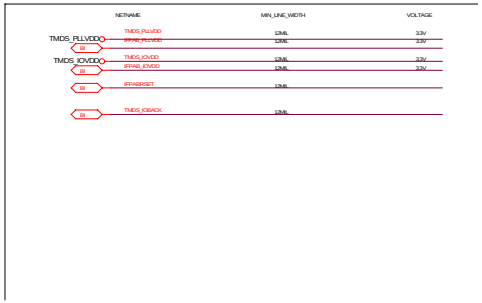


TMDS_IOVDD BACKDRIVE PREVENTION



Hotplug Detection





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK A/B & PUs, TMDS IO BACKDRIVE PREVENTION,DVI CONNECTOR SOUTH

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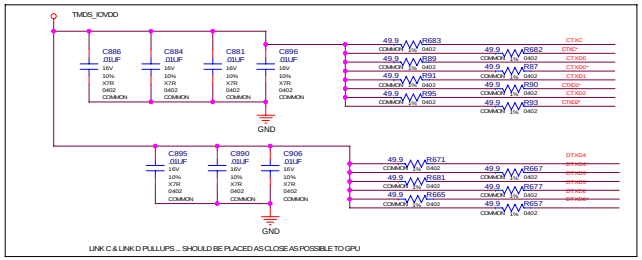
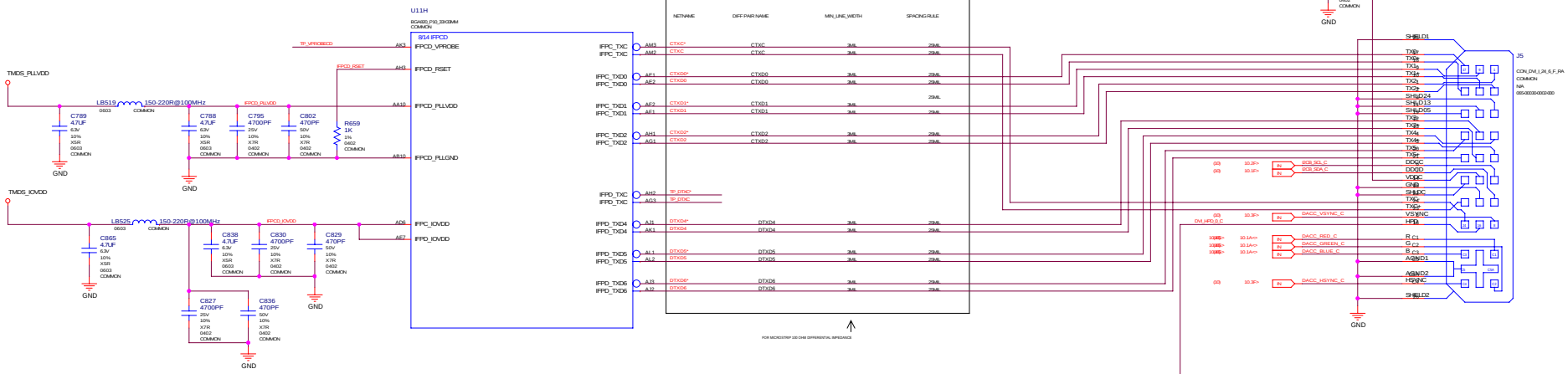
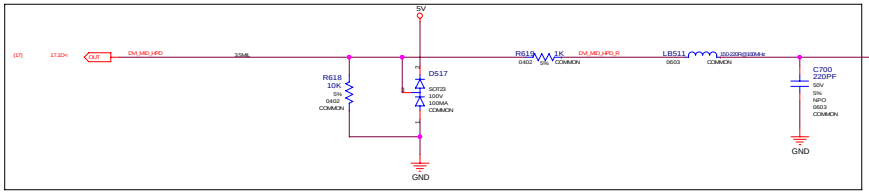
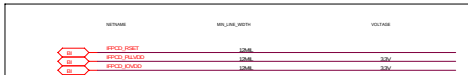
INTERNAL TMDS .. LINK C & D





Hotplug Detection





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK C/D & PLs,DVI CONNECTOR MID

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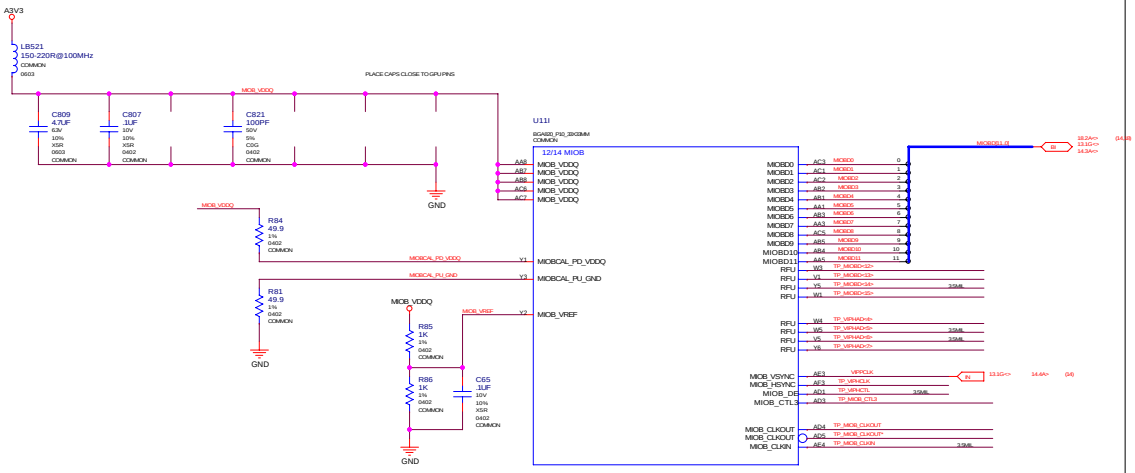
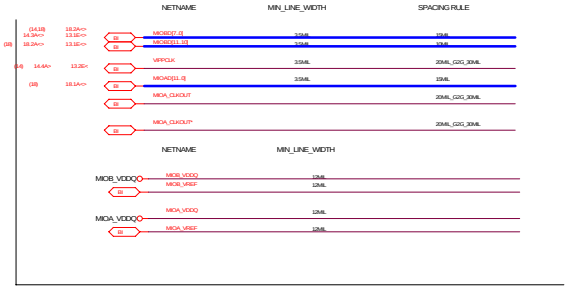
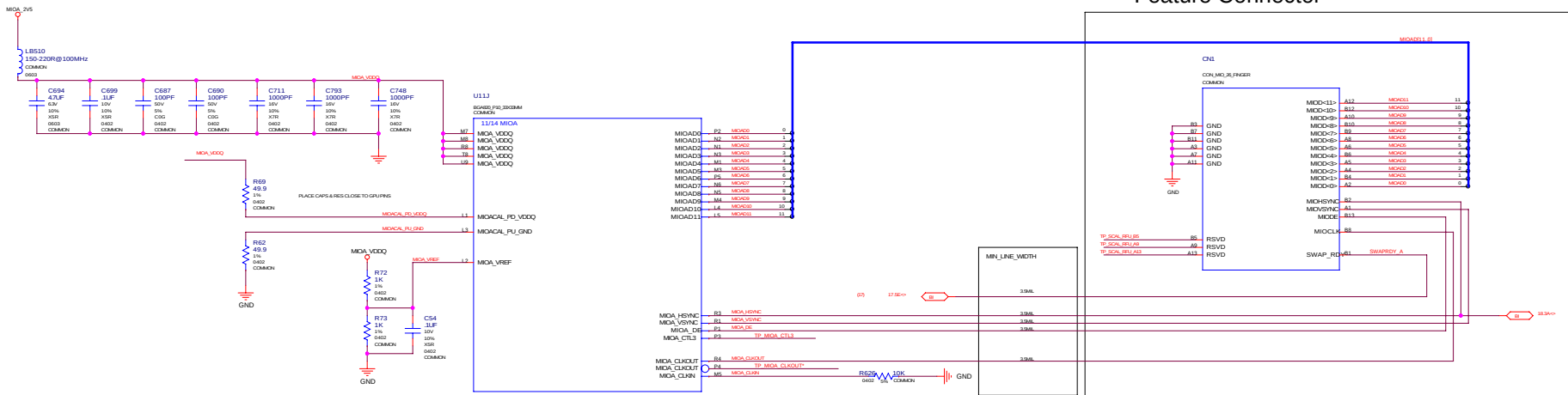
G3 VIP/MIOB





G3 MIOA



Feature Connector

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB, FEATURE CONNECTOR

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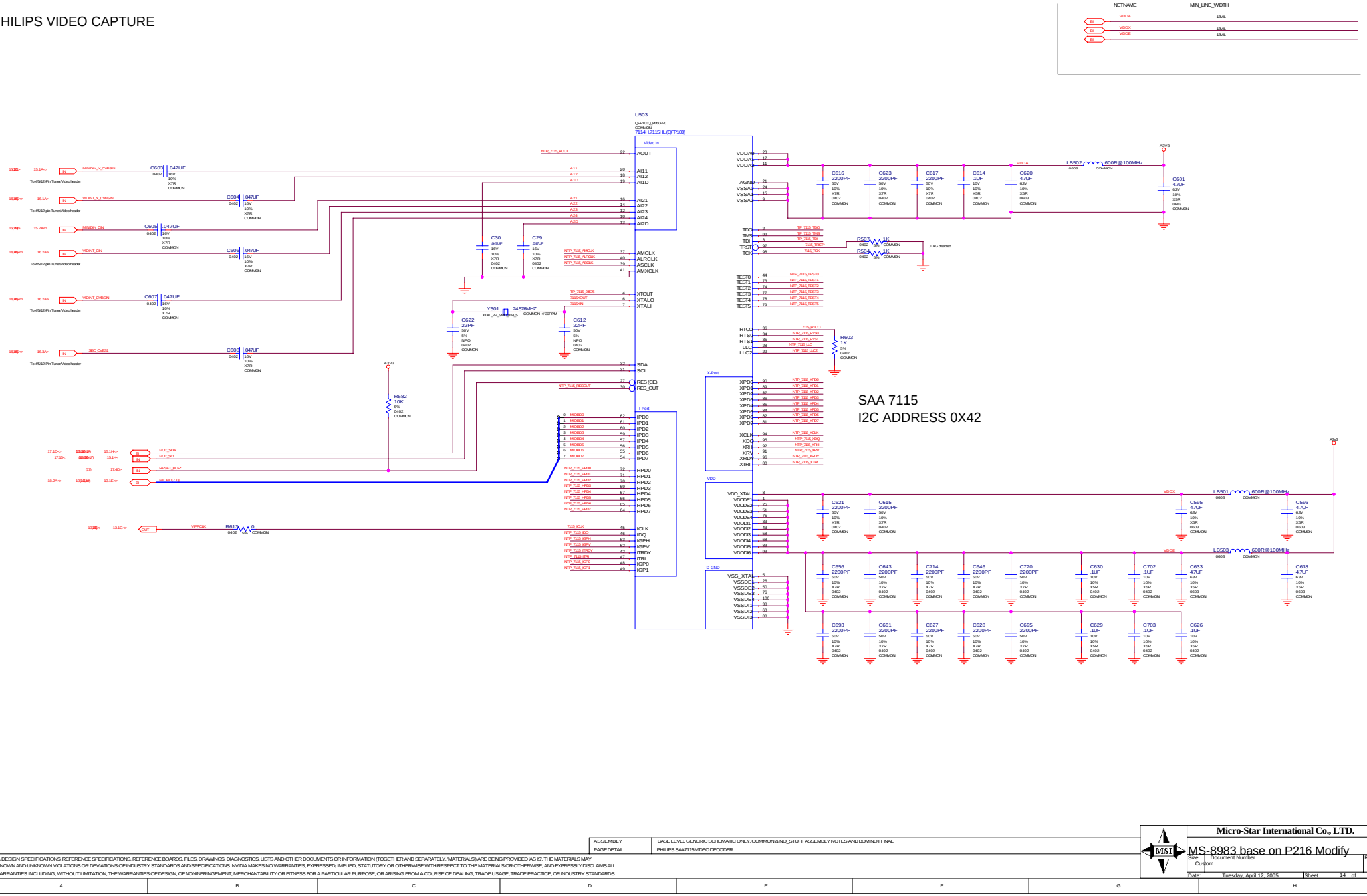
PHILIPS VIDEO CAPTURE



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PHILIPS SAA7115 VIDEO DECODER

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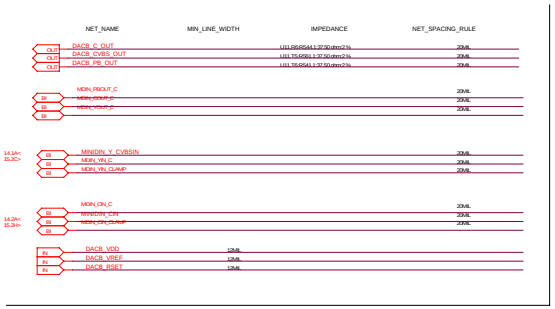
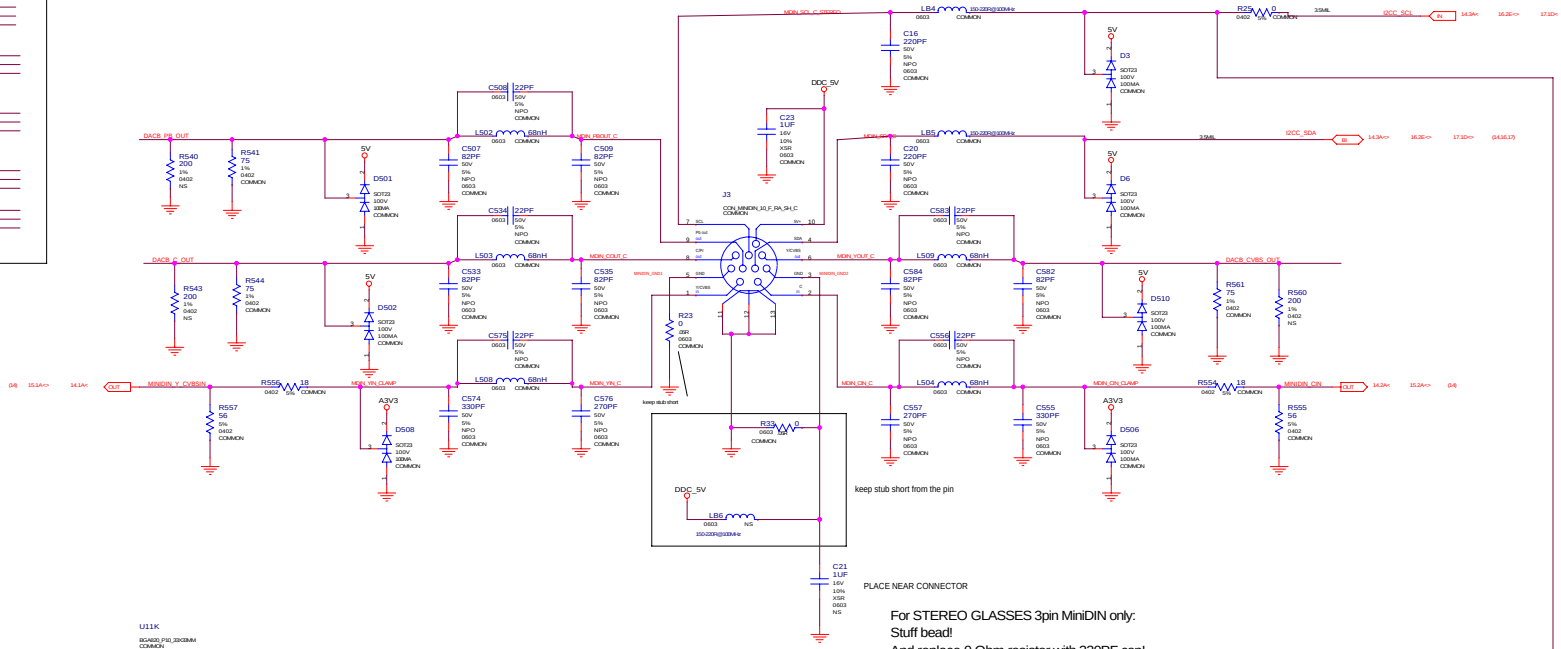
DACB .. MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES

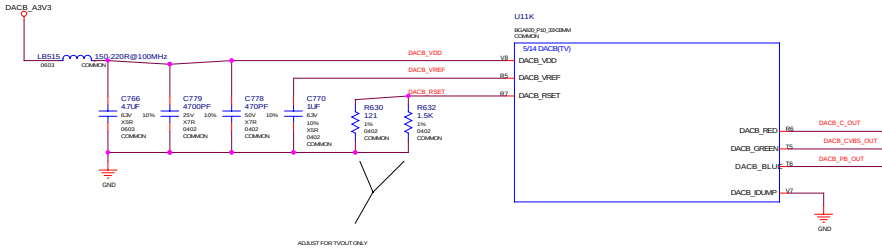


FILTER NOTES:

SD: USE L=1.8UH

HD: USE L=7

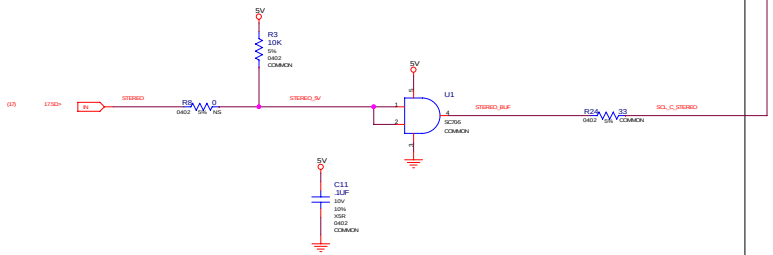




For STEREO GLASSES 3pin MiniDIN only:
Stuff bead!
And replace 0 Ohm resistor with 220PF cap!

STEREO GLASSES BUFFER

Place close to MiniDIN connector!



FOR DEBUG PURPOSES ONLY .. DEFAULT IS NO STUFF

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTERS, MINIDIN CONNECTOR NORTH

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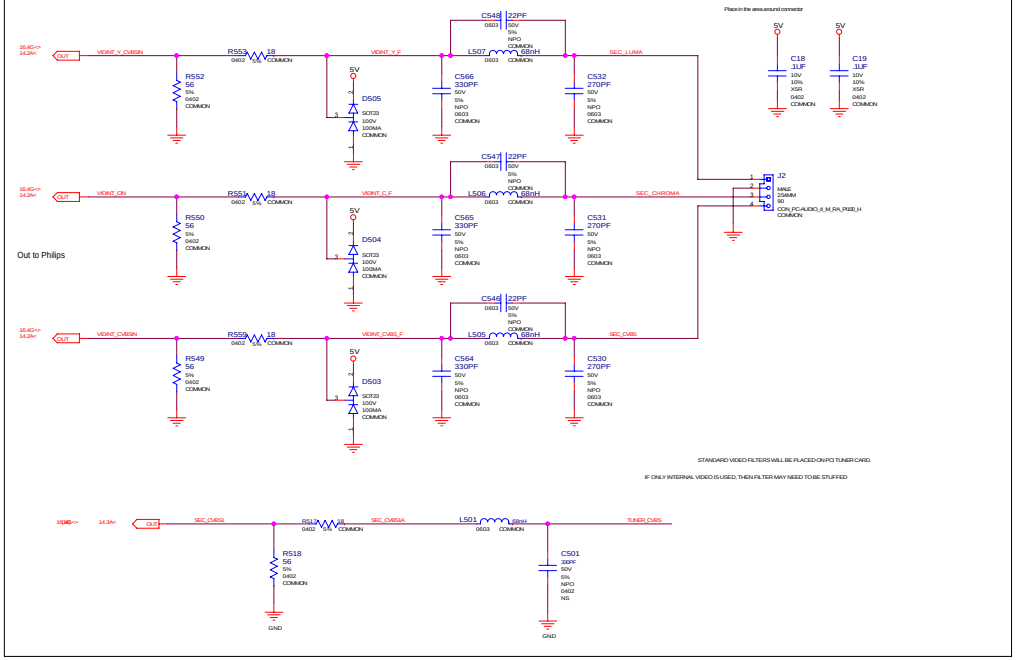
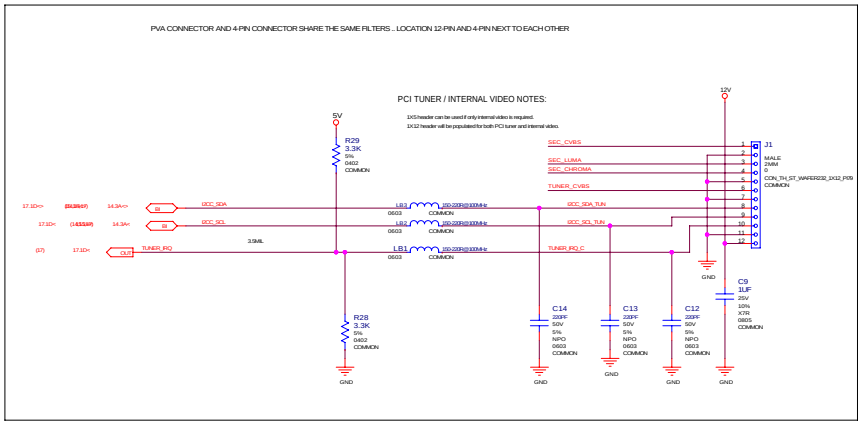
4-Pin Video In, 12-pin Video In connectors

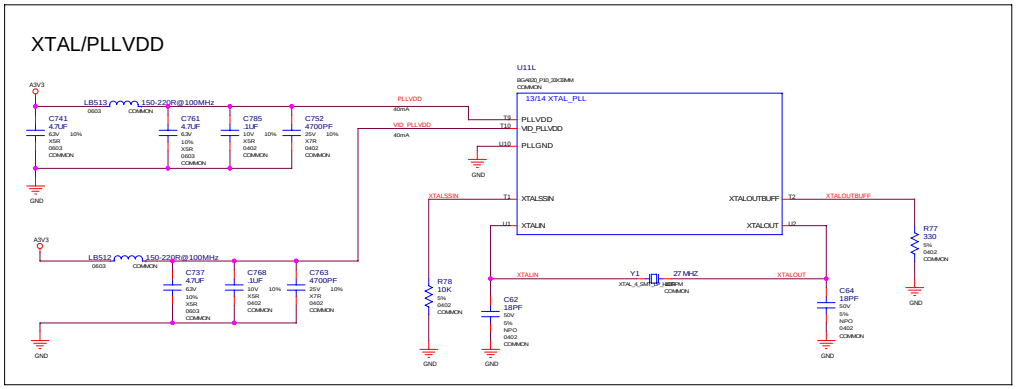
EXTERNAL 4-PIN VIDEO IN CONNECTOR

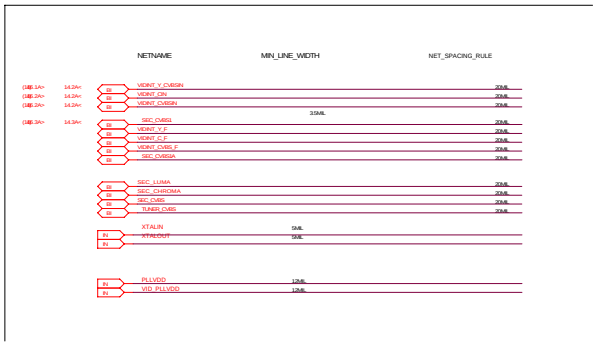


EXTERNAL 12-PIN PVA CONNECTOR



XTAL/PLLVDD





ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	4-PIN & 12-PIN VIDEO HEADERS, XTAL

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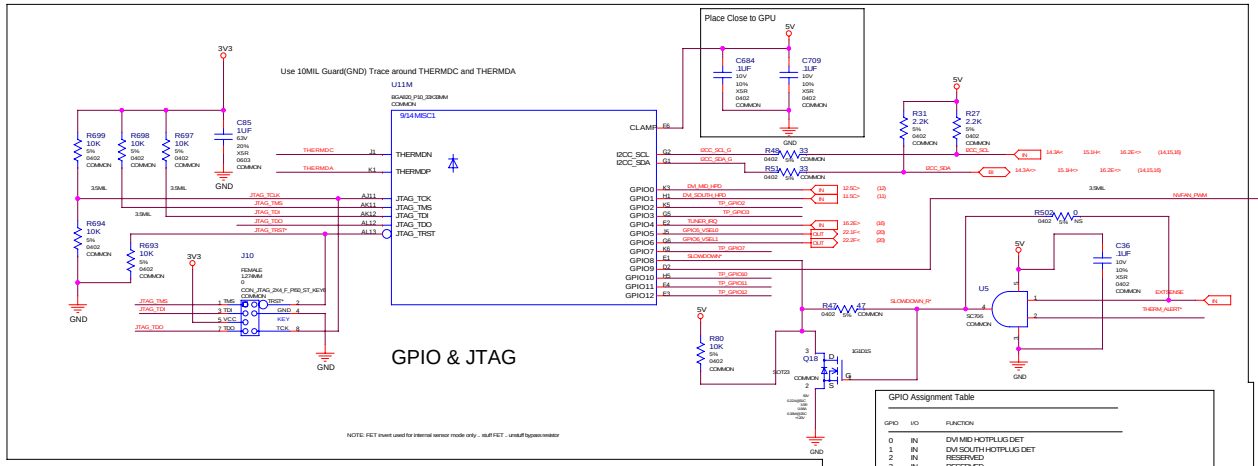
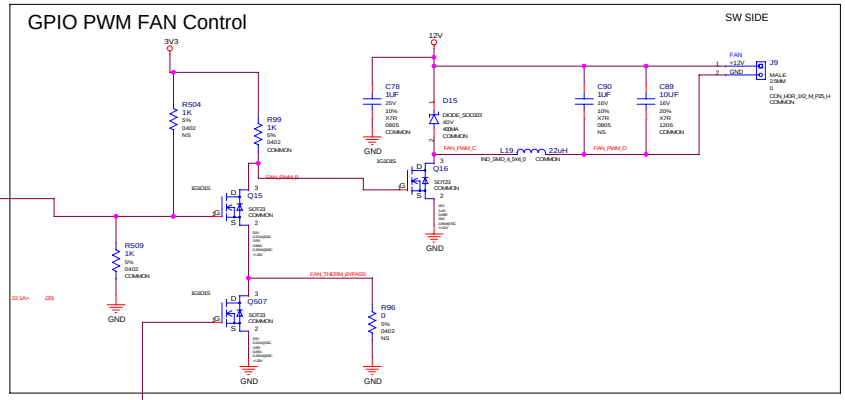
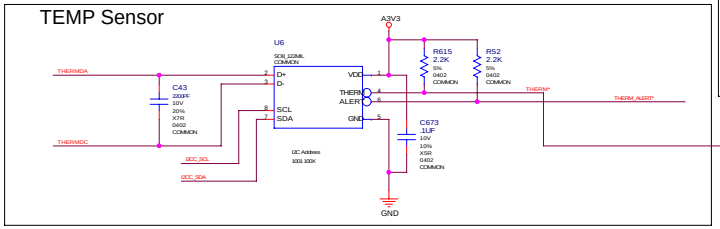
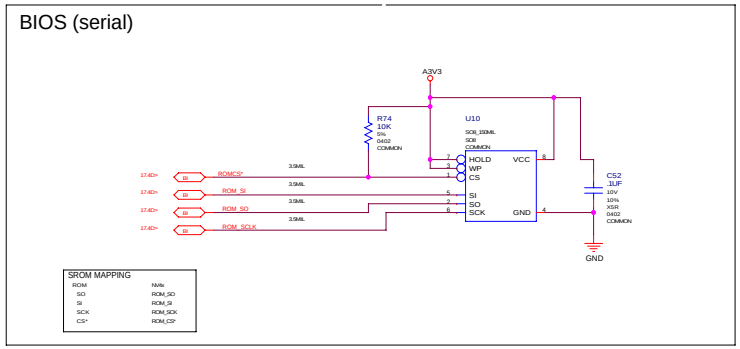
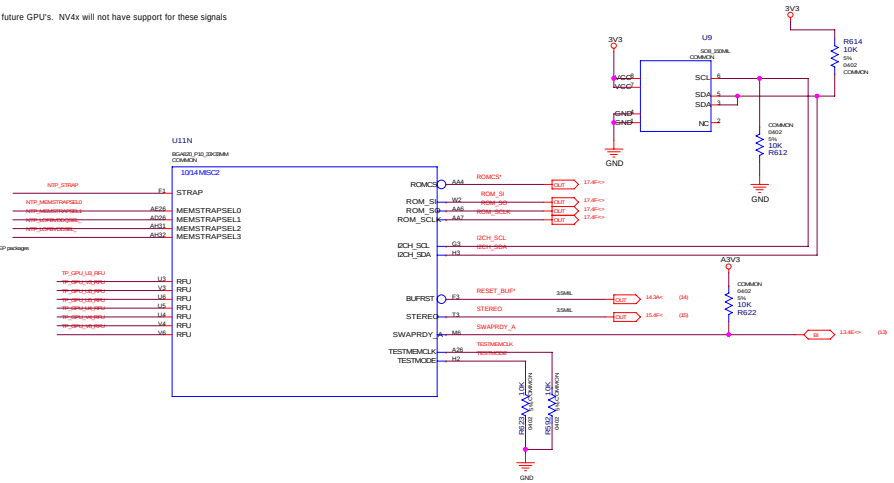








AUDIO and VIDEO signals are reserved for future GPU's. NV4x will not have support for these signals



NETNAME	MIN_LINE_WIDTH	VOLTAGE
THERMDC	10MIL	
THERMDA	10MIL	
FAN_PWM_B	12MIL	
FAN_PWM_C	12MIL	
FAN_PWM_D	12MIL	

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	JTAG, BIOS ROM, HDCP ROM, FAN CONTROL, TEMP SENSOR & GPIO's

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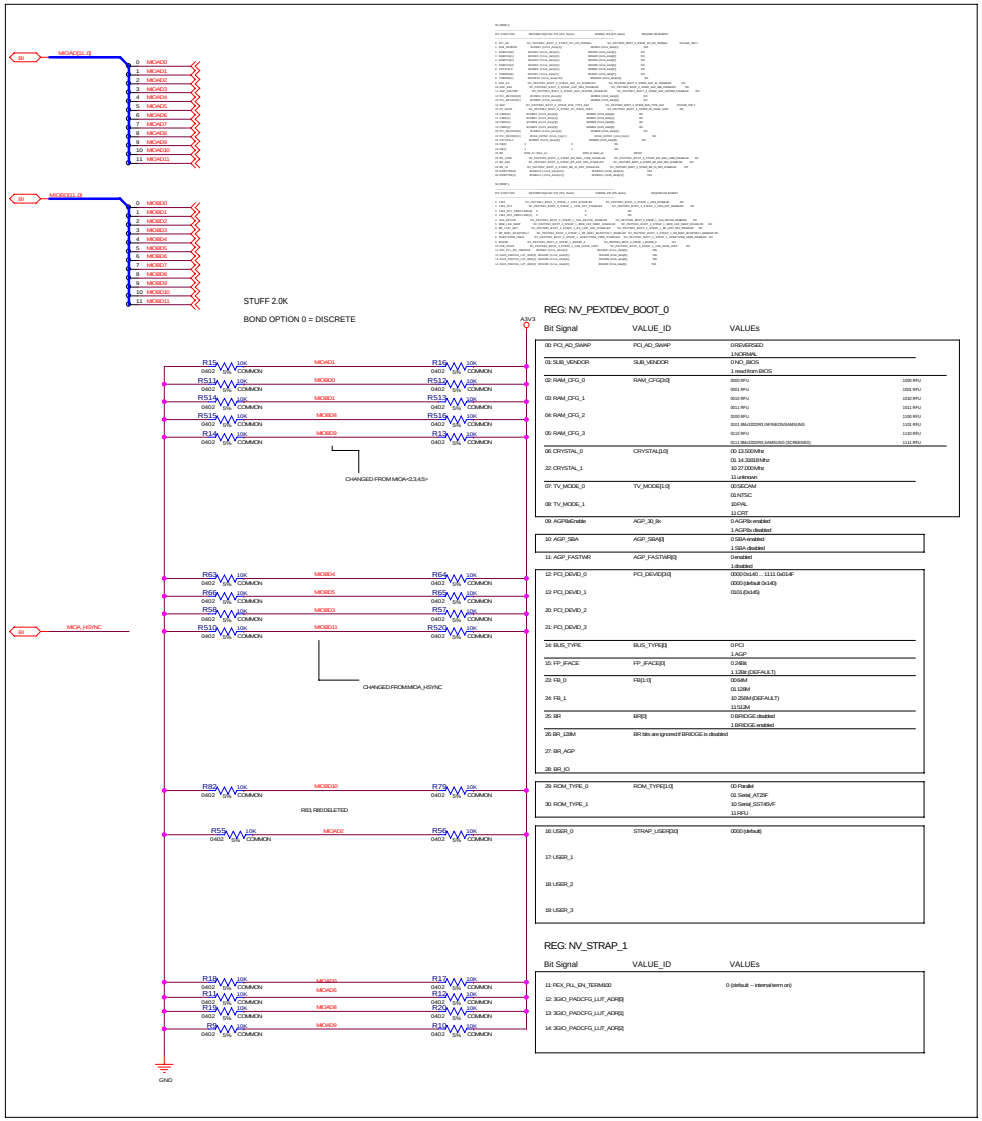
BIOS, Straps, Misc

Straps

Assembly: BIOS



REG: NV_PEXTDEV_BOOT_0

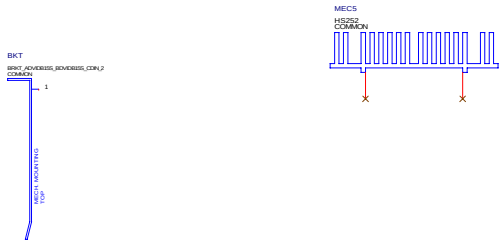
Bit	Signal	VALUE_ID	VALUEs
00	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED 1 NORMAL
01	SUB_VENDOR	SUB_VENDOR	0 NO_BIOS 1 read from BIOS
02	RAM_CFG_0	RAM_CFG[3:0]	0000 RFU 0001 RFU 0010 RFU 0011 RFU 0100 RFU 0101 8Mx32DDR1/NP/NEC/SAMSUNG 0110 RFU 0111 8Mx32DDR1/SAMSUNG (SCREENED)
03	RAM_CFG_1		1000 RFU 1001 RFU 1010 RFU 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 RFU
04	RAM_CFG_2		
05	RAM_CFG_3		
06	CRYSTAL_0	CRYSTAL[1:0]	00 13.500Mhz 01 14.318180Mhz 10 27.000Mhz 11 unknown
07	TV_MODE_0	TV_MODE[1:0]	00 SECAM 01 NTSC
08	TV_MODE_1		10 PAL 11 CRT
09	AGPSBAEnable	AGP_30_8x	0 AGPSb enabled 1 AGPSb disabled
10	AGP_SBA	AGP_SBA[0]	0 SBA enabled 1 SBA disabled
11	AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled
12	PCI_DEVID_0	PCI_DEVID[5:0]	000000-b40 ... 1111 0x14F 0000 (default 0x140)
13	PCI_DEVID_1		0101 (0x145)
20	PCI_DEVID_2		
21	PCI_DEVID_3		
14	BUS_TYPE	BUS_TYPE[0]	0 PCI 1 AGP
15	FP_IFACE	FP_IFACE[0]	0 24bit 1 12bit (DEFAULT)
23	FB_0	FB[1:0]	00 64M 01 128M
24	FB_1		10 256M (DEFAULT) 11 512M
25	BR	BR[0]	0 BRIDGE disabled 1 BRIDGE enabled
26	BR_128M	BR bits are ignored if BRIDGE is disabled	
27	BR_AGP		
28	BR_IO		
29	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F
30	ROM_TYPE_1		10 Serial_SST45VF 11 RFU
16	USER_0	STRAP_USER[3:0]	0000 (default)
17	USER_1		
18	USER_2		
19	USER_3		

REG: NV_STRAP_1

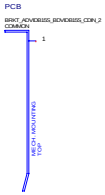
Bit	Signal	VALUE_ID	VALUEs
11	PEX_PLL_EN_TERM100		0 (default – internal term on)
12	3GIO_PADCFG_LUT_ADR[0]		
13	3GIO_PADCFG_LUT_ADR[1]		
14	3GIO_PADCFG_LUT_ADR[2]		

Mechanical parts

NEED FANSINK SYMBOL FOR P216



155-00002-0000-000 SCREW PHIL PAN HD SS MACH 4-40 3/16



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS STRAPS & MECHANICALS

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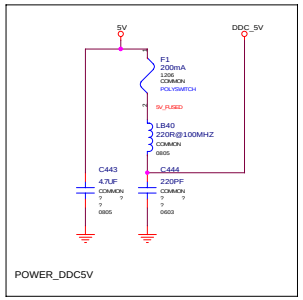
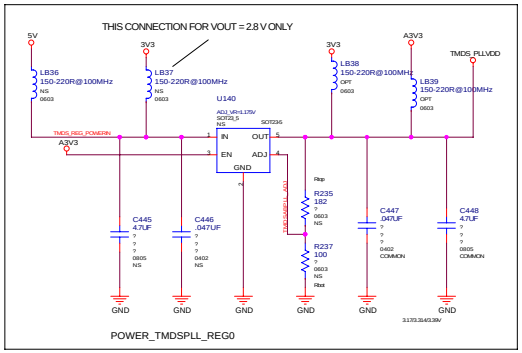
Power Supply ... TMDS/A3V3/FBVDD

DDC 5V

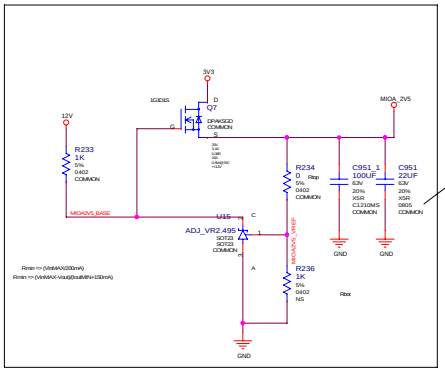


TMDS AB/CD PLL Supply



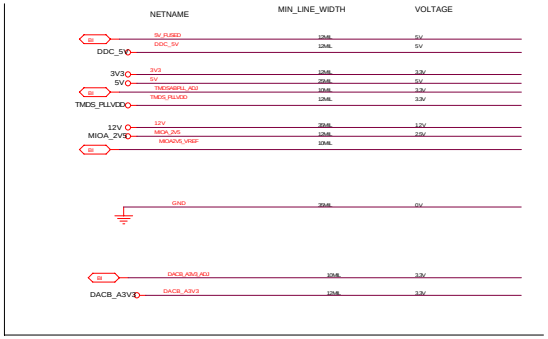
Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+(100/182))

MIOA_VDDQ

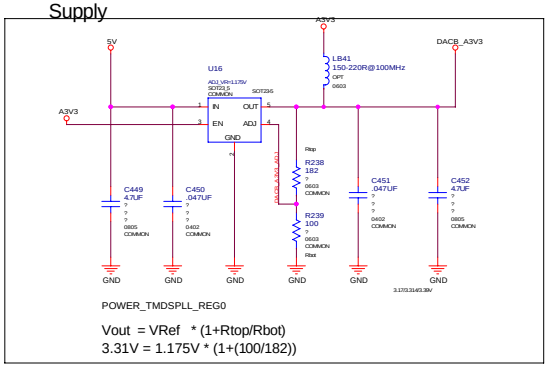


CHANGED TO 22UF FROM 1UF

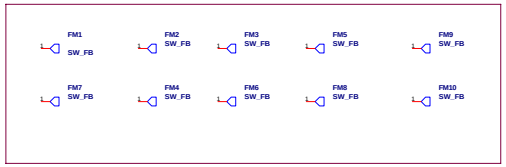
Vref = 2.5V
Vout = 2.495(1+Rtop/Rbot) + (Iref + Rtop)
For Vout = Vref (Rtop = 0ohm, Rbot = NO STUFF)



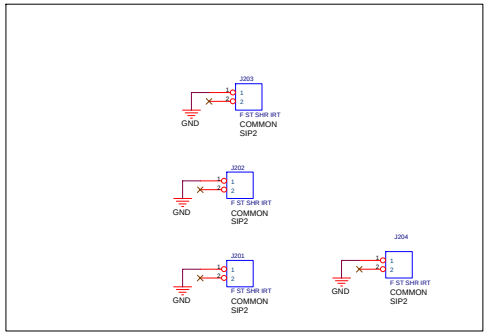
DACB Supply



Vout = VRef * (1+Rtop/Rbot)
3.31V = 1.175V * (1+(100/182))



Fiducial Point



Test point

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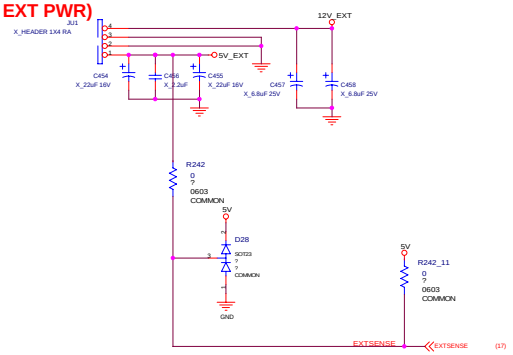
ISL6549 for Nvidia NV4x Graphic card power ckt

Add External Power Connector



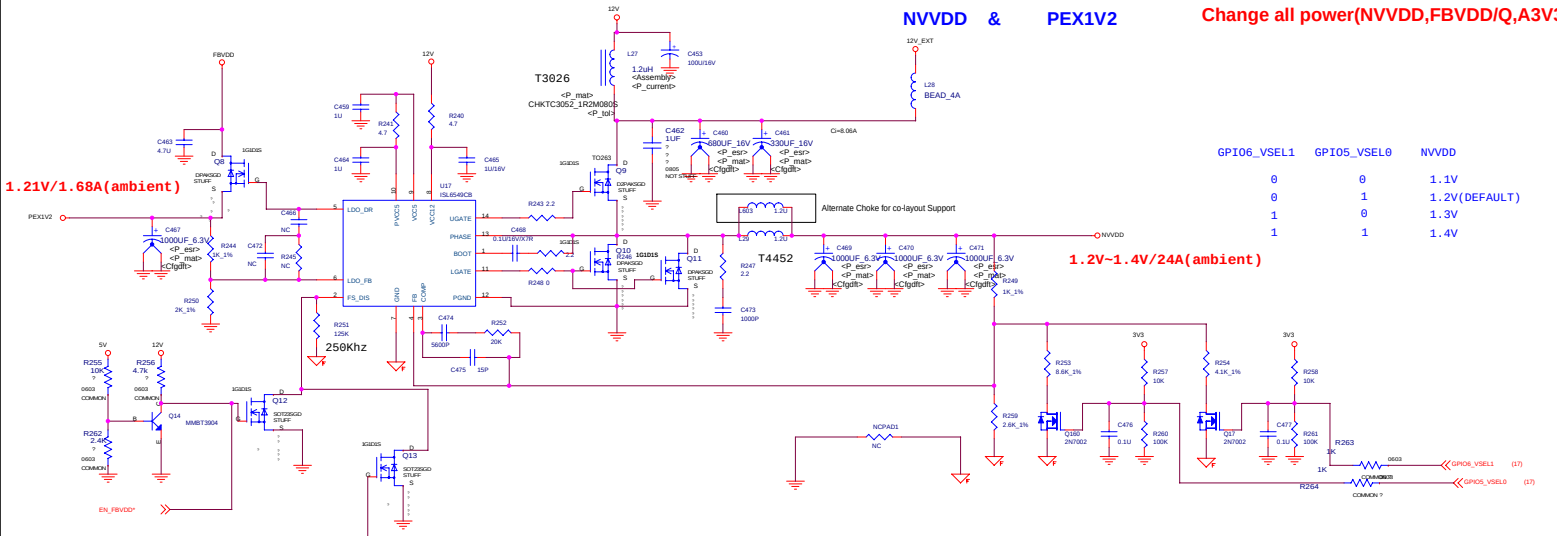
NVVDD & PEX1V2

Change all power(NVVDD,FBVDD/Q,A3V3,5V & ADD EXT PWR)

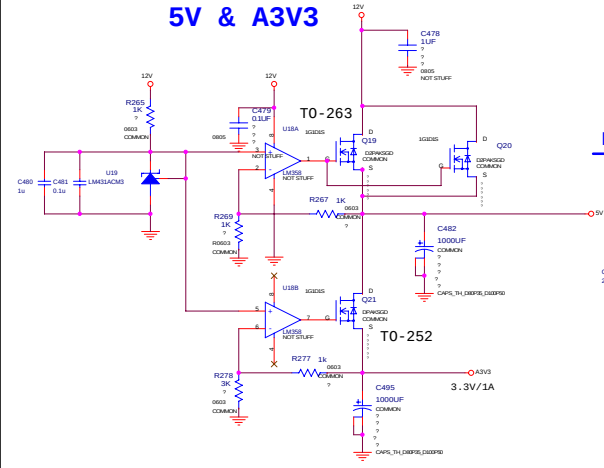
GPIO6_VSEL1	GPIO5_VSEL0	NVVDD
0	0	1.1V
0	1	1.2V(DEFAULT)
1	0	1.3V
1	1	1.4V

1.21V/1.68A(ambient)

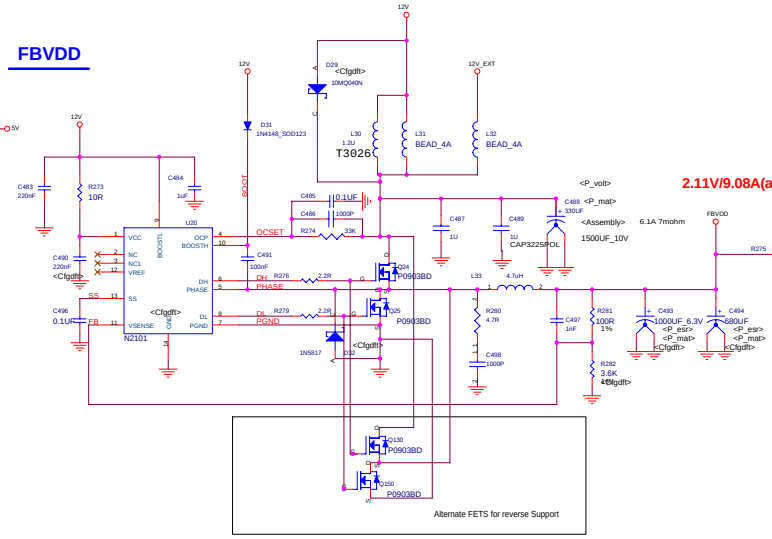
1.2V~1.4V/24A(ambient)



5V & A3V3

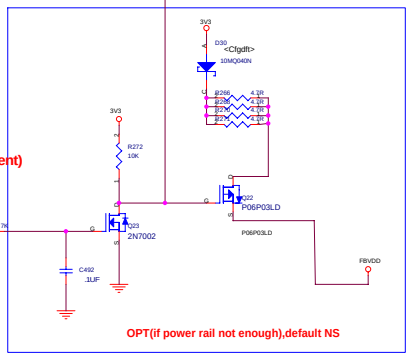


FBVDD



PWR current share for FBVDD

2.11V/9.08A(ambient)



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