

C116-B, NV18B/NV31/NV34, 8MX16DDR, 128MB, Video IN/OUT, DVI-I, VGA

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A00
B00

HISTORY:

A00: INITIAL VERSION
B00: ADD A.T.E. TEST POINTS
ADD CIRCUIT TO SUPPORT NV31/NV34
CONNECT W83785(U90 0) TO VGA THERMDA/C

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Rev.

00B

Doc. Name

TOP PAGE

Date

Friday, February 14, 2008

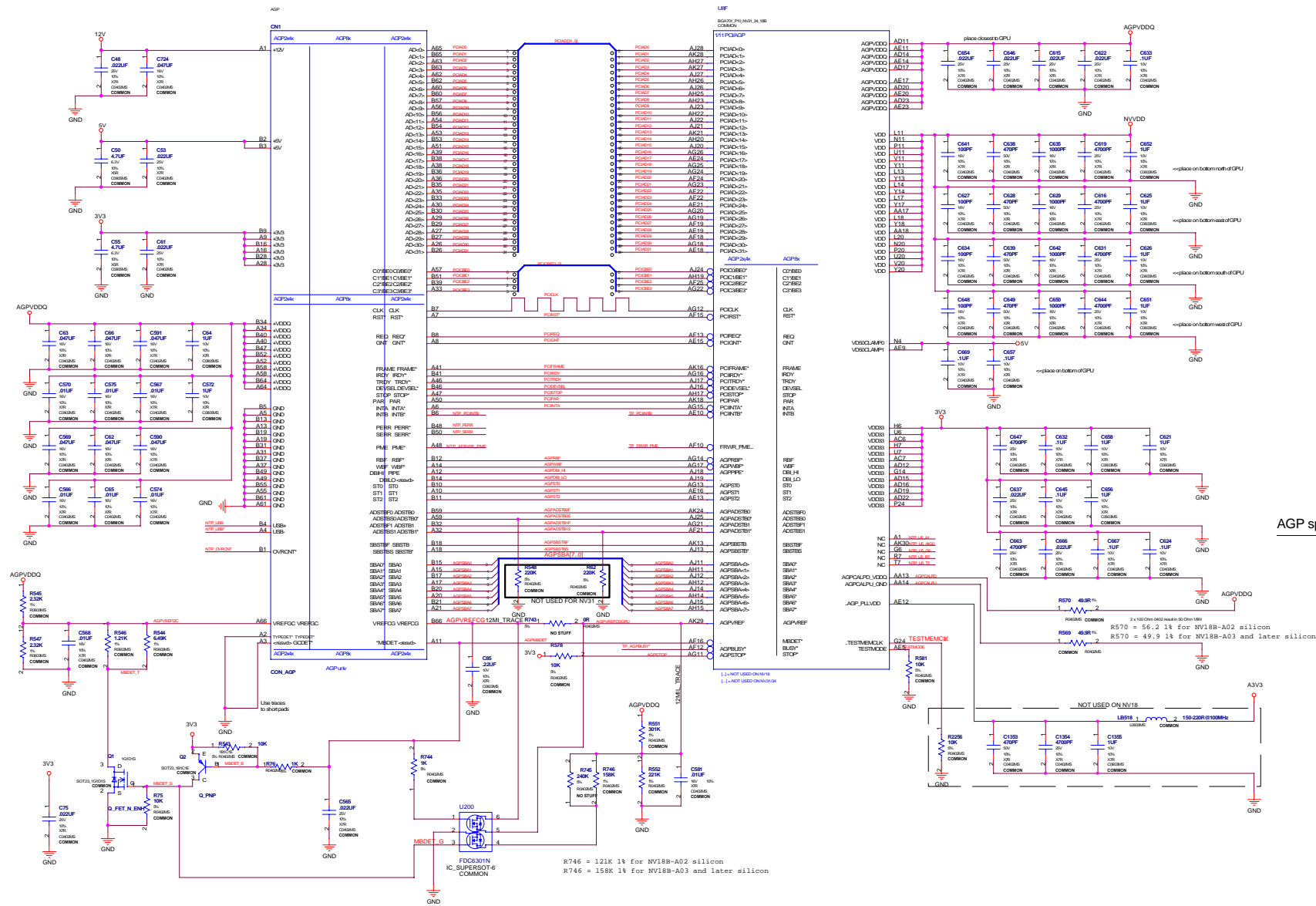
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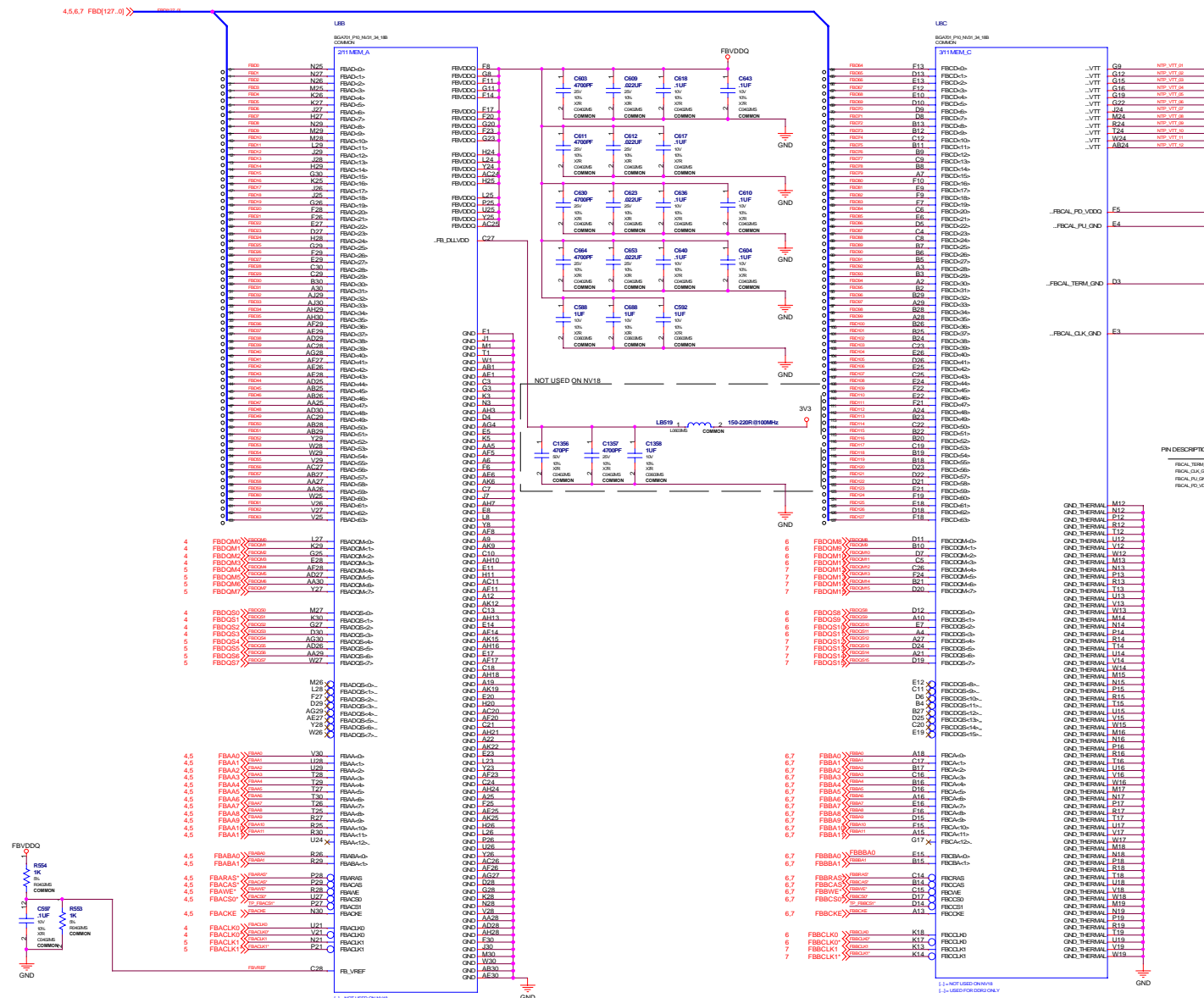
NV18 AGP SECTION AND AGP CONNECTOR



AGP spacing rules

Component	Value
AGP_VDDQ	100nF
AGP_VDD	100nF
AGP_A	100nF
AGP_B	100nF
AGP_C	100nF
AGP_D	100nF
AGP_E	100nF
AGP_F	100nF
AGP_G	100nF
AGP_H	100nF
AGP_I	100nF
AGP_J	100nF
AGP_K	100nF
AGP_L	100nF
AGP_M	100nF
AGP_N	100nF
AGP_O	100nF
AGP_P	100nF
AGP_Q	100nF
AGP_R	100nF
AGP_S	100nF
AGP_T	100nF
AGP_U	100nF
AGP_V	100nF
AGP_W	100nF
AGP_X	100nF
AGP_Y	100nF
AGP_Z	100nF

NV18 FRAMEBUFFER INTERFACE AND DECOUPLING



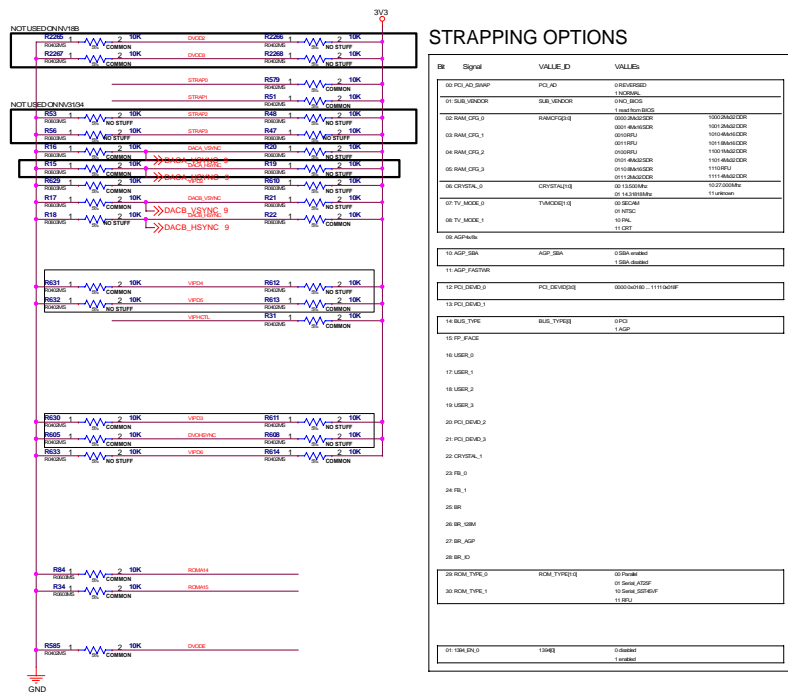
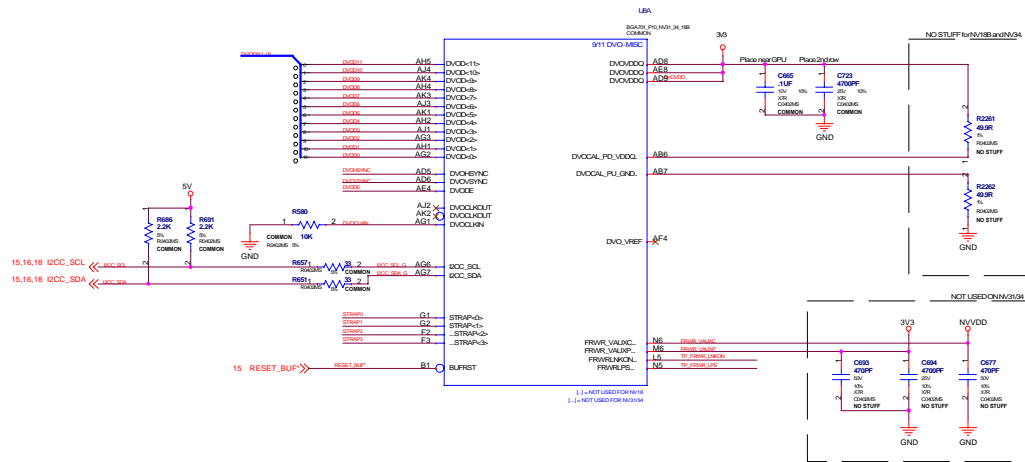
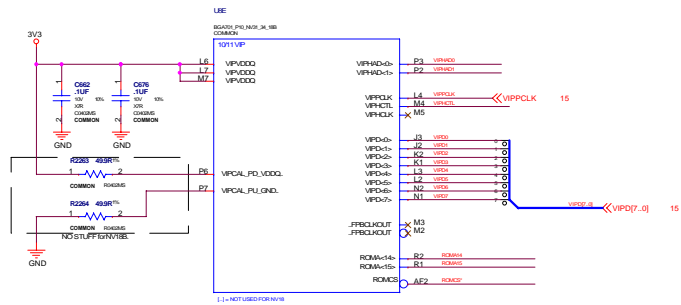
PIN DESCRIPTION	NV18B	N31	N34
RIBCAL_TERM_GND	NOT USED	TIE TO GND	NOT USED
RIBCAL_CLK_GND	NOT USED	50 OHM 1% TO GND	NOT USED
RIBCAL_PU_GND	NOT USED	50 OHM 1% TO GND	50 OHM 1% TO GND
RIBCAL_PD_VDDQ	NOT USED	50 OHM 1% TO FBVDDQ	50 OHM 1% TO FBVDDQ

QND-THERMAL_M12
QND-THERMAL_M13
QND-THERMAL_P12
QND-THERMAL_P13
QND-THERMAL_T12
QND-THERMAL_T13
QND-THERMAL_V12
QND-THERMAL_V13
QND-THERMAL_M14
QND-THERMAL_M15
QND-THERMAL_P14
QND-THERMAL_P15
QND-THERMAL_T14
QND-THERMAL_T15
QND-THERMAL_V14
QND-THERMAL_V15
QND-THERMAL_M16
QND-THERMAL_M17
QND-THERMAL_P16
QND-THERMAL_P17
QND-THERMAL_T16
QND-THERMAL_T17
QND-THERMAL_V16
QND-THERMAL_V17
QND-THERMAL_M18
QND-THERMAL_M19
QND-THERMAL_P18
QND-THERMAL_P19
QND-THERMAL_T18
QND-THERMAL_T19
QND-THERMAL_V18
QND-THERMAL_V19

100

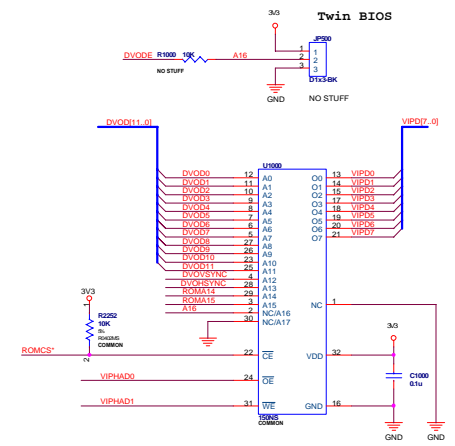
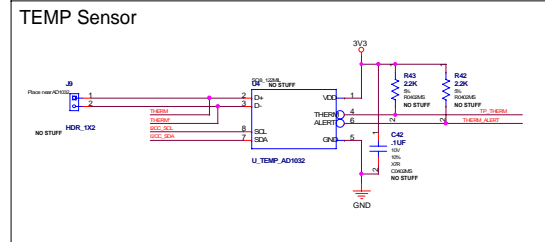
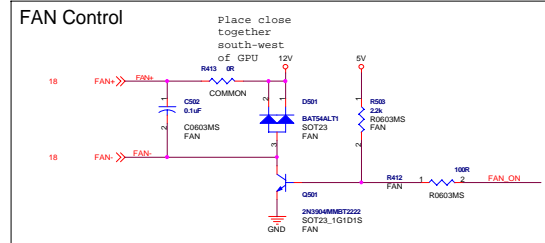
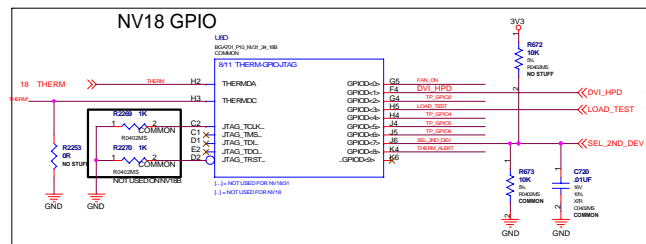
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NV18 STRAPPING, I/O INTERFACE, BIOS, FAN CONTROL AND TEMP SENSOR



STRAPPING OPTIONS

IN	Signal	VALUE_D	VALUES
03	PC1_A0_B0P	PC1_A0	00000000 10000000
07	SLB1_S0000	SLB1_S0000	PC01_S000 1000000000
02	RAM_C02_0	RAM_C02[0]	00000000 00000001 00000010 00000011 00000100 00000101 00000110 00000111 00010000 00010001 00010010 00010011 00010100 00010101 00010110 00010111 00011000 00011001 00011010 00011011 00011100 00011101 00011110 00011111 00100000 00100001 00100010 00100011 00100100 00100101 00100110 00100111 00101000 00101001 00101010 00101011 00101100 00101101 00101110 00101111 00110000 00110001 00110010 00110011 00110100 00110101 00110110 00110111 00111000 00111001 00111010 00111011 00111100 00111101 00111110 00111111 01000000 01000001 01000010 01000011 01000100 01000101 01000110 01000111 01001000 01001001 01001010 01001011 01001100 01001101 01001110 01001111 01010000 01010001 01010010 01010011 01010100 01010101 01010110 01010111 01011000 01011001 01011010 01011011 01011100 01011101 01011110 01011111 01100000 01100001 01100010 01100011 01100100 01100101 01100110 01100111 01101000 01101001 01101010 01101011 01101100 01101101 01101110 01101111 01110000 01110001 01110010 01110011 01110100 01110101 01110110 01110111 01111000 01111001 01111010 01111011 01111100 01111101 01111110 01111111 10000000 10000001 10000010 10000011 10000100 10000101 10000110 10000111 10001000 10001001 10001010 10001011 10001100 10001101 10001110 10001111 10010000 10010001 10010010 10010011 10010100 10010101 10010110 10010111 10011000 10011001 10011010 10011011 10011100 10011101 10011110 10011111 10100000 10100001 10100010 10100011 10100100 10100101 10100110 10100111 10101000 10101001 10101010 10101011 10101100 10101101 10101110 10101111 10110000 10110001 10110010 10110011 10110100 10110101 10110110 10110111 10111000 10111001 10111010 10111011 10111100 10111101 10111110 10111111 11000000 11000001 11000010 11000011 11000100 11000101 11000110 11000111 11001000 11001001 11001010 11001011 11001100 11001101 11001110 11001111 11010000 11010001 11010010 11010011 11010100 11010101 11010110 11010111 11011000 11011001 11011010 11011011 11011100 11011101 11011110 11011111 11100000 11100001 11100010 11100011 11100100 11100101 11100110 11100111 11101000 11101001 11101010 11101011 11101100 11101101 11101110 11101111 11110000 11110001 11110010 11110011 11110100 11110101 11110110 11110111 11111000 11111001 11111010 11111011 11111100 11111101 11111110 11111111
05	ADP_A0	ADP_A0	00000000 10000000
11	ADP_F0270		00000000 10000000
12	PC1_DE0_0	PC1_DE0[0]	00000000...11110000
13	PC1_DE0_1		
14	SLB1_T0P	SLB1_T0P[0]	0000 1000
15	FP_FACE		
16	USER_0		
17	USER_1		
18	USER_2		
19	USER_3		
20	PC1_DE0_2		
21	PC1_DE0_3		
22	CRYS0A_1		
23	FR_0		
24	FR_1		
25	SR		
26	SR_V000		
27	SR_A0P		
28	SR_0		
29	RCM1_T0P_0	RCM1_T0P[0]	00000000 01000000 10000000 11000000
	RCM1_T0P_1		
	RCM1_T0P_2		
01	CR_0_0	[1000]	00000000 10000000



NET	NET_PHYSICAL_TYPE	VOLTAGE
745M1	24K8_TRACE	
745M2	24K8_TRACE	
NET	Diffpair	NET_SPACING_RULE
745M3	24K8_GIG_24K8	
745M4	24K8_CUP_24K8	
DIFFPAIR_0	24K8	
DIFF_0	24K8	
DIFF_PAIRING	24K8	
DIFF_PAIRING	24K8	
DIFFPAIR_0	24K8	
DIFFPAIR_0	24K8_GIG_24K8	



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Size	Document Number	
Custom	Strapping, I/O interface, BIOS	
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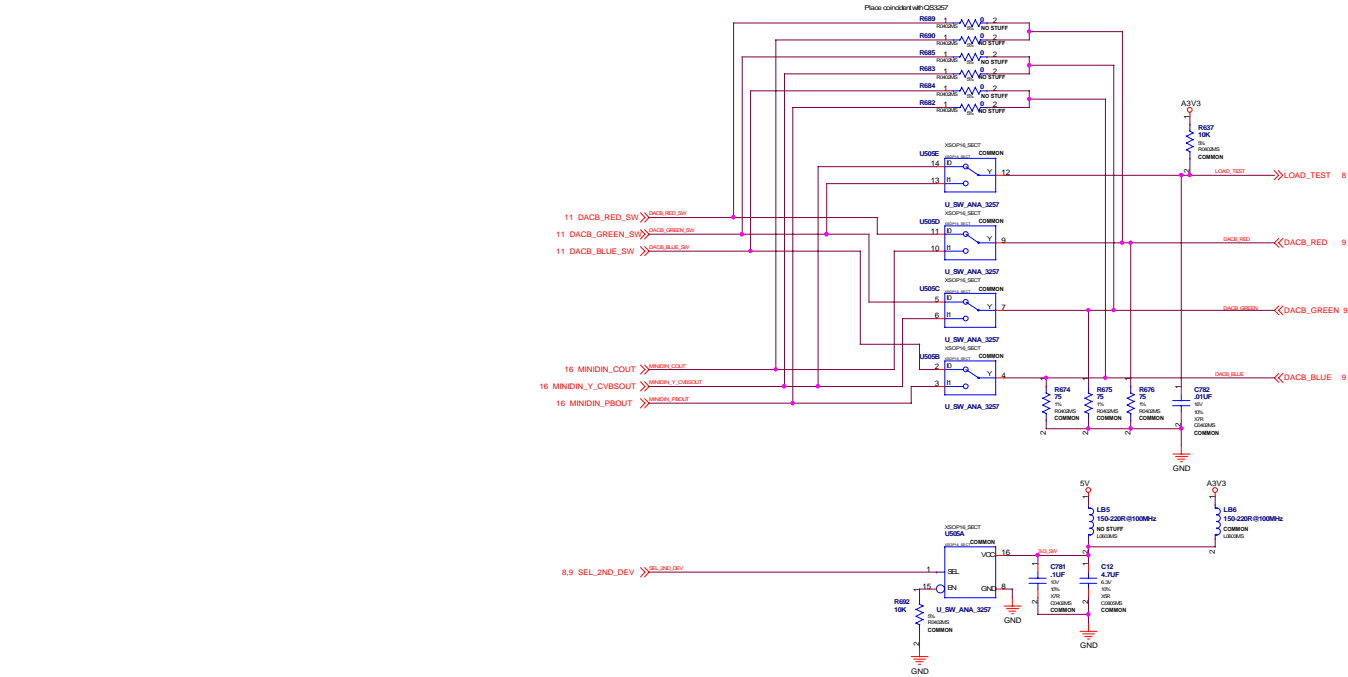
G		H	
NET		NET_PHYSICAL_TYPE	VOLTAGE
DACA_VDD		DACA_TRACE	3.3V
DACA_WBST		DACA_TRACE	
DACA_WBST		DACA_TRACE	
DACA_VDD		DACA_TRACE	3.3V
DACA_WBST		DACA_TRACE	
DACA_WBST		DACA_TRACE	
VDD_VDD		DACA_TRACE	3.3V
NET		IMPEDANCE	NET_SPACING_RULE
12 DACA_RED		37.5 OHM	20M_000_20M_0
12 DACA_GREEN		37.5 OHM	20M_000_20M_0
12 DACA_BLUE		37.5 OHM	20M_000_20M_0
10 DACA_RED		37.5 OHM	20M_000_20M_0
10 DACA_GREEN		37.5 OHM	20M_000_20M_0
10 DACA_BLUE		37.5 OHM	20M_000_20M_0

The image displays four circuit diagrams, each showing a different implementation of HS and VS SYNC signals using 74VHC00 inverters and 74VHC02 NAND gates. Each diagram includes a 5V power supply, a 100k pull-up resistor, and a 10k current-limiting resistor. The output of each circuit is labeled as D[CA,VB]_HSYNC_BUF 1 and D[CA,VB]_VSYNC_BUF 1.

- U1A:** The circuit uses a 74VHC02 NAND gate (U1A) and two 74VHC00 inverters (U1B and U1C). The input D[CA]_VSYNC is connected to pin 1 of U1A. The output of U1A is connected to pin 3 of U1B. The output of U1B is connected to pin 1 of U1C. The output of U1C is connected to pin 2 of U1A. The output of U1A is connected to D[CA]_VSYNC_BUF 1. The output of U1B is connected to D[CA]_HSYNC_BUF 1.
- U1B:** The circuit uses a 74VHC02 NAND gate (U1B) and two 74VHC00 inverters (U1C and U1D). The input D[CA]_VSYNC is connected to pin 4 of U1B. The output of U1B is connected to pin 6 of U1C. The output of U1C is connected to pin 4 of U1D. The output of U1D is connected to pin 5 of U1B. The output of U1B is connected to D[CA]_VSYNC_BUF 1. The output of U1C is connected to D[CA]_HSYNC_BUF 1.
- U1C:** The circuit uses a 74VHC02 NAND gate (U1C) and two 74VHC00 inverters (U1D and U1E). The input D[CA]_VSYNC is connected to pin 10 of U1C. The output of U1C is connected to pin 8 of U1D. The output of U1D is connected to pin 10 of U1E. The output of U1E is connected to pin 9 of U1C. The output of U1C is connected to D[CA]_VSYNC_BUF 1. The output of U1D is connected to D[CA]_HSYNC_BUF 1.
- U1D:** The circuit uses a 74VHC02 NAND gate (U1D) and two 74VHC00 inverters (U1E and U1F). The input D[CA]_VSYNC is connected to pin 13 of U1D. The output of U1D is connected to pin 11 of U1E. The output of U1E is connected to pin 13 of U1F. The output of U1F is connected to pin 12 of U1D. The output of U1D is connected to D[CA]_VSYNC_BUF 1. The output of U1E is connected to D[CA]_HSYNC_BUF 1.

Please make sure to keep all components and nets related to pins XTALIN, XTALOUT, XTALSSIN, and XTALOUTBUFF away from everything else (place all on TOP).

DACB SWITCH BETWEEN VGA OUT AND TV OUT

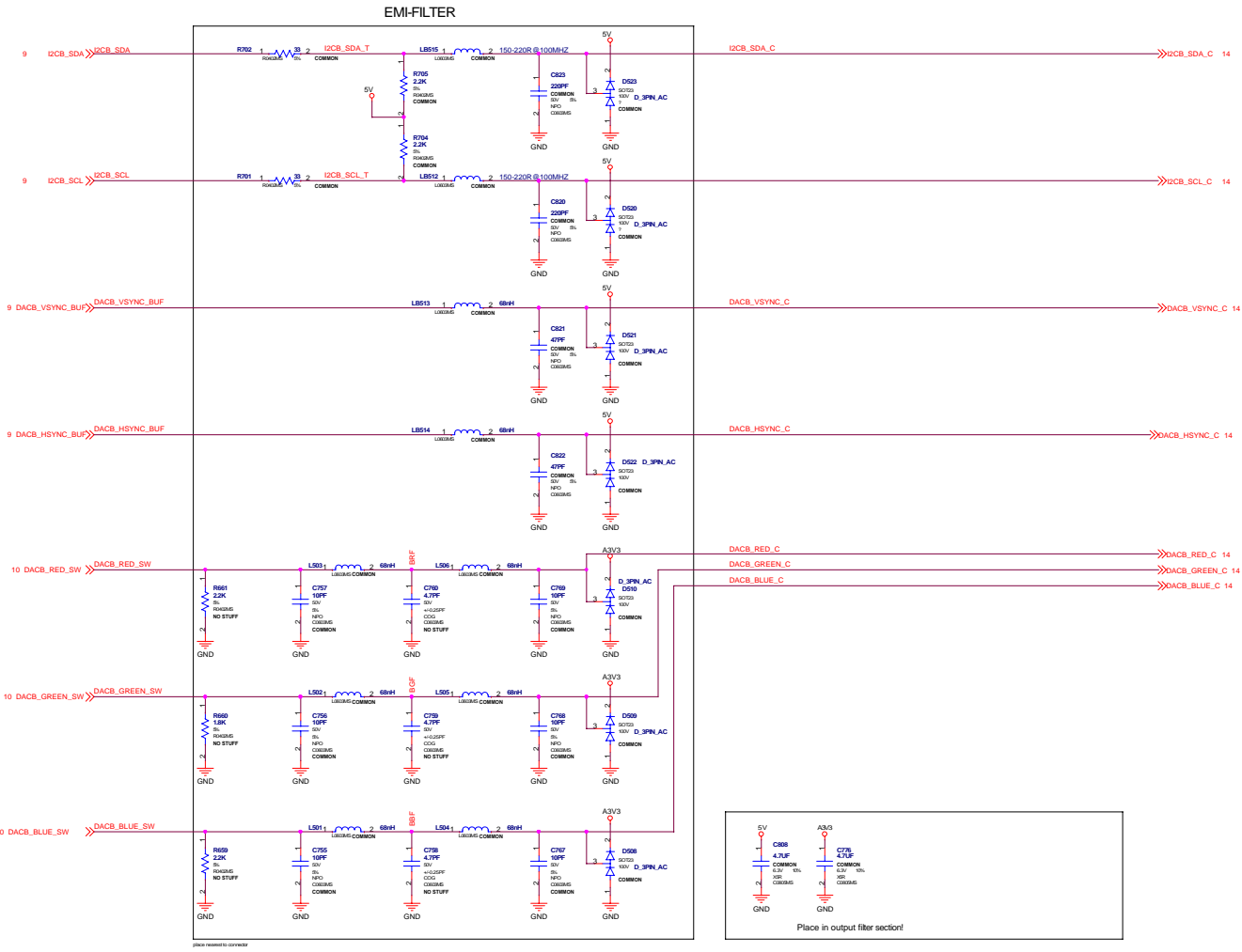


NET	IMPEDANCE	NET_SPACING_RULE
11 DACB_RED_SW	37.5 OHM	200M_000_200M
11 DACB_GREEN_SW	37.5 OHM	200M_000_200M
11 DACB_BLUE_SW	37.5 OHM	200M_000_200M
16 MINIDIN_COUT	37.5 OHM	200M_000_200M
16 MINIDIN_Y_CVBSOUT	37.5 OHM	200M_000_200M
16 MINIDIN_PBOUT	37.5 OHM	200M_000_200M

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Custom SWITCH BETWEEN VGA AND TV-OUT		
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DACB output



NET	IMPEDANCE	NET_SPACING_RULE
SDA	37.5 OHM	20MIL TRACE
SCL	37.5 OHM	20MIL TRACE
VSYNC	37.5 OHM	20MIL TRACE
Hsync	10MIL TRACE	20MIL TRACE
RED	10MIL TRACE	20MIL TRACE
GREEN	10MIL TRACE	20MIL TRACE
BLUE	10MIL TRACE	20MIL TRACE

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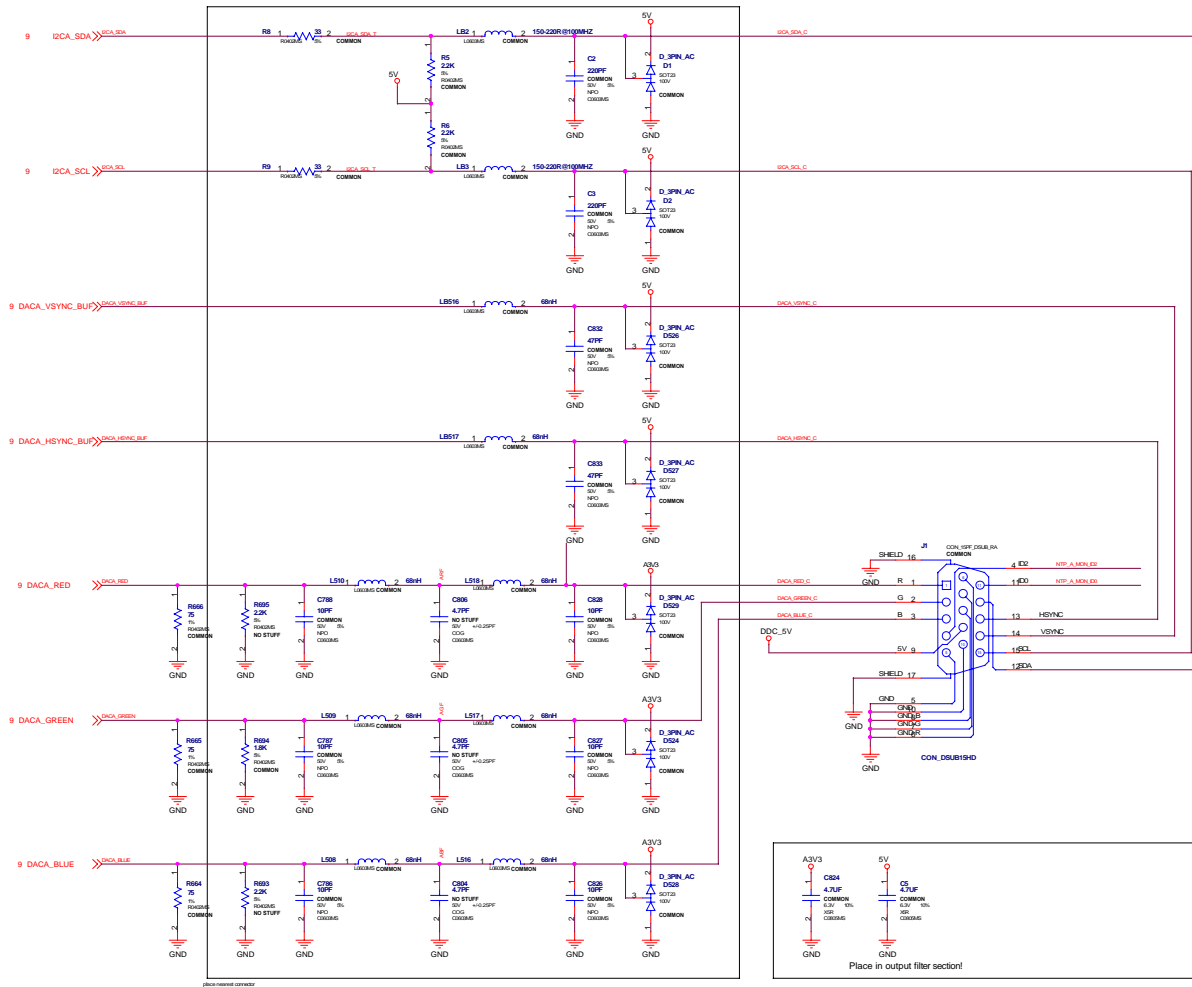
Rev. 008

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DACB output

EMI-FILTER



NET	IMPEDANCE	NET_SPACING_RULE
DCA_SDA	37.5 OHM	20M_C02_00A
DCA_SCL	37.5 OHM	20M_C02_00A
DCA_VSYNC	37.5 OHM	20M_C02_00A
DCA_HSYNC	37.5 OHM	20M_C02_00A
DCA_RED_C	10MIL TRACE	20M_C02_00A
DCA_GREEN_C	10MIL TRACE	20M_C02_00A
DCA_BLUE_C	10MIL TRACE	20M_C02_00A

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Doc	Custom	DAC A CONNECT	
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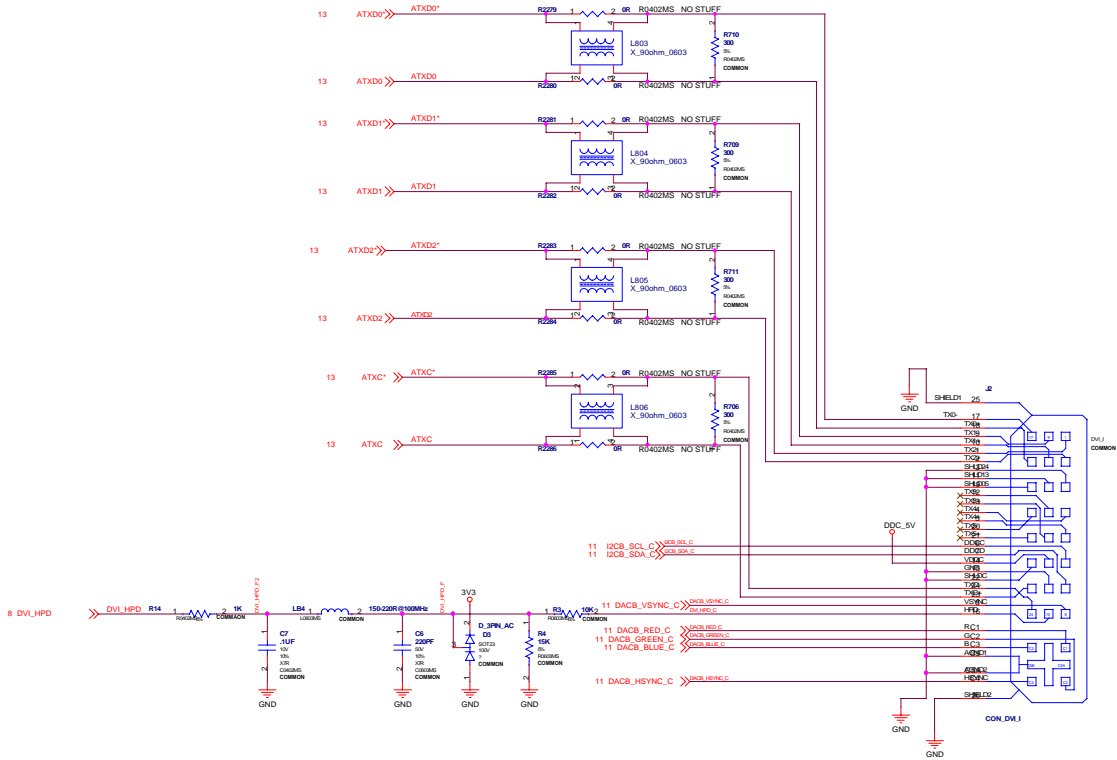
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TMDS POWER AND DECOUPLING


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DVI_I OUTPUT



NET	Diffpair	NET_SPACING_RULE
13 ATXD0	ATXD0	18in_000_25in_4
13 ATXD0	ATXD0	18in_000_25in_4
13 ATXD1	ATXD1	18in_000_25in_4
13 ATXD1	ATXD1	18in_000_25in_4
13 ATXD2	ATXD2	18in_000_25in_4
13 ATXD2	ATXD2	18in_000_25in_4
13 ATXC	ATXC	18in_000_25in_4
13 ATXC	ATXC	18in_000_25in_4

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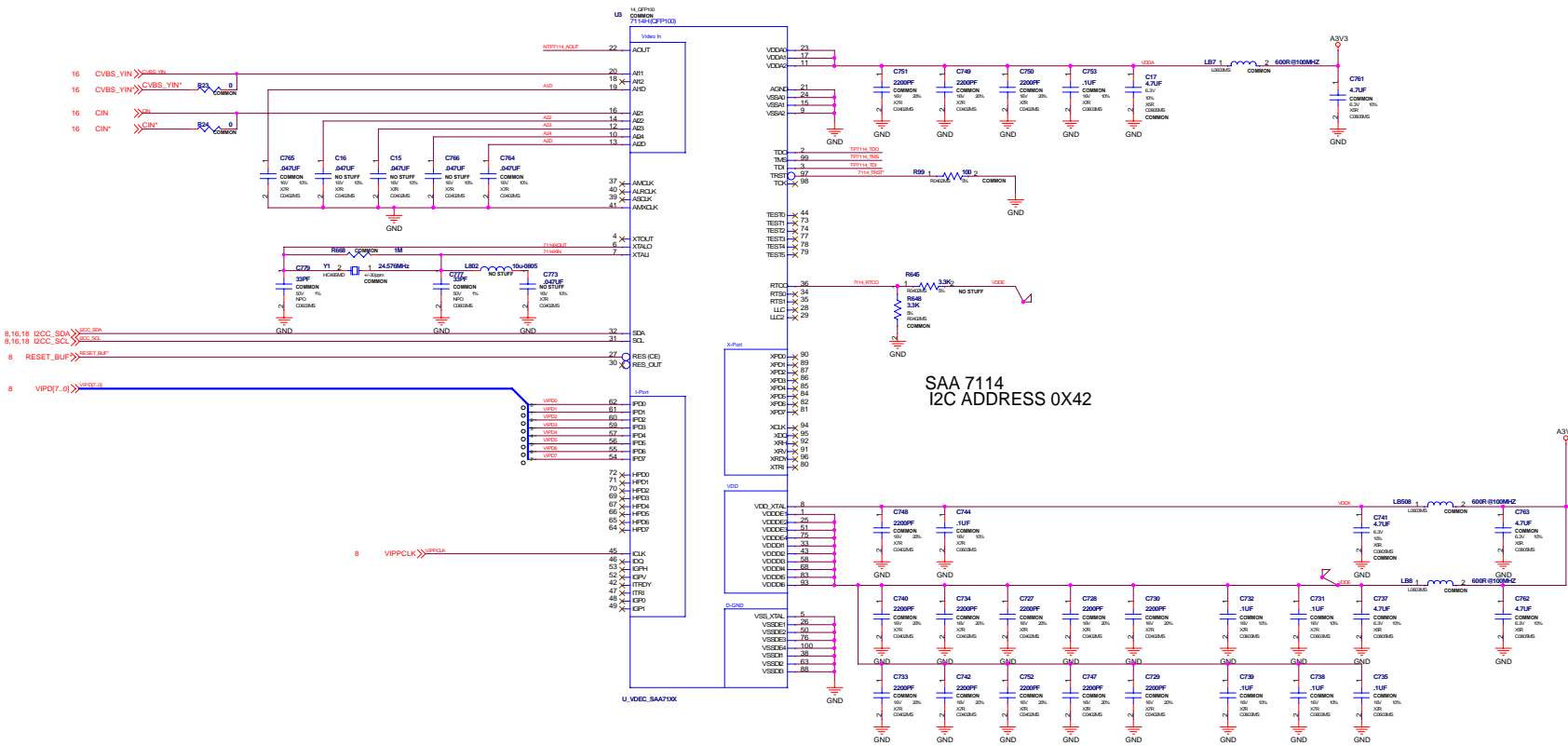
DVI CONNECT

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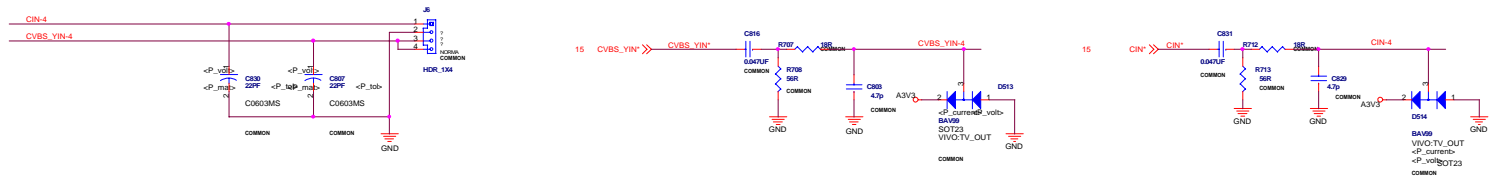
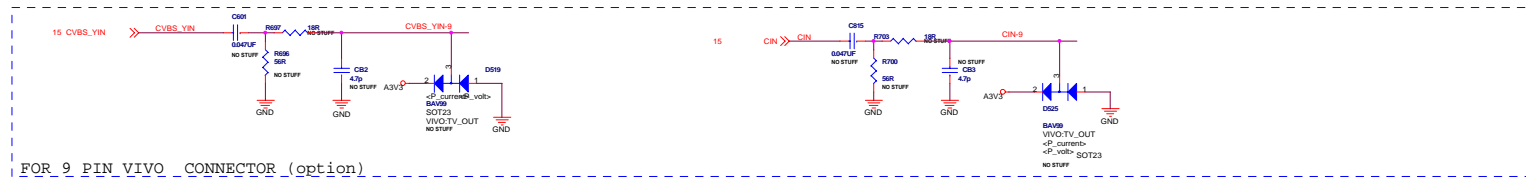
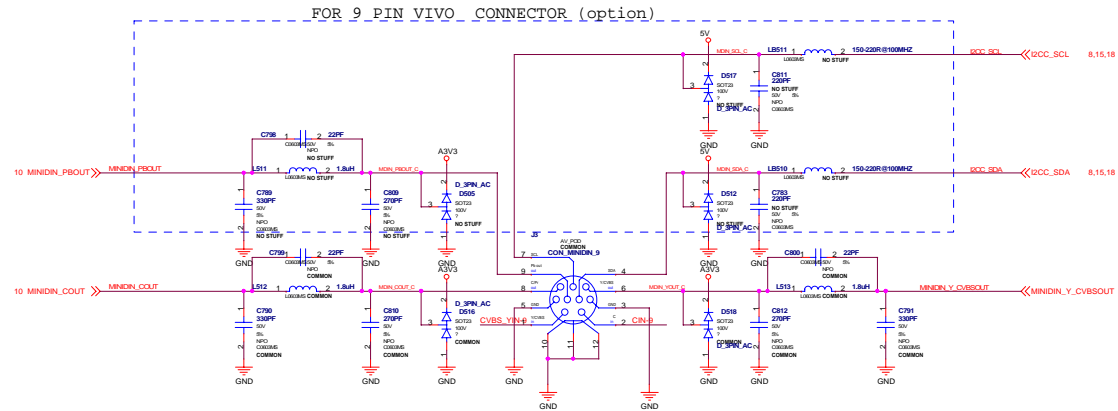
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VIDEO CAPTURE

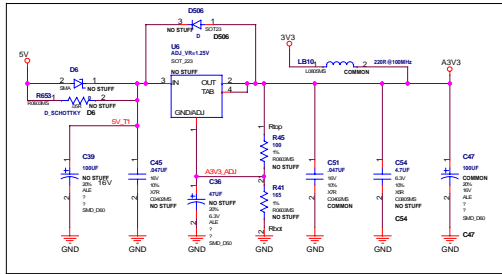


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I2C ADDRESS 0X42

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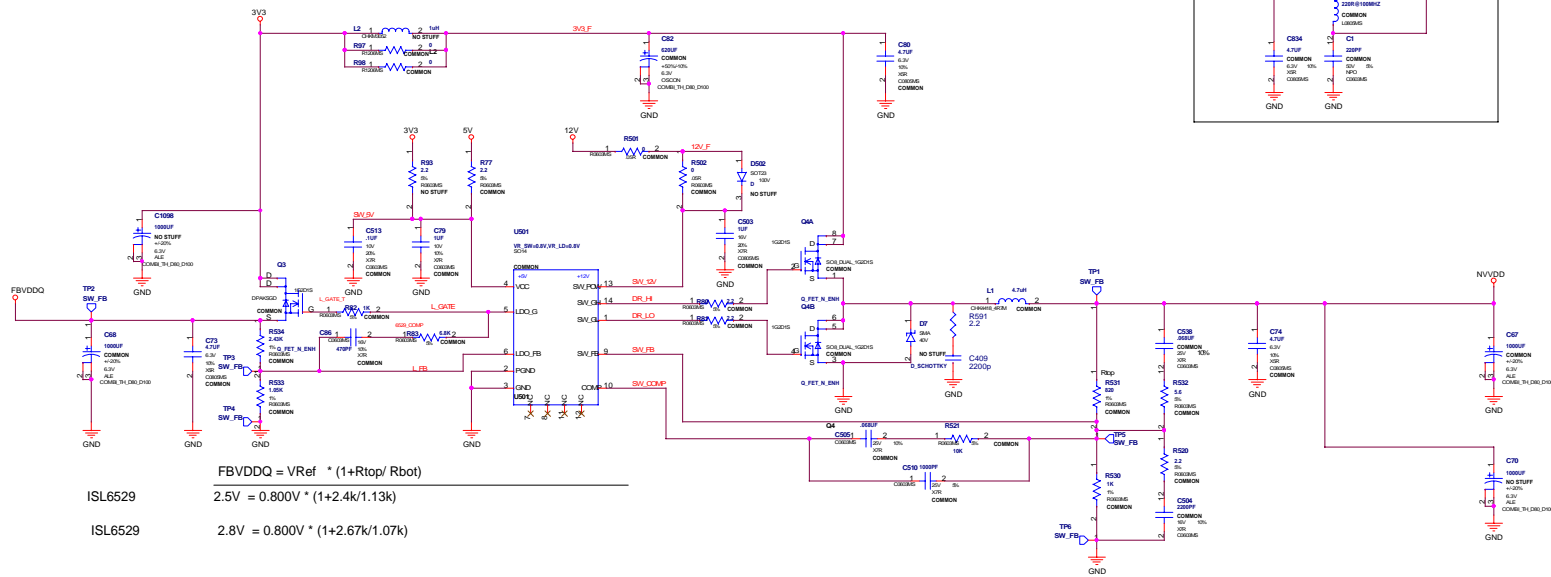
ANALOG 3V3



$$V_{out} = V_{Ref} * (1 + R_{bot}/R_{top})$$

$$3.31V = 1.25V * (1 + (165/100))$$

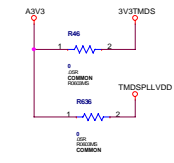
NVDD-SWITCHER / FBVDD-LDO CONTROLER ISL6529



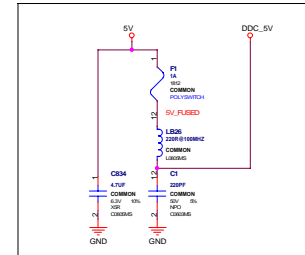
	$\text{FBVDDQ} = \text{VRef} \cdot (1 + \text{Rtop}/\text{Rbot})$
ISL6529	$2.5\text{V} = 0.800\text{V} \cdot (1 + 2.4\text{k}/1.13\text{k})$
ISL6529	$2.8\text{V} = 0.800\text{V} \cdot (1 + 2.67\text{k}/1.07\text{k})$

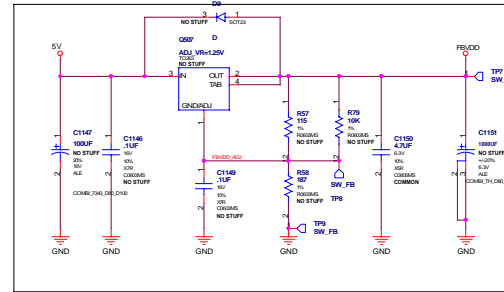
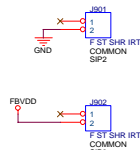
$$1.656V = 0.800V * (1 + 1070/1000)$$

TMDS 3V3 Supply
TMDS PLL Supply

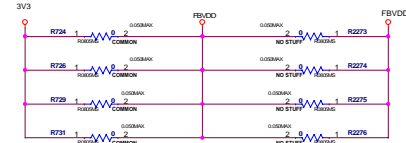
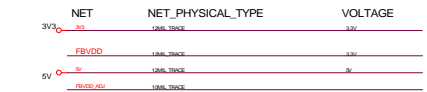


DDC 5V

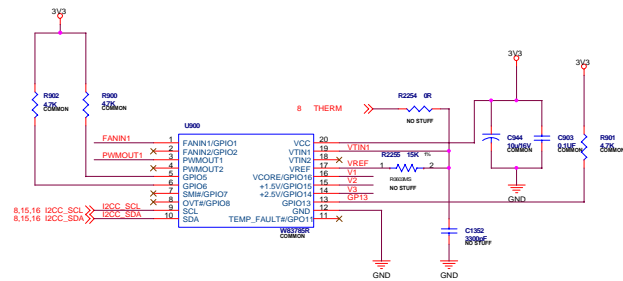
[illegible]



$$\begin{aligned}\text{FBVDD} &= \text{VRef} * (1 + \text{Rbot} / \text{Rtop}) \\ 3.315\text{V} &= 1.250\text{V} * (1 + 165 / 100) \\ 3.300\text{V} &= 1.250\text{V} * (1 + 187 / 115)\end{aligned}$$



VOLTAGE SENSING CIRCUIT



Place close
together
south-west
of GPU

