

C116, NV18, 8MX16DDR, 128MB, Video IN/OUT, DVI-I, VGA

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HISTORY:


A00

- X00: INITIAL VERSION
- X01 Remove R117, C87, C131, C143 for CKE
 - Change C736, C743 to 18pf capacitors.
 - Remove C1099 - additional Capacitor for AGPVREFog
 - Changed AGPVREFog circuit.

C116 Base on P112 to Modify.

- 1. Change page 4~7 & page 18 Reference.
- 2. Change J1 foot print from slim type to stand D-SUB.
- 3. Remove I1394 function.
- ~~4. Page 2, change voltage C75.1 & Q2.2 from 3V3 to A3V3.~~
- 5. Page 8, Add Twin Bios for MSI function.
- 6. Page 16 ,replace INTERNAL VIDEO CAPTURE CONNECTOR.
- 7. Page 17 ,ADD C874 & C1098 ALE CAP. (DUAL-LAY)
- 8. Page 18 , Add H/W Monitor function for MSI .
- 9. Page 2 change Q508, Q509 footprint from SOT23 to SOT-6 U200 package.

600-10116-000X-A00



Micro-Star International Co., Ltd.

MS-8893 base on C116 Modify

Doc: Custom

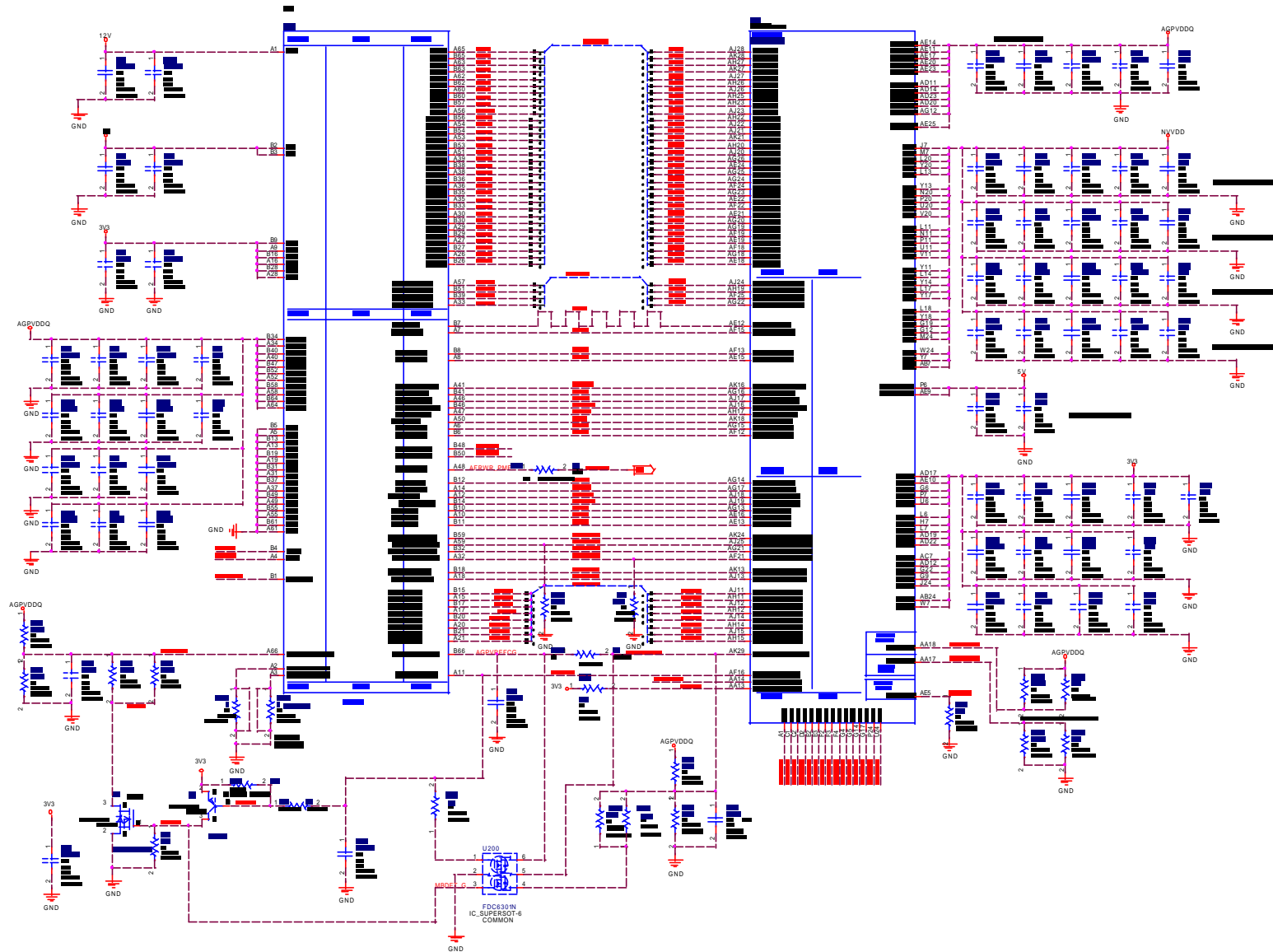
Date: Monday, September 16, 2008

Doc Number: 00A

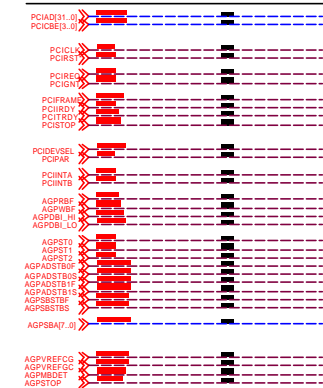
TOP PAGE

Sheet: 1 of 17

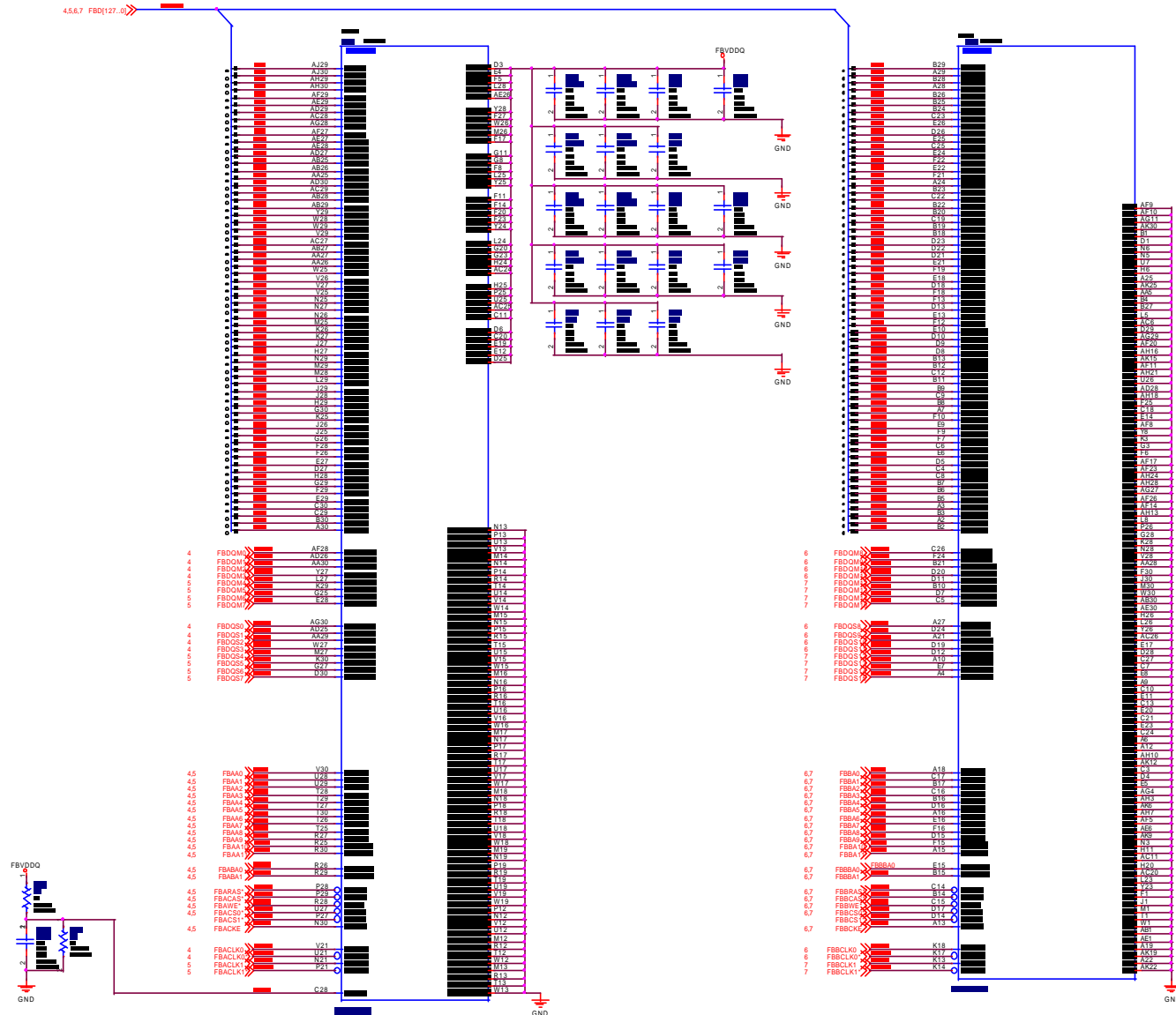
NV18 AGP SECTION AND AGP CONNECTOR

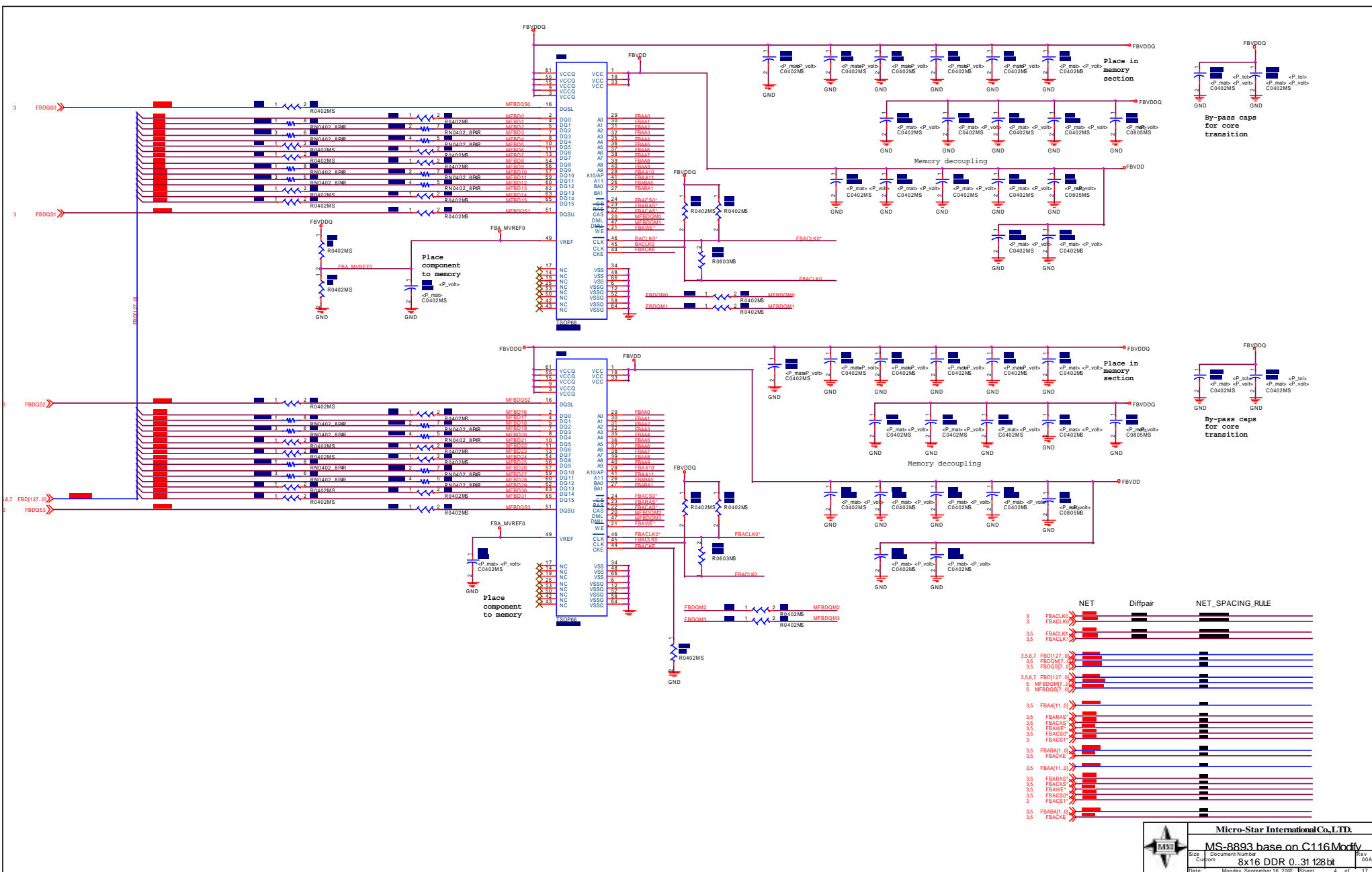


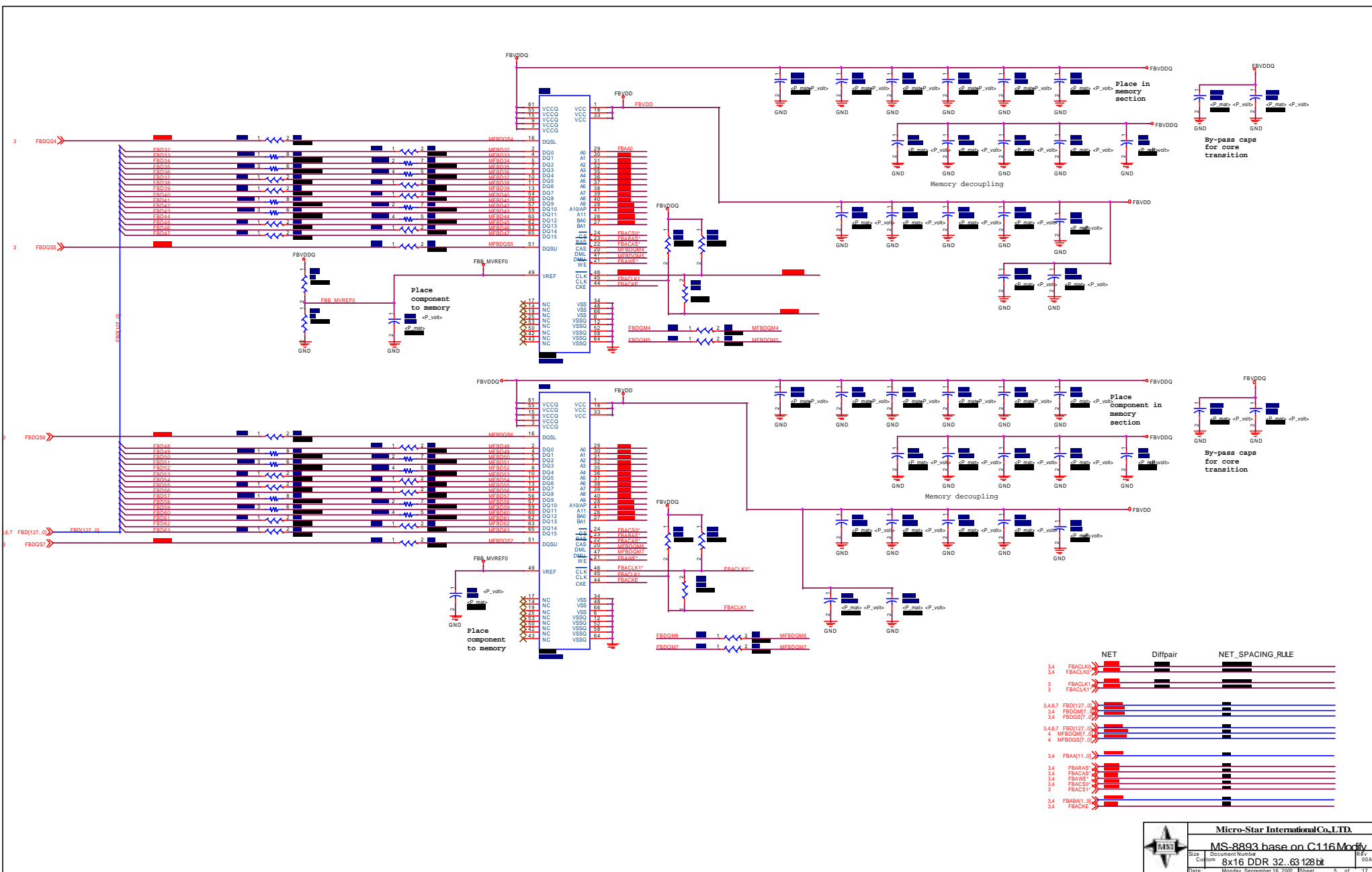
AGP spacing rules

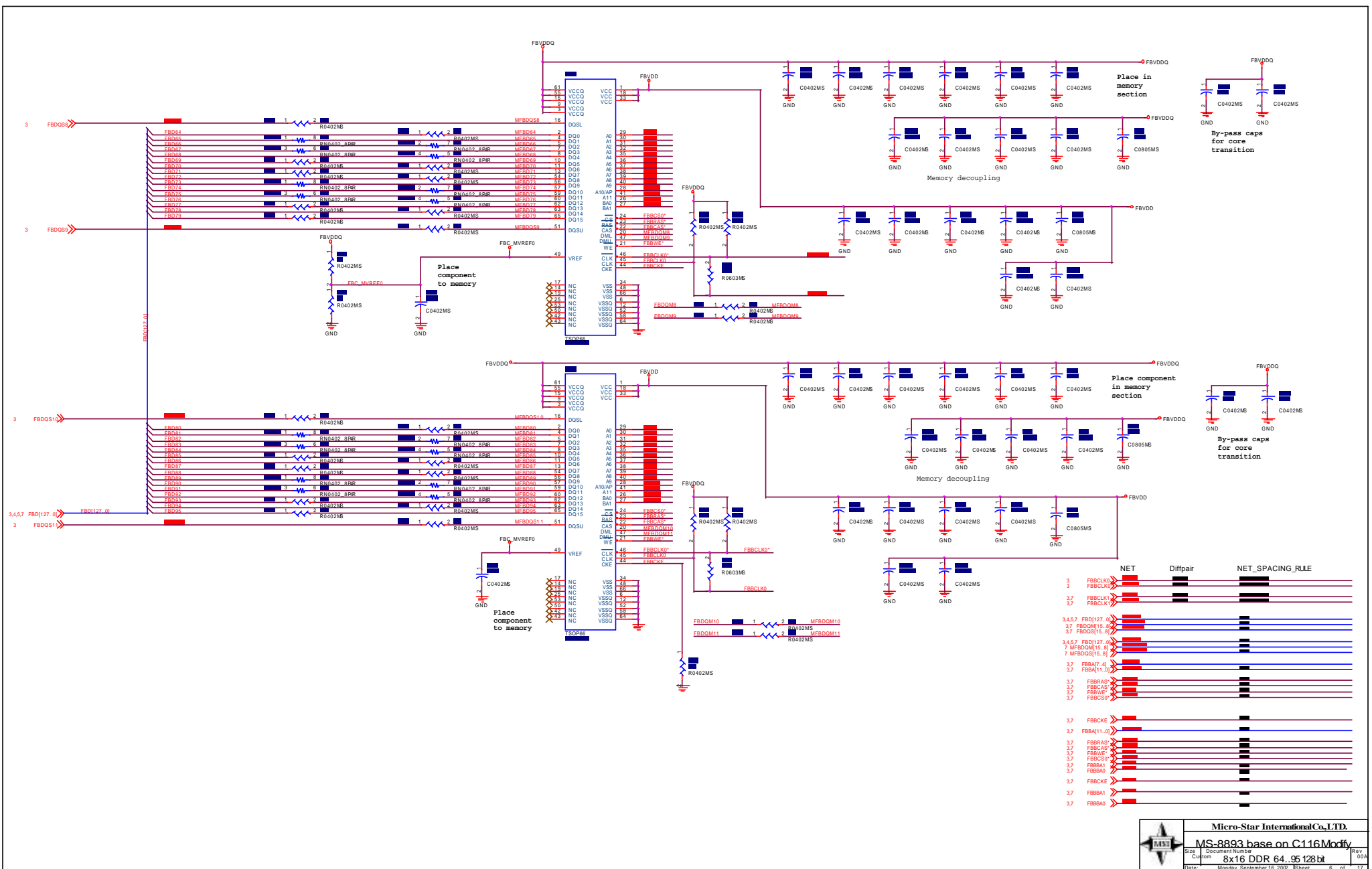


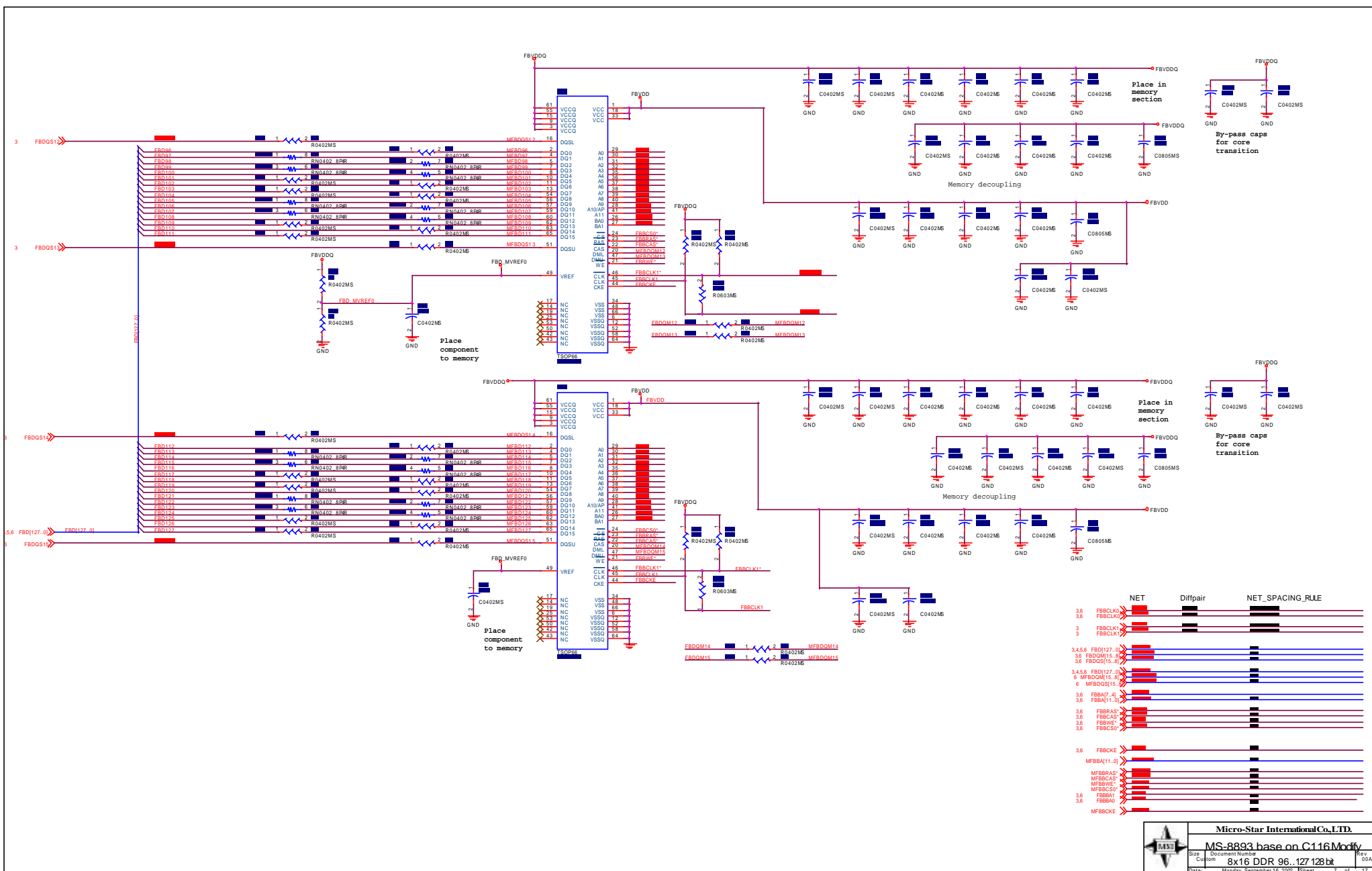
NV18 FRAMEBUFFER INTERFACE AND DECOUPLING



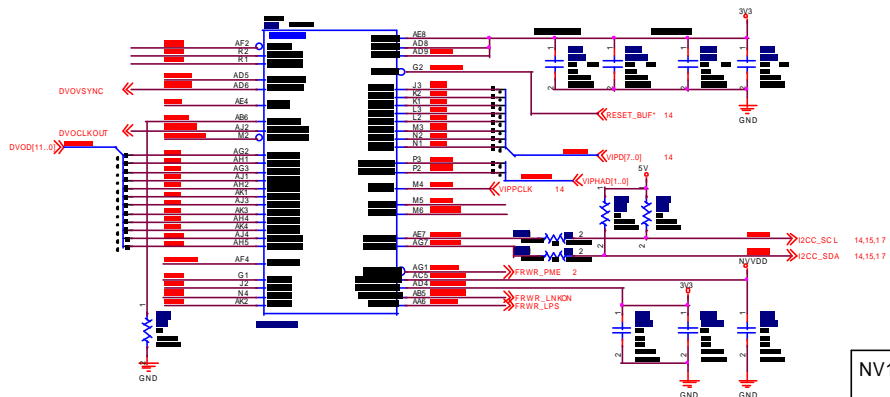




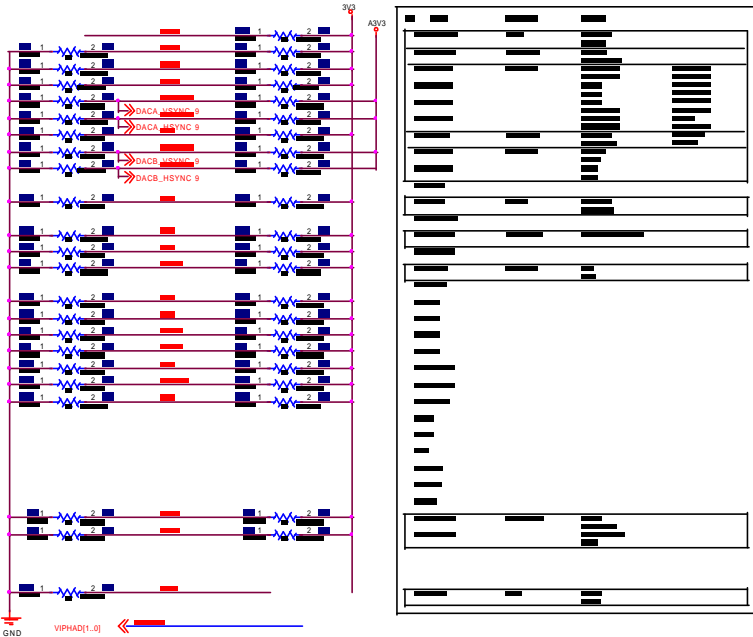




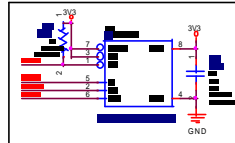
NV18 STRAPPING, I/O INTERFACE, BIOS, FAN CONTROL AND TEMP SENSOR



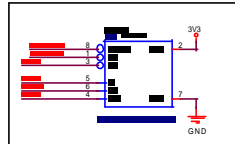
STRAPPING OPTIONS



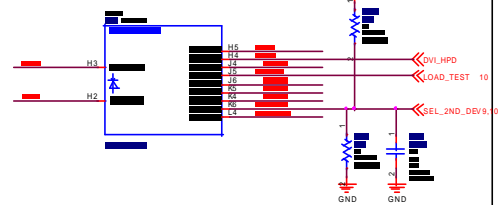
BIOS (serial)



BIOS (alternative)

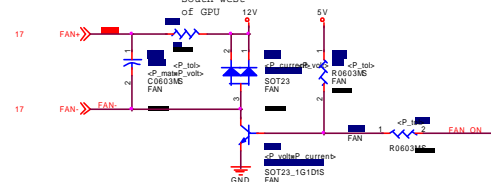


NV18 GPIO

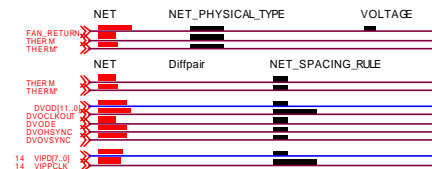
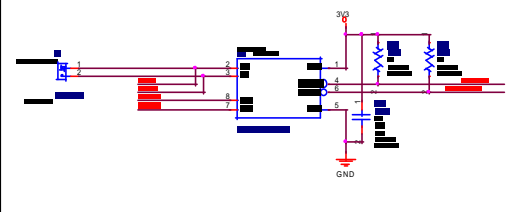


FAN Control

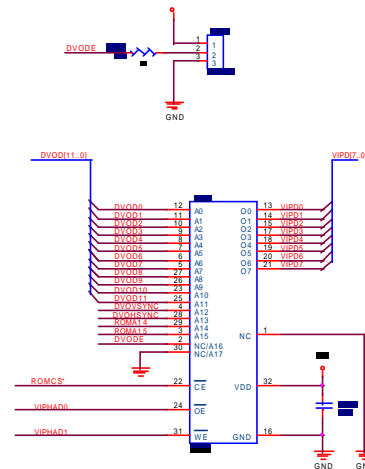
Place close
together
south-west
of GPU 133



TEMP Sensor

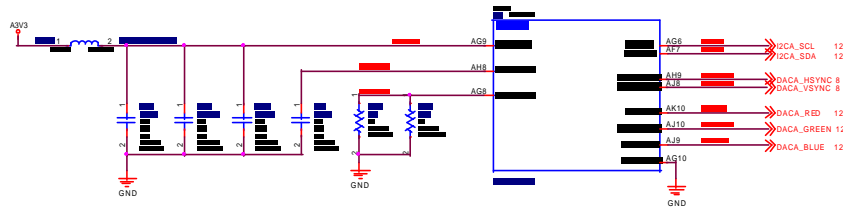


Twin BIOS

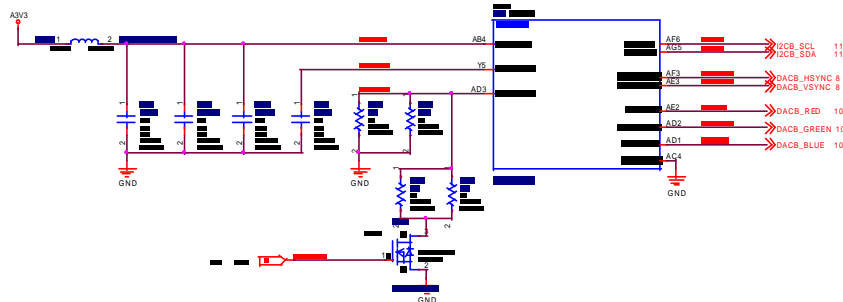


NV18 DAC_A, DAC_B, PLL, SYNC AMPL

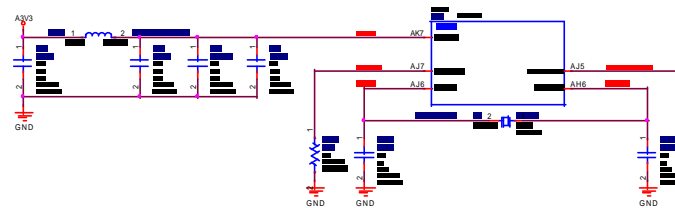
NV18 DAC_A



NV18 DAC_B with RSet select

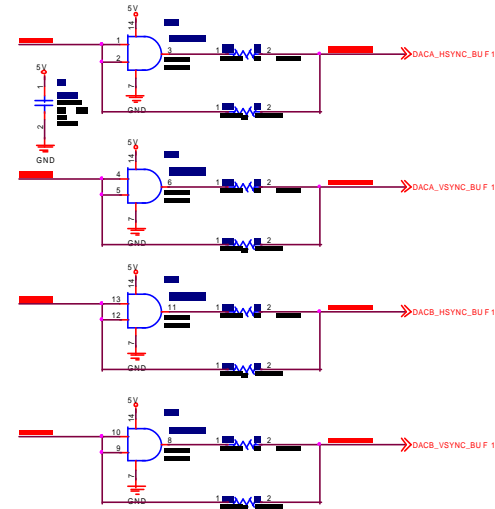


NV18 PLL

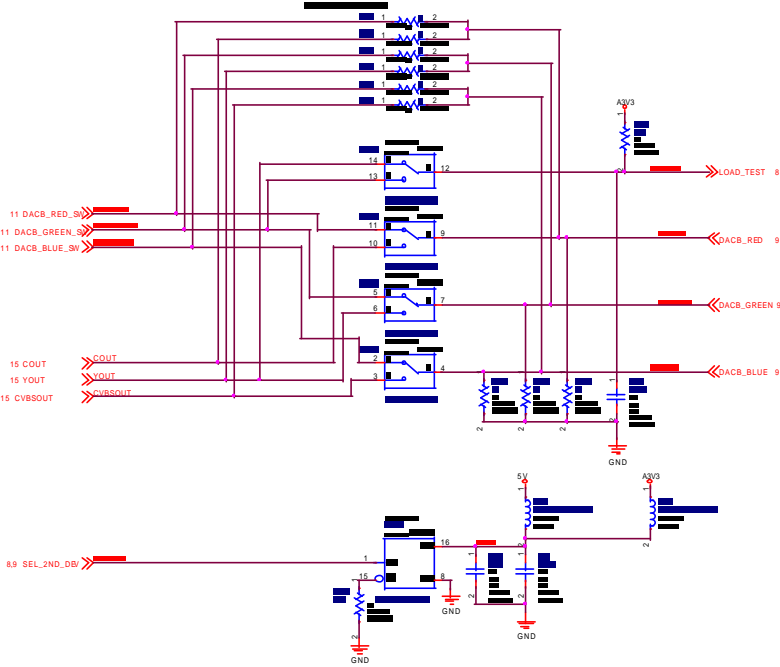


NET	NET_PHYSICAL_TYPE	VOLTAGE
DACA_VDD		
DACA_VREF		
DACA_RSET		
DACB_VDD		
DACB_VREF		
DACB_RSET		
PLL_VDD		
NET	Diffpair	NET_SPACING_RULE
12 DACA_RED		
12 DACA_GREEN		
12 DACA_BLUE		
10 DACB_RED		
10 DACB_GREEN		
10 DACB_BLUE		

SYNC Amplifier

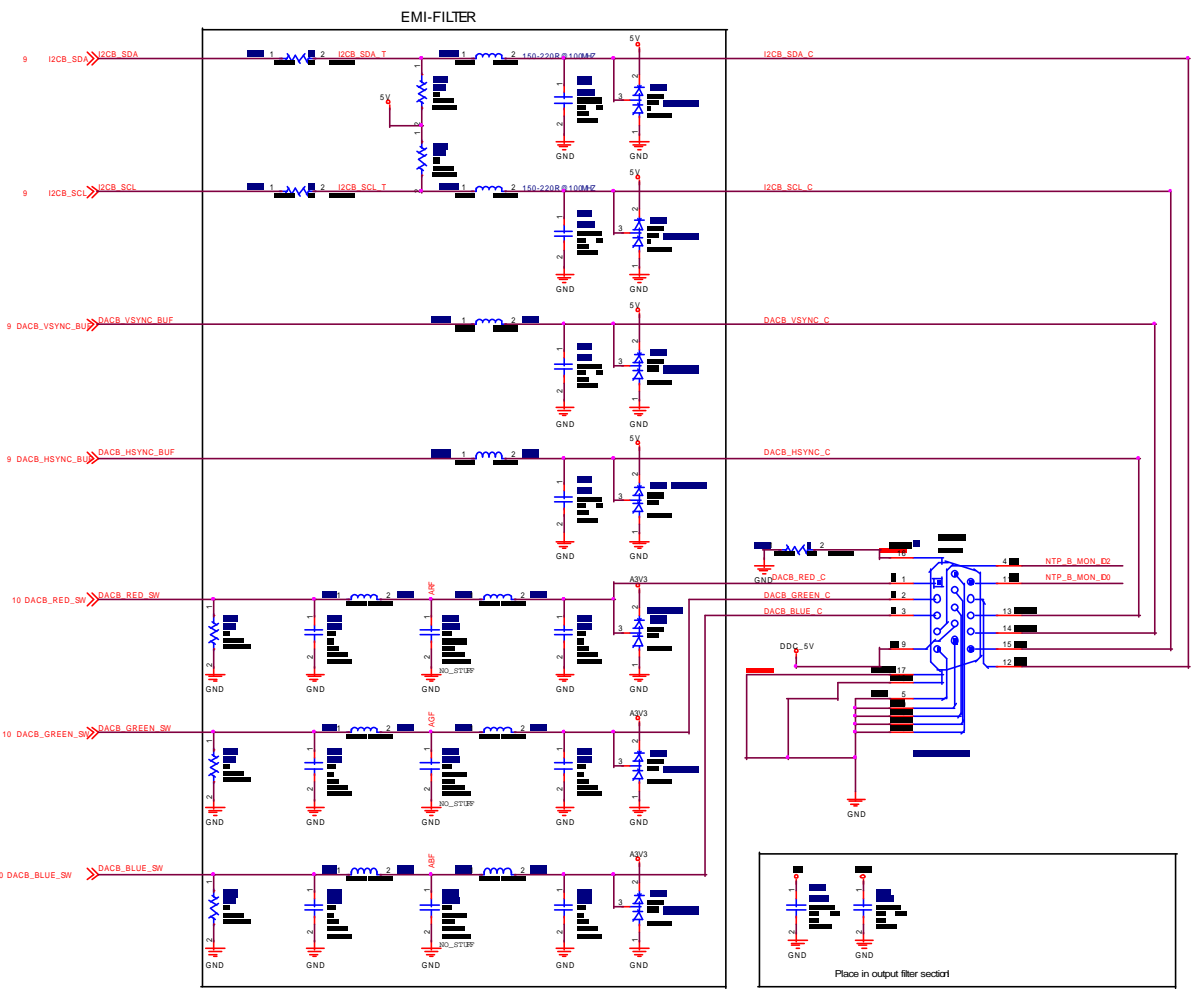


DACB SWITCH BETWEEN VGA OUT AND TV OUT



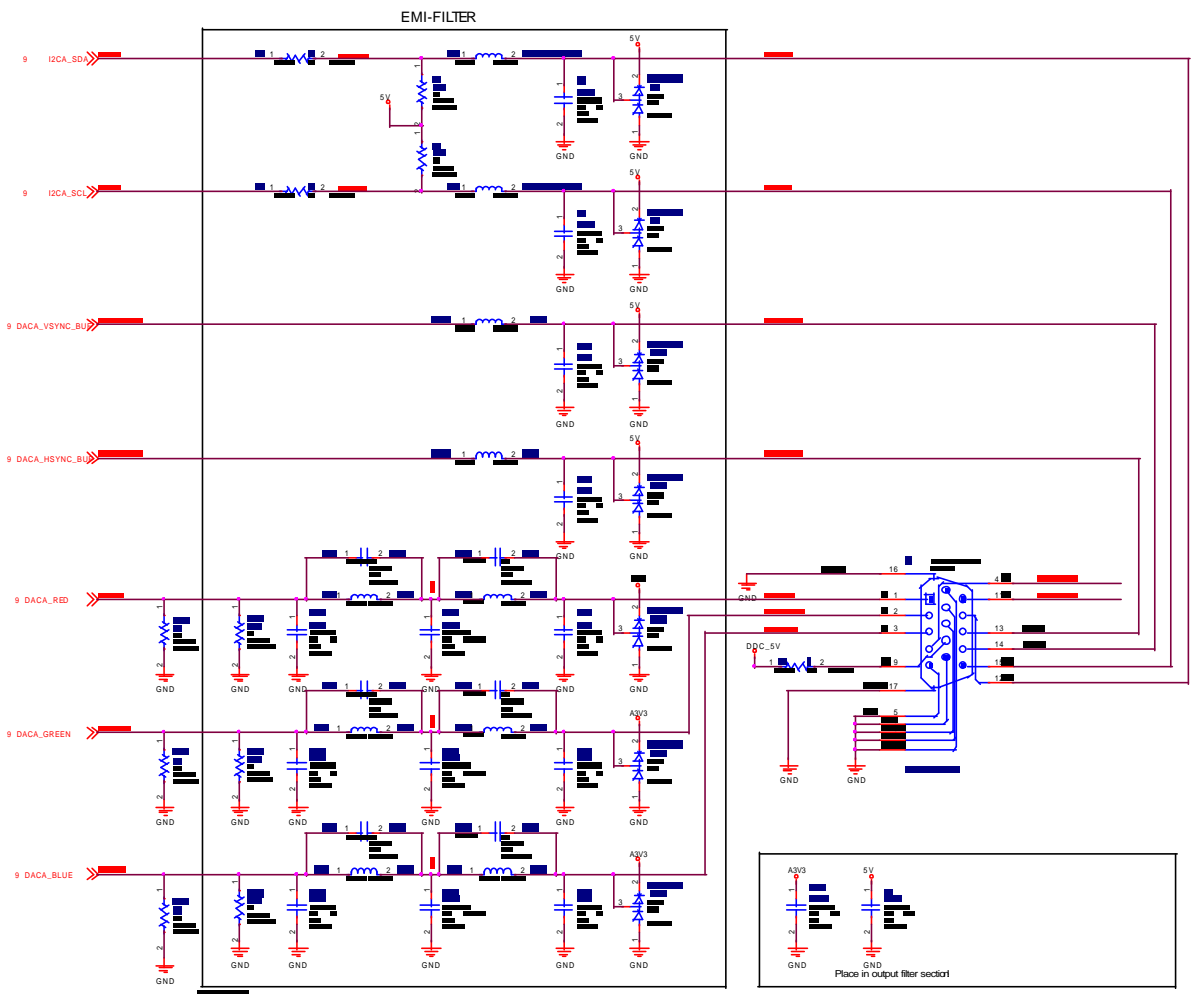
NET	Diffpair	NET_SPACING_RULE
11 DACB_RED_S		
11 DACB_GREEN_S		
11 DACB_BLUE_S		
MINIDIN_COUT		
MINIDIN_Y_CVBSOUT		
MINIDIN_PSOUT		

DACA output



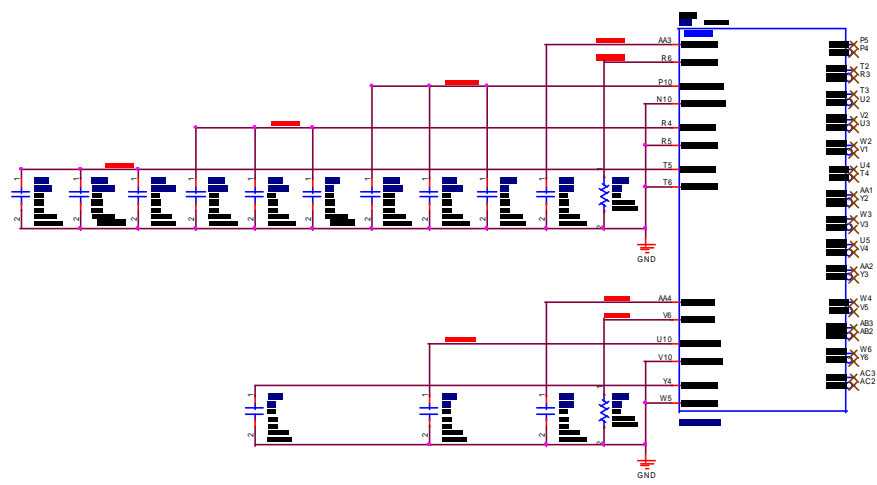
NET	Diffpair	NET_SPACING_RULE
BFB		
BGP		
BGP		
DACB_RED_C		
DACB_GREEN_C		
DACB_BLUE_C		

DACB output

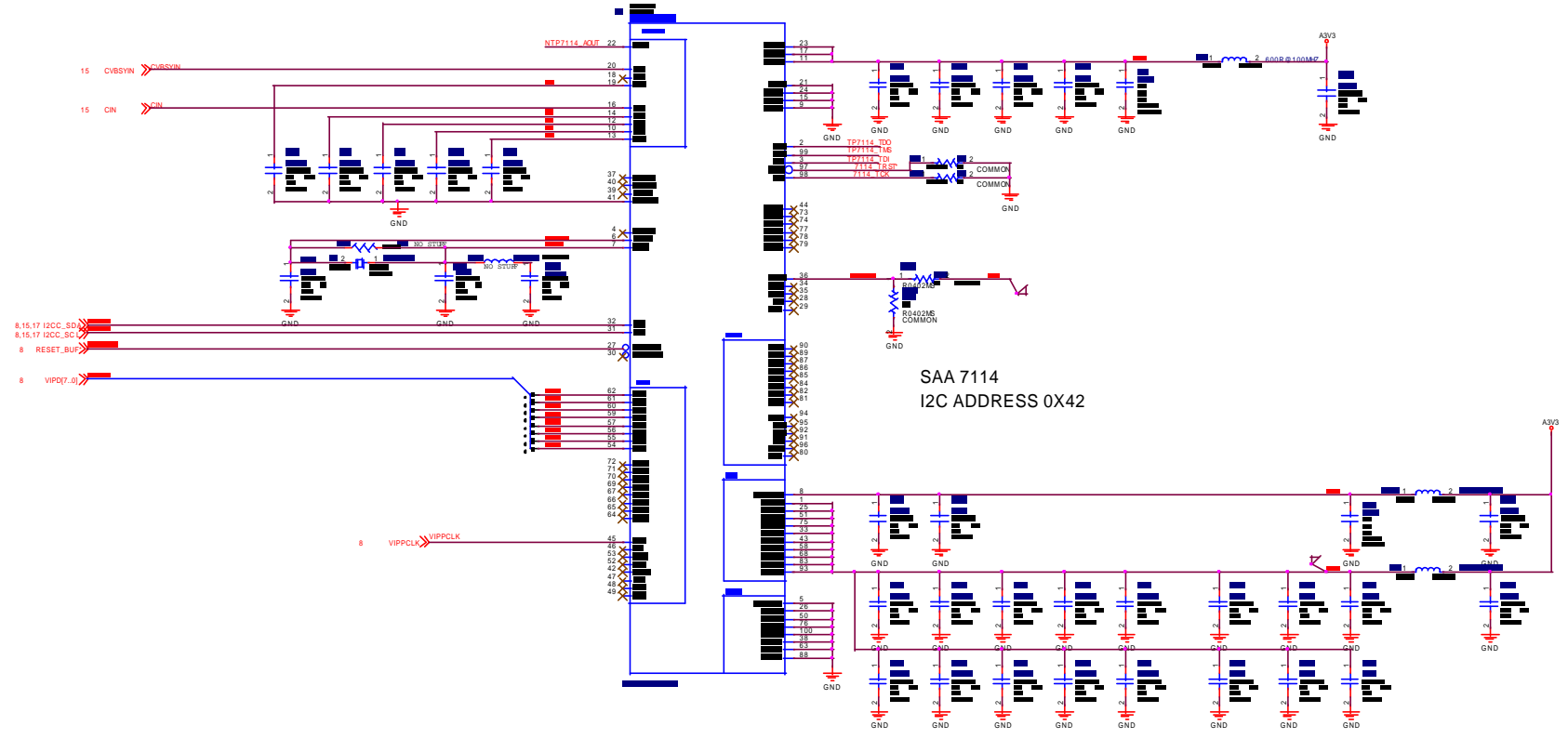


NET	Diffpair	NET_SPACING_RULE
ARD		
ARD		
ARD		
DACA_RED_C		
DACA_GREEN_C		
DACA_BLUE_C		

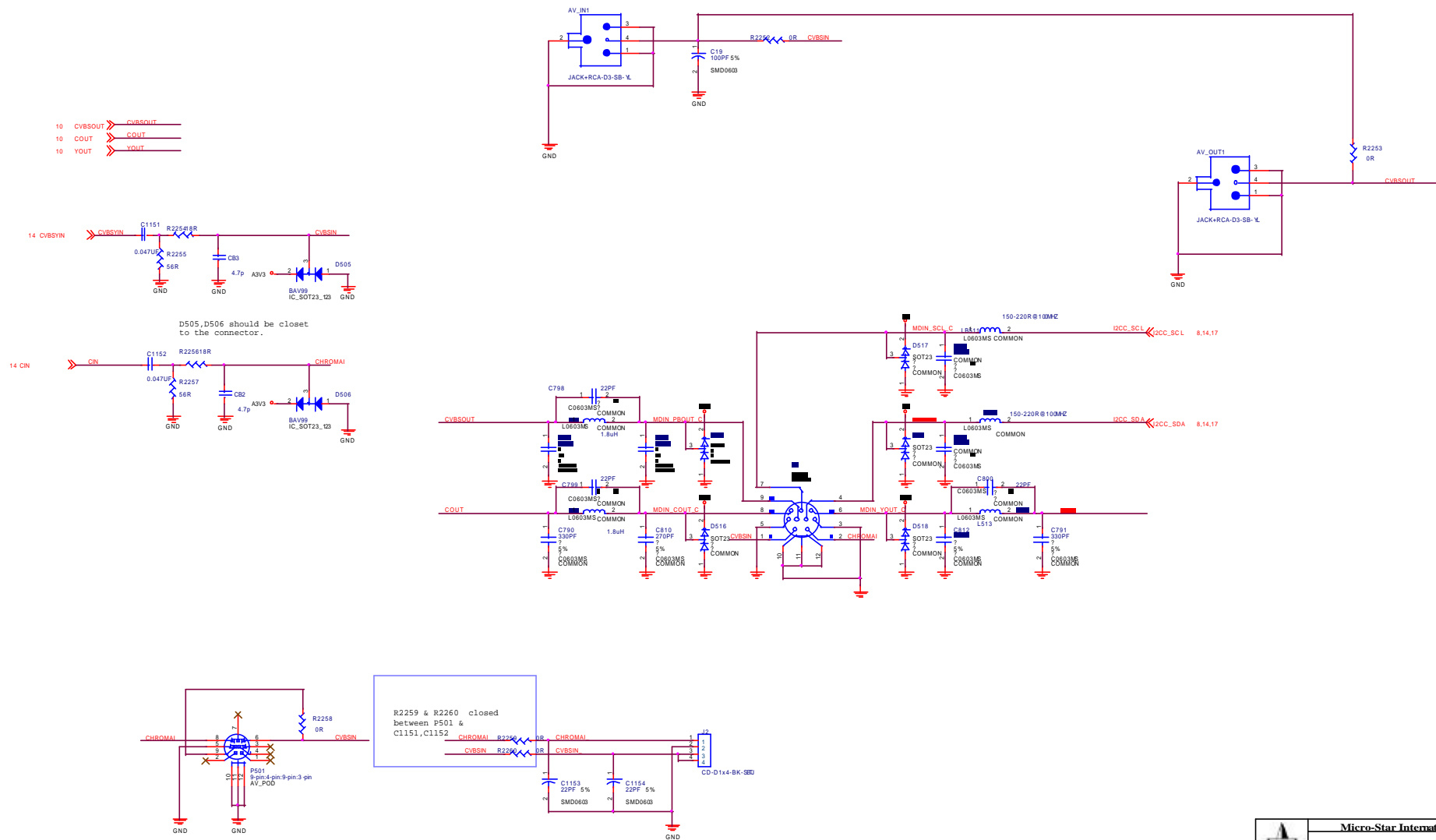
INTERNAL TMD5 POWER AND DECOUPLING



VIDEO CAPTURE

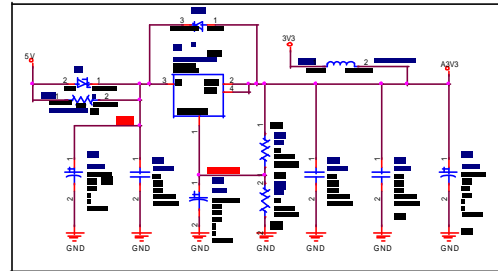


VIDEO IN/OUT CONNECTOR



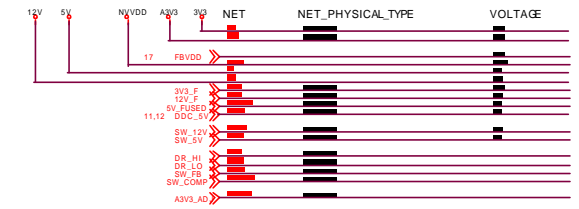
POWER SUPPLY

ANALOG 3V3

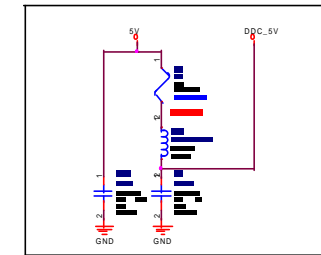


$$V_{out} = V_{Ref} * (1 + R_{bot}/R_{top})$$

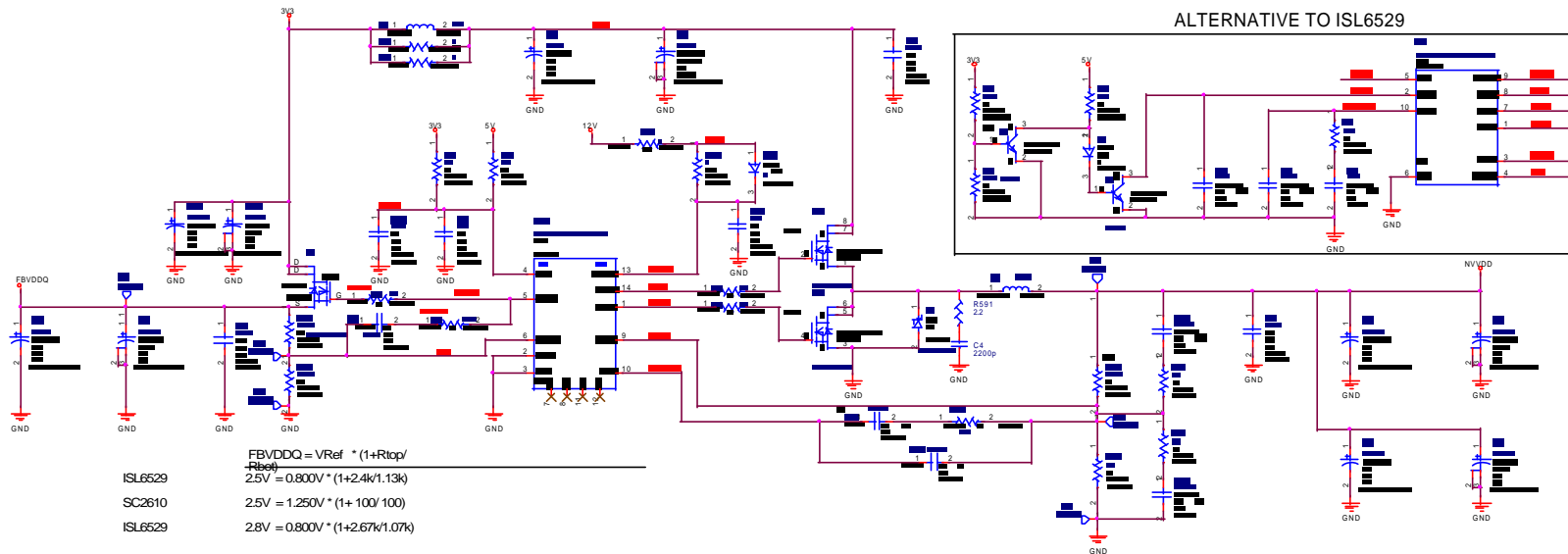
$$3.31V = 1.25V * (1 + (165/100))$$



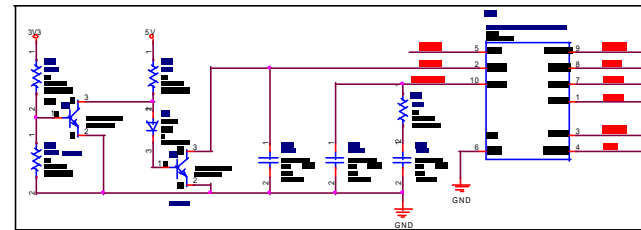
DDC 5V



NVDD-SWITCHER / FBVDD-LDO CONTROLLER ISL6529



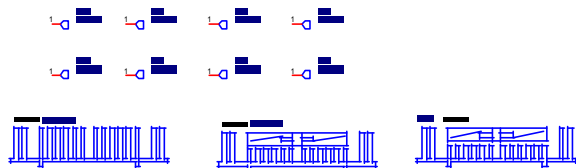
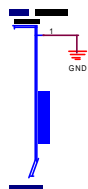
ALTERNATIVE TO ISL6529



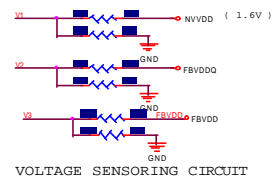
ISL6529 $FBVDDQ = V_{Ref} * (1 + R_{top}/R_{bot})$
 $2.5V = 0.800V * (1 + 2.4k/1.13k)$
 SC2610 $2.5V = 1.250V * (1 + 100/100)$
 ISL6529 $2.8V = 0.800V * (1 + 2.67k/1.07k)$

ISL6529 $NVDD = V_{Ref} * (1 + R_{top}/R_{bot})$
 $1.656V = 0.800V * (1 + 1070/1000)$
 SC2610 $1.656V = 0.800V * (1 + 1070/1000)$

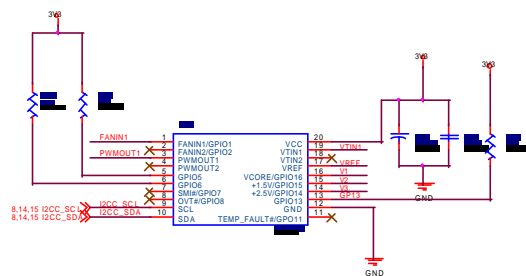
MECHANICS



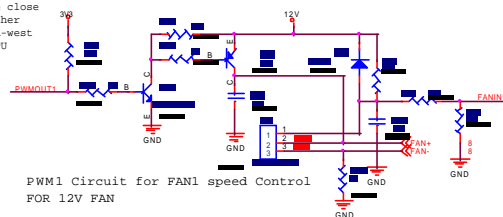
H/W Monitor Funtion



VOLTAGE SENSING CIRCUIT

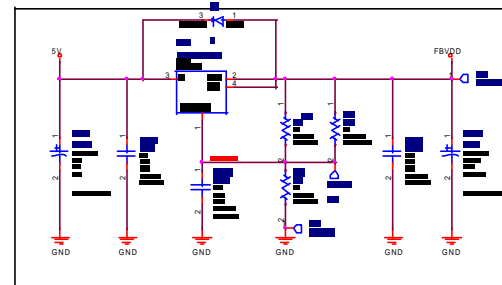


Place close together south-west of GPU



PWM1 Circuit for FAN1 speed Control FOR 12V FAN

FBVDD Supply



$$\begin{aligned} \text{FBVDD} &= V_{\text{Ref}} * (1 + R_{\text{bot}} / R_{\text{top}}) \\ 3.315\text{V} &= 1.250\text{V} * (1 + 165 / 100) \\ 3.300\text{V} &= 1.250\text{V} * (1 + 187 / 115) \end{aligned}$$

NET	NET_PHYSICAL_TYPE	VOLTAGE
3V3		
FBVDD	20MIL_TRACE	
5V		
FBVDD_ADJ		

