

GA102 DT SKU P-BOARD

350W, FH Std PCB, 384b, GDDR6X x8
DP + DP + DP + HDMI/DP

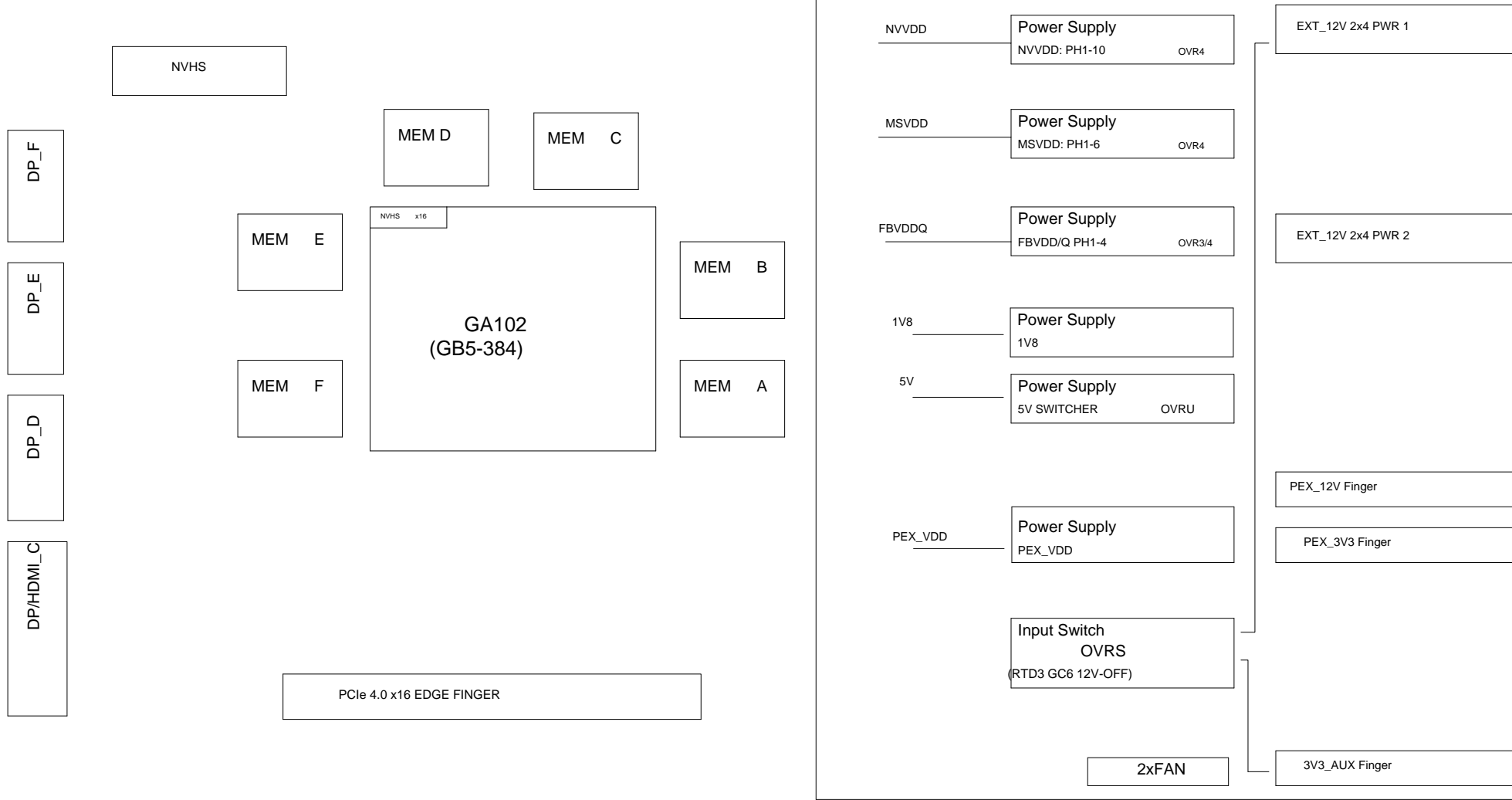
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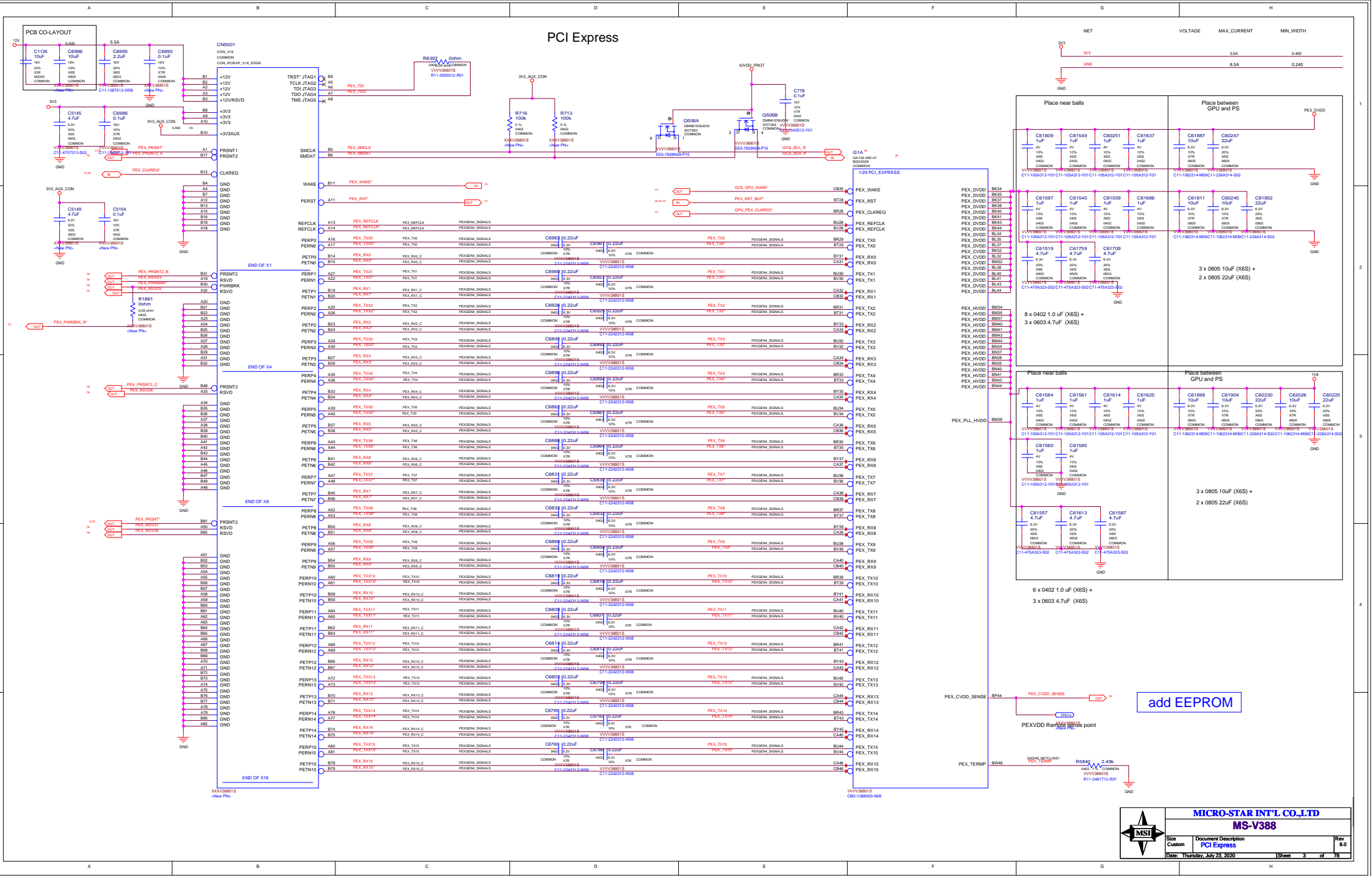
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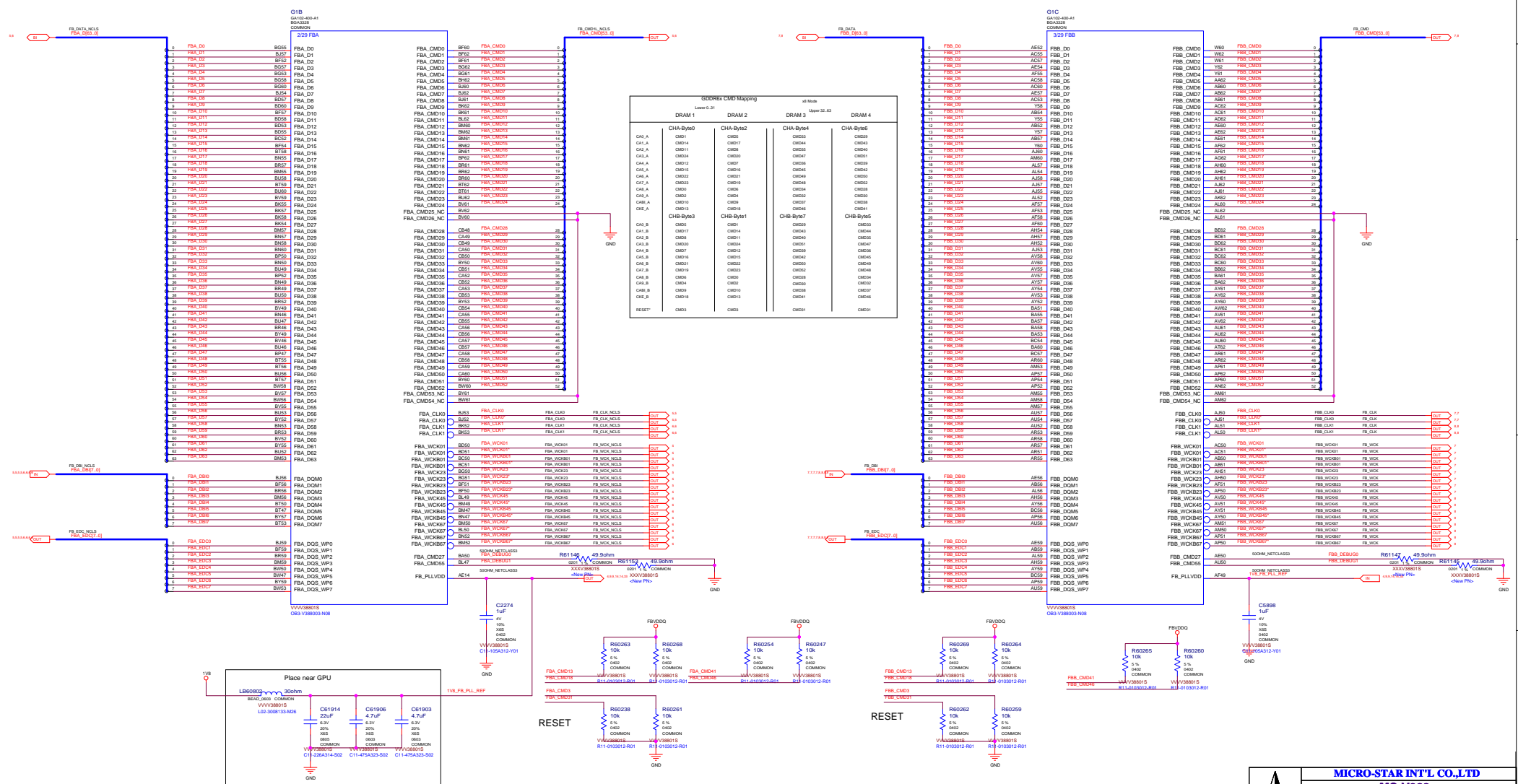
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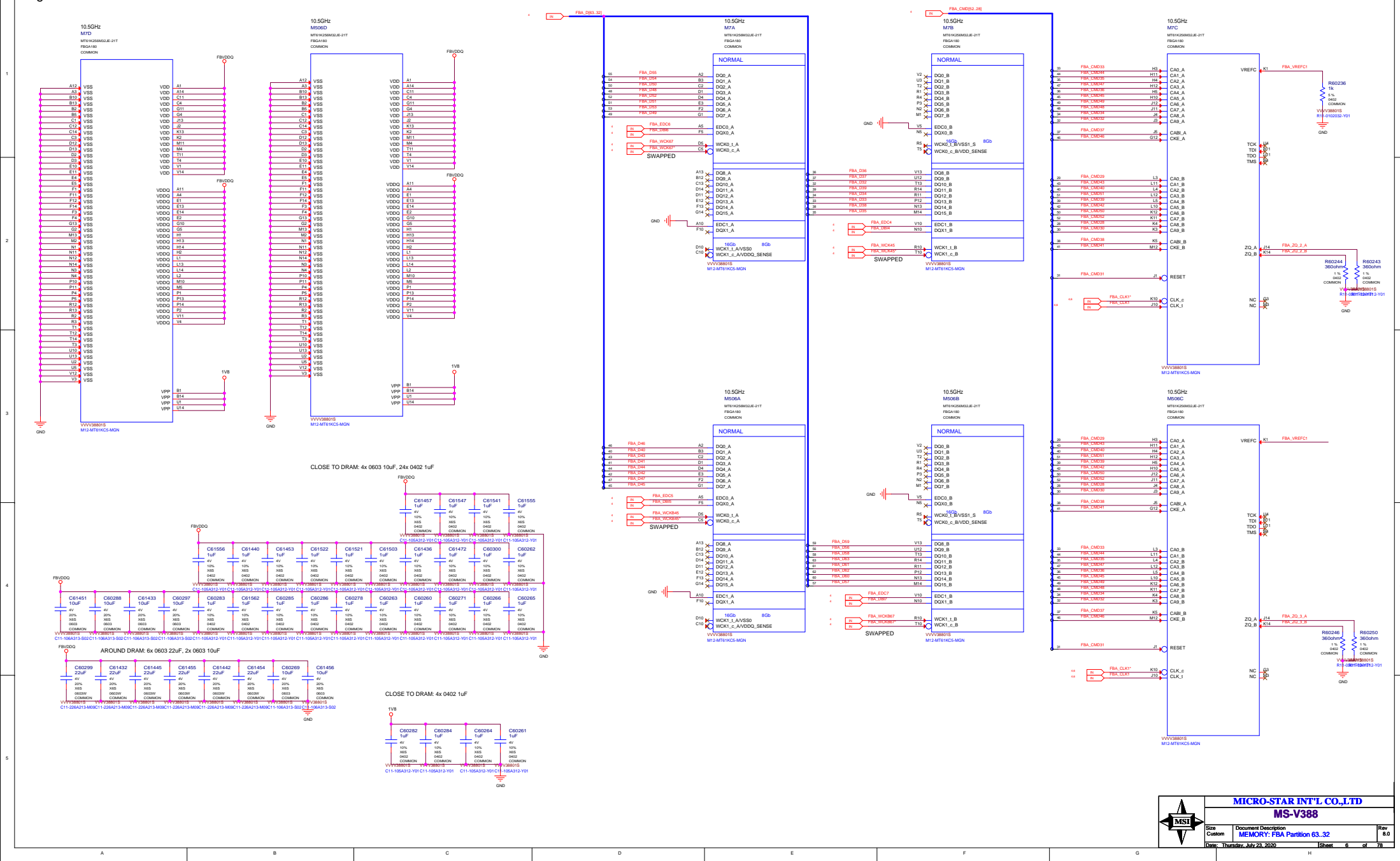
Block Diagram

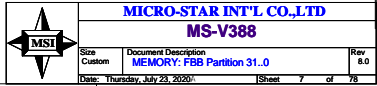


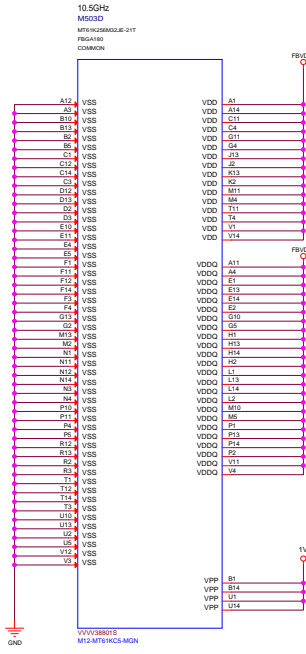




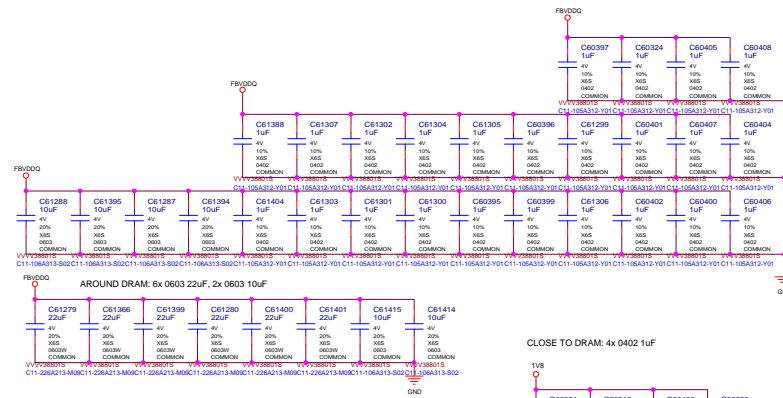




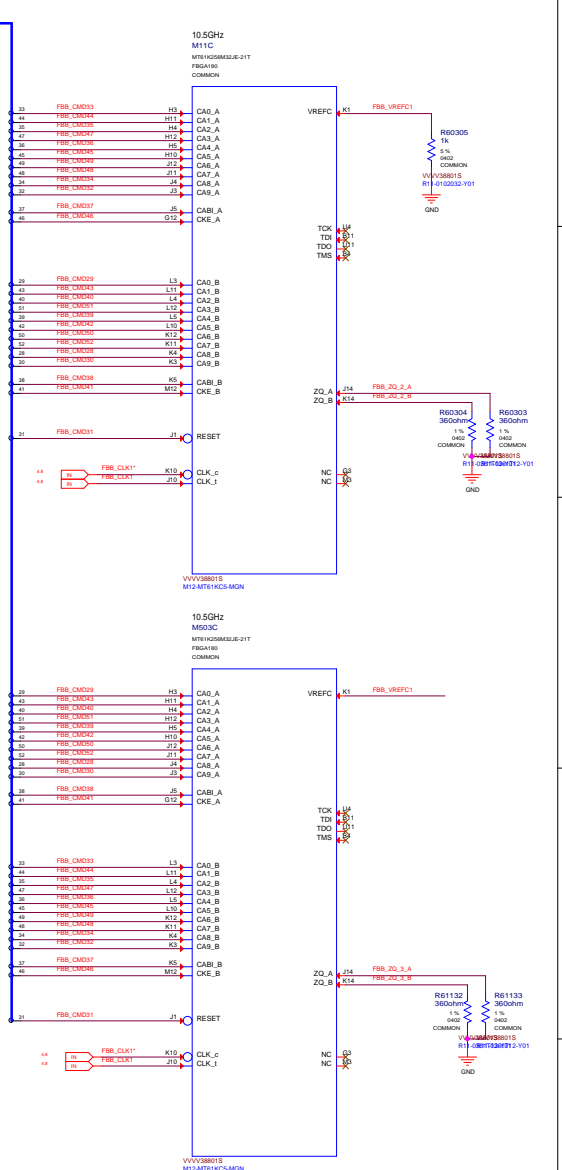
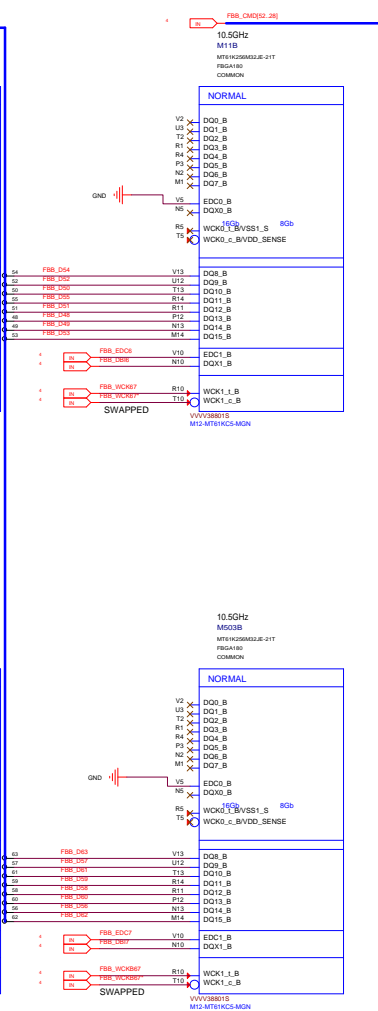
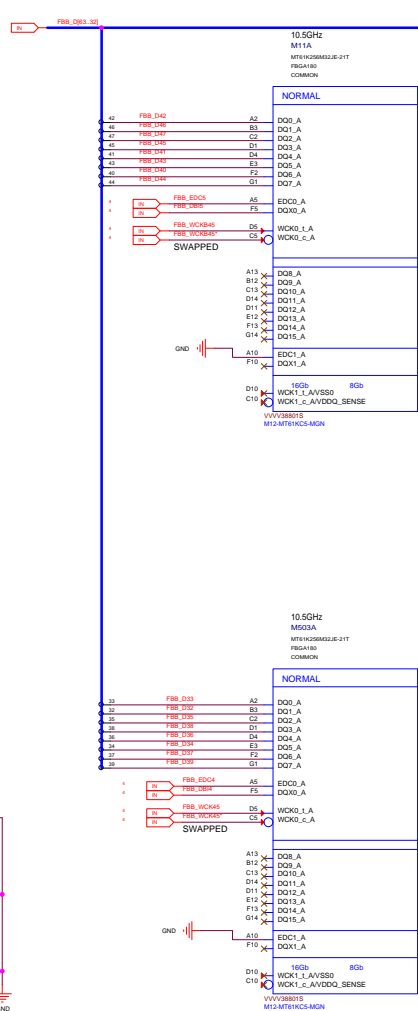
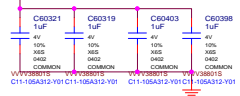




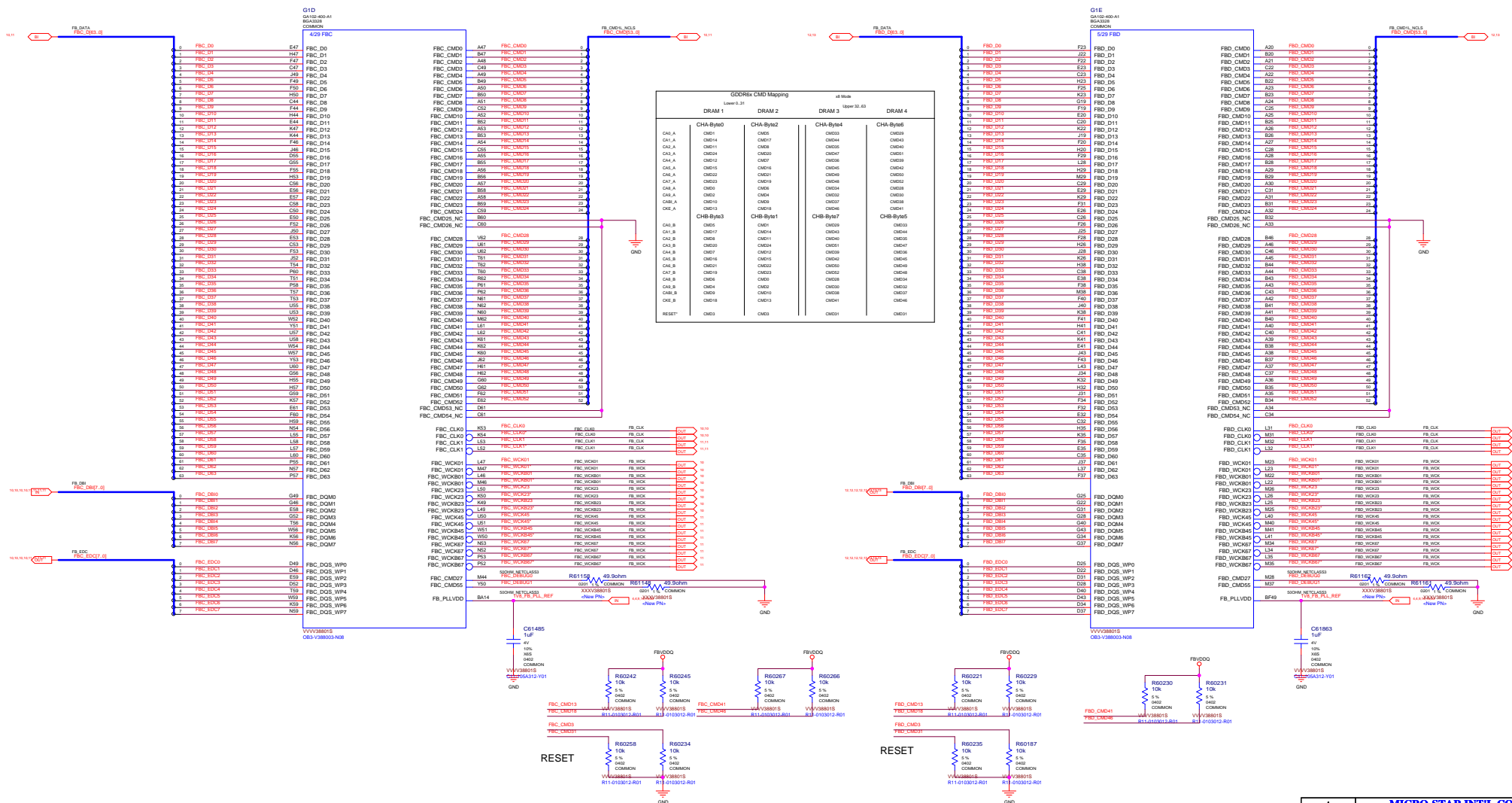
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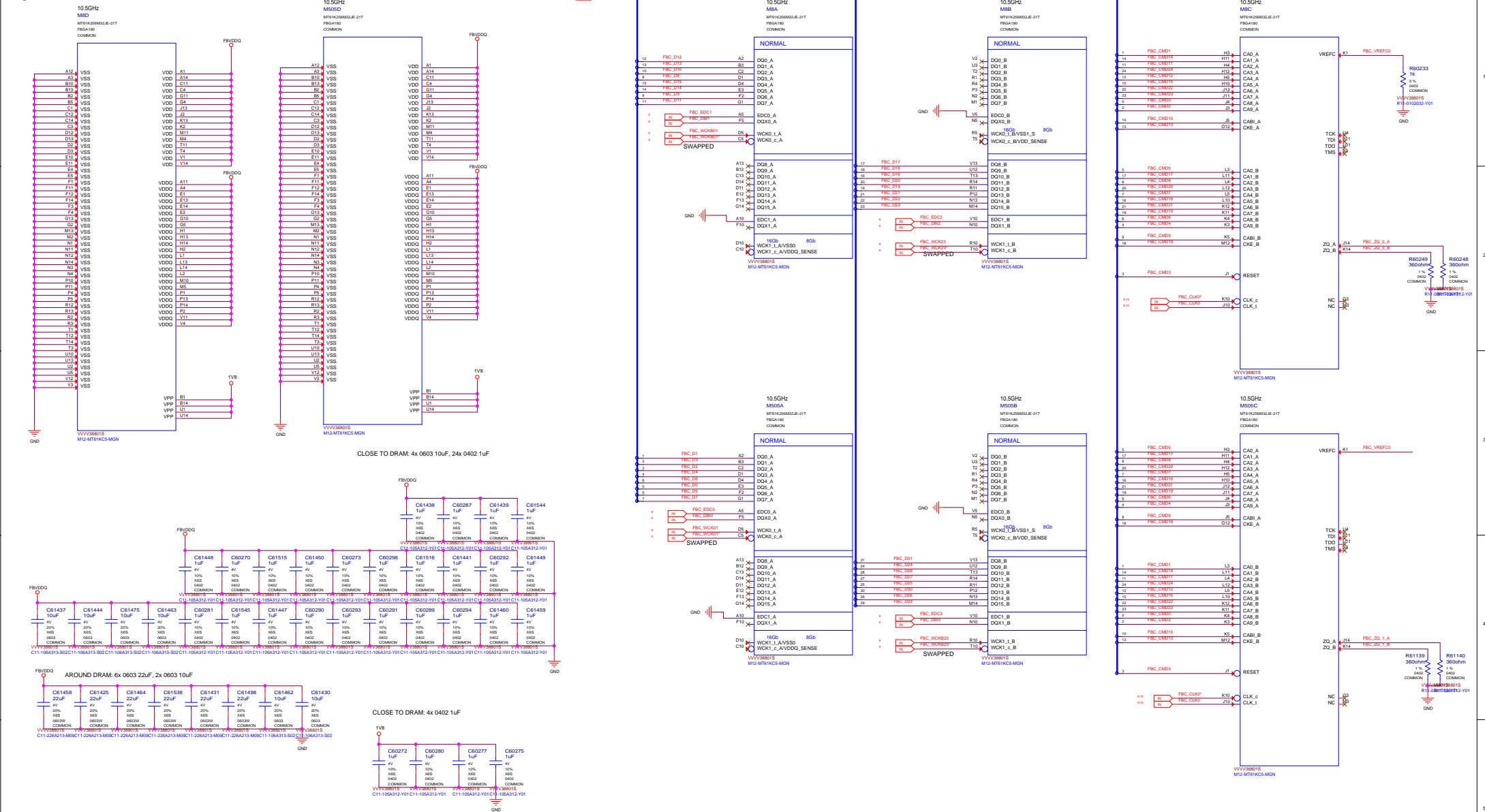


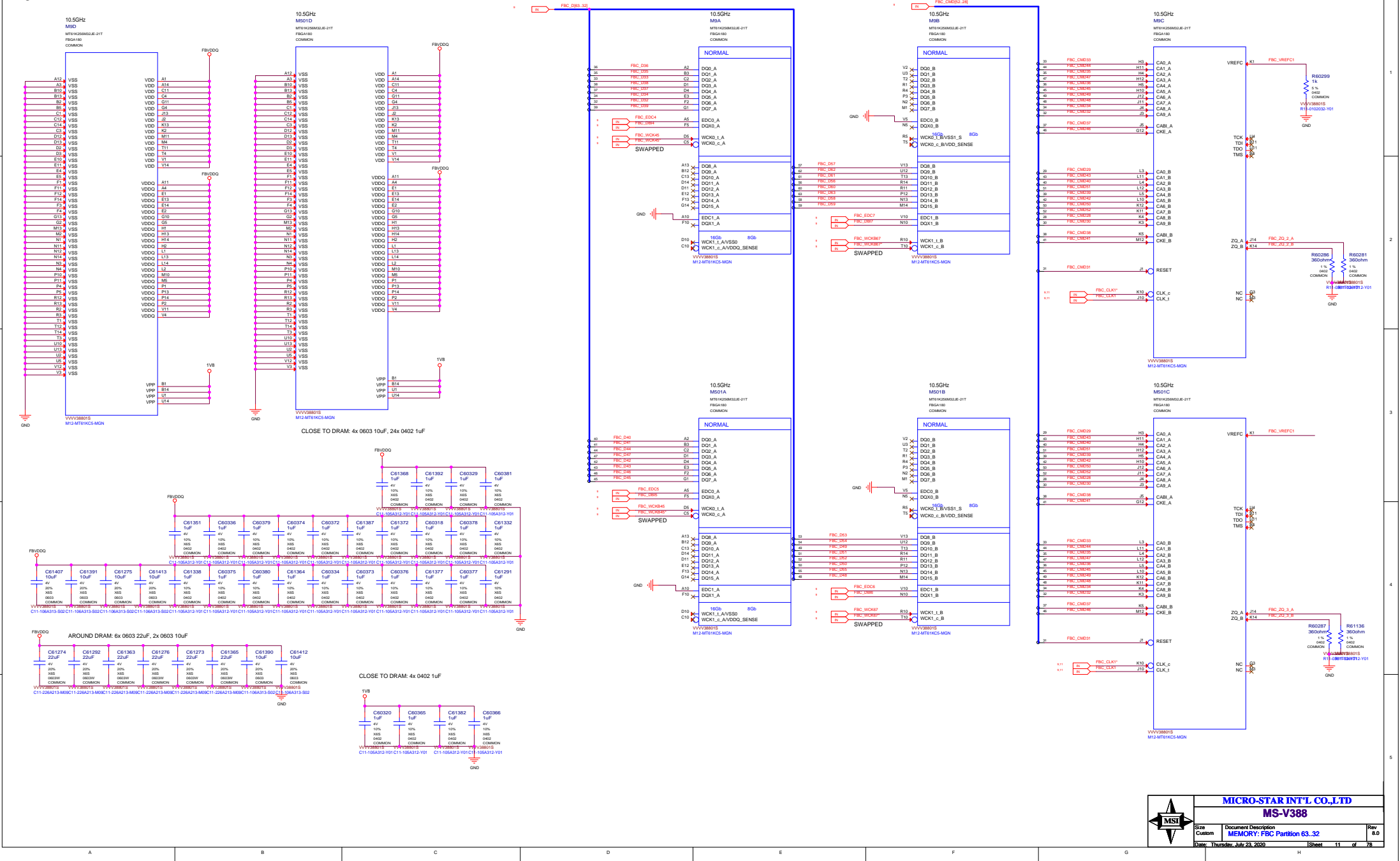
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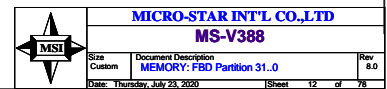
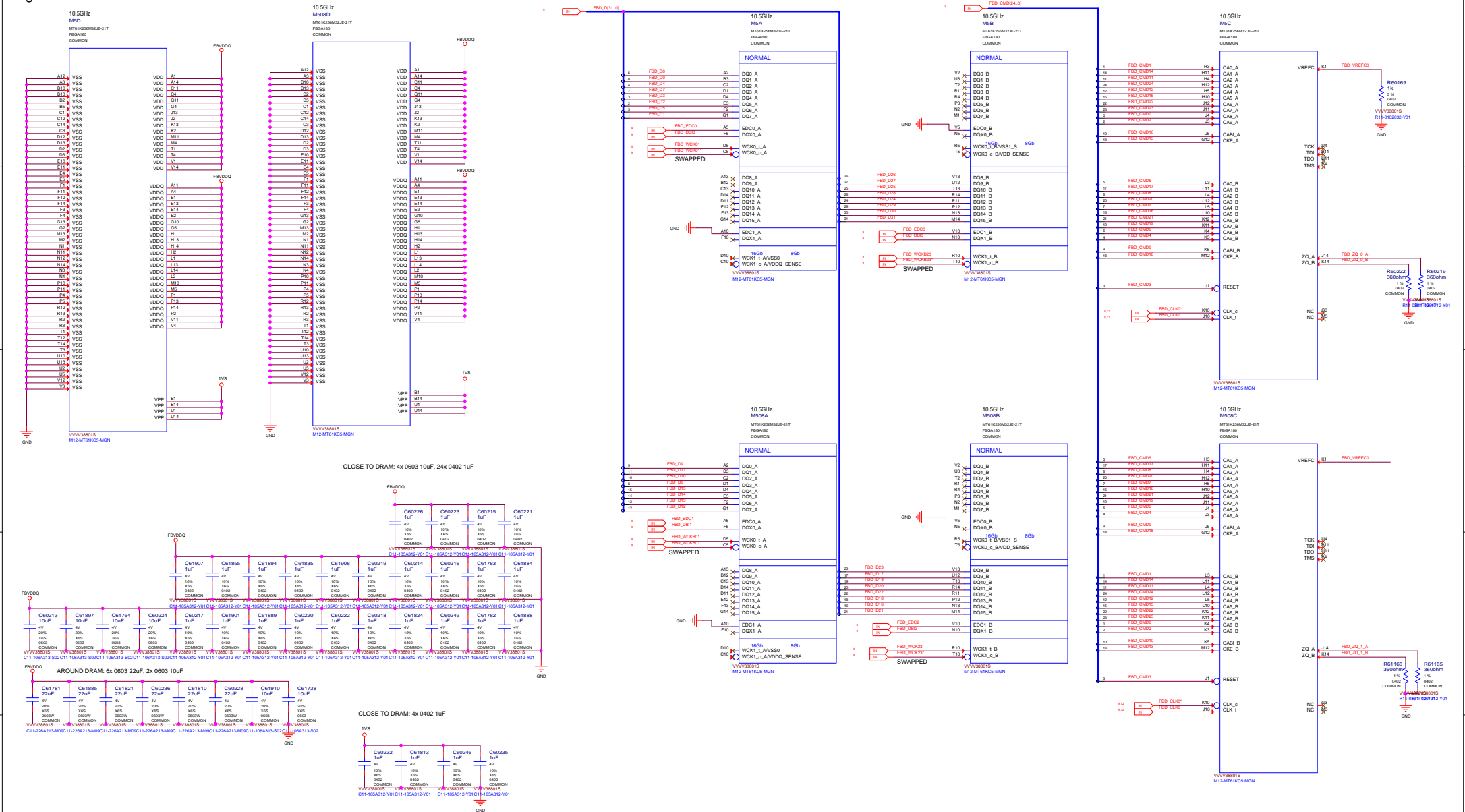


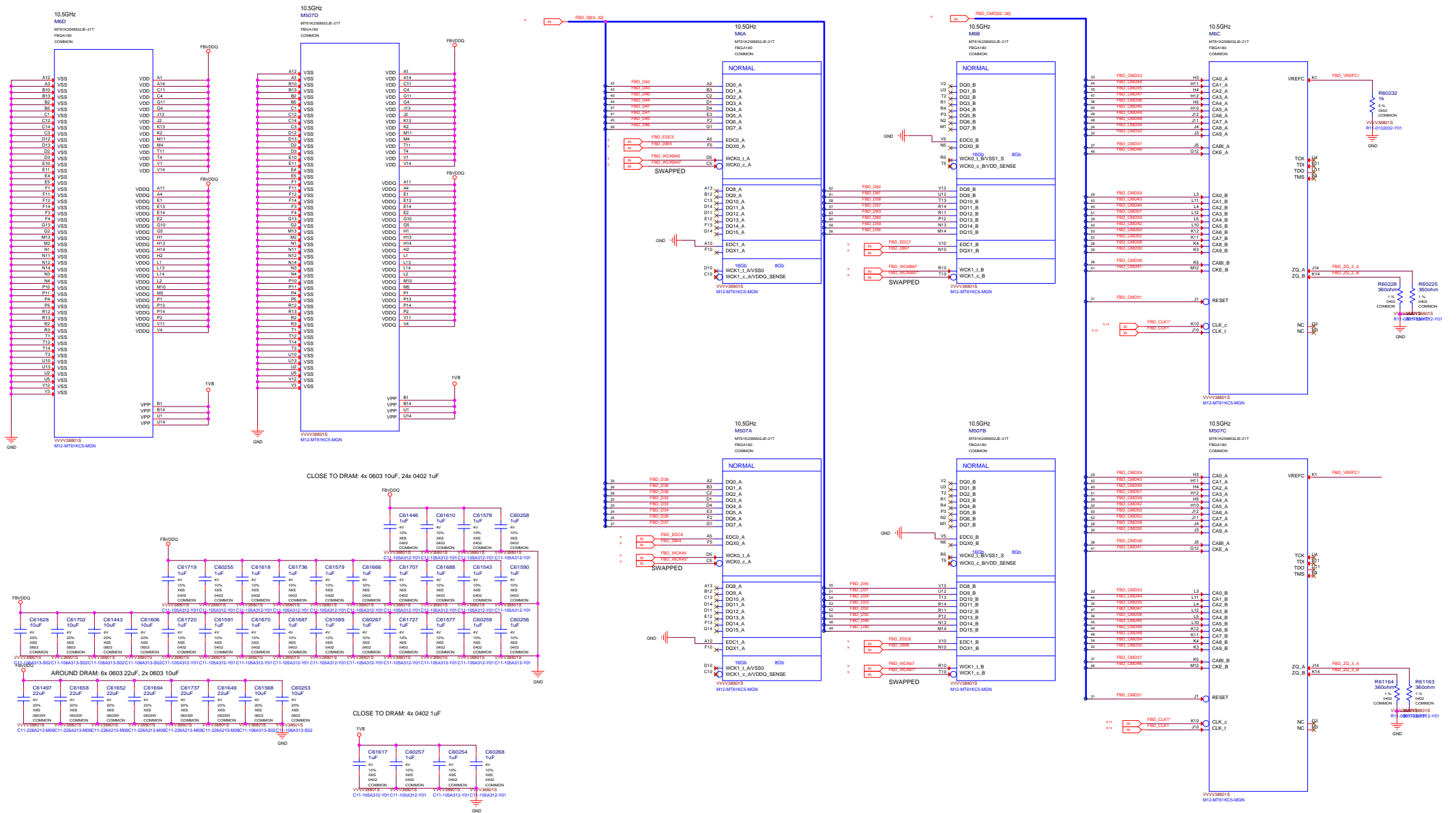
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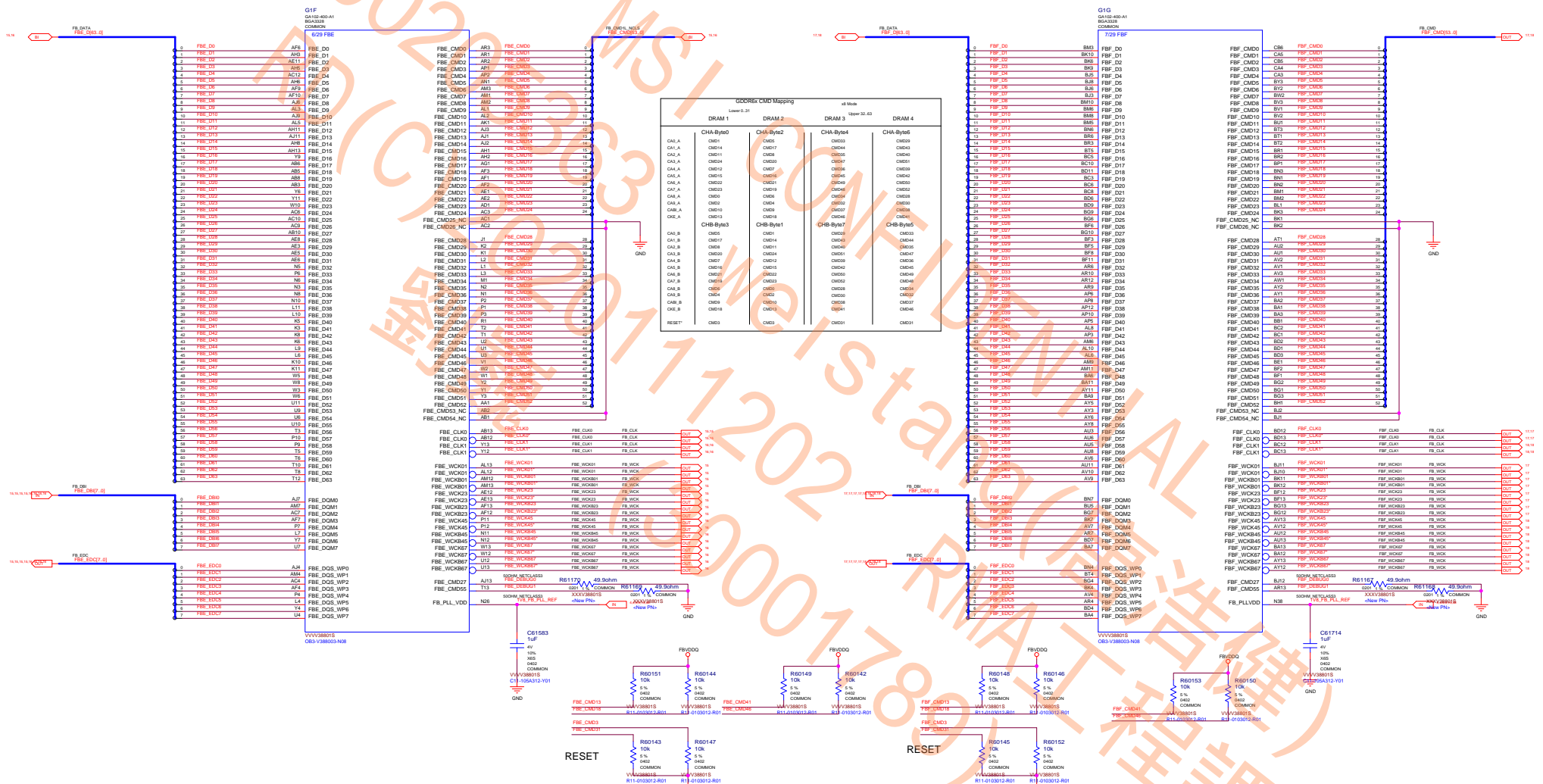


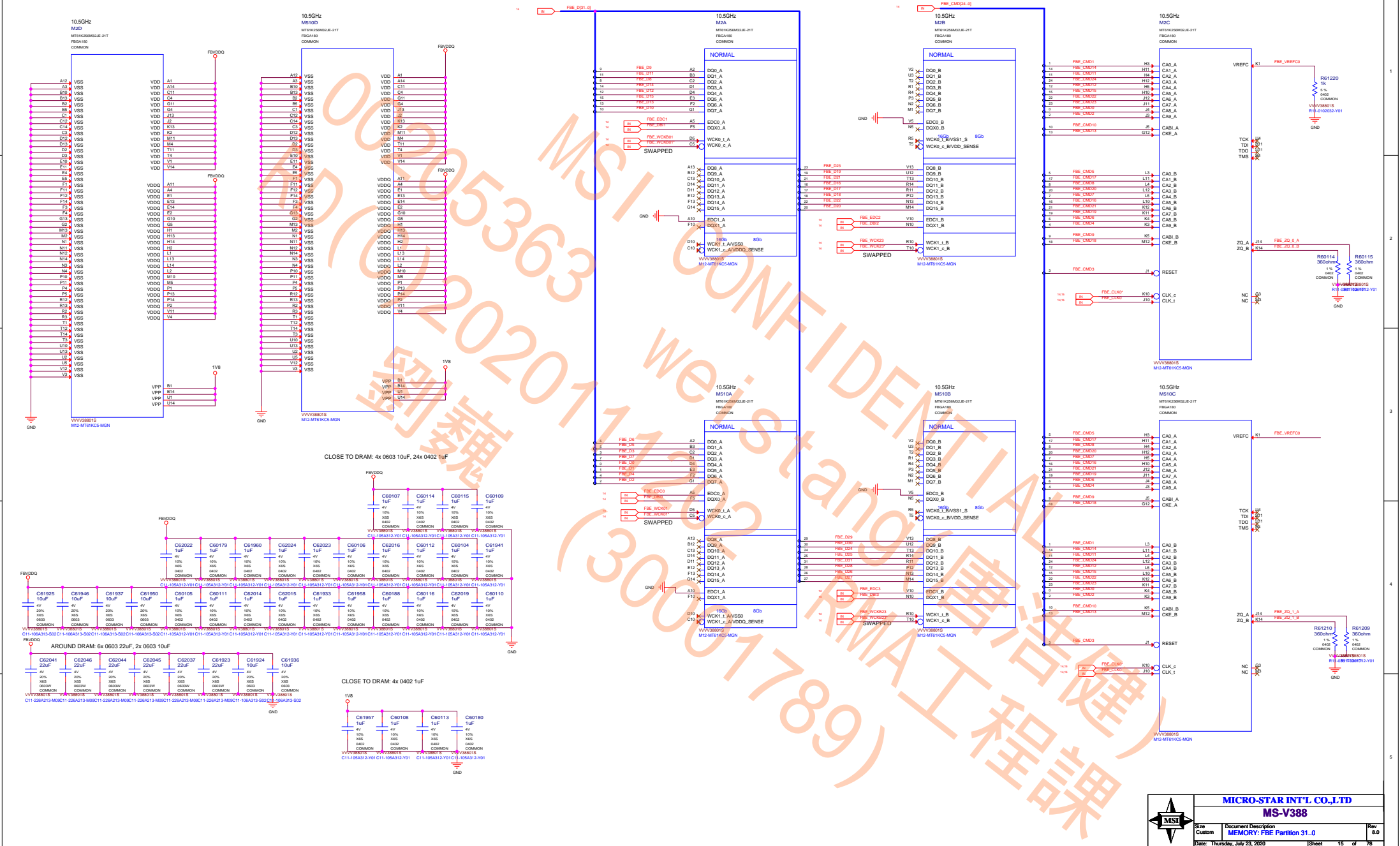


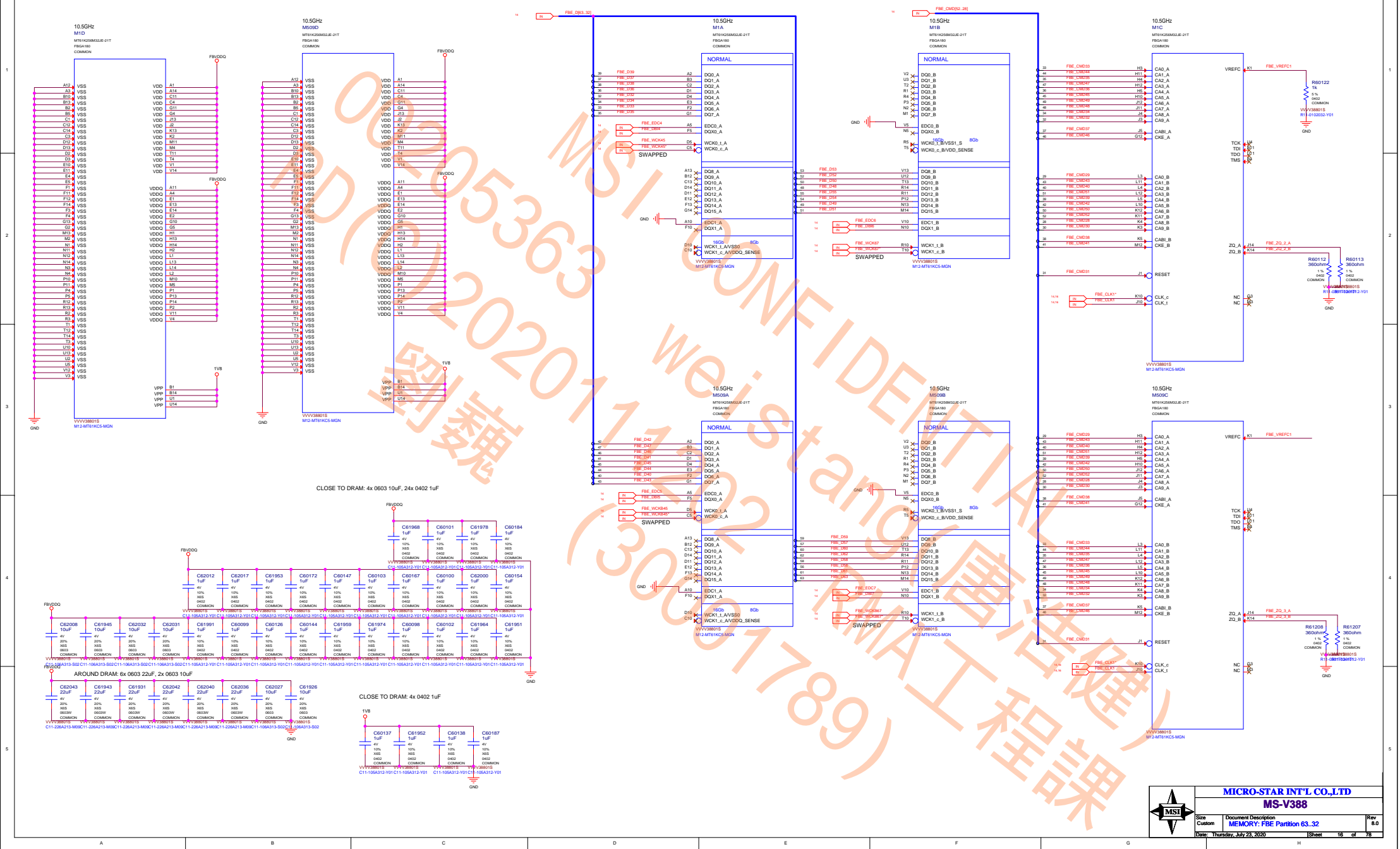


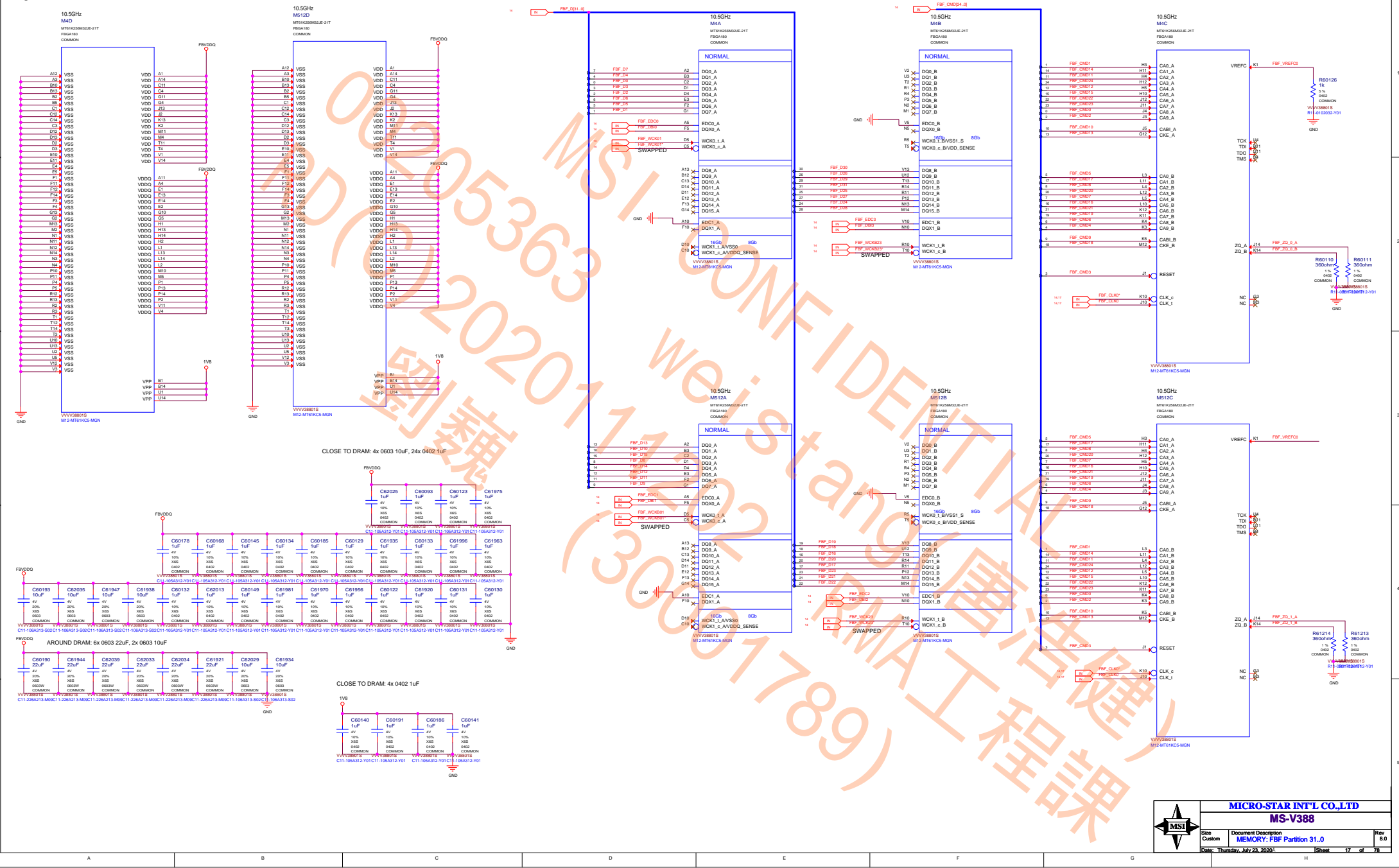


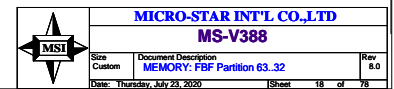
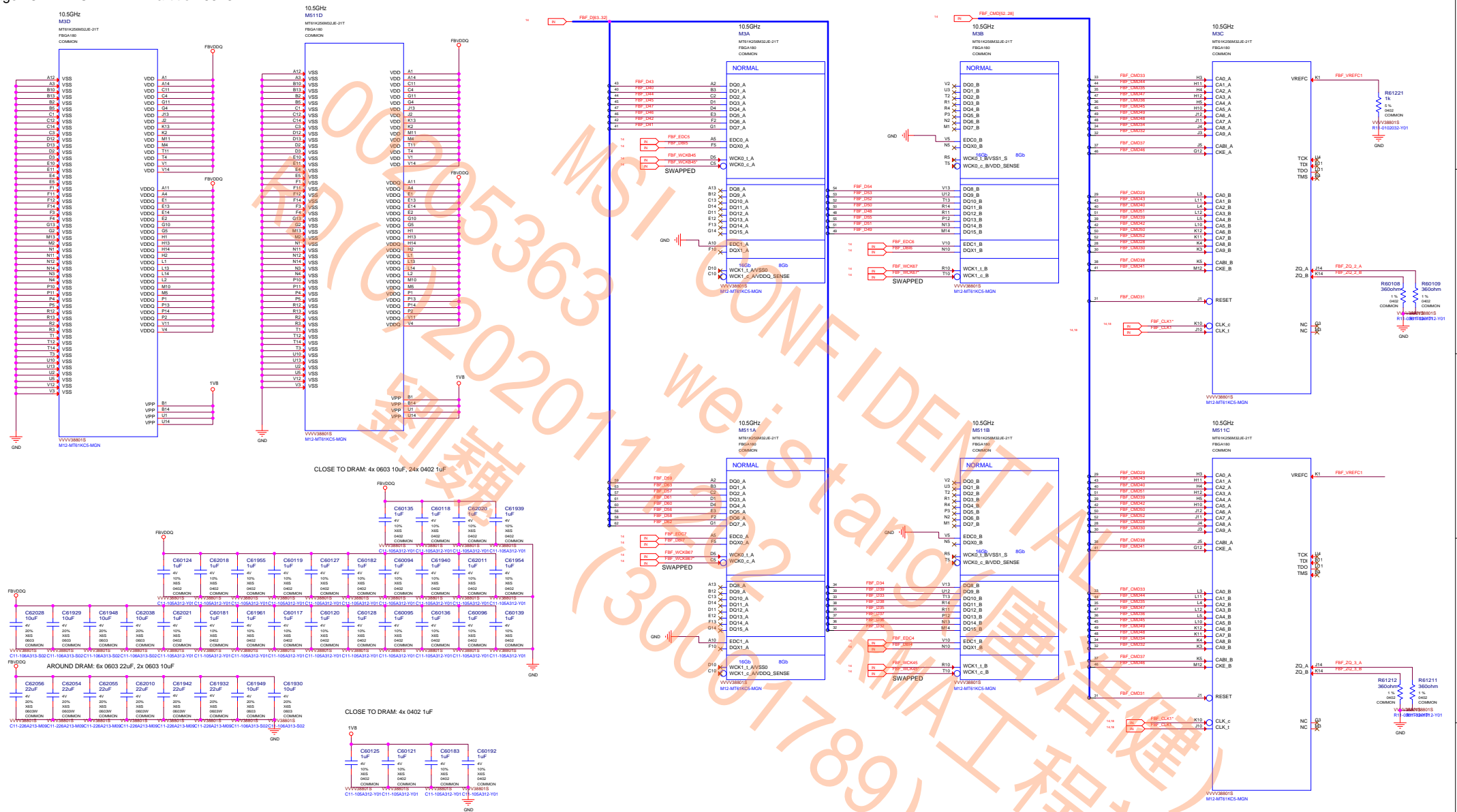








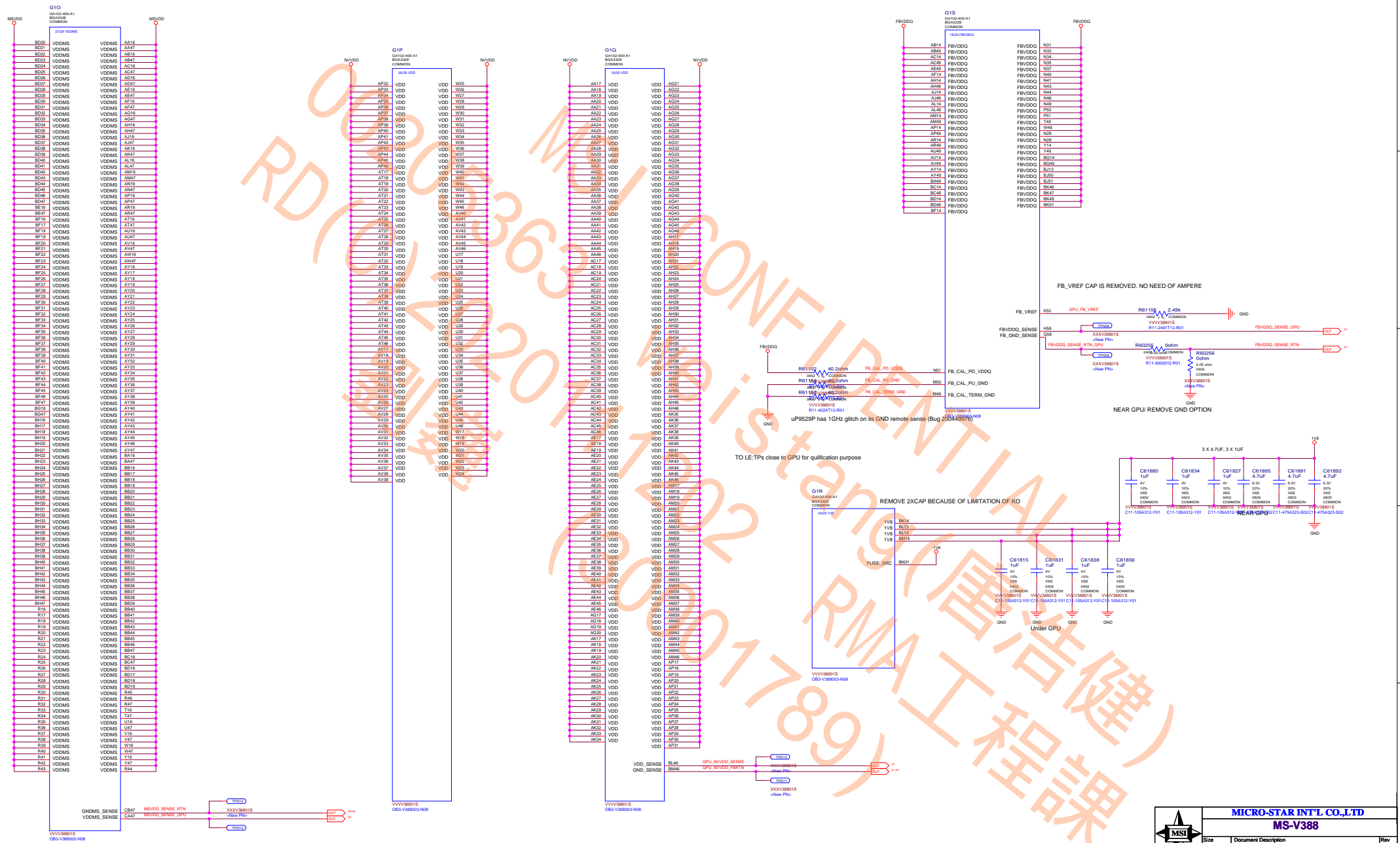




GPU GND, RFUs & RSVD

G1H DA150-400-A1 BOARD COMMON			G1I DA150-400-A1 BOARD COMMON			G1K DA150-400-A1 BOARD COMMON			G1L DA150-400-A1 BOARD COMMON			G1M DA150-400-A1 BOARD COMMON			G1N DA150-400-A1 BOARD COMMON		
2039 GND			2039 GND			2039 GND			2039 GND			2039 NC/DNU			2039 GND		
A11 GND	GND	AD53	A156 GND	GND	AF58	A1923 GND	GND	BC17	BR33	GND	V2	AV	NC	F15	GND	GND	G24
A13 GND	GND	AD56	A158 GND	GND	AF59	A1924 GND	GND	BC18	BR34	GND	V3	AV	NC	F16	GND	GND	G25
A15 GND	GND	AD57	A160 GND	GND	AF60	A1925 GND	GND	BC19	BR35	GND	V4	AV	NC	F17	GND	GND	G26
A17 GND	GND	AD58	A162 GND	GND	AF61	A1926 GND	GND	BC20	BR36	GND	V5	AV	NC	F18	GND	GND	G27
A19	GND	AD59	A164 GND	GND	AF62	A1927 GND	GND	BC21	BR37	GND	V6	AV	NC	F19	GND	GND	G28
A21	GND	AD60	A166 GND	GND	AF63	A1928 GND	GND	BC22	BR38	GND	V7	AV	NC	F20	GND	GND	G29
A23	GND	AD61	A168 GND	GND	AF64	A1929 GND	GND	BC23	BR39	GND	V8	AV	NC	F21	GND	GND	G30
A25	GND	AD62	A170 GND	GND	AF65	A1930 GND	GND	BC24	BR40	GND	V9	AV	NC	F22	GND	GND	G31
A27	GND	AD63	A172 GND	GND	AF66	A1931 GND	GND	BC25	BR41	GND	V10	AV	NC	F23	GND	GND	G32
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A57	GND	AD78	A202 GND	GND	AF81	A1946 GND	GND	BC40	BR56	GND	V25	AV	NC	F38	GND	GND	G47
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GPU PWR and GND



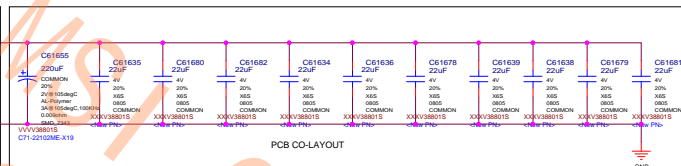
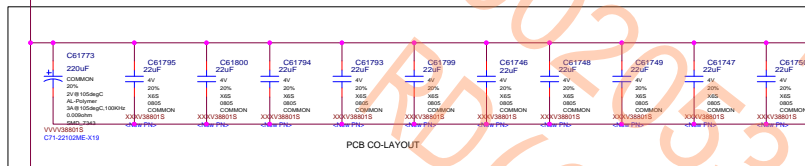
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Size Custom	Document Description GPU PWR and GND	Rev 8.0
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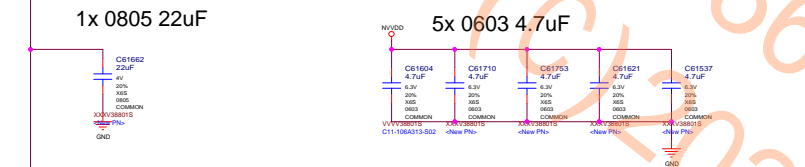
NVVDD

UNDER GPU

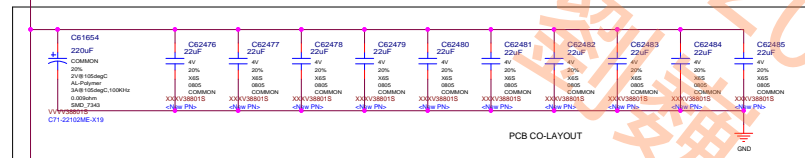
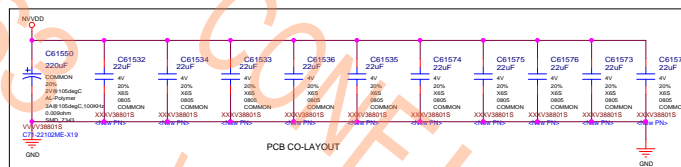
4x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 0805 22uF)



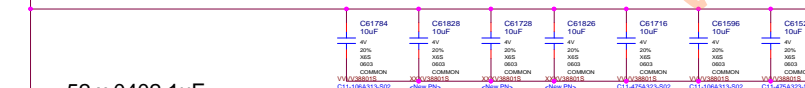
1x 0805 22uF



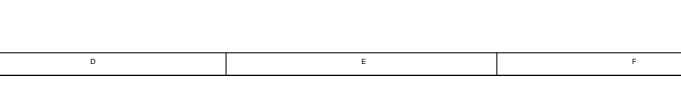
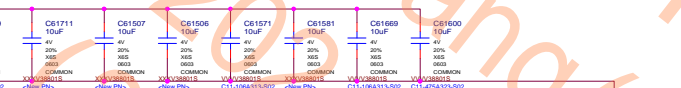
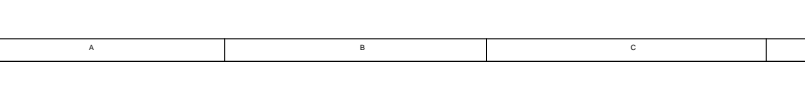
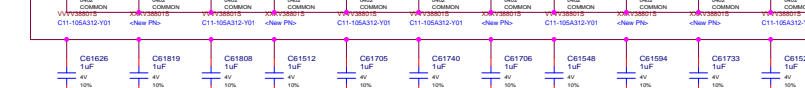
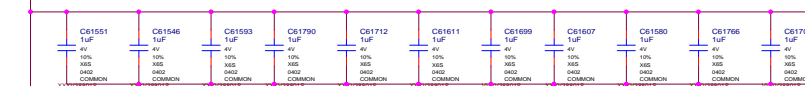
5x 0603 4.7uF



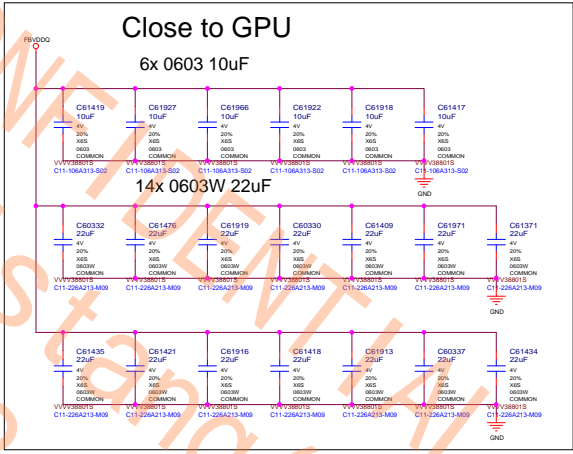
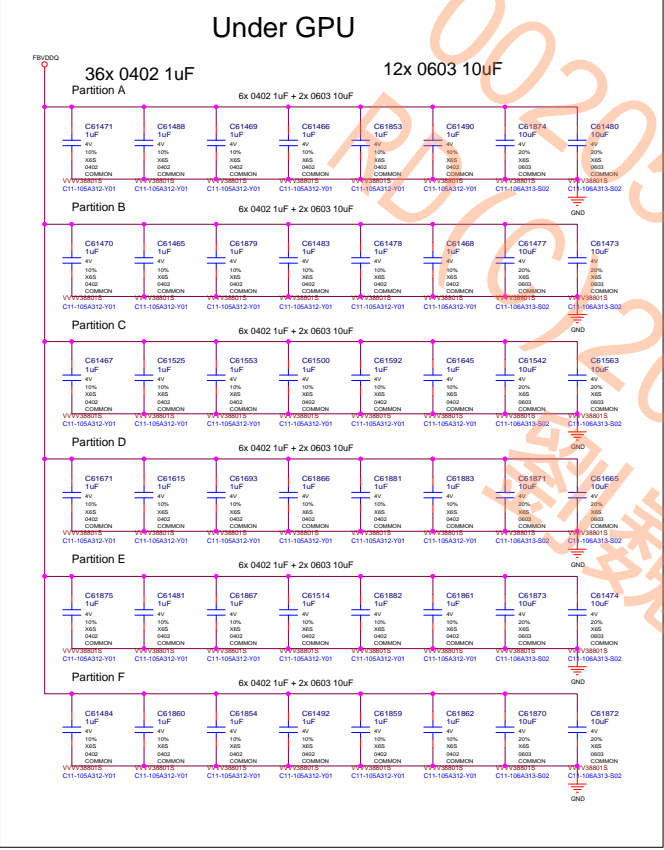
14x 0603 10uF



52 x 0402 1uF

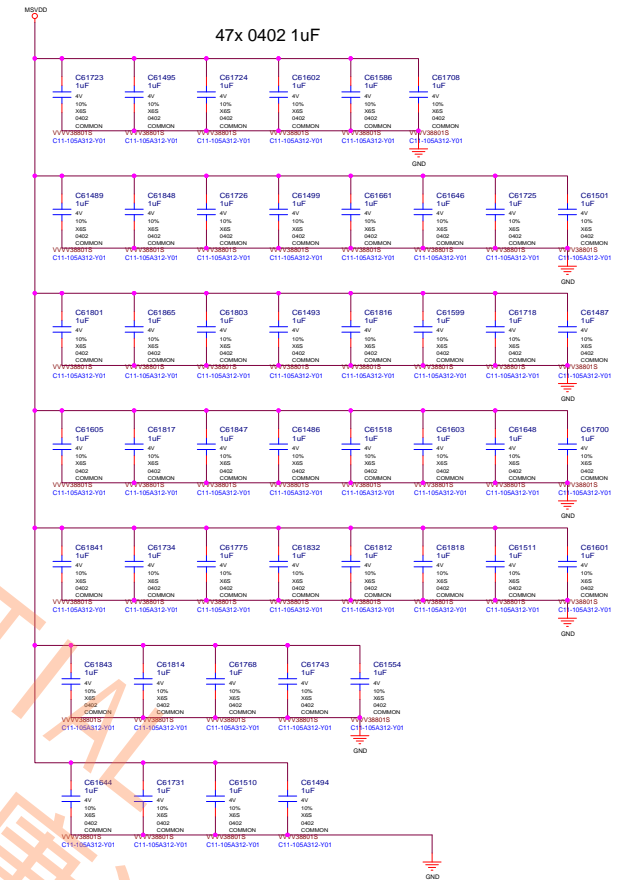
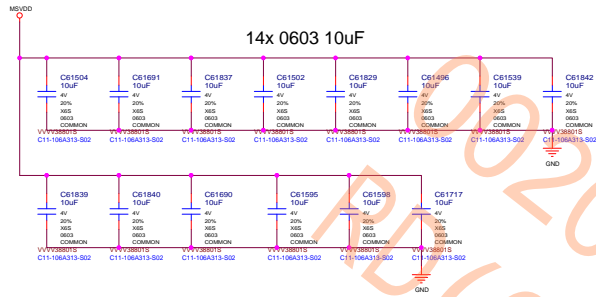


FBVDDQ

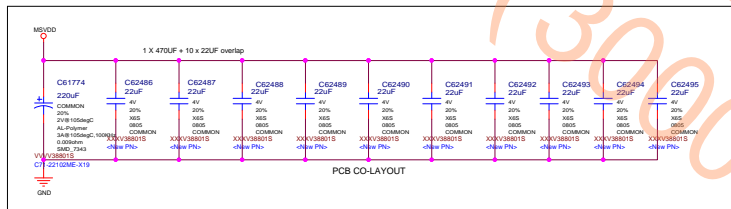
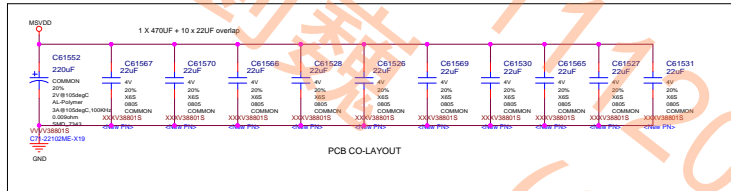


MSVDD

UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3x 1uF 0402 DUE TO SPACE RESTRICTION

BLANK

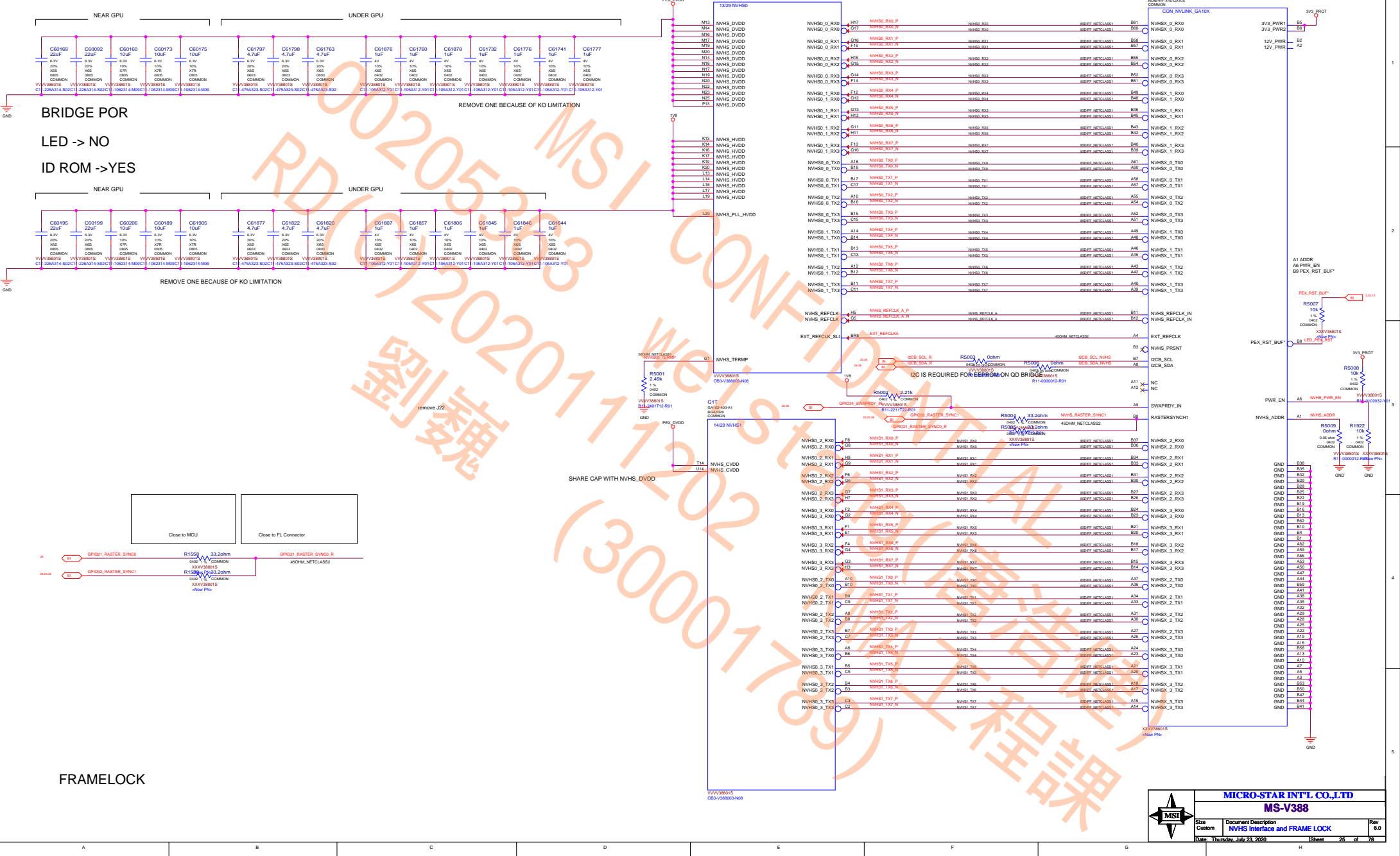


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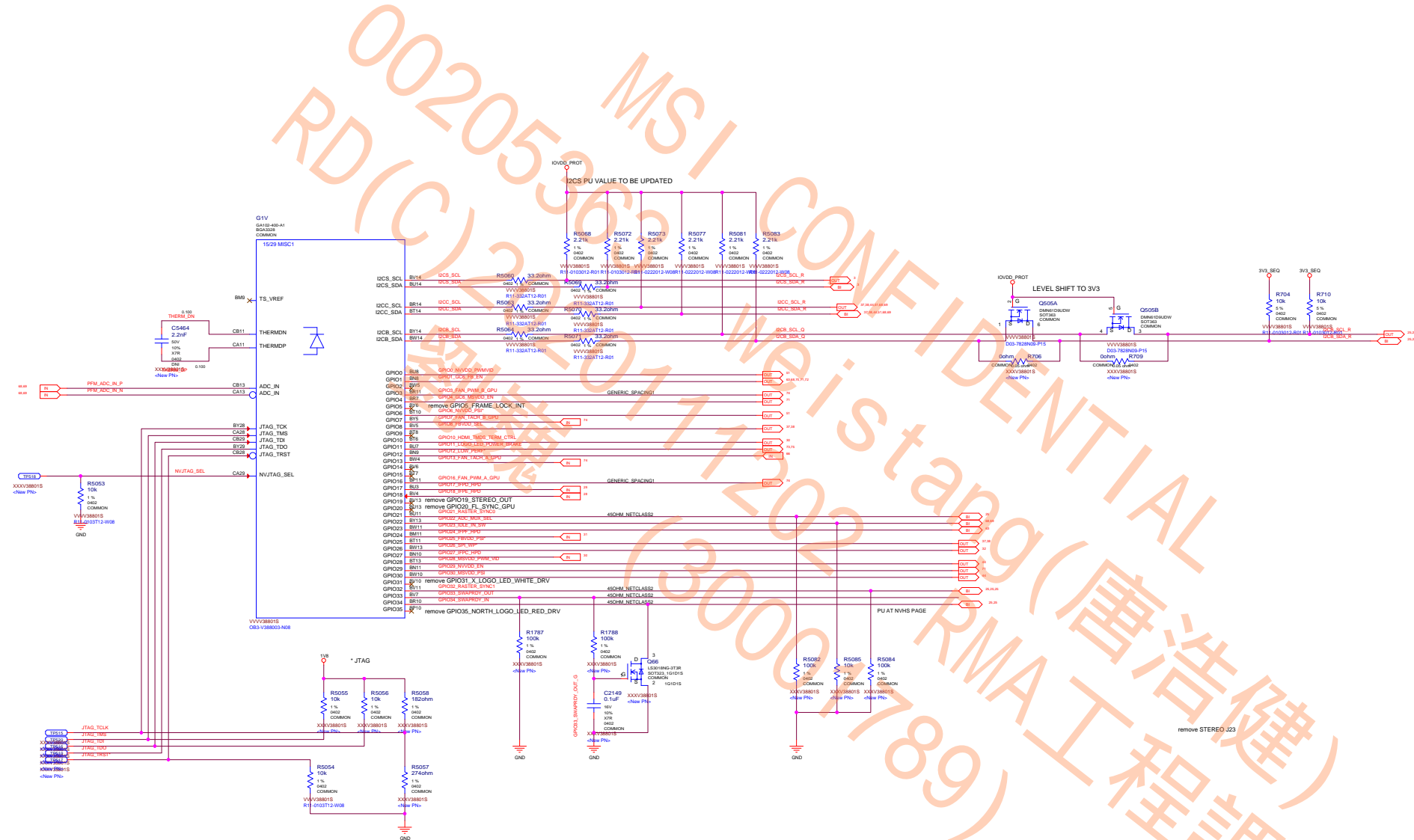
MS-V388

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NVHS Interface and FRAME LOCK



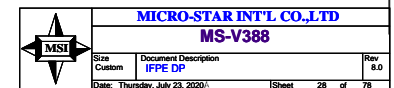
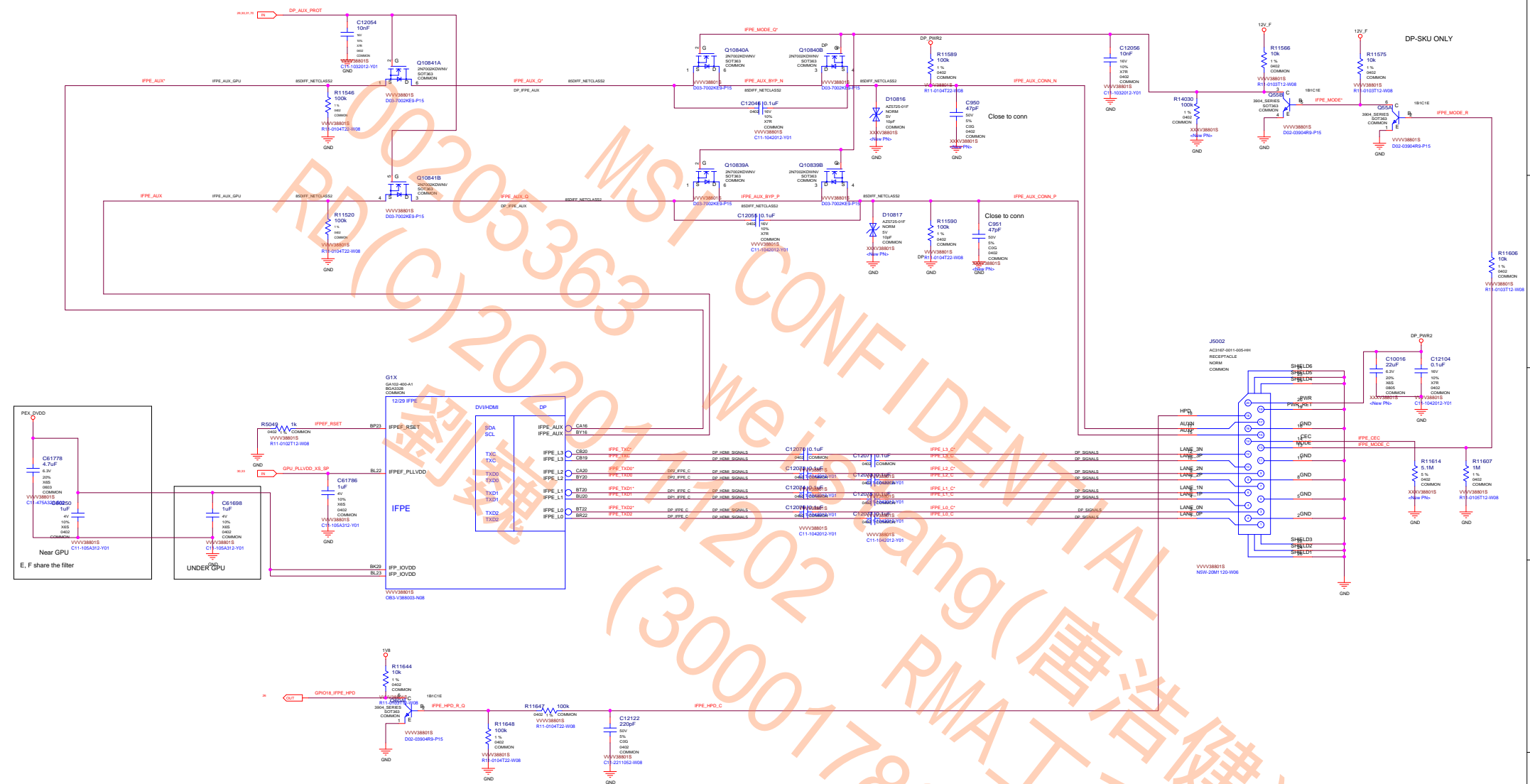
MISC1: Fan, Thermal, JTAG, GPIO, STEREO

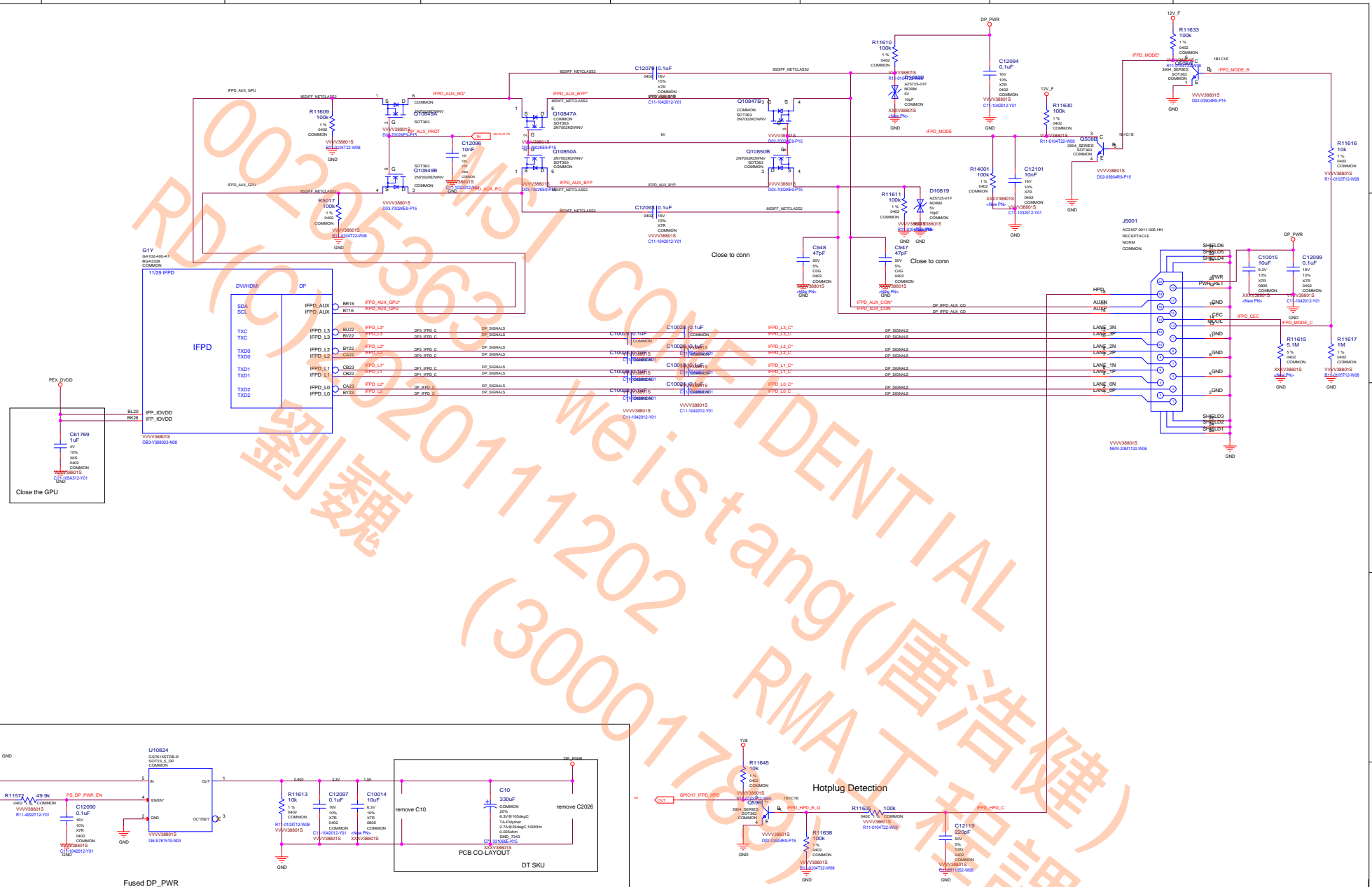


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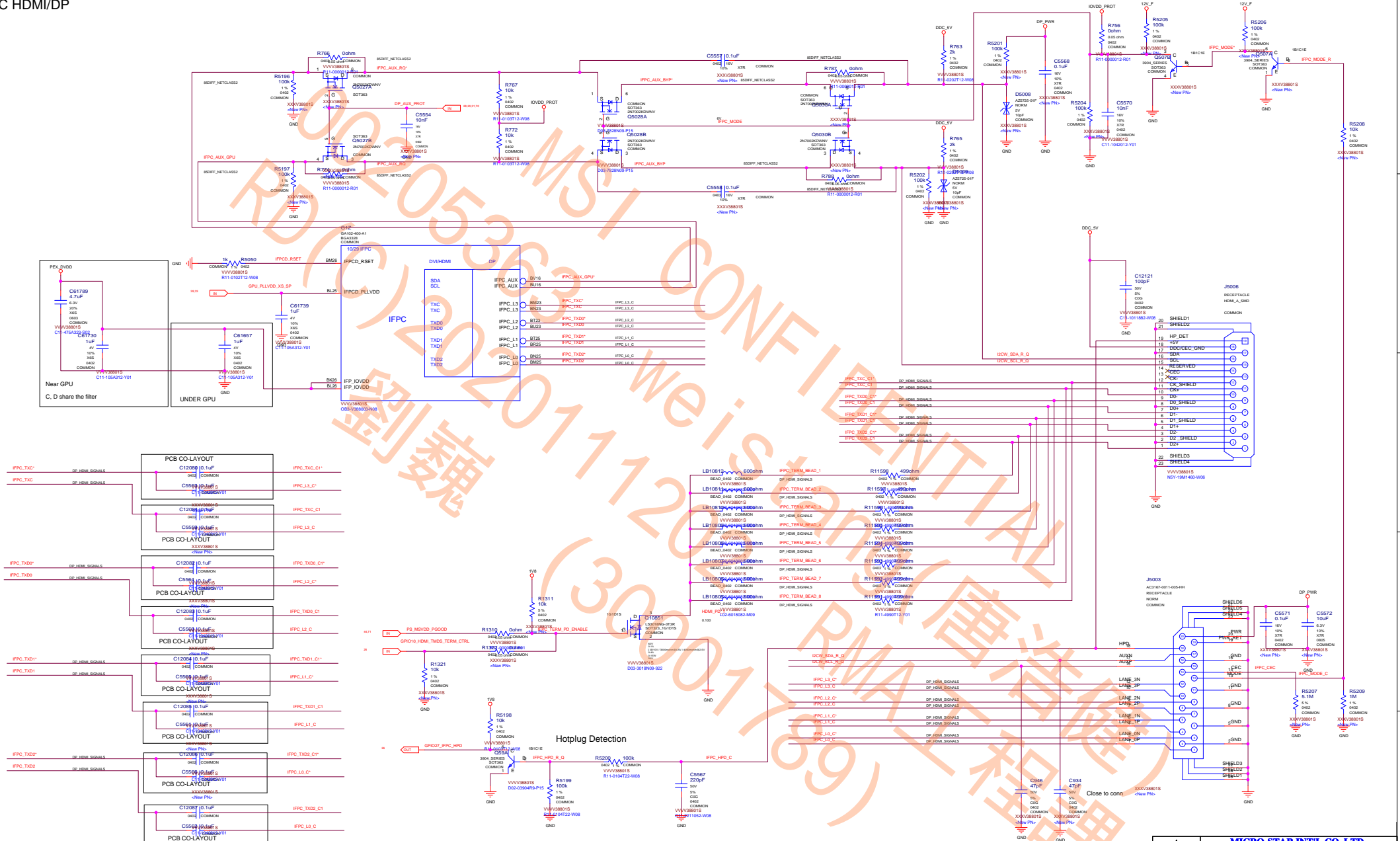
Size Custom	Document Description MISC1: Fan, Thermal, JTAG, GPIO, STEREO	Rev 8.0
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IFPE DP





IFPC HDMI/DP



MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb 19Gbps
L	H	L	00010	RAMCFG TBD
H	L	L	00100	RAMCFG TBD
H	L	H	00101	RAMCFG TBD
H	L	H	00101	RAMCFG MICRON 8Gb 21Gbps

DEFAULT

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0]/FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	H	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

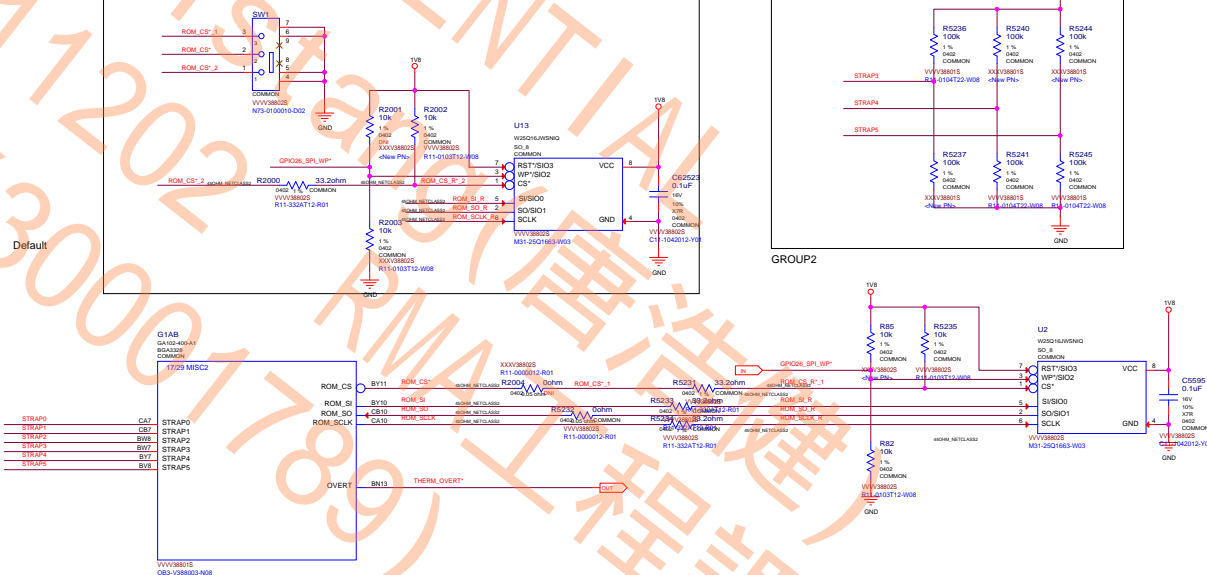
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

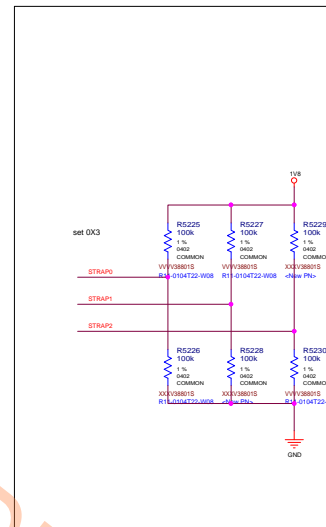
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

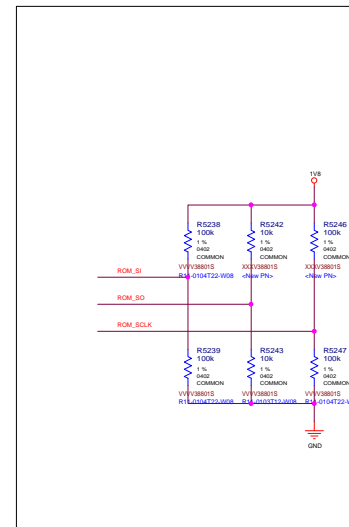
Dual BIOS



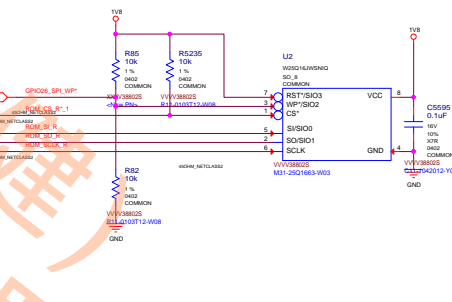
GROUP0



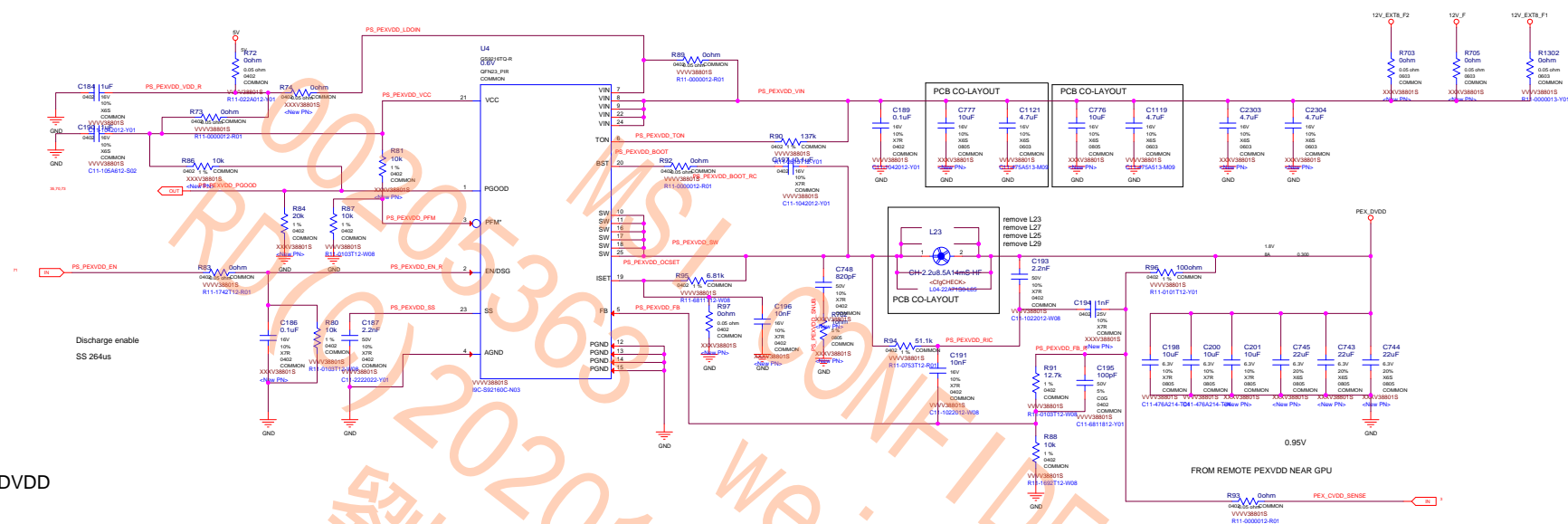
GROUP1



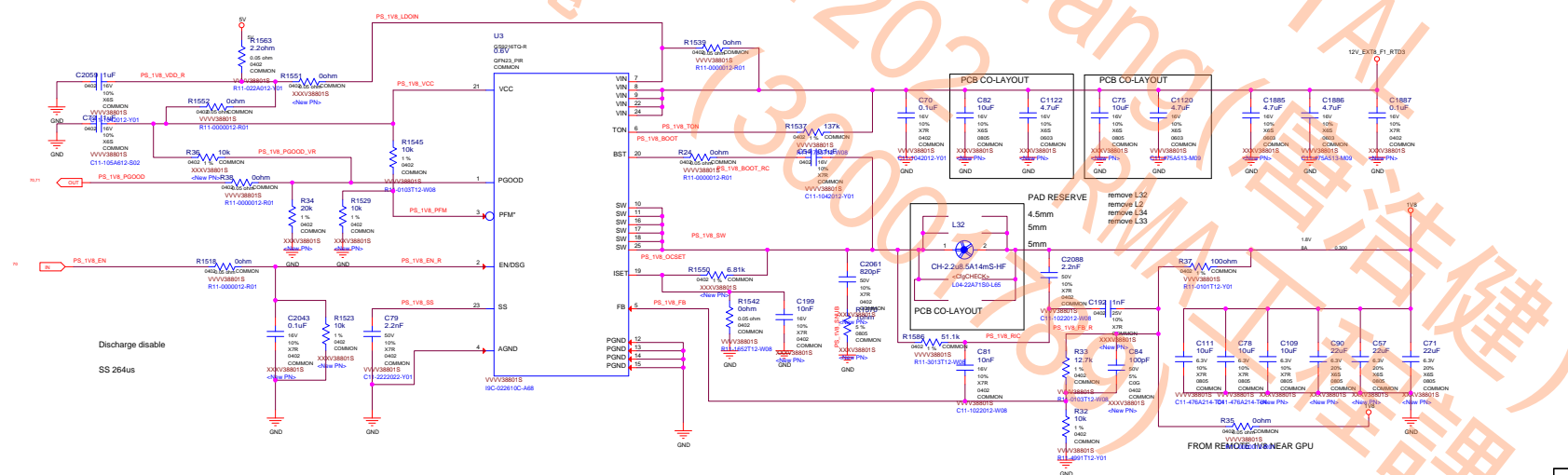
GROUP2



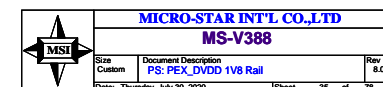
PS: PEX_DVDD 1V8 Rail



PEX_DVDD




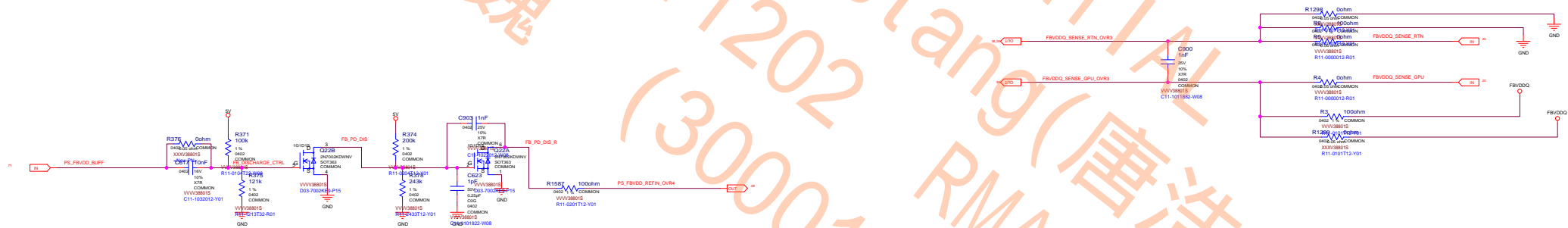
1V8



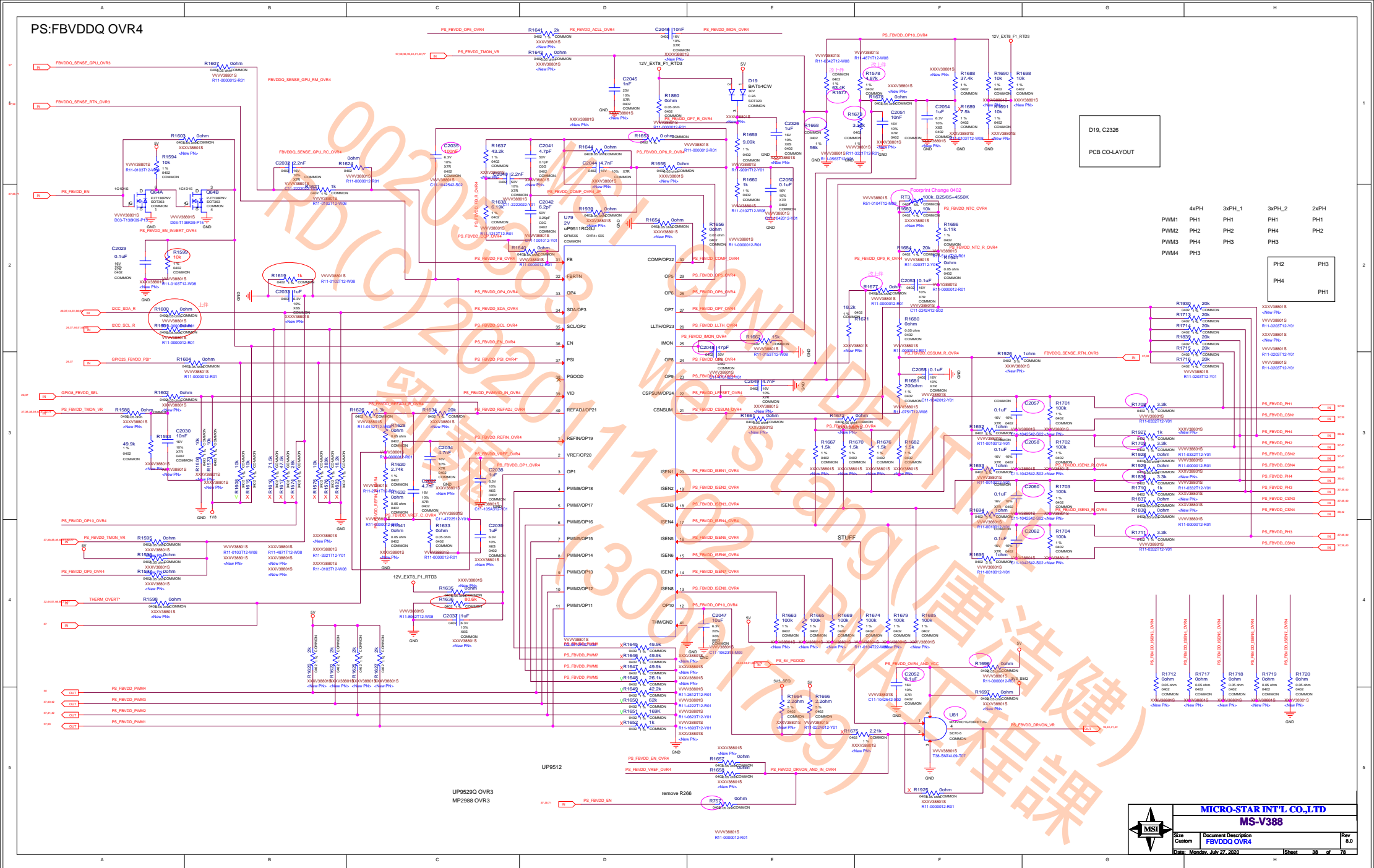
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唐浩健
RMA工程課
(30001789)

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	Size	Document Description	Rev
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Date: Wednesday, July 22, 2020		Sheet 36 of 78	



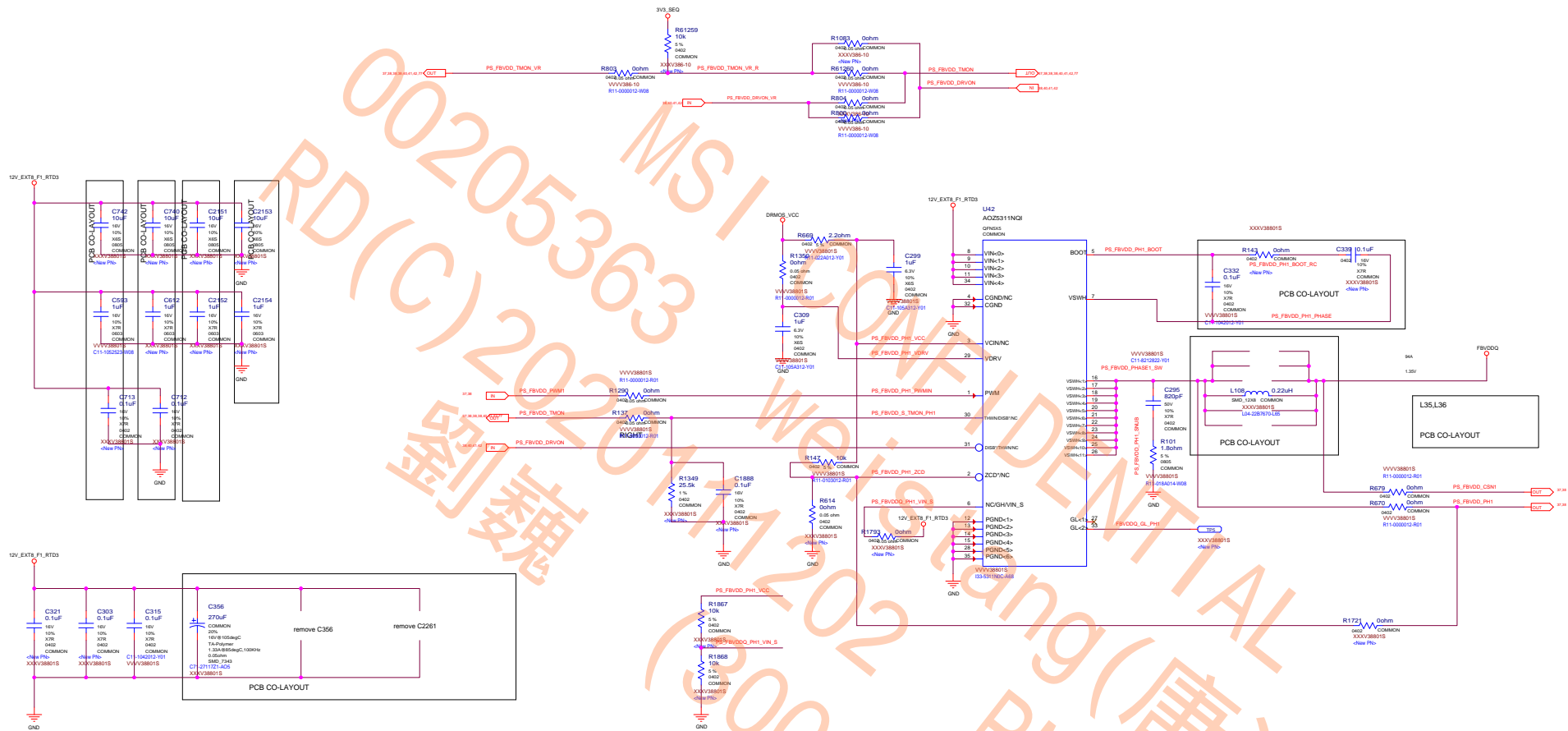
PS:FBVDDQ OVR4



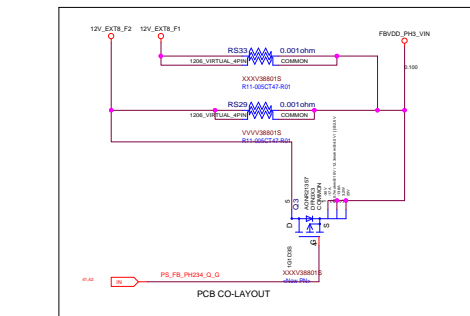
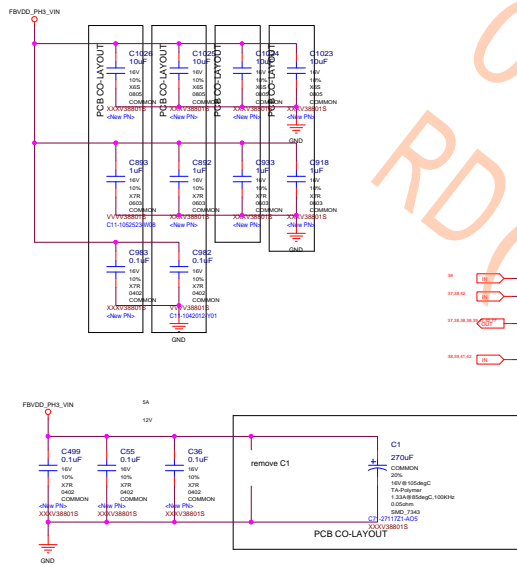
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Date: Monday, July 27, 2020		Sheet 28 of 28

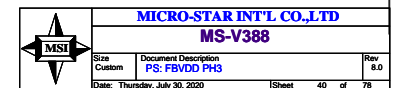
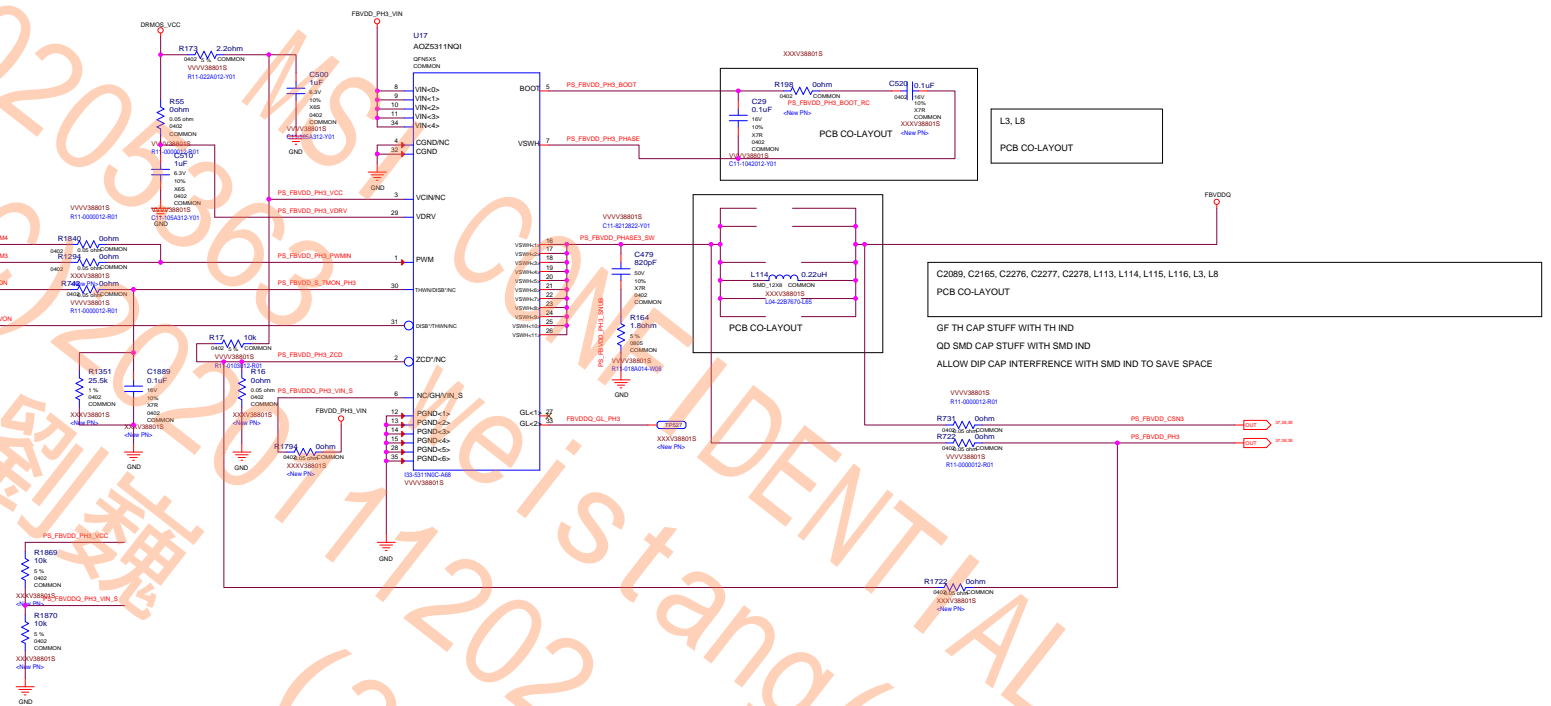
PS: FBVDD PH1



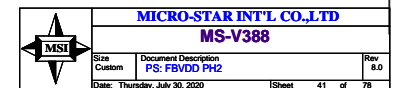
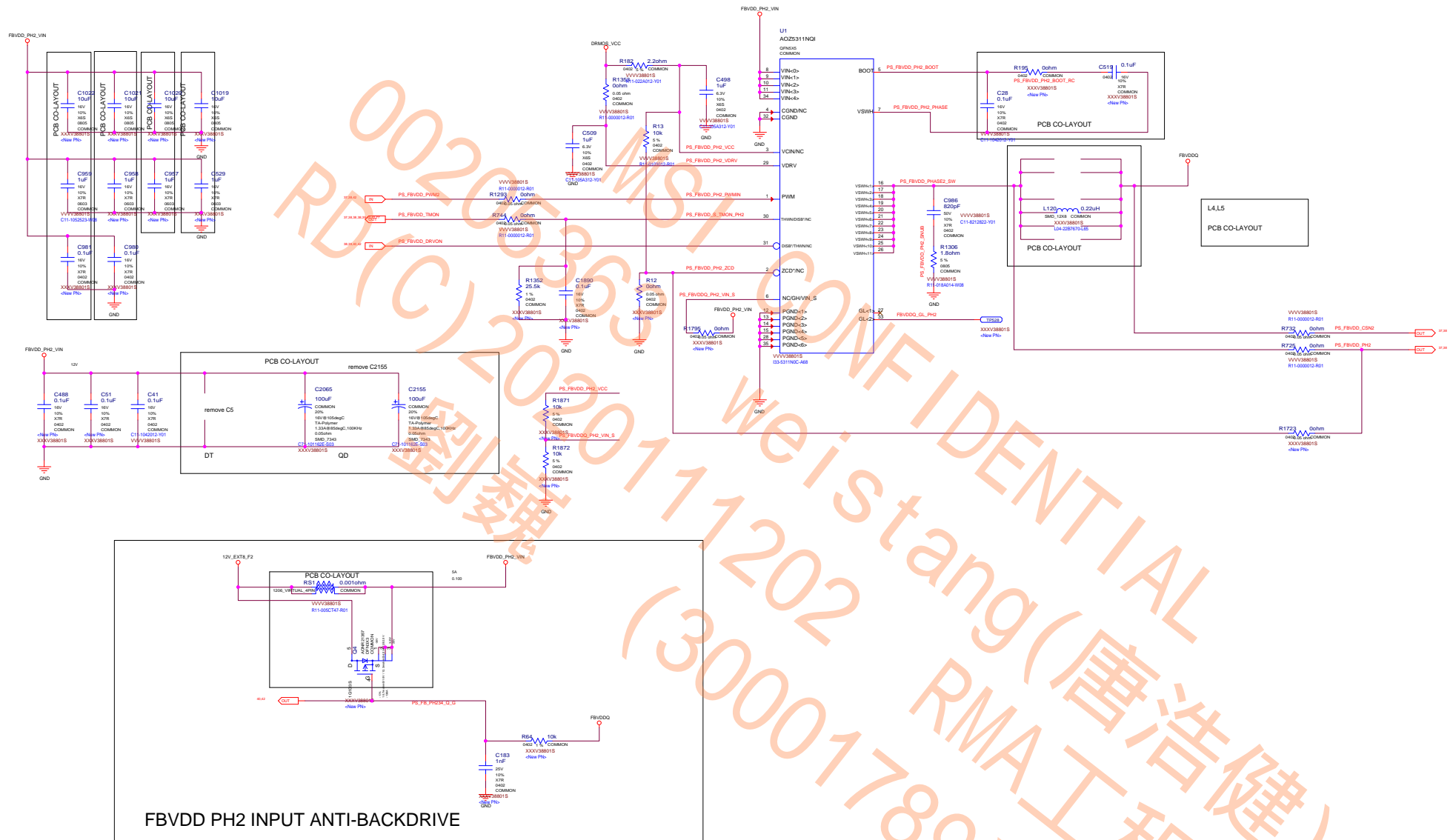
PS: FBVDD PH3



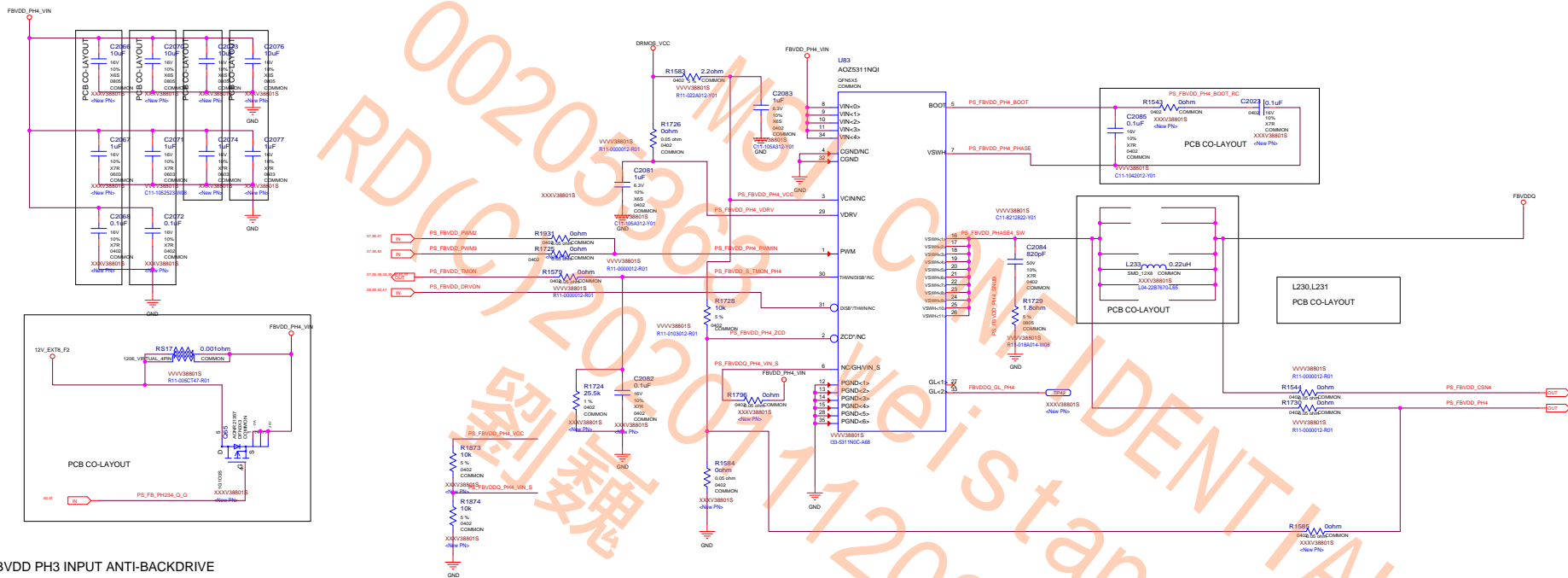
FBVDD PH3 INPUT ANTI-BACKDRIVE



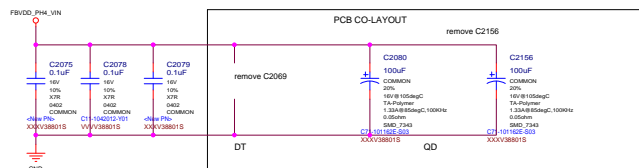
PS: FBVDD PH2



PS: FBVDD PH4

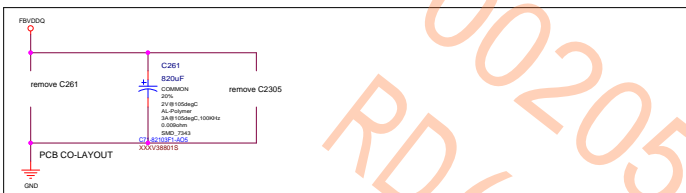


FBVDD PH3 INPUT ANTI-BACKDRIVE

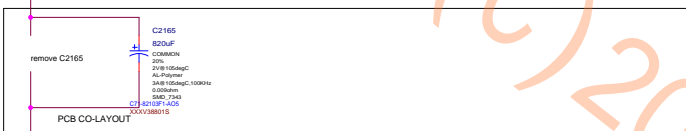


REFER TO PCB FOR BOM STUFFING

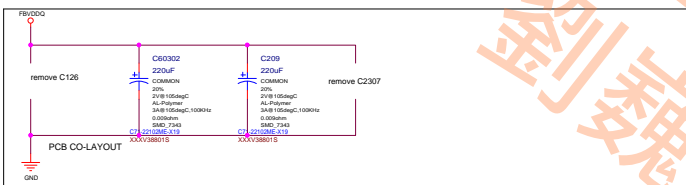
PH1 TOP



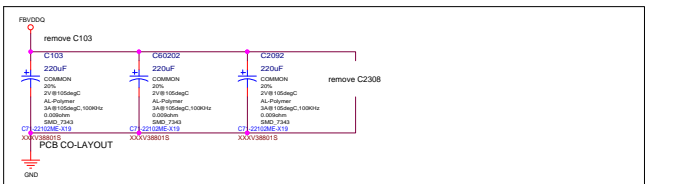
PH3 TOP



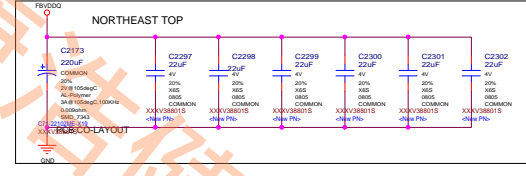
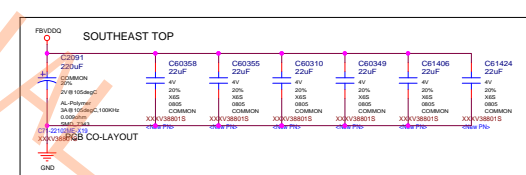
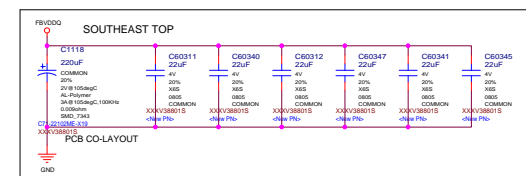
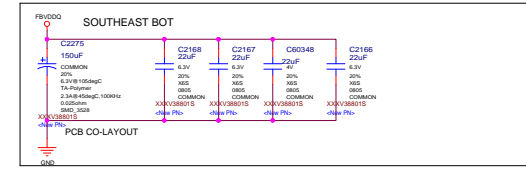
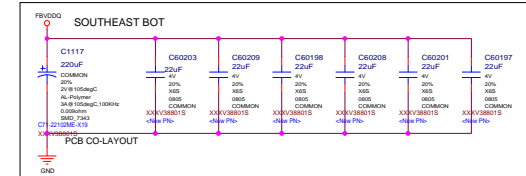
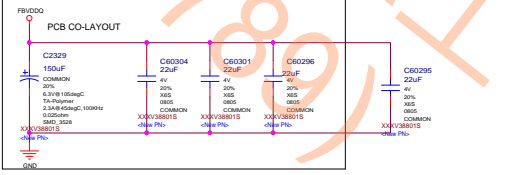
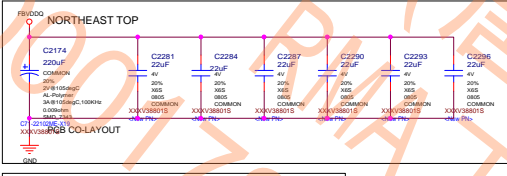
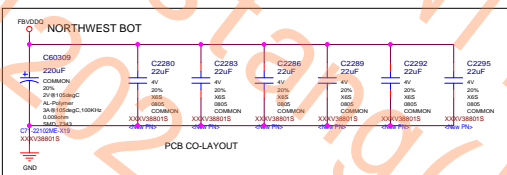
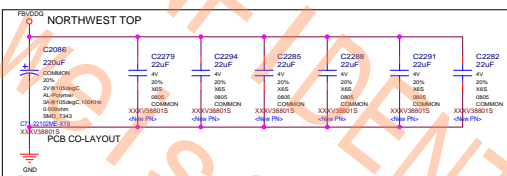
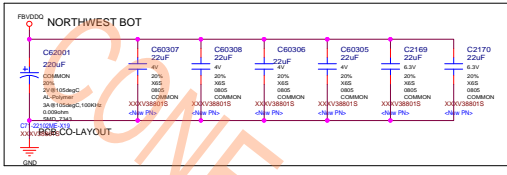
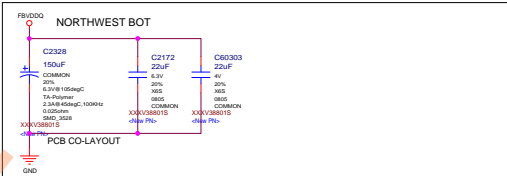
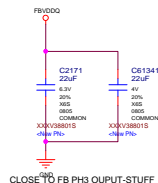
PH2 TOP



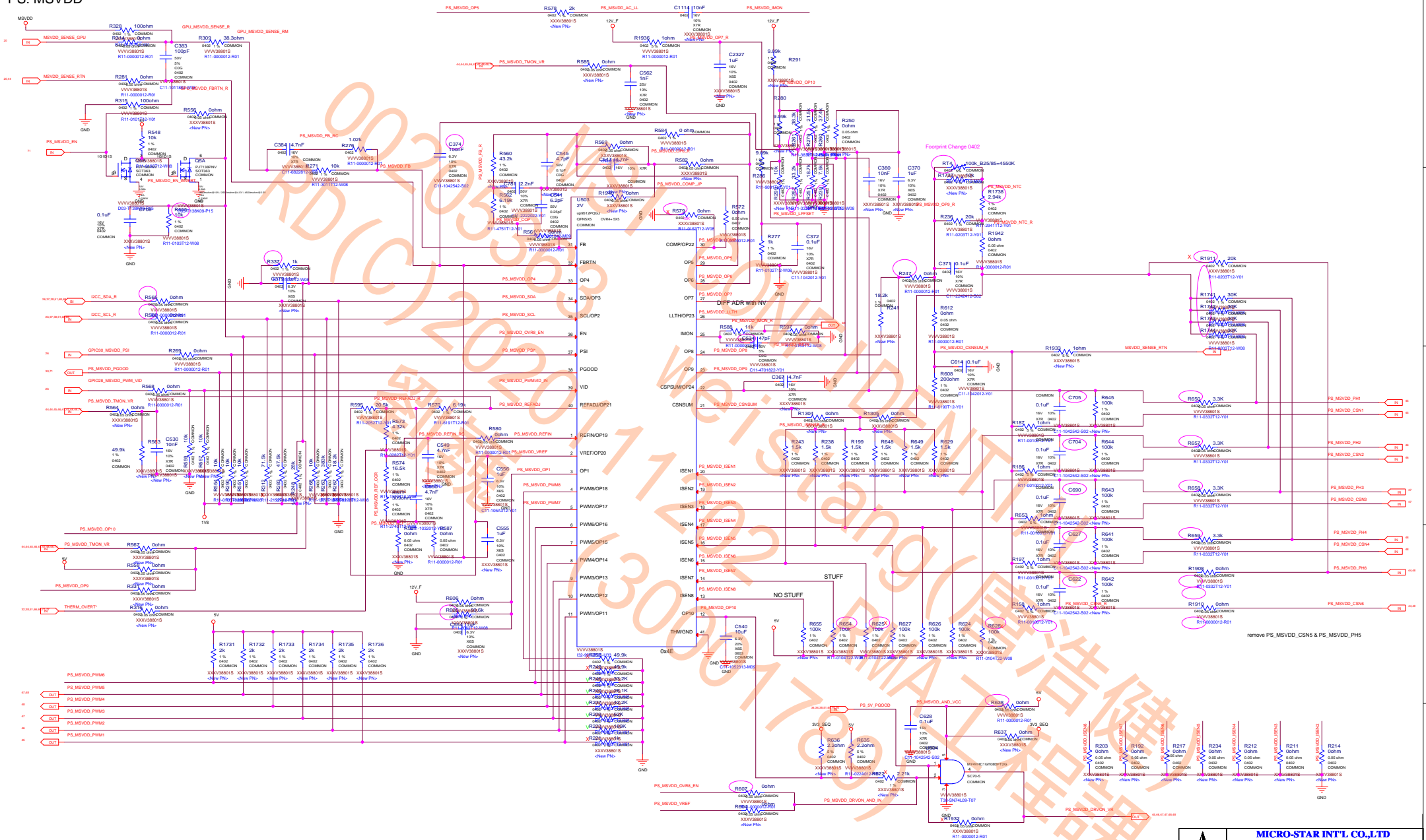
PH4 TOP



PH4 TOP



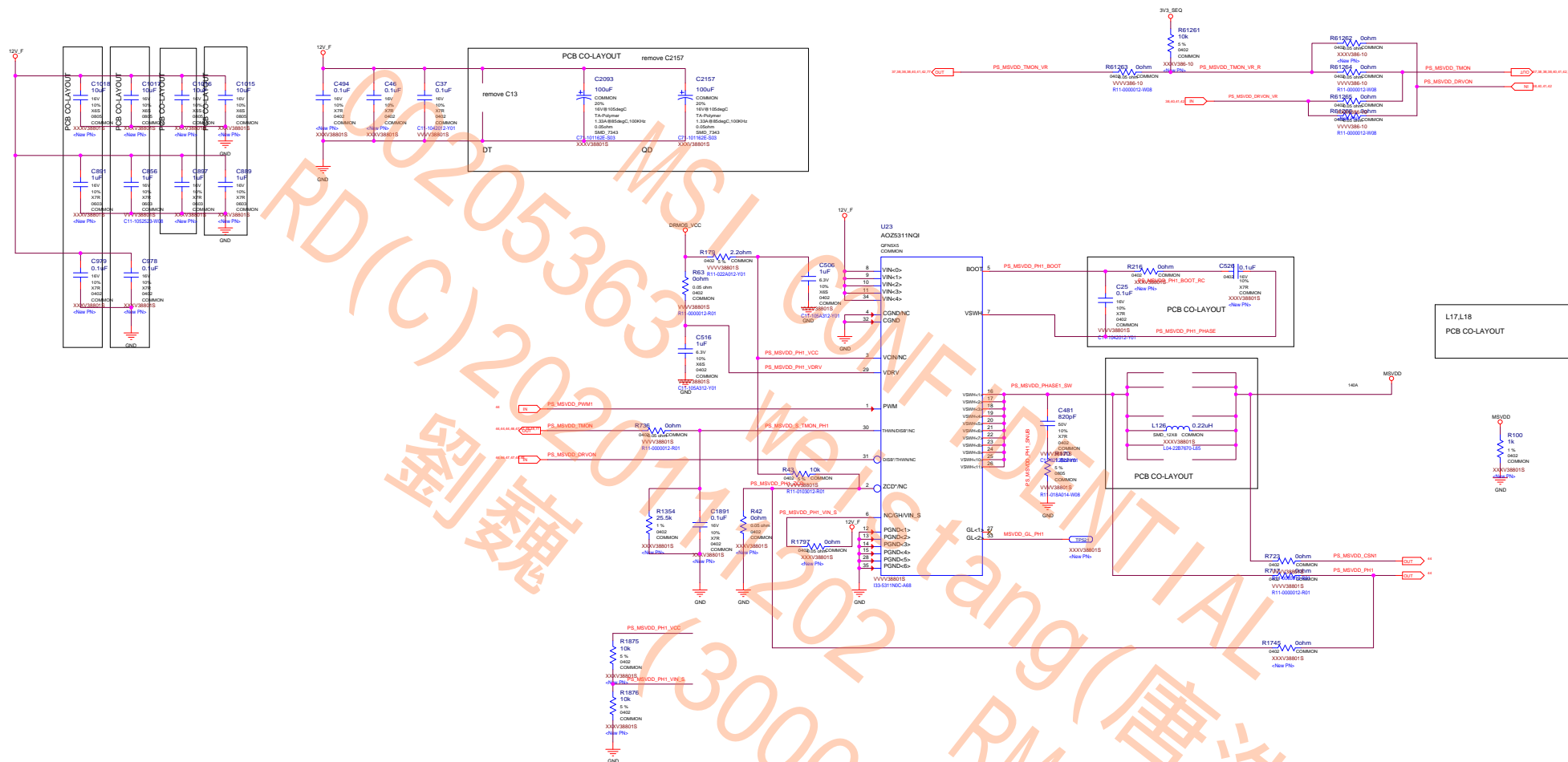
PS: MSVDD



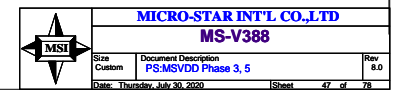
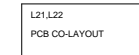
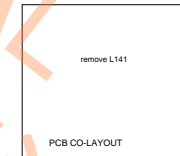
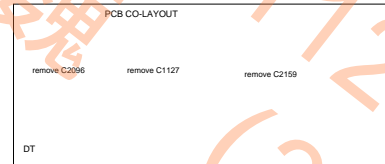
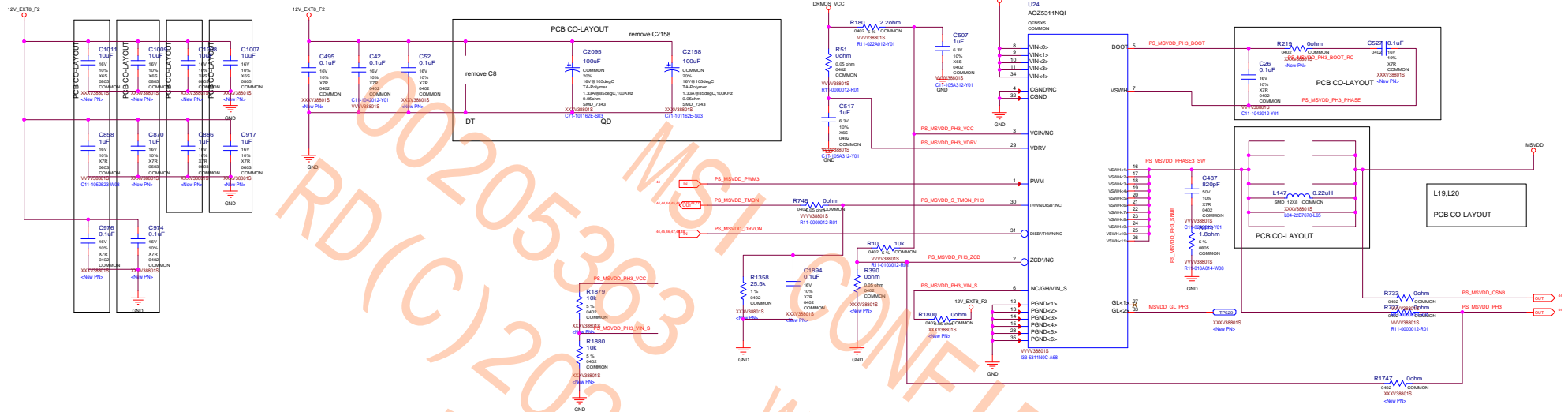
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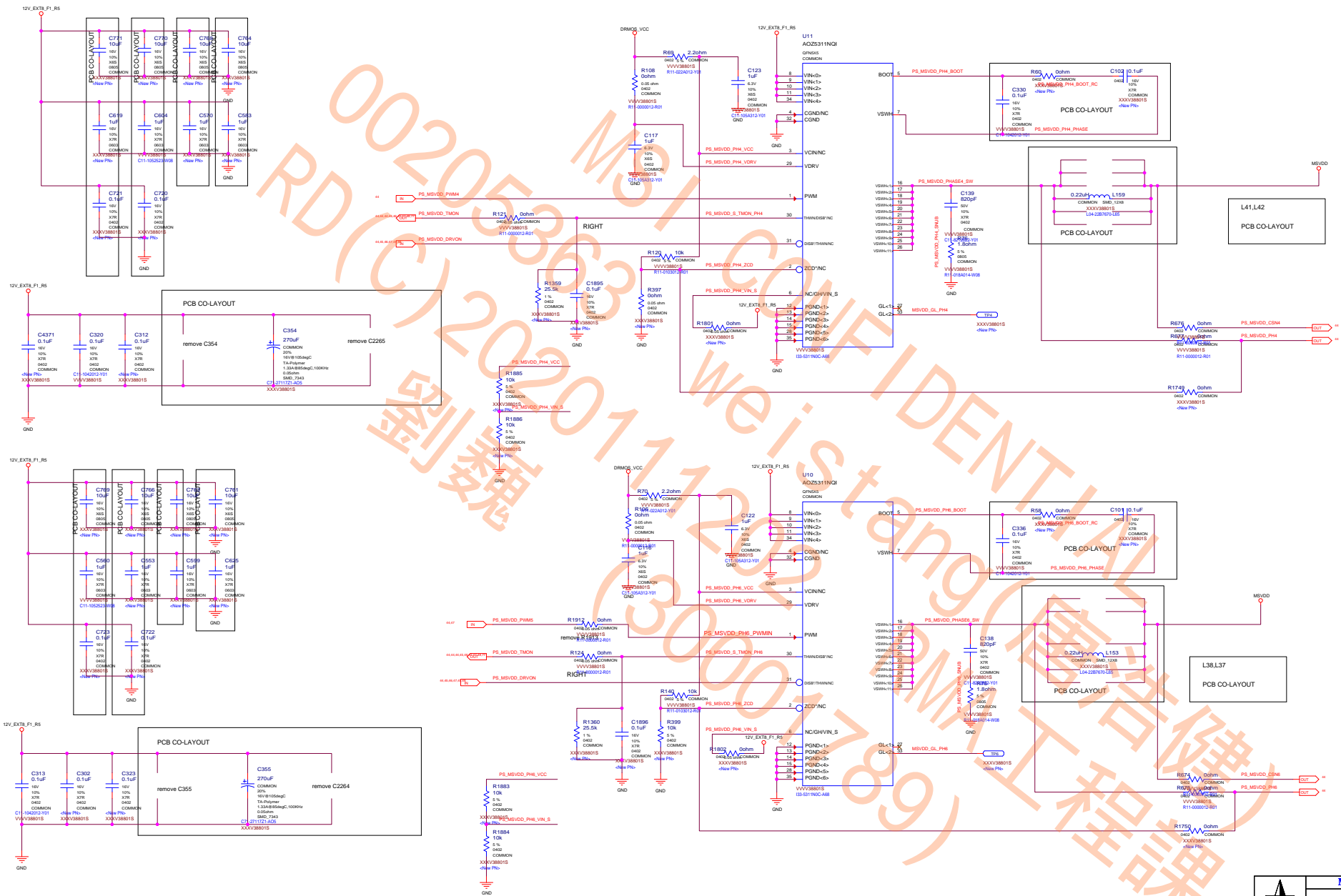
Size Custom	Document Description PS: MSVDD	Rev 8.0
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PS: MSVDD Phase 1



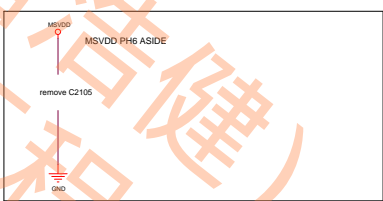
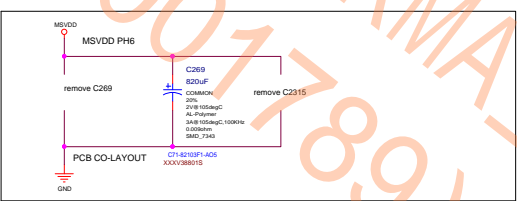
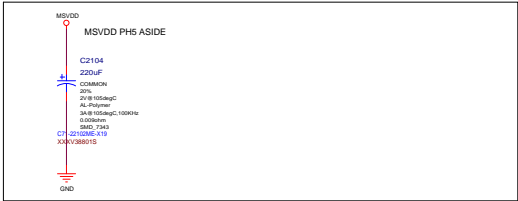
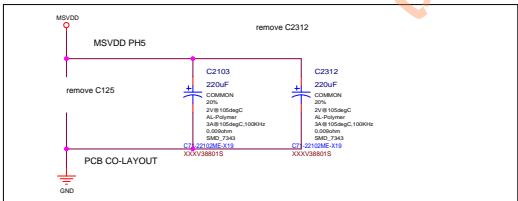
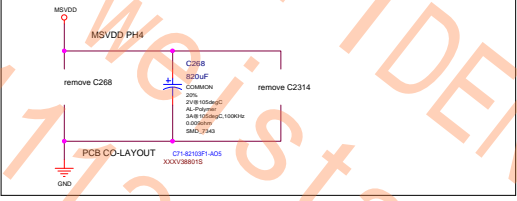
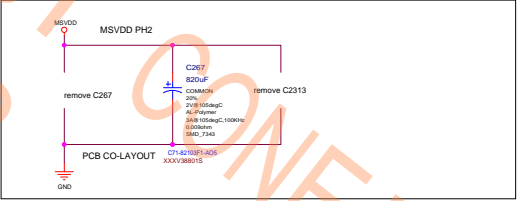
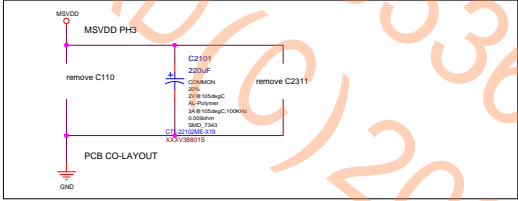
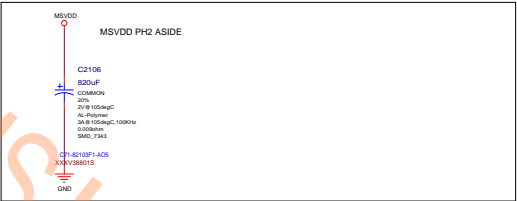
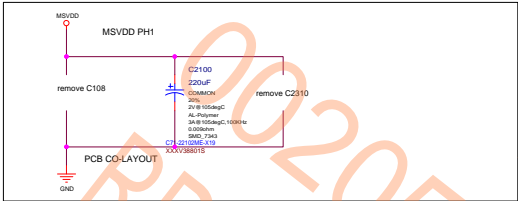
PS:MSVDD Phase 3, 5





PS:MSVDD OUTPUT CAP (TOP)

REFER TO PCB FOR BOM STUFFING



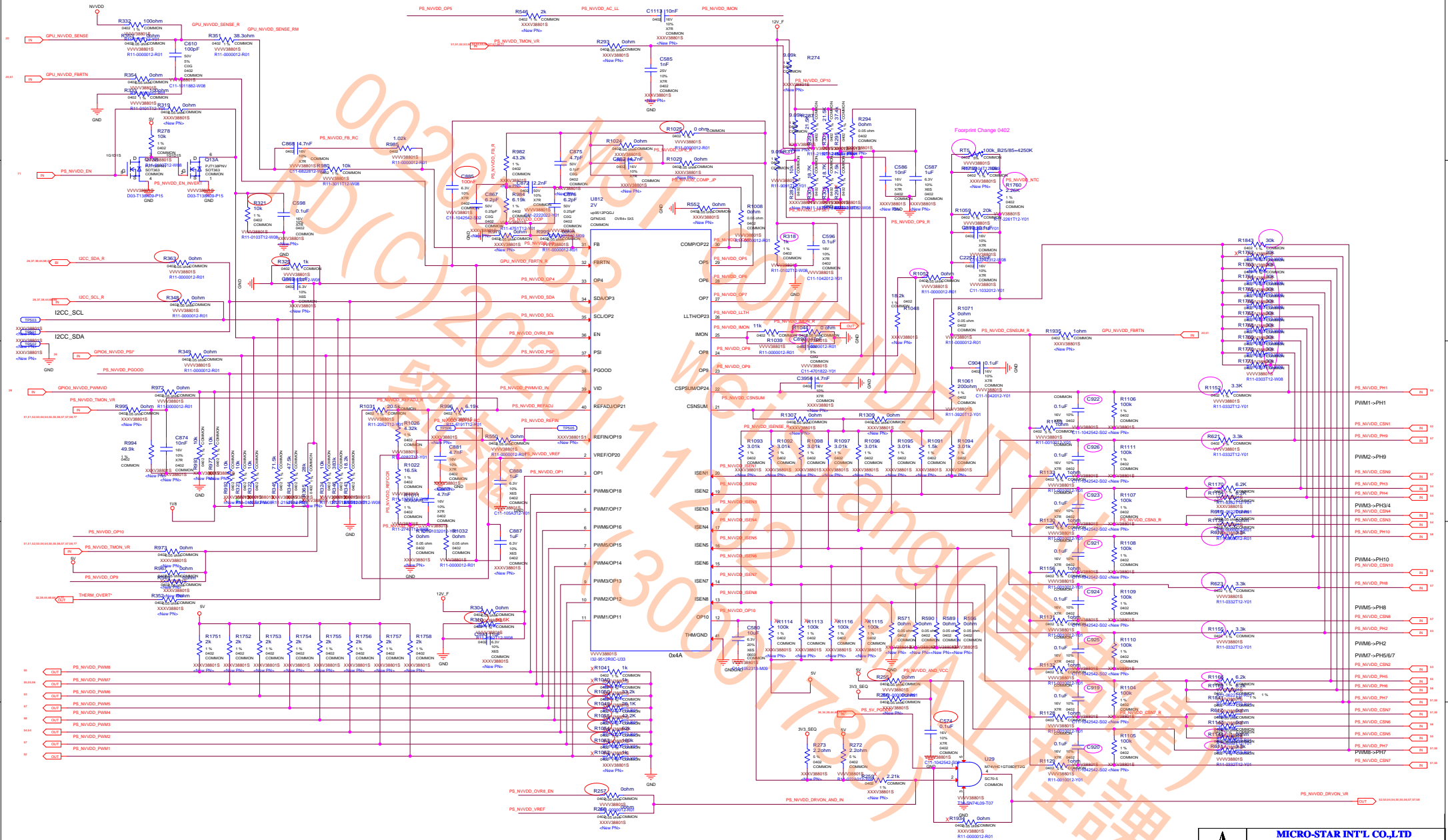
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00205363
RD(C)2020171202
Weistang (唐浩健)
(30001789)
RMA工程課

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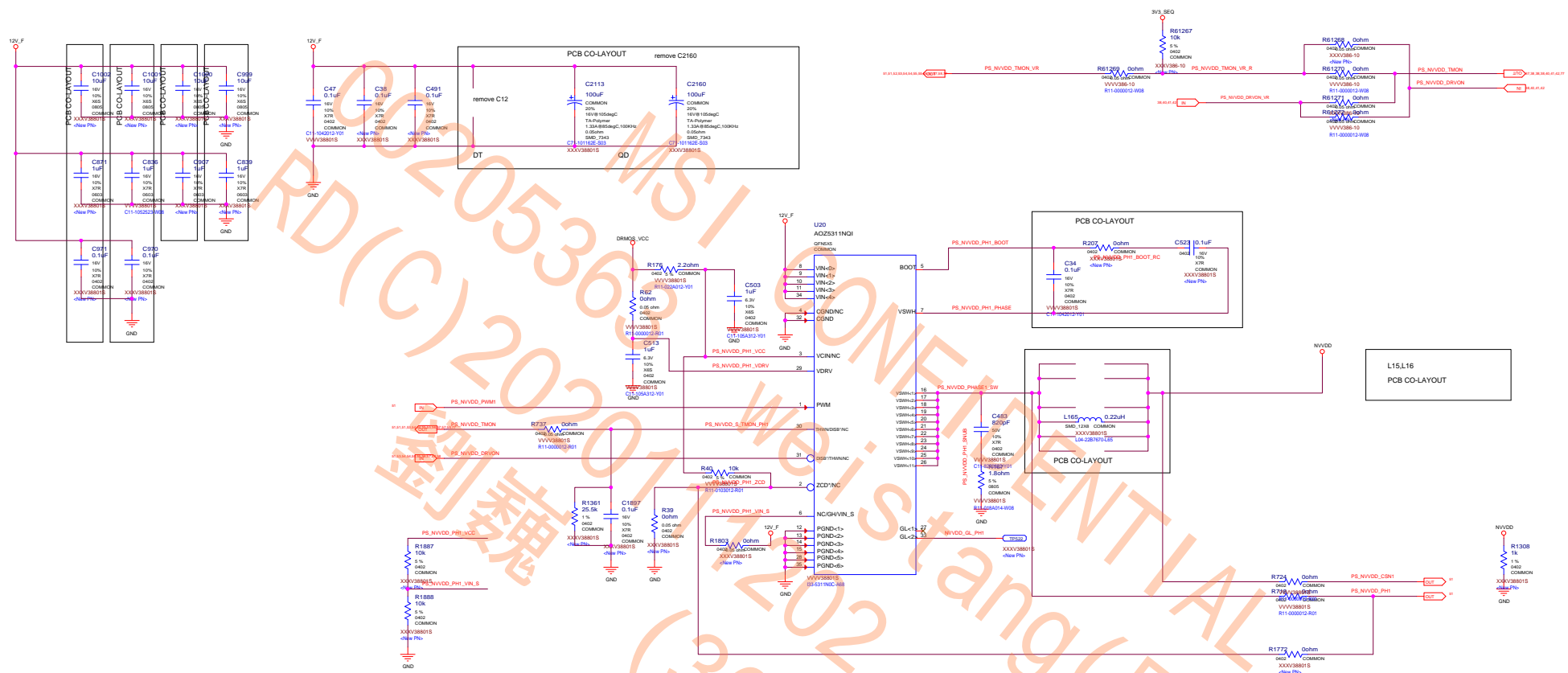
PS: NVVDD Controller_OVR8



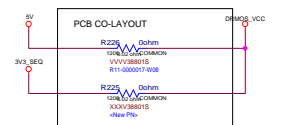
MICRO-STAR INT'L CO.,LTD
MS-V388

Size Custom	Document Description PS: NVDD Controller_OVR8	Rev 8.0
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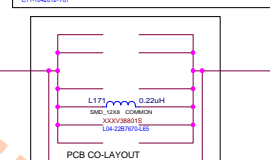
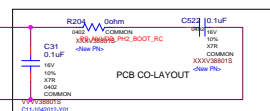
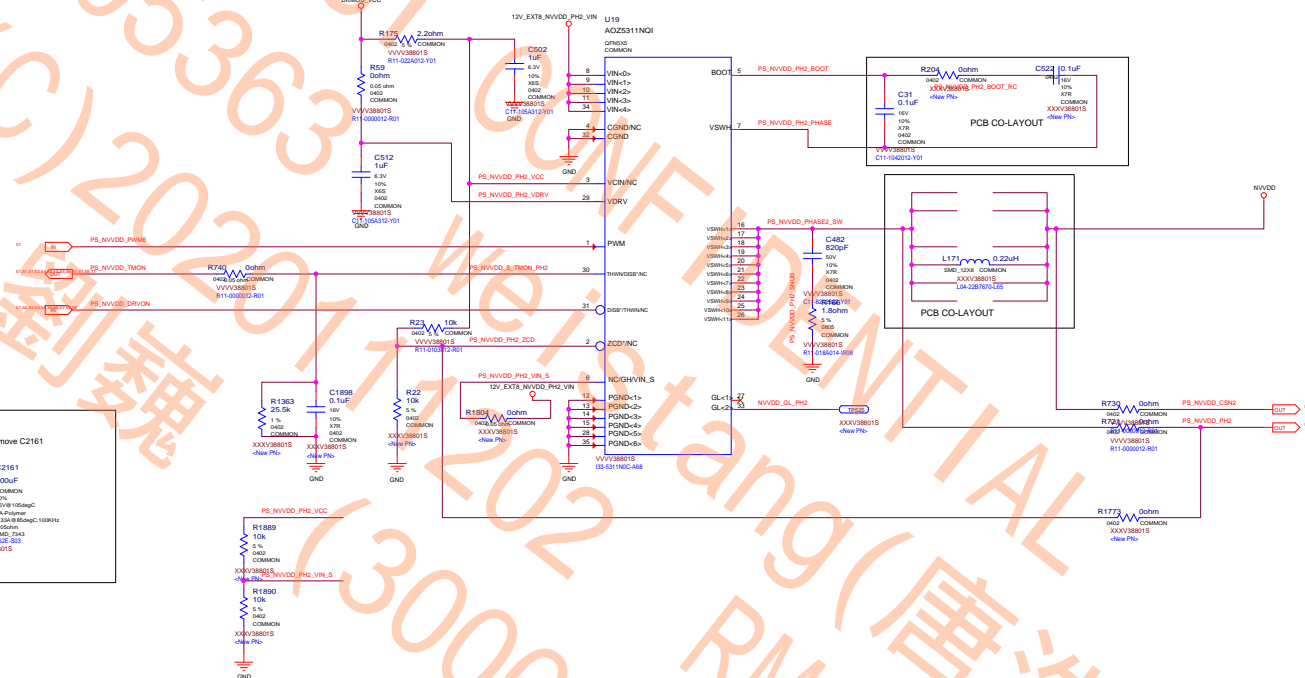
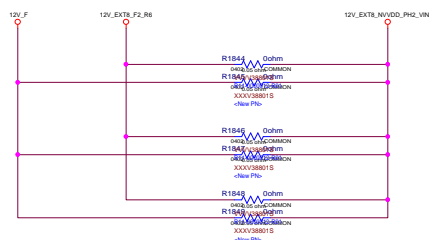
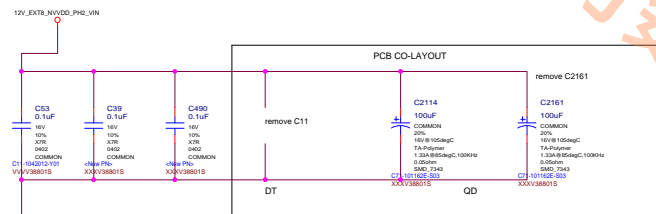
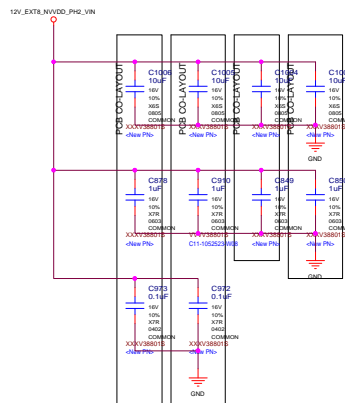
PS: NVVDD Phase 1



PS: NVVDD Phase 2 (PWM6)



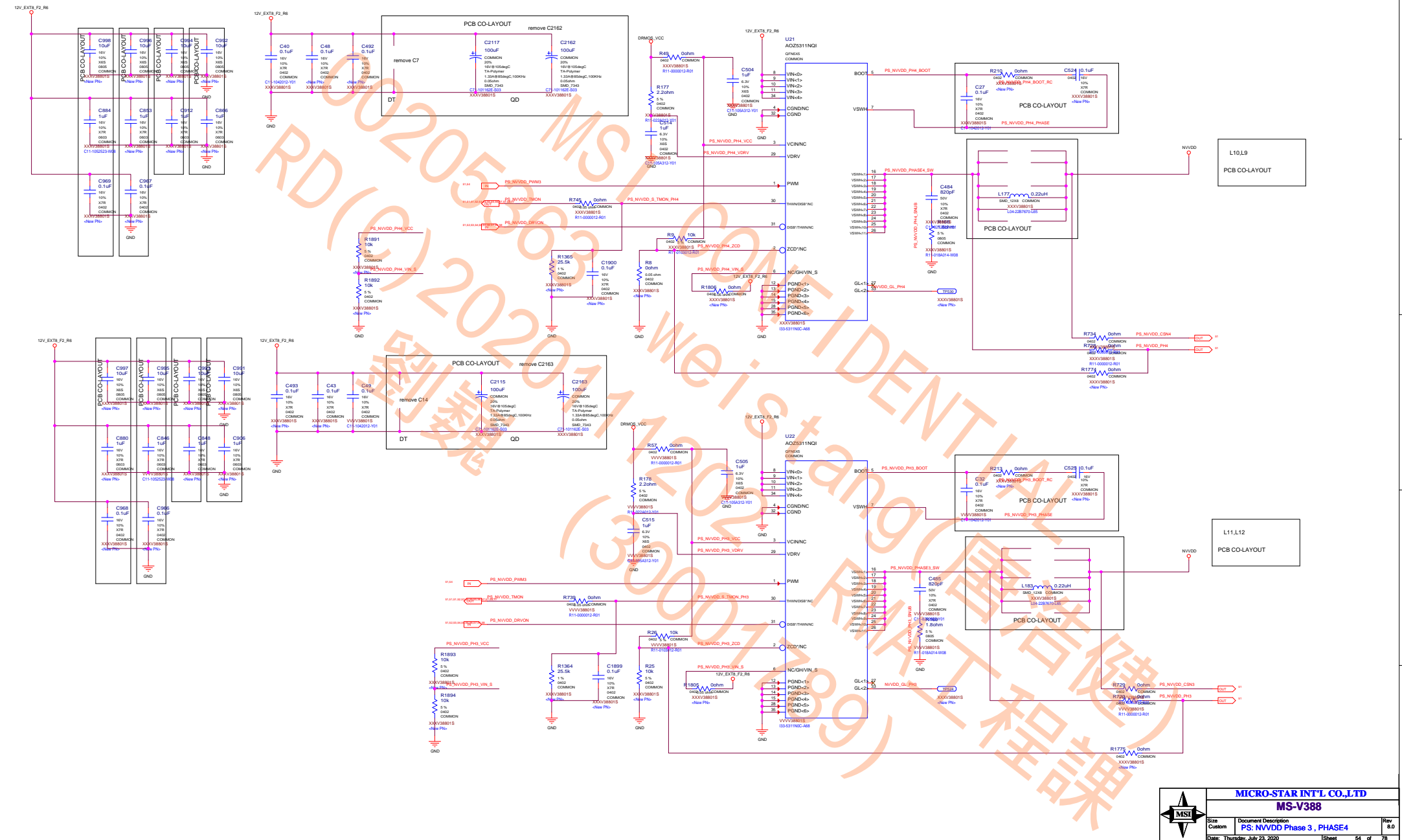
MPS DRMOS WITH 3V3 SUPPLY



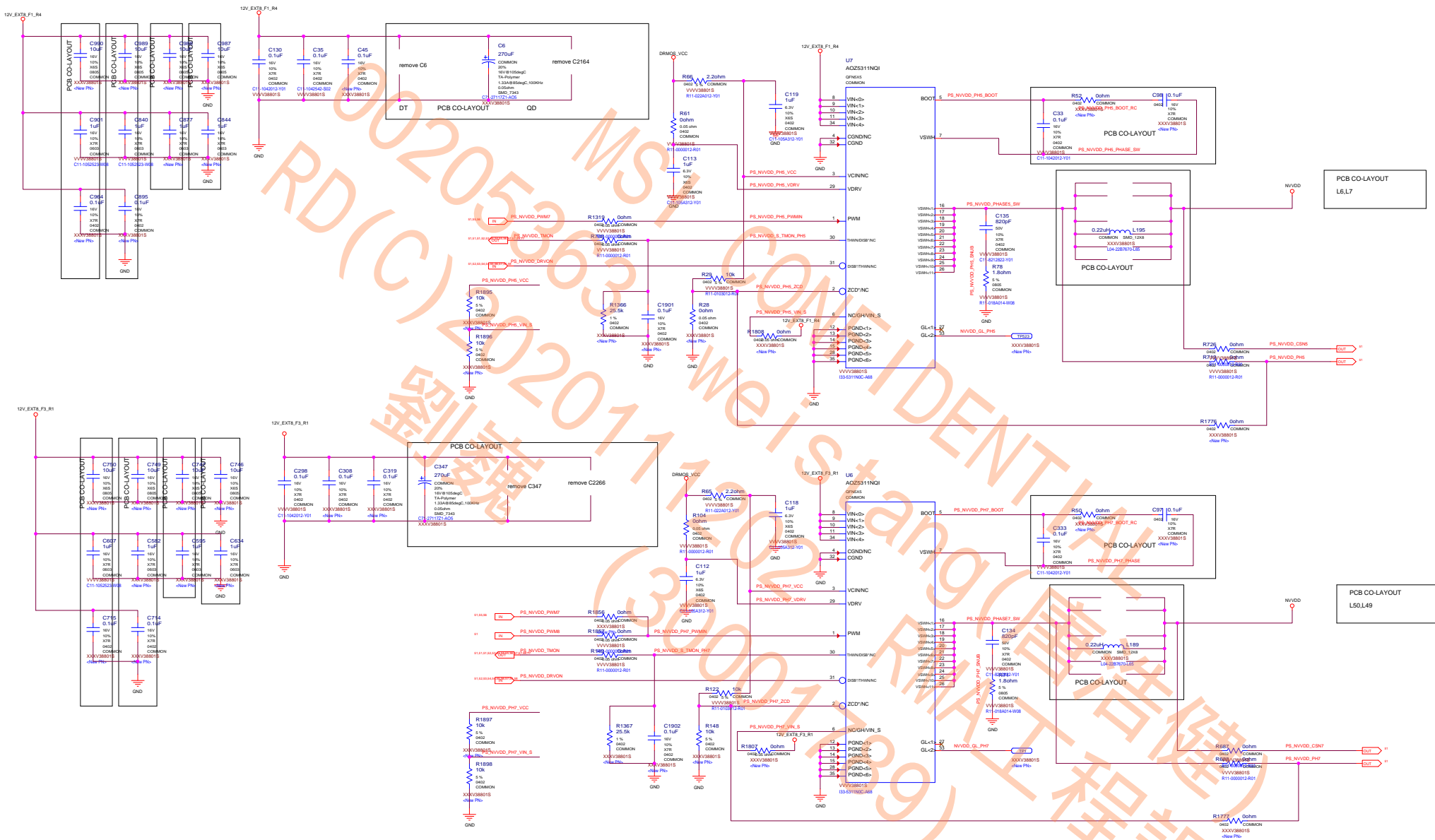
L13,L14

PCB CO-LAYOUT

PS: NVVDD Phase 3 (PWM3), PHASE4 (PWM3)



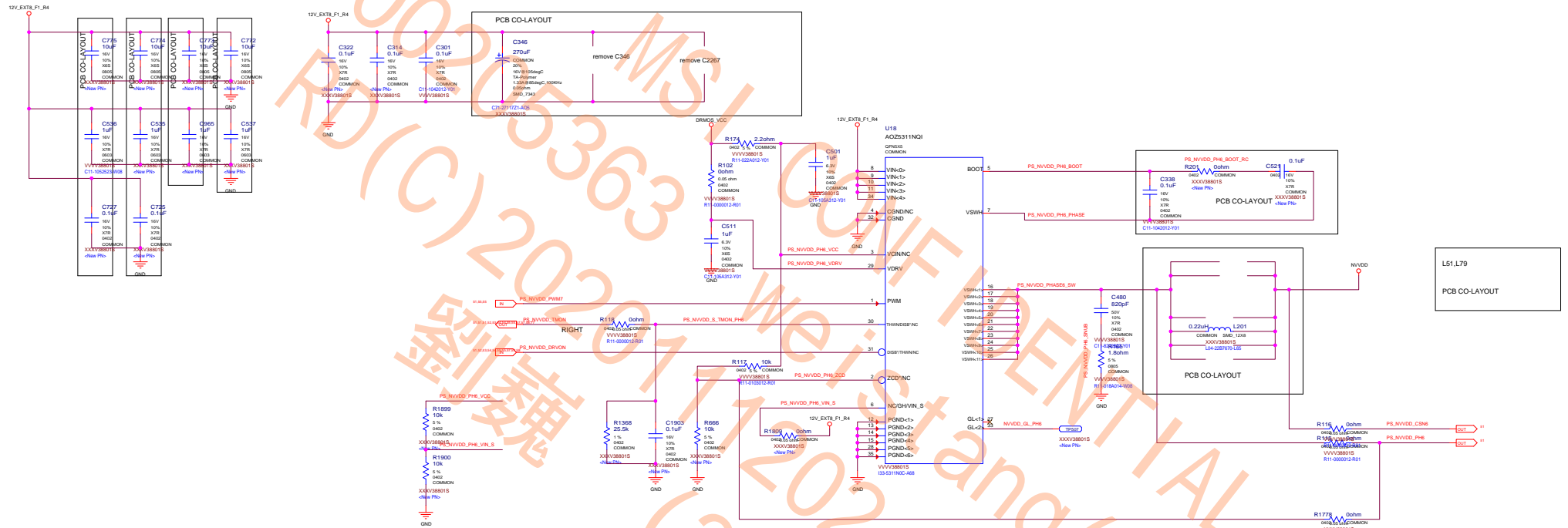
PS: NVVDD PH 5(PWM4), PH7(PWM8/4)



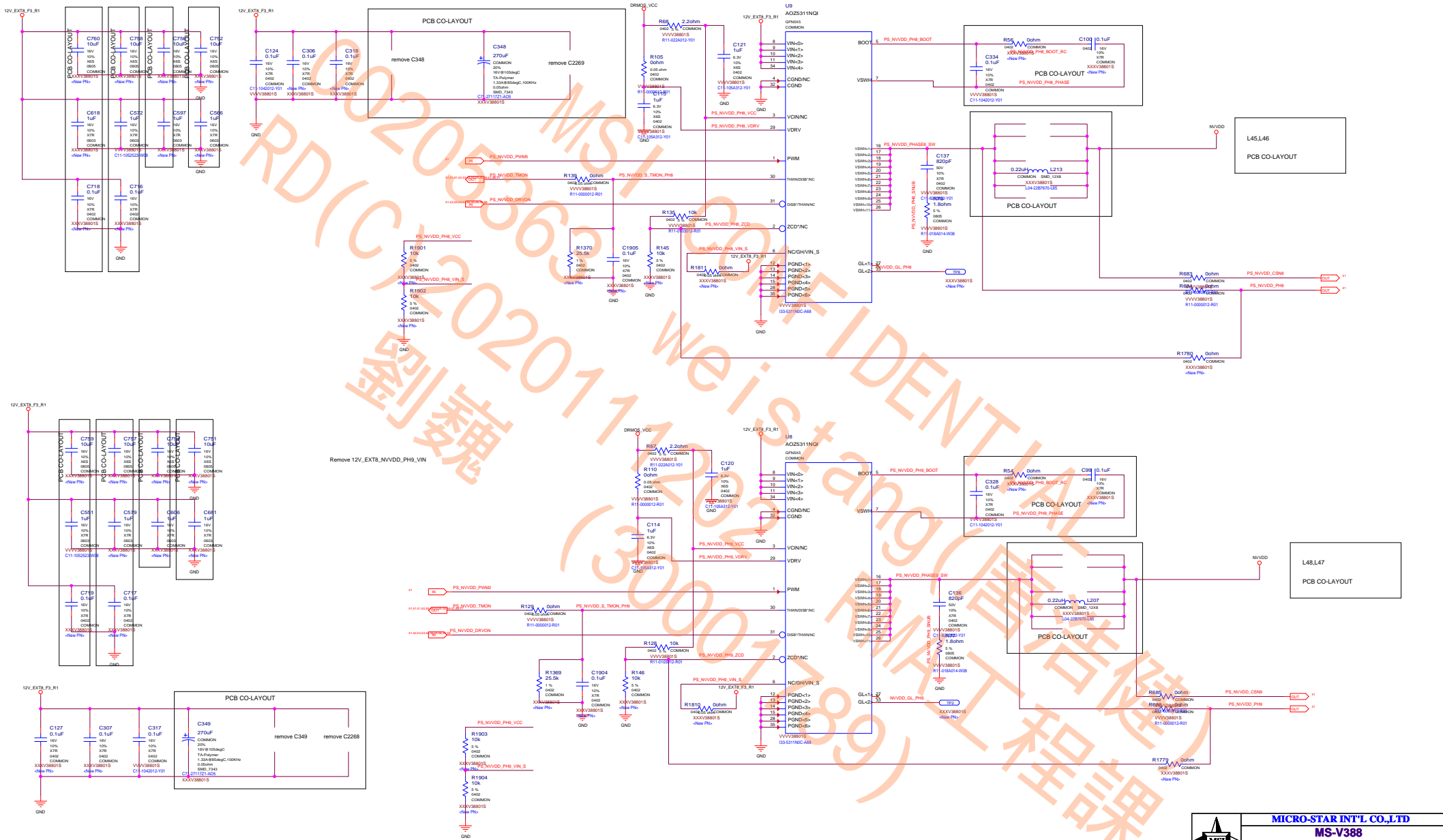
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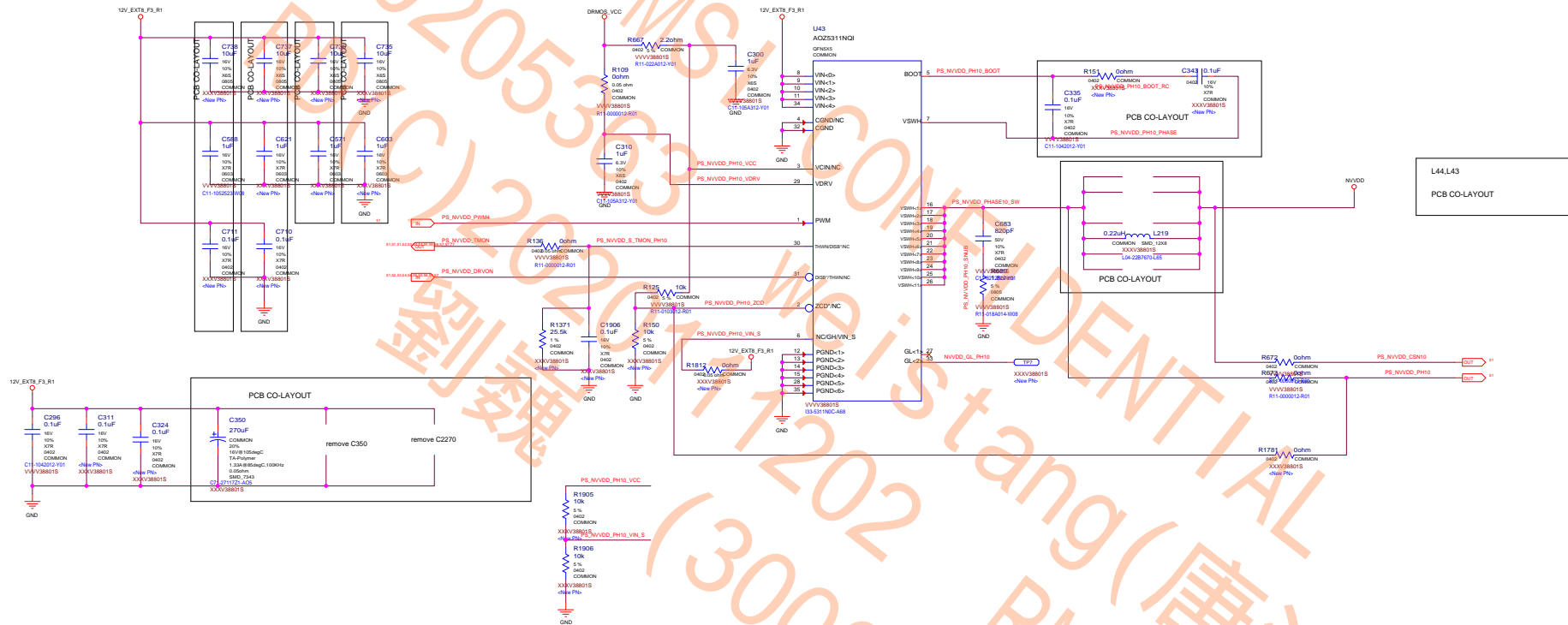
Size Custom	Document Description PS: NVDD PH 5, PH7	Rev 8.0
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PS: NVVDD Phase 6(PWM4)




PS: NVVDD PH 8 (PWM5), PH 9(PWM2)





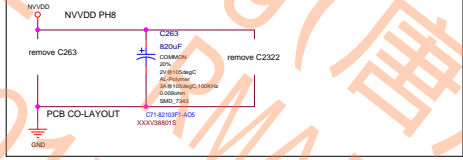
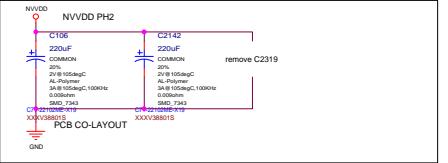
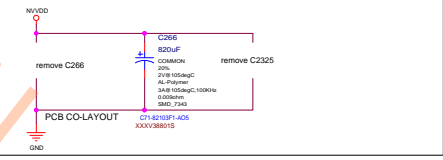
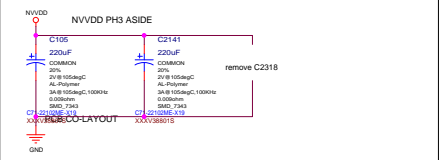
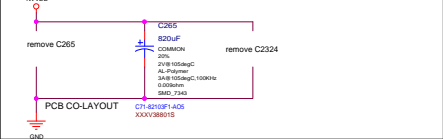
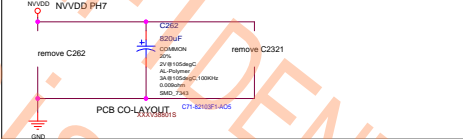
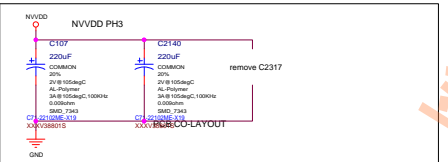
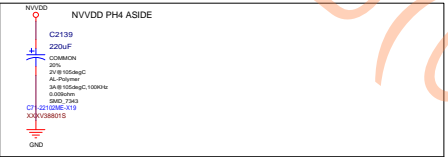
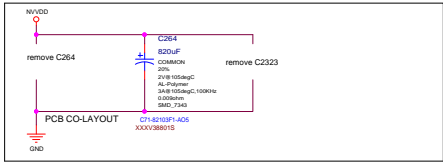
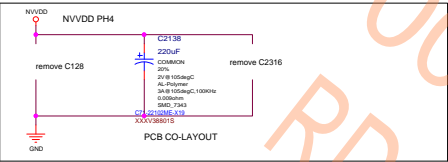
MSI CONFIDENTIAL
00205363
RD(C)202011202
劉魏
weistang(唐浩健)
(30001789)
RMA工程課

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REFER TO PCB FOR BOM STUFFING



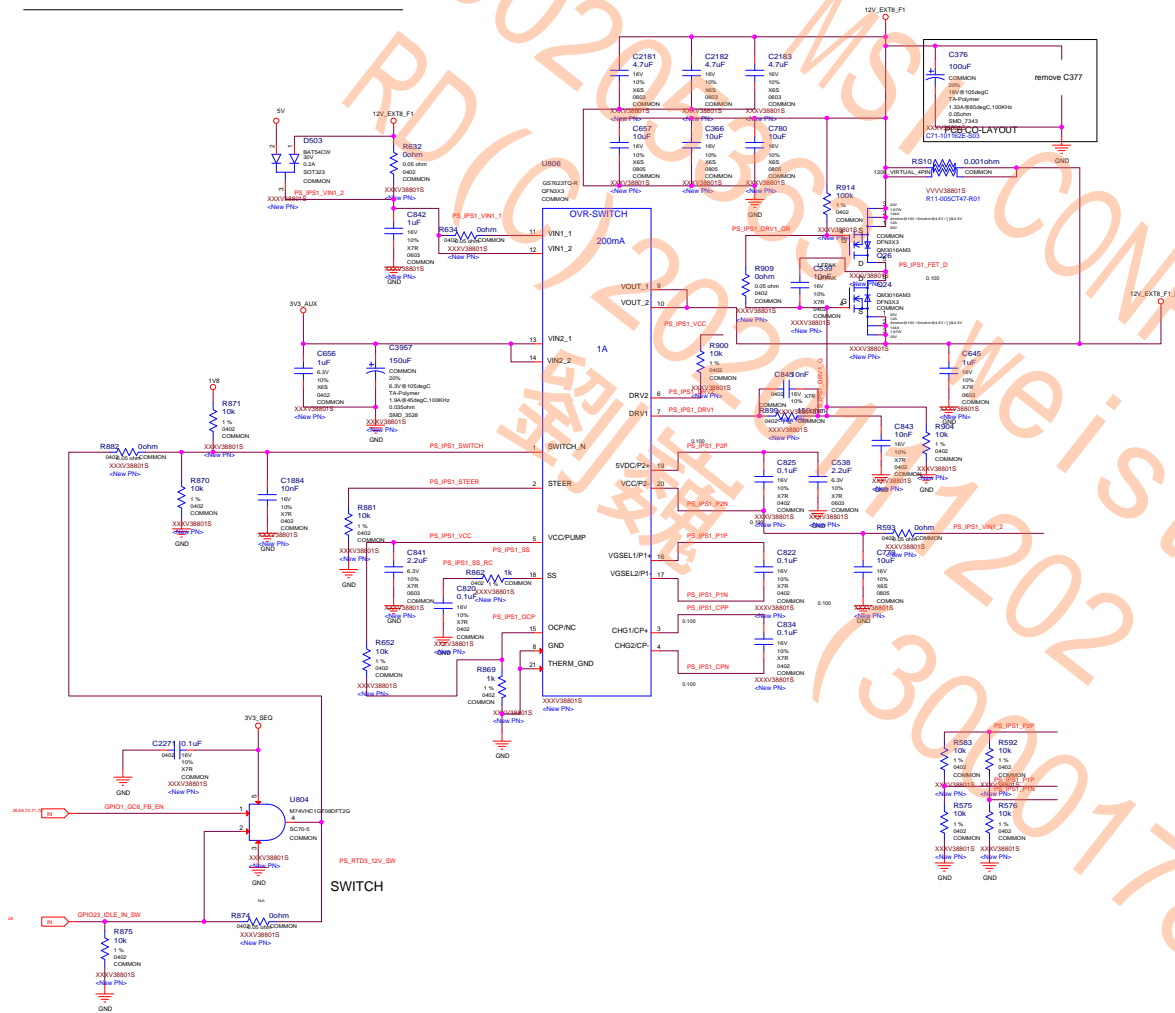
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PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPI01	GPI023	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

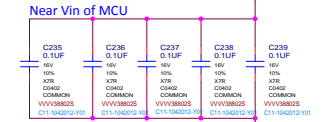


LED_A

LED_B

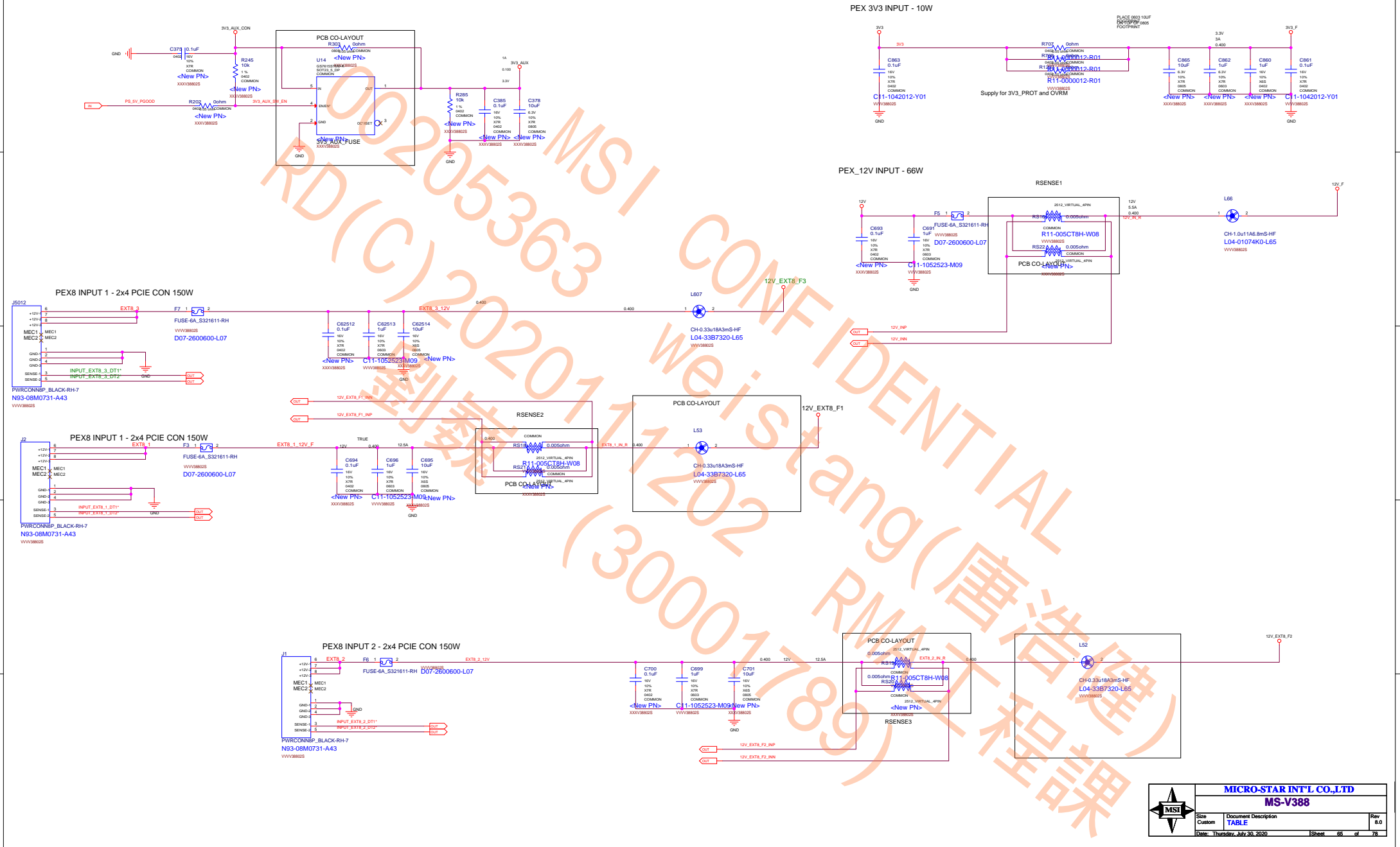
LED_C

LED_D

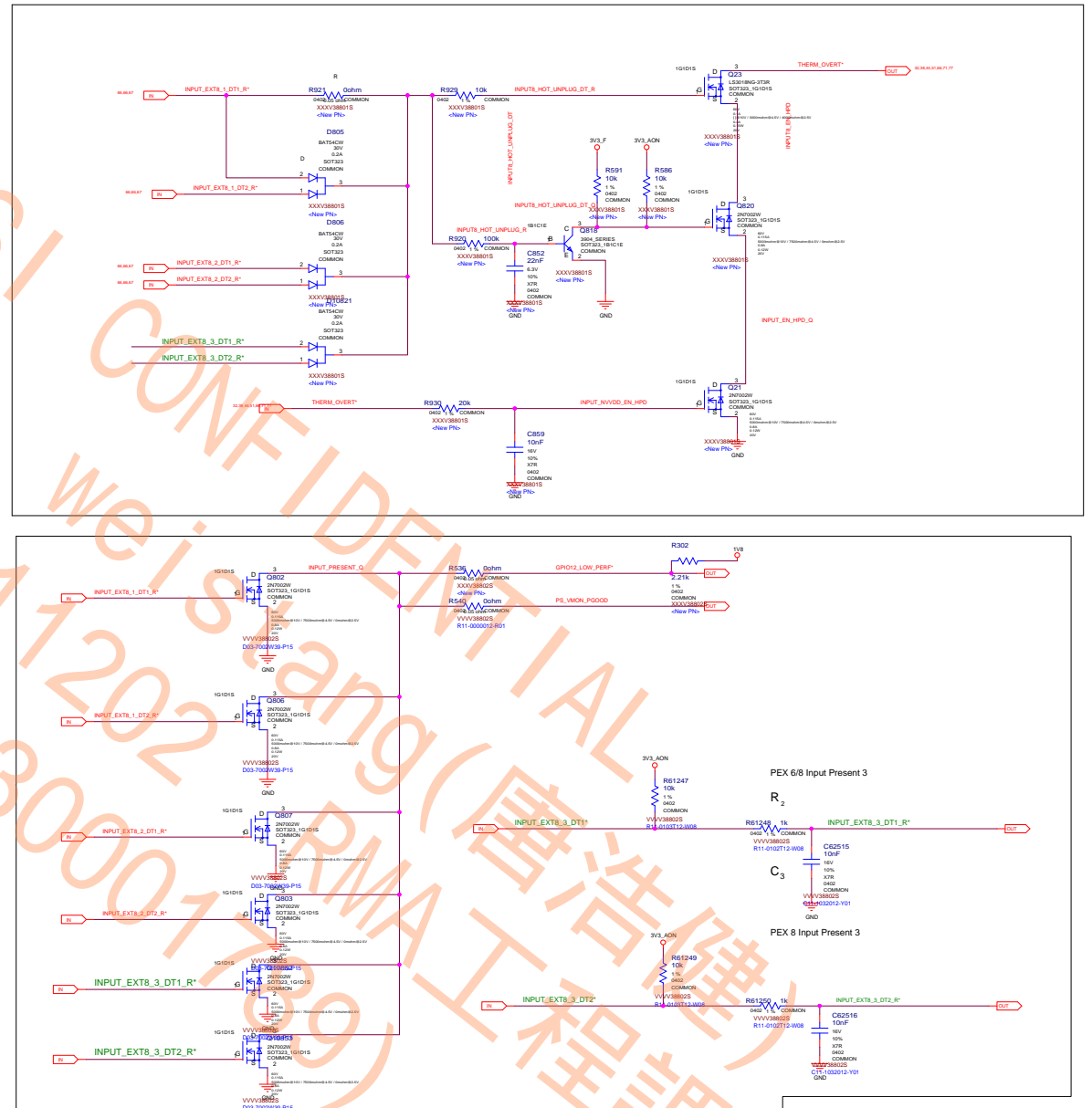
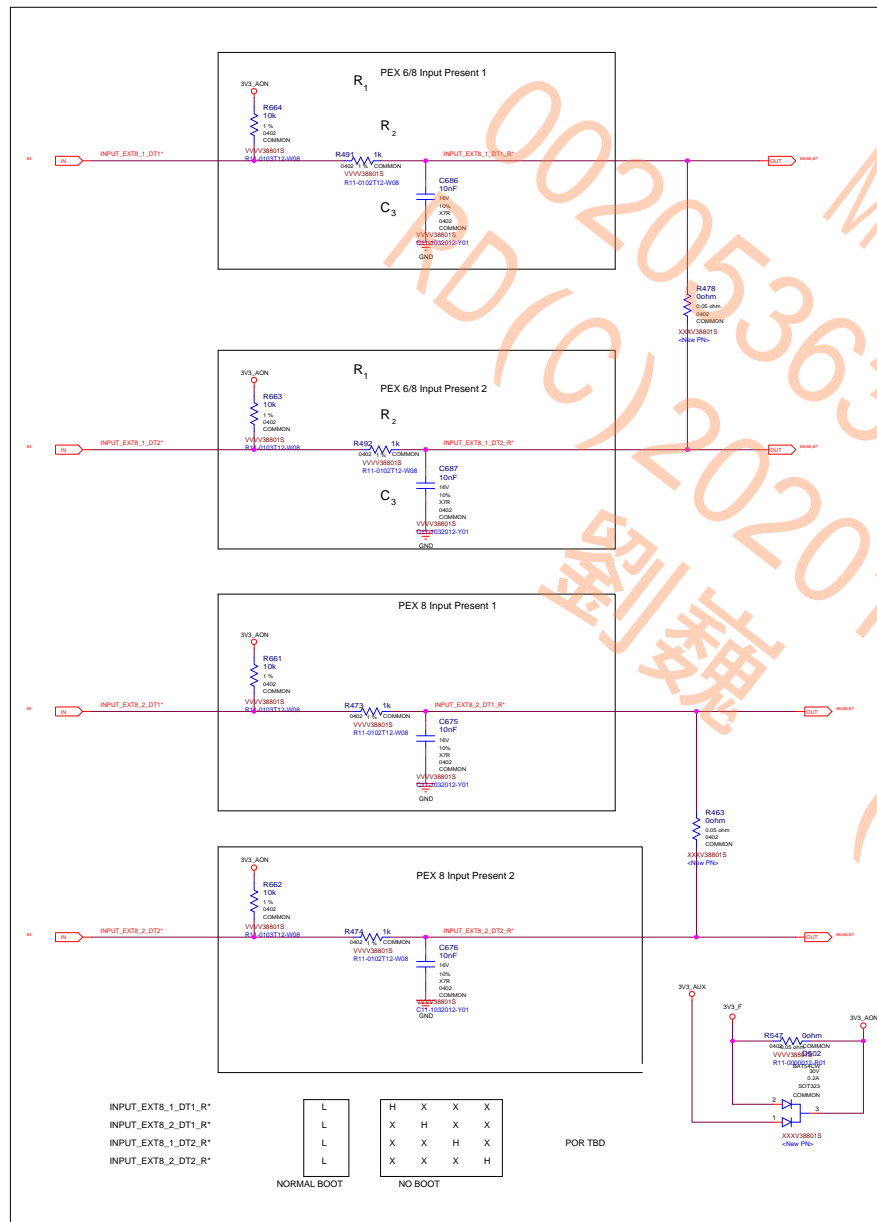


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Custom	TABLE	8.0	
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PS: Inputs, Filtering, and Monitoring



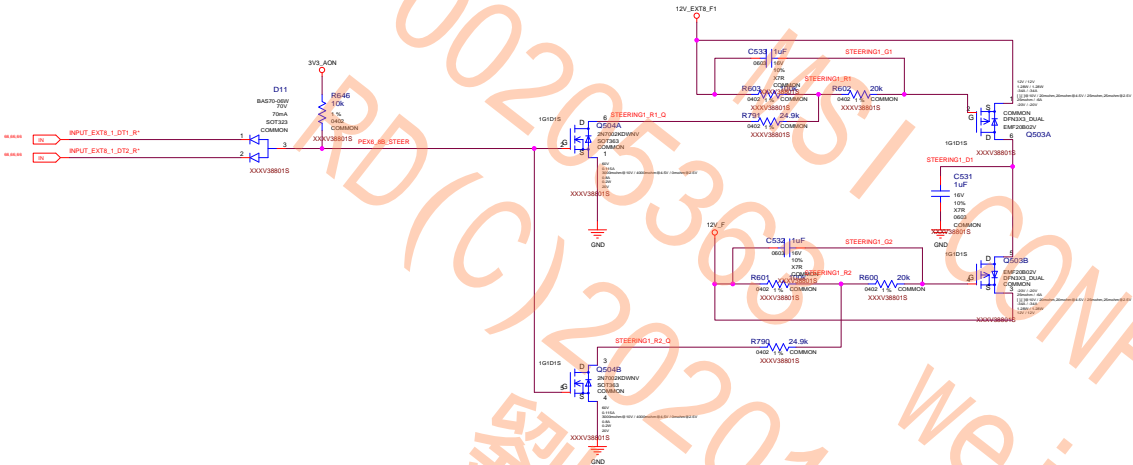
PS: 12V Current Steering & Hot Unplug Detect



PS: Discrete Steering

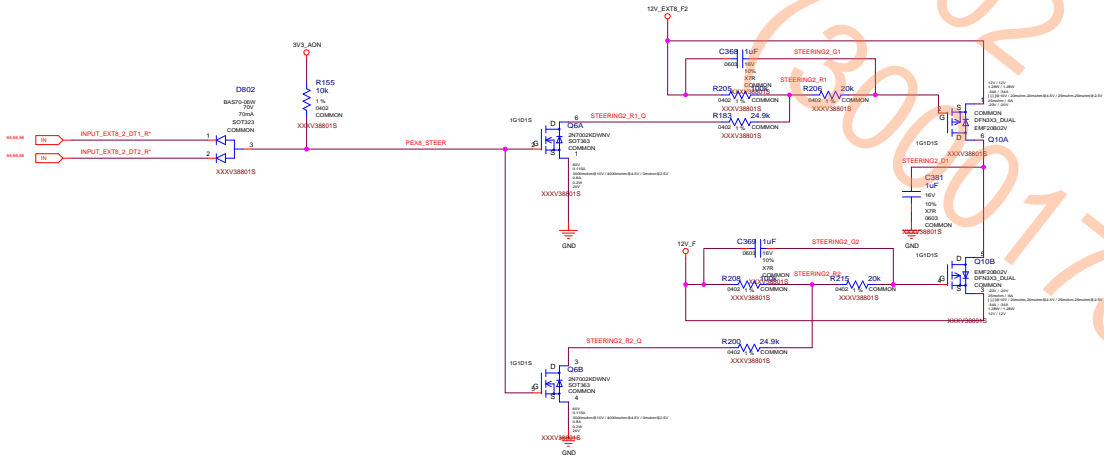
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1



NO STUFF BY DEFAULT REF ONLY

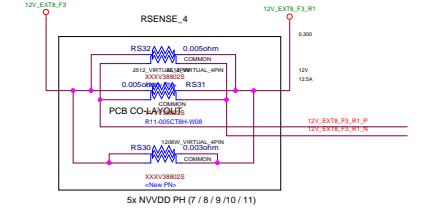
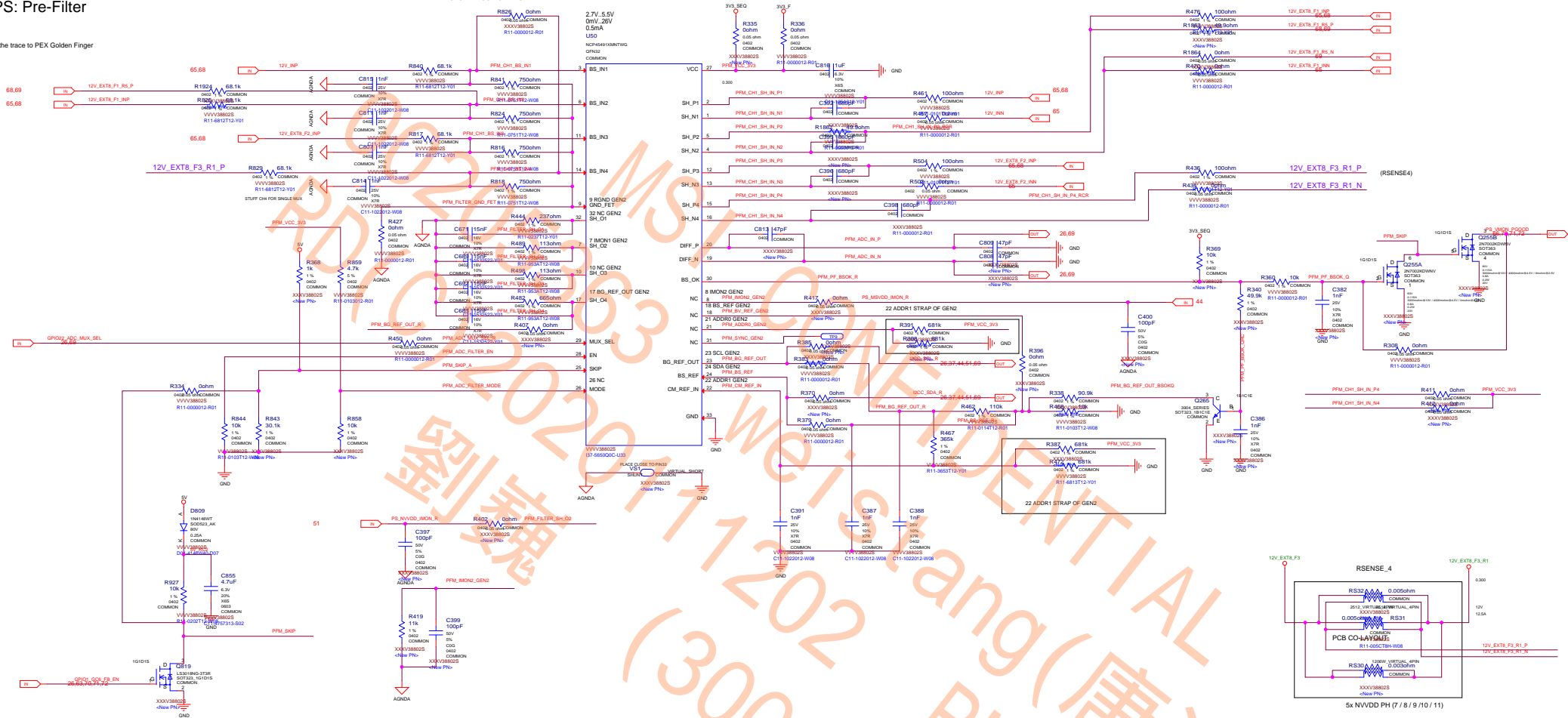
PEX12V AND 12V_EXT8_F2



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PS: Pre-Filter

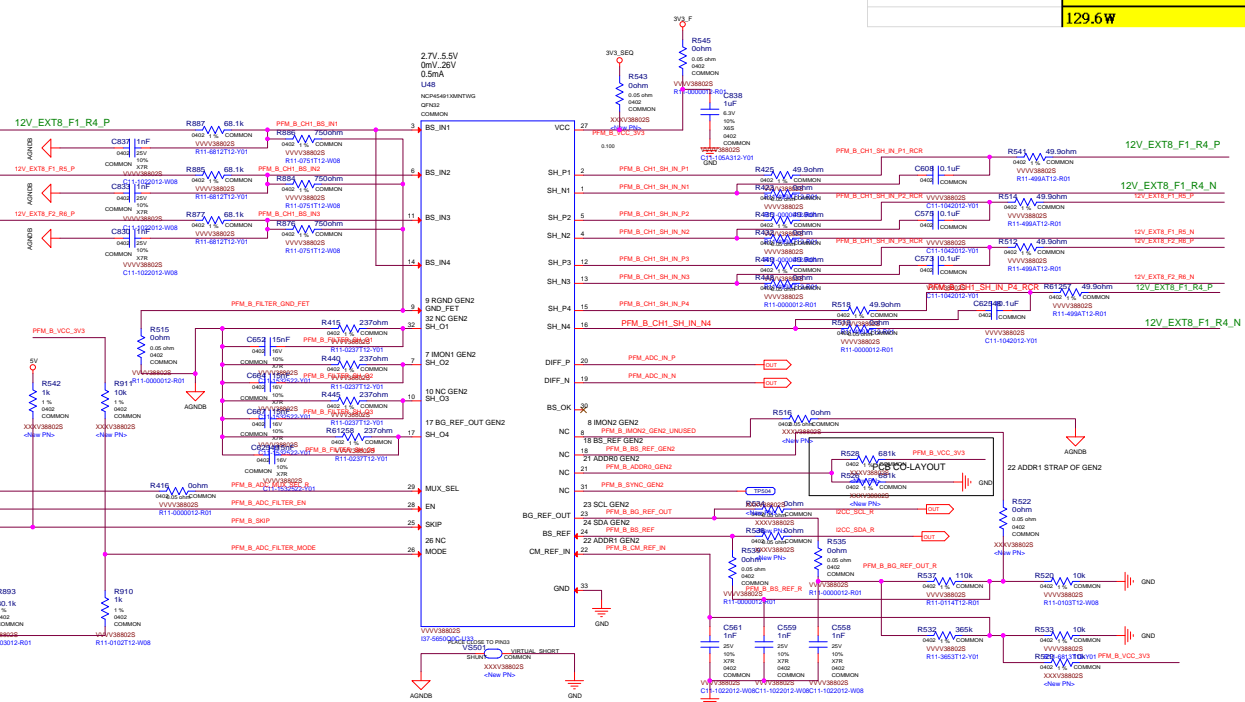
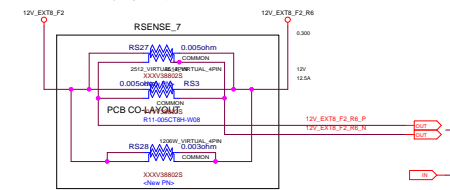
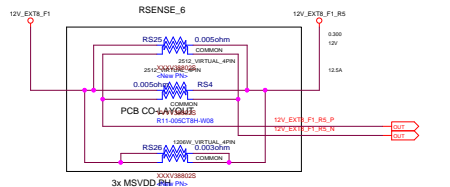
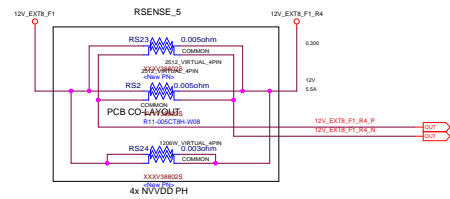
Route the trace to PEX Golden Finger



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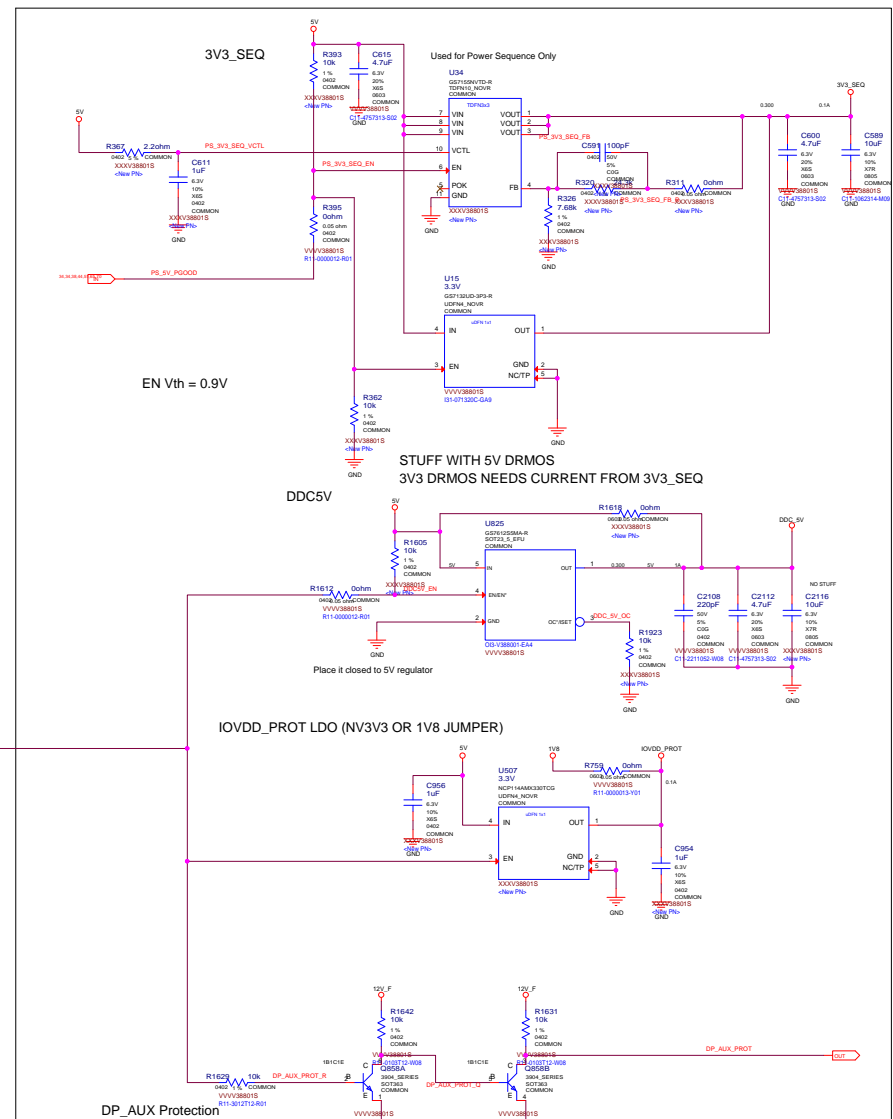
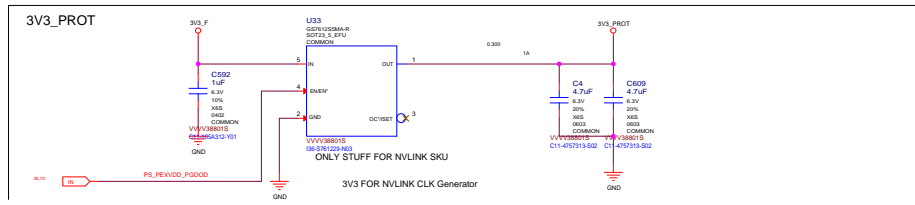
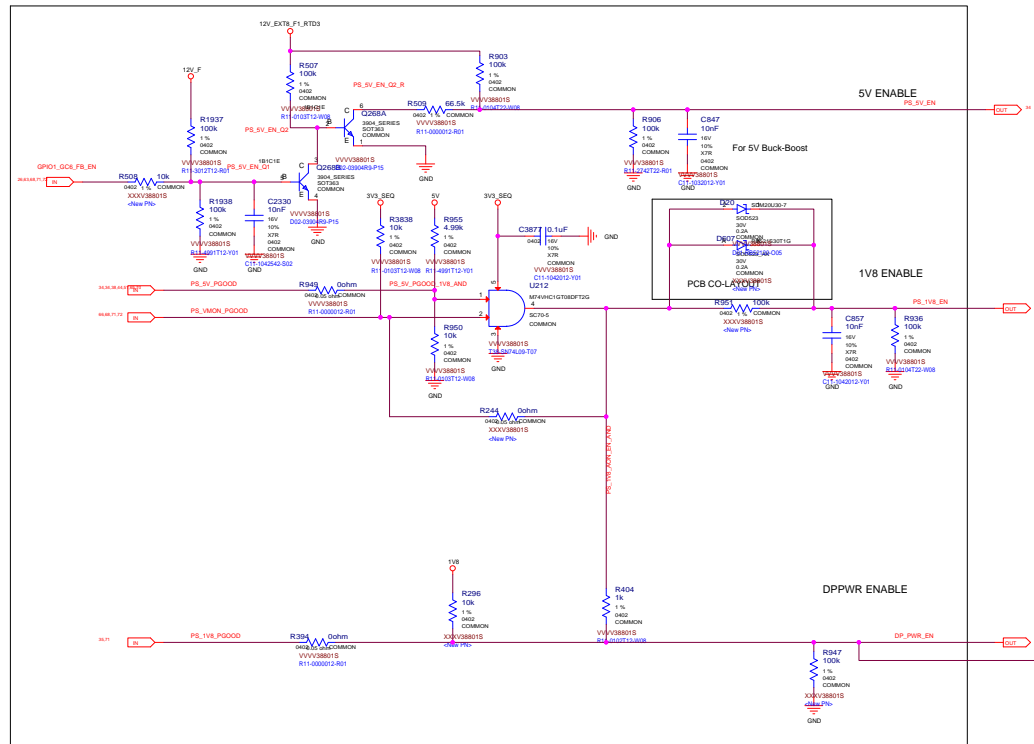
PS: Pre-Filter B



BUS	connect A	connect B	connect C
(RSENSE1)	(RSENSE2)	(RSENSE3)	(RSENSE4)
12V_F	NET NAME: F1	NET NAME: F2	NET NAME: 12V_EXT8_F3_R1
FB 4	PEXVDD	FB-2(左)	
MSVDD1		FB-3	
NVVD1	(RSENSE2)	MSVDD3(左)	NVVD7
	NET NAME:12V_EXT8_F1_R1	MSVDD5(左)	NVVD8
	FB 1	(RSENSE7)	NVVD9
	5V	NET NAME: 12V_EXT8_F2_R6	NVVD10
	1V8	NVVD2(左)	NVVD11
	(RSENSE6)	NVVD3(左)	
	NET NAME:12V_EXT8_F1_R5	NVVD4(左)	
	MSVDD2		
	MSVDD4		
52.8W	MSVDD6	73.5+27+30=130.5W	122.5W
	(RSENSE5)		
	NET NAME: 12V_EXT8_F1_R4		
	NVVD5-F1-R4		
	NVVD6-F1-R4		
	129.6W		80W/6=13.3W/270W/11=24.5W



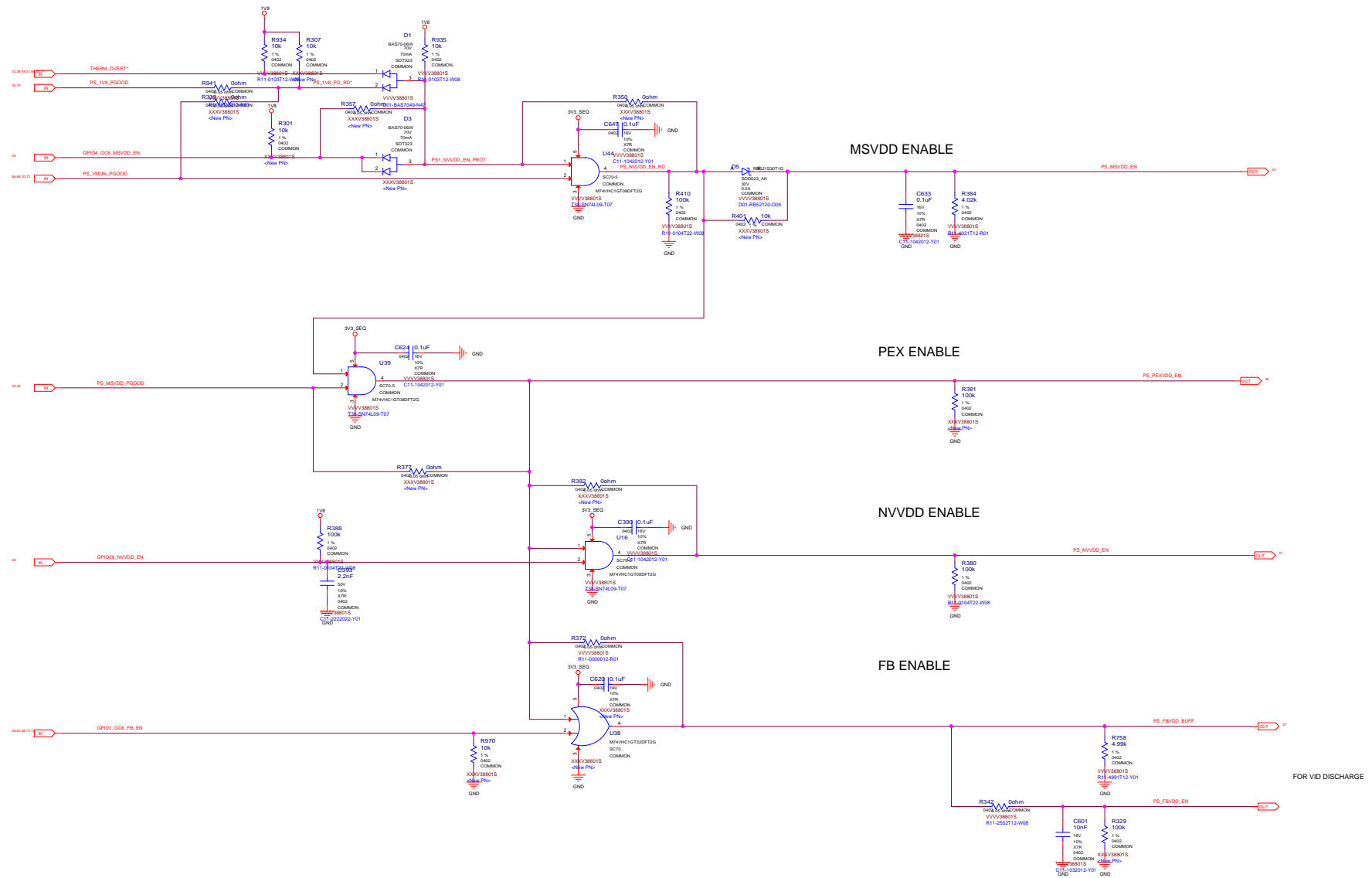
SEQUENCE:5V,1V8,3V3_SEQ ENABLE



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Size Custom	Document Description SEQUENCE:5V,1V8,3V3_SEQ ENABLE	Rev 8.0
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SEQUENCE:NV,PEX,FB ENABLE

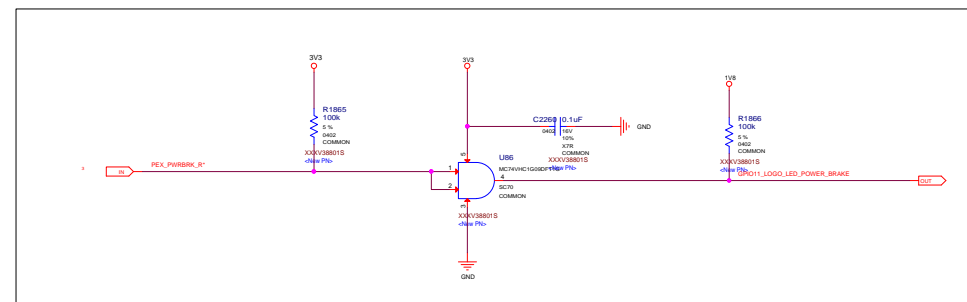


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Size Custom	Document Description SEQUENCE:NV,PEX,FB ENABLE	Rev 8.0
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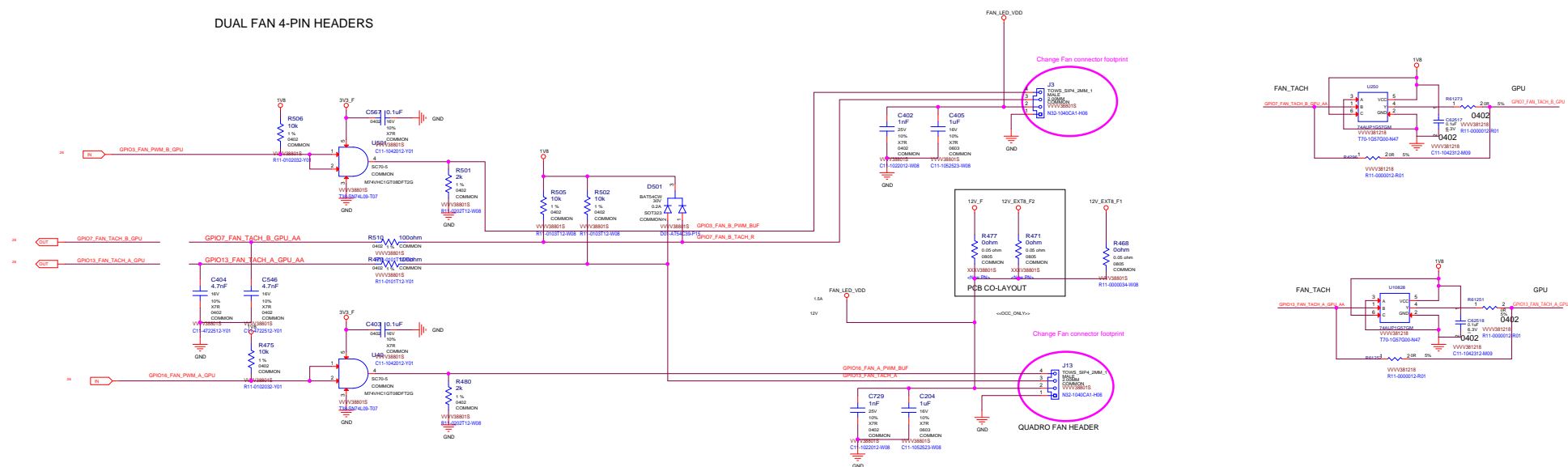
3V3 can be monitored by OVR-M with un-used Channel



MISC: LED & FAN

2-PIN LED HEADER

DUAL FAN 4-PIN HEADERS



MISC: RGBW LED REF

CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALINGN WITH PASH
IF ADDITIONAL POWER CONSUPTION R
NEEDED, IT SHOULD BE ON LED MOD.

1: 12V
2: BLUE
3: GREEN
4: RED
5: WHITE


WHITE DRIVE

LOGO LED RED

RED DRIVE

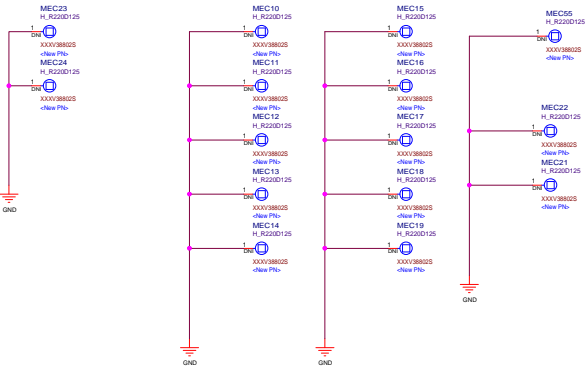
GREEN DRIVE

BLUE DRIVE

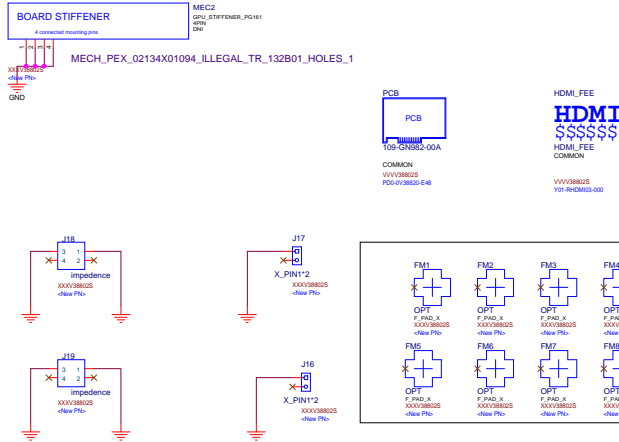
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Size	Document Description	Rev
Custom	MISC: RGBW LED REF	8.0
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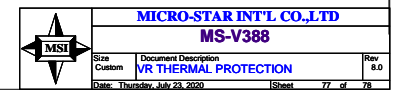
Mechanical: Mounting holes

Mechanical Holes Symbol



BACK STIFFENER:



[illegible]

PCI TERM

