

P727-A01: G96, GB1-128, GDDR3, DL-DVI, DL-DVI/VGA, SD/HDTV

PAGE SUMMARY:

- Page 1: TABLE OF CONTENTS
- Page 2: PCI EXPRESS INTERFACE, PEX_VDD DECOUPLING CAPS
- Page 3: FBA MEMORY INTERFACE, GPU NVVDD & FBVDDQ DECOUPLING CAPS
- Page 4: FBA 16/32Mx32 GDDR3 MEMORIES, FBA COMMAND BUS PU'S, FBA CLK TERMS
- Page 5: FBA MEMORY FBVDDQ DECOUPLING CAPS
- Page 6: FBC MEMORY INTERFACE
- Page 7: FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS PU'S, FBC CLK TERMS
- Page 8: FBC MEMORY FBVDDQ DECOUPLING CAPS, GPU GND CONNECTIONS
- Page 9: DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH
- Page 10: DACC FILTERS, DACC SYNC BUFFERS & DB15 MID
- Page 11: TMDS LINK A/B, DVI CONNECTOR SOUTH
- Page 12: TMDS LINK C/D, AC COUPLING, PD's, DVI CONNECTOR MID
- Page 13: MIOA & MIOB, SLI CONNECTOR
- Page 14: DACB FILTERS, MINIDIN CONNECTOR NORTH, SD/HD VIDEO OUTPUT CONNECTOR
- Page 15: SPDIF-IN, XTAL, MECHANICALS, THERMALS
- Page 16: EXTERNAL THERMAL SENSOR, 4PIN FAN CONTROL, GPIO
- Page 17: BIOS ROM, HDCP ROM, STRAPPING OPTIONS
- Page 18: HYBRID POWER CIRCUIT
- Page 19: POWER SUPPLY LINEARS: 5V, DDC5V, IFP PLLVDD, IFP IOVDD, MIO VDD, 3V3 FILTER, 12V FILTER
- Page 20: POWER SUPPLY: FBVDDQ SINGLE PHASE SWITCHER
- Page 21: POWER SUPPLY: PEX_VDD SINGLE PHASE SWITCHER
- Page 22: POWER SUPPLY: NVVDD DUAL PHASE SWITCHER
- Page 23: POWER SUPPLY: NVVDD VOLTAGE SELECTION

REV	VARIANT	NPVN	ASSEMBLY
B	BASE	600-10727-0000-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKJ0000	600-10727-0000-100	G96-400, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
2	SKJ0001	600-10727-0001-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI HDTV-Out
3	SKJ0002	600-10727-0002-100	G96-300, 650/800MHz 256MB 16Mx32 GDDR3, DVI DVI
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TABLE OF CONTENTS

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA



NV_PN

600-10727-base-sch A

ID

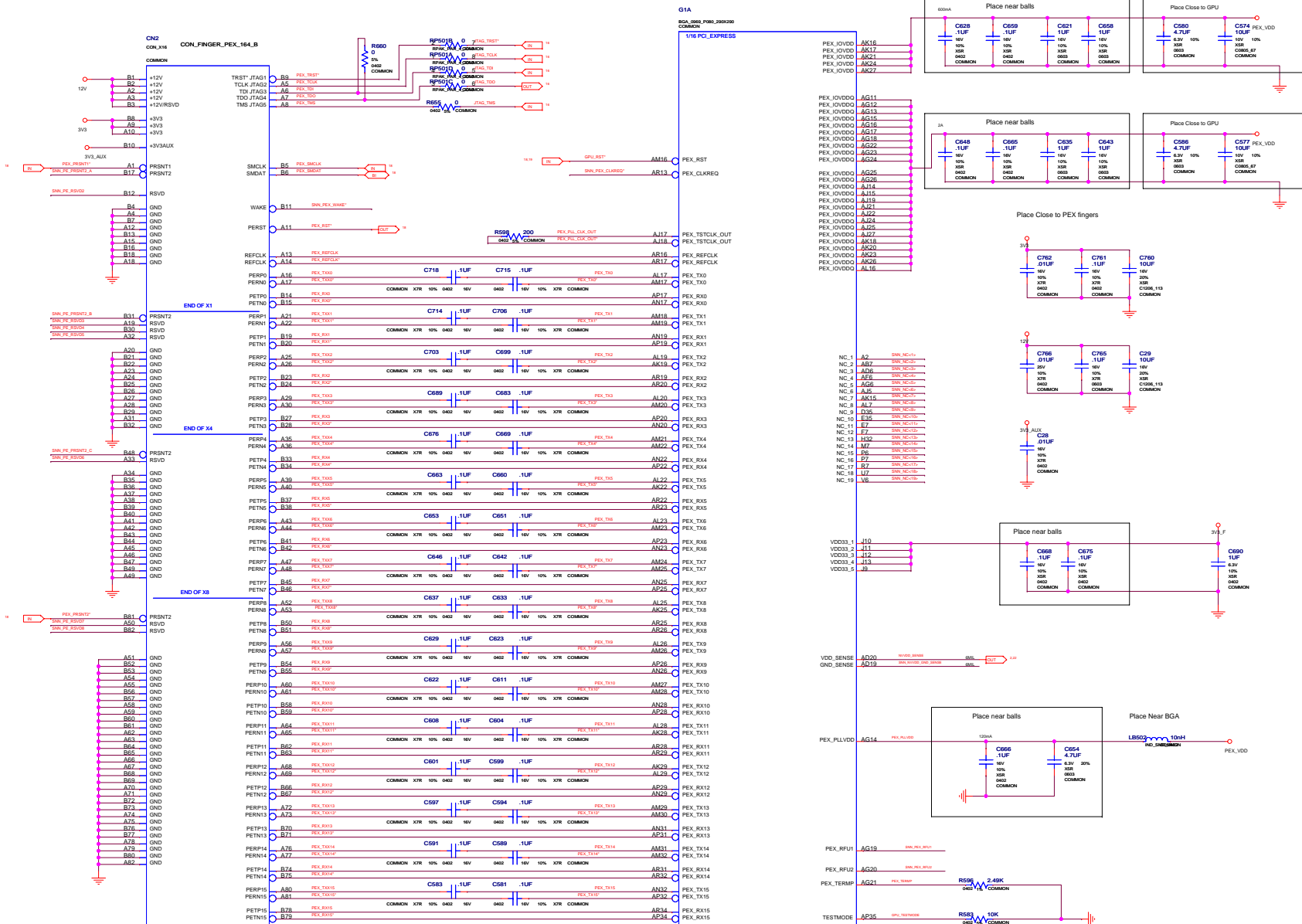
PAGE

NAME

DATE

31-OCT-2009

16X PEX INTERFACE



NET	DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL
PEX_RX0	PEX_TX0	10000	1
PEX_RX1	PEX_TX1	10000	1
PEX_RX2	PEX_TX2	10000	1
PEX_RX3	PEX_TX3	10000	1
PEX_RX4	PEX_TX4	10000	1
PEX_RX5	PEX_TX5	10000	1
PEX_RX6	PEX_TX6	10000	1
PEX_RX7	PEX_TX7	10000	1
PEX_RX8	PEX_TX8	10000	1
PEX_RX9	PEX_TX9	10000	1
PEX_RX10	PEX_TX10	10000	1
PEX_RX11	PEX_TX11	10000	1
PEX_RX12	PEX_TX12	10000	1
PEX_RX13	PEX_TX13	10000	1
PEX_RX14	PEX_TX14	10000	1
PEX_RX15	PEX_TX15	10000	1
PEX_RX16	PEX_TX16	10000	1
PEX_RX17	PEX_TX17	10000	1
PEX_RX18	PEX_TX18	10000	1
PEX_RX19	PEX_TX19	10000	1
PEX_RX20	PEX_TX20	10000	1
PEX_RX21	PEX_TX21	10000	1
PEX_RX22	PEX_TX22	10000	1
PEX_RX23	PEX_TX23	10000	1
PEX_RX24	PEX_TX24	10000	1
PEX_RX25	PEX_TX25	10000	1
PEX_RX26	PEX_TX26	10000	1
PEX_RX27	PEX_TX27	10000	1
PEX_RX28	PEX_TX28	10000	1
PEX_RX29	PEX_TX29	10000	1
PEX_RX30	PEX_TX30	10000	1
PEX_RX31	PEX_TX31	10000	1
PEX_RX32	PEX_TX32	10000	1
PEX_RX33	PEX_TX33	10000	1
PEX_RX34	PEX_TX34	10000	1
PEX_RX35	PEX_TX35	10000	1
PEX_RX36	PEX_TX36	10000	1
PEX_RX37	PEX_TX37	10000	1
PEX_RX38	PEX_TX38	10000	1
PEX_RX39	PEX_TX39	10000	1
PEX_RX40	PEX_TX40	10000	1
PEX_RX41	PEX_TX41	10000	1
PEX_RX42	PEX_TX42	10000	1
PEX_RX43	PEX_TX43	10000	1
PEX_RX44	PEX_TX44	10000	1
PEX_RX45	PEX_TX45	10000	1
PEX_RX46	PEX_TX46	10000	1
PEX_RX47	PEX_TX47	10000	1
PEX_RX48	PEX_TX48	10000	1
PEX_RX49	PEX_TX49	10000	1
PEX_RX50	PEX_TX50	10000	1
PEX_RX51	PEX_TX51	10000	1
PEX_RX52	PEX_TX52	10000	1
PEX_RX53	PEX_TX53	10000	1
PEX_RX54	PEX_TX54	10000	1
PEX_RX55	PEX_TX55	10000	1
PEX_RX56	PEX_TX56	10000	1
PEX_RX57	PEX_TX57	10000	1
PEX_RX58	PEX_TX58	10000	1
PEX_RX59	PEX_TX59	10000	1
PEX_RX60	PEX_TX60	10000	1
PEX_RX61	PEX_TX61	10000	1
PEX_RX62	PEX_TX62	10000	1
PEX_RX63	PEX_TX63	10000	1
PEX_RX64	PEX_TX64	10000	1
PEX_RX65	PEX_TX65	10000	1
PEX_RX66	PEX_TX66	10000	1
PEX_RX67	PEX_TX67	10000	1
PEX_RX68	PEX_TX68	10000	1
PEX_RX69	PEX_TX69	10000	1
PEX_RX70	PEX_TX70	10000	1
PEX_RX71	PEX_TX71	10000	1
PEX_RX72	PEX_TX72	10000	1
PEX_RX73	PEX_TX73	10000	1
PEX_RX74	PEX_TX74	10000	1
PEX_RX75	PEX_TX75	10000	1
PEX_RX76	PEX_TX76	10000	1
PEX_RX77	PEX_TX77	10000	1
PEX_RX78	PEX_TX78	10000	1
PEX_RX79	PEX_TX79	10000	1
PEX_RX80	PEX_TX80	10000	1
PEX_RX81	PEX_TX81	10000	1
PEX_RX82	PEX_TX82	10000	1
PEX_RX83	PEX_TX83	10000	1
PEX_RX84	PEX_TX84	10000	1
PEX_RX85	PEX_TX85	10000	1
PEX_RX86	PEX_TX86	10000	1
PEX_RX87	PEX_TX87	10000	1
PEX_RX88	PEX_TX88	10000	1
PEX_RX89	PEX_TX89	10000	1
PEX_RX90	PEX_TX90	10000	1
PEX_RX91	PEX_TX91	10000	1
PEX_RX92	PEX_TX92	10000	1
PEX_RX93	PEX_TX93	10000	1
PEX_RX94	PEX_TX94	10000	1
PEX_RX95	PEX_TX95	10000	1
PEX_RX96	PEX_TX96	10000	1
PEX_RX97	PEX_TX97	10000	1
PEX_RX98	PEX_TX98	10000	1
PEX_RX99	PEX_TX99	10000	1

1.0	NVDD0_SENSE	0.2V
1.0	NVDD0_SENSE	0V
1.0	PEX_PL1VDD	1.00V 1.2V
1.0	PEX_PL1VDD	1.00V 1.2V
1.0	PEX_PL1VDD	1.00V 1.2V

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 10000 ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	PEX EXPRESS INTERFACE; PEX_VDD DECOUPLING CAPS

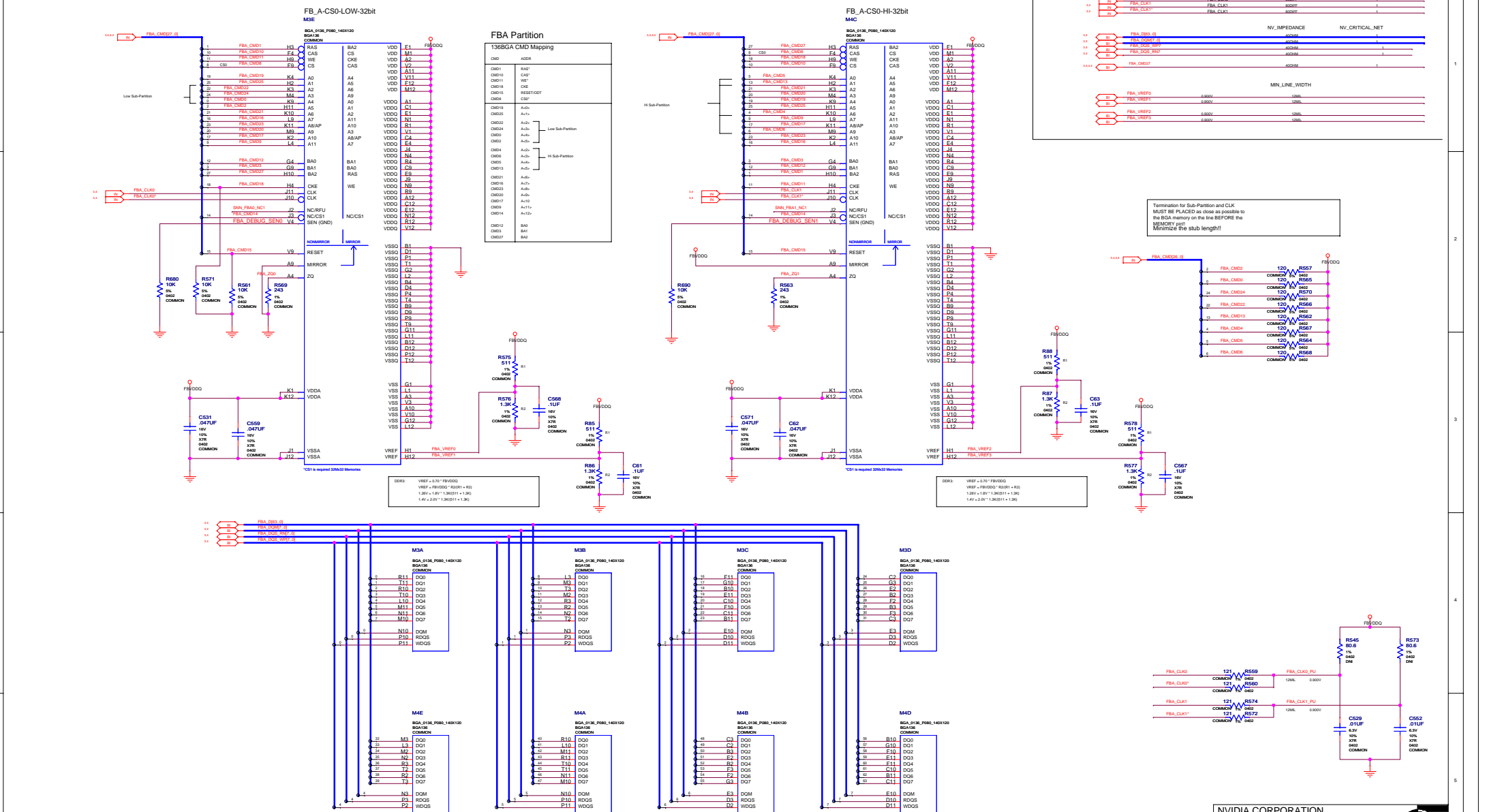
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTIC LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION
3701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050 USA

NV_PN 600-10727-base-sch A

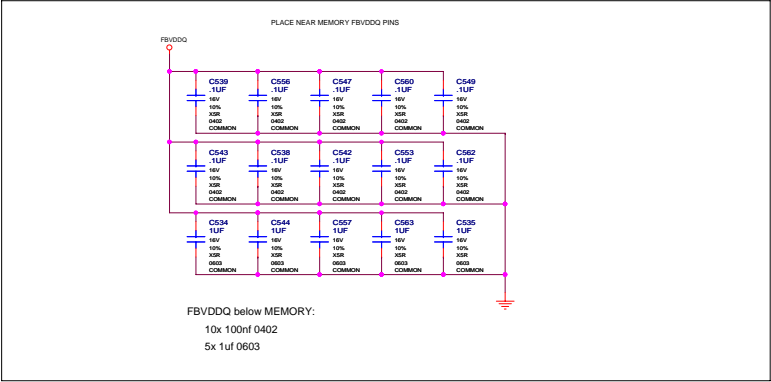
DATE 31-OCT-2007

FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3

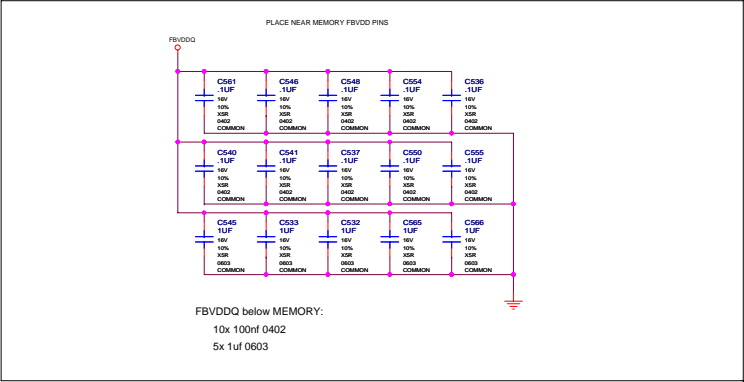


FRAME BUFFER: PARTITION A DECOUPLING

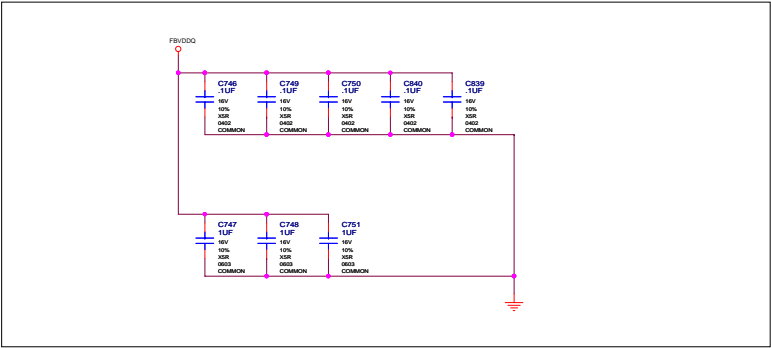
Decoupling for FBA 0..31



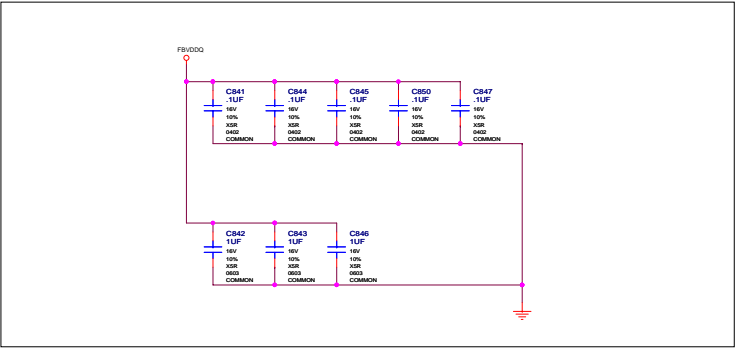
Decoupling for FBA 32..63



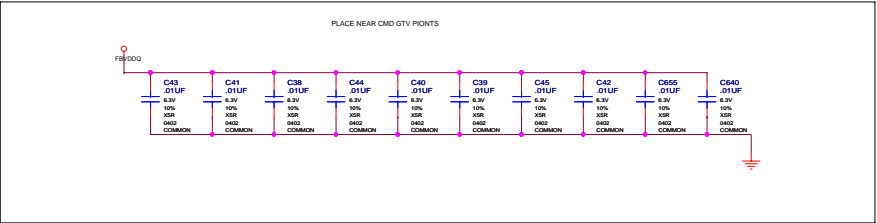
Decoupling for FBA A1 0..31



Decoupling for FBA A1 0..31



Return path coupling GND/FBVDDQ for FBA



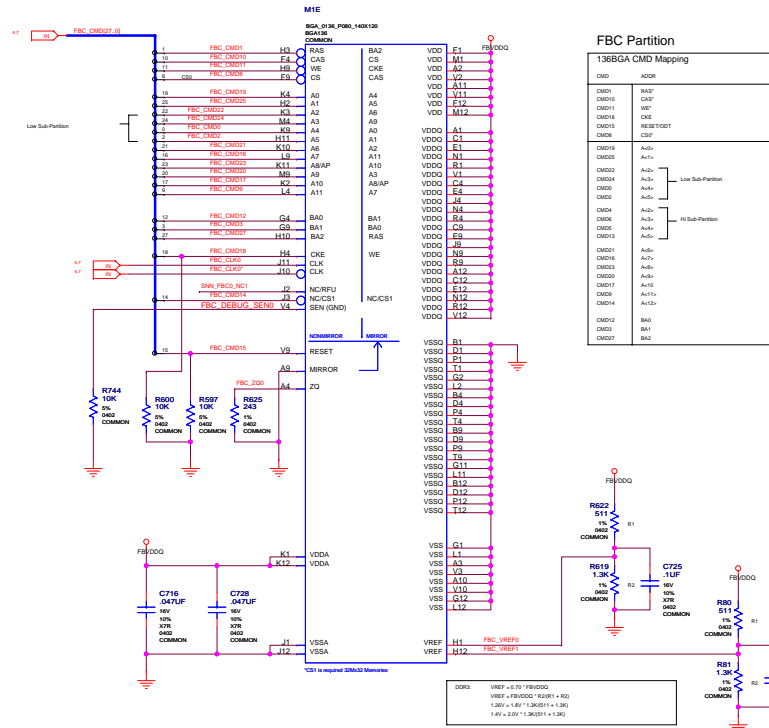
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASIC LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 1000 ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

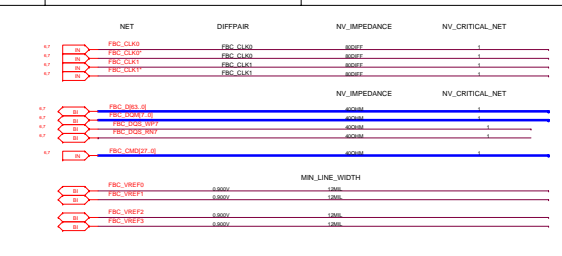
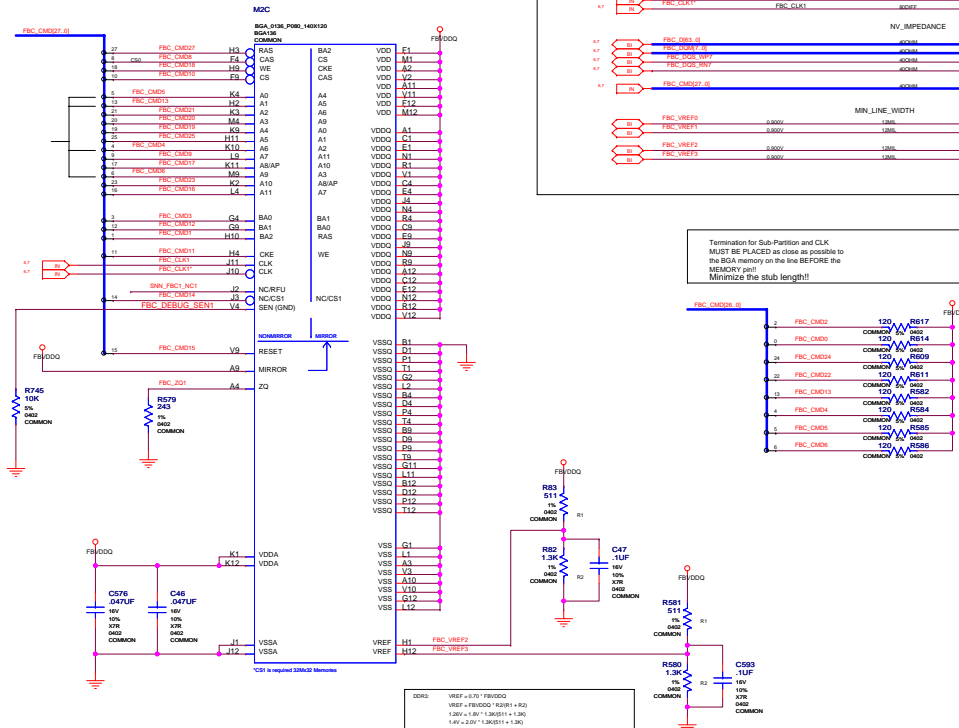
NVIDIA CORPORATION	
3701 SAN TOMAS EXPRESSWAY	
SANTA CLARA, CA 95050, USA	
NV_PN	600-10727-base-sch A
ID	PAGE
NAME	DATE 31-OCT-2007

FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3

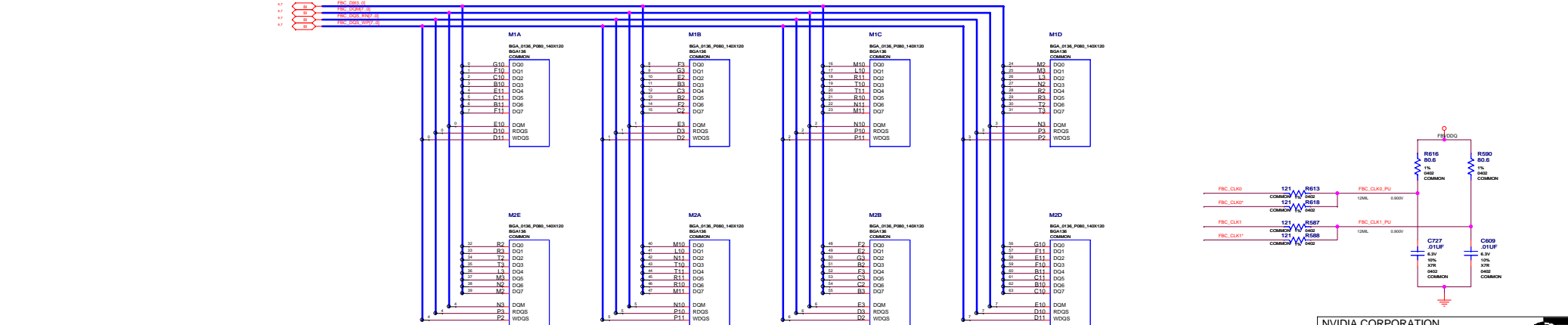
FB_C-CS0-LOW-32bit



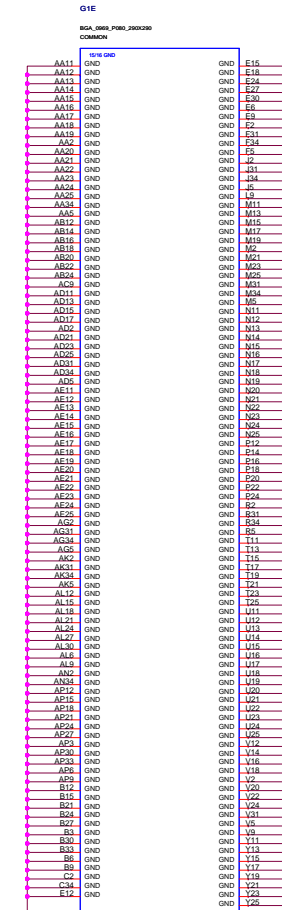
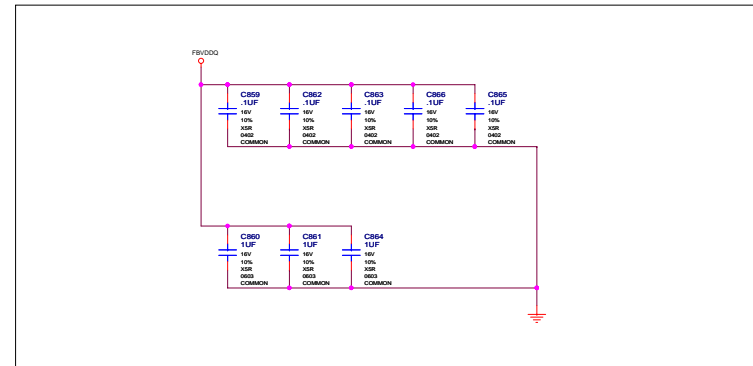
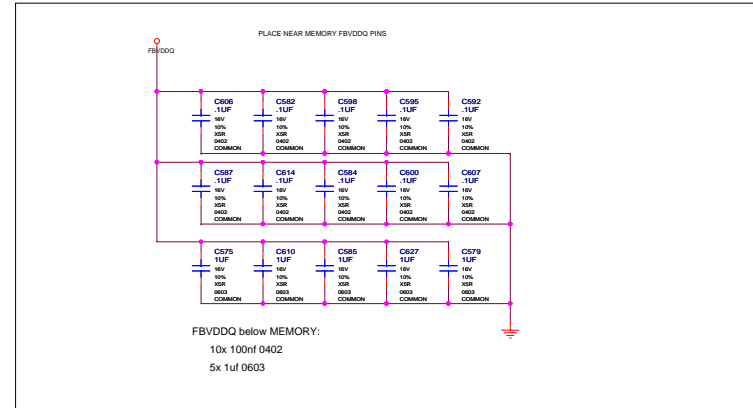
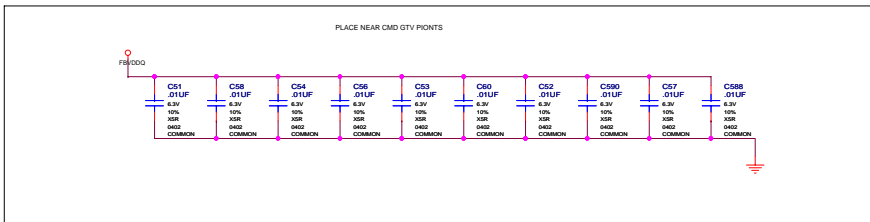
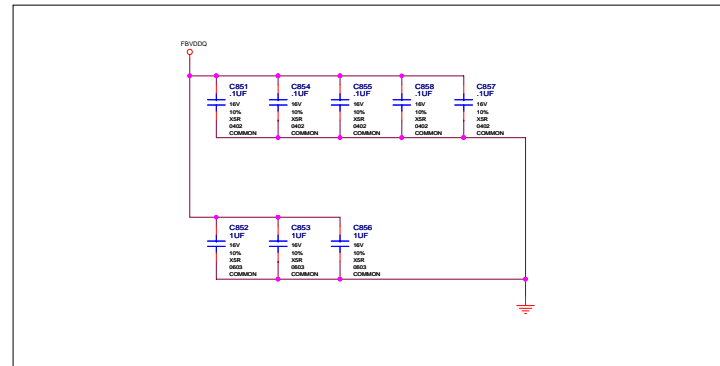
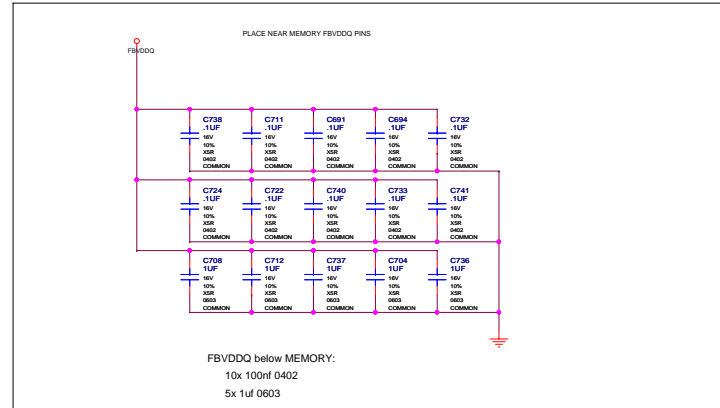
FB_C-CS0-HI-32bit



Termination for Sub-Partition and CLK MUST BE PLACED as close as possible to the BGA memory on the line BEFORE the MEMORY pin!
Minimize the stub length!




Decoupling for FBC 0..31



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

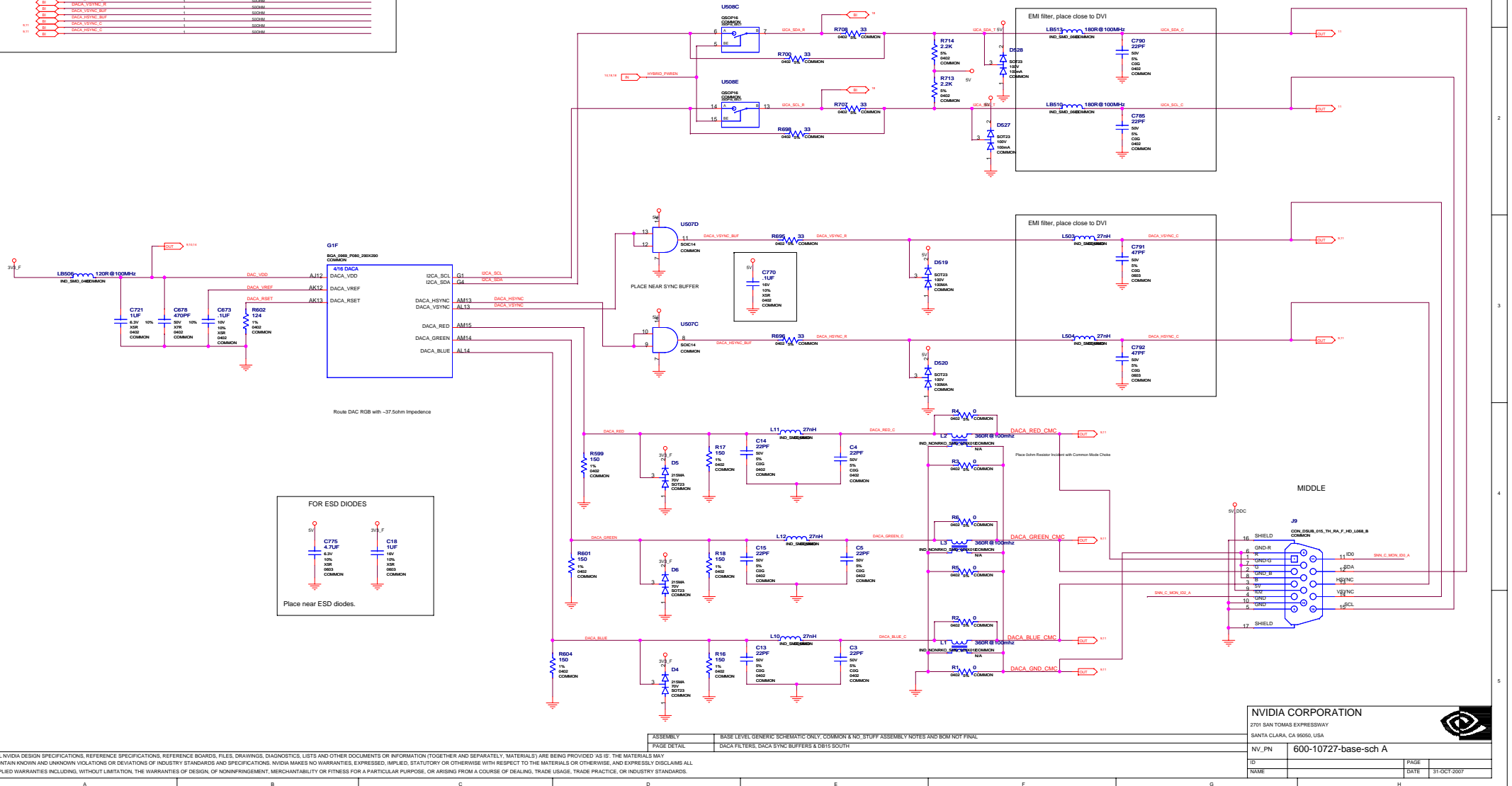
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS, GPU GND CONNECTIONS

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN 600-10727-base-sch A			
ID		PAGE	
NAME		DATE	31-OCT-2007

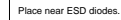
Primary Display (DACA), DVI-I

DACA RGB-FILTER

NET_NAME	INV_CRITICAL_NET	IMPEDANCE	MIN_LINE_WIDTH
DACA_VDD		3.3V	120u
DACA_VREF			120u
DACA_VREF			120u
DACA_RED		750m	
DACA_GREEN		750m	
DACA_BLUE		750m	
DACA_RED_C		750m	
DACA_GREEN_C		750m	
DACA_BLUE_C		750m	
DACA_GND_CMC			20
DACA_RED_CMC		750m	
DACA_GREEN_CMC		750m	
DACA_BLUE_CMC		750m	
DACA_HSYNC		500m	
DACA_VSYNC		500m	
DACA_VSYNC_B		500m	
DACA_VSYNC_R		500m	
DACA_VSYNC_G		500m	
DACA_VSYNC_C		500m	
DACA_HSYNC_C		500m	
DACA_VSYNC_C		500m	



Accession	Gene	Protein	Accession
10.12	DACC_VSYN2_C	1	SDCHM
10.12	DACC_HSYN2_C	1	SDCHM



PAGE DETAIL	DACC FILTERS, DACC SYNC BUFFERS & DB15 MI
-------------	---

CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

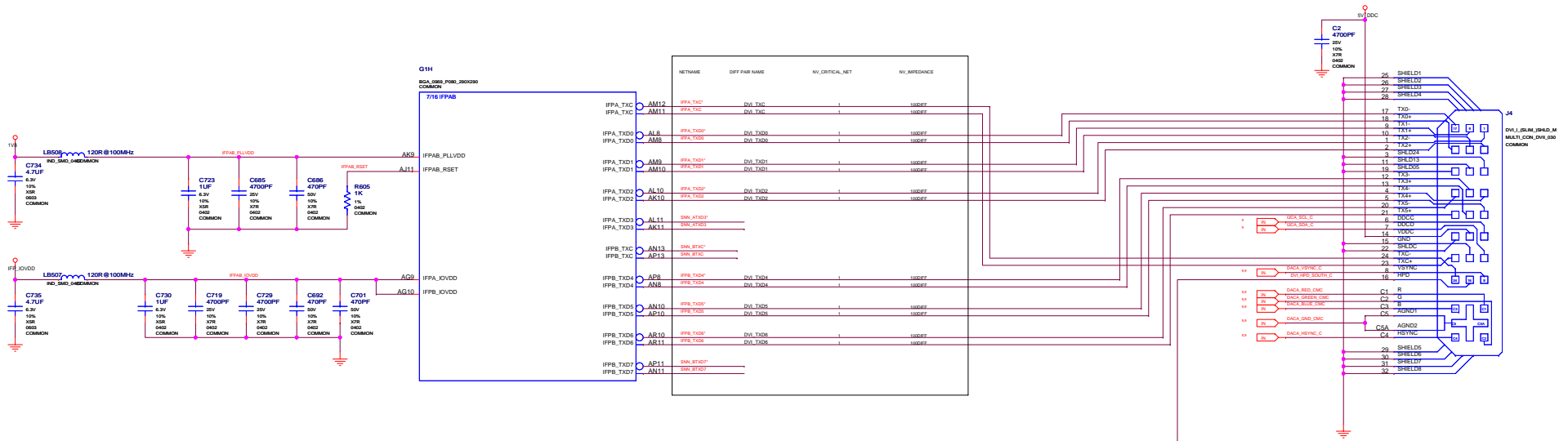
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



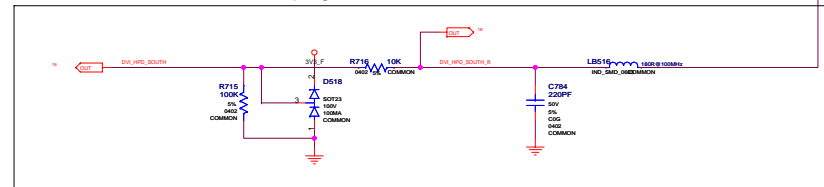
ID	
NAME	

	H
--	---

TMDS LINK: A & B



Hotplug Detection



NETNAME	MIN_LINE_WIDTH	VOLTAGE
FFAB_PU_VDD	12MIL	1.8V
FFAB_IO_VDD	12MIL	3.3V
FFABRESET	12MIL	

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

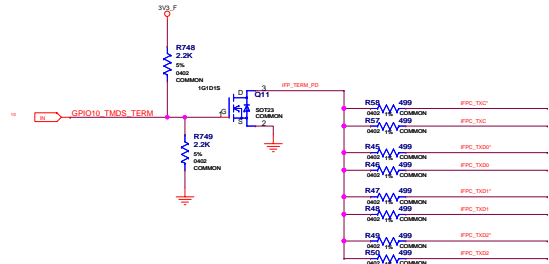


NV_PN	600-10727-base-sch A
-------	----------------------

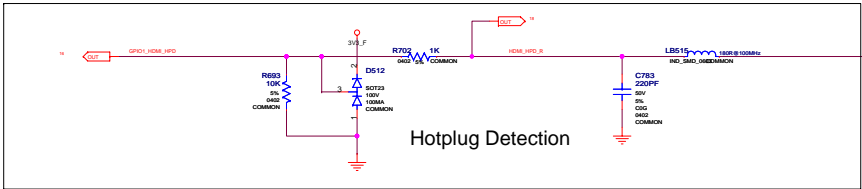
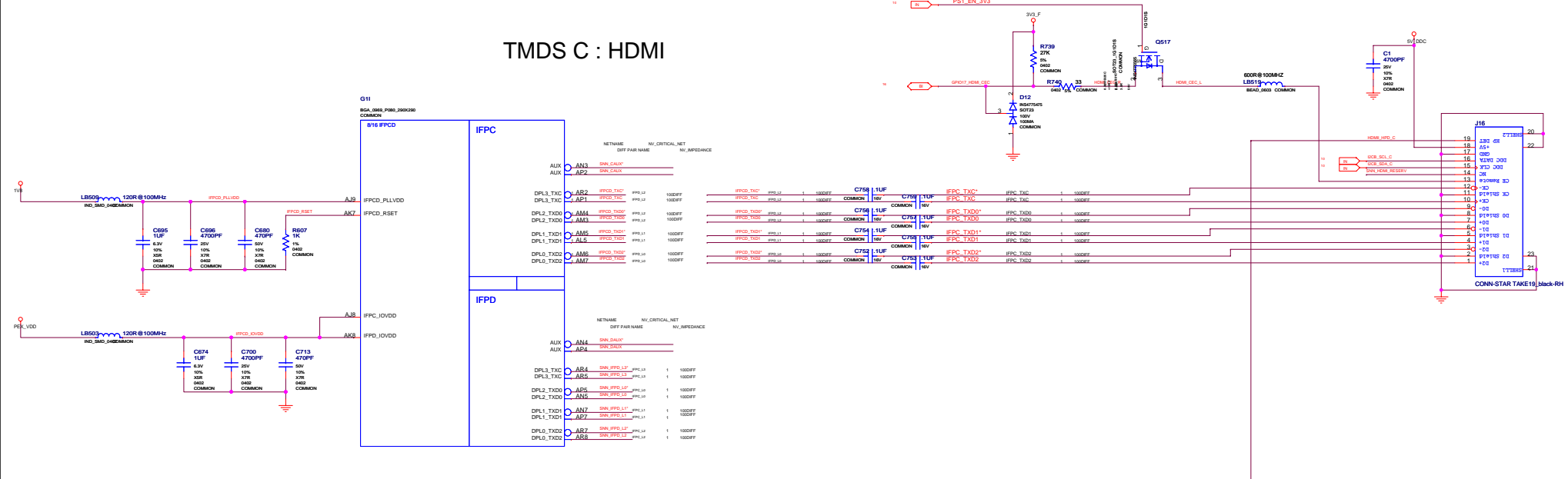
ID	PAGE
NAME	DATE 31-OCT-2007

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

TMDS LINK: C & D



TMDS C : HDMI



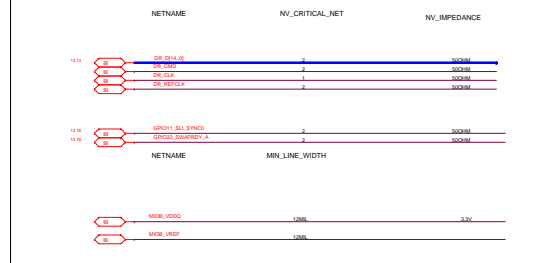
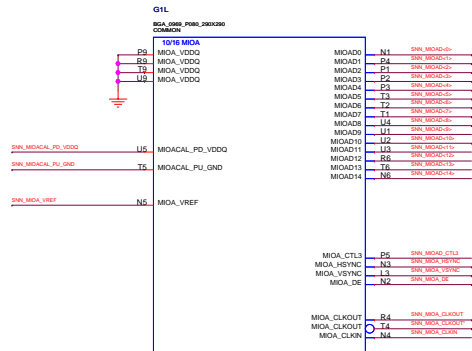
NETNAME	MIN_LENGTH	VOLTAGE
IFCD_FLVDD	1200	1.8V
IFCD_OVDD	1200	3.3V
IFCD_TERM_PD	1000	1.8V

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTIC LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE PRACTICE, OR INDUSTRY STANDARDS.

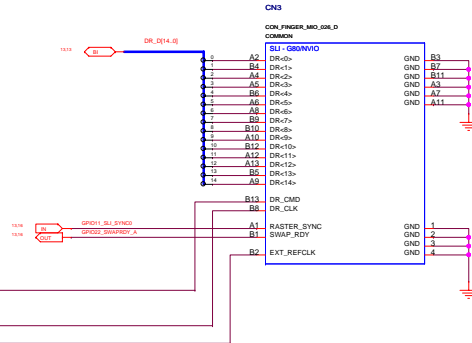
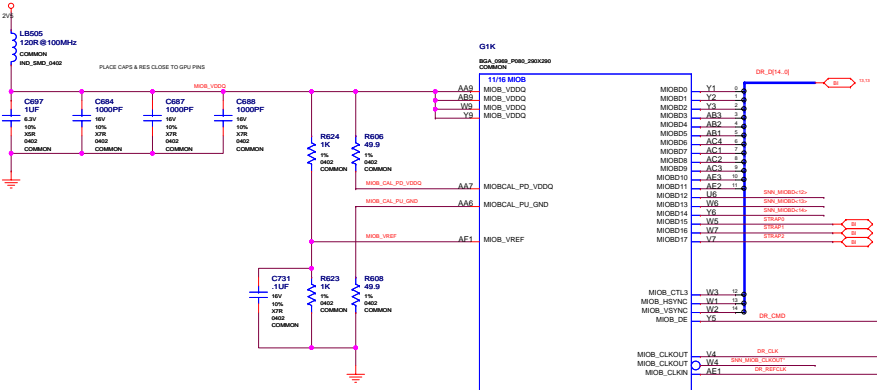
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 3100FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK C/D; AC COUPLING; PD; DVI CONNECTOR MID

NVIDIA CORPORATION	
3701 SAN TOMAS EXPRESSWAY	
SANTA CLARA, CA 95050, USA	
NV_PN	600-10727-base-sch A
ID	
NAME	
PAGE	31-OCT-2007

MIOA/B SLI



SLI Connector



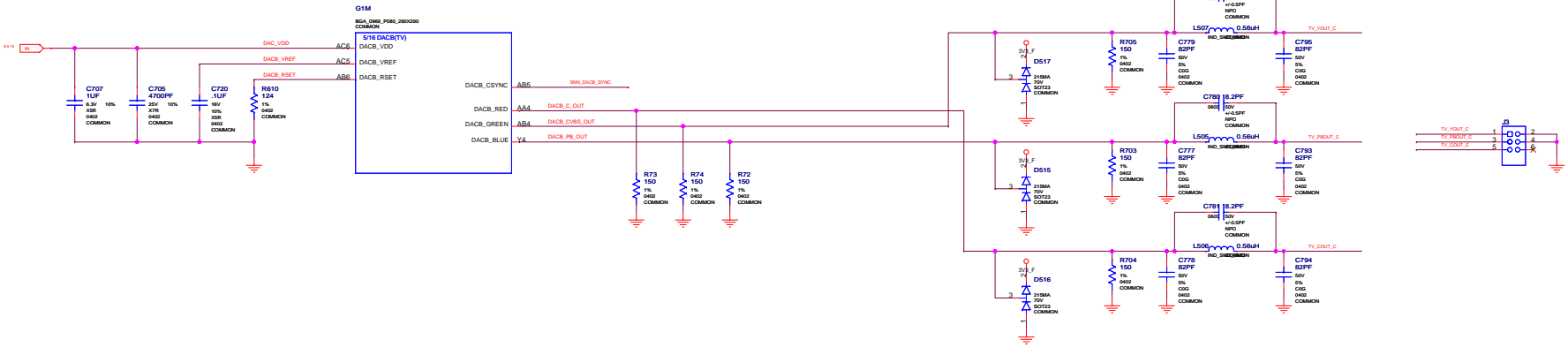
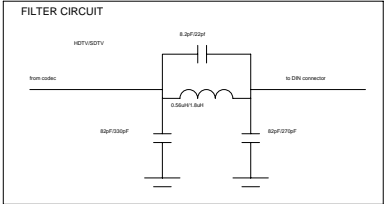
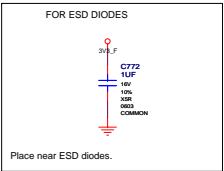
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTIC LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MIOA & MIOB SLI CONNECTOR

NVIDIA CORPORATION	
3701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA	
NV_PN	600-10727-base-sch A
ID	PAGE
NAME	DATE 31-OCT-2007

DACB: SD/HD VIDEO OUT CONNECTOR

NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
DACB_C_OUT		75OHM	1
DACB_CVBS_OUT		75OHM	1
DACB_PB_OUT		75OHM	1
TV_PROUT_C		75OHM	1
TV_PROUT_S		75OHM	1
TV_PROUT_E		75OHM	1
DACB_VREF	100M		
DACB_RSET	100M		



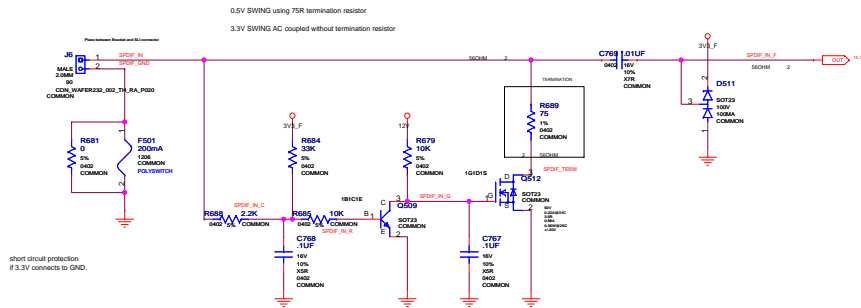
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. STOP/ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTER, MINOR CONNECTOR NORTH, SD/HD VIDEO OUTPUT CONNECTOR

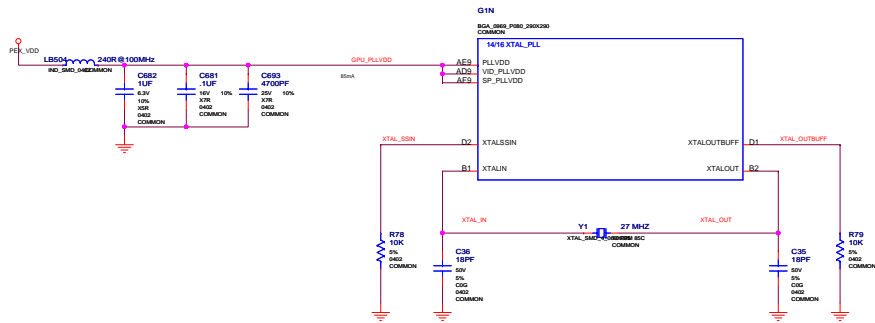
NVIDIA CORPORATION	
3701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA	
NV_PN	600-10727-base-sch A
ID	
NAME	
PAGE	31-OCT-2007

XTAL/PLLVD/SPDIF IN

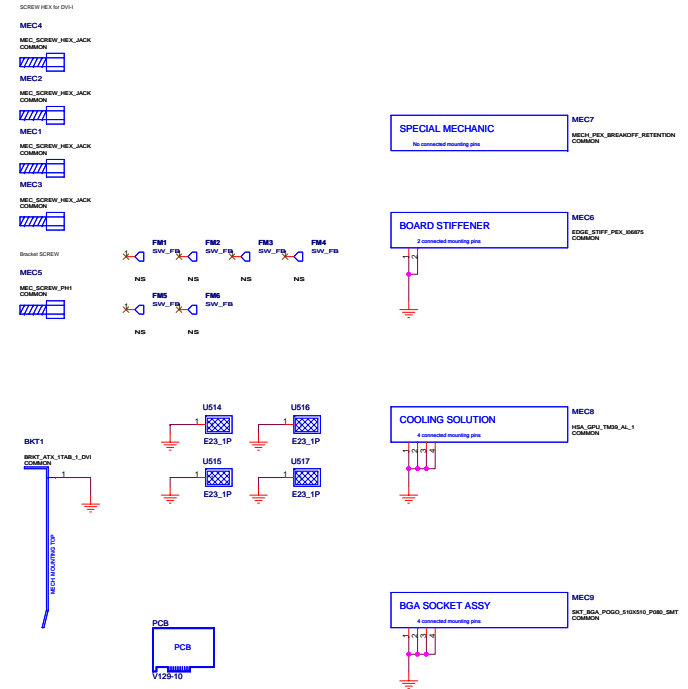
SPDIF IN



XTAL/GPU_PLLVDD



MECHANICALS & THERMALS

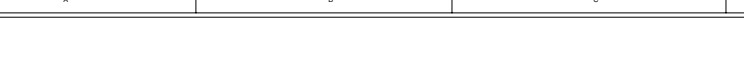
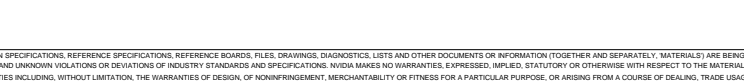
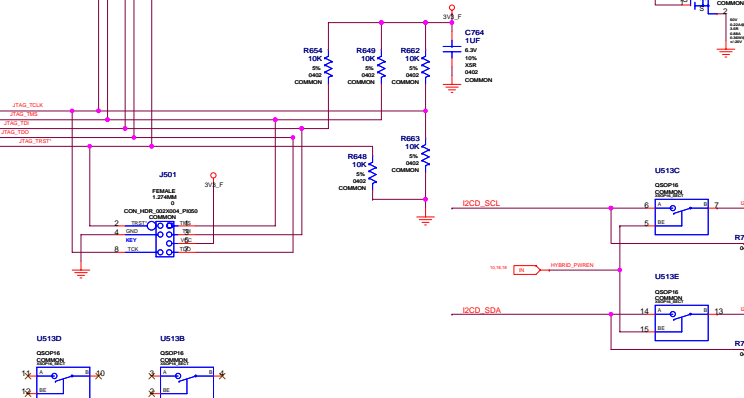
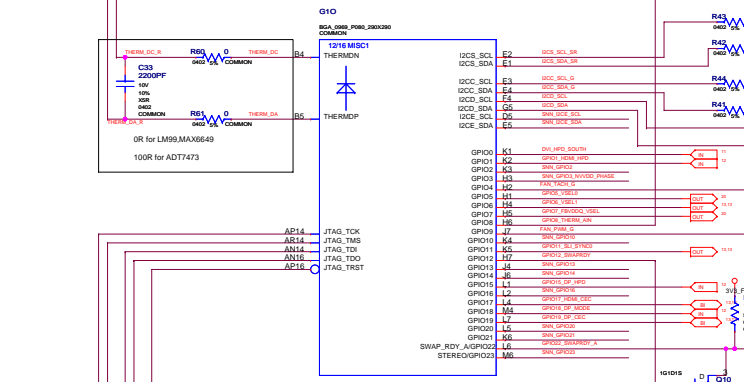
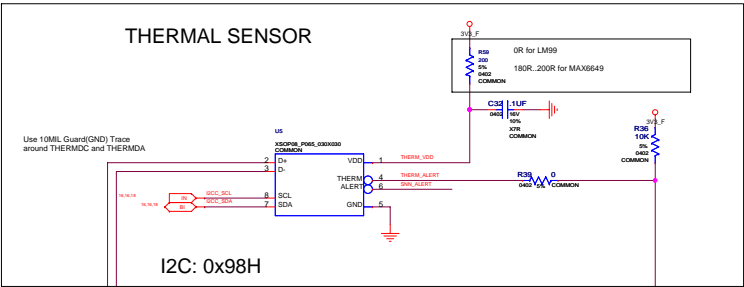


NETNAME	MIN_LINE_WIDTH
GPU_PLLVDD	1200L 1.2V
XTAL_IN	1000L
XTAL_OUT	1000L
XTAL_SSN	1000L
XTAL_OUTBUFF	1000L
SPDIF_IN	1000L 2
SPDIF_IN	1000L 2
SPDIF_OUT	1000L 0V

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTIC LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

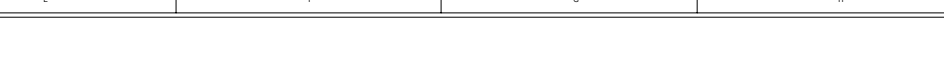
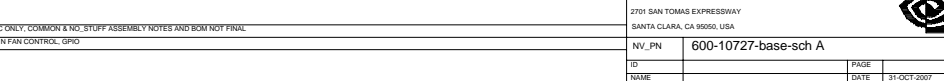
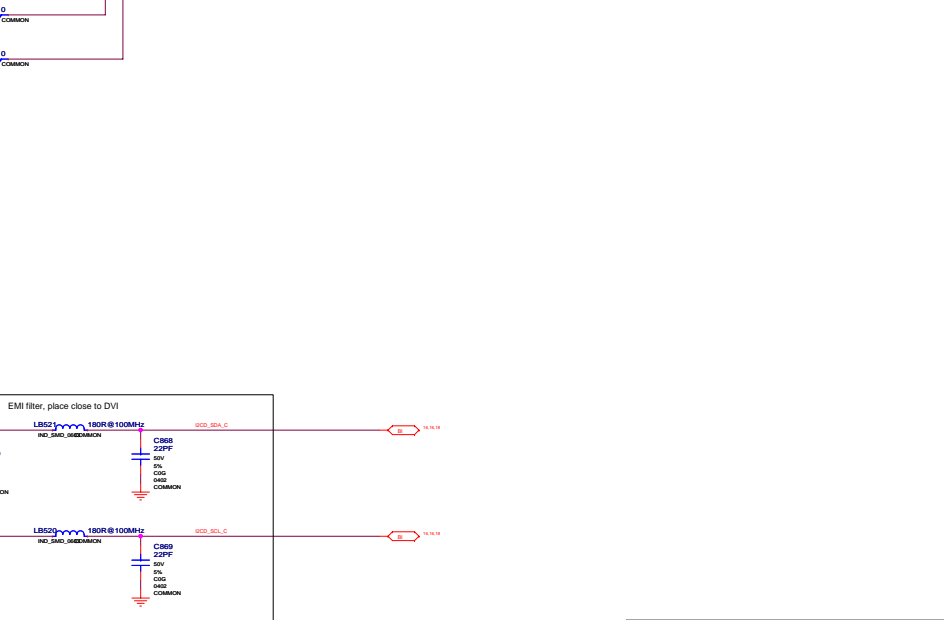
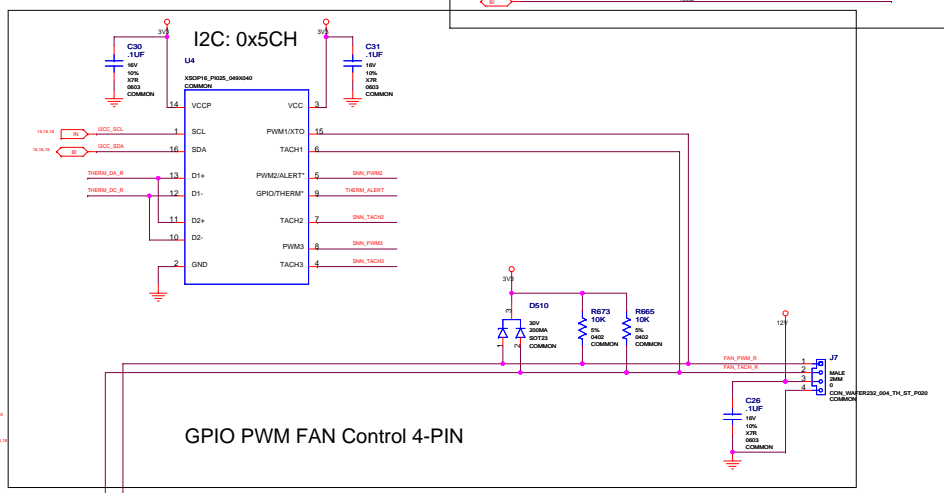
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDIF-IN, XTAL, MECHANICALS, THERMALS

NVIDIA CORPORATION	
3701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA	
NV_PN	600-10727-base-sch A
ID	PAGE
NAME	DATE 31-OCT-2007



GPIO & JTAG

THERMAL SENSOR, FAN CONTROLLER
uses 3V3: always on.



NETNAME	MIN_LINE_WIDTH	VOLTAGE
THERM_DC	10MIL	3V3
THERM_DA	10MIL	3V3
THERM_DB	10MIL	3V3
THERM_DC_E	10MIL	3V3
THERM_DA_E	10MIL	3V3
THERM_DB_E	10MIL	3V3

ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO. 310FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE: DETAIL

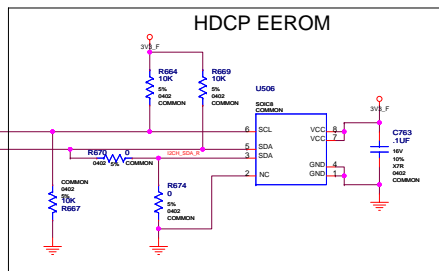
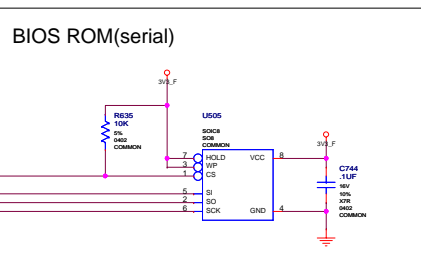
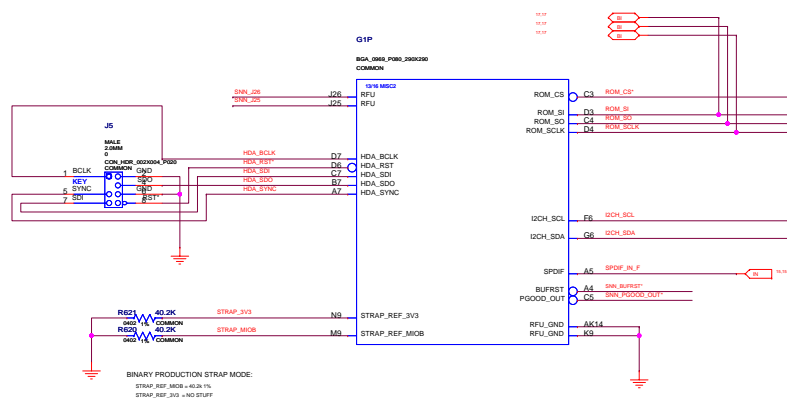
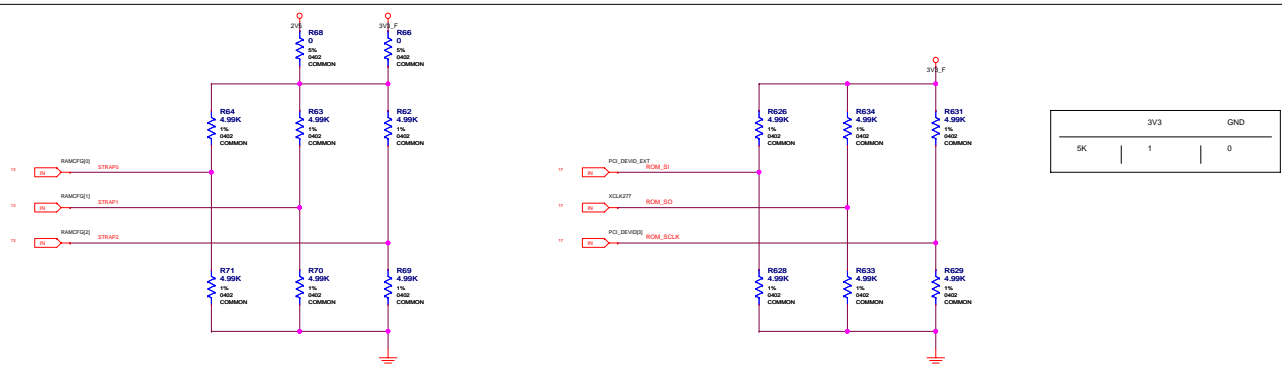
NVIDIA CORPORATION	
3701 SAN TOMAS EXPRESSWAY	
SANTA CLARA, CA 95050, USA	
NV_PN	600-10727-base-sch A
ID	
NAME	
PAGE	
DATE	31-OCT-2007



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTIC LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE PRACTICE, OR INDUSTRY STANDARDS.

STRAPPING OPTIONS

Assembly: BIOS



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA



NV_PN	600-10727-base-sch A
-------	----------------------

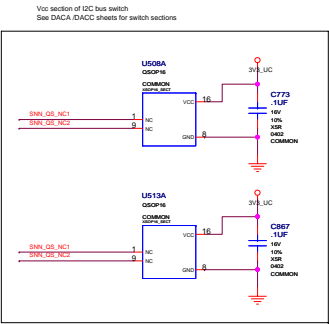
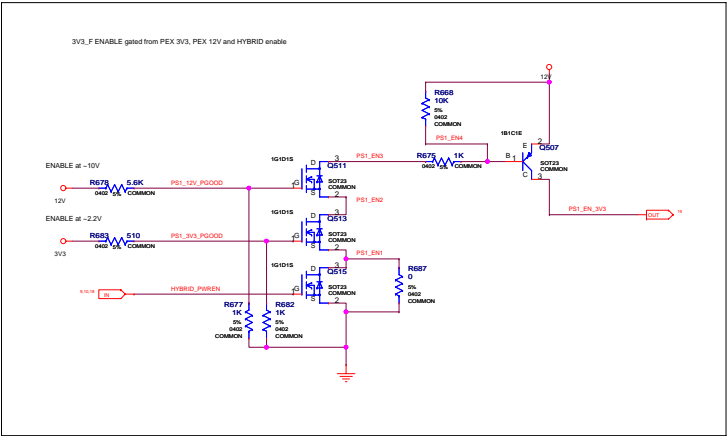
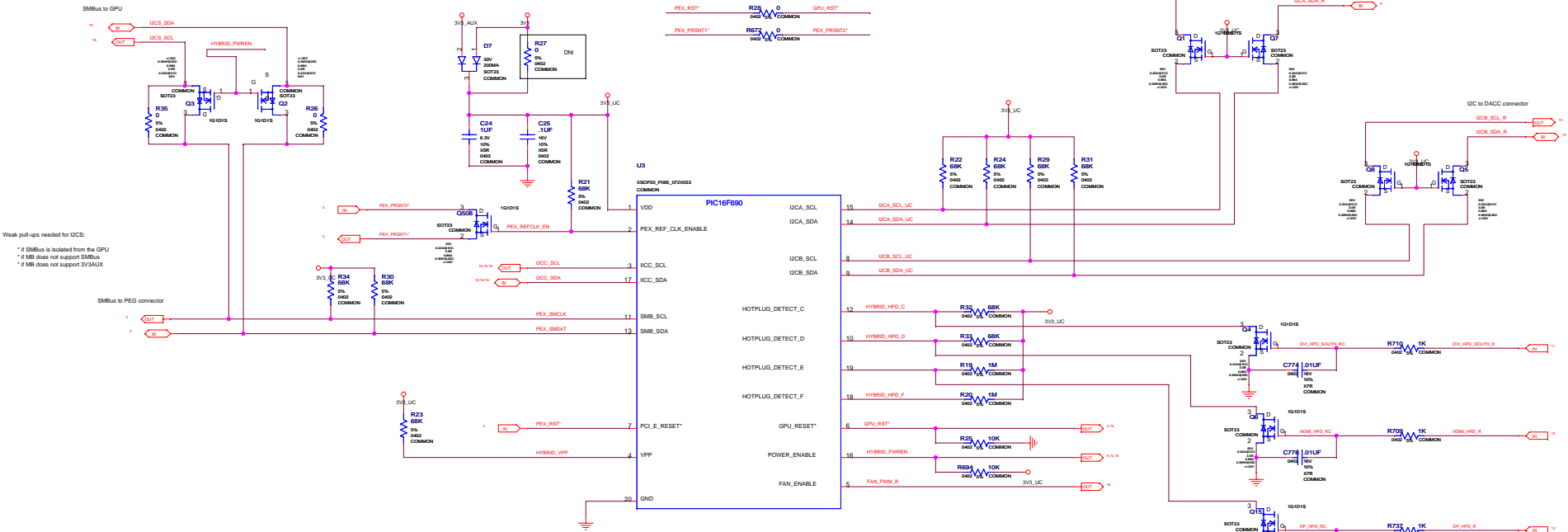
ID	PAGE
NAME	DATE 31-OCT-2007

[illegible]

HYBRID POWER

Per Datasheet:
 $V_f = 400\text{mV}$ at 10mA
* expected current < 2mA

Stuff only to bypass the micro-controller



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

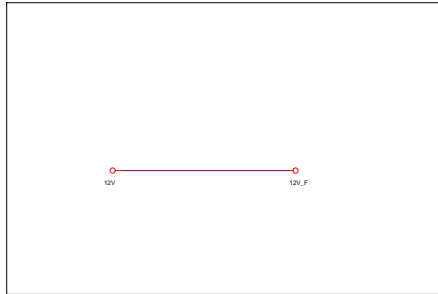
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	HYBRID POWER CIRCUIT

NVIDIA CORPORATION	
3701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA	
NV_PN	600-10727-base-sch A
ID	PAGE
NAME	DATE 31-OCT-2007

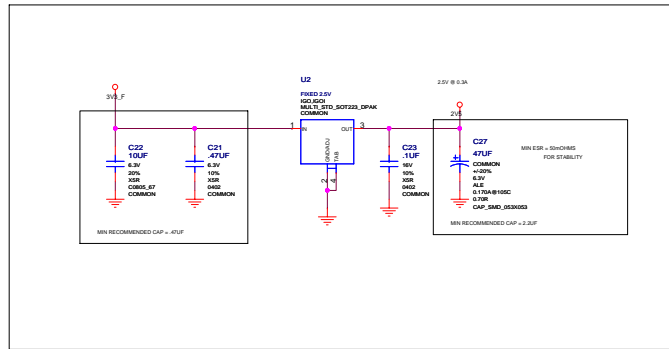
	NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
B	5V_FUSE0	0.1A	100MIL	5V
	5V_D00	0.1A	120MIL	5V
	5V_D0C	0.1A	100MIL	5V
B	5V	0.15A	100MIL	5V
	APC_116_A00		100MIL	1.8V
	V18	0.12A	100MIL	1.8V
B	V15	0.2A	120MIL	2.2V
	V15		100MIL	2V
	GND		100MIL	0V
B	2V5_F	1.5A	100MIL	3.3V
	12V_F	6A	200MIL	12V
	12V_F			

5V DDC

12V filter



MIO_VDD 2.5V

[illegible]

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY LINES: 5V, DDC5V, I/F PLLVDD, I/F IOVDD, MIO VDD, 3V3 FILTER, 12V FILTER

NV_PN	600-10727-base-sch A
-------	----------------------

	PAGE	
	DATE	31-OCT-2007

31-OCT-2007

FrameBuffer: Partition A 16/32Mx32 BGA136 GDDR3

1

2

3

4

5

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

FBA Partition	
136BGA CMD Mapping	
CMD	ADDR
CM01	BA0*
CM02	BA1*
CM03	BA2*
CM04	BA3*
CM05	BA4*
CM06	BA5*
CM07	BA6*
CM08	BA7*
CM09	BA8*
CM10	BA9*
CM11	BA10*
CM12	BA11*
CM13	BA12*
CM14	BA13*
CM15	BA14*
CM16	BA15*
CM17	BA16*
CM18	BA17*
CM19	BA18*
CM20	BA19*
CM21	BA20*
CM22	BA21*
CM23	BA22*
CM24	BA23*
CM25	BA24*
CM26	BA25*
CM27	BA26*

NET		DIFFPAIR	NV_IMPEDANCE	NV_CRITICAL_NET
1	FBA_CMD01	FBA_CMD01	800PT	1
2	FBA_CMD02	FBA_CMD02	800PT	1
3	FBA_CMD03	FBA_CMD03	800PT	1
4	FBA_CMD04	FBA_CMD04	800PT	1
5	FBA_CMD05	FBA_CMD05	800PT	1
6	FBA_CMD06	FBA_CMD06	800PT	1
7	FBA_CMD07	FBA_CMD07	800PT	1
8	FBA_CMD08	FBA_CMD08	800PT	1
9	FBA_CMD09	FBA_CMD09	800PT	1
10	FBA_CMD10	FBA_CMD10	800PT	1
11	FBA_CMD11	FBA_CMD11	800PT	1
12	FBA_CMD12	FBA_CMD12	800PT	1
13	FBA_CMD13	FBA_CMD13	800PT	1
14	FBA_CMD14	FBA_CMD14	800PT	1
15	FBA_CMD15	FBA_CMD15	800PT	1
16	FBA_CMD16	FBA_CMD16	800PT	1
17	FBA_CMD17	FBA_CMD17	800PT	1
18	FBA_CMD18	FBA_CMD18	800PT	1
19	FBA_CMD19	FBA_CMD19	800PT	1
20	FBA_CMD20	FBA_CMD20	800PT	1
21	FBA_CMD21	FBA_CMD21	800PT	1
22	FBA_CMD22	FBA_CMD22	800PT	1
23	FBA_CMD23	FBA_CMD23	800PT	1
24	FBA_CMD24	FBA_CMD24	800PT	1
25	FBA_CMD25	FBA_CMD25	800PT	1
26	FBA_CMD26	FBA_CMD26	800PT	1
27	FBA_CMD27	FBA_CMD27	800PT	1
28	FBA_CMD28	FBA_CMD28	800PT	1
29	FBA_CMD29	FBA_CMD29	800PT	1
30	FBA_CMD30	FBA_CMD30	800PT	1
31	FBA_CMD31	FBA_CMD31	800PT	1
32	FBA_CMD32	FBA_CMD32	800PT	1
33	FBA_CMD33	FBA_CMD33	800PT	1
34	FBA_CMD34	FBA_CMD34	800PT	1
35	FBA_CMD35	FBA_CMD35	800PT	1
36	FBA_CMD36	FBA_CMD36	800PT	1
37	FBA_CMD37	FBA_CMD37	800PT	1
38	FBA_CMD38	FBA_CMD38	800PT	1
39	FBA_CMD39	FBA_CMD39	800PT	1
40	FBA_CMD40	FBA_CMD40	800PT	1
41	FBA_CMD41	FBA_CMD41	800PT	1
42	FBA_CMD42	FBA_CMD42	800PT	1
43	FBA_CMD43	FBA_CMD43	800PT	1
44	FBA_CMD44	FBA_CMD44	800PT	1
45	FBA_CMD45	FBA_CMD45	800PT	1
46	FBA_CMD46	FBA_CMD46	800PT	1
47	FBA_CMD47	FBA_CMD47	800PT	1
48	FBA_CMD48	FBA_CMD48	800PT	1
49	FBA_CMD49	FBA_CMD49	800PT	1
50	FBA_CMD50	FBA_CMD50	800PT	1
51	FBA_CMD51	FBA_CMD51	800PT	1
52	FBA_CMD52	FBA_CMD52	800PT	1
53	FBA_CMD53	FBA_CMD53	800PT	1
54	FBA_CMD54	FBA_CMD54	800PT	1
55	FBA_CMD55	FBA_CMD55	800PT	1
56	FBA_CMD56	FBA_CMD56	800PT	1
57	FBA_CMD57	FBA_CMD57	800PT	1
58	FBA_CMD58	FBA_CMD58	800PT	1
59	FBA_CMD59	FBA_CMD59	800PT	1
60	FBA_CMD60	FBA_CMD60	800PT	1
61	FBA_CMD61	FBA_CMD61	800PT	1
62	FBA_CMD62	FBA_CMD62	800PT	1
63	FBA_CMD63	FBA_CMD63	800PT	1
64	FBA_CMD64	FBA_CMD64	800PT	1
65	FBA_CMD65	FBA_CMD65	800PT	1
66	FBA_CMD66	FBA_CMD66	800PT	1
67	FBA_CMD67	FBA_CMD67	800PT	1
68	FBA_CMD68	FBA_CMD68	800PT	1
69	FBA_CMD69	FBA_CMD69	800PT	1
70	FBA_CMD70	FBA_CMD70	800PT	1
71	FBA_CMD71	FBA_CMD71	800PT	1
72	FBA_CMD72	FBA_CMD72	800PT	1
73	FBA_CMD73	FBA_CMD73	800PT	1
74	FBA_CMD74	FBA_CMD74	800PT	1
75	FBA_CMD75	FBA_CMD75	800PT	1
76	FBA_CMD76	FBA_CMD76	800PT	1
77	FBA_CMD77	FBA_CMD77	800PT	1
78	FBA_CMD78	FBA_CMD78	800PT	1
79	FBA_CMD79	FBA_CMD79	800PT	1
80	FBA_CMD80	FBA_CMD80	800PT	1
81	FBA_CMD81	FBA_CMD81	800PT	1
82	FBA_CMD82	FBA_CMD82	800PT	1
83	FBA_CMD83	FBA_CMD83	800PT	1
84	FBA_CMD84	FBA_CMD84	800PT	1
85	FBA_CMD85	FBA_CMD85	800PT	1
86	FBA_CMD86	FBA_CMD86	800PT	1
87	FBA_CMD87	FBA_CMD87	800PT	1
88	FBA_CMD88	FBA_CMD88	800PT	1
89	FBA_CMD89	FBA_CMD89	800PT	1
90	FBA_CMD90	FBA_CMD90	800PT	1
91	FBA_CMD91	FBA_CMD91	800PT	1
92	FBA_CMD92	FBA_CMD92	800PT	1
93	FBA_CMD93	FBA_CMD93	800PT	1
94	FBA_CMD94	FBA_CMD94	800PT	1
95	FBA_CMD95	FBA_CMD95	800PT	1
96	FBA_CMD96	FBA_CMD96	800PT	1
97	FBA_CMD97	FBA_CMD97	800PT	1
98	FBA_CMD98	FBA_CMD98	800PT	1
99	FBA_CMD99	FBA_CMD99	800PT	1
100	FBA_CMD100	FBA_CMD100	800PT	1
101	FBA_CMD101	FBA_CMD101	800PT	1
102	FBA_CMD102	FBA_CMD102	800PT	1
103	FBA_CMD103	FBA_CMD103	800PT	1
104	FBA_CMD104	FBA_CMD104	800PT	1
105	FBA_CMD105	FBA_CMD105	800PT	1
106	FBA_CMD106	FBA_CMD106	800PT	1
107	FBA_CMD107	FBA_CMD107	800PT	1
108	FBA_CMD108	FBA_CMD108	800PT	1
109	FBA_CMD109	FBA_CMD109	800PT	1
110	FBA_CMD110	FBA_CMD110	800PT	1
111	FBA_CMD111	FBA_CMD111	800PT	1
112	FBA_CMD112	FBA_CMD112	800PT	1
113	FBA_CMD113	FBA_CMD113	800PT	1
114	FBA_CMD114	FBA_CMD114	800PT	1
115	FBA_CMD115	FBA_CMD115	800PT	1
116	FBA_CMD116	FBA_CMD116	800PT	1
117	FBA_CMD117	FBA_CMD117	800PT	1
118	FBA_CMD118	FBA_CMD118	800PT	1
119	FBA_CMD119	FBA_CMD119	800PT	1
120	FBA_CMD120	FBA_CMD120	800PT	1
121	FBA_CMD121	FBA_CMD121	800PT	1
122	FBA_CMD122	FBA_CMD122	800PT	1
123	FBA_CMD123	FBA_CMD123	800PT	1
124	FBA_CMD124	FBA_CMD124	800PT	1
125	FBA_CMD125	FBA_CMD125	800PT	1
126	FBA_CMD126	FBA_CMD126	800PT	1
127	FBA_CMD127	FBA_CMD127	800PT	1
128	FBA_CMD128	FBA_CMD128	800PT	1
129	FBA_CMD129	FBA_CMD129	800PT	1
130	FBA_CMD130	FBA_CMD130	800PT	1
131	FBA_CMD131	FBA_CMD131	800PT	1
132	FBA_CMD132	FBA_CMD132	800PT	1
133	FBA_CMD133	FBA_CMD133	800PT	1
134	FBA_CMD134	FBA_CMD134	800PT	1
135	FBA_CMD135	FBA_CMD135	800PT	1
136	FBA_CMD136	FBA_CMD136	800PT	1

Termination for Sub-Partition and CLK MUST BE PLACED as close as possible to the BGA memory on the line BEFORE the MEMORY pin! Minimize the stub length!

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN

600-10727-base-sch A

ID

PAGE

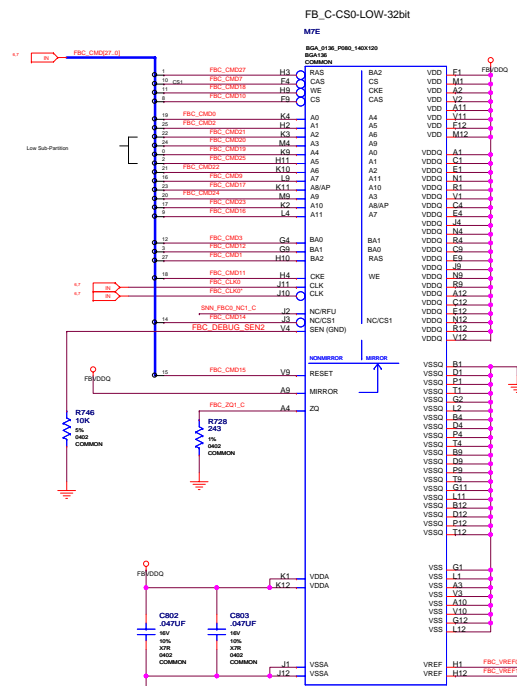
NAME

DATE

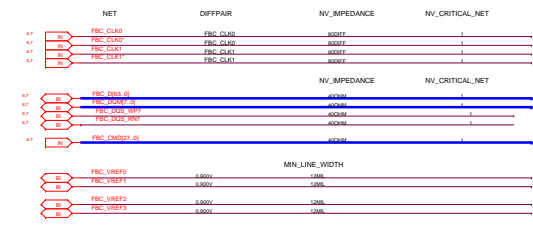
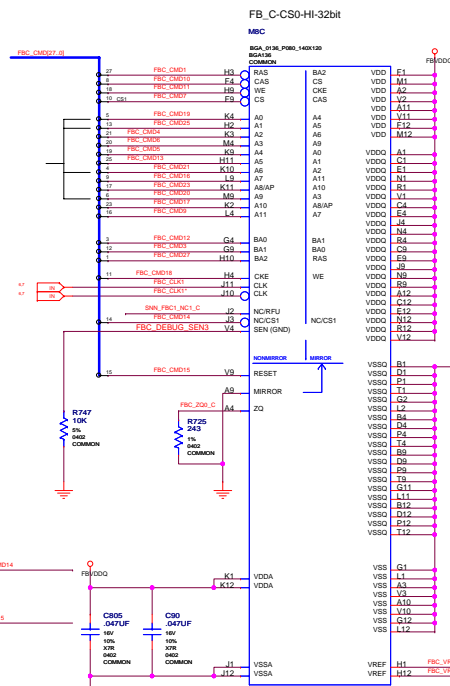
31-OCT-2007

ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO STUFF ASSEMBLY NOTES AND BOARD NOT FINAL
PAGE DETAIL: FBA 16/32Mx32 GDDR3 MEMORIES; FBA COMMAND BUS P0/FBA CLK TERMS

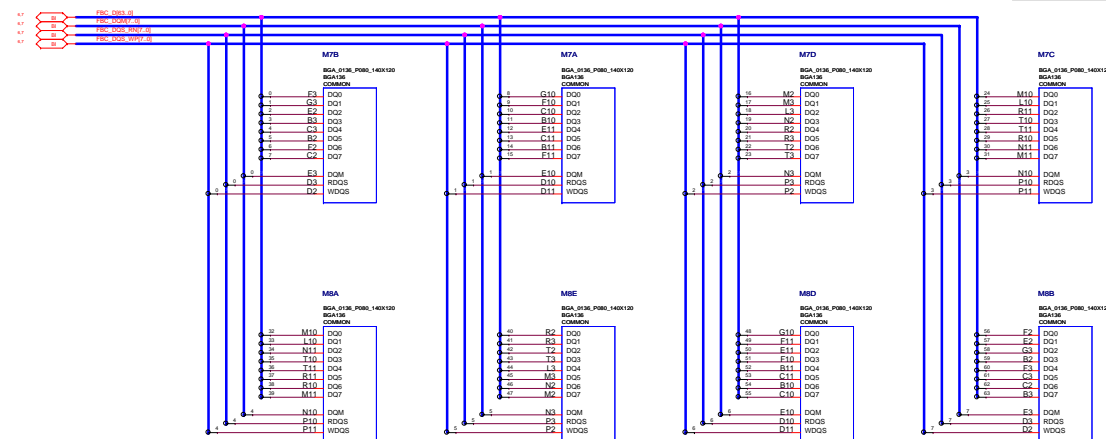
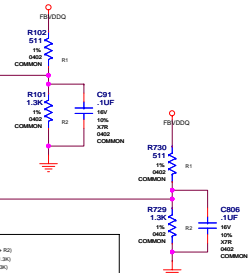
FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3



FBC Partition			CSD
CMD	ADDR		
CMD01	R40*		
CMD02	C40*		
CMD11	WE*		
CMD18	CKE		
CMD19	RESET/ODT		
CMD6	CS0*		
CMD19	A0-0		
CMD05	A0-1		
CMD04	A0-2	} Low Sub-Partition	
CMD04	A0-3		
CMD03	A0-4		
CMD3	A0-5		
CMD4	A0-6	} H0 Sub-Partition	
CMD6	A0-6		
CMD6	A0-6		
CMD5	A0-6		
CMD13	A0-6		
CMD21	A0-6		
CMD16	A0-7		
CMD23	A0-8		
CMD20	A0-9		
CMD17	A0-10		
CMD9	A0-11		
CMD14	A0-12		
CMD12	BA0		
CMD3	BA1		
CMD27	BA2		



Termination for Sub-Partition and CLK
MUST BE PLACED as close as possible to
the BGA memory on the line BEFORE the
MEMORY pin!!
Minimize the stub length!!



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS P/U'S, FBC CLK TERMS

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95060, USA



NV_PN	600-10727-base-sch A
-------	----------------------

ID		PAGE	
NAME		DATE	31-OCT-2007

1



3

5

NV_PN	600-10727-base-sch A
-------	----------------------

NV_PN	600-10727-base-sch A
-------	----------------------

ID		PAGE	
NAME		DATE	31-OCT-2007

[illegible]