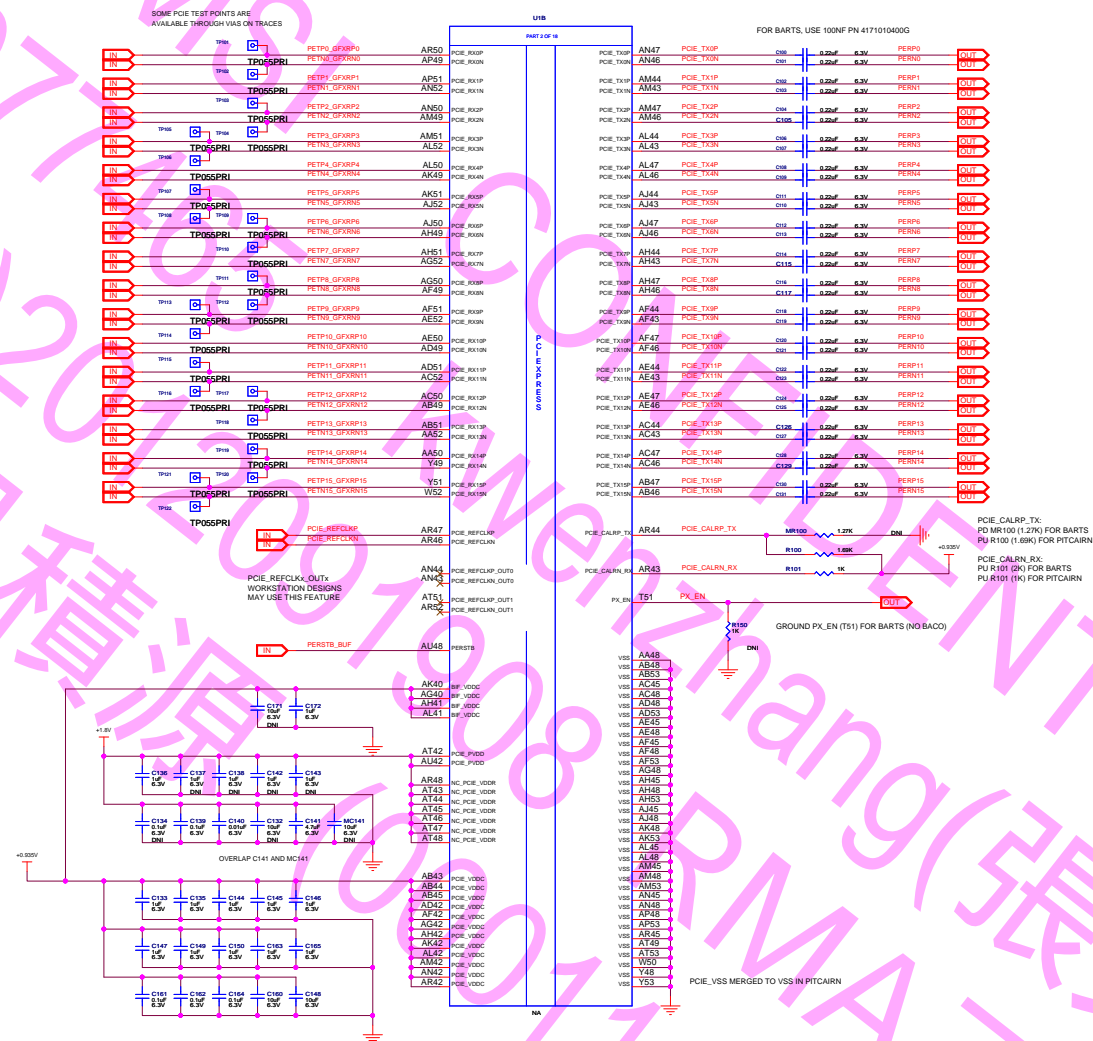
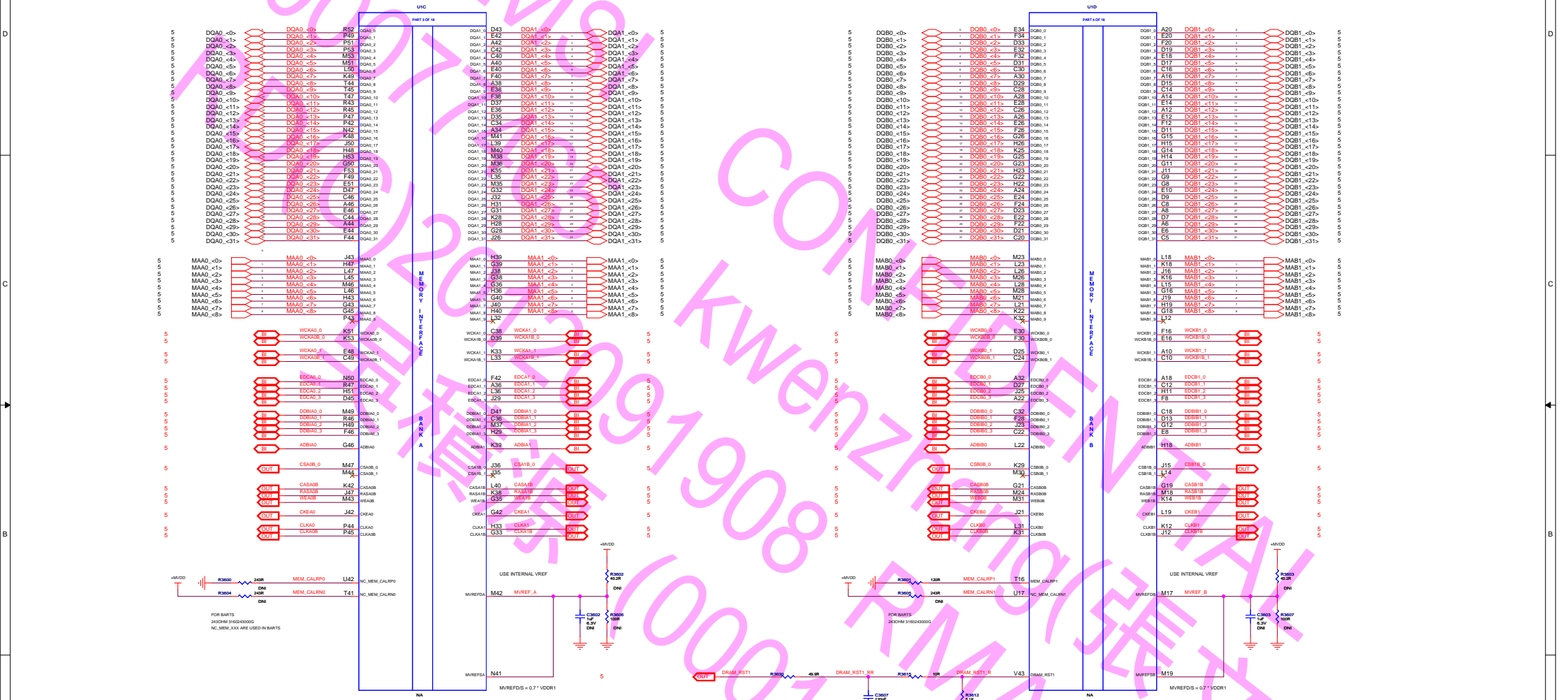


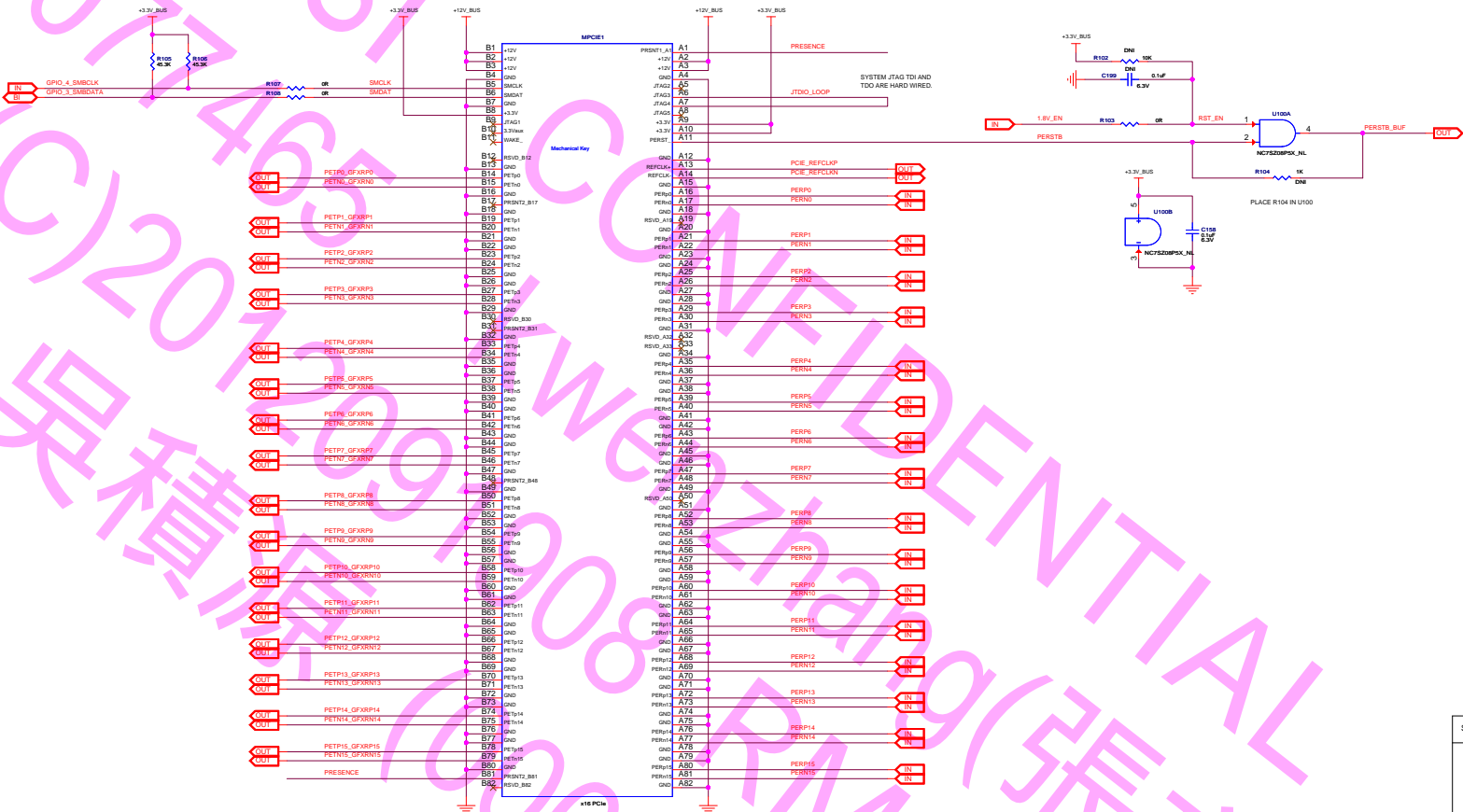
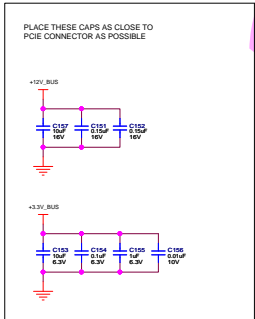
(2) PITCAIRN PCIE INTERFACE



(3) PITCAIRN MEM INTERFACE CH AB



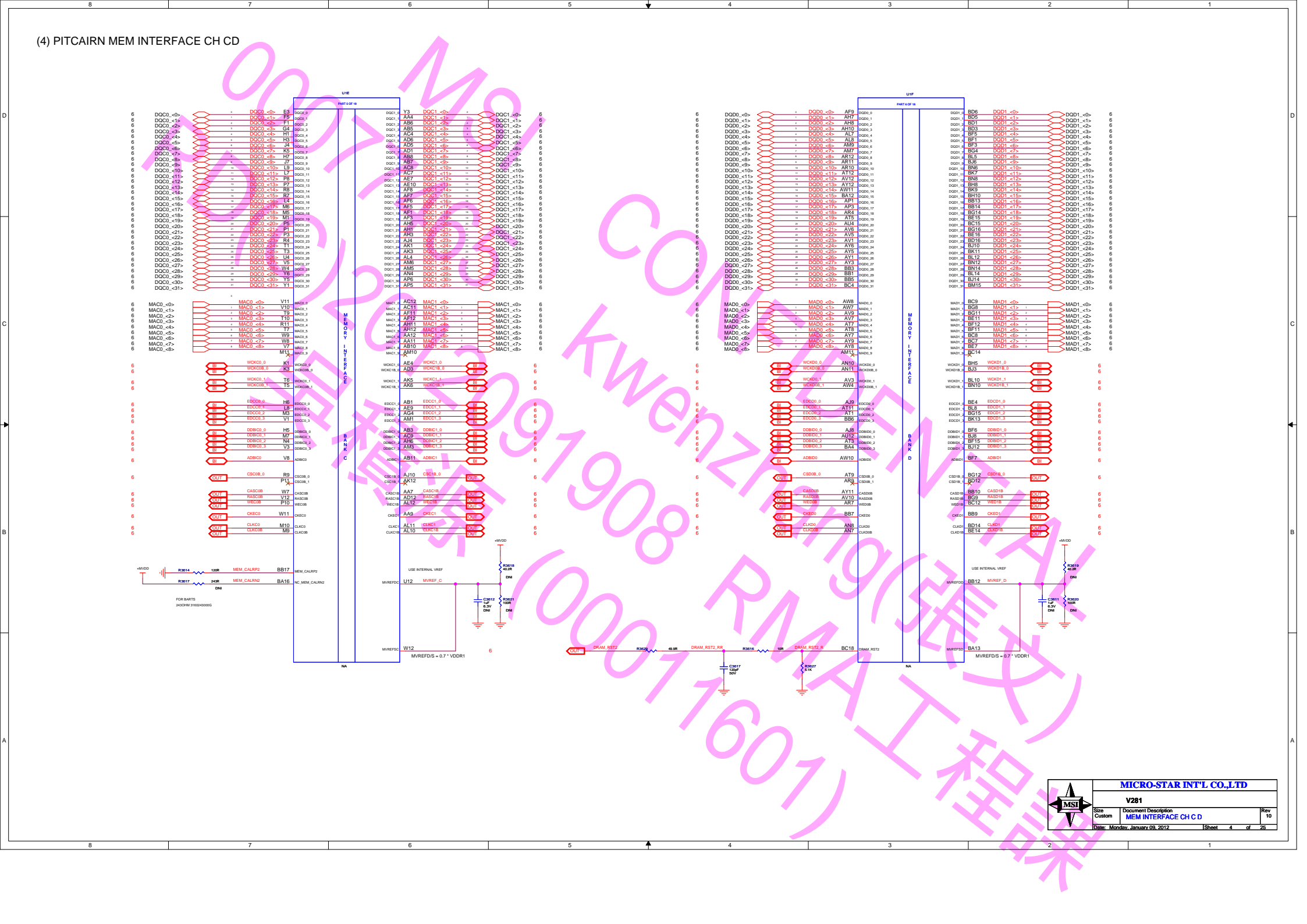
(1) PCI-EXPRESS EDGE CONNECTOR



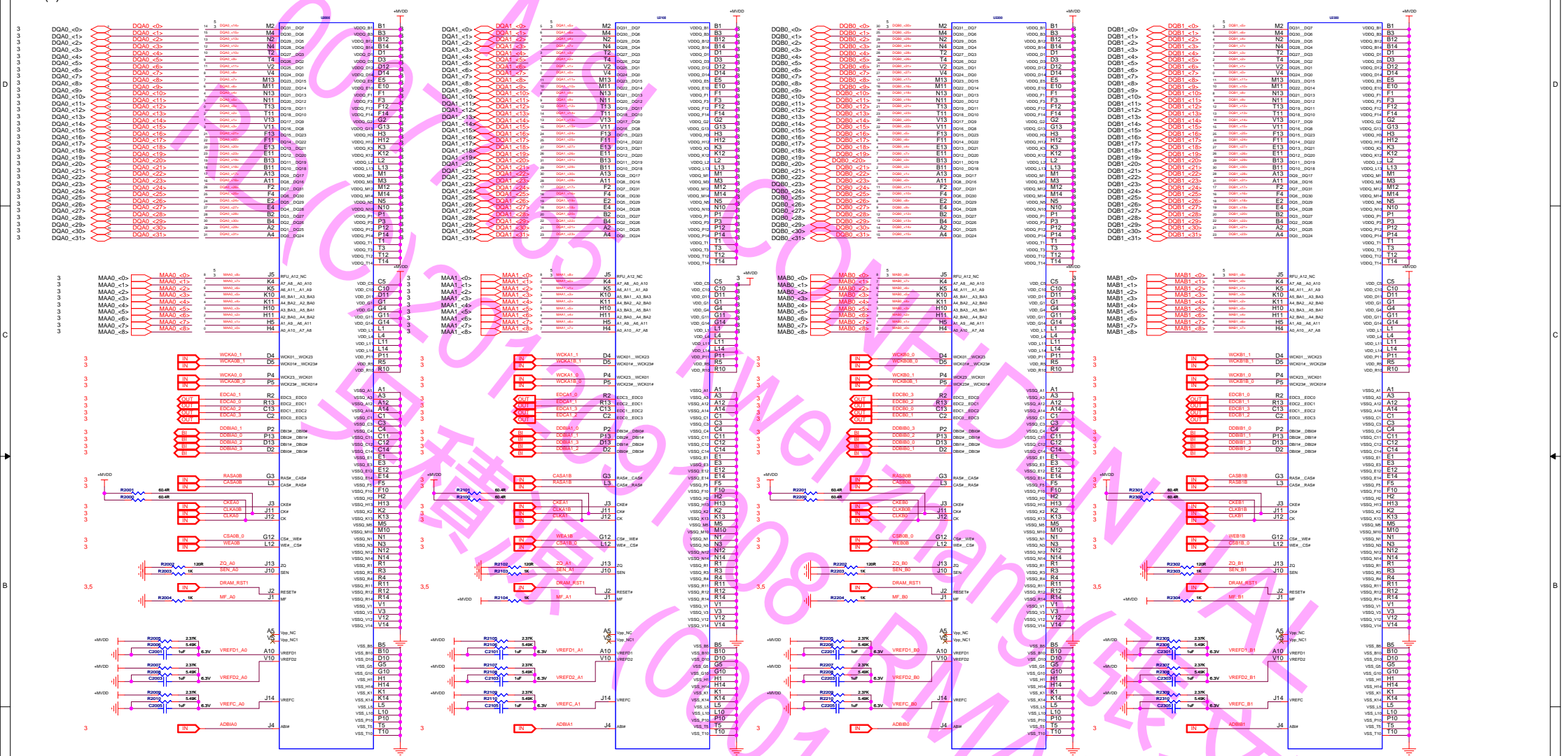
SYMBOL LEGEND	
DNI	DO NOT INSTALL
b or #	ACTIVE LOW
BUG	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

		MICRO-STAR INT'L CO.,LTD	
MIS-V281		Rev 10	
Size	Custom	Document Description	01 PCI-EXPRESS
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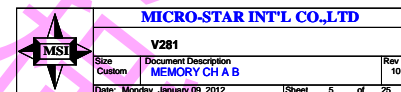
(4) PITCAIRN MEM INTERFACE CH C D



(5) GDDR5 MEMORY CH AB



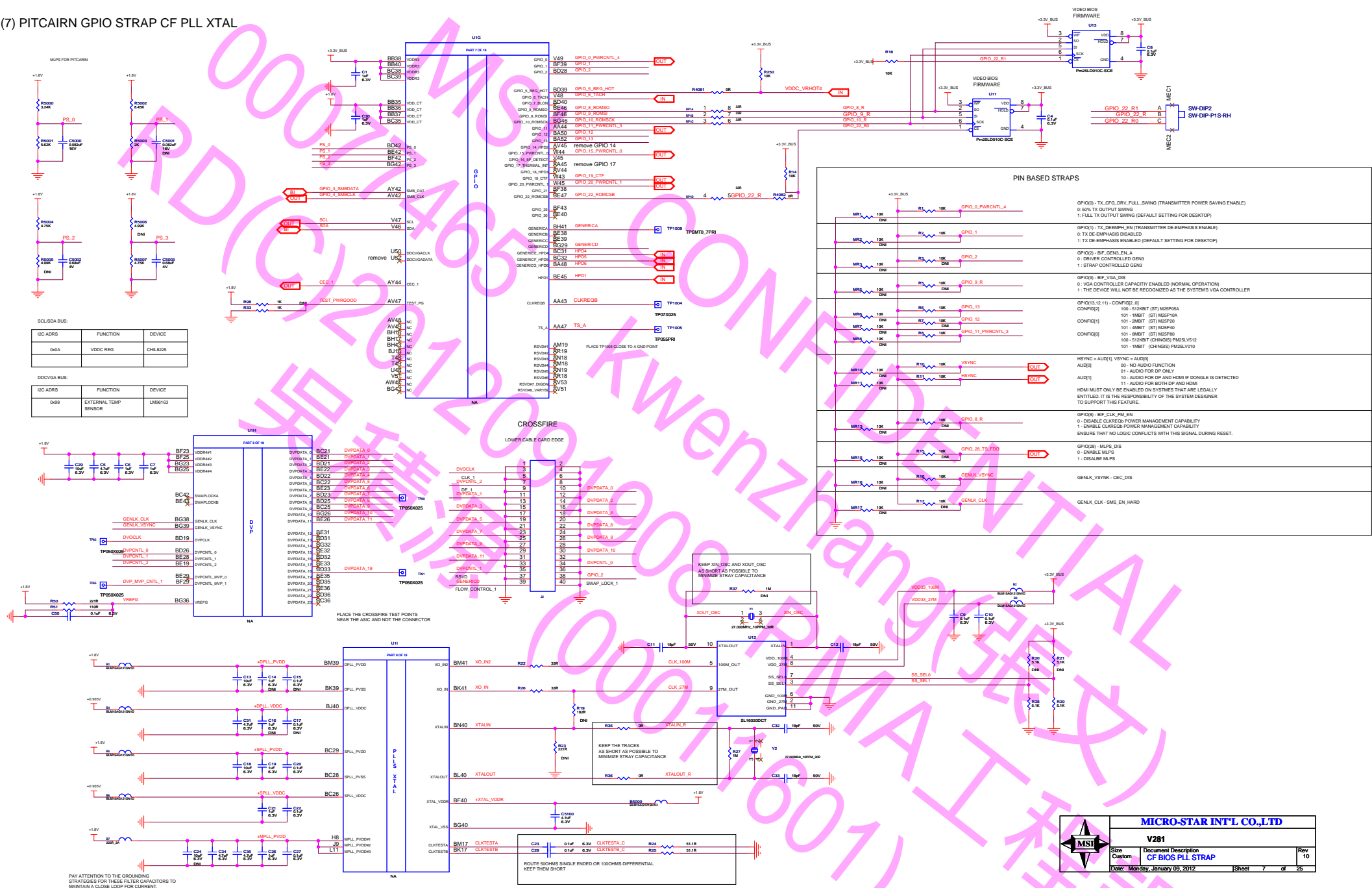
DRAM SCAN PINS
SSH [J2] - SCAN SHIFT
SCK [G12] - SCAN CLOCK
SOUT [C2] - SCAN OUTPUT
SEN [J10] - SCAN ENABLE
SOE# [J1] - SCAN OUTPUT ENABLI

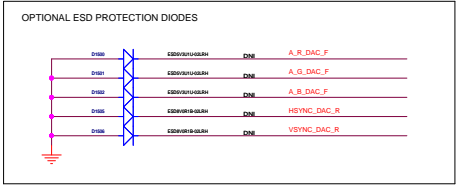
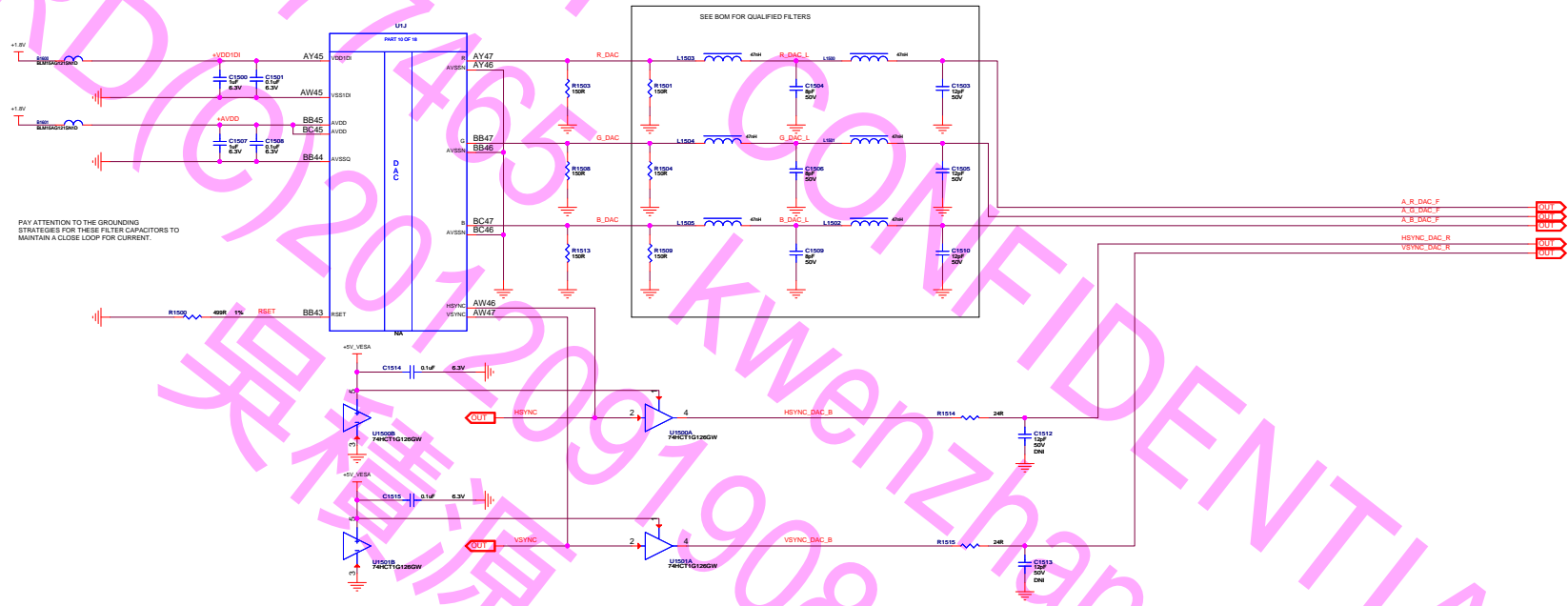


(6) GDDR5 MEMORY CH CD



(7) PITCAIRN GPIO STRAP CF PLL XTAL



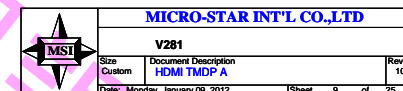
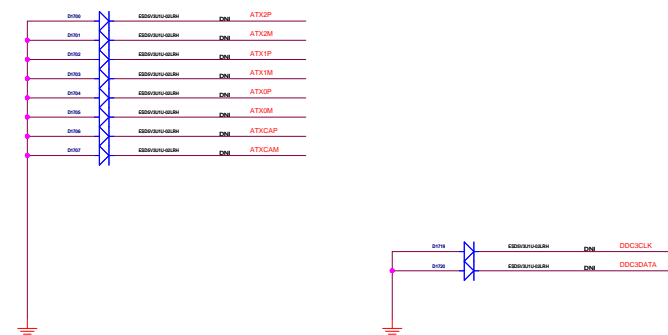


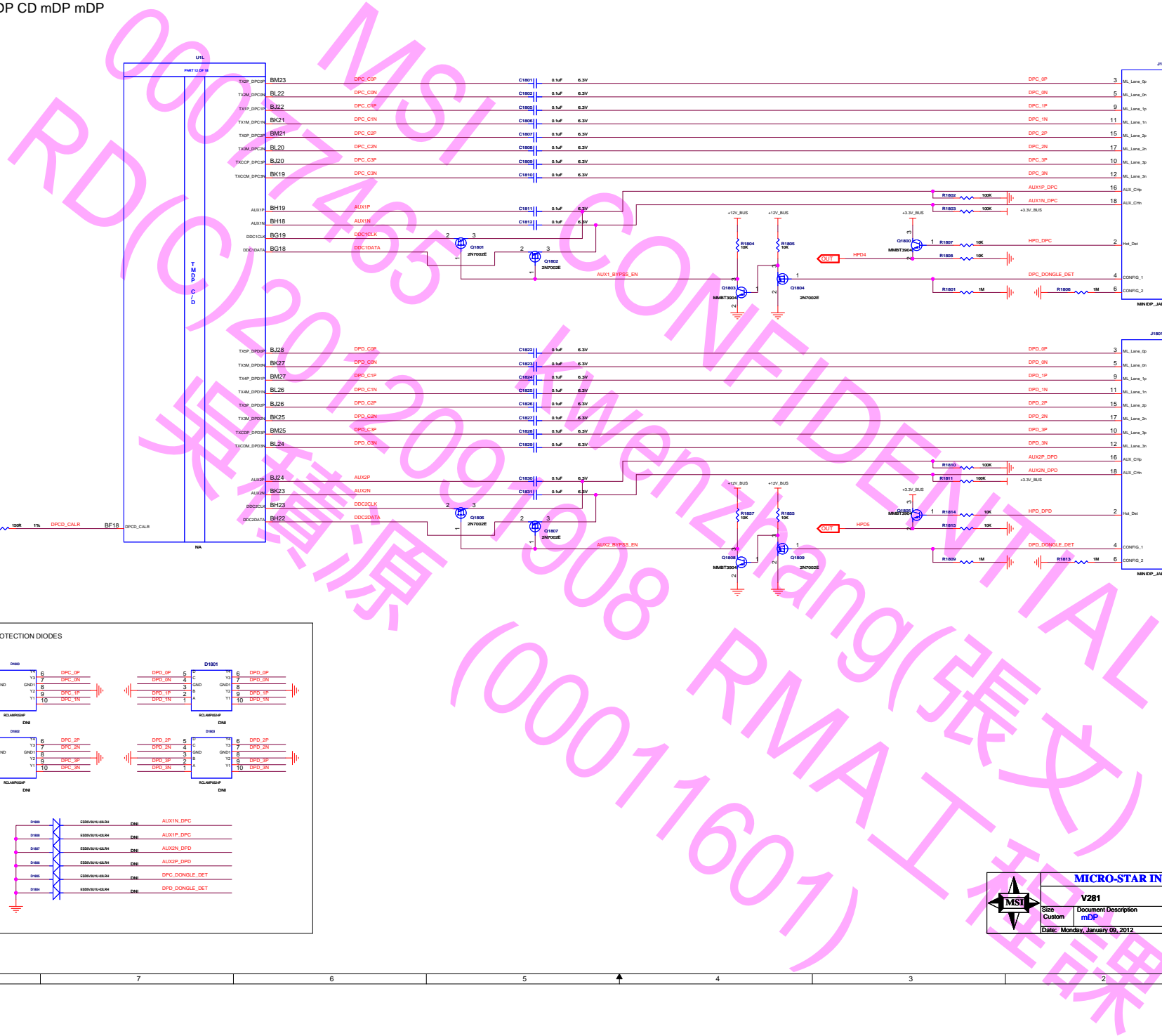
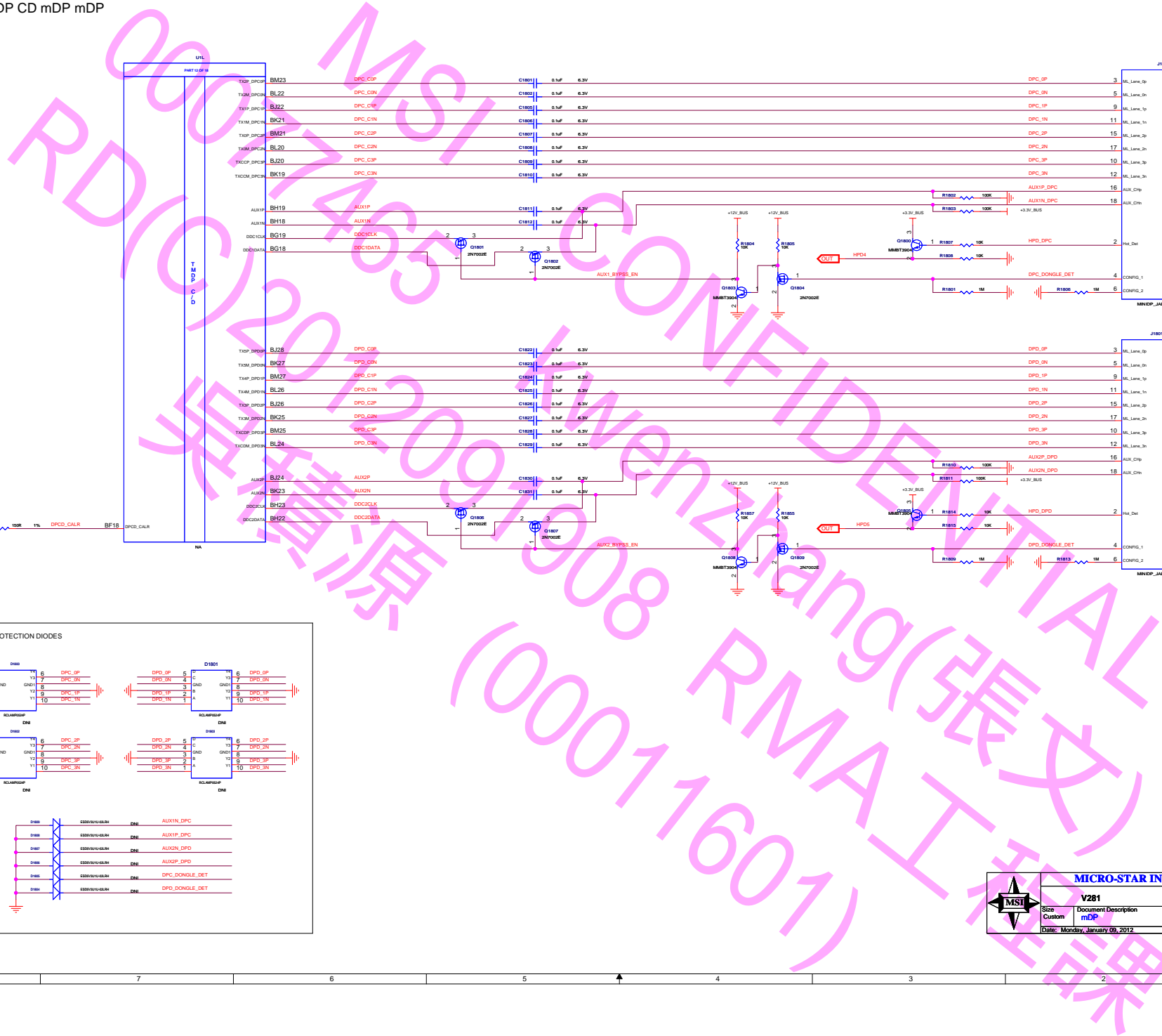
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	V281		
	Size	Document Description	Rev
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Date: Monday, January 09, 2012			Sheet 08 of 25

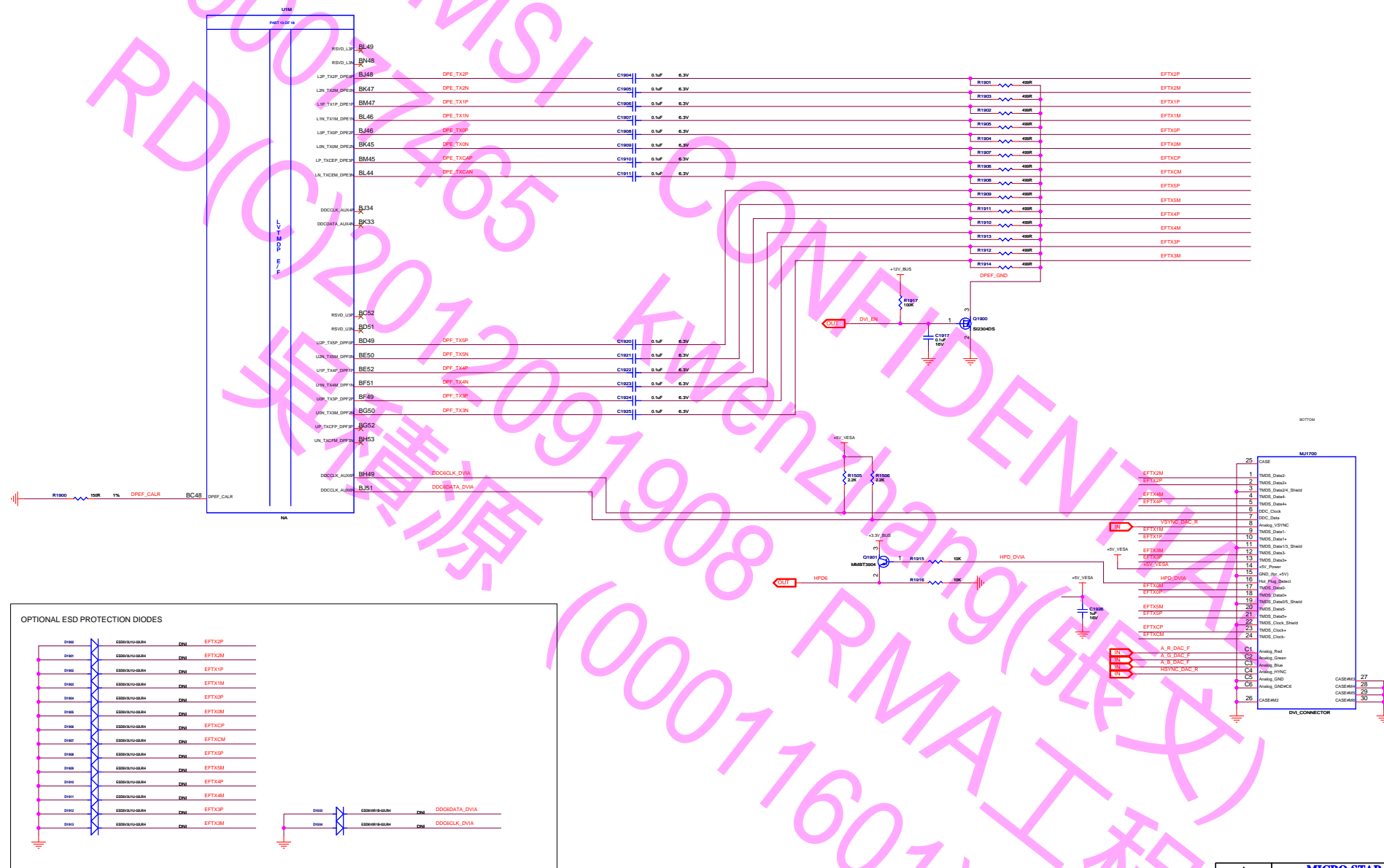
(9) PITCAIRN TMDP AB HDMI sDVI



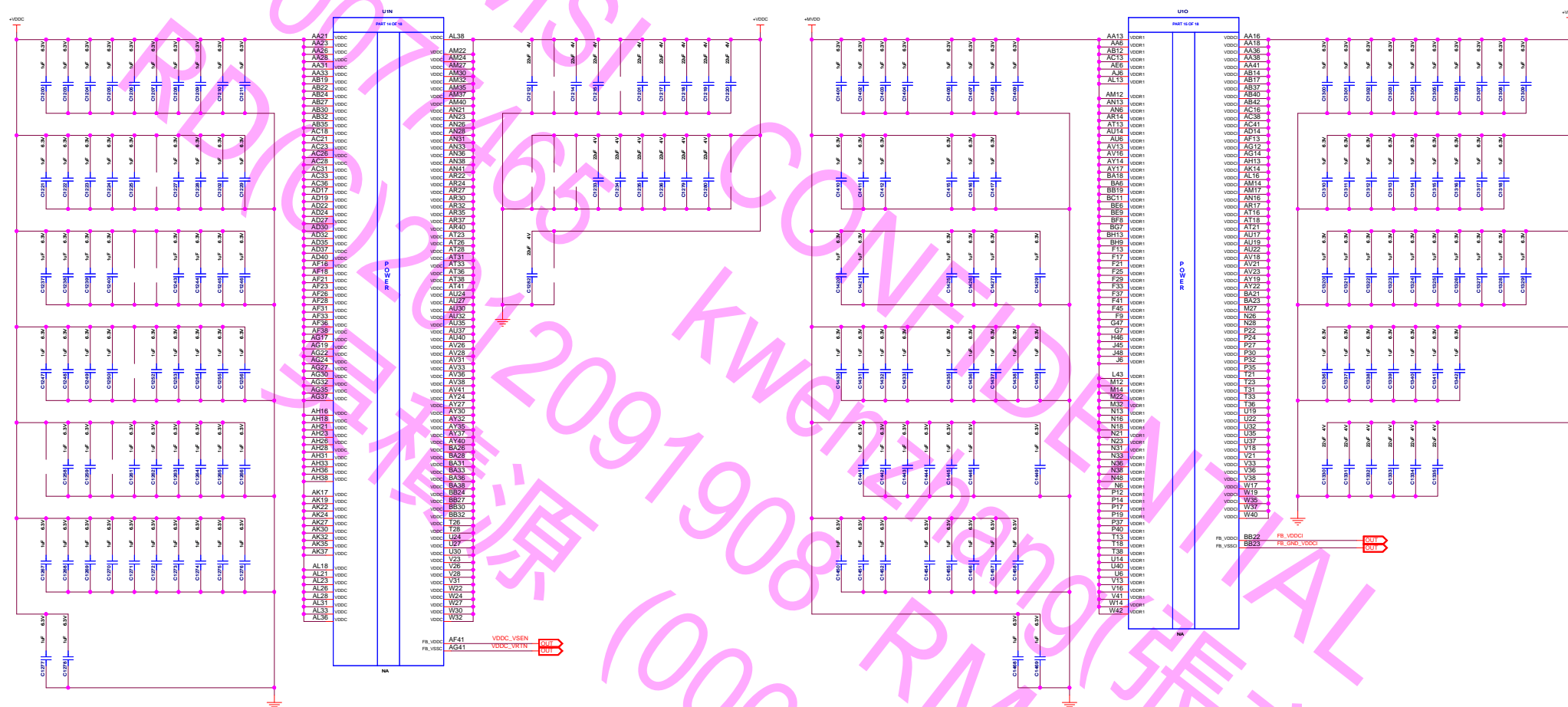
OPTIONAL ESD PROTECTION DIODES








(12) PITCAIRN POWER



U1P		U1Q	
PART 16 OF 16		PART 17 OF 16	
A46	VS	BA17	VS
AA10	VS	BA18	VS
AA14	VS	BA2	VS
AA17	VS	BA20	VS
AA19	VS	BA21	VS
AA2	VS	BA27	VS
AA22	VS	BA30	VS
AA24	VS	BA32	VS
AA27	VS	BA33	VS
AA30	VS	BA35	VS
AA32	VS	BA37	VS
AA33	VS	BA40	VS
AA37	VS	BA41	VS
AA40	VS	BB1	VS
AA42	VS	BB10	VS
AA5	VS	BB16	VS
AB13	VS	BB21	VS
AB16	VS	BB26	VS
AB18	VS	BB31	VS
AB21	VS	BB33	VS
AB23	VS	BB40	VS
AB26	VS	BB41	VS
AB28	VS	BB5	VS
AB31	VS	BB53	VS
AB33	VS	BB6	VS
AB36	VS	BC16	VS
AB38	VS	BC18	VS
AB41	VS	BC19	VS
AB5	VS	BC2	VS
AC10	VS	BC20	VS
AC14	VS	BC30	VS
AC17	VS	BC32	VS
AC18	VS	BC6	VS
AC2	VS	BD15	VS
AC22	VS	BD16	VS
AC24	VS	BD20	VS
AC27	VS	BD30	VS
AC30	VS	BE12	VS
AC32	VS	BE10	VS
AC35	VS	BE16	VS
AC37	VS	BE20	VS
AC40	VS	BE3	VS
AC42	VS	BF14	VS
AC5	VS	BF16	VS
AD13	VS	BF23	VS
AD16	VS	BF21	VS
AD18	VS	BF22	VS
AD21	VS	BF30	VS
AD23	VS	BF9	VS
AD26	VS	BG2	VS
AD28	VS	AT37	VS
AD31	VS	AT40	VS
AD33	VS	BH16	VS
AD36	VS	AU13	VS
AD38	VS	AU15	VS
AD41	VS	AU18	VS
AE1	VS	AU2	VS
AE2	VS	AU21	VS
AE3	VS	AU23	VS
AF10	VS	BU30	VS
AF14	VS	BU42	VS
AF17	VS	BU16	VS
AF19	VS	BU33	VS
AF22	VS	BU11	VS
AF24	VS	BU38	VS
AF27	VS	BM7	VS
AF30	VS	BM9	VS
AF32	VS	BN22	VS
AF35	VS	BN16	VS
AF37	VS	F10	VS
AF40	VS	F11	VS
AG13	VS	F14	VS
AG16	VS	F16	VS
AG18	VS	F18	VS
AG2	VS	AV24	VS
AG21	VS	P25	VS
AG23	VS	P27	VS
AG26	VS	P31	VS
AG28	VS	P30	VS
AG31	VS	P36	VS
AG33	VS	P38	VS
AG36	VS	P43	VS
AG38	VS	P47	VS
AG5	VS	F7	VS
AH14	VS	AW2	VS
AH17	VS	AW9	VS
AH19	VS	AW22	VS
AH22	VS	AW8	VS
AH24	VS	AW9	VS
AH27	VS	AY10	VS
AH30	VS	AY13	VS
AH32	VS	AY18	VS
AH37	VS	AY23	VS
AH40	VS	AY28	VS
AH6	VS	AY30	VS
AJ1	VS	AY31	VS
AJ2	VS	AY33	VS
AJ7	VS	AY36	VS
AK13	VS	AY38	VS
AK16	VS	AY40	VS
AK18	VS	AY44	VS
AK19	VS	AY48	VS
AK21	VS	AY49	VS
AK23	VS	B11	VS
AK26	VS	B13	VS
AK28	VS	B16	VS
AK31	VS	B17	VS
AK33	VS	B19	VS
AK36	VS	B21	VS
AK38	VS	B23	VS
AK41	VS	B26	VS
AL14	VS	B27	VS
AL17	VS	B29	VS
AL19	VS	B31	VS
AL2	VS	B33	VS
AL22	VS	B36	VS
AL24	VS	B37	VS
AL27	VS	B39	VS
AL30	VS	B41	VS
AL32	VS	B43	VS
AL36	VS	B46	VS
AL37	VS	B47	VS
AL40	VS	B7	VS
AL6	VS	B9	VS
AL9	VS	BA14	VS



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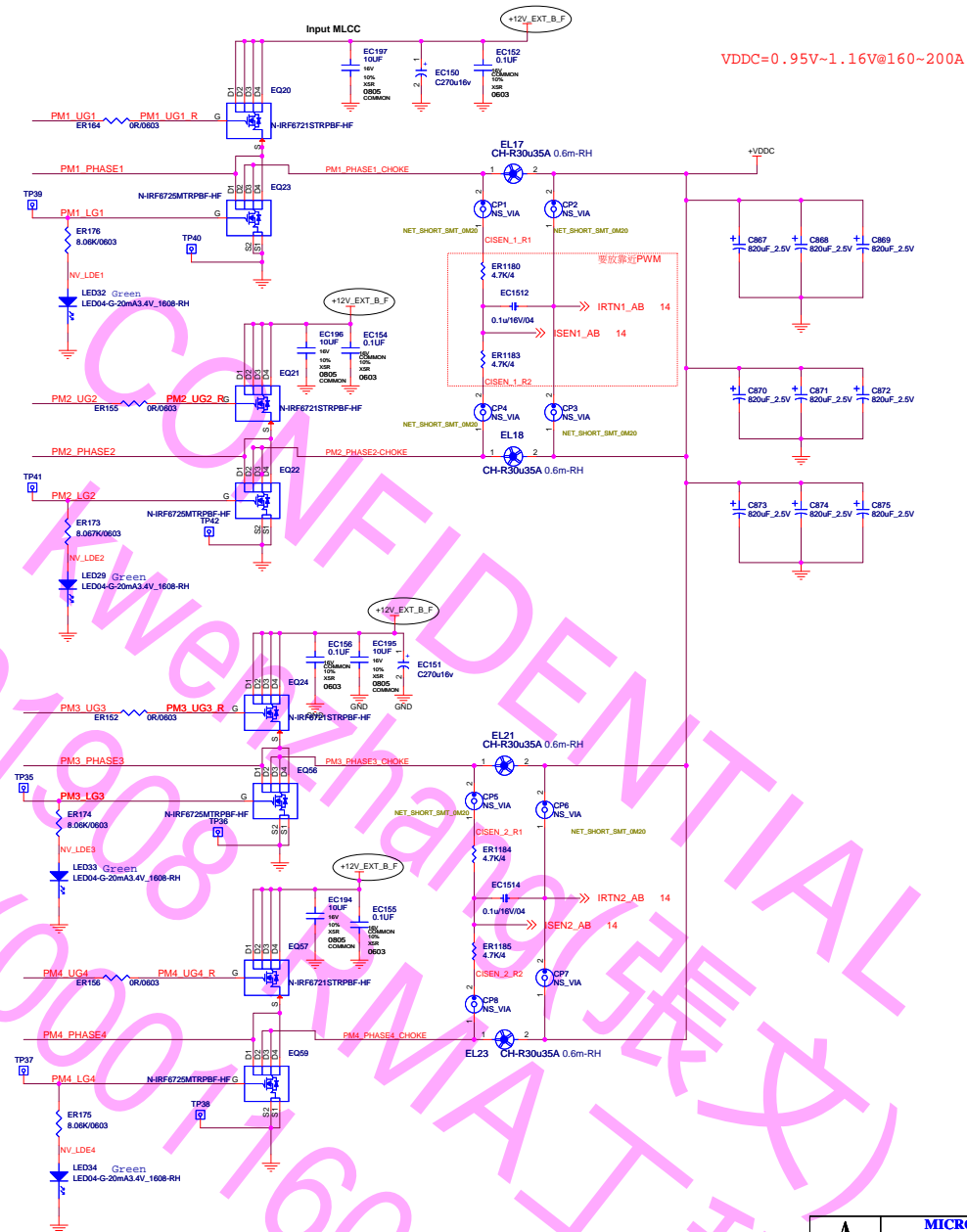
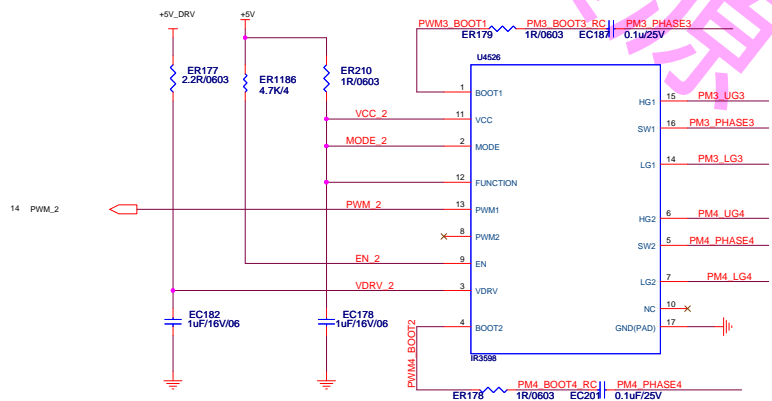
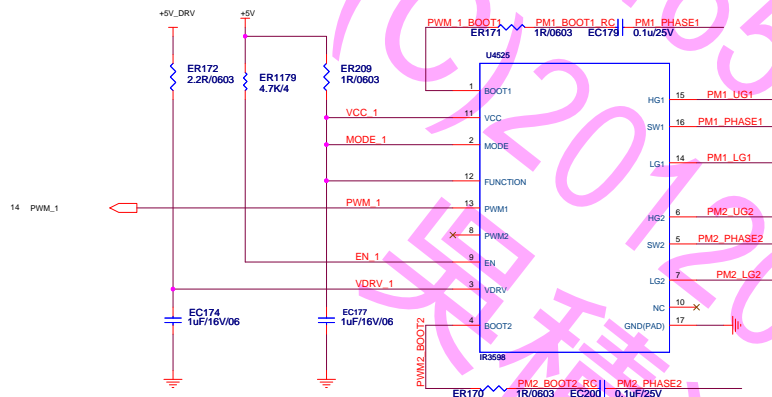
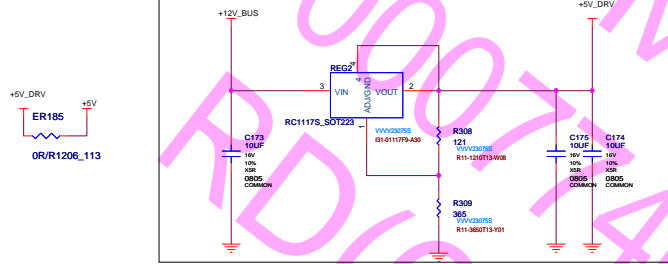
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Power Supply: VDDC PHASE 1,~4

5V POWER SUPPLY FOR DRIVER



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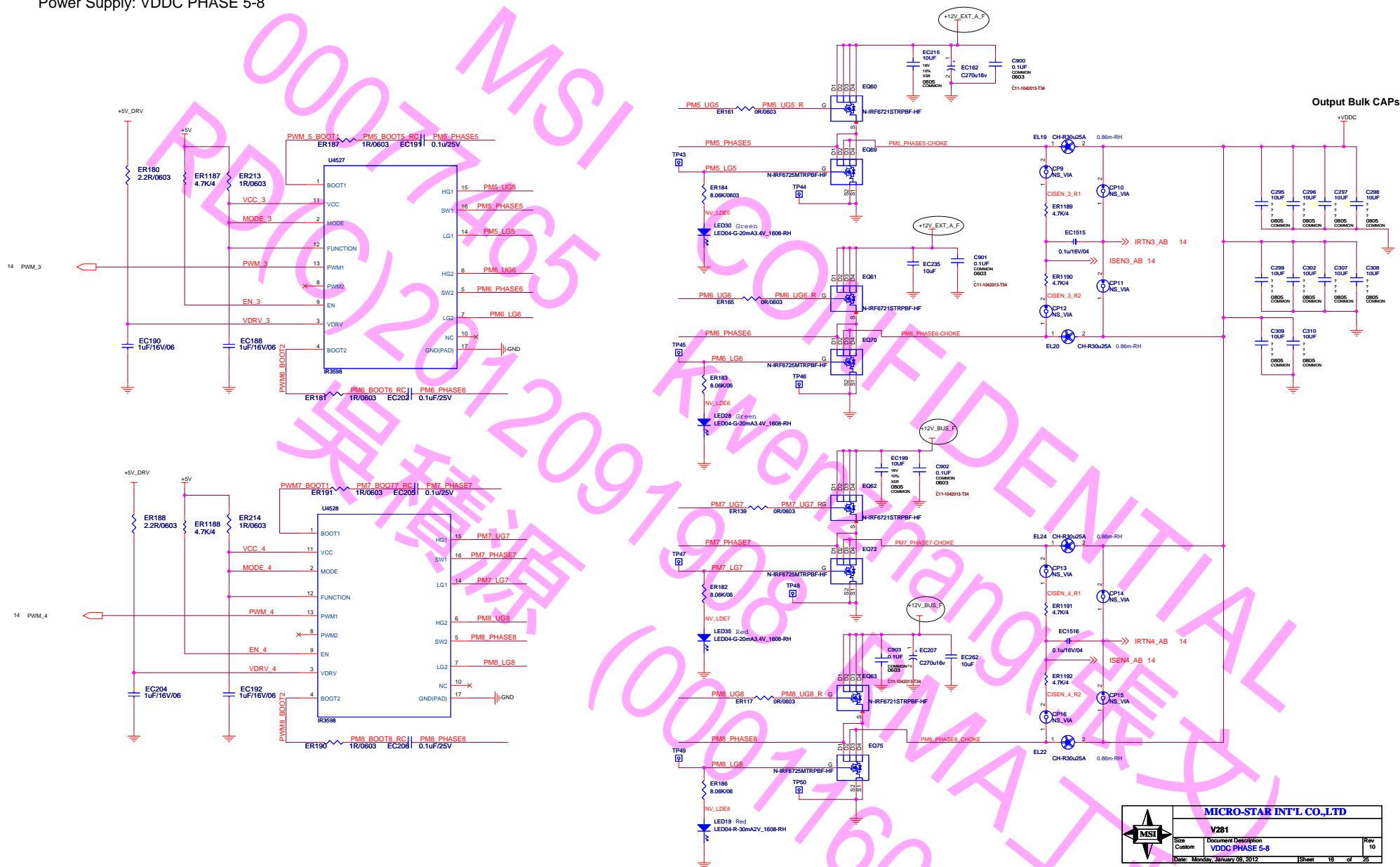
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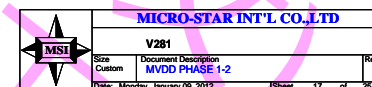
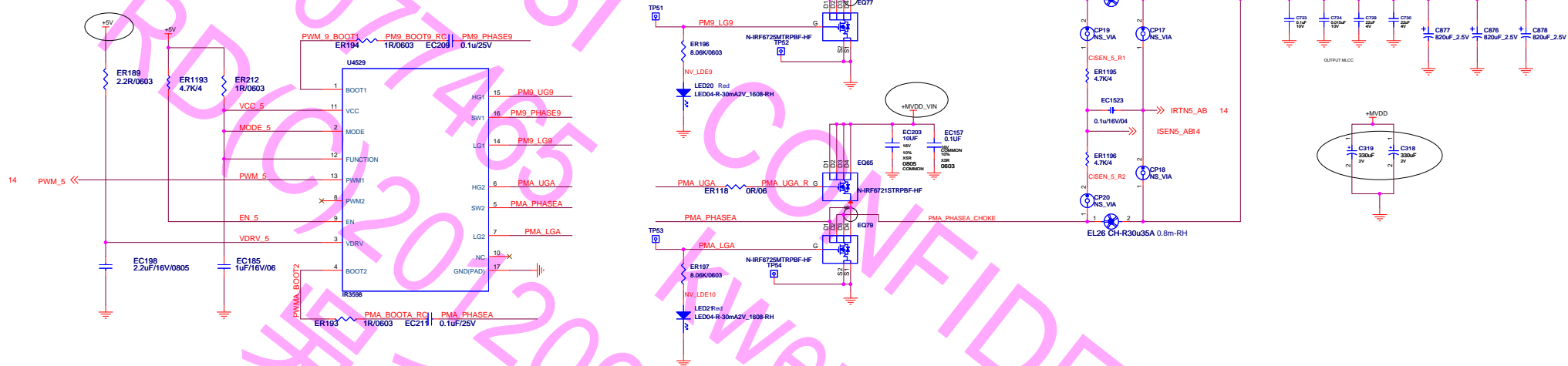
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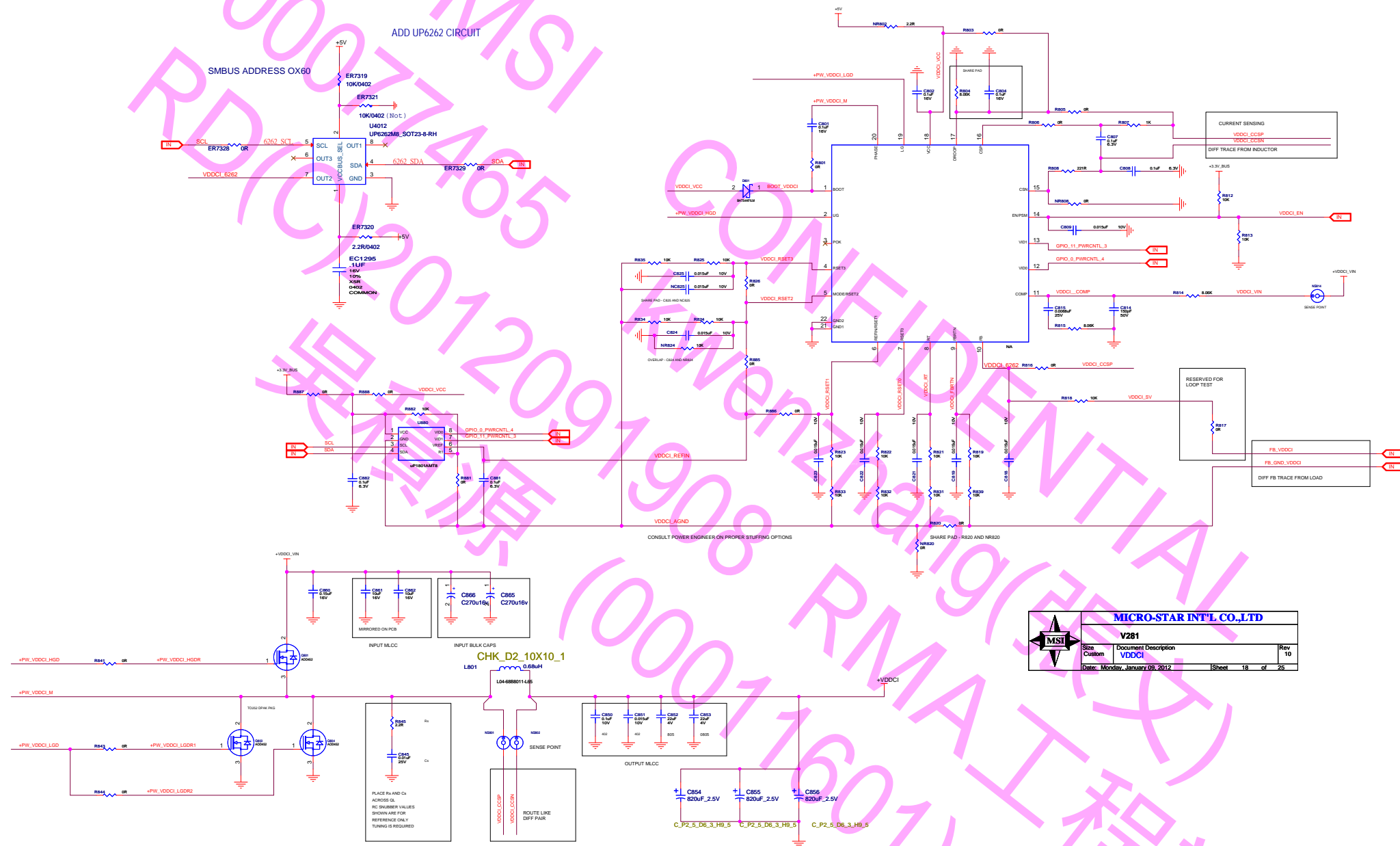
Date: Monday, January 09, 2012


Sheet

Power Supply: VDDC PHASE 5-8







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LAYOUT GUIDELINE

1. POSITION THE CONTROLLER (U703) SUCH THAT LGATE (PIN4) IS THE CLOSEST TO THE GATE OF THE MOSFETS. YOU CAN PLACE THE GATE RESISTORS R721 AND R722 NEXT TO THE GATE OF THE MOSFETS. MAKE THE GATE DRIVE TRACES (PIN_4, M2000, LG2000) AS SHORT AS POSSIBLE TO REDUCE THE TRACE INDUCTANCE.

2. PLACE THE BYPASS CAPACITORS FOR VCC (C703) AS WELL AS BOOST CAPS (C705) AS CLOSE TO THE CONTROLLER AS POSSIBLE.

3. VOLTAGE AMPLIFIER COMPENSATION NETWORK: PLACE R714 CLOSE TO THE PIN 7. PLACE THE REST OF THE COMPENSATION NETWORK (R716, R711, R712, R713, C711, C712 AND C713) CLOSE TO THE PINS 7 AND 6.

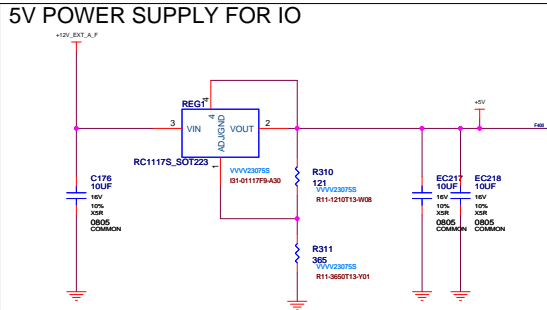
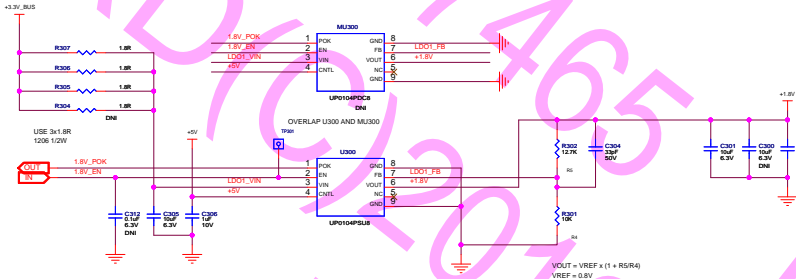


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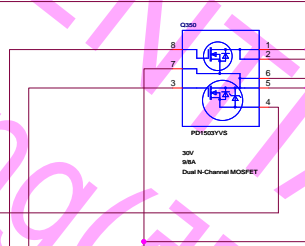
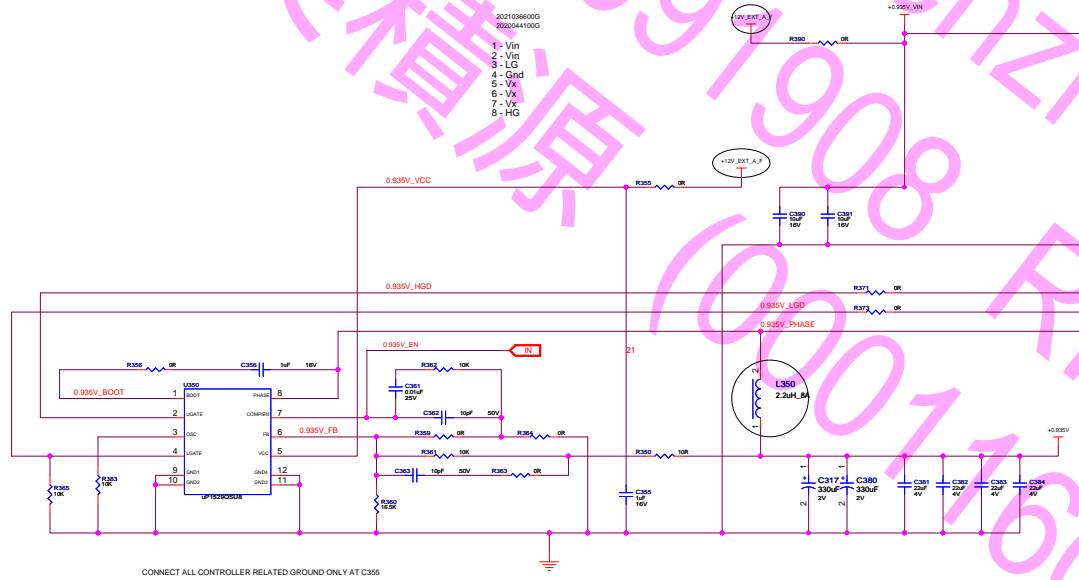
(17) SMALL RAIL REGULATOR

LDO #1: VIN = 3.0V TO 3.6V MAX VOUT = +1.8V +/-2% IOUT = 1.3A RMS MAX
PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING

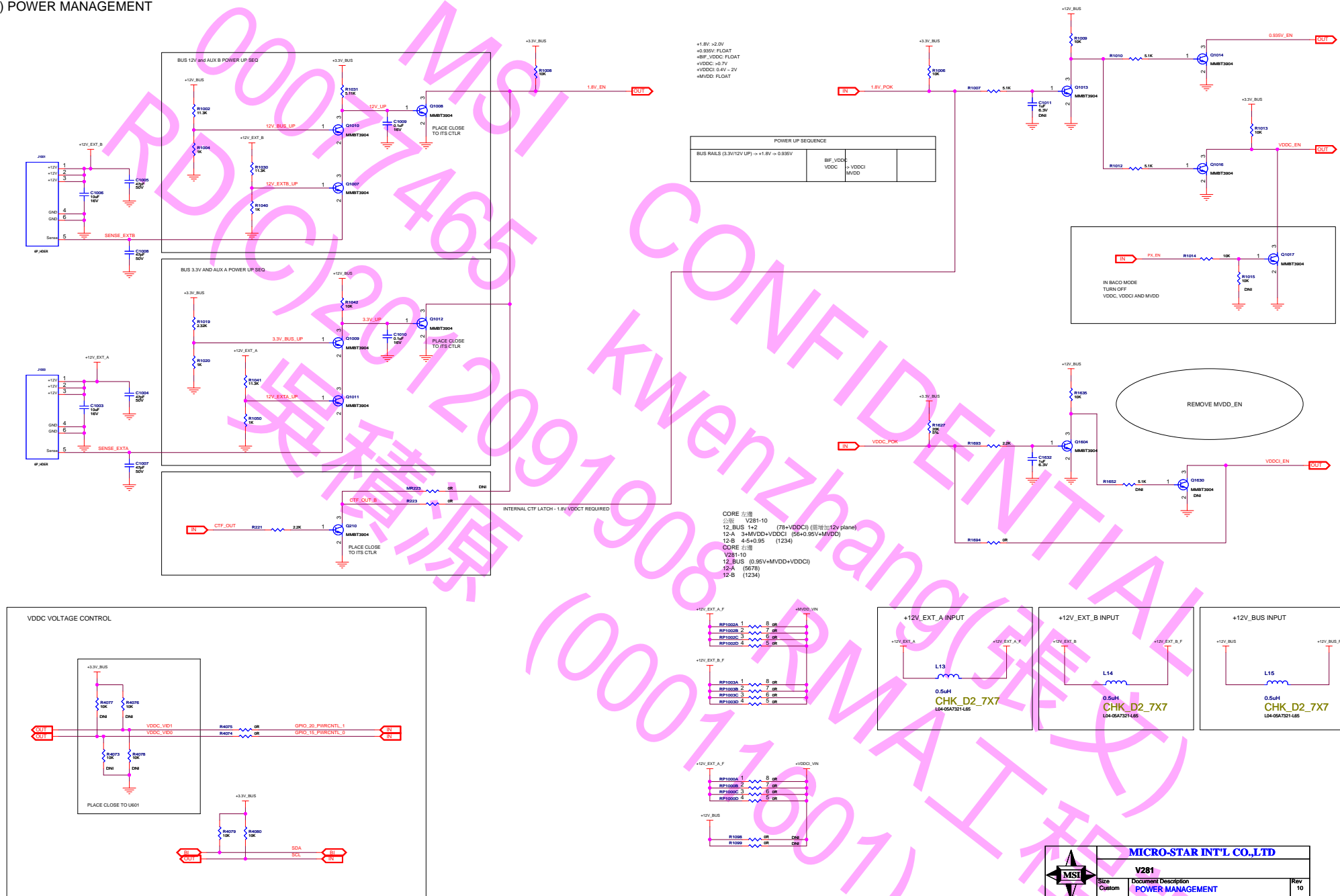
REGULATOR FOR +5V RAILS
IOUT MAX = 150mA



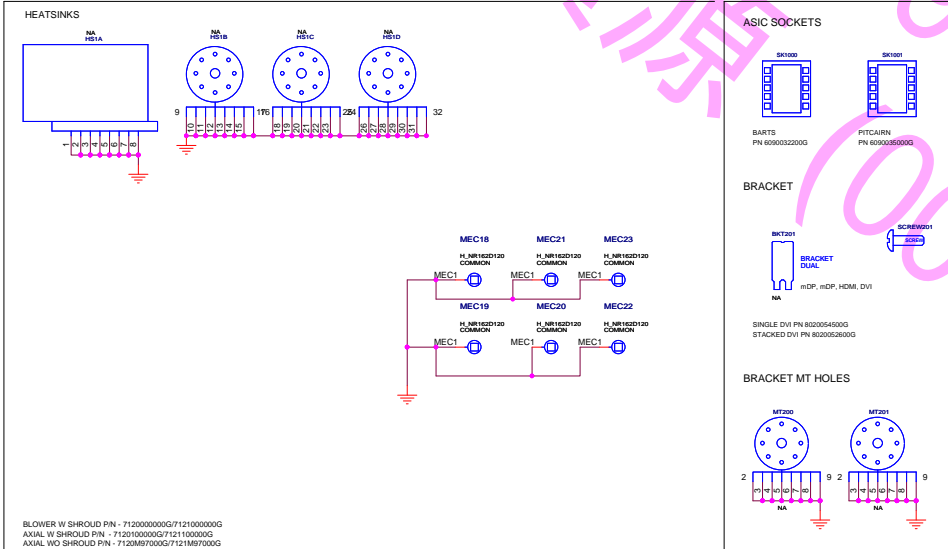
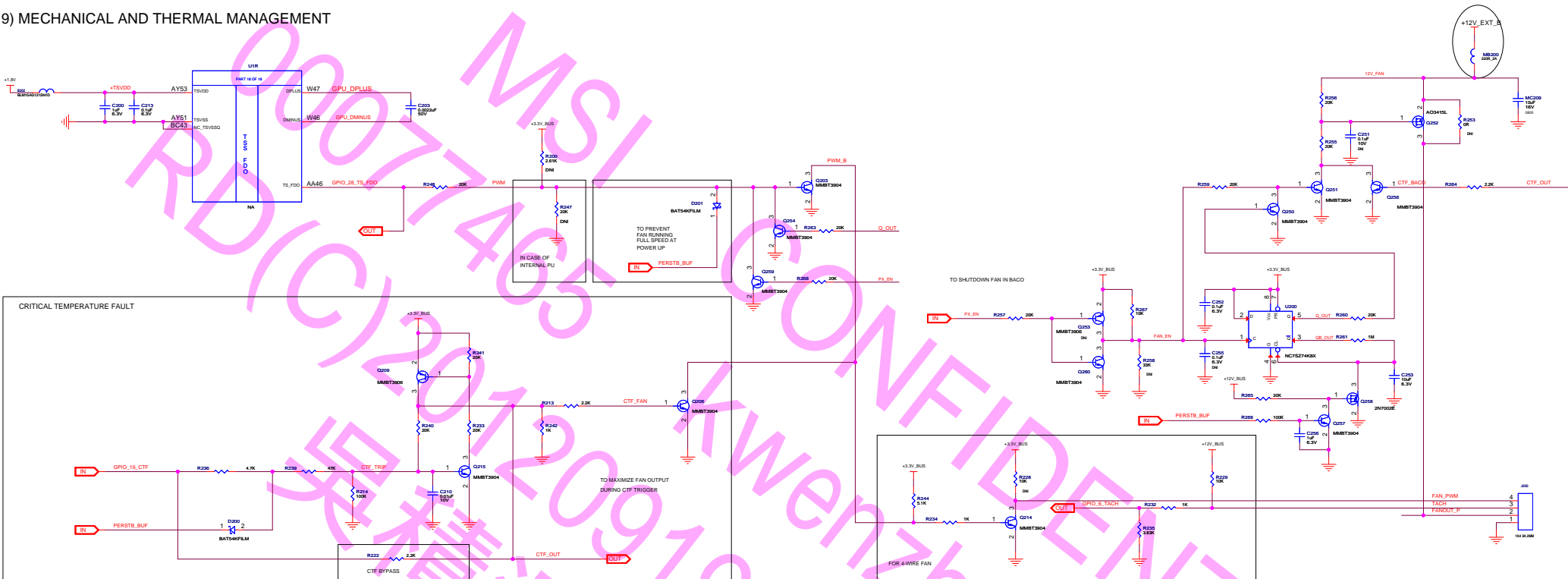
0.935V REGULATOR



(18) POWER MANAGEMENT



(19) MECHANICAL AND THERMAL MANAGEMENT



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AMD



TITLE:

Pitcairn GDDR5 x32

DOCUMENT NUMBER:

105-C401xx-00

DATE:

Wed Dec 21 19:16:58 2011

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NOTES:

NOTE

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1 Commerce Valley Drive East
Markham, ON L3T 7X6

SCH Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	10/26/2011	INITIAL DESIGN BASED ON CHAS FITZGERALD TRENAL LAYOUT
1	00B	10/26/2011	LAYOUT INCREASE SPACING BETWEEN BGA AND JANE
2	00C	10/11/2011	UPDATE FANBOARD CIRCULARITY LAYOUT SERVICE DISPLAY SETTINGS
3	00	10/10/2011	ADD FAN BOARD ADDRESS B3 INPUT OPTION FOR 0.880 BGA ADD BGA1-BGA8, RING, COT

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(20) DEBUG CIRCUIT

