

NV20, 4MX16 DDR, RGB, EXTERNAL DVI-I, TV-DOWN, TV IF , AGP4X  
PCI DEVICE ID 0X0=0X200 FOR NV20.

NVVD SET TO: 1.52V  
FBVDD SET TO: 3.47V  
FBVDDQ SET TO: 2.59V

HISTORY REVISION:

X00: Based on P50-A06  
- See change list in 149- file.  
- Set FBVDDQ=2.59V


P50-A07-X01:  
- Changed all memory clk/clk# diff pair resistors to 68R 5% (from 47R)

P50-A08:  
X04: - Delay PLL\_VDD to come up after NVVD.  
X05: - Added 1UF across R257.  
X06: - Removed X04-5 above, added a switcher generated PLL delay option.  
- SSENNA cap for 2nd SW changed to 1UF.  
- A05 SI, NVVD=1.52V

P50-A09:  
X02: - Changed PLL VDD and DAC VDD to be gated by Fet controlled by FBVDD power good signal.  
X03: - Added option to pull up power good to 12V

ECO1235: - Changed R841 PU to 10K (from 4.7K)

ECO1373: - Moved 75 ohm termination closer to filter for noise level reduction.  
Replaced C303,306,309 with 75ohm and no stuffed R208-210.



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Doc C

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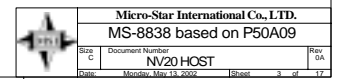
Monday, May 18, 2009

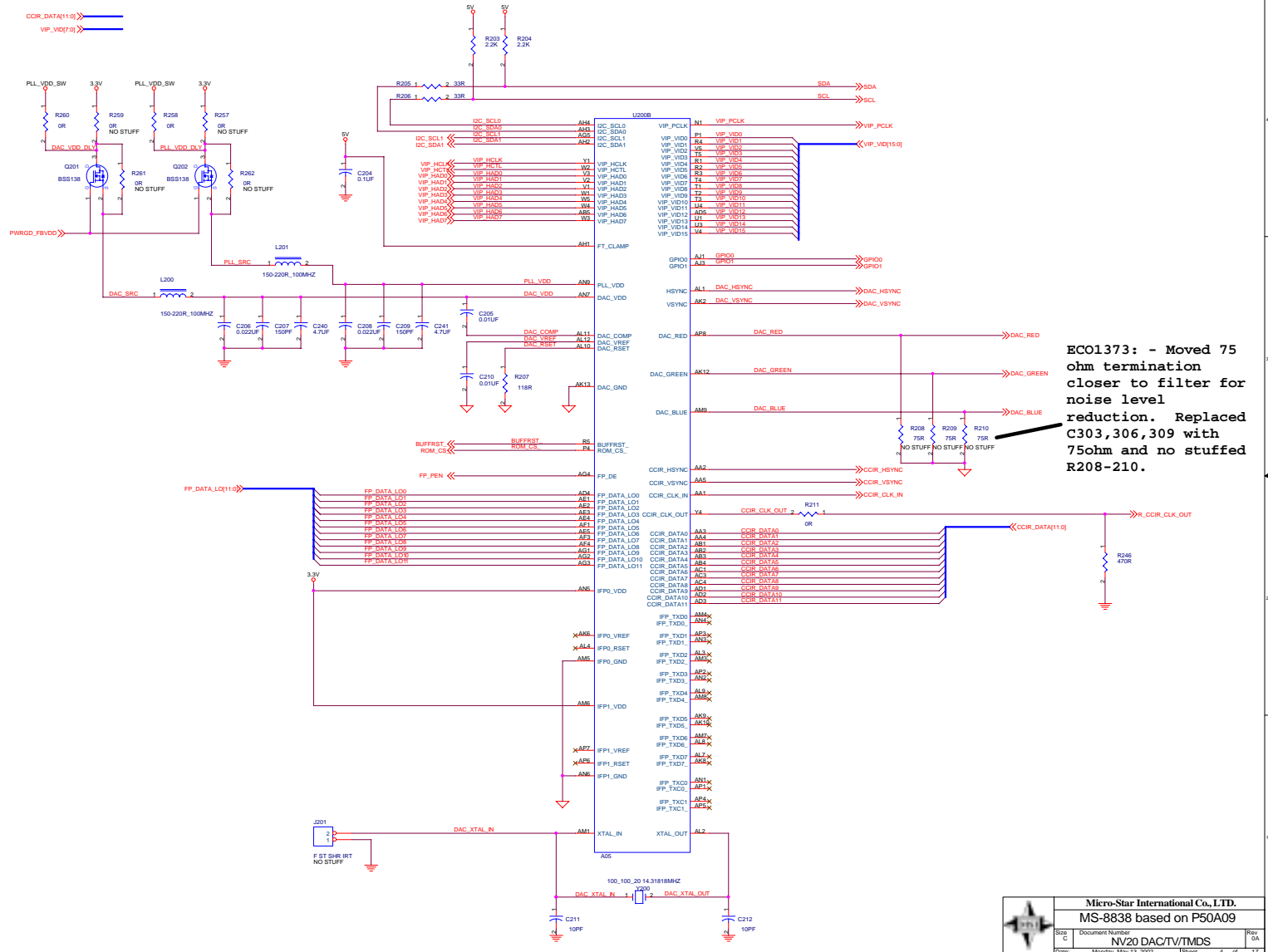
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In all cases each capacitor should be low ESR/ESL and placed as close as possible to the respective rail connector pin(s).

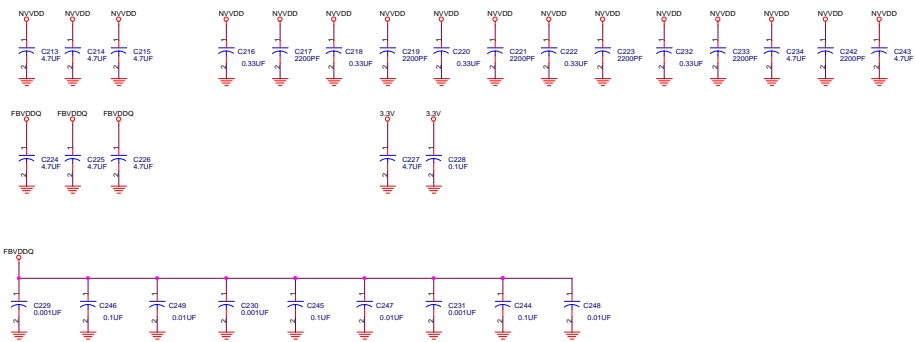
A trace across the 2 resistor pads can be cut to enable A0722 mode for debug.





Use thick (non-impedance controlled) traces on XTALIN/OUT

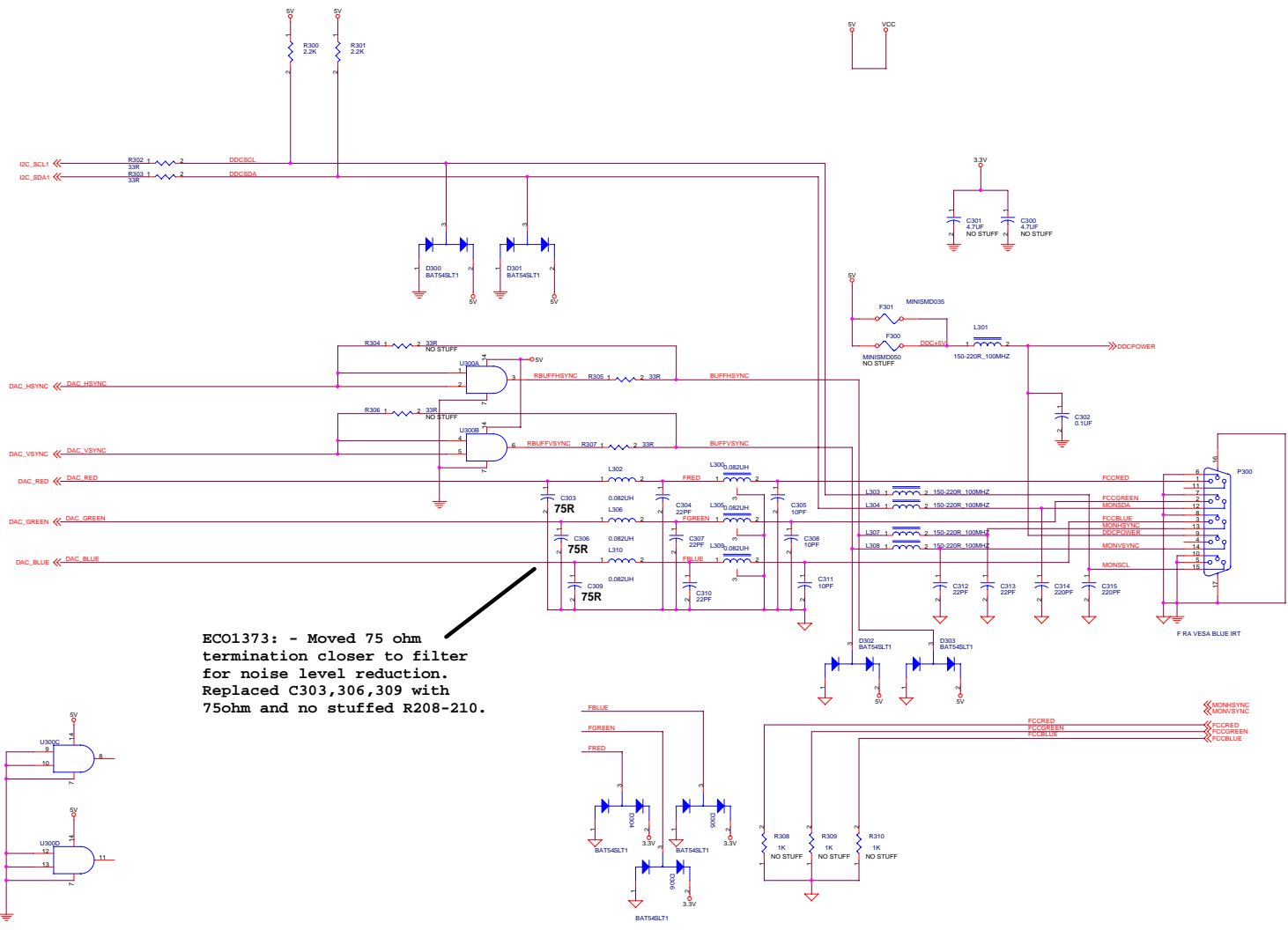
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NV20 DAC/TV/TMDS		Date	Monday, May 13, 2008
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VIP\_VID[15:0]  
FP\_DATA[10:11:0]

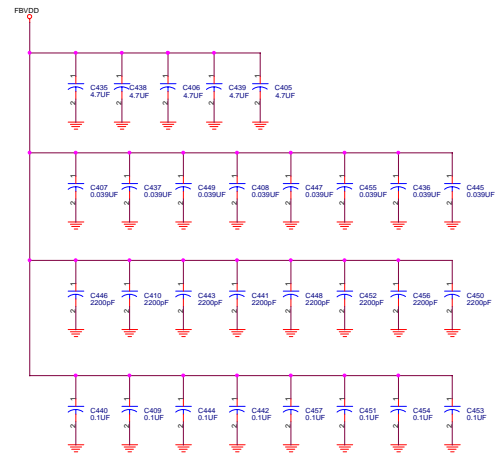
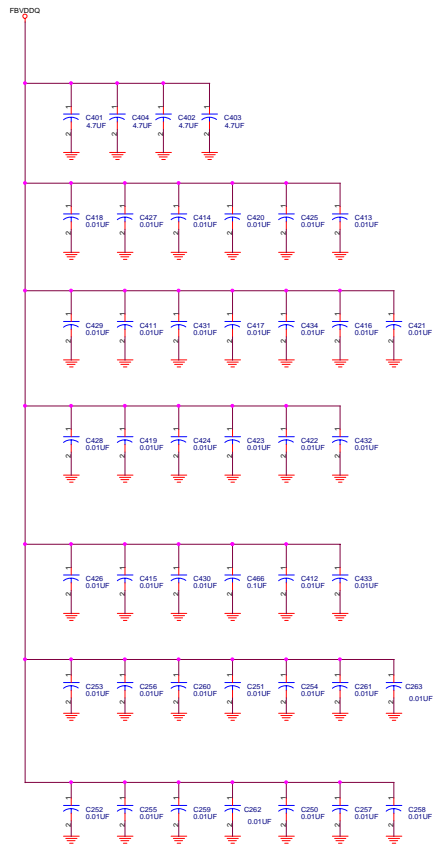
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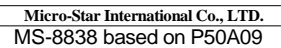
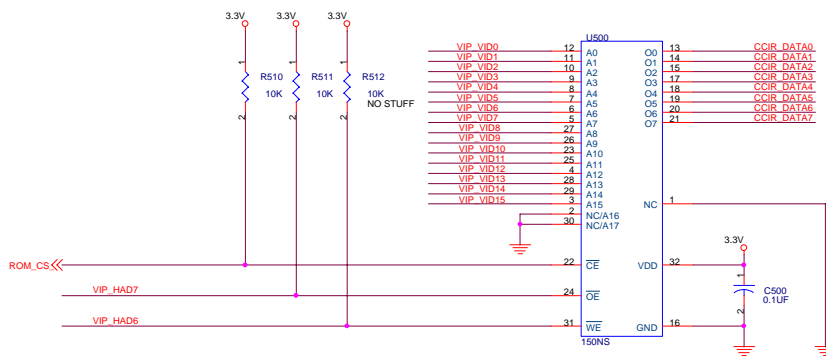




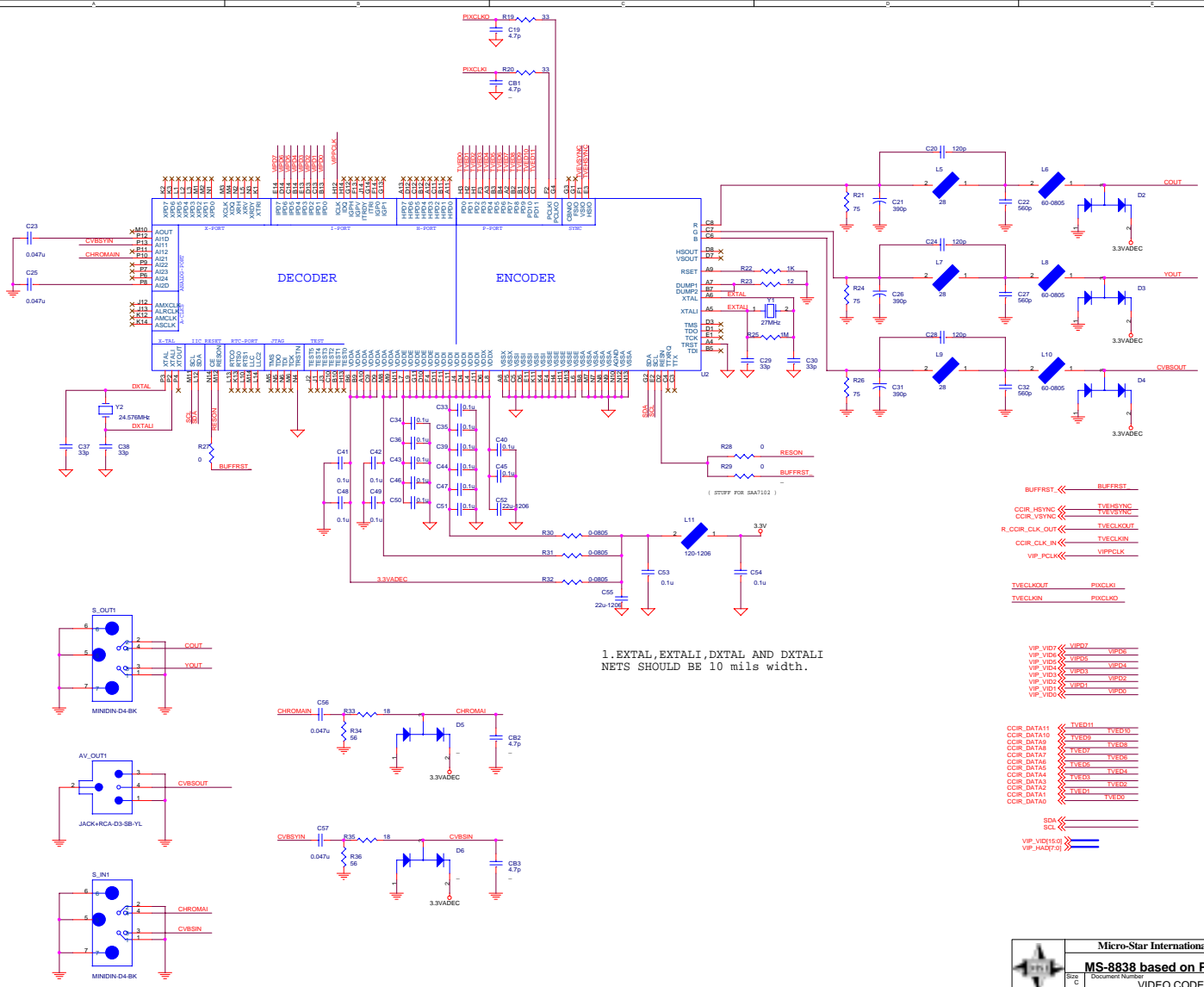


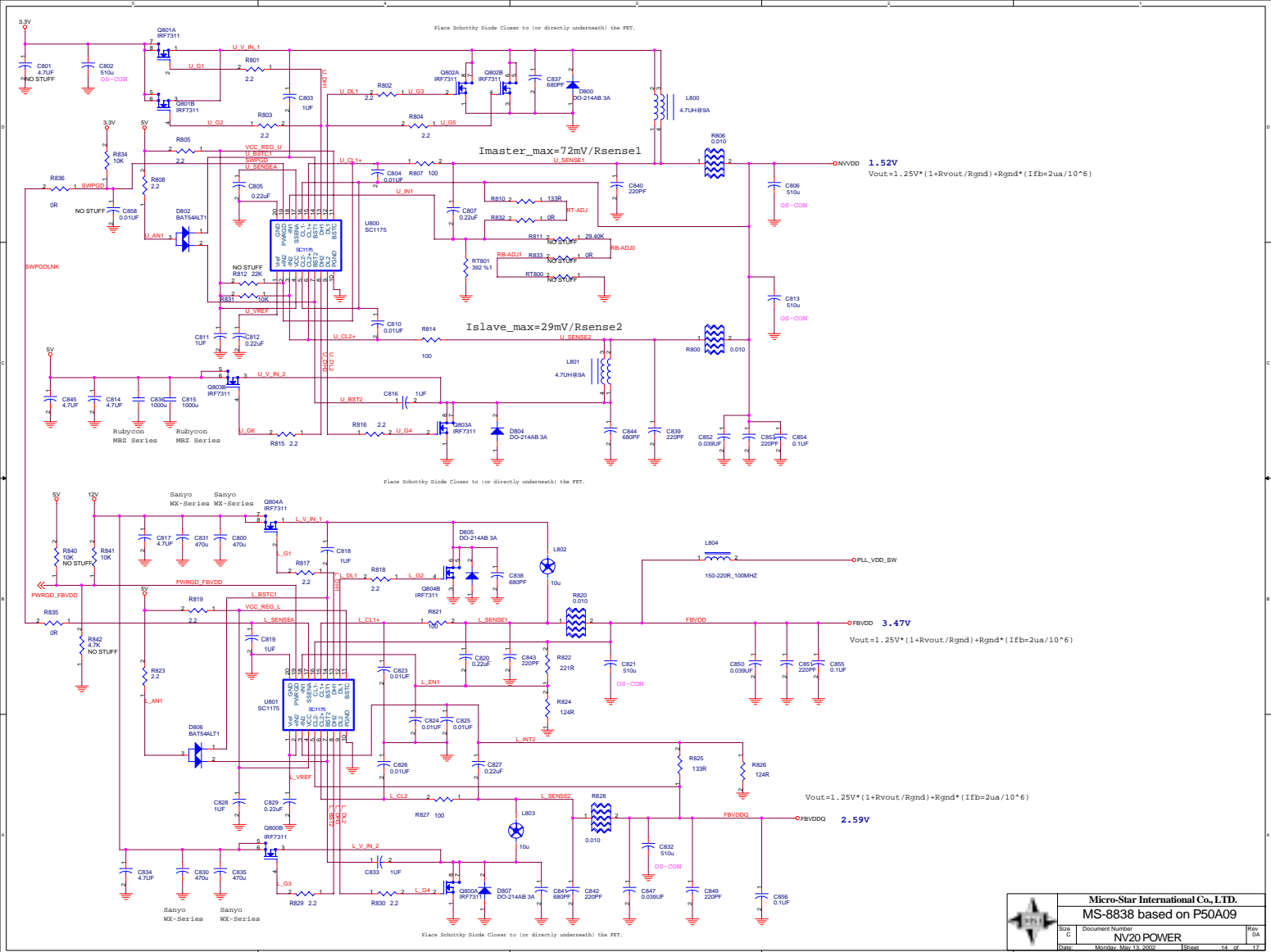


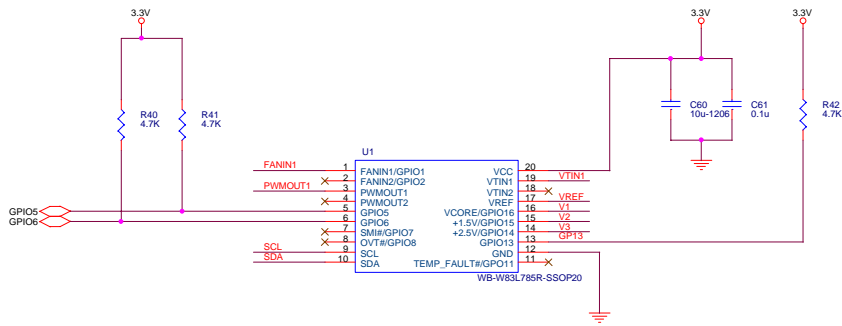




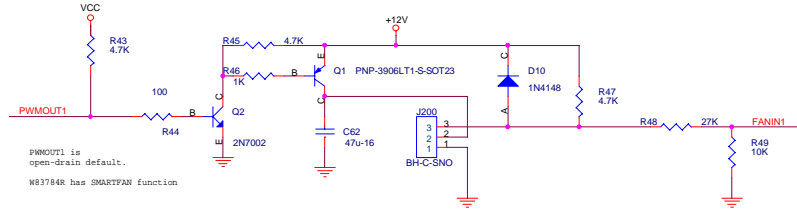
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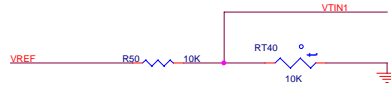




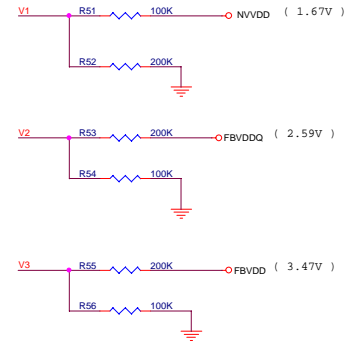
SDA << SDA 4.13  
SCL << SCL 4.13



PWM1 Circuit for FAN1 speed Control  
FOR 12V FAN



TEMPERATURE SENSING CIRCUIT



VOLTAGE SENSING CIRCUIT

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P300-2  
SCREW



JP1  
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