MS-V091 -- G84, 256/512 MB 16x32 DDR3-136pin, DVI-I,SD/HDTV,VIVO,

SUMMARY:

1. Base on V069-100 to Modify HDMI change to internal support
2. BGA-136 DDRIII
3. RT-8805 Two Phase PWM for NVVDD
4. MS-11 for FBVDD

Table of Contents:

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Page 21: Linear Power
Page 22: NVVDD with MS-11 MS-V1
Page 23: FBVDD with MS-11 MS-V1

Rev History

OA

Page 3 Enable G23pin H_PLLVDD 1V2 for G84 only
Page 11 reserve G84 SLI circuit
Page 12,13,14 reserve DAC_Vref power for G84 DACA,B,C
Page 16 reserve 1V8 for G84 IFPAB_PLLVDD
Page 17 reserve 1V8 for G84 IFPCD_PLLVDD
Page 18 reserve 1V2 for G84 PLLVDD and VID_PLLVDD
Page 20 reserve MIOB_CTL3 new strap for G84 PCI_DEVID_4
Page 20 reserve ROM_SI pull-down resister required if MIOA VDDQ=2.5V for G84
Page 21add 1V8 power for G84
Page 22,23 Reserve MS-V1co-lay circuit

100

Page 3 H_PLLVDD 1V2 use 0ohm connect to PEX1V2
Page 3 Reserve G84 Dual Rank(Stacked Die) circuit FBA_CMD7----CS1 FBA_CMD27---BA2
Page 7 Reserve G84 Dual Rank(Stacked Die) circuit FBC_CMD7----CS1 FBC_CMD27---BA2
Page 7 Reserve I2CS citcuit for G84
Page 6,10 Enable FBAA2 and FBCC2 BA2 Pin this is for Stacked Die Function
Page 13 Modify RGB circuit
Page 15 Modify SAA7115 RESET circuit
Page 18 Modify Spidf circuit
Page 21 Modify Linear Power circuit
Page 22 NVVDD PWM Change to RT-8805 Two Phase
Page 22,23 Remove MS-V1co-lay circuit

110

Page 3 Connect FBVDD for G84
Page 18 Reverve other Spidf circuit
Page 22 Co-lay small chock for NVVDD

V091-Base on V089-110 to Modify

1.Modify to power NVVDD and FBVDDQ cirdcuit
2.Remove HDMI Circuit Add DIV Circuit
3.Rem SPIDF Circuit
4.Add Dual VBIOS Circuit
5.Add Thermal Protection Circut

MSI	Micro-Star International Co., LTD.		
	SUMMARY		
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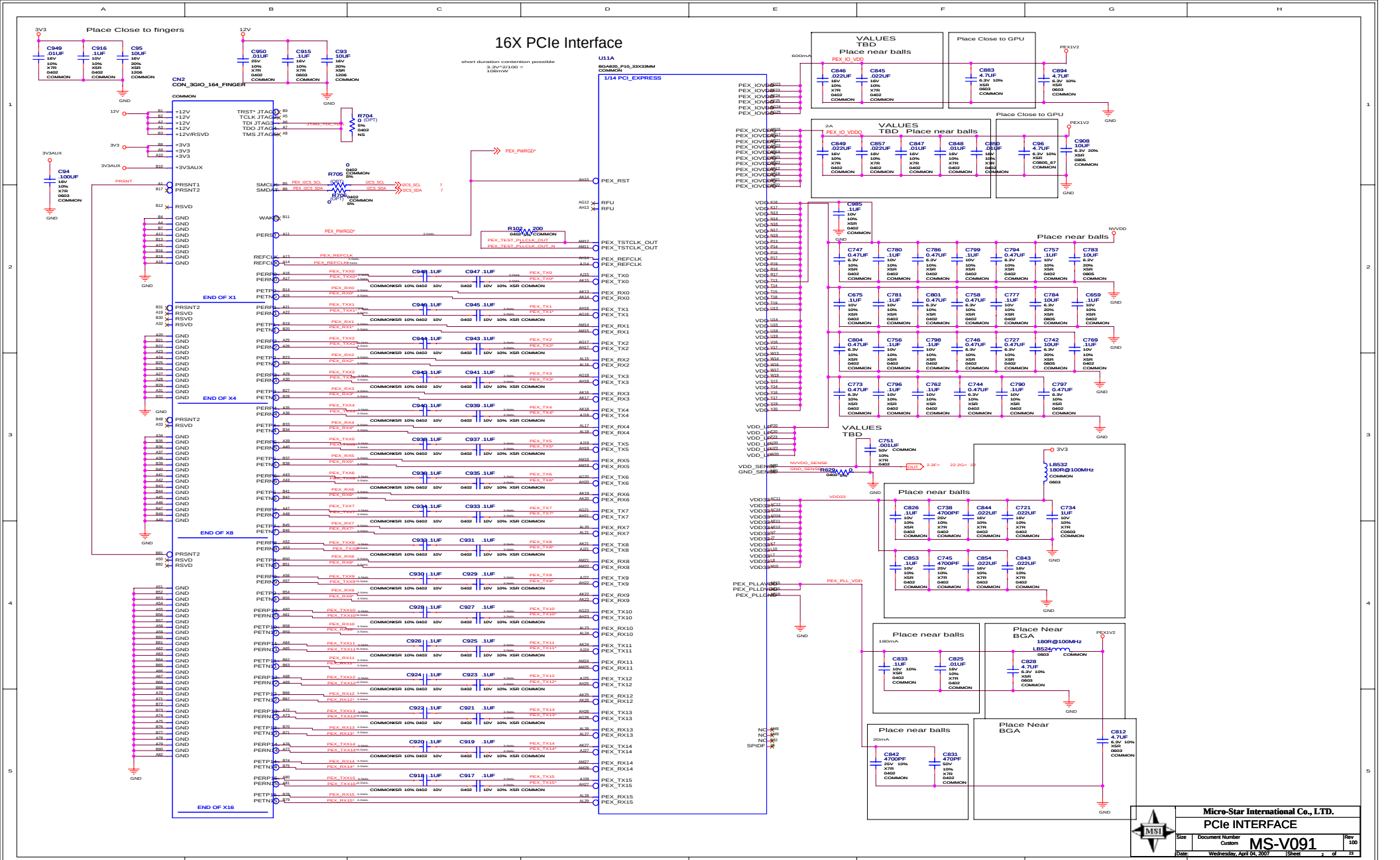
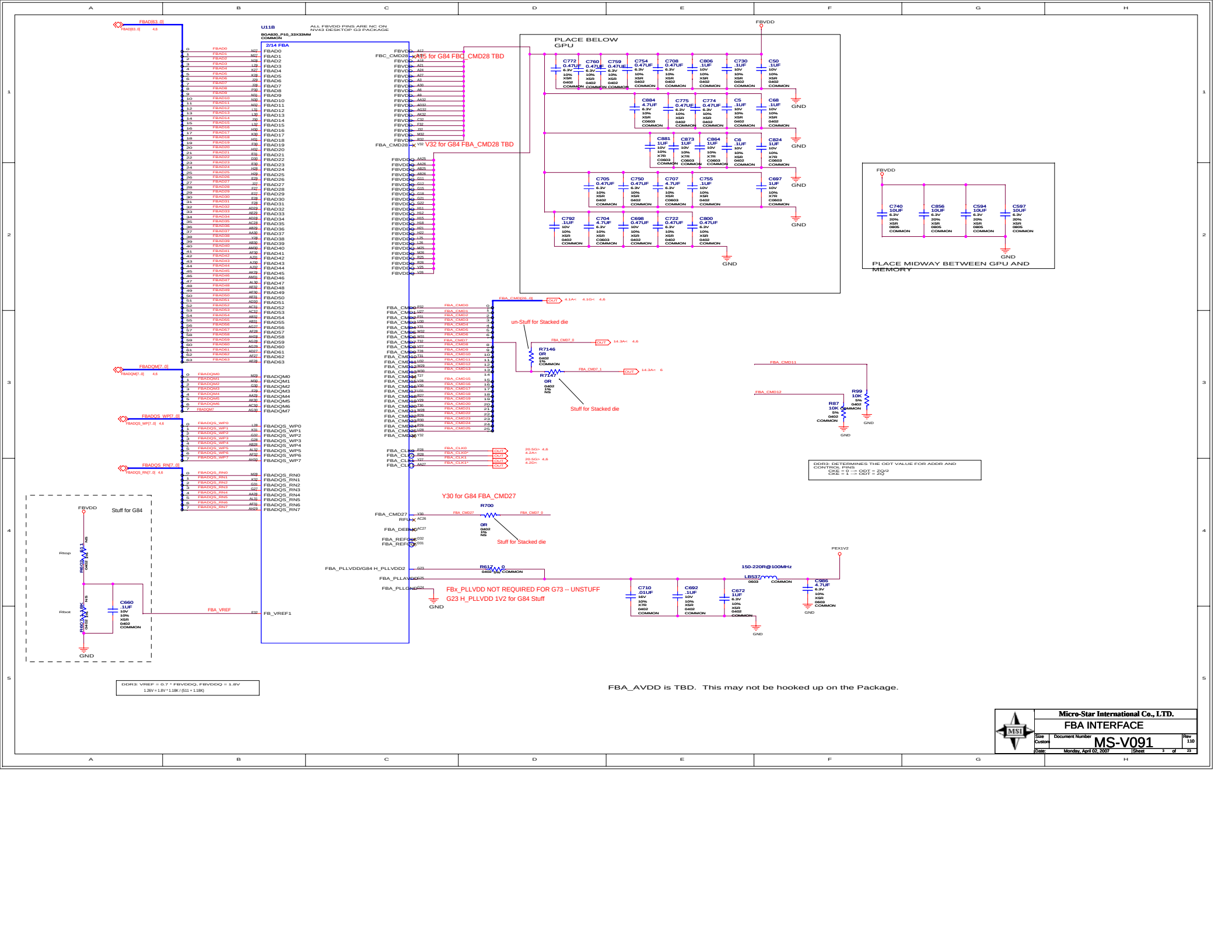
16X PCIe Interface




U11B
ALL FBVDD PINS ARE NC ON NV43 DESKTOP G3 PACKAGE
8GA820_P10_33X33MM
COMMON
2/14 FBA
PLACE BELOW GPU
PLACE MIDWAY BETWEEN GPU AND MEMORY
Stuff for G84
Stuff for Stacked die
un-Stuff for Stacked die
Y30 for G84 FBA_CMD27
V32 for G84 FBA_CMD28 TBD
FBx_PLLVDD NOT REQUIRED FOR G73 -- UNSTUFF
G23 H_PLLVDD 1V2 for G84 Stuff
DDR3: VREF = 0.7 * FBVDDQ, FBVDDQ = 1.8V
1.26V = 1.8V * 1.18K / (511 + 1.18K)
DDR3: DETERMINES THE ODT VALUE FOR ADDR AND CONTROL PINS
CKE = 0 --> ODT = ZQ/2
CKE = 1 --> ODT = ZQ
FBA_AVDD is TBD. This may not be hooked up on the Package.
Micro-Star International Co., LTD.
FBA INTERFACE
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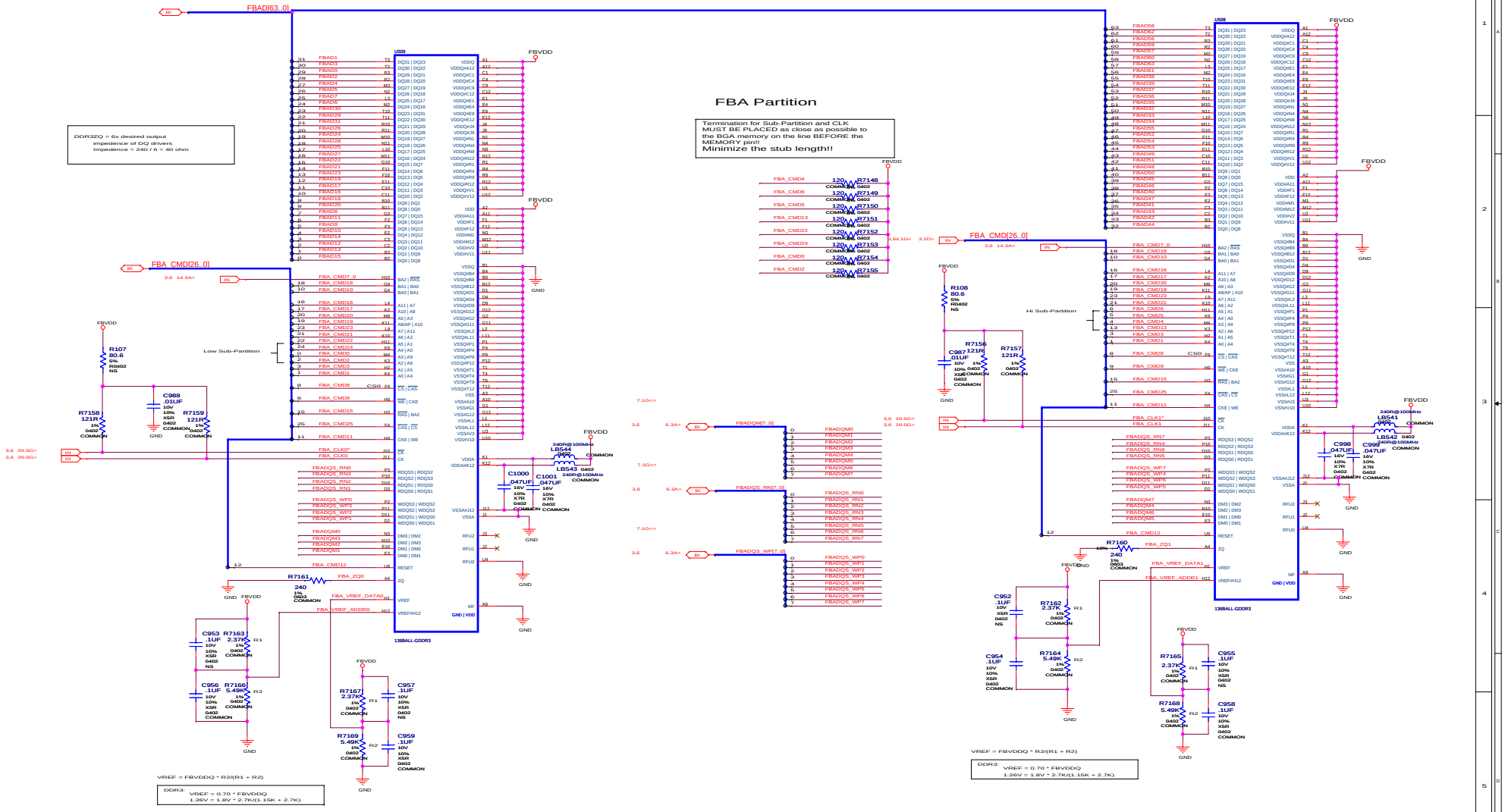
FrameBuffer: Partition A
16Mx32 BGA136 DDR3



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FB A1	
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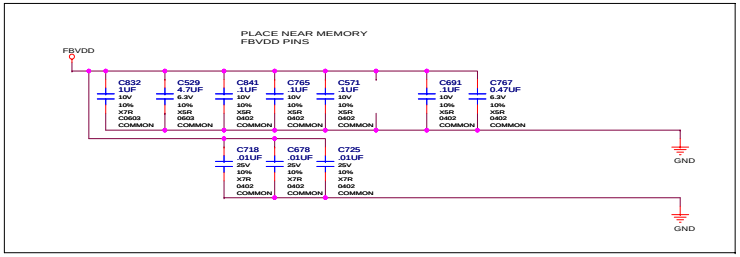
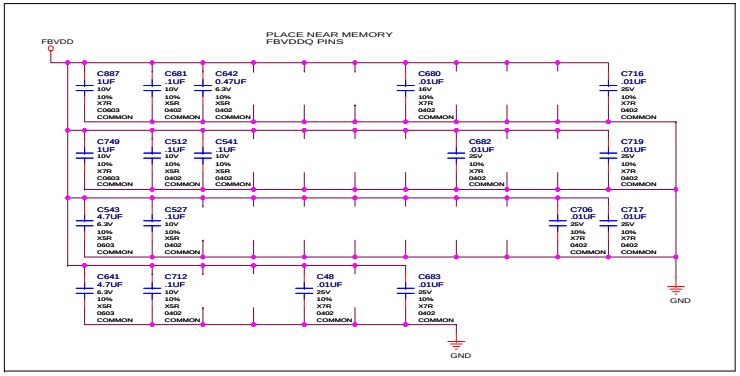
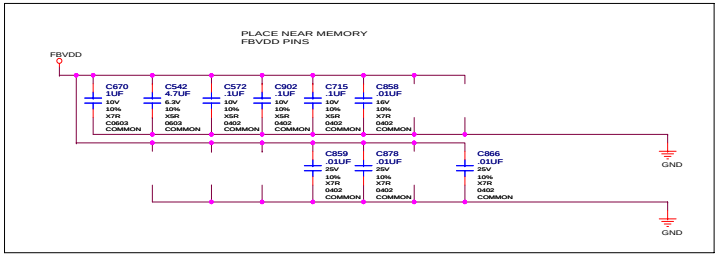
FRAME BUFFER: PARTITION A DECOUPLING

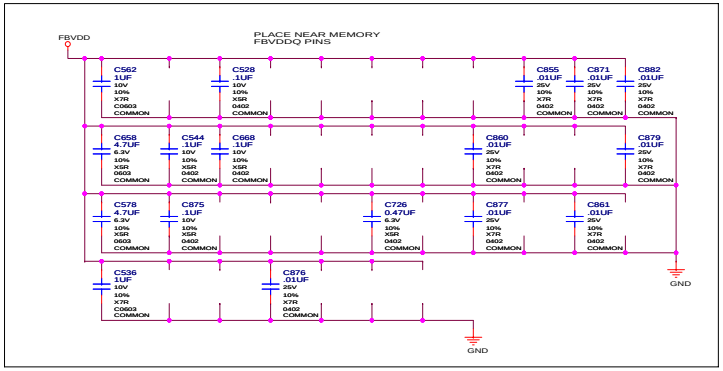
Decoupling for FBA 0..31





Decoupling for FBA 32..63





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FBA DECOUPLING	
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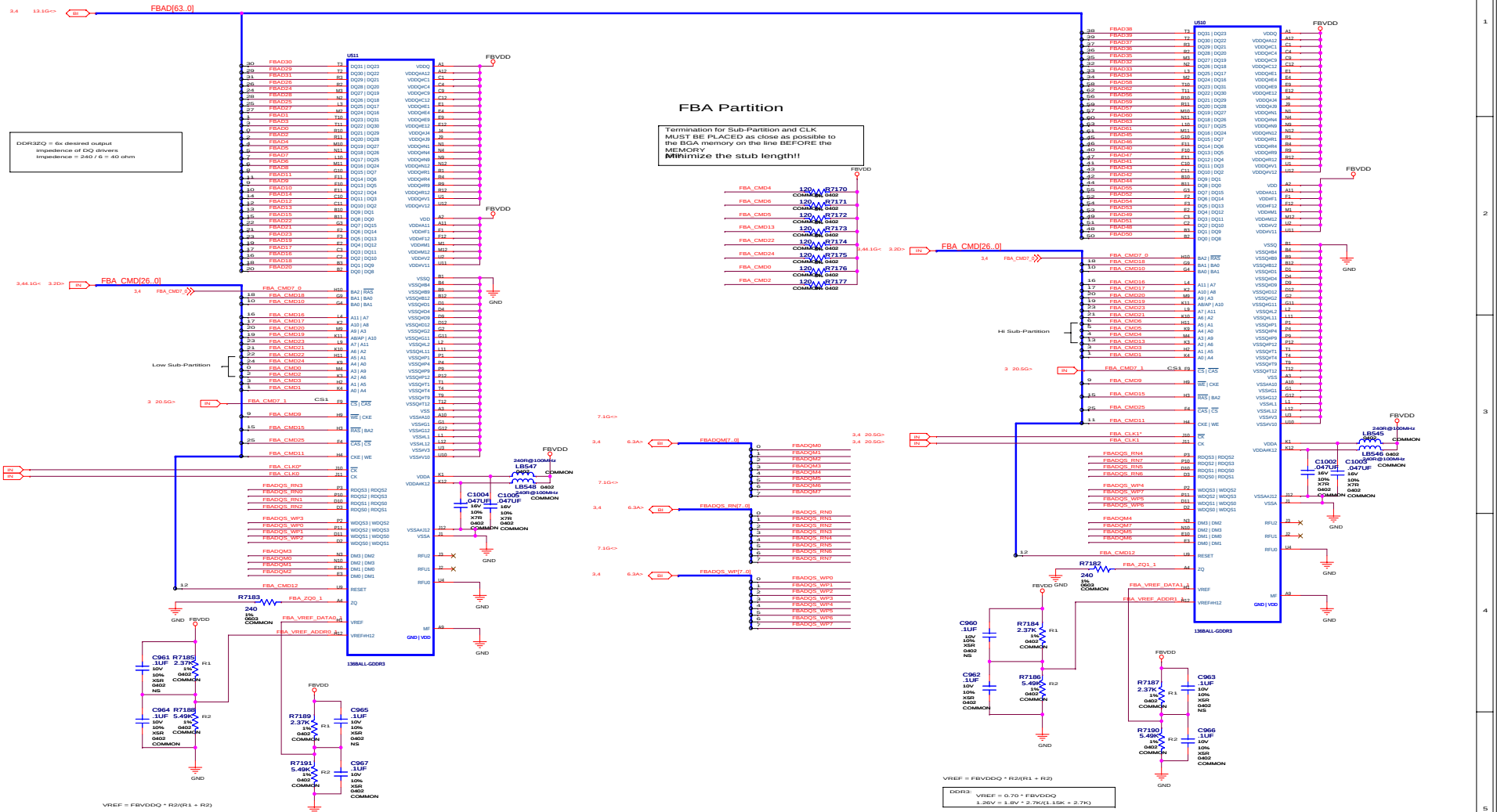
FrameBuffer: Partition A
16Mx32 BGA136 DDR3



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FB A2	
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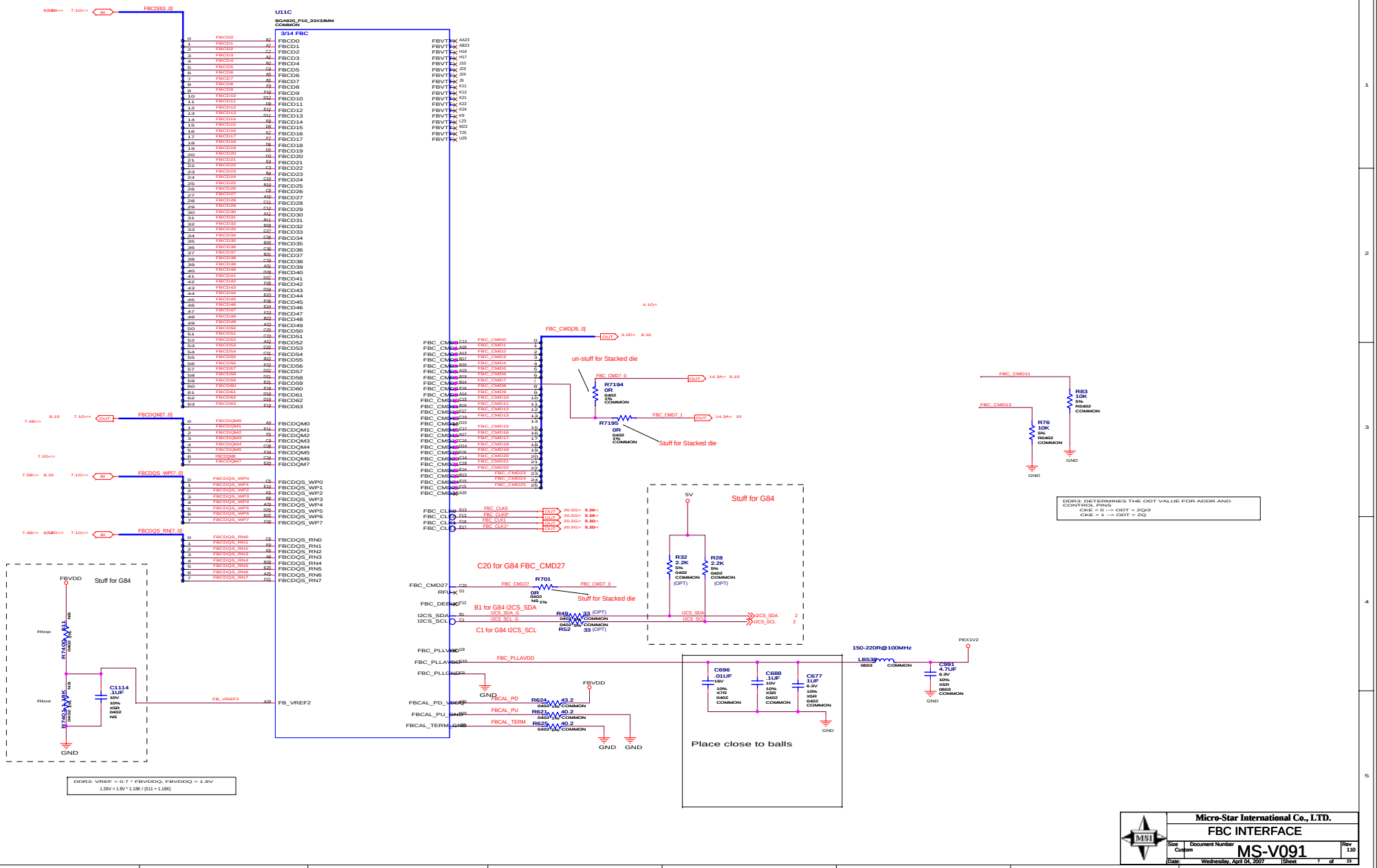
U11C
8GA820_P10_33X33MM
COMMON
3/14 FBC
FBCD[63..0]
FBCDQM[7..0]
FBCDQS_WP[7..0]
FBCDQS_RN[7..0]
FBVDD
Stuff for G84
Rtop
Rbot
C1114
1UF
10V
X5R
0402
NS
FB_VREF2
GND
DDR3: VREF = 0.7 * FBVDDQ, FBVDDQ = 1.8V
1.26V = 1.8V * 118K / (511 + 118K)
un-stuff for Stacked die
FBC_CMD[26..0]
FBC_CMD7_0
R7194
0R
0402
1%
COMMON
R7195
Stuff for Stacked die
FBC_CMD11
FBC_CMD12
R83
10K
5%
R0402
COMMON
R76
10K
5%
R0402
COMMON
DDR3: DETERMINES THE ODT VALUE FOR ADDR AND CONTROL PINS
CKE = 0 --> ODT = 2Q/2
CKE = 1 --> ODT = 2Q
C20 for G84 FBC_CMD27
R701
Stuff for Stacked die
B1 for G84 I2CS_SDA
C1 for G84 I2CS_SCL
R49
R52
33
(OPT)
COMMON
Stuff for G84
5V
R32
2.2K
5%
0402
(OPT)
R28
2.2K
5%
0402
COMMON
(OPT)
I2CS_SDA
I2CS_SCL
FBC_PLLAVDD
150-220R@100MHz
LB539
0603
COMMON
PEX1V2
C696
.01UF
10V
10%
X7R
0402
COMMON
C688
1UF
10V
10%
X5R
0402
COMMON
C677
1UF
6.3V
10%
X5R
0402
COMMON
C991
4.7UF
6.3V
10%
X5R
0603
COMMON
Place close to balls
FBCAL_PD
FBCAL_PU
FBCAL_TERM
R624
R621
R625
43.2
40.2
40.2
COMMON
Micro-Star International Co., LTD.
FBC INTERFACE
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1.0
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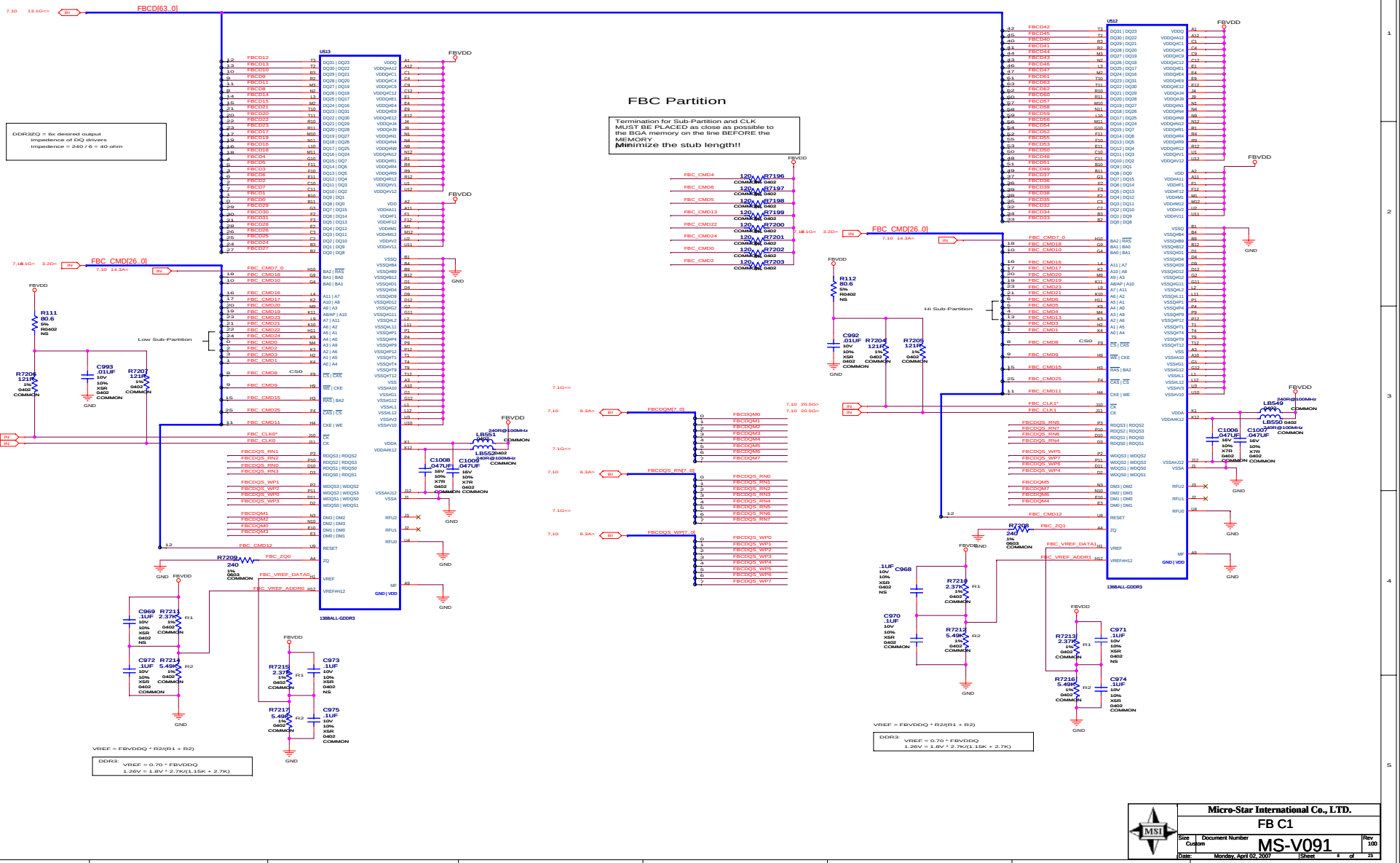
23

FRAMEBUFFER: PARTITION C 16Mx32 BGA136 DDR3



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FB C1	
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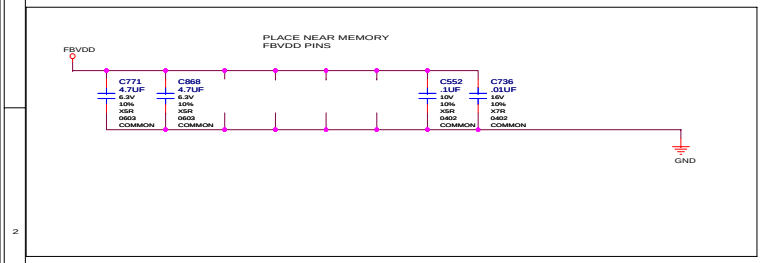
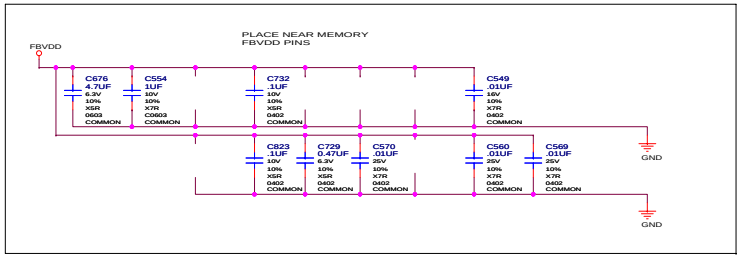
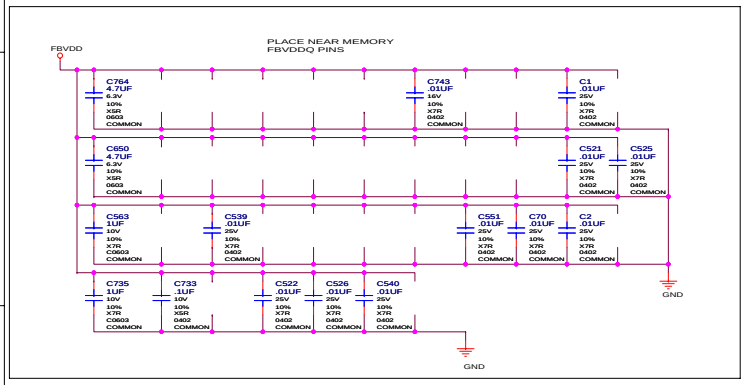
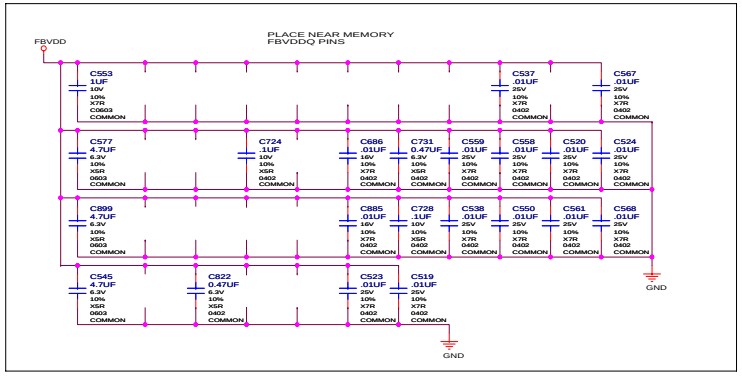
FRAMEBUFFER: PARTITION C DECOUPLING

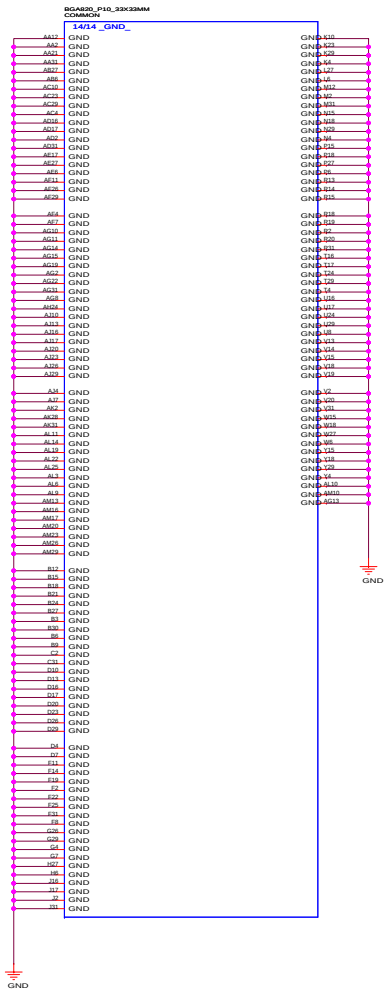
Decoupling for FBC 0..31











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FBC DECOUPLING	
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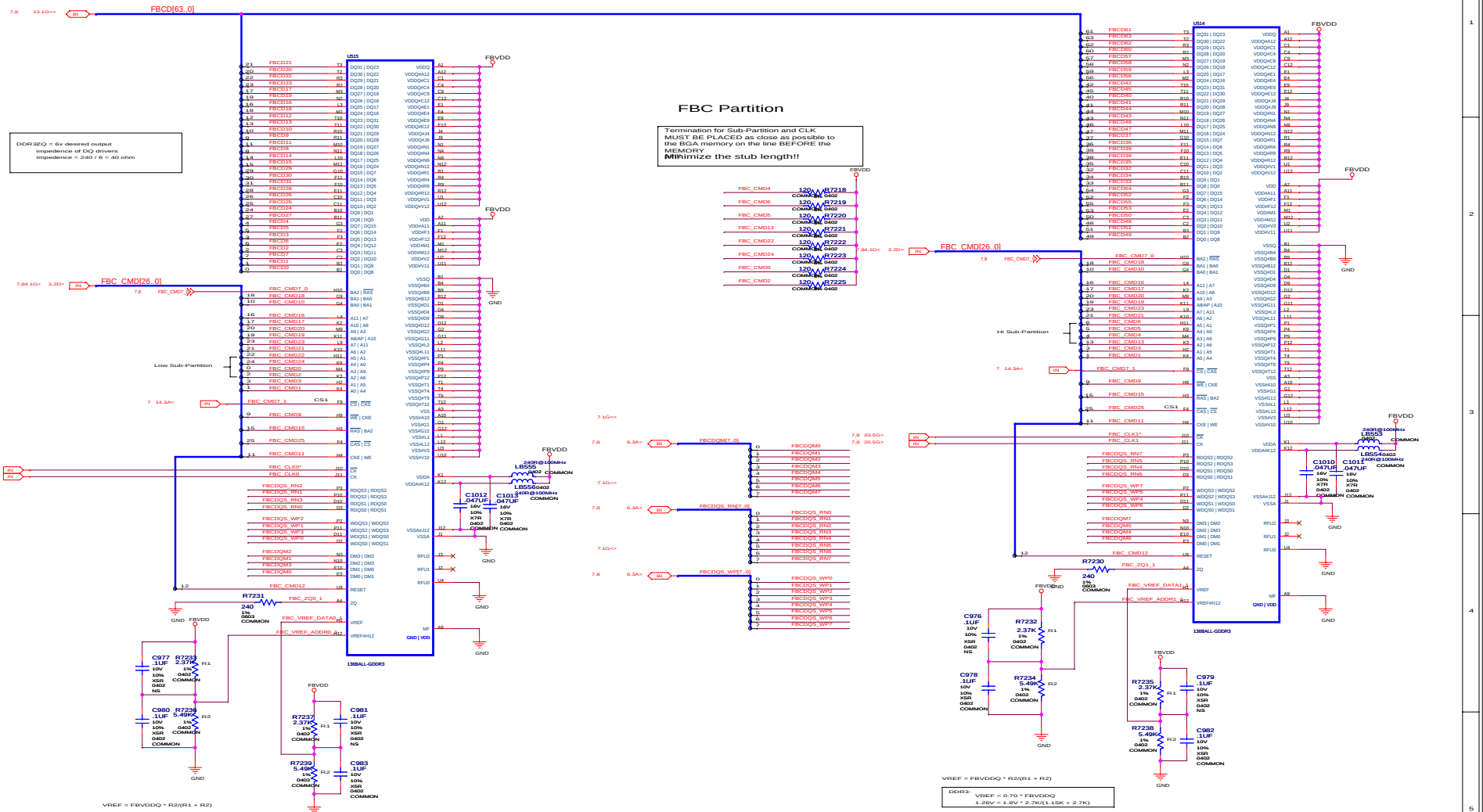
FRAMEBUFFER: PARTITION C 8Mx32 BGA136 DDR3



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FB C2	
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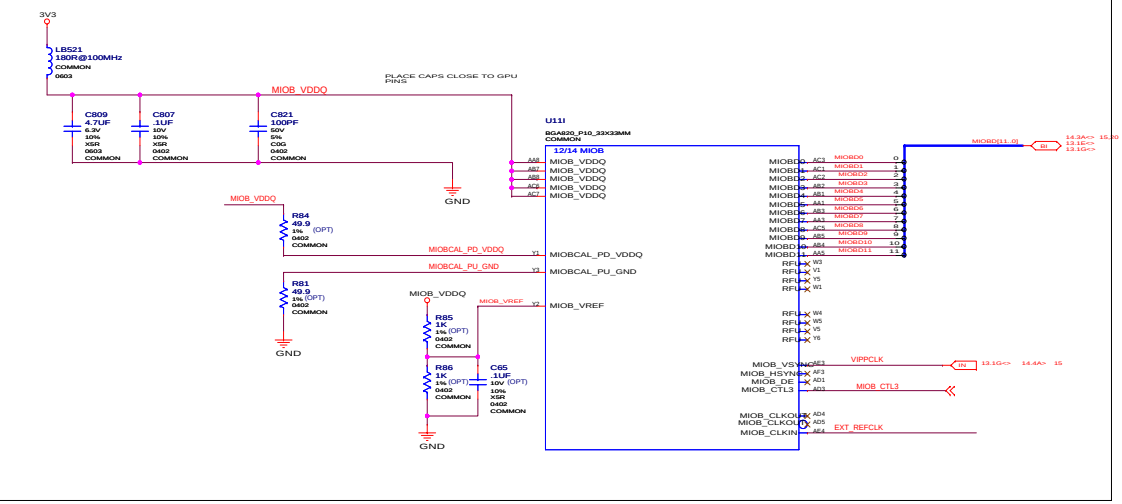
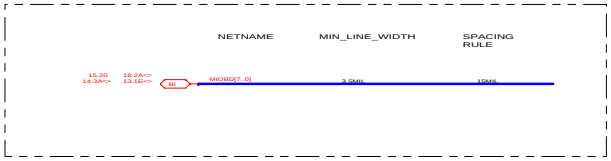
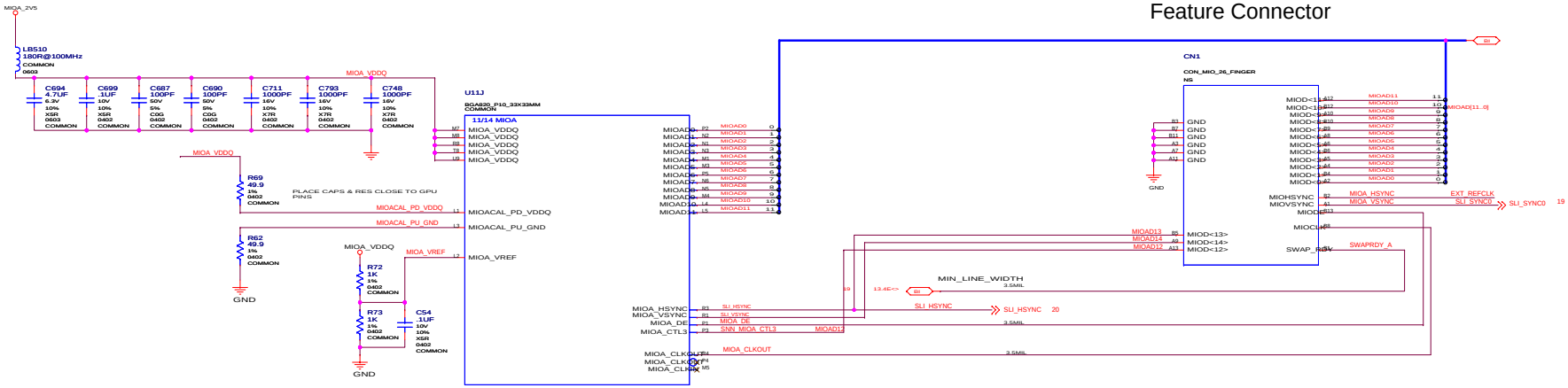
G3 VIP/MIOB





G3 MIOA



Feature Connector

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MIOA/MIOB	
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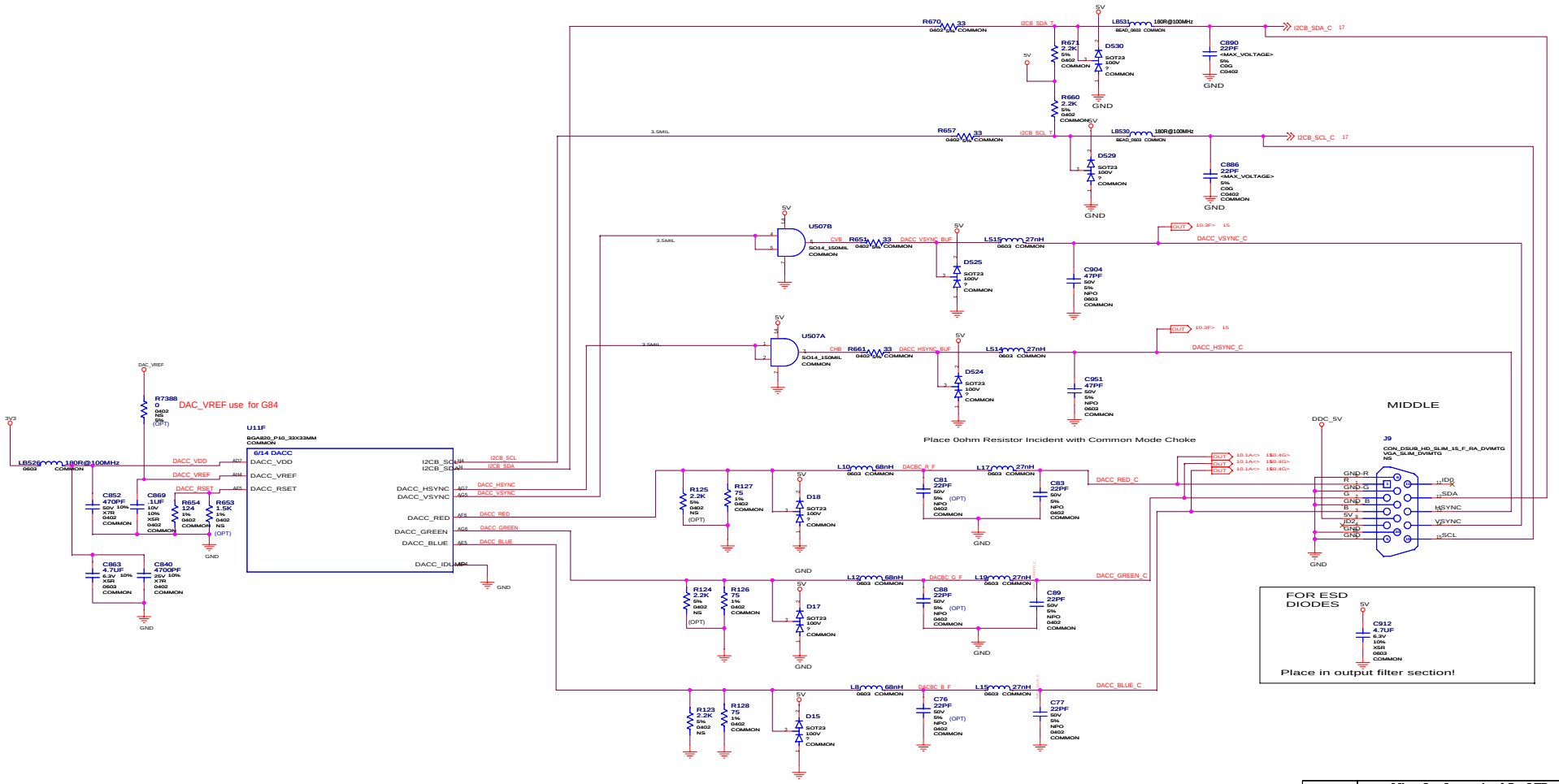
Secondary Display (DACC),Slim DB15



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DACC	
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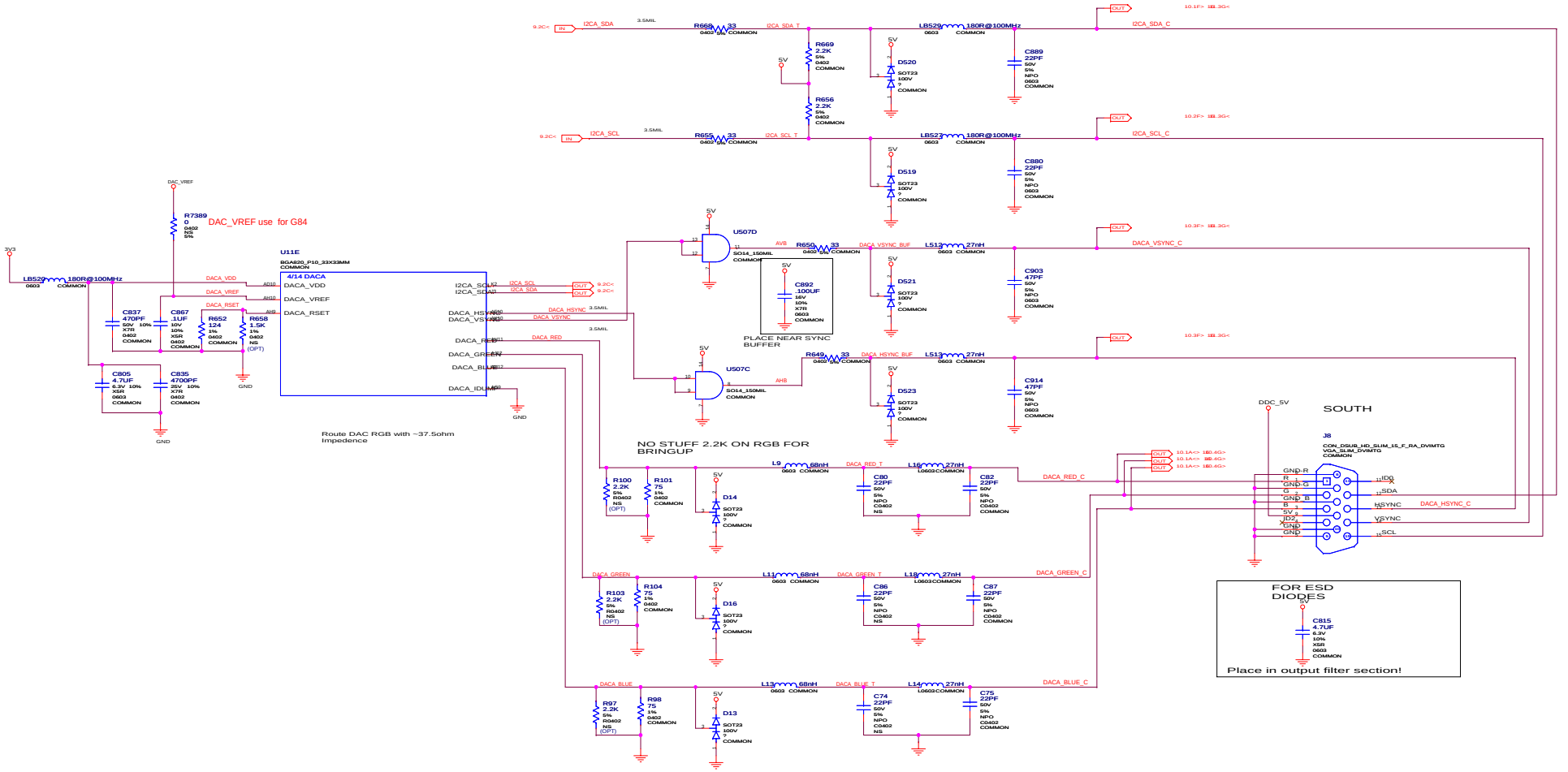
Primary Display (DACA), Slim DB15

DACA RGB-FILTER



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DACA	
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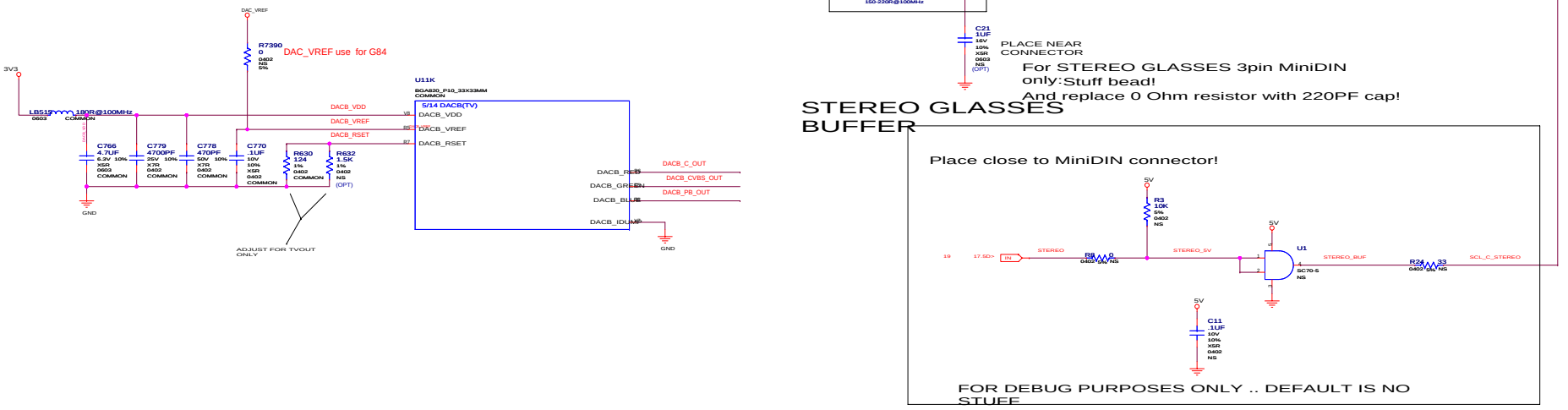
DACB .. MiniDIN VIDEO IN/OUT CONNECTOR /STEREO GLASSES

FILTER NOTES:

SD: USE L=1.8UH

HD: USE L=?



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DACB	
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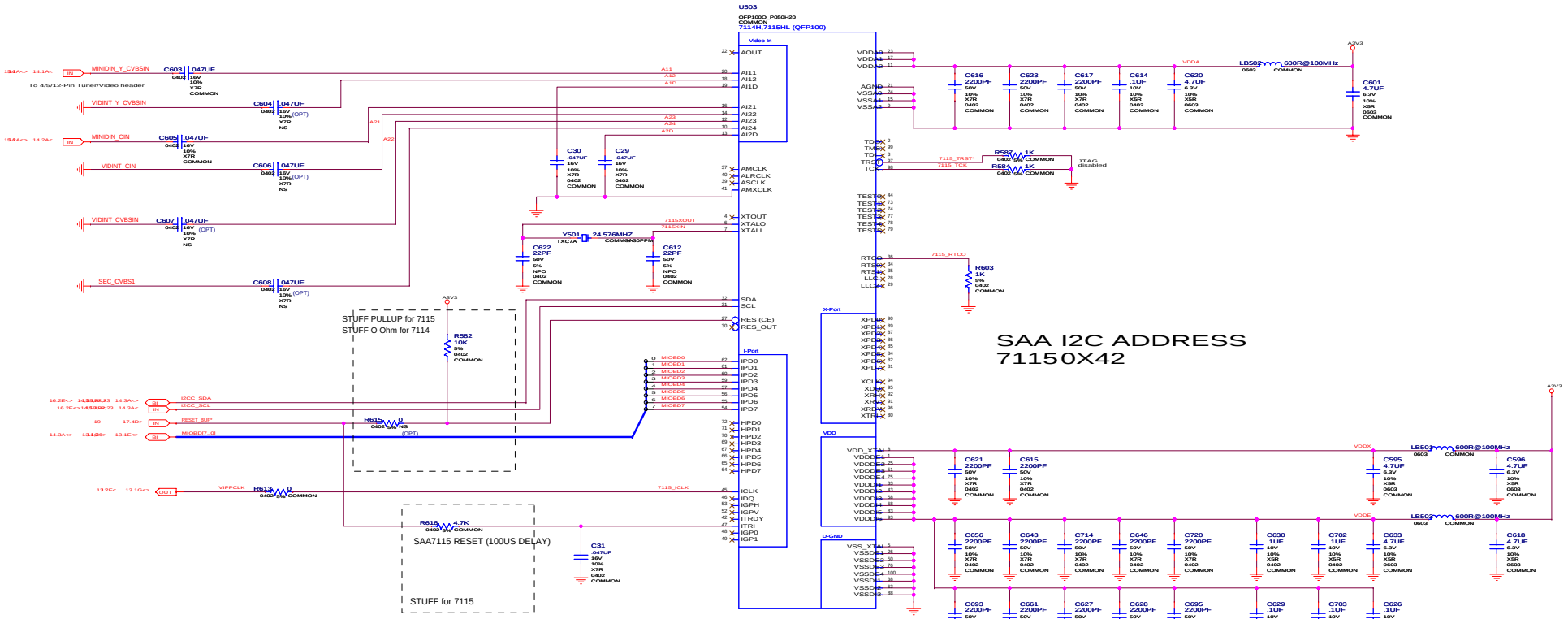
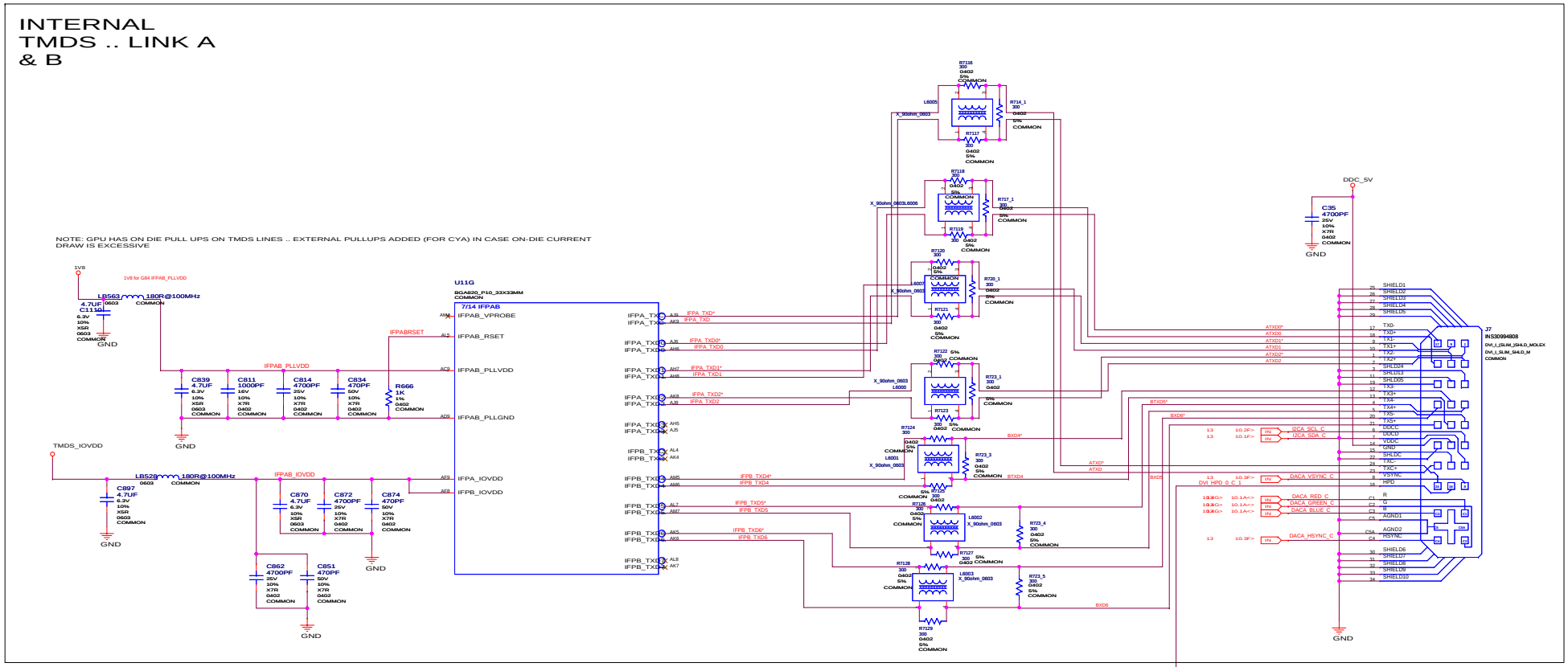
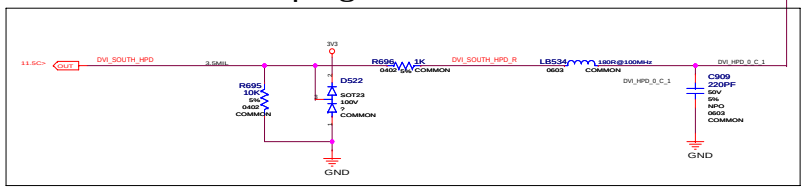
PHILIPS VIDEO CAPTURE



INTERNAL
TMDS .. LINK A
& B



Hotplug Detection



Micro-Star International Co., LTD.	
TMDS LINK A & B	
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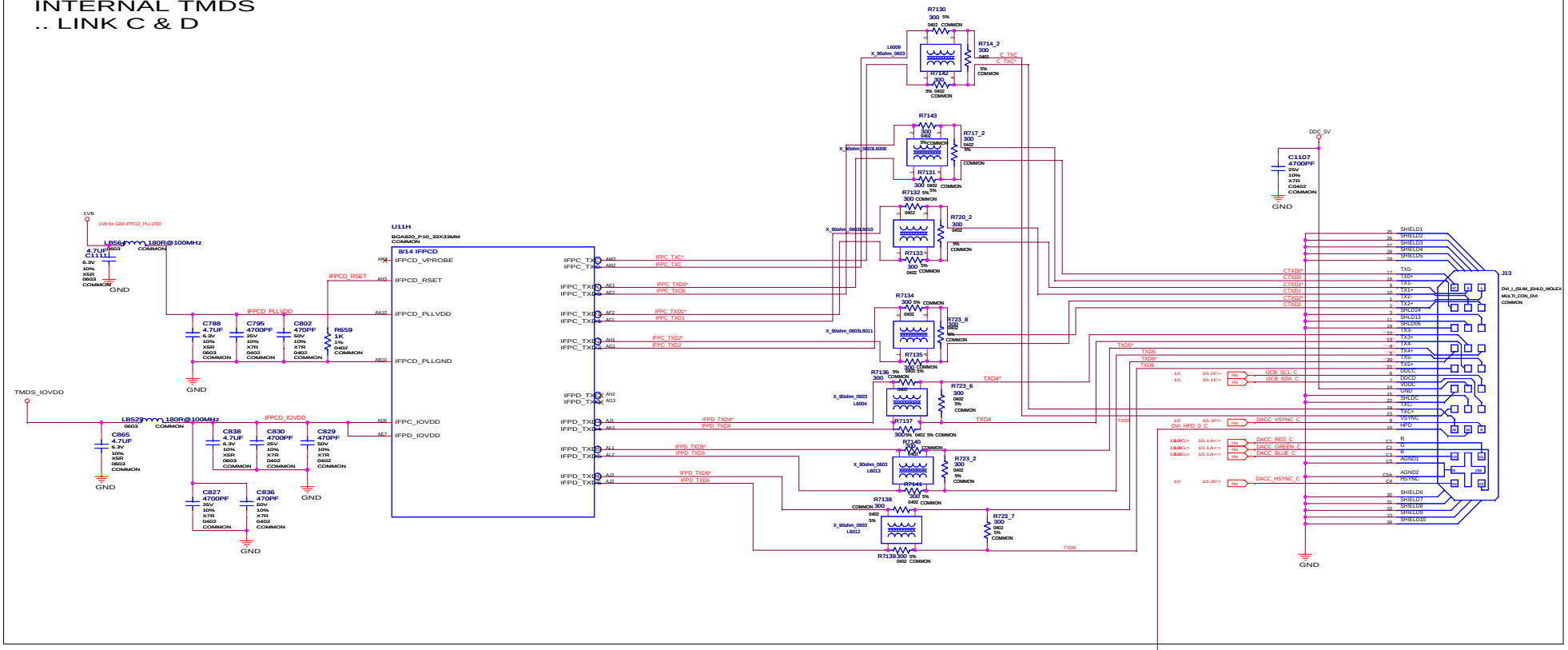
INTERNAL TMDS
.. LINK C & D



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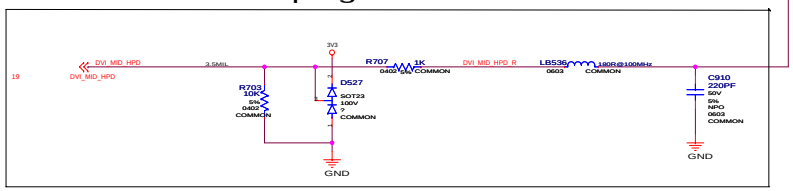

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TMDS LINK C & D	
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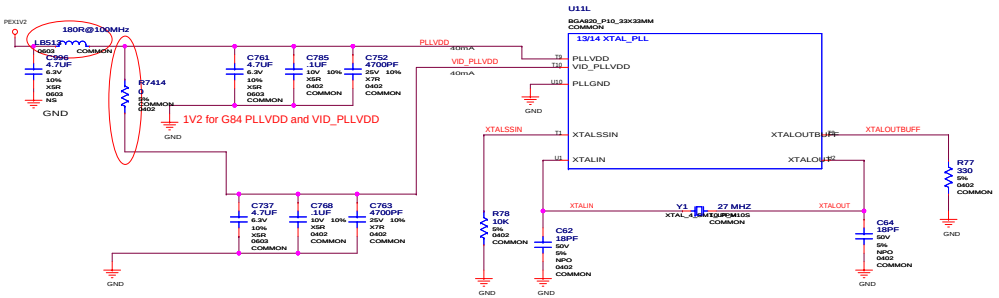
XTAL/PLLVDD



MSI	Micro-Star International Co., LTD.	
	XTAL/SPDIF IN	
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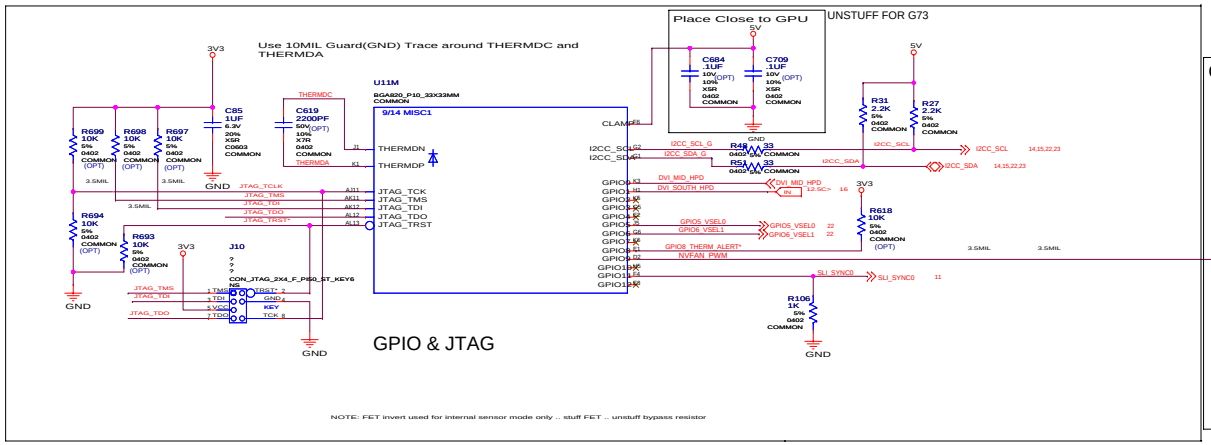
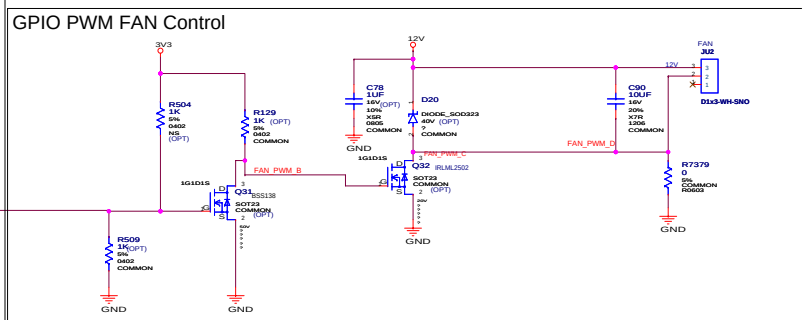
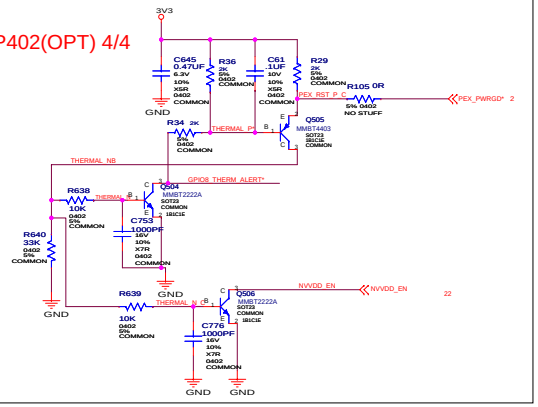




Thermal Protection

3/12 ADD

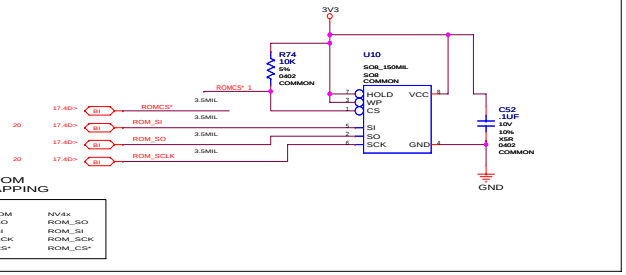
P-release P402(OPT) 4/4



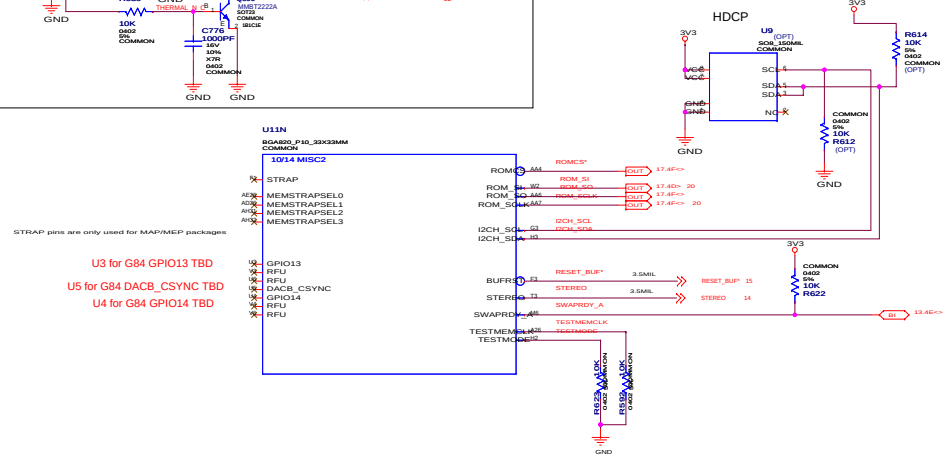
GPIO Assignment Table

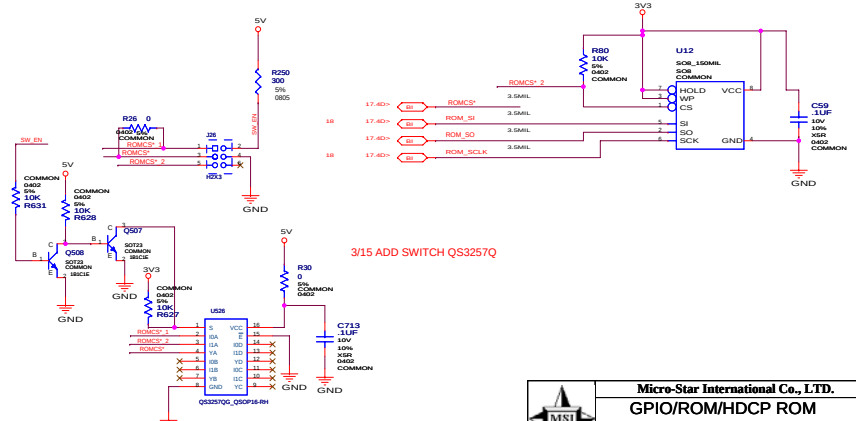
GPIO I/O		FUNCTION
0	IN	DVI MID HOTPLUG DET
1	IN	HDMI hotplug
2	IN	RESERVED
3	IN	RESERVED
4	IN	TUNER IRQ
5	OUT	NVVDD VOLTAGE SELECT 0
6	OUT	NVVDD VOLTAGE SELECT 1
7	Out	TPI INTERRUPT ENABLE
8	IN	RESERVED
9	OUT	PWM FAN
10	IN	INT from Sii1930
11	IN	TVRSET
12	IN	uC PROGRAMMING CONTROL

BIOS (serial)



3/13 NEW ADD DUAL VBIOS,LED circuit





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GPIO/ROM/HDCP ROM	
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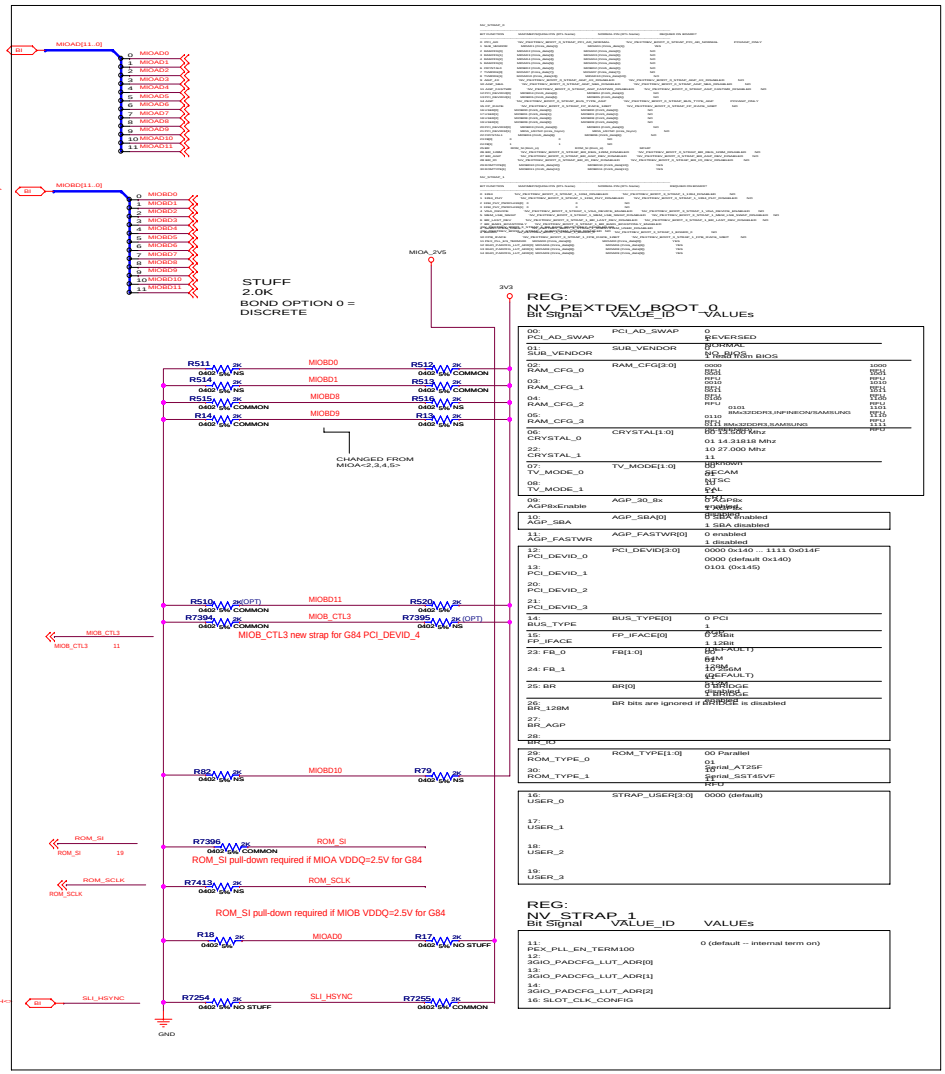
BIOS, Straps, Misc

Straps

Assembly:
BIOS



REG:
NV_PEXTDEV_BOOT_0

Bit	Signal	VALUE_ID	VALUEs
00:	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED 1 NORMAL
01:	SUB_VENDOR	SUB_VENDOR	0 NVIDIA 1 Read from BIOS
02: 03: 04: 05:	RAM_CFG_0 RAM_CFG_1 RAM_CFG_2 RAM_CFG_3	RAM_CFG[3:0]	0000 RFU 0001 RFU 0010 RFU 0011 RFU 0100 RFU 0101 RFU 0110 RFU 0111 RFU 1000 RFU 1001 RFU 1010 RFU 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 RFU
06: 22:	CRYSTAL_0 CRYSTAL_1	CRYSTAL[1:0]	00 13.5000 Mhz 01 14.31818 Mhz 10 27.000 Mhz 11
07: 08:	TV_MODE_0 TV_MODE_1	TV_MODE[1:0]	00 unknown 01 SECAM 10 NTSC 11 PAL
09:	AGP8xEnable	AGP_30_8x	0 AGPPRO 1 AGP30
10:	AGP_SBA	AGP_SBA[0]	0 SBA disabled 1 SBA enabled
11:	AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled
12: 13: 20: 21:	PCI_DEVID_0 PCI_DEVID_1 PCI_DEVID_2 PCI_DEVID_3	PCI_DEVID[3:0]	0000 0x140 ... 1111 0x014F 0000 (default 0x140) 0101 (0x145)
14: 15:	BUS_TYPE FP_IFACE	BUS_TYPE[0] FP_IFACE[0]	0 PCI 1 AGP 0 24bit 1 12Bit
23: 24:	FB_0 FB_1	FB[1:0]	00 64M 01 128M 10 256M 11 RFU (DEFAULT)
25:	BR	BR[0]	0 BRIDGE 1 NORTH BRIDGE
26: 27: 28:	BR_128M BR_AGP BR_IO	BR bits are ignored if BR=DISABLE is disabled	0 disabled 1 enabled
29: 30:	ROM_TYPE_0 ROM_TYPE_1	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F 10 Serial_SST45VF 11 RFU
16: 17: 18: 19:	USER_0 USER_1 USER_2 USER_3	STRAP_USER[3:0]	0000 (default)

REG:
NV_STRAP_1

Bit	Signal	VALUE_ID	VALUEs
11: 12: 13: 14: 16:	PEX_PLL_EN_TERM100 3GIO_PADCFG_LUT_ADR[0] 3GIO_PADCFG_LUT_ADR[1] 3GIO_PADCFG_LUT_ADR[2] SLOT_CLK_CONFIG		0 (default -- internal term on)

Mechanical parts

NEED FANSINK SYMBOL
FOR P216

MEC2 MEC_HEX_JACK_SCREW COMMON
MEC1 MEC_HEX_JACK_SCREW COMMON
MEC4 MEC_HEX_JACK_SCREW COMMON
MEC3 MEC_HEX_JACK_SCREW COMMON

155-00002-0000-000 SCREW PHIL PAN HD SS MACH 4-40 3/16

BKT BRKT_ADVID815S_8DVIDB15S_CDIN_2 COMMON

FAN HDA_GPU_TM31-2_T_A_L COMMON

PCB PCB V089-100

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM5 SW_FB
FM4 SW_FB
FM5 SW_FB

Fiducial Point

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Straps/Mechanical	
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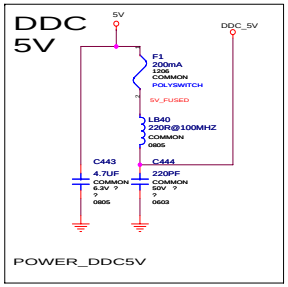
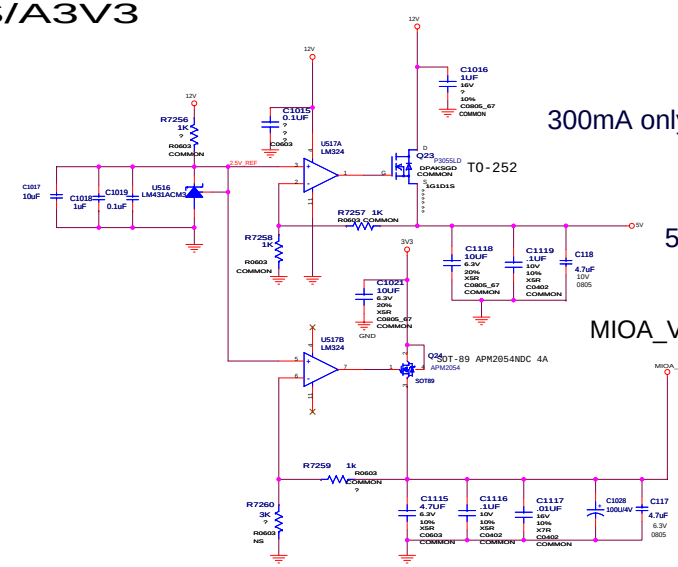
Power Supply TMDS/A3V3



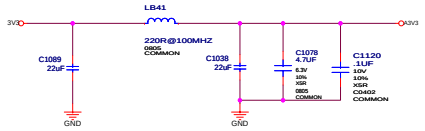


300mA only

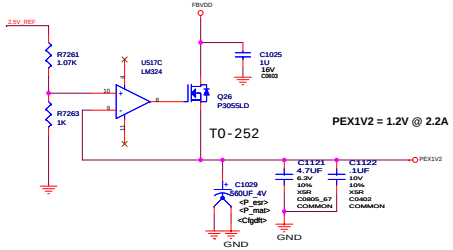
5V & A2V5

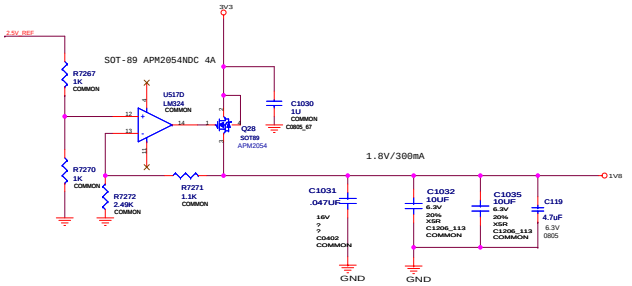
MIOA_VDDQ 2V5

Vout=2.5V



PEX1V2

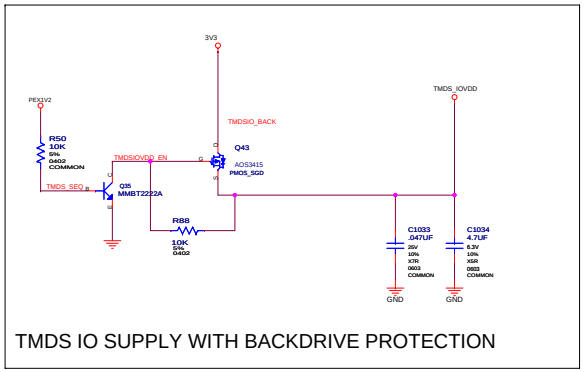




1V8 Supply use for G84 Non-use for G73

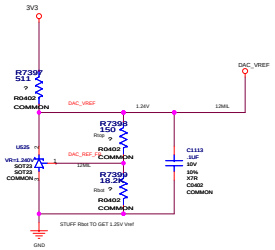
Vout=Vref(1+Rtopt/Rbot)

Vout=1.25(1+1.1K/2.49K)=1.8V



TMDS IO SUPPLY WITH BACKDRIVE PROTECTION

DAC V_REFERENCE SUPPLY for G84



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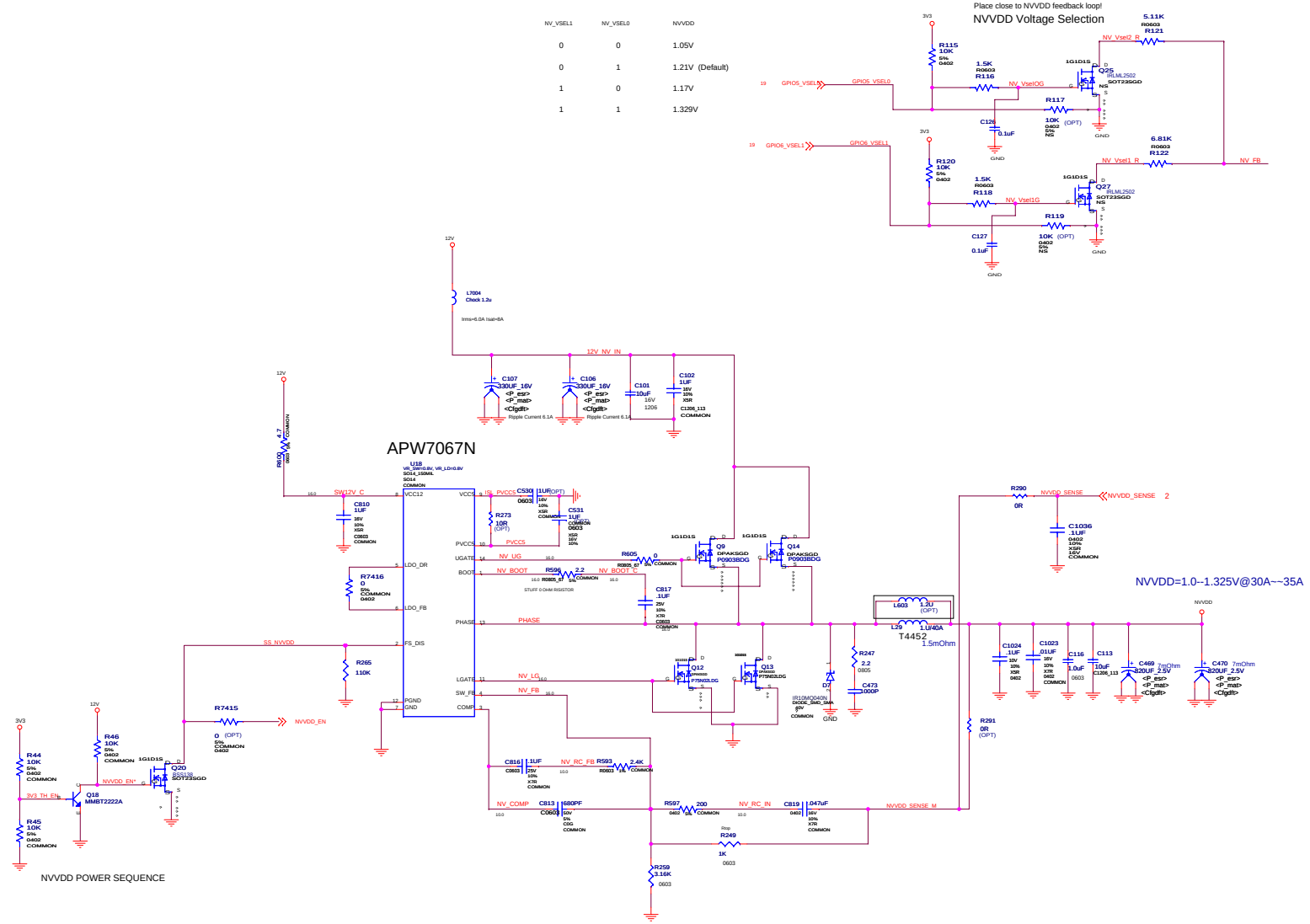
NVVDD

NV_VSEL1	NV_VSEL0	NVVDD
0	0	1.05V
0	1	1.21V (Default)
1	0	1.17V
1	1	1.329V



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NVVDD

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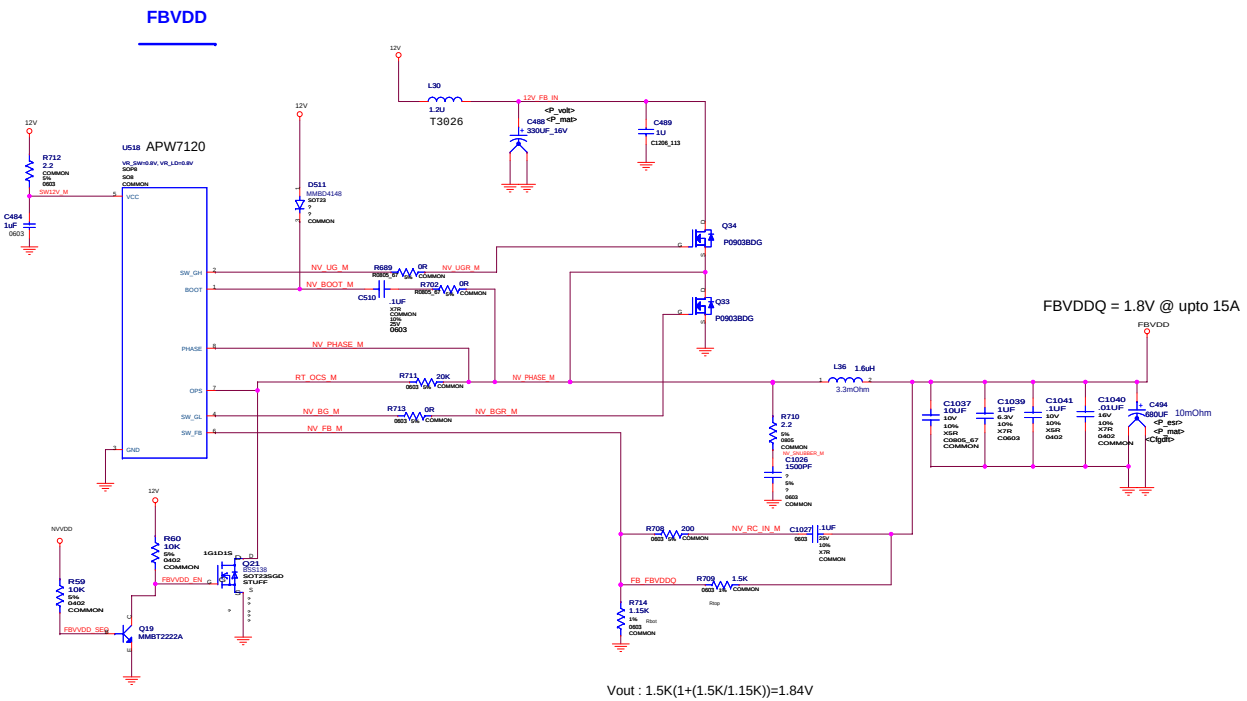
FBVDD



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FBVDD		
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