

MS-V013 VER 0A

NV-AGP NV44A 128MB, BGA 8MX16 DDR,VGA,DVI-I,TV-OUT(HT-10)

P362: NV44A, TSOP MEMORY x16

- Page1: P362 Overview
- Page2: AGP Interface
- Page3: Frame Buffer Interface
- Page4: Memory 1st bank 0..31
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- Page12: VIDEO CAPTURE: SAA7115
- Page13: PowerSupplyI: NVVDD, FBVDDQ
- Page14: PowerSupplyII: 5V, DDC5V, F3V3, TMDS\_PLLVDD
- Page15: VIDEO CONNECTORS: MiniDIN, 2x6 HDR

REV HISTORY

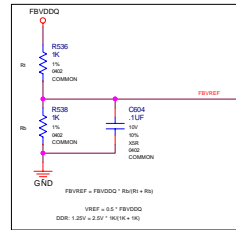
A01

- 1/31/2005:
- 1.PAGE12:VIDEO CAPTURE: SAA7115  
Removed:  
U2  
C15,16,18,19,20,21,22,686,687,688,689,690,691,692,693,694,695,696,697,698,  
699,700,701,702,703,704,705,708,709,710,711,712,713,714,715,716,717,718  
R15,R16,R17,R20,R21,R653  
LB9,LB10,LB511
- 2.Changed Page6: DAC-A, DB15 Connector: DACA Sling-type CRT  
Removed:  
J4  
Add:  
J3001,J503
- 3.Changed Page7: DAC-B, MUX, DB15:DACB DVI-I  
Removed:  
J1
- 4.Removed Page15: VIDEO CONNECTORS: MiniDIN, 2x6 HDR: TV-IN( Pin1,2) Circuit  
Removed:  
LB3,LB4  
C7,C8  
R7,R8,R9,R10
- Change Page10: STRAPS, Mechanical Parts: STRAPS Footprint  
R640,641/ 595,601 / 596,602 / 643,644 / 651,652 / 647,648  
/ 649,650 / 645,646 / 598,604 / 597,603 / 631,632 / 606,608
- 6.Changed Page14: PowerSupplyII: 5V, DDC5V, A3V3, F3V3, TMDS\_PLLVDD :  
PWM Circuit R,L,C,Mos Cost Down  
Removed:  
R525  
L6,L7,L8  
Q3,Q4,Q6  
Add:  
R999,R1000,R1001,R1002  
C200,C201,C202,C203,C204,C205,C206,C207  
C1501,C1502  
Q10,Q11,Q12  
L805,L602

REV	VARIANT	NVPN	ASSEMBLY
0	BASE	800-83pp-xxxx-vvv	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	0000	800-10362-0000-000	NV44A, 392250, 128MB/64-66, 16Mx16, VGA+DVI+HDTV-out
2	0001	800-10362-0001-000	<UNDEFINED>
3	0002	800-10362-0002-000	<UNDEFINED>
4	0003	800-10362-0003-000	NV44A, 392250, 128MB/64-66, 16Mx16, VGA+DVI+HDTV-out, VIDEO IN
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>



## GPU: FB-Interface



### X-Caps for FB\_CMD BUS

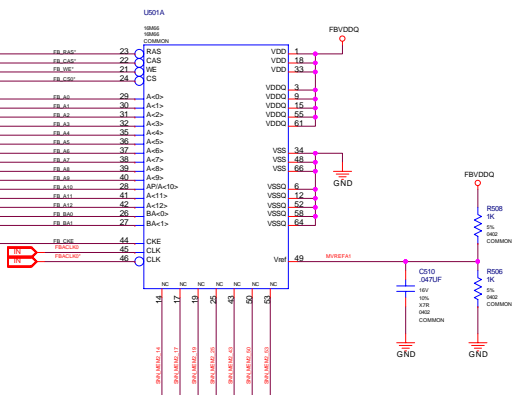
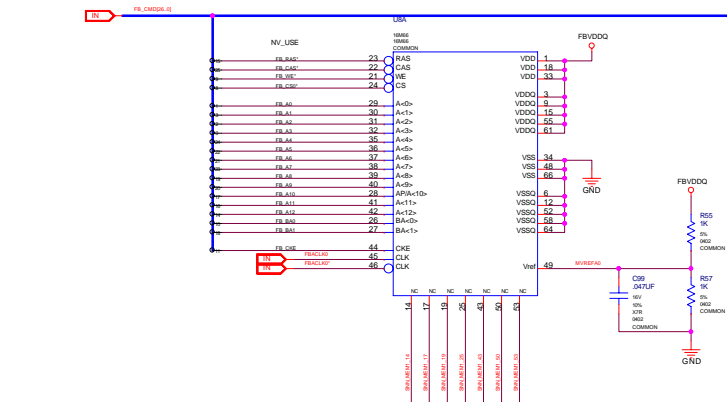
Four circuit diagrams are shown, each representing a different X-Cap connection for the FB\_CMD BUS. Each diagram includes a 10V supply, a capacitor (C105, C110, C307, or C308) with a value of 0.1uF, and a common rail (X18, X19, X20, or X21) connected to GND. The common rail is labeled 'X18 COMMON', 'X19 COMMON', 'X20 COMMON', and 'X21 COMMON' respectively.

# LABTESTPOINTS

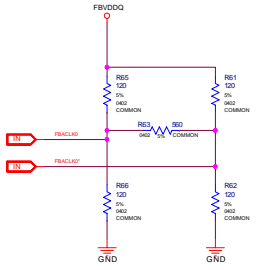
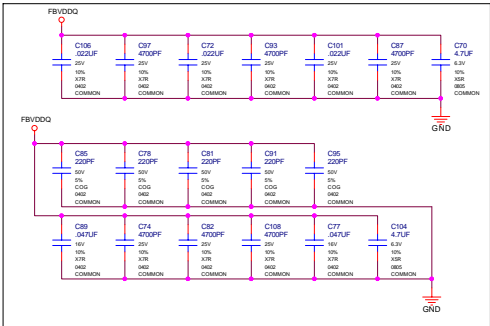
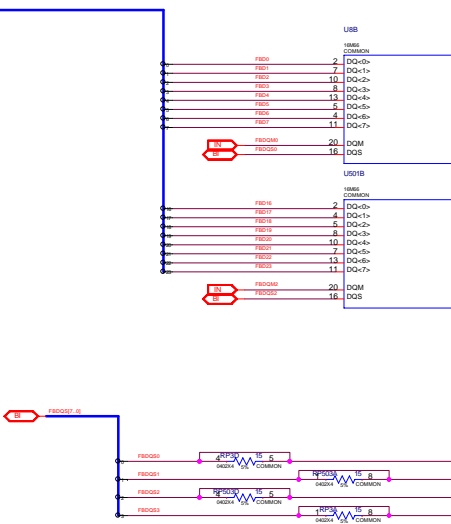
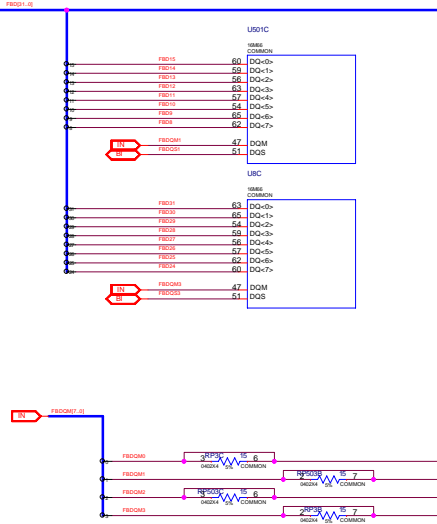
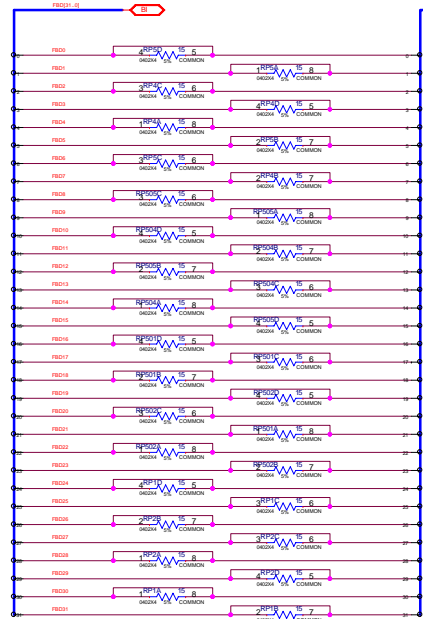
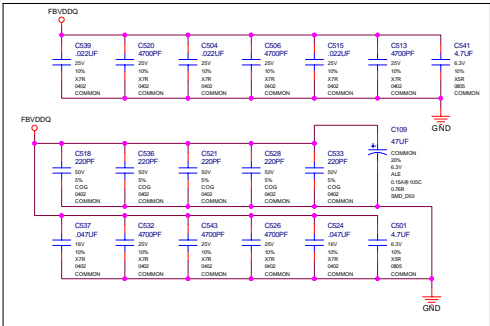
The diagram illustrates the connections for Lab Test Points. It features two main components, SP2 and SP1, each represented by a blue rounded rectangle. SP2 is located at the top right, and SP1 is at the bottom right. Between them are seven horizontal lines, each representing a test point. On the left side, there are seven blue rounded rectangles labeled T24, T22, T26, TP11, TP12, and T28. On the right side, there are two blue rounded rectangles labeled SP2 and SP1. The connections are as follows: T24 is connected to SP2 via a red line labeled F80030. T22 is connected to SP2 via a red line labeled F80031. T26 is connected to SP2 via a red line labeled F80032. TP11 is connected to SP1 via a red line labeled F80033. TP12 is connected to SP1 via a red line labeled F80034. T28 is connected to SP1 via a red line labeled F80035. There are also two red lines labeled F80036 and F80037 that do not connect to any of the labeled test points.

Test Point	Connection Label	Destination
T24	F80030	SP2
T22	F80031	SP2
T26	F80032	SP2
TP11	F80033	SP1
TP12	F80034	SP1
T28	F80035	SP1
	F80036	
	F80037	

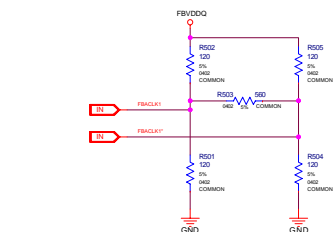
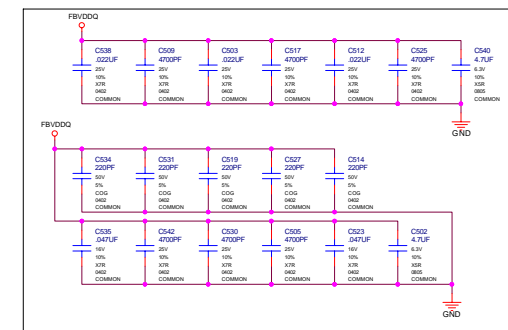
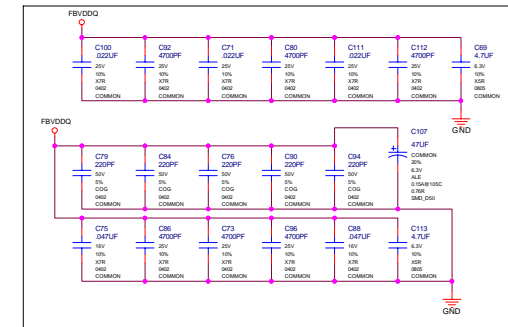
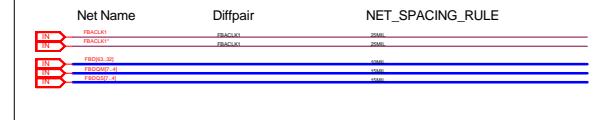
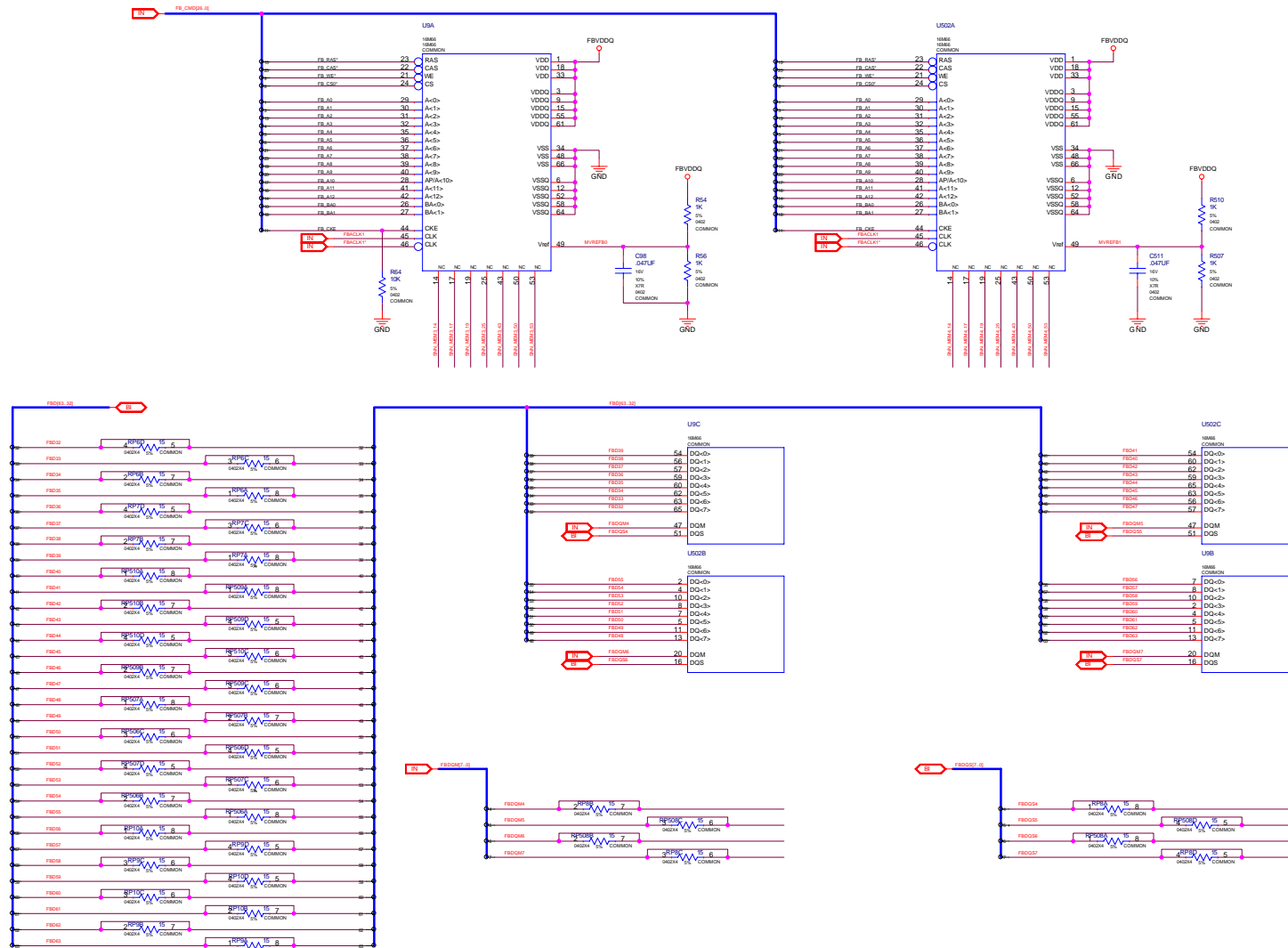
Memory Bit 0..31



Net Name	Diffpair	NET_SPACING_RULE
FBVDDQ	FBVDDQ	30MIL
VDDQ	VDDQ	30MIL
VSSQ	VSSQ	30MIL
FBVDDQ	FBVDDQ	30MIL
VDDQ	VDDQ	30MIL
VSSQ	VSSQ	30MIL

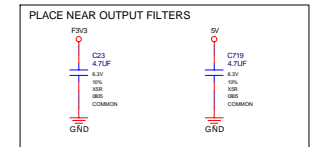
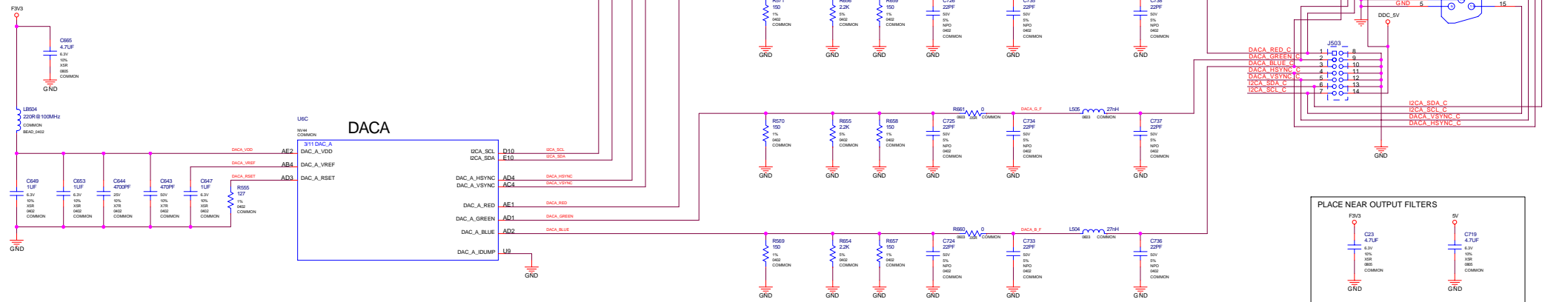
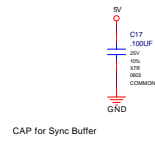


## Memory Bit 32..63

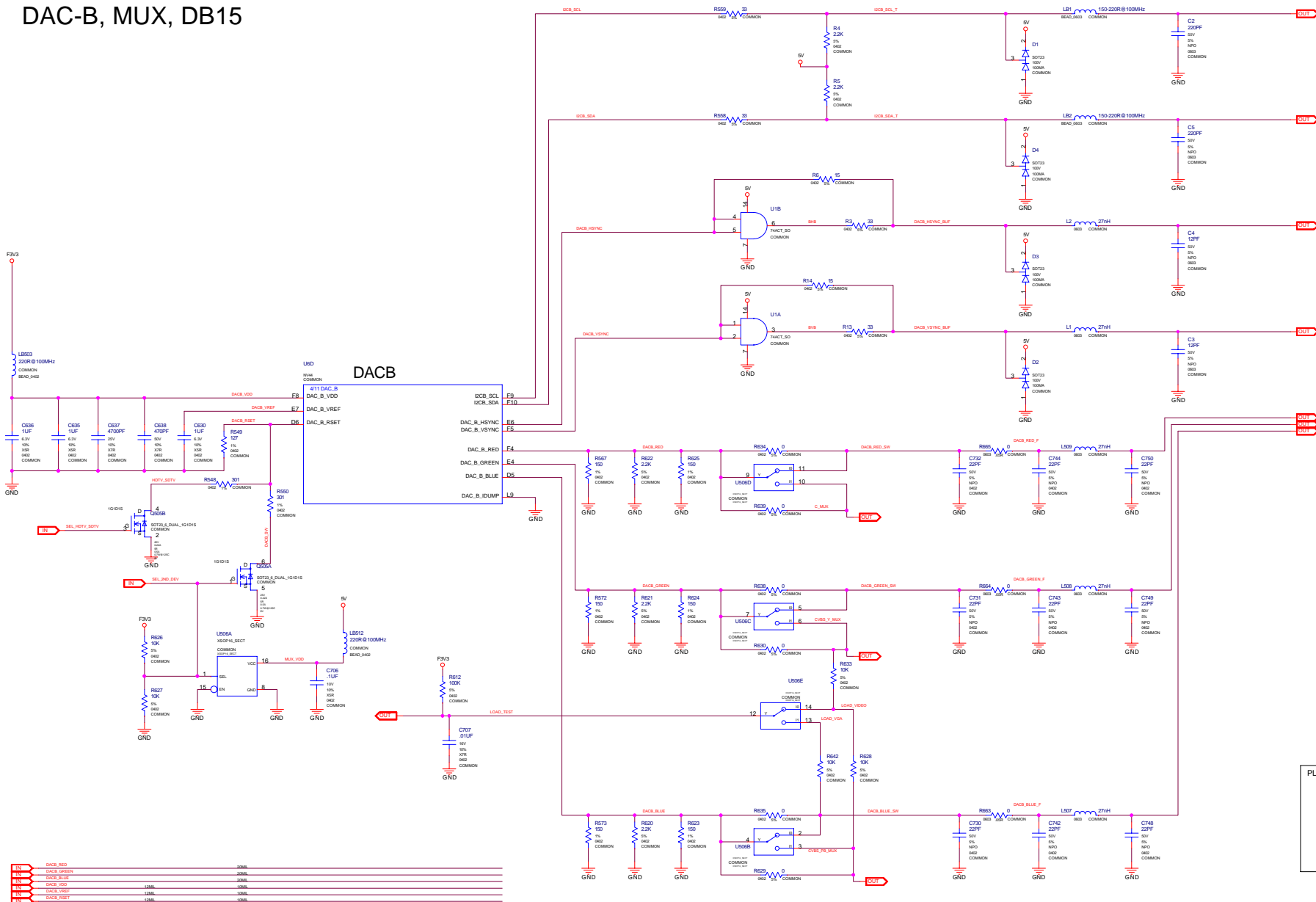


## DAC-A, DB15 Connector

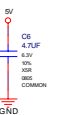
	Net Name	MIN_LINE_WIDTH	NET_SPACING_TYPE
100	SDA_001	100M	100M
100	SDA_002	100M	100M
100	SDA_003	100M	100M
100	SDA_004	100M	100M
100	SDA_005	100M	100M
100	SDA_006	100M	100M
100	SDA_007	100M	100M
100	SDA_008	100M	100M
100	SDA_009	100M	100M
100	SDA_010	100M	100M
100	SDA_011	100M	100M
100	SDA_012	100M	100M
100	SDA_013	100M	100M
100	SDA_014	100M	100M
100	SDA_015	100M	100M
100	SDA_016	100M	100M
100	SDA_017	100M	100M
100	SDA_018	100M	100M
100	SDA_019	100M	100M
100	SDA_020	100M	100M
100	SDA_021	100M	100M
100	SDA_022	100M	100M
100	SDA_023	100M	100M
100	SDA_024	100M	100M
100	SDA_025	100M	100M
100	SDA_026	100M	100M
100	SDA_027	100M	100M
100	SDA_028	100M	100M
100	SDA_029	100M	100M
100	SDA_030	100M	100M
100	SDA_031	100M	100M
100	SDA_032	100M	100M
100	SDA_033	100M	100M
100	SDA_034	100M	100M
100	SDA_035	100M	100M
100	SDA_036	100M	100M
100	SDA_037	100M	100M
100	SDA_038	100M	100M
100	SDA_039	100M	100M
100	SDA_040	100M	100M
100	SDA_041	100M	100M
100	SDA_042	100M	100M
100	SDA_043	100M	100M
100	SDA_044	100M	100M
100	SDA_045	100M	100M
100	SDA_046	100M	100M
100	SDA_047	100M	100M
100	SDA_048	100M	100M
100	SDA_049	100M	100M
100	SDA_050	100M	100M
100	SDA_051	100M	100M
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100	SDA_060	100M	100M
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100	SDA_067	100M	100M
100	SDA_068	100M	100M
100	SDA_069	100M	100M
100	SDA_070	100M	100M
100	SDA_071	100M	100M
100	SDA_072	100M	100M
100	SDA_073	100M	100M
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100	SDA_076	100M	100M
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100	SDA_081	100M	100M
100	SDA_082	100M	100M
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100	SDA_084	100M	100M
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100	SDA_089	100M	100M
100	SDA_090	100M	100M
100	SDA_091	100M	100M
100	SDA_092	100M	100M
100	SDA_093	100M	100M
100	SDA_094	100M	100M
100	SDA_095	100M	100M
100	SDA_096	100M	100M
100	SDA_097	100M	100M
100	SDA_098	100M	100M
100	SDA_099	100M	100M
100	SDA_100	100M	100M



## DAC-B, MUX, DB15

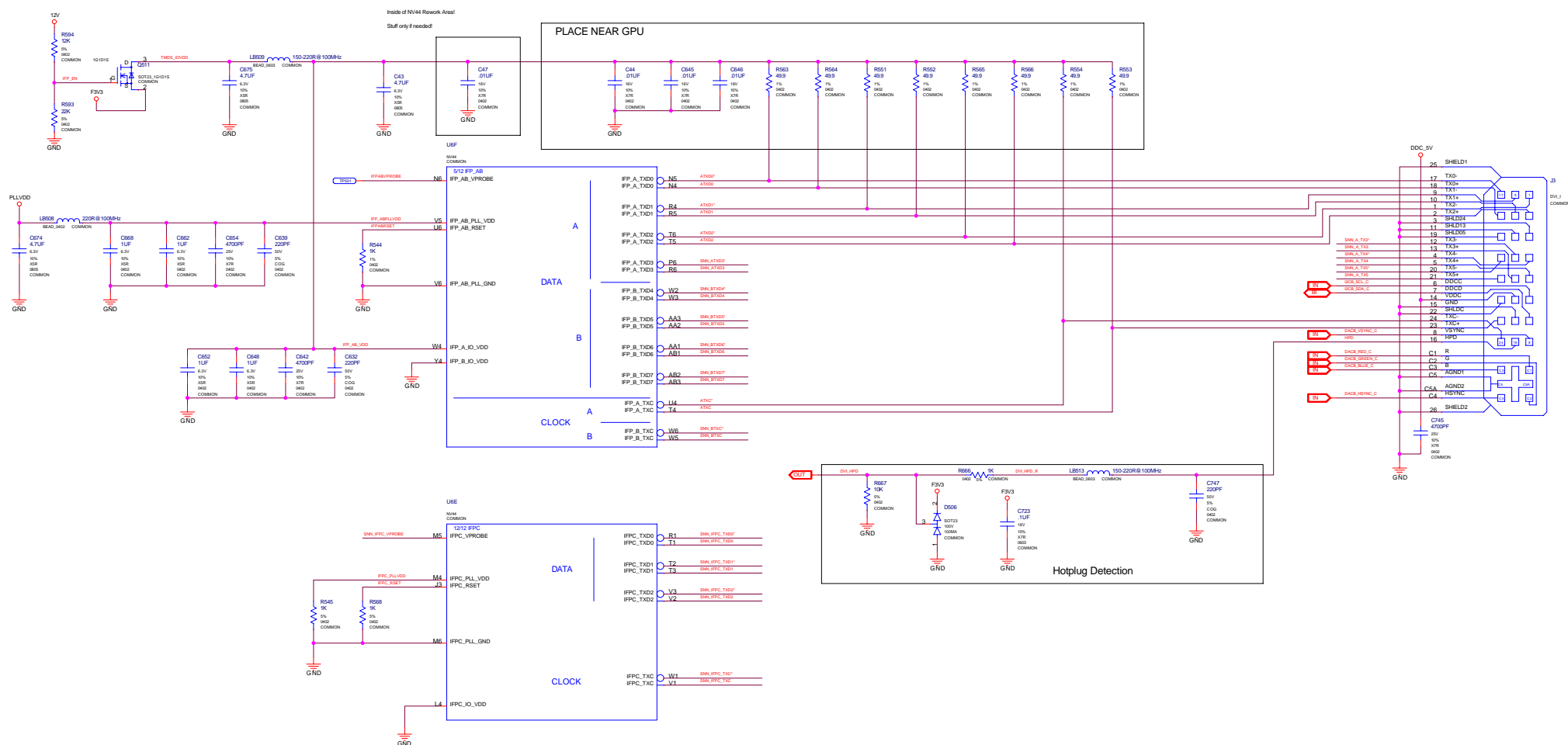


PLACE NEAR OUTPUT FILTERS



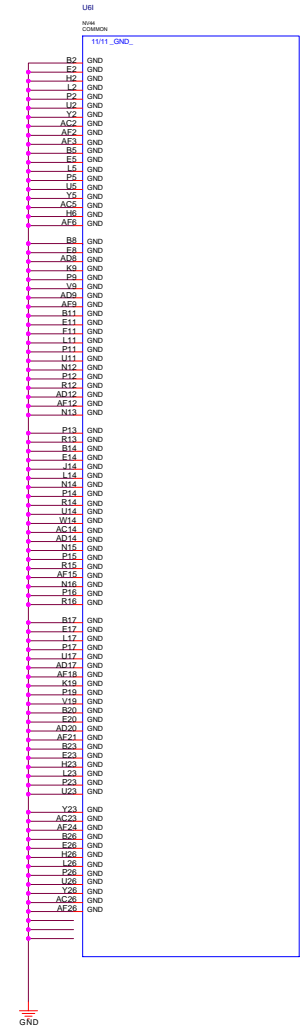
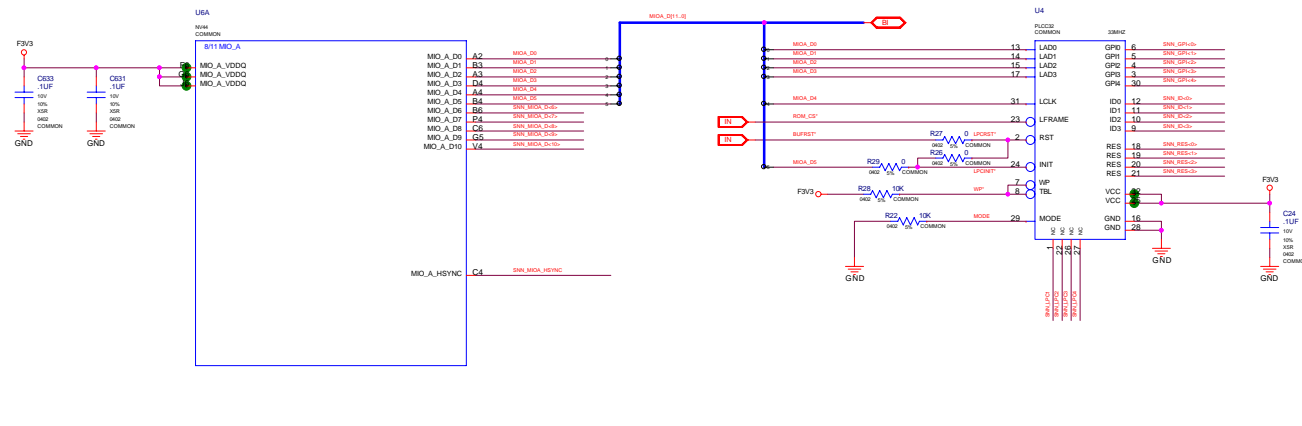
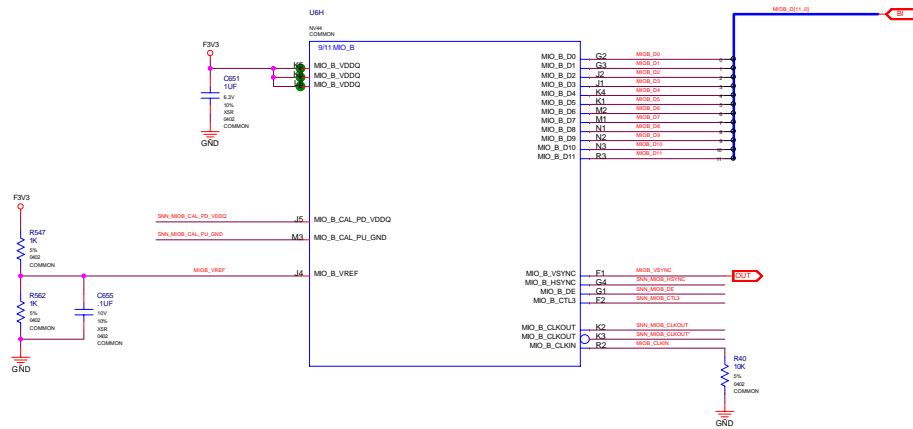
Internal TMDS, DVI-Connector

Net Name	Diffpair	NET_SPACING_RULE	Voltage
Net1	DIFF_PAIR1_VDD		3.3V
Net2	DIFF_PAIR2_VDD		3.3V
Net3	DIFF_PAIR3_VDD		3.3V
Net4	DIFF_PAIR4_VDD		3.3V
Net5	DIFF_PAIR5_VDD		3.3V
Net6	DIFF_PAIR6_VDD		3.3V
Net7	DIFF_PAIR7_VDD		3.3V
Net8	DIFF_PAIR8_VDD		3.3V
Net9	DIFF_PAIR9_VDD		3.3V
Net10	DIFF_PAIR10_VDD		3.3V
Net11	DIFF_PAIR11_VDD		3.3V
Net12	DIFF_PAIR12_VDD		3.3V
Net13	DIFF_PAIR13_VDD		3.3V
Net14	DIFF_PAIR14_VDD		3.3V
Net15	DIFF_PAIR15_VDD		3.3V
Net16	DIFF_PAIR16_VDD		3.3V
Net17	DIFF_PAIR17_VDD		3.3V
Net18	DIFF_PAIR18_VDD		3.3V
Net19	DIFF_PAIR19_VDD		3.3V
Net20	DIFF_PAIR20_VDD		3.3V
Net21	DIFF_PAIR21_VDD		3.3V
Net22	DIFF_PAIR22_VDD		3.3V
Net23	DIFF_PAIR23_VDD		3.3V
Net24	DIFF_PAIR24_VDD		3.3V
Net25	DIFF_PAIR25_VDD		3.3V
Net26	DIFF_PAIR26_VDD		3.3V
Net27	DIFF_PAIR27_VDD		3.3V
Net28	DIFF_PAIR28_VDD		3.3V
Net29	DIFF_PAIR29_VDD		3.3V
Net30	DIFF_PAIR30_VDD		3.3V
Net31	DIFF_PAIR31_VDD		3.3V
Net32	DIFF_PAIR32_VDD		3.3V
Net33	DIFF_PAIR33_VDD		3.3V
Net34	DIFF_PAIR34_VDD		3.3V
Net35	DIFF_PAIR35_VDD		3.3V
Net36	DIFF_PAIR36_VDD		3.3V
Net37	DIFF_PAIR37_VDD		3.3V
Net38	DIFF_PAIR38_VDD		3.3V
Net39	DIFF_PAIR39_VDD		3.3V
Net40	DIFF_PAIR40_VDD		3.3V
Net41	DIFF_PAIR41_VDD		3.3V
Net42	DIFF_PAIR42_VDD		3.3V
Net43	DIFF_PAIR43_VDD		3.3V
Net44	DIFF_PAIR44_VDD		3.3V
Net45	DIFF_PAIR45_VDD		3.3V
Net46	DIFF_PAIR46_VDD		3.3V
Net47	DIFF_PAIR47_VDD		3.3V
Net48	DIFF_PAIR48_VDD		3.3V
Net49	DIFF_PAIR49_VDD		3.3V
Net50	DIFF_PAIR50_VDD		3.3V
Net51	DIFF_PAIR51_VDD		3.3V
Net52	DIFF_PAIR52_VDD		3.3V
Net53	DIFF_PAIR53_VDD		3.3V
Net54	DIFF_PAIR54_VDD		3.3V
Net55	DIFF_PAIR55_VDD		3.3V
Net56	DIFF_PAIR56_VDD		3.3V
Net57	DIFF_PAIR57_VDD		3.3V
Net58	DIFF_PAIR58_VDD		3.3V
Net59	DIFF_PAIR59_VDD		3.3V
Net60	DIFF_PAIR60_VDD		3.3V
Net61	DIFF_PAIR61_VDD		3.3V
Net62	DIFF_PAIR62_VDD		3.3V
Net63	DIFF_PAIR63_VDD		3.3V
Net64	DIFF_PAIR64_VDD		3.3V
Net65	DIFF_PAIR65_VDD		3.3V
Net66	DIFF_PAIR66_VDD		3.3V
Net67	DIFF_PAIR67_VDD		3.3V
Net68	DIFF_PAIR68_VDD		3.3V
Net69	DIFF_PAIR69_VDD		3.3V
Net70	DIFF_PAIR70_VDD		3.3V
Net71	DIFF_PAIR71_VDD		3.3V
Net72	DIFF_PAIR72_VDD		3.3V
Net73	DIFF_PAIR73_VDD		3.3V
Net74	DIFF_PAIR74_VDD		3.3V
Net75	DIFF_PAIR75_VDD		3.3V
Net76	DIFF_PAIR76_VDD		3.3V
Net77	DIFF_PAIR77_VDD		3.3V
Net78	DIFF_PAIR78_VDD		3.3V
Net79	DIFF_PAIR79_VDD		3.3V
Net80	DIFF_PAIR80_VDD		3.3V
Net81	DIFF_PAIR81_VDD		3.3V
Net82	DIFF_PAIR82_VDD		3.3V
Net83	DIFF_PAIR83_VDD		3.3V
Net84	DIFF_PAIR84_VDD		3.3V
Net85	DIFF_PAIR85_VDD		3.3V
Net86	DIFF_PAIR86_VDD		3.3V
Net87	DIFF_PAIR87_VDD		3.3V
Net88	DIFF_PAIR88_VDD		3.3V
Net89	DIFF_PAIR89_VDD		3.3V
Net90	DIFF_PAIR90_VDD		3.3V
Net91	DIFF_PAIR91_VDD		3.3V
Net92	DIFF_PAIR92_VDD		3.3V
Net93	DIFF_PAIR93_VDD		3.3V
Net94	DIFF_PAIR94_VDD		3.3V
Net95	DIFF_PAIR95_VDD		3.3V
Net96	DIFF_PAIR96_VDD		3.3V
Net97	DIFF_PAIR97_VDD		3.3V
Net98	DIFF_PAIR98_VDD		3.3V
Net99	DIFF_PAIR99_VDD		3.3V
Net100	DIFF_PAIR100_VDD		3.3V



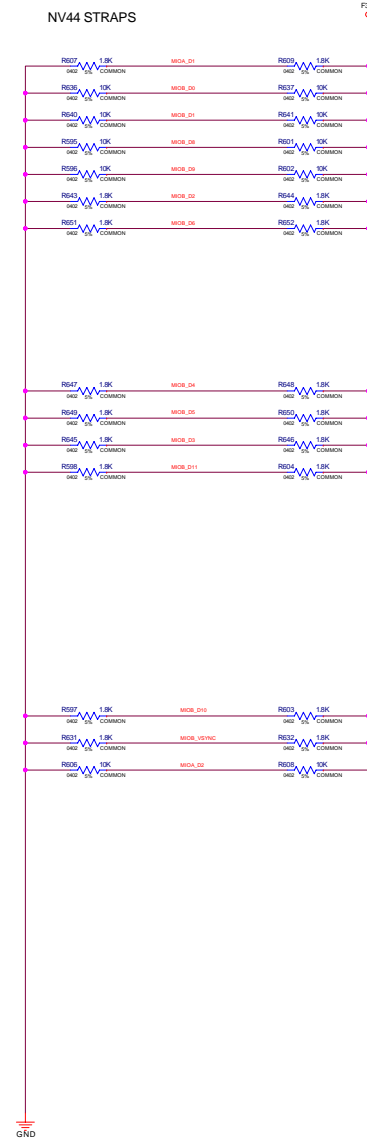
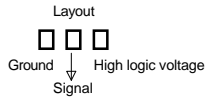


## MIOA, MIOB Interface, LPC-ROM

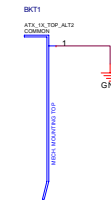
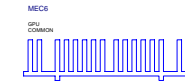


## STRAPS, Mechanical Parts

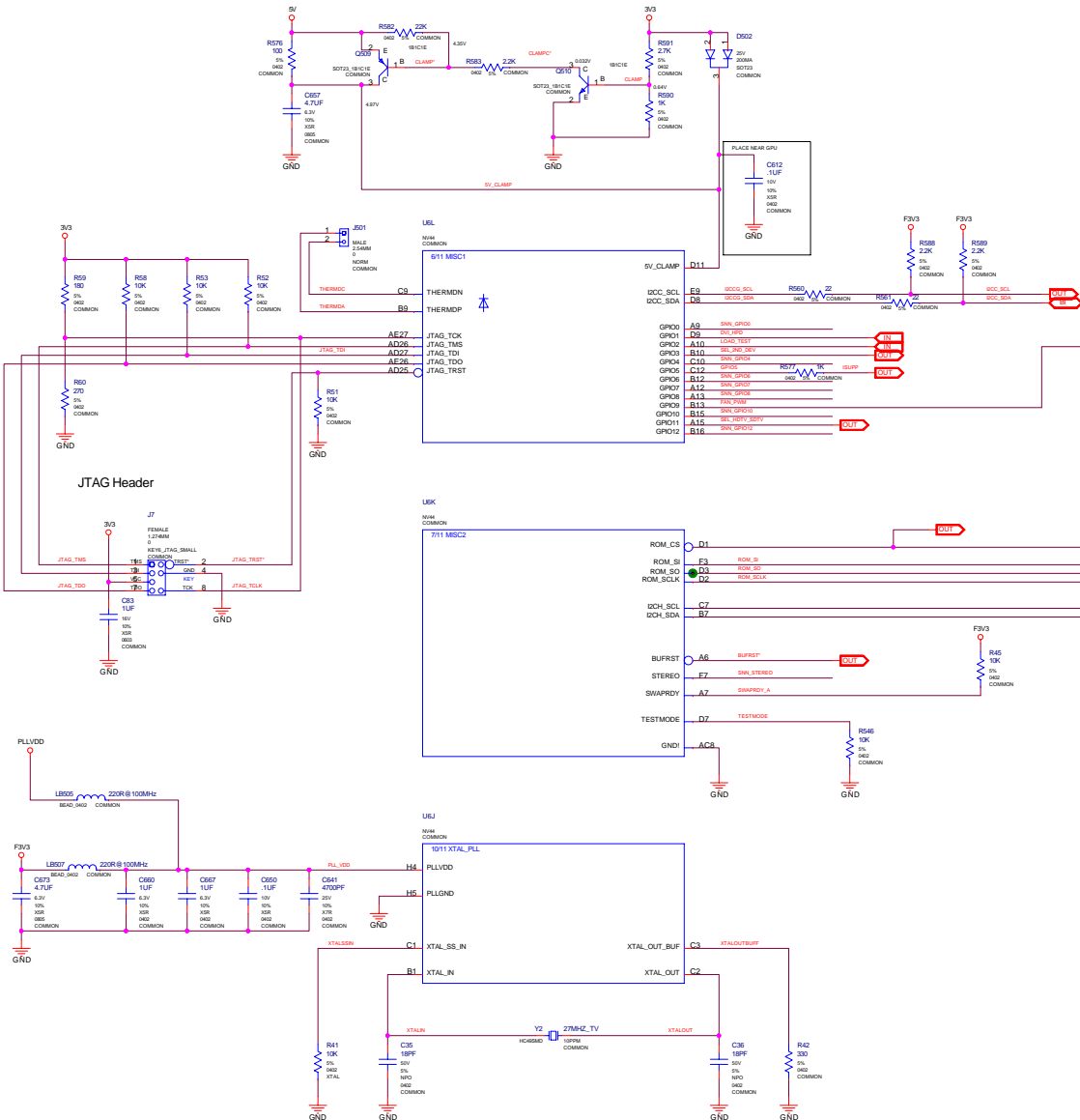
Overlap pads to save space  
and to prevent assembly of  
both resistors.



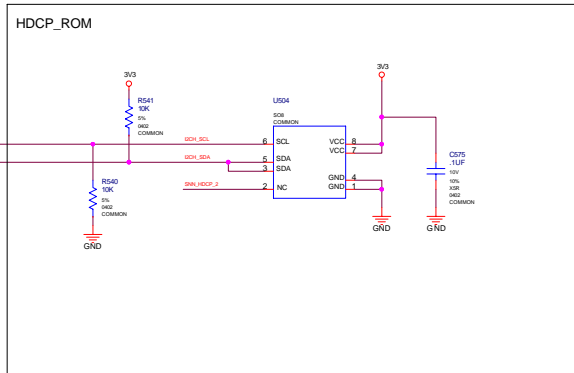
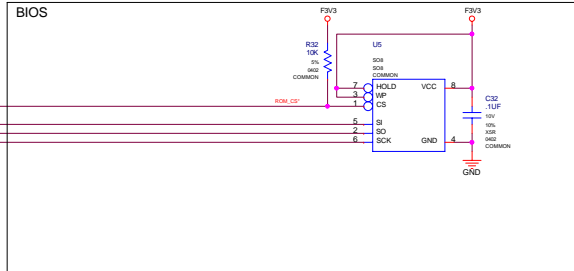
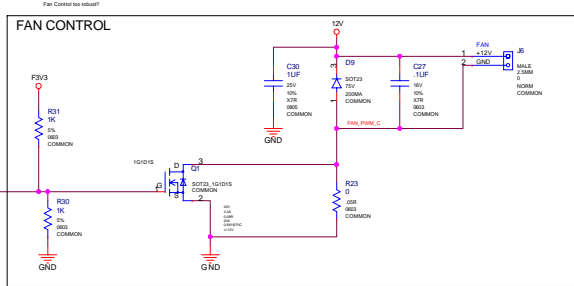
Bit	Signal	Values
00	PCI_AD_STAMP	0 UNVERGISED 1 NORMAL
01	SUB_VENDOR	0 END_BIOS 1 BIOS FROM BIOS
02	RAM_CFG_0	See <a href="http://support.lenovo.com/Project/...AfterQuietStop_Table for details">http://support.lenovo.com/Project/...AfterQuietStop_Table for details</a>
03	RAM_CFG_1	
04	RAM_CFG_2	
05	RAM_CFG_3	
06	CRYSTL_0	00 13.500 MHz 01 14.28518 MHz 02 27.000 MHz 03 UNKNOWN
22	CRYSTL_1	
07	TV_MODE_0	00 SECAM 01 NTSC 02 PAL 11 CRT
08	TV_MODE_1	
09	ASPI_30_3s	0 ASPIN ENABLED 1 ASPIN DISABLED
10	ASPI_38A	0 SBA ENABLED 1 SBA DISABLED
11	ASPI_FASTWIN	0 FFW ENABLED 1 FFW DISABLED
12	PCI_DEV0_0	0000 (always factory image)
13	PCI_DEV0_1	
20	PCI_DEV0_2	
21	PCI_DEV0_3	
14	BUS_TYPE	0 PCI 1 AGP
15	FP_SPACE	0 2MB 1 128M (DEFAULT)
23	FL_0	0 0MB 01 128M 10 256M (DEFAULT) 11 512M
24	FL_1	
25	BR	0 BRIDGE DISABLED 1 BRIDGE ENABLED
26	BR_10M	BR BITS KNOWN IF BRIDGE IS DISABLED
27	BR_AGP	
28	BR_3D	
29	ROM_TYPE_0	00 UNWALLED 01 SERIAL_A22F 10 SERIAL_A204GP 11 LPC
30	ROM_TYPE_1	
16	USER_0	0000 (DEFAULT)
17	USER_1	
18	USER_2	
19	USER_3	
FEL_FIL_EN_TERM100		
SIOF_FIOFIO_LST_ADDR[0]		
SIOF_FIOFIO_LST_ADDR[1]		



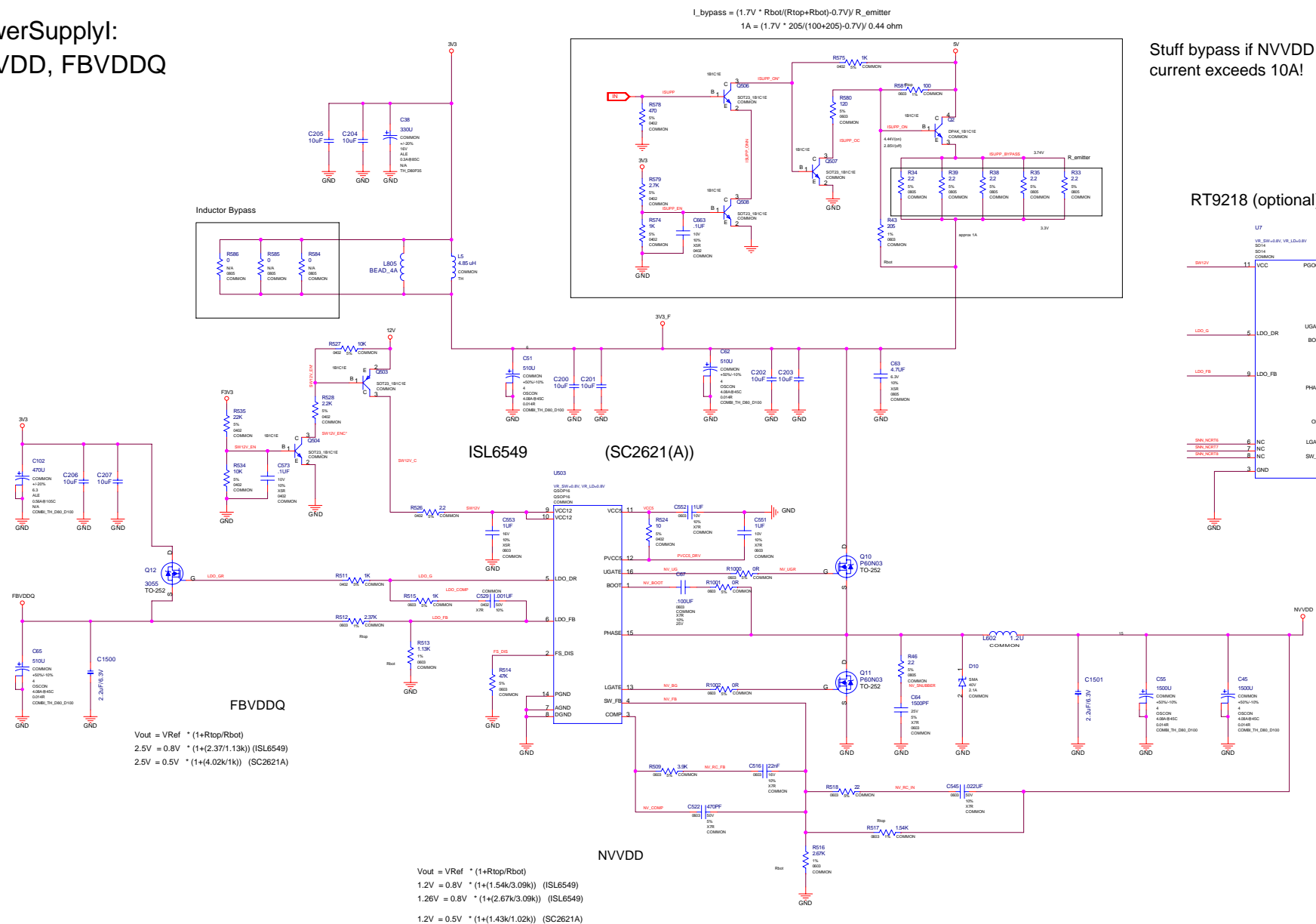
XTAL, GPIO, BIOS, Fan Control, JTAG Headers



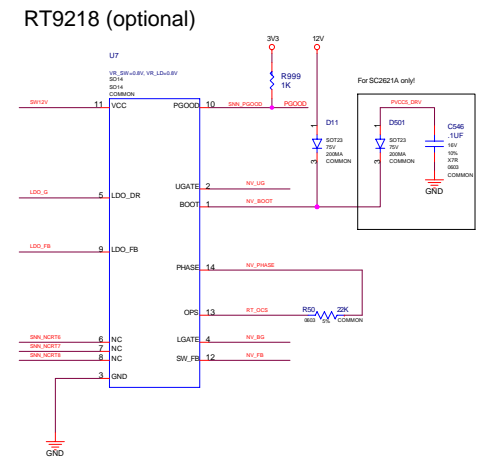
Net Name	NET_PHYSICAL_TYPE	NET_SPACING_RULE
XTALIN	SMALL_TRACE	20MIL
XTALOUT	SMALL_TRACE	20MIL
PLLVD0	SMALL_TRACE	20MIL
PLLVD1	SMALL_TRACE	20MIL



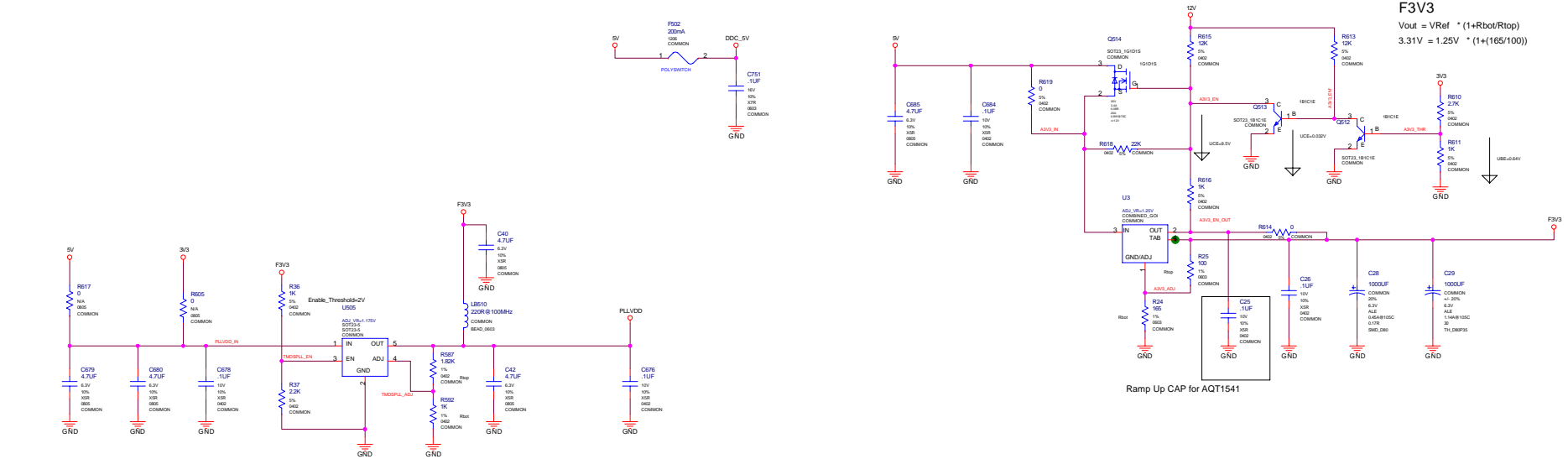
PowerSupply:  
NVVDD, FBVDDQ



Stuff bypass if NVVDD  
current exceeds 10A!



# PowerSupplyII: DDC5V, F3V3, TMDS\_PLLVDD



TMDS\_PLLVDD  
 $V_{out} = V_{Ref} \cdot (1 + R_{top}/R_{bot})$   
 $3.31V = 1.175V \cdot (1 + (1.82k/1k))$

Net Name	NET_PHYSICAL_TYPE	Voltage
5V	120A	5V
DDC_5V	120A	5V
F3V3	120A	3.3V
PLLVD	120A	3.3V
12V_IN	120A	12V

SV\_FUSED

125ns

500ns

