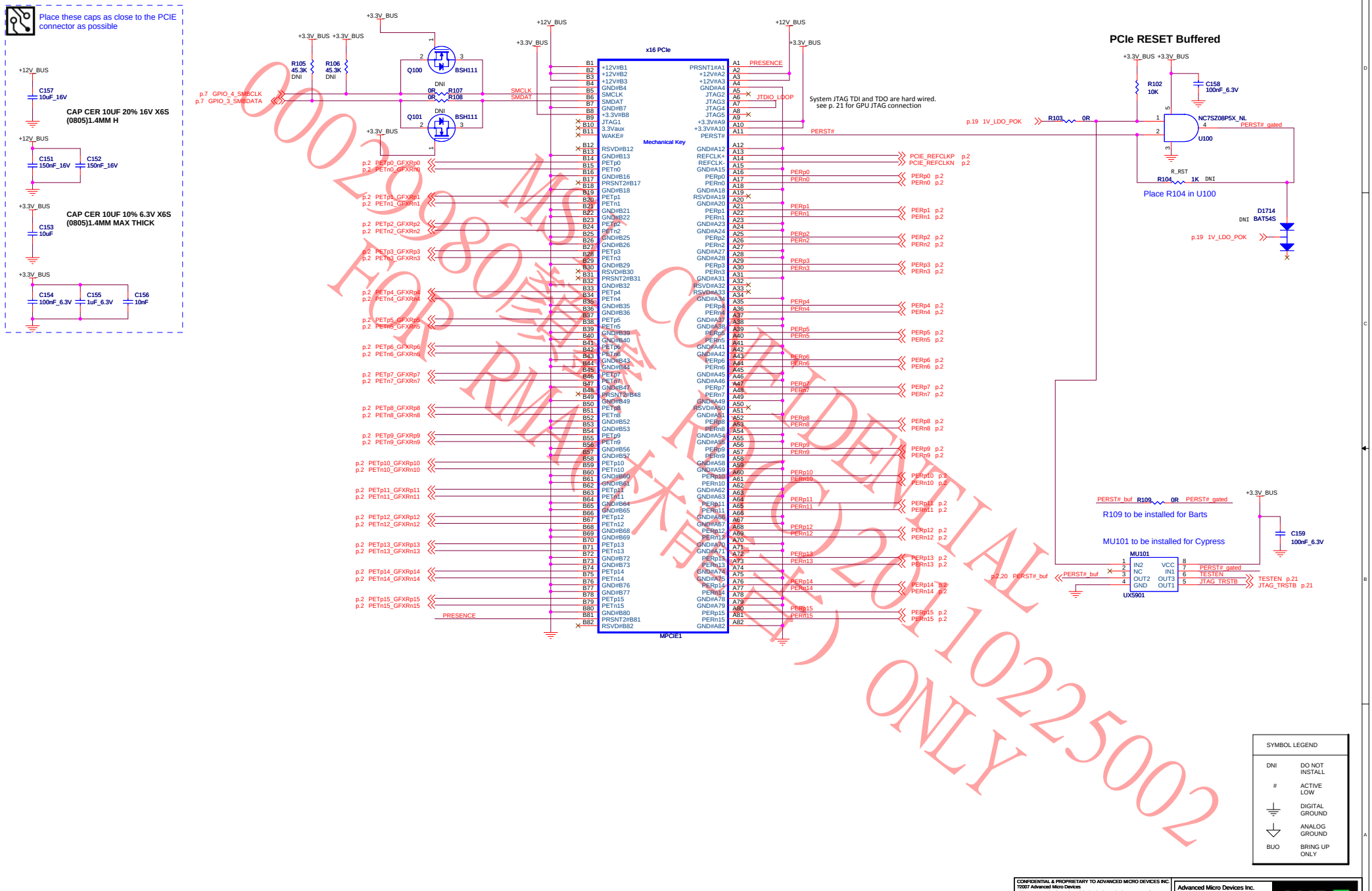
PCI-EXPRESS EDGE CONNECTOR

Koopa



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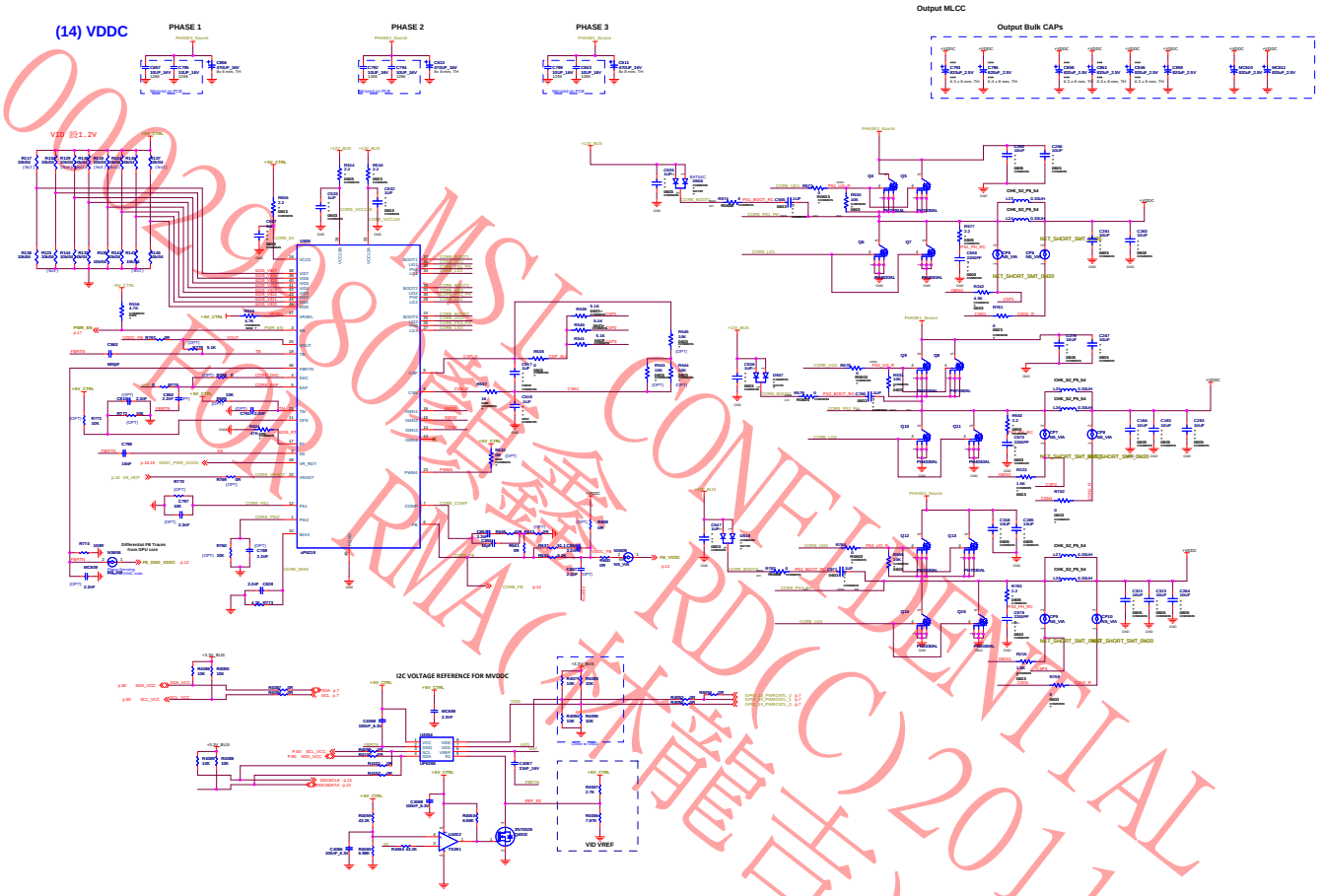
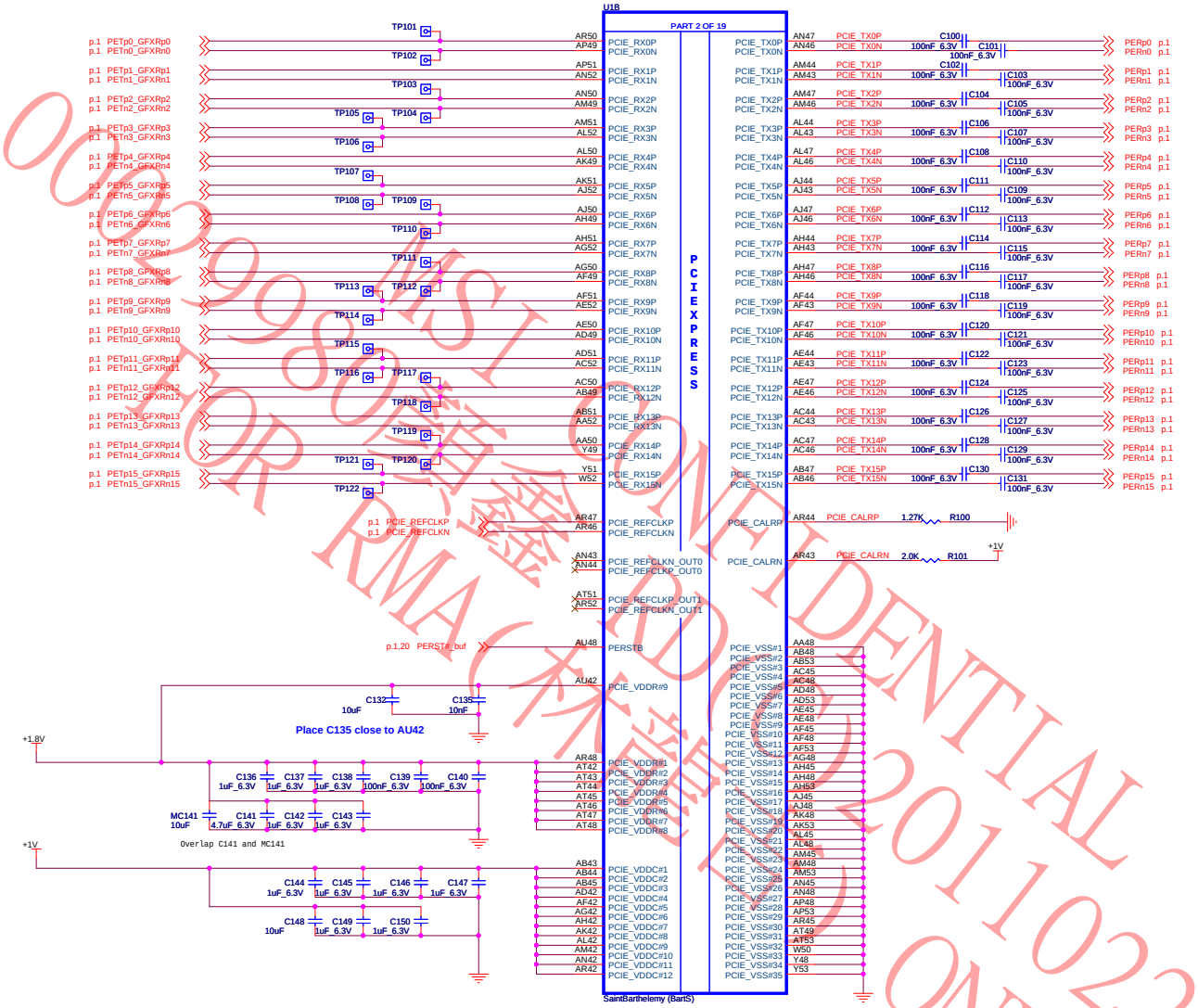


(2) BARTS PCIE Interface

NOTE: Some of the PCIE testpoints will be available through vias on traces.



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Title	ASIC PCIE Interface
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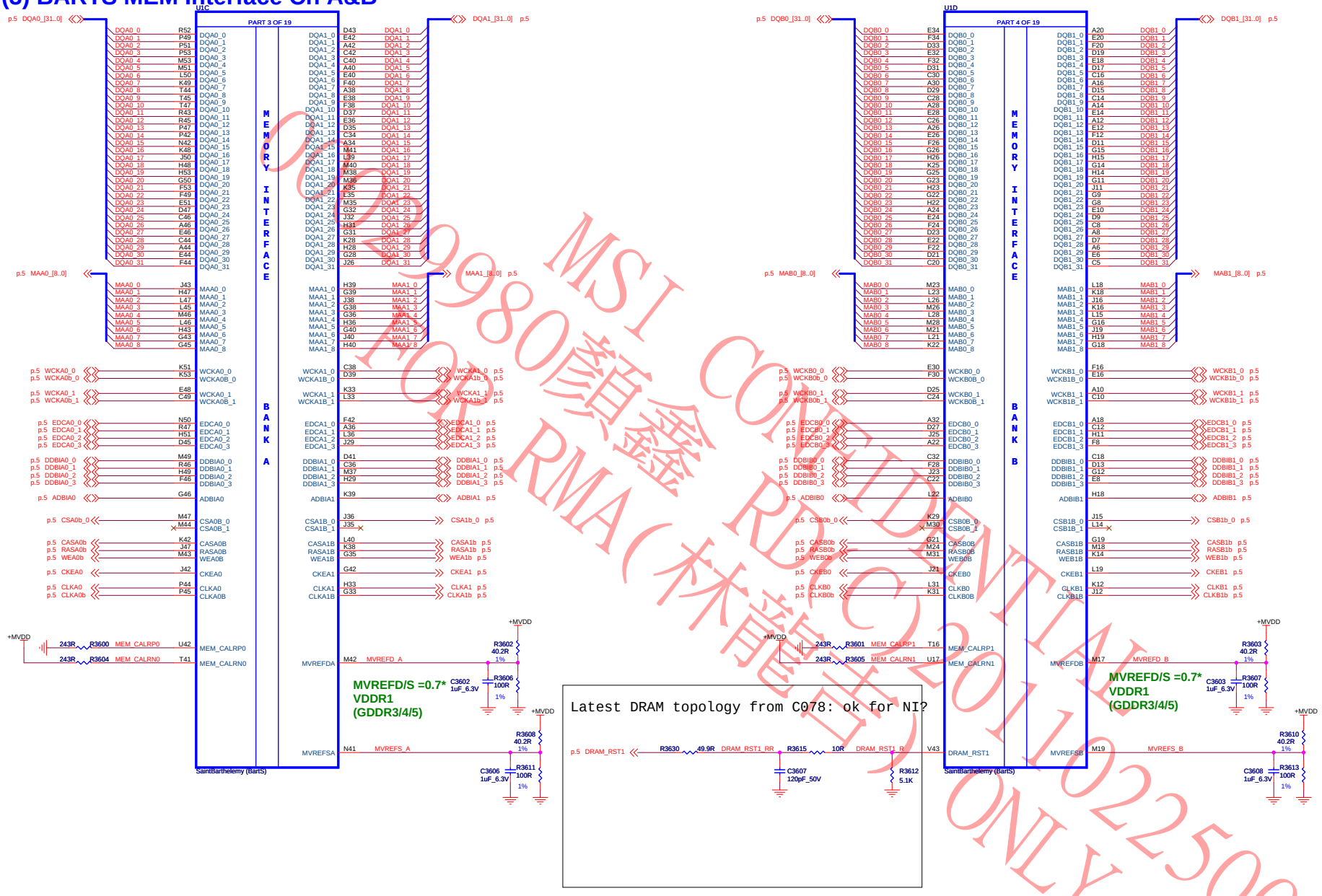
(3) BARTS MEM Interface Ch A&B



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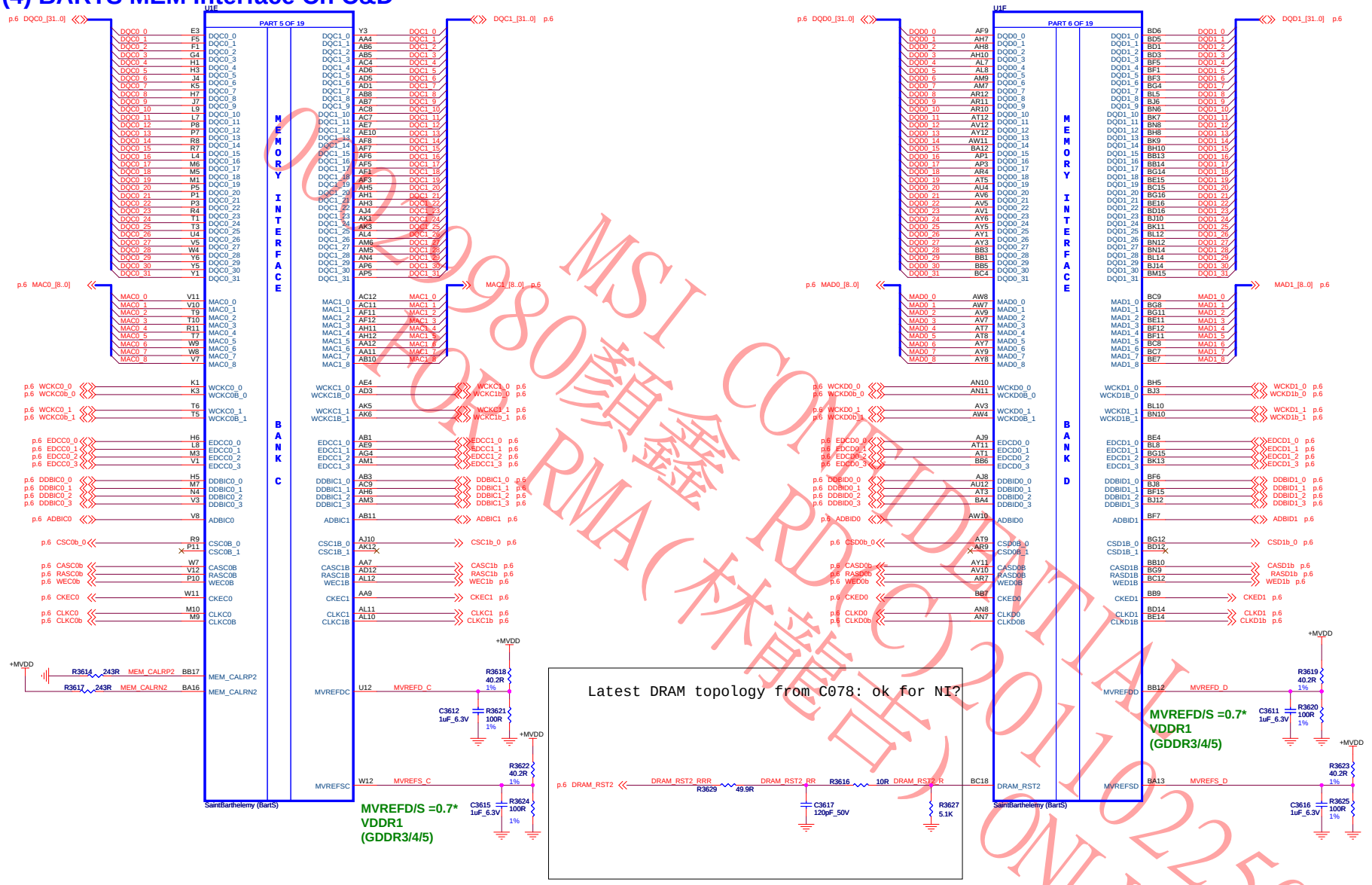
(4) BARTS MEM Interface Ch C&D



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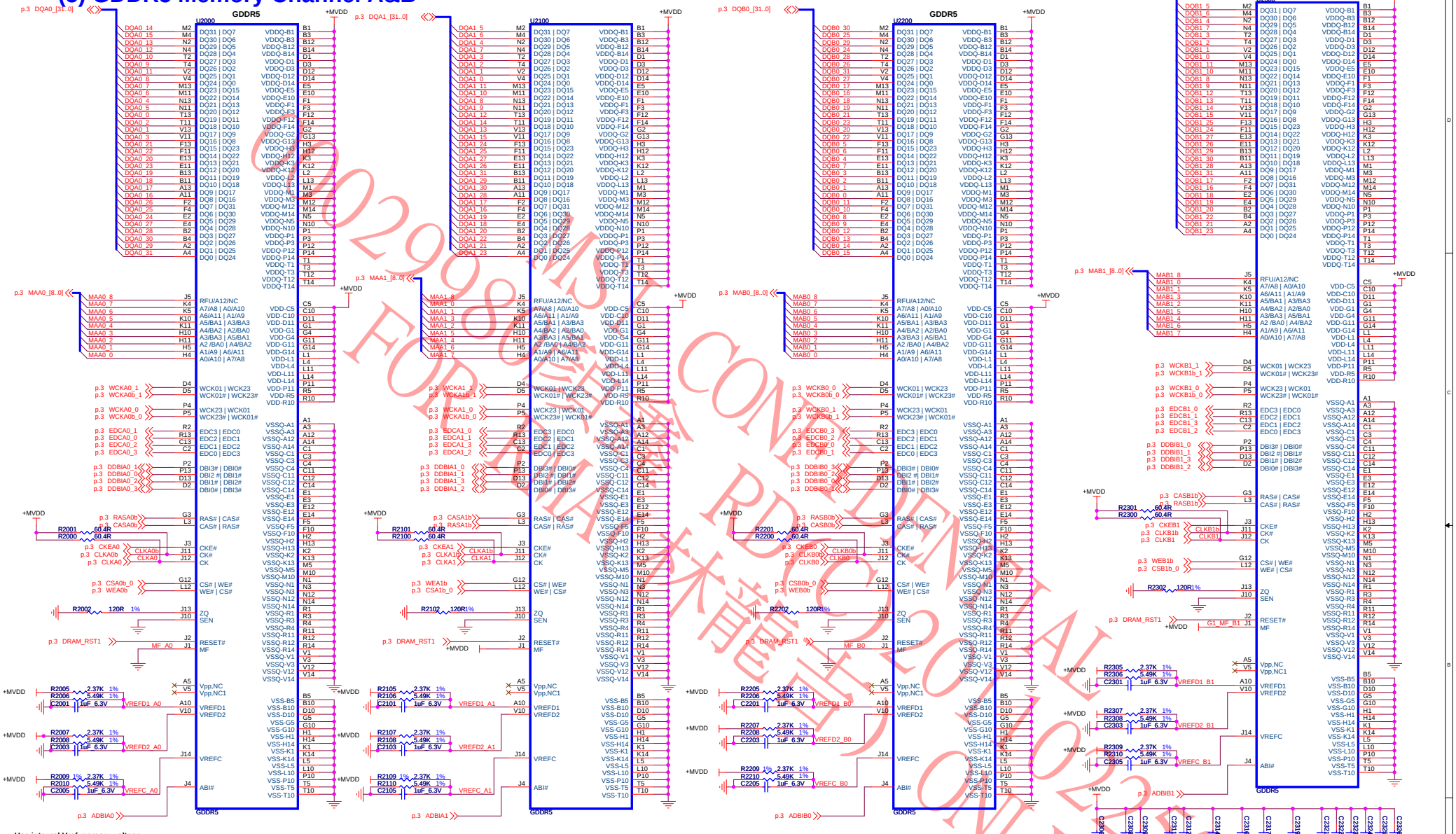
(5) GDDR5 Memory Channel A&B



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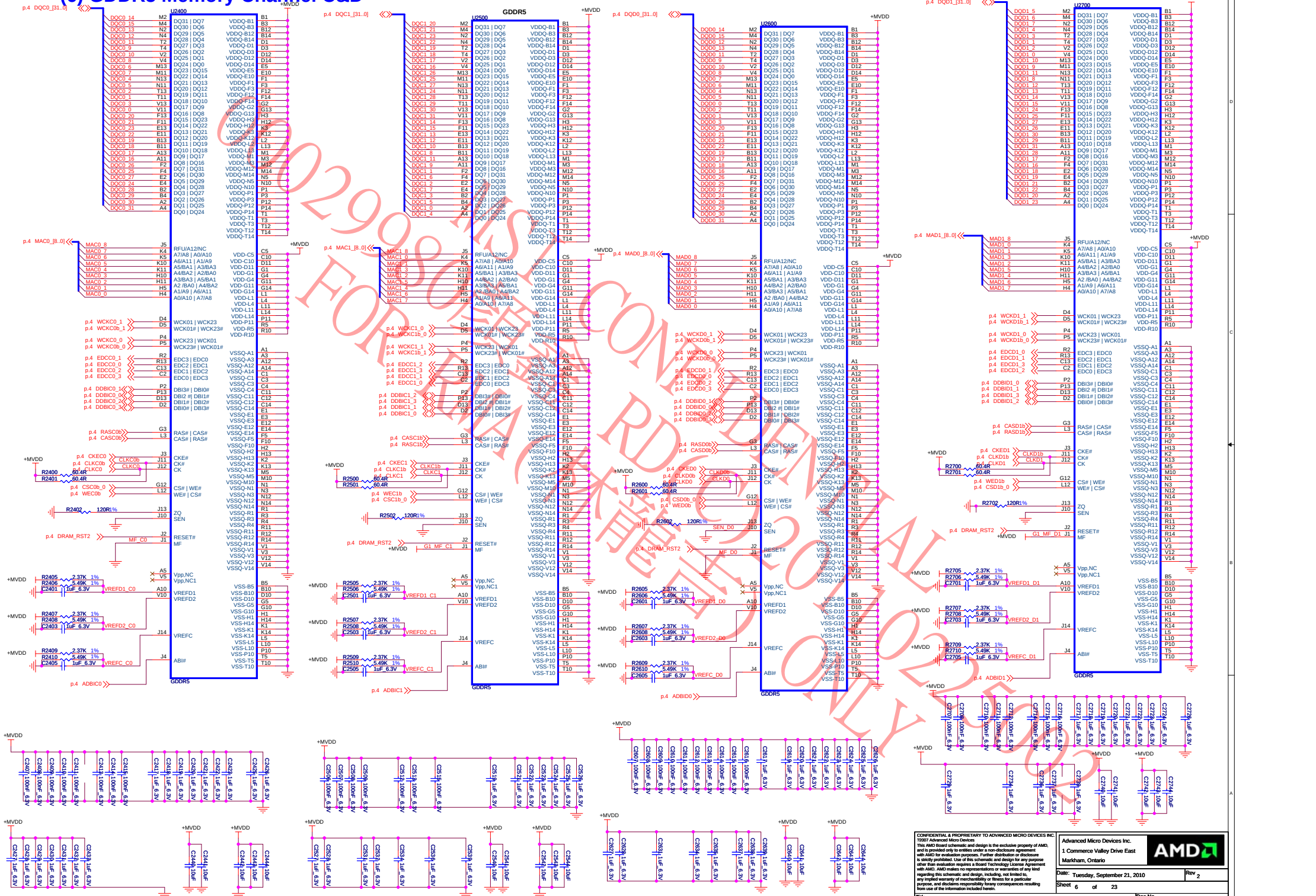
(6) GDDR5 Memory Channel C&D



(07) BARTS GPIOs Strap CF XTAL OSC

PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

SCL / SDA BUS:

I2C Address	Function	Device
0x0A	VDDC REG	

DDC6 BUS:

I2C Address	Function	Device
0x98	LM96163 - External Temperature Sensor	LM96163

DDC6_CLK 原本接去P21
LM96163 FOR BACKUP THERMAL CONTROL

PWRGOOD must be connected to GND for normal operation

PIN BASED STRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

VGA DISABLE : 1 for disable (set to 0 for normal operation)

GPIO(13,12,11) - CONFIG[2..0]

CONFIG[2]	100 - 512Kbit	M25P05A	(ST)
	101 - 1Mbit	M25P10A	(ST)
CONFIG[1]	101 - 2Mbit	M25P20	(ST)
	101 - 4Mbit	M25P40	(ST)
CONFIG[0]	101 - 8Mbit	M25P80	(ST)
	100 - 512Kbit	Pm25LV512	(Chingis)
	101 - 1Mbit	Pm25LV010	(Chingis)

VIP_DEVICE_STRAP_DIS
V2SYNC H2SYNC ?

RESERVED:
Internal use only. Other logic must not affect these signals during RESET.

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

RESERVED:
STRAP_BIOS_ROM_EN
CLKREQ# that requires open drain connection, and cannot be used as pinstrap
Don't set high at reset

Internal use only. Other logic must not affect these signals during RESET.

CrossFire Card-Edge

Lower Cable Card Edge

Place the crossfire testpoints near the ASIC and not the connector

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

Keep XIN_OSC and XOUT_OSC as short as possible to minimize stray capacitance

Overlap R26 and R19

Divider for 1.8V signaling.

route 50ohms single-ended/100ohms diff and keep short

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Title	ASIC GPIO, STRAPS,CF, and XTAL
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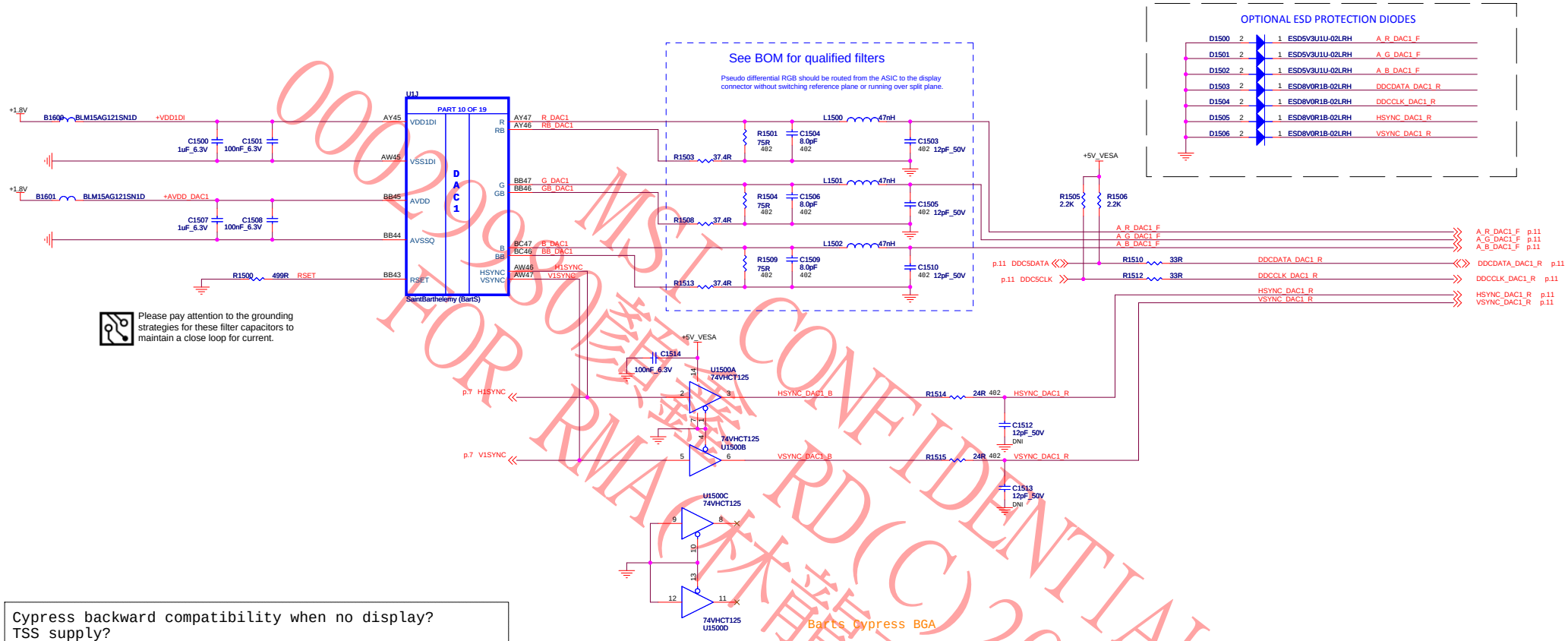
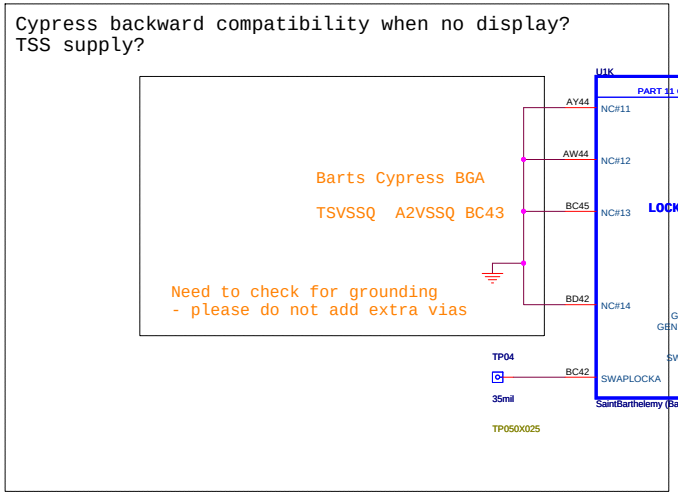
(08) BARTS DAC1





Barts Cypress BGA

NC B2 BG40
NC B2B BF40
NC COMP BE40
NC G2 BG43
NC G2B BF43
NC R2 BG42
NC R2B BF42
SWAPLOCKA R2SET BC42
NC A2VDD BD42
NC A2VDDQ BC45
NC VDD2DI AY44
NC VSS2DI AW44
GENLK_CLK H2SYNC BG38
GENLK_VSYNC V2SYNC BG39
TSVSSQ A2VSSQ BC43
SWAPLOCKB Y BE43
NC C BE42

RSVD NM_VDDC AM19
RSVD NM_VDDCI AR19
RSVD NM_VDDR1 AN18
RSVD NM_VSS AM18
RSVD NM_VSS AN19
RSVD NM_VSS AR18

VSS VSS_MECH (12x)

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Title Power Management

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(09) BARTS TMDS A&B

1.8V to be merged:
which bead to use in case of merge? 1 bead for all the rails?

1.0V to be merged:
which bead to use in case of merge? 1 bead for all the rails?

Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

U1L
PART 12 OF 19
TMDP A/B
SaintBarthelemy (BartS)

Optional ESD protection dioes

TOP

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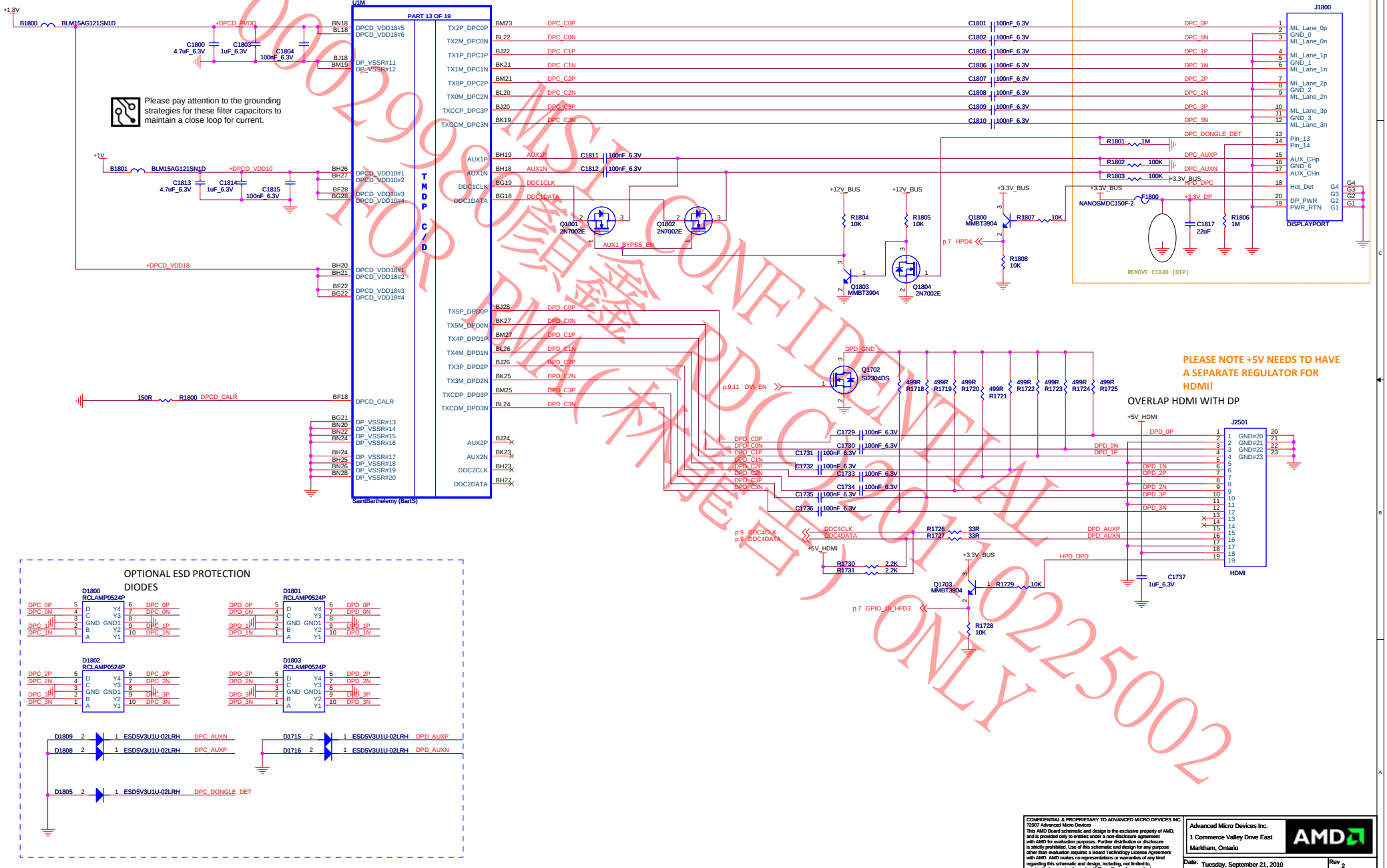
(10) BARTS Display Port/HDMI C&D



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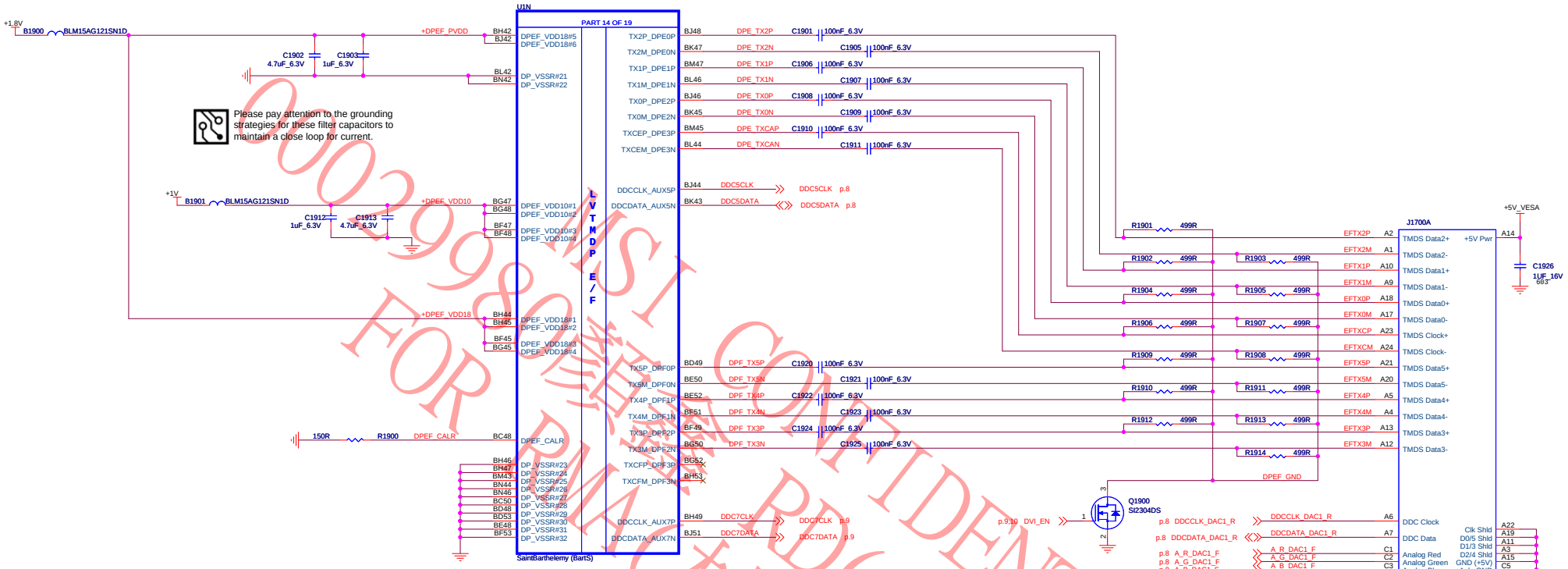
(11) BARTS LVTMDP E&F



Optional ESD protection dioes

D1900	2	1	ESD5V3U1U-02LRH	EFTX2P
D1901	2	1	ESD5V3U1U-02LRH	EFTX2M
D1902	2	1	ESD5V3U1U-02LRH	EFTX1P
D1903	2	1	ESD5V3U1U-02LRH	EFTX1M
D1904	2	1	ESD5V3U1U-02LRH	EFTX0P
D1905	2	1	ESD5V3U1U-02LRH	EFTX0M
D1906	2	1	ESD5V3U1U-02LRH	EFTXCP
D1907	2	1	ESD5V3U1U-02LRH	EFTXCM
D1908	2	1	ESD5V3U1U-02LRH	EFTX5P
D1909	2	1	ESD5V3U1U-02LRH	EFTX5M
D1910	2	1	ESD5V3U1U-02LRH	EFTX4P
D1911	2	1	ESD5V3U1U-02LRH	EFTX4M
D1912	2	1	ESD5V3U1U-02LRH	EFTX3P
D1913	2	1	ESD5V3U1U-02LRH	EFTX3M

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Title TMDS EF

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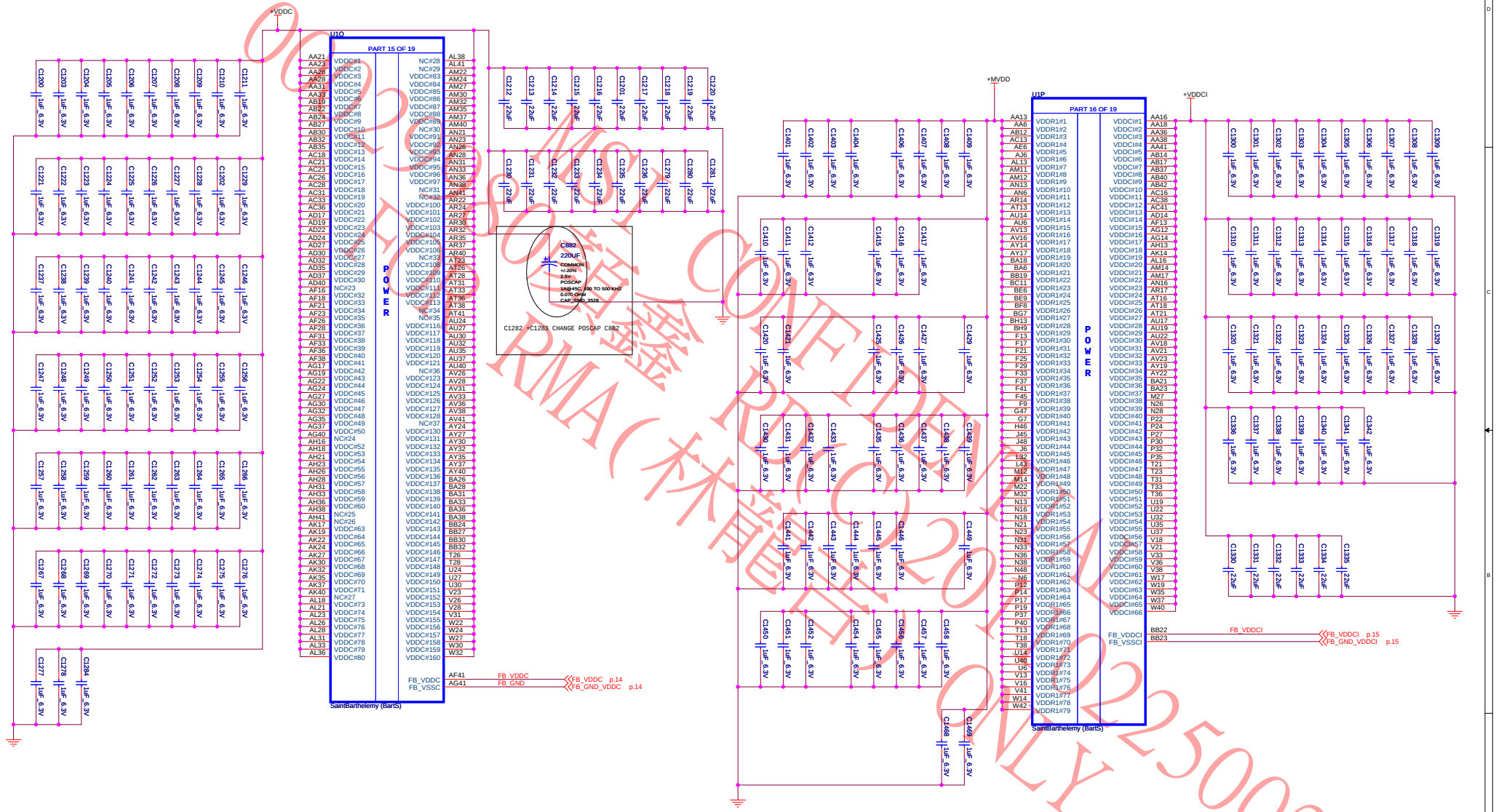
(12) BARTS Power



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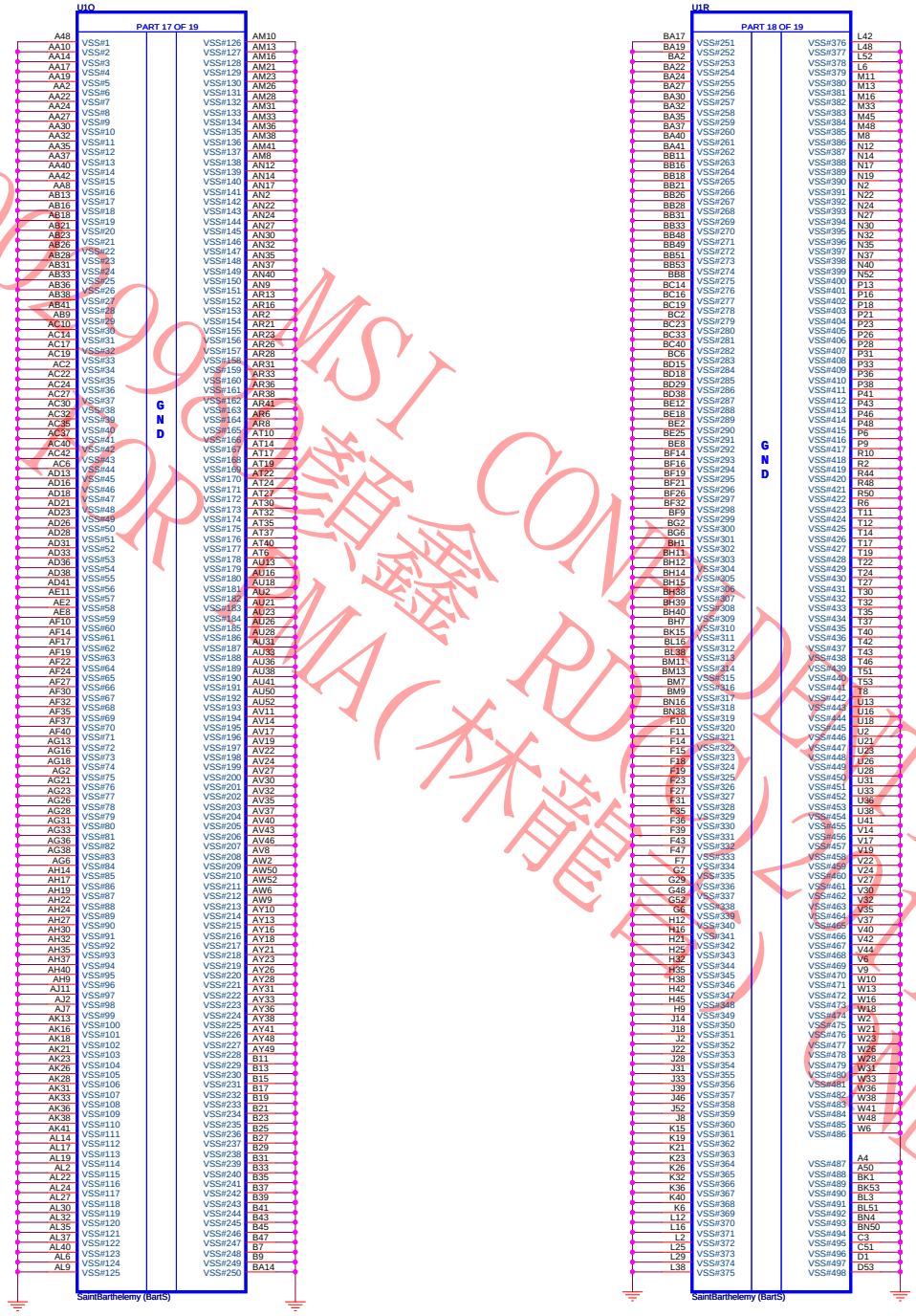
(13) BARTS GND



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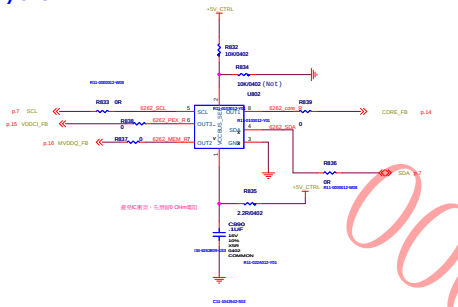
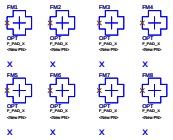
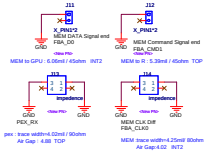
(14) 6262







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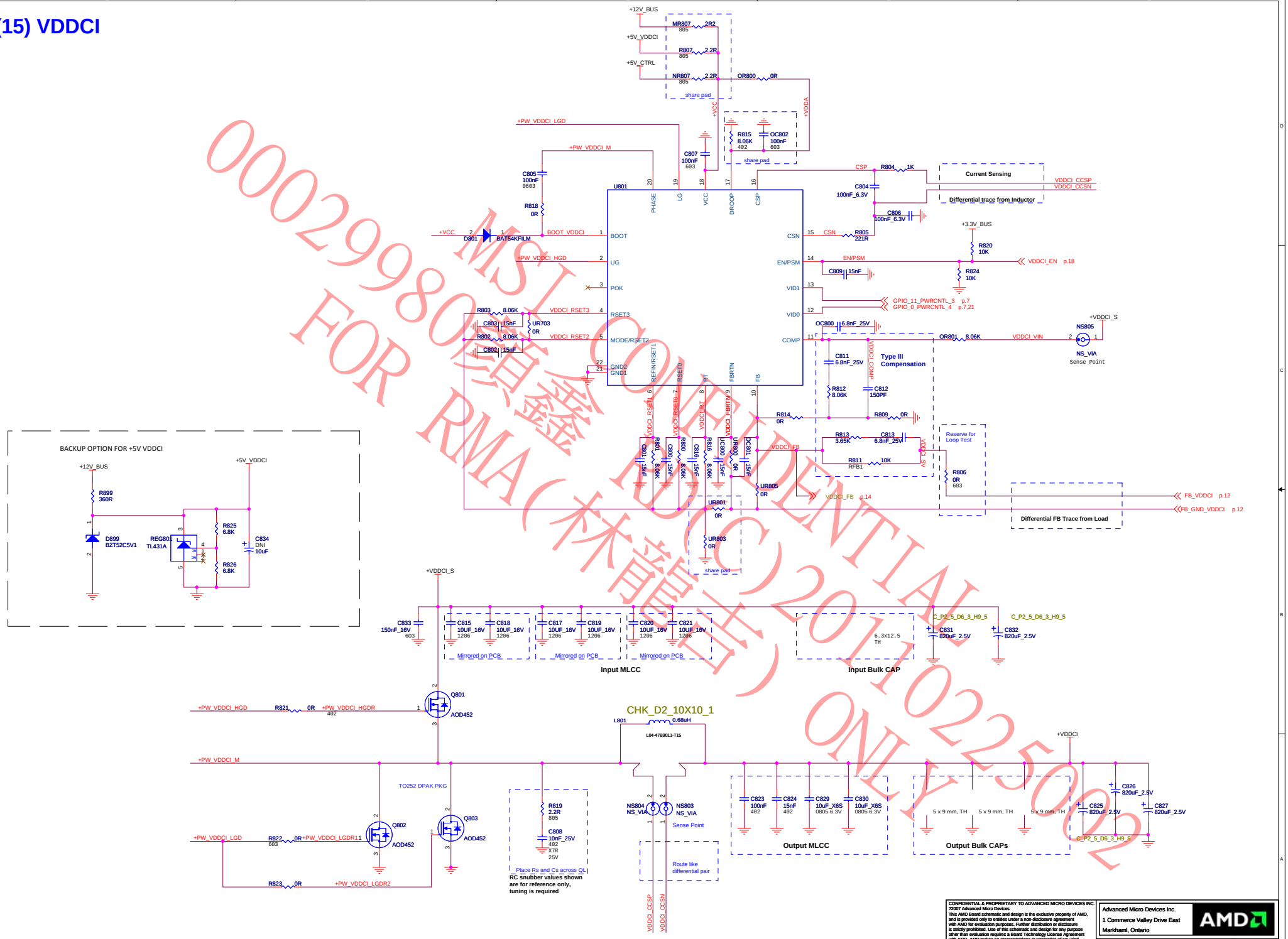
(15) VDDCI



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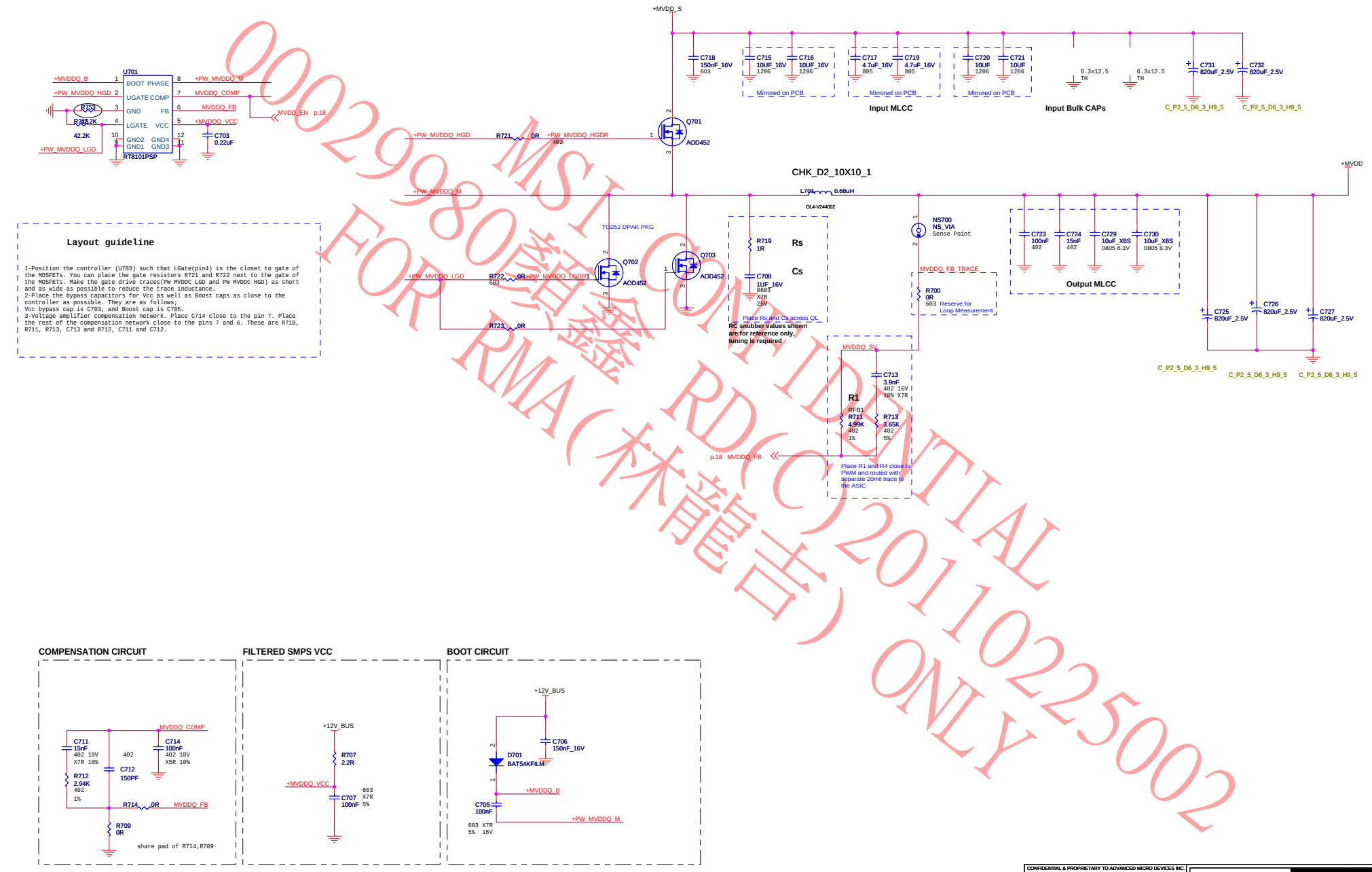
(16) MVDD



Layout guideline

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

COMPENSATION CIRCUIT

FILTERED SMPS VCC

BOOT CIRCUIT

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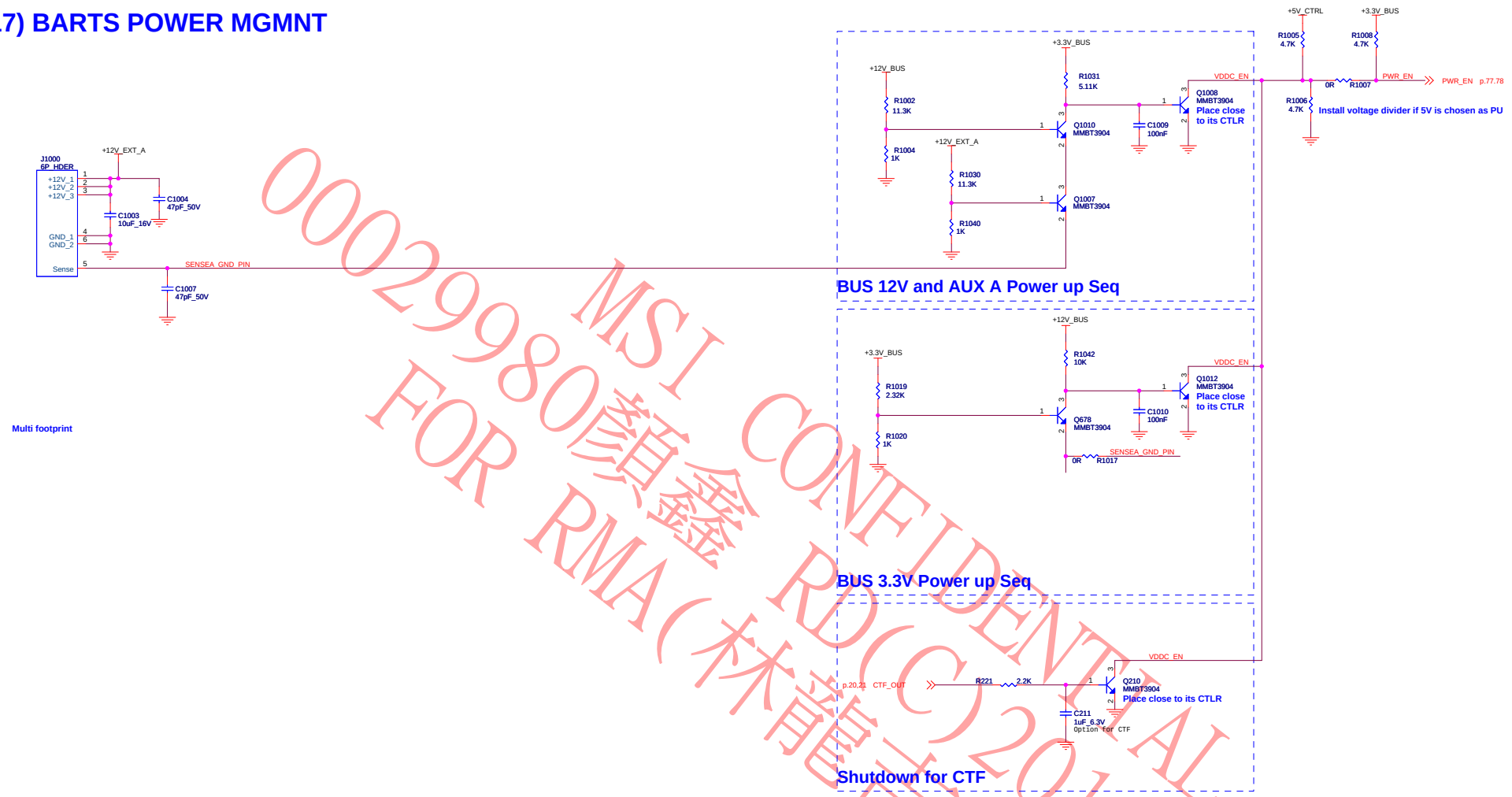
(17) BARTS POWER MGMNT



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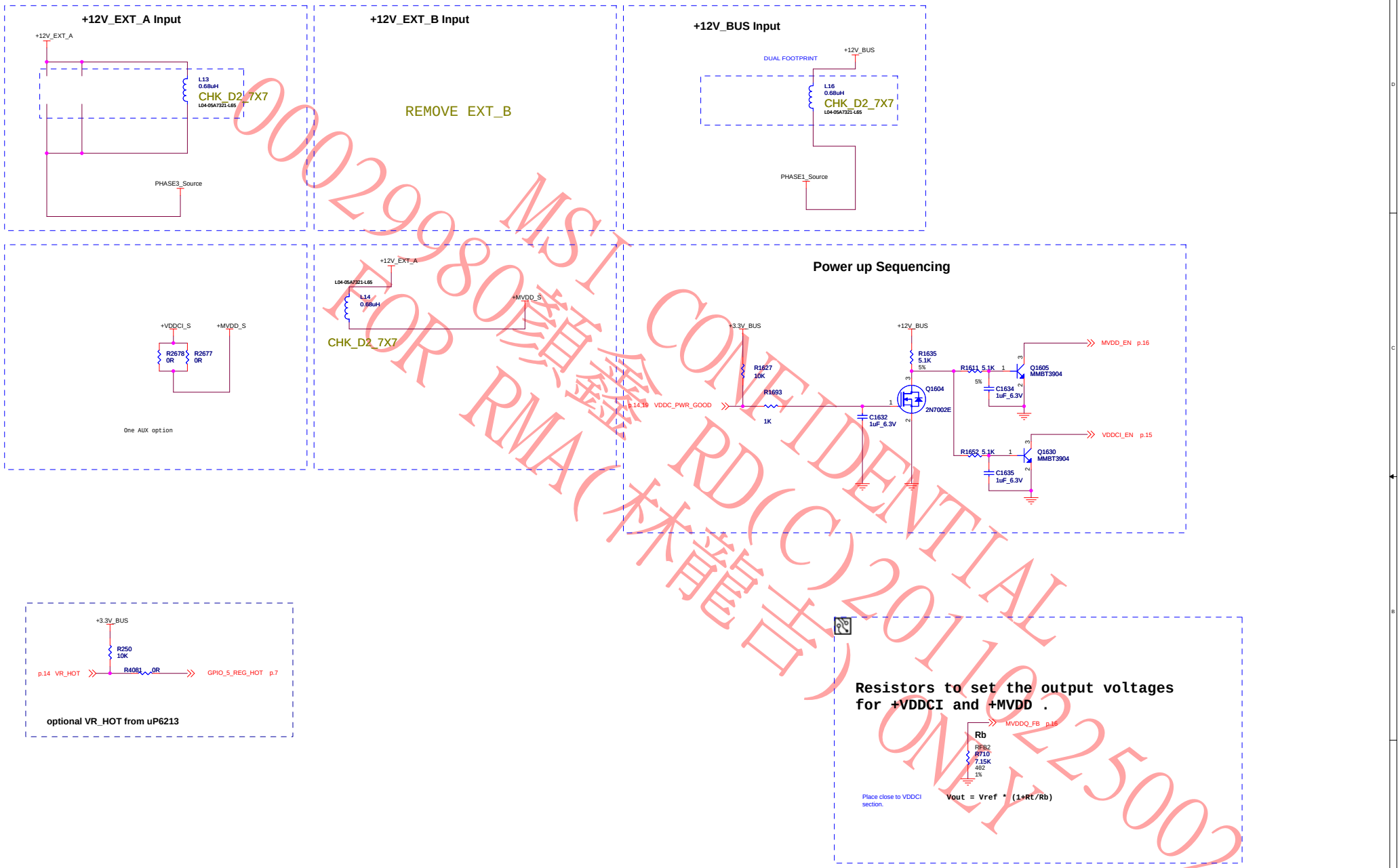
(18) BARTS VDDCI POWER PLAY



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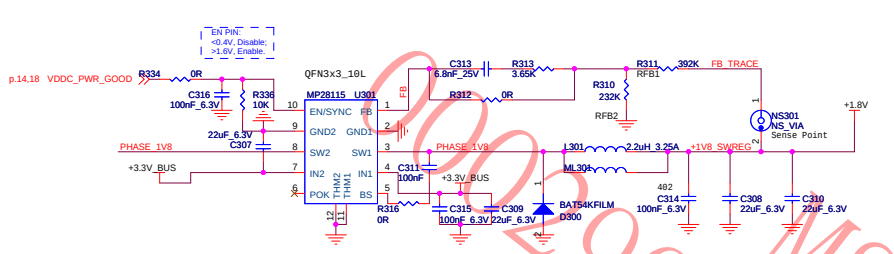
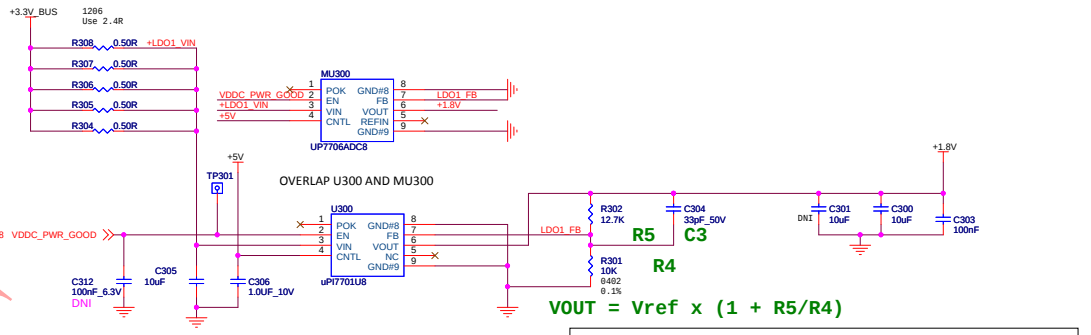
(18) BARTS Small Rail Regulators

LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

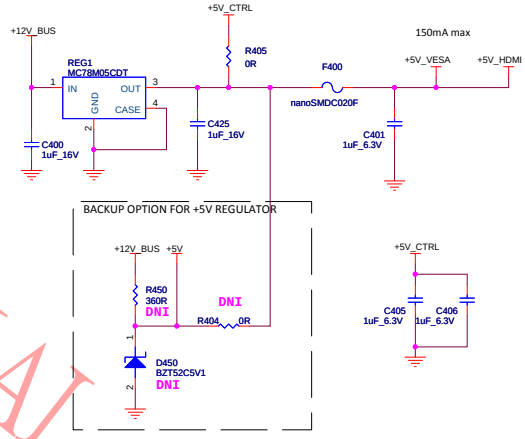




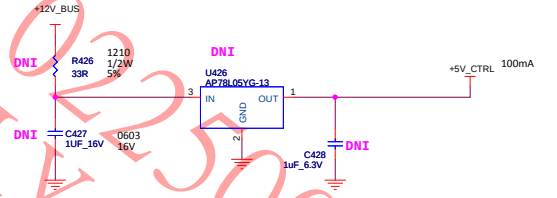
Regulators for +5V, +5V_VESA and +5V_HDMI
Iout max = 150mA (DVI+HDMI)

Other cheaper solution at 5MHz switching for 1.8V

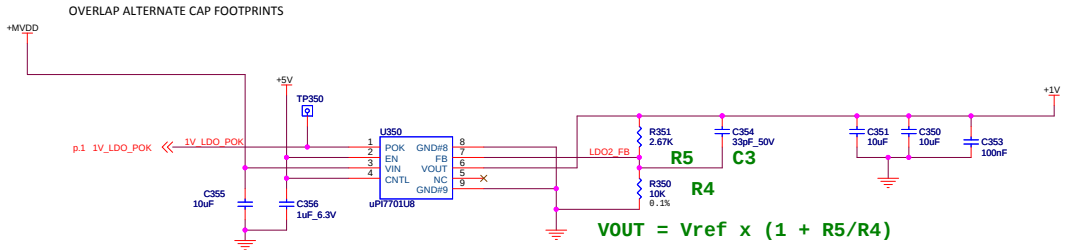
REMOVE



optional 5V power for VDDC regulator;



LDO #2: Vin = +1.35V to 1.8VMAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



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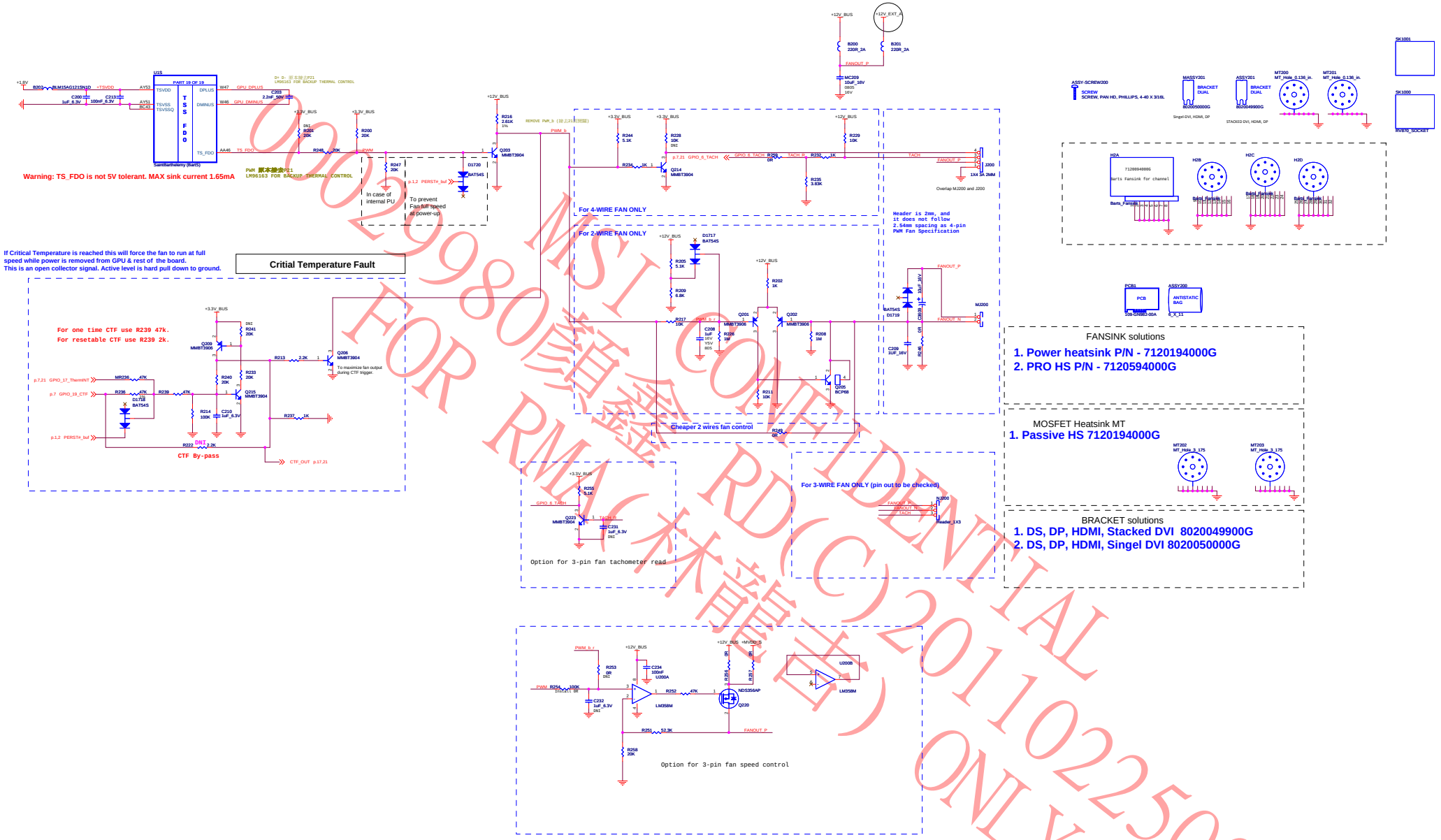
(20) BARTS Mechanical and Thermal Management



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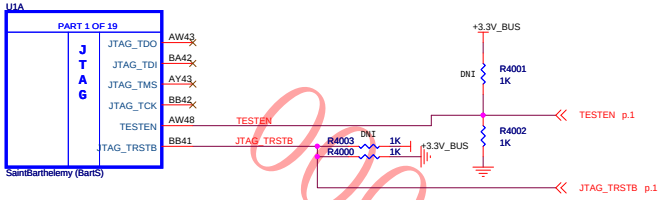
(21) BARTS Debug Circuits

JTAG



For ALL bringup boards DNI R4000 and stuff R4003 otherwise the TAPC will be struck in Test-Logic-Reset and be useless since TRSTB is not on the connector.

LM96163 FOR BACKUP THERMAL CONTROL

SWITCH CONNECTIONS TO PINSTRAPS

GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

To ACCESS the VDDC CONTROLLER through I2C

LED RED "ON" shows Fault

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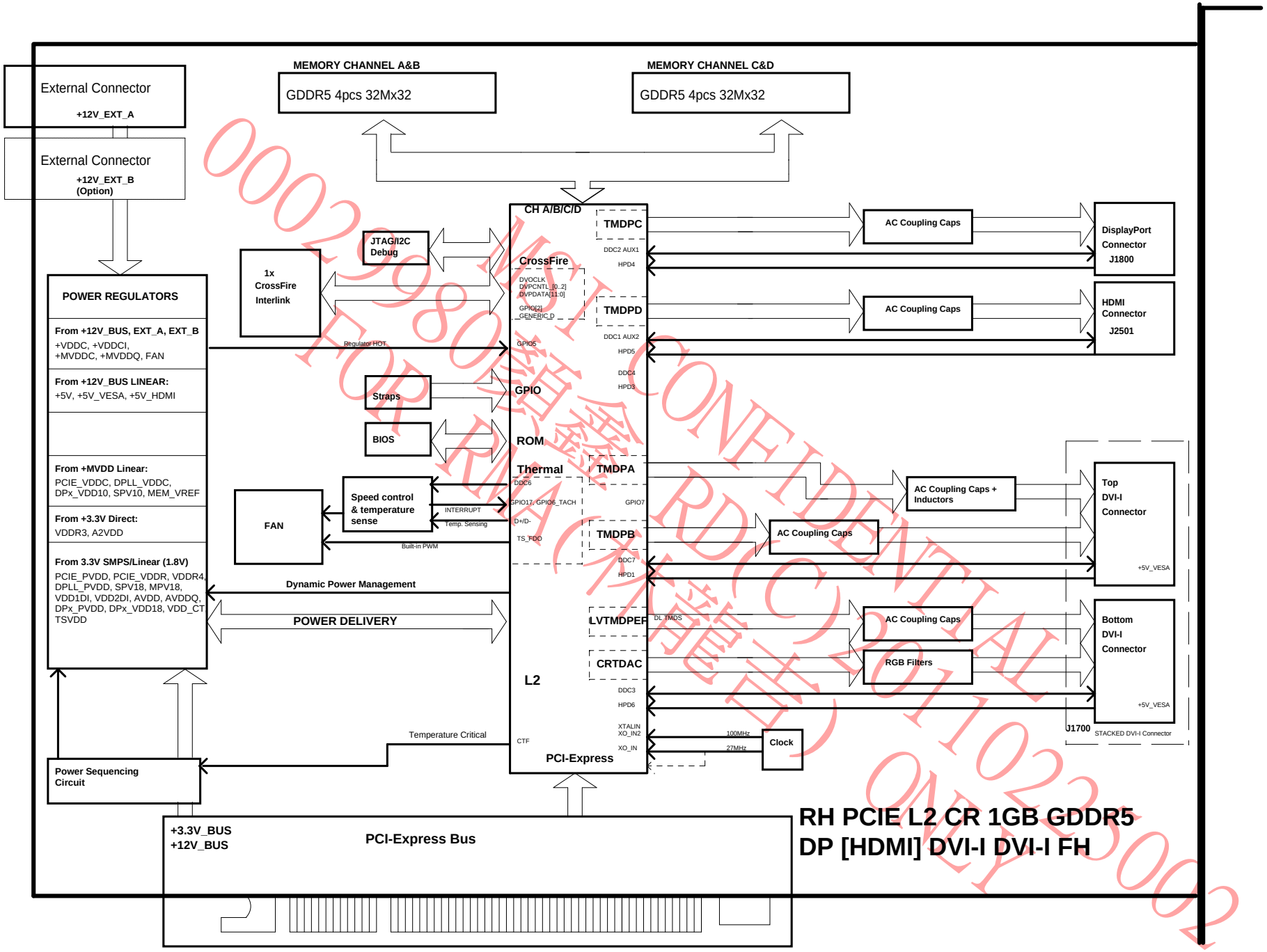

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Title	Block Diagram	Doc No.	105-C223XX-00B

Title	Schematic No.	Date:
RH BARTS GDDR5 DP-HDMI-DVII-DVII	105-C223XX-00B	Tuesday, September 21, 2010

REVISION HISTORY

NOTE: This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	21/06/2010	Initial release. Based on C221 layout
1	00B		Page17: add C221 Page14: update Q601,Q602,Q603,Q604 symbol Page18: add R241, R201. Page18: add optional 3-pin fan tach circuitry;add optional 3-pin fan speed control circuitry