

電子類元件 零件承認書文件 CHECK LIST

零件廠商： AOS

品名規格：SMD QFN-31L 5*5 MOS AOZ5332QI 50A AOS

技嘉料號：10IFD-505332-00R

項次	文件項目
Data Sheet 檢核項目	
1	DATASHEET (含機構尺寸、 端子腳鍍層材質、MSL Report)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間, 焊接/過爐次數與曲線圖)。 註 2
8	零件樣品 20PCS(Chipset 等高單價, 至少 1PCS)
9	電子零件承認基本調查表。註 3
10	以上資料電子檔為 PDF 檔, 且是同 1 個 File
GSCM 綠色產品管理系統-物料管制文件檢核清單	
物料管制文件 1	GSCM 綠色產品管理系統：零件照片
物料管制文件 2	GSCM 綠色產品管理系統：不使用禁用物質證明書 (保證書)。 註 4
物料管制文件 3	GSCM 綠色產品管理系統：Data Sheet
GSCM 綠色產品管理系統-MCD 表格	
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
其他文件 (僅適用電阻、電容類之系列元件)	
附件 1	危害物質測試報告 Test Report of Hazardous Substances。 註 5
附件 2	元件調查表 Component Composition Table

- ※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等
- ※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)
- 2.1. 基本需符合 JEDEC 規範
- 2.2. Ambient Temp. (Reflow Temp endure): >225°C, 70 sec. 零件塑膠材質需 PA9T(含)等級以上
- 2.3. PASTE IN HOLE 零件塑膠材質需 PA9T(含)等級以上
- ※ 3. 電子零件適用(技嘉)料號：**積體電路(IC) 10H*,10T*,10I*,10D*,10G*,11T***
非 IC 類：10C*,11C*,10L*,11L*,10X*,11X*,10R*,11B*
- ※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”
- ※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

電子零件承認基本調查表

一、原物料規格/來源			
項次	部位名稱/規格	材質	原物料來源產地
1	BONDING WIRE	Metal	PANDAN,SINGAPORE
2	DIE ATTACH-HENKEL	Adhesive	CALIFORNIA,USA
3	DIE ATTACH-INDIUM	Adhesive	ILLINOIS ,USA
4	CHIP-JIREH	WAFER	HILLSBORO,USA
5	CHIP-TSMC	WAFER	HSINCHU,TAIWAN
6	CLIP	Metal	SUZHOU,CHINA
7	LEADFRAME	Metal	SHENZHEN,CHINA
8	LEADFINISH	Metal materials plating layer	WUXI,CHINA
9	MOLD COMPOUND	Epoxy Resin	SUZHOU,CHINA

二、晶圓廠(非 IC 類免填)					
項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	JIREH	USA	8	100	自有
2	TSMC	USA	8	100	外包
3					

三、封裝廠(IC 類)；成品之生產製造工廠(非 IC 類)				
項次	工廠名稱	生產產地	投產比率(%)	自有/外包
1	AOS	CHINA	100	自有
2				
3				


四、產能	
總產能(月/PCS)	可供技嘉產能(月/PCS)
6M	1.5M

- ※ 1. IC 類之晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動) 時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件
- ※ 2. 非 IC 類零件之成品生產製造工廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動) 時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件
- ※ 3. 以上資訊欄位若有不足，可自行增加行數

承認書

SPECIFICATION APPROVAL FORM

廠 商 : 技嘉科技股份有限公司
承認書編號 : _____
品 名 : AOZ5332QI
規 格 : SMD QFN-31L 5*5
數 量 : _____
承 辦 人 : Daniel Liu
日 期 : 2018/10/22
用 途 : _____

公 司 承 認 章	廠 商 承 認 章
	

志遠電子股份有限公司
TECHMOSA INTERNATIONAL INC.

台北縣中和市立德街 118 號 6F
TEL: (02) 8226-7698 FAX: (02) 2651-3280

General Description

The AOZ5332QI is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High-Side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low-Side MOSFET has ultra low ON resistance to minimize conduction loss.

The AOZ5332QI is intended for use with 3V and 5V (CMOS) and Tri-State input compatibility by using the PWM input for accurate control of the power MOSFET switching activities.

A number of features are provided making the AOZ5332QI a highly versatile power module. The bootstrap diode is integrated in the driver. The Low-Side MOSFET can be driven into diode emulation mode to provide asynchronous operation when required. The pin-out is optimized for low parasitics, keeping their effects to a minimum.

Features

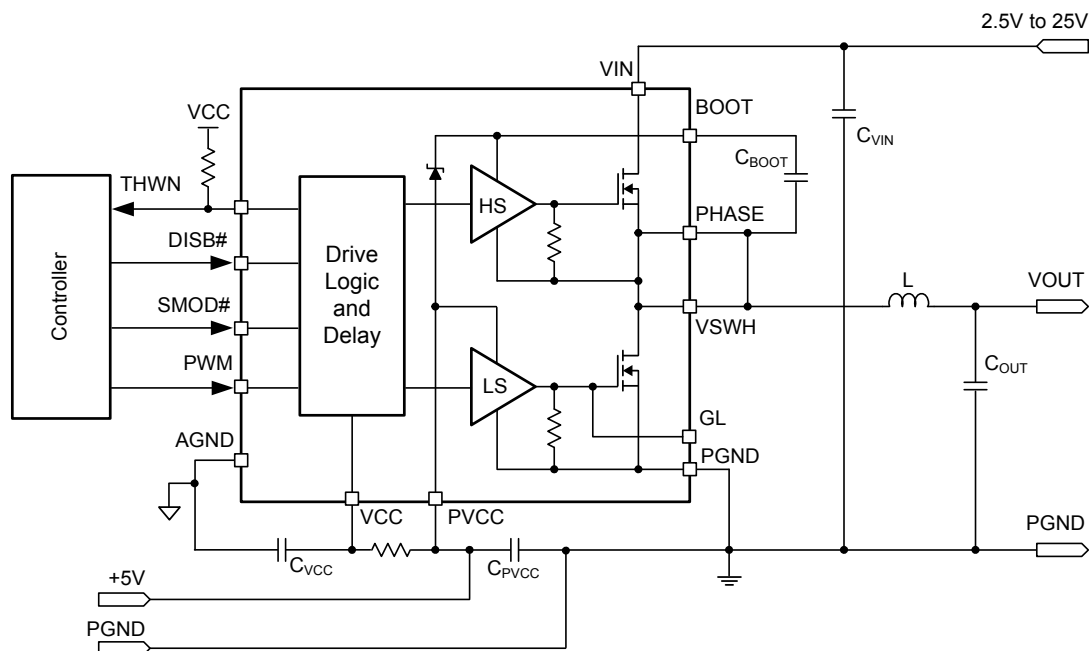
- 2.5V to 25V power supply range
- 4.5V to 5.5V driver supply range
- Up to 70A peak current
- Continuous current up to 50A
- Up to 2MHz switching operation
- 3V / 5V PWM / Tri-state input compatible
- Under-Voltage Lockout protection
- SMOD# control for Diode Emulation / CCM operation
- Low Profile 5x5 QFN-31L package

Applications

- Memory and graphic cards
- VRMs for motherboards
- Point of load DC/DC converters
- Video gaming console



Typical Application Circuit



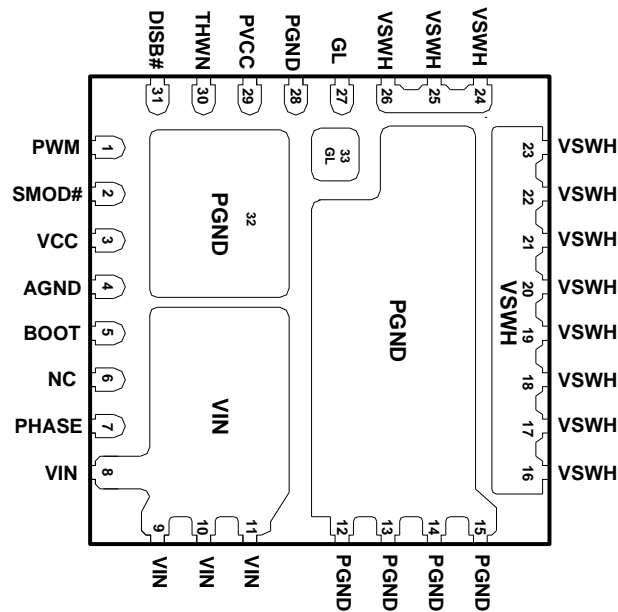
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5332QI	-40°C to +85°C	QFN5x5_31L	RoHS



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

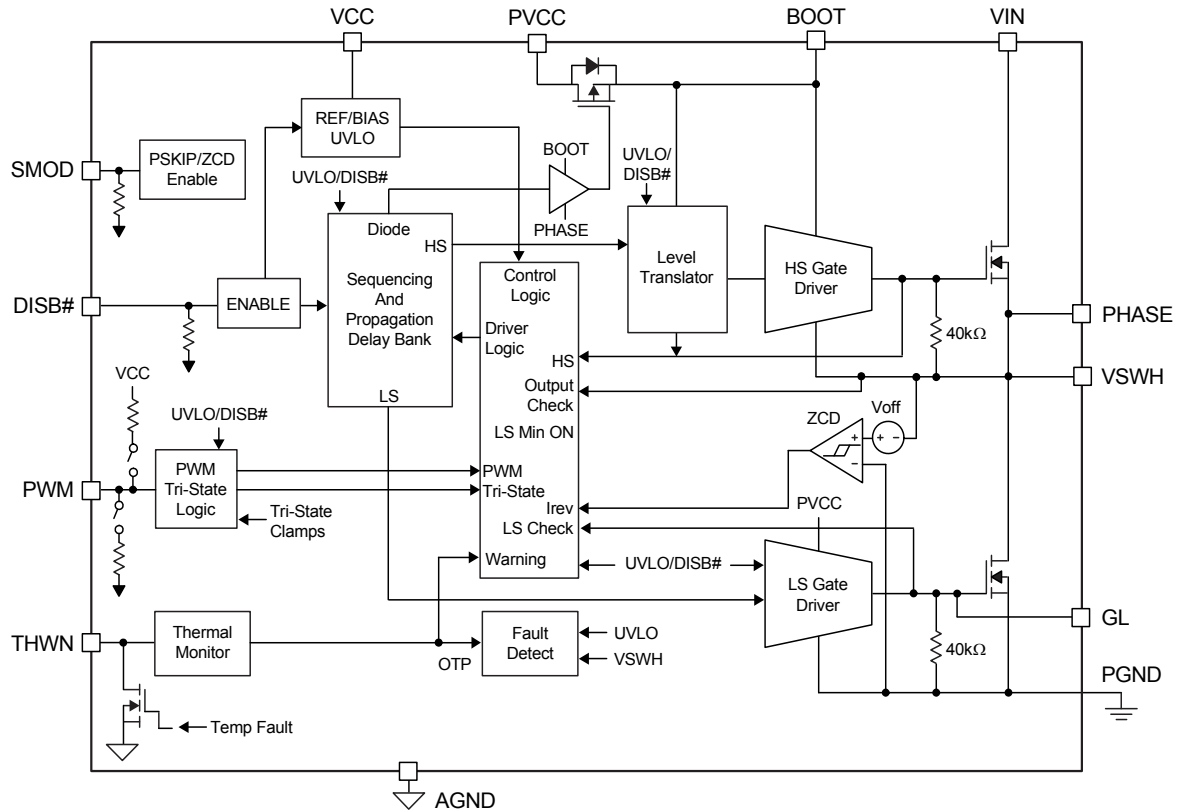


QFN5x5_31L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PWM	PWM input signal from the controller IC. When DISB#=0V, the internal resistor divider will be disconnected and this pin will be at High Impedance.
2	SMOD#	Pull Low to Enable Discontinuous Mode of Operation (DCM), Diode emulation or Skip Mode. There is an internal pull-down resistor on this pin.
3	VCC	5V Bias for Internal Logic Blocks. Ensure to position a 1 μ F MLCC directly between Vcc (Pin 3) and AGND (Pin 4).
4	AGND	Signal Ground
5	BOOT	High Side MOSFET Gate Driver supply rail. Connect a 100nF ceramic capacitor between BOOT and the PHASE (Pin 7).
6	NC	No Connect.
7	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (pin5). It is required to be connected to Pin 16 - 26 externally on PCB.
8, 9, 10, 11	VIN	Power stage High Voltage Input (Drain Connection of High-Side MOSFET).
12, 13, 14, 15	PGND	Power Ground pin for power stage (Source Connection of Low-Side MOSFET).
16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26	VSWH	Switching node connected to the source of High Side MOSFET and the drain of Low Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal. Ensure these pins are connected to pin 7 externally on PCB.
27, 33	GL	Low Side MOSFET Gate connection. This is for test purposes only.
28, 32	PGND	Power Ground pin for High Side and Low Side MOSFET Gate Drivers. Ensure to connect 1 μ F across PGND (pin 28) to PVCC (Pin 29) independently.
29	PVCC	5V Power Rail for High Side and Low Side MOSFET Drivers. Ensure to position a 1 μ F MLCC directly between PVCC (Pin 29) and PGND (Pin 28).
30	THWN	Thermal warning indicator. This is an open-drain output. When the temperature at the driver I.C. die reaches the Over Temperature Threshold, this pin is pulled low.
31	DISB#	Output disable pin. When this pin is pulled to a logic low level, the I.C. is disabled. There is an internal pull-down resistor to AGND.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC, PVCC)	-0.3V to 6.5V
High Voltage Supply (VIN)	-0.3V to 30V
Control Inputs (PWM, SMOD#, DISB#)	-0.3V to (VCC+0.3V)
Output (THWN)	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 35V
Bootstrap Voltage Transient ⁽¹⁾ (BOOT-PGND)	-0.3V to 40V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3V to PVCC
BOOT Voltage Transient ⁽¹⁾ (BOOT-PHASE/VSWH)	-0.3V to 7V
Switch Node Voltage DC (PHASE/VSWH)	-0.3V to 30V
Switch Node Voltage Transient ⁽¹⁾ (PHASE/VSWH)	-8V to 37V
Low Side Gate Voltage DC (GL)	(PGND-0.3V) to (PVCC+0.3V)
Low Side Gate Voltage Transient ⁽¹⁾ (GL)	(PGND-2.5V) to (PVCC+0.3V)
Storage Temperature (T _S)	-65°C to +150°C
Max Junction Temperature (T _J)	125°C
ESD Rating ⁽²⁾	2.0kV

Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	2.5V to 25V
Low Voltage / MOSFET Driver Supply VCC, PVCC	4.5V to 5.5V
Control Inputs (PWM, SMOD#, DISB#)	0V to (VCC-0.3V)
Output (THWN)	0V to (VCC-0.3V)
Operating Frequency	200kHz to 2MHz

Electrical Characteristics⁽³⁾

$T_A = 25^\circ\text{C}$ to 125°C . Typical values reflect 25°C ambient temperature; $V_{IN} = 12\text{V}$, $V_{CC} = P_{VCC} = 5.0\text{V}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{IN}	Power Stage Power Supply		2.5		25	V
V _{CC}	Low Voltage Bias Supply	PVCC=VCC	4.5		5.5	V
R _{θJC} ⁽⁴⁾	Thermal Resistance	PCB Temp = 100°C		2.5		°C/W
R _{θJA} ⁽⁴⁾				13.8		°C/W
Input Supply and UVLO						
V _{CCON}	Under-Voltage Lockout	V _{CC} Rising		3.5	3.3	V
V _{CC_HYST}		V _{CC} HYST		400		mV
I _{VCC}	Control Circuit Bias Current	DISB# = 0V, V _{CC} = 5V (Shutdown)		1		μA
		SMOD# = High, DISB# = High, V _{PWM} = 0V (No Switching)		720		
		SMOD# = Low, DISB# = High, V _{PWM} = 0V (No Switching)		590		
		SMOD# = Low, DISB# = High, V _{PWM} =1.65V (Tri-State, No Switching)		500		
I _{PVCC}	Drive Circuit Operating Current	DISB# = High, V _{PWM} = 400kHz, 20% Duty Cycle		20		mA
		DISB# = High, V _{PWM} = 1MHz, 20% Duty Cycle		50		μA
PWM Input						
V _{PWMH}	PWM Input High Threshold	V _{PWM} Rising = V _{CC} = 5V	2.7			V
V _{PWML}	PWM Input Low Threshold	V _{PWM} Falling = V _{CC} = 5V			0.7	V
I _{PWM_SRC}	PWM Pin Input Current	Source, V _{PWM} = 0V		150		μA
I _{PWM_SNK}		Sink, V _{PWM} = 3.3V		150		μA
V _{TRI}	PWM Input Tri State Threshold Window	V _{CC} = PVCC = 5V -40°C < Temp <125°C	1.35		2.0	V
V _{TRI_CLMP}	PWM Tri-State Voltage Clamp	DISB# = 5V, PWM = Floating		1.65		V
DISB# Input						
V _{DISB#_ON}	Outputs Enable Threshold	V _{CC} = PVCC = 5V	2.0			V
V _{DISB#_OFF}	Outputs Disable Threshold	V _{CC} = PVCC = 5V			0.8	V
R _{DISB#}	DISB# Input Resistance	Pull-Down Resistor		810		kΩ
SMOD# Input						
V _{SMOD#_H}	SMOD# Rising Threshold	V _{CC} = PVCC = 5V	2.0			V
V _{SMOD#_L}	SMOD# Falling Threshold	V _{CC} = PVCC = 5V			0.8	V
R _{SMOD#}	SMOD# Input Resistance	Pull-Down Resistor		810		kΩ
Gate Driver Timing						
t _{PDLU}	PWM to High Side Gate	PWM: H → L, VSWH: H → L		30		ns
t _{PDLL}	PWM to Low Side Gate	PWM: L → H, GL: H → L		25		ns
t _{PDHU}	Low Side to High Side Gate Deadtime	GL: H → L, GH ⁽³⁾ : L → H		15		ns
t _{PDHL}	High Side to Low Side Gate Deadtime	VSWH: H → 1V, GL: L → H		13		ns
t _{TSSHD}	Tri State Shutdown Delay	PWM: L → V _{TRI} , GL: H → L and PWM: H → V _{TRI} , VSWH: H → L		25		ns

Electrical Characteristics⁽³⁾

$T_A = 25^\circ\text{C}$ to 125°C . Typical values reflect 25°C ambient temperature; $V_{IN} = 12\text{V}$, $V_{CC} = P_{VCC} = 5.0\text{V}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{TSEXIT}	Tri State Propagation Delay	PWM: $V_{TRI} \rightarrow 2.2\text{V}$, VSWH: L \rightarrow H PWM: $V_{TRI} \rightarrow 0.8\text{V}$, GL: L \rightarrow H		35		ns
t_{LGMIN}	LS Minimum On Time	SMOD# = L		350		ns
Thermal Notification⁽⁴⁾						
t_{JTHDN}	Junction Thermal Threshold			150		$^\circ\text{C}$
t_{JHYST}	Junction Thermal Hysteresis			30		$^\circ\text{C}$
V_{THWN}	THWN Pin Output Low			60		$^\circ\text{C}$
R_{THWN}	THWN Pull Down Resistance			120		$^\circ\text{C}$

Notes:

3. All voltages are specified with respect to the corresponding AGND pin.
4. Characterization value. Not tested in production.
5. GH is an internal pin.

Table 1. Input Control Truth Table

DISB#	SMOD#	PWM	GH (Not a Pin)	GL
L	X	X	L	L
H	L	H	H	L
H	L	L	L	H ⁽⁶⁾ , Forward I_L L, Reverse I_L
H	X	Tri State	L	L
H	H	H	H	L
H	H	L	L	H

Note:

Diode emulation mode is activated when SMOD# pin is held low.

6. Zero Cross Detection (ZCD) at $I_L \cdot R_{dson(LS)} = 2\text{mV}$ (offset) turns off GL.

Timing Diagram

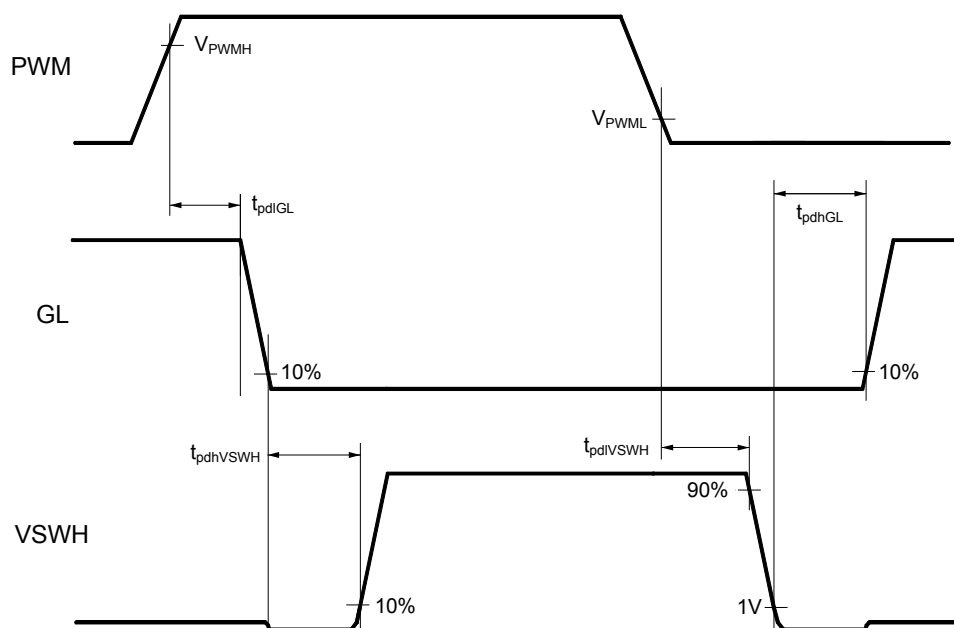


Figure 1. PWM Logic Input Timing Diagram

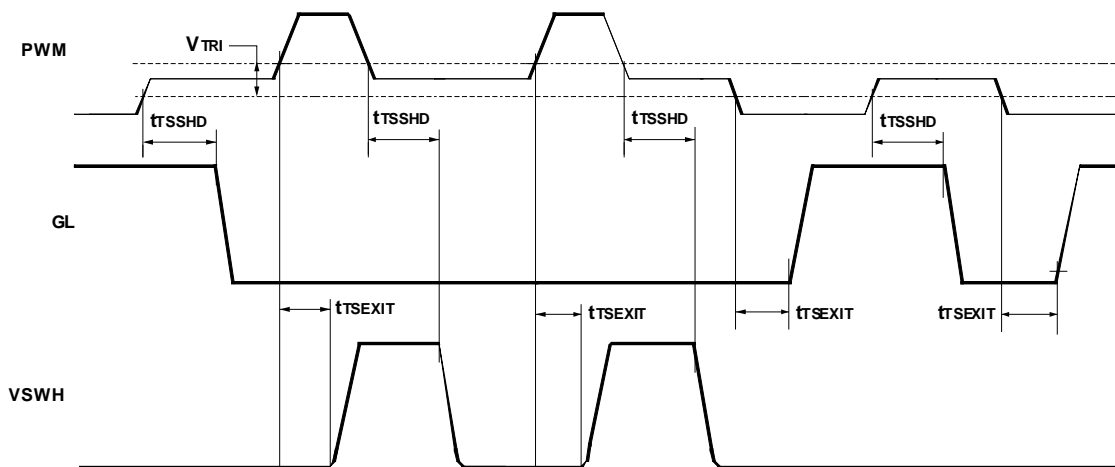


Figure 2. PWM Tri-State HoldOff and Exit Timing Diagram

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $PV_{CC} = V_{CC} = 5\text{V}$, unless otherwise specified.

Figure 3. Efficiency: $V_{IN} = 12\text{V}$, $V_O = 1\text{V}$, Freq = 600kHz

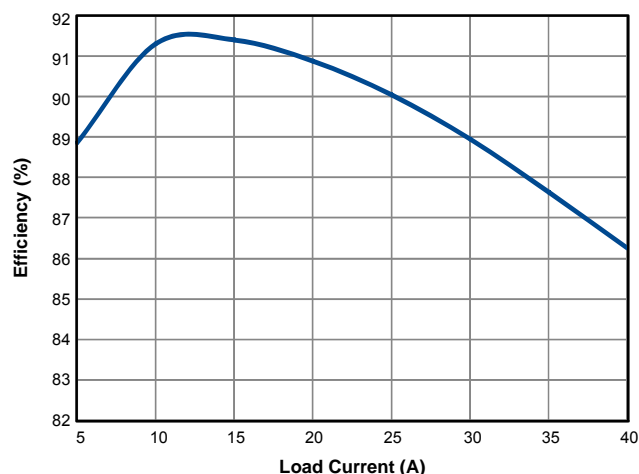


Figure 4. Power Loss: $V_{IN} = 12\text{V}$, $V_O = 1\text{V}$, Freq = 600kHz

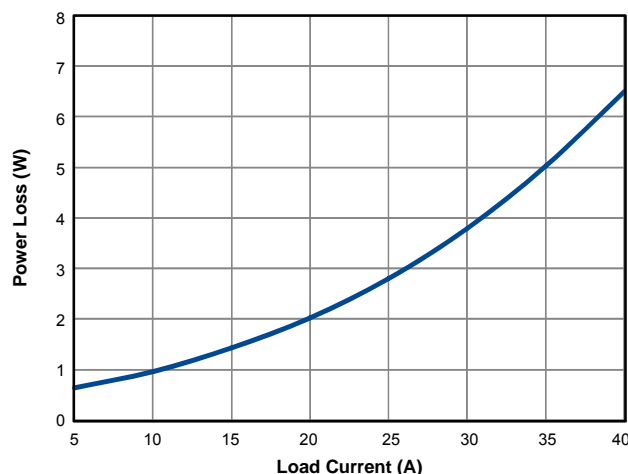


Figure 5. Supply Current (I_{PVCC}) vs. Temperature

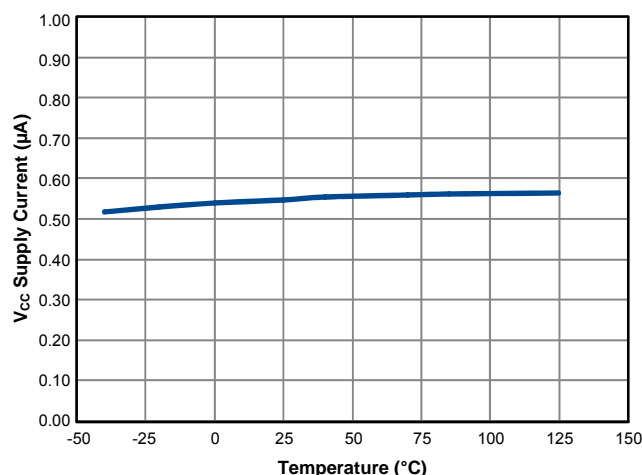


Figure 6. PWM Threshold vs. Temperature

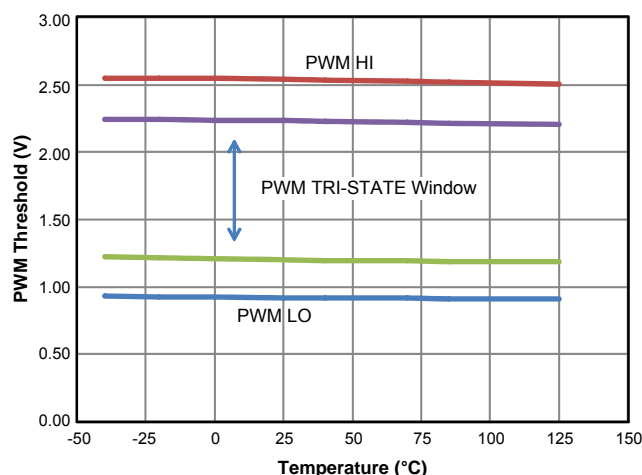


Figure 7. SMOD# Threshold vs. Temperature

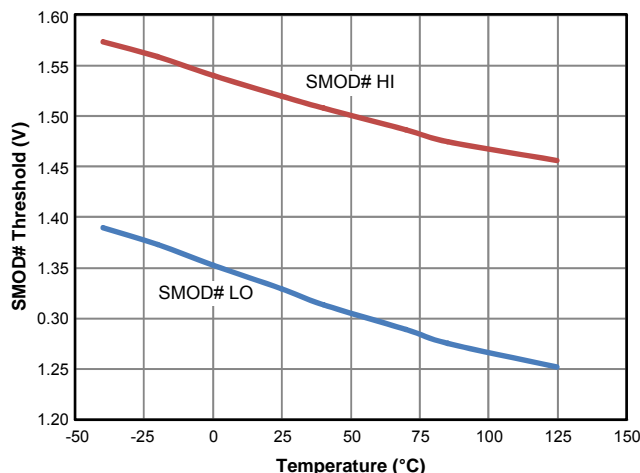
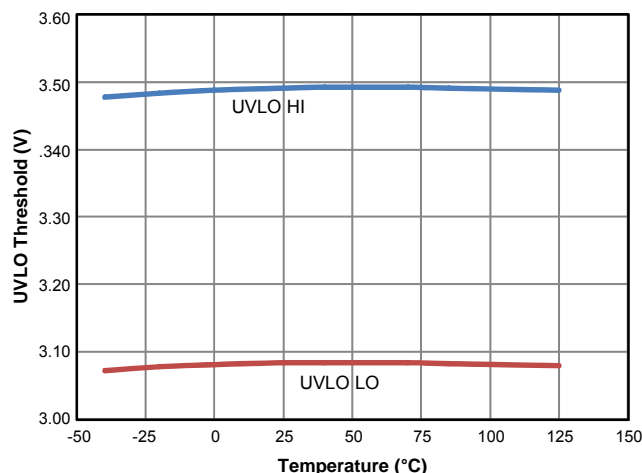


Figure 8. UVLO (V_{CC}) Threshold vs. Temperature



Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $PV_{CC} = V_{CC} = 5\text{V}$, unless otherwise specified.

Figure 9. DISB# Input Threshold vs. Temperature

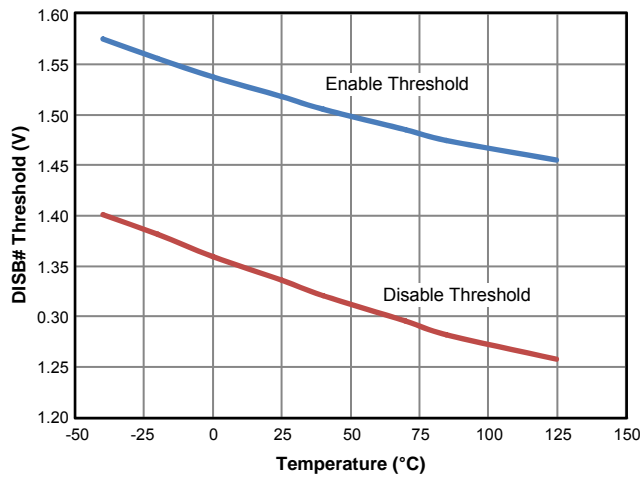
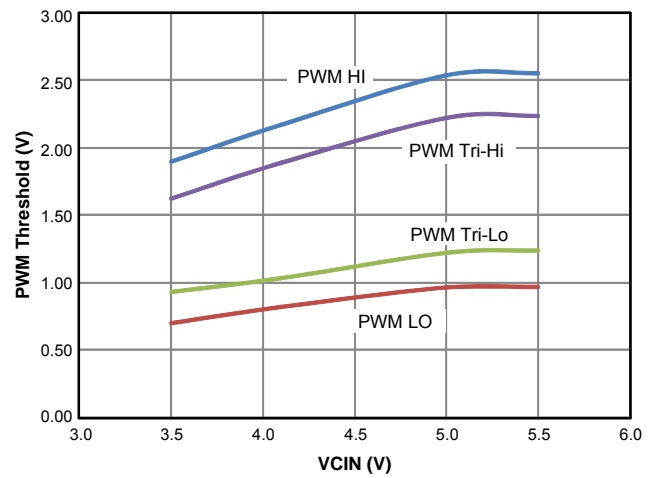


Figure 10. PWM Threshold vs. V_{CIN}



Application Information

AOZ5332QI is a fully integrated power module designed to work over an input voltage range of 2.5V to 25V with a separate 5V supply for gate drive and internal control circuitry. The MOSFETs are individually optimized for efficient operation on either High-Side or Low-Side switches in a low duty cycle synchronous buck converter. High current MOSFET Gate Drivers are also integrated, minimizing parasitic loop inductance resulting to optimum switching.

Powering the Module and the Gate Drives

An external supply PVCC = 5V is required for driving the MOSFETs. The MOSFETs are designed with optimally customized gate thresholds voltages, achieving the most advantageous compromise between fast switching speed and minimal power loss. The control logic supply VCC can be derived from the gate drive supply PVCC through an RC filter to bypass the switching noise. The gate driver is capable of supplying several amperes of peak current into the Low-Side MOSFET to achieve extremely fast switching. A ceramic bypass capacitor of 1 μ F or higher is recommended from PVCC to AGND.

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor (100nF) between the BOOT pin and the PHASE node. It is recommended that this capacitor Cboot be connected as close as possible to the device across pins 5 and 7. The Bootstrap Diode is integrated into the package. Rboot is an optional resistor used by designers to slow down the turn on speed of the High-Side MOSFET. Typical values between 1 Ω to 5 Ω is a compromise between the need to keep both the switching time and VSWH node spikes as low as possible.

Under-voltage Lockout

The AO5332QI carries out normal operation when VCC rises above the UVLO exit threshold voltage. The under-voltage lockout is set at 3.5V nominally and exits the lockout when the VCC rises above this voltage threshold. Since the PWM control signals are provided typically from an external controller, extra care must be taken during start up.

Typical system operation begins with a soft start sequence to minimize in-rush current through the converter during start up. Powering the module with a full duty cycle PWM signal may lead to a number of undesirable consequences as explained below. AOZ5332QI provides UVLO and thermal monitor protection. The PWM controller should provides current monitoring and protection under all possible operating and transient conditions.

Disable (DISB#) Function

The AOZ5332QI provide enable and disable function through DISB# pin. In the low state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFETs. In this state, standby current is minimized. If DSBL# is left unconnected, an internal pull-down resistor will pull the pin to AGND and shut down the IC.

In the high state, the DSBL# pin enables the driver IC, and the driver signal follows the external PWM signal.

Input Voltage VIN

AOZ5332QI is rated to operate over a wide input range of 2.5V to 25V. As with any other synchronous buck converter, large pulse currents at high frequency and extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to bypass the input supply (VIN) very close to the package leads with X7R or X5R quality surface mount ceramic capacitors.

The High-Side MOSFET is optimized for fast switching with low duty ratios made possible due to low gate charges (Q_T). When the module is operated at low VIN the duty cycle ratio will be higher and conduction losses in the High-Side MOSFET will also be correspondingly higher. The total power loss for the module may still be low but the High-Side MOSFET higher conduction losses may generate higher temperature. The two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation. Hence, it is recommended that worst case junction temperature be measured for both High-Side MOSFET and Low-Side MOSFET to ensure they are operating within safe limits at high duty cycle ratio.

PWM Input

AOZ5332QI is compatible with 3V and 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives.

The PWM input is also a tri-state compatible input. When the PWM output of the Master Controller is in high impedance or not connected, both the gate driver outputs will turn off the MOSFETs. The PWM Input and Tri-State Thresholds table in Table 2 lists the thresholds levels for high and low level transitions as well as tri-state window. As shown in Fig.2, there is a HOLDOFF delay between the corresponding PWM tri-state signal and the output gate drivers being pulled low. This delay is typically 25ns and intended to prevent spurious triggering caused by tri-state mode entrance.

Table 2. PWM Input and Tri-State Threshold

Threshold	V _{PWMH}	V _{PWML}	V _{TRIH}	V _{TRIL}
AOZ5332QI	2.7V	0.8V	1.35V	2.05V

Note: See Figure 2 for propagation delays and tri-state window.

Diode Mode Emulation of Low-Side MOSFET (SMOD#)

AOZ5332QI can be operated in the diode emulation or pulse skipping mode using the SMOD# pin. This enables the converter to operate in asynchronous mode during start up, light load or under pre-bias conditions. If SMOD# is taken high, the controller will use the PWM signal and generate both the High and Low Side complementary gate drive outputs with minimal anti-overlap delays necessary to avoid cross conduction. When the SMOD# pin is pulled low, the High-Side MOSFET drive is not affected but the module's diode emulation mode is activated for the Low-Side MOSFET. See Table 1 for all possible logic inputs and corresponding output drive conditions.

Gate Drives

AOZ5332QI has an internal high current high speed driver for both High-Side MOSFET and Low-Side MOSFET. Propagation delays between transitions of the PWM waveform and corresponding gate drives are kept to the minimum. AOZ5332QI has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFETs are not turned ON at the same time.

1) PWM from L to H

When the falling edge of GL goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHU}), the GH is turned on.

2) PWM from H to L

When the falling edge of the VSWH voltage goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHL}), the GL is turned on.

Thermal Warning (THWN)

The module temperature is internally sensed and an alarm is asserted if it exceeds 150°C. The alarm is reset when the temperature cools down to 120°C. The THWN is an open drain pin that is pulled to AGND to indicate an over-temperature condition. It may be pulled up to VCC through a resistor for monitoring purposes. The AOZ5332QI device will not power down during the over temperature condition.

PCB Layout Guidelines

AOZ5332QI is a high current module rated for operation up to 2MHz. This requires fast switching speeds to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package eliminates driver-to-MOSFET gate pad parasitics of the package or PCB.

While excellent switching speeds can be achieved, correspondingly high levels of dv/dt and di/dt will be observed throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the area of the primary switching current loop, formed by the VIN, VSWH and the input bypass capacitor C_{VIN}. The PCB design is somewhat simplified because of the optimized pin out in AOZ5332QI. The bulk of VIN and PGND pins are located adjacent to each other and the input capacitors should be placed as close as possible to these pins. The area of the secondary switching loop, formed by Low-Side MOSFET, output inductor and output capacitor C_{out} is the next critical parameter. This requires the second layer or "Inner 1" be the PGND plane. Via should be placed near input capacitors' PGND pads.

While AOZ5332QI is optimally efficient, it can still dissipate high power which requires attention to thermal design. MOSFETs in the package are directly attached to individual exposed pads to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal relief pads should be placed correspondingly to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the High Voltage system input, is desirable and vias should be provided near the device to connect the VIN pads to the power plane. Significant amount of heat is dissipated through multiple PGND pins. A large copper area connected to the PGND pins in addition to the system ground plane through vias will further improve thermal dissipation.

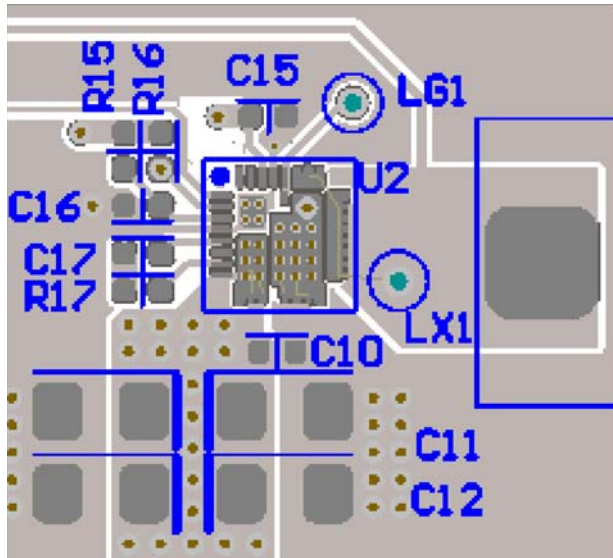


Figure 11 Top Layer of Demo Board, VIN, VSWH and PGND Copper Pads

As shown on Figure 11, the top most layer of the PCB should comprise of wide and exposed copper area for the primary AC current loop that runs along VIN pad originating from the input capacitors that are mounted to a large PGND pad. They serve as thermal relief as heat flows down to the VIN exposed pad that fan out to a wider area. Adding vias will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spike appear at the VSWH terminal which are caused by the large internal di/dt s produced by the in- package parasitics. To minimize the effects of this interference, the VSWH terminal at which the main inductor L is mounted so the inductor can physically fit. The goal is to employ the least amount of copper area for this VSWH terminal just enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH pad or Inductor terminal is voided and the shape of this void is replicated descending down through the rest of the layers. Refer to Figure 12.

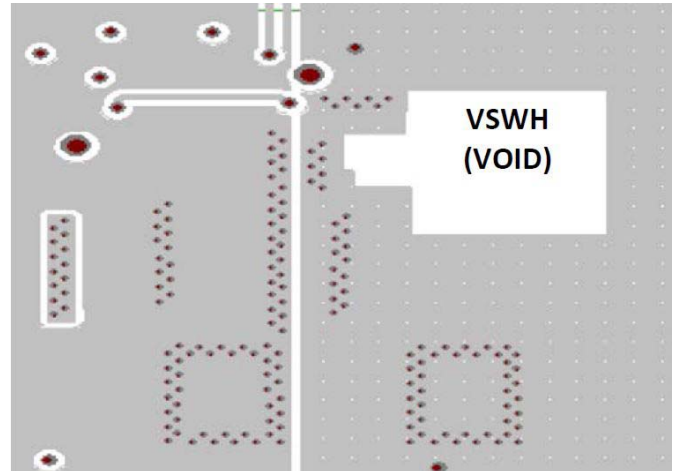


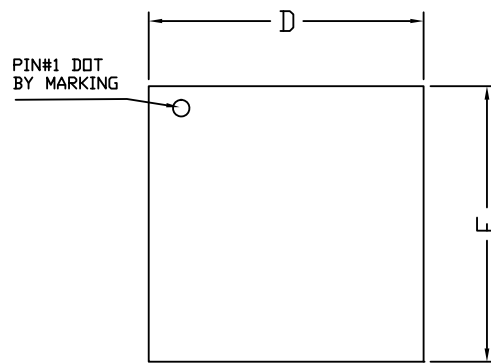
Figure 12. Bottom Layer of PCB

Positioning vias through the landing pattern of the VIN and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer. (See RECOMMENDED LANDING PATTERN AND VIA PLACEMENT section).

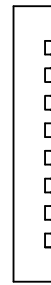
The exposed pads dimensional footprint of the 5x5 QFN package is shown on the package dimensions page. For optimal thermal relief, it is recommended to fill the PGND and VIN exposed landing pattern with 10mil diameter vias. 10mil diameter is a commonly used via diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.

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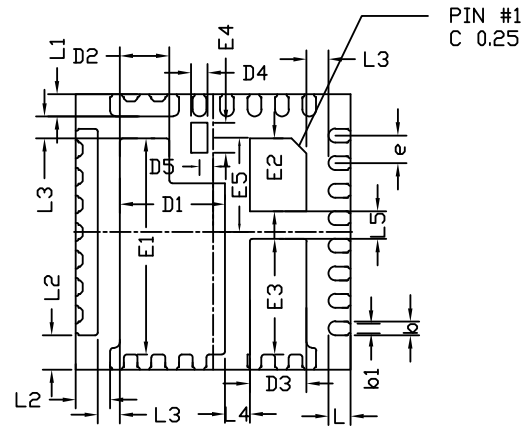
Package Dimensions, QFN5x5A_31L EP3_S



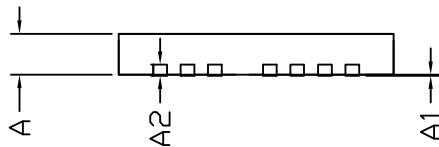
Top View



Side View

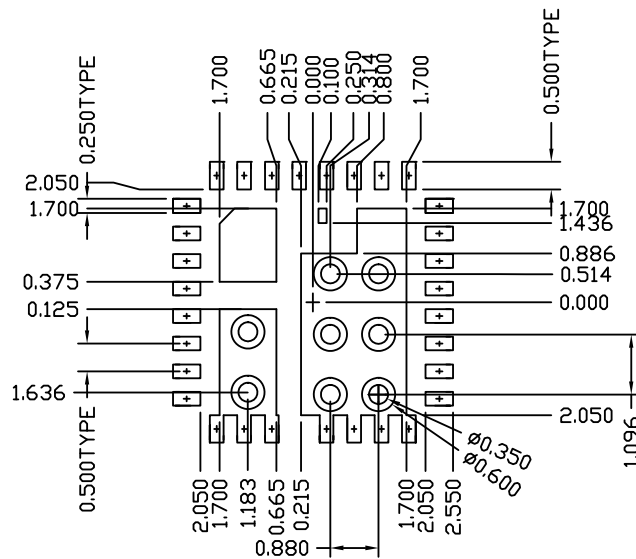


Bottom View



Side View

Recommended Land Pattern Via Placements



UNIT: mm

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	-	0.050	0.000	-	0.002
A2	0.2REF			0.008REF		
D	4.900	5.000	5.100	0.193	0.197	0.201
E	4.900	5.000	5.100	0.193	0.197	0.201
D1	1.870	1.920	1.970	0.074	0.076	0.078
D2	0.850	0.900	0.950	0.033	0.035	0.037
D3	0.990	1.040	1.090	0.039	0.041	0.043
D4	0.250	0.300	0.350	0.010	0.012	0.014
D5	0.200	0.250	0.300	0.008	0.010	0.012
E1	3.875	3.925	3.975	0.153	0.155	0.156
E2	1.270	1.320	1.370	0.050	0.052	0.054
E3	2.050	2.100	2.150	0.081	0.083	0.085
E4	0.500	0.550	0.600	0.020	0.022	0.024
E5	1.661	1.711	1.761	0.065	0.067	0.069
L	0.350	0.400	0.450	0.014	0.016	0.018
L1	0.350	0.400	0.450	0.014	0.016	0.018
L2	0.575	0.625	0.675	0.023	0.025	0.027
L3	0.350	0.400	0.450	0.014	0.016	0.018
L4	0.400	0.450	0.500	0.016	0.018	0.020
L5	0.450	0.500	0.550	0.018	0.020	0.022
b	0.200	0.250	0.300	0.008	0.010	0.012
b1	0.130	0.180	0.230	0.005	0.007	0.009
e	0.50BSC			0.02BSC		

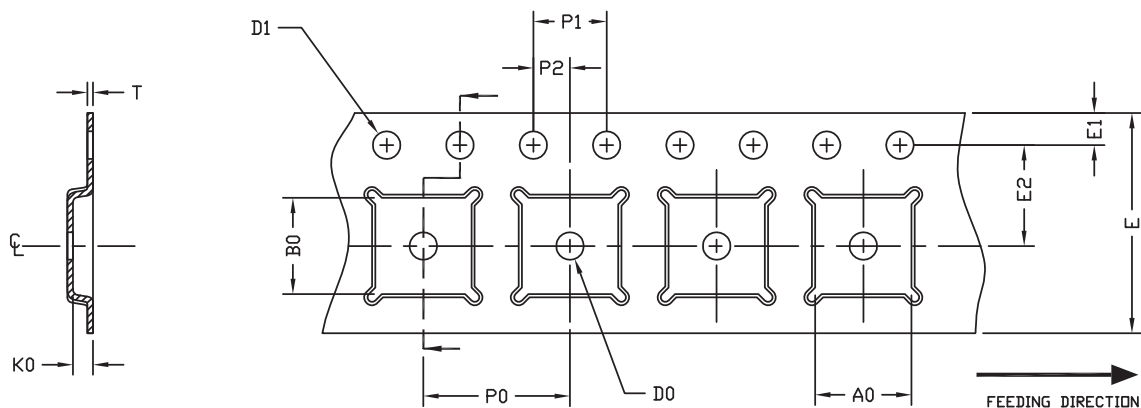
NOTE

CONTROLLING DIMENSION IS MILLIMETER.

CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN5x5A_31L_EP3_S

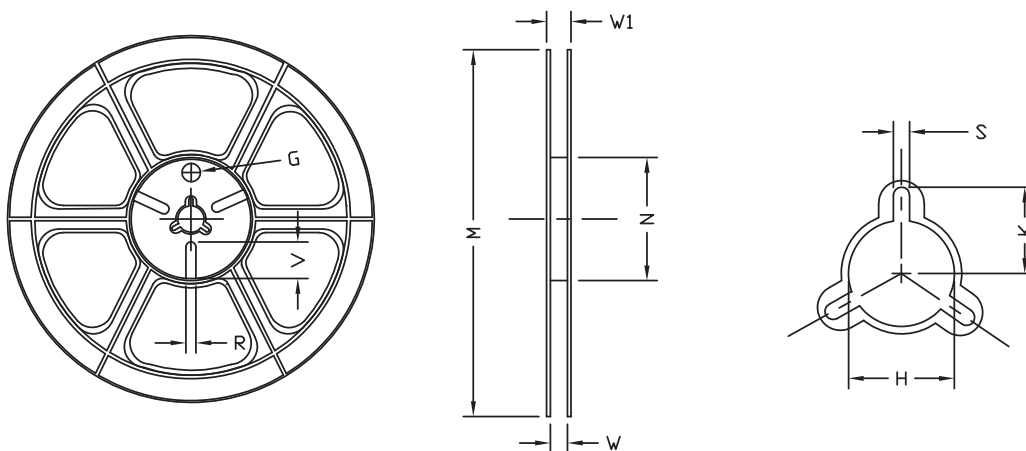
Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 -0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

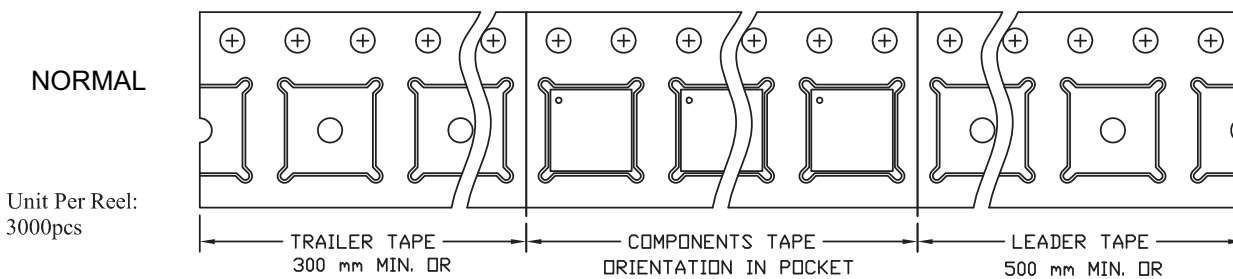
Reel



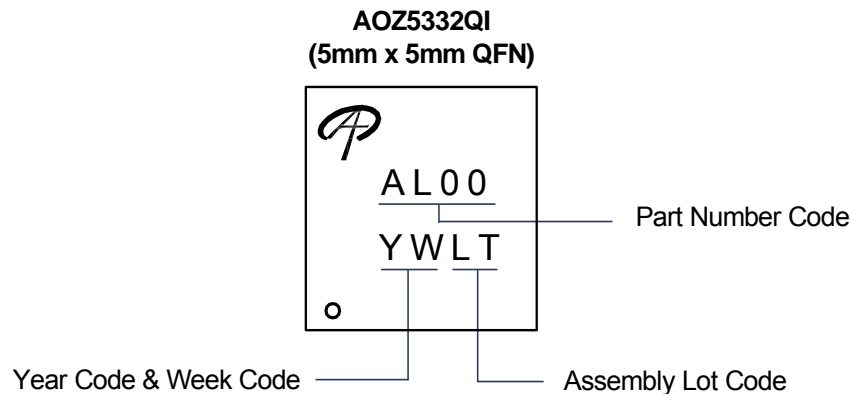
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	Ø330	Ø330.0 ±2.0	Ø79.0 ±1.0	12.4 +2.0 -0.0	17.0 +2.6 -1.2	Ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

Leader/Trailer & Orientation



Part Marking



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