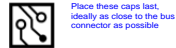
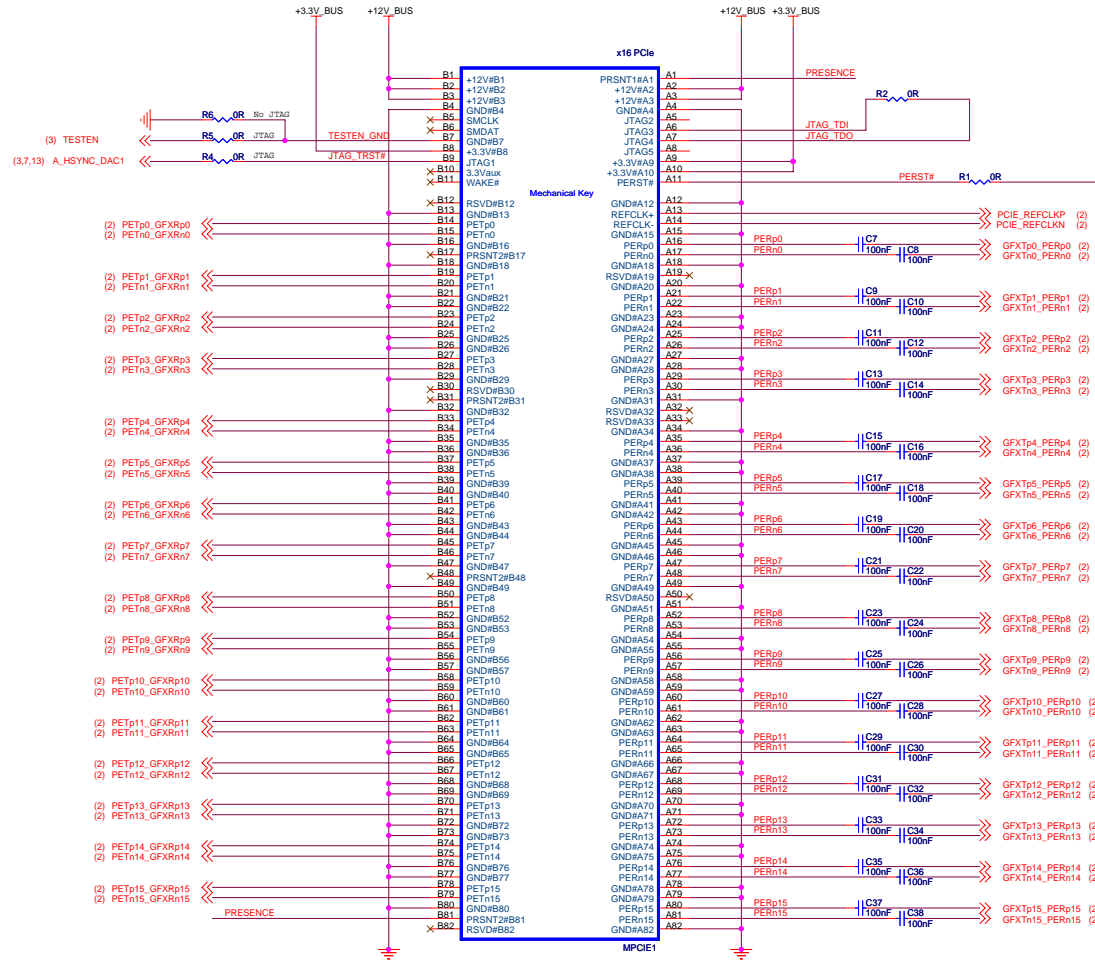
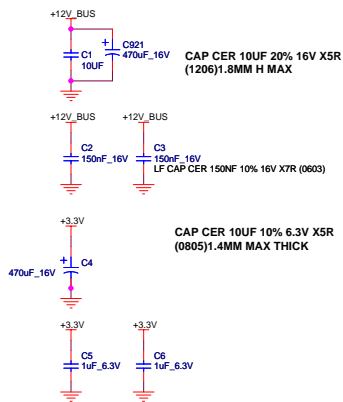


PCI-EXPRESS EDGE CONNECTOR



Place these caps last, ideally as close to the bus connector as possible

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND



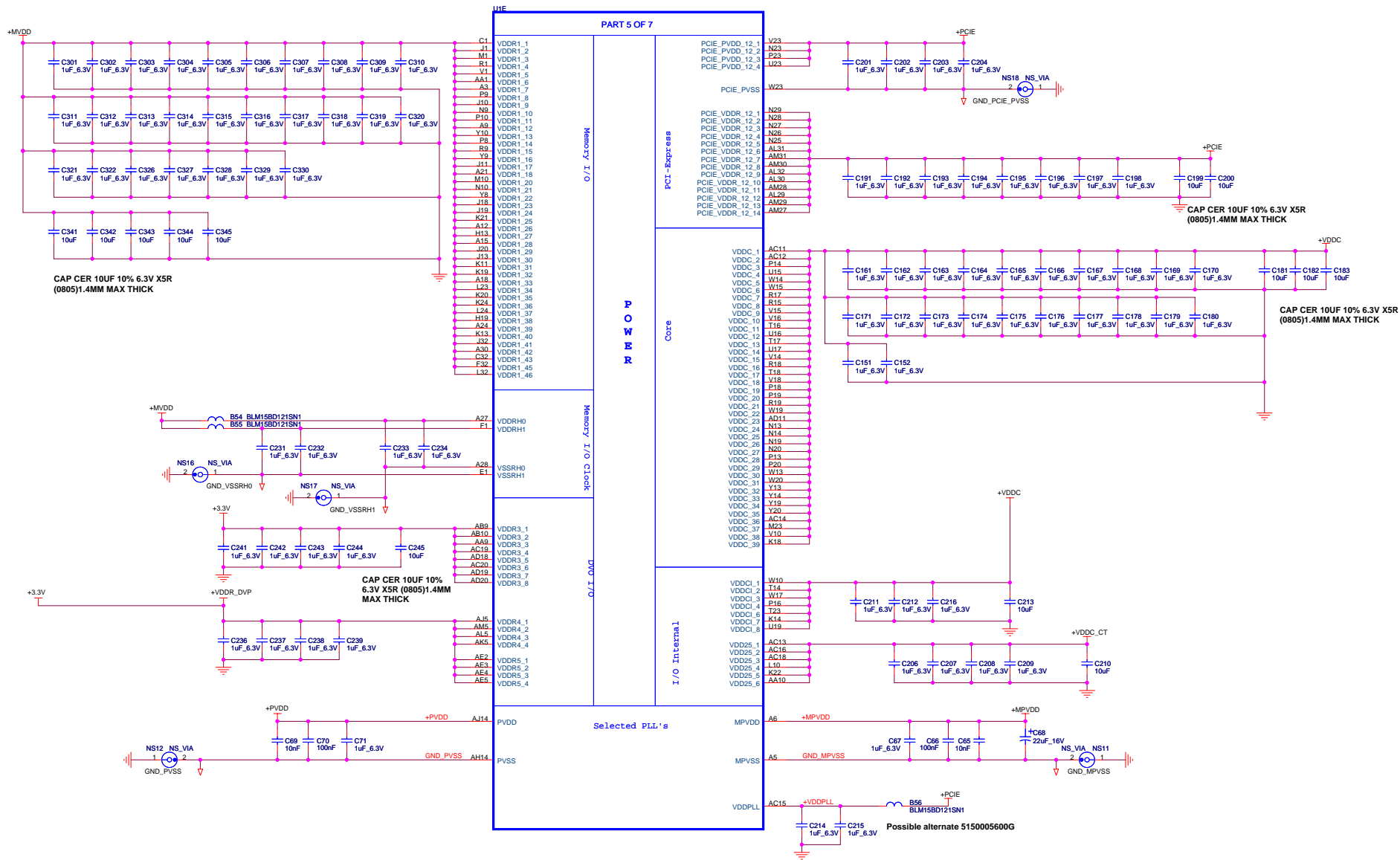
ATI Technologies Inc.

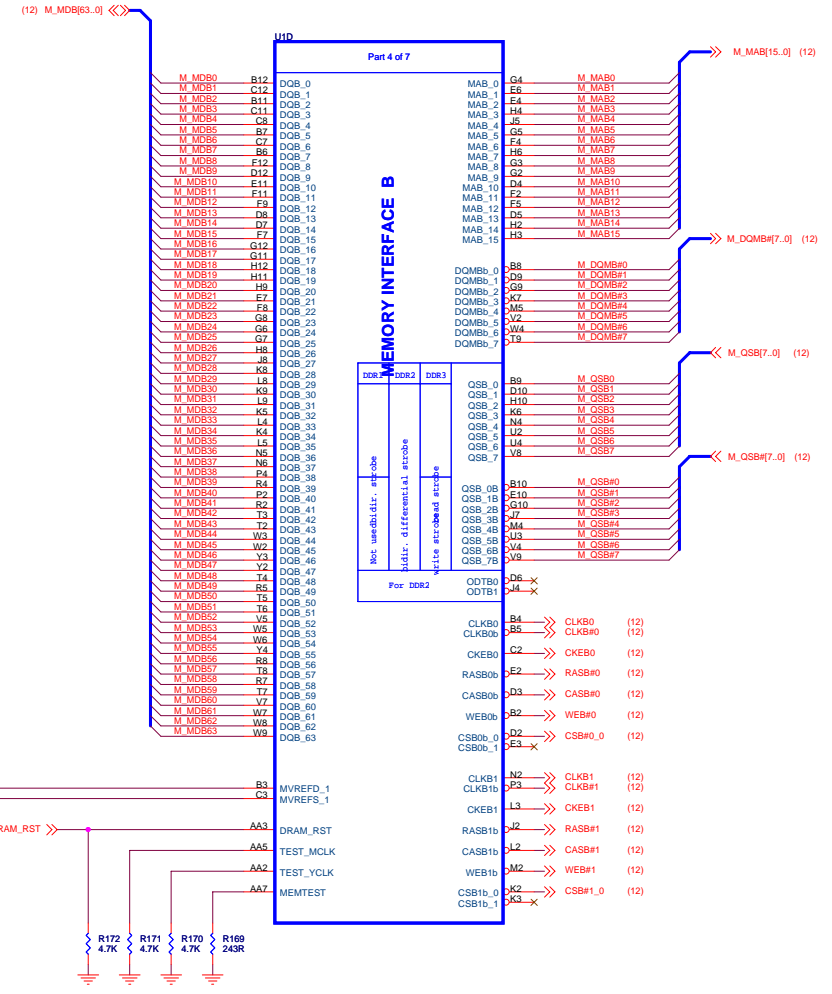
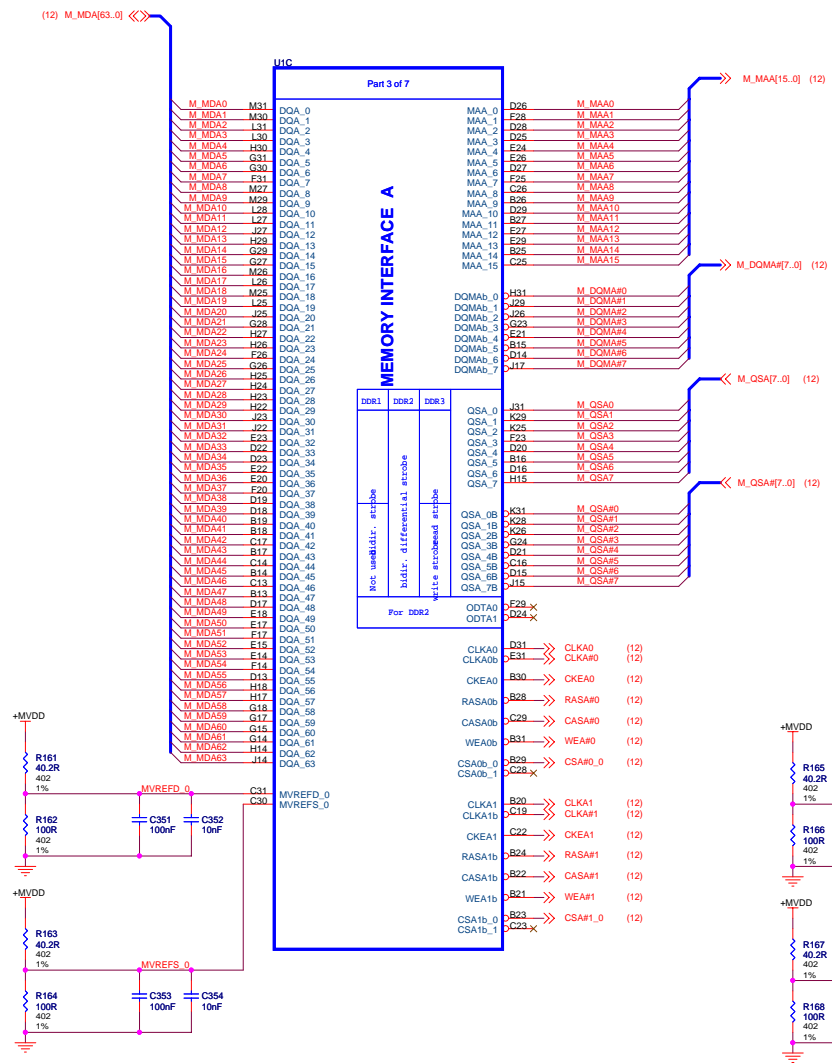
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title: PCI-E RV560LE 256MB GDDR3 Dual DL-DVI-H VIVO FH

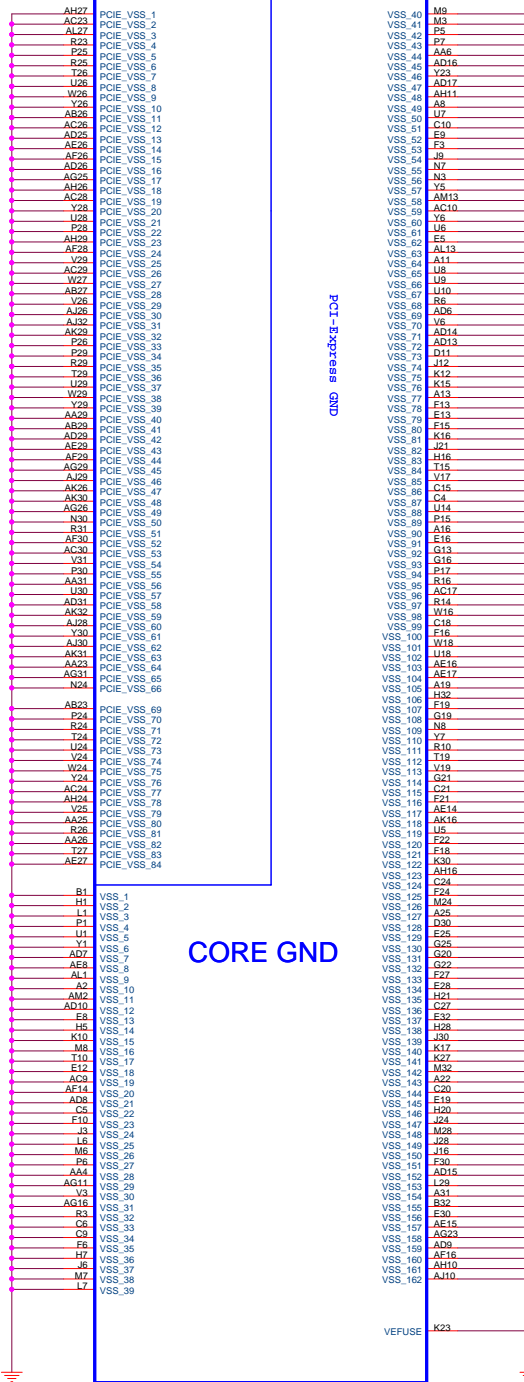
Size: C Document Number: 105-A880xx-00C

Date: Thursday, August 17, 2006 Sheet 1 of 20

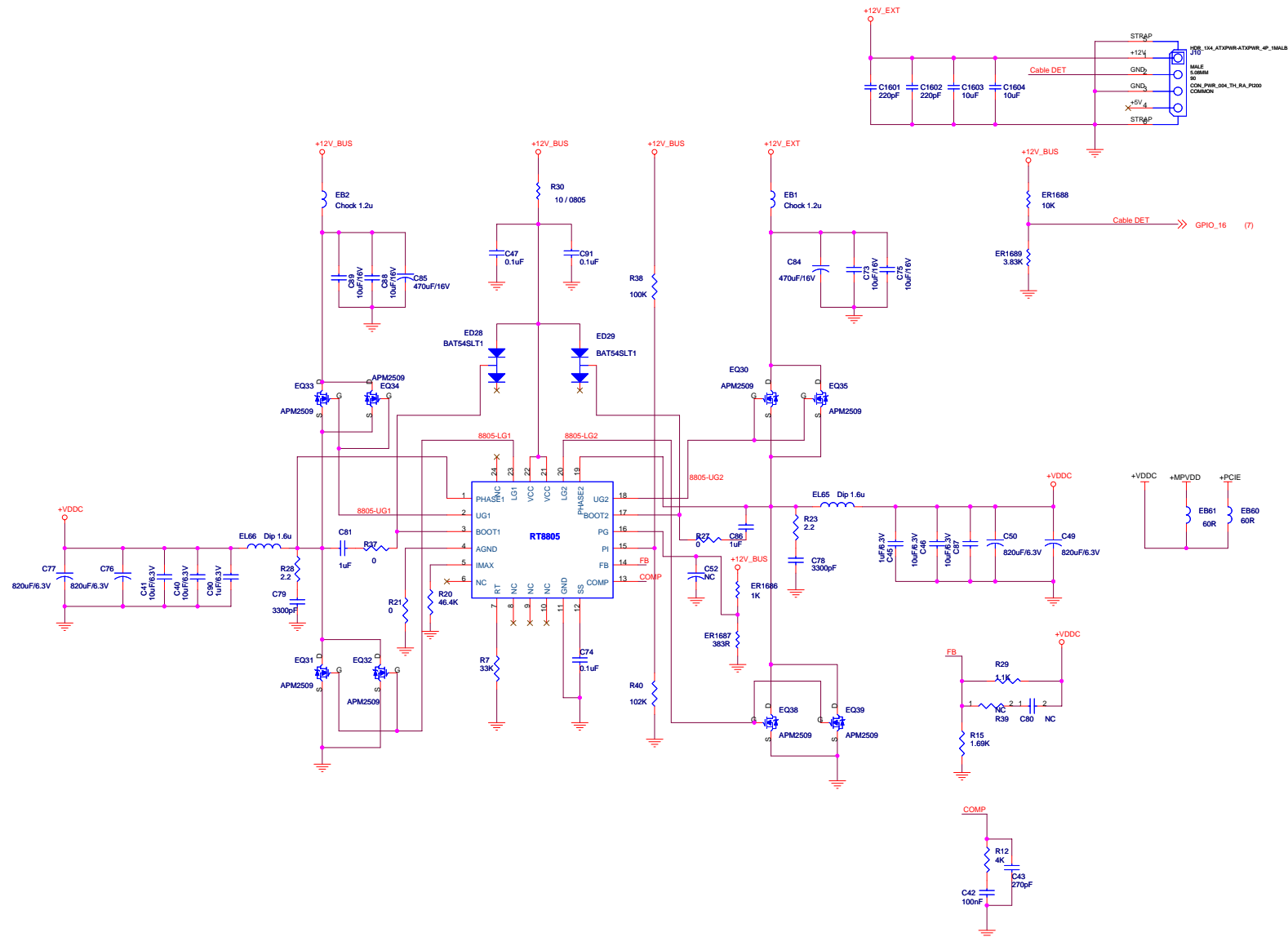




Part 6 of 7

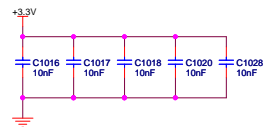
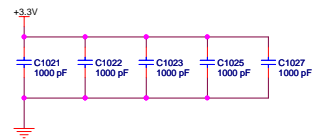
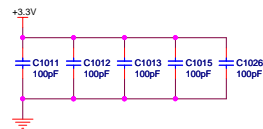
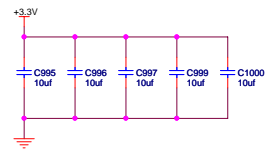
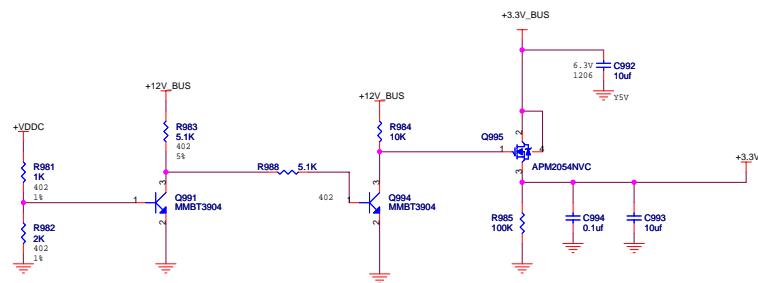


CORE REGULATOR VDDC



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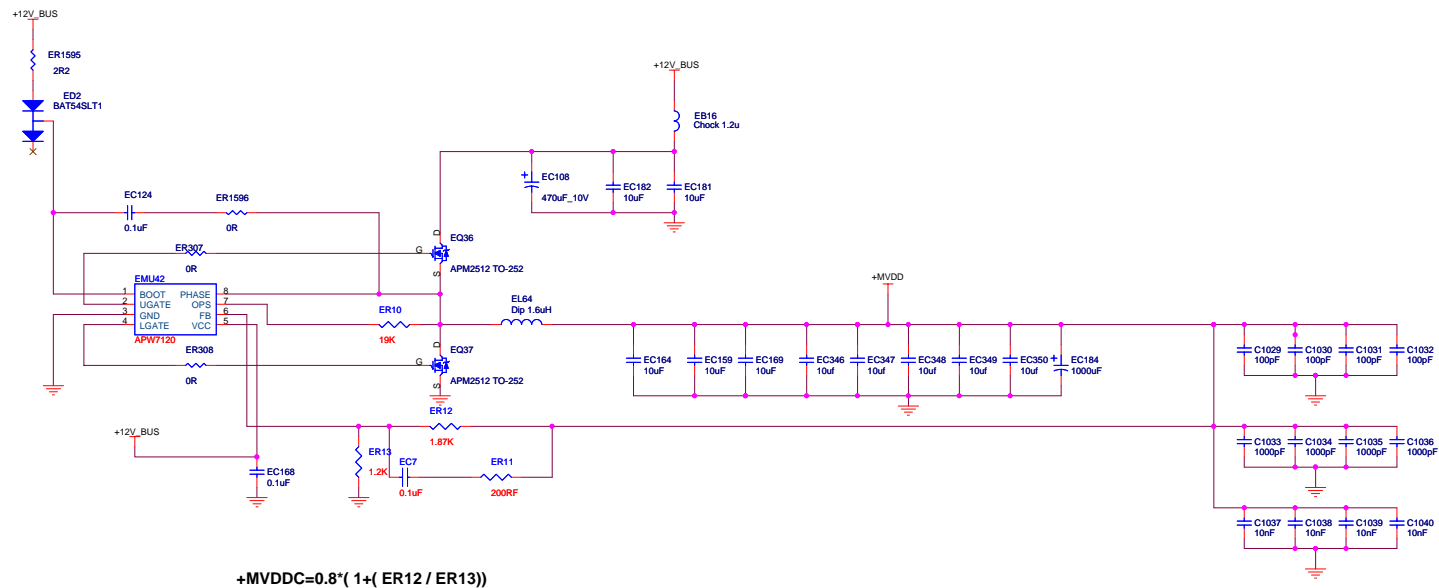
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Size		Document Number				Rev	
Custom		105-A880xx-00C				2	
Date: Monday, August 21, 2006				Sheet 8 of 20			



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Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO	Rev	2
Size	Custom	Document Number	105-A880xx-00C
Date	Tuesday, July 18, 2006	Sheet	9 of 20



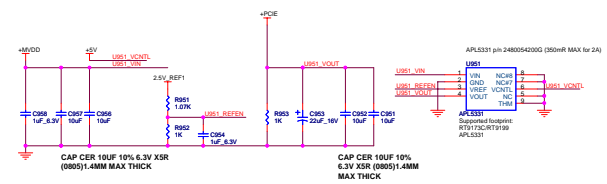
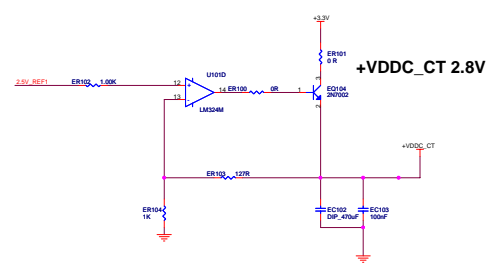
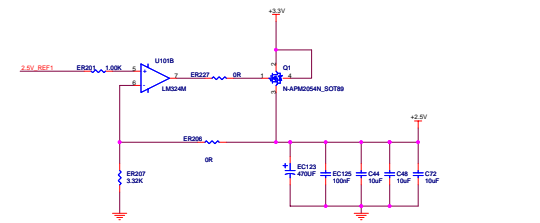
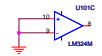
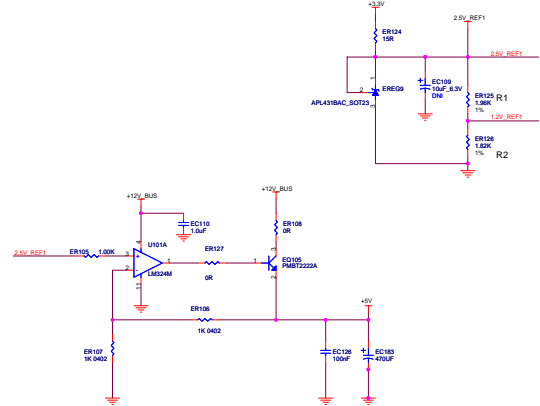
Regulator for MVDD
Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G



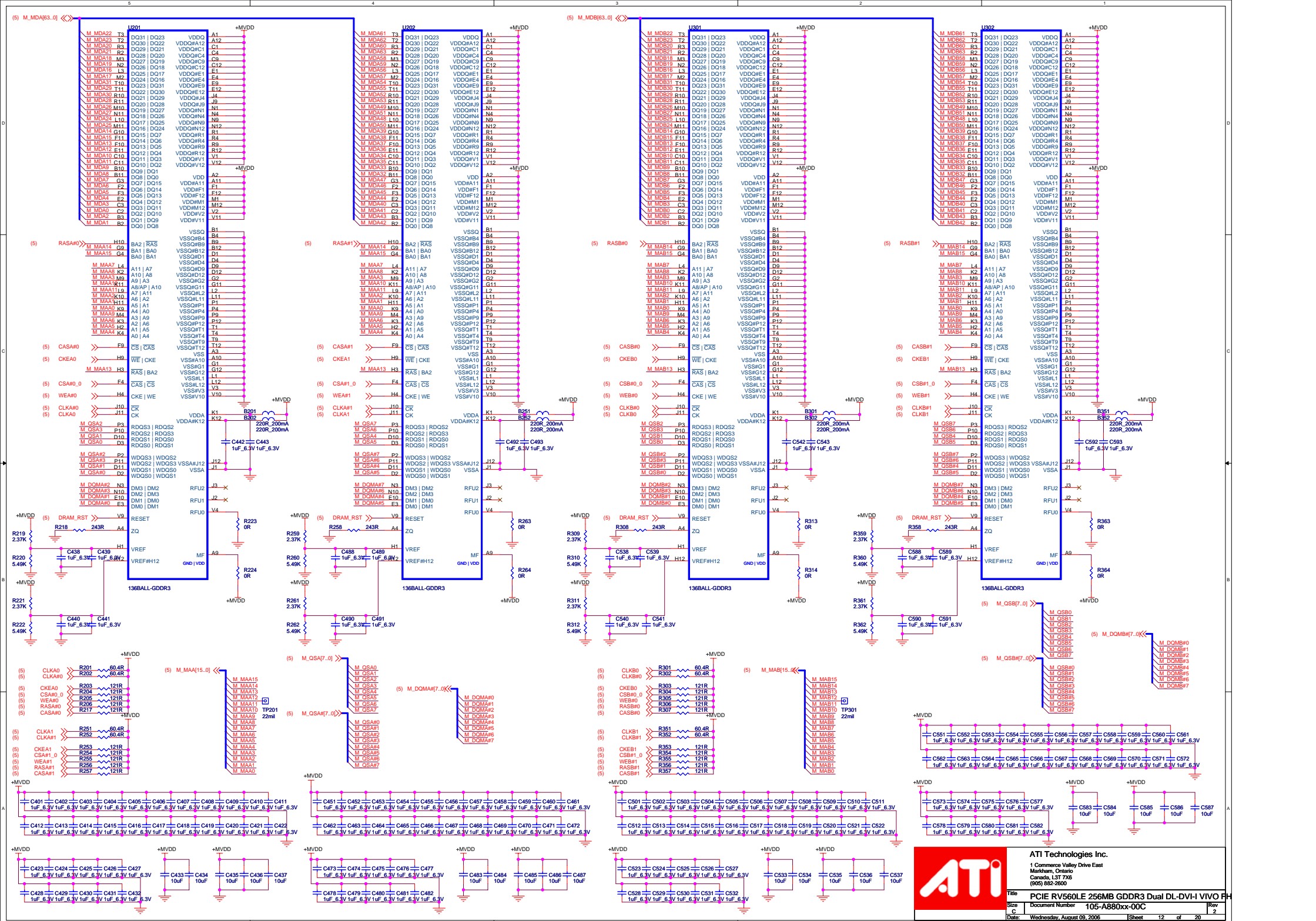
ATI Technologies Inc.
 1 Commerce Valley Drive East
 Markham, Ontario
 Canada, L3T 7X6
 (905) 882-2600

Title	PCIE RV560LE 256MB GDDR3 Dual DL-DVI-I VIVO	Rev	2
Size	Custom	Document Number	105-A880xx-00C
Date	Wednesday, August 08, 2006	Sheet	10 of 20

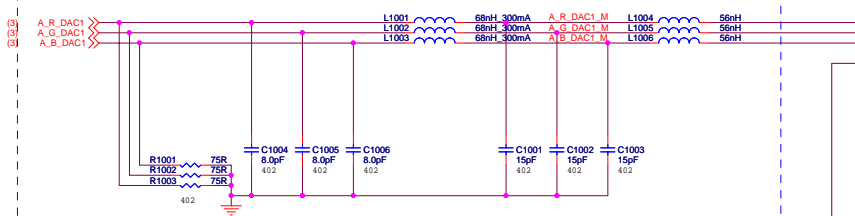


+PCIE 1.2V~1.25V (1.2A)
+MPVDD 1.2V (10mA)

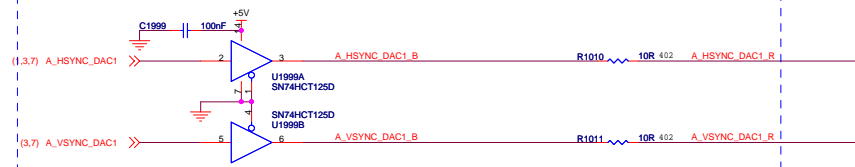
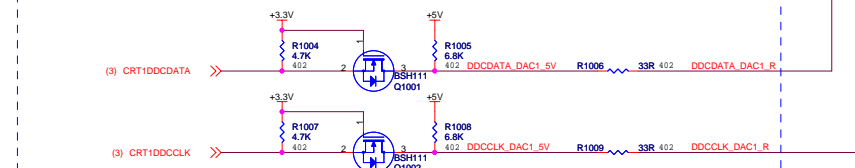




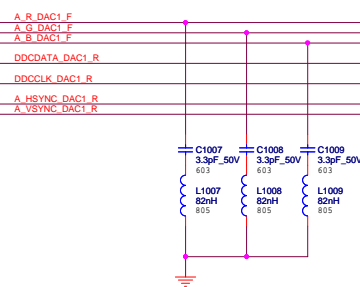
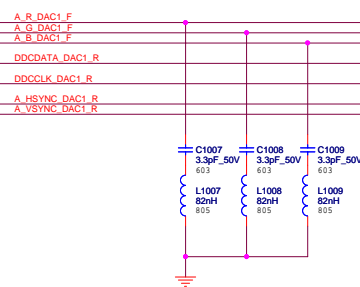
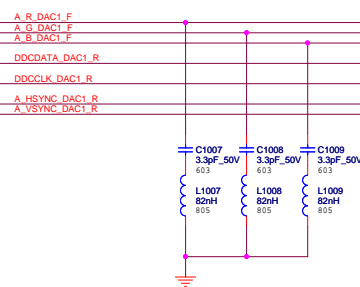
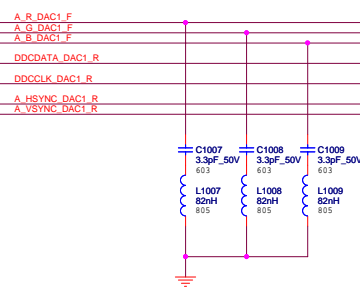
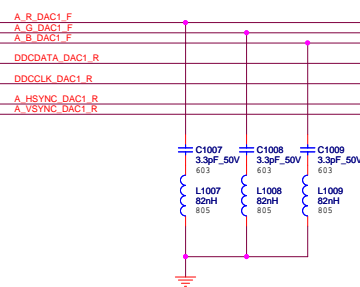
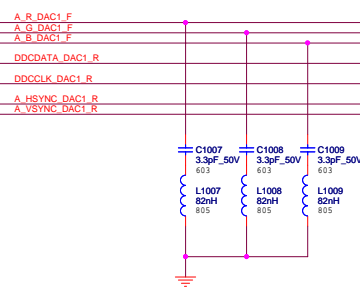
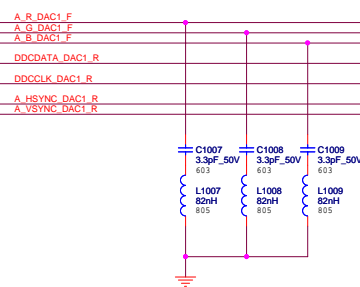
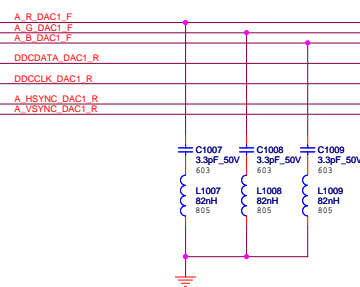
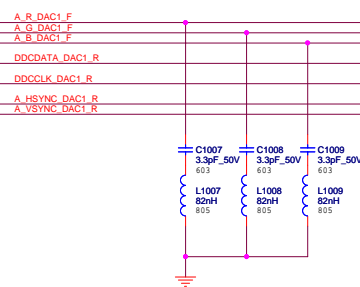
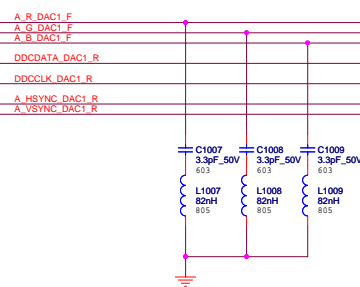
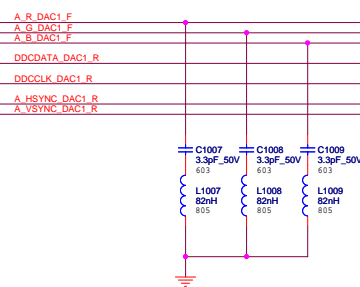
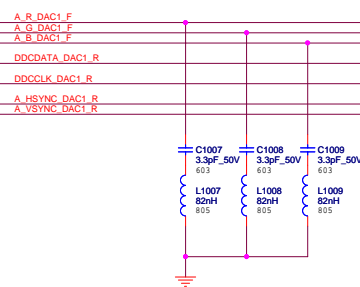
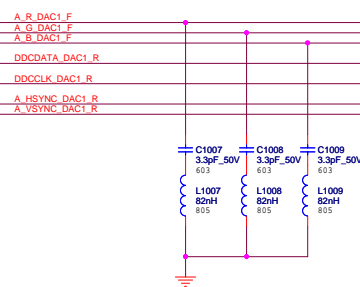
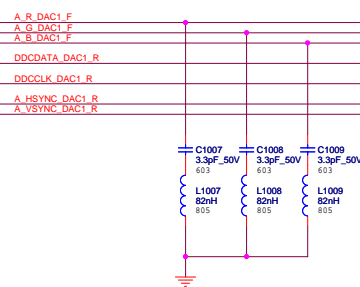
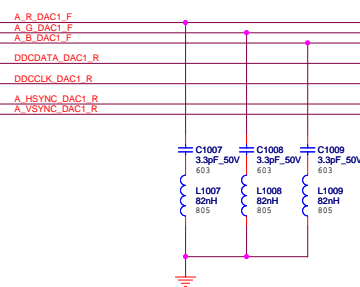
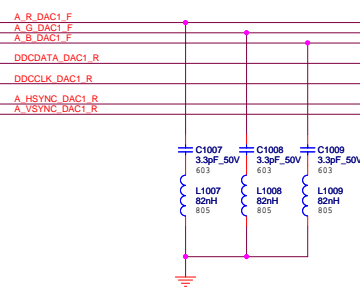
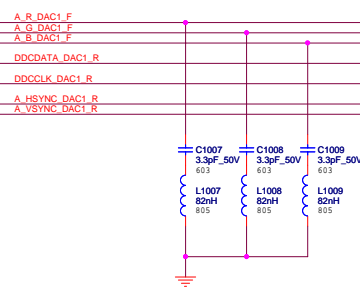
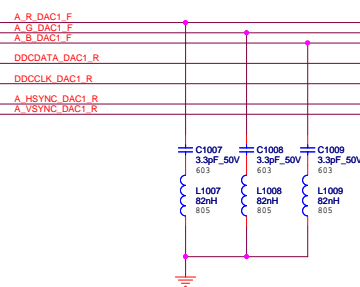
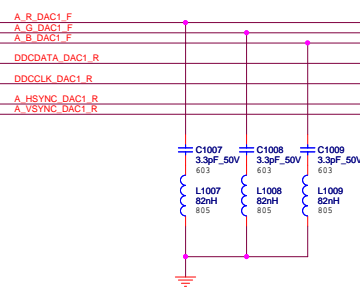
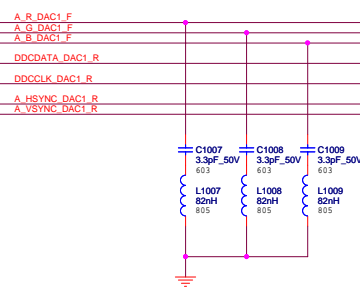
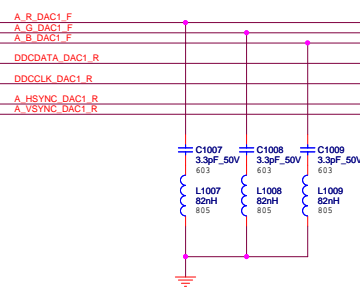
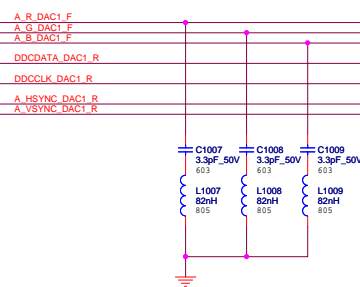
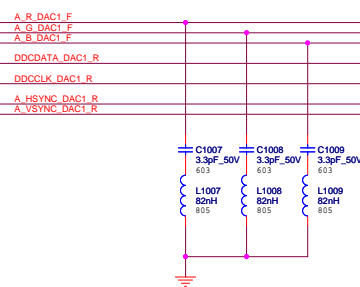
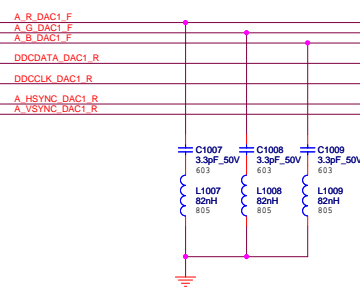
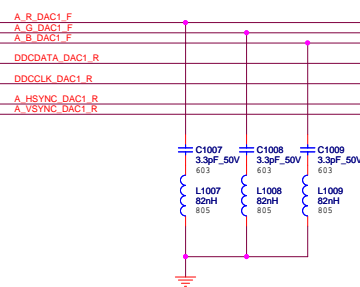
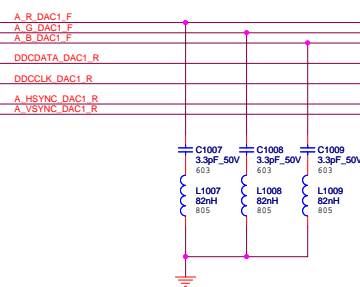
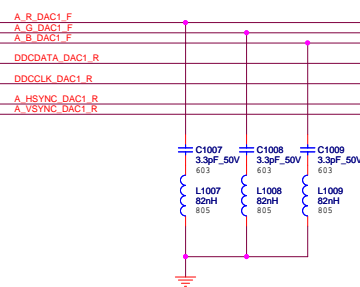
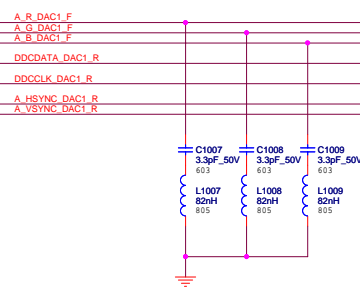
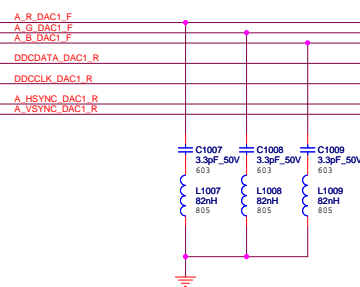
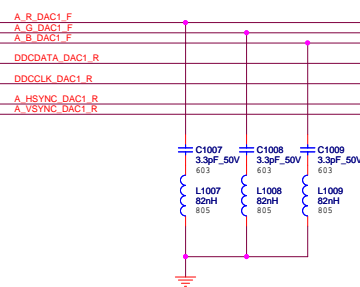
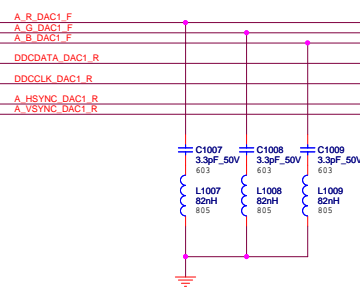
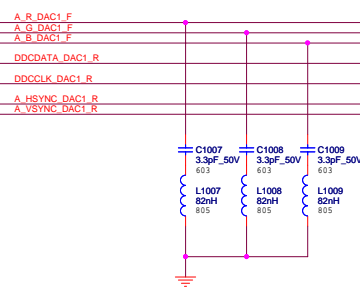
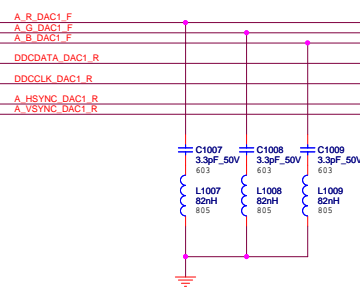
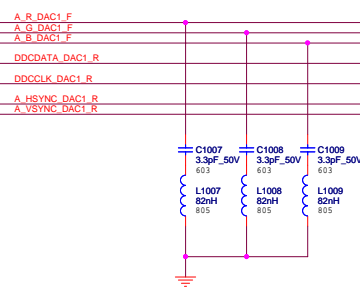
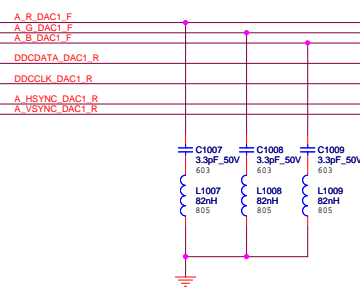
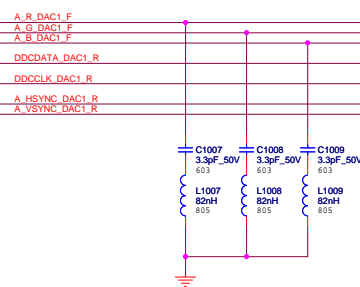
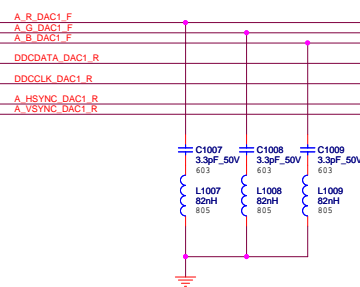
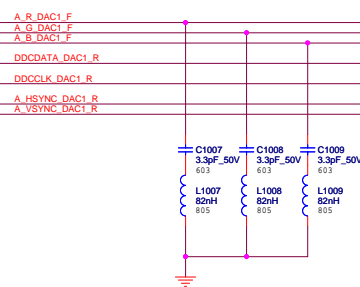
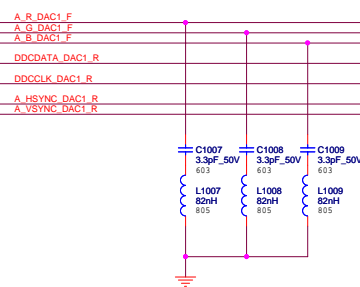
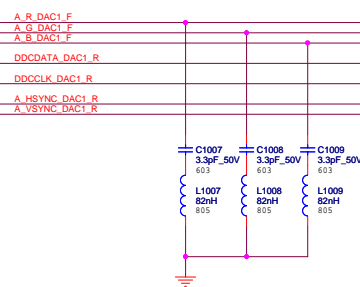
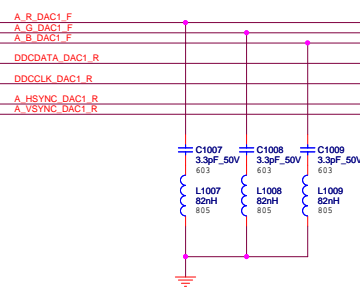
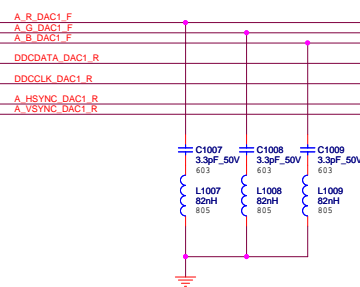
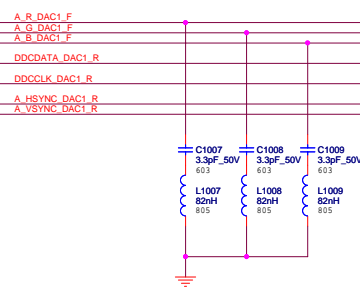
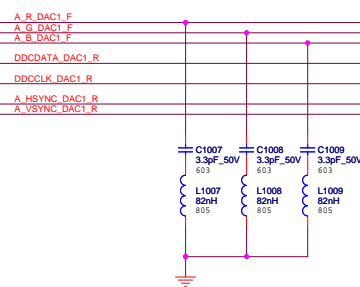
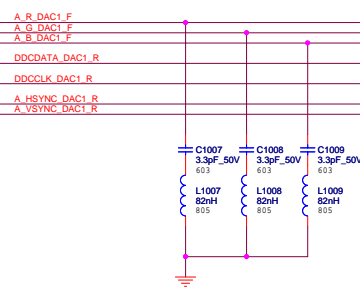
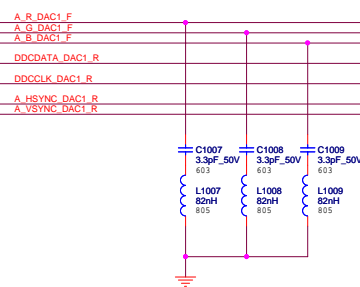
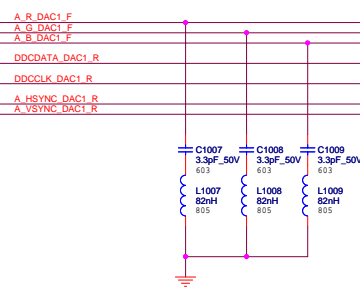
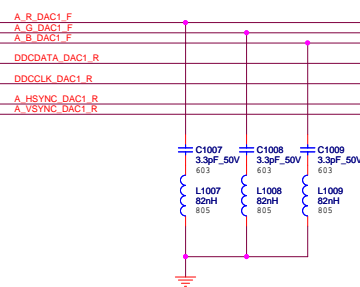
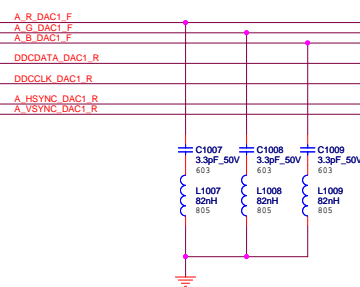
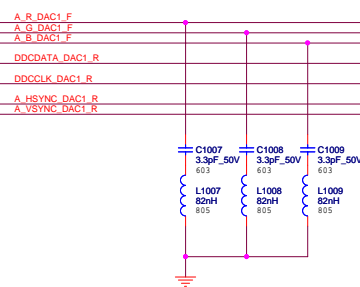
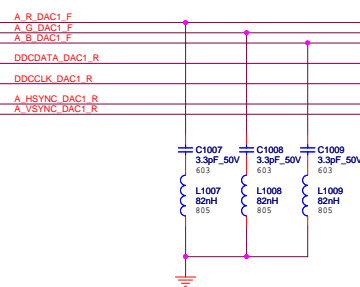
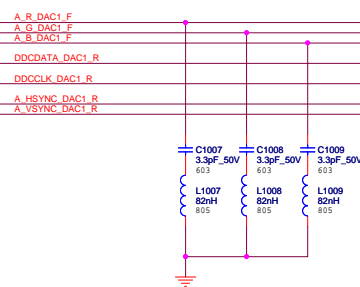
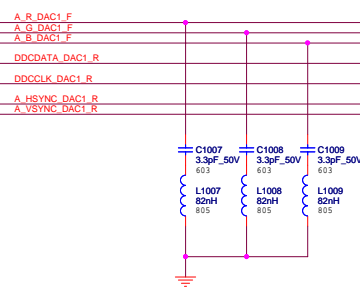
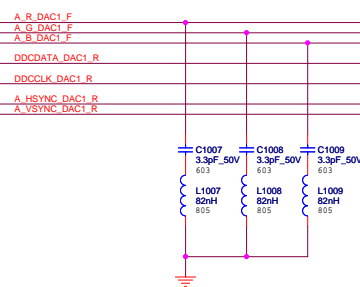
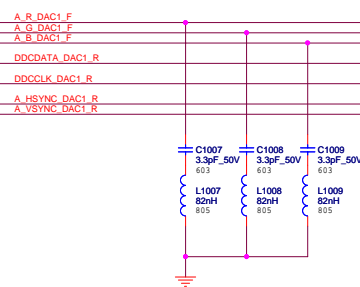
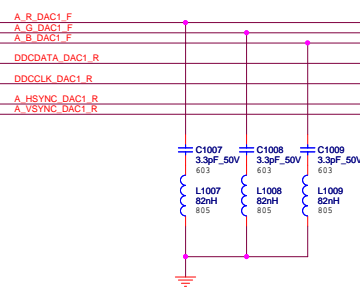
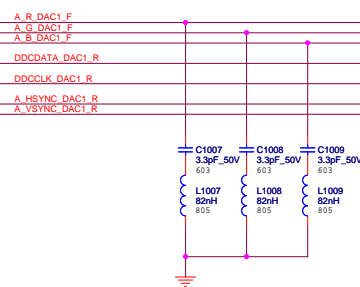
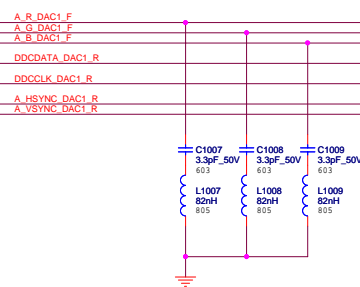
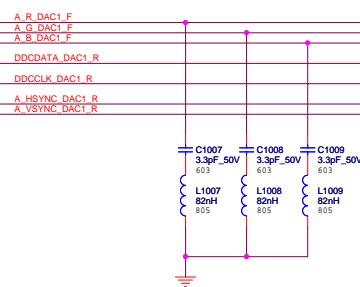
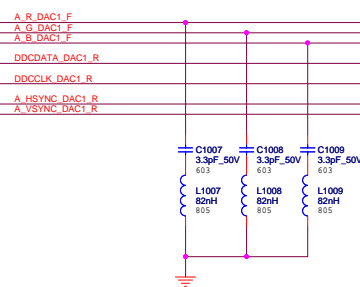
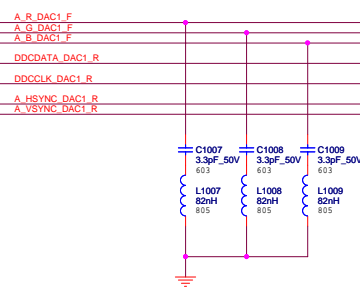
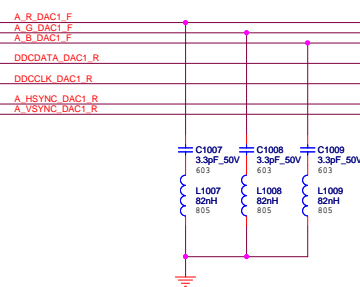
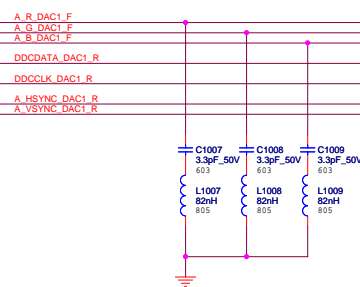
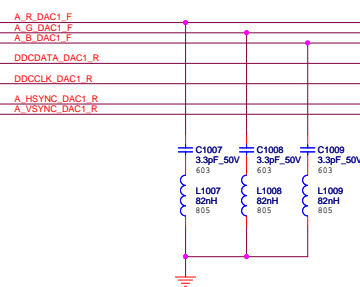
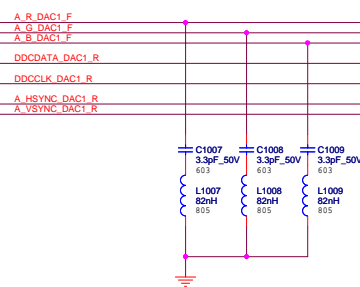
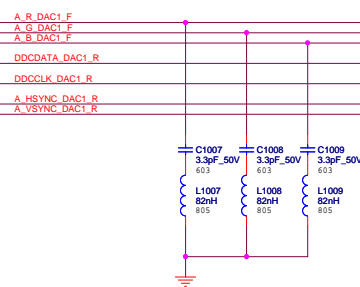
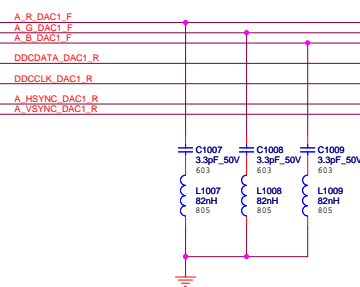
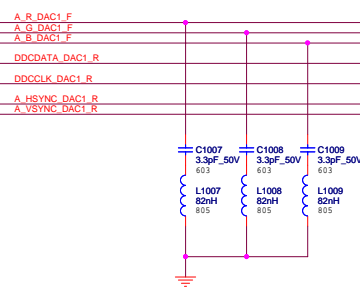
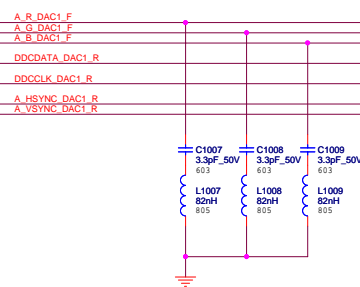
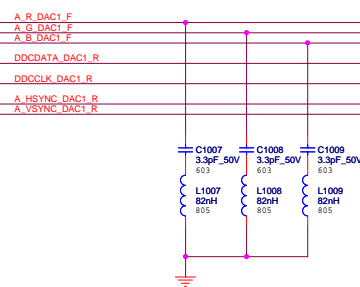
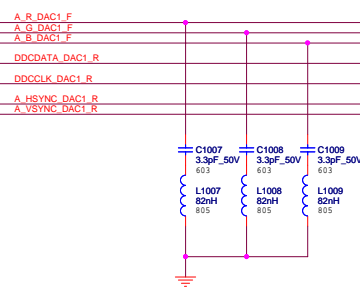
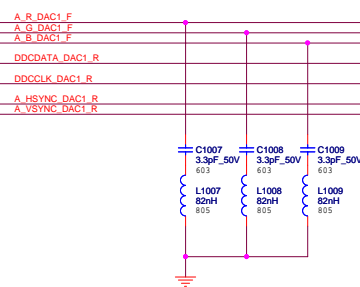
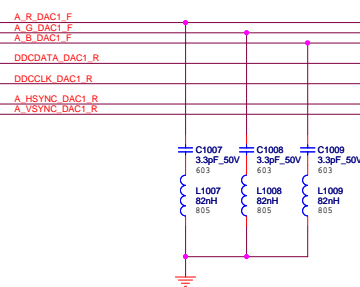
(3) A_R_DAC1
(3) A_G_DAC1
(3) A_B_DAC1



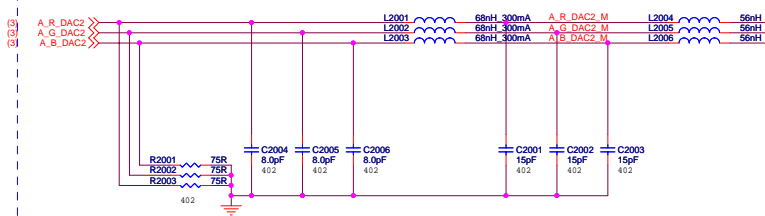
RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane



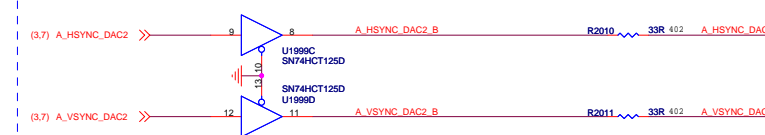
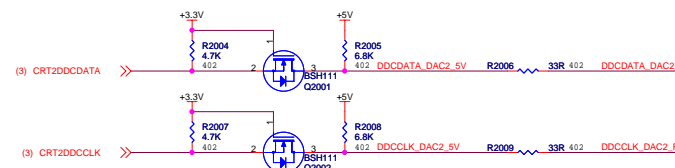
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane



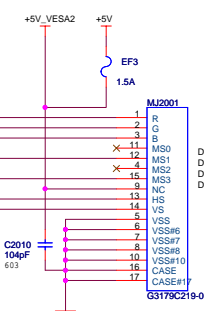
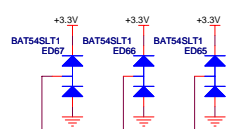
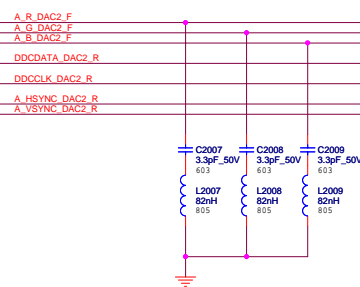
(3) A_R_DAC2
(3) A_G_DAC2
(3) A_B_DAC2



RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane

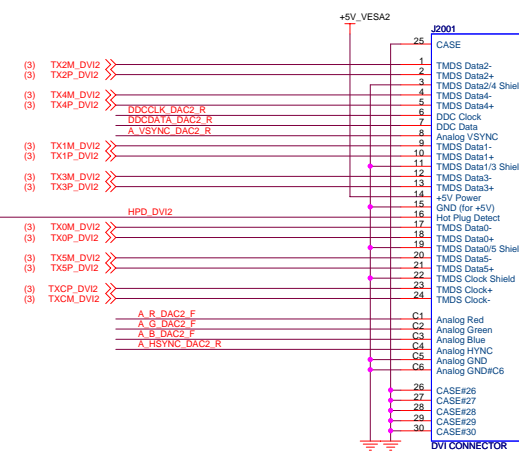
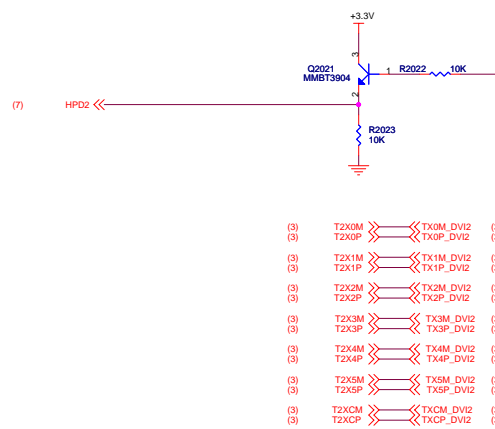


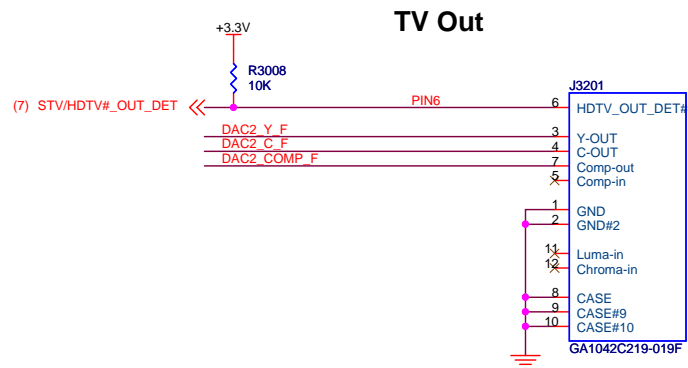
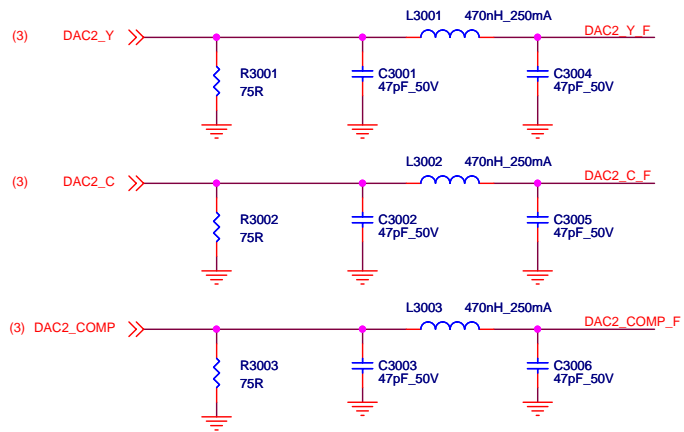
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional SDA
12	Monitor ID bit 1	Data from display	SDA	SDA	Optional SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional SCL
15	Monitor ID bit 3	Open	Open	Open	Optional SCL
9	N/C	+5V	+5V	+5V	Optional
Hardware Support	Mechanical Key	50mA min 1A max	50mA min 1A max	50mA min 1A max	Yes

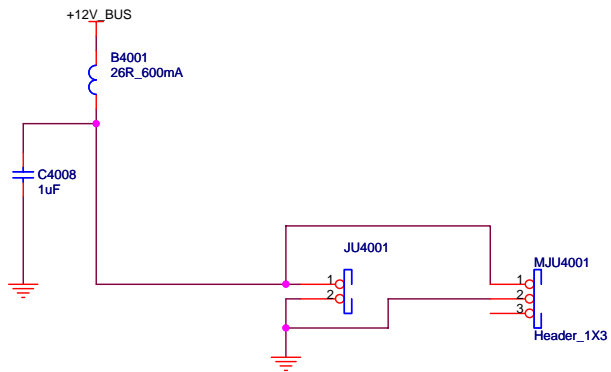
Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





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 (905) 882-2600

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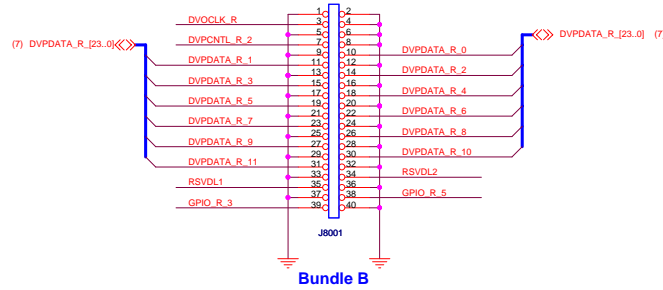


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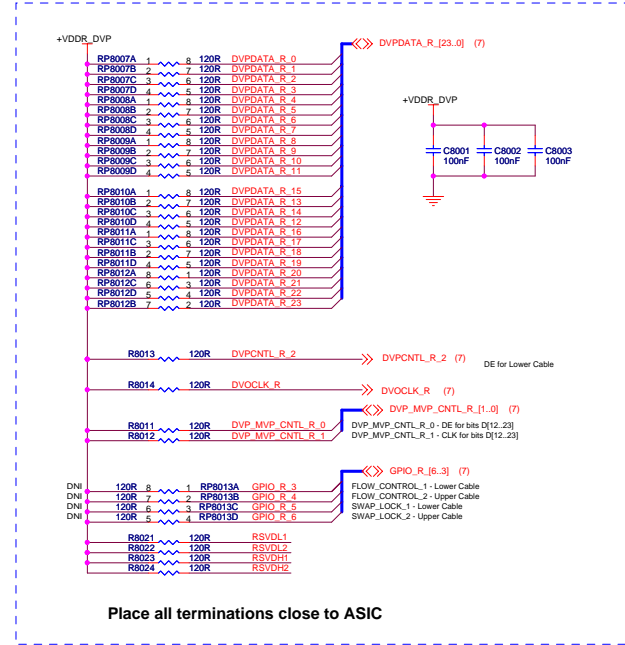
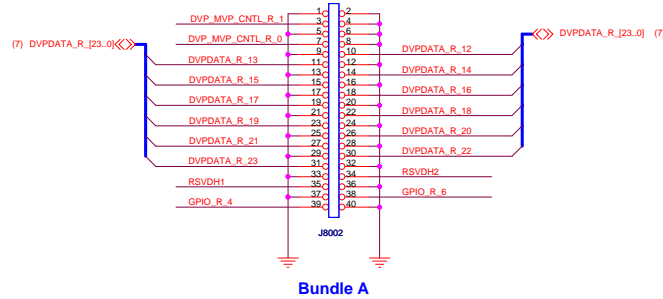
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CrossFire Card-Edge

Lower Cable Card Edge



Upper Cable Card Edge



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DVI/PGA SCREWS

- ASSY-SCREW1

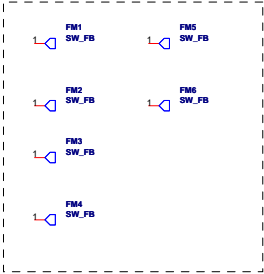
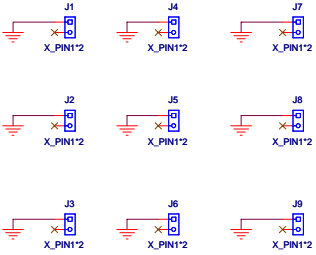
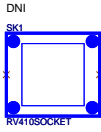
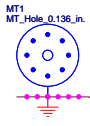
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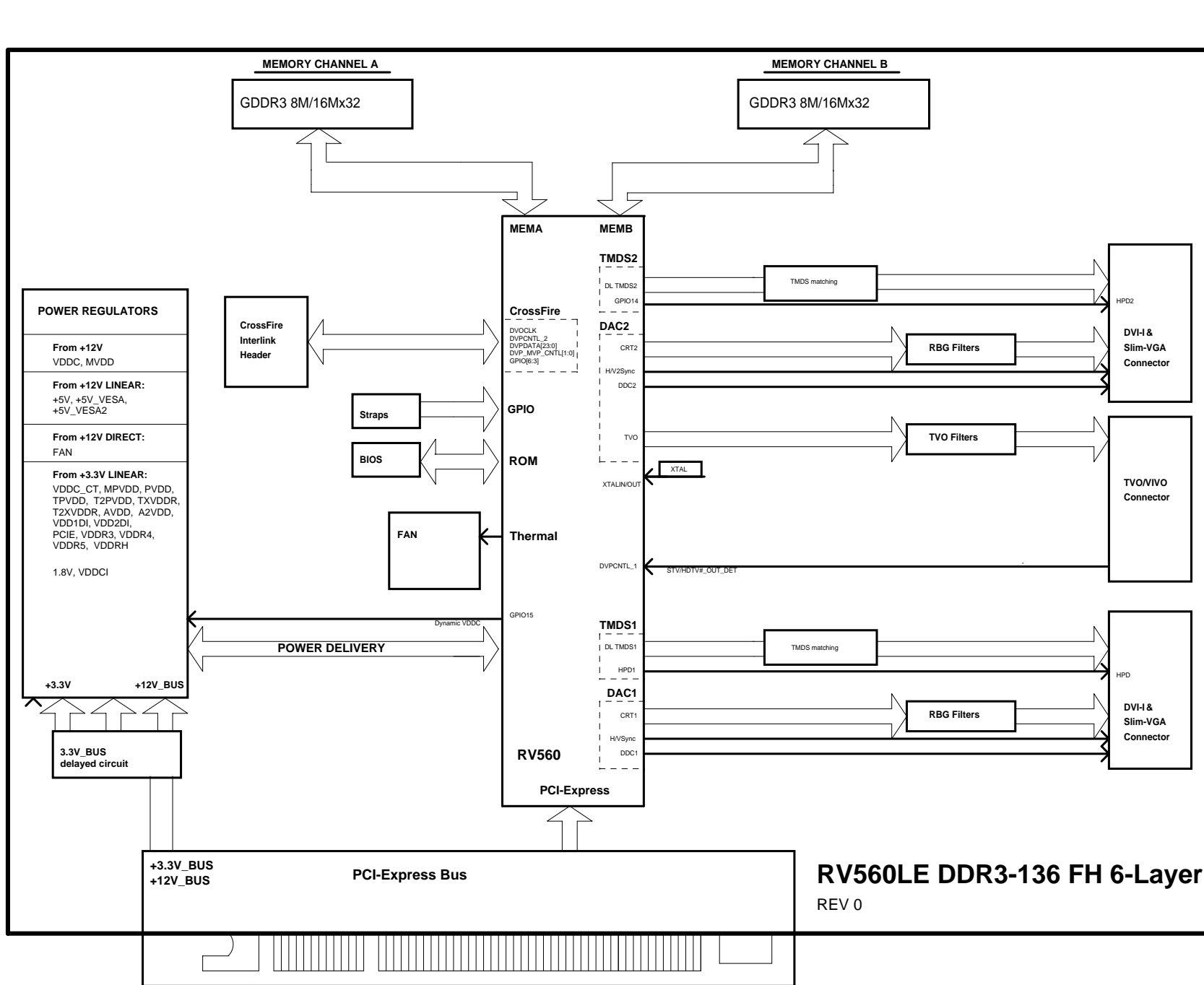
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Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/02/27	Design based on 105/109-A671xx-20 (pg 03) Change TMDS power decouplings, change crystal/oscillator sharing circuit (pg 04) Change VDDR4/VDDR5 to have 1.8V/3.3V option , Separate VDDCI from VDDC option, add decoupling for VDDC and VDDCI (pg 07) Connect DVO to CrossFire Edge Connector, change pin straps matching RV570, remove PAL/NTSC header, H/W FPGA Crossfire (pg 08) New SMPS Tile (A800-00A-46) for RV560 VDDC 46A solution (pg 09) New SMPS Tile (A800-00A-30_VT) for RV560 VDDC 30A solution (pg 10) New SMPS Tile (A800-00A-8) for RV560 MVDD 8A solution (pg 11) Remove 1.8V regulator, LED for Dyn. VDDC, add VDDCI regulator (pg 12) Improve power sequencing and +5V sequencing from +5V_SMPS, add LDO new footprints, remove MVDD to 2.5V short (pg 13) Remove +5V_EN, change +5V to +5V_SMPS with current up to 115mA, add VDDC output current monitoring for debugging (pg 15) Remove H/W FPGA CrossFile options, change ESD protection to +5V_VESA (pg 16) Remove H/W FPGA CrossFile options and chnige ESD protetion to +5V_VESA2 (pg 17) Change RTAVDD regulator for power sequencing, add Dell specific TVO mapping (pg 18) Update fan control for other thermal monitoring IC options (pg 19) Add CrossFire Edge Connectors and 1.8V regulator
1	00B	06/03/06	Fix DFM issues on layout (pg 03/07) Add clock source to GenericA/B for ASIC debugging (pg 13) Add J601 for ease of bring up for VDDC current monitoring
2	00C	06/05/08	(pg 03) Add MR25 and C61 for VREFG (pg 03) Change GND_TXVSSR and GND_T2XVSSR directly to GND (pg 08) Remove VR650, VR663, MR676, MR677, MR673, MU678 and U678, modify BUSEN and share it to MU601 (pg 08) Remove redundant external detection circuits (pg 11) Replace RP801 with B801-B803 (pg 11) Add resistors to dissipate Q_MVDD, sourced from 3.3V_BUS (pg 12) Add RP952 for PCIE VDDC share, add 5V_EN, remove Q998 for RTAVDD_ENb (pg 13) Add Q922 for improved power dissipation, use series R926-R928 dissipation and add 5V_EN option (pg 17) Replace RTAVDD regulator with AP1118 (pg 19) Crossfire pin mapping change, 50R impedance matched (Layout) Power distribution layout change (Layout) TMDS1 and TMDS2 termination resistor changes

Title				RV560LE 256MB GDDR3 VGA VIVO DVI-I (DL-TMDS1+DAC2) FH			
Size B		Document Number				Rev	
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