

P977-A01: G96, GB1-128, GDDR3, DL-DVI/VGA, DL-DVI/VGA, SD/HDTV

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- Page 19: POWER SUPPLY: FBVDDQ , PEX\_VDD
- Page 20: POWER SUPPLY: NVVDD

REV HISTORY

- Version : 0A
- 6/26 PAGE 16 add D701 for 4PIN FAN control protect
- 6/26 PAGE 12 DVI change to HDMI  
add I2CD\_SCL, I2CD\_SDA  
add GPIO17\_HDMI\_CMC
- PAGE 14 disable DACB (TVfunction)
- 6/27 PAGE 20 change NVVDD power solution (UP6205)
- 6/30 PAGE 20 add GPIO5\_VSEL0
- PAGE 19 change FBVDD output choke footprint  
add R1901 for RT9259A, add R1902 for UP6161  
change Hi-Low side MOS from power pack to T0252
- 7/01 PAGE 19 change R511 from 0402 to 0603  
change R515 to 100K ohm for 300Khz  
change C558,C550 from 0603 to 0805, 25V  
add R1903 for Hi-side GATE resistor
- 7/02 PAGE 16 add R1601,R1602,R1603 ,R1604 pull high resistor for I2CD (pull high 5V)
- PAGE 17 add R1701 (no stuff), R1702(stuff), R1703(no stuff), R1704(no stuff), R1705(no stuff) pull down resistor for HDA
- PAGE 18 change L5 footprint (12V input)
- PAGE 16 add D1201,D1202 for protection diode (I2CD)  
add LB1201, LB1202, C1201, C1202 for EMI filter
- PAGE 20 change UGATE resister R7302,R7313 footprint to 0805
- 7/04 PAGE 11 add EMI bridge (R1101~R1107)
- 7/04 PAGE 11 add FM1 ~- FM6 for optical point
- 7/09 PAGE 19 del output choke colay L17  
change Q2 from T0252, PEX\_VDD output CAP change to 1000 UF\_DIP
- 7/09 PAGE 19 change L5 foot print to CHK\_D2\_P5
- 7/10 PAGE 15 add EM100~EM103 for EMI SPRING

- Version : 10
- 8/22 PAGE 16 add R1216, R1217, R1218, R1219 bridge resistor for EMI
- PAGE 19 del C113, add R1904 for UPI 6161 OCP resistor

REV	VARIANT	NPVN	ASSEMBLY
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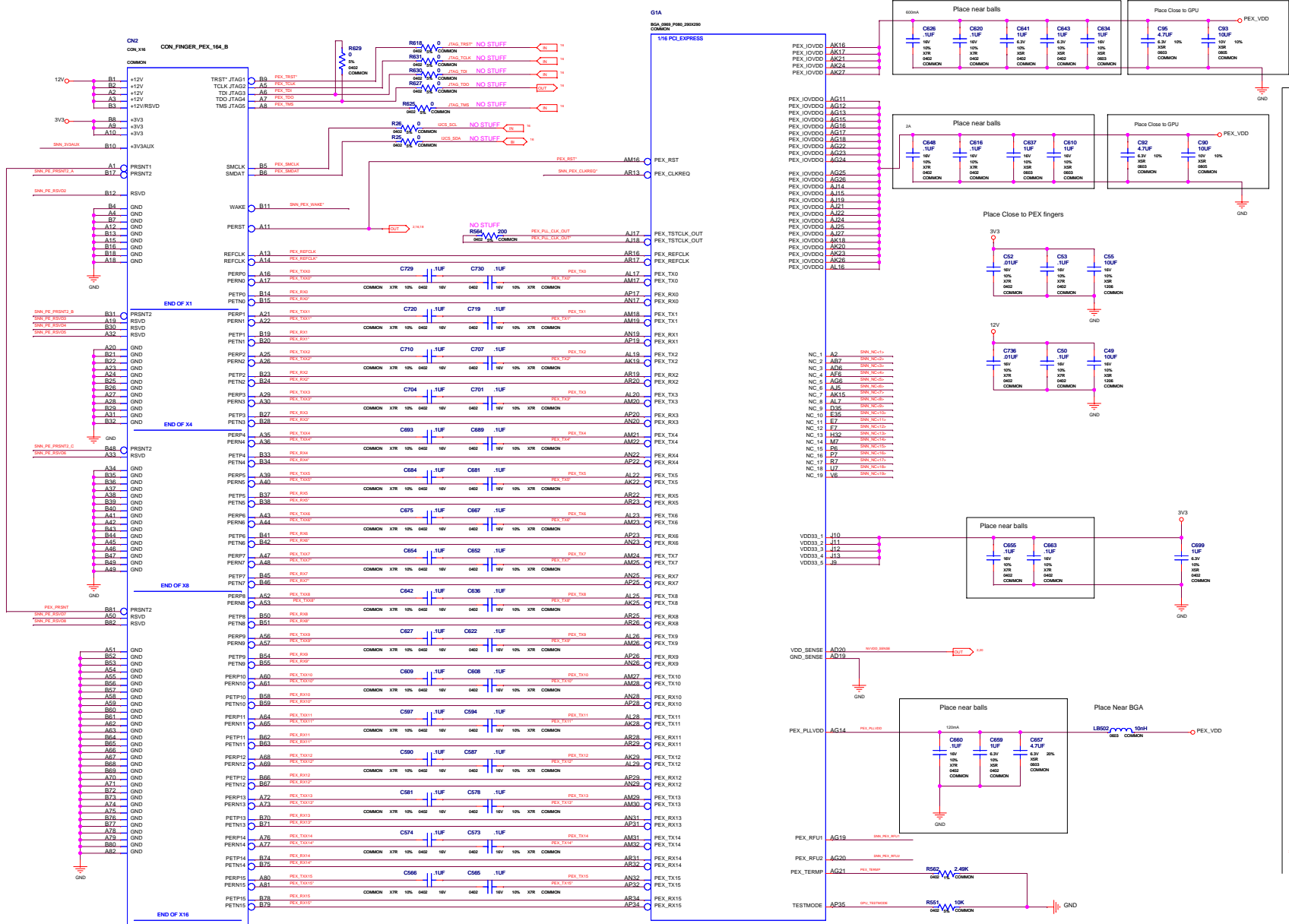
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PAGE DETAIL	TABLE OF CONTENTS

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# 16X PEX INTERFACE



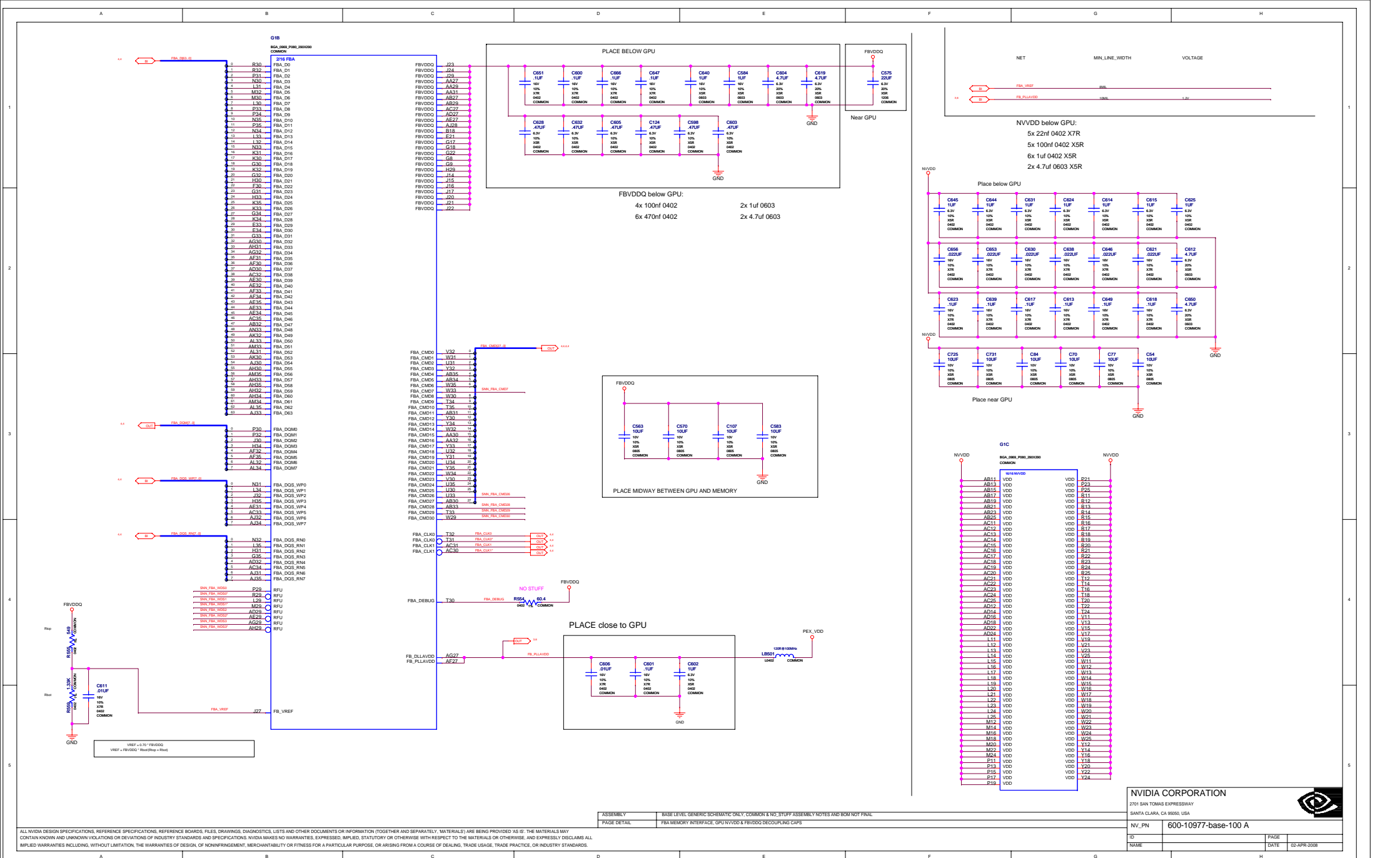
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PEX_2	PEX_2	NO	NO
PEX_3	PEX_3	NO	NO
PEX_4	PEX_4	NO	NO
PEX_5	PEX_5	NO	NO
PEX_6	PEX_6	NO	NO
PEX_7	PEX_7	NO	NO
PEX_8	PEX_8	NO	NO
PEX_9	PEX_9	NO	NO
PEX_10	PEX_10	NO	NO
PEX_11	PEX_11	NO	NO
PEX_12	PEX_12	NO	NO
PEX_13	PEX_13	NO	NO
PEX_14	PEX_14	NO	NO
PEX_15	PEX_15	NO	NO

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ASSEMBLY: BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON AND VIO. 3/10/07. ASSEMBLY NOTES AND BOM NOT FINAL.  
PAGE DETAIL: PCI EXPRESS INTERFACE, PEX\_VDD DECOUPLING CAPS

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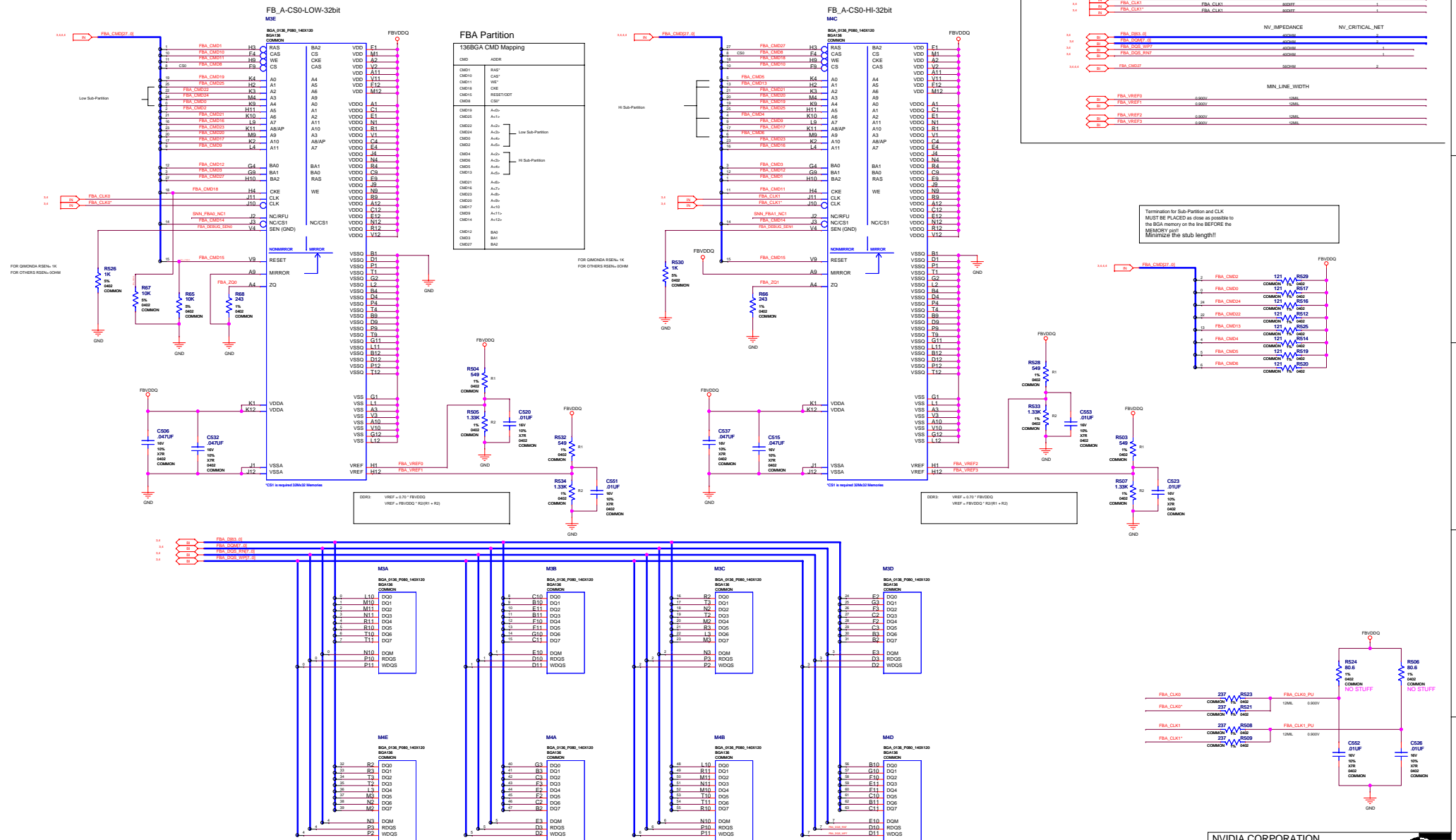
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NAME	DATE 02-APR-2008



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY INTERFACE, GPU NVVDD & FBVDDQ DECOUPLING CAPS


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<b>NAME</b>		<b>DATE</b>	02-APR-2008

Framebuffer: Partition A 16/32Mx32 BGA136 GDDR3



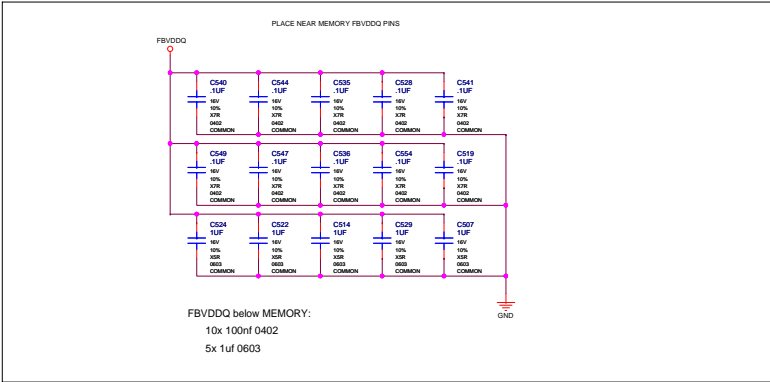
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA 1632Mx32 GDDR3 MEMORIES, FBA COMMAND BUS PUS, FBA CLK TERMS

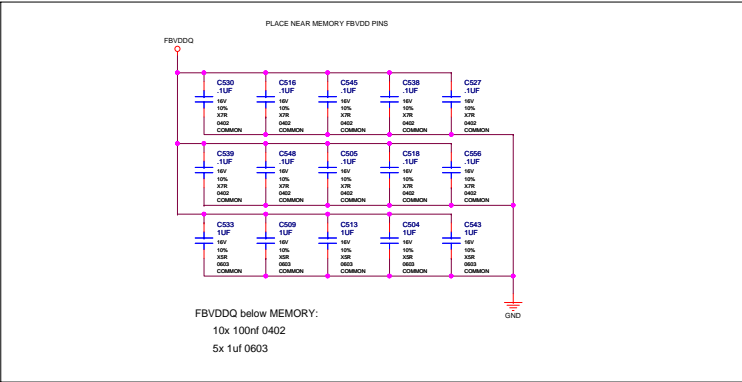
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<b>NAME</b>		<b>DATE</b>	02-APR-2008

FRAME BUFFER: PARTITION A DECOUPLING

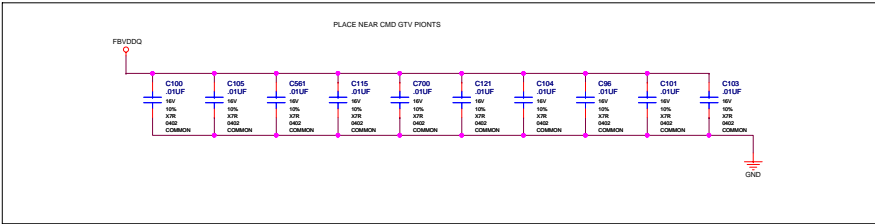
Decoupling for FBA 0..31



Decoupling for FBA 32..63



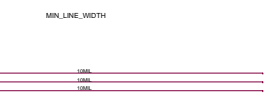
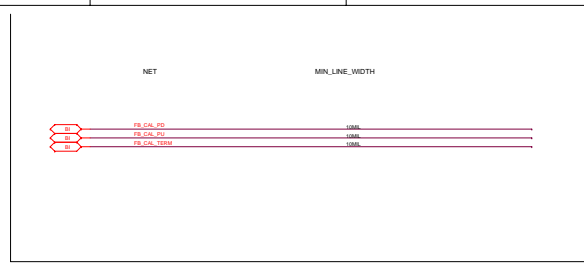
Return path coupling GND/FBVDDQ for FBA



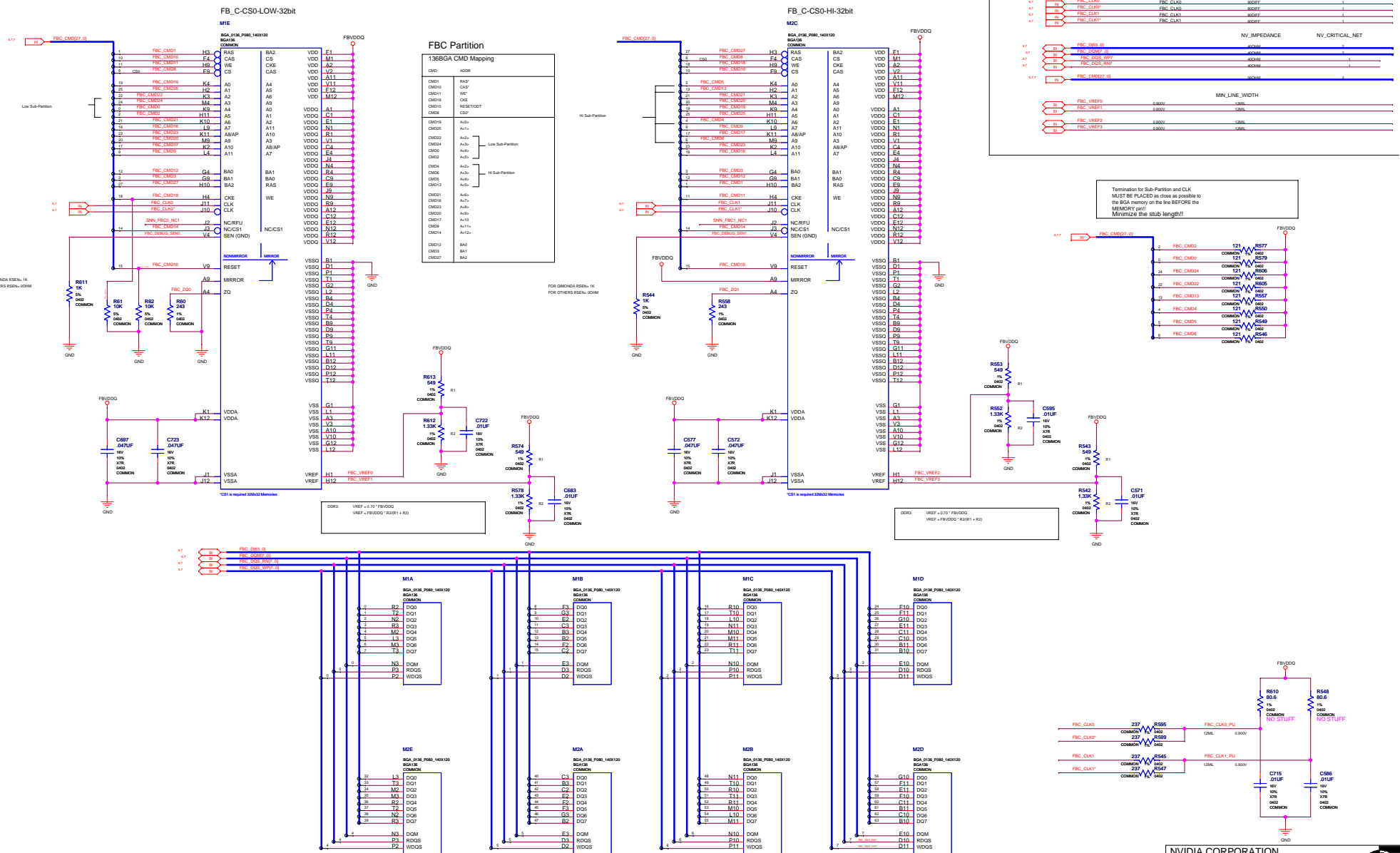
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ASSEMBLY	BASE LEVEL GENERIC BOM/MATN ONLY, COMMON & NO. 3100FF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBA MEMORY FBVDDQ DECOUPLING CAPS

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FRAMEBUFFER: PARTITION C 16/32Mx32 BGA136 GDDR3



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC 16/32MX32 GDDR3 MEMORIES, FBC CMD BUS P/U'S, FBC CLK TERMS

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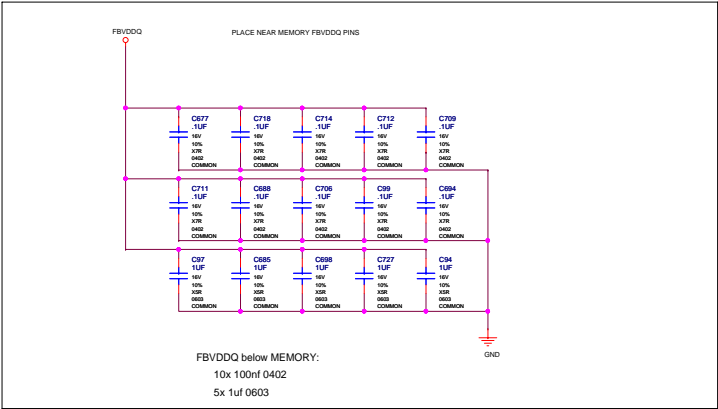


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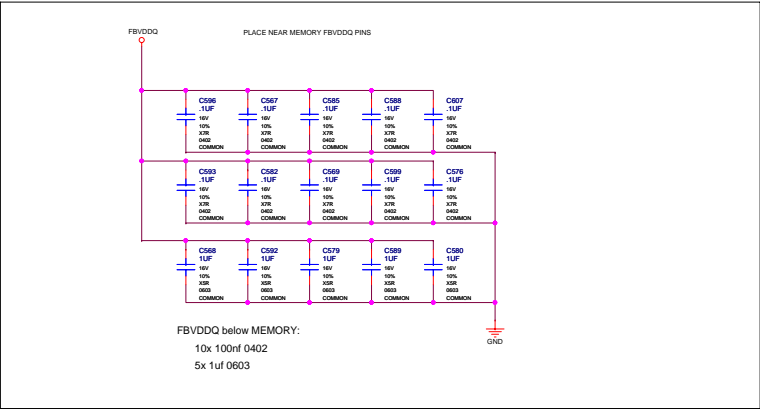
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FRAMEBUFFER: PARTITION C DECOUPLING

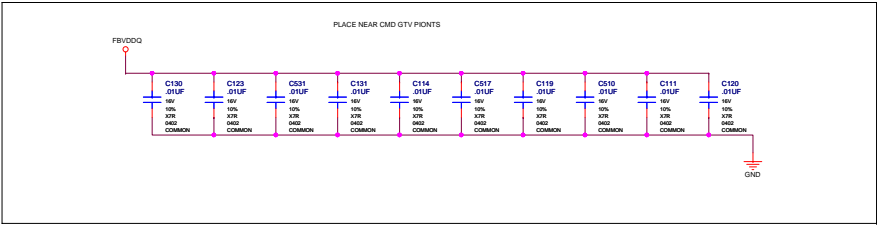
Decoupling for FBC 0..31



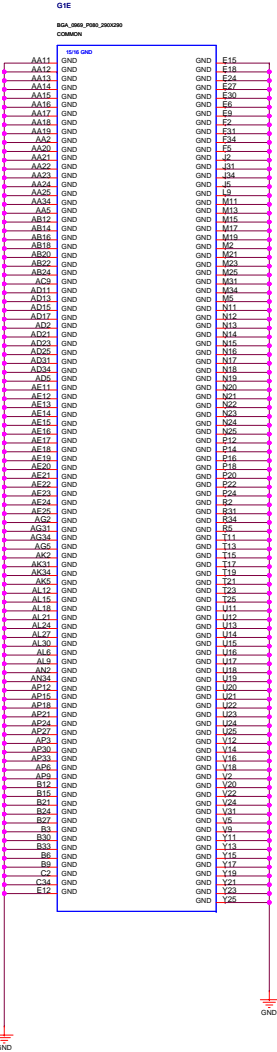
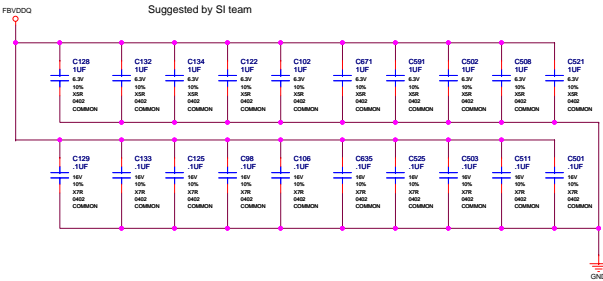
Decoupling for FBC 32..63



Return path coupling GND/FBVDDQ for FBC



Suggested by SI team



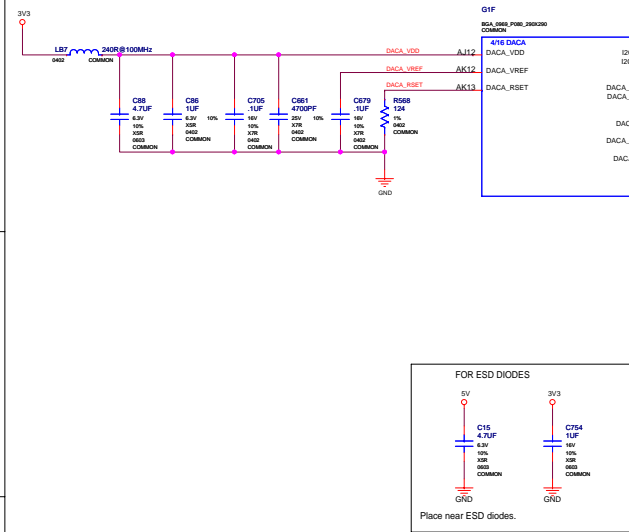
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ASSEMBLY	BASE LEVEL "GENERIC" BOARD ONLY. COMMON & NO. 3100P ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FBC MEMORY FBVDDQ DECOUPLING CAPS, GPU GND CONNECTIONS

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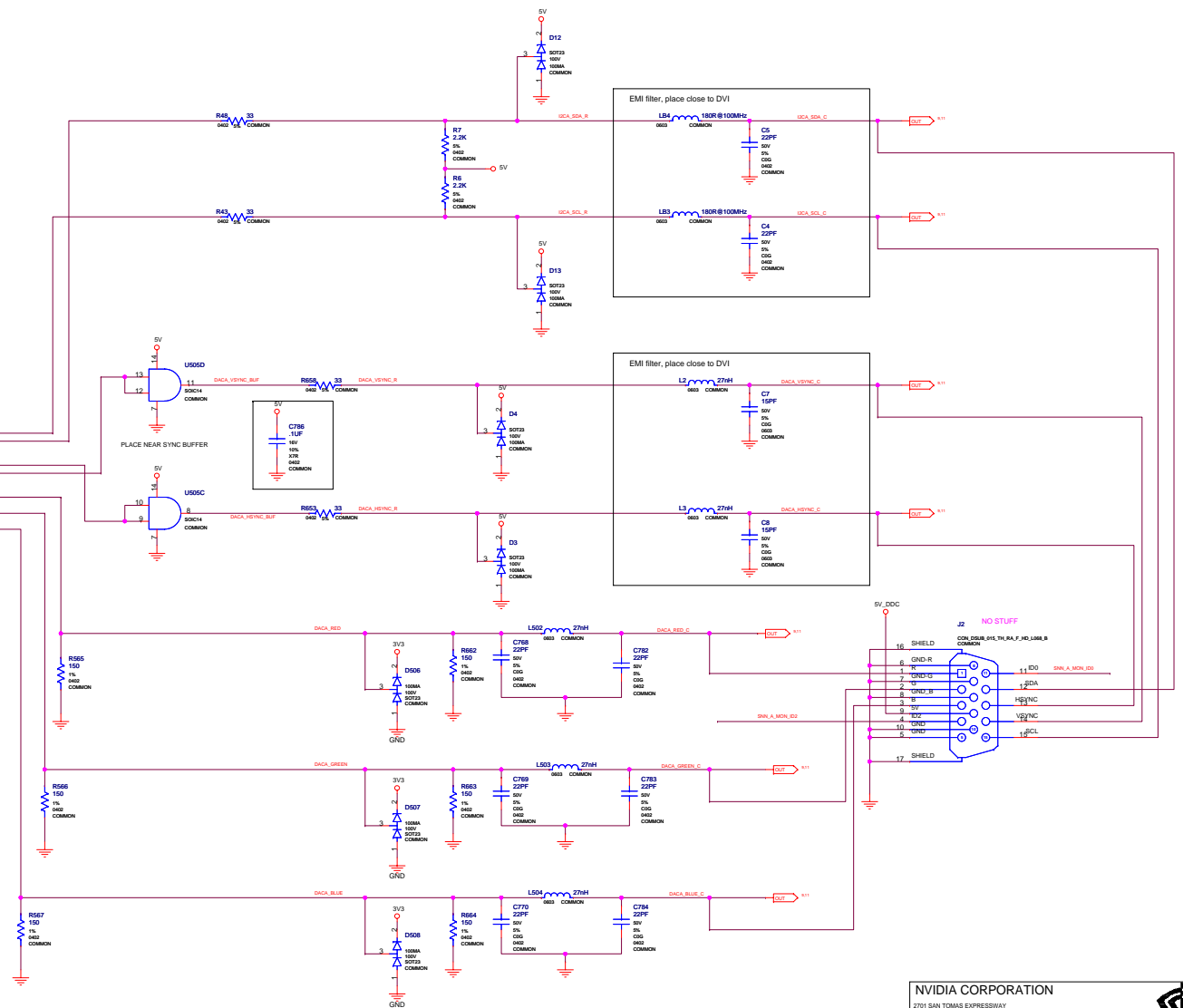


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R11	<b>B</b>	DACA_WB6	1	120V
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	<b>B</b>	DACA_WB121	1	120V
	<b>B</b>	DACA_WB122	1	120V
	<b>B</b>	DACA_WB123	1	120V
	<b>B</b>	DACA_WB124	1	120V
	<b>B</b>	DACA_WB125	1	120V
	<b>B</b>	DACA_WB126	1	120V
	<b>B</b>	DACA_WB127	1	120V
	<b>B</b>	DACA_WB128	1	120V
	<b>B</b>	DACA_WB129	1	120V
	<b>B</b>	DACA_WB130	1	120V
	<b>B</b>	DACA_WB131	1	120V
	<b>B</b>	DACA_WB132	1	120V
	<b>B</b>	DACA_WB133	1	120V
	<b>B</b>	DACA_WB134	1	120V
	<b>B</b>	DACA_WB135	1	120V
	<b>B</b>	DACA_WB136	1	120V
	<b>B</b>	DACA_WB137	1	120V
	<b>B</b>	DACA_WB138	1	120V
	<b>B</b>	DACA_WB139	1	120V
	<b>B</b>	DACA_WB140	1	120V
	<b>B</b>	DACA_WB141	1	120V
	<b>B</b>	DACA_WB142	1	120V
	<b>B</b>	DACA_WB143	1	120V
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	<b>B</b>	DACA_WB204	1	120V
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	<b>B</b>	DACA_WB206	1	120V
	<b>B</b>	DACA_WB207	1	120V
	<b>B</b>	DACA_WB208	1	120V
	<b>B</b>	DACA_WB209	1	120V
	<b>B</b>	DACA_WB210	1	120V
	<b>B</b>	DACA_WB211	1	120V
	<b>B</b>	DACA_WB212	1	120V
	<b>B</b>	DACA_WB213	1	120V
	<b>B</b>	DACA_WB214	1	120V
	<b>B</b>	DACA_WB215	1	120V
	<b>B</b>	DACA_WB216	1	120V
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	<b>B</b>	DACA_WB280	1	120V
	<b>B</b>	DACA_WB281	1	120V
	<b>B</b>	DACA_WB282	1	120V
	<b>B</b>	DACA_WB283	1	120V
	<b>B</b>	DACA_WB284	1	120V
	<b>B</b>	DACA_WB285	1	120V
	<b>B</b>	DACA_WB286	1	1



Primary Display (DACA), DVI-I

## DACA RGB-FILTER



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACA FILTERS, DACA SYNC BUFFERS & DB15 SOUTH

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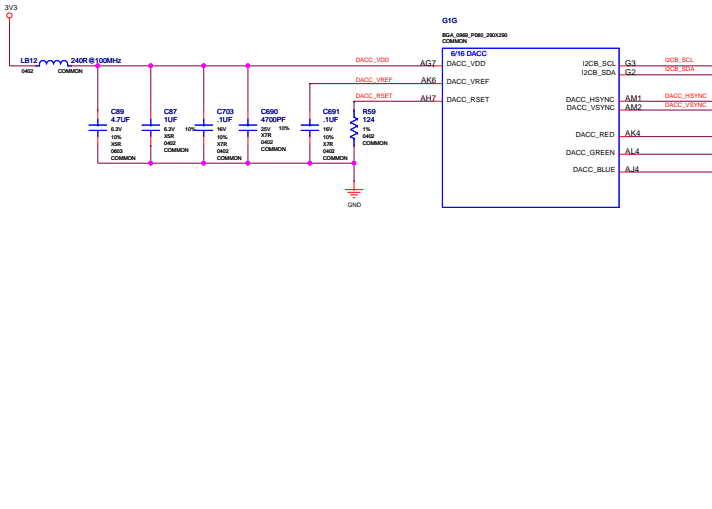


NV_PN	600-10977-base-100 A
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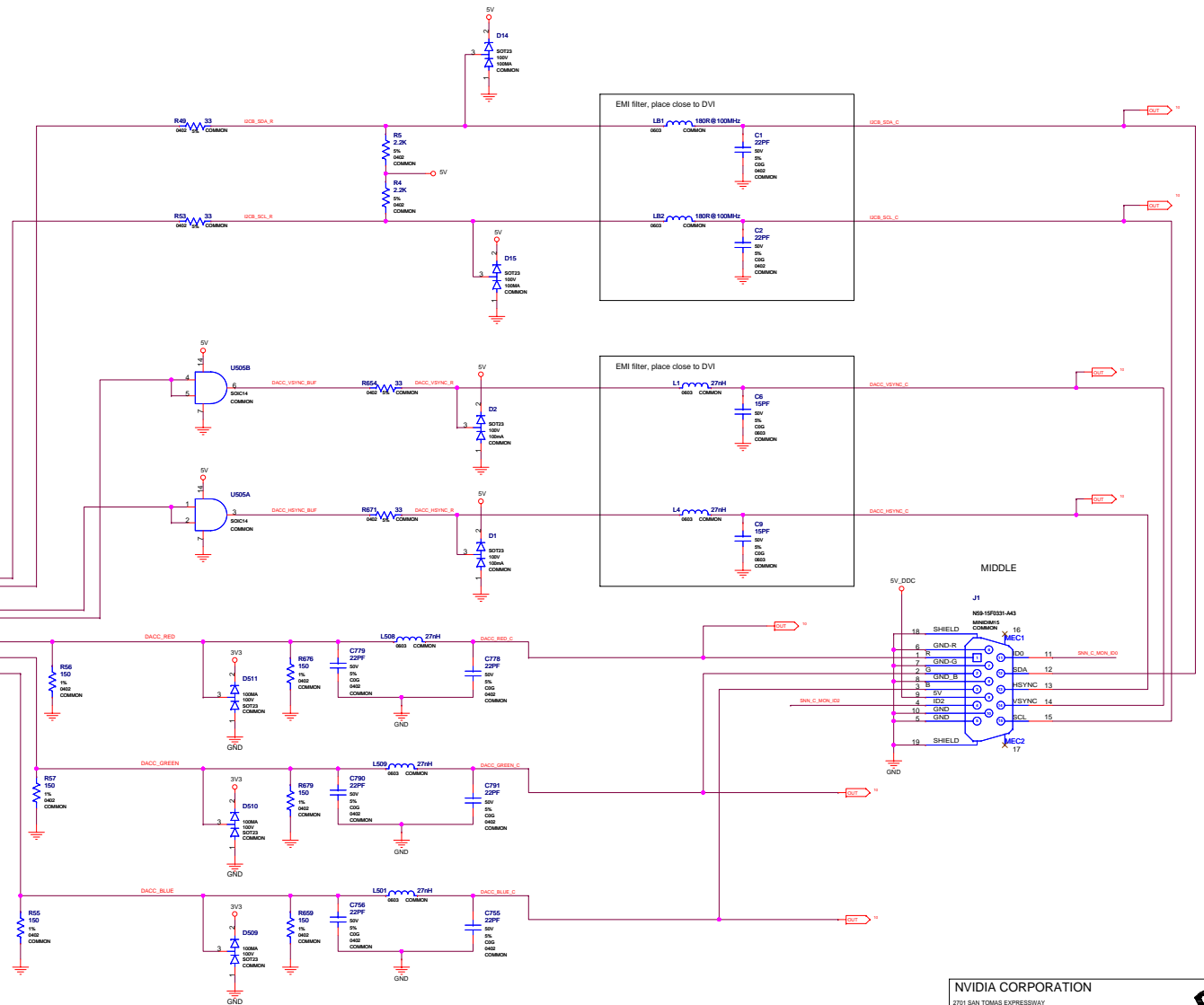
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NAME		DATE	02-APR-2008


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19	DACC_VREF	1	SDI0H
20	DACC_WDET	1	SDI0H
21	DACC_RED	1	SDI0H
22	DACC_GREEN	1	SDI0H
23	DACC_BLUE	1	SDI0H
24	DACC_RED_C	1	SDI0H
25	DACC_GREEN_C	1	SDI0H
26	DACC_BLUE_C	1	SDI0H
27	DACC_VSYNC	1	SDI0H
28	DACC_VSYNC_R	1	SDI0H
29	DACC_VSYNC_B	1	SDI0H
30	DACC_VSYNC_RBP	1	SDI0H
31	DACC_VSYNC_RBP	1	SDI0H
32	DACC_VSYNC_C	1	SDI0H
33	DACC_VSYNC_C	1	SDI0H
34	DSI0_B0H	2	SDI0H
35	DSI0_B0L	2	SDI0H
36	DSI0_B0H_C	2	SDI0H
37	DSI0_B0L_C	2	SDI0H
38	DSI0_B0H_R	2	SDI0H
39	DSI0_B0H_C	2	SDI0H
40	DSI0_B0L_C	2	SDI0H




## DACC RGB-FILTER



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<b>NV_PN</b> 600-10977-base-100 A			
<b>ID</b>		<b>PAGE</b>	
<b>NAME</b>		<b>DATE</b>	02-APR-2008

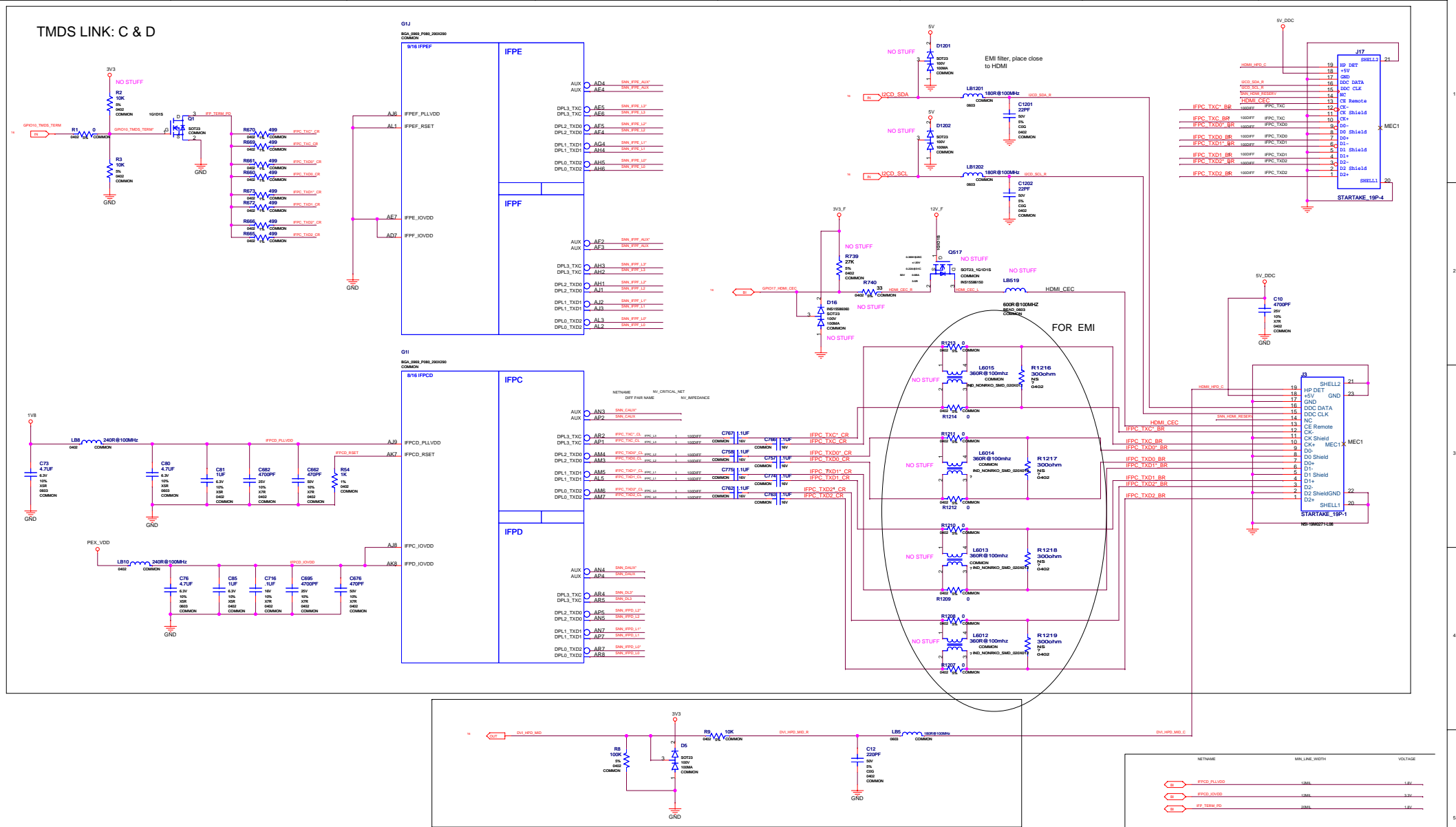
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The schematic shows the power supply section. It starts with a 5V input labeled "5V1". This input goes through a series resistor R10 (100Ω) to a junction. From this junction, one path goes down to ground through a 20mA fuse F1 (SOF23). The other path continues to the right, passing through a 10K resistor R11. After R11, there is another junction. One path from this junction goes down to ground through a capacitor C20 (220µF). The other path continues to the right, passing through an inductor L86 (100nH), and finally reaching the output node labeled "5V2".

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<b>ID</b>		<b>PAGE</b>	
<b>NAME</b>		<b>DATE</b>	02-APR-2008

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMDS LINK A/B, DVI CONNECTOR SOUTH

TMDS LINK: C & D



## Hotplug Detection

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	TMD5 LINK C/D, AC COUPLING, PD's, DVI CONNECTOR MID

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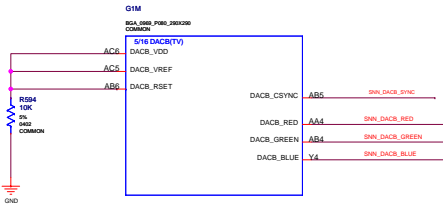
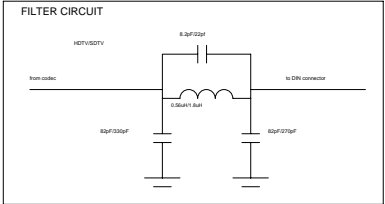
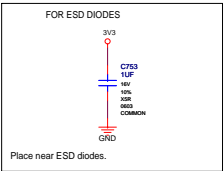
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NAME	DATE 02-APR-2008

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DACB: SD/HD VIDEO OUT CONNECTOR

NET_NAME	MIN_LINE_WIDTH	NV_IMPEDANCE	NV_CRITICAL_NET
OUT	DACB_C_OUT	50OHM	1
OUT	DACB_CVBS_OUT	50OHM	1
OUT	DACB_PB_OUT	50OHM	1
BI	TV_PROOF_C	50OHM	1
BI	TV_PROOF_E	50OHM	1
BI	TV_PROOF_E	50OHM	1
BI	DACB_VREF	100M	
BI	DACB_RSET	100M	



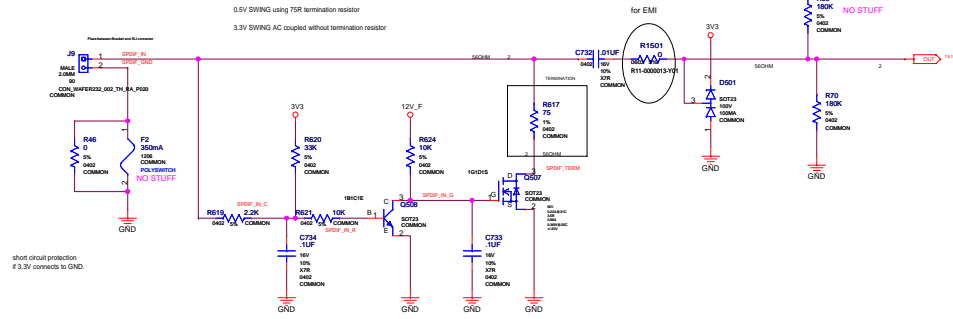
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ASSEMBLY	BASE LEVEL GENERIC BOARD/PCB ONLY; COMMON & NO. 31000 ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	DACB FILTER, MINIDIN CONNECTOR NORTH, SD/HD VIDEO OUTPUT CONNECTOR

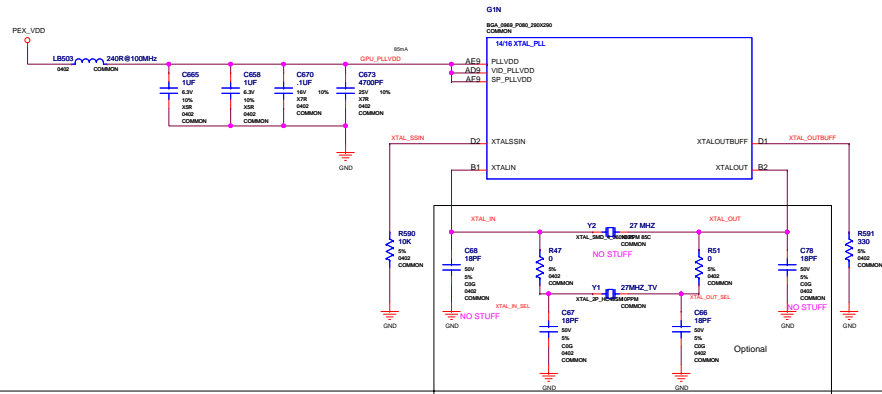
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NV_PN	600-10977-base-100 A		
ID		PAGE	
NAME		DATE	02-APR-2008

## XTAL/PLLVDD/SPDIF IN

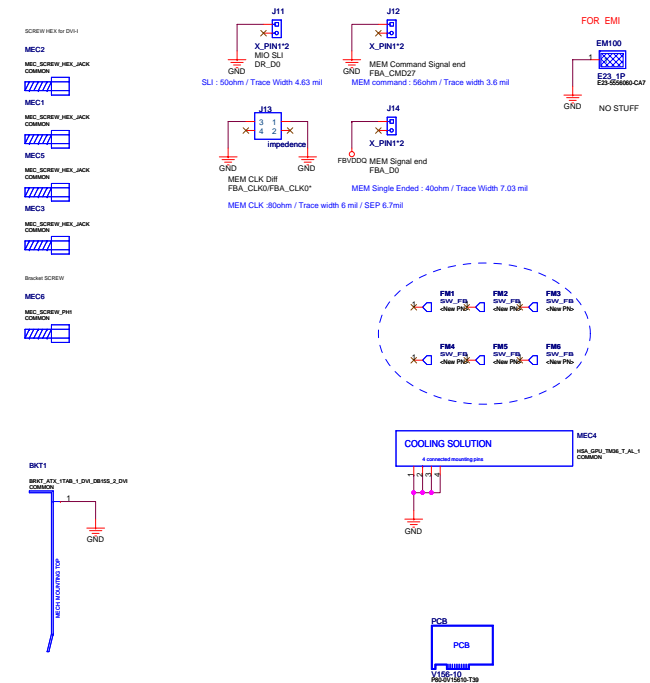
## SPDIF IN



## XTAL/GPU\_PLLVDD



## MECHANICALS &amp; THERMALS



Timing diagram for the NETNAME signal. The diagram shows a sequence of events: CPU\_PULSED (100ns, 2.2V), XTAL\_IN (100ns), XTAL\_OUT (100ns), XTAL\_EEN (100ns), XTAL\_OUTBUFF (100ns), SIOF\_IN (500ns, 2V), SIOF\_OUP (500ns, 2V), and SIOF\_GND (100ns, 2V). The signal transitions between high and low states at various points, with the high state being at 2.2V and the low state being at 0V.

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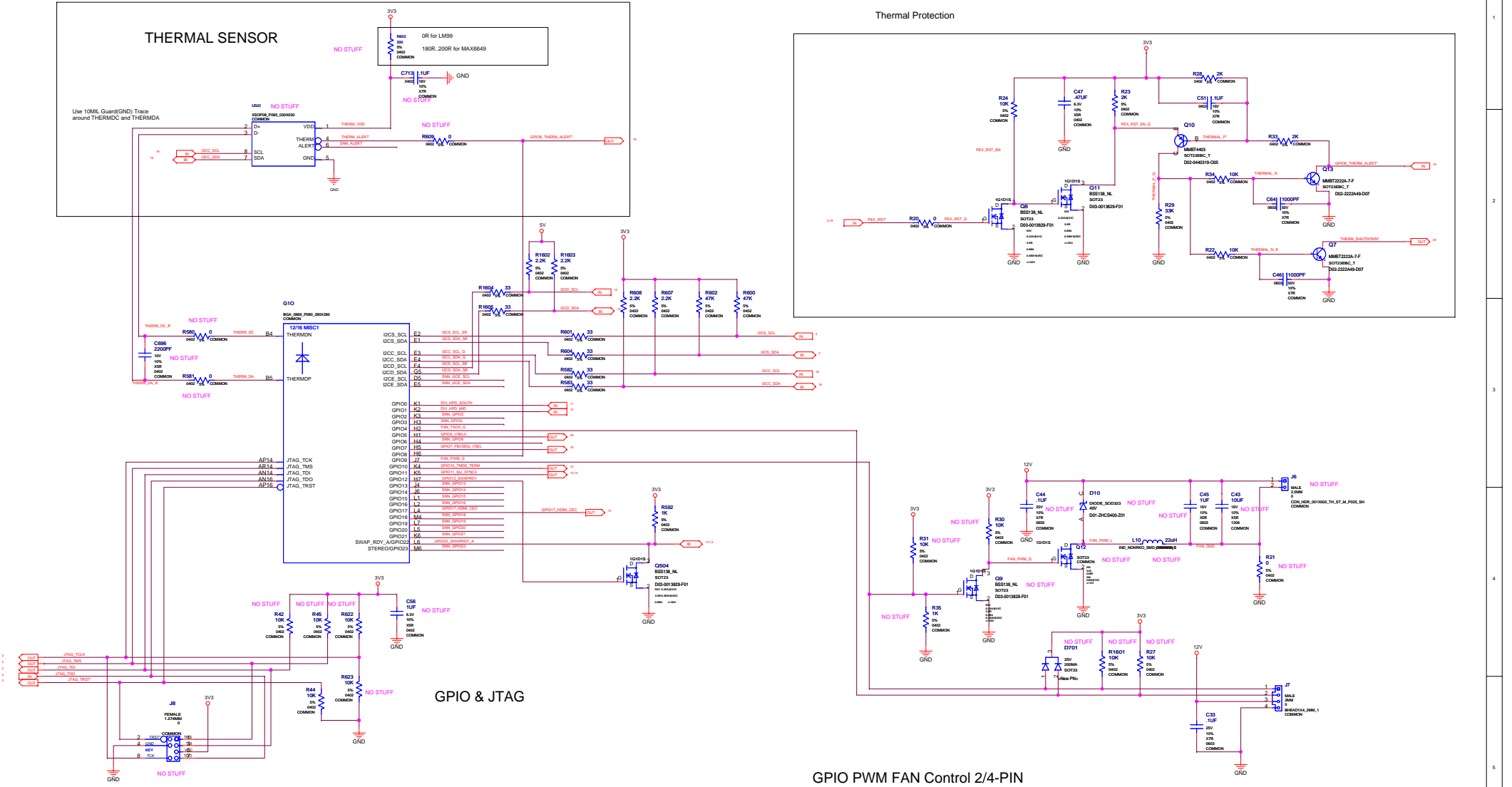
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	SPDF-IN, XTAL, MECHANICALS, THERMALS

EXTERNAL THERMAL SENSOR, 4PIN FAN CONTROL, GPIO, THERMAL PROTECTION



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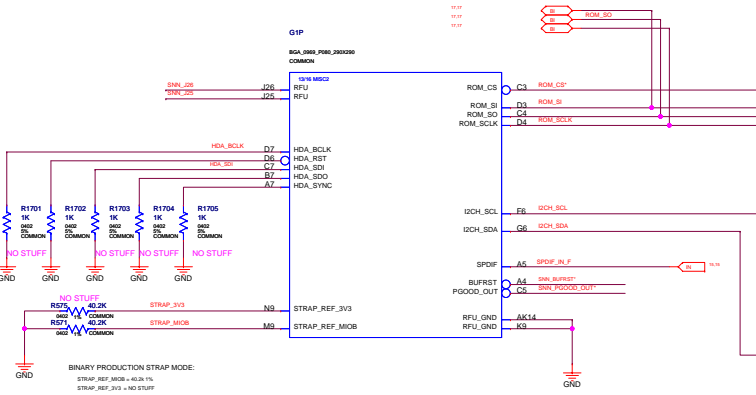
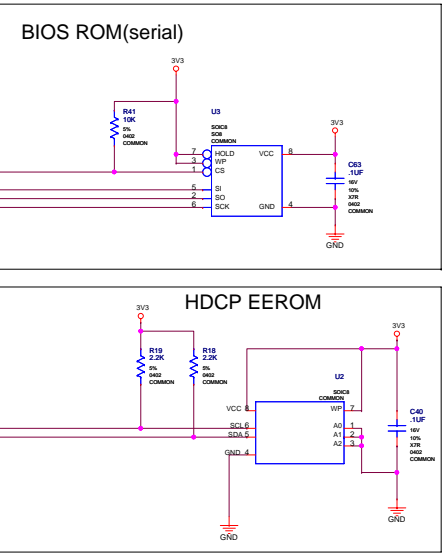
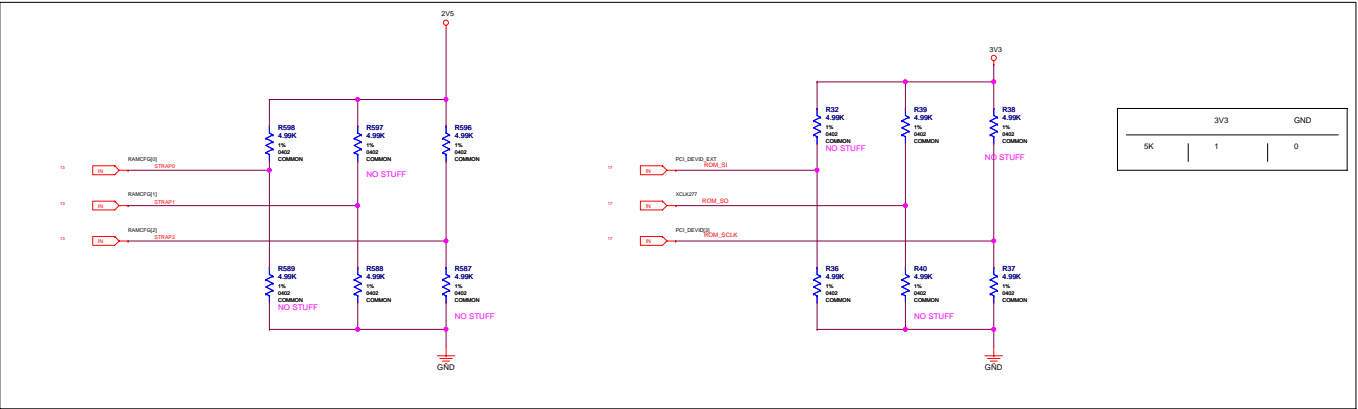
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO. 3V3/5V ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	EXTERNAL THERMAL SENSOR, 4PIN FAN CONTROL, GPIO, THERMAL PROTECTION

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STRAPPING OPTIONS

Assembly: BIOS



NET_NAME	MIN_LINE_WIDTH	IV_IMPEDANCE	IV_CRITICAL_NET
HDA_BCLK	100um	100um	1
HDA_RST	100um	100um	1
HDA_SDI	100um	100um	1
HDA_SDO	100um	100um	1
HDA_SYNC	100um	100um	1
HDA_SDI_R	100um	100um	1

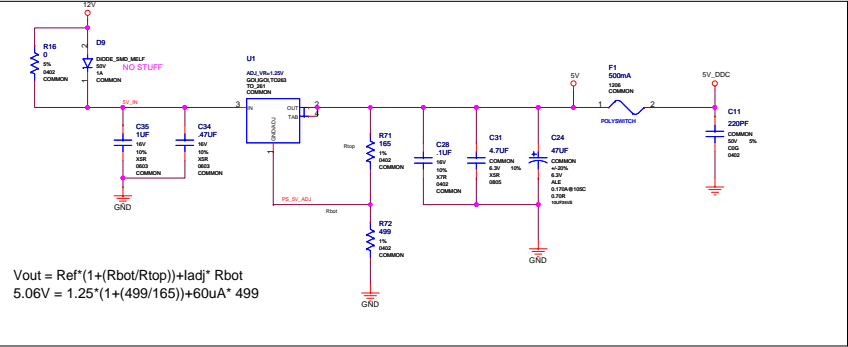
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ASSEMBLY	BIOS ROM, HDCP ROM, STRAPPING OPTIONS
PAGE DETAIL	BIOS ROM, HDCP ROM, STRAPPING OPTIONS

NVIDIA CORPORATION	
3701 SAN TOMAS EXPRESSWAY	
SANTA CLARA, CA 95050, USA	
NV_PN	600-10977-base-100 A
ID	PAGE
NAME	DATE 02-APR-2008

Power Supply: 5V, 5V\_DDC, IFP\_PLLVDD, MIOA\_VDD, TMDS BACKDRIVE

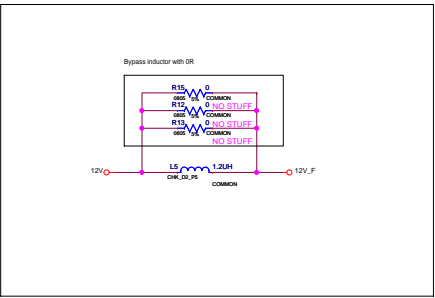
5V REGULATOR



$V_{out} = V_{ref} * (1 + (R_{bot}/R_{top})) + I_{adj} * R_{bot}$   
 $5.06V = 1.25 * (1 + (499/165)) + 60\mu A * 499$

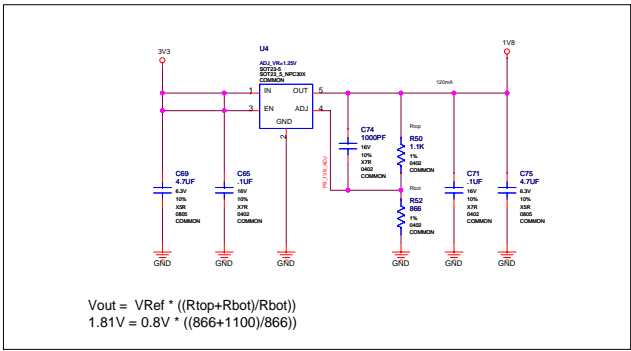
5V DDC

12V filter



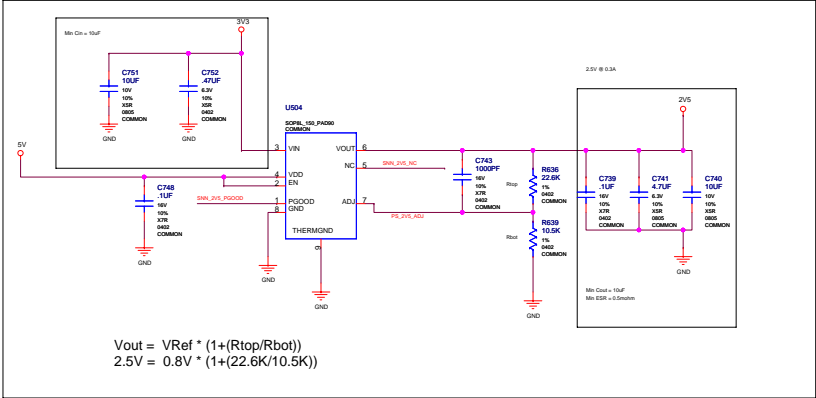
NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
5V_DDC	0.1A	12MIL	5V
5V	0.1A	12MIL	5V
1V8	0.12A	12MIL	1.8V
2V5	0.3A	12MIL	2.5V
GND		10MIL	0
12V_F	8A	20MIL	12V

IFP PLL Supply 1.8V



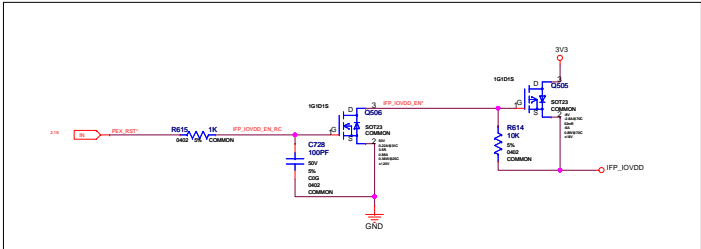
$V_{out} = V_{ref} * ((R_{top} + R_{bot}) / R_{bot})$   
 $1.81V = 0.8V * ((866 + 1100) / 866)$

MIO\_VDD 2.5V



$V_{out} = V_{ref} * (1 + (R_{top}/R_{bot}))$   
 $2.5V = 0.8V * (1 + (22.6K/10.5K))$

TMDS BACKDRIVE



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COORDINATE NO. 31000 ASSEMBLY NOTES AND BOM NOT FINAL.
PAGE DETAIL	5V_DDC/5V_IFP_PLLVDD/MIO_VDD_TMDS_BACKDRIVE

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SANTA CLARA, CA 95050, USA			
NV_PN	600-10977-base-100 A	PAGE	
ID		DATE	02-APR-2008
NAME			

POWER SUPPLY: FBVDD/Q,PEX\_VDD


NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
FBVDDQ	10A	20MIL	1.8V
PEX_VDD	3A	18MIL	1.1V

PEXVDD Power Supply  
PEXVDD = 1.1V @ 3A

FBVDDQ Power Supply  
FBVDDQ = 1.8 - 2.0 V@ 10A

GPIO7	
FBVDDQ = 1.816V	0
FBVDDQ = 1.997V	1

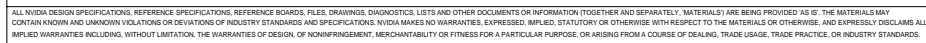
NVIDIA CORPORATION  
3701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA




NV_PN	600-10977-base-100 A		
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NAME		DATE	02-APR-2008

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## UP6205 3\*3 Modulize circuit ver:1



<b>NVIDIA CORPORATION</b> 7701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
INV_PN 600-10977-base-100 A			
D		PAGE	
NAME <ENGINEER>		DATE	02-APR-2008

A		B		C		D		E		F		G		H	
Title: Cref Part		C89 (10.44)		C551 (4.30)		C547 (16.10)		J9 (16.24)		R15 (16.20)		R543 (7.30)		R539 (16.37)	
Report: C90 (2.10)		C552 (4.30)		C554 (4.30)		C548 (2.10)		J10 (16.24)		R16 (16.24)		R544 (20.30)		R540 (20.30)	
Design: 1077_A00		C91 (11.38)		C555 (4.30)		C549 (20.40)		L1 (16.30)		R17 (20.30)		R545 (7.50)		R541 (20.30)	
Date: Jan 16		C92 (2.10)		C556 (19.30)		C550 (20.30)		L2 (6.30)		R18 (17.40)		R546 (7.20)		R542 (20.40)	
15.00.01.2008		C93 (2.10)		C557 (19.30)		C551 (20.30)		L3 (9.30)		R19 (17.40)		R547 (7.50)		R543 (20.40)	
BKT1 (15.30)		C94 (8.20)		C558 (19.30)		C552 (2.30)		L4 (16.30)		R20 (16.30)		R548 (7.40)		R544 (20.10)	
C1 (10.30)		C95 (2.10)		C559 (19.30)		C553 (20.30)		L5 (16.30)		R21 (16.40)		R549 (7.20)		R545 (20.40)	
C2 (10.30)		C96 (8.40)		C560 (19.30)		C554 (20.40)		L6 (20.30)		R22 (16.20)		R550 (7.20)		R546 (20.30)	
C3 (11.20)		C97 (8.20)		C561 (19.30)		C555 (2.30)		L7 (20.30)		R23 (16.10)		R551 (2.50)		R547 (20.40)	
C4 (8.20)		C98 (8.40)		C562 (19.30)		C556 (2.30)		L8 (20.30)		R24 (16.30)		R552 (7.30)		R548 (20.20)	
								L9 (20.10)		R25 (16.10)		R553 (7.30)		R549 (20.40)	
								L10 (16.40)		R26 (2.10)		R554 (3.40)		R550 (20.40)	
								L11 (19.30)		R27 (16.40)		R555 (3.40)		R551 (20.40)	
								L12 (19.30)		R28 (16.10)		R556 (8.50)		R552 (20.40)	
								L13 (19.30)		R29 (16.20)		R557 (7.20)		R553 (20.30)	
								L14 (19.30)		R30 (16.40)		R558 (7.20)		R554 (16.30)	
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								L20 (14.40)		R36 (17.20)		R564 (2.30)		R560 (12.10)	
								L21 (16.40)		R37 (17.20)		R565 (4.50)		R561 (12.10)	
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								L23 (16.30)		R39 (17.10)		R567 (8.50)		R563 (9.40)	
								L24 (9.20)		R40 (17.20)		R568 (3.30)		R564 (9.50)	
								L25 (12.20)		R41 (16.40)		R569 (13.40)		R565 (12.20)	
								L26 (11.30)		R42 (16.40)		R570 (11.30)		R566 (12.20)	
								L27 (14.40)		R43 (9.20)		R571 (17.40)		R567 (12.20)	
								L28 (11.30)		R44 (16.50)		R572 (13.30)		R568 (12.20)	
								L29 (12.40)		R45 (16.50)		R573 (13.40)		R569 (12.10)	
								L30 (11.30)		R46 (16.50)		R574 (7.30)		R570 (12.10)	
								L31 (14.40)		R47 (15.50)		R575 (17.40)		R571 (10.30)	
								L32 (12.40)		R48 (9.20)		R576 (13.40)		R572 (12.20)	
								L33 (11.30)		R49 (16.40)		R577 (13.40)		R573 (12.20)	
								L34 (10.30)		R50 (16.30)		R578 (7.30)		R574 (12.20)	
								L35 (10.40)		R51 (15.50)		R579 (7.20)		R575 (12.20)	
								L36 (10.40)		R52 (16.30)		R580 (16.30)		R576 (10.40)	
								L37 (10.40)		R53 (16.20)		R581 (16.30)		R577 (12.20)	
								L38 (10.40)		R54 (16.20)		R582 (16.30)		R578 (12.20)	
								L39 (10.40)		R55 (15.50)		R583 (16.30)		R579 (10.40)	
								L40 (10.40)		R56 (14.40)		R584 (14.40)		L1 (16.20)	
								L41 (10.40)		R57 (16.40)		R585 (14.40)		L2 (17.40)	
								L42 (10.40)		R58 (16.40)		R586 (14.40)		L3 (17.30)	
								L43 (10.40)		R59 (16.40)		R587 (17.20)		L4 (16.30)	
								L44 (10.40)		R60 (17.20)		R588 (17.20)		L501 (19.20)	
								L45 (10.40)		R61 (17.20)		R589 (17.20)		L502 (16.20)	
								L46 (10.40)		R62 (17.20)		R590 (15.50)		L503 (20.20)	
								L47 (10.40)		R63 (19.30)		R591 (15.50)		L504 (16.30)	
								L48 (10.40)		R64 (19.20)		R592 (16.40)		L505 (9.30 9.30)	
								L49 (10.40)		R65 (14.20)		R593 (13.40)		Y1 (15.50)	
								L50 (10.40)		R66 (14.20)		R594 (14.40)		Y2 (16.50)	
								L51 (10.40)		R67 (14.20)		R595 (7.50)			
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								L53 (10.40)		R69 (16.40)		R597 (19.40)			
								L54 (10.40)		R70 (16.40)		R598 (17.10)			
								L55 (10.40)		R71 (16.40)		R599 (17.50)			
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