1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K94 CHOPIN MLB

PVT

REV. A

LAST_MODIFIED=Mon Jan 10 13:11:06 2011

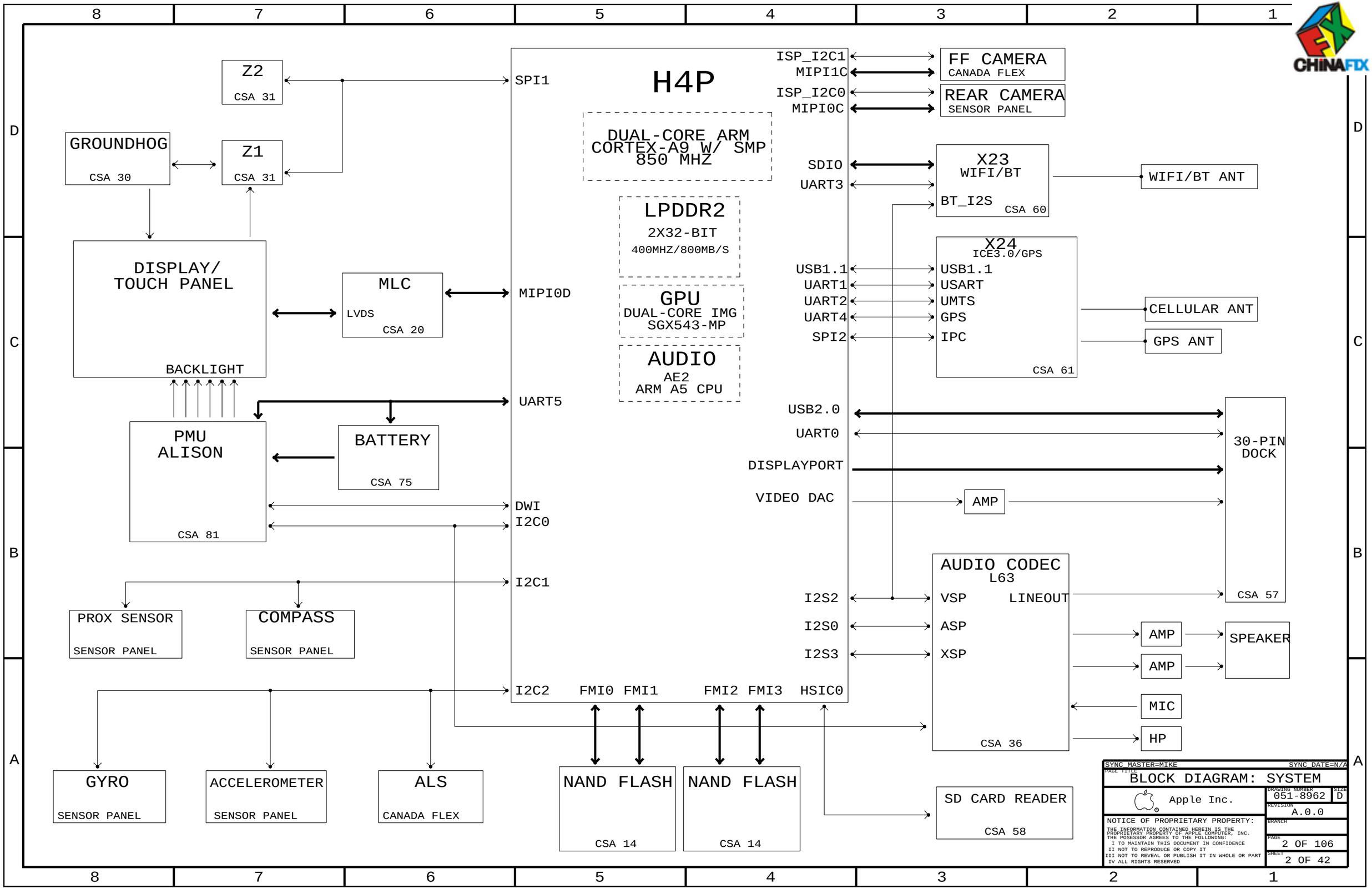
REV	ECN	DESCRIPTION OF REVISION
A	0001052699	PRODUCTION RELEASED

DRAWING
TITLE=BACH
ABBREV=DRAWING

DRAWING TITLE: CHOPIN MLB

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 106
SHEET: 1 OF 42



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE

BLOCK DIAGRAM: SYSTEM

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

PAGE 2 OF 106

SHEET 2 OF 42

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD
32GB_PROD
64GB_PROD

BKLT_PLL

DEVELOPMENT_JTAG
DEVELOPMENT_JTAG_TAP
JTAG_VAR
JTAG_TAP_NOT

SPEAKER
INTERNAL_MIC

PORTRAIT_DOCK

MLC_DEV
MLC_PROD

K93
K94

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE

ADD DEVELOPMENT AND OTHER BOMS ONCE YOU GET BOM NUMBERS

BOM OPTIONS

PROGRAMMABLE PARTS

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-8962	1	SCH,CHOPIN_AUDIO,MLB,K94	SCH1	
820-3069	1	PCBF,CHOPIN_AUDIO,MLB,K94	PCB1	

PD PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-1396	1	FENCE,GRAPE,MLB,K93/K94	FENCE1	
806-1397	1	CAN,GRAPE,MLB,K93/K94	CAN1	NOSTUFF
806-1398	1	FENCE,CPU,MLB,K93/K94	FENCE2	
806-1399	1	CAN,CPU,MLB,K93/K94	CAN2	NOSTUFF
806-1400	1	FENCE,NAND,MLB,K93/K94	FENCE3	
806-1401	1	CAN,NAND,MLB,K93/K94	CAN3	NOSTUFF

TOP BARCODE LABEL/EEE CODES (ONLY ONE IS USED PER BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7651	1	EEEE FOR 639-1180 (K93 16G)	DH36	CRITICAL	EEEE_K93_16G
825-7651	1	EEEE FOR 639-1426 (K93 32G)	DH37	CRITICAL	EEEE_K93_32G
825-7651	1	EEEE FOR 639-1428 (K93 64G)	DG99	CRITICAL	EEEE_K93_64G
825-7651	1	EEEE FOR 639-1112 (K94 16G)	DFC4	CRITICAL	EEEE_K94_16G
825-7651	1	EEEE FOR 639-1181 (K94 32G)	DFC5	CRITICAL	EEEE_K94_32G
825-7651	1	EEEE FOR 639-1182 (K94 64G)	DFC6	CRITICAL	EEEE_K94_64G
825-7651	1	EEEE FOR 639-1430 (K95 16G)	DH3C	CRITICAL	EEEE_K95_16G
825-7651	1	EEEE FOR 639-1427 (K95 32G)	DH3D	CRITICAL	EEEE_K95_32G
825-7651	1	EEEE FOR 639-1429 (K95 64G)	DG9C	CRITICAL	EEEE_K95_64G

BOTTOM LABEL TYPE 1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	631- B/C LABEL	LBL1	CRITICAL	
825-7639	1	639- B/C LABEL	LBL2	CRITICAL	

BOTTOM LABEL TYPE 2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7640	1	MATRIX LABEL	LBL3	CRITICAL	
825-7640	1	631- MATRIX LABEL	LBL4	CRITICAL	

SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE: BOM TABLE

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 5 OF 106
SHEET: 3 OF 42

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

NEED TO ADD BOM TABLE FOR ALT P/N OF HYNIX (?)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION

U0652
H4P-512MB
BGA
SYM 11 OF 12
SC58940X01-A030

AU14 AU15 AU16 AU17 AV1 AV2 AV3 AV4 AV5 AV6 AV7 AV8 AV9 AV10 AV11 AV12 AV13 AV14 AV15 AV16 AV17 AV29 AV33 AV34 AW1 AW2 AW4 AW23 AW33 AW34 AY1 AY2 AY3 AY4 AY20 AY22 AY24 AY30 AY31 AY32 AY33 AY34 B1 B2 B7 B9 B10 B12 B13 B15 B17 B18 B20 B22 B23 B28 B29 B30 B32 B33 B34 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C23 C27 C29 C32 C33 D1 D3 D5 D7 D9 D11 D13 D15 D16 D23 — VSS

D27 D32 E1 E2 E3 E4 E6 E8 E10 E12 E14 E16 E17 E18 E19 E20 E21 E22 E23 E25 E26 E27 E28 E30 E31 E32 E34 F1 F2 F3 F5 F19 F20 F21 F22 F23 F25 F26 F29 F30 F31 F32 G1 G3 G4 G7 G8 G9 G10 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G25 G28 G29 G30 H1 H2 H3 H5 H7 H8 H10 H12 H14 H16 H18 H20 H22 H24 H25 H29 H30 J1 J2 J3 J4 J7 J9 J11 J13 J15 J17 J19 — VSS

=PP1V1_PLL_H4 (32)

R0620 0.00 — C0651 0.01UF — PP1V1_PLL4_F
R0621 0.00 — C0648 0.01UF — PP1V1_PLL3_F
R0622 0.00 — C0646 0.01UF — PP1V1_PLL2_F
R0623 0.00 — C0644 0.01UF — PP1V1_PLL1_F
R0624 0.00 — C0608 0.01UF + C0660 56PF — PP1V1_PLL0_F

0% 1/32W MF 01005; 10% 6.3V X5R 01005; 5% 6.3V NP0-C0G 01005

VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

=PP1V1_USB_H4 (32 4) — C0643 0.22UF 20% 6.3V X5R 0201

=PP1V2_HSIC_H4 (32) — C0642 0.01UF + C0641 0.01UF

JTAGSEL
0 - PARALLEL
1 - DAISY-CHAIN (FOR USE WITH 5-WIRE JTAG)
PER RADAR #6755237

TP_HSIC1_AP_DATA	A26	HSIC1_DATA
TP_HSIC1_AP_STB	A27	HSIC1_STB
NC_HSIC2_AP_DATA	C26	HSIC2_DATA
NC_HSIC2_AP_STB	D26	HSIC2_STB
AP_JTAG_SEL	N31	JTAG_SEL
NC_JTAG_AP_RTCK	M30	JTAG_TRTCK
JTAG_AP_TRST_L	N29	JTAG_TRST*
JTAG_AP_TDO	M31	JTAG_TDO
JTAG_AP_TDI	M32	JTAG_TDI
JTAG_AP_TMS	N32	JTAG_TMS
JTAG_AP_TCK	N30	JTAG_TCK
AP_TESTMODE	P29	TESTMODE
	M28	FUSE1_FSRC
AP_TST_STPCLK	P33	TST_STPCLK
TP_AP_TST_CLKOUT	P34	TST_CLKOUT
AP_FAST_SCAN_CLK	T32	FAST_SCAN_CLK (FOR IC TESTER)
AP_HOLD_RESET	P31	HOLD_RESET (0=NORMAL)
RST_AP_1V8_L	P32	RESET*
AP_CFSB	W30	CFSB
	G11	DDR0_CKEIN
AP_DDR1_CKEIN_1V2	R7	DDR1_CKEIN

SYM 1 OF 12
U0652
H4P-512MB
BGA

HSIC_VDD121 D25; HSIC_VDD122 D24; HSIC_DVDD F24; PLL0_AVDD11 C19; PLL1_AVDD11 C20; PLL2_AVDD11 C21; PLL3_AVDD11 C15; PLL4_AVDD11 C17; PLL_USB_AVDD11 C23; MIPI0D_VDD11_PLL AK30; MIPI1D_VDD11_PLL AT34; USB_DVDD C28; H27; USB_VDD330 M25

HSIC_VSS121 C25; HSIC_VSS122 C24; HSIC_DVSS E24; PLL0_AVSS11 D19; PLL1_AVSS11 D20; PLL2_AVSS11 D21; PLL3_AVSS11 D16; PLL4_AVSS11 D17; PLL_USB_AVSS11 D22; MIPI_VSS_0 AN10; MIPI_VSS_1 AN11; USB_DVSS D28; USB_VSSA0 H26; USB_VSSAC J26

WDOG P30 — RST_PMU_IN (OUT) 35

XI0 A18 — 39 XTAL_24M_I
XO0 A19 — 39 XTAL_24M_O

R0655 1.00M 1% MF 01051/32W
R0640 22 5% 1/32W MF 01005
CRITICAL Y0602 SM-2 24.000MHZ-16PF-60PPM
39 24M_O — C0613 22PF 5% 16V CERM 01005
C0607 22PF 5% 16V CERM 01005

USB11_DP A22 — USB_FS_D_P (BI) 11 39
USB11_DM A23 — USB_FS_D_N (BI) 11 39
USB_DP A29 — USB_D_P (BI) 28 39
USB_DM A28 — USB_D_N (BI) 28 39

USB_ANALOGTEST G26 — NC_USB_ANALOGTEST
USB_VBUS F27 — USB_AP_VBUS — R0651 100K 5% 1/32W MF 01005 — PPVBUS_USB 34
USB_ID F28 — NC_USB_ID
USB_BRICKID G27 — USB_BRICKID (OUT) 35
USB_REXT A21 — USB_REXT — R0642 44.2 1% 1/20W MF 201

DZ0600 GDZT2R5.1B GO2-0201

NOTE: PAGE 4608 H4P UM V0.83

PP1V1_PLL_USB_F — C0652 0.01UF — R0625 0.00 — =PP1V1_USB_H4 (4 32)

VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

PP1V1_MIPID_PLL_F — C0661 56PF 5% 6.3V NP0-C0G 01005; C0654 0.1UF 10% 6.3V X5R 201; C0655 1UF 10% 6.3V CERM 402 — FL0610 80-OHM-0.2A-0.4-OHM 0201-1 — =PP1V1_MIPI_PLL_H4 (32)

=PP1V1_USB_H4 (4 32) — C0627 0.01UF

=PP3V3_USB_H4 (4 32) — C0640 1UF + C0630 0.01UF

10% 6.3V X5R 01005; 10% 6.3V CERM 402

=PP3V3_USB_H4 (32 4) — R0617 10K 1% 1/32W MF 01005 — R0632 100K 5% 1/32W MF 01005 — 35 31 28 (IN) RST_AP_L

NOSTUFF XW0604 SHORT-01005

R0688 42.2K 1% MF 01005 — C0618 1000PF 10% 16V X7R 201

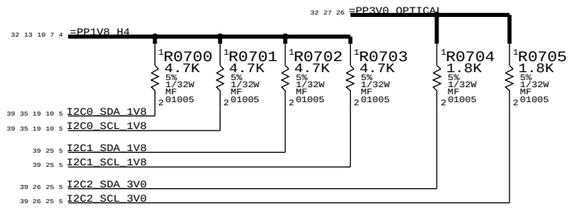
NOSTUFF XW0605 SHORT-01005 — AP_DDR1_CKEIN

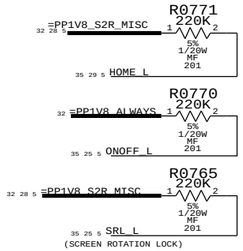
R0689 82.5K 1% 1/32W MF 01005

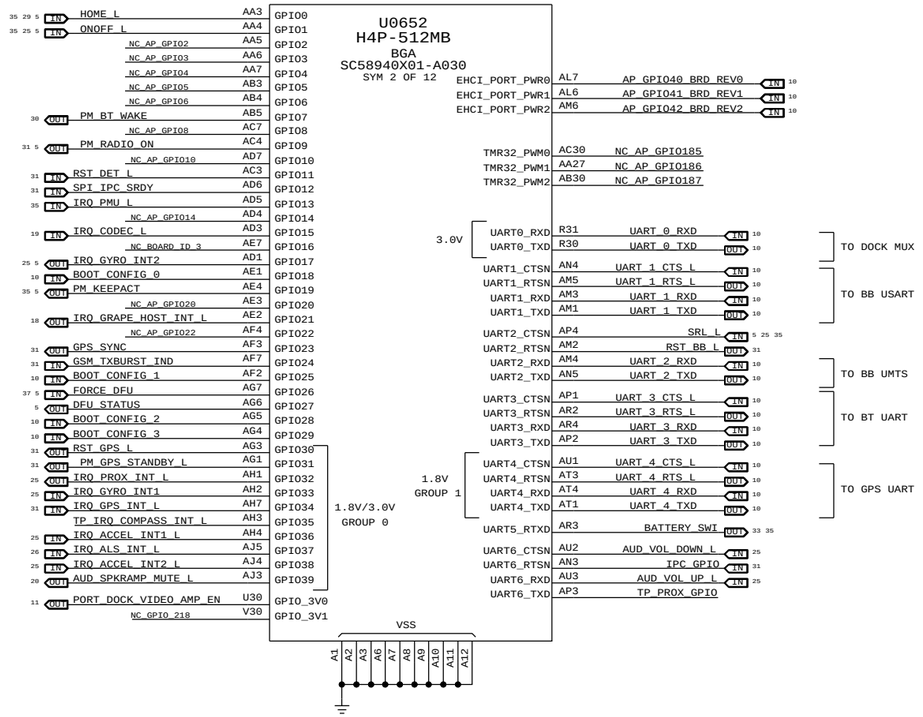
=PP1V8_H4 (32 13 10 7 5 4) — R0645 100K — JTAG_AP_TCK 4 28 39; R0646 100K — JTAG_AP_TMS 4 28 39; R0647 100K — JTAG_AP_TDI 4 10 39

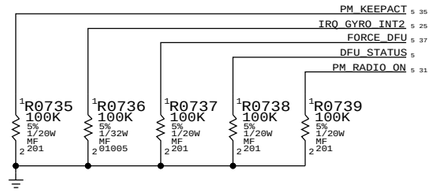
DEVELOPMENT_JTAG_TAP — R0662 100K

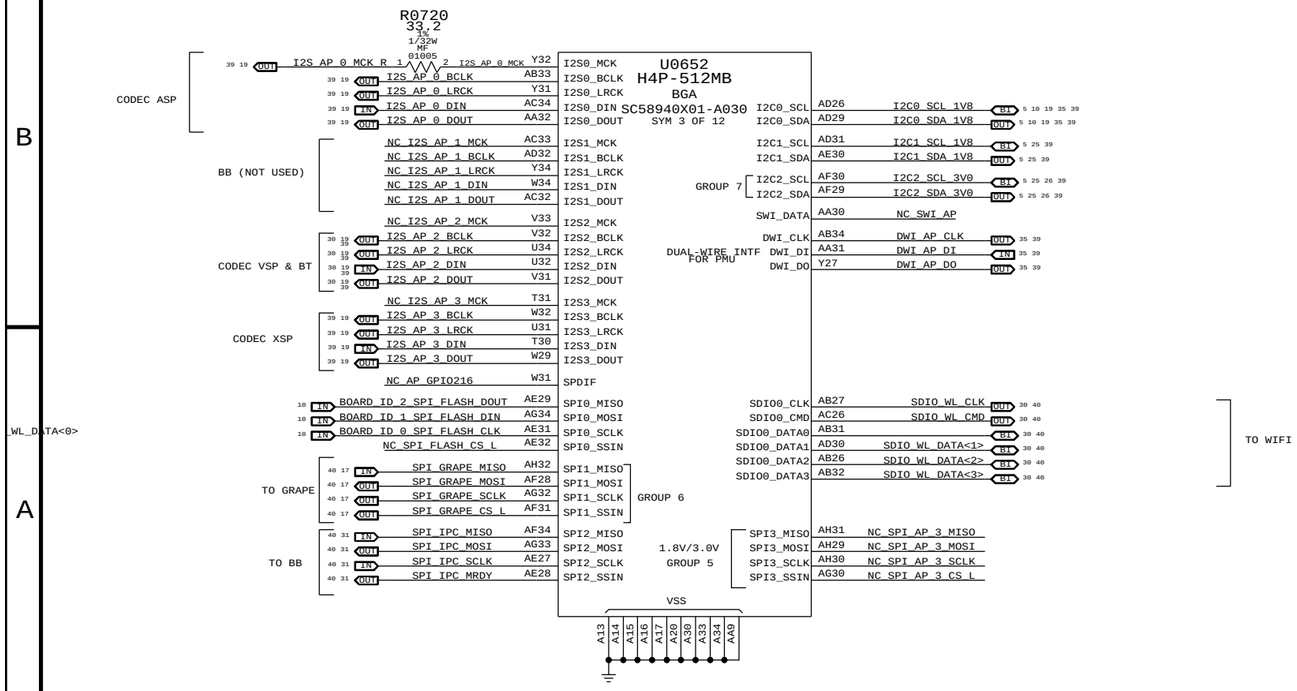
SYNC_MASTER=JAMES	SYNC_DATE=N/A
PAGE TITLE: AP: MAIN	
Apple Inc.	DRAWING NUMBER 051-8962 · SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 6 OF 106
	SHEET 4 OF 42











SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE: AP: I/Os

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

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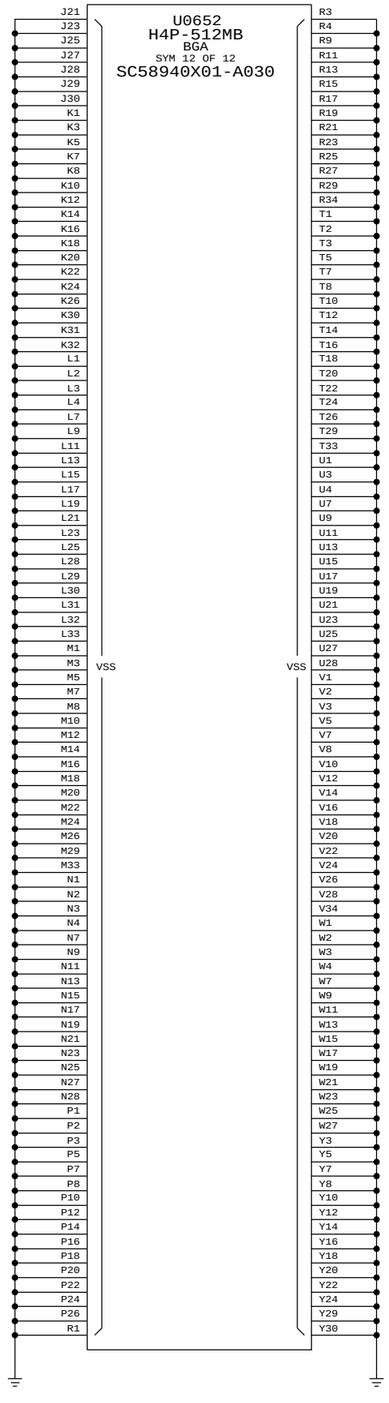
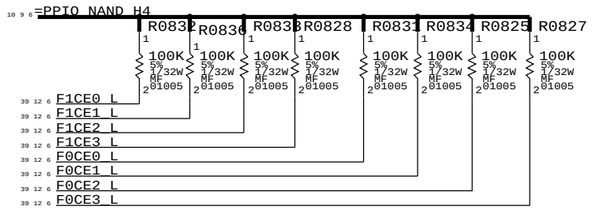
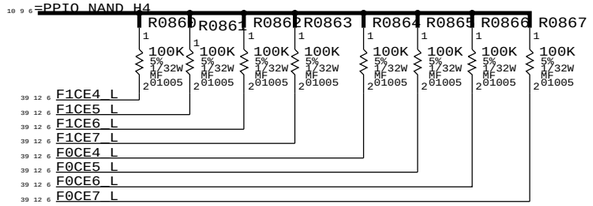
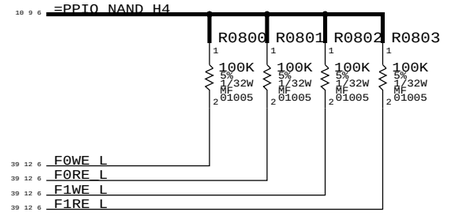
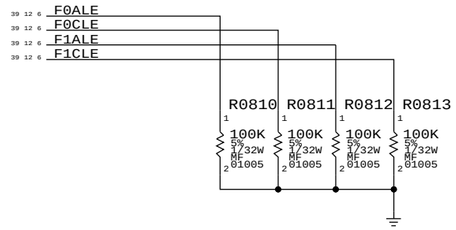
SHEET 5 OF 42

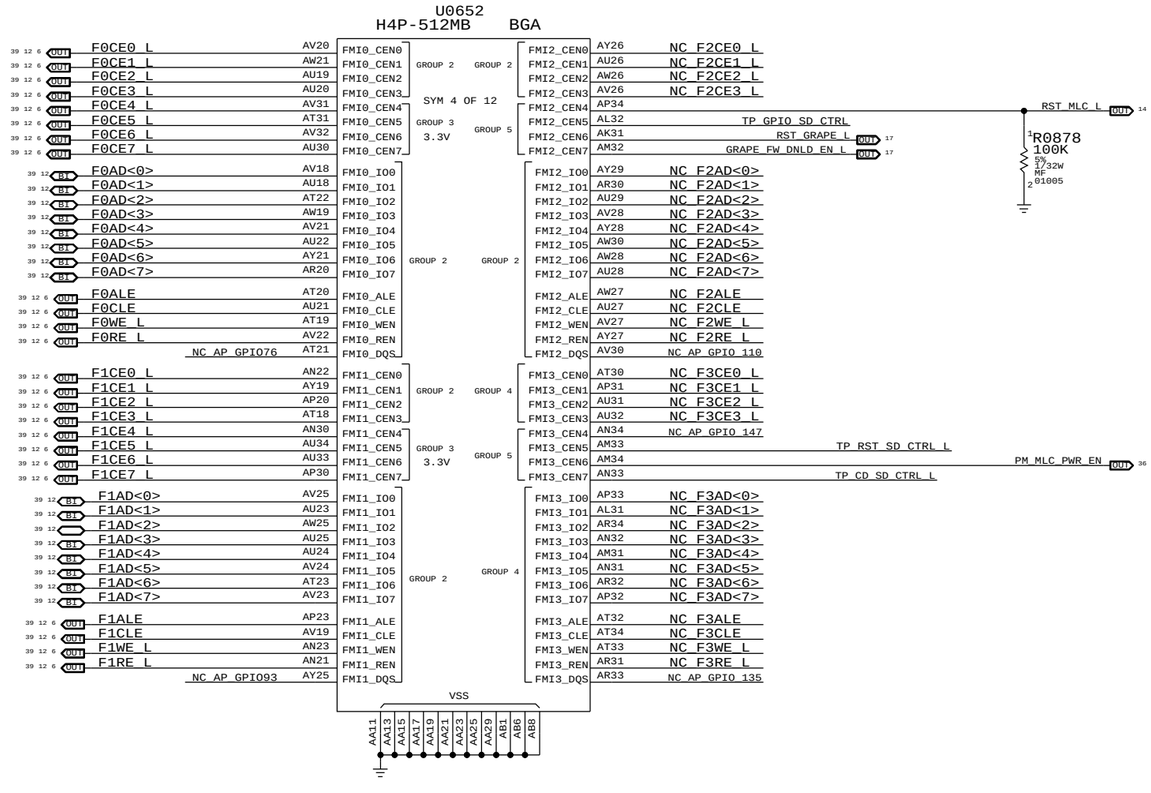












SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE

AP: NAND

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

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BRANCH

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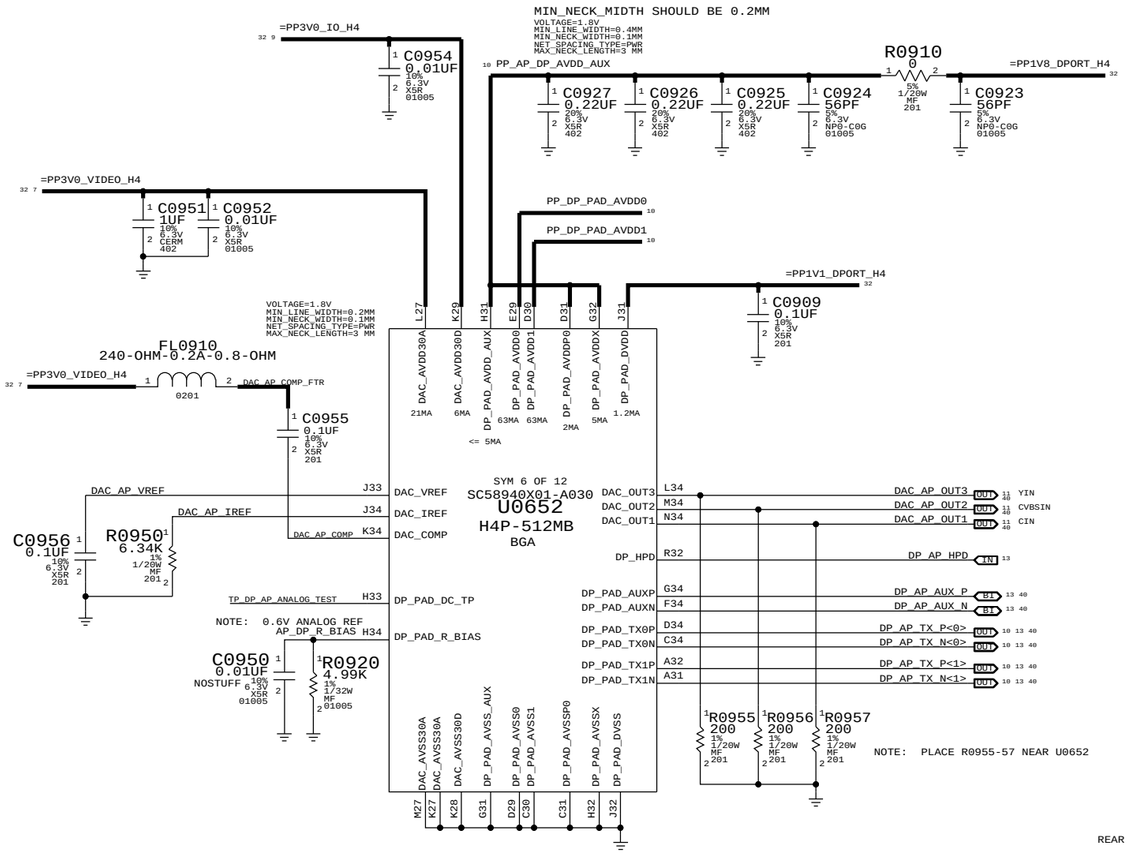
SHEET 6 OF 42



SYNC_MASTER=JAMES	SYNC_DATE=N/A
PAGE TITLE: AP: TV,DP,MIPI	
Apple Inc.	DRAWING NUMBER: 051-8962 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 9 OF 106
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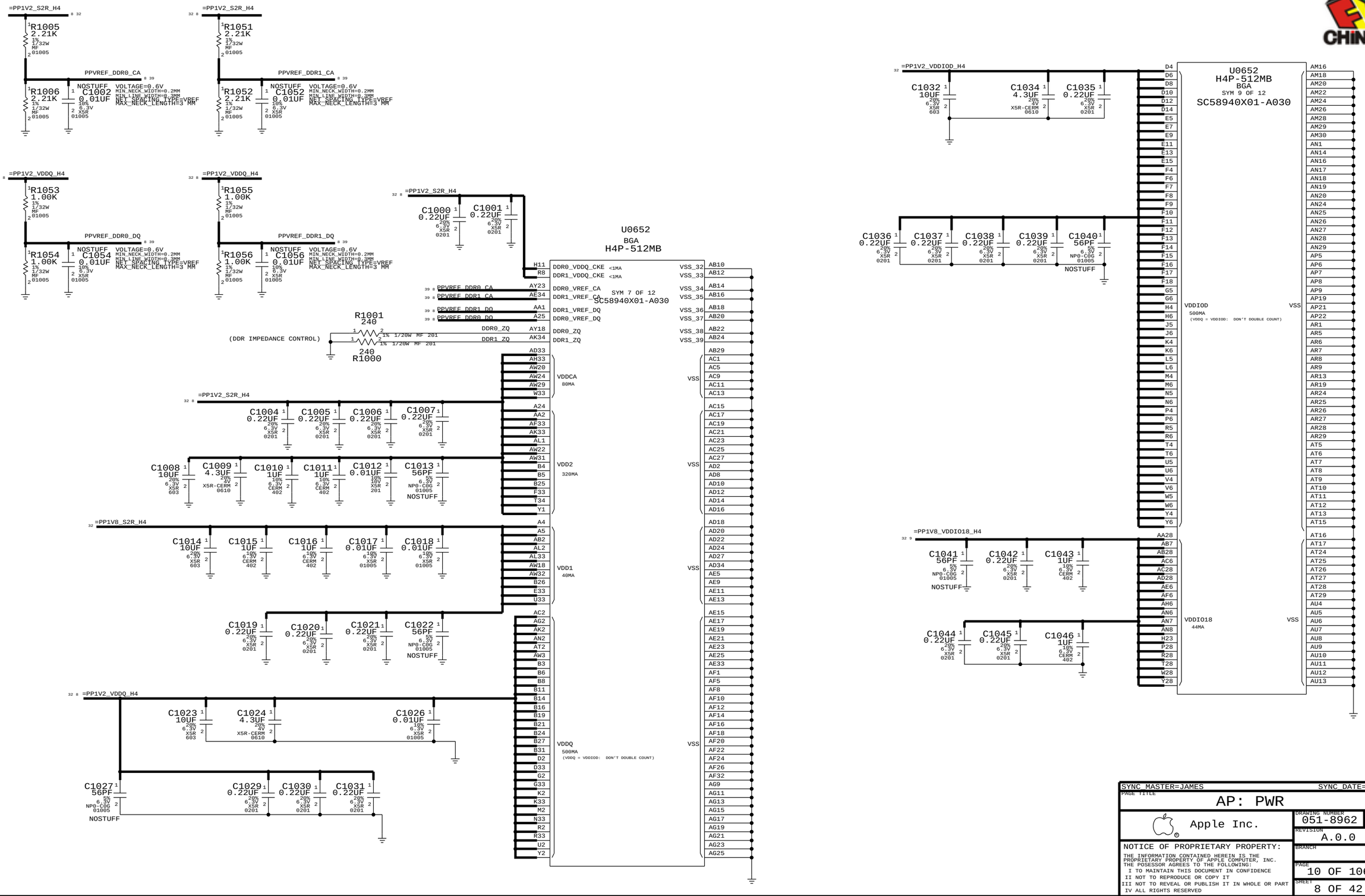

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE: AP: PWR

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH:

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=PPVDD_SOC_H4

C1100 4.3UF 20% 4V X5R-CERM 0610
C1101 10UF 20% 6.3V X5R 603
C1102 4.3UF 20% 4V X5R-CERM 0610
C1103 4.3UF 20% 4V X5R-CERM 0610

NOSTUFF NOSTUFF NOSTUFF NOSTUFF

C1104 56PF 5% 6.3V NP0-C0G 01005
C1105 56PF 5% 6.3V NP0-C0G 01005
C1106 56PF 5% 6.3V NP0-C0G 01005
C1107 56PF 5% 6.3V NP0-C0G 01005

C1108 0.22UF 20% 6.3V X5R 0201
C1109 0.22UF 20% 6.3V X5R 0201
C1110 0.22UF 20% 6.3V X5R 0201
C1111 0.22UF 20% 6.3V X5R 0201

C1112 0.22UF 20% 6.3V X5R 0201
C1113 0.22UF 20% 6.3V X5R 0201
C1114 0.22UF 20% 6.3V X5R 0201
C1115 0.22UF 20% 6.3V X5R 0201
C1116 0.22UF 20% 6.3V X5R 0201

C1117 0.22UF 20% 6.3V X5R 0201
C1118 0.22UF 20% 6.3V X5R 0201
C1119 0.22UF 20% 6.3V X5R 0201
C1120 0.22UF 20% 6.3V X5R 0201

C1121 4.3UF 20% 4V X5R-CERM 0610

U0652
H4P-512MB
BGA
SYM 10 OF 12
SC58940X01-A030

VDD 2100MA

AA20 AA22 AA24 AB9 AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AC8 AC10 AC12 AC14 AC16 AC18 AC20 AC22 AC24 AD9 AD11 AD13 AD15 AD17 AD19 AD21 AD23 AD25 AE8 AE10 AE12 AE14 AE16 AE18 AE20 AE22 AE24 AF9 AF11 AF13 AF15 AF17 AF19 AF21 AF23 AF25 AG8 AG10 AG12 AG14 AG16 AG18 AG20 AG22 AG24 AG26 AH9 AH11 AH13 AH15 AH17 AH19 AH21 AH23 AH25 AJ8 AJ10 AJ12 AJ14 AJ16 AJ18 AJ20 AJ22 AJ24 AJ26 AK9 AK11 AK13 AK15 AK17 AK19 AK21 AK23 AK25 AL8 AL10 AL12 AL14 AL16 AL18

AL20 AL22 AL24 AL26 AM9 AM11 AM13 AM15 AM17 AM19 AM21 AM23 AM25 H9 H13 H15 H17 H19 H21 J8 J10 J12 J14 J16 J18 J20 J22 J24 K9 K11 K13 K15 K17 K19 K21 K23 K25 L8 L10 L12 L14 L16 L18 L20 L22 L24 L26 M9 M11 M13 M15 M17 M19 M21 M23 M25 N20 N22 N24 N26 P19 P21 P23 P25 P27 R20 R22 R24 R26 T19 T21 T23 T25 T27 U20 U22 U24 U26 V19 V21 V23 V25 V27 W20 W22 W24 W26 Y19 Y21 Y23 Y25

=PPVDD_CPU_H4

C1125 10UF 20% 6.3V X5R 603
C1126 4.3UF 20% 4V X5R-CERM 0610
C1127 4.3UF 20% 4V X5R-CERM 0610
C1128 4.3UF 20% 4V X5R-CERM 0610

C1129 56PF 5% 6.3V NP0-C0G 01005
C1130 56PF 5% 6.3V NP0-C0G 01005
C1131 56PF 5% 6.3V NP0-C0G 01005
C1132 56PF 5% 6.3V NP0-C0G 01005

C1133 0.22UF 20% 6.3V X5R 0201
C1134 0.22UF 20% 6.3V X5R 0201
C1135 0.22UF 20% 6.3V X5R 0201
C1136 0.22UF 20% 6.3V X5R 0201

C1137 0.22UF 20% 6.3V X5R 0201
C1138 0.22UF 20% 6.3V X5R 0201
C1139 0.22UF 20% 6.3V X5R 0201
C1140 0.22UF 20% 6.3V X5R 0201
C1141 0.22UF 20% 6.3V X5R 0201

U0652
H4P-512MB
BGA
SYM 8 OF 12
SC58940X01-A030

AA8 AA10 AA12 AA14 AA16 AA18 N8 N10 N12 N14 N16 N18 P9 P11 P13 P15 P17 R10 R12 R14 R16 R18 T9 T11 T13 T15 T17 U8 U10 U12 U14 U16 U18 V9 V11 V13 V15 V17 W8 W10 W12 W14 W16 W18 Y9 Y11 Y13 Y15 Y17

VDD_CPU 1900MA

=PP3V0_IO_H4

C1142 0.22UF 20% 6.3V X5R 0201
C1143 0.22UF 20% 6.3V X5R 0201

G23 G24 U29 V29

VDDIO30 100MA

AJ7 AK7 AN9

VDDIOD0 9MA GPIO[30-39] 1.8V
VDDIOD1 10MA UART4 1.8V

=PP1V8_VDDIO18_H4

C1150 0.22UF 20% 6.3V X5R 0201
C1151 0.22UF 20% 6.3V X5R 0201
C1152 56PF 5% 6.3V NP0-C0G 01005

NOSTUFF

AP24 AP25 AP26 AP27 AP28 AR21 AR22 AR23

VDDIOD2 24MA EMI[0-2] 3.3V

=PPIO_NAND_H4

C1144 0.22UF 20% 6.3V X5R 0201
C1145 0.22UF 20% 6.3V X5R 0201
C1146 56PF 5% 6.3V NP0-C0G 0100S
C1147 1UF 10% 6.3V CERM 402
C1148 1UF 10% 6.3V CERM 402
C1149 10UF 20% 6.3V X5R 603

NOSTUFF

AP29 AL27 AM27 AJ27 AK27

VDDIOD3 24MA EMI[0-1]_CEN[4-7] 3.3V
VDDIOD4 24MA EMI[3] 3.3V
VDDIOD5 24MA EMI[2:3]_CEN[4-7] SPI3,ISP FLASH NOT USED

=PP3V0_IO_H4

C1180 1UF 10% 6.3V CERM 402
C1181 1UF 10% 6.3V CERM 402
C1182 1UF 10% 6.3V CERM 402
C1160 0.22UF 20% 6.3V X5R 0201
C1161 0.22UF 20% 6.3V X5R 0201

AH27 AG27

VDDIOD6 1MA SPI1
VDDIOD7 1MA I2C2
3.0V

VSS

AH5 AH8 AH10 AH12 AH14 AH16 AH18 AH20 AH22 AH24 AH26 AH28 AH34 AJ1 AJ2 AJ6 AJ9 AJ11 AJ13 AJ15 AJ17 AJ19 AJ21 AJ23 AJ25 AJ28 AJ29 AJ30 AJ31 AJ33 AJ34 AK1 AK3 AK4 AK5 AK6 AK8 AK10 AK12 AK14 AK16 AK18 AK20 AK22 AK24 AK26 AK28 AK29 AK30 AK32 AL3 AL4 AL5 AL9 AL11 AL13 AL15 AL17 AL19 AL21 AL23 AL25 AL28 AL29 AL30 AL34 AM7 AM8 AM10 AM12 AM14

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
AP: PWR

Apple Inc.

DRAWING NUMBER 051-8962
SIZE D
REVISION A.0.0
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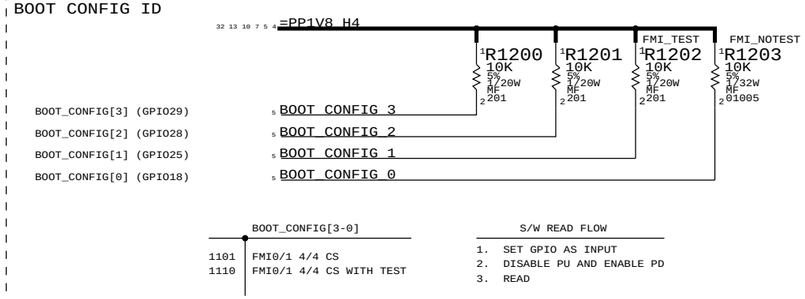
BOOT CONFIG ID

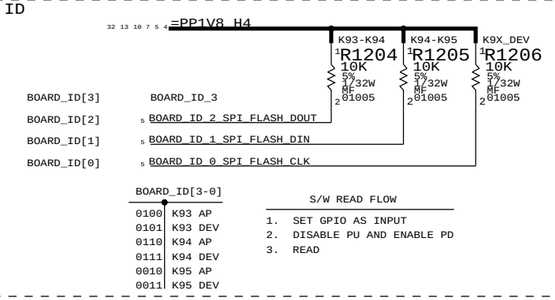


BOOT_CONFIG[3-0]	
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS WITH TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID

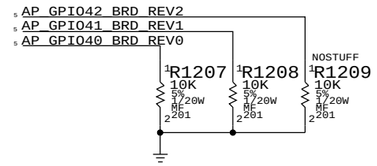


BOARD_ID[3-0]	
0100	K93 AP
0101	K93 DEV
0110	K94 AP
0111	K94 DEV
0010	K95 AP
0011	K95 DEV

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION



BRD_REV[2-0]	
000	PROTO 1
001	PROTO 2
010	EVT
011	EVT2
100	DVT

S/W READ FLOW

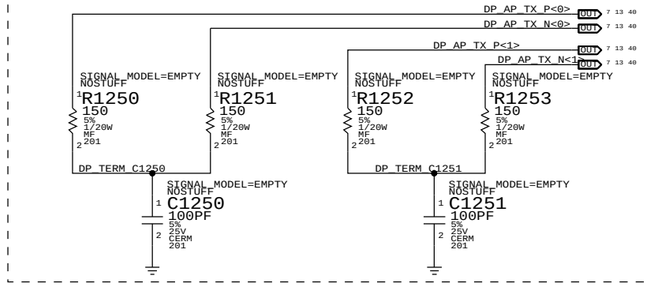
1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

FOR REFERENCE

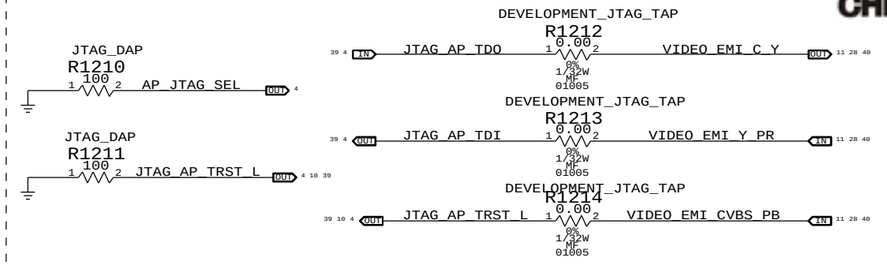
BOOT_CONFIG[3:0]

0000	SPI0
0001	SPI3
0010	SPI0 W/TEST
0011	SPI3 W/TEST
0100	FMI0 2CS
0101	FMI0 4CS
0110	FMI0 4CS W/TEST
0111	RESERVED
1000	FMI1 2 CS
1001	FMI1 4 CS
1010	FMI1 4CS W/TEST
1011	RESERVED
1100	FMI0/1 2/2 CS
CURRENT SETTING -> 1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS W/TEST
1111	RESERVED

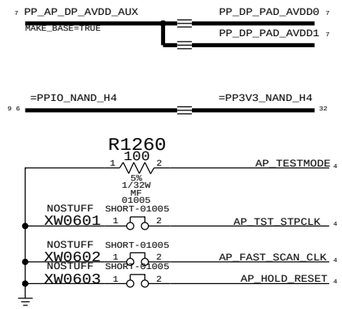
PLACEMENT NOTE: NEAR U0652

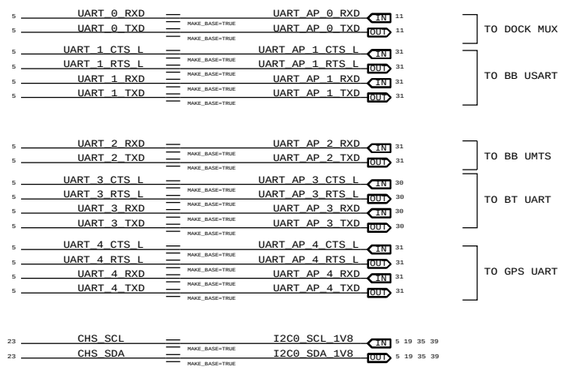


JTAG



2-WIRE DAP	SCAN DUMP	PRODUCTION
DEVELOPMENT_JTAG	DEVELOPMENT_JTAG	JTAG_DAP
JTAG_DAP	DEVELOPMENT_JTAG_TAP	





SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE

AP: MISC & ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 | SIZE D

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NOTE:
LDO3 PROVIDES 50MA TO BOTH H4P AND U1300
IF THAT'S NOT ENOUGH, STUFF R1371 AND NOSTUFF R1370

=PP3V0_VIDEO_BUF
R1371 0.00 0% 1/32W MF 01005
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
NOSTUFF
=PP3V0_VIDEO_BUFFER
R1370 0.00 0% 1/32W MF 01005
~15MA
PP3V0_U0900_FILTR
C1370 0.1UF 10% 6.3V X5R 201

=PP3V2_S2R_USBMUX
C1301 56PF 5% 6.3V NP0-C0G 01005
C1300 0.1UF 10% 6.3V X5R 201

U1300
THS7380IZSYR
UCSP

VA_0 C1, VA_1 C4, VDL D2, VDH E2

PORT_DOCK_VIDEO_AMP_EN
R1372 100K 5% 1/32W MF 01005

NOTE: PLACE R0960-62 NEAR U0900

YIN	DAC_AP_OUT3	A3	CH.1_IN	CH.1_OUT	A2	BUF_Y_PR	JTAG_DAP R1360 75 1% 1/20W MF 201 VIDEO_EMI_Y_PR
CVBSIN	DAC_AP_OUT2	A4	CH.2_IN	CH.2_OUT	A1	BUF_CVBS_PB	JTAG_DAP R1361 75 1% 1/20W MF 201 VIDEO_EMI_CVBS_PB
CIN	DAC_AP_OUT1	B4	CH.3_IN	CH.3_OUT	B1	BUF_C_Y	JTAG_DAP R1362 75 1% 1/20W MF 201 VIDEO_EMI_C_Y
	UART_AP_0_TXD	D4	TX_VLOW	RX_VHIGH/USB_2D+	E1	USB_FS_P_ACC_RX	
	UART_AP_0_RXD	E4	RX_VLOW	TX_VHIGH/USB_2D-	D1	USB_FS_N_ACC_TX	
	USB_BB_D_P	F3	USB_D+	USB_1D+	F2	USB_FS_D_P	
	USB_BB_D_N	F4	USB_D-	USB_1D-	F1	USB_FS_D_N	
				SEL	C2	DOCK_BB_EN	

VID_EN C3
AGND B2, B3
DGND D3, E3

R1315 1.00M 5% 1/32W MF 01005
R1320 100K 5% 1/32W MF 01005

NOTE:
DOCK_BB_EN = 1: BB USB <-> DOCK SERIAL
DOCK_BB_EN = 0: BB USB <-> H4P FS USB
H4P UART0 <-> DOCK SERIAL

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
AP: VIDEO BUFFER,BB USB MUXES

Apple Inc.

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16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	1	TOSHIBA 32NM 16GB RAW	U1400	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	16GB_PROD	U1400	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	16GB_PROD	U1400	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	16GB_PROD	U1400	HYNIX 26NM 16GB PPN

32GB FLASH CONFIGURATIONS

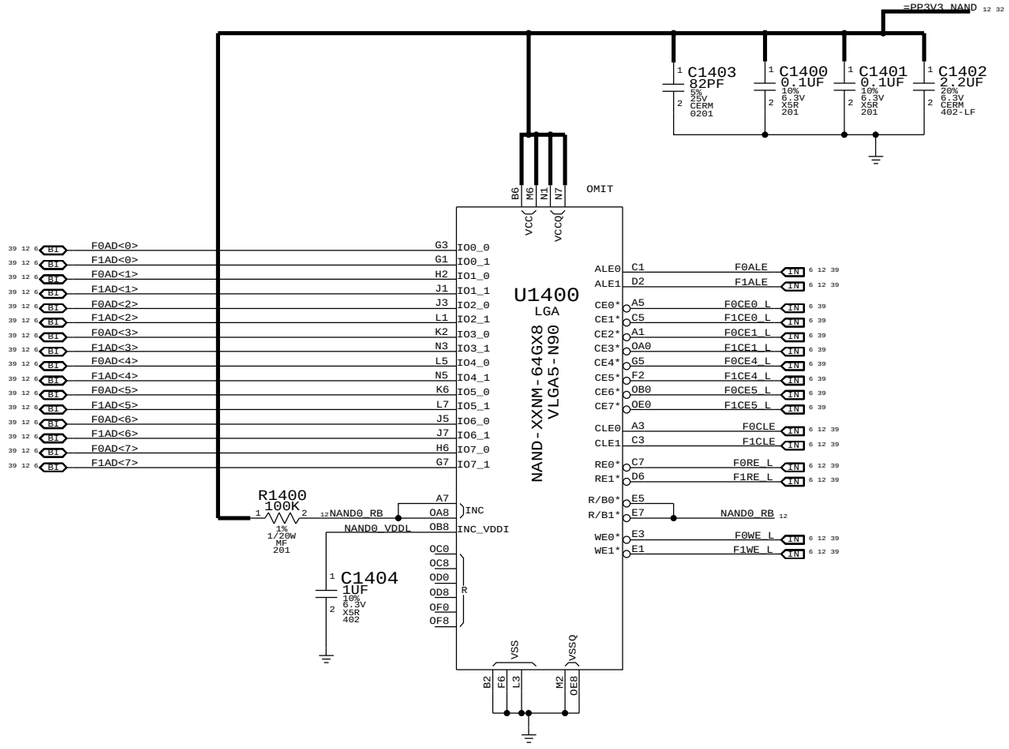
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	2	TOSHIBA 32NM 16GB RAW	U1400,U1410	32GB_PROD

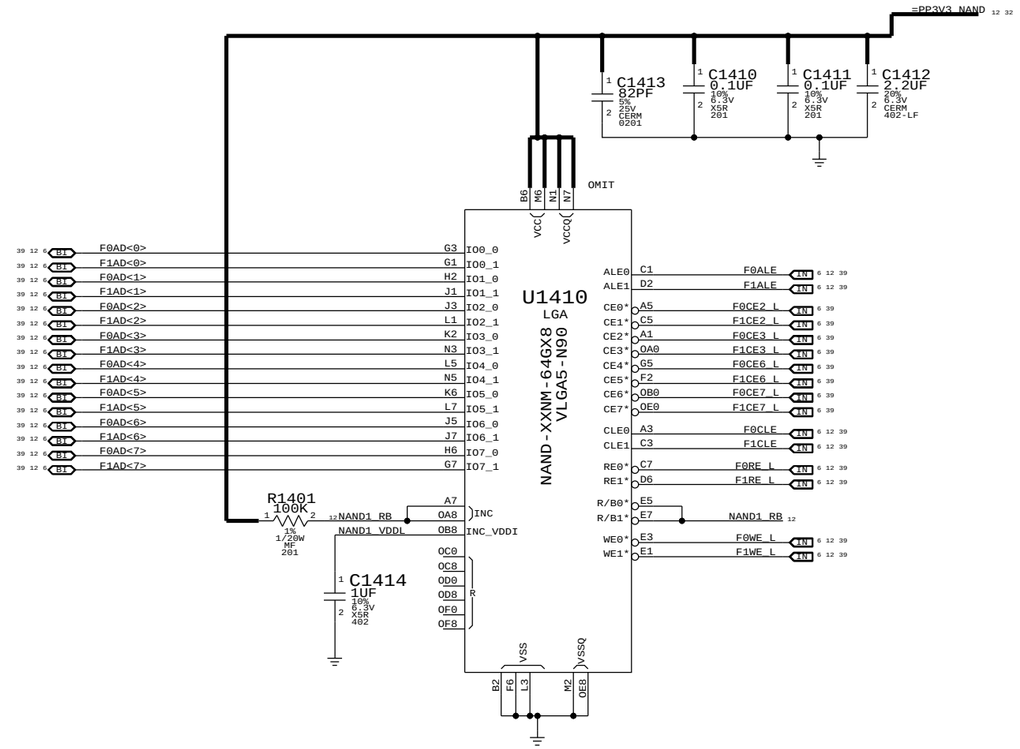
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	32GB_PROD	U1400,U1410	HYNIX 26NM 16GB PPN

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0702	2	TOSHIBA 32NM 32GB RAW	U1400,U1410	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0665	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 35NM 32GB RAW
335S0791	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 27NM 32GB RAW
335S0722	335S0702	64GB_PROD	U1400,U1410	SANDISK 32NM 32GB RAW
335S0782	335S0702	64GB_PROD	U1400,U1410	HYNIX 26NM 32GB PPN





SYNC_MASTER=JONATHAN SYNC_DATE=N/A

PAGE TITLE: NAND

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH:

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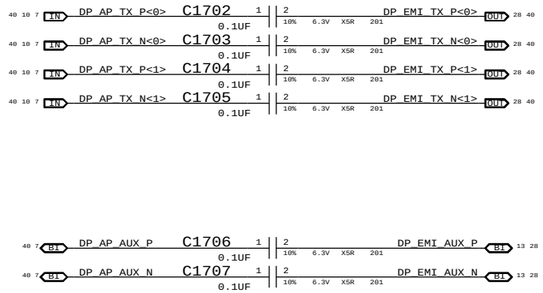
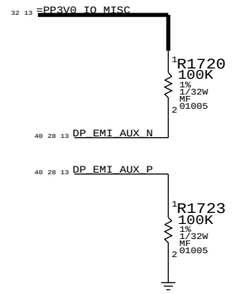
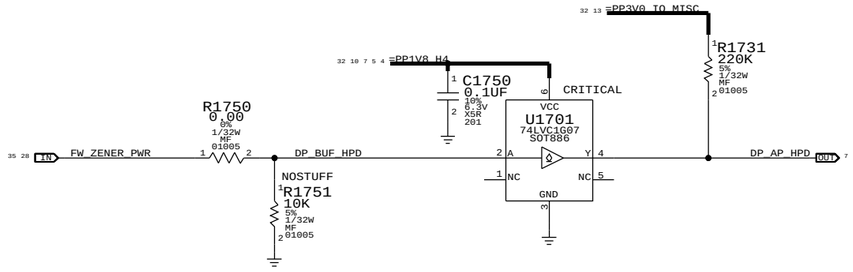
DISPLAYPORT AC COUPLING





DISPLAYPORT HOT PLUG DETECT



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0536	311S0341		U1701	RADAR:8481319

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
VIDEO: DISPLAY PORT

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

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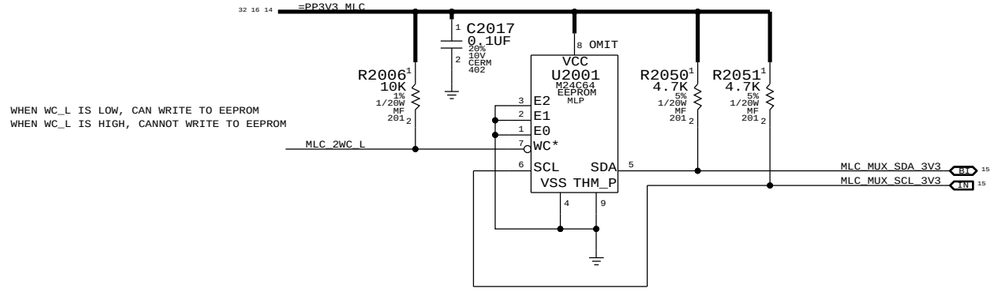
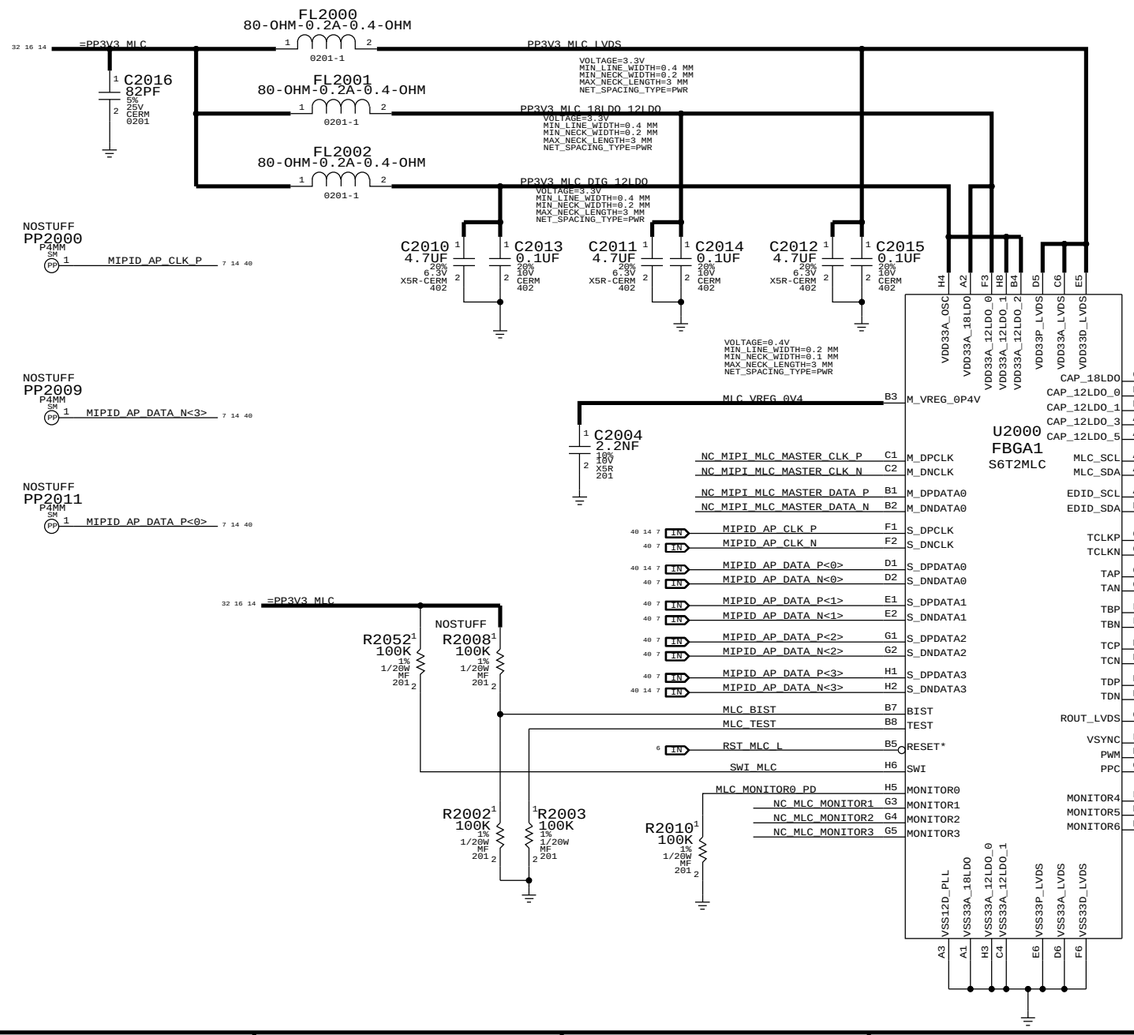
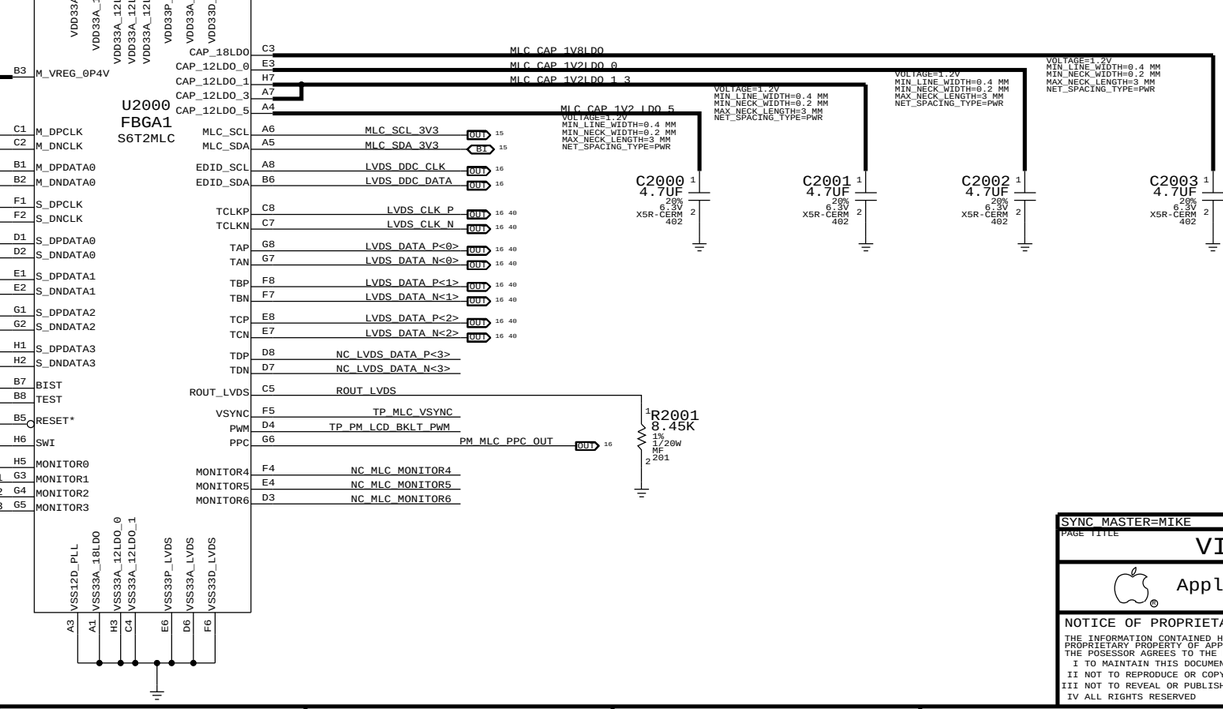
MLC EEPROM:RAW APN 335S0661

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2799	1	MLC EEPROM 100MHZ LVDS,2MHZ SWI	U2001	CRITICAL	100MHZ_PANEL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0618			RADAR:8377307







SYNC_MASTER=MIKE	SYNC_DATE=N/A
PAGE TITLE: VIDEO: MLC	
Apple Inc.	DRAWING NUMBER: 051-8962 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 20 OF 106
	SHEET: 14 OF 42

14 MLC_SDA_3V3 ═══ MLC_MUX_SDA_3V3 14
14 MLC_SCL_3V3 ═══ MLC_MUX_SCL_3V3 14

SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
VIDEO: MLC ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
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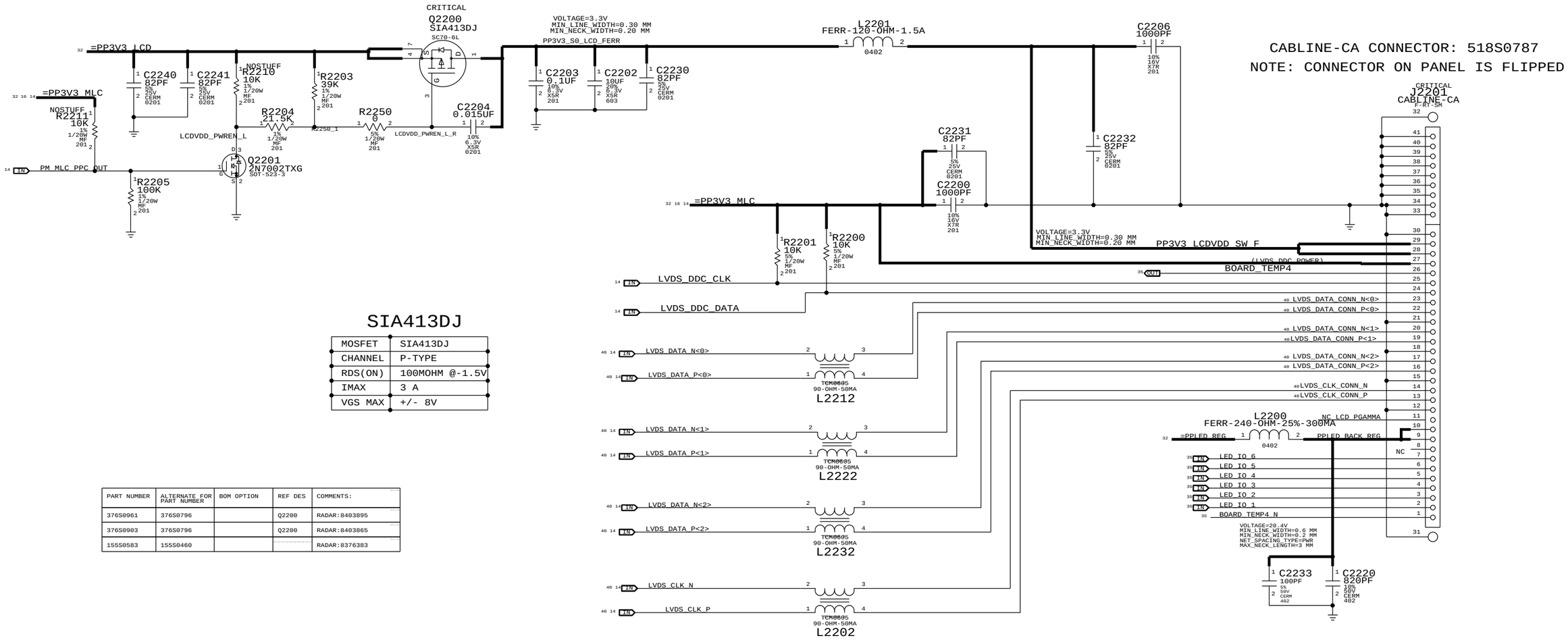
LVDS CONNECTOR



SIA413DJ

MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS(ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

NOSTUFF RESISTORS ARE THERE TO INVESTIGATE POSSIBILITY OF REMOVING THE CHOKE

SYNC_MASTER=ALEX SYNC_DATE=N/A

PAGE TITLE: VIDEO: LVDS CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH:

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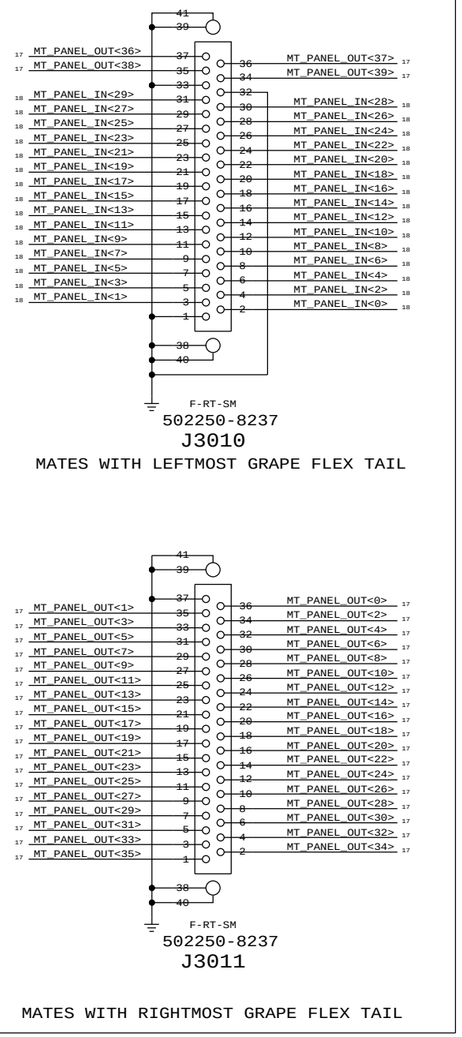
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

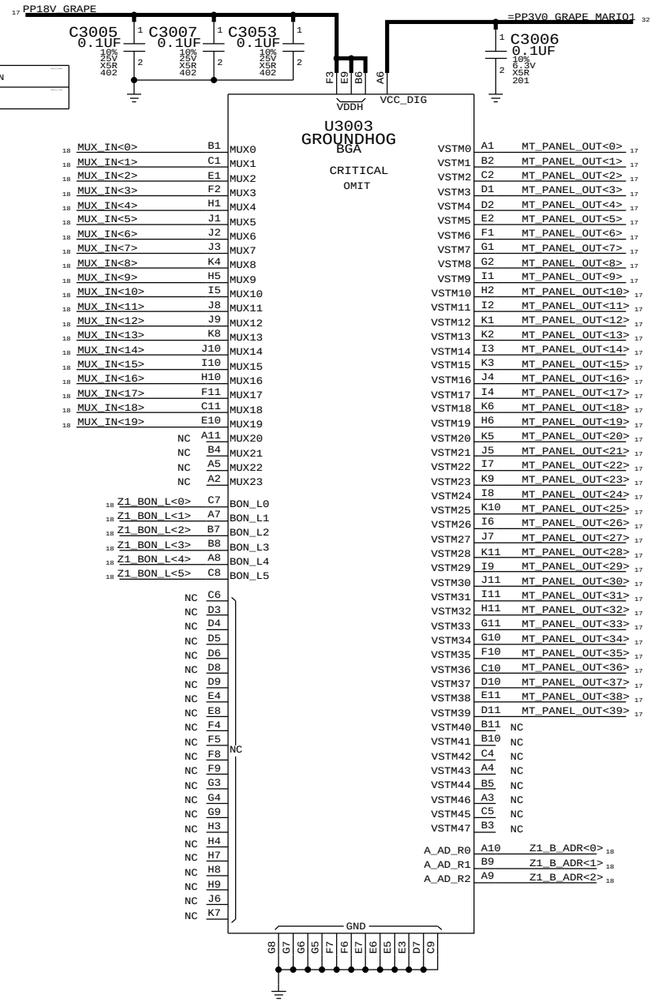
CONNECTORS TO GRAPE FLEX

P/N 518S0817

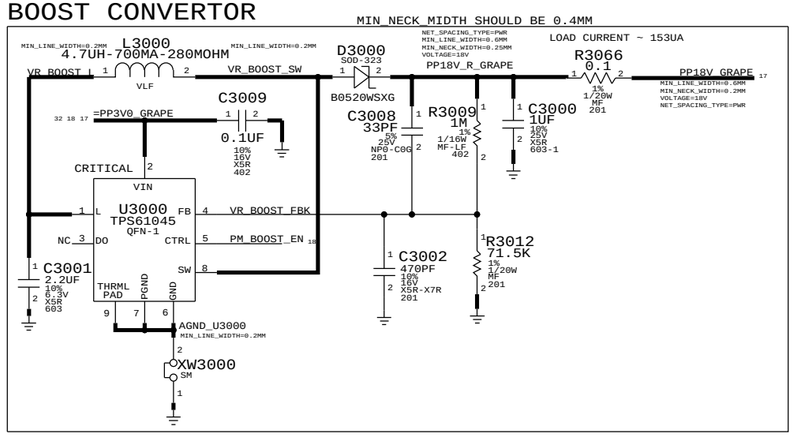


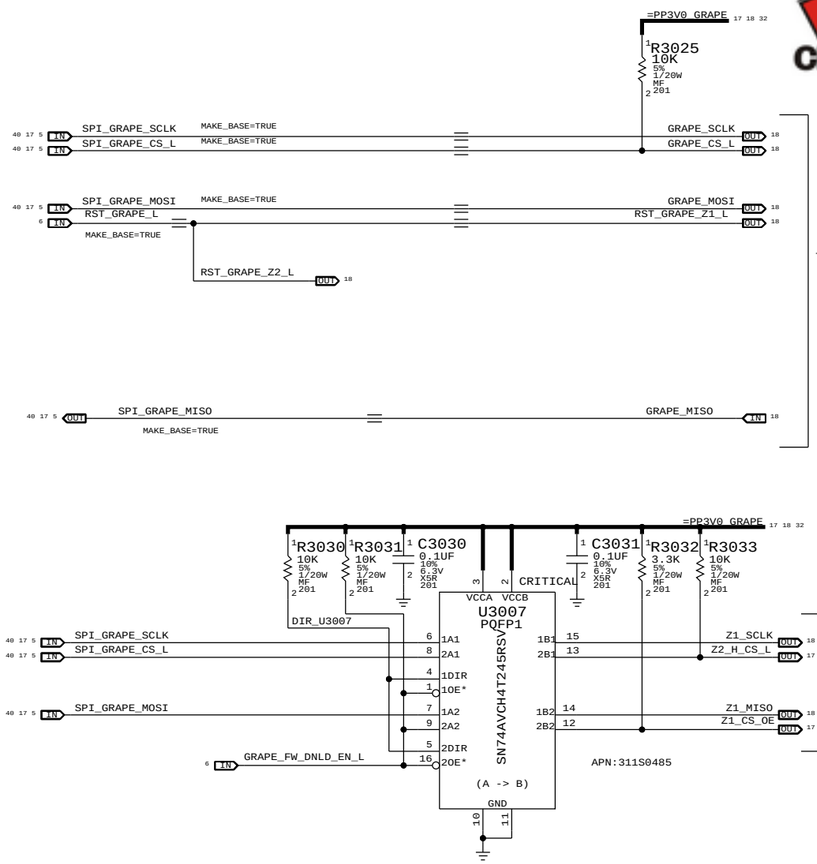
MATES WITH LEFTMOST GRAPE FLEX TAIL

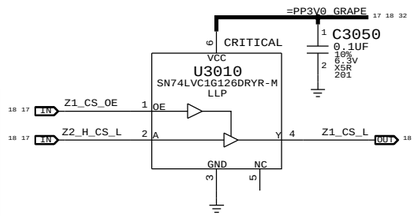
MATES WITH RIGHTMOST GRAPE FLEX TAIL

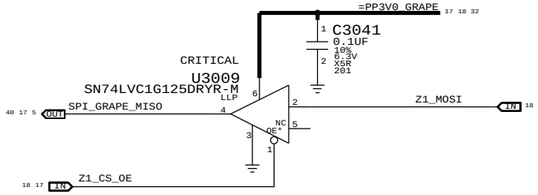


BOOST CONVERTOR









PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

SYNC_MASTER=RAMSIN SYNC_DATE=N/A

PAGE TITLE

GRAPE: GROUNDHOG,CONN,BOOST

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

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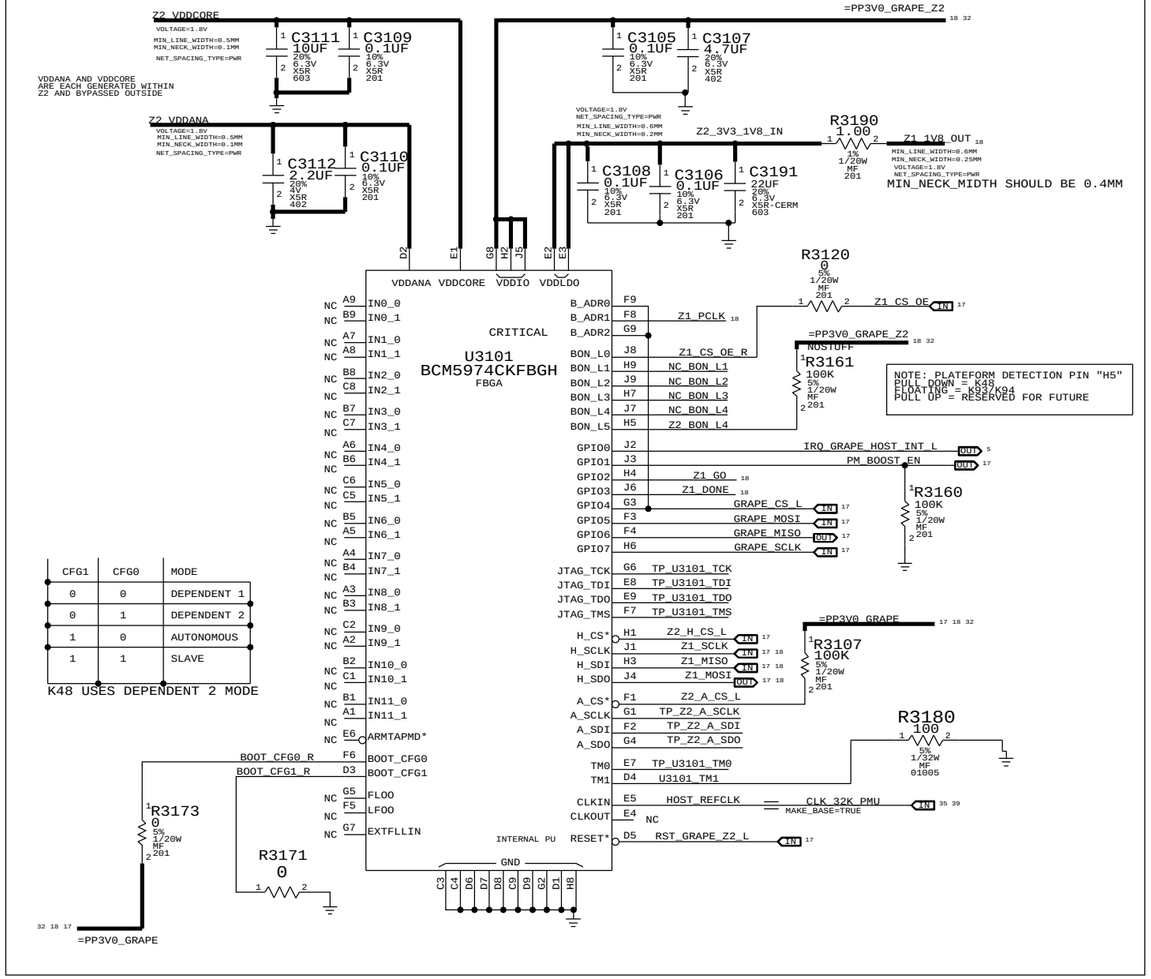
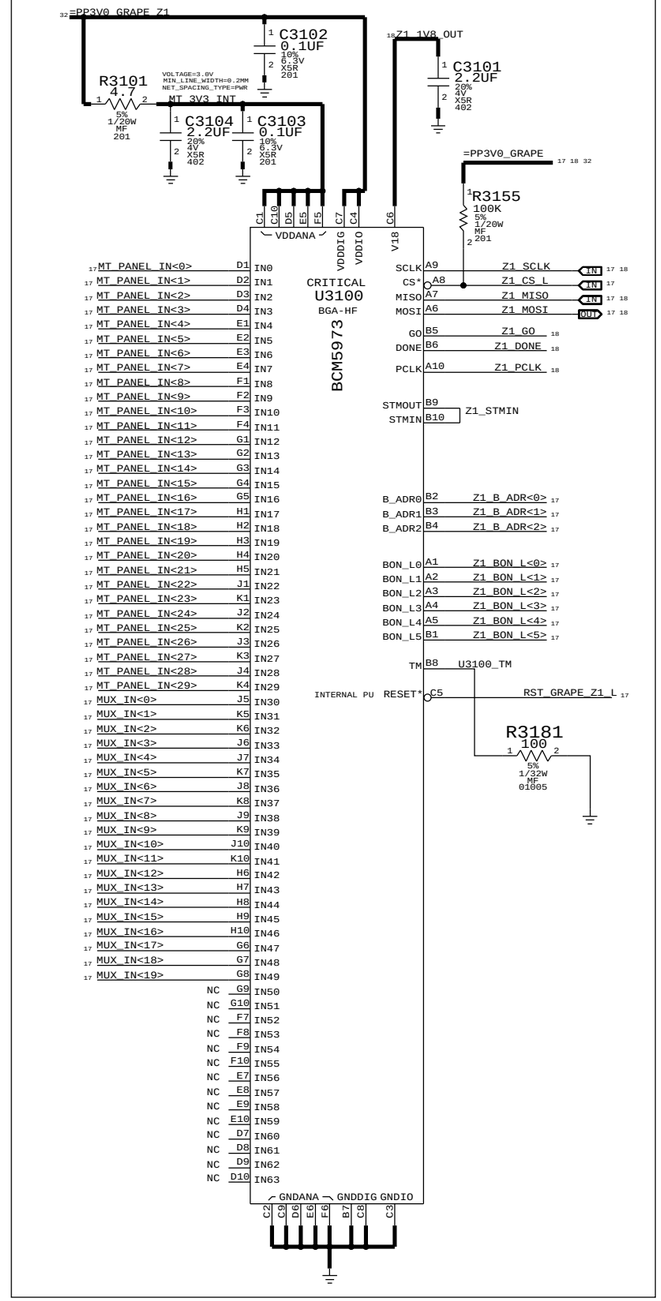
ARM9 MCU (Z2 BASED)



ZEPHYR 1+ ASIC



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0648		C3107	RADAR:8392120
138S0618	138S0648		C3107	BOM CONSOLIDATION

SYNC_MASTER=RAMSIN SYNC_DATE=N/A

PAGE TITLE: GRAPE: Z1, Z2

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

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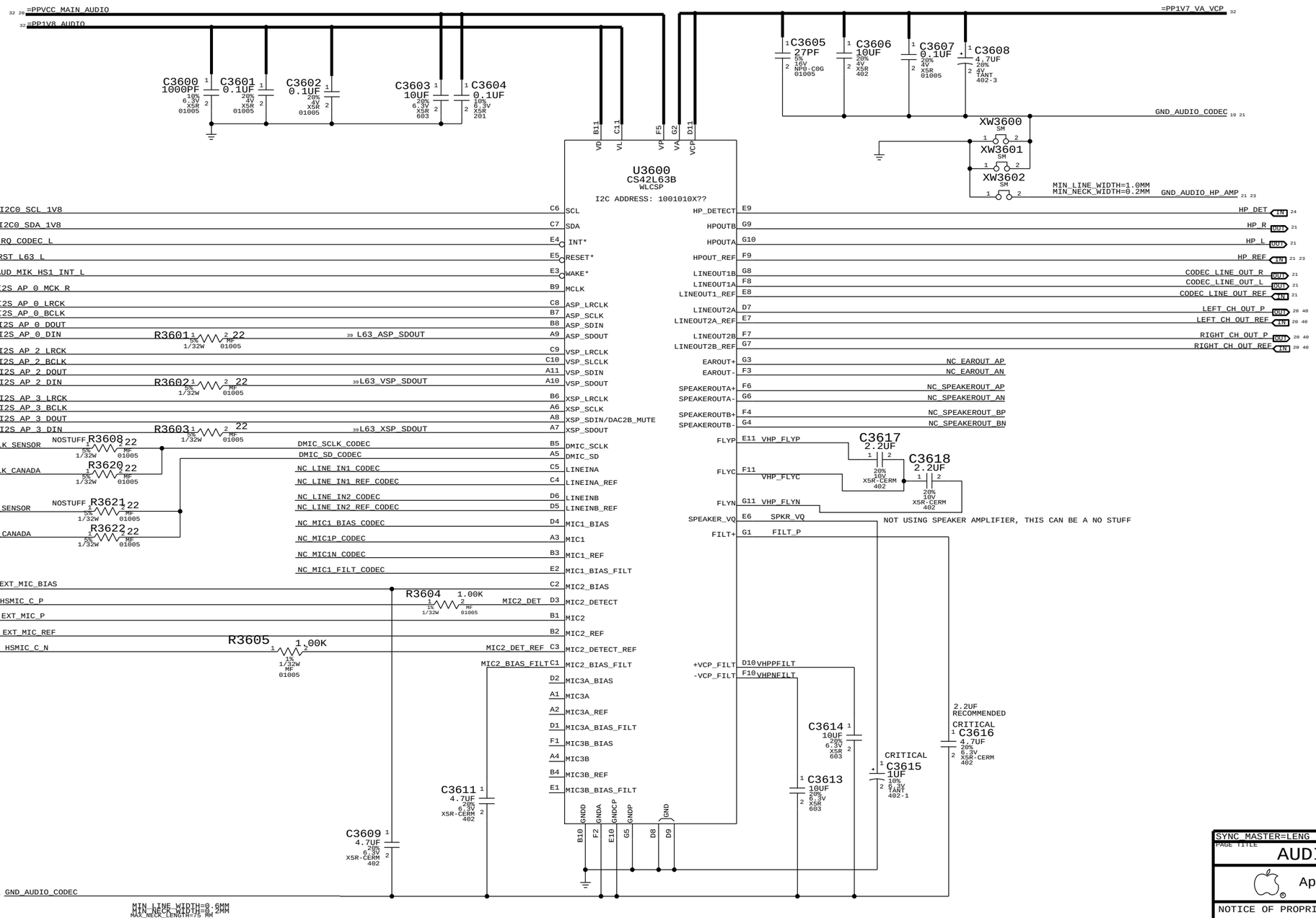
L63 AUDIO CODEC

APN:338S0940



SYNC_MASTER=LENG	SYNC_DATE=N/A
PAGE TITLE	AUDIO: L63 CODEC
Apple Inc.	DRAWING NUMBER 051-8962 SIZE D
	REVISION A.0.0
	BRANCH
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SPEAKER AMPLIFIER

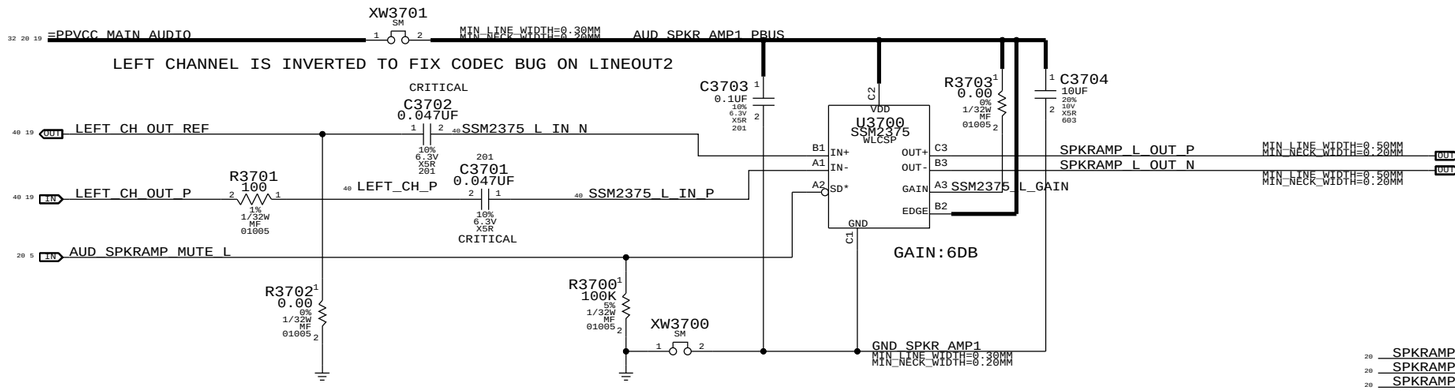
APN:353S2958

80HZ +/- XXX%

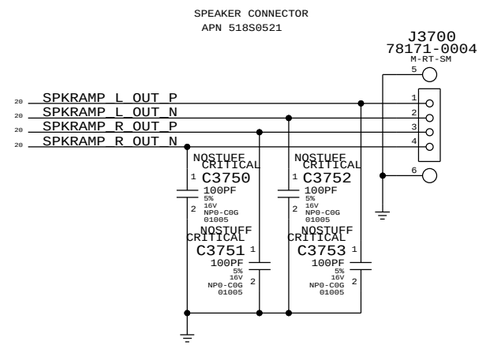
TURN ON TIME: 7.5MS

TURN ON DELAY: 20MS

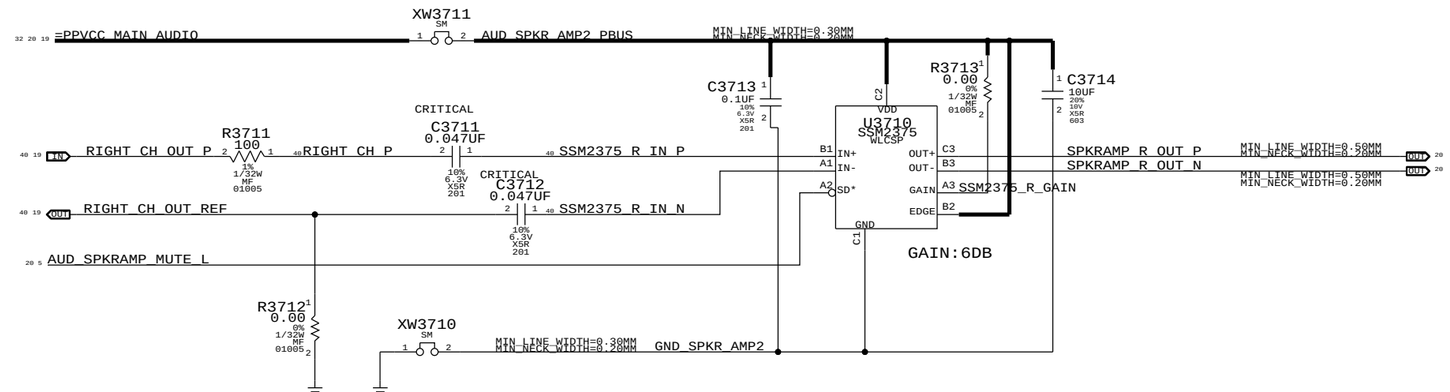
GAIN	VDD	GND
12DB	47K	NC
9DB	NC	47K
6DB	SHORT	NC
3DB	NC	NC
0DB	NC	SHORT



SPEAKER CONNECTOR
APN 518S0521



L63 LINEOUT2A IS CONNECTED TO U3700
L63 LINEOUT2B IS CONNECTED TO U3710



SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

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BRANCH

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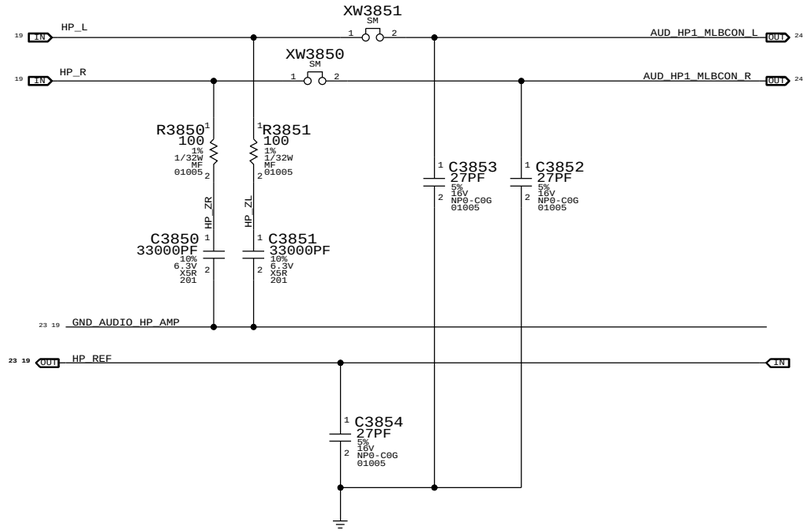
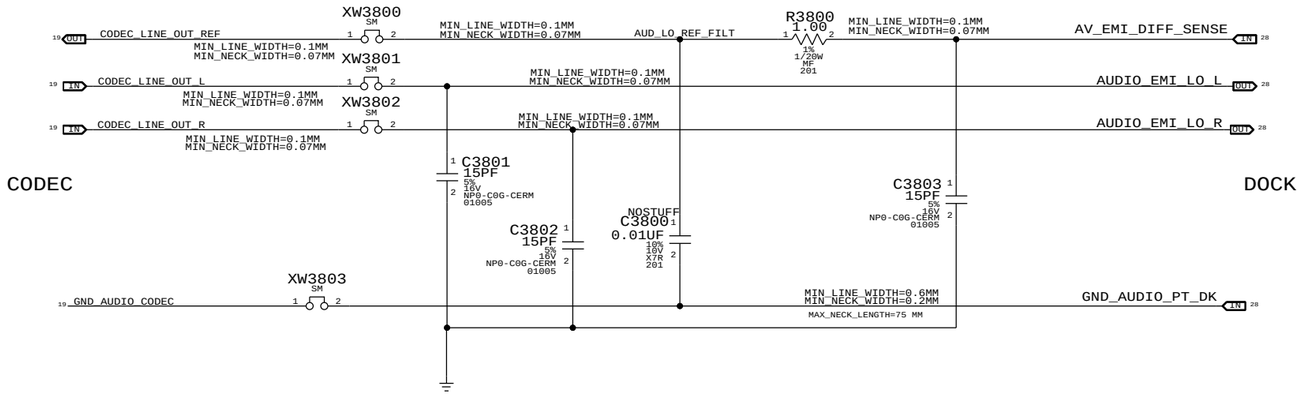
SHEET 20 OF 42

HEADPHONE OUTPUT ZOBEL NETWORK



DOCK LINE OUTPUT



SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE
AUDIO: HEADPHONE OUT

Apple Inc.

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SHEET 21 OF 42

SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE

AUDIO: BLANK

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DRAWING NUMBER 051-8962 SIZE D

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BRANCH

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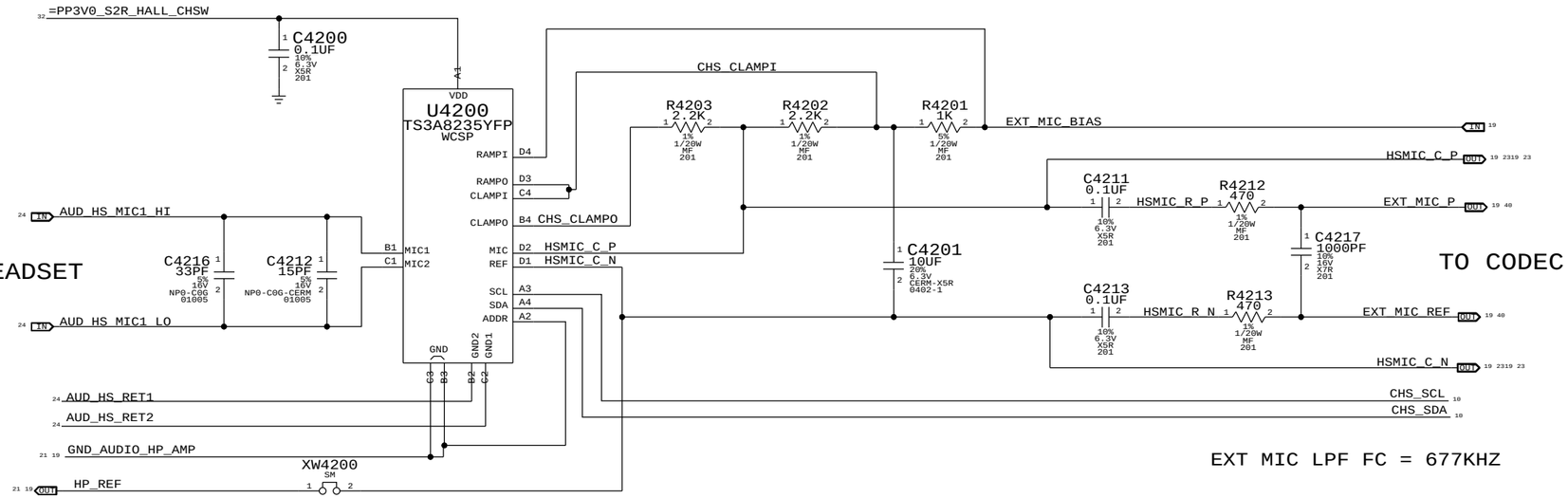
EXTERNAL (HEADSET) MIC INPUT CIRCUITRY



EXT MIC LPF FC = 677KHZ

SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE

AUDIO: DETECT/MIC BIAS

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

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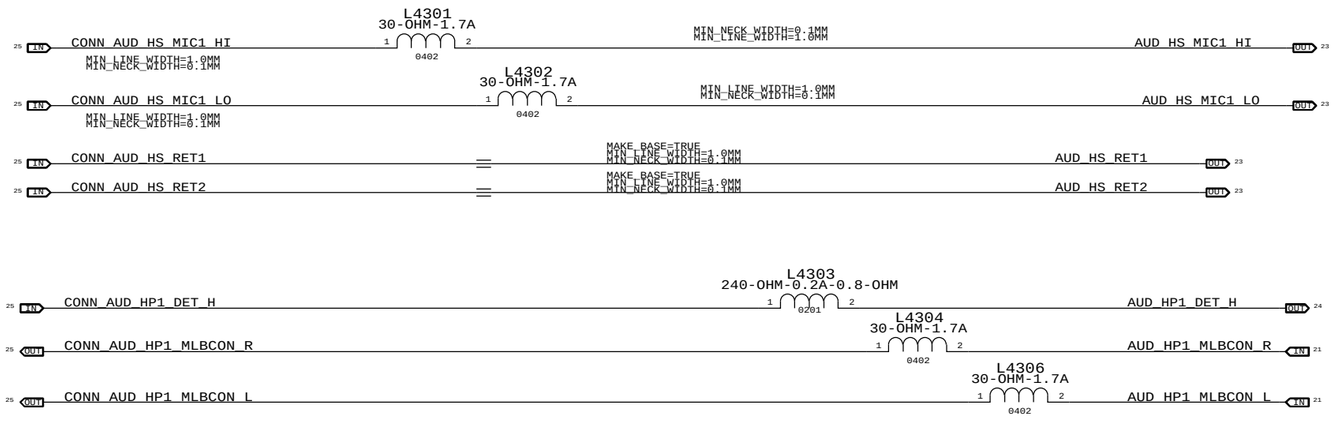
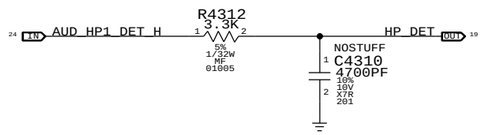
HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29
PLACE ALL COMPONENTS NEAR J5501



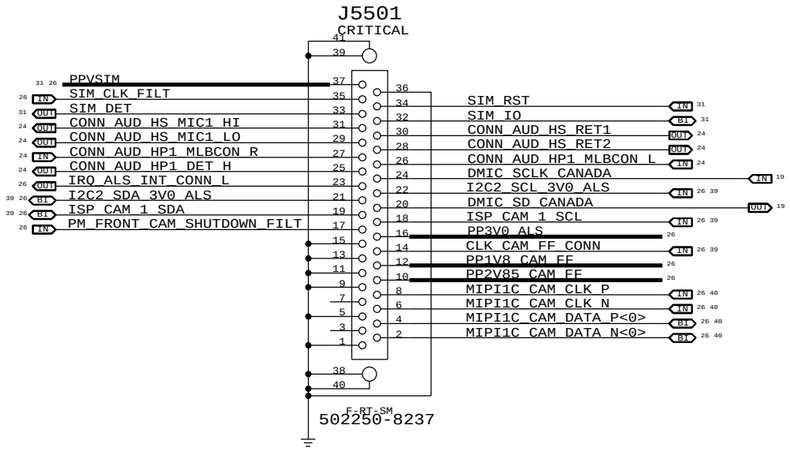
HEADSET JACK INSERTION DETECT



SYNC_MASTER=LENG	SYNC_DATE=N/A
PAGE TITLE: AUDIO: HP/MIC FILTERS	
Apple Inc.	DRAWING NUMBER: 051-8962 · SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 43 OF 106
	SHEET: 24 OF 42

CANADA FLEXES CONN.

APN: 518S0817



SENSOR BOARD CONN ALIASES

39 27	CLK_CAM_RF_FILT	MAKE_BASE=TRUE	CONN_CLK_CAM_RF_FILT	27
40 27	MIPI0C_CAM_DATA_N<0>	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_DATA_N<0>	27
40 27	MIPI0C_CAM_DATA_P<0>	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_DATA_P<0>	27
		MAKE_BASE=TRUE		
40 27	MIPI0C_CAM_CLK_N		CONN_MIPI0C_CAM_CLK_N	27
40 27	MIPI0C_CAM_CLK_P	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_CLK_P	27
7	PM_REAR_CAM_SHUTDOWN	MAKE_BASE=TRUE	CONN_PM_REAR_CAM_SHUTDOWN	27
27	PP1V8_SENSOR_FILT	MAKE_BASE=TRUE	CONN_PP1V8_SENSOR_FILT	27
27	PP2V85_CAM_REAR	MAKE_BASE=TRUE	CONN_PP2V85_CAM_REAR	27
19	DMIC_SD_SENSOR	MAKE_BASE=TRUE	CONN_DMIC_SD_SENSOR	27
19	DMIC_SCLK_SENSOR	MAKE_BASE=TRUE	CONN_DMIC_SCLK_SENSOR	27
39 7	ISP_AP_0_SCL	MAKE_BASE=TRUE	CONN_ISP_AP_0_SCL	27
39 7	ISP_AP_0_SDA	MAKE_BASE=TRUE	CONN_ISP_AP_0_SDA	27
39 26 5	I2C2_SCL_3V0	MAKE_BASE=TRUE	CONN_I2C2_SCL_3V0	27
39 26 5	I2C2_SDA_3V0	MAKE_BASE=TRUE	CONN_I2C2_SDA_3V0	27
5	IRQ_ACCEL_INT1_L	MAKE_BASE=TRUE	CONN_IRQ_ACCEL_INT1_L	27
5	IRQ_ACCEL_INT2_L	MAKE_BASE=TRUE	CONN_IRQ_ACCEL_INT2_L	27
5	IRQ_GYRO_INT1	MAKE_BASE=TRUE	CONN_IRQ_GYRO_INT1	27
5	IRQ_GYRO_INT2	MAKE_BASE=TRUE	CONN_IRQ_GYRO_INT2	27
39 5	I2C1_SCL_1V8	MAKE_BASE=TRUE	CONN_I2C1_SCL_1V8	27
39 5	I2C1_SDA_1V8	MAKE_BASE=TRUE	CONN_I2C1_SDA_1V8	27
35	IRQ_HALL	MAKE_BASE=TRUE	CONN_IRQ_HALL	27
5	IRQ_PROX_INT_L	MAKE_BASE=TRUE	CONN_IRQ_PROX_INT_L	27
27	PP3V0_S2R_HALL_FILT	MAKE_BASE=TRUE	CONN_PP3V0_S2R_HALL	27
35 5	ONOFF_L	MAKE_BASE=TRUE	CONN_ONOFF_FTR_L	27
35 5	SRL_L	MAKE_BASE=TRUE	CONN_SRL_FTR_L	27
5	AUD_VOL_UP_L	MAKE_BASE=TRUE	CONN_AUD_VOL_UP_FTR_L	27
5	AUD_VOL_DOWN_L	MAKE_BASE=TRUE	CONN_AUD_VOL_DOWN_FTR_L	27
		MAKE_BASE=TRUE		
27	PP3V0_OPTICAL_SENS	MAKE_BASE=TRUE	CONN_PP3V0_OPTICAL_SENS	27

SYNC_MASTER=MARK B. SYNC_DATE=N/A

PAGE TITLE

CONNECTOR: CANADA FLEX CONN,SENSOR PANEL ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

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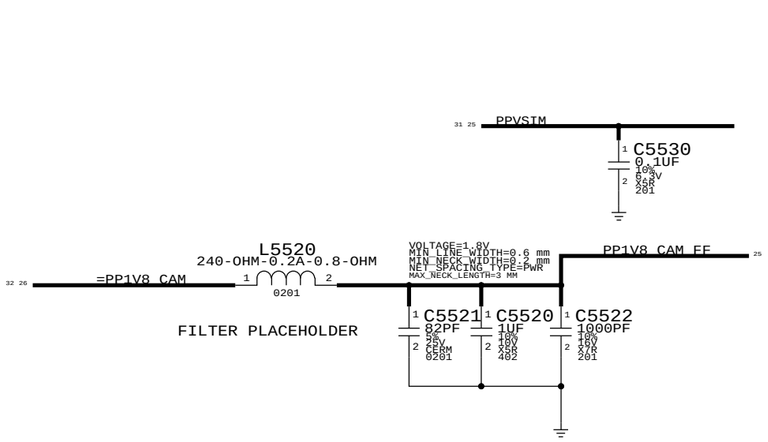
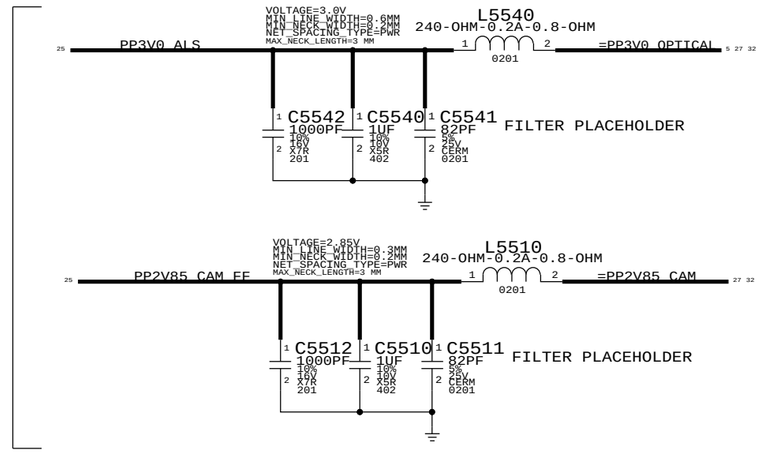
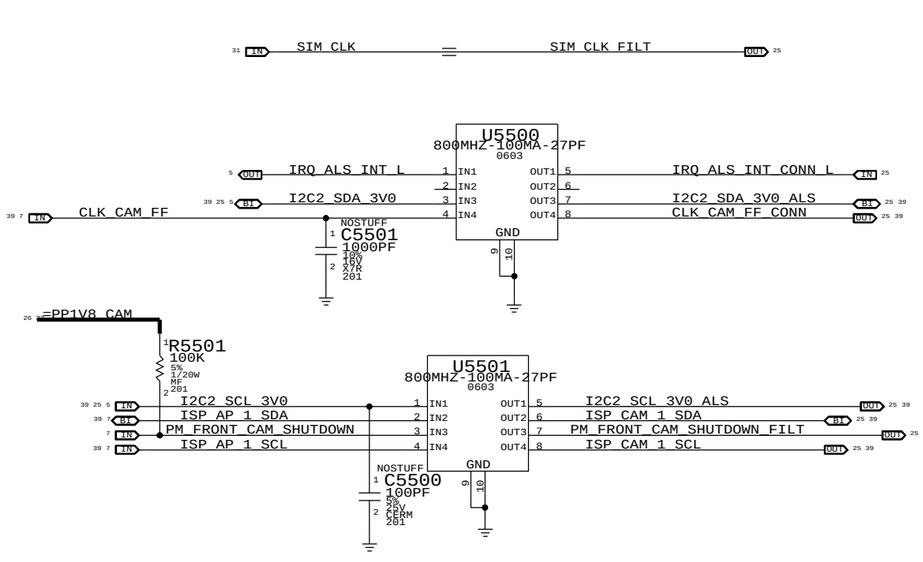
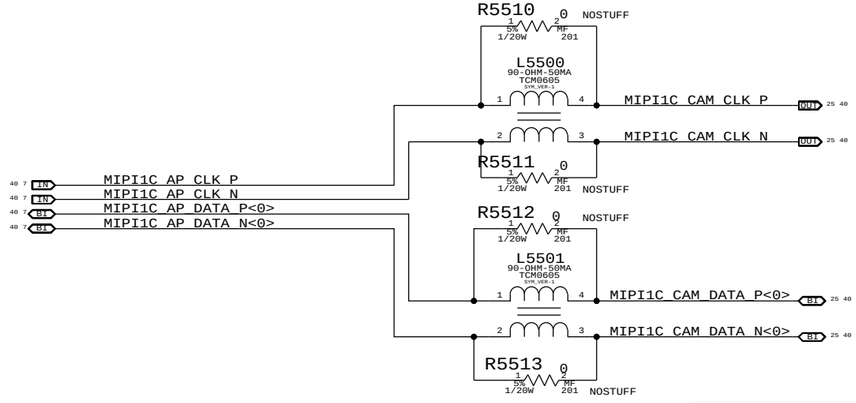


CANADA FLEX CONN ON PG 54



CANADA FLEX SIGNAL FILTERS





SYNC_MASTER=MARK B. SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: CANADA FLEX FILTERS

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
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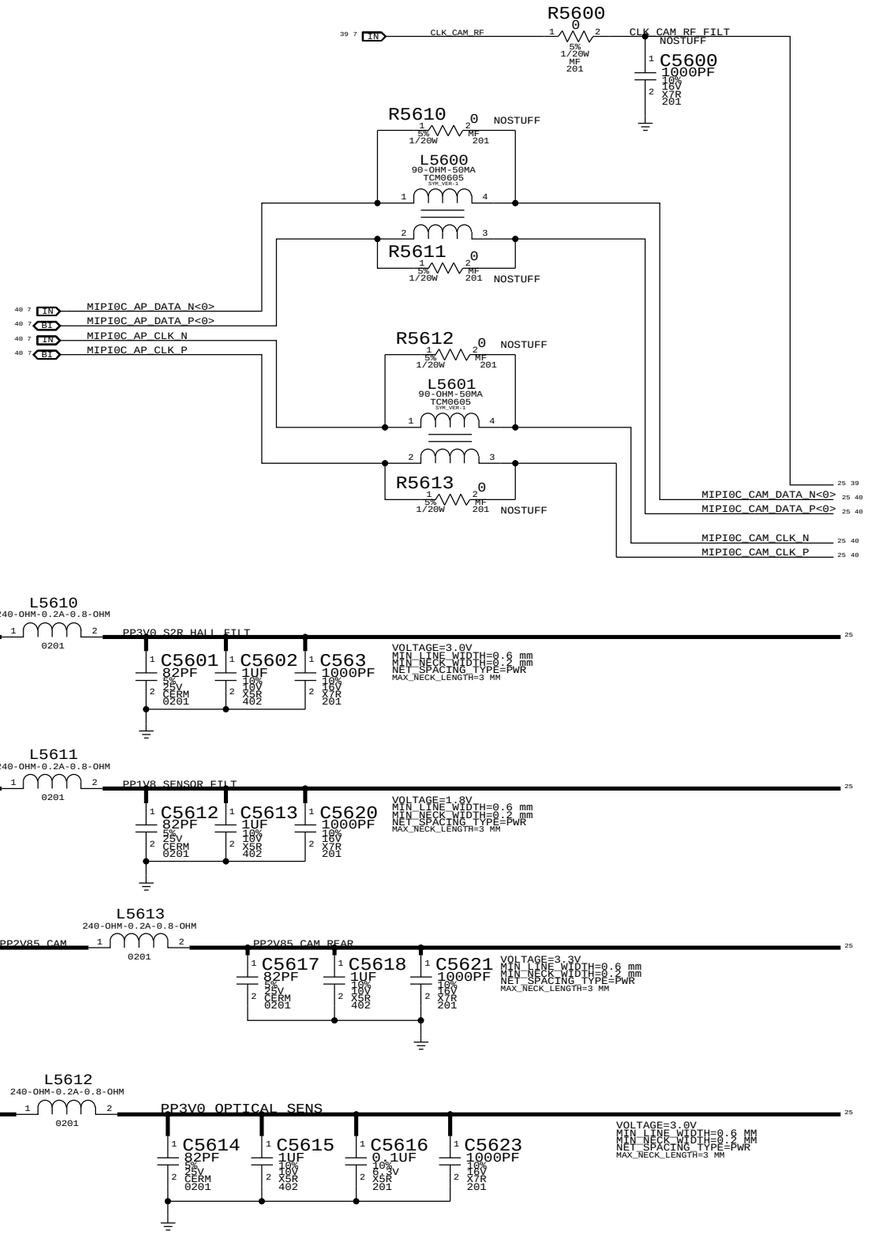
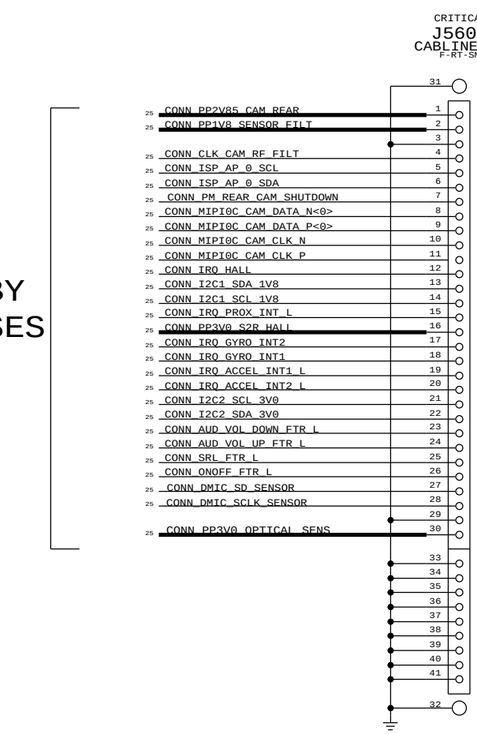


SENSOR PANEL CONNECTOR

CABLINE-CA CONNECTOR: 518S0787

CONNECTED BY
PG 54 ALIASES



SYNC_MASTER=MARK B. SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: SENSOR PANEL CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
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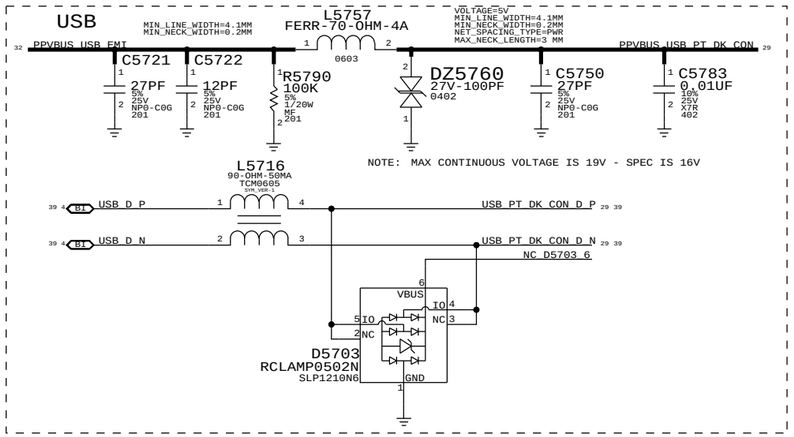
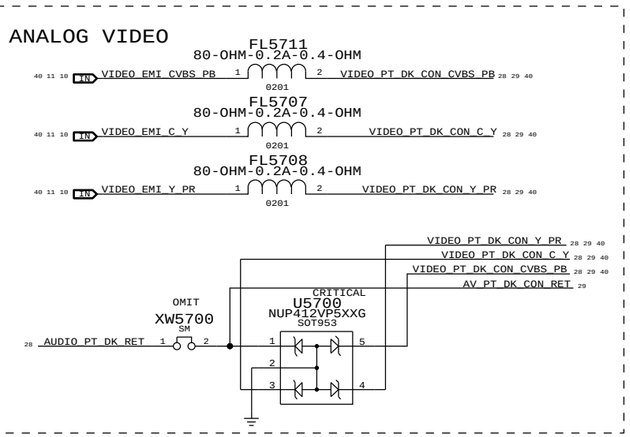
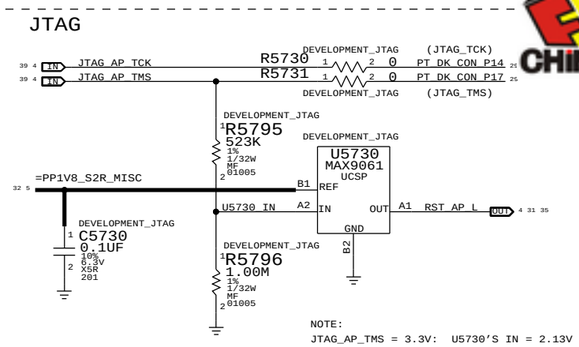
USB



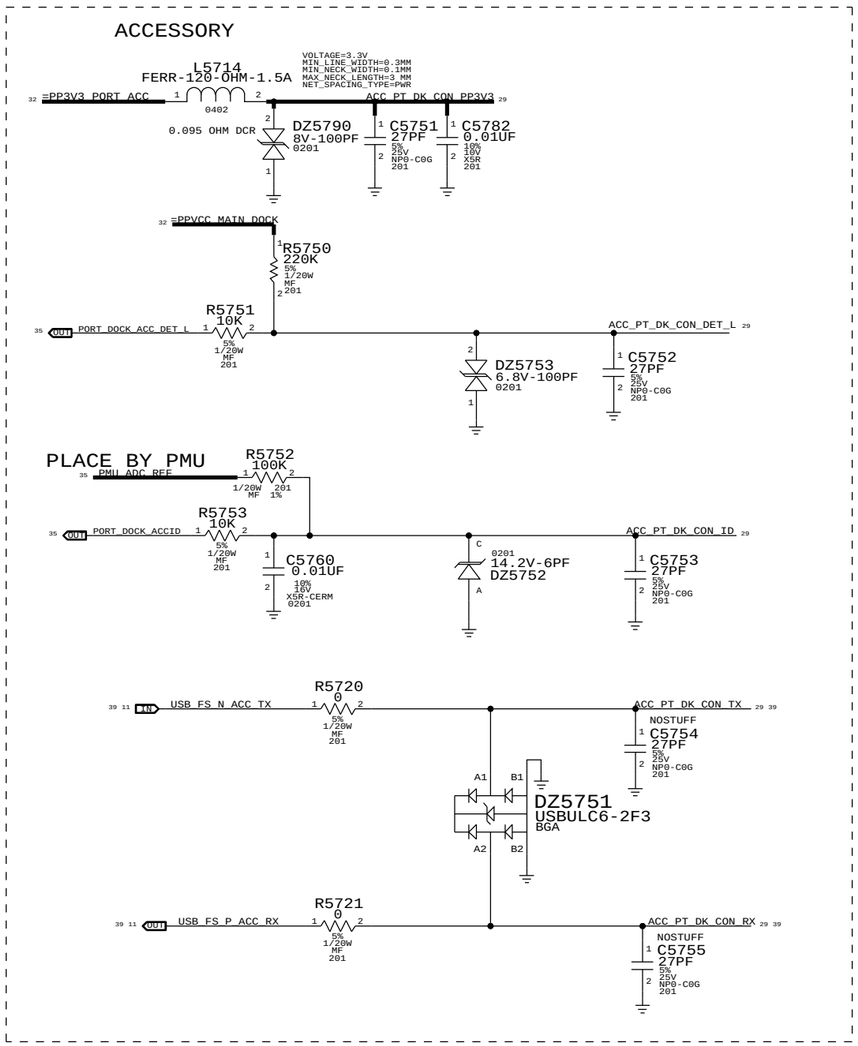
ANALOG VIDEO



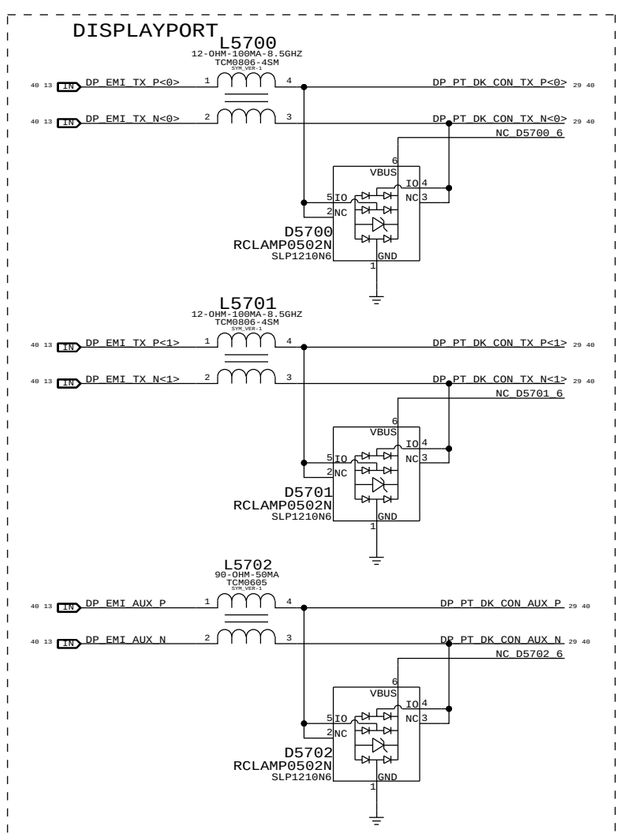
JTAG



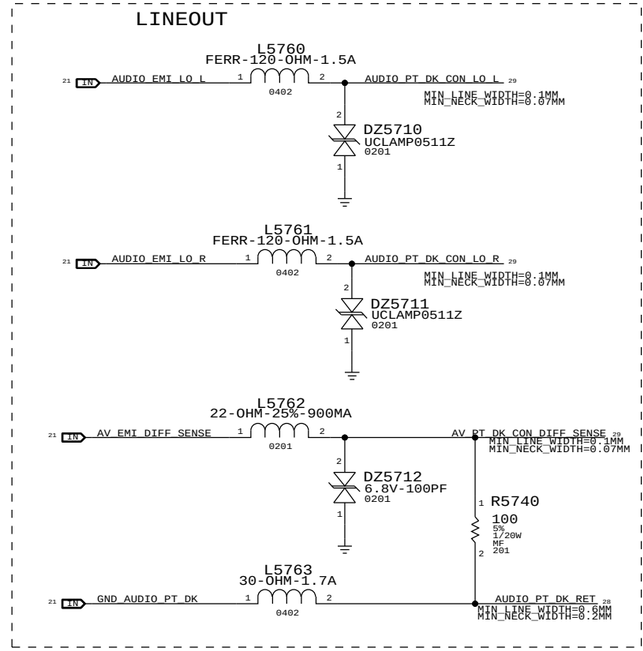
ACCESSORY



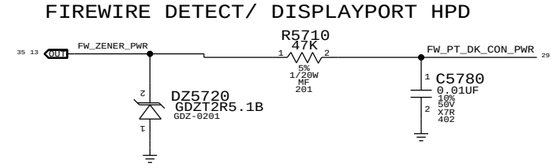
DISPLAYPORT



LINEOUT



FIREWIRE DETECT/ DISPLAYPORT HPD



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0090	377S0081		DZ5751	?
377S0111	377S0099		DZ5710,DZ5711	RADAR:8379541
377S0107	377S0066		DZ5700,DZ5701,DZ5702,DZ5703	RADAR:8289785
155S0625	155S0559		L5700,L5701	RADAR:8423156

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE: IO FLEX: DOCK COMPONENTS

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

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PN 516S0817 (PLUG - MALE)

CRITICAL

J5900
AXK844135WG
M-ST-SM

28	PPVBUS_USB_PT_DK_CON	2	1		
		4	3	USB_PT_DK_CON_D_P	BI 28 39
		6	5	USB_PT_DK_CON_D_N	BI 28 39
		8	7		
		10	9		
		12	11	DP_PT_DK_CON_TX_P<0>	IN 28 40
		14	13	DP_PT_DK_CON_TX_N<0>	IN 28 40
		16	15		
		18	17		
		20	19	DP_PT_DK_CON_TX_P<1>	IN 28 40
40 28	IN VIDEO_PT_DK_CON_CVBS_PB	22	21	DP_PT_DK_CON_TX_N<1>	IN 28 40
40 28	IN VIDEO_PT_DK_CON_C_Y	24	23		
40 28	IN VIDEO_PT_DK_CON_Y_PR	26	25	AV_PT_DK_CON_DIFF_SENSE	OUT 28
28	OUT ACC_PT_DK_CON_ID	28	27	AUDIO_PT_DK_CON_LO_L	IN 28
(DP_HPD) 28	OUT FW_PT_DK_CON_PWR	30	29	AUDIO_PT_DK_CON_LO_R	IN 28
28	ACC_PT_DK_CON_PP3V3	32	31	AV_PT_DK_CON_RET	OUT 28
		34	33	ACC_PT_DK_CON_DET_L	OUT 28
(JTAG_TCK) 28	IN PT_DK_CON_P14	36	35	DP_PT_DK_CON_AUX_P	BI 28 40
(JTAG_TMS) 28	IN PT_DK_CON_P17	38	37	DP_PT_DK_CON_AUX_N	BI 28 40
39 28	OUT ACC_PT_DK_CON_RX	40	39		
39 28	IN ACC_PT_DK_CON_TX	42	41	HOME_L	OUT 5 29 35
		44	43		

35 29 5 OUT HOME_L

DZ5750
6.8V-100PF
0201

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
IO FELX: B2B Connector

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

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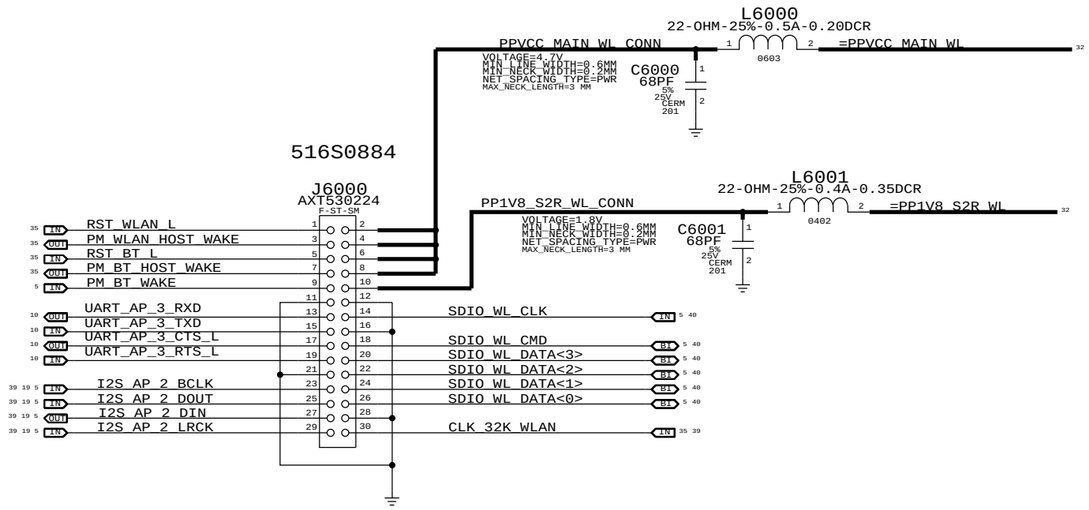
X23 WIFI/BT CONNECTOR



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: X23 WIFI/BT

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DRAWING NUMBER 051-8962 SIZE D

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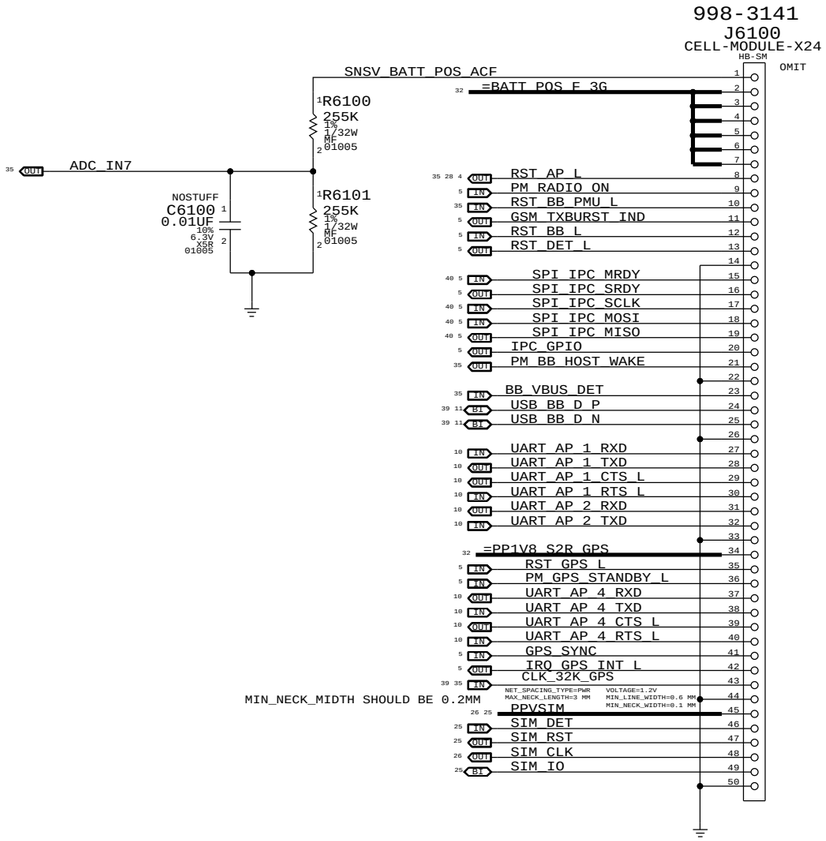
X24 CELLULAR/GPS CONNECTOR



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: X24 CELLULAR/GPS

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POWER CONN / ALIAS

LDO RAILS

PROGRAMMABLE ON/OFF

34 PP3V0_S2R_HALL
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_S2R_HALL (27)
→ =PP3V0_S2R_HALL_CHSW (23)

34 PP1V7_VA_VCP
MAKE_BASE=TRUE
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V7_VA_VCP (19)

34 PP3V0_VIDEO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_VIDEO_BUFFER (11)
→ =PP3V0_VIDEO_H4 (7)

34 PP3V0_OPTICAL
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_OPTICAL (5 26 27)

34 PP3V2_SD
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

34 PP3V3_ACC
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V3_PORT_ACC (28)

34 PP3V0_VIDEO_BUF
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_VIDEO_BUF (11)

34 PP3V2_S2R_USBMUX
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V2_S2R_USBMUX (11)

34 PP3V0_IO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_IO_H4 (7 9)
→ =PP3V0_IO_MISC (13)

34 PP2V85_CAM
MAKE_BASE=TRUE
VOLTAGE=2.85V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP2V85_CAM (26 27)

34 PP3V0_GRAPE
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_GRAPE (17 18)
→ =PP3V0_GRAPE_Z1 (18)
→ =PP3V0_GRAPE_Z2 (18)
→ =PP3V0_GRAPE_MARIO1 (17)

34 PP1V1
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
→ =PP1V1_PLL_H4 (4)
→ =PP1V1_MIPI_H4 (7)
→ =PP1V1_DPORT_H4 (7)
→ =PP1V1_USB_H4 (4)
MIN_NECK_MIDTH SHOULD BE 0.2MM → =PP1V1_MIPI_PLL_H4 (4)

34 PP1V8_ALWAYS
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_ALWAYS (5)

BUCK RAILS

34 PP1V2_SOC
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PPVDD_SOC_H4 (9)

34 PP1V2_CPU
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PPVDD_CPU_H4 (9)

34 PP1V2_S2R
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PP1V2_S2R_H4 (8)

34 PP1V8_S2R
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_S2R_H4 (8)
→ =PP1V8_S2R_WL (30)
→ =PP1V8_S2R_GPS (31)
→ =PP1V8_S2R_MISC (5 28)

34 PP1V8
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PP1V8_CAM (26)
→ =PP1V8_SENSOR (27)
→ =PP1V8_AUDIO (19)
→ =PP1V8_H4 (4 5 7 10 13)
→ =PP1V8_VDDIO18_H4 (8 9)
→ =PP1V8_MIPI_H4 (7)
→ =PP1V8_DPORT_H4 (7)

34 PP3V3_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PP3V3_NAND (12)
→ =PP3V3_USB_H4 (4)
→ =PP3V3_MLC_HI (36)
→ =PP3V3_LCD (16)
→ =PP3V3_NAND_H4 (10)

35 PPLED_OUT
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPLED_REG (16)

36 PP3V3_MLC_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V3_MLC (14 16)

34 PP1V2
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PP1V2_VDDQ_H4 (8)
→ =PP1V2_VDDIOD_H4 (8)
→ =PP1V2_HSIC_H4 (4)

GND
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=GND
MAX_NECK_LENGTH=5 MM

CHARGER MAIN

35 34 PPVCC_MAIN
MAKE_BASE=TRUE
VOLTAGE=4.7V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPVCC_MAIN_AUDIO (19 20)
→ =PPVCC_MAIN_WL (30)
→ =PPVCC_MAIN_DOCK (28)
→ =PPVCC_MAIN_LED (35)

BATTERY

37 34 PPBATT_VCC
MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=1.7 MM
→ =BATT_POS_F_3G (31)
→ =BATT_POS_CONN (33)

USB POWER INPUT

28 PPVBUS_USB_EMI
MAKE_BASE=TRUE
→ PPVBUS_USB_DCIN (34)

SYNC_MASTER=YOSH SYNC_DATE=N/A

PAGE TITLE
POWER: ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
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BRANCH
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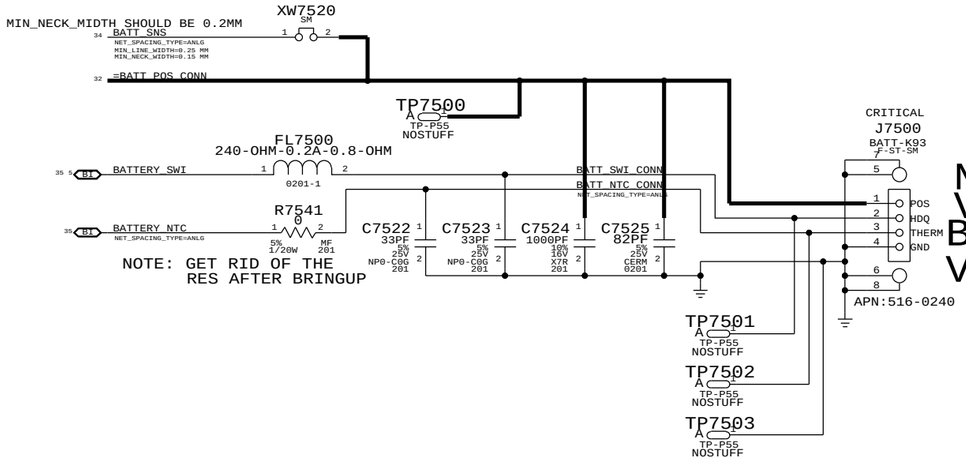
SHEET 32 OF 42



NOTE:
VERIFY PINOUT OF
BATTERY CONNECTOR
VERIFY MOUNTING CONN TO GND

SYNC_MASTER=YOSH SYNC_DATE=N/A

PAGE TITLE
POWER: BATTERY CONNECTOR

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0542	1	IC,PMU,ALISON,D1946A2,OTPXX,UFBGA292	U8100	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0392	197S0299		Y8138	ALT FOUNDRY

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

USB REVERSE VOLTAGE PROTECTION

NOTE: FOR NO BATTERY SITUATION

VCC_MAIN BYPASS
TOTAL CAPS = ~400UF
(DISTRIBUTED AND NO DE-RATING)

(PLACE ONE 1UF CAP AT EACH VDD INPUT)

NOTE: CONCERNED ABOUT ESR > 20MOHM

LDO BYPASS

ADDITIONAL DISTRIBUTED:
PP1V2: 30UF (NO DE-RATING)
PP1V8: 6UF (NO DE-RATING)

SYNC_MASTER=YOSH	SYNC_DATE=N/A
PAGE TITLE	POWER: PMU
Apple Inc.	DRAWING NUMBER 051-8962 SIZE D
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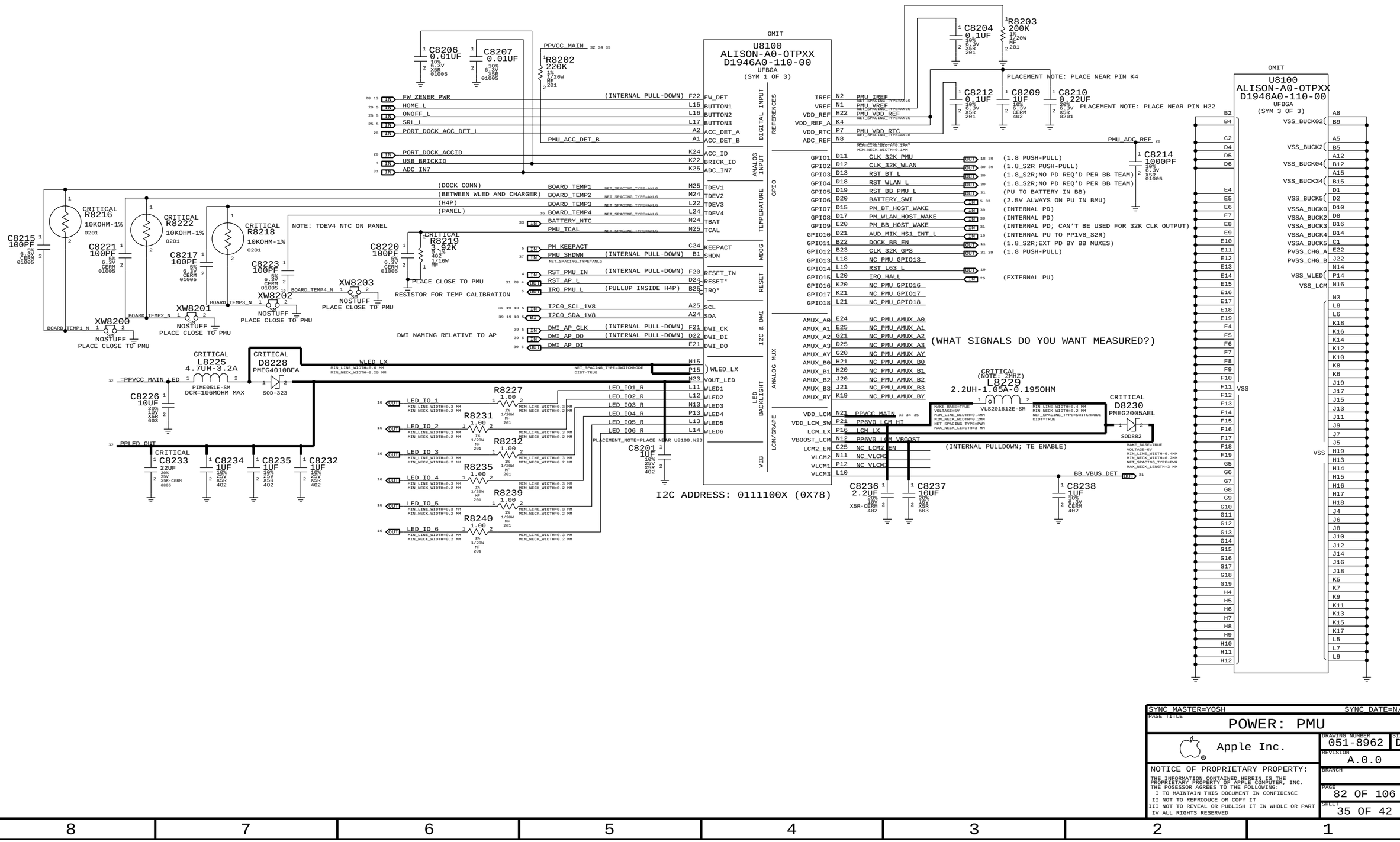
U8100
ALISON-A0-OTPXX
D1946A0-110-00
UFBGA
(SYM 1 OF 3)
OMIT
DIGITAL INPUT
REFERENCES
ANALOG INPUT
GPIO
TEMPERATURE
WDOG
RESET
I2C & DWI
ANALOG MUX
LED BACKLIGHT
LCM/GRAPE
VIB
FW_ZENER_PWR
HOME_L
ONOFF_L
SRL_L
PORT_DOCK_ACC_DET_L
PMU_ACC_DET_B
PORT_DOCK_ACCID
USB_BRICKID
ADC_IN7
(INTERNAL PULL-DOWN)
FW_DET
BUTTON1
BUTTON2
BUTTON3
ACC_DET_A
ACC_DET_B
ACC_ID
BRICK_ID
ADC_IN7
PPVCC_MAIN
C8206 0.01UF
C8207 0.01UF
R8202 220K
R8203 200K
C8204 0.1UF
C8212 0.1UF
C8209 1UF
C8210 0.22UF
PLACEMENT NOTE: PLACE NEAR PIN K4
PLACEMENT NOTE: PLACE NEAR PIN H22
PMU_ADC_REF
C8214 1000PF
(DOCK CONN)
(BETWEEN WLED AND CHARGER)
(H4P)
(PANEL)
BOARD_TEMP1
BOARD_TEMP2
BOARD_TEMP3
BOARD_TEMP4
BATTERY_NTC
PMU_TCAL
TDEV1
TDEV2
TDEV3
TDEV4
TBAT
TCAL
CRITICAL R8216 10KOHM-1%
CRITICAL R8222 10KOHM-1%
CRITICAL R8218 10KOHM-1%
C8215 100PF
C8221 100PF
C8217 100PF
C8223 100PF
NOTE: TDEV4 NTC ON PANEL
C8220 100PF
CRITICAL R8219 3.92K
RESISTOR FOR TEMP CALIBRATION
PLACE CLOSE TO PMU
XW8200 NOSTUFF
XW8201 NOSTUFF
XW8202 NOSTUFF
XW8203 NOSTUFF
PM_KEEPACT
PMU_SHDWN
SHDN
KEEPACT
RESET_IN
RST_PMU_IN
RST_AP_L
RESET*
IRQ_PMU_L
IRQ*
I2C0_SCL_1V8
I2C0_SDA_1V8
SCL
SDA
DWI_AP_CLK
DWI_AP_DO
DWI_AP_DI
DWI_CK
DWI_DI
DWI_DO
DWI NAMING RELATIVE TO AP
I2C ADDRESS: 0111100X (0X78)
GPIO1 CLK_32K_PMU (1.8 PUSH-PULL)
GPIO2 CLK_32K_WLAN (1.8_S2R PUSH-PULL)
GPIO3 RST_BT_L (1.8_S2R;NO PD REQ'D PER BB TEAM)
GPIO4 RST_WLAN_L (1.8_S2R;NO PD REQ'D PER BB TEAM)
GPIO5 RST_BB_PMU_L (PU TO BATTERY IN BB)
GPIO6 BATTERY_SWI (2.5V ALWAYS ON PU IN BMU)
GPIO7 PM_BT_HOST_WAKE (INTERNAL PD)
GPIO8 PM_WLAN_HOST_WAKE (INTERNAL PD)
GPIO9 PM_BB_HOST_WAKE (INTERNAL PD; CAN'T BE USED FOR 32K CLK OUTPUT)
GPIO10 AUD_MIK_HS1_INT_L (INTERNAL PU TO PP1V8_S2R)
GPIO11 DOCK_BB_EN (1.8_S2R;EXT PD BY BB MUXES)
GPIO12 CLK_32K_GPS (1.8 PUSH-PULL)
GPIO13 NC_PMU_GPIO13
GPIO14 RST_L63_L
GPIO15 IRQ_HALL (EXTERNAL PU)
GPIO16 NC_PMU_GPIO16
GPIO17 NC_PMU_GPIO17
GPIO18 NC_PMU_GPIO18
AMUX_A0 NC_PMU_AMUX_A0
AMUX_A1 NC_PMU_AMUX_A1
AMUX_A2 NC_PMU_AMUX_A2
AMUX_A3 NC_PMU_AMUX_A3
AMUX_AY NC_PMU_AMUX_AY
AMUX_B0 NC_PMU_AMUX_B0
AMUX_B1 NC_PMU_AMUX_B1
AMUX_B2 NC_PMU_AMUX_B2
AMUX_B3 NC_PMU_AMUX_B3
AMUX_BY NC_PMU_AMUX_BY
(WHAT SIGNALS DO YOU WANT MEASURED?)
VDD_LCM PPVCC_MAIN
VDD_LCM_SW PP6V0_LCM_HI
LCM_LX LCM_LX
VBOOST_LCM PP6V0_LCM_VBOOST
LCM2_EN NC_LCM2_EN
VLCM2 NC_VLCM2
VLCM1 NC_VLCM1
VLCM3
(INTERNAL PULLDOWN; TE ENABLE)
BB_VBUS_DET
C8236 2.2UF
C8237 10UF
C8238 1UF
CRITICAL L8225 4.7UH-3.2A
CRITICAL D8228 PMEG4010BEA
WLED_LX
=PPVCC_MAIN_LED
PPLED_OUT
C8226 10UF
C8233 22UF
C8234 1UF
C8235 1UF
C8232 1UF
LED_IO1_R
LED_IO2_R
LED_IO3_R
LED_IO4_R
LED_IO5_R
LED_IO6_R
LED_IO 1
LED_IO 2
LED_IO 3
LED_IO 4
LED_IO 5
LED_IO 6
R8227 1.00
R8231 1.00
R8232 1.00
R8235 1.00
R8239 1.00
R8240 1.00
C8201 1UF
PLACEMENT_NOTE=PLACE NEAR U8100.N23
CRITICAL L8229 2.2UH-1.05A-0.195OHM
VLS201612E-SM
CRITICAL D8230 PMEG2005AEL
SOD882
VSS_BUCK02
VSS_BUCK2
VSS_BUCK04
VSS_BUCK34
VSS_BUCK5
VSSA_BUCK0
VSSA_BUCK2
VSSA_BUCK3
VSSA_BUCK4
VSSA_BUCK5
PVSS_CHG_A
PVSS_CHG_B
VSS_WLED
VSS_LCM
VSS
SYNC_MASTER=YOSH
SYNC_DATE=N/A
PAGE TITLE
POWER: PMU
Apple Inc.
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SIZE D
REVISION A.0.0
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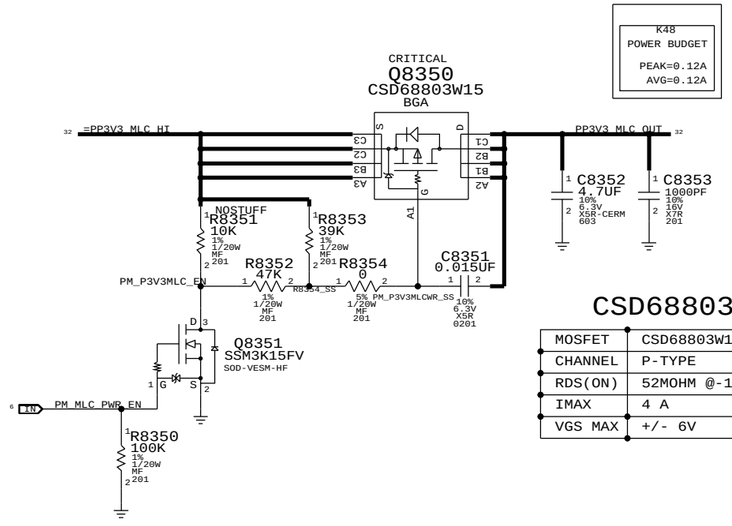

CSD68803

MOSFET	CSD68803W15
CHANNEL	P-TYPE
RDS(ON)	52MOHM @-1.8V
IMAX	4 A
VGS MAX	+/- 6V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0972	376S0612		Q8351	RADAR:8537160

SYNC_MASTER=YOSH SYNC_DATE=N/A

PAGE TITLE
POWER: 3.3V MLC & 1.2V VR

Apple Inc.

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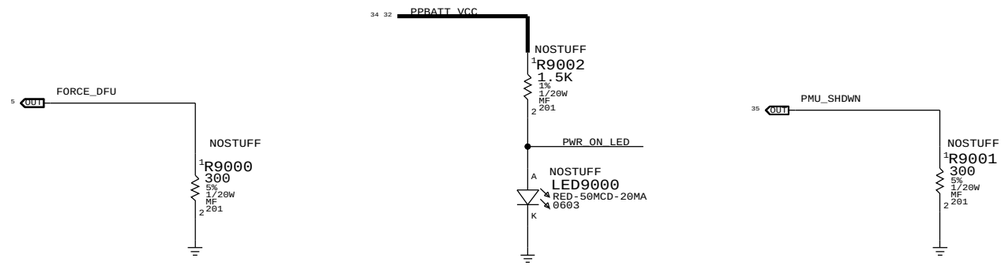
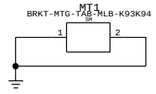
DEBUG RESET ACCESS

PLACE OUTSIDE OF CAN?



LEFT AND RIGHT MOUNTING TABS



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE: DEBUG AND MISC

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BRANCH:

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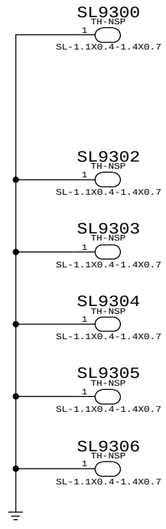
PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
FCT/ICT TEST/BRACKETS

Apple Inc.

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
L63	CLK_50S	CLK	CLK_32K_PMU	18 35
L102	CLK_50S	CLK	CLK_32K_WLAN	30 35
L61	CLK_50S	CLK	CLK_32K_GPS	31 35
L68	CLK_50S	CLK	CLK_CAM_FF	7 26
L80	CLK_50S	CLK	CLK_CAM_FF_FILT	
L95	CLK_50S	CLK	CLK_CAM_FF_CONN	25 26
L96	CLK_50S	CLK	CLK_CAM_RF	7 27
L94	CLK_50S	CLK	CLK_CAM_RF_FILT	25 27
L130	CLK_50S	CLK	I2S_AP_0_MCK	5
L131	CLK_50S	CLK	I2S_AP_0_MCK_R	5 19
L157	CLK_50S	CLK	CLK_CAM_FF_R	7
L158	CLK_50S	CLK	CLK_CAM_RF_R	7

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
L60	NAND_50S	NAND	F0AD<7..0>	6 12
L45	NAND_50S	NAND	F0CE0_L	6 12
L48	NAND_50S	NAND	F0CE1_L	6 12
L67	NAND_50S	NAND	F0CE2_L	6 12
L46	NAND_50S	NAND	F0CE3_L	6 12
L163	NAND_50S	NAND	F0CE4_L	6 12
L164	NAND_50S	NAND	F0CE5_L	6 12
L166	NAND_50S	NAND	F0CE6_L	6 12
L165	NAND_50S	NAND	F0CE7_L	6 12
L41	NAND_50S	NAND	F0CLE	6 12
L42	NAND_50S	NAND	F0ALE	6 12
L43	NAND_50S	NAND	F0RE_L	6 12
L44	NAND_50S	NAND	F0WE_L	6 12
L37	NAND_50S	NAND	F0WP_L	
L49	NAND_50S	NAND	F1AD<7..0>	6 12
L61	NAND_50S	NAND	F1CE0_L	6 12
L62	NAND_50S	NAND	F1CE1_L	6 12
L63	NAND_50S	NAND	F1CE2_L	6 12
L64	NAND_50S	NAND	F1CE3_L	6 12
L167	NAND_50S	NAND	F1CE4_L	6 12
L168	NAND_50S	NAND	F1CE5_L	6 12
L169	NAND_50S	NAND	F1CE6_L	6 12
L170	NAND_50S	NAND	F1CE7_L	6 12
L65	NAND_50S	NAND	F1CLE	6 12
L66	NAND_50S	NAND	F1ALE	6 12
L67	NAND_50S	NAND	F1RE_L	6 12
L68	NAND_50S	NAND	F1WE_L	6 12
L69	NAND_50S	NAND	F1WP_L	
L105	NAND_50S	NAND	F2AD<7..0>	
L103	NAND_50S	NAND	F2CE0_L	
L106	NAND_50S	NAND	F2CE1_L	
L108	NAND_50S	NAND	F2CE2_L	
L107	NAND_50S	NAND	F2CE3_L	
L109	NAND_50S	NAND	F2CLE	
L110	NAND_50S	NAND	F2ALE	
L111	NAND_50S	NAND	F2RE_L	
L112	NAND_50S	NAND	F2WE_L	
L113	NAND_50S	NAND	F2WP_L	
L114	NAND_50S	NAND	F3AD<7..0>	
L151	NAND_50S	NAND	F3CE0_L	
L152	NAND_50S	NAND	F3CE1_L	
L153	NAND_50S	NAND	F3CE2_L	
L154	NAND_50S	NAND	F3CE3_L	
L155	NAND_50S	NAND	F3CLE	
L120	NAND_50S	NAND	F3ALE	
L121	NAND_50S	NAND	F3RE_L	
L122	NAND_50S	NAND	F3WE_L	
L123	NAND_50S	NAND	F3WP_L	

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
H16		JTAG	JTAG_AP_TCK	4 28
H15		JTAG	JTAG_AP_TMS	4 28
H14		JTAG	JTAG_AP_TDI	4 10
H13		JTAG	JTAG_AP_TDO	4 10
H20		JTAG	JTAG_AP_TRST_L	4 10

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I1	I2C_50S	I2C	I2C1_SDA_1V8	5 25
I2	I2C_50S	I2C	I2C1_SCL_1V8	5 25
I8	I2C_50S	I2C	I2C0_SDA_1V8	5 10 19 35
I4	I2C_50S	I2C	I2C0_SCL_1V8	5 10 19 35
I61	I2C_50S	I2C	I2C2_SDA_3V0	5 25 26
I62	I2C_50S	I2C	I2C2_SCL_3V0	5 25 26
I98	I2C_50S	I2C	ISP_AP_0_SCL	7 25
I99	I2C_50S	I2C	ISP_AP_0_SDA	7 25
I100	I2C_50S	I2C	ISP_AP_1_SCL	7 26
I101	I2C_50S	I2C	ISP_AP_1_SDA	7 26
I105	I2C_50S	I2C	I2C2_SCL_3V0_ALS	25 26
I106	I2C_50S	I2C	I2C2_SDA_3V0_ALS	25 26
I124	I2C_50S	I2C	ISP_CAM_1_SCL	25 26
I125	I2C_50S	I2C	ISP_CAM_1_SDA	25 26

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I92		CRYSTAL	XTAL_24M_I	4
I90		CRYSTAL	XTAL_24M_O	4
I89		CRYSTAL	24M_O	4

VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I136		VREF	PPVREF_DDR0_CA	8
I137		VREF	PPVREF_DDR0_DQ	8
I138		VREF	PPVREF_DDR1_CA	8
I139		VREF	PPVREF_DDR1_DQ	8

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
L5	USB_90D	USB	USB_D_P	4 28
L6	USB_90D	USB	USB_D_N	4 28
L7	USB_90D	USB	USB_PT_DK_CON_D_P	28 29
L8	USB_90D	USB	USB_PT_DK_CON_D_N	28 29
L82	USB_90D	USB	USB_BB_D_P	11 31
L83	USB_90D	USB	USB_BB_D_N	11 31
L84	USB_90D	USB	USB_FS_D_P	4 11
L85	USB_90D	USB	USB_FS_D_N	4 11
L127	USB_90D	USB	USB_FS_N_ACC_TX	11 28
L128	USB_90D	USB	USB_FS_P_ACC_RX	11 28
L171	USB_90D	USB	ACC_PT_DK_CON_TX	28 29
L172	USB_90D	USB	ACC_PT_DK_CON_RX	28 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
L140	I2S_50S	I2S	I2S_AP_0_BCLK	5 19
L141	I2S_50S	I2S	I2S_AP_0_LRCK	5 19
L142	I2S_50S	I2S	I2S_AP_0_DIN	5 19
L143	I2S_50S	I2S	I2S_AP_0_DOUT	5 19
L160	I2S_50S	I2S	L63_ASP_SDOUT	19
L144	I2S_50S	I2S	I2S_AP_2_BCLK	5 19 30
L145	I2S_50S	I2S	I2S_AP_2_LRCK	5 19 30
L146	I2S_50S	I2S	I2S_AP_2_DIN	5 19 30
L147	I2S_50S	I2S	I2S_AP_2_DOUT	5 19 30
L150	I2S_50S	I2S	L63_VSP_SDOUT	19
L148	I2S_50S	I2S	I2S_AP_3_BCLK	5 19
L149	I2S_50S	I2S	I2S_AP_3_LRCK	5 19
L190	I2S_50S	I2S	I2S_AP_3_DIN	5 19
L192	I2S_50S	I2S	I2S_AP_3_DOUT	5 19
L191	I2S_50S	I2S	L63_XSP_SDOUT	19

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I195		DWI	DWI_AP_CLK	5 35
I196		DWI	DWI_AP_DI	5 35
I194		DWI	DWI_AP_DO	5 35

SYNC_MASTER=MIKE SYNC_DATE=N/A

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ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I213	VID_50S	ANALOG_VIDEO	DAC_AP_OUT1 7 11
I214	VID_50S	ANALOG_VIDEO	DAC_AP_OUT2 7 11
I215	VID_50S	ANALOG_VIDEO	DAC_AP_OUT3 7 11
I232	VID_50S	ANALOG_VIDEO	BUF_C_Y 11
I233	VID_50S	ANALOG_VIDEO	BUF_CVBS_PB 11
I234	VID_50S	ANALOG_VIDEO	BUF_Y_PR 11
I219	VID_50S	ANALOG_VIDEO	VIDEO_EMI_CVBS_PB 10 11 28
I220	VID_50S	ANALOG_VIDEO	VIDEO_EMI_C_Y 10 11 28
I221	VID_50S	ANALOG_VIDEO	VIDEO_EMI_Y_PR 10 11 28
I222	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_CVBS_PB 28 29
I223	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_C_Y 28 29
I224	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_Y_PR 28 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I91	MIPI_100D	MIPI	MIPID_AP_DATA_P<0> 7 14
I92	MIPI_100D	MIPI	MIPID_AP_DATA_N<0> 7 14
I93	MIPI_100D	MIPI	MIPID_AP_DATA_P<1> 7 14
I94	MIPI_100D	MIPI	MIPID_AP_DATA_N<1> 7 14
I95	MIPI_100D	MIPI	MIPID_AP_DATA_P<2> 7 14
I96	MIPI_100D	MIPI	MIPID_AP_DATA_N<2> 7 14
I97	MIPI_100D	MIPI	MIPID_AP_DATA_P<3> 7 14
I274	MIPI_100D	MIPI	MIPID_AP_DATA_N<3> 7 14
I97	MIPI_100D	MIPI	MIPID_AP_CLK_P 7 14
I98	MIPI_100D	MIPI	MIPID_AP_CLK_N 7 14
I831	MIPI_100D	MIPI	MIPI0C_AP_DATA_P<0> 7 27
I832	MIPI_100D	MIPI	MIPI0C_AP_DATA_N<0> 7 27
I833	MIPI_100D	MIPI	MIPI0C_AP_CLK_P 7 27
I834	MIPI_100D	MIPI	MIPI0C_AP_CLK_N 7 27
I834	MIPI_100D	MIPI	MIPI0C_CAM_DATA_P<0> 25 27
I834	MIPI_100D	MIPI	MIPI0C_CAM_DATA_N<0> 25 27
I834	MIPI_100D	MIPI	MIPI0C_CAM_CLK_P 25 27
I834	MIPI_100D	MIPI	MIPI0C_CAM_CLK_N 25 27
I834	MIPI_100D	MIPI	MIPI1C_AP_DATA_P<0> 7 26
I834	MIPI_100D	MIPI	MIPI1C_AP_DATA_N<0> 7 26
I834	MIPI_100D	MIPI	MIPI1C_AP_CLK_P 7 26
I834	MIPI_100D	MIPI	MIPI1C_AP_CLK_N 7 26
I835	MIPI_100D	MIPI	MIPI1C_CAM_DATA_P<0> 25 26
I835	MIPI_100D	MIPI	MIPI1C_CAM_DATA_N<0> 25 26
I836	MIPI_100D	MIPI	MIPI1C_CAM_CLK_P 25 26
I836	MIPI_100D	MIPI	MIPI1C_CAM_CLK_N 25 26

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	4:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I1476	LVDS_100D	LVDS	LVDS_DATA_P<2..0> 14 16
I1476	LVDS_100D	LVDS	LVDS_DATA_N<2..0> 14 16
I1245	LVDS_100D	LVDS	LVDS_DATA_CONN_P<2..0> 16
I1245	LVDS_100D	LVDS	LVDS_DATA_CONN_N<2..0> 16
I1476	LVDS_100D	LVDS	LVDS_CLK_P 14 16
I1476	LVDS_100D	LVDS	LVDS_CLK_N 14 16
I1245	LVDS_100D	LVDS	LVDS_CLK_CONN_P 16
I1245	LVDS_100D	LVDS	LVDS_CLK_CONN_N 16

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I247	DP_100D	DP	DP_AP_TX_P<0> 7 10 13
I249	DP_100D	DP	DP_AP_TX_N<0> 7 10 13
I248	DP_100D	DP	DP_AP_TX_P<1> 7 10 13
I250	DP_100D	DP	DP_AP_TX_N<1> 7 10 13
I251	DP_100D	DP	DP_AP_AUX_P 7 13
I252	DP_100D	DP	DP_AP_AUX_N 7 13
I273	DP_100D	DP	DP_EMI_TX_P<0> 13 28
I274	DP_100D	DP	DP_EMI_TX_N<0> 13 28
I275	DP_100D	DP	DP_EMI_TX_P<1> 13 28
I276	DP_100D	DP	DP_EMI_TX_N<1> 13 28
I277	DP_100D	DP	DP_EMI_AUX_P 13 28
I278	DP_100D	DP	DP_EMI_AUX_N 13 28
I827	DP_100D	DP	DP_PT_DK_CON_TX_P<0> 28 29
I826	DP_100D	DP	DP_PT_DK_CON_TX_N<0> 28 29
I824	DP_100D	DP	DP_PT_DK_CON_TX_P<1> 28 29
I831	DP_100D	DP	DP_PT_DK_CON_TX_N<1> 28 29
I830	DP_100D	DP	DP_PT_DK_CON_AUX_P 28 29
I832	DP_100D	DP	DP_PT_DK_CON_AUX_N 28 29

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I1587	AUDIO	AUDIO	LEFT_CH_OUT_P 19 20
I1588	AUDIO	AUDIO	LEFT_CH_OUT_REF 19 20
I1589	AUDIO	AUDIO	LEFT_CH_P 20
I1590	AUDIO	AUDIO	SSM2375_L_IN_P 20
I1591	AUDIO	AUDIO	SSM2375_L_IN_N 20
I1592	AUDIO	AUDIO	RIGHT_CH_OUT_P 19 20
I1593	AUDIO	AUDIO	RIGHT_CH_OUT_REF 19 20
I1594	AUDIO	AUDIO	RIGHT_CH_P 20
I1595	AUDIO	AUDIO	SSM2375_R_IN_P 20
I1596	AUDIO	AUDIO	SSM2375_R_IN_N 20
I1371	AUDIO	AUDIO	EXT_MIC_P 19 23
I1372	AUDIO	AUDIO	EXT_MIC_REF 19 23

SDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SDIO_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SDIO	*	*	2:1_SPACING
SDIO_CLK	*	*	4:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I1506	SDIO_50S	SDIO_CLK	SDIO_WL_CLK 5 30
I1281	SDIO_50S	SDIO_CLK	SDIO_WL_CLK_R
I1211	SDIO_50S	SDIO	SDIO_WL_CMD 5 30
I1507	SDIO_50S	SDIO	SDIO_WL_DATA<3..0> 5 30

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I1356	SPI_50S	SPI	SPI_GRAPE_MISO 5 17
I1358	SPI_50S	SPI	SPI_GRAPE_MOSI 5 17
I1357	SPI_50S	SPI	SPI_GRAPE_SCLK 5 17
I1767	SPI_50S	SPI	SPI_GRAPE_CS_L 5 17
I1356	SPI_50S	SPI	SPI_IPC_MISO 5 31
I1358	SPI_50S	SPI	SPI_IPC_MOSI 5 31
I1357	SPI_50S	SPI	SPI_IPC_SCLK 5 31
I1767	SPI_50S	SPI	SPI_IPC_MRDY 5 31

SYNC_MASTER=MIKE SYNC_DATE=N/A

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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,BOTTOM	NO_TYPE,BGA,BGA06-06	MM	15.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES
45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2,ISL3,ISL8,ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4,ISL5,ISL6,ISL7	Y	0.060 MM	0.060 MM	3.0 MM		
45_OHM_SE	*	N	0.060 MM	0.060 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

50 OHMS - CLEAR ON LAYER 2 AND 5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP	Y	0.240 MM	0.240 MM	3.0 MM		
50_OHM_SE	ISL4	Y	0.060 MM	0.060 MM	3.0 MM		

50 OHMS - CLEAR ON TOP AND BOTTOM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL2,ISL9	Y	0.090 MM	0.090 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES
100 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP,BOTTOM	Y	0.076 MM	0.076 MM		0.210 MM	0.210 MM
100_OHM_DIFF	N	Y	0.057 MM	0.057 MM	=STANDARD	0.300 MM	0.300 MM

90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL3,ISL8,ISL9	Y	0.054 MM	0.054 MM	=STANDARD	0.200 MM	0.100 MM
90_OHM_DIFF	ISL4,ISL5,ISL6,ISL7	Y	0.060 MM	0.060 MM	=STANDARD	0.200 MM	0.100 MM

AUDIO PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	

0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.060 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.090 MM	?
2:1_SPACING	*	0.120 MM	?
2.5:1_SPACING	*	0.150 MM	?
3:1_SPACING	*	0.180 MM	?
4:1_SPACING	*	0.240 MM	?
5:1_SPACING	*	0.300 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP,BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

SYNC_MASTER=MIKE SYNC_DATE=N/A

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