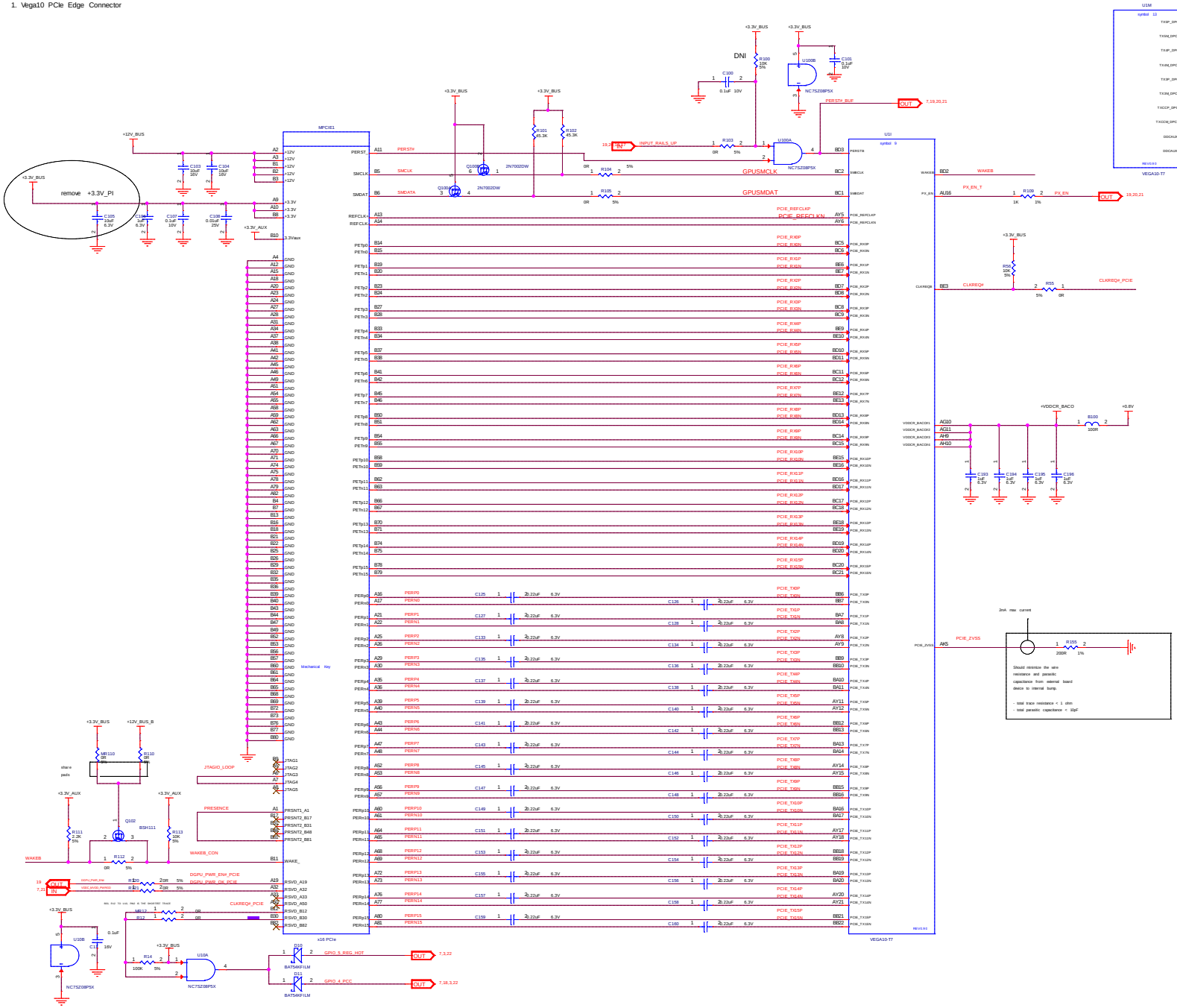
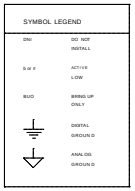
1. Vega10 PCIe Edge Connector





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3	Vega10 - GPIO, EXTRA
4	Vega10 - DFTIO, FREE, HPM_DAP, CRACKMON
5	Vega10 - TMDPAB 1xDP, 1xHDMI & +5V VESA
6	Vega10 - TMDPEF 2xDP
7	Control - VDDC / MVDD
8	Reg - VDDCR_SOC PHASES I and VII
9	Reg - VDDCR_SOC PHASES V and XI
10	Reg - VDDCR_SOC PHASES III and IX
11	Reg - VDDCR_SOC PHASES IV and X
12	Reg - VDDCR_SOC PHASES II and VIII
13	Reg - VDDCR_SOC PHASES VI and XII
14	Reg - VDDCR_IO
15	Reg - VDDCR_MEM and VPP
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Size	Document Description	Rev
Custom	PCIE	2.0

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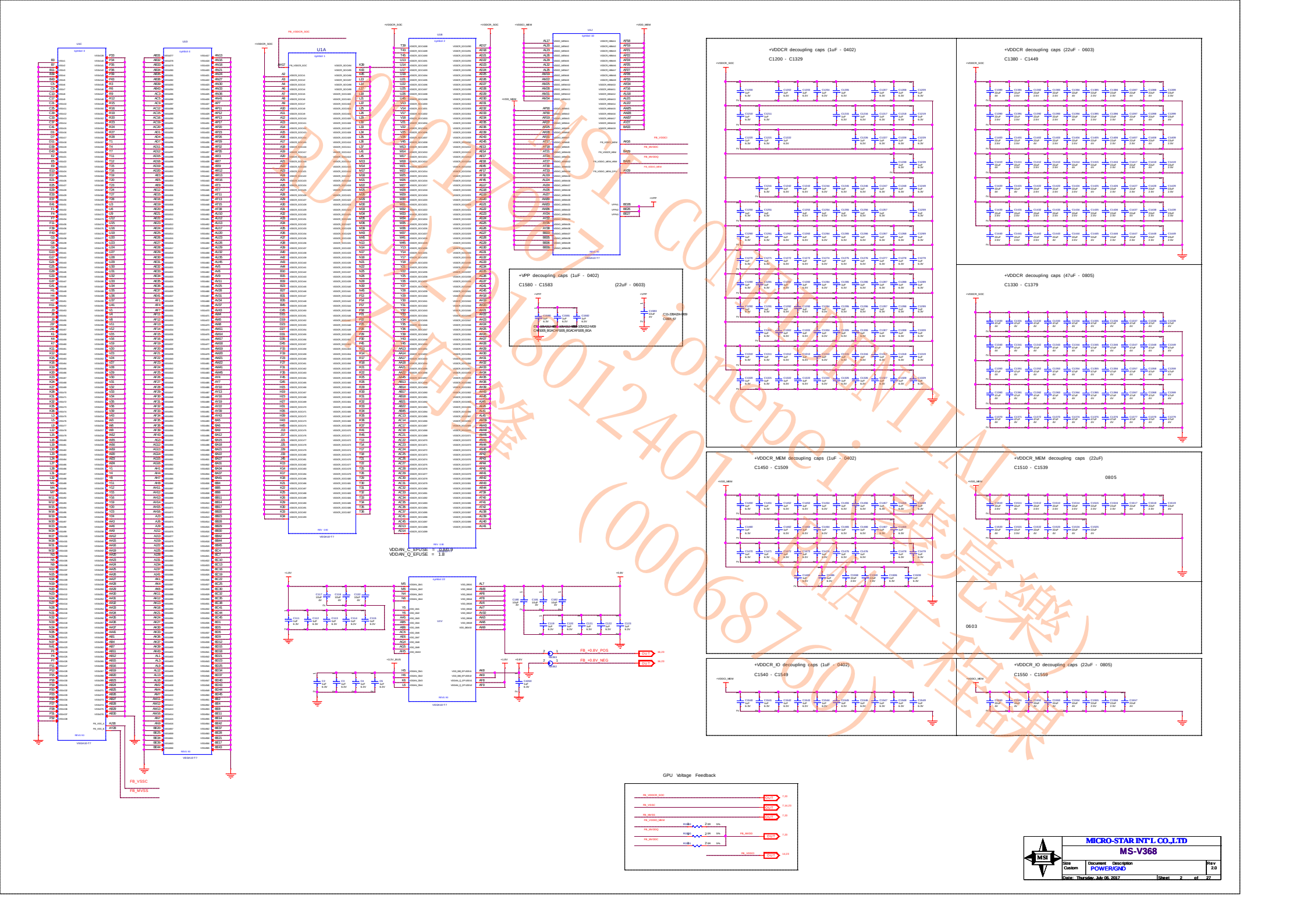
+VDDCR decoupling caps (1uF - 0402)
C1200 - C1329
+VDDCR decoupling caps (22uF - 0603)
C1380 - C1449
+VDDCR decoupling caps (47uF - 0805)
C1330 - C1379
+VPP decoupling caps (1uF - 0402)
C1580 - C1583
(22uF - 0603)
+VDDCR_MEM decoupling caps (1uF - 0402)
C1450 - C1509
+VDDCR_MEM decoupling caps (22uF)
C1510 - C1539
0805
0603
+VDDCR_IO decoupling caps (1uF - 0402)
C1540 - C1549
+VDDCR_IO decoupling caps (22uF - 0805)
C1550 - C1559
GPU Voltage Feedback
MICRO-STAR INT'L CO.,LTD
MS-V368
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Custom
Document Description
POWER/GND
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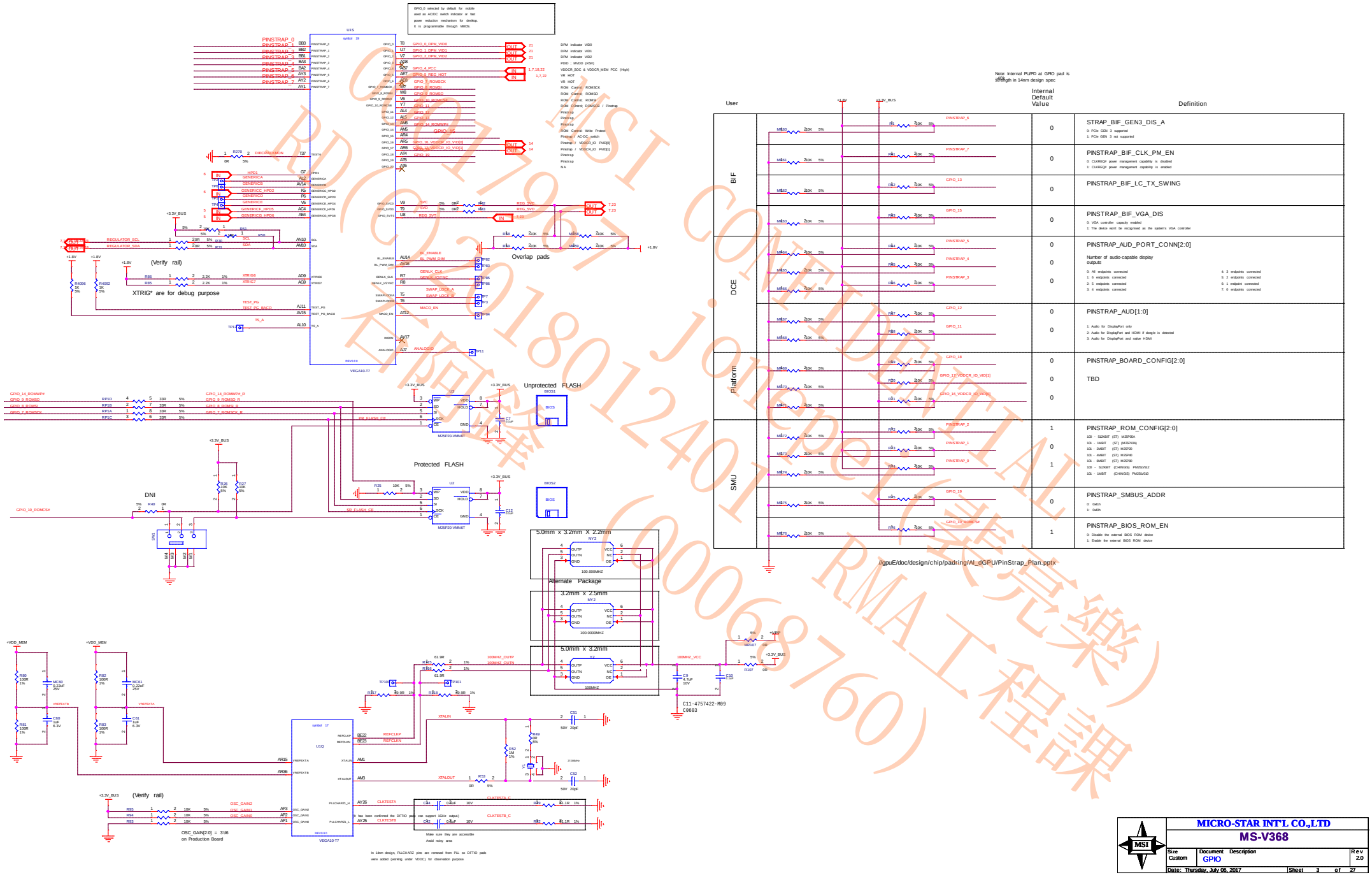
GPIO_0 selected by default for mobile used as AC/DC switch indicator or fast power reduction mechanism for desktop. It is programmable through VBIOS.
PINSTRAP_0
PINSTRAP_1
PINSTRAP_2
PINSTRAP_3
PINSTRAP_4
PINSTRAP_5
PINSTRAP_6
PINSTRAP_7
GPIO_0_DPM_VID0
GPIO_1_DPM_VID1
GPIO_2_DPM_VID2
GPIO_4_PCC
GPIO_5_REG_HOT
GPIO_7_ROMSCK
GPIO_8_ROMSI
GPIO_9_ROMSO
GPIO_10_ROMCS#
GPIO_11
GPIO_12
GPIO_13
GPIO_14_ROMWP#
GPIO_15
GPIO_16_VDDCR_IO_VID[0]
GPIO_17_VDDCR_IO_VID[1]
GPIO_18
GPIO_19
DPM_indicator_VID0
DPM_indicator_VID1
DPM_indicator_VID2
PGD_/_WVID_(RSV)
VDDCR_SOC_&_VDDCR_MEM_PCC_(Hi/gh)
VR_HOT
ROM_Control_:_ROMSCK
ROM_Control_:_ROMSO
ROM_Control_:_ROMCS#
ROM_Control_:_ROMSCLK_/_Pinstrap
Pinstrap_Protect_ROM_Control_Write
Pinstrap_/_AC-DC_switch
Pinstrap_/_VDDCR_IO_PVID[0]
Pinstrap_/_VDDCR_IO_PVID[1]
N.A
Note: Internal PU/PD at GPIO pad is strength in 14nm design spec
Internal Default Value
Definition
User
BIF
DCE
Platform
SMU
STRAP_BIF_GEN3_DIS_A
0: PCIe GEN 3 supported
1: PCIe GEN 3 not supported
PINSTRAP_BIF_CLK_PM_EN
0: CLKREQ# power management capability is disabled
1: CLKREQ# power management capability is enabled
PINSTRAP_BIF_LC_TX_SWING
PINSTRAP_BIF_VGA_DIS
0: VGA controller capacity enabled
1: The device won't be recognised as the system's VGA controller
PINSTRAP_AUD_PORT_CONN[2:0]
Number of audio-capable display outputs
0: All endpoints connected
1: 6 endpoints connected
2: 5 endpoints connected
3: 4 endpoints connected
4: 3 endpoints connected
5: 2 endpoints connected
6: 1 endpoint connected
7: 0 endpoints connected
PINSTRAP_AUD[1:0]
1: Audio for DisplayPort only
2: Audio for DisplayPort and HDMI if dongle is detected
3: Audio for DisplayPort and native HDMI
PINSTRAP_BOARD_CONFIG[2:0]
TBD
PINSTRAP_ROM_CONFIG[2:0]
100 - S12KBIT (ST) M25P05A
101 - 1MBIT (ST) (M25P10A)
101 - 2MBIT (ST) M25P20
101 - 4MBIT (ST) M25P40
101 - 8MBIT (ST) M25P80
100 - S12KBIT (CHINGS) PN25LV512
101 - 1MBIT (CHINGS) PN25LV010
PINSTRAP_SMBUS_ADDR
0: 0x1h
1: 0x0h
PINSTRAP_BIOS_ROM_EN
0: Disable the external BIOS ROM device
1: Enable the external BIOS ROM device
//gpuE/doc/design/chip/padring/AI_dGPU/PinStrap_Plan.pptx
(Verify rail)
XTRIG* are for debug purpose
Overlap pads
Unprotected FLASH
Protected FLASH
DNI
Alternate Package
5.0mm x 3.2mm X 2.2mm
3.2mm x 2.5mm
5.0mm x 3.2mm
(Verify rail)
OSC_GAIN[2:0] = 3'd6 on Production Board
Make sure they are accessible
Avoid noisy area
In 14nm design, PLLCHAR2 pins are removed from PLL so DFTIO pads were added (working under VDDC) for observation purpose.
MICRO-STAR INT'L CO.,LTD
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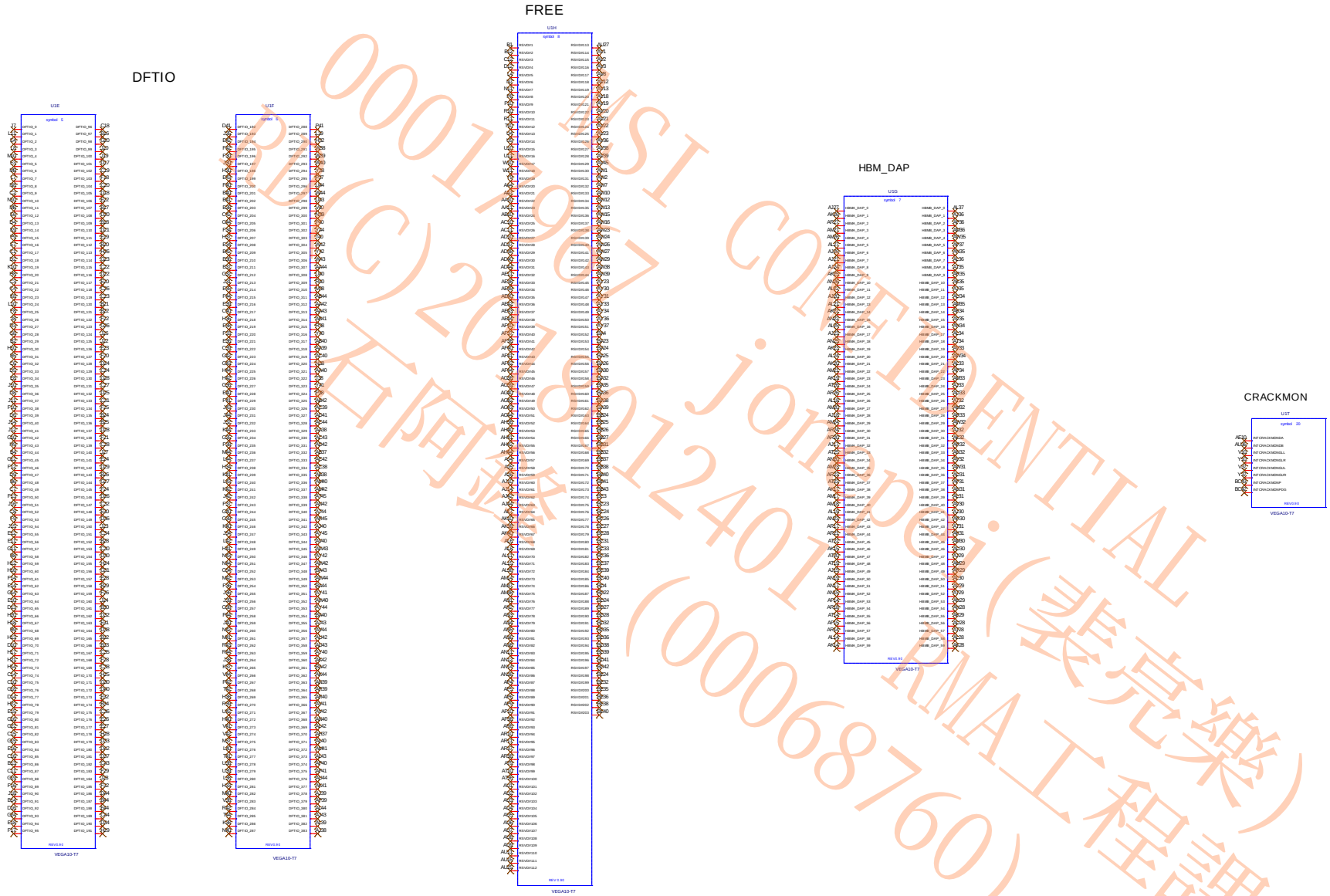

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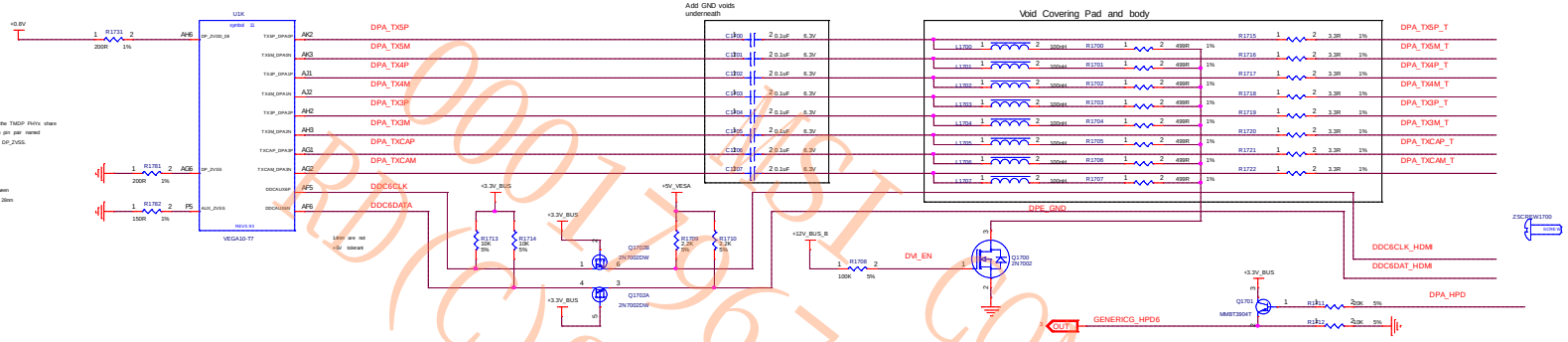
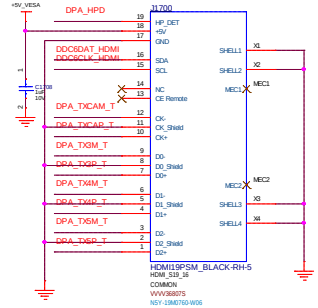
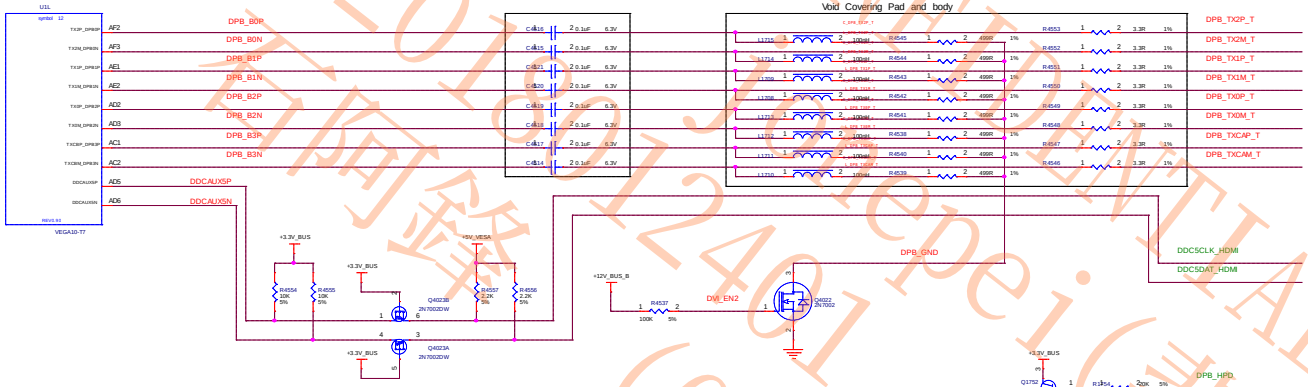
Ensure traces < 5 inches MAX (if routed on same layer)

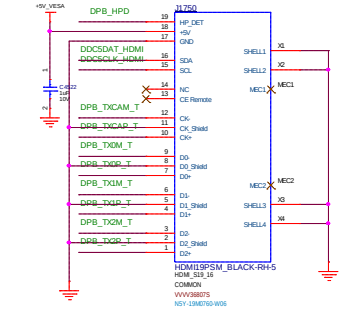
For differential routing on HDMI 2.0 connection, use dogbone shape antipads for the transitional vias of the same differential pair, and the distance from the via edge to the shape boundary should be

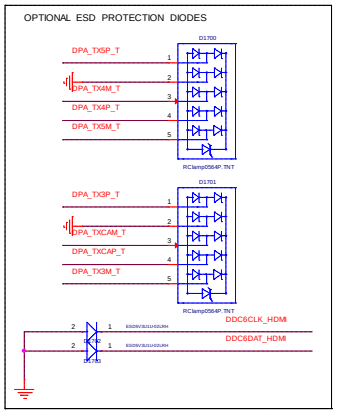


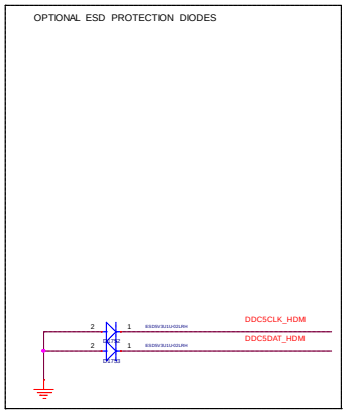


Ensure traces < 5 inches









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MS-V368		
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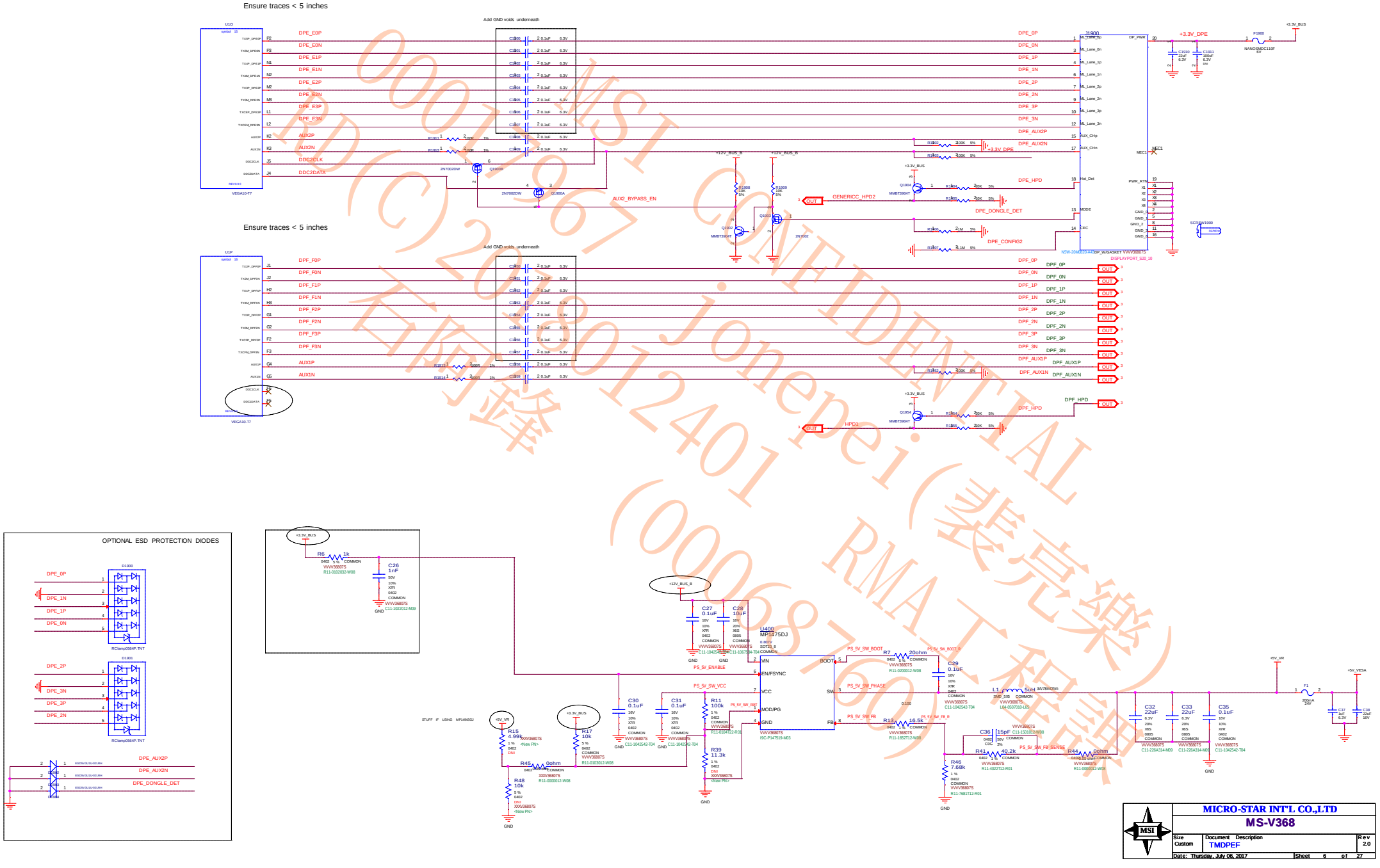
Ensure traces < 5 inches
Add GND voids underneath
U1O
VEGA10-T7
DPE_E0P
DPE_E0N
DPE_E1P
DPE_E1N
DPE_E2P
DPE_E2N
DPE_E3P
DPE_E3N
AUX2P
AUX2N
DDC2CLK
DDC2DATA
AUX2_BYPASS_EN
GENERICC_HPD2
DPE_DONGLE_DET
DPE_CONFIG2
DPE_HPD
+3.3V_DPE
+12V_BUS_B
Ensure traces < 5 inches
Add GND voids underneath
U1P
VEGA10-T7
DPF_F0P
DPF_F0N
DPF_F1P
DPF_F1N
DPF_F2P
DPF_F2N
DPF_F3P
DPF_F3N
AUX1P
AUX1N
HPD1
DPF_HPD
OPTIONAL ESD PROTECTION DIODES
D1900
D1901
RClamp0564P.TNT
DPE_AUX2P
DPE_AUX2N
DPE_DONGLE_DET
U400
MP1475DJ
PS_5V_ENABLE
PS_5V_SW_VCC
PS_5V_SW_BOOT
PS_5V_SW_PHASE
PS_5V_SW_FB
PS_5V_SW_FB_SENSE
PS_5V_SW_BOOT_R
PS_5V_SW_FB_R
STUFF IF USING MP1496GJ
+5V_VR
+5V_VESA
GND
MICRO-STAR INT'L CO.,LTD
MS-V368
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Custom
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TMDPEF
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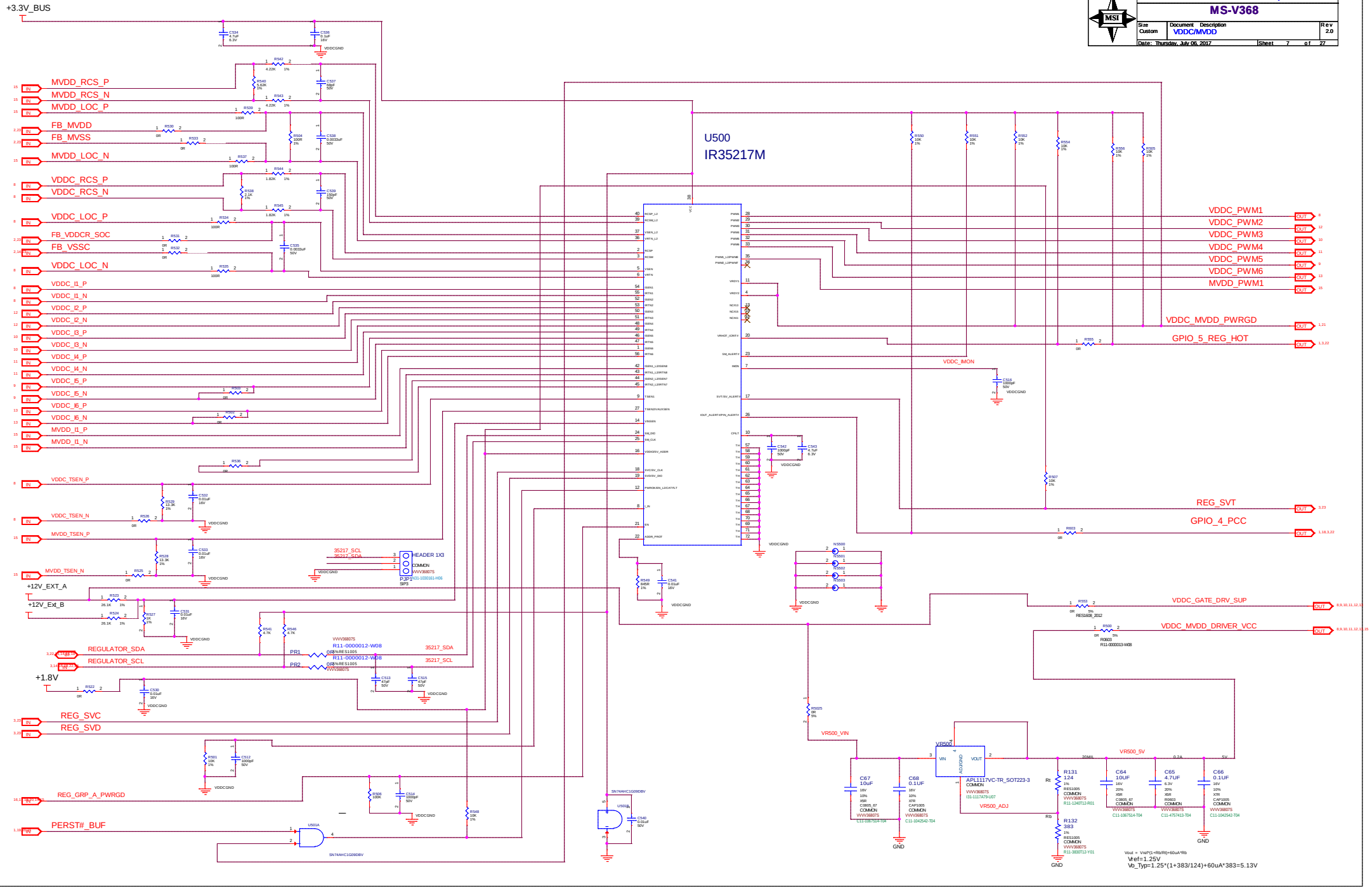
+3.3V_BUS
MICRO-STAR INT'L CO.,LTD
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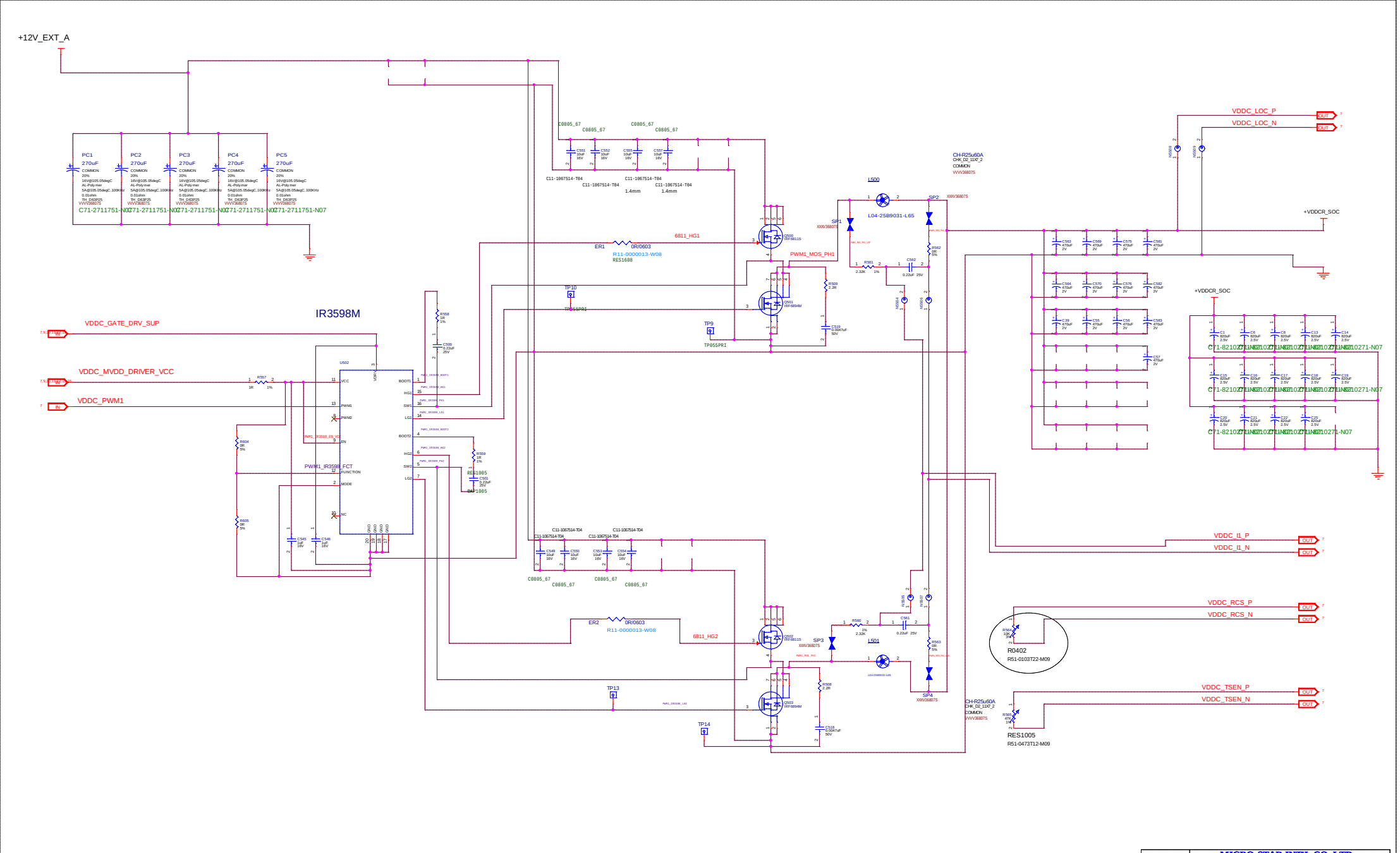
U500
IR35217M
MVDD_RCS_P
MVDD_RCS_N
MVDD_LOC_P
FB_MVDD
FB_MVSS
MVDD_LOC_N
VDDC_RCS_P
VDDC_RCS_N
VDDC_LOC_P
FB_VDDCR_SOC
FB_VSSC
VDDC_LOC_N
VDDC_I1_P
VDDC_I1_N
VDDC_I2_P
VDDC_I2_N
VDDC_I3_P
VDDC_I3_N
VDDC_I4_P
VDDC_I4_N
VDDC_I5_P
VDDC_I5_N
VDDC_I6_P
VDDC_I6_N
MVDD_I1_P
MVDD_I1_N
VDDC_TSEN_P
VDDC_TSEN_N
MVDD_TSEN_P
MVDD_TSEN_N
+12V_EXT_A
+12V_Ext_B
REGULATOR_SDA
REGULATOR_SCL
+1.8V
REG_SVC
REG_SVD
REG_GRP_A_PWRGD
PERST#_BUF
35217_SCL
35217_SDA
VDDC_PWM1
VDDC_PWM2
VDDC_PWM3
VDDC_PWM4
VDDC_PWM5
VDDC_PWM6
MVDD_PWM1
VDDC_MVDD_PWRGD
GPIO_5_REG_HOT
VDDC_IMON
REG_SVT
GPIO_4_PCC
VDDC_GATE_DRV_SUP
VDDC_MVDD_DRIVER_VCC
VR500_VIN
VR500_5V
VR500_ADJ
APL1117VC-TR_SOT223-3
Vout = Vref*(1+Rt/Rb)+60uA*Rb
Vref=1.25V
Vo_Typ=1.25*(1+383/124)+60uA*383=5.13V



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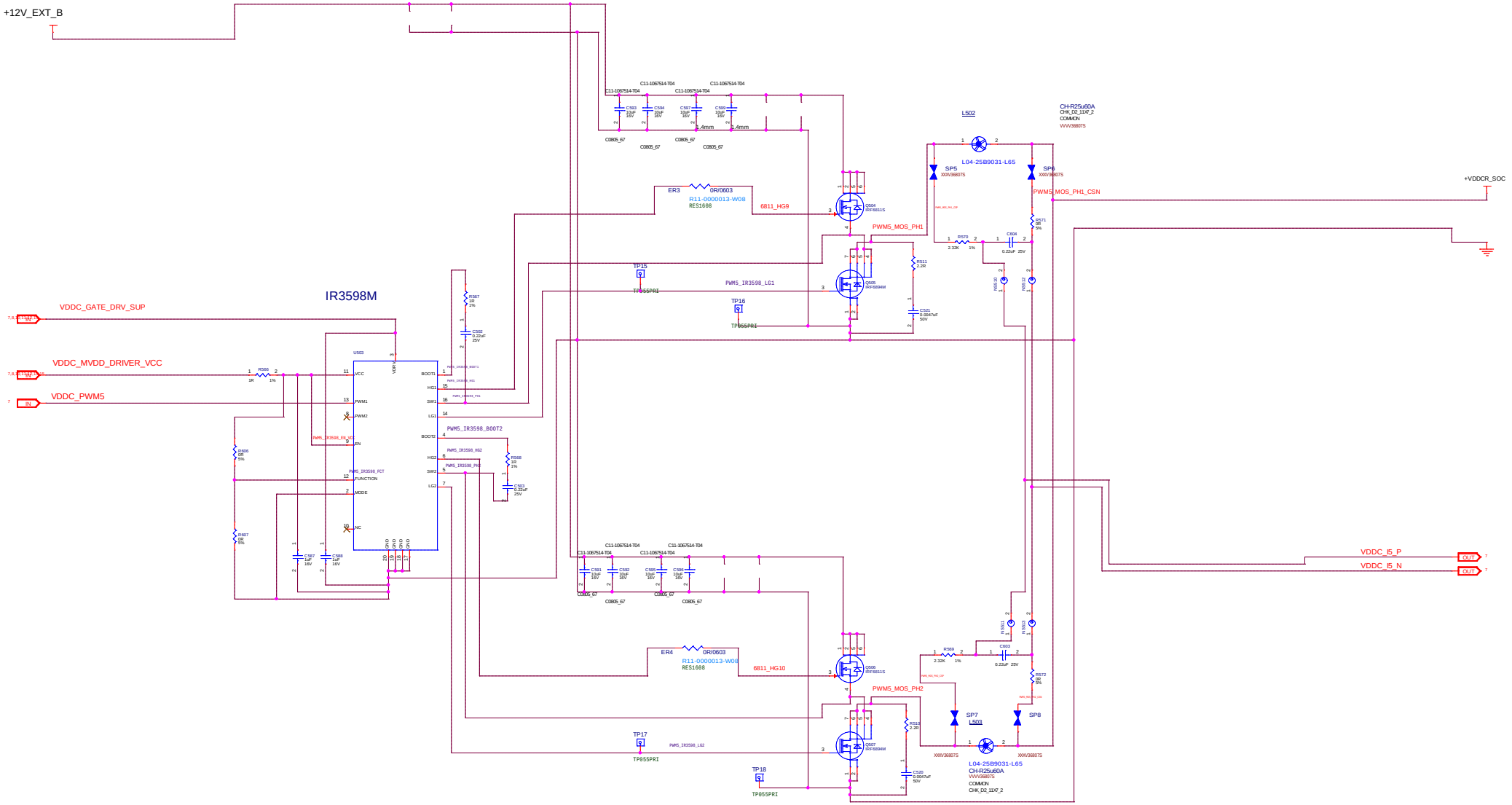

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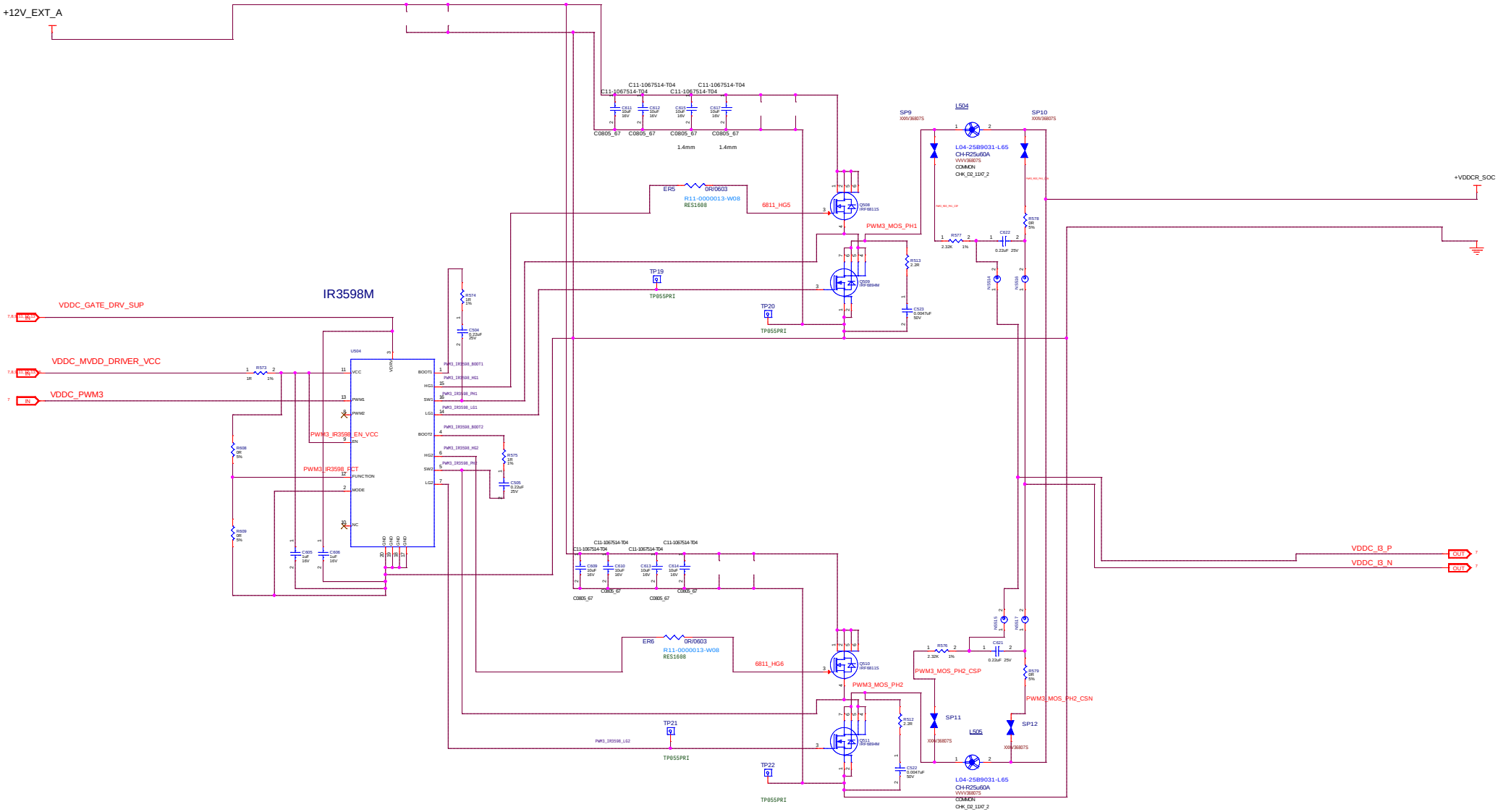

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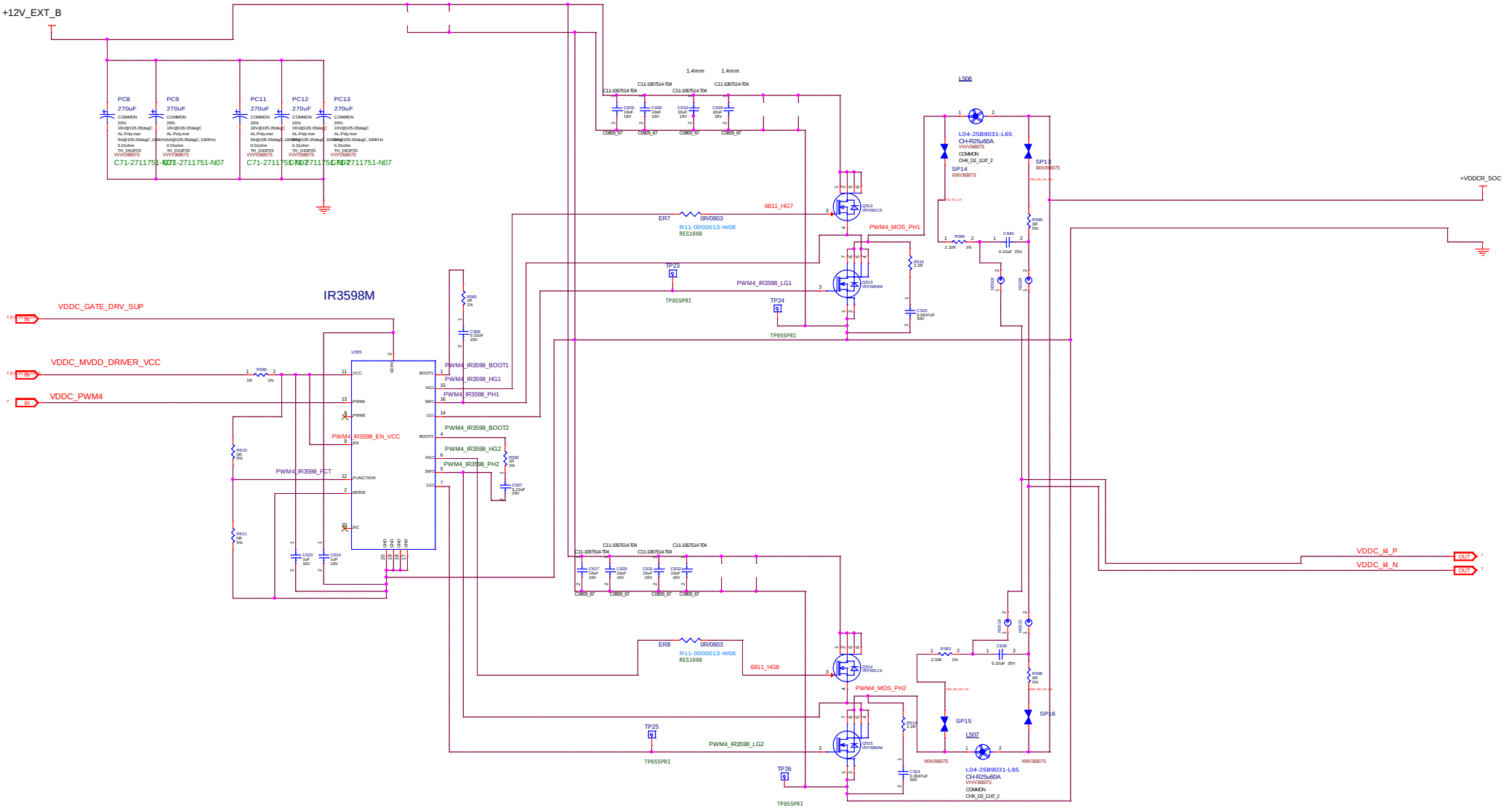

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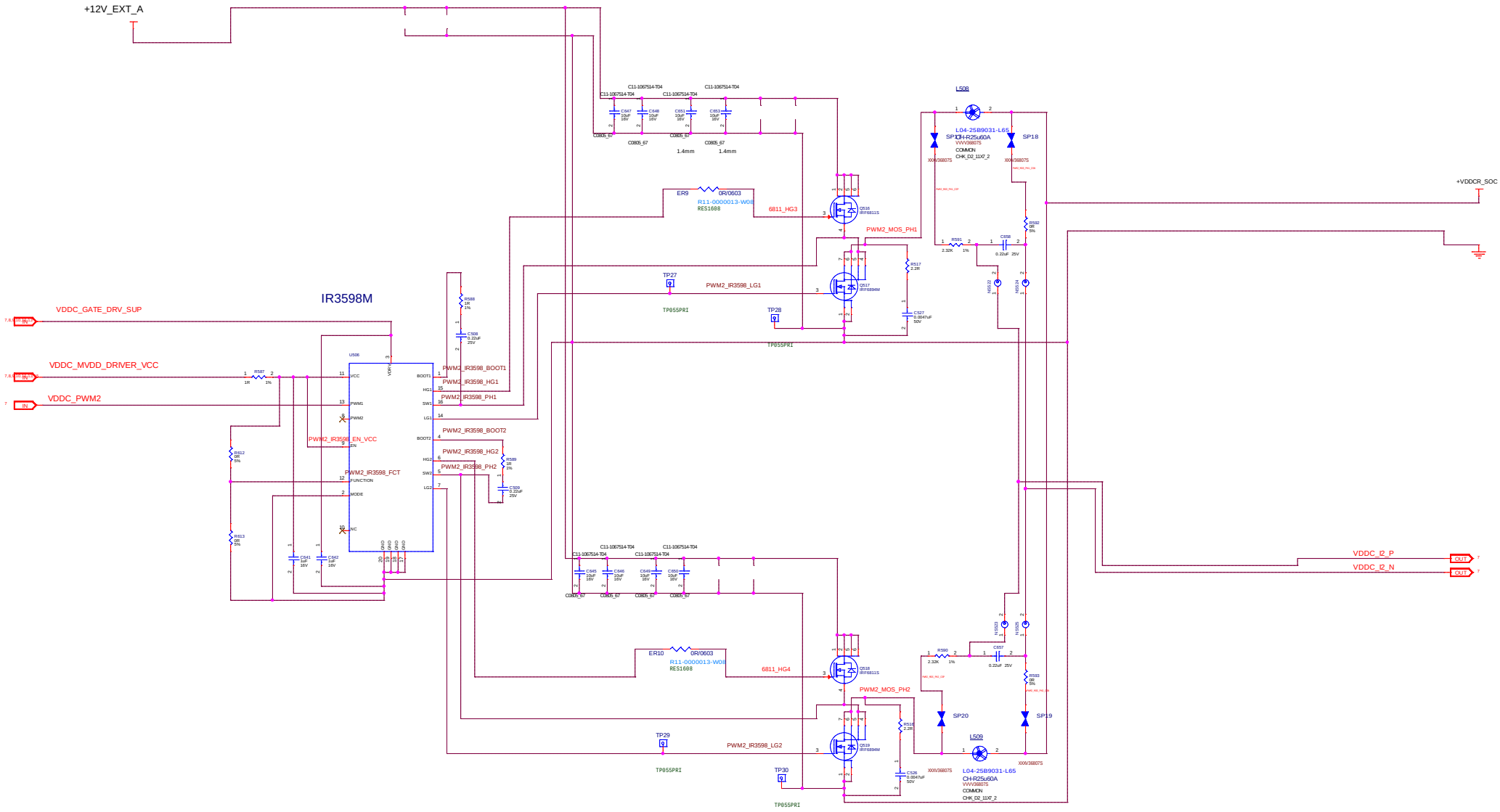
+12V_EXT_A
IR3598M
VDDC_GATE_DRV_SUP
VDDC_MVDD_DRIVER_VCC
VDDC_PWM2
PWM2_IR3598_BOOT1
PWM2_IR3598_HG1
PWM2_IR3598_PH1
PWM2_IR3598_BOOT2
PWM2_IR3598_HG2
PWM2_IR3598_PH2
PWM2_IR3598_EN_VCC
PWM2_IR3598_FCT
PWM2_IR3598_LG1
PWM2_IR3598_LG2
PWM2_MOS_PH1
PWM2_MOS_PH2
6811_HG3
6811_HG4
ER9
ER10
R11-0000013-W08
RES1608
0R/0603
L04-25B9031-L65
CH-R25u60A
COMMON
CHK_D2_11X7_2
L508
L509
SP18
SP19
SP20
TP27
TP28
TP29
TP30
TP055PRI
+VDDCR_SOC
VDDC_I2_P
VDDC_I2_N
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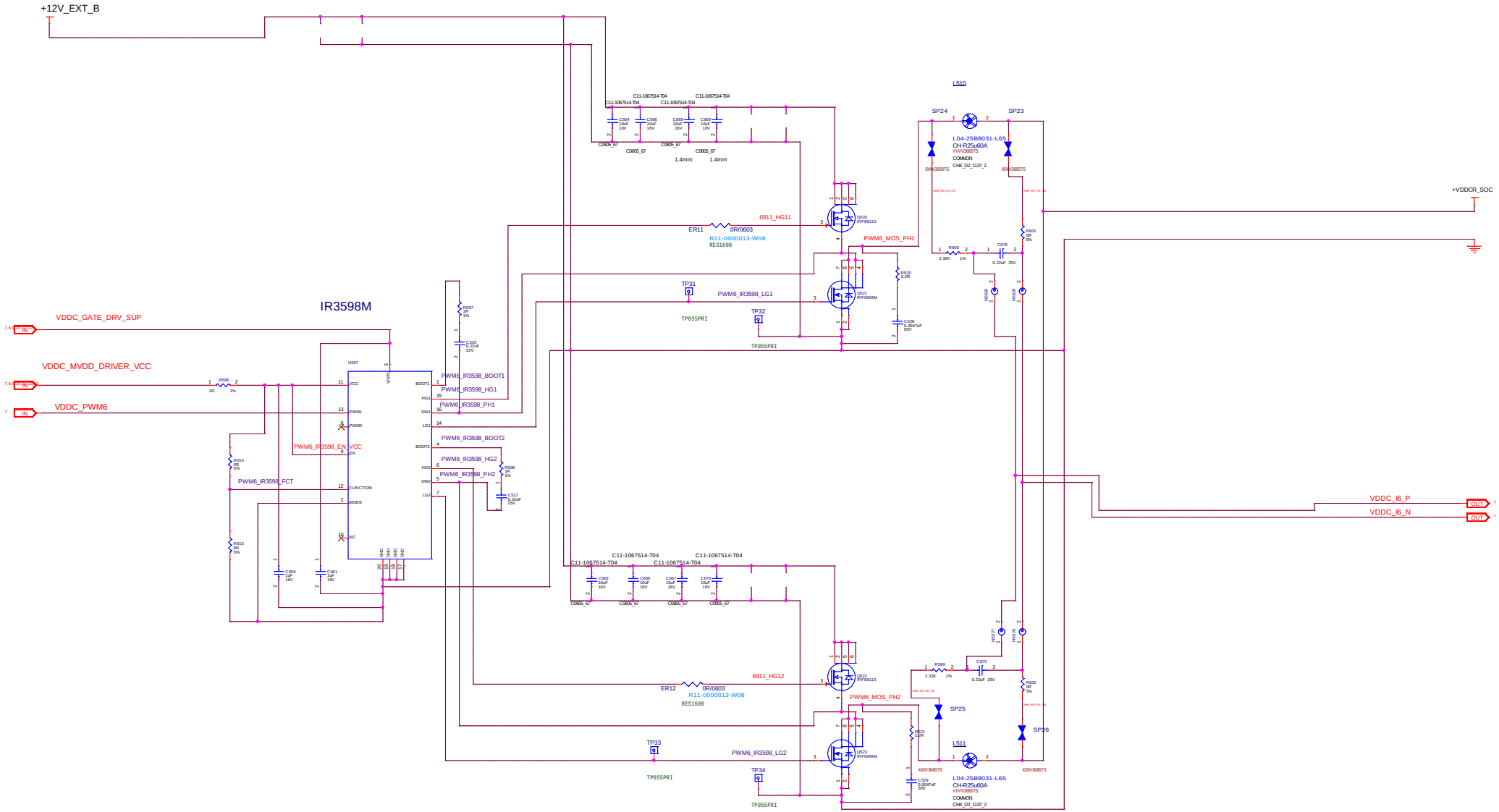

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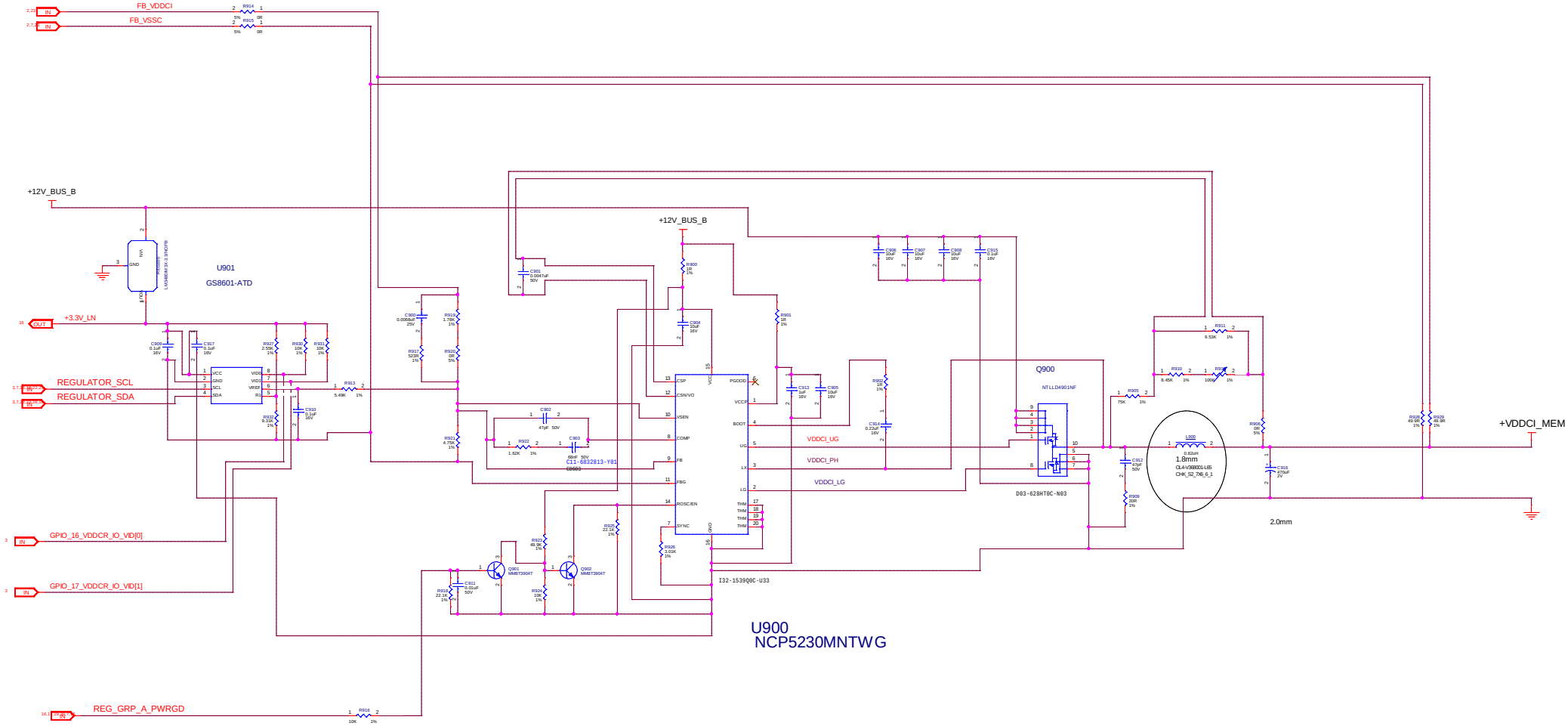

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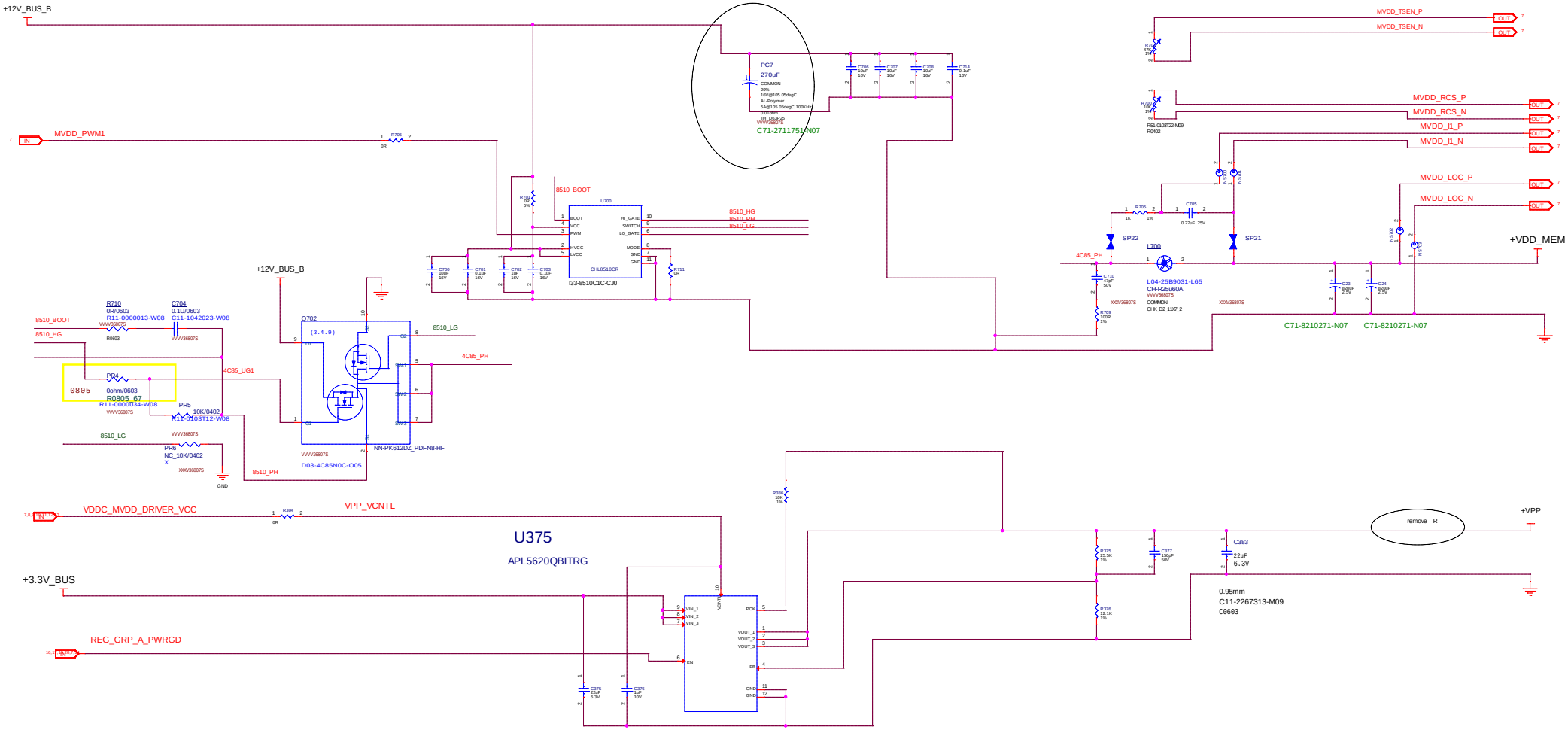

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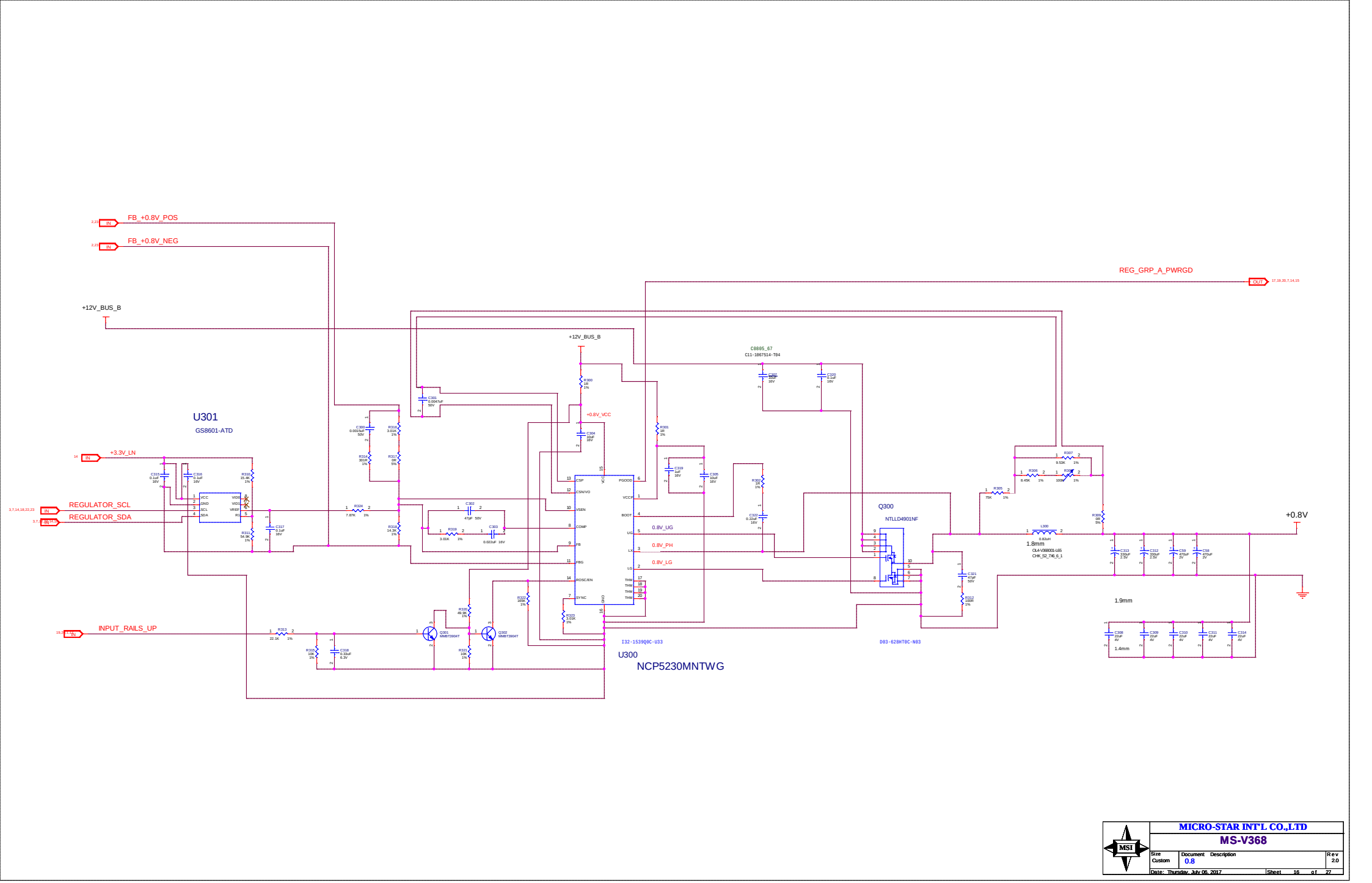

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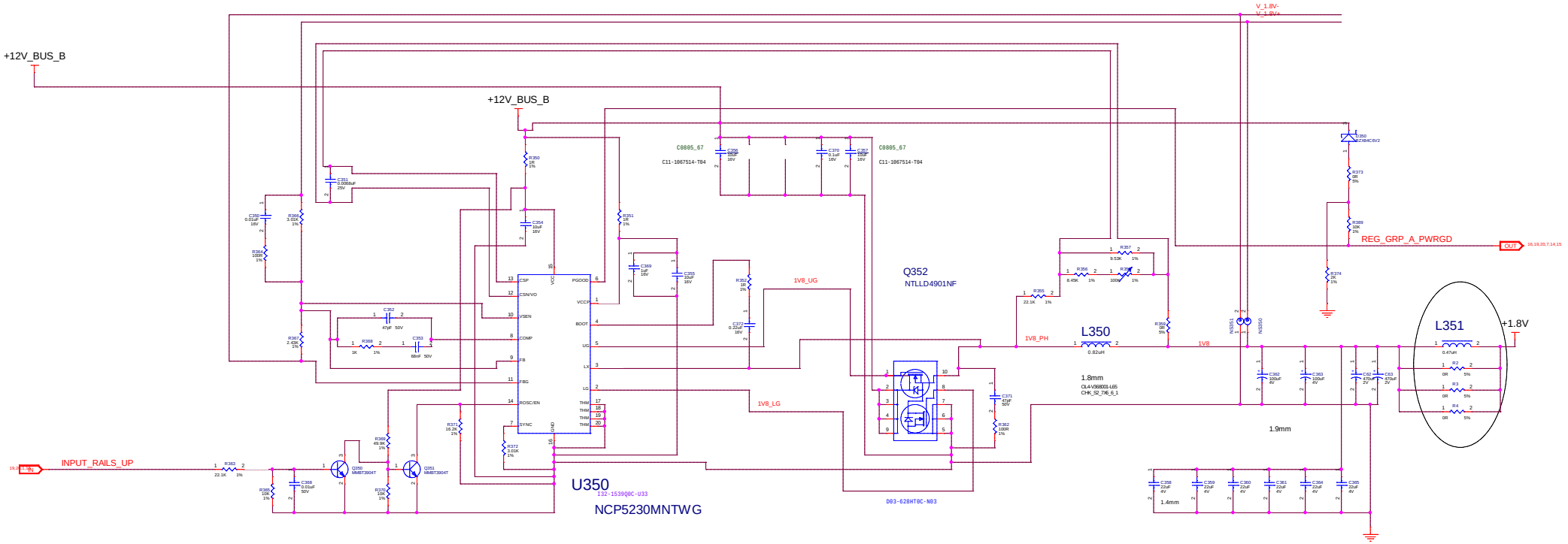

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remove PCC

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MS-V368

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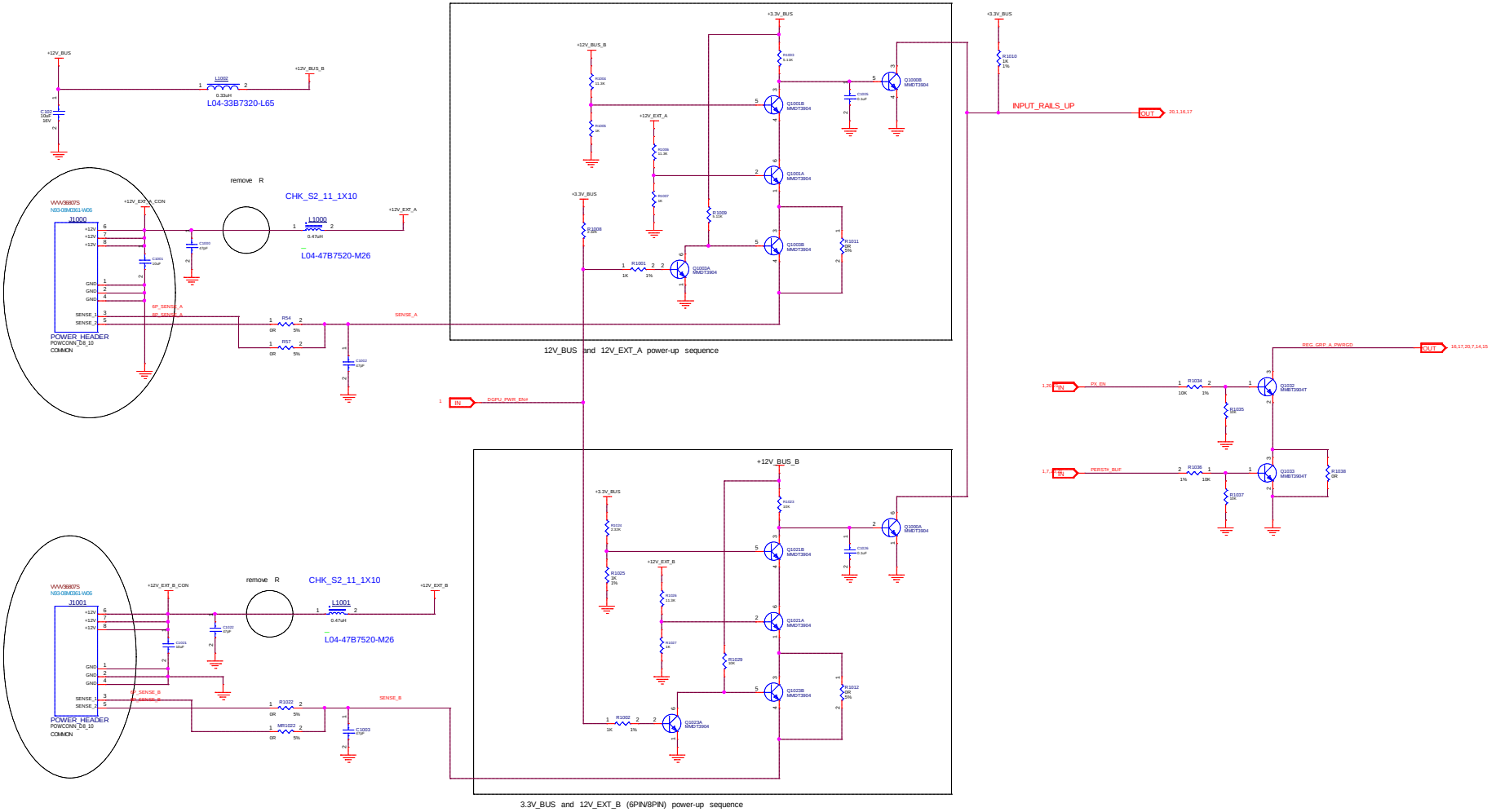

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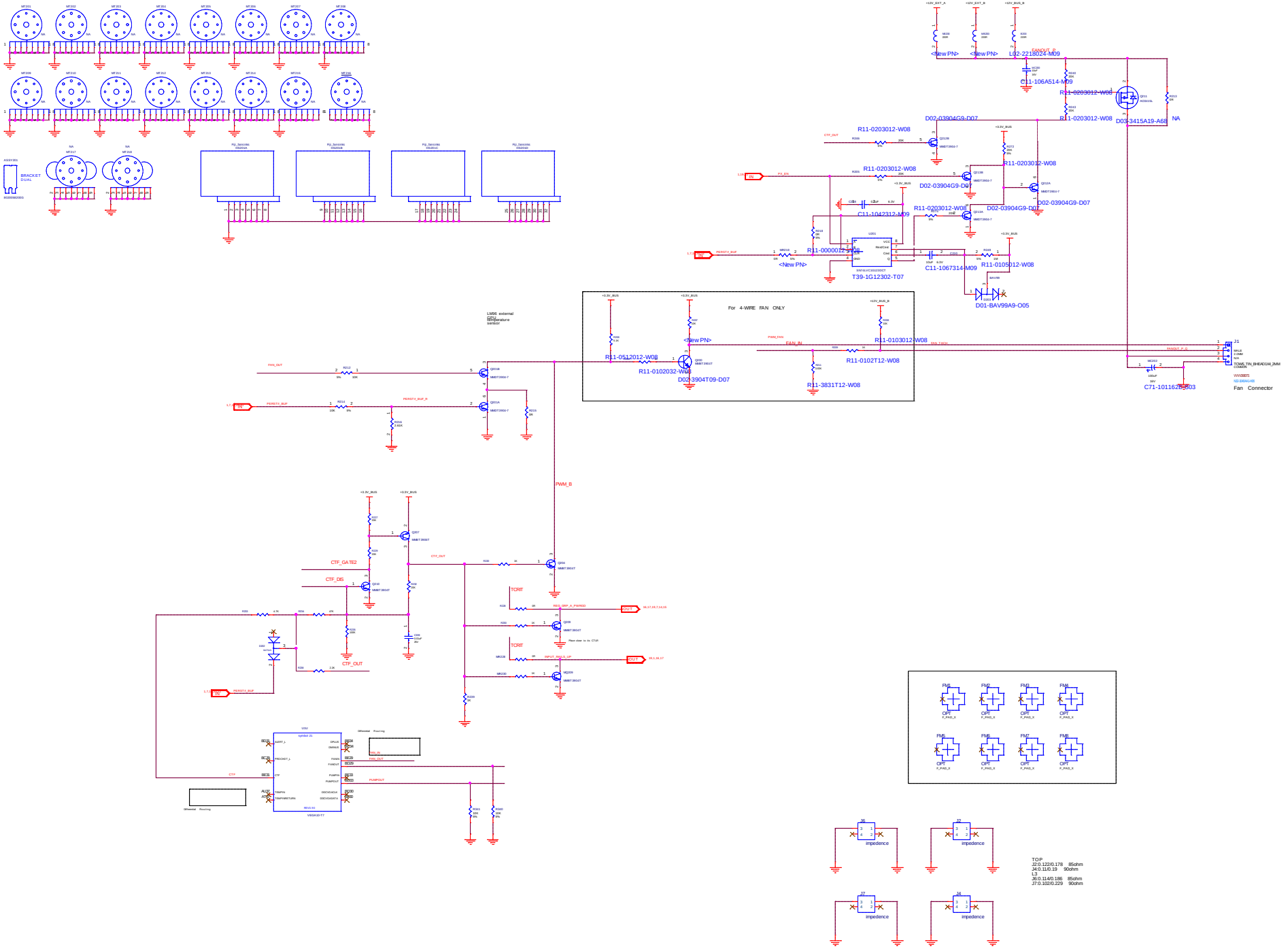

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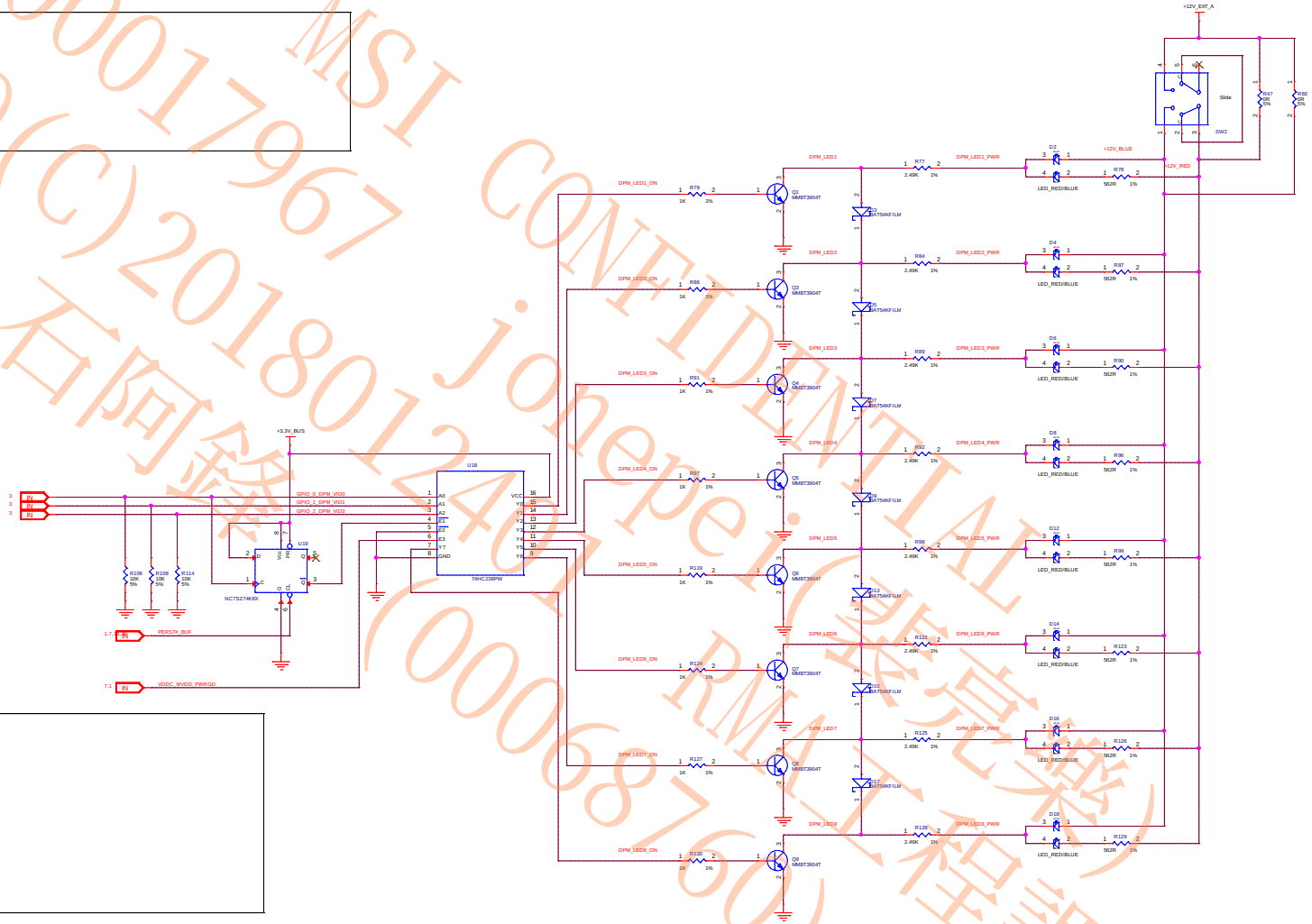
LED GREEN "ON" indicates BACO mode



RADEON Lightbar header

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RD(C)20180124017
joneper (李宗勳)
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右向後 (00068760)

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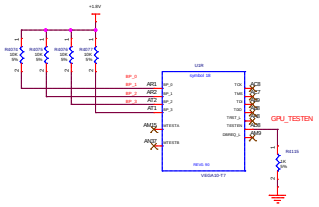
00017967 jonepei(裴完樂)
RD(C)20180124O1 RMA工程課
石阿鋒 (00068760)



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0	A	10/9/15	Initial schematic creation
	B	6/30/16	Many Changes on PI circuit , Minor Chnages on SMPS
	C	9/30/16	Many Changes on PI circuit , ASIC SYMBOL UPDATED FOR FLASH ROM INTERFACE , flash ROM SI/SO swapped , RP1 added
	D	11/29/16	Changes on PI circuit , 100MHz HCSL clock source replced (contact AMD for detailes)
	E	01/05/17	PI circuit removed , 200R added to DP AUX (6 resistors)
	-00	02/02/17	1.8V/VPP Kelvin resistors dual footprinted , DP AUX (6 resistors changed to 100R) , Changed R4033 to 360R 1206 and moved to 12V_AUX , SMBUS Address note swap , J4001 removed , R115/R116 changed to 61.9R , R205 added

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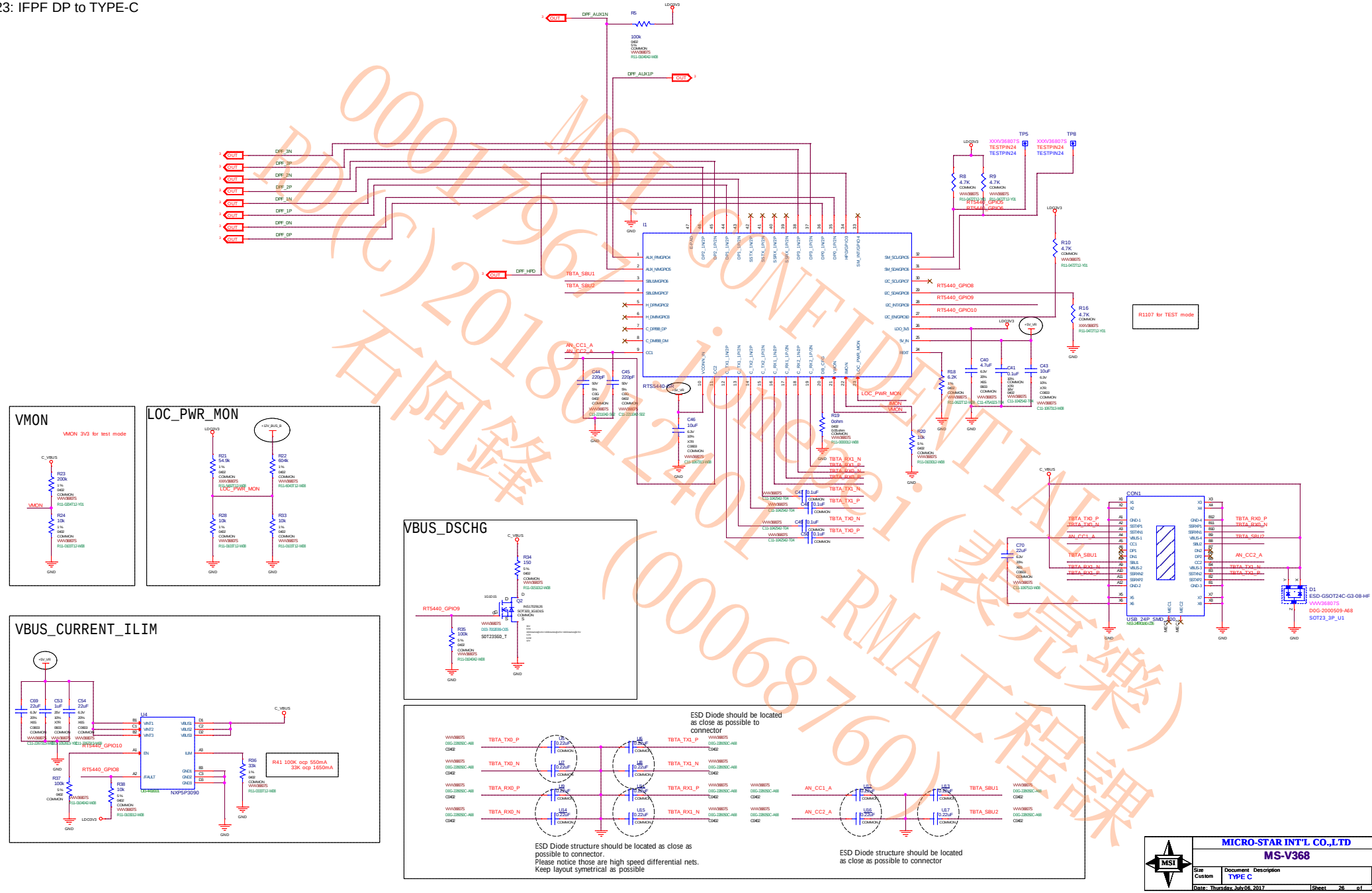
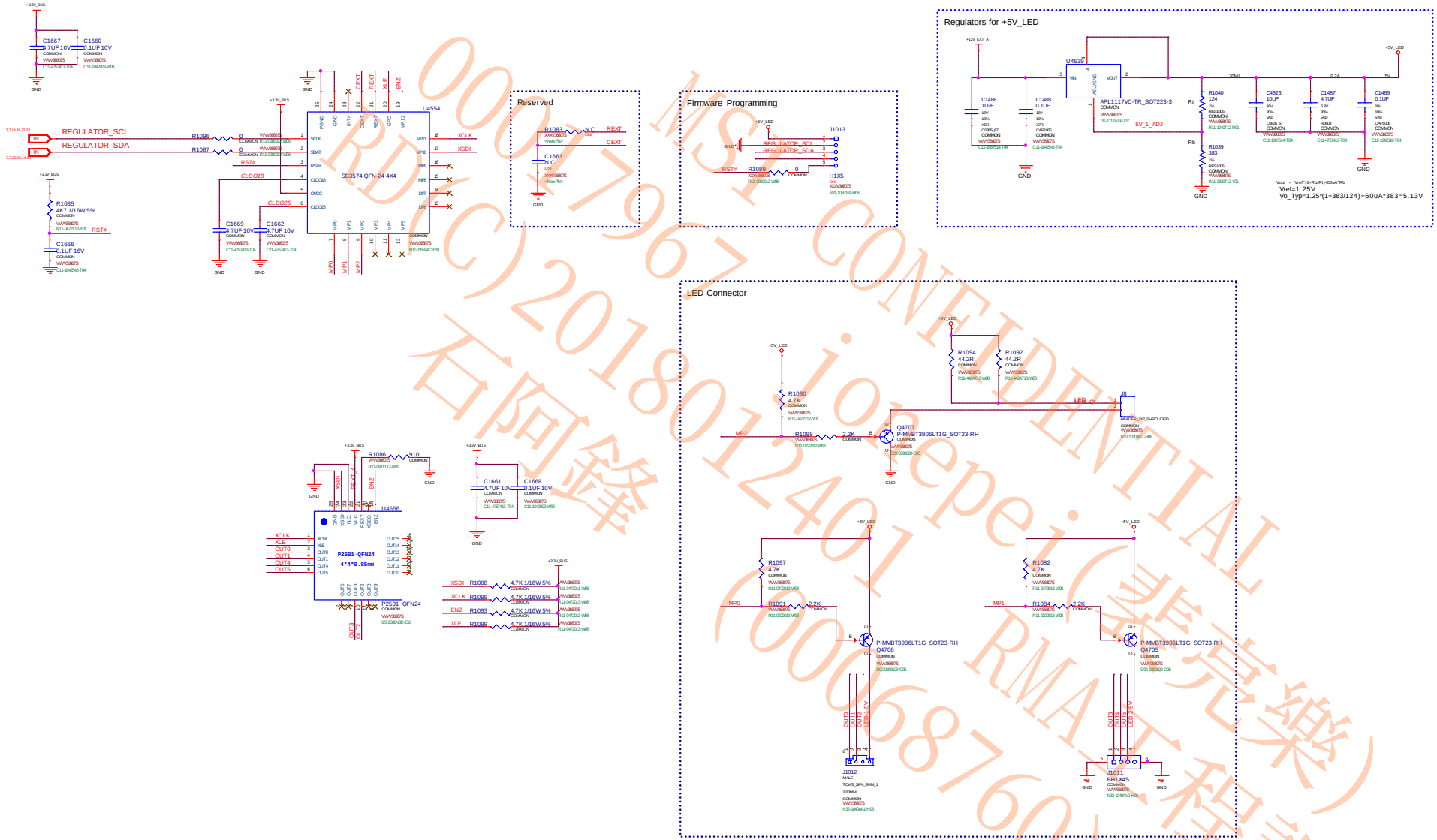
Page23: IFPF DP to TYPE-C



Page39: LED_CONTROLLER_ENE3574



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