

P1040-A03 GF114

GF114-400, 1024MB/2048MB, GDDR5 256b 32M/64Mx32
DVI-I-DL, DVI-I-DL/DP, mHDMI

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REV	VARIANT	W/VPN	ASSEMBLY
B	BASE	600-11040-BASE_300	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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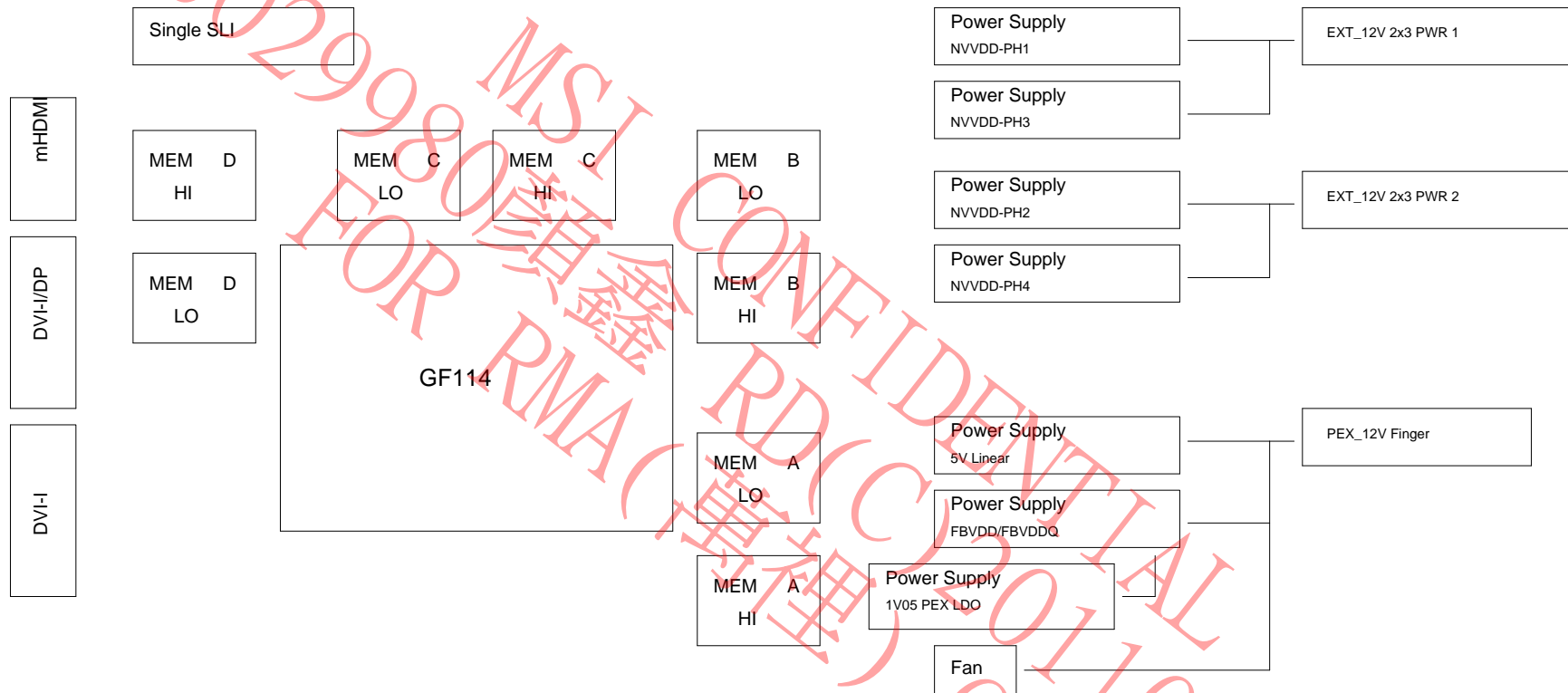


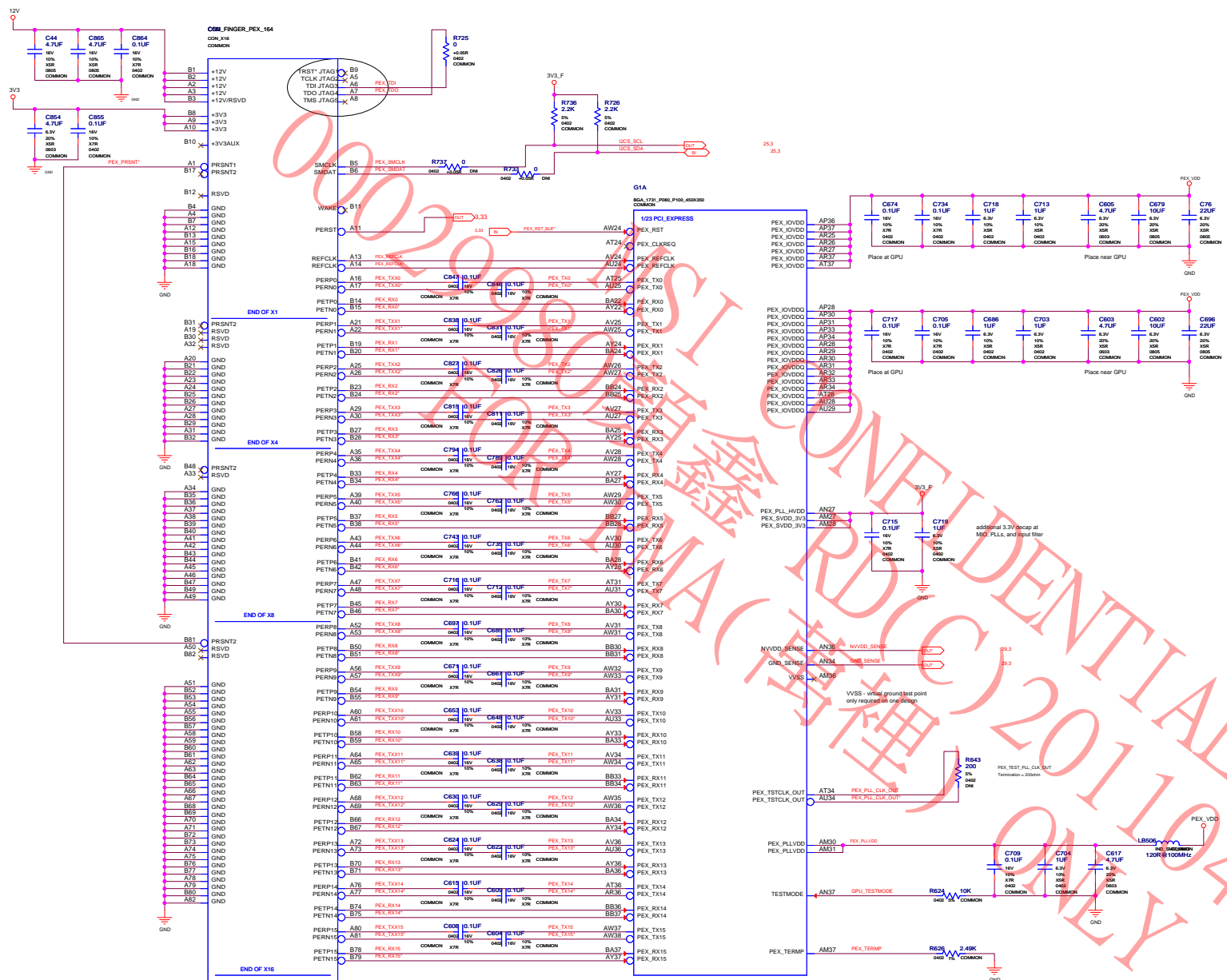
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MS-V260

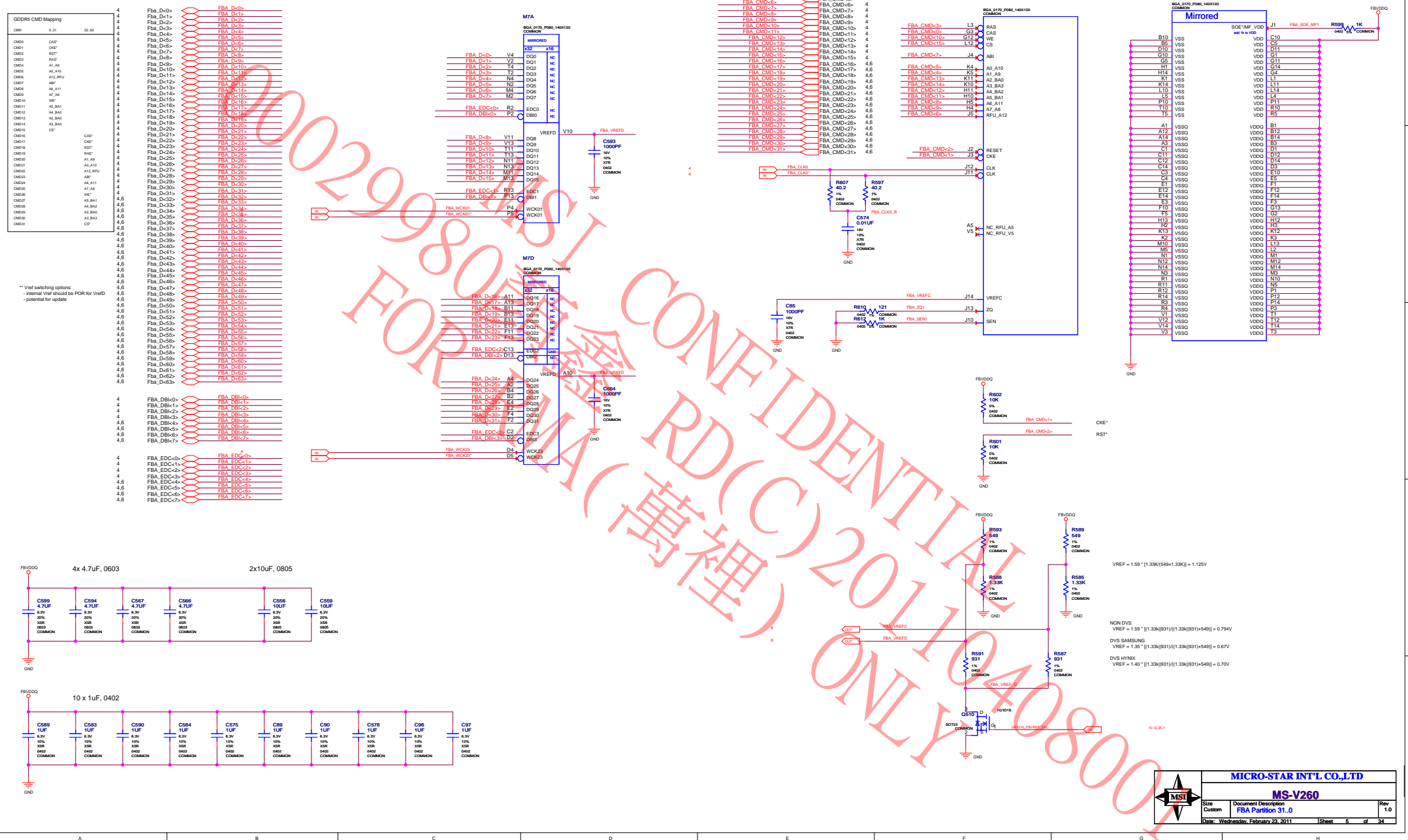
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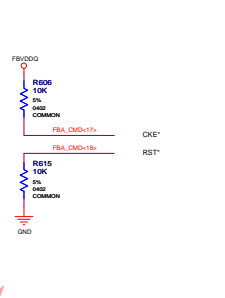
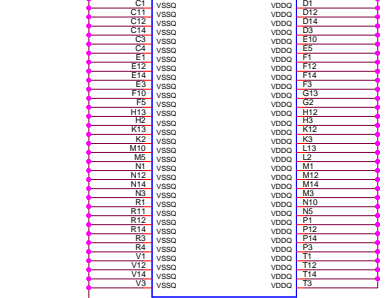
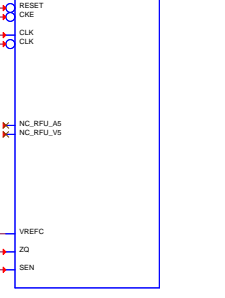
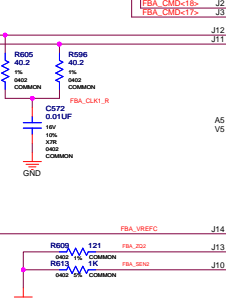
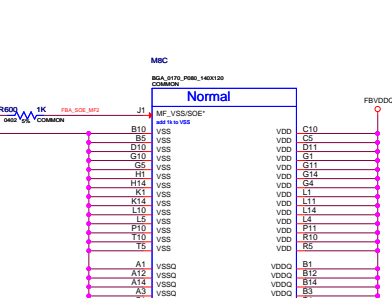
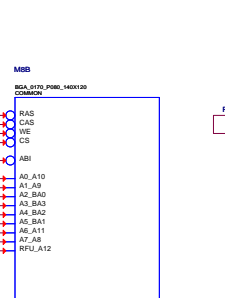
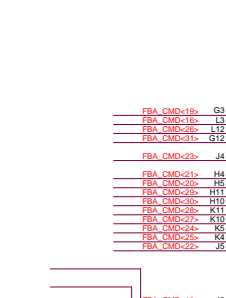
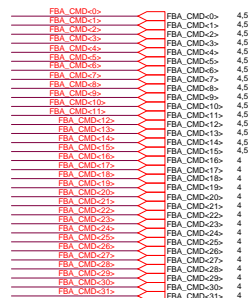
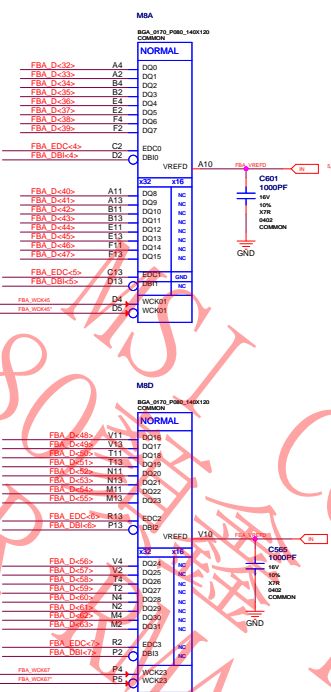
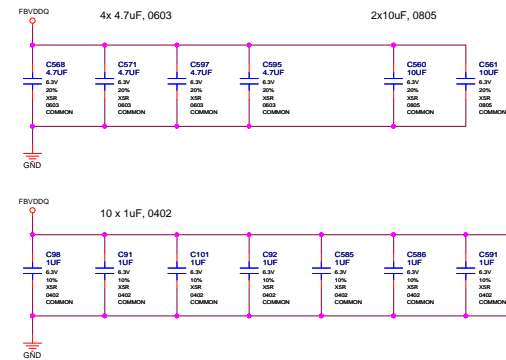
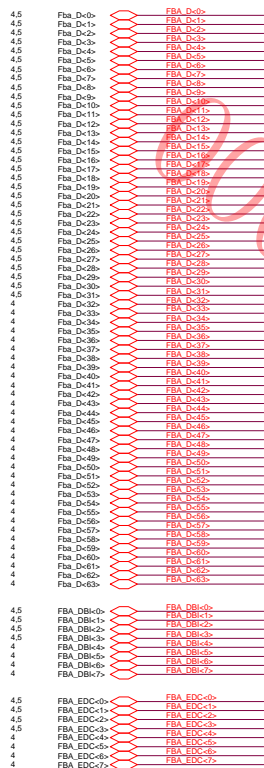


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	MS-V260		
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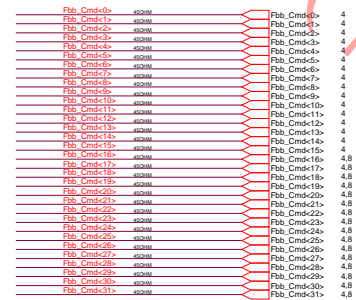
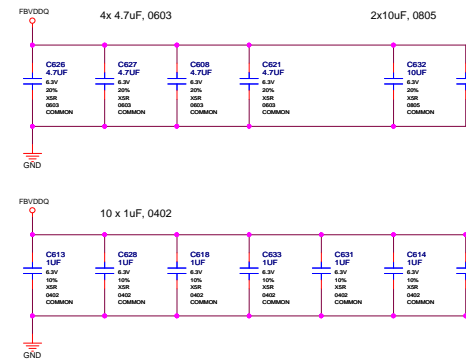
GDGRS CAM Mapping		
CMD		GDGRS
CMD0	CAS*	
CMD1	CST*	
CMD2	BEST	
CMD3	RAS*	
CMD4	A1, A0	
CMD5	A0, A10	
CMD6	A2, RFU	
CMD7	ABP	
CMD8	AL, A11	
CMD9	A2, A8	
CMD10	WE*	
CMD11	AS, BA1	
CMD12	A4, BA2	
CMD13	A4, BA3	
CMD14	A3, BA3	
CMD15	C5*	
CMD16		CAS*
CMD17		CME*
CMD18		BEST*
CMD19		RAS*
CMD20		A1, A0
CMD21		A2, A10
CMD22		A2, RFU
CMD23		ABP
CMD24		AL, A11
CMD25		A2, A8
CMD26		WE*
CMD27		AS, BA1
CMD28		AS, BA2
CMD29		A2, BA2
CMD30		A3, BA3
CMD31		C5*

** Vref switching options:
- internal Vref should be POR for VrefD



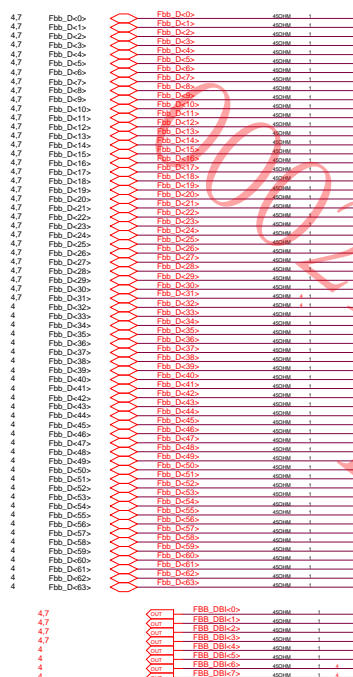
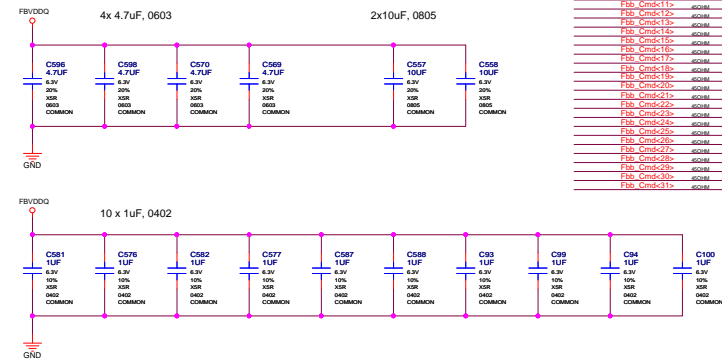
GDDR5 CMD Mapping		
CMD0	CS#	30,35
CMD0	CAS#	4
CMD1	OE#	4
CMD2	WE#	4
CMD3	RA#	4
CMD4	A1,A0	4
CMD5	A2,A15	4
CMD6	A16,RP0	4
CMD7	AB#	4
CMD8	AB,A11	4
CMD9	A2,A8	4
CMD10	WE#	4
CMD11	A2,A8	4
CMD12	A2,BAG	4
CMD13	A2,BAG	4
CMD14	A2,BAG	4
CMD15	CS#	4
CMD16	CAS#	4
CMD17	OE#	4
CMD18	WE#	4
CMD19	A1,A0	4
CMD20	A2,A15	4
CMD21	A16,RP0	4
CMD22	AB#	4
CMD23	AB,A11	4
CMD24	A2,A8	4
CMD25	WE#	4
CMD26	A2,A8	4
CMD27	A2,BAG	4
CMD28	A2,BAG	4
CMD29	A2,BAG	4
CMD30	CS#	4
CMD31	CAS#	4

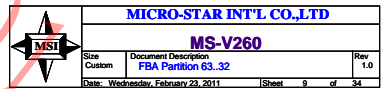
** Vref switching option:
external Vref should be POR for VrefH
potential for update



GDDR5 CMD Mapping		
CMD	IO	IO
CM00	CAS*	30,35
CM01	OE*	
CM02	WE*	
CM03	WE*	
CM04	AL, A10	
CM05	AL, A10	
CM06	AL, A10	
CM07	AB*	
CM08	AL, A11	
CM09	AL, A10	
CM10	WE*	
CM11	AL, BA1	
CM12	AL, BA2	
CM13	AL, BA3	
CM14	AL, BA3	
CM15	CE*	
CM16	CAS*	
CM17	OE*	
CM18	WE*	
CM19	WE*	
CM20	AL, A10	
CM21	AL, A10	
CM22	AL, A10	
CM23	AB*	
CM24	AL, A11	
CM25	AL, A10	
CM26	WE*	
CM27	AL, BA1	
CM28	AL, BA2	
CM29	AL, BA3	
CM30	AL, BA3	
CM31	CE*	

** We switching options:
 - Internal Vref should be POR for VrefD
 - potential for update

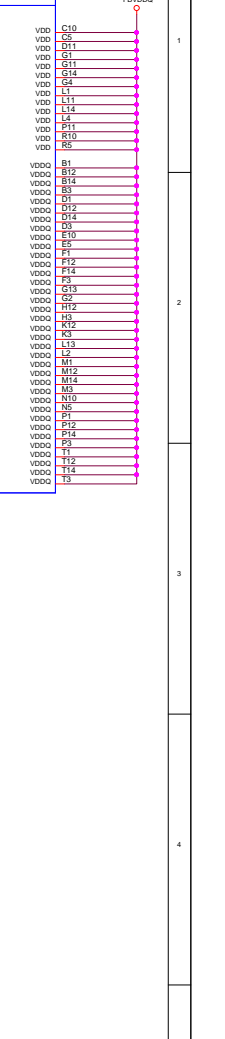
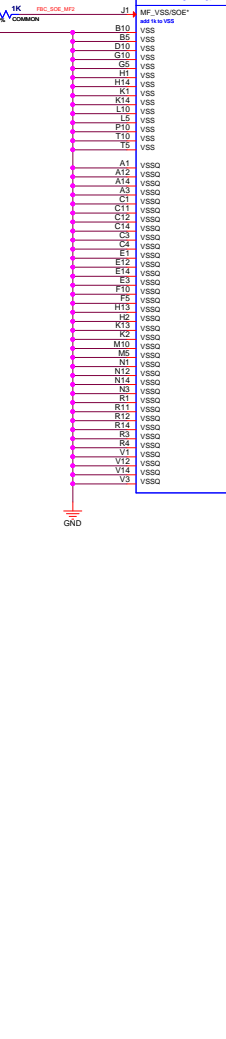
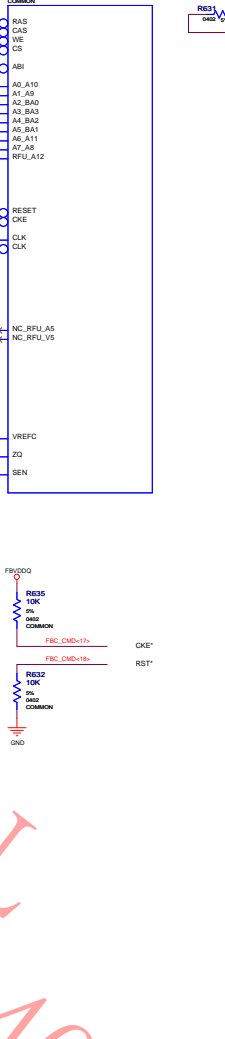
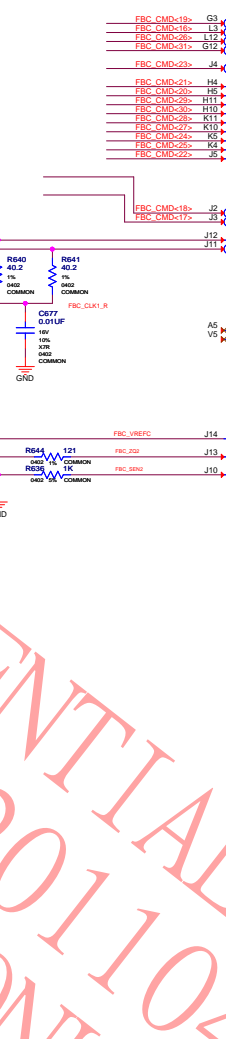
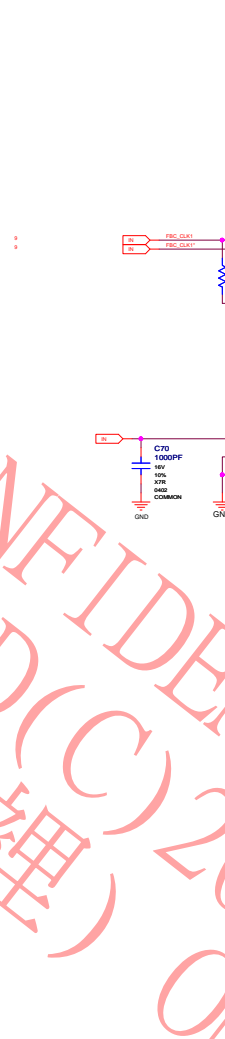
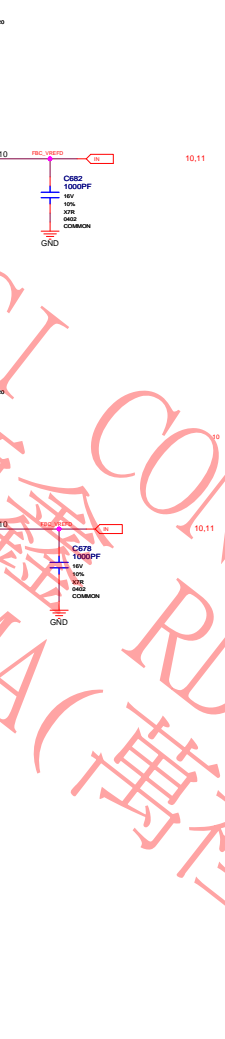
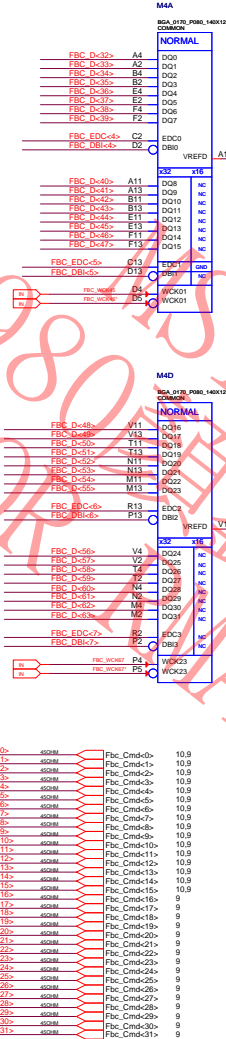
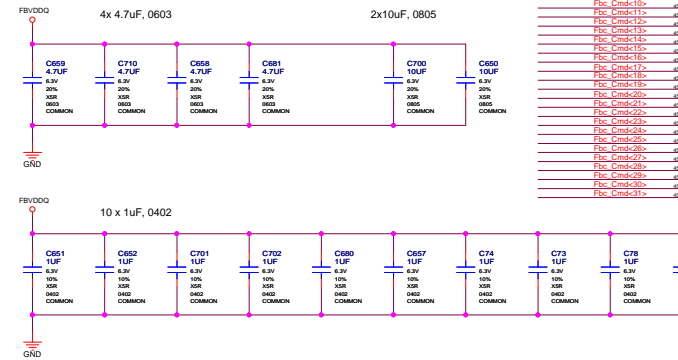






GDORS CMD Mapping		
CMD	Q-31	30..63
CMD0	CAD*	
CMD1	CAD*	
CMD2	RST*	
CMD3	RST*	
CMD4	A1..A9	
CMD5	A10..A19	
CMD6	A20..A29	
CMD7	A30..A39	
CMD8	A40..A49	
CMD9	A50..A59	
CMD10	A60..A69	
CMD11	A70..A79	
CMD12	A80..A89	
CMD13	A90..A99	
CMD14	A100..A109	
CMD15	CAD	
CMD16	CAD*	
CMD17	RST*	
CMD18	RST*	
CMD19	A1..A9	
CMD20	A10..A19	
CMD21	A20..A29	
CMD22	A30..A39	
CMD23	A40..A49	
CMD24	A50..A59	
CMD25	A60..A69	
CMD26	A70..A79	
CMD27	A80..A89	
CMD28	A90..A99	
CMD29	A100..A109	
CMD30	CAD	
CMD31	CAD*	

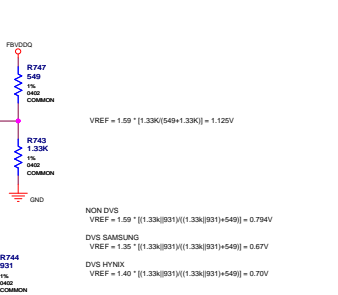
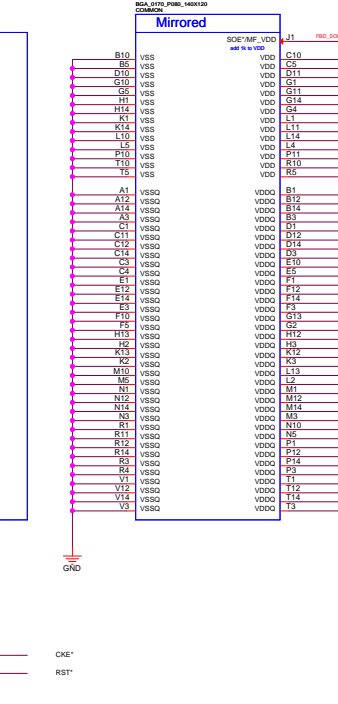
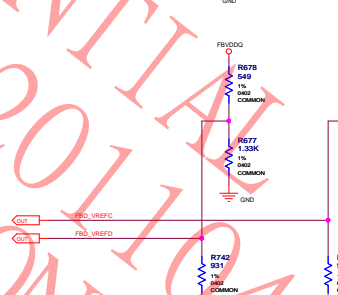
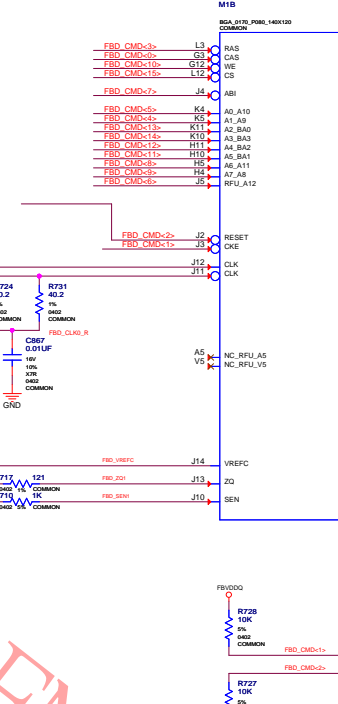
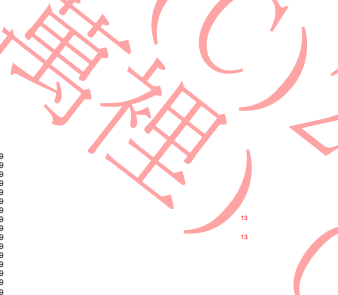
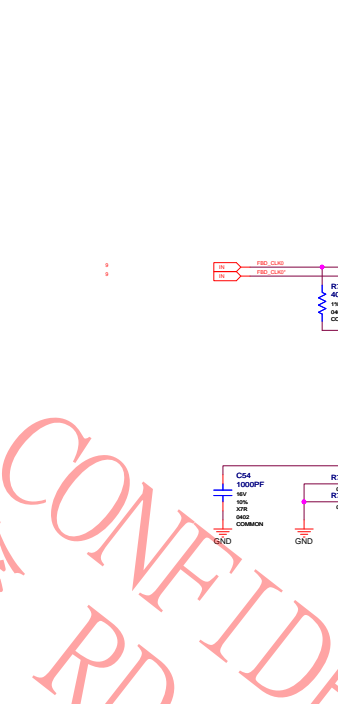
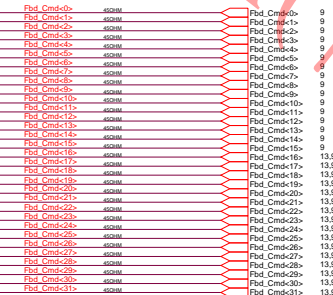
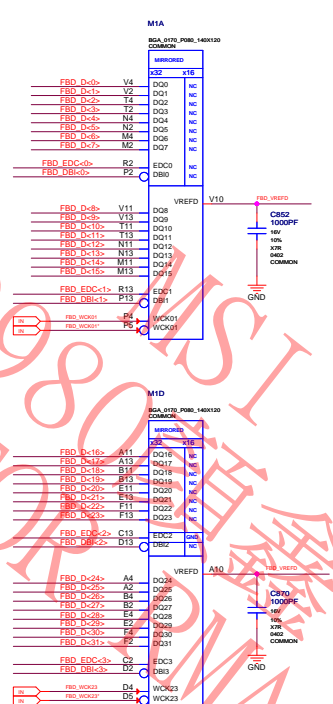
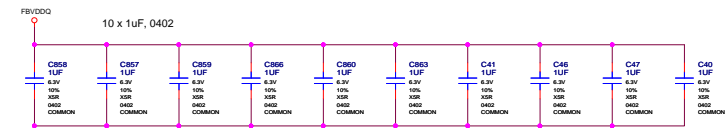
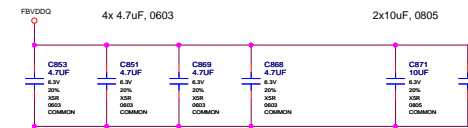
** Vref switching options:
- Internal Vref should be POR for VrefD
- potential for update



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GDORS CMD Mapping		
CMD	0..31	32..63
CMD0	CMD7	
CMD1	CMD8	
CMD2	RES7	
CMD3	RAS7	
CMD4	A1, A9	
CMD5	A1, A10	
CMD6	A12, RFU	
CMD7	AB7	
CMD8	AB, A11	
CMD9	A2, AB	
CMD10	WE7	
CMD11	AS, BA1	
CMD12	A1, BA2	
CMD13	A2, BA3	
CMD14	A3, BA4	
CMD15	CS7	
CMD16	CMD7	
CMD17	RES7	
CMD18	RAS7	
CMD19	AB7	
CMD20	A1, A9	
CMD21	A1, A10	
CMD22	A12, RFU	
CMD23	AB7	
CMD24	AB, A11	
CMD25	A2, AB	
CMD26	WE7	
CMD27	AS, BA1	
CMD28	A1, BA2	
CMD29	A2, BA3	
CMD30	A3, BA4	
CMD31	CS7	

** Vref switching options:
- Internal Vref should be POR for VrefD
- potential for update



$$VREF = 1.59 \times [1.33 \times (931 + 1.33)] = 1.125V$$

$$NON DVS$$

$$VREF = 1.59 \times [1.33 \times (931 + 1.33)] = 0.794V$$

$$DVS SAMPLING$$

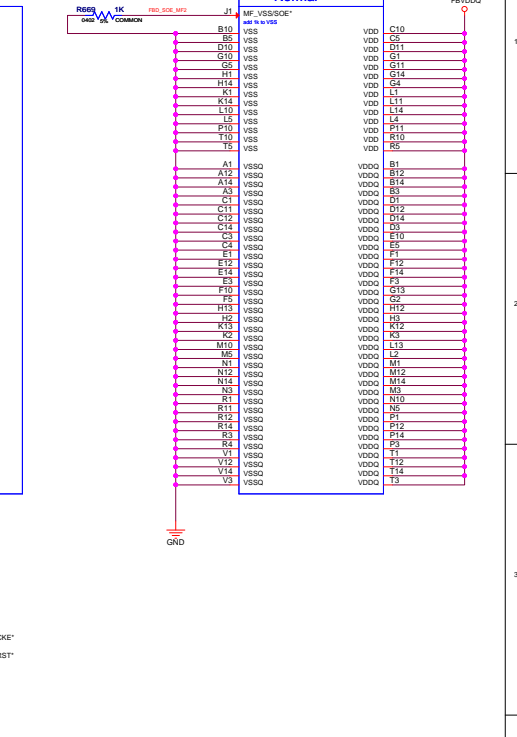
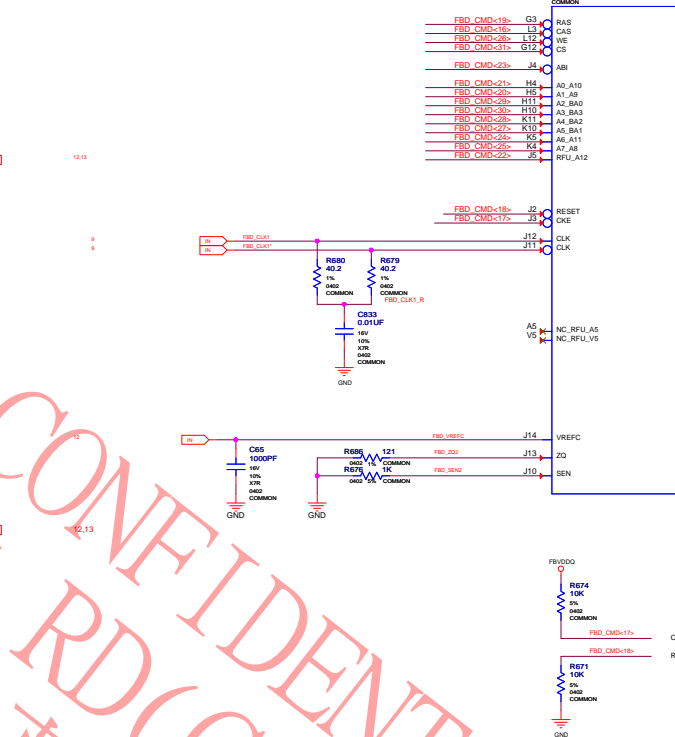
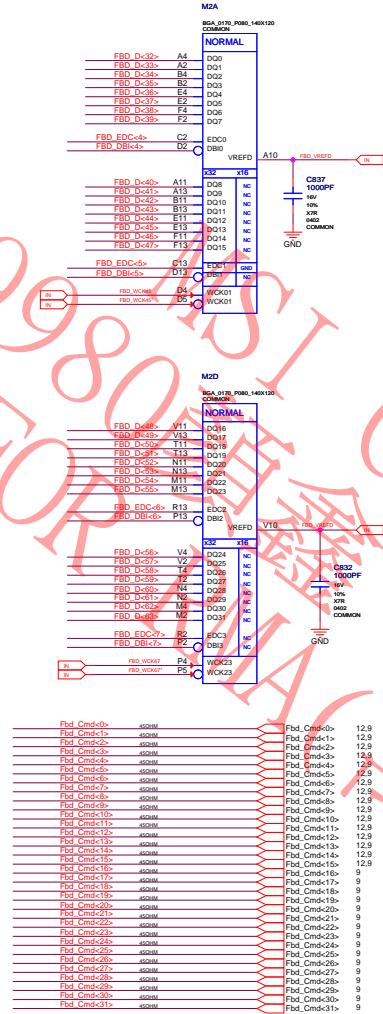
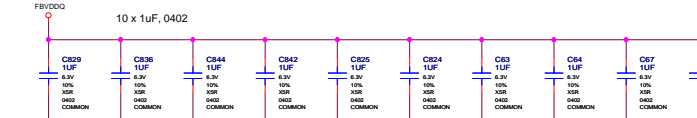
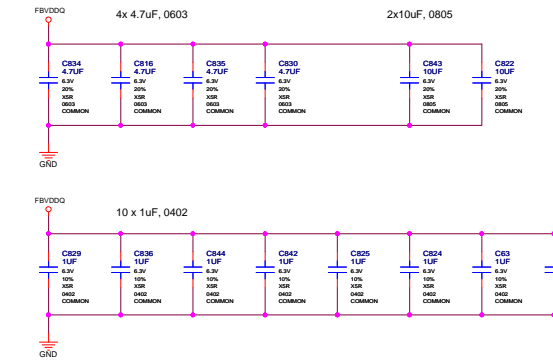
$$VREF = 1.59 \times [1.33 \times (931 + 1.33)] = 0.67V$$

$$DVS HYPIX$$

$$VREF = 1.40 \times [1.33 \times (931 + 1.33)] = 0.70V$$

GDORG CMD Mapping		
CMD	0..31	32..63
CMD0	CAS*	
CMD1	RAS*	
CMD2	RST*	
CMD3	BA0*	
CMD4	AL BA0	
CMD5	AL BA1	
CMD6	AL BA2	
CMD7	AL BA3	
CMD8	AL BA4	
CMD9	AL BA5	
CMD10	AL BA6	
CMD11	AL BA7	
CMD12	AL BA8	
CMD13	AL BA9	
CMD14	AL BA10	
CMD15	AL BA11	
CMD16	AL BA12	
CMD17	AL BA13	
CMD18	AL BA14	
CMD19	AL BA15	
CMD20	AL BA16	
CMD21	AL BA17	
CMD22	AL BA18	
CMD23	AL BA19	
CMD24	AL BA20	
CMD25	AL BA21	
CMD26	AL BA22	
CMD27	AL BA23	
CMD28	AL BA24	
CMD29	AL BA25	
CMD30	AL BA26	
CMD31	AL BA27	

** Vref switching options:
- internal Vref should be POR for VrefID
- potential for update



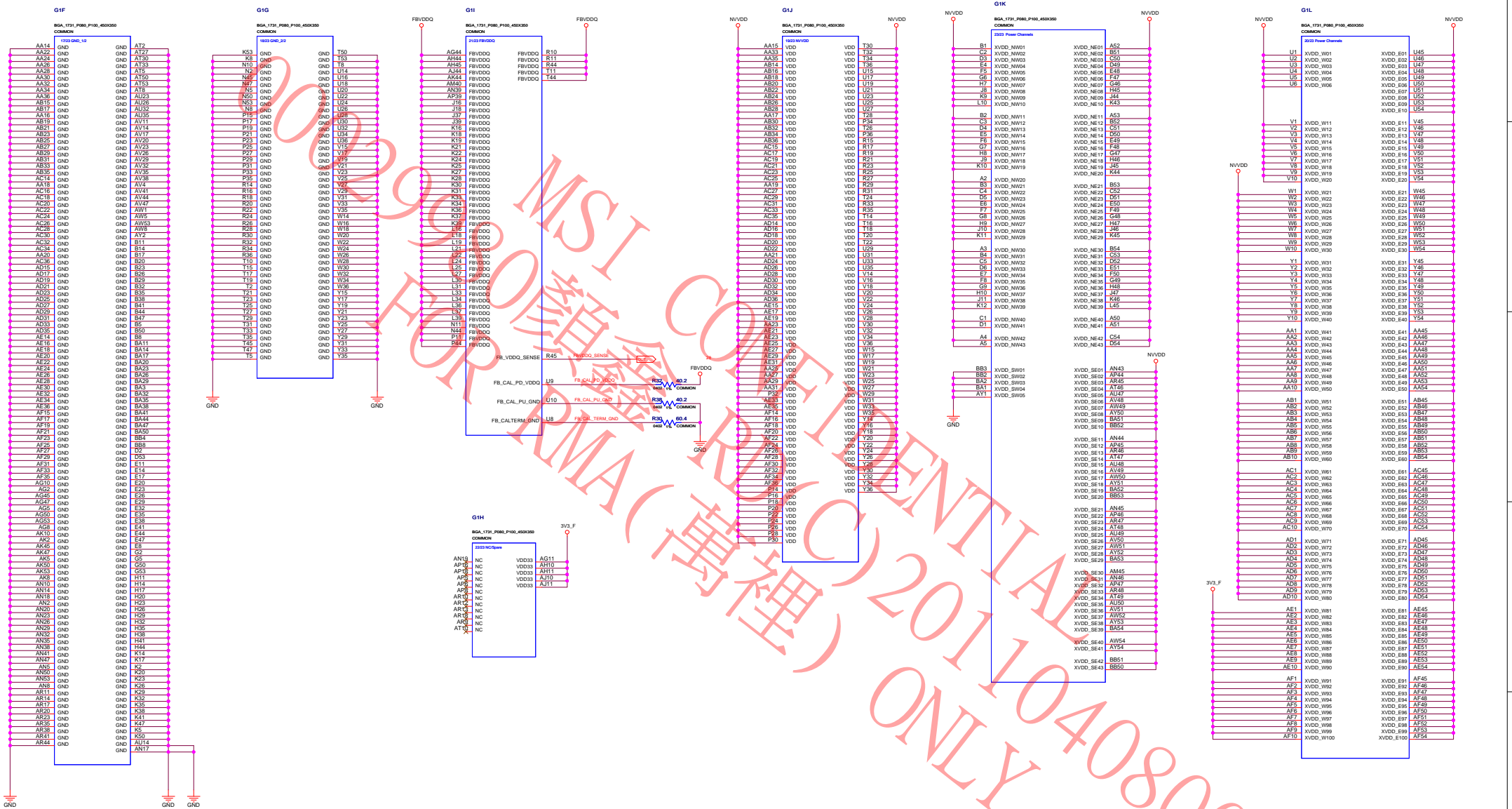
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FOR RMA(萬裡) RD(C) 2011040800
Remove NET ONLY

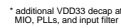
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MS-V260		
Size Custom	Document Description 空白	Rev 1.0
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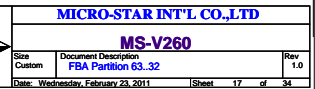
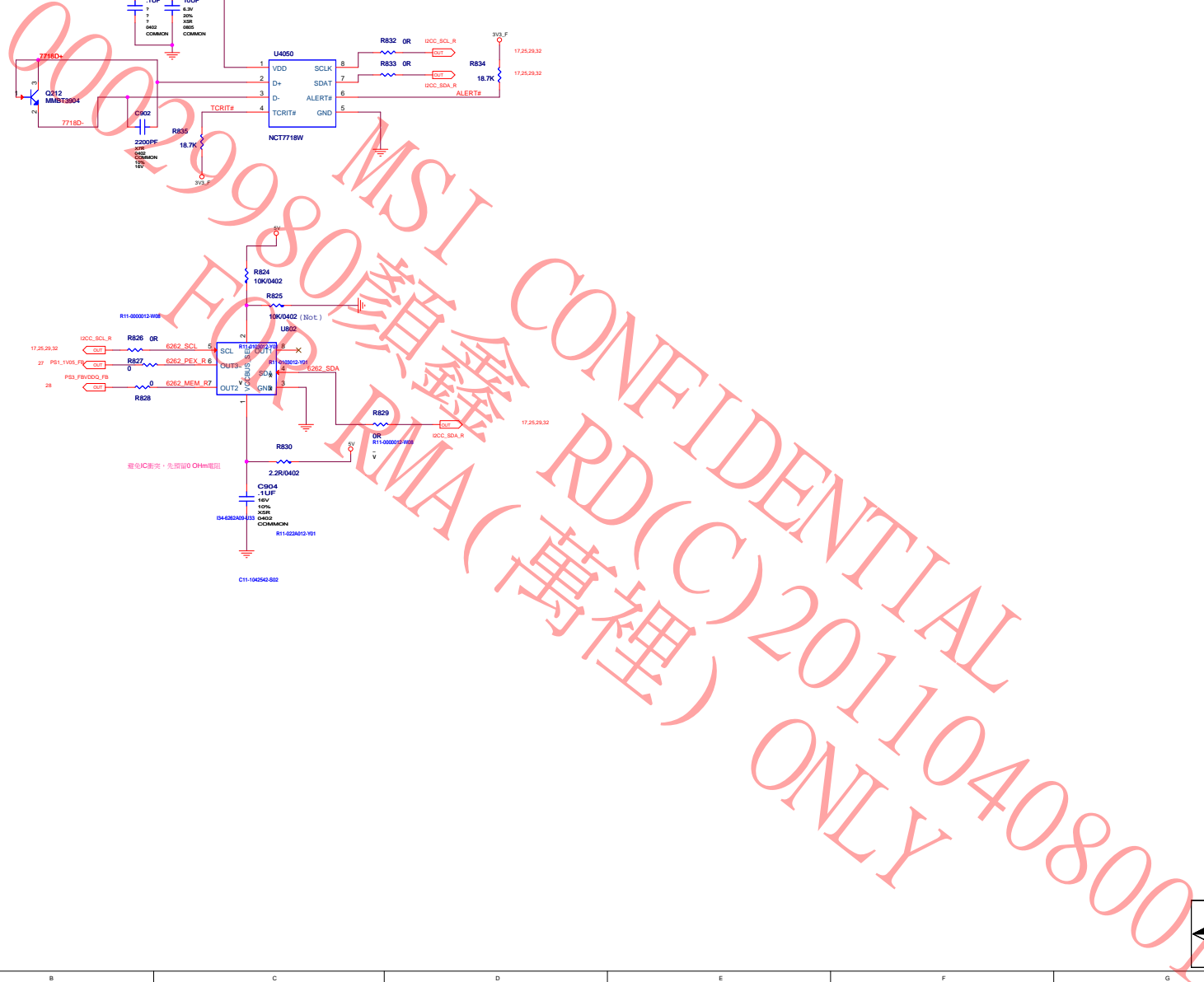
** Power channels are configurable.

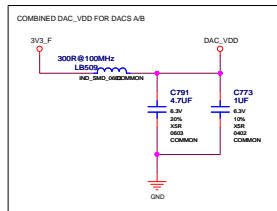
XVDD_.* pins are not connected on the substrate.

Therefore, XVDD_.* pins can be assigned as needed.

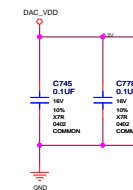






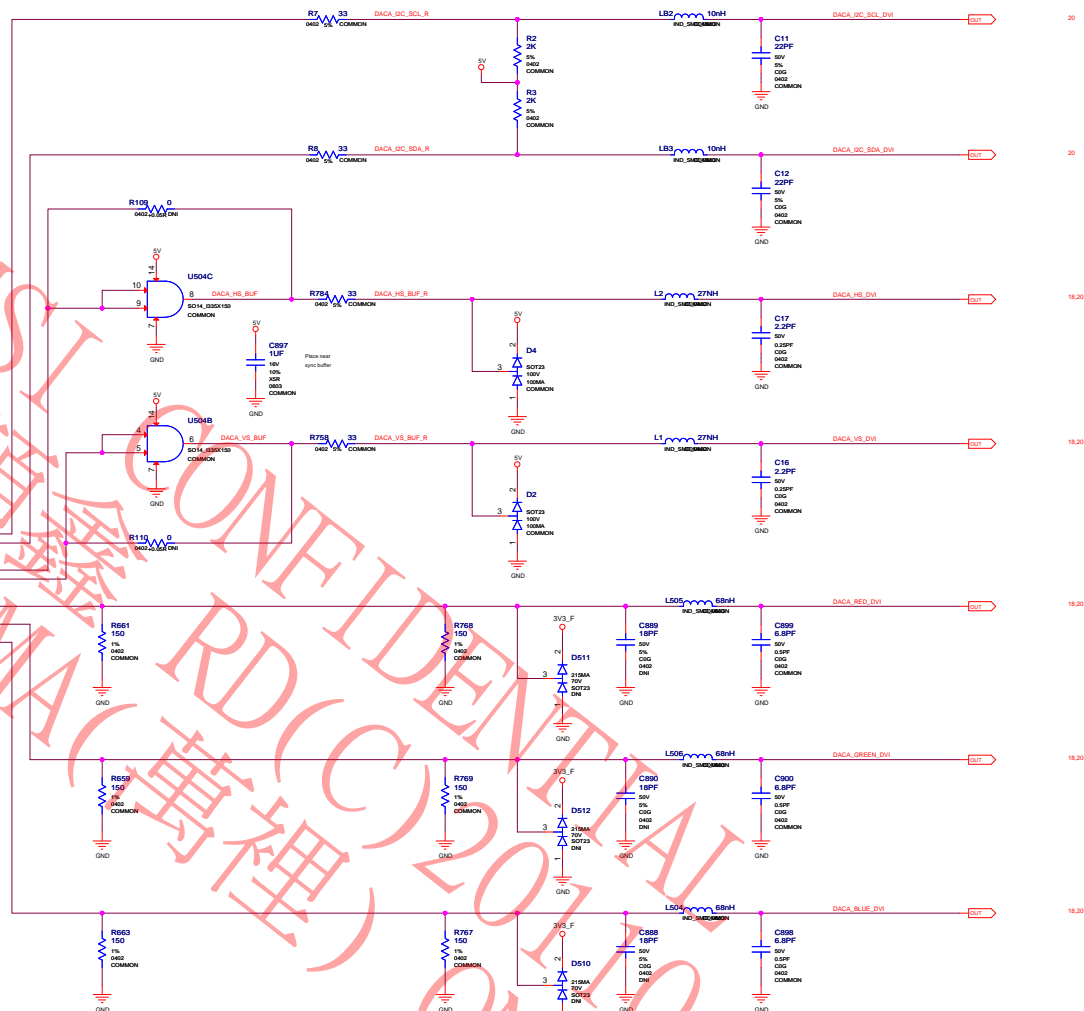


COMMON DAC_VDD FOR DAC A/B

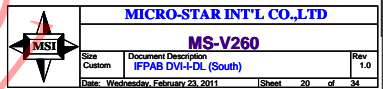


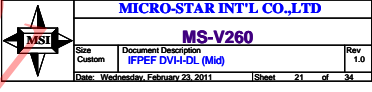
DACA NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE
DACA_RED_DVI	1	50OHM
DACA_GREEN_DVI	1	50OHM
DACA_BLUE_DVI	1	50OHM
DACA_HS_DVI	2	50OHM
DACA_VS_DVI	2	50OHM



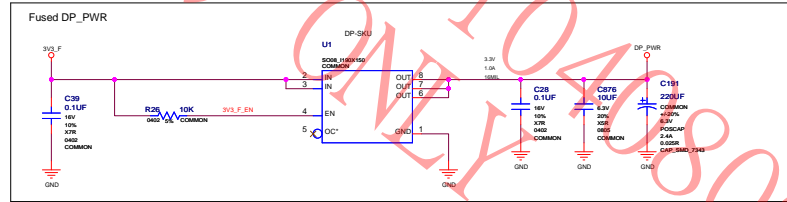
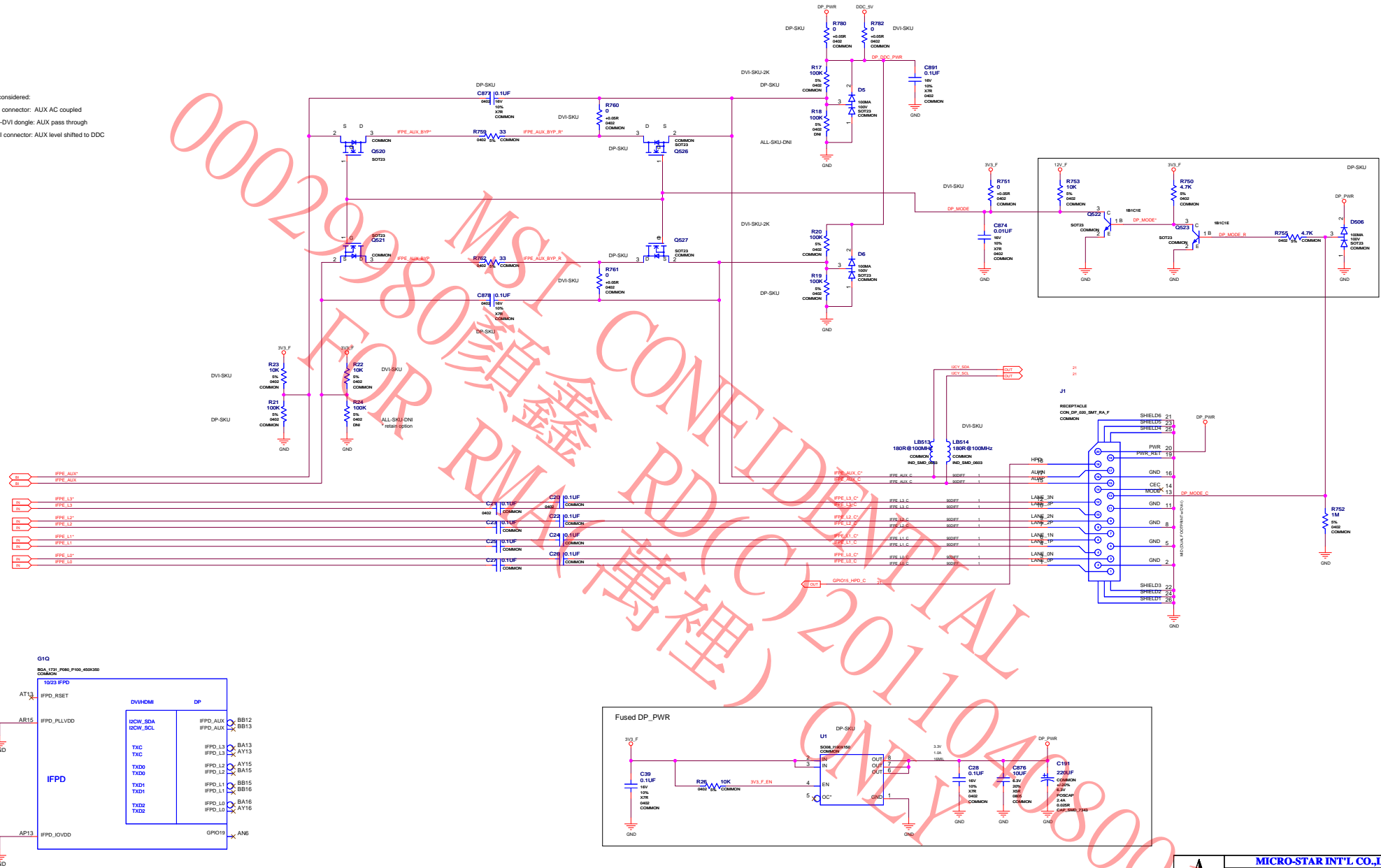
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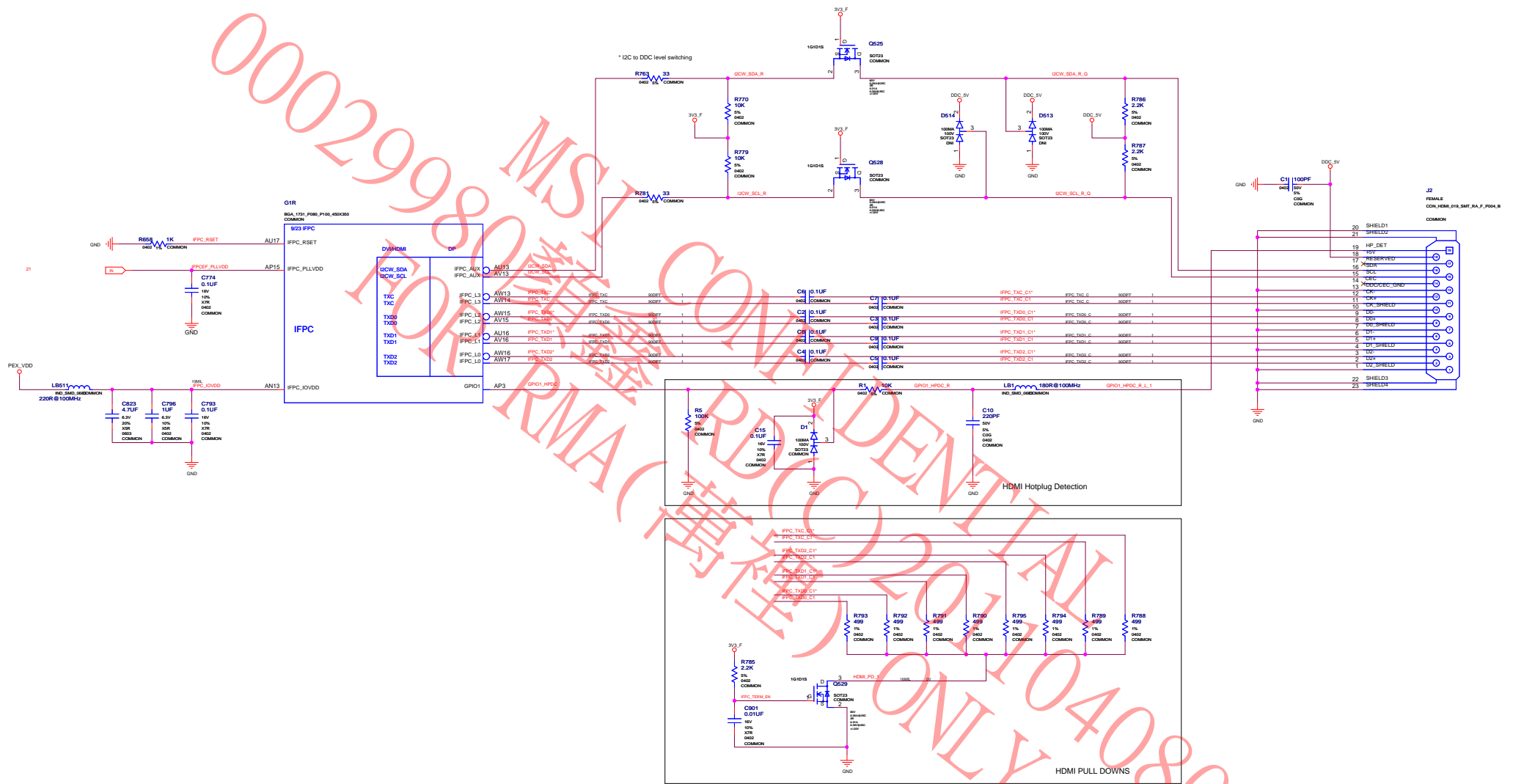


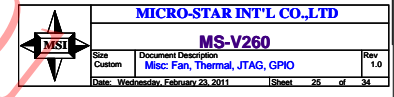
Three cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through
3. DP AUX to DVI connector: AUX level shifted to DDC



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Page26: Misc: ROM, HDCP, XTAL, Straps

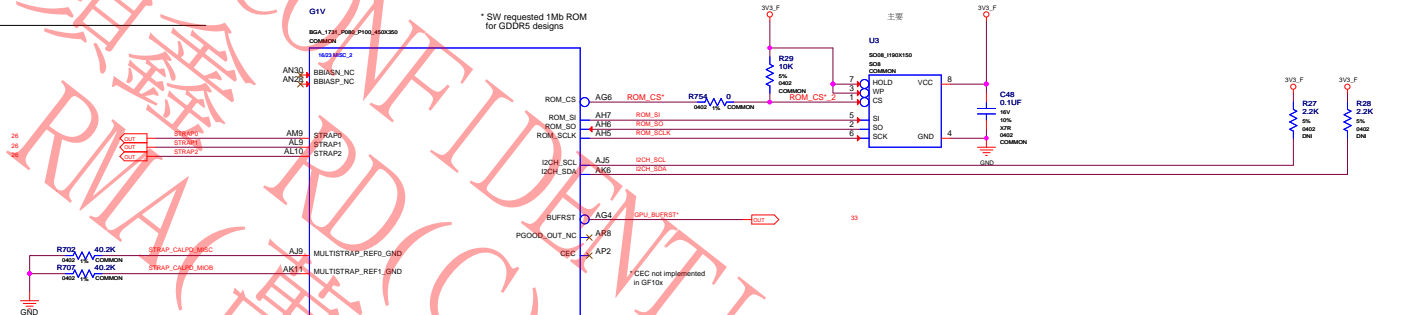
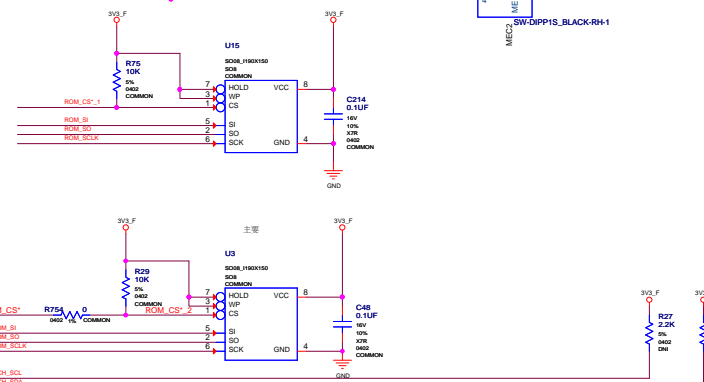
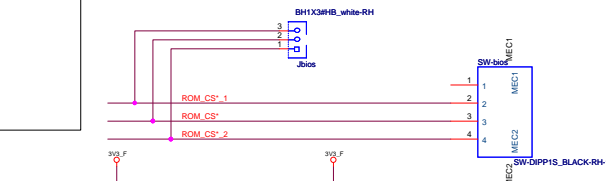
STRAP0	USER_BIT [3..0]	0000 => 5K PD	
STRAP1	3GIO_PADCFG_LUT_ADR	0000 =>5K PD	0000 Desktop
STRAP2	PCI_DEVID [3..0]	0000 For 0x1200 => 5K PD 0001 For 0x1201 => 10K PD	-400 GPU
ROM_SI	RAMCFG[0]	32Mx32 256 bit Hynix for SMU 01/050 second memory 0110 PD 10K	
	RAMCFG[1]	32Mx32 256 bit Samsung for SMU 01/050 first memory 0111 PD 20K	
	RAMCFG[2]	64Mx32 256 bit Hynix for SMU 2 second memory 0110 PD 20K	
	RAMCFG[3]	64Mx32 256 bit Samsung for SMU 2 first memory 0111 PU 40K	
ROM_SO	VGA_DEVICE	1	
	SMB_ALT_ADDR	0	10k PD
	FB[0]_BAR_SIZE	0	
ROM_SCLK	XCLK_417	0	
	PEX_PLL_EN_TERM100	1 ENABLED	
	SLOT_CLK_CFG	1 ENABLE	45K PD
	SUB_VENDOR	1 Dedicated BIOS	
	PCI_DEVID_EXT[4]	0 0x0	

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

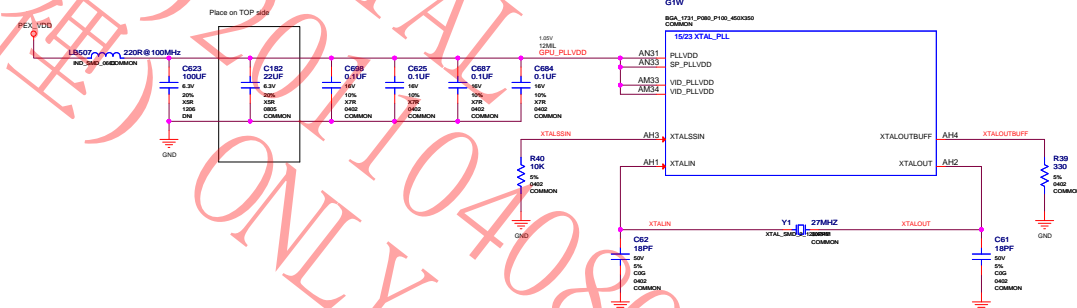
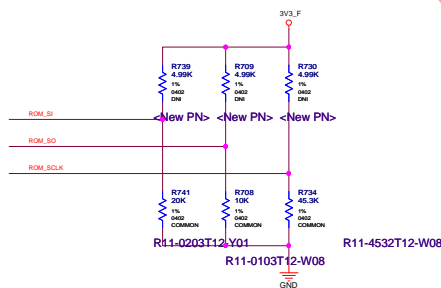
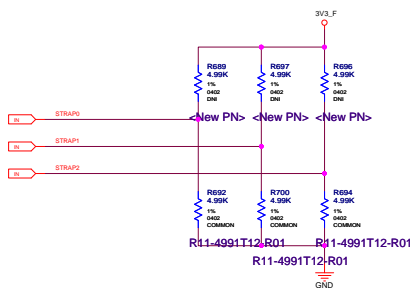
CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	32Mx32 256-bit Qimonda		
0010	32Mx32 256-bit Hynix		
0011	32Mx32 256-bit Samsung		
0100	Reserved		
0101	64Mx32 192-bit Qimonda		
0110	64Mx32 256-bit Hynix		
0111	64Mx32 256-bit Samsung		
1000	Reserved		
1001	32Mx32 192-bit Qimonda		
1010	32Mx32 192-bit Hynix		
1011	32Mx32 192-bit Samsung		
1100	Reserved		
1101	64Mx32 192-bit Qimonda		
1110	64Mx32 192-bit Hynix		
1111	64Mx32 192-bit Samsung		

MISC NET RULES

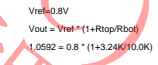
NET	NV_CRITICAL	NV_IMPEDANCE
-----	-------------	--------------




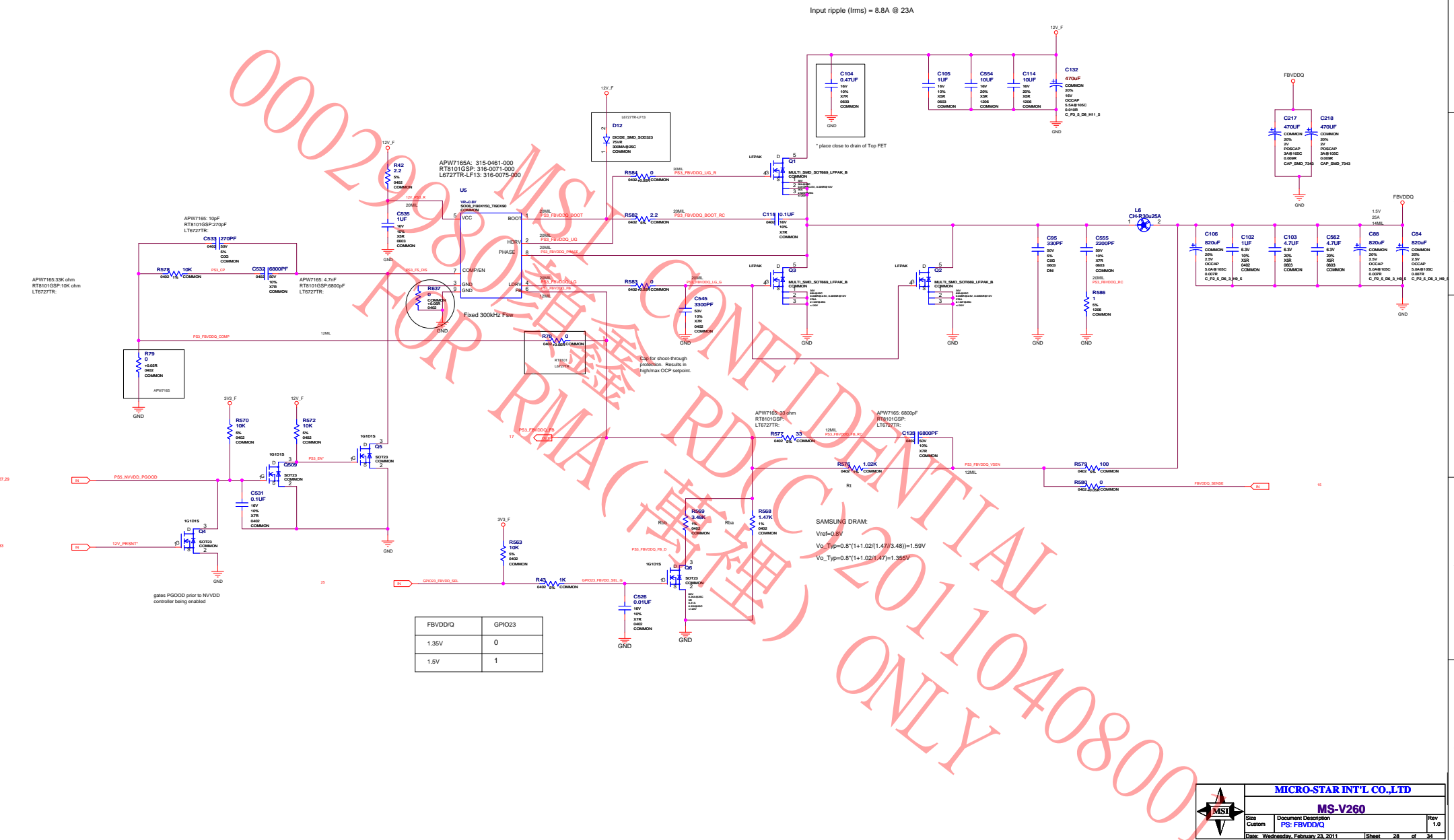
	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	45.2k 1% TO GND	NC
BINARY BRINGUP	NC	NC
MULTI-LEVEL	45.2k 1% TO GND	45.2k 1% TO GND

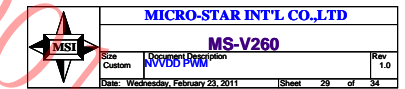


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Custom	ROM, HDCP, XTAL, Straps	1.0	
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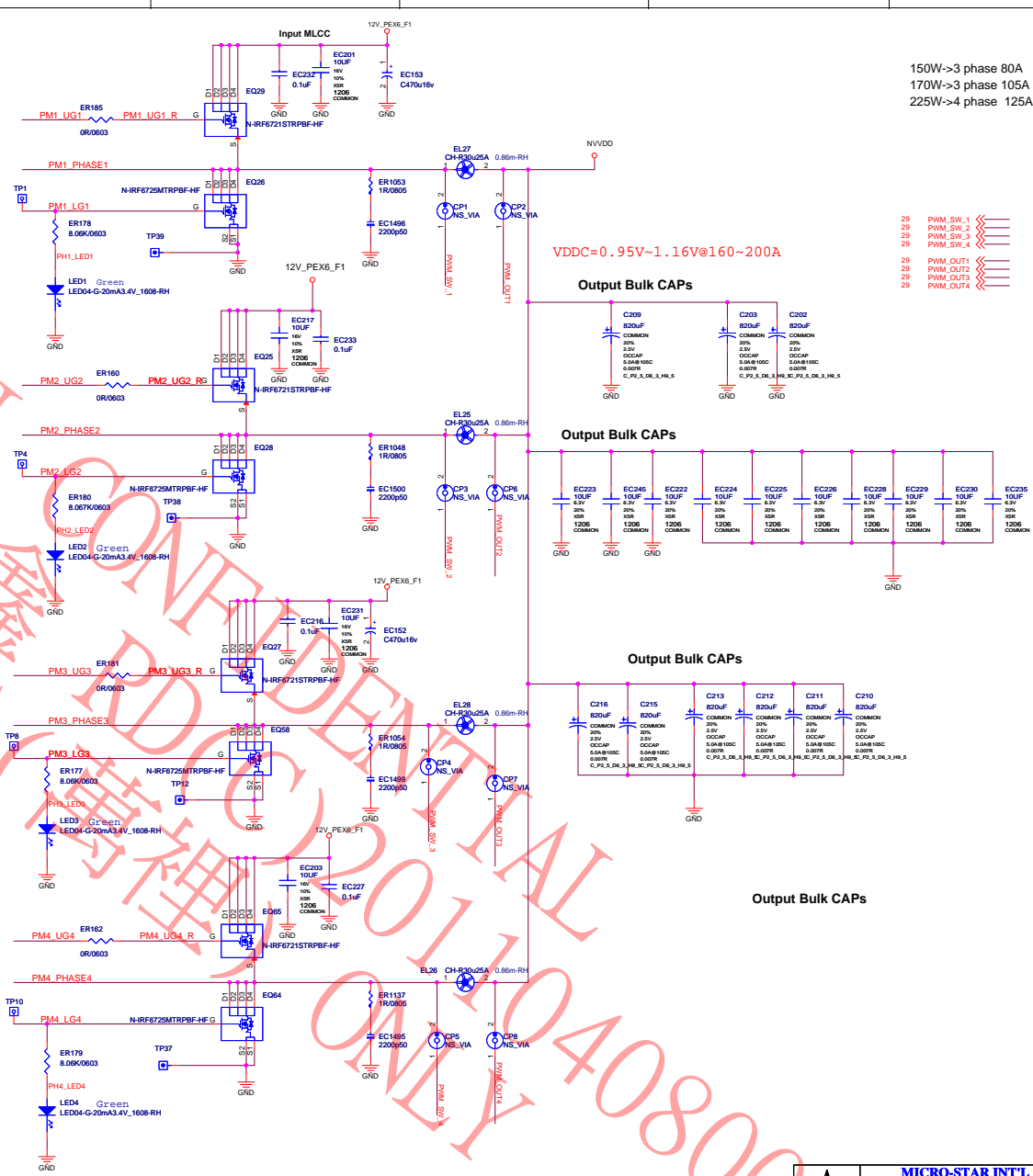
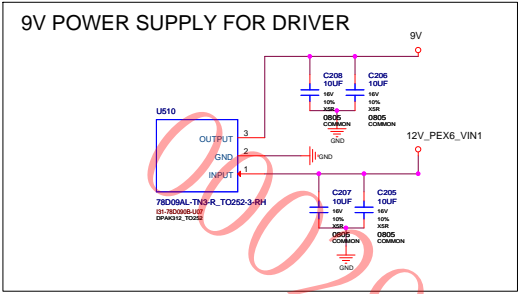


		MICRO-STAR INT'L CO.,LTD	
		MS-V260	
Size Custom	Document Description PS: 5V, PEX_VDD	Rev 1.0	
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Power Supply: NVVDD PHASE 1,~4

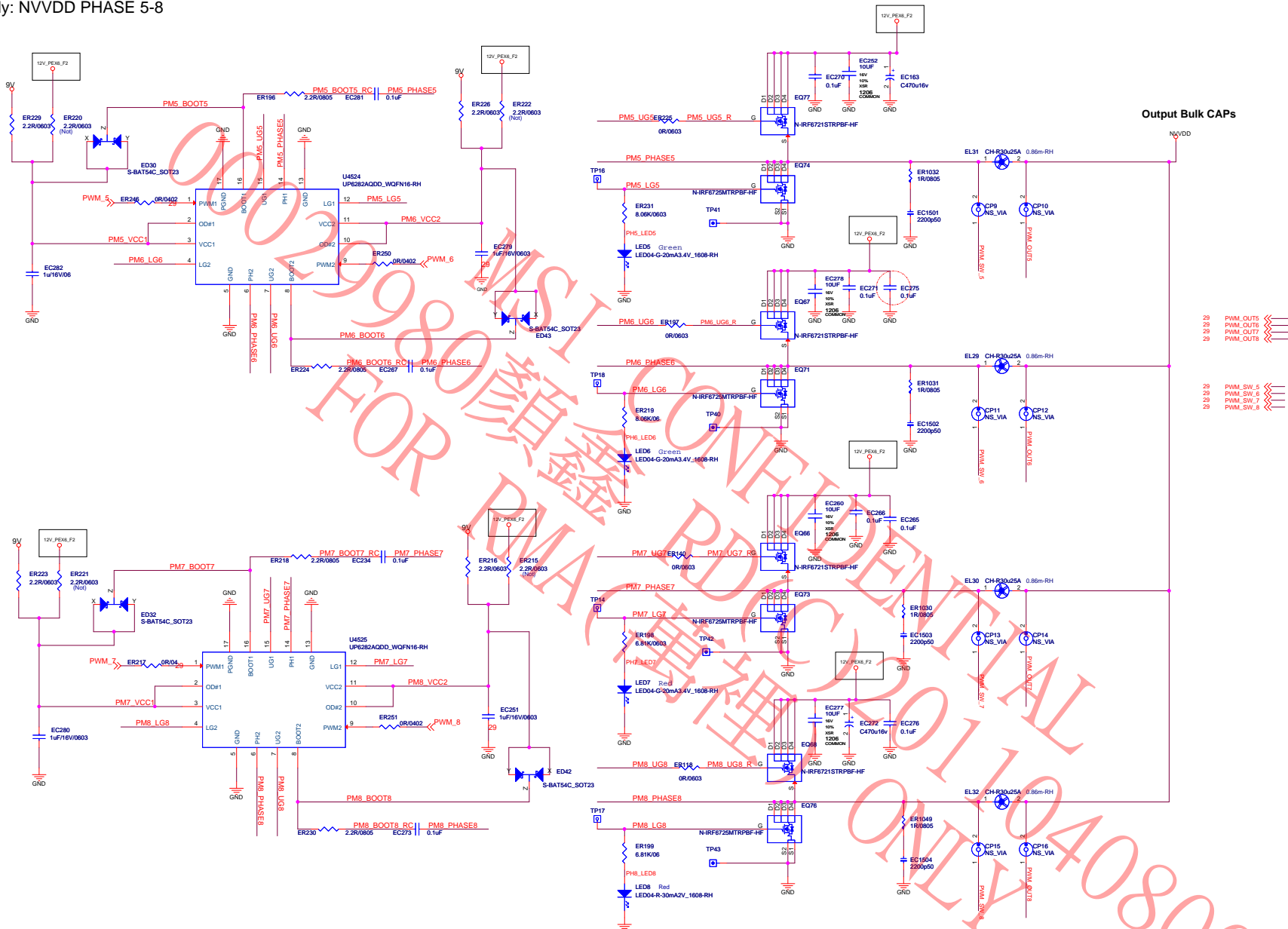



150W->3 phase 80A
170W->3 phase 105A
225W->4 phase 125A

29 PWM_SW_1
29 PWM_SW_2
29 PWM_SW_3
29 PWM_SW_4
29 PWM_OUT1
29 PWM_OUT2
29 PWM_OUT3
29 PWM_OUT4

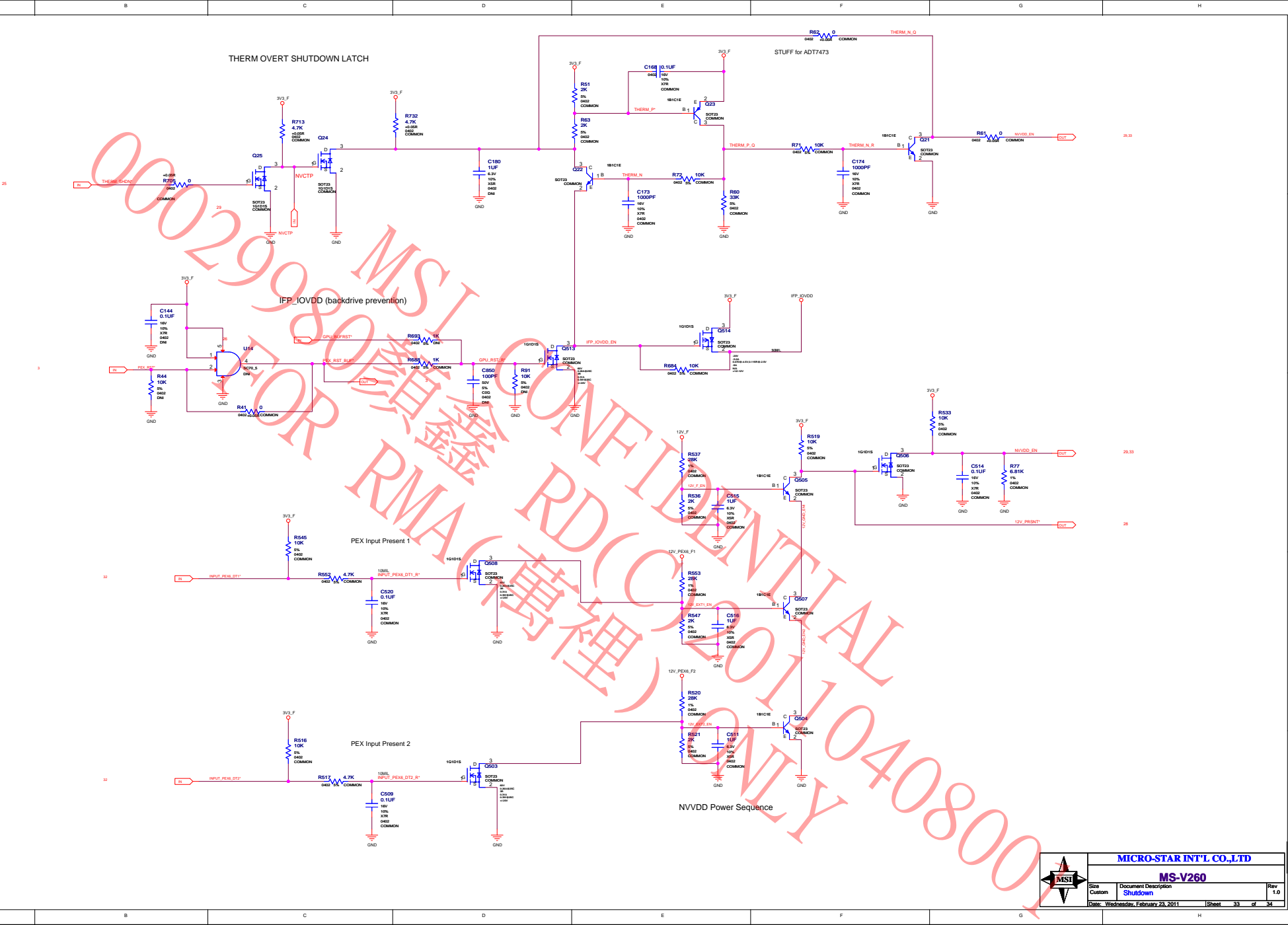
MICRO-STAR INT'L CO.,LTD		
MS-V260		
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Custom	NVVDD PHASE 1,~4	1.0
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Power Supply: NVVDD PHASE 5-8



	MICRO-STAR INT'L CO.,LTD		
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	NV/DD PHASE 5-8		
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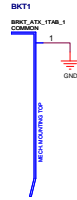




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Custom	Shutdown	1.0
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Brackets:

Bracket with DVI_DP1_NHDM: 151-10001-0352-071
Bracket with DVI_DP1_NHDM: 151-10001-0353-071
Bracket with DVI_DP1: 151-10001-XXXX-XXX



Bracket Screw



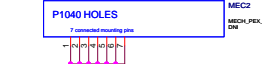
GPU Socket Symbol
* for bringup only



Bringup Cooler Symbol
* for bringup only

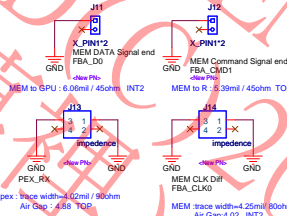
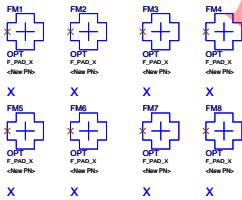


Mechanical Holes Symbol



Hockey Stick

SPECIAL MECHANIC
No connected mounting pins



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