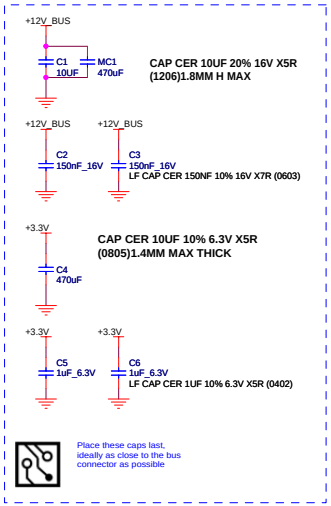
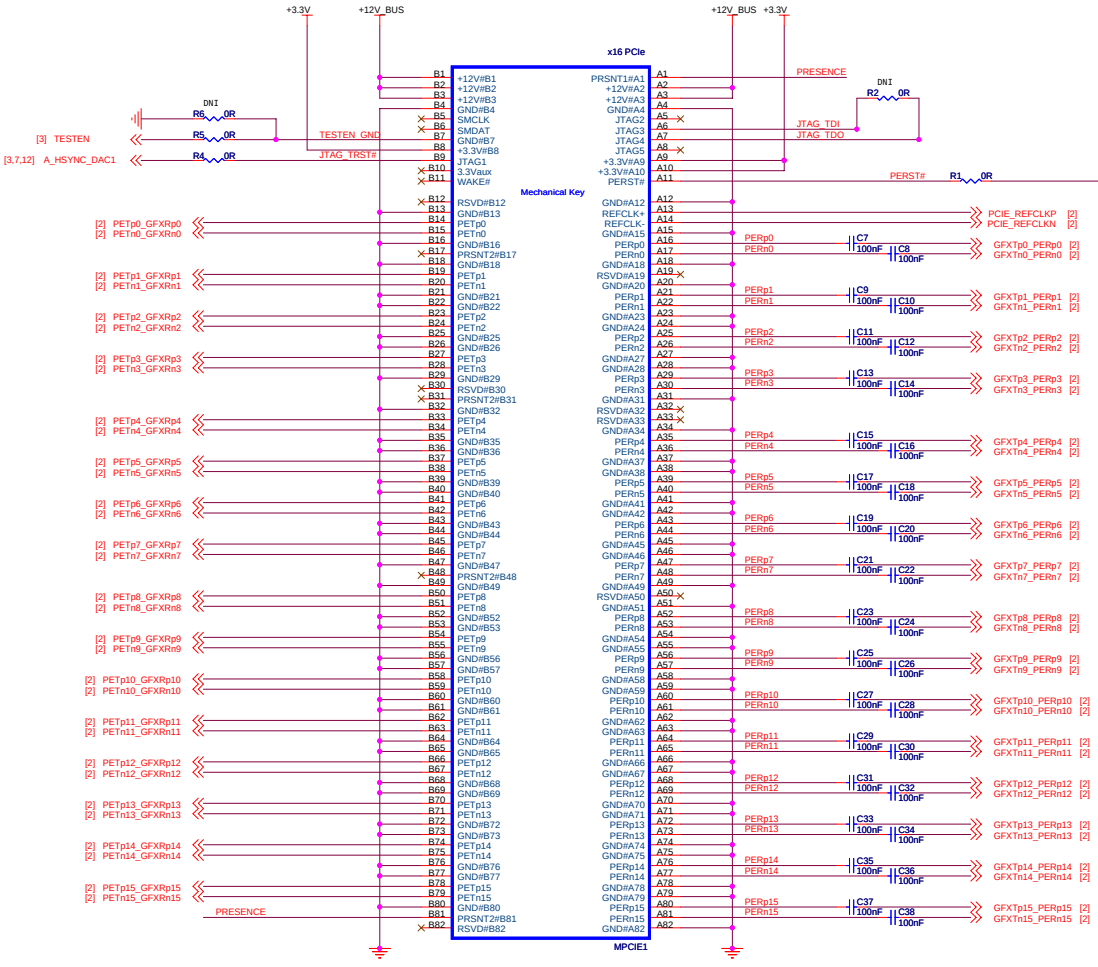
PCI-EXPRESS EDGE CONNECTOR





Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.
Pull-up may or may not be required on SMPS_EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

Typical trigger when +12V ramps above 10V (1.1V)

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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Size C	Document Number 105-A671xx-00B		Rev 1
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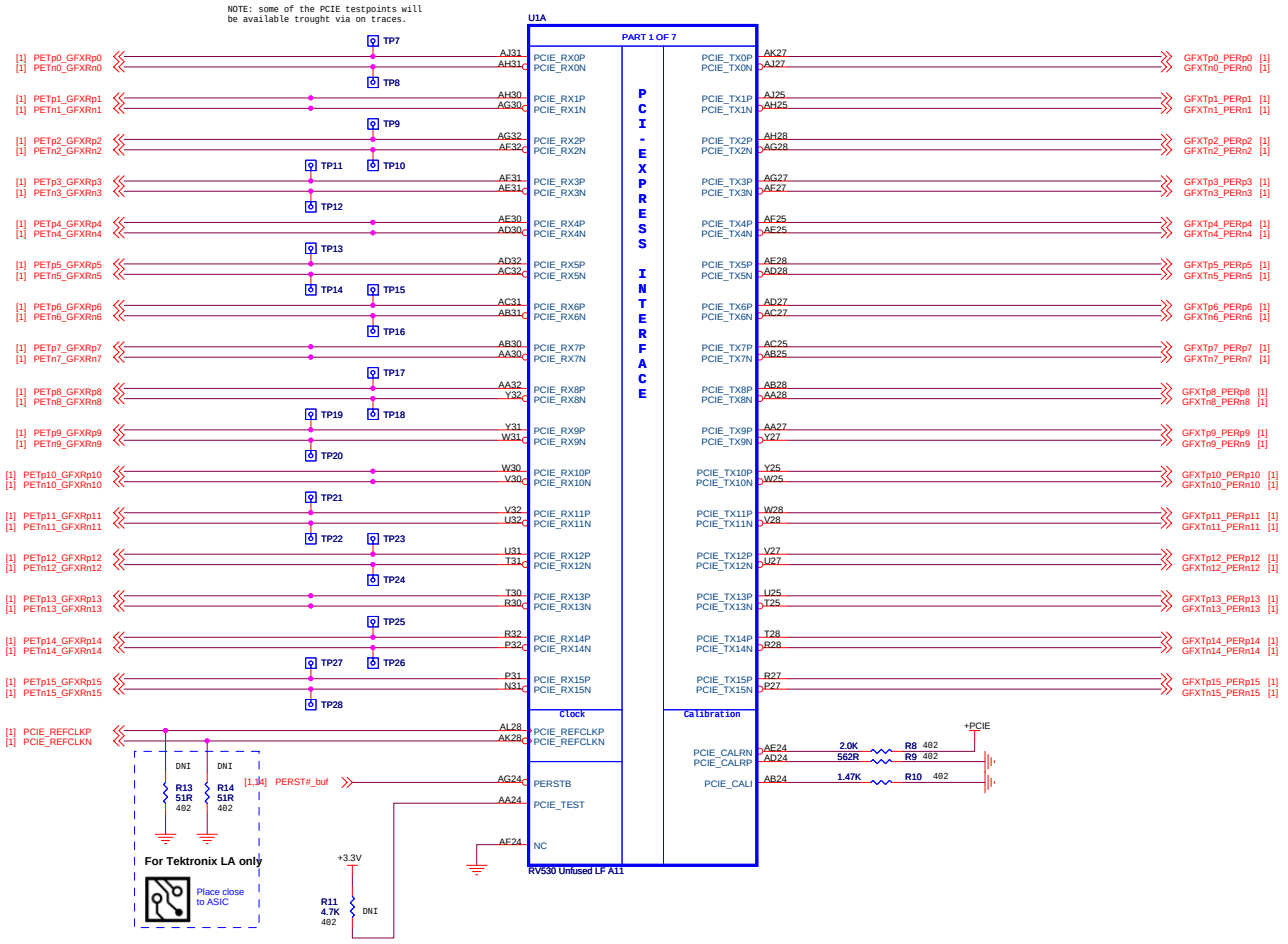

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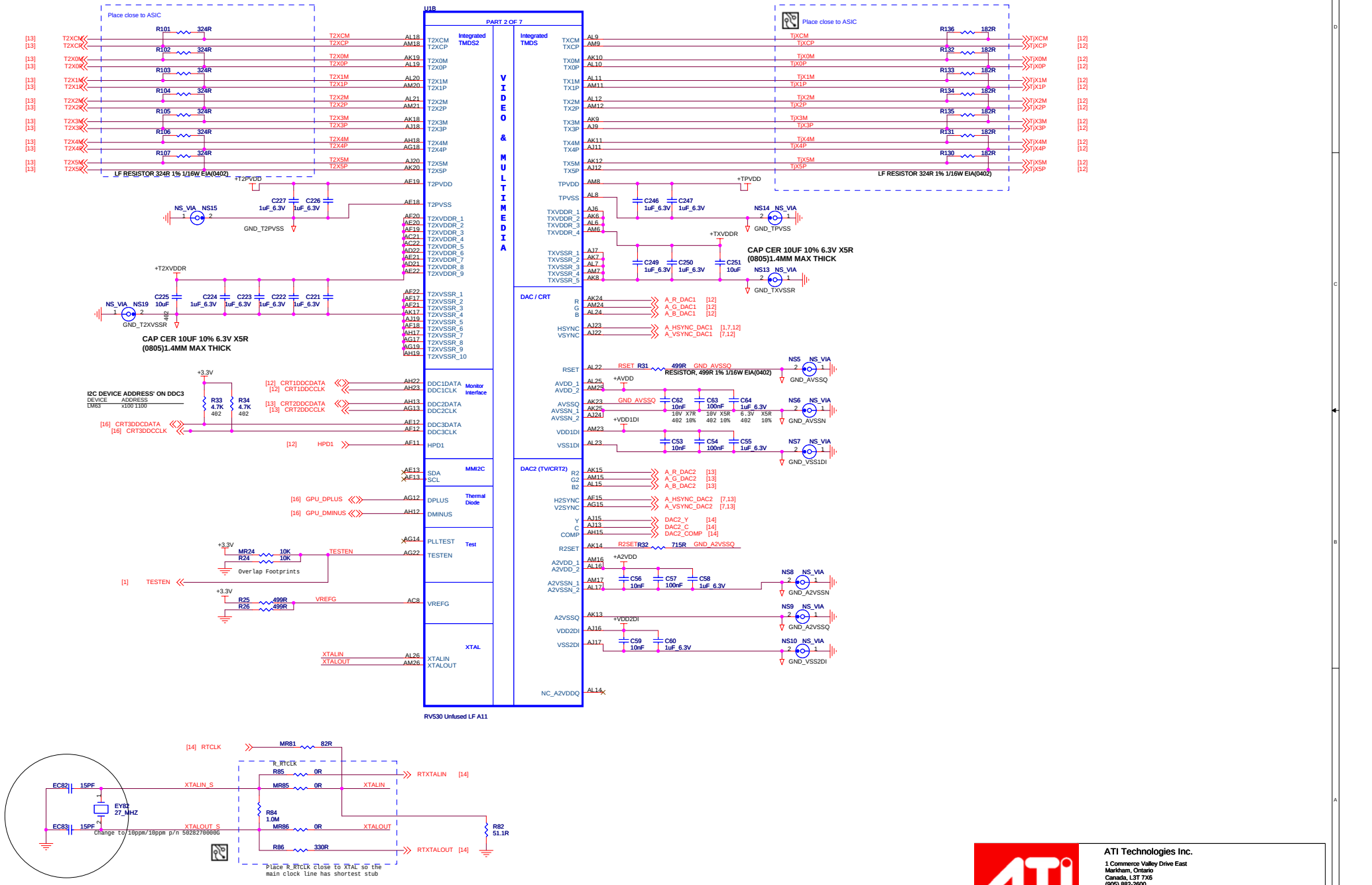

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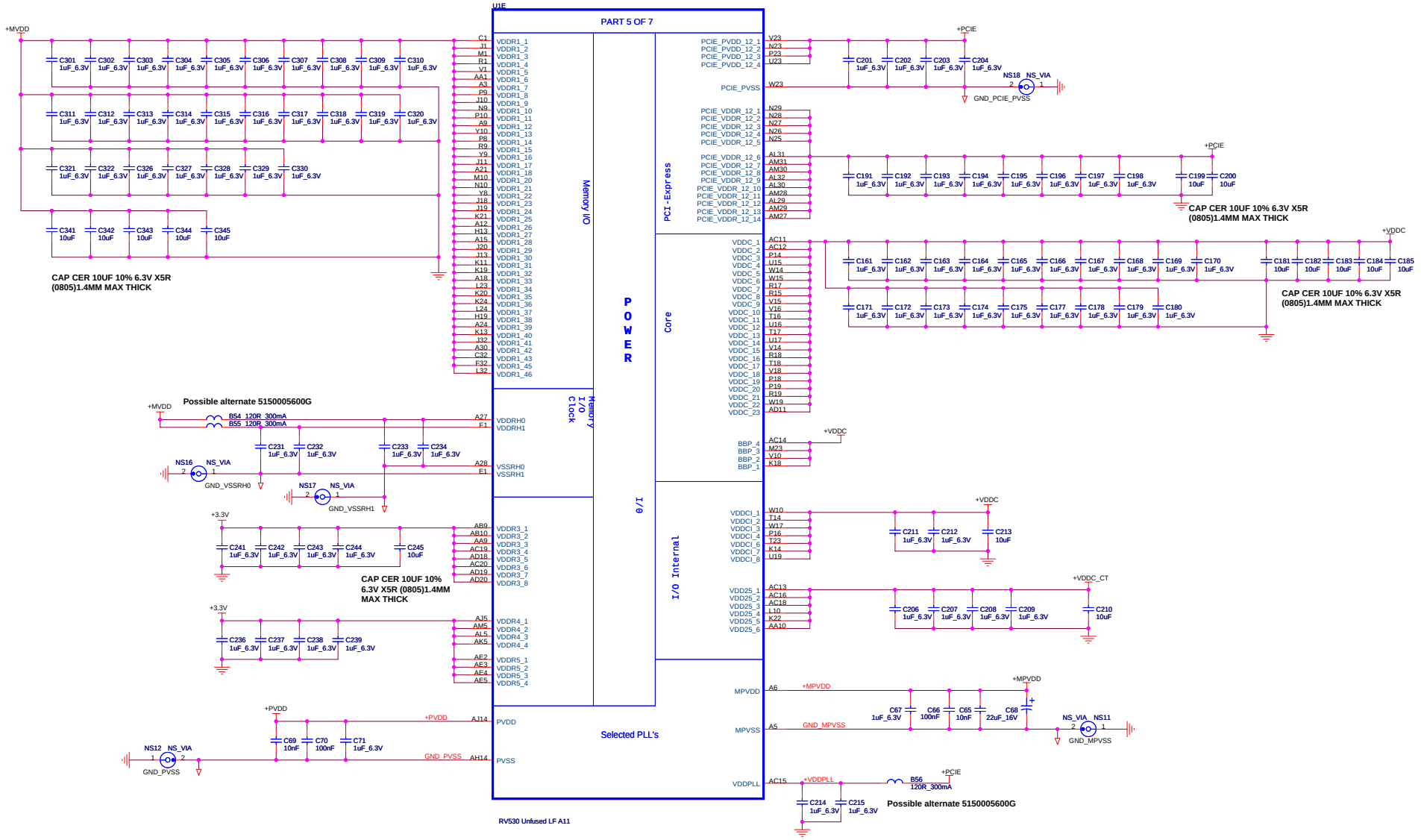

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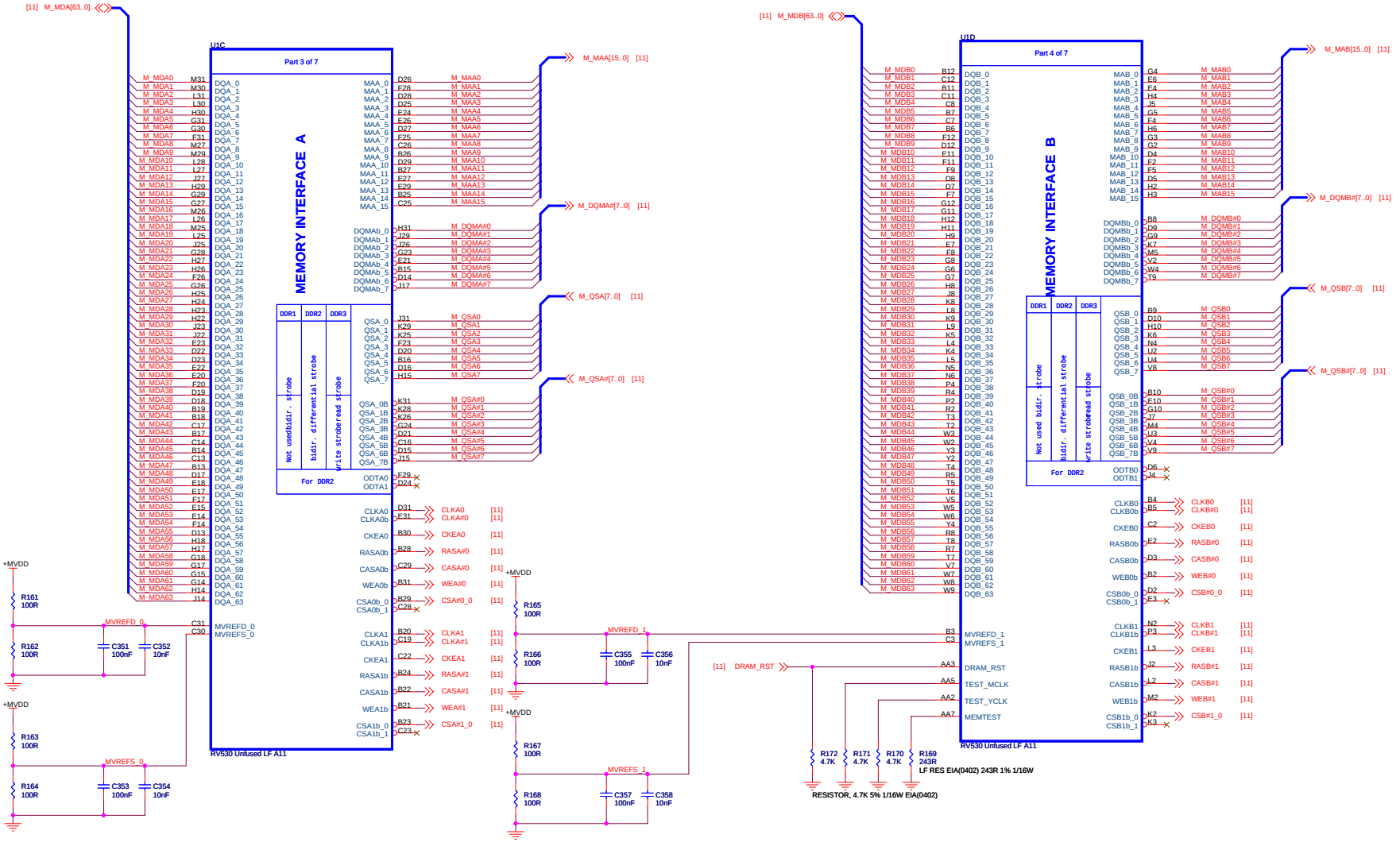

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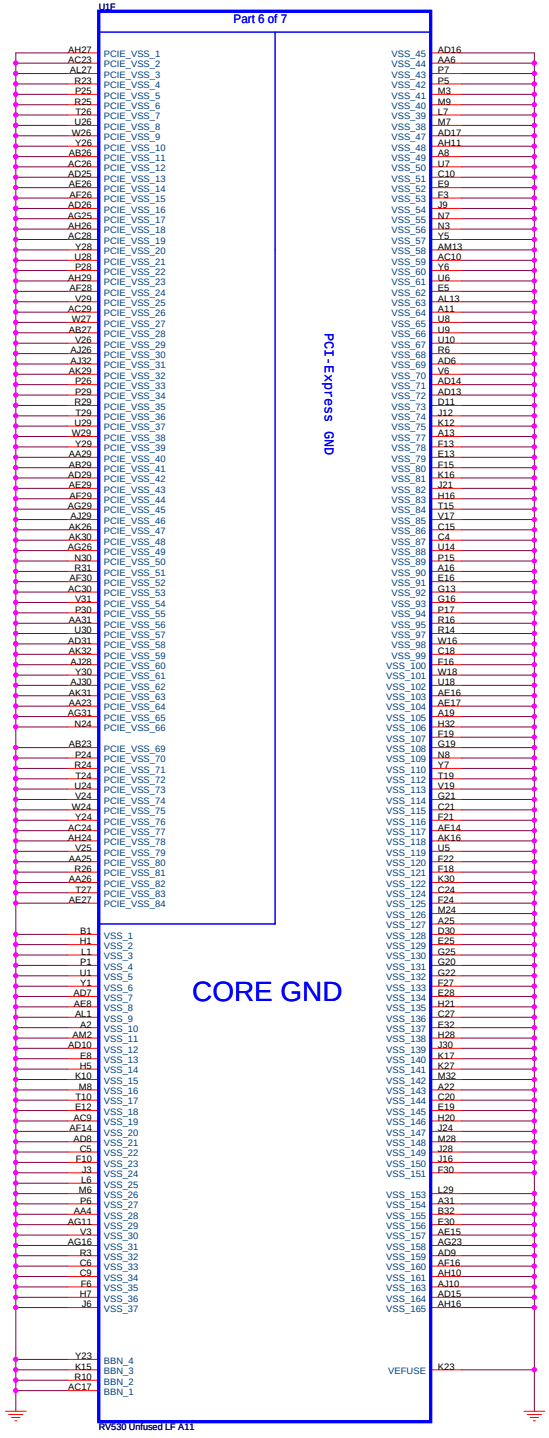

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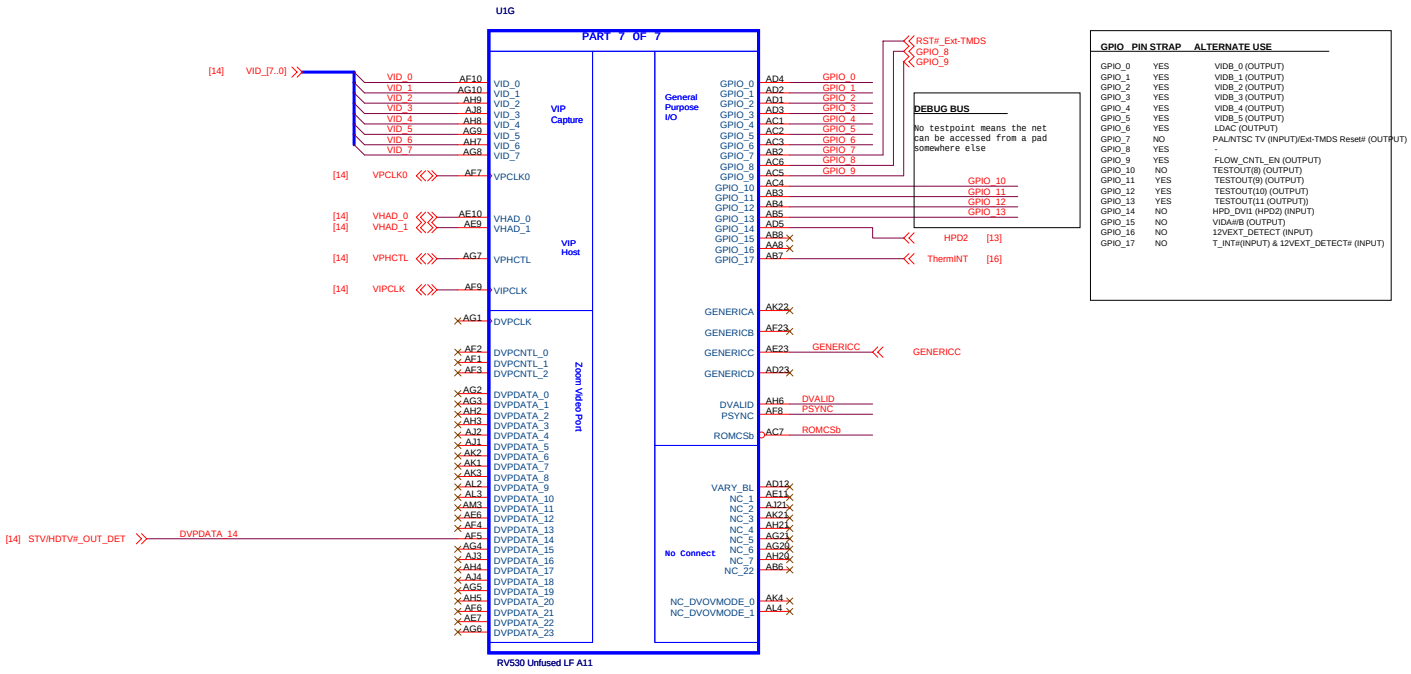
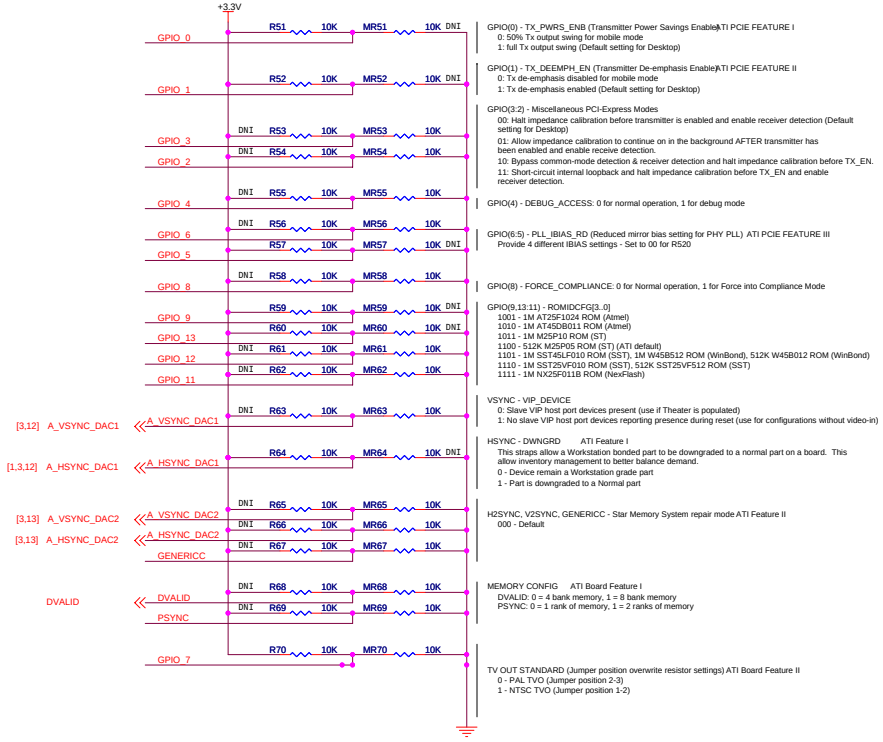
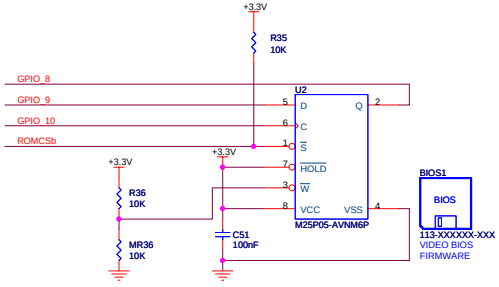


PIN BASED STRAPS





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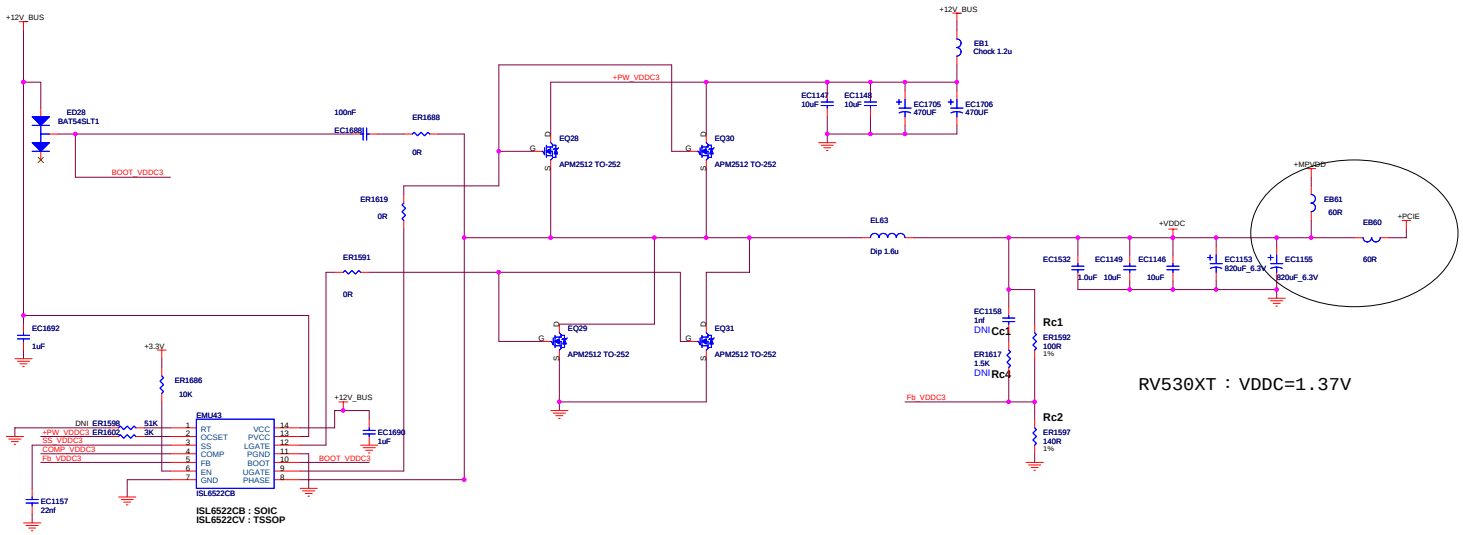
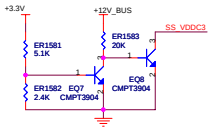
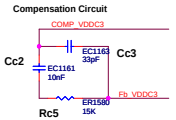
CORE REGULATOR VDDC



RV530XT : VDDC=1.37V

Lower MOSFET should be surrounded by
a lot of copper for heat dissipation

POWER SEQUENCING CIRCUIT:	DESIGN NOTES:
	
FOR ALTERNATE #1 Remove R374, R375, R371, C168 and U32 Install R370, R112, R954, R305-R308, C160 C159 and MU32	**FOR ALTERNATE #2** Change C157 for 10 uF and C121 for 1 uF Replace C764 by 0 Ohm resistor Replace R314 with a bead Remove R954, R370, R305-R308, C159, R112, C160 and MU32 Install R374, R375, R371, C168 and U32 **Compensation circuit** Rc1 = 10K, Rc2 = 8.06K R313 = 93.1K, C171 = 3.9 nF, C170 = 10 pF

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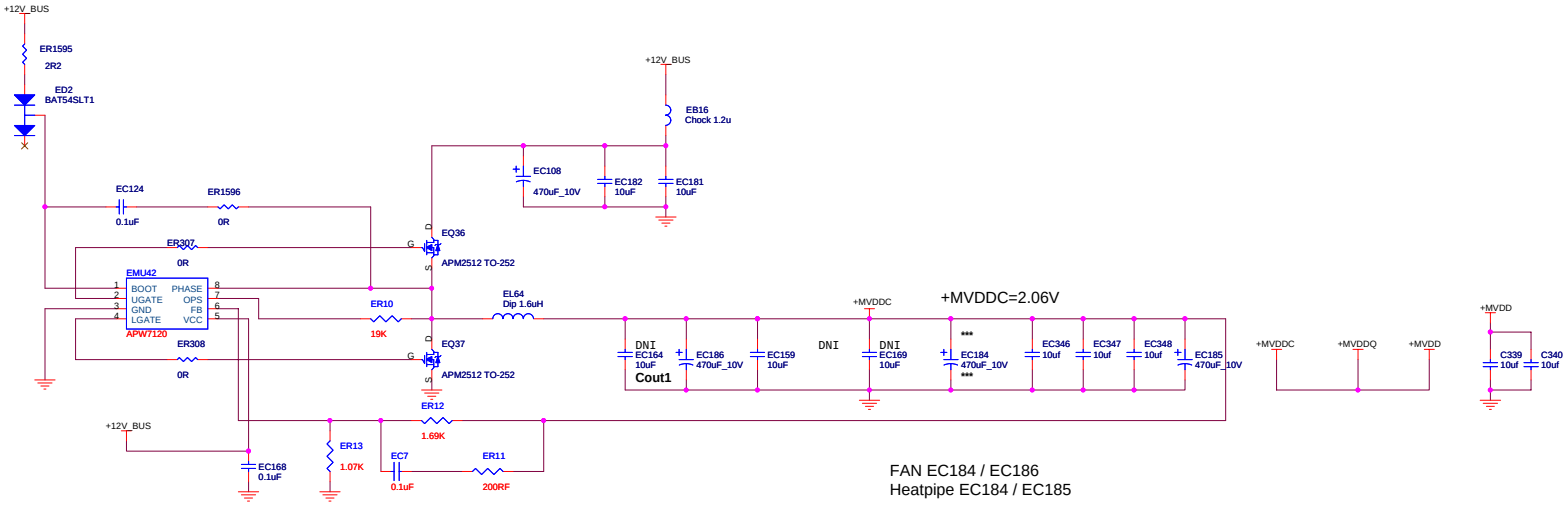

FAN EC184 / EC186
Heatpipe EC184 / EC185

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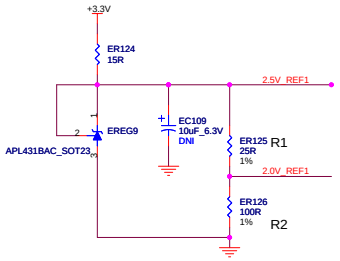
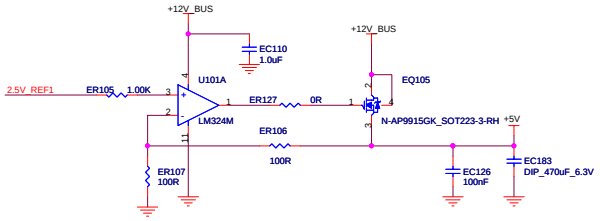
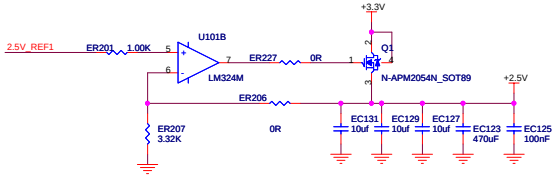
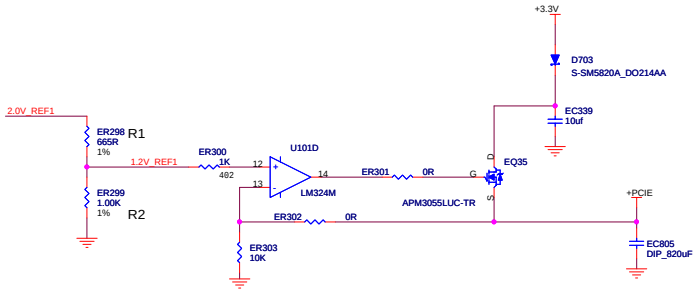
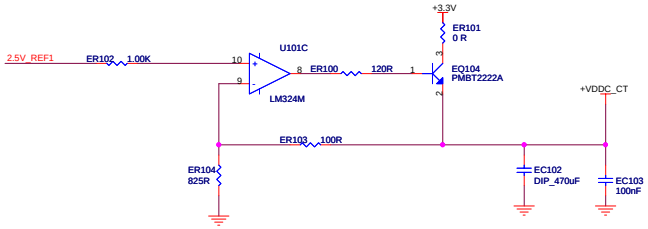


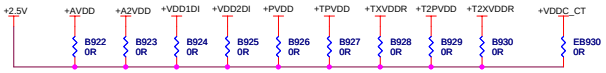








For RV530XT VDDC_CT=2.8V



Replace with 5050004800
120R, 300MA EIA(0402)

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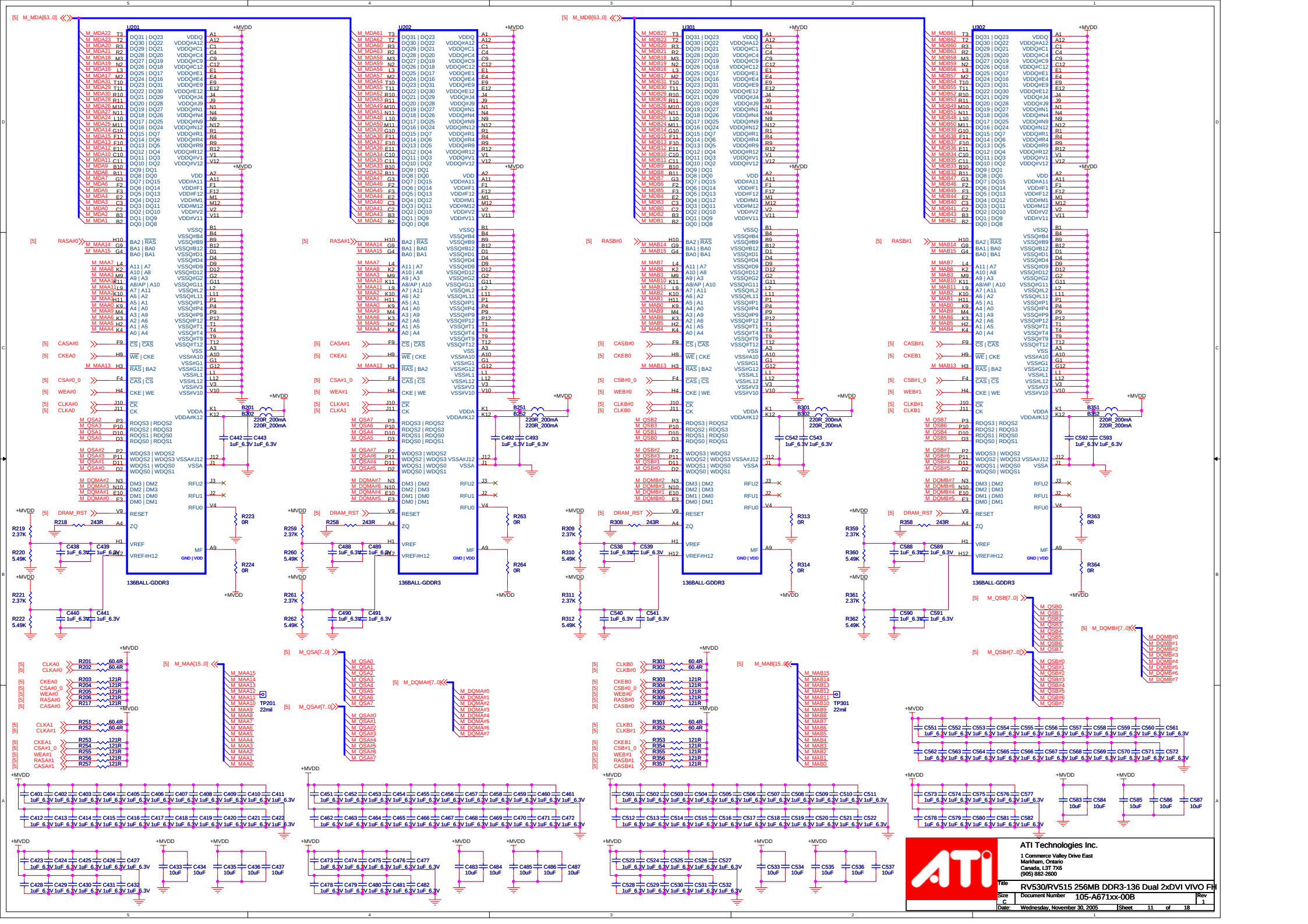
U201
U202
U301
U302
136BALL-GDDR3
M_MDA[63..0]
M_MDB[63..0]
RASA#0
RASA#1
RASB#0
RASB#1
CASA#0
CASA#1
CASB#0
CASB#1
CKEA0
CKEA1
CKEB0
CKEB1
WEA#0
WEA#1
WEB#0
WEB#1
CLKA0
CLKA#0
CLKA1
CLKA#1
CLKB0
CLKB#0
CLKB1
CLKB#1
DRAM_RST
+MVDD
220R_200mA
M_QSA[7..0]
M_QSB[7..0]
M_MAA[15..0]
M_MAB[15..0]
M_DQMA#[7..0]
M_DQMB#[7..0]
TP201
TP301
22mil
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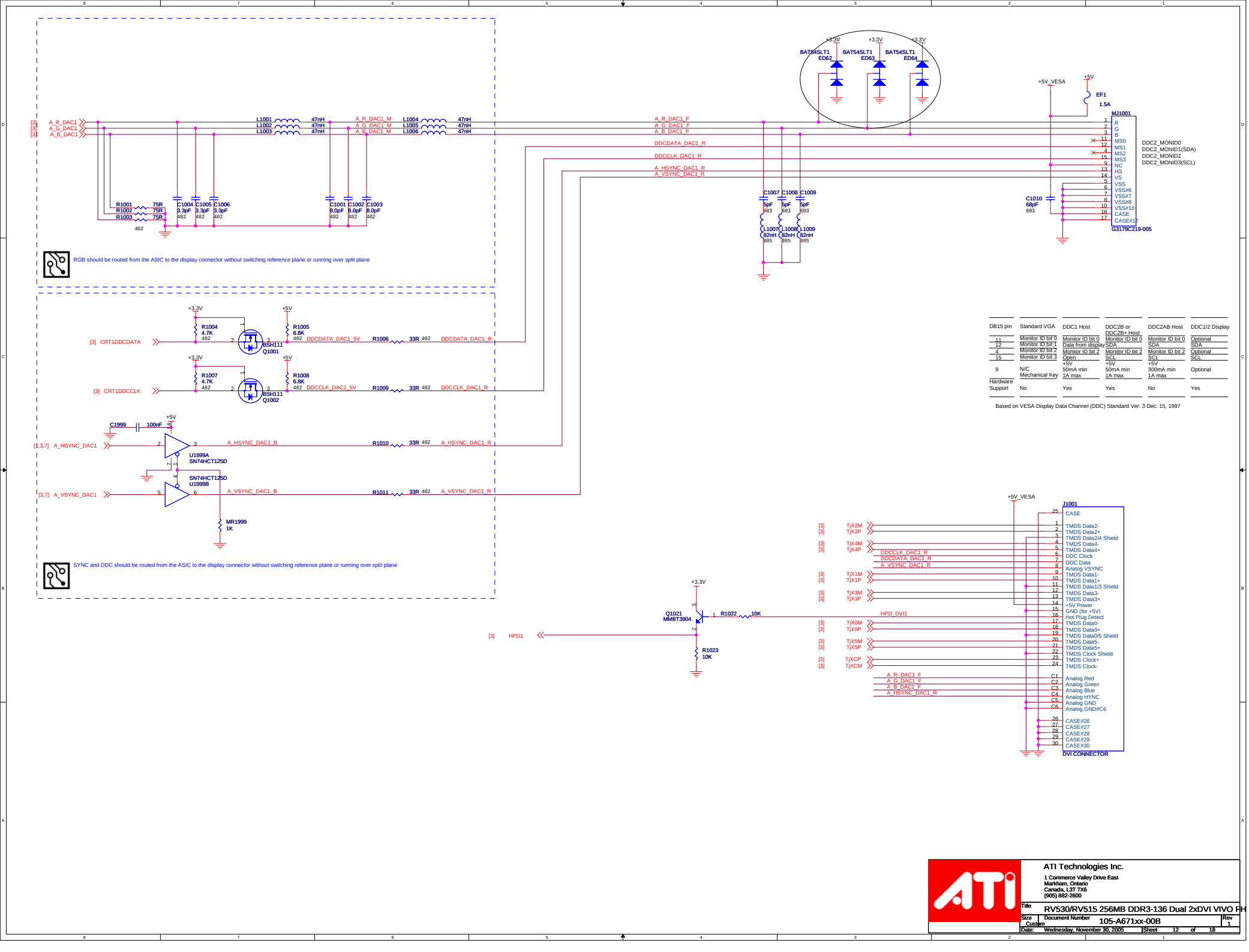

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
		+5V	+5V	+5V	
9	N/C	50mA min	50mA min	300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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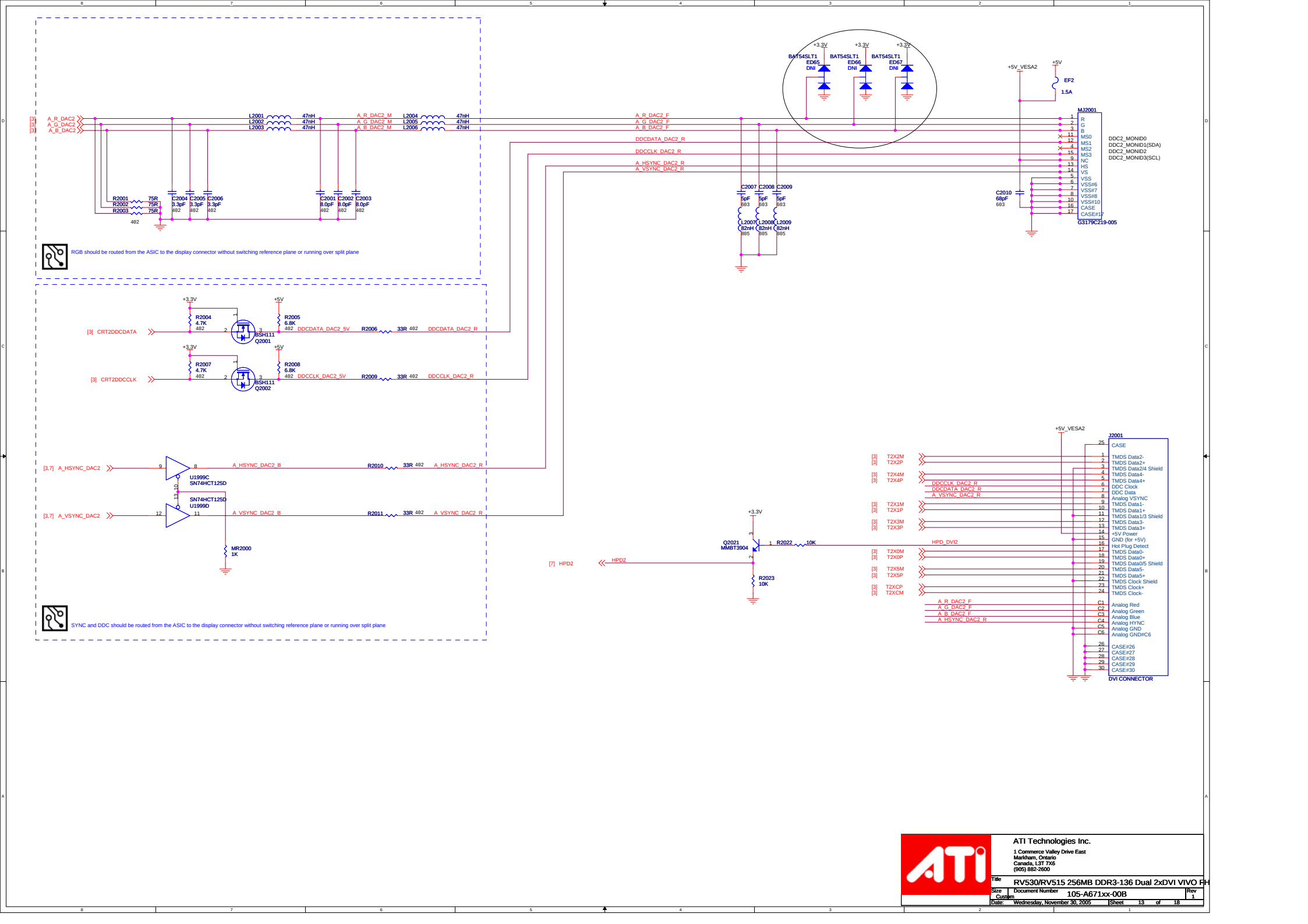

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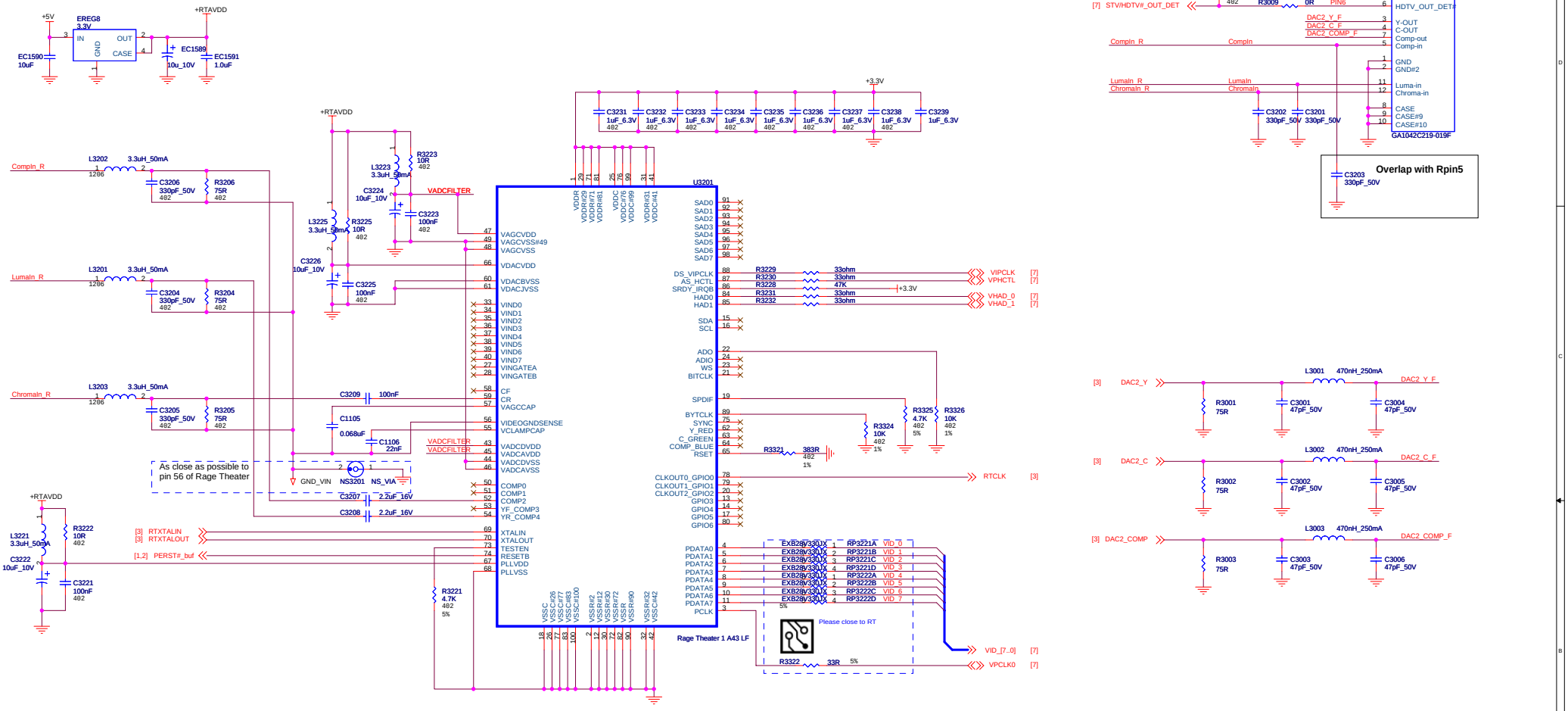
+RTAVDD
Vout = 3.3V
Iout = 125mA MAX, 80mA RMS



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DVI/VGA SCREWS

SCREW1
SCREW JACKSCREW ASSY 7020000800

SCREW2
SCREW JACKSCREW ASSY 7020000800

SCREW3
SCREW JACKSCREW ASSY 7020000800

SCREW4
SCREW JACKSCREW ASSY 7020000800

PCB

MT1
MT_Hole_0.136_in.
DNI

MT2
MT_Hole_0.136_in_6VIA
DNI

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM4 SW_FB
FM5 SW_FB
FM6 SW_FB

DNI
SK1
RV410SOCKET

H2
LOW PROFILE HS

BKT

J1 X_PIN1*2
J2 X_PIN1*2
J3 X_PIN1*2
J4 X_PIN1*2
J5 X_PIN1*2
J6 X_PIN1*2
J7 X_PIN1*2
J8 X_PIN1*2
J9 X_PIN1*2

<Variant Name>

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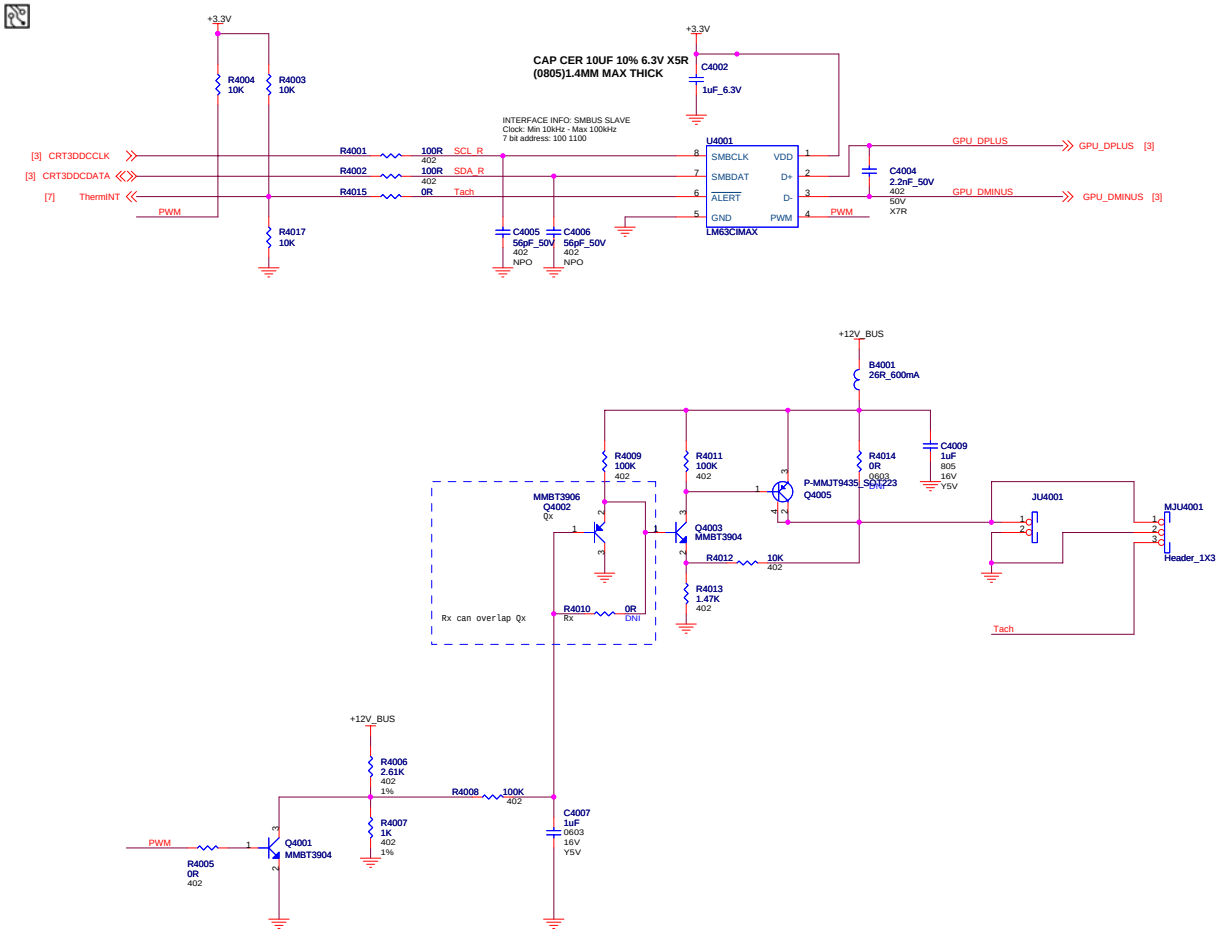

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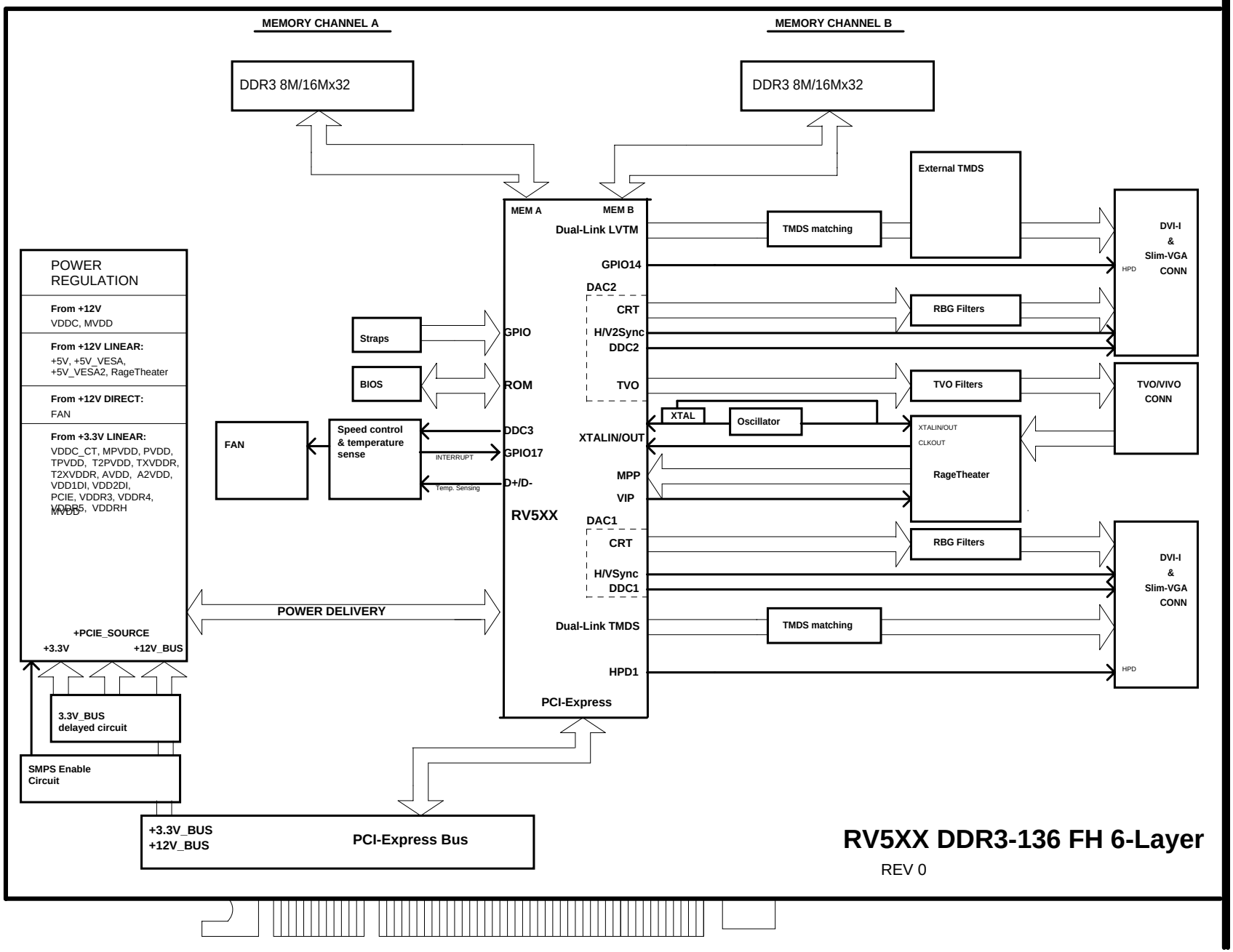

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<variant Name>

Title	Schematic No.	Date:
RV530/RV515 256MB DDR3-136 Dual 2xDVI VIVO FH	105-A671xx-00B	**Wednesday, November 30, 2005**

REVISION HISTORY

Rev 1

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
A	00A	05/07/20	Design based on A676-00B and memory of A675-00B (pg 01) Delete redundant SMPS_EN circuits (pg 03) Remove TMDS joins and add TMDS2 terminations (pg 04) Add 1.8V option for VDDR4 and VDDR5 (pg 05) Add additional separate MVREF, QS# and address; remove ODT for DDR2 (pg 07) Add DVO port and GPIO7 for ext TMDS reset (pg 11) Change power sequence circuit for +5V and add 1.8V power supply (pg 12) Add memory based on A675-00B (pg 13) Add ext TMDS HDCP support (pg 14) Remove HPD2 option (pg 15) Add 2nd DVI connector (pg 16) Remove C3241, C3242, C3243, C3244 and C3245. Remove +MVDDC/+MVDDQ reference, use only +MVDD
B	00B	09/14/05	Added crossfire slave requirements