NV15, 1/2MX32 TERMINATED DDR, RGB, INTERNAL DVI-I, AGP.

PCI DEVICE ID 0X0=0X150 FOR NV15.

STRAPS: AGP4X, SIDEBAND DIS, FAST WRITE ENA, ADP BIOS, NORMAL PCIAD, 14.318MHZ

SWITCHER1(VTT) SET TO 1.25V
SWITCHER2(NVVDD) SET TO 2.05V
LINEAR(FBVDDQ) SET TO 2.5V

HISTORY FROM REV. C01:

1) Updated BOM/Schematic Discrepancies.
2) Only Support Terminated DDR.
3) Removed External TMDS.
3) GNDed Unused DFP pins.
3) Added bracket and hex screws for DVI connector.
4) Re-implemented the LCC from C01 after the TMDS regulator circuit on the DFPAVCC rail.
5) Changed DFP_Vref filter CAP C221 and C222 to DFPAVCC (it was filter to GND).
6) Increased C222(DFP_Vref filter) to 2x22uf.
7) Added 10UF(CASEB) and a 0.1UF(0603) decoupling for AGP 3.3V at NV15.
8) Added decoupling for the FBVDDQ at NV15.T6/U6 to lower the DFPAVCC noise from 246mVpp to 150mVpp.
9) Changed both switcher output inductors to 7.8UH.
10) Changed DFP_VREF R218 to 0-Ohm
11) Changed DFP_RSET R217 to 681-Ohm 1%
12) C225 decoupled to GND
13) Changed R112 to 301K 1%.
14) Changed R115 to 221K 1%.
15) Changed R500 to 681 1%.
16) Changed R217 to 432 1%.
17) Remove C221-100pF to have room for item 18 below.
18) Increased DFP_Vref to 2x22UF to DFPAVCC and 1x22UF to GND.
19) Changed R217 to 100R 1%.

602-P0020-0000-E00

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NV15, 2MX32 DDR 64MB, RGB, DVI-I, AGP4X

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Scale

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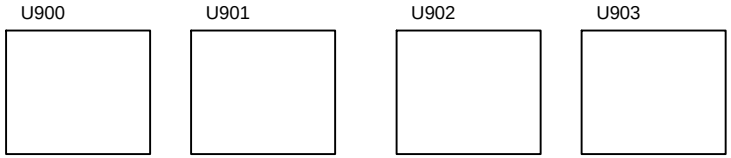
{Item}\t{Quantity}\t{Reference}\t{Assembly}{Source Package} {Value}\t
{Assembly}{Source Package} {Value}{PN}{AVL1}{AVL2}{AVL3}{AVL4}{AVL5}



Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
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PCB

M/B

FANHEATSINK

HeatSink

BRACKET

Mech

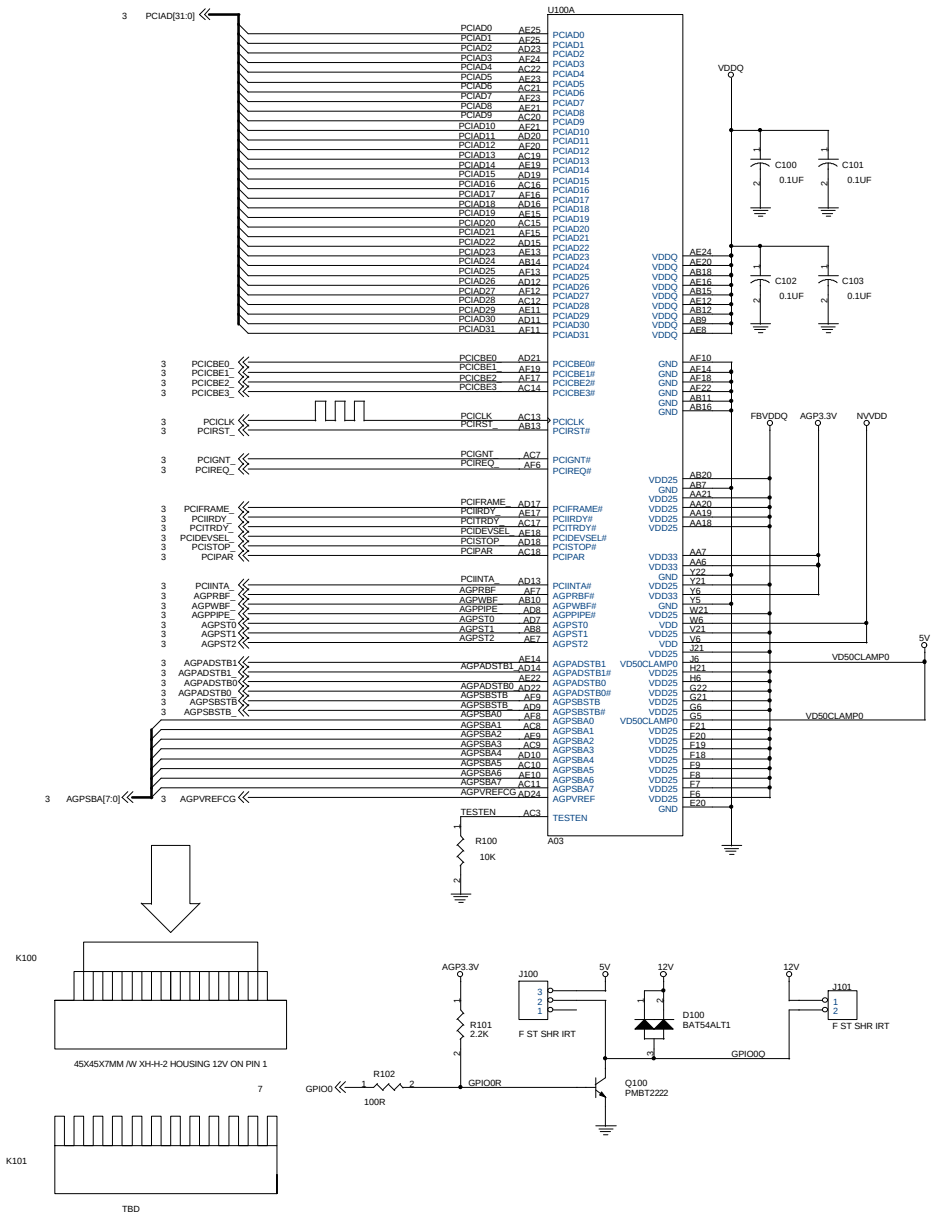
SCREW-1

SCREW

SCREW-2

SCREW

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, November 14, 2000	Sheet 1 of 1	



1a. NV15 HOST

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C			

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Scale

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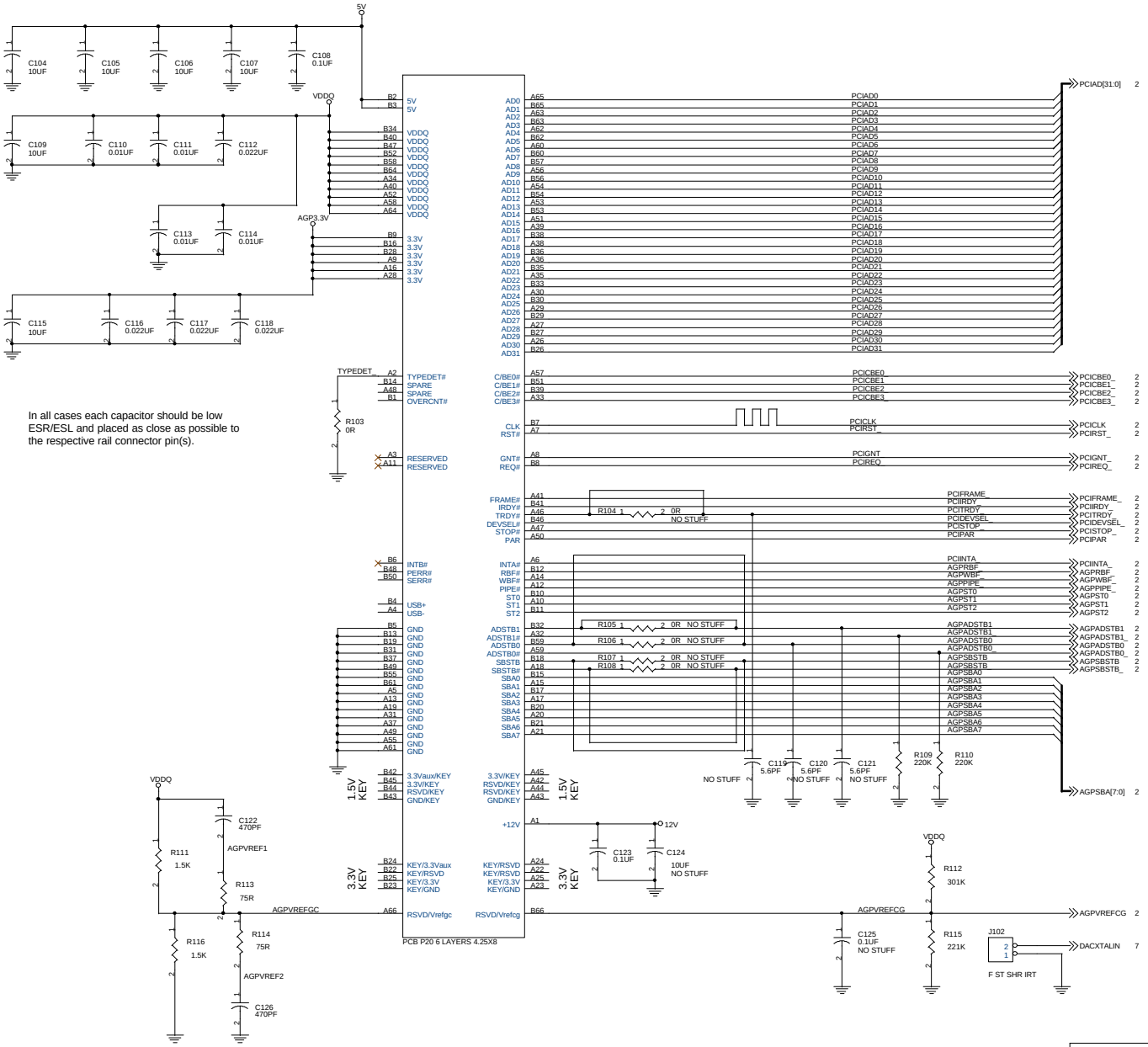

In all cases each capacitor should be low ESR/ESL and placed as close as possible to the respective rail connector pin(s).

1b1. AGP I/O

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	Size: C	CAGE Code	DWG NO / Rev
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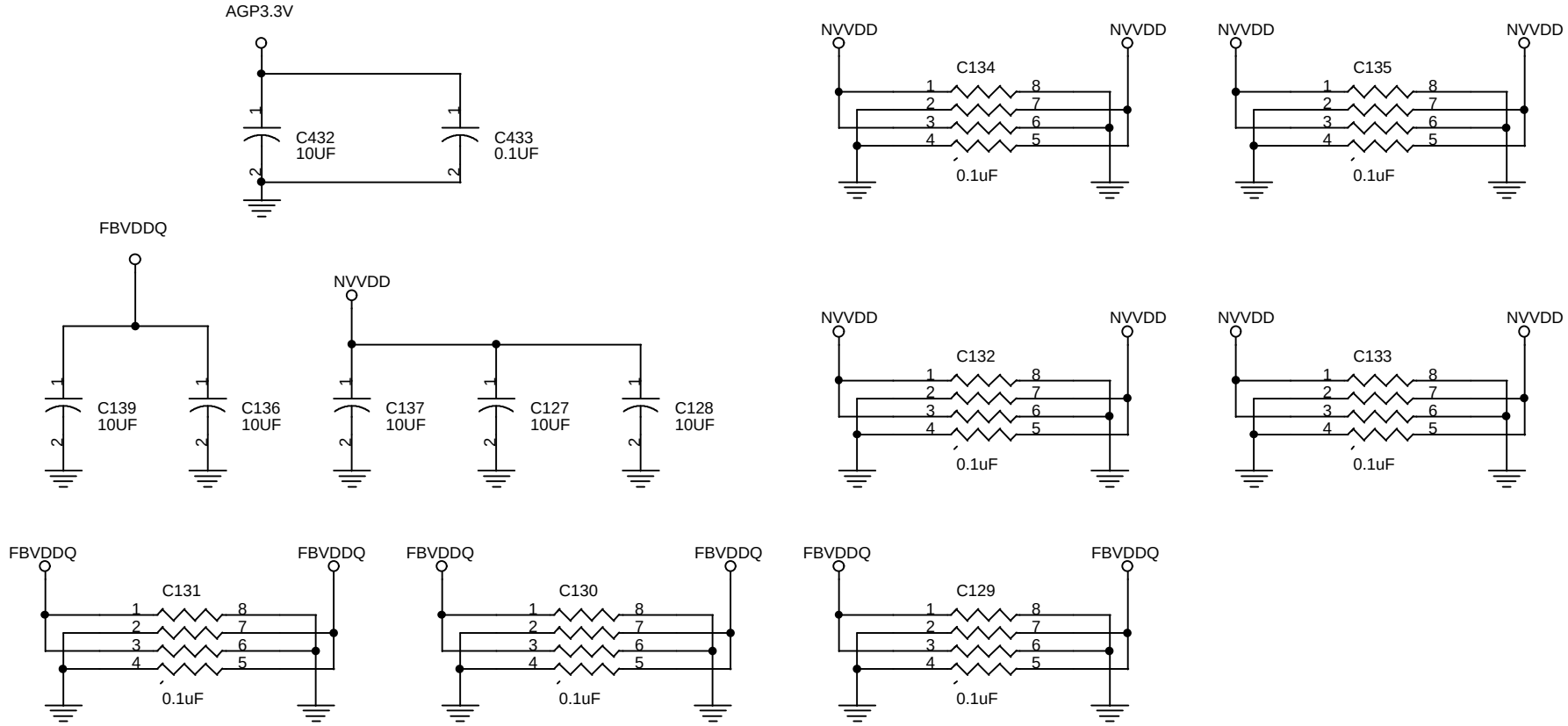

1y. NV15 DECOUPLING

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3535 Monroe St
Santa Clara, CA 95051, USA

Size	CAGE Code	DWG NO	Rev
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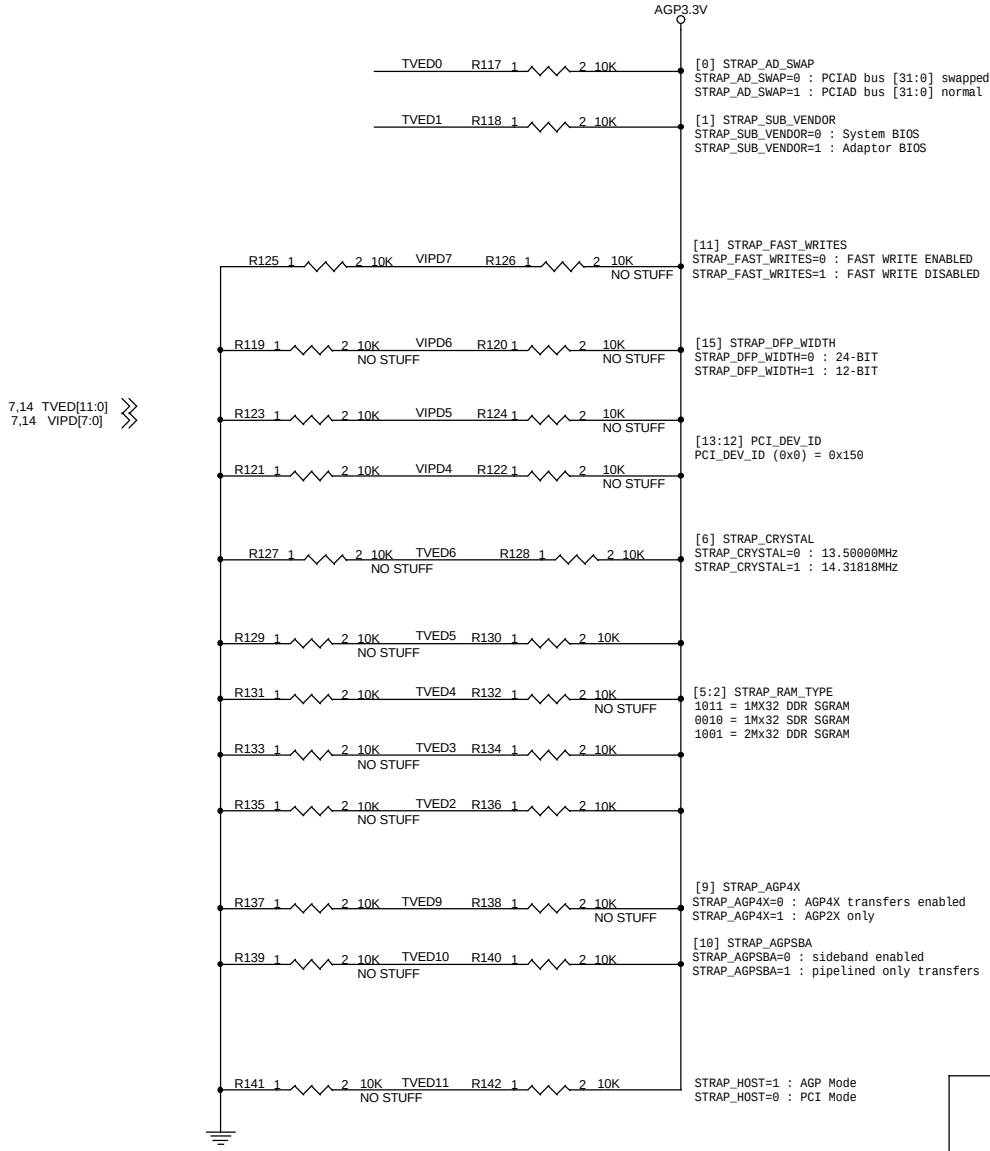

1z. NV15 HOST STRAPS

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Size	CAGE Code	DWG NO	Rev
B			

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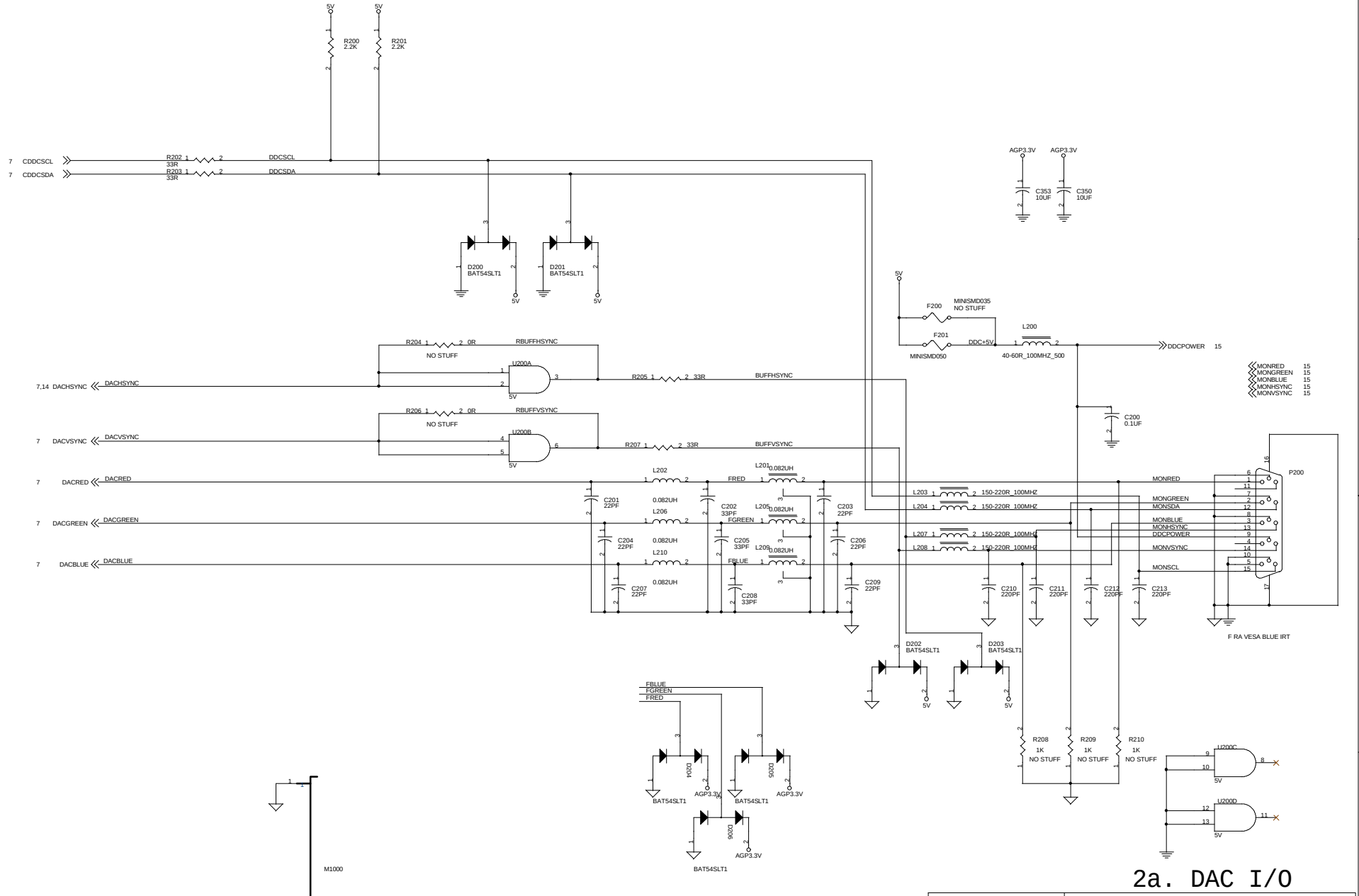

2a. DAC I/O

NVIDIA	NVIDIA Corporation 3535 Monroe St. Santa Clara, CA 95051, USA		
	Size: C	CAGE Code	DWG NO / Rev
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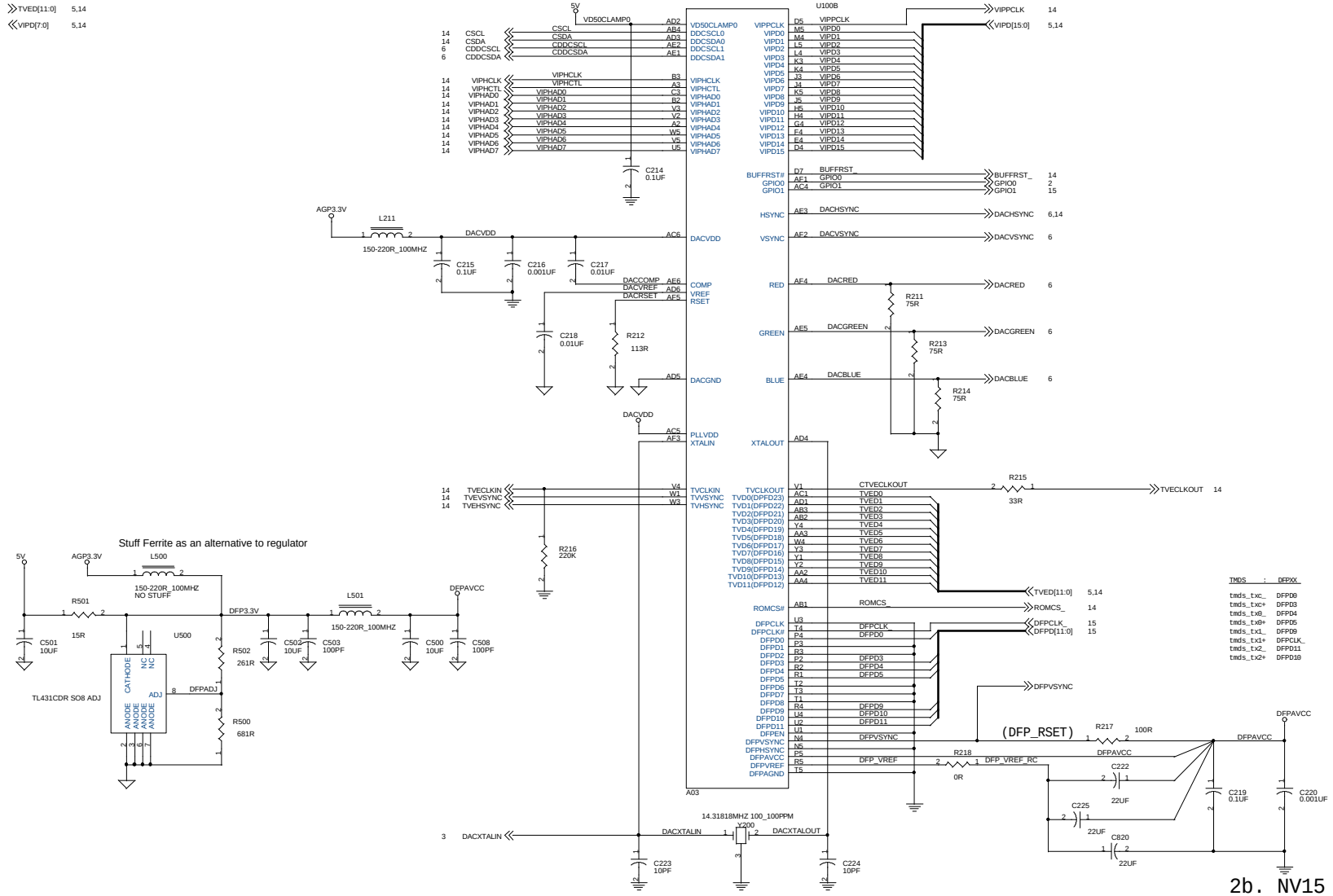

2b. NV15 DAC/TV/TMDS

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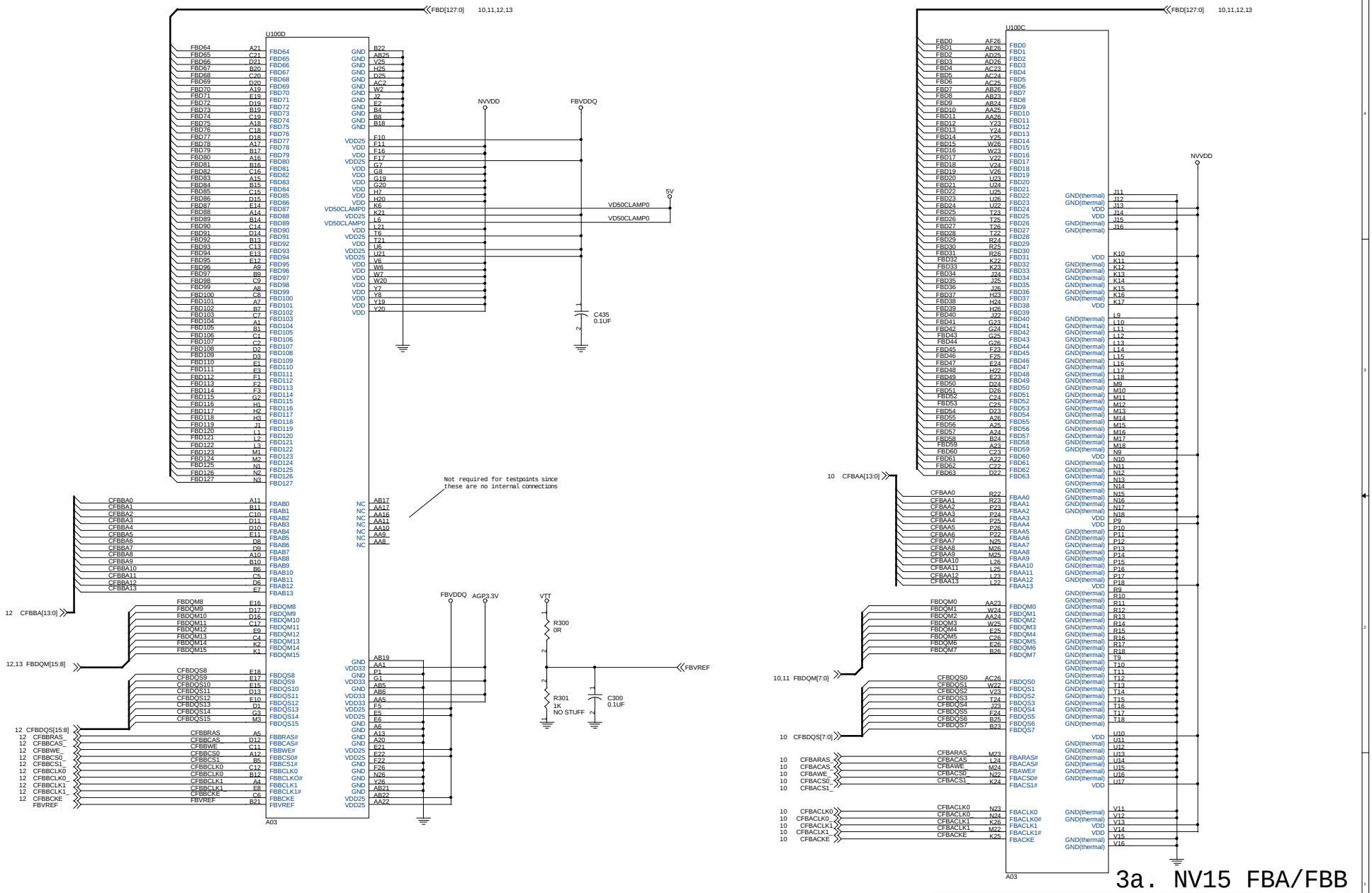

3a. NV15 FBA/FBB

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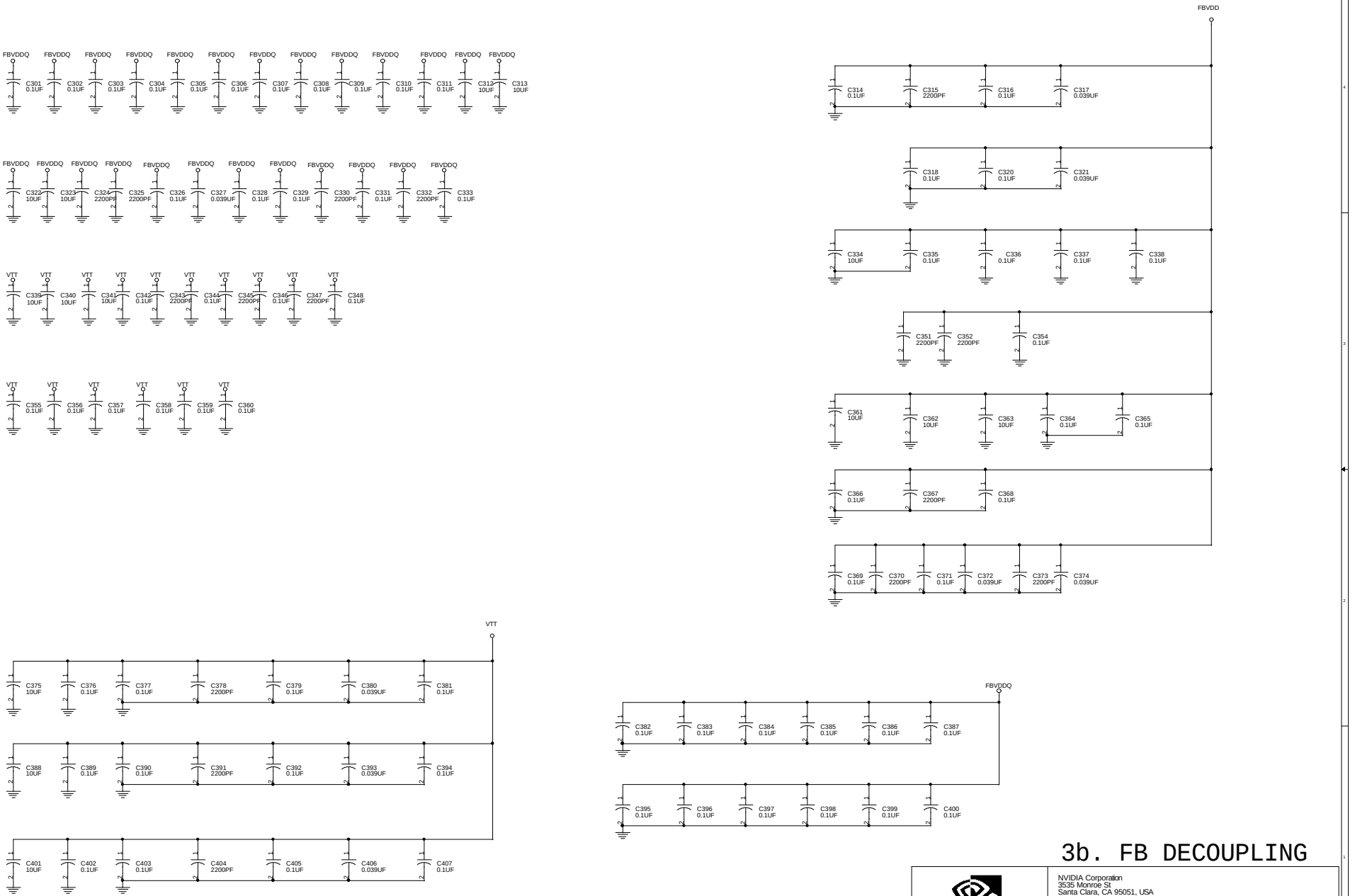

3b. FB DECOUPLING

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Size	CAGE Code	DWG NO	Rev
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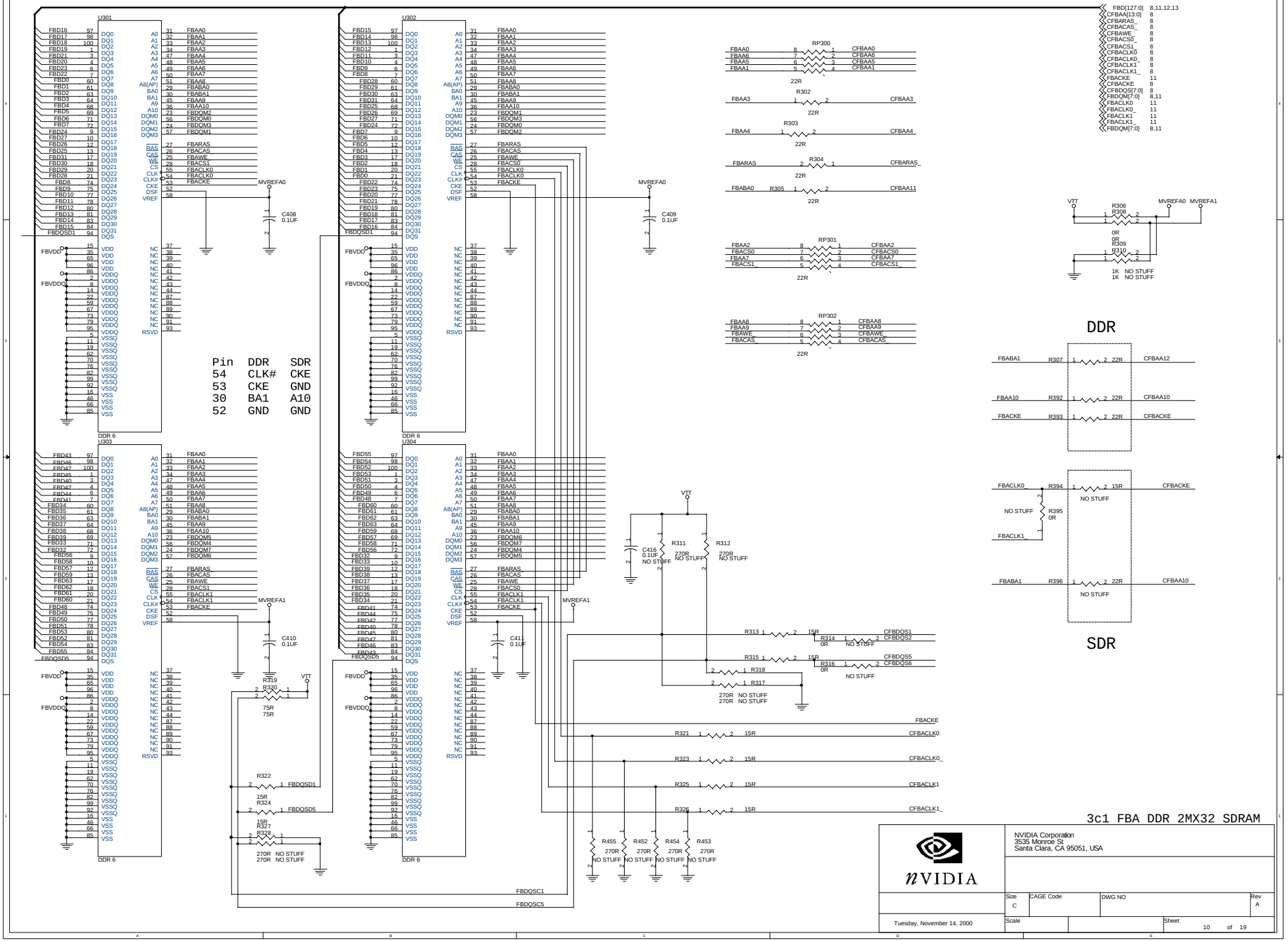
U301
U302
U303
U304
DDR 6
MVREFA0
MVREFA1
VTT
C408 0.1UF
C409 0.1UF
C410 0.1UF
C411 0.1UF
C416 0.1UF NO STUFF
RP300
RP301
RP302
R302
R303
R304
R305
R306
R308
R309
R310
R311
R312
R313
R314
R315
R316
R317
R318
R319
R320
R321
R322
R323
R324
R325
R326
R327
R328
R392
R393
R394
R395
R396
R307
22R
75R
15R
270R NO STUFF
0R
1K NO STUFF
FBD[127:0] 8,11,12,13
CFBAA[13:0] 8
CFBARAS_ 8
CFBACAS_ 8
CFBAWE_ 8
CFBACS0_ 8
CFBACS1_ 8
CFBACLK0 8
CFBACLK0_ 8
CFBACLK1 8
CFBACLK1_ 8
FBACKE 11
CFBACKE 8
CFBDQS[7:0] 8
FBDQM[7:0] 8,11
FBACLK0 11
FBACLK0_ 11
FBACLK1 11
FBACLK1_ 11
FBDQM[7:0] 8,11
DDR
SDR
Pin DDR SDR
54 CLK# CKE
53 CKE GND
30 BA1 A10
52 GND GND
3c1 FBA DDR 2MX32 SDRAM
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Tuesday, November 14, 2000
Size C
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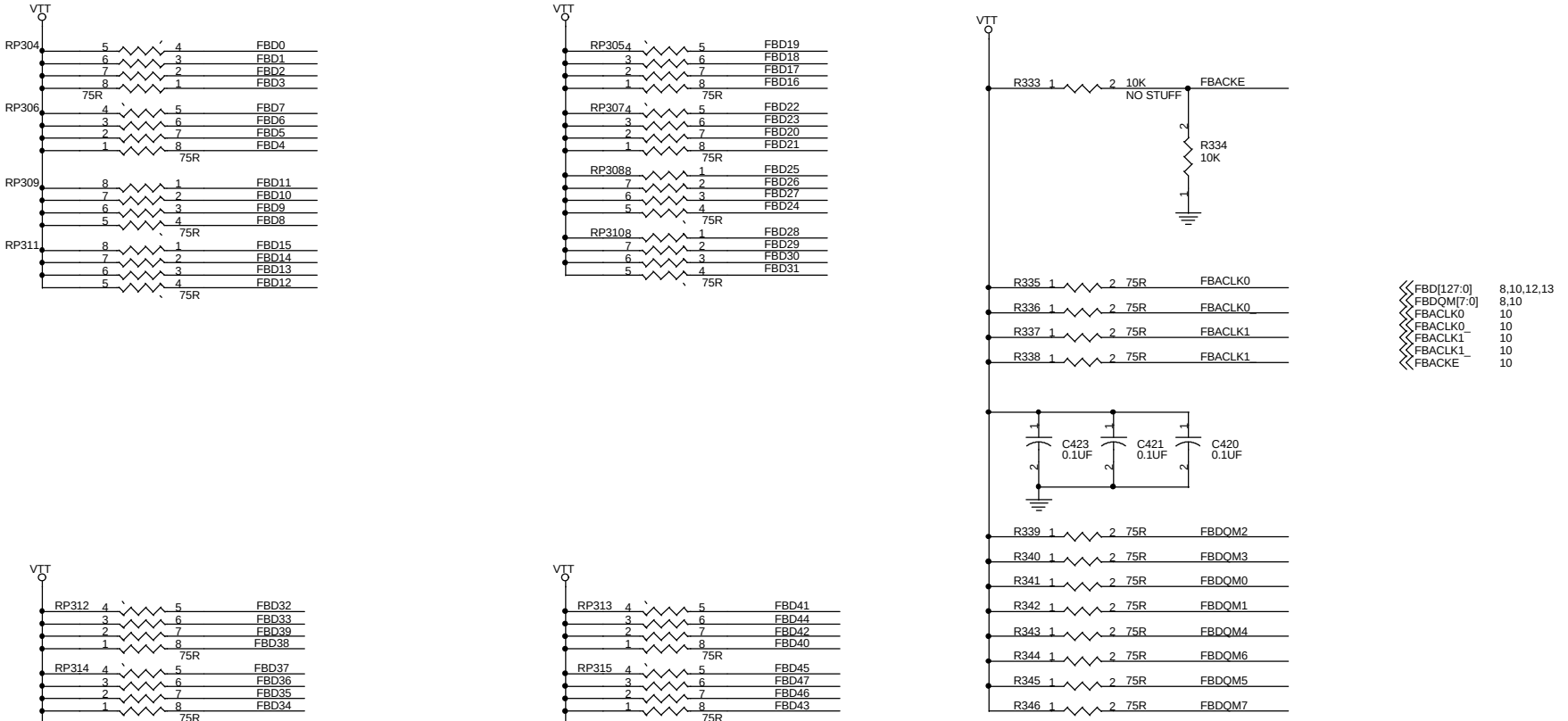

FBD[127:0]	8,10,12,13
FBDQM[7:0]	8,10
FBACLK0	10
FBACLK0_	10
FBACLK1	10
FBACLK1_	10
FBACKE	10

3c2. FBA DDR 2MX32 SDRAM TERM

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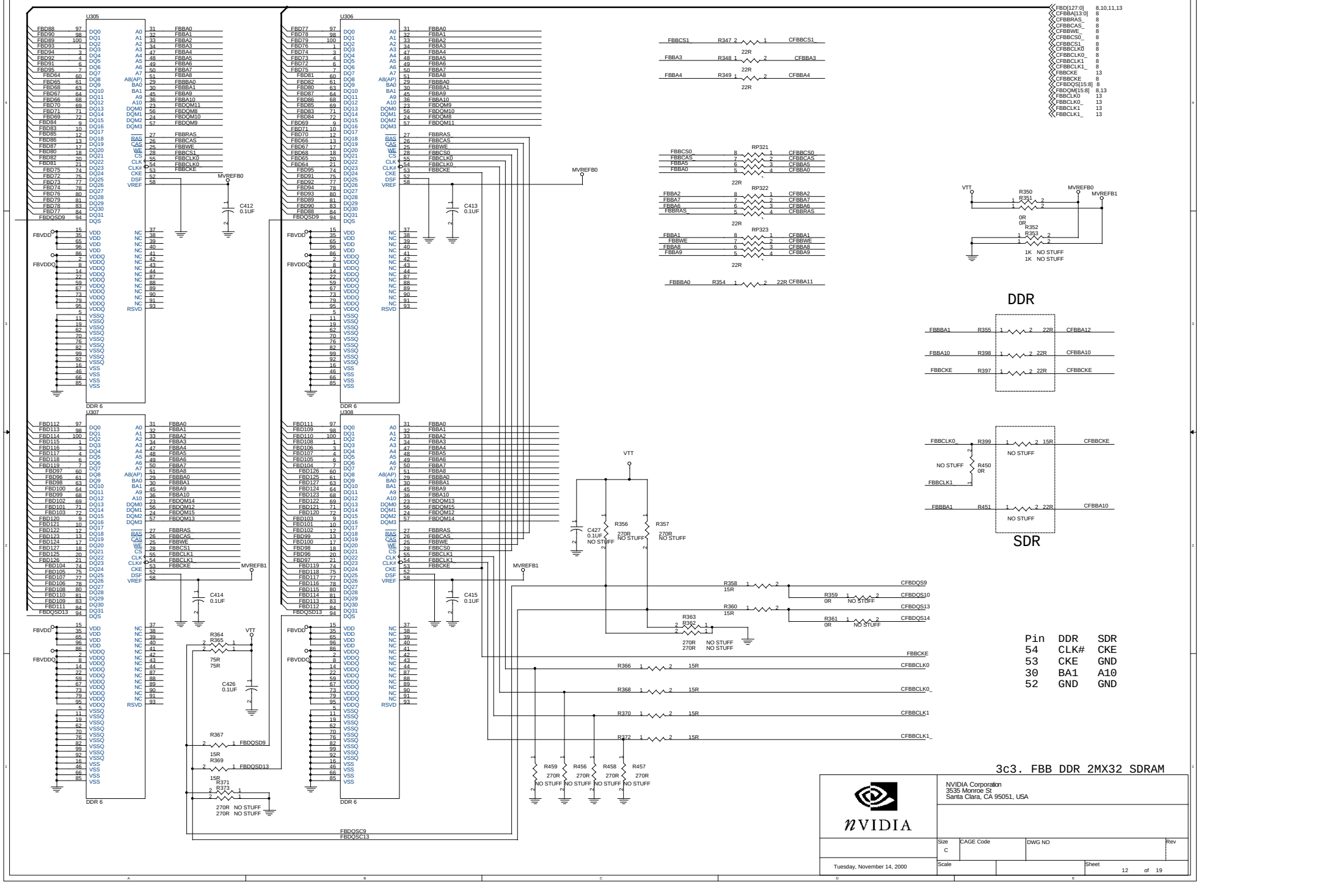
U305
U306
U307
U308
DDR 6
MVREFB0
MVREFB1
VTT
C412 0.1UF
C413 0.1UF
C414 0.1UF
C415 0.1UF
C426 0.1UF
C427 0.1UF NO STUFF
RP321
RP322
RP323
R347 22R
R348 22R
R349 22R
R354 22R
R350 0R
R351 0R
R352 1K NO STUFF
R353 1K NO STUFF
DDR
SDR
R355 22R
R398 22R
R397 22R
R399 15R NO STUFF
R450 0R NO STUFF
R451 22R NO STUFF
R356 270R NO STUFF
R357 270R NO STUFF
R358 15R
R359 0R NO STUFF
R360 15R
R361 0R NO STUFF
R362 270R NO STUFF
R363 270R NO STUFF
R364 75R
R365 75R
R366 15R
R367 15R
R368 15R
R369 15R
R370 15R
R371 270R NO STUFF
R372 15R
R373 270R NO STUFF
R456 270R NO STUFF
R457 270R NO STUFF
R458 270R NO STUFF
R459 270R NO STUFF
FBDQSC9
FBDQSC13
Pin DDR SDR
54 CLK# CKE
53 CKE GND
30 BA1 A10
52 GND GND
3c3. FBB DDR 2MX32 SDRAM
NVIDIA Corporation
3535 Monroe St.
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Tuesday, November 14, 2000
Size C
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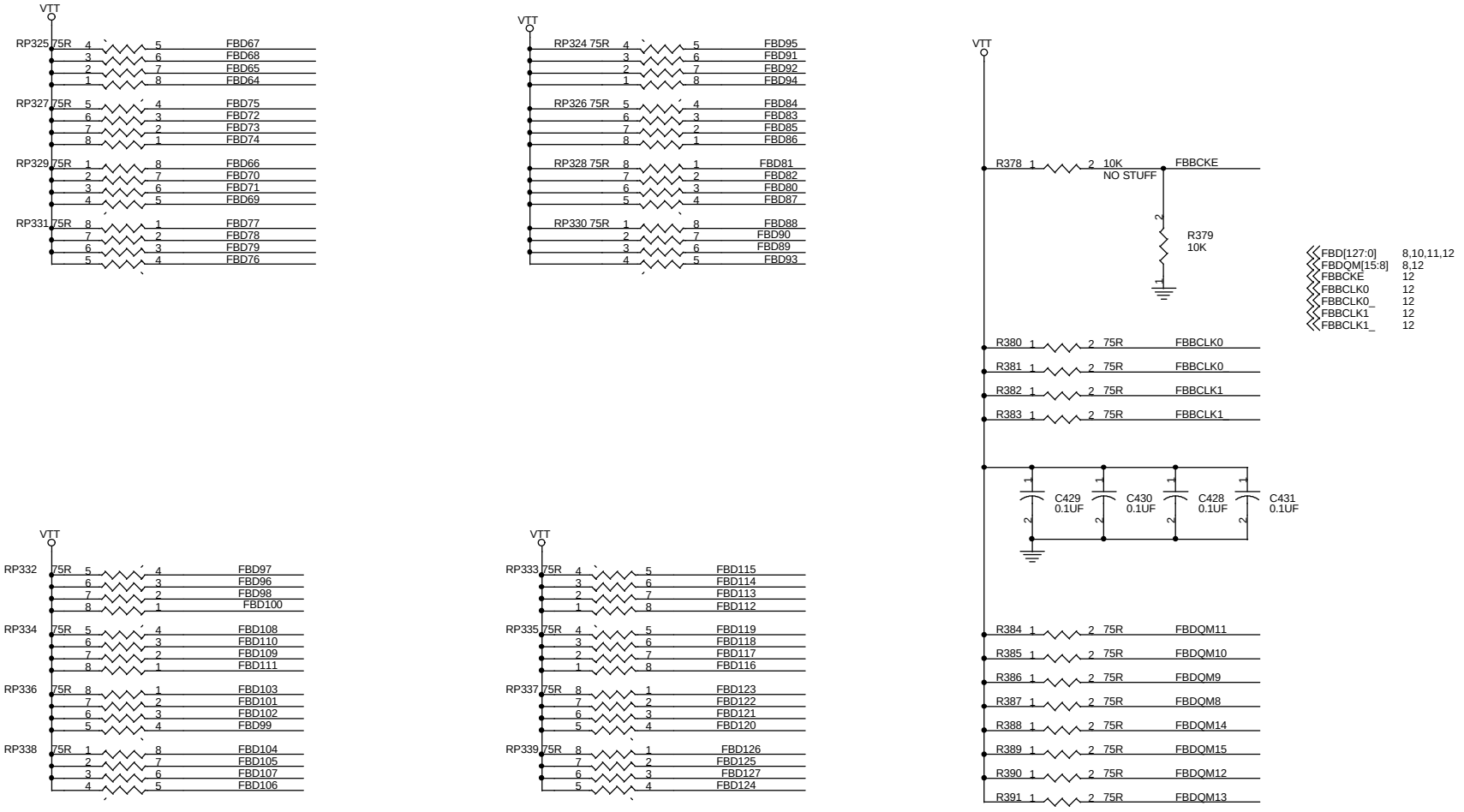

3c4. FBB DDR 2MX32 SDRAM TERM

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Size	CAGE Code	DWG NO	Rev
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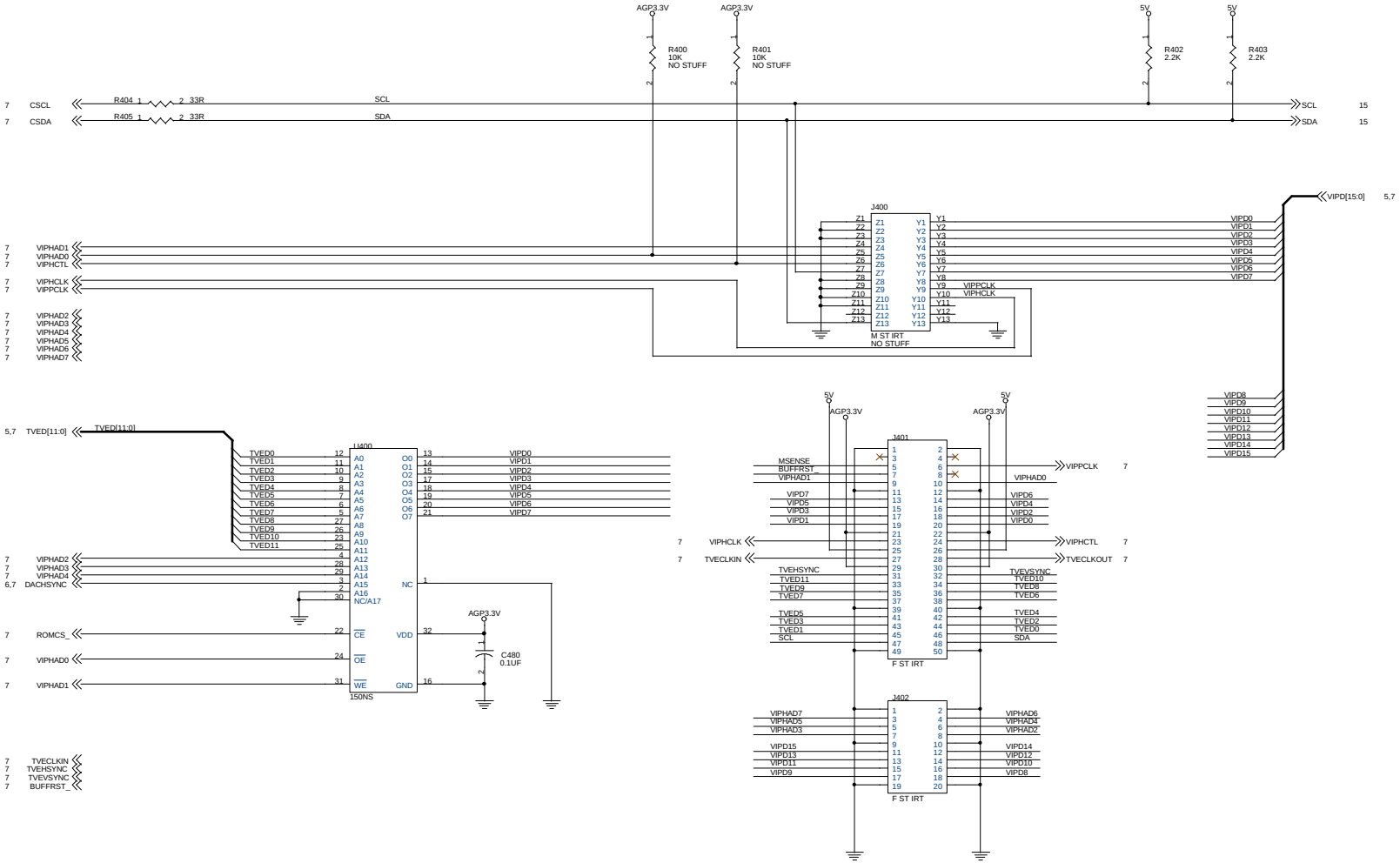

4a. ROM VIP & VIDEO IF

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Size	CAGE Code	DWG NO	Rev
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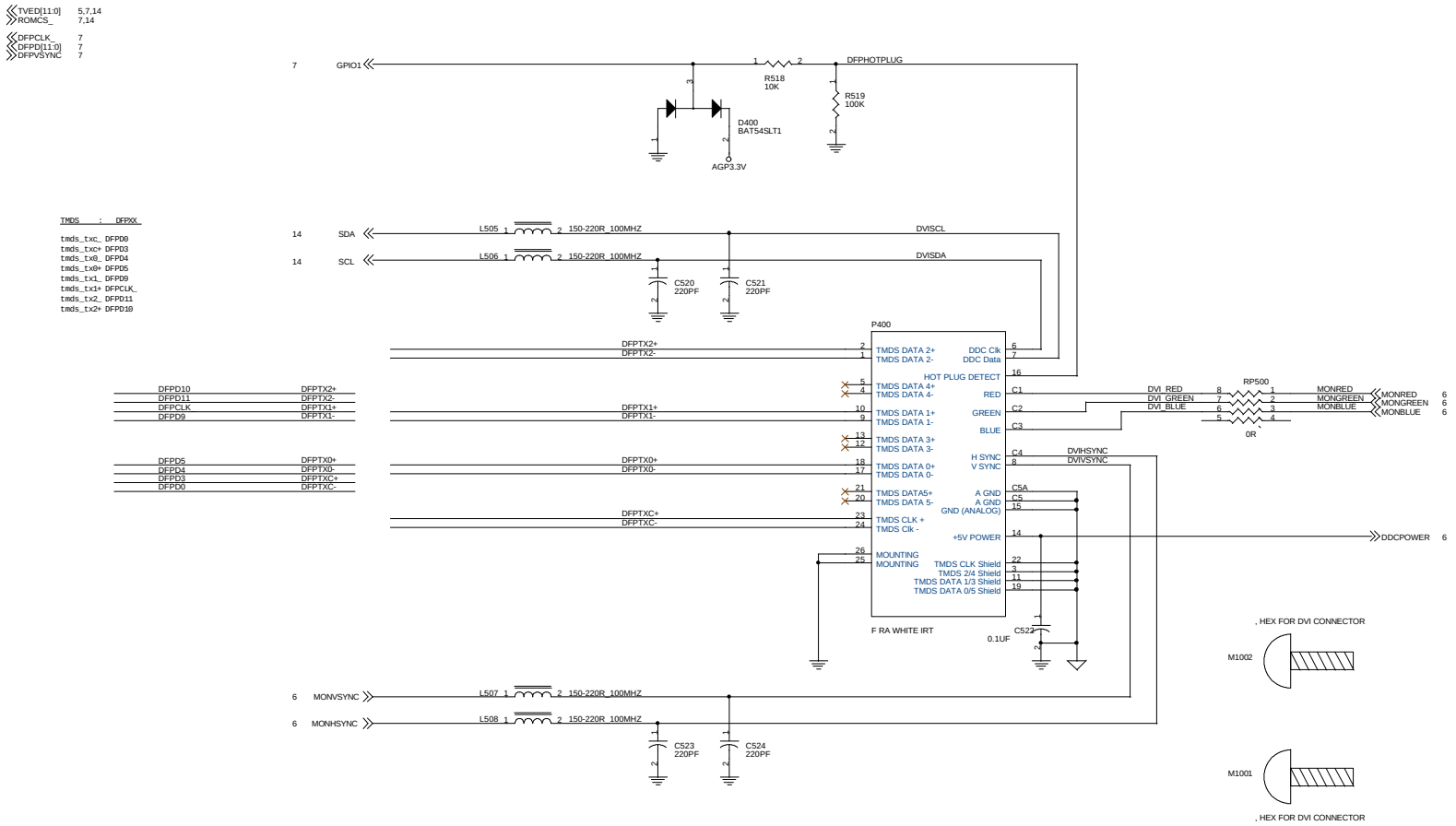

5a. DVI-I I/O

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Size	CAGE Code	DWG NO	Rev
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Scale

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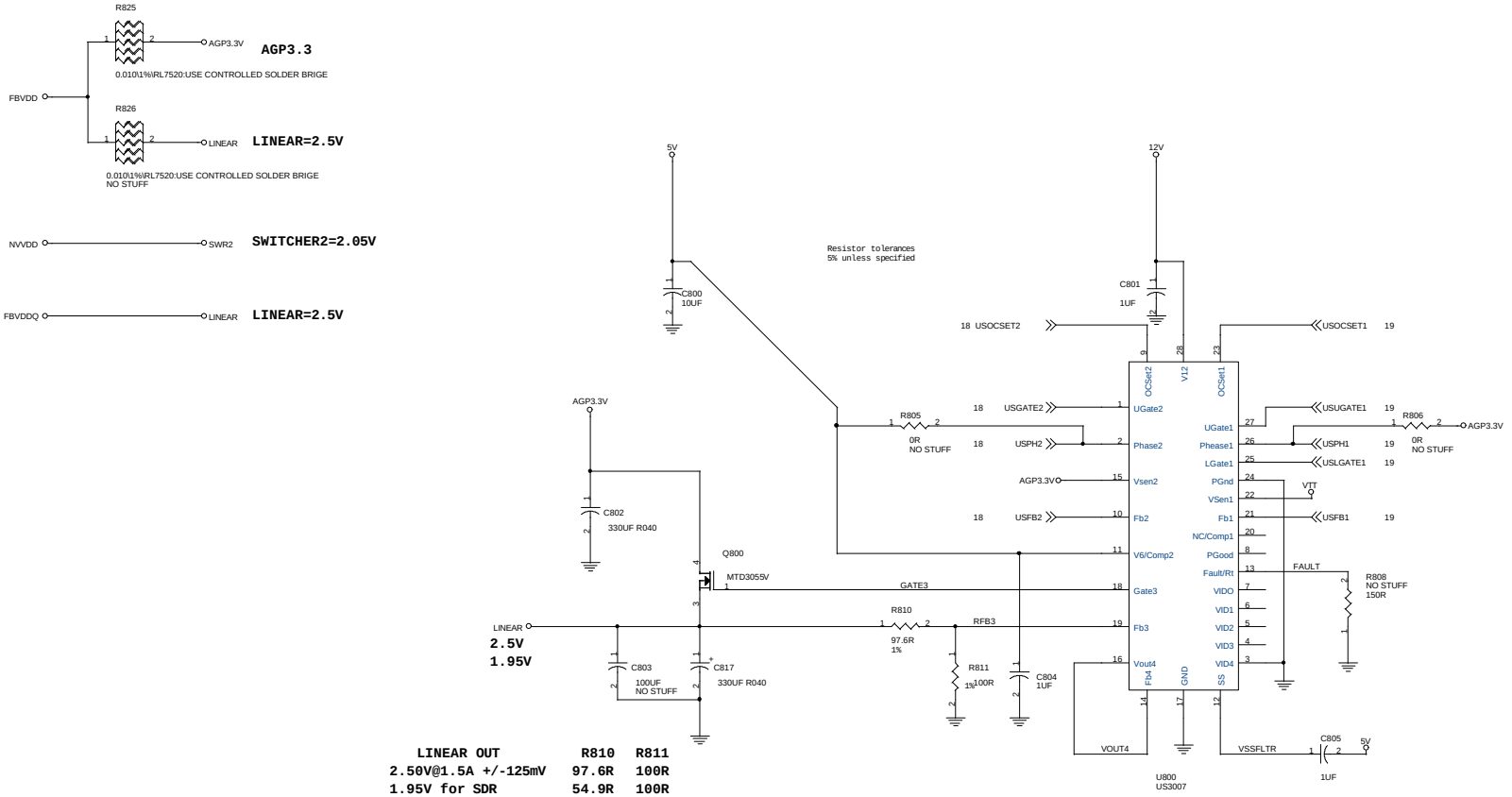

LINEAR OUT	R810	R811
2.50V@1.5A +/-125mV	97.6R	100R
1.95V for SDR	54.9R	100R

R810=((LINEAR OUT/1.26)-1)*100(R811)

8b1. NV15 BASE POWER SOLUTION

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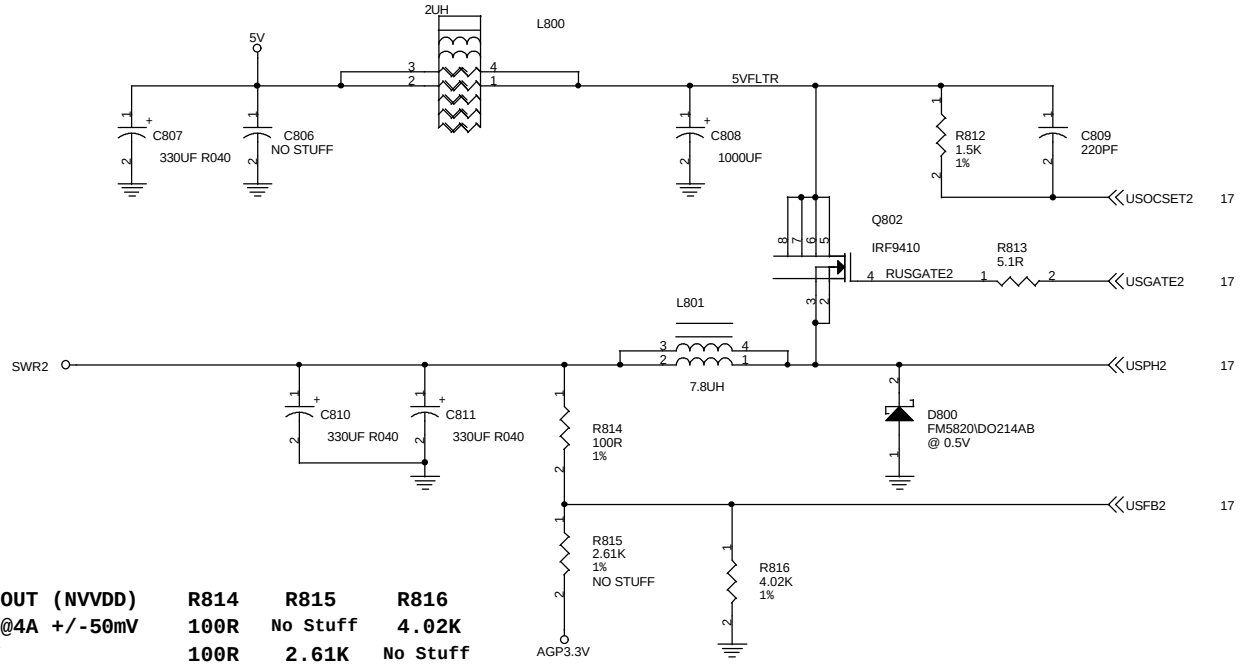

SWR2 OUT (NVVDD)	R814	R815	R816
2.05V@4A +/-50mV	100R	No Stuff	4.02K
1.95V	100R	2.61K	No Stuff

R816=100/((2.05V/2)-1)

R815=130/(2-1.95v)

8b2. NV15 DDR POWER ADDER

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Size	CAGE Code	DWG NO	Rev
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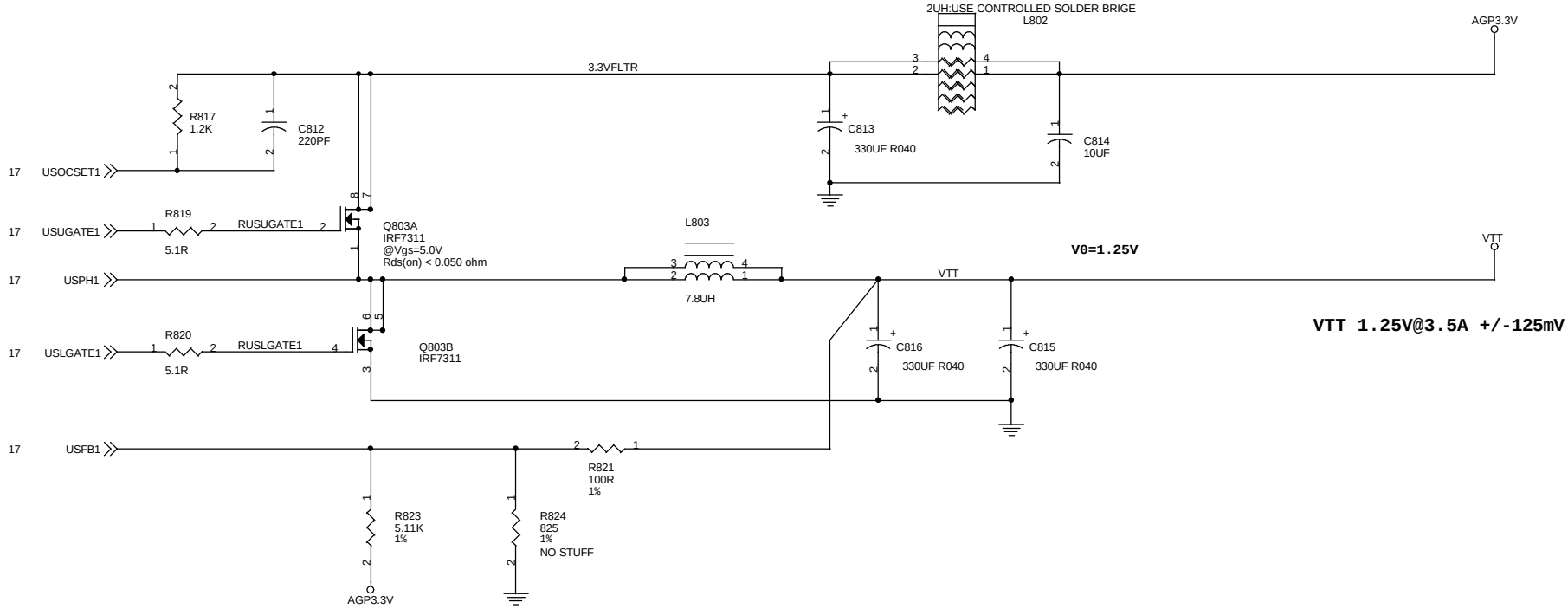

8b2. NV15 VTT POWER ADDER

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