電子類元件 零件承認書文件 CHECK LIST

零件廠商：**UPI**　　品名規格：SMD VQFN4x4 - 24L
技嘉料號：10TA1-609509-00H

項次	文件項目
	Data Sheet檢核項目
1	DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2**
8	零件樣品 20PCS(Chipset 等高單價，至少 1PCS)
9	**電子零件承認基本調查表。註 3**
10	以上資料電子檔為 PDF 檔，且是同 1 個 File
	GSCM 綠色產品管理系統-物料管制文件檢核清單
物料管制文件 1	GSCM 綠色產品管理系統：零件照片
物料管制文件 2	GSCM 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4**
物料管制文件 3	GSCM 綠色產品管理系統：Data Sheet
	GSCM 綠色產品管理系統-MCD 表格
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
	其他文件 **(僅適用電阻、電容類之系列元件)**
附件 1	危害物質測試報告 Test Report of Hazardous Substances。**註 5**
附件 2	元件調查表 Component Composition Table

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等
※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)
2.1. 基本需符合 JEDEC 規範
2.2. Ambient Temp. (Reflow Temp endurace): >225℃, 70 sec. 零件塑膠材質需 PA9T(含)等級以上
2.3. PASTE IN HOLE 零件塑膠材質需 PA9T(含)等級以上
※ **3. 電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G*,11T***
非 IC 類：10C*,11C*,10L*,11L*,10X*,11X*,10R*,11B*
※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”
※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

電子零件承認基本調查表

一、原物料規格/來源			
項次	部位名稱/規格	材質	原物料來源產地
1	CHIP	金屬	MAXCHIP
2	DIE ATTACH	EPOXY	SUMITOMO
3	LEAD FRAME	金屬	SHINKO
4	BONDING WIRE	金屬	MK
5	MOLDING COMPOUND	EPOXY	SUMITOMO
6	PLATING	鍍錫	JAU JANQ

二、晶圓廠(非 IC 類免填)					
項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	(MAX)鉅晶電子	TW	8	100	NA

三、封裝廠(IC 類)；成品之生產製造工廠(非 IC 類)				
項次	工廠名稱	生產產地	投產比率(%)	自有/外包
1	GTK(超豐電子)	TW	50	NA
2	ASE-KS(日月光-昆山)	CN	50	NA

四、產能	
總產能(月/PCS)	可供技嘉產能(月/PCS)
NA	NA

※ 1. IC 類之晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 2. 非 IC 類零件之成品生產製造工廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動 (包含 AVL 或相關資訊文件之異動)時，請主動通知技嘉 Sourcer 與 RD 承認單位，並更新文件

※ 3. 以上資訊欄位若有不足，可自行增加行數

3/2/1-Phase Synchronous-Rectified Buck Controller for Mobile GPU Power

General Description

The uP9509 is a 3/2/1-phase synchronous-rectified buck controller specifically designed to work with 4.5V ~ 26V input voltage and deliver high quality output voltage for high-performance graphic processor power.

The uP9509 adopts proprietary RCOT™ technology, providing flexible selection of output LC filter and excellent transient response to load and line change.

The uP9509 supports NVIDIA Open Voltage Regulator-2+ with PWMVID feature. The PWMVID input is buffered and filtered to generate accurate reference voltage, and the output voltage is precisely regulated to the reference input.

The uP9509 integrates two bootstrapped MOSFET gate drivers and one PWM output achieving optimal balance between cost and flexibility. The uP9509 uses MOSFET $R_{DS(ON)}$ current sensing for channel current balance.

Other features include accurate and reliable over current limit protection, adjustable on-time setting, power saving control input, and power good output. This part is available in a VQFN4x4 - 24L package.

Ordering Information

Order Number	Package Type	Top Marking
uP9509PQAG	VQFN4x4 - 24L	uP9509P

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

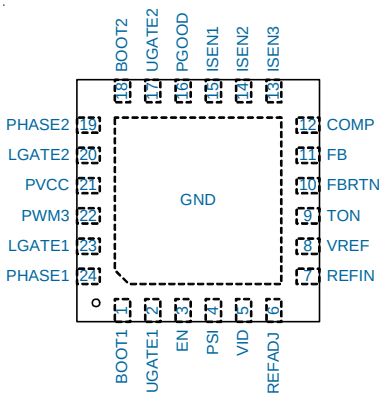
Features

- **Support NVIDIA's Open VReg Type-2+ PWMVID Technology**
- **Wide Input Voltage Range 4.5V ~ 26V**
- **Robust Constant On-Time Control**
- **3/2/1 Phase Operation**
- **Two Integrated MOSFET Drivers with Shoot-Through Protection and Internal Bootstrap Schottky Diode**
- **Adjustable Current Balancing by $R_{DS(ON)}$ Current Sensing**
- **Adjustable Operation Frequency**
- **External Compensation**
- **Dynamic Output Voltage Adjustment**
- **Adjustable Per-Phase Over Current Limit**
- **Power Good Indication**
- **Over Voltage Protection**
- **Under Voltage Protection**
- **Adjustable Soft-Start Time**
- **Over Temperature Protection**
- **RoHS Compliant and Halogen Free**

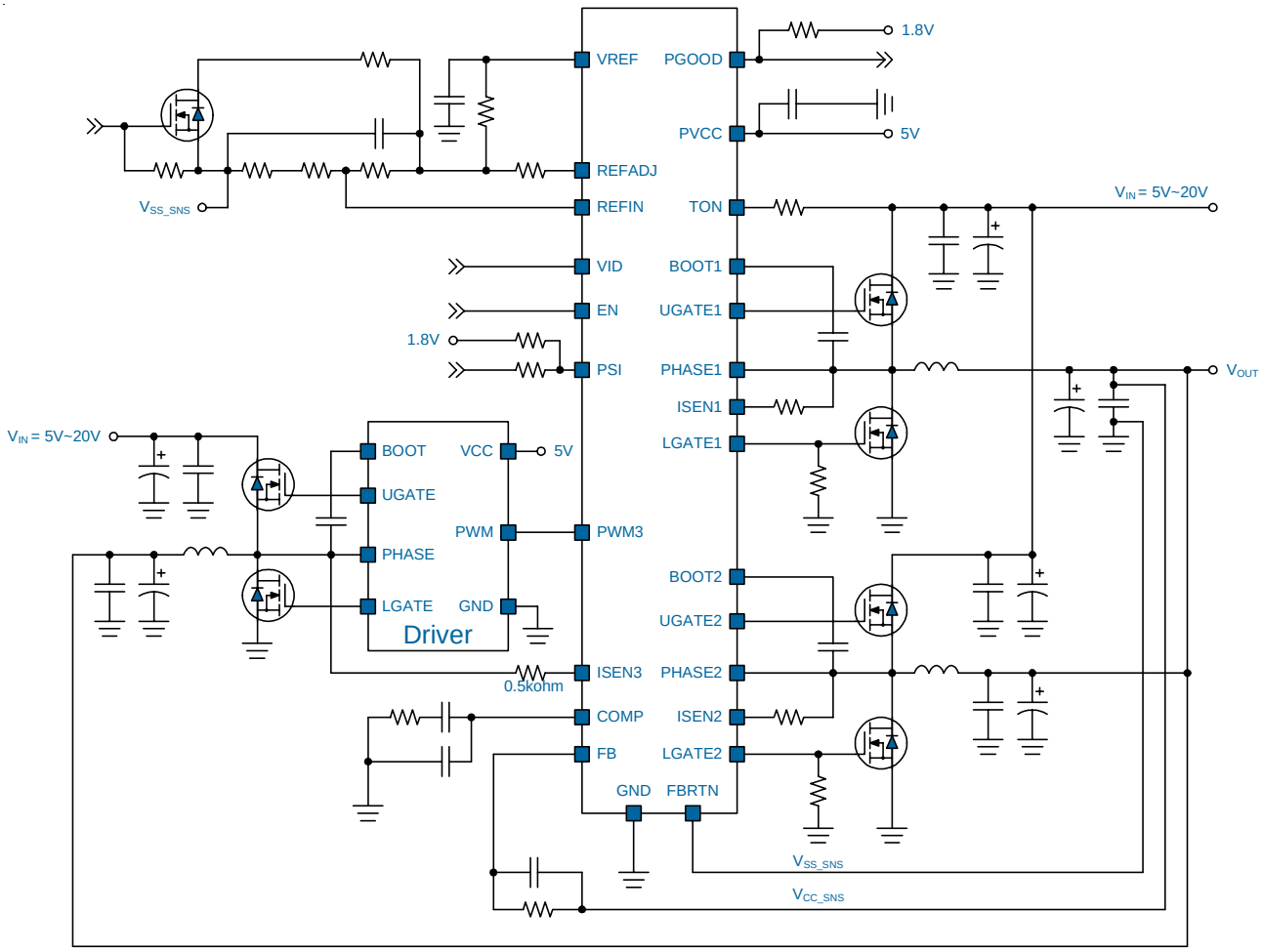
Applications

- **Middle-High End GPU Core Power**
- **High End Desktop PC Memory Core Power**
- **Low Output Voltage, High Power Density DC-DC Converters**
- **Voltage Regulator Modules**

Pin Configuration



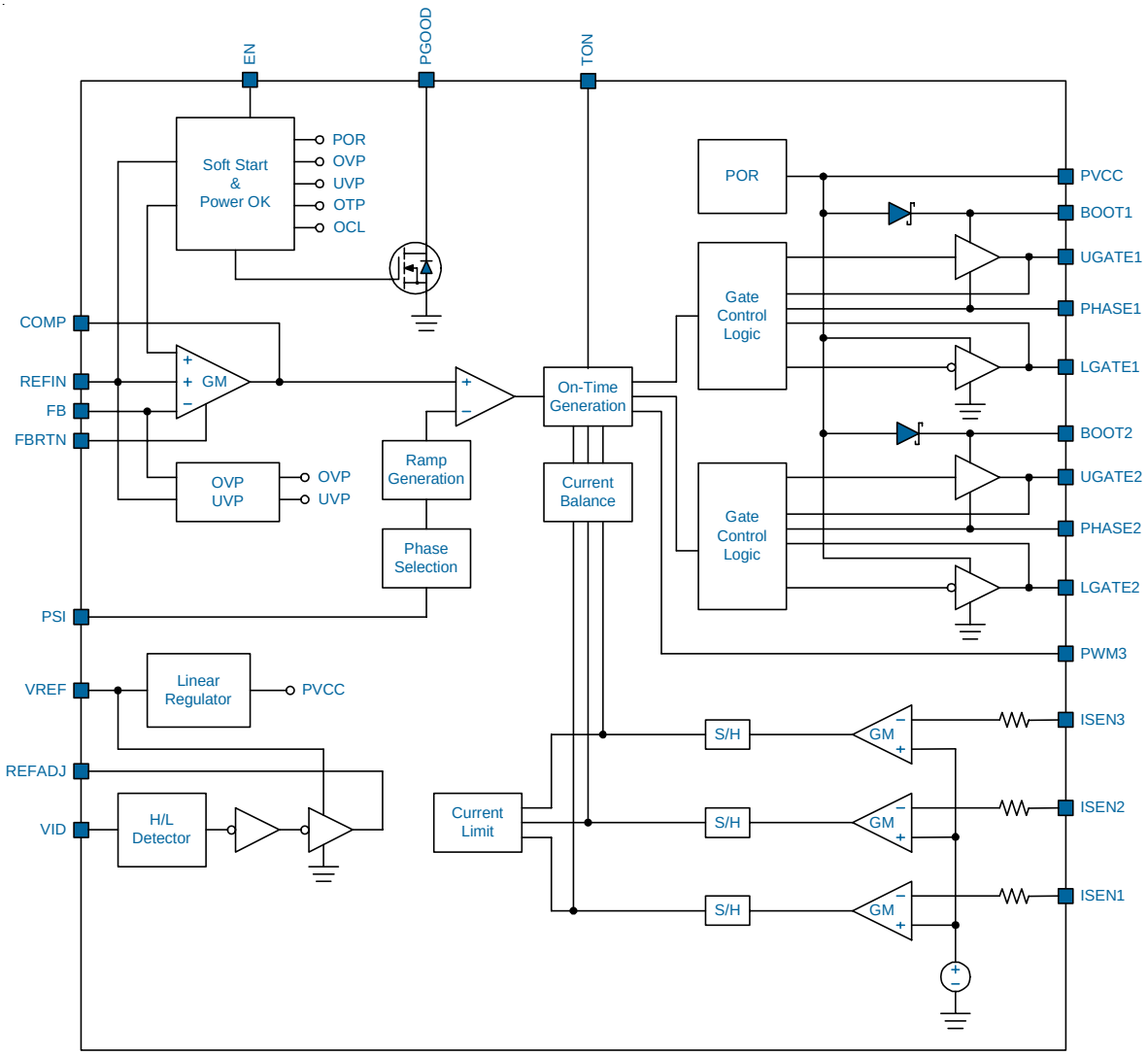
Typical Application Circuit



Functional Pin Description

No.	Name	Pin Function
1	BOOT1	**BOOT for Phase 1.** Connect a capacitor form this pin to PHASE1 to form a bootstrap circuit for upper gate driver of the phase 1.
2	UGATE1	**Upper Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 upper MOSFET.
3	EN	**Enable.** Chip enable.
4	PSI	**Power Saving Input.** An input pin receiving power saving control signal from GPU.
5	VID	**VID.** PWMVID input pin.
6	REFADJ	**Reference Adjustment.** PWMVID output pin. Connect this pin with an RC integrator to generate REFIN voltage.
7	REFIN	**Reference Input.** Connect this pin to an external reference voltage through a resistor or connect to the output of the REFADJ circuit.
8	VREF	**Reference Voltage.** 2V LDO voltage output pin. Connect an at least 1uF decoupling capacitor between this pin and GND.
9	TON	**On-time Setting Pin.** Connect a resistor from this pin to VIN to set the on-time of the upper MOSFET.
10	FBRTN	**Return for the Reference Circuit.** Connect this pin to the ground point where output voltage is to be regulated.
11	FB	**Feedback Pin.** This pin is the inverting input of the error amplifier.
12	COMP	**Compensation Output.** This pin is the output of the error amplifier.
13	ISEN3	**ISEN3.** Connect this pin to the PHASE3 pin with 0.5kohm to sense phase 3 output current. **DO NOT use other resistor.**
14	ISEN2	**ISEN2.** Connect this pin to the PHASE2 pin with a resistor to sense phase 2 output current.
15	ISEN1	**ISEN1.** Connect this pin to the PHASE1 pin with a resistor to sense phase 1 output current.
16	PGOOD	**Power Good Indication.** Open-drain structure. Connect this pin to a voltage source with a pull-up resistor.
17	UGATE2	**Upper Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 upper MOSFET.
18	BOOT2	**BOOT for Phase 2.** Connect a capacitor form this pin to PHASE2 to form a bootstrap circuit for upper gate driver of the phase 2.
19	PHASE2	**Phase Pin for Phase 2.** This pin is the return path of upper gate driver for phase 2. Connect a capacitor from this pin to BOOT2 to form a bootstrap circuit for upper gate driver of the phase2.
20	LGATE2	**Lower Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 lower MOSFET.
21	PVCC	**Supply Input for the IC.** Voltage power supply of the IC. Connect this pin to a 5V supply and decouple using at least a 1uF ceramic capacitor.
22	PWM3	**PWM Output of Phase 3**. Connect this pin to the PWM input pin of the companion gate driver. Connect this pin to GND when maximum 2 phase operation.
23	LGATE1	**Lower Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 lower MOSFET.
24	PHASE1	**Phase Pin for Phase 1.** This pin is the return path of upper gate driver for phase 1. Connect a capacitor from this pin to BOOT1 to form a bootstrap circuit for upper gate driver of the phase 1.
Exposed Pad		**Ground.** Tie this pin to ground island/plane through the lowest impedance connection available.

Functional Block Diagram



Functional Description

Supply Input and Power On Reset

The uP9509 receives supply input from PVCC pin to provide current to gate drivers and internal control circuit. PVCC is continuously monitored for power on reset. The POR level is typical 4.1V at rising. The TON pin voltage is used for on-time calculation and should be connected to the supply input of power stage.

The uP9509 integrates floating MOSFET gate driver that are powered from the PVCC pin. A bootstrap schottky diode is embedded to facilitates PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications. An external Schottky diode with lower voltage drop can improve the power conversion efficiency.

Phase Number of Operation (Hard-wire Programming)

The uP9509 supports 3/2/1 phase operation. The maximum phase number of operation is determined by checking the PWM3 status when POR. Connect PWM3 pin to GND with 100kΩ resistor for maximum 2-phase operation; Connect ISEN2 to PVCC with 100kΩ resistor for maximum 1-phase operation. Once selected, the maximum phase number of operation is latched and can only be changed at the next POR.

Constant On-Time Setting

The uP9509 adopts a compensated constant-on-time control scheme. A resistor R_{TON} connected to TON pin programs the constant on time according to the equation:

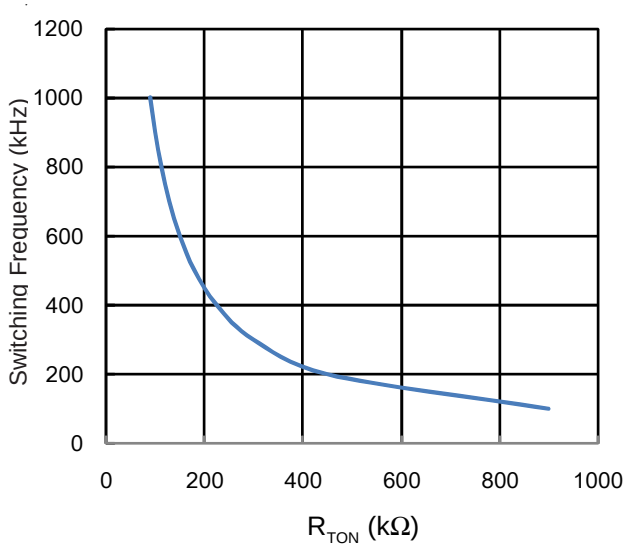


Figure 1. Switching Frequency vs. R_{TON}

$$T_{ON}(ns) = \frac{V_{OUT}}{V_{IN}} \times \frac{R_{TON}}{9} \times 100 \quad (ns)$$

where R_{TON} is in kΩ, V_{IN} is the supply input voltage and V_{OUT} is the output voltage.

Voltage Control Loop and PWMVID Function

Figure 2 illustrates the voltage control loop of the uP9509. FB and REFIN are negative and positive inputs of the Error Amplifier respectively. The Error Amplifier modulates the COMP voltage V_{COMP} of buck converter to force FB voltage V_{FB} follows V_{REFIN}.

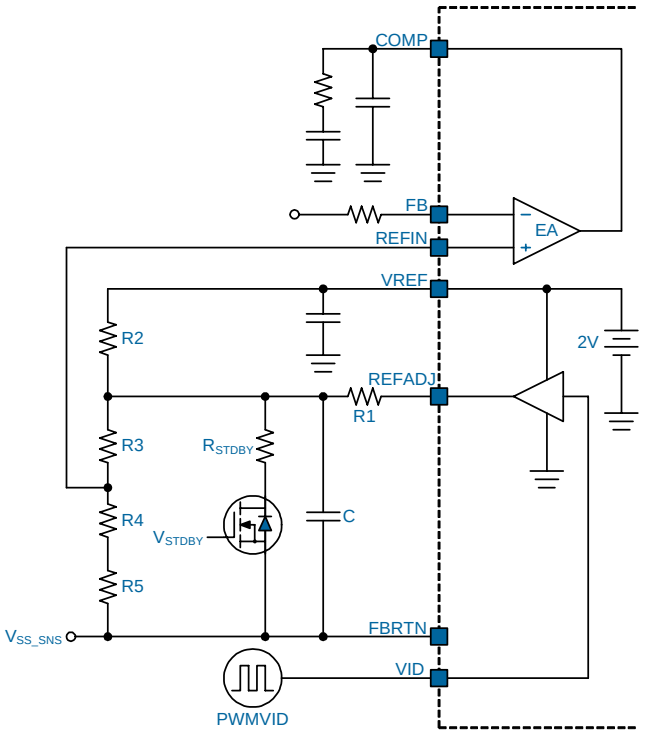


Figure 2. Voltage Control Loop

The PWMVID signal from GPU is applied to the VID pin, which is the input pin of the internal buffer. This buffer plays the role of level shifting, and the output of this buffer is injected into the external RC integrator to generate REFIN voltage, which can be calculated as:

$$V_{REFIN} =$$

$$V_{VREF} \times D \times \frac{R2//(R3+R4+R5)}{R1+R2//(R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5} +$$

$$V_{VREF} \times \frac{R1//(R3+R4+R5)}{R2+R1//(R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5}$$

where $V_{REFIN,DC}$ is the DC voltage of REFIN, V_{VREF} is the voltage of VREF (typically 2V), and D is the duty cycle of PWMVID input.

Boot Voltage and Standby Mode

The new generation PWMVID structure includes two operation modes other than normal operation: boot mode and standby mode. During boot mode, the GPU stops sending PWMVID signal and the input of the PWMVID buffer is floating. The REFADJ pin enters high impedance state after the VID pin enters tri-state region, and the REFIN voltage can then be calculated as:

$$V_{REFIN,BOOT} = V_{VREF} \times \frac{R4+R5}{R2+R3+R4+R5}$$

During standby mode, other than GPU stopping the PWMVID transaction, an external system standby signal additionally controls the entry of standby mode. An additional external switch should be connected in parallel with the original PWMVID resistors as shown in Figure 3 to generate the standby mode voltage:

$$V_{REFIN,STDBY} = V_{VREF} \times \frac{(R3+R4+R5)//R_{STDBY}}{R2+(R3+R4+R5)//R_{STDBY}} \times \frac{R4+R5}{R3+R4+R5}$$

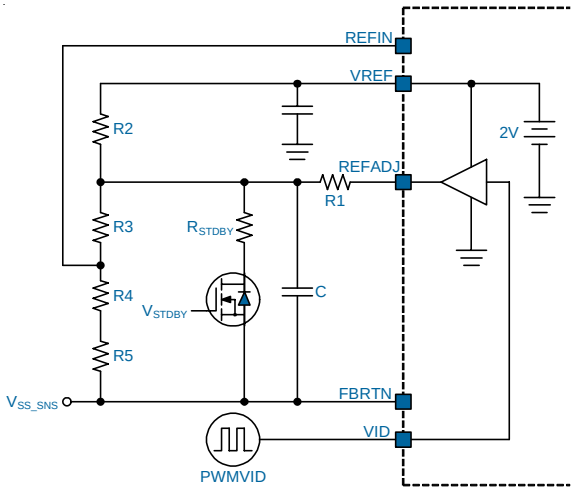


Figure 3. Standby Mode Configuration

Channel Current Balance

The uP9509 senses phase currents for current balance by the means of on-resistance of power stage low-side MOSFET as shown in Figure 4.

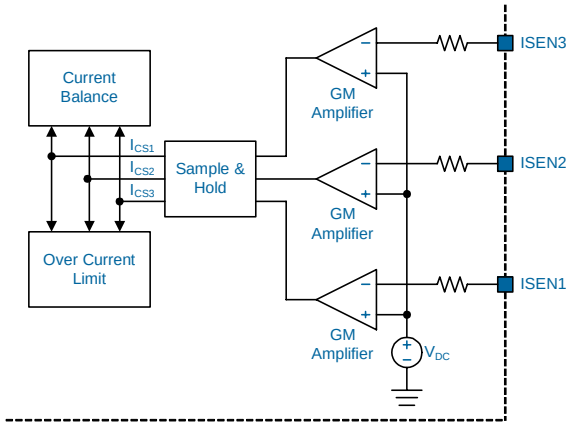


Figure 4. $R_{DS(ON)}$ Current Sensing Scheme

The GM amplifier senses the voltage drop across the low-side MOSFET and converts it into current signal each time it turns on. The sampled and held current is expressed as:

$$I_{CSX} = \frac{(I_{LX} \times R_{DS(ON)} + V_{DC})}{R_{ISENX}}$$

where I_{LX} is the phase N current in Ampere, $R_{DS(ON)}$ is the on-resistance of low-side MOSFET of the power stage in mΩ, V_{DC} is an internal 30mV voltage source, and R_{ISENX} is the external sensing resistor connected at ISENx pins. In this current sense mechanism, the valley of the inductor current is sampled and held. Therefore, the equivalent sensed current can be described by the following equation:

$$I_{LX\_SH} = I_{LX\_AVG} - \frac{1}{2} \times \Delta I_{LX}$$

The sensed current I_{LX_SH} is mirrored to the current balance circuit, comparing between each other, and generating current adjusting signals for each phase. These current adjusting signals are fed to the on-time circuit of the uP9509 to separately adjust each phase on-time for the purpose of adjusting current balance.

Soft-Start and Power Good

A built-in soft-start is used to prevent surge current from power supply input during turn on. The error amplifier is a three-input device. Reference voltage V_{REFIN} or the internal soft-start voltage SS whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. SS internally ramps up to PVCC with a slew rate determined by V_{REFIN} after the soft start cycle is initiated. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level. The output voltage ramp-up time can be selected through a resistor which is connected from LGATE2 to GND. The output ramp-up selection table shown as following table.

Functional Description

R_{LG2}	Output Voltage Ramp Up Time
15k	150us
20k	500us
30k	1ms
Open	1.5ms

Table 1. Output Ramp Up Time Setting

Power Saving Mode

The uP9509 provides power saving features for platform designers to program platform specific power saving configuration. There are four operation modes: multi-phase CCM, multi-phase DCM, single-phase CCM, and single-phase DCM. The uP9509 switches between these four operation modes according to the input voltage level of the PSI pin. Figure 5 shows typical PSI application circuit, and table 1 shows recommended PSI setting voltage level of four operation modes. In single-phase operation, the uP9509 auto-selects phase 1 to be the operating phase. In DCM, the uP9509 automatically reduces switching frequency at light load to maintain high efficiency. As the load current decreases, the rectifying MOSFET is turned off when zero inductor current is detected, and the converter runs in discontinuous conduction mode.

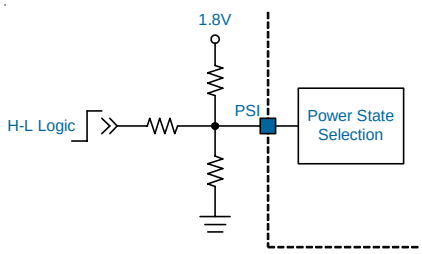


Figure 5. PSI application circuit

Operation Mode	Recommended Voltage Setting at PSI
Multi-Phase CCM	1.8V
Multi-Phase DCM	1.2V
Single-Phase CCM	0.6V
Single-Phase DCM	GND

Table 2. Recommended PSI Setting

Over Current Limit

The uP9509 monitors the inductor valley current by low side MOSFET $R_{DS(ON)}$ when it turns on. The over current limit is triggered once the sensing current level is higher than V_{OC}. When triggered, the over current limit will keep high side MOSFET off even the voltage loop commands it to turn on.

The output voltage will decrease if the load continuously demands more current than current limit level. The current limit threshold is set by connecting a resistor (Roc) from LGATE1 to GND. The voltage across PHASE and GND pins is compared with V_{OC} for current limit. The current limit threshold is calculated as:

$$I_{LIM}(A) = \frac{V_{OC}(mV)}{R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

And , Roc resistance can be calculated as:

$$R_{OC}(k\Omega) = \frac{500mV}{\frac{V_{OC}(mV) - 20mV}{180mV} \times \frac{255}{8}(uA) + 5uA}$$

V_{OC} is the per-phase GND-PHASE voltage when the power stage low-side MOSFETs is turned-on; $R_{DS(ON)}$ is the on-resistance of equivalent per-phase power stage low side MOSFET and I_{RIPPLE} is the peak-to-peak inductor ripple current at steady state.

Over Voltage Protection (OVP)

The OVP is triggered if V_{FB} > 1.5xV_{REFIN} sustained 6us. When OVP is activated, the uP9509 turns on all low-side MOSFET and turns off all high-side MOSFET. The over voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Under Voltage Protection (UVP)

The under voltage protection is triggered if V_{FB} < 0.5xV_{REFIN} sustained 10us. When UVP is activated, the uP9509 turns off all high-side and low-side MOSFET. The under voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Over Temperature Protection (OTP)

The uP9509 monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP9509 is forced into shutdown mode. The over temperature protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, PVCC ---------- -0.3V to +6.5V

BOOTx to PHASEx

DC ---------- -0.3V to +6V

PHASEx to GND

DC ---------- -0.7V to +28V

< 100ns ---------- -8V to +36V

BOOTx to GND

DC ---------- -0.3V to +34V

< 100ns ---------- -5V to +42V

UGATEx to PHASEx

DC ---------- -0.3V to +6V

< 100ns ---------- -5V to +7V

LGATEx to GND

DC ---------- -0.3V to +6V

< 100ns ---------- -5V to +7V

Other Pins ---------- -0.3V to +6V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

HBM (Human Body Mode) ---------- 2kV

MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

VQFN4x4 - 24L θ_{JA} ---------- 40°C/W

VQFN4x4 - 24L θ_{JC} ---------- 4°C/W

Power Dissipation, P_D @ T_A = 25°C

VQFN4x4 - 24L ---------- 2.5W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Input Voltage, V_{IN} ---------- 4.5V to 26V

Control Voltage, V_{PVCC} ---------- 4.5V to 5.5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(PVCC = 5V, T_A = 25°C, unless otherwise specified)

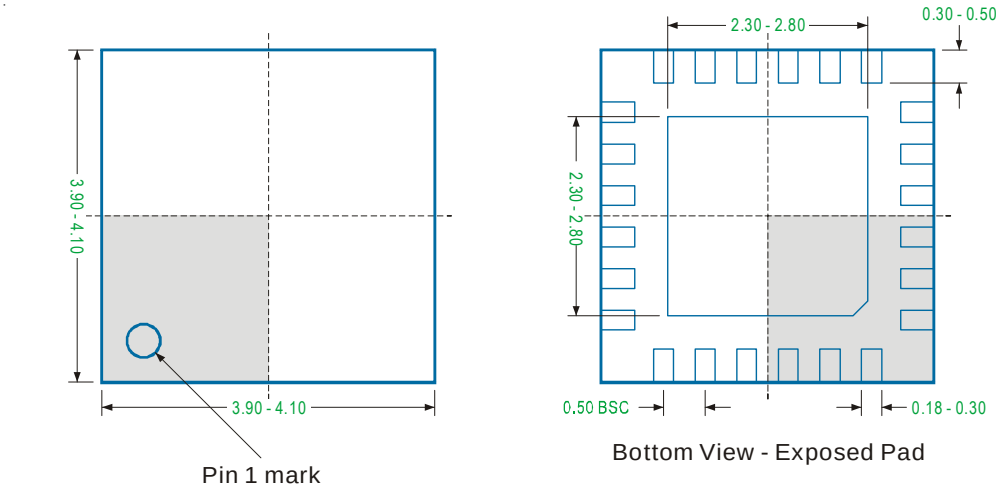
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Quiescent Current	I_Q	V_{REFIN} = 0.9V, EN = 1.8V, V_{FB} = 1V, no switching	--	1	--	mA
Shutdown Current	I_{SHDN}	EN = 0V	--	2	--	uA
PVCC POR Threshold	$V_{PVCCRTH}$	V_{PVCC} rising	3.9	4.1	4.3	V
PVCC POR Hysteresis	$V_{PVCCHYS}$		--	0.3	--	V
VREF Voltage Accuracy	V_{REF}		1.98	2	2.02	V
VREF Sourcing Current	I_{REF}		10	--	--	mA
Control Input: EN						
Logic Low Threshold	V_{EN_L}		--	--	0.6	V
Logic High Threshold	V_{EN_H}		1.2	--	--	V
Internal Pull-down Current	I_{EN}		--	10	--	uA
Reference Voltage						
REFIN Disable Threshold			--	0.1	--	V
External Rererence Voltage Range	V_{REFIN}		0.2	--	2	V
On Time						
One Shot Width	T_{ON}	V_{IN} = 12V, V_{OUT} = 1.2V, F_{SW} = 300kHz	--	333	--	ns
Minimum Off Time	T_{OFF_MIN}		--	300	--	ns
Minimum On Time	T_{ON_MIN}		--	80	--	ns
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	--	70	--	dB
Gain Bandwidth Product	$G_{EW(EA)}$	Guaranteed by Design	--	10	--	MHz
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Trans-conductance	GM		--	2020	--	uA/V
Maximum Current (Source & Sink)	I_{COMP}		300	--	--	uA
Current Sense Amplifier (Current Balance)						
Input Offset Voltage	V_{OFF_CSA}		-1	--	1	mV
Max Sourcing Current	I_{SRC_CSA}		100	--	--	uA
ISENx Voltage	V_{DC_CSA}		25	30	35	mV
Internal Current Sense Resistance	R_{SENX_INT}		--	4	--	kΩ
FBRTN						
FBRTN Current	I_{FBRTN}	EN = 1.4V, no switching	--	--	500	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Soft Start						
Initialization Time at POR	T_{INIT_POR}		--	--	350	us
Initialization Time	T_{INIT}		--	--	250	us
PWMVID Buffer						
VID Input Low Level	V_{IL_VID}		--	--	0.6	V
VID Input High Level	V_{IH_VID}		1.2	--	--	V
VID Tri-state Delay	T_{TRI_VID}		--	100	--	ns
V_{REFADJ} Source Resistance	R_{BF_SRC}	I_{SRC} = 1mA	--	20	--	Ω
V_{REFADJ} Sink Resistance	R_{BF_SNK}	I_{SNK} = 1mA	--	20	--	Ω
PSI						
Power Saving Mode Logic	V_{PSI}	Multi-Phase CCM	1.6	--	--	V
		Multi-Phase DCM	1	--	1.4	V
		Single-Phase CCM	0.4	--	0.8	V
		Single-Phase DCM	--	--	0.2	V
Gate Drivers						
Upper Gate Source	R_{UG_SRC}	I_{UG} = -80mA	--	1	2	Ω
Upper Gate Sink	R_{UG_SNK}	I_{UG} = 80mA	--	0.5	1	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = -80mA	--	1	2	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 80mA	--	0.4	0.8	Ω
Dead Time	T_{DT}		--	30	--	ns
Internal Bootstrap Schottky Diode						
Forward Voltage	V_F	Forward Bias Current = 3.5mA	--	0.33	--	V
Zero Current Detection Threshold						
Zero Current Threshold	V_{ZC}		-0.5	--	0.5	mV
Protection						
OCP Threshold	V_{OC}		20	--	200	mV
OVP Threshold	V_{OVP}	V_{FB}/V_{REFIN}	150	--	--	%
UVP Threshold	V_{UVP}	V_{FB}/V_{REFIN}	40	--	50	%
OTP Threshold			--	150	--	°C
Power Good Indicator						
PGOOD Output Low Level		I_{SINK} = 4mA	--	--	0.3	V
Leakage Current		V_{PG} = 5V	--	--	0.1	uA

Package Information

VQFN4x4 - 24L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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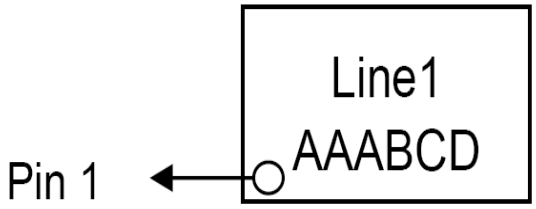
Top Marking Rule



Line 1 : Product Code

Part No.	Product Code
uP9509PQAG	**uP9509P**

Line 2 :
AAA - uPI internal trace code
BCD - Date Code, rules as below:

B：Last one of western calendar year (0~9), ex. 2007=7, 2008=8

C：Month

Month	Code	Month	Code	Month	Code	Month	Code
Jan	1	Apr	4	Jul	7	Oct	A
Feb	2	May	5	Aug	8	Nov	B
Mar	3	Jun	6	Sep	9	Dec	C

D：Date

Date	Code	Date	Code	Date	Code	Date	Code
1	1	9	9	17	H	25	S
2	2	10	A	18	J	26	T
3	3	11	B	19	K	27	U
4	4	12	C	20	L	28	V
5	5	13	D	21	M	29	W
6	6	14	E	22	N	30	X
7	7	15	F	23	P	31	Y
8	8	16	G	24	R		

VQFN4x4 Package –uP9509PQAG

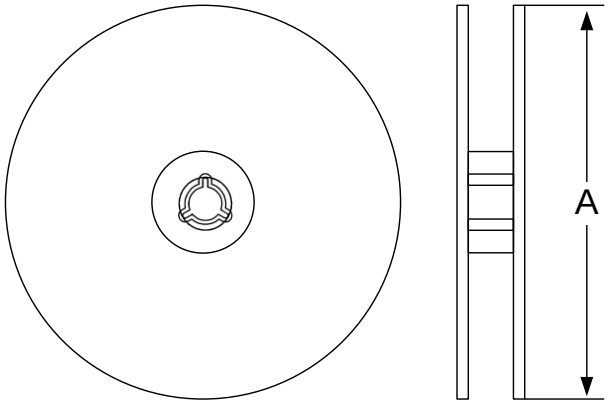
Definition:

QFN = Quad Flat No Lead

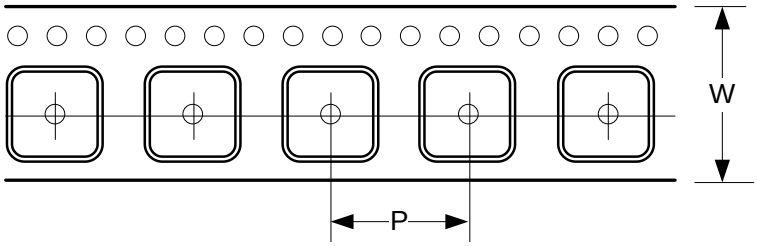
V Type= Very Thin Package(Thickness = 0.9 ± 0.1mm)

Tape & Reel Drawing

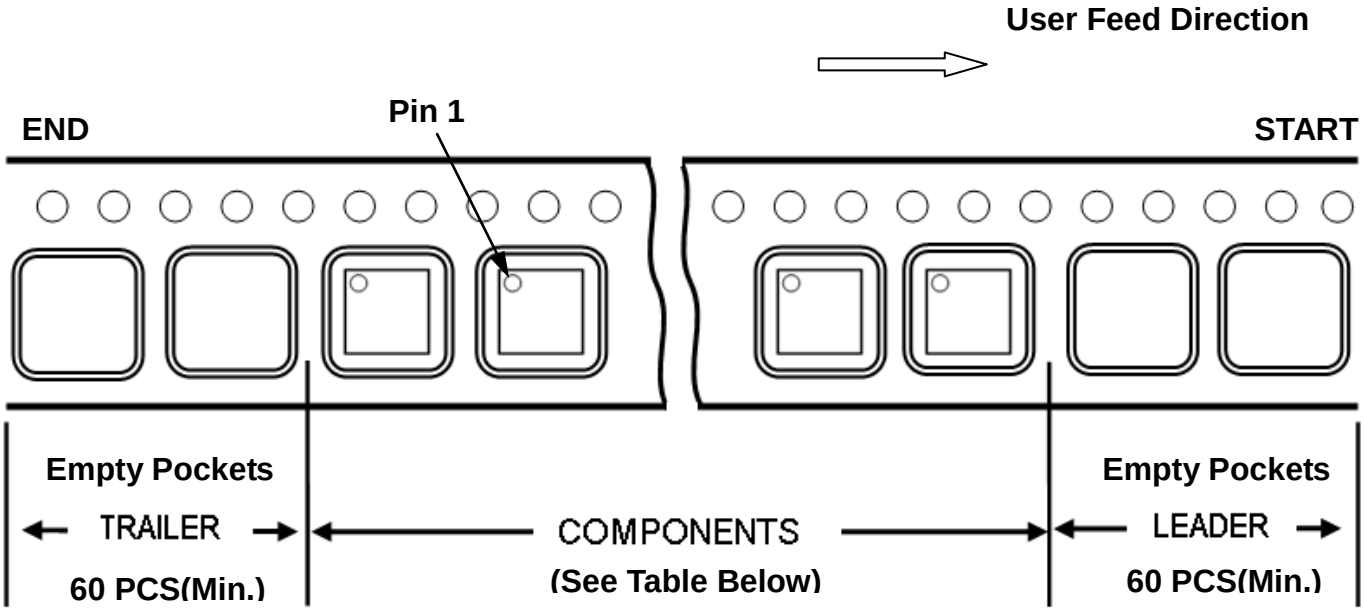
Lock Reel



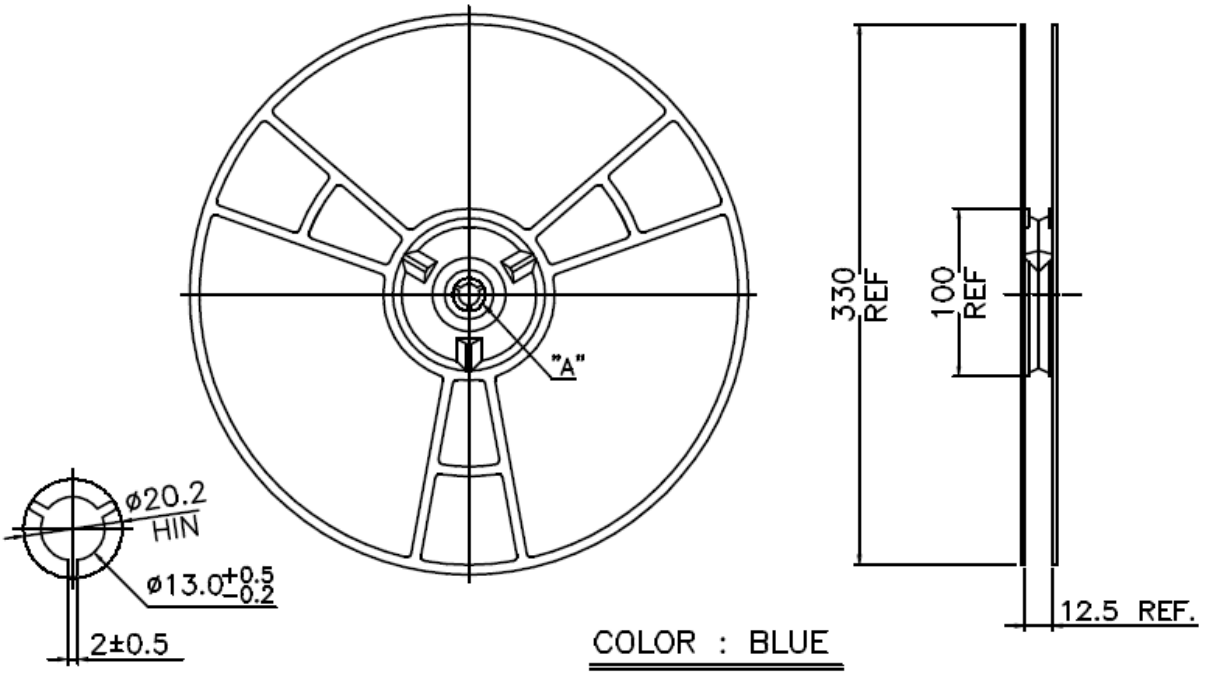
Carrier Tape

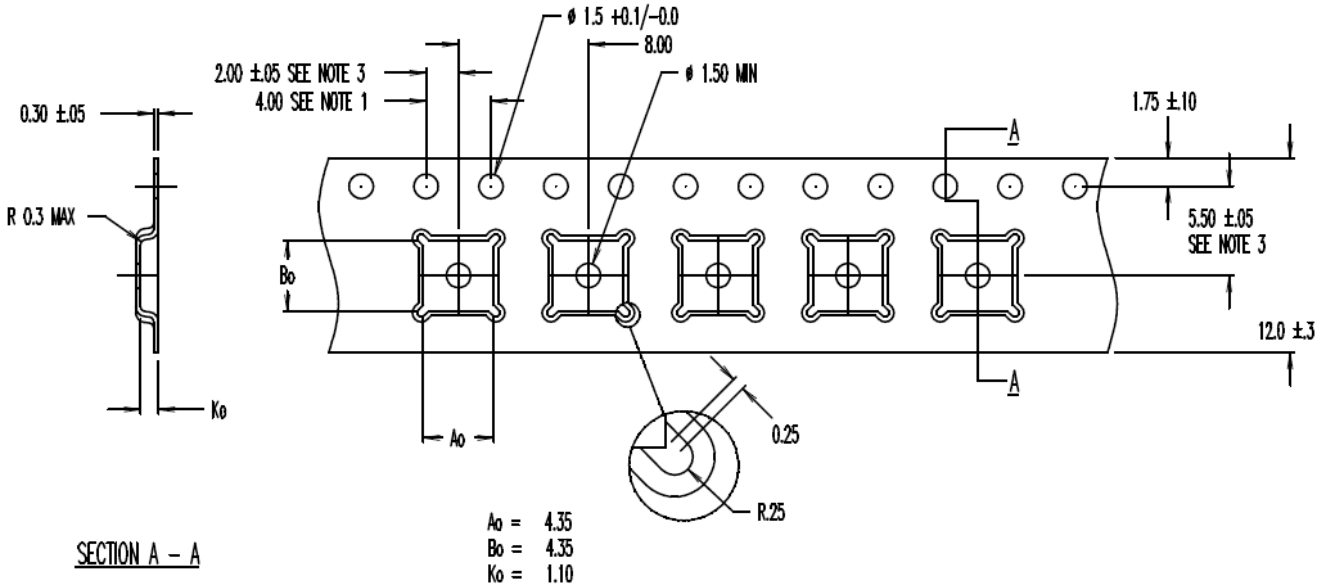


Packing Illustration



Carrier Tape Drawing





Packing Quantity List

PKG Type Body Size	Reel Diameter(A) (inch/mm)	Carrier Width(W) (mm)	Carrier Pitch(P) (mm)	Reel Quantity (pcs)	Remark
VQFN 4x4	13 / 330	12	8	2500	

Packaging Drawing

Barcode Label – Apply for Reel/Al Bag/Inner Box and Outer Carton

P/N：uPI Part Number

LOT：Wafer Lot Number

QTY：Packing Quantity

D/C：Manufacturing Date Code

DATE：Packing Date

Note：For Internal Use Only

Inner Box

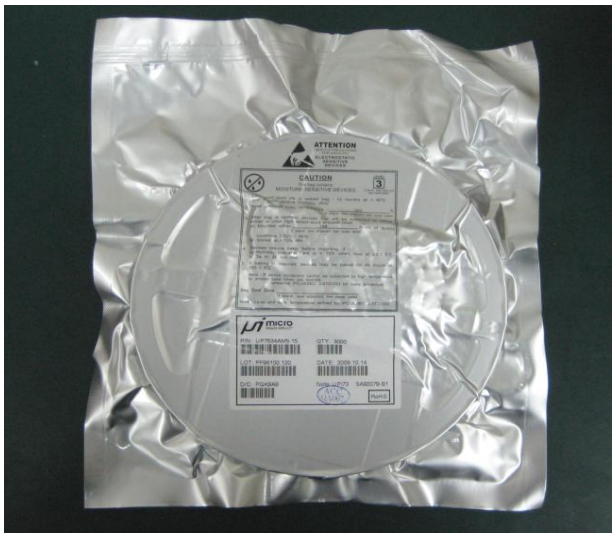
Box (13” Reel 355 x338 x 50 mm)

Outer Carton

Carton A (382 x 283 x390 mm)

Package Storage Condition:

- Vacuum Sealed into Moisture Barrier Bag and Meet MSL Level 3 requests.
- Comply with J-STD-033 standard.



- Storage Condition

  Vacuum Sealed : 12 months at <40℃ and 90%RH

  Bag Opened : Within 168 hrs at < 30℃ / 60%RH

- Baking Condition

  Re-Backing @ 125℃ +/- 5 ℃, 9hrs for IC only;

  Floor life begins counting at time =0 after Re-Backing.

  The times of Re-Backing: 2 times, Max.