<Variant Name>

Title

PCI-E RV370 128M TSOP VO-SV/DI

Schematic No. 105-A260xx-10

Date: **Tuesday, May 25, 2004**

REVISION HISTORY

Rev 6

Sch Rev	Date	REVISION DESCRIPTION
0 00A	2003-09-10	PRELIMINARY BASED ON 105-A181xx-00A and 105-A200xx-00 - Use 402 R and C footprints as preferred - (pg1) Add 0R bypass for PERST#, and use XOR spared gate for buffer - (pg1) Keep only 1 100uF decoupling for +12V_BUS - (pg1) Connect B3 of edge connector directly to +12V_BUS - (pg2) Remove oscillator and change crystal to surface mount - (pg2) Hard pull-down on TEST_Y/MCLK - (pg2) Remove thermal interrupt, no provision for speed controlled fan - (pg2) Remove redundant TPs - (pg2) Pull-up on DVPCNTL_[3:0], remove RageTheater capture ports (VID/DVO[7:0]) - (pg2) DVOMode pull-up to 1.8V, set to 12-bit DVO (1.8V DVO I/O signalling) - (pg3) Memory interface based on A198, remove Channel B - (pg4) Remove power-up diodes - (pg5, 6, 7) Redesigned power regulators - (pg8, 9) Channel A only Series-Terminated TSOP interface (based on A200) - (pg11, 12, 13) Front-end based on Low-Profile VGA/DVI + VO design (based on A200)
	2003-09-22	- (pg5) Add RC snubber circuit on switching regulator - (pg7) Add R124 for power dissipation
	2003-10-16	- (pg14) Add MT2, second mounting hole - (pg6 and 7) Remove R817, option for sharing REG8 and REG9, due to layout concerns - (pg4) Add C979..C985 On request of EMI team. These are for decoupling ajacent planes. - (pg6) Make RP2 dual footprint with 0402 Caps C986..C989. Created a similar circuit using RP195 and C990..C993. The RP can be used to short +MVDDQ and +MVDDC, and the caps can be used to decouple the planes. - (pg6) Add C973..C978 Decoupling caps. These are placed accross +MVDDQ/+MVDDC plane splits - (pg11) Remove R994..R996 stitching GND to Chassis GND.
1 00B	2003/11/14	- (Layout) Change to 6-layer PCB - (Layout) Change PCIE test points - (pg1) Change PCIE test points, add 3.3V_BUS polymer cap, add R1244 - (pg2) Add R23 for DVO pull-down - (pg4) Add B15 for +3.3V_BUS VDDR4 alternate, change PCIE regulators filter from 100nF to 1uF - (pg5) Add stand-alone +PCIE_VDDR, +PCIE_PVDD12 and +PCIE_PVDD18 regulators, improve power sequence circuit - (pg5) Add R315 and R316 to select +12V_BUS or +5V for boot circuit, change R368 footprint to 603 - (pg6) Add C314 and C315 for MVDDC and MVDDQ, 1.8V from PCIE_PVDD18 - (pg7) Remove R124, add polymer cap for PCIE_PVDD18, add +PCIE_VDDR and +PCIE_PVDD12 tied option and single package FET for +PCIE_VDDR - (pg14) Add fan connector
2 00C	2004/03/05	- (pg02, 10) Fix pull-up +VDD_DVO to +VDDR4 - (Layout) TVO filters move close to connector - (pg04) Remove CP2, 3, 4, 5, 6 and 8 for dual footprint manufacturing issues (Capacitor packs sharing with 402 footprints) - (Layout) Components using the same foot print. (remove MC2) - (pg06) Remove C986, C987, C988, C989, C990, C991, C992 and C993 - (pg06) Add C800 for options - (pg11) +5V supply with current limiting for VESA DDC spec, remove F1, B21 - (pg05) Remove dual-packaged MOSFET - (Layout/EMI) C507, C508, C509, R513, R514, R515 (added), L60, L61 and L62 connect to digital Gnd instead of chassis Gnd.
3 00E 00D and 00E are in parallel	2004/04/16	- (pg04) Remove redudant dual-footprint capacitor array - (pg11) Add R994, extra resistor to tide chassis/digital ground - (pg12) Add R916 and R917 for +5V_VESA resistor dissipation to meet 70% derating spec - (pg13) Remove R513 and R514 and tide TVO MiniDIN shield directly to chassis ground
4 00D 00D and 00E are in parallel	2004/04/16	- (pg11, 12, 13 and 14) Change chassis ground to digital ground - (pg11) Remove R991, R992, R993, R994, R997, R998 and R999 for chassis/digital ground tide - (pg12) Change DVI-I connector to fully-shielded connector - (pg14) Remove Mounting Hole MT2 - (Layout) Remove TMDS ground guards
5 00	2004/04/27	Released based on -00D PCB (not -00E) - (pg05) Tide R357 to +3.3V instead of +12V for proper power sequence

<Variant Name>

Title	Schematic No.	Date:
PCI-E RV370 128M TSOP VO-SV/DI	105-A260xx-10	**Tuesday, May 25, 2004**

REVISION HISTORY

Rev 6

Sch Rev	Date	REVISION DESCRIPTION
6 10	2004-05-11	(pg01) Add 1K resistor on PCIE transmit (R701~R732)

PCI-EXPRESS EDGE CONNECTOR

+12V_BUS
C5 100uF_16V
DNI

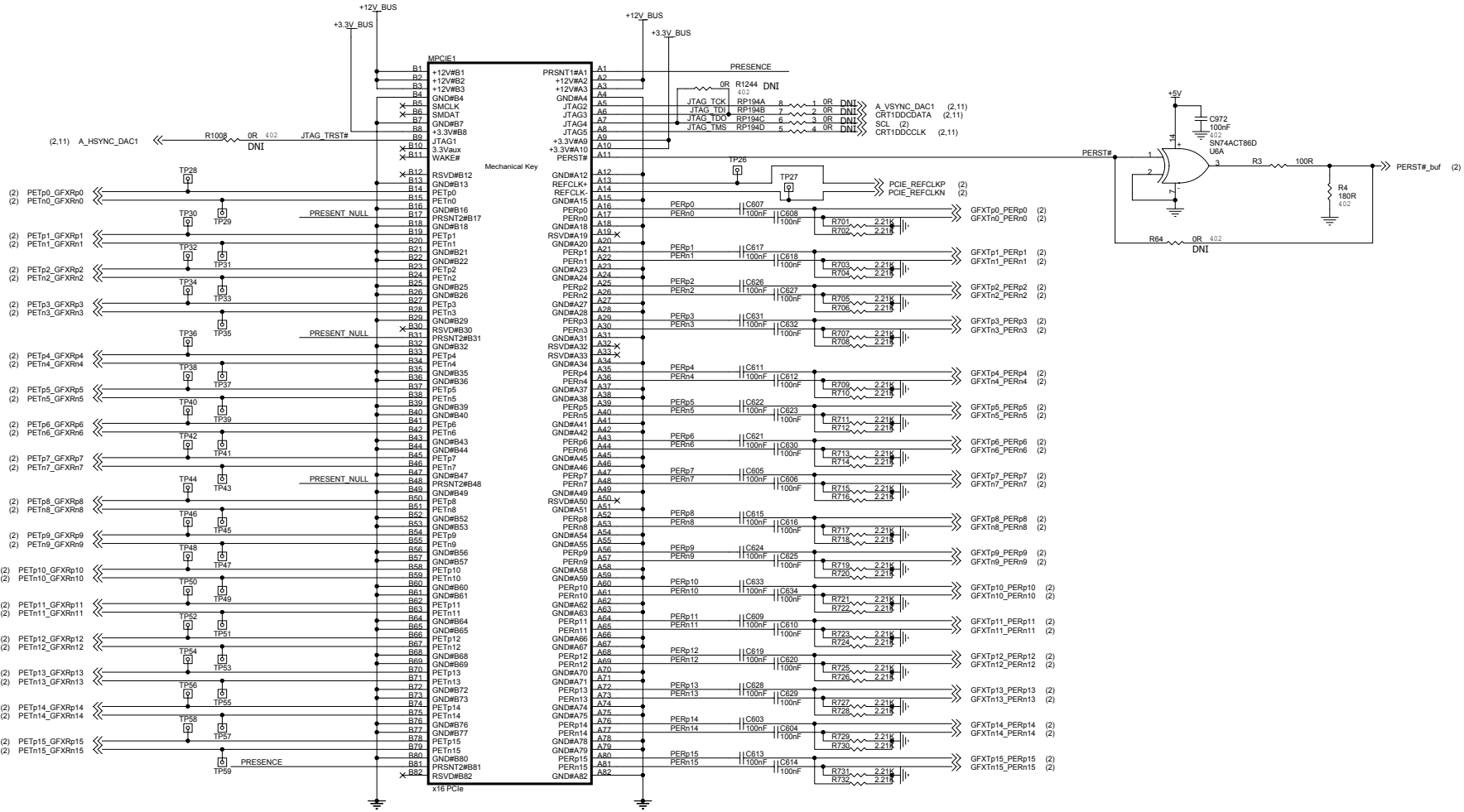
+3.3V_BUS
C8 100uF_16V >=6.3V
DNI

+3.3V_BUS
C2 47uF_16V >=6.3V
DNI

USE 47uF TANTALUM CAPACITOR OR HIGHER

GND_MPVSS GND_TPVSS GND_A2VSSN GND_AVSSQ GND_RSET
GND_AVSSN GND_PVSS GND_TXVSSR GND_A2VSSQ GND_R2SET

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

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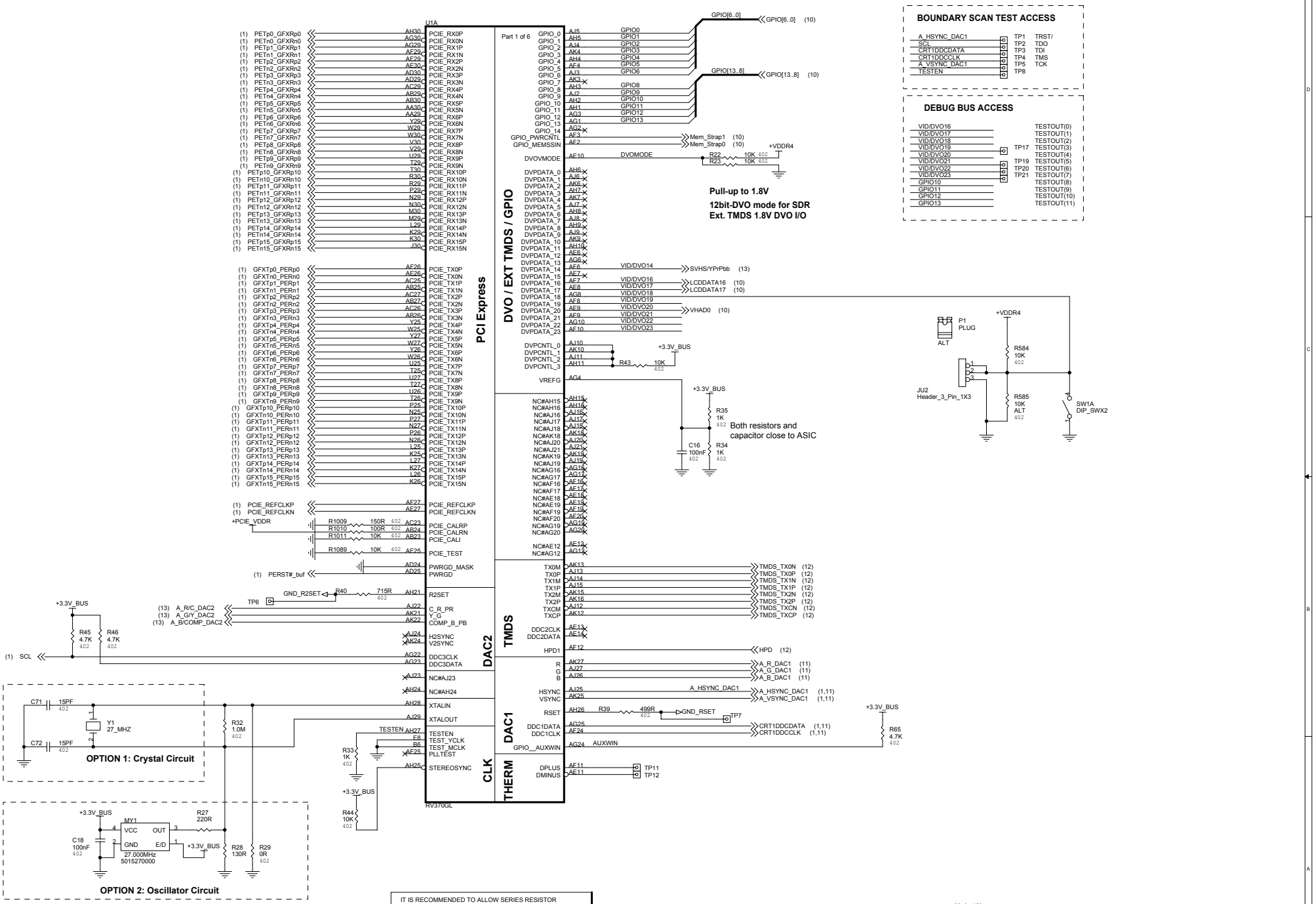

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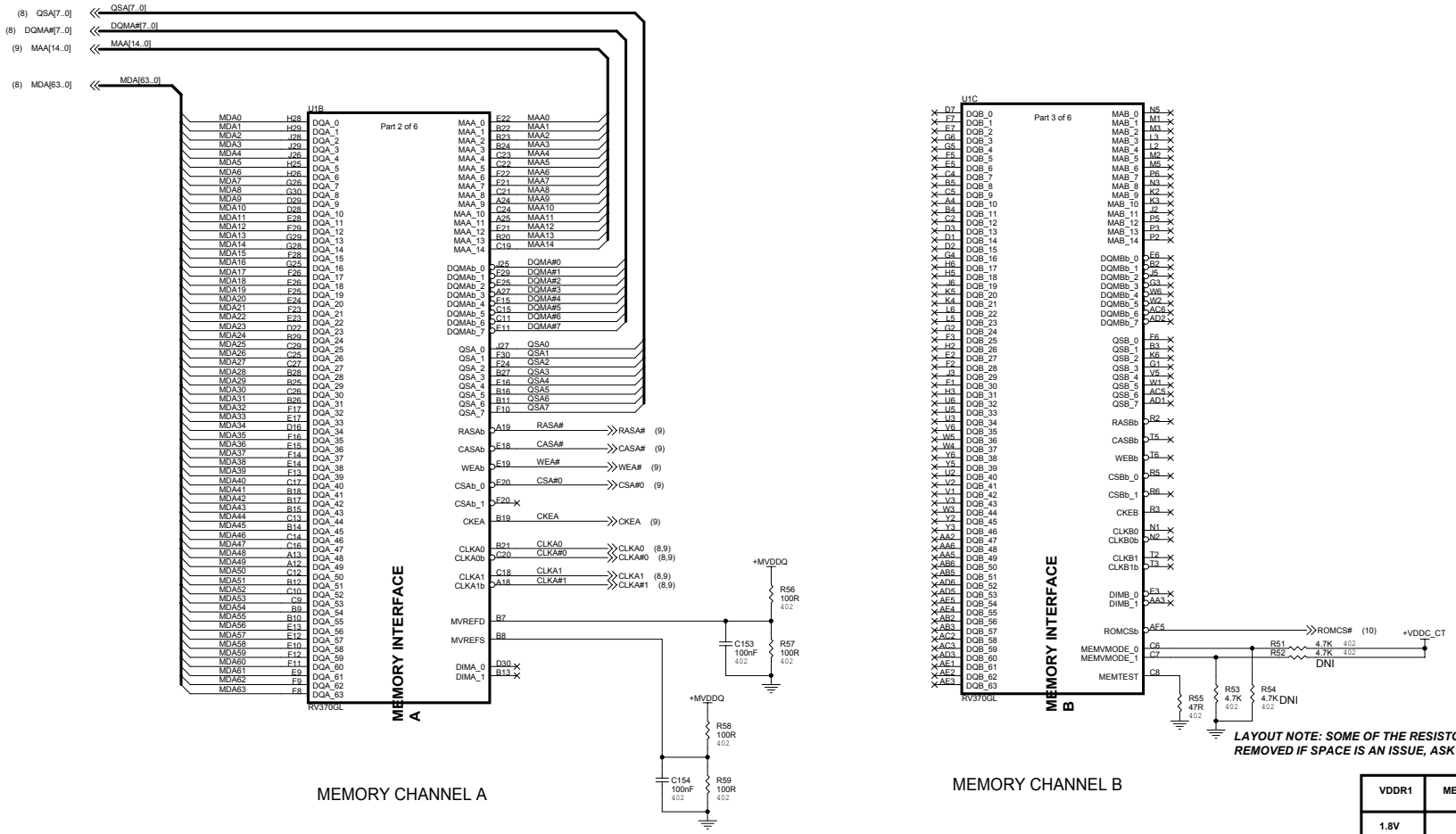

MEMORY CHANNEL A

PLACE C351/152 VERY CLOSE TO ASIC
R56/57/58/59 CLOSE TO ASIC AS WELL

MEMORY CHANNEL B

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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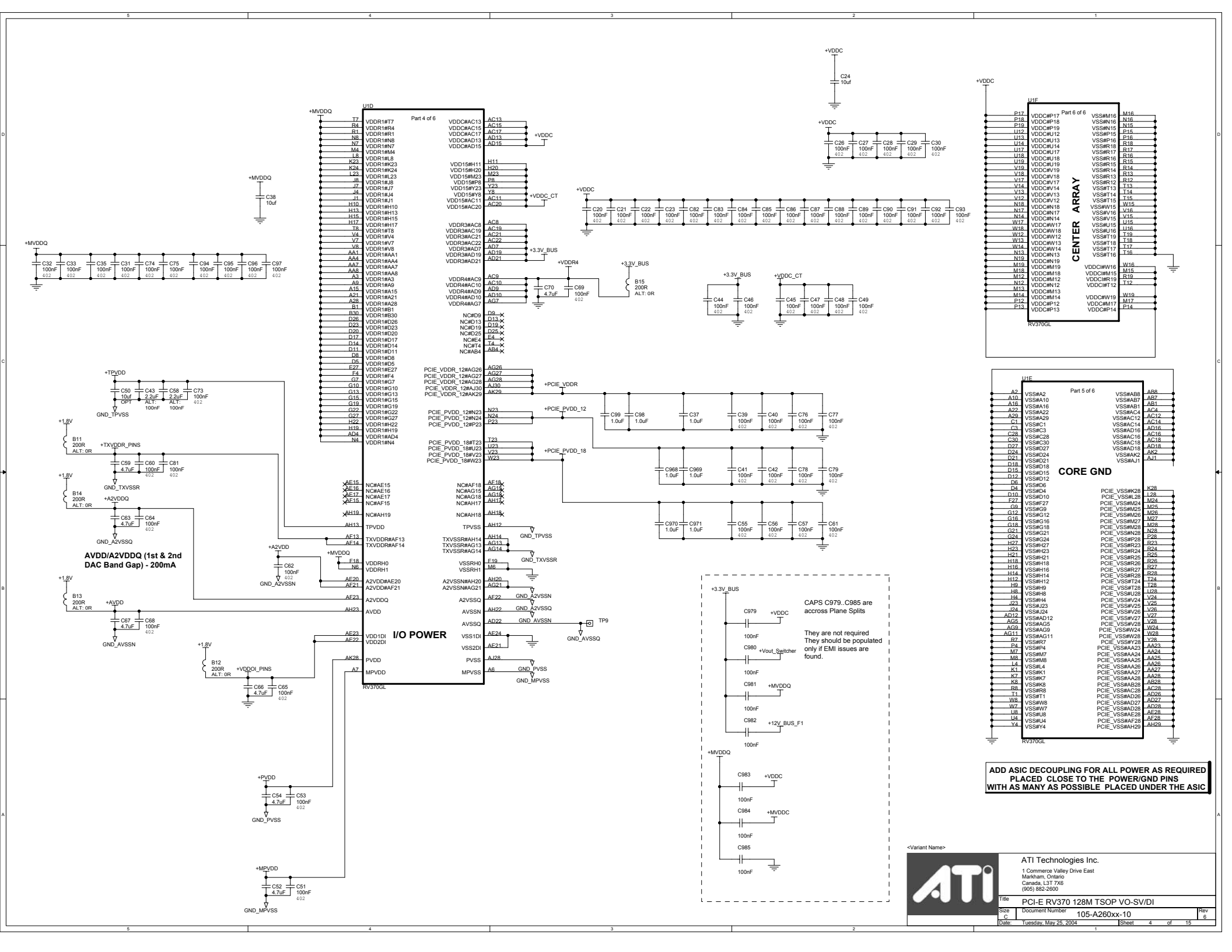
U1D
Part 4 of 6
RV370GL
I/O POWER
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
U1F
Part 6 of 6
CENTER ARRAY
RV370GL
U1E
Part 5 of 6
CORE GND
RV370GL
CAPS C979..C985 are accross Plane Splits
They are not required They should be populated only if EMI issues are found.
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED PLACED CLOSE TO THE POWER/GND PINS WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
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Regulator for VDDC (ASIC Core)

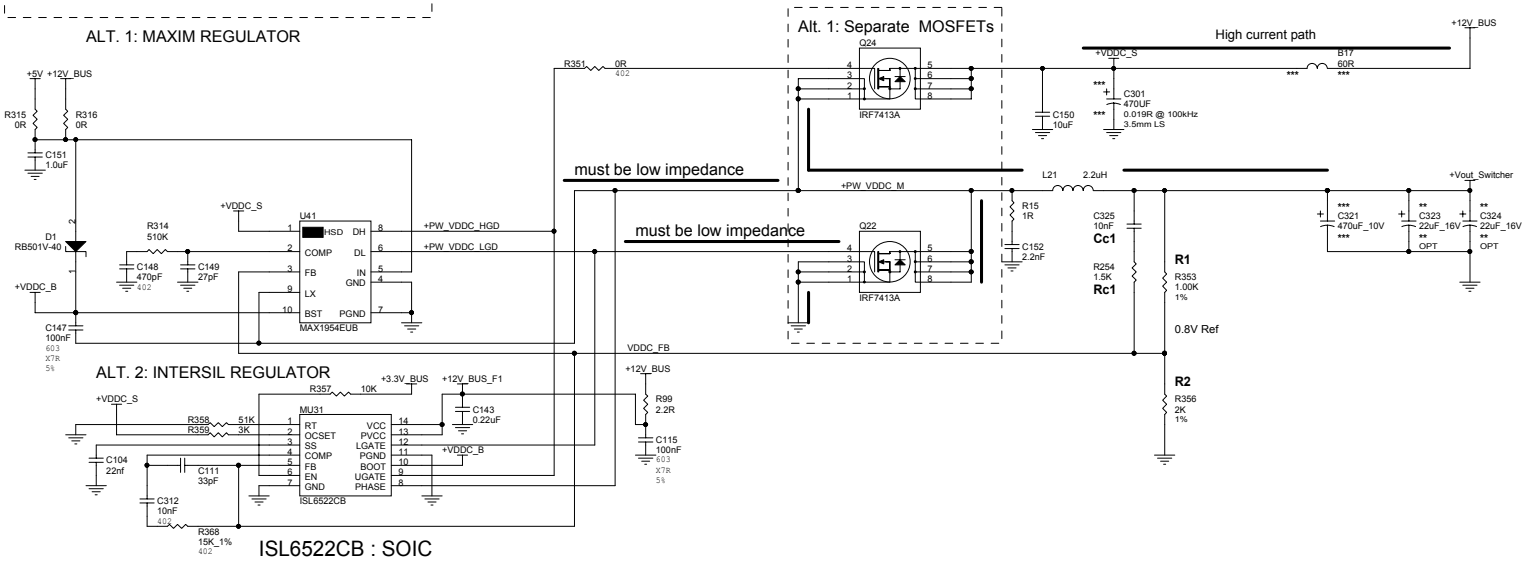
Vout = 1.2V ~ 1.3V

*** Indicate number of power via required for the connection

Part	NOTES
MAX1954	Do not install Cc1, Rc1
ISL6522	Install Cc1, Rc1

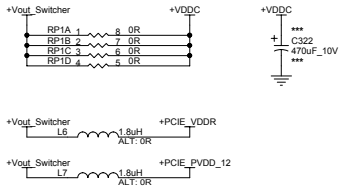
Part	Vout	R1	R2
MAX1954 ISL6522	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
0.8V Ref	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100

ALT. 1: MAXIM REGULATOR



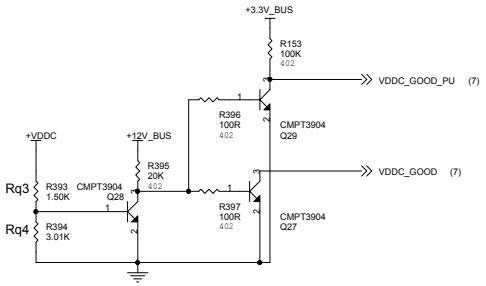
ALT. 2: INTERSIL REGULATOR

ISL6522CB : SOIC



Circuit to hold PCI-E voltage low and wait for +VDDC for proper power sequence

+VDDC	Rq3	Rq4
+1.3V	1.5K	2.4K
+1.2V	1.5K	3K



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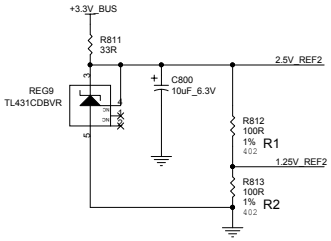
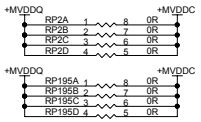
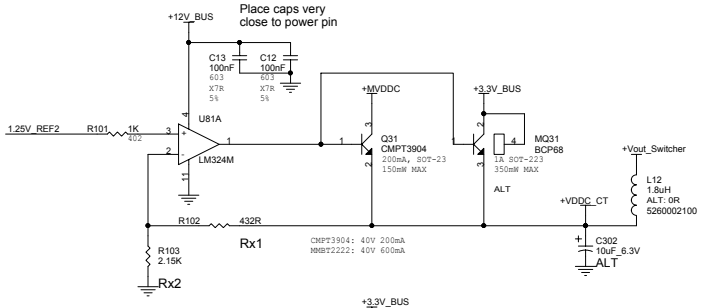


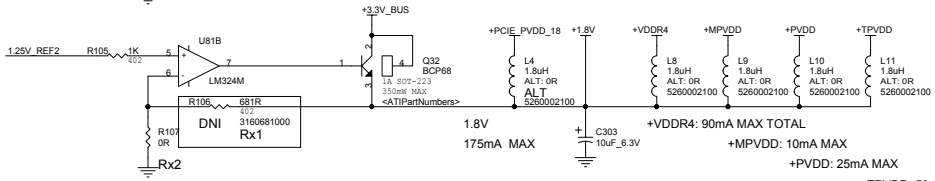
Voltage Req.	R1	R2
0.8V	150R P/N 3160150000 402	71.5R P/N 324075R500
1.25V	100R P/N 3160100000 402	100R P/N 3160100000 402
1.5V	100R P/N 3160100000 402	150R P/N 3160150000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.55	475R (402, 1%) P/N 3160475000	2K (402, 1%) P/N 3160200100
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240015200

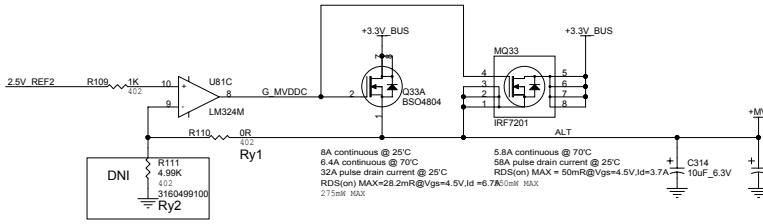
Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.61V	221R (402, 1%) P/N 3160221000	4.99K (402, 1%) P/N 3160499100
2.5V	0R P/N 3230000000 603 P/N 3150000000 402	DNI

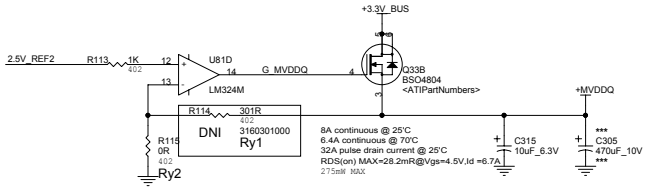




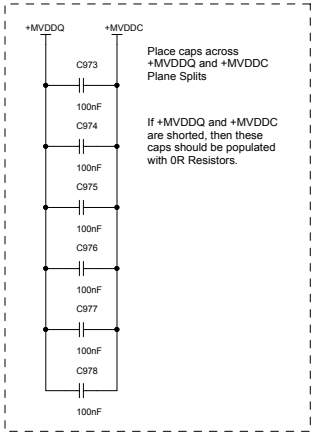


Rails derived from +VDDR4
+AVDD: 10mA MAX
+A2VDDQ: 20mA MAX
+VDDQI_PINS: 20mA MAX
+TXVDDR_PINS: 20mA MAX



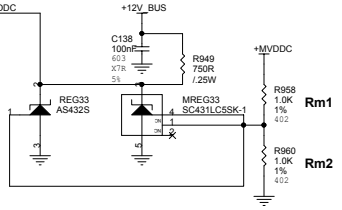


	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100



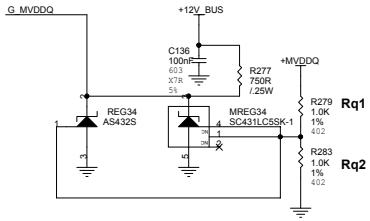
Alt. regulator for +MVDDC
Vout = 2.5V ~ 2.6V
Iout = 500mA MAX

Voltage Req.	Rm1	Rm2
3.34V [-0.04V/+0.04V]	4.32K	2.55K
3.45V [-0.04V/+0.04V]	4.32K	2.43K
2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100

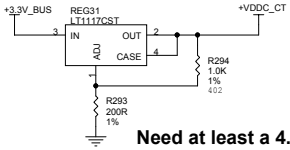


Alt regulator for +MVDDQ
Vout = 2.5V ~ 2.6V
Iout = 200mA MAX

Voltage Req.	Rq1	Rq2
1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
2.5V	1K 3240100100	1K 3240100100
2.6V	4.75K 3240475100	4.32K 3240432100

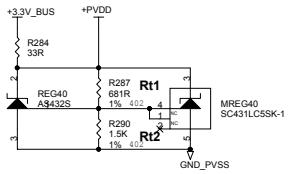


Alt regulator for +VDDC_CT
Vout = 1.5V
Iout = 150mA MAX

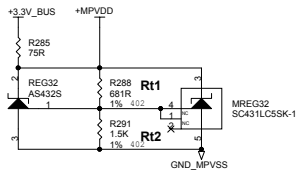


Need at least a 4.7uF output cap for stability

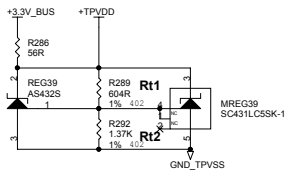
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



Alt regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX



Alt. regulator for +TPVDD
Vout = 1.65V ~ 1.85V
Iout = 20mA MAX



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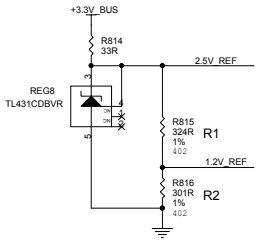
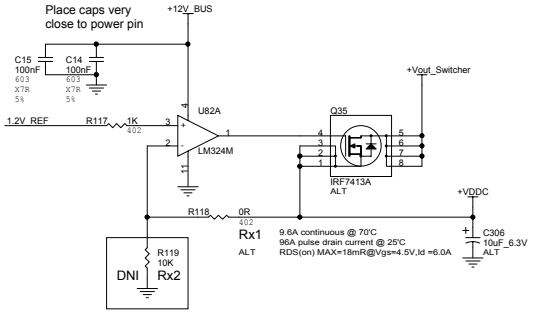
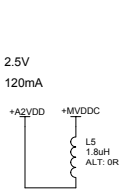
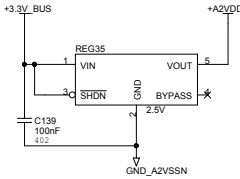




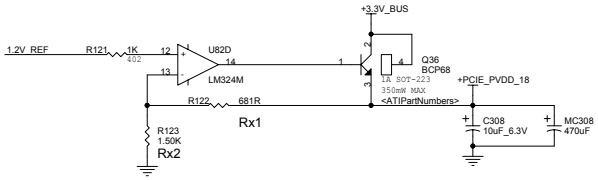
1.3V
8A MAX
MIGHT NEED HEATSINK ON FET



Alt. regulator for +A2VDD
Vout = 2.5V
Iout = 120mA MAX

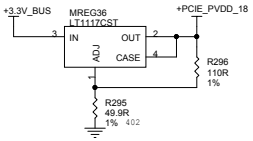


+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.



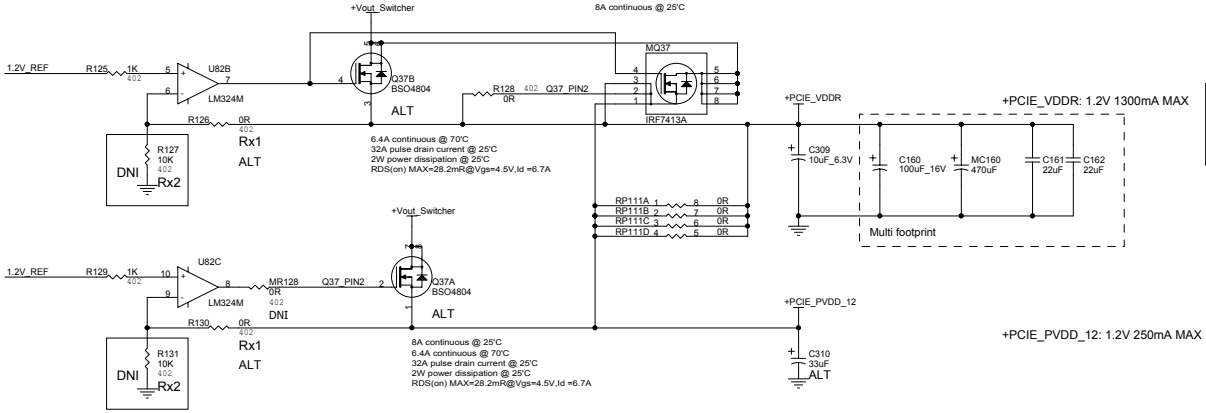
+PCIE_PVDD_18: 1.8V 500mA MAX

Alt. regulator for PCIE_PVDD_18
Vout = 1.82V
Iout = 500mA MAX



Need at least a 10uF Tant. output cap for stability
Min. Load Current: 10mA

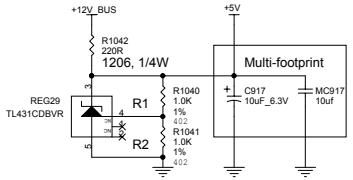
Optional when +Vout_Switcher is above 1.2V

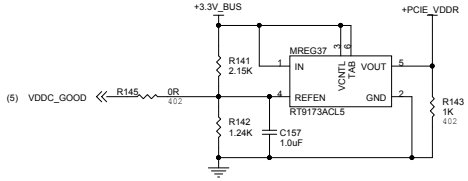


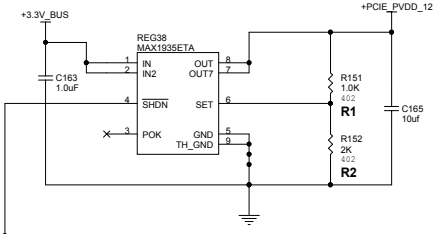
+PCIE_VDDR: 1.2V 1300mA MAX

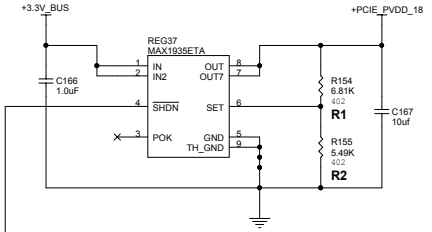
+PCIE_PVDD_12: 1.2V 250mA MAX

Regulator for +5V
Vout = 5V
Iout = 20mA MAX









Part	Vout	R1	R2
MAX1935 0.8V Ref	1.2V	1.00K 1% 402 ATI P/N 3160100100	2.00K 1% 402 ATI P/N 3160200100
	1.79V	6.81K 1% ATI P/N 3160681100	5.49K 1% 402 ATI P/N 3160549100

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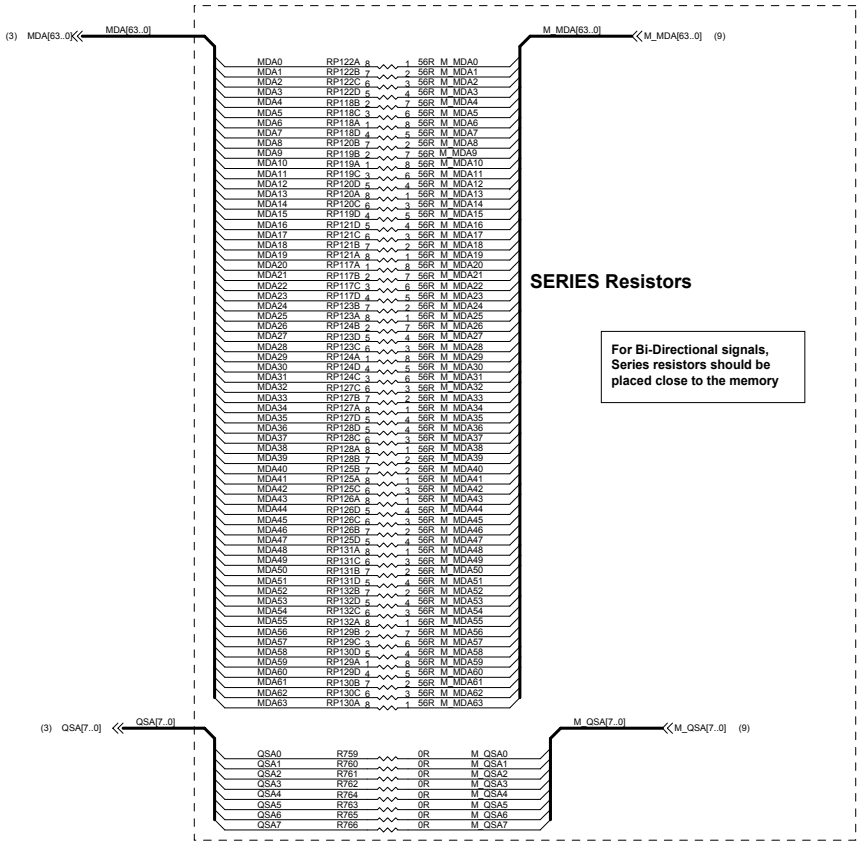

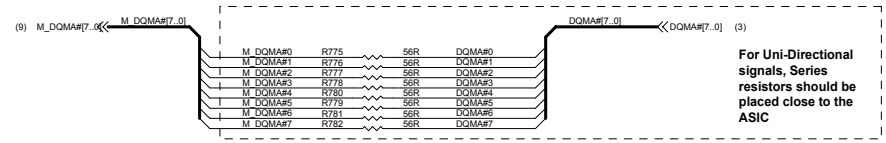

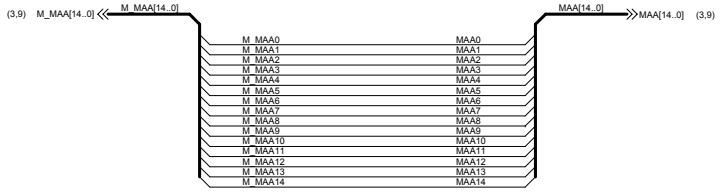

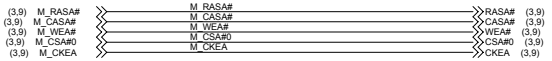

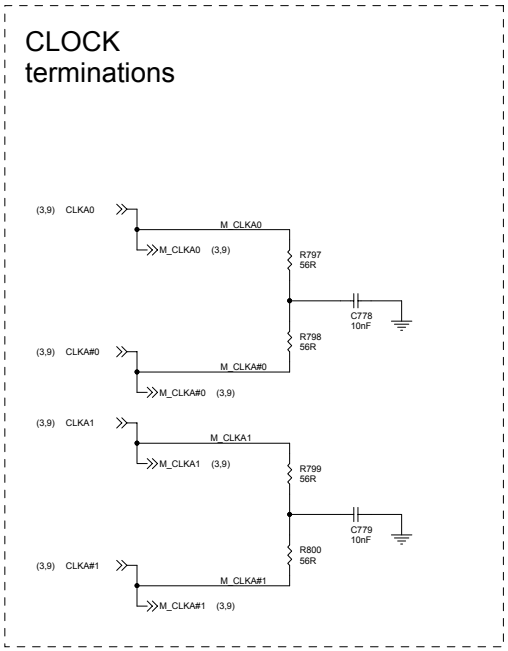

<variant_name>

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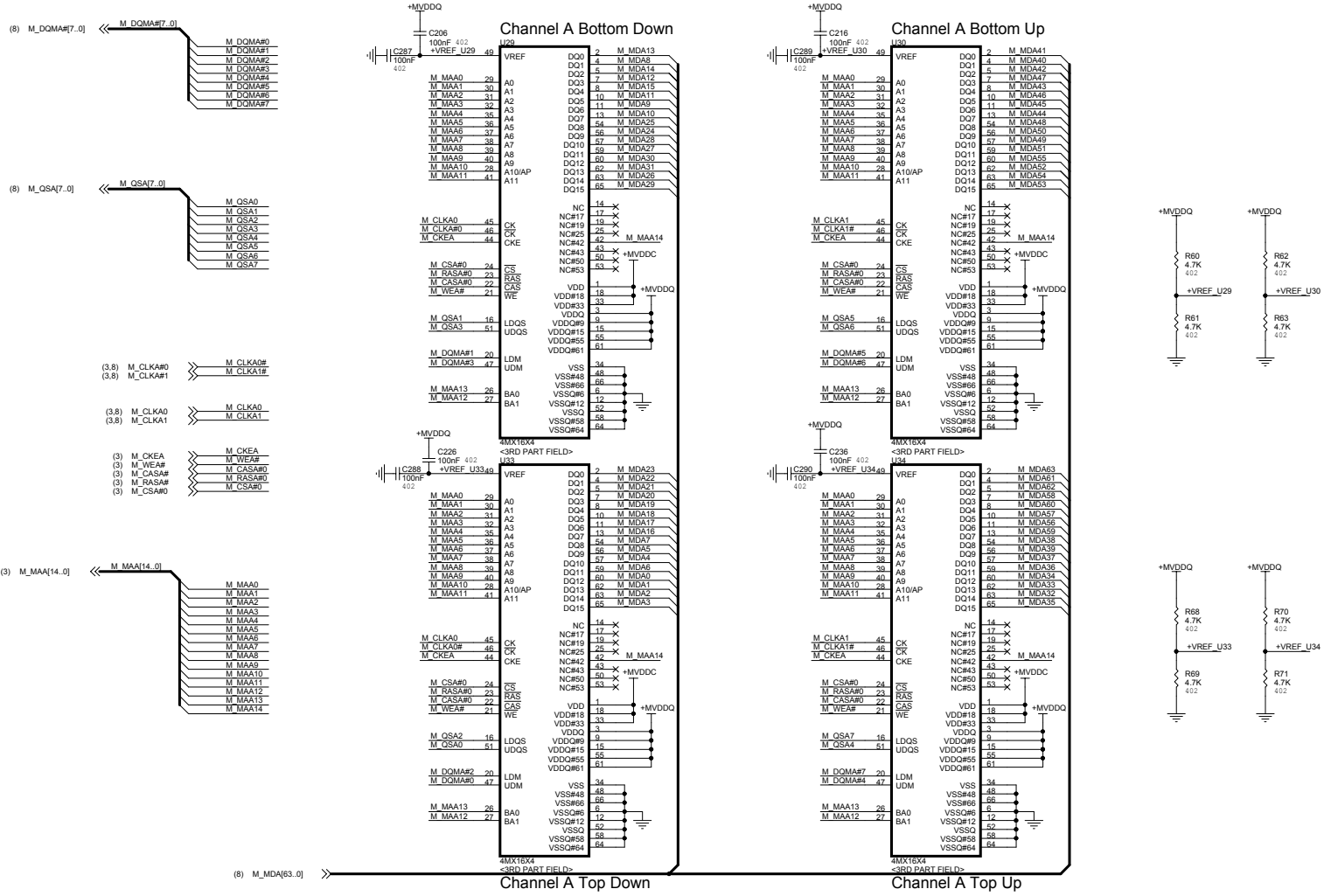
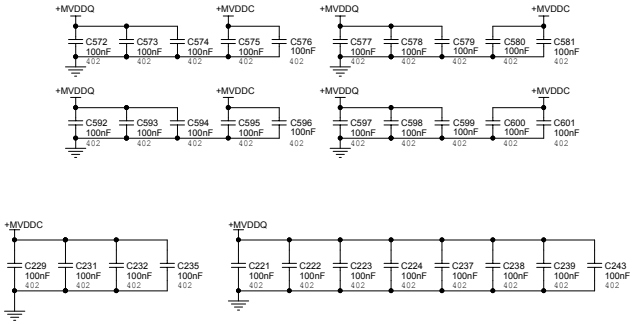


Put 1 1uF cap per power pin of memory



DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

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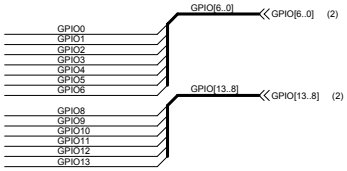
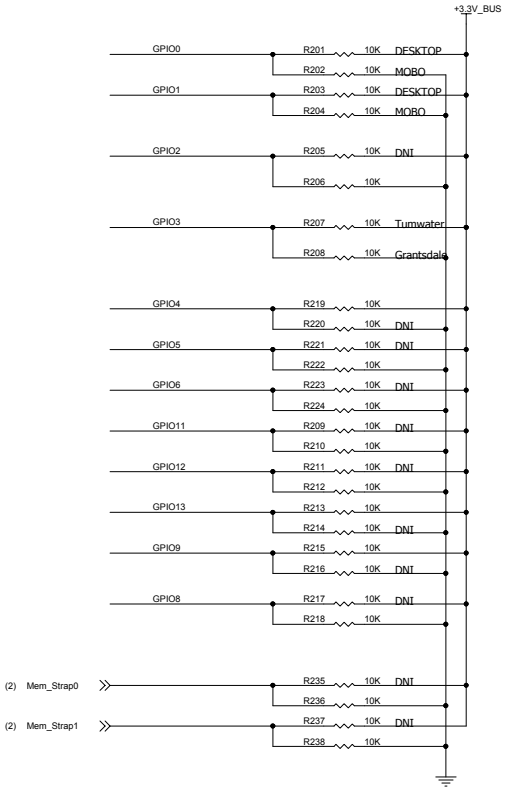
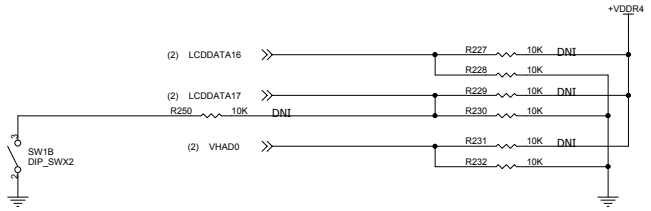
OPTION STRAPS



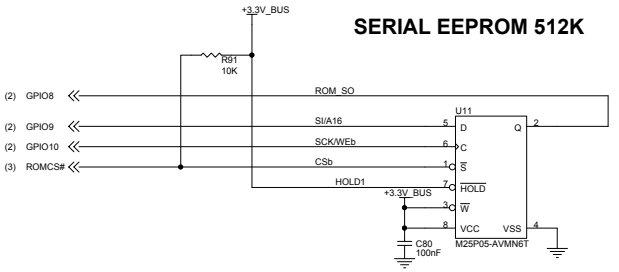




STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1



SERIAL EEPROM 512K

<Variant Name>

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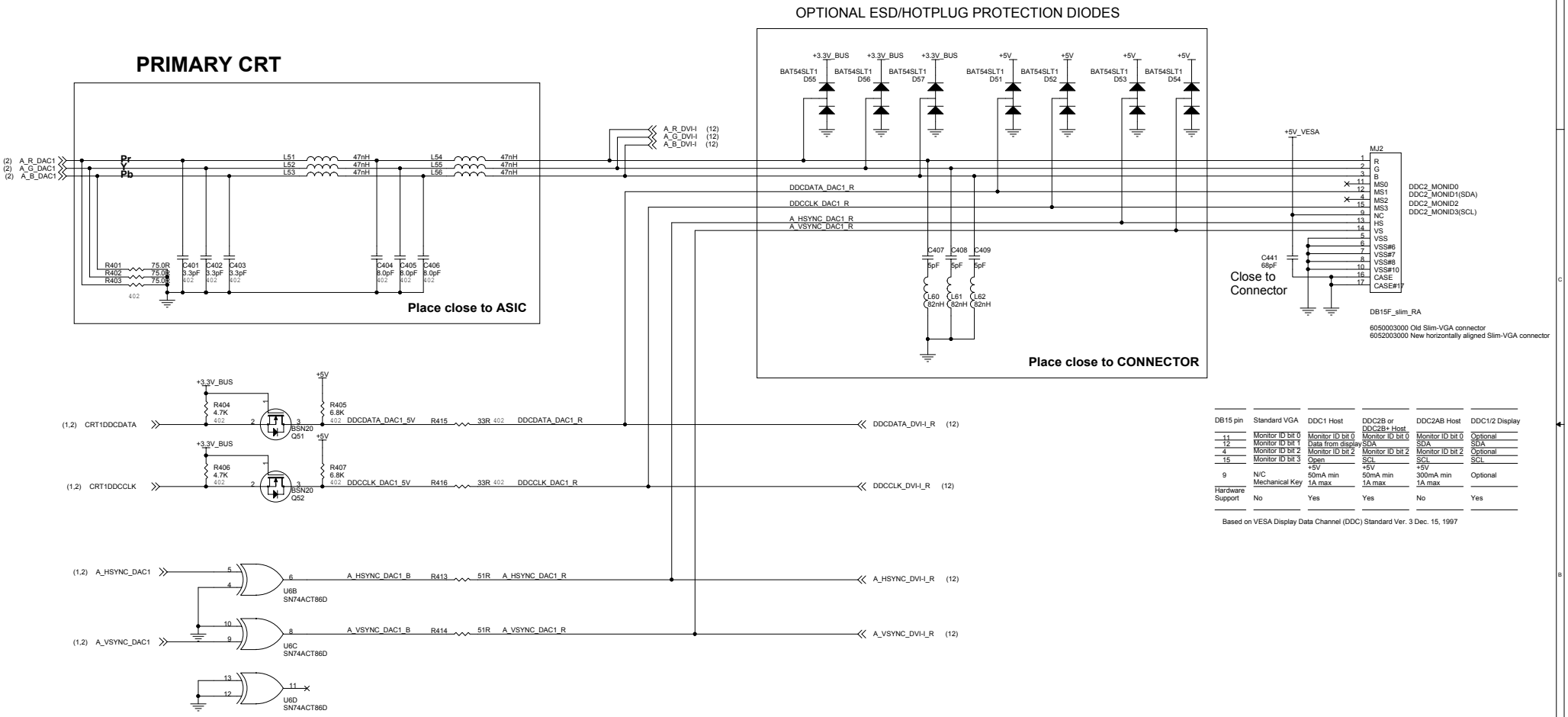
PRIMARY CRT



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

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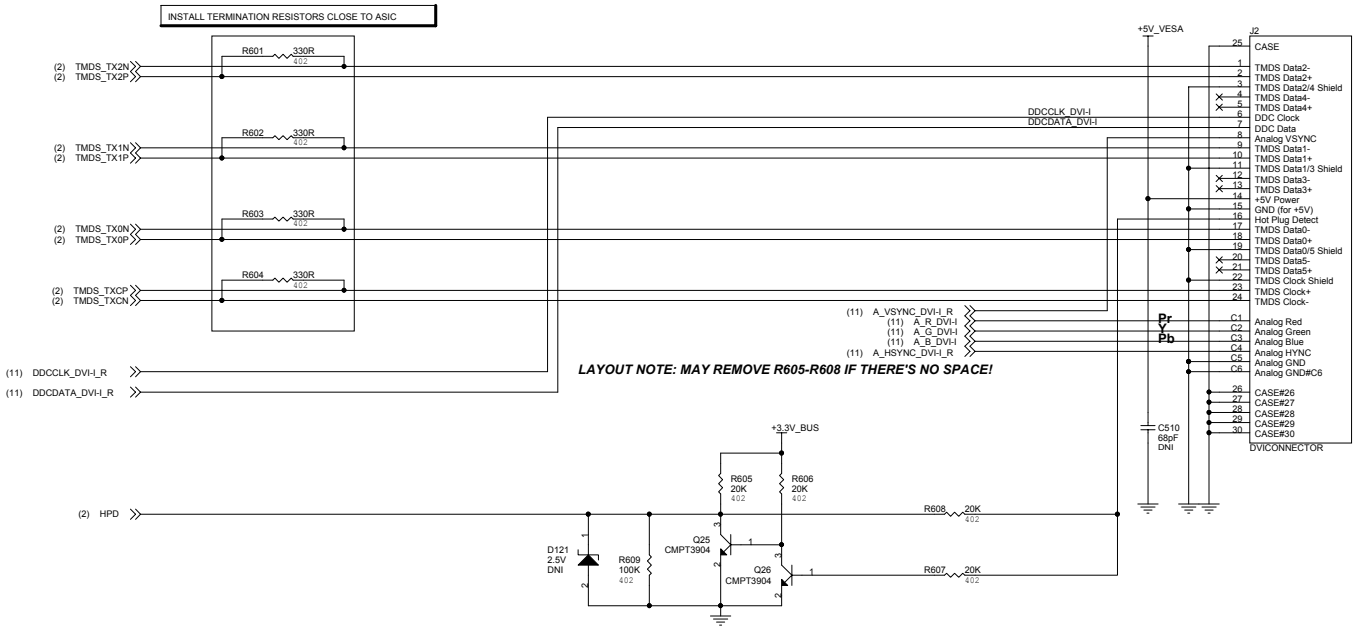
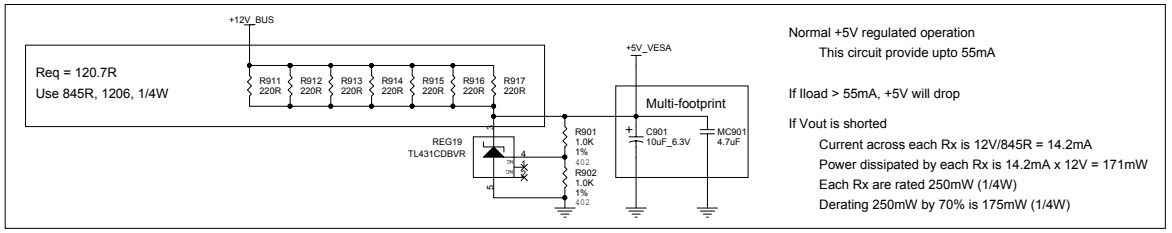
PRIMARY DVI-I CONNECTOR





Normal +5V regulated operation
This circuit provide upto 55mA

If Iload > 55mA, +5V will drop

If Vout is shorted
Current across each Rx is 12V/845R = 14.2mA
Power dissipated by each Rx is 14.2mA x 12V = 171mW
Each Rx are rated 250mW (1/4W)
Derating 250mW by 70% is 175mW (1/4W)

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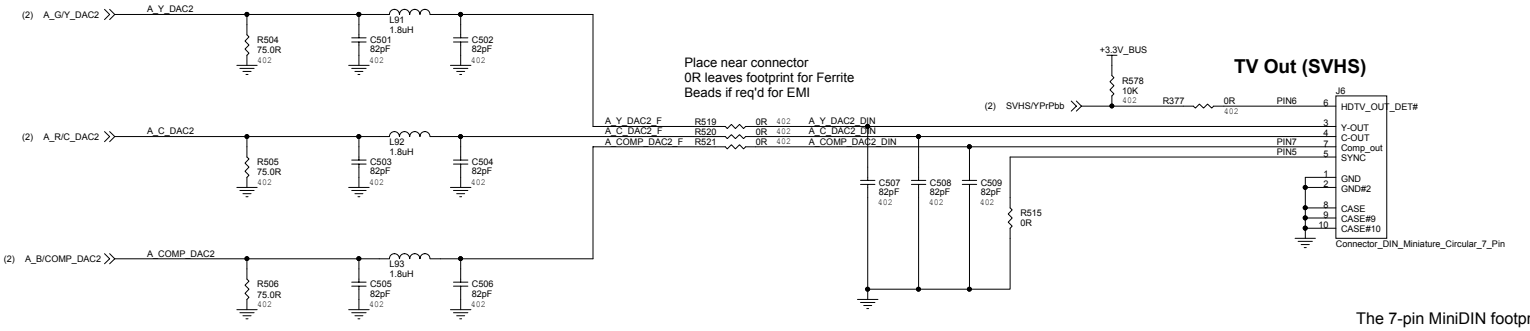
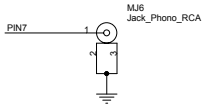
Place Resistors close to ASIC.



TV Out (SVHS)

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500
- 4-pin Svideo MiniDIN P/N 6070001000



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DVI/VGA SCREWS

ASSY1
SCREW
JACKSCREW

ASSY2
SCREW
JACKSCREW

Bracket Screws

ASSY3
SCREW
PAN_HEAD

MISC. BOARD PARTS

ASSY7
ANTISTATIC BAG
6_X_11

ASSY5
ATI LOGO LABEL
ATI_LOGO_LABEL

ASSY-PCB
ATI LOGO LABEL

ASSY8
BLANK LABEL

9050005900;9050005900;9050005900;9050005900

+12V_BUS

JU1

H101
heatsink
7120005800

H100
HEATSINK
7120005100

Spring push-pin

MH101
HEATSINK
7120002700

MH100
HEATSINK
7120008000

ITW push-pin

MT1
MT_Hole_0.136_in.

ATX Brackets

ASSY10
BRACKET
DVI ATX
NO TABS, DVI
80200321A0

ASSY11
BRACKET
DVI+MiniDIN ATX
TOP TAB (LP), DIN, DVI
8020033000

DNE
Slim-VGA ATX
6052003000 New horizontally aligned Slim-VGA connector

ASSY13
BRACKET
Slim-VGA+MiniDIN ATX
TOP TAB (LP), DIN, VGA
6052003000 New horizontally aligned Slim-VGA connector

LP Brackets

ASSY14
BRACKET
DVI LP
LP, NO TABS, DVI
8020032600

ASSY15
BRACKET
DVI+MiniDIN LP
LP, TOP TAB, DIN, DVI
8020032700

ASSY16
BRACKET
Slim-VGA LP
No Top Tab
LP, NO TABS, VGA
80200326A0
6052003000 New horizontally aligned Slim-VGA connector

ASSY17
BRACKET
Slim-VGA+MiniDIN LP
LP, TOP TAB, DIN, VGA
80200327A0
6052003000 New horizontally aligned Slim-VGA connector

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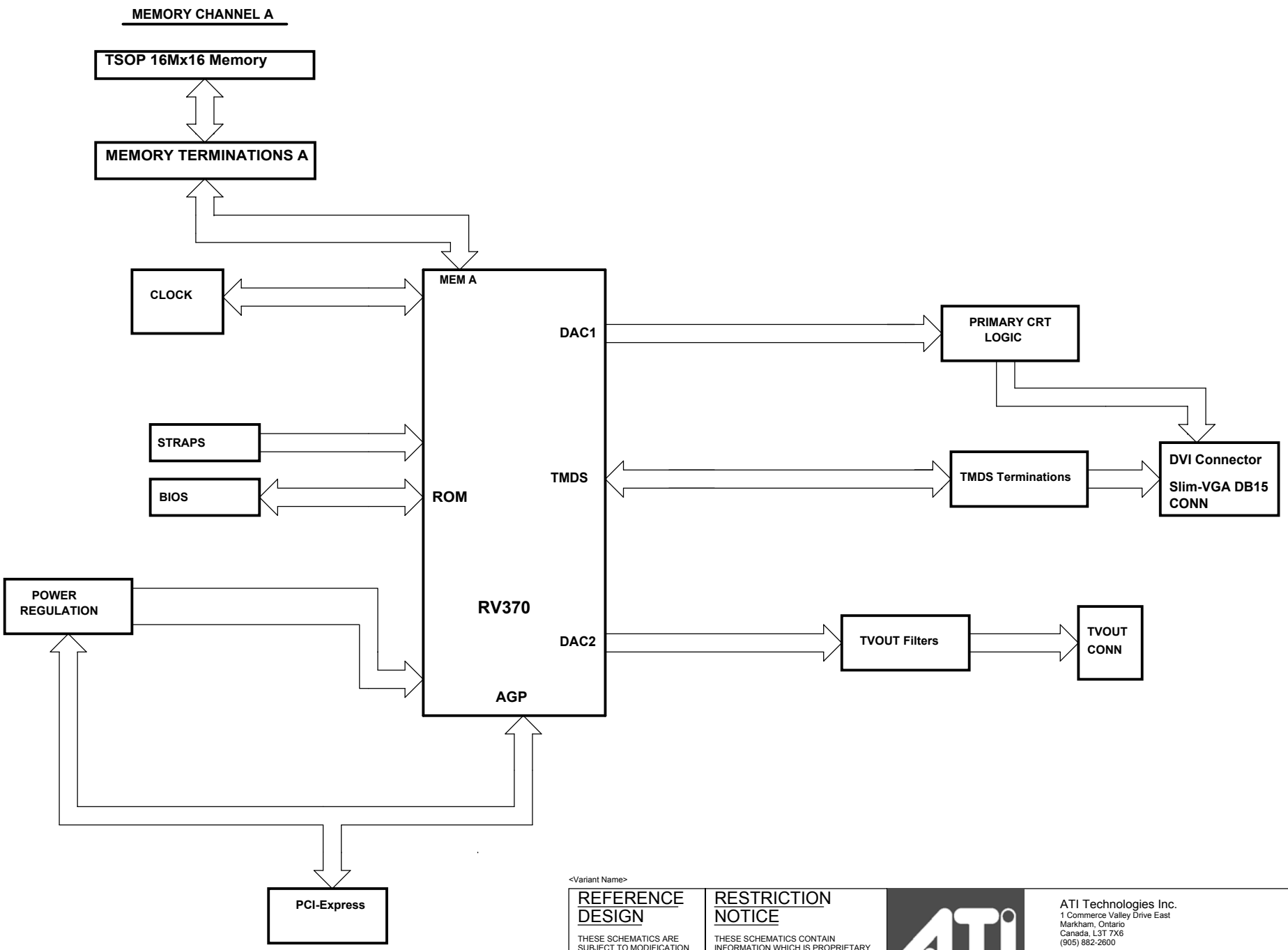

<Variant Name>

REFERENCE DESIGN

THESE SCHEMATICS ARE SUBJECT TO MODIFICATION AND DESIGN IMPROVEMENTS. PLEASE CONTACT ATI FIELD APPLICATION ENGINEERING BEFORE USING THE INFORMATION CONTAINED HEREIN.

RESTRICTION NOTICE

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