1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD
B	0003279770	PRODUCTION RELEASED	2014-09-29

MLB B - PVT

LAST_MODIFIED=Mon Sep 29 18:09:18 2014

RADIO_MLB SYNC VER 0.109.0
WIFI_DEV SYNC VER 0.68.0
ROTTERDAM SYNC VER 0.11.0

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	TABLE OF CONTENTS	N/A	N/A
2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A
3	4	BOM TABLES	N/A	N/A
4	5	SOC: MISC & ALIASES	N/A	N/A
5	6	SOC: MAIN	N/A	N/A
6	7	SOC: I/OS	N/A	N/A
7	8	SOC: NAND	N/A	N/A
8	9	SOC: MIPI, ISP	N/A	N/A
9	10	SOC: EDP, PCIE	N/A	N/A
10	11	SOC: DDR	N/A	N/A
11	12	SOC: IO POWER	N/A	N/A
12	13	SOC: SOC POWER AND GND	N/A	N/A
13	14	SOC: CPU, GPU, SRAM POWER	N/A	N/A
14	16	DDR: CHANNEL 0 AND 1	N/A	N/A
15	17	DDR: CHANNEL 2 AND 3	N/A	N/A
16	18	NAND	N/A	N/A
17	20	SENSOR: OSCAR	N/A	N/A
18	21	SENSOR: CARBON, PHOS+, MAGN	N/A	N/A
19	22	SENSOR: HALL EFFECT	N/A	N/A
20	27	CAMERA: CAM CONNS	N/A	N/A
21	28	CAMERA: CAM SUPPORT	N/A	N/A
22	30	AUDIO: L81 CODEC	N/A	N/A
23	31	AUDIO: HP/DMIC FLEX CONNS	N/A	N/A
24	32	AUDIO: SPEAKER AMPS	N/A	N/A
25	35	IO: TRISTAR	N/A	N/A
26	36	IO: FILTERS	N/A	N/A
27	37	IO: HOTBAR PADS	N/C	N/A
28	39	IO: BUTTON FLEX CONN	N/A	N/A
29	40	GRAPE: STINGER & CONN	N/A	N/A
30	41	GRAPE: CUMULUS	N/A	N/A
31	45	DISPLAY: CONNECTOR	N/A	N/A
32	46	DISPLAY: EDP SUPPORT	N/A	N/A
33	47	MESA: SUPPORT	N/A	N/A
34	48	ROTTERDAM	ROTTERDAM	05/13/2014
35	50	CELL: PROBE PTS & DEBUG CONN	RADIO	09/29/2014
36	51	CELL: BB PMU (1/2)	RADIO	09/29/2014
37	52	CELL: BB PMU (2/2)	RADIO	09/29/2014
38	53	CELL: BASEBAND (1/2)	RADIO	09/29/2014
39	54	CELL: BASEBAND (2/2)	RADIO	09/29/2014
40	55	CELL: BASEBAND (3/3)	RADIO	09/29/2014
41	56	CELL: RF TXCVR (1/3)	RADIO	09/29/2014
42	57	CELL: RF TXCVR (2/3)	RADIO	09/29/2014
43	58	CELL: RF TXCVR (3/3)	RADIO	09/29/2014
44	59	CELL: QFE DCDC	RADIO	09/29/2014
45	60	CELL: 2G PA	RADIO	09/29/2014
46	61	CELL: VLB PAD	RADIO	09/29/2014
47	62	CELL: LB PAD	RADIO	09/29/2014
48	63	CELL: MB PAD	RADIO	09/29/2014
49	64	CELL: HB PAD	RADIO	09/29/2014
50	65	CELL: ANTENNA SWITCH	RADIO	09/29/2014
51	66	CELL: HB SWITCH	RADIO	09/29/2014
52	67	CELL: RX DIV (1/2)	RADIO	09/29/2014
53	68	CELL: RX DIV (2/2)	RADIO	09/29/2014
54	69	CELL: GPS	RADIO	09/29/2014
55	70	CELL: ANT FEEDS & GPS (J82)	RADIO	09/29/2014
56	74	WIFI/BT: J82 ANT INTERFACE	WIFI	09/29/2014
57	75	WIFI/BT: WIFI/BT MODULE	WIFI	09/29/2014
58	78	SENSOR: HAMMERHEAD	N/A	N/A
59	79	CELL: SIM AND ANT SW FILT	N/A	N/A
60	81	PMU: ARABELA (1/3)	N/A	N/A
61	82	PMU: ARABELA (2/3)	N/A	N/A
62	83	PMU: ARABELA (3/3)	N/A	N/A
63	84	POWER: J82 SPECIFIC	N/A	N/A
64	86	POWER: EXTERNAL SWITCHES	N/A	N/A
65	88	PMU: CHARGER BUCK	N/A	N/A
66	89	POWER: BATTERY CONN	N/A	N/A
67	90	SOC: DEBUG	N/A	N/A
68	91	ALIASES: BB/WLAN/BT	N/A	N/A
69	93	TEST: TPS/HOLES/FIDUCUALS	N/A	N/A
70	95	TEST: EE TP/PP	N/A	N/A
71	96	TEST: CELL EE TP/PP	N/A	N/A
72	121	POWER: ALIASES	N/A	N/A
73	155	BB/WLAN VOLTAGE ATTRIBUTES	N/A	N/A

DRAWING

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-0301	1	SCH,MLB-B,J82	SCH1	CRITICAL	
820-3633	1	PCBF,MLB-B,J82	PCB1	CRITICAL	

CAPRI

Left side

- COMPASS — CSA 21 — SPI
- PHOSPHOROUS+ — CSA 21 — SPI
- GRYO — CSA 21 — SPI
- ACCEL — CSA 21 — SPI
- PROX SENSOR — CSA 78 — I2C
- TEMP SENSOR — CSA 78 — I2C
- HELIUM — CSA 78 — I2C
- GRAPE — CSA 41
  - CUMULUS
  - CUMULUS
- STINGER — CSA 40 — I2C
- DISPLAY/ TOUCH PANEL
  - BACKLIGHT
  - EDP
  - I2C MESA
  - SPI
- ALS (MIC) — I2C
- ALS (AJ) — I2C
- OSCAR — CSA 20
  - I2C
  - SPI (M)
  - I2C
  - UART
  - UART
  - BASEBAND
- PMU ARABELA — CSA 81-83
  - BMU
  - BATTERY
  - HDQ
  - I2S3
  - IRQ
  - DWI
  - I2C
  - GPIO
- HALL EFF 1 — CSA 22
- HALL EFF 2 — IO FLEX
- BUTTON FLEX — CSA 39

Right side

- REAR CAMERA — CSA 27 — ISP0, ISP0_I2C, MIPI0C
- FRONT CAMERA — CSA 27 — ISP1, ISP1_I2C, MIPI1C
- BT / WIFI/BT / WLAN / COEX — CSA — I2S4, UART3, PCIE1, UART2
  - MIMO
  - WIFI/BT ANT
  - WIFI/BT ANT
- CELLULAR/ GPS — NOT ON WIFI-ONLY CONFIG
  - COEX
  - UART
  - HSIC IPC — HSIC0, GPIO
  - UART — UART1
  - USB
  - PRIMARY CELLULAR ANT
  - DIVERSITY CELLULAR ANT
  - GPS ANT
  - SIM CARD
- TRISTAR — CSA 35
  - USB1
  - UART2
  - I2C — I2C0
  - USB0 — USB2.0
  - UART1 — UART0
  - UART0 — UART6
  - JTAG
  - DIG
- L81 AUDIO CODEC — CSA 30
  - SPI — SPI1
  - ASP — I2S0
  - XSP — I2S1
  - MBUS
  - HP
  - MIC1
  - MIC2
- AMP — CSA 33 — RIGHT SPEAKER — IO FLEX
- AMP — CSA 32 — LEFT SPEAKER — IO FLEX
- LPDDR3 — CSA 16 — DDR0, DDR1
- LPDDR3 — CSA 17 — DDR2, DDR3
- NAND FLASH — CSA 18 — FMI0, FMI1

Signals to/from CAPRI

SPI3, UART8, I2C2, SPI2, I2C1, LPDP, NC --, DWI1, UART5 (HDQ), DWI0, I2C0, GPIO, OSCAR, HSIC0, GPIO, UART1, I2C0, USB2.0, UART0, UART6, JTAG, SPI1, I2S0, I2S1

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-7118	1	RADIO FENCE X190	PD_FENCE_RADIO	CRITICAL	MLB_B
806-00001	1	AP FENCE X190	PD_FENCE_AP	CRITICAL	
806-6353	1	GRAPE FENCE X190	PD_FENCE_GRAPE	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-00067	1	EEEE FOR 639-5813 (MLB A 16GB)	EEEE_FQJ3	CRITICAL	EEEE_MLB_A_16GB
825-00067	1	EEEE FOR 639-5814 (MLB A 32GB)	EEEE_FQJ0	CRITICAL	EEEE_MLB_A_32GB
825-00067	1	EEEE FOR 639-5815 (MLB A 64GB)	EEEE_FQJ1	CRITICAL	EEEE_MLB_A_64GB
825-00067	1	EEEE FOR 639-5816 (MLB A 128GB)	EEEE_FQJ2	CRITICAL	EEEE_MLB_A_128GB
825-00067	1	EEEE FOR 639-4747 (MLB B 16GB)	EEEE_FH54	CRITICAL	EEEE_MLB_B_16GB
825-00067	1	EEEE FOR 639-5809 (MLB B 32GB)	EEEE_FQHY	CRITICAL	EEEE_MLB_B_32GB
825-00067	1	EEEE FOR 639-5810 (MLB B 64GB)	EEEE_FQHW	CRITICAL	EEEE_MLB_B_64GB
825-00067	1	EEEE FOR 639-5811 (MLB B 128GB)	EEEE_FQHV	CRITICAL	EEEE_MLB_B_128GB

CKPLUS WAIVE TABLE

CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00016	1	IC,CAPRI,A1,PROD,ASE	U0600	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S00021	343S00016		U0600	IC,CAPRI,A1,PROD,SCK

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0675	1	IC,PMU,ARABELA,D2207A0,TOP-AC,FCBGA380	U8100	CRITICAL	

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0803	2	IC,CAPRI,DRAM,10X10MM,FBGA261	U1600,U1700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0804	333S0803		U1600,U1700	ELPIDA DRAM
333S00014	333S0803		U1600,U1700	SAMSUNG DRAM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0972	1	TOSHIBA 16GB MLC 1YNM PPN1.5	U1800	CRITICAL	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S1035	335S0972	16GB_PROD	U1800	HYNIX 16GB MLC 1YNM PPN1.5

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00011	1	SANDISK 64GB TLC 1YNM PPN1.5	U1800	CRITICAL	64GB_PROD

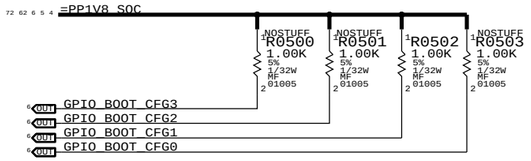
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00017	335S00011	64GB_PROD	U1800	TOSHIBA 64GB TLC 1YNM PPN

128GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00012	1	SANDISK 128GB TLC 1YNM PPN1.5	U1800	CRITICAL	128GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00018	335S00012	128GB_PROD	U1800	TOSHIBA 128GB TLC 1YNM PPN

BOOT CONFIG ID

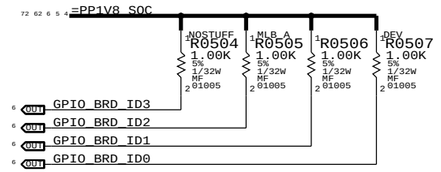


BOOT_CFG[3:0]	MODE
0000	SPI
0001	SPI W/TEST
CURRENT SETTING ---> 0010	NAND
0011	NAND W/TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID



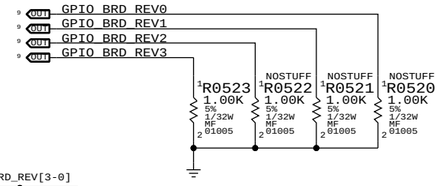
BRD_ID[3-0]	
0000	RESERVED
0001	RESERVED
0010	MLB_B AP
0011	MLB_B DEV
0100	RESERVED
0101	RESERVED
0110	MLB_A AP
0111	MLB_A DEV
1000	UNUSED
1001	UNUSED
1010	UNUSED
1011	UNUSED
1100	RESERVED
1101	RESERVED

RDAR://PROBLEM/15529479

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

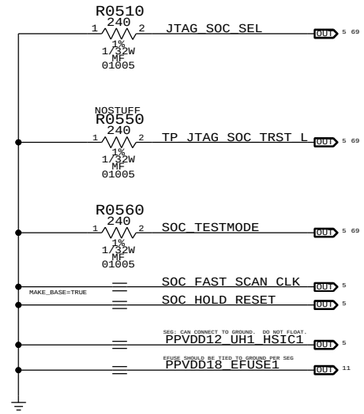
BOARD REVISION

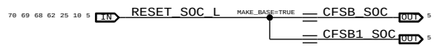


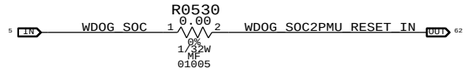
BRD_REV[3-0]	
0000	RESERVED
0001	RESERVED
0010	PROTO 1 (BRING UP)
0011	PROTO 1 (LOCAL/CHINA)
0100	PROTO 2
0101	PRE-EVT
0110	EVT
CURRENT SETTING ---> 0111	DVT & PVT
1000	UNUSED

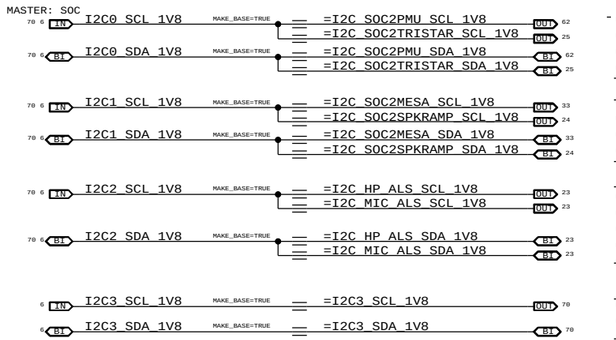
S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ









TO:
ARIADELA ADDR: 0B0111100X
TRISTAR ADDR: 0B0011010X

TO:
MESA EEPROM (MEM) ADDR: 0B1010000X
MESA EEPROM (ID) ADDR: 0B1011000X
SPEAKER AMP LEFT ADDR: 0B0110001X
SPEAKER AMP RIGHT ADDR: 0B0110100X

TO:
ALS(MIC) ADDR: 0B0101001X
ALS(HP) ADDR: 0B1001001X

TO:
PROBE POINTS

ON IN HIBERNATE
VDD1, VDD2, VDDIOD_DDRXCA (VDDCA), VDD12_CKE_DDR0, VDD12_CKE_DDR1

=PP1V2_HSIC_SOC
C0610 0.22UF 20% 6.3V X5R 01005-1
C0611 0.22UF 20% 6.3V X5R 01005-1
C0612 0.22UF 20% 6.3V X5R 01005-1
C0615 0.01UF 10% 6.3V X5R 01005
C0620 100PF 5% 16V NP0-C0G 01005

PPVDD12_UH1_HSIC1

=PP0V95_USB_SOC
C0630 0.01UF 10% 6.3V X5R 01005
C0631 0.22UF 20% 6.3V X5R 01005-1
C0632 100PF 5% 16V NP0-C0G 01005

=PP3V3_USB_SOC
C0640 0.01UF 10% 6.3V X5R 01005
C0645 0.22UF 20% 6.3V X5R 01005-1
C0641 100PF 5% 16V NP0-C0G 01005

H24 AM43 SEG: CAN CONNECT TO GROUND. DO NOT FLOAT.
CKPLUS_WAIVE=PWRTERM2GND

F23 J25 H25

VDD12_UH0_HSIC0
VDD12_UH1_HSIC1
13MA EACH

VDDH_USB 20MA
VDD095_USB 5MA
VDD33_USB

U0600
TMKP88A0-N
FCBGA
SYM 4 OF 15
OMIT_TABLE

HSIC_BB_DATA D25 UH1_HSIC0_DATA
HSIC_BB_STB E25 UH1_HSIC0_STB
NC_HSIC1_DATA NO_TEST=TRUE AV38 UH2_HSIC1_DATA
NC_HSIC1_STB NO_TEST=TRUE AU38 UH2_HSIC1_STB

=PP1V8_SOC
R0610 100K 5% 1/32W MF 01005
R0611 100K 5% 1/32W MF 01005
R0612 100K 5% 1/32W MF 01005

JTAG_SOC_SEL U37 JTAG_SEL
NC_JTAG_SOC_TRTCK NO_TEST=TRUE R36 JTAG_TRTCK
TP_JTAG_SOC_TRST_L U40 JTAG_TRST*
TP_JTAG_SOC_TDO U36 JTAG_TDO
JTAG_SOC_TDI T41 JTAG_TDI
JTAG_SOC_TMS U38 JTAG_TMS
JTAG_SOC_TCK U41 JTAG_TCK

=PP1V8_SOC
R0634 10K 5% 1/32W MF 01005

RESET_SOC_L AR41 RESET*
C0660 0.01UF 10% 16V X5R-CERM 0201

POWER-ON RESET FAIL SAFE I/O
CFSB_SOC AR39 CFSB
CFSB1_SOC AN26 CFSB1
SOC_HOLD_RESET AN38 HOLD_RESET
TP0600 TP-P55
SOC_TST_CLKOUT AM40 TST_CLKOUT
SOC_FAST_SCAN_CLK AR40 FAST_SCAN_CLK
SOC_TESTMODE AT39 TESTMODE

ANALOGMUXOUT G35 TP_ANALOGMUXOUT
USB_DP B26 USB_SOC_P
USB_DM C26 USB_SOC_N

USB_VBUS HAS 70K INPUT IMPEDANCE
VIN 5.6V MAX
USB_VBUS F22 USB_VBUS_DETECT_R
R0630 68.1K 1% 1/32W MF 01005
USB_VBUS_DETECT

USB_ID F25 NC_USB_ID NO_TEST=TRUE

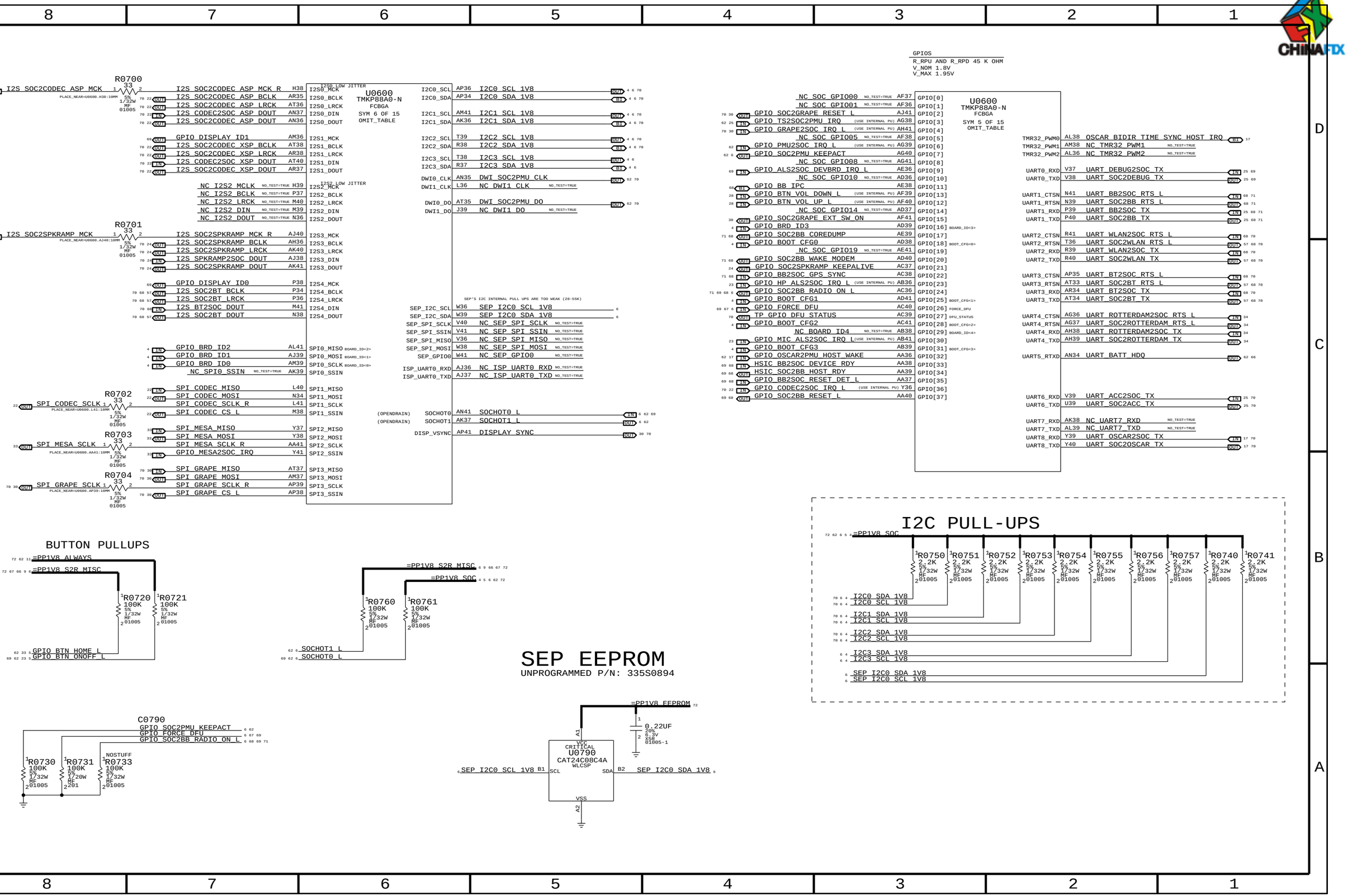
USB_REXT F24 USB_REXT0
R0660 200 1% 1/32W MF 01005
PLACE_NEAR=U0600.F24:5MM

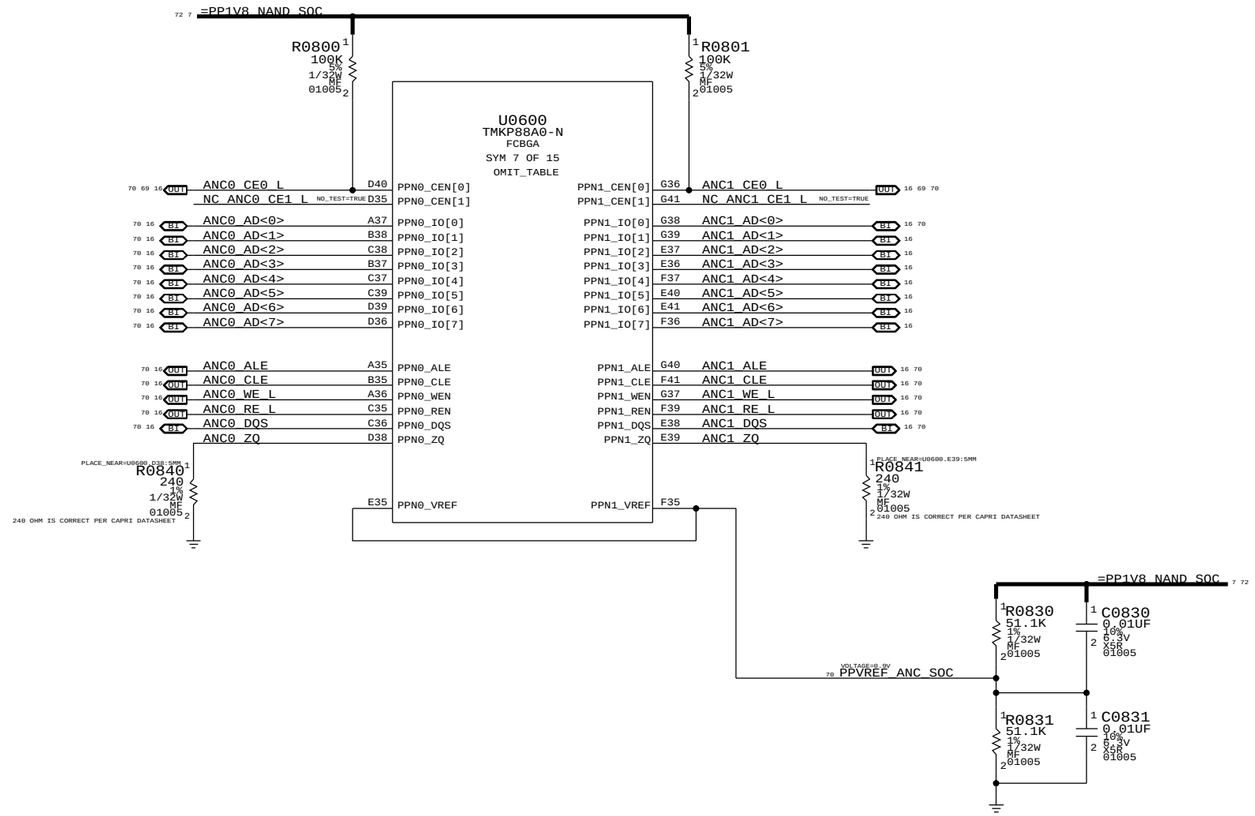
WDOG AN39 WDOG_SOC

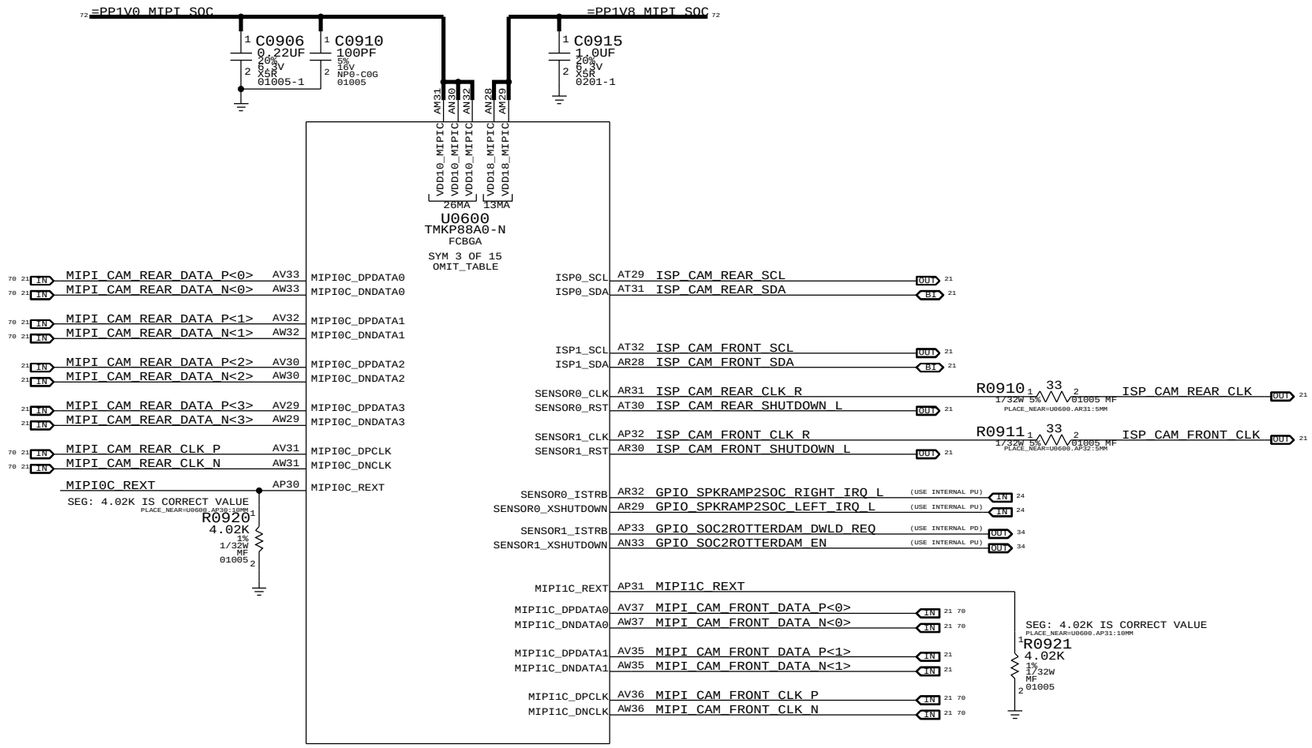
XI0 H41 XTAL_SOC_24M_I
XO0 H40 XTAL_SOC_24M_O

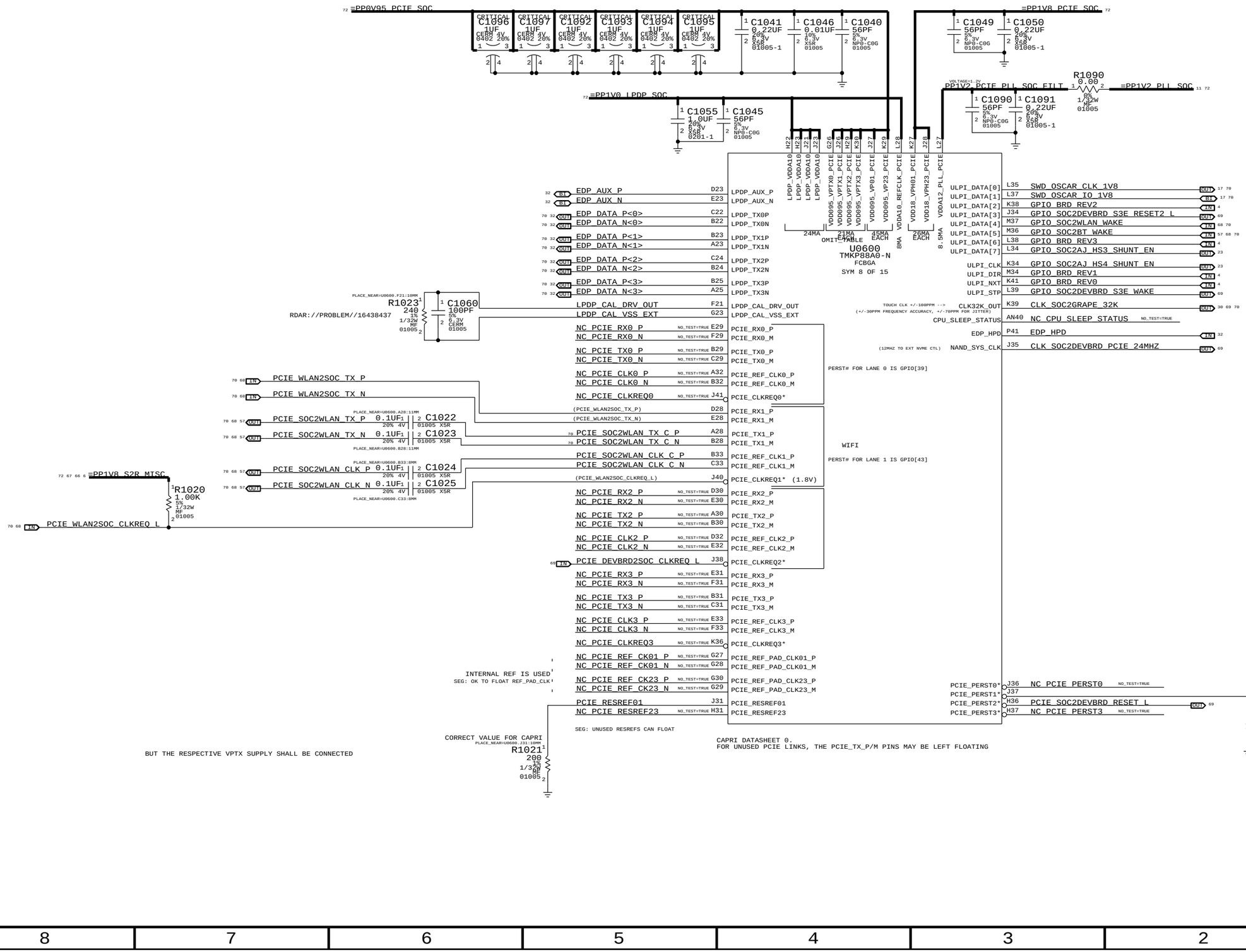
ALWAYS-ON 1.8V
(REQUEST_DFU1_L) HOLD_KEY* AP27 GPIO_BTN_ONOFF_L
(REQUEST_DFU2_L) MENU_KEY* AM26 GPIO_BTN_HOME_L

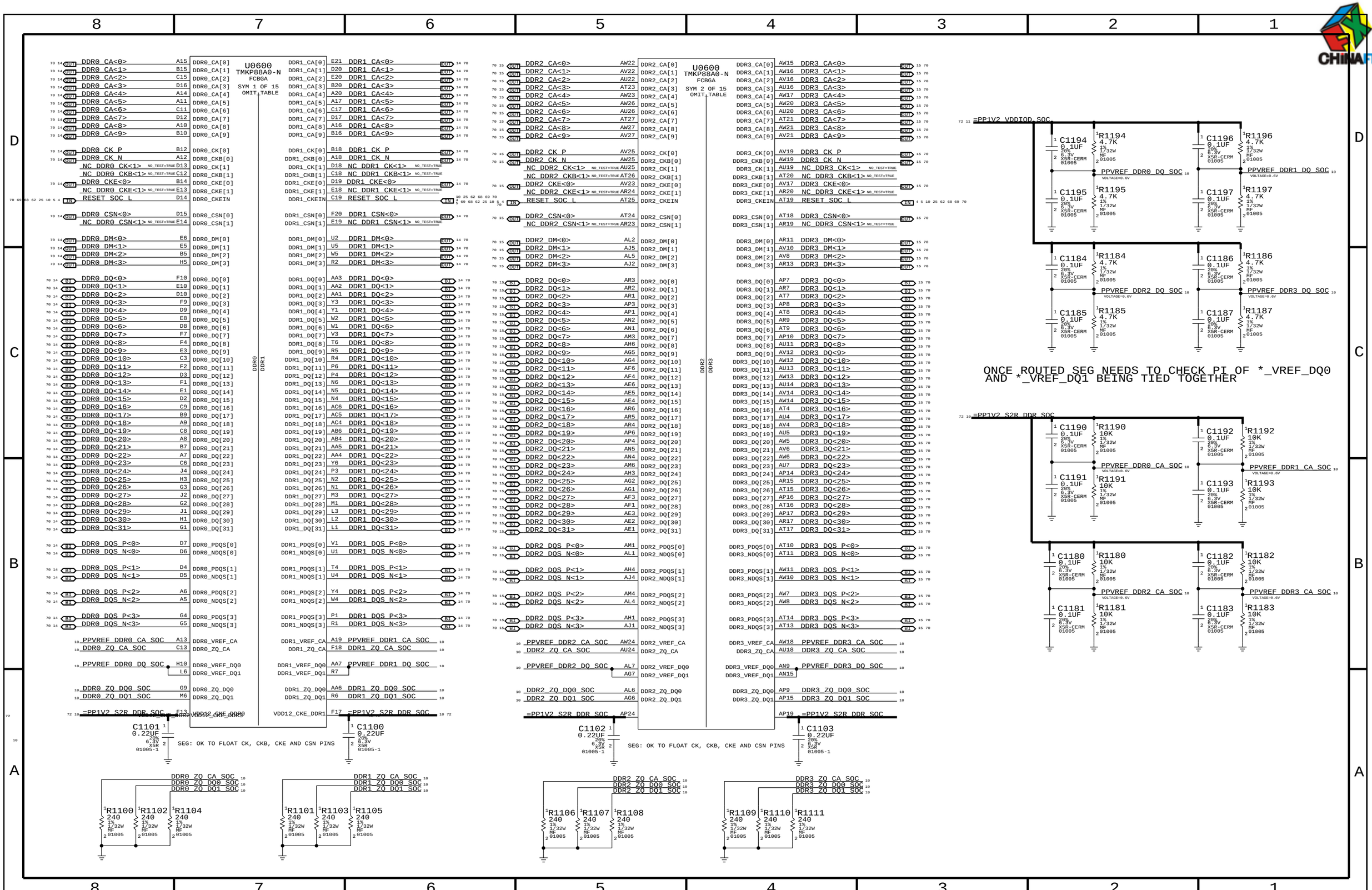
R0640 1.00M 1% 1/32W MF 01005
R0641 1.33K 1% 1/32W MF 01005
CRITICAL
Y0600 1.60X1.20MM-SM
24.000MHZ-30PPM-9.5PF-60OHM
SOC_24M_O
CRITICAL
C0650 12PF 5% 16V CERM 01005
CRITICAL
C0651 12PF 5% 16V CERM 01005

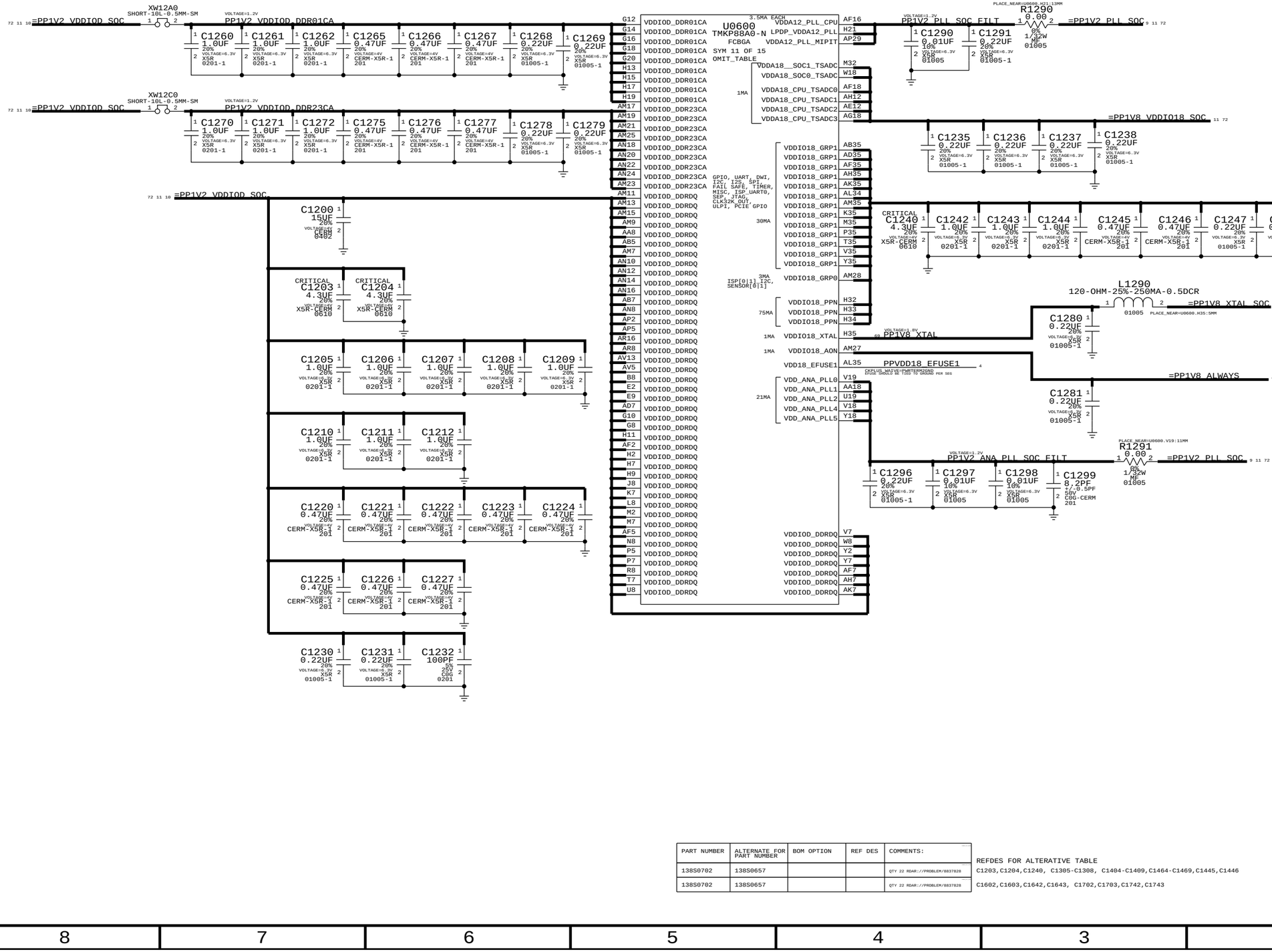

R0700
33
I2S_SOC2CODEC_ASP_MCK
I2S_SOC2CODEC_ASP_MCK_R
I2S_SOC2CODEC_ASP_BCLK
I2S_SOC2CODEC_ASP_LRCK
I2S_CODEC2SOC_ASP_DOUT
I2S_SOC2CODEC_ASP_DOUT
R0701
33
I2S_SOC2SPKRAMP_MCK
I2S_SOC2SPKRAMP_MCK_R
I2S_SOC2SPKRAMP_BCLK
I2S_SOC2SPKRAMP_LRCK
I2S_SPKRAMP2SOC_DOUT
I2S_SOC2SPKRAMP_DOUT
R0702
33
SPI_CODEC_SCLK
R0703
33
SPI_MESA_SCLK
R0704
33
SPI_GRAPE_SCLK
U0600
TMKP88A0-N
FCBGA
SYM 6 OF 15
OMIT_TABLE
I2S0_MCK
I2S0_BCLK
I2S0_LRCK
I2S0_DIN
I2S0_DOUT
I2S1_MCK
I2S1_BCLK
I2S1_LRCK
I2S1_DIN
I2S1_DOUT
I2S2_MCK
I2S2_BCLK
I2S2_LRCK
I2S2_DIN
I2S2_DOUT
I2S3_MCK
I2S3_BCLK
I2S3_LRCK
I2S3_DIN
I2S3_DOUT
I2S4_MCK
I2S4_BCLK
I2S4_LRCK
I2S4_DIN
I2S4_DOUT
SPI0_MISO
SPI0_MOSI
SPI0_SCLK
SPI0_SSIN
SPI1_MISO
SPI1_MOSI
SPI1_SCLK
SPI1_SSIN
SPI2_MISO
SPI2_MOSI
SPI2_SCLK
SPI2_SSIN
SPI3_MISO
SPI3_MOSI
SPI3_SCLK
SPI3_SSIN
I2C0_SCL
I2C0_SDA
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA
I2C3_SCL
I2C3_SDA
DWI0_CLK
DWI1_CLK
DWI0_DO
DWI1_DO
SEP_I2C_SCL
SEP_I2C_SDA
SEP_SPI_SCLK
SEP_SPI_SSIN
SEP_SPI_MISO
SEP_SPI_MOSI
SEP_GPIO0
ISP_UART0_RXD
ISP_UART0_TXD
SOCHOT0
SOCHOT1
DISP_VSYNC
GPIOS
R_RPU AND R_RPD 45 K OHM
V_NOM 1.8V
V_MAX 1.95V
U0600
TMKP88A0-N
FCBGA
SYM 5 OF 15
OMIT_TABLE
GPIO[0]
GPIO[1]
GPIO[2]
GPIO[3]
GPIO[4]
GPIO[5]
GPIO[6]
GPIO[7]
GPIO[8]
GPIO[9]
GPIO[10]
GPIO[11]
GPIO[12]
GPIO[13]
GPIO[14]
GPIO[15]
GPIO[16]
GPIO[17]
GPIO[18]
GPIO[19]
GPIO[20]
GPIO[21]
GPIO[22]
GPIO[23]
GPIO[24]
GPIO[25]
GPIO[26]
GPIO[27]
GPIO[28]
GPIO[29]
GPIO[30]
GPIO[31]
GPIO[32]
GPIO[33]
GPIO[34]
GPIO[35]
GPIO[36]
GPIO[37]
NC_SOC_GPIO00
NC_SOC_GPIO01
GPIO_SOC2GRAPE_RESET_L
GPIO_TS2SOC2PMU_IRQ
GPIO_GRAPE2SOC_IRQ_L
NC_SOC_GPIO05
GPIO_PMU2SOC_IRQ_L
GPIO_SOC2PMU_KEEPACT
NC_SOC_GPIO08
GPIO_ALS2SOC_DEVBRD_IRQ_L
NC_SOC_GPIO10
GPIO_BB_IPC
GPIO_BTN_VOL_DOWN_L
GPIO_BTN_VOL_UP_L
NC_SOC_GPIO14
GPIO_SOC2GRAPE_EXT_SW_ON
GPIO_BRD_ID3
GPIO_SOC2BB_COREDUMP
GPIO_BOOT_CFG0
NC_SOC_GPIO19
GPIO_SOC2BB_WAKE_MODEM
GPIO_SOC2SPKRAMP_KEEPALIVE
GPIO_BB2SOC_GPS_SYNC
GPIO_HP_ALS2SOC_IRQ_L
GPIO_SOC2BB_RADIO_ON_L
GPIO_BOOT_CFG1
GPIO_FORCE_DFU
TP_GPIO_DFU_STATUS
GPIO_BOOT_CFG2
NC_BOARD_ID4
GPIO_MIC_ALS2SOC_IRQ_L
GPIO_BOOT_CFG3
GPIO_OSCAR2PMU_HOST_WAKE
HSIC_BB2SOC_DEVICE_RDY
HSIC_SOC2BB_HOST_RDY
GPIO_BB2SOC_RESET_DET_L
GPIO_CODEC2SOC_IRQ_L
GPIO_SOC2BB_RESET_L
TMR32_PWM0
TMR32_PWM1
TMR32_PWM2
UART0_RXD
UART0_TXD
UART1_CTSN
UART1_RTSN
UART1_RXD
UART1_TXD
UART2_CTSN
UART2_RTSN
UART2_RXD
UART2_TXD
UART3_CTSN
UART3_RTSN
UART3_RXD
UART3_TXD
UART4_CTSN
UART4_RTSN
UART4_RXD
UART4_TXD
UART5_RTXD
UART6_RXD
UART6_TXD
UART7_RXD
UART7_TXD
UART8_RXD
UART8_TXD
OSCAR_BIDIR_TIME_SYNC_HOST_IRQ
NC_TMR32_PWM1
NC_TMR32_PWM2
UART_DEBUG2SOC_TX
UART_SOC2DEBUG_TX
UART_BB2SOC_RTS_L
UART_SOC2BB_RTS_L
UART_BB2SOC_TX
UART_SOC2BB_TX
UART_WLAN2SOC_RTS_L
UART_SOC2WLAN_RTS_L
UART_WLAN2SOC_TX
UART_SOC2WLAN_TX
UART_BT2SOC_RTS_L
UART_SOC2BT_RTS_L
UART_BT2SOC_TX
UART_SOC2BT_TX
UART_ROTTERDAM2SOC_RTS_L
UART_SOC2ROTTERDAM_RTS_L
UART_ROTTERDAM2SOC_TX
UART_SOC2ROTTERDAM_TX
UART_BATT_HDQ
UART_ACC2SOC_TX
UART_SOC2ACC_TX
NC_UART7_RXD
NC_UART7_TXD
UART_OSCAR2SOC_TX
UART_SOC2OSCAR_TX
BUTTON PULLUPS
=PP1V8_ALWAYS
=PP1V8_S2R_MISC
R0720
100K
R0721
100K
GPIO_BTN_HOME_L
GPIO_BTN_ONOFF_L
=PP1V8_S2R_MISC
=PP1V8_SOC
R0760
100K
R0761
100K
SOCHOT1_L
SOCHOT0_L
I2C PULL-UPS
=PP1V8_SOC
R0750
2.2K
R0751
2.2K
R0752
2.2K
R0753
2.2K
R0754
2.2K
R0755
2.2K
R0756
2.2K
R0757
2.2K
R0740
2.2K
R0741
2.2K
I2C0_SDA_1V8
I2C0_SCL_1V8
I2C1_SDA_1V8
I2C1_SCL_1V8
I2C2_SDA_1V8
I2C2_SCL_1V8
I2C3_SDA_1V8
I2C3_SCL_1V8
SEP_I2C0_SDA_1V8
SEP_I2C0_SCL_1V8
SEP EEPROM
UNPROGRAMMED P/N: 335S0894
C0790
GPIO_SOC2PMU_KEEPACT
GPIO_FORCE_DFU
GPIO_SOC2BB_RADIO_ON_L
R0730
100K
R0731
100K
R0733
100K
NOSTUFF
=PP1V8_EEPROM
0.22UF
U0790
CAT24C08C4A
WLCSP
VCC
CRITICAL
SCL
SDA
VSS
SEP_I2C0_SCL_1V8
SEP_I2C0_SDA_1V8


=PP1V8_NAND_SOC
R0800
100K
1%
1/32W
MF
01005
R0801
100K
1%
1/32W
MF
01005
U0600
TMKP88A0-N
FCBGA
SYM 7 OF 15
OMIT_TABLE
ANC0_CE0_L
NC_ANC0_CE1_L
NO_TEST=TRUE
ANC0_AD<0>
ANC0_AD<1>
ANC0_AD<2>
ANC0_AD<3>
ANC0_AD<4>
ANC0_AD<5>
ANC0_AD<6>
ANC0_AD<7>
ANC0_ALE
ANC0_CLE
ANC0_WE_L
ANC0_RE_L
ANC0_DQS
ANC0_ZQ
PPN0_CEN[0]
PPN0_CEN[1]
PPN0_IO[0]
PPN0_IO[1]
PPN0_IO[2]
PPN0_IO[3]
PPN0_IO[4]
PPN0_IO[5]
PPN0_IO[6]
PPN0_IO[7]
PPN0_ALE
PPN0_CLE
PPN0_WEN
PPN0_REN
PPN0_DQS
PPN0_ZQ
PPN0_VREF
PPN1_CEN[0]
PPN1_CEN[1]
PPN1_IO[0]
PPN1_IO[1]
PPN1_IO[2]
PPN1_IO[3]
PPN1_IO[4]
PPN1_IO[5]
PPN1_IO[6]
PPN1_IO[7]
PPN1_ALE
PPN1_CLE
PPN1_WEN
PPN1_REN
PPN1_DQS
PPN1_ZQ
PPN1_VREF
ANC1_CE0_L
NC_ANC1_CE1_L
NO_TEST=TRUE
ANC1_AD<0>
ANC1_AD<1>
ANC1_AD<2>
ANC1_AD<3>
ANC1_AD<4>
ANC1_AD<5>
ANC1_AD<6>
ANC1_AD<7>
ANC1_ALE
ANC1_CLE
ANC1_WE_L
ANC1_RE_L
ANC1_DQS
ANC1_ZQ
PLACE_NEAR=U0600.D38:5MM
R0840
240
1%
1/32W
MF
01005
240 OHM IS CORRECT PER CAPRI DATASHEET
PLACE_NEAR=U0600.E39:5MM
R0841
240
1%
1/32W
MF
01005
240 OHM IS CORRECT PER CAPRI DATASHEET
=PP1V8_NAND_SOC
R0830
51.1K
1%
1/32W
MF
01005
C0830
0.01UF
10%
6.3V
X5R
01005
VOLTAGE=0.8V
PPVREF_ANC_SOC
R0831
51.1K
1%
1/32W
MF
01005
C0831
0.01UF
10%
6.3V
X5R
01005


=PP1V0_MIPI_SOC
C0906
0.22UF
20%
6.3V
X5R
01005-1
C0910
100PF
5%
16V
NP0-C0G
01005
=PP1V8_MIPI_SOC
C0915
1.0UF
20%
6.3V
X5R
0201-1
AM31 VDD10_MIPIC
AN30 VDD10_MIPIC
AN32 VDD10_MIPIC
26MA
AN28 VDD18_MIPIC
AW28 VDD18_MIPIC
13MA
U0600
TMKP88A0-N
FCBGA
SYM 3 OF 15
OMIT_TABLE
MIPI_CAM_REAR_DATA_P<0> AV33 MIPI0C_DPDATA0
MIPI_CAM_REAR_DATA_N<0> AW33 MIPI0C_DNDATA0
MIPI_CAM_REAR_DATA_P<1> AV32 MIPI0C_DPDATA1
MIPI_CAM_REAR_DATA_N<1> AW32 MIPI0C_DNDATA1
MIPI_CAM_REAR_DATA_P<2> AV30 MIPI0C_DPDATA2
MIPI_CAM_REAR_DATA_N<2> AW30 MIPI0C_DNDATA2
MIPI_CAM_REAR_DATA_P<3> AV29 MIPI0C_DPDATA3
MIPI_CAM_REAR_DATA_N<3> AW29 MIPI0C_DNDATA3
MIPI_CAM_REAR_CLK_P AV31 MIPI0C_DPCLK
MIPI_CAM_REAR_CLK_N AW31 MIPI0C_DNCLK
MIPI0C_REXT AP30 MIPI0C_REXT
SEG: 4.02K IS CORRECT VALUE
PLACE_NEAR=U0600.AP30:10MM
R0920
4.02K
1%
1/32W
MF
01005
ISP0_SCL AT29 ISP_CAM_REAR_SCL
ISP0_SDA AT31 ISP_CAM_REAR_SDA
ISP1_SCL AT32 ISP_CAM_FRONT_SCL
ISP1_SDA AR28 ISP_CAM_FRONT_SDA
SENSOR0_CLK AR31 ISP_CAM_REAR_CLK_R
SENSOR0_RST AT30 ISP_CAM_REAR_SHUTDOWN_L
R0910
33
1/32W 5%
01005 MF
PLACE_NEAR=U0600.AR31:5MM
ISP_CAM_REAR_CLK
SENSOR1_CLK AP32 ISP_CAM_FRONT_CLK_R
SENSOR1_RST AR30 ISP_CAM_FRONT_SHUTDOWN_L
R0911
33
1/32W 5%
01005 MF
PLACE_NEAR=U0600.AP32:5MM
ISP_CAM_FRONT_CLK
SENSOR0_ISTRB AR32 GPIO_SPKRAMP2SOC_RIGHT_IRQ_L
SENSOR0_XSHUTDOWN AR29 GPIO_SPKRAMP2SOC_LEFT_IRQ_L
SENSOR1_ISTRB AP33 GPIO_SOC2ROTTERDAM_DWLD_REQ
SENSOR1_XSHUTDOWN AN33 GPIO_SOC2ROTTERDAM_EN
(USE INTERNAL PU)
MIPI1C_REXT AP31 MIPI1C_REXT
MIPI1C_DPDATA0 AV37 MIPI_CAM_FRONT_DATA_P<0>
MIPI1C_DNDATA0 AW37 MIPI_CAM_FRONT_DATA_N<0>
MIPI1C_DPDATA1 AV35 MIPI_CAM_FRONT_DATA_P<1>
MIPI1C_DNDATA1 AW35 MIPI_CAM_FRONT_DATA_N<1>
MIPI1C_DPCLK AV36 MIPI_CAM_FRONT_CLK_P
MIPI1C_DNCLK AW36 MIPI_CAM_FRONT_CLK_N
SEG: 4.02K IS CORRECT VALUE
PLACE_NEAR=U0600.AP31:10MM
R0921
4.02K
1%
1/32W
MF
01005


=PP0V95_PCIE_SOC
=PP1V8_PCIE_SOC
C1096 1UF CERM 4V 0402 20%
C1097 1UF CERM 4V 0402 20%
C1092 1UF CERM 4V 0402 20%
C1093 1UF CERM 4V 0402 20%
C1094 1UF CERM 4V 0402 20%
C1095 1UF CERM 4V 0402 20%
C1041 0.22UF 20% 6.3V X5R 01005-1
C1046 0.01UF 10% 6.3V X5R 01005
C1040 56PF 5% 6.3V NP0-C0G 01005
C1049 56PF 5% 6.3V NP0-C0G 01005
C1050 0.22UF 20% 6.3V X5R 01005-1
=PP1V0_LPDP_SOC
C1055 1.0UF 20% 6.3V X5R 0201-1
C1045 56PF 5% 6.3V NP0-C0G 01005
PP1V2_PCIE_PLL_SOC_FILT
R1090 0.00 5% 1/32W MF 01005
=PP1V2_PLL_SOC
C1090 56PF 5% 6.3V NP0-C0G 01005
C1091 0.22UF 20% 6.3V X5R 01005-1
LPDP_VDDA10
VDD095_VPTX0_PCIE
VDD095_VPTX1_PCIE
VDD095_VPTX2_PCIE
VDD095_VPTX3_PCIE
VDD095_VP01_PCIE
VDD095_VP23_PCIE
VDDA10_REFCLK_PCIE
VDD18_VPH01_PCIE
VDD18_VPH23_PCIE
VDDA12_PLL_PCIE
24MA
21MA EACH
OMITTABLE
45MA EACH
8MA
26MA EACH
8.5MA
U0600
TMKP88A0-N
FCBGA
SYM 8 OF 15
EDP_AUX_P
EDP_AUX_N
EDP_DATA_P<0>
EDP_DATA_N<0>
EDP_DATA_P<1>
EDP_DATA_N<1>
EDP_DATA_P<2>
EDP_DATA_N<2>
EDP_DATA_P<3>
EDP_DATA_N<3>
LPDP_CAL_DRV_OUT
LPDP_CAL_VSS_EXT
R1023 240 1% 1/32W MF 01005
C1060 100PF 5% 6.3V CERM 01005
RDAR://PROBLEM//16438437
ULPI_DATA[0] SWD_OSCAR_CLK_1V8
ULPI_DATA[1] SWD_OSCAR_IO_1V8
ULPI_DATA[2] GPIO_BRD_REV2
ULPI_DATA[3] GPIO_SOC2DEVBRD_S3E_RESET2_L
ULPI_DATA[4] GPIO_SOC2WLAN_WAKE
ULPI_DATA[5] GPIO_SOC2BT_WAKE
ULPI_DATA[6] GPIO_BRD_REV3
ULPI_DATA[7] GPIO_SOC2AJ_HS3_SHUNT_EN
ULPI_CLK GPIO_SOC2AJ_HS4_SHUNT_EN
ULPI_DIR GPIO_BRD_REV1
ULPI_NXT GPIO_BRD_REV0
ULPI_STP GPIO_SOC2DEVBRD_S3E_WAKE
TOUCH CLK +/-100PPM --> (+/-30PPM FREQUENCY ACCURACY, +/-70PPM FOR JITTER)
CLK32K_OUT CLK_SOC2GRAPE_32K
CPU_SLEEP_STATUS
AN40 NC_CPU_SLEEP_STATUS
EDP_HPD
(12MHZ TO EXT NVME CTL) NAND_SYS_CLK J35 CLK_SOC2DEVBRD_PCIE_24MHZ
PERST# FOR LANE 0 IS GPIO[39]
NC_PCIE_RX0_P
NC_PCIE_RX0_N
NC_PCIE_TX0_P
NC_PCIE_TX0_N
NC_PCIE_CLK0_P
NC_PCIE_CLK0_N
NC_PCIE_CLKREQ0
PCIE_WLAN2SOC_TX_P
PCIE_WLAN2SOC_TX_N
PCIE_SOC2WLAN_TX_P 0.1UF C1022 20% 4V 01005 X5R
PCIE_SOC2WLAN_TX_N 0.1UF C1023 20% 4V 01005 X5R
PCIE_SOC2WLAN_TX_C_P
PCIE_SOC2WLAN_TX_C_N
WIFI
PERST# FOR LANE 1 IS GPIO[43]
PCIE_SOC2WLAN_CLK_C_P
PCIE_SOC2WLAN_CLK_C_N
PCIE_SOC2WLAN_CLK_P 0.1UF C1024 20% 4V 01005 X5R
PCIE_SOC2WLAN_CLK_N 0.1UF C1025 20% 4V 01005 X5R
=PP1V8_S2R_MISC
R1020 1.00K 5% 1/32W MF 01005
PCIE_WLAN2SOC_CLKREQ_L
NC_PCIE_RX2_P
NC_PCIE_RX2_N
NC_PCIE_TX2_P
NC_PCIE_TX2_N
NC_PCIE_CLK2_P
NC_PCIE_CLK2_N
PCIE_DEVBRD2SOC_CLKREQ_L
NC_PCIE_RX3_P
NC_PCIE_RX3_N
NC_PCIE_TX3_P
NC_PCIE_TX3_N
NC_PCIE_CLK3_P
NC_PCIE_CLK3_N
NC_PCIE_CLKREQ3
NC_PCIE_REF_CK01_P
NC_PCIE_REF_CK01_N
NC_PCIE_REF_CK23_P
NC_PCIE_REF_CK23_N
PCIE_RESREF01
NC_PCIE_RESREF23
INTERNAL REF IS USED
SEG: OK TO FLOAT REF_PAD_CLK
SEG: UNUSED RESREFS CAN FLOAT
CORRECT VALUE FOR CAPRI
R1021 200 1% 1/32W MF 01005
BUT THE RESPECTIVE VPTX SUPPLY SHALL BE CONNECTED
CAPRI DATASHEET 0.
FOR UNUSED PCIE LINKS, THE PCIE_TX_P/M PINS MAY BE LEFT FLOATING
PCIE_PERST0*
PCIE_PERST1*
PCIE_PERST2*
PCIE_PERST3*
NC_PCIE_PERST0
NC_PCIE_PERST3
PCIE_SOC2DEVBRD_RESET_L
PCIE_SOC2WLAN_RESET_L
R1022 100K 5% 1/32W MF 01005


U0600
TMKP88A0-N
FCBGA
SYM 1 OF 15
OMIT_TABLE
DDR0_CA[0] DDR0 CA<0> A15
DDR0_CA[1] DDR0 CA<1> B15
DDR0_CA[2] DDR0 CA<2> C15
DDR0_CA[3] DDR0 CA<3> D16
DDR0_CA[4] DDR0 CA<4> A14
DDR0_CA[5] DDR0 CA<5> A11
DDR0_CA[6] DDR0 CA<6> C11
DDR0_CA[7] DDR0 CA<7> D12
DDR0_CA[8] DDR0 CA<8> A10
DDR0_CA[9] DDR0 CA<9> B10
DDR0_CK[0] DDR0 CK_P B12
DDR0_CKB[0] DDR0 CK_N A12
DDR0_CK[1] NC_DDR0_CK<1> NO_TEST=TRUE D13
DDR0_CKB[1] NC_DDR0_CKB<1> NO_TEST=TRUE C12
DDR0_CKE[0] DDR0 CKE<0> B14
DDR0_CKE[1] NC_DDR0_CKE<1> NO_TEST=TRUE E13
DDR0_CKEIN RESET_SOC_L D14
DDR0_CSN[0] DDR0 CSN<0> D15
DDR0_CSN[1] NC_DDR0_CSN<1> NO_TEST=TRUE E14
DDR0_DM[0] DDR0 DM<0> E6
DDR0_DM[1] DDR0 DM<1> E5
DDR0_DM[2] DDR0 DM<2> B5
DDR0_DM[3] DDR0 DM<3> H5
DDR0_DQ[0] DDR0 DQ<0> F10
DDR0_DQ[1] DDR0 DQ<1> E10
DDR0_DQ[2] DDR0 DQ<2> D10
DDR0_DQ[3] DDR0 DQ<3> F9
DDR0_DQ[4] DDR0 DQ<4> D9
DDR0_DQ[5] DDR0 DQ<5> E8
DDR0_DQ[6] DDR0 DQ<6> D8
DDR0_DQ[7] DDR0 DQ<7> F7
DDR0_DQ[8] DDR0 DQ<8> F4
DDR0_DQ[9] DDR0 DQ<9> E3
DDR0_DQ[10] DDR0 DQ<10> C3
DDR0_DQ[11] DDR0 DQ<11> F2
DDR0_DQ[12] DDR0 DQ<12> D3
DDR0_DQ[13] DDR0 DQ<13> F1
DDR0_DQ[14] DDR0 DQ<14> E1
DDR0_DQ[15] DDR0 DQ<15> D2
DDR0_DQ[16] DDR0 DQ<16> C9
DDR0_DQ[17] DDR0 DQ<17> B9
DDR0_DQ[18] DDR0 DQ<18> A9
DDR0_DQ[19] DDR0 DQ<19> C8
DDR0_DQ[20] DDR0 DQ<20> A8
DDR0_DQ[21] DDR0 DQ<21> B7
DDR0_DQ[22] DDR0 DQ<22> A7
DDR0_DQ[23] DDR0 DQ<23> C6
DDR0_DQ[24] DDR0 DQ<24> J4
DDR0_DQ[25] DDR0 DQ<25> H3
DDR0_DQ[26] DDR0 DQ<26> G3
DDR0_DQ[27] DDR0 DQ<27> J2
DDR0_DQ[28] DDR0 DQ<28> G2
DDR0_DQ[29] DDR0 DQ<29> J1
DDR0_DQ[30] DDR0 DQ<30> H1
DDR0_DQ[31] DDR0 DQ<31> G1
DDR0_PDQS[0] DDR0 DQS P<0> D7
DDR0_NDQS[0] DDR0 DQS N<0> D6
DDR0_PDQS[1] DDR0 DQS P<1> D4
DDR0_NDQS[1] DDR0 DQS N<1> D5
DDR0_PDQS[2] DDR0 DQS P<2> A6
DDR0_NDQS[2] DDR0 DQS N<2> A5
DDR0_PDQS[3] DDR0 DQS P<3> G4
DDR0_NDQS[3] DDR0 DQS N<3> G5
DDR0_VREF_CA PPVREF_DDR0_CA_SOC A13
DDR0_ZQ_CA DDR0_ZQ_CA_SOC C13
DDR0_VREF_DQ0 PPVREF_DDR0_DQ_SOC H10
DDR0_VREF_DQ1 L6
DDR0_ZQ_DQ0 DDR0_ZQ_DQ0_SOC G9
DDR0_ZQ_DQ1 DDR0_ZQ_DQ1_SOC M6
VDD12_CKE_DDR0 =PP1V2_S2R_DDR_SOC F13
DDR0
DDR1
DDR1_CA[0] DDR1 CA<0> E21
DDR1_CA[1] DDR1 CA<1> D20
DDR1_CA[2] DDR1 CA<2> E20
DDR1_CA[3] DDR1 CA<3> B20
DDR1_CA[4] DDR1 CA<4> A20
DDR1_CA[5] DDR1 CA<5> A17
DDR1_CA[6] DDR1 CA<6> C17
DDR1_CA[7] DDR1 CA<7> D17
DDR1_CA[8] DDR1 CA<8> A16
DDR1_CA[9] DDR1 CA<9> B16
DDR1_CK[0] DDR1 CK_P B18
DDR1_CKB[0] DDR1 CK_N A18
DDR1_CK[1] NC_DDR1_CK<1> NO_TEST=TRUE D18
DDR1_CKB[1] NC_DDR1_CKB<1> NO_TEST=TRUE C18
DDR1_CKE[0] DDR1 CKE<0> D19
DDR1_CKE[1] NC_DDR1_CKE<1> NO_TEST=TRUE E18
DDR1_CKEIN RESET_SOC_L C19
DDR1_CSN[0] DDR1 CSN<0> F20
DDR1_CSN[1] NC_DDR1_CSN<1> NO_TEST=TRUE E19
DDR1_DM[0] DDR1 DM<0> U2
DDR1_DM[1] DDR1 DM<1> U5
DDR1_DM[2] DDR1 DM<2> W5
DDR1_DM[3] DDR1 DM<3> R2
DDR1_DQ[0] DDR1 DQ<0> AA3
DDR1_DQ[1] DDR1 DQ<1> AA2
DDR1_DQ[2] DDR1 DQ<2> AA1
DDR1_DQ[3] DDR1 DQ<3> Y3
DDR1_DQ[4] DDR1 DQ<4> Y1
DDR1_DQ[5] DDR1 DQ<5> W2
DDR1_DQ[6] DDR1 DQ<6> W1
DDR1_DQ[7] DDR1 DQ<7> V3
DDR1_DQ[8] DDR1 DQ<8> T6
DDR1_DQ[9] DDR1 DQ<9> R5
DDR1_DQ[10] DDR1 DQ<10> R4
DDR1_DQ[11] DDR1 DQ<11> P6
DDR1_DQ[12] DDR1 DQ<12> P4
DDR1_DQ[13] DDR1 DQ<13> N6
DDR1_DQ[14] DDR1 DQ<14> N5
DDR1_DQ[15] DDR1 DQ<15> N4
DDR1_DQ[16] DDR1 DQ<16> AC6
DDR1_DQ[17] DDR1 DQ<17> AC5
DDR1_DQ[18] DDR1 DQ<18> AC4
DDR1_DQ[19] DDR1 DQ<19> AB6
DDR1_DQ[20] DDR1 DQ<20> AB4
DDR1_DQ[21] DDR1 DQ<21> AA5
DDR1_DQ[22] DDR1 DQ<22> AA4
DDR1_DQ[23] DDR1 DQ<23> Y6
DDR1_DQ[24] DDR1 DQ<24> P3
DDR1_DQ[25] DDR1 DQ<25> N2
DDR1_DQ[26] DDR1 DQ<26> N1
DDR1_DQ[27] DDR1 DQ<27> M3
DDR1_DQ[28] DDR1 DQ<28> M1
DDR1_DQ[29] DDR1 DQ<29> L3
DDR1_DQ[30] DDR1 DQ<30> L2
DDR1_DQ[31] DDR1 DQ<31> L1
DDR1_PDQS[0] DDR1 DQS P<0> V1
DDR1_NDQS[0] DDR1 DQS N<0> U1
DDR1_PDQS[1] DDR1 DQS P<1> T4
DDR1_NDQS[1] DDR1 DQS N<1> U4
DDR1_PDQS[2] DDR1 DQS P<2> Y4
DDR1_NDQS[2] DDR1 DQS N<2> W4
DDR1_PDQS[3] DDR1 DQS P<3> P1
DDR1_NDQS[3] DDR1 DQS N<3> R1
DDR1_VREF_CA PPVREF_DDR1_CA_SOC A19
DDR1_ZQ_CA DDR1_ZQ_CA_SOC F18
DDR1_VREF_DQ0 PPVREF_DDR1_DQ_SOC AA7
DDR1_VREF_DQ1 R7
DDR1_ZQ_DQ0 DDR1_ZQ_DQ0_SOC AA6
DDR1_ZQ_DQ1 DDR1_ZQ_DQ1_SOC R6
VDD12_CKE_DDR1 =PP1V2_S2R_DDR_SOC F17
SEG: OK TO FLOAT CK, CKB, CKE AND CSN PINS
C1101 0.22UF 20% 6.3V X5R 01005-1
C1100 0.22UF 20% 6.3V X5R 01005-1
R1100 240 1% 1/32W MF 01005
R1102 240 1% 1/32W MF 01005
R1104 240 1% 1/32W MF 01005
R1101 240 1% 1/32W MF 01005
R1103 240 1% 1/32W MF 01005
R1105 240 1% 1/32W MF 01005
DDR0_ZQ_CA_SOC
DDR0_ZQ_DQ0_SOC
DDR0_ZQ_DQ1_SOC
DDR1_ZQ_CA_SOC
DDR1_ZQ_DQ0_SOC
DDR1_ZQ_DQ1_SOC
U0600
TMKP88A0-N
FCBGA
SYM 2 OF 15
OMIT_TABLE
DDR2_CA[0] DDR2 CA<0> AW22
DDR2_CA[1] DDR2 CA<1> AV22
DDR2_CA[2] DDR2 CA<2> AU22
DDR2_CA[3] DDR2 CA<3> AT23
DDR2_CA[4] DDR2 CA<4> AW23
DDR2_CA[5] DDR2 CA<5> AW26
DDR2_CA[6] DDR2 CA<6> AU26
DDR2_CA[7] DDR2 CA<7> AT27
DDR2_CA[8] DDR2 CA<8> AW27
DDR2_CA[9] DDR2 CA<9> AV27
DDR2_CK[0] DDR2 CK_P AV25
DDR2_CKB[0] DDR2 CK_N AW25
DDR2_CK[1] NC_DDR2_CK<1> NO_TEST=TRUE AU25
DDR2_CKB[1] NC_DDR2_CKB<1> NO_TEST=TRUE AT26
DDR2_CKE[0] DDR2_CKE<0> AV23
DDR2_CKE[1] NC_DDR2_CKE<1> NO_TEST=TRUE AR24
DDR2_CKEIN RESET_SOC_L AT25
DDR2_CSN[0] DDR2_CSN<0> AT24
DDR2_CSN[1] NC_DDR2_CSN<1> NO_TEST=TRUE AR23
DDR2_DM[0] DDR2_DM<0> AL2
DDR2_DM[1] DDR2_DM<1> AJ5
DDR2_DM[2] DDR2_DM<2> AL5
DDR2_DM[3] DDR2_DM<3> AJ2
DDR2_DQ[0] DDR2_DQ<0> AR3
DDR2_DQ[1] DDR2_DQ<1> AR2
DDR2_DQ[2] DDR2_DQ<2> AR1
DDR2_DQ[3] DDR2_DQ<3> AP3
DDR2_DQ[4] DDR2_DQ<4> AP1
DDR2_DQ[5] DDR2_DQ<5> AN2
DDR2_DQ[6] DDR2_DQ<6> AN1
DDR2_DQ[7] DDR2_DQ<7> AM3
DDR2_DQ[8] DDR2_DQ<8> AH6
DDR2_DQ[9] DDR2_DQ<9> AG5
DDR2_DQ[10] DDR2_DQ<10> AG4
DDR2_DQ[11] DDR2_DQ<11> AF6
DDR2_DQ[12] DDR2_DQ<12> AF4
DDR2_DQ[13] DDR2_DQ<13> AE6
DDR2_DQ[14] DDR2_DQ<14> AE5
DDR2_DQ[15] DDR2_DQ<15> AE4
DDR2_DQ[16] DDR2_DQ<16> AR6
DDR2_DQ[17] DDR2_DQ<17> AR5
DDR2_DQ[18] DDR2_DQ<18> AR4
DDR2_DQ[19] DDR2_DQ<19> AP6
DDR2_DQ[20] DDR2_DQ<20> AP4
DDR2_DQ[21] DDR2_DQ<21> AN5
DDR2_DQ[22] DDR2_DQ<22> AN4
DDR2_DQ[23] DDR2_DQ<23> AM6
DDR2_DQ[24] DDR2_DQ<24> AH3
DDR2_DQ[25] DDR2_DQ<25> AG2
DDR2_DQ[26] DDR2_DQ<26> AG1
DDR2_DQ[27] DDR2_DQ<27> AF3
DDR2_DQ[28] DDR2_DQ<28> AF1
DDR2_DQ[29] DDR2_DQ<29> AE3
DDR2_DQ[30] DDR2_DQ<30> AE2
DDR2_DQ[31] DDR2_DQ<31> AE1
DDR2_PDQS[0] DDR2_DQS_P<0> AM1
DDR2_NDQS[0] DDR2_DQS_N<0> AL1
DDR2_PDQS[1] DDR2_DQS_P<1> AH4
DDR2_NDQS[1] DDR2_DQS_N<1> AJ4
DDR2_PDQS[2] DDR2_DQS_P<2> AM4
DDR2_NDQS[2] DDR2_DQS_N<2> AL4
DDR2_PDQS[3] DDR2_DQS_P<3> AH1
DDR2_NDQS[3] DDR2_DQS_N<3> AJ1
DDR2_VREF_CA PPVREF_DDR2_CA_SOC AW24
DDR2_ZQ_CA DDR2_ZQ_CA_SOC AU24
DDR2_VREF_DQ0 PPVREF_DDR2_DQ_SOC AL7
DDR2_VREF_DQ1 AG7
DDR2_ZQ_DQ0 DDR2_ZQ_DQ0_SOC AL6
DDR2_ZQ_DQ1 DDR2_ZQ_DQ1_SOC AG6
=PP1V2_S2R_DDR_SOC AP24
DDR2
DDR3
DDR3_CA[0] DDR3 CA<0> AW15
DDR3_CA[1] DDR3 CA<1> AW16
DDR3_CA[2] DDR3 CA<2> AV16
DDR3_CA[3] DDR3 CA<3> AU16
DDR3_CA[4] DDR3 CA<4> AW17
DDR3_CA[5] DDR3 CA<5> AW20
DDR3_CA[6] DDR3 CA<6> AU20
DDR3_CA[7] DDR3 CA<7> AT21
DDR3_CA[8] DDR3 CA<8> AW21
DDR3_CA[9] DDR3 CA<9> AV21
DDR3_CK[0] DDR3 CK_P AV19
DDR3_CKB[0] DDR3 CK_N AW19
DDR3_CK[1] NC_DDR3_CK<1> NO_TEST=TRUE AU19
DDR3_CKB[1] NC_DDR3_CKB<1> NO_TEST=TRUE AT20
DDR3_CKE[0] DDR3 CKE<0> AV17
DDR3_CKE[1] NC_DDR3_CKE<1> NO_TEST=TRUE AR20
DDR3_CKEIN RESET_SOC_L AT19
DDR3_CSN[0] DDR3 CSN<0> AT18
DDR3_CSN[1] NC_DDR3_CSN<1> NO_TEST=TRUE AR19
DDR3_DM[0] DDR3 DM<0> AR11
DDR3_DM[1] DDR3 DM<1> AV10
DDR3_DM[2] DDR3 DM<2> AV8
DDR3_DM[3] DDR3 DM<3> AR13
DDR3_DQ[0] DDR3 DQ<0> AP7
DDR3_DQ[1] DDR3 DQ<1> AR7
DDR3_DQ[2] DDR3 DQ<2> AT7
DDR3_DQ[3] DDR3 DQ<3> AP8
DDR3_DQ[4] DDR3 DQ<4> AT8
DDR3_DQ[5] DDR3 DQ<5> AR9
DDR3_DQ[6] DDR3 DQ<6> AT9
DDR3_DQ[7] DDR3 DQ<7> AP10
DDR3_DQ[8] DDR3 DQ<8> AU11
DDR3_DQ[9] DDR3 DQ<9> AV12
DDR3_DQ[10] DDR3 DQ<10> AW12
DDR3_DQ[11] DDR3 DQ<11> AU13
DDR3_DQ[12] DDR3 DQ<12> AW13
DDR3_DQ[13] DDR3 DQ<13> AU14
DDR3_DQ[14] DDR3 DQ<14> AV14
DDR3_DQ[15] DDR3 DQ<15> AW14
DDR3_DQ[16] DDR3 DQ<16> AT4
DDR3_DQ[17] DDR3 DQ<17> AU4
DDR3_DQ[18] DDR3 DQ<18> AV4
DDR3_DQ[19] DDR3 DQ<19> AU5
DDR3_DQ[20] DDR3 DQ<20> AW5
DDR3_DQ[21] DDR3 DQ<21> AV6
DDR3_DQ[22] DDR3 DQ<22> AW6
DDR3_DQ[23] DDR3 DQ<23> AU7
DDR3_DQ[24] DDR3 DQ<24> AP14
DDR3_DQ[25] DDR3 DQ<25> AR15
DDR3_DQ[26] DDR3 DQ<26> AT15
DDR3_DQ[27] DDR3 DQ<27> AP16
DDR3_DQ[28] DDR3 DQ<28> AT16
DDR3_DQ[29] DDR3 DQ<29> AP17
DDR3_DQ[30] DDR3 DQ<30> AR17
DDR3_DQ[31] DDR3 DQ<31> AT17
DDR3_PDQS[0] DDR3 DQS P<0> AT10
DDR3_NDQS[0] DDR3 DQS N<0> AT11
DDR3_PDQS[1] DDR3 DQS P<1> AW11
DDR3_NDQS[1] DDR3 DQS N<1> AW10
DDR3_PDQS[2] DDR3 DQS P<2> AW7
DDR3_NDQS[2] DDR3 DQS N<2> AW8
DDR3_PDQS[3] DDR3 DQS P<3> AT14
DDR3_NDQS[3] DDR3 DQS N<3> AT13
DDR3_VREF_CA PPVREF_DDR3_CA_SOC AW18
DDR3_ZQ_CA DDR3_ZQ_CA_SOC AU18
DDR3_VREF_DQ0 PPVREF_DDR3_DQ_SOC AN9
DDR3_VREF_DQ1 AN15
DDR3_ZQ_DQ0 DDR3_ZQ_DQ0_SOC AP9
DDR3_ZQ_DQ1 DDR3_ZQ_DQ1_SOC AP15
=PP1V2_S2R_DDR_SOC AP19
C1102 0.22UF 20% 6.3V X5R 01005-1
C1103 0.22UF 20% 6.3V X5R 01005-1
SEG: OK TO FLOAT CK, CKB, CKE AND CSN PINS
R1106 240 1% 1/32W MF 01005
R1107 240 1% 1/32W MF 01005
R1108 240 1% 1/32W MF 01005
R1109 240 1% 1/32W MF 01005
R1110 240 1% 1/32W MF 01005
R1111 240 1% 1/32W MF 01005
DDR2_ZQ_CA_SOC
DDR2_ZQ_DQ0_SOC
DDR2_ZQ_DQ1_SOC
DDR3_ZQ_CA_SOC
DDR3_ZQ_DQ0_SOC
DDR3_ZQ_DQ1_SOC
=PP1V2_VDDIOD_SOC
C1194 0.1UF 20% 6.3V X5R-CERM 01005
C1195 0.1UF 20% 6.3V X5R-CERM 01005
C1196 0.1UF 20% 6.3V X5R-CERM 01005
C1197 0.1UF 20% 6.3V X5R-CERM 01005
R1194 4.7K 1% 1/32W MF 01005
R1195 4.7K 1% 1/32W MF 01005
R1196 4.7K 1% 1/32W MF 01005
R1197 4.7K 1% 1/32W MF 01005
PPVREF_DDR0_DQ_SOC VOLTAGE=0.6V
PPVREF_DDR1_DQ_SOC VOLTAGE=0.6V
C1184 0.1UF 20% 6.3V X5R-CERM 01005
C1185 0.1UF 20% 6.3V X5R-CERM 01005
C1186 0.1UF 20% 6.3V X5R-CERM 01005
C1187 0.1UF 20% 6.3V X5R-CERM 01005
R1184 4.7K 1% 1/32W MF 01005
R1185 4.7K 1% 1/32W MF 01005
R1186 4.7K 1% 1/32W MF 01005
R1187 4.7K 1% 1/32W MF 01005
PPVREF_DDR2_DQ_SOC VOLTAGE=0.6V
PPVREF_DDR3_DQ_SOC VOLTAGE=0.6V
ONCE ROUTED SEG NEEDS TO CHECK PI OF *_VREF_DQ0 AND *_VREF_DQ1 BEING TIED TOGETHER
=PP1V2_S2R_DDR_SOC
C1190 0.1UF 20% 6.3V X5R-CERM 01005
C1191 0.1UF 20% 6.3V X5R-CERM 01005
C1192 0.1UF 20% 6.3V X5R-CERM 01005
C1193 0.1UF 20% 6.3V X5R-CERM 01005
R1190 10K 1% 1/32W MF 01005
R1191 10K 1% 1/32W MF 01005
R1192 10K 1% 1/32W MF 01005
R1193 10K 1% 1/32W MF 01005
PPVREF_DDR0_CA_SOC VOLTAGE=0.6V
PPVREF_DDR1_CA_SOC VOLTAGE=0.6V
C1180 0.1UF 20% 6.3V X5R-CERM 01005
C1181 0.1UF 20% 6.3V X5R-CERM 01005
C1182 0.1UF 20% 6.3V X5R-CERM 01005
C1183 0.1UF 20% 6.3V X5R-CERM 01005
R1180 10K 1% 1/32W MF 01005
R1181 10K 1% 1/32W MF 01005
R1182 10K 1% 1/32W MF 01005
R1183 10K 1% 1/32W MF 01005
PPVREF_DDR2_CA_SOC VOLTAGE=0.6V
PPVREF_DDR3_CA_SOC VOLTAGE=0.6V

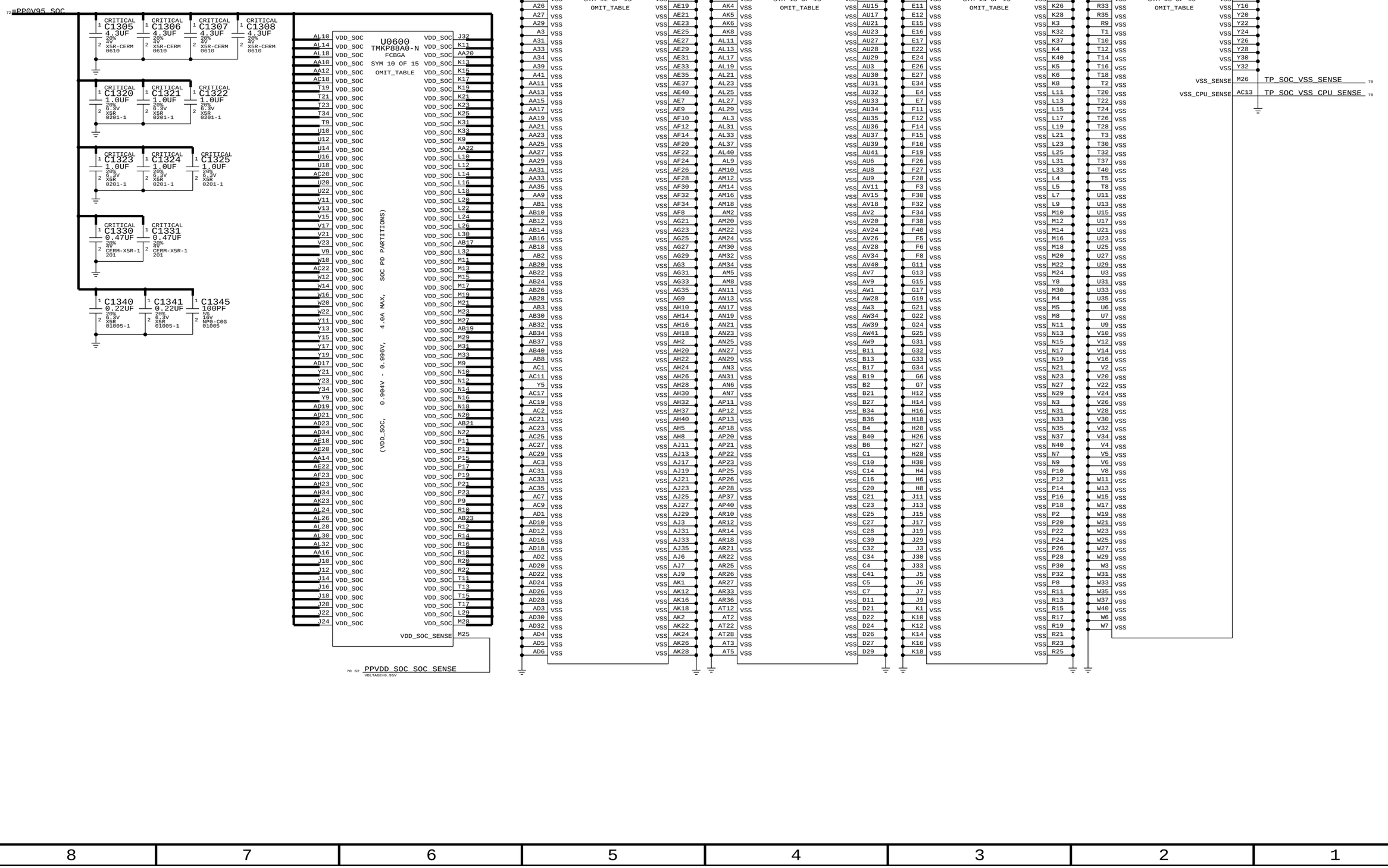


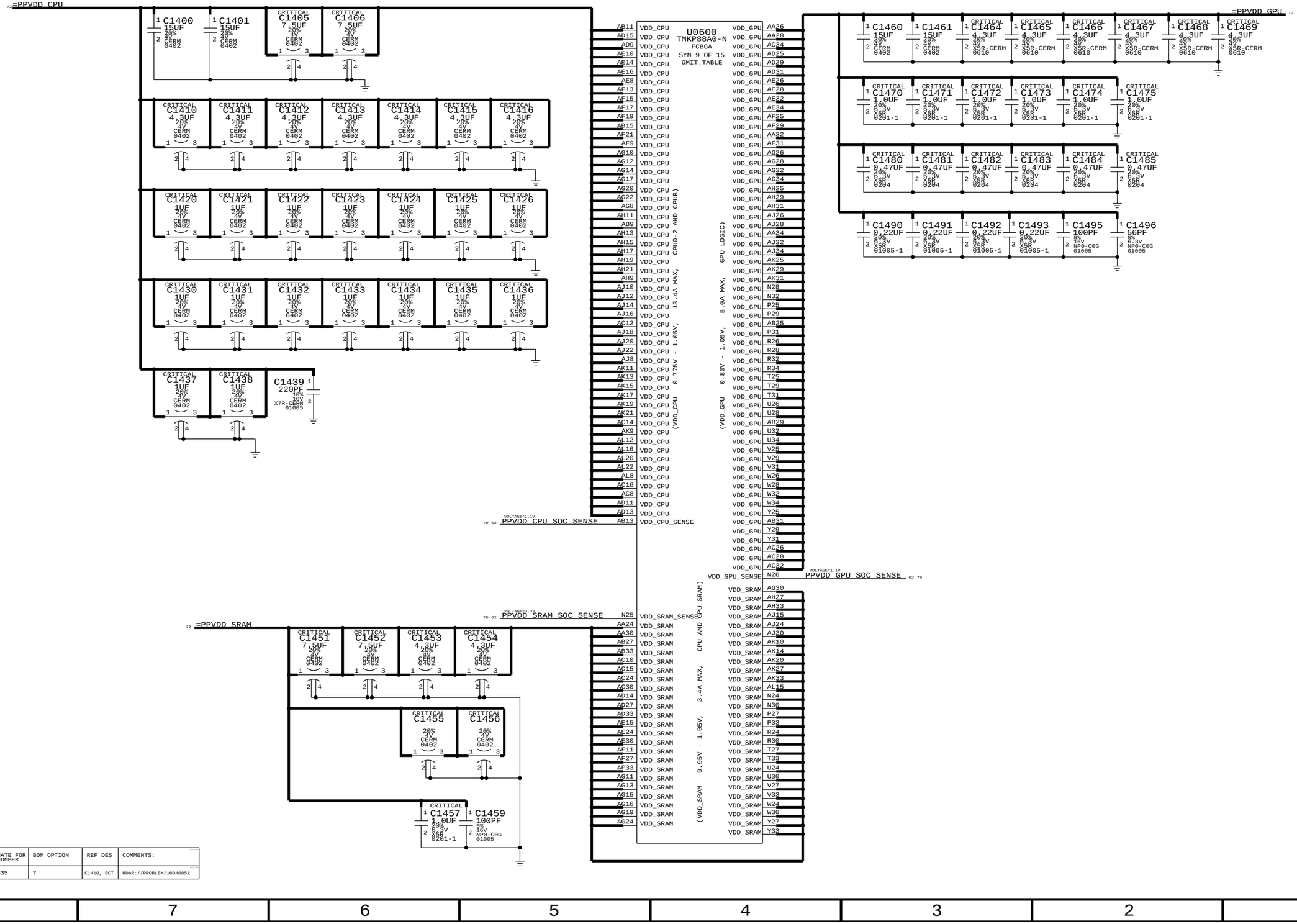
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657			QTY 22 RDAR://PROBLEM/8837828
138S0702	138S0657			QTY 22 RDAR://PROBLEM/8837828

REFDES FOR ALTERATIVE TABLE

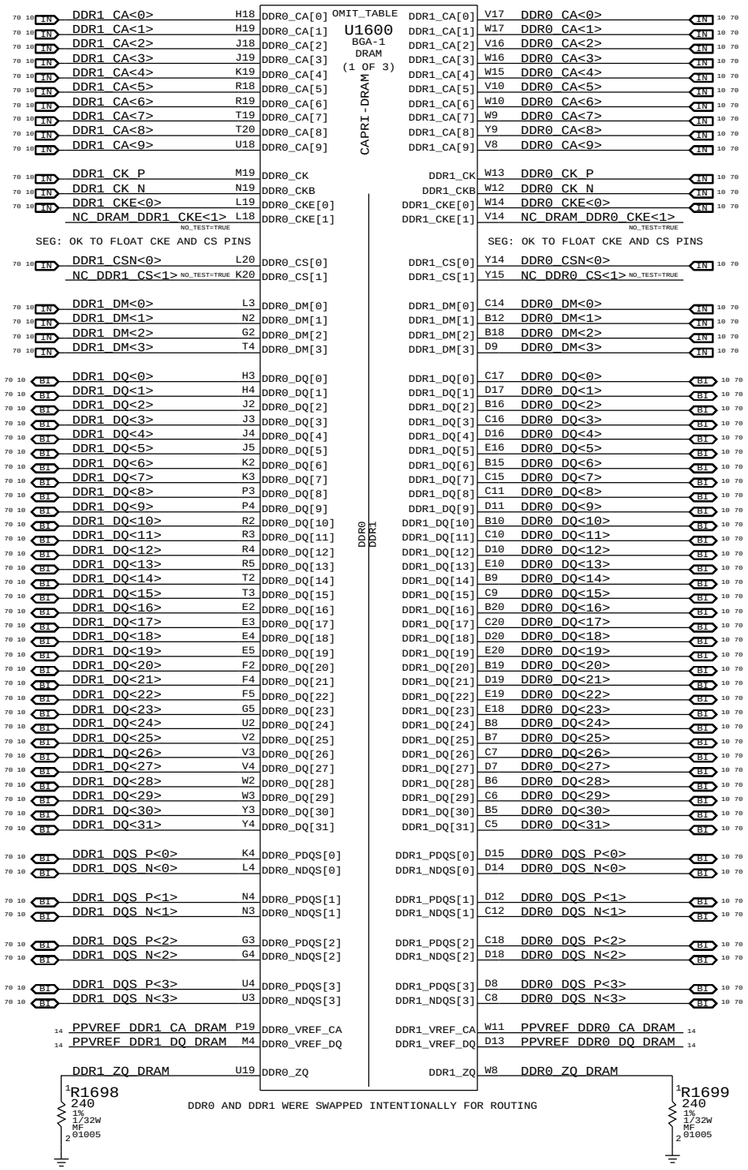
C1203,C1204,C1240, C1305-C1308, C1404-C1409,C1464-C1469,C1445,C1446

C1602,C1603,C1642,C1643, C1702,C1703,C1742,C1743


=PP0V95_SOC
CRITICAL C1305 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1306 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1307 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1308 4.3UF 20% 4V X5R-CERM 0610
CRITICAL C1320 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C1321 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C1322 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C1323 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C1324 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C1325 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C1330 0.47UF 20% 4V CERM-X5R-1 201
CRITICAL C1331 0.47UF 20% 4V CERM-X5R-1 201
C1340 0.22UF 20% 6.3V X5R 01005-1
C1341 0.22UF 20% 6.3V X5R 01005-1
C1345 100PF 5% 16V NP0-C0G 01005
U0600 TMKP88A0-N FCBGA SYM 10 OF 15 OMIT_TABLE
U0600 TMKP88A0-N FCBGA SYM 12 OF 15 OMIT_TABLE
U0600 TMKP88A0-N FCBGA SYM 13 OF 15 OMIT_TABLE
U0600 TMKP88A0-N FCBGA SYM 14 OF 15 OMIT_TABLE
U0600 TMKP88A0-N FCBGA SYM 15 OF 15 OMIT_TABLE
VDD_SOC
SOC PD PARTITIONS)
4.0A MAX,
(VDD_SOC, 0.904V - 0.996V,
VDD_SOC_SENSE
PPVDD_SOC_SOC_SENSE
VOLTAGE=0.95V
VSS
VSS_SENSE
TP_SOC_VSS_SENSE
VSS_CPU_SENSE
TP_SOC_VSS_CPU_SENSE



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00006	138S0835	?	C1410, ECT	RDAR://PROBLEM/16040051


DDR1_CA<0> H18 DDR0_CA[0]
DDR1_CA<1> H19 DDR0_CA[1]
DDR1_CA<2> J18 DDR0_CA[2]
DDR1_CA<3> J19 DDR0_CA[3]
DDR1_CA<4> K19 DDR0_CA[4]
DDR1_CA<5> R18 DDR0_CA[5]
DDR1_CA<6> R19 DDR0_CA[6]
DDR1_CA<7> T19 DDR0_CA[7]
DDR1_CA<8> T20 DDR0_CA[8]
DDR1_CA<9> U18 DDR0_CA[9]
OMIT_TABLE
U1600
BGA-1
DRAM
(1 OF 3)
CAPRI-DRAM
DDR1_CA[0] V17 DDR0_CA<0>
DDR1_CA[1] W17 DDR0_CA<1>
DDR1_CA[2] V16 DDR0_CA<2>
DDR1_CA[3] W16 DDR0_CA<3>
DDR1_CA[4] W15 DDR0_CA<4>
DDR1_CA[5] V10 DDR0_CA<5>
DDR1_CA[6] W10 DDR0_CA<6>
DDR1_CA[7] W9 DDR0_CA<7>
DDR1_CA[8] Y9 DDR0_CA<8>
DDR1_CA[9] V8 DDR0_CA<9>
DDR1_CK P M19 DDR0_CK
DDR1_CK N N19 DDR0_CKB
DDR1_CKE<0> L19 DDR0_CKE[0]
NC_DRAM DDR1 CKE<1> L18 DDR0_CKE[1]
NO_TEST=TRUE
SEG: OK TO FLOAT CKE AND CS PINS
DDR1_CK P W13 DDR0 CK P
DDR1_CK N W12 DDR0 CK N
DDR1_CKE<0> W14 DDR0_CKE<0>
NC_DRAM DDR0 CKE<1> V14
NO_TEST=TRUE
SEG: OK TO FLOAT CKE AND CS PINS
DDR1_CSN<0> L20 DDR0_CS[0]
NC_DDR1_CS<1> K20 DDR0_CS[1]
DDR1_CS[0] Y14 DDR0 CSN<0>
DDR1_CS[1] Y15 NC_DDR0_CS<1>
NO_TEST=TRUE
DDR1_DM<0> L3 DDR0_DM[0]
DDR1_DM<1> N2 DDR0_DM[1]
DDR1_DM<2> G2 DDR0_DM[2]
DDR1_DM<3> T4 DDR0_DM[3]
DDR1_DM[0] C14 DDR0_DM<0>
DDR1_DM[1] B12 DDR0_DM<1>
DDR1_DM[2] B18 DDR0_DM<2>
DDR1_DM[3] D9 DDR0_DM<3>
DDR1_DQ<0> H3 DDR0_DQ[0]
DDR1_DQ<1> H4 DDR0_DQ[1]
DDR1_DQ<2> J2 DDR0_DQ[2]
DDR1_DQ<3> J3 DDR0_DQ[3]
DDR1_DQ<4> J4 DDR0_DQ[4]
DDR1_DQ<5> J5 DDR0_DQ[5]
DDR1_DQ<6> K2 DDR0_DQ[6]
DDR1_DQ<7> K3 DDR0_DQ[7]
DDR1_DQ<8> P3 DDR0_DQ[8]
DDR1_DQ<9> P4 DDR0_DQ[9]
DDR1_DQ<10> R2 DDR0_DQ[10]
DDR1_DQ<11> R3 DDR0_DQ[11]
DDR1_DQ<12> R4 DDR0_DQ[12]
DDR1_DQ<13> R5 DDR0_DQ[13]
DDR1_DQ<14> T2 DDR0_DQ[14]
DDR1_DQ<15> T3 DDR0_DQ[15]
DDR1_DQ<16> E2 DDR0_DQ[16]
DDR1_DQ<17> E3 DDR0_DQ[17]
DDR1_DQ<18> E4 DDR0_DQ[18]
DDR1_DQ<19> E5 DDR0_DQ[19]
DDR1_DQ<20> F2 DDR0_DQ[20]
DDR1_DQ<21> F4 DDR0_DQ[21]
DDR1_DQ<22> F5 DDR0_DQ[22]
DDR1_DQ<23> G5 DDR0_DQ[23]
DDR1_DQ<24> U2 DDR0_DQ[24]
DDR1_DQ<25> V2 DDR0_DQ[25]
DDR1_DQ<26> V3 DDR0_DQ[26]
DDR1_DQ<27> V4 DDR0_DQ[27]
DDR1_DQ<28> W2 DDR0_DQ[28]
DDR1_DQ<29> W3 DDR0_DQ[29]
DDR1_DQ<30> Y3 DDR0_DQ[30]
DDR1_DQ<31> Y4 DDR0_DQ[31]
DDR0
DDR1
DDR1_DQ[0] C17 DDR0_DQ<0>
DDR1_DQ[1] D17 DDR0_DQ<1>
DDR1_DQ[2] B16 DDR0_DQ<2>
DDR1_DQ[3] C16 DDR0_DQ<3>
DDR1_DQ[4] D16 DDR0_DQ<4>
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DDR1_PDQS N<0> L4 DDR0_NDQS[0]
DDR1_PDQS P<1> N4 DDR0_PDQS[1]
DDR1_PDQS N<1> N3 DDR0_NDQS[1]
DDR1_PDQS P<2> G3 DDR0_PDQS[2]
DDR1_PDQS N<2> G4 DDR0_NDQS[2]
DDR1_PDQS P<3> U4 DDR0_PDQS[3]
DDR1_PDQS N<3> U3 DDR0_NDQS[3]
DDR1_PDQS[0] D15 DDR0_DQS_P<0>
DDR1_NDQS[0] D14 DDR0_DQS_N<0>
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DDR1_NDQS[1] C12 DDR0_DQS_N<1>
DDR1_PDQS[2] C18 DDR0_DQS_P<2>
DDR1_NDQS[2] D18 DDR0_DQS_N<2>
DDR1_PDQS[3] D8 DDR0_DQS_P<3>
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PPVREF_DDR1_DQ_DRAM M4 DDR0_VREF_DQ
DDR1_ZQ_DRAM U19 DDR0_ZQ
DDR1_VREF_CA W11 PPVREF_DDR0_CA_DRAM
DDR1_VREF_DQ D13 PPVREF_DDR0_DQ_DRAM
DDR1_ZQ W8 DDR0_ZQ_DRAM
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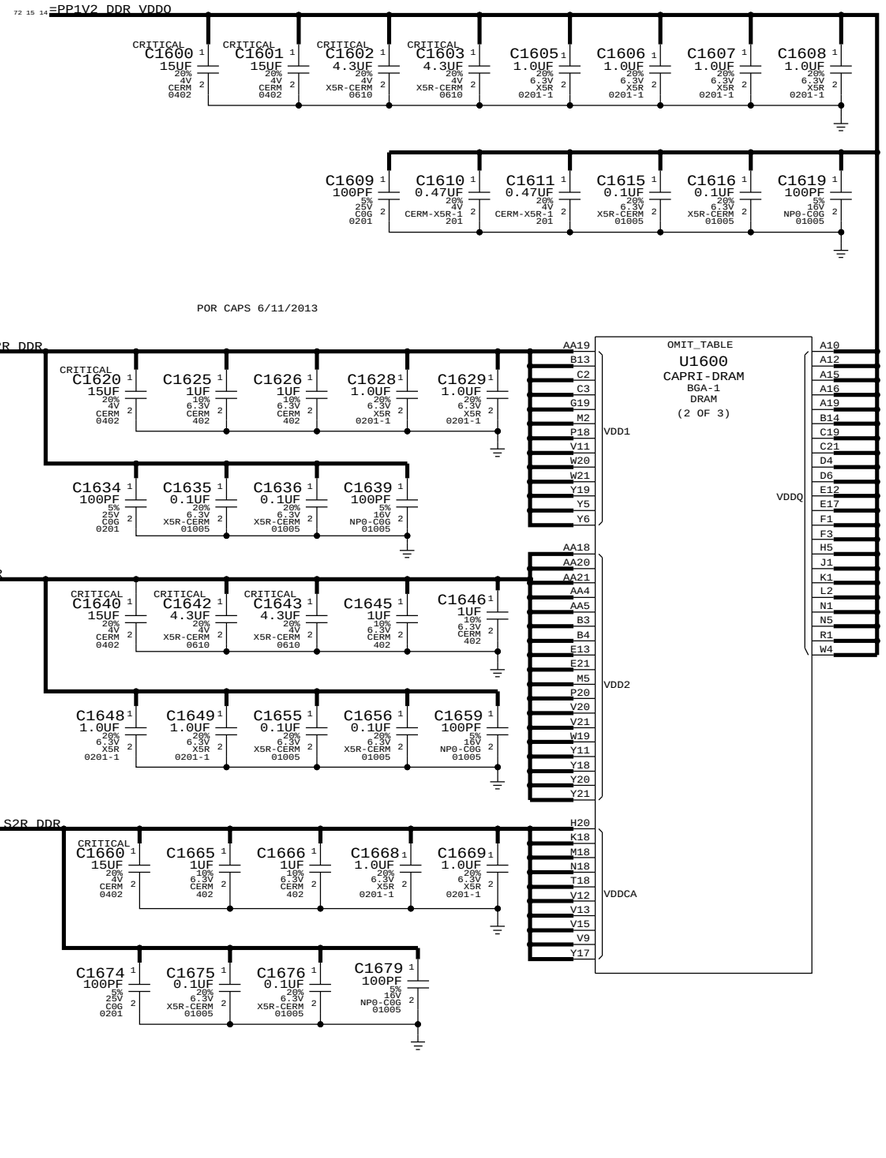
R1699 240 1% 1/32W MF 01005
DDR0 AND DDR1 WERE SWAPPED INTENTIONALLY FOR ROUTING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C1601 15UF 20% 4V CERM 0402
C1602 4.3UF 20% 4V X5R-CERM 0610
C1603 4.3UF 20% 4V X5R-CERM 0610
C1605 1.0UF 20% 6.3V X5R 0201-1
C1606 1.0UF 20% 6.3V X5R 0201-1
C1607 1.0UF 20% 6.3V X5R 0201-1
C1608 1.0UF 20% 6.3V X5R 0201-1
C1609 100PF 5% 25V C0G 0201
C1610 0.47UF 20% 4V CERM-X5R-1 201
C1611 0.47UF 20% 4V CERM-X5R-1 201
C1615 0.1UF 20% 6.3V X5R-CERM 01005
C1616 0.1UF 20% 6.3V X5R-CERM 01005
C1619 100PF 5% 16V NP0-C0G 01005
POR CAPS 6/11/2013
=PP1V8_S2R_DDR
C1620 15UF 20% 4V CERM 0402
C1625 1UF 10% 6.3V CERM 402
C1626 1UF 10% 6.3V CERM 402
C1628 1.0UF 20% 6.3V X5R 0201-1
C1629 1.0UF 20% 6.3V X5R 0201-1
C1634 100PF 5% 25V C0G 0201
C1635 0.1UF 20% 6.3V X5R-CERM 01005
C1636 0.1UF 20% 6.3V X5R-CERM 01005
C1639 100PF 5% 16V NP0-C0G 01005
AA19 B13 C2 C3 G19 M2 P18 V11 W20 W21 Y19 Y5 Y6
VDD1
OMIT_TABLE
U1600
CAPRI-DRAM
BGA-1
DRAM
(2 OF 3)
A10 A12 A15 A16 A19 B14 C19 C21 D4 D6 E12 E17 F1 F3 H5 J1 K1 L2 N1 N5 R1 W4
VDDQ
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C1642 4.3UF 20% 4V X5R-CERM 0610
C1643 4.3UF 20% 4V X5R-CERM 0610
C1645 1UF 10% 6.3V CERM 402
C1646 1UF 10% 6.3V CERM 402
C1648 1.0UF 20% 6.3V X5R 0201-1
C1649 1.0UF 20% 6.3V X5R 0201-1
C1655 0.1UF 20% 6.3V X5R-CERM 01005
C1656 0.1UF 20% 6.3V X5R-CERM 01005
C1659 100PF 5% 16V NP0-C0G 01005
AA18 AA20 AA21 AA4 AA5 B3 B4 E13 E21 M5 P20 V20 V21 W19 Y11 Y18 Y20 Y21
VDD2
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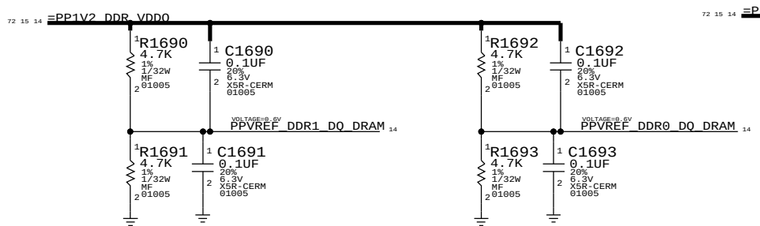
C1665 1UF 10% 6.3V CERM 402
C1666 1UF 10% 6.3V CERM 402
C1668 1.0UF 20% 6.3V X5R 0201-1
C1669 1.0UF 20% 6.3V X5R 0201-1
C1674 100PF 5% 25V C0G 0201
C1675 0.1UF 20% 6.3V X5R-CERM 01005
C1676 0.1UF 20% 6.3V X5R-CERM 01005
C1679 100PF 5% 16V NP0-C0G 01005
H20 K18 M18 N18 T18 V12 V13 V15 V9 Y17
VDDCA
OMIT_TABLE
U1600
CAPRI-DRAM
BGA-1
DRAM
(3 OF 3)
A1 A18 A2 A20 A21 A3 A4 A5 A6 A8 AA1 AA2 AA3 AA6 AA7 B1 B11 B17 B2 B21 C1 C13 C4 D1 D2 D21 D3 D5 E1 E14 E15 E6 E7 E9 F18 F19
VSS
F20 F21 G1 G18 G20 G21 H2 J20 K5 L5 M20 M3 N20 P2 R20 T5 U1 U20 V18 V19 V5 V6 V7 W1 W18 W5 W6 W7 Y1 Y10 Y12 Y13 Y16 Y2 Y7 Y8
VSS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C1690 0.1UF 20% 6.3V X5R-CERM 01005
R1691 4.7K 1% 1/32W MF 01005
C1691 0.1UF 20% 6.3V X5R-CERM 01005
VOLTAGE=0.6V
PPVREF_DDR1_DQ_DRAM
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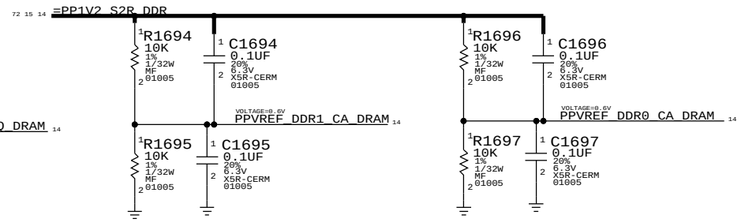
C1692 0.1UF 20% 6.3V X5R-CERM 01005
R1693 4.7K 1% 1/32W MF 01005
C1693 0.1UF 20% 6.3V X5R-CERM 01005
VOLTAGE=0.6V
PPVREF_DDR0_DQ_DRAM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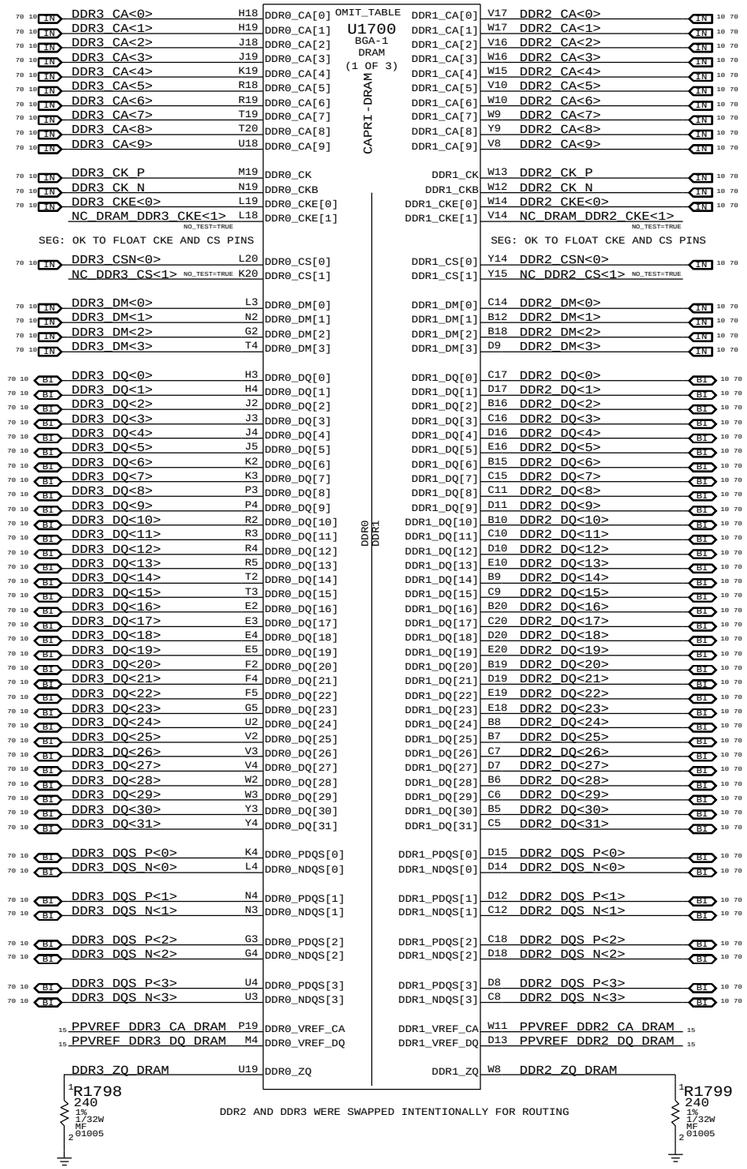
R1695 10K 1% 1/32W MF 01005
C1695 0.1UF 20% 6.3V X5R-CERM 01005
VOLTAGE=0.6V
PPVREF_DDR1_CA_DRAM
R1696 10K 1% 1/32W MF 01005
C1696 0.1UF 20% 6.3V X5R-CERM 01005
R1697 10K 1% 1/32W MF 01005
C1697 0.1UF 20% 6.3V X5R-CERM 01005
VOLTAGE=0.6V
PPVREF_DDR0_CA_DRAM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DDR3_CA<4> K19 DDR0_CA[4]
DDR3_CA<5> R18 DDR0_CA[5]
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DDR3_CA<7> T19 DDR0_CA[7]
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DDR3_CA<9> U18 DDR0_CA[9]
OMIT_TABLE
U1700
BGA-1
DRAM
(1 OF 3)
CAPRI-DRAM
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DDR3_CK_N N19 DDR0_CKB
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NC_DRAM_DDR3_CKE<1> L18 DDR0_CKE[1]
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SEG: OK TO FLOAT CKE AND CS PINS
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NC_DDR3_CS<1> NO_TEST=TRUE K20 DDR0_CS[1]
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DDR3_DQ<21> F4 DDR0_DQ[21]
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PPVREF_DDR3_DQ_DRAM M4 DDR0_VREF_DQ
DDR3_ZQ_DRAM U19 DDR0_ZQ
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DDR1
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DDR1_CA[6] W10 DDR2_CA<6>
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DDR1_CA[8] Y9 DDR2_CA<8>
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DDR1_CKB W12 DDR2_CK_N
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SEG: OK TO FLOAT CKE AND CS PINS
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DDR1_DQ[13] E10 DDR2_DQ<13>
DDR1_DQ[14] B9 DDR2_DQ<14>
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DDR1_DQ[25] B7 DDR2_DQ<25>
DDR1_DQ[26] C7 DDR2_DQ<26>
DDR1_DQ[27] D7 DDR2_DQ<27>
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DDR1_DQ[29] C6 DDR2_DQ<29>
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DDR1_NDQS[2] D18 DDR2_DQS_N<2>
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DDR1_NDQS[3] C8 DDR2_DQS_N<3>
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DDR1_VREF_DQ D13 PPVREF_DDR2_DQ_DRAM
DDR1_ZQ W8 DDR2_ZQ_DRAM
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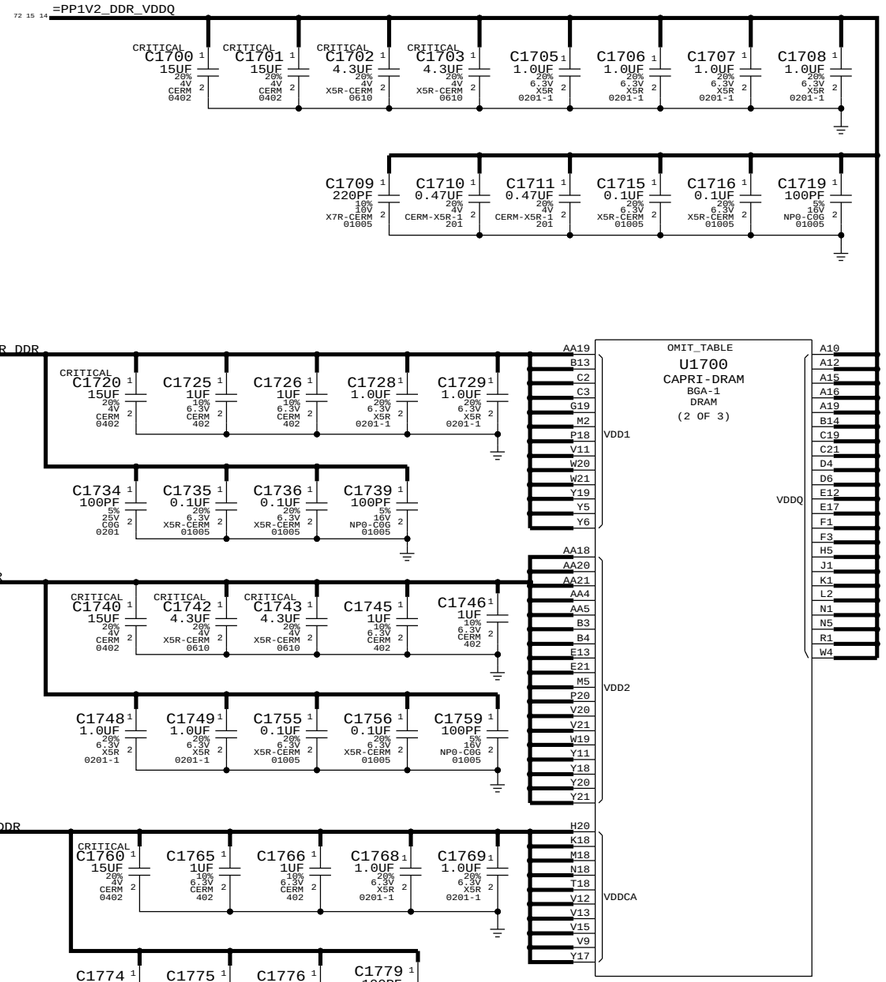
R1799 240 1% 1/32W MF 01005
DDR2 AND DDR3 WERE SWAPPED INTENTIONALLY FOR ROUTING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C1703 4.3UF 20% 4V X5R-CERM 0610
C1705 1.0UF 20% 6.3V X5R 0201-1
C1706 1.0UF 20% 6.3V X5R 0201-1
C1707 1.0UF 20% 6.3V X5R 0201-1
C1708 1.0UF 20% 6.3V X5R 0201-1
C1709 220PF 10% 10V X7R-CERM 01005
C1710 0.47UF 20% 4V CERM-X5R-1 201
C1711 0.47UF 20% 4V CERM-X5R-1 201
C1715 0.1UF 20% 6.3V X5R-CERM 01005
C1716 0.1UF 20% 6.3V X5R-CERM 01005
C1719 100PF 5% 16V NP0-C0G 01005
=PP1V8_S2R_DDR
C1720 15UF 20% 4V CERM 0402
C1725 1UF 10% 6.3V CERM 402
C1726 1UF 10% 6.3V CERM 402
C1728 1.0UF 20% 6.3V X5R 0201-1
C1729 1.0UF 20% 6.3V X5R 0201-1
C1734 100PF 5% 25V C0G 0201
C1735 0.1UF 20% 6.3V X5R-CERM 01005
C1736 0.1UF 20% 6.3V X5R-CERM 01005
C1739 100PF 5% 16V NP0-C0G 01005
VDD1
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C1742 4.3UF 20% 4V X5R-CERM 0610
C1743 4.3UF 20% 4V X5R-CERM 0610
C1745 1UF 10% 6.3V CERM 402
C1746 1UF 10% 6.3V CERM 402
C1748 1.0UF 20% 6.3V X5R 0201-1
C1749 1.0UF 20% 6.3V X5R 0201-1
C1755 0.1UF 20% 6.3V X5R-CERM 01005
C1756 0.1UF 20% 6.3V X5R-CERM 01005
C1759 100PF 5% 16V NP0-C0G 01005
VDD2
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C1765 1UF 10% 6.3V CERM 402
C1766 1UF 10% 6.3V CERM 402
C1768 1.0UF 20% 6.3V X5R 0201-1
C1769 1.0UF 20% 6.3V X5R 0201-1
C1774 100PF 5% 25V C0G 0201
C1775 0.1UF 20% 6.3V X5R-CERM 01005
C1776 0.1UF 20% 6.3V X5R-CERM 01005
C1779 100PF 5% 16V NP0-C0G 01005
VDDCA
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U1700
CAPRI-DRAM
BGA-1
DRAM
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VDDQ
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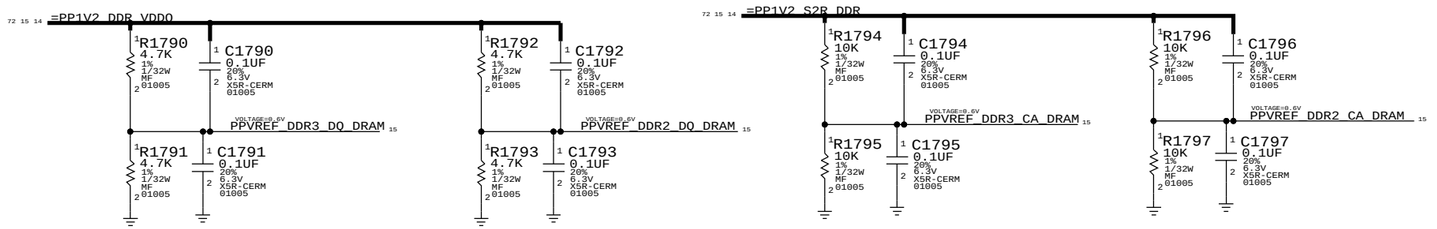
CAPRI-DRAM
BGA-1
DRAM
(3 OF 3)
VSS
VSS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C1790 0.1UF 20% 6.3V X5R-CERM 01005
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C1791 0.1UF 20% 6.3V X5R-CERM 01005
VOLTAGE=0.6V
PPVREF_DDR3_DQ_DRAM
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C1792 0.1UF 20% 6.3V X5R-CERM 01005
R1793 4.7K 1% 1/32W MF 01005
C1793 0.1UF 20% 6.3V X5R-CERM 01005
VOLTAGE=0.6V
PPVREF_DDR2_DQ_DRAM
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C1794 0.1UF 20% 6.3V X5R-CERM 01005
R1795 10K 1% 1/32W MF 01005
C1795 0.1UF 20% 6.3V X5R-CERM 01005
VOLTAGE=0.6V
PPVREF_DDR3_CA_DRAM
R1796 10K 1% 1/32W MF 01005
C1796 0.1UF 20% 6.3V X5R-CERM 01005
R1797 10K 1% 1/32W MF 01005
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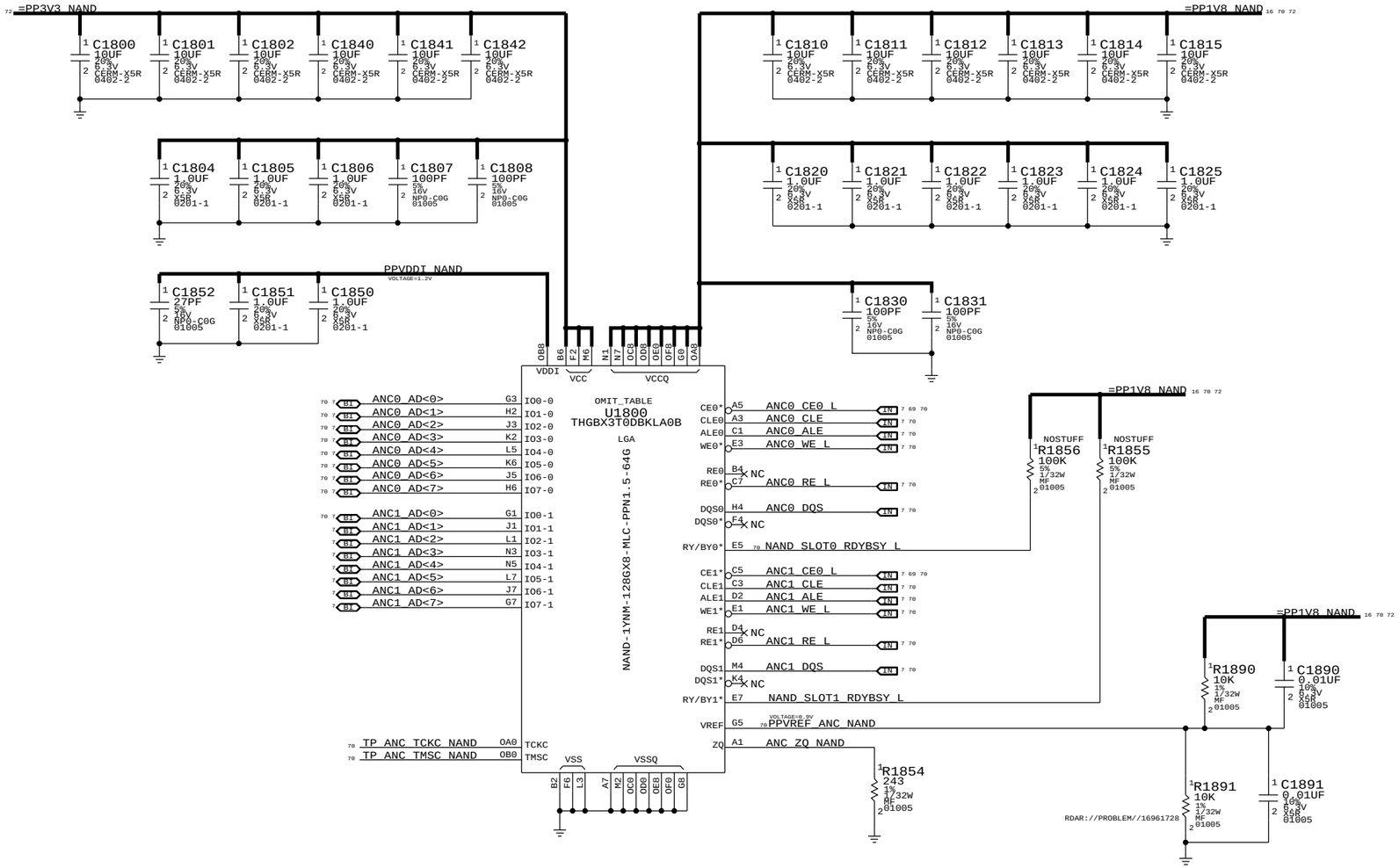
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C1800 10UF 20% 6.3V CERM-X5R 0402-2
C1801 10UF 20% 6.3V CERM-X5R 0402-2
C1802 10UF 20% 6.3V CERM-X5R 0402-2
C1840 10UF 20% 6.3V CERM-X5R 0402-2
C1841 10UF 20% 6.3V CERM-X5R 0402-2
C1842 10UF 20% 6.3V CERM-X5R 0402-2
C1804 1.0UF 20% 6.3V X5R 0201-1
C1805 1.0UF 20% 6.3V X5R 0201-1
C1806 1.0UF 20% 6.3V X5R 0201-1
C1807 100PF 5% 16V NP0-C0G 01005
C1808 100PF 5% 16V NP0-C0G 01005
PPVDDI_NAND
VOLTAGE=1.2V
C1852 27PF 5% 16V NP0-C0G 01005
C1851 1.0UF 20% 6.3V X5R 0201-1
C1850 1.0UF 20% 6.3V X5R 0201-1
=PP1V8_NAND
C1810 10UF 20% 6.3V CERM-X5R 0402-2
C1811 10UF 20% 6.3V CERM-X5R 0402-2
C1812 10UF 20% 6.3V CERM-X5R 0402-2
C1813 10UF 20% 6.3V CERM-X5R 0402-2
C1814 10UF 20% 6.3V CERM-X5R 0402-2
C1815 10UF 20% 6.3V CERM-X5R 0402-2
C1820 1.0UF 20% 6.3V X5R 0201-1
C1821 1.0UF 20% 6.3V X5R 0201-1
C1822 1.0UF 20% 6.3V X5R 0201-1
C1823 1.0UF 20% 6.3V X5R 0201-1
C1824 1.0UF 20% 6.3V X5R 0201-1
C1825 1.0UF 20% 6.3V X5R 0201-1
C1830 100PF 5% 16V NP0-C0G 01005
C1831 100PF 5% 16V NP0-C0G 01005
OMIT_TABLE
U1800
THGBX3T0DBKLA0B
LGA
NAND-1YNM-128GX8-MLC-PPN1.5-64G
VDDI
VCC
VCCQ
VSS
VSSQ
ANC0_AD<0> G3 IO0-0
ANC0_AD<1> H2 IO1-0
ANC0_AD<2> J3 IO2-0
ANC0_AD<3> K2 IO3-0
ANC0_AD<4> L5 IO4-0
ANC0_AD<5> K6 IO5-0
ANC0_AD<6> J5 IO6-0
ANC0_AD<7> H6 IO7-0
ANC1_AD<0> G1 IO0-1
ANC1_AD<1> J1 IO1-1
ANC1_AD<2> L1 IO2-1
ANC1_AD<3> N3 IO3-1
ANC1_AD<4> N5 IO4-1
ANC1_AD<5> L7 IO5-1
ANC1_AD<6> J7 IO6-1
ANC1_AD<7> G7 IO7-1
TP_ANC_TCKC_NAND OA0 TCKC
TP_ANC_TMSC_NAND OB0 TMSC
CE0* A5 ANC0_CE0_L
CLE0 A3 ANC0_CLE
ALE0 C1 ANC0_ALE
WE0* E3 ANC0_WE_L
RE0 B4 NC
RE0* C7 ANC0_RE_L
DQS0 H4 ANC0_DQS
DQS0* F4 NC
RY/BY0* E5 NAND_SLOT0_RDYBSY_L
CE1* C5 ANC1_CE0_L
CLE1 C3 ANC1_CLE
ALE1 D2 ANC1_ALE
WE1* E1 ANC1_WE_L
RE1 D4 NC
RE1* D6 ANC1_RE_L
DQS1 M4 ANC1_DQS
DQS1* K4 NC
RY/BY1* E7 NAND_SLOT1_RDYBSY_L
VREF G5 PPVREF_ANC_NAND
VOLTAGE=0.9V
ZQ A1 ANC_ZQ_NAND
R1854 243 1% 1/32W MF 01005
NOSTUFF R1856 100K 5% 1/32W MF 01005
NOSTUFF R1855 100K 5% 1/32W MF 01005
R1890 10K 1% 1/32W MF 01005
C1890 0.01UF 10% 6.3V X5R 01005
R1891 10K 1% 1/32W MF 01005
C1891 0.01UF 10% 6.3V X5R 01005
RDAR://PROBLEM//16961728

OSCAR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00016	155S0686		FL2000 & MORE	RDAR://PROBLEM/15809407

OSCAR2

APN 337S4534 (A0)

FL2000 120-OHM-25%-250MA-0.5DCR 01005
FL2001 120-OHM-25%-250MA-0.5DCR 01005
C2000 1.0UF 20% 6.3V X5R 0201-1
C2001 1.0UF 20% 6.3V X5R 0201-1
VDDIO CRITICAL
VDDC CRITICAL
U2000 LPC18B1UK/CPA0-00 WLCSP

UART_OSCAR2SOC_TX	C11	U0_TXD/GPIO0[15]	
UART_SOC2OSCAR_TX	A9	U0_RXD/GPIO0[16]	
GPIO_OSCAR2WLAN_CONTEXT_A	E10	U1_RXD/GPIO0[22]	
GPIO_OSCAR2WLAN_CONTEXT_B	F11	U1_TXD/GPIO0[23]	
TP_OSCAR_P0_05	F1	U2_RXD/GPIO0[5]	
TP_OSCAR_P0_06	F3	U2_TXD/GPIO0[6]	
UART_OSCAR2BB_TX	F9	U3_TXD/GPIO0[1]	
UART_BB2OSCAR_TX	F13	U3_RXDGPIO0[2]	
SPI_SENSORS_SCLK	A7	SPI0_SCK/GPIO0[12]	
SPI_SENSORS_MISO	A5	SPI0_MISO/GPIO0[13]	
SPI_SENSORS_MOSI_R	B6	SPI0_MOSI/GPIO0[14]	
SPI_OSCAR2GYRO_CS_L	D9	SPI0_SSEL0/GPIO0[3]	
SPI_OSCAR2PHOS_CS_L	B4	SPI0_SSEL1/GPIO0[18]	
SPI_OSCAR2COMPASS_CS_L	D7	SPI0_SSEL2/GPIO0[4]	
SPI_OSCAR2ACCEL_CS_L	C5	SPI0_SSEL3/GPIO0[25]	
RESET*	F7		

CLKOUT/GPIO0[0]	F5	OSCAR_BIDIR_TIME_SYNC_HOST_IRQ
GPIO0[7]	E4	GPIO_GYRO2OSCAR_IRQ1
GPIO0[8]	D3	GPIO_COMPASS2OSCAR_IRQ
NMI/GPIO0[24]	A13	GPIO_GYRO2OSCAR_IRQ2
GPIO0[26]	A3	GPIO_ACCEL2OSCAR_IRQ1
SWO/GPIO0[27]	A11	GPIO_ACCEL2OSCAR_IRQ2
WDFLAG/GPIO1[2]	D11	TP_OSCAR_P1_02
ALARM1/GPIO1[3]	D5	TP_OSCAR_P1_03
ALARM0/GPIO1[4]	C3	GPIO_OSCAR2PMU_HOST_WAKE
SWDIO/GPIO0[19]	B10	SWD_OSCAR_IO_1V8
SWCLK/GPIO0[20]	B8	SWD_OSCAR_CLK_1V8
CLK32K/GPIO0[21]	E2	TP_OSCAR_P0_21
I2C0_SDAP/GPIO0[10]	B12	I2C_OSCAR2PROX_SDA_1V8
I2C0_SCL/GPIO0[11]	A1	I2C_OSCAR2PROX_SCL_1V8
I2C1_SDA/GPIO0[9]	E6	TP_OSCAR_P0_09
I2C1_SCL/GPIO0[17]	E8	TP_OSCAR_P0_17
I2C2_SDA/GPIO1[0]	C9	GPIO_PROX2OSCAR_IRQ_L
I2C2_SCL/GPIO1[1]	C7	GPIO_OSCAR2COMPASS_TRIGGER

PROX ADDR: 0B0101000X
HELIUM ADDR: 0B1110000X
TEMP ADDR: 0B1110111X

SPI_OSCAR2ACCEL_SCLK R2003 33 1/32W MF 01005 5% PLACE_NEAR=U2000.A7:2MM
SPI_OSCAR2PHOS_SCLK R2002 33 1/32W MF 01005 5% PLACE_NEAR=U2000.A7:2MM
SPI_OSCAR2COMPASS_SCLK R2001 33 1/32W MF 01005 5% PLACE_NEAR=U2000.A7:2MM
SPI_OSCAR2GYRO_SCLK R2000 33 1/32W MF 01005 5% PLACE_NEAR=U2000.A7:3MM
SPI_SENSORS_MOSI R2020 33 1/32W MF 01005 5% PLACE_NEAR=U2000.B6:2MM
SPI_OSCAR2COMPASS_MOSI R2021 33 1/32W MF 01005 5% PLACE_NEAR=U2000.B6:2MM

=PP1V8_S2R_OSCAR
R2010 100K 5% 1/32W MF 01005
CLK_PMU2OSCAR_32K_AND_RESET_L
NOSTUFF C2010 56PF 5% 6.3V NP0-C0G 01005

VSS
D1
C13

SENSORS

GYRO

APN: 338S1192

=PP3V0_S2R_GYRO — R2150 0.00 0% 1/32W MF 01005 — PP3V0_GYRO_FILT (VOLTAGE=3.0V)

C2150 10UF 20% 6.3V CERM-X5R 0402-2

C2155 0.22UF 20% 6.3V X5R 01005-1

C2157 0.22UF 20% 6.3V X5R 01005-1 — =PP1V8_S2R_GYRO

CKPLUS_WAIVE=PWRTERM2GND

U2150 AP3GDL20HAB18TR LGA CRITICAL

SPI_OSCAR2GYRO_CS_L (IN)	5 CS	SCL/SPC 2	SPI_OSCAR2GYRO_SCLK (IN 17)
GPIO_GYRO2OSCAR_IRQ2 (OUT)	6 DRDY/INT2	SDA/SDI/SDO 3	SPI_SENSORS_MOSI (IN 17 18)
	8 DEN	SDO/SA0 4	SPI_GYRO_MISO_R
GPIO_GYRO2OSCAR_IRQ1 (OUT)	7 INT1	RES0 9, RES1 10, RES2 11	
		CAP 14	GYRO_CAP
		VDD 15, VDD_IO 16, GND 13, GND 12	

R2151 33 5% 1/32W MF 01005 — SPI_SENSORS_MISO (OUT 17 18)

CAP APN: 132S0288 — C2152 0.1UF 10% 16V X5R-CERM 0201

ACCEL

=PP1V8_S2R_ACCEL — FL2180 120-OHM-25%-250MA-0.5DCR 01005 — PP1V8_ACCEL_FILT (VOLTAGE=1.8V)

C2180 0.1UF 20% 6.3V X5R-CERM 01005

C2181 0.1UF 20% 6.3V X5R-CERM 01005

U2180 BMA282 LGA CRITICAL

SPI_OSCAR2ACCEL_CS_L (IN 17)	4 CS*	SCX 1	SPI_OSCAR2ACCEL_SCLK (IN 17)
		SDX 2	SPI_SENSORS_MOSI (IN 17 18)
		SDO 3	SPI_ACCEL_MISO_R
GPIO_ACCEL2OSCAR_IRQ1 (OUT 17)	6 INT1	PS 13	
GPIO_ACCEL2OSCAR_IRQ2 (OUT 17)	5 INT2		
		GND 9, 11, 12, 14	GNDIO 10
		VDD 8, VDDIO 7	

R2180 33 5% 1/32W MF 01005 — SPI_SENSORS_MISO (OUT 17 18)

PHOSPHORUS

APN: 338S00044

=PP1V8_S2R_PHOS — FL2120 120-OHM-25%-250MA-0.5DCR 01005 — PP1V8_PHOS_FILT (VOLTAGE=1.8V)

C2120 0.1UF 20% 6.3V X5R-CERM 01005

C2125 1.0UF 20% 6.3V X5R 0201-1

U2120 BMP282BC LGA CRITICAL

SPI_OSCAR2PHOS_SCLK (IN 17)	1 SCK	SDI 3	SPI_SENSORS_MOSI (IN 17 18)
SPI_OSCAR2PHOS_CS_L (IN 17)	2 CS*	SDO 5	SPI_PHOS_MISO_R
		GND 4, 7	
		VDD 8, VDDIO 6	

R2121 33 5% 1/32W MF 01005

R2122 33 5% 1/32W MF 01005 — SPI_SENSORS_MISO (OUT 17 18)

COMPASS

APN: 338S1014

=PP3V0_S2R_COMPASS — FL2140 120-OHM-25%-250MA-0.5DCR 01005 — PP3V0_COMPASS (VOLTAGE=3.0V)

=PP1V8_S2R_COMPASS — FL2141 120-OHM-25%-250MA-0.5DCR 01005 — PP1V8_COMPASS (VOLTAGE=1.8V)

C2142 1.0UF 20% 6.3V X5R 0201-1

C2140 0.1UF 20% 6.3V X5R-CERM 01005

C2141 0.1UF 20% 6.3V X5R-CERM 01005

GND_COMPASS

U2140 AK8963C CSP CRITICAL

	D1 CAD0	SCL/SK A3	SPI_OSCAR2COMPASS_SCLK_R
	D2 CAD1	SDA/SI A4	SPI_OSCAR2COMPASS_MOSI (IN 17)
	NC C2 TST1	CSB* A2	SPI_OSCAR2COMPASS_CS_L (IN 17)
	NC B3 RSV	SO B4	SPI_COMPASS_MISO_R
GPIO_OSCAR2COMPASS_TRIGGER (IN 17)	C3 TRG	DRDY A1	GPIO_COMPASS2OSCAR_IRQ (OUT 17)
PP1V8_COMPASS (69 18)	D4 RST*	VSS C1	XW2140 SHORT-10L-0.25MM-SM
		VDD B1, VID C4	

R2141 33 5% 1/32W MF 01005 — SPI_OSCAR2COMPASS_SCLK (IN 17)

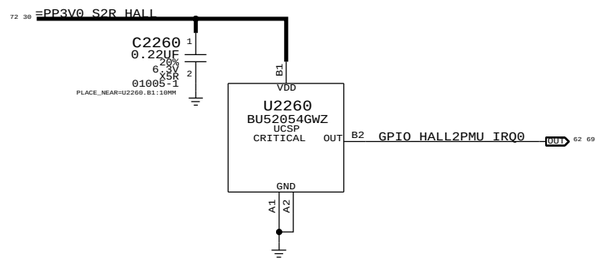
R2142 33 5% 1/32W MF 01005 — SPI_SENSORS_MISO (OUT 17 18)

GND_COMPASS (VOLTAGE=0V)

HALL EFFECT

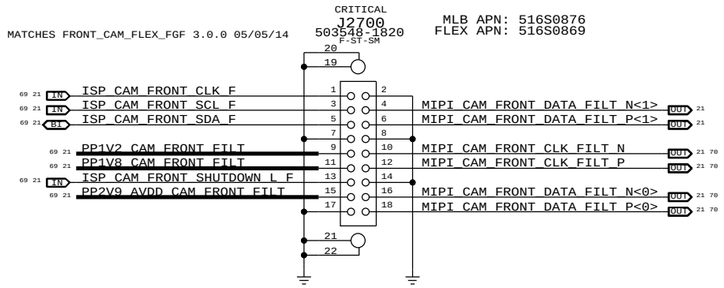
HALL EFFECT

APN 353S3687

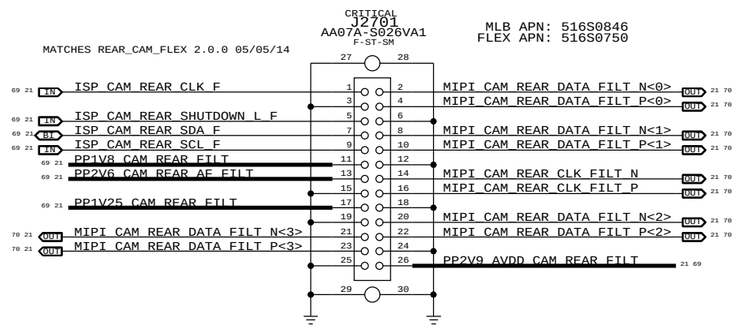


FRONT & REAR CAMERA CONNECTORS

FRONT CAMERA CONNECTOR



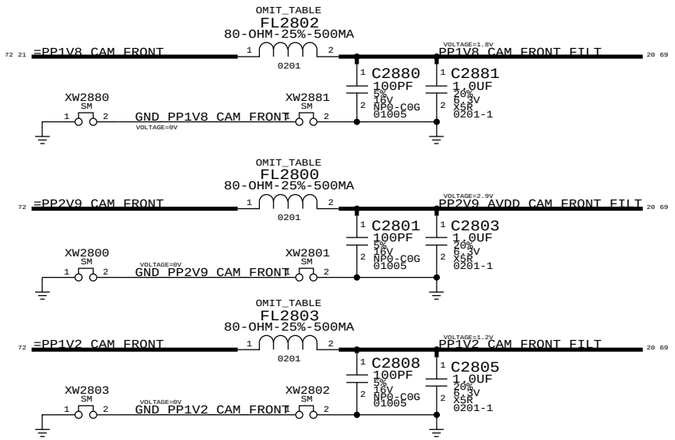
REAR CAMERA CONNECTOR

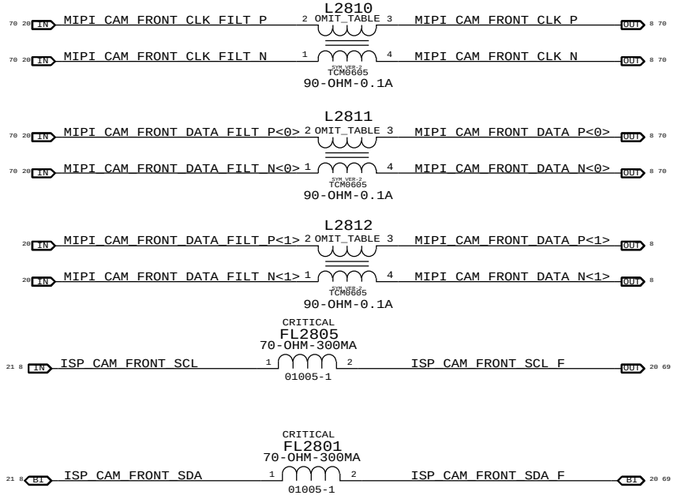


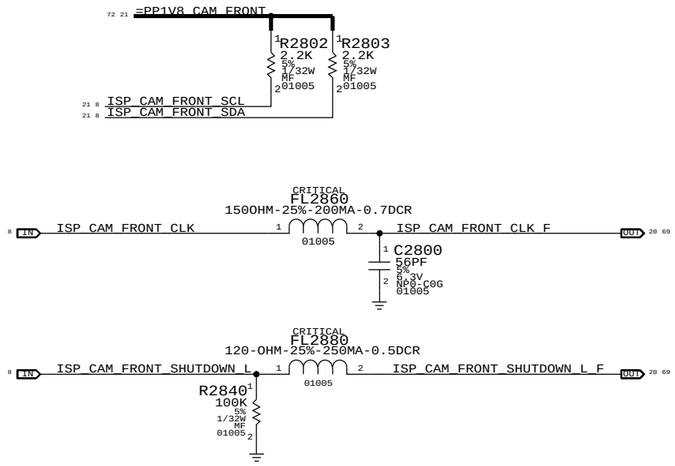
FRONT CAMERA SUPPORT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S00018	7	FERRITE,80OHM,25%,500MA,0.18DCR	FL2800,FL2802,FL2803,FL2861,FL2871,FL2881,FL2891	CRITICAL	
155S00667	8	COMMON MODE CHOKE,90OHM,100MA	L2810,L2811,L2812,L2852,L2853,L2854,L2855,L2856	CRITICAL	

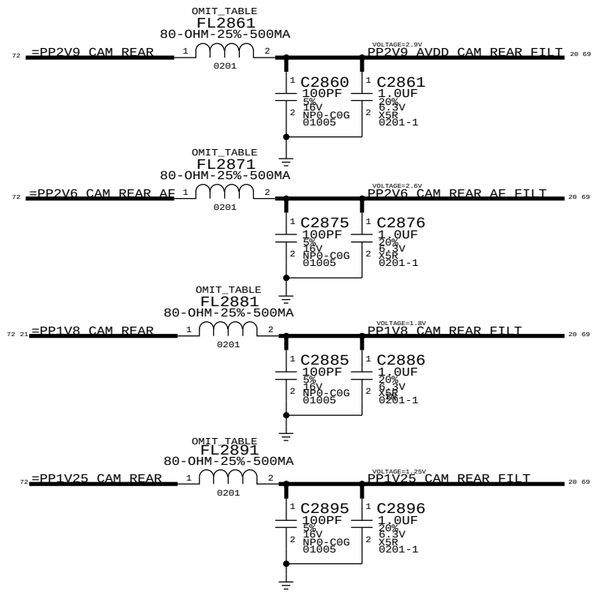
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0885	155S0610	?	FL2860, ECT	RDAR://PROBLEM/128S0271

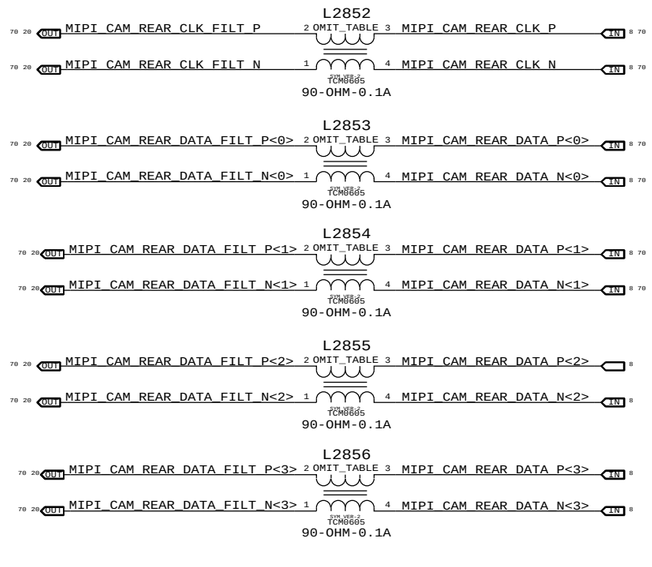


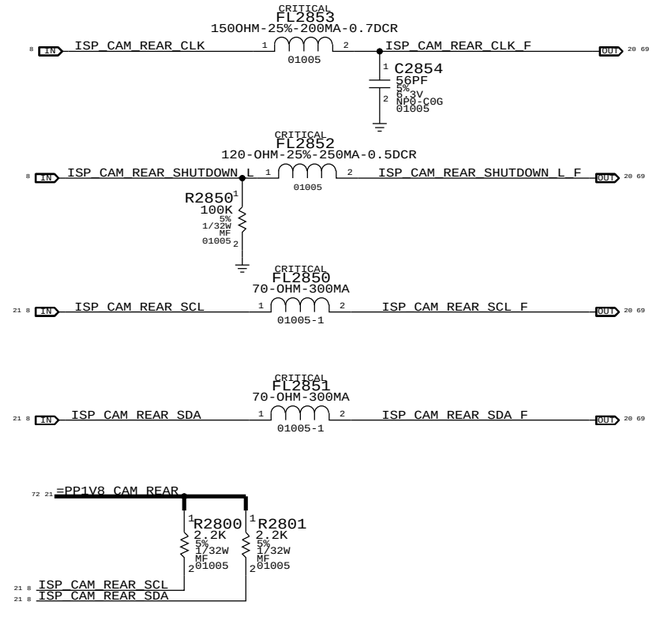




REAR CAMERA SUPPORT







PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S1213	338S1116		U3000	RDAR://PROBLEM/13394605
155S0661	155S0511			RDAR://PROBLEM/12639854

L3000,L3001,L3002,L3003,L3004,L3005

MIKEY BUS FILTER

R3030 12 5% 1/20W MF 201 — PLACE_NEAR=U3000.J4:10MM
R3031 12 5% 1/20W MF 201 — PLACE_NEAR=U3000.K4:10MM
C3030 100PF 5% 16V NP0-C0G 01005
C3031 100PF 5% 16V NP0-C0G 01005 NOSTUFF
C3032 100PF 5% 16V NP0-C0G 01005

=PPVCC_MAIN_AUDIO
=PP1V8_AUDIO
=PP1V7_VA_VCP
GND_AUDIO_CODEC

C3002 0.1UF 20% 6.3V X5R-CERM 01005 — PLACE_NEAR=U3000.A9:5MM
C3015 0.1UF 20% 6.3V X5R-CERM 01005 — PLACE_NEAR=U3000.A8:5MM
C3004 0.1UF 10% 6.3V CERM-X5R 0201
C3040 CRITICAL 10UF 20% 6.3V X5R 0402-10
C3041 CRITICAL 10UF 20% 6.3V X5R 0402-10
C3042 CRITICAL 10UF 20% 6.3V X5R 0402-10
C3001 CRITICAL 4.7UF 20% 6.3V X5R 402
C3003 CRITICAL 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=U3000.G1:5MM
C3050 CRITICAL 4.7UF 20% 6.3V X5R 402
C3051 CRITICAL 1.0UF 20% 6.3V X5R 0201-1
C3005 CRITICAL 4.7UF 20% 6.3V X5R 402
C3006 CRITICAL 4.7UF 20% 6.3V X5R 402
R3050 1.00 1% 1/20W MF-LF 0201 — VOLTAGE=1.7V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.15MM
R3051 1.00 1% 1/20W 0201 MF-LF — VOLTAGE=4.2V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.15MM
R3052 255K 1% 1/20W 201 MF — VOLTAGE=4.2V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.15MM
C3014 0.1UF 10% 6.3V CERM-X5R 0201
C3013 0.1UF 10% 6.3V CERM-X5R 0201
PP1V7_VCP
PPVCC_VPROG_CP
PPVCC_VPROG_MB_F
L81_FLYP
L81_FLYC
L81_FLYN

CRITICAL U3000 CS42L81-CWZR-A1 WLCSP SYM 1 OF 2

VA	G1		
VCP0	G8		
VCP1	G9		
VD	A9		
VL	A8		
VP0	E8		
VP1	E9		
VPROG_CP	G10		
VPROG_MB	H1		
+VCP_FILT	H9	L81_PVCP	MIN_LINE_WIDTH=0.30MM, MIN_NECK_WIDTH=0.15MM
GNDCP	J9	GND_AUDIO_CODEC	
-VCP_FILT	K9	L81_NVCP	MIN_NECK_WIDTH=0.15MM, MIN_LINE_WIDTH=0.30MM
FLYP	H10		
FLYC	J10		
FLYN	K10		
AOUT1+	F10	NC_CODEC_AOUT1_P	NO_TEST=TRUE
AOUT1-	F9	NC_CODEC_AOUT1_N	NO_TEST=TRUE
AOUT2+	D10	NC_CODEC_AOUT2_P	NO_TEST=TRUE
AOUT2-	D9	NC_CODEC_AOUT2_N	NO_TEST=TRUE
DP	J4	L81_MBUS_P	22
DN	K4	L81_MBUS_N	22
HPOUTA	J8	CODEC_HP_LEFT	
HPOUTB	K8	CODEC_HP_RIGHT	
HS3	J1	CODEC_HP_HS3	22
HS4	K1	CODEC_HP_HS4	22
HS3_REF	K7	CODEC_HP_HS3_REF	
HS4_REF	J7	CODEC_HP_HS4_REF	
HPDETECT	H8	CODEC_HP_DET	
LINEOUTA	K6	NC_CODEC_LINEOUTA	NO_TEST=TRUE
LINEOUTB	J6	NC_CODEC_LINEOUTB	NO_TEST=TRUE
LINEOUT_REF	H6		
FILT+	E1	L81_FILT	
FILT-	F1		
NC_MIC1_BIAS	H2	MIC1_BIAS	NO_TEST=TRUE
AIN1P	E3	AIN1+	22
AIN1N	E4	AIN1-	22
MIC1_BIAS_FILT	H3	MIC1_BIAS_FILT	22
L81_MIC2_BIAS_IN	J3	MIC2_BIAS_IN	
L81_MIC2_BIAS	G4	MIC2_BIAS	
	K3	MIC2_BIAS_FILT_IN	
L81_MIC2_BIAS_FILT	F3	MIC2_BIAS_FILT	
L81_AIN2_POS	C1	AIN2+	
L81_AIN2_NEG	D1	AIN2-	
NC_MIC3_BIAS	H4	MIC3_BIAS	NO_TEST=TRUE
AIN3P	C3	AIN3+	22 69
AIN3N	C2	AIN3-	22 69
MIC3_BIAS_FILT	G3	MIC3_BIAS_FILT	22
NC_MIC4_BIAS	F4	MIC4_BIAS	NO_TEST=TRUE
AIN4P	D2	AIN4+	22
AIN4N	E2	AIN4-	22
MIC4_BIAS_FILT	F2	MIC4_BIAS_FILT	22
NC_SPEAKER_VQ	C10	SPEAKER_VQ	NO_TEST=TRUE
GNDP	E10		
GNDD	A10		
GNDHS	K2		
GNDHS	J2		
GNDA	G2		

C3007 CRITICAL 4.7UF 20% 6.3V X5R 402
C3008 CRITICAL 4.7UF 20% 6.3V X5R 402
C3010 10UF 20% 6.3V CERM-X5R 0402-2

R3001 2.21K 1% 1/20W MF 201
C3011 CRITICAL 1.0UF 20% 6.3V X5R 0201-1
C3012 CRITICAL 4.7UF 20% 6.3V X5R 402
L81_MIC2_BIAS_FILT_IN

XW3002 SHORT-8L-0.25MM-SM — NO_XNET_CONNECTION=TRUE
CODEC_HP_HS4 — HP_MIC_POS
C3016 0.1UF 10% 6.3V CERM-X5R 0201

XW3003 SHORT-8L-0.25MM-SM — NO_XNET_CONNECTION=TRUE
CODEC_HP_HS3 — HP_MIC_NEG
C3017 0.1UF 10% 6.3V CERM-X5R 0201

NOTE: EXTMIC INPUTS FROM HS3/HS4 MUST USE EXTERNAL SWITCHES FOR RETURN CURRENTS

XW3000 SM — GNDAUDIO_CODEC

L3000 FERR-33-OHM-0.8A-0.09-OHM CRITICAL 0201 — PLACE_NEAR=J3100.3:10MM — CONN_HP_LEFT_FILT — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM
L3001 FERR-33-OHM-0.8A-0.09-OHM CRITICAL 0201 — PLACE_NEAR=J3100.1:10MM — CONN_HP_RIGHT_FILT
L3002 FERR-33-OHM-0.8A-0.09-OHM CRITICAL 0201 — PLACE_NEAR=J3100.14:10MM — CONN_HP_HS3_FILT — MIN_LINE_WIDTH=0.50MM, MIN_NECK_WIDTH=0.20MM
L3003 FERR-33-OHM-0.8A-0.09-OHM CRITICAL 0201 — PLACE_NEAR=J3100.13:10MM — CONN_HP_HS4_FILT
L3004 FERR-33-OHM-0.8A-0.09-OHM CRITICAL 0201 — PLACE_NEAR=J3100.12:10MM — CONN_HP_HS3_REF_FILT
L3005 FERR-33-OHM-0.8A-0.09-OHM CRITICAL 0201 — PLACE_NEAR=J3100.11:10MM — CONN_HP_HS4_REF_FILT

R3020 3.3K 5% 1/32W MF 01005 — CODEC_HP_DET_R
L3020 240-OHM-0.2A-0.8-OHM 0201-2 — CONN_HP_HEADSET_DET_FILT
C3020 4700PF 10% 16V X7R 201 NOSTUFF

TO HEADPHONE JACK

MIKEY_TS_P
MIKEY_TS_N

CODEC_AIN — MAKE_BASE=TRUE — AIN1P, AIN1N, AIN3P, AIN3N, AIN4P, AIN4N
C3090 0.01UF 10% 6.3V X5R 01005

CODEC_MIC_BIAS_FILT — MAKE_BASE=TRUE — MIC1_BIAS_FILT, MIC3_BIAS_FILT, MIC4_BIAS_FILT
C3091 0.01UF 10% 6.3V X5R 01005

DMIC_BTN_SD — R3012 — DMIC_BTN_SD_R
DMIC_BTN_SCLK — R3013 — DMIC_BTN_SCLK_R
DMIC_MIC_SD — R3014 — DMIC_MIC_SD_R
DMIC_MIC_SCLK — R3015 — DMIC_MIC_SCLK_R
22 5% 1/32W MF 01005

R3010 22 5% 1/32W MF 01005 — I2S_CODEC2SOC_ASP_DOUT
R3011 22 5% 1/32W MF 01005 — I2S_CODEC2SOC_XSP_DOUT

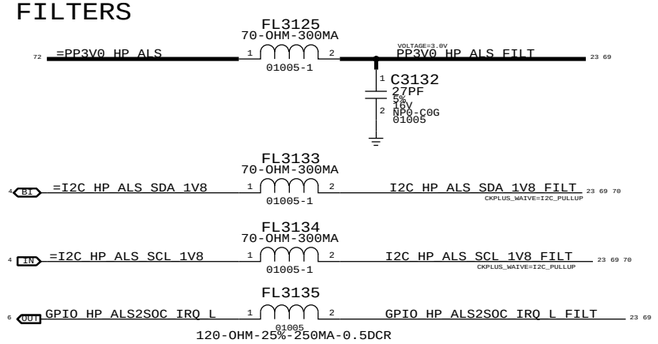
CRITICAL U3000 CS42L81-CWZR-A1 WLCSP SYM 2 OF 2

DMIC1_SD	B1	GND0	C6
DMIC1_SCLK	B2	GND1	D3
		GND2	D5
		GND3	D6
		GND4	D7
		GND5	D8
		GND6	E5
		GND7	E6
		GND8	E7
		GND9	F5
		GND10	F6
DMIC2_SD	B7	GND11	F7
DMIC2_SCLK	B6	GND12	F8
		GND13	G5
		GND14	G6
		GND15	G7
		GND16	H5
		GND17	H7
		GND18	J5
MCLK	C8		
ASP_SCLK	A3		
ASP_LRCK	B3		
ASP_SDIN	A2		
ASP_SDOUT	A1		
XSP_SCLK	B4		
XSP_LRCK_FSYNC	B5		
XSP_SDIN_DAC2_MUTE	A5		
XSP_SDOUT	A4		
MBUS_REF	K5		
CS*	C5		
CCLK	A6		
CDIN	B8		
CDOUT	A7		
INT*	B9	TSTI0	C4
WAKE*	B10	TSTI1	C7
RESET*	C9	TSTI2	D4

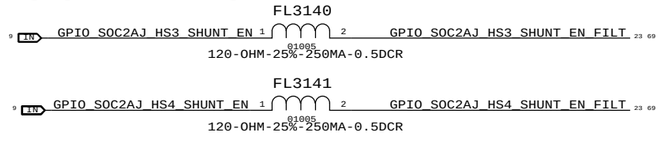
I2S_SOC2CODEC_ASP_MCK
I2S_SOC2CODEC_ASP_BCLK
I2S_SOC2CODEC_ASP_LRCK
I2S_SOC2CODEC_ASP_DOUT
I2S_CODEC2SOC_ASP_DOUT_R
I2S_SOC2CODEC_XSP_BCLK
I2S_SOC2CODEC_XSP_LRCK
I2S_SOC2CODEC_XSP_DOUT
I2S_CODEC2SOC_XSP_DOUT_R
L81_MBUS_REF
SPI_CODEC_CS_L
SPI_CODEC_SCLK
SPI_CODEC_MOSI
SPI_CODEC_MISO
GPIO_CODEC2SOC_IRQ_L
GPIO_CODEC2PMU_HS_IRQ_L
GPIO_PMU2CODEC_RESET_L

AUDIO JACK AND DMIC CONN

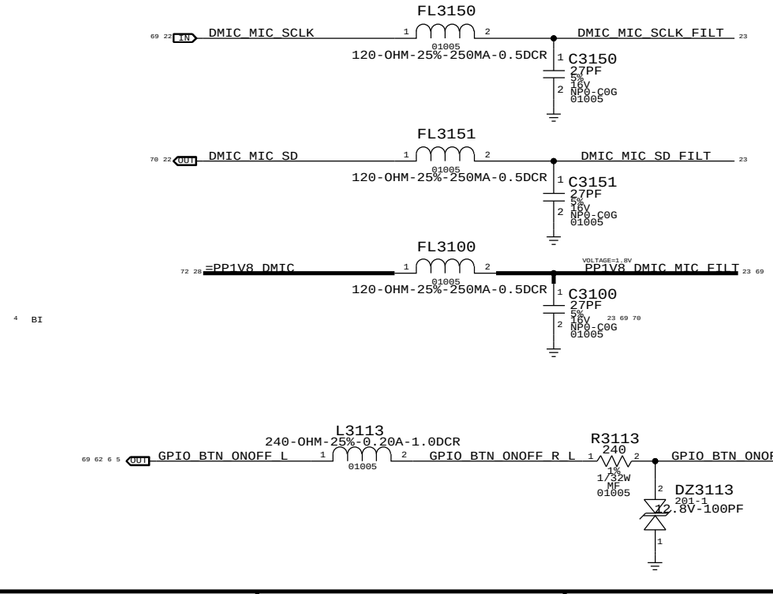
ALS FILTERS



SHUNT FILTERS

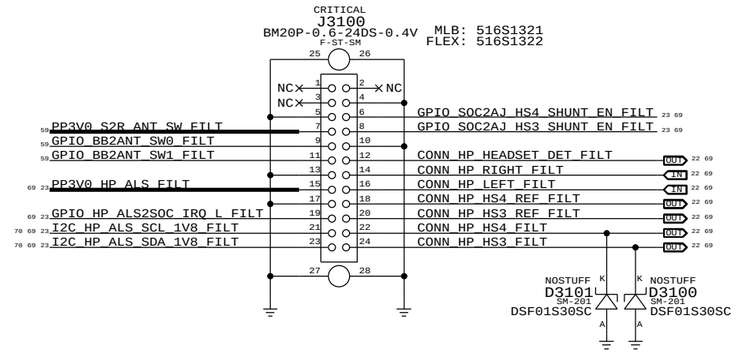


DMIC FILTERS

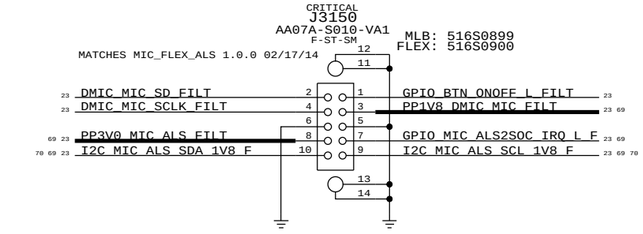


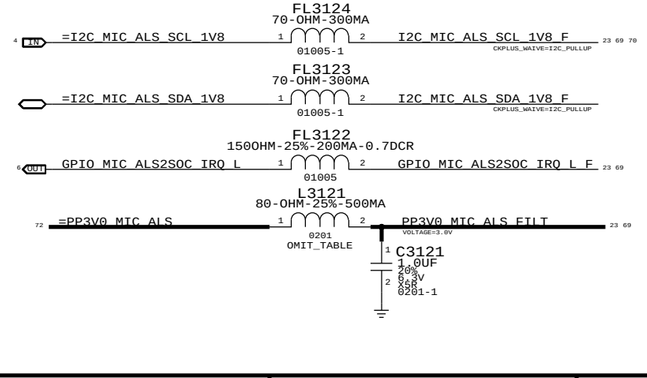
AUDIO JACK B2B CONNECTOR

MATCHES ALS_AUDIO_JACK_FLEX 2.1.0 02/18/14



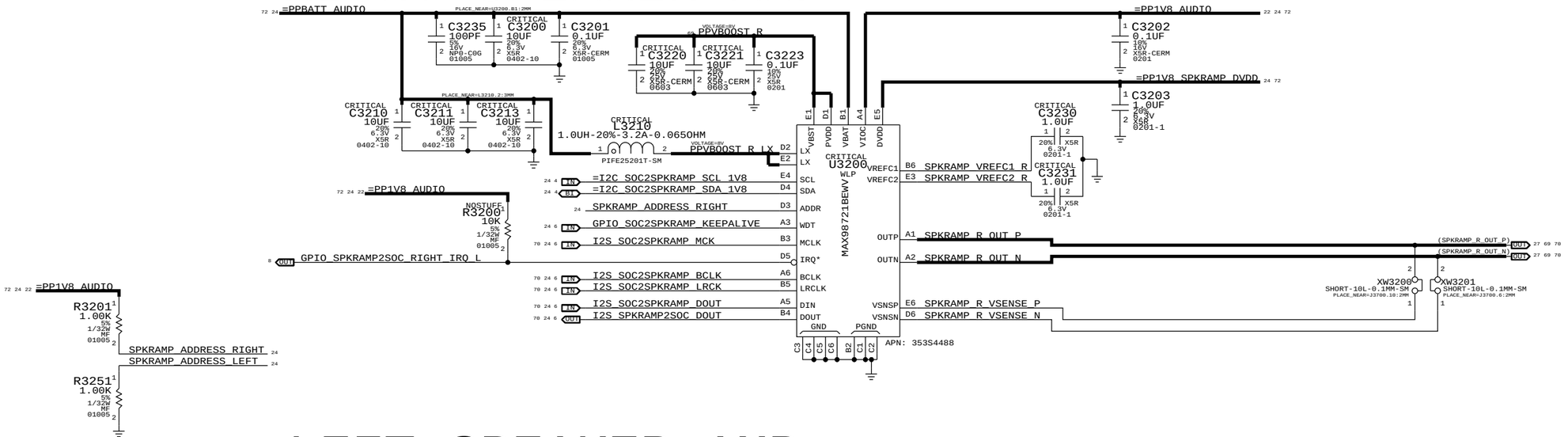
MIC FLEX CONNECTOR



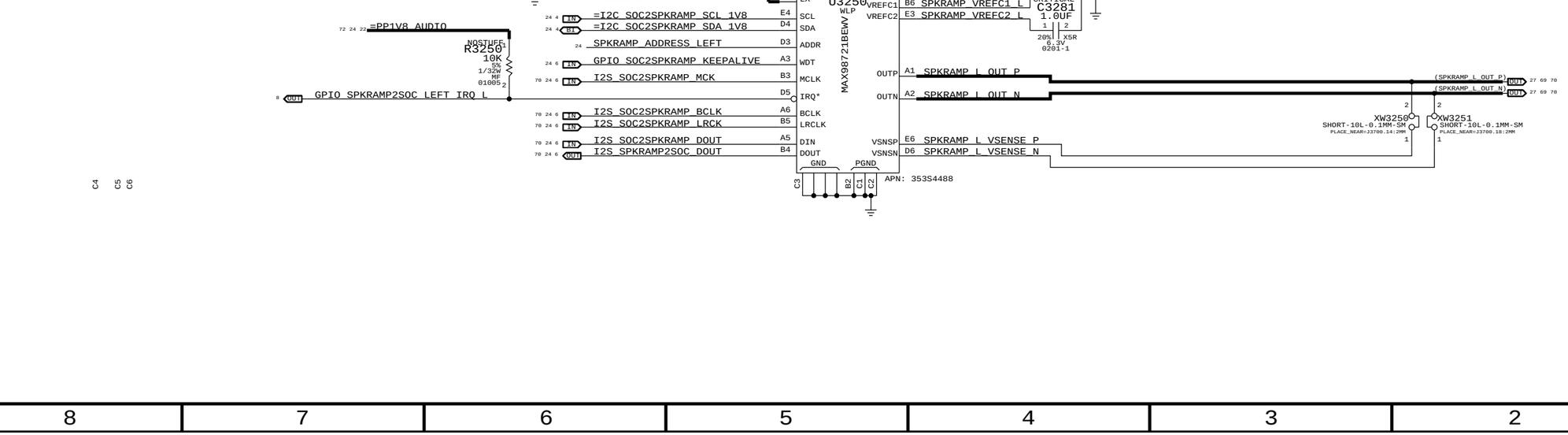


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S00018	1	FERRITE,80OHM,25%,500MA,0.18DCR	L3121	CRITICAL	

RIGHT SPEAKER AMP



LEFT SPEAKER AMP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0667	2	COMMON MODE CHOKE,90OHM,100MA	L3530,L3531	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0155	377S0104	?		RDAR://PROBLEM/12840267

DZ3500,DZ3501,DZ3502,DZ3503,DZ3590

=PP3V0_S2R_TRISTAR
C3530 1.0UF 20% 6.3V X5R 0201-1
C3535 0.22UF 20% 6.3V X5R 0201
C3540 15PF 5% 16V NP0-C0G-CERM 01005
=PP3V3_ACC
C3542 15PF 5% 16V NP0-C0G-CERM 01005
C3532 0.22UF 20% 6.3V X5R 0204
=PP1V8_S2R_TRISTAR
C3531 0.22UF 20% 6.3V X5R 0201
C3541 15PF 5% 16V NP0-C0G-CERM 01005
VOLTAGE=15V
PPVBUS_PROT
C3543 8.2PF +/-0.5PF 50V C0G-CERM 201
C3534 1UF 10% 25V X5R 402
C3545 1UF 10% 25V X5R 402

U3500
CBTL1610A1UK
WLCSP
CRITICAL

MIKEY_TS_P	C3	DIG_DP	P_IN F6
MIKEY_TS_N	C4	DIG_DN	ACC1 C5 PPOUT_E75_ACC_ID1
USB_BB_P	A1	USB1_DP	ACC2 E5 PPOUT_E75_ACC_ID2
USB_BB_N	B1	USB1_DN	DP1 A2 E75_DPAIR1_P
PMU_USB_BRICKID	C2	BRICK_ID	DN1 B2 E75_DPAIR1_N
USB_SOC_P	A3	USB0_DP	DP2 A4 E75_DPAIR2_P
USB_SOC_N	B3	USB0_DN	DN2 B4 E75_DPAIR2_N
		CON_DET_L	E3 TS_E75_ACC_DET_L
UART_SOC2ACC_TX	E2	UART0_TX	
UART_ACC2SOC_TX	E1	UART0_RX	POW_GATE_EN* D6 OVP_SW_EN_L OUT
UART_SOC2DEBUG_TX	F2	UART1_TX	SWITCH_EN E4 RESET_SOC_L IN
UART_DEBUG2SOC_TX	F1	UART1_RX	HOST_RESET B6 GPIO_TS2PMU_RESET OUT
UART_BB2SOC_TX	D2	UART2_TX	SDA D3 =I2C_SOC2TRISTAR_SDA_1V8 OUT
UART_SOC2BB_TX	D1	UART2_RX	SCL D4 =I2C_SOC2TRISTAR_SCL_1V8 IN
JTAG_SOC_TCK_R	A5	JTAG_CLK	INT C6 GPIO_TS2SOC2PMU_IRQ OUT
JTAG_SOC_TMS_R	B5	JTAG_DIO	BYPASS E6 BYPASS_TS
		DVSS F5	
		DVSS C1	
		DVSS A6	
		VDD_1V8 F3	
		VDD_3V0 F4	
		ACC_PWR D5	

ACCESSORY USB
ACCESSORY UART
TRISTAR TX IS AN INPUT AND ITS RX IS AN OUT
SOC DEBUG UART
BB DEBUG UART (T'S OFF TO SOC UART)

C3533 1.0UF 20% 6.3V X5R 0201-1

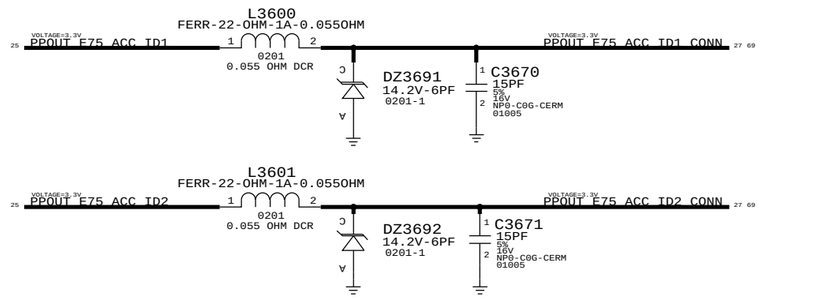
JTAG_SOC_TCK
R3530 0.00 0% 1/32W MF 01005
PLACE_NEAR=U3500.A5:5MM
JTAG_SOC_TMS
R3531 0.00 0% 1/32W MF 01005
PLACE_NEAR=U3500.B5:5MM

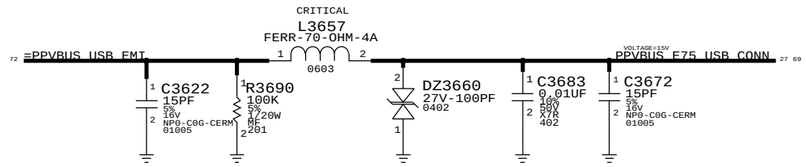
XW3500 SHORT-10L-0.25MM-SM
L81_MBUS_REF
PLACE_NEAR=U3500.F5:5MM

OMIT_TABLE
L3530 90-OHM-0.1A TCM0605
E75_DPAIR1_CONN_P
E75_DPAIR1_CONN_N
CRITICAL DZ3500 ESD0P2RF-02LS TSSLP-2-1 0.4PF
CRITICAL DZ3501 ESD0P2RF-02LS TSSLP-2-1 0.4PF

OMIT_TABLE
L3531 90-OHM-0.1A TCM0605
E75_DPAIR2_CONN_P
E75_DPAIR2_CONN_N
CRITICAL DZ3502 ESD0P2RF-02LS TSSLP-2-1 0.4PF
CRITICAL DZ3503 ESD0P2RF-02LS TSSLP-2-1 0.4PF

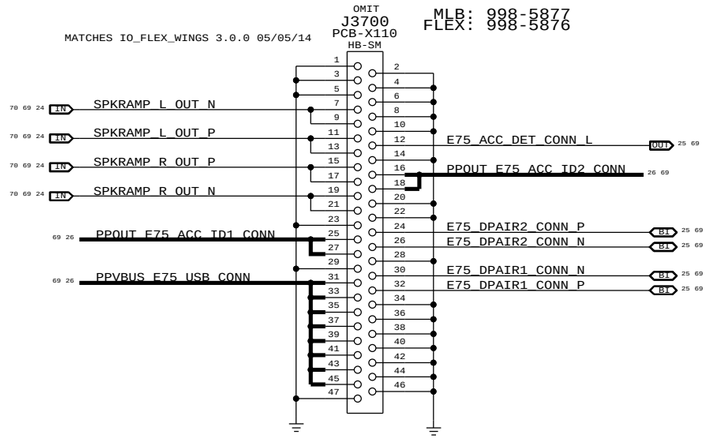
R3590 10K 5% 1/32W MF 01005
E75_ACC_DET_R_L
FL3590 120-OHM-25%-250MA-0.5DCR 01005
E75_ACC_DET_CONN_L
CRITICAL D3591L SM-201 DSF01S30SC
NOSTUFF C3590 15PF 5% 16V NP0-C0G-CERM 01005
CRITICAL DZ3590 ESD0P2RF-02LS TSSLP-2-1



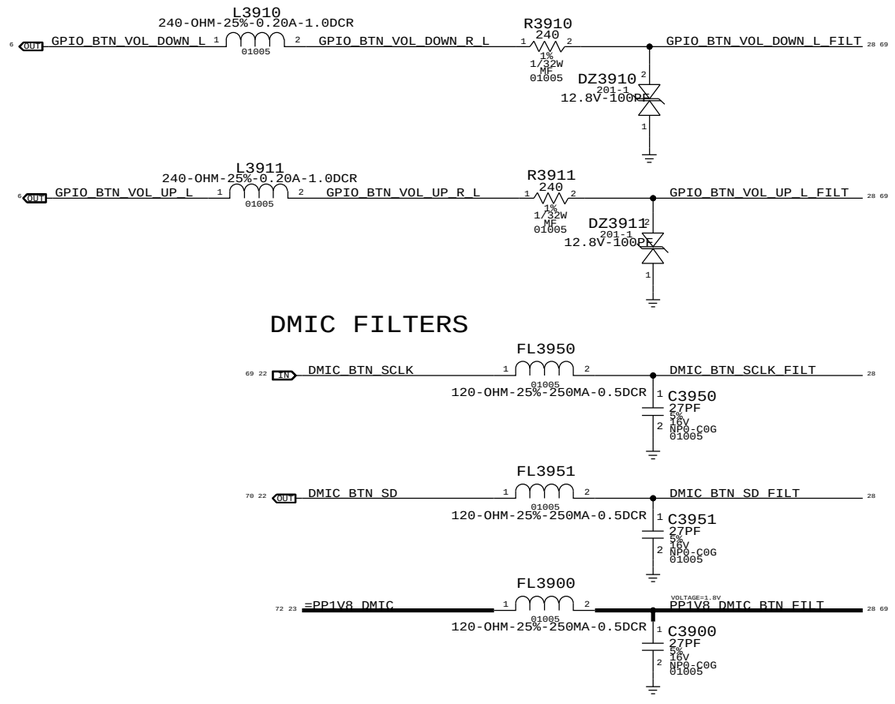


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0116	377S0108		DZ3660	RDAR://PROBLEM/8370432
155S0320	155S0513		L3600,L3601	RDAR://PROBLEM/9625601
155S0741	155S0397		L3657	RDAR://PROBLEM/11238851

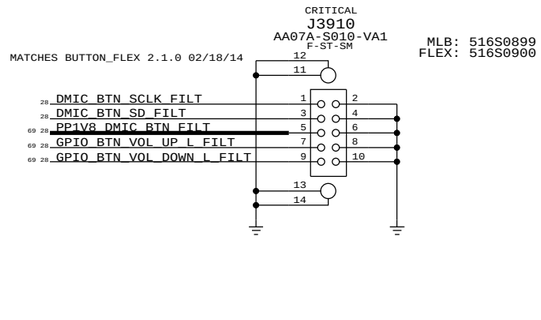
IO FLEX HOTBAR PADS



BUTTON CONNECTOR



DMIC FILTERS



MLB: 516S0899
FLEX: 516S0900

STINGER

CRITICAL
J4020
AA21
F-ST-SM

MATCHES GRAPE_FLEX_ALT3 1.1.0 01/13/14

MLB APN: 516S1070
FLEX APN: 516S1071

MT_PANEL_OUT<39>	3	4	MT_PANEL_OUT<0>	29 70
MT_PANEL_OUT<38>	5	6	MT_PANEL_OUT<1>	29 70
MT_PANEL_OUT<37>	7	8	MT_PANEL_OUT<2>	29 70
MT_PANEL_OUT<36>	9	10	MT_PANEL_OUT<3>	29 70
MT_PANEL_OUT<35>	11	12	MT_PANEL_OUT<4>	29 70
MT_PANEL_OUT<34>	13	14	MT_PANEL_OUT<5>	29 70
MT_PANEL_OUT<33>	15	16	MT_PANEL_OUT<6>	29 70
MT_PANEL_OUT<32>	17	18	MT_PANEL_OUT<7>	29 70
MT_PANEL_OUT<31>	19	20	MT_PANEL_OUT<8>	29 70
MT_PANEL_OUT<30>	21	22	MT_PANEL_OUT<9>	29 70
MT_PANEL_OUT<29>	23	24	MT_PANEL_OUT<10>	29 70
MT_PANEL_OUT<28>	25	26	MT_PANEL_OUT<11>	29 70
MT_PANEL_OUT<27>	27	28	MT_PANEL_OUT<12>	29 70
MT_PANEL_OUT<26>	29	30	MT_PANEL_OUT<13>	29 70
MT_PANEL_OUT<25>	31	32	MT_PANEL_OUT<14>	29 70
MT_PANEL_OUT<24>	33	34	MT_PANEL_OUT<15>	29 70
MT_PANEL_OUT<23>	35	36	MT_PANEL_OUT<16>	29 70
MT_PANEL_OUT<22>	37	38	MT_PANEL_OUT<17>	29 70
MT_PANEL_OUT<21>	39	40	MT_PANEL_OUT<18>	29 70
MT_PANEL_OUT<20>	41	42	MT_PANEL_OUT<19>	29 70

CRITICAL
J4040
AA21-S034VA1
F-ST-SM

MATCHES GRAPE_FLEX_ALT3 1.1.0 01/13/14

MLB APN: 516S1174
FLEX APN: 516S1175

PP3V0_S2R_GRAPE_HALL_FILT	1	2	GPIO_HALL2PMU_IRQ1_FILT	OUT 30 69
	3	4		
MT_PANEL_IN<29>	5	6	MT_PANEL_IN<14>	OUT 30 70
MT_PANEL_IN<28>	7	8	MT_PANEL_IN<13>	OUT 30 70
MT_PANEL_IN<27>	9	10	MT_PANEL_IN<12>	OUT 30 70
MT_PANEL_IN<26>	11	12	MT_PANEL_IN<11>	OUT 30 70
MT_PANEL_IN<25>	13	14	MT_PANEL_IN<10>	OUT 30 70
MT_PANEL_IN<24>	15	16	MT_PANEL_IN<9>	OUT 30 70
MT_PANEL_IN<23>	17	18	MT_PANEL_IN<8>	OUT 30 70
MT_PANEL_IN<22>	19	20	MT_PANEL_IN<7>	OUT 30 70
MT_PANEL_IN<21>	21	22	MT_PANEL_IN<6>	OUT 30 70
MT_PANEL_IN<20>	23	24	MT_PANEL_IN<5>	OUT 30 70
MT_PANEL_IN<19>	25	26	MT_PANEL_IN<4>	OUT 30 70
MT_PANEL_IN<18>	27	28	MT_PANEL_IN<3>	OUT 30 70
MT_PANEL_IN<17>	29	30	MT_PANEL_IN<2>	OUT 30 70
MT_PANEL_IN<16>	31	32	MT_PANEL_IN<1>	OUT 30 70
MT_PANEL_IN<15>	33	34	MT_PANEL_IN<0>	OUT 30 70
	35	36		
	37	38		

=PP5V25_GRAPE
=PPVCC_MAIN_GRAPE
PPVDD_STINGER_BOOST
=PP1V8_GRAPE_EXT_SW

C4016 0.1UF 10% 10V X5R-CERM 0201
C4018 4.7UF 20% 6.3V X5R-CERM1 402
C4019 4.7UF 20% 10V X5R-CERM 0402
C4020 0.1UF 10% 25V X5R 0201
C4021 10UF 20% 25V X5R-CERM 0603
C4022 0.1UF 10% 25V X5R 01005

VBAT N7, N9
VBATDRV
VDDH B6, E6, H7, J5, L5
VDDHV B5, F5, H6, H9, K5, M5
VDDIO J10

CRITICAL
U4003
STINGER
CSP

CUMULUS_VSTM<0>	A2	TXI0	TX00	A3	MT_PANEL_OUT<0>
CUMULUS_VSTM<1>	A4	TXI1	TX01	A5	MT_PANEL_OUT<1>
CUMULUS_VSTM<2>	A7	TXI2	TX02	A6	MT_PANEL_OUT<2>
CUMULUS_VSTM<3>	A9	TXI3	TX03	A8	MT_PANEL_OUT<3>
CUMULUS_VSTM<4>	B1	TXI5	TX04	B2	MT_PANEL_OUT<4>
CUMULUS_VSTM<5>	B3	TXI6	TX05	B4	MT_PANEL_OUT<5>
CUMULUS_VSTM<6>	B8	TXI7	TX06	B7	MT_PANEL_OUT<6>
CUMULUS_VSTM<7>	B10	TXI8	TX07	B9	MT_PANEL_OUT<7>
CUMULUS_VSTM<8>	C1	TXI9	TX08	C2	MT_PANEL_OUT<8>
CUMULUS_VSTM<9>	C3	TXI10	TX09	C4	MT_PANEL_OUT<9>
CUMULUS_VSTM<10>	C8	TXI11	TX010	C7	MT_PANEL_OUT<10>
CUMULUS_VSTM<11>	C10	TXI12	TX011	C9	MT_PANEL_OUT<11>
CUMULUS_VSTM<12>	D1	TXI13	TX012	D2	MT_PANEL_OUT<12>
CUMULUS_VSTM<13>	D3	TXI14	TX013	D4	MT_PANEL_OUT<13>
CUMULUS_VSTM<14>	D5	TXI15	TX014	D6	MT_PANEL_OUT<14>
CUMULUS_VSTM<15>	D8	TXI16	TX015	D7	MT_PANEL_OUT<15>
CUMULUS_VSTM<16>	D10	TXI17	TX016	D9	MT_PANEL_OUT<16>
CUMULUS_VSTM<17>	E1	TXI18	TX017	E2	MT_PANEL_OUT<17>
CUMULUS_VSTM<18>	E3	TXI19	TX018	E4	MT_PANEL_OUT<18>
CUMULUS_VSTM<19>	E8	TXI20	TX019	E7	MT_PANEL_OUT<19>
CUMULUS_VSTM<20>	E10	TXI21	TX020	E9	MT_PANEL_OUT<20>
CUMULUS_VSTM<21>	F1	TXI22	TX021	F2	MT_PANEL_OUT<21>
CUMULUS_VSTM<22>	F3	TXI23	TX022	F4	MT_PANEL_OUT<22>
CUMULUS_VSTM<23>	F8	TXI24	TX023	F7	MT_PANEL_OUT<23>
CUMULUS_VSTM<24>	F10	TXI25	TX024	F9	MT_PANEL_OUT<24>
CUMULUS_VSTM<25>	G1	TXI26	TX025	G2	MT_PANEL_OUT<25>
CUMULUS_VSTM<26>	G3	TXI27	TX026	G4	MT_PANEL_OUT<26>
CUMULUS_VSTM<27>	G5	TXI28	TX027	G6	MT_PANEL_OUT<27>
CUMULUS_VSTM<28>	G8	TXI29	TX028	G7	MT_PANEL_OUT<28>
CUMULUS_VSTM<29>	G10	TXI30	TX029	G9	MT_PANEL_OUT<29>
CUMULUS_VSTM<30>	H1	TXI31	TX030	H2	MT_PANEL_OUT<30>
CUMULUS_VSTM<31>	H3	TXI32	TX031	H4	MT_PANEL_OUT<31>
CUMULUS_VSTM<32>	J1	TXI33	TX032	J2	MT_PANEL_OUT<32>
CUMULUS_VSTM<33>	J3	TXI34	TX033	J4	MT_PANEL_OUT<33>
CUMULUS_VSTM<34>	K1	TXI35	TX034	K2	MT_PANEL_OUT<34>
CUMULUS_VSTM<35>	K3	TXI36	TX035	K4	MT_PANEL_OUT<35>
CUMULUS_VSTM<36>	L1	TXI37	TX036	L2	MT_PANEL_OUT<36>
CUMULUS_VSTM<37>	L3	TXI38	TX037	L4	MT_PANEL_OUT<37>
CUMULUS_VSTM<38>	M1	TXI39	TX038	M2	MT_PANEL_OUT<38>
CUMULUS_VSTM<39>	M3		TX039	M4	MT_PANEL_OUT<39>

R4010 78.7K 1% 1/32W MF 01005
C4012 33000PF 10% 6.3V X5R 201

STINGER_FREQ J6 FREQ
STINGER_SS L7 SS

DIDT=TRUE
SWITCH_MODE=TRUE
STINGER_LX M8, M9, M10 SW

STINGER_COMP M6 COMP
STINGER_FB K10 FBK_IN

I2C_GRAPE_SCL_1V8 N2 SCL
I2C_GRAPE_SDA_1V8 N3 SDA

R4011 3.09K 1% 1/20W MF 201
STINGER_COMP_R
C4013 33000PF 10% 6.3V X5R

AVSS C6, F6, H5, N6
PGND L8, L9, L10
FBK_GND K9
SGND N8
PBKG A1, A10, C5, E5, H8, M7, N1, N10

STINGER_FB
10K 1% 1/32W MF 01005
VOLTAGE=8V
GND_STINGER_FB
R4012 154K 1% 1/32W MF 01005

BOOST INPUT
=PPVCC_MAIN_GRAPE
CRITICAL
L4001 10UH-20%-0.89A-228MOHM VLS4012E-SM
D4001 NSR10F40NXT5G DSN2
VOLTAGE=21.2V
PPVDD_STINGER_BOOST
C4015 10UF 20% 6.3V X5R 0402-10
C4014 10UF 20% 25V X5R-CERM 0603
C4017 10UF 20% 25V X5R-CERM 0603

GAIN0 L6 =PP1V8_GRAPE_EXT_SW
GAIN1 K6
GAIN2 J7
PCTL0 K8
PCTL1 K7
PD* J9 GPIO_GRAPE2STINGER_SHDWN_L
SYNC J8 GPIO_GRAPE2STINGER_SYNC
EN N5 GPIO_GRAPE2STINGER_EN
STEP_CLOCK H10 CLK_GRAPE2STINGER_STEP
RDY/TMUX N4 GPIO_GRAPE2STINGER_RDY

201
R4013

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00018	2	IC,CUMULUS,C1,OPTION1	U4100,U4150	CRITICAL	

=PP1V8_GRAPE_EXT_SW

R4102 4.7K 1% 1/32W MF 01005

R4104 4.7K 1% 1/32W MF 01005

JTAG_CUMULUS_M_TMS

CUMULUS_M_BCFG_RTCK

=PP1V8_GRAPE_EXT_SW

R4152 4.7K 1% 1/32W MF 01005

R4154 4.7K 1% 1/32W MF 01005

JTAG_CUMULUS_S_TMS

CUMULUS_S_BCFG_RTCK

=PP1V8_GRAPE_EXT_SW

R4180 4.7K 1% 1/32W MF 01005

R4181 4.7K 1% 1/32W MF 01005

I2C_GRAPE_SCL_1V8

I2C_GRAPE_SDA_1V8

MASTER CUMULUS

=PP5V25_GRAPE

C4100 1UF 20% 10V X5R 0201

C4101 100PF 5% 16V NP0-C0G 01005

=PP1V8_GRAPE_EXT_SW

C4106 0.1UF 20% 4V X5R 01005

PPVDDCORE_CUMULUS_M VOLTAGE=1.8V

PPVDDANA_CUMULUS_M VOLTAGE=1.8V

C4105 56PF 5% 6.3V NP0-C0G 01005

C4102 2.2UF 20% 4V X5R-CERM 0201

C4103 2.2UF 20% 4V X5R-CERM 0201

C4104 56PF 5% 6.3V NP0-C0G 01005

=PP1V8_GRAPE_EXT_SW

C4108 4.7UF 20% 6.3V X5R-CERM1 402

C4109 0.1UF 20% 4V X5R 01005

C4110 100PF 5% 6.3V CERM 01005

U4100 CUMULUS-C1 WLBGA OMIT_TABLE

MT_PANEL_IN<0>	B9	IN0_0	
MT_PANEL_IN<1>	B8	IN1_0	
MT_PANEL_IN<2>	A9	IN2_0	
MT_PANEL_IN<3>	B7	IN3_0	
MT_PANEL_IN<4>	B6	IN4_0	
MT_PANEL_IN<5>	A8	IN5_0	
MT_PANEL_IN<6>	B5	IN6_0	
MT_PANEL_IN<7>	B4	IN7_0	
MT_PANEL_IN<8>	A7	IN8_0	
MT_PANEL_IN<9>	B3	IN9_0	
MT_PANEL_IN<10>	A6	IN10_0	
MT_PANEL_IN<11>	A3	IN11_0	
MT_PANEL_IN<12>	A5	IN12_0	
MT_PANEL_IN<13>	A4	IN13_0	
MT_PANEL_IN<14>	B2	IN14_0	
NC_CUMULUS_M_IN14_1 (NO_TEST=TRUE)	A2	IN14_1	
SPI_GRAPE_CS_L	E4	H_CS*	
GPIO_GRAPE2SOC_IRQ_L	F1	H_INT*	
SPI_GRAPE_SCLK	D3	H_SCLK	
SPI_GRAPE_MOSI	D2	H_SDI	
SPI_GRAPE_MISO	E1	H_SDO	
TP_JTAG_CUMULUS_M_TCK	C4	JTAG_TCK	
TP_JTAG_CUMULUS_M_TDI	C3	JTAG_TDI	
I2C_GRAPE_SDA_1V8	E2	JTAG_TDO	
JTAG_CUMULUS_M_TMS	C6	JTAG_TMS	
CUMULUS_M_BCFG_RTCK	E3	BCFG_RTCK	
CLK_SOC2GRAPE_32K	D1	CLKIN/RESET*	
	D9	RSTOVR*	

	E9	VSTM_0	CUMULUS_VSTM<0>
	E5	VSTM_1	CUMULUS_VSTM<1>
	F7	VSTM_2	CUMULUS_VSTM<2>
	E6	VSTM_3	CUMULUS_VSTM<3>
	E7	VSTM_4	CUMULUS_VSTM<4>
	F8	VSTM_5	CUMULUS_VSTM<5>
	G9	VSTM_6	CUMULUS_VSTM<6>
	D6	VSTM_7	CUMULUS_VSTM<7>
	D7	VSTM_8	CUMULUS_VSTM<8>
	D8	VSTM_9	CUMULUS_VSTM<9>
	F9	VSTM_10	CUMULUS_VSTM<10>
	D5	VSTM_11	CUMULUS_VSTM<11>
	F6	VSTM_12	CUMULUS_VSTM<12>
	F5	VSTM_13	CUMULUS_VSTM<13>
	G4	VSTM_14	CUMULUS_VSTM<14>
	E8	VSTM_15	CUMULUS_VSTM<15>
	G8	VSTM_16	CUMULUS_VSTM<16>
	G7	VSTM_17	CUMULUS_VSTM<17>
	G6	VSTM_18	CUMULUS_VSTM<18>
	G5	VSTM_19	CUMULUS_VSTM<19>
	G1	GPIO_1/CK	CUMULUS_M2S_CLK
	D4	GPIO_2/SD	CUMULUS_M2S_SDA
	F2	GPIO_3	DISPLAY_SYNC
	F3	GPIO_4	CUMULUS_M_GPIO_4
	C2	TM_ACS*	NC_CUMULUS_M_TM_ACS_L (NO_TEST=TRUE)
	G3	TM_OVR	I2C_GRAPE_SCL_1V8

R4101 4.7K 1% 1/32W MF 01005

GPIO_SOC2GRAPE_RESET_L

R4106 100K 5% 1/32W MF 01005

R4110 4.7K 1% 1/32W MF 01005

GND

C7 C9 G2

SLAVE CUMULUS

=PP5V25_GRAPE

C4150 1UF 20% 10V X5R 0201

=PP1V8_GRAPE_EXT_SW

C4156 0.1UF 20% 4V X5R 01005

PPVDDCORE_CUMULUS_S VOLTAGE=1.8V

PPVDDANA_CUMULUS_S VOLTAGE=1.8V

C4155 56PF 5% 6.3V NP0-C0G 01005

C4152 2.2UF 20% 4V X5R-CERM 0201

C4153 2.2UF 20% 4V X5R-CERM 0201

C4154 56PF 5% 6.3V NP0-C0G 01005

=PP1V8_GRAPE_EXT_SW

C4159 0.1UF 20% 4V X5R 01005

C4158 100PF 5% 6.3V CERM 01005

U4150 CUMULUS-C1 WLBGA OMIT_TABLE

MT_PANEL_IN<15>	B9	IN0_0	
MT_PANEL_IN<16>	B8	IN1_0	
MT_PANEL_IN<17>	A9	IN2_0	
MT_PANEL_IN<18>	B7	IN3_0	
MT_PANEL_IN<19>	B6	IN4_0	
MT_PANEL_IN<20>	A8	IN5_0	
MT_PANEL_IN<21>	B5	IN6_0	
MT_PANEL_IN<22>	B4	IN7_0	
MT_PANEL_IN<23>	A7	IN8_0	
MT_PANEL_IN<24>	B3	IN9_0	
MT_PANEL_IN<25>	A6	IN10_0	
MT_PANEL_IN<26>	A3	IN11_0	
MT_PANEL_IN<27>	A5	IN12_0	
MT_PANEL_IN<28>	A4	IN13_0	
MT_PANEL_IN<29>	B2	IN14_0	
NC_CUMULUS_S_IN14_1 (NO_TEST=TRUE)	A2	IN14_1	
TP_CUMULUS_S_CS_L	E4	H_CS*	
CLK_GRAPE2STINGER_STEP	F1	H_INT*	
GPIO_GRAPE2STINGER_SYNC	D3	H_SCLK	
GPIO_GRAPE2STINGER_RDY	D2	H_SDI	
GPIO_GRAPE2STINGER_EN	E1	H_SDO	
NC_CUMULUS_S_TCK (NO_TEST=TRUE)	C4	JTAG_TCK	
NC_CUMULUS_S_TDI (NO_TEST=TRUE)	C3	JTAG_TDI	
NC_CUMULUS_S_TDO (NO_TEST=TRUE)	E2	JTAG_TDO	
JTAG_CUMULUS_S_TMS	C6	JTAG_TMS	
CUMULUS_S_BCFG_RTCK	E3	BCFG_RTCK	
CLK_SOC2GRAPE_32K	D1	CLKIN/RESET*	
GPIO_SOC2GRAPE_RESET_L	D9	RSTOVR*	

	E9	VSTM_0	CUMULUS_VSTM<20>
	E5	VSTM_1	CUMULUS_VSTM<21>
	F7	VSTM_2	CUMULUS_VSTM<22>
	E6	VSTM_3	CUMULUS_VSTM<23>
	E7	VSTM_4	CUMULUS_VSTM<24>
	F8	VSTM_5	CUMULUS_VSTM<25>
	G9	VSTM_6	CUMULUS_VSTM<26>
	D6	VSTM_7	CUMULUS_VSTM<27>
	D7	VSTM_8	CUMULUS_VSTM<28>
	D8	VSTM_9	CUMULUS_VSTM<29>
	F9	VSTM_10	CUMULUS_VSTM<30>
	D5	VSTM_11	CUMULUS_VSTM<31>
	F6	VSTM_12	CUMULUS_VSTM<32>
	F5	VSTM_13	CUMULUS_VSTM<33>
	G4	VSTM_14	CUMULUS_VSTM<34>
	E8	VSTM_15	CUMULUS_VSTM<35>
	G8	VSTM_16	CUMULUS_VSTM<36>
	G7	VSTM_17	CUMULUS_VSTM<37>
	G6	VSTM_18	CUMULUS_VSTM<38>
	G5	VSTM_19	CUMULUS_VSTM<39>
	G1	GPIO_1/CK	CUMULUS_M2S_CLK
	D4	GPIO_2/SD	CUMULUS_M2S_SDA
	F2	GPIO_3	TP_CUMULUS_S_GPIO_3
	F3	GPIO_4	GPIO_GRAPE2STINGER_SHDWN_L
	C2	TM_ACS*	NC_CUMULUS_S_TM_ACS_L (NO_TEST=TRUE)
	G3	TM_OVR	

R4159 4.7K 1% 1/32W MF 01005

GND

C7 C9 G2

HALL EFFECT

FL4124 240-OHM-25%-0.20A-1.0DCR 01005

GPIO_HALL2PMU_IRQ1

GPIO_HALL2PMU_IRQ1_FILT

FL4125 70-OHM-300MA 01005-1

=PP3V0_S2R_HALL

PP3V0_S2R_GRAPE_HALL_FILT

C4125 27PF 5% 16V NP0-C0G 01005

X5R-CERM

=PP1V8_S2R_GRAPE_EXTERNAL_SW

=PPVCC_MAIN_GRAPE

C4190 0.1UF 10% 16V 0201

C4196 1.0UF 20% 6.3V X5R 0201-1

U4190 SLG5AP1443V TDFN

VCC_MAIN_GRAPE_RAMP

GPIO_SOC2GRAPE_EXT_SW_ON

C4193 4700PF 10% 16V X7R 201

R4194 100K 5% 1/32W MF 01005

C4195 10UF 20% 6.3V X5R 0402-10

PP1V8_GRAPE_EXT_SW

LAYOUT NOTE:
PUT THERMAL VIAS AROUND U4100 IN CASE OF SHORTED CONDITION

DISPLAY CONNECTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
131S00011	131S0641	?	C4550, ECT	RDAR://PROBLEM/15682101

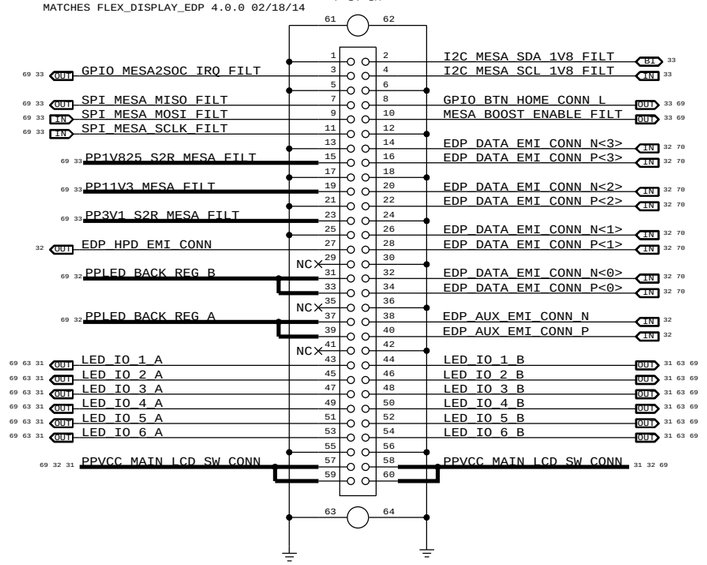
DISPLAY CONNECTOR

CRITICAL

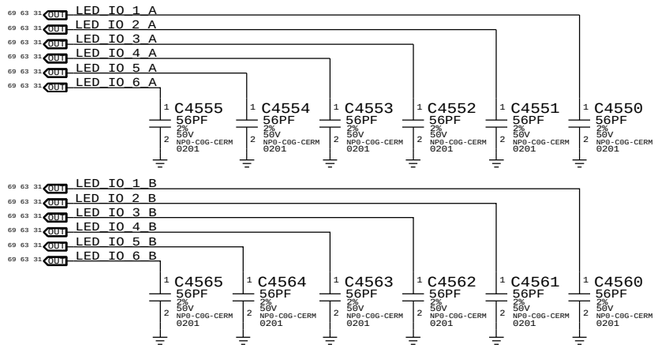
J4500
BM15P1.0-60DS-0.35V
F-ST-SM

MLB APN: 516S1243
FLEX APN: 516S1244

MATCHES FLEX_DISPLAY_EDP 4.0.0 02/18/14

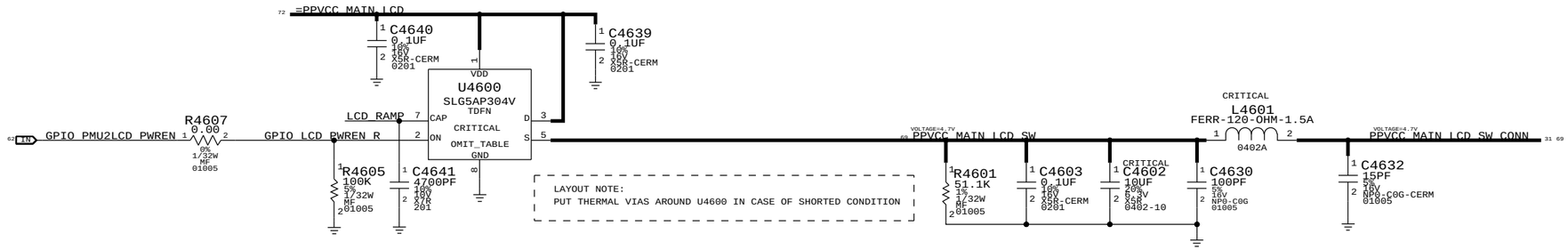


SWAPPED LED STRING A AND B INTENTIONALLY TO EASE ROUTING

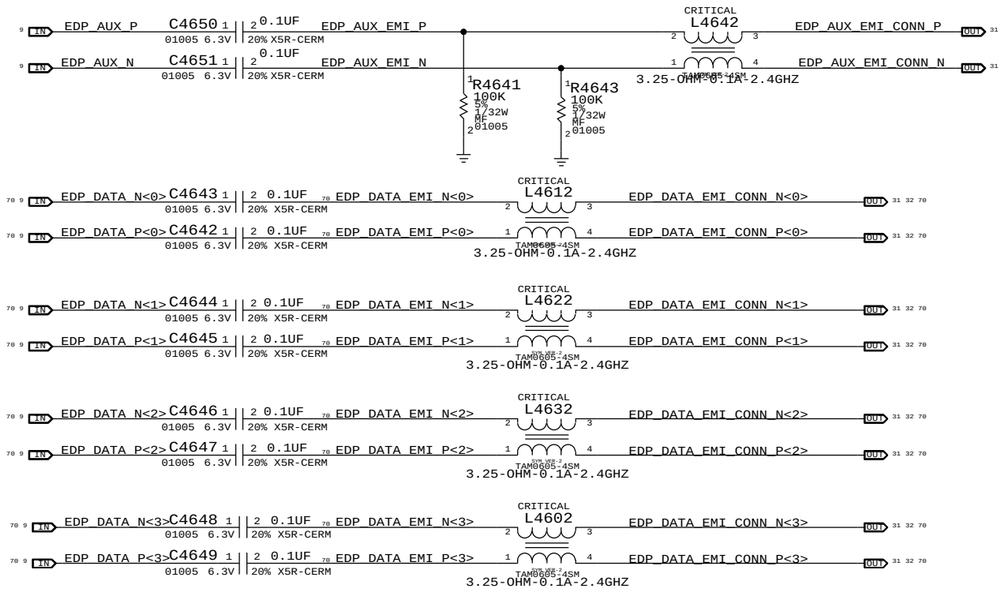


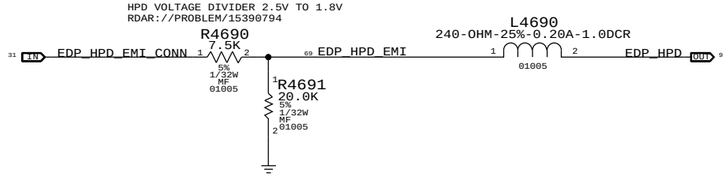
EDP CONNECTOR SUPPORT

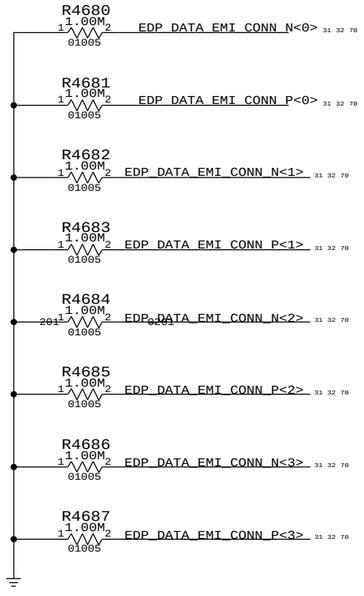
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0914	155S0897	?	L4602, ECT	RDAR://PROBLEM/15954071

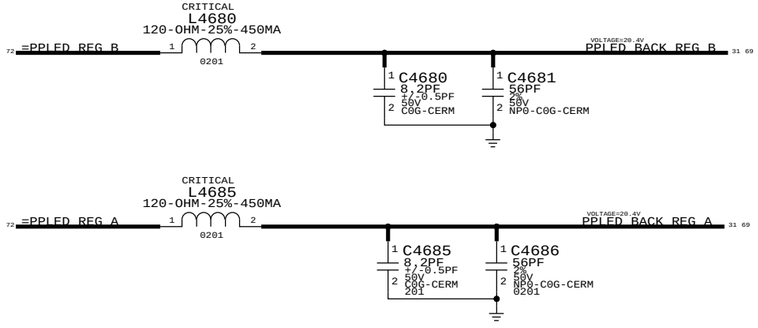


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4272	1	IC,SLG5AP1423V	U4600	CRITICAL	?





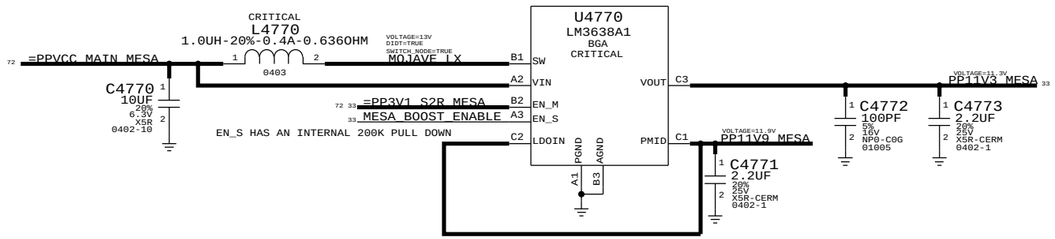


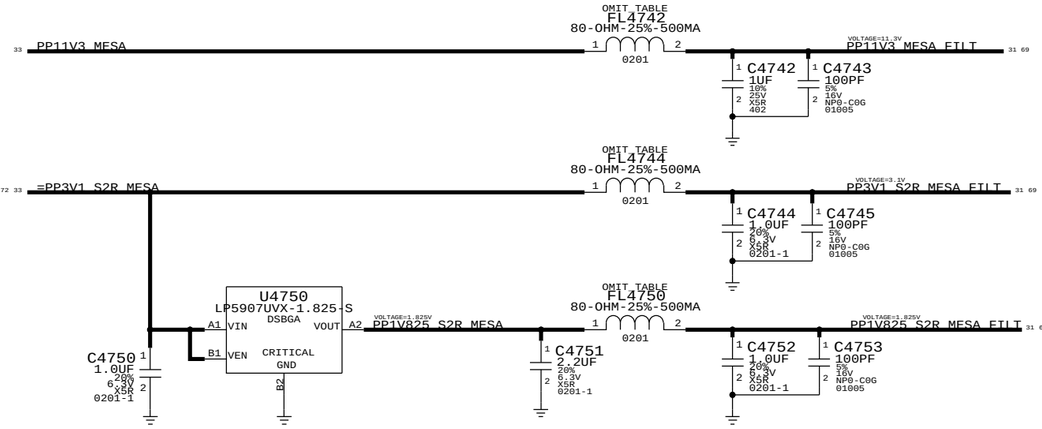


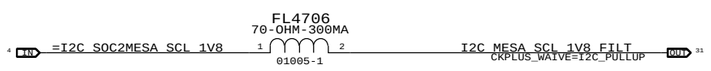
MESA & HOME BUTTON

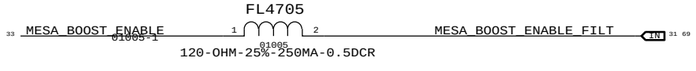
MOJAVE

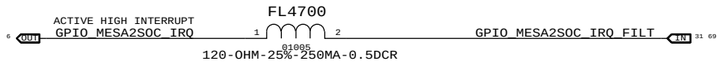
USING A1 BECAUSE NAVAJO NEEDS 11V3

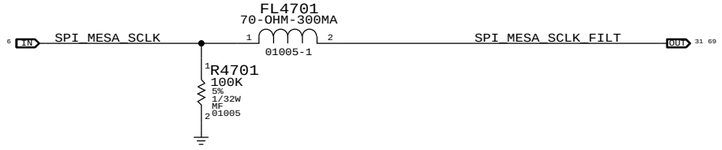




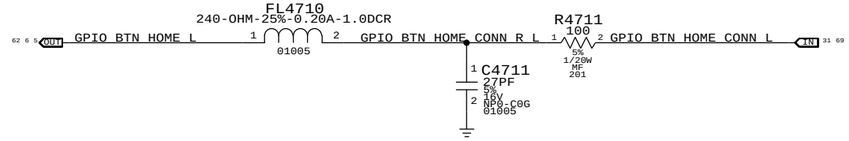








HOME BUTTON FILTERS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S00018	3	FERRITE,800HM,25%,500MA,0.18DCR	FL4742,FL4744,FL4750	CRITICAL	

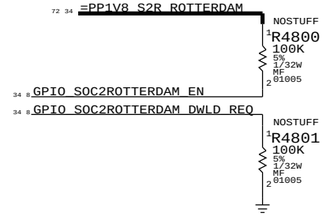
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00017	155S0755			RDAR://PROBLEM/15807137

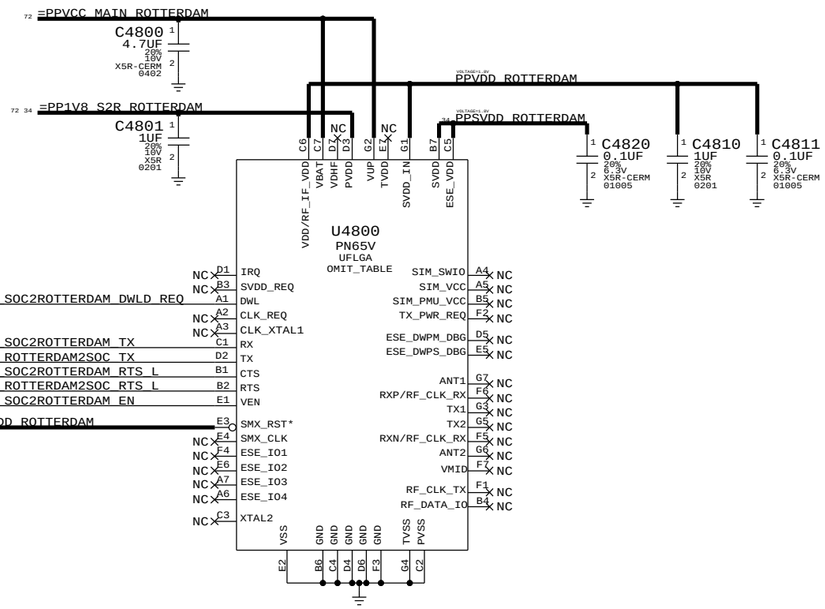
FL3910,FL3911,FL4124,L4690,FL4710

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00018	155S0664			RDAR://PROBLEM/15796569

FL2800,FL2802,FL2803,FL2861,FL2871,FL2881,FL2891,FL4742,FL4744,FL4750,FL7900

J82 - ROTTERDAM





PP4800 P4MM 1 UART_SOC2ROTTERDAM_TX 6 34
PP4801 P4MM 1 UART_ROTTERDAM2SOC_TX 6 34
PP4802 P4MM 1 UART_SOC2ROTTERDAM_RTS_L 6 34
PP4803 P4MM 1 UART_ROTTERDAM2SOC_RTS_L 6 34
PP4804 P4MM 1 GPIO_SOC2ROTTERDAM_EN 8 34
PP4806 P4MM 1 GPIO_SOC2ROTTERDAM_DWLD_REQ 8 34

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00043	1	IC,ROTTERDAM,MP,UFLGA49	U4800	CRITICAL	

AP INTERFACE & DEBUG CONNECTOR

TEST POINTS

TP5000 A 1 TP-PS 50_BB_HSIC_STROBE 39 68
TP5001 A 1 TP-PS 50_BB_HSIC_DATA 39 68
TP5002 A 1 TP-PS BB_DEBUG_ERROR 40
TP5003 A 1 TP-PS PS_HOLD_PMIC 35 37
TP5004 A 1 TP-PS PMIC_RESOUT_L 35 37 39
TP5005 A 1 TP-PS MDM_CLK 37 39
TP5006 A 1 TP-PS PP_LDO11 35 36 38 39 40 42 43 44 73
TP5007 A 1 TP-PS SPMI_DATA 37 39
TP5008 A 1 TP-PS SPMI_CLK 37 39
TP5025 A 1 TP-PS BOUNDARY_SCAN_EN 39 69
TP5021 A 1 TP-PS PP_BATT_VCC 35 44 53 68 73
TP5028 A 1 TP-PS
TP5026 A 1 TP-PS
TP5027 A 1 TP-PS

TP5009 A 1 TP-PS BB_JTAG_RST_L 35 39
TP5010 A 1 TP-PS BB_JTAG_TCK 35 39
TP5011 A 1 TP-PS BB_JTAG_TMS 35 39
TP5012 A 1 TP-PS BB_JTAG_TDO 35 39
TP5013 A 1 TP-PS BB_JTAG_TDI 35 39
TP5014 A 1 TP-PS BB_JTAG_TRST_L 35 39
TP5015 A 1 TP-PS BB_DEBUG_STATUS 40
TP5016 A 1 TP-PS BOOT_HSIC 35 40
TP5017 A 1 TP-PS RFFE1_CLK 35 40 44 45 46 47 48 49
TP5018 A 1 TP-PS RFFE1_DATA 35 40 44 45 46 47 48 49
TP5019 A 1 TP-PS RFFE2_CLK 35 40 50 51 53
TP5020 A 1 TP-PS RFFE2_DATA 35 40 50 51 53
TP5031 A 1 TP-PS 90_BBUSB_N 35 39
TP5030 A 1 TP-PS 90_BBUSB_P 35 39

PROBE POINTS

PP5000 P4MM SM 1 SLEEP_CLK_32K 37 39
PP5001 P4MM SM 1 BB_EEPROM_SCL 39 40
PP5002 P4MM SM 1 BB_EEPROM_SDA 39 40
PP5003 P4MM SM 1 ET_DAC_P 40 44
PP5004 P4MM SM 1 ET_DAC_N 40 44

TP5029 A 1 TP-PS PP_LDO6 36 69 71 73

DEBUG CONNECTOR

NOSTUFF
J5006
AXE654124
M-ST-SM

PP_BATT_VCC IN 35 44 53 68 73

39 35	OUT	BB_JTAG_RST_L	10	9	PP_LDO11 IN 35 36 38 39 40 42 43 44 73
68 37	OUT	RF_PMIC_RESET_L	12	11	NC BT_WAKE
68 37	OUT	RADIO_ON_L	14	13	
			16	15	NC PP_LDO5
68 39	OUT	BB_USB_VBUS	18	17	NC WLAN_REG_ON
39 35	BI	90_BBUSB_N	20	19	RFFE1_DATA BI 35 40 44 45 46 47 48 49
39 35	BI	90_BBUSB_P	22	21	RFFE1_CLK BI 35 40 44 45 46 47 48 49
68	OUT	RESET_1V8_L	24	23	PMIC_RESOUT_L IN 35 37 39
39 35	OUT	BB_JTAG_TCK	26	25	RFFE2_DATA BI 35 40 50 51 53
39 35	OUT	BB_JTAG_TMS	28	27	
39 35	IN	BB_JTAG_TDO	30	29	BB_HOST_RDY IN 40 68
39 35	OUT	BB_JTAG_TDI	32	31	NC BT_REG_ON
39 35	OUT	BB_JTAG_TRST_L	34	33	BB_WAKE_HOST IN 40 68
		RTCLK NC	36	35	RFFE2_CLK BI 35 40 50 51 53
			38	37	BB_RESET_DET_L IN 40 68
37 35	OUT	PS_HOLD_PMIC	40	39	NC BB_SIM_CLK
68 40	IN	BB_UART_TXD	42	41	NC BB_SIM_DATA
68 40	OUT	BB_UART_RXD	44	43	NC BB_SIM_DETECT
		BB_UART_RTS_L NC	46	45	BB_RST_L OUT 37 68
		BB_UART_CTS_L NC	48	47	NC BB_SIM_RESET
		DEBUG_LED NC	50	49	BB_DEVICE_RDY IN 40 68
		GPIO51/BOOT_CONFIG_3 NC	52	51	GPIO54/BOOT_CONFIG_6 BOOT_HSIC IN 35 40
		GPIO53/BOOT_CONFIG_1 NC	54	53	NC GPIO48/BOOT_CONFIG_6
			58	57	

CONFIG _RF BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S0273	1	0.8PF 0201	C6001	CRITICAL	X137_RF
131S0273	1	0.8PF 0201	C6001	CRITICAL	X202_RF
131S0431	1	0.2PF 0201	C6013	CRITICAL	X190_RF
131S0273	1	0.8PF 0201	C6013	CRITICAL	X137_RF
131S0273	1	0.8PF 0201	C6013	CRITICAL	X202_RF
152S2020	1	3.6NH +/-0.1NH 400MA 0201	L6001	CRITICAL	X190_RF
152S2022	1	4.3NH 3% 500MA 0201	L6001	CRITICAL	X137_RF
152S2022	1	4.3NH 3% 500MA 0201	L6001	CRITICAL	X202_RF
131S0323	1	1.1PF 0201	C6421	CRITICAL	X190_RF
152S1217	1	1.0NH +/-0.1NH 750MA 0201	L6402	CRITICAL	X190_RF
152S2042	1	1.8NH +/-0.1NH 800MA 0201	L6402	CRITICAL	X137_RF
152S2042	1	1.8NH +/-0.1NH 800MA 0201	L6402	CRITICAL	X202_RF
152S1994	1	6.8NH 3% 210MA 01005	C6202	CRITICAL	X190_RF
152S1977	1	10.0NH 3% 170MA 01005	C6202	CRITICAL	X137_RF
152S1994	1	6.8NH 3% 210MA 01005	C6202	CRITICAL	X202_RF
152S00028	1	22NH 3% 120MA 01005	L6720	CRITICAL	X190_RF
152S1979	1	18NH 1% 140MA 01005	L6720	CRITICAL	X137_RF
152S1979	1	18NH 1% 140MA 01005	L6720	CRITICAL	X202_RF
138S0831	5	MURATA 2.2UF CAPACITOR	C5101,C5121,C5122,C6010,C6011	CRITICAL	CELL

REPLACES 138S0917 - 138S0917 CAN ONLY BE USED ON RAILS WITH 3V OR LESS

73 44 43 42 40 39 38 36 35 PP_LDO11

CELL RADIO_BB
R5001 1 10K 1% 1/32W MF 01005 2
R5002 1 10K 1% 1/32W MF 01005 2
R5003 1 10K 1% 1/32W MF 01005 2

40 35 BOOT_HSIC
40 BOOT_HSIC_USB
40 WATCHDOG_DISABLE

RADIO <-- 39 35 90_BBUSB_N XW5001 SM 1 2 90_BB_USB_N BI 68
RADIO <-- 39 35 90_BBUSB_P XW5002 SM 1 2 90_BB_USB_P BI 68
AP -->

PP_VCC_MAIN CURRENT SENSE

BATT --> 68 53 44 35 73 PP_BATT_VCC
RADIO <-- 73 36 PP_BATT_VCC_RADIO

CELL R5004 1 0.010 1% 1/6W MF 0402 2

U5000 INA216A2YFF WCSP-4
A1 IN+
A2 IN-
B1 GND
B2 OUT

ADC_IMEAS_RADIO 1

CELL R5005 0.00 2 0% 1/32W MF 01005 RADIO_ASM

NOSTUFF
C5001 1 0.1UF 20% 4V X5R 01005 2

RADIO_TO_PMU_ADC_IMEAS_RADIO 68

BOM ALTERNATES

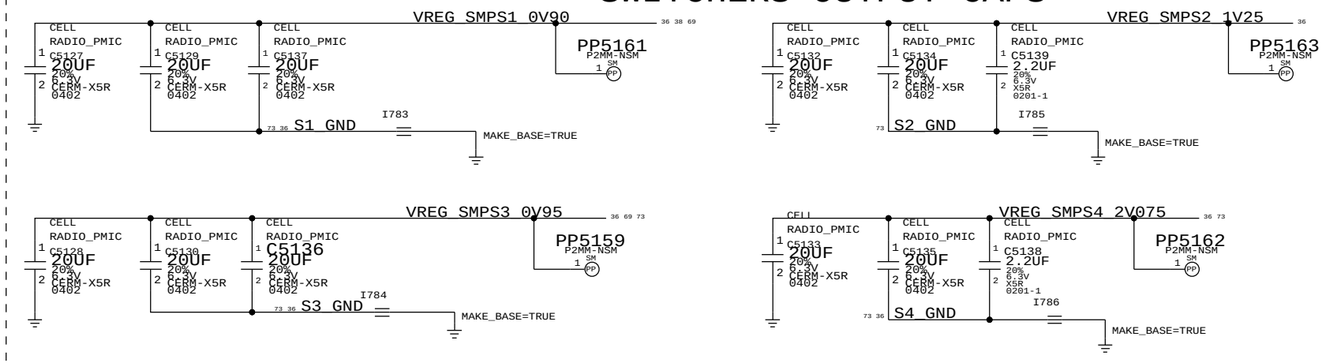
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1850	152S1721		L5101,L5103,L5104	MURATA IN, 2.2UH, 2016
152S2050	152S1857		L5902	TAIYO IND, 2.2UH, 2012

REVISION DATE: 9/29/2014

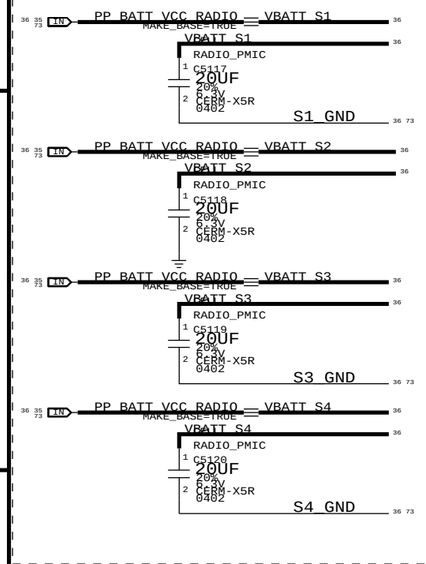
BASEBAND PMU (1 OF 2)

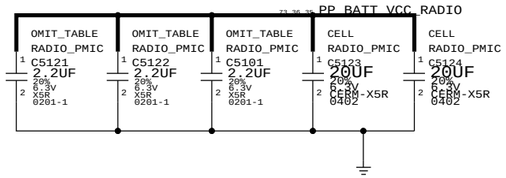
C332
R302
L304
U301

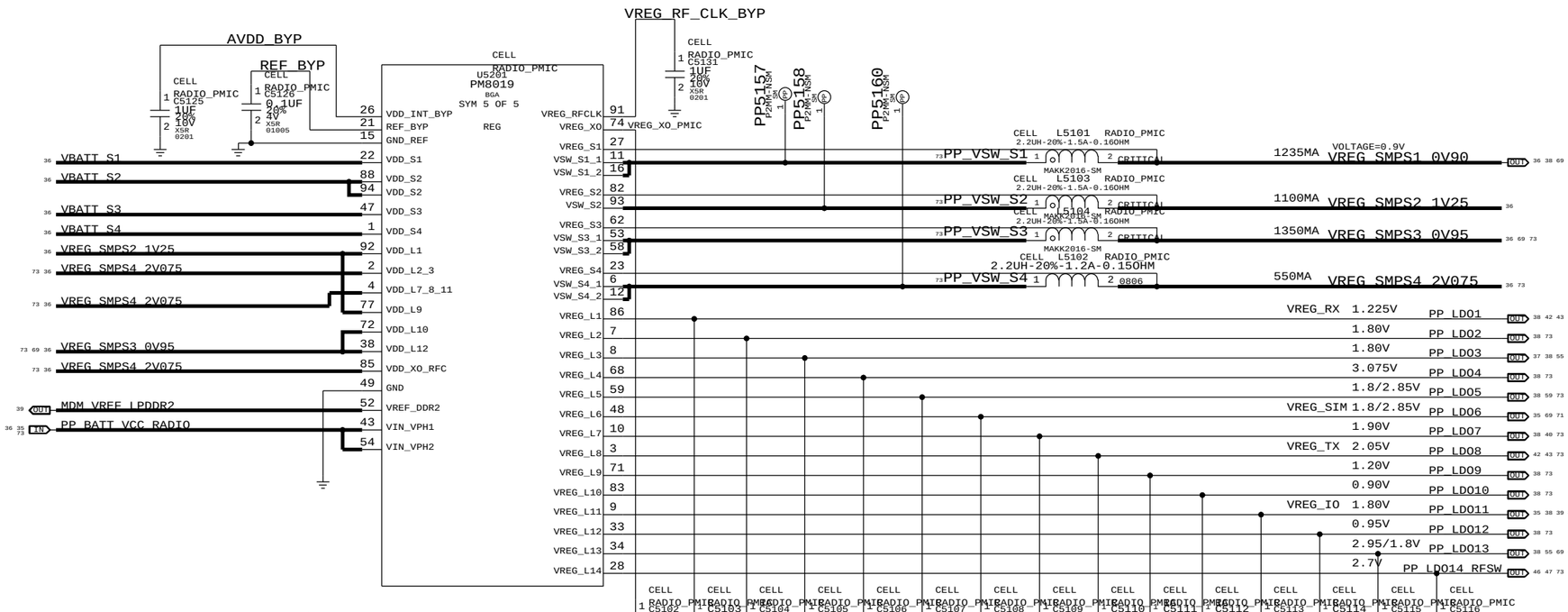
SWITCHERS OUTPUT CAPS



SWITCHERS BULK CAPS



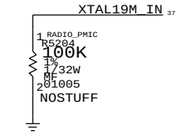


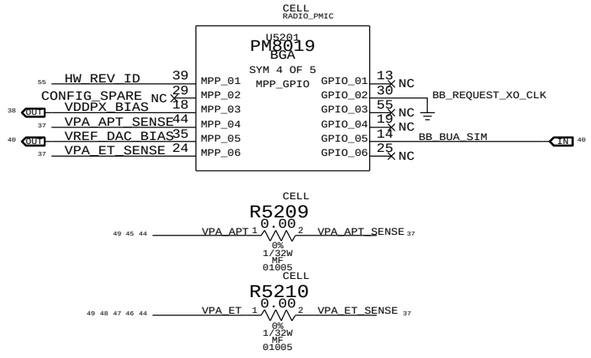


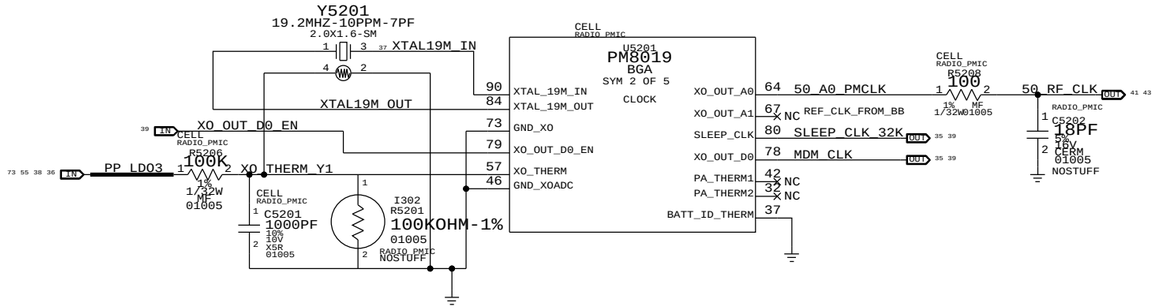
BASEBAND PMU (2 OF 2)

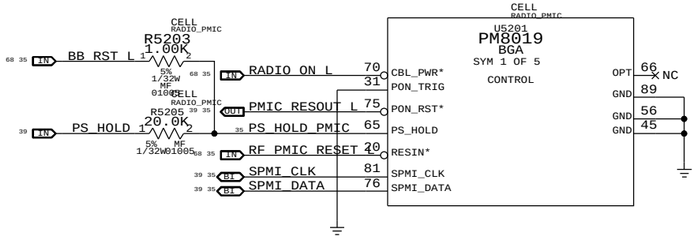
C401
R411
L400
U404

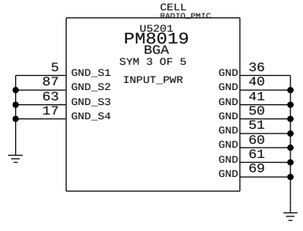
HW_REV_ID	R5202	R5207	J82 REV	J97 REV	J99 REV
0.10V	887K	51.1K	N/A	PROTO0	N/A
0.20V	422K	51.1K	PROTO0	PROTO0B	PROTO0
0.30V	255K	51.1K	PROTO1	PROTO1	PROTO1
0.40V	178K	51.1K	PROTO2		
0.50V	255K	100K	EVT		
0.60V	102K	51.1K	DVT		
0.70V	82.5K	51.1K	PVT		











BASEBAND (1 OF 3)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

C538
R500
L500
U502

CHINAFIX

CELL
RADIO_BB
U5401
ASIC-MDM9625M-333P
BGA
SYM 5 OF 6
PWR

(MSM CORE)
PP_LDO10
VDD_CORE: E15 K14 K15 L13 L14 M8 M9 M12 M13 N7 N8 N11 N12 P7 P10 P11

(MSM MEMORY)
PP_LDO12
VDD_MEM: E13 F8 F9 F15 G8 K10 L9 L10 N15 P14 P15 R7 R8 E5

(MODEM SUB SYSTEM)
VREG_SMPS1_0V90
VDD_MODEM: F6 F7 F10 F11 G6 G9 G10 G13 G14 G15 H8 H9 H12 H13 J7 J8 J11 J12 K6 K7 K11 L6

(EBI1 PAD)
PP_LDO9
VDD_P1: F19 L19 L20 M1 T19

(SDC1 PAD)
PP_LDO13
VDD_P2: B20

(GENIO PAD)
PP_VDD11
VDD_P3: B2 J19 K2 V2 V5 V19

(UIM1 PAD)
VDD_P4: R19

(UIM2 PAD)
PP_LDO5
VDD_P5: U19

(HSIC PAD)
PP_LDO9
VDD_P6: V9

VDDPX_BIAS
VREF_SDC: A19
VREF_UIM: U20

PP_LDO12
VDD_USB_CORE: V13

PP_LDO2
VDD_USB_1P8: U11

PP_LDO4
VDD_USB_3P3: V10

PP_LDO7
VDD_A2: C12 C9 B12

PP_LDO1
VDD_A1: B9 C6 B6 B15

PP_LDO10
VDD_PLL: U13 R12 D17

PP_LDO3
VDD_PLL2: E16

NC
VDD_ALWAYS_ON: T17

(LPDDR2)
PP_LDO11
VDD_DDR_CORE_1P8: J20 K1

(LPDDR2_CORE)
PP_LDO9
VDD_DDR_CORE_1P2: E20 H1 P1 P20

(QFUSE PROGRAMMING)
PP_LDO3
VDD_QFPROM_PRG: W8

CELL
RADIO_BB
U5401
ASIC-MDM9625M-333P
BGA
SYM 6 OF 6
GND

GND: A2 A20 C14 C20 E14 F12 F13 F14 F20 G7 G11 G12 H6 H7 H10 H11 H14 H15 J1 J6 J9 J10 J13 J14 K8 K9 K12 K13 K19 K20 L1 L7 L8 L11 L12 L15 M6 M7 M10 M11 M14 M15 M20 N1 N6 N9 N10 N13 N14 P6 P8 P9 P12 R20 T20 V20 W1 W5 W9 W20 W12 A12 A6 E12 E9 A9 E6 A17 C17 B17 P13 R13 R14 A15

(MSM CORE)
PP_LDO10
C5301 C5304 C5307 C5310 C5313 C5316 2.2UF 20% 4V X5R-CERM 0201

(MSM MEMORY)
PP_LDO12
C5302 C5305 C5308 C5311 C5314 C5317 2.2UF 20% 4V X5R-CERM 0201

(MODEM SUB SYSTEM)
VREG_SMPS1_0V90
C5303 C5306 C5309 C5312 C5315 C5318 2.2UF 20% 4V X5R-CERM 0201

(EBI1 PAD)
PP_LDO9
C5319 C5322 2.2UF 20% 4V X5R-CERM 0201

(SDC1 PAD)
PP_LDO13
C5320 2.2UF 20% 4V X5R-CERM 0201 NOSTUFF

(GENIO PAD)
PP_VDD11
C5321 C5323 4V X5R-CERM 0201

(HSIC PAD)
PP_LDO9
C5324 2.2UF 20% 4V X5R-CERM 0201

VDDPX_BIAS
C5325 0.1UF 20% 4V X5R 01005 NOSTUFF

(USB CORE)
PP_LDO12
C5326 4V X5R-CERM 0201

(USB 1.8V)
PP_LDO2
C5327 2.2UF 20% 4V X5R-CERM 0201

(COMBO DAC/BBRX)
PP_LDO7
C5328 2.2UF 20% 4V X5R-CERM 0201

(BBRX)
PP_LDO1
C5329 4V X5R-CERM 0201

(GPS ADC)
PP_LDO1
C5330 0.1UF 20% 4V X5R 01005 NOSTUFF

(PLL)
PP_LDO10
C5331 2.2UF 20% 4V X5R-CERM 0201 NOSTUFF

(PLL)
PP_LDO3
C5334 2.2UF 20% 4V X5R-CERM 0201 NOSTUFF

(LPDDR2)
PP_LDO11
C5332 C5333 C5335 2.2UF 20% 4V X5R-CERM 0201

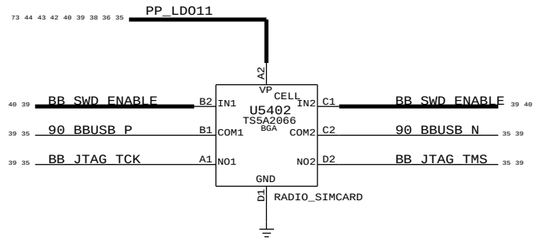
(LPDDR2 CORE)
PP_LDO9
C5336 C5338 2.2UF 20% 4V X5R-CERM 0201

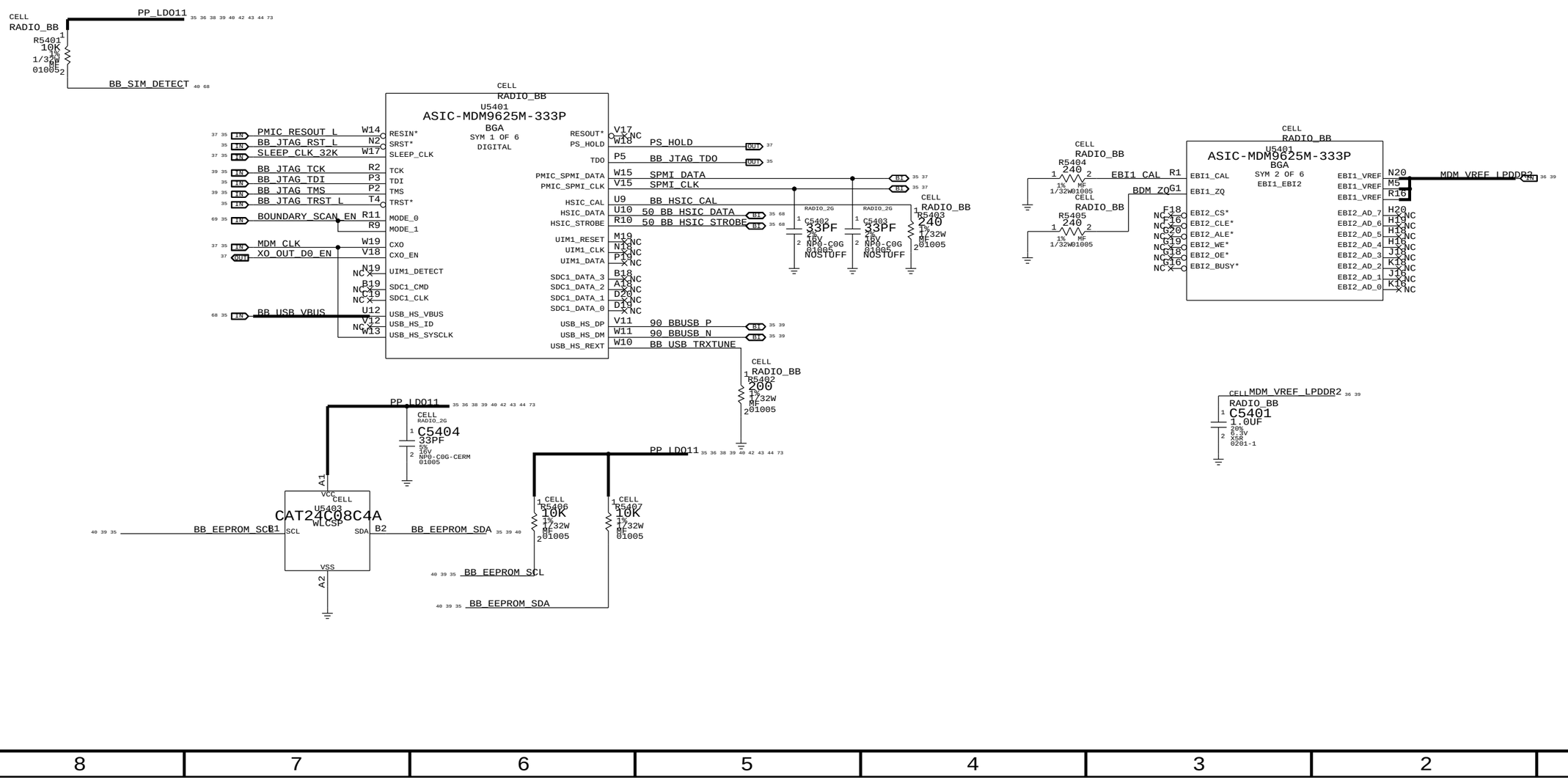
(QFUSE)
PP_LDO3
C5337 2.2UF 20% 4V X5R-CERM 0201

BASEBAND (2 OF 3)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

C600
R606
L600
U602

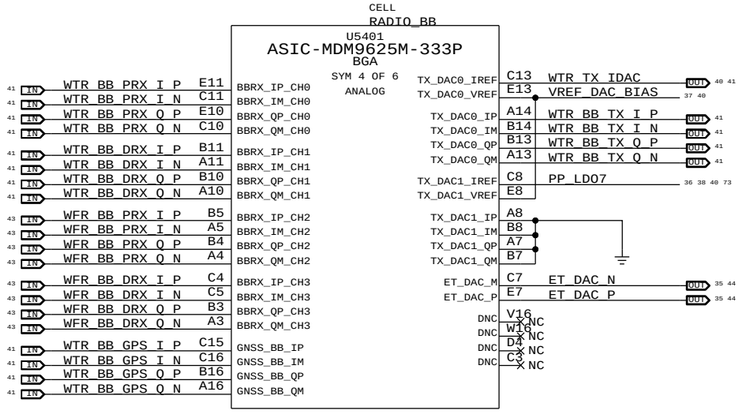


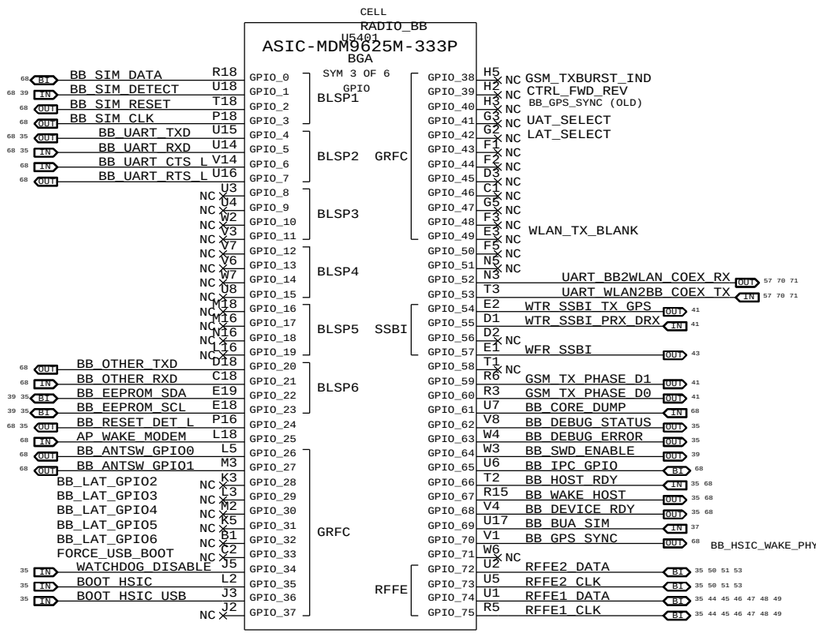


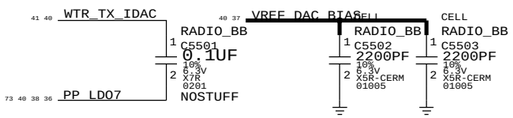
BASEBAND (3 OF 3)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

C704
R700
L700
U702





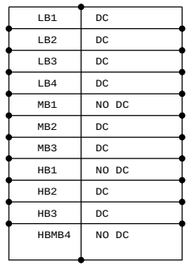


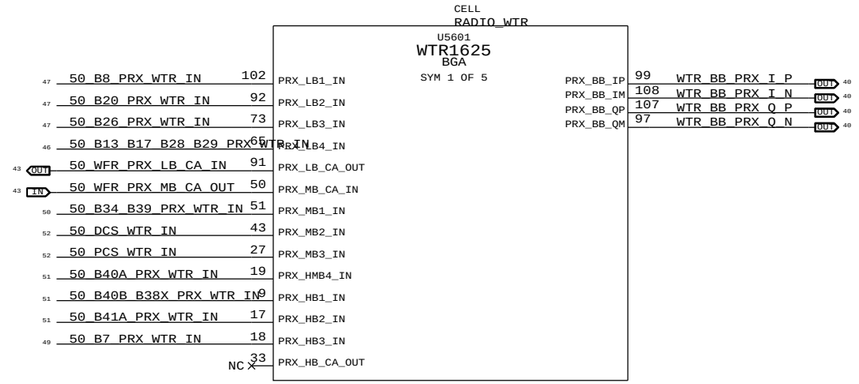
MAKE_BASE=TRUE

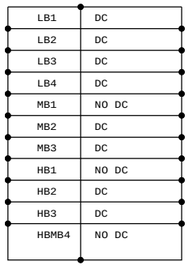
WTR TRANSCEIVER (1 OF 2)

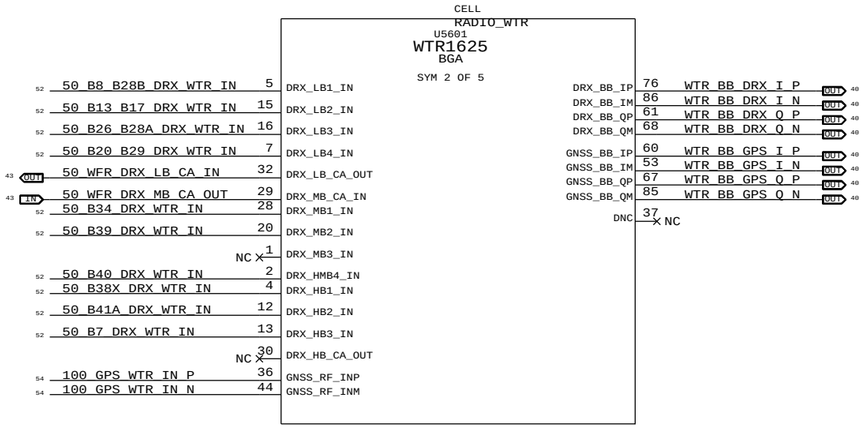
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

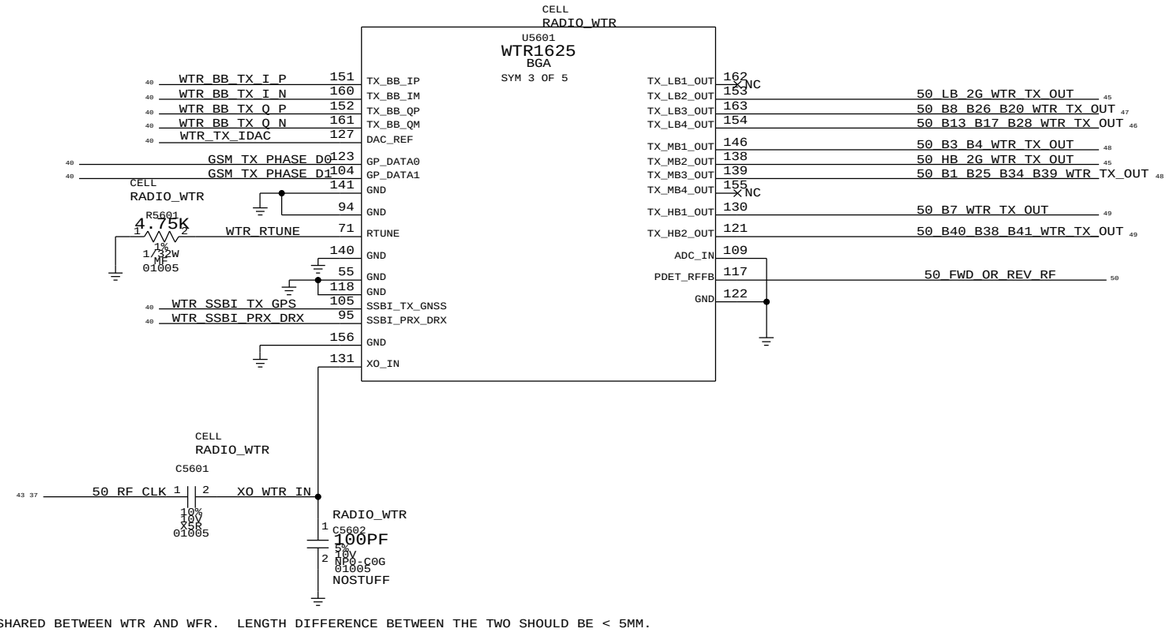
C802
R802
L800
U803











RF_CLK IS SHARED BETWEEN WTR AND WFR. LENGTH DIFFERENCE BETWEEN THE TWO SHOULD BE < 5MM.

WTR TRANSCEIVER (2 OF 2)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

C934
R926
L3802_RF
U902

WTR DECOUPLING CAPS

PP_LDO8 TRUE — VREG_2V
PP_LDO1 TRUE — VREG_1P3V

R5705 0 5% 1/20W MF 201 — MAKE_BASE=TRUE — VREG_2V_FILT1
R5707 0 5% 1/20W MF 201 — MAKE_BASE=TRUE — VREG_1P3V_FILT2
L5701 22NH-3%-0.25A 0201
MAKE_BASE=TRUE — VREG_1P3V_FILT2

C5701 10UF 20% 6.3V CERM-X5R 0402-2
C5704 10UF 20% 6.3V CERM-X5R 0402-2
C5707 10UF 20% 6.3V CERM-X5R 0402-2

VDD_DRX_BB_2V — C5718 100PF 5% 10V NP0-C0G 01005 NOSTUFF
VDD_TX_DA_2V — C5711 100PF 5% 10V NP0-C0G 01005 NOSTUFF
VDD_TX_BBF_2V — C5712 100PF 5% 10V NP0-C0G 01005 NOSTUFF
VDD_PRX_BB_2V

R5703 0.00 1% 1/20W MF 0201 — VDD_PRX_VCO_2V — C5713 0.1UF 20% 4V X5R 01005
R5704 0.00 1% 1/20W MF 0201 — VDD_SHDR_VCO_2V — C5714 0.1UF 20% 4V X5R 01005
R5702 0.00 1% 1/20W MF 0201 — VDD_TX_VCO_2V — C5715 0.1UF 20% 4V X5R 01005
VDD_TX_PLL_2V — C5702 0.1UF 20% 4V X5R 01005
R5706 0.00 0% 1/32W MF 01005 — VDD_XO_2V — C5703 0.1UF 10% 6.3V CERM-X5R 0201
VDD_FBRX_2V — C5716 0.1UF 20% 4V X5R 01005
L175 — VDD_PRX_2V

MAKE_BASE=TRUE — PP_LDO11 — VDD_MSM_1P3V — C5709 1.0UF 20% 6.3V CERM 0201-1 — C5717 0.1UF 20% 4V X5R 01005 NOSTUFF

VDD_PRX_LO_HB_1P3V — C5727 0.1UF 20% 4V X5R 01005
VDD_DRX_LB_1P3V
VDD_PRX_LB_1P3V
VDD_DRX_LO2_1P3V — C5728 0.1UF 20% 4V X5R 01005
VDD_DRX_LO1_1P3V — C5708 0.1UF 20% 4V X5R 01005
VDD_DRX_MB_1P3V
VDD_DRX_HB_1P3V

R5701 0.00 1% 1/20W MF 0201 — VREG_1P3V_FILT2_GPS — MAKE_BASE=TRUE — VDD_GPS_LNA_1P3V — C5725 0.1UF 20% 4V X5R 01005
VDD_GPS_BB_1P3V — C5726 0.1UF 20% 4V X5R 01005
VDD_GPS_PLL_1P3V
VDD_GPS_VCO_1P3V

VDD_SHDR_PLL_1P3V — C5719 0.1UF 20% 4V X5R 01005 NOSTUFF
VDD_PRX_HBMB_1P3V
VDD_SHDR_VCO_1P3V — C5720 0.1UF 20% 4V X5R 01005
VDD_PRX_VCO_1P3V

DELETED C3805 PR REVIEW FEEDBACK

VDD_PRX_LO_HBMB_1P3V — C5705 0.1UF 20% 4V X5R 01005
VDD_TX_SYNTH_1P3V — C5721 0.1UF 20% 4V X5R 01005
VDD_TX_LO_1P3V — C5722 0.1UF 20% 4V X5R 01005
VDD_TX_UPC_1P3V — C5723 100PF 5% 10V NP0-C0G 01005
R5708 0.00 1% 1/20W MF 0201 — VDD_TX_VCO_1P3V — C5706 0.1UF 20% 4V X5R 01005
L5702 8.2NH-3%-0.19A-1.6OHM 01005 — VDD_TX_DA_1P3V — C5724 100PF 5% 10V NP0-C0G 01005 NOSTUFF

U5601 WTR1625 BGA SYM 4 OF 5

VDD_PRX_VCO_1P3V 90	VDD_RF1_P_VCO	VDD_RF2_T_DA	129 VDD_TX_DA_2V
VDD_PRX_VCO_2V 80	VDD_RF2_P_VCO	VDD_RF1_T_DA	137 VDD_TX_DA_1P3V
VDD_PRX_LO_HB_1P3V 25	VDD_RF1_P_HB_LO	VDD_RF1_T_UPC	136 VDD_TX_UPC_1P3V
VDD_PRX_LB_1P3V 72	VDD_RF1_P_LB	VDD_RF1_T_LO	135 VDD_TX_LO_1P3V
VDD_PRX_HBMB_1P3V 34	VDD_RF1_P_HMB	VDD_RF2_T_BB	126 VDD_TX_BBF_2V
VDD_PRX_LO_HBMB_1P3V 57	VDD_RF1_P_HMB_LO	VDD_RF2_FBRX	116 VDD_FBRX_2V
VDD_PRX_PLL_1P3V 79	VDD_RF1_P_PLL	VDD_RF2_T_VCO	157 VDD_TX_VCO_2V
VDD_PRX_BB_2V 98	VDD_RF2_P_BB	VDD_RF1_T_VCO	149 VDD_TX_VCO_1P3V
VDD_PRX_2V 100	VDD_RF2_P_RX	VDD_RF1_T_SYN	115 VDD_TX_SYNTH_1P3V
VDD_DRX_LO1_1P3V 14	VDD_RF1_D_LB_LO	VDD_RF2_T_PLL	114 VDD_TX_PLL_2V
VDD_DRX_LO2_1P3V 38	VDD_RF1_D_LOM	VDD_RF1_G_LNA	52 VDD_GPS_LNA_1P3V
VDD_DRX_LB_1P3V 31	VDD_RF1_D_LB	VDD_RF1_G_VCO	74 VDD_GPS_VCO_1P3V
VDD_DRX_HB_1P3V 22	VDD_RF1_D_HB	VDD_RF1_G_PLL	93 VDD_GPS_PLL_1P3V
VDD_DRX_MB_1P3V 11	VDD_RF1_D_MB	VDD_RF1_G_BB	59 VDD_GPS_BB_1P3V
VDD_DRX_BB_2V 54	VDD_RF2_D_BB	GND	113 PWRTERM2GND
VDD_SHDR_VCO_1P3V 48	VDD_RF1_S_VCO	VDD_RF2_XO	147 VDD_XO_2V
VDD_SHDR_VCO_2V 62	VDD_RF2_S_VCO	VDD_DIO	103 VDD_MSM_1P8V
VDD_SHDR_PLL_1P3V 78	VDD_RF1_S_PLL		

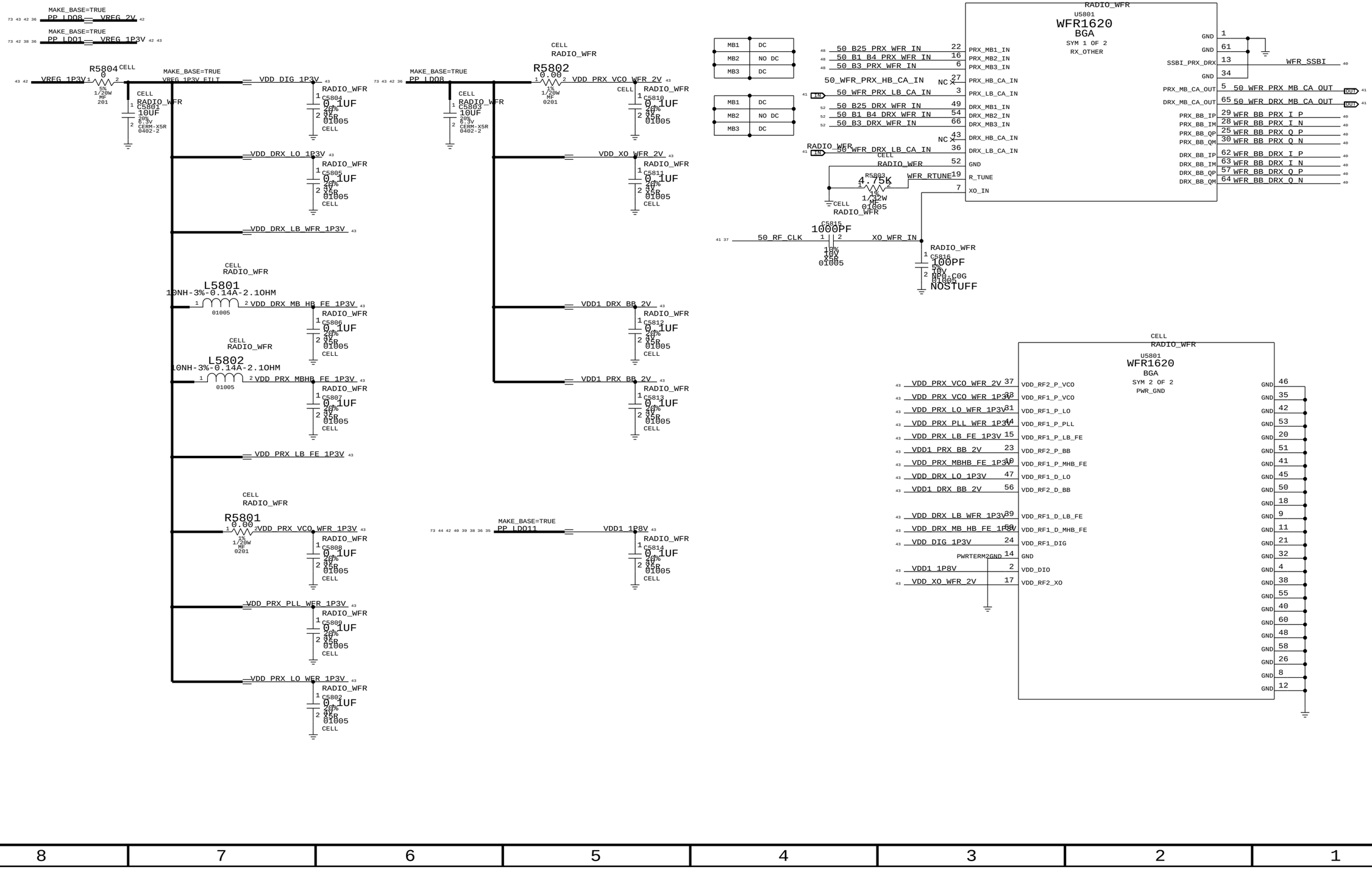
U5601 WTR1625 BGA SYM 5 OF 5

89 GND	GND	111 GND
56 GND	GND	101 GND
83 GND	GND	110 GND
82 GND	GND	145 GND
58 GND	GND	144 GND
35 GND	GND	143 GND
8 GND	GND	128 GND
26 GND	GND	120 GND
64 GND	GND	119 GND
42 GND	GND	106 GND
41 GND	GND	150 GND
81 GND	GND	134 GND
21 GND	GND	159 GND
6 GND	GND	142 GND
24 GND	GND	125 GND
39 GND	GND	124 GND
10 GND	GND	148 GND
3 GND	GND	158 GND
23 GND	GND	133 GND
46 GND	GND	112 GND
49 GND	GND	132 GND
69 GND	GND	45 GND
88 GND	GND	66 GND
70 GND	GND	84 GND
63 GND	GND	75 GND
40 GND	GND	164 GND
47 GND		
87 GND		
77 GND		
96 GND		

WFR TRANSCEIVER

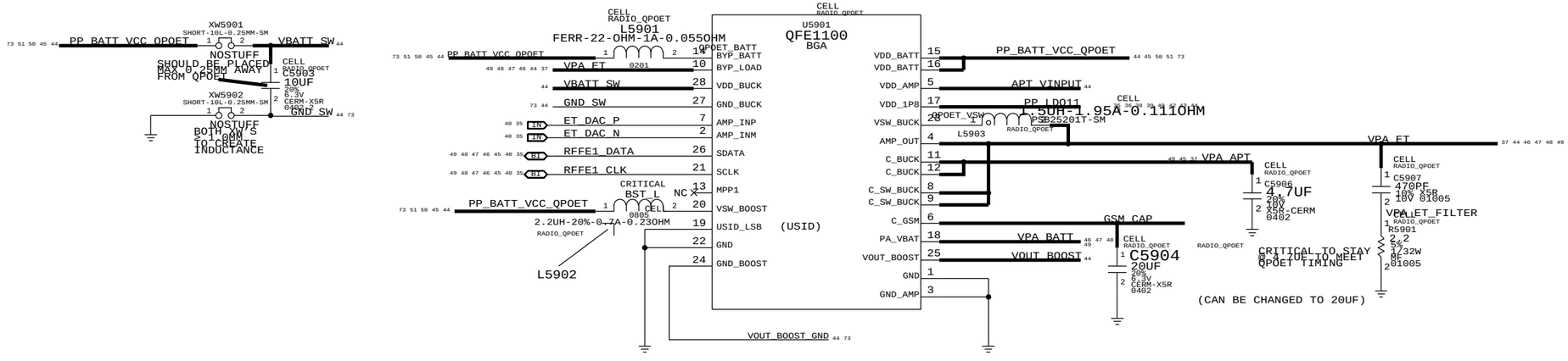
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

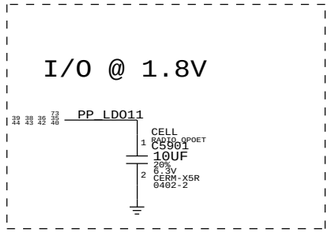
C1019
R1016
L1000
U1002

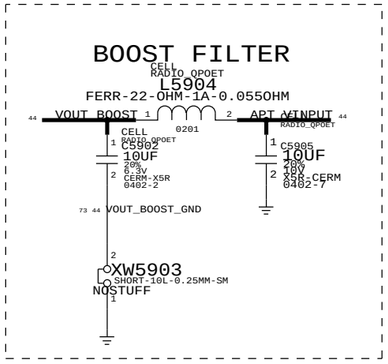


QFE DCDC

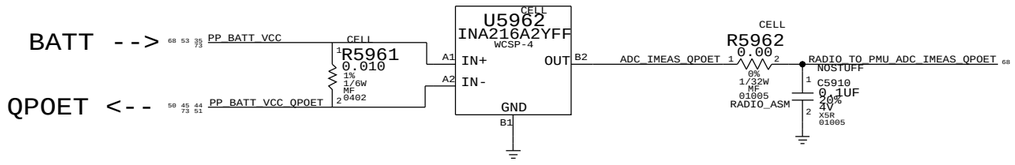
C1110
R1102
L1104
U1101







PP_VCC_MAIN CURRENT SENSE

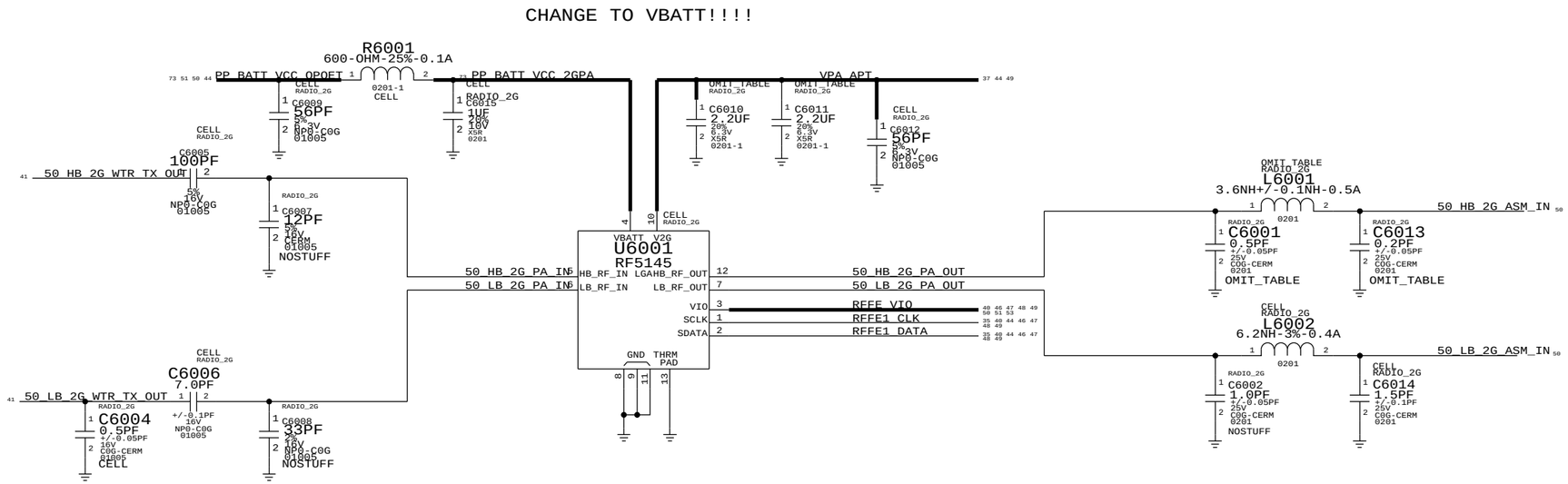


2G PA

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

C1208
R1200
L1204
U1201

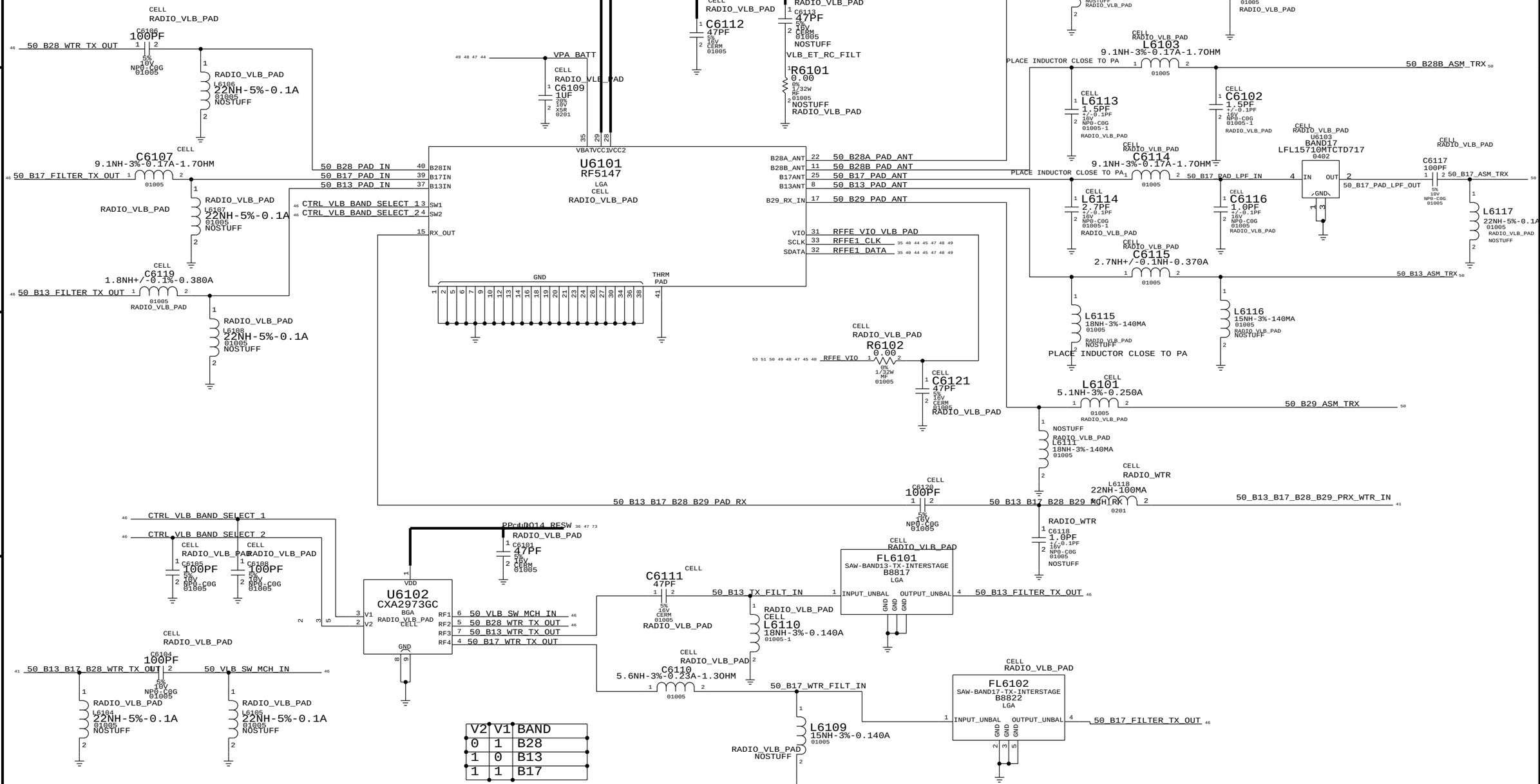
CHANGE TO VBATT!!!!



VERY LOW BAND PAD (B13, B17, B28)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

C1332
R1300
L4215_RF
U1304



LOW BAND PAD (B8, B26, B20)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

C4317_RF
R1400
L4316_RF
U1402

CHINAFIX

CAPACITOR THAT'S SUPPOSED TO GO HERE IS LOCATED ON MID BAND PAD. THE 2 PAD'S NEED TO SHARE DECOUPLING

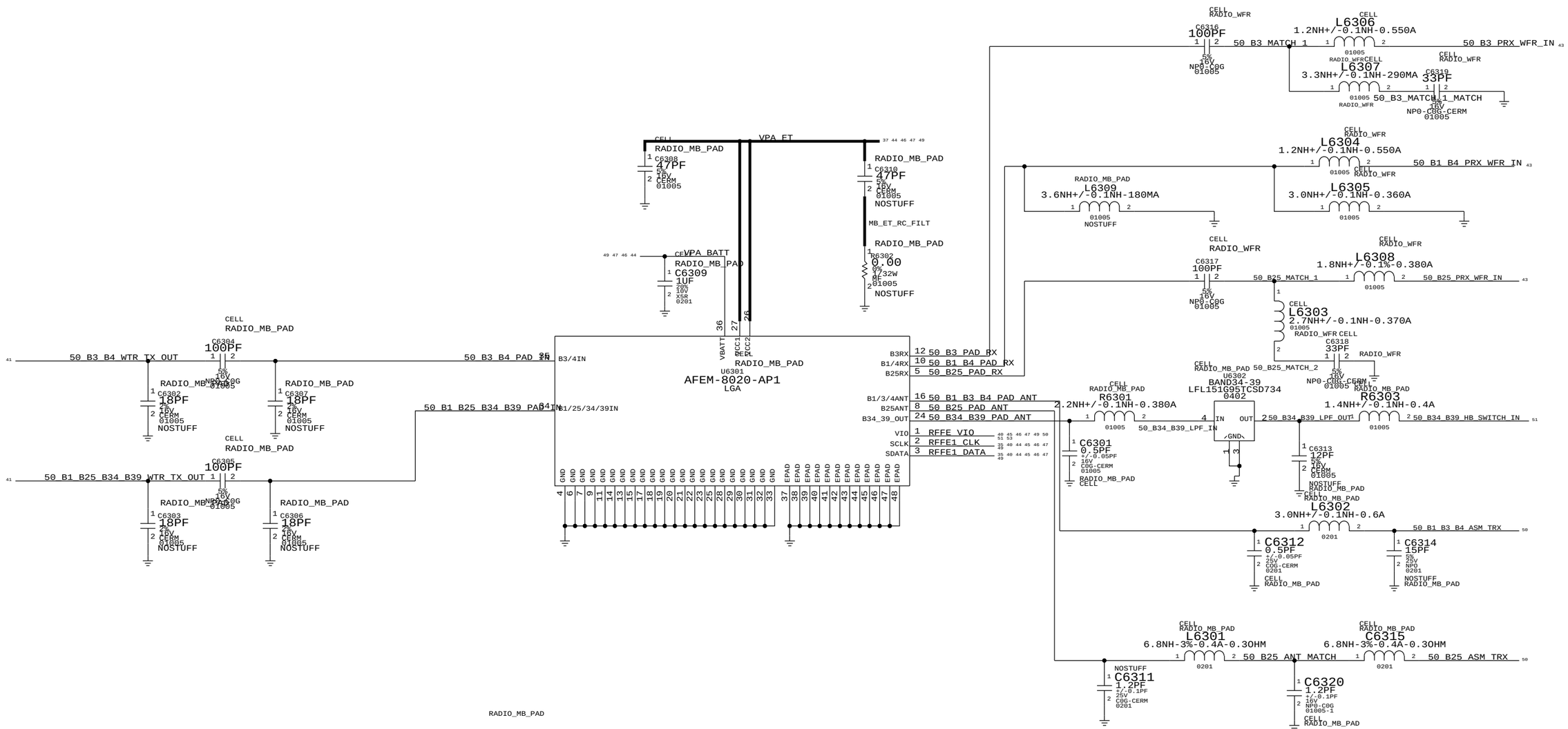
WTR OUTPUT HAS DC FIRST SHUNT MUST BE A CAPACITOR.

PLACE INDUCTOR CLOSE TO PA

V2	V1	BAND
0	1	B8
1	0	B20
1	1	B26

MID BAND PAD (B1, B25, B3, B4, B34, B39)

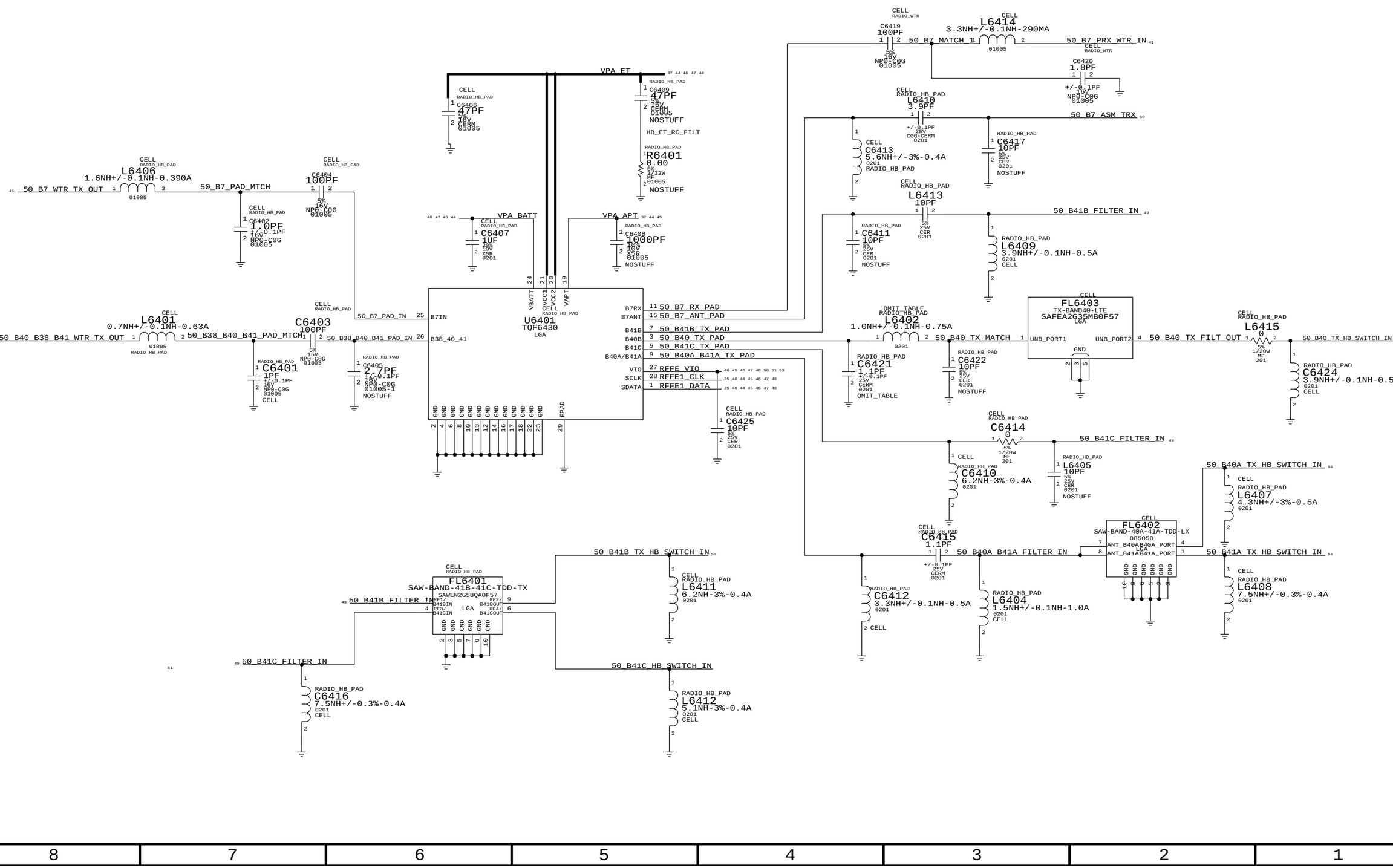
C1510
R1500
L4409_RF
U1501



HIGH BAND PAD (B7, B38, B40, B41, XGP)

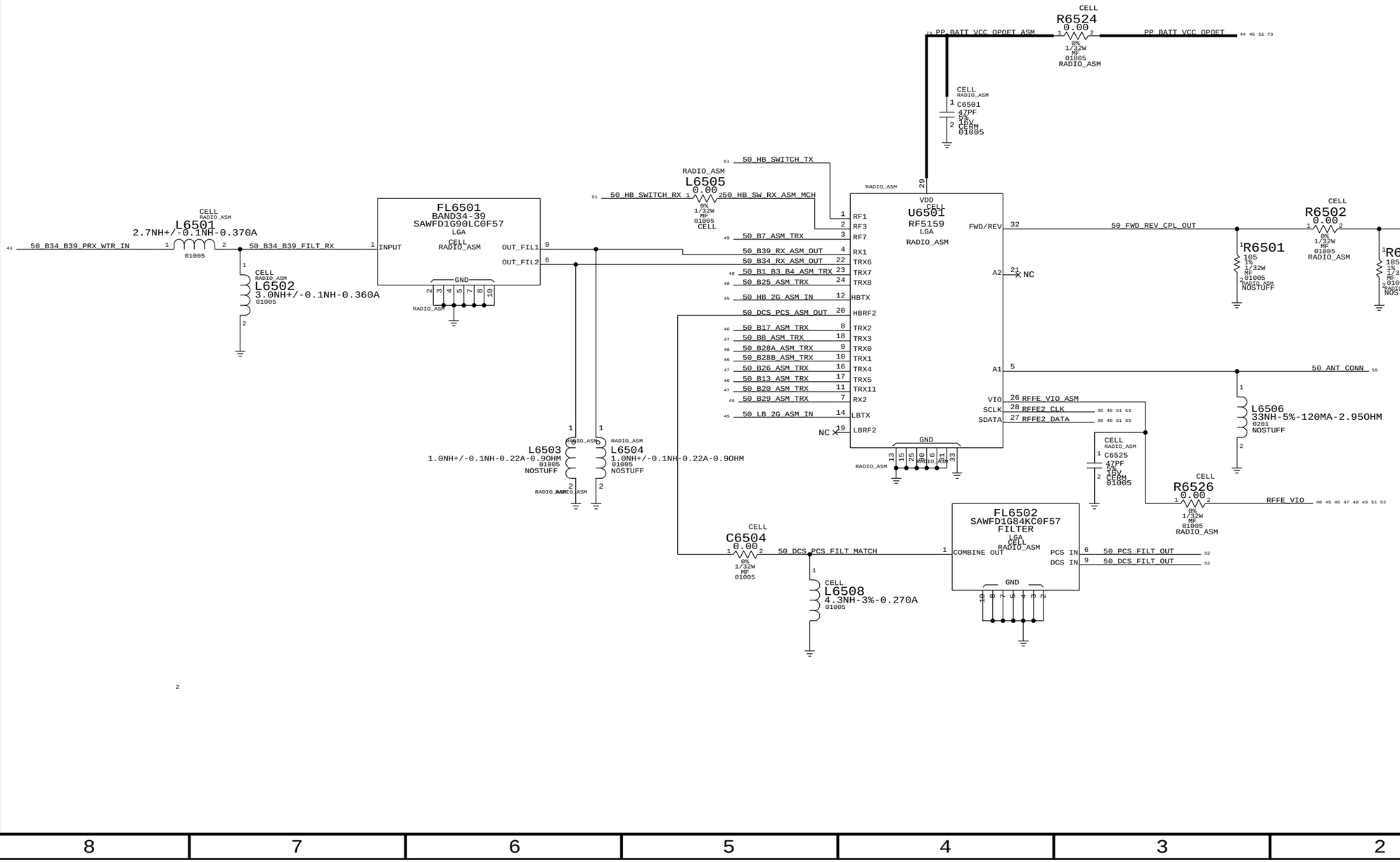
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

C1614
R1600
L1616
U1601

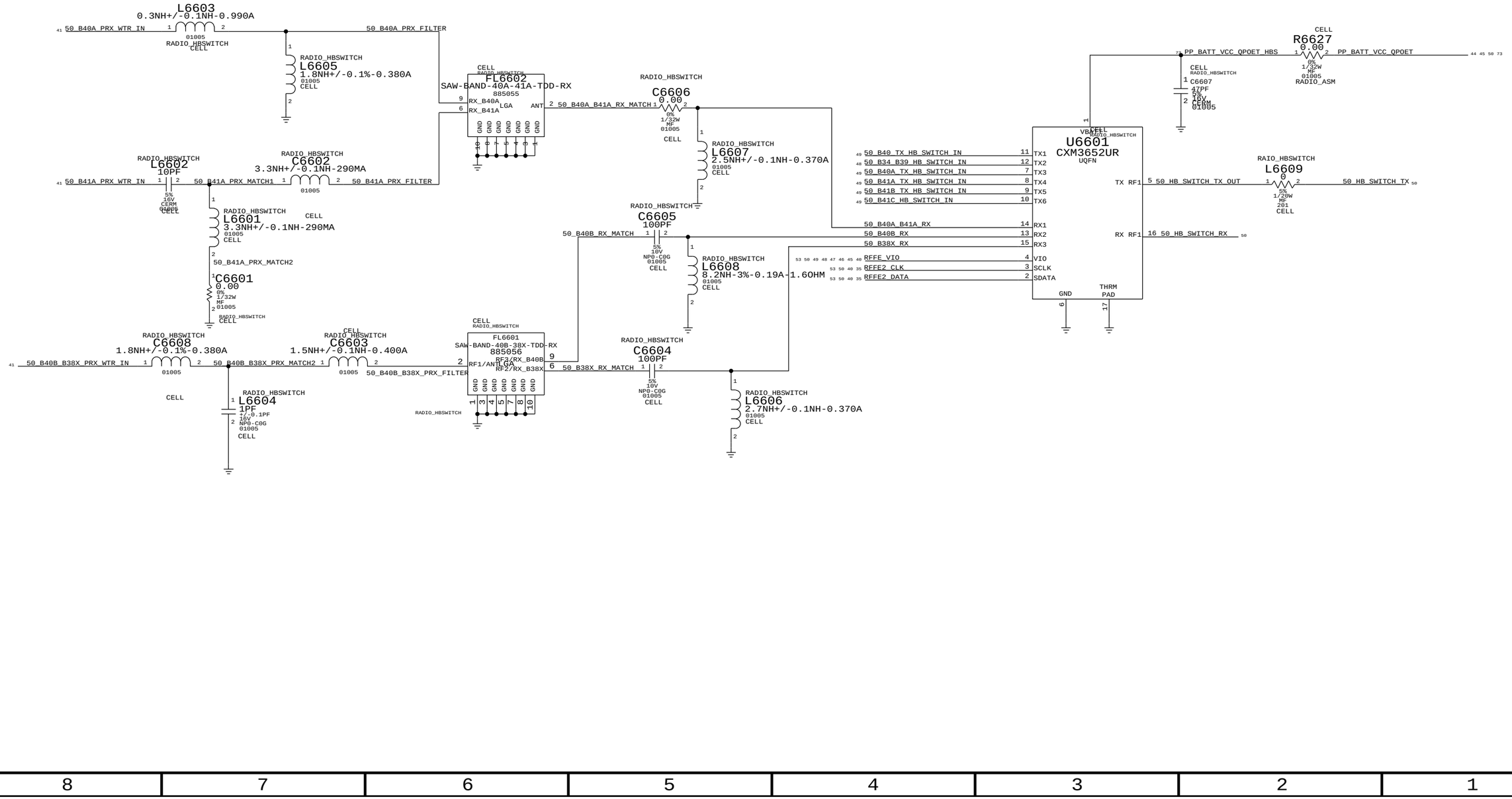


ANTENNA SWITCH

C1702
R1700
L4608_RF
U1702



HIGH BAND SWITCH

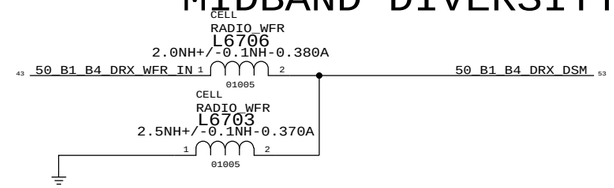


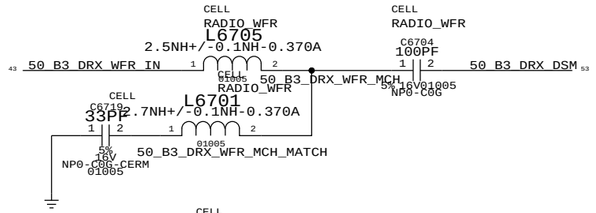
RX DIVERSITY (1 OF 2)

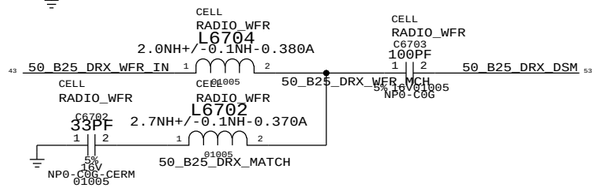
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

C4826_RF
R1800
L1829
U1801

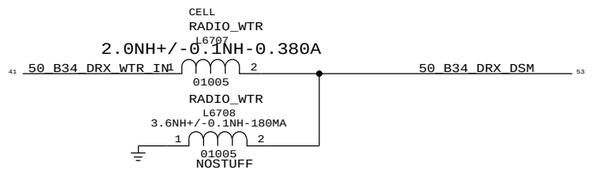
MIDBAND DIVERSITY - WFR

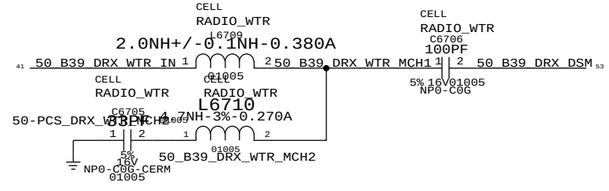




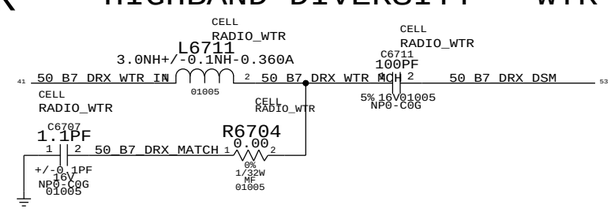


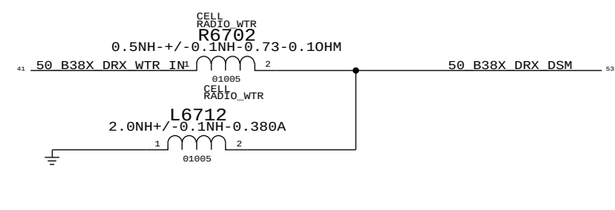
MIDBAND DIVERSITY - WTR

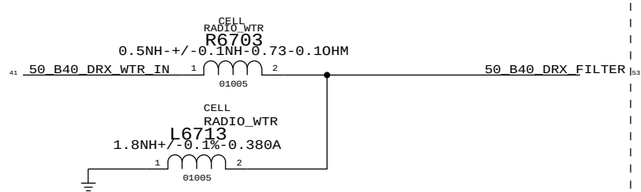


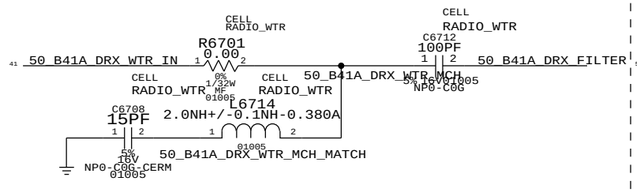


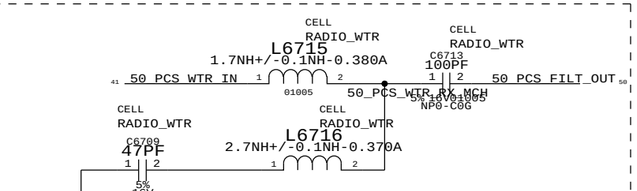
HIGHBAND DIVERSITY - WTR

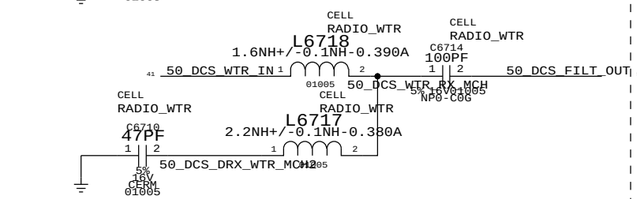




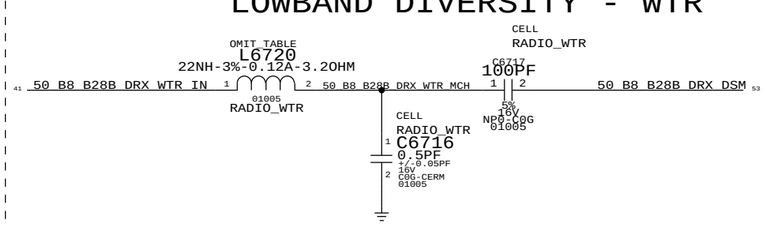


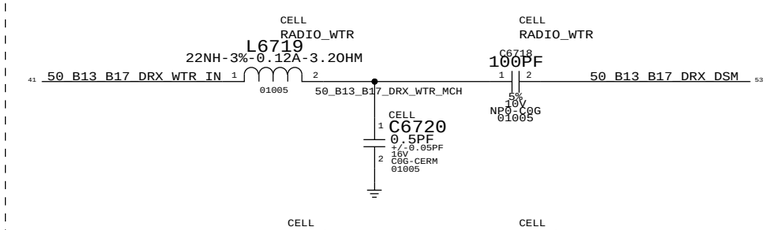


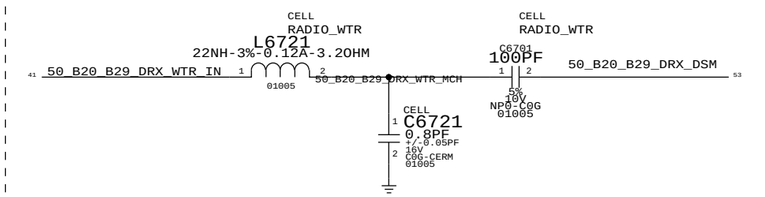


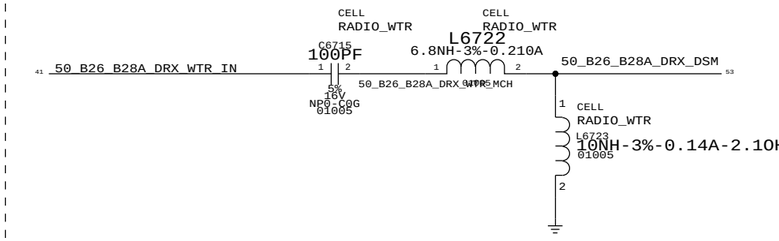


LOWBAND DIVERSITY - WTR



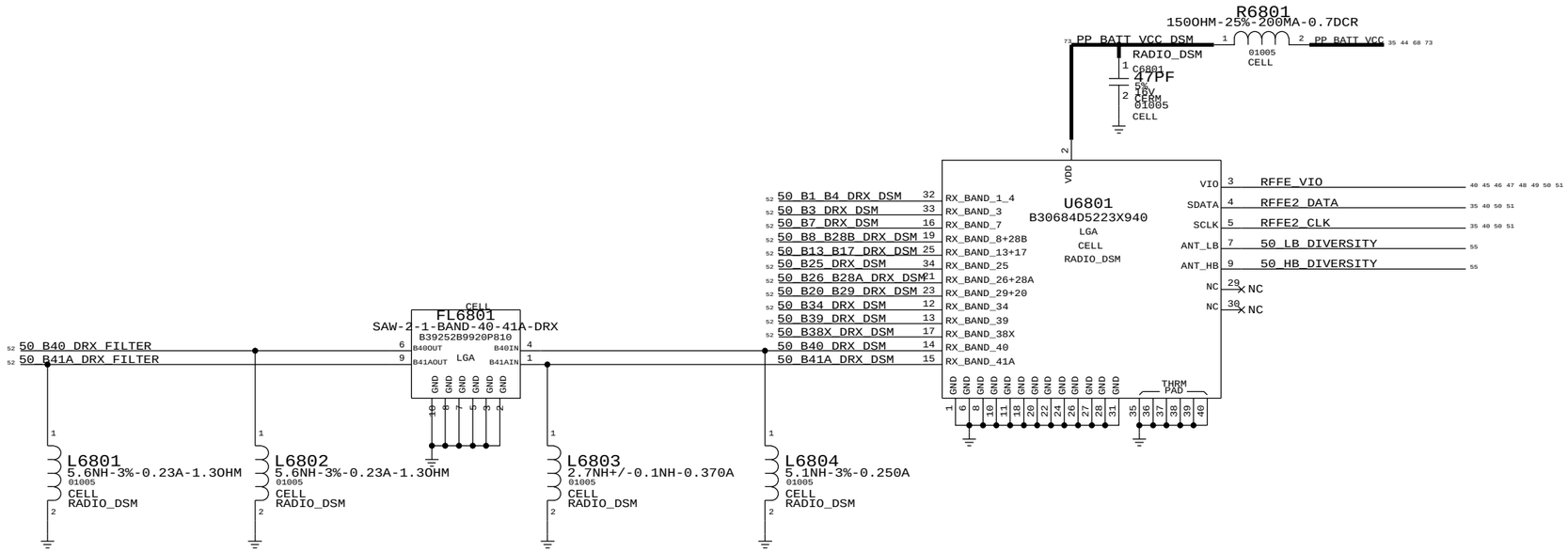






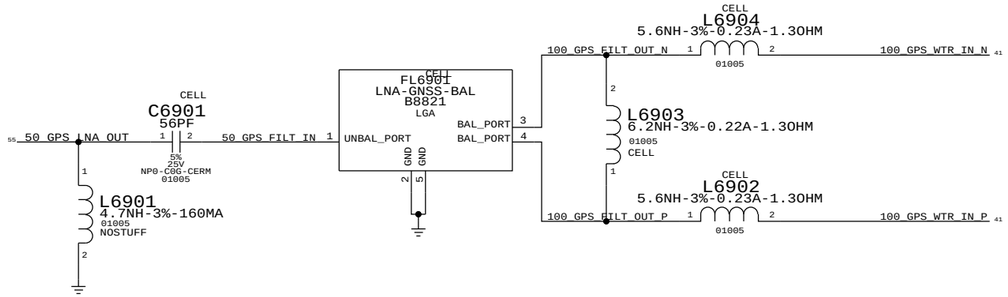
RX DIVERSITY (2 OF 2)

C1900
R1900
L1900
U1901



GPS

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



ANTENNA FEEDS AND GPS (J82)

PRI_ANT COAX

CRITICAL CELL
J7001
MM5829-2700
F-ST-SM

50_ANT_CONN

GPS_DRX_ANT

CELL
CRITICAL
J7410
MM4829-2702
F-ST-SM

50 GPS DRX WIFI G0 ANT COAX

CELL
DPX162690DT-8049C1SJ
FL7003
SM

50 LB DIVERSITY
LOW_BAND
HIGH_BAND
COMMON
GND

50 WIFI G1

CELL
J7004
MM8830-2600B
F-RT-SM

CELL
R7001
0
5%
1/20W
MF
201

50 GPS HB WIFI G0

50 GPS DRX WIFI G0 NOTCHPLEXER

CELL
FL7002
885060
DIPLEXER-CELL-WIFI
LGA

RF1
SMD2_RF1/SMD4_GND
SMD1_RF2
RF3
RF2
GND

CELL
C7001
0.2PF
+/-0.1PF
25V
C0G-CERM
201
NOSTUFF

CELL
L7003
3.2NH+/-0.1NH-0.5A
0201
CELL

50 NOTCHPLEXER SMD2

CELL
C7002
7.5NH+/-0.3%-0.4A
0201
NOSTUFF

50 GPS DRX NOTCHPLEXER

50 NOTCHPLEXER SMD1

CELL
L7002
3.6NH+/-0.1NH-0.5A
0201
CELL

CELL
R7002
6.8PF
+/-0.1PF
25V
C0G
0201

50 NOTCHPLEXER MATCH

CELL
C7004
5.6NH+/-3%-0.4A
0201

GND

CELL
L7004
0.3PF
+/-0.1PF
25V
C0G-CERM
201

50 GPS DRX SW CONN

CELL
R7004
1.8NH+/-0.1NH-0.8A
0201

50 GPS EXTRACT ANT

NOSTUFF
L7005
5.6NH-3%-0.35A
0201

R7003
150OHM-25%-200MA-0.7DCR
01005
CELL

PP_LDO13_GPS
PP_LDO13

OLD: LDO6
NEW: LDO13

BYPASS INTEGRATED INTO MODULE

CELL
U7001
LNA-CELL-GPS
LGA

VDD
ANT
TBD
GPS_OUT
CELL_OUT
GND
EPAD

50 GPS LNA OUT

CELL
R7005
0
5%
1/20W
MF
201

50 EXTRACT DRX
50 HB DIVERSITY

CELL
C7006
0.2PF
+/-0.1PF
25V
C0G-CERM
201
NOSTUFF

J82 HW_ID (MAPPING PG 52)

EVT

RADIO_PMIC
PP_LDO3

RADIO_PMIC
R7010
102K
1%
1/32W
MF
01005
CELL

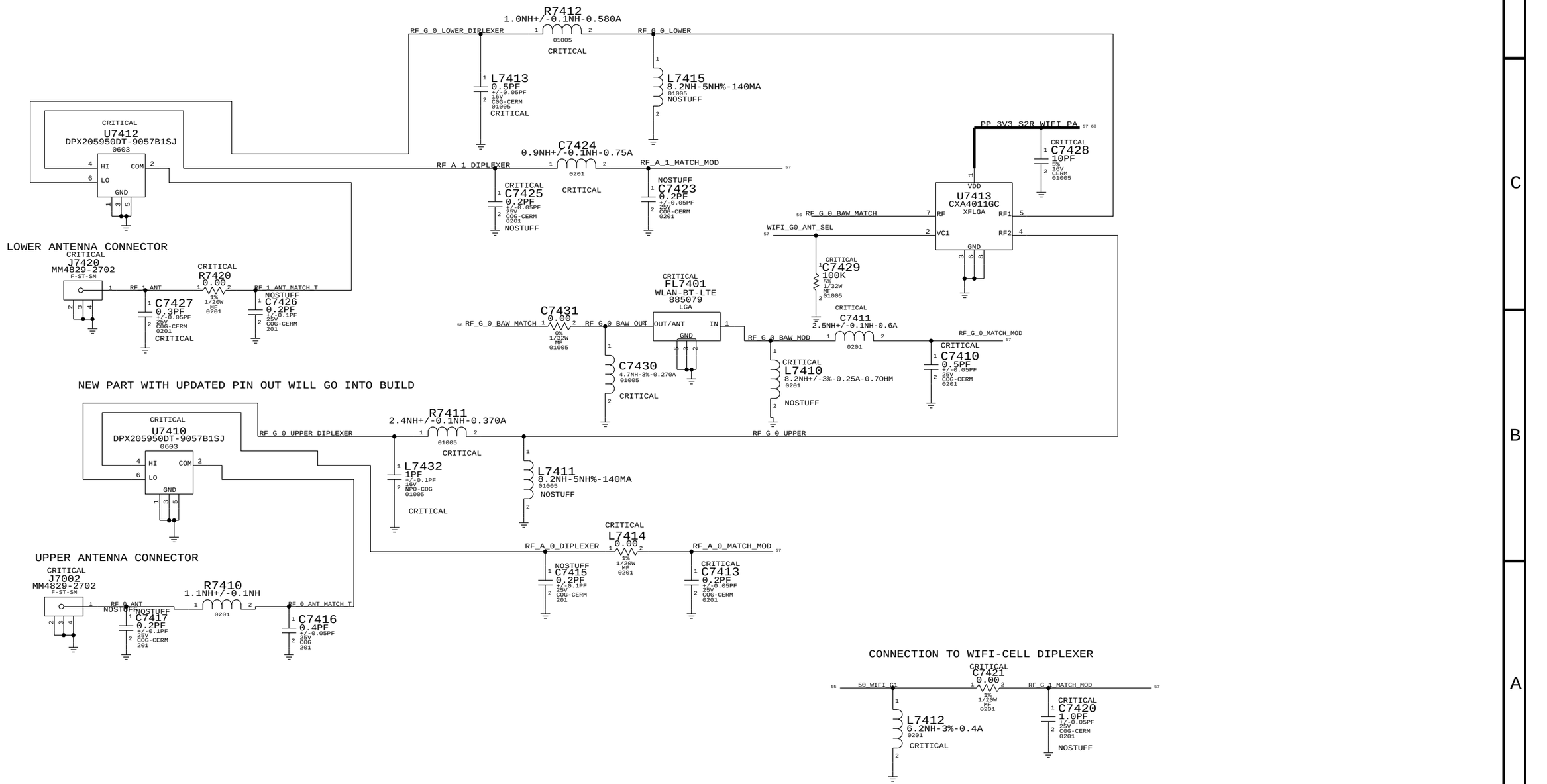
HW_REV_ID

RADIO_PMIC
R7011
51.1K
1%
1/32W
MF
01005
CELL

HW_REV_ID	R7010	R7011	J82 REV	J97 REV	J99 REV
0.10V	887K	51.1K	N/A	PROTO0	PROTO0
0.20V	422K	51.1K	PROTO0	PROTO0B	PROTO1
0.30V	255K	51.1K	PROTO1	PROTO1	PROTO2
0.40V	178K	51.1K	PROTO2		
0.50V	255K	100K	PRE-EVT		
0.60V	102K	51.1K	EVT		
0.70V	82.5K	51.1K	DVT		

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0565	197S0598		Y5201	KDS XTAL, 19.2MHZ
197S0593	197S0598		Y5201	NDK XTAL, 19.2MHZ

WIFI/BT (2 OF 5)
WIFI/BT FRONT END FOR J82



WIFI/BT (3 OF 5)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0251	1	MODULE, WIFI/BT, STELLA CIDRE	U7500	CRITICAL	MLB_A
339S0241	1	MODULE, WIFI/BT, STELLA	U7500	CRITICAL	MLB_B

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0250	339S0251	MLB_A	U7500	STELLA CIDRE ALT
339S0229	339S0241	MLB_B	U7500	STELLA ALT

NOTE* PIN5 SHOULD BE NC FOR J81/J96/J97/J98/J99

U7500
LBEE5UAZLC-670
LGA
SYM 2 OF 2
OMIT_TABLE

GND: 15, 19, 23, 24, 26, 27, 29, 30, 32, 33, 34, 36, 37, 38, 40, 57, 59, 64, 67, 69, 72, 75, 78

THRM_PAD: 81–113, 114–170

PP_1V8_S2R_VDDIO_WLAN_BT → R7513 0.00 0% 1/32W MF 01005 → PP_WL_VDDIO
C7501 27PF 5% 16V NP0-C0G 01005
C7500 0.01UF 10% 6.3V X5R 01005

PP_VCC_MAIN_WLAN
C7583 4.7UF 20% 6.3V X5R-CERM1 402
C7584 4.7UF 20% 6.3V X5R-CERM1 402

PP_3V3_S2R_WIFI_PA
C7580 4.7UF 20% 6.3V X5R-CERM1 402
C7581 10UF 20% 6.3V CERM-X5R 0402-2
C7582 10UF 20% 6.3V CERM-X5R 0402-2

U7500
LBEE5UAZLC-670
LGA
339S0229 2
CRITICAL
MODULE_INST
OMIT_TABLE

VDDIO_1P8	11		
BATT_VCC	58		
BATT_RF_VCC	25		
BATT_RF_VCC	35		
CLK_PMU2WLAN_32K	68	CLK32K_AP	
UART_SOC2WLAN_TX	48	FAST_UART_RX	
UART_WLAN2SOC_RX	54	FAST_UART_TX	
WLAN_GPIO_8	53	WL_GPIO_8	
UART_WLAN2SOC_CTS_L	46	FAST_RTS_OUT	
GPIO_PMU2WLAN_REG_ON	60	WLAN_REG_ON	
GPIO_PMU2BT_REG_ON	56	BT_REG_ON	
JTAG_WLAN_SEL	45	JTAG_SEL	
	2	ANT_SWITCH_CORE1	NC
WIFI_G0_ANT_SEL	5	ANT_SWITCH_CORE0	
WLAN_GPIO_10 / GPIO_SOC2WLAN_PCIE_DEV_WAKE	66	HSIC_WLAN_DATA	NC
	65	HSIC_WLAN_STROBE	NC
UART_SOC2WLAN_RTS_L → R7592 0.00 0% 1/32W MF 01005 → UART_SOC2WLAN_RTS_L_RES	47	HSIC_DEV_RDY	
	61	HSIC_HOST_READY_PCIE_DEV_WAKE	
	62	HSIC_RESUME_FAST_CTS_IN_JTAG_TCK	
JTAG_WLAN_TMS	63	JTAG_TMS	
JTAG_WLAN_TRST	44	JTAG_TRST	
WLAN_SECI_IN	43	SEC_IN/JTAG_TDI	
UART_WLAN2BB_COEX_TX	42	SEC_OUT/JTAG_TDO	
GPIO_BT2PMU_HOST_WAKE	17	HOST_WAKE_BT	
RF_G_0_MATCH_MOD	22	2G_CORE0_ANT	
RF_G_1_MATCH_MOD	31	2G_CORE1_ANT	
RF_A_0_MATCH_MOD	28	5G_CORE0_ANT	
RF_A_1_MATCH_MOD	39	5G_CORE1_ANT	
BT_EXT_SYNC	20	BT_GPIO3	
BT_EXT_CLK	21	BT_GPIO5	
	41	NC	NC

R7500 10K 5% 1/32W MF 01005 (WLAN_GPIO_10 → UART_SOC2WLAN_RTS_L)

R7589 0.00 0% 1/32W MF 01005: UART_BB2WLAN_COEX_RX → JTAG_WLAN_TRST

BT_GPIO4	10	NC	
BT_WAKE	16	GPIO_SOC2BT_WAKE	
BT_USB_DP	3	NC	
BT_USB_DN	4	NC	
BT_UART_RXD	13	UART_SOC2BT_TX	
BT_UART_TXD	12	UART_BT2SOC_RX	
BT_UART_CTS*	9	UART_SOC2BT_RTS_L	
BT_UART_RTS*	8	UART_BT2SOC_CTS_L	
BT_PCM_CLK	6	I2S_SOC2BT_BCLK	
BT_PCM_SYNC	18	I2S_SOC2BT_LRCK	
BT_PCM_OUT	14	I2S_BT2SOC_DIN	
BT_PCM_IN	7	I2S_SOC2BT_DOUT	
WL_GPIO_9	52	WLAN_GPIO_9	OSCAR_CONTEXT_A
WL_GPIO_13	51	OSCAR2RADIO_CONTEXT_B	
WL_HOST_WAKE	55	GPIO_WLAN2PMU_HOST_WAKE	
WLAN_PCIE_PME	79	PCIE_WLAN2PMU_WAKE_L	
WLAN_PCIE_CLKREQ	80	PCIE_WLAN2SOC_CLKREQ	
WLAN_PERST	1	PCIE_SOC2WLAN_PERST	
WLAN_PCIE_RDP0	77	PCIE_SOC2WLAN_TX_P	
WLAN_PCIE_RDN0	76	PCIE_SOC2WLAN_TX_N	
WLAN_PCIE_TDP0	73	PCIE_TX_P	
WLAN_PCIE_TDN0	74	PCIE_TX_N	
WLAN_PCIE_REFCLKP	71	PCIE_SOC2WLAN_CLK_P	
WLAN_PCIE_REFCLKN	70	PCIE_SOC2WLAN_CLK_N	
WL_UART_RX	50	WL_UART_RX	
WL_UART_TX	49		

C7589 0.1UF 20% 6.3V X5R-CERM 01005: PCIE_WLAN2SOC_RX_P
C7590 0.1UF 20% 6.3V X5R-CERM 01005: PCIE_WLAN2SOC_RX_N

PP7590 P4MM SM (PP) 1
PP7591 P4MM SM (PP) 1 WL_UART_TX

BOOTSTRAP CONFIGURATION

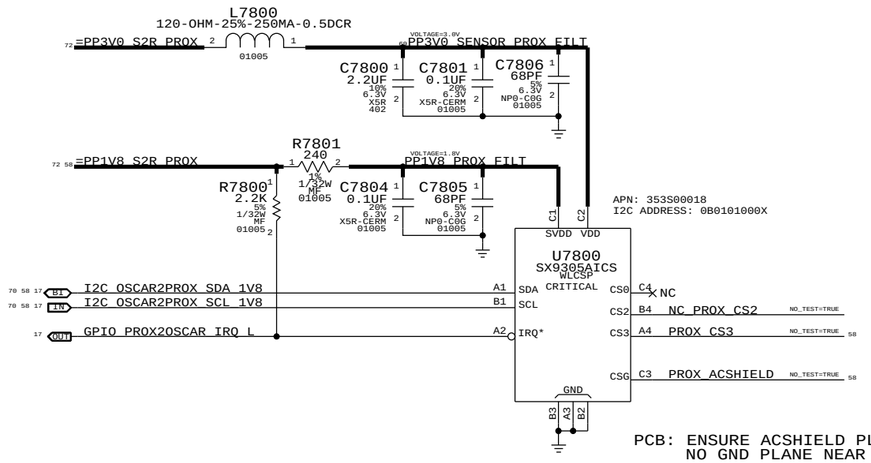
PP_1V8_S2R_VDDIO_WLAN_BT
R7586 10K 5% 1/32W MF 01005
R7587 10K 5% 1/32W MF 01005
R7590 10K 5% 1/32W MF 01005: GPIO_PMU2WLAN_REG_ON → WLAN_REG_RC
C7588 4.7UF 20% 6.3V X5R-CERM1 402
R7585 10K 5% 1/32W MF 01005

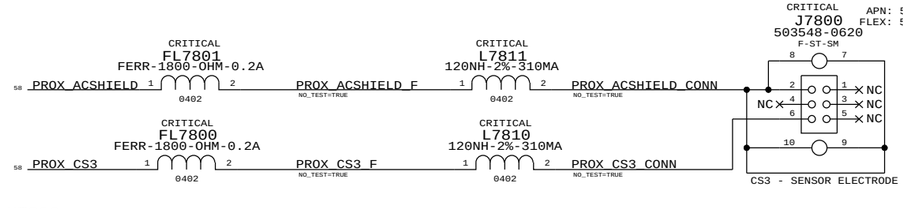
GPIO 10 → WLAN_GPIO_10
GPIO 09 → WLAN_GPIO_9
GPIO 08 → WLAN_GPIO_8

GPIO [10:8] = 011 FOR PCIE

C7592 0.01UF 10% 6.3V X5R 01005
U7503 74AUC1G126 BGA-Y2P: OSCAR2RADIO_CONTEXT_A → WLAN_GPIO_9
C1

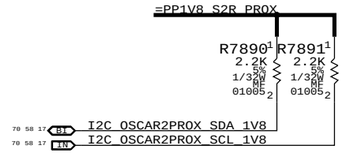
LAST UPDATED: 11/6/2013





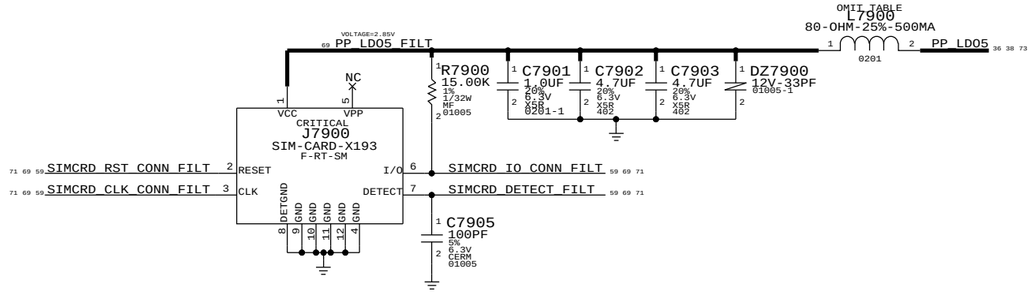
PCB: ENSURE ACSHIELD PLANE UNDER U7800
NO GND PLANE NEAR PROX_CS NETS.

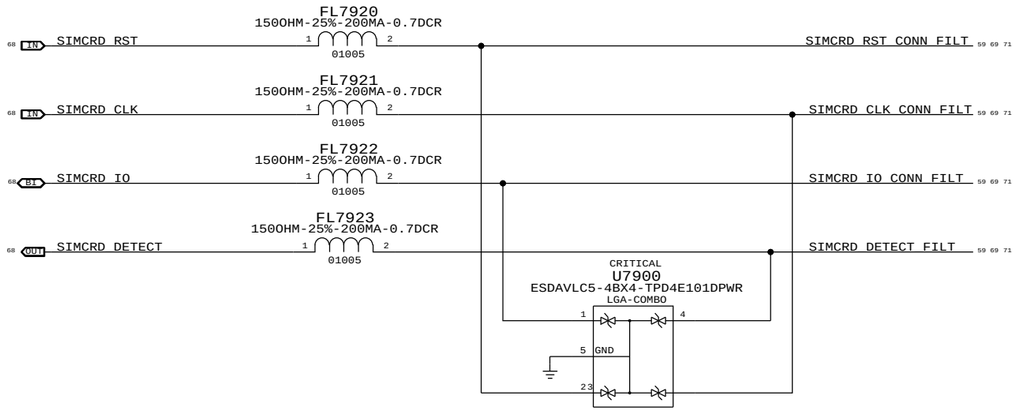
PCB: ACSHIELD NEEDS TO BE A PLANE UNDER
PROX_CS NETS AND ALSO TIE TO CONNECTOR.

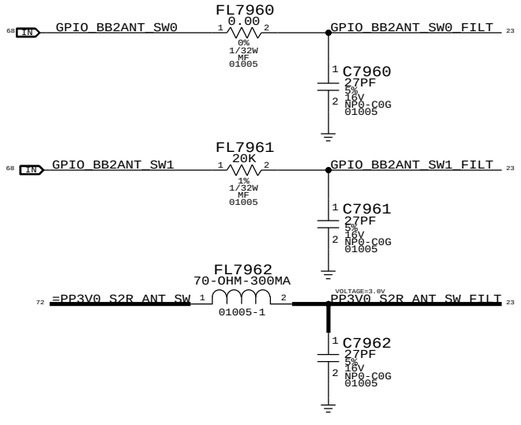


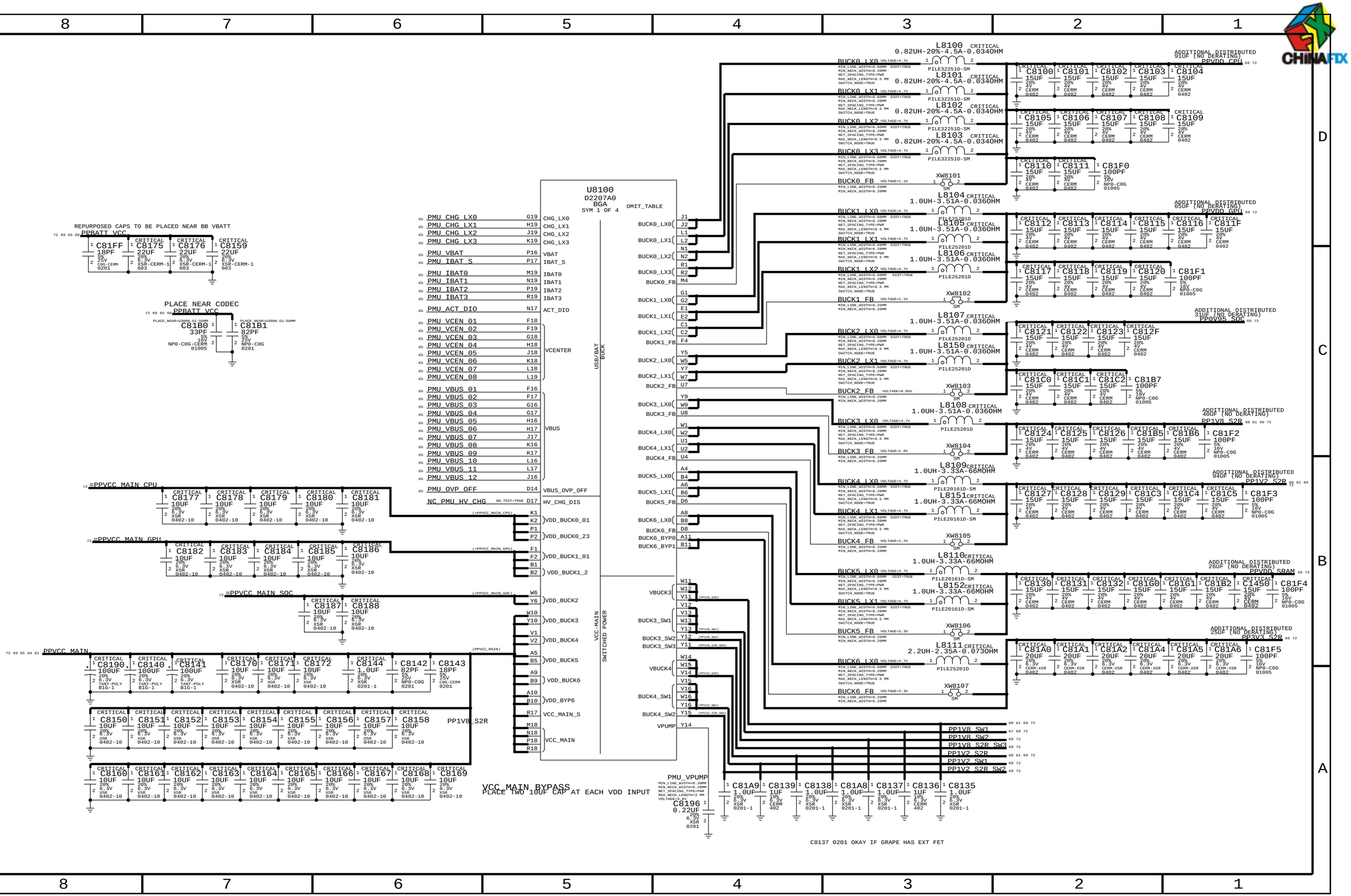
SIM CARD AND ANTENNA SWITCH FILTERS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S00018	1	FERRITE,800HM,25%,500MA,0.18DCR	L7900	CRITICAL	








U8100
D2207A0
BGA
SYM 1 OF 4
OMIT_TABLE
USB/BAT
BUCK
VCC-MAIN
SWITCHED POWER
PMU_CHG_LX0
PMU_CHG_LX1
PMU_CHG_LX2
PMU_CHG_LX3
PMU_VBAT
PMU_IBAT_S
PMU_IBAT0
PMU_IBAT1
PMU_IBAT2
PMU_IBAT3
PMU_ACT_DIO
PMU_VCEN_01
PMU_VCEN_02
PMU_VCEN_03
PMU_VCEN_04
PMU_VCEN_05
PMU_VCEN_06
PMU_VCEN_07
PMU_VCEN_08
PMU_VBUS_01
PMU_VBUS_02
PMU_VBUS_03
PMU_VBUS_04
PMU_VBUS_05
PMU_VBUS_06
PMU_VBUS_07
PMU_VBUS_08
PMU_VBUS_09
PMU_VBUS_10
PMU_VBUS_11
PMU_VBUS_12
PMU_OVP_OFF
NC_PMU_HV_CHG
VCENTER
VBUS
VBUS_OVP_OFF
HV_CHG_DIS
VDD_BUCK0_01
VDD_BUCK0_23
VDD_BUCK1_01
VDD_BUCK1_2
VDD_BUCK2
VDD_BUCK3
VDD_BUCK4
VDD_BUCK5
VDD_BUCK6
VDD_BYP6
VCC_MAIN_S
VCC_MAIN
L8100 CRITICAL 0.82UH-20%-4.5A-0.034OHM
L8101 CRITICAL 0.82UH-20%-4.5A-0.034OHM
L8102 CRITICAL 0.82UH-20%-4.5A-0.034OHM
L8103 CRITICAL 0.82UH-20%-4.5A-0.034OHM
L8104 CRITICAL 1.0UH-3.51A-0.036OHM
L8105 CRITICAL 1.0UH-3.51A-0.036OHM
L8106 CRITICAL 1.0UH-3.51A-0.036OHM
L8107 CRITICAL 1.0UH-3.51A-0.036OHM
L8150 CRITICAL 1.0UH-3.51A-0.036OHM
L8108 CRITICAL 1.0UH-3.51A-0.036OHM
L8109 CRITICAL 1.0UH-3.33A-66MOHM
L8151 CRITICAL 1.0UH-3.33A-66MOHM
L8110 CRITICAL 1.0UH-3.33A-66MOHM
L8152 CRITICAL 1.0UH-3.33A-66MOHM
L8111 CRITICAL 2.2UH-2.35A-0.073OHM
PILE32251D-SM
PILE20161D-SM
PILE25201D
XW8101
XW8102
XW8103
XW8104
XW8105
XW8106
XW8107
ADDITIONAL DISTRIBUTED 910UF (NO DERATING) PPVDD_CPU
ADDITIONAL DISTRIBUTED 65UF (NO DERATING) PPVDD_GPU
ADDITIONAL DISTRIBUTED 31UF (NO DERATING) PP0V95_SOC
ADDITIONAL DISTRIBUTED 40UF (NO DERATING) PP1V8_S2R
ADDITIONAL DISTRIBUTED 94UF (NO DERATING) PP1V2_S2R
ADDITIONAL DISTRIBUTED 26UF (NO DERATING) PPVDD_SRAM
ADDITIONAL DISTRIBUTED 25UF (NO DERATING) PP3V3_S2R
REPURPOSED CAPS TO BE PLACED NEAR BB VBATT
PPBATT_VCC
C81FF 18PF 5% 25V C0G-CERM 0201
C8175 22UF 20% 6.3V X5R-CERM-1 0603
C8176 22UF 20% 6.3V X5R-CERM-1 0603
C8159 22UF 20% 6.3V X5R-CERM-1 0603
PLACE NEAR CODEC
PPBATT_VCC
C81B0 33PF 5% 16V NP0-C0G 01005
C81B1 82PF 5% 25V NP0-C0G 0201
=PPVCC_MAIN_CPU
C8177 C8178 C8179 C8180 C8181 10UF 20% 6.3V X5R 0402-10
=PPVCC_MAIN_GPU
C8182 C8183 C8184 C8185 C8186 10UF 20% 6.3V X5R 0402-10
=PPVCC_MAIN_SOC
C8187 C8188 10UF 20% 6.3V X5R 0402-10
PPVCC_MAIN
C8190 C8140 C8141 100UF 20% 6.3V TANT-POLY B1G-1
C8170 C8171 C8172 10UF 20% 6.3V X5R 0402-10
C8144 1.0UF 20% 6.3V X5R 0201-1
C8142 82PF 5% 25V NP0-C0G 0201
C8143 18PF 5% 25V C0G-CERM 0201
C8150 C8151 C8152 C8153 C8154 C8155 C8156 C8157 C8158 10UF 20% 6.3V X5R 0402-10
PP1V8_S2R
C8160 C8161 C8162 C8163 C8164 C8165 C8166 C8167 C8168 C8169 10UF 20% 6.3V X5R 0402-10
VCC_MAIN_BYPASS
PLACE TWO 10UF CAP AT EACH VDD INPUT
PMU_VPUMP
C8196 0.22UF 20% 6.3V X5R 0201
C81A9 C8139 C8138 C81A8 C8137 C8136 C8135 1.0UF 20% 6.3V X5R 0201-1
C8137 0201 OKAY IF GRAPE HAS EXT FET
PP1V8_SW1
PP1V8_SW2
PP1V8_S2R_SW3
PP1V2_S2R
PP1V2_SW1
PP1V2_S2R_SW2
C8100 C8101 C8102 C8103 C8104 15UF 20% 4V CERM 0402
C8105 C8106 C8107 C8108 C8109 15UF 20% 4V CERM 0402
C8110 C8111 15UF 20% 4V CERM 0402
C81F0 100PF 5% 16V NP0-C0G 01005
C8112 C8113 C8114 C8115 C8116 C811F 15UF 20% 4V CERM 0402
C8117 C8118 C8119 C8120 15UF 20% 4V CERM 0402
C81F1 100PF 5% 16V NP0-C0G 01005
C8121 C8122 C8123 C812F 15UF 20% 4V CERM 0402
C81C0 C81C1 C81C2 15UF 20% 4V CERM 0402
C81B7 100PF 5% 16V NP0-C0G 01005
C8124 C8125 C8126 C81B5 C81B6 15UF 20% 4V CERM 0402
C81F2 100PF 5% 16V NP0-C0G 01005
C8127 C8128 C8129 C81C3 C81C4 C81C5 15UF 20% 4V CERM 0402
C81F3 100PF 5% 16V NP0-C0G 01005
C8130 C8131 C8132 C81G0 C81G1 C81B2 C1450 15UF 20% 4V CERM 0402
C81F4 100PF 5% 16V NP0-C0G 01005
C81A0 C81A1 C81A2 C81A4 C81A5 C81A6 20UF 20% 6.3V CERM-X5R 0402
C81F5 100PF 5% 16V NP0-C0G 01005

PCB: ADD A VIA PER PIN FOR ALL VSS_* AND VSSA_* PINS

U8100
D2207A0
BGA
SYM 4 OF 4
OMIT_TABLE

VSS_BUCK01: H1, H2
VSS_BUCK1_12: D1, D2
VSS_BUCK0_12: M1, M2
VSS_BUCK2: W4, Y4
VSS_BUCK4: Y1, Y2, Y3
VSS_BUCK5: A3, B3
VSS_BUCK23: W8, Y8
VSS_BUCK56: A7, B7
VSS_BUCK04: T1, T2
VSS_WLED: D18, D19
VSS_LCM: B18
VSS: A1, A2, A19, C3, C4, C5, C6, C8, C11, C14, D3, D12, D13, E3, E15, E17, F3, F7, F8, F9, F10, F11, F12, F13, F15, G3, G7, G8, G9, G10, G11, G12, G13, G15, H3, H7, H8, H9, H10, H11, H12, H13, H15, J3, J7, J8, J9, J10, J11, J12, J13, K3, K7, K8, K9, K10, K11, K12, K13, K15, L3, L7, L8, L9, L10, L11, L12, L13, L15, M3, M7, M8, M9, M10, M11, M12, M13, M16, N3, N7, N8, N9, N10, N11, N12, N13, N15, P3, P7, P8, P9, P10, P11, P12, P13, P15, R3, R7, R8, R9, R10, R11, R12, R13, R15, T3, T8, T10, U3, U9, U19, V3, V5, V6, V7, V9, W3, Y19

VOLTAGE=0V

0.22UF 4.7UF 10UF

LDO INPUTS

PP1V8_S2R — 1 CAP PER PIN
- C8200 1UF 10% 6.3V CERM 402
- C8203 1UF 10% 6.3V CERM 402

PP1V2_S2R
- C8201 1UF 10% 6.3V CERM 402

PPVCC_MAIN → VDD_LDO1_3_4 V17, VDD_LDO2 C13, VDD_LDO5 B13, VDD_LDO6 B12, VDD_LDO7 B14, VDD_LDO8 W18, VDD_LDO9 B16, VDD_LDO10 B17, VDD_LDO11 C15, VDD_LDO13 W17, VDD_LDO14 C16

U8100
D2207A0
BGA OMIT_TABLE
SYM 2 OF 4

LDO INPUT / LDO

WLED_LX_A
=PPLED_PMU_OUT_A D16
LED_PMU_1_A E14
LED_PMU_2_A F14
LED_PMU_3_A G14
LED_PMU_4_A H14
LED_PMU_5_A J14
LED_PMU_6_A J15

WLED_LX_B
=PPLED_PMU_OUT_B E16
LED_PMU_1_B K14
LED_PMU_2_B L14
LED_PMU_3_B M14
LED_PMU_4_B M15
LED_PMU_5_B N14
LED_PMU_6_B P14

WLED_LXA0 C18, WLED_LXA1 C19, VOUT_WLED_A E18, WLED1_A, WLED2_A, WLED3_A, WLED4_A, WLED5_A, WLED6_A
WLED_LXB0, WLED_LXB1 E19, VOUT_WLED_B, WLED1_B, WLED2_B, WLED3_B, WLED4_B, WLED5_B, WLED6_B

LCD BACKLIGHT LCM/GRAPE

XTAL

LDO OUTPUTS

VLDO1	U18 (50MA; 2.5-3.3V)	PP3V0_S2R_HALL	61 69 72
VLDO2	C12 (100MA; 1.65-1.885V)	PP1V7_VA_VCP	61 69 72
VLDO3	V18 (50MA; 2.5-3.3V)	PP3V0_S2R_SENSOR	61 69 72
VLDO4	T19 (50MA; 2.5-3.3V)	PP3V0_ALS	61 69 72
VLDO5	A13 (100MA; 2.5-3.6V)	PP3V1_S2R_MESA	61 69 72
VLDO6	A12 (150MA; 2.5-3.6V)	PP3V3_ACC	61 69 72
VLDO7	A14 (300MA; 1.7-3.0V)	PP3V0_S2R_TRISTAR	61 69 72
VLDO8	Y18 (300MA; 1.7-3.0V)	PP3V0_MISC	61 69 72
VLDO9	A16 (300MA; 1.2-3.0V)	PP1V25_CAM	61 69 72
VLDO10	A17 (150MA; 0.6-1.2V)	PP1V0_SOC	61 69 72
VLDO11	B15 (300MA; 1.7-3.0V)	PP2V6_CAM_AF	61 69 72
VLDO13	Y17 (300MA; 1.7-3.0V)	PP2V9_CAM	61 69 72
VLDO14	A15 (300MA; 1.2-3.0V)	PP1V8_SPARE	61 69 72
ON_BUF	T13 (10MA; 1.8V; ON_BUFF)	PP1V8_ALWAYS	61 69 72

VDD_LCM_SW	C17 (NOTE: 2MHZ)	=PPVCC_MAIN_VDD_LCM	72
VDD_BOOST_LCM	A18 VOLTAGE=6.0V	PP6V0_LCM_HI	63 70
BOOST_LCM_LX	B19 VOLTAGE=6.0V	LCM_LX	63
LCM_FB	D15 VOLTAGE=6.0V	PP6V0_LCM_VBOOST	63 69
VDD_LCM	U17		
VLCM1	T16 (100MA; 5.0-6.0V)	PP5V25_GRAPE	69 72
VLCM2	T18 (100MA; 5.0-6.0V) NO_TEST=TRUE	NC_VLCM2	
LCM2_EN	D7		
VLCM3	T17 (5MA; 5.0-6.0V) NO_TEST=TRUE	NC_VLCM3	

C8212 10UF 20% 25V X5R_CERM 0603

XTAL1 W19 PMU_XTAL
XTAL2 V19 PMU_EXTAL

CRITICAL Y8200 32.768K-20PPM-12.5PF 2012-1
CRITICAL C8215 18PF 5% 25V C0G-CERM 0201
CRITICAL C8216 18PF 5% 25V C0G-CERM 0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392		Y8200	RDAR://PROBLEM/9936684
138S0703	138S0648		C8235	AND ~15X MORE REFDES

LDO BYPASS

PP3V0_S2R_HALL	C8232 10UF 20% 6.3V X5R 0402-10	C8235 4.7UF 20% 6.3V X5R 402	C8233 20UF 20% 6.3V CERM-X5R 0402	C8234 4.7UF 20% 6.3V X5R 402	C82A3 2.2UF 10% 6.3V X5R 402	C8237 2.2UF 10% 6.3V X5R 402	C8231 10UF 20% 6.3V X5R 0402-10	C8230 2.2UF 10% 6.3V X5R 402
PP1V7_VA_VCP								
PP3V0_S2R_SENSOR								
PP3V0_ALS								
PP3V1_S2R_MESA								
PP3V3_ACC								
PP3V0_S2R_TRISTAR								

PP3V0_MISC	C8242 20% 6.3V X5R 0201	C8270 20% 6.3V X5R 402	C8241 20% 6.3V X5R 0402-10	C8240 10UF 20% 6.3V X5R 0402-10	C8239 4.7UF 20% 6.3V X5R 402	C82A9 100PF 10% 16V NP0-C0G 01005	C8238 4.7UF 20% 6.3V X5R 402	C8271 10UF 20% 6.3V X5R 0402-10
PP1V25_CAM								
PP1V0_SOC								
PP2V6_CAM_AF								
PP2V9_CAM								
PP1V8_SPARE								
PP1V8_ALWAYS								

I2C ADDRESS: 0111100X (0X78)

U8100 OMIT_TABLE
D2207A0
BGA
SYM 3 OF 4

BUTTON1	C9	GPIO_BTN_HOME_L	IN	33 6 5	
BUTTON2	C10	GPIO_BTN_ONOFF_L	IN	69 23 6 5	
BUTTON3	E8	NC_PMU_BTN3	NO_TEST=TRUE		
BUTTON4	E9	NC_PMU_BTN4	NO_TEST=TRUE		
ACC_DET	R4				
BRICK_ID	R16	PMU_USB_BRICKID_R			
ADC_IN7	N16	ADC_IN7			
ADC_IN31	R14				
KEEPACT	D9	GPIO_SOC2PMU_KEEPACT	IN	6	
SHDN	U12	PMU_SHDWN	IN (INTERNAL PD)	67	
RESET_IN1	N6	WDOG_SOC2PMU_RESET_IN	IN (INTERNAL PD)	4	
RESET_IN2	P6	GPIO_TS2PMU_RESET	IN	25	
RESET_IN3	R6	SOCHOT1_L	IN	6	
RESET*	D10	RESET_SOC_L	OUT	70 69 68 25 10 5 4	
IRQ*	E4	GPIO_PMU2SOC_IRQ_L	OUT (PU IN SOC)	6	
SCL	E12	=I2C_SOC2PMU_SCL_1V8	IN	4	
SDA	E13	=I2C_SOC2PMU_SDA_1V8	BI	4	
DWI_CK	D11	DWI_SOC2PMU_CLK	IN (INTERNAL PD)	70 6	
DWI_DI	E11	DWI_SOC2PMU_DO	IN (INTERNAL PD)	70 6	
DWI_DO	E10	NC_PMU_DWI_DO	NO_TEST=TRUE		
TDEV1	V4	PA_NTC_P	NET_SPACING_TYPE=BOARD_TEMP	70 68	
TDEV2	V10		NET_SPACING_TYPE=BOARD_TEMP		
TDEV3	T11		NET_SPACING_TYPE=BOARD_TEMP		
TDEV4	T12		NET_SPACING_TYPE=BOARD_TEMP		
TDEV5	L5		NET_SPACING_TYPE=BOARD_TEMP		
TDEV6	T6		NET_SPACING_TYPE=BOARD_TEMP		
TDEV7	N4		NET_SPACING_TYPE=BOARD_TEMP		
TDEV8	P5		NET_SPACING_TYPE=BOARD_TEMP		
TBAT	T15	BATT_NTC		69 66	
TCAL	T14	PMU_TCAL		70	
IREF	U13	PMU_IREF	NET_SPACING_TYPE=ANALOG		
VREF	U16	PMU_VREF	NET_SPACING_TYPE=ANALOG		
VDD_REF	M17	PMU_VDD_REF	NET_SPACING_TYPE=ANALOG		
VDD_REF_A	U14		NET_SPACING_TYPE=ANALOG		
VDD_RTC	U15	PMU_VDD_RTC	NET_SPACING_TYPE=ANALOG		
OUT_32K	T9	NC_PMU_OUT_32K	NO_TEST=TRUE		
GPIO1	U6	CLK_PMU2OSCAR_32K_AND_RESET_L	OUT		17 69 70
GPIO2	U5	CLK_PMU2WLAN_32K	OUT		57 68 69 70
GPIO3	T7	GPIO_PMU2BT_REG_ON	OUT		57 68 69 70
GPIO4	M6	GPIO_PMU2WLAN_REG_ON	OUT		57 68 69 70
GPIO5	T5	GPIO_PMU2BBPMU_RESET_R_L	OUT		
GPIO6	T4	UART_BATT_HDQ			6 66
GPIO7	R5	GPIO_BT2PMU_HOST_WAKE	IN		57 68 70
GPIO8	P4	GPIO_WLAN2PMU_HOST_WAKE	IN		57 68 70
GPIO9	N5	GPIO_BB2PMU_HOST_WAKE_L	IN		68 69 70
GPIO10	M5	GPIO_CODEC2PMU_HS_IRQ_L	IN		22 69 70
GPIO11	L4	GPIO_HALL2PMU_IRQ0	IN		19 69
GPIO12	K5	GPIO_TS2SOC2PMU_IRQ	IN		6 25
GPIO13	J6	GPIO_HALL2PMU_IRQ1	IN		30
GPIO14	H4	PCIE_WLAN2PMU_WAKE_L	IN		57 68
GPIO15	G5	GPIO_PMU2CODEC_RESET_L (USE INTERNAL PU)	OUT		22
GPIO16	F5	GPIO_OSCAR2PMU_HOST_WAKE	IN		6 17
GPIO17	E5	GPIO_PMU2BB_VBUS_DET	OUT		68 69 71
GPIO18	E6	GPIO_PMU2LCD_PWREN	OUT		32
GPIO19	E7	NC_PMU_GPIO19	NO_TEST=TRUE		
GPIO20	D5	GPIO_DEVBRD2PMU_WAKE_L	IN		69
GPIO21	D4	NC_PMU_GPIO21	NO_TEST=TRUE		
AMUX_A0	G6	PPVDD_CPU_SOC_SENSE			13 70
AMUX_A1	F6	PPVDD_GPU_SOC_SENSE			13 70
AMUX_A2	H6	PPVDD_SRAM_SOC_SENSE			13 70
AMUX_A3	J5	ADC_BB2PMU_IMEAS_RADIO			68
AMUX_AY	G4	TP_AMUX_AY			70
AMUX_B0	L6	NC_PMU_AMUX_B0	NO_TEST=TRUE		
AMUX_B1	J4	NC_PMU_AMUX_B1	NO_TEST=TRUE		
AMUX_B2	K6	PPVDD_SOC_SOC_SENSE			12 70
AMUX_B3	K4	ADC_BB2PMU_IMEAS_QPOET			68
AMUX_BY	H5	TP_AMUX_BY			70
BUCK_LDO_UOV	U10	TP_BUCK_LDO_UOV			70
BUCK_SLPD_MUX	U11	TP_BUCK_SLPD_MUX			70
PRE_UVLO	V8	SOCHOT0_L_R		70	
SYS_ALIVE*	C7	(SYS_ALIVE)			

BLOCKS: ANALOG INPUT, REFRENCES; DIGITAL INPUT, 32K CLK; WDOG; RESET; GPIO; I2C & DWI; TEMPERATURE; ANALOG MUX

R8399 0.00 1% 1/20W MF 0201
C8301 0.01UF 10% 6.3V X5R 01005
C8302 0.01UF 10% 6.3V X5R 01005

C8305 0.1UF 10% 6.3V CERM-X5R 0201
R8303 200K 0.5% 1/20W MF 0201
C8306 0.1UF 10% 6.3V CERM-X5R 0201
C8307 1UF 10% 10V X5R 402-1
C8308 1UF 20% 10V X5R 0201

R8330 1.00K 5% 1/32W MF 01005
GPIO_PMU2BBPMU_RESET_L OUT 68 69 70 71

C8340 100PF 5% 16V NP0-C0G 01005
R8340 3.92K 0.1% 0201 1/20W MF CRITICAL
RESISTOR FOR TEMP CALIBRATION

=PP1V8_ALWAYS 6 11 72
=PP1V8_SOC 4 5 6 72
R8370 10K 5% 1/32W MF 01005 NOSTUFF
R8372 100K 5% 1/32W MF 01005
R8371 0.00 1/32W MF 01005
SOCHOT0_L OUT 6 69
SYS_ALIVE OUT 70

PLACE_XW_AND_CAP CLOSE TO PMU

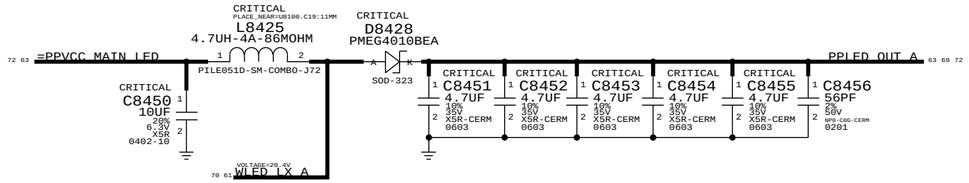
XW8328 PLACE_NEAR=U8100.V10:10MM
XW8321 PLACE_NEAR=U8100.T11:12MM
XW8322 PLACE_NEAR=U8100.T12:12MM
XW8323 PLACE_NEAR=U8100.L5:10MM
XW8324 PLACE_NEAR=U8100.T6:10MM
XW8325 PLACE_NEAR=U8100.N4:10MM
XW8326 PLACE_NEAR=U8100.P5:11MM

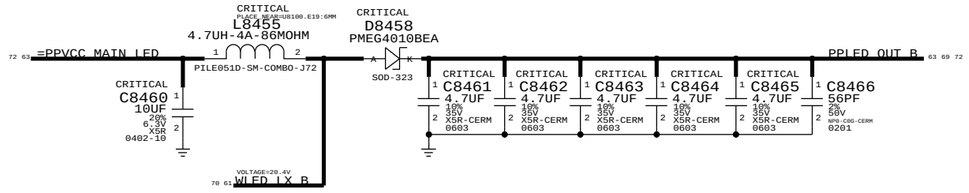
	R	C	BOARD_TEMP_P	BOARD_TEMP_N	PLACE_NEAR	NO_XNET_CONNECTION=TRUE
TEMP2 - NEAR SPEAKER AMPS	R8328 10KOHM-1%-0.31MA 0201	C8328 100PF 5% 16V NP0-C0G 01005	BOARD_TEMP2_P	BOARD_TEMP2_N	U3200.A1:12MM	U3200.A1:12MM
TEMP3 - NEAR WIFI	R8321 10KOHM-1%-0.31MA 0201	C8321 100PF 5% 16V NP0-C0G 01005	BOARD_TEMP3_P	BOARD_TEMP3_N	U7500.I33:10MM	U7500.I33:10MM
TEMP4 - NEAR REAR CAM	R8322 10KOHM-1%-0.31MA 0201	C8322 100PF 5% 16V NP0-C0G 01005	BOARD_TEMP4_P	BOARD_TEMP4_N	J2701.I3:10MM	J2701.I3:10MM
TEMP5 - NEAR NAND	R8323 10KOHM-1%-0.31MA 0201	C8323 100PF 5% 16V NP0-C0G 01005	BOARD_TEMP5_P	BOARD_TEMP5_N	U1800.B2:10MM	U1800.B2:10MM
TEMP6 - NEAR FRONT CAM	R8324 10KOHM-1%-0.31MA 0201	C8324 100PF 5% 16V NP0-C0G 01005	BOARD_TEMP6_P	BOARD_TEMP6_N	J3100.I1:10MM	J3100.I1:10MM
TEMP7 - NEAR PMU	R8325 10KOHM-1%-0.31MA 0201	C8325 100PF 5% 16V NP0-C0G 01005	BOARD_TEMP7_P	BOARD_TEMP7_N	U8100.H9:10MM	U8100.H9:10MM
TEMP8 - NEAR SOC	R8326 10KOHM-1%-0.31MA 0201	C8326 100PF 5% 16V NP0-C0G 01005	BOARD_TEMP8_P	BOARD_TEMP8_N	U0600.Y22:13MM	U0600.Y22:13MM

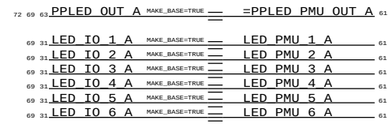
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0706	138S0739		C8308	
118S0764	118S0717		R8340	RDAR://PROBLEM/8380367
107S0150	107S0208		R8321-R8328	RDAR://PROBLEM/8380367

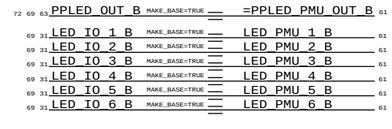
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1837	152S1789		L8425,L8455	RDAR://PROBLEM/13487208

BACKLIGHT CIRCUIT MOVED HERE TO PERMIT SYNCING WITH DESIGNS USING BEACON

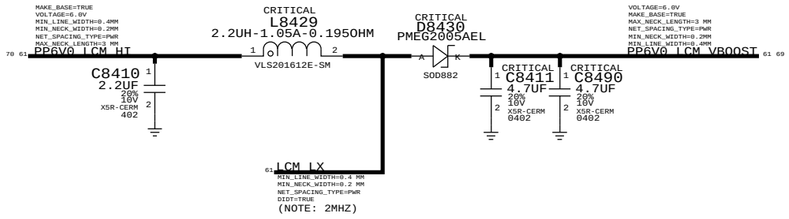


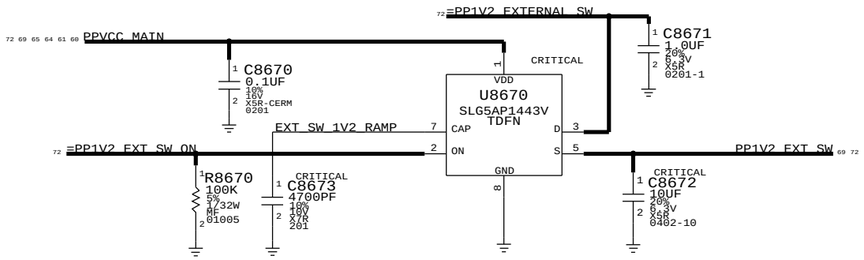


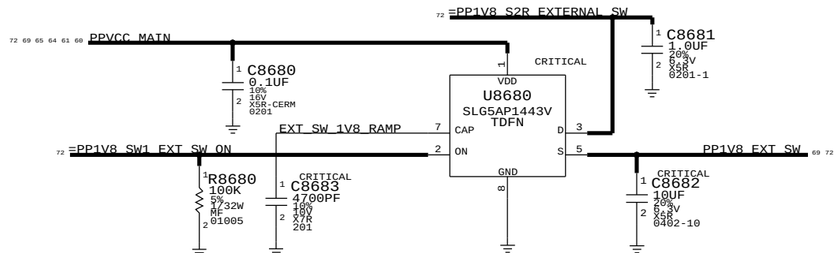




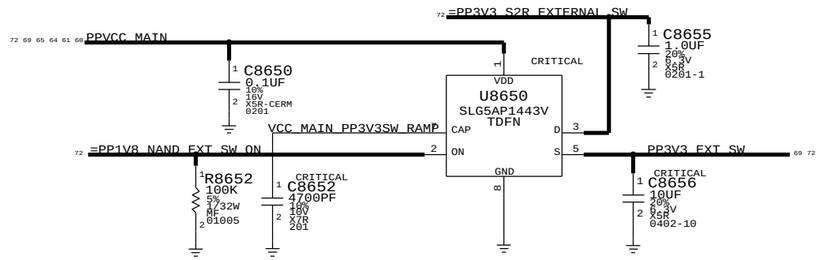
LCM BOOST MOVED HERE TO PERMIT SYNCING WITH DESIGNS USING KONA



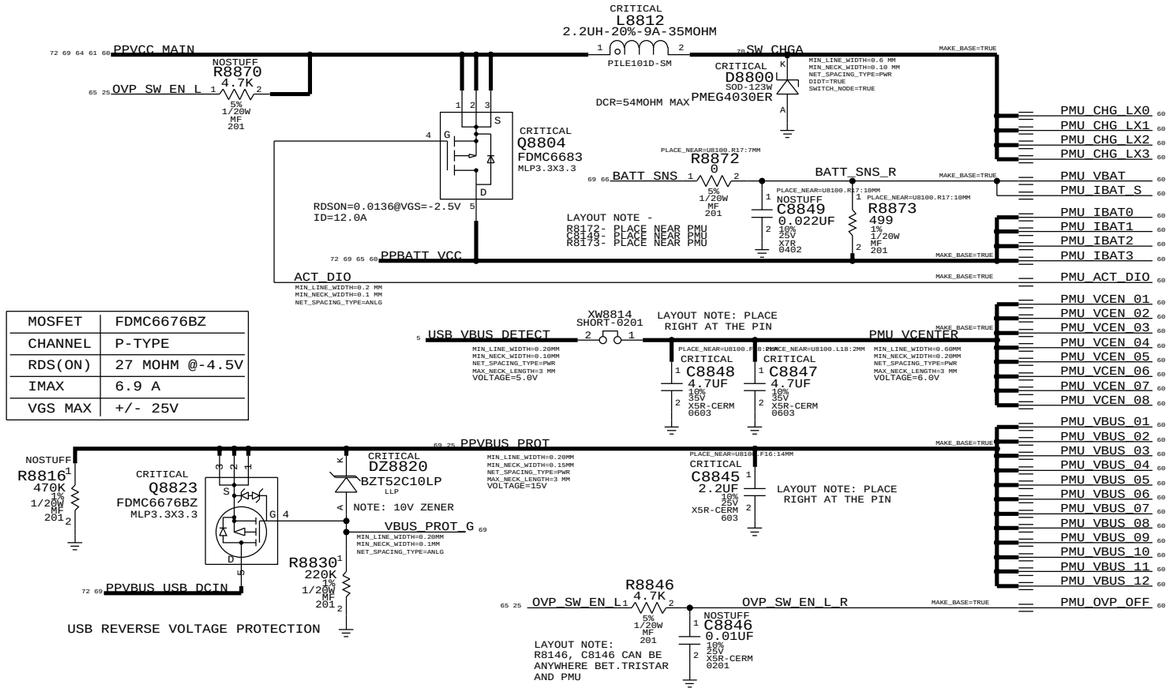




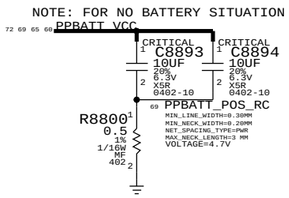
BUCK6 POWER IS ON IN HIBERNATE DUE TO WIFI PAS
SWITCH NEEDED TO GATE POWER TO NAND AND SOC

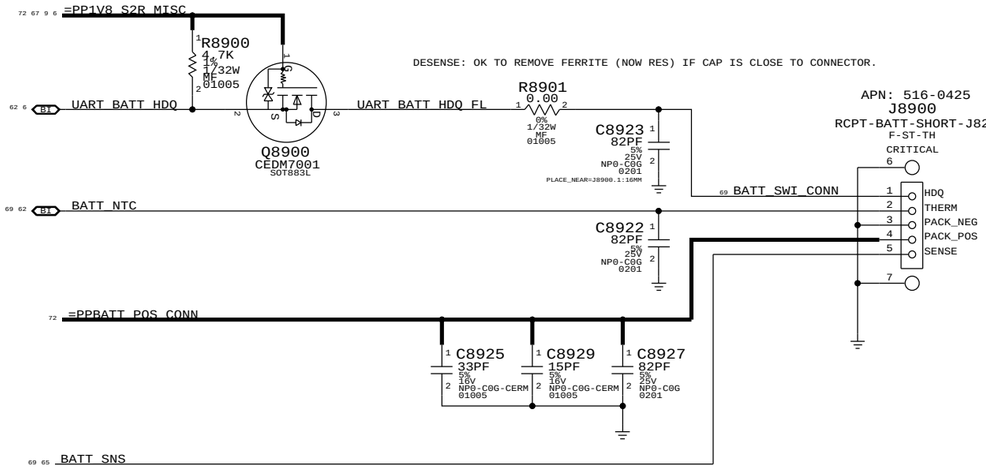


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1192	376S0929	?	Q8823	RDAR://PROBLEM/16073848



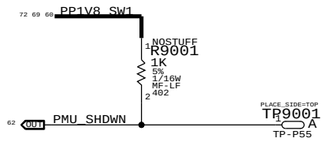
NOTE: FOR NO BATTERY SITUATION

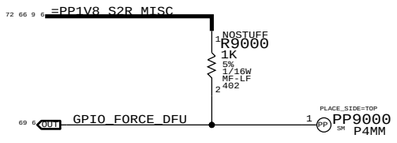




PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0823		FL8900	RDAR://PROBLEM/11282371

DEBUG RESET ACCESS





CELLULAR AND WLAN/BT ALIASES

BASEBAND

GPIO

71 69 6	IN	GPIO_SOC2BB_RADIO_ON_L	MAKE_BASE=TRUE	RADIO_ON_L	OUT 35 37
69 6	IN	GPIO_SOC2BB_RESET_L	MAKE_BASE=TRUE	BB_RST_L	OUT 35 37
69 6	OUT	GPIO_BB2SOC_RESET_DET_L	MAKE_BASE=TRUE	BB_RESET_DET_L	IN 35 40
71 70 69 62	IN	GPIO_PMU2BBPMU_RESET_L	MAKE_BASE=TRUE	RF_PMIC_RESET_L	OUT 35 37
71 6	IN	GPIO_SOC2BB_WAKE_MODEM	MAKE_BASE=TRUE	AP_WAKE_MODEM	OUT 40
70 69 62 25 10 5 4	OUT	RESET_SOC_L	MAKE_BASE=TRUE	RESET_1V8_L	IN 35
71 6	IN	GPIO_SOC2BB_COREDUMP	MAKE_BASE=TRUE	BB_CORE_DUMP	OUT 40
6	BI	GPIO_BB_IPC	MAKE_BASE=TRUE	BB_IPC_GPIO	BI 40
71 6	OUT	GPIO_BB2SOC_GPS_SYNC	MAKE_BASE=TRUE	BB_GPS_SYNC	IN 40
70 69 62	OUT	GPIO_BB2PMU_HOST_WAKE_L	MAKE_BASE=TRUE	BB_WAKE_HOST	IN 35 40

UART

71 25 6	OUT	UART_BB2SOC_TX	MAKE_BASE=TRUE	BB_UART_TXD	IN 35 40
71 25 6	IN	UART_SOC2BB_TX	MAKE_BASE=TRUE	BB_UART_RXD	OUT 35 40
71 6	OUT	UART_BB2SOC_RTS_L	MAKE_BASE=TRUE	BB_UART_RTS_L	IN 40
71 6	IN	UART_SOC2BB_RTS_L	MAKE_BASE=TRUE	BB_UART_CTS_L	OUT 40
71 17	IN	UART_OSCAR2BB_TX	MAKE_BASE=TRUE	BB_OTHER_RXD	OUT 40
71 17	OUT	UART_BB2OSCAR_TX	MAKE_BASE=TRUE	BB_OTHER_TXD	IN 40

HSIC

69 6	IN	HSIC_SOC2BB_HOST_RDY	MAKE_BASE=TRUE	BB_HOST_RDY	OUT 35 40
69 6	OUT	HSIC_BB2SOC_DEVICE_RDY	MAKE_BASE=TRUE	BB_DEVICE_RDY	IN 35 40
71 5	BI	HSIC_BB_DATA	MAKE_BASE=TRUE	50_BB_HSIC_DATA	BI 35 39
71 5	BI	HSIC_BB_STB	MAKE_BASE=TRUE	50_BB_HSIC_STROBE	BI 35 39

USB

71 69 62	IN	GPIO_PMU2BB_VBUS_DET	MAKE_BASE=TRUE	BB_USB_VBUS	OUT 35 39
71 25	BI	USB_BB_P	MAKE_BASE=TRUE	90_BB_USB_P	BI 35
71 25	BI	USB_BB_N	MAKE_BASE=TRUE	90_BB_USB_N	BI 35

SIM CARD

59	IN	SIMCRD_DETECT	MAKE_BASE=TRUE	BB_SIM_DETECT	OUT 39 40
59	OUT	SIMCRD_RST	MAKE_BASE=TRUE	BB_SIM_RESET	IN 40
59	OUT	SIMCRD_CLK	MAKE_BASE=TRUE	BB_SIM_CLK	IN 40
59	BI	SIMCRD_IO	MAKE_BASE=TRUE	BB_SIM_DATA	BI 40

ADC

62	OUT	ADC_BB2PMU_IMEAS_RADIO	MAKE_BASE=TRUE	RADIO_TO_PMU_ADC_IMEAS_RADIO	IN 35
62	OUT	ADC_BB2PMU_IMEAS_QPOET	MAKE_BASE=TRUE	RADIO_TO_PMU_ADC_IMEAS_QPOET	IN 44

POWER

72		=PPBATT_VCC_BB		PP_BATT_VCC	35 44 53 73

LOWER ANT CTRL

59	OUT	GPIO_BB2ANT_SW0	MAKE_BASE=TRUE	BB_ANTSW_GPIO0	IN 40
59	OUT	GPIO_BB2ANT_SW1	MAKE_BASE=TRUE	BB_ANTSW_GPIO1	IN 40

WLAN/BT

GPIO

70 69 68 62 57	IN	CLK_PMU2WLAN_32K	MAKE_BASE=TRUE	CLK_PMU2WLAN_32K	OUT 57 62 68 69 70
70 69 68 62 57	IN	GPIO_PMU2BT_REG_ON	MAKE_BASE=TRUE	GPIO_PMU2BT_REG_ON	OUT 57 62 68 69 70
70 69 68 62 57	IN	GPIO_PMU2WLAN_REG_ON	MAKE_BASE=TRUE	GPIO_PMU2WLAN_REG_ON	OUT 57 62 68 69 70
70 68 57 9	IN	GPIO_SOC2BT_WAKE	MAKE_BASE=TRUE	GPIO_SOC2BT_WAKE	OUT 9 57 68 70
70 9	IN	GPIO_SOC2WLAN_WAKE	MAKE_BASE=TRUE	GPIO_SOC2WLAN_PCIE_DEV_WAKE	OUT 57
70 68 62 57	OUT	GPIO_BT2PMU_HOST_WAKE	MAKE_BASE=TRUE	GPIO_BT2PMU_HOST_WAKE	IN 57 62 68 70
70 68 62 57	OUT	GPIO_WLAN2PMU_HOST_WAKE	MAKE_BASE=TRUE	GPIO_WLAN2PMU_HOST_WAKE	IN 57 62 68 70

PCIE

70 9	IN	PCIE_SOC2WLAN_RESET_L	MAKE_BASE=TRUE	PCIE_SOC2WLAN_PERST	OUT 57
70 9	OUT	PCIE_WLAN2SOC_CLKREQ_L	MAKE_BASE=TRUE	PCIE_WLAN2SOC_CLKREQ	IN 57
68 62 57	OUT	PCIE_WLAN2PMU_WAKE_L	MAKE_BASE=TRUE	PCIE_WLAN2PMU_WAKE_L	IN 57 62 68
70 68 57 9	IN	PCIE_SOC2WLAN_CLK_P	MAKE_BASE=TRUE	PCIE_SOC2WLAN_CLK_P	OUT 9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_CLK_N	MAKE_BASE=TRUE	PCIE_SOC2WLAN_CLK_N	OUT 9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_TX_P	MAKE_BASE=TRUE	PCIE_SOC2WLAN_TX_P	OUT 9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_TX_N	MAKE_BASE=TRUE	PCIE_SOC2WLAN_TX_N	OUT 9 57 68 70
70 9	OUT	PCIE_WLAN2SOC_TX_P	MAKE_BASE=TRUE	PCIE_WLAN2SOC_RX_P	IN 57
70 9	OUT	PCIE_WLAN2SOC_TX_N	MAKE_BASE=TRUE	PCIE_WLAN2SOC_RX_N	IN 57
70		PCIE_WLAN2SOC_TX_C_P	MAKE_BASE=TRUE	PCIE_TX_P	57
70		PCIE_WLAN2SOC_TX_C_N	MAKE_BASE=TRUE	PCIE_TX_N	57

TO KEEP PP NAMING CONSISTENT

UART

70 68 57 6	IN	UART_SOC2BT_TX	MAKE_BASE=TRUE	UART_SOC2BT_TX	OUT 6 57 68 70
70 68 57 6	IN	UART_SOC2BT_RTS_L	MAKE_BASE=TRUE	UART_SOC2BT_RTS_L	OUT 6 57 68 70
70 6	OUT	UART_BT2SOC_TX	MAKE_BASE=TRUE	UART_BT2SOC_RX	IN 57
70 6	OUT	UART_BT2SOC_RTS_L	MAKE_BASE=TRUE	UART_BT2SOC_CTS_L	IN 57
70 68 57 6	IN	UART_SOC2WLAN_TX	MAKE_BASE=TRUE	UART_SOC2WLAN_TX	OUT 6 57 68 70
70 68 57 6	IN	UART_SOC2WLAN_RTS_L	MAKE_BASE=TRUE	UART_SOC2WLAN_RTS_L	OUT 6 57 68 70
70 6	OUT	UART_WLAN2SOC_TX	MAKE_BASE=TRUE	UART_WLAN2SOC_RX	IN 57
70 6	OUT	UART_WLAN2SOC_RTS_L	MAKE_BASE=TRUE	UART_WLAN2SOC_CTS_L	IN 57
		TP_WL_UART_RX	MAKE_BASE=TRUE	WL_UART_RX	57
		TP_WL_UART_TX	MAKE_BASE=TRUE	WL_UART_TX	57

RESOLVES CKPLUS ERROR IN NAME

I2S

70 6	OUT	I2S_BT2SOC_DOUT	MAKE_BASE=TRUE	I2S_BT2SOC_DIN	IN 57
70 68 57 6	IN	I2S_SOC2BT_DOUT	MAKE_BASE=TRUE	I2S_SOC2BT_DOUT	OUT 6 57 68 70
70 68 57 6	IN	I2S_SOC2BT_BCLK	MAKE_BASE=TRUE	I2S_SOC2BT_BCLK	OUT 6 57 68 70
70 68 57 6	IN	I2S_SOC2BT_LRCK	MAKE_BASE=TRUE	I2S_SOC2BT_LRCK	OUT 6 57 68 70

OSCAR CONTEXT

17	IN	GPIO_OSCAR2WLAN_CONTEXT_A	MAKE_BASE=TRUE	OSCAR2RADIO_CONTEXT_A	OUT 57 70
17	IN	GPIO_OSCAR2WLAN_CONTEXT_B	MAKE_BASE=TRUE	OSCAR2RADIO_CONTEXT_B	OUT 57 70

JTAG

70	OUT	TP_JTAG_WLAN_TMS	MAKE_BASE=TRUE	JTAG_WLAN_TMS	IN 57
70	OUT	TP_JTAG_WLAN_TRST	MAKE_BASE=TRUE	JTAG_WLAN_TRST	IN 57

POWER

72		=PPVCC_MAIN_WLAN		PP_VCC_MAIN_WLAN	57
72		=PP3V3_S2R_WIFI_PA		PP_3V3_S2R_WIFI_PA	56 57
72		=PP1V8_S2R_VDDIO_WLAN_BT		PP_1V8_S2R_VDDIO_WLAN_BT	57 73

NO CONNECT

		NC_WLAN_GPIO3	NO_TEST=TRUE MAKE_BASE=TRUE	BT_EXT_SYNC	OUT 57
		NC_WLAN_GPIO5	NO_TEST=TRUE MAKE_BASE=TRUE	BT_EXT_CLK	OUT 57

SLOTS FOR RADIO FENCE

SL9110 TH-NSP — SL-1.1X0.4-1.4X0.7 — SL9111 TH-NSP — SL-1.1X0.4-1.4X0.7

NTC FOR BB

CRITICAL
R9127
10KOHM-1%-0.31MA
0201
PLACE_NEAR=U5401.A2:11MM
NO_XNET_CONNECTION=TRUE
(TEMP1 - NEAR BB)

C9127
100PF
5%
16V
NP0-C0G
01005
PLACE_NEAR=U8100.V4:11MM
NO_XNET_CONNECTION=TRUE

PA_NTC_P — 62 70
PA_NTC_N — XW9127 SM — PLACE_NEAR=U8100.V4:11MM

SMT TEST FIXTURE TP

POWER - BUCKS

MUST HAVE

PPVDD_CPU	FUNC_TEST=TRUE	60 72
PPVDD_GPU	FUNC_TEST=TRUE	60 72
PP0V95_SOC	FUNC_TEST=TRUE	60 72
PP1V8_S2R	FUNC_TEST=TRUE	60 61 72
PP1V8_SW1	FUNC_TEST=TRUE	60 67 72
PP1V8_SW1_FOREHEAD	FUNC_TEST=TRUE	72
PP1V8_EXT_SW	FUNC_TEST=TRUE	64 72
PP1V8_SW2	FUNC_TEST=TRUE	60 72
PP1V8_GRAPE_EXT_SW	FUNC_TEST=TRUE	30 72
PP1V8_S2R_SW3	FUNC_TEST=TRUE	60 72
PP1V2_S2R	FUNC_TEST=TRUE	60 61 72
PP1V2_SW1	FUNC_TEST=TRUE	60 72
PP1V2_EXT_SW	FUNC_TEST=TRUE	64 72
PP1V2_S2R_SW2	FUNC_TEST=TRUE	60 72
PPVDD_SRAM	FUNC_TEST=TRUE	60 72
PP3V3_S2R	FUNC_TEST=TRUE	60 72
PP3V3_EXT_SW	FUNC_TEST=TRUE	64 72

POWER - LDOS

PP1V7_VA_VCP	FUNC_TEST=TRUE	61 72
PP3V0_S2R_SENSOR	FUNC_TEST=TRUE	61 72
PP3V0_ALS	FUNC_TEST=TRUE	61 72
PP3V3_ACC	FUNC_TEST=TRUE	61 72
PP3V0_S2R_TRISTAR	FUNC_TEST=TRUE	61 72
PP3V1_S2R_MESA	FUNC_TEST=TRUE	61 72
PP1V0_SOC	FUNC_TEST=TRUE	61 72
PP1V8_SPARE	FUNC_TEST=TRUE	61 72
PP3V0_S2R_HALL	FUNC_TEST=TRUE	61 72
PP3V0_MISC	FUNC_TEST=TRUE	61 72
PP1V25_CAM	FUNC_TEST=TRUE	61 72
PP2V6_CAM_AF	FUNC_TEST=TRUE	61 72
PP2V9_CAM	FUNC_TEST=TRUE	61 72

POWER - OTHER

MUST HAVE

PP1V8_ALWAYS	FUNC_TEST=TRUE	61 72
PPBATT_VCC	FUNC_TEST=TRUE	60 65 69 72
PPLED_OUT_A	FUNC_TEST=TRUE	63 72
PPLED_OUT_B	FUNC_TEST=TRUE	63 72
PP5V25_GRAPE	FUNC_TEST=TRUE	61 72
PP1V8_XTAL	FUNC_TEST=TRUE	11
PPVCC_MAIN	FUNC_TEST=TRUE	60 61 64 65 72
PPBATT_POS_RC	FUNC_TEST=TRUE	65
PP6V0_LCM_VBOOST	FUNC_TEST=TRUE	61 63
PPVBUS_USB_DCIN	FUNC_TEST=TRUE	65 72
PPVBUS_PROT	FUNC_TEST=TRUE	25 65
VBUS_PROT_G	FUNC_TEST=TRUE	65

POWER - CAMERA (FRONT)

MUST HAVE

PP1V2_CAM_FRONT_FILT	FUNC_TEST=TRUE	20 21
PP1V8_CAM_FRONT_FILT	FUNC_TEST=TRUE	20 21
PP2V9_AVDD_CAM_FRONT_FILT	FUNC_TEST=TRUE	20 21

POWER - CAMERA (REAR)

MUST HAVE

PP1V25_CAM_REAR_FILT	FUNC_TEST=TRUE	20 21
PP1V8_CAM_REAR_FILT	FUNC_TEST=TRUE	20 21
PP2V6_CAM_REAR_AF_FILT	FUNC_TEST=TRUE	20 21
PP2V9_AVDD_CAM_REAR_FILT	FUNC_TEST=TRUE	20 21

POWER - AUDIO

PP1V8_DMIC_MIC_FILT	FUNC_TEST=TRUE	23
PP1V8_DMIC_BTN_FILT	FUNC_TEST=TRUE	28
PP1V7_VCP	FUNC_TEST=TRUE	22
PPVBOOST_R	FUNC_TEST=TRUE	24
PPVBOOST_L	FUNC_TEST=TRUE	24

POWER - SENSORS

PP1V8_COMPASS	FUNC_TEST=TRUE	18
PP1V8_PHOS_FILT	FUNC_TEST=TRUE	18
PP1V8_OSCAR_FILT	FUNC_TEST=TRUE	17
PP1V2_OSCAR_FILT	FUNC_TEST=TRUE	17
PP3V0_GYRO_FILT	FUNC_TEST=TRUE	18
PP3V0_SENSOR_PROX_FILT	FUNC_TEST=TRUE	58

POWER - DISPLAY

MUST HAVE

PPVCC_MAIN_LCD_SW_CONN	FUNC_TEST=TRUE	31 32
PPVCC_MAIN_LCD_SW	FUNC_TEST=TRUE	32

POWER - MESA

MUST HAVE

PP1V825_S2R_MESA_FILT	FUNC_TEST=TRUE	31 33
PP3V1_S2R_MESA_FILT	FUNC_TEST=TRUE	31 33
PP11V3_MESA_FILT	FUNC_TEST=TRUE	31 33

POWER - GRAPE

PPVDD_STINGER_BOOST	FUNC_TEST=TRUE	29

POWER - BACKLIGHT

MUST HAVE

PPLED_BACK_REG_A	FUNC_TEST=TRUE	31 32
LED_IO_1_A	FUNC_TEST=TRUE	31 63
LED_IO_2_A	FUNC_TEST=TRUE	31 63
LED_IO_3_A	FUNC_TEST=TRUE	31 63
LED_IO_4_A	FUNC_TEST=TRUE	31 63
LED_IO_5_A	FUNC_TEST=TRUE	31 63
LED_IO_6_A	FUNC_TEST=TRUE	31 63
PPLED_BACK_REG_B	FUNC_TEST=TRUE	31 32
LED_IO_1_B	FUNC_TEST=TRUE	31 63
LED_IO_2_B	FUNC_TEST=TRUE	31 63
LED_IO_3_B	FUNC_TEST=TRUE	31 63
LED_IO_4_B	FUNC_TEST=TRUE	31 63
LED_IO_5_B	FUNC_TEST=TRUE	31 63
LED_IO_6_B	FUNC_TEST=TRUE	31 63

SOC - JTAG/RESET

MUST HAVE

JTAG_SOC_SEL	FUNC_TEST=TRUE	4 5
JTAG_SOC_TCK	FUNC_TEST=TRUE	5 25
JTAG_SOC_TDI	FUNC_TEST=TRUE	5
JTAG_SOC_TMS	FUNC_TEST=TRUE	5 25
TP_JTAG_SOC_TRST_L	FUNC_TEST=TRUE	4 5
TP_JTAG_SOC_TDO	FUNC_TEST=TRUE	5
SOC_TESTMODE	FUNC_TEST=TRUE	4 5
RESET_SOC_L	FUNC_TEST=TRUE	4 5 10 25 62 68 70
GPIO_FORCE_DFU	FUNC_TEST=TRUE	6 67

SOC - UART

UART_SOC2DEBUG_TX	FUNC_TEST=TRUE	6 25
UART_DEBUG2SOC_TX	FUNC_TEST=TRUE	6 25

SOC - USB

USB_SOC_N	FUNC_TEST=TRUE	5 25
USB_SOC_P	FUNC_TEST=TRUE	5 25

E75

E75_ACC_DET_CONN_L	FUNC_TEST=TRUE	25 27
PPVBUS_E75_USB_CONN	FUNC_TEST=TRUE	26 27 69
PPOUT_E75_ACC_ID1_CONN	FUNC_TEST=TRUE	26 27
PPOUT_E75_ACC_ID2_CONN	FUNC_TEST=TRUE	26 27
E75_DPAIR1_CONN_N	FUNC_TEST=TRUE	25 27
E75_DPAIR1_CONN_P	FUNC_TEST=TRUE	25 27
E75_DPAIR2_CONN_N	FUNC_TEST=TRUE	25 27
E75_DPAIR2_CONN_P	FUNC_TEST=TRUE	25 27

AUDIO - HEADPHONE

MUST HAVE

CONN_HP_HEADSET_DET_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS3_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS3_REF_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS4_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS4_REF_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_LEFT_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_RIGHT_FILT	FUNC_TEST=TRUE	22 23
GPIO_SOC2AJ_HS3_SHUNT_EN_FILT	FUNC_TEST=TRUE	23
GPIO_SOC2AJ_HS4_SHUNT_EN_FILT	FUNC_TEST=TRUE	23

AUDIO - SPEAKER AMPS

SPKRAMP_L_OUT_N	FUNC_TEST=TRUE	24 27 70
SPKRAMP_L_OUT_P	FUNC_TEST=TRUE	24 27 70
SPKRAMP_R_OUT_N	FUNC_TEST=TRUE	24 27 70
SPKRAMP_R_OUT_P	FUNC_TEST=TRUE	24 27 70

AUDIO - CODEC

AIN3P	FUNC_TEST=TRUE	22
AIN3N	FUNC_TEST=TRUE	22
GPIO_CODEC2PMU_HS_IRQ_L	FUNC_TEST=TRUE	22 62 70
GND_AUDIO_CODEC	FUNC_TEST=TRUE	22
MIKEY_TS_P	FUNC_TEST=TRUE	22 25
MIKEY_TS_N	FUNC_TEST=TRUE	22 25

AUDIO - DIGITAL MICS

DMIC_MIC_SCLK	FUNC_TEST=TRUE	22 23
DMIC_BTN_SCLK	FUNC_TEST=TRUE	22 28

BUTTONS

GPIO_BTN_HOME_CONN_L	FUNC_TEST=TRUE	31 33
GPIO_BTN_ONOFF_L	FUNC_TEST=TRUE	5 6 23 62
GPIO_BTN_VOL_UP_L_FILT	FUNC_TEST=TRUE	28
GPIO_BTN_VOL_DOWN_L_FILT	FUNC_TEST=TRUE	28

NAND

ANC0_CE0_L	FUNC_TEST=TRUE	7 16 70
ANC1_CE0_L	FUNC_TEST=TRUE	7 16 70

BATTERY

MUST HAVE

BATT_SWI_CONN	FUNC_TEST=TRUE	66
BATT_NTC	FUNC_TEST=TRUE	62 66
BATT_SNS	FUNC_TEST=TRUE	65 66

GRAPE

CLK_SOC2GRAPE_32K	FUNC_TEST=TRUE	9 30 70

BASEBAND

MUST HAVE

BOUNDARY_SCAN_EN	FUNC_TEST=TRUE	35 39
GPIO_PMU2BBPMU_RESET_L	FUNC_TEST=TRUE	62 68 70 71
GPIO_SOC2BB_RADIO_ON_L	FUNC_TEST=TRUE	6 68 71
HSIC_SOC2BB_HOST_RDY	FUNC_TEST=TRUE	6 68
GPIO_BB2SOC_RESET_DET_L	FUNC_TEST=TRUE	6 68
HSIC_BB2SOC_DEVICE_RDY	FUNC_TEST=TRUE	6 68
GPIO_SOC2BB_RESET_L	FUNC_TEST=TRUE	6 68
GPIO_PMU2BB_VBUS_DET	FUNC_TEST=TRUE	62 68 71
GPIO_BB2PMU_HOST_WAKE_L	FUNC_TEST=TRUE	62 68 70

BASEBAND - POWER

PP_LDO6	FUNC_TEST=TRUE	35 36 71 73
PP_LDO13	FUNC_TEST=TRUE	36 38 55 73
VREG_SMPS1_0V90	FUNC_TEST=TRUE	36 38
VREG_SMPS3_0V95	FUNC_TEST=TRUE	36 73

BASEBAND - SIM CARD

MUST HAVE

PP_LDO5_FILT	FUNC_TEST=TRUE	59
SIMCRD_RST_CONN_FILT	FUNC_TEST=TRUE	59 71
SIMCRD_CLK_CONN_FILT	FUNC_TEST=TRUE	59 71
SIMCRD_IO_CONN_FILT	FUNC_TEST=TRUE	59 71
SIMCRD_DETECT_FILT	FUNC_TEST=TRUE	59 71

WIFI/BT

MUST HAVE

GPIO_PMU2BT_REG_ON	FUNC_TEST=TRUE	57 62 68 70
GPIO_PMU2WLAN_REG_ON	FUNC_TEST=TRUE	57 62 68 70
CLK_PMU2WLAN_32K	FUNC_TEST=TRUE	57 62 68 70

CAMERA - REAR

ISP_CAM_REAR_CLK_F	FUNC_TEST=TRUE	20 21
ISP_CAM_REAR_SCL_F	FUNC_TEST=TRUE	20 21
ISP_CAM_REAR_SDA_F	FUNC_TEST=TRUE	20 21
ISP_CAM_REAR_SHUTDOWN_L_F	FUNC_TEST=TRUE	20 21

CAMERA - FRONT

ISP_CAM_FRONT_CLK_F	FUNC_TEST=TRUE	20 21
ISP_CAM_FRONT_SCL_F	FUNC_TEST=TRUE	20 21
ISP_CAM_FRONT_SDA_F	FUNC_TEST=TRUE	20 21
ISP_CAM_FRONT_SHUTDOWN_L_F	FUNC_TEST=TRUE	20 21

MESA

MUST HAVE

GPIO_MESA2SOC_IRQ_FILT	FUNC_TEST=TRUE	31 33
MESA_BOOST_ENABLE_FILT	FUNC_TEST=TRUE	31 33
SPI_MESA_MISO_FILT	FUNC_TEST=TRUE	31 33
SPI_MESA_MOSI_FILT	FUNC_TEST=TRUE	31 33
SPI_MESA_SCLK_FILT	FUNC_TEST=TRUE	31 33

HALL EFFECT

MUST HAVE

GPIO_HALL2PMU_IRQ0	FUNC_TEST=TRUE	19 62
GPIO_HALL2PMU_IRQ1_FILT	FUNC_TEST=TRUE	29 30
PP3V0_S2R_GRAPE_HALL_FILT	FUNC_TEST=TRUE	29 30

ALS

MUST HAVE

PP3V0_MIC_ALS_FILT	FUNC_TEST=TRUE	23
PP3V0_HP_ALS_FILT	FUNC_TEST=TRUE	23
GPIO_HP_ALS2SOC_IRQ_L_FILT	FUNC_TEST=TRUE	23
GPIO_MIC_ALS2SOC_IRQ_L_F	FUNC_TEST=TRUE	23
I2C_HP_ALS_SCL_1V8_FILT	FUNC_TEST=TRUE	23 70
I2C_HP_ALS_SDA_1V8_FILT	FUNC_TEST=TRUE	23 70
I2C_MIC_ALS_SCL_1V8_F	FUNC_TEST=TRUE	23 70
I2C_MIC_ALS_SDA_1V8_F	FUNC_TEST=TRUE	23 70

DISPLAY

MUST HAVE

EDP_HPD_EMI	FUNC_TEST=TRUE	32

OSCAR

MUST HAVE

CLK_PMU2OSCAR_32K_AND_RESET_L	FUNC_TEST=TRUE	17 62 70

SOCHOT0_L	FUNC_TEST=TRUE	6 62

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

SL9300 APN: 998-2691 TH-NSP
SL-1.1X0.4-1.4X0.7
SL9301 TH-NSP SL-1.1X0.4-1.4X0.7
SL9302 TH-NSP SL-1.1X0.4-1.4X0.7
SL9320 TH-NSP SL-1.1X0.4-1.4X0.7
SL9321 TH-NSP SL-1.1X0.4-1.4X0.7

FOREHEAD B2B STANDOFFS

STD9300 APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM

C9301 0.01UF 10% 6.3V X5R 01005
STD9301 APN: 860-8373 STDOFF-3.3X1.8R1.05H-SM
STD9301_AC_R
09/17/13 AC CAP RDAR://PROBLEM//14999426
STD9303 APN: 860-00013
STDOFF-3.3X1.8R0.84H-TH

BUTTON FLEX B2B STANDOFFS

STD9302 APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM

GRAPE AND DISPLAY B2B STANDOFFS

STD9305 APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM
STD9306
STDOFF-3.3X1.8R1.05H-SM
STD9307
STDOFF-3.3X1.8R1.05H-SM

FID9300 FID 0P5SM1P0SQ-NSP
FID9301 FID 0P5SM1P0SQ-NSP
FID9302 FID 0P5SM1P0SQ-NSP
FID9303 FID 0P5SM1P0SQ-NSP
FID9304 FID 0P5SM1P0SQ-NSP
FID9305 FID 0P5SM1P0SQ-NSP

TP9310A TP9311A TP9312A TP9315A TP9316A TP9317A
TP-1P0-TOP PLACE_NEAR=J3700.9:20MM / PLACE_NEAR=J3700.9:30MM
PPVBUS_E75_USB_CONN 26 27 69

TP9300A TP9301A TP9302A TP9305A TP9306A TP9307A
TP-1P0-TOP PLACE_NEAR=J8900.4:20MM / PLACE_NEAR=J8900.3:20MM
PPBATT_VCC 60 65 69 72

DEV BOARD NET TERMINATION

NC_SOC_GPIO09	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_ALS2SOC_DEVBRD_IRQ_L	6
NC_PMU_GPIO20	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_DEVBRD2PMU_WAKE_L	62
NC_ULPI_STP	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_SOC2DEVBRD_S3E_WAKE	9
NC_ULPI_DATA3	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_SOC2DEVBRD_S3E_RESET2_L	9
NC_PCIE_CLKREQ2	NO_TEST=TRUE MAKE_BASE=TRUE	PCIE_DEVBRD2SOC_CLKREQ_L	9
NC_PCIE_PERST2	NO_TEST=TRUE MAKE_BASE=TRUE	PCIE_SOC2DEVBRD_RESET_L	9
NC_NAND_SYS_CLK	NO_TEST=TRUE MAKE_BASE=TRUE	CLK_SOC2DEVBRD_PCIE_24MHZ	9
NC_I2S4_MCK	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_DISPLAY_ID0	6
NC_I2S1_MCK	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO_DISPLAY_ID1	6

EE CHARACTERIZATION TP

SOC

PP9501 P4MM SM (PT) 1 RESET_SOC_L — PLACE_SIDE=TOP — 4 5 10 25 62 68 69
PP9503 P4MM SM (PT) 1 SOCHOT0_L_R — 62
TP_GPIO_DFU_STATUS — FUNC_TEST=TRUE — 6
PP9502 P4MM SM (PT) 1 TP_ANALOGMUXOUT — 5
PP9507 P4MM SM (PT) 1 PPVDD_CPU_SOC_SENSE — PLACE_NEAR=U0600.AB13:1.5MM — 13 62
PP9508 P4MM SM (PT) 1 PPVDD_GPU_SOC_SENSE — PLACE_NEAR=U0600.N26:1.5MM — 13 62
PP9509 P4MM SM (PT) 1 PPVDD_SRAM_SOC_SENSE — PLACE_NEAR=U0600.N25:1.5MM — 13 62
PP9513 P4MM SM (PT) 1 PPVDD_SOC_SOC_SENSE — PLACE_NEAR=U0600.M25:1.5MM — 12 62
PP9509 P4MM SM (PT) 1 TP_SOC_VSS_SENSE — PLACE_NEAR=U0600.M26:1MM — 12
PP9510 P4MM SM (PT) 1 TP_SOC_VSS_CPU_SENSE — PLACE_NEAR=U0600.AC13:1MM — 12

NAND

ANC0_AD<1..7> — FUNC_TEST=TRUE — 7 16
ANC0_CE0_L — FUNC_TEST=TRUE — 7 16 69
ANC0_ALE — FUNC_TEST=TRUE — 7 16
ANC0_CLE — FUNC_TEST=TRUE — 7 16
ANC0_WE_L — FUNC_TEST=TRUE — 7 16
ANC0_RE_L — FUNC_TEST=TRUE — 7 16
ANC1_AD<0> — FUNC_TEST=TRUE — 7 16
ANC1_CE0_L — FUNC_TEST=TRUE — 7 16 69
ANC1_ALE — FUNC_TEST=TRUE — 7 16
ANC1_CLE — FUNC_TEST=TRUE — 7 16
ANC1_WE_L — FUNC_TEST=TRUE — 7 16
ANC1_RE_L — FUNC_TEST=TRUE — 7 16
ANC1_DQS — FUNC_TEST=TRUE — 7 16
PPVREF_ANC_SOC — FUNC_TEST=TRUE — 7
PPVREF_ANC_NAND — FUNC_TEST=TRUE — 16
NAND_SLOT0_RDYBSY_L — FUNC_TEST=TRUE — 16

PP9505 P4MM SM (PT) 1 ANC0_AD<0> — PLACE_SIDE=BOTTOM — NO_XNET_CONNECTION=TRUE — 7 16
PP9506 P4MM SM (PT) 1 ANC0_DQS — PLACE_SIDE=BOTTOM PLACE_NEAR=U0600.C36:2MM — NO_XNET_CONNECTION=TRUE — 7 16
PP9500 P4MM SM (PT) 1 GND — (PLACE_SIDE=TOP)
PP9504 P4MM SM (PT) 1 =PP1V8_NAND — (PLACE_SIDE=TOP) — 16 72
PP95G0 P4MM SM (PT) 1 TP_ANC_TCKC_NAND — (PLACE_SIDE=TOP) — 16
PP95G4 P4MM SM (PT) 1 TP_ANC_TMSC_NAND — (PLACE_SIDE=TOP) — 16

PMU

GPIO_PMU2BBPMU_RESET_L — FUNC_TEST=TRUE — 62 68 69 71
GPIO_BT2PMU_HOST_WAKE — FUNC_TEST=TRUE — 57 62 68 70
GPIO_BB2PMU_HOST_WAKE_L — FUNC_TEST=TRUE — 62 68 69
GPIO_CODEC2PMU_HS_IRQ_L — FUNC_TEST=TRUE — 22 62 69
PMU_TCAL — FUNC_TEST=TRUE — 62
CLK_PMU2WLAN_32K — FUNC_TEST=TRUE — 57 62 68 69 70
CLK_PMU2OSCAR_32K_AND_RESET — FUNC_TEST=TRUE — 17 62 69
PA_NTC_P — FUNC_TEST=TRUE — 62 68
BOARD_TEMP2_P — FUNC_TEST=TRUE — 62
BOARD_TEMP3_P — FUNC_TEST=TRUE — 62
BOARD_TEMP4_P — FUNC_TEST=TRUE — 62
BOARD_TEMP5_P — FUNC_TEST=TRUE — 62
BOARD_TEMP6_P — FUNC_TEST=TRUE — 62
BOARD_TEMP7_P — FUNC_TEST=TRUE — 62
BOARD_TEMP8_P — FUNC_TEST=TRUE — 62
TP_BUCK_LDO_VOV — FUNC_TEST=TRUE — 62
TP_BUCK_SLPD_MUX — FUNC_TEST=TRUE — 62
TP_AMUX_AY — FUNC_TEST=TRUE — 62
TP_AMUX_BY — FUNC_TEST=TRUE — 62

PP9511 P4MM SM (PT) 1 DWI_SOC2PMU_CLK — NO_TEST=TRUE — 6 62
PP9512 P4MM SM (PT) 1 DWI_SOC2PMU_DO — NO_TEST=TRUE — 6 62
PP95F1 P4MM SM (PT) 1 SYS_ALIVE — 62

6 68

GRAPE

I2C_GRAPE_SDA_1V8 (CUMULUS TDO) — FUNC_TEST=TRUE — 29 30
TP_JTAG_CUMULUS_M_TCK — FUNC_TEST=TRUE — 30
TP_JTAG_CUMULUS_M_TDI — FUNC_TEST=TRUE — 30
JTAG_CUMULUS_M_TMS — FUNC_TEST=TRUE — 30
SPI_GRAPE_SCLK — FUNC_TEST=TRUE — 6 30
SPI_GRAPE_MISO — FUNC_TEST=TRUE — 6 30
SPI_GRAPE_MOSI — FUNC_TEST=TRUE — 6 30
SPI_GRAPE_CS_L — FUNC_TEST=TRUE — 6 30
GPIO_SOC2GRAPE_RESET_L — FUNC_TEST=TRUE — 6 30
GPIO_GRAPE2SOC_IRQ_L — FUNC_TEST=TRUE — 6 30
DISPLAY_SYNC — FUNC_TEST=TRUE — 6 30
CLK_SOC2GRAPE_32K — FUNC_TEST=TRUE — 9 30 69
CUMULUS_M2S_CLK — FUNC_TEST=TRUE — 30
CUMULUS_M2S_SDA — FUNC_TEST=TRUE — 30
I2C_GRAPE_SDA_1V8 — FUNC_TEST=TRUE — 29 30 70
I2C_GRAPE_SCL_1V8 — FUNC_TEST=TRUE — 29 30

PP9514 P4MM SM (PT) 1 TP_CUMULUS_S_CS_L — 30
PP9515 P4MM SM (PT) 1 TP_CUMULUS_S_GPIO_3 — 30

AUDIO

DMIC_MIC_SD — FUNC_TEST=TRUE — 22 23
DMIC_BTN_SD — FUNC_TEST=TRUE — 22 28
GPIO_CODEC2SOC_IRQ_L — FUNC_TEST=TRUE — 6 22

TP9500 A TP-P5 1
TP9501 A TP-P5 1 — SPKRAMP_R_OUT_P — FUNC_TEST=TRUE — 24 27 69
TP9502 A TP-P5 1 — SPKRAMP_R_OUT_N — FUNC_TEST=TRUE — 24 27 69
TP9503 A TP-P5 1
TP9510 A TP-P5 1
TP9511 A TP-P5 1 — SPKRAMP_L_OUT_P — FUNC_TEST=TRUE — 24 27 69
TP9512 A TP-P5 1 — SPKRAMP_L_OUT_N — FUNC_TEST=TRUE — 24 27 69
TP9513 A TP-P5 1

PP95D0 P4MM SM (PT) 1 I2S_SOC2SPKRAMP_MCK — 6 24
PP95D1 P4MM SM (PT) 1 I2S_SOC2SPKRAMP_BCLK — 6 24
PP95D2 P4MM SM (PT) 1 I2S_SOC2SPKRAMP_LRCK — 6 24
PP95D3 P4MM SM (PT) 1 I2S_SOC2SPKRAMP_DOUT — 6 24
PP95D4 P4MM SM (PT) 1 I2S_SPKRAMP2SOC_DOUT — 6 24
PP95D7 P4MM SM (PT) 1 I2S_SOC2CODEC_ASP_MCK — 6 22
PP95D8 P4MM SM (PT) 1 I2S_SOC2CODEC_ASP_BCLK — 6 22
PP95D9 P4MM SM (PT) 1 I2S_SOC2CODEC_ASP_LRCK — 6 22
PP95DA P4MM SM (PT) 1 I2S_SOC2CODEC_ASP_DOUT — 6 22
PP95DB P4MM SM (PT) 1 I2S_CODEC2SOC_ASP_DOUT — 6 22
PP95DC P4MM SM (PT) 1 I2S_SOC2CODEC_XSP_BCLK — 6 22
PP95DD P4MM SM (PT) 1 I2S_SOC2CODEC_XSP_LRCK — 6 22
PP95DE P4MM SM (PT) 1 I2S_SOC2CODEC_XSP_DOUT — 6 22
PP95DF P4MM SM (PT) 1 I2S_CODEC2SOC_XSP_DOUT — 6 22

CAMERA - FRONT

PP9520 P4MM SM (PT) 1 MIPI_CAM_FRONT_CLK_P — PLACE_NEAR=U0600.AV36:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9521 P4MM SM (PT) 1 MIPI_CAM_FRONT_CLK_N — PLACE_NEAR=U0600.AW36:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9522 P4MM SM (PT) 1 MIPI_CAM_FRONT_DATA_P<0> — PLACE_NEAR=U0600.AV37:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9523 P4MM SM (PT) 1 MIPI_CAM_FRONT_DATA_N<0> — PLACE_NEAR=U0600.AW37:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70

CAMERA - REAR

PP9524 P4MM SM (PT) 1 MIPI_CAM_REAR_CLK_P — PLACE_NEAR=U0600.AV31:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9525 P4MM SM (PT) 1 MIPI_CAM_REAR_CLK_N — PLACE_NEAR=U0600.AW31:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9526 P4MM SM (PT) 1 MIPI_CAM_REAR_DATA_P<0> — PLACE_NEAR=U0600.AV33:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9527 P4MM SM (PT) 1 MIPI_CAM_REAR_DATA_N<0> — PLACE_NEAR=U0600.AW33:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70

OSCAR

PP95C0 P4MM SM (PT) 1 TP_OSCAR_P0_05 — 17
PP95C1 P4MM SM (PT) 1 TP_OSCAR_P0_06 — 17
PP95C2 P4MM SM (PT) 1 TP_OSCAR_P0_09 — 17
PP95C3 P4MM SM (PT) 1 TP_OSCAR_P0_17 — 17
PP95C4 P4MM SM (PT) 1 TP_OSCAR_P0_21 — 17
PP95C8 P4MM SM (PT) 1 TP_OSCAR_P1_02 — 17
PP95C9 P4MM SM (PT) 1 TP_OSCAR_P1_03 — 17
PP95CD P4MM SM (PT) 1 SWD_OSCAR_IO_1V8 — 9 17
PP95CF P4MM SM (PT) 1 SWD_OSCAR_CLK_1V8 — 9 17

CHAN 0 NEAR DRAM

PP9534 P4MM SM (PT) 1 DDR0_CK_P — PLACE_NEAR=U1600.W13:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9535 P4MM SM (PT) 1 DDR0_CK_N — PLACE_NEAR=U1600.W12:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9536 P4MM SM (PT) 1 DDR0_CKE<0> — PLACE_NEAR=U1600.W14:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9537 P4MM SM (PT) 1 DDR0_CA<0> — PLACE_NEAR=U1600.V17:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9538 P4MM SM (PT) 1 DDR0_CA<1> — PLACE_NEAR=U1600.W17:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9539 P4MM SM (PT) 1 DDR0_CA<2> — PLACE_NEAR=U1600.V16:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9540 P4MM SM (PT) 1 DDR0_CA<3> — PLACE_NEAR=U1600.W16:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9541 P4MM SM (PT) 1 DDR0_CSN<0> — PLACE_NEAR=U1600.Y14:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9530 P4MM SM (PT) 1 DDR0_DQS_P<0> — PLACE_NEAR=U1600.D15:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9531 P4MM SM (PT) 1 DDR0_DQS_N<0> — PLACE_NEAR=U1600.D14:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9532 P4MM SM (PT) 1 DDR0_DQ<0> — PLACE_NEAR=U1600.C17:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70

CHAN 0 NEAR SOC

PP9570 P4MM SM (PT) 1 DDR0_DQS_P<0> — PLACE_NEAR=U0600.D7:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9571 P4MM SM (PT) 1 DDR0_DQS_N<0> — PLACE_NEAR=U0600.D6:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9572 P4MM SM (PT) 1 DDR0_DQ<0> — PLACE_NEAR=U0600.F10:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70

CHAN 1 NEAR DRAM

PP9542 P4MM SM (PT) 1 DDR1_DQS_P<0> — PLACE_NEAR=U1600.K4:1MM — NO_XNET_CONNECTION=TRUE — 70 10 14
PP9543 P4MM SM (PT) 1 DDR1_DQS_N<0> — PLACE_NEAR=U1600.L4:1MM — NO_XNET_CONNECTION=TRUE — 70 10 14
PP9544 P4MM SM (PT) 1 DDR1_DQ<0> — PLACE_NEAR=U1600.H3:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70

CHAN 1 NEAR SOC

PP9582 P4MM SM (PT) 1 DDR1_DQS_P<0> — PLACE_NEAR=U0600.V1:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9583 P4MM SM (PT) 1 DDR1_DQS_N<0> — PLACE_NEAR=U0600.U1:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9584 P4MM SM (PT) 1 DDR1_DQ<0> — PLACE_NEAR=U0600.AA3:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70

WIFI

TP_JTAG_WLAN_TMS — FUNC_TEST=TRUE — 68
TP_JTAG_WLAN_TRST — FUNC_TEST=TRUE — 68
JTAG_WLAN_SEL (TDI) — FUNC_TEST=TRUE — 57
UART_SOC2WLAN_RTS_L (TDO) — FUNC_TEST=TRUE — 6 57 68
TP95B0 A TP-P5 1 — WLAN_SECI_IN — FUNC_TEST=TRUE — 57
OSCAR2RADIO_CONTEXT_A — FUNC_TEST=TRUE — 57 68
OSCAR2RADIO_CONTEXT_B — FUNC_TEST=TRUE — 57 68
UART_BT2SOC_TX — FUNC_TEST=TRUE — 6 68
UART_SOC2BT_TX — FUNC_TEST=TRUE — 6 57 68
UART_SOC2WLAN_TX — FUNC_TEST=TRUE — 6 57 68
UART_WLAN2SOC_TX — FUNC_TEST=TRUE
UART_BB2WLAN_COEX_RX — FUNC_TEST=TRUE — 40 57 71
UART_WLAN2BB_COEX_TX — FUNC_TEST=TRUE — 40 57 71
I2S_SOC2BT_BCLK — FUNC_TEST=TRUE — 6 57 68
I2S_SOC2BT_LRCK — FUNC_TEST=TRUE — 6 57 68
I2S_BT2SOC_DOUT — FUNC_TEST=TRUE — 6 68
I2S_SOC2BT_DOUT — FUNC_TEST=TRUE — 6 57 68
CLK_PMU2WLAN_32K — FUNC_TEST=TRUE — 57 62 68 69 70
GPIO_PMU2WLAN_REG_ON — FUNC_TEST=TRUE — 57 62 68 69
GPIO_PMU2BT_REG_ON — FUNC_TEST=TRUE — 57 62 68 69
GPIO_WLAN2PMU_HOST_WAKE — FUNC_TEST=TRUE — 57 62 68
GPIO_BT2PMU_HOST_WAKE — FUNC_TEST=TRUE — 57 62 68 70
GPIO_SOC2WLAN_WAKE — FUNC_TEST=TRUE — 9 68
GPIO_SOC2BT_WAKE — FUNC_TEST=TRUE — 9 57 68

OTHER PPS
PP95B8 P4MM SM (PT) 1 WLAN_GPIO_8 — NO_TEST=TRUE — 57
PP95B9 P4MM SM (PT) 1 WLAN_GPIO_10 — NO_TEST=TRUE — 57

I2C

I2C_OSCAR2PROX_SDA_1V8 — FUNC_TEST=TRUE — 17 58
I2C_OSCAR2PROX_SCL_1V8 — FUNC_TEST=TRUE — 17 58
I2C0_SCL_1V8 — FUNC_TEST=TRUE — 4 6
I2C0_SDA_1V8 — FUNC_TEST=TRUE — 4 6
I2C1_SCL_1V8 — FUNC_TEST=TRUE — 4 6
I2C1_SDA_1V8 — FUNC_TEST=TRUE — 4 6
I2C2_SCL_1V8 — FUNC_TEST=TRUE — 4 6
I2C2_SDA_1V8 — FUNC_TEST=TRUE — 4 6

PP95F4 P4MM SM (PT) 1 =I2C3_SDA_1V8 — 4
PP95F5 P4MM SM (PT) 1 =I2C3_SCL_1V8 — 4

I2C_HP_ALS_SCL_1V8_FILT — FUNC_TEST=TRUE — 23 69
I2C_HP_ALS_SDA_1V8_FILT — FUNC_TEST=TRUE — 23 69
I2C_MIC_ALS_SCL_1V8_F — FUNC_TEST=TRUE — 23 69
I2C_MIC_ALS_SDA_1V8_F — FUNC_TEST=TRUE — 23 69

UART

UART_SOC2ACC_TX — FUNC_TEST=TRUE — 6 25
UART_ACC2SOC_TX — FUNC_TEST=TRUE — 6 25
UART_SOC2OSCAR_TX — FUNC_TEST=TRUE — 6 17
UART_OSCAR2SOC_TX — FUNC_TEST=TRUE — 6 17

CHAN 2 NEAR DRAM

PP9548 P4MM SM (PT) 1 DDR2_CK_P — PLACE_NEAR=U1700.W13:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9549 P4MM SM (PT) 1 DDR2_CK_N — PLACE_NEAR=U1700.W12:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9550 P4MM SM (PT) 1 DDR2_CKE<0> — PLACE_NEAR=U1700.W14:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9551 P4MM SM (PT) 1 DDR2_CA<0> — PLACE_NEAR=U1700.V17:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9552 P4MM SM (PT) 1 DDR2_CA<1> — PLACE_NEAR=U1700.W17:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9553 P4MM SM (PT) 1 DDR2_CA<2> — PLACE_NEAR=U1700.V16:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9554 P4MM SM (PT) 1 DDR2_CA<3> — PLACE_NEAR=U1700.W16:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9555 P4MM SM (PT) 1 DDR2_CSN<0> — PLACE_NEAR=U1700.Y14:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9545 P4MM SM (PT) 1 DDR2_DQS_P<0> — PLACE_NEAR=U1700.D15:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9546 P4MM SM (PT) 1 DDR2_DQS_N<0> — PLACE_NEAR=U1700.D14:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9547 P4MM SM (PT) 1 DDR2_DQ<0> — PLACE_NEAR=U1700.C17:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70

CHAN 2 NEAR SOC

PP9585 P4MM SM (PT) 1 DDR2_DQS_P<0> — PLACE_NEAR=U0600.AM1:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9586 P4MM SM (PT) 1 DDR2_DQS_N<0> — PLACE_NEAR=U0600.AL1:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9587 P4MM SM (PT) 1 DDR2_DQ<0> — PLACE_NEAR=U0600.AR3:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70

CHAN 3 NEAR DRAM

PP9556 P4MM SM (PT) 1 DDR3_DQS_P<0> — PLACE_NEAR=U1700.K4:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9557 P4MM SM (PT) 1 DDR3_DQS_N<0> — PLACE_NEAR=U1700.L4:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9558 P4MM SM (PT) 1 DDR3_DQ<0> — PLACE_NEAR=U1700.H3:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70

CHAN 3 NEAR SOC

PP9596 P4MM SM (PT) 1 DDR3_DQS_P<0> — PLACE_NEAR=U0600.AT10:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9597 P4MM SM (PT) 1 DDR3_DQS_N<0> — PLACE_NEAR=U0600.AT11:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9598 P4MM SM (PT) 1 DDR3_DQ<0> — PLACE_NEAR=U0600.AP7:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70

PP95B5 P4MM SM (PT) 1 UART_WLAN2SOC_RTS_L — 6 68
PP95B6 P4MM SM (PT) 1 UART_BT2SOC_RTS_L — 6 68
PP95B7 P4MM SM (PT) 1 UART_SOC2BT_RTS_L — 6 57 68

SOC SIDE PCIE TPS
PP95A0 P4MM SM (PT) 1 PLACE_NEAR=U0600.D28:3MM — PCIE_WLAN2SOC_TX_P — 9 68 70
PP95A1 P4MM SM (PT) 1 PLACE_NEAR=U0600.E28:3MM — PCIE_WLAN2SOC_TX_N — 9 68 70

REMOVED PCIE_SOC2WLAN_TX_C_P PP BECAUSE THE IT BLOCKED THE SHIM RING.
REMOVED PCIE_SOC2WLAN_TX_C_N PP BECAUSE THE *_P VERSION WAS REMOVED

PP95A6 P4MM SM (PT) 1 PLACE_NEAR=U0600.J40:3MM — PCIE_WLAN2SOC_CLKREQ_L — 9 68 70

WLAN SIDE PCIE TPS
PP95A7 P4MM SM (PT) 1 PLACE_NEAR=U7500.73:3MM — PCIE_WLAN2SOC_TX_C_P — 68 70
PP95A8 P4MM SM (PT) 1 PLACE_NEAR=U7500.74:3MM — PCIE_WLAN2SOC_TX_C_N — 68 70
PP95A9 P4MM SM (PT) 1 PLACE_NEAR=U7500.77:3MM — PCIE_SOC2WLAN_TX_P — 9 57 68 70
PP95B0 P4MM SM (PT) 1 PLACE_NEAR=U7500.76:3MM — PCIE_SOC2WLAN_TX_N — 9 57 68 70
PP95B1 P4MM SM (PT) 1 PLACE_NEAR=U7500.71:3MM — PCIE_SOC2WLAN_CLK_P — 9 57 68 70
PP95B2 P4MM SM (PT) 1 PLACE_NEAR=U7500.70:3MM — PCIE_SOC2WLAN_CLK_N — 9 57 68 70
PP95B3 P4MM SM (PT) 1 PLACE_NEAR=U7500.1:3MM — PCIE_SOC2WLAN_RESET_L — 9 68 70

HIGH SPEED, NO TEST

DDR0_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR0_CK_P — NO_TEST=TRUE — 10 14 70
DDR0_CK_N — NO_TEST=TRUE — 10 14 70
DDR0_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR0_CKE<0..1> — NO_TEST=TRUE — 10 14
DDR0_CSN<0..1> — NO_TEST=TRUE — 10 14 70
DDR0_DM<0..3> — NO_TEST=TRUE — 10 14
DDR0_DQ<0..31> — NO_TEST=TRUE — 10 14 70
DDR0_DQS_P<0..3> — NO_TEST=TRUE — 10 14 70
DDR0_DQS_N<0..3> — NO_TEST=TRUE — 10 14 70
DDR1_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR1_CK_P — NO_TEST=TRUE — 10 14
DDR1_CK_N — NO_TEST=TRUE — 10 14
DDR1_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR1_CKE<0..1> — NO_TEST=TRUE — 10 14
DDR1_CSN<0..1> — NO_TEST=TRUE — 10 14
DDR1_DM<0..3> — NO_TEST=TRUE — 10 14
DDR1_DQ<0..31> — NO_TEST=TRUE — 10 14 70
DDR1_DQS_P<0..3> — NO_TEST=TRUE — 10 14 70
DDR1_DQS_N<0..3> — NO_TEST=TRUE — 10 14 70
DDR2_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR2_CK_P — NO_TEST=TRUE — 10 15 70
DDR2_CK_N — NO_TEST=TRUE — 10 15 70
DDR2_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR2_CKE<0..1> — NO_TEST=TRUE — 10 15 70
DDR2_CSN<0..1> — NO_TEST=TRUE — 10 15 70
DDR2_DM<0..3> — NO_TEST=TRUE — 10 15
DDR2_DQ<0..31> — NO_TEST=TRUE — 10 15 70
DDR2_DQS_P<0..3> — NO_TEST=TRUE — 10 15 70
DDR2_DQS_N<0..3> — NO_TEST=TRUE — 10 15 70
DDR3_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR3_CK_P — NO_TEST=TRUE — 10 15
DDR3_CK_N — NO_TEST=TRUE — 10 15
DDR3_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR3_CKE<0..1> — NO_TEST=TRUE — 10 15
DDR3_CSN<0..1> — NO_TEST=TRUE — 10 15
DDR3_DM<0..3> — NO_TEST=TRUE — 10 15
DDR3_DQ<0..31> — NO_TEST=TRUE — 10 15 70
DDR3_DQS_P<0..3> — NO_TEST=TRUE — 10 15 70
DDR3_DQS_N<0..3> — NO_TEST=TRUE — 10 15 70

MIPI_CAM_REAR_CLK_P — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_CLK_N — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_DATA_P<0..1> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_DATA_N<0..1> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_CLK_FILT_P — NO_TEST=TRUE — 20 21
MIPI_CAM_REAR_CLK_FILT_N — NO_TEST=TRUE — 20 21
MIPI_CAM_REAR_DATA_FILT_P<0..3> — NO_TEST=TRUE — 20 21
MIPI_CAM_REAR_DATA_FILT_N<0..3> — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_CLK_P — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_CLK_N — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_DATA_P<0> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_DATA_N<0> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_CLK_FILT_P — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_CLK_FILT_N — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_DATA_FILT_P<0> — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_DATA_FILT_N<0> — NO_TEST=TRUE — 20 21

EDP_DATA_P<0..3> — NO_TEST=TRUE — 9 32
EDP_DATA_N<0..3> — NO_TEST=TRUE — 9 32
EDP_DATA_EMI_P<0..3> — NO_TEST=TRUE — 32
EDP_DATA_EMI_N<0..3> — NO_TEST=TRUE — 32
EDP_DATA_EMI_CONN_P<0..3> — NO_TEST=TRUE — 31 32
EDP_DATA_EMI_CONN_N<0..3> — NO_TEST=TRUE — 31 32

PCIE_WLAN2SOC_TX_P — NO_TEST=TRUE — 9 68 70
PCIE_WLAN2SOC_TX_N — NO_TEST=TRUE — 9 68 70
PCIE_SOC2WLAN_TX_P — NO_TEST=TRUE — 9 57 68 70
PCIE_SOC2WLAN_TX_N — NO_TEST=TRUE — 9 57 68 70
PCIE_SOC2WLAN_CLK_P — NO_TEST=TRUE — 9 57 68 70
PCIE_SOC2WLAN_CLK_N — NO_TEST=TRUE — 9 57 68 70
PCIE_WLAN2SOC_TX_C_P — NO_TEST=TRUE — 68 70
PCIE_WLAN2SOC_TX_C_N — NO_TEST=TRUE — 68 70
PCIE_SOC2WLAN_TX_C_P — NO_TEST=TRUE — 9
PCIE_SOC2WLAN_TX_C_N — NO_TEST=TRUE — 9
PCIE_WLAN2SOC_CLKREQ_L — NO_TEST=TRUE — 9 68 70
PCIE_SOC2WLAN_RESET_L — NO_TEST=TRUE — 9 68 70

POWER, NO TEST

PP6V0_LCM_HI — NO_TEST=TRUE — 61 63
SW_CHGA — NO_TEST=TRUE — 65
WLED_LX_A — NO_TEST=TRUE — 61 63
WLED_LX_B — NO_TEST=TRUE — 61 63

L81_PVCP — NO_TEST=TRUE — 22
L81_NVCP — NO_TEST=TRUE — 22
L81_FLYC — NO_TEST=TRUE — 22
L81_FLYN — NO_TEST=TRUE — 22
L81_FLYP — NO_TEST=TRUE — 22

GRAPE NO_TEST
MT_PANEL_IN<0..29> — NO_TEST=TRUE — 29 30
MT_PANEL_OUT<0..39> — NO_TEST=TRUE — 29

RF TEAM REQUESTED TPS

SIMCRD_RST_CONN_FILT	FUNC_TEST=TRUE	59 69
SIMCRD_CLK_CONN_FILT	FUNC_TEST=TRUE	59 69
SIMCRD_IO_CONN_FILT	FUNC_TEST=TRUE	59 69
SIMCRD_DETECT_FILT	FUNC_TEST=TRUE	59 69
PP_LDO6	FUNC_TEST=TRUE	35 36 69 73
UART_BB2SOC_TX	FUNC_TEST=TRUE	6 25 68
UART_SOC2BB_TX	FUNC_TEST=TRUE	6 25 68
UART_BB2SOC_RTS_L	FUNC_TEST=TRUE	6 68
UART_SOC2BB_RTS_L	FUNC_TEST=TRUE	6 68
UART_OSCAR2BB_TX	FUNC_TEST=TRUE	17 68
UART_BB2OSCAR_TX	FUNC_TEST=TRUE	17 68
UART_BB2WLAN_COEX_RX	FUNC_TEST=TRUE	40 57 70
UART_WLAN2BB_COEX_TX	FUNC_TEST=TRUE	40 57 70
GPIO_SOC2BB_WAKE_MODEM	FUNC_TEST=TRUE	6 68
GPIO_BB2SOC_GPS_SYNC	FUNC_TEST=TRUE	6 68
USB_BB_P	FUNC_TEST=TRUE	25 68
USB_BB_N	FUNC_TEST=TRUE	25 68
GPIO_SOC2BB_COREDUMP	FUNC_TEST=TRUE	6 68
GPIO_SOC2BB_RADIO_ON_L	FUNC_TEST=TRUE	6 68 69
GPIO_PMU2BBPMU_RESET_L	FUNC_TEST=TRUE	62 68 69 70
GPIO_PMU2BB_VBUS_DET	FUNC_TEST=TRUE	62 68 69

PP9600_P4MM_SN	1 HSIC_BB_DATA	5 68
PP9601_P4MM_SR	1 HSIC_BB_STB	5 68

POWER CONNECTIONS

BUCK0 (DWI DVC)

69 60 PPVDD_CPU — =PPVDD_CPU 13
MAKE_BASE=TRUE
VOLTAGE=1.1V

BUCK1 (DWI DVC)

69 60 PPVDD_GPU — =PPVDD_GPU 13
MAKE_BASE=TRUE
VOLTAGE=1.1V

BUCK2

69 60 PP0V95_SOC — =PP0V95_SOC 12
MAKE_BASE=TRUE
VOLTAGE=0.95V
=PP0V95_PCIE_SOC 9
=PP0V95_USB_SOC 5

BUCK3

69 61 60 PP1V8_S2R — =PP1V8_S2R_DDR 14 15
MAKE_BASE=TRUE
VOLTAGE=1.8V
=PP1V8_S2R_GRAPE_EXTERNAL_SW 30
=PP1V8_S2R_TRISTAR 25
=PP1V8_S2R_VDDIO_WLAN_BT 68
=PP1V8_S2R_MISC 6 9 66 67
=PP1V8_S2R_EXTERNAL_SW 64
=PP1V8_S2R_ROTTERDAM 34

BUCK3_SW

BUCK3_SW1

69 67 60 PP1V8_SW1 — =PP1V8_AUDIO 22 24
MAKE_BASE=TRUE
VOLTAGE=1.8V
=PP1V8_SW1_EXT_SW_ON 64
XWC130
SM
1 2 PP1V8_SW1_FOREHEAD 69 72
72 69 PP1V8_SW1_FOREHEAD — =PP1V8_CAM_FRONT 21
MAKE_BASE=TRUE
VOLTAGE=1.8V
=PP1V8_CAM_REAR 21
=PP1V8_DMIC 23 28

BUCK3_SW1_EXT

69 64 PP1V8_EXT_SW — =PP1V8_VDDIO18_SOC 11
MAKE_BASE=TRUE
VOLTAGE=1.8V
=PP1V8_XTAL_SOC 11
=PP1V8_PCIE_SOC 9
=PP1V8_MIPI_SOC 8
=PP1V8_NAND_SOC 7
=PP1V8_NAND 16 70
=PP1V8_NAND_EXT_SW_ON 64
=PP1V8_SOC 4 5 6 62
=PP1V8_EEPROM 6

BUCK3_SW2

69 60 PP1V8_SW2 — =PP1V8_SPKRAMP_DVDD 24
MAKE_BASE=TRUE
VOLTAGE=1.8V
69 30 PP1V8_GRAPE_EXT_SW — =PP1V8_GRAPE_EXT_SW 29 30
MAKE_BASE=TRUE
VOLTAGE=1.8V

BUCK3_SW3

69 60 PP1V8_S2R_SW3 — =PP1V8_S2R_OSCAR 17
MAKE_BASE=TRUE
VOLTAGE=1.8V
=PP1V8_S2R_PHOS 18
=PP1V8_S2R_GYRO 18
=PP1V8_S2R_COMPASS 18
=PP1V8_S2R_ACCEL 18
=PP1V8_S2R_PROX 58

BUCK4

69 61 60 PP1V2_S2R — =PP1V2_EXTERNAL_SW 64
MAKE_BASE=TRUE
3V1_S2R_MESA VOLTAGE=1.2V
=PP1V2_S2R_DDR 14 15
=PP1V2_S2R_DDR_SOC 10

BUCK4_SW1

69 60 PP1V2_SW1 — =PP1V2_EXT_SW_ON 64
MAKE_BASE=TRUE
VOLTAGE=1.2V
69 64 PP1V2_EXT_SW — =PP1V2_DDR_VDDQ 14 15
MAKE_BASE=TRUE
VOLTAGE=1.2V
=PP1V2_VDDIOD_SOC 10 11
=PP1V2_HSIC_SOC 5
=PP1V2_PLL_SOC 9 11
=PP1V2_CAM_FRONT 21

BUCK4_SW2

69 60 PP1V2_S2R_SW2 — =PP1V2_S2R_OSCAR 17
MAKE_BASE=TRUE
VOLTAGE=1.2V

BUCK5 (DWI DVC)

69 60 PPVDD_SRAM — =PPVDD_SRAM 13
MAKE_BASE=TRUE
VOLTAGE=1.1V

BUCK6

69 60 PP3V3_S2R — =PP3V3_S2R_EXTERNAL_SW 64
MAKE_BASE=TRUE
VOLTAGE=3.3V
=PP3V3_S2R_WIFI_PA 68
69 64 PP3V3_EXT_SW — =PP3V3_NAND 16
MAKE_BASE=TRUE
VOLTAGE=3.3V
=PP3V3_USB_SOC 5

LDO1

69 61 PP3V0_S2R_HALL — =PP3V0_S2R_HALL 19 30
MAKE_BASE=TRUE
VOLTAGE=3.0V

LDO2

69 61 PP1V7_VA_VCP — =PP1V7_VA_VCP 22
MAKE_BASE=TRUE
VOLTAGE=1.7V

LDO3

69 61 PP3V0_S2R_SENSOR — =PP3V0_S2R_PROX 58
MAKE_BASE=TRUE
VOLTAGE=3.0V
=PP3V0_S2R_COMPASS 18
=PP3V0_S2R_GYRO 18

LDO4

69 61 PP3V0_ALS — =PP3V0_HP_ALS 23
MAKE_BASE=TRUE
VOLTAGE=3.0V
=PP3V0_MIC_ALS 23

LDO5

69 61 PP3V1_S2R_MESA —
MAKE_BASE=TRUE
VOLTAGE=3.1V

LDO6

69 61 PP3V3_ACC — =PP3V3_ACC 25
MAKE_BASE=TRUE
VOLTAGE=3.3V

LDO7

69 61 PP3V0_S2R_TRISTAR — =PP3V0_S2R_TRISTAR 25
MAKE_BASE=TRUE
VOLTAGE=3.0V
=PP3V0_S2R_ANT_SW 59

LDO8

72 69 61 PP3V0_MISC — PP3V0_MISC 61 69 72
MAKE_BASE=TRUE
VOLTAGE=3.0V

LDO9

69 61 PP1V25_CAM — =PP1V25_CAM_REAR 21
MAKE_BASE=TRUE
VOLTAGE=1.25V

LDO10

69 61 PP1V0_SOC — =PP1V0_MIPI_SOC 8
MAKE_BASE=TRUE
VOLTAGE=1.0V
=PP1V0_LPDP_SOC 9

LDO11

69 61 PP2V6_CAM_AF — =PP2V6_CAM_REAR_AF 21
MAKE_BASE=TRUE
VOLTAGE=2.6V

LDO13

69 61 PP2V9_CAM — =PP2V9_CAM_FRONT 21
MAKE_BASE=TRUE
VOLTAGE=2.9V
=PP2V9_CAM_REAR 21

LDO14

72 69 61 PP1V8_SPARE — PP1V8_SPARE 61 69 72
MAKE_BASE=TRUE
VOLTAGE=1.8V

VLCM1

69 61 PP5V25_GRAPE — =PP5V25_GRAPE 29 30
MAKE_BASE=TRUE
VOLTAGE=5.25V

CHARGER MAIN

69 65 64 61 60 PPVCC_MAIN — =PPVCC_MAIN_AUDIO 22
MAKE_BASE=TRUE
VOLTAGE=4.7V
=PPVCC_MAIN_LED 63
=PPVCC_MAIN_CPU 60
=PPVCC_MAIN_GPU 60
=PPVCC_MAIN_SOC 60
=PPVCC_MAIN_GRAPE 29 30
=PPVCC_MAIN_LCD 32
=PPVCC_MAIN_VDD_LCM 61
=PPVCC_MAIN_WLAN 68
=PPVCC_MAIN_MESA 33
=PPVCC_MAIN_ROTTERDAM 34

BATTERY

69 65 60 PPBATT_VCC — =PPBATT_POS_CONN 66
MAKE_BASE=TRUE
VOLTAGE=4.7V
=PPBATT_VCC_BB 68
=PPBATT_AUDIO 24

USB POWER INPUT

69 65 PPVBUS_USB_DCIN — =PPVBUS_USB_EMI 26
MAKE_BASE=TRUE
VOLTAGE=16V

ON_BUF

69 61 PP1V8_ALWAYS — =PP1V8_ALWAYS 6 11 62
MAKE_BASE=TRUE
VOLTAGE=1.8V

BACKLIGHT BOOST

69 63 PPLED_OUT_A — =PPLED_REG_A 32
MAKE_BASE=TRUE
VOLTAGE=20.4V

69 63 PPLED_OUT_B — =PPLED_REG_B 32
MAKE_BASE=TRUE
VOLTAGE=20.4V

1.225V	PP_LDO1	36 38 42 43
1.8V	PP_LDO2	36 38
1.8V	PP_LDO3	36 37 38 55
3.075V	PP_LDO4	36 38
2.85V	PP_LDO5	36 38 59
2.85V	PP_LDO6	35 36 69 71
1.9V	PP_LDO7	36 38 40
2.05V	PP_LDO8	36 42 43
1.2V	PP_LDO9	36 38
0.9V	PP_LDO10	36 38
1.8V	PP_LDO11	35 36 38 39 40 42 43 44
0.95V	PP_LDO12	36 38
2.95V	PP_LDO13	36 38 55 69
2.95V	PP_LDO13_GPS	55
2.7V	PP_LDO14_RFSW	36 46 47
0.95V	VREG_SMPS3_0V95	36 69
2.075V	VREG_SMPS4_2V075	36

0.9V	PP_VSW_S1	36
1.25V	PP_VSW_S2	36
0.95V	PP_VSW_S3	36
2.075V	PP_VSW_S4	36

4.7V	PP_BATT_VCC	35 44 53 68
4.7V	PP_VCC_MAIN	73
4.2V	PP_BATT_VCC_2GPA	45
4.2V	PP_BATT_VCC_QPOET	44 45 50 51
4.2V	PP_BATT_VCC_RADIO	35 36
4.7V	PP_BATT_VCC_DSM	53
4.2V	PP_BATT_VCC_QPOET_HBS	51
4.2V	PP_BATT_VCC_QPOET_ASM	50
1.8V	PP_1V8_S2R_VDDIO_WLAN_BT	57 68
1.8V	PP_WL_VDDIO	57
4.7V	PP_VCC_MAIN	73

0V	S1_GND	36
0V	S2_GND	36
0V	S3_GND	36
0V	S4_GND	36
0V	GND_SW	44
0V	VOUT_BOOST_GND	44