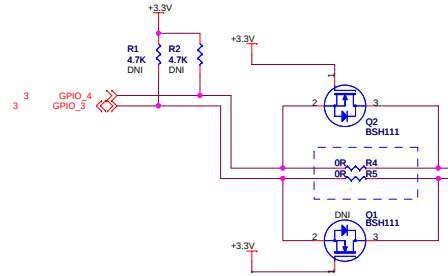
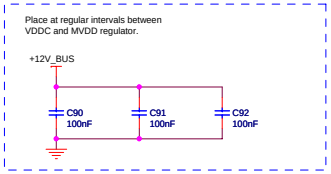
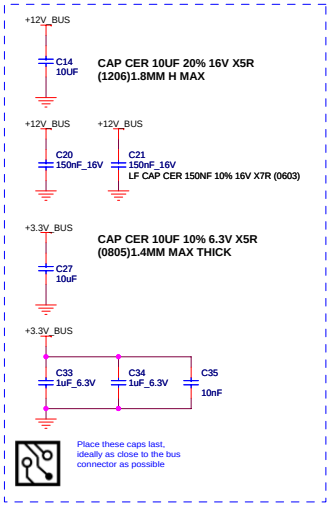
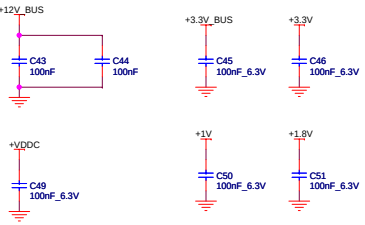
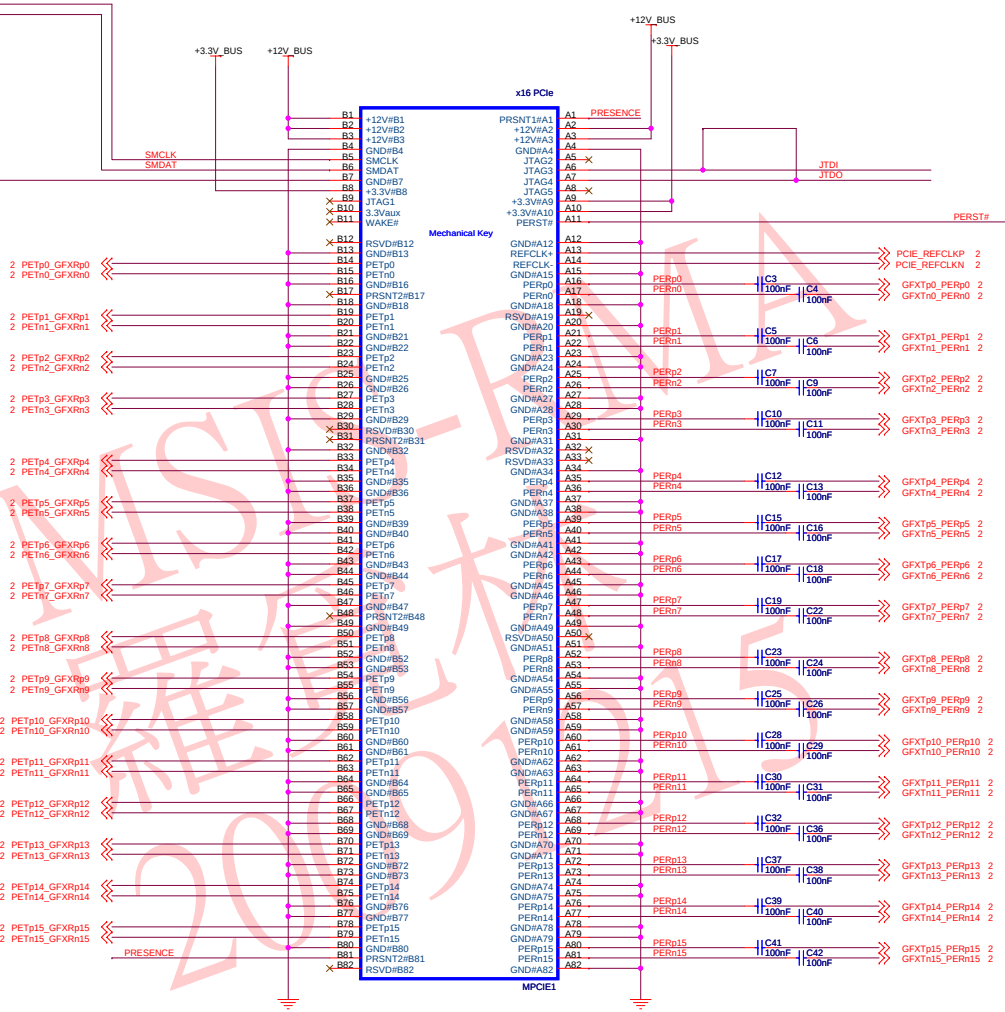
# PCI-EXPRESS EDGE CONNECTOR

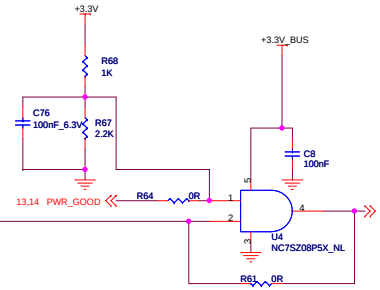



SYMBOL LEGEND

| | |
|---|---|
| DNI | DO NOT INSTALL |
| # | ACTIVE LOW |
| | DIGITAL GROUND |
| | ANALOG GROUND |



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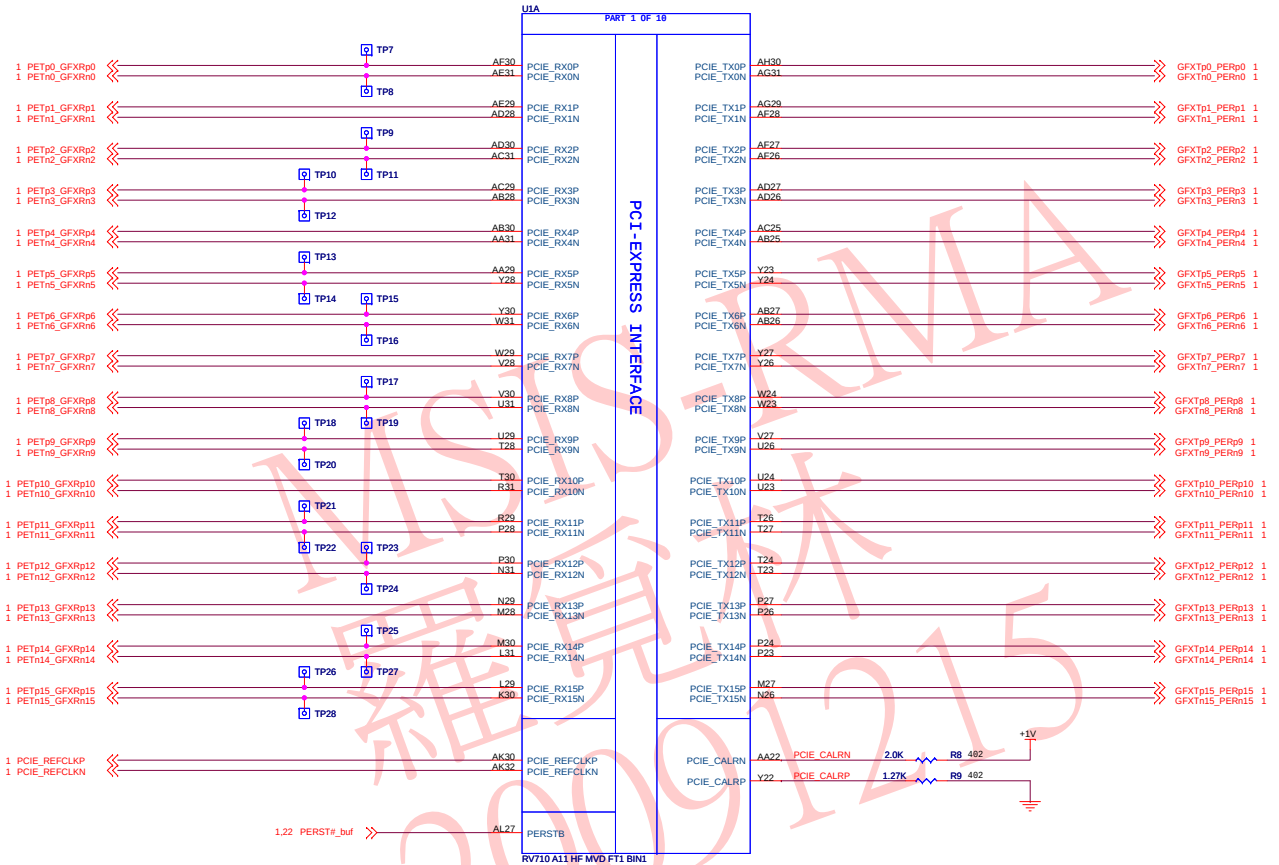
# (2) Cedar PCIE Interface

NOTE: some of the PCIE testpoints will
be available through via on traces.





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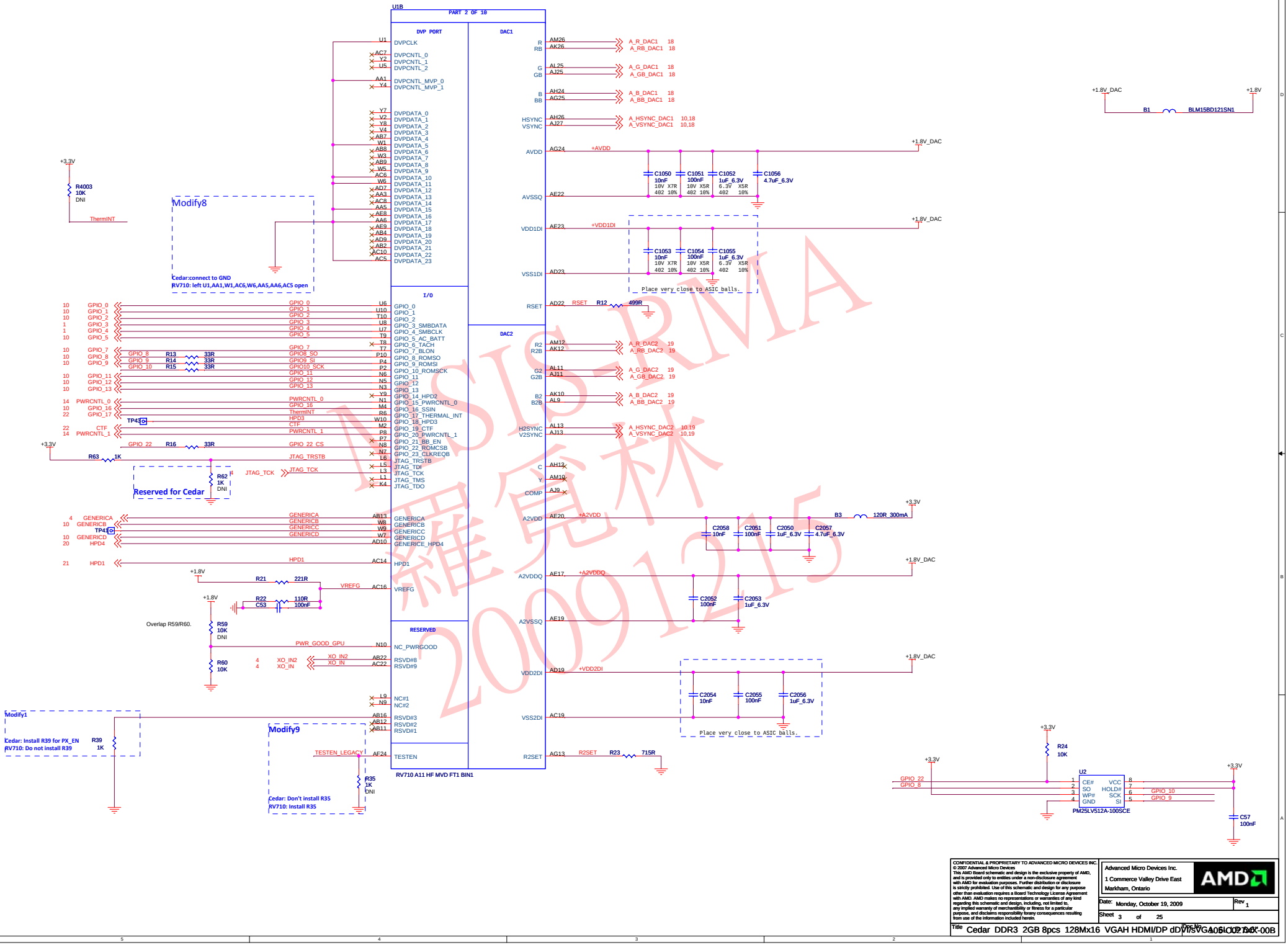
# (3) Cedar Main







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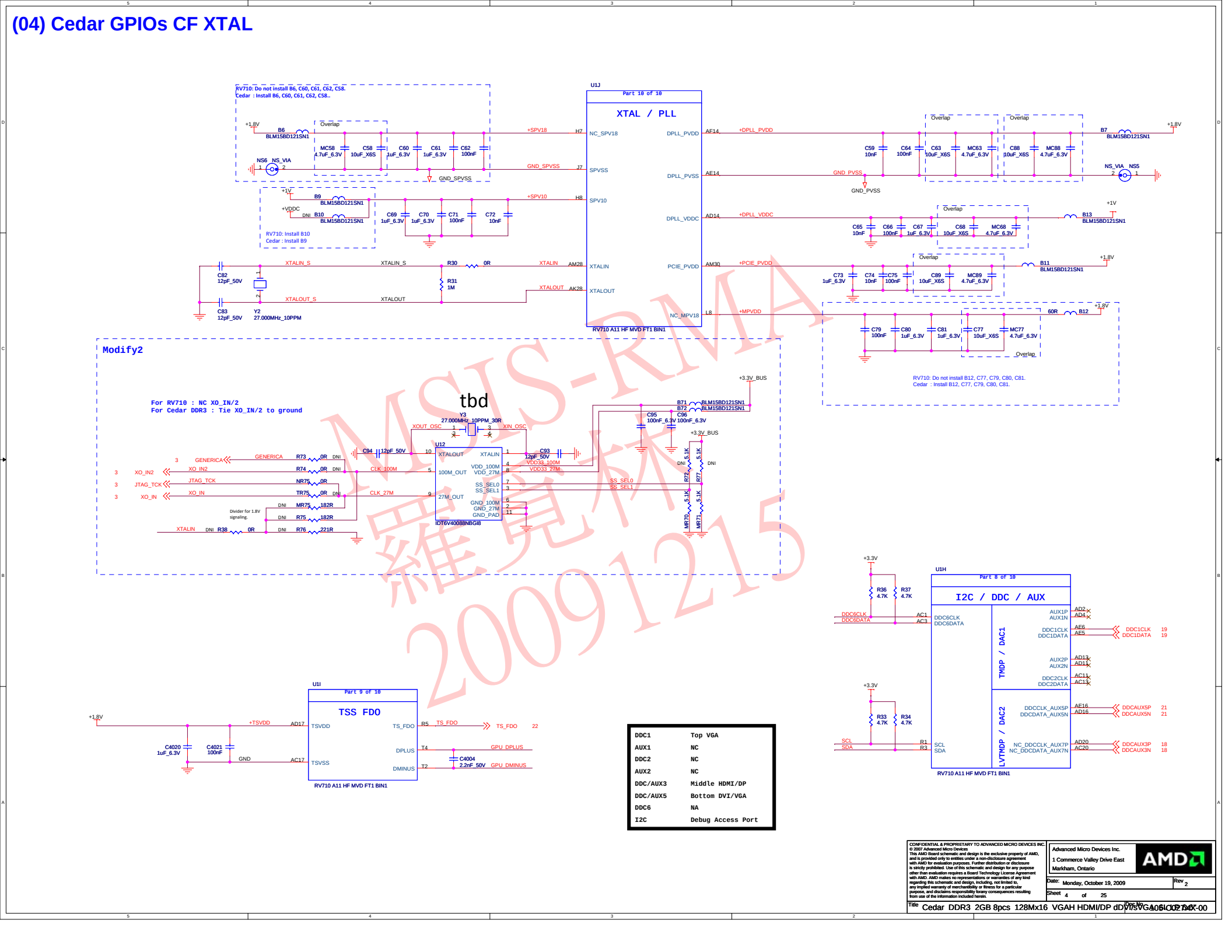
# (04) Cedar GPIOs CF XTAL




| | |
|---|---|
| DDC1 | Top VGA |
| AUX1 | NC |
| DDC2 | NC |
| AUX2 | NC |
| DDC/AUX3 | Middle HDMI/DP |
| DDC/AUX5 | Bottom DVI/VGA |
| DDC6 | NA |
| I2C | Debug Access Port |

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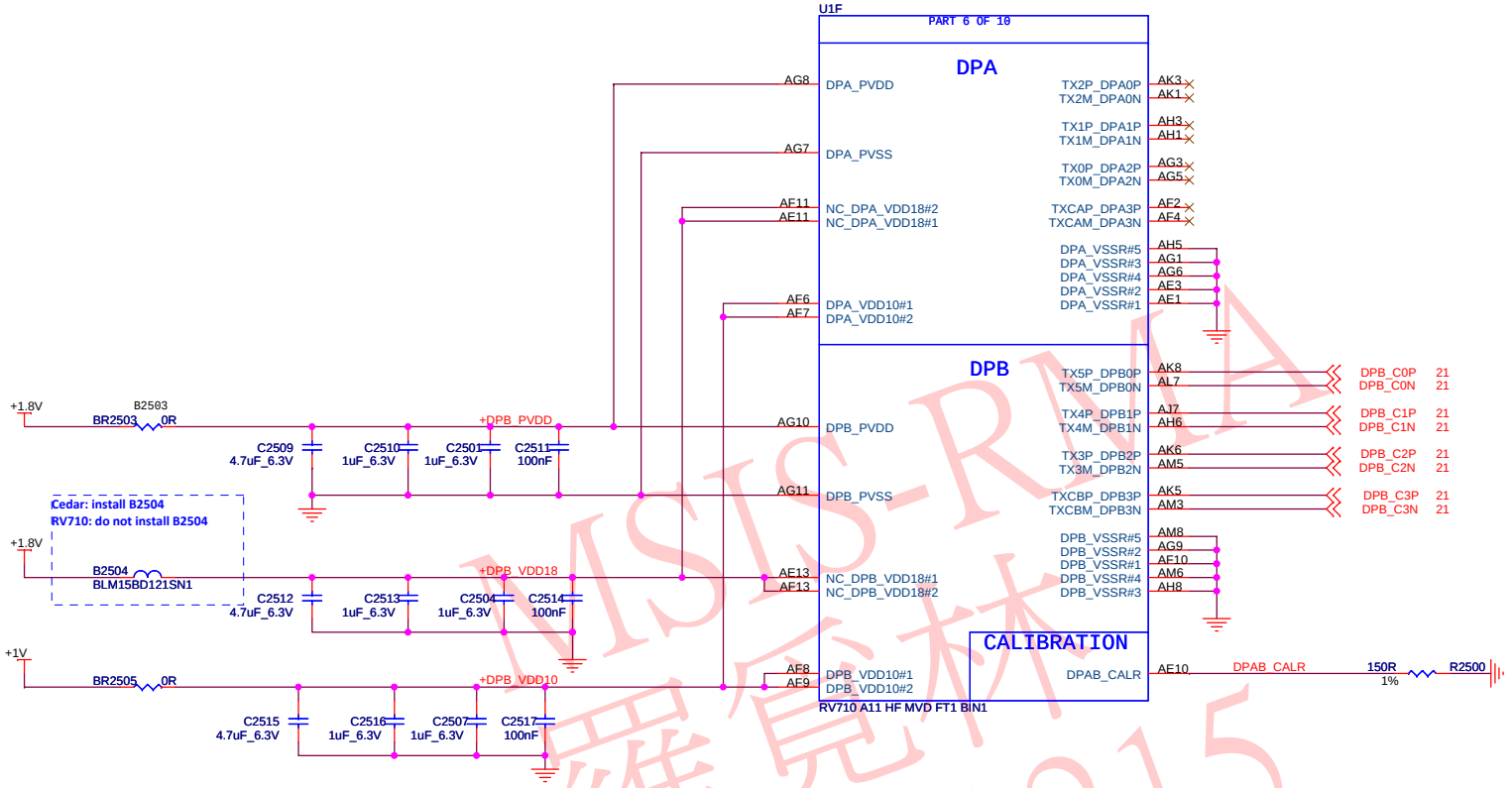
# (05) Cedar TMDP A&B

## TMDP INTERFACE





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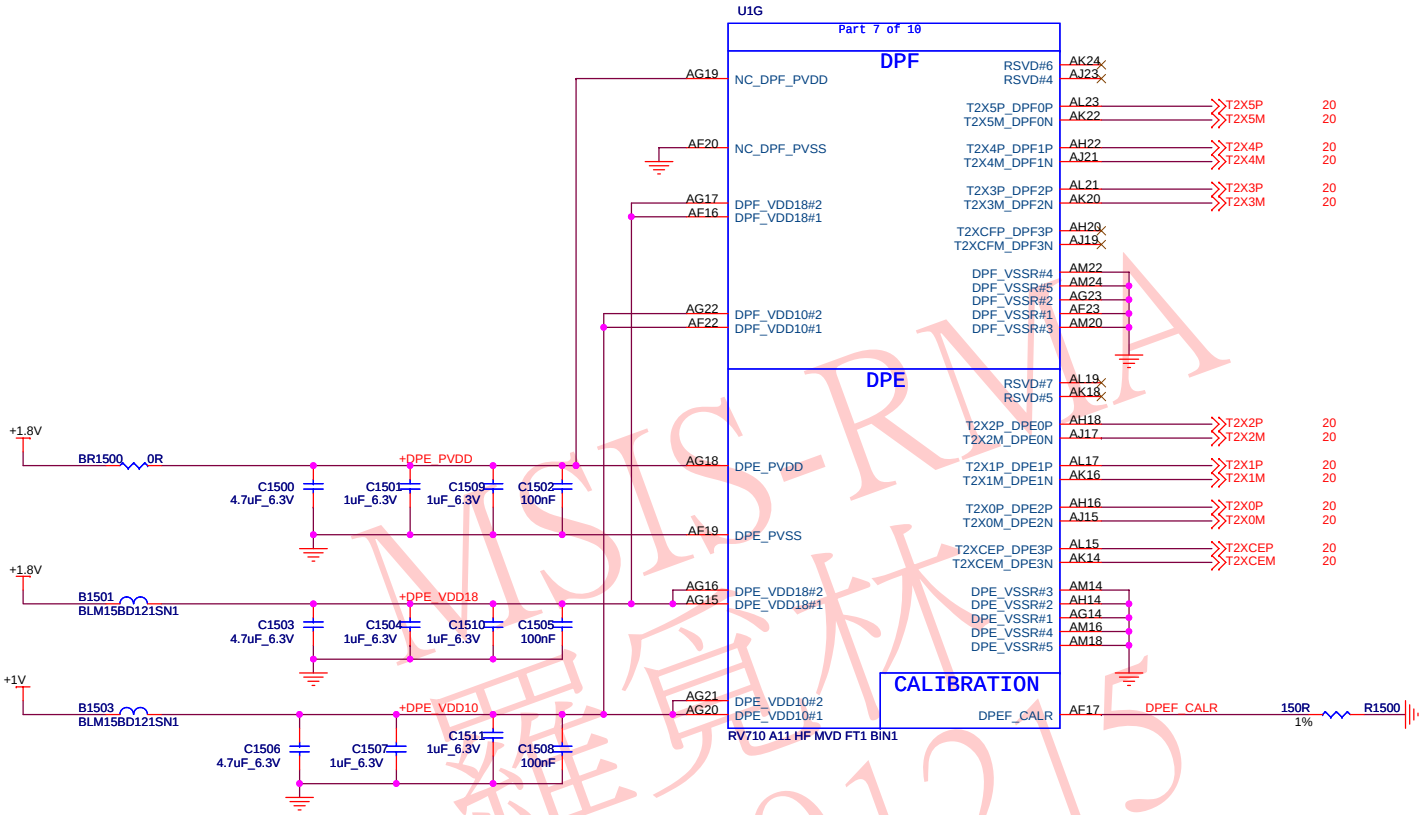
# (06) Cedar TMDP E&F

## LVTMDP INTERFACE







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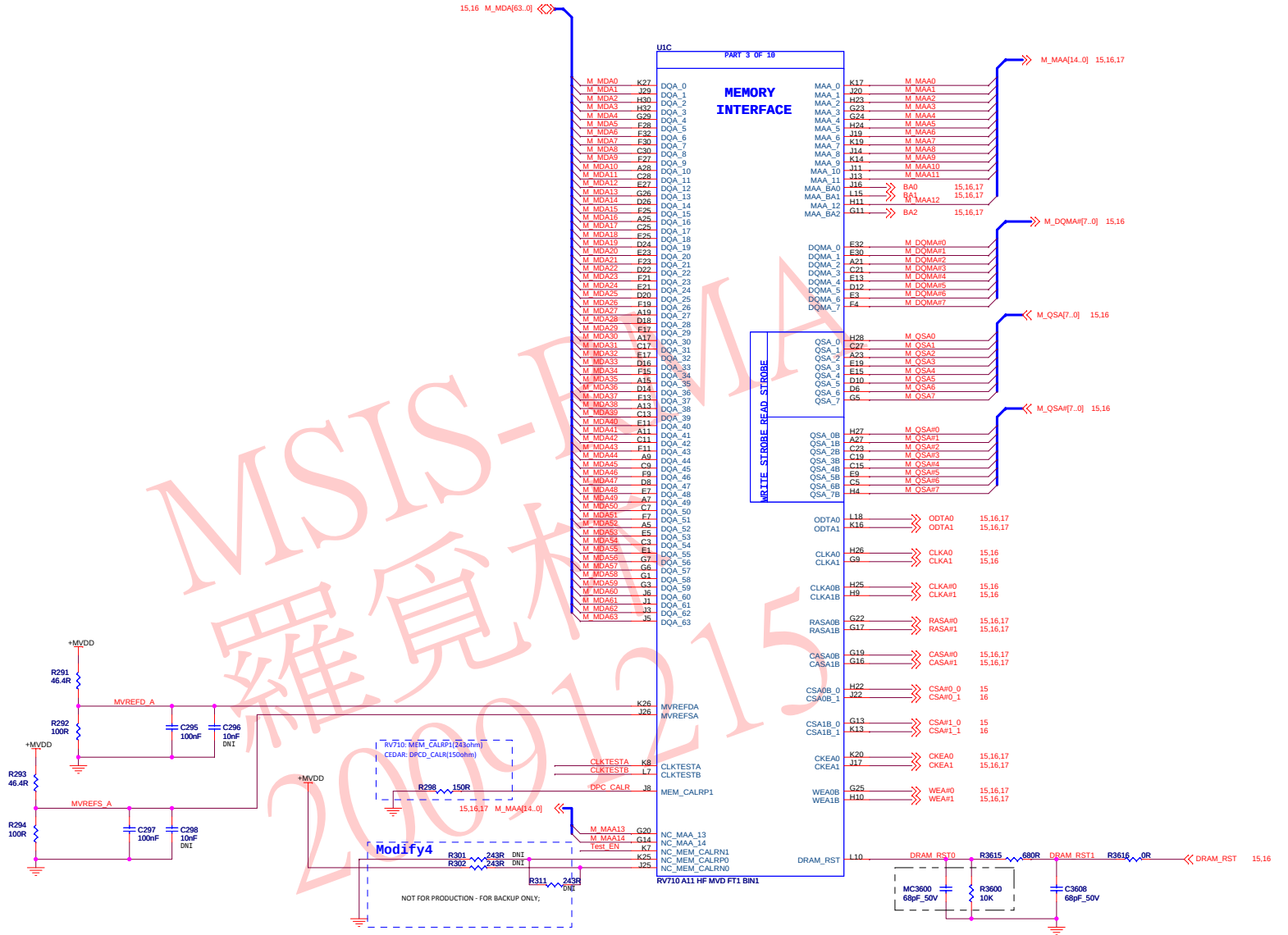
Doc No 105-C12768-00

# (07) Cedar MEM Interface Ch A

## MEMORY INTERFACE









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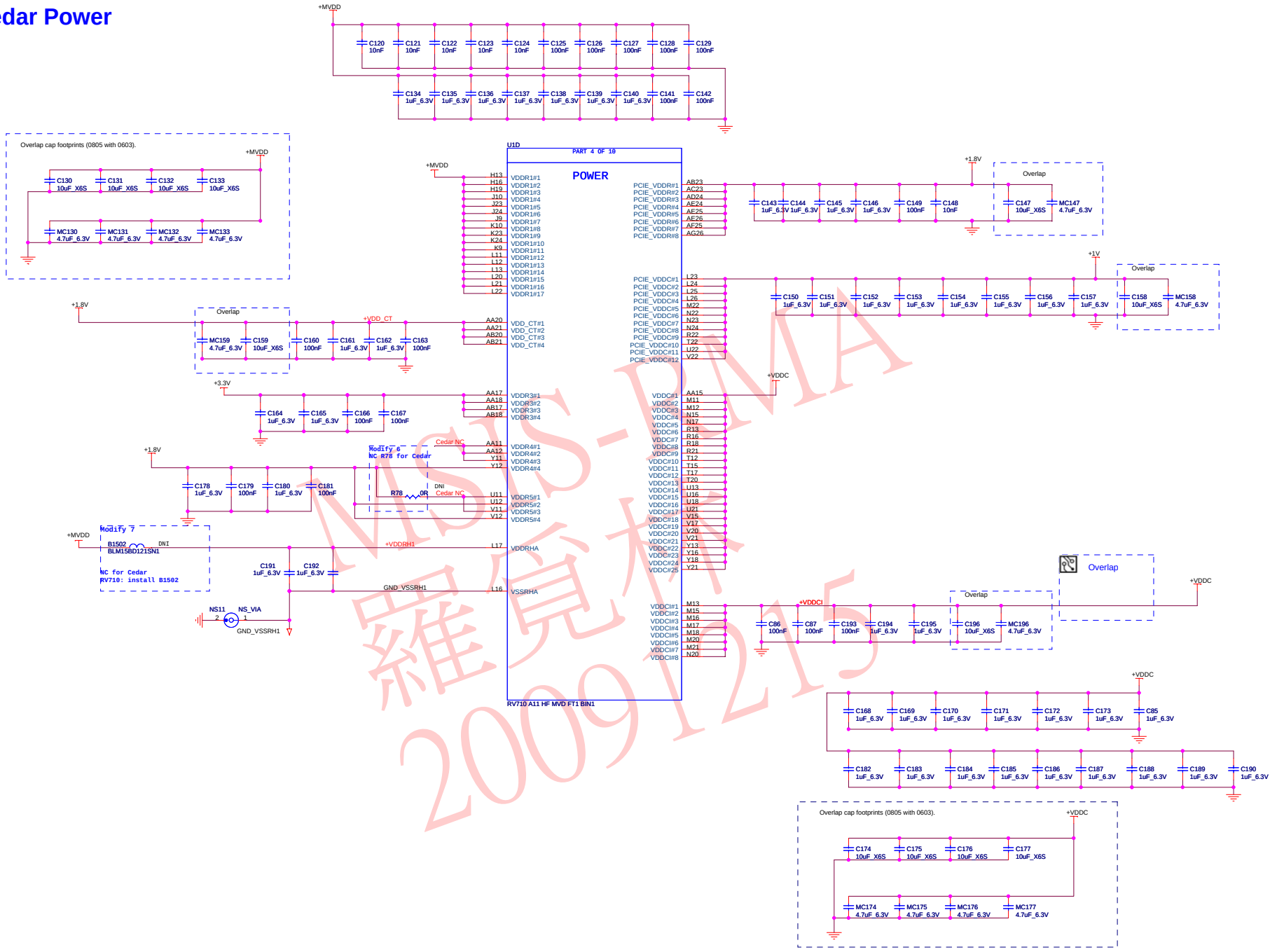
# (08) Cedar Power





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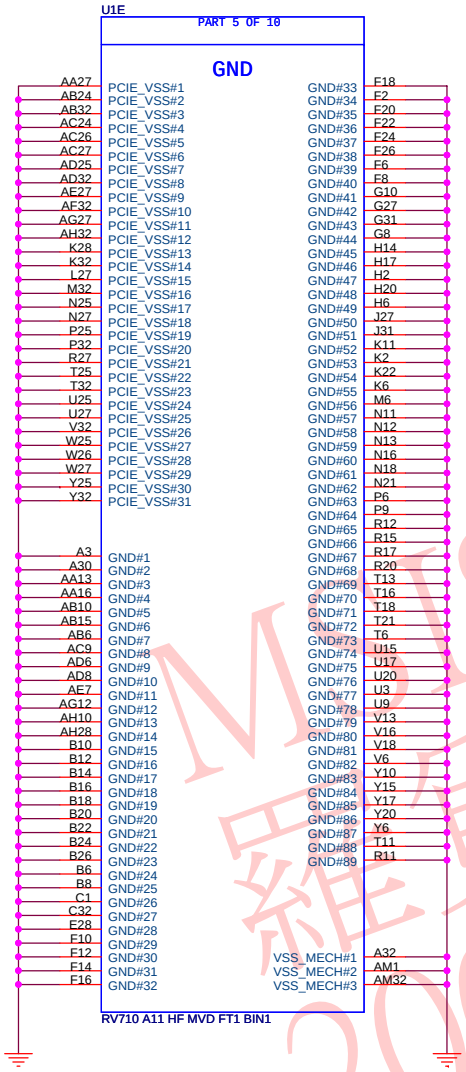
# (09) Cedar GND





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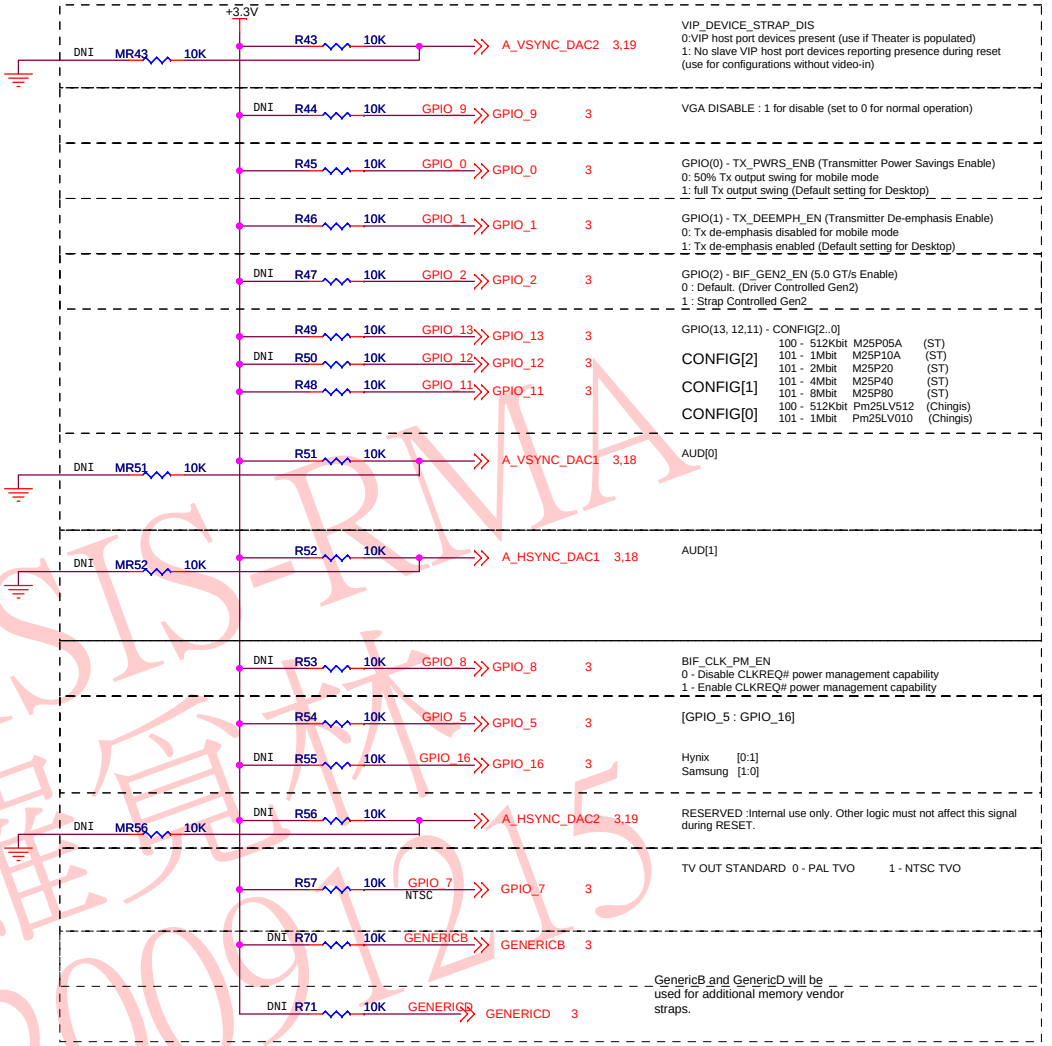
# (10) Cedar STRAPS

## PIN BASED STRAPS





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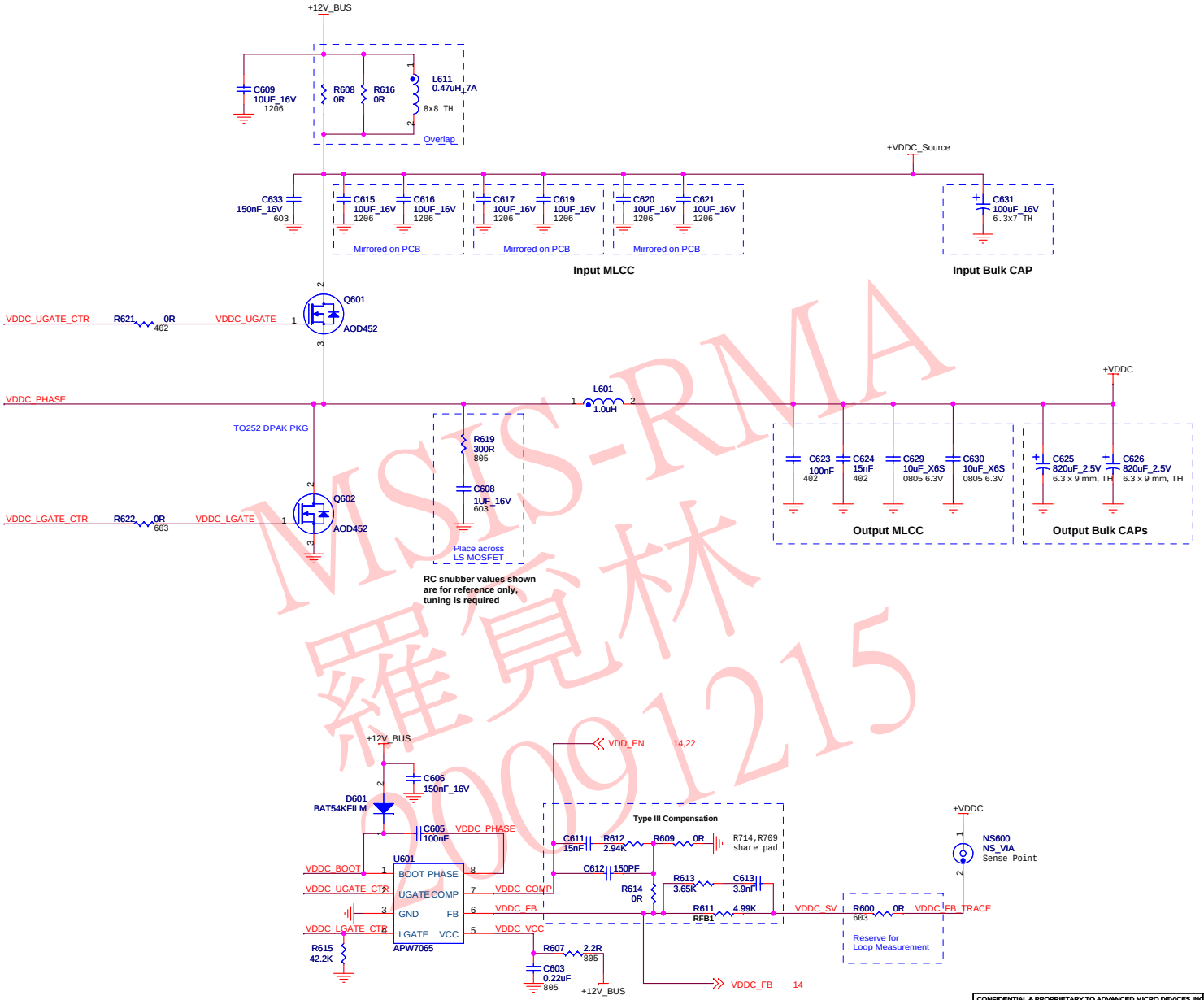






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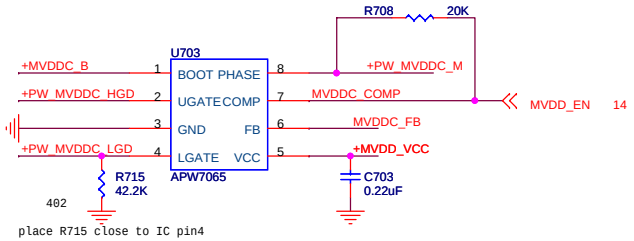
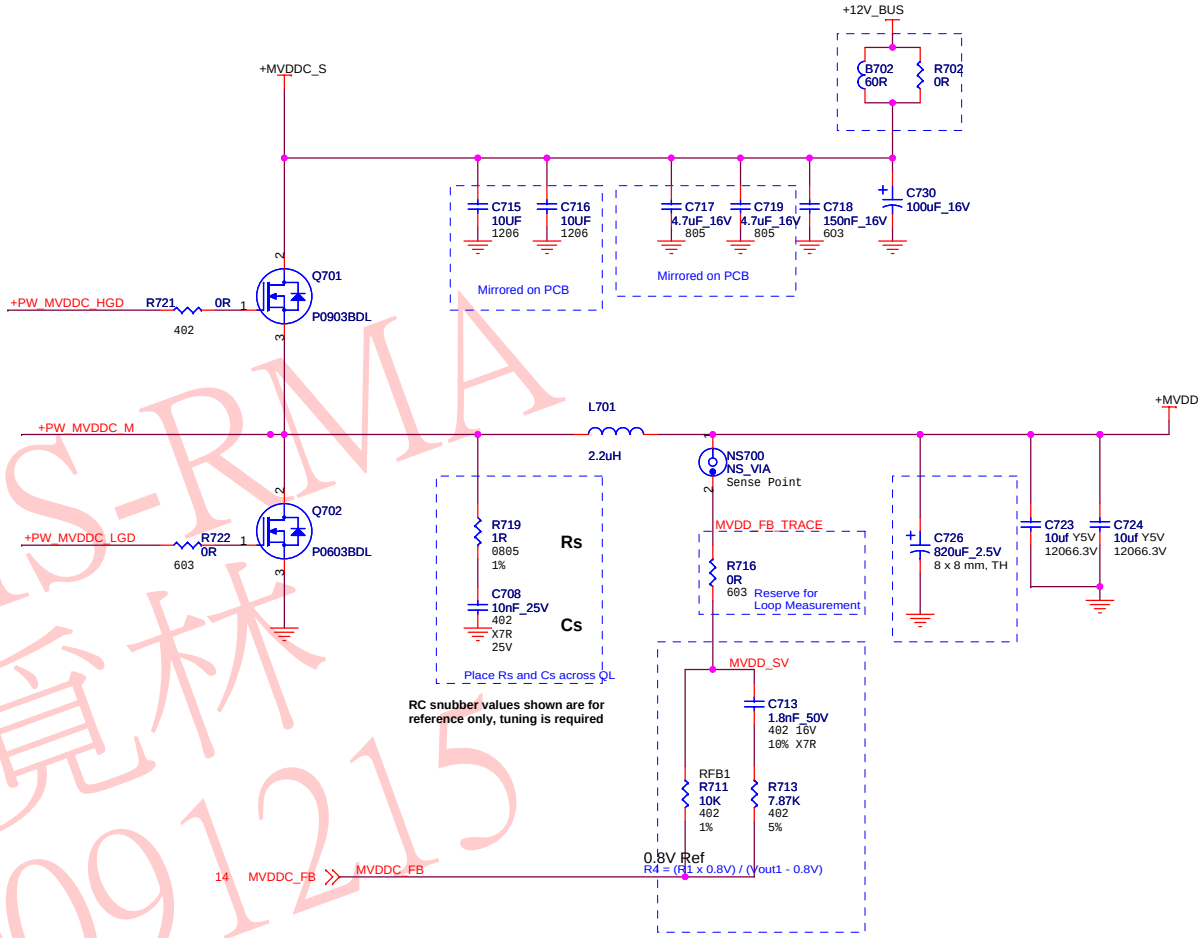
# (12) MVDD

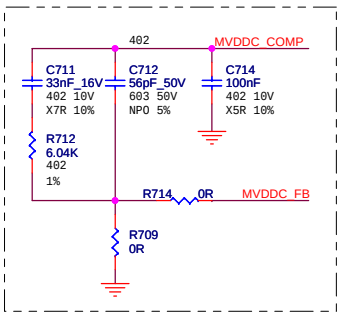



**Layout guideline**

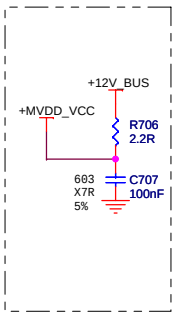
1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



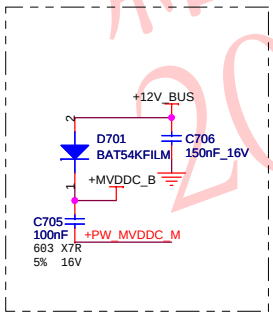

**COMPENSATION CIRCUIT**




**FILTERED SMPS VCC**




**BOOT CIRCUIT**





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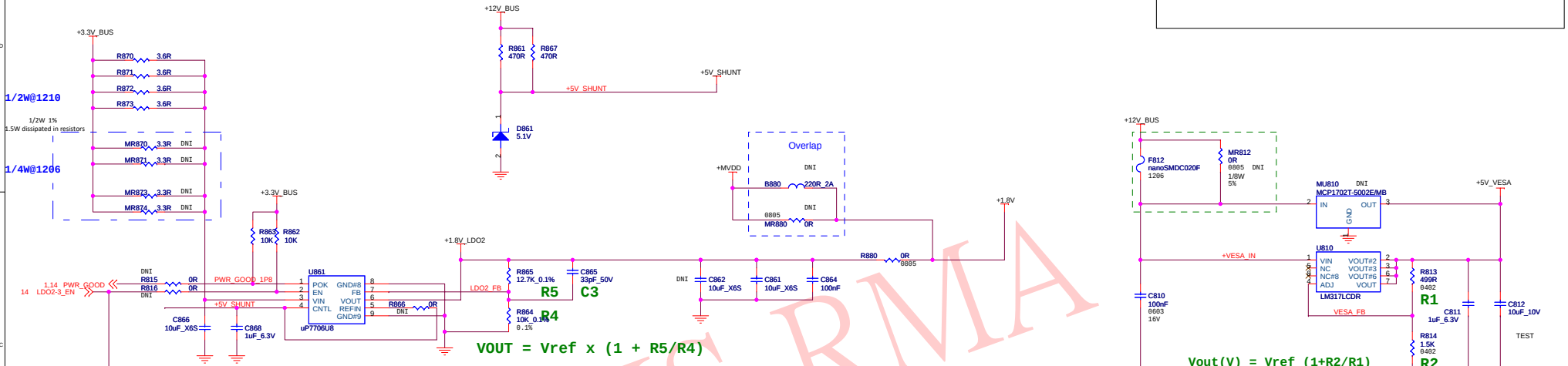
# (13) Linear Regulators

**LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX**
**PCB: 50 to 70mm sq. copper area for cooling**

**Regulators for +5V_VESA**

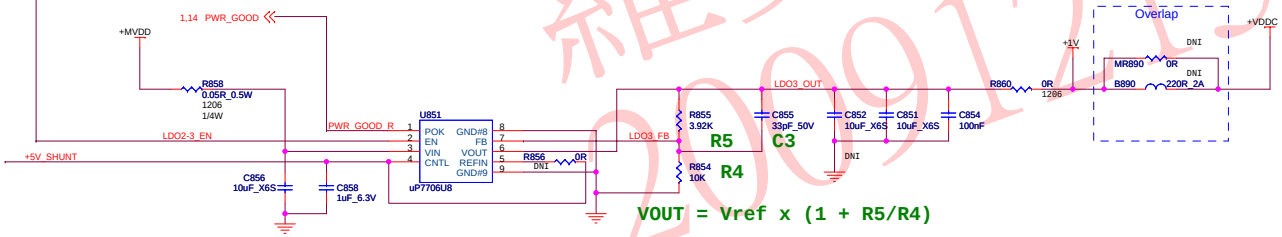


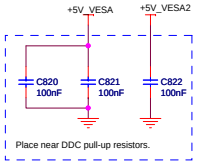


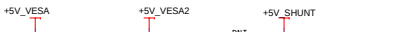


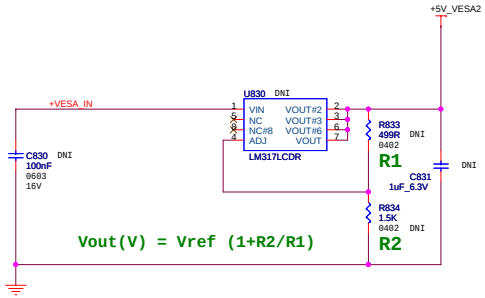

**LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX**
**PCB: 50 to 70mm sq. copper area for cooling**

| 1.0V WORST-CASE REQUIREMENT | |
|---|---|
| Display Config | Est. Current |
| DVI+HDMI+DP | 1560mA |





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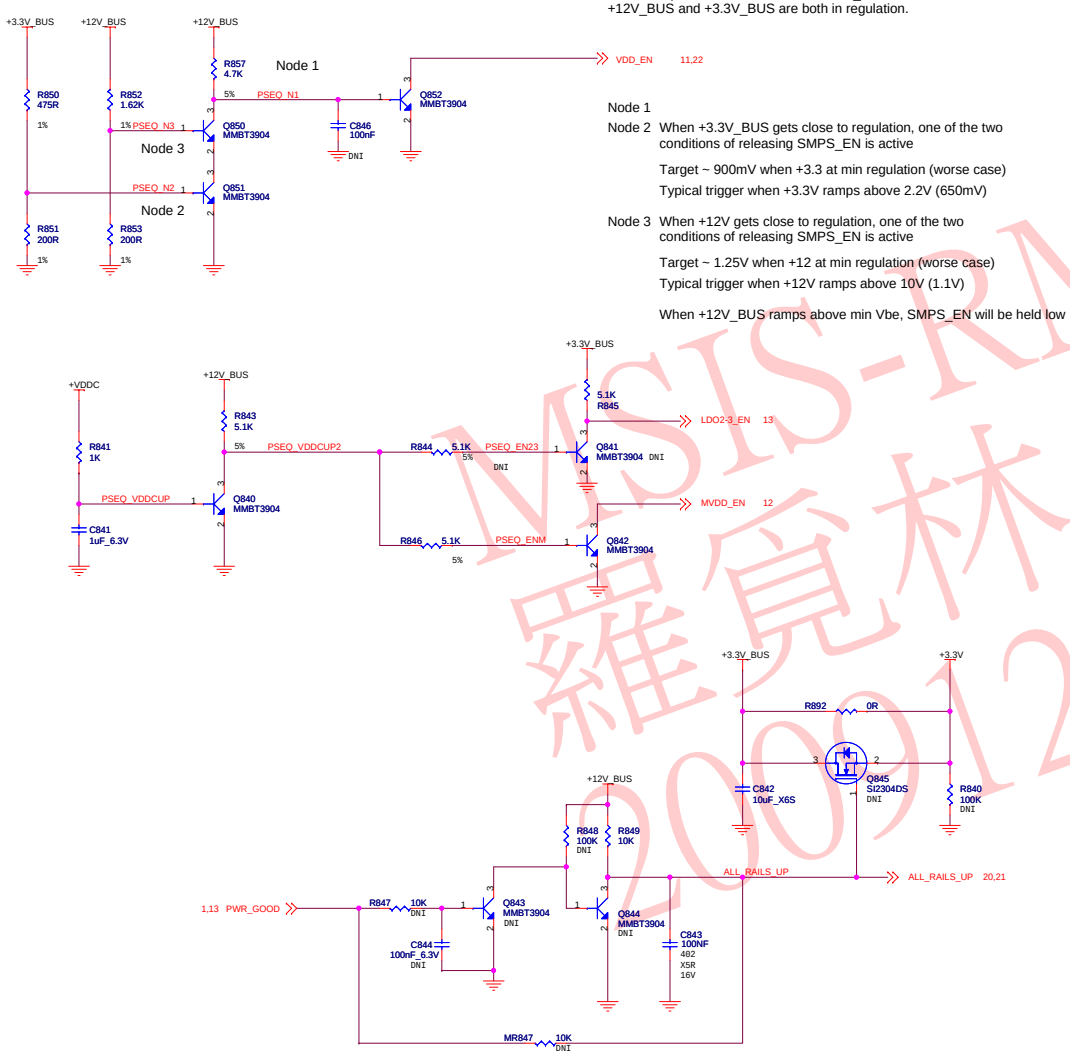
# (14) Power Management

## Power up/down Sequencing




Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation.

Node 1

Node 2 When +3.3V_BUS gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

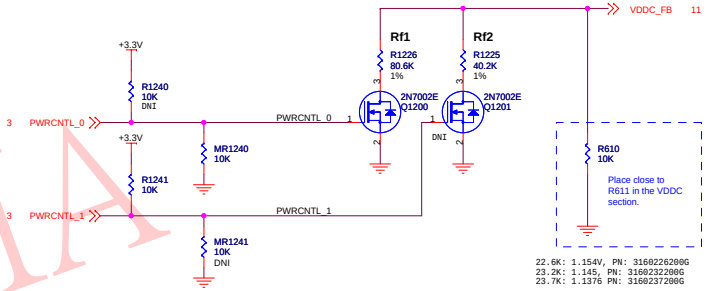
Typical trigger when +12V ramps above 10V (1.1V)

When +12V_BUS ramps above min Vbe, SMPS_EN will be held low

## Power Play

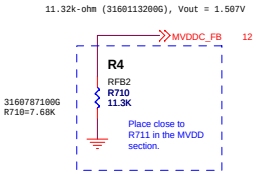
### VDDC Voltage Settings Using GPIOs

| PWRCNTL_1 GPIO_20 | PWRCNTL_0 GPIO_15 | Output Voltage (V) Rf1= Rf2= | | Rf1= Rf2= | Rf1= Rf2= | |
|---|---|---|---|---|---|---|
| 0 | 0 | | | | | |
| 0 | 1 | | | | | |
| 1 | 0 | | | | | |
| 1 | 1 | 1 | 0 | 1 | | Power-up Default |




### MVDD Voltage Settings Using GPIOs

| PWRCNTL_2 GPIO_6 | Output Voltage (V) Rf1= Rf2= | | Rf1= Rf2= | Rf1= Rf2= | |
|---|---|---|---|---|---|
| 0 | | | | | |
| 1 | 1 | 0 | 1 | | Power-up Default |





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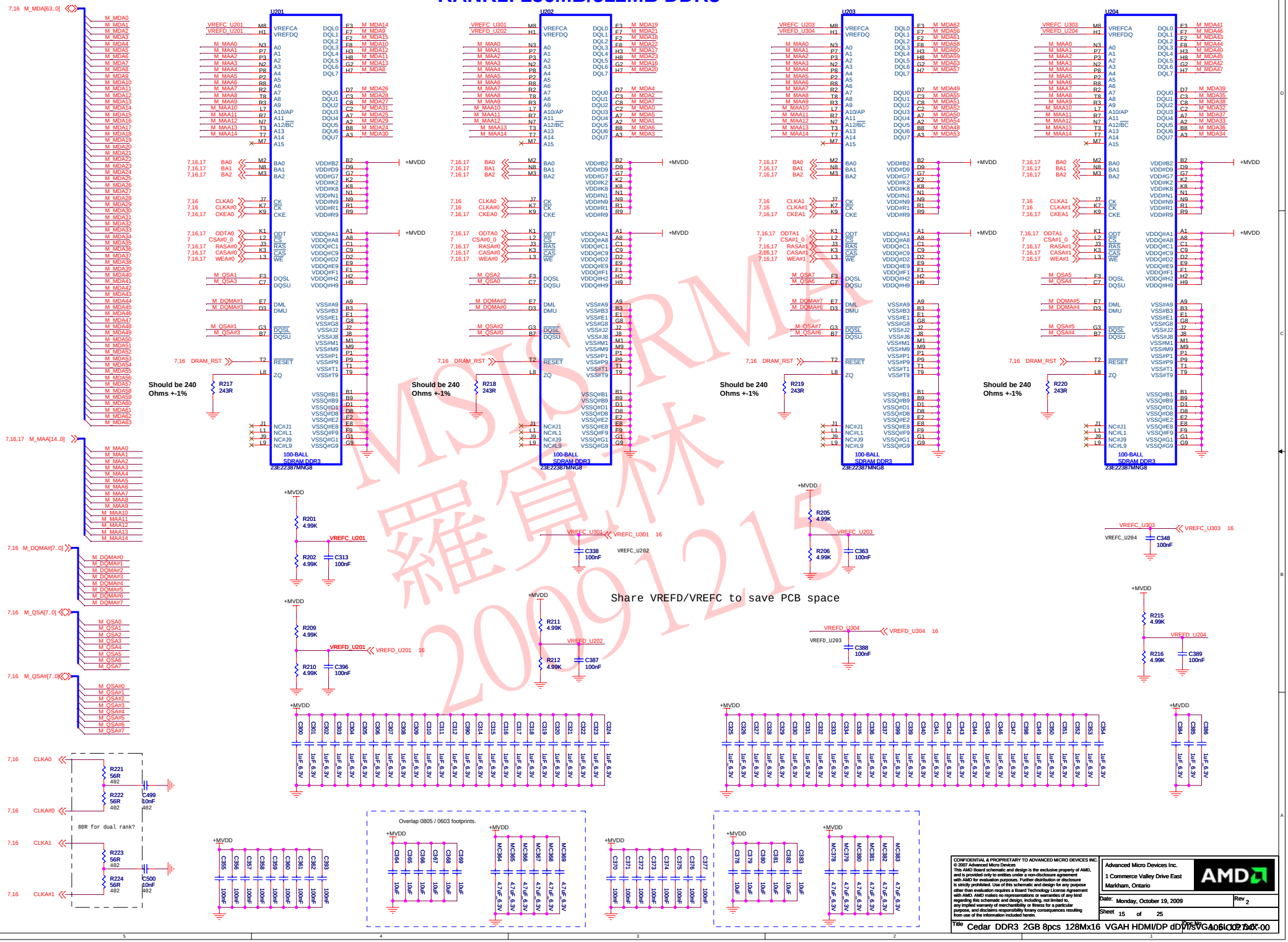
# (15) DDR3 RANK1

## RANK1: 256MB/512MB DDR3





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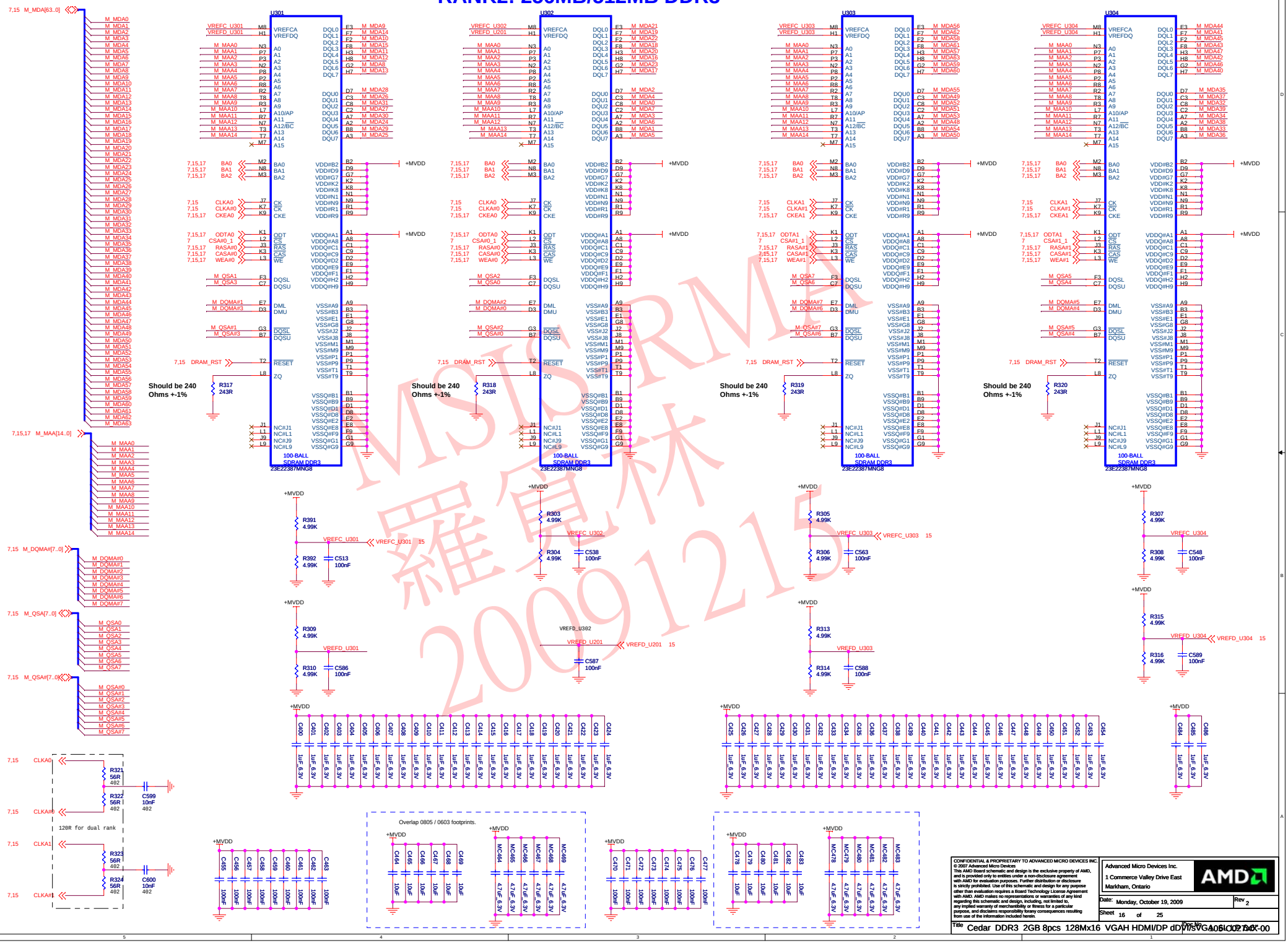
# (16) DDR3 RANK2

## RANK2: 256MB/512MB DDR3





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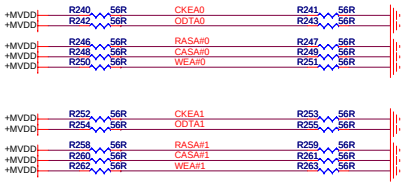
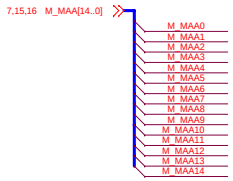
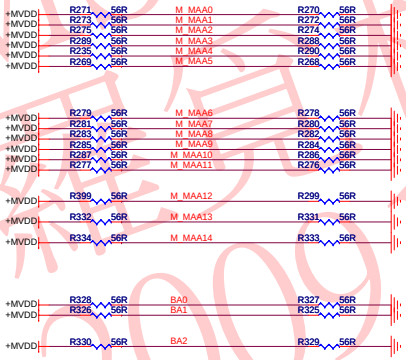
# (17) DDR3 Termination







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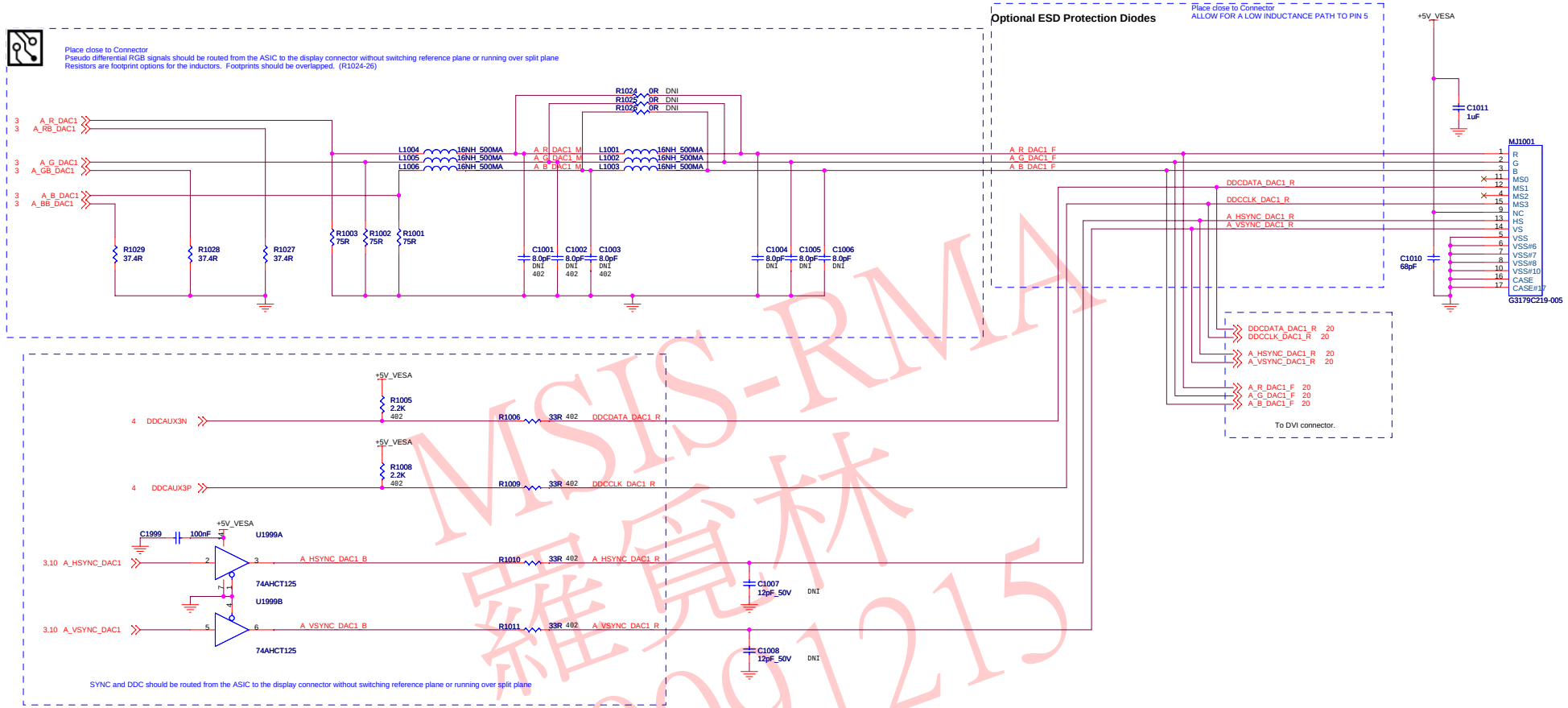
| Sheet 17 of 25 | |
| Title Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI/sVGA 05-10274-00 | Doc No 105-C02740-00 |

# (18) DAC1 OUTPUT

## DAC 1 OUTPUT





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Title Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI/sVGA 105-C02xxx-00

Doc No A05-C02xxx-00

# (19) DAC2 OUTPUT

## DAC 2 OUTPUT

Optional ESD Protection Diodes

Place near D2002, D2003, D2004, D2005

Place close to Connector

Pseudo differential RGB signals should be routed from the ASIC to the display connector without switching reference plane or running over split plane

3 A_R_DAC2
3 A_RB_DAC2
3 A_G_DAC2
3 A_GB_DAC2
3 A_B_DAC2
3 A_BB_DAC2

R2024 0R DNI
R2025 0R DNI
R2026 0R DNI

A_R_DAC2_M L2001 16NH_500MA
A_G_DAC2_M L2002 16NH_500MA
A_B_DAC2_M L2003 16NH_500MA

OVERLAP

R2029 37.4R
R2028 37.4R
R2027 37.4R
R2003 75R
R2002 75R
R2001 75R

C2004 8.0pF DNI
C2005 8.0pF DNI
C2006 8.0pF DNI

A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
A_HSYNC_DAC2_R
A_VSYNC_DAC2_R

+5V_VESA2
C2011 1uF
C2010 68pF

J2
A_R_DAC2_F
A_B_DAC2_F
A_G_DAC2_F
DDCDATA_DAC2_R
A_HSYNC_DAC2_R
DDCCLK_DAC2_R
A_VSYNC_DAC2_R
Header_16_Pin_2X8

**2X8 HEADER FOR VGA RIBBON CONNECTOR**

RV710: DDC2 is 5V tolerant. Do not install level shifter.
--> Do not install R2013, R2015, Q2001, Q2002. Install R2014, R2016.
RV810: DDC2 is NOT 5V tolerant. Install level shifter.
--> Do not install R2014, R2016. Install R2013, R2015, Q2001, Q2002.

+5V_VESA2
R2005 2.2K 402
4 DDC1DATA
R2006 33R 402 DDCDATA_DAC2_R

+5V_VESA2
R2008 2.2K 402
4 DDC1CLK
R2009 33R 402 DDCCLK_DAC2_R

U1999C 74AHCT125
3,10 A_HSYNC_DAC2
A_HSYNC_DAC2_B
R2010 33R 402 A_HSYNC_DAC2_R
C2007 12pF_50V

U1999D 74AHCT125
3,10 A_VSYNC_DAC2
A_VSYNC_DAC2_B
R2011 33R 402 A_VSYNC_DAC2_R
C2008 12pF_50V

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane





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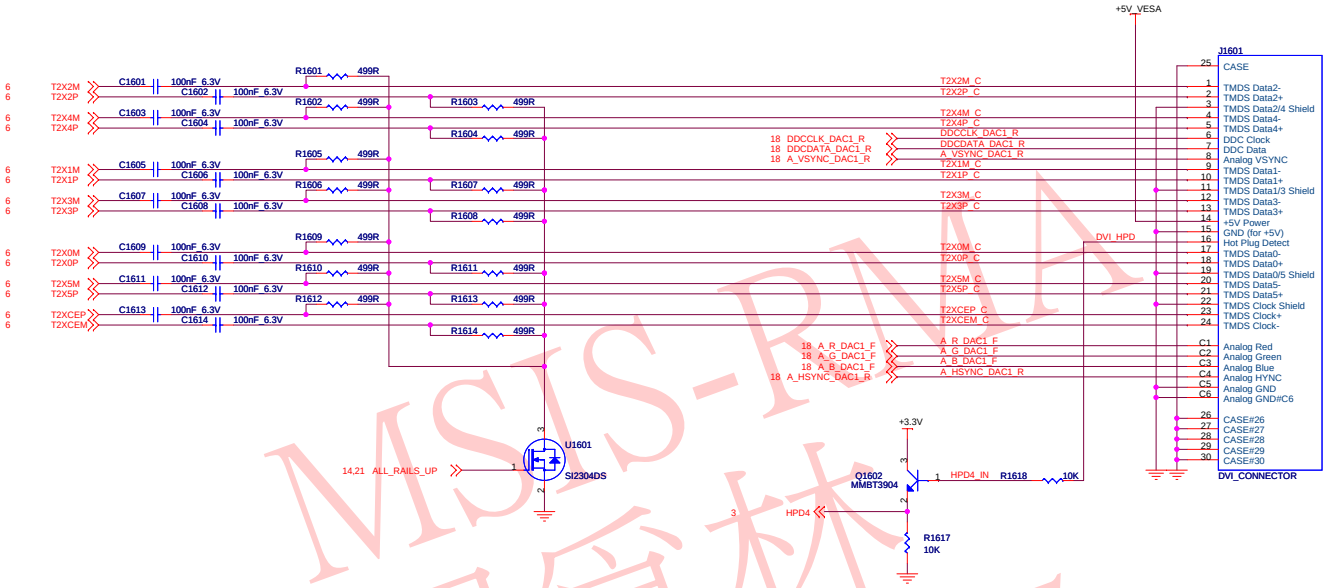
Title Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI/sVGA 105-C02xxx-00

Doc No 105-C02xxx-00

# (20) DVI OUTPUT

## DPE / DPF OUTPUT





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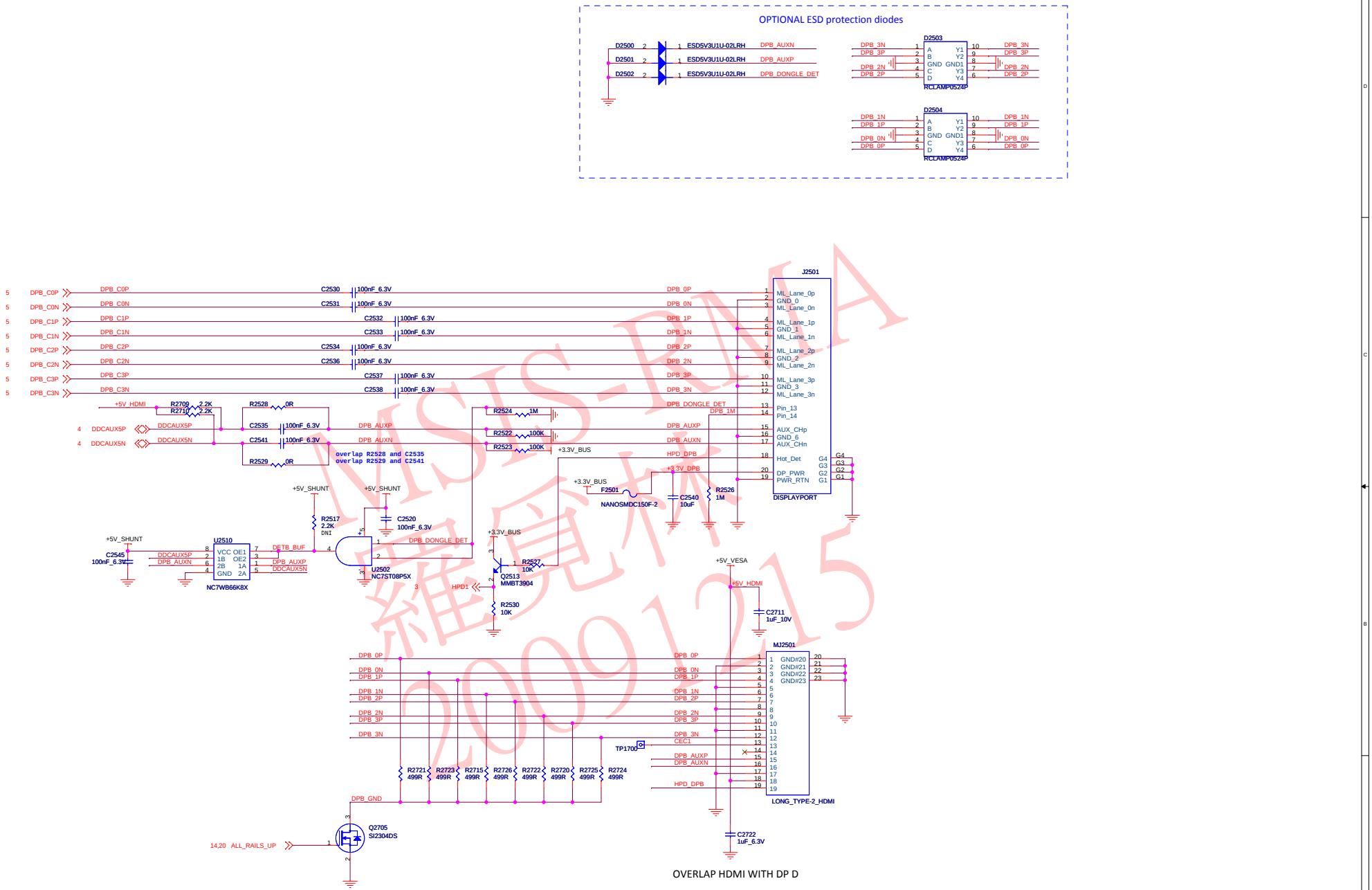
| Title | Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI/sVGA 216-0774000 |
| Doc No | 105-C02740-00B |



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| Date: | Monday, October 19, 2009 |
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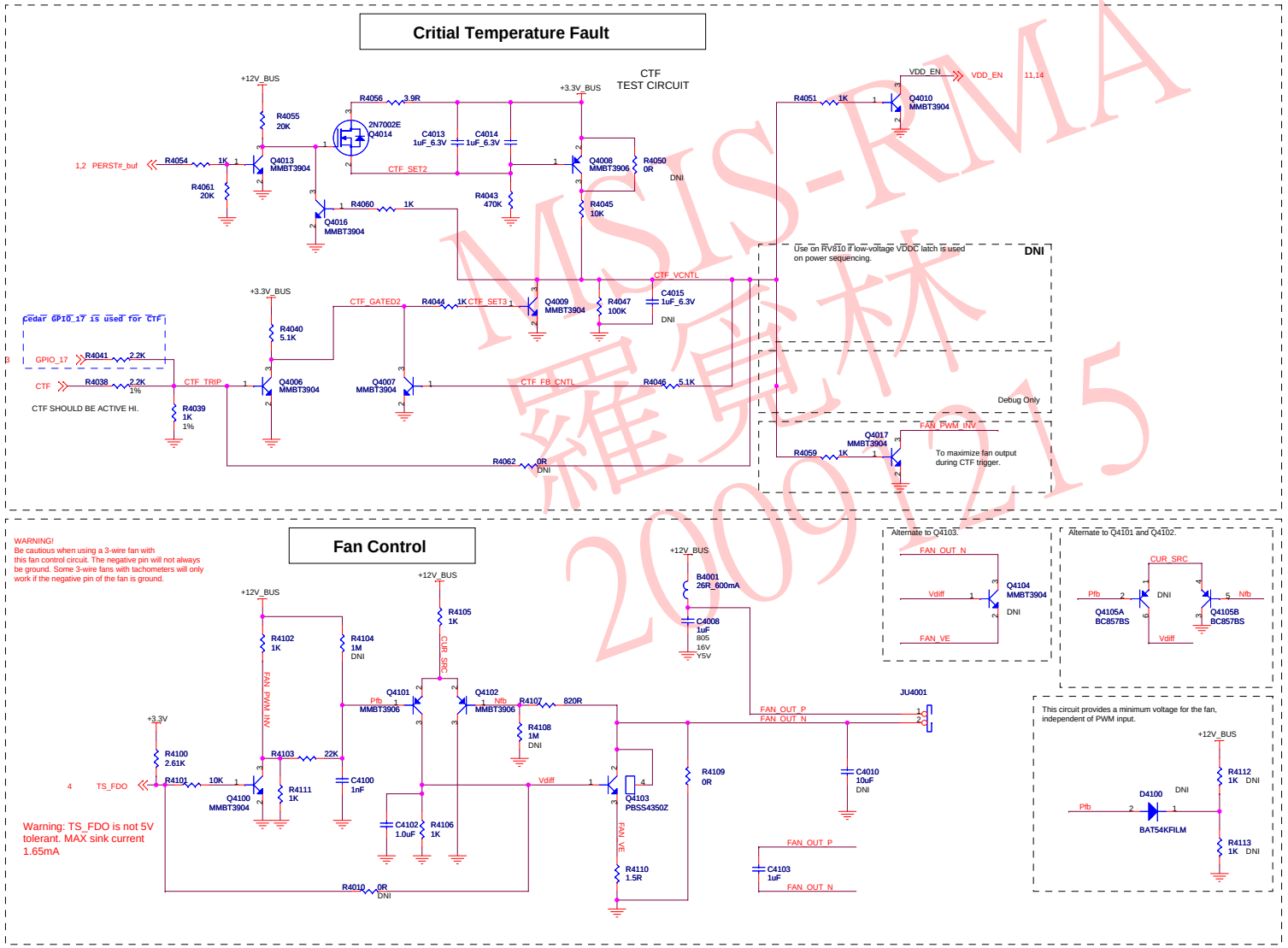
| Title | Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI/sVGA 05LC02200-00B |
| Doc No | A05LC02200 |

# (22) Thermal Management





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| Doc No | 105-C02240-00 |
| Title | Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI/sVGA 105-C02240-00 |

## For DVI Connector

ASSY-SCREW200
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW201
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

## Bracket Components

MT200
MT_Hole_3_4

ASSY-SCREW202
SCREW
SCREW

**7020005200G**

MT2
MT_Hole_0.136_in.

H3
HEATSINK

**Square Fansink 12W**

**7120036200G BLACK**

**7120336200G RED**

H1A RV610_FANSINK

**Rectangular Fansink 22W**

**7120035100G**

H1B RV610_FANSINK
H1C RV610_FANSINK
H1D RV610_FANSINK

**Dual-slot Heatsink 14W**

**7120181000G**

ASSY1
BRACKET
8020040100G

ASSY2
BRACKET
LP
8020040400G

| SKU | | P/N | CONFIGURATION | Form Factor |
|---|---|---|---|---|
| | PERCH | 8020051300G | DVI + DP + VGA | FH / SS |
| BASS | | 8020051400G | DVI +HDMI+ VGA | FH / SS |
| | PERCH | 8020051600G | DVI + DP | LP / SS |
| BASS | | 80200516A0G | DVI +HDMI | LP / SS |
| | PERCH | 8020051700G | DVI + DP + VGA | FH / DS |
| BASS | | 80200517A0G | DVI +HDMI+ VGA | FH / DS |





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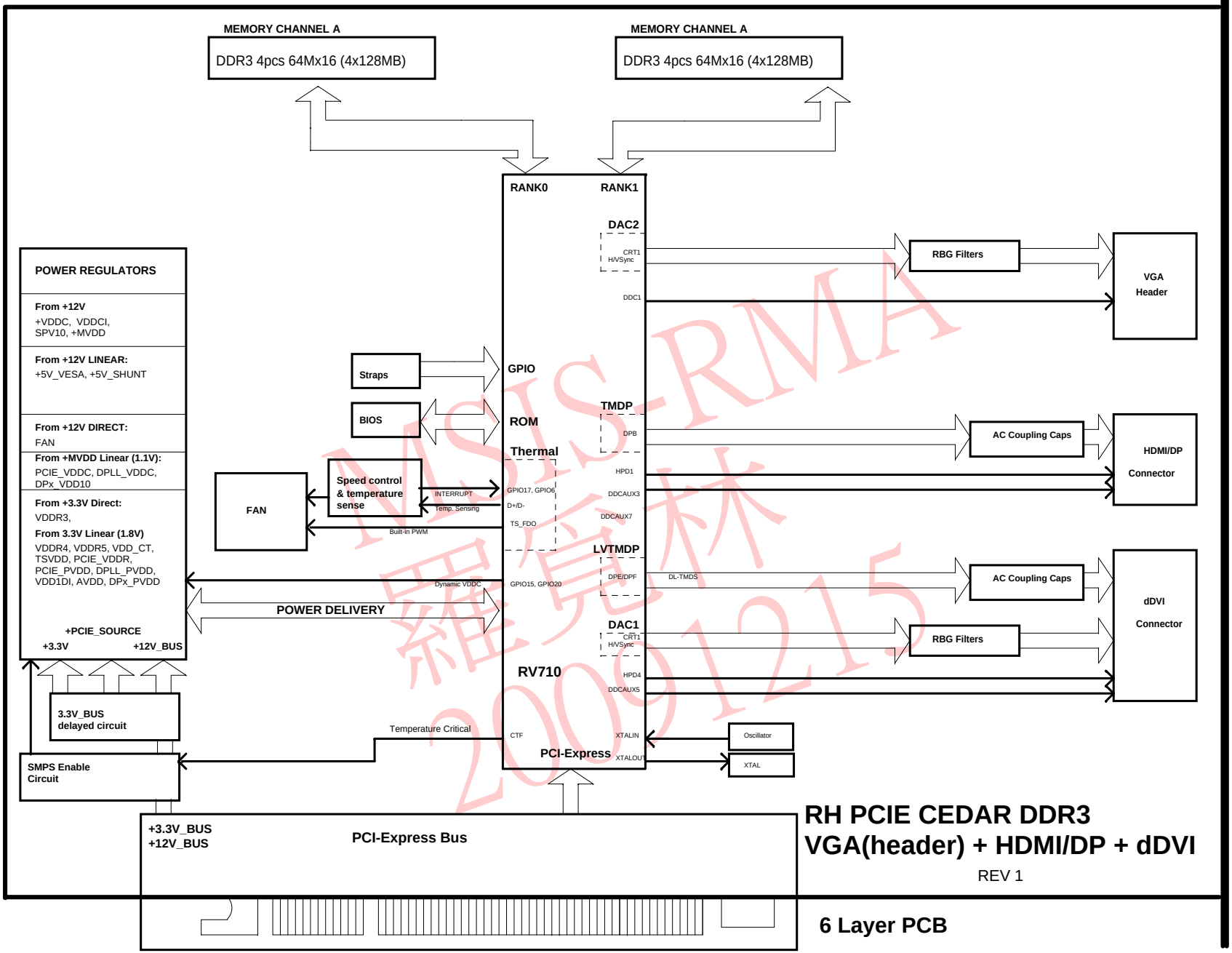
Title Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI/sVGA 215-0912XX-00B

Doc No 105-C12XXX




# RH PCIE CEDAR DDR3
# VGA(header) + HDMI/DP + dDVI

REV 1

**6 Layer PCB**





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| Doc No | 105-C02240-00 |

| Title | Schematic No. | Date: |
|---|---|---|
| Cedar DDR3 2GB 8pcs 128Mx16 VGAH HDMI/DP dDVI/sVGA 6L LP 6.6" | 105-C027XX-00 | Friday, October 16, 2009 |

# REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
**For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.**
**Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 2

## Cedar 1GB DDR3 Walleye

| Sch Rev | PCB Rev | Date | REVISION DESCRIPTION |
|---|---|---|---|
| 0 | 00A | 2008.12.30 | Sch no change. just modify HDMI connector location on PCB |
| 1 | 00B | 2009.08.24 | Page 1:remove C1,C2,R3,U3,Add Q1,Q2<br>Page 7:Add C97,C98<br>Page 10:Add MR43,MR51,MR52,MR56<br>Page 18:Add L1004,L1005,L1006<br>Page 19:Remove R2013,R2014,R2015,R2016,Q2001,Q2002 |
| 2 | 00 | 2009.09.23 | Change HDMI/DP DDC line to DDCAUX3 |