文曄科技
WT MICROELECTRONICS
地址：台北縣中和市中正路 738 號 14 樓
14F., NO.738,CHUNG CHENG ROAD ., CHUNG HO CITY ,
TAIPEI HSIEN, TAIWAN, R.O.C
TEL:(02)8226-9088 FAX:(02)8226-9099

承 認 書
APPROVAL SHEET

□	送測日期 ： TEST DATE	26-Feb-14
□	客戶名稱 ： CUSTOMER	技嘉科技股份有限公司
□	品 名 ： PART NAME	FDMF6823C 10IFD-506823-01R
□	廠 牌 ： BRAND	FAIRCHILD
□	包 裝 ： PACKAGE	Power 66
□	承認日期 ： APPROVED DATE	26-Feb-14

電子類元件 零件承認書文件 CHECK LIST

零件廠商：FAIRCHILD

品名規格：FDMF6823C **技嘉料號：10IFD-506823-01R**

項次	文件項目
Data Sheet 檢核項目	
1	DATASHEET (含機構尺寸、**端子腳鍍層材質、MSL Report**)
2	零件 Making 文字面說明
3	零件 Part Number 說明
4	零件 Qualification Test Report
5	料件包裝方式及包裝 Label 之零件 Part number 說明
6	UL Safety Report (If Request)
7	零件耐溫焊接 Profile(包含最高耐焊溫度,時間，焊接/過爐次數與曲線圖)。**註 2**
8	零件樣品 20PCS(Chipset 等高單價， 至少 1PCS)
9	**主動電子零件承認基本調查表。註 3**
10	以上資料電子檔為 PDF 檔，且是同 1 個 File
GPMS 綠色產品管理系統-物料管制文件檢核清單	
物料管制文件 1	GPMS 綠色產品管理系統：零件照片
物料管制文件 2	GPMS 綠色產品管理系統：不使用禁用物質證明書 (保證書)。**註 4**
物料管制文件 3	GPMS 綠色產品管理系統：Data Sheet
GPMS 綠色產品管理系統-MCD 表格	
MCD 表格	物質內容宣告表格 (Material Content Declaration, MCD)
其他文件 (僅適用電阻、電容類之系列元件)	
附件 1	危害物質測試報告 Test Report of Hazardous Substances。**註 5**
附件 2	元件調查表 Component Composition Table

※ 1. 各項說明文件內容應明訂零件交貨時之規格、方式；如捲盤、文字印刷為雷射或油墨等
※ 2. 零件耐溫焊接 Profile 需附相關測試報告 (國際認證之實驗室資格單位所出具之測試報告)
※ **3. 主動電子零件適用(技嘉)料號：積體電路(IC) 10H*,10T*,10I*,10D*,10G***
※ 4. 物料管制文件 2：網通事業群之所屬料件須一併提交 “不使用禁用物質證明書(保證書)+ REACH 調查表”
※ 5. 危害物質測試報告 Test Report of Hazardous Substances：泛指為具有 ISO/IEC 17025 國際認證之實驗室資格單位所出具之測試報告

主動電子零件承認基本調查表

Version R4

一、原物料規格/來源			
項次	部位名稱/規格	材質	原物料來源產地
1	Lead/Ball Finish	Matte Tin (Sn)	Philippines
2			
3			
4			

二、晶圓廠					
項次	工廠名稱	生產產地	Wafer (吋)	投產率(%)	自有/外包
1	Texas Instruments	Philippines			
2					
3					

三、封裝廠				
項次	工廠名稱	生產產地	投產比率(%)	自有/外包
1	Texas Instruments	Philippines		
2				
3				

四、產能	
總產能(月/PCS)	可供技嘉產能(月/PCS)

※ 1. 晶圓廠、封裝廠之所有 AVL 請均表列，並提供相關資訊與文件。當異動（包含 AVL 或相關資訊文件之異動）時，請主動通知技嘉研發管理與 CE 單位，並更新文件

※ 2. 以上資訊欄位若有不足，可自行增加行數

FAIRCHILD SEMICONDUCTOR®

April 2013

FDMF6823C — Extra-Small, High-Performance, High-Frequency DrMOS Module

Benefits

- Ultra-Compact 6x6 mm PQFN, 72% Space-Saving Compared to Conventional Discrete Solutions
- Fully Optimized System Efficiency
- Clean Switching Waveforms with Minimal Ringing
- High-Current Handling

Features

- Over 93% Peak-Efficiency
- High-Current Handling: 50 A
- High-Performance PQFN Copper-Clip Package
- 3-State 5 V PWM Input Driver
- Skip-Mode SMOD# (Low-Side Gate Turn Off) Input
- Thermal Warning Flag for Over-Temperature Condition
- Driver Output Disable Function (DISB# Pin)
- Internal Pull-Up and Pull-Down for SMOD# and DISB# Inputs, Respectively
- Fairchild PowerTrench® Technology MOSFETs for Clean Voltage Waveforms and Reduced Ringing
- Fairchild SyncFET™ (Integrated Schottky Diode) Technology in Low-Side MOSFET
- Integrated Bootstrap Schottky Diode
- Adaptive Gate Drive Timing for Shoot-Through Protection
- Under-Voltage Lockout (UVLO)
- Optimized for Switching Frequencies up to 1 MHz
- Low-Profile SMD Package
- Fairchild Green Packaging and RoHS Compliance
- Based on the Intel® 4.0 DrMOS Standard

Description

The XS™ DrMOS family is Fairchild's next-generation, fully optimized, ultra-compact, integrated MOSFET plus driver power stage solution for high-current, high-frequency, synchronous buck DC-DC applications. The FDMF6823C integrates a driver IC, two power MOSFETs, and a bootstrap Schottky diode into a thermally enhanced, ultra-compact 6x6 mm package.

With an integrated approach, the complete switching power stage is optimized with regard to driver and MOSFET dynamic performance, system inductance, and power MOSFET $R_{DS(ON)}$. XS™ DrMOS uses Fairchild's high-performance PowerTrench® MOSFET technology, which dramatically reduces switch ringing, eliminating the need for snubber circuit in most buck converter applications.

A driver IC with reduced dead times and propagation delays further enhances the performance. A thermal warning function warns of a potential over-temperature situation. The FDMF6823C also incorporates a Skip Mode (SMOD#) for improved light-load efficiency. The FDMF6823C also provides a 3-state 5V PWM input for compatibility with a wide range of PWM controllers.

Applications

- High-Performance Gaming Motherboards
- Compact Blade Servers, V-Core and Non-V-Core DC-DC Converters
- Desktop Computers, V-Core and Non-V-Core DC-DC Converters
- Workstations
- High-Current DC-DC Point-of-Load Converters
- Networking and Telecom Microprocessor Voltage Regulators
- Small Form-Factor Voltage Regulator Modules

Ordering Information

Part Number	Current Rating	Package	Top Mark
FDMF6823C	50 A	40-Lead, Clipbond PQFN DrMOS, 6.0 mm x 6.0 mm Package	FDMF6823C

Typical Application Circuit

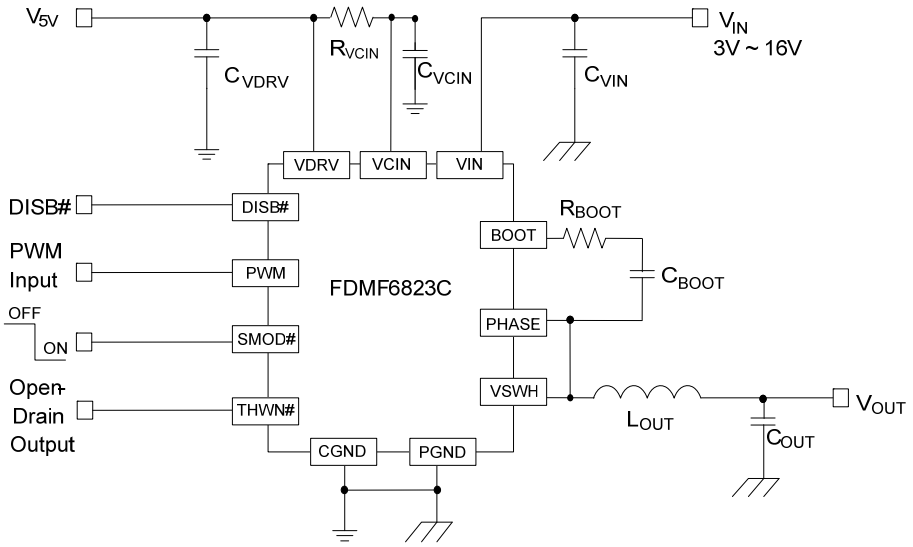


Figure 1. Typical Application Circuit

DrMOS Block Diagram

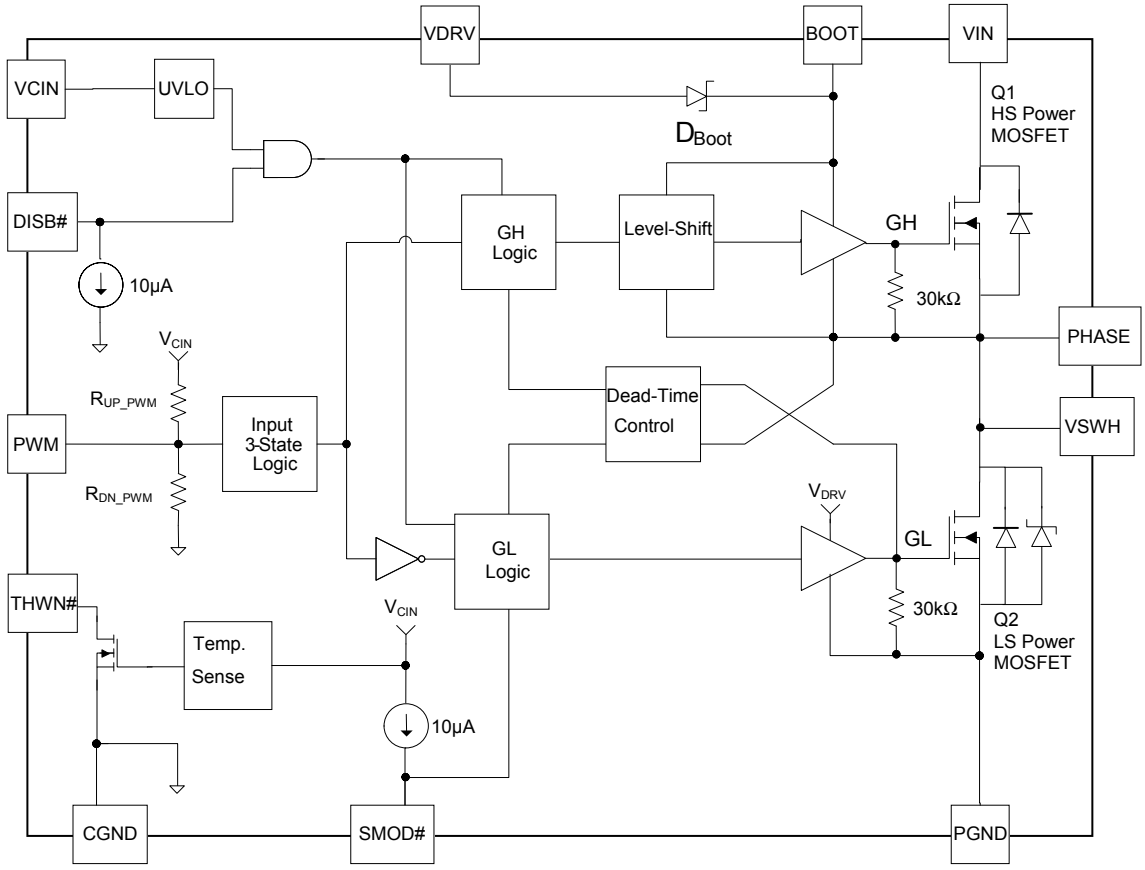


Figure 2. DrMOS Block Diagram

Pin Configuration

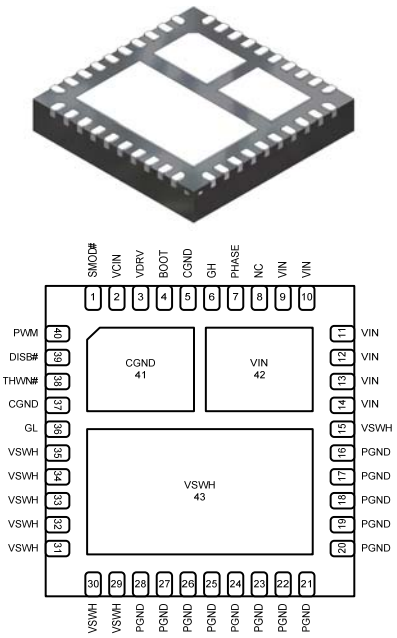


Figure 3. Bottom View

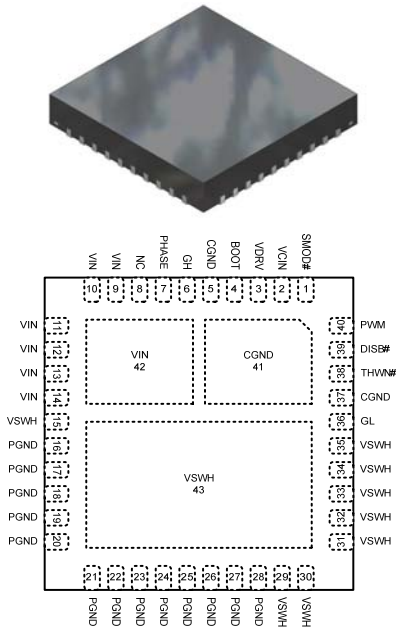


Figure 4. Top View

Pin Definitions

Pin #	Name	Description
1	SMOD#	When SMOD#=HIGH, the low-side driver is the inverse of the PWM input. When SMOD#=LOW, the low-side driver is disabled. This pin has a 10 µA internal pull-up current source. Do not add a noise filter capacitor.
2	VCIN	IC bias supply. Minimum 1 µF ceramic capacitor is recommended from this pin to CGND.
3	VDRV	Power for the gate driver. Minimum 1 µF ceramic capacitor is recommended to be connected as close as possible from this pin to CGND.
4	BOOT	Bootstrap supply input. Provides voltage supply to the high-side MOSFET driver. Connect a bootstrap capacitor from this pin to PHASE.
5, 37, 41	CGND	IC ground. Ground return for driver IC.
6	GH	For manufacturing test only. This pin must float; it must not be connected to any pin.
7	PHASE	Switch node pin for bootstrap capacitor routing. Electrically shorted to VSWH pin.
8	NC	No connect. The pin is not electrically connected internally, but can be connected to VIN for convenience.
9 - 14, 42	VIN	Power input. Output stage supply voltage.
15, 29 - 35, 43	VSWH	Switch node input. Provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-through protection.
16 – 28	PGND	Power ground. Output stage ground. Source pin of the low-side MOSFET.
36	GL	For manufacturing test only. This pin must float; it must not be connected to any pin.
38	THWN#	Thermal warning flag, open collector output. When temperature exceeds the trip limit, the output is pulled LOW. THWN# does not disable the module.
39	DISB#	Output disable. When LOW, this pin disables the power MOSFET switching (GH and GL are held LOW). This pin has a 10 µA internal pull-down current source. Do not add a noise filter capacitor.
40	PWM	PWM signal input. This pin accepts a three-state 5 V PWM signal from the controller.

Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CIN}	Supply Voltage	Referenced to CGND	-0.3	6.0	V
V_{DRV}	Drive Voltage	Referenced to CGND	-0.3	6.0	V
$V_{DISB\#}$	Output Disable	Referenced to CGND	-0.3	6.0	V
V_{PWM}	PWM Signal Input	Referenced to CGND	-0.3	6.0	V
$V_{SMOD\#}$	Skip Mode Input	Referenced to CGND	-0.3	6.0	V
V_{GL}	Low Gate Manufacturing Test Pin	Referenced to CGND	-0.3	6.0	V
$V_{THWN\#}$	Thermal Warning Flag	Referenced to CGND	-0.3	6.0	V
V_{IN}	Power Input	Referenced to PGND, CGND	-0.3	25.0	V
V_{BOOT}	Bootstrap Supply	Referenced to VSWH, PHASE	-0.3	6.0	V
		Referenced to CGND	-0.3	25.0	V
V_{GH}	High Gate Manufacturing Test Pin	Referenced to VSWH, PHASE	-0.3	6.0	V
		Referenced to CGND	-0.3	25.0	V
V_{PHS}	PHASE	Referenced to CGND	-0.3	25.0	V
V_{SWH}	Switch Node Input	Referenced to PGND, CGND (DC Only)	-0.3	25.0	V
		Referenced to PGND, <20 ns	-8.0	28.0	V
V_{BOOT}	Bootstrap Supply	Referenced to VDRV		22.0	V
		Referenced to VDRV, <20 ns		25.0	V
$I_{THWN\#}$	THWN# Sink Current		-0.1	7.0	mA
$I_{O(AV)}$	Output Current[1]	f_{SW}=300 kHz, V_{IN}=12 V, V_O=1.0 V		50	A
		f_{SW}=1 MHz, V_{IN}=12 V, V_O=1.0 V		45	
θ_{JPCB}	Junction-to-PCB Thermal Resistance			2.7	°C/W
T_A	Ambient Temperature Range		-40	+125	°C
T_J	Maximum Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
ESD	Electrostatic Discharge Protection	Human Body Model, JESD22-A114	2000		V
		Charged Device Model, JESD22-C101	2500		

Note:

1. $I_{O(AV)}$ is rated using Fairchild's DrMOS evaluation board, at T_A = 25°C, with natural convection cooling. This rating is limited by the peak DrMOS temperature, T_J = 150°C, and varies depending on operating conditions and PCB layout. This rating can be changed with different application settings.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CIN}	Control Circuit Supply Voltage	4.5	5.0	5.5	V
V_{DRV}	Gate Drive Circuit Supply Voltage	4.5	5.0	5.5	V
V_{IN}	Output Stage Supply Voltage	3.0	12.0	16.0[2]	V

Note:

2. Operating at high V_{IN} can create excessive AC overshoots on the VSWH-to-GND and BOOT-to-GND nodes during MOSFET switching transients. For reliable DrMOS operation, VSWH-to-GND and BOOT-to-GND must remain at or below the Absolute Maximum Ratings shown in the table above. *Refer to the "Application Information" and "PCB Layout Guidelines" sections of this datasheet for additional information*.

Electrical Characteristics

Typical values are V_{IN} = 12 V, V_{CIN} = 5 V, V_{DRV} = 5 V, and $T_A = T_J$ = +25°C unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Basic Operation						
I_Q	Quiescent Current	$I_Q=I_{VCIN}+I_{VDRV}$, PWM=LOW or HIGH or Float			2	mA
V_{UVLO}	UVLO Threshold	V_{CIN} Rising	2.9	3.1	3.3	V
V_{UVLO_Hys}	UVLO Hysteresis			0.4		V
PWM Input (V_{CIN} = V_{DRV} = 5 V ±10%)						
R_{UP_PWM}	Pull-Up Impedance	V_{PWM}=5 V		10		kΩ
R_{DN_PWM}	Pull-Down Impedance	V_{PWM}=0 V		10		kΩ
V_{IH_PWM}	PWM High Level Voltage		3.04	3.55	4.05	V
V_{TRI_HI}	3-State Upper Threshold		2.95	3.45	3.94	V
V_{TRI_LO}	3-State Lower Threshold		0.98	1.25	1.52	V
V_{IL_PWM}	PWM Low Level Voltage		0.84	1.15	1.42	V
$t_{D\_HOLD-OFF}$	3-State Shut-Off Time			160	200	ns
V_{HiZ_PWM}	3-State Open Voltage		2.20	2.50	2.80	V
$t_{PWM-OFF\_MIN}$	PWM Minimum Off Time		120			ns
PWM Input (V_{CIN} = V_{DRV} = 5 V ±5%)						
R_{UP_PWM}	Pull-Up Impedance	V_{PWM}=5 V		10		kΩ
R_{DN_PWM}	Pull-Down Impedance	V_{PWM}=0 V		10		kΩ
V_{IH_PWM}	PWM High Level Voltage		3.22	3.55	3.87	V
V_{TRI_HI}	3-State Upper Threshold		3.13	3.45	3.77	V
V_{TRI_LO}	3-State Lower Threshold		1.04	1.25	1.46	V
V_{IL_PWM}	PWM Low Level Voltage		0.90	1.15	1.36	V
$t_{D\_HOLD-OFF}$	3-State Shut-Off Time			160	200	ns
V_{HiZ_PWM}	3-State Open Voltage		2.30	2.50	2.70	V
$t_{PWM-OFF\_MIN}$	PWM Minimum Off Time		120			ns
DISB# Input						
V_{IH_DISB}	High-Level Input Voltage		2			V
V_{IL_DISB}	Low-Level Input Voltage				0.8	V
I_{PLD}	Pull-Down Current			10		µA
t_{PD_DISBL}	Propagation Delay	PWM=GND, Delay Between DISB# from HIGH to LOW to GL from HIGH to LOW		25		ns
t_{PD_DISBH}	Propagation Delay	PWM=GND, Delay Between DISB# from LOW to HIGH to GL from LOW to HIGH		25		ns
SMOD# Input						
V_{IH_SMOD}	High-Level Input Voltage		2			V
V_{IL_SMOD}	Low-Level Input Voltage				0.8	V
I_{PLU}	Pull-Up Current			10		µA
t_{PD_SLGLL}	Propagation Delay	PWM=GND, Delay Between SMOD# from HIGH to LOW to GL from HIGH to LOW		10		ns
t_{PD_SHGLH}	Propagation Delay	PWM=GND, Delay Between SMOD# from LOW to HIGH to GL from LOW to HIGH		10		ns

Continued on the following page…

Electrical Characteristics

Typical values are V_{IN} = 12 V, V_{CIN} = 5 V, V_{DRV} = 5 V, and $T_A = T_J$ = +25°C unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Thermal Warning Flag						
T_{ACT}	Activation Temperature			150		°C
T_{RST}	Reset Temperature			135		°C
R_{THWN}	Pull-Down Resistance	I_{PLD}=5 mA		30		Ω
250 ns Timeout Circuit						
$t_{D\_TIMEOUT}$	Timeout Delay	SW=0 V, Delay Between GH from HIGH to LOW and GL from LOW to HIGH		250		ns
High-Side Driver (f_{SW} = 1000 kHz, I_{OUT} = 30 A, T_A = +25°C)						
R_{SOURCE_GH}	Output Impedance, Sourcing	Source Current=100 mA		1		Ω
R_{SINK_GH}	Output Impedance, Sinking	Sink Current=100 mA		0.8		Ω
t_{R_GH}	Rise Time	GH=10% to 90%		10		ns
t_{F_GH}	Fall Time	GH=90% to 10%		10		ns
t_{D_DEADON}	LS to HS Deadband Time	GL Going LOW to GH Going HIGH, 1.0 V GL to 10% GH		15		ns
t_{PD_PLGHL}	PWM LOW Propagation Delay	PWM Going LOW to GH Going LOW, V_{IL_PWM} to 90% GH		20	30	ns
t_{PD_PHGHH}	PWM HIGH Propagation Delay (SMOD# =0)	PWM Going HIGH to GH Going HIGH, V_{IH_PWM} to 10% GH (SMOD# =0, I_{D_LS}>0)		30		ns
t_{PD_TSGHH}	Exiting 3-State Propagation Delay	PWM (From 3-State) Going HIGH to GH Going HIGH, V_{IH_PWM} to 10% GH		30		ns
Low-Side Driver (f_{SW} = 1000 kHz, I_{OUT} = 30 A, T_A = +25°C)						
R_{SOURCE_GL}	Output Impedance, Sourcing	Source Current=100 mA		1		Ω
R_{SINK_GL}	Output Impedance, Sinking	Sink Current=100 mA		0.5		Ω
t_{R_GL}	Rise Time	GL=10% to 90%		20		ns
t_{F_GL}	Fall Time	GL=90% to 10%		10		ns
$t_{D\_DEADOFF}$	HS to LS Deadband Time	SW Going LOW to GL Going HIGH, 2.2 V SW to 10% GL		15		ns
t_{PD_PHGLL}	PWM-HIGH Propagation Delay	PWM Going HIGH to GL Going LOW, V_{IH_PWM} to 90% GL		10	25	ns
t_{PD_TSGLH}	Exiting 3-State Propagation Delay	PWM (From 3-State) Going LOW to GL Going HIGH, V_{IL_PWM} to 10% GL		20		ns
Boot Diode						
V_F	Forward-Voltage Drop	I_F=20 mA		0.3		V
V_R	Breakdown Voltage	I_R=1 mA	22			V

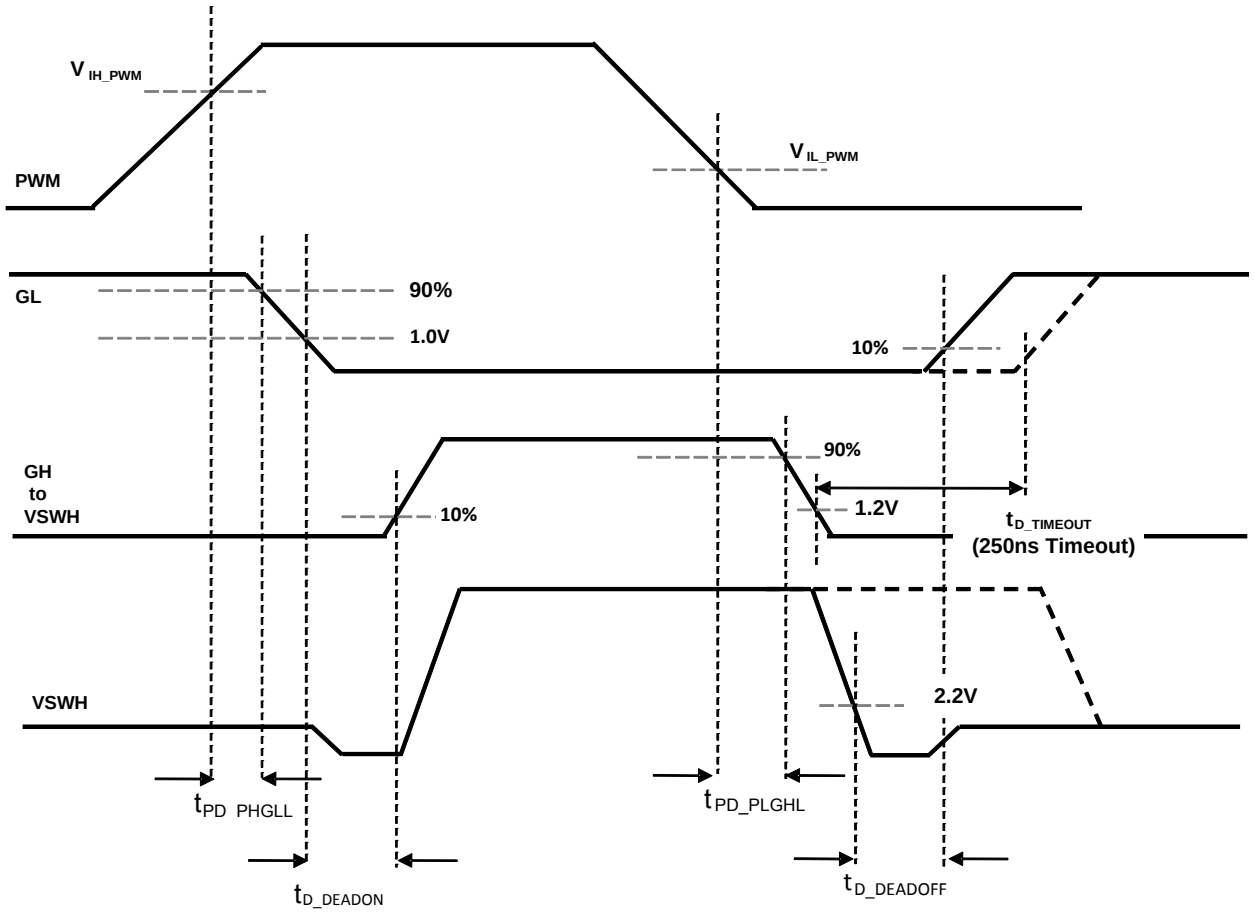


Figure 5. PWM Timing Diagram

Typical Performance Characteristics

Test Conditions: V_{IN}=12 V, V_{OUT}=1 V, V_{CIN}=5 V, V_{DRV}=5 V, L_{OUT}=250 nH, T_A=25°C, and natural convection cooling, unless otherwise specified.

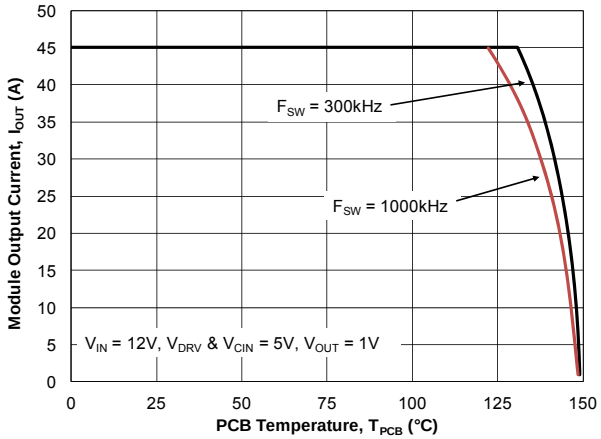


Figure 6. Safe Operating Area

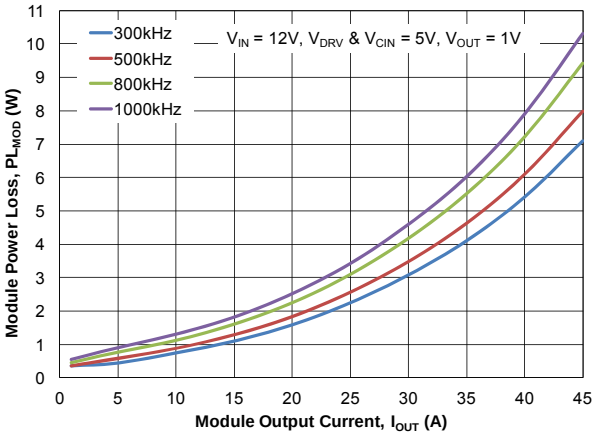


Figure 7. Power Loss vs. Output Current

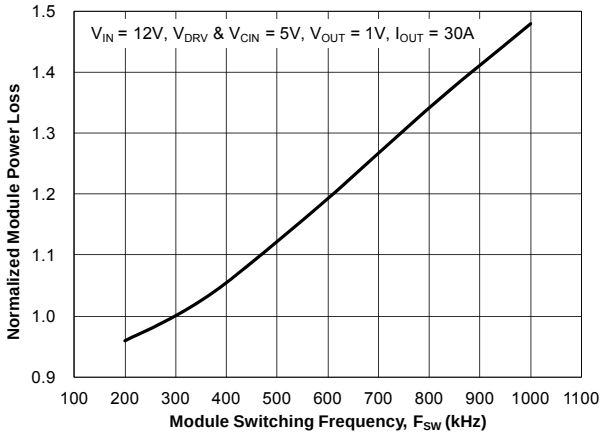


Figure 8. Power Loss vs. Switching Frequency

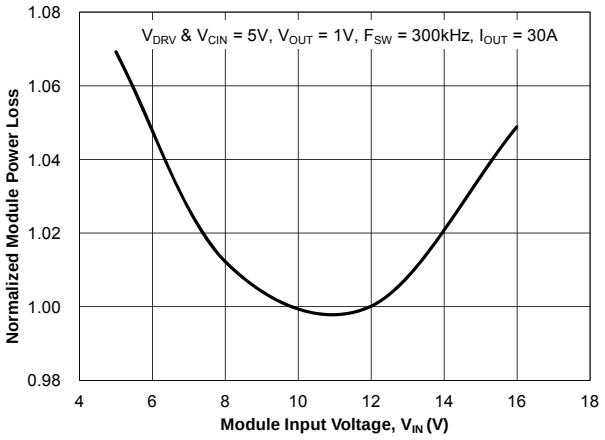


Figure 9. Power Loss vs. Input Voltage

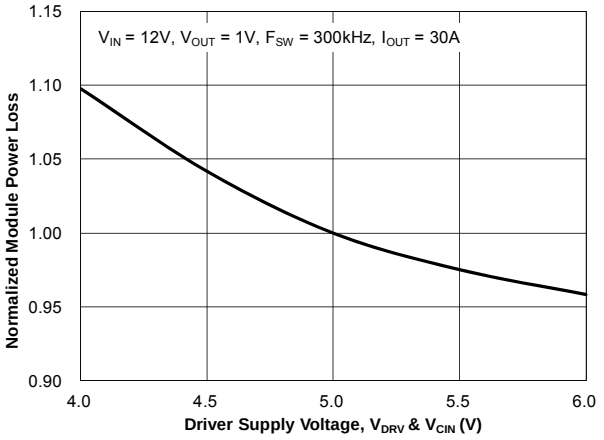


Figure 10. Power Loss vs. Driver Supply Voltage

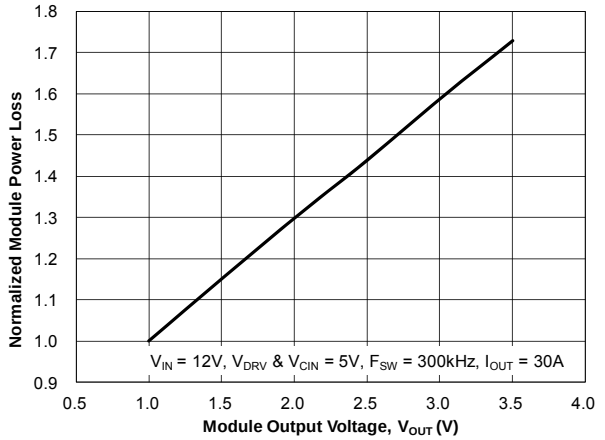


Figure 11. Power Loss vs. Output Voltage

Typical Performance Characteristics

Test Conditions: V_{IN}=12 V, V_{OUT}=1 V, V_{CIN}=5 V, V_{DRV}=5 V, L_{OUT}=250 nH, T_A=25°C, and natural convection cooling, unless otherwise specified.

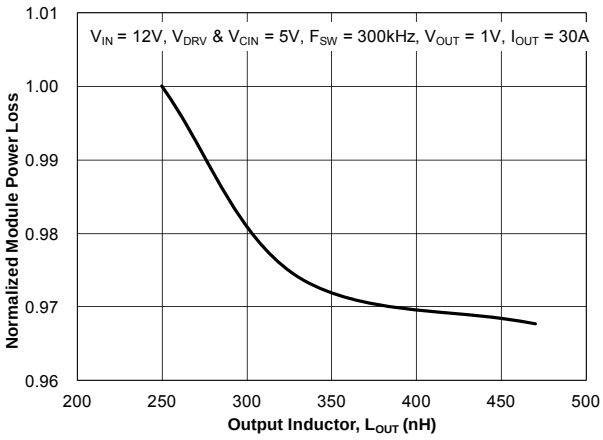


Figure 12. Power Loss vs. Output Inductor

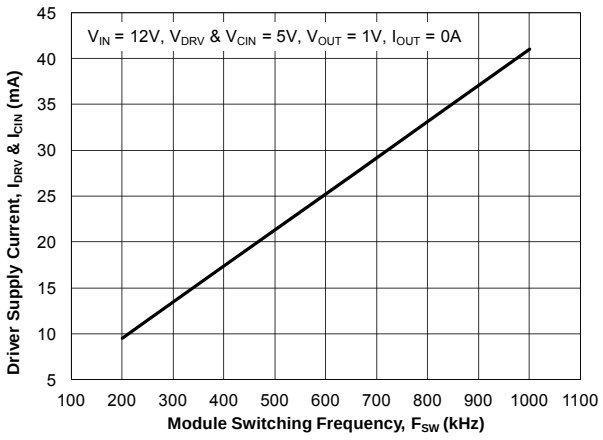


Figure 13. Driver Supply Current vs. Switching Frequency

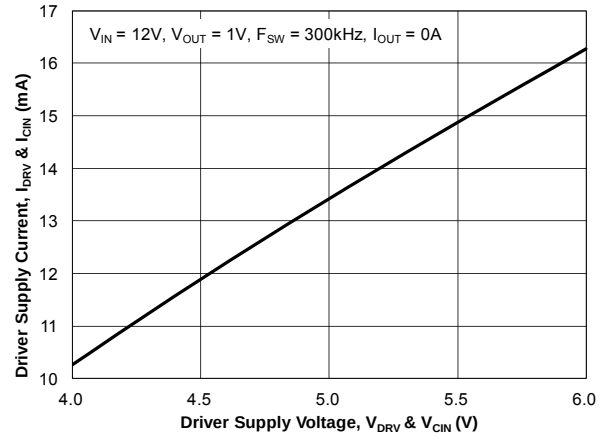


Figure 14. Driver Supply Current vs. Driver Supply Voltage

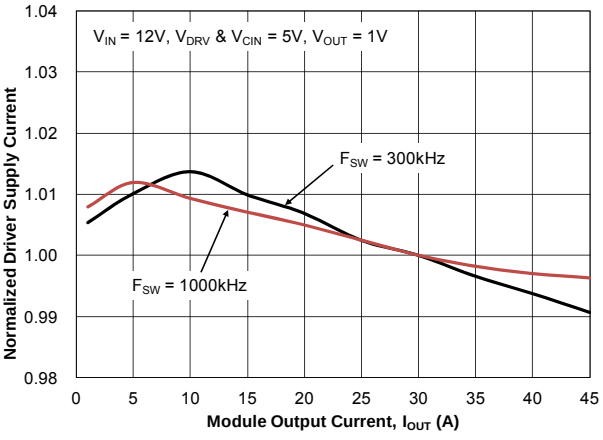


Figure 15. Driver Supply Current vs. Output Current

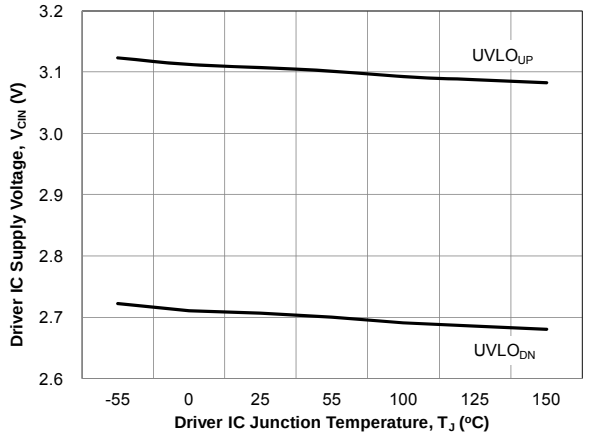


Figure 16. UVLO Threshold vs. Temperature

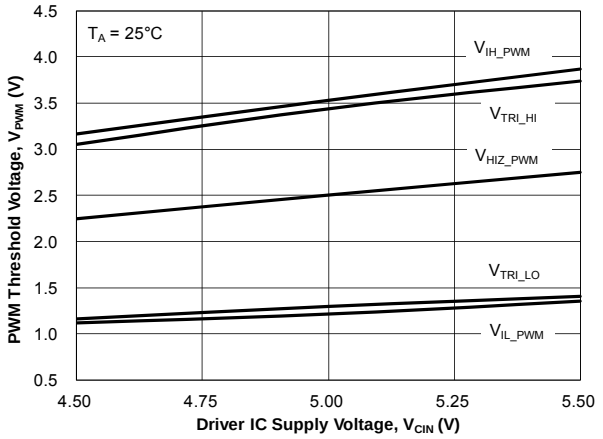


Figure 17. PWM Threshold vs. Driver Supply Voltage

Typical Performance Characteristics

Test Conditions: V_{CIN}=5 V, V_{DRV}=5 V, T_A=25°C, and natural convection cooling, unless otherwise specified.

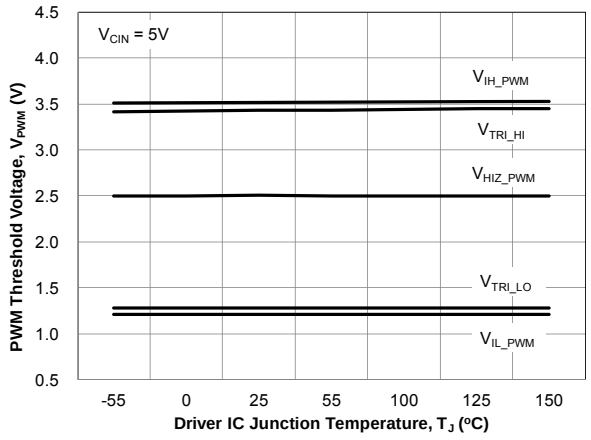


Figure 18. PWM Threshold vs. Temperature

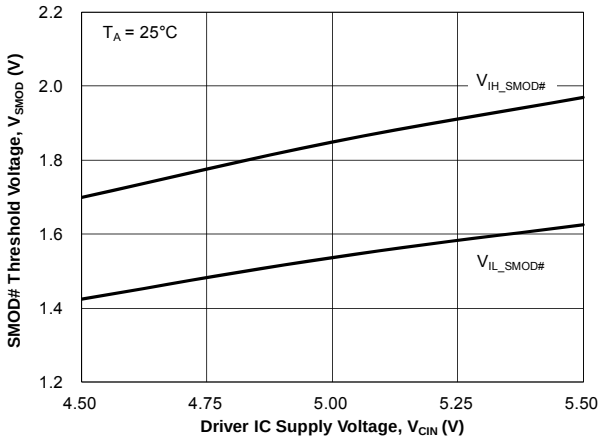


Figure 19. SMOD# Threshold vs. Driver Supply Voltage

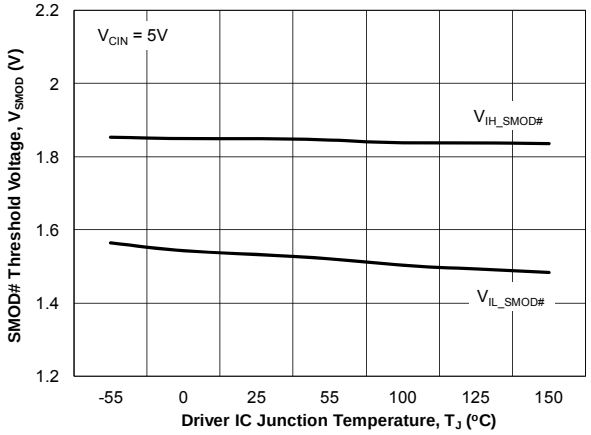


Figure 20. SMOD# Threshold vs. Temperature

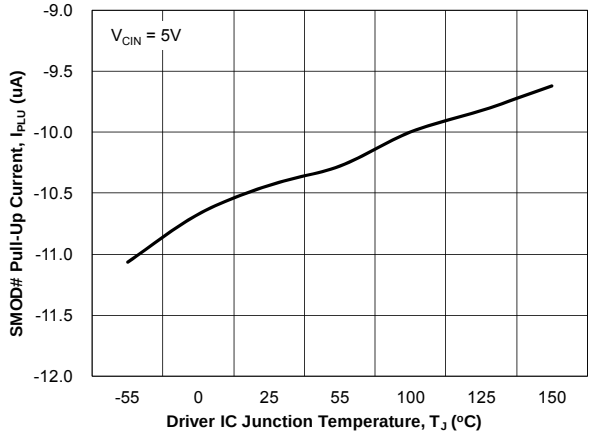


Figure 21. SMOD# Pull-Up Current vs. Temperature

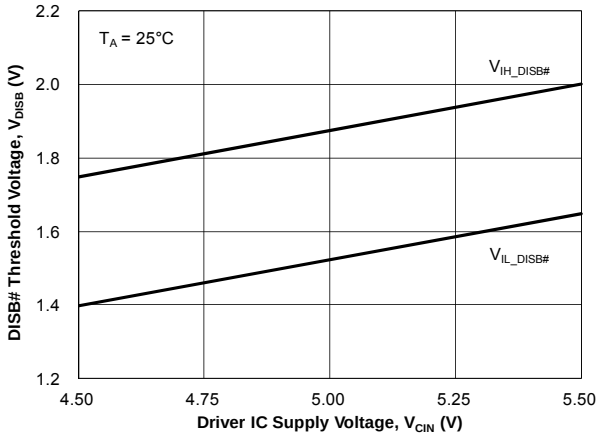


Figure 22. DISB# Threshold vs. Driver Supply Voltage

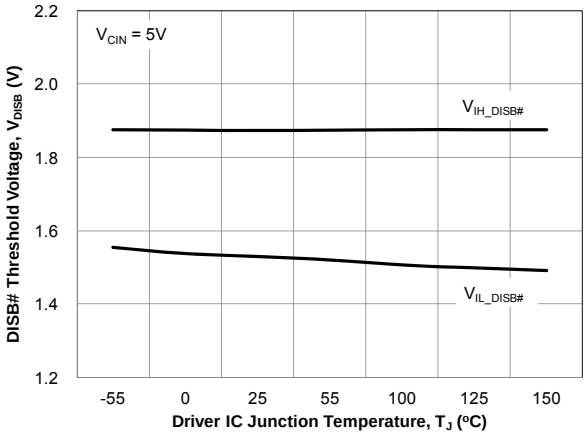


Figure 23. DISB# Threshold vs. Temperature

Typical Performance Characteristics

Test Conditions: V_{CIN}=5 V, V_{DRV}=5 V, T_A=25°C, and natural convection cooling, unless otherwise specified.

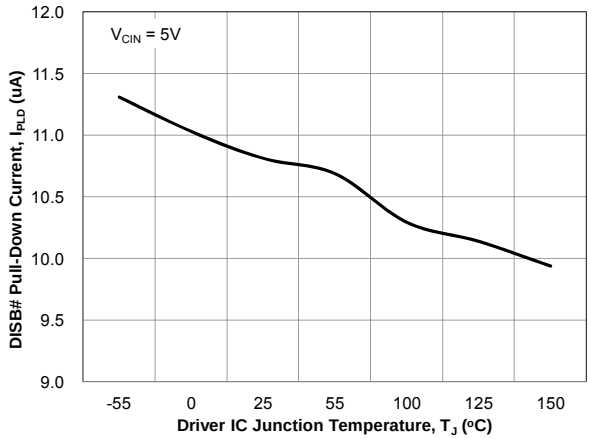


Figure 24. DISB# Pull-Down Current vs. Temperature

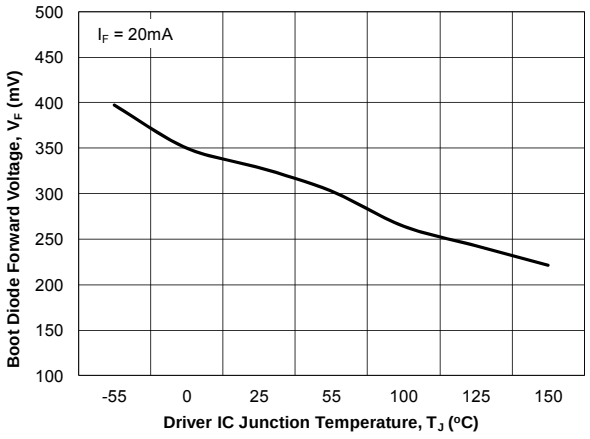


Figure 25. Boot Diode Forward Voltage vs. Temperature

Functional Description

The FDMF6823C is a driver-plus-FET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 1 MHz.

VCIN and Disable (DISB#)

The VCIN pin is monitored by an Under-Voltage Lockout (UVLO) circuit. When V_{CIN} rises above ~3.1 V, the driver is enabled. When V_{CIN} falls below ~2.7 V, the driver is disabled (GH, GL=0). The driver can also be disabled by pulling the DISB# pin LOW (DISB# < V_{IL_DISB}), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH (DISB# > V_{IH_DISB}).

Table 1. UVLO and Disable Logic

UVLO	DISB#	Driver State
0	X	Disabled (GH, GL=0)
1	0	Disabled (GH, GL=0)
1	1	Enabled (*see Table 2*)
1	Open	Disabled (GH, GL=0)

Note:
3. DISB# internal pull-down current source is 10 µA.

Thermal Warning Flag (THWN#)

The FDMF6823C provides a thermal warning flag (THWN#) to warn of over-temperature conditions. The thermal warning flag uses an open-drain output that pulls to CGND when the activation temperature (150°C) is reached. The THWN# output returns to a high-impedance state once the temperature falls to the reset temperature (135°C). For use, the THWN# output requires a pull-up resistor, which can be connected to VCIN. THWN# does NOT disable the DrMOS module.

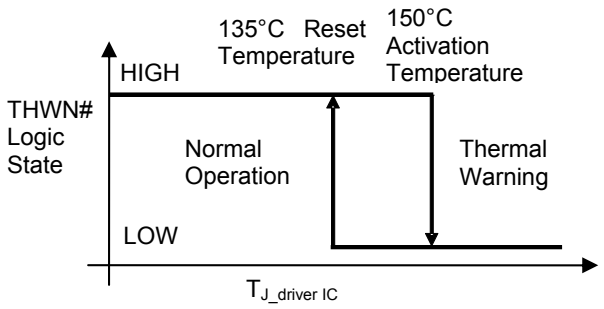


Figure 26. THWN Operation

Three-State PWM Input

The FDMF6823C incorporates a three-state 5 V PWM input gate drive design. The three-state gate drive has both logic HIGH level and LOW level, along with a three-state shutdown window. When the PWM input signal enters and remains within the three-state window for a defined hold-off time ($t_{D\_HOLD-OFF}$), both GL and GH are pulled LOW. This enables the gate drive to shut down both high-side and low-side MOSFETs to support features such as phase shedding, which is common on multi-phase voltage regulators.

Exiting Three-State Condition

When exiting a valid three-state condition, the FDMF6823C follows the PWM input command. If the PWM input goes from three-state to LOW, the low-side MOSFET is turned on. If the PWM input goes from three-state to HIGH, the high-side MOSFET is turned on. This is illustrated in Figure 27. The FDMF6823C design allows for short propagation delays when exiting the three-state window *(see Electrical Characteristics)*.

Low-Side Driver

The low-side driver (GL) is designed to drive a ground-referenced, low-$R_{DS(ON)}$, N-channel MOSFET. The bias for GL is internally connected between the VDRV and CGND pins. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled (DISB#=0 V), GL is held LOW.

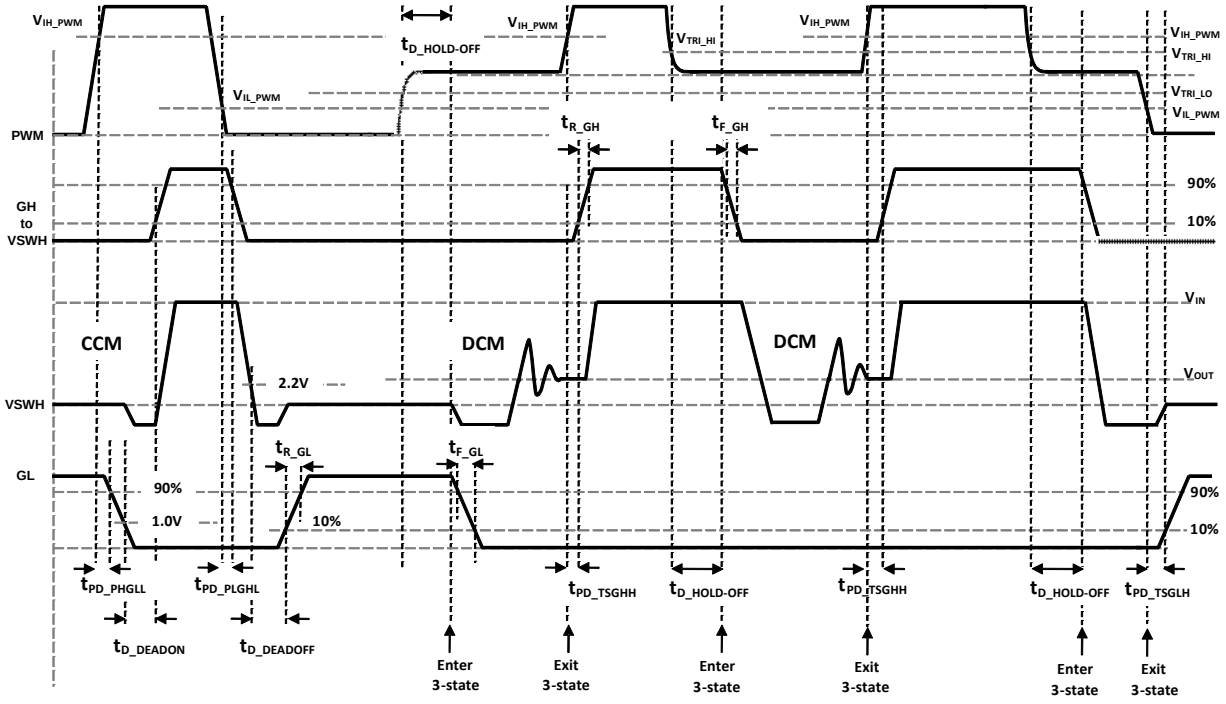
High-Side Driver

The high-side driver (GH) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit consisting of the internal Schottky diode and external bootstrap capacitor (C_{BOOT}). During startup, V_{SWH} is held at PGND, allowing C_{BOOT} to charge to V_{DRV} through the internal diode. When the PWM input goes HIGH, GH begins to charge the gate of the high-side MOSFET (Q1). During this transition, the charge is removed from C_{BOOT} and delivered to the gate of Q1. As Q1 turns on, V_{SWH} rises to V_{IN}, forcing the BOOT pin to V_{IN} + V_{BOOT}, which provides sufficient V_{GS} enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling GH to V_{SWH}. C_{BOOT} is then recharged to V_{DRV} when V_{SWH} falls to PGND. GH output is in-phase with the PWM input. The high-side gate is held LOW when the driver is disabled or the PWM signal is held within the three-state window for longer than the three-state hold-off time, $t_{D\_HOLD-OFF}$.

Adaptive Gate Drive Circuit

The driver IC advanced design ensures minimum MOSFET dead-time, while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive adaptively to ensure they do not conduct simultaneously. Figure 27 provides the relevant timing waveforms. To prevent overlap during the LOW-to-HIGH switching transition (Q2 off to Q1 on), the adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes HIGH, Q2 begins to turn off after a propagation delay (t_{PD_PHGLL}). Once the GL pin is discharged below 1.0 V, Q1 begins to turn on after adaptive delay t_{D_DEADON}.

To preclude overlap during the HIGH-to-LOW transition (Q1 off to Q2 on), the adaptive circuitry monitors the voltage at the GH-to-PHASE pin pair. When the PWM signal goes LOW, Q1 begins to turn off after a propagation delay (t_{PD_PLGHL}). Once the voltage across GH-to-PHASE falls below 2.2 V, Q2 begins to turn on after adaptive delay $t_{D\_DEADOFF}$.



Notes:

t_{PD_xxx} = propagation delay from external signal (PWM, SMOD#, etc.) to IC generated signal. Example (t_{PD_PHGLL} – PWM going HIGH to LS V_{GS} (GL) going LOW)

t_{D_xxx} = delay from IC generated signal to IC generated signal. Example (t_{D_DEADON} – LS V_{GS} (GL) LOW to HS V_{GS} (GH) HIGH)

PWM

t_{PD_PHGLL} = PWM rise to LS V_{GS} fall, V_{IH_PWM} to 90% LS V_{GS}

t_{PD_PLGHL} = PWM fall to HS V_{GS} fall, V_{IL_PWM} to 90% HS V_{GS}

t_{PD_PHGHH} = PWM rise to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS} (SMOD# held LOW)

SMOD#

t_{PD_SLGLL} = SMOD# fall to LS V_{GS} fall, V_{IL_SMOD} to 90% LS V_{GS}

t_{PD_SHGLH} = SMOD# rise to LS V_{GS} rise, V_{IH_SMOD} to 10% LS V_{GS}

Exiting 3-state

t_{PD_TSGHH} = PWM 3-state to HIGH to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS}

t_{PD_TSGLH} = PWM 3-state to LOW to LS V_{GS} rise, V_{IL_PWM} to 10% LS V_{GS}

Dead Times

t_{D_DEADON} = LS V_{GS} fall to HS V_{GS} rise, LS-comp trip value (~1.0V GL) to 10% HS V_{GS}

$t_{D\_DEADOFF}$ = VSWH fall to LS V_{GS} rise, SW-comp trip value (~2.2V VSWH) to 10% LS V_{GS}

Figure 27. PWM and 3-StateTiming Diagram

Skip Mode (SMOD#)

The Skip Mode function allows for higher converter efficiency when operated in light-load conditions. When SMOD# is pulled LOW, the low-side MOSFET gate signal is disabled (held LOW), preventing discharge of the output capacitors as the filter inductor current attempts reverse current flow – known as "Diode Emulation" Mode.

When the SMOD# pin is pulled HIGH, the synchronous buck converter works in Synchronous Mode. This mode allows for gating on the Low Side MOSFET. When the SMOD# pin is pulled LOW, the low-side MOSFET is gated off. If the SMOD# pin is connected to the PWM controller, the controller can actively enable or disable SMOD# when the controller detects light-load condition from output current sensing. Normally this pin is active LOW. *See Figure 28 for timing delays*.

Table 2. SMOD# Logic

DISB#	PWM	SMOD#	GH	GL
0	X	X	0	0
1	3-State	X	0	0
1	0	0	0	0
1	1	0	1	0
1	0	1	0	1
1	1	1	1	0

Note:

4. The SMOD# feature is intended to have a short propagation delay between the SMOD# signal and the low-side FET V_{GS} response time to control diode emulation on a cycle-by-cycle basis.

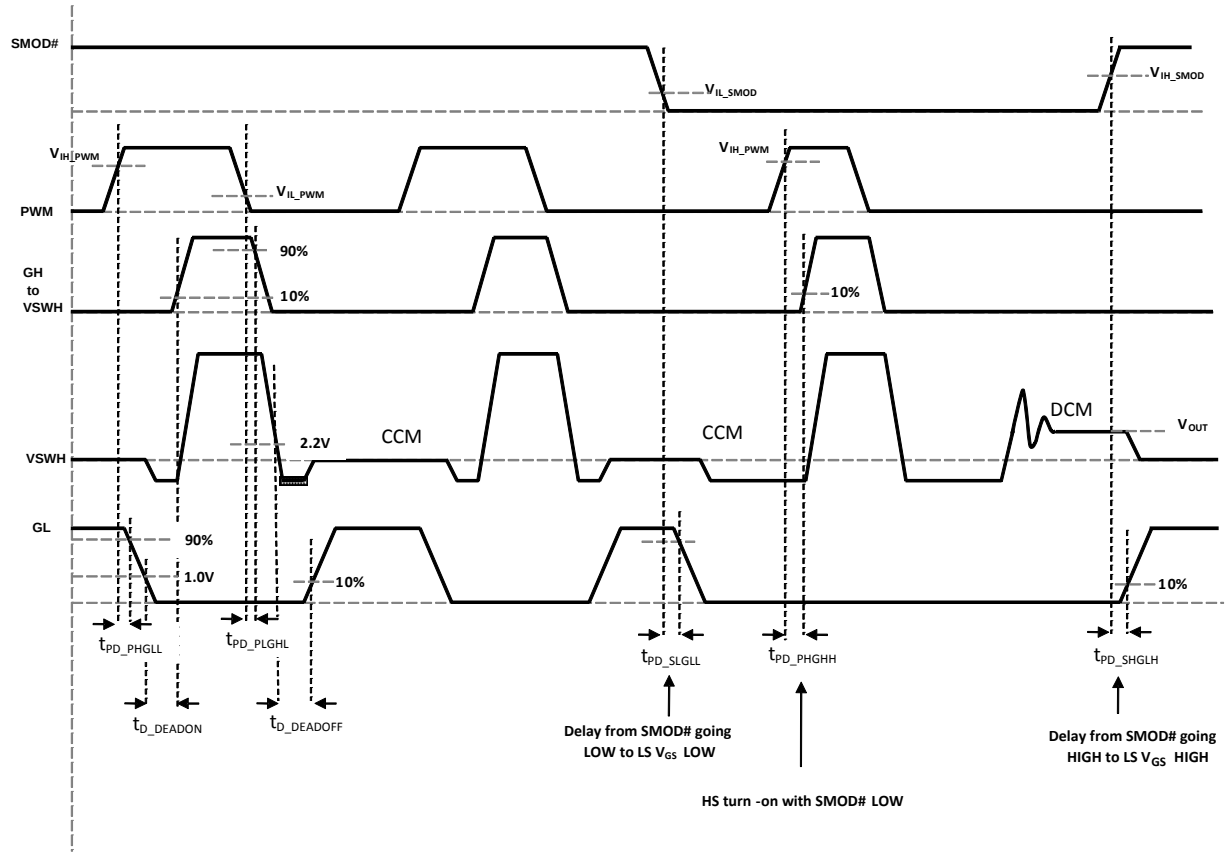


Figure 28. SMOD# Timing Diagram

Application Information

Supply Capacitor Selection

For the supply inputs (V_{CIN}), a local ceramic bypass capacitor is recommended to reduce noise and to supply the peak current. Use at least a 1 µF X7R or X5R capacitor. Keep this capacitor close to the VCIN pin and connect it to the GND plane with vias.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}), as shown in Figure 30. A bootstrap capacitance of 100 nF X7R or X5R capacitor is usually adequate. A series bootstrap resistor may be needed for specific applications to improve switching noise immunity. The boot resistor may be required when operating above 15 V_{IN} and is effective at controlling the high-side MOSFET turn-on slew rate and V_{SHW} overshoot. R_{BOOT} values from 0.5 to 3.0 Ω are typically effective in reducing VSWH overshoot.

VCIN Filter

The VDRV pin provides power to the gate drive of the high-side and low-side power MOSFET. In most cases, it can be connected directly to VCIN, the pin that provides power to the logic section of the driver. For additional noise immunity, an RC filter can be inserted between the VDRV and VCIN pins. Recommended values would be 10 Ω and 1 µF.

Power Loss and Efficiency

Measurement and Calculation

Refer to Figure 30 for power loss testing method.

Power loss calculations are:

$$P_{IN}=(V_{IN} \times I_{IN}) + (V_{5V} \times I_{5V}) \text{ (W)} \quad (1)$$

$$P_{SW}=V_{SW} \times I_{OUT} \text{ (W)} \quad (2)$$

$$P_{OUT}=V_{OUT} \times I_{OUT} \text{ (W)} \quad (3)$$

$$P_{LOSS\_MODULE}=P_{IN} - P_{SW} \text{ (W)} \quad (4)$$

$$P_{LOSS\_BOARD}=P_{IN} - P_{OUT} \text{ (W)} \quad (5)$$

$$EFF_{MODULE}=100 \times P_{SW}/P_{IN} \text{ (\%)} \quad (6)$$

$$EFF_{BOARD}=100 \times P_{OUT}/P_{IN} \text{ (\%)} \quad (7)$$

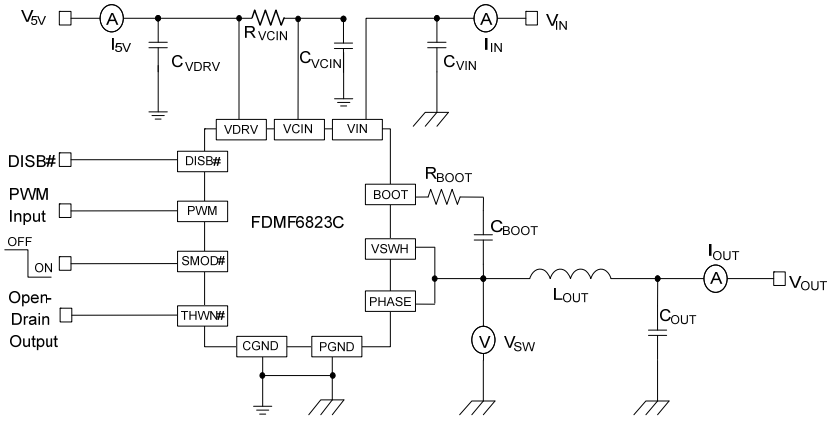


Figure 29. Block Diagram With V_{CIN} Filter

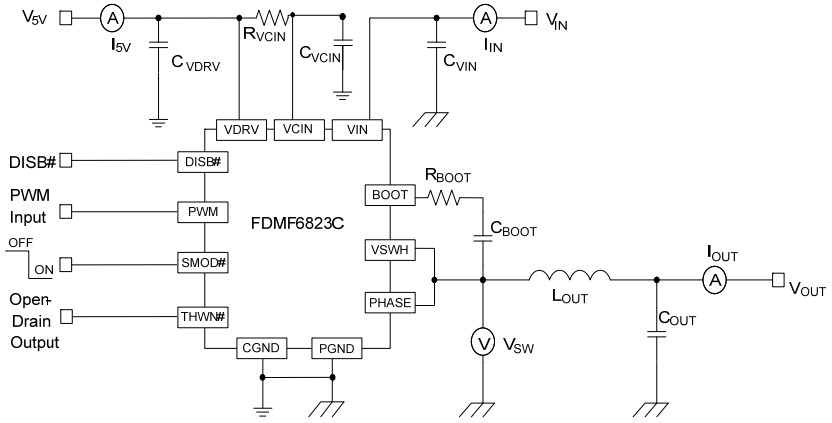


Figure 30. Power Loss Measurement

PCB Layout Guidelines

Figure 31 and Figure 32 provide an example of a proper layout for the FDMF6823C and critical components. All of the high-current paths, such as VIN, VSWH, VOUT, and GND copper, should be short and wide for low inductance and resistance. This aids in achieving a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

Recommendations for PCB Designers

1. Input ceramic bypass capacitors must be placed close to the VIN and PGND pins. This helps reduce the high-current power loop inductance and the input current ripple induced by the power MOSFET switching operation.
2. The V_{SWH} copper trace serves two purposes. In addition to being the high-frequency current path from the DrMOS package to the output inductor, it serves as a heat sink for the low-side MOSFET in the DrMOS package. The trace should be short and wide enough to present a low-impedance path for the high-frequency, high-current flow between the DrMOS and inductor. The short and wide trace minimizes electrical losses as well as the DrMOS temperature rise. Note that the V_{SWH} node is a high-voltage and high-frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. Since this copper trace acts as a heat sink for the lower MOSFET, balance using the largest area possible to improve DrMOS cooling while maintaining acceptable noise emission.
3. An output inductor should be located close to the FDMF6823C to minimize the power loss due to the V_{SWH} copper trace. Care should also be taken so the inductor dissipation does not heat the DrMOS.
4. PowerTrench® MOSFETs are used in the output stage and are effective at minimizing ringing due to fast switching. In most cases, no VSWH snubber is required. If a snubber is used, it should be placed close to the VSWH and PGND pins. The selected resistor and capacitor need to be the proper size for power dissipation.
5. VCIN, VDRV, and BOOT capacitors should be placed as close as possible to the VCIN-to-CGND, VDRV-to-CGND, and BOOT-to-PHASE pin pairs to ensure clean and stable power. Routing width and length should be considered as well.
6. Include a trace from the PHASE pin to the VSWH pin to improve noise margin. Keep this trace as short as possible.
7. The layout should include the option to insert a small-value series boot resistor between the boot capacitor and BOOT pin. The boot-loop size, including R_{BOOT} and C_{BOOT}, should be as small as possible. The boot resistor may be required when operating above 15 V_{IN} and is effective at controlling the high-side MOSFET turn-on slew rate and V_{SHW} overshoot. R_{BOOT} can improve noise operating margin in synchronous buck designs that may have noise issues due to ground bounce or high positive and negative V_{SWH} ringing. Inserting a boot resistance lowers the DrMOS efficiency. Efficiency versus noise trade-offs must be considered. R_{BOOT} values from 0.5 Ω to 3.0 Ω are typically effective in reducing V_{SWH} overshoot.
8. The VIN and PGND pins handle large current transients with frequency components greater than 100 MHz. If possible, these pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is discouraged since this adds inductance to the power path. This added inductance in series with either the VIN or PGND pin degrades system noise immunity by increasing positive and negative V_{SWH} ringing.
9. GND pad and PGND pins should be connected to the GND copper plane with multiple vias for stable grounding. Poor grounding can create a noise transient offset voltage level between CGND and PGND. This could lead to faulty operation of the gate driver and MOSFETs.
10. Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add an additional BOOT to the PGND capacitor. This may lead to excess current flow through the BOOT diode.
11. The SMOD# and DISB# pins have weak internal pull-up and pull-down current sources, respectively. These pins should not have any noise filter capacitors. Do not to float these pins unless absolutely necessary.
12. Use multiple vias on the VIN and VOUT copper areas to interconnect top, inner, and bottom layers to distribute current flow and heat conduction. Do not put many vias on the VSWH copper to avoid extra parasitic inductance and noise on the switching waveform. As long as efficiency and thermal performance are acceptable, place only one VSWH copper on the top layer and use no vias on the VSWH copper to minimize switch node parasitic noise. Vias should be relatively large and of reasonably low inductance. Critical high-frequency components, such as R_{BOOT}, C_{BOOT}, RC snubber, and bypass capacitors; should be located as close to the respective DrMOS module pins as possible on the top layer of the PCB. If this is not feasible, they can be connected from the backside through a network of low-inductance vias.

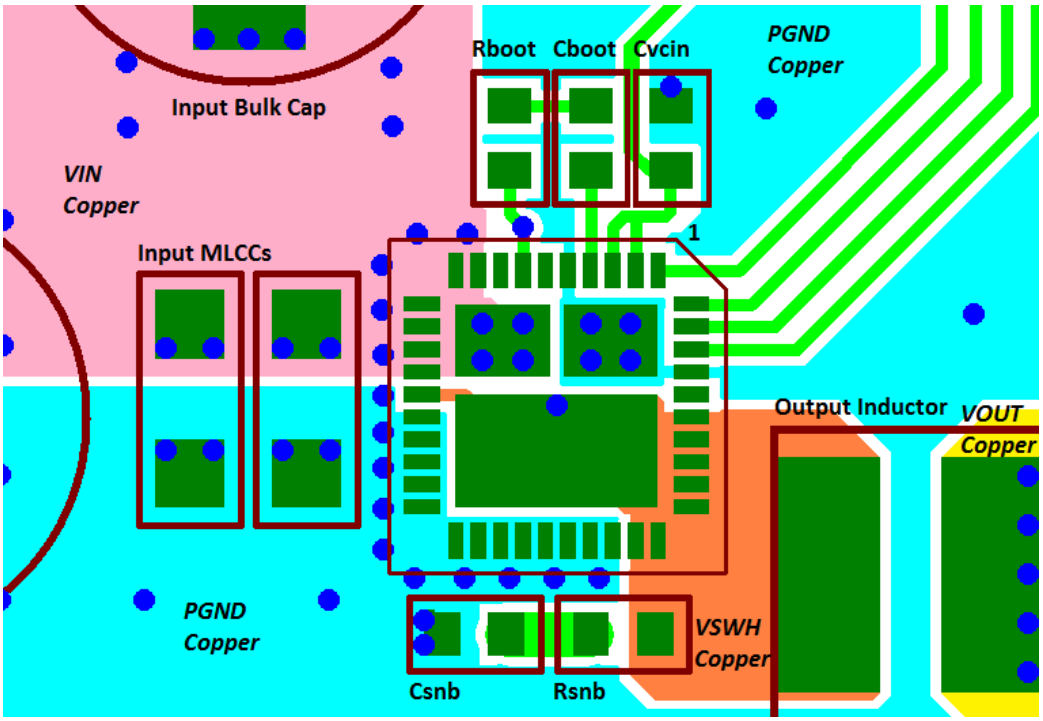


Figure 31. PCB Layout Example (Top View)

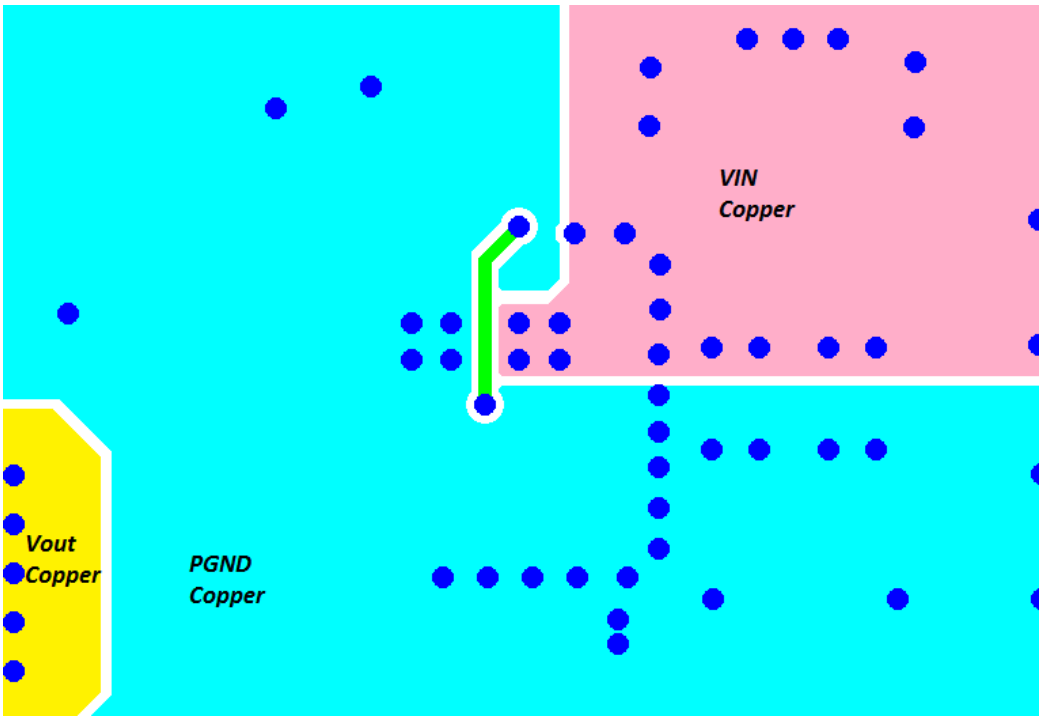


Figure 32. PCB Layout Example (Bottom View)

Physical Dimensions

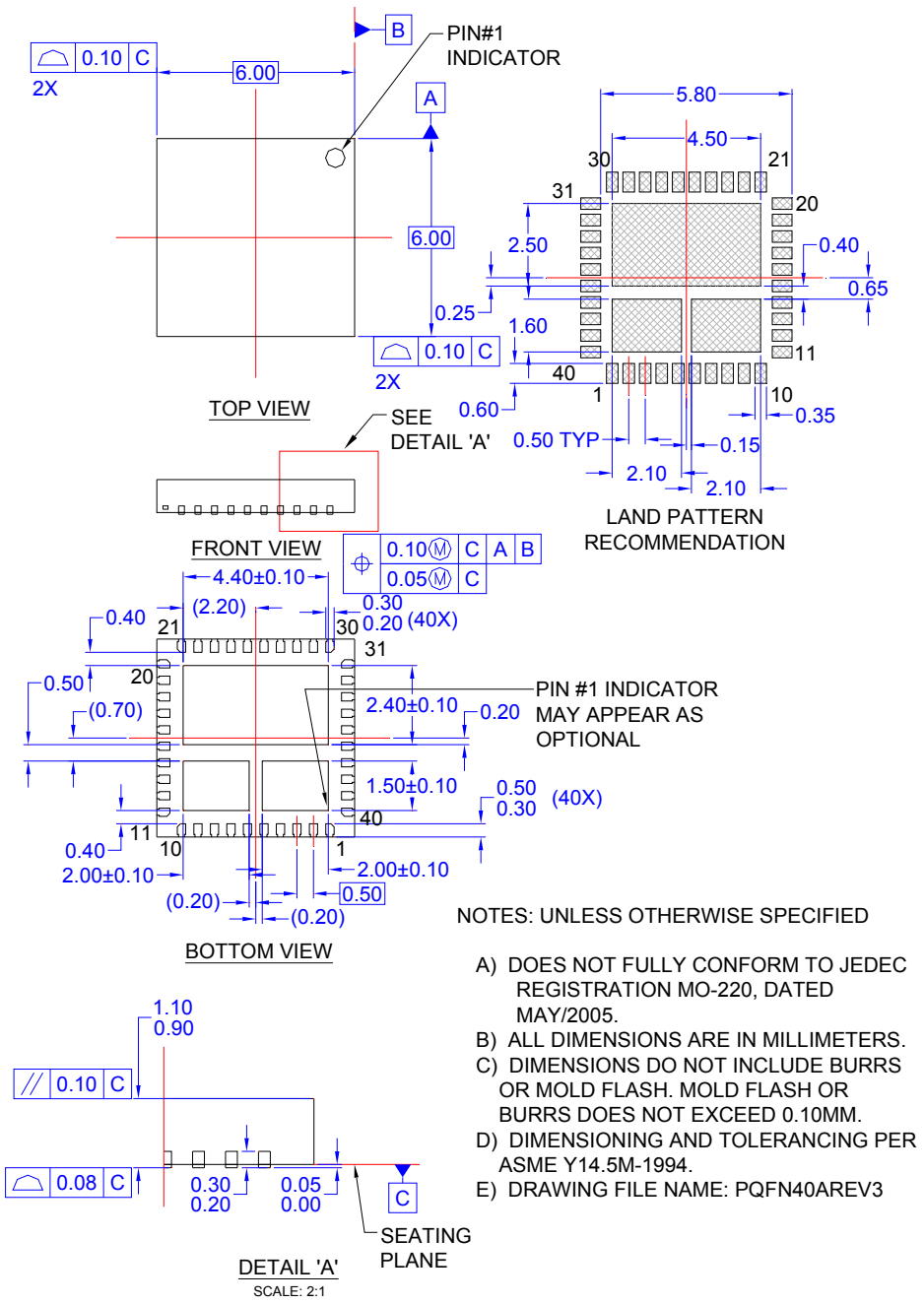


Figure 33. 40-Lead, Clipbond PQFN DrMOS, 6.0x6.0 mm Package

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

2Cool™
AccuPower™
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
mWSaver™
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
µSerDes™
SerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

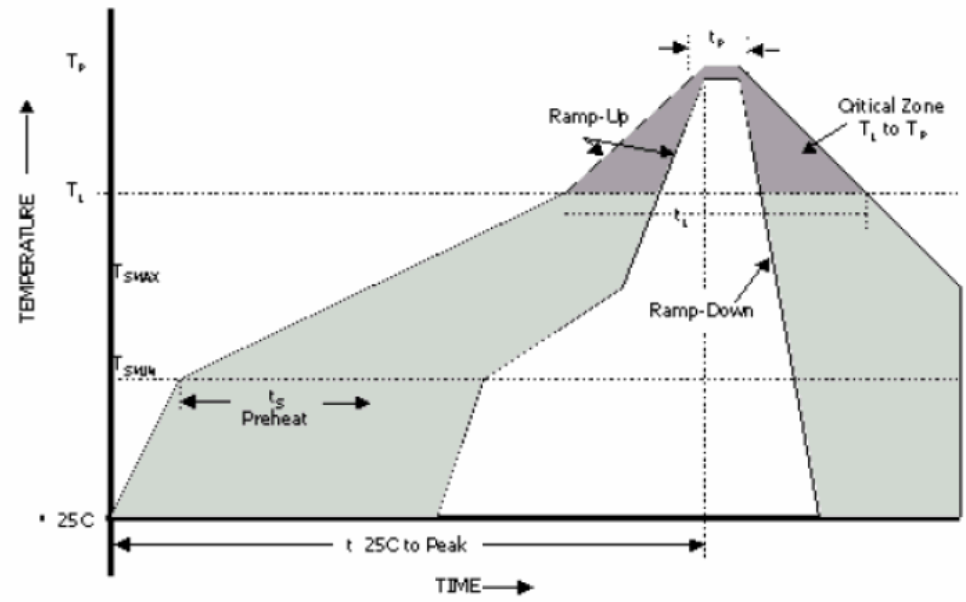
PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I64

Preconditioning Profile



Reflow Condition

Reflow Condition	Large Pkg	Small Pkg
Average Ramp-Up Rate (T_L to Peak)	3C/sec max.	3C/sec max.
Preheat		
	150C	150C
	200C	200C
Tsmax to TL	60 - 180 sec	60 - 180 sec
Time maintained above:	3C/sec max.	3C/sec max.
	217C	217C
	60 - 150 sec	60 - 150 sec
Peak Temperature (T_p)	245 +0/-5C	260 +0/-5C
Time within 5C of actual Peak Temperature (t_p)	10 - 30 sec	20 - 40 sec
Ramp-down Rate	6C/sec max.	6C/sec max.
Time 25C to Peak Temperature	8 minutes max.	8 minutes max.

Marking

Product Number	Line 1	Line 2	Line 3	Line 4	Line
FDMF6823C	**$Y**(Logo) **&Z**(Assembly Plant) **&3**(Date Code) **&K**(Lot Run)	FDMF	6823C		

Top Mark Convention - Date Code Type

Date Code Type indicates which weekly schema to use for Date Code

Value	Description
S1	Weekly schema
S2	Bi-weekly schema
S6	Six-week schema
S8	Eight-week schema

Back to Top Mark Search tool

Line 1: F →Logo

D → assembly plant

D41→ date code

AN → lot run

Line 2: FDMF

Line 3: 6823C

Top Mark Convention Symbol List

(please click on each symbol to see more details)

Symbol	Format	Description
$Y	FS or	Fairchild Semiconductor (FSC) logo graphic
&Z	Z	Designates the Assembly plant code
&4	XXYY	4-Digit Date code format
&3	XYY	3-Digit Date code format
&2	XY	2-Digit Date code format
&G	YY	Weekly Date code format
&T	TT	Die Run Traceability Code
&W	----	Six-Week Binary Datecoding Scheme
&V	---	Eight-Week Binary Datecoding Scheme
&Y	----	Binary Calendar Year Coding Scheme
&C	T	Single digit Die Run Code (last digit of the two digit code)
&U	U	Wafer Fab Code
&E		Designates Space
&.	.	Pin one dot (For SC70, SOT23, MLP binary marking type and WLCSP)
&H	Lot Number	Last 3 digit of workstream lot number
&O		Plant Code identifier on Tiny Logic Package
&K	KK	2-Digits Lot Run Traceability Code

Top Mark Convention - Assembly Plant Code

Table 1: (For most Fairchild products)

A = China (Subcontractor)
B = Bangkok, Thailand (Subcontractor)
C = Singapore (Subcontractor)
D = Cebu, Philippines
E = Korea (Subcontractor)
H = Philippines (Subcontractor)
J = Japan (Subcontractor)
K = Korea
L = Salt Lake City, UT
M = Malacca, Malaysia (Subcontractor)
N = (ChipPAC, Subcontractor)
P = Penang, Malaysia
S = Singapore (NSSG, Subcontractor)
T = Taiwan (Subcontractor)
V = Malaysia (Carsem, Subcontractor)
X = USA (Subcontractor)
Y = Malaysia (Unisem, Subcontractor)
Z = South Portland, ME
1 = FAIRCHILD SUZHOU, China

Table 2: (Fairchild Korea products)

Note: There are about 3,700 Fairchild Korea products with a different set of assembly plant values.
Please enter a product number in the search form. Then click on the "(*Assembly Plant*)" text link. If it is a Fairchild Korea product, you will be led to this table.
Fairchild Korea manufactures Small Signal Transistor, High-voltage MOSFET, JFET, IGBT, Diode, SPM, Motor IC, General Purpose Standard Linear, PWM, Standard & Green FPS, Reference, Regulator, TRIAC, LDO & VREF.

A = FINE, Korea
A = ASE, Korea
B = SP Semi(SPS), Korea
B = Hana Semiconductor, Thailand
C = JCET, China
D = Fairchild Cebu, Philippines
E = Nantong, Fujitsu
F = KEC, Korea
G = SHEDCL, China
H = SUNGJIN, Korea
K = AUK Dalian, China
M = ENOCH, Korea
N = STS, Korea
P = Fairchild Penang, Malaysia
R = CHIPPAC SHANGHAI, China
S = SIGNETICS, Korea
T = AUK, Korea
U = HMC, Korea
U = UNISEM V = SZEC, China
W = AHG
X = PSTS(STS China plant), China
Y = AHG, Weihai, China
Z = Team Pacific, Philippines
1 = FAIRCHILD SUZHOU, China

Top Mark Convention - 3-Digit Date Code

Contents

Summary

Symbol	Format	Description	Applicable Packages
&3	XYY	3-digit date code X stands for calendar year YY stands for workweek	TSSOP-8L MOSFET BGA SOT-223 SSOT-8 TO-218 (DPP) TO-220 TO-247 TO-247ST (DPP) TO-251/252 TO-263/262 TO-268 (DPP) SSOT-227/ISOTOP SOIC-8 (DPP) TO-92/226/237

Table 1: Numeric Calendar Year Coding Scheme

Calendar Year	Non-Lead Free Products	Lead Free Products
2007	7YY	HYY
2008	8YY	JYY
2009	9YY	KYY
2010	0YY	AYY
2011	1YY	BYY
2012	2YY	CYY
2013	3YY	DYY
2014	4YY	EYY
2015	5YY	FYY
2016	6YY	GYY
2017	7YY	HYY
2018	8YY	JYY
2019	9YY	KYY

Note: The marking of the calendar year will repeat after the cycle of ten (10) years.
YY stands for workweek code.

Table 2: Six weeks numeric date code scheme
Date Code Type is "S6" for this scheme.

Workweek No.	Value
Workweek 06-11	X06
Workweek 12-17	X12
Workweek 18-23	X18
Workweek 24-29	X24
Workweek 30-35	X30
Workweek 36-41	X36
Workweek 42-47	X42
Workweek 48-51	X48
Workweek 52-05	X52

Table 3: Two weeks numeric date code scheme
Date Code Type is "S2" for this scheme.

Work Week No.	Value
Workweek 1,2	X01
Workweek 3,4	X03
Workweek 5,6	X05
(continues for the rest of the workweeks)	
Workweek 49,50	X49
Workweek 51,52	X51
Workweek 53	X53

Table 4: Weekly numeric date code scheme
Date Code Type is "S1" for this scheme.

Work Week No.	Value
Workweek 01	X01
Workweek 02	X02
Workweek 03	X03
(continues for the rest of the workweeks)	
Workweek 51	X51
Workweek 52	X52
Workweek 53	X53

Back to top

Back to Top Mark Search tool

料號說明: FDMF→ package → Power 66

6823C → P/N → Extra-Small, High-Performance, High-Frequency DrMOS Module

FAIRCHILD SEMICONDUCTOR®

Certificate of Compliance

DUNS		Document Date	URL for Additional Information
00-489-5751		Fri, Sep 13, 2013 06:03 PM	Fairchildsemi.com
Contact	**Title**	**Phone**	**Email**
David Lancaster	**Product Ecology Manager**	801.562.7455	david.lancaster@fairchildsemi.com

Material Declaration Processing Information

FSID	Material Declaration	Site Owner	Assembly Location	Package Weight(g)	MSL Rating
FDMF6823C	Power-66	CEBU	INTERNAL CEBU	0.1343122	1
Terminal Finish	**Base Alloy**	**Green Status**	**Reflow Cycles**	**Max Time at Temp**	**Peak Temp**
Matte Tin (Sn)	CU Alloy	This product is green as defined by Fairchild's Green Policy. Please use this link to access Fairchild's Green Product Definition. Fairchild's Green Policy	3	30	260

Homogenous Material Composition Declaration

Component	Material	Weight of Component(mg)	Substance	Weight (mg)	CAS	PPM in FSID
Chip	Other inorganic materials	0.0961	Silicon	0.0961	7440-21-3	715
Die Attach	Other Nonferrous metals & alloys	5.1000	Silver	0.1275	7440-22-4	949
			Tin	0.2550	7440-31-5	1899
			Lead	4.7175	7439-92-1	35123
Encapsulation	Thermoplastics	63.2160	Carbon Black	0.3160	1333-86-4	2353
			Phenol resin	2.2100	9003-35-4	16454
			Epoxy Resin	3.7900	29690-82-2	28218
			Silica, vitreous	56.9000	60676-86-0	423640
Lead Frame	Copper & its alloys	44.2001	Zinc	0.0486	7440-66-6	362
			Silver	0.0535	7440-22-4	398
			Iron	0.9980	7439-89-6	7430
			Copper	43.1000	7440-50-8	320894
Lead Frame Clip		19.6000	Copper	19.6000	7440-50-8	145929
Terminal Finish	Other Nonferrous metals & alloys	2.0000	Tin	2.0000	7440-31-5	14891
Wire Bond	Precious metals	0.1000	Gold	0.1000	7440-57-5	745

Note: The substance content disclosed herewith is approximate and is based on various methods including, engineering calculations, supplier surveys, Material Safety Data Sheets, analytical measurements. Fairchild may update this document without notification.

Additionally, the following should be noted:

- This statement may not include information regarding the miniscule quantities of dopant and metal materials in the electrical devices contained within the finished product.
- CAS numbers listed for Resin substances are generic and may contain alternate substances of similar composition.

RoHS Declaration

The European Parliament and of the Council on the Restriction of the use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive restricts the concentration of Lead (Pb), Mercury (Hg), Hexavalent Chromium (Cr6+), Polybrominated Biphenyls (PBB), Polybrominated Diphenyl Ethers (PBDE) to 0.1% (1000 PPM) and restricts the concentration of Cadmium (Cd) to 0.01% (100 PPM) in homogeneous materials of electronic products.

The FSC part number listed above and the homogenous materials in the product are compliant with the Directive 2011/65/EU.

Exemptions as declared for the directive are: 7(a)-Lead in high melting temperature type solders (i.e. lead based solder alloys containing 85 % by weight or more lead).

China RoHS

With the possible exception of lead, if applicable (refer to the RoHS Declaration statement above), this product and all homogeneous materials in the product comply with the China RoHS standard SJ/T 11363-2006.

REACH Compliance

European Union Regulation (EC) No 1907/2006 concerning the Registration, Evaluation, Authorization, and Restriction of Chemicals (REACH) entered into force on June 1, 2007. Fairchild Semiconductor agrees with the purpose of REACH, which is to ensure a high level of protection of human health and the environment. Fairchild semiconductor is compliant with all applicable requirements of REACH and upon request will provide information regarding the chemical composition of our products.

Fairchild Semiconductor is neither a manufacturer nor importer of preparations into Europe and therefore the registration requirements of REACH do not apply to us. It is expected that any electronic materials manufacturer that uses preparations from Europe in their products will ensure compliance with REACH registration requirements.

Product (articles) manufacturers or importers into Europe are obligated under Article 33 of REACH to inform recipients of any articles that contain chemicals on the Substances of Very High Concern (SVHC) candidate list above a 0.1% concentration (by weight per article). Products manufactured and marketed by Fairchild Semiconductor do not contain substances on the REACH SVHC candidate list (as published by the ECHA on the following publication dates) in concentrations greater than 0.1% by weight per article:

October 28, 2008; January 13; 2010, March 30, 2010; June 18, 2010; December 15, 2010; June 20, 2011; December 19, 2011; June 18, 2012*; December 19, 2012; June 20, 2013.

Fairchild Semiconductor will continue to monitor the developments of REACH and is committed to meeting our responsibilities as an environmentally-responsible company. Please refer to the web site below for additional information regarding SVHC:
ECHA European Chemical Agency

* Diboron trioxide was added to REACH Annex XIV as a Substance of Very High Concern(SVHC) on June 18, 2012. Fairchild products in glass encapsulated packages may list Diboron trioxide as a constituent material in the glass encapsulation, in a concentration greater than 0.1%; REACH classifies; glass as a substance of unknown or variable composition, complex reaction products or biological matter (UVCB) containing the elements silica, calcium, sodium, potassium, magnesium and other cautions bonded together with oxygen. In glass, these elements are bonded into a non crystalline molecular structure with completely different properties than the starting material; Therefore Diboron trioxide is not present in the finished Fairchild product and does not require notification of the presents of a SVHC.

Joint Industry Guide (JIG) 101

With the exception of RoHS exemptions listed above (if applicable), this product does not contain any restricted substances listed in the Joint Industry Guide (JIG) 101 in concentrations greater than the threshold listed. The list of JIG substances may be viewed using this web link.

Joint Industry Guide (JIG) 101

The signature below is of the Company's designated personnel with delegated product ecology compliance responsibility and verifies that to the best of our knowledge the statements above are valid and accurate.

David Lancaster

Product Ecology Manager
Fairchild Semiconductor
3333 W 9000 S
West Jordan, UT 84088
Tel 1-801-562-7455
Email: david.lancaster@fairchildsemi.com

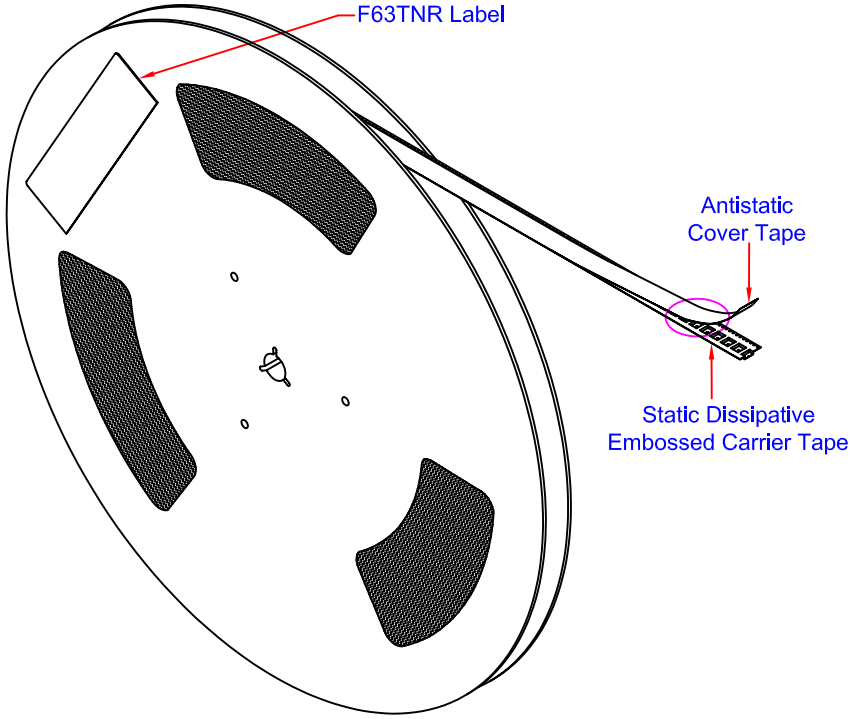
FAIRCHILD
SEMICONDUCTOR®

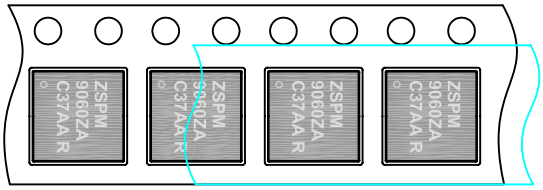
Environmental Declaration

The content of this document is based upon information collected from Fairchild Semiconductor's supply chain, manufacturing facilities and affiliates worldwide. Providing for limitations below, Fairchild Semiconductor certifies that the information provided in this document is correct as of the date indicated on this page.

Fairchild has implemented systems to ensure our products are compliant to environmental regulations and laws worldwide. However, not all materials in Fairchild's products may have been independently verified regarding substance content. In the event of any issues arising from information in this document, the warranty section of Fairchild's standard terms and conditions of sale shall apply, unless alternate contracts have been agreed upon in writing by both parties.

PQFN-40L-DrMOS_ZM01 Packing Configuration: Figure 1.0





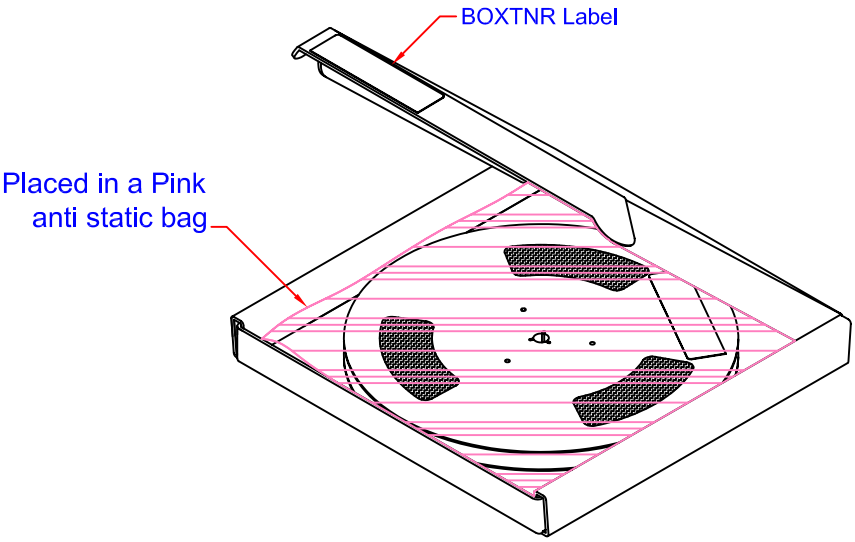
PQFN-40L-DrMOS_ZM01 Unit Orientation

Packing Description:

PQFN-40L-DrMOS_ZM01 parts are shipped in tape. The carrier tape is made from a conductive / dissipative (carbon filled) polycarbonate resin or polystyrene. The cover tape is a multilayer film HAA (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 13" or 330mm diameter reel. The reels are dark blue or black in color and is made of polystyrene plastic (anti-static coated).

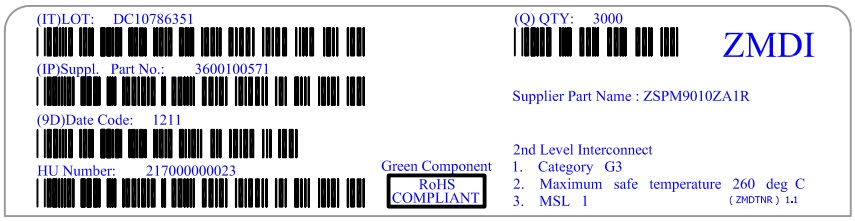
These full reels are individually barcode labeled, and placed in a pink anti static bag inside a box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One pizza box contains one reel maximum. And this box is placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

PQFN-40L-DrMOS_ZM01 Packing information	
Packing Option	Standard (no flow code)
Packing type	TNR
Qty per Reel/Tube/Bag	3000
Reel Size	13" Dia
Box Dimension (mm)	INTR0004
Max qty per Box	3,000

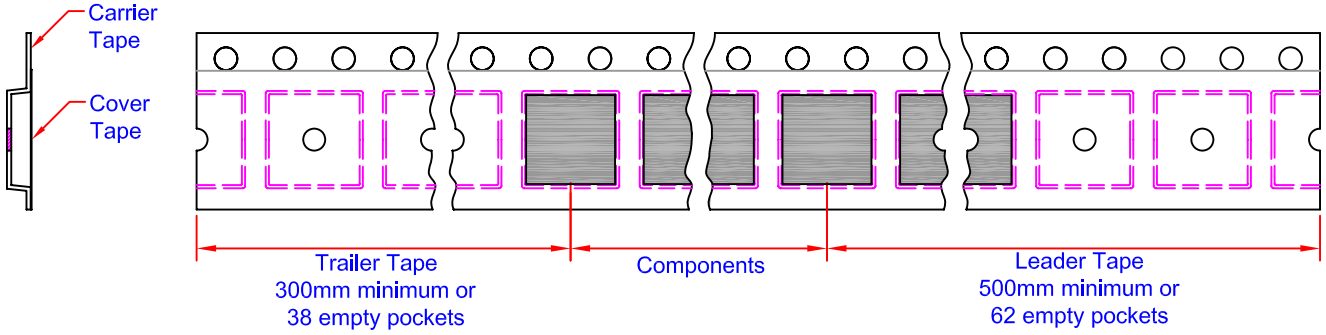


No FSC label and information
(INTR0004)

Barcode Label Sample



PQFN-40L-DrMOS_ZM01 Tape Leader and Trailer Configuration: Figure 2.0

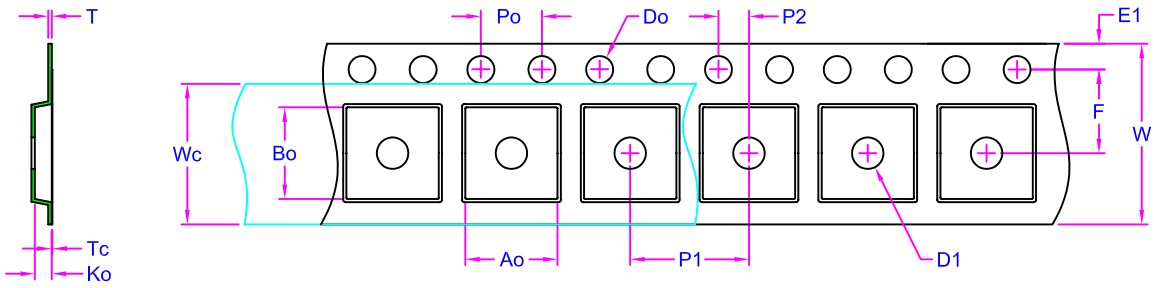


NOTES:

A. ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

B. DRAWING FILE NAME: PKG-PQFN40A_ZM01REV1

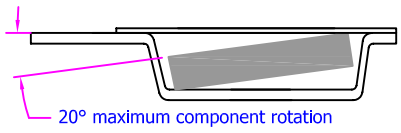
PQFN-40L-DrMOS_ZM01 Embossed Carrier Tape Configuration: Figure 3.0



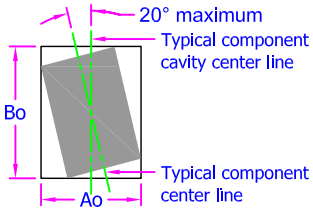
User Direction of Feed

Dimensions are in millimeters														
Pkg type	Ao	Bo	W	Do	D1	E1	F	P1	P2	Po	Ko	T	Wc	Tc
PQFN-40L-DrMOS_ZM01 (12mm)	6.30 ±0.10	6.30 ±0.10	12.00 +0.20 -0.10	1.50 +0.10 -0.00	1.50 +0.25 -0.00	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	2.00 ±0.05	4.00 ±0.10	1.30 ±0.10	0.30 ±0.05	9.20 ±0.10	0.05 ±0.01

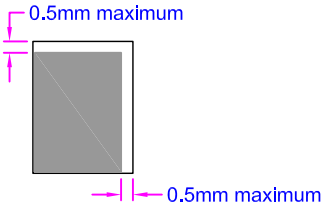
Notes: Ao, Bo, and Ko dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C). Camber requirement is also compliant to above mentioned standards.



Sketch A (Side or Front Sectional View)
Component Rotation

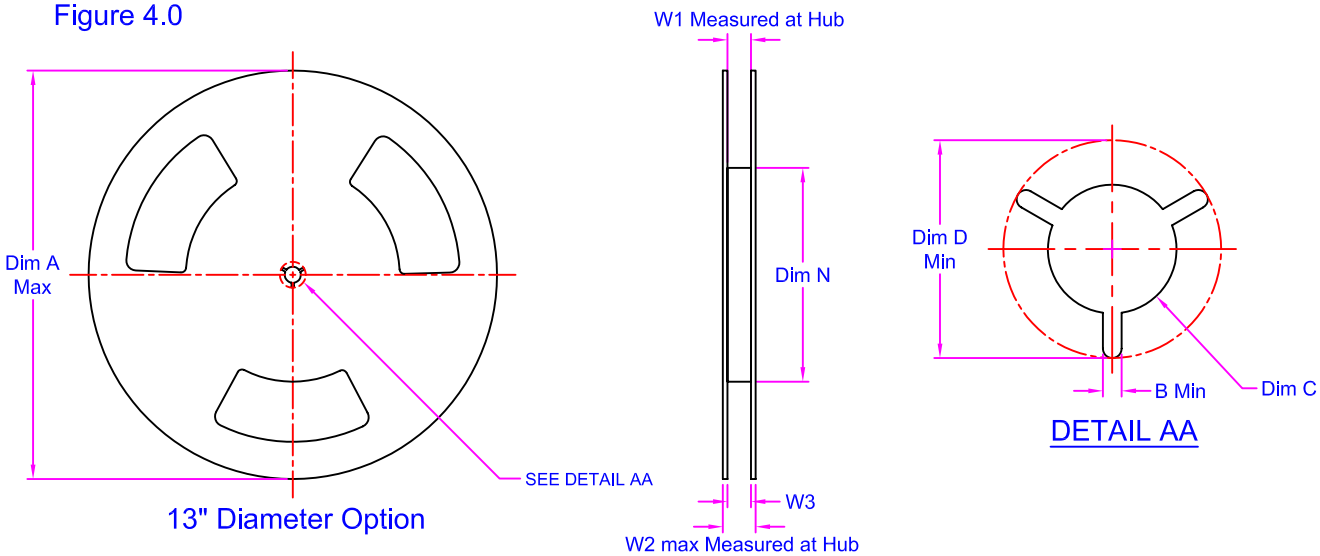


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

PQFN-40L-DrMOS_ZM01 Reel Configuration: Figure 4.0



13" Diameter Option

DETAIL AA

Dimensions are in millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	13" Dia	330	1.5	13+0.5/-0.2	20.2	178	12.4+2/-0	18.4	11.9-15.4

NOTES:

A. ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED
B. DRAWING FILE NAME: PKG-PQFN40A_ZM01REV1
C. PLASTIC REEL W1 DIMENSION CONTROL LIMIT OF;
8MM REEL = ±1.0MM AND 12MM REEL AND ABOVE = ±1.5MM