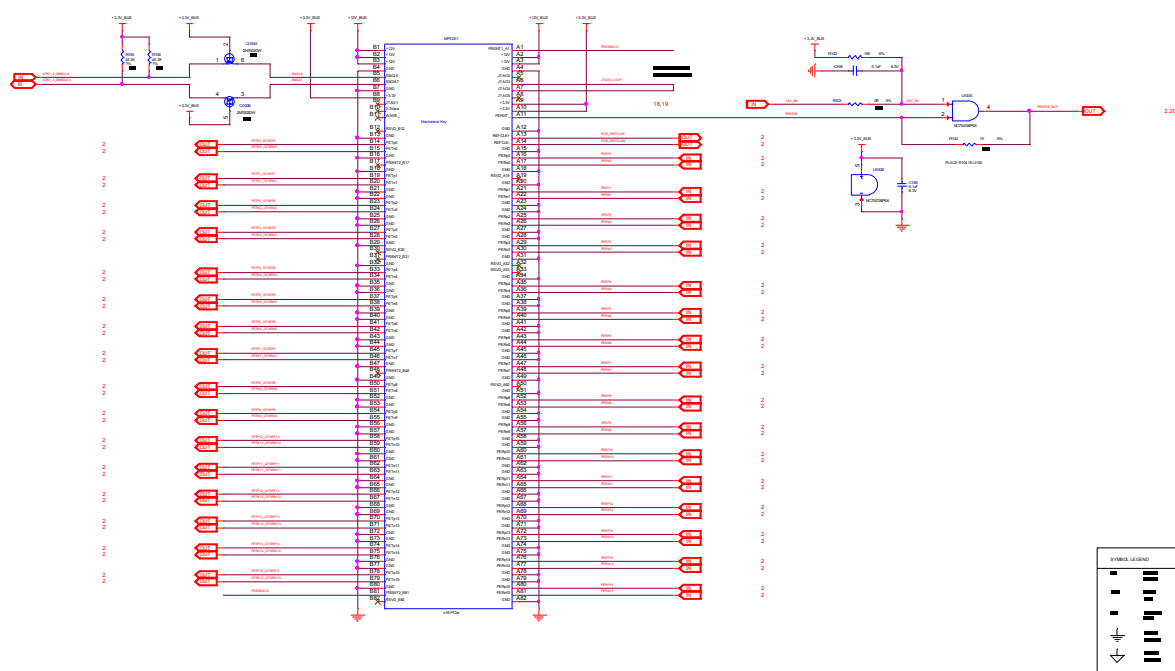
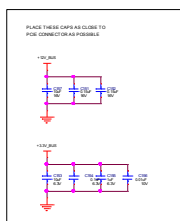










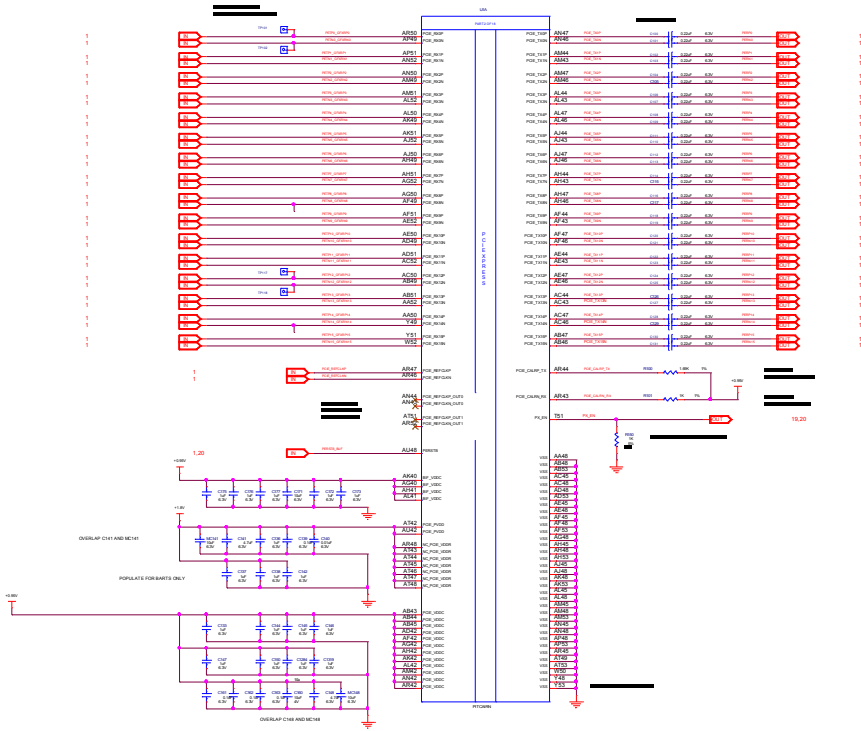


(1) PCI-EXPRESS EDGE CONNECTOR

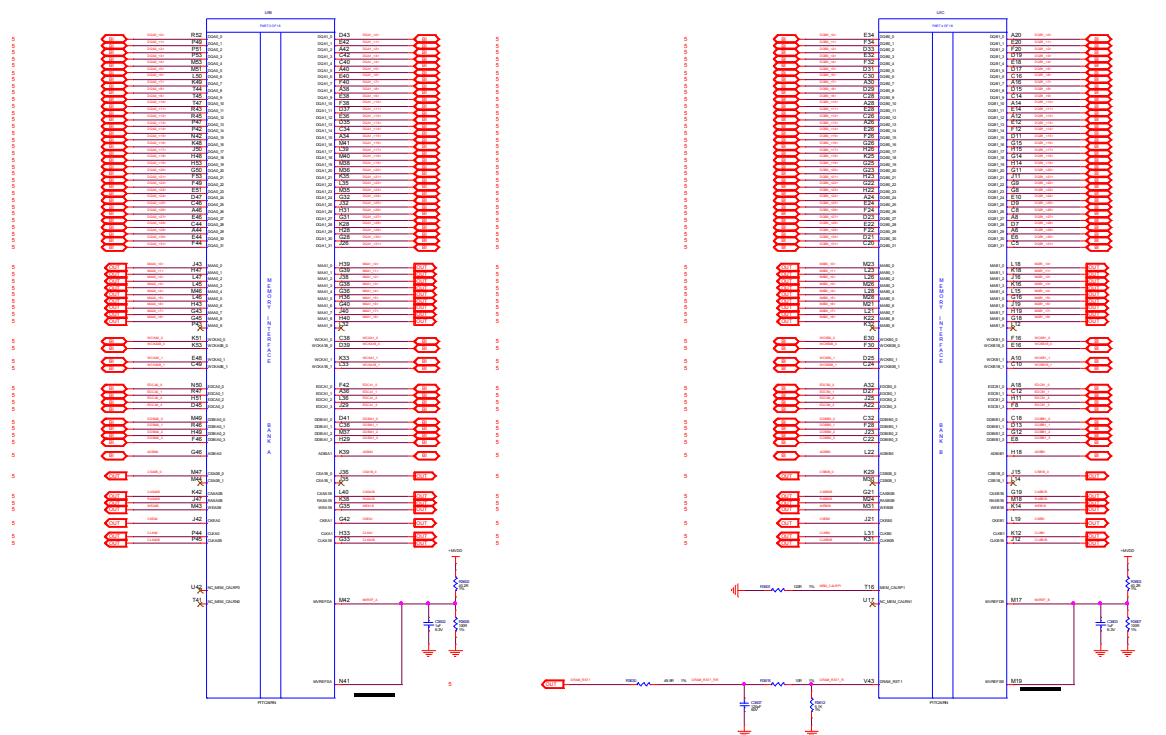


SYMBOL LEGEND	
	
	
	
	
	

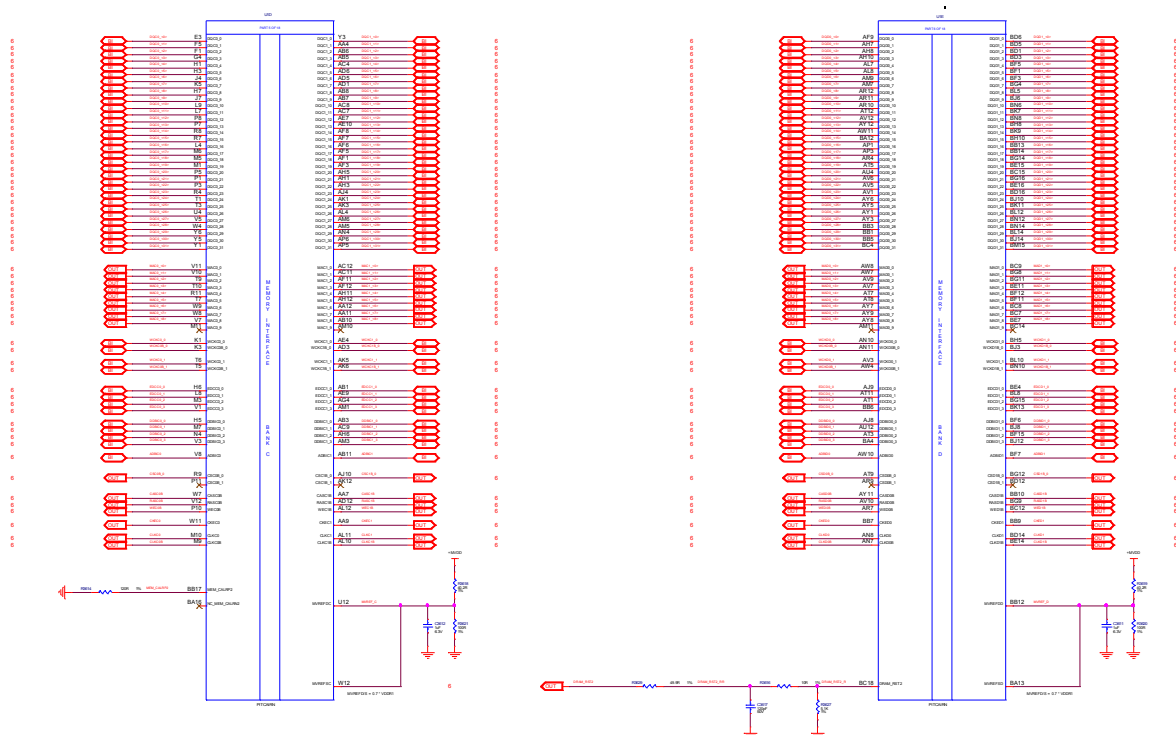
(2) CURACAO PCIE INTERFACE



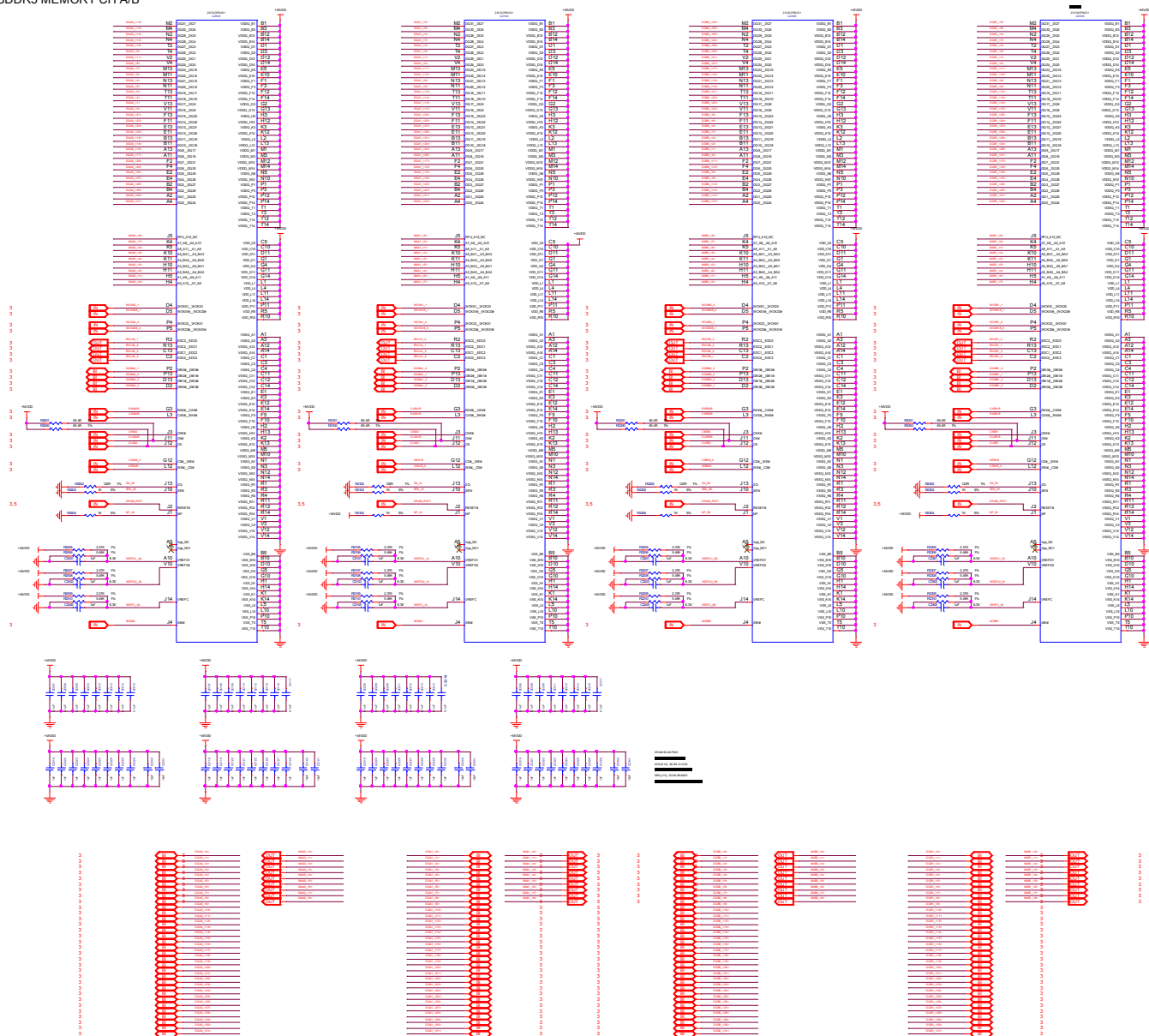
(3) CURACAO MEM INTERFACE CH A/B



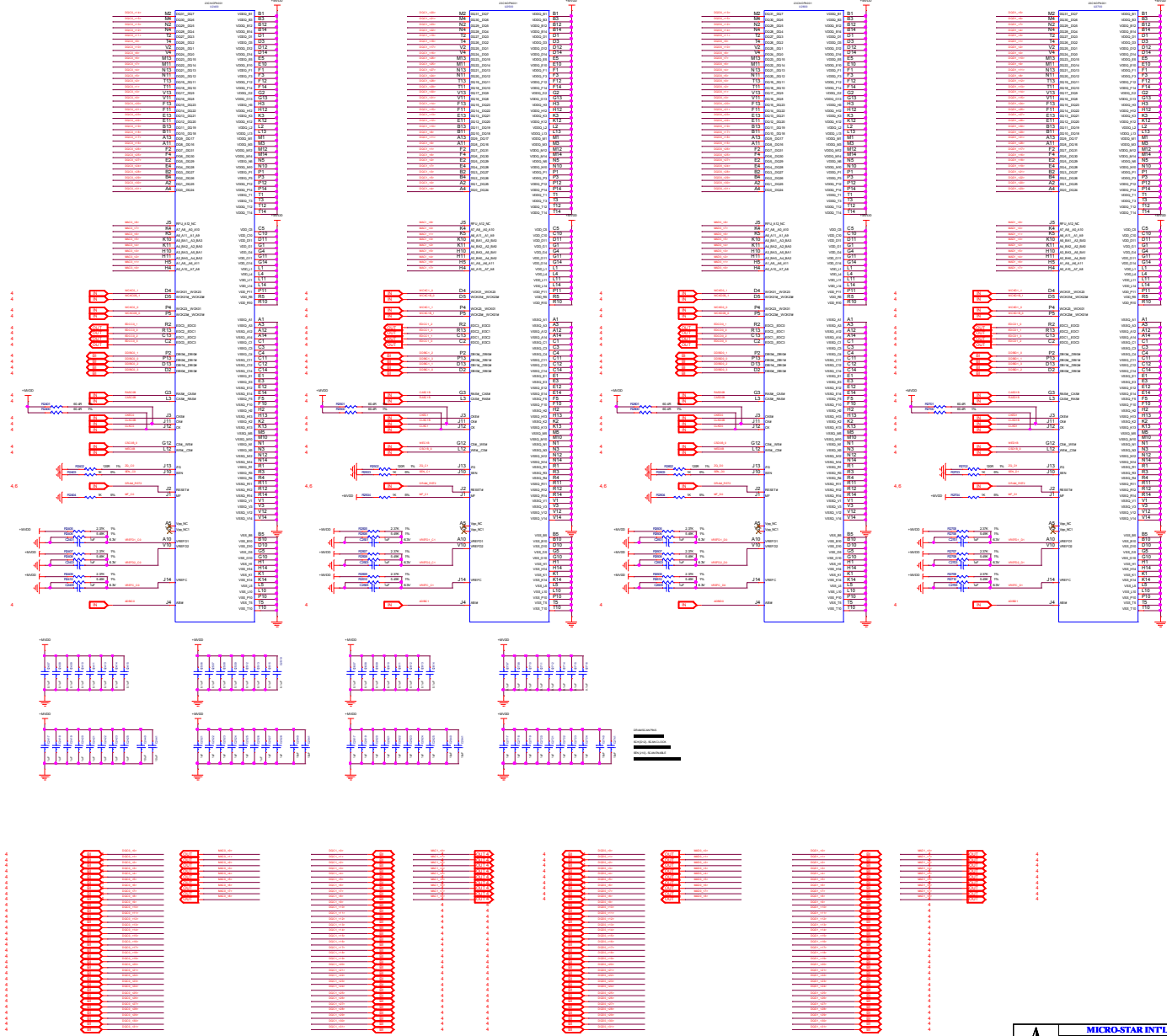
(4) CURACAO MEM INTERFACE CH C/D



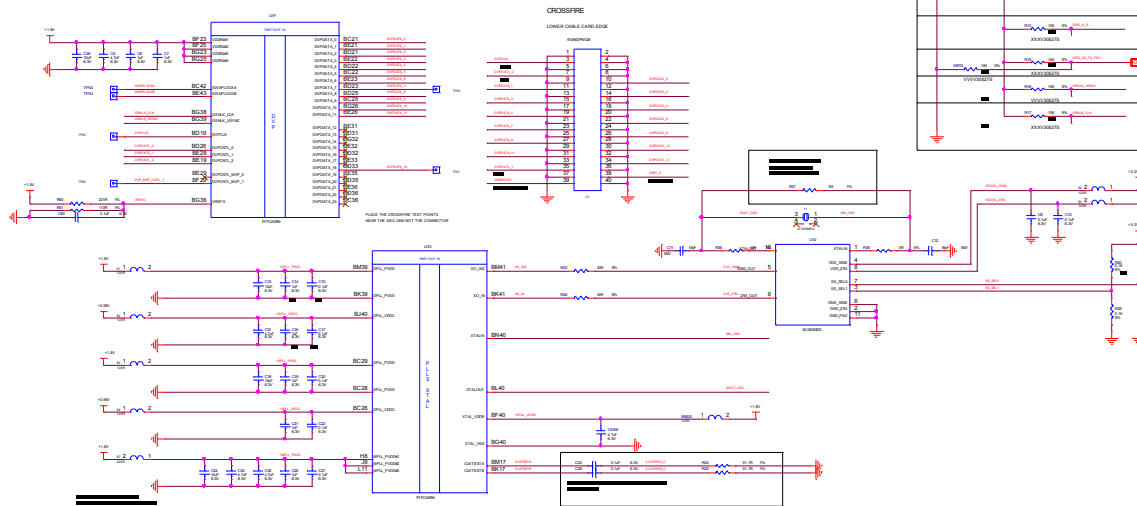
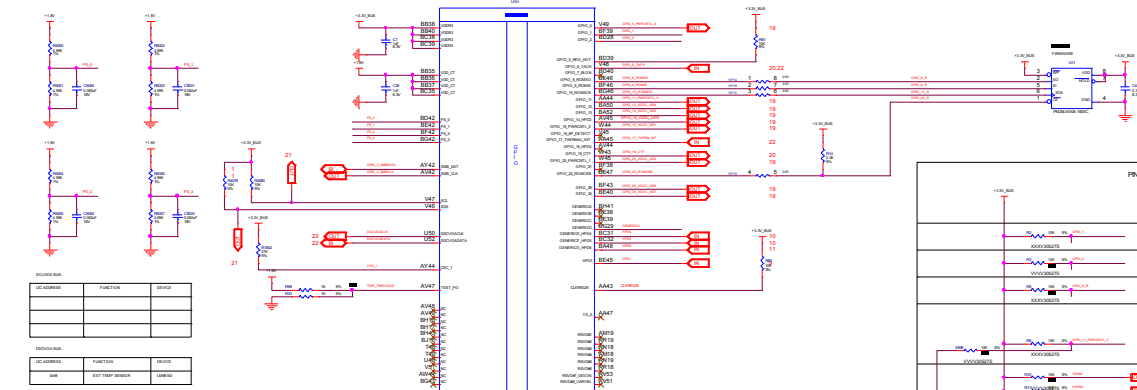
(5) GDDR5 MEMORY CH A/B



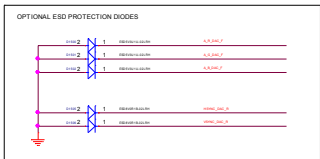
(6) GDDR5 MEMORY CH C/D



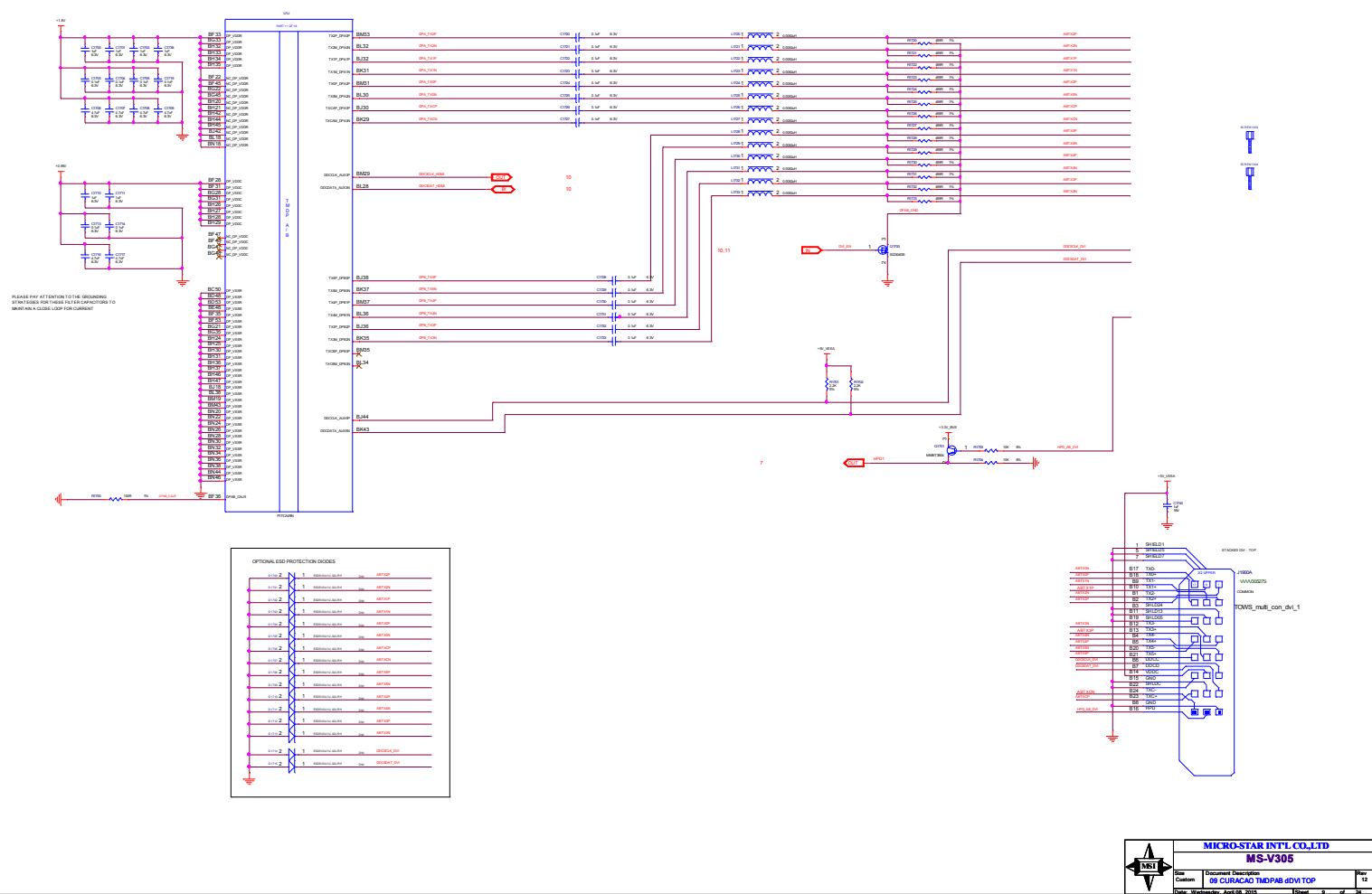
(7) CURACAO GPIO STRAP CF XTAL

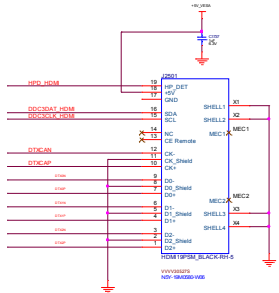
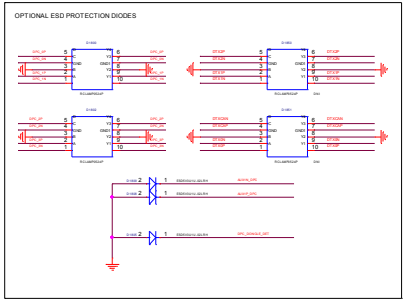
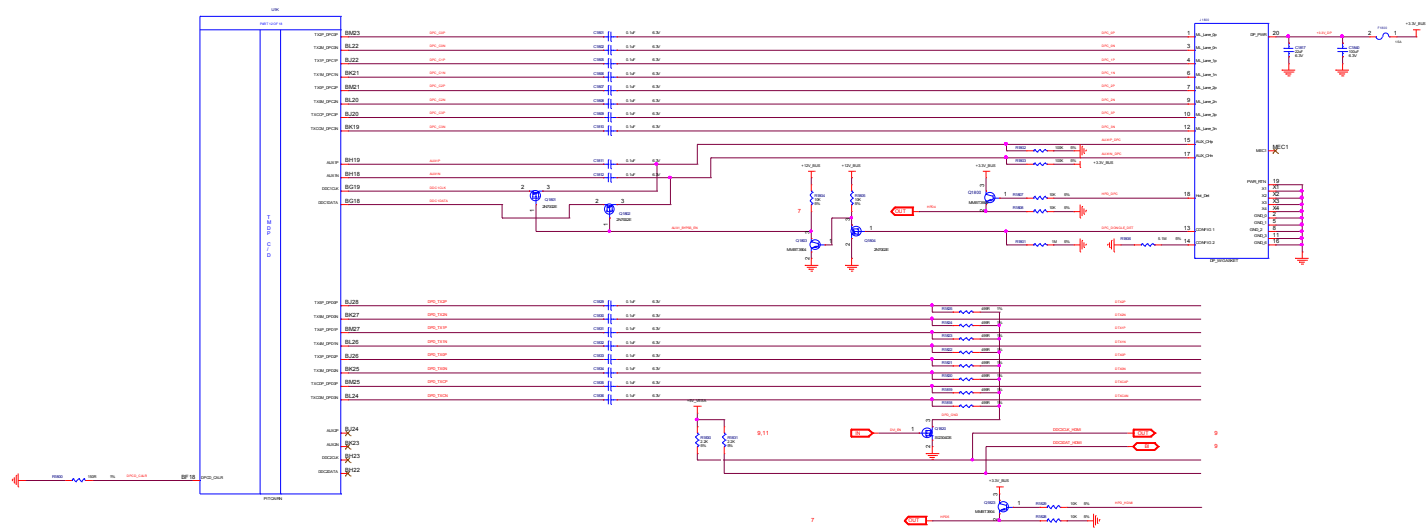


(8) CURACAO DAC1 LOCK

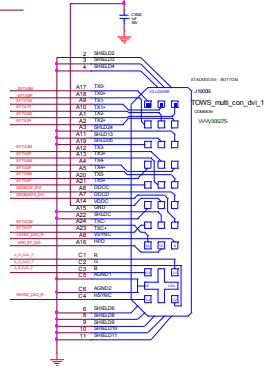
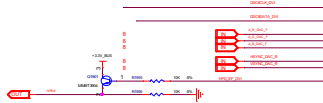
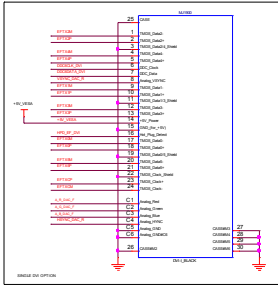
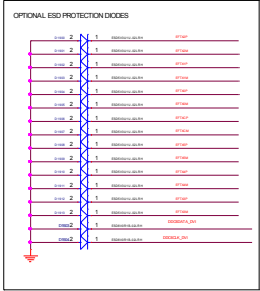
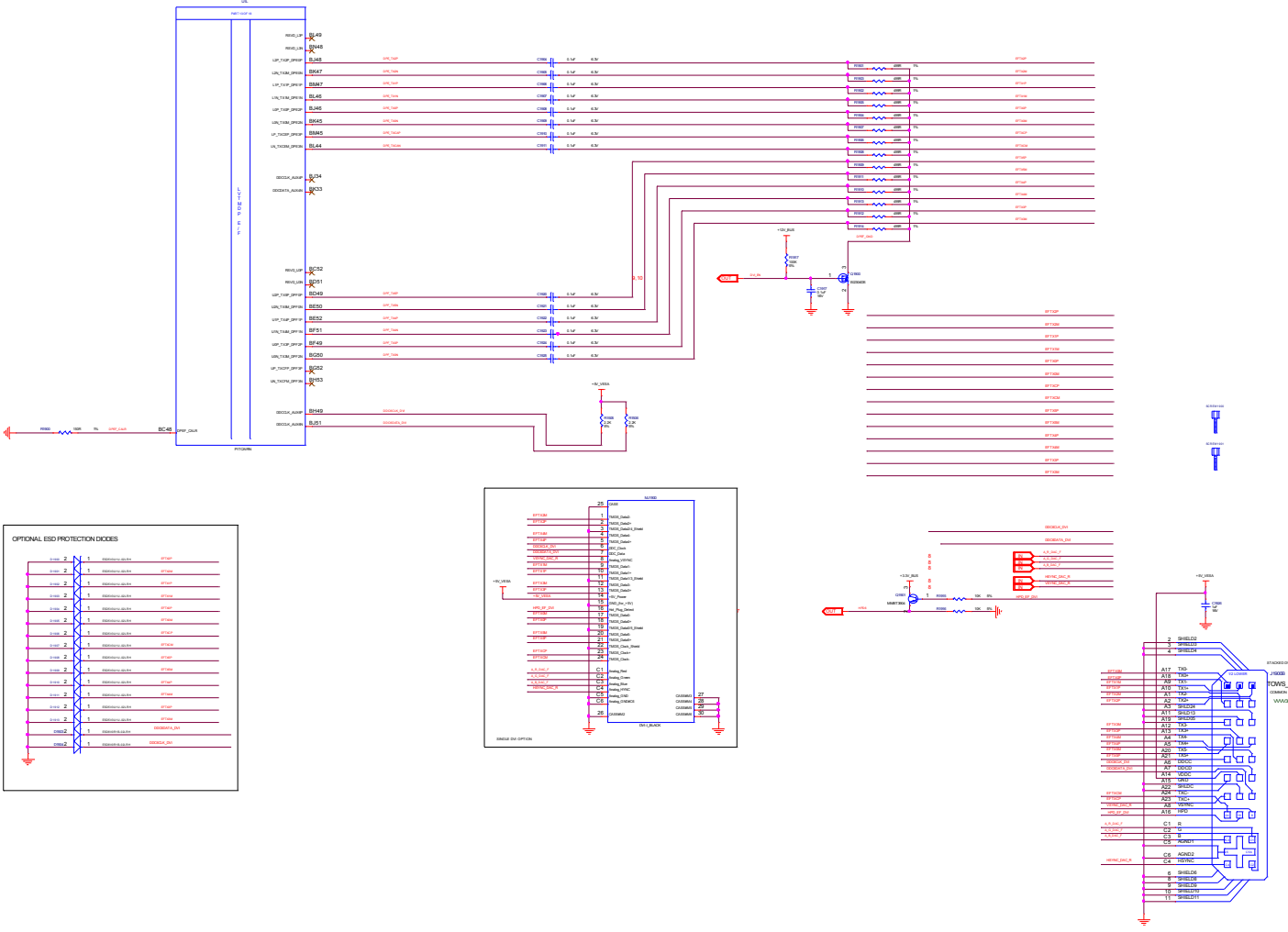


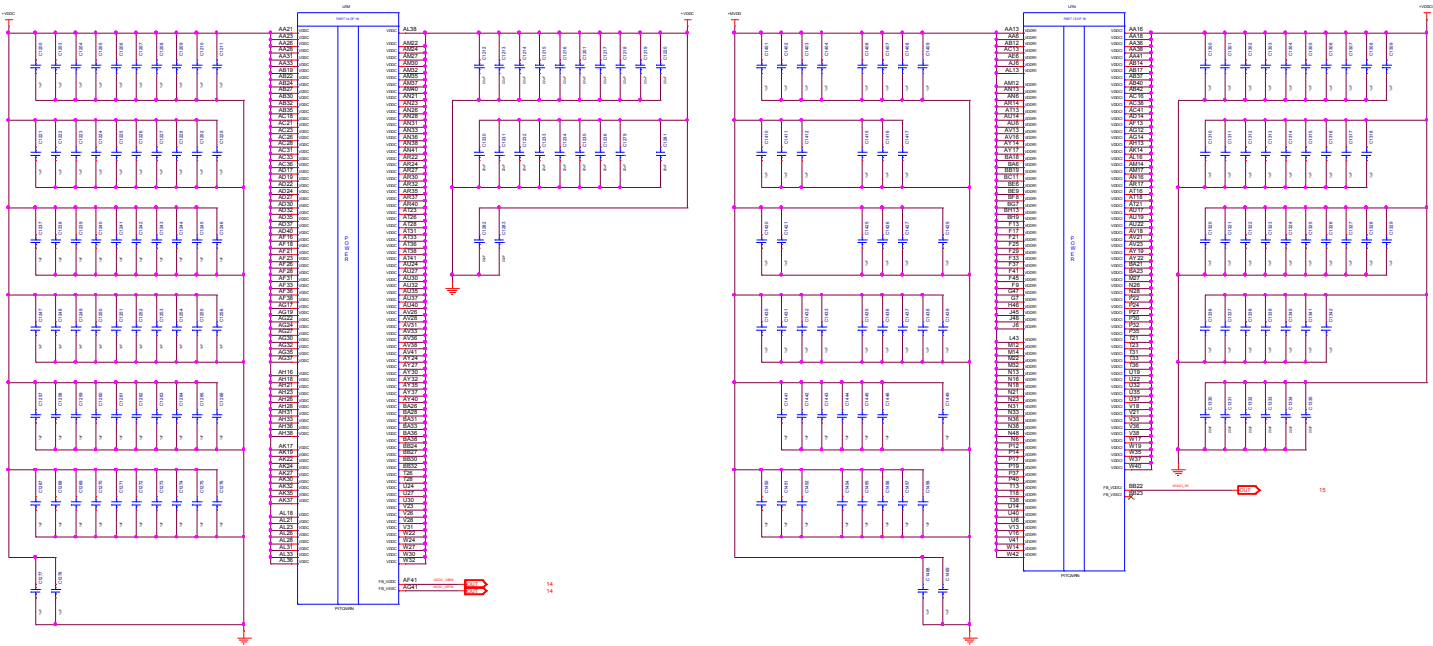
(9) CURACAO TMDP A/B

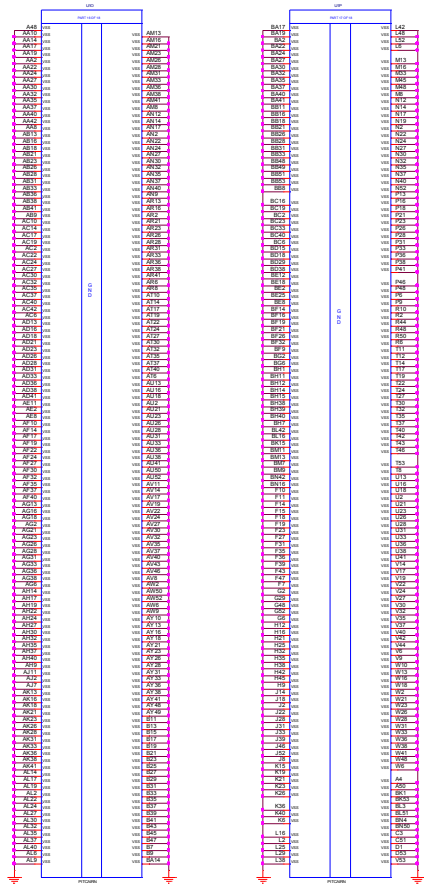


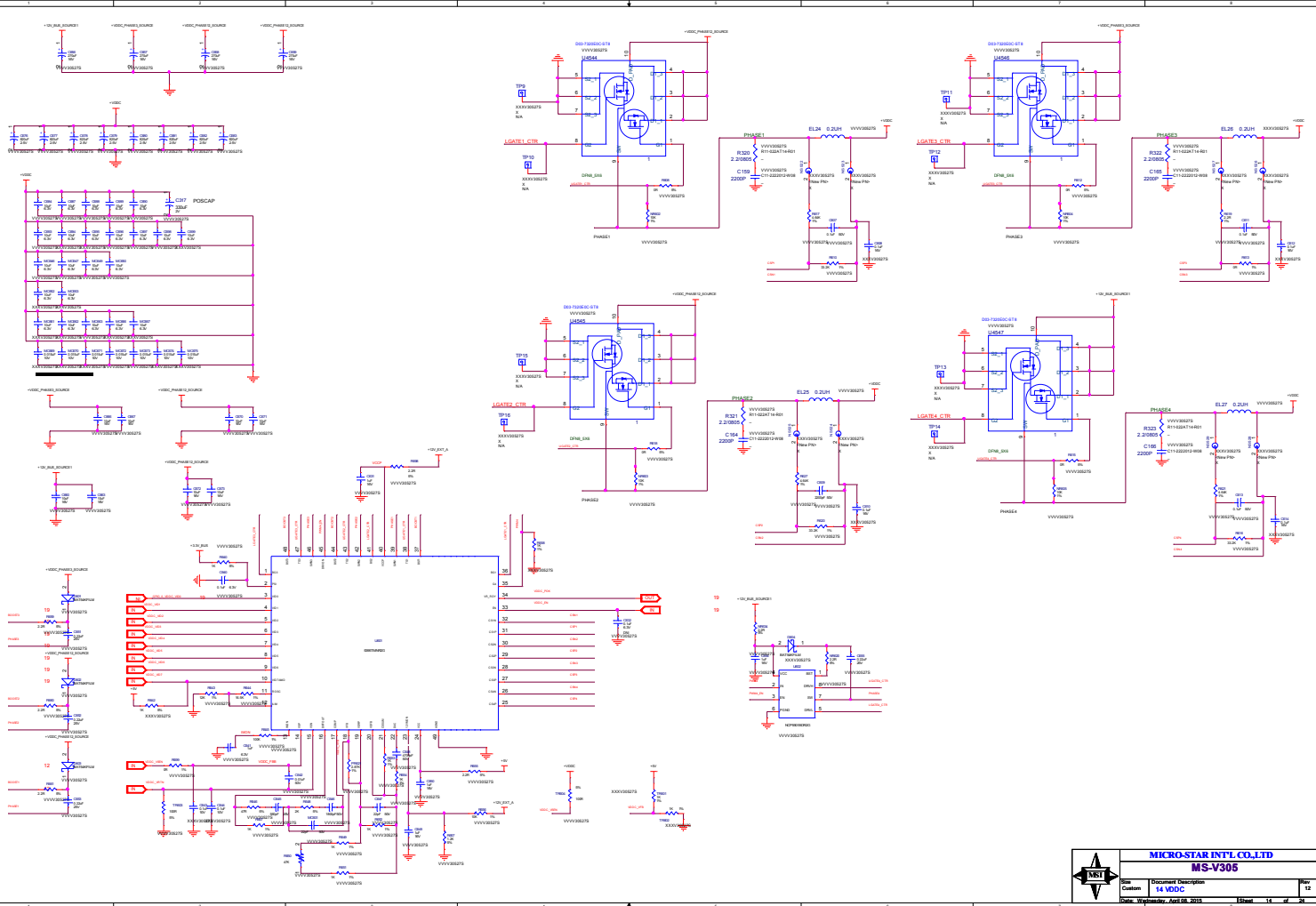


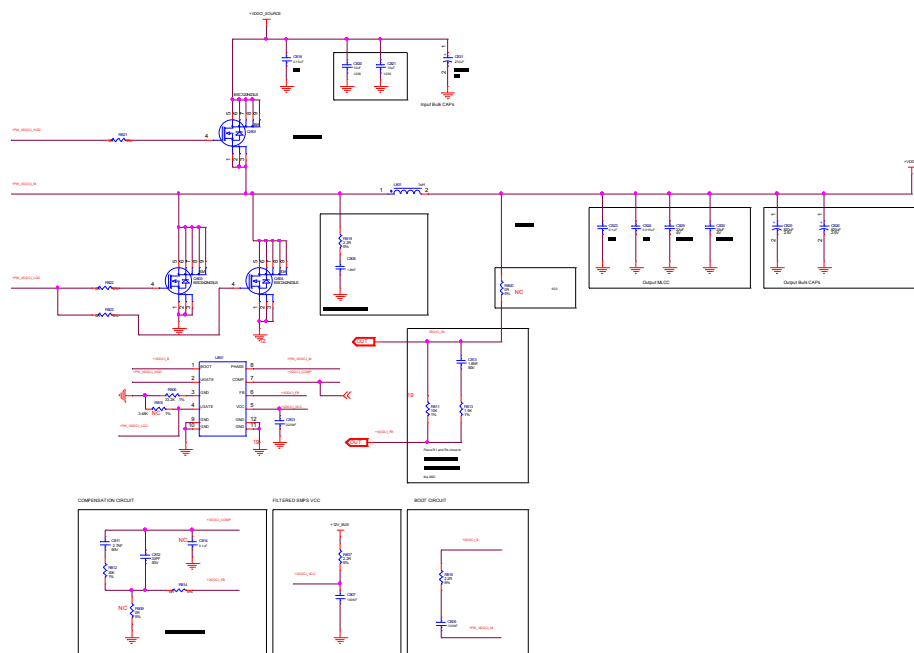
MICRO-STAR INTL CO., LTD		
MS-V305		
Rev	Document Description	Rev
01	10 CURACAO TMDPCD DP HDM	12
Date: September, April 08, 2015		











Layout guideline

1. The layout of the power plane should be as uniform as possible, and the thickness of the power plane should be as uniform as possible.

2. The layout of the power plane should be as uniform as possible, and the thickness of the power plane should be as uniform as possible.

3. The layout of the power plane should be as uniform as possible, and the thickness of the power plane should be as uniform as possible.

4. The layout of the power plane should be as uniform as possible, and the thickness of the power plane should be as uniform as possible.

5. The layout of the power plane should be as uniform as possible, and the thickness of the power plane should be as uniform as possible.

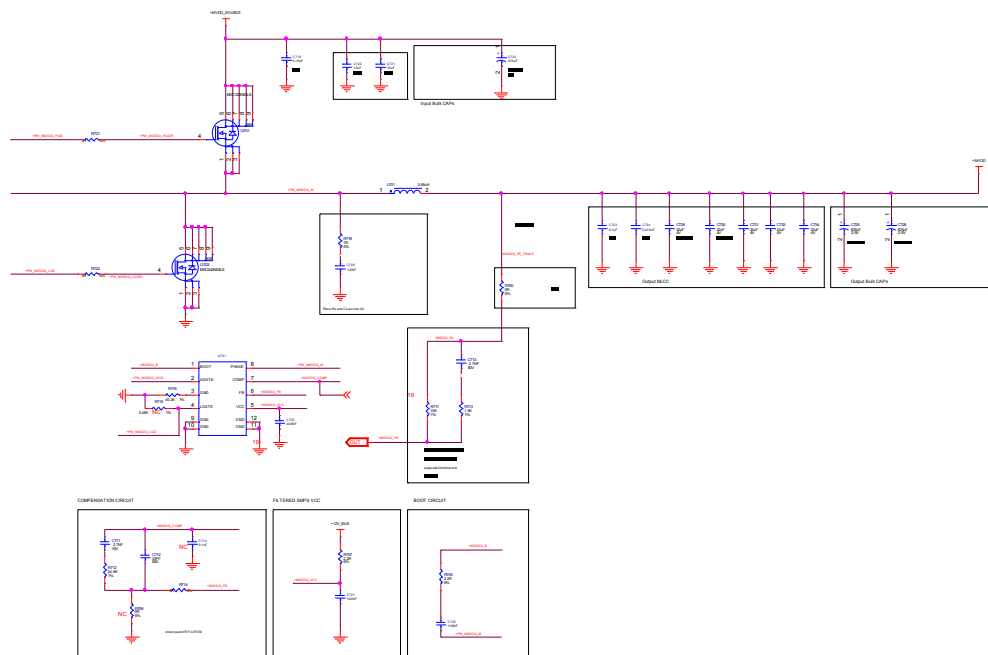
6. The layout of the power plane should be as uniform as possible, and the thickness of the power plane should be as uniform as possible.

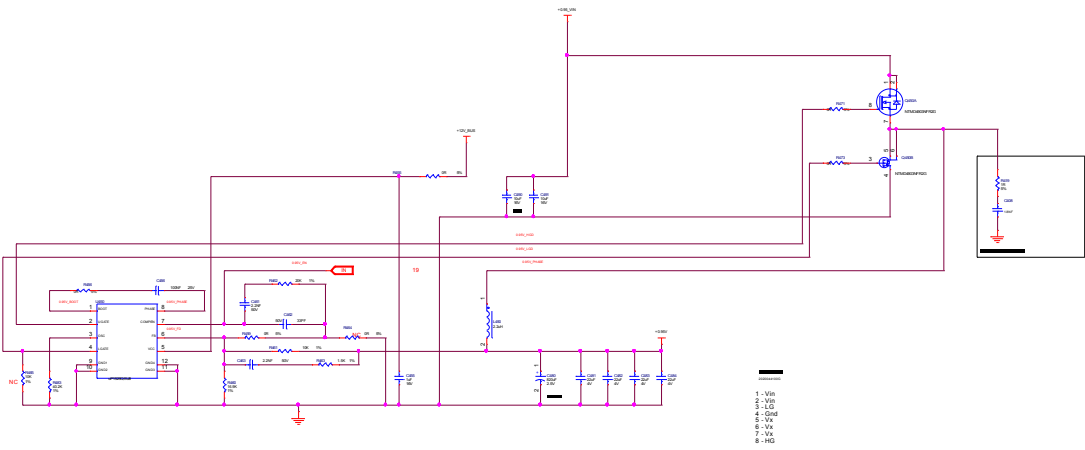
7. The layout of the power plane should be as uniform as possible, and the thickness of the power plane should be as uniform as possible.

8. The layout of the power plane should be as uniform as possible, and the thickness of the power plane should be as uniform as possible.

9. The layout of the power plane should be as uniform as possible, and the thickness of the power plane should be as uniform as possible.

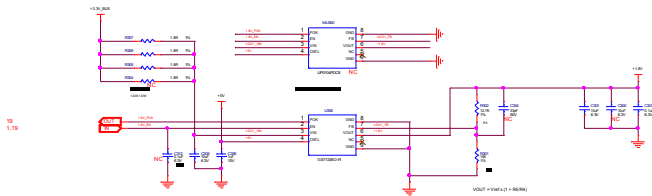
10. The layout of the power plane should be as uniform as possible, and the thickness of the power plane should be as uniform as possible.



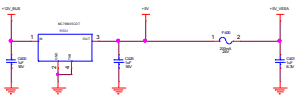


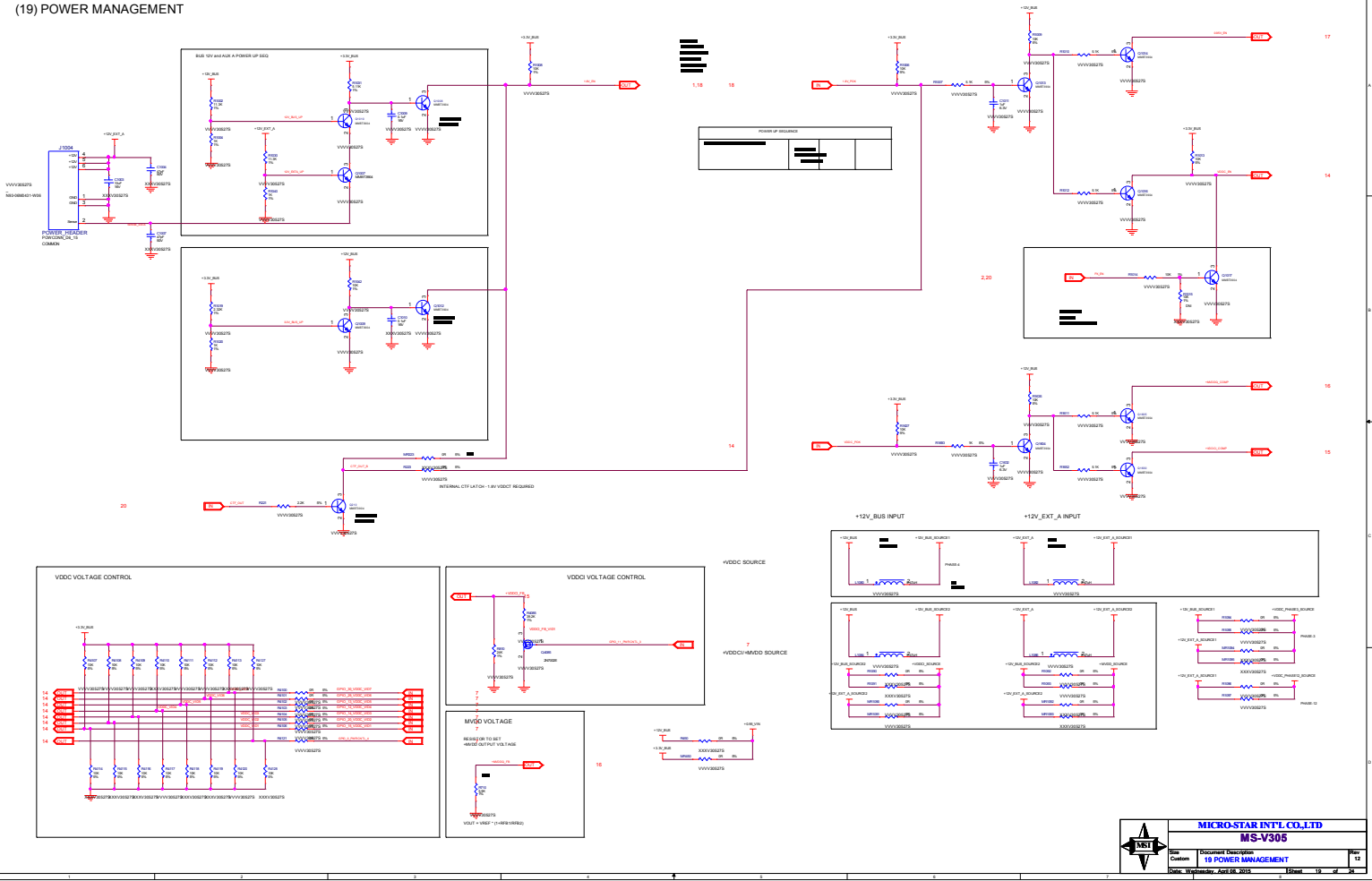
(18) SMALL RAIL REGULATORS

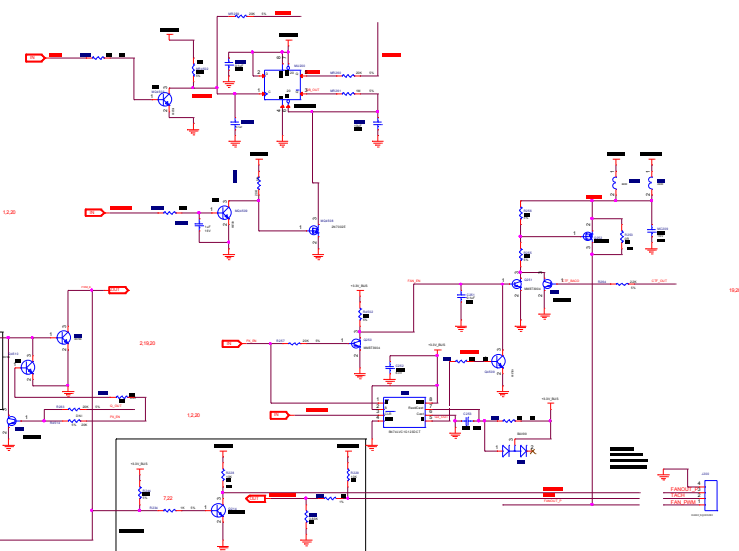
LOAD #1: VIN = 3.0V TO 3.6V MAX VOUT = +1.8V \pm 1.2% IOUT = 1.3A RMS MAX
PCB: 50 TO 70mm SQ. COPPER AREA FOR COOLING



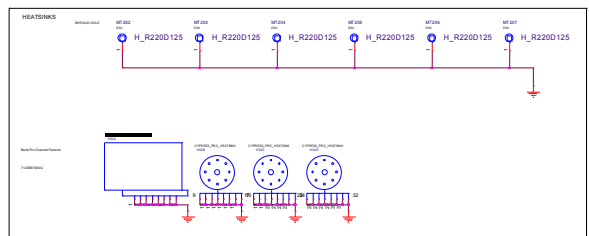
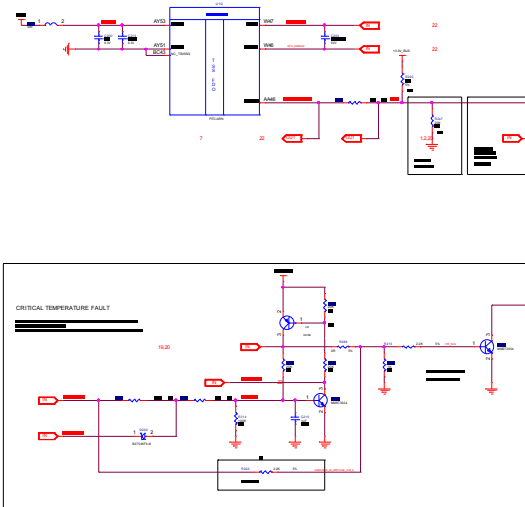
REGULATOR FOR +5V RAILS
IOUT MAX = 150mA



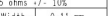

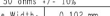
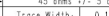




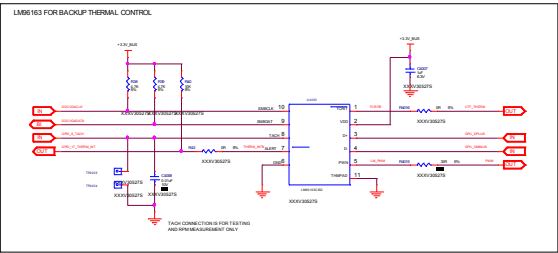
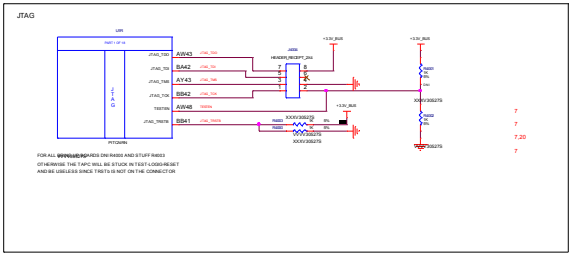
(20) MECHANICAL AND THERMAL MANAGEMENT



D1	D3	M1	M2
DIFFERENTIAL IMPEDANCE 45 ohms +/- 10%	DIFFERENTIAL IMPEDANCE 80 ohms +/- 10%	MICROSTRIP IMPEDANCE 50 ohms +/- 10%	MICROSTRIP IMPEDANCE 45 ohms +/- 5 ohms
Trace Width: 0.11 mm	Trace Width: 0.13 mm	Trace Width: 0.102 mm	Trace Width: 0.13 mm
Spacing: 0.14 mm	Spacing: 0.18 mm	On Layers: 1, 6	On Layers: 1, 6
On Layers: 1, 6	On Layers: 1, 6	Referenced to: 2, 5	Referenced to: 2, 5
Referenced to: 2, 5	Referenced to: 2, 5	Note: DVO, CLKTEST, RGB	Note: MEM
Note: DP, PCIe	Note: MEM_CLK		





Note:

2015/02/25	
page: 7	移除GPIO_0_PWRCNTL_4 / GPIO_13_VDDC_VID5 / GPIO_12_VDDC_VID4 預留線路
page:12	移除C317 poscap
page:14	移除VDDC out put cap*22pcs & add 330uFposcap*1 移除PWM VID0 pull low 電阻建立至page19微控制 MOS更換為dual N 物料
page:19	新增GPIO_0 High / LOW 控制 移除VDDCI VOLTAGE CONTROL GPIO_0 選擇線路 更換L1082 footprint 更換POWER_HEADER footprint
page:20	移除2 PIN風扇線路 / 增加螺絲孔*3
page:21	新增LED線路
page:22	移除CTF debug 線路 移除BACO MODE LED 線路 移除VDDC / VDDCI debug 測試點
2015/02/25	
page:20	修改4PIN FANCONINTER 接線
page:21	修改2PIN header 大小為2