

GF100-P1022

P1022-B00 GF100, GDDR5 384Bi t  
DVI -I -DL, DVI -I -DL/DP, Mi ni -HDMI

TABLE OF CONTENTS

Page	Descripti on
1	Table of Contents
2	Block Diagram
3	PCI Express 2.0
4	MEMORY: GPU Partit ion A/B
5	FBA Partit ion
6	FBB Partit ion
7	MEMORY: GPU Partit ion C/D
8	FBC Partit ion
9	FBD Partit ion
10	MEMORY: GPU Partit ion E/F
11	FBE Partit ion
12	FBF Partit ion
13	GDDR5 Memory Decoupling
14	GPU Decoupling
15	DAC_A for South DVI -I
16	DAC_B for Mid DVI -I
17	I FP A/B Interface (South DVI )
18	I FP E/F Interface(Mi ddl e DVI )
19	I FP D Interface/Mi d DP
20	I FP C Interface (North mHDMI )
21	MI SC: GPIO, I2C, ROM, and XTAL
22	Mul ti -use I O(MI O) Interface
23	GPU POWER CONNECTIONS
24	Strapping Configurati on
25	MI SC: Thermal / BACKDRIVE

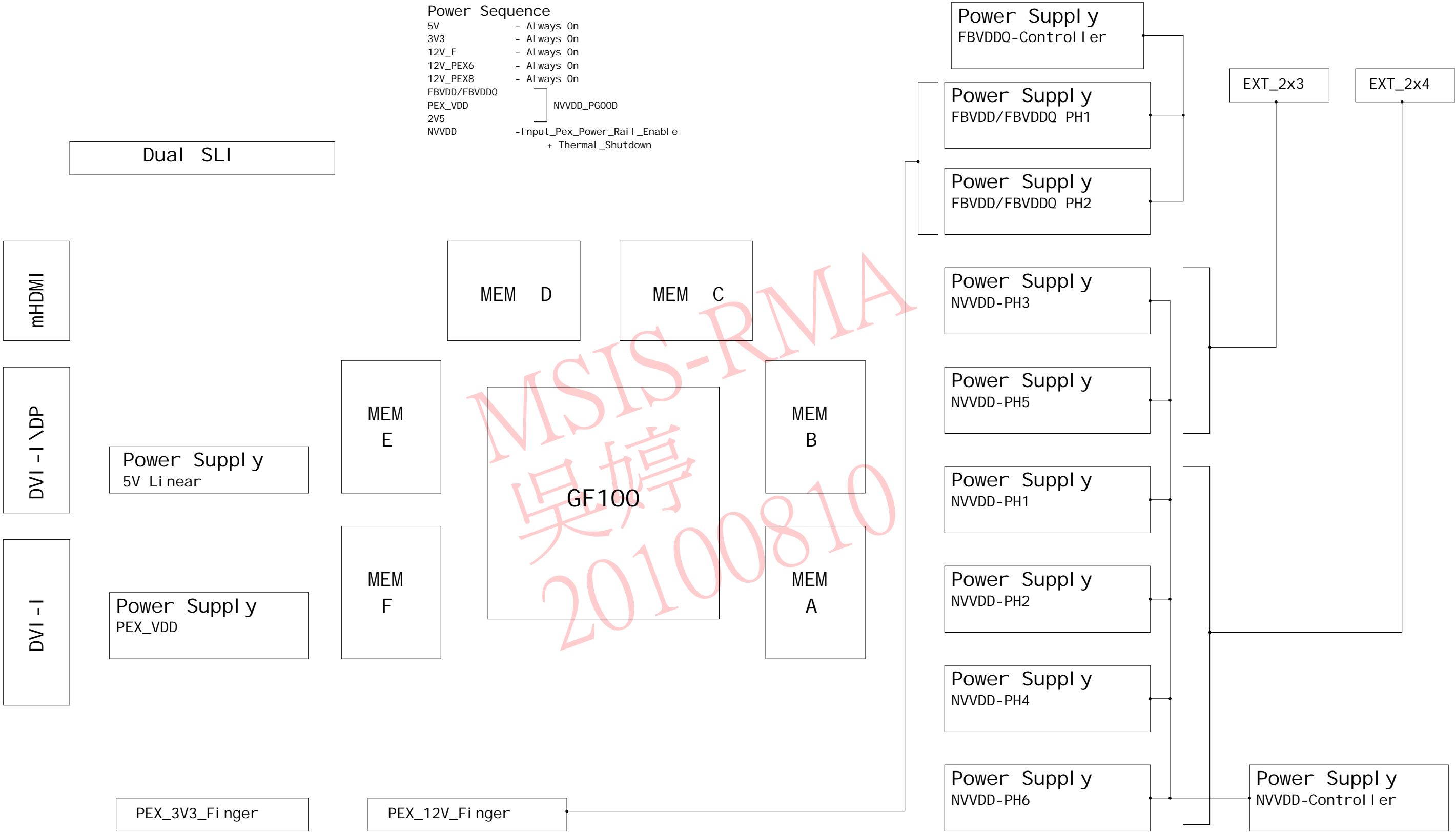
Page	Descri ption
26	Mechani cal
27	Power Supply: 5V, PEX_PLLVDD, 8V5
28	Power Supply: PEXVDD
29	Power Supply: FBVDDQ
30	Power Supply: NVVDD Controller
31	Power Supply: NVVDD Phase 1-2 of 6
32	Power Supply: NVVDD Phase 3-4 of 6
33	Power Supply: NVVDD Phase 5-6 of 6
34	Power Input, LED, Power Sequence
35	Power Supply: NVVDD Controller(Option)

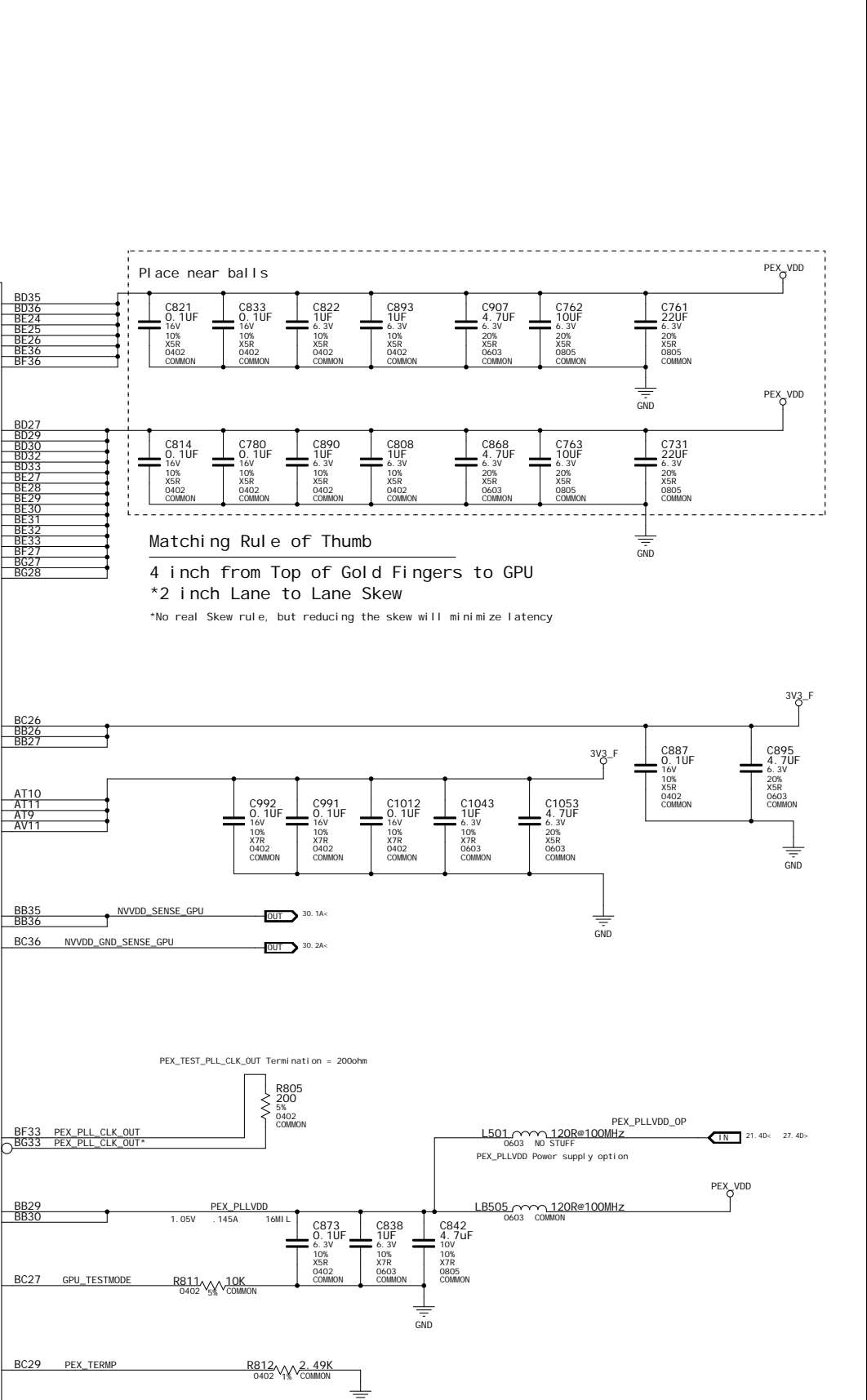
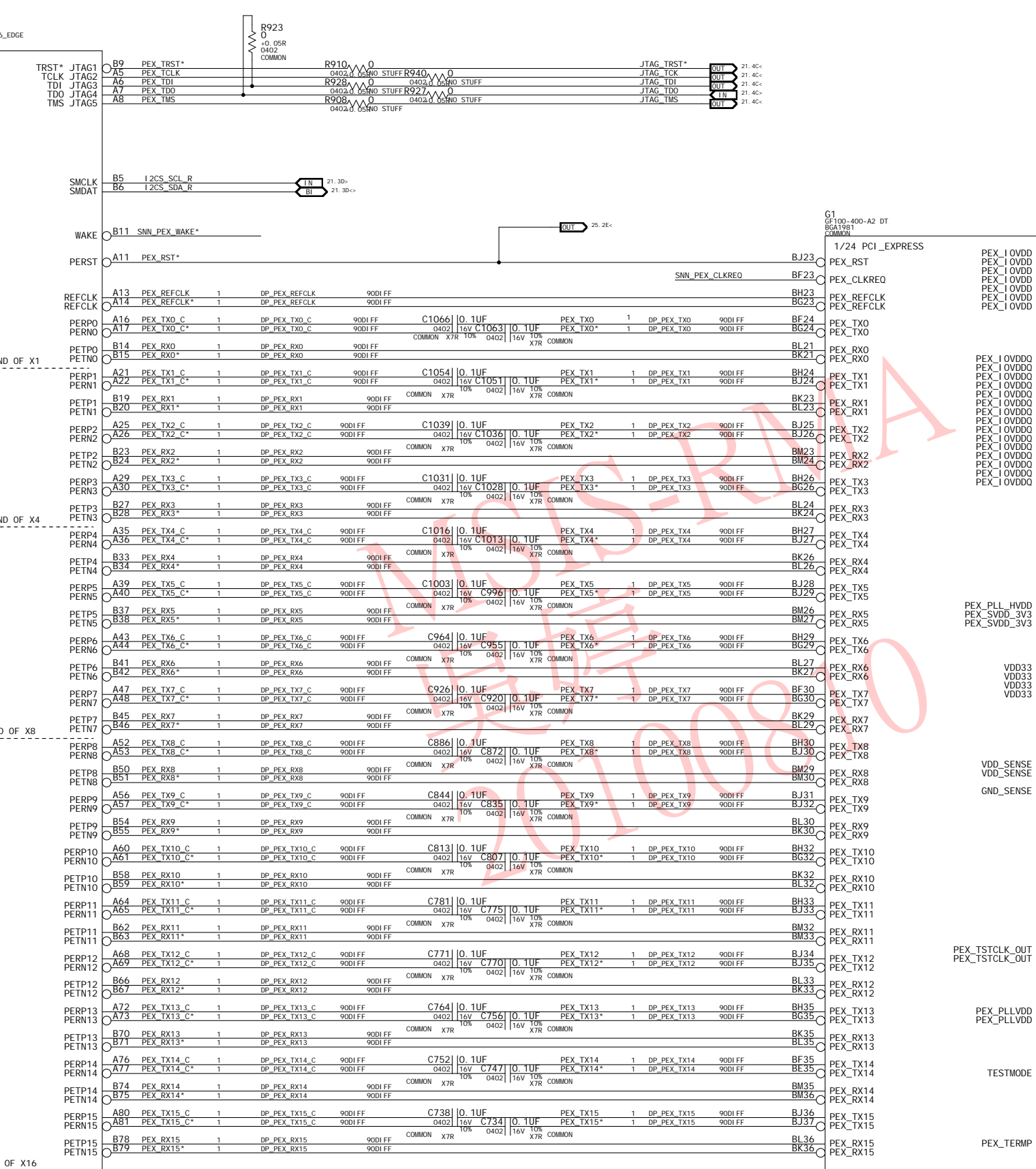
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2	SKU0001	600-11022-0001-200	P1022 GF100-400 1536MB GDDR5 32x32M DVI -I +DP+mHDMI
3	SKU0090	600-11022-0090-200	P1022 GF100-400 1536MB GDDR5 32MX32 DVI -I +DVI -I +mHDMI ADT7473 ENGINEERING SKU
4	SKU9900	600-11022-9900-200	P1022 GF100-400 1536MB GDDR5 32MX32 DVI -I +DVI -I +mHDMI PRIMARION ENGINEERING SKU
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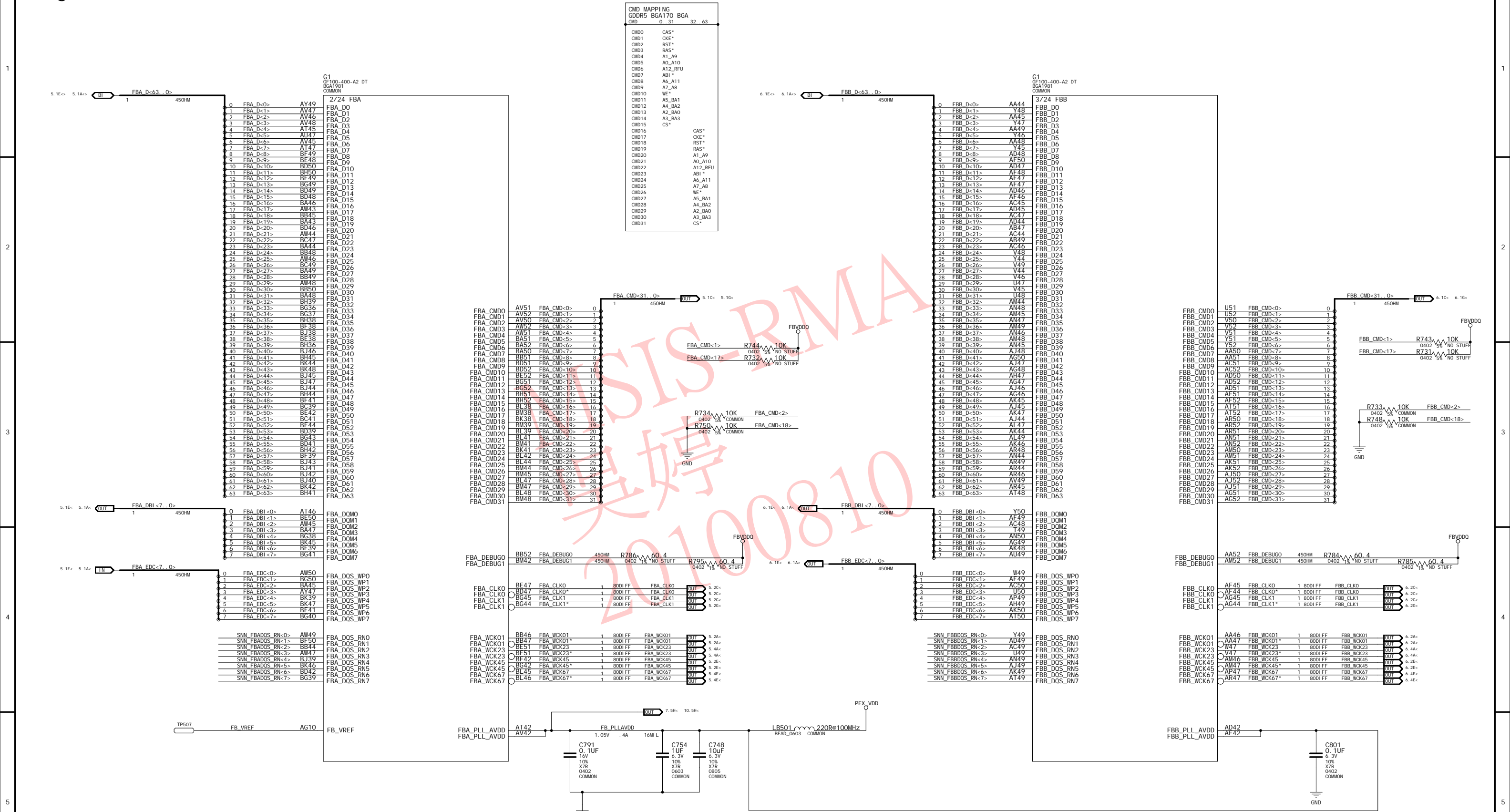
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Power Sequence

5V	- Always On
3V3	- Always On
12V_F	- Always On
12V_PEX6	- Always On
12V_PEX8	- Always On
FBVDD/FBVDDQ	- NVVDD_PG00D
PEX_VDD	- NVVDD_PG00D
2V5	- Input_Pex_Power_Rail_Enable
NVVDD	+ Thermal_Shutdown







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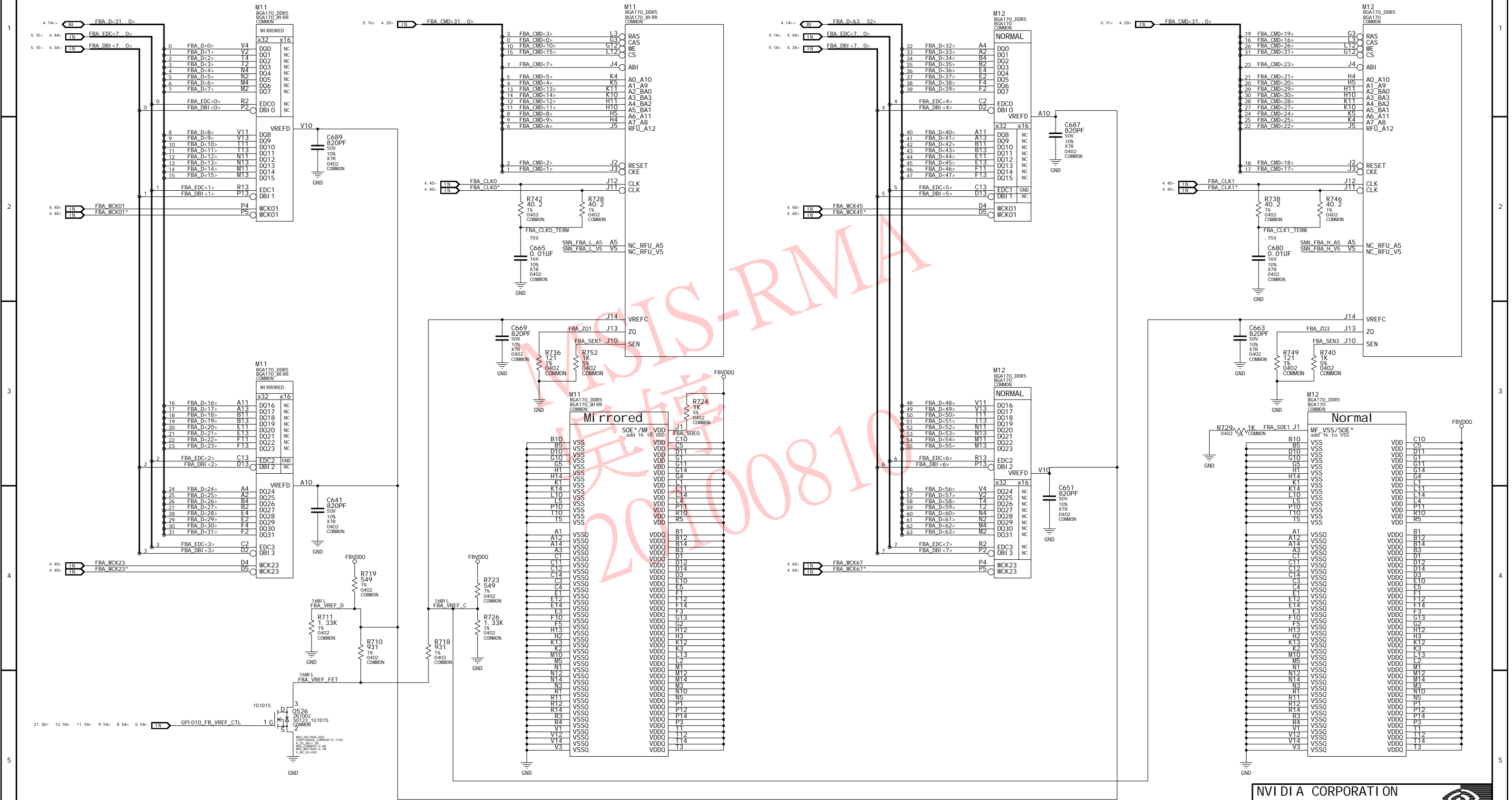
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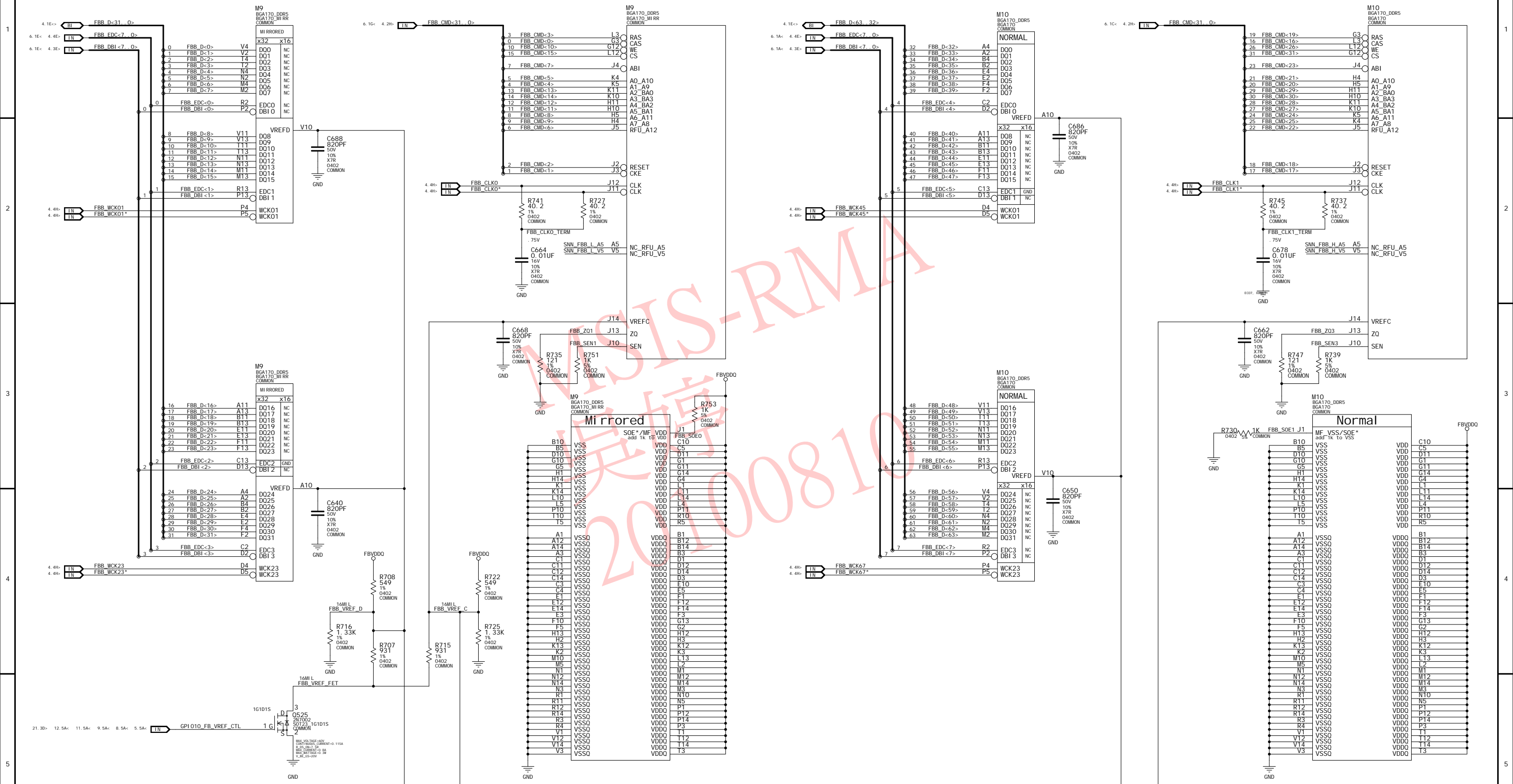


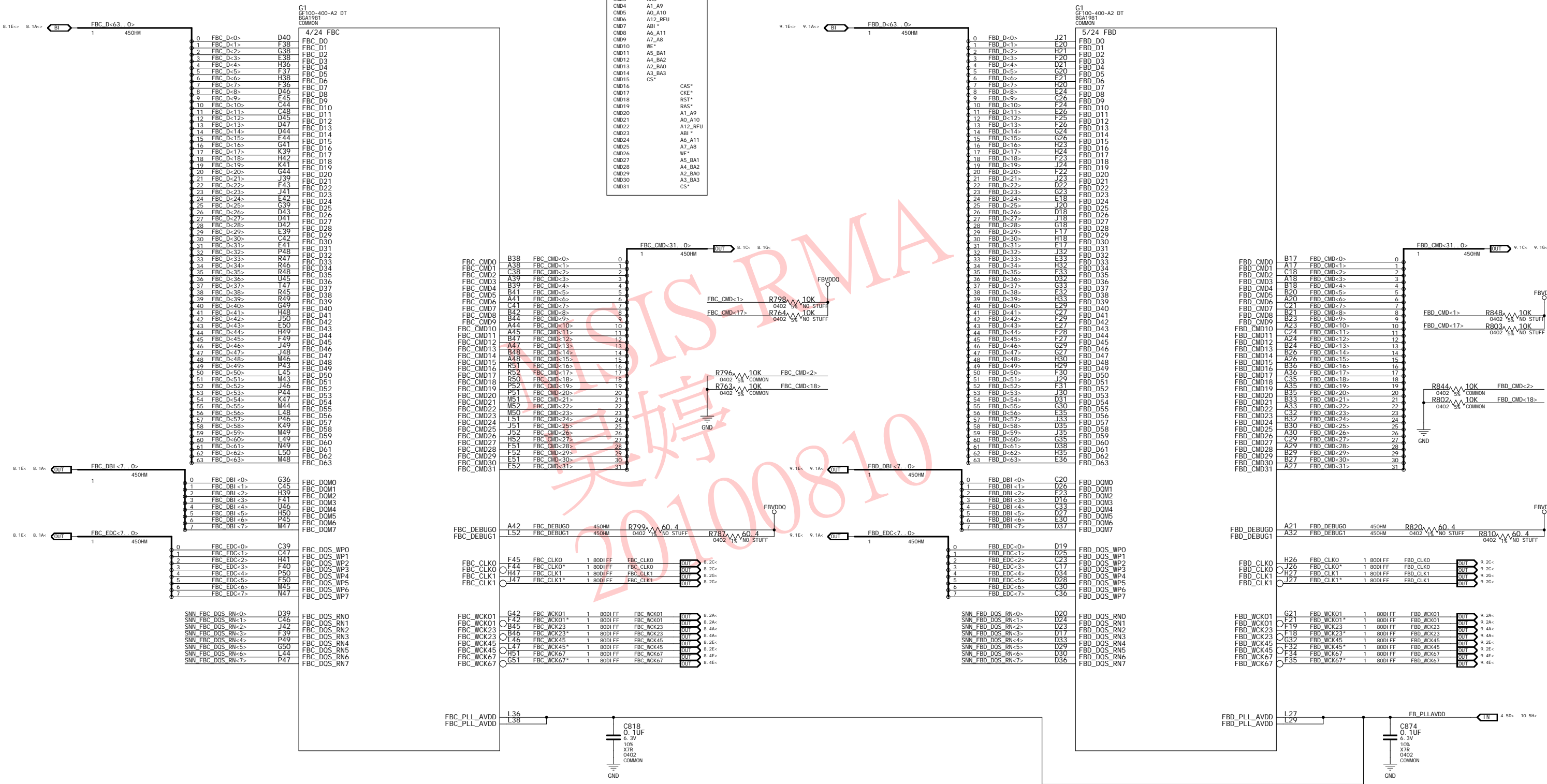
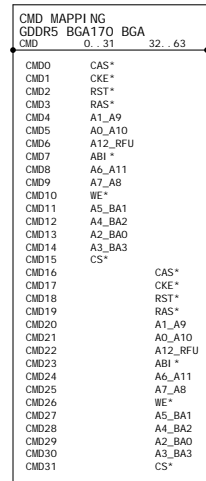


ASSEMBLY	P1022 GF100-400 1536MB GDDR5 32x32m DVI-I+DVI-I+mHDMI
PAGE DETAIL	FBA Partition

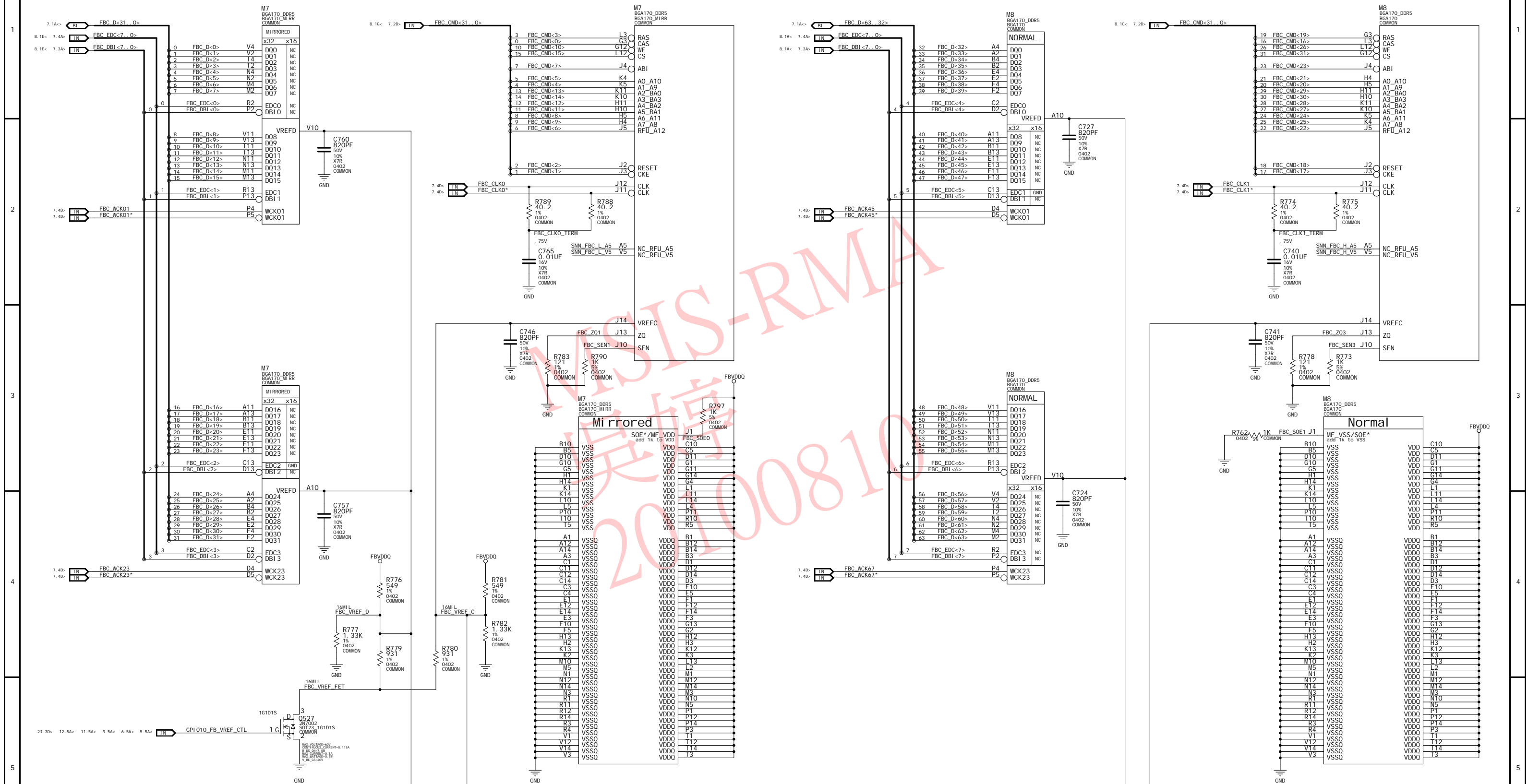
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PCB REV	P1022-B00	PAGE	5 OF 35
BOM REV	J	DATE	25-MAR-2010





## Page8: FBC Parti ti on



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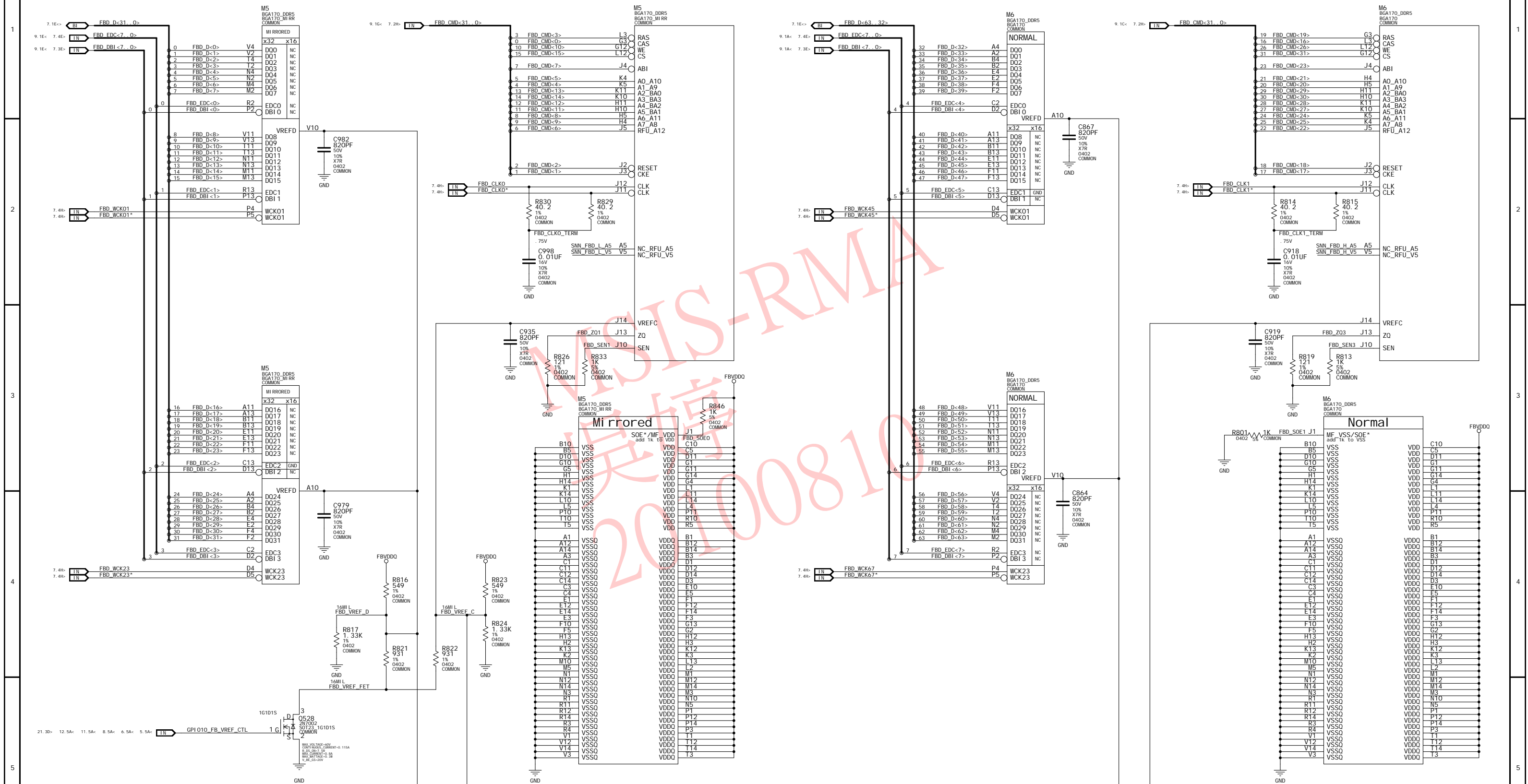


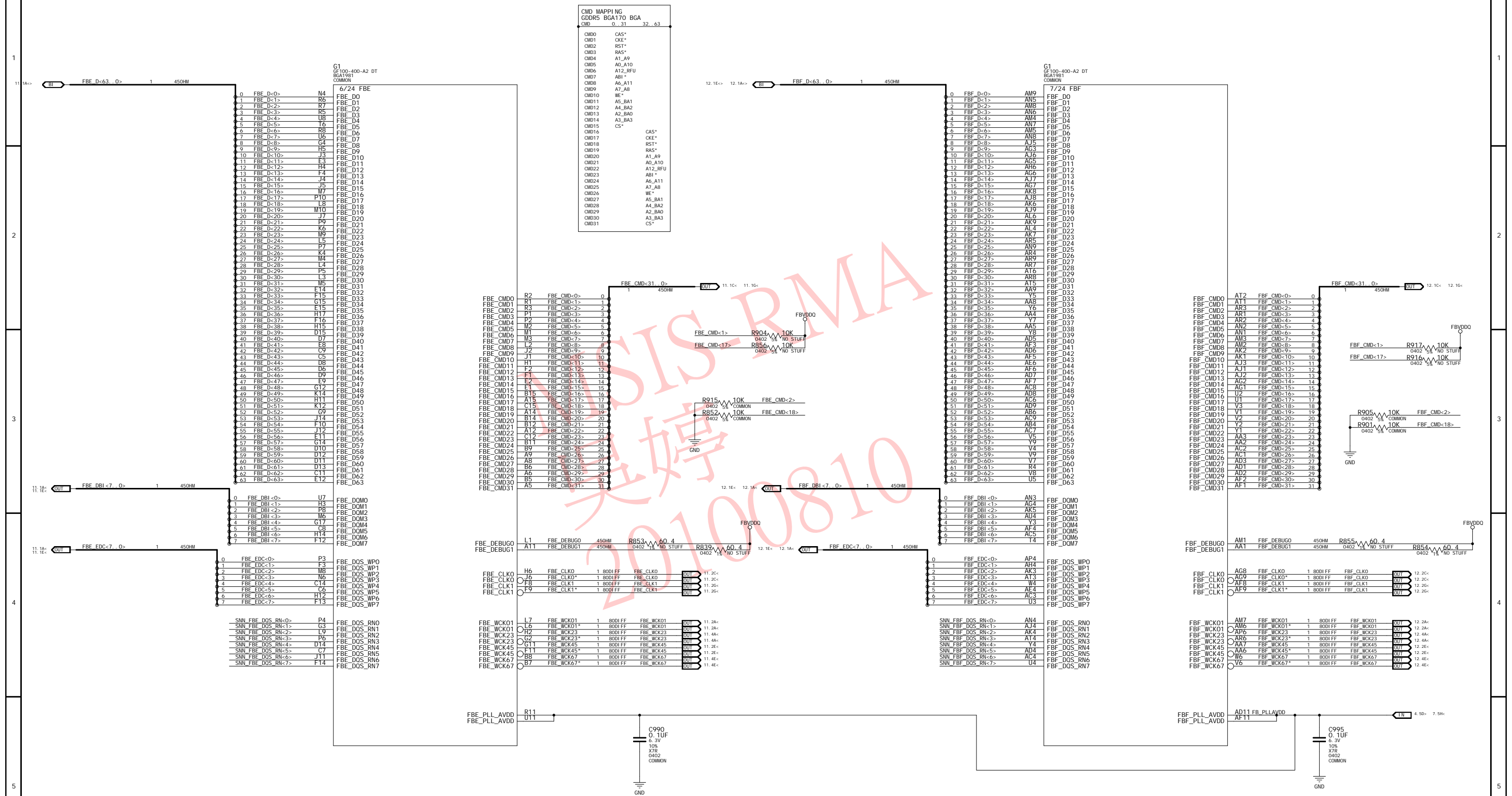
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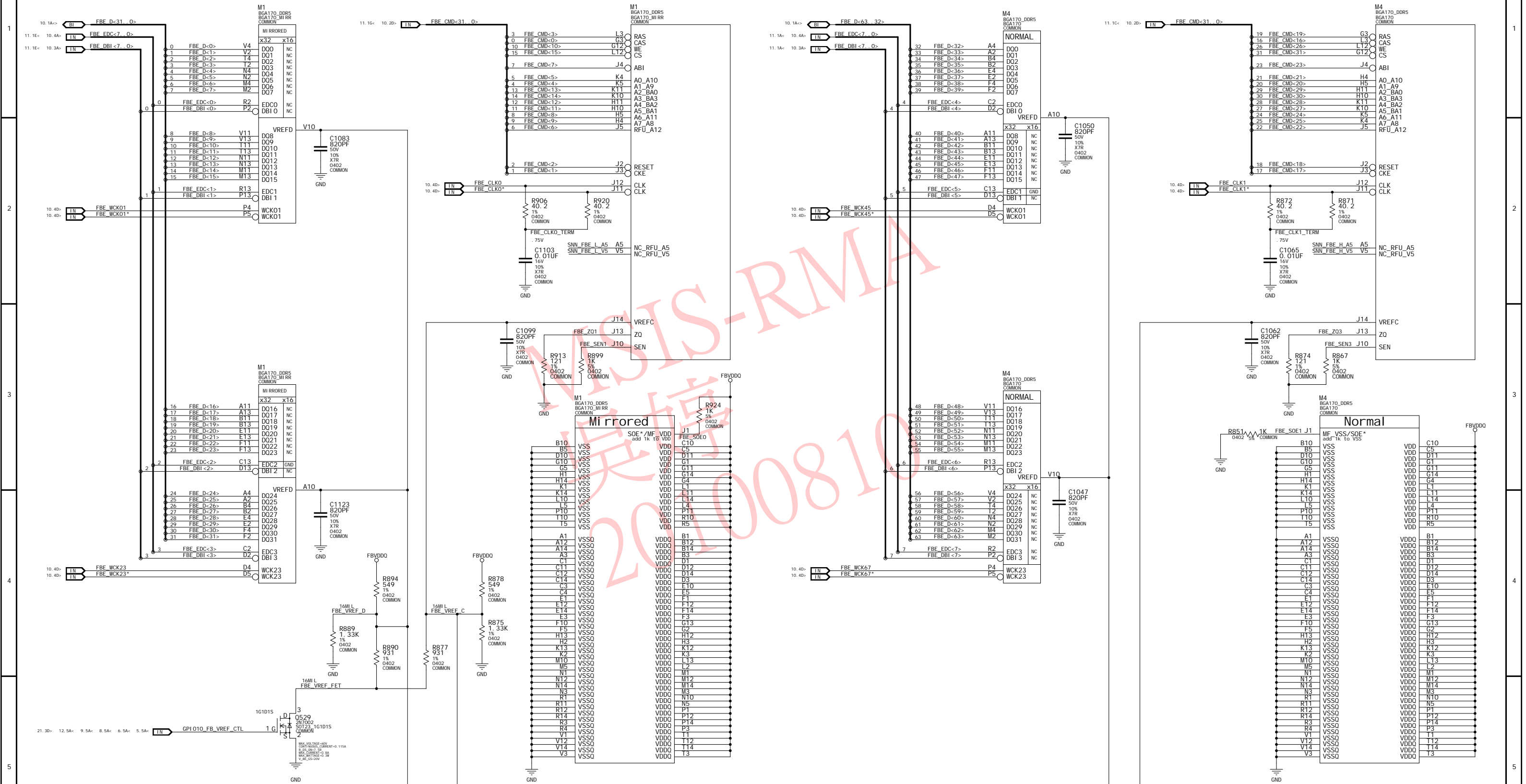
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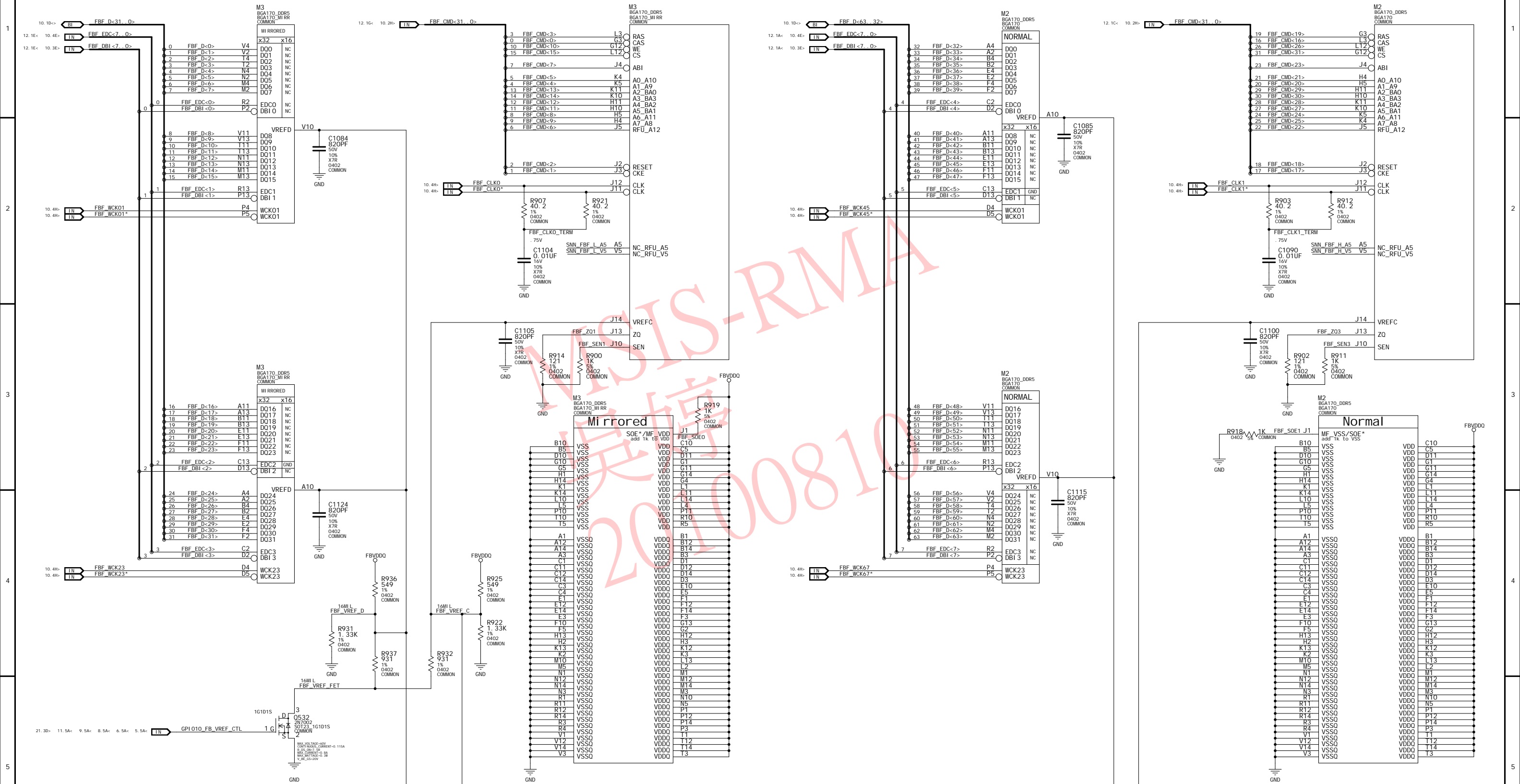






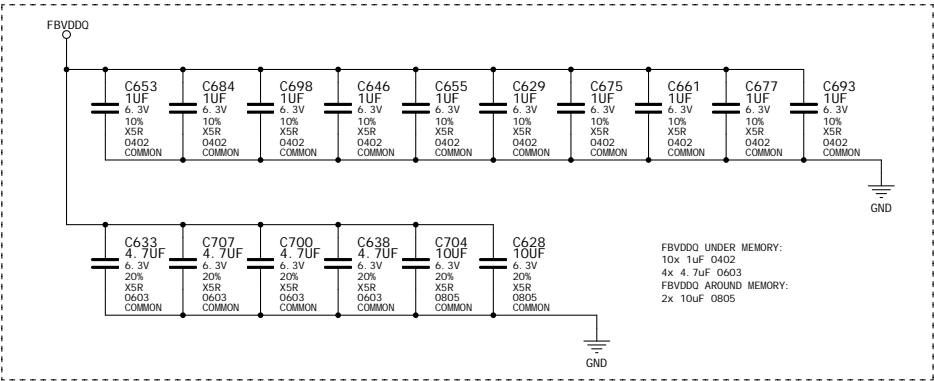
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PAGE DETAIL	FBE Partition

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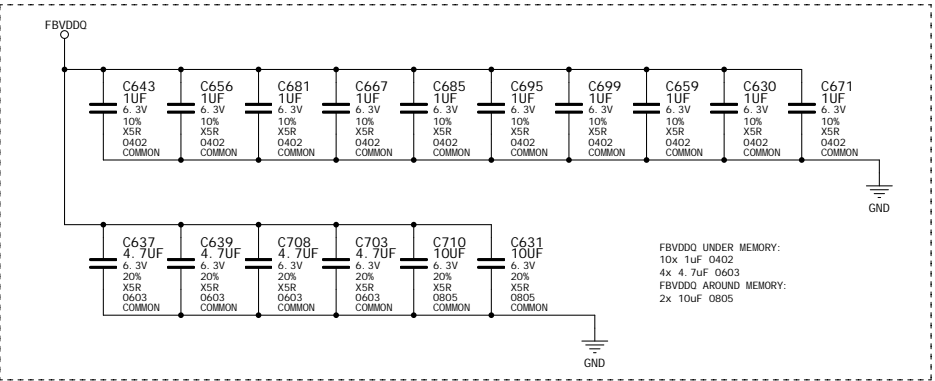




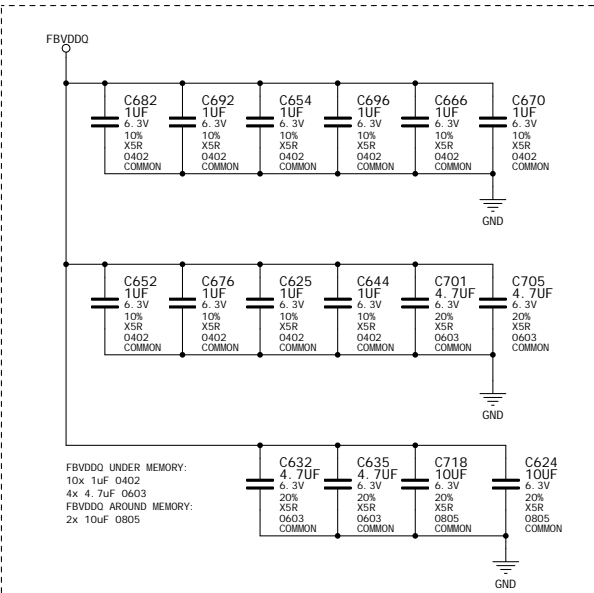
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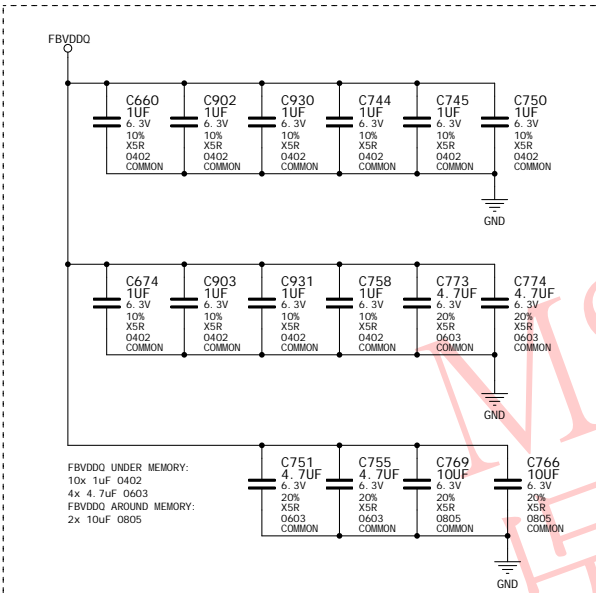
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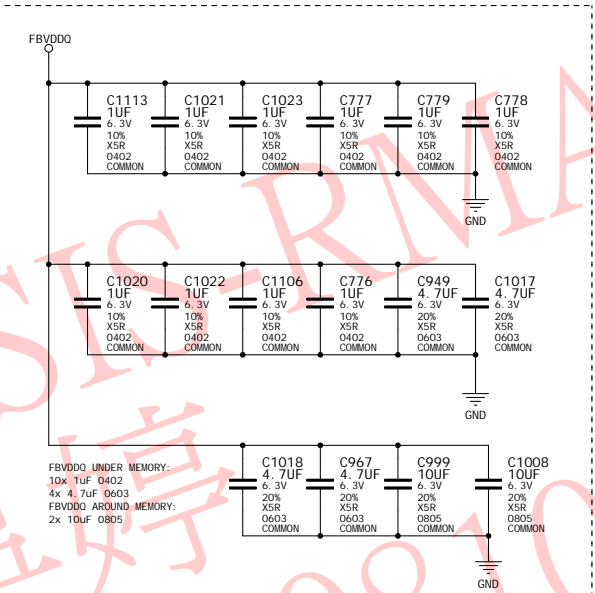
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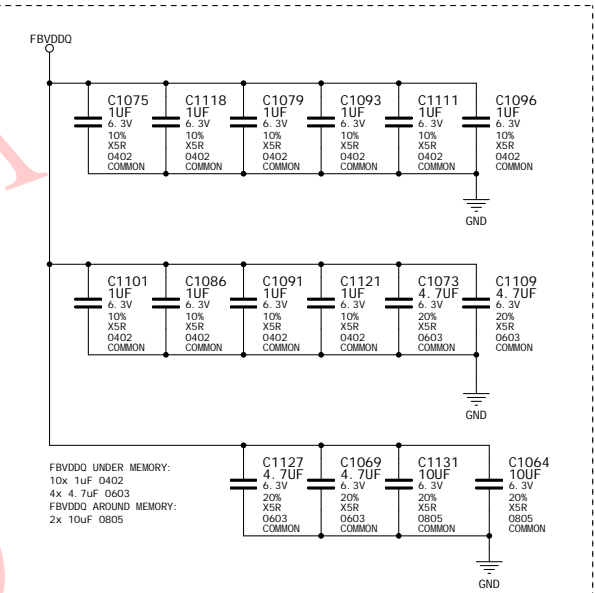
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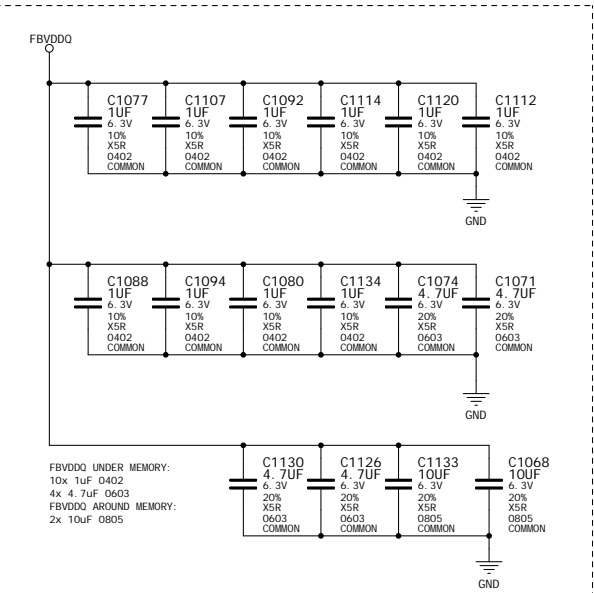
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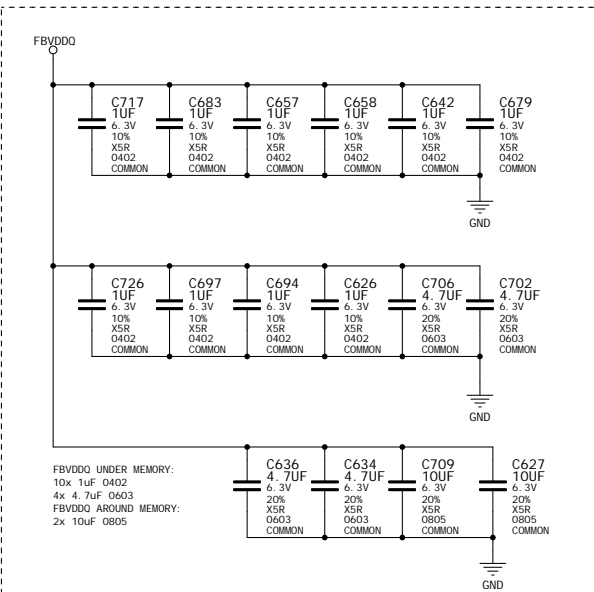
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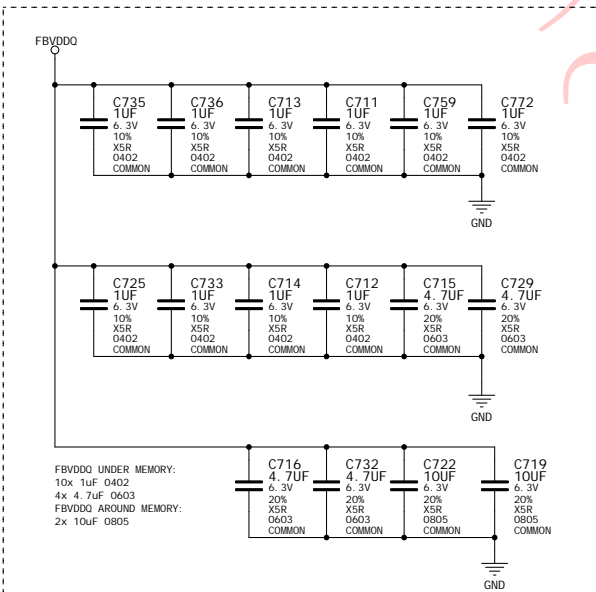
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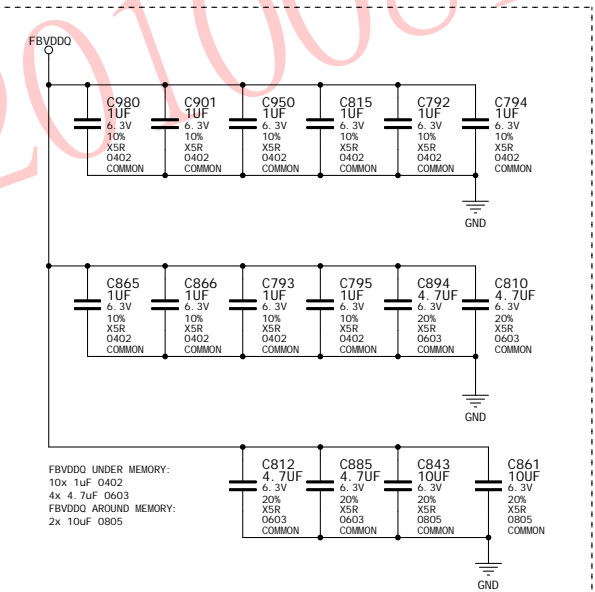
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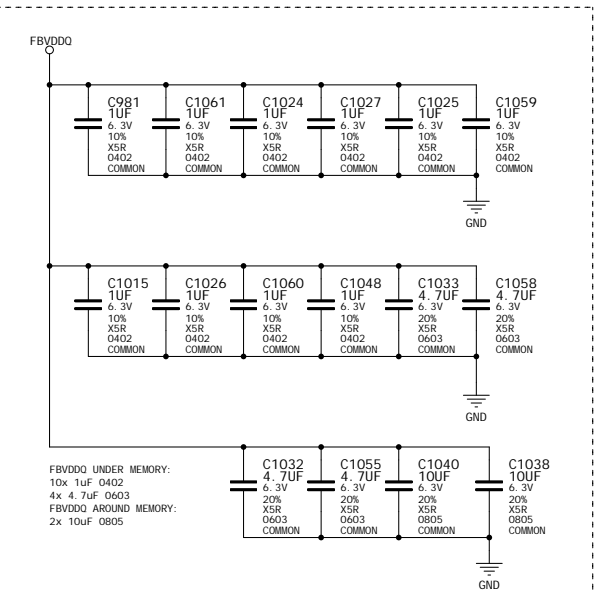
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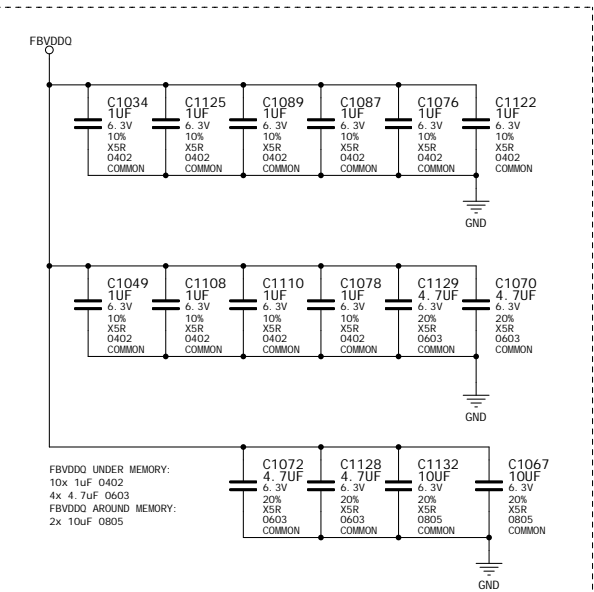
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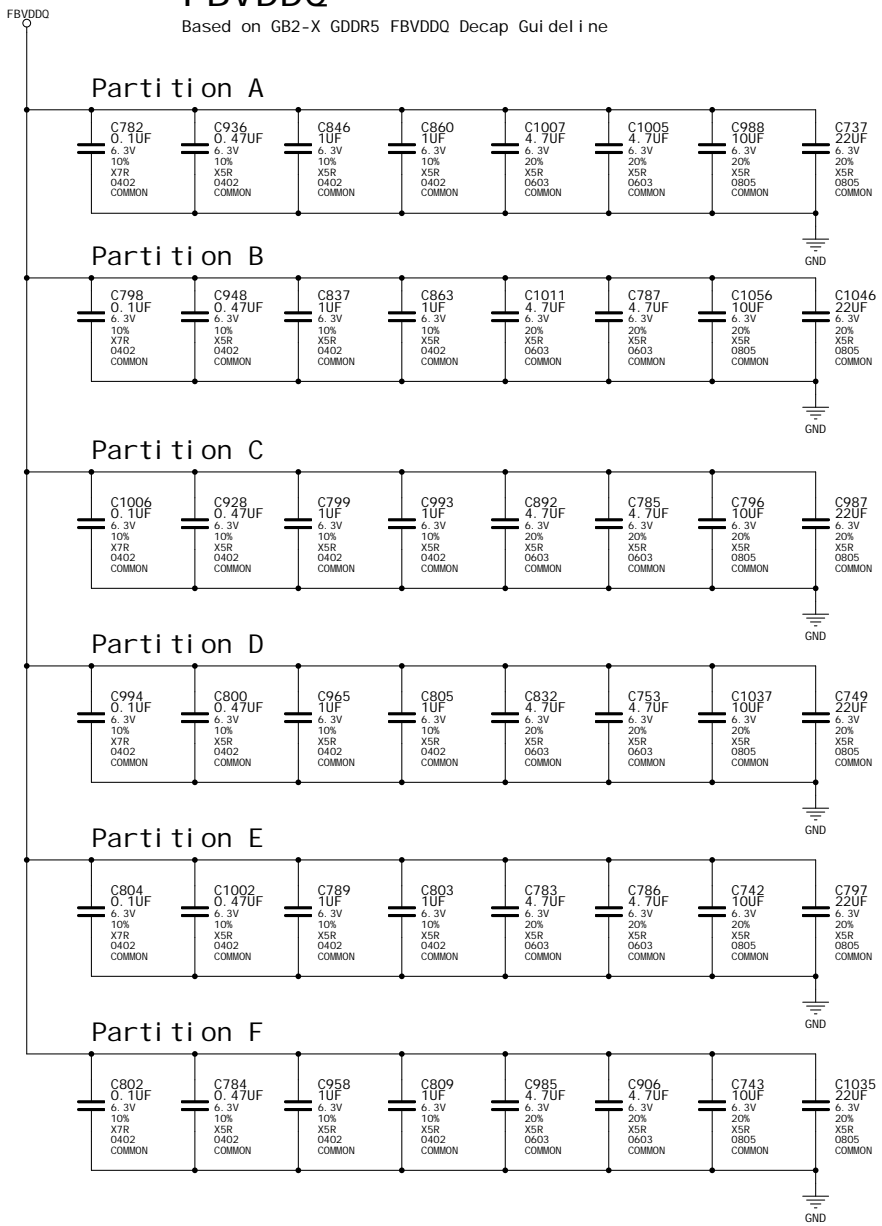


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FBVDDQ

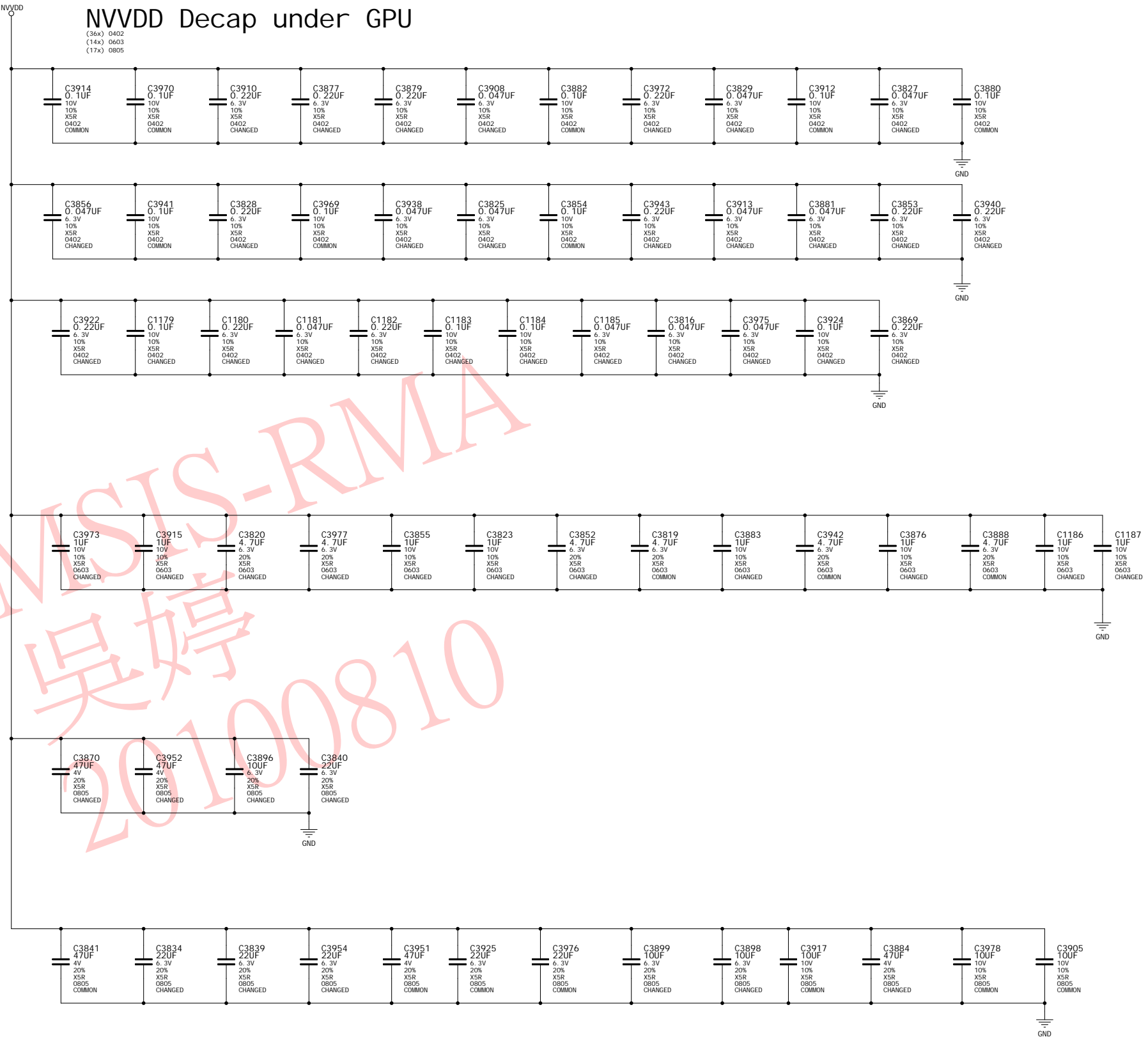
Based on GB2-X GDDR5 FBVDDQ Decap Guideline



FBVDDQ under GPU  
0.1uF 0402 X7R x6  
0.47uF 0402 X5R x6  
1uF 0402 X5R x12  
FBVDDQ around GPU  
4.7uF 0603 X5R x12  
10uF 0805 X5R x6  
22uF 0805 X5R x6

NVVDD Decap under GPU

(36x) 0402  
(14x) 0603  
(17x) 0805



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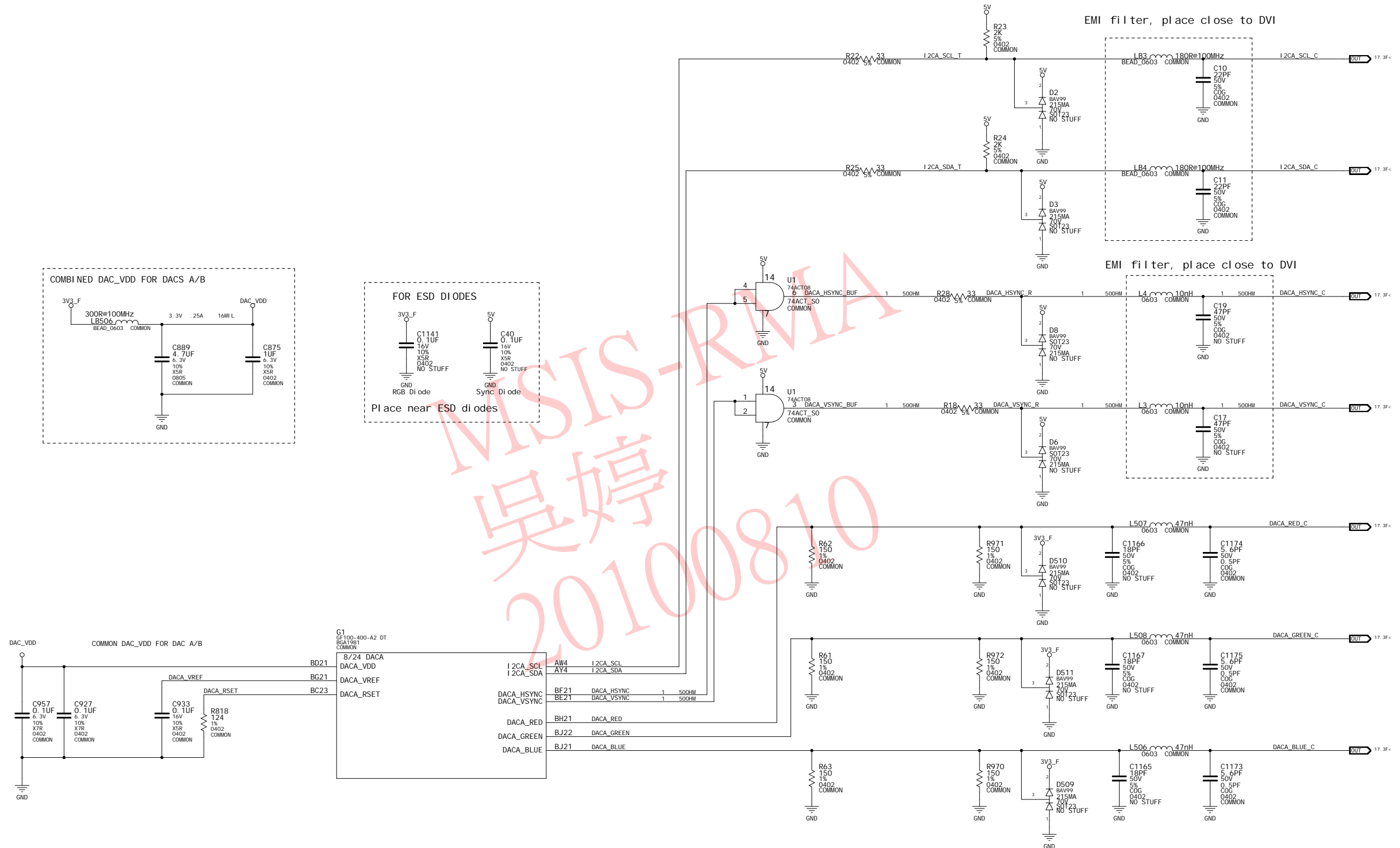
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PAGE DETAIL GPU Decoupling

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PAGE 14 OF 35  
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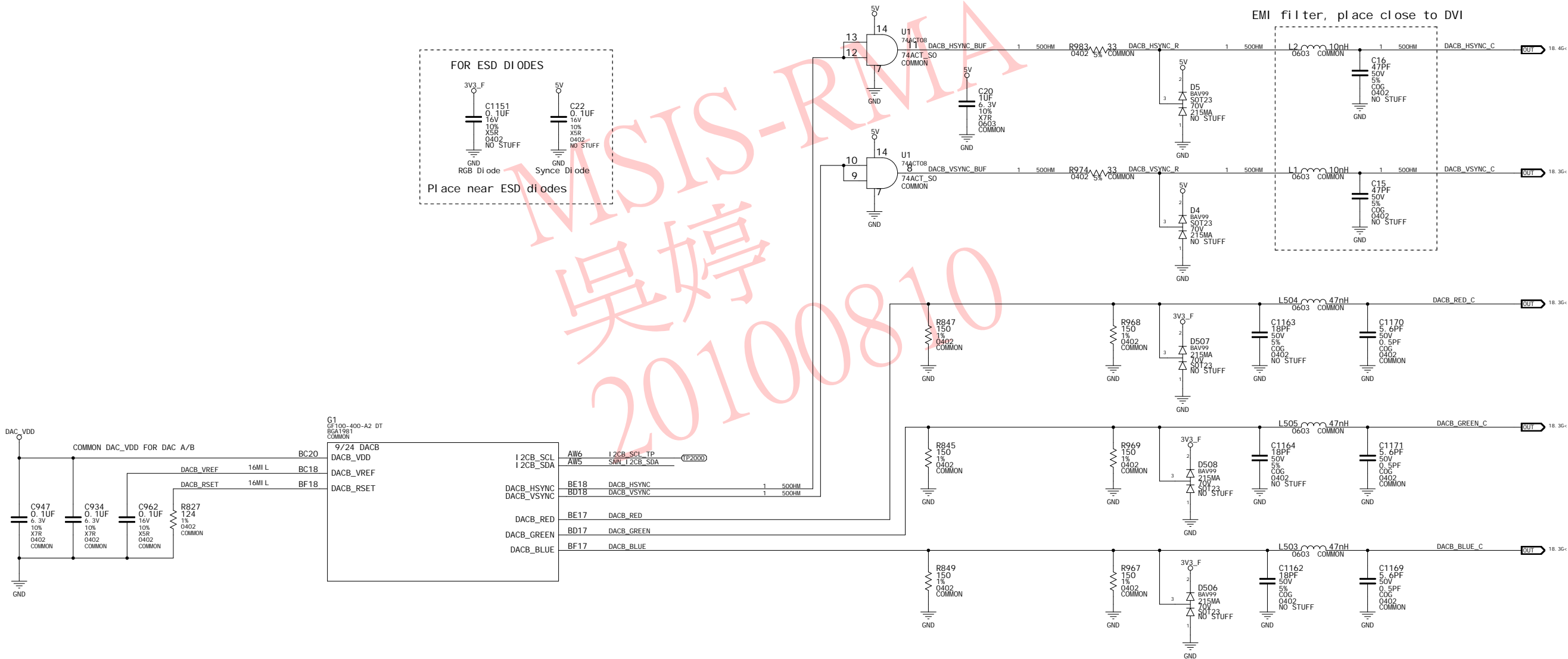
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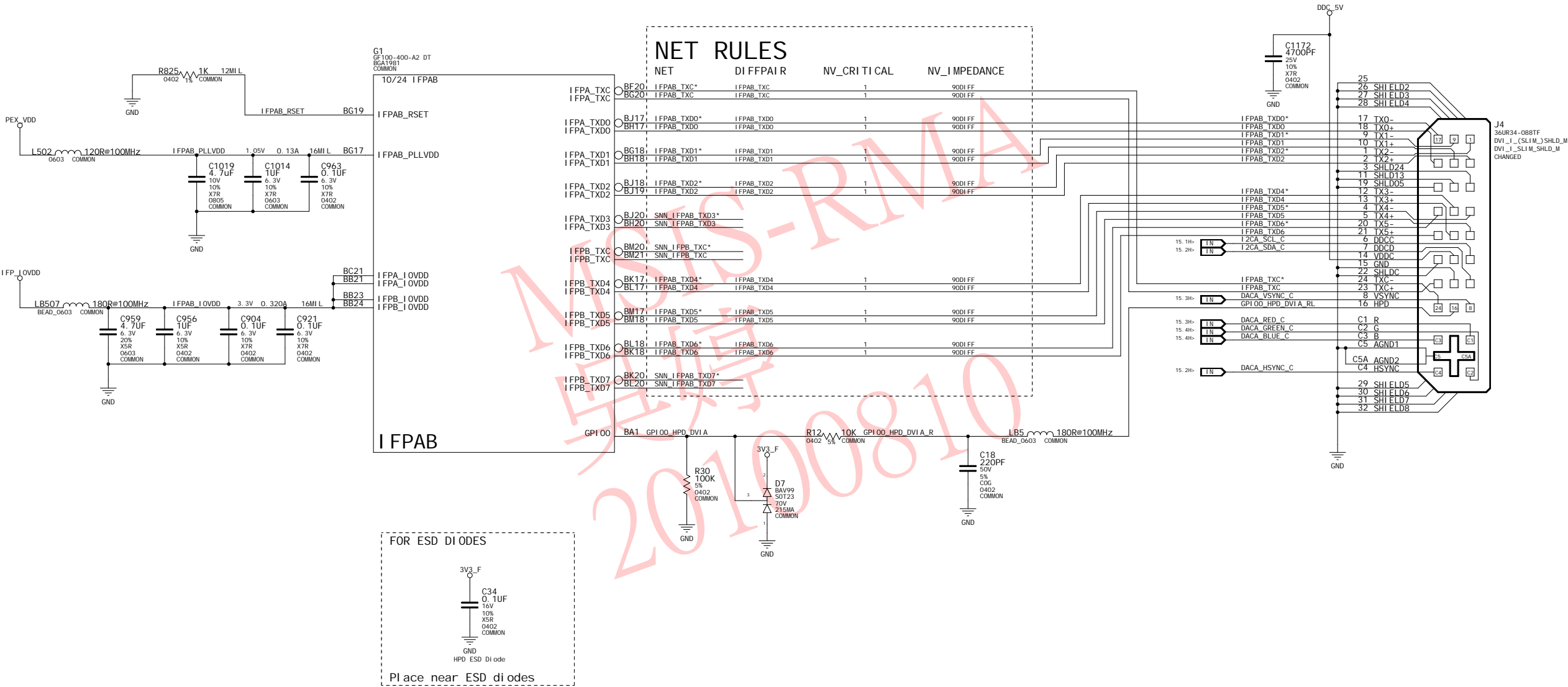
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PAGE DETAIL	DAC_A for South DVI -I

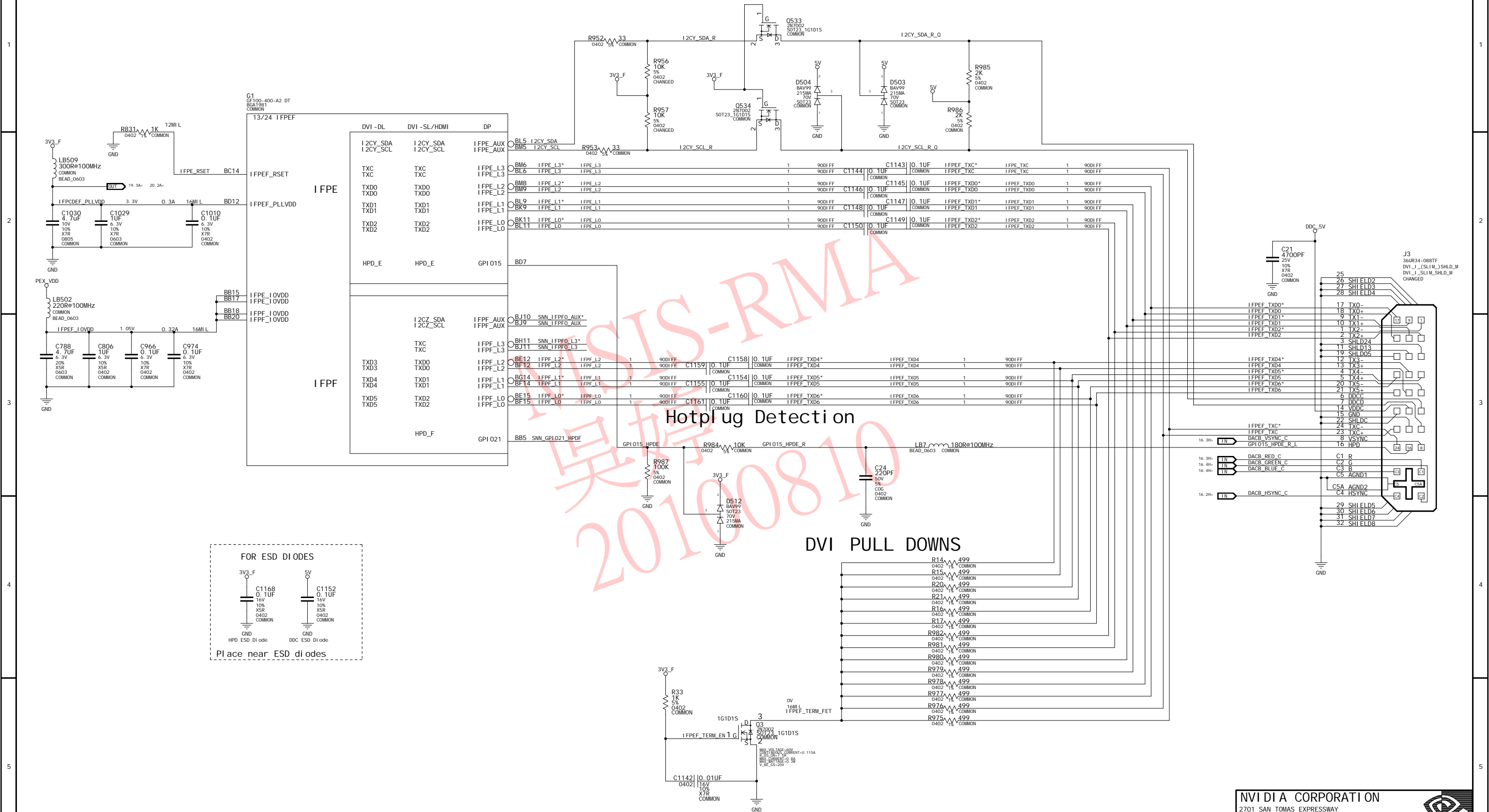
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<b>BOM REV</b>	J	<b>DATE</b>	25-MAR-2010






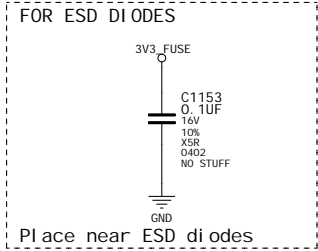




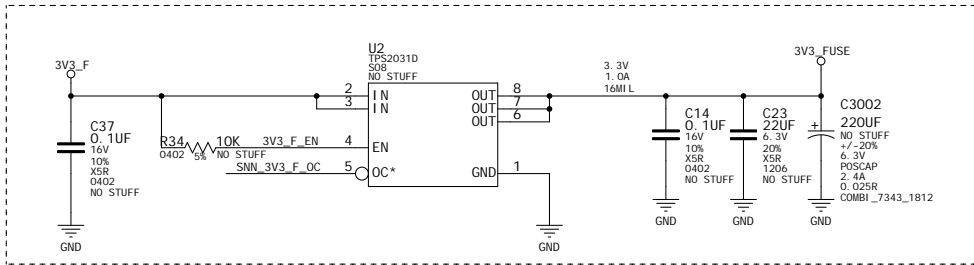
ASSEMBLY	P1022 GF100-400 1536MB GDDR5 32x32M DVI -I +DVI -I +mHDMI
PAGE DETAIL	I/F E/F Interface(Middle DVI)

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## DP Hotplug Detection



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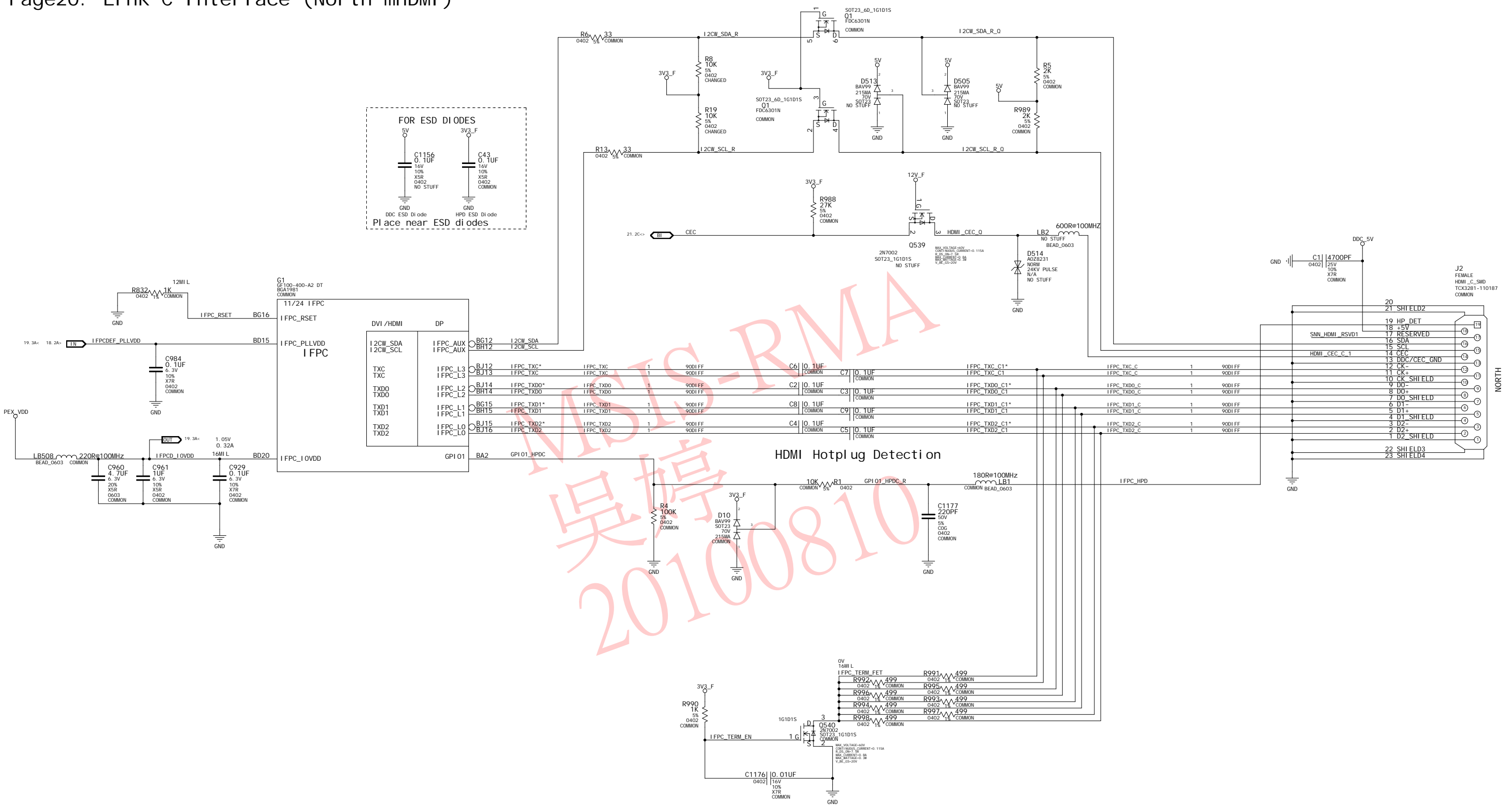
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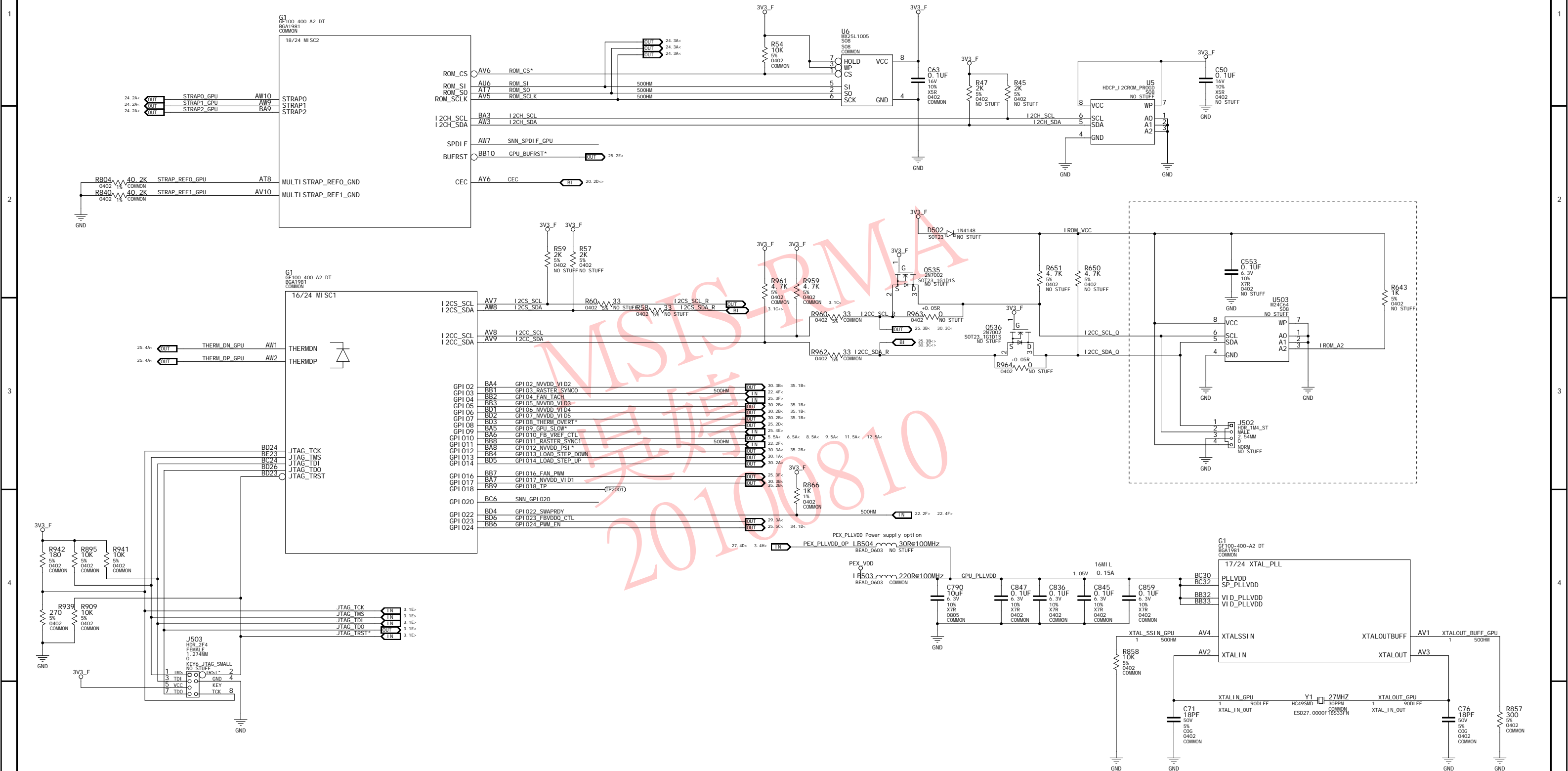
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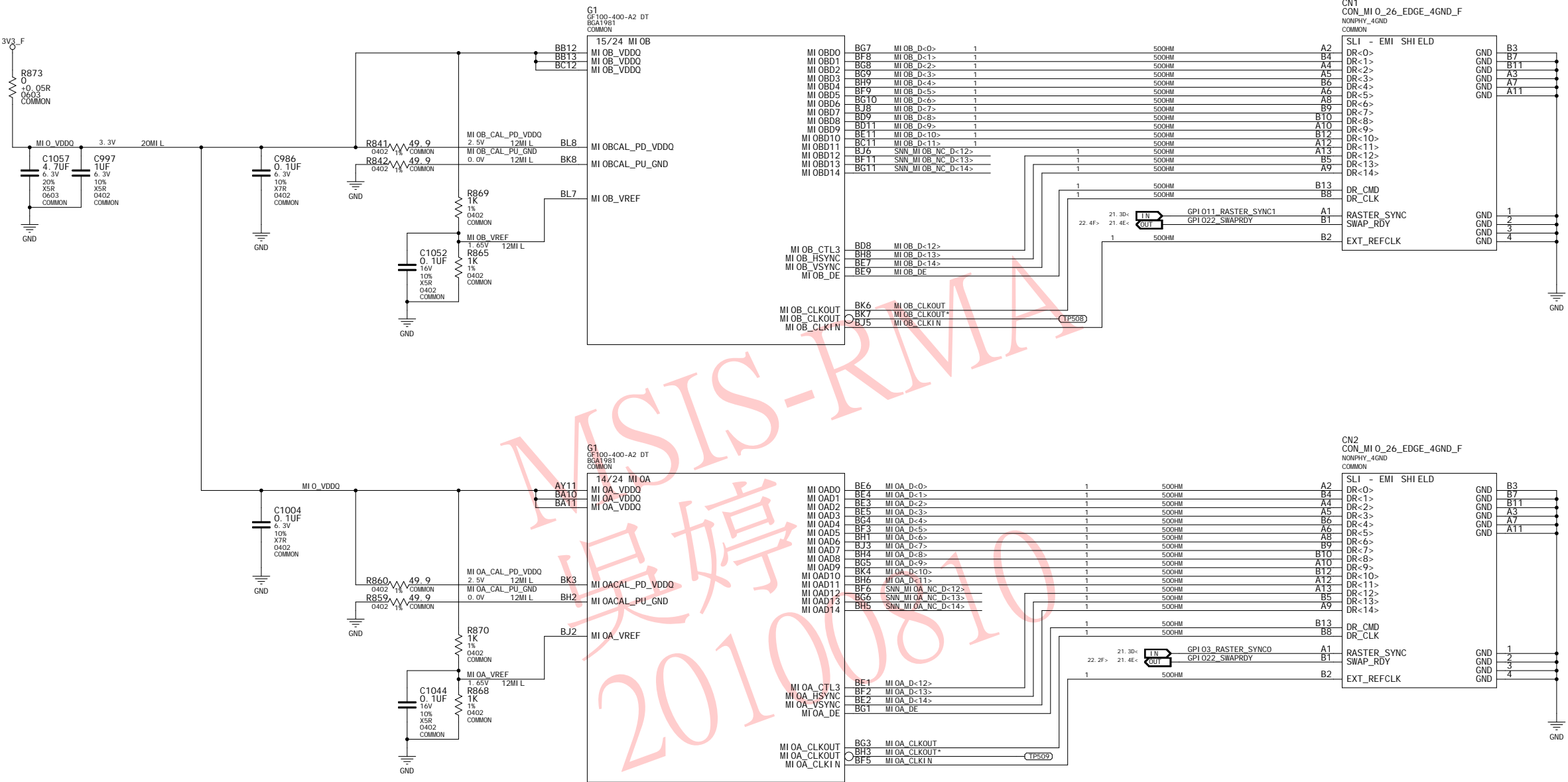




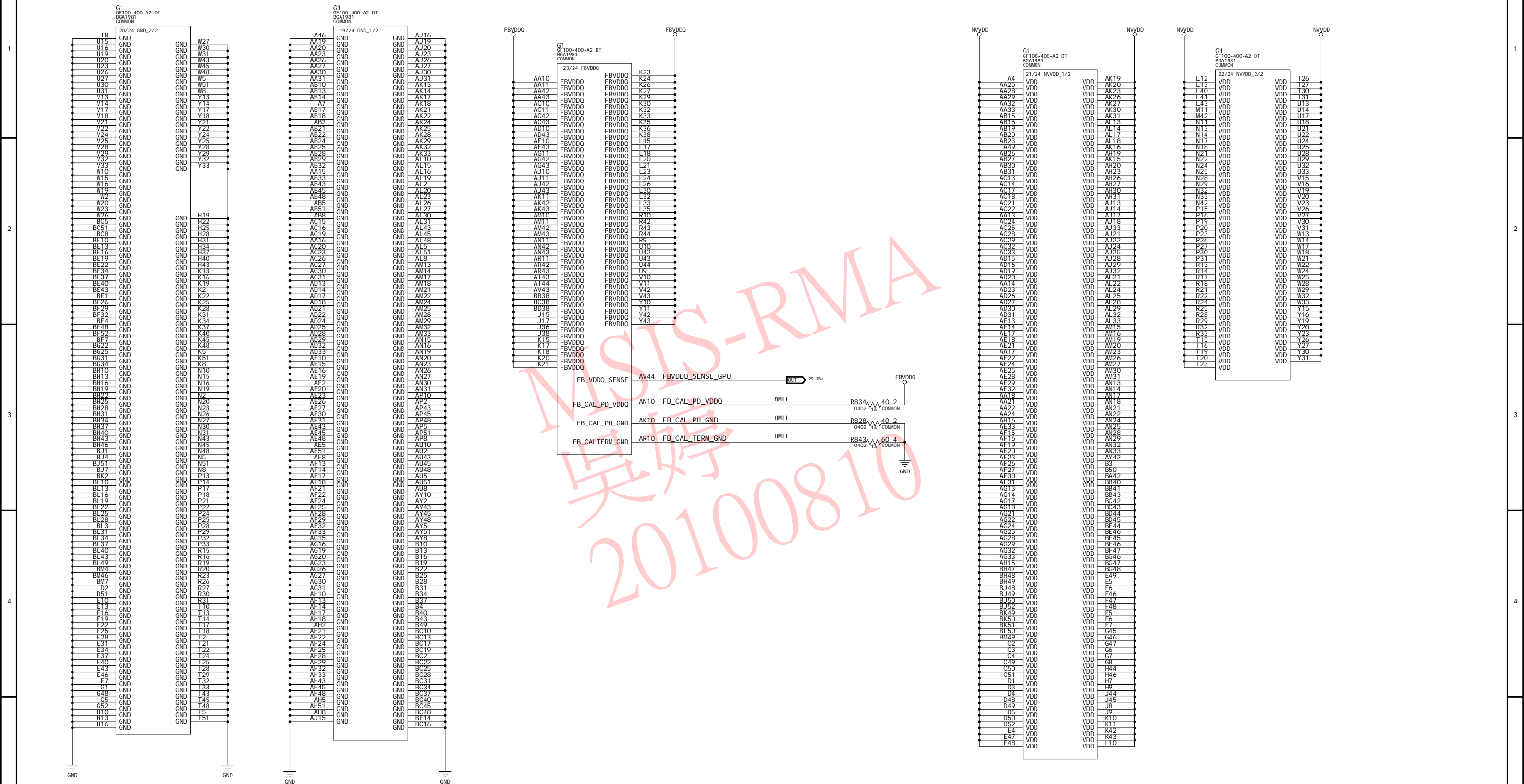
ASSEMBLY	P1022 GF100-400 1536MB GDDR5 32x32M DVI -I +DVI -I +mHDMI
PAGE DETAIL	MISC: GPIO, I2C, ROM, and XTAL

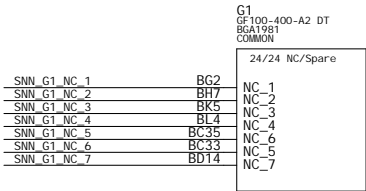
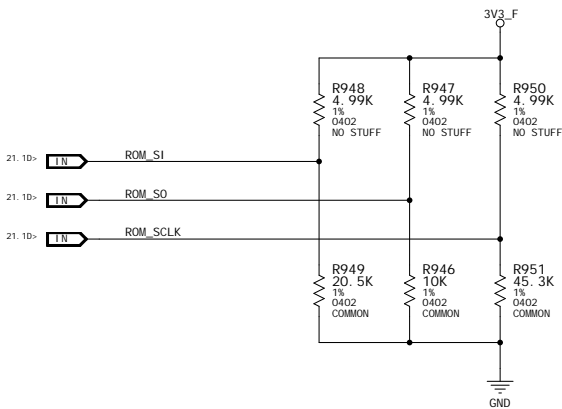
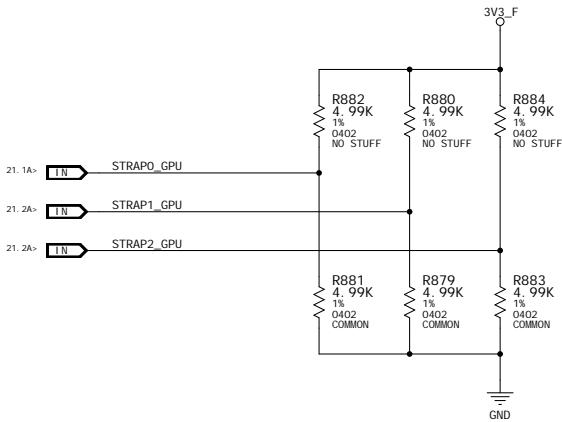
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Page22: Mul ti -use IO(MI O) Interface



## Page23: GPU POWER CONNECTIONS

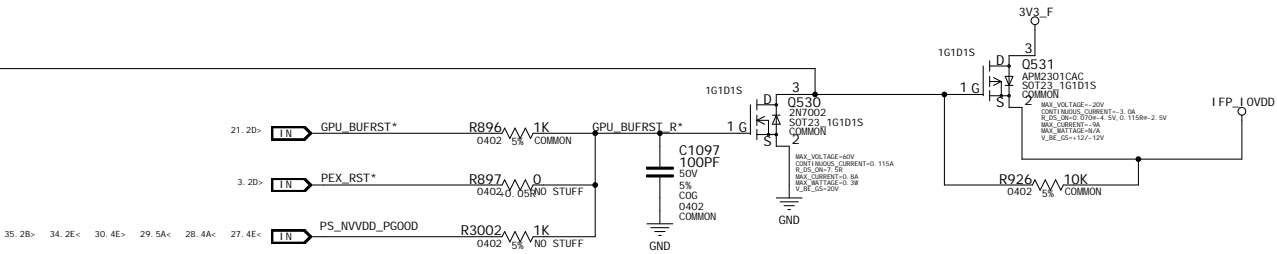
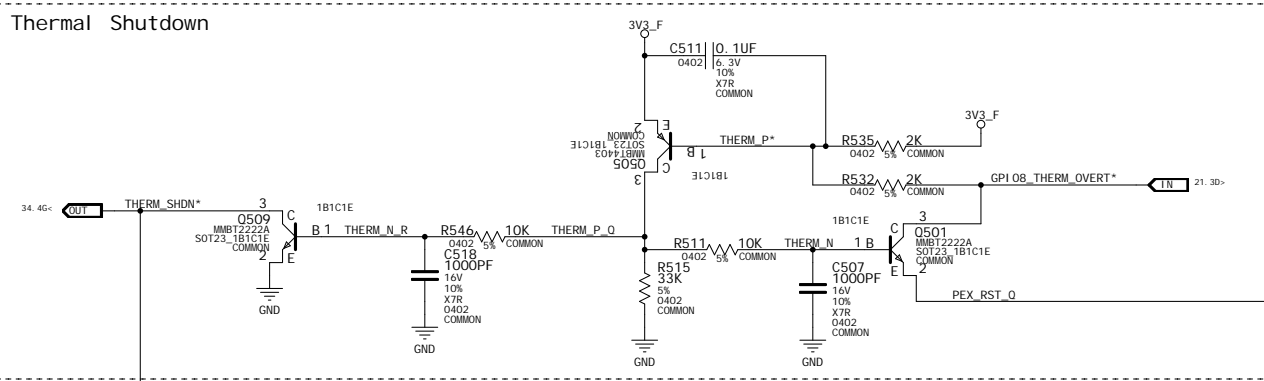




STRAP0	USER_BIT [3..0]	0000: => 5K PD	
STRAP1	3GIO_PADCFG_LUT_ADR	0000 : =>5K PD	0000 Desktop
STRAP2	PCI_DEVID [3:0]	0000 : =>5K PD	For 0x06C0
ROM_SI	RAMCFG[0]		0001 32Mx32 GDDR5 384-bit Qimonda 0010 32Mx32 GDDR5 384-bit Hynix 0011 32Mx32 GDDR5 384-bit Samsung
	RAMCFG[1]		
	RAMCFG[2]		0101 64Mx32 GDDR5 384-bit Qimonda 0110 64Mx32 GDDR5 384-bit Hynix 0011 64Mx32 GDDR5 384-bit Samsung
	RAMCFG[3]		
ROM_SO	VGA_DEVICE	1 FOR GPU0; 0 FOR GPU1	
	SMB_ALT_ADDR	0	10k PD FOR GPU0 5K PD FOR GPU1
	FB[0]_BAR_SIZE	0	
	XCLK_417	0	
ROM_SCLK	PEX_PLL_EN_TERM100	1 ENABLED	
	SLOT_CLK_CFG	1 ENABLE	45K PD
	SUB_VENDOR	1 Dedicated BIOS	
	PCI_DEVID_EXT	0 0xC	

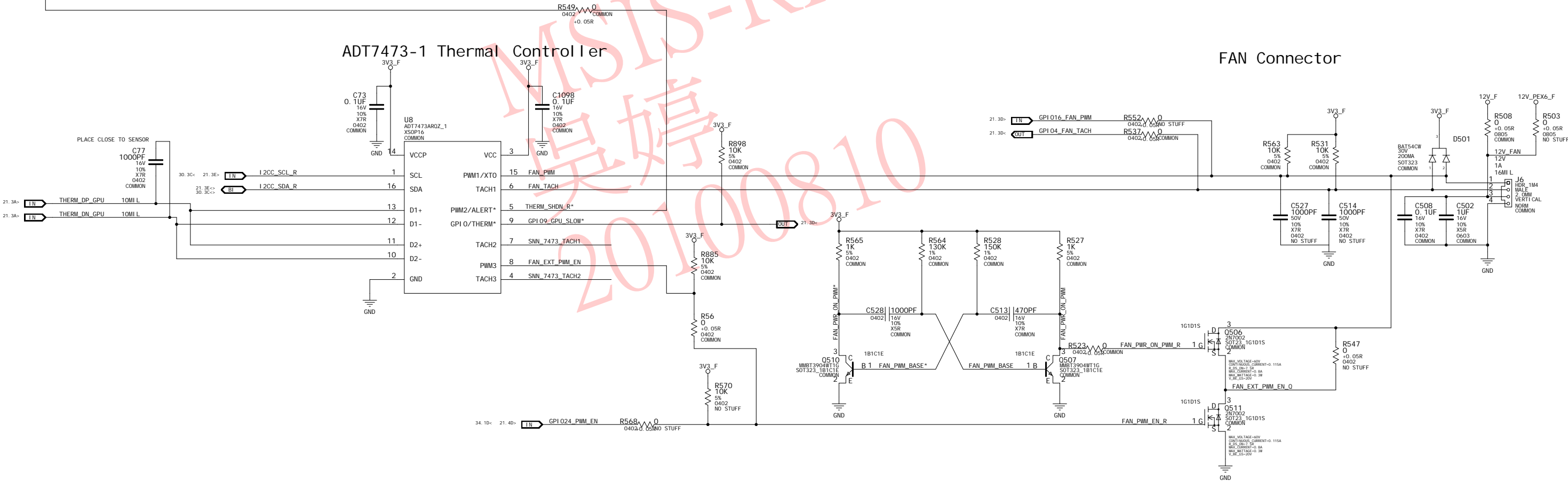
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111





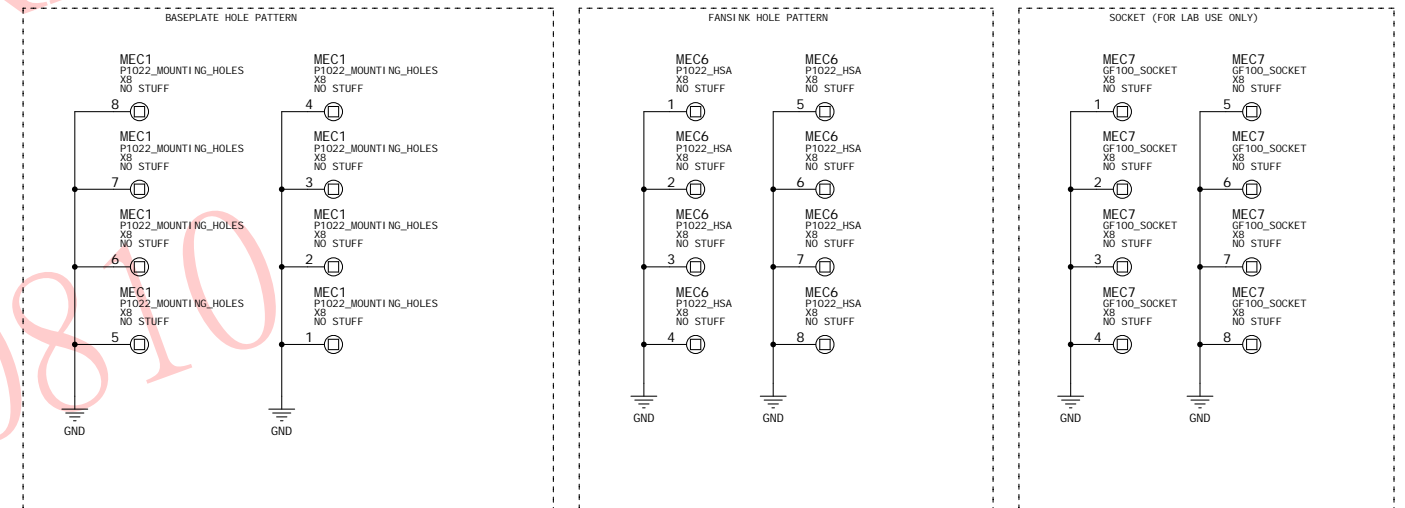
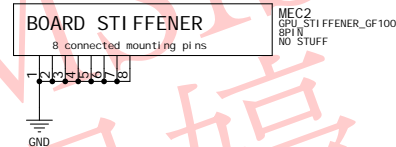
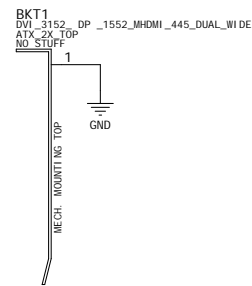
ADT7473-1 Thermal Controller

FAN Connector



Brackets:

151-10001-0352-071 DVI , DVI , mHDMI  
151-10001-0353-071 DVI , DP, mHDMI



ASSEMBLY	P1022 GF100-400 1536MB GDDR5 32x32M DVI -I +DVI -I +mHDMI
PAGE DETAIL	Mechanical

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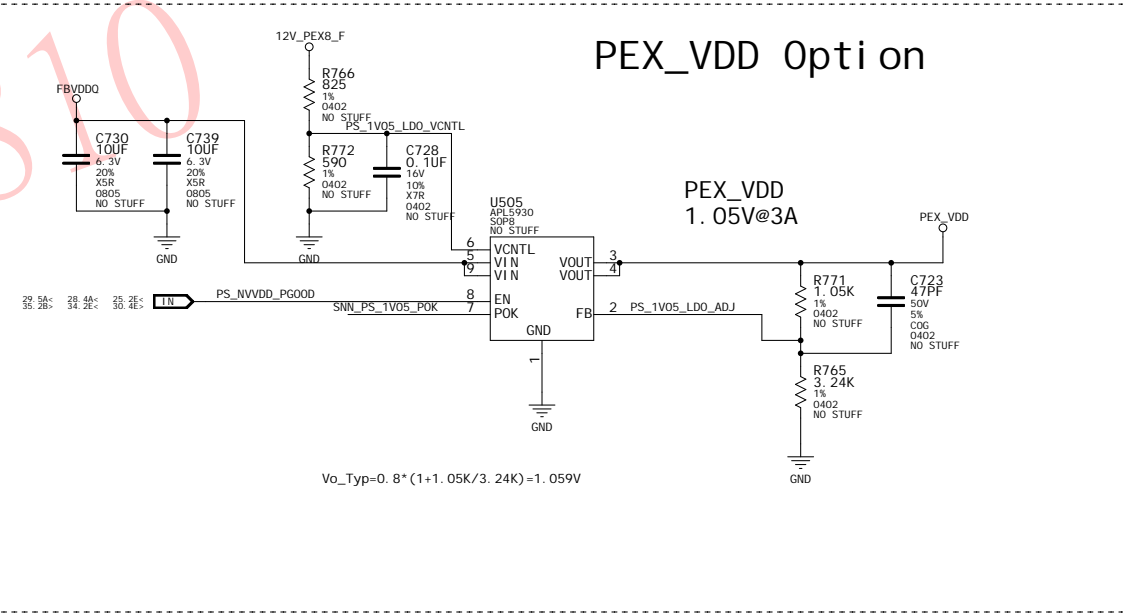
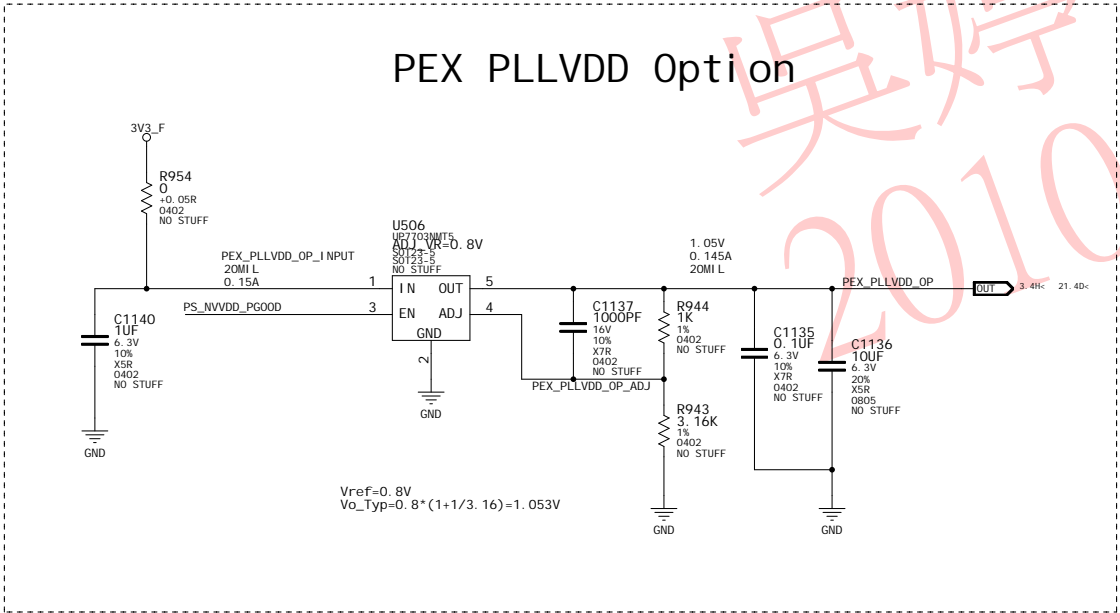
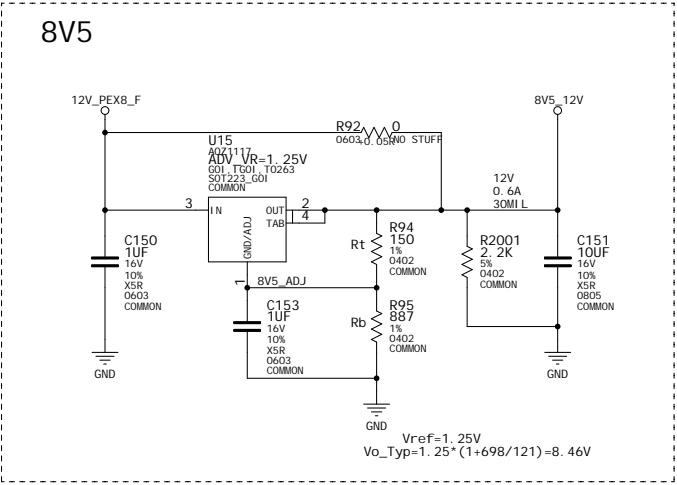
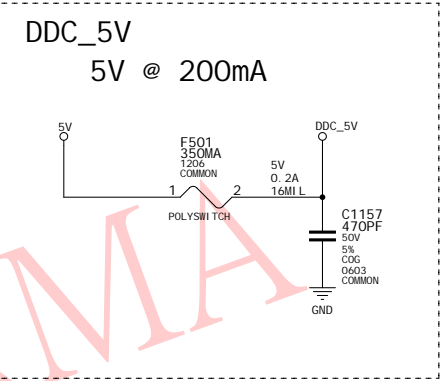
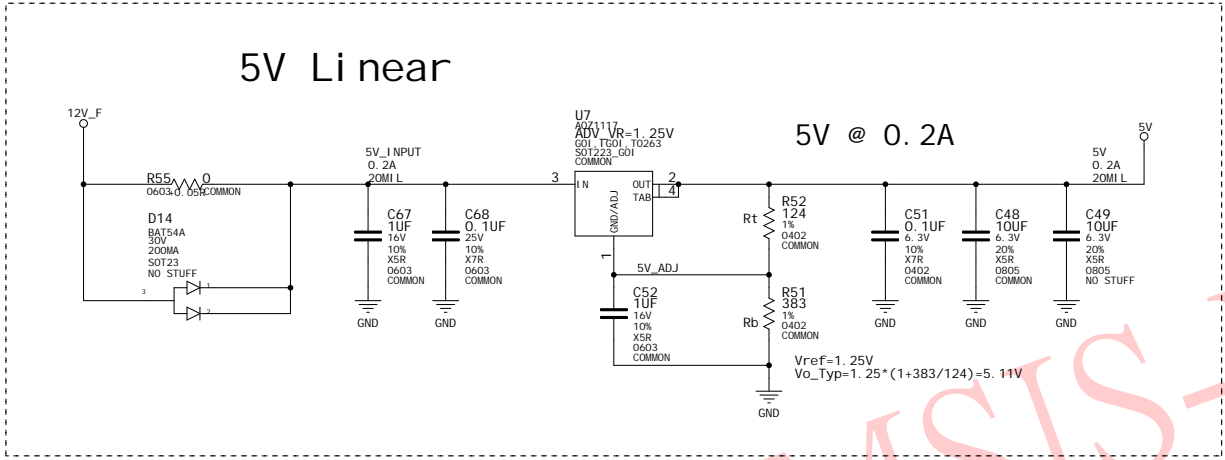
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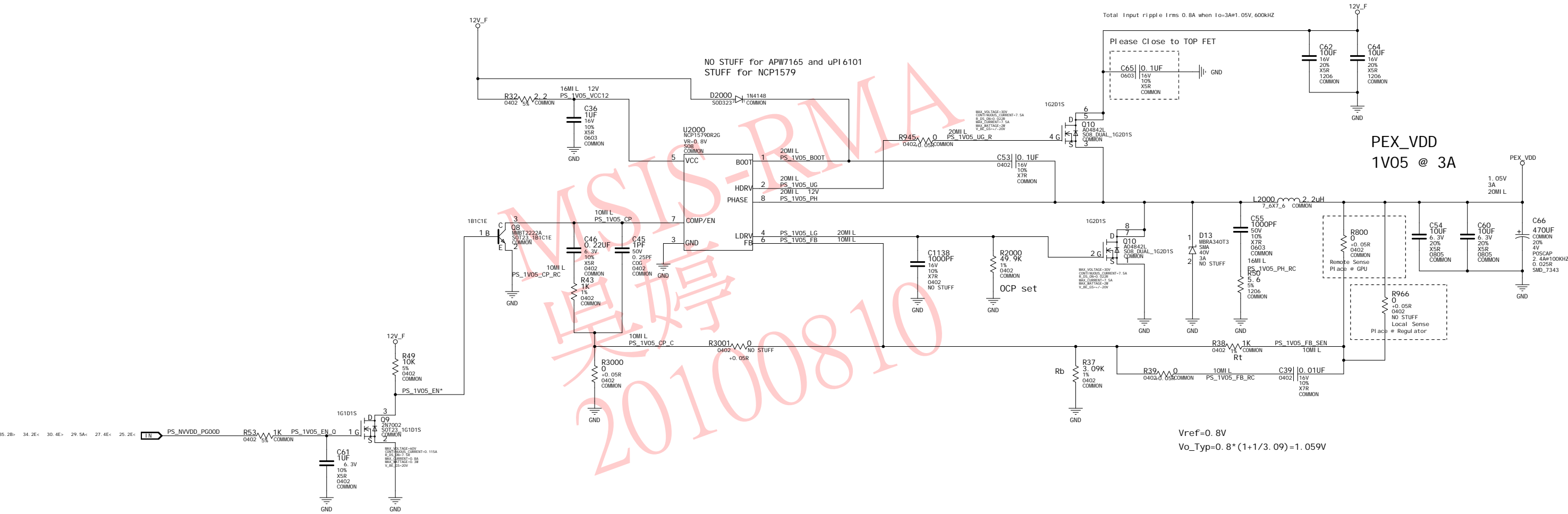
SANTA CLARA, CA 95050, USA



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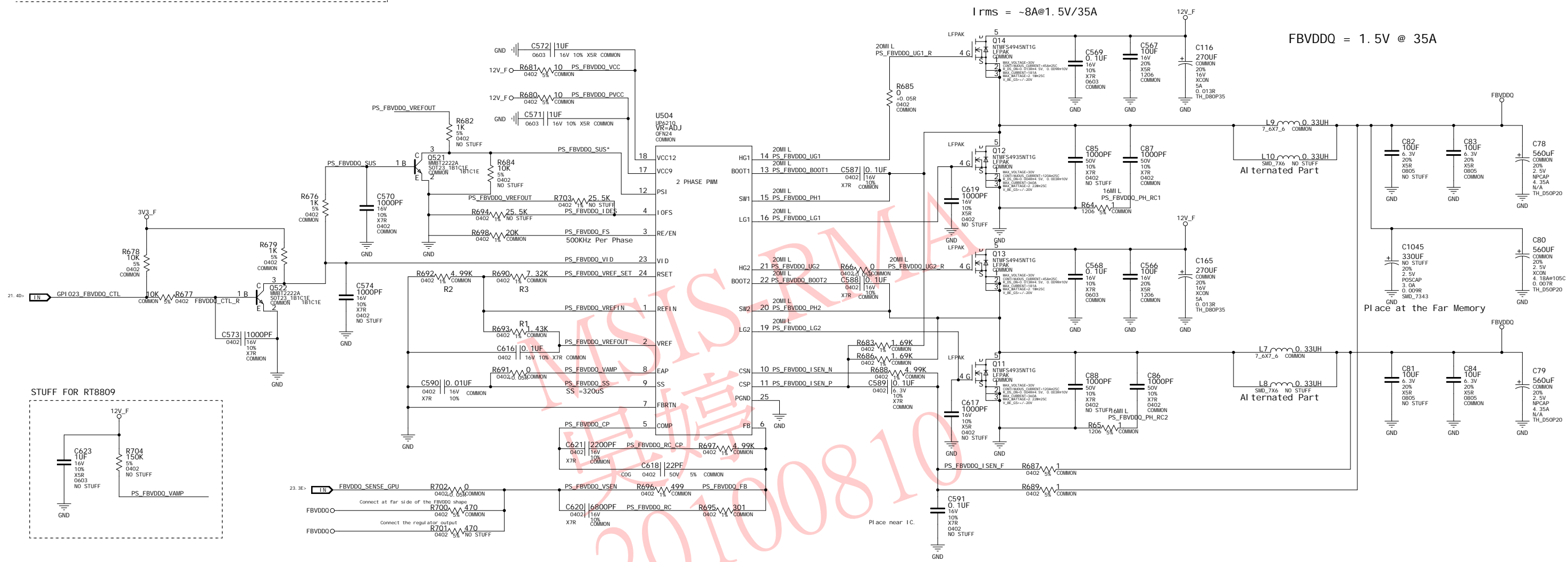
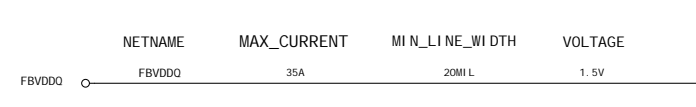
PCB REV	P1022-B00	PAGE	26 OF 35
BOM REV	J	DATE	25-MAR-2010



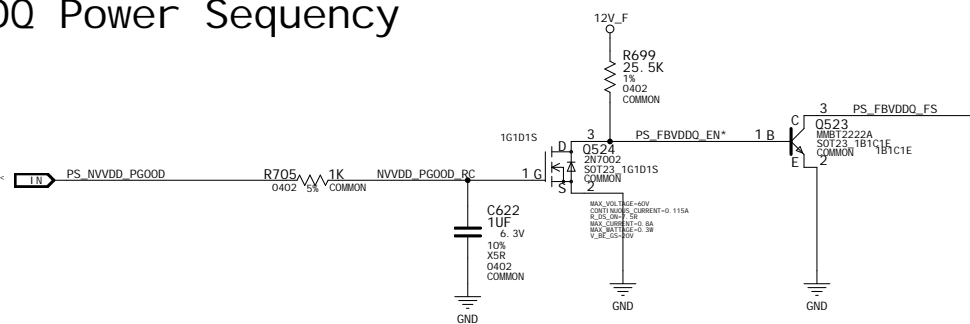


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PCB REV	P1022-B00	PAGE	28 OF 35
BOM REV	J	DATE	25-MAR-2010



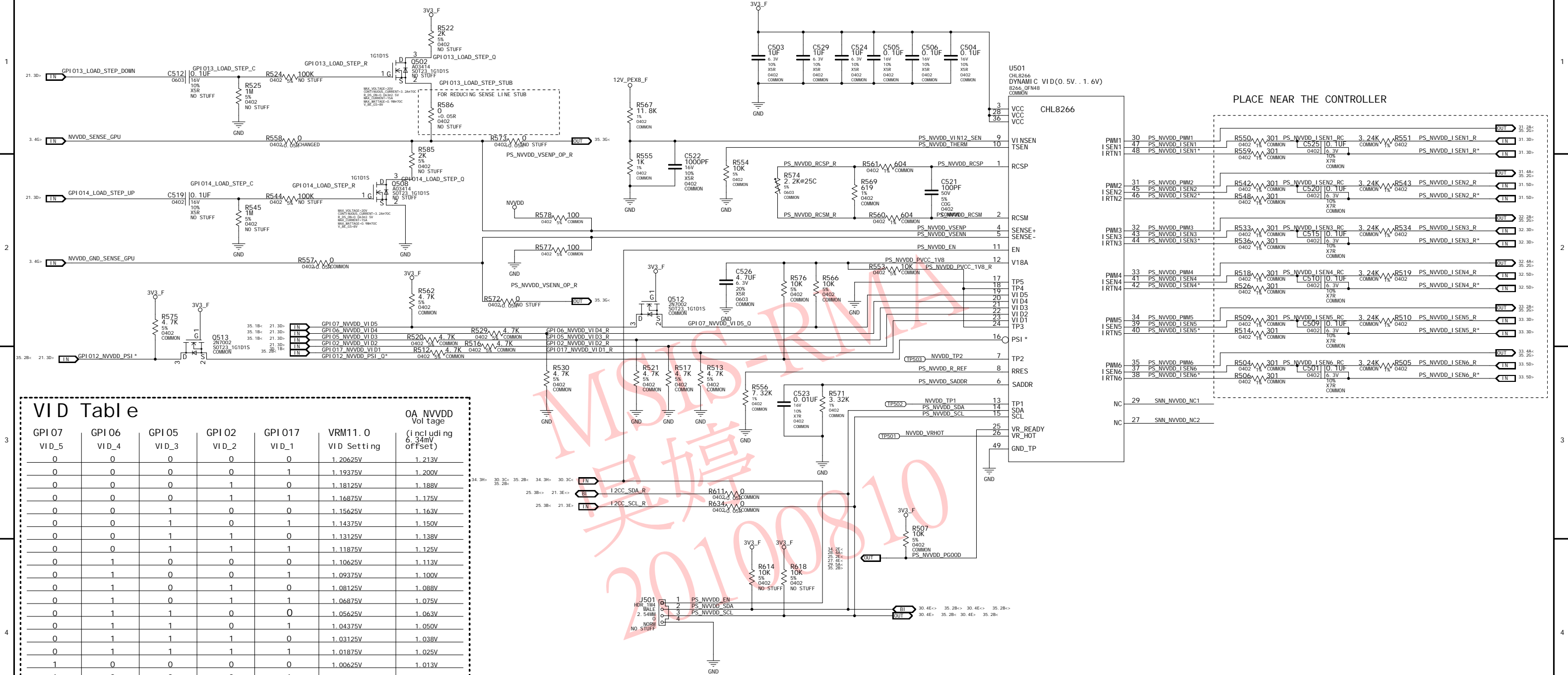
## FBVDDQ Power Sequency



GPI 023	FBVDD0 Vol tage	FBVDD0 Cal cul a tion
0	1.35V (Low perf mode)	$FBVDD0 = 2.0V * (4.99K / (7.32K + [1.43K + (4.99K / 7.32K)])) = 1.354V$
1	1.55V (3D)	$FBVDD0 = 2.0V * 4.99K / (1.43K + 4.99K) = 1.554V$



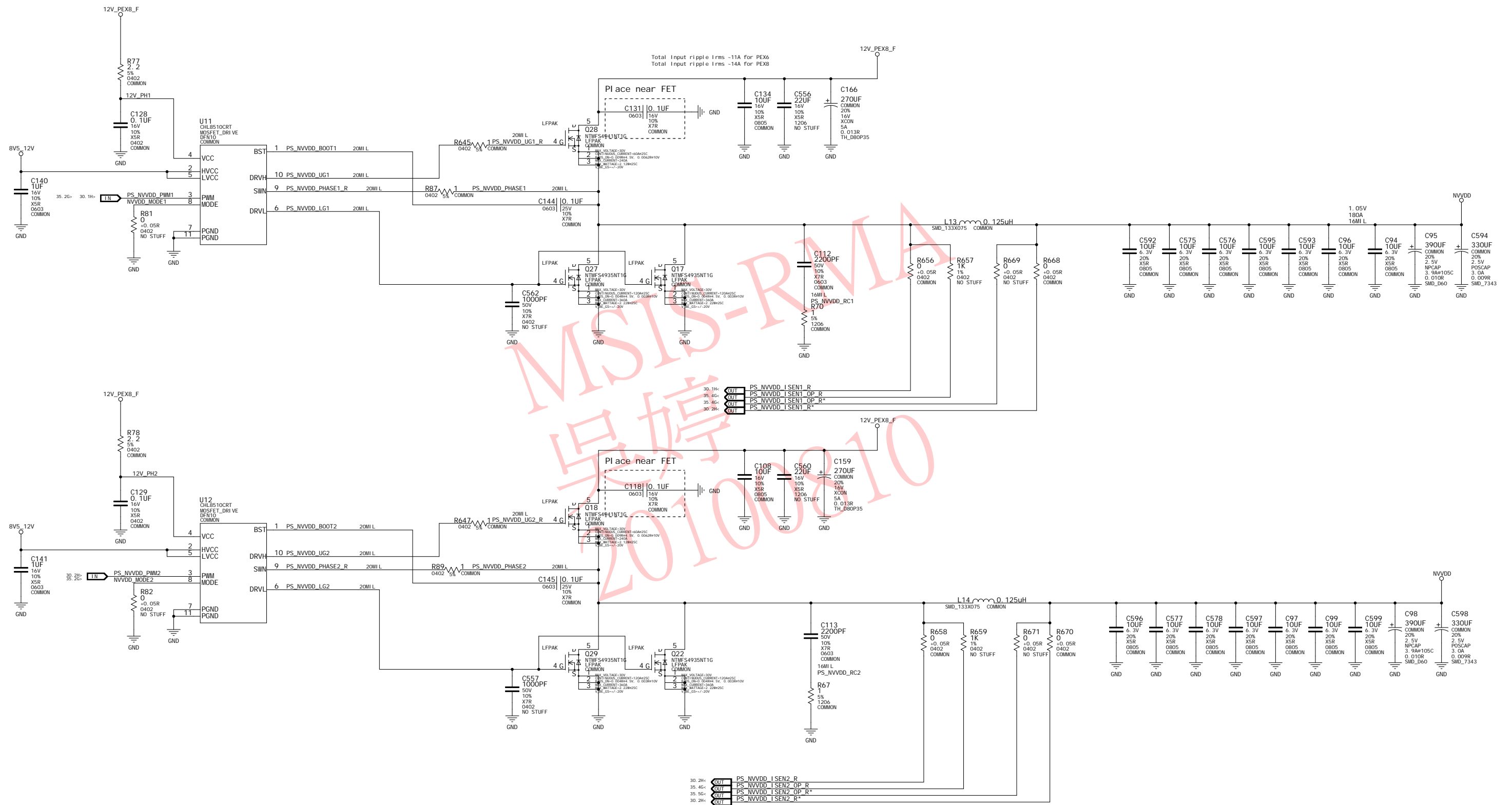
Page30: Power Supply: NVVDD Controller

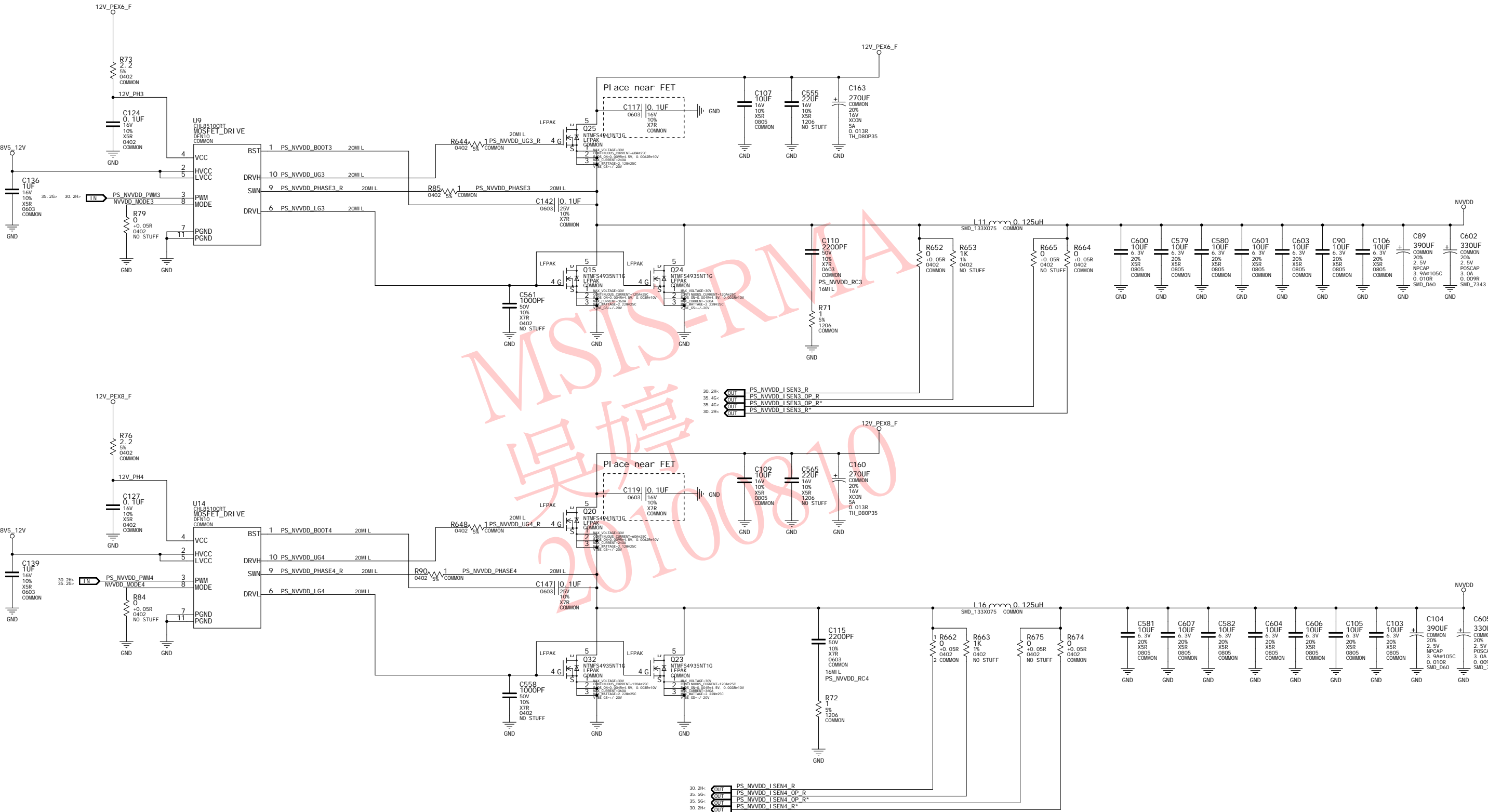


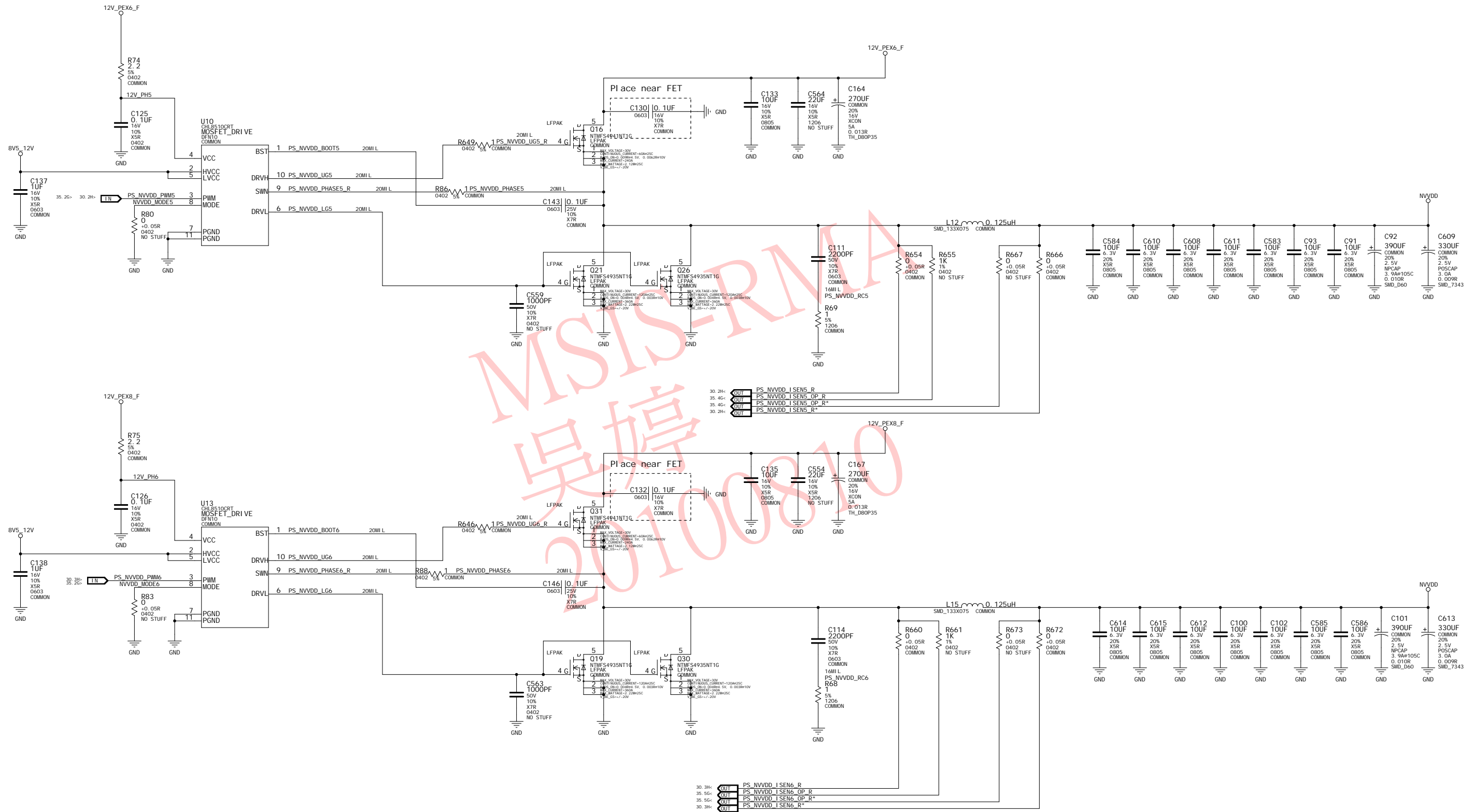
VID Table

GPI 07 VID_5	GPI 06 VID_4	GPI 05 VID_3	GPI 02 VID_2	GPI 017 VID_1	VRM11.0 VID Setting	0A NVVDD Voltage (including 6.34mV offset)
0	0	0	0	0	1.20625V	1.213V
0	0	0	0	1	1.19375V	1.200V
0	0	0	1	0	1.18125V	1.188V
0	0	0	1	1	1.16875V	1.175V
0	0	1	0	0	1.15625V	1.163V
0	0	1	0	1	1.14375V	1.150V
0	0	1	1	0	1.13125V	1.138V
0	0	1	1	1	1.11875V	1.125V
0	1	0	0	0	1.10625V	1.113V
0	1	0	0	1	1.09375V	1.100V
0	1	0	1	0	1.08125V	1.088V
0	1	0	1	1	1.06875V	1.075V
0	1	1	0	0	1.05625V	1.063V
0	1	1	0	1	1.04375V	1.050V
0	1	1	1	0	1.03125V	1.038V
0	1	1	1	1	1.01875V	1.025V
1	0	0	0	0	1.00625V	1.013V
1	0	0	0	1	0.99375V	1.000V
1	0	0	1	0	0.98125V	0.988V
1	0	0	1	1	0.96875V	0.975V
1	0	1	0	0	0.95625V	0.963V
1	0	1	0	1	0.94375V	0.950V
1	0	1	1	0	0.93125V	0.938V
1	0	1	1	1	0.91875V	0.925V
1	1	0	0	0	0.90625V	0.913V
1	1	0	0	1	0.89375V	0.900V
1	1	0	1	0	0.88125V	0.888V
1	1	0	1	1	0.86875V	0.875V
1	1	1	0	0	0.85625V	0.863V
1	1	1	0	1	0.84375V	0.850V
1	1	1	1	0	0.83125V	0.838V
1	1	1	1	1	0.81875V	0.825V

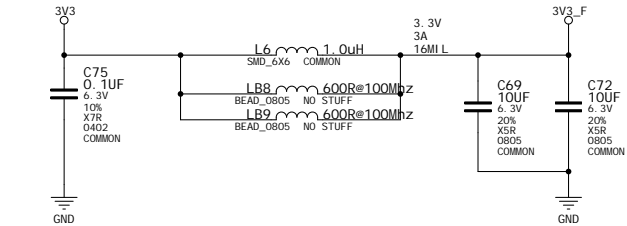
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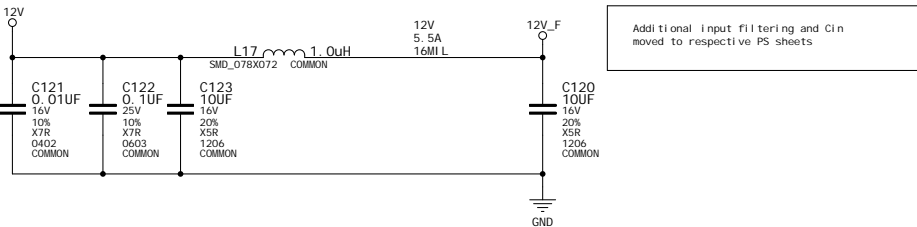




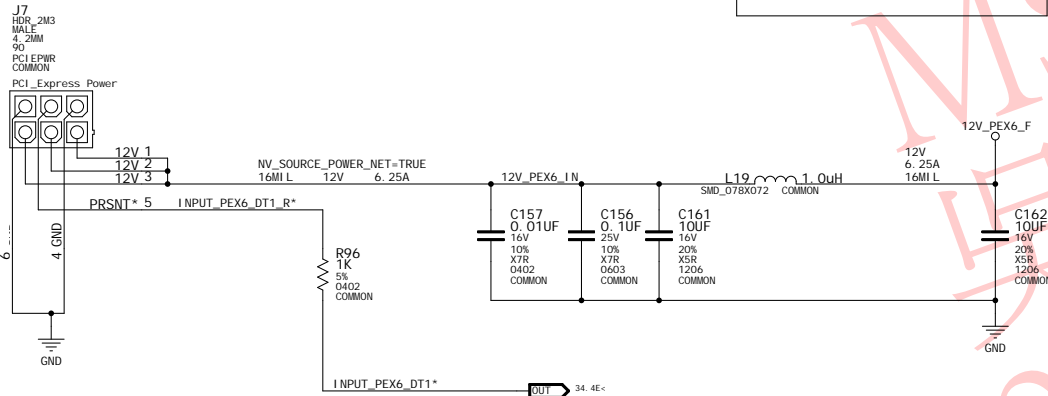
PEX 3V3 INPUT - 10W



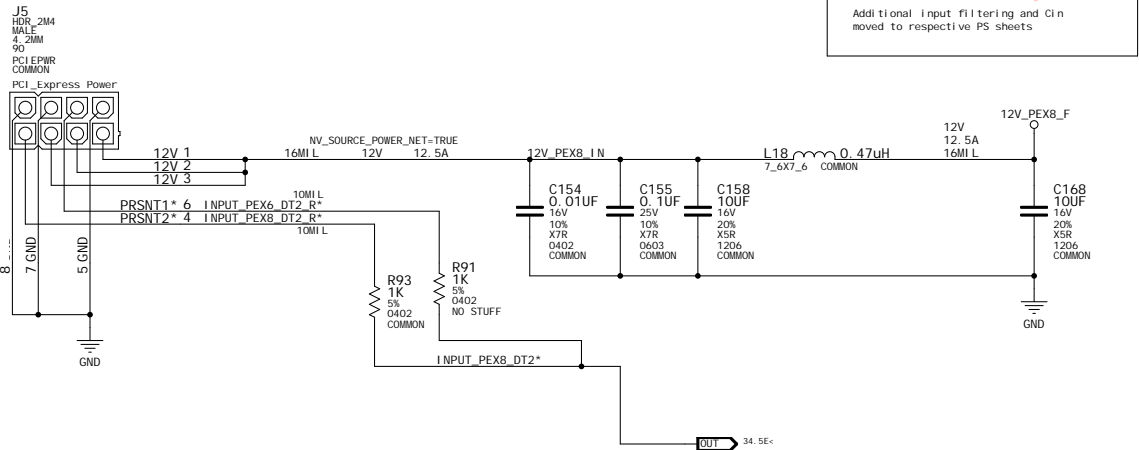
PEX\_12V INPUT - 66W



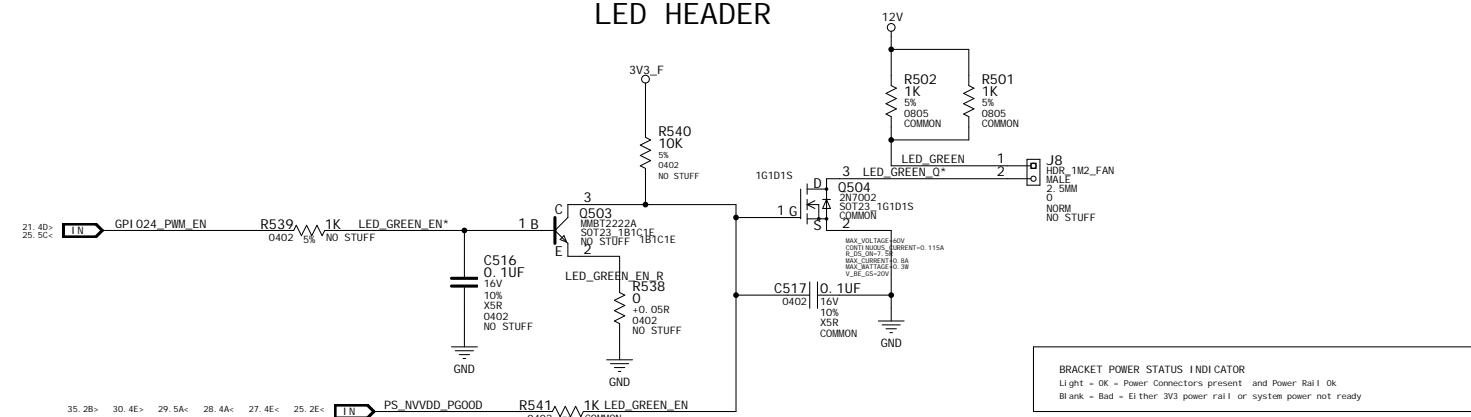
PEX6 INPUT 1 - 2x3 PCIE CON 75W  
MUST BE ATTACHED AND POWERED TO START BOARD



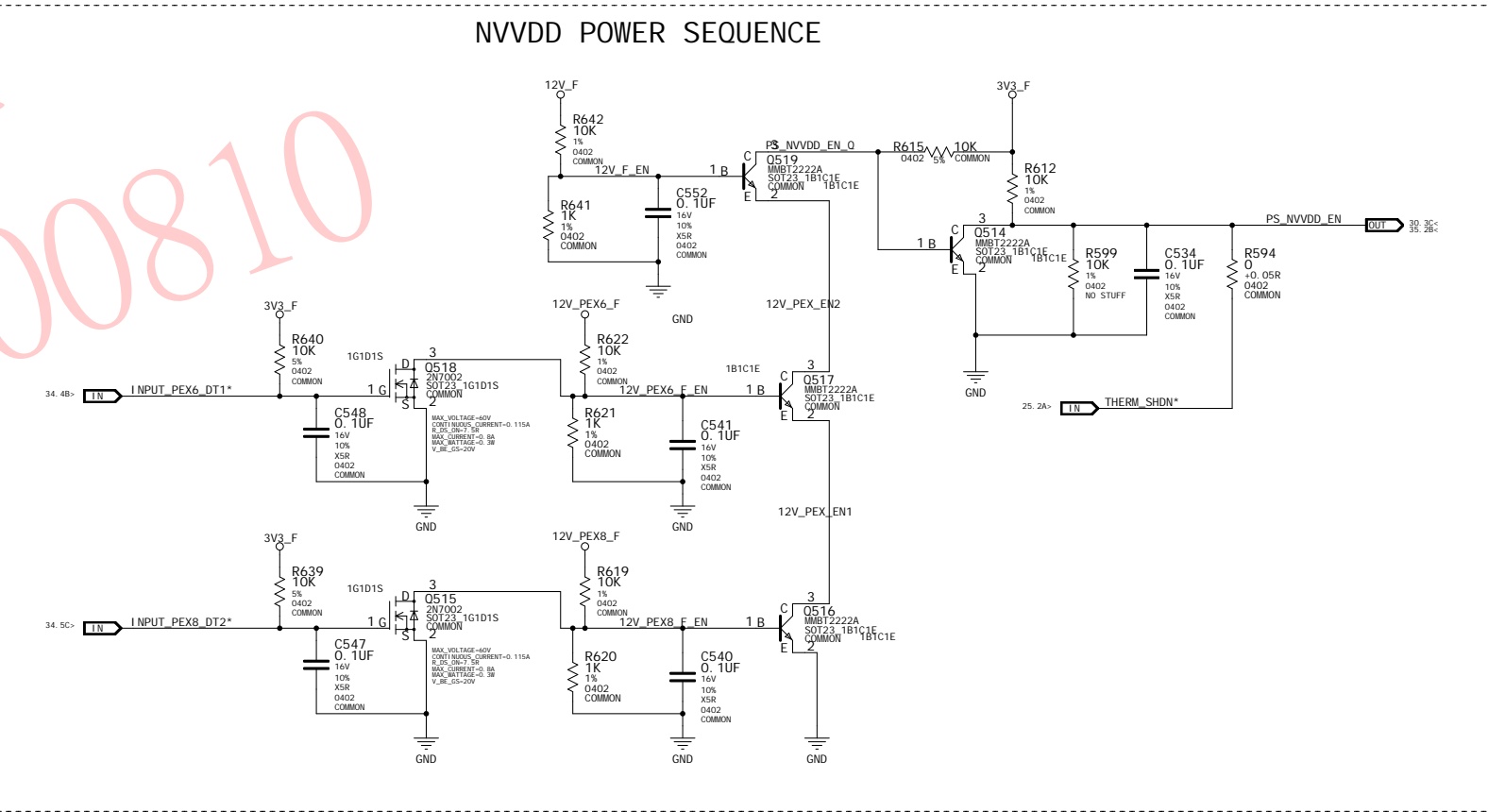
PEX8 INPUT 2 - 2x4 PCIE CON 150W  
MUST BE ATTACHED AND POWERED TO START BOARD



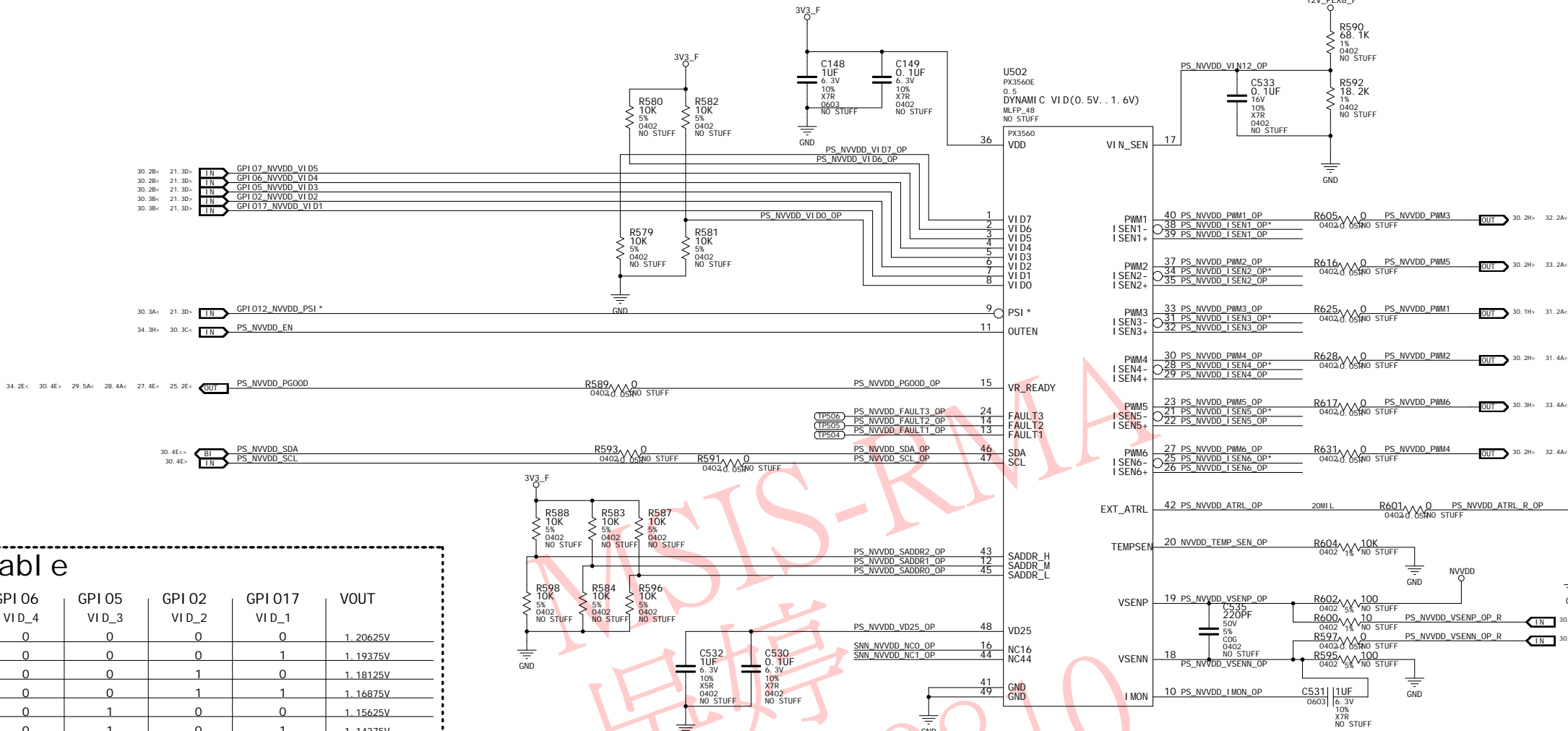
LED HEADER



NVDD POWER SEQUENCE



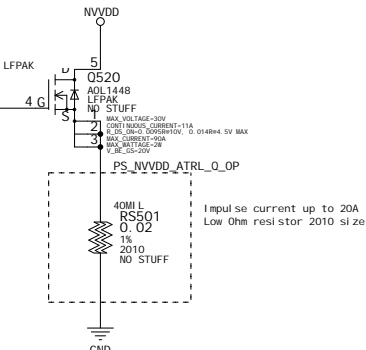




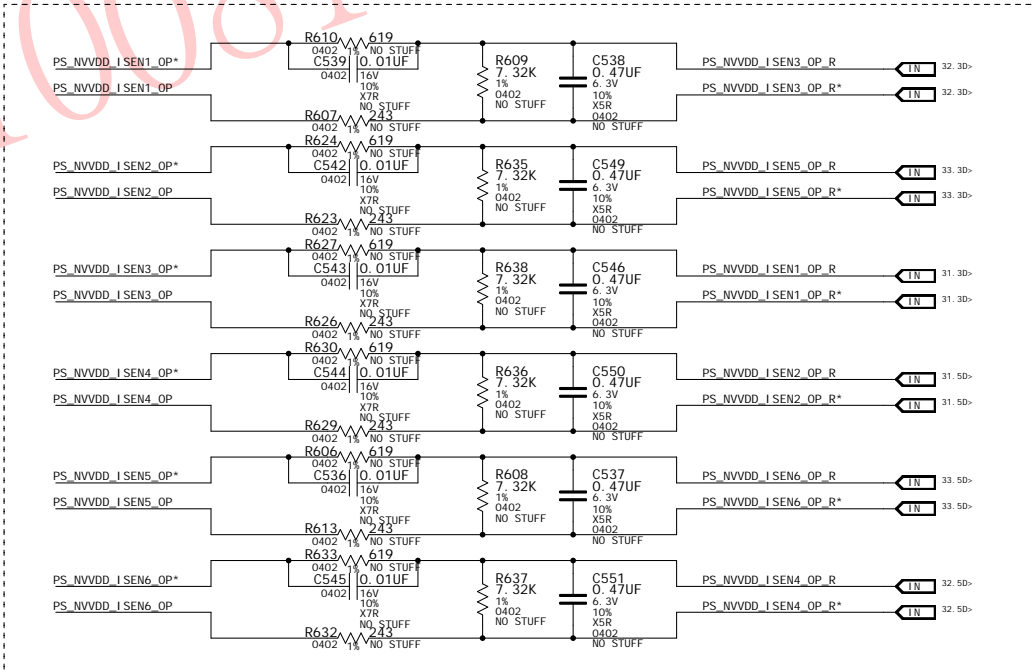
## VI D Table

GPI 07 VID_5	GPI 06 VID_4	GPI 05 VID_3	GPI 02 VID_2	GPI 017 VID_1	VOUT
0	0	0	0	0	1.20625V
0	0	0	0	1	1.19375V
0	0	0	1	0	1.18125V
0	0	0	1	1	1.16875V
0	0	1	0	0	1.15625V
0	0	1	0	1	1.14375V
0	0	1	1	0	1.13125V
0	0	1	1	1	1.11875V
0	1	0	0	0	1.10625V
0	1	0	0	1	1.09375V
0	1	0	1	0	1.08125V
0	1	0	1	1	1.06875V
0	1	1	0	0	1.05625V
0	1	1	0	1	1.04375V
0	1	1	1	0	1.03125V
0	1	1	1	1	1.01875V
1	0	0	0	0	1.00625V
1	0	0	0	1	0.99375V
1	0	0	1	0	0.98125V
1	0	0	1	1	0.96875V
1	0	1	0	0	0.95625V
1	0	1	0	1	0.94375V
1	0	1	1	0	0.93125V
1	0	1	1	1	0.91875V
1	1	0	0	0	0.90625V
1	1	0	0	1	0.89375V
1	1	0	1	0	0.88125V
1	1	0	1	1	0.86875V
1	1	1	0	0	0.85625V
1	1	1	0	1	0.84375V
1	1	1	1	0	0.83125V
1	1	1	1	1	0.81875V

## EXTERNAL ATR CIRCUIT



PLACE FET AT THE POWER SUPPLY OUTPUT



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PCB REV	P1022-B00	PAGE	35 OF 35
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