

P141-A03, NV31/NV34/NV18B  
4(8,16)Mx16, 64(128,256)MB, VIDEO IN/OUT, DVI-I, VGA

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17	POWER SUPPLY: FBVDD, DDC5V

HISTORY:

A00

X00:	INITIAL VERSION
X01:	First Review
	Replaced series resistors in sync lines with 33ohms
	Moved clamping diodes next to GPU
	Added parallel caps to EMI filter DACB
	Removed not needed strap on SAA7114
	Connected RESET and WP of SST ROM to ROMVCC
	Added parallel ROM and Strapps
	Added FBVDD regulator
	Added STEREO glasses circuit
	Removed Decoupling CAPs on VIP VDD, covered by Caps on page 2
	Added ROM_VCC for cleaner planes
	Changed used TMDS lines of IFPA and IFPB to TP from NTP
	Changed Resistor for AGP Vref circuit to 158k
X02:	Final Review
	Added clock termination resistors
	Added net name for FBCALxxx
	Added cap on filter input for FB_DLLVDD, DACA_VDD & DACB_VDD
	Changed netnames for SAA7114 NTPs to NTP_xxx
	Added 1uF cap parallel to fan connector
	Changed all xxCALxx resistors to 50 Ohms
	Changed all FBxDQS*-<x> to NTP_FBxDQS*-<x> with NO_TEST property

A01

X00:	Fixed pin swap on parallel ROM A12 & A13
	Added charge pump for SC2612
	Added resistors to swap GPIO for DACB loadtest
	Added resistors for I2C on internal Video IN connector
X01:	Updated variant information for new Sbom structure

A02

X00:	Added sw adjust for NVVDD
	Exchanged TMDSIOVDD regulator to lower the voltage drop
	Changed TMDSPLLVD regulator bypass to A3V3
	Addrd 1k series resistor in DACB load detection circuit

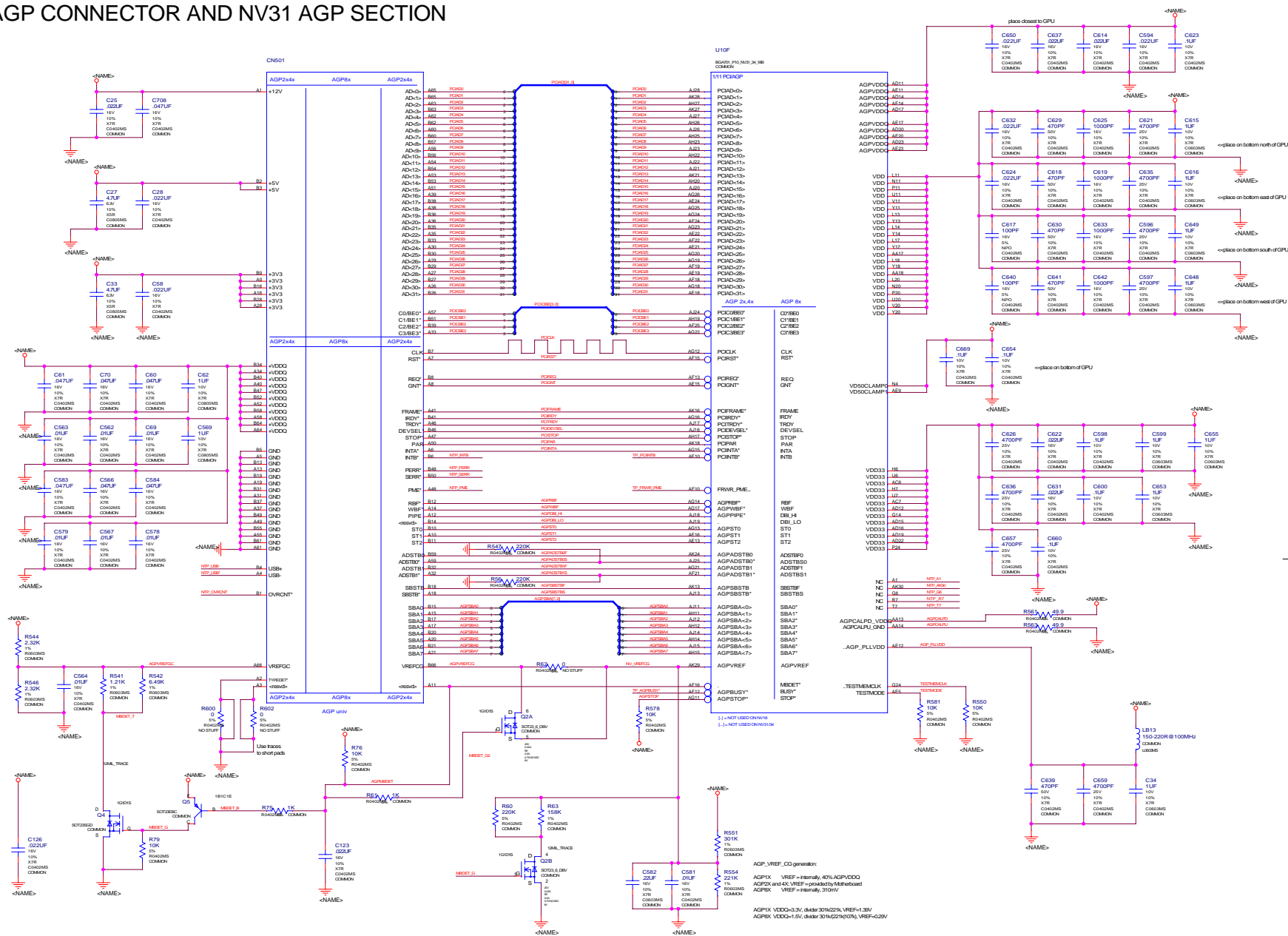
A03

X00:	Removed GPIO5 from NVVDD adjust
	Fixed values for DAC Rset resitors
	Removed Sync Buffer bypass
	Removed 2nd voltage selection fet
	Changed to new internal video connector
	Added snubber to NVVDD and FBVDD regulator

8912 version 210 base on P141-A03 Modify.  
1.Page 13 add 1\*4 pin vedio-in connector.

602-10141-0000-000 Base Schematic

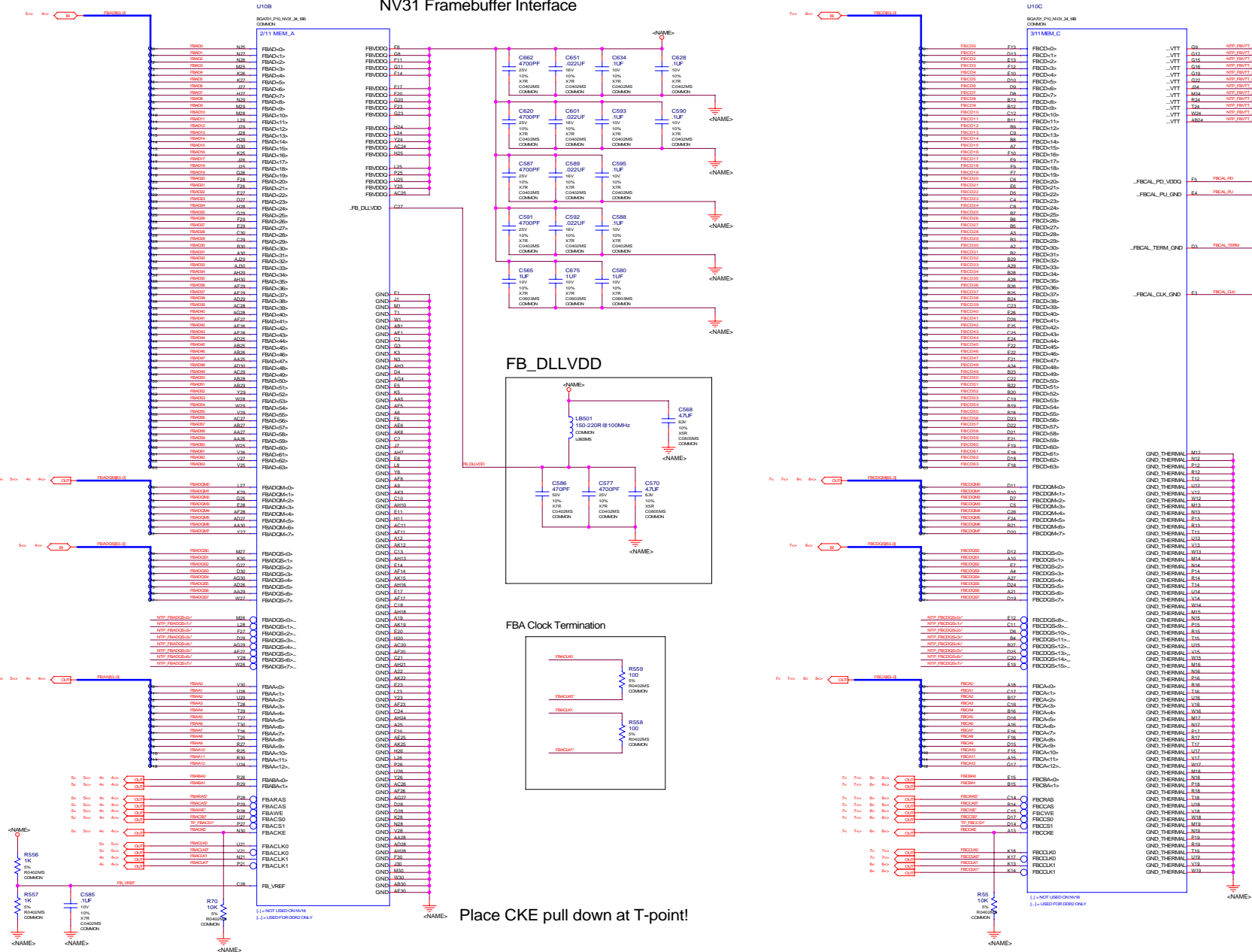
## AGP CONNECTOR AND NV31 AGP SECTION



### AGP rules

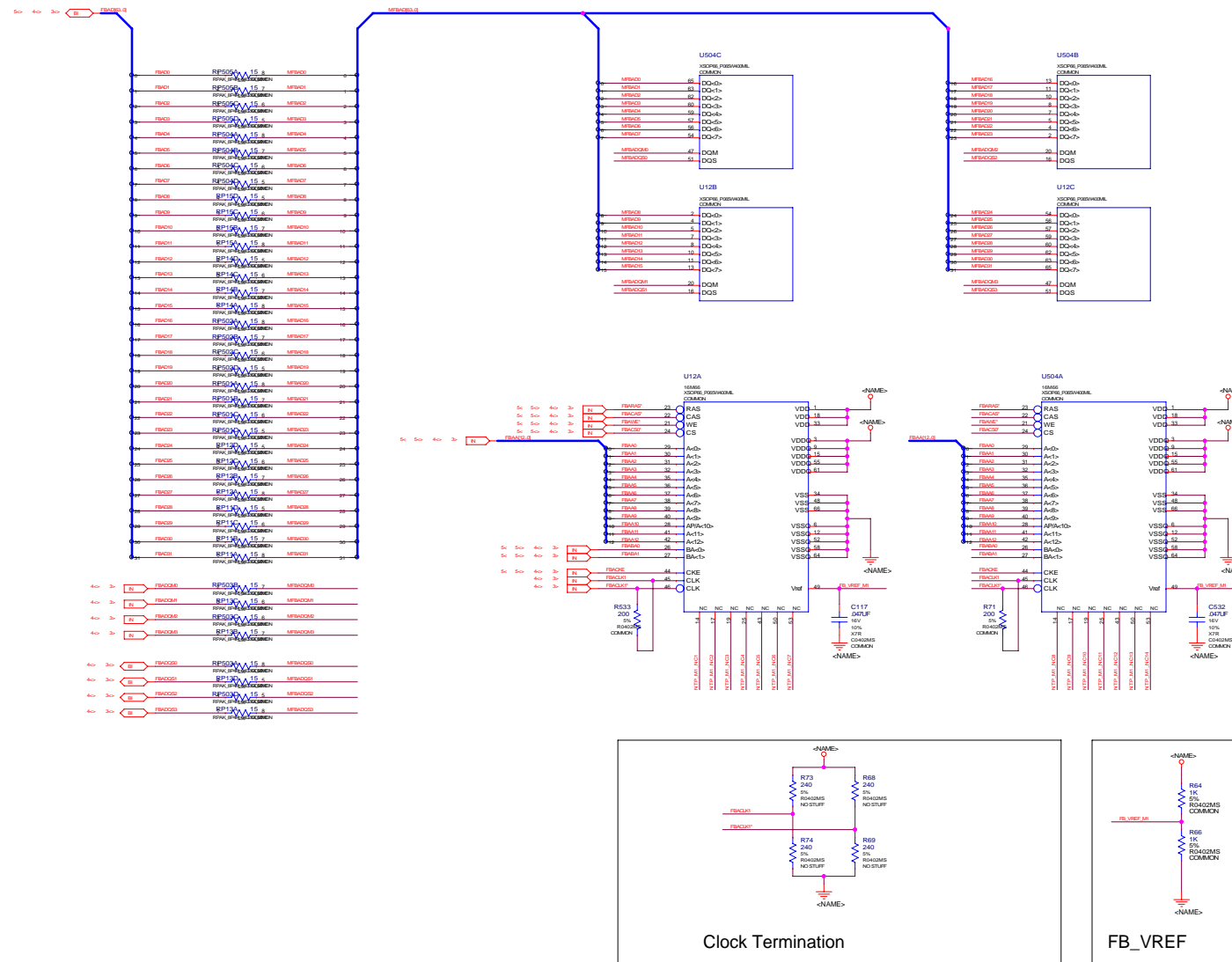
Net Spelling		Net Spelling
00	POWDER 00	13.00
01	POWDER 01	13.00
02	POWDER 02	13.00
03	POWDER 03	13.00
04	POWDER 04	13.00
05	POWDER 05	13.00
06	POWDER 06	13.00
07	POWDER 07	13.00
08	POWDER 08	13.00
09	POWDER 09	13.00
10	POWDER 10	13.00
11	POWDER 11	13.00
12	POWDER 12	13.00
13	POWDER 13	13.00
14	POWDER 14	13.00
15	POWDER 15	13.00
16	POWDER 16	13.00
17	POWDER 17	13.00
18	POWDER 18	13.00
19	POWDER 19	13.00
20	POWDER 20	13.00
21	POWDER 21	13.00
22	POWDER 22	13.00
23	POWDER 23	13.00
24	POWDER 24	13.00
25	POWDER 25	13.00
26	POWDER 26	13.00
27	POWDER 27	13.00
28	POWDER 28	13.00
29	POWDER 29	13.00
30	POWDER 30	13.00
31	POWDER 31	13.00
32	POWDER 32	13.00
33	POWDER 33	13.00
34	POWDER 34	13.00
35	POWDER 35	13.00
36	POWDER 36	13.00
37	POWDER 37	13.00
38	POWDER 38	13.00
39	POWDER 39	13.00
40	POWDER 40	13.00
41	POWDER 41	13.00
42	POWDER 42	13.00
43	POWDER 43	13.00
44	POWDER 44	13.00
45	POWDER 45	13.00
46	POWDER 46	13.00
47	POWDER 47	13.00
48	POWDER 48	13.00
49	POWDER 49	13.00
50	POWDER 50	13.00
51	POWDER 51	13.00
52	POWDER 52	13.00
53	POWDER 53	13.00
54	POWDER 54	13.00
55	POWDER 55	13.00
56	POWDER 56	13.00
57	POWDER 57	13.00
58	POWDER 58	13.00
59	POWDER 59	13.00
60	POWDER 60	13.00
61	POWDER 61	13.00
62	POWDER 62	13.00
63	POWDER 63	13.00
64	POWDER 64	13.00
65	POWDER 65	13.00
66	POWDER 66	13.00
67	POWDER 67	13.00
68	POWDER 68	13.00
69	POWDER 69	13.00
70	POWDER 70	13.00
71	POWDER 71	13.00
72	POWDER 72	13.00
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75	POWDER 75	13.00
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77	POWDER 77	13.00
78	POWDER 78	13.00
79	POWDER 79	13.00
80	POWDER 80	13.00
81	POWDER 81	13.00
82	POWDER 82	13.00
83	POWDER 83	13.00
84	POWDER 84	13.00
85	POWDER 85	13.00
86	POWDER 86	13.00
87	POWDER 87	13.00
88	POWDER 88	13.00
89	POWDER 89	13.00
90	POWDER 90	13.00
91	POWDER 91	13.00
92	POWDER 92	13.00
93	POWDER 93	13.00
94	POWDER 94	13.00
95	POWDER 95	13.00
96	POWDER 96	13.00
97	POWDER 97	13.00
98	POWDER 98	13.00
99	POWDER 99	13.00
100	POWDER 100	13.00

# NV31 Framebuffer Interface



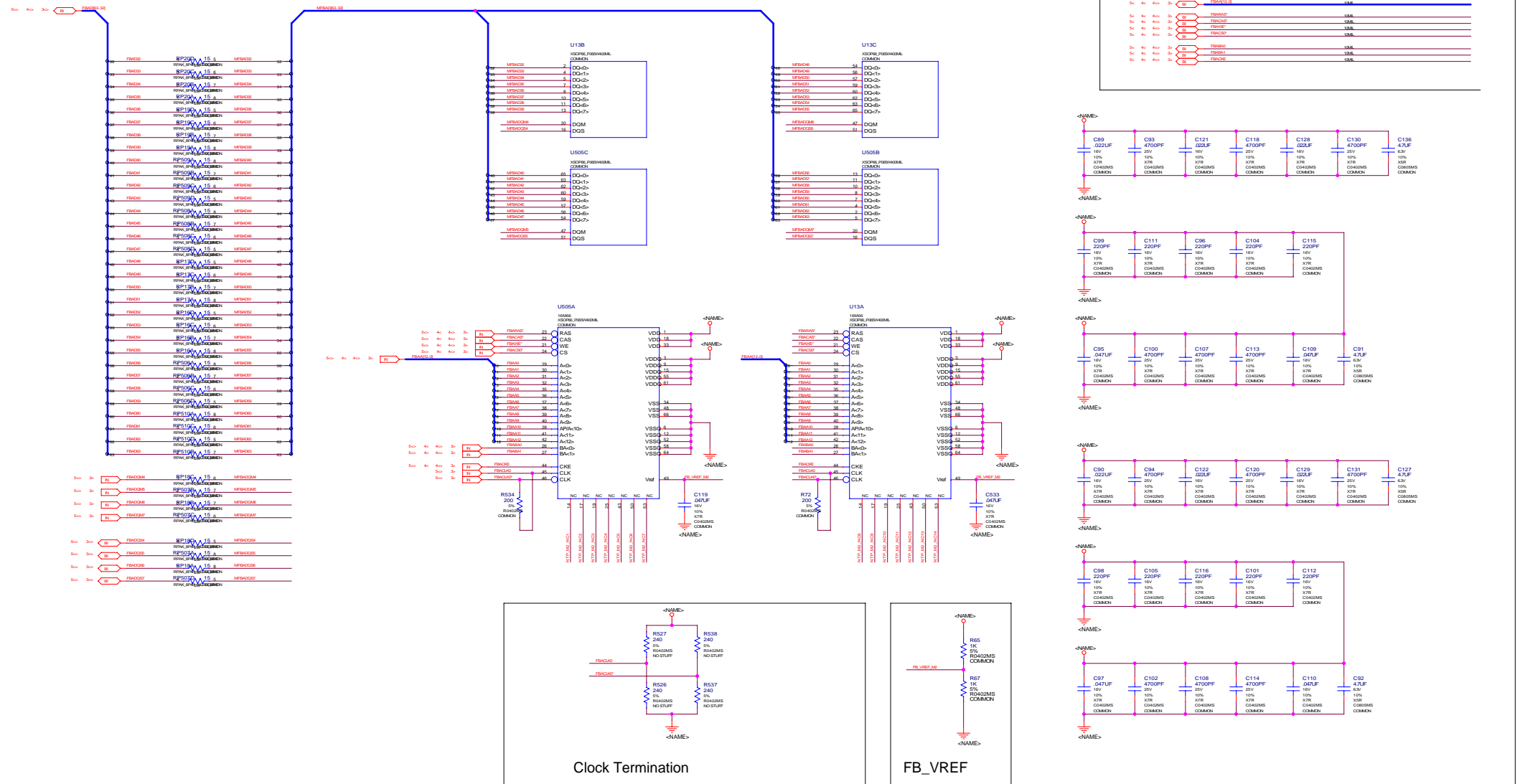
# MEMORY 8(16)Mx16DDR Partition A , Bits 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

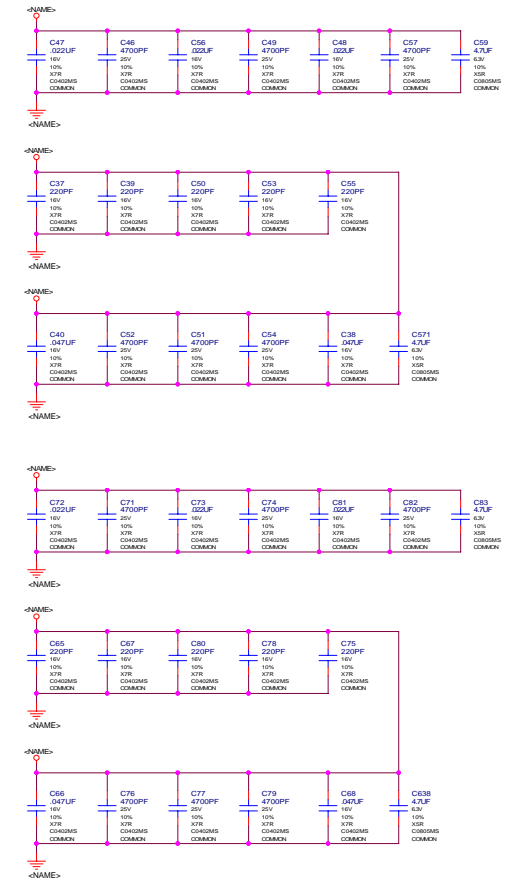
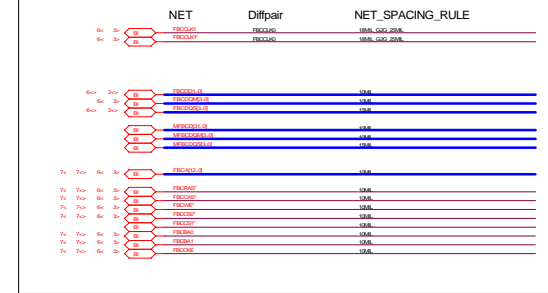


# MEMORY 8(16)Mx16DDR Partition A , Bits 32..63

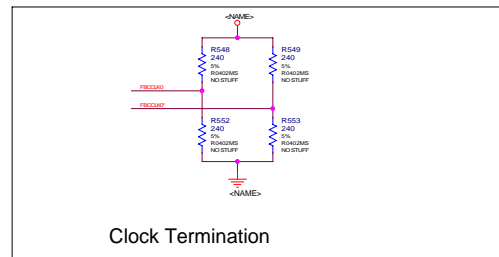
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

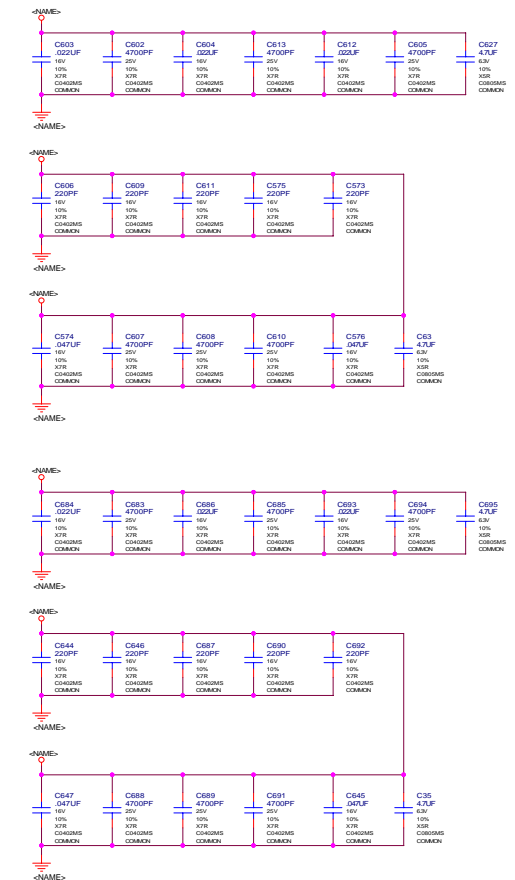


PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

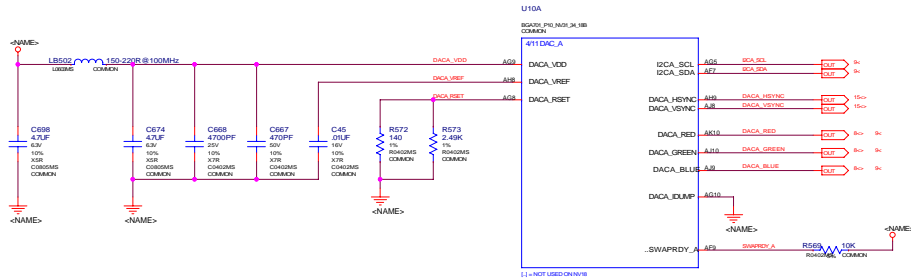


FB\_VREF

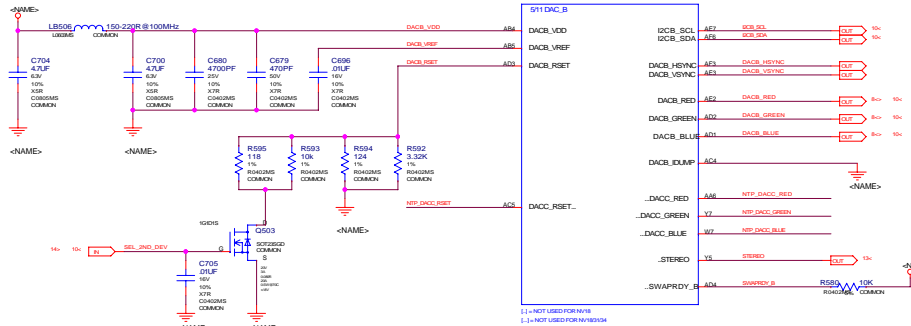
FB\_VREF



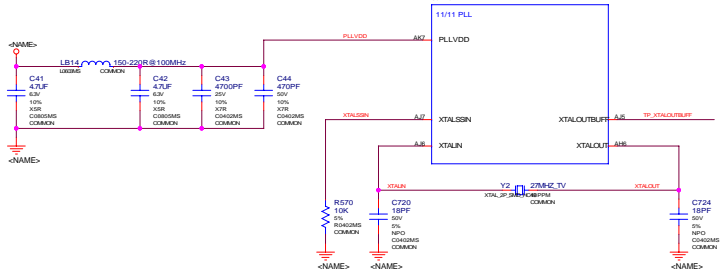
NV31 DAC\_A



NV31 DAC\_B with RSet select



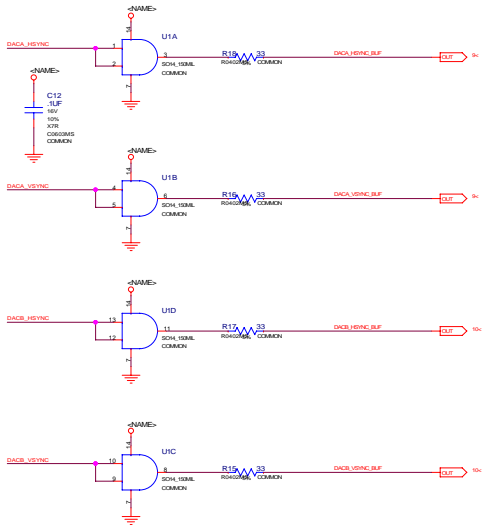
NV31 PLL



NET	NET_PHYSICAL_TYPE	VOLTAGE
DACA_VDD	10K_TRACE	3.3V
DACA_VREF	10K_TRACE	3.3V
DACA_VDD	10K_TRACE	3.3V
DACA_VREF	10K_TRACE	3.3V
DACA_VDD	10K_TRACE	3.3V
DACA_VREF	10K_TRACE	3.3V
DACA_VDD	10K_TRACE	3.3V
DACA_VREF	10K_TRACE	3.3V
PLL_VDD	10K_TRACE	3.3V
XTALOUT	10K_TRACE	3.3V

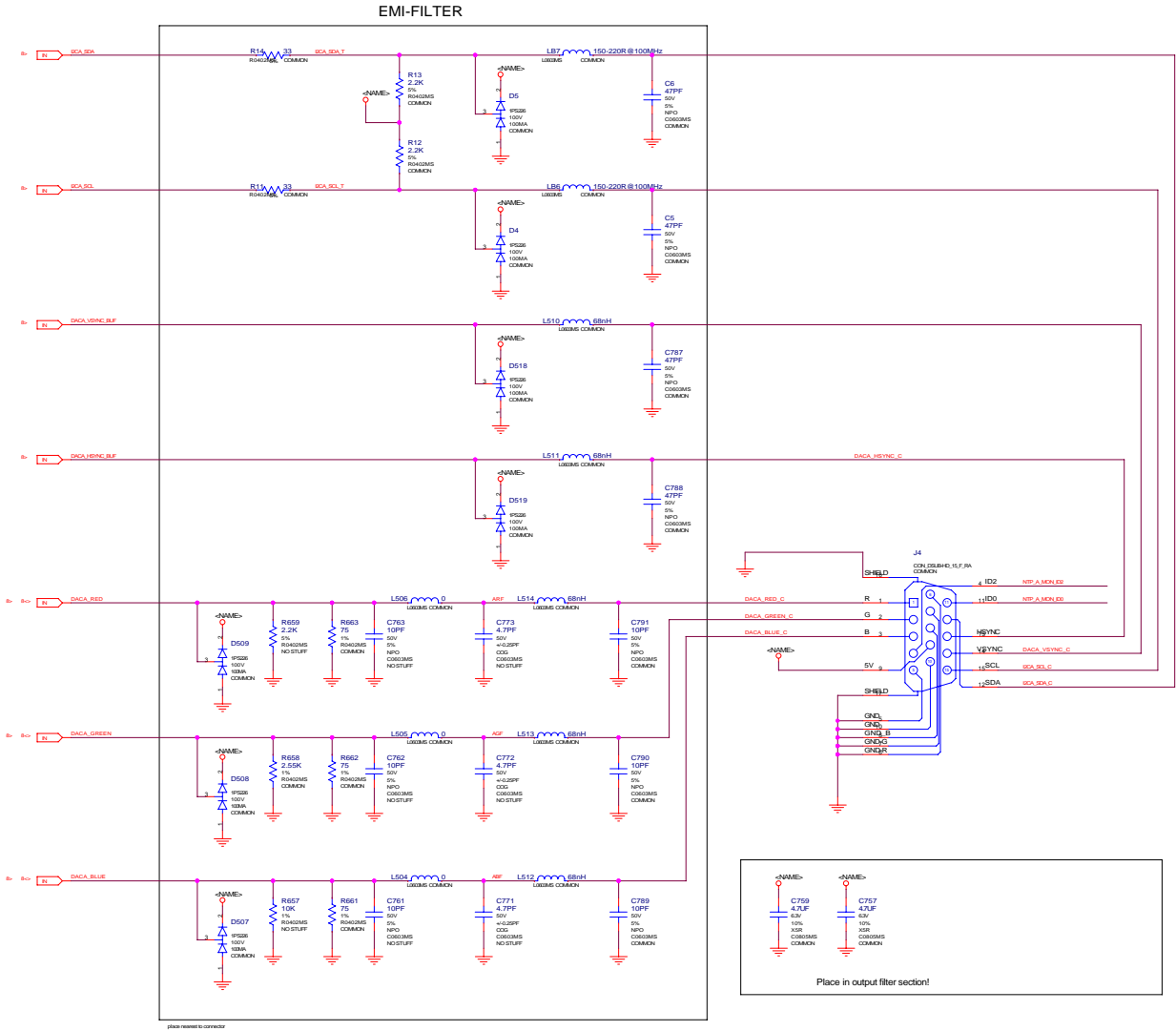
NET	NET_PHYSICAL_TYPE	NET_SPACING_RULE
DACA_VDD	10K_TRACE	10K
DACA_VREF	10K_TRACE	10K
DACA_VDD	10K_TRACE	10K
DACA_VREF	10K_TRACE	10K
DACA_VDD	10K_TRACE	10K
DACA_VREF	10K_TRACE	10K
DACA_VDD	10K_TRACE	10K
DACA_VREF	10K_TRACE	10K
DACA_VDD	10K_TRACE	10K
DACA_VREF	10K_TRACE	10K

SYNC Buffer





NET	NET_SPACING_RULE
REF	20MIL_G01.20MIL
REF	20MIL_G02.20MIL
REF	20MIL_G03.20MIL
DACA_RED_C	20MIL_G01.20MIL
DACA_GREEN_C	20MIL_G01.20MIL
DACA_BLUE_C	20MIL_G01.20MIL



Place all filter components on the side nearest to the reference GND plane!

Route all signals only on layers referenced to GND!

Don't split the reference GND plane beneath a RGB signal!

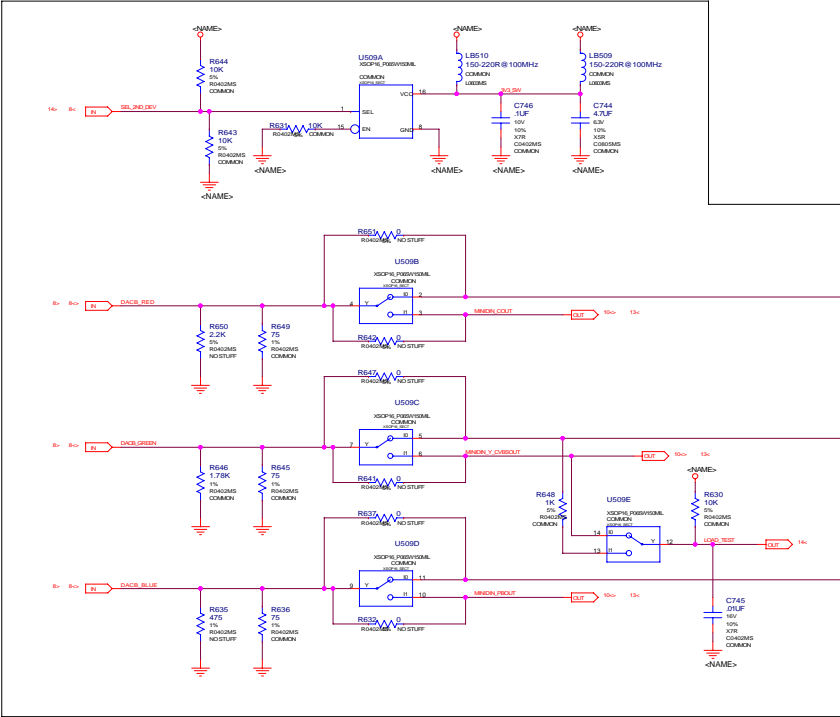
Secondary Display (DACB), SILM DB15 optional DVI-I

Place all filter components on the side nearest to the reference GND plane!

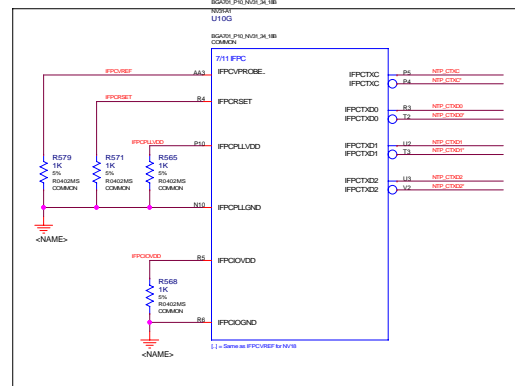
Route all signals only on layers referenced to GND!

Don't split the reference GND plane beneath a RGB signal!

DACB Multiplexer

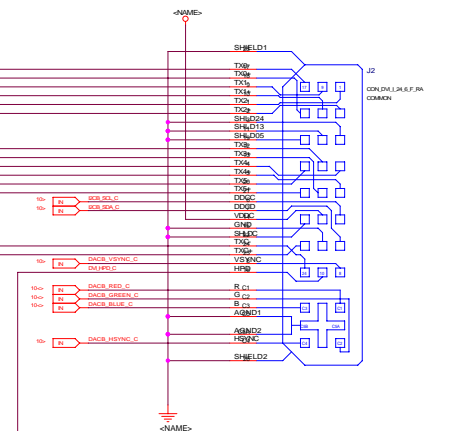


## Unused Transmitter

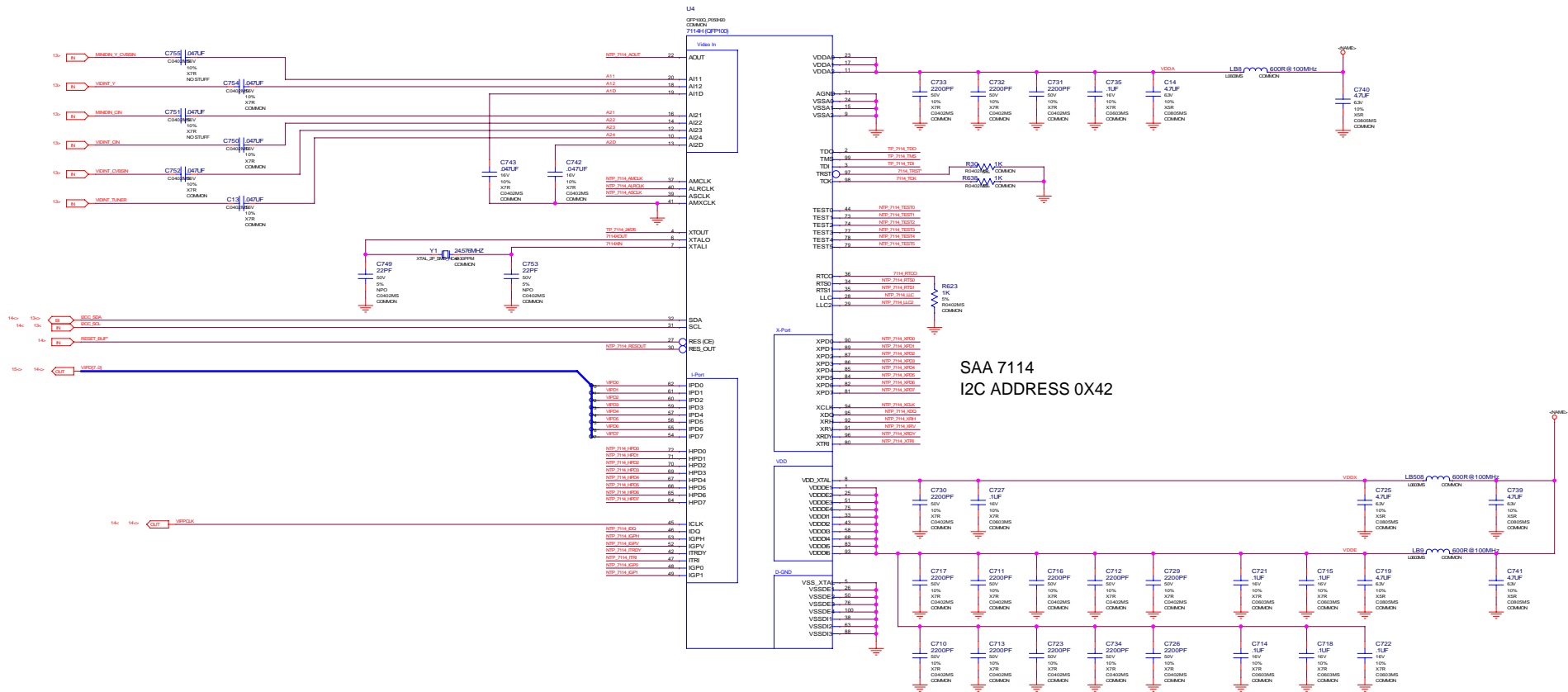


The diagram shows a 10-bit DAC circuit. It features a series of resistors (R001 to R019) and operational amplifiers (U001 to U006). The input is a 5V source connected to R010. The output is connected to a 5V source. The circuit is labeled with component values and names.

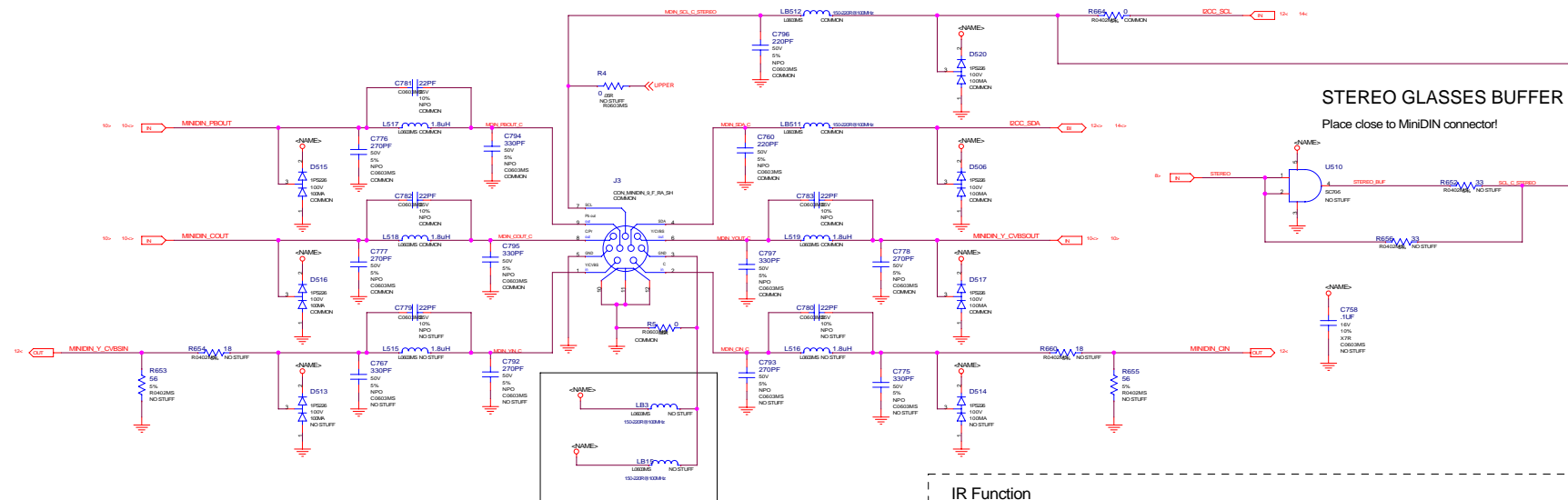
NET	Difpair	NET_SPACING_RULE
10	ATD0	23A, GIG 33A
10	ATD1	23B, GIG 33B
20	ATD0	23A, GIG 33A
20	ATD1	23B, GIG 33B
30	ATD0	23A, GIG 33A
30	ATD1	23B, GIG 33B
40	ATD0	23A, GIG 33A
40	ATD1	23B, GIG 33B
50	ATD0	23A, GIG 33A
50	ATD1	23B, GIG 33B
60	BD00	23A, GIG 33A
60	BD01	23B, GIG 33B
70	BD00	23A, GIG 33A
70	BD01	23B, GIG 33B
80	BD00	23A, GIG 33A
80	BD01	23B, GIG 33B



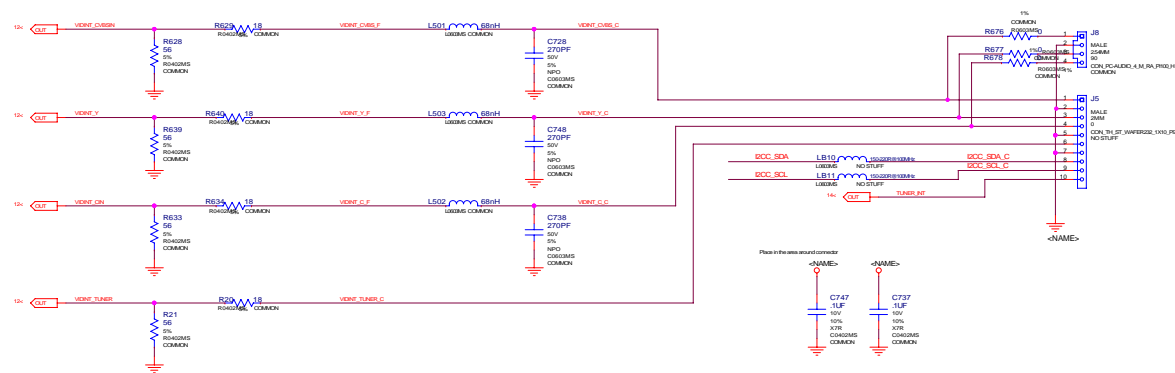
# VIDEO CAPTURE



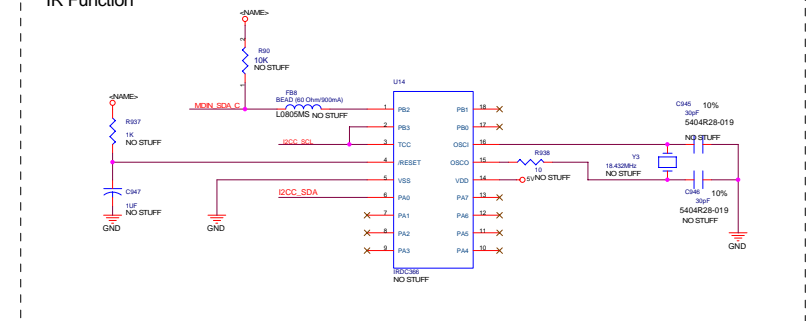
## VIDEO IN/OUT CONNECTOR /STEREO GLASSES



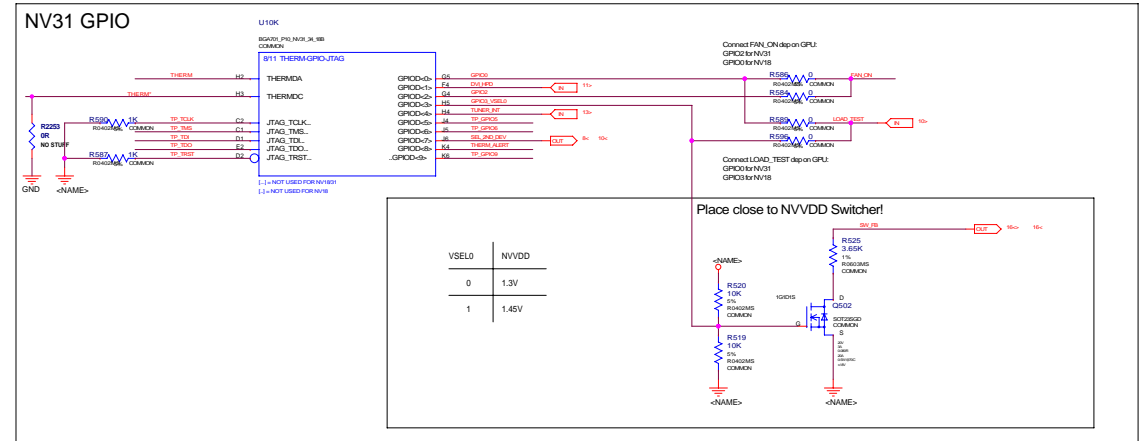
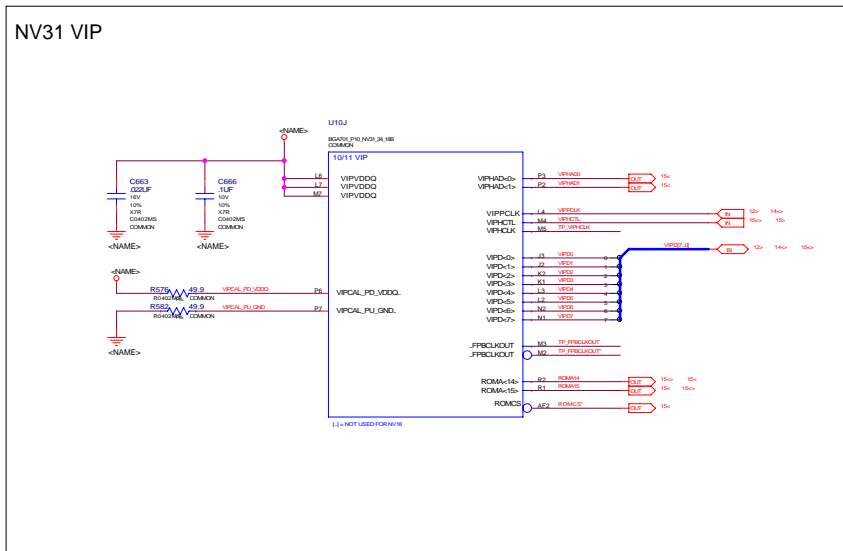
## INTERNAL VIDEO IN CONNECTOR



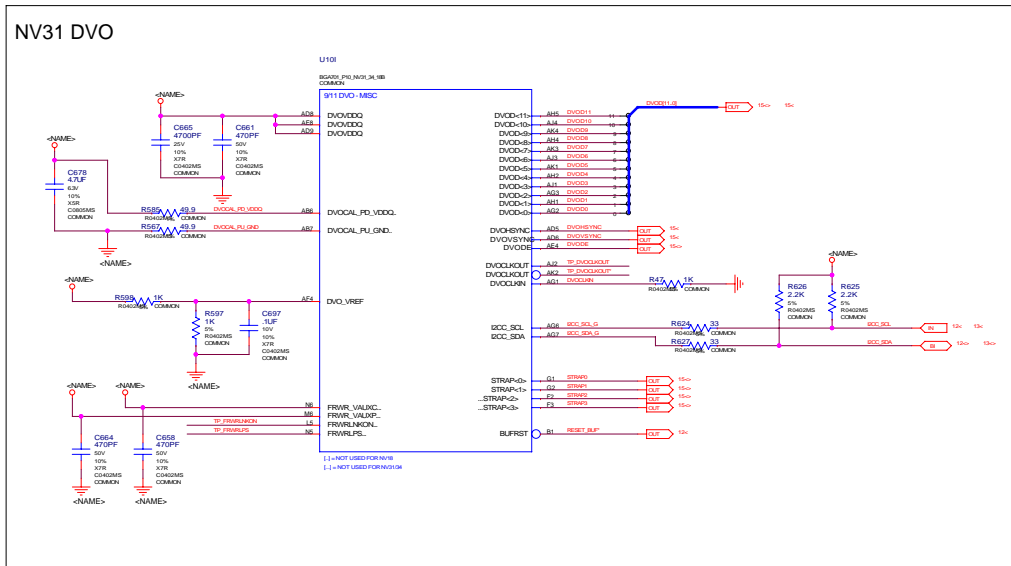
## IR Function



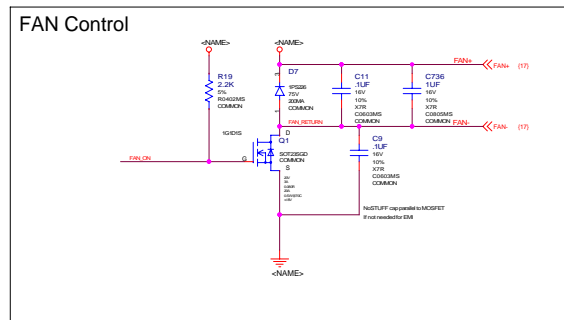
## NV31 VIP



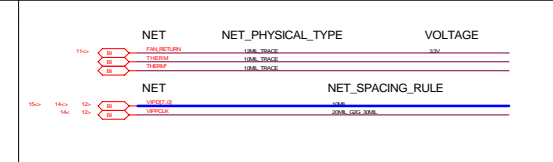
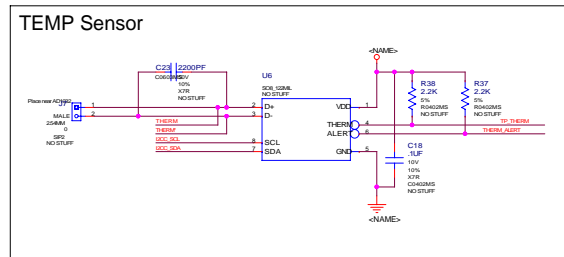
## NV31 DVO



FAN Control

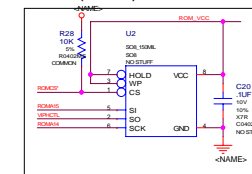
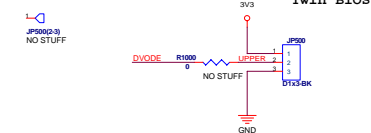



## TEMP Sensor



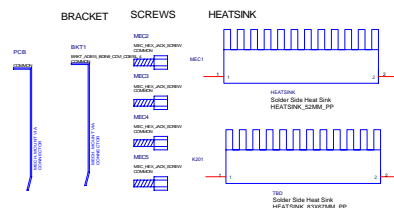
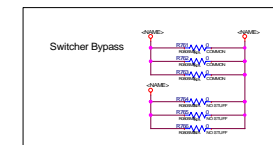
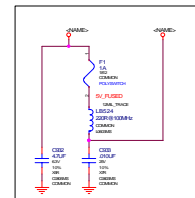
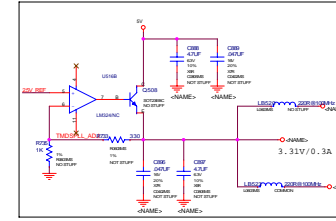
OR MASK  
1  $\Rightarrow$  DESIRED=1 AND MASK=0

## BIOS (serial)

[illegible]

	<b>Micro-Star International Co., LTD.</b>		
	<b>MS-8912 base on P141-A03 modify</b>		
	Size Custom	Document Number <b>NV31 BIOS STRAPPING</b>	Rev 300
Date:	Expiry: Expiration: 94-0000	ISheet: 15	of 17

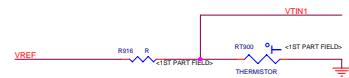
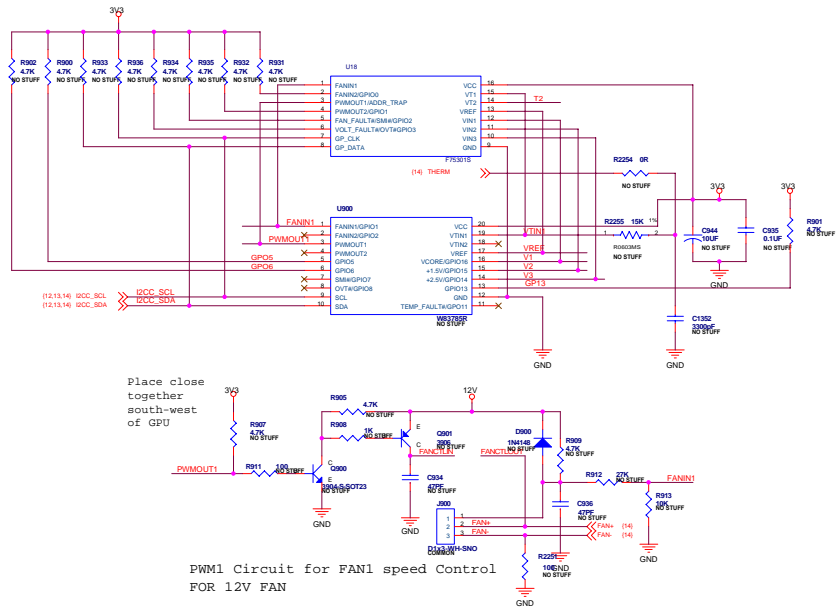
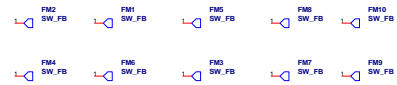
TMDS PLL Supply



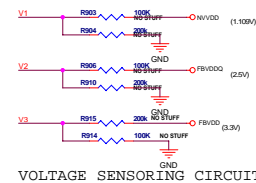
ISL6225  $FBVDD = [0.9V * (1K+375)] / 375 = 3.3V$   
 NV31  $NVDD = [0.9V * (1K+4.3K)] / 4.3K = 1.109V$   
 NV18B Stand Volt need 1.656 V.



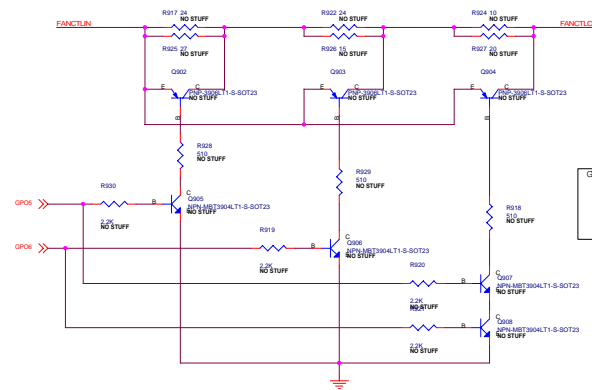
## H/W Monitor Funtion



## TEMPERATURE SENSING CIRCUIT



VOLTAGE SENSING CIRCUIT



GPO5	GPO6	Q1	Q2	Q3	Vout
0	0	off	off	off	9V
1	0	on	off	off	10V
0	1	off	on	off	11V
1	1	on	on	on	12V