

PG301 A02


Comanche 192b GDDR5, <150W, 2-way SLI  
Tall DVI-I + DP + DP + DP/HDMI + DP

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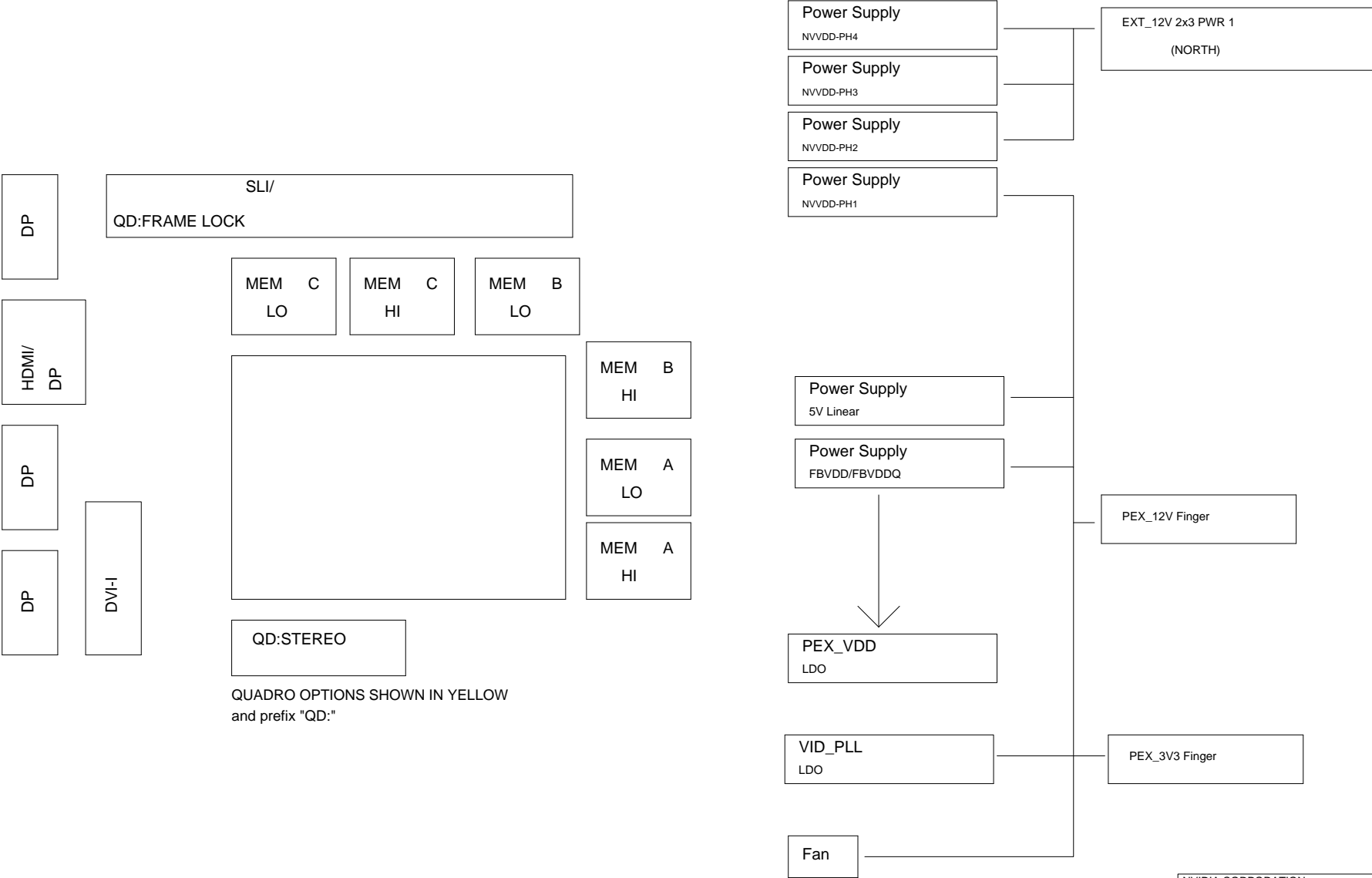
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Block Diagram



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ASSEMBLY	BASIC LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	Block Diagram


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PCI Express



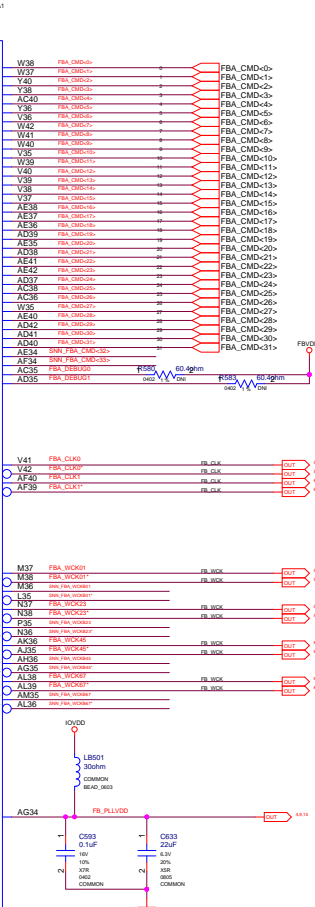
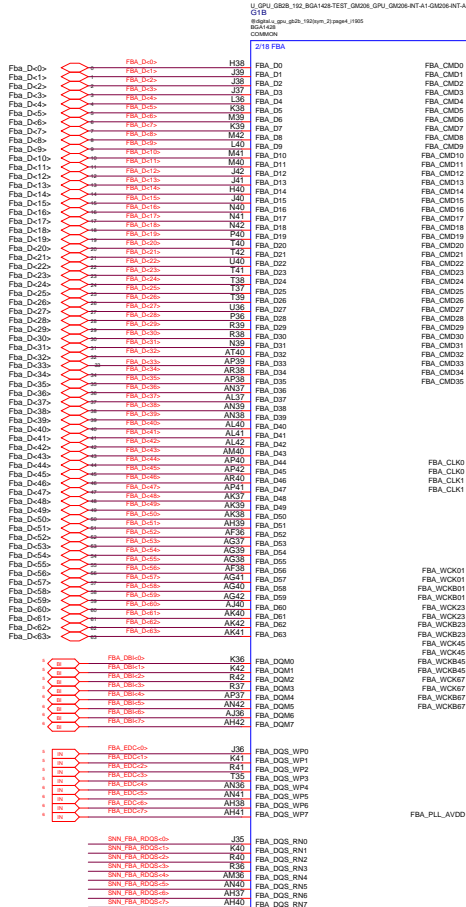
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PCI Express

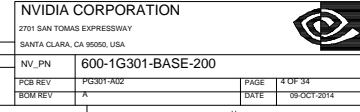
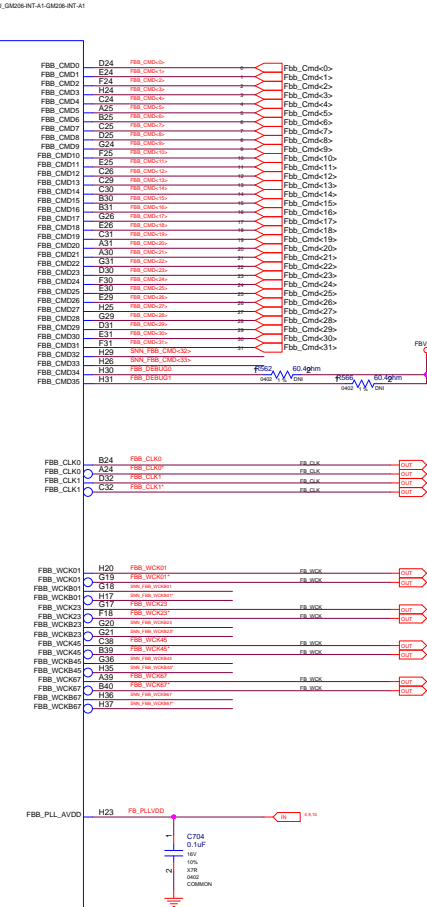
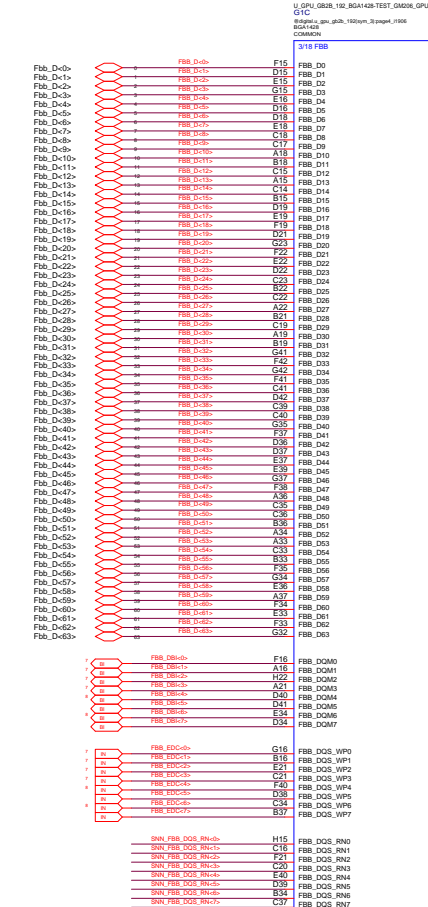
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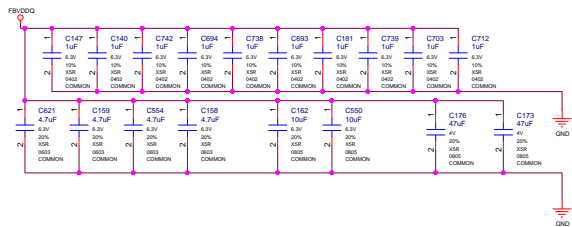
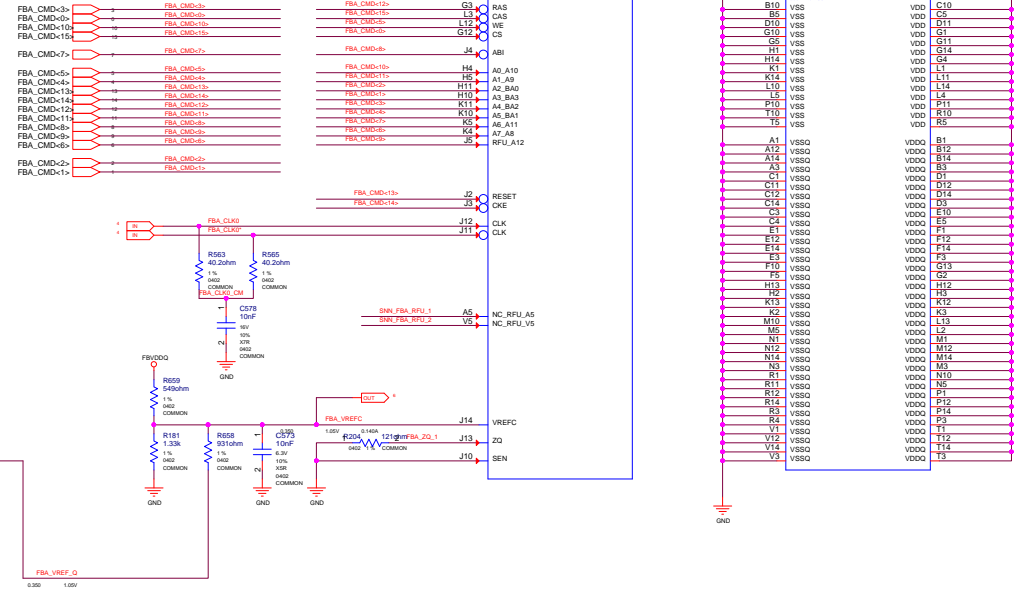
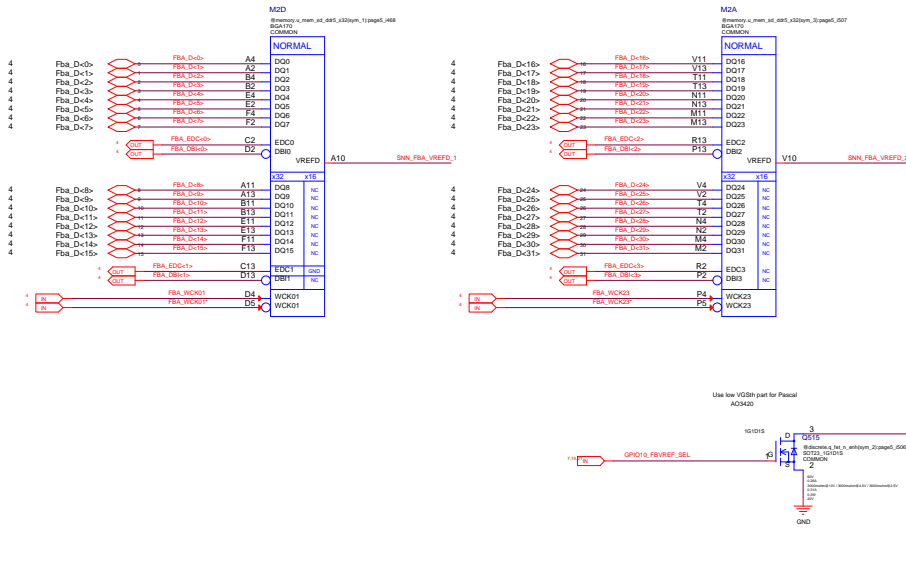
MEMORY: GPU Partition A/B



GDDR5\_BGA170\_MIRROR



# MEMORY: FBA Partition 31..0



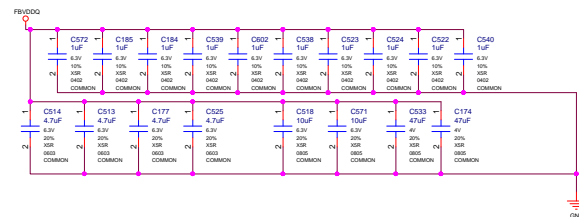
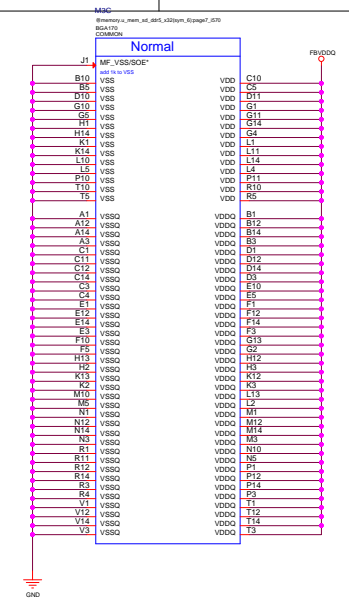
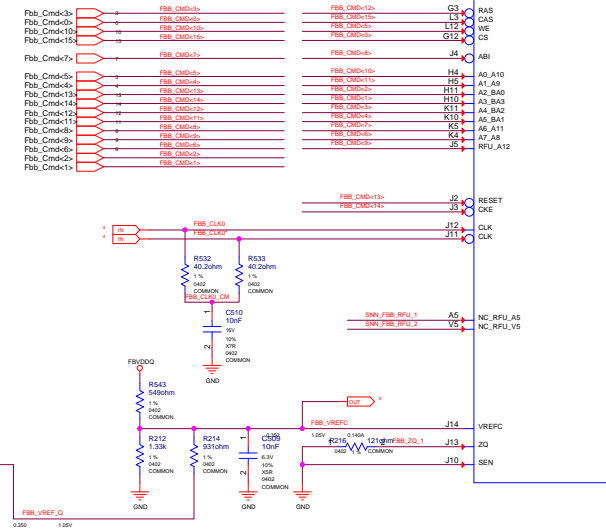
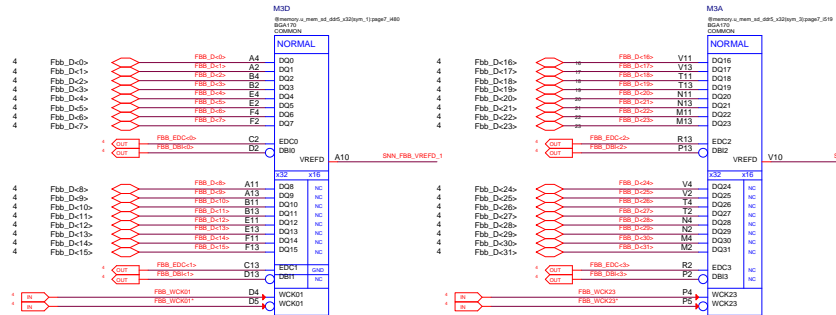
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PAGE DETAIL	MEMORY FB(31..0)

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MEMORY: FBB Partition 31..0

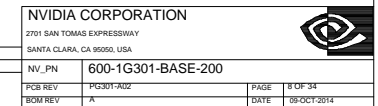


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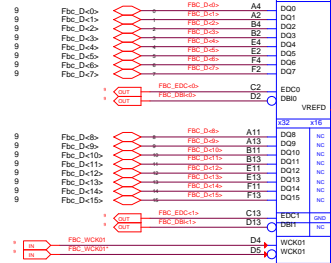




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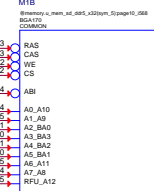
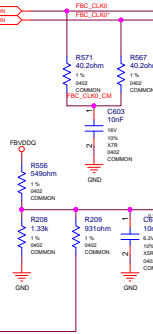
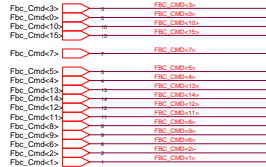
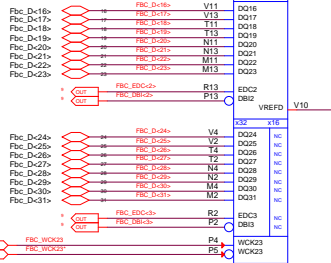
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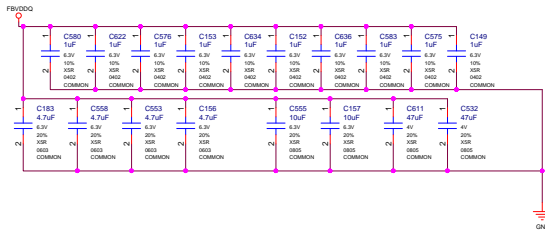
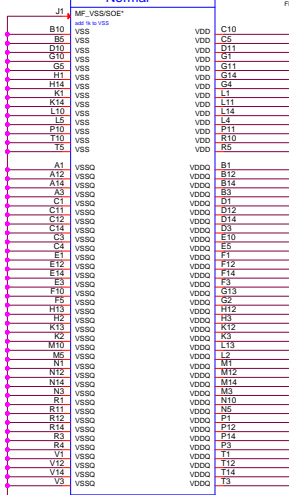
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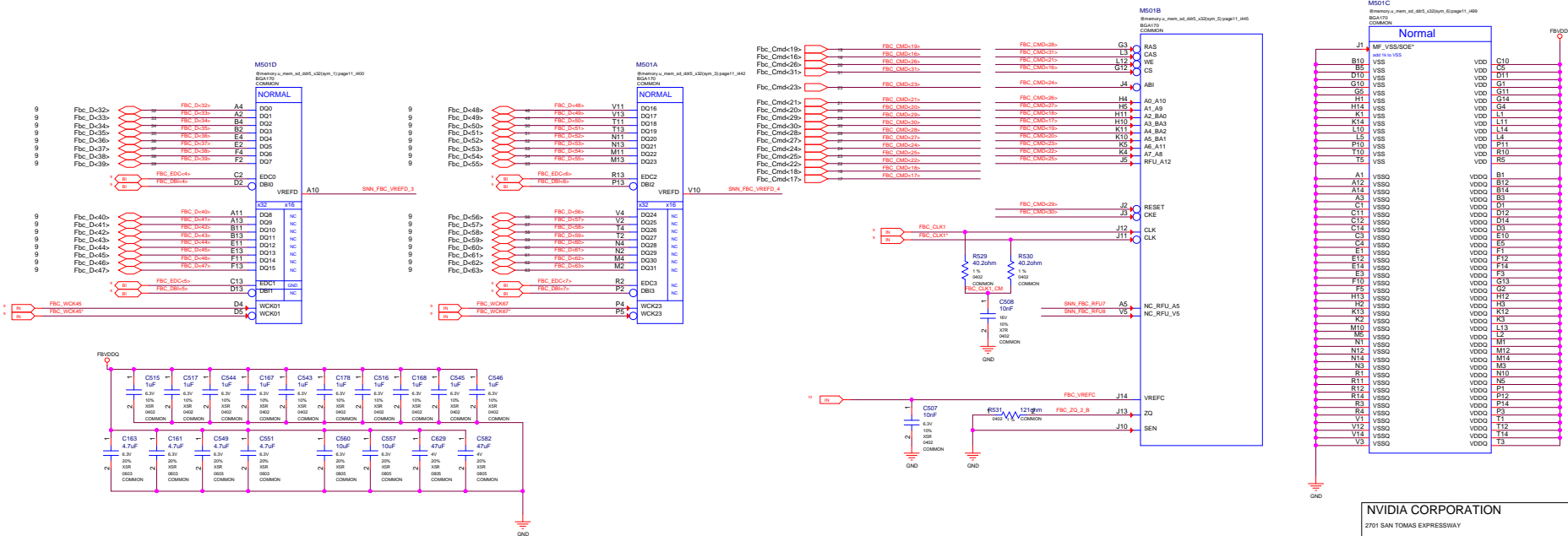
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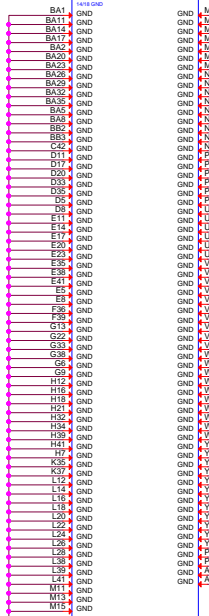
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G11

BGA1426

COMMON

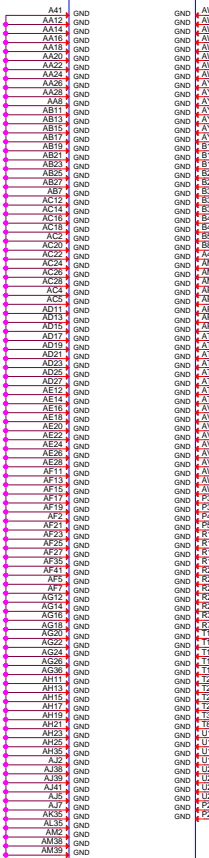


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G11

BGA1426

COMMON

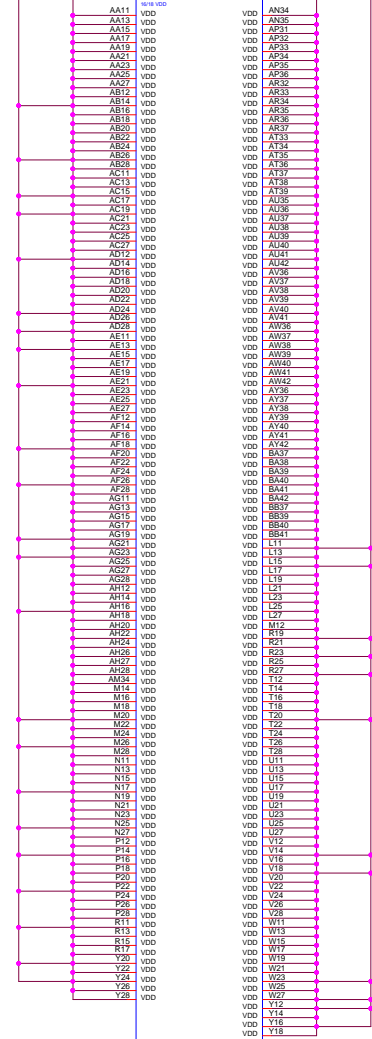


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BGA1426

COMMON

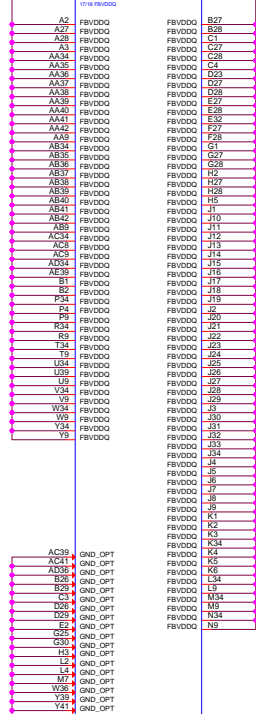


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G11

BGA1426

COMMON

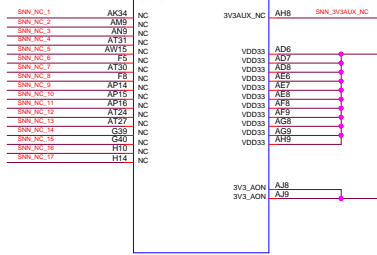


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G11

BGA1426

COMMON



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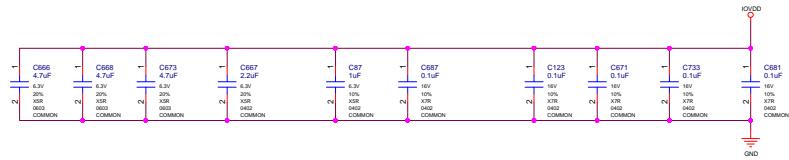
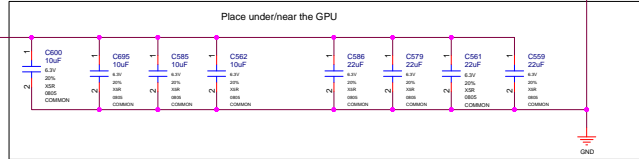
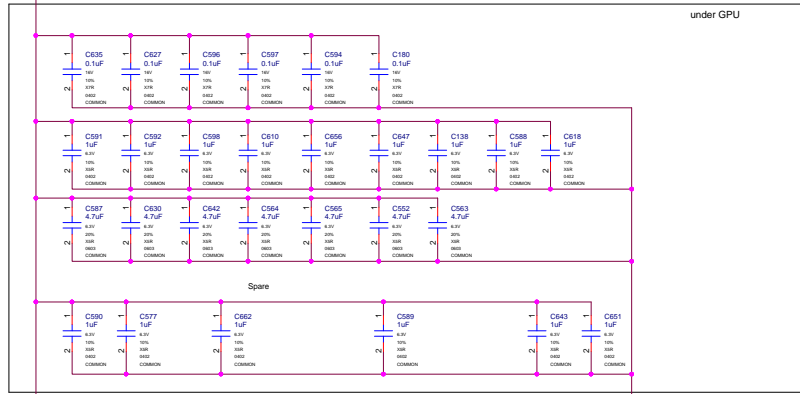
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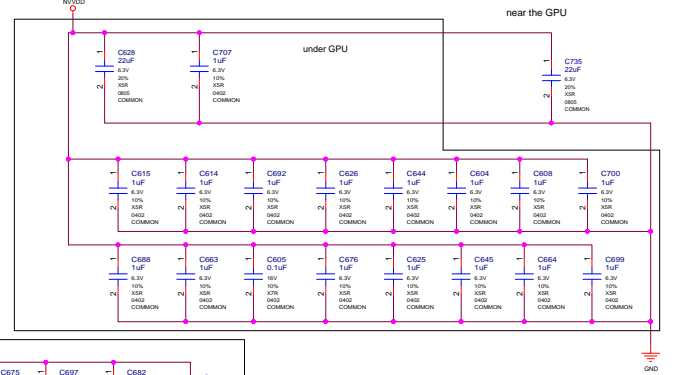
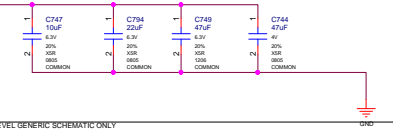
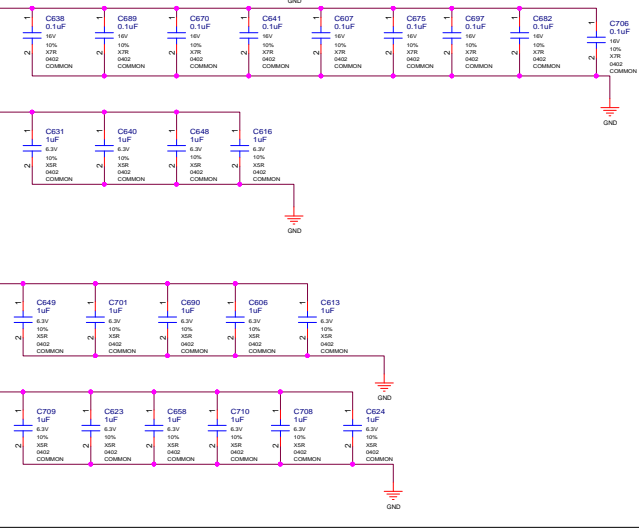
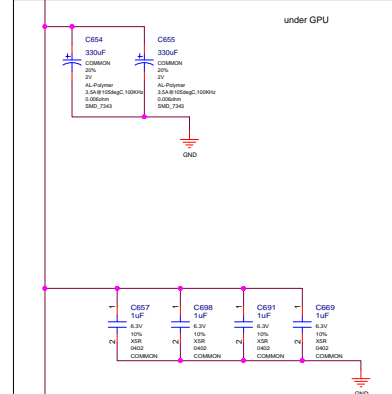
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# GPU Decoupling

FBVDDQ



NVVD




	Under GPU	Near GPU
NVVD	90uF + 1x 330uF	88uF
SVVD	32uF	22uF
Combined (Maxwell)	122uF + 1x 330uF	110uF

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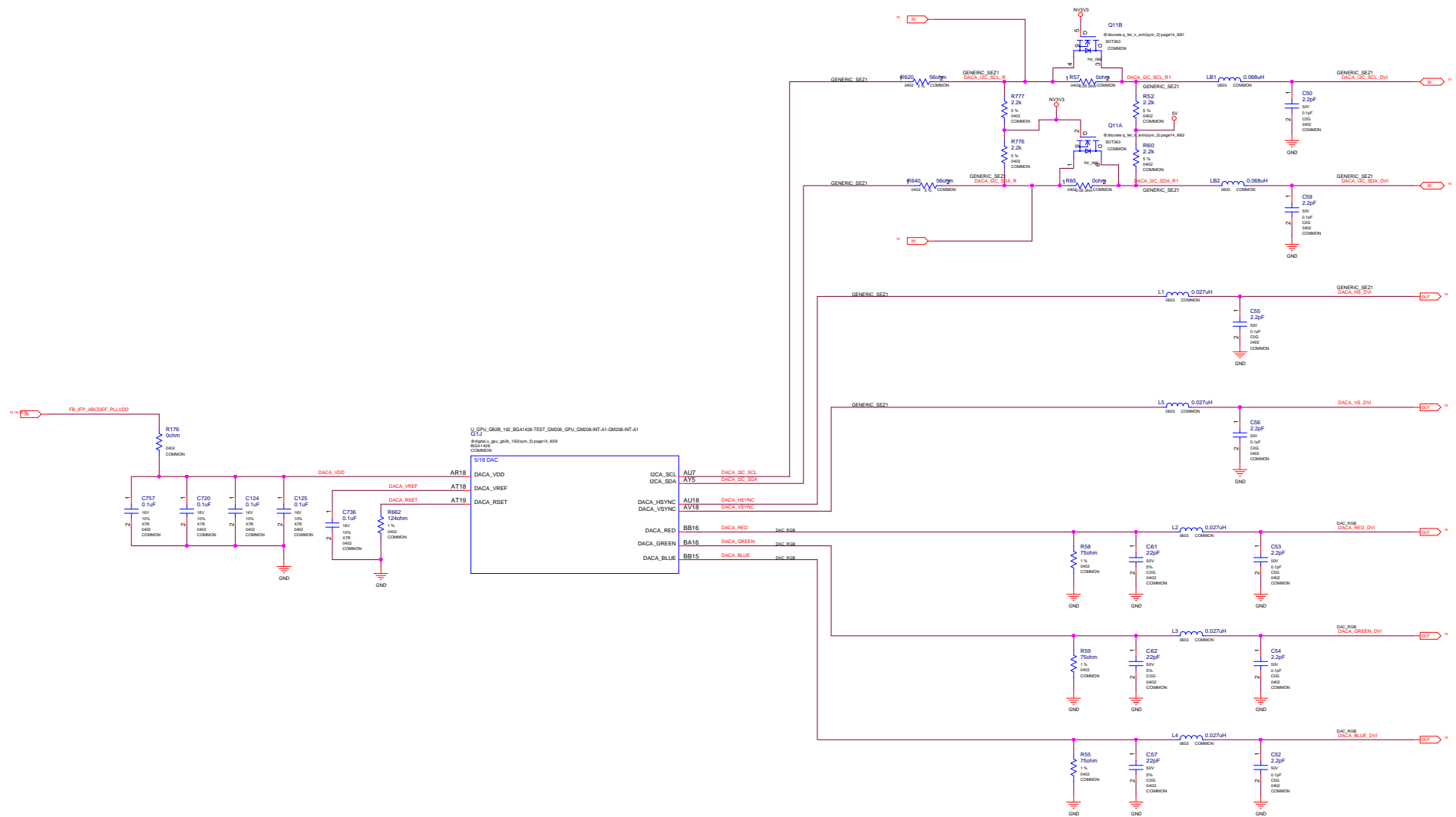
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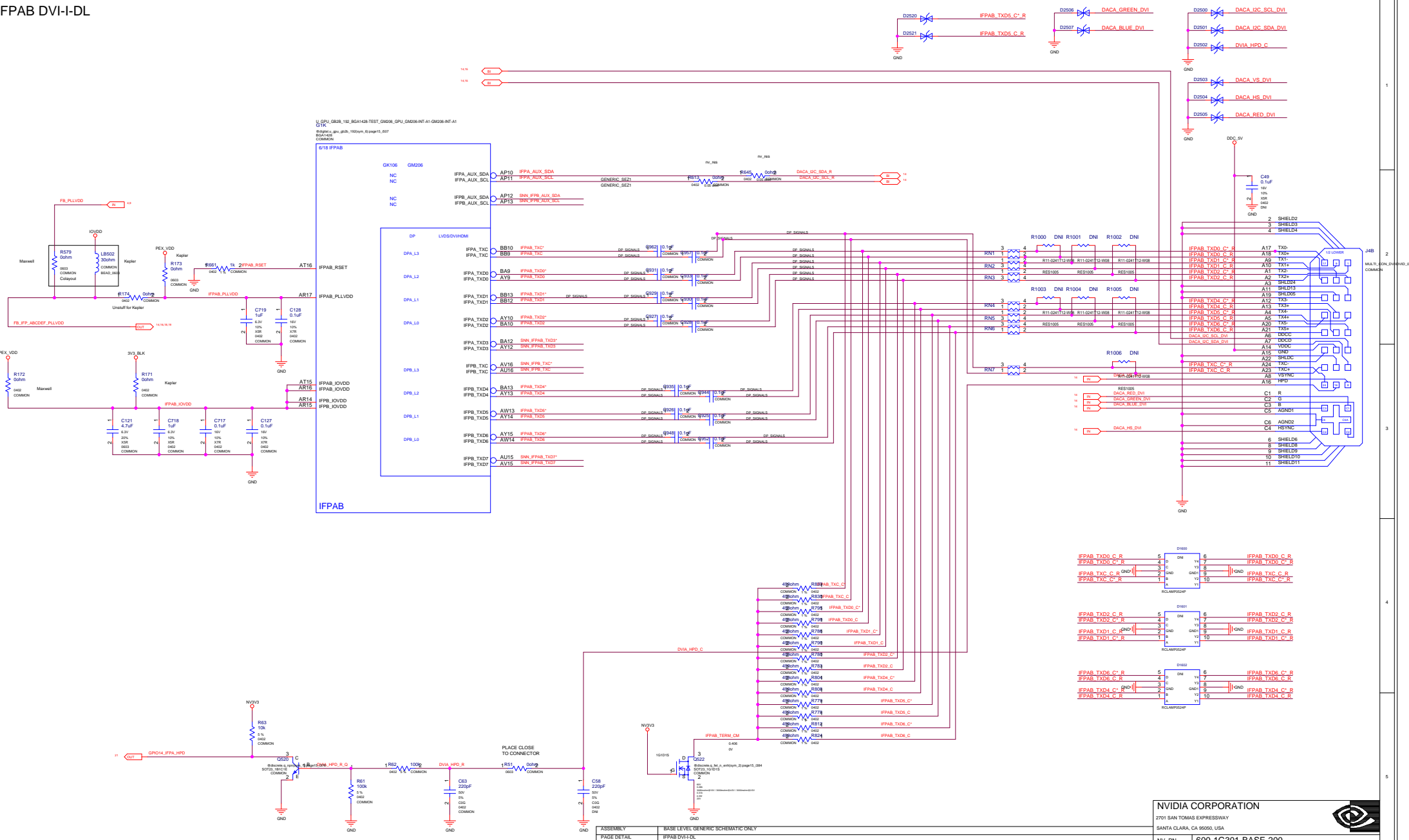
## DACA Interface




ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DACA Interface

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## IFPAB DVI-I-DL



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IFPF DP

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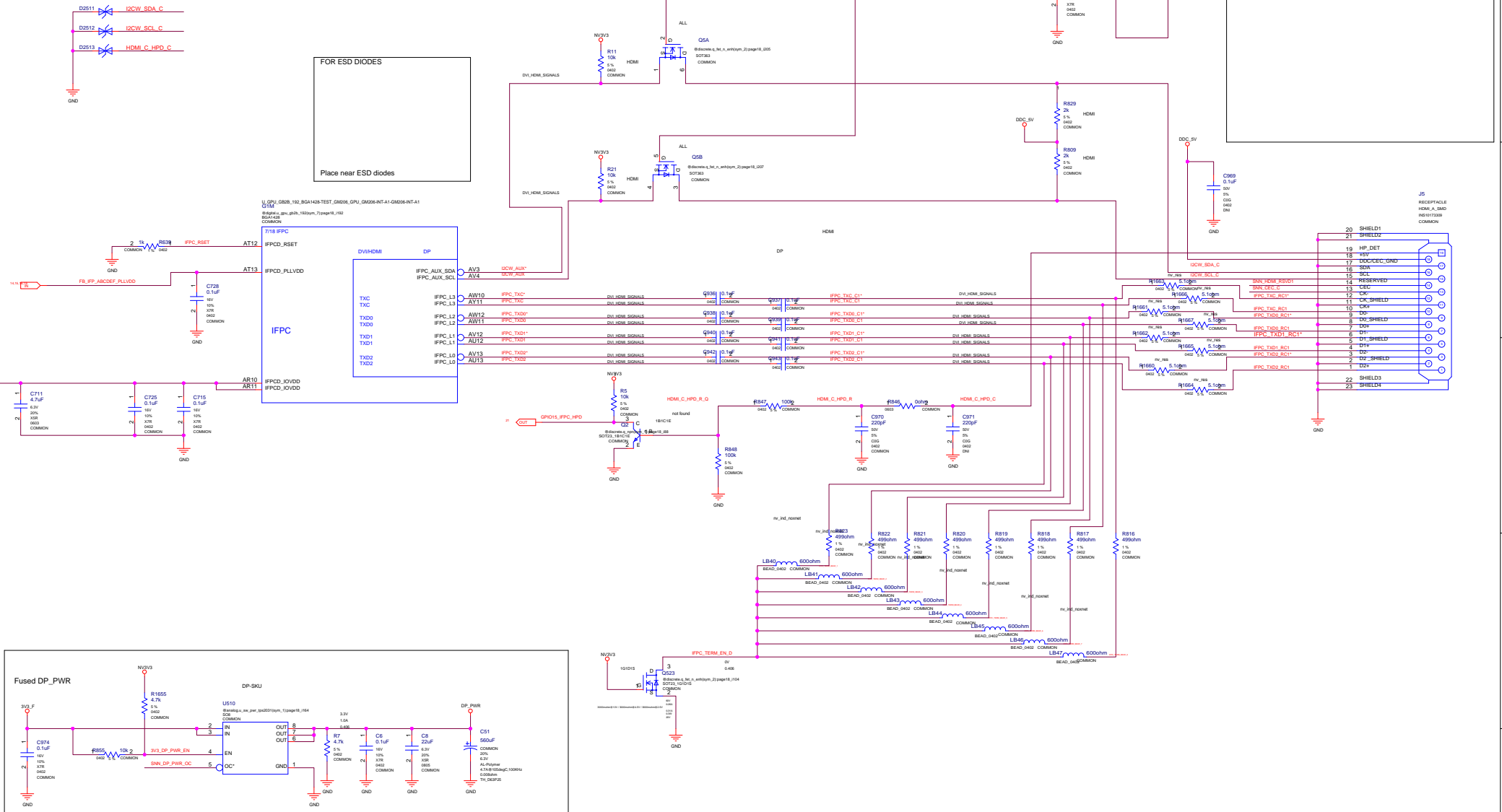
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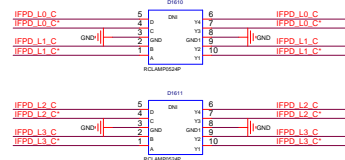
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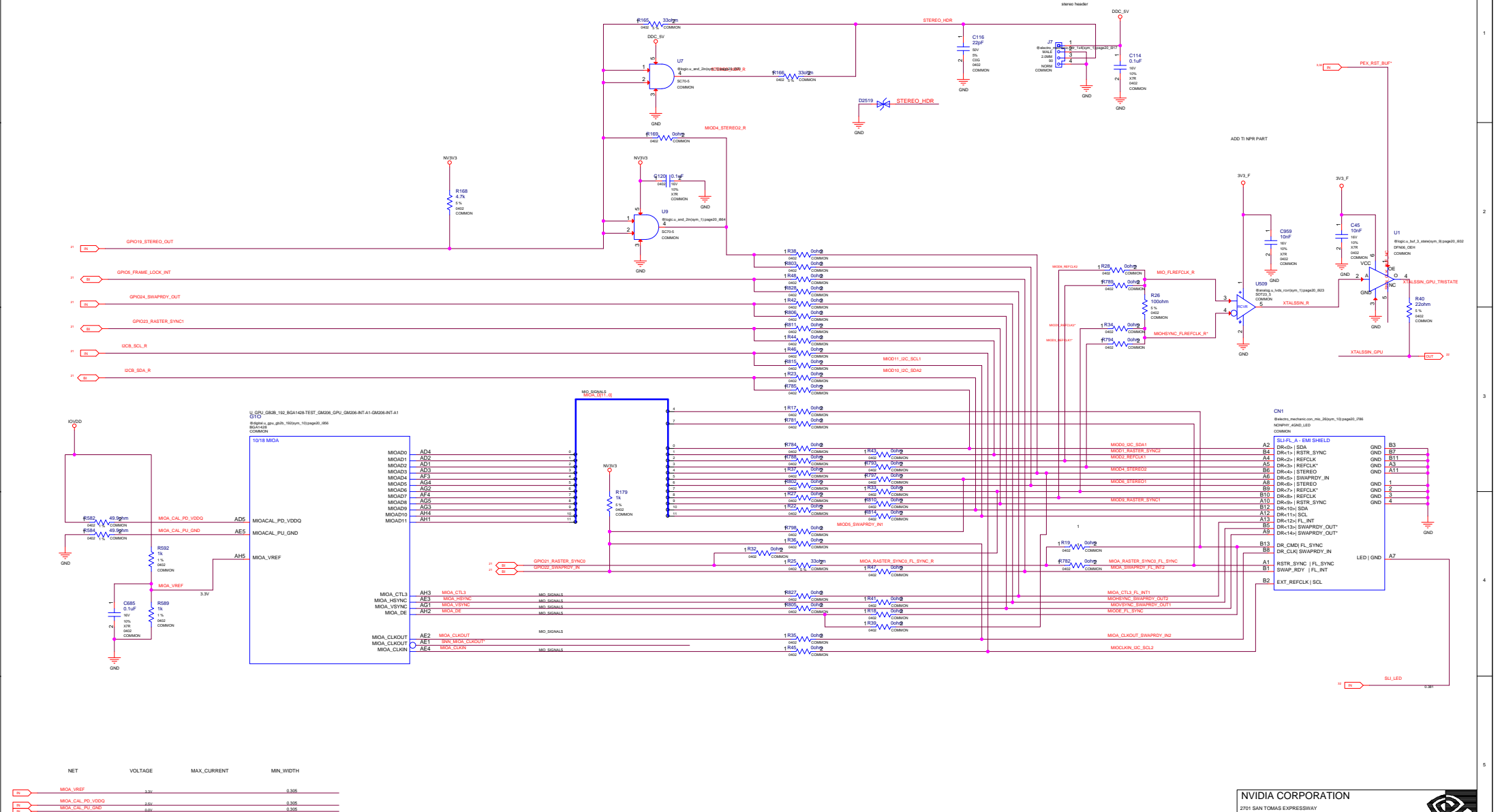


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPC HDM/DP

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MIOA/SLI Interface



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ASSEMBLY      BASE LEVEL GENERIC SCHEMATIC ONLY  
PAGE DETAIL      MIOA

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NV\_PN

600-1G301-BASE-200

PCB REV

PG301-AD2

BOX REV

A

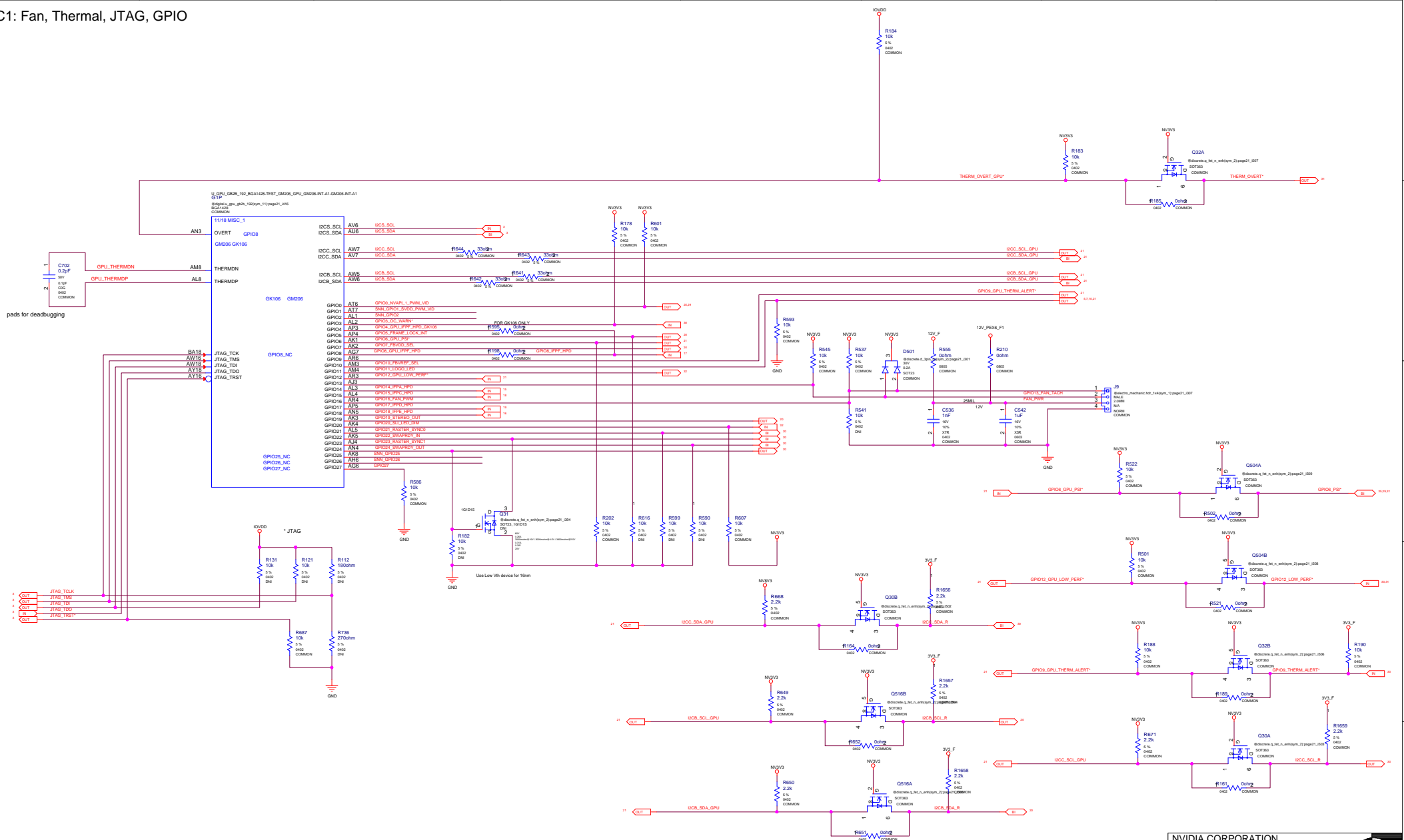
PAGE

20 OF 34

DATE

08-OCT-2014

MISC1: Fan, Thermal, JTAG, GPIO



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PCB REV	PG301-A02	PAGE	21 OF 34
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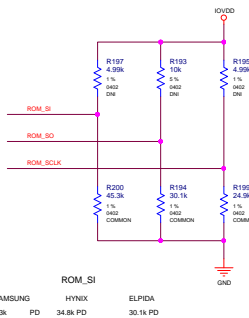
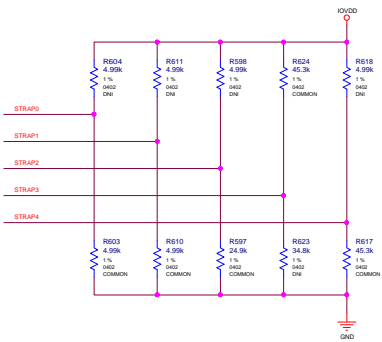
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO

MISC2: ROM, XTAL, Straps

	KEPLER	MAXWELL
STRAP0	USER_BIT [3:0]*	
STRAP1	3GIO_PADCFG_LUT_ADR*	
STRAP2	PCI_DEVID [3:0]*	
STRAP3	SOR_EXPOSED [3:0]*	
STRAP4	DP_PLL_VDD_33V*	
	PEX_MAX_SPEED*	
	PEX_SPD_CHANGE_GEN3*	
	*	
ROM_SI	RAMCFG[0]*	RAMCFG[0]*
	RAMCFG[1]*	RAMCFG[1]*
	RAMCFG[2]*	RAMCFG[2]*
	RAMCFG[3]*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	VGA_DEVICE*
	SMB_ALT_ADDR*	SMB_ALT_ADDR*
	FB[0]_APERTURE_SIZE*	PCIE_CFG*
	FB[1]_APERTURE_SIZE*	DEVID_SEL*
ROM_SCLK	PEX_PLL_EN_TERM100*	SOR0_EXPOSED*
	PCI_DEVID_EXT[5]*	SOR1_EXPOSED*
	SUB_VENDOR*	SOR2_EXPOSED*
	PCI_DEVID_EXT[4]*	SOR3_EXPOSED*

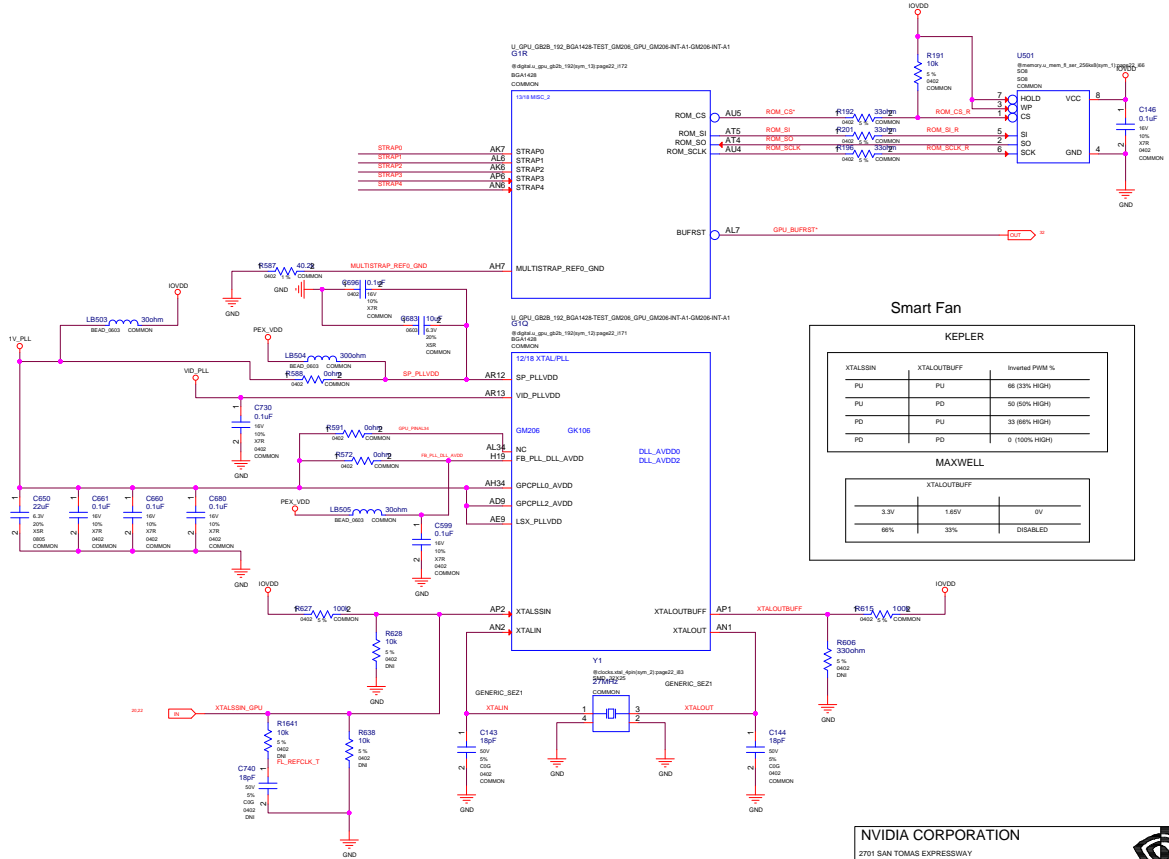
MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND

MAXWELL		
3.3V	1.65V	0V
G06+ISLAND ENABLED	G06+ DEBUG MODE	G06+ ISLAND DISABLED



ROM_SI		
SAMSUNG	HYNIX	ELPIDA
45.3k	PD	34.8k PD
		30.1k PD

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111



Smart Fan		
KEPLER		
XTALSSN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PD	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)
MAXWELL		
XTALOUTBUFF		
3.3V	1.65V	0V
66%	33%	DISABLED

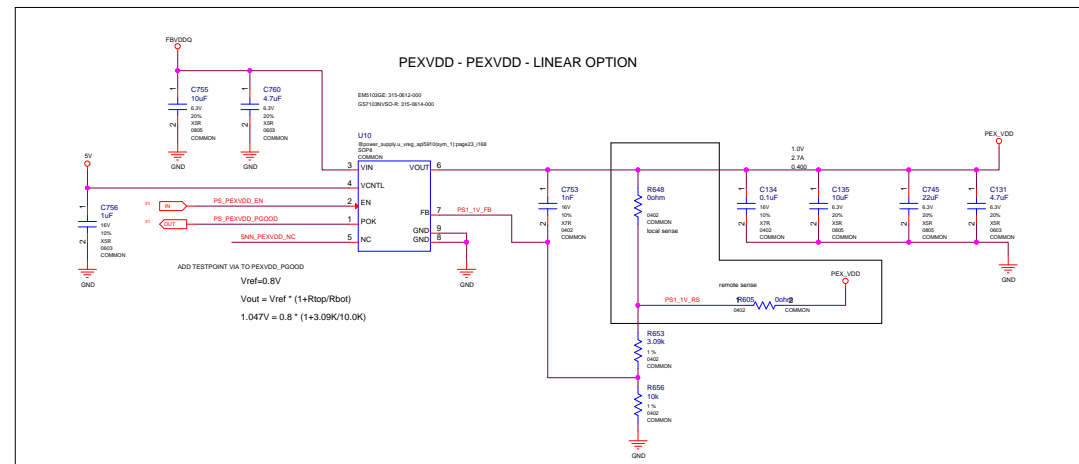
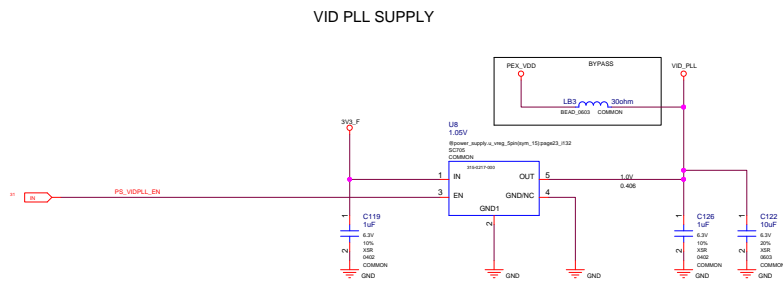
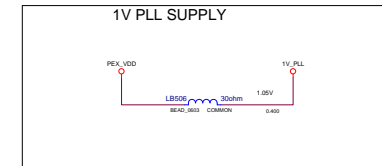
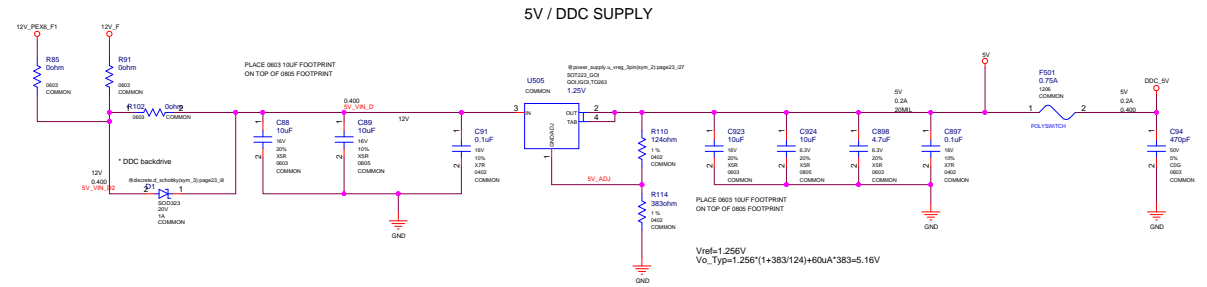
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ASSEMBLY		BASE LEVEL GENERIC SCHEMATIC ONLY	
PAGE DETAIL		MISC2: ROM, XTAL, Straps	
NV_PN		600-1G301-BASE-200	
PCBR REV		PG301-7A02	
BOM REV		A	
PAGE		22 OF 34	
DATE		05-OCT-2014	

PS: 5V, PEX\_VDD

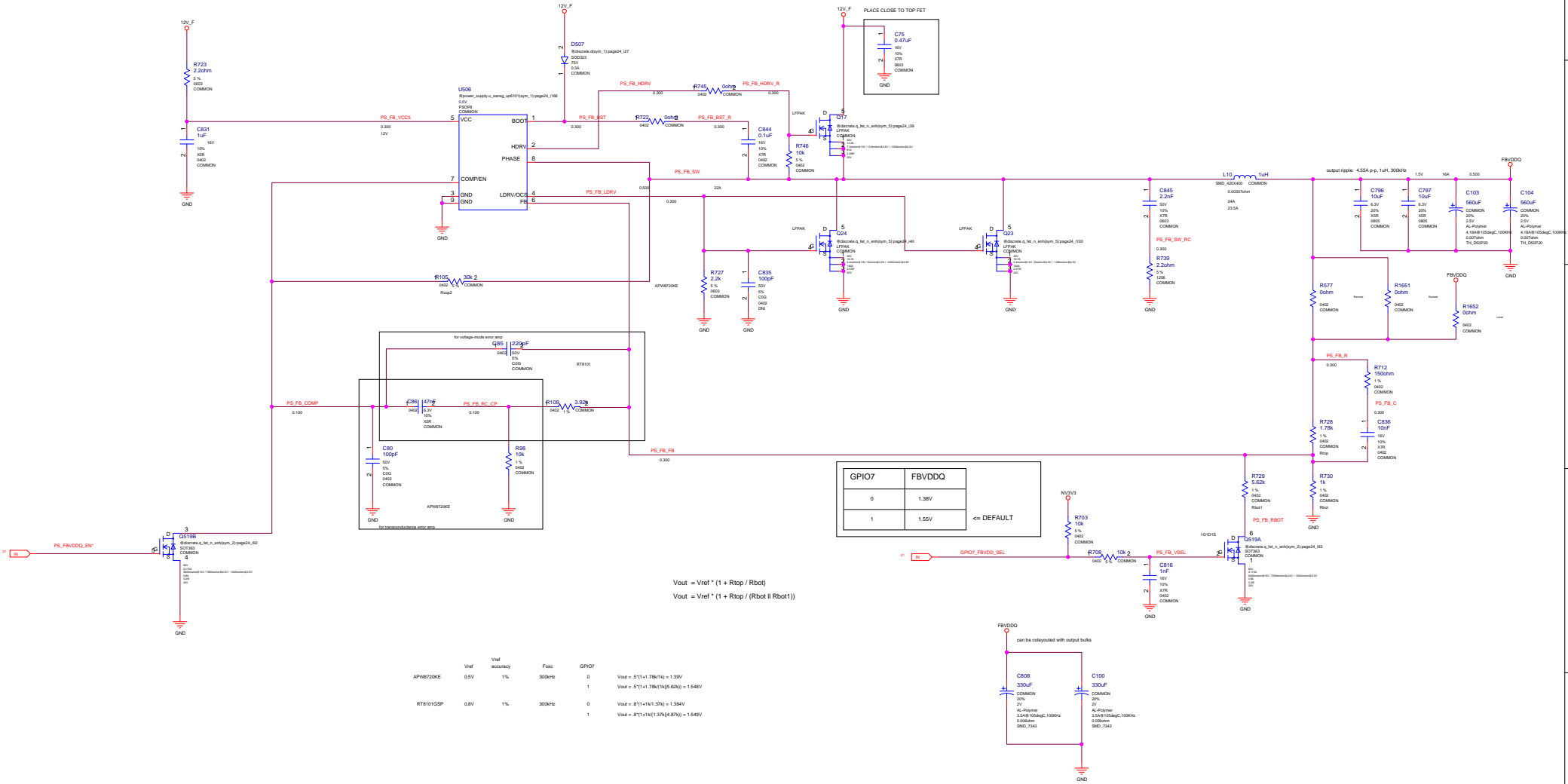


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 5V, PEX_VDD, VID_PLL

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<b>NV_PN</b>	<b>600-1G301-BASE-200</b>		
<b>PCB REV</b>	<b>PG301-A02</b>	<b>PAGE</b>	<b>23 OF 34</b>
<b>BOM REV</b>	<b>A</b>	<b>DATE</b>	<b>09-OCT-2014</b>

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PS: FBVDDQ

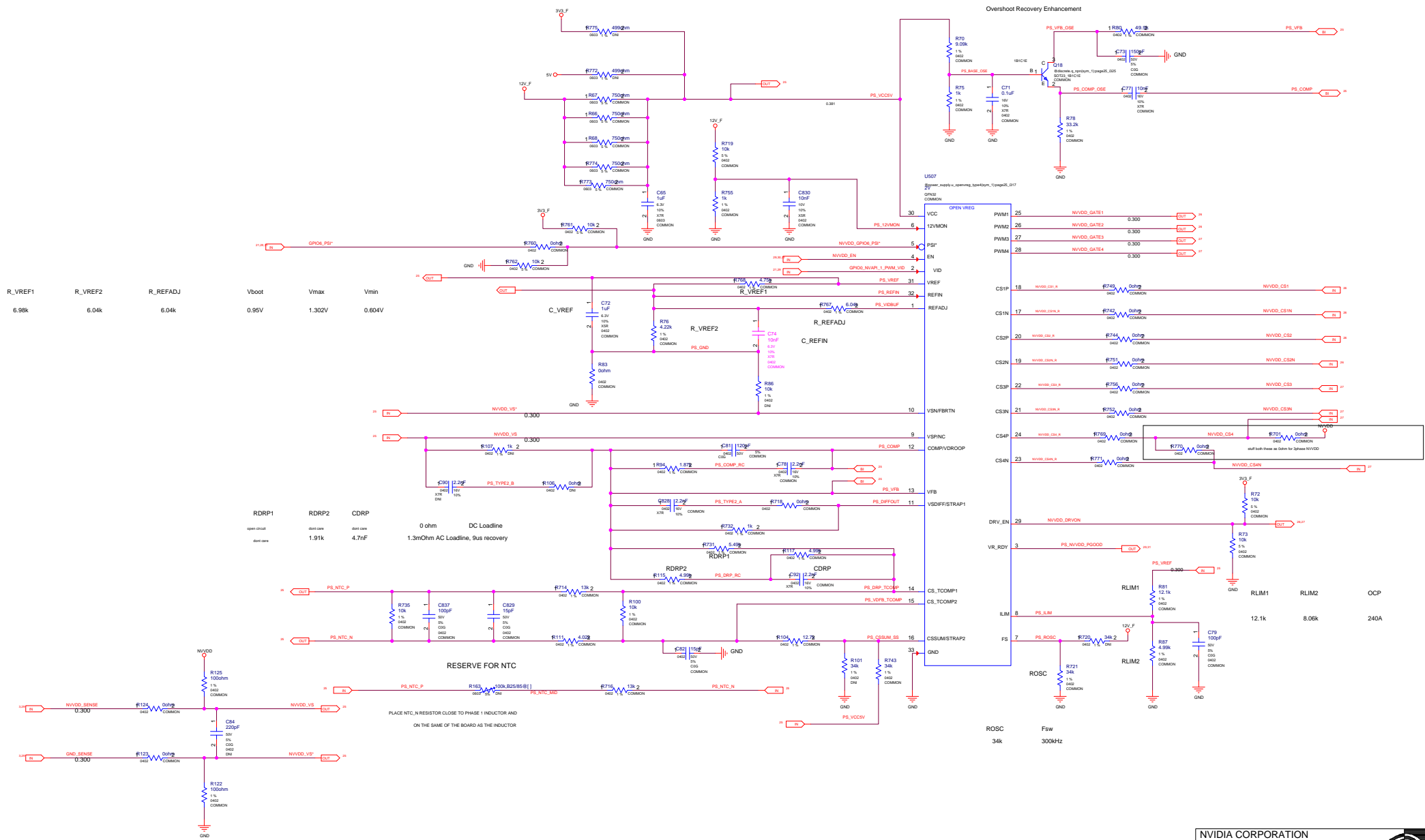


$$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$$
$$V_{out} = V_{ref} * (1 + R_{top} / (R_{bot} || R_{bot1}))$$

	Vref	Vref accuracy	Fosc	GPIO7	
APW8220KE	0.5V	1%	300kHz	0	$V_{out} = 5V * (1 + 78k / 1k) = 1.39V$
				1	$V_{out} = 5V * (1 + 78k / (1k    82k)) = 1.548V$
RT8101GSP	0.8V	1%	300kHz	0	$V_{out} = 8V * (1 + 1k / 1.37k) = 1.384V$
				1	$V_{out} = 8V * (1 + 1k / (1.37k    82k)) = 1.548V$



PS: NVVDD Controller



R_VREF1	R_VREF2	R_REFADJ	Vboot	Vmax	Vmin
6.98k	6.04k	6.04k	0.95V	1.302V	0.604V

RDRP1	RDRP2	CDRP	DC Loadline
0 ohm	1.91k	4.7nF	1.3mOhm AC Loadline, 9us recovery

RESERVE FOR NTC

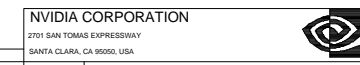
PLACE NTC\_N RESISTOR CLOSE TO PHASE 1 INDUCTOR AND ON THE SAME OF THE BOARD AS THE INDUCTOR

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Controller 0V4 option

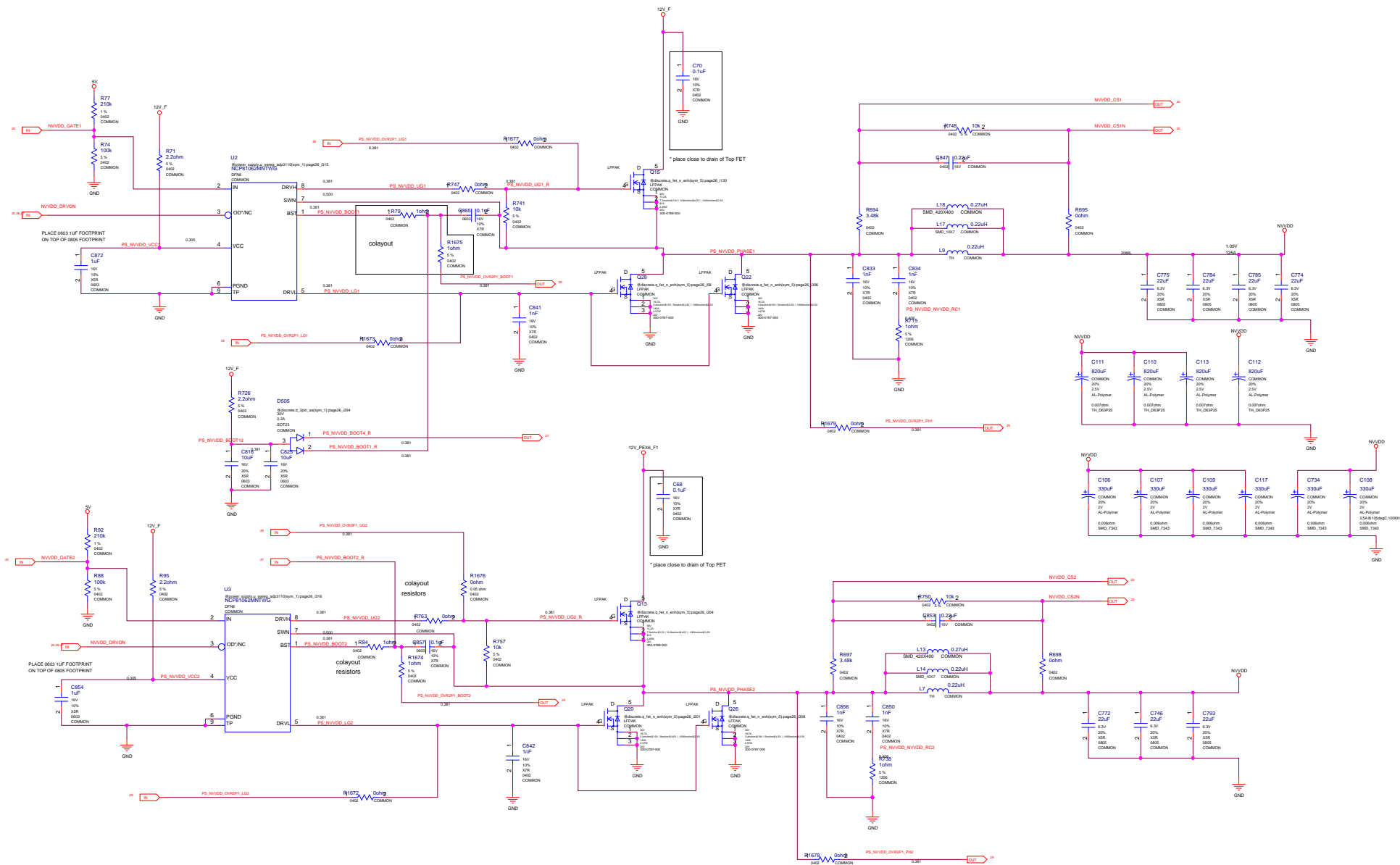
NV_PN	600-1G301-BASE-200
PCB REV	PG301-7A02
BOM REV	A

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## PS: NVVDD Phase 1,2



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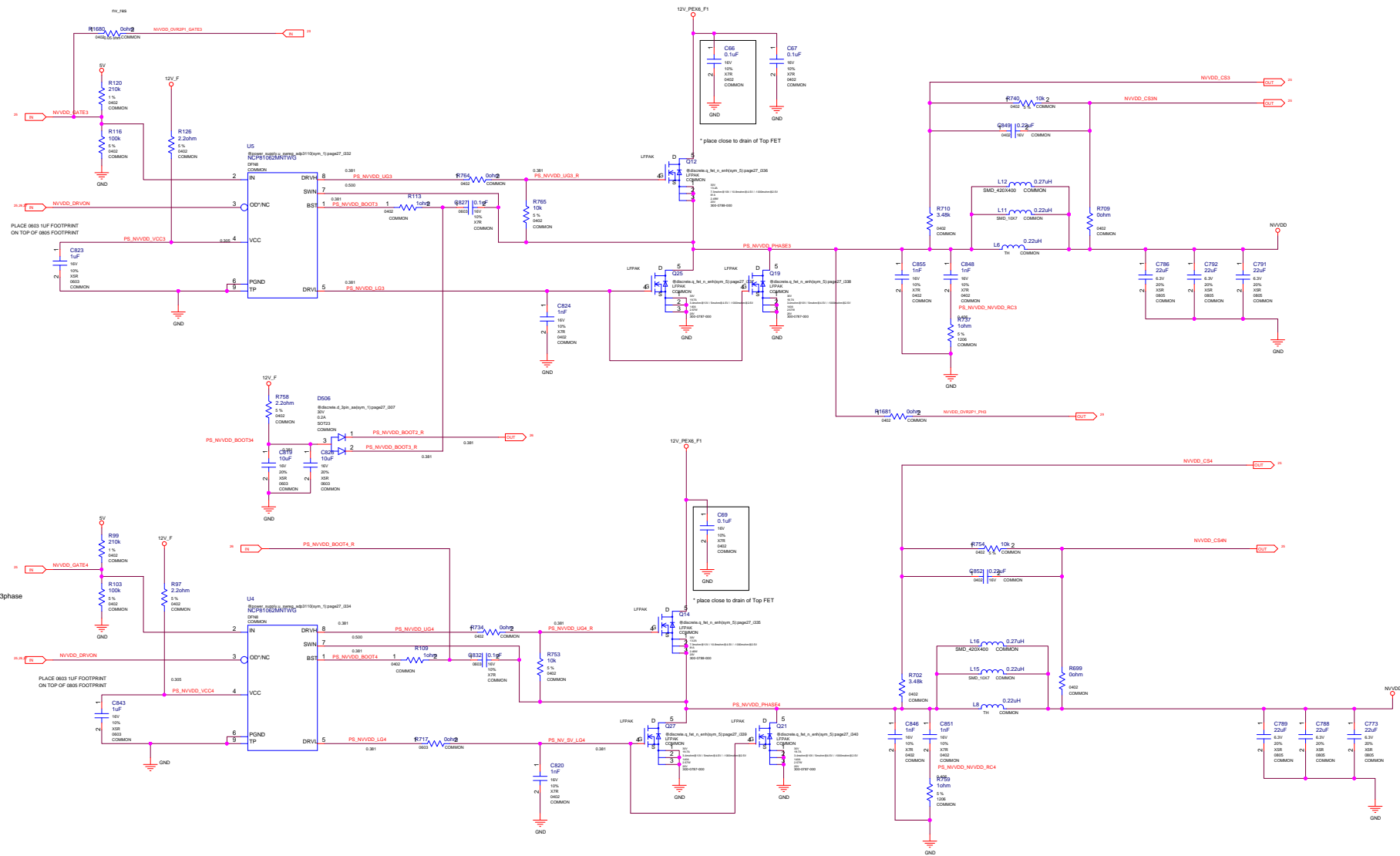
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NV_PN	600-1G301-BASE-200		
PCB REV	PG301-A02	PAGE	26 OF 34
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PS: NVVDD Phase 3,4



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 3,4

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NV_PN	600-1G301-BASE-200		
PCB REV	PG301-A02	PAGE	27 OF 34
BOM REV	A	DATE	09-OCT-2014

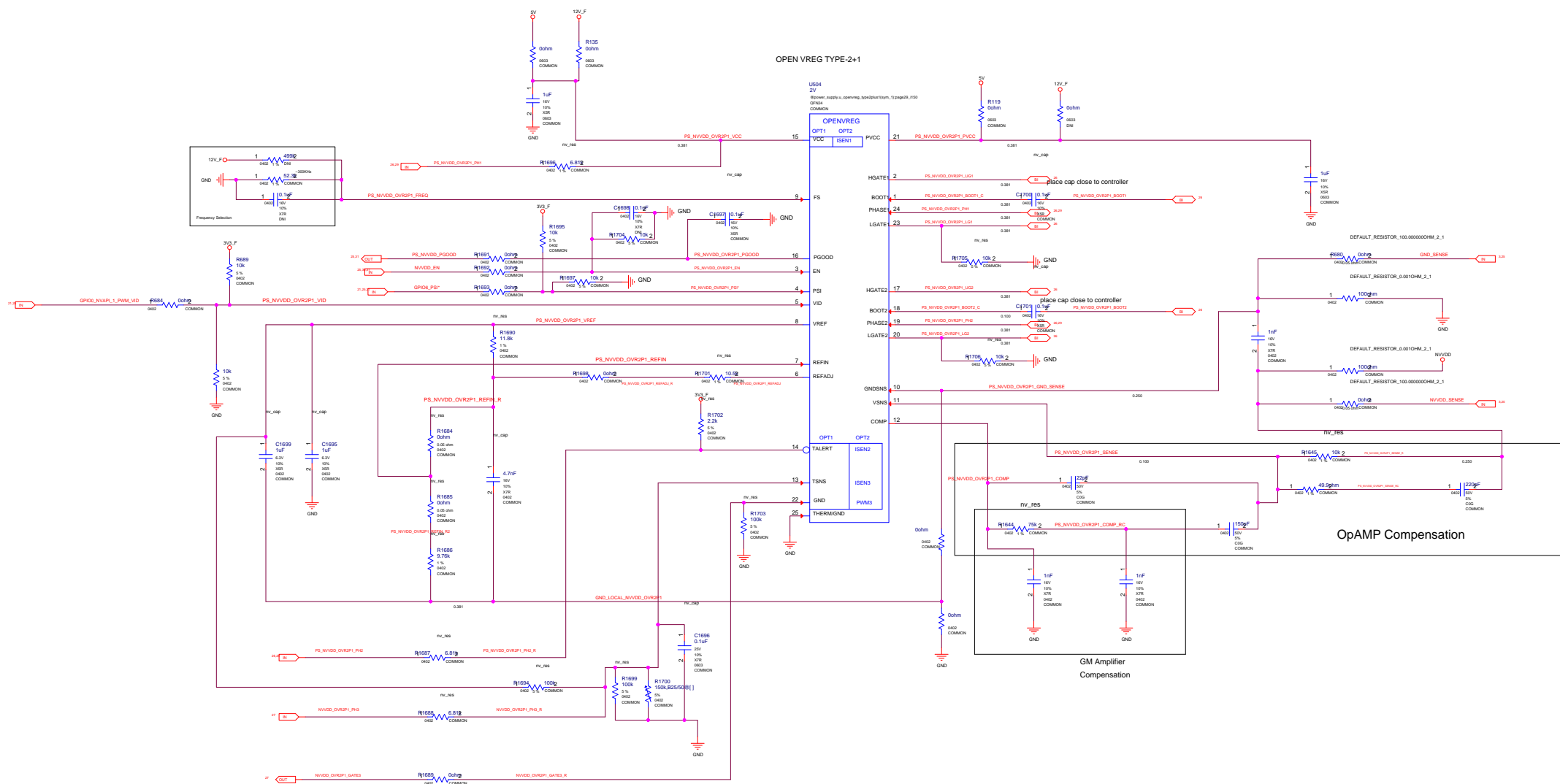
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	(RESERVED)

NV_PN	600-1G301-BASE-200		
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NV_PN	600-1G301-BASE-200		
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## PS: NVVDD OVR2+1 POWER



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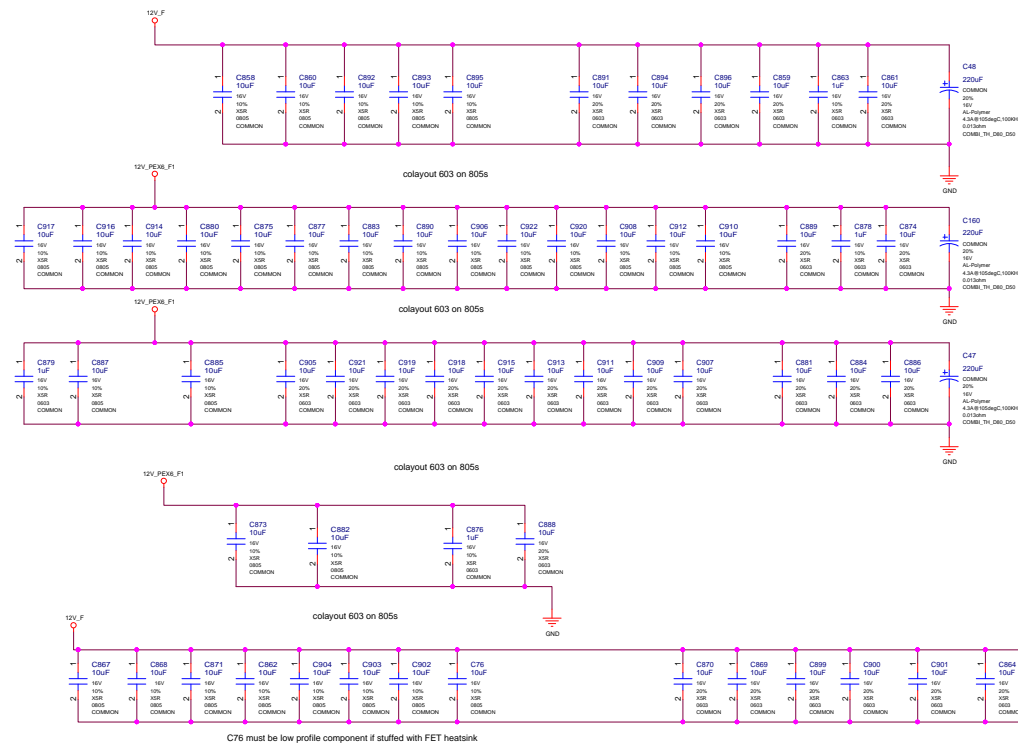
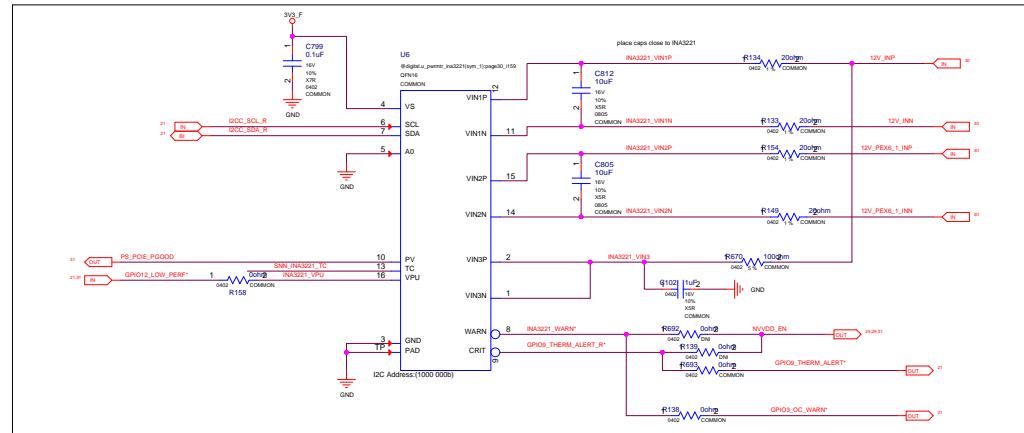
NV_PN	600-1G301-BASE-200
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PCB REV	PG301-A02	PAGE	29 OF 34
BOM REV	A	DATE	09-OCT-2014

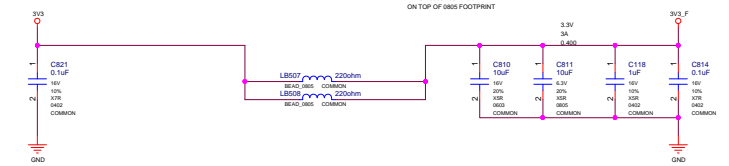
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD OVR2+1 option

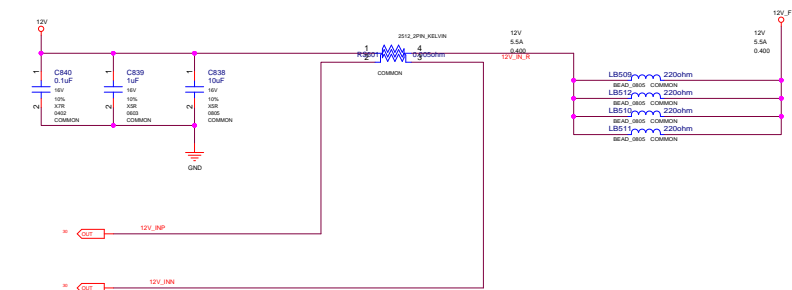
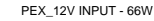
## PS: Inputs, Filtering, and Monitoring



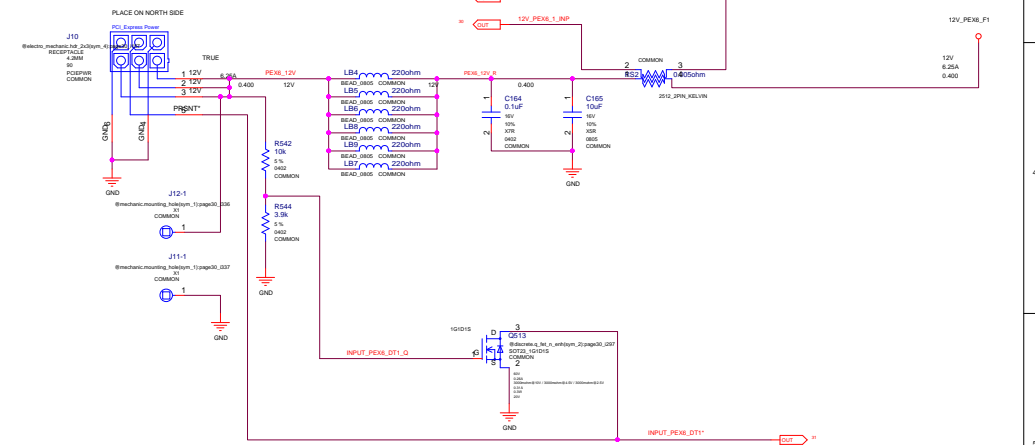
C76 must be low profile component if stuffed with FET heatsink



PLACE 0803 10UF FOOTPRINT  
ON TOP OF THE ELECTROLYTIC



## PEX6 INPUT - 2x3 PCIE CON 75W



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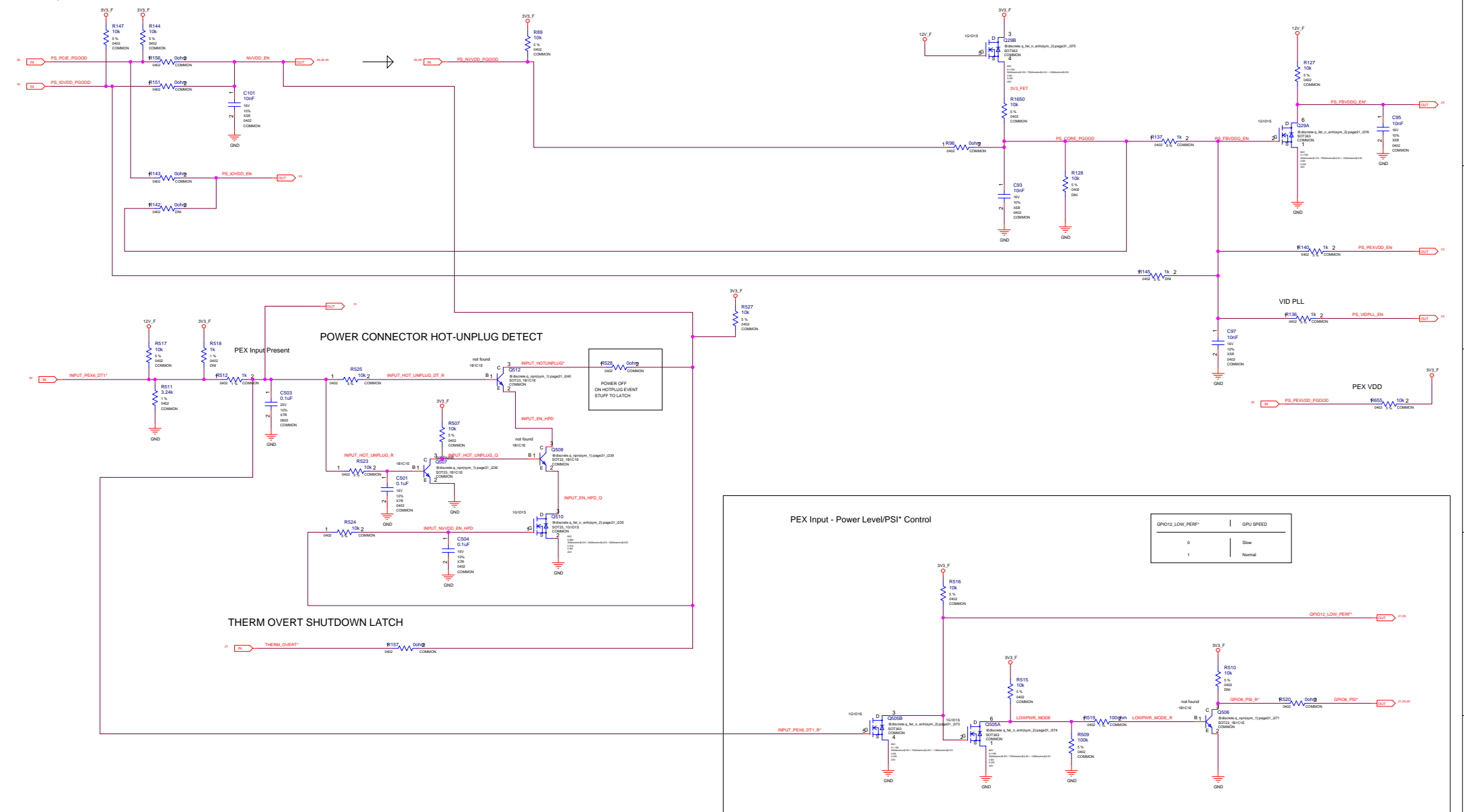


NV_PN	600-1G301-BASE-200
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## PS: Sequence and Shutdown



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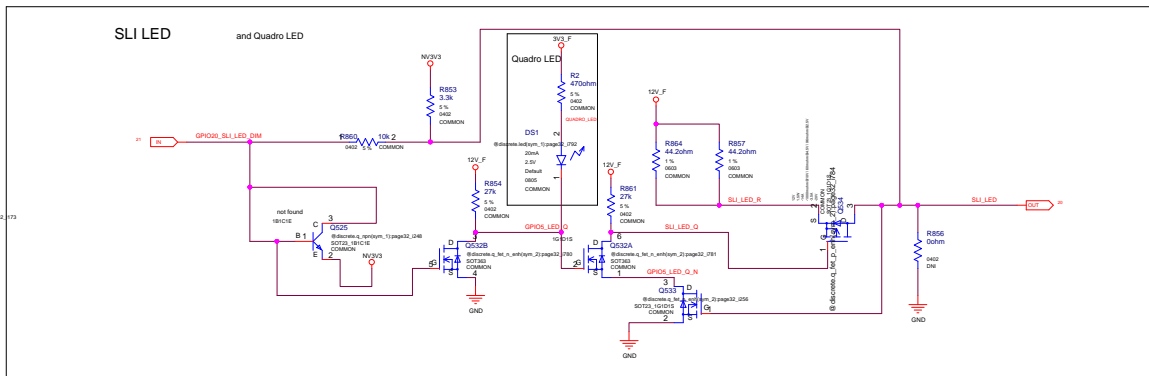
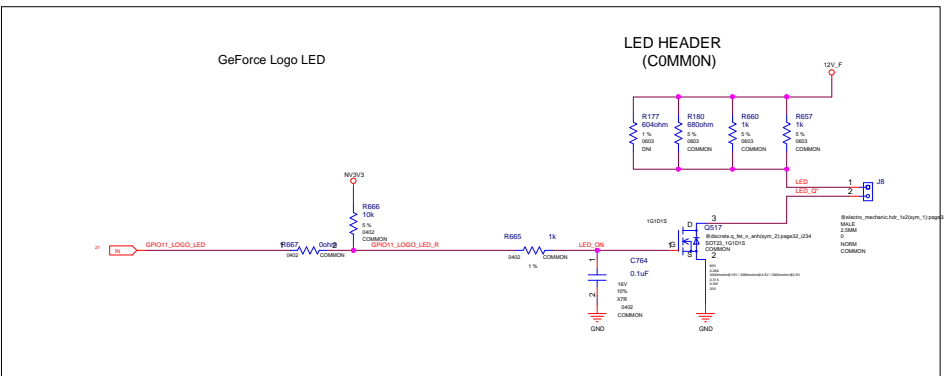
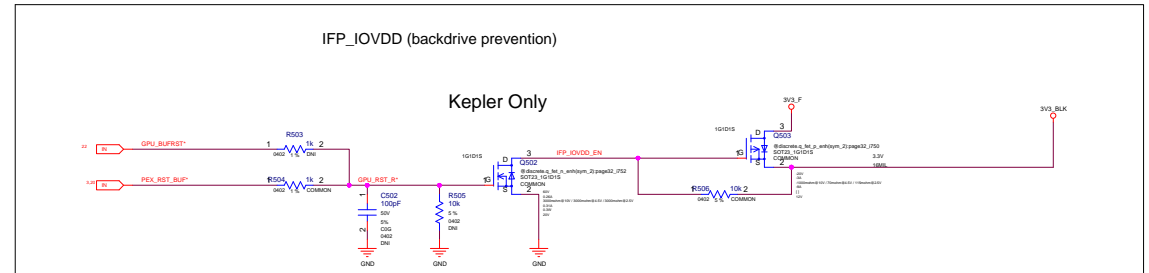


NV_PN	600-1G301-BASE-200
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LEDs



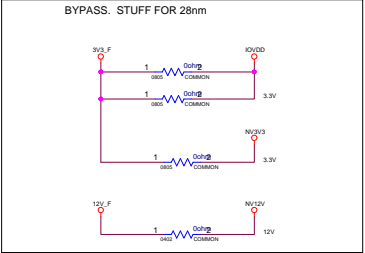
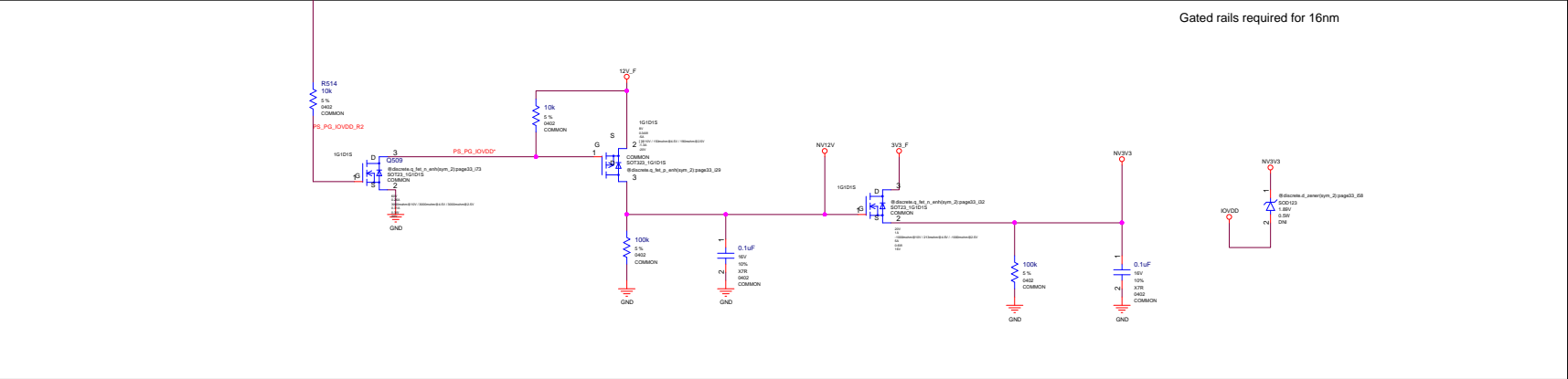
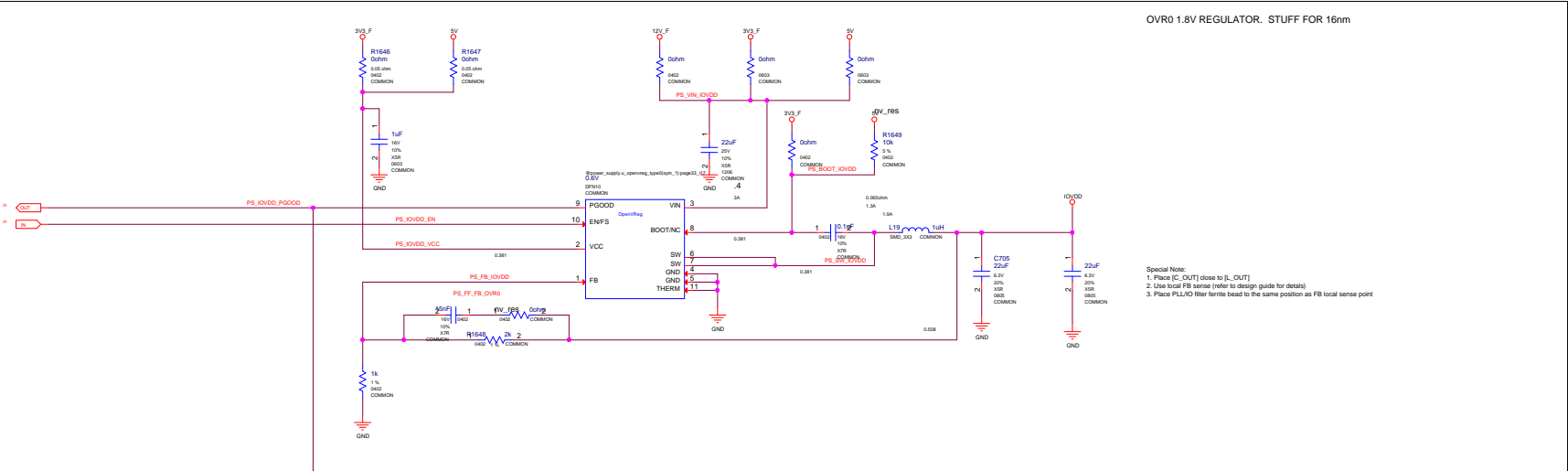
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PAGE DETAIL	LEDs

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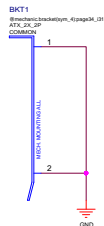
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: IOVDD Regulator

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NV_PN	600-1G301-BASE-200		
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Mechanical: Bracket/Thermal Solution

Brackets:

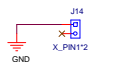


For DVI Connector

DVDVI SCREWS with top tab



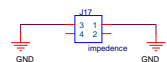
Reserve J3 - J20 for Impedance check



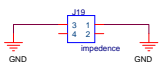
MEM Data  
FBC\_D<9>  
Top  
0.129MM / 47ohm +/- 10%  
Reference L2\_GND



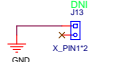
SLU Data  
MDA\_D7  
L3  
0.101MM / 52ohm +/- 10%  
Reference L2\_GND



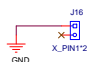
MEM CLK  
FBA\_CLK1/FBA\_CLK1\*  
L3\_Inner  
0.103mm/0.101mm / 80ohm +/- 10%  
Reference L2\_Inner GND



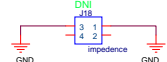
HDMI TMDS signals  
IFPC\_TXC/IFPC\_TXC\*  
L4\_Inner  
0.104mm/0.26mm / 95ohm +/- 10%  
Reference L5\_Inner GND



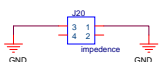
RGB signal  
DACA\_GREEN\_DVI  
Bottom  
0.102MM / 52ohm +/- 10%  
Reference L5\_Inner GND



MEM Address  
FBC\_CMD<4>  
L4  
0.127MM / 47ohm +/- 10%  
Reference L5\_GND



PEX\_PCEI / DVI IFPEF  
PEX\_RX13/PEX\_RX13\* IFPEF\_TXC\_C\*\_R/IFPEF\_TXC\_C\*\_R  
TOP  
0.101MM/0.123MM / 90ohm +/- 10%  
Reference L2\_Inner GND



PEX\_PCEI / DVI IFPAB  
PEX\_TX6/PEX\_TX6\* IFPAB\_TXD1\_C\*\_R/IFPAB\_TXD1\_C\*\_R  
Bottom  
0.101MM/0.123MM / 90ohm +/- 10%  
Reference L5\_Inner GND



F\_PAD\_X  
F\_SW\_FB



F\_PAD\_X  
F\_SW\_FB



F\_PAD\_X  
F\_SW\_FB



F\_PAD\_X  
F\_SW\_FB



F\_PAD\_X  
F\_SW\_FB



F\_PAD\_X  
F\_SW\_FB

FET H6

COOLING SOLUTION



MEC1  
Branch:mech/bracket/200\_2/page04\_40  
PWB  
COMMON

MEC2-15  
Branch:mech/bracket/200\_2/page04\_41  
PWB  
COMMON

MEC2-14  
Branch:mech/bracket/200\_2/page04\_42  
PWB  
COMMON

MEC2-13  
Branch:mech/bracket/200\_2/page04\_43  
PWB  
COMMON

MEC2-12  
Branch:mech/bracket/200\_2/page04\_45  
PWB  
COMMON

MEC2-11  
Branch:mech/bracket/200\_2/page04\_46  
PWB  
COMMON

MEC2-10  
Branch:mech/bracket/200\_2/page04\_47  
PWB  
COMMON

MEC2-9  
Branch:mech/bracket/200\_2/page04\_48  
PWB  
COMMON

MEC2-8  
Branch:mech/bracket/200\_2/page04\_49  
PWB  
COMMON

MEC2-7  
Branch:mech/bracket/200\_2/page04\_50  
PWB  
COMMON

MEC2-6  
Branch:mech/bracket/200\_2/page04\_51  
PWB  
COMMON

MEC2-5  
Branch:mech/bracket/200\_2/page04\_52  
PWB  
COMMON

MEC2-4  
Branch:mech/bracket/200\_2/page04\_53  
PWB  
COMMON

MEC2-3  
Branch:mech/bracket/200\_2/page04\_54  
PWB  
COMMON

MEC2-2  
Branch:mech/bracket/200\_2/page04\_55  
PWB  
COMMON

MEC2-1  
Branch:mech/bracket/200\_2/page04\_56  
PWB  
COMMON

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DATE 05-OCT-2014

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