

PG150-C03

384b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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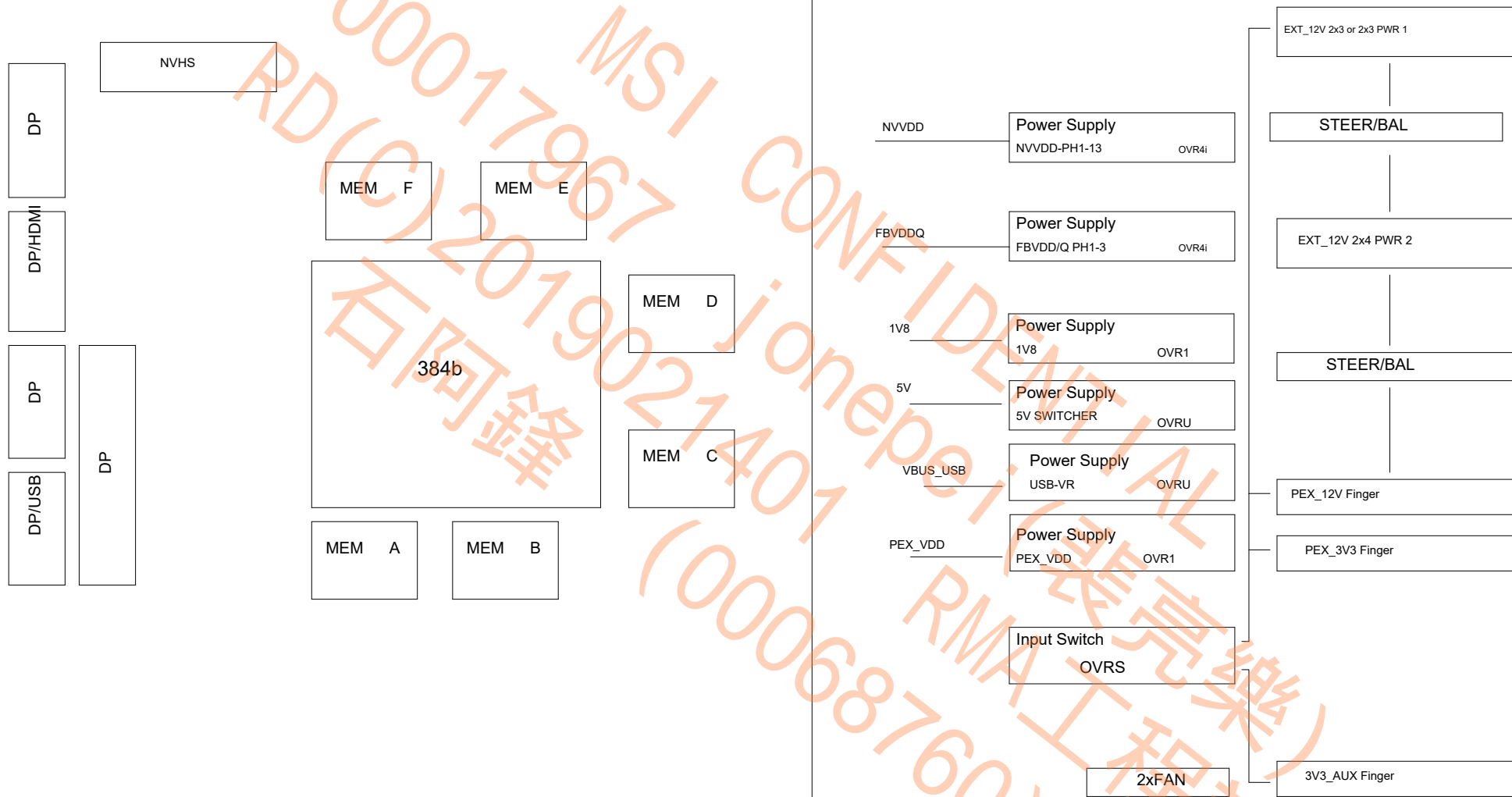
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Block Diagram



PCI Express



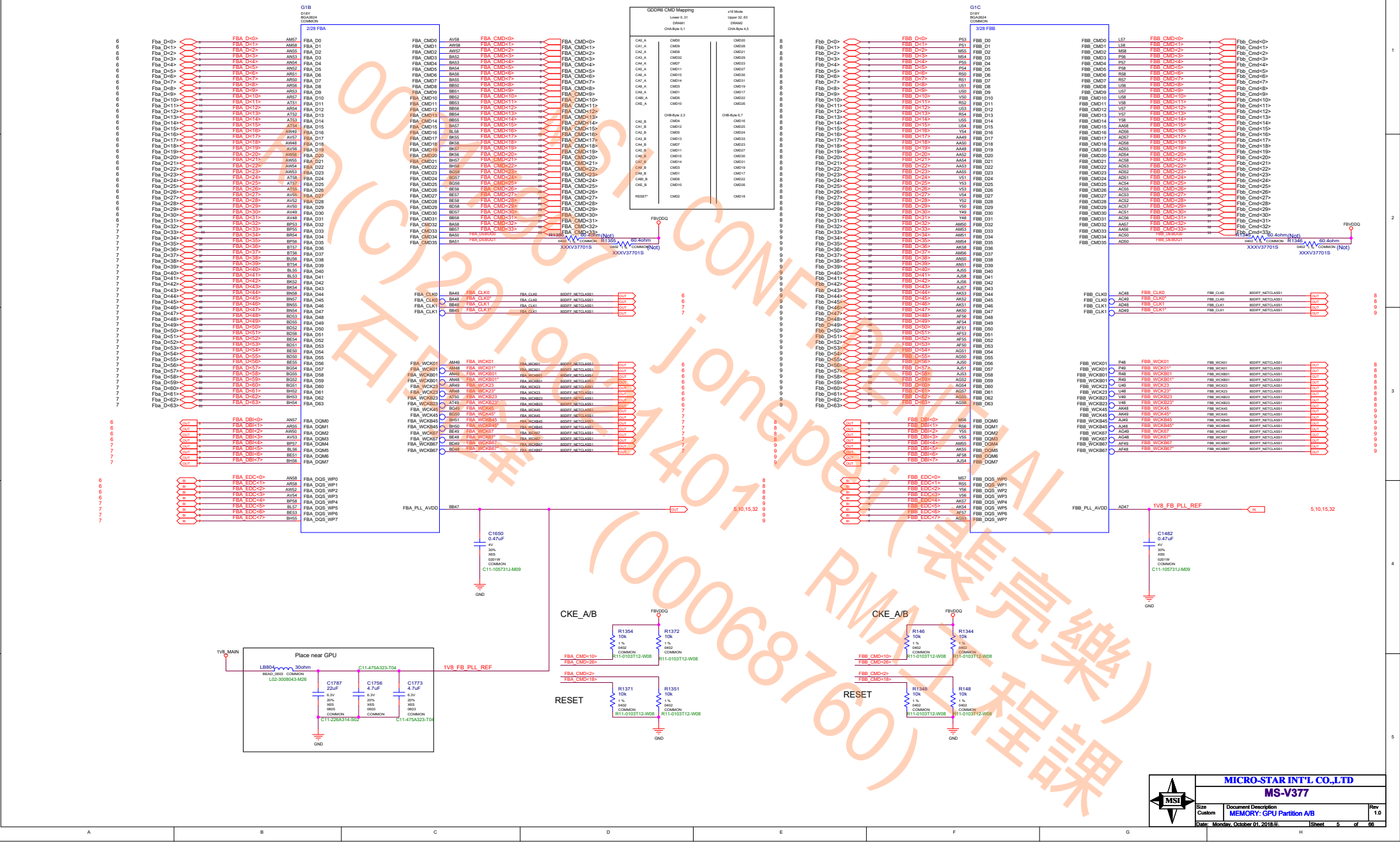
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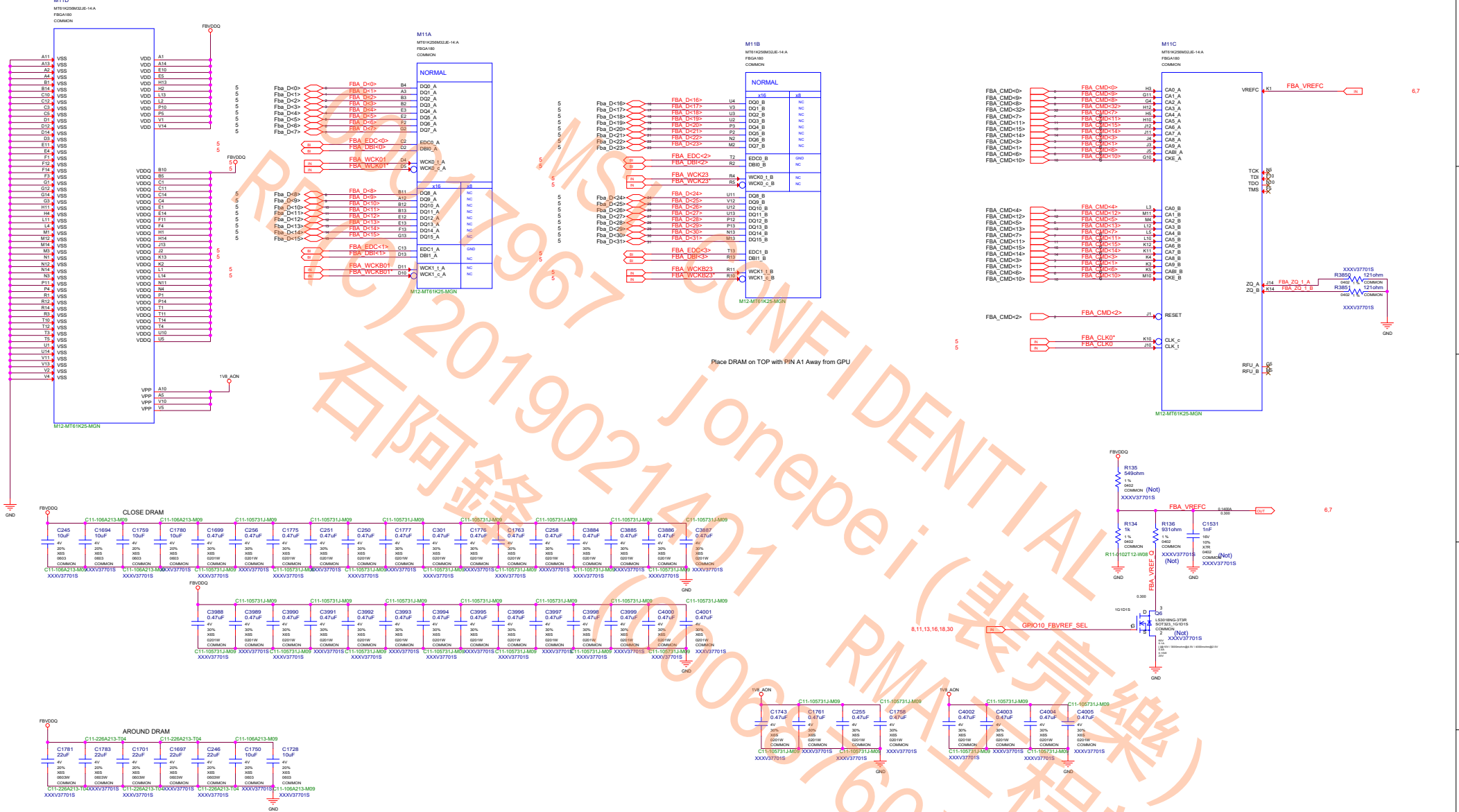
PCI TERM

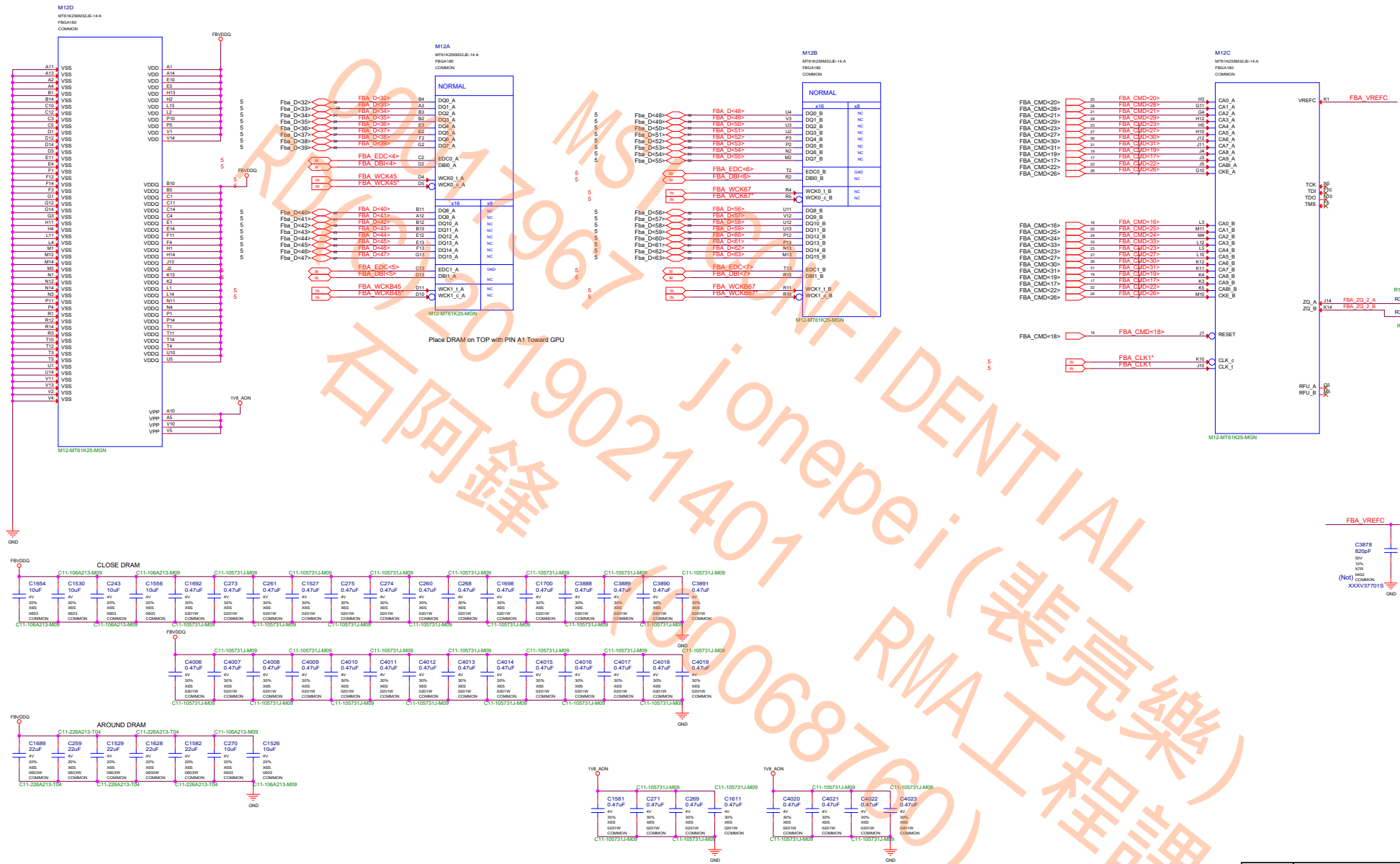


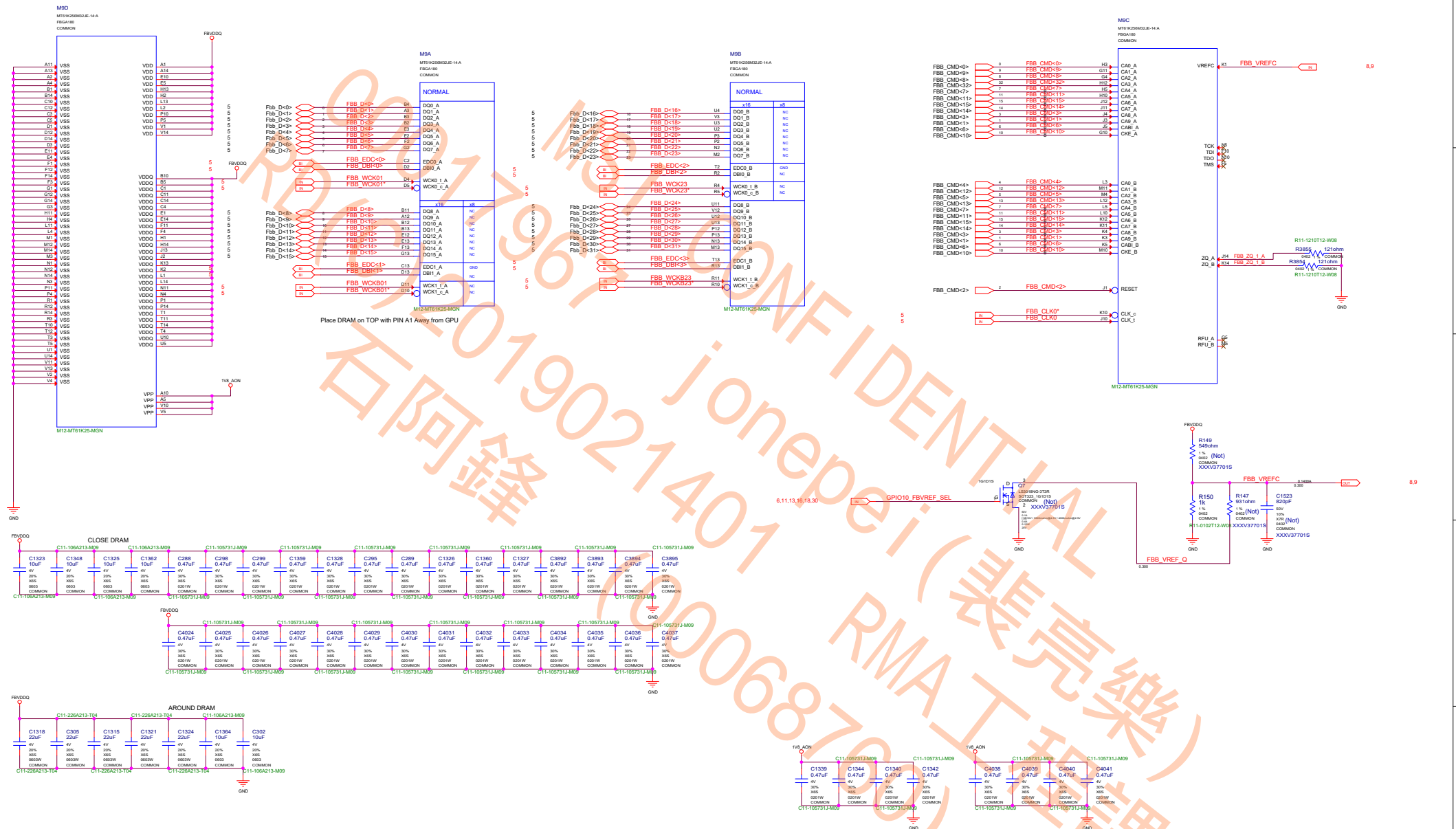
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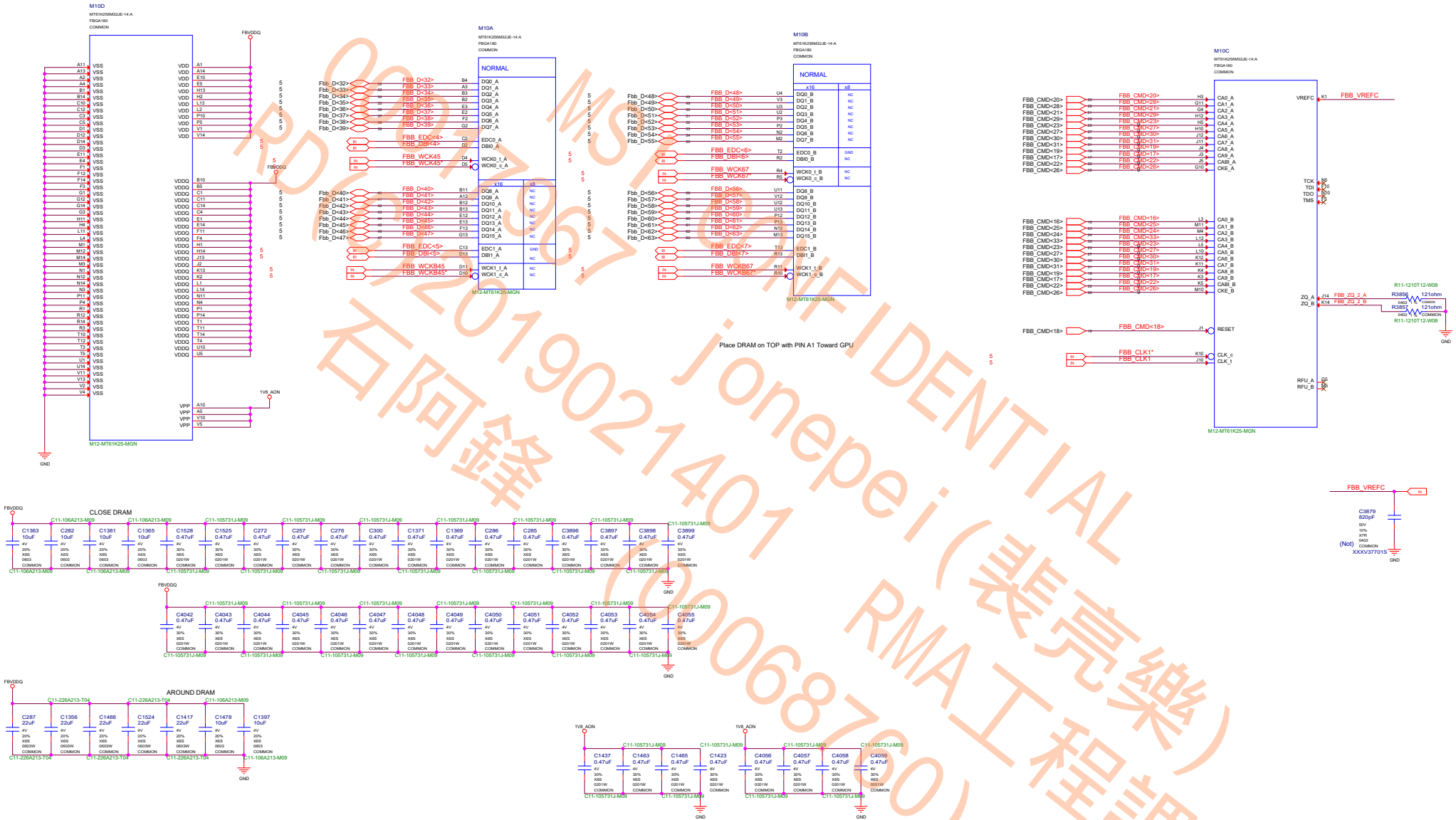


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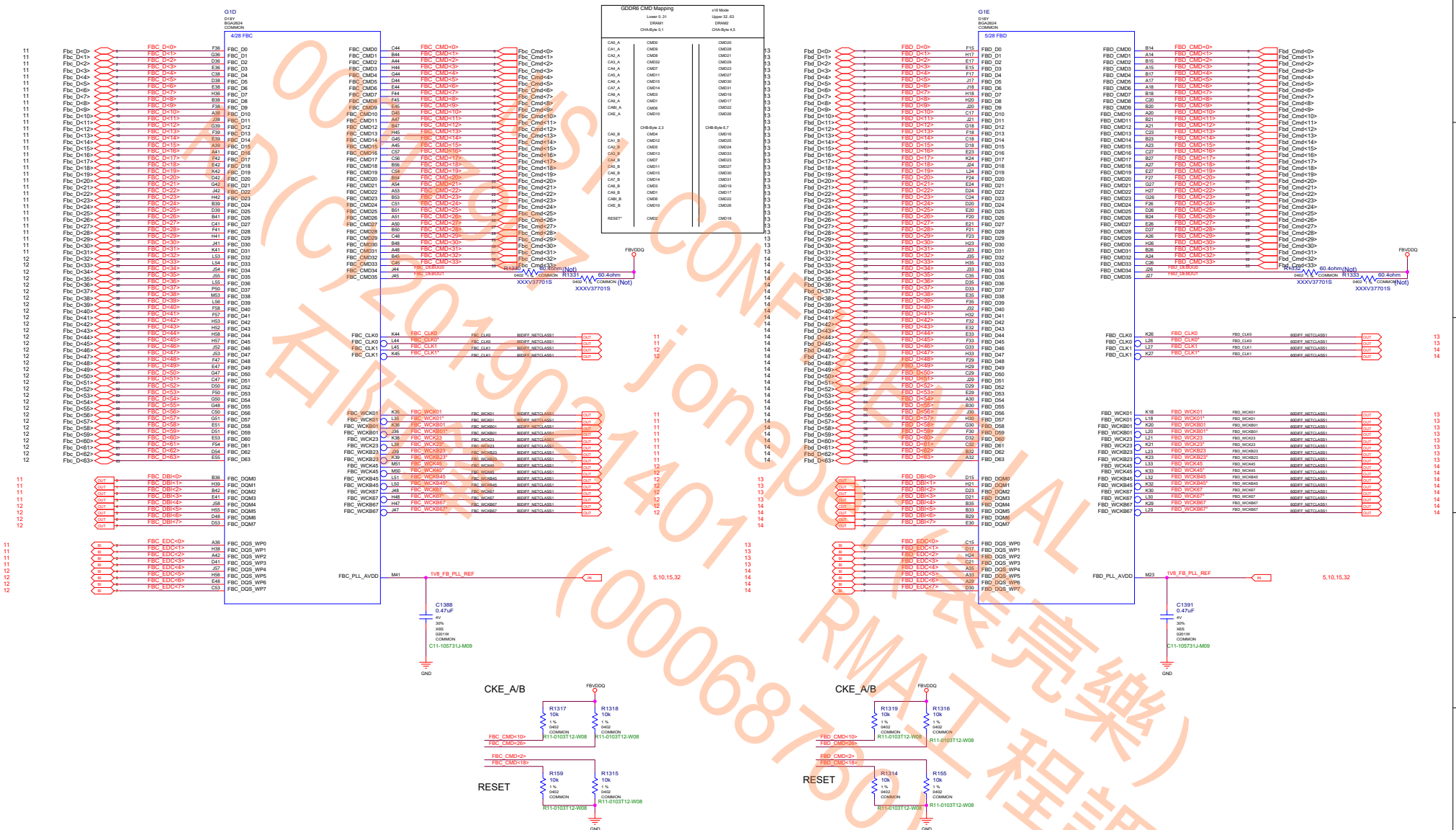




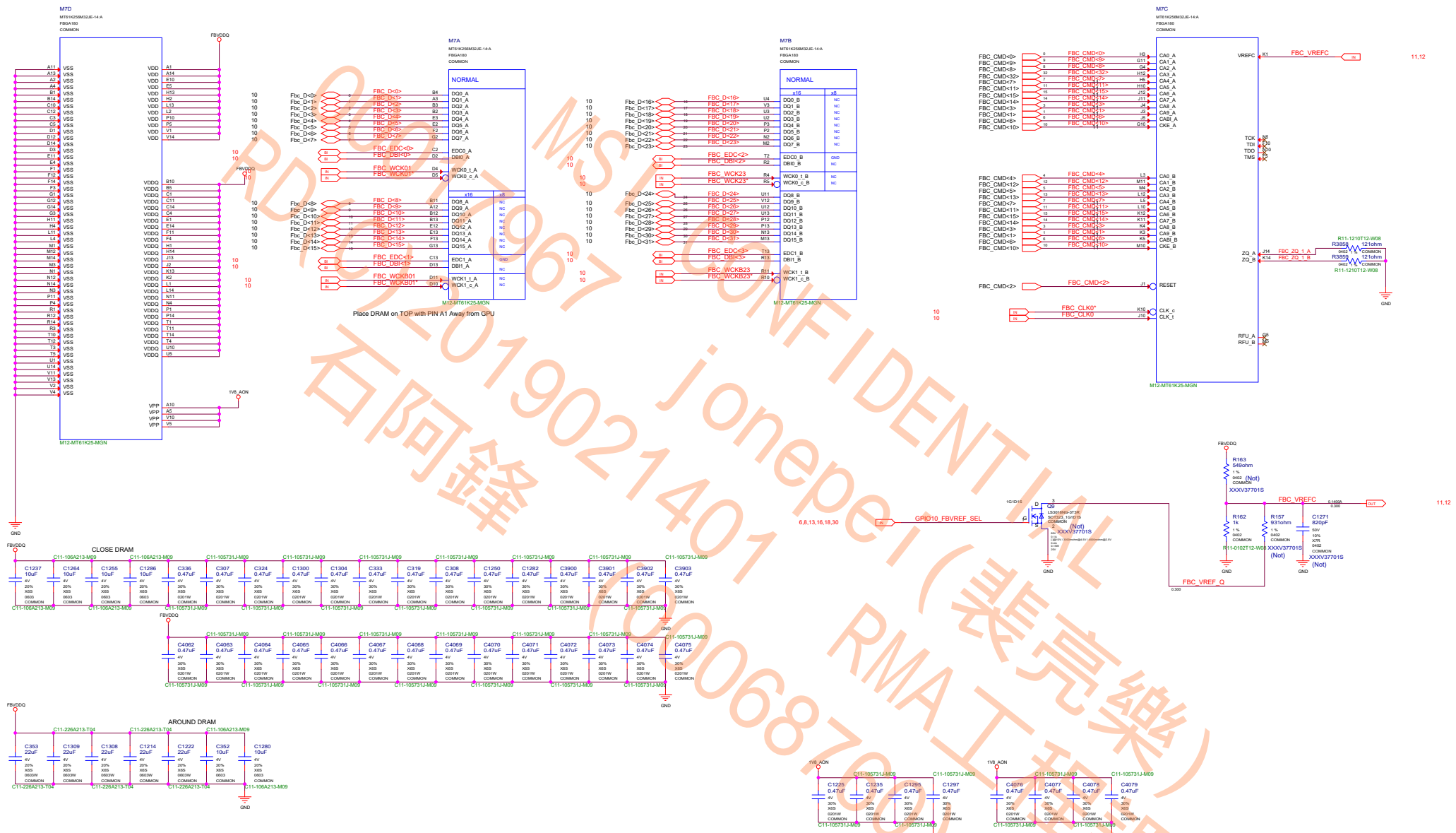




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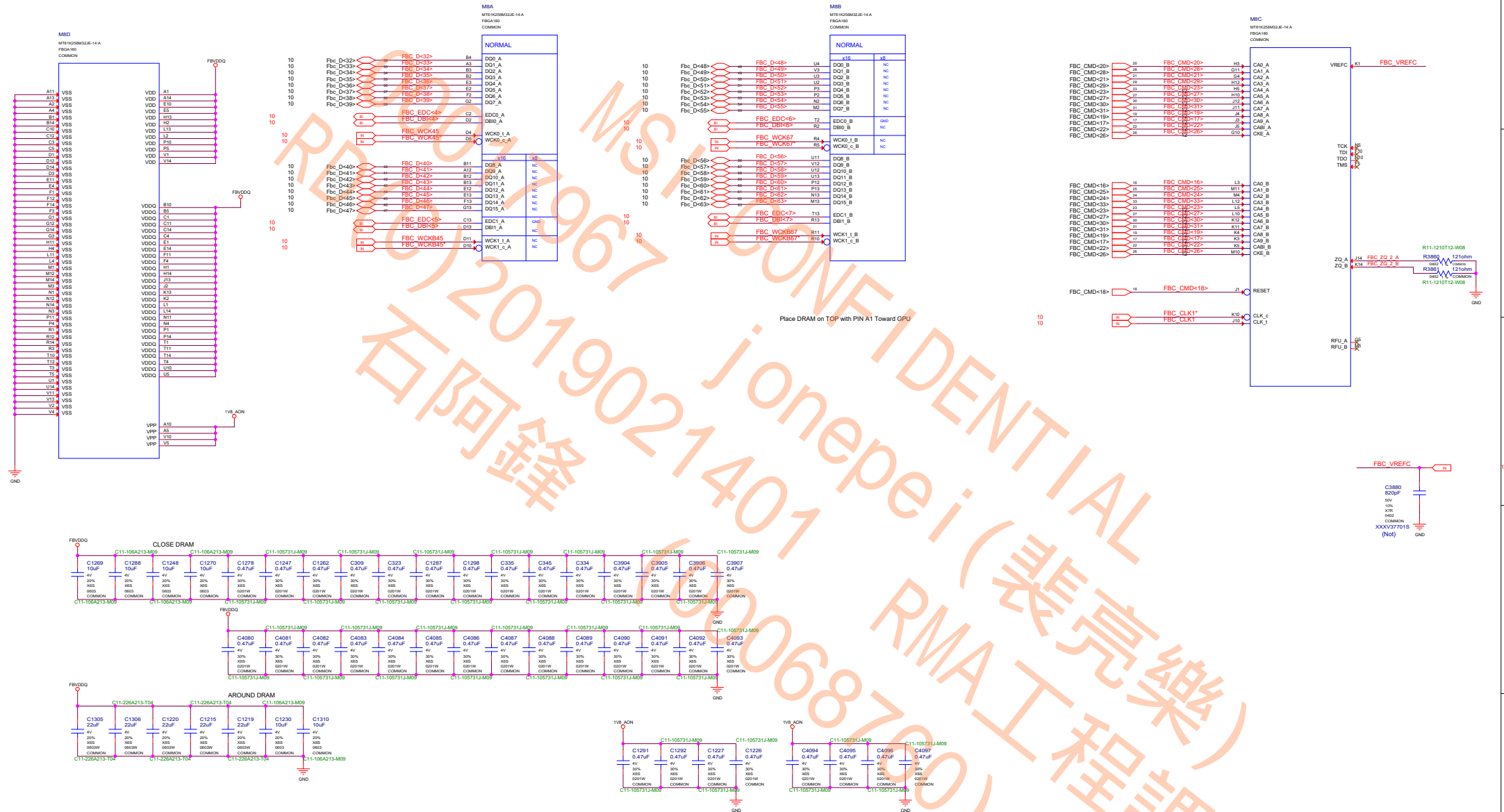


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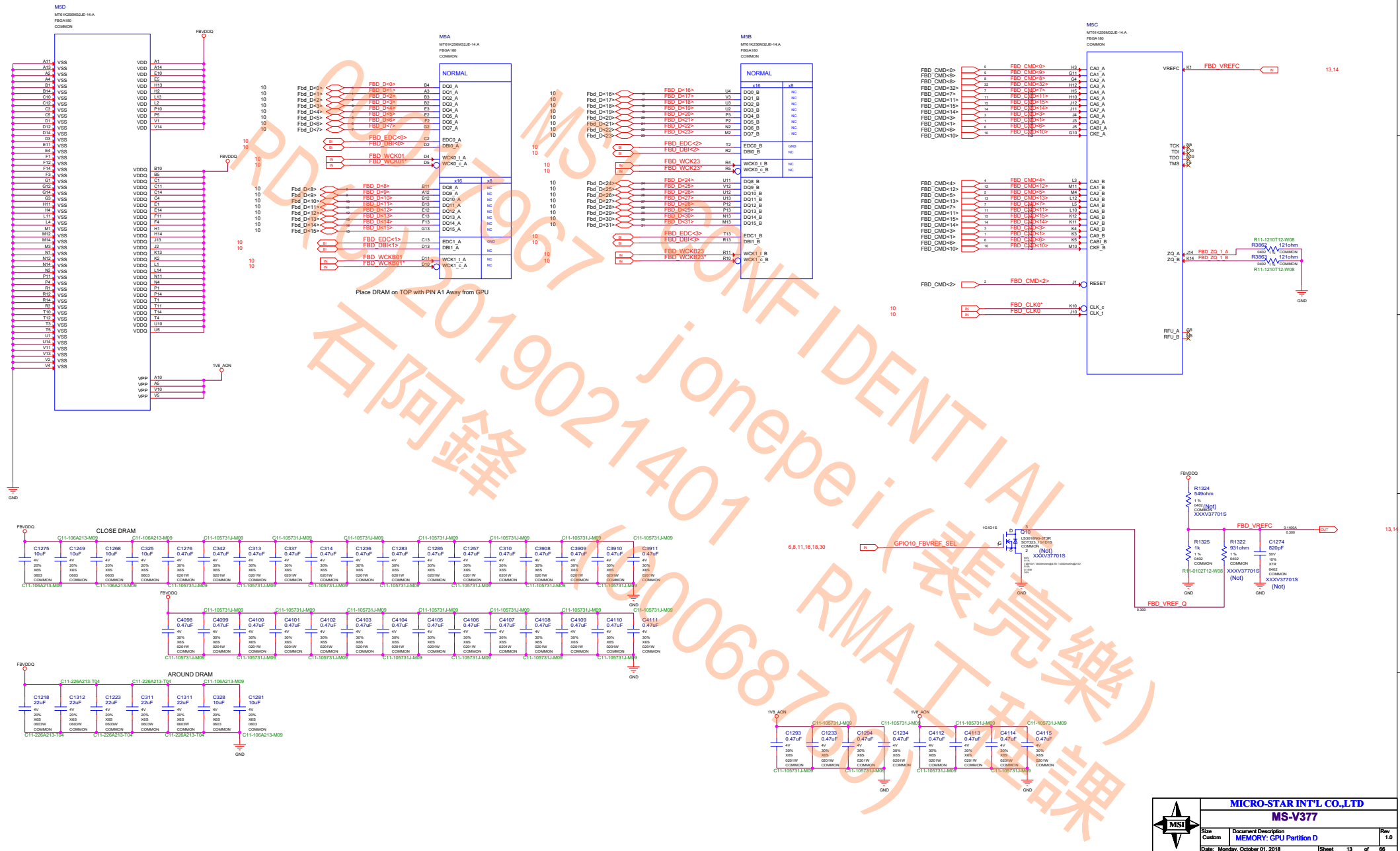


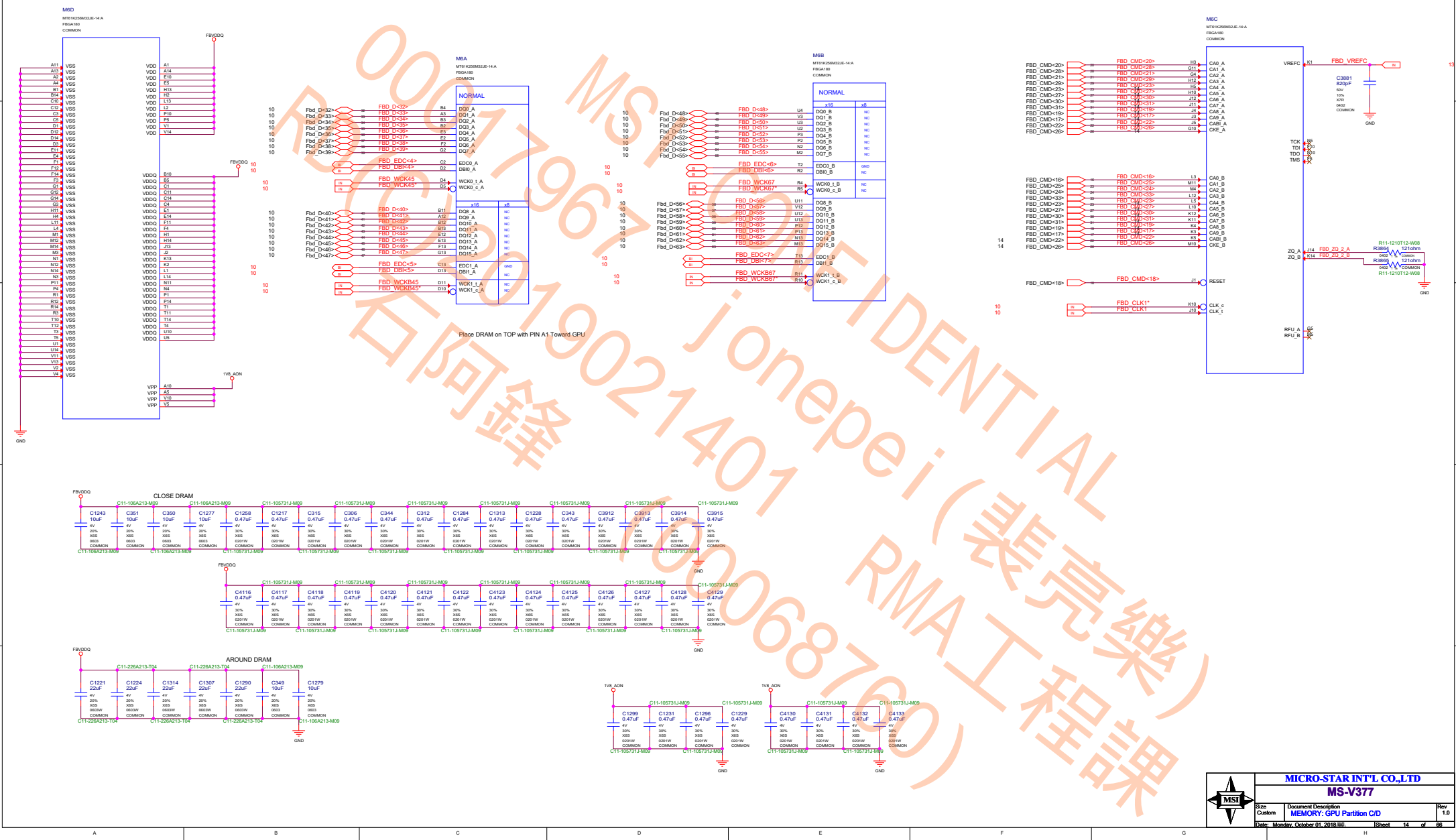
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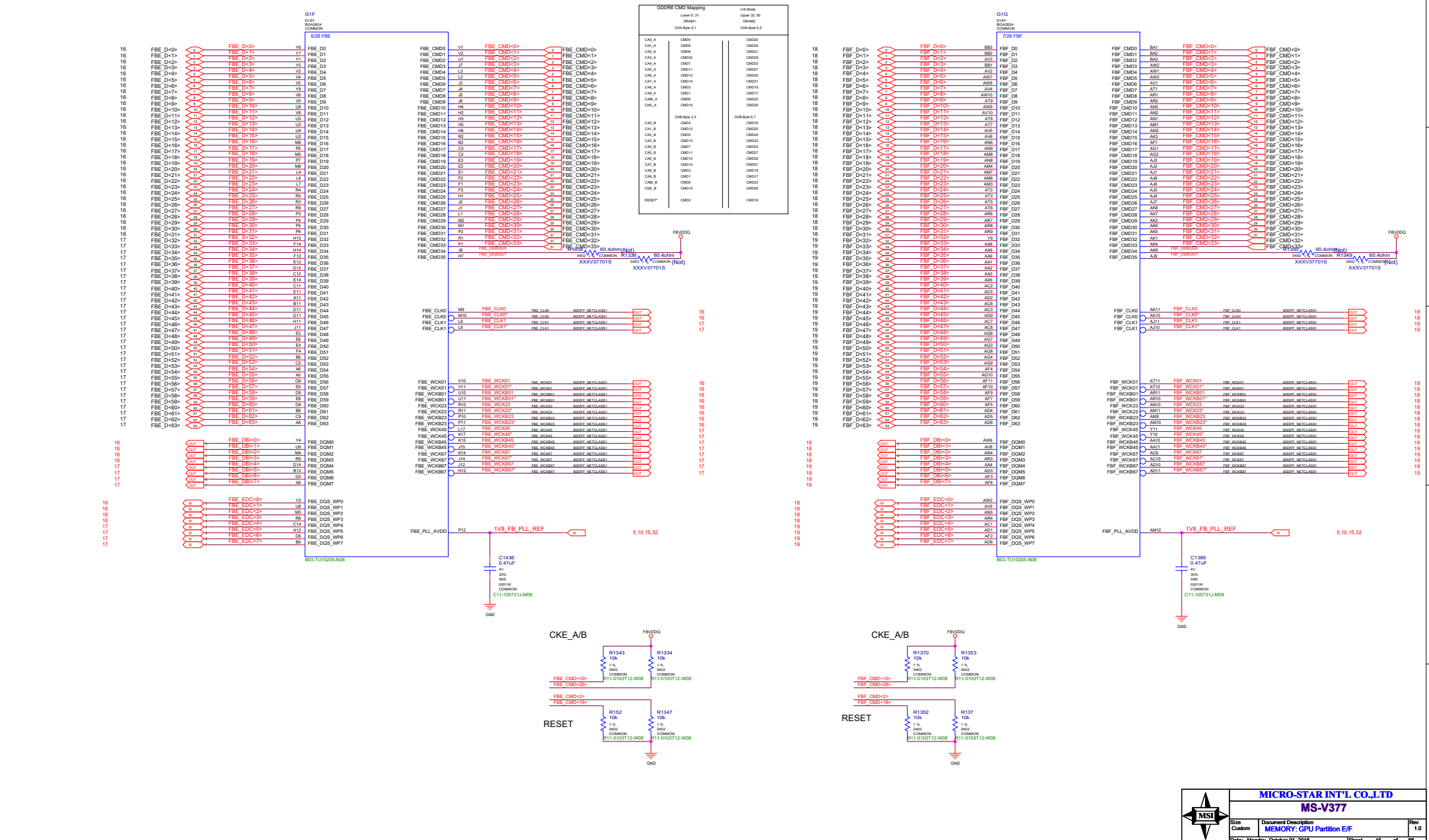
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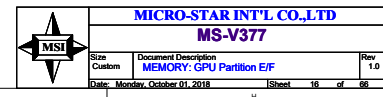
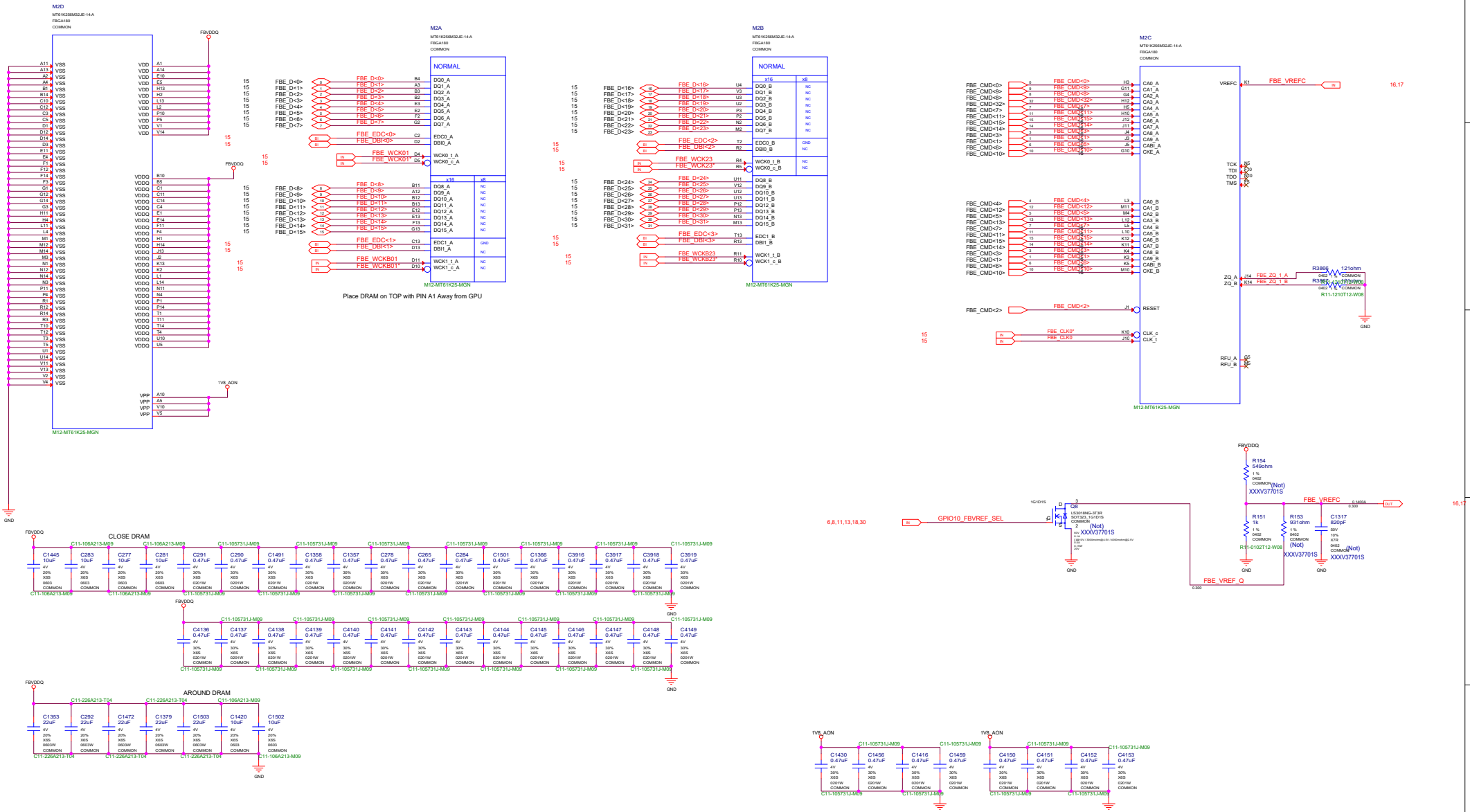
MEMORY: FBD Partition 31.0



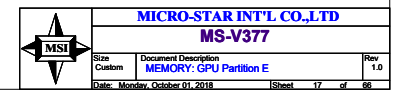
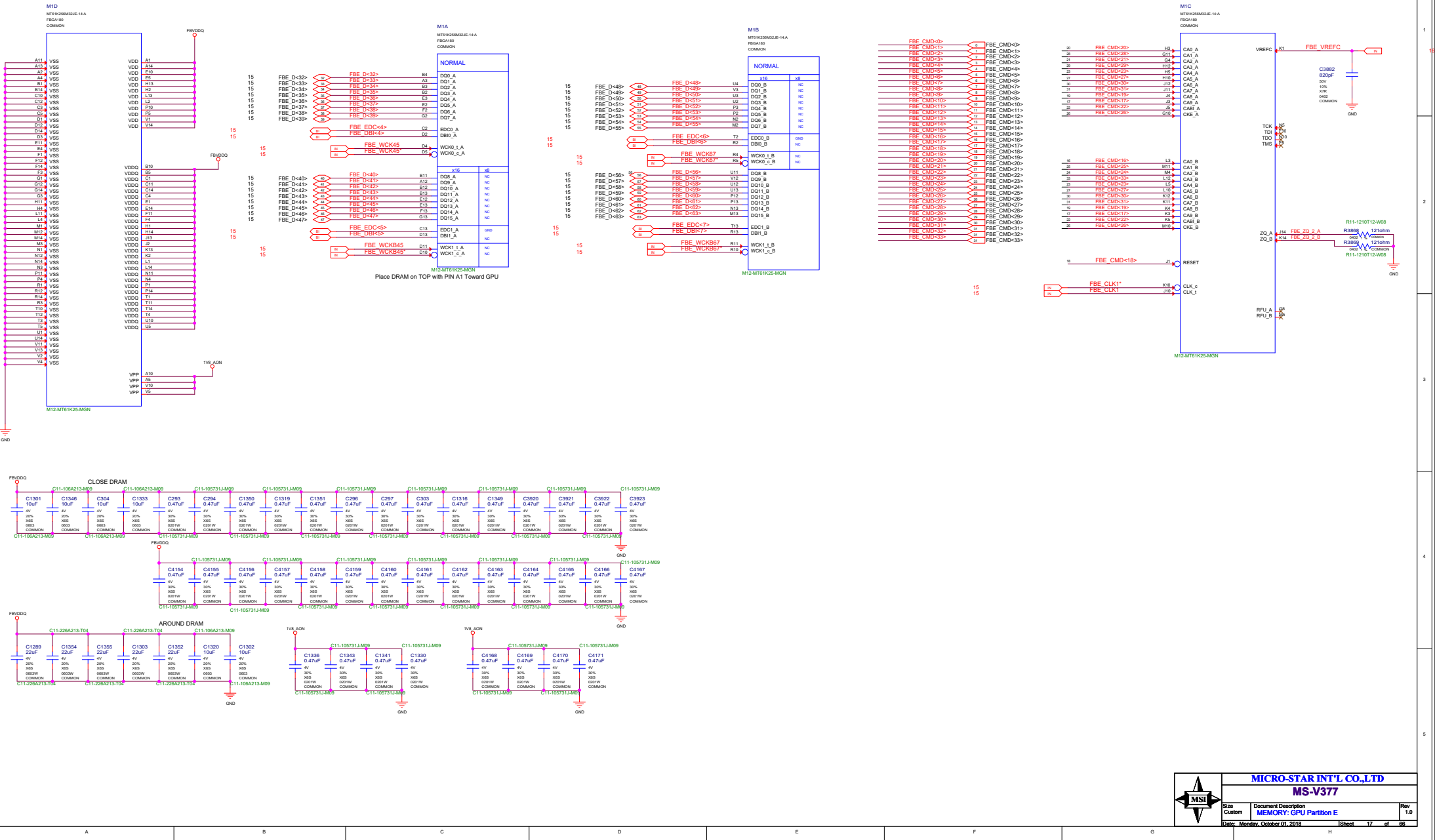




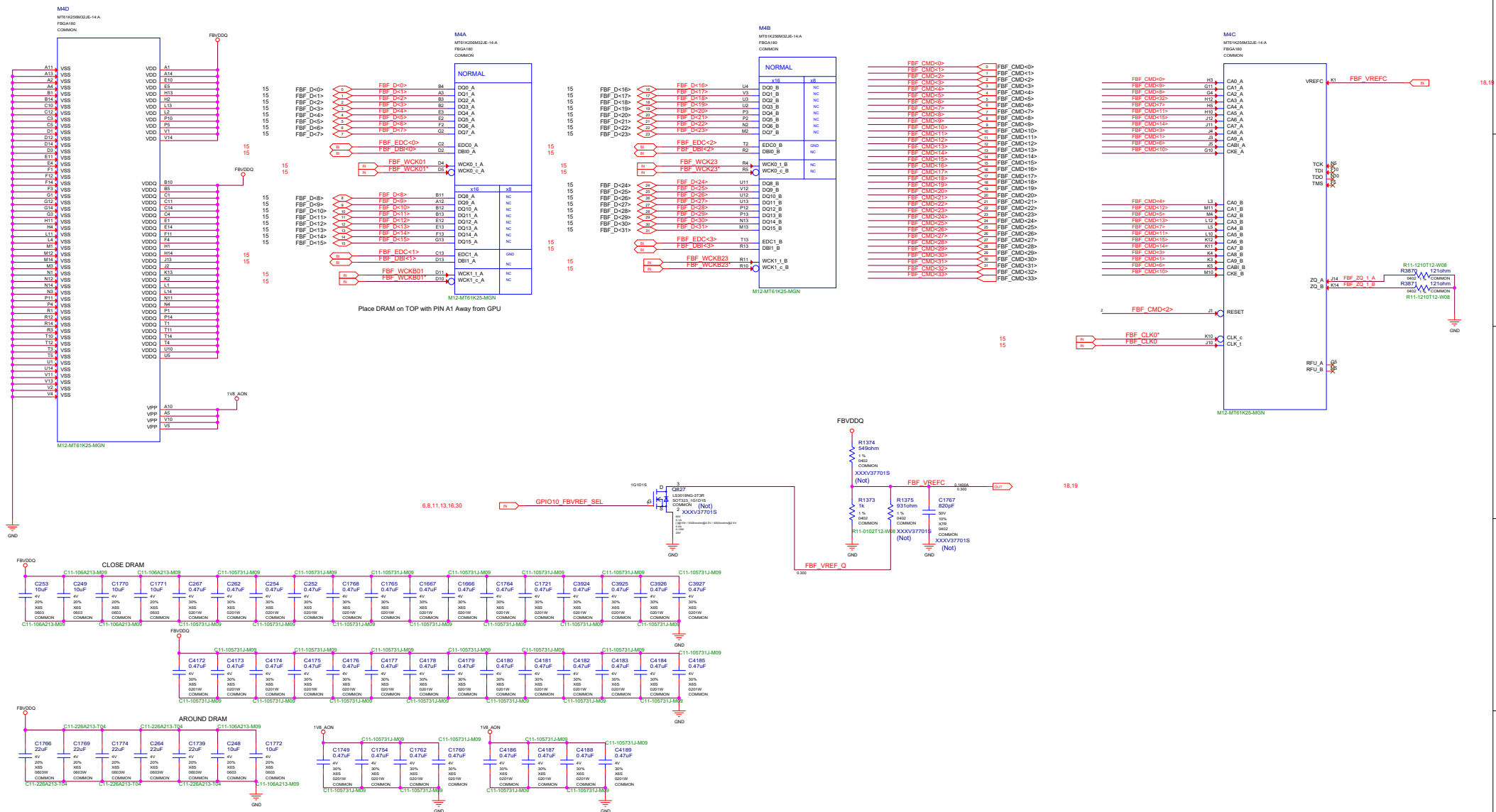
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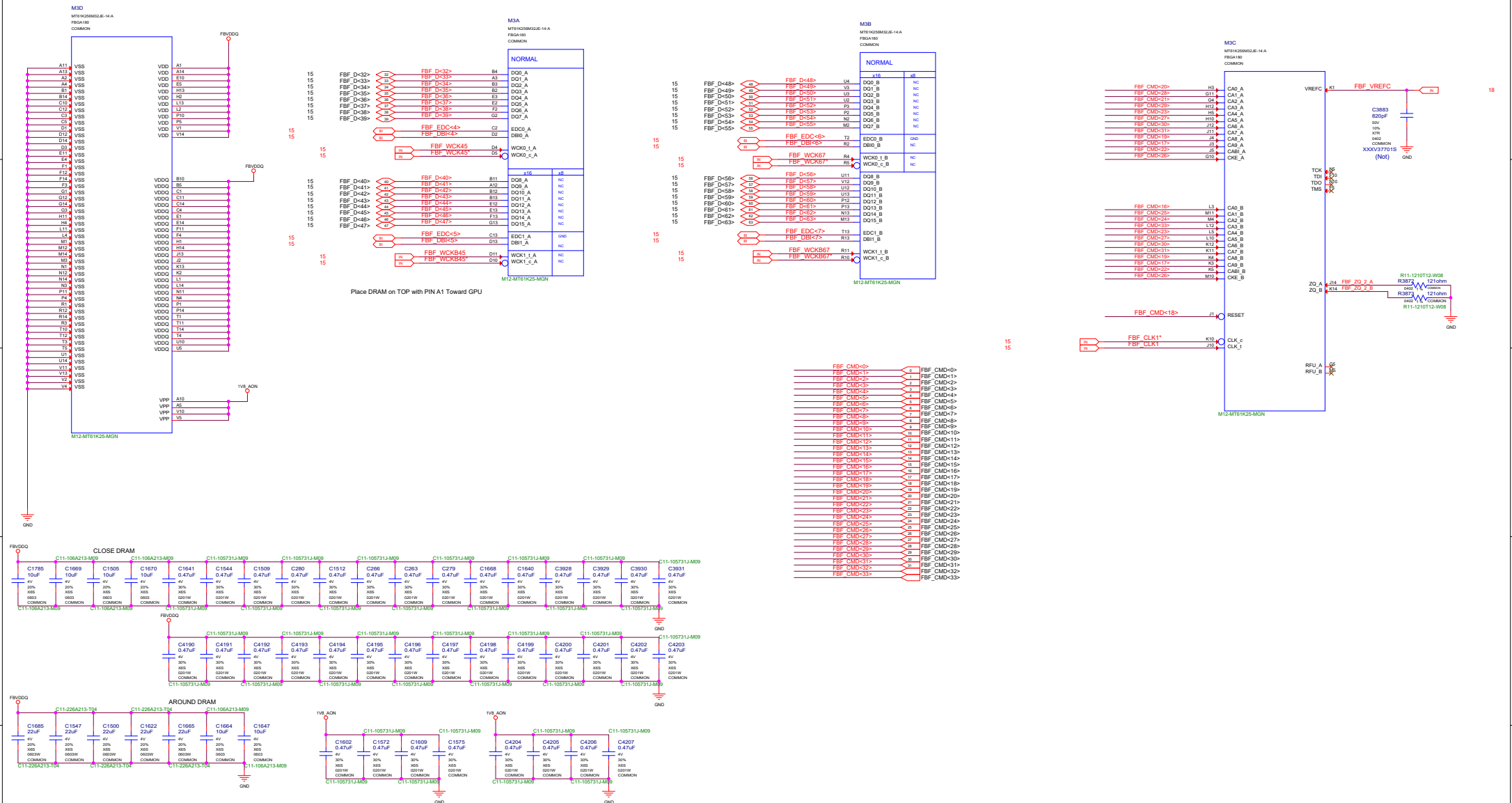
MEMORY: FBE Partition 63..32



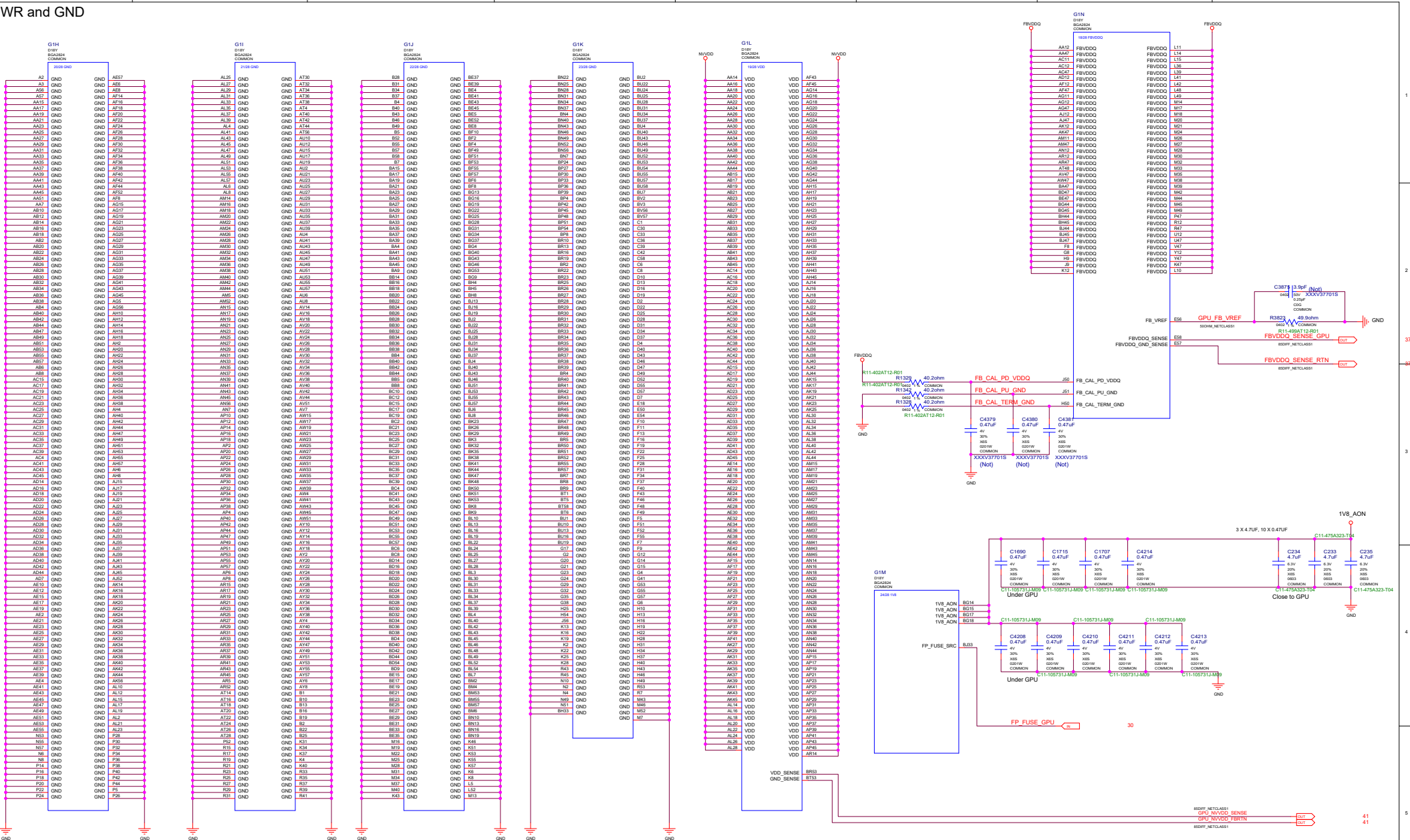
MEMORY: FBF Partition 31..0



MEMORY: FBF Partition 63..32

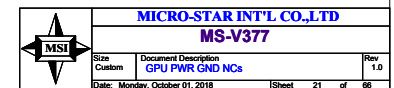
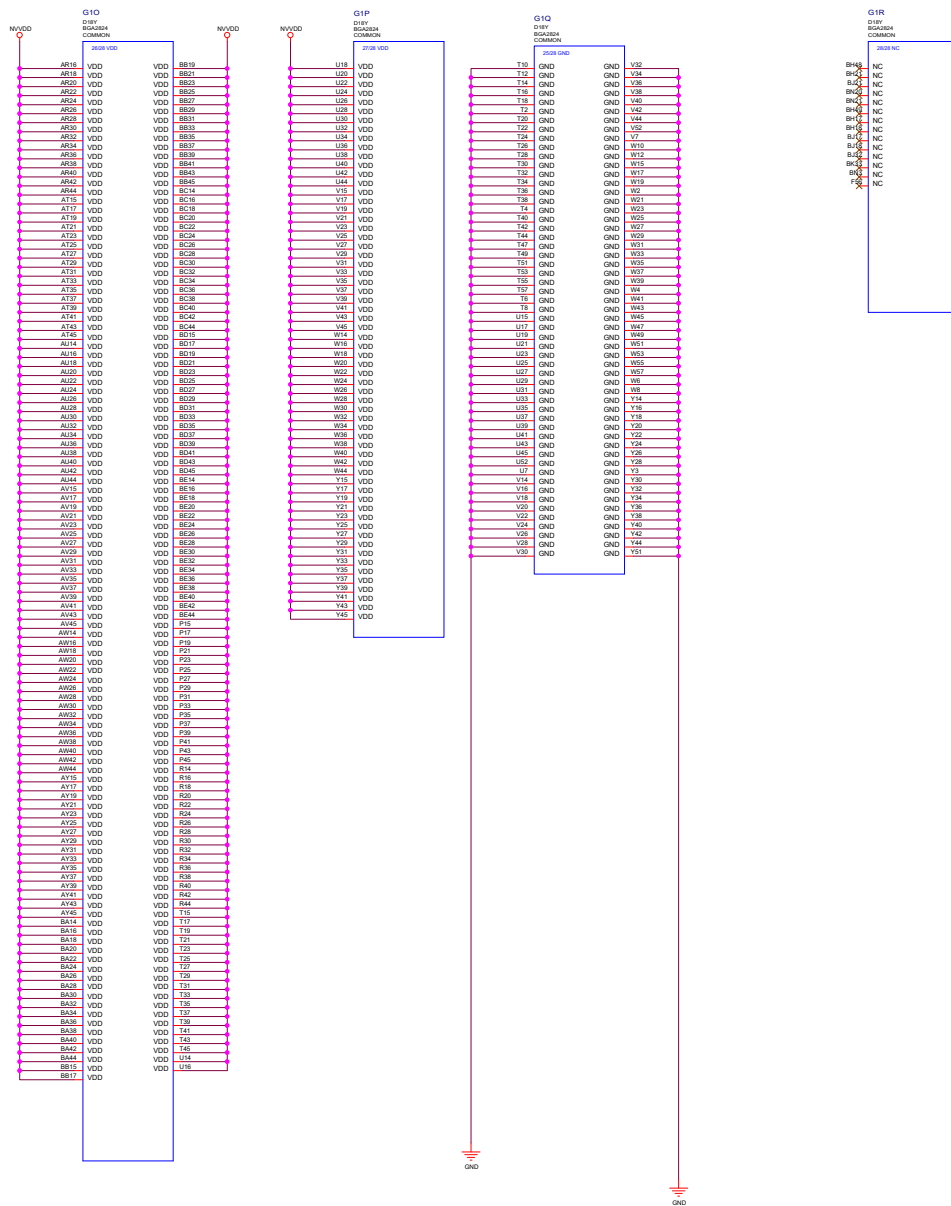


GPU PWR and GND

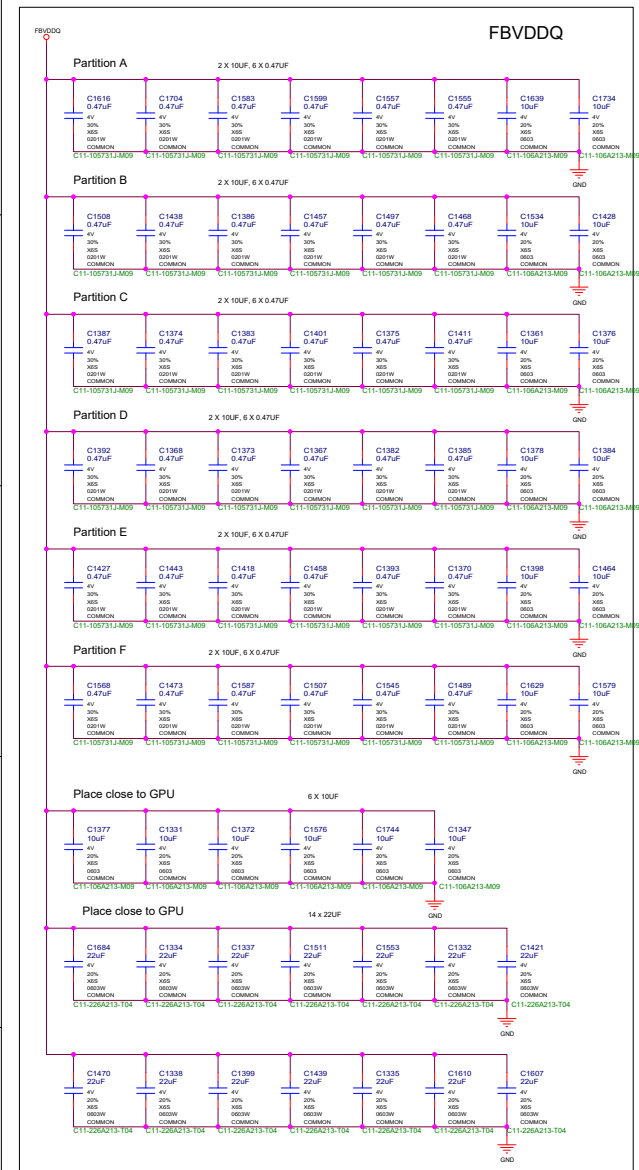


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GPU PWR and GND	1.0	

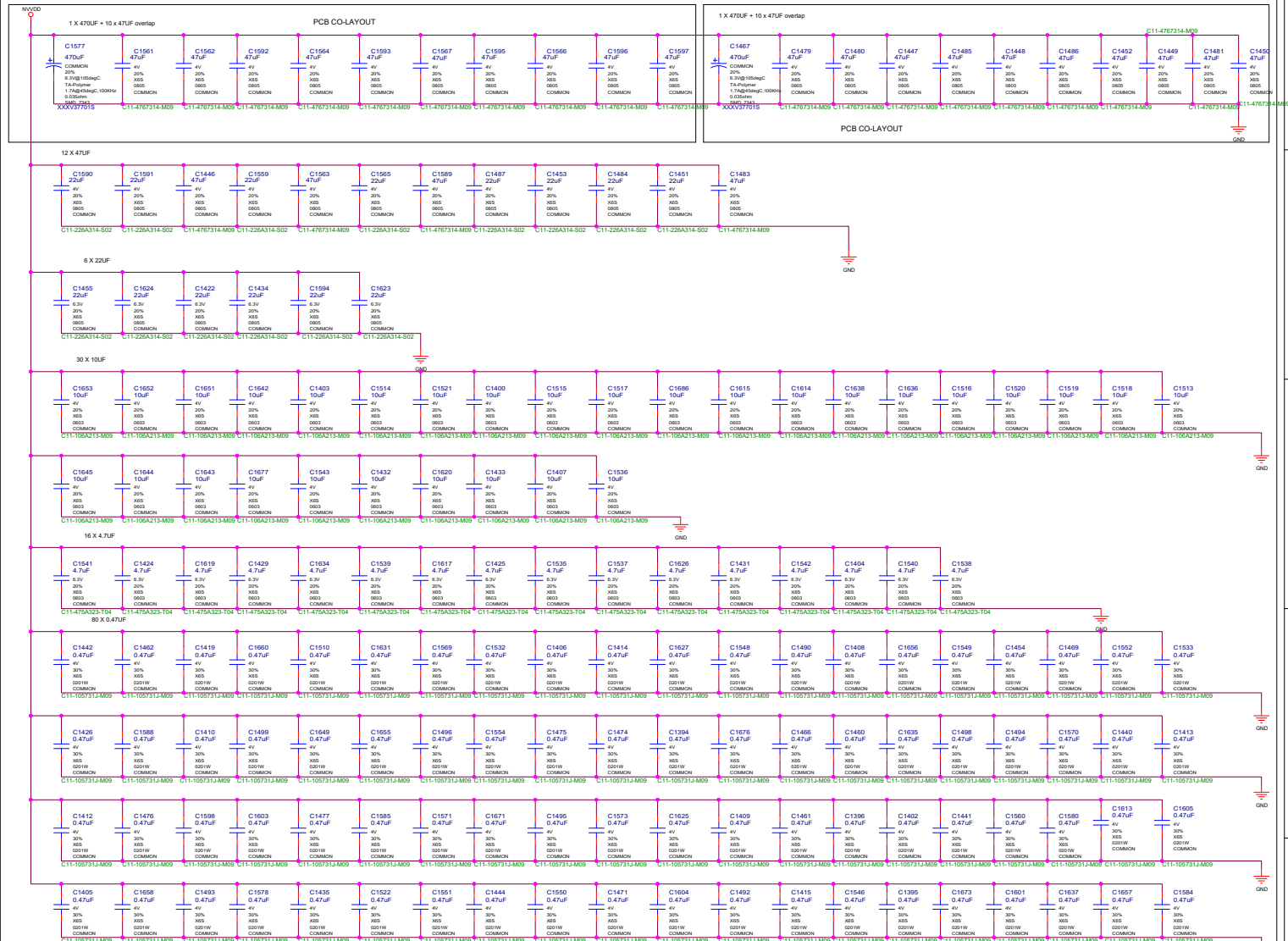
GPU PWR GND NCs



GPU Decoupling



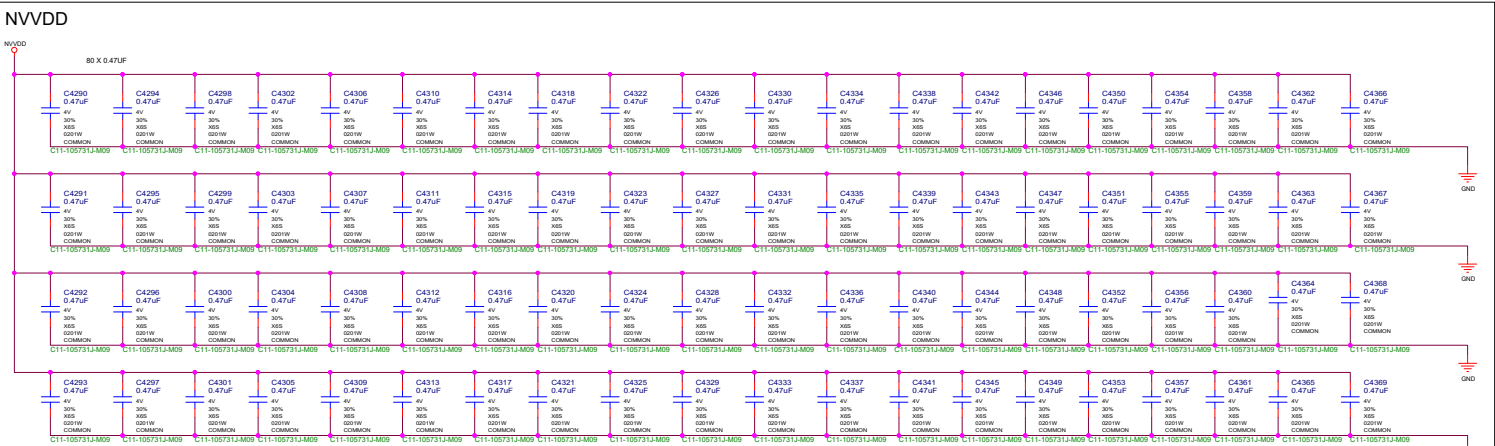
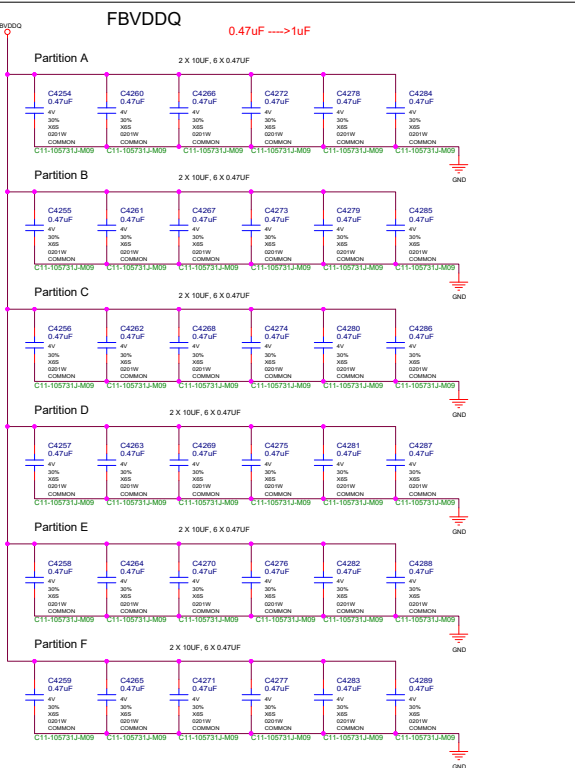
NVVDD



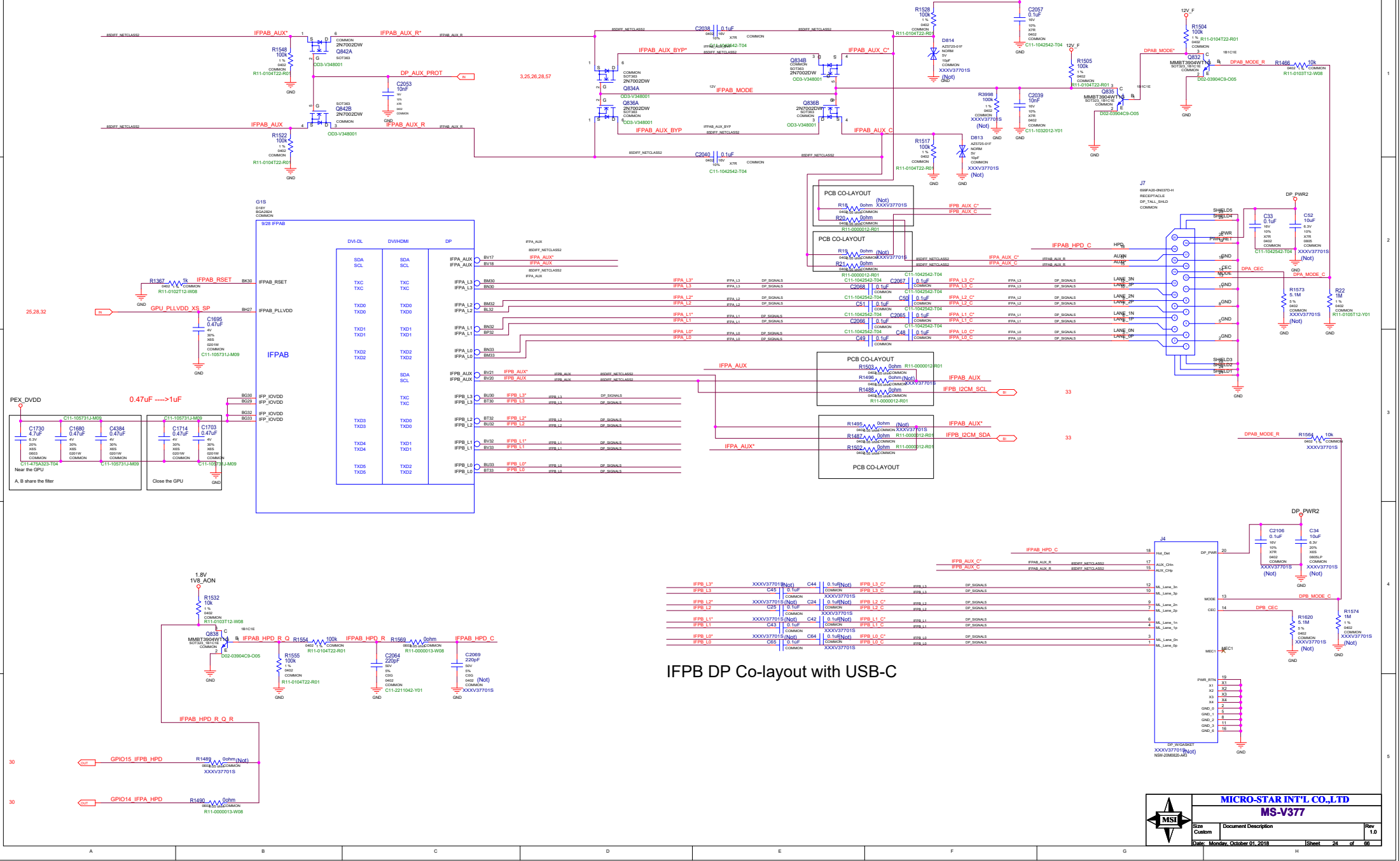
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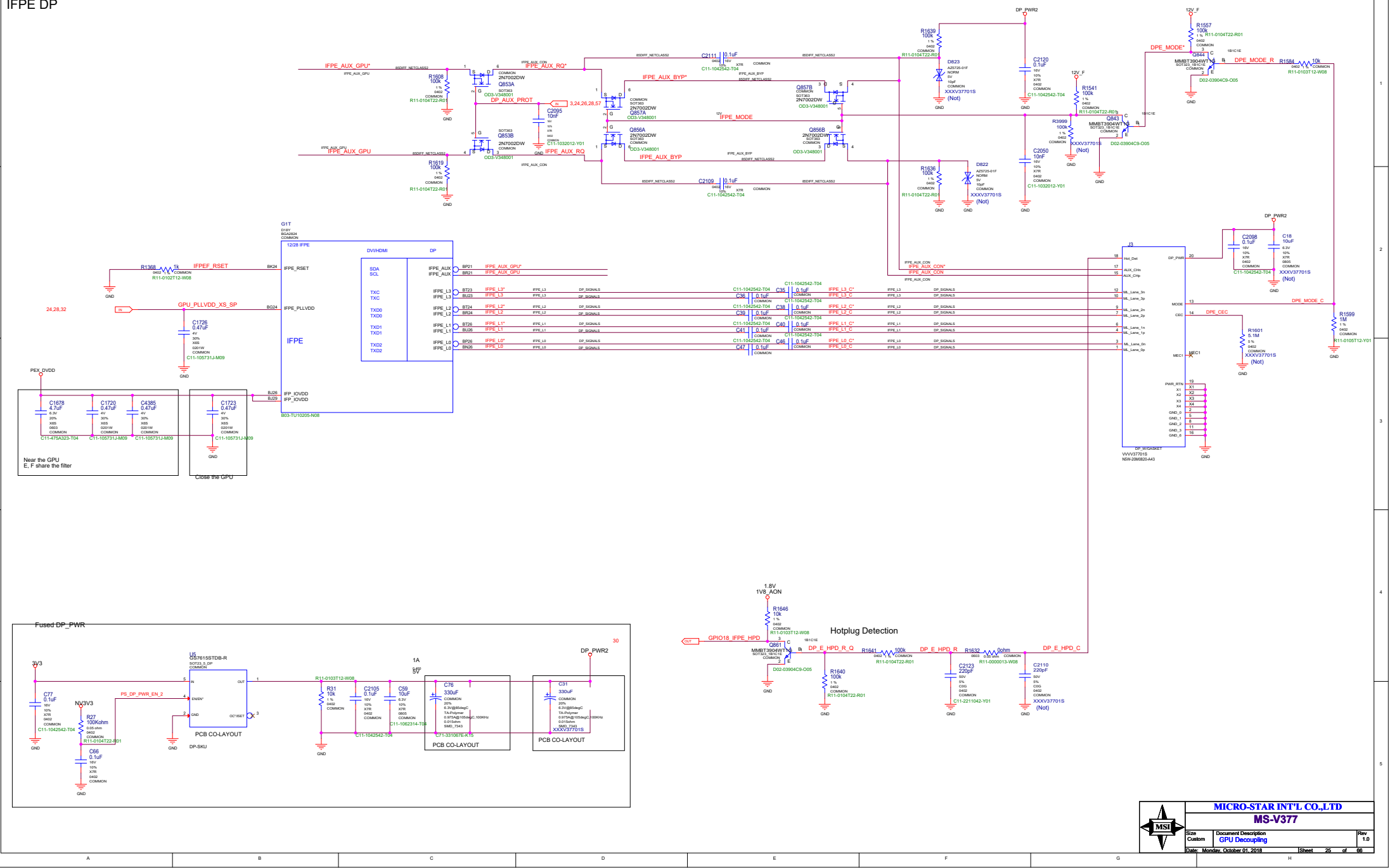
Size: Custom Document Description: GPU Decoupling Sheet: 22 of 66
Date: Monday, October 01, 2018 Rev: 1.0

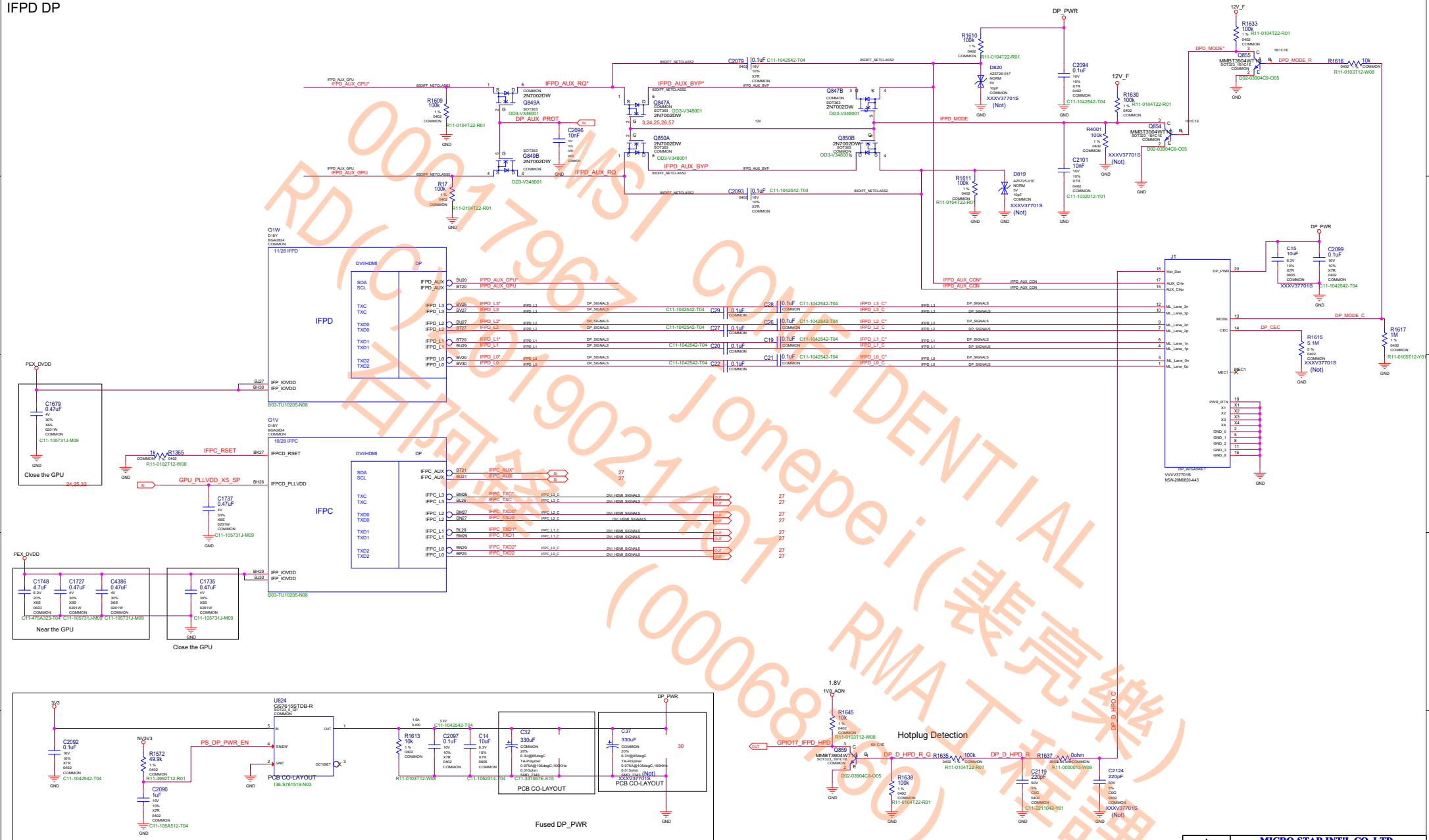
GPU Decoupling



IFPAB TALL-DP







NVHS Interface and FRAME LOCK



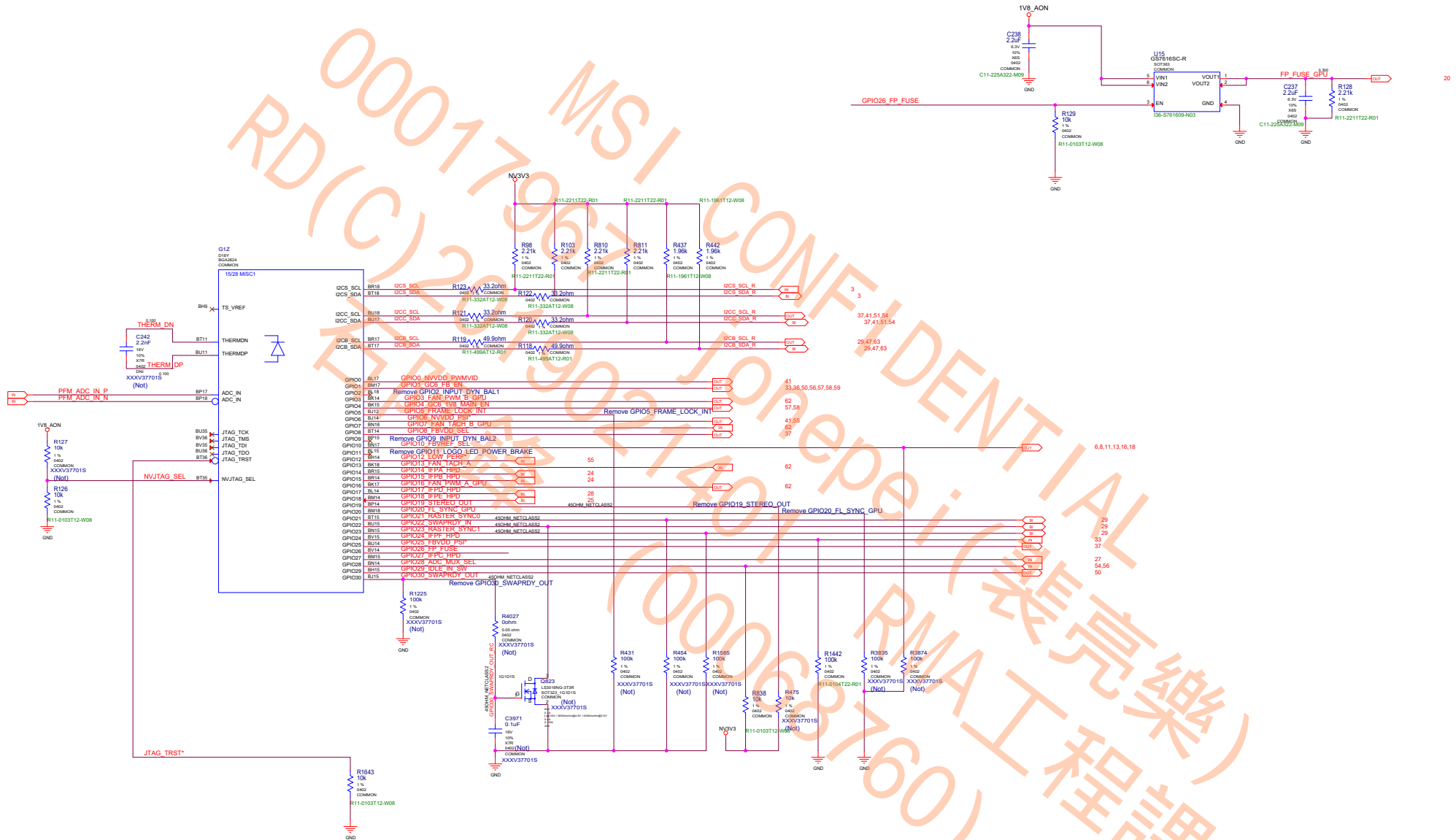
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Custom		1.0
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MISC1: Fan, Thermal, JTAG, GPIO, STEREO



MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
H	L	H	00101
H	H	L	00110
H	H	H	00111
L	L	M	01000
L	M	L	01001

DEFAULT

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	H	XXX0	FS_OVERT DISABLE

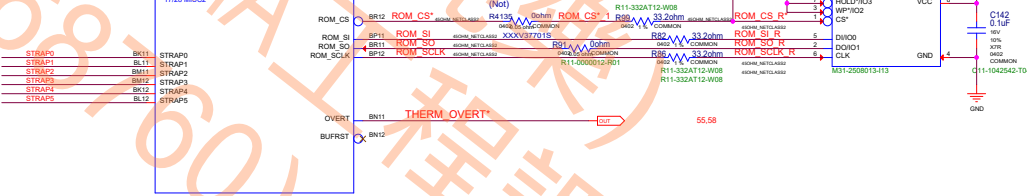
DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

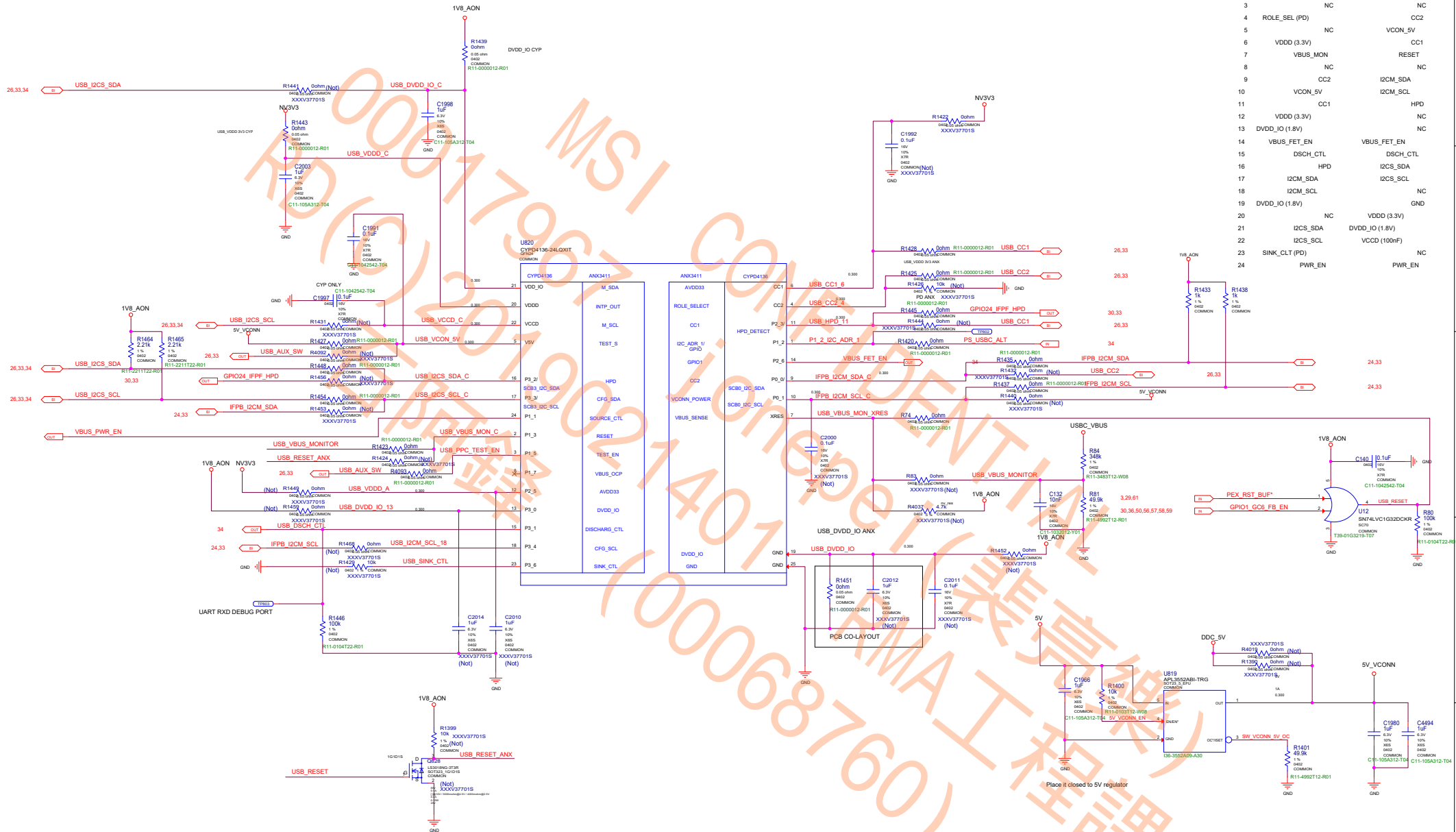
Default

SKU 200

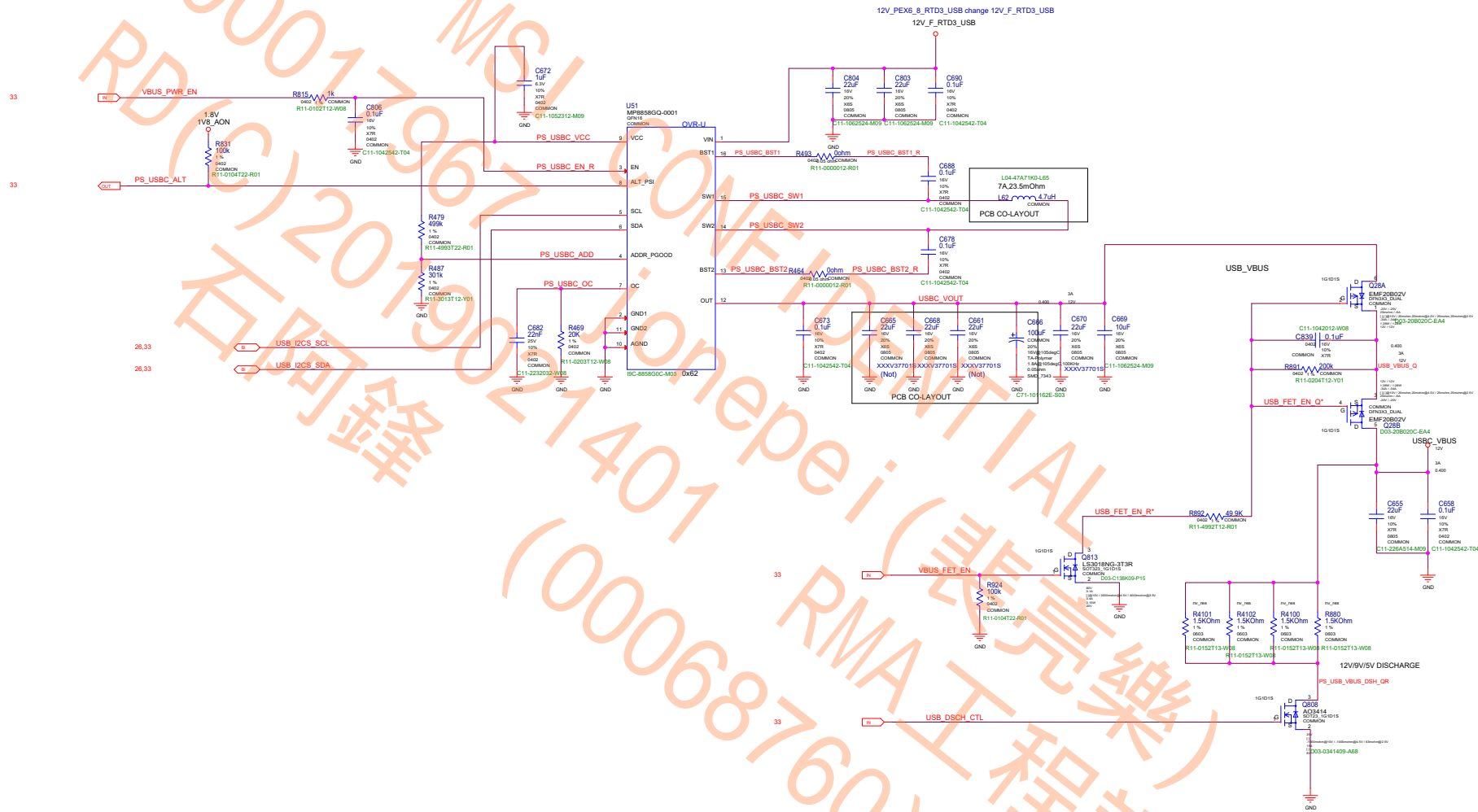
9/26 modify ROM_CS*_2



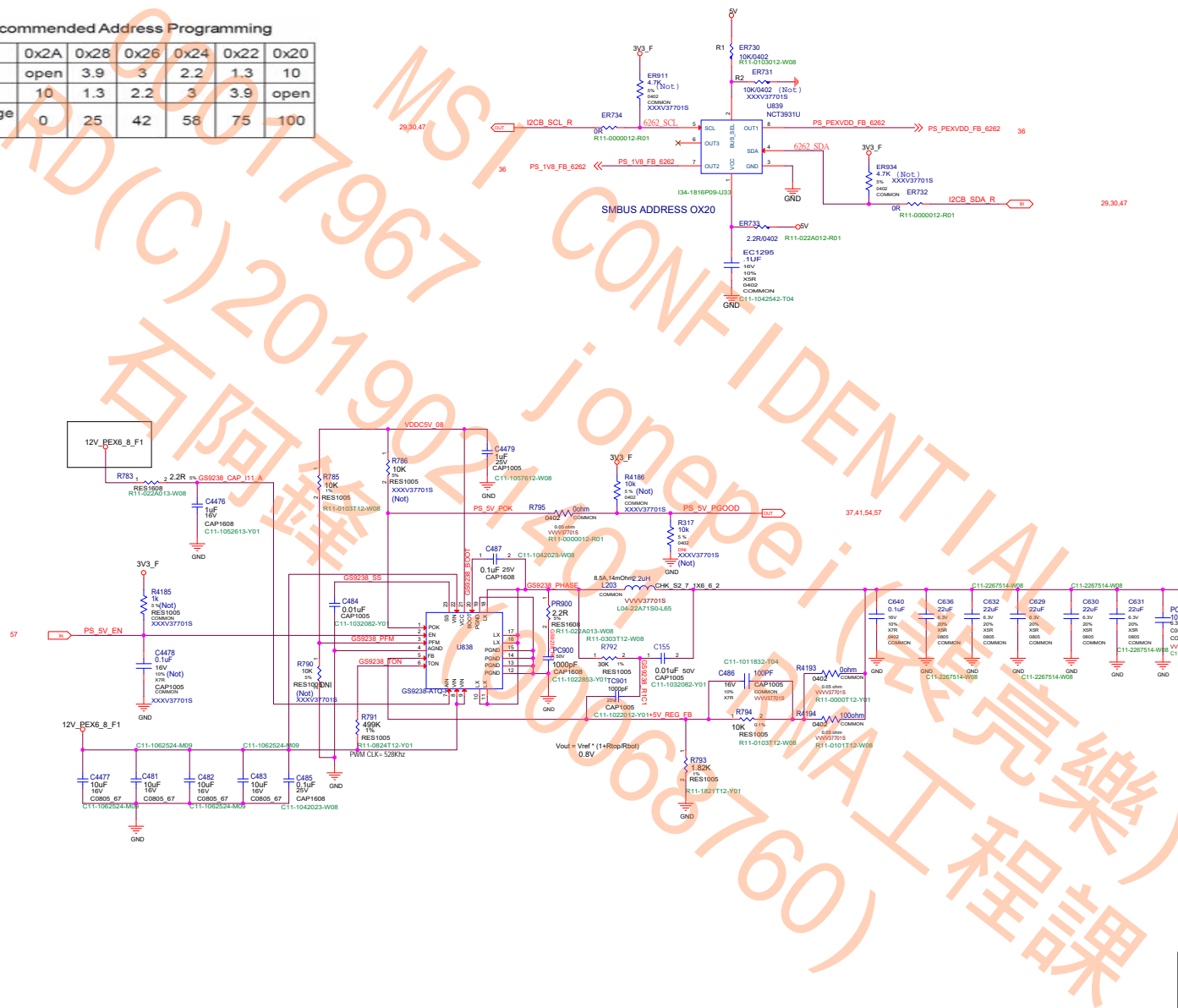
MISC: USB PPC



PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_SV
6	VDDO (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_SV	I2CM_SCL
11	CC1	HPD
12	VDDO (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDO (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCO (100mF)
23	SINK_CTL (PD)	NC
24	PWR_EN	PWR_EN

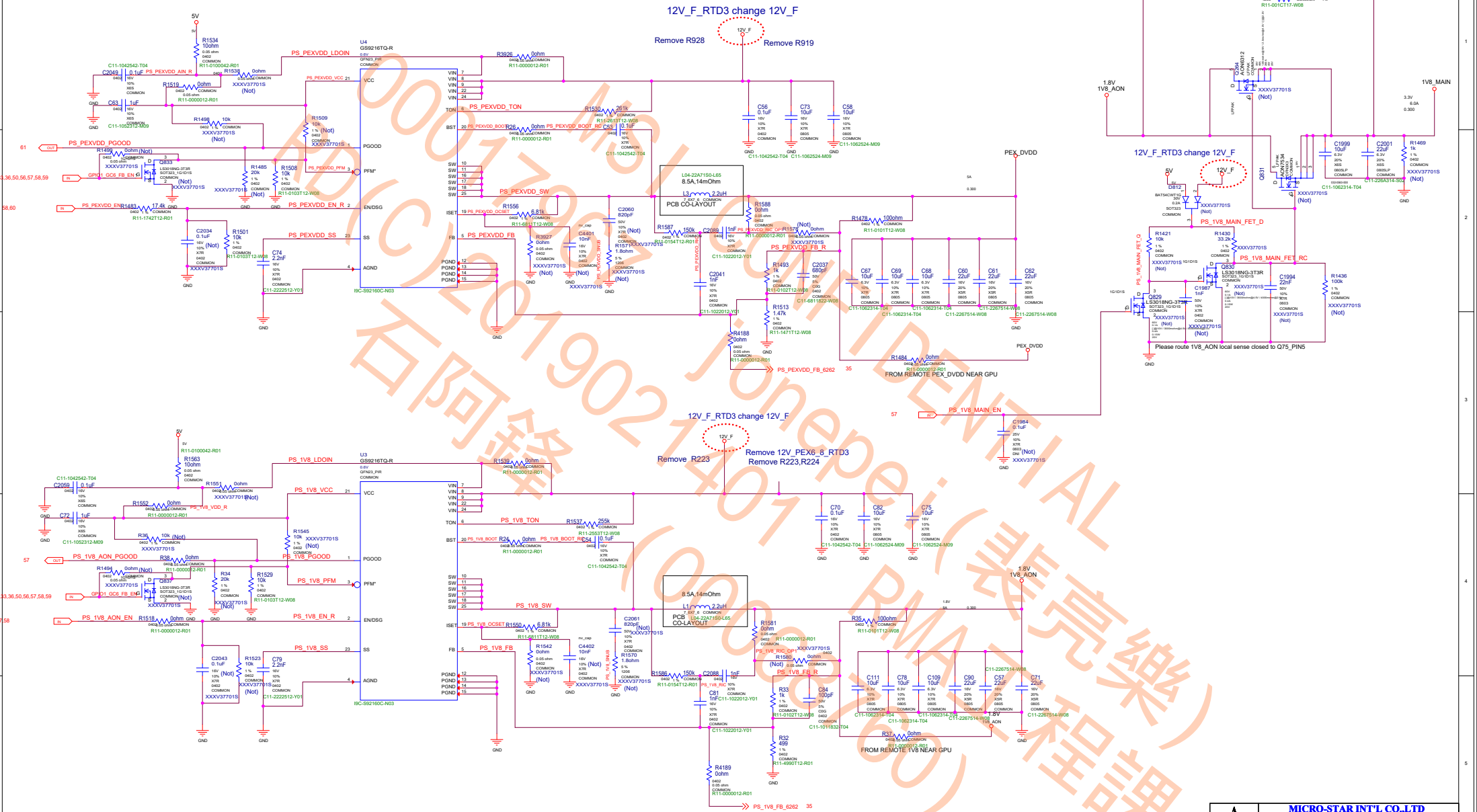


Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (k Ω)	open	3.9	3	2.2	1.3	10
R2 (k Ω)	10	1.3	2.2	3	3.9	open
BUS_SEL Voltage (% of VCC)	0	25	42	58	75	100



description

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PS: FBVDD Controller

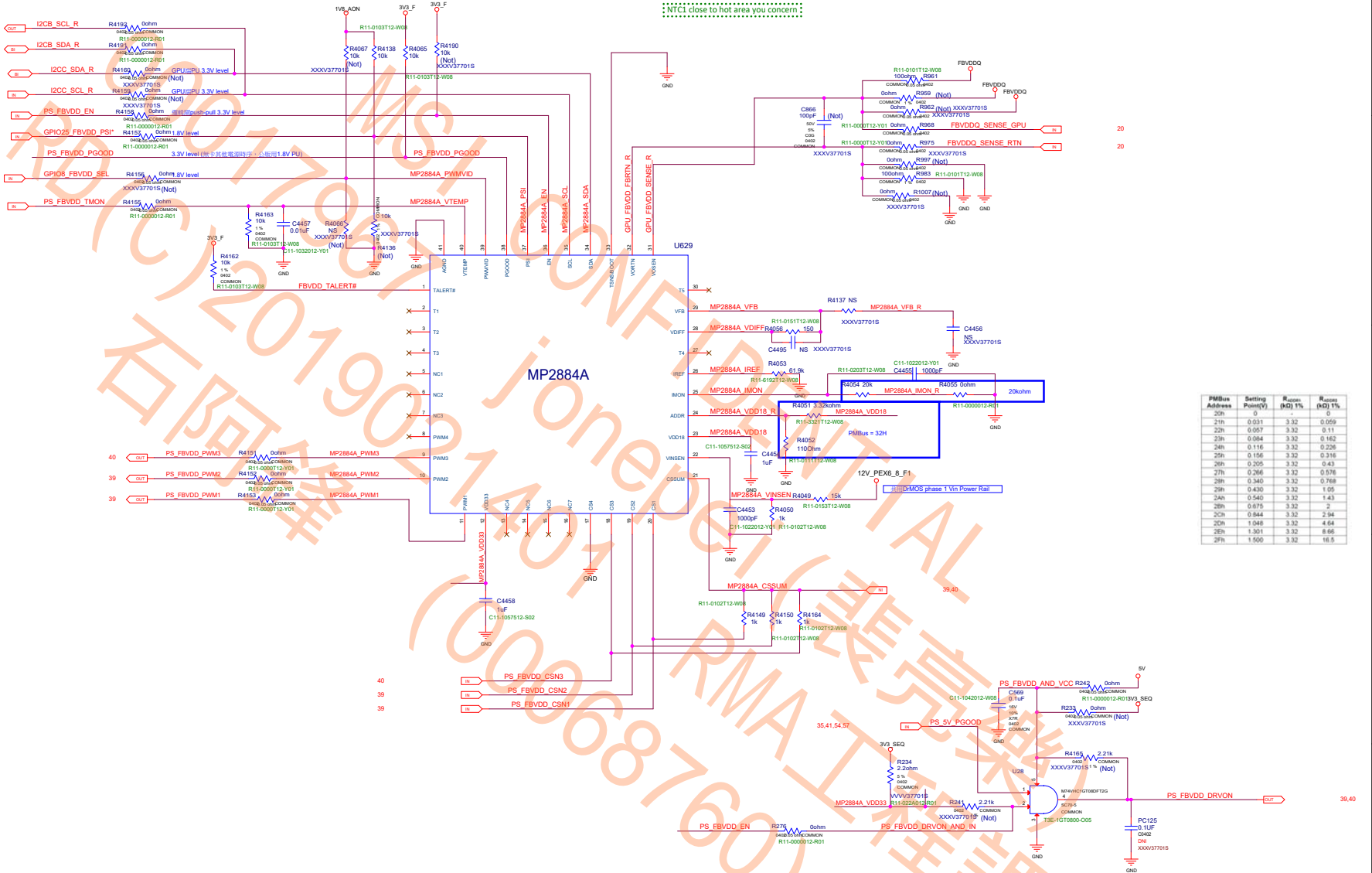
EN Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

PWMVID	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1Fr

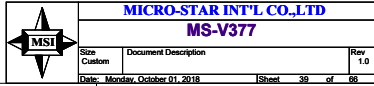
	+NVVDD
TDC	??A
IccMax	??A
Vboot	1.35V
Load Line	0mohm

29.30,47
29.30,47
30.41,51,54
30.41,51,54
58,60
30
30
39,40,66



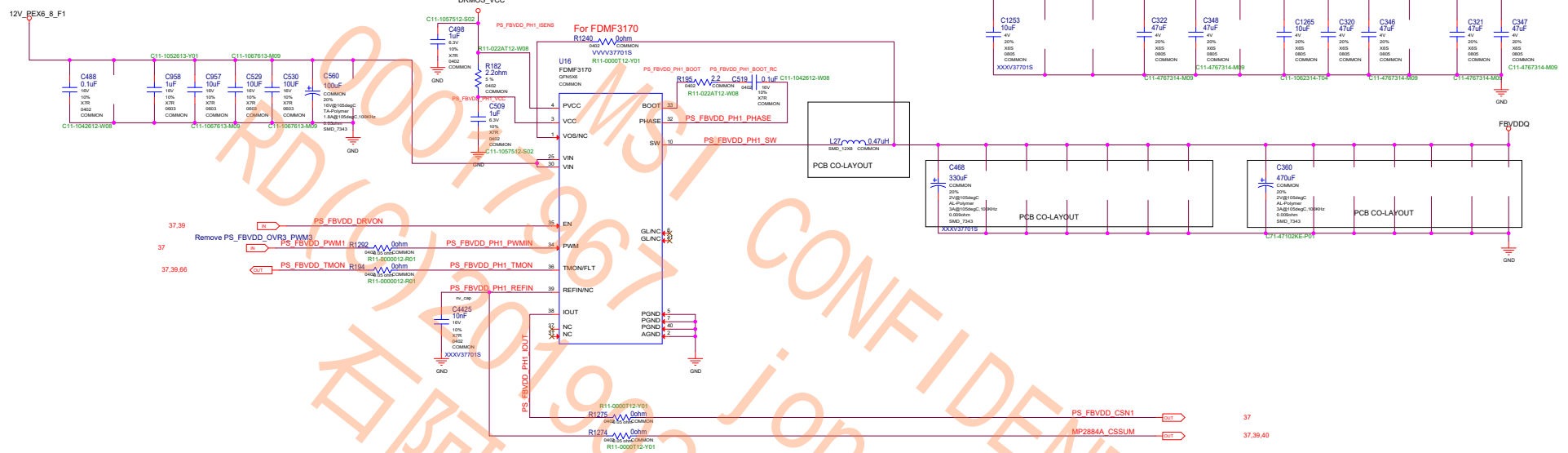
MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2019021401 RMA工程課
石阿鋒 (00068760)

12V_F_RTD3 change 12V_PEX6_8_F1



PS: FBVDD PH1

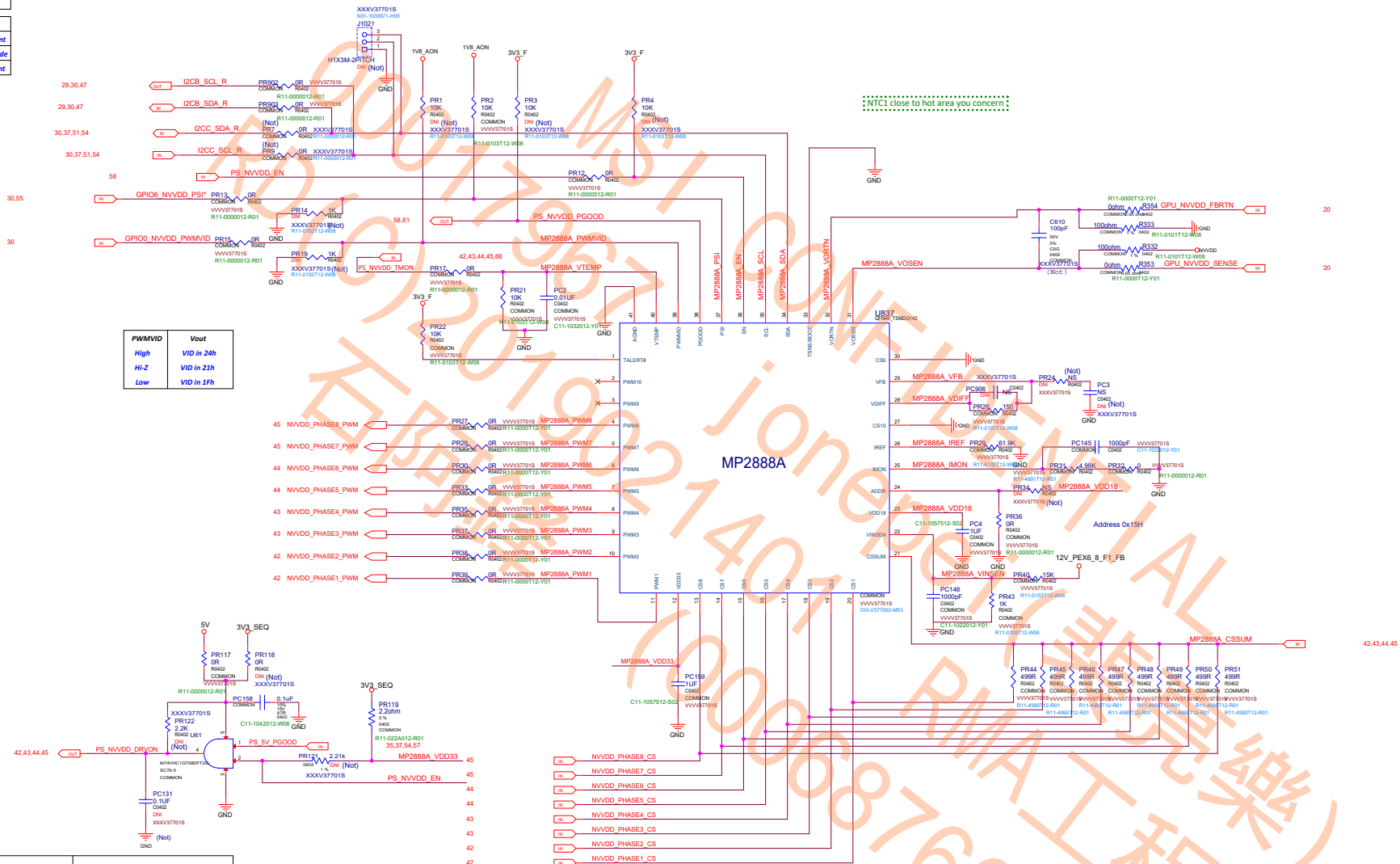
FBVDD_PH2_3_VIN change 12V_PEX6_8_F1



Remove 12V_PEX_FB ---->FBVDD_PH2_3_VIN circuit

EN Type	R3
<i>Open Drain</i>	<i>10k</i>
<i>Push Pull</i>	<i>NS</i>

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count



	+NVVDD
TDC	200A
IccMax	330A
Vboot	0.8V
Load Line	0mohm

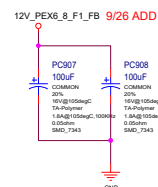
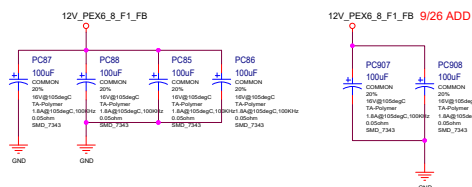
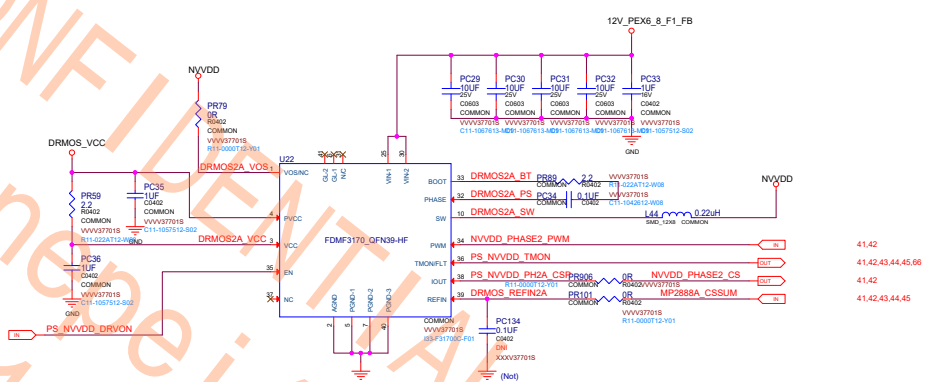
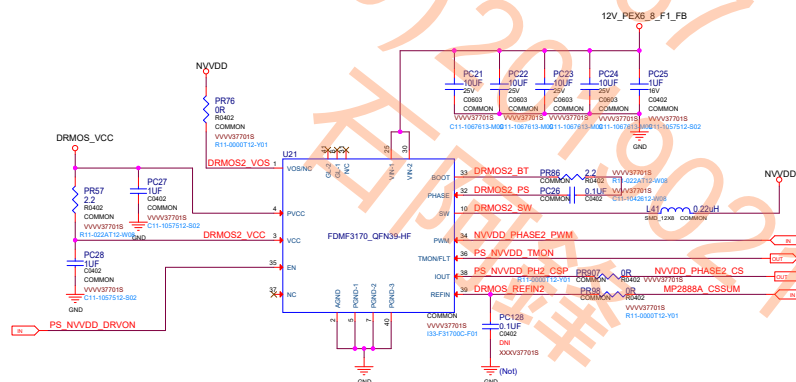
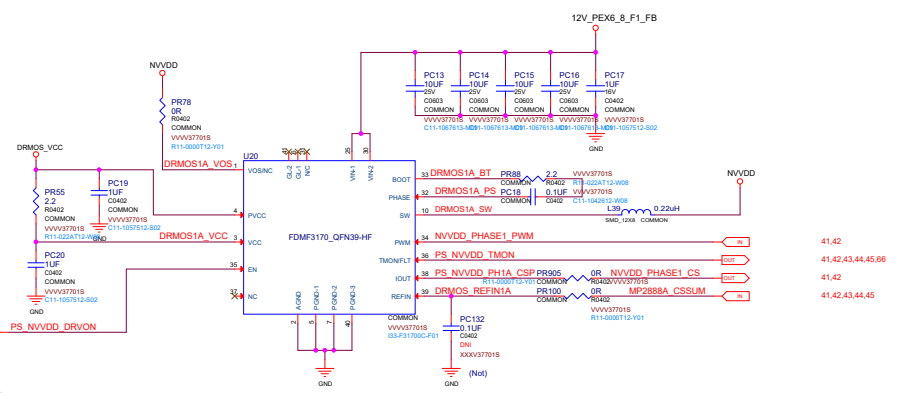
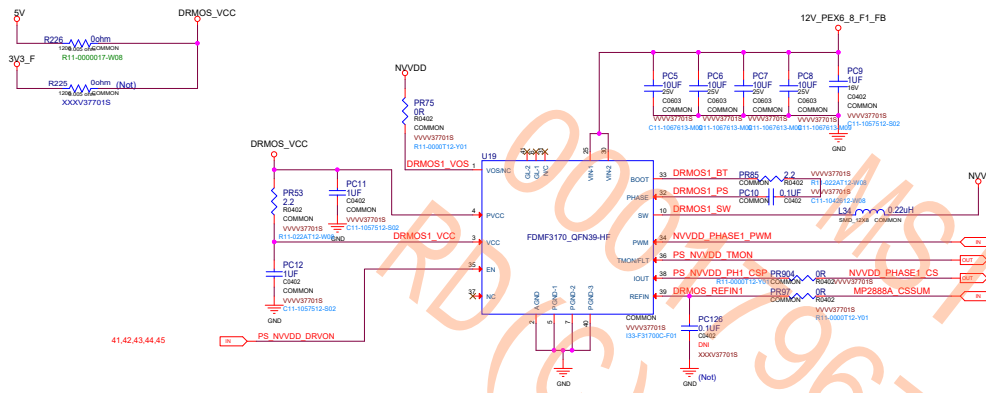
PMBus Address	Setting Point(V)	R _{DS(on)} (mΩ)	R _{DS(on)} (mΩ) 1%
20h	0	3.32	0.059
21h	0.031	3.32	0.11
22h	0.057	3.32	0.162
23h	0.084	3.32	0.216
24h	0.116	3.32	0.270
25h	0.156	3.32	0.323
26h	0.205	3.32	0.433
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.94
2Dh	1.048	3.32	4.4
2Eh	1.301	3.32	8.66
2Fh	1.605	3.32	13.5

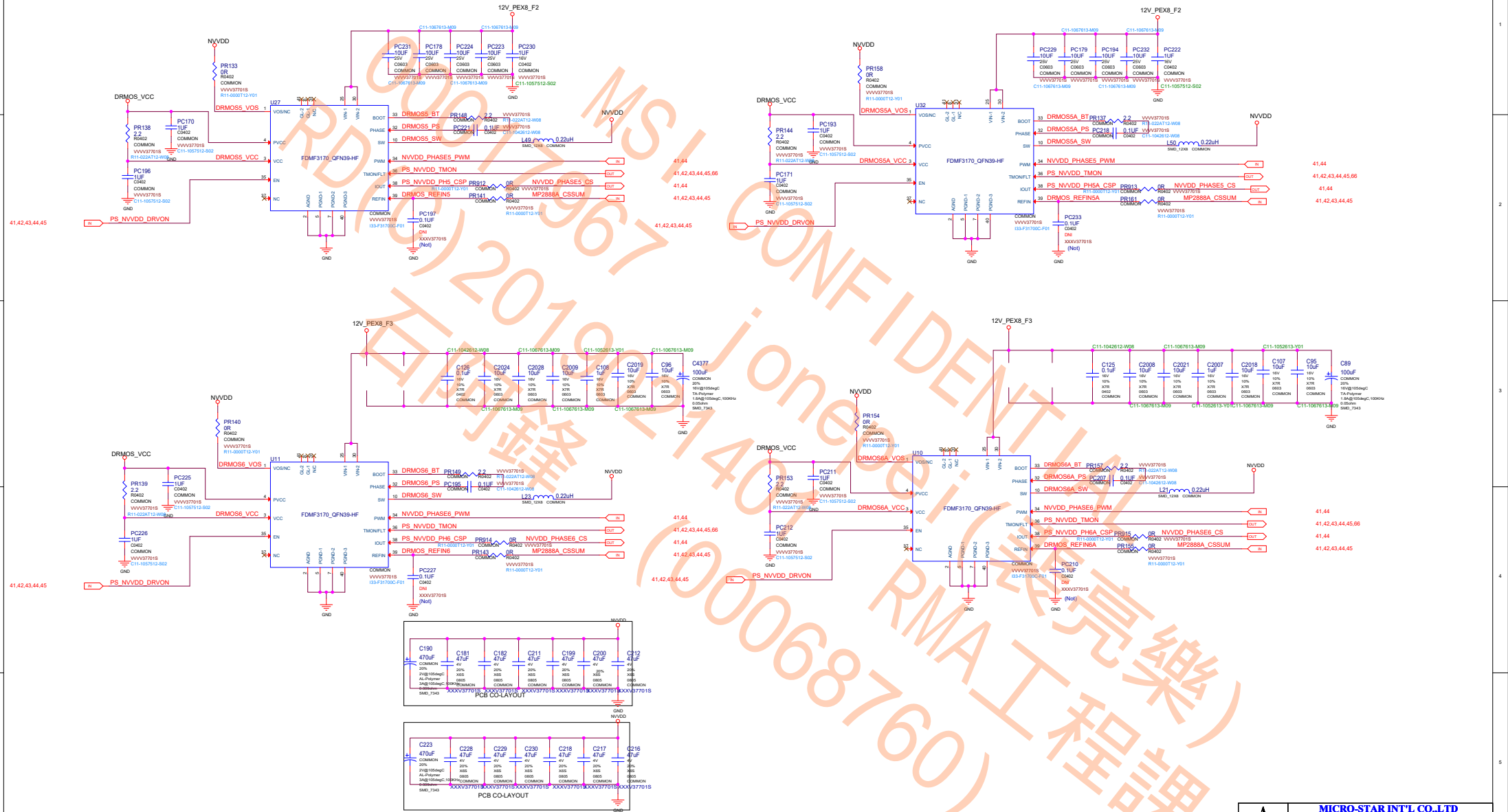


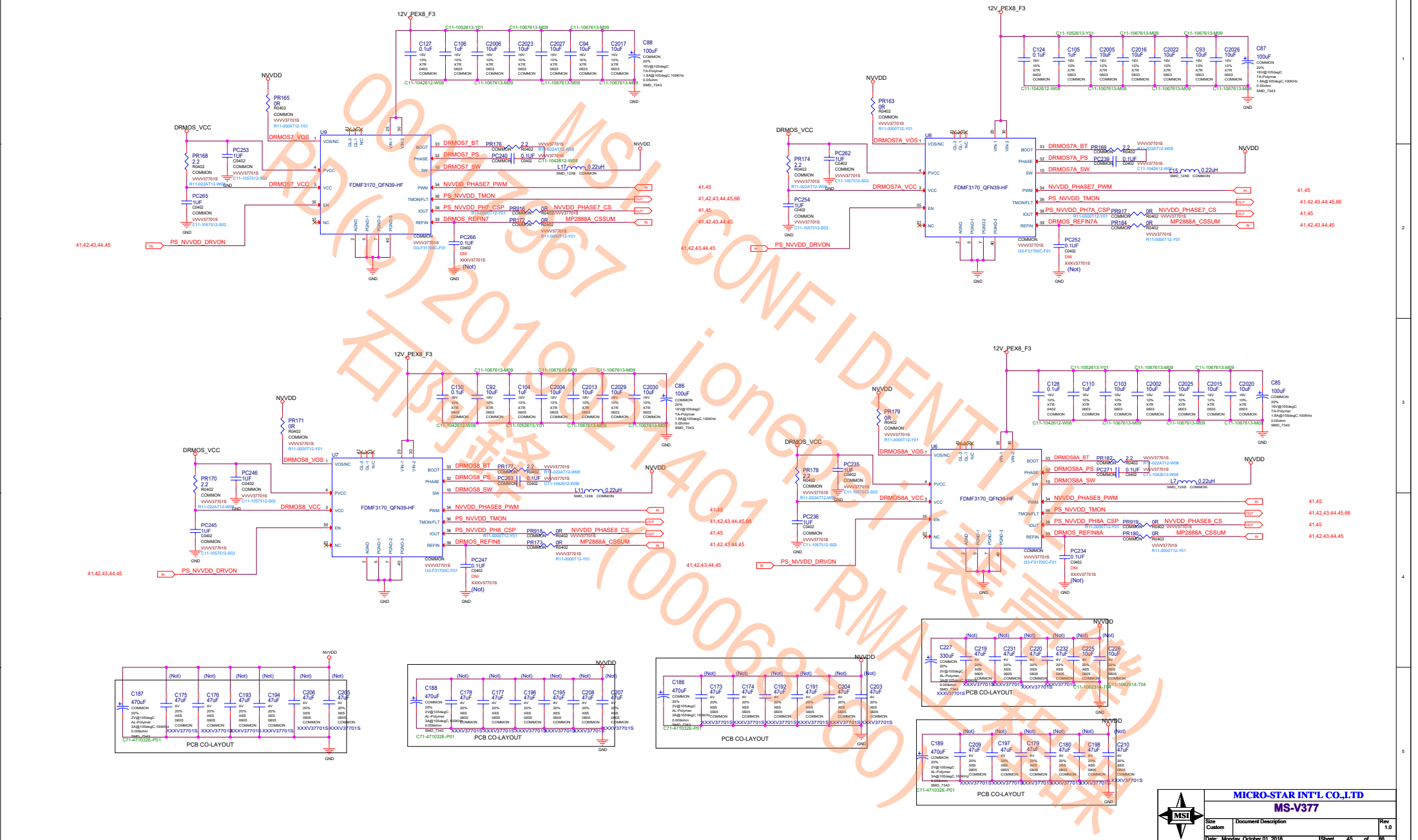
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PS: NVVDD Phase 1~4





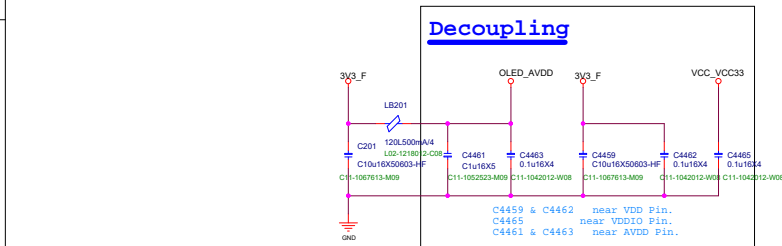
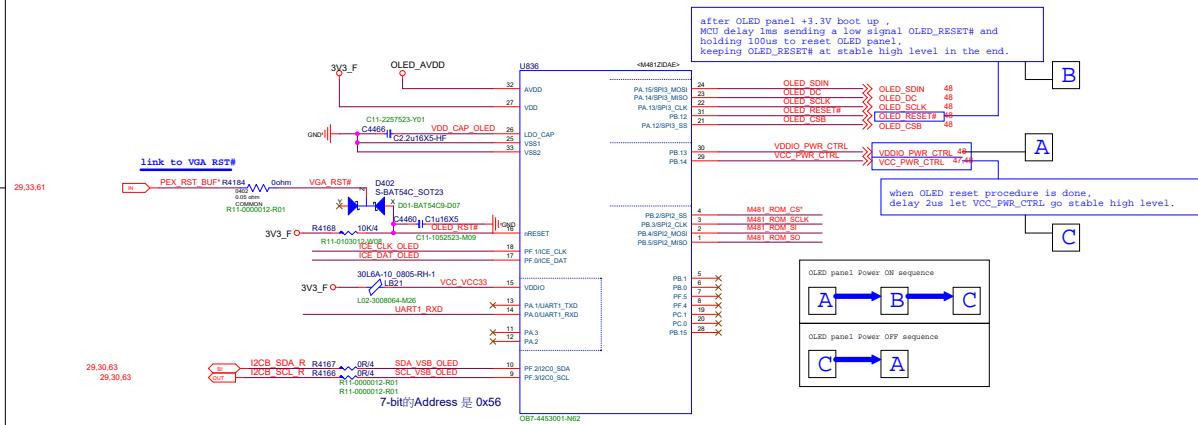




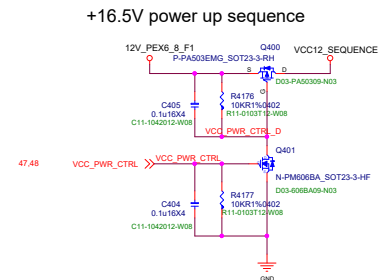
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PS: NVVDD PH 9,10
32 PIN OLED MCU

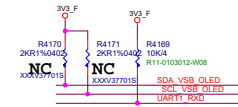
MPS1542 BUCK BOOST FOR OLED POWER 12Vin 16.5Vout



PIN FUNCTIONS

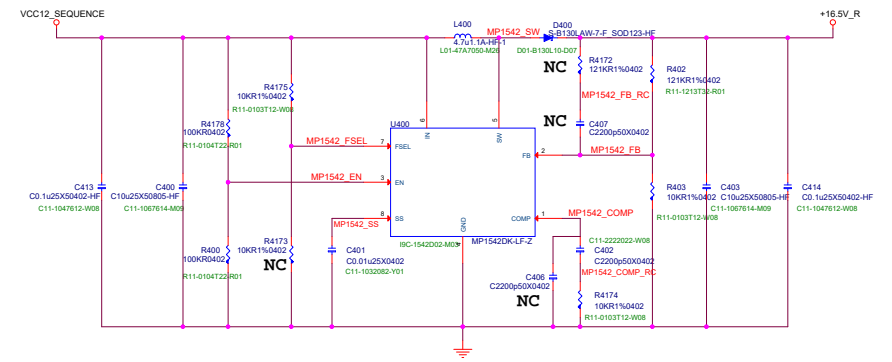
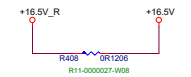
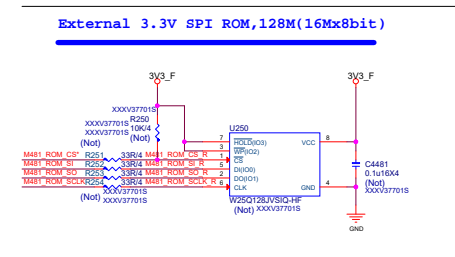
Pin #	Name	Description
1	COMP	Compensation Pin. Connect a capacitor and resistor in series to ground for loop stability.
2	FB	Feedback Input. Reference voltage is 1.25V. Connect a resistor divider to this pin.
3	EN	Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input source (through a 100kΩ pull-up resistor if V_{IN} is 6V) for automatic startup. EN cannot be left floating.

I2C and UART Reserve



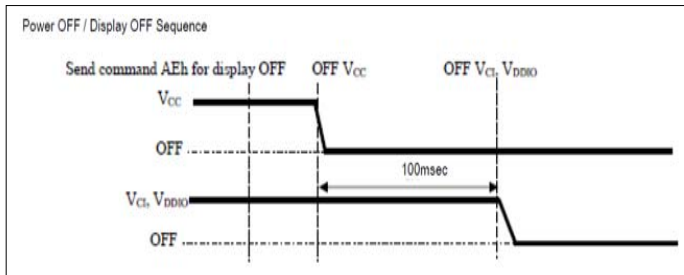
```
pull high I2C don't leave it floating,
once R23 + R24 removed
pull high UART Rx don't leave it floating
```

FW update



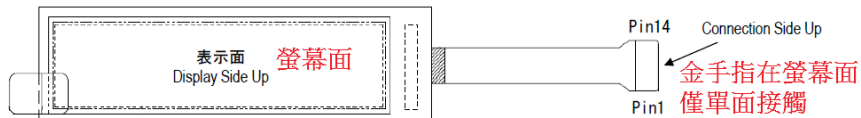
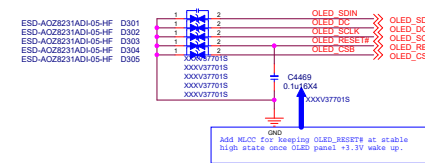
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I:Input, O:Output, P:Power

PIN No	名称 Pin Name	機能 Function Description	I/O
1	VCC	OLED駆動電源 OLED Driving Voltage	P
2	AGND	グラウンド Analog Ground	P
3	FR	同期信号 Synchronization Signal	O
4	CSB	チップセレクト Chip Select	I
5	RSTB	リセット Reset	I
6	DC	データ/コマンド選択 Data/Command Selection	I
7	SCLK	シリアルクロック Serial Clock	I
8	SDIN	データ Data Input	I
9	GND	グラウンド Ground Pin	P
10	AGND	グラウンド Analog Ground	P
11	VCI	ロジック電源 Logic Power Voltage	P
12	VDD	コア電源 Core Voltage	P
13	VCOMH	COMH 電源 COMH Voltage	P
14	VCC	OLED駆動電源 OLED Driving Voltage	P

[illegible][illegible]

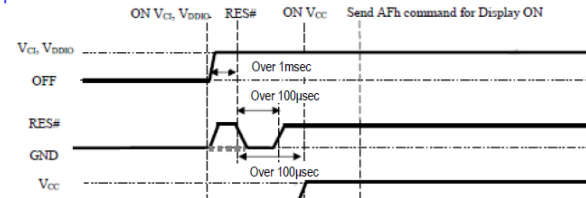
Add MLOC for keeping OLED_RESET# at stable high state once OLED panel +3.3V wake up.

MCU NUC481
OLED controller
VDDIO for UART

VDD/CI	3.3
--------	-----

1. after OLED panel +3.3V boot up ,
delay 1ms sending a low signal OLED_RESET# and
holding 100us to reset OLED panel,
keeping OLED_RESET# at stable high level in the end
2. when OLED reset procedure is done,
delay 2us let VCC_PWR_CTRL go stable high level.

Power ON / Display ON Sequence OLED panel



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A		B		C		D		E		F		G		H	
PS: NVVDD PH 13,14															
1															
2															
3															
4															
5															
A		B		C		D		E		F		G		H	



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PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

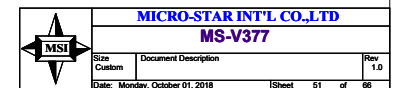
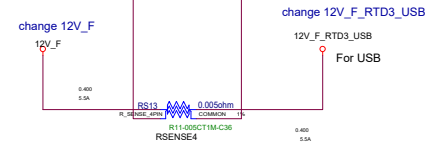
Remove 12V_F_RTD3 circuit

AND GATE LOGIC FOR P-BOARD

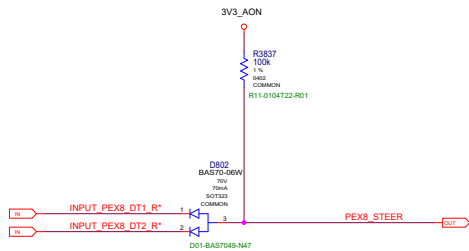
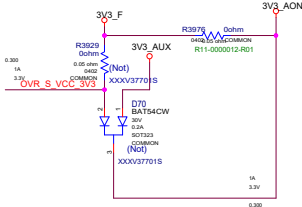
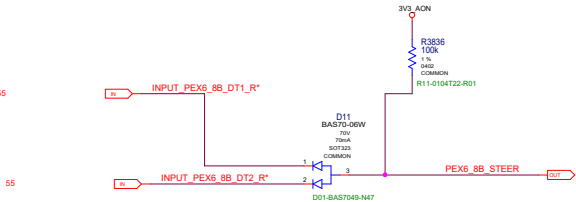
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

Remove 3V3_RTD3 circuit

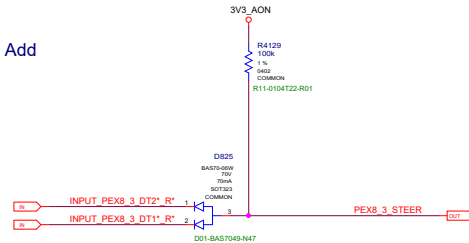




PS: Input Switch Rail Balance

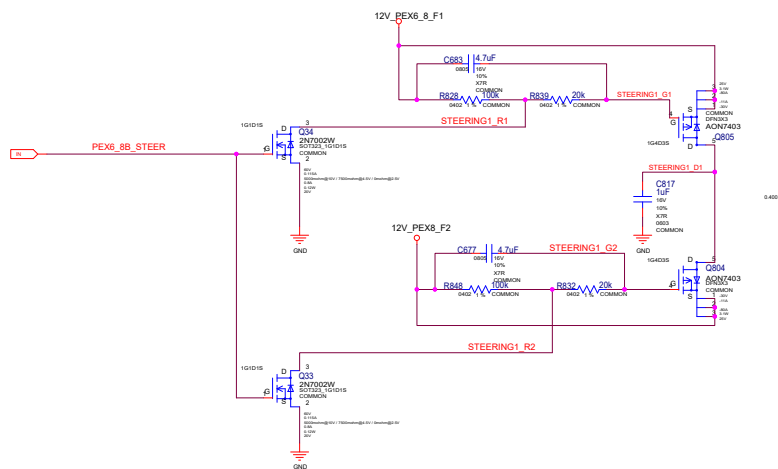


Add



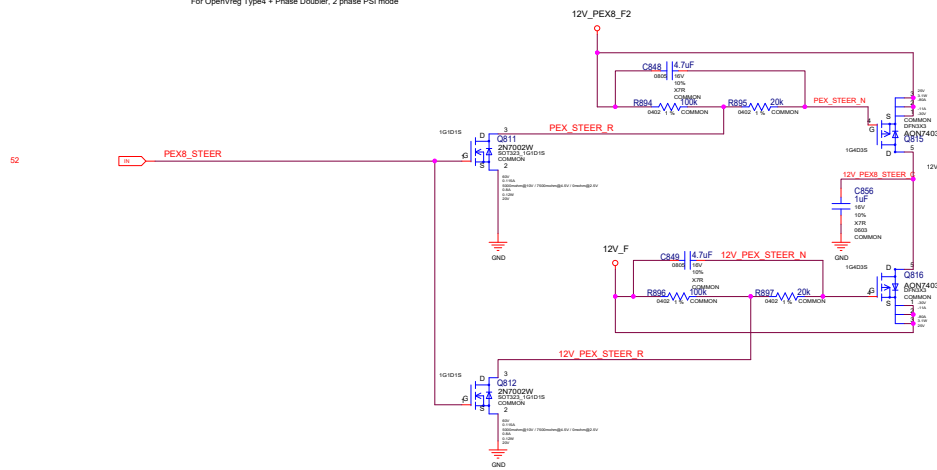
Remove NVVDD VIN change circuit

12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

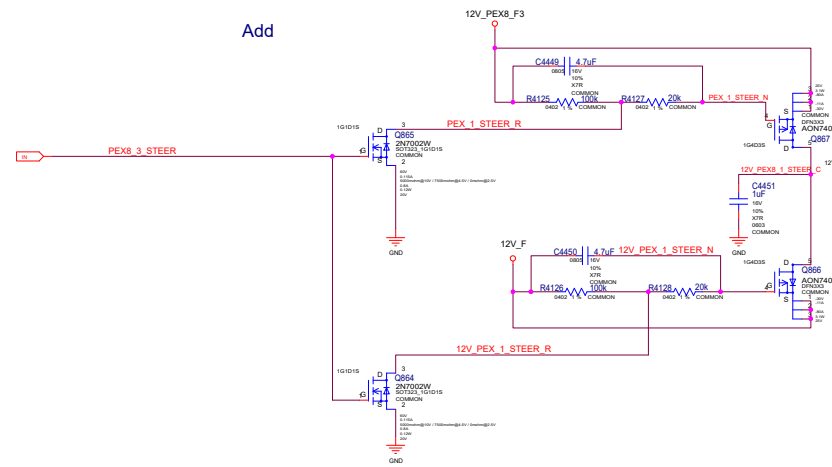


12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

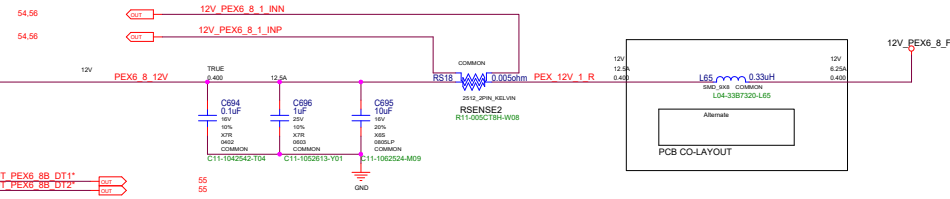
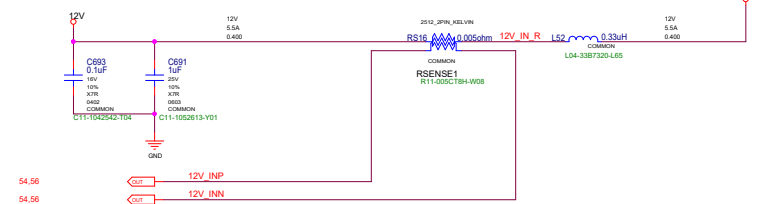
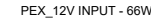
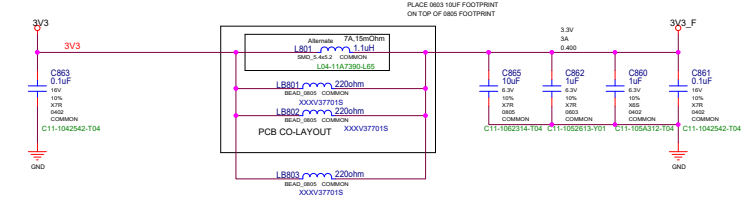
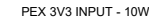
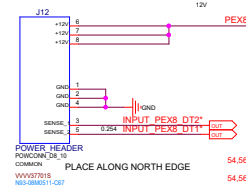
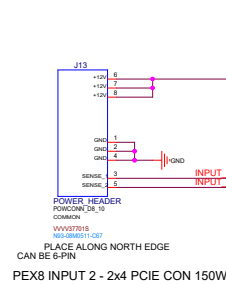
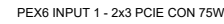
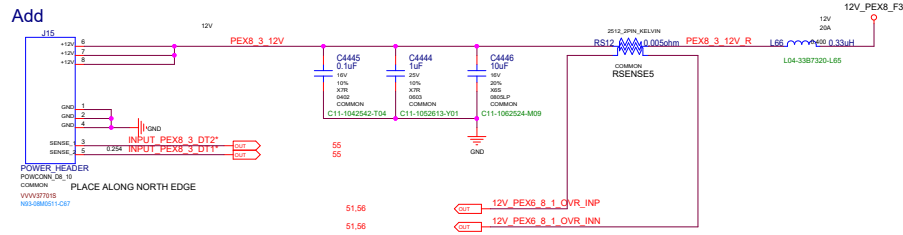
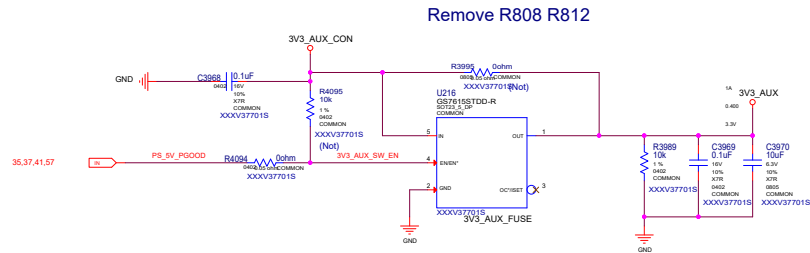
For OpenVing Type4 + Phase Doubler, 2 phase PSI mode



Add

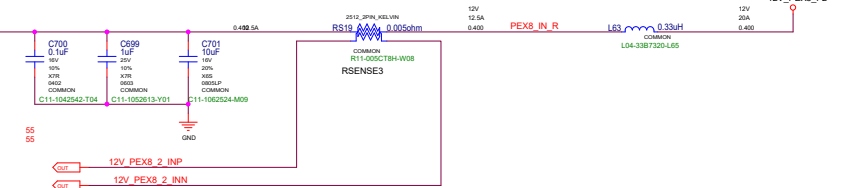


PS: Inputs, Filtering, and Monitoring

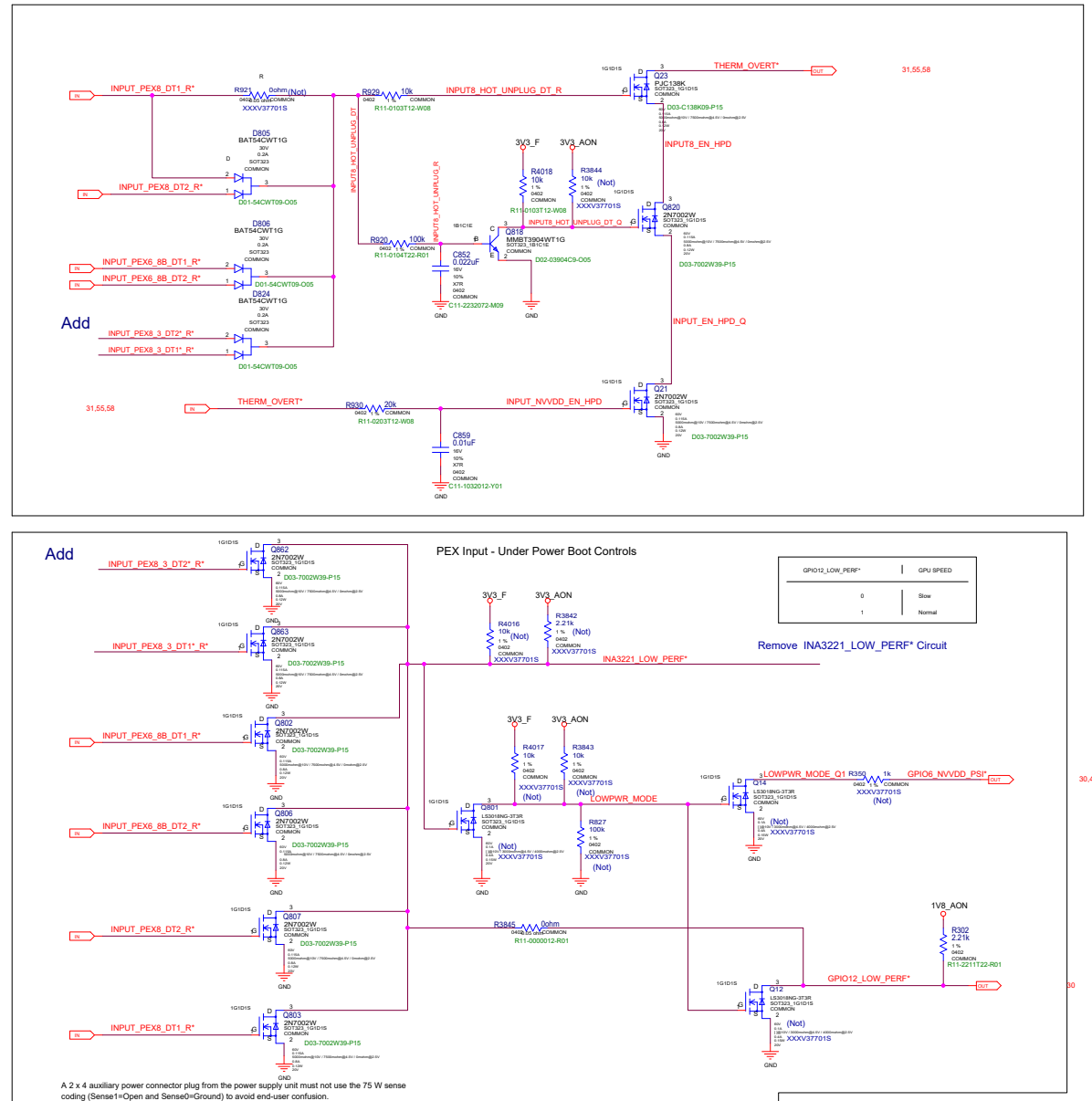
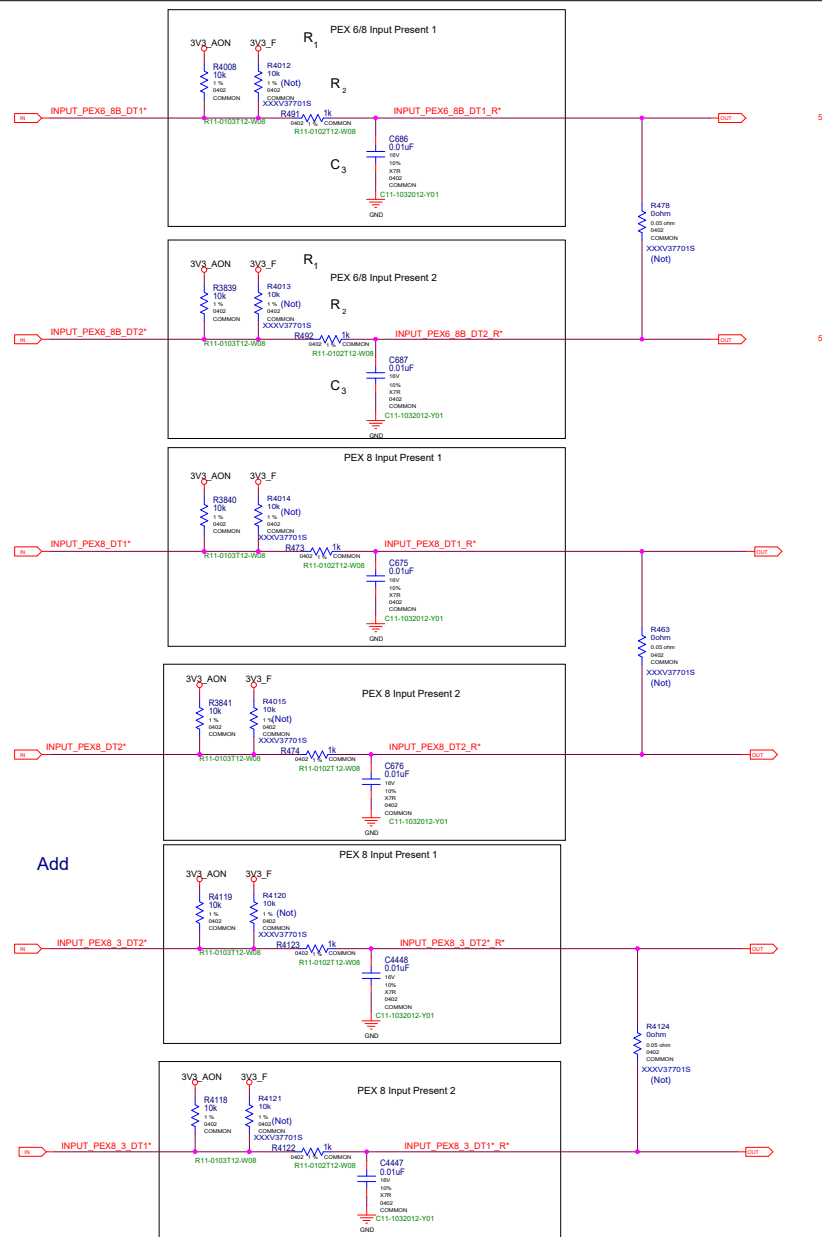


Remove RS14 RS15

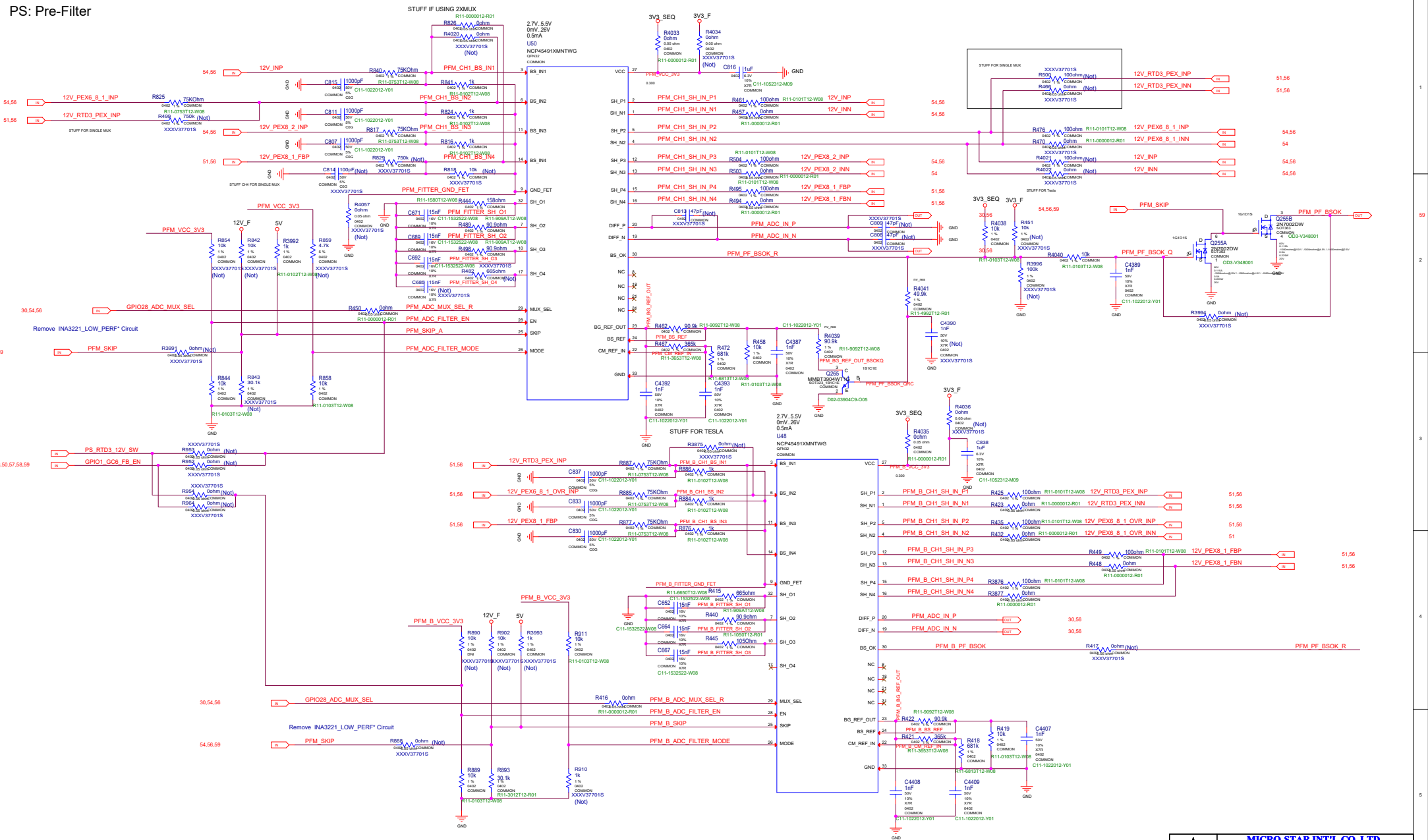
STUFF FOR SINGLE CONNECTOR



PS: 12V Current Steering & Hot Unplug Detect



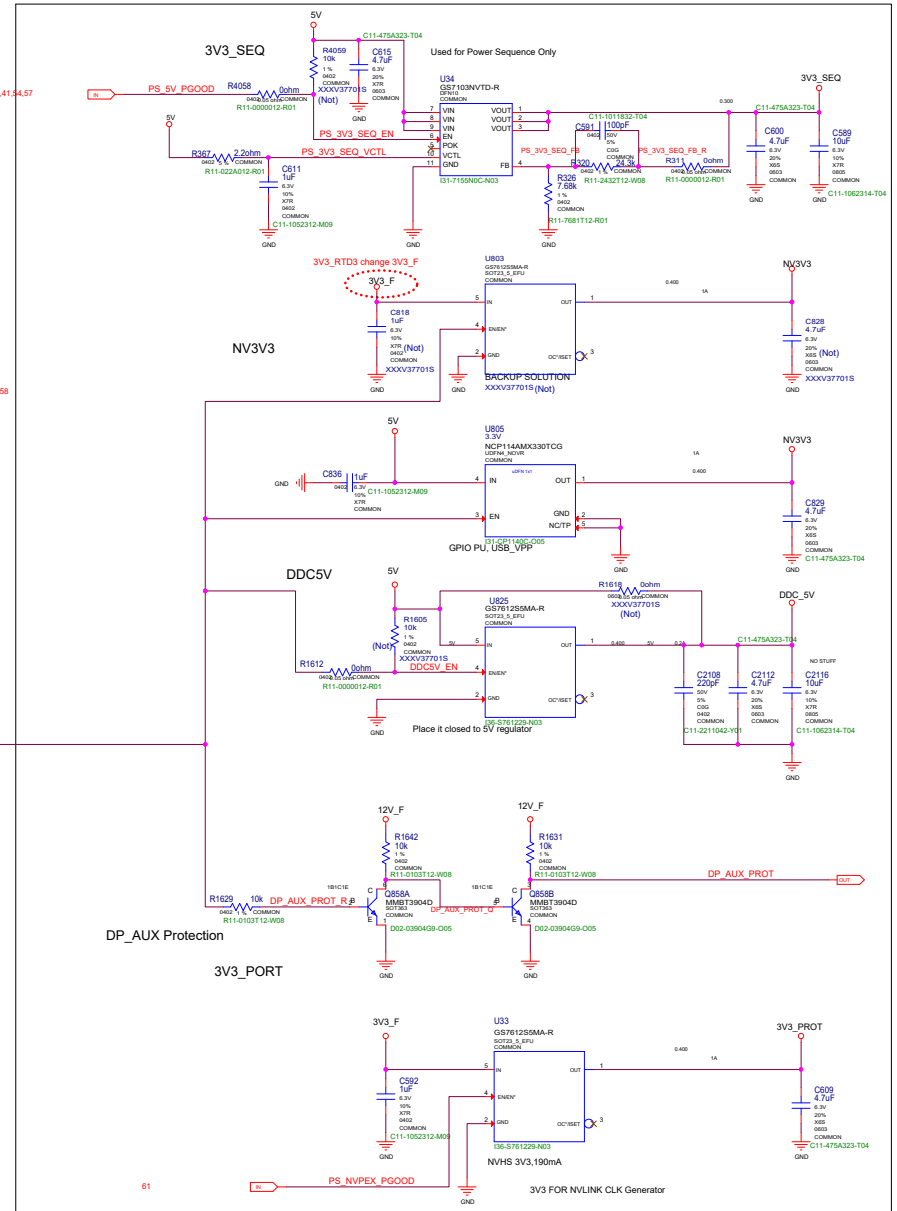
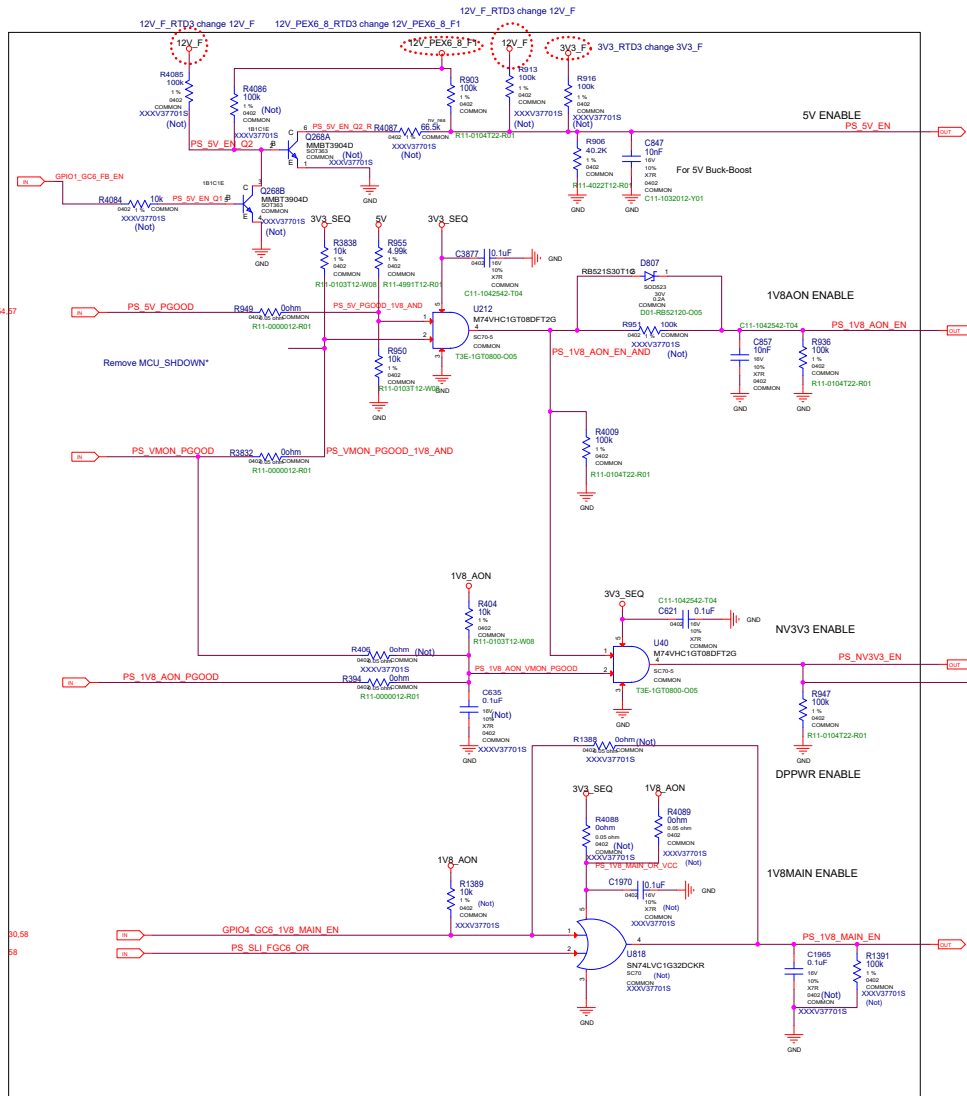
PS: Pre-Filter



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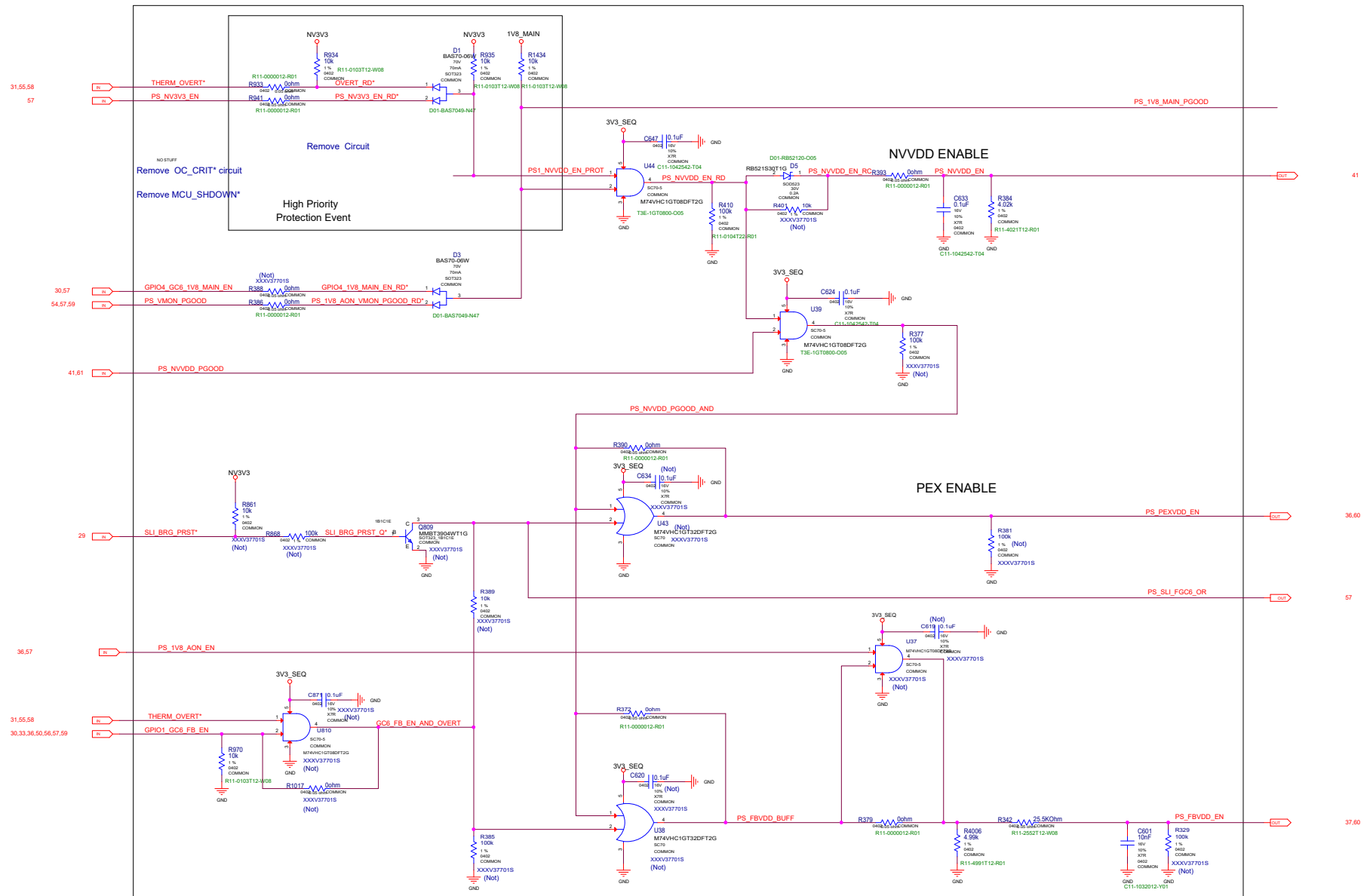
SEQUENCE:5V,1V8,NV3V3 ENABLE

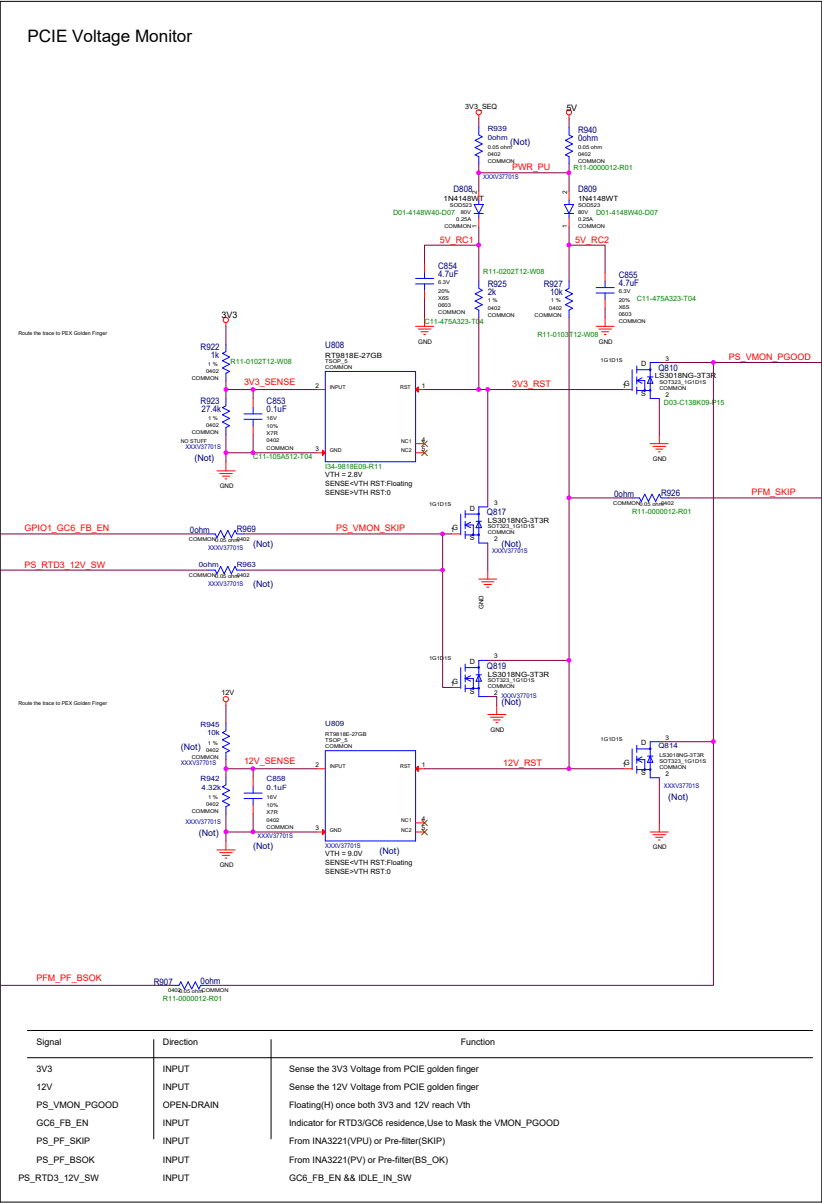


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SEQUENCE:NV,PEX,FB ENABLE





BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

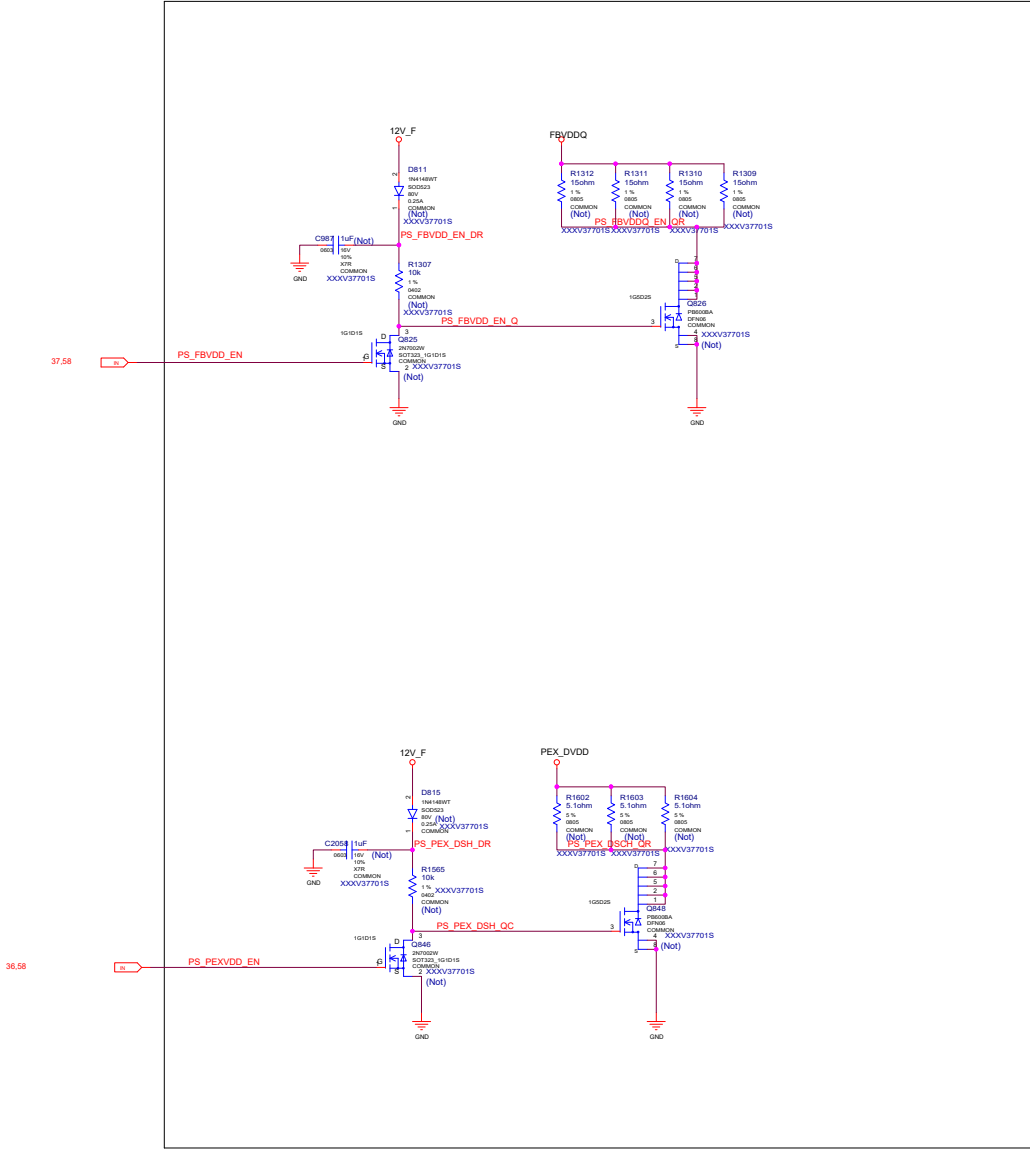
Power Supply

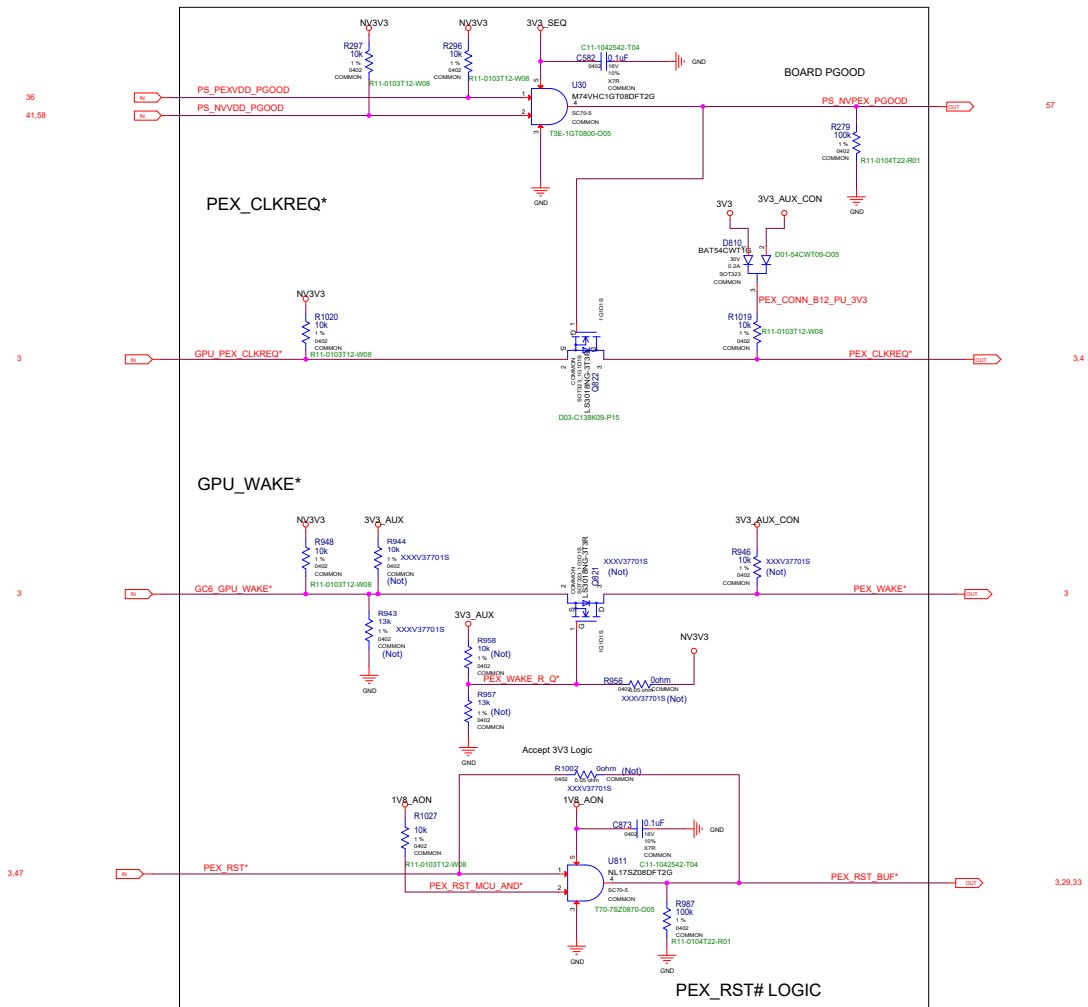
INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

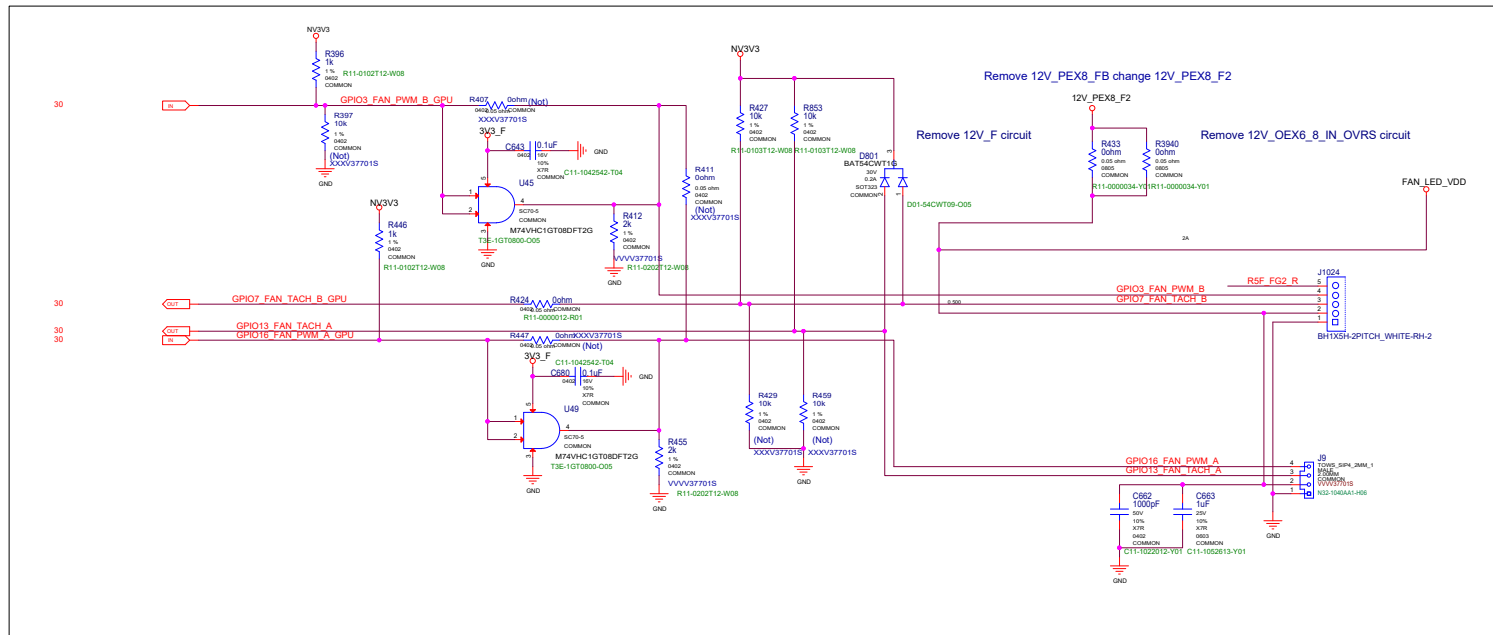
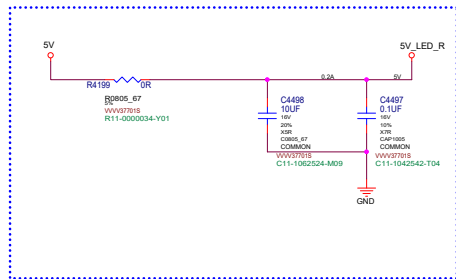
Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

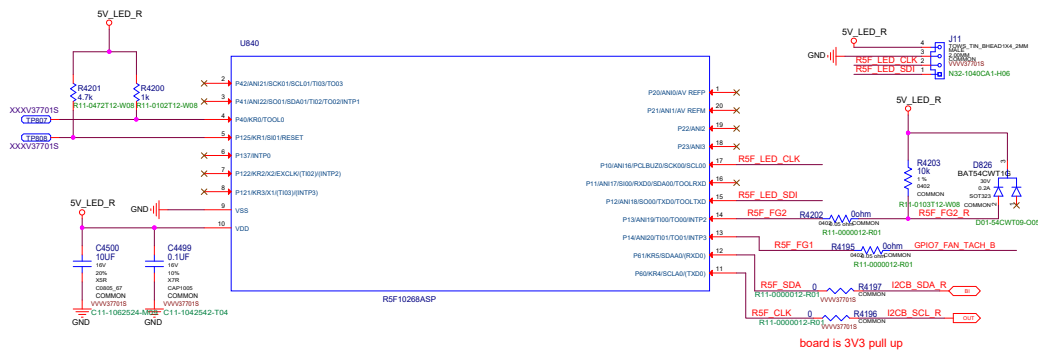




MISC: FAN



LED BOOST



board is 3V3 pull up

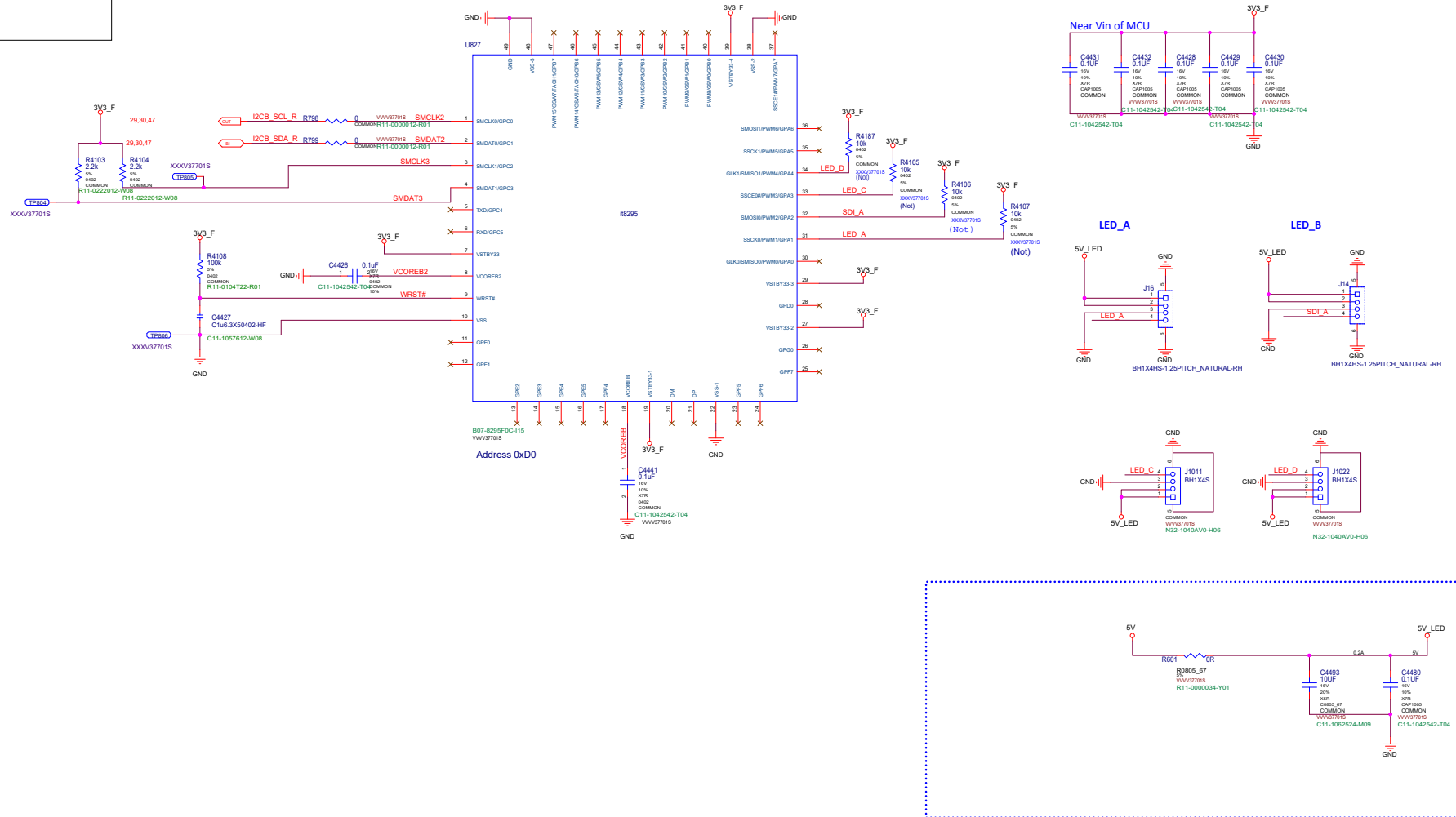


Remove LED BOOST



9/27 Remove J803
9/27 ADD TP804 / TP805

Firmware Programming Debug



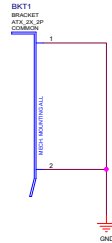
ZERO IDLE POWER MCU



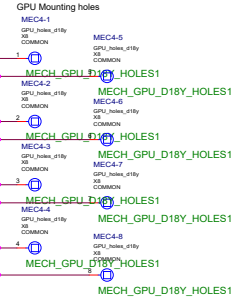
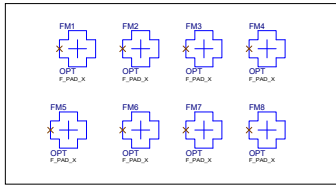
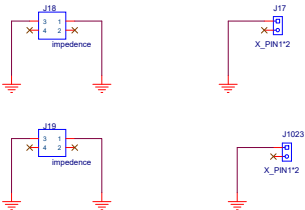
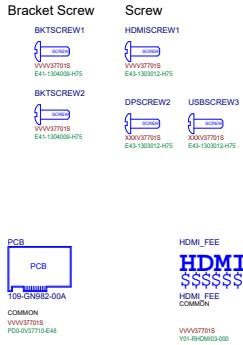
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Mechanical: Bracket/Thermal Solution

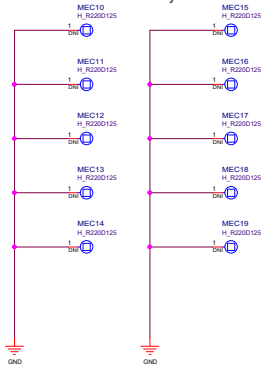
Brackets:



Bracket Screw



Mechanical Holes Symbol



VR THERMAL PROTECTION

41,42,43,44,45

IN

PS_NVVDD_TMON

R313

0ohm

0406 0.000000 12-R01

0406 0.000000 12-R01

37,39,40

IN

PS_FBVDD_TMON

R341

0ohm

0406 0.000000 12-R01

0406 0.000000 12-R01