MS8956 00A

ATI R360 9800XT, BGA 4MX32/8MX32 DDR, DUAL VGA, VIDEO IN, TV-OUT, AGP 8X, SCART

FREQUENCY	MHZ
CORE	412
MEMORY	365

MS-8956 ATI R360 9800XT

Size	Document Number	Rev
B	COVER	00A

Date: Thursday, December 04, 2003 Sheet 1 of 20

MEMORY CHANNEL A B

DDR 4M X 32 (BGA)
SHT 13

MEMORY TERMINATIONS A B
SHT 11

MA/B[14..0] MDA/B[63..0] QSA/B[7..0] CS0A/B# DQMA/B[0..7]
CASA/B# RASA/B# WEA/B# CKEA/B CLKA/B01 CLKA/B01#

MEMORY CHANNEL C D

DDR 4M X 32 (BGA)
SHT 14

MEMORY TERMINATIONS C D
SHT 12

MC/D[14..0] MDC/D[63..0] QSC/D[7..0] CS0C/D# DQMC/D[0..7]
CASC/D# RASC/D# WEA/B# CKEC/DCLKC/D01 CLKC/D01#

MEM A B

MEM C D

DAC1

R G B HSY VSY DDC1DATA DDC1CLK

PRIMARY CRT LOGIC
SHT 17

VGA1
DB15
CONN
SHT 17

STRAPS
SHT 15

BIOS
SHT 16

ROMCS#

ROM

TMDS

TMDS_TX[C,2..0]N TMDS_TX[C,2..0]P HPD, DDC2CLK DDC2DATA

INTEG TMDS LOGIC

DVI-I1
CONN
SHT 18

TVO
DVO
VIP

DVO, VIP Host, VIP Data

THEATER VIDEO-IN CONN
SHT 18

External power

FAN
SHT 16

R350
SHEET 4, 5, 6, 9, 10

Y/R C/G COMP/B H2SYNC

CRT2DDCDATA CRT2DDCCLK V2SYNC

POWER REGULATION
SHT 7,8

VDDC VDDC18 VDD VTT VDDQ
PVDD TPVDD MPVDD
A2VDD Vref

DAC2

D E M U X
SEL
SHT 18

TVOUT LOGIC
SHT 18

TVout CONN
SHT 18

GPIO

SECONDARY CRT LOGIC
SHT 17

AGP

AD31..0 CBE3..0 CPUCLK STOP# PAR REQ#
IRDY# GNT# TRDY# DEVSEL# RESET#
FRAME# CLK INTR SUSPEND# SERR#
AGPREF SBA[7..0] ST2..0 SB_STB SB_STB#
AD_STB1 AD_STB1# AD_STB0 AD_STB0# RBF#

+3.3V +5V +12V

AGP BUS 2X/4X/8X
SHT 2

MS-8956 ATI R360 9800XT

Size	Document Number	Rev
B	**BLOCK**	00A

Date: Thursday, December 04, 2003 Sheet 2 of 20

2X/4X/8X AGP BUS

GND_MPVSS GND_TPVSS GND_A2VSSN GND_AVSSQ GND_RSET GND_TVVSSN VGND
GND_AVSSN GND_PVSS GND_TXVSSR GND_A2VSSQ GND_R2SET

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

+12V_BUS C1 100uF_16V ALU
+5V_BUS C2 100uF_16V
+3.3V_BUS C3 100uF_16V

AGP_C/BE#[3..0] AGP_C/BE#[3..0] (4)
AGP_AD[31..0] AGP_AD[31..0] (4)
AGP_SBA[7..0] AGP_SBA[7..0] (4)
AGP_ST[2..0] AGP_ST[2..0] (4)

(4) AGP_INTR#
+12V_BUS +3.3V_BUS +VDDQ_BUS
TYDET R1 0R GND_TY
+3.3V_BUS +5V_BUS +VDDQ_BUS

MAGP1

A1	12V		B1	OVRCNT#	
A2	TYPEDET#	TYDET	B2	5.0V	
A3	GC_DET#/RESERVED	AGP_GC_8X_DET#	B3	5.0V#B3	
A4	USB-		B4	USB+	
A5	GND	GND_TY	B5	GND#B5	
A6	INTA#		B6	INTB#	
A7	RST#	AGP_RST#	B7	CLK	AGP_AGPCLK_R R3 0R AGP_AGPCLK (4)
A8	GNT#	(4) AGP_GNT#	B8	REQ#	AGP_REQ# (4)
A9	VCC3.3		B9	VCC3.3#B9	
A10	ST1	AGP_ST1	B10	ST0	AGP_ST0
A11	MB_DET#/RESERVED	(4) AGP_MB_8X_DET# R4 0R	B11	ST2	AGP_ST2
A12	DBI_HI/PIPE#	(4) AGP_DBI_HI R5 0R AGP_DBI_HI_R	B12	RBF#	AGP_RBF# (4)
A13	GND#A13	(4) AGP_WBF#	B13	GND#B13	AGP_DBI_LO_R R6 0R AGP_DBI_LO (4)
A14	WBF#		B14	DBI_LO/RESERVED	
A15	SBA1	AGP_SBA1	B15	SBA0	AGP_SBA0
A16	VCC3.3#A16		B16	VCC3.3#B16	
A17	SBA3	AGP_SBA3	B17	SBA2	AGP_SBA2
A18	SB_STB#	AGP_SBSTB# R +VDDQ_BUS R7 8K2 (4) AGP_SBSTB#	B18	SB_STB	AGP_SBSTB_R R8 0R AGP_SBSTB (4)
A19	GND#A19		B19	GND#B19	
A20	SBA5	AGP_SBA5	B20	SBA4	AGP_SBA4
A21	SBA7	AGP_SBA7	B21	SBA6	AGP_SBA6
A22	RESERVED		B22	RESERVED#B22	
A23	GND#A23		B23	GND#B23	
A24	RESERVED#A24		B24	3.3VAUX	
A25	VCC3.3#A25		B25	VCC3.3#B25	
A26	AD30	AGP_AD30	B26	AD31	AGP_AD31
A27	AD28	AGP_AD28	B27	AD29	AGP_AD29
A28	VCC3.3#A28		B28	VCC3.3#B28	
A29	AD26	AGP_AD26	B29	AD27	AGP_AD27
A30	AD24	AGP_AD24	B30	AD25	AGP_AD25
A31	GND#A31	AGP_ADSTB1# R +VDDQ_BUS R9 8K2 (4) AGP_ADSTB1#	B31	GND#B31	AGP_ADSTB1_R R10 0R AGP_ADSTB1 (4)
A32	AD_STB1#		B32	AD_STB1	
A33	C/BE3#	AGP_C/BE#3	B33	AD23	AGP_AD23
A34	VDDQ1.5		B34	VDDQ1.5#B34	
A35	AD22	AGP_AD22	B35	AD21	AGP_AD21
A36	AD20	AGP_AD20	B36	AD19	AGP_AD19
A37	GND#A37		B37	GND#B37	
A38	AD18	AGP_AD18	B38	AD17	AGP_AD17
A39	AD16	AGP_AD16	B39	C/BE2#	AGP_C/BE#2
A40	VDDQ1.5#A40		B40	VDDQ1.5#B40	
A41	FRAME#	(4) AGP_FRAME#	B41	IRDY#	AGP_IRDY# (4)
A42	KEY		B42	KEY#B42	
A43	KEY#A43		B43	KEY#B43	
A44	KEY#A44		B44	KEY#B44	
A45	KEY#A45		B45	KEY#B45	
A46	TRDY#	(4) AGP_TRDY# R13 0R AGP_TRDY#_R	B46	DEVSEL#	AGP_DEVSEL#_R AGP_DEVSEL#_R (4)
A47	STOP#	(4) AGP_STOP# R15 0R AGP_STOP#_R	B47	VDDQ1.5#B47	
A48	PME#		B48	PERR#	
A49	GND#A49	AGP_PAR_R	B49	GND#B49	
A50	PAR	(4) AGP_PAR	B50	SERR#	
A51	AD15	AGP_AD15	B51	C/BE1#	AGP_C/BE#1
A52	VDDQ1.5#A52		B52	VDDQ1.5#B52	
A53	AD13	AGP_AD13	B53	AD14	AGP_AD14
A54	AD11	AGP_AD11	B54	AD12	AGP_AD12
A55	GND#A55		B55	GND#B55	
A56	AD9	AGP_AD9	B56	AD10	AGP_AD10
A57	C/BE0#	AGP_C/BE#0	B57	AD8	AGP_AD8
A58	VDDQ1.5#A58	AGP_ADSTB0# R +VDDQ_BUS R16 8K2 (4) AGP_ADSTB0#	B58	VDDQ1.5#B58	AGP_ADSTB0_R R17 0R AGP_ADSTB0 (4)
A59	AD_STB0#		B59	AD_STB0	
A60	AD6	AGP_AD6	B60	AD7	AGP_AD7
A61	GND#A61		B61	GND#B61	
A62	AD4	AGP_AD4	B62	AD5	AGP_AD5
A63	AD2	AGP_AD2	B63	AD3	AGP_AD3
A64	VDDQ1.5#A64		B64	VDDQ1.5#B64	
A65	AD0	AGP_AD0	B65	AD1	AGP_AD1
A66	VREFGC	(4) AGP_VREFGC AGP_VREFGC	B66	VREFCG	AGP_AGPREF (4)

1.5V_AGP_BUS

C4 X_10pF

DNI C1127 2.2uF

+5V_BUS
C5 100nF R19 10K
U2A 74ACT08MTC
(4,9,10,19) AGP_RESET# R22 100R
AGP_RST# PWGOOD_VDDC (8)
R854 X_180R R25 180R C731 X_100nF

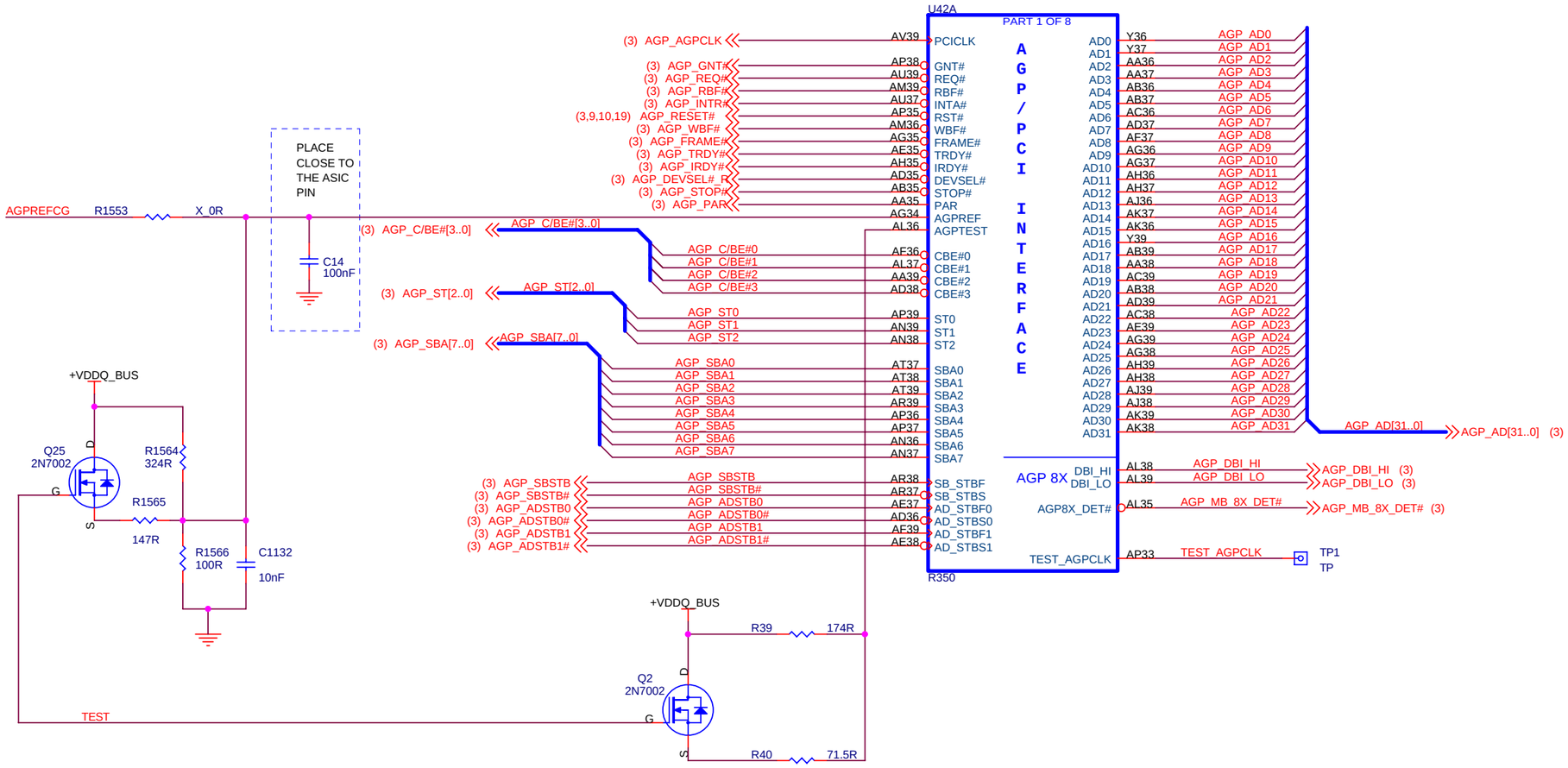
SYMBOL LEGEND

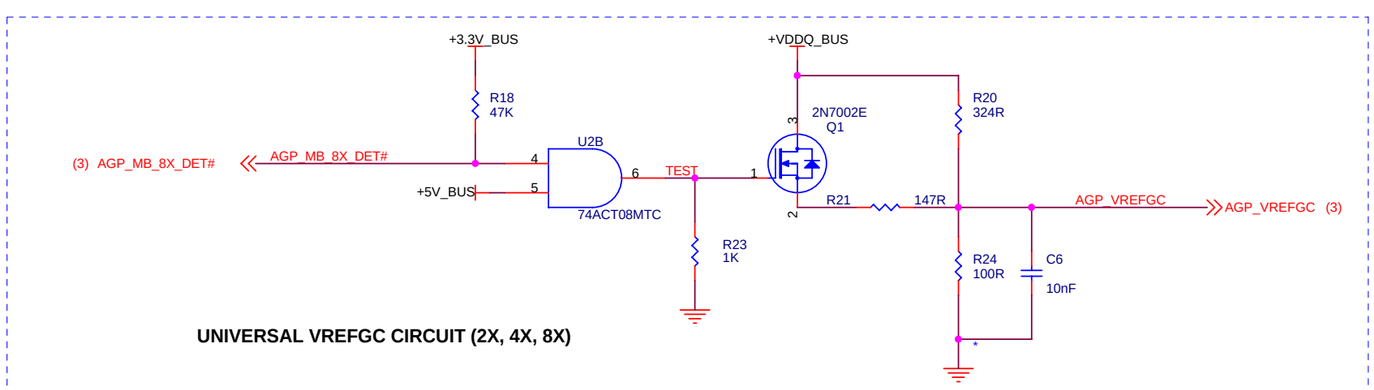
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

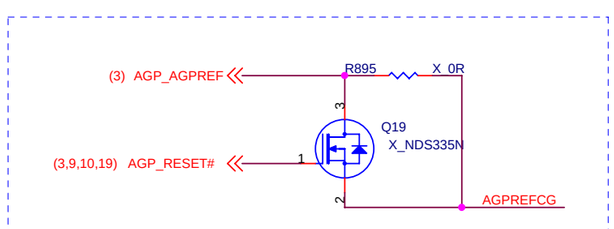
MS-8956 ATI R360 9800XT

Size	Document Number	Rev
B	AGP 4X / 8X BUS	00A

Date: Thursday, December 04, 2003 Sheet 3 of 20







MS-8956 ATI R360 9800XT		
Size B	Document Number R350_AGP	Rev 00A
Date: Thursday, December 04, 2003	Sheet 4 of 20	

APPLICATION	TVOVMODE	DVOVMODE	
TVout w/ Rage Theatre	0V	X	
ext 24b DDR TMDS	VDDC18	VDDC18	
ext 12b DDR TMDS&TVout	0V	VDDC18	VIA 1623M used
24b SDR TMDS	0V	0V	Theater used

Note1 : PVSS, and MPVSS go to ground plane directly through their own dedicated via. No connection with other VSS..

Note2 : Separate vias for AVSSQ (A2VSSQ), and AVSSN (A2VSSN) to ground plane.

Note3 : AVDD/AVSSN power need to use a pair of short traces (20mil at least) and direct to link to AVDD & AVSSN balls, the ground return point should be near the ground trace start point.

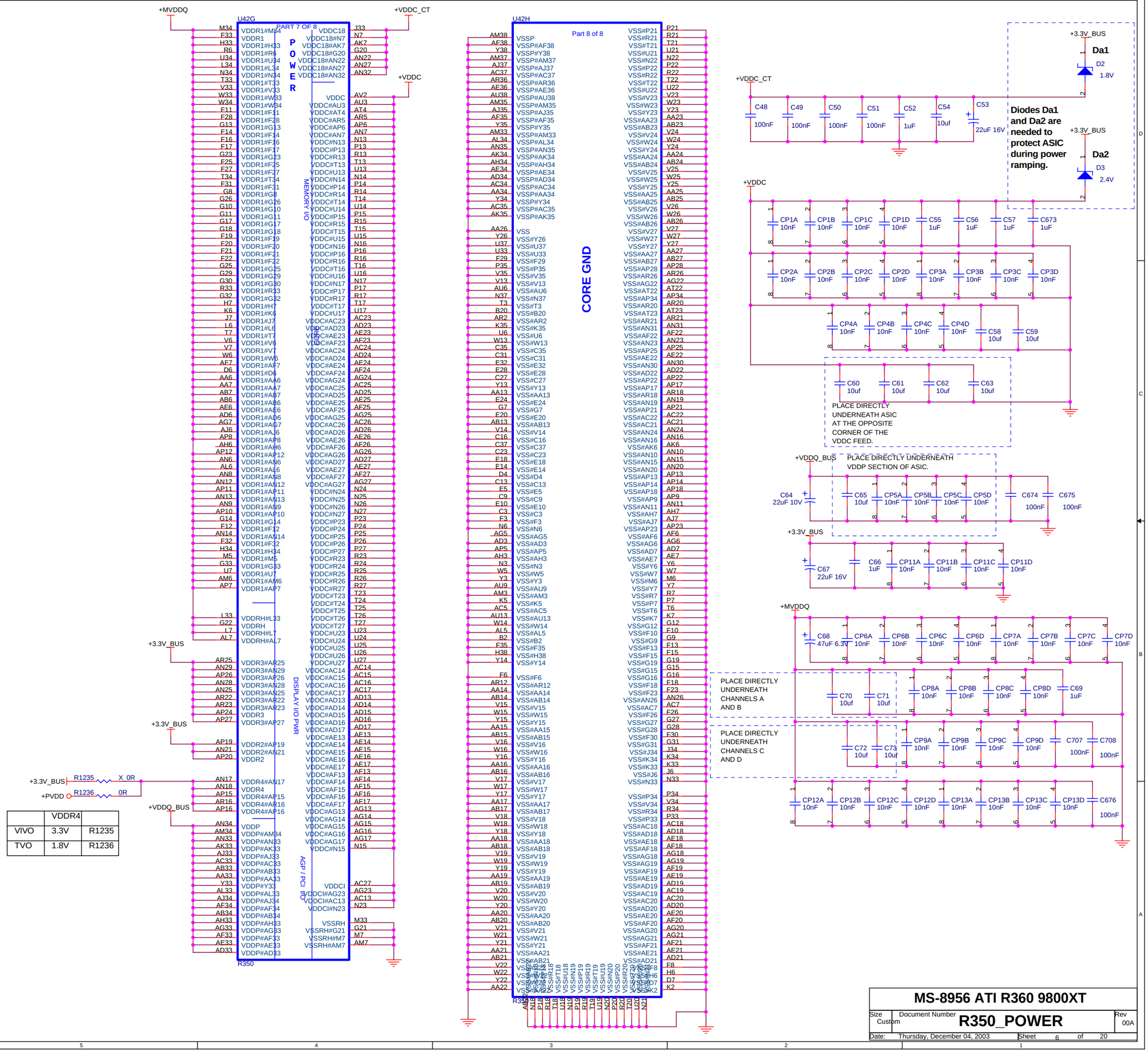
Note4: Rset resistor ground point should link to AVSSQ trace, or have via at resistor directly to ground plane.

Note5 : Populate Ra9 and Ra10 only if they are not populated on page 24 or 25 or 31 or 32.

Theater install ---- install Ra1,Ra4; remove Ra2,Ra3,Ra5; R58=330R

Theater not install ---- install Ra2,Ra3,Ra5; remove Ra1,Ra4; R58=0R

MS-8956 ATI R360 9800XT		
Size B	Document Number R350_MAIN	Rev 00A
Date: Thursday, December 04, 2003	Sheet 5 of 20	



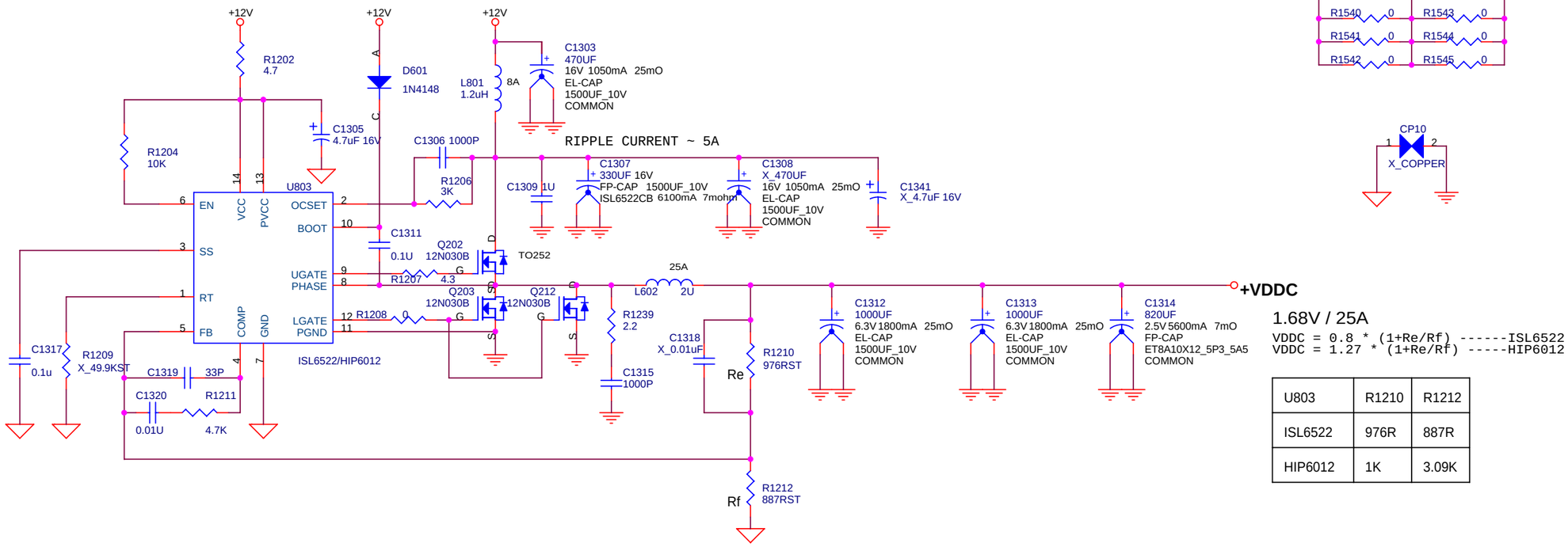
	VDDR4	
VIVO	3.3V	R1235
TVO	1.8V	R1236

MS-8956 ATI R360 9800XT

Size	Document Number	Rev
Custom	R350_POWER	00A

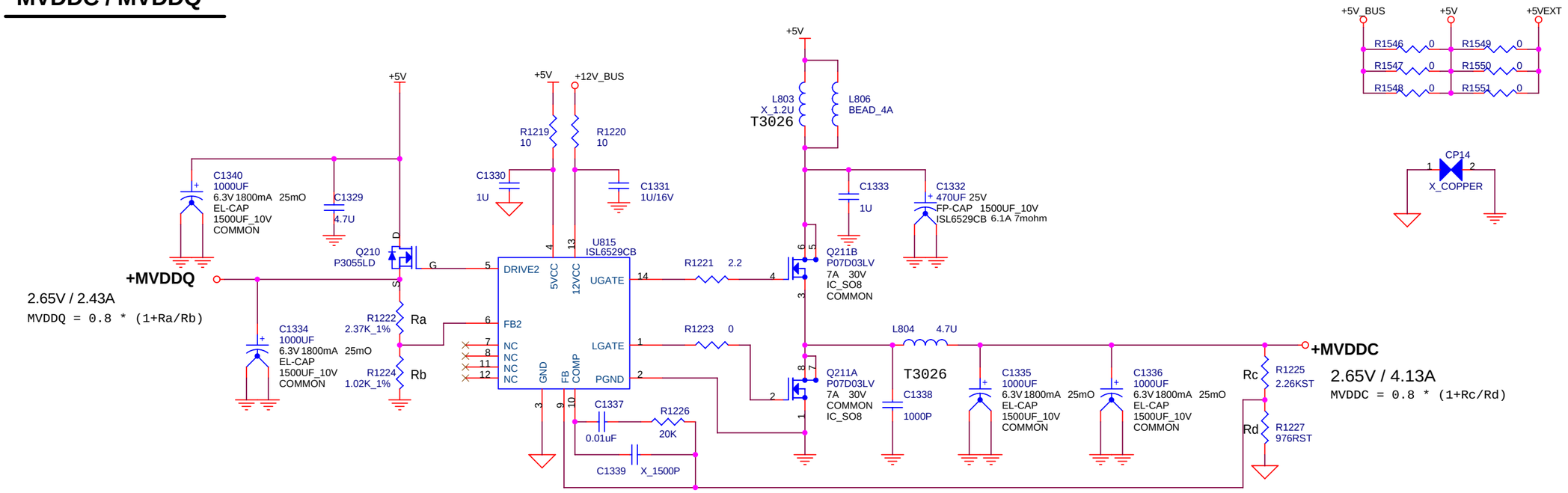
Date: Thursday, December 04, 2003 Sheet 6 of 20

VDDC



U803	R1210	R1212
ISL6522	976R	887R
HIP6012	1K	3.09K

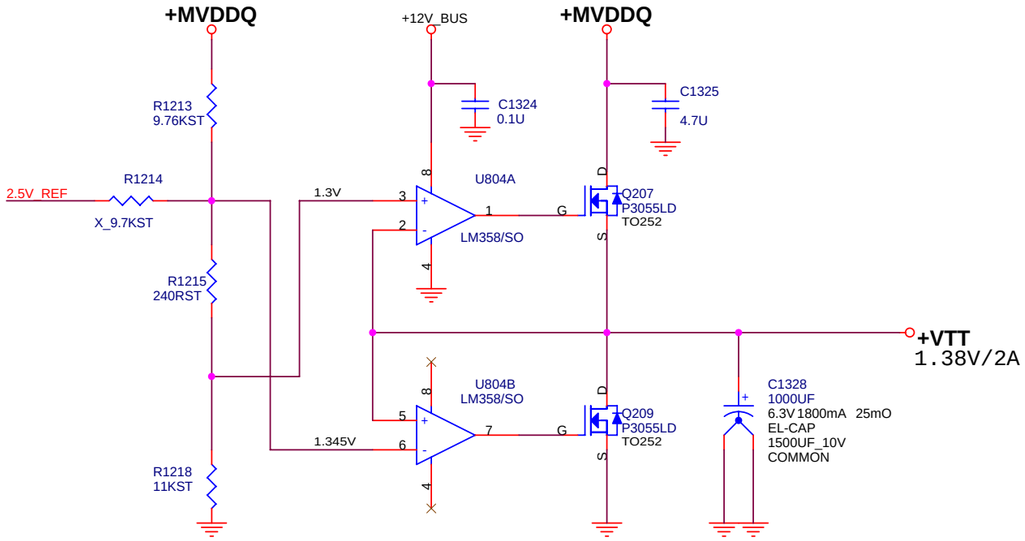
MVDDC / MVDDQ



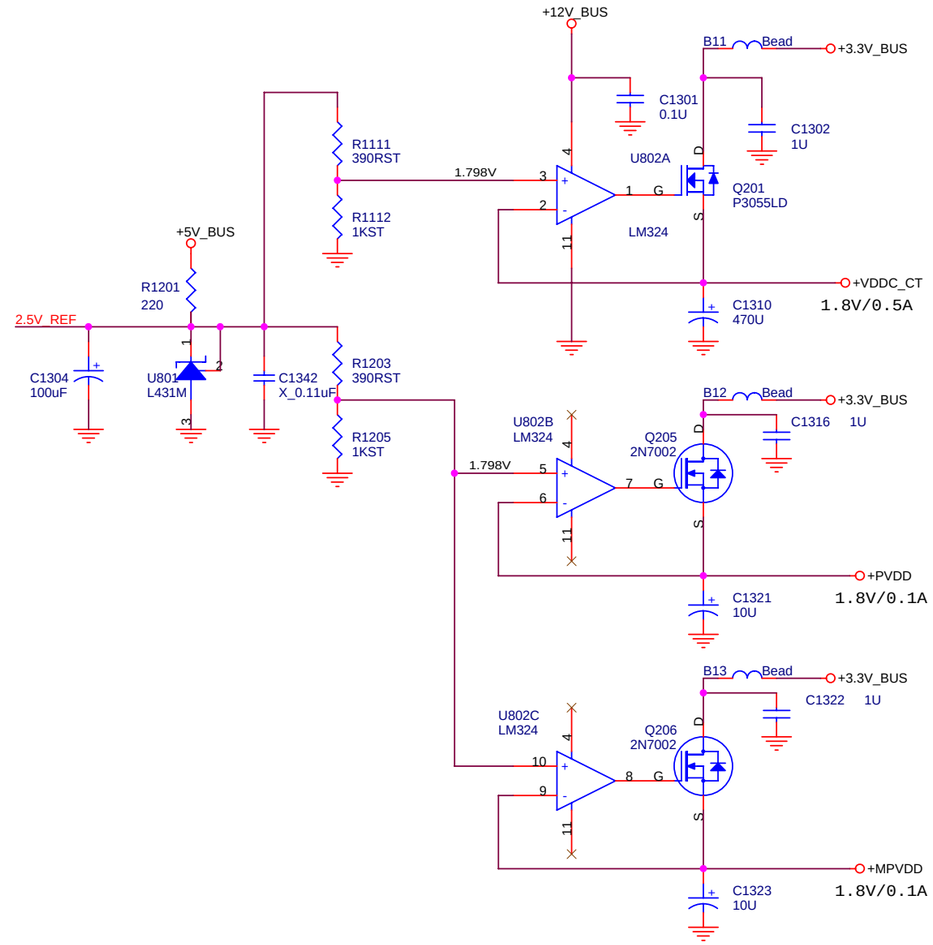
Size: Custom	Document Number: REGULATOR FOR GPU AND MEMORY	Rev: 00A
Date: Thursday, December 04, 2003	Sheet 7 of 20	

MS-8956 ATI R360 9800XT

VTT

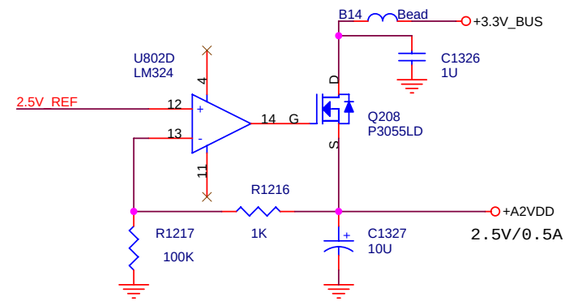


VDDC_CT / PVDD / MPVDD (1.8V)

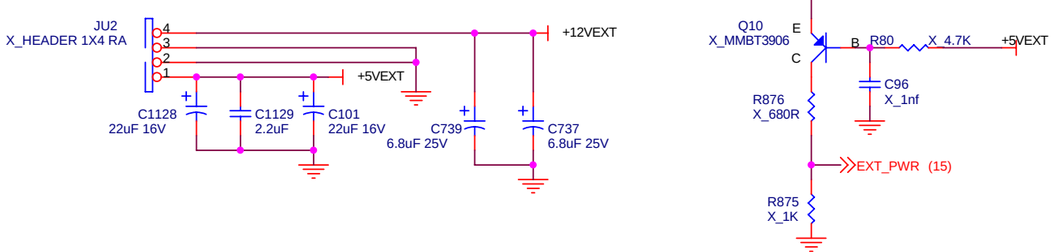


POWER SEQUENCE

A2VDD (2.5V)



EXTERNAL POWER DETECT

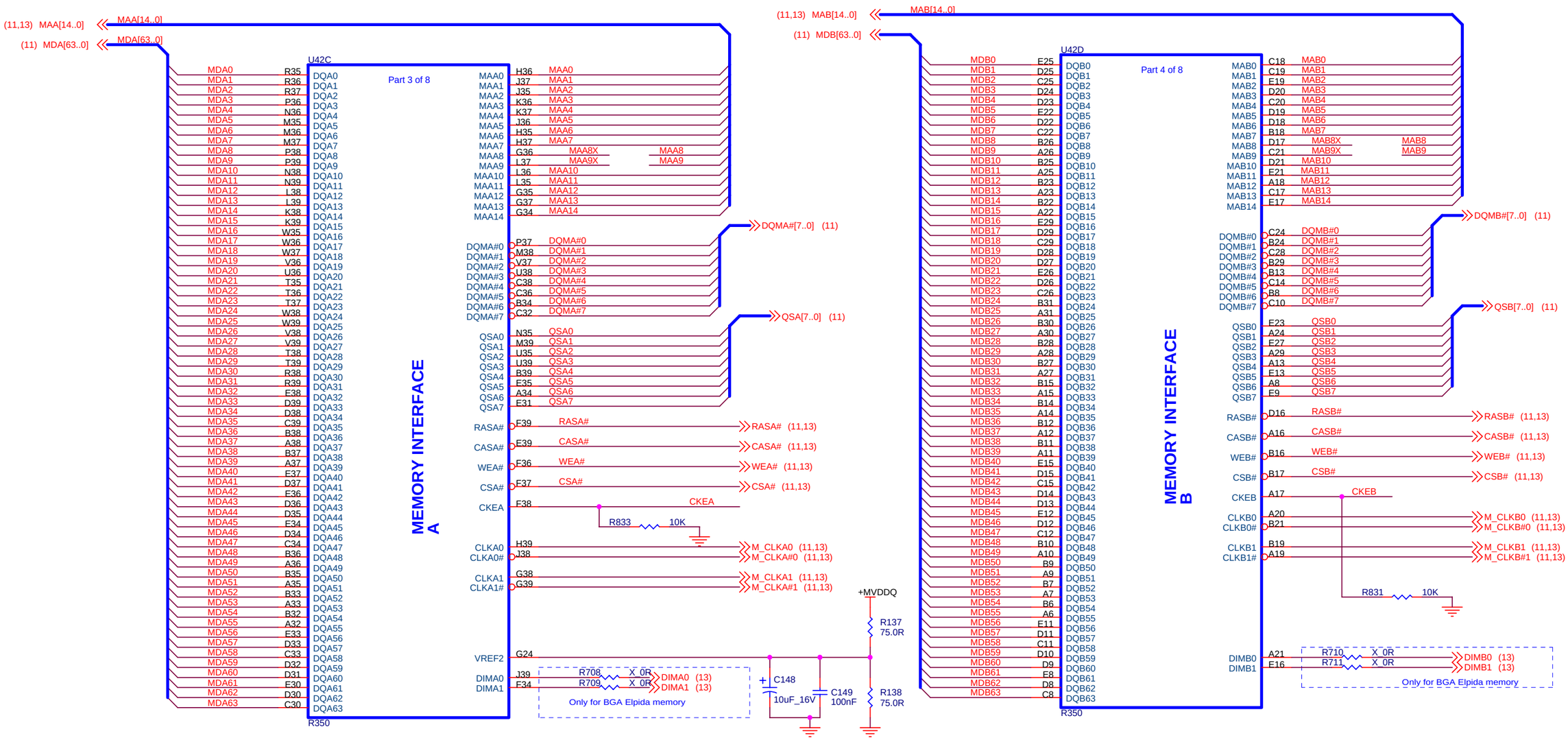


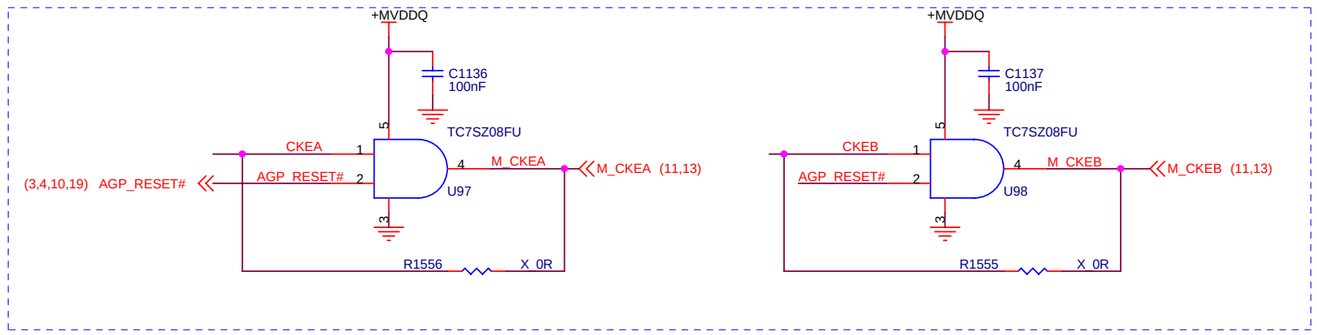
MS-8956 ATI R360 9800XT

Size	Document Number	Rev
Custom	REGULATOR FOR VTT AND OTHERS	00A
Date: Thursday, December 04, 2003	Sheet 8 of 20	

R360
MEMORY CHANNELS A and B

MEMORY SIZE	4MX32	8MX32
MAA8X MAB8X	MAA8 MAB8	MAA9 MAB9
MAA9X MAB9X	MAA9 MAB9	MAA8 MAB8

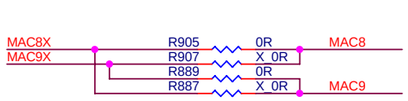




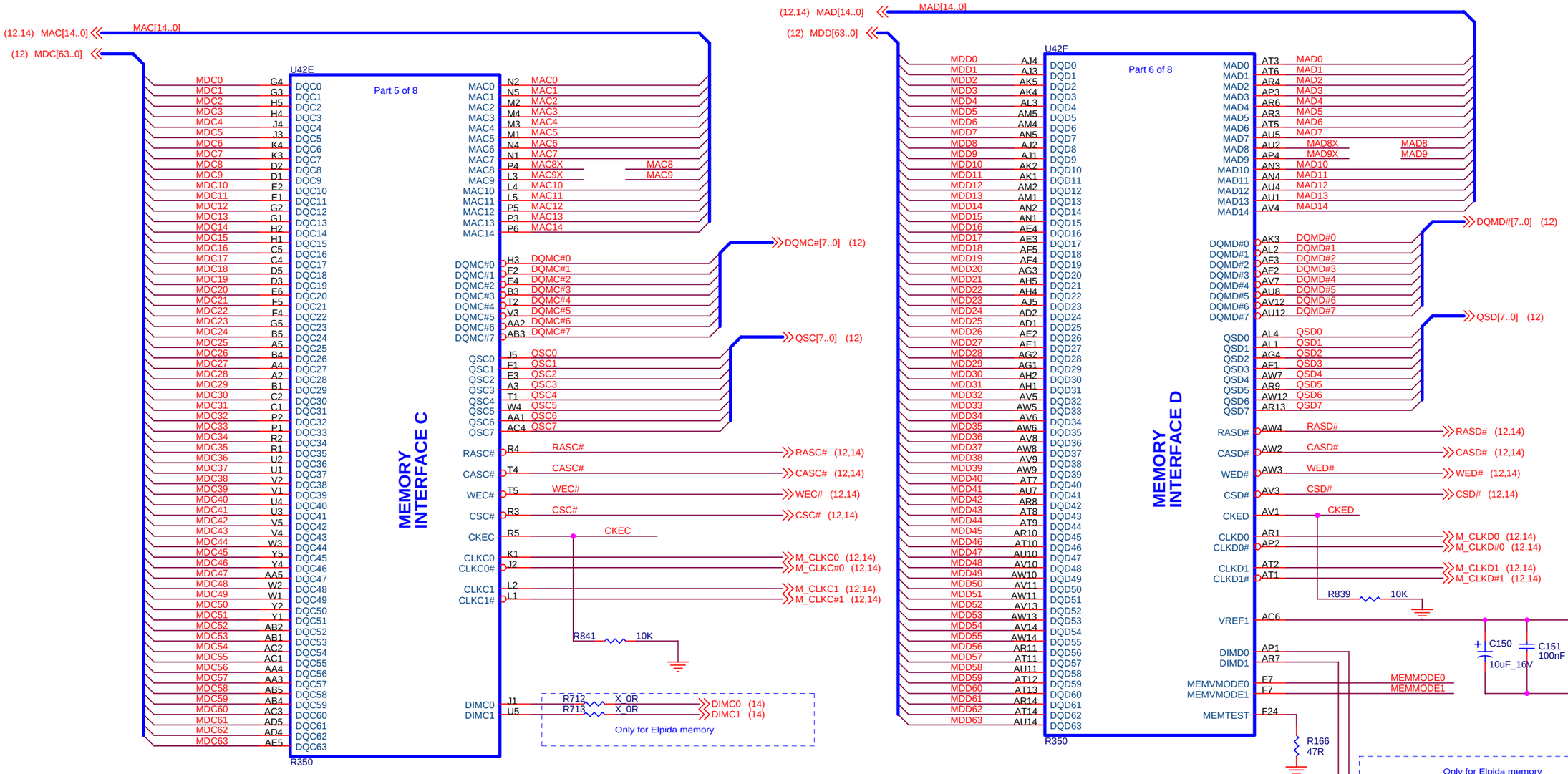
MS-8956 ATI R360 9800XT

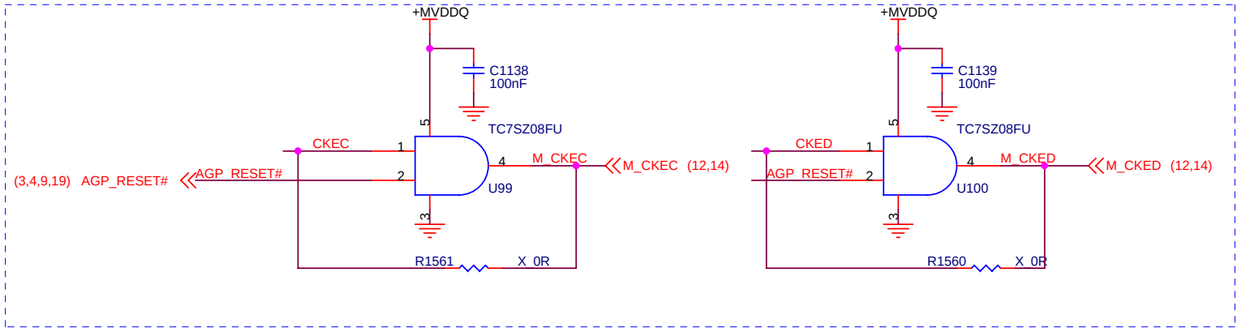
Size	Document Number	Rev
B	R350_MEMORY CHANNEL A / B	00A
Date: Thursday, December 04, 2003	Sheet 9 of 20	

R360
MEMORY CHANNELS C and D



MEMORY SIZE	4MX32	8MX32
MAC8X MAD8X	MAC8 MAD8	MAC9 MAD9
MAC9X MAD9X	MAC9 MAD9	MAC8 MAD8





MEMVMODE[1:0]	MEMORY IO VOLTAGE
0 1	2.5V (DDR)
1 0	1.8V (DDR)
1 1	3.3V (SDR)

MS-8956 ATI R360 9800XT

Size	Document Number	Rev
B	R350_MEMORY CHANNEL C / D	00A

Date: Thursday, December 04, 2003 Sheet 10 of 20

Vtt TERMINATION for DDR

MDA[63..0] → MDA[63..0] (9)
MAA[14..0] → MAA[14..0] (9,13)
M_MDA[63..0] → M_MDA[63..0] (13)

+VTT
+MVDDQ

RP1A–RP1D, RP2A–RP2D, RP3A–RP3D, RP4A–RP4D, RP5A–RP5D, RP6A–RP6D, RP7A–RP7D, RP8A–RP8D, RP9A–RP9D, RP10A–RP10D, RP11A–RP11D, RP12A–RP12D, RP13A–RP13D, RP14A–RP14D, RP15A–RP15D, RP16A–RP16D, RP17A–RP17D, RP18A–RP18D, RP19A–RP19D, RP20A–RP20D: 56R MDA0 … MDA63

C152 100nF, C154 100nF, C156 100nF, C158 100nF, C161 100nF, C162 100nF, C164 100nF, C166 100nF, C168 100nF, C170 100nF, C173 100nF, C175 100nF, C177 100nF

RP25A–RP25D, RP26A–RP26D, RP27A–RP27D, RP28A–RP28D, RP29A–RP29D, RP30A–RP30D, RP31A–RP31D, RP32A–RP32D, RP33A–RP33D, RP34A–RP34D, RP35A–RP35D, RP36A–RP36D, RP37A–RP37D, RP38A–RP38D, RP39A–RP39D, RP40A–RP40D: 47R MDA0 … MDA63 → M_MDA0 … M_MDA63

MAA0 … MAA14 → M_MAA0 … M_MAA14 (9,13)

WEA# → M_WEA# (9,13)
RASA# → M_RASA# (9,13)
CASA# → M_CASA# (9,13)
CSA# → M_CSA# (9,13)

R189, R190, R192, R194, R196, R198, R200, R202: 56R DQMA#0 … DQMA#7

RP23B 56R WEA#
RP23C 56R CASA#
RP20C 56R RASA#
RP23A 56R CSA#

DQMA#[7..0] (9)
WEA# (9,13)
CASA# (9,13)
RASA# (9,13)
CSA# (9,13)

Rf

R776 56R M_CLK0
R778 56R M_CLK#0
R780 56R M_CLK1
R782 56R M_CLK#1

M_CLKA0 (9,13)
M_CLKA#0 (9,13)
M_CLKA1 (9,13)
M_CLKA#1 (9,13)

C179 22uF

+VTT
R832 X 56R M_CKEA → M_CKEA (9,13)

M_QSA[7..0] (13)

R718 56R QSA0 R208 56R M_QSA0
R719 56R QSA1 R210 56R M_QSA1
R720 56R QSA2 R212 56R M_QSA2
R721 56R QSA3 R214 56R M_QSA3
R722 56R QSA4 R216 56R M_QSA4
R723 56R QSA5 R218 56R M_QSA5
R724 56R QSA6 R220 56R M_QSA6
R725 56R QSA7 R222 56R M_QSA7

QSA0 … QSA7 → QSA[7..0] (9)

RP23D 5 4 56R
RP66D 5 4 56R

RP46A–RP46D, RP47A–RP47D, RP48A–RP48D, RP49A–RP49D, RP50A–RP50D, RP51A–RP51D, RP52A–RP52D, RP53A–RP53D, RP54A–RP54D, RP55A–RP55D, RP56A–RP56D, RP57A–RP57D, RP58A–RP58D, RP59A–RP59D, RP60A–RP60D, RP61A–RP61D, RP62A–RP62D, RP63A–RP63D, RP64A–RP64D, RP65A–RP65D: 56R MDB0 … MDB63

C153 100nF, C155 100nF, C157 100nF, C159 100nF, C160 100nF, C163 100nF, C165 100nF, C167 100nF, C169 100nF, C171 100nF, C172 100nF, C174 100nF, C176 100nF

RP75A–RP75D, RP76A–RP76D, RP77A–RP77D, RP78A–RP78D, RP79A–RP79D, RP80A–RP80D, RP81A–RP81D, RP82A–RP82D, RP83A–RP83D, RP84A–RP84D, RP85A–RP85D, RP86A–RP86D, RP87A–RP87D, RP88A–RP88D, RP89A–RP89D, RP90A–RP90D: 47R MDB0 … MDB63 → M_MDB0 … M_MDB63

MDB[63..0] → MDB[63..0] (9)
MAB[14..0] → MAB[14..0] (9,13)
M_MDB[63..0] → M_MDB[63..0] (13)

WEB# → M_WEB# (9,13)
RASB# → M_RASB# (9,13)
CASB# → M_CASB# (9,13)
CSB# → M_CSB# (9,13)

+VTT
R830 X 4.7K M_CKEB → M_CKEB (9,13)

R191, R193, R195, R197, R199, R201, R203, R204: 56R DQMB#0 … DQMB#7

RP66B 56R WEB#
RP66C 56R CASB#
RP65C 56R RASB#
RP66A 56R CSB#

DQMB#[7..0] (9)
WEB# (9,13)
CASB# (9,13)
RASB# (9,13)
CSB# (9,13)

Rff

R775 56R M_CLKB0
R777 56R M_CLKB#0
R779 56R M_CLKB1
R781 56R M_CLKB#1

M_CLKB0 (9,13)
M_CLKB#0 (9,13)
M_CLKB1 (9,13)
M_CLKB#1 (9,13)

C178 22uF

M_QSB[7..0] (13)

R726 56R QSB0 R207 56R M_QSB0
R727 56R QSB1 R209 56R M_QSB1
R728 56R QSB2 R211 56R M_QSB2
R729 56R QSB3 R213 56R M_QSB3
R730 56R QSB4 R215 56R M_QSB4
R731 56R QSB5 R217 56R M_QSB5
R732 56R QSB6 R219 56R M_QSB6
R733 56R QSB7 R221 56R M_QSB7

Differential CLOCK termination

Either Rf or Rf1,Rf2, Rf3, Rf4, Cf1, Cf2 should be mounted. Differential termination should be placed close to the memory.

M_CLKA1 — R826 56R — Rf1 — Cf1 C711 10nF — Rf2 R169 56R — M_CLKA#1
M_CLKA0 — R827 56R — Rf3 — Cf2 C712 10nF — Rf4 R170 56R — M_CLKA#0

Differential CLOCK termination

Either Rff or Rf5,Rf6, Rf7, Rf8, Cf3, Cf4 should be mounted. Differential termination should be placed close to the memory.

M_CLKB1 — R828 56R — Rf5 — Cf3 C713 10nF — Rf6 R172 56R — M_CLKB#1
M_CLKB0 — R829 56R — Rf7 — Cf4 C714 10nF — Rf8 R171 56R — M_CLKB#0

M_DQMA#[7..0] (13)

DQMA#0 R173 47R M_DQMA#0
DQMA#1 R174 47R M_DQMA#1
DQMA#2 R175 47R M_DQMA#2
DQMA#3 R176 47R M_DQMA#3
DQMA#4 R177 47R M_DQMA#4
DQMA#5 R178 47R M_DQMA#5
DQMA#6 R179 47R M_DQMA#6
DQMA#7 R180 47R M_DQMA#7

M_DQMB#[7..0] (13)

DQMB#0 R181 47R M_DQMB#0
DQMB#1 R182 47R M_DQMB#1
DQMB#2 R183 47R M_DQMB#2
DQMB#3 R184 47R M_DQMB#3
DQMB#4 R185 47R M_DQMB#4
DQMB#5 R186 47R M_DQMB#5
DQMB#6 R187 47R M_DQMB#6
DQMB#7 R188 47R M_DQMB#7

M_MAB[14..0] (9,13)

MAB0 … MAB14 → M_MAB0 … M_MAB14

QSB[7..0] (9)

QSB0 … QSB7

MS-8956 ATI R360 9800XT

Size	Document Number	Rev
B	VTT TERMINATION A / B	00A
Date: Thursday, December 04, 2003	Sheet 11 of 20	

Vtt TERMINATION for DDR

MDC[63..0] (10)
MAC[14..0] (10,14)
M_MDC[63..0] (14)
MDD[63..0] (10)
MAD[14..0] (10,14)
M_MDD[63..0] (14)

+VTT
+MVDDQ

RP91A RP91B RP91C RP91D RP92A RP92B RP92C RP92D RP93A RP93B RP93C RP93D RP94A RP94B RP94C RP94D RP95A RP95B RP95C RP95D RP96A RP96B RP96C RP96D RP97A RP97B RP97C RP97D RP98A RP98B RP98C RP98D RP99A RP99B RP99C RP99D RP100A RP100B RP100C RP100D RP101A RP101B RP101C RP101D RP102A RP102B RP102C RP102D RP103A RP103B RP103C RP103D RP104A RP104B RP104C RP104D RP105A RP105B RP105C RP105D RP106A RP106B RP106C RP106D — 56R MDC0 … MDC63

C180 C182 C184 C186 C189 C190 C192 C194 — 100nF

RP108D RP109A RP108C RP107C RP107B RP108B RP109B RP110B RP110A RP108A RP107D RP107A RP109C RP109D RP110D — 56R MAC0 … MAC14

C197 C199 — 100nF

RP111A RP111B RP111C RP111D RP112A RP112B RP112C RP112D RP113A RP113B RP113C RP113D RP114A RP114B RP114C RP114D RP115A RP115B RP115C RP115D RP116A RP116B RP116C RP116D RP117A RP117B RP117C RP117D RP118A RP118B RP118C RP118D RP119A RP119B RP119C RP119D RP120A RP120B RP120C RP120D RP121A RP121B RP121C RP121D RP122A RP122B RP122C RP122D RP123A RP123B RP123C RP123D RP124A RP124B RP124C RP124D RP125A RP125B RP125C RP125D RP126A RP126B RP126C RP126D — 47R

MDC0 … MDC63 → M_MDC0 … M_MDC63
MAC0 … MAC14 → M_MAC0 … M_MAC14

WEC# RASC# CASC# CSC# → M_WEC# M_RASC# M_CASC# M_CSC# (10,14)

R244 R246 R248 R250 R252 R254 R256 R258 — 56R DQMC#0 … DQMC#7

C200 — 100nF

DQMC#[7..0] (10)

RP132B RP132C RP110C RP132A — 56R WEC# CASC# RASC# CSC#

C203 — 100nF

WEC# (10,14)
CASC# (10,14)
RASC# (10,14)
CSC# (10,14)

Rp

R784 R786 R788 R790 — 56R M_CLKC0 M_CLKC#0 M_CLKC1 M_CLKC#1

M_CLKC0 (10,14)
M_CLKC#0 (10,14)
M_CLKC1 (10,14)
M_CLKC#1 (10,14)

R734 R735 R736 R737 R738 R739 R740 R741 — 56R QSC0 … QSC7 — R262 R264 R266 R268 R270 R272 R274 R276 — 56R M_QSC0 … M_QSC7

M_QSC[7..0] (14)
QSC[7..0] (10)

QSC0 QSC1 QSC2 QSC3 QSC4 QSC5 QSC6 QSC7

C205 — 100nF

C207 22uF

RP132D 5 4 56R
RP156D 5 4 56R

RP136A RP136B RP136C RP136D RP137A RP137B RP137C RP137D RP138A RP138B RP138C RP138D RP139A RP139B RP139C RP139D RP140A RP140B RP140C RP140D RP141A RP141B RP141C RP141D RP142A RP142B RP142C RP142D RP143A RP143B RP143C RP143D RP144A RP144B RP144C RP144D RP145A RP145B RP145C RP145D RP146A RP146B RP146C RP146D RP147A RP147B RP147C RP147D RP148A RP148B RP148C RP148D RP149A RP149B RP149C RP149D RP150A RP150B RP150C RP150D RP151A RP151B RP151C RP151D — 56R MDD0 … MDD63

C181 C183 C185 C187 C188 C191 C193 C195 — 100nF

RP153D RP154A RP153C RP152C RP152B RP153B RP154B RP155B RP155A RP153A RP152D RP152A RP154C RP154D RP155D — 56R MAD0 … MAD14

C196 C198 — 100nF

RP160A RP160B RP160C RP160D RP161A RP161B RP161C RP161D RP162A RP162B RP162C RP162D RP163A RP163B RP163C RP163D RP164A RP164B RP164C RP164D RP165A RP165B RP165C RP165D RP166A RP166B RP166C RP166D RP167A RP167B RP167C RP167D RP168A RP168B RP168C RP168D RP169A RP169B RP169C RP169D RP170A RP170B RP170C RP170D RP171A RP171B RP171C RP171D RP172A RP172B RP172C RP172D RP173A RP173B RP173C RP173D RP174A RP174B RP174C RP174D RP175A RP175B RP175C RP175D — 47R

MDD0 … MDD63 → M_MDD0 … M_MDD63

WED# RASD# CASD# → M_WED# M_RASD# M_CASD# (10,14)
CSD# → M_CSD# (10,14)

R243 R245 R247 R249 R251 R253 R255 R257 — 56R DQMD#0 … DQMD#7

C201 — 100nF

DQMD#[7..0] (10)

+VTT R838 X_56R M_CKED → M_CKED (10,14)

RP156B RP156C RP155C RP156A — 56R WED# CASD# RASD# CSD#

C202 — 100nF

WED# (10,14)
CASD# (10,14)
RASD# (10,14)
CSD# (10,14)

Rpp

R783 R785 R787 R789 — 56R M_CLKD0 M_CLKD#0 M_CLKD1 M_CLKD#1

M_CLKD0 (10,14)
M_CLKD#0 (10,14)
M_CLKD1 (10,14)
M_CLKD#1 (10,14)

R742 R743 R744 R745 R746 R747 R748 R749 — 56R QSD0 … QSD7 — R261 R263 R265 R267 R269 R271 R273 R275 — 56R M_QSD0 … M_QSD7

M_QSD[7..0] (14)

C204 — 100nF

C206 22uF

Differential CLOCK termination

Either Rp or Rg1,Rg2, Rg3, Rg4, Cg1, Cg2 should be mounted. Differential termination should be placed close to the memory.

M_CLKC1 — R834 56R — Rg1 — Cg1 C715 10nF — Rg2 R224 56R — M_CLKC#1
M_CLKC0 — R835 56R — Rg3 — Cg2 C716 10nF — Rg4 R223 56R — M_CLKC#0

Differential CLOCK termination

Either Rpp or Rg5,Rg6, Rg7, Rg8, Cg3, Cg4 should be mounted. Differential termination should be placed close to the memory.

M_CLKD1 — R836 56R — Rg5 — Cg3 C717 10nF — Rg6 R226 56R — M_CLKD#1
M_CLKD0 — R837 56R — Rg7 — Cg4 C718 10nF — Rg8 R225 56R — M_CLKD#0

M_DQMC#[7..0] (14)

DQMC#0 … DQMC#7 — R227 R228 R229 R230 R231 R232 R233 R234 — 47R — M_DQMC#0 … M_DQMC#7

M_DQMD#[7..0] (14)

DQMD#0 … DQMD#7 — R235 R236 R237 R238 R239 R240 R241 R242 — 47R — M_DQMD#0 … M_DQMD#7

M_MAD[14..0] (10,14)

MAD0 … MAD14 → M_MAD0 … M_MAD14

QSD[7..0] (10)

QSD0 … QSD7

MS-8956 ATI R360 9800XT		
Size B	Document Number: VTT TERMINATION C / D	Rev 00A
Date: Thursday, December 04, 2003	Sheet 12 of 20	

64MBytes DDR 128Mbit 1Mx32x4 uBGA Channels A and B - rank 1

(11) M_DQMA#[7..0] — M_DQMA#0 … M_DQMA#7
(11) M_DQMB#[7..0] — M_DQMB#0 … M_DQMB#7
(11) M_QSA[7..0] — M_QSA0 … M_QSA7
(11) M_QSB[7..0] — M_QSB0 … M_QSB7
(9,11) M_CKEA, M_WEA#, M_CASA#, M_RASA#, M_CSA#, M_CLKA0, M_CLKA1, M_CLKA#0, M_CLKA#1, M_CKEB, M_WEB#, M_CASB#, M_RASB#, M_CSB#, M_CLKB0, M_CLKB1, M_CLKB#0, M_CLKB#1

Only for BGA Elpida memory: (9) DIMA0, (9) DIMA1, (9) DIMB0, (9) DIMB1 → DIMA0, DIMA1, DIMB0, DIMB1

(9,11) M_MAA[14..0] — M_MAA0 … M_MAA14
(9,11) M_MAB[14..0] — M_MAB0 … M_MAB14

U52

M_MAA12 M3, M_MAA13 L4, M_MAA11 L6, M_MAA10 K5, M_MAA9 L7, M_MAA8 M10, M_MAA7 M9, M_MAA6 M8, M_MAA5 L8, M_MAA4 M7, M_MAA3 M6, M_MAA2 L5, M_MAA1 M5, M_MAA0 M4
DIMA0 K11, M_MAA14 L3
+MVDDQ
R277 4.99K, R281 4.99K, C208 100nF
M_CLKA#0 L11, M_CSA# M1, M_RASA# L1, M_CASA# K1, M_WEA# K2, M_DQMA#1 A11, M_DQMA#2 G2, M_DQMA#0 G11, M_DQMA#3 A2, M_CLKA0 L10, M_CKEA M11, M_QSA1 A12, M_QSA2 G1, M_QSA0 G12, M_QSA3 A1
+MVDDC
C679 10uF, +MVDDQ C679 10uF, +MVDDQ C683 10uF
1MX32X4

U53

M_MAA12 M3, M_MAA13 L4, M_MAA11 L6, M_MAA10 K5, M_MAA9 L7, M_MAA8 M10, M_MAA7 M9, M_MAA6 M8, M_MAA5 L8, M_MAA4 M7, M_MAA3 M6, M_MAA2 L5, M_MAA1 M5, M_MAA0 M4
DIMA1 K11, M_MAA14 L3
+MVDDQ
R278 4.99K, R282 4.99K, C209 100nF
M_CLKA#1 L11, M_CSA# M1, M_RASA# L1, M_CASA# K1, M_WEA# K2, M_DQMA#5 A11, M_DQMA#6 G2, M_DQMA#4 G11, M_DQMA#7 A2, M_CLKA1 L10, M_CKEA M11, M_QSA5 A12, M_QSA6 G1, M_QSA4 G12, M_QSA7 A1
+MVDDC
+MVDDQ C680 10uF, +MVDDQ C214 10uF
1MX32X4

U54

M_MAB12 M3, M_MAB13 L4, M_MAB11 L6, M_MAB10 K5, M_MAB9 L7, M_MAB8 M10, M_MAB7 M9, M_MAB6 M8, M_MAB5 L8, M_MAB4 M7, M_MAB3 M6, M_MAB2 L5, M_MAB1 M5, M_MAB0 M4
DIMB0 K11, M_MAB14 L3
+MVDDQ
R279 4.99K, R283 4.99K, C210 100nF
M_CLKB#0 L11, M_CSB# M1, M_RASB# L1, M_CASB# K1, M_WEB# K2, M_DQMB#1 A11, M_DQMB#2 G2, M_DQMB#0 G11, M_DQMB#3 A2, M_CLKB0 L10, M_CKEB M11, M_QSB1 A12, M_QSB2 G1, M_QSB0 G12, M_QSB3 A1
+MVDDC
+MVDDQ C212 22uF_16V, +MVDDQ C682 10uF, +MVDDQ C215 10uF
1MX32X4

U55

M_MAB12 M3, M_MAB13 L4, M_MAB11 L6, M_MAB10 K5, M_MAB9 L7, M_MAB8 M10, M_MAB7 M9, M_MAB6 M8, M_MAB5 L8, M_MAB4 M7, M_MAB3 M6, M_MAB2 L5, M_MAB1 M5, M_MAB0 M4
DIMB1 K11, M_MAB14 L3
+MVDDQ
R280 4.99K, R284 4.99K, C211 100nF
M_CLKB#1 L11, M_CSB# M1, M_RASB# L1, M_CASB# K1, M_WEB# K2, M_DQMB#4 A11, M_DQMB#6 G2, M_DQMB#5 G11, M_DQMB#7 A2, M_CLKB1 L10, M_CKEB M11, M_QSB4 A12, M_QSB6 G1, M_QSB5 G12, M_QSB7 A1
+MVDDC
+MVDDQ C213 10uF, +MVDDQ C681 10uF
1MX32X4

(11) M_MDA[63..0] — M_MDA[63..0]
(11) M_MDB[63..0] — M_MDB[63..0]

Decoupling

+MVDDQ: C216 100nF, C217 100nF, C218 100nF, C219 100nF, C220 100nF, C221 100nF, C222 100nF, C223 100nF, C224 100nF, C225 100nF, C226 100nF, C227 100nF, C228 100nF, C229 100nF, C230 100nF, C231 100nF, C232 100nF, C233 100nF, C234 100nF, C235 100nF
+MVDDC: C236 100nF, C237 100nF, C238 100nF, C239 100nF, C240 100nF, C241 100nF, C242 100nF, C243 100nF, C244 100nF, C245 100nF, C246 100nF, C247 100nF, C248 100nF, C249 100nF, C250 100nF, C251 100nF, C252 100nF, C253 100nF, C254 100nF, C255 100nF

MS-8956 ATI R360 9800XT

Size	Document Number	Rev
B	BGA 4MX32 DDR A AND B	00A
Date: Thursday, December 04, 2003	Sheet 13 of 20	

64MBytes DDR 128Mbit 1Mx32x4 uBGA Channels C and D - rank1

(12) M_DQMC#[7..0] — M_DQMC#0 … M_DQMC#7
(12) M_DQMD#[7..0] — M_DQMD#0 … M_DQMD#7
(12) M_QSC[7..0] — M_QSC0 … M_QSC7
(12) M_QSD[7..0] — M_QSD0 … M_QSD7
(10,12) M_CKEC
(10,12) M_WEC#
(10,12) M_CASC#
(10,12) M_RASC#
(10,12) M_CSC#
(10,12) M_CLKC0
(10,12) M_CLKC1
(10,12) M_CLKC#0
(10,12) M_CLKC#1
(10,12) M_CKED
(10,12) M_WED#
(10,12) M_CASD#
(10,12) M_RASD#
(10,12) M_CSD#
(10,12) M_CLKD0
(10,12) M_CLKD1
(10,12) M_CLKD#0
(10,12) M_CLKD#1

(10) DIMC0 — DIMC0
(10) DIMC1 — DIMC1
(10) DIMD0 — DIMD0
(10) DIMD1 — DIMD1
Only for BGA Elpida memory

(10,12) M_MAC[14..0] — M_MAC0 … M_MAC14
(10,12) M_MAD[14..0] — M_MAD0 … M_MAD14

(12) M_MDC[63..0]
(12) M_MDD[63..0]

U56

M_MAC12 M3, M_MAC13 L4, M_MAC11 L6, M_MAC10 K5, M_MAC9 L7, M_MAC8 M10, M_MAC7 M9, M_MAC6 M8, M_MAC5 L8, M_MAC4 M7, M_MAC3 M6, M_MAC2 L5, M_MAC1 M5, M_MAC0 M4
DIMC0 K11
M_MAC14 L3
M_CLKC0 L11, M_CSC# M1, M_RASC# L1, M_CASC# K1, M_WEC# K2, M_DQMC#1 A11, M_DQMC#2 G2, M_DQMC#0 G11, M_DQMC#3 A2, M_CLKC0 L10, M_CKEC M11
M_QSC1 A12, M_QSC2 G1, M_QSC0 G12, M_QSC3 A1
M_MDC8 A7, M_MDC9 B8, M_MDC10 A8, M_MDC11 A9, M_MDC12 B12, M_MDC13 C11, M_MDC14 C12, M_MDC15 D12, M_MDC16 J2, M_MDC17 J1, M_MDC18 H1, M_MDC19 H2, M_MDC20 F1, M_MDC21 F2, M_MDC22 E1, M_MDC23 E2, M_MDC0 E11, M_MDC1 E12, M_MDC2 F11, M_MDC3 F12, M_MDC4 H11, M_MDC5 H12, M_MDC6 J11, M_MDC7 J12, M_MDC24 D1, M_MDC25 C1, M_MDC26 C2, M_MDC27 B1, M_MDC28 A4, M_MDC29 A5, M_MDC30 B5, M_MDC31 A6
+MVDDQ, +MVDDC
C684 10uF
C688 10uF
R285 4.99K
R289 4.99K
C256 100nF
1MX32X4

U57

M_MAC12 M3, M_MAC13 L4, M_MAC11 L6, M_MAC10 K5, M_MAC9 L7, M_MAC8 M10, M_MAC7 M9, M_MAC6 M8, M_MAC5 L8, M_MAC4 M7, M_MAC3 M6, M_MAC2 L5, M_MAC1 M5, M_MAC0 M4
DIMC1 K11
M_MAC14 L3
M_CLKC1 L11, M_CSC# M1, M_RASC# L1, M_CASC# K1, M_WEC# K2, M_DQMC#5 A11, M_DQMC#6 G2, M_DQMC#4 G11, M_DQMC#7 A2, M_CLKC1 L10, M_CKEC M11
M_QSC5 A12, M_QSC6 G1, M_QSC4 G12, M_QSC7 A1
M_MDC47 A7, M_MDC46 B8, M_MDC45 A8, M_MDC44 A9, M_MDC43 B12, M_MDC42 C11, M_MDC41 C12, M_MDC40 D12, M_MDC55 J2, M_MDC54 J1, M_MDC53 H1, M_MDC52 H2, M_MDC51 F1, M_MDC50 F2, M_MDC49 E1, M_MDC48 E2, M_MDC39 E11, M_MDC38 E12, M_MDC37 F11, M_MDC36 F12, M_MDC35 H11, M_MDC34 H12, M_MDC33 J11, M_MDC32 J12, M_MDC63 D1, M_MDC62 C1, M_MDC61 C2, M_MDC60 B1, M_MDC59 A4, M_MDC58 A5, M_MDC57 B5, M_MDC56 A6
+MVDDQ, +MVDDC
C685 10uF
C262 10uF
R286 4.99K
R290 4.99K
C258 100nF
1MX32X4

U58

M_MAD12 M3, M_MAD13 L4, M_MAD11 L6, M_MAD10 K5, M_MAD9 L7, M_MAD8 M10, M_MAD7 M9, M_MAD6 M8, M_MAD5 L8, M_MAD4 M7, M_MAD3 M6, M_MAD2 L5, M_MAD1 M5, M_MAD0 M4
DIMD0 K11
M_MAD14 L3
M_CLKD0 L11, M_CSD# M1, M_RASD# L1, M_CASD# K1, M_WED# K2, M_DQMD#1 A11, M_DQMD#2 G2, M_DQMD#0 G11, M_DQMD#3 A2, M_CLKD0 L10, M_CKED M11
M_QSD1 A12, M_QSD2 G1, M_QSD0 G12, M_QSD3 A1
M_MDD8 A7, M_MDD9 B8, M_MDD10 A8, M_MDD11 A9, M_MDD12 B12, M_MDD13 C11, M_MDD14 C12, M_MDD15 D12, M_MDD16 J2, M_MDD17 J1, M_MDD18 H1, M_MDD19 H2, M_MDD20 F1, M_MDD21 F2, M_MDD22 E1, M_MDD23 E2, M_MDD0 E11, M_MDD1 E12, M_MDD2 F11, M_MDD3 F12, M_MDD4 H11, M_MDD5 H12, M_MDD6 J11, M_MDD7 J12, M_MDD24 D1, M_MDD25 C1, M_MDD26 C2, M_MDD27 B1, M_MDD28 A4, M_MDD29 A5, M_MDD30 B5, M_MDD31 A6
+MVDDQ, +MVDDC
C686 10uF
C260 22uF 16V
C263 10uF
R288 4.99K
R291 4.99K
C257 100nF
1MX32X4

U59

M_MAD12 M3, M_MAD13 L4, M_MAD11 L6, M_MAD10 K5, M_MAD9 L7, M_MAD8 M10, M_MAD7 M9, M_MAD6 M8, M_MAD5 L8, M_MAD4 M7, M_MAD3 M6, M_MAD2 L5, M_MAD1 M5, M_MAD0 M4
DIMD1 K11
M_MAD14 L3
M_CLKD1 L11, M_CSD# M1, M_RASD# L1, M_CASD# K1, M_WED# K2, M_DQMD#5 A11, M_DQMD#6 G2, M_DQMD#4 G11, M_DQMD#7 A2, M_CLKD1 L10, M_CKED M11
M_QSD5 A12, M_QSD6 G1, M_QSD4 G12, M_QSD7 A1
M_MDD47 A7, M_MDD46 B8, M_MDD45 A8, M_MDD44 A9, M_MDD43 B12, M_MDD42 C11, M_MDD41 C12, M_MDD40 D12, M_MDD55 J2, M_MDD54 J1, M_MDD53 H1, M_MDD52 H2, M_MDD51 F1, M_MDD50 F2, M_MDD49 E1, M_MDD48 E2, M_MDD39 E11, M_MDD38 E12, M_MDD37 F11, M_MDD36 F12, M_MDD35 H11, M_MDD34 H12, M_MDD33 J11, M_MDD32 J12, M_MDD63 D1, M_MDD62 C1, M_MDD61 C2, M_MDD60 B1, M_MDD59 A4, M_MDD58 A5, M_MDD57 B5, M_MDD56 A6
+MVDDQ, +MVDDC
C687 10uF
C261 10uF
R287 4.99K
R292 4.99K
C259 100nF
1MX32X4

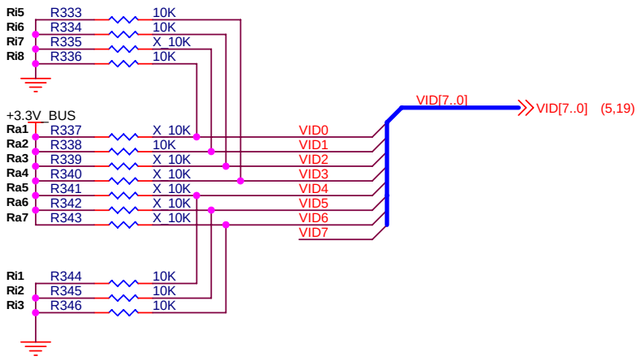
Decoupling

+MVDDQ: C264 100nF, C265 100nF, C266 100nF, C267 100nF, C268 100nF, C269 100nF, C270 100nF, C271 100nF, C272 100nF, C273 100nF, C274 100nF, C275 100nF, C276 100nF, C277 100nF, C278 100nF, C279 100nF, C280 100nF, C281 100nF, C282 100nF, C283 100nF
+MVDDC: C284 100nF, C285 100nF, C286 100nF, C287 100nF, C288 100nF, C289 100nF, C290 100nF, C291 100nF, C292 100nF, C293 100nF, C294 100nF, C295 100nF, C296 100nF, C297 100nF, C298 100nF, C299 100nF, C300 100nF, C301 100nF, C302 100nF, C303 100nF

MS-8956 ATI R360 9800XT

Size	Document Number	Rev
B	BGA 4MX32 DDR C AND D	00A
Date: Thursday, December 04, 2003	Sheet 14 of 20	

STRAPPING



AGPFBSKEW -- VID(1:0)

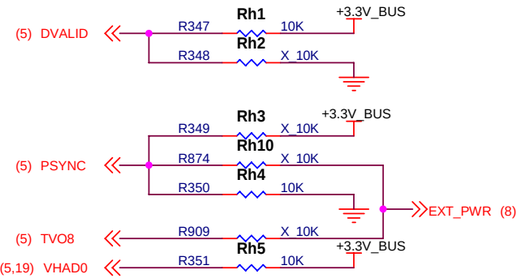
Ra2	Ra1	Ri7	Ri8	
DNI	DNI	10K	10K	refclk slightly earlier than feedback (00)
DNI	10K	10K	DNI	refclk 1 tap earlier than feedback (01)
10K	DNI	DNI	10K	refclk 1 tap later than feedback DEFAULT (10)
10K	10K	DNI	DNI	refclk 2 taps earlier than feedback (11)

X0CLK_SKEW --VID(3:2)

Ra4	Ra3	Ri5	Ri6	
DNI	DNI	10K	10K	x0clk to agpclk 0 tap delay DEFAULT
DNI	10K	10K	DNI	x0clk to agpclk 1 tap delay
10K	DNI	DNI	10K	x0clk to agpclk 2 taps delay
10K	10K	DNI	DNI	x0clk to agpclk 3 taps delay

BUSCFG -- VID(6:4)

BUSTYPE_2 VID6		BUSTYPE_1 VID5		BUSTYPE_0 VID4		
Ra7	Ri3	Ra6	Ri2	Ra5	Ri1	AGP8X_DET = 0 (both GC and MB 8x capable)
						DESCRIPTION
DNI	10K	DNI	10K	DNI	10K	AGP 8X, 0.8V signaling PLL CLK, IDSEL = AD16
DNI	10K	DNI	10K	10K	DNI	AGP 8X, 0.8V signaling PLL CLK, IDSEL = AD17
DNI	10K	10K	DNI	DNI	10K	AGP 4X, 0.8V signaling PLL CLK, IDSEL = AD16
DNI	10K	10K	DNI	10K	DNI	AGP 4X, 0.8V signaling PLL CLK, IDSEL = AD17
						AGP8X_DET = 1 (either GC or MB not 8x capable)
DNI	10K	DNI	10K	DNI	10K	AGP 4X, PLL CLK, IDSEL = AD16
DNI	10K	DNI	10K	10K	DNI	AGP 4X, PLL CLK, IDSEL = AD17
DNI	10K	10K	DNI	DNI	10K	AGP 1X/2X, PLL CLK, IDSEL = AD16
DNI	10K	10K	DNI	10K	DNI	AGP 1X/2X, PLL CLK, IDSEL = AD17
10K	DNI	DNI	10K	DNI	10K	PCI 66MHz, PLL CLK
10K	DNI	DNI	10K	10K	DNI	PCI 33MHz, 3.3V, REF CLK
10K	DNI	10K	DNI	DNI	10K	AGP 1X, REF CLK, IDSEL = AD16
10K	DNI	10K	DNI	10K	DNI	AGP 1X, REF CLK, IDSEL = AD17

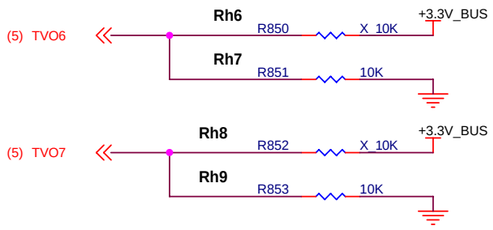


INSTALL	DEVICE ID
Rh1	NORMAL ID (default) Install it all the time when it is normal device ID
Rh2	Use workstation DEVICE_ID when WSEN = 1

INSTALL	DNI	ID_DISABLE
Rh4	Rh10	Normal operation
Rh3	Rh10	CHIP SHUTS DOWN
Rh10	Rh3 Rh4	Circuitry for external power detection. (DEFAULT)

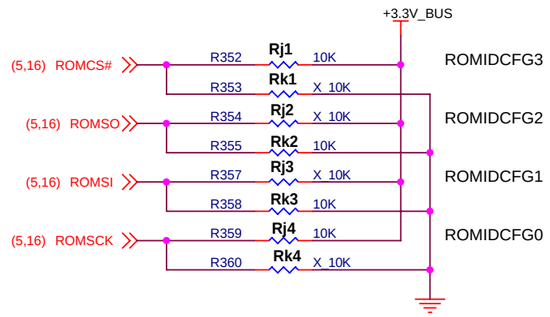
INSTALL	VIP DEVICE
Rh5	NO SLAVE VIP (DEFAULT) Install it when internal pull-up doesn't work
	SLAVE VIP --- VIP device will drive low when VIP is attached.

MEMORY TYPE STRAPS



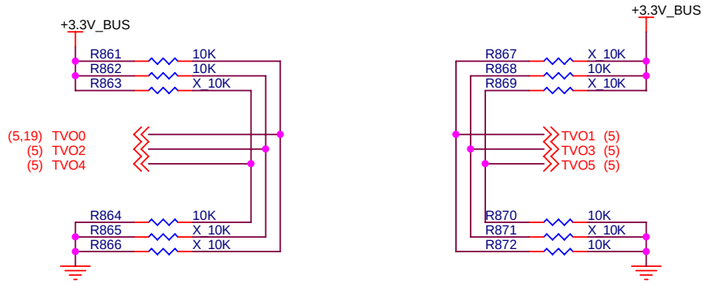
MEMORY TYPE STRAPS

	TVO7	TVO6
SAM	0	0
INF	1	0
HYN	0	1
TBD	1	1



Rj1	Rk1	Rj2	Rk2	Rj3	Rk3	Rj4	Rk4	ROMIDCFG[3:0]
DNI	10K	DNI	10K	DNI	10K	DNI	10K	No ROM, CHG ID = 00
DNI	10K	DNI	10K	10K	DNI	DNI	10K	No ROM, CHG ID = 01
DNI	10K	10K	DNI	DNI	10K	DNI	10K	No ROM, CHG ID = 10
DNI	10K	10K	DNI	10K	DNI	DNI	10K	No ROM, CHG ID = 11
10K	DNI	DNI	10K	DNI	10K	DNI	10K	Parallel ROM on TVO (default)
10K	DNI	DNI	10K	DNI	10K	10K	DNI	Serial AT25F1024, ID's from ROM
10K	DNI	DNI	10K	10K	DNI	DNI	10K	Serial AT45DB011, ID's from ROM
10K	DNI	DNI	10K	10K	DNI	10K	DNI	Serial ST M25P10, ID's from ROM
10K	DNI	10K	DNI	DNI	10K	DNI	10K	Serial ST M25P05, ID's from ROM
10K	DNI	10K	DNI	DNI	10K	10K	DNI	Serial SST45LF010, ID's from ROM
10K	DNI	10K	DNI	10K	DNI	DNI	10K	Parallel ROM on DVO
10K	DNI	10K	DNI	10K	DNI	10K	DNI	Serial ISSI NX25F011B, ID's from ROM

TVO Straps



TVO1	
0	PAL
1	NTSC

TVO2	
0	YPrPb
1	SVHS/CVBS

TVO4	TMDS
0	NO
1	YES

TVO0	TVO3	DAC2
0	0	OFF
0	1	TV-OUT
1	0	CRT
1	1	BOTH

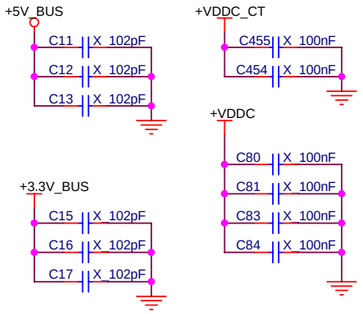
TVO5	
0	NO VIDEO CAPATURE
1	RAGE THEATER 1 OR 2

MS-8956 ATI R360 9800XT

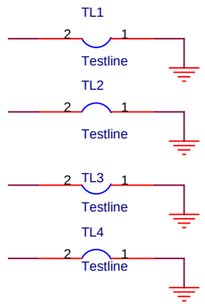
Size	Document Number	Rev
B	STRAPPING	00A

Date: Thursday, December 04, 2003 Sheet 15 of 20

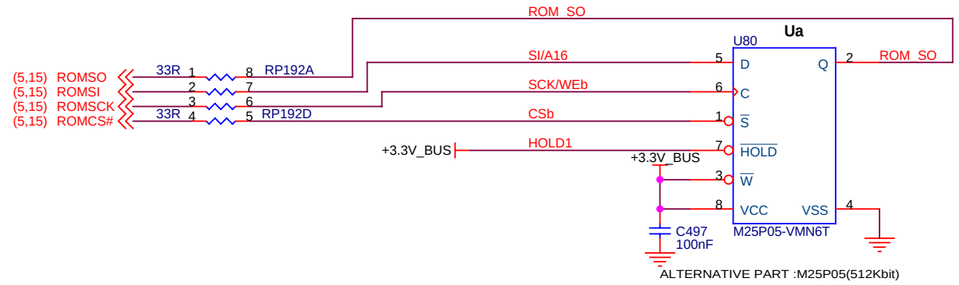
EMI



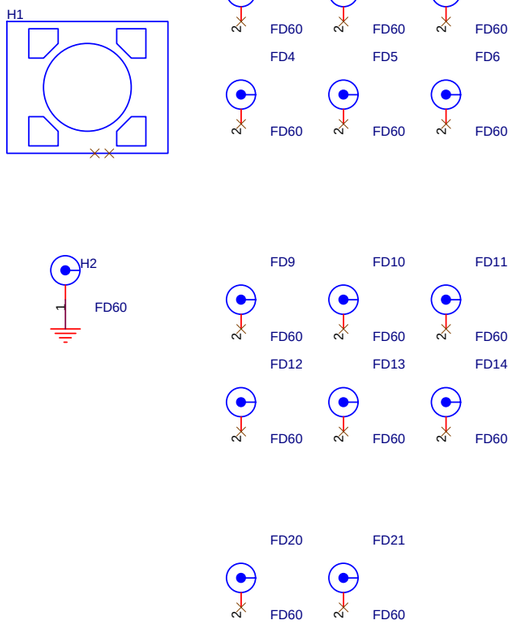
Impendence Test Line



SERIAL EEPROM 512K/1M



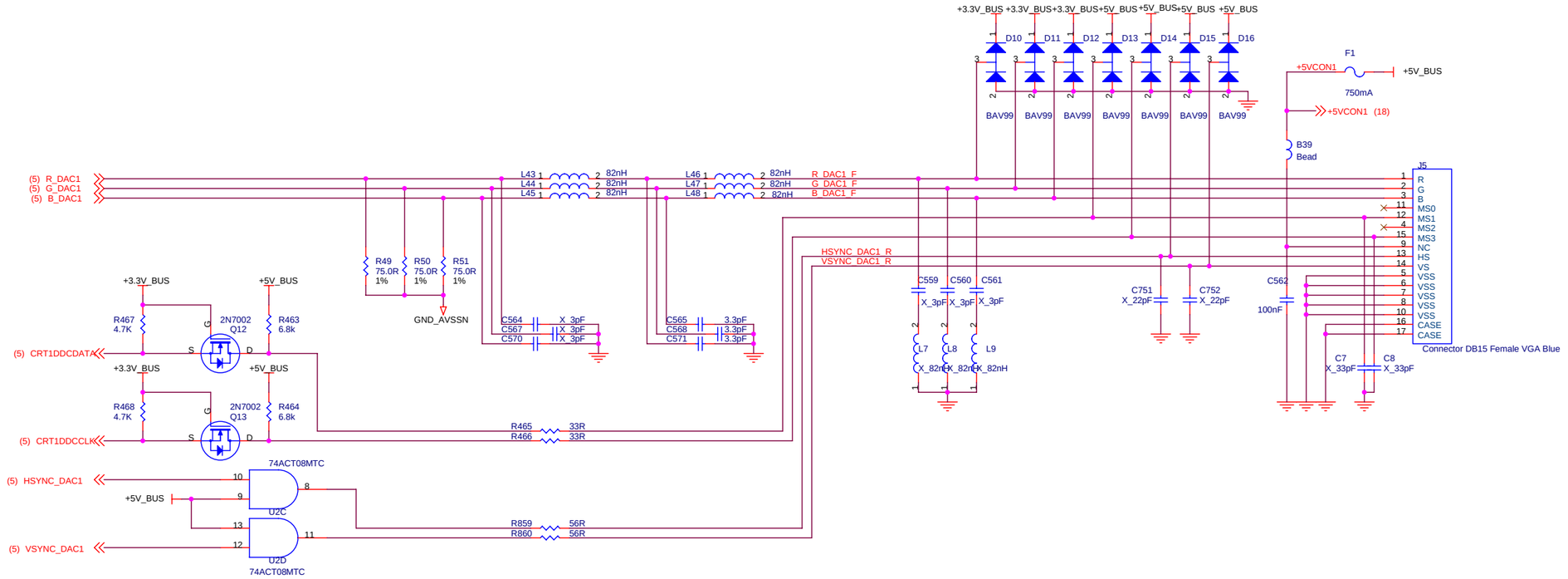
ALTERNATIVE PART :M25P05(512Kbit)



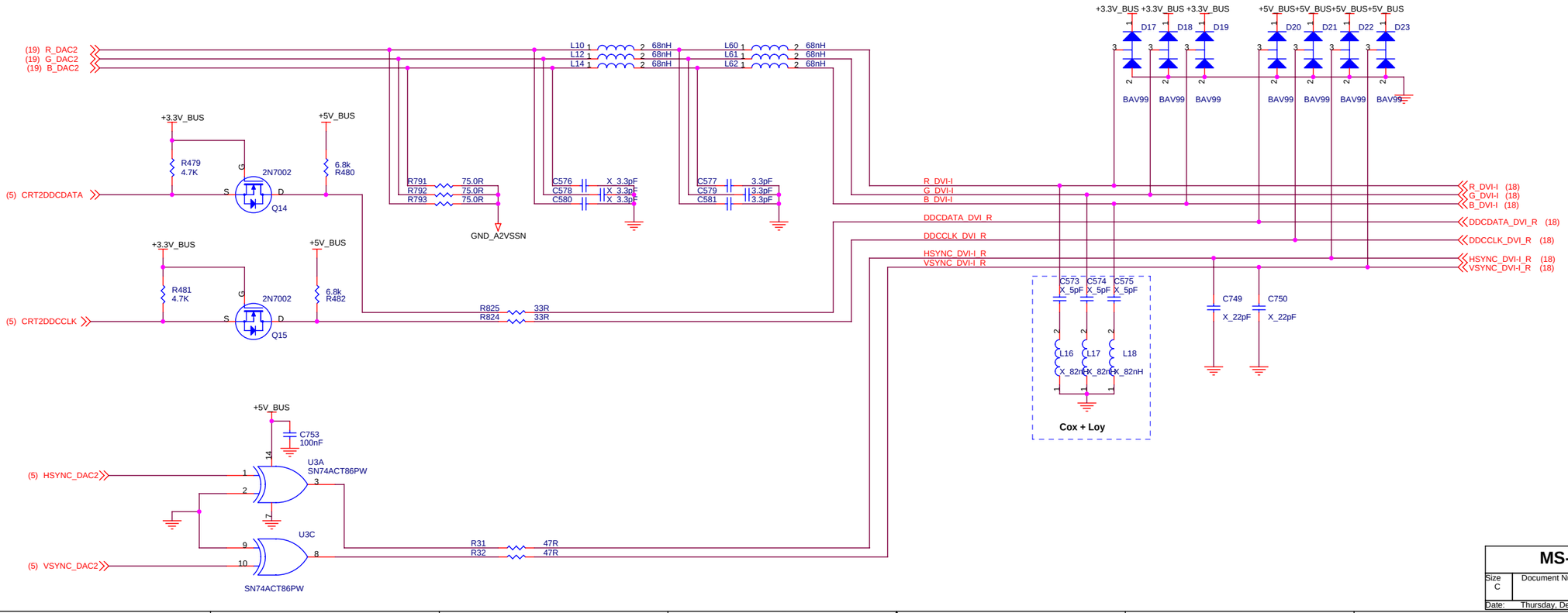
MS-8956 ATI R360 9800XT

Size	Document Number	Rev
B	FAN / BIOS	00A
Date: Thursday, December 04, 2003	Sheet 16 of 20	

PRIMARY CRT INTERFACE

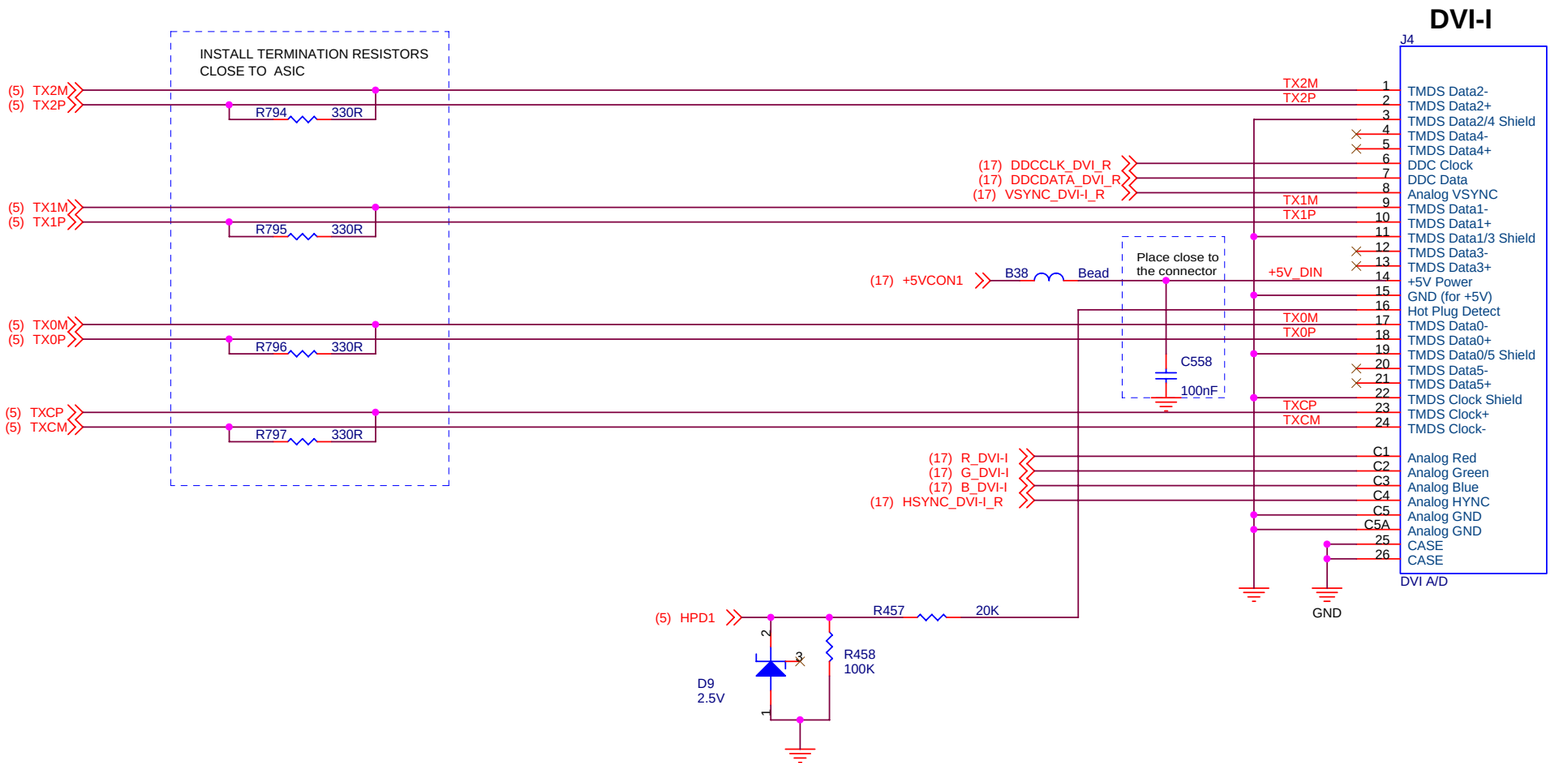


SECONDARY CRT INTERFACE



MS-8956 ATI R360 9800XT		
Size C	Document Number **CRT DISPLAY**	Rev 00A
Date: Thursday, December 04, 2003	Sheet 17 of 20	

PRIMARY DVI-I CONNECTOR (DVI-I)



MS-8956 ATI R360 9800XT		
Size B	Document Number **DVI-I DISPLAY**	Rev 00A
Date: Thursday, December 04, 2003	Sheet 18 of 20	

ATi Theater Decoder

PLACE CLOSE TO RAGE THEATRE

U12

RAGE THEATER

PLACE AS CLOSE TO THE RAGE THEATRE AS POSSIBLE.

VIA TV Encoder

U10

VT1623M

VIVO Connector

JA

CD-D1x4-BK-SBTJ

Regulator for RVDD

REG7 3.3V_ATI/2.5V_VIA

ADJ

	RVDD
ATi Theater	3.3V
VIA VT1623M	2.5V

VIDEO IN

DEMUX

TV-OUT from VIA 1623M : install R96, R97, R98 ; remove U96
TV-OUT from ATi R360 : remove R96, R97, R98 ; install U96

Uv1

U96

IDT3257

SCART

JSCART

COM-D9-GN

TV OUT

TV-OUT from VIA 1623M : install R90, R92, R94 ; remove R91, R93, R95
TV-OUT from ATi R360 : remove R90, R92, R94 ; install R91, R93, R95

MS-8956 ATI R360 9800XT

Size	Document Number	Rev
Custom	ATi Decoder & VIA Encoder	00A
Date: Thursday, December 04, 2003	Sheet 19 of 20	

TEMPERATURE SENSE AND SPEED CONTROLLED FAN

+12V_BUS
B59
Bead
+12V_BUS
R11
0R
MJU1
JUI1
Header_1X3
C1134
0.1uF
R1573
0R
DNI
+3.3V_BUS
C1516
10uF
C1517
0.1uF
C1518
100pF
R1609
10K
TEMPERATURE SENSE DIODE.
MUST BE PLACED AT THE HOT
SPOT.
R1610
10K
U106
SMBCLK
SMBDAT
ALERT
GND
VDD
D+
D-
PWM
LM63CIMAX
D+
D-
C1519
2.2nF
Q214
CMPT3904
(5,19) SCL
(5,19) SDA
R1620
R1621
100R
SCL_R
SDA_R
TACH
C1524
56pF
C1525
56pF
+3.3V_BUS
U110
NC7S04M5
C1576
100nF
(5) ThermINT
+3.3V_BUS
R1681
1K
R1682
DNI
0R
Q213
MMBT2222ALT1
MMBT2222ALT1
Q215
C1577
1uF
PWM
R1683
10R
R1684
0R
TACH
C1520
DNI
10nF
+12V_BUS
R1611
0R
DNI
R1631
10K
+3.3V_BUS
R1613
10K
DNI
R1614
10K
DNI
U107 DNI
NC#3
NC#4
PWM
GND
D-
ADD
SCL
THERM
FAULT
TACH
INT
NC
NC#11
D+
VCC
SDA
ADM1030ARQ
PWM
D-
SCL_R
DNI R1615 0R
DNI R1616 0R
TACH
R1612
0R
DNI
D+
SDA_R
+3.3V_BUS
C1578
10uF
DNI
C1579
0.1uF
DNI
C1580
100pF
DNI
R1628
DNI
0R
DNI
R1629
10K

MS-8956 ATI R360 9800XT		
Size B	Document Number **THERMAL CONTROL**	Rev 00A
Date: Thursday, December 04, 2003	Sheet 20 of 20	