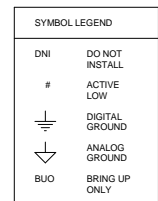
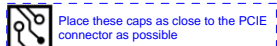
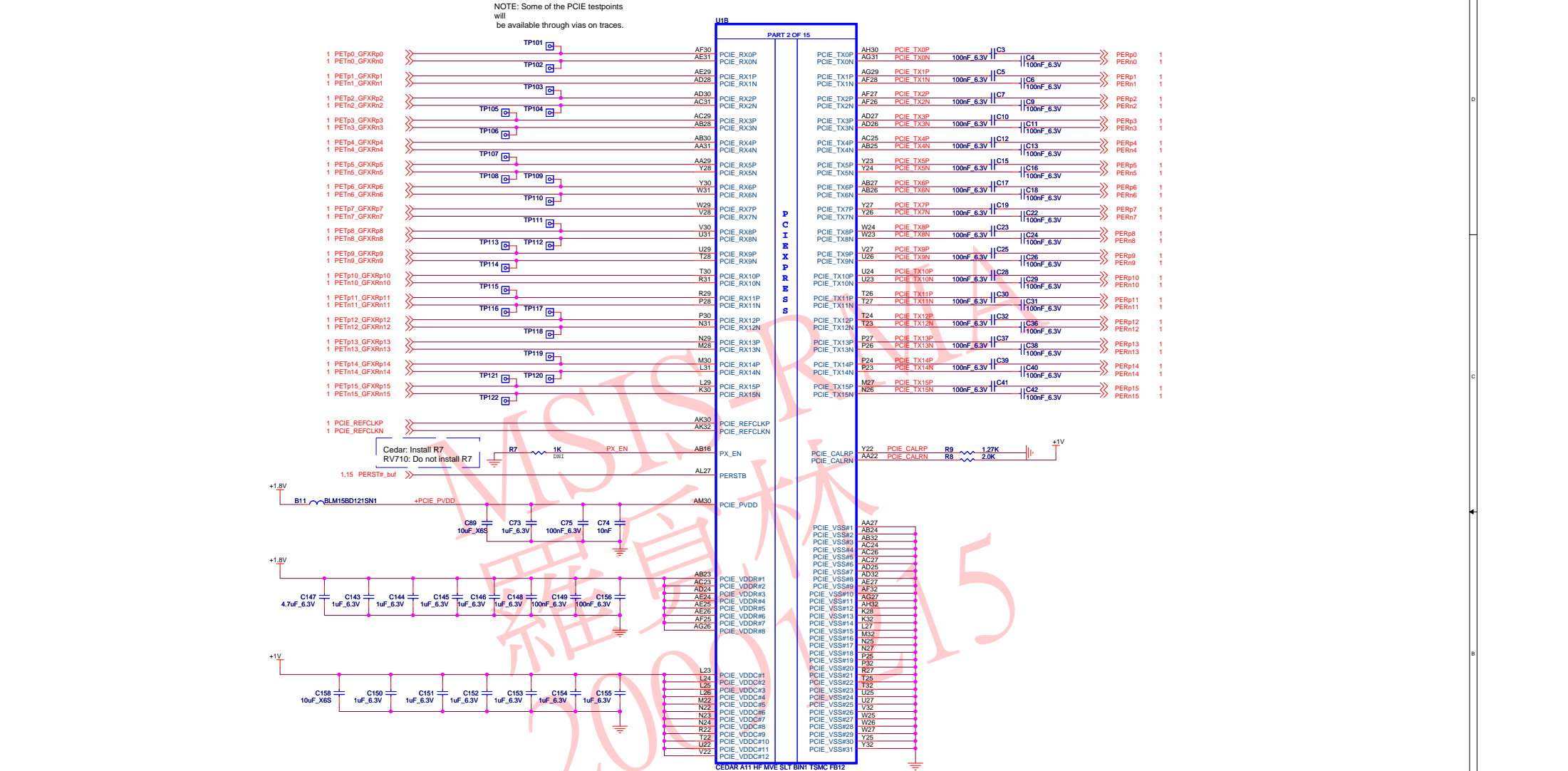


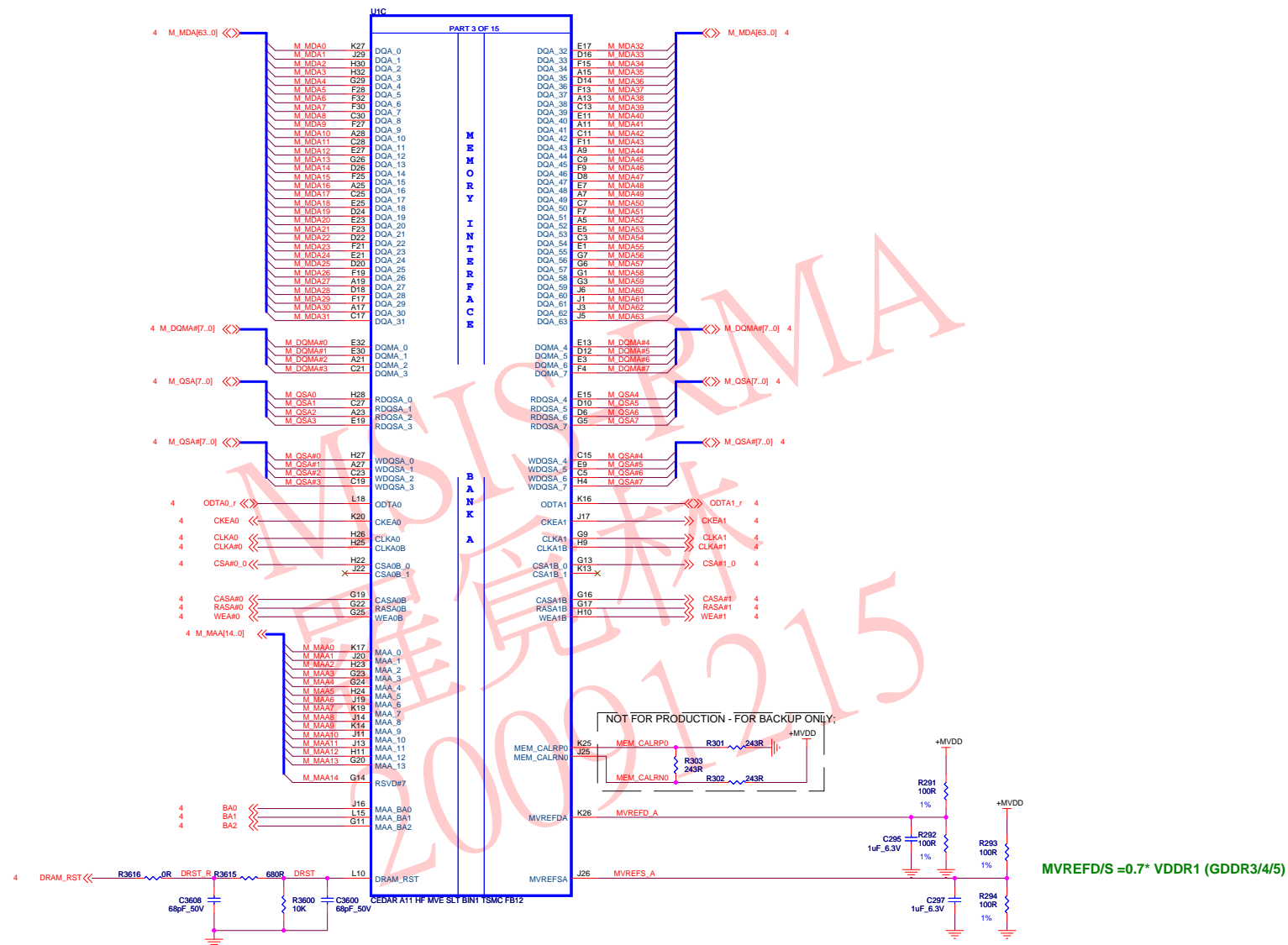
CEDAR BASS / PERCH



CEDAR PCIe Interface



CEDAR MEM Interface Ch A&B



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Date: Friday, November 06, 2009

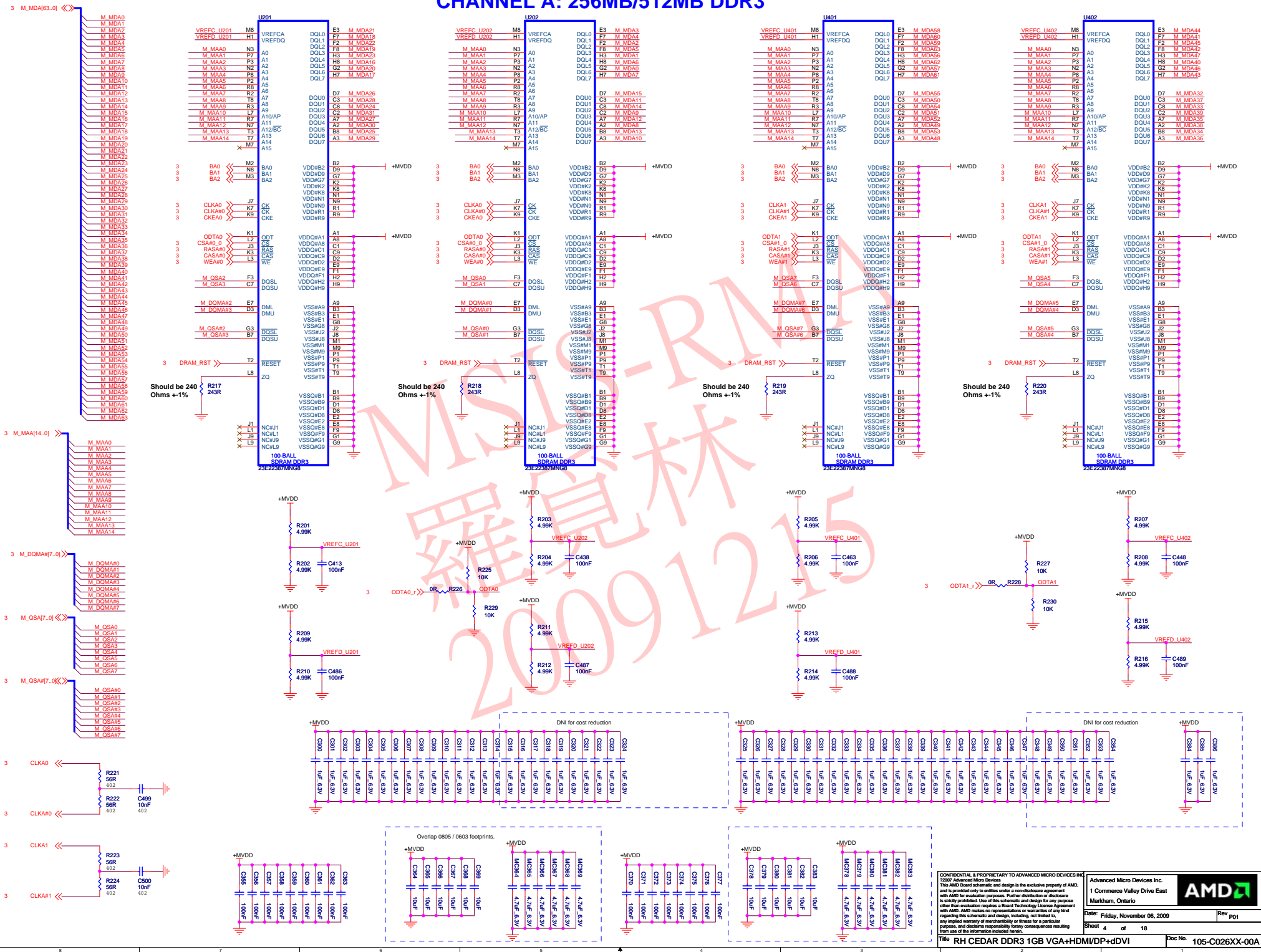
Sheet 3 of 18

Rev P01

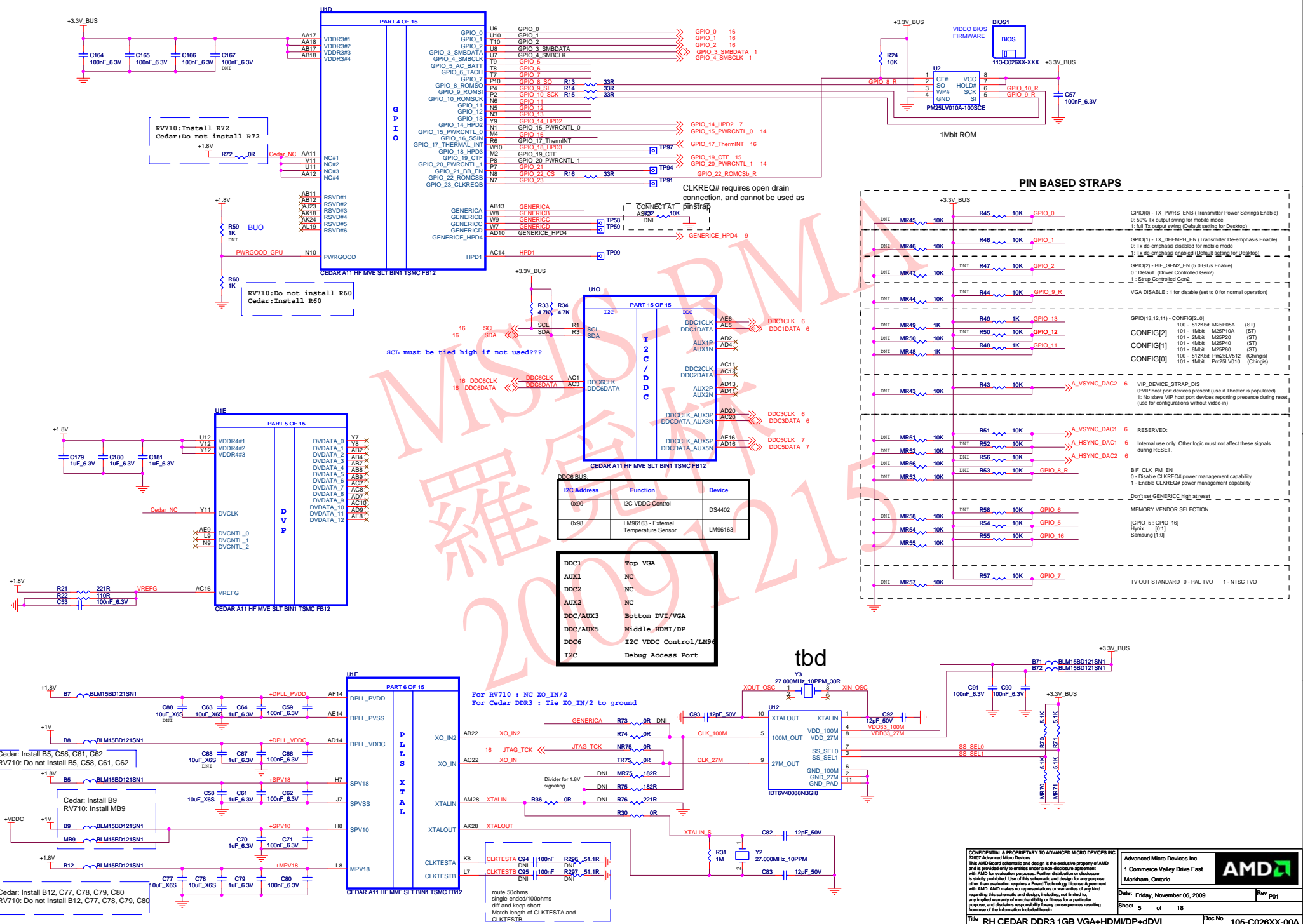
Title	RH CEDAR DDR3 1GB VGA+HDMI/DP+dDVI
-------	------------------------------------

Doc No. 105-C026XY-00A

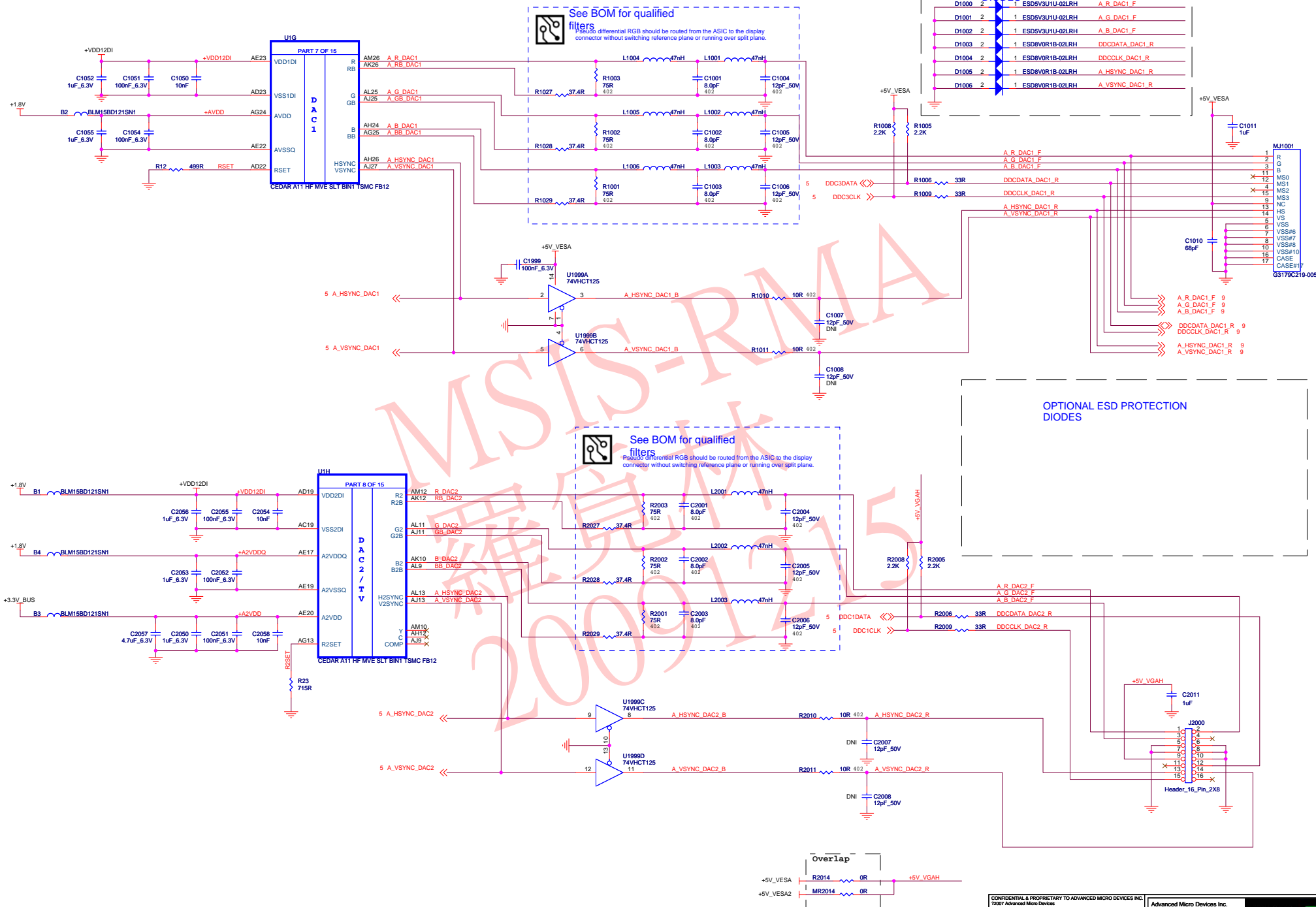
CHANNEL A: 256MB/512MB DDR3



CEDAR GPIOs Strap CF XTAL OSC




CEDAR DAC1 and DAC2

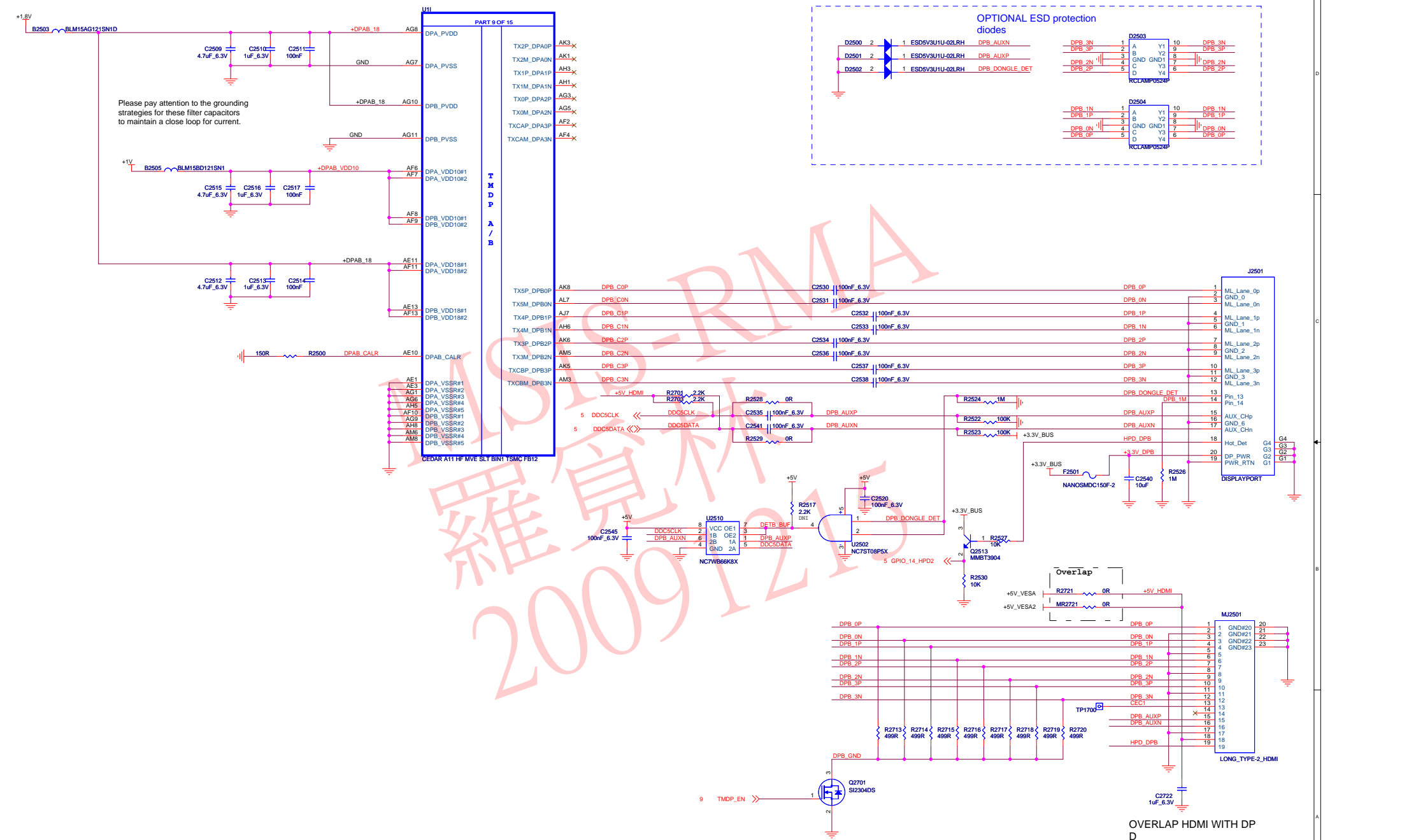


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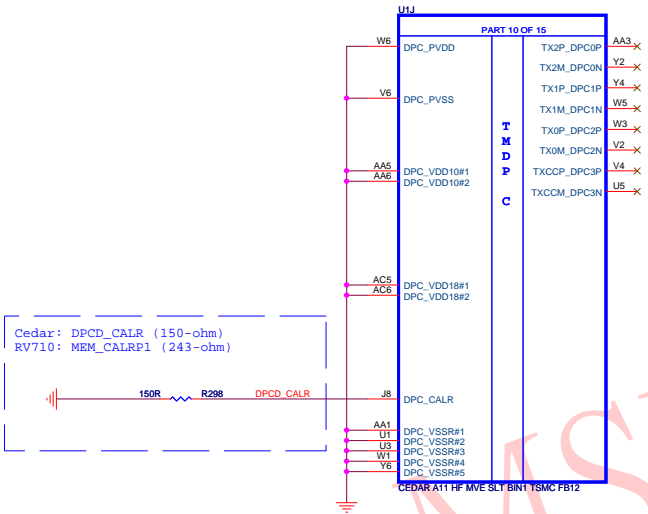
Advanced Micro Devices Inc. 1 Commerce Valley Drive East Markham, Ontario			
Date: Friday, November 06, 2009		Rev P01	
Sheet 6	of 18		

CEDAR TMDP A&B DP/HDMI OVERLAP

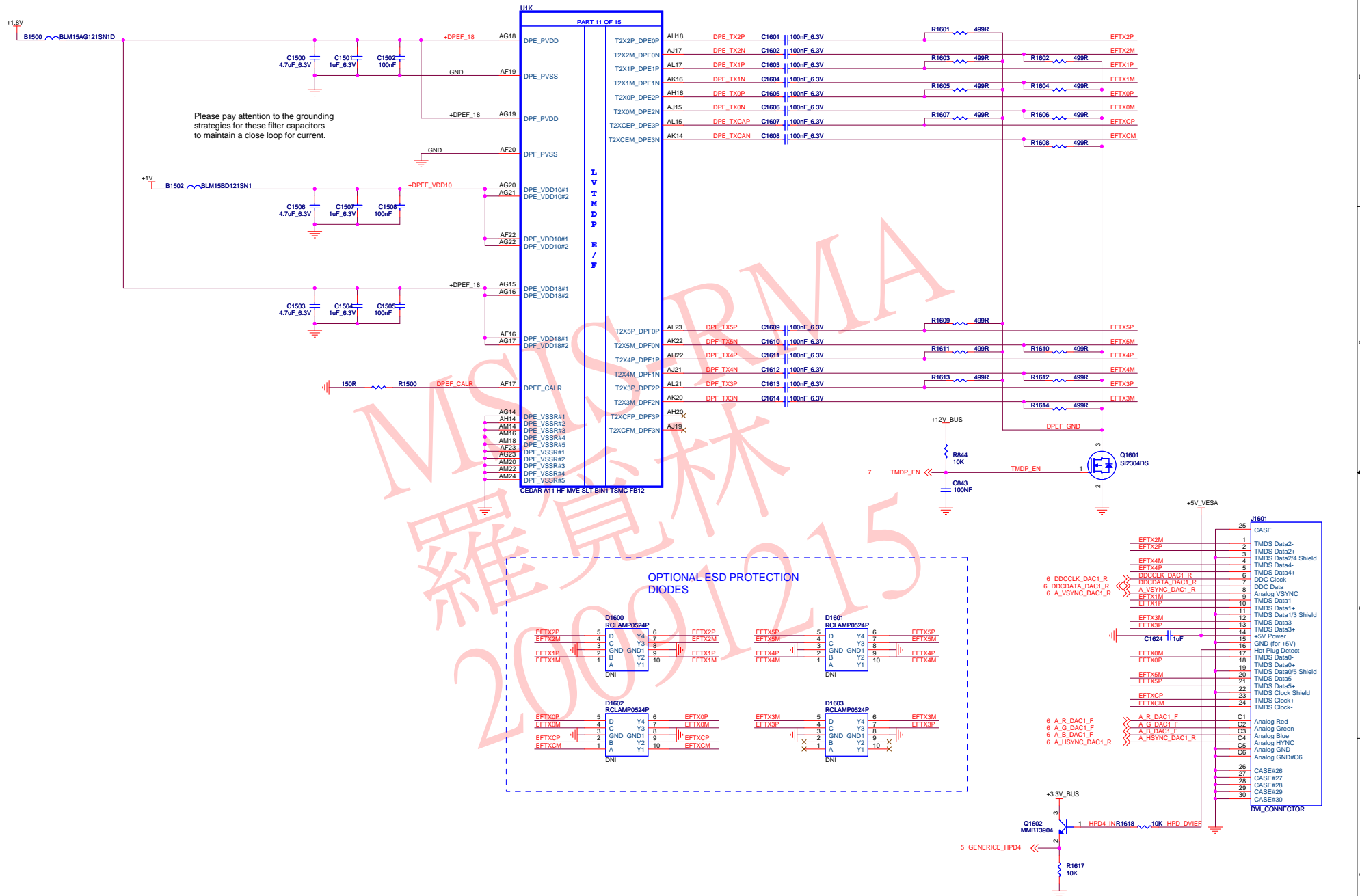


OVERLAP HDMI WITH DP
D

CEDAR Display Port C (Unused)



CEDAR LVTMDP E&F dDVI-I



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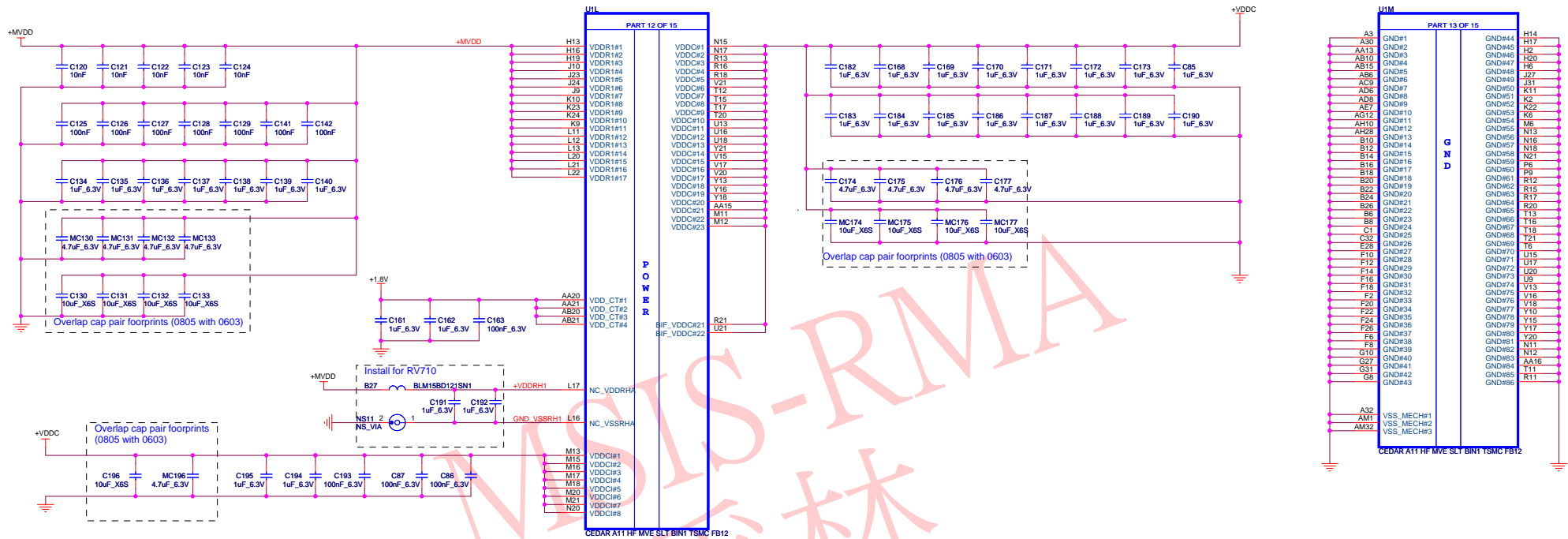
Sheet 9 of 18

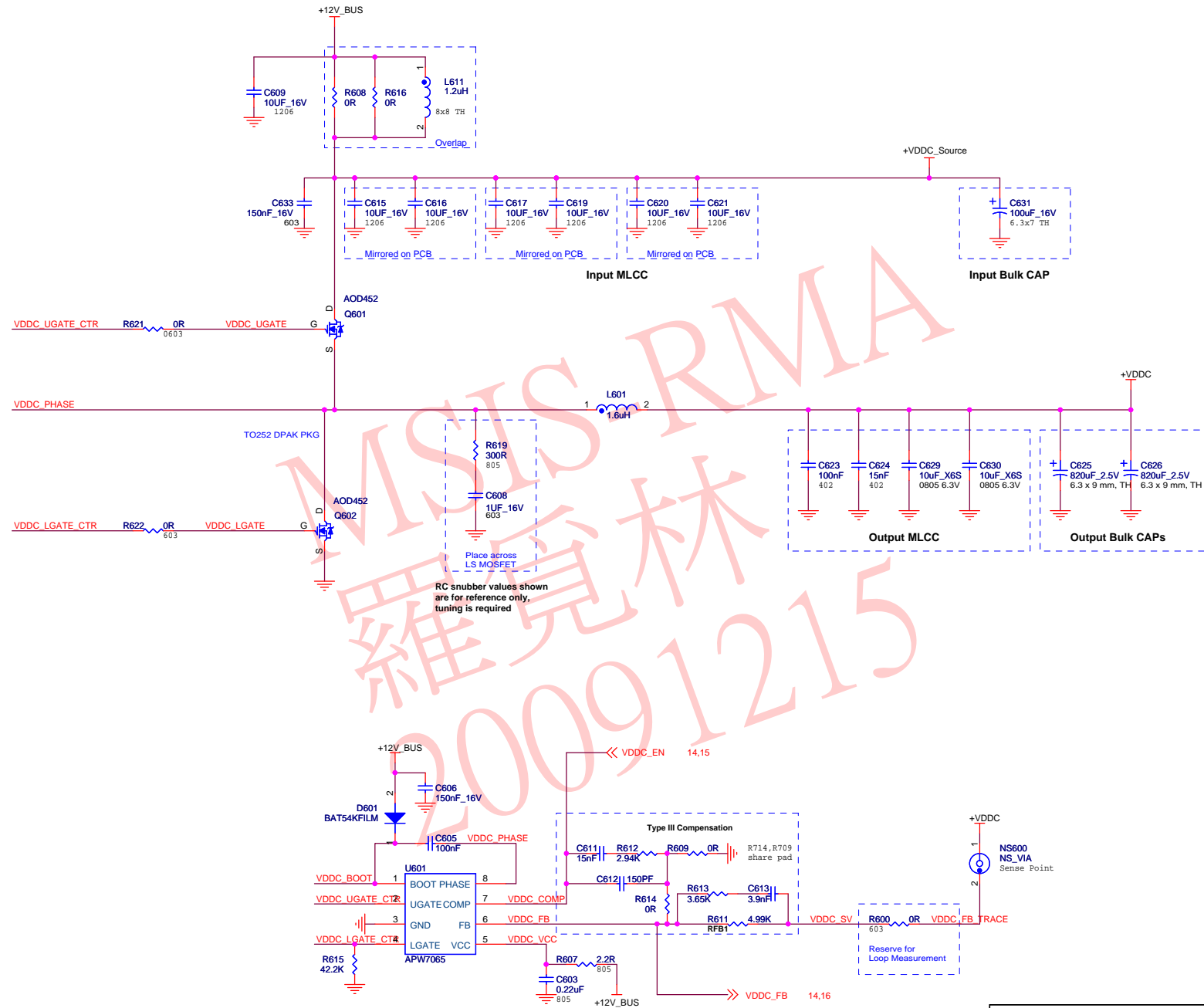
Rev P01

Title	RH CEDAR DDR3 1GB VGA+HDMI/DP+dDVI
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Doc No. 105-C026XX-00A

CEDAR Power & GND



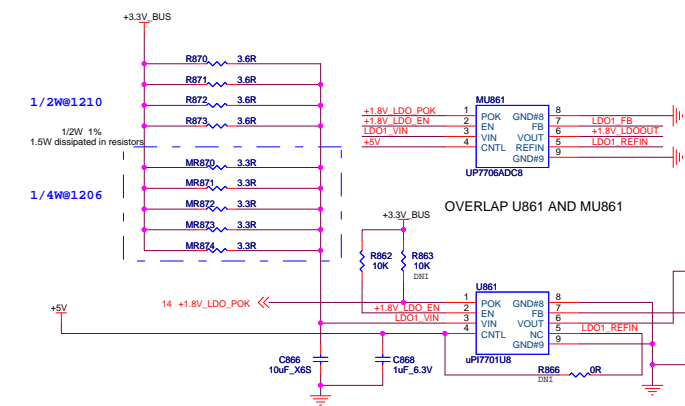


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Date: Friday, November 06, 2009		
Sheet 11 of 18		Rev P01
DMI/DP+dDVI		Doc No. 105-C026XX-00A

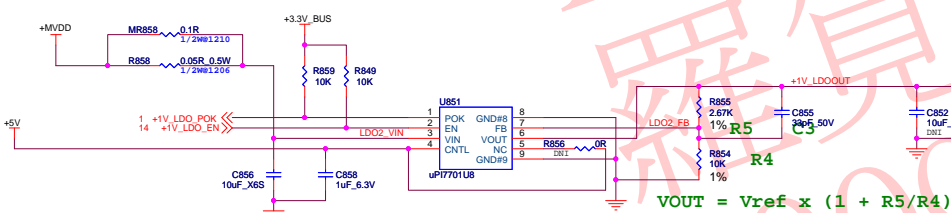
Linear Regulators

LDO #1: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



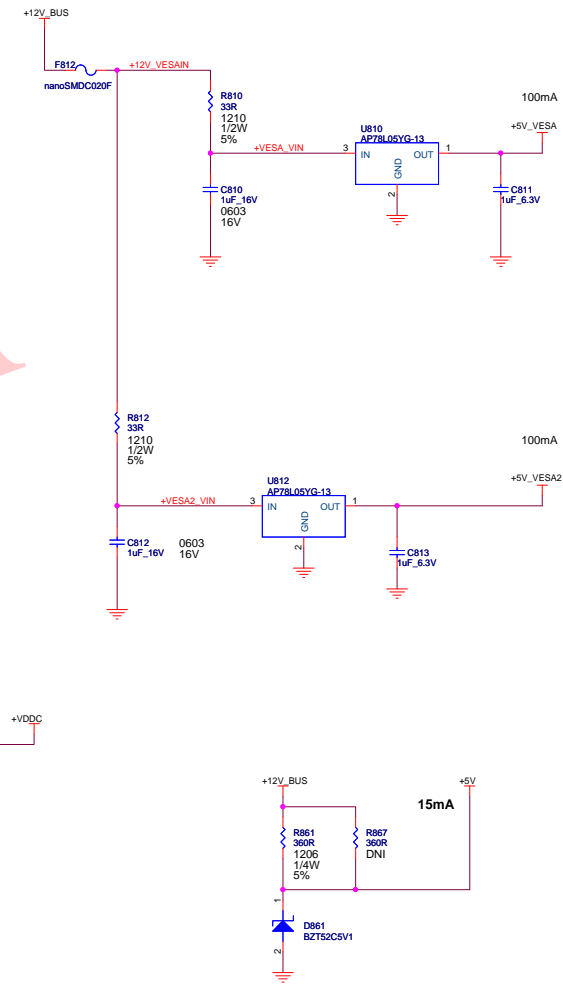
1.8V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1330mA

LDO #2: Vin = +1.32V to 1.84VMAX Vout = +1.01V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



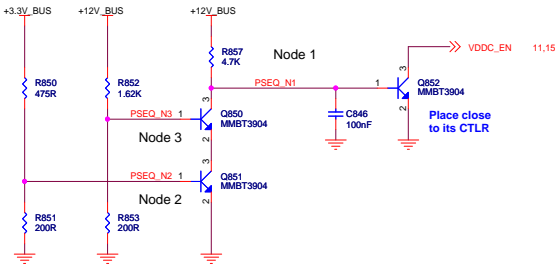
1.0V WORST-CASE REQUIREMENT	
Display Config	Est. Current
DVI+HDMI+DP	1560mA

Regulators for +5V, +5V_VESA and +5V_VESA2

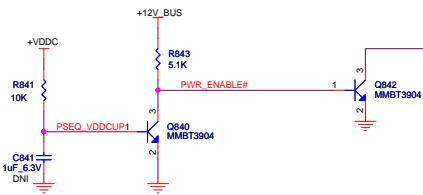


Power Management - Power Gating and Dynamic Voltage Control

12V_BUS & 3V3_BUS POWER SEQUENCING



POWER SEQUENCING CIRCUIT



Install R839 to gate 1V LDO with 1.8V LDO.

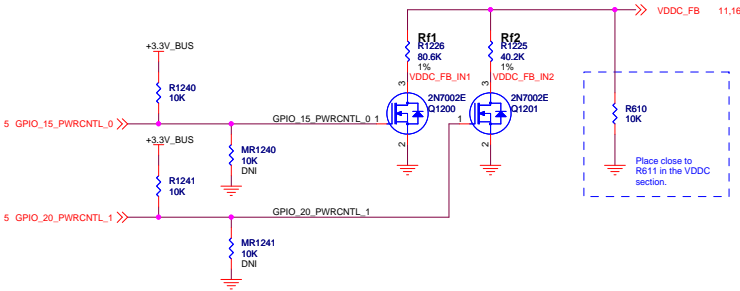


MVDD Low Side Divider

- Hi-Side Divider RFB1 is Fixed to 10K
- $V_o = V_{ref} * (1 + RFB1 / RFB2)$
- $V_{ref} = 0.8V$



VDDC Low Side Divider



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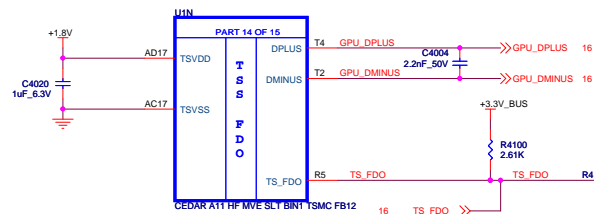
Rev P01

Sheet 14 of 18

Doc No. 105-C026XX-00A

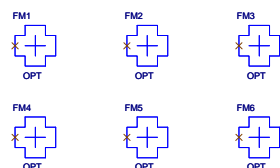
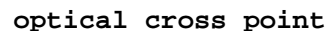
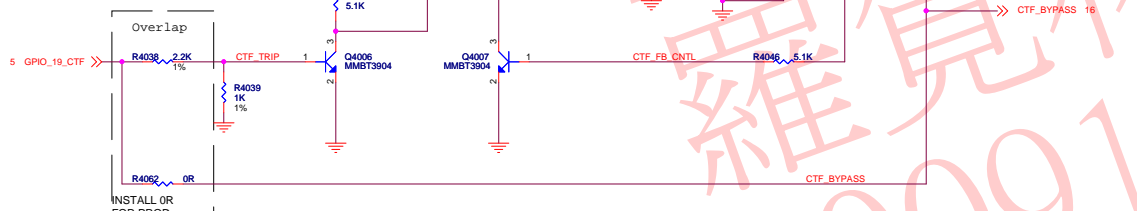
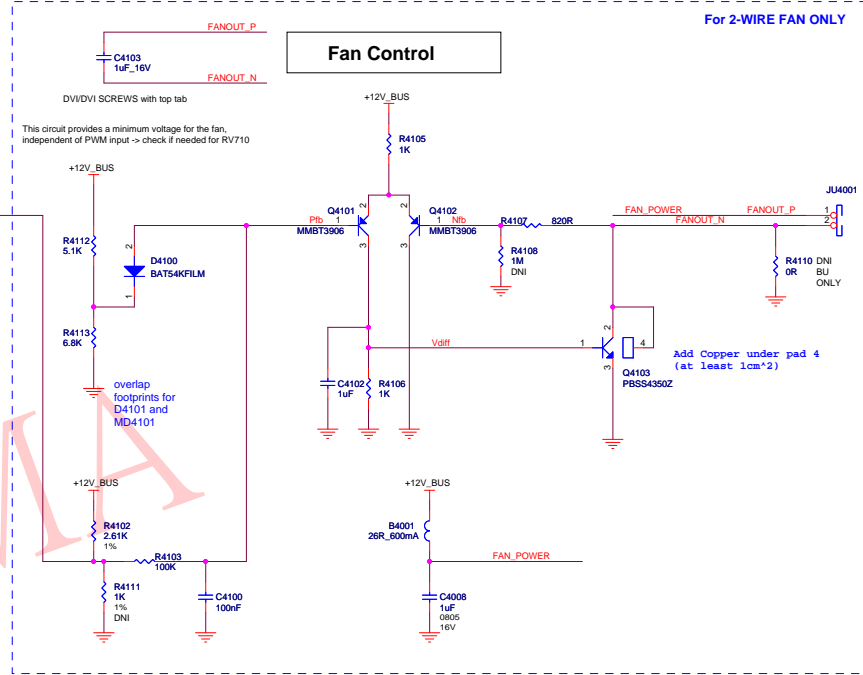
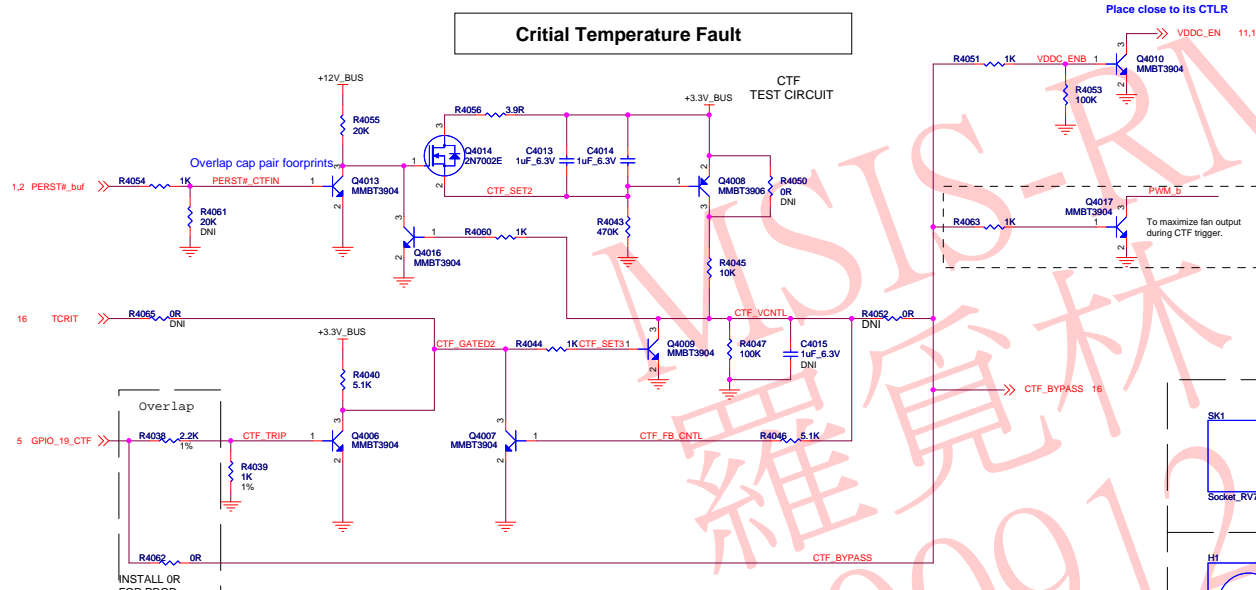
TRB RH CEDAR DDR3 1GB VGA+HDMI/DP+JdVI

Mechanical and Thermal Management



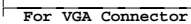
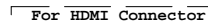
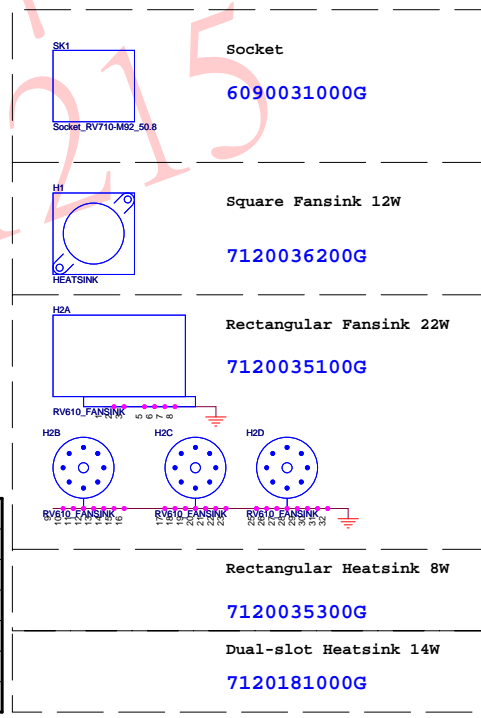
Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.

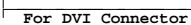


TOP & BOT layer set each 3 points

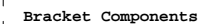
SKU		P/N	CONFIGURATION	Form Factor
	PERCH	8020051300G	DVI + DP + VGA	PH / SS
BASS		8020051400G	DVI +HDMI+ VGA	PH / SS
	PERCH	8020051600G	DVI + DP	LP / SS
BASS		80200516A0G	DVI +HDMI	LP / SS
	PERCH	8020051700G	DVI + DP + VGA	PH / DS
BASS		80200517A0G	DVI +HDMI+ VGA	PH / DS



7020000800G



7020000800G



7020005200G



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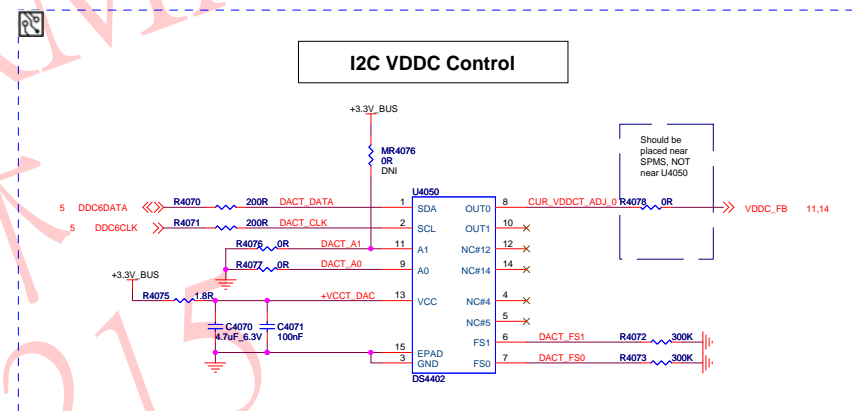
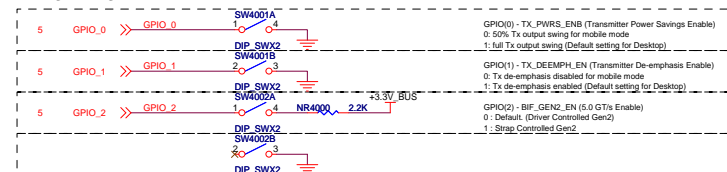
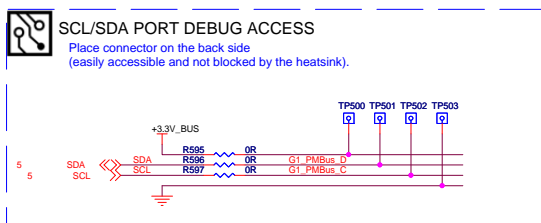
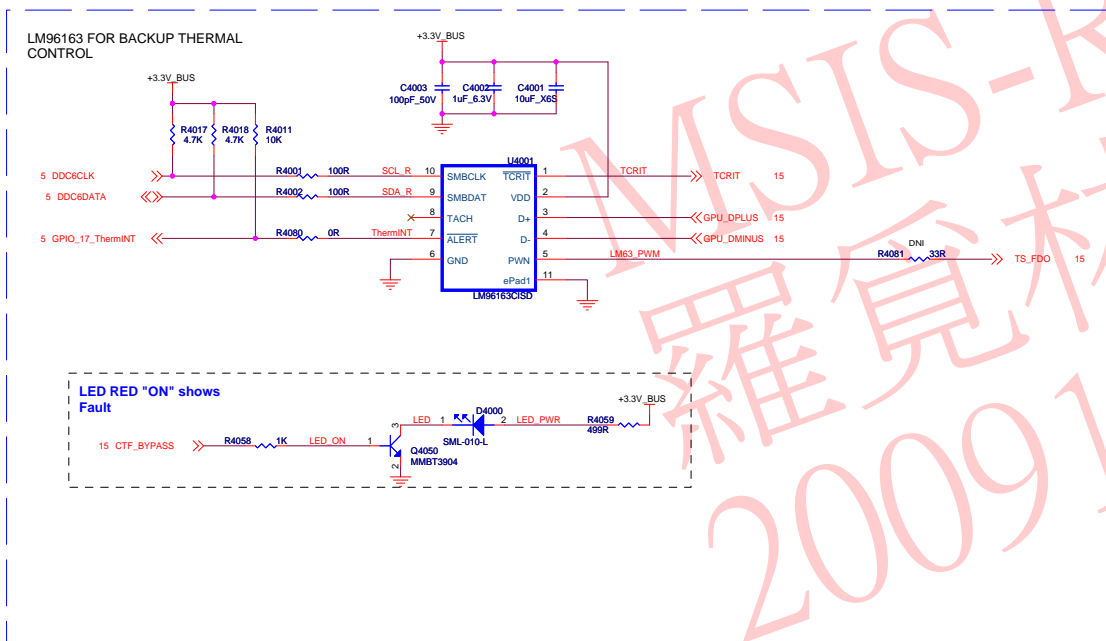
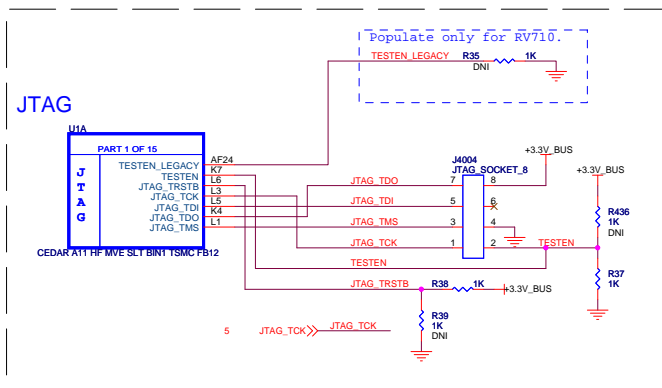


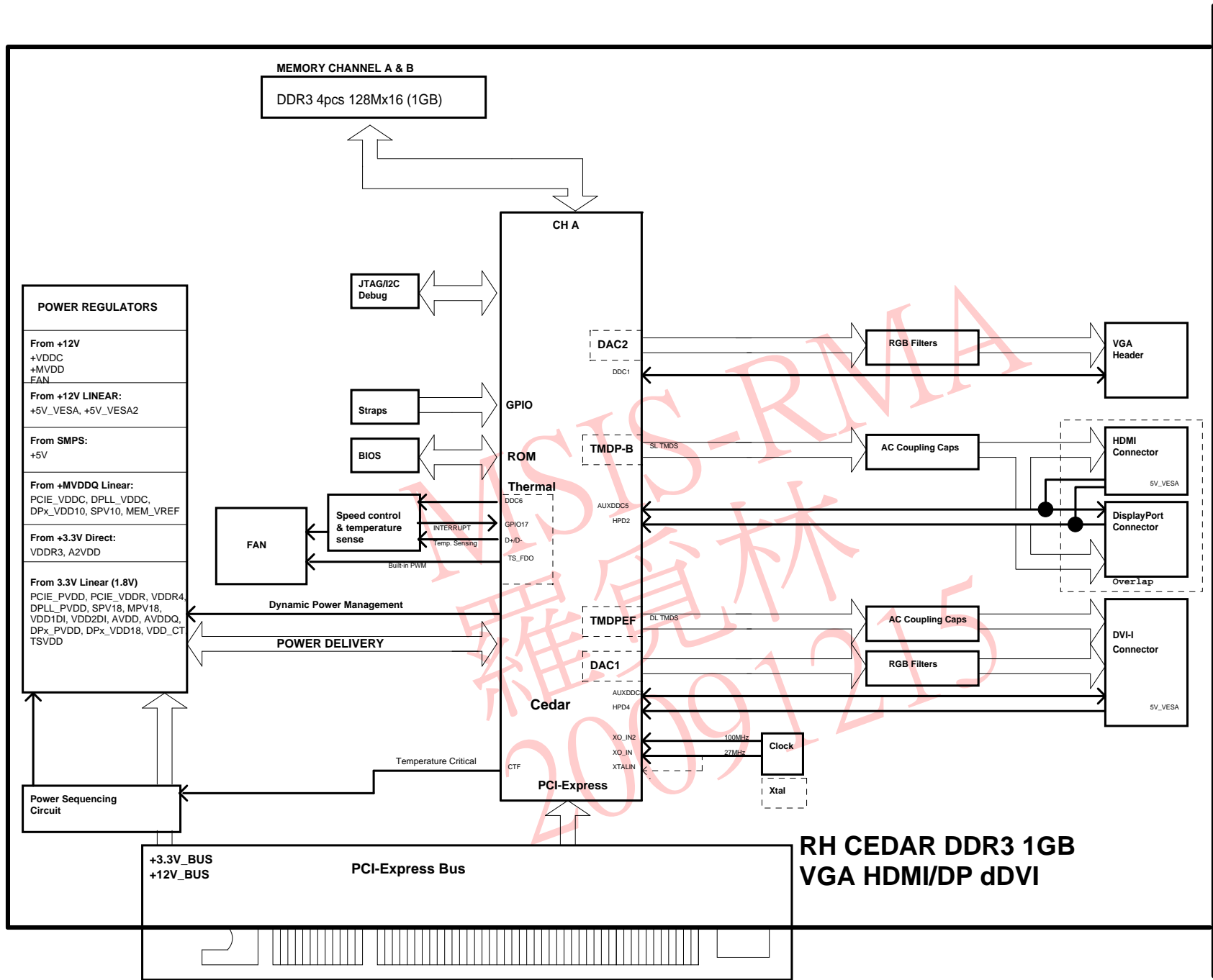
Rev	P01
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Title RH CEDAR DDR3 1GB VGA+HDMI/DP+dDVI

Doc No. 105-C026XX-00A

(19) Debug Circuits





<div>AMD</div>			Title		Schematic No.		Date:				
			RH CEDAR DDR3 1GB VGA+HDMI/DP+dDVI		105-C026XX-00		Friday, November 06, 2009				
			REVISION HISTORY					NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.		Rev P03	
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION								
00	00A	2009/03/23									
01	00B	2009/07/3									
02	00C	2009/08/12	Initial Cedar schematic								
03	00D	2009/09/24	Change DDC line configuration								
V212	5.0	2009/10/30	Page 11 : changed L601 & L611 & C631 & C626 & change R621 footprint from 0402 to 0603 Page 12 : changed L701 & C730 & C726 Add L702 & change R721 footprint from 0402 to 0603 Page 15 : add optical cross point								
V212	5.0	2009/11/3	Page 15 : add Q4017 & R4063 to maximize fan output during CTF trigger. remove MT201								

MSIS-RMA
羅覓林
20091215