

**A 256MB MEMORY APERTURE SIZE CAN BE DEFINED USING A SEPARATE ROM OR STRAPPING**

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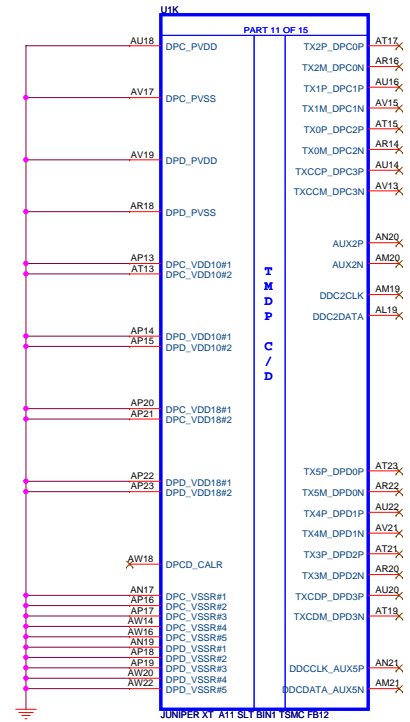
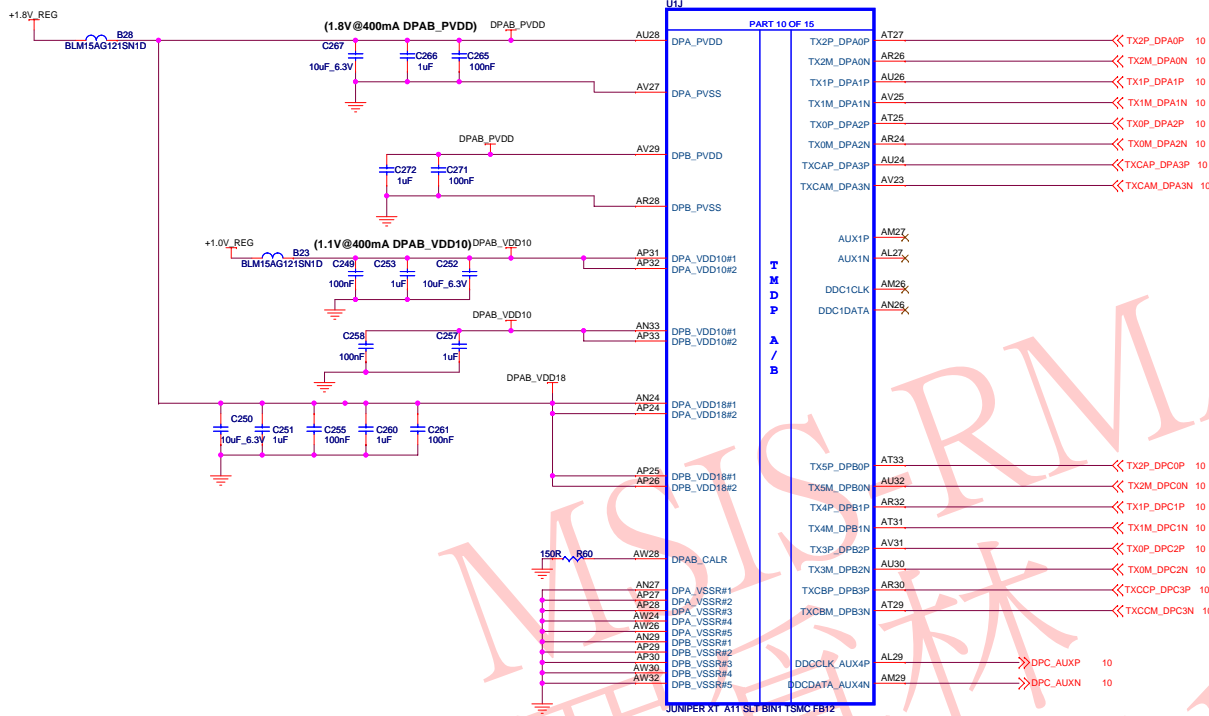
**SERIAL EEPROM 512K/1M**

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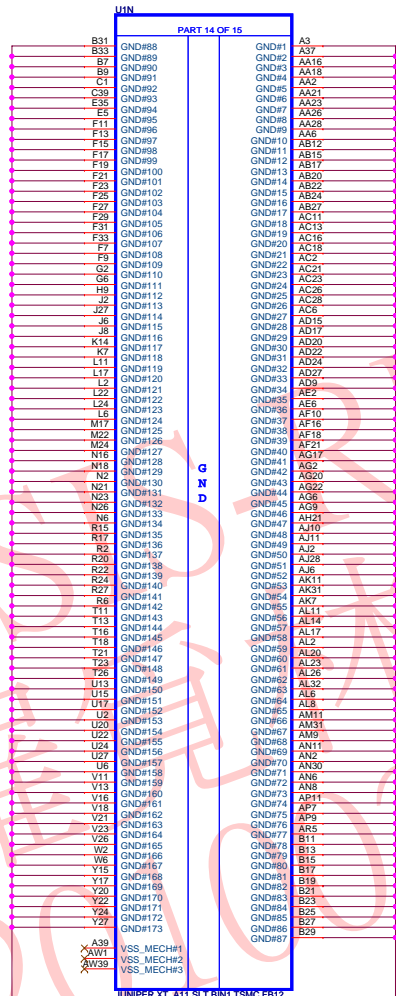
Date: Monday, December 07, 2009  
Sheet 2 of 16  
Rev 0

Title: RH Redwood/ Broadway M2 package MXM3.0 DDR3 Doc No: 105-C076XX-00B



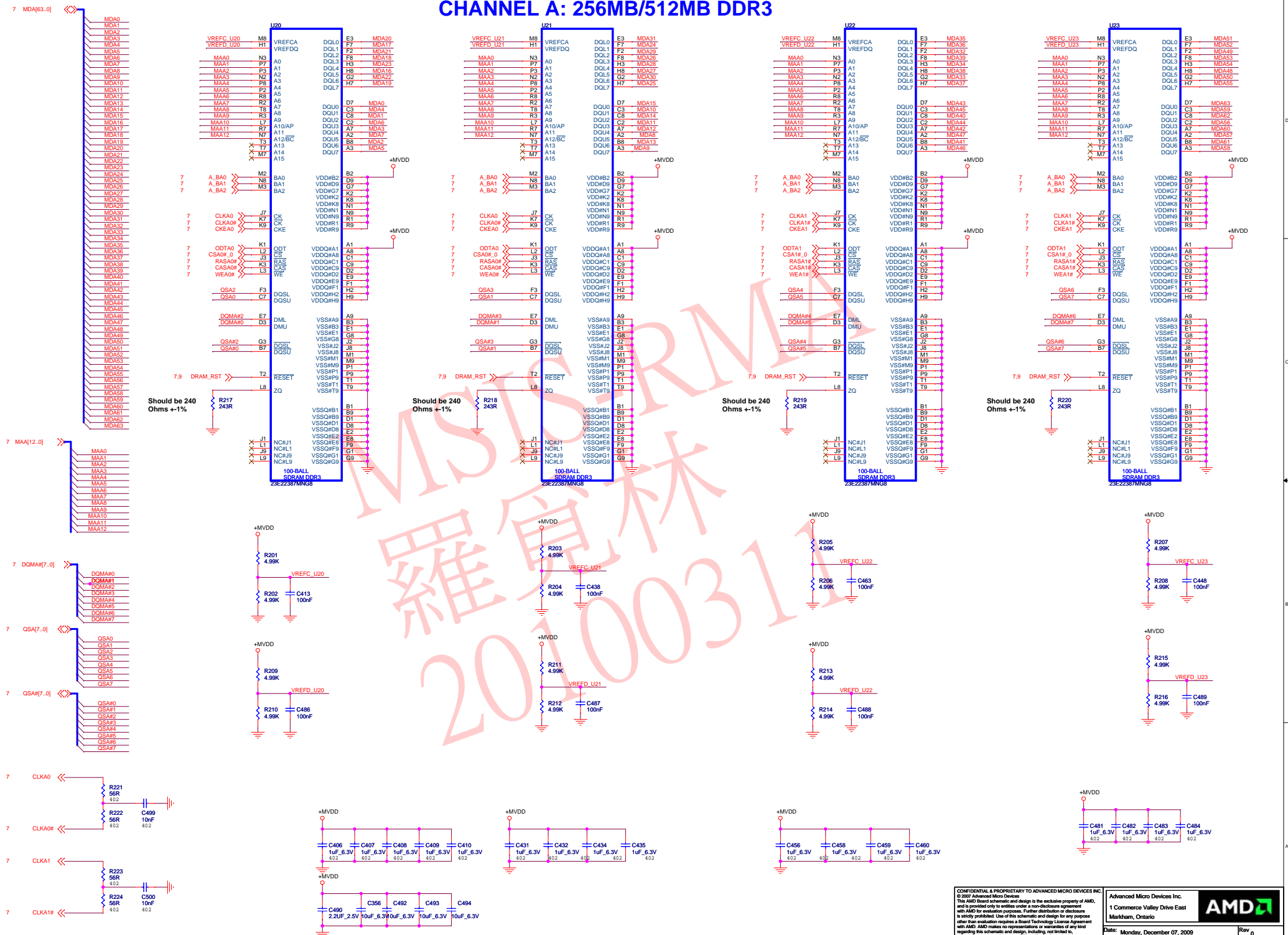






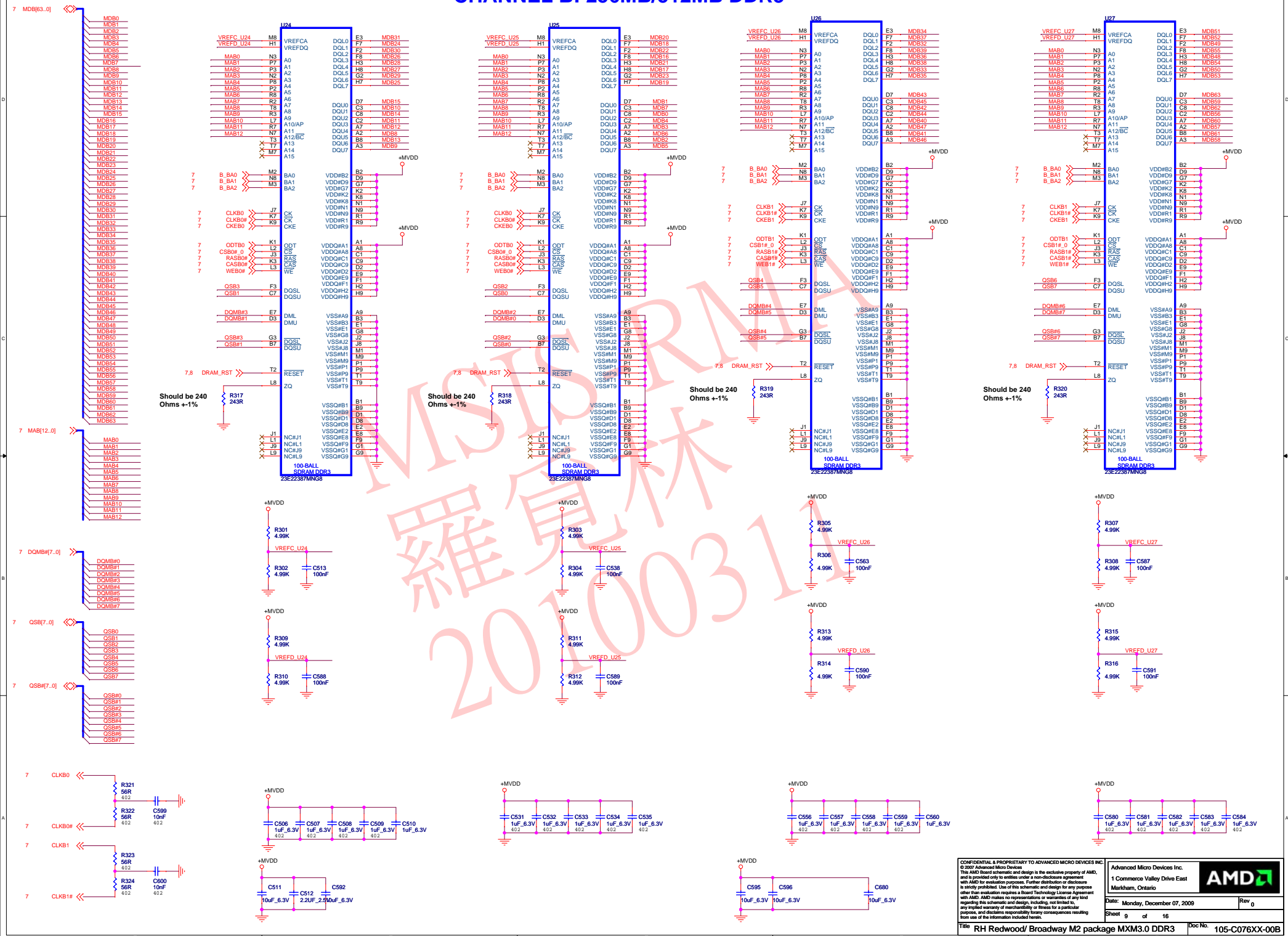


# CHANNEL A: 256MB/512MB DDR3

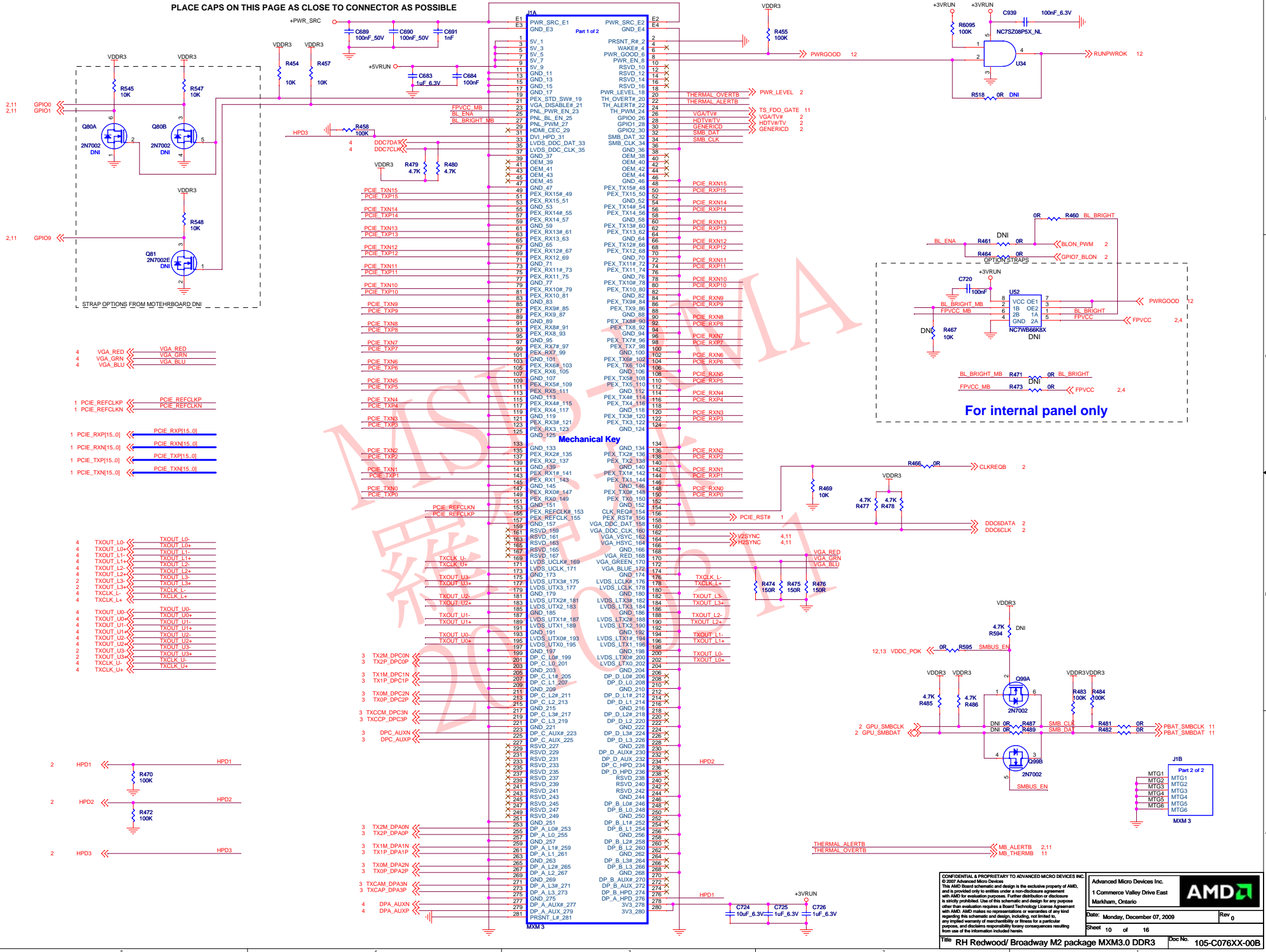


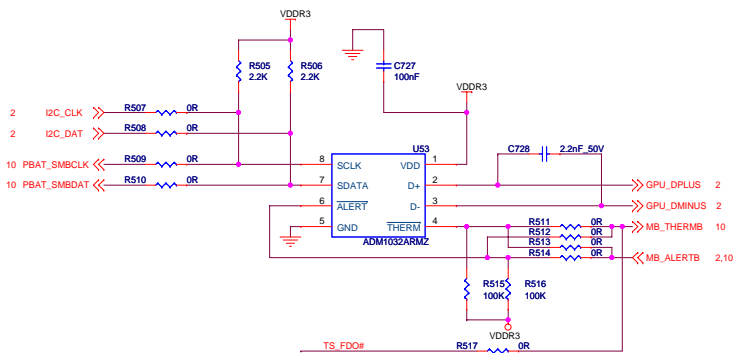


# CHANNEL B: 256MB/512MB DDR3



PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECT AS POSSIBLE





## PIN STRAPS



## CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC	built-in HDMI connector	0
CCBYPASS	HSYNC	Audio function present	0
AUD[1]	HSYNC	Audio function present	1
AUD[0]	HSYNC	Audio function present	1
MEMORY_CINFIG	[GPIOs.GPIO16]	Audio function present	1
HYNIX	[0:1]	Audio function present	1
SAMSUNG	[1:0]	Audio function present	1

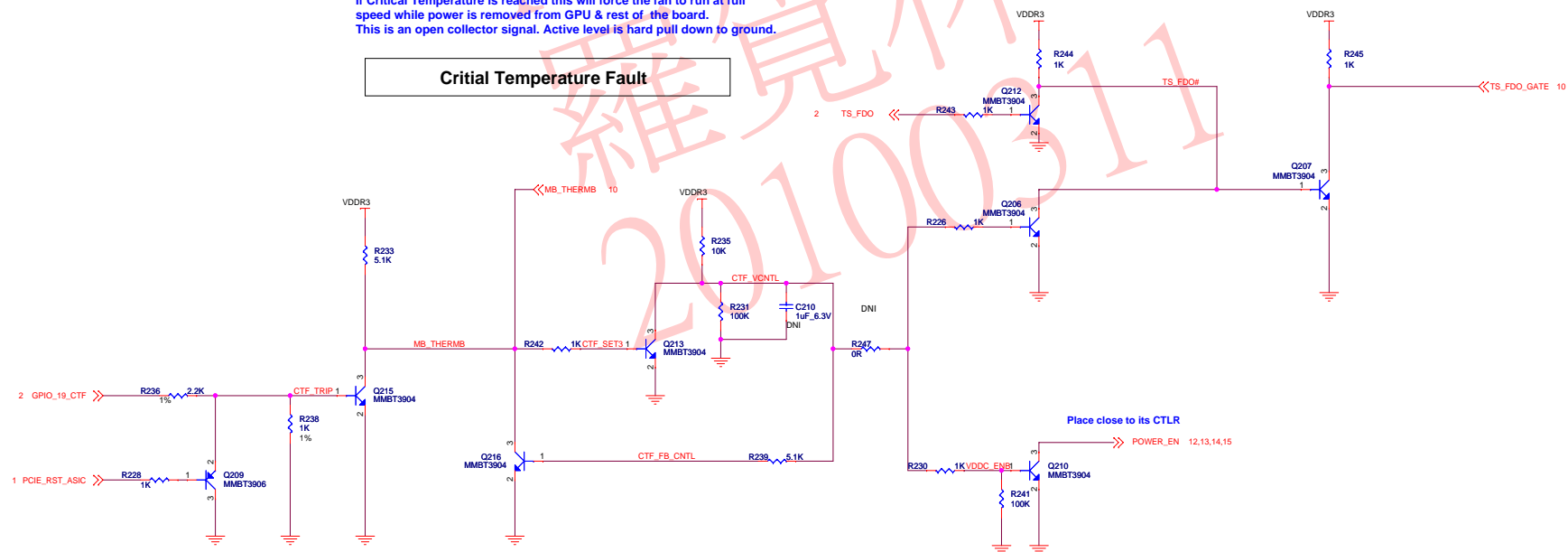
## AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

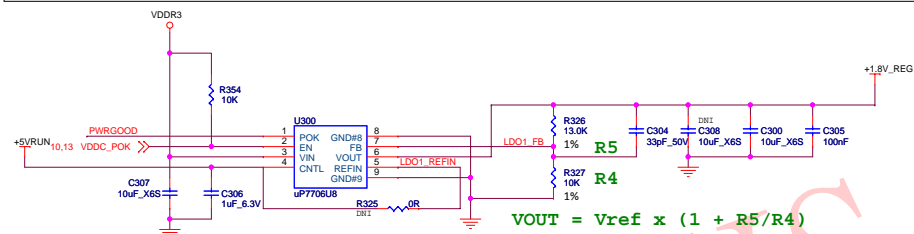
H2SYNC	GENERIC
GPIO_28_TDO	GPIO21_BB_EN

If Critical Temperature is reached this will force the fan to run at full speed while power is removed from GPU & rest of the board. This is an open collector signal. Active level is hard pull down to ground.

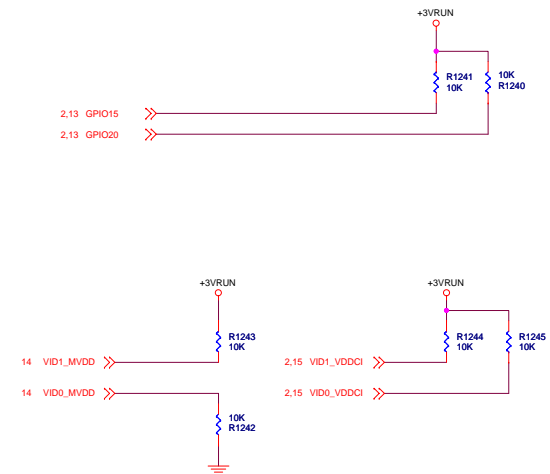
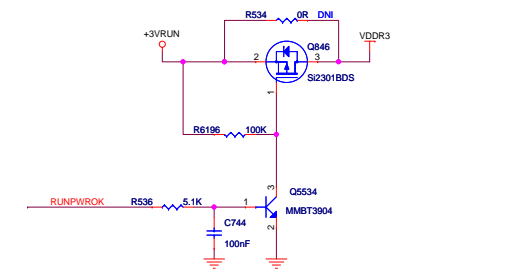
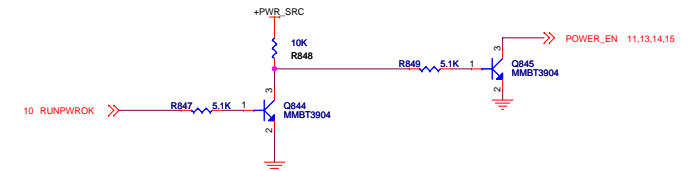
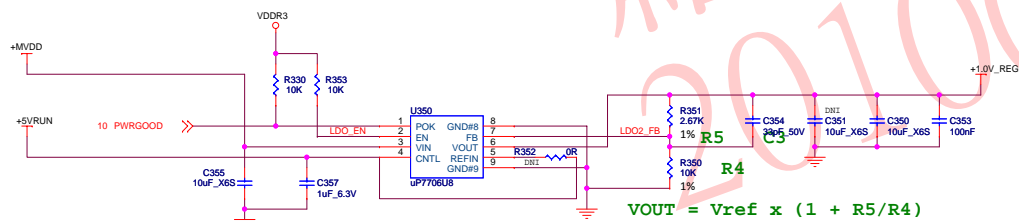
## Critical Temperature Fault



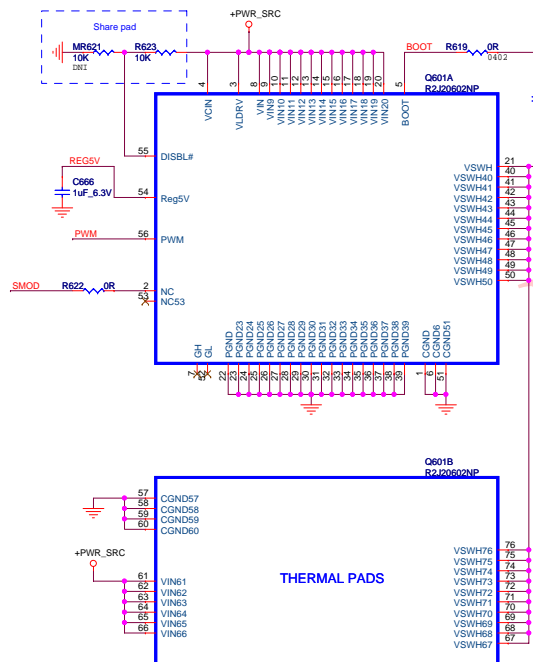
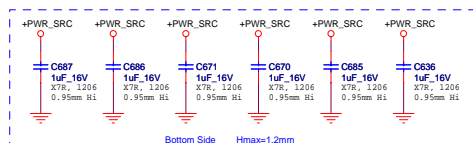
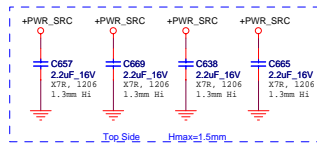
**LDO #1:** Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 0.8A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling



**LDO #2:** Vin = +1.32V to 1.84VMAX Vout = +1.0V +/- 2% Iout = 1.7A (TBV) RMS MAX  
PCB: 50 to 70mm sq. copper area for cooling



# INPUT CAP



Pin	Difference Between R2J2062NP and R2J2065NP
3	VLDIV
8	VIN
2	NC
53	NC

# OUTPUT CAP

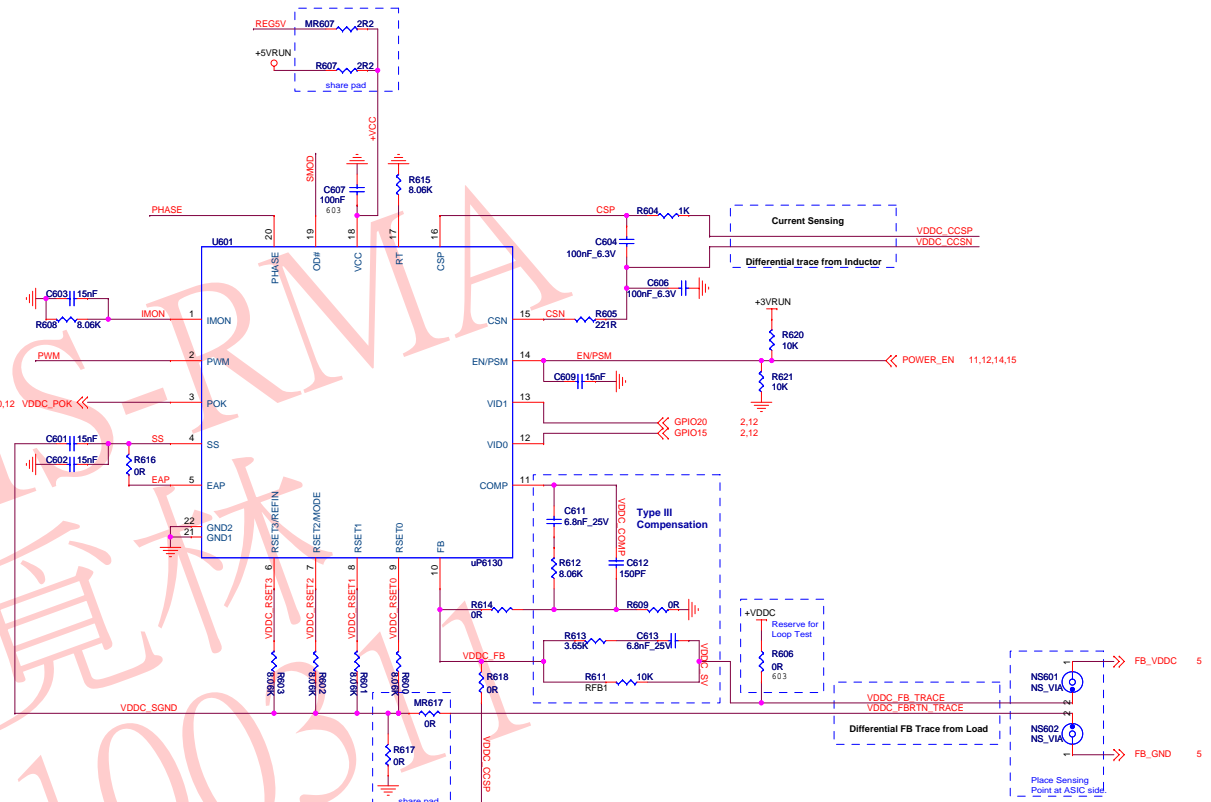
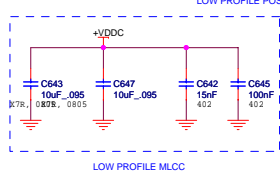
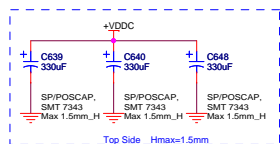
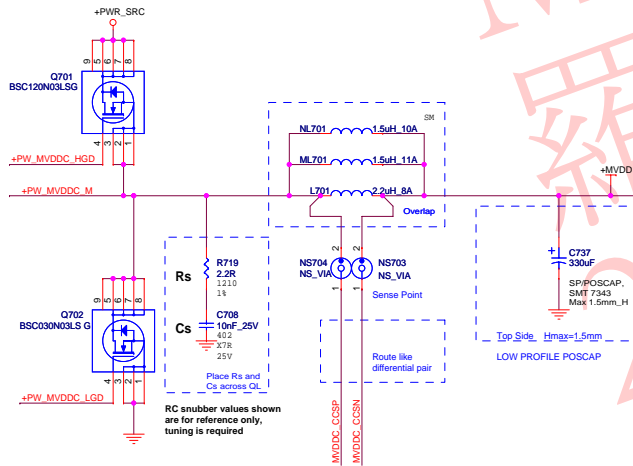



Figure 10 illustrates the recommended layout for the 100W module, showing the top and bottom sides of the PCB.

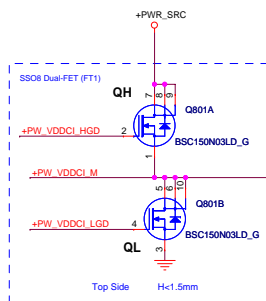
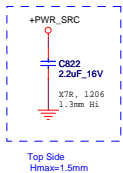
**Top Side:** The layout shows four power MOSFETs (C721, C732, C729, C731) connected to a PWR\_SRC and a common ground. The MOSFETs are arranged in a row, with C721 and C732 on the left, and C729 and C731 on the right. The layout is labeled "Top Side" and "Hmax=1.5mm".

**Bottom Side:** The layout shows two power MOSFETs (C730, C733) connected to a PWR\_SRC and a common ground. The MOSFETs are arranged in a row, with C730 on the left and C733 on the right. The layout is labeled "Bottom Side" and "Hmax=1.2mm".

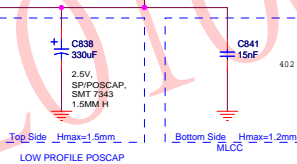
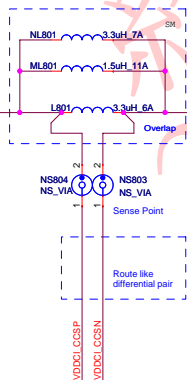


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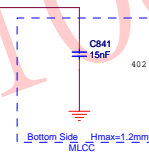
# INPUT CAP



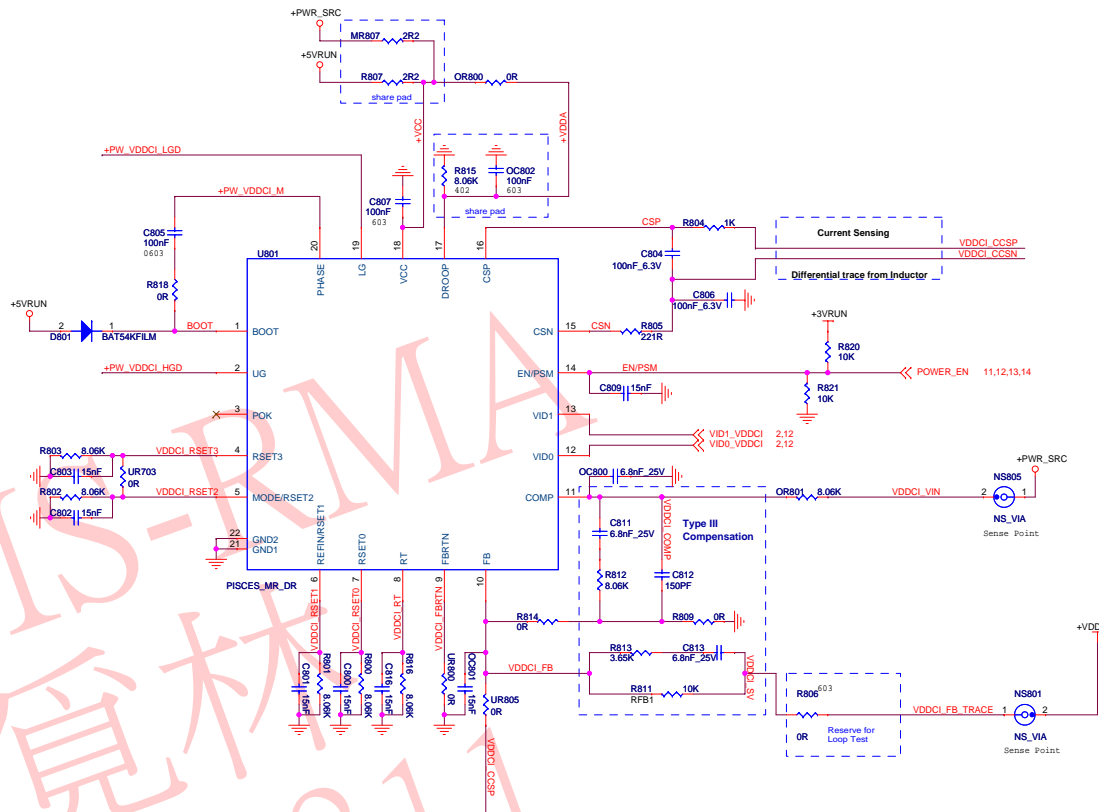
Place Rs and Cs across QL  
RC snubber values shown  
are for reference only,  
tuning is required



LOW PROFILE POSCAP



MLCC



<div>AMD</div>			Title		Schematic No.		Date:	
			RH Redwood/ Broadway M2 package MXM3.0 DDR3		105-C076XX-00B		Monday, December 07, 2009	
			REVISION HISTORY		NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.			Rev 0
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION					
0	00A	09/27/09	Create new SCHs					
	00B	12/03/09	Added PWR_EN short to DrMOS Added DrMOS Thermal Pad					
			<div>MSIS-RMA 羅覓林 20100311</div>					