

P2030

GK106, 2GB GDDR5, 192b mixed mode x16, x32
Stacked DVI-I/DVI-D + HDMI/DP + DP

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Basen on V287-1.1

- 1.page 22 change PEX_VDD and PEX_VDD1 circuit
- 2.page 23 change FBVDDQ circuit
- 3.page 25/26 change NVVDD circuit
- 4.page 19 and 20 remove SLI 相關co-lay circuit
- 5.page 29 remove SLI LED circuit
- 6.page 27 remove input power co-lay circuit
- 7.page 15 and 16 add DVI ESD component
- 8.page 17 add HDMI I2C ESD component
- 9 page 17 remove DP co-layout

REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-12030-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-12030-0000-000	GK106-400, 2048MB, GDDR5 192b Stacked DVI-I DL/DVI-D DL, HDMI, DP
2	SKU0010	600-12030-0010-000	GK106-250, 2048MB, GDDR5, 192b Stacked DVI-I DL/DVI-D, HDMI, DP
3	SKU0050	600-12030-0050-000	GK106-200, 2048MB, GDDR5, 128b Stacked DVI-I DL/DVI-D, HDMI, DP
4	SKU0060	600-52030-0060-000	GK106-875, 3072MB, GDDR5, 192b DVI-I DP, DP Workstation
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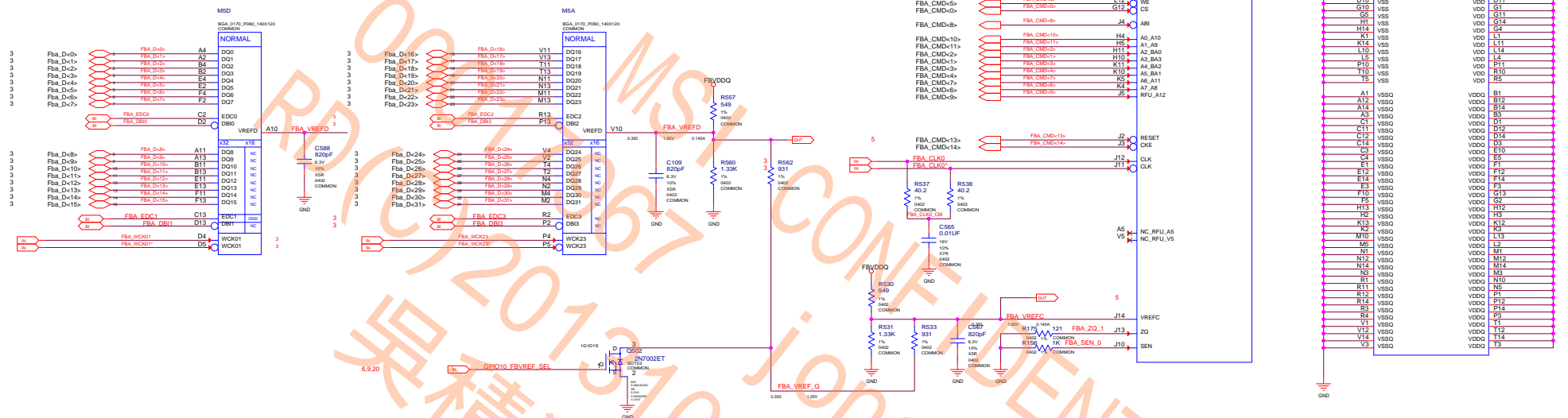
	MICRO-STAR INT'L CO.,LTD		
	MS-V295		
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	Custom	01_Table of Contents	10
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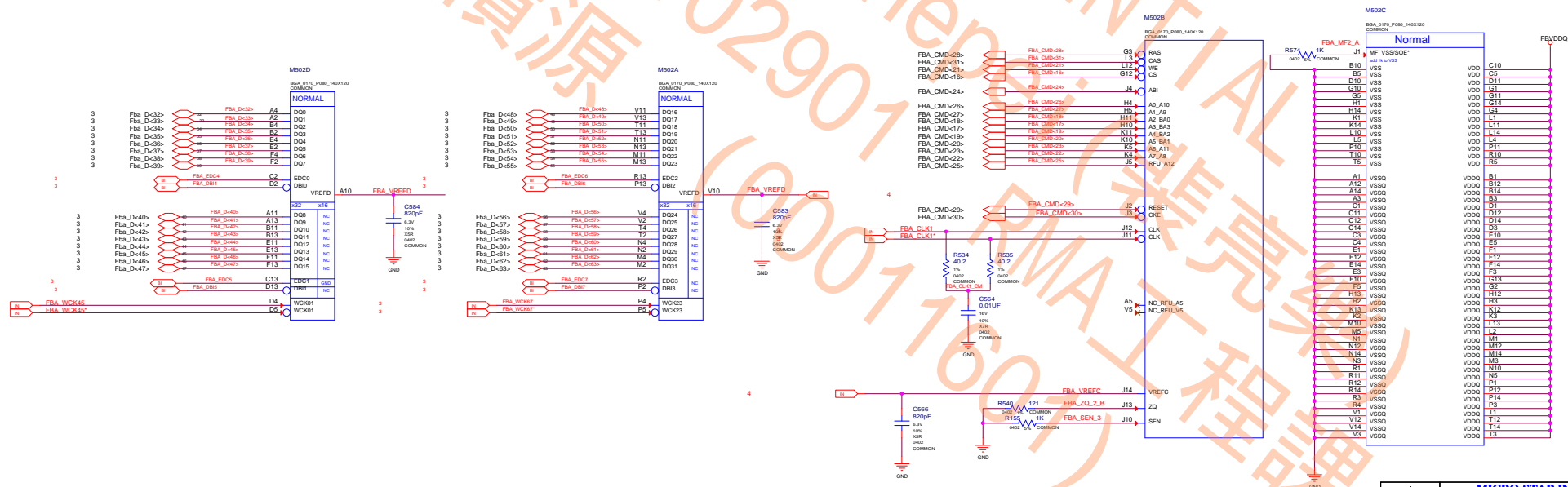
PCI Express

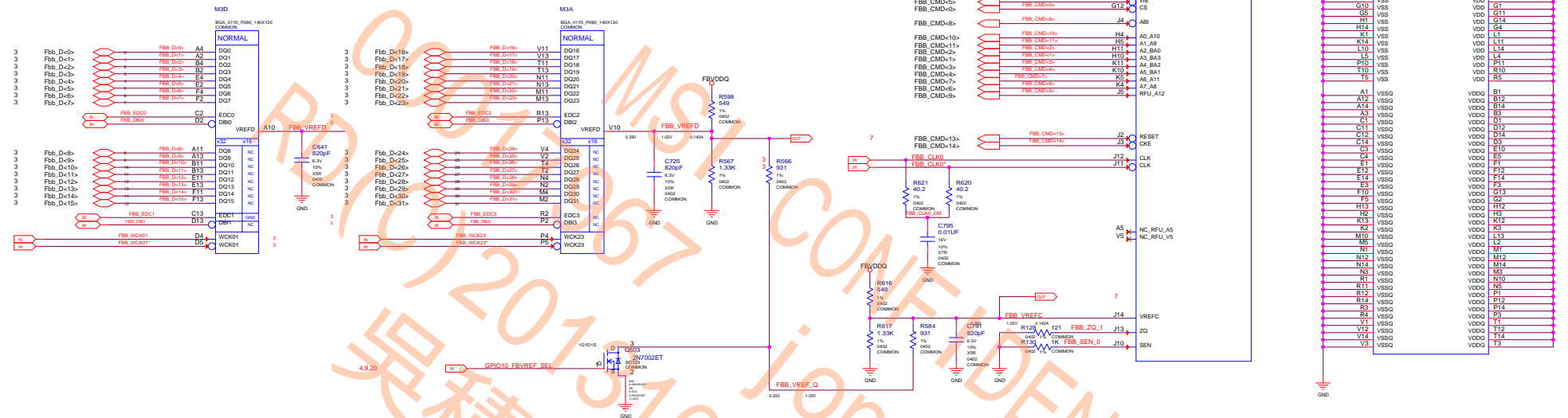


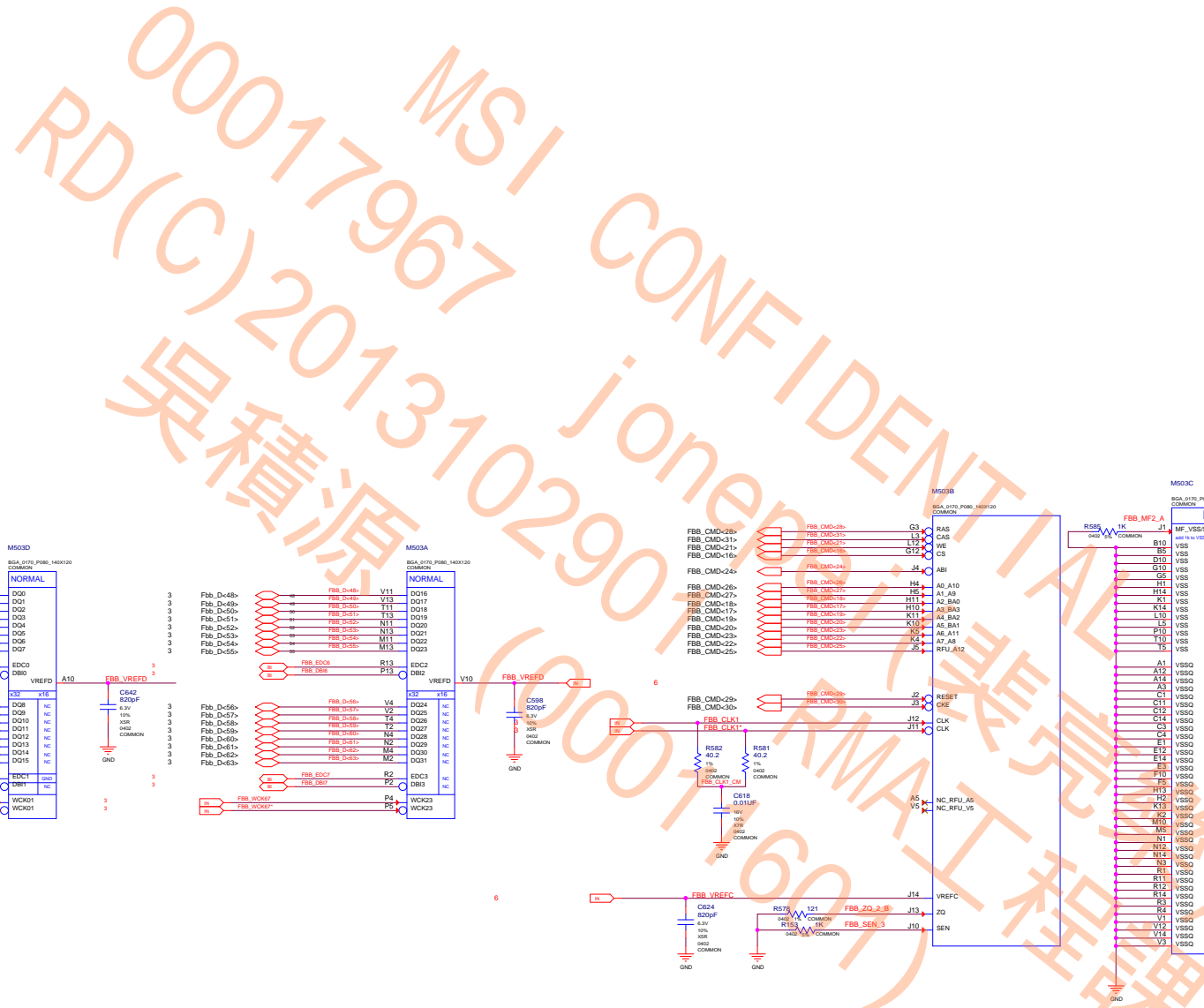


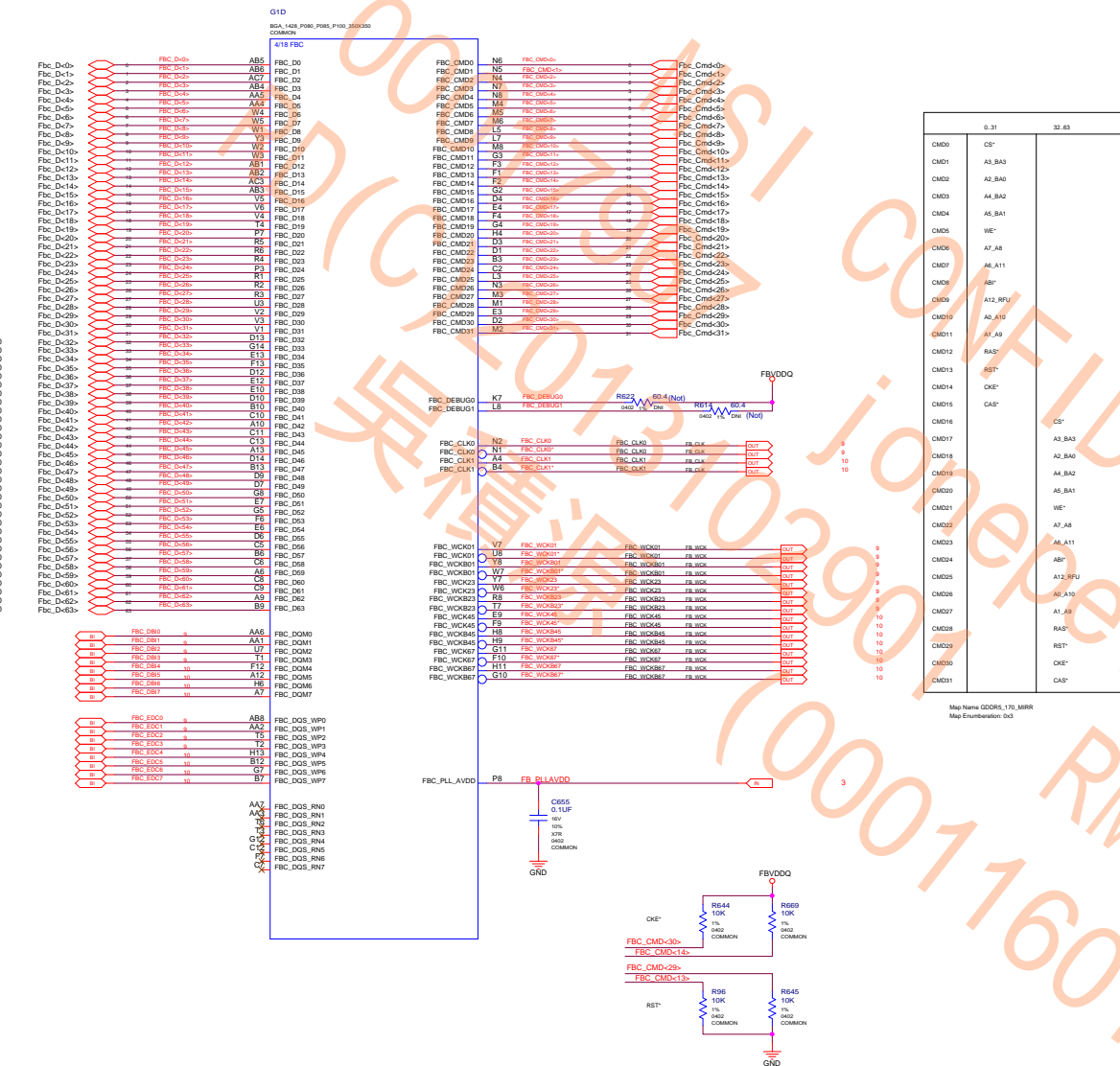
MEMORY: FBA Partition 31..0



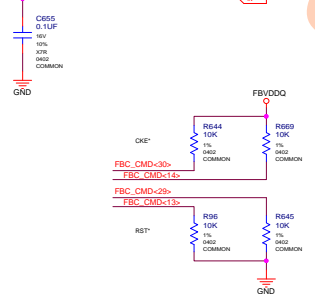


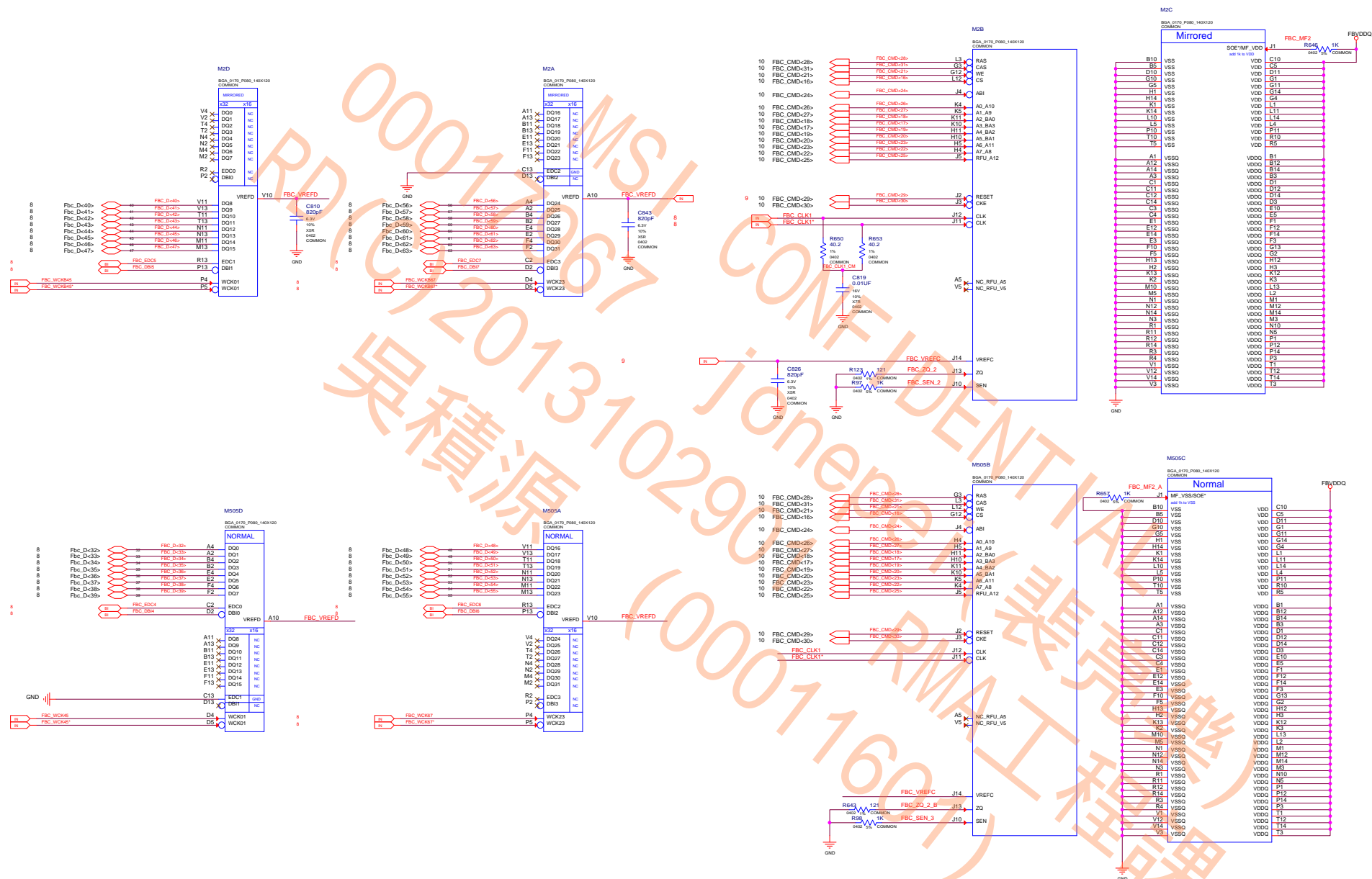




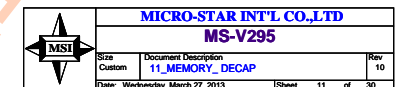
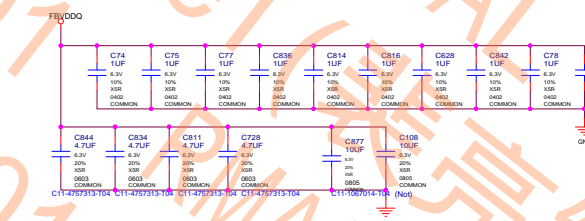
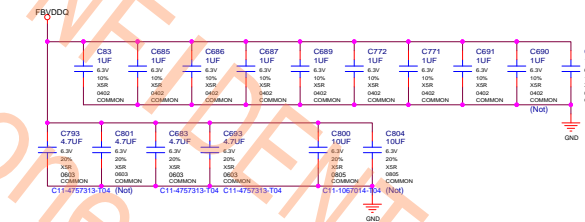
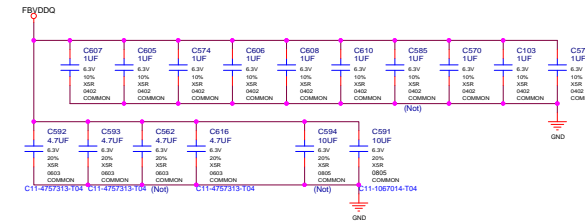


	0.31	32.83
CM000	CS*	
CM001	A3_BA3	
CM002	A2_BA0	
CM003	A4_BA2	
CM004	A5_BA1	
CM005	WE*	
CM006	A7_A8	
CM007	A8_A11	
CM008	AB*	
CM009	A12_RFU	
CM010	A0_A10	
CM011	A1_A9	
CM012	RA5*	
CM013	RS*	
CM014	CKE*	
CM015	CAS*	
CM016		CS*
CM017		A3_BA3
CM018		A2_BA0
CM019		A4_BA2
CM020		A5_BA1
CM021		WE*
CM022		A7_A8
CM023		A8_A11
CM024		AB*
CM025		A12_RFU
CM026		A0_A10
CM027		A1_A9
CM028		RA5*
CM029		RS*
CM030		CKE*
CM031		CAS*

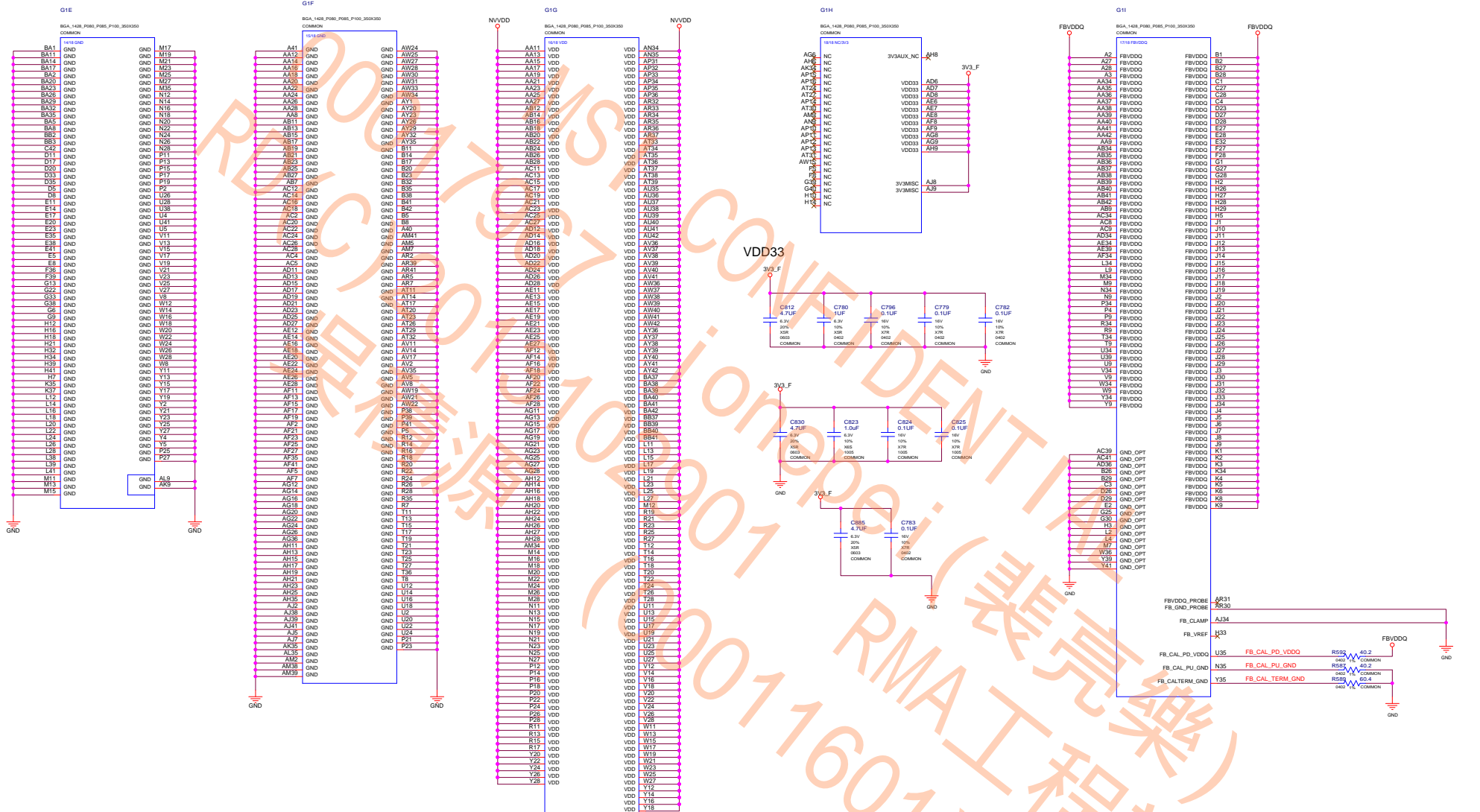




A	B	C	D	E	F	G	H
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GPU PWR and GND



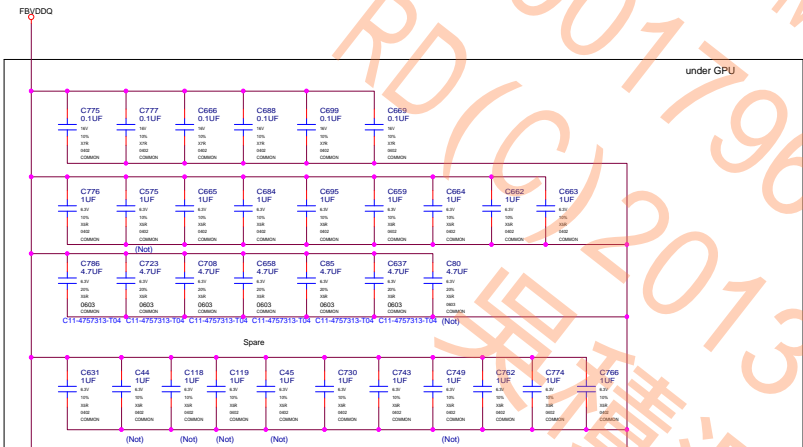
MICRO-STAR INT'L CO.,LTD

MS-V295

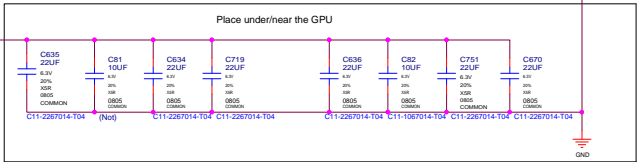
Size Custom	Document Description 12_GPU PWR and GND	Rev 10
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GPU Decoupling

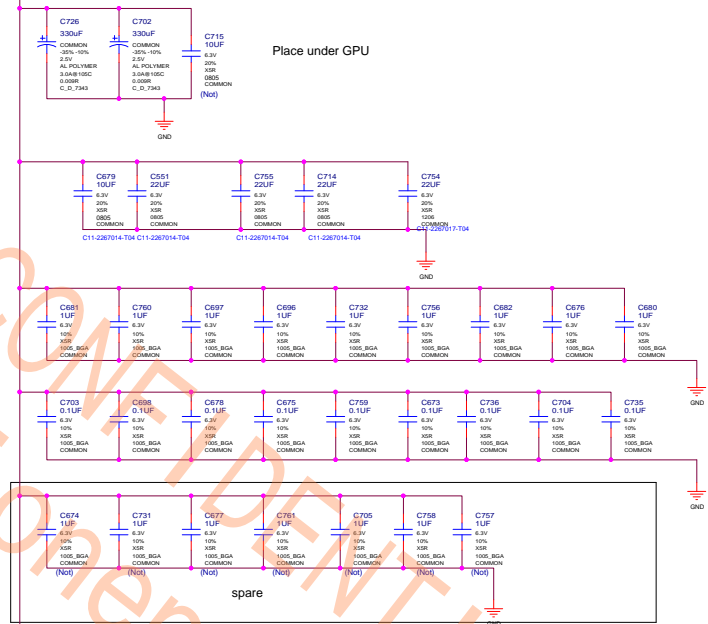
FBVDDQ



Place under/near the GPU

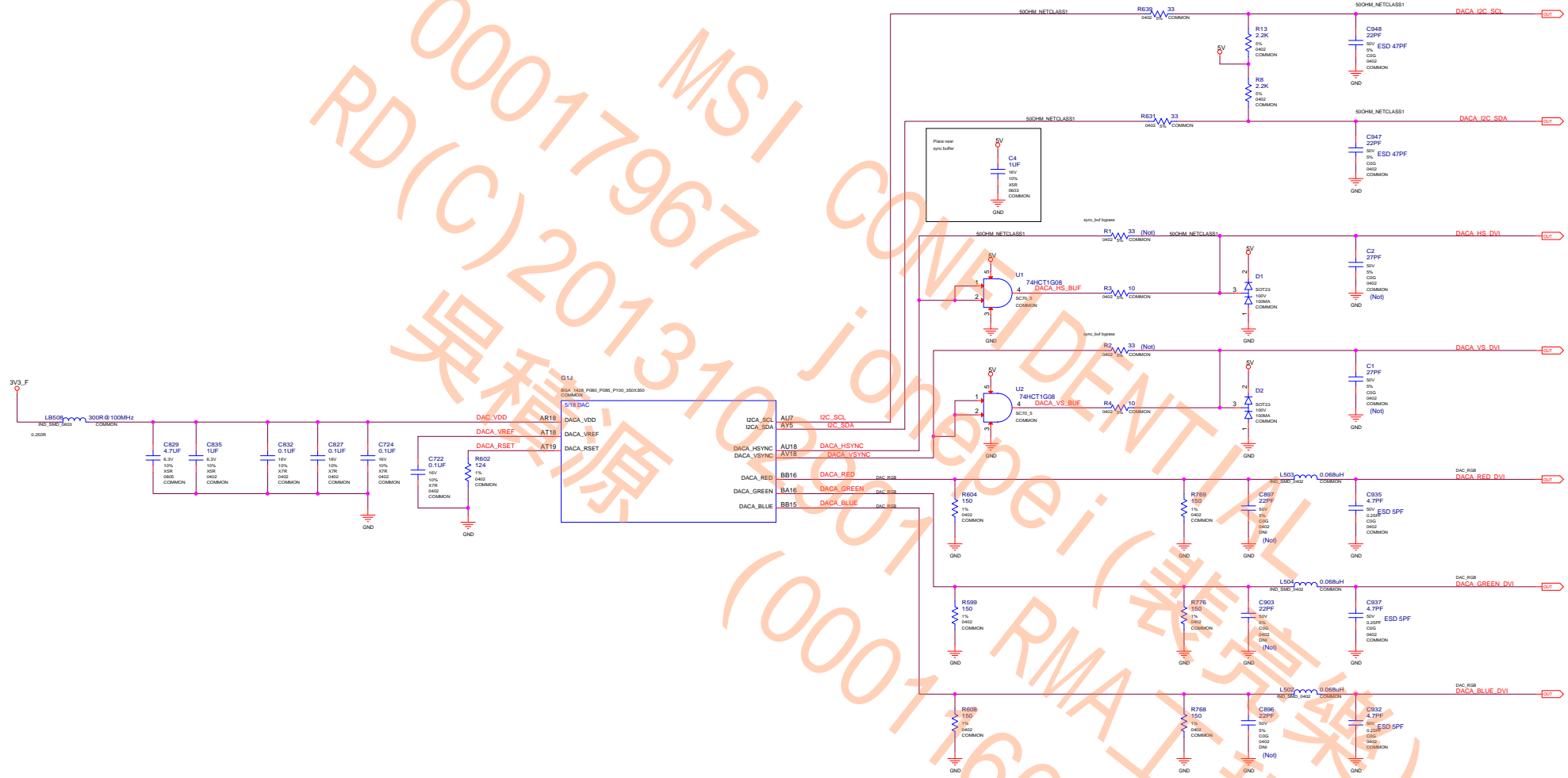


NVDD



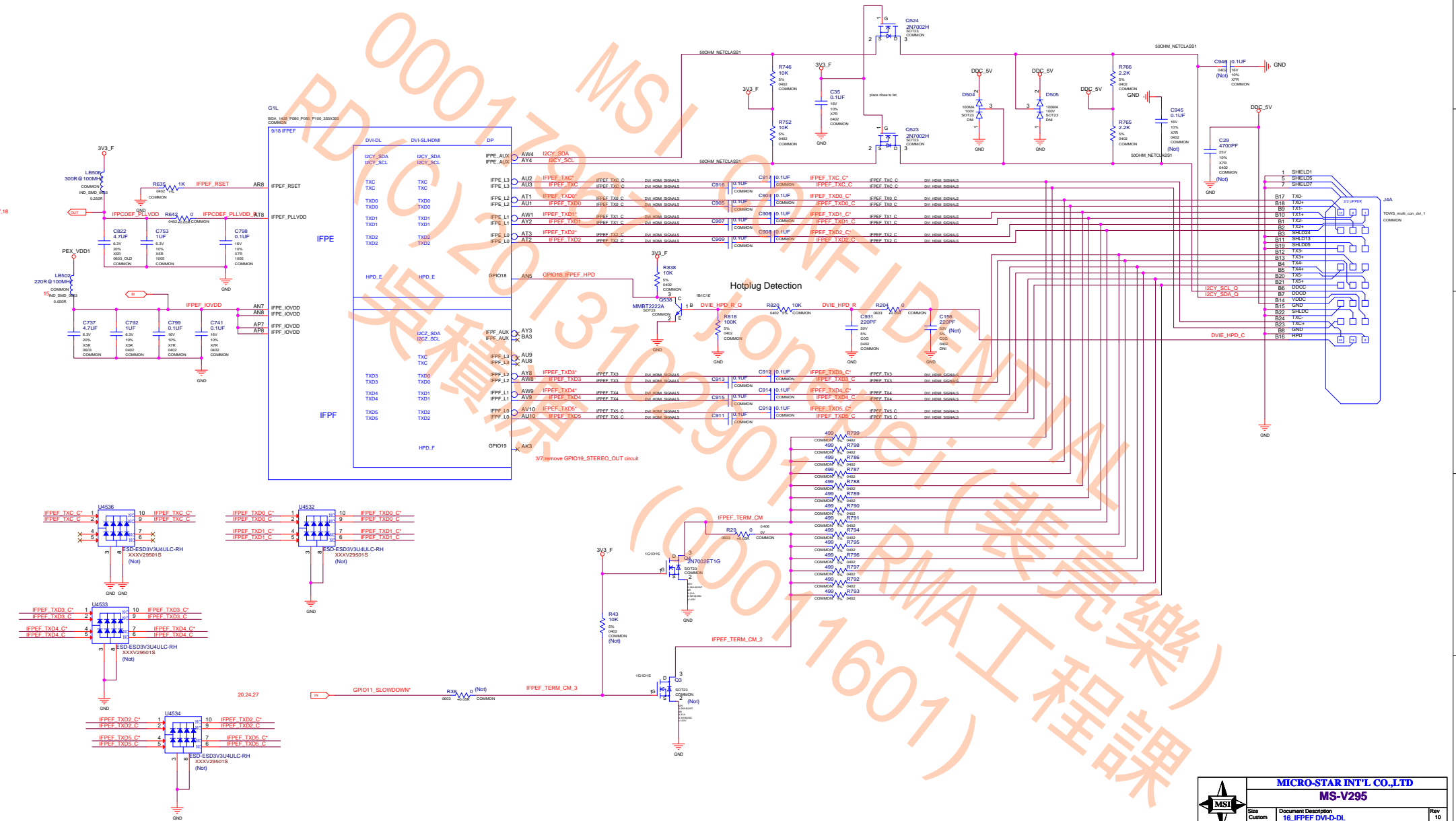
	guidelines	actual
Under GPU	2x 330uF 9mOhm	1x 330uF 9mOhm
	1x 47uF 1206	1x 22uF 1206
	2x 22uF 805	4x 22uF 805
	2x 10uF 805	9x 10uF 805
	9x 0.1uF 402	9x 0.1uF 402
	9x 0.1uF 402	spare sites (not stuffed)
		1x 7543
		27x 402
near GPU	1x 47uF 1206	2x 22uF
	2x 22uF 805	spare sites (not stuffed)
	2x 10uF 805	2x 4.7uF 603
	1x 10uF 402	3x 805
	1x 0.1uF 402	

DACA Interface

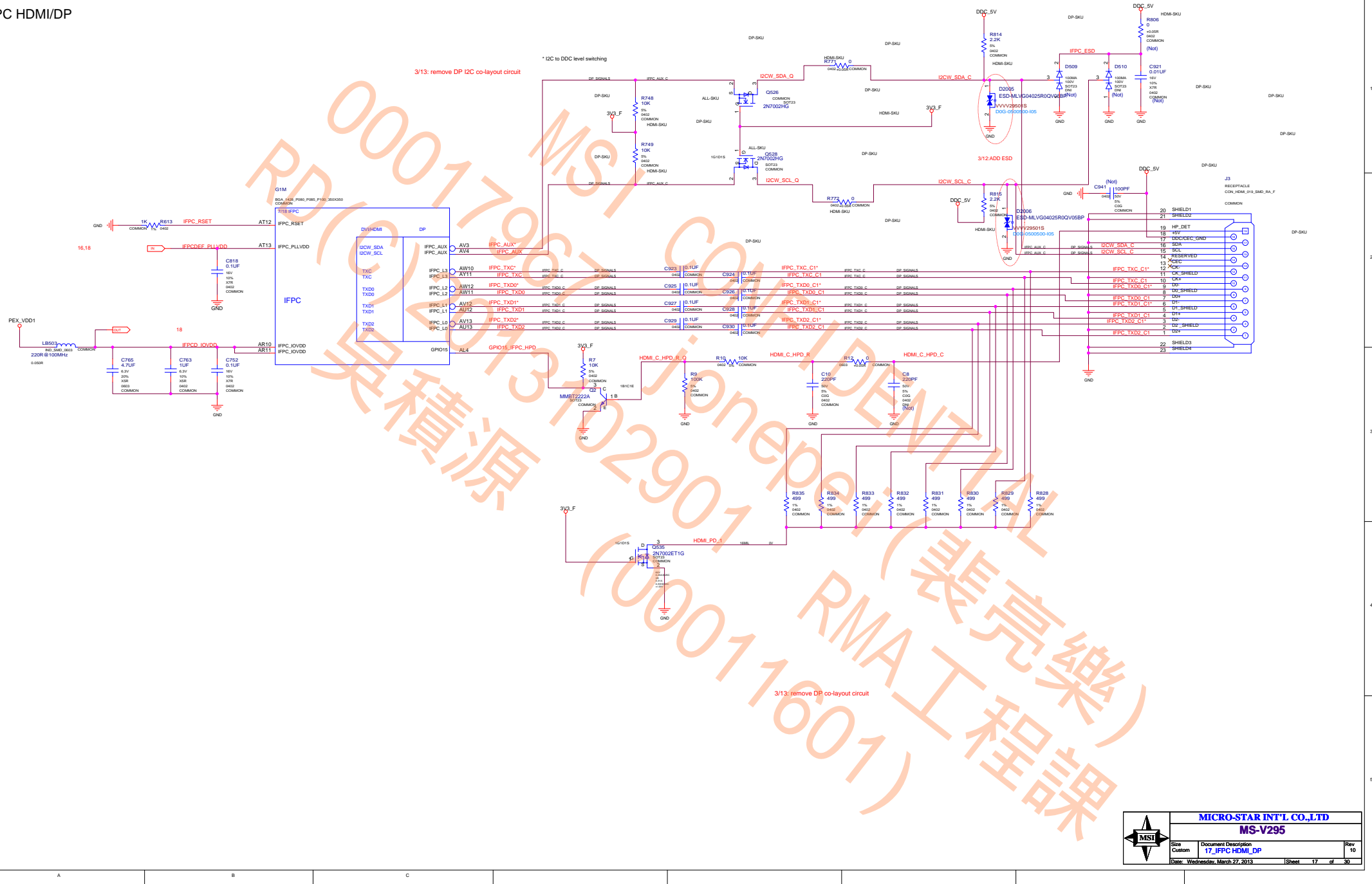


NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DAC_VDD	3.3V	0.25A	16MIL

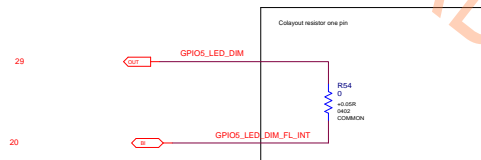
			MICRO-STAR INT'L CO.,LTD MS-V295	
Size	Custom	Document Description	14_DACA Interface	Rev 10
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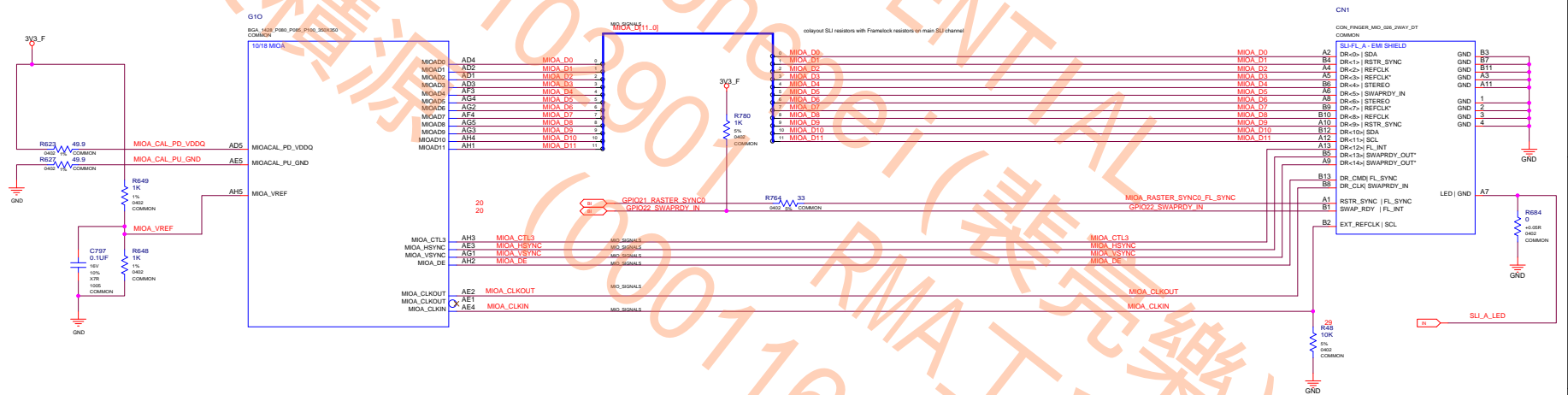
IFPC HDMI/DP



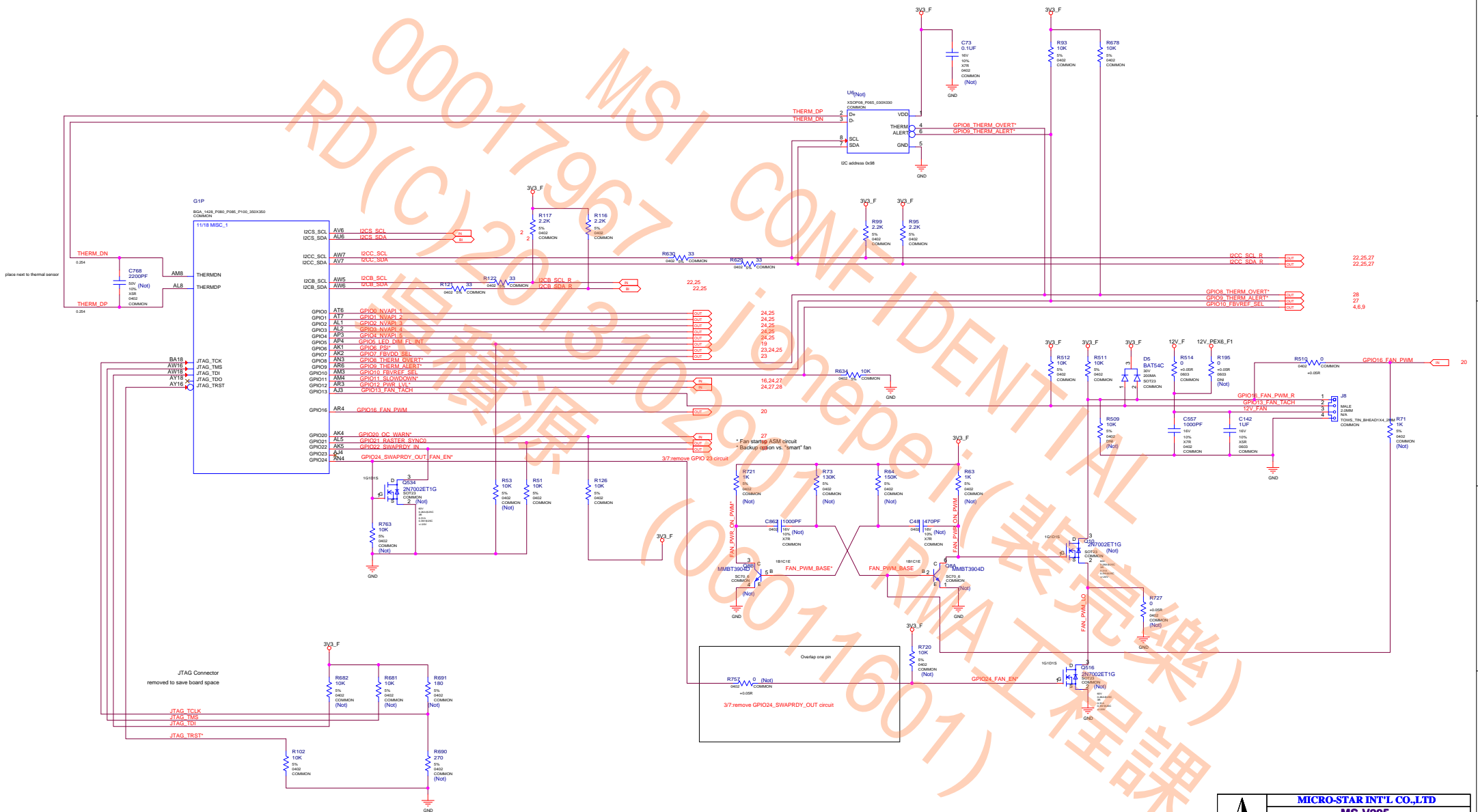
MIOA/SLI Interface



37:remove GPIO19_STEREO_OUT and PEX_RST_BUF* and XTALSSIN_GPU circuit



MISC1: Fan, Thermal, JTAG, GPIO

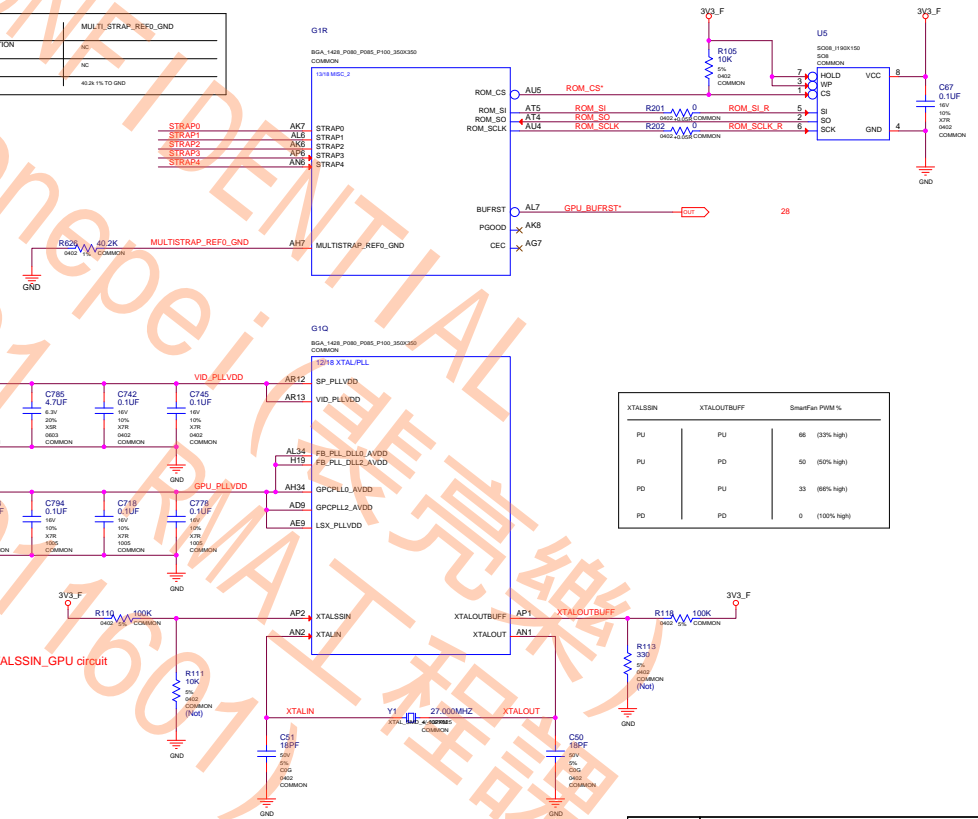


MISC2: ROM, XTAL, Straps

STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0000 - (0x11C0)* 0010 - (0x11C1)* 0050 - (0x11C4)* 0500 - (0x11FA)*	5K PD -400 GPU* 10K PD -250 GPU* 25K PD -225 GPU* 15K PU -875 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	35K PU*
STRAP4	*		
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	45K PD*
	PEX_MAX_SPEED*	1* FOR GEN2/3*	
	DP_PLL_VDD_33V*	1* FOR 3_3V*	
ROM_SI	RAMCFG[3]*	0*	35K PD* 45K PD*
	RAMCFG[2]*	1*	Hylix Samsung
	RAMCFG[1]*	1*	
	RAMCFG[0]*	0*	
ROM_SO	FB[1]_APERTURE_SIZE*	0* For 128MB*	
	FB[0]_APERTURE_SIZE*	1* For 128MB*	30x PD*
	SMB_ALT_ADDR*	0*	
	VGA_DEVICE*	1*	
ROM_SCLK	PCI_DEVID_EXT[4]*	0* For 0x11C0*	25K PD* 25K PD* 25K PD* 35K PU*
	SUB_VENDOR*	1* Dedicated BIOS*	StdA0: 11C0 StdA1: 11C1 StdA2: 11C4 StdA3: 11FA
	PCI_DEVID_EXT[5]*	0* For 0x11C0*	
	PEX_PLL_EN_TERM100*	0* ENABLED*	

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI LEVEL	40.2% 1% TO GND



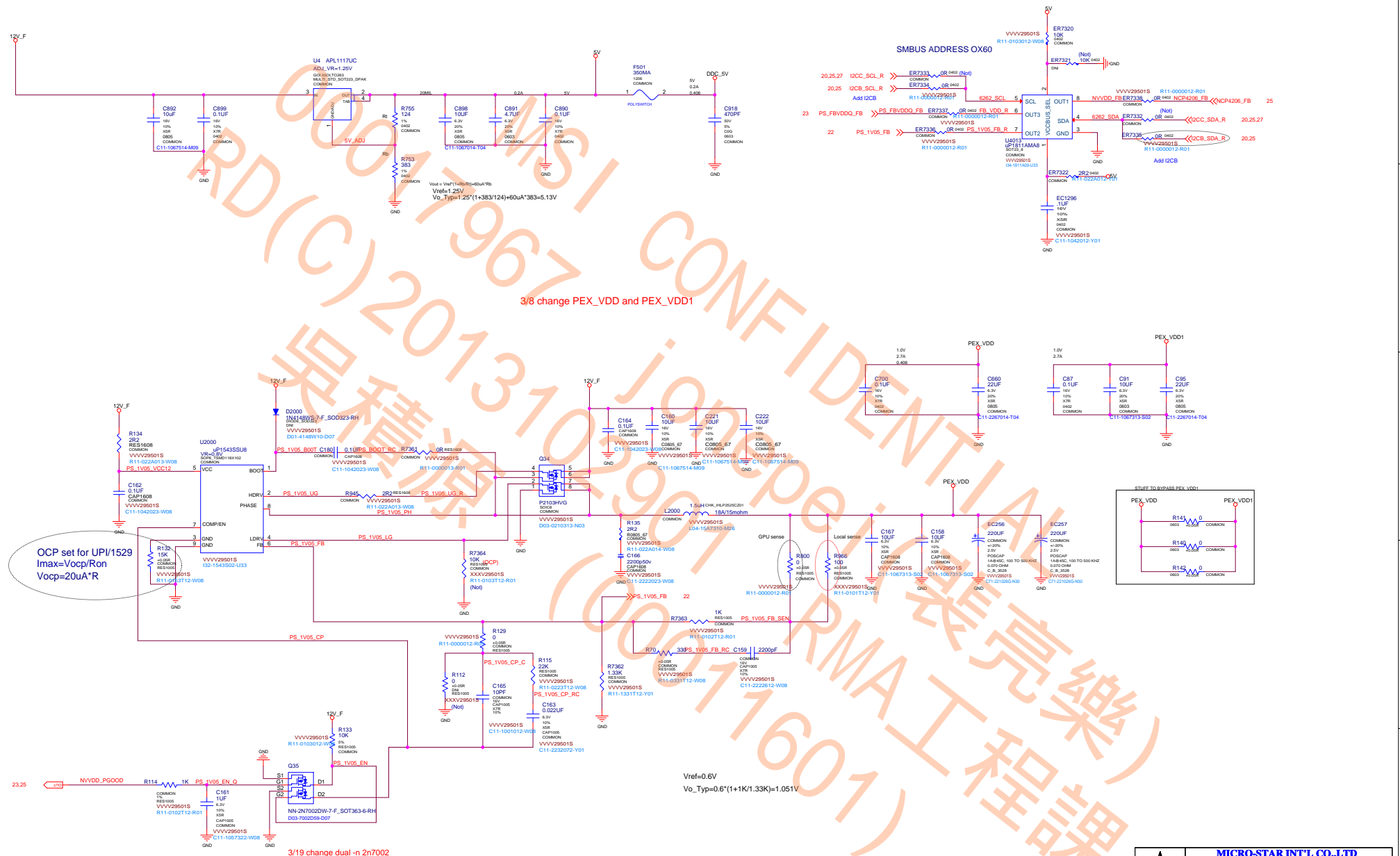
XTALSSN	XTALOUTBUFF	SmartFan PWM %
PU	PU	66 (33% high)
PU	PD	50 (50% high)
PD	PU	33 (66% high)
PD	PD	0 (100% high)



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PS: 5V, PEX_VDD

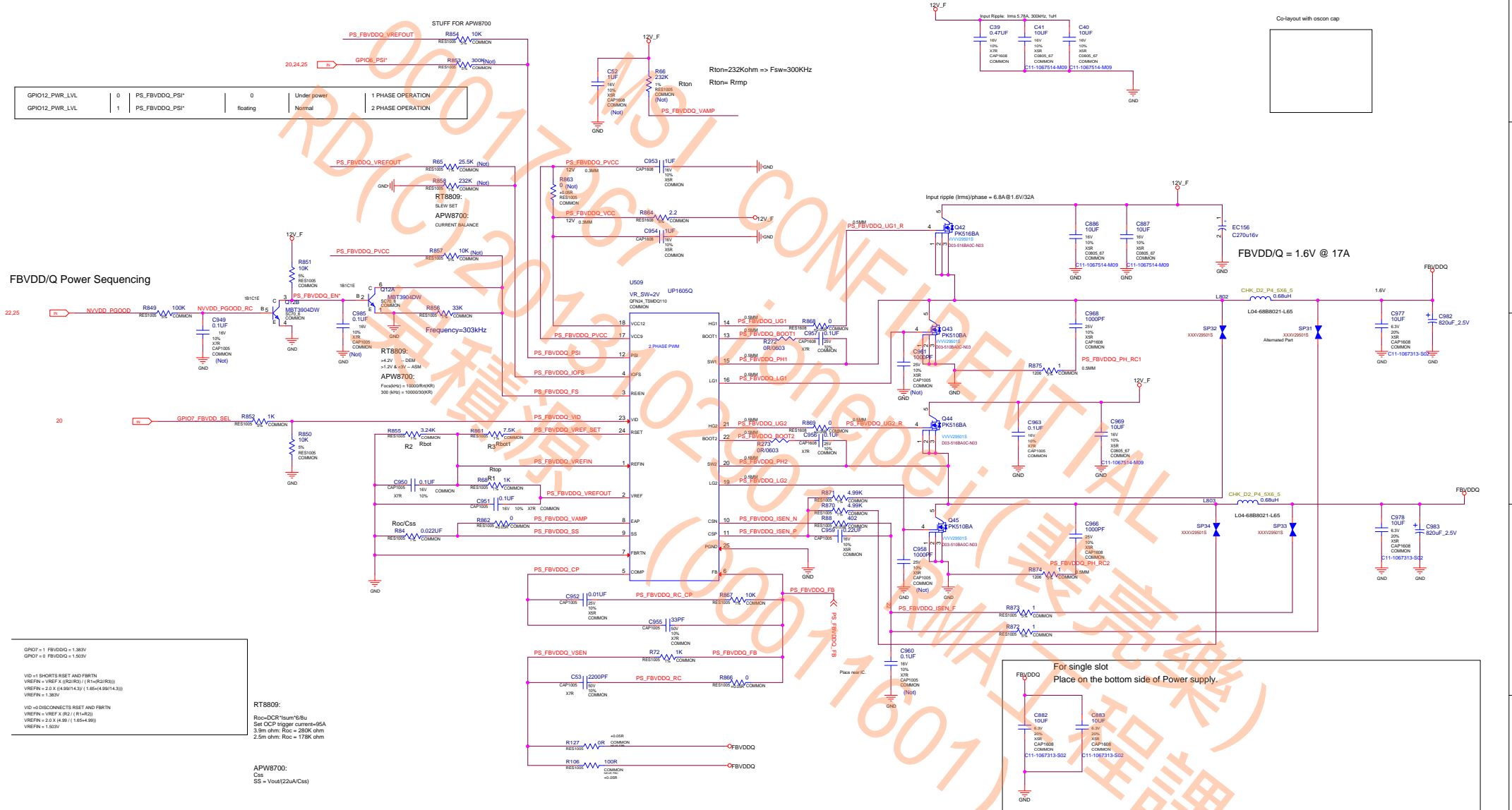


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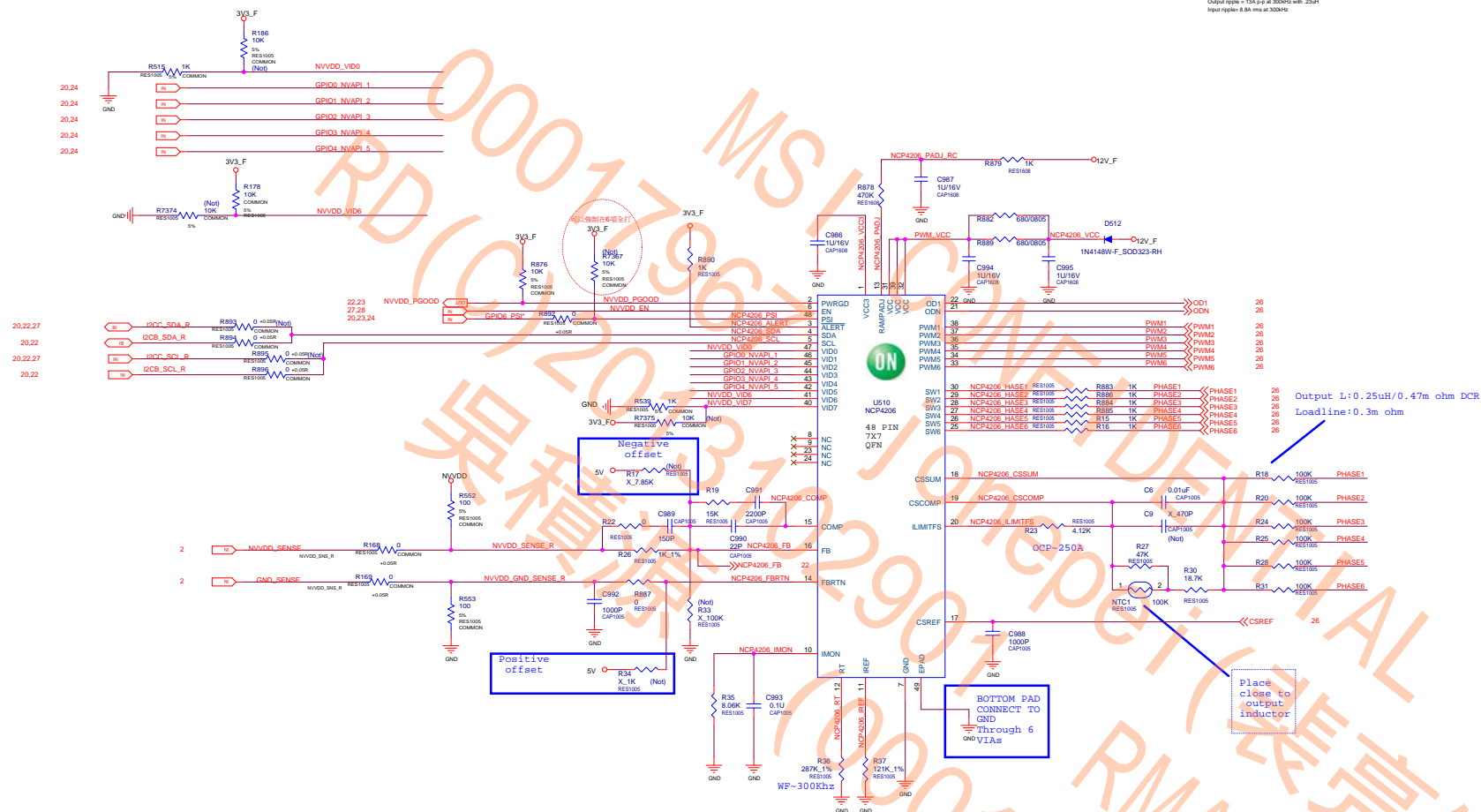
Size Custom	Document Description 22_PS_5V, PEX_VDD	Rev 10
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PS: FBVDDQ



PS: NVVDD
2/3/4/5/6 PHASE DESIGN

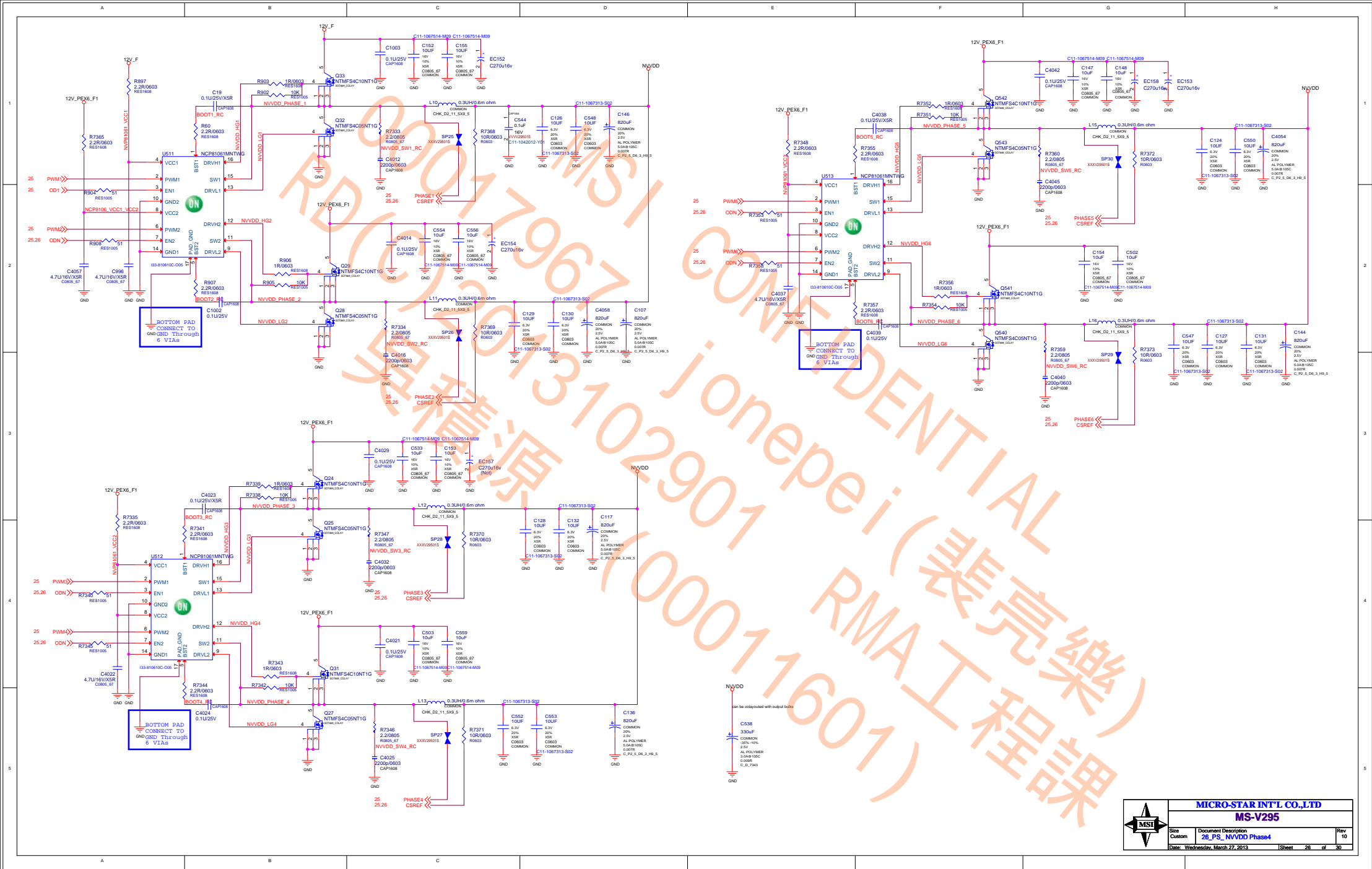
Output ripple = 13A p-p at 300kHz with .23uH
Input ripple= 8.8A rms at 300kHz



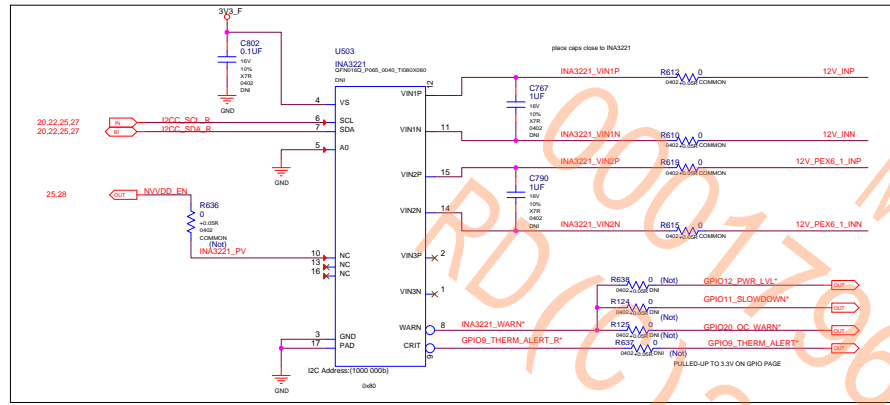
MICRO-STAR INT'L CO.,LTD

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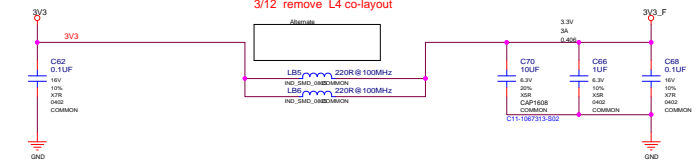
Size Custom	Document Description 25_PS_NVDD Supply	Rev 10
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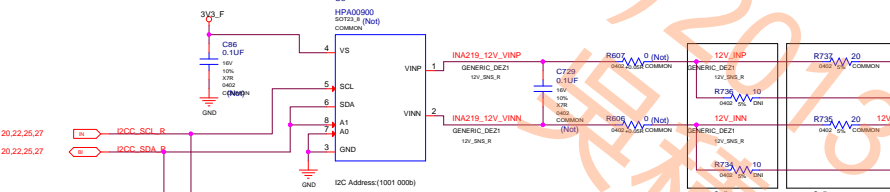
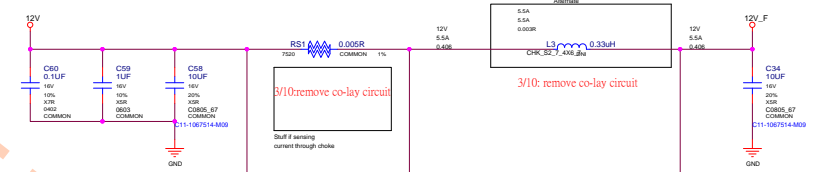
PS: Inputs, Filtering, and Monitoring



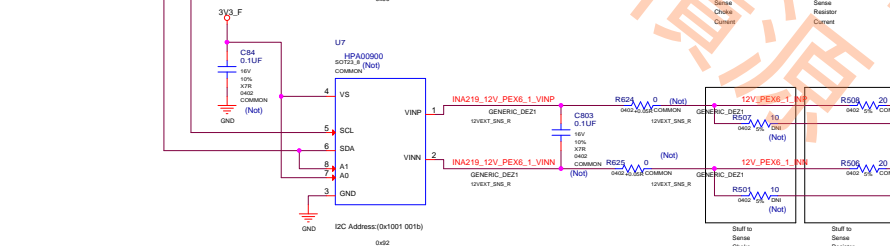
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



20.24.28
16.20.24
20
20



20.24.28
16.20.24
20
20

20.24.28
16.20.24
20
20

20.24.28
16.20.24
20
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16.20.24
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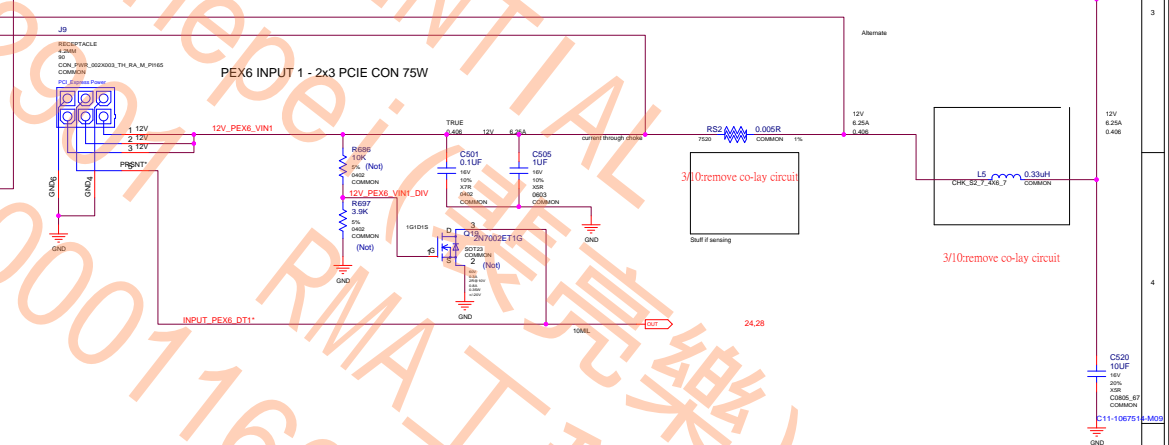
20.24.28
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16.20.24
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16.20.24
20
20

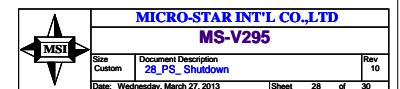
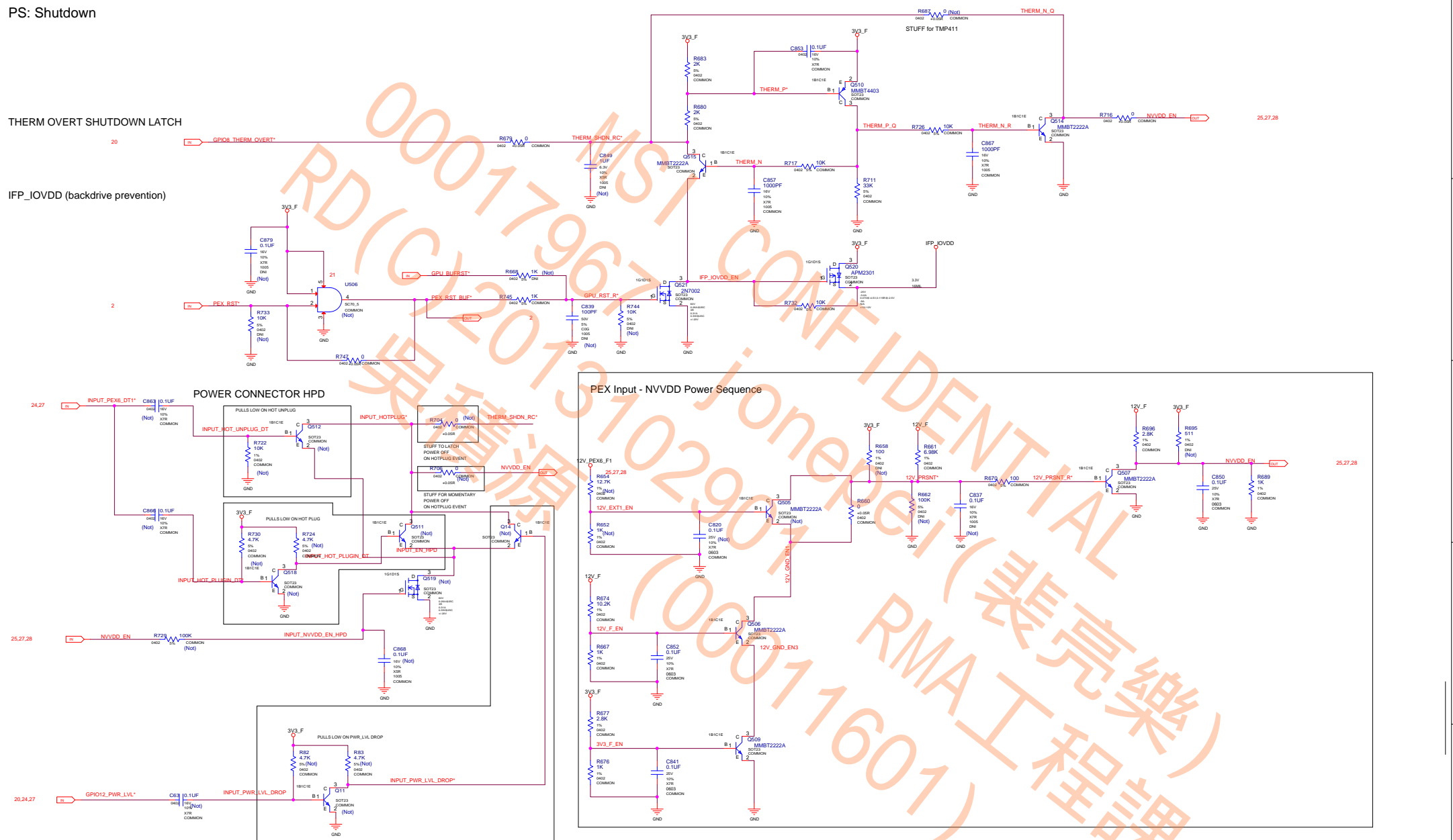
PEX6 INPUT 1 - 2x3 PCIe CON 75W



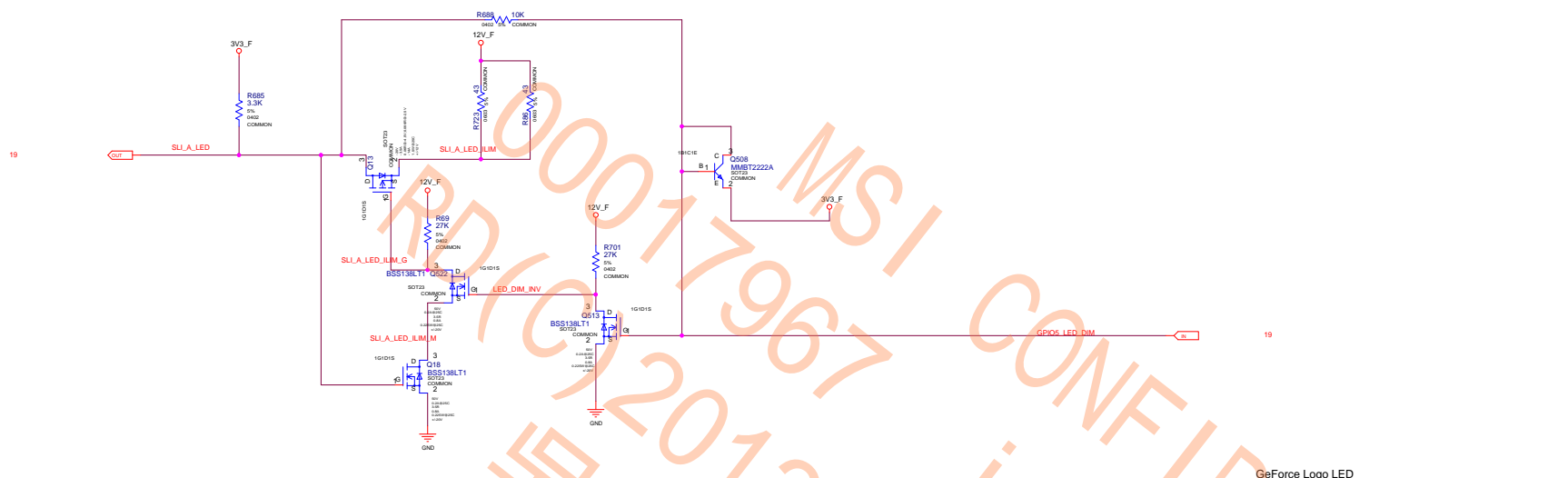
PS: Shutdown

THERM OVERT SHUTDOWN LATCH

IFP_IOVDD (backdrive prevention)



PS: Board LED



GeForce Logo LED

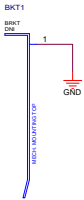
LED HEADER
(COMMON)

3/7: remove LED circuit

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Custom	29_PS_Board LED; Lighted SLI	10
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Mechanical: Bracket/Thermal Solution

Bracket:



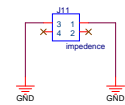
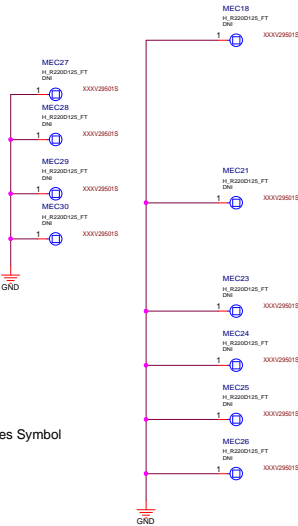
Bracket Screw



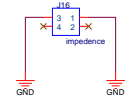
Hockey Stick



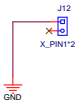
Mechanical Holes Symbol



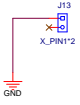
TOP Differential_WCK
0.12 / 0.101mm 80 ohm +/- 10%



INT3 Differential_Memory Clock
0.103 / 0.101mm 80 ohm +/- 10%

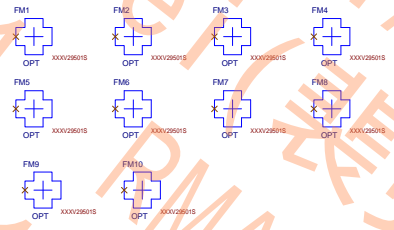


TOP FBA_D : 0.17mm / 40ohm



INT3 FBA_D : 0.178mm / 40ohm

optical cross point



Top & bottom each layer set 4 points