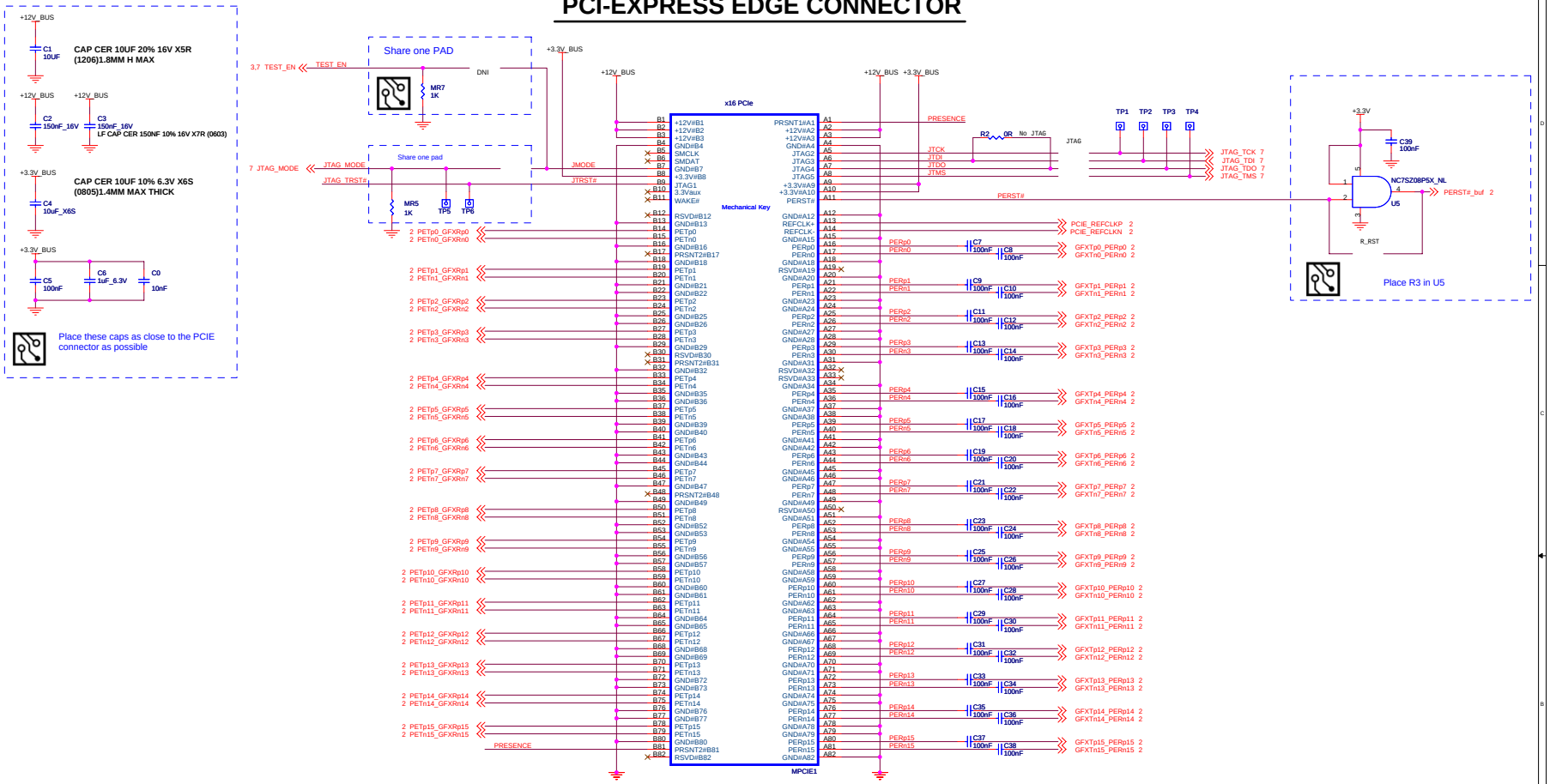
PCI-EXPRESS EDGE CONNECTOR



SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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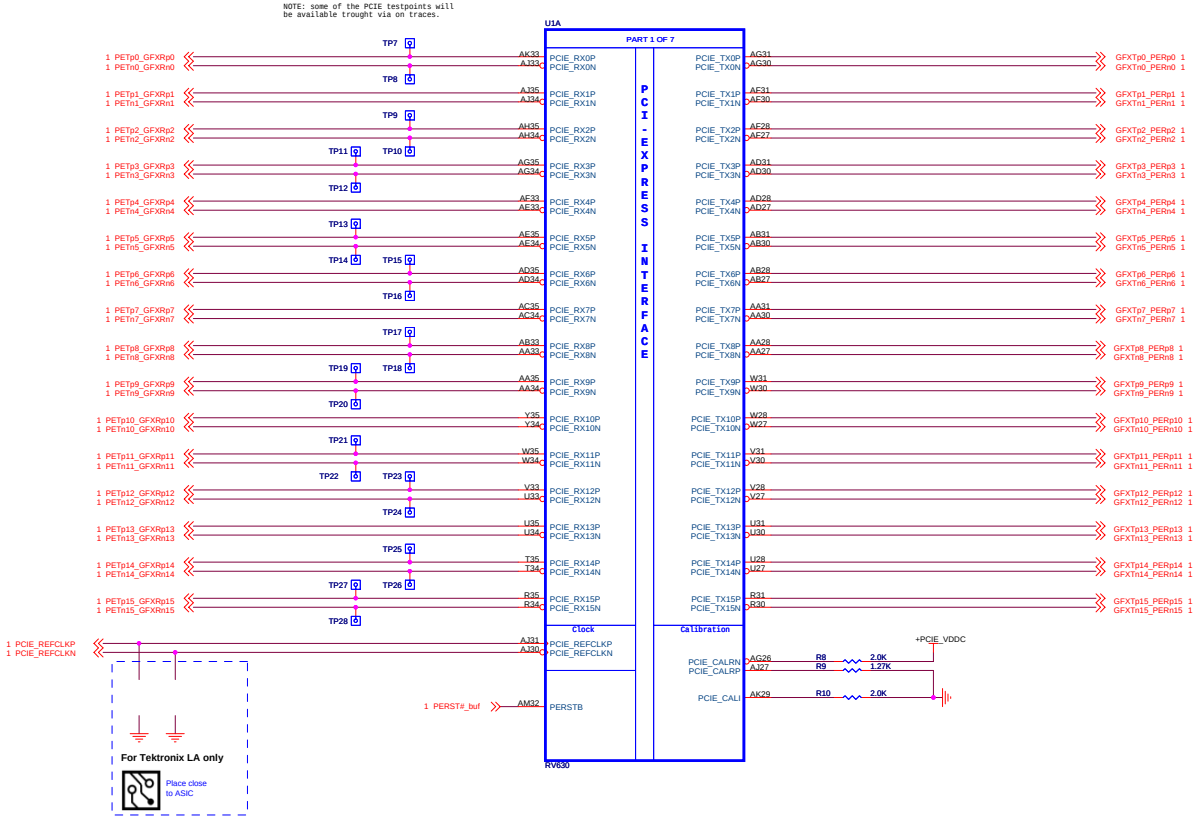

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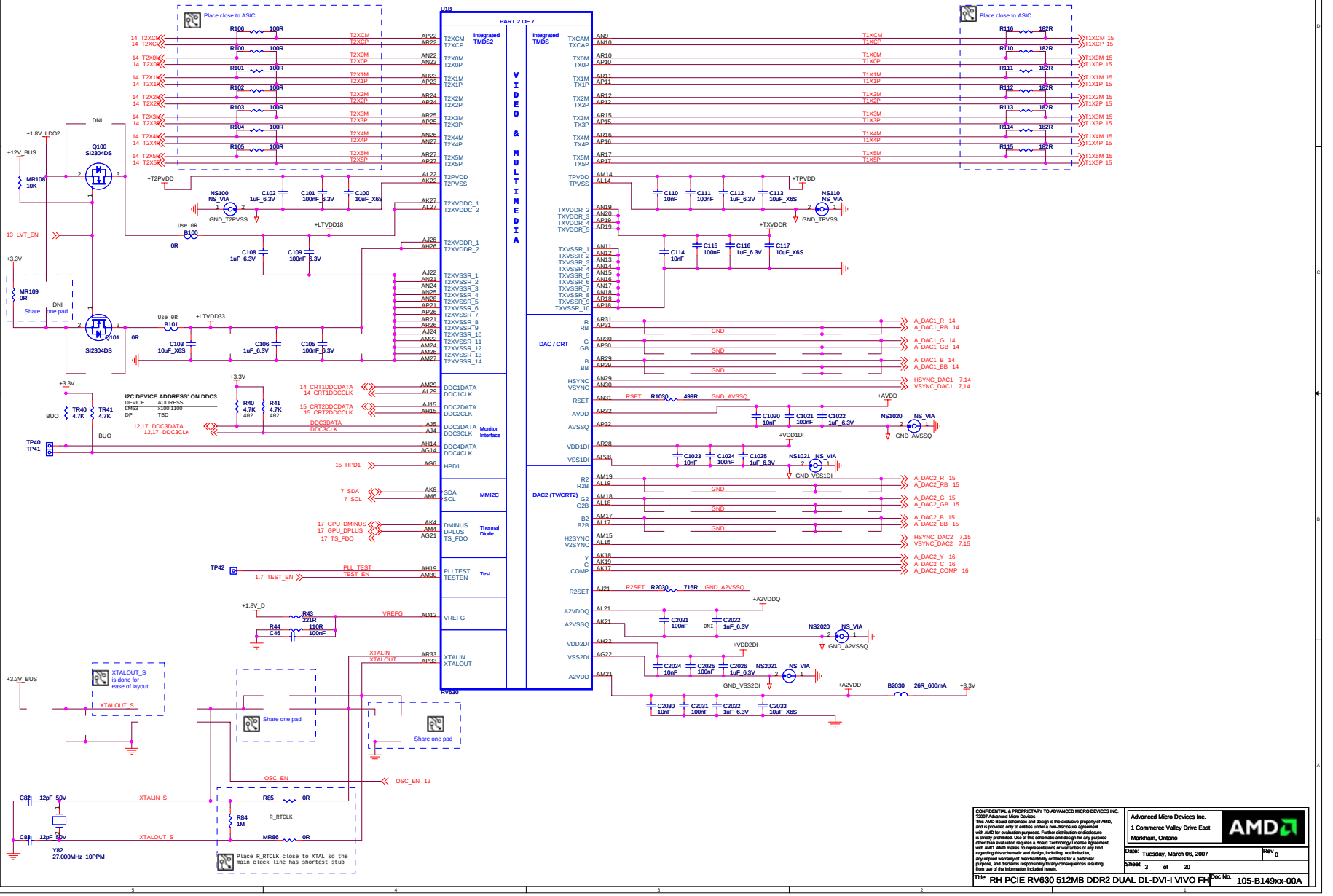
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402



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Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 10%, 0805, 6.3V, 1.4MM MAX THICK
1uF, X6S, 10%, 0402, 6.3V
100nF, X7R, 10%, 0402
10nF , X7R, 10%, 0402

U1E

PART 5 OF 7

POWER

Memory I/O

PCI-Express

Core

Selected PLL's

Mechanical Pins

RV630

+MVDD

+VDDC

+PCIE_PVDD

+PCIE_VDDC

+PCIE_VDDR

+1.8V_D

+3.3V

+DPLL_PVDD

+MPVDD

+VDDCI

GND_VSSRHA

GND_VSSRHB

GND_PCIE_PVSS

GND_PVSS

GND_MPVSS

B930 BLM15BD121SN1

B120 BLM15BD121SN1

B123 BLM15BD121SN1

B920 220R_2A

B77 220R_2A

B67 26R_600mA

MB60 BLM15BD121SN1

R900 0R

NS18_NS_VIA

NS120 NS_VIA

NS123 NS_VIA

NS70_NS_VIA

NS_VIA_NS64

Install only one of these two

Install only one of these two

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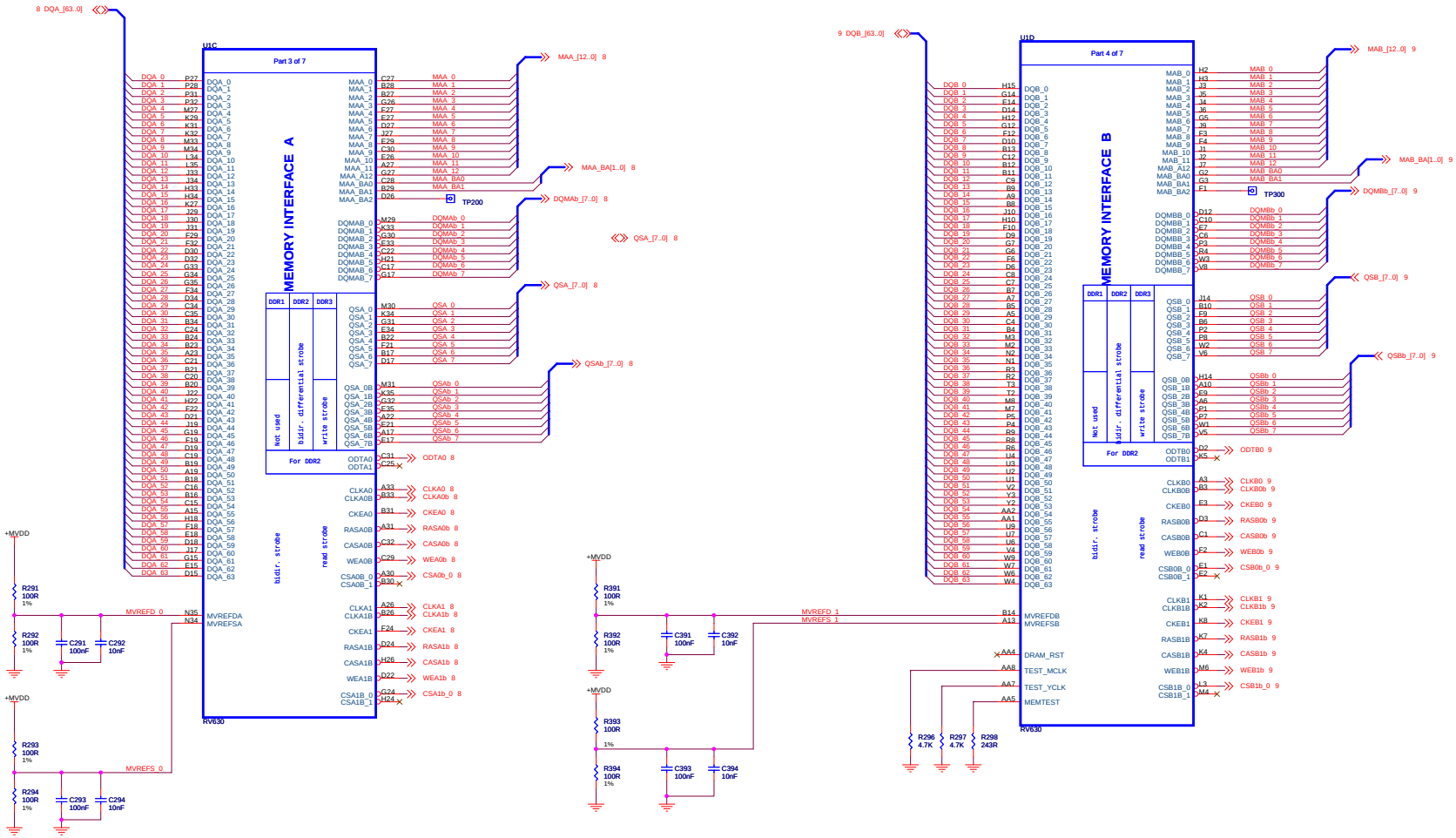

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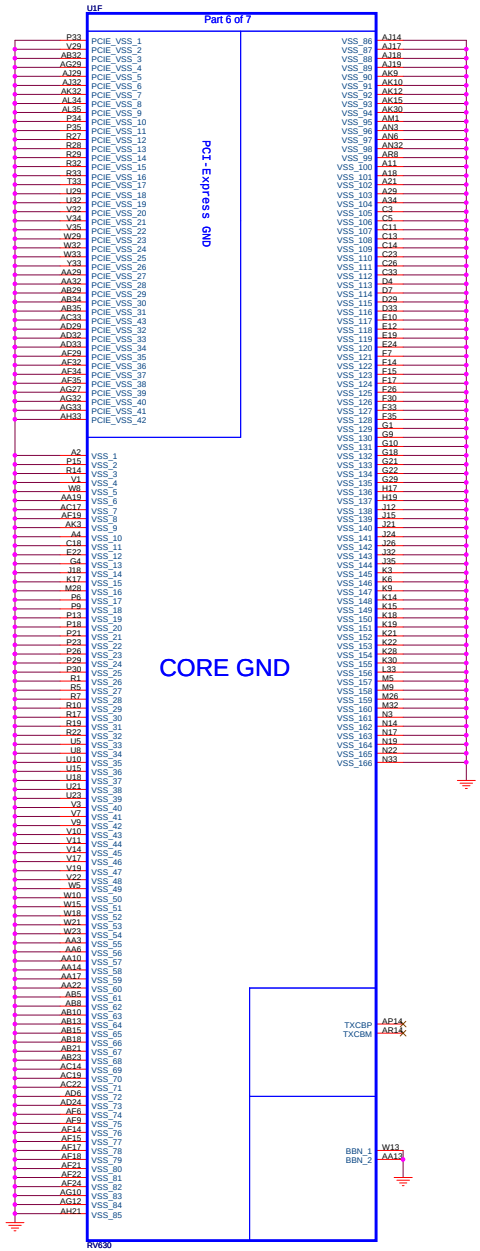

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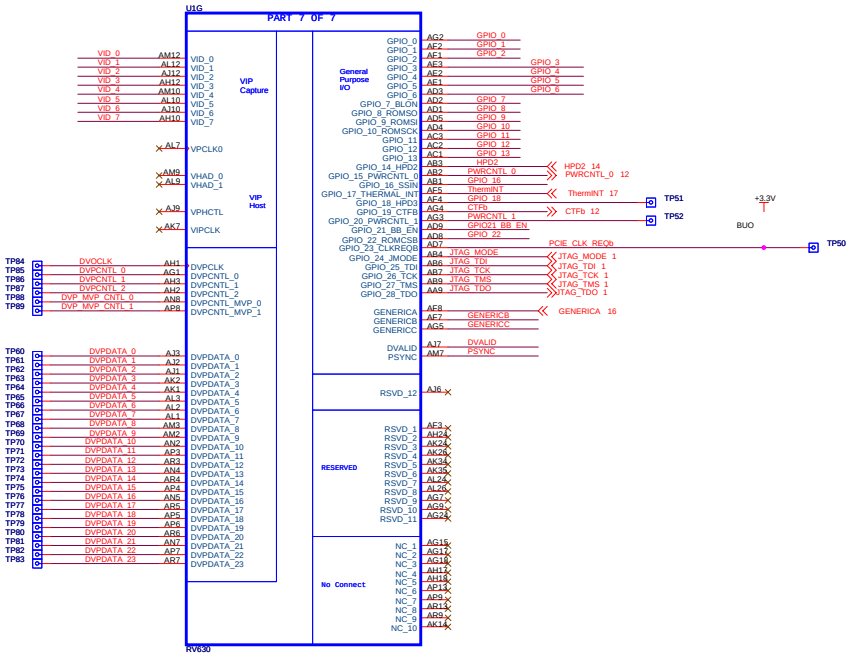
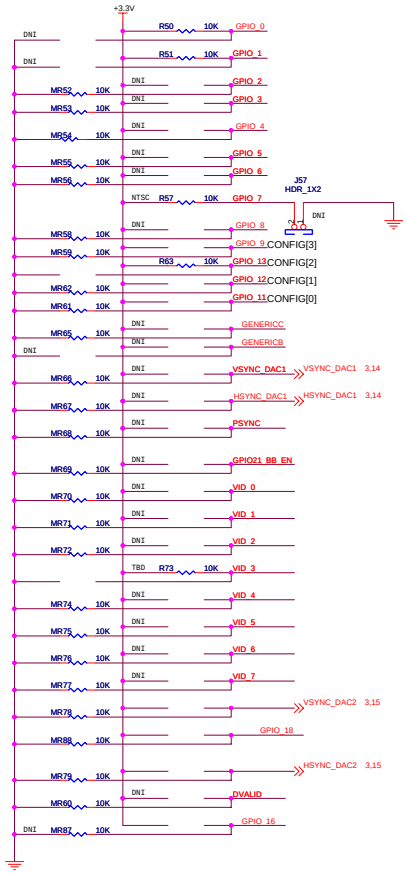


PIN BASED STRAPS



GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) ATI PCIE FEATURE I
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) ATI PCIE FEATURE II
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

ATI Internal Use Only - Reserved (Default: 00)

DEBUG_ACCESS
ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

TV OUT STANDARD (Jumper position overwrite resistor settings)
0 - PAL TVO (Jumper is closed)
1 - NTSC TVO (Jumper is open)

ATI Internal Use Only - Reserved (Default: 0)

GPIO(9,13:11) - CONFIG[3..0]
0010 - 512Kbit AT25F512A (Atmel)
0011 - 1Mbit AT25F1024A (Atmel)
0100 - 512Kbit M25P05A (ST)
0101 - 1Mbit M25P10A (ST)
0101 - 2Mbit M25P20 (ST)
0100 - 512Kbit Pm25LV512 (Chingis)
0101 - 1Mbit Pm25LV010 (Chingis)

ATI Internal Use Only - Reserved (Default: 0)

VIP_DEVICE_STRAP_EN
0: Slave VIP host port devices present (use if Theater is populated)
1: No slave VIP host port devices reporting presence during reset (use for configurations without video-in)

ATI Internal Use Only - Reserved

VGA DISABLE : 1 for disable (set to 0 for normal operation)

ATI Internal Use Only - Reserved (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

MSI_DIS (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

BIF_AUDIO_EN
0 - Disable HD Audio 1- Enable HD Audio

ATI Internal Use Only - Reserved (Default: 0)

64BAR_EN_A (Default: 0)

ATI Internal Use Only - Reserved (Default: 0)

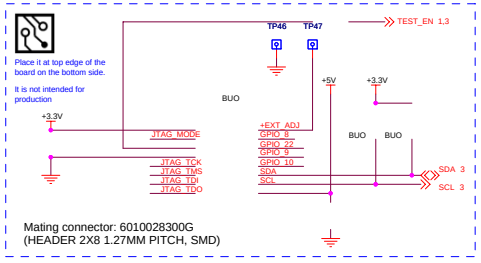
ATI Internal Use Only - Reserved (Default: 0)

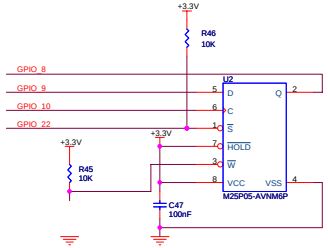
MEMORY CONFIG ATI Board Feature I

VSYNC_DAC2	CHECK ATI MEMORY
GPIO18	TUNING DOCUMENT

BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

Pull-Down Resistors are for BU until built-in pull-downs are verified.





BIOS1
BIOS
113-B149XX-XXX
VIDEO BIOS FIRMWARE

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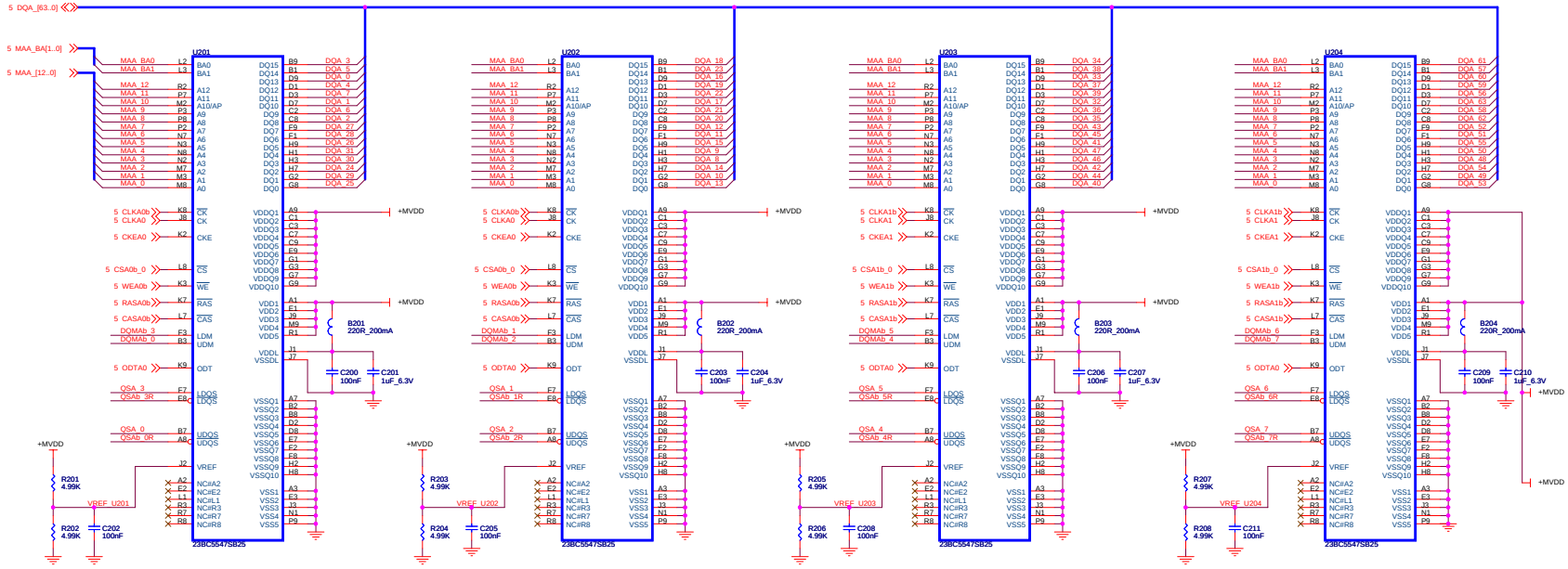
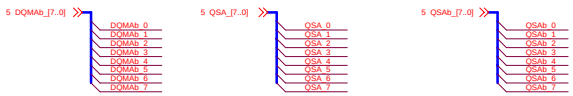
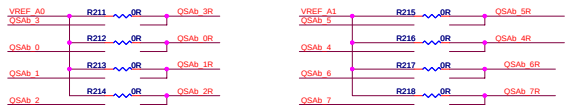
CHANNEL A: 128MB/256MB DDR2

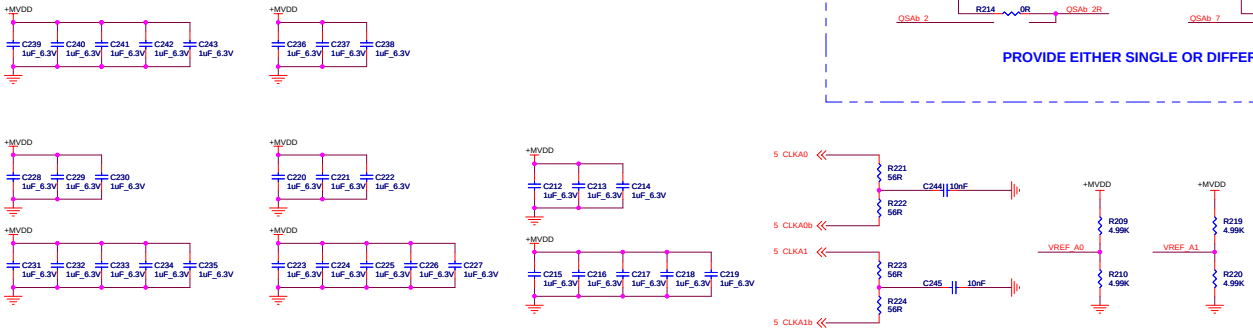




DUAL FOOT PRINT FOR R AND MR** DESTINATION**
MAINTAIN THE DIFFERENTIAL FOR EACH PAIR.



PROVIDE EITHER SINGLE OR DIFFERENTIAL DQS FOR EACH BYTE



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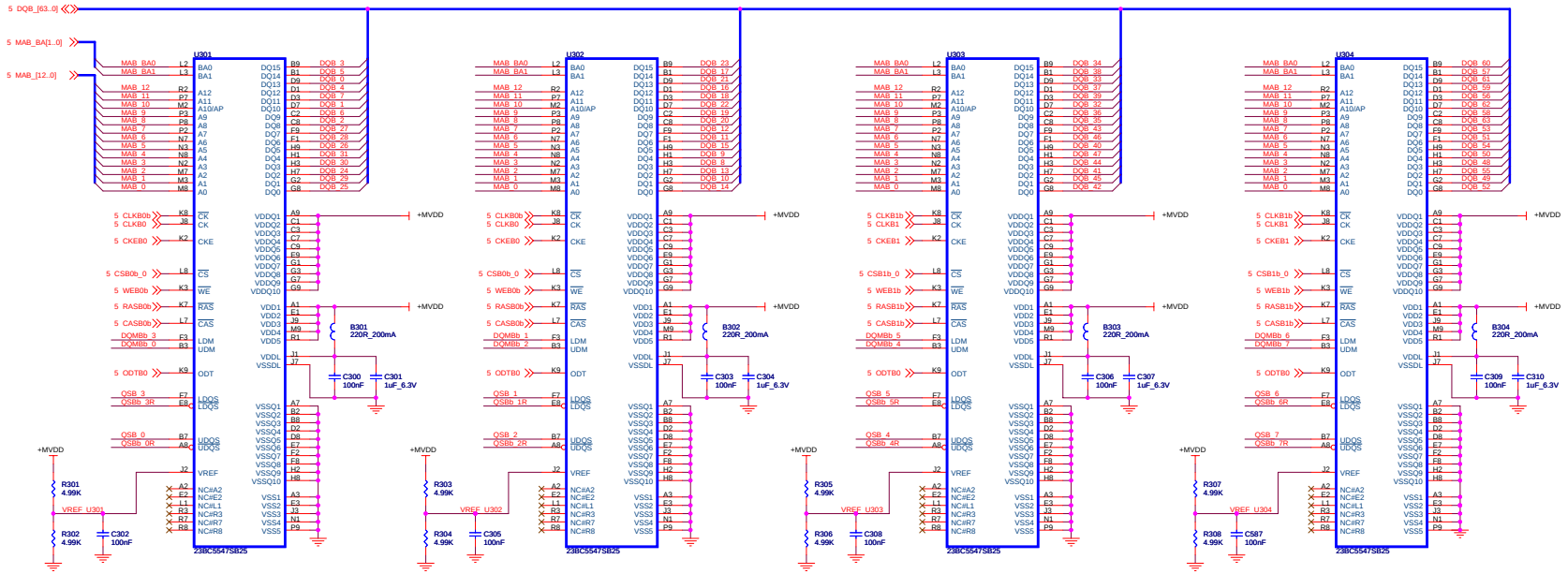
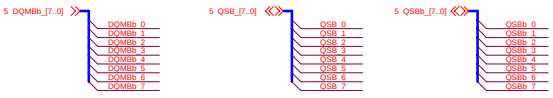
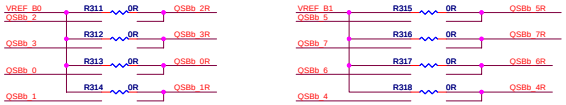
CHANNEL B: 128MB/256MB DDR2

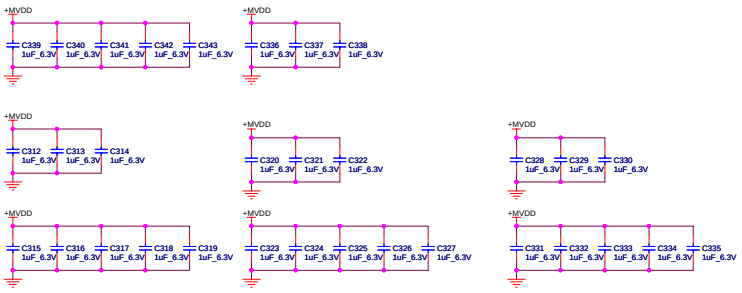


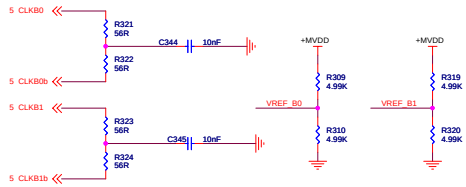


DUAL FOOT PRINT FOR R AND MR** DESTINATION**
MAINTAIN THE DIFFERENTIAL FOR EACH PAIR.



PROVIDE EITHER SINGLE OR DIFFERENTIAL DQS FOR EACH BYTE





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Information on Compatable Controller Parts

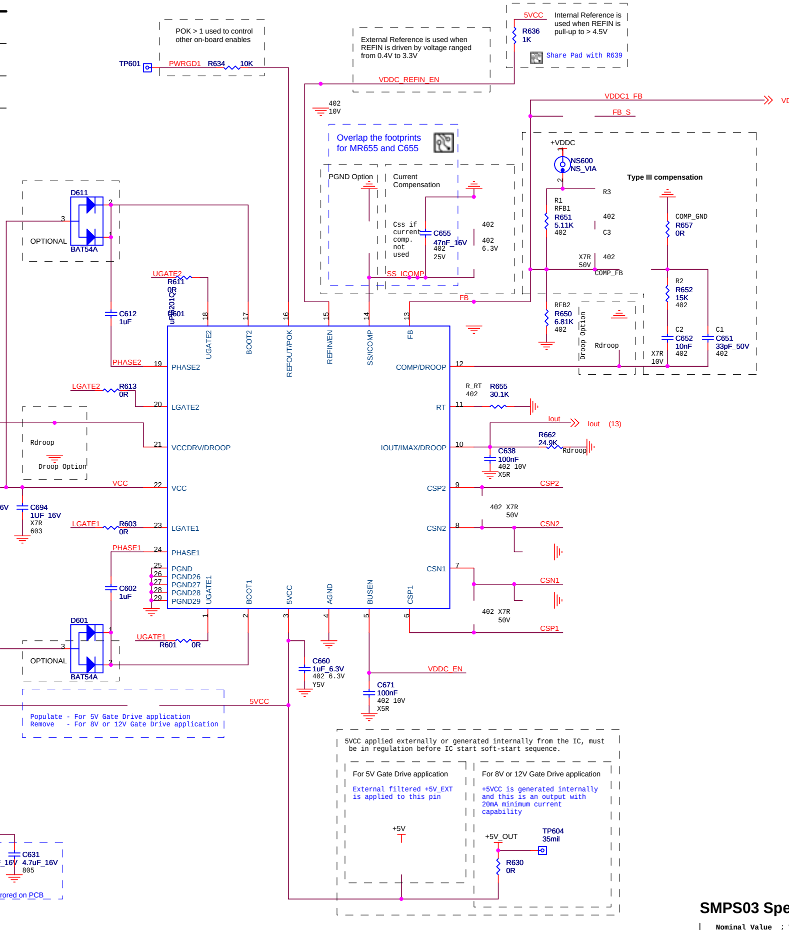
	PWM IC #1	PWM IC #2	PWM IC #3	PWM IC #4
Gate drive voltage	5V, 8V, 12V	5V, 8V, 12V	5V only	12V only
Vref	0.6V	0.6V	0.6V	0.6V
Bootstrap diodes	Internal (DNP D601, D611)	Internal (DNP D601, D611)	External (Populate D601, D611)	Internal (DNP D601, D611)
Phase current adjustable (unbalanced between phases)	Yes	Yes	Yes	TBD
Option Pin Selection				
Pin 10 (IOUT/IMAX/DROOP)	IOUT/DROOP (R662)	IOUT/IMAX	IOUT	IOUT/IMAX
Pin 11 (RT)	R_RT ~= 10,000,000/Fsw	TBD	R_RT ~= 18,600,000/Fsw	TBD
Pin 12 (COMP/DROOP)	COMP	DROOP (R663)	COMP	COMP
Pin 14 (SS/ICOMP)	SS/EN	GND (SS fixed internally)	ICOMP (SS dependent on Fsw)	SS
Pin 16 (REFOUT/POK)	POK (Open drain)	IREFOUT/POK POK voltage = 1.2V	INREFOUT/POK PGood voltage = 1.25V	INREFOUT/PGOOD Vrefout = 0.6V
Pin 21 (VCCDRV/DROOP)	VCCDRV	VCCDRV	DROOP (R664)	DROOP (R664)

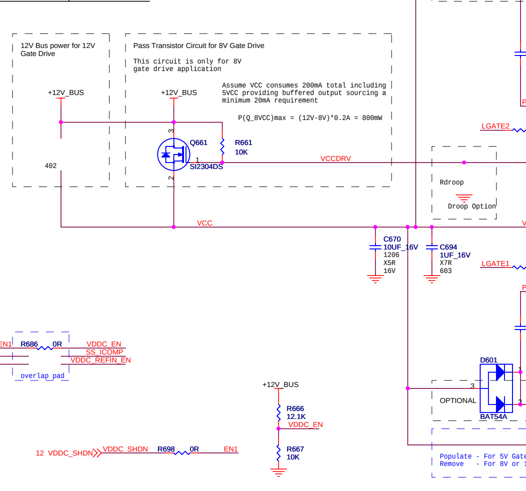
Choosing Different Gate Drive

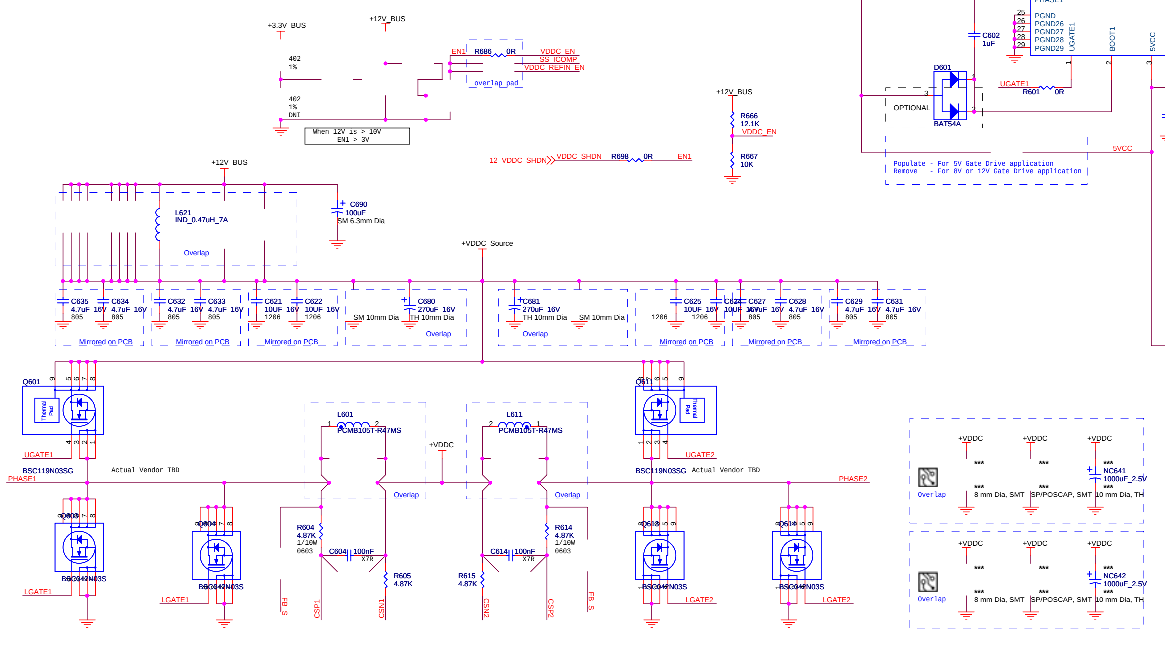
Gate Drive	Populate	Do Not Populate
5V Gate Drive	R631, R632	R630, R670, C660, R661, Q661
8V Gate Drive	R630, C660, R661, Q661	R631, R632, R670
12V Gate Drive	R630, C660, R670	R631, R632, R661, Q661

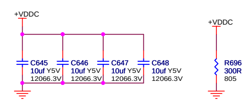
External Detection Circuit and Indication

Cases	Behaviour	Notifications
External cable not plugged in +12V_BUS not in regulation	12V_EXT_DETb = X EN1 -> "0" (by Ri2) ENb1 -> 3.3V ENBUS = "0"	VDDC disabled
External cable not plugged in +12V_BUS in regulation	12V_EXT_DETb = "1" EN1 -> 3V (by Ri1 and Ri2) ENb1 = 0V ENBUS = "1"	VDDC enabled External Power Missing
External cable plugged in +12V_XXX not in regulation	12V_EXT_DETb = "0" EN1 < 3V (due to low 12V) ENb1 = 3.3V ENBUS = "0"	VDDC disabled
External cable plugged in +12V_XXX in regulation	12V_EXT_DETb = "0" EN1 -> 3V ENb1 = 0V ENBUS = "1"	VDDC enabled Normal Operation









SMPS03 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	1.2V ; +2.5%/-2.5%	0.8V ~ 1.5V
Vout ripple (DC)	TBD	
Iout	TBD	55A (target 60A) max
Step load	TBD	
Vout ripple (AC)	TBD	
Switching Freq.	TBD	50kHz ~ 1MHz
Protections		

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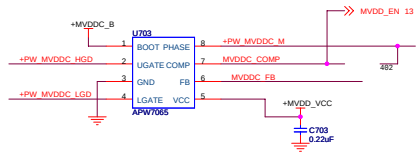
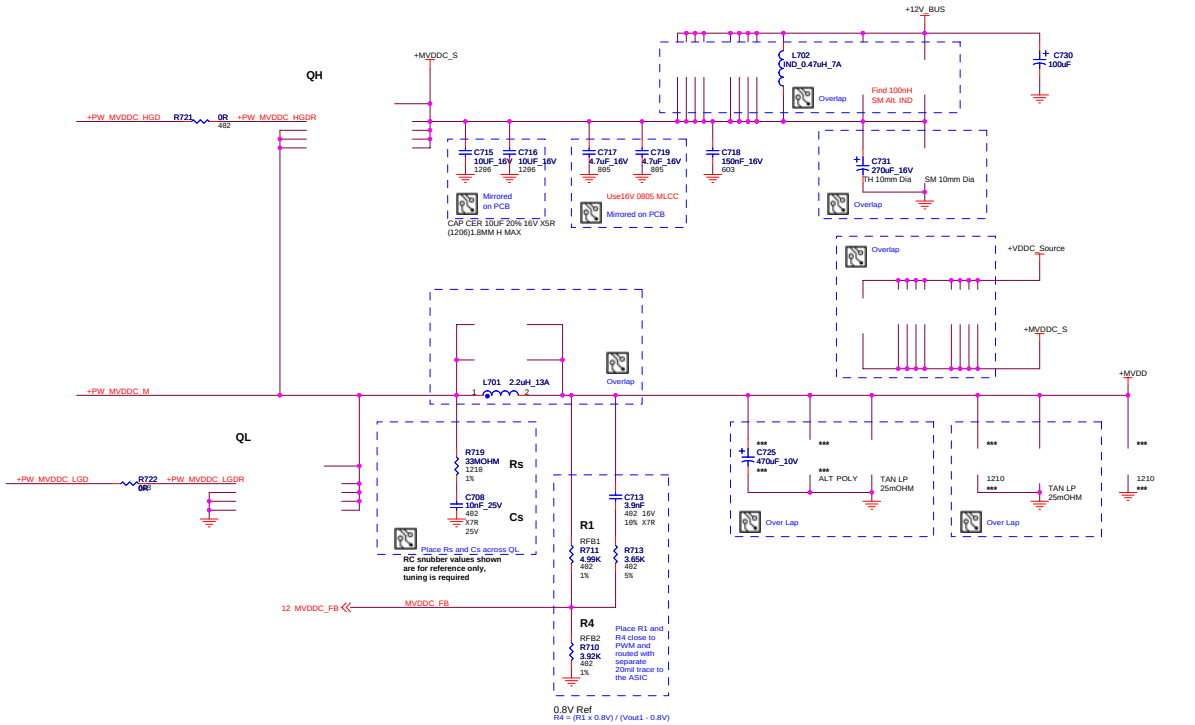
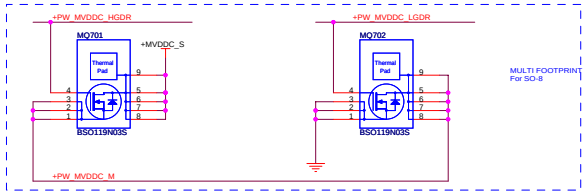


List of supported foodprint

The following ICs are not necessarily evaluated by ATI, please refer to BOM for evaluation status

- **ANPEC APW7120/APW7065 (12V)**
- **CAT CAT7583 (12V)**
- **INTERSIL ISL6545**
- **NEXSEM NX2114/2307**
- **RICHTEK RT9214/RT8101**
- **OnSemi ON1582**
- **uPI UP6101 (No Ext_Vref in)**
- **uPI UP6103 (with Ext_Vref in, can use voltage console UP6261 to change Vout)**





SMPS02- Regulator for MVDD

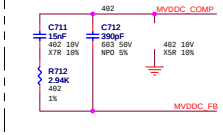
Vout = 1.8V ~ 2.85V

Part	Vout	RFB1	RFB2
0.8V Ref	2.03V (1.98V~2.08V)	4.99K p/n 3160499100G	3.24K p/n 3160324100G

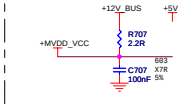
SMPS02 Specifications

	Nominal Value ; Tolerance	Adjustable range / Notes
Vin (power stage)	12V ; +/-8% PCIe	ATX12V ver. 2.2 +/-5%
Vout	2V ; +2%/-2%	1.8V ~ 2.85V
Vout ripple (DC)	50mVpp	
Iout	6Aavg, 8Adc_max	
Step load	3Amax	
Vout ripple (AC)	+/-10% or 200mVpp @ 3A step load	
Switching Freq.	~300kHz	TBD
Protections		

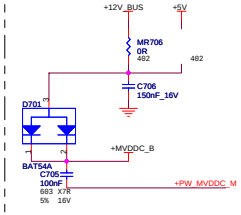
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



Layout guideline for Nexsem NX2114/2307

1-Position the controller (U703) such that LGate(pin4) is the closet to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces(PW MVDDC LGD and PW MVDDC HGD) as short and as wide as possible to reduce the trace inductance.
2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows;
Vcc bypass cap is C703, and Boost cap is C705.
3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.

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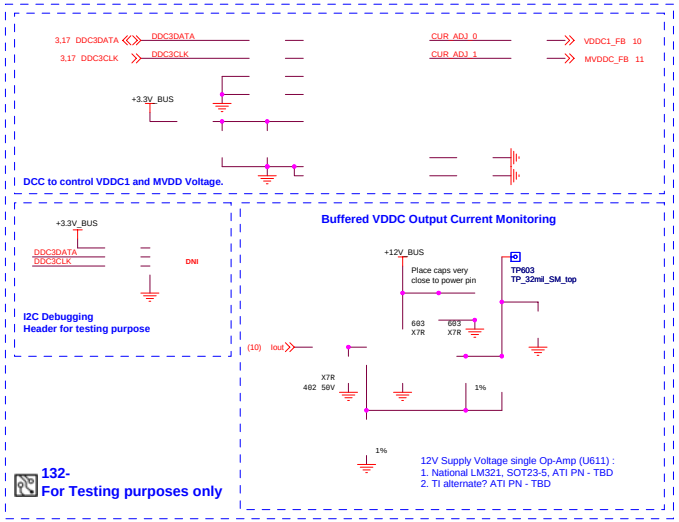
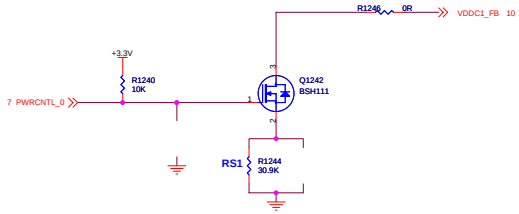
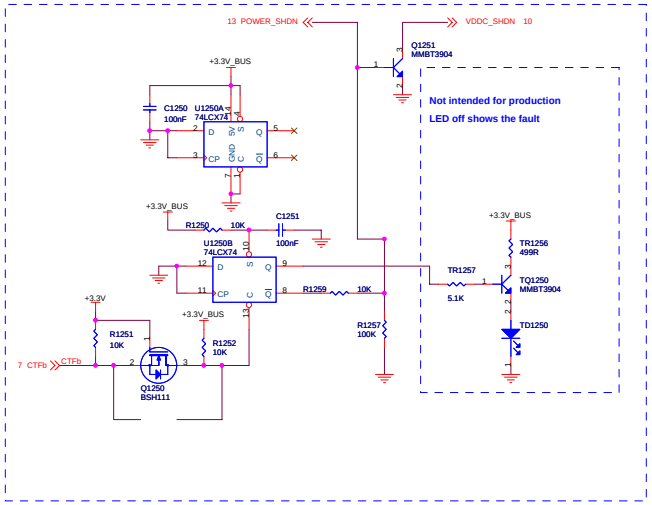




SMPS03- Regulator for VDDC

Vout = .9V ~ 1.2V

	VDDC	RS1	PWRCNTL_0
0.6V Ref	.9V	N/A	LOW
	1.0V	59.0K 1% ATI # 3160590200G	HIGH
	1.1V	30.9K 1% ATI # 3160309200G	HIGH
	1.2V	20.0K 1% ATI # 3160200200G	HIGH



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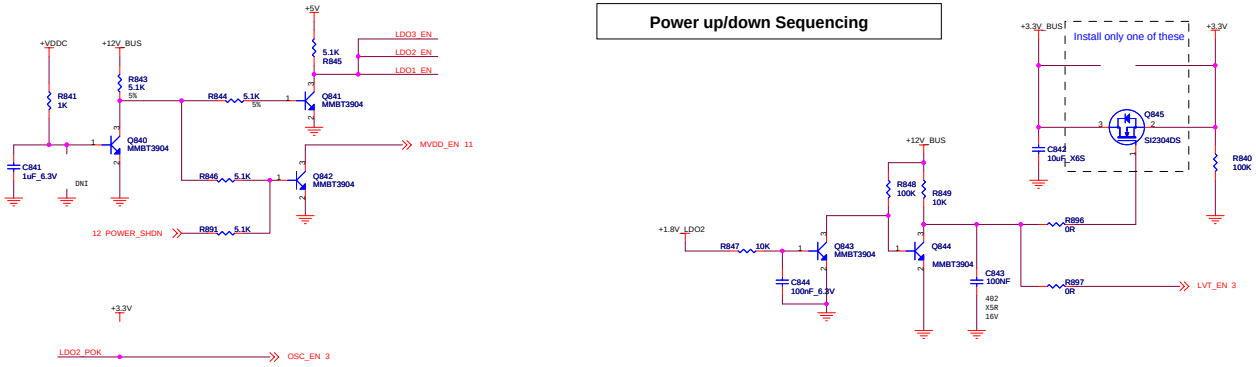
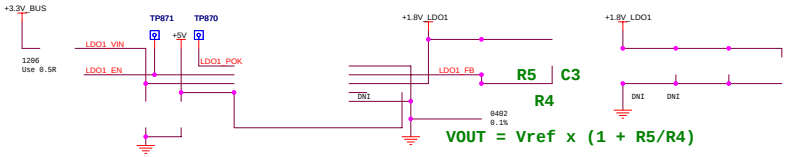
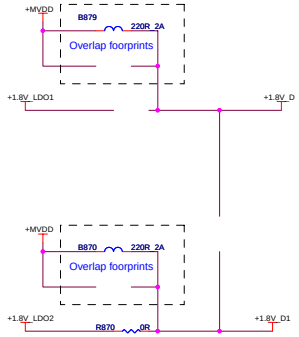
Power up/down Sequencing

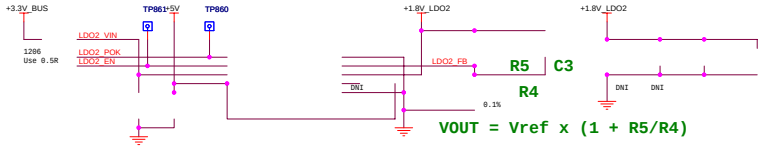


LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

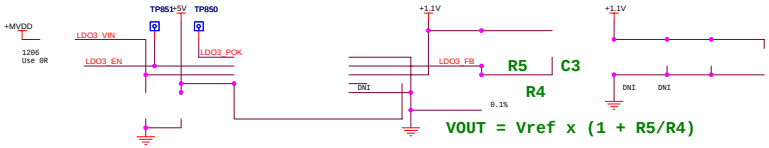




LDO #2: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 0.8A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

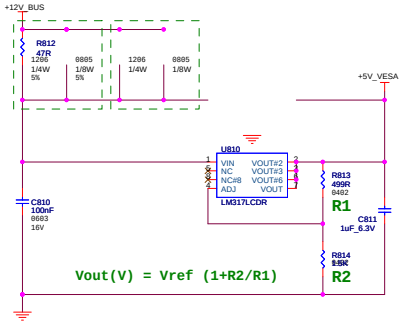


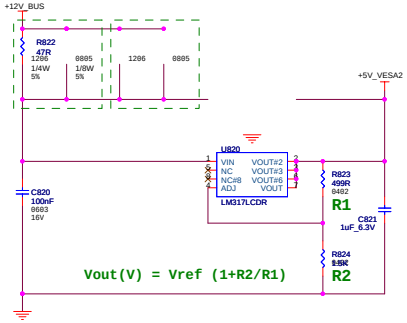
LDO #3: Vin = +1.45V to 2.1VMAX Vout = +1.1V +/- 2% Iout = 1.1A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling

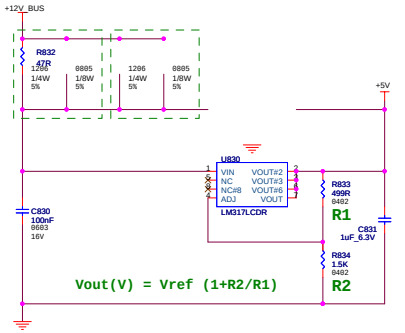


Shared Power Rails

Regulators for +5V, +5V_VESA and +5V_VESA2







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See BOM for qualified filters

3 A_DAC1_R — R1001 75R — L1001 47nH — A_R_DAC1_M — L1004 0R
3 A_DAC1_RB — R1027 37.4R
3 A_DAC1_G — R1002 75R — L1002 47nH — A_G_DAC1_M — L1005 0R
3 A_DAC1_GB — R1028 37.4R
3 A_DAC1_B — R1003 75R — L1003 47nH — A_B_DAC1_M — L1006 0R
3 A_DAC1_BB — R1029 37.4R

Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.

For ESD Protection

+3.3V, +5V_VESA

A_R_DAC1_F
A_G_DAC1_F
A_B_DAC1_F
DDCDATA_DAC1_R
DDCCLK_DAC1_R
HSYNC_DAC1_R
VSYNC_DAC1_R

+5V_VESA

DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)

603

3 CRT1DDCDATA — +3.3V — R1004 10K — +5V — R1005 4.7K — Q1001 BSH111 — DDCDATA_DAC1_5V — R1006 33R — DDCDATA_DAC1_R

3 CRT1DDCCLK — +3.3V — R1007 10K — +5V — R1008 2.2K — Q1002 BSH111 — DDCCLK_DAC1_5V — R1009 33R — DDCCLK_DAC1_R

C1999 100nF — +5V — 74VHC125 U1999A

3,7 HSYNC_DAC1 — HSYNC_DAC1_B — R1010 10R — HSYNC_DAC1_R

U1999B

3,7 VSYNC_DAC1 — VSYNC_DAC1_B — R1011 10R — VSYNC_DAC1_R

74VHC125

SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
	Mechanical Key	1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

7 HPD2 — Q1021 MMBT3904 — +3.3V — R1022 10K — R1023 10K — HPD_DVI2

+5V_VESA

J1001

3 T2X2M	1	TMDS Data2-
3 T2X2P	2	TMDS Data2+
	3	TMDS Data2/4 Shield
3 T2X4M	4	TMDS Data4-
3 T2X4P	5	TMDS Data4+
DDCCLK_DAC1_R	6	DDC Clock
DDCDATA_DAC1_R	7	DDC Data
VSYNC_DAC1_R	8	Analog VSYNC
3 T2X1M	9	TMDS Data1-
3 T2X1P	10	TMDS Data1+
	11	TMDS Data1/3 Shield
3 T2X3M	12	TMDS Data3-
3 T2X3P	13	TMDS Data3+
	14	+5V Power
	15	GND (for +5V)
HPD_DVI2	16	Hot Plug Detect
3 T2X0M	17	TMDS Data0-
3 T2X0P	18	TMDS Data0+
	19	TMDS Data0/5 Shield
3 T2X5M	20	TMDS Data5-
3 T2X5P	21	TMDS Data5+
	22	TMDS Clock Shield
3 T2XCP	23	TMDS Clock+
3 T2XCM	24	TMDS Clock-
A_R_DAC1_F	C1	Analog Red
A_G_DAC1_F	C2	Analog Green
A_B_DAC1_F	C3	Analog Blue
HSYNC_DAC1_R	C4	Analog HYNC
	C5	Analog GND
	C6	Analog GND#C6
	26	CASE#26
	27	CASE#27
	28	CASE#28
	29	CASE#29
	30	CASE#30

DVI_CONNECTOR

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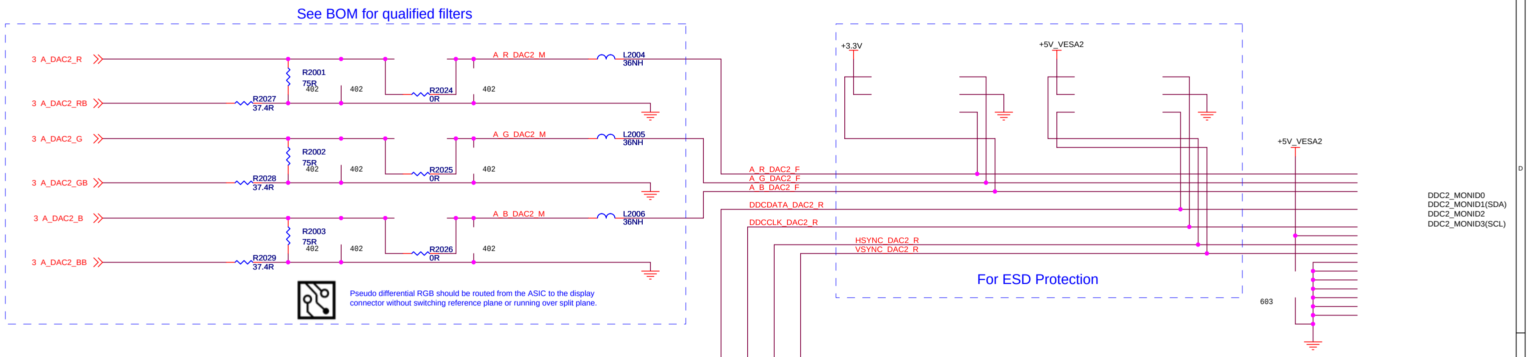
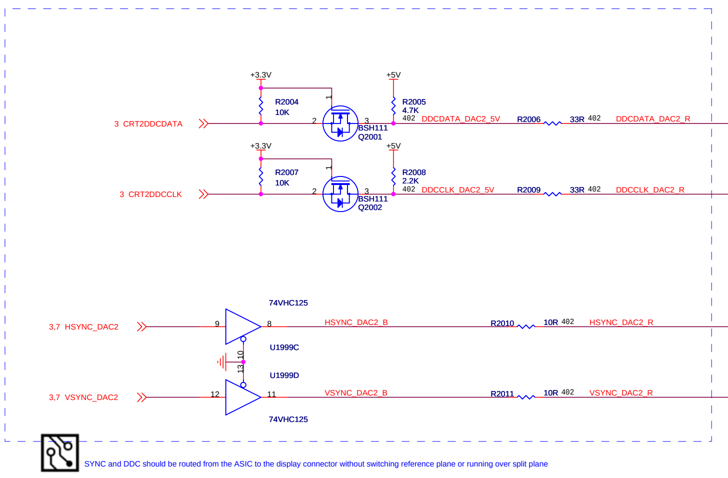
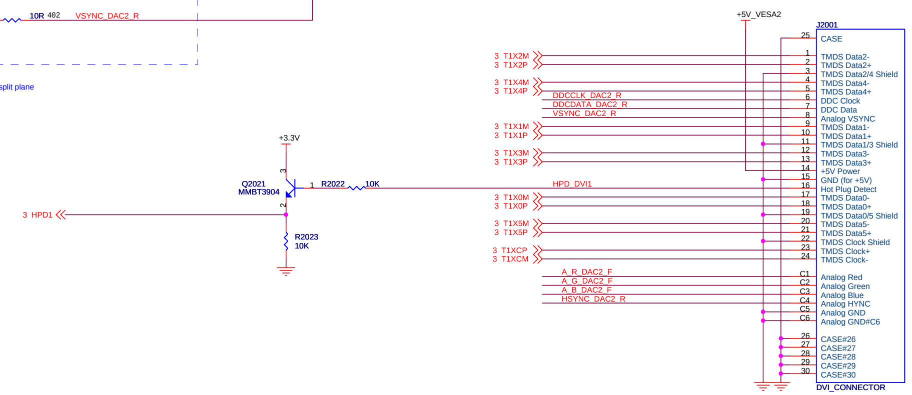

See BOM for qualified filters
3 A_DAC2_R
3 A_DAC2_RB
3 A_DAC2_G
3 A_DAC2_GB
3 A_DAC2_B
3 A_DAC2_BB
R2001 75R
R2002 75R
R2003 75R
R2027 37.4R
R2028 37.4R
R2029 37.4R
R2024 0R
R2025 0R
R2026 0R
A_R_DAC2_M
A_G_DAC2_M
A_B_DAC2_M
L2004 36NH
L2005 36NH
L2006 36NH
Pseudo differential RGB should be routed from the ASIC to the display connector without switching reference plane or running over split plane.
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
DDCDATA_DAC2_R
DDCCLK_DAC2_R
HSYNC_DAC2_R
VSYNC_DAC2_R
+3.3V
+5V_VESA2
For ESD Protection
603
DDC2_MONID0
DDC2_MONID1(SDA)
DDC2_MONID2
DDC2_MONID3(SCL)


+3.3V
+5V
R2004 10K
R2005 4.7K
3 CRT2DDCDATA
BSH111 Q2001
DDCDATA_DAC2_5V
R2006 33R
DDCDATA_DAC2_R
R2007 10K
R2008 2.2K
3 CRT2DDCCLK
BSH111 Q2002
DDCCLK_DAC2_5V
R2009 33R
DDCCLK_DAC2_R
74VHC125
3,7 HSYNC_DAC2
HSYNC_DAC2_B
R2010 10R
HSYNC_DAC2_R
U1999C
U1999D
3,7 VSYNC_DAC2
VSYNC_DAC2_B
R2011 10R
VSYNC_DAC2_R
SYNC and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane


+3.3V
Q2021 MMBT3904
R2022 10K
HPD_DVI1
3 HPD1
R2023 10K
+5V_VESA2
J2001
3 T1X2M
3 T1X2P
3 T1X4M
3 T1X4P
DDCCLK_DAC2_R
DDCDATA_DAC2_R
VSYNC_DAC2_R
3 T1X1M
3 T1X1P
3 T1X3M
3 T1X3P
3 T1X0M
3 T1X0P
3 T1X5M
3 T1X5P
3 T1XCP
3 T1XCM
A_R_DAC2_F
A_G_DAC2_F
A_B_DAC2_F
HSYNC_DAC2_R
CASE
TMDS Data2-
TMDS Data2+
TMDS Data2/4 Shield
TMDS Data4-
TMDS Data4+
DDC Clock
DDC Data
Analog VSYNC
TMDS Data1-
TMDS Data1+
TMDS Data1/3 Shield
TMDS Data3-
TMDS Data3+
+5V Power
GND (for +5V)
Hot Plug Detect
TMDS Data0-
TMDS Data0+
TMDS Data0/5 Shield
TMDS Data5-
TMDS Data5+
TMDS Clock Shield
TMDS Clock+
TMDS Clock-
Analog Red
Analog Green
Analog Blue
Analog HYNC
Analog GND
Analog GND#C6
CASE#26
CASE#27
CASE#28
CASE#29
CASE#30
DVI_CONNECTOR

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C Mechanical Key	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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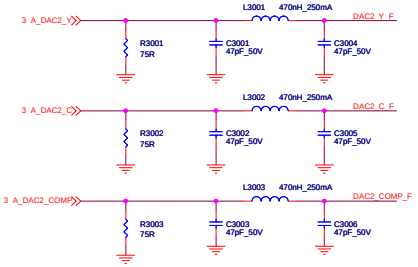
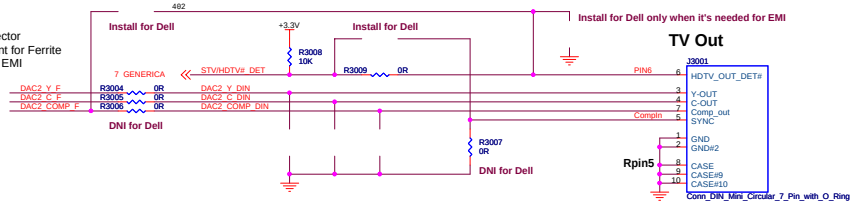


Place near connector
0R leaves footprint for Ferrite Beads if req'd for EMI



The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G

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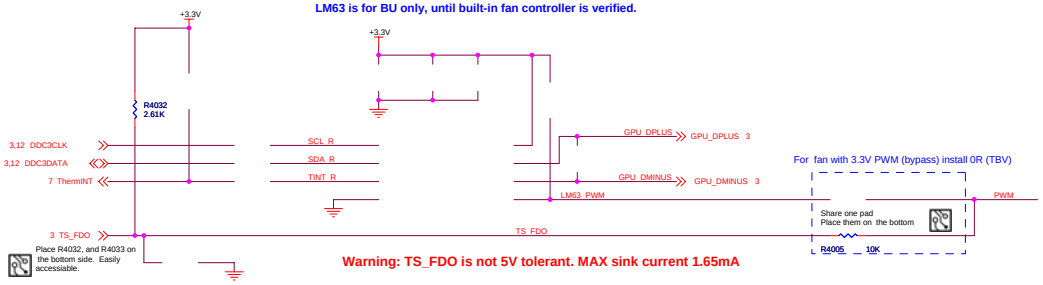
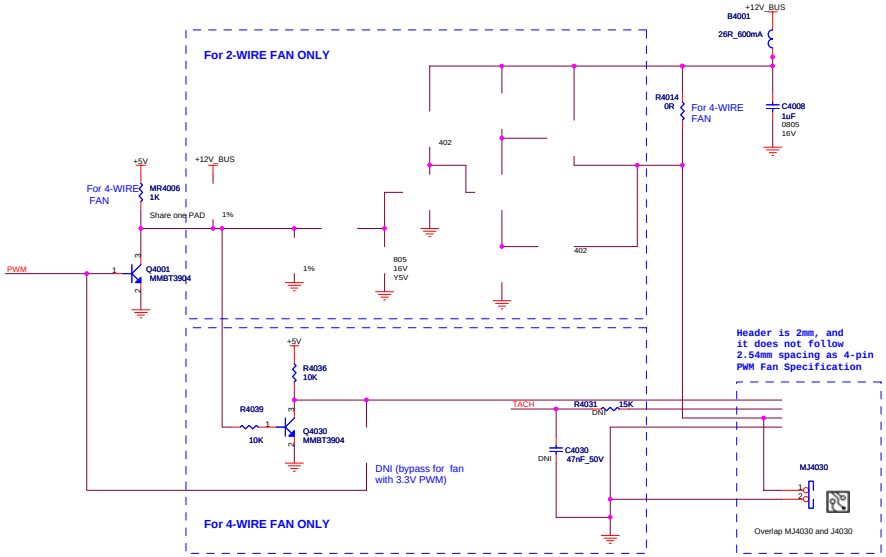
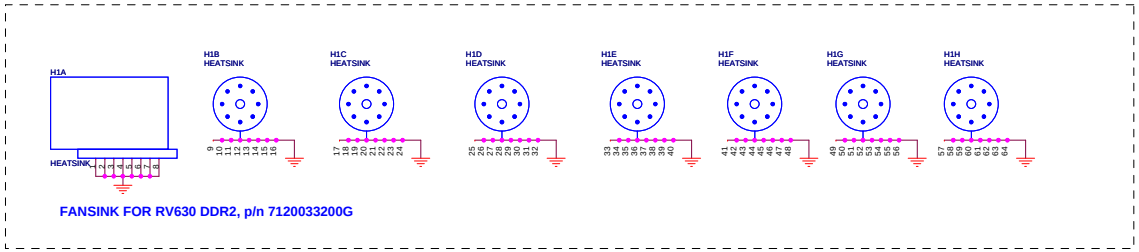
LM63 is for BU only, until built-in fan controller is verified.



Warning: TS_FDO is not 5V tolerant. MAX sink current 1.65mA





FANSINK FOR RV630 DDR2, p/n 7120033200G

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DVI/DVI SCREWS with top tab

ASSY-SCREW2

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW1

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3

SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY1

ANTISTATIC
BAG

6_X_11

ASSY2

BRACKET

8020038600G

MT1
MT_Hole_0.136_in.

MT2
MT_Hole_0.136_in_6VIA

PCB1

PCB

109-B14931-00A

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<Variant Name>

Title	Schematic No.	Date:
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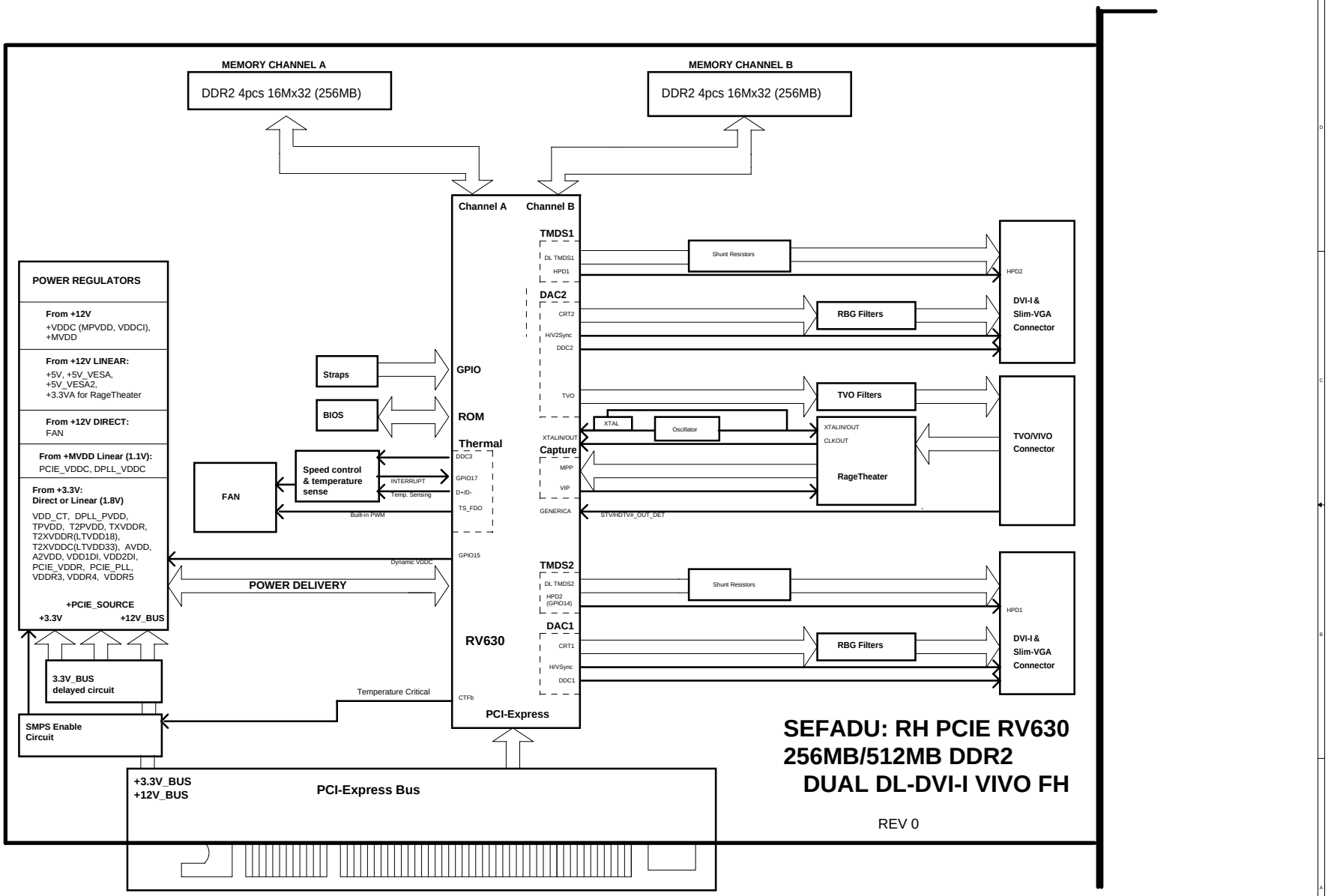
REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	06/11/17	Initial design for RV630 DDR2



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Title	RH PCIE RV630 512MB DDR2 DUAL DL-DVI-I VIVO FH
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