

PG150-C03

384b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

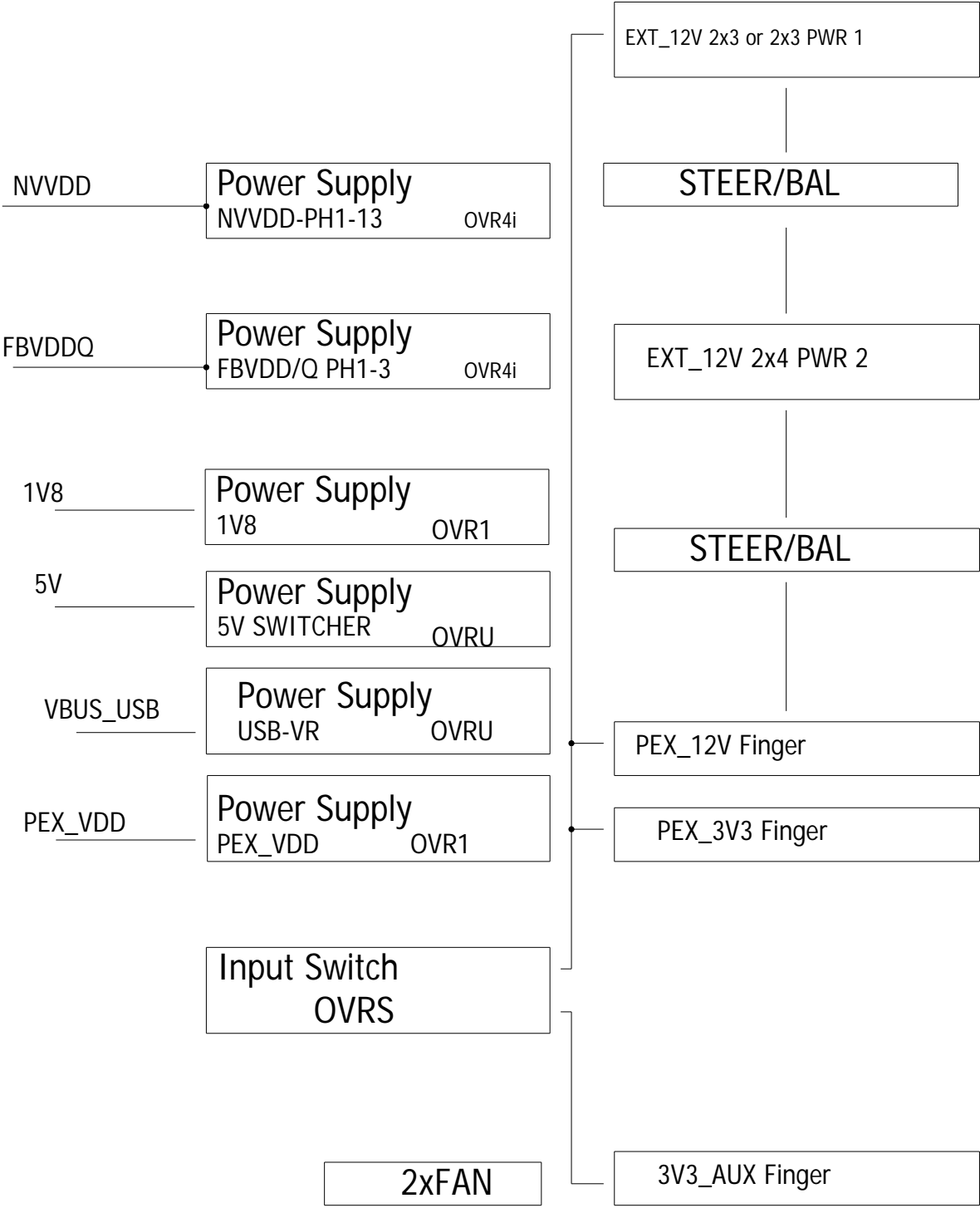
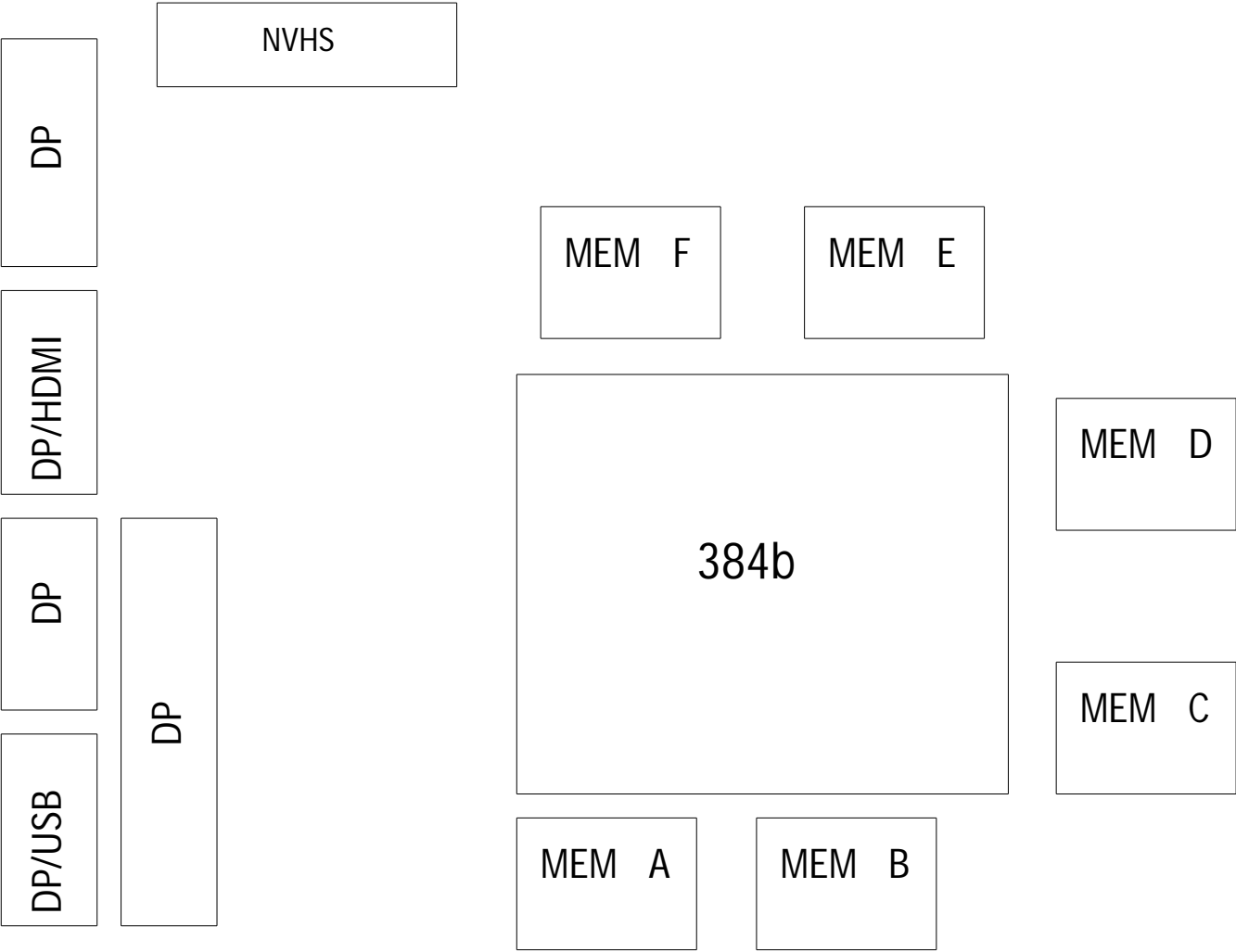
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Block Diagram

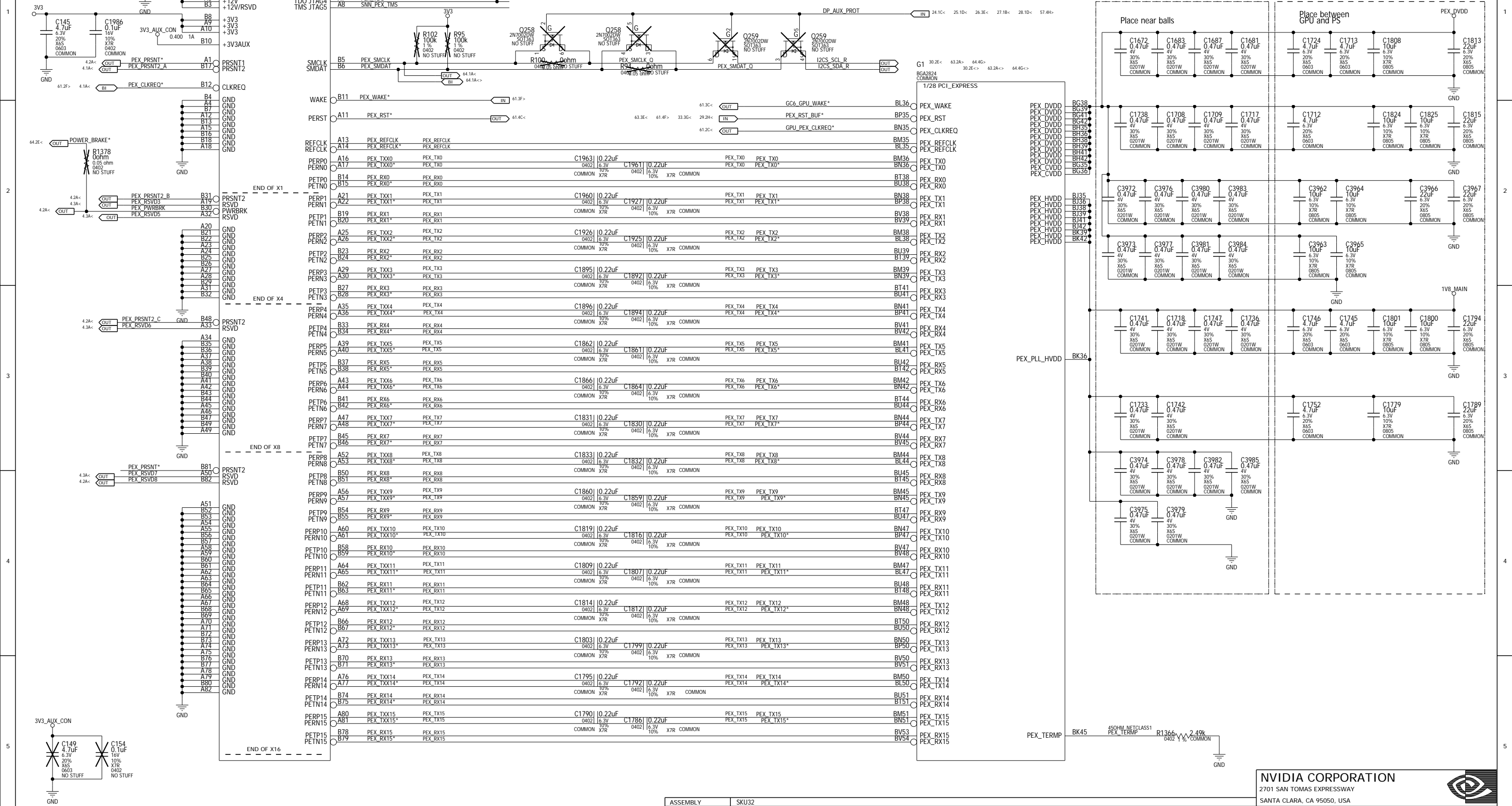


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ASSEMBLY	SKU32
PAGE DETAIL	BLOCK DIAGRAM

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20% X6S 0805LP COMMON	10% X6S 0603 COMMON
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	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
3V3	3V3 NV_SOURCE_POWER_NET		3.0A	0.400
	GND NV_SOURCE_POWER_NET		8.5A	0.400

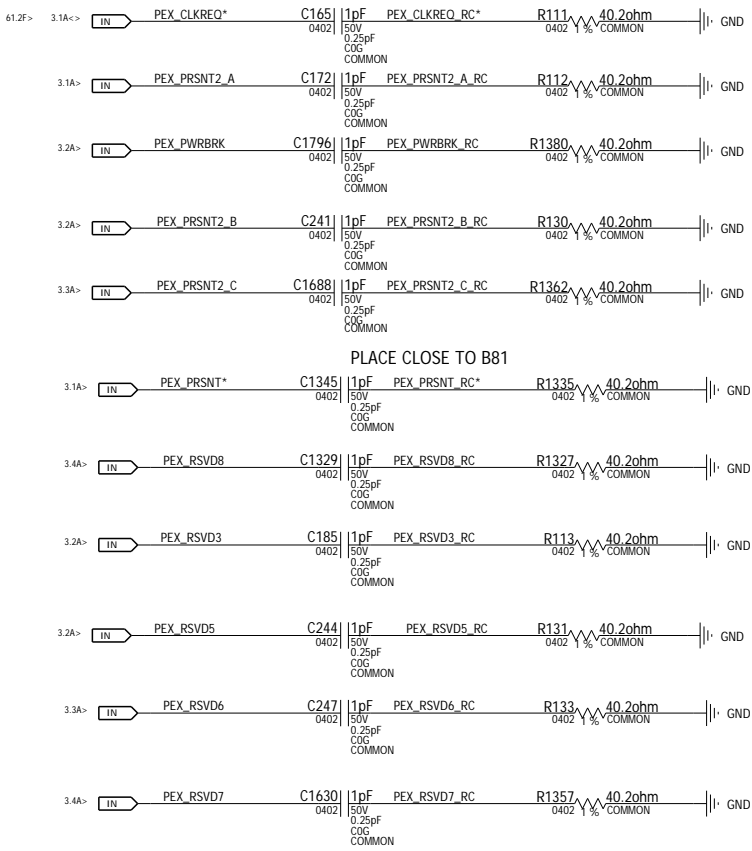
ASSEMBLY	SKU32
PAGE DETAIL	PCI EXPRESS

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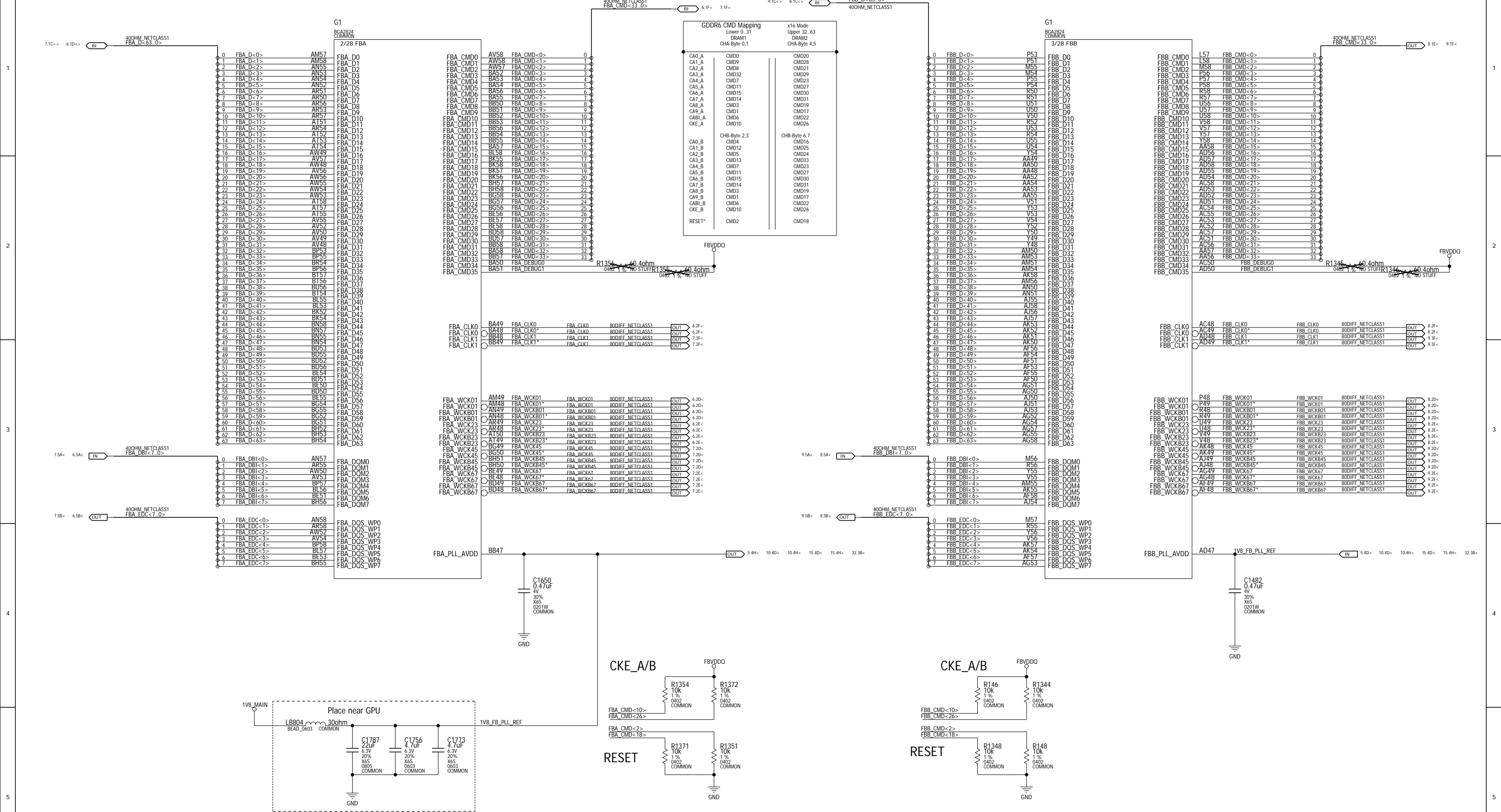


PCI TERM



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MEMORY: GPU Partition A/B



MEMORY: FBA Partition 31..0



Place DRAM on TOP with PIN A1 Away from GPU

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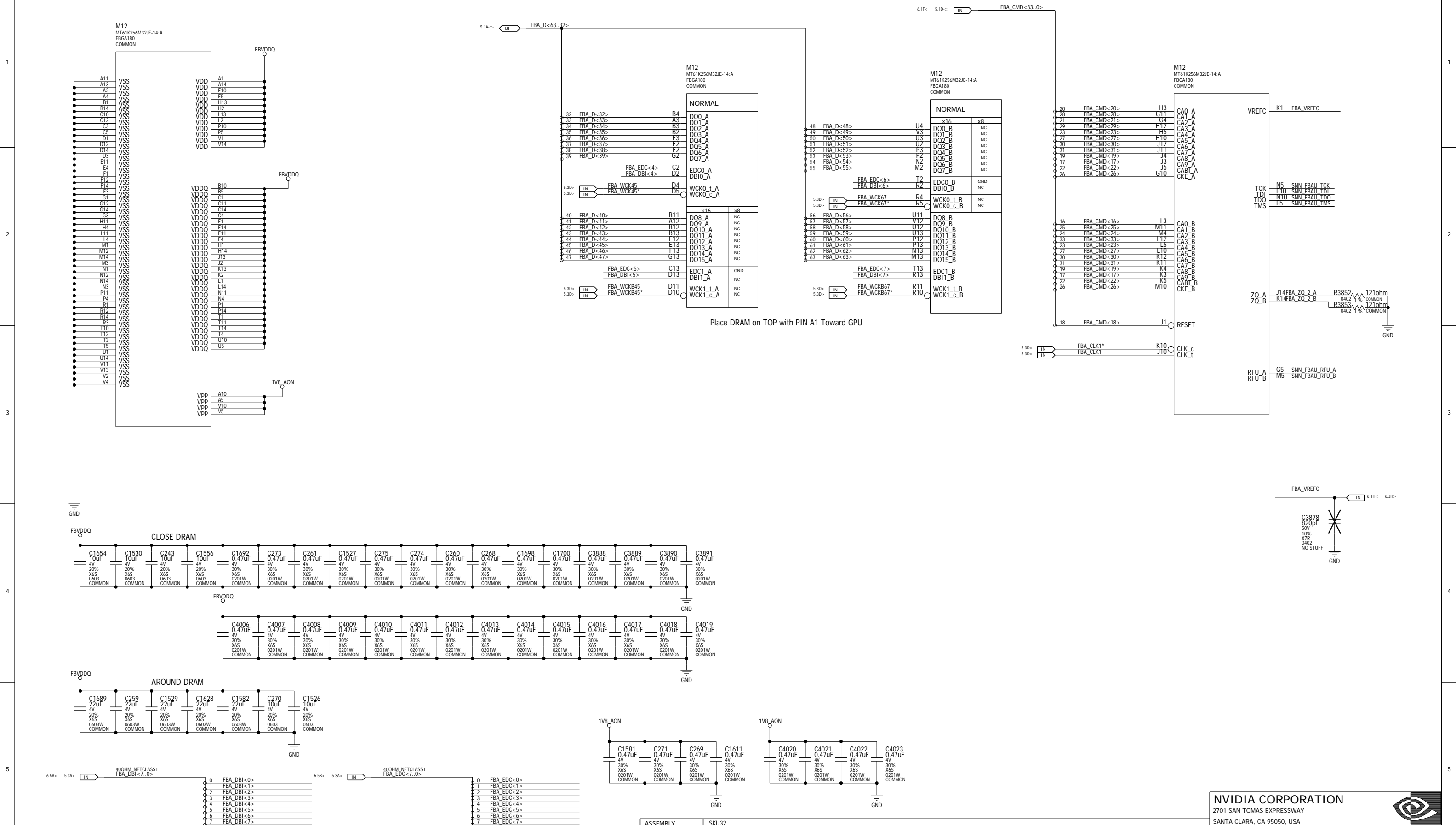
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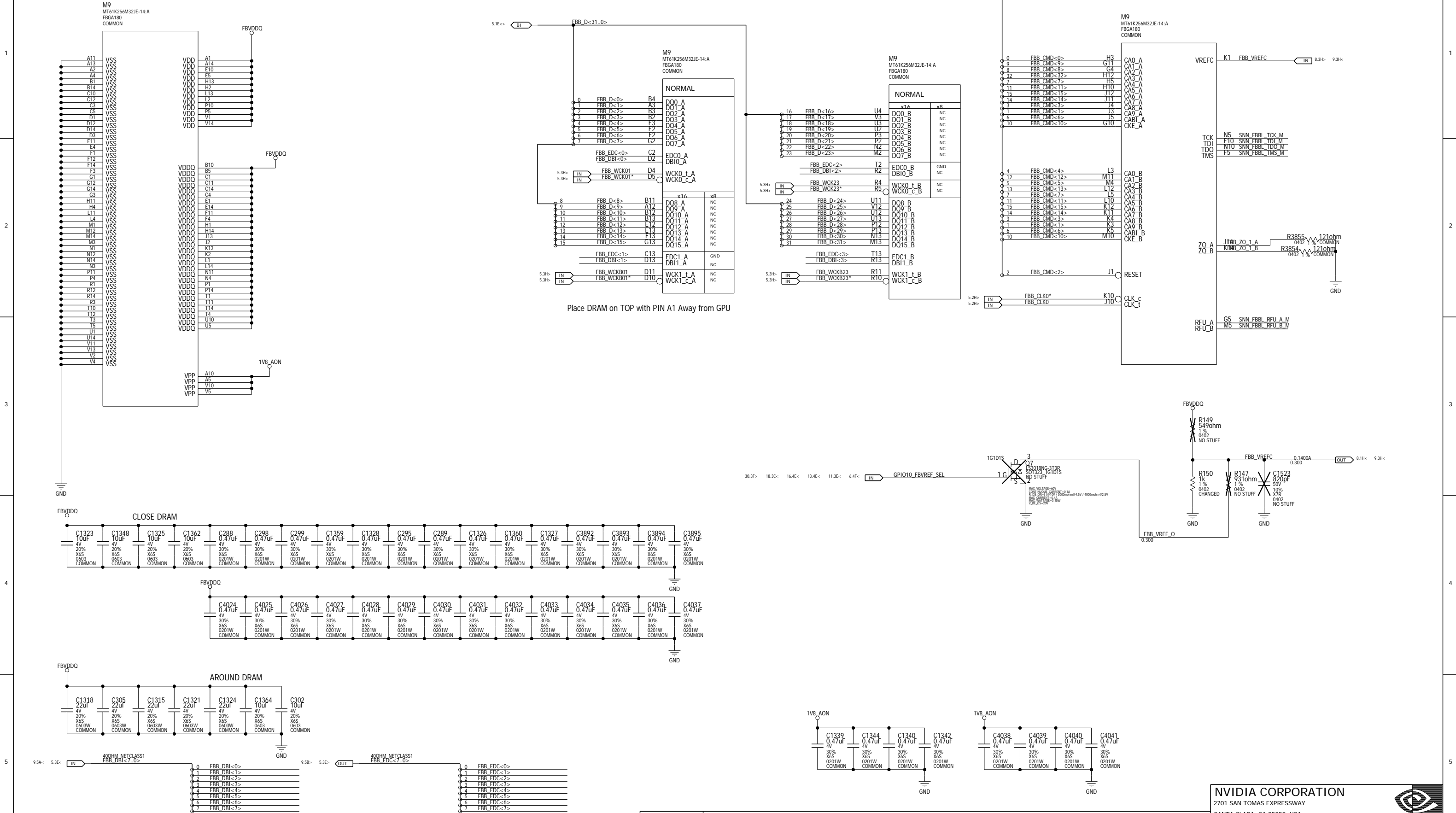
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MEMORY: FBA Partition 63..32



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MEMORY: FBB Partition 31..0



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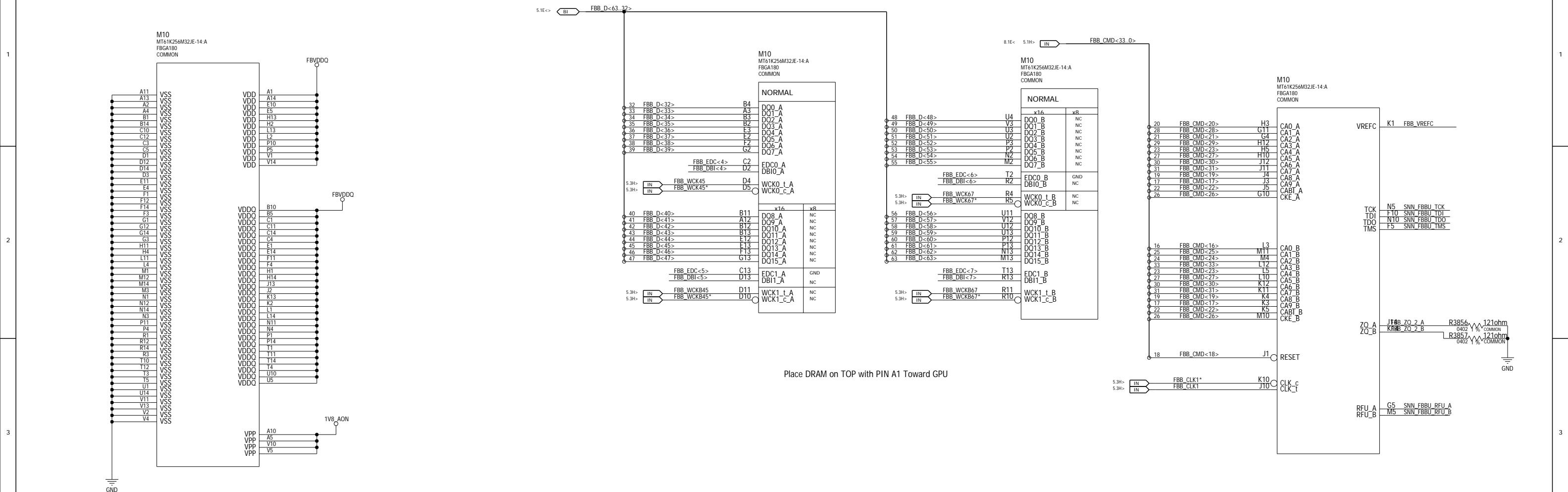
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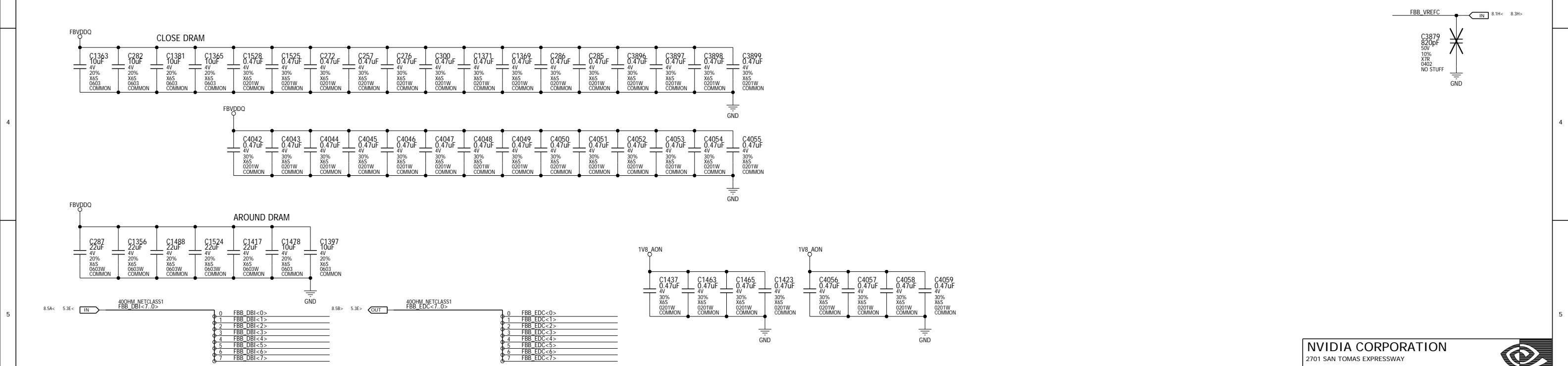
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MEMORY: FBB Partition 63..32



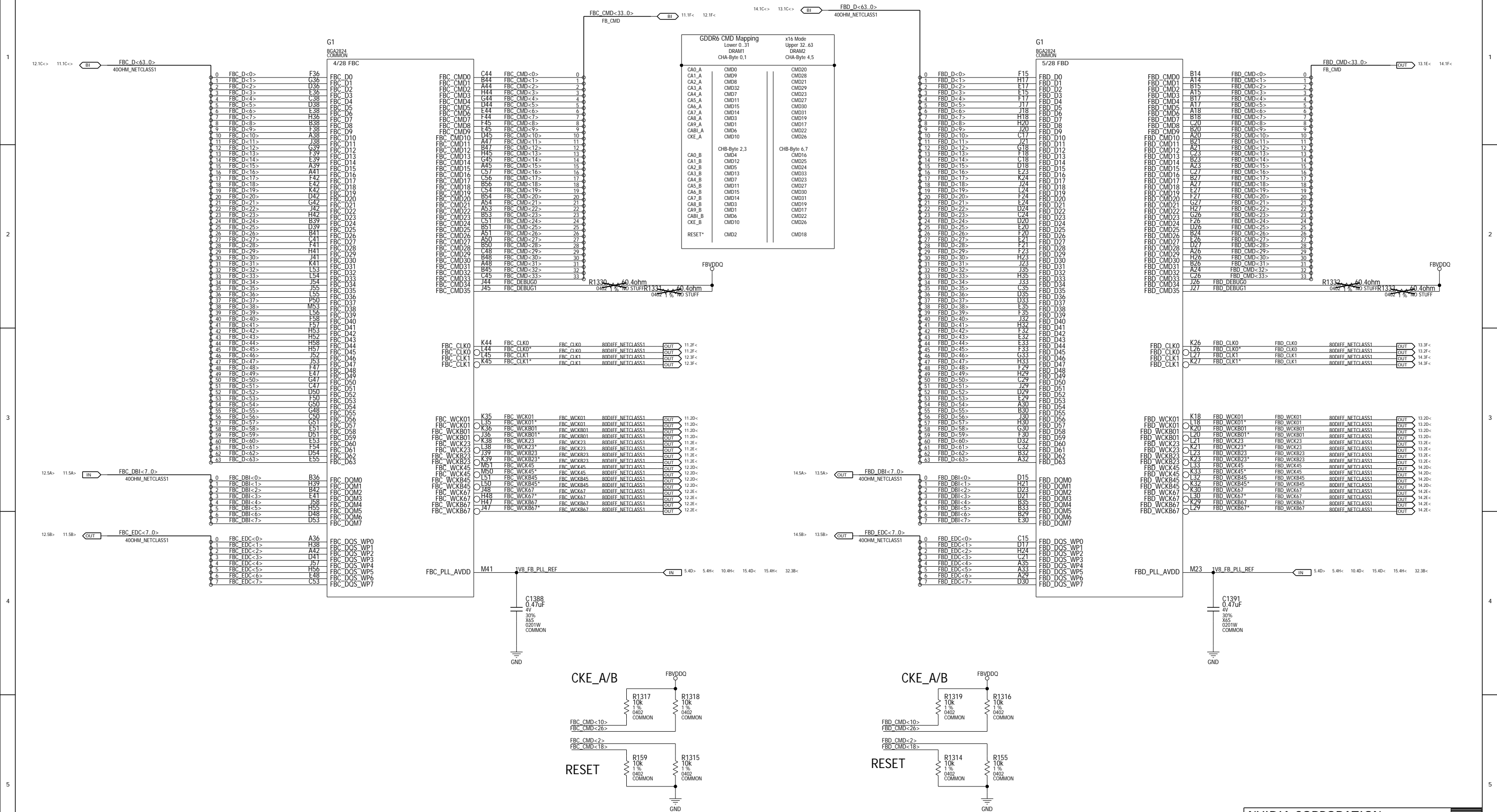
Place DRAM on TOP with PIN A1 Toward GPU



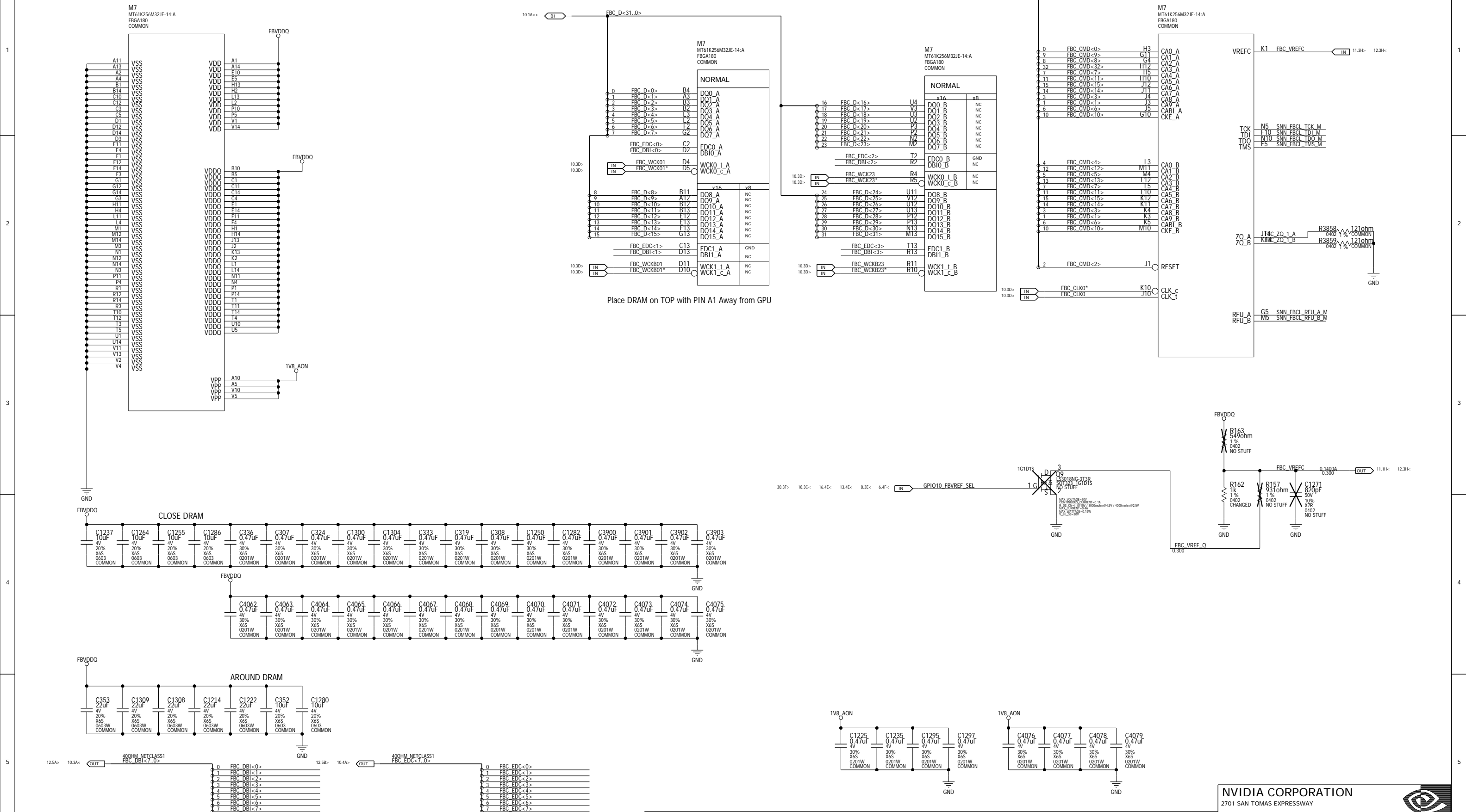
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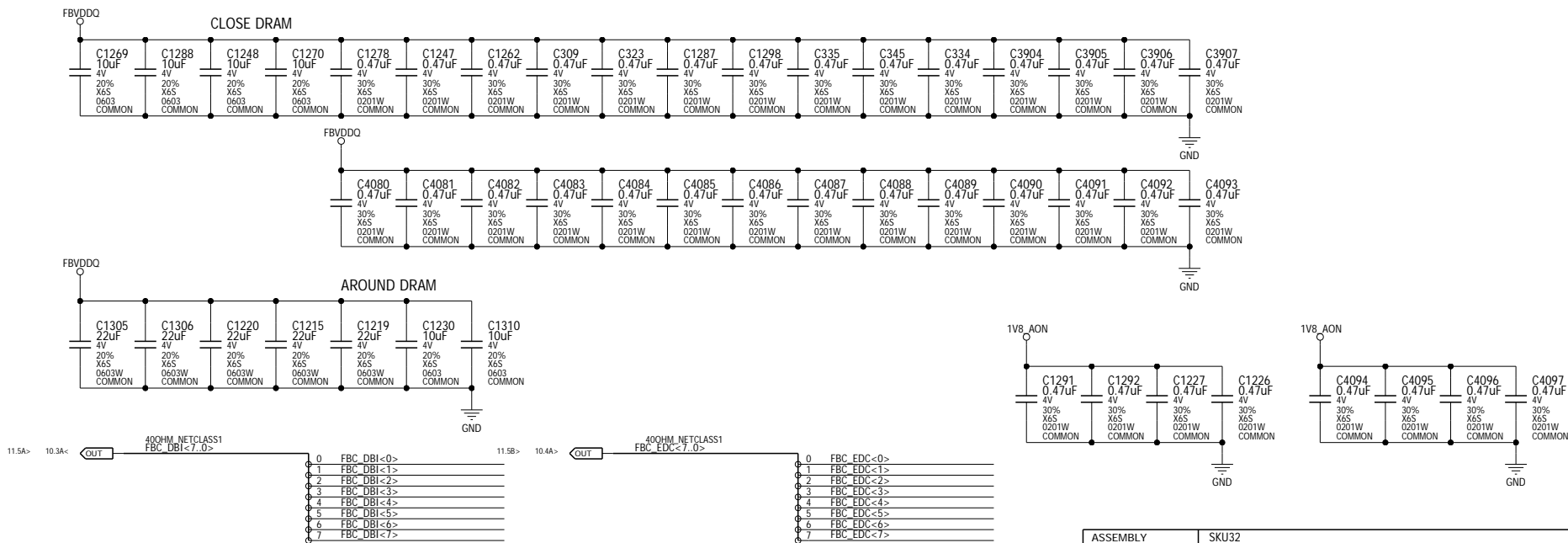
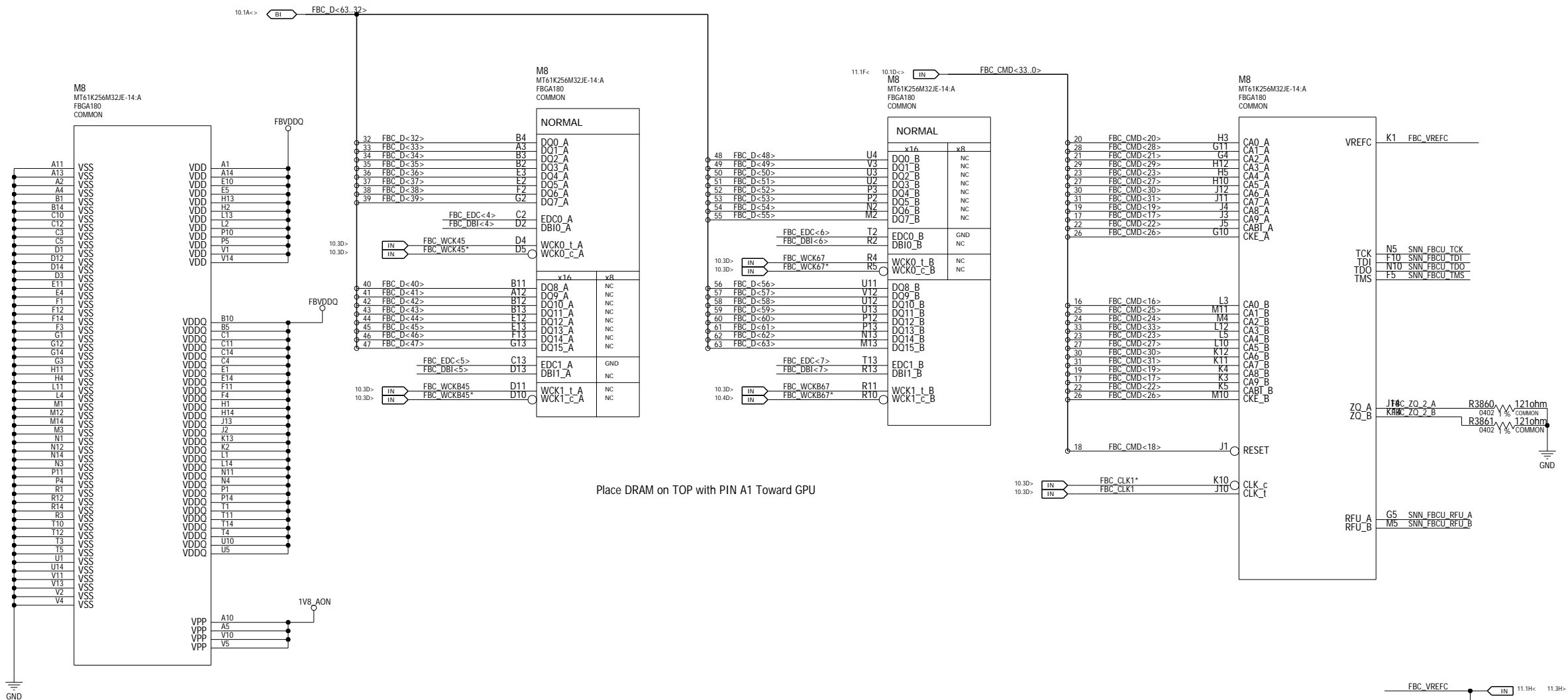
MEMORY: GPU Partition C/D



MEMORY: FBC Partition 31..0

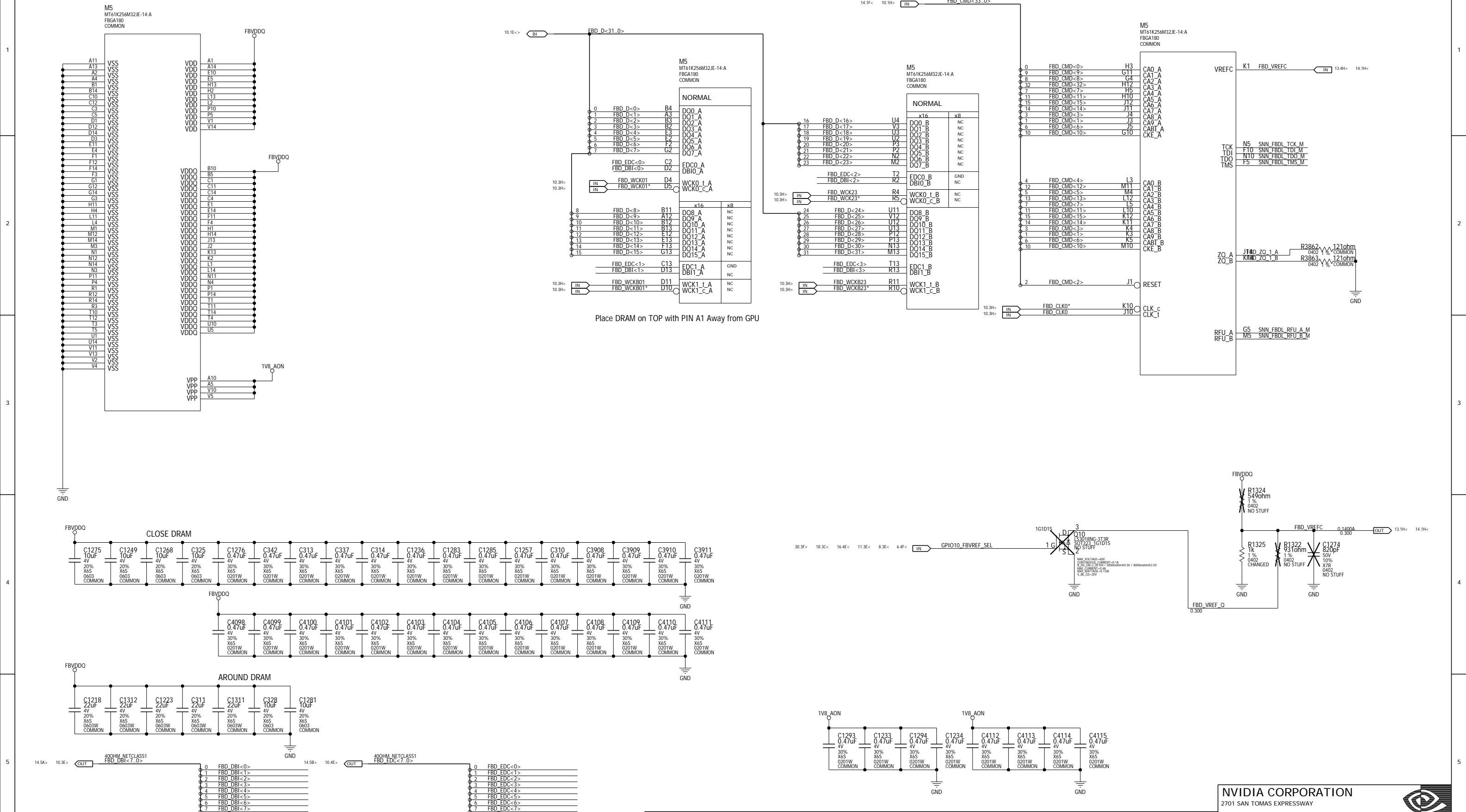


MEMORY: FBC Partition 63..32

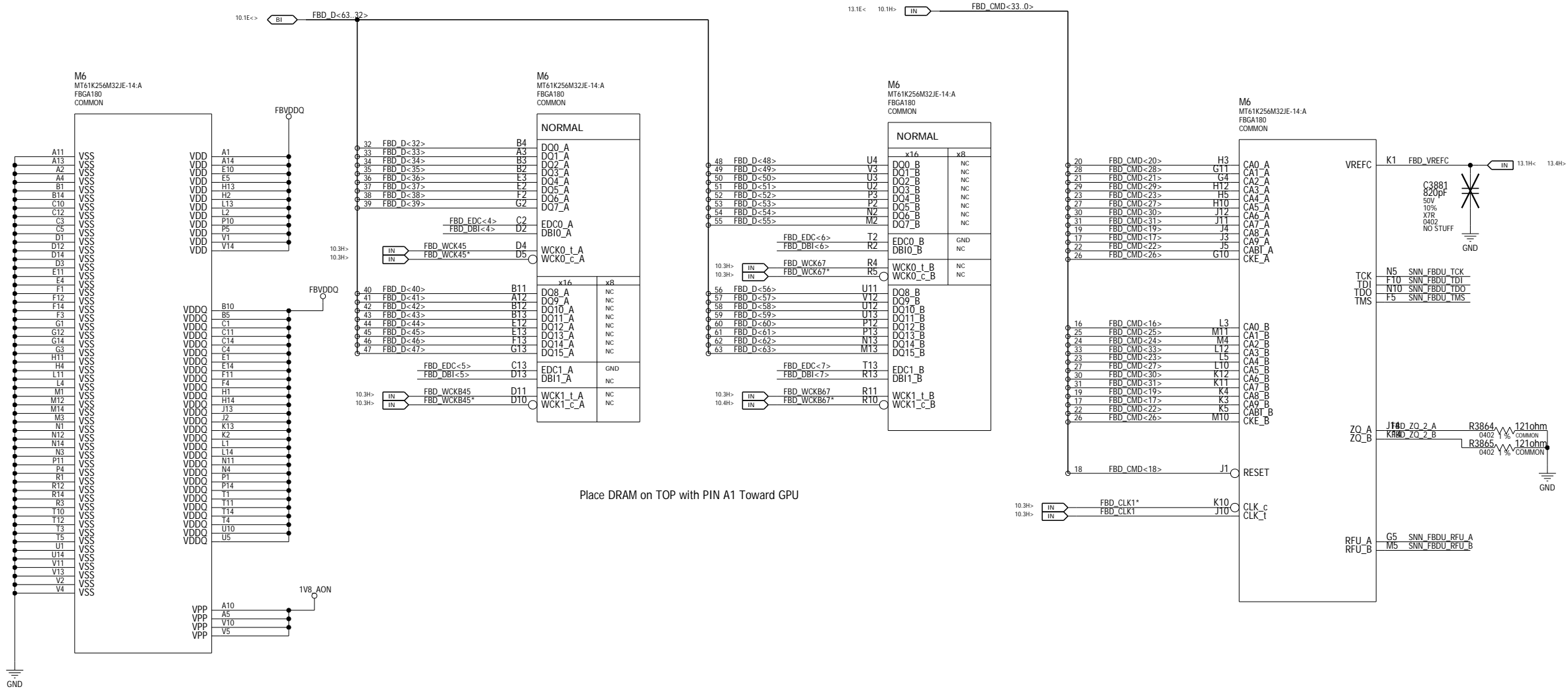


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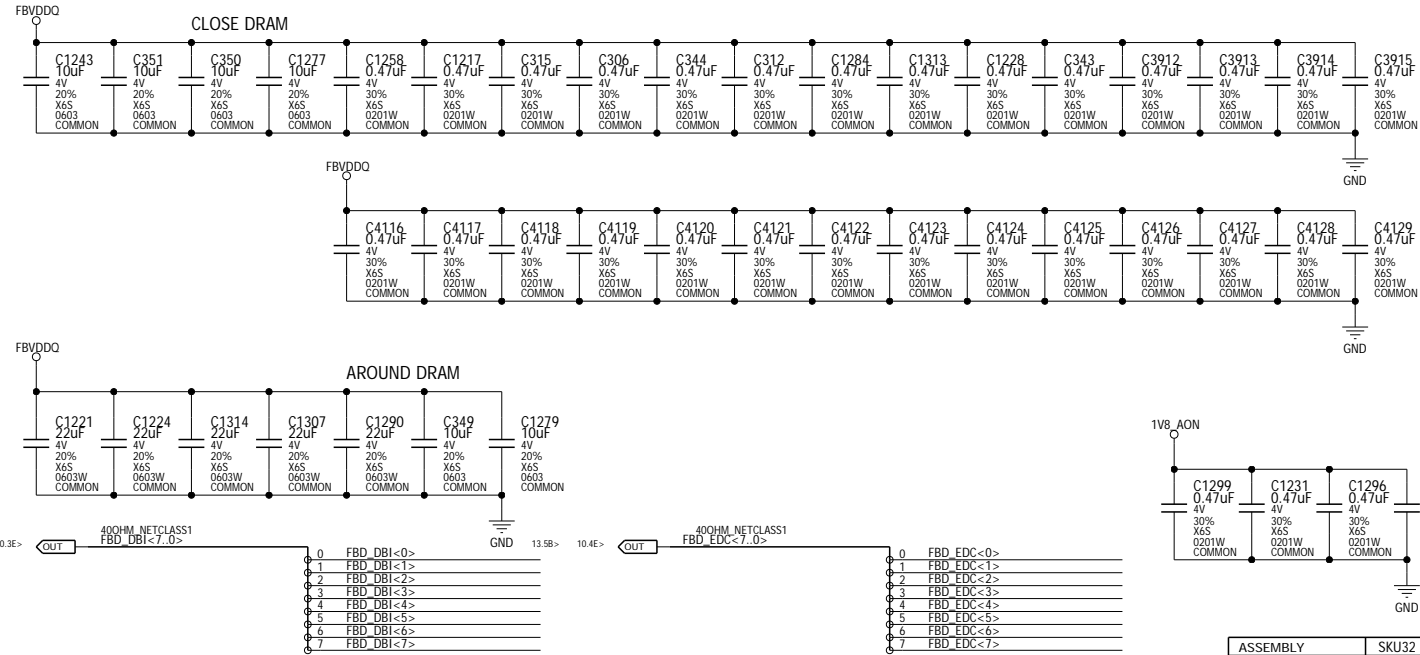
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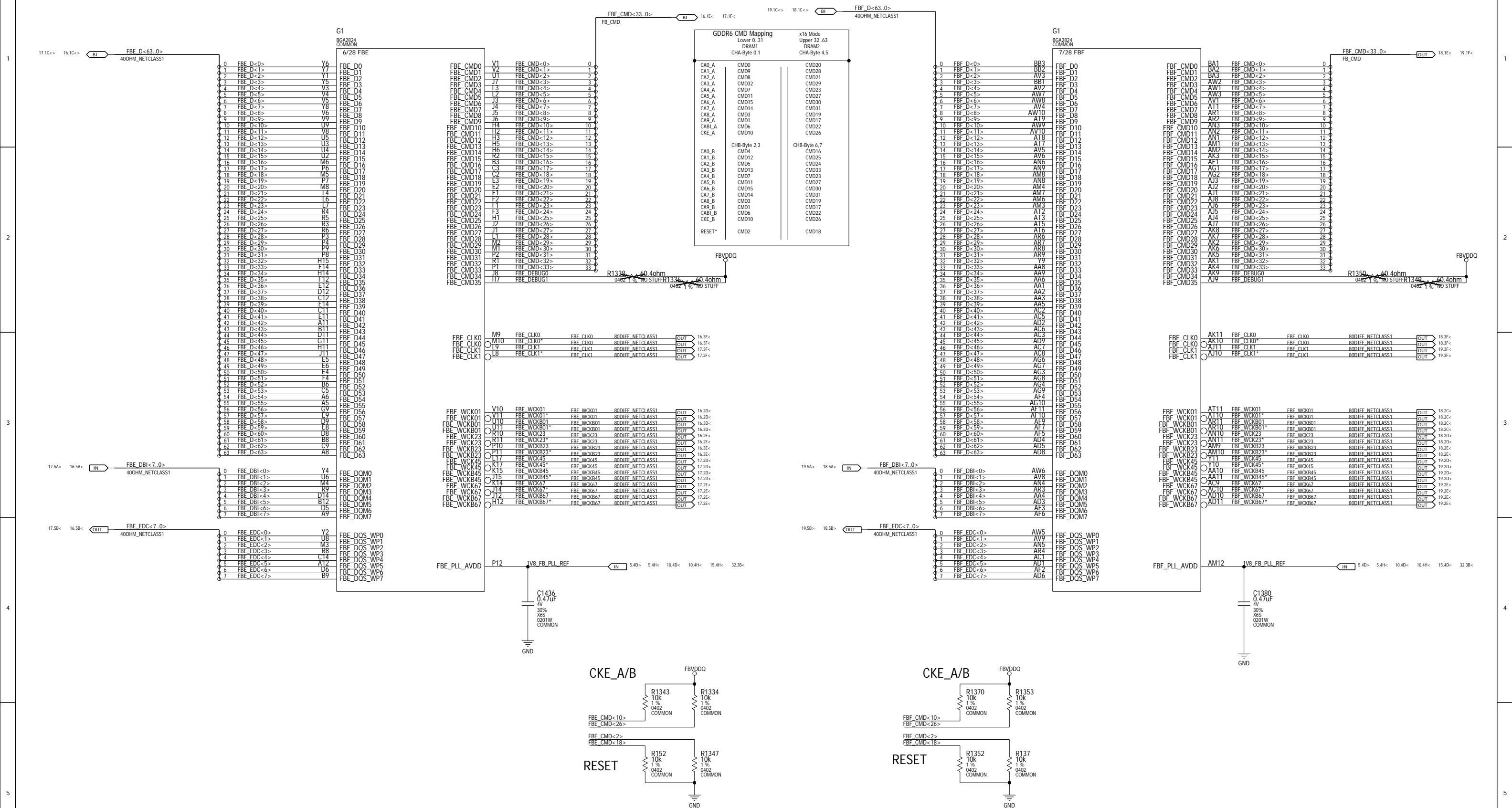
MEMORY: FBD Partition 63..32



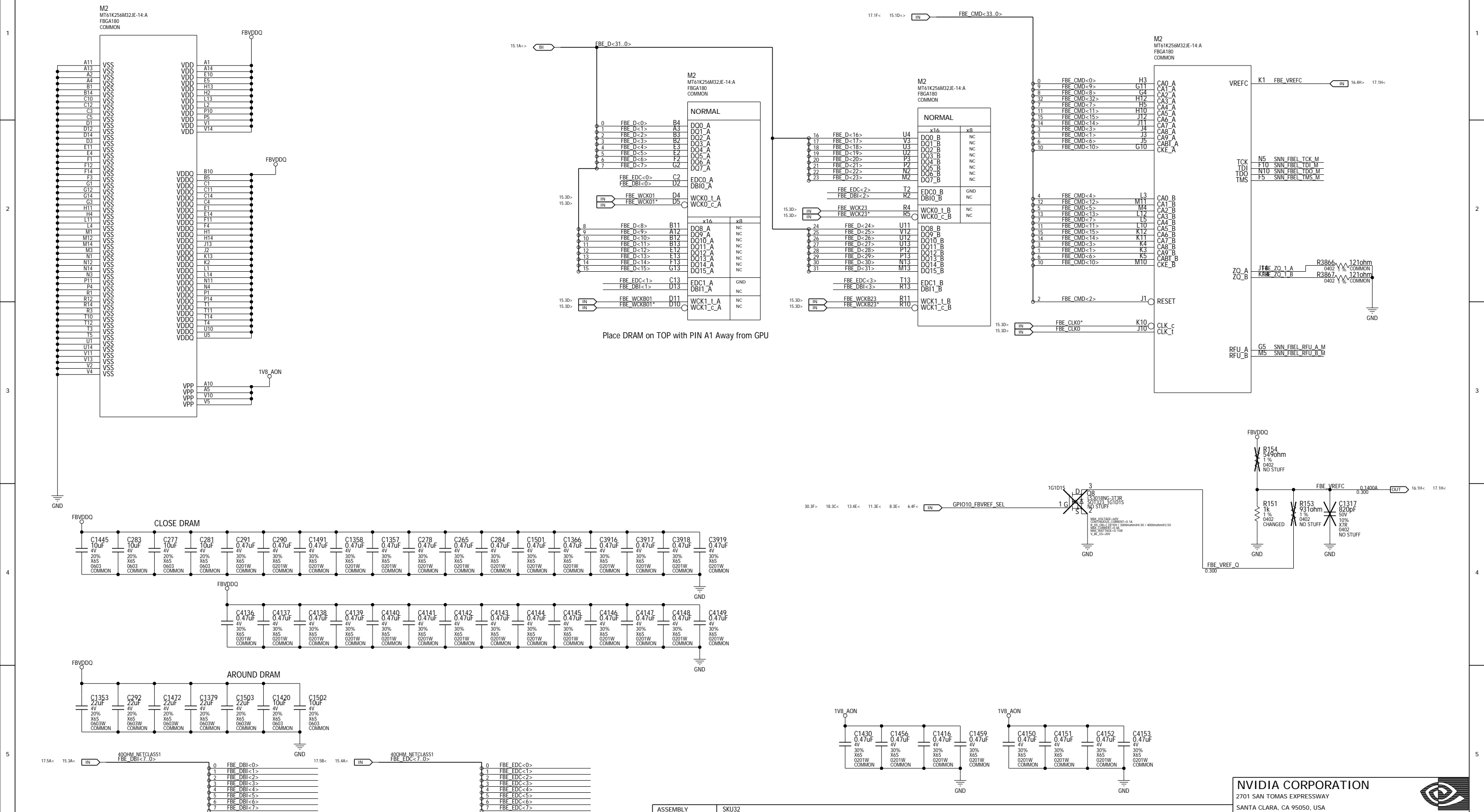
Place DRAM on TOP with PIN A1 Toward GPU



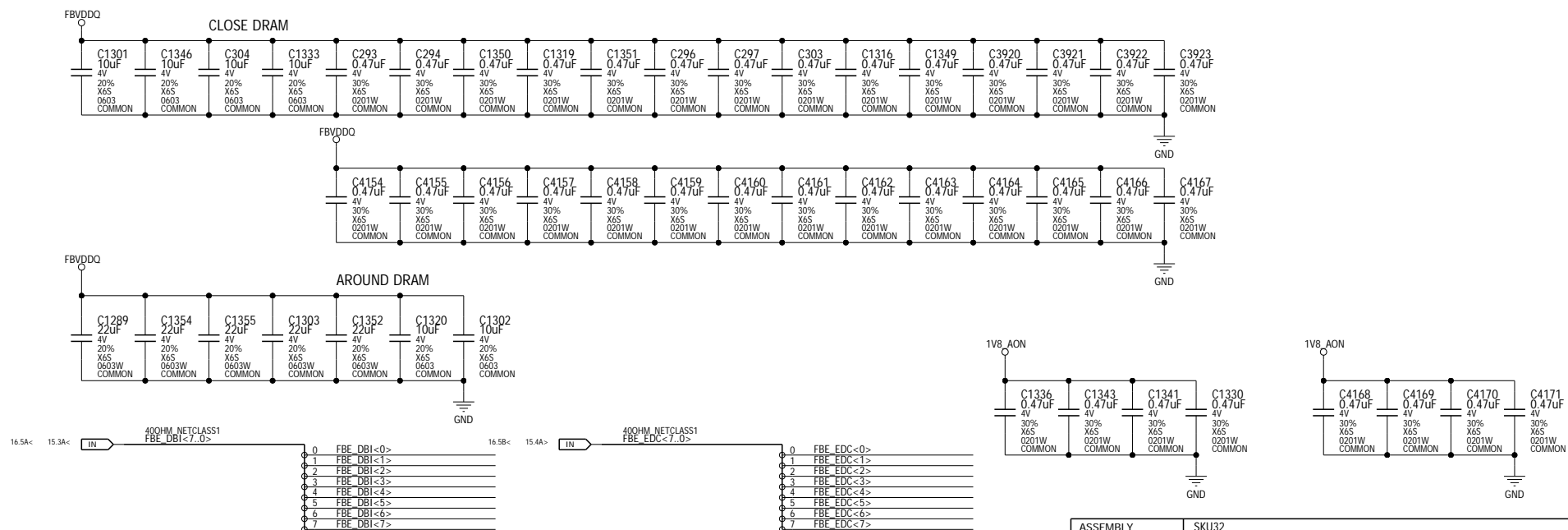
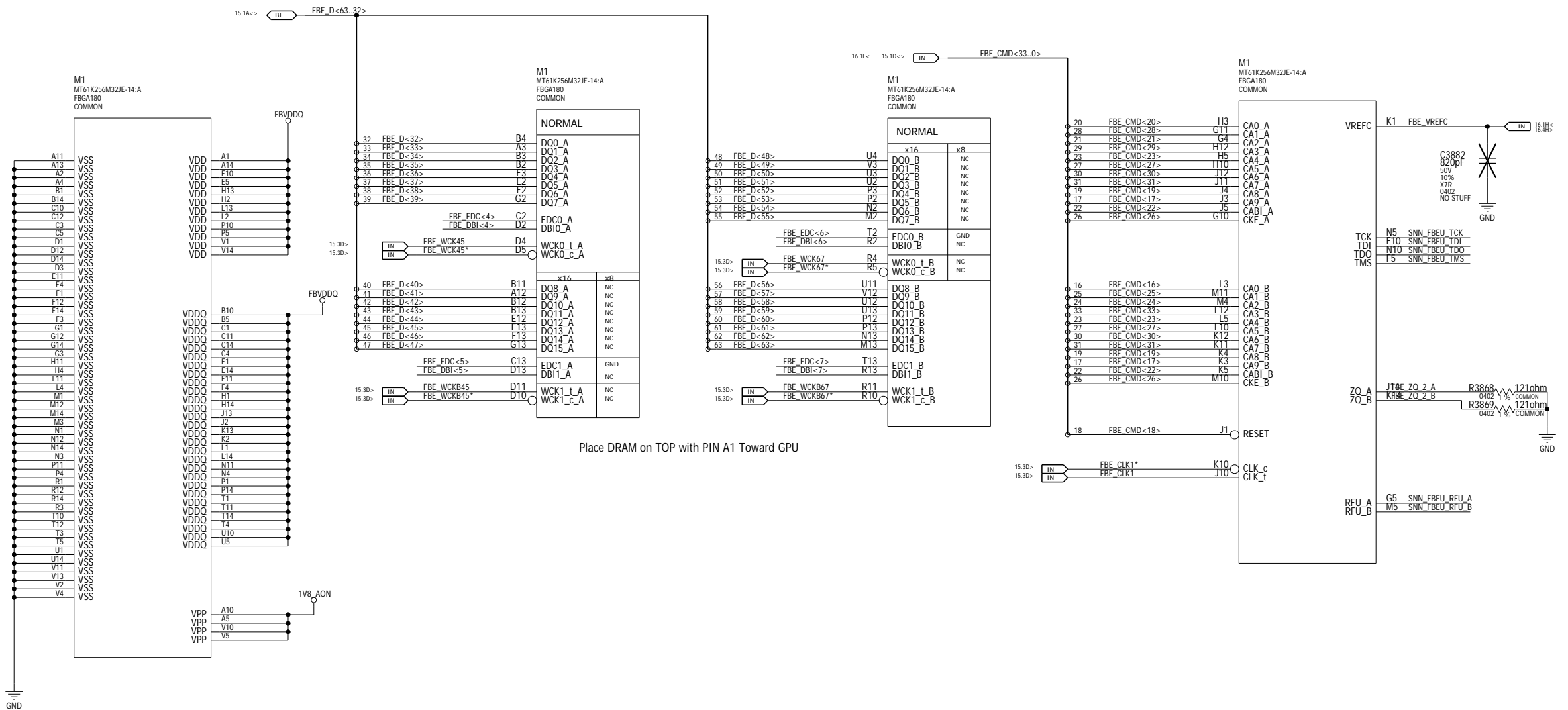
MEMORY: GPU Partition E/F



MEMORY: FBE Partition 31..0



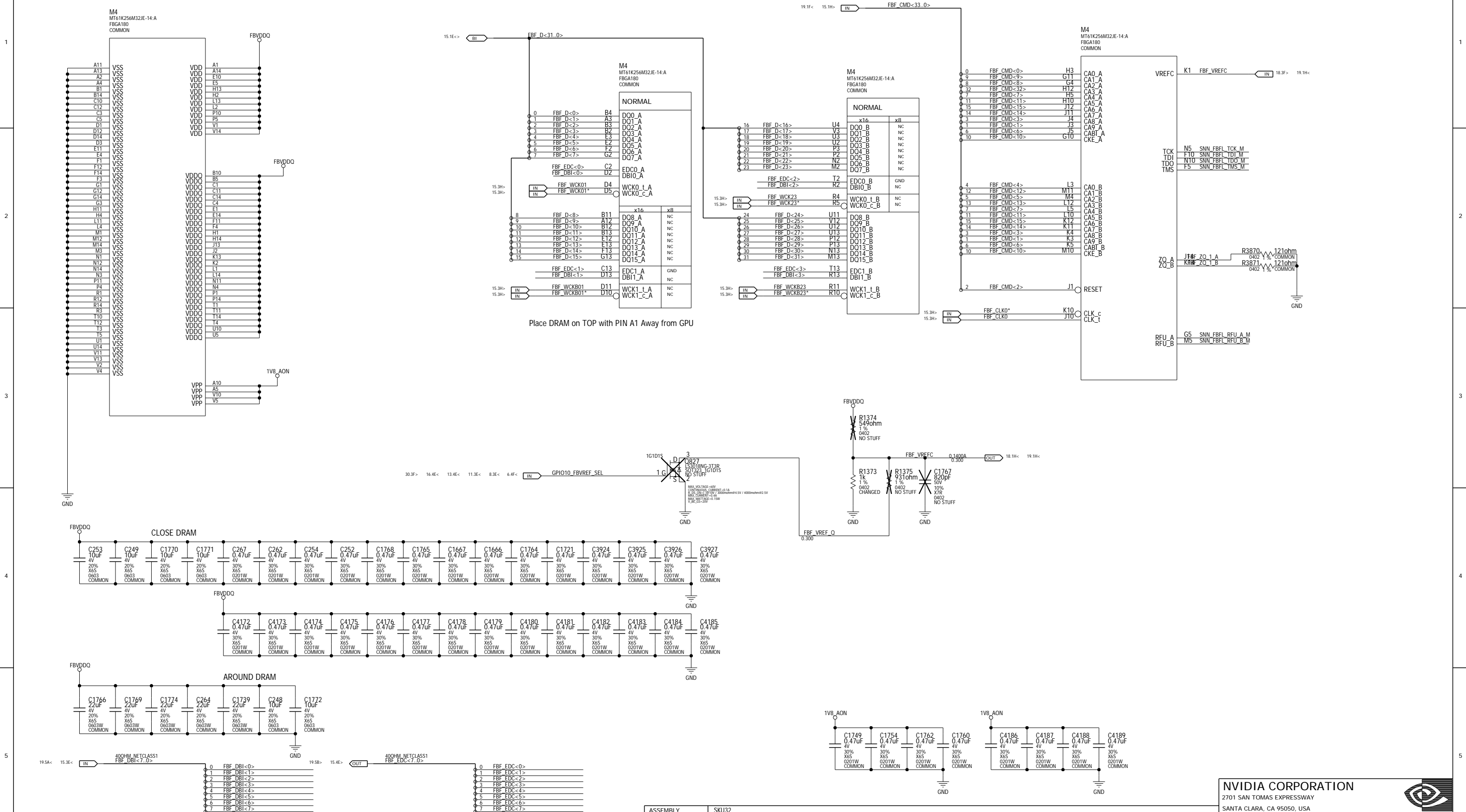
MEMORY: FBE Partition 63..32



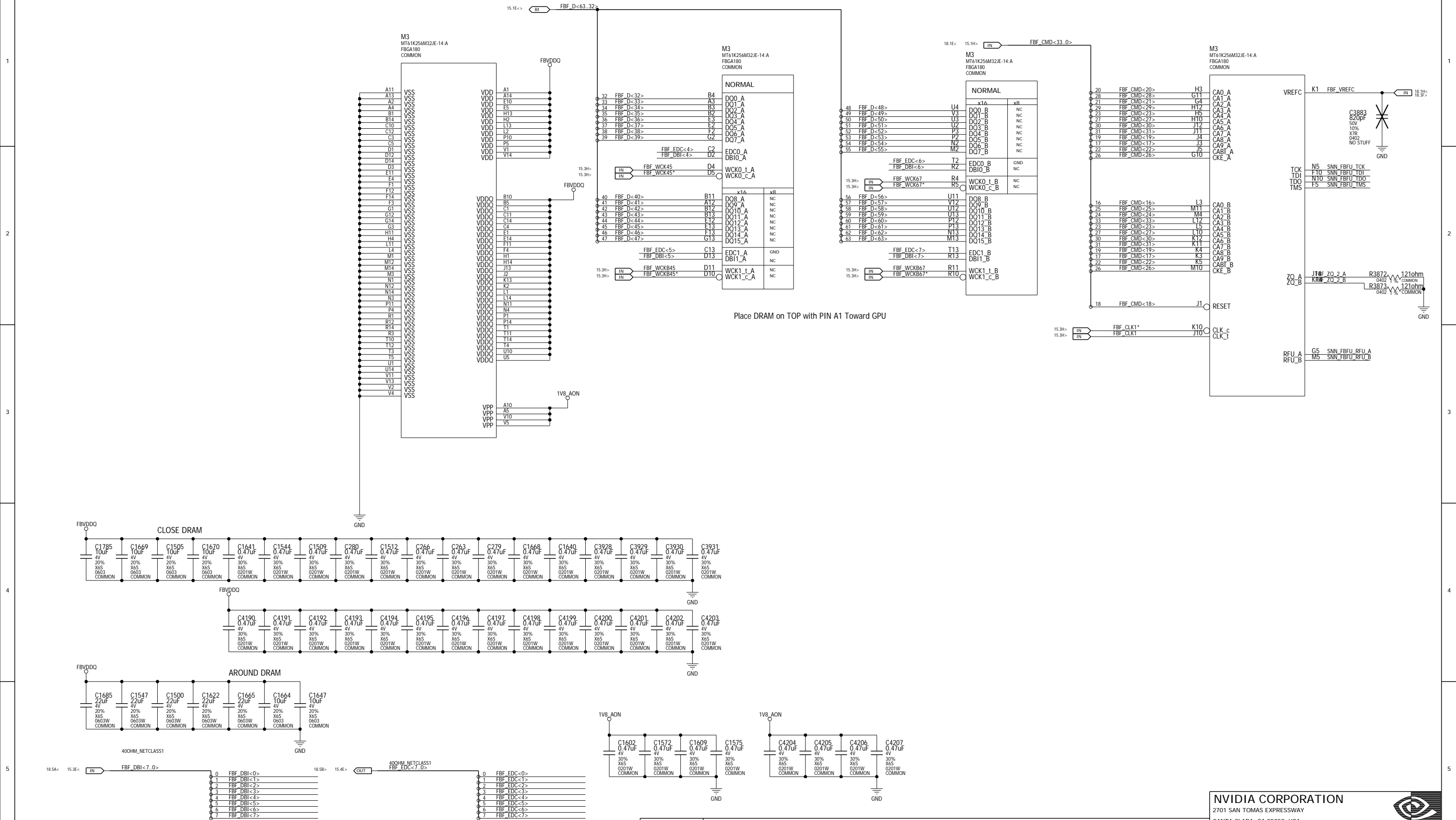
ASSEMBLY	SKU32
PAGE DETAIL	MEMORY: FBE PARTITION[63:32]

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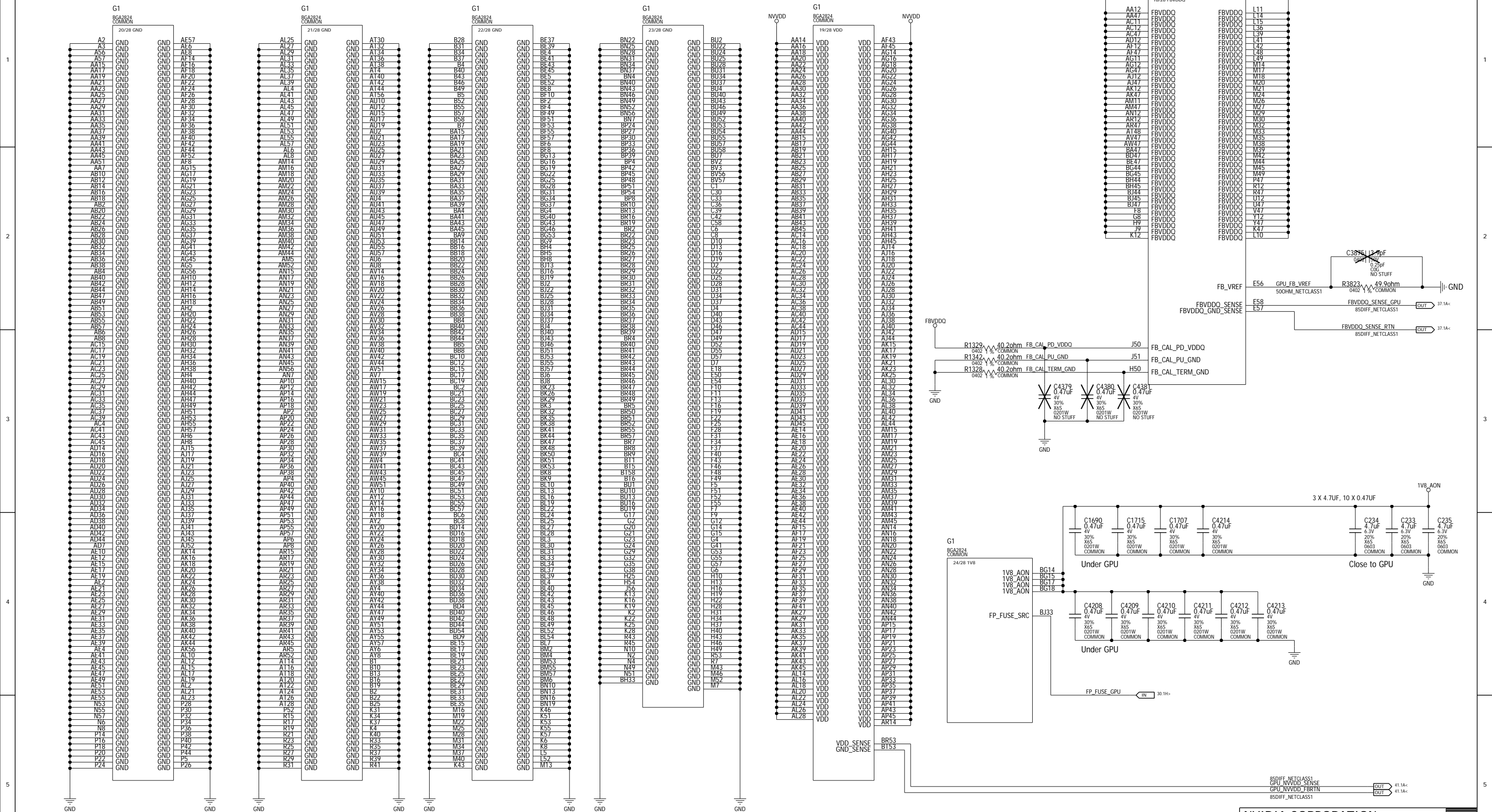
MEMORY: FBF Partition 31..0



MEMORY: FBF Partition 63..32



GPU PWR and GND



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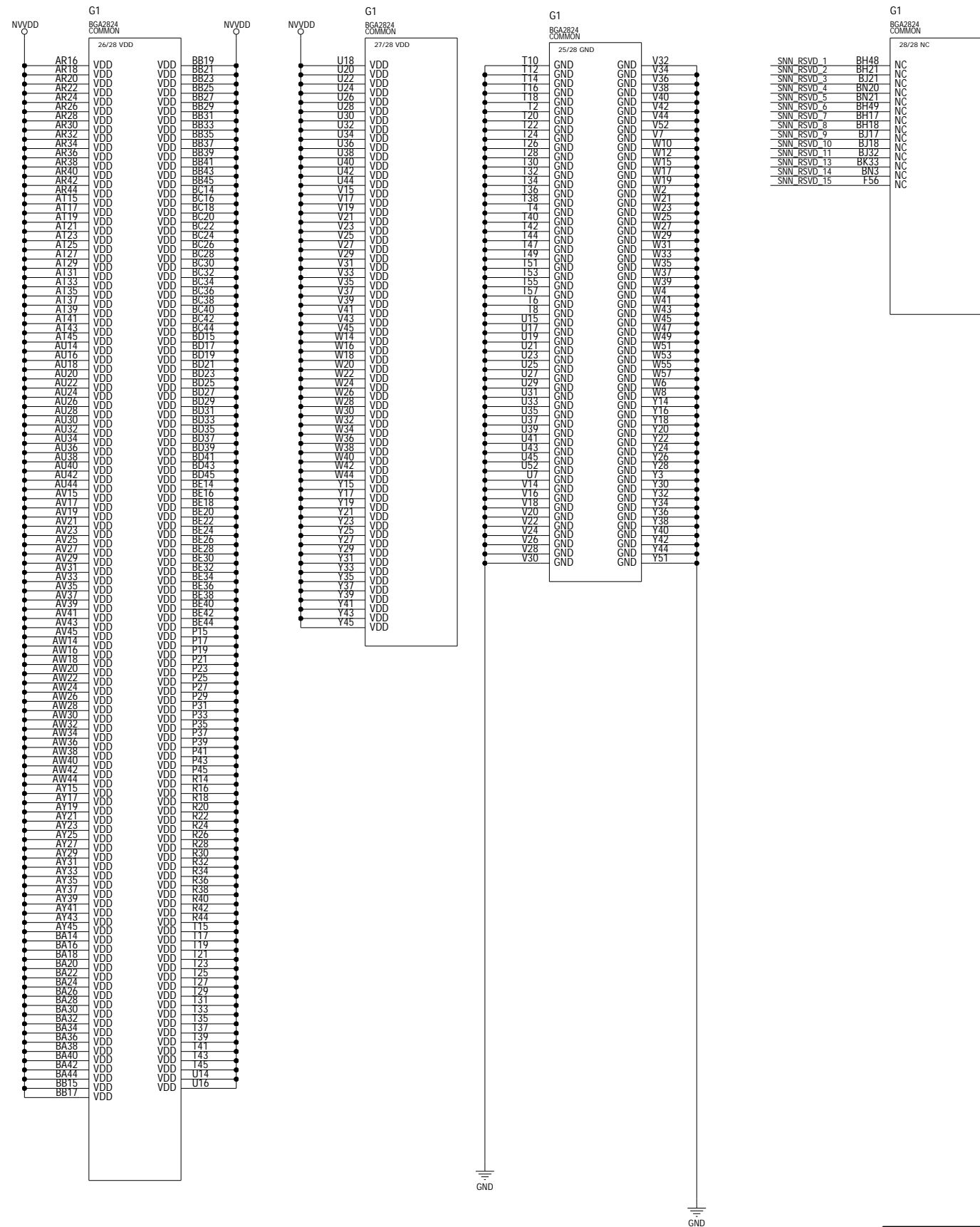


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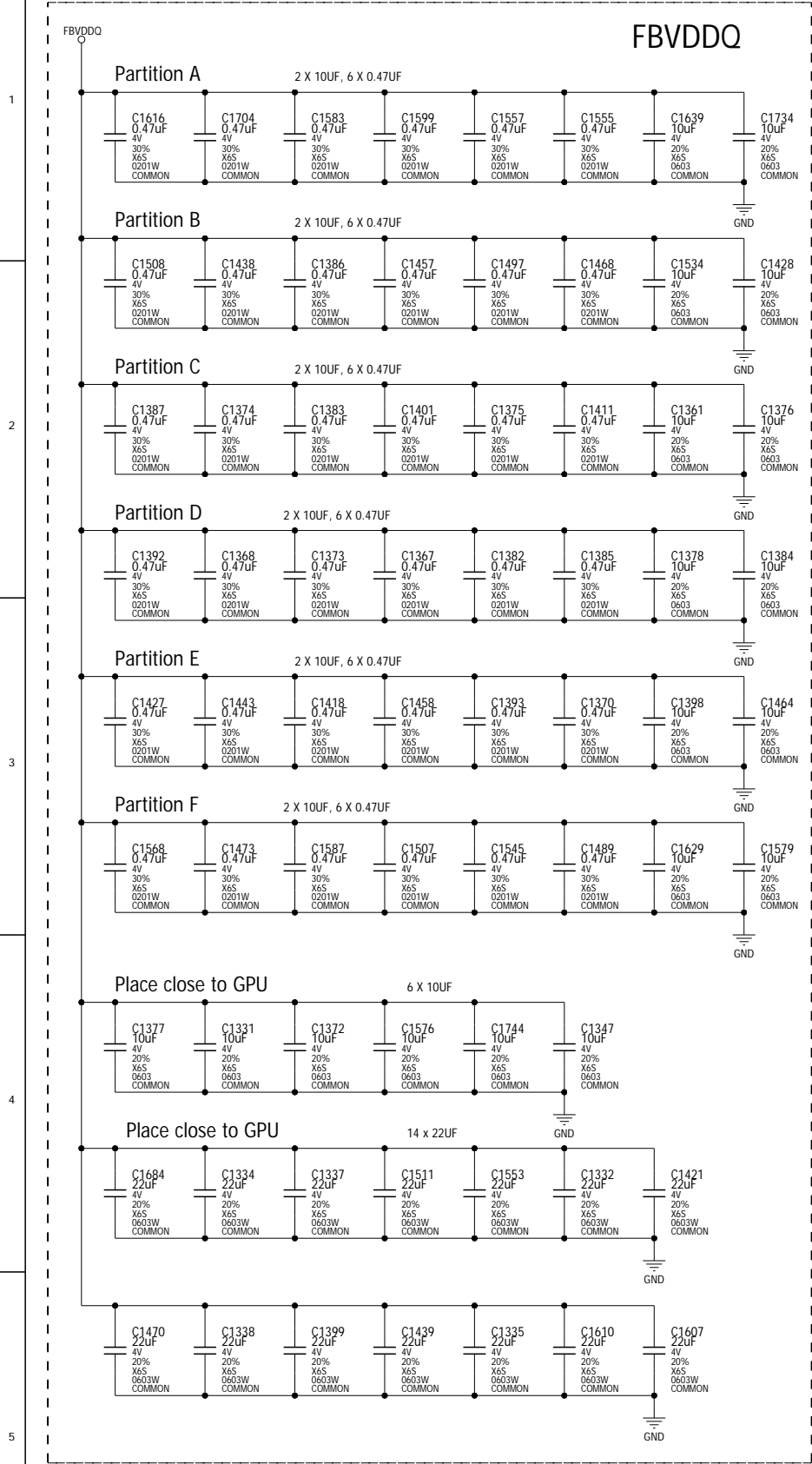
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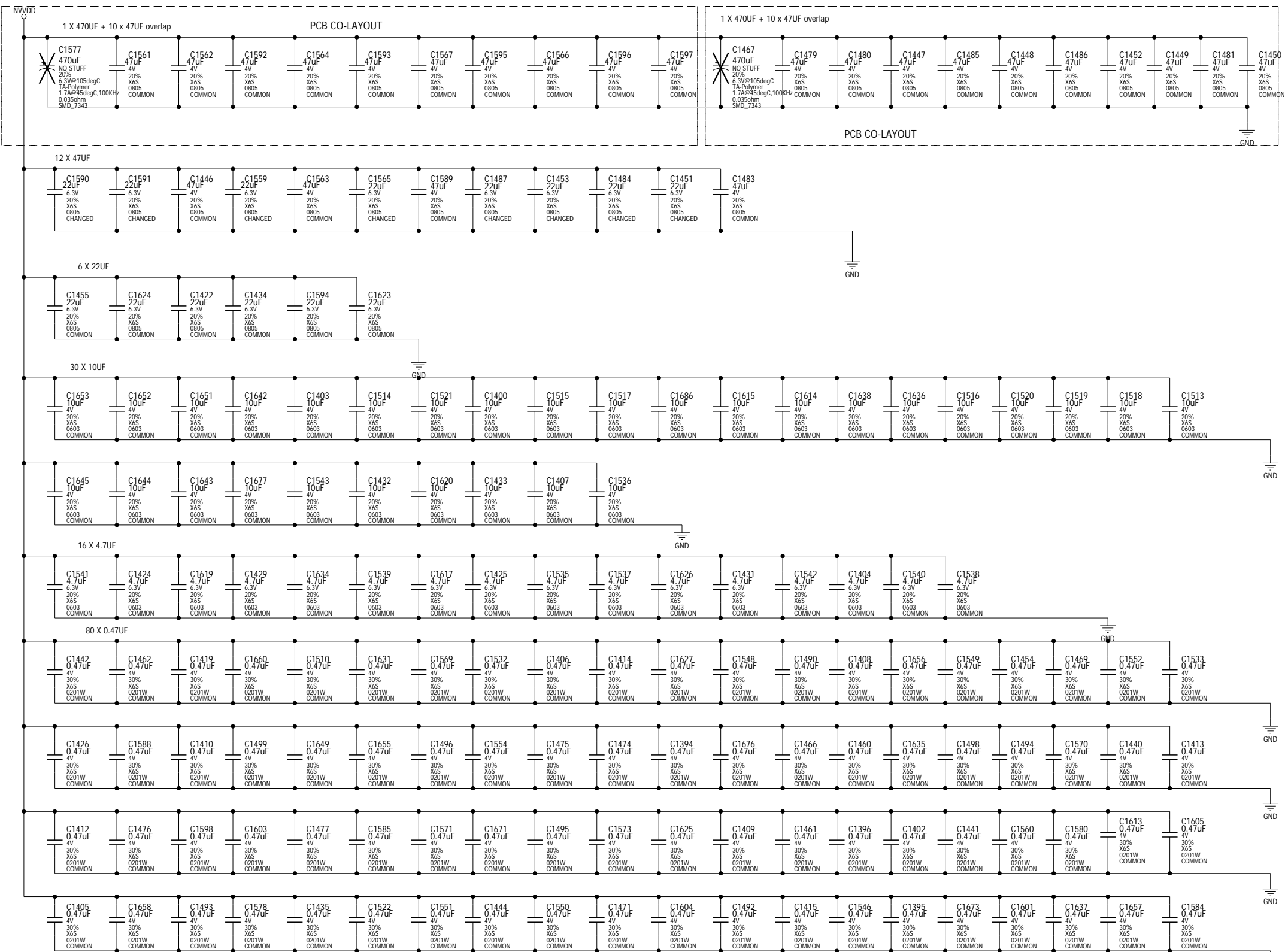
GPU PWR GND NCs



GPU Decoupling



NVVD



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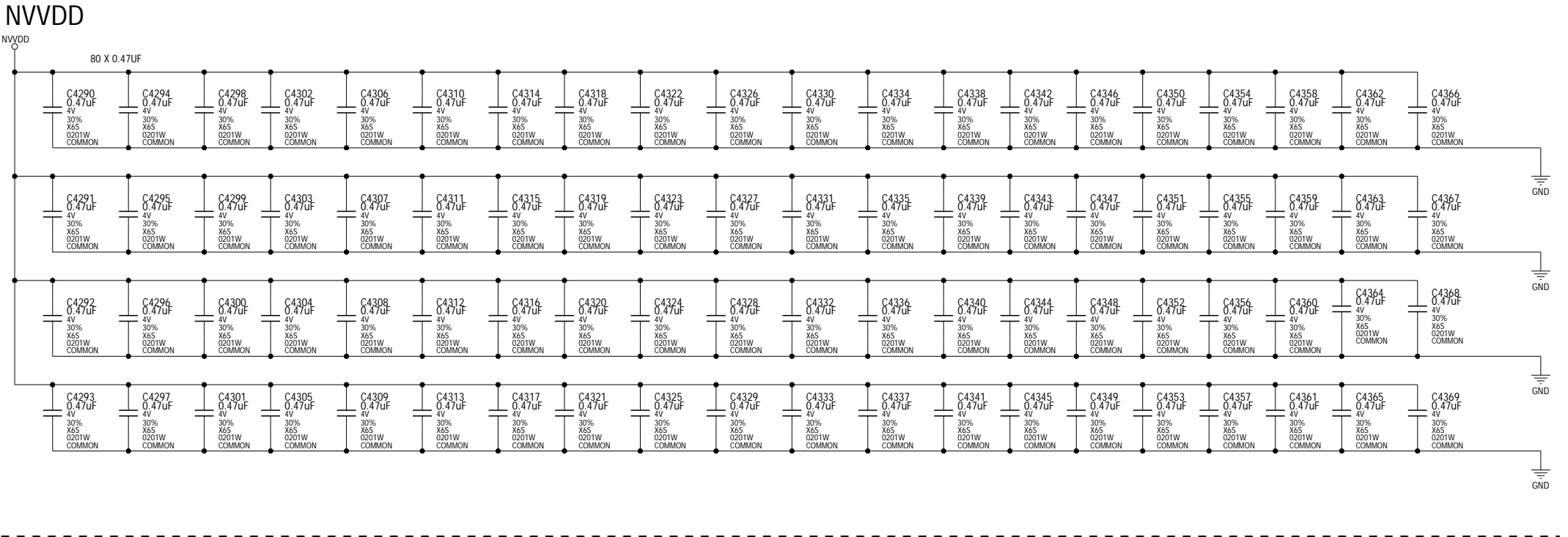
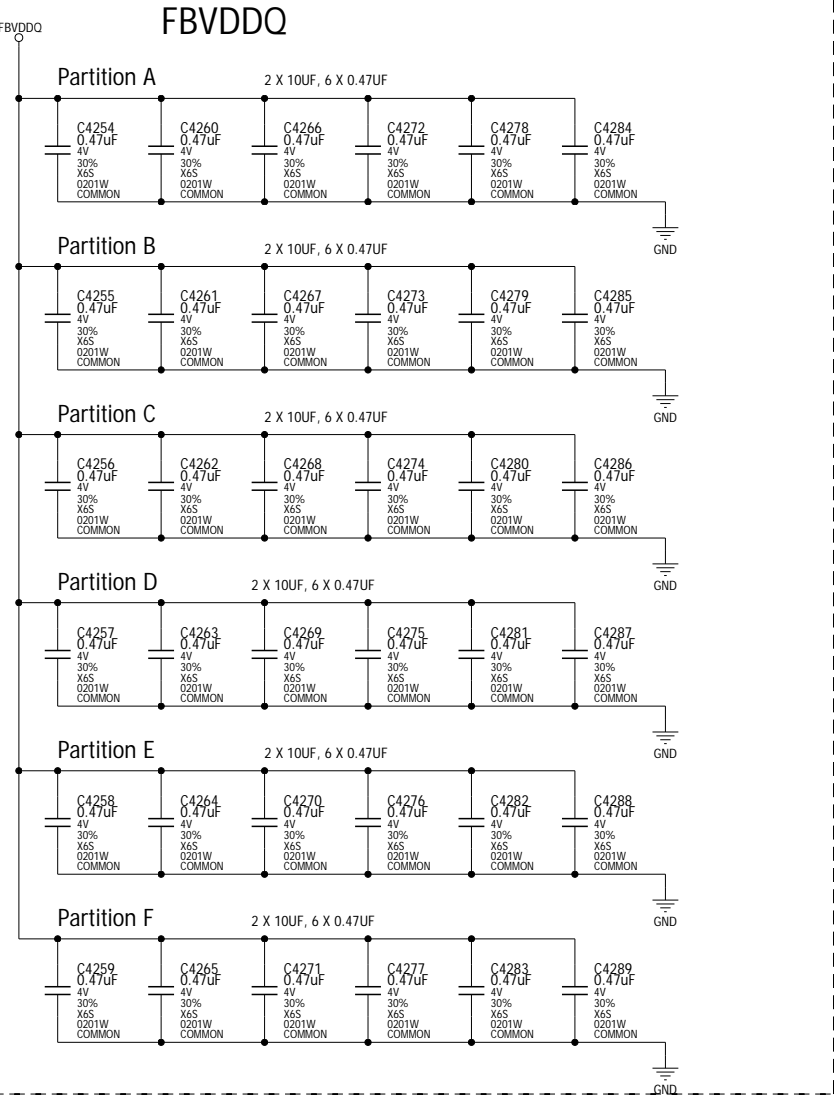
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GPU Decoupling



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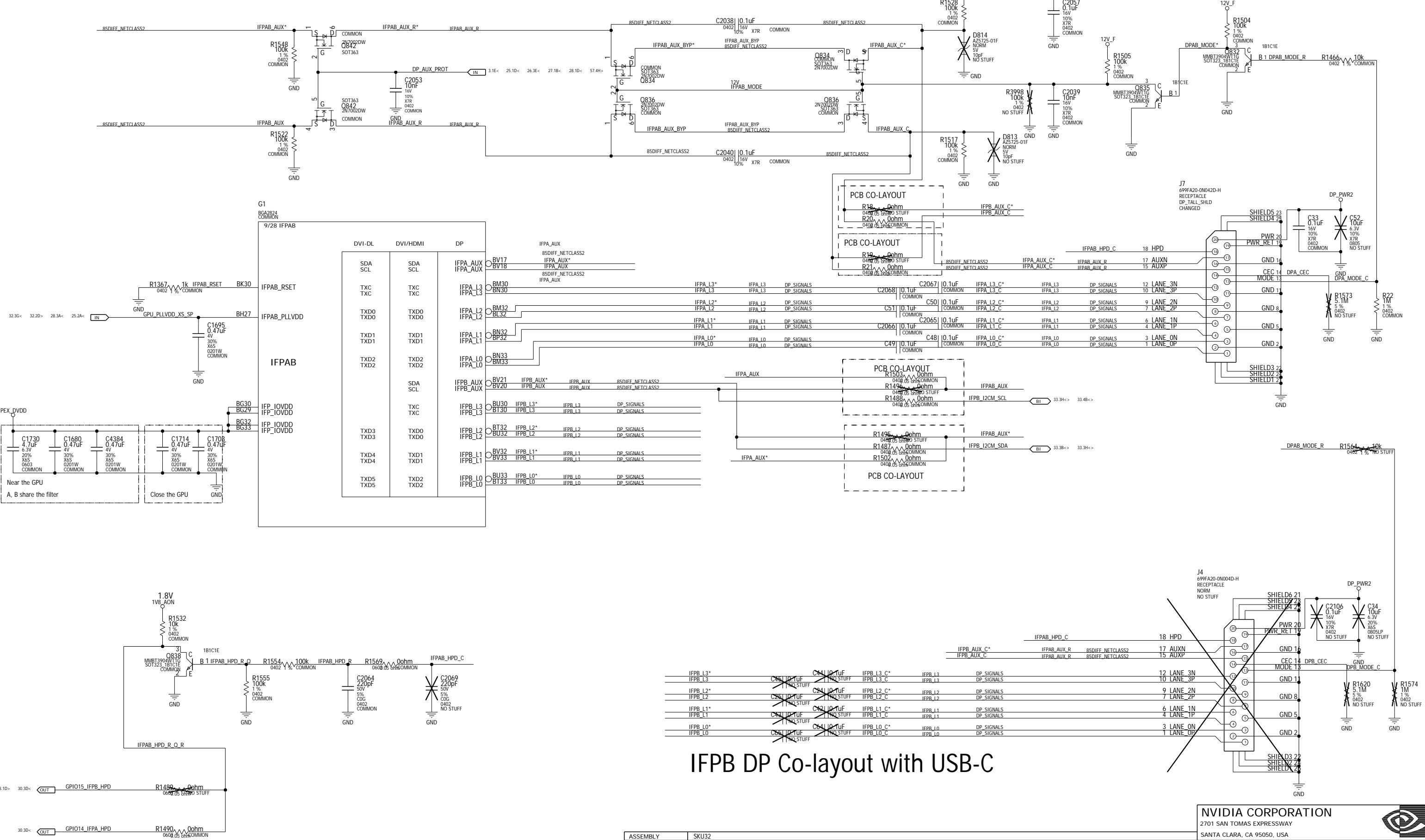
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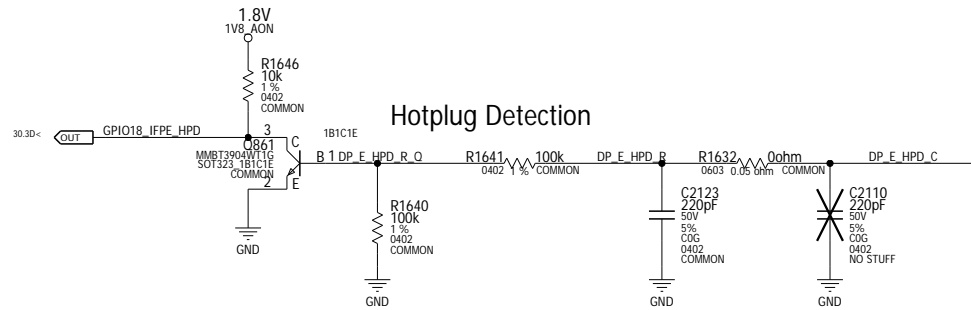
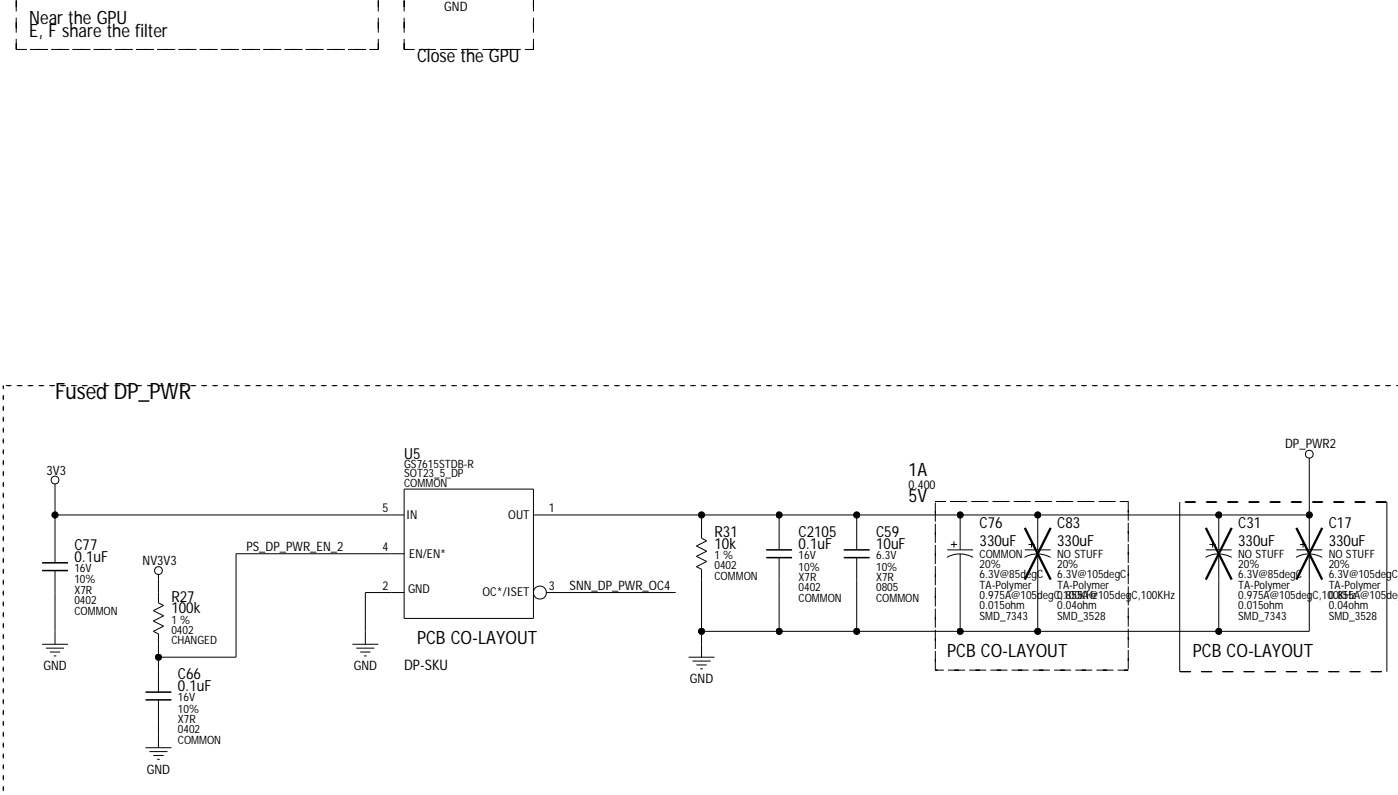
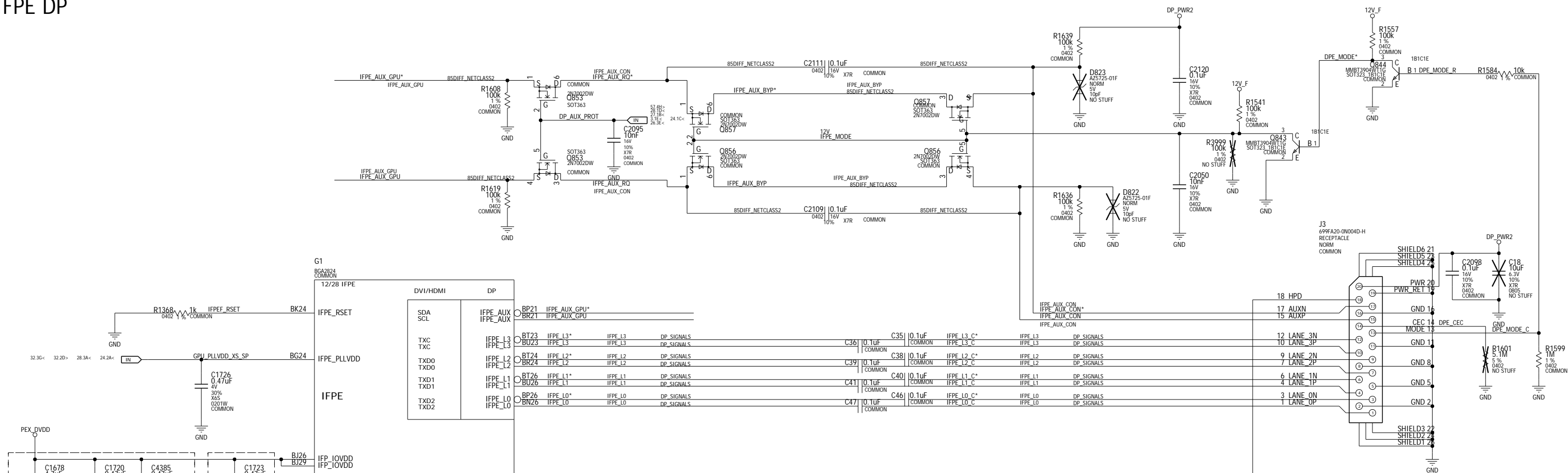
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IFPAB TALL-DP



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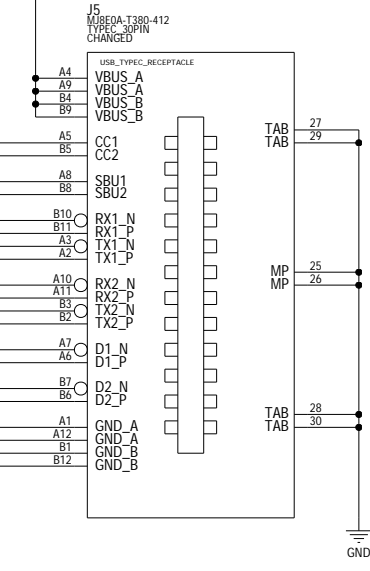
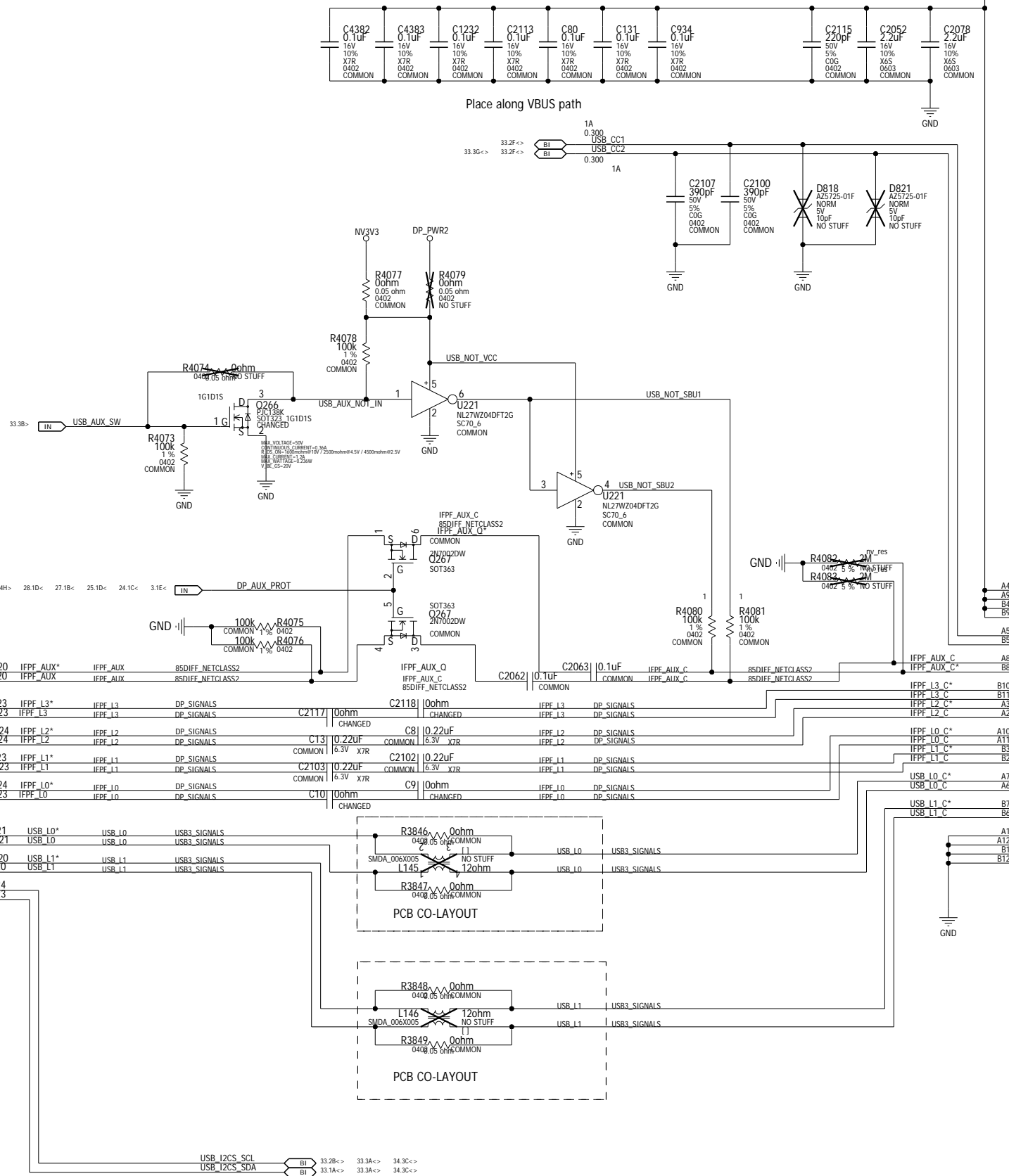
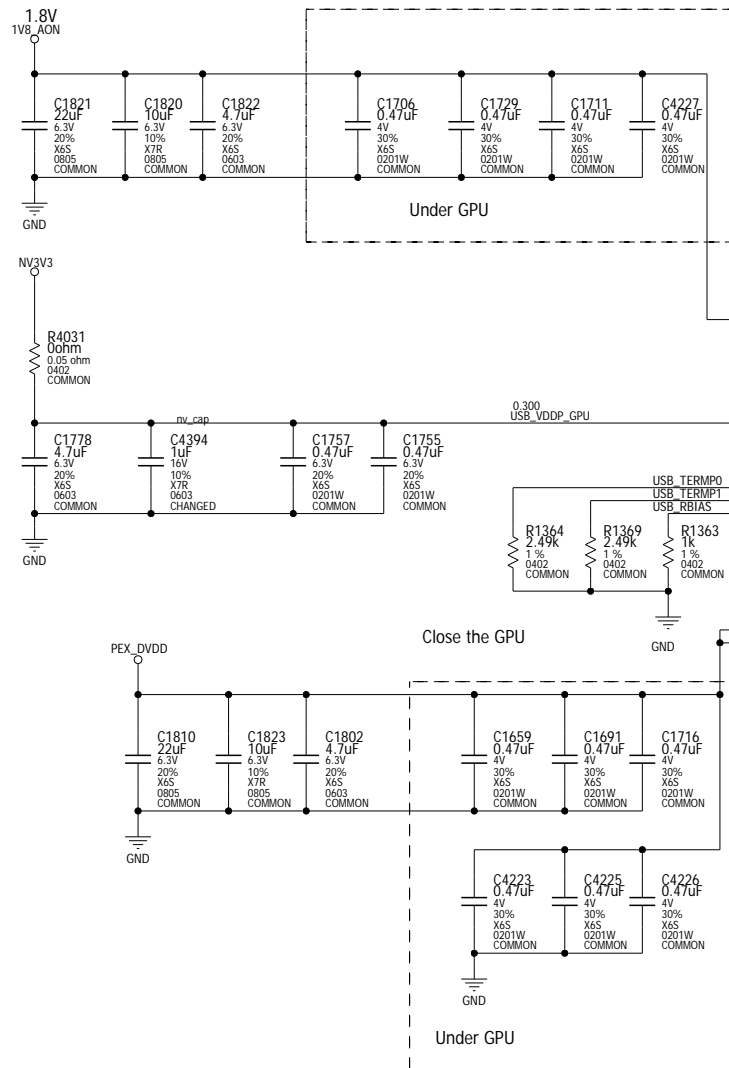
IFPE DP



ASSEMBLY	SKU32
PAGE DETAIL	IFPE DP

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IFPF USBC



ASSEMBLY	SKU32
PAGE DETAIL	IFPF USB

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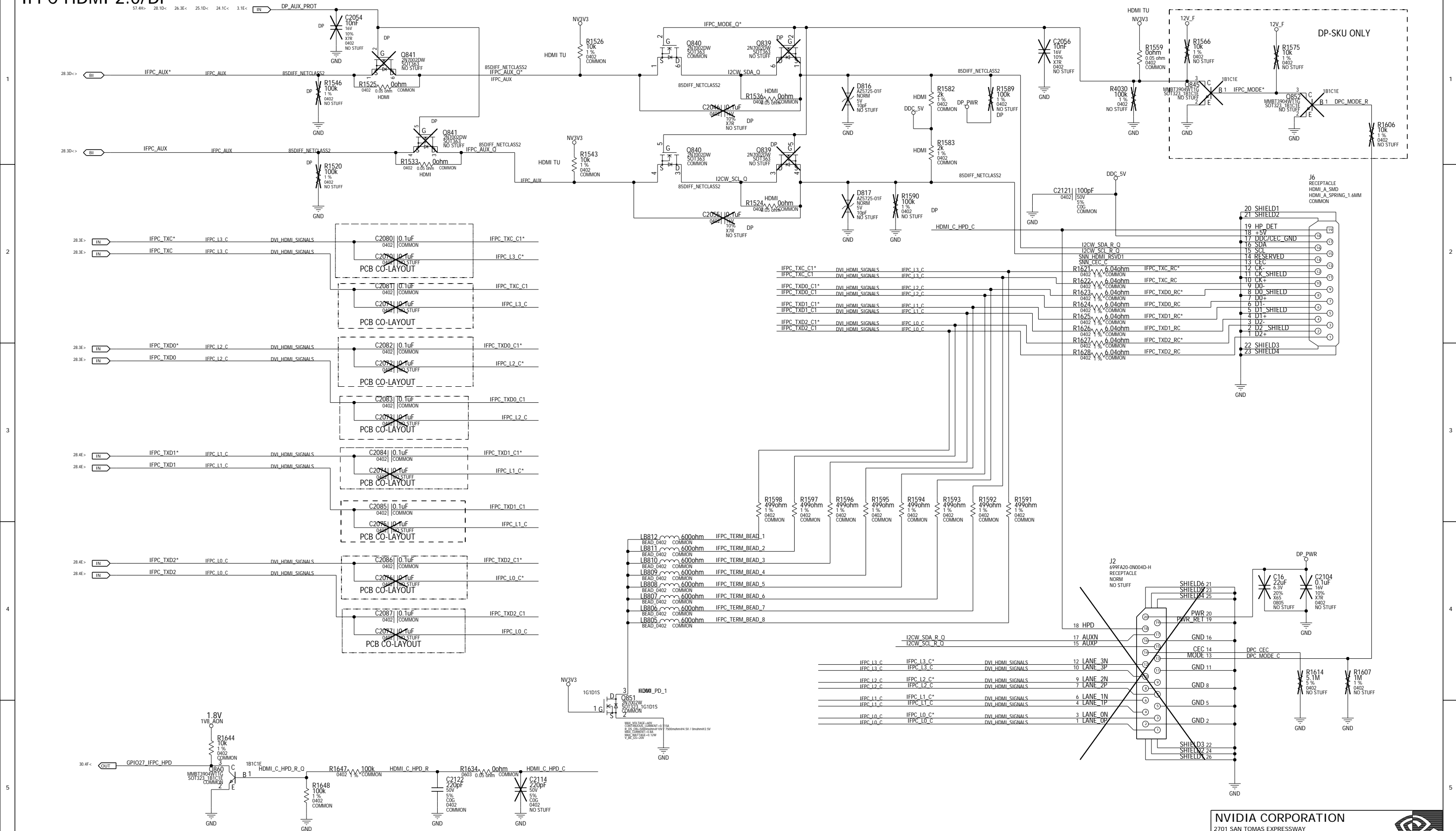
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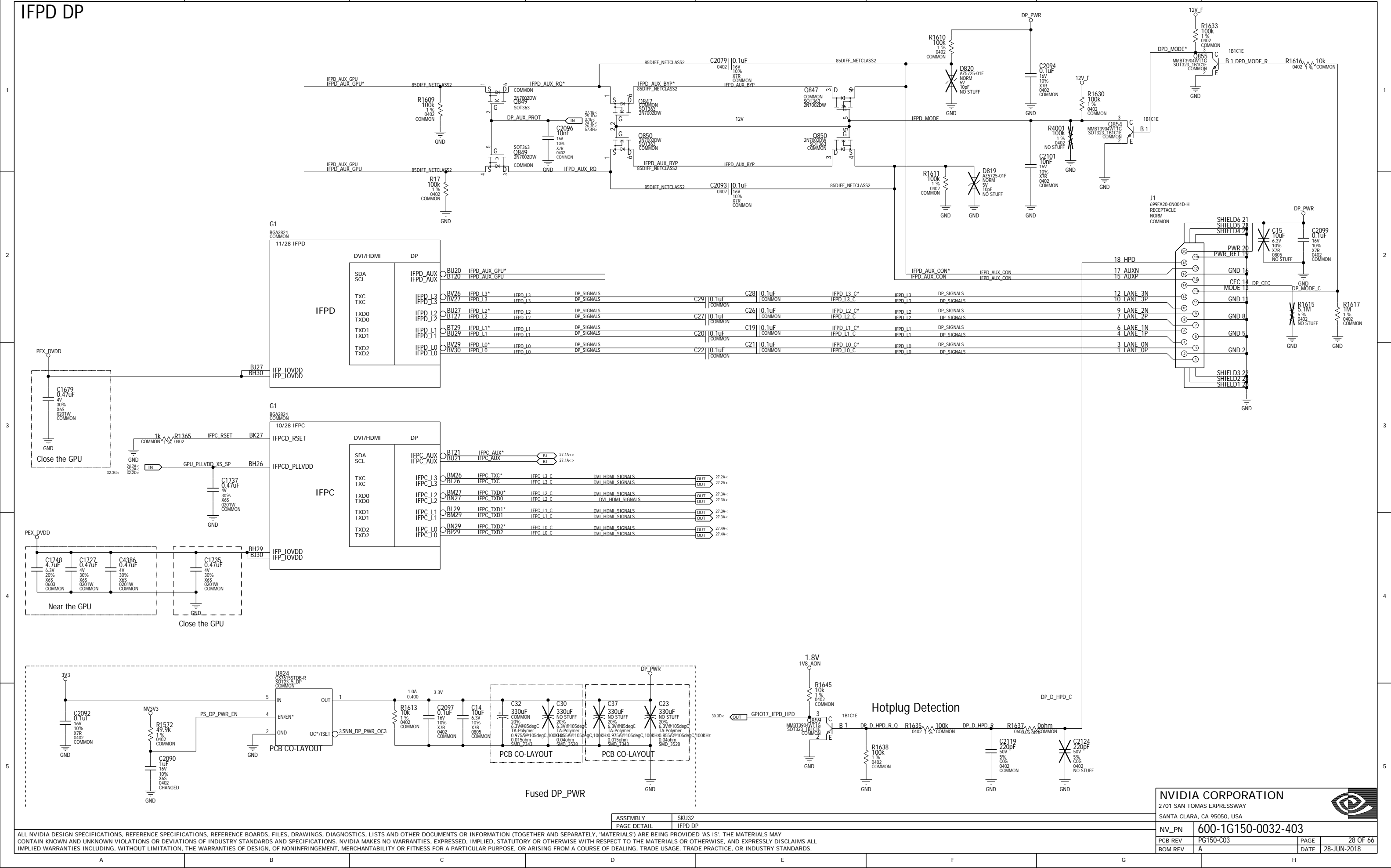


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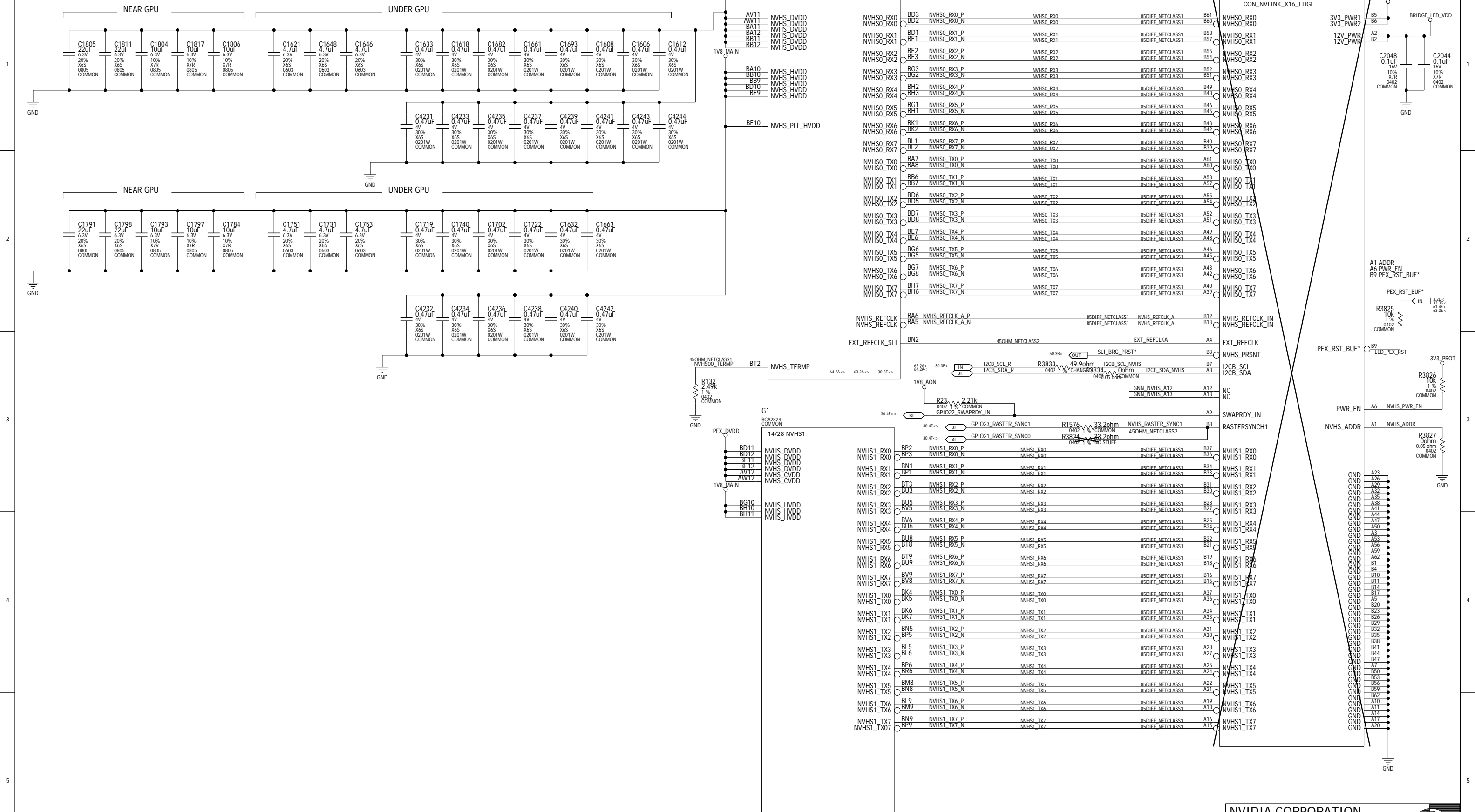
ASSEMBLY	SKU32
PAGE DETAIL	IFPC HDMI/DP

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IFPD DP




NVHS Interface and FRAME LOCK

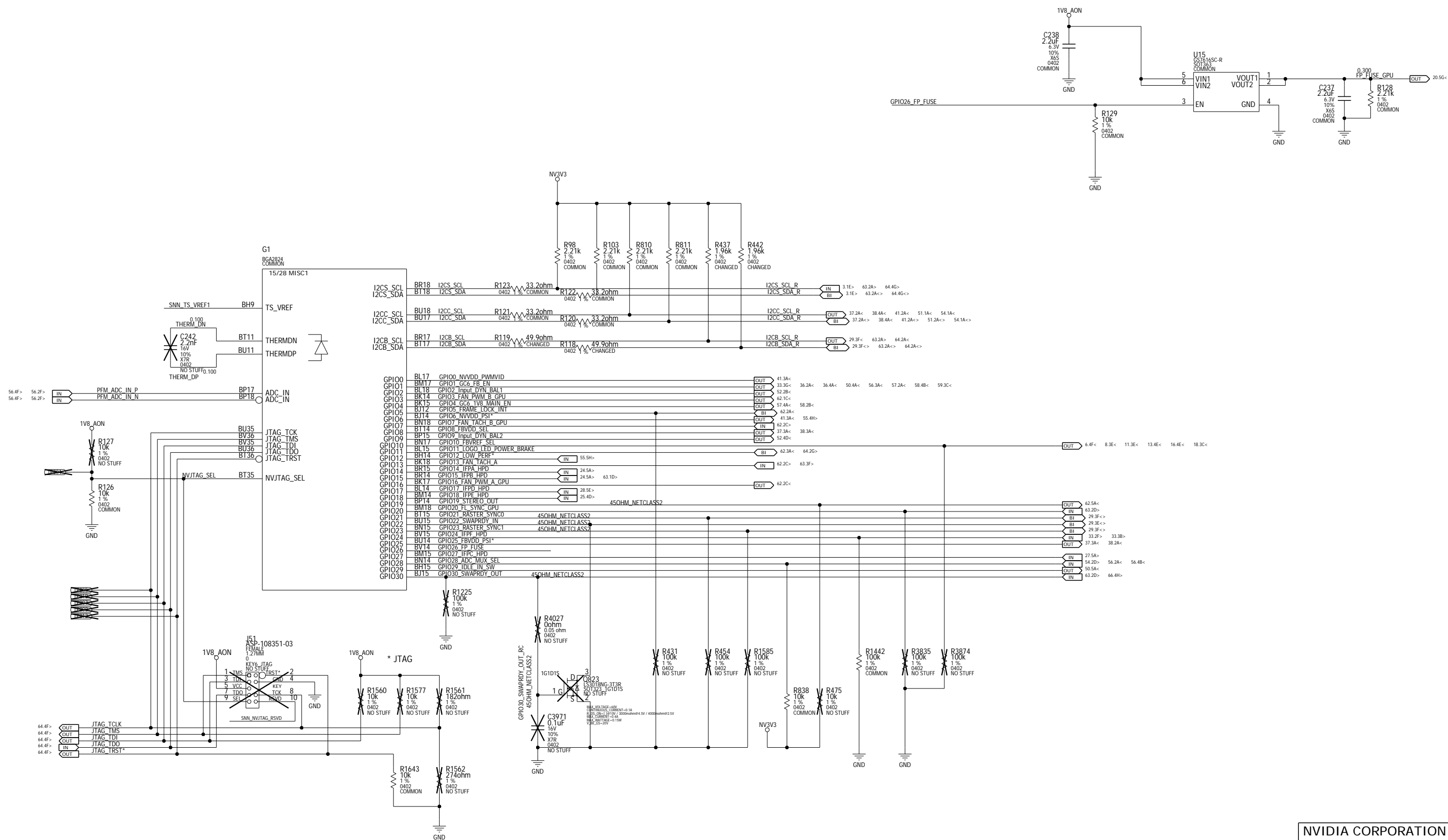



ASSEMBLY	SKU32
PAGE DETAIL	NVHS X16

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MISC1: Fan, Thermal, JTAG, GPIO, STEREO



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MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
H	L	H	00101
H	H	L	00110
H	H	H	00111
L	L	M	01000
L	M	L	01001

DEFAULT

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	H	XXX0	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

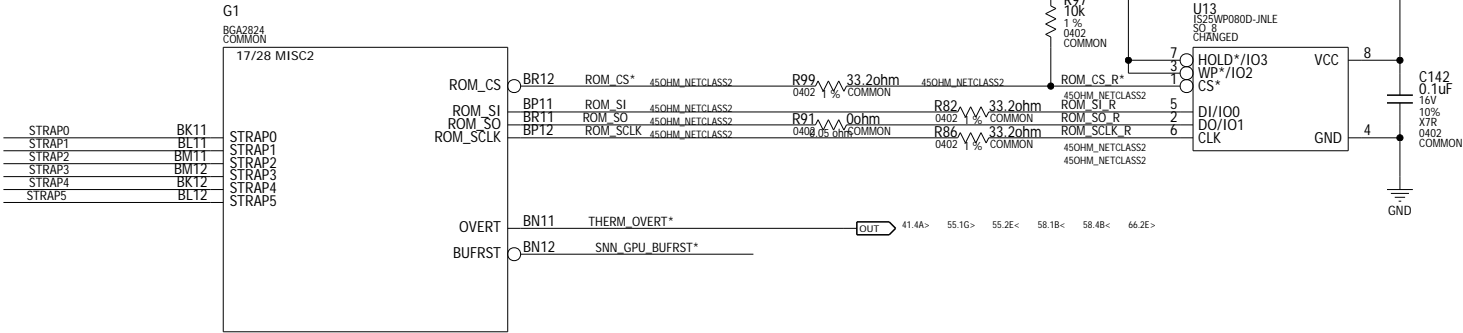
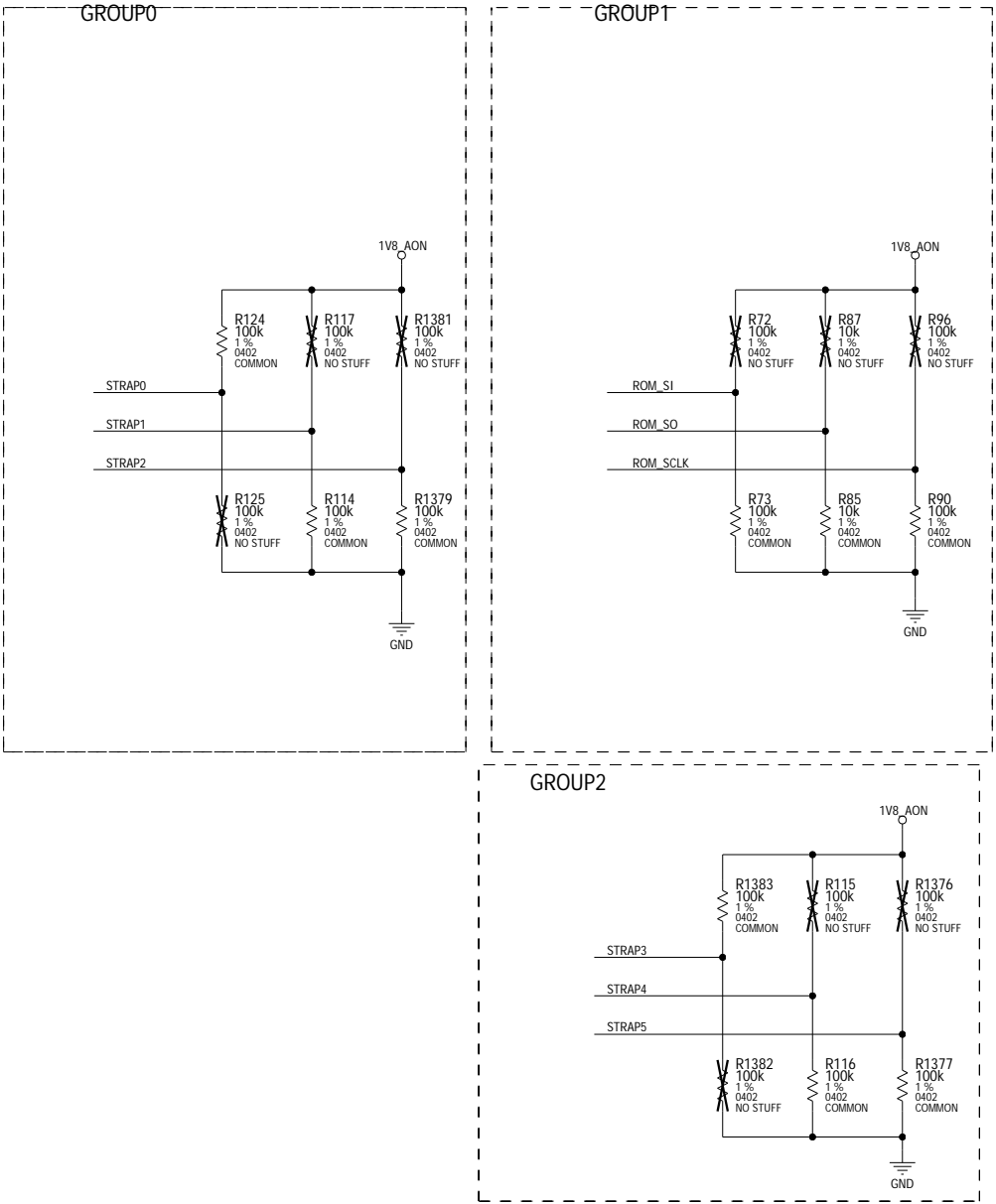
SKU 200

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

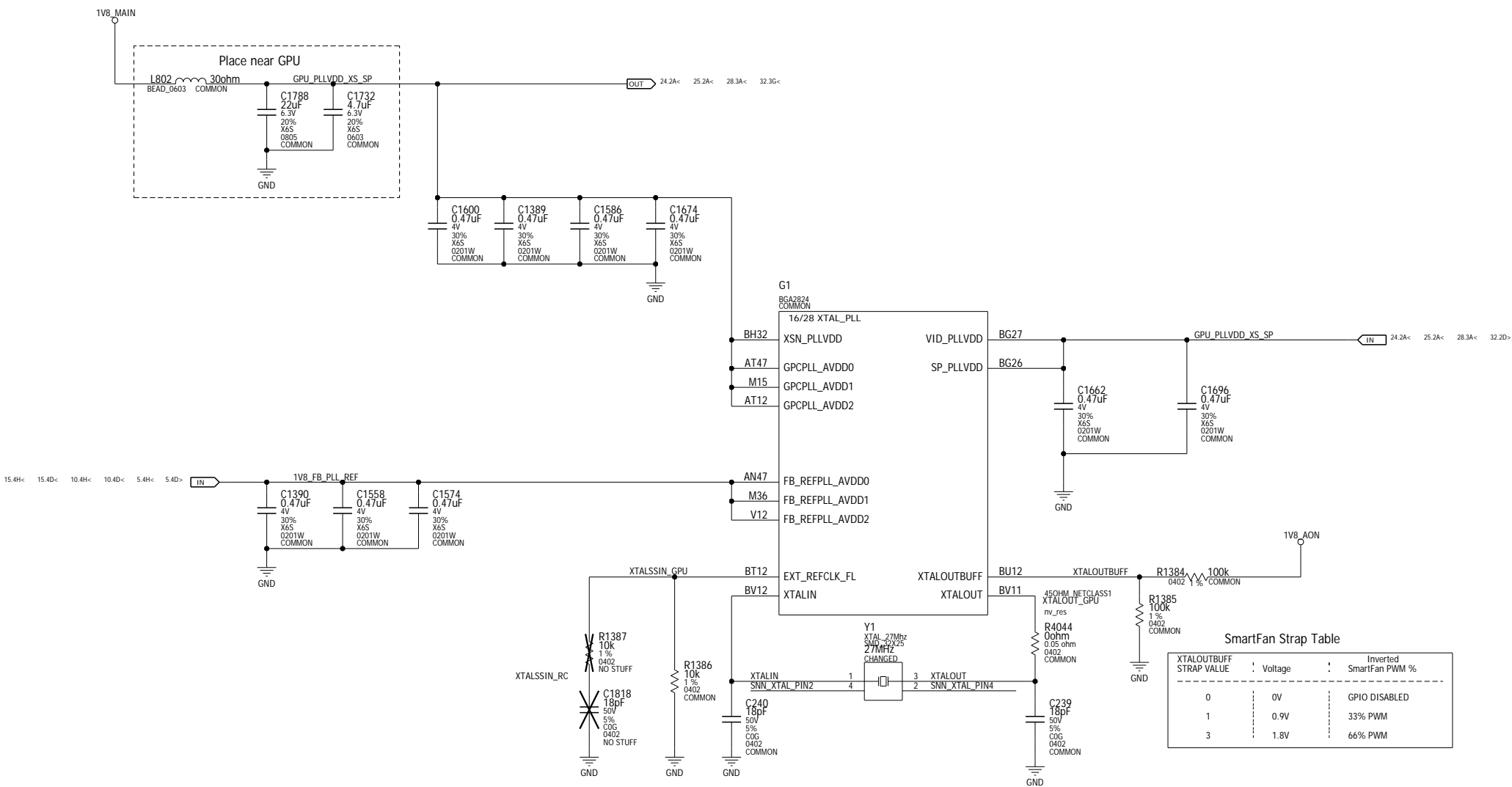
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



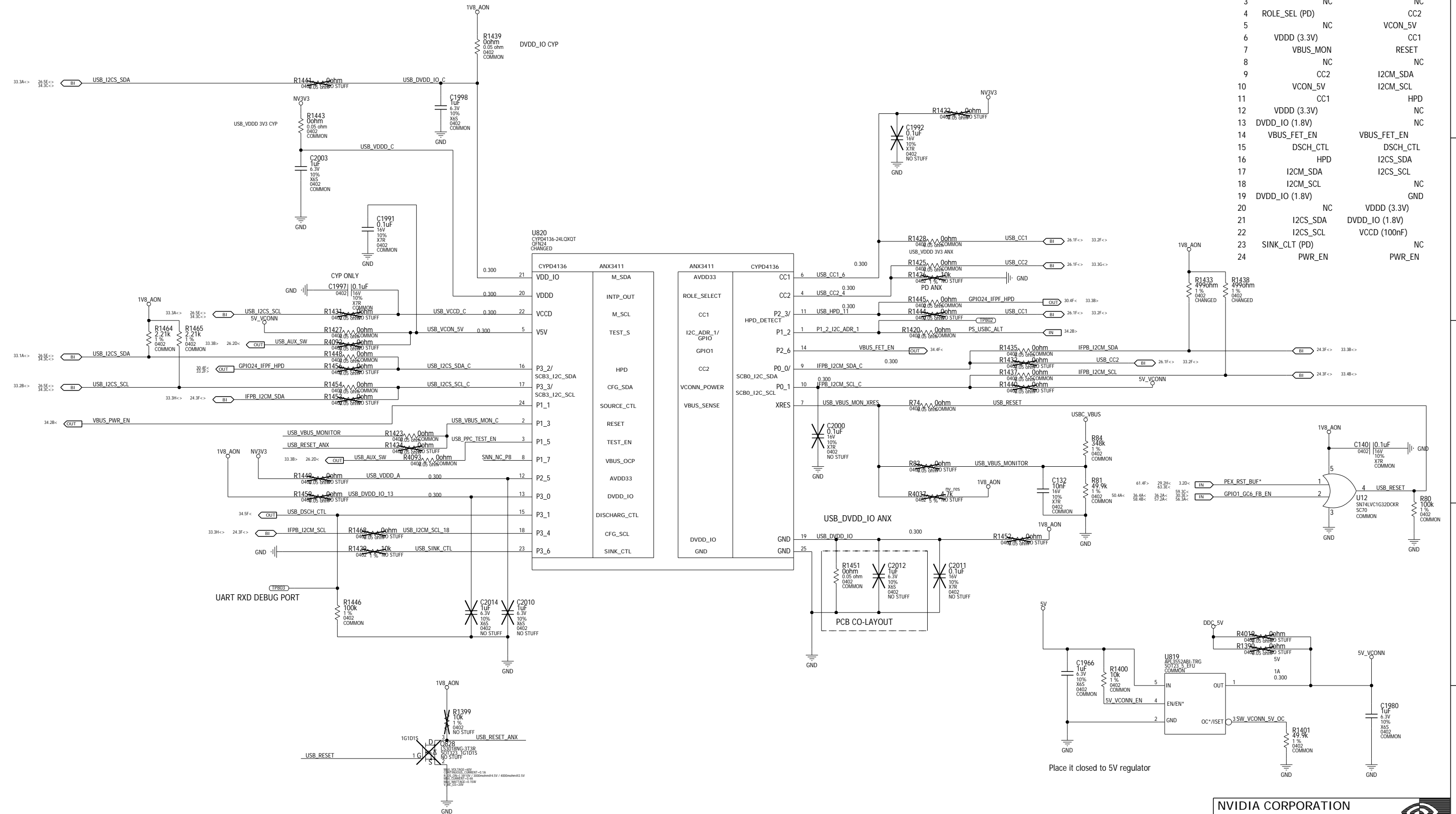
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MISC2: XTAL. PLL



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MISC: USB PPC



PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN

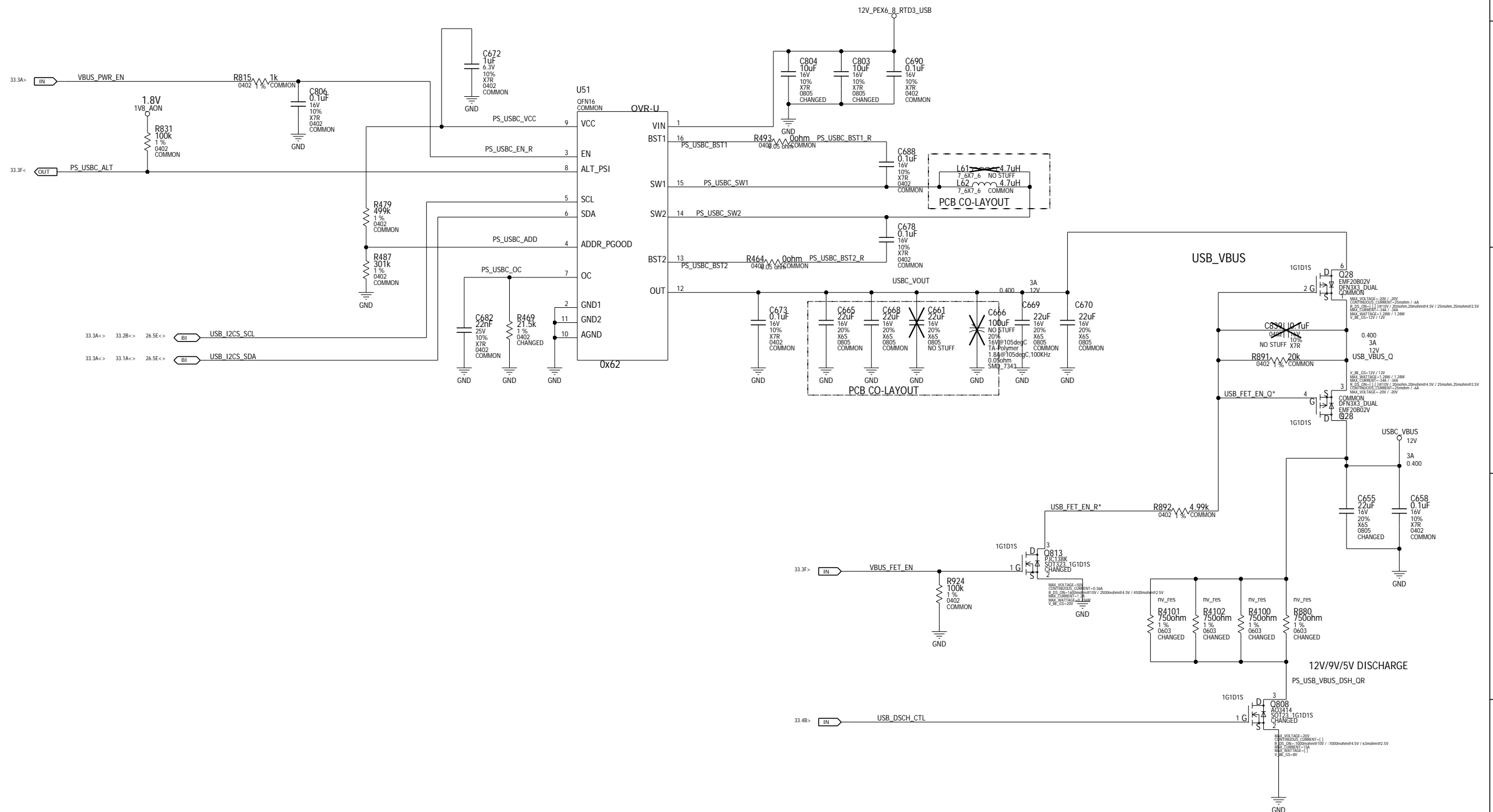
ASSEMBLY	SKU32
PAGE DETAIL	MISC: USB PPC


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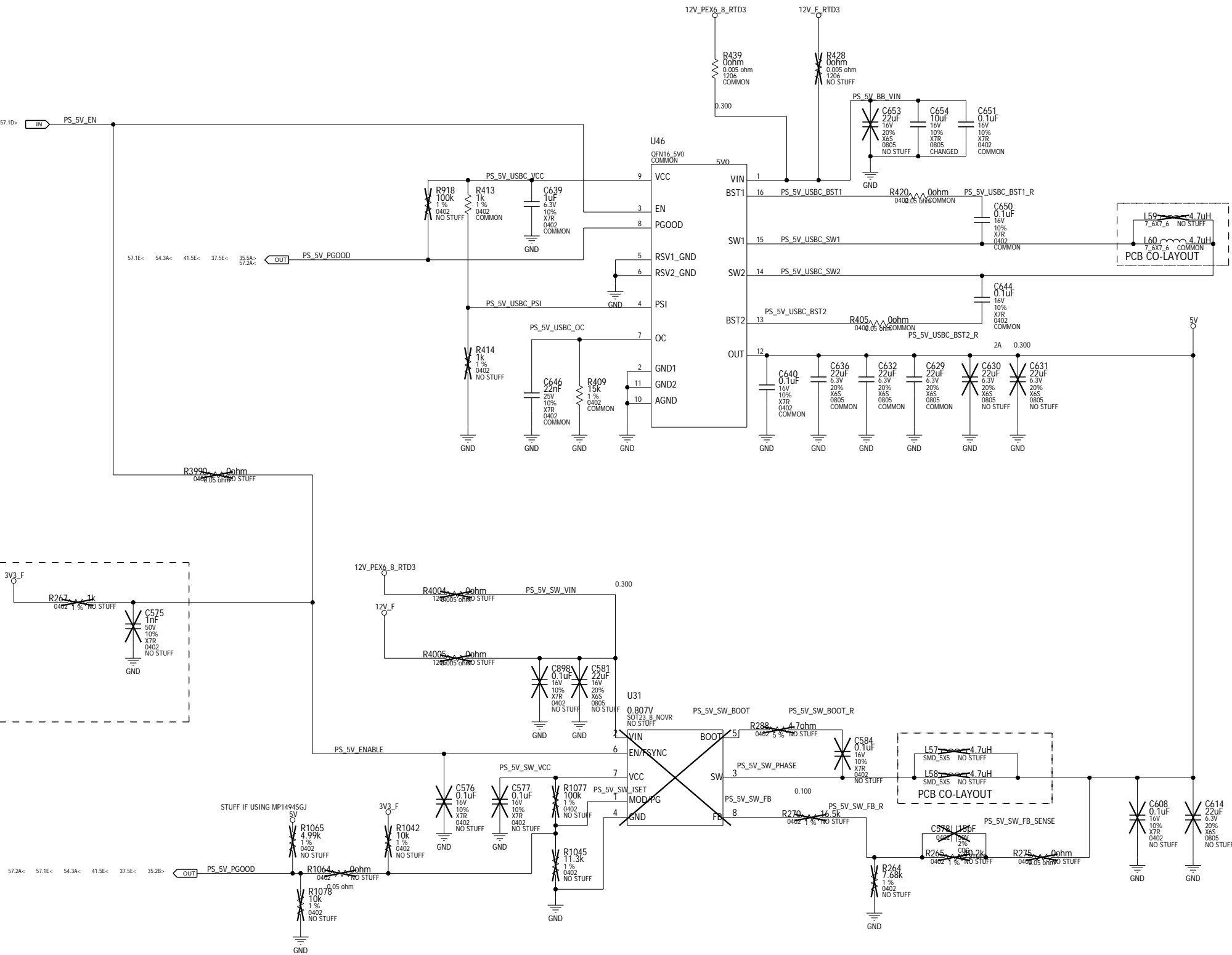
PS: USB VR



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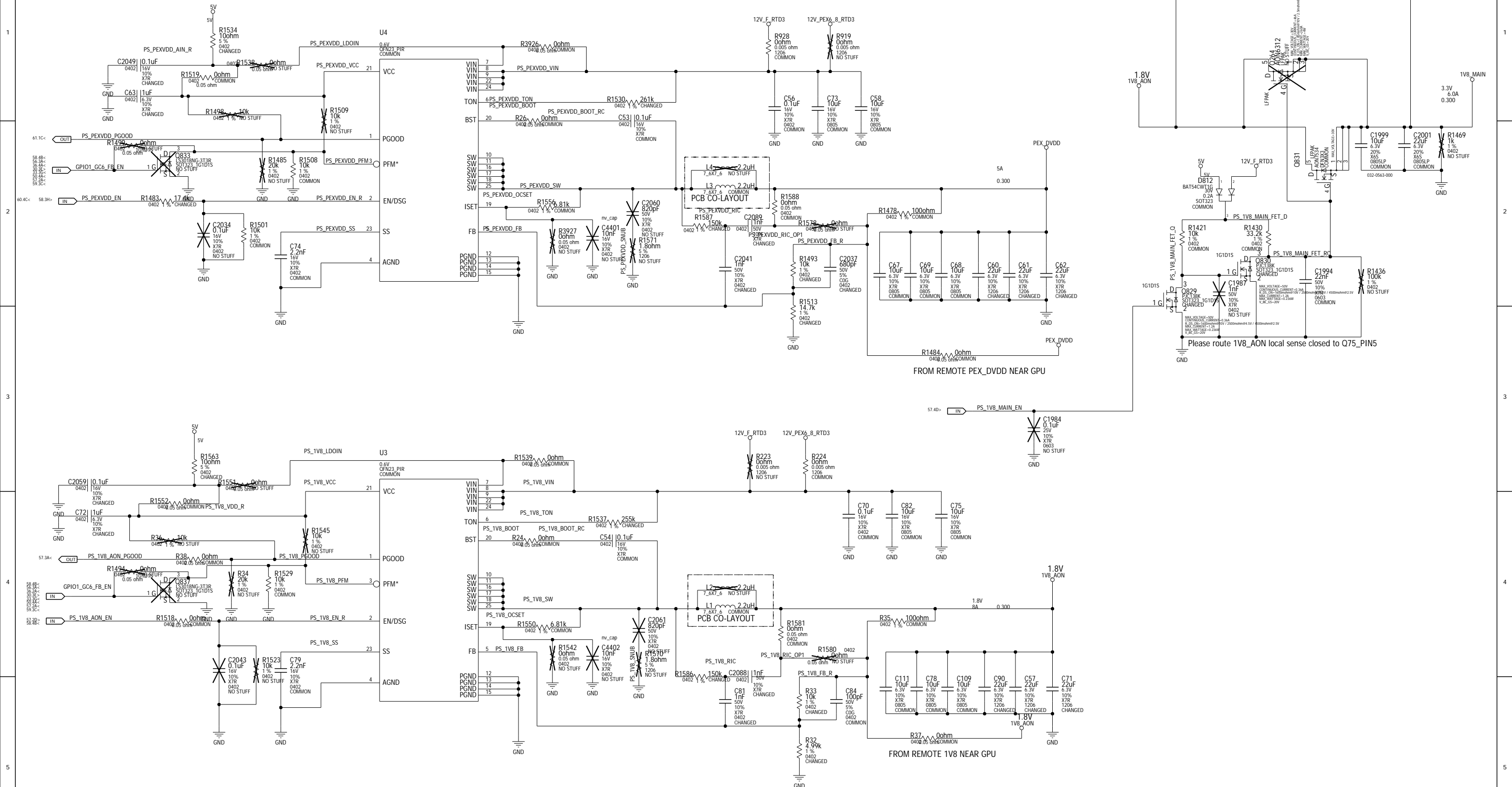
PS: 5V, 5V_BACKUP




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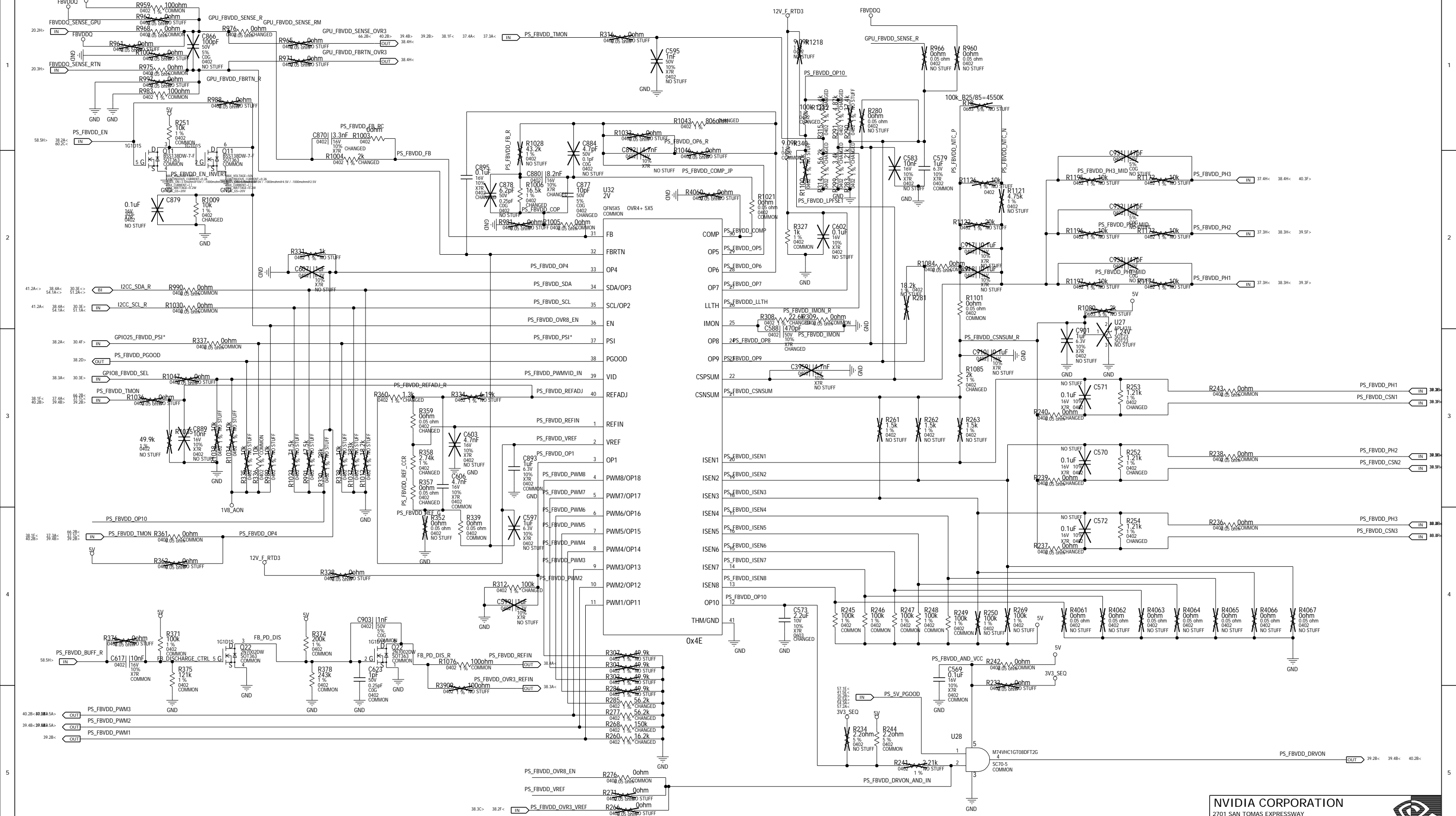
PS: PEXVDD 1V8 Rail



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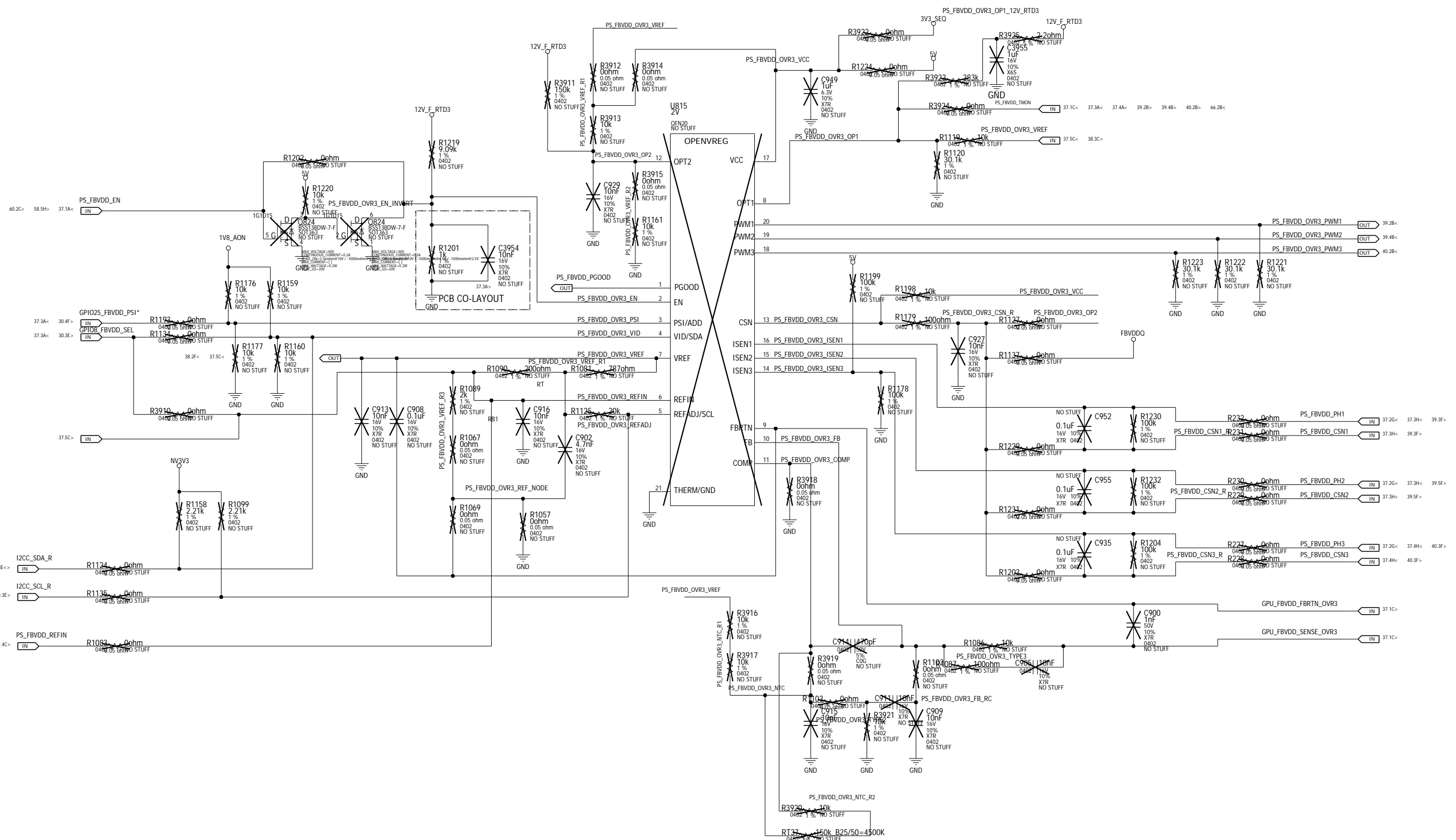
PS: FBVDD Controller



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ASSEMBLY	SKU32
PAGE DETAIL	PS: FBVDD Controller

PS: FBVDD Controller OVR3



ASSEMBLY	SKU32
PAGE DETAIL	PS: FBVDD Controller OVR3

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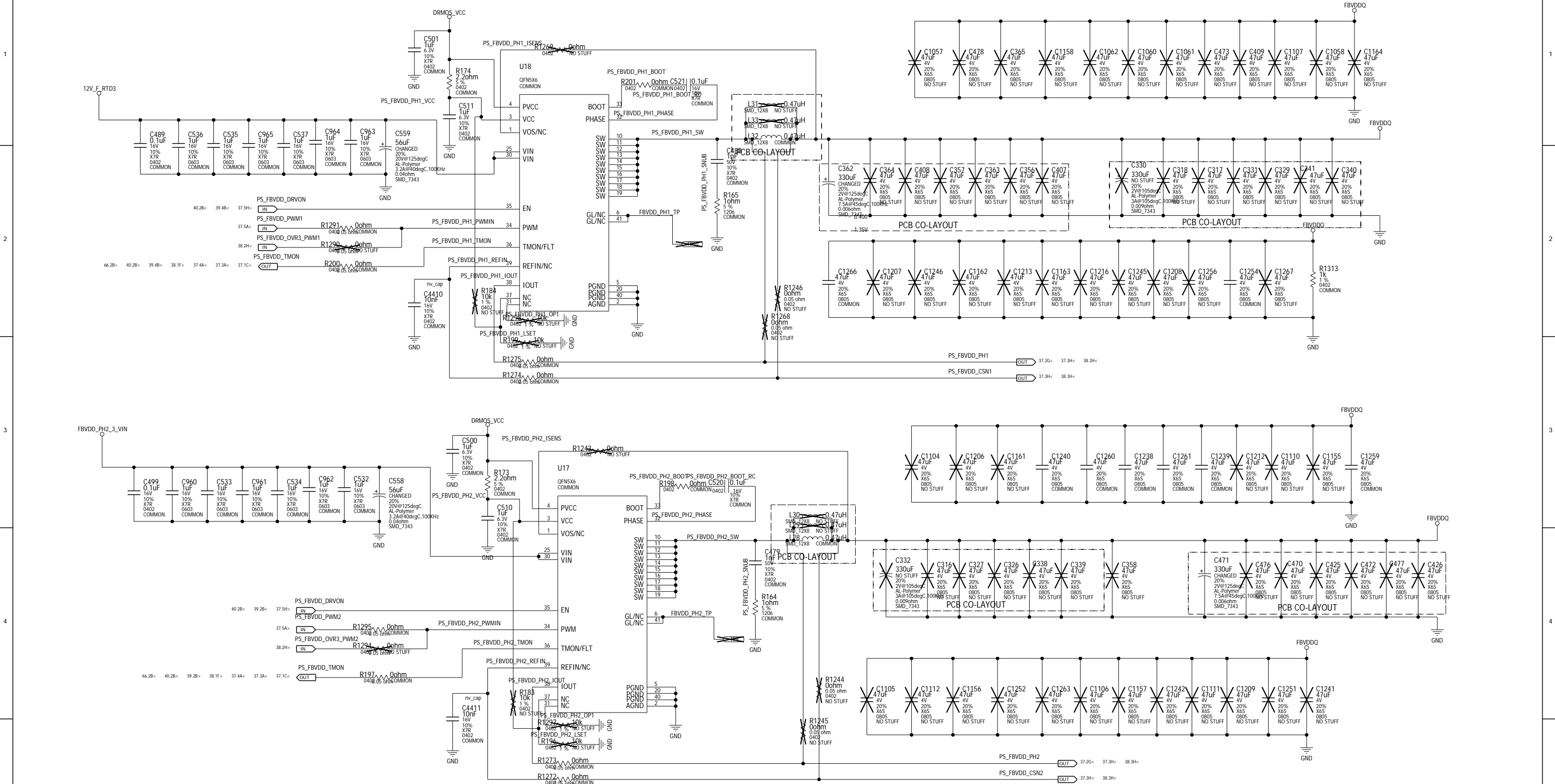
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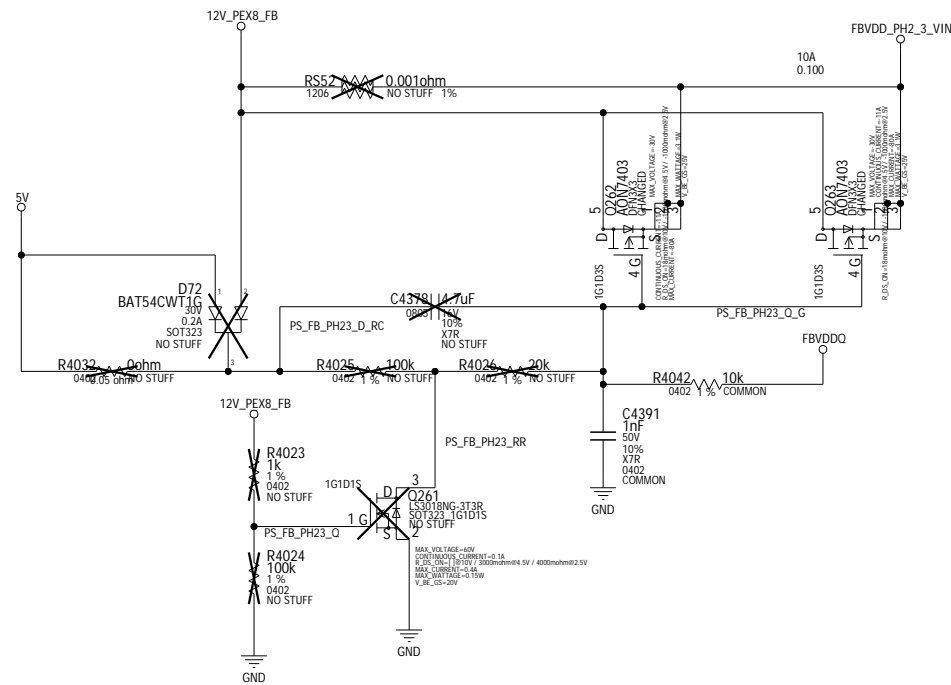
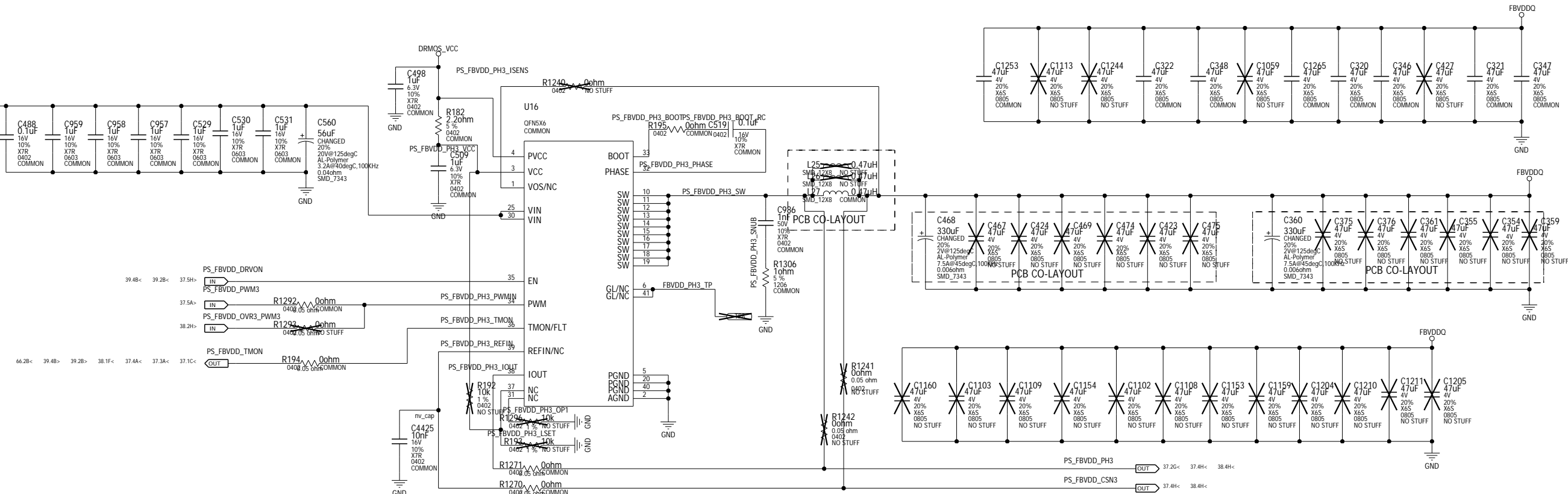


PS: FBVDD PH1, 2



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PS: FBVDD PH3



ASSEMBLY	SKU32
PAGE DETAIL	PS: FBVDD Phase 3

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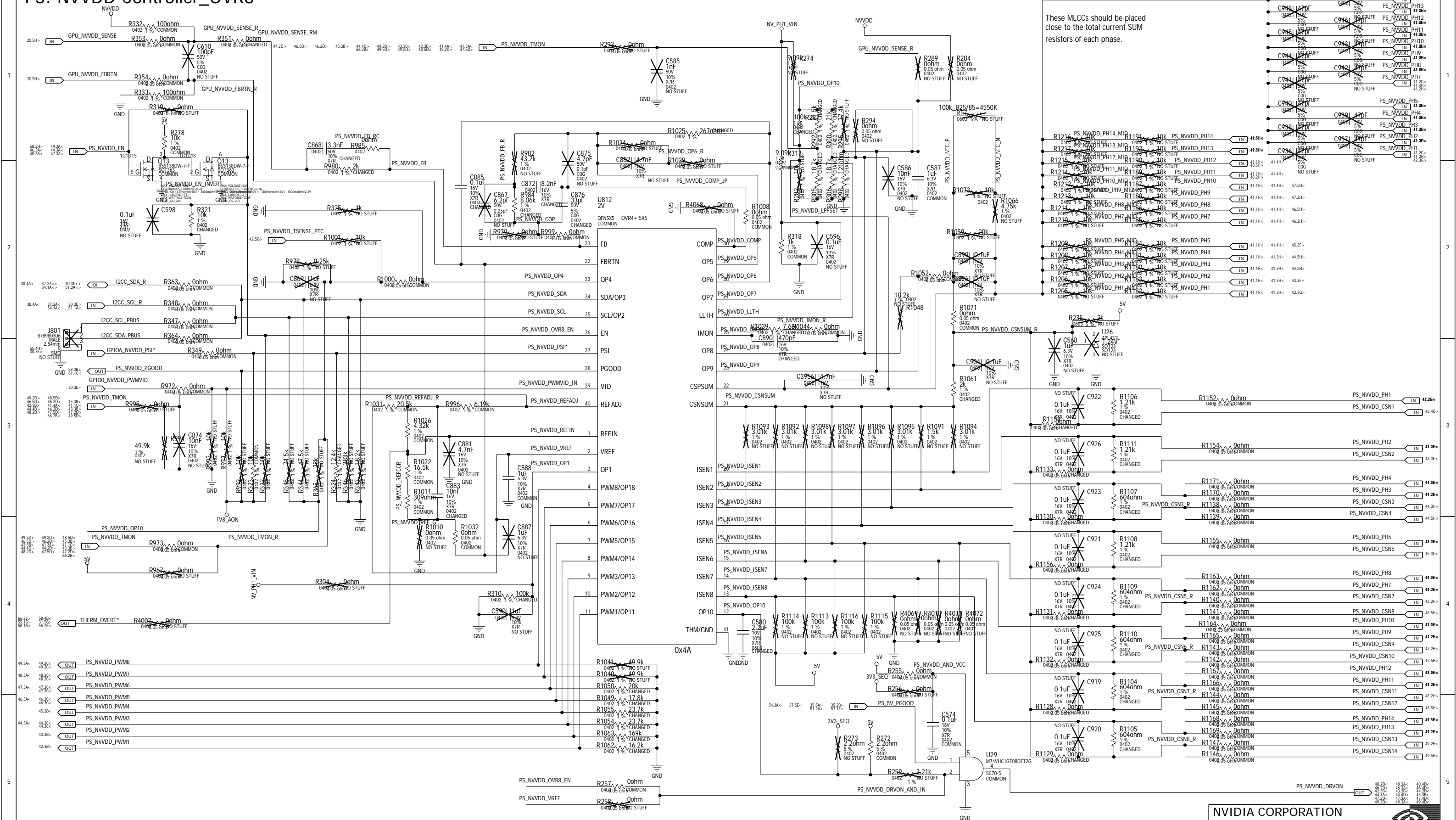
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PS: NVVDD Controller_OVR8



These MLCCs should be placed close to the total current SUM resistors of each phase.

ASSEMBLY	SKU32
PAGE DETAIL	PS: NVVDD Controller_OVR8

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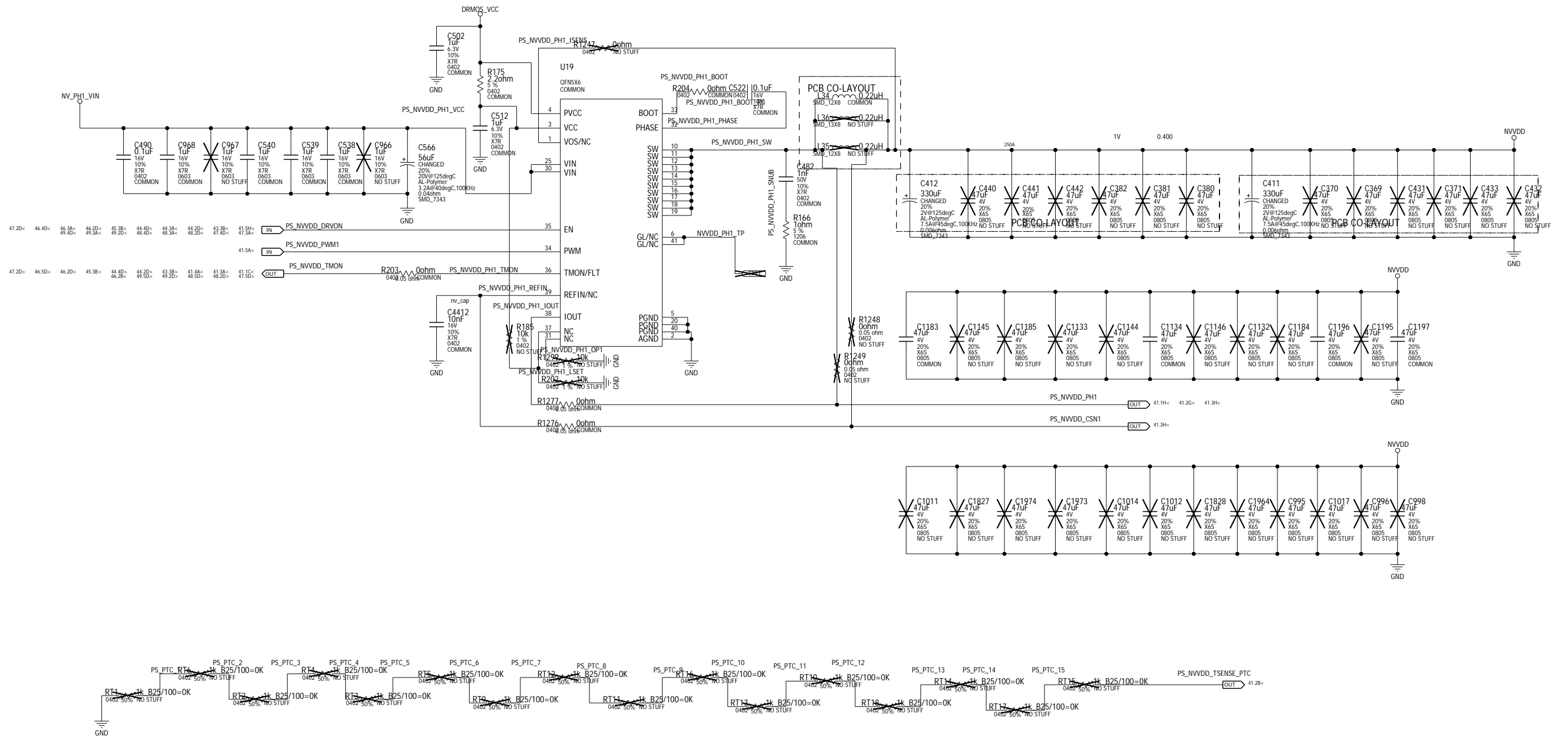
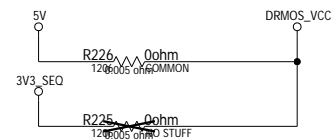
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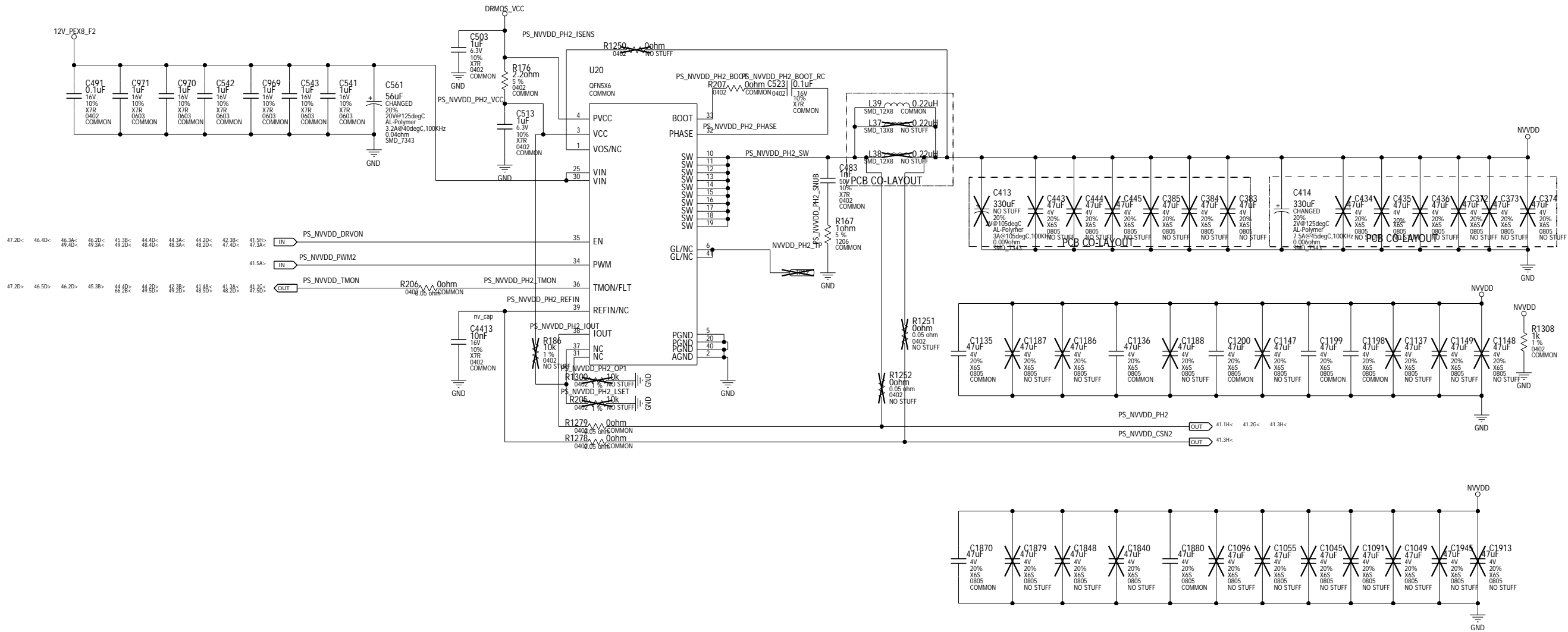
PS: NVVDD Phase 1



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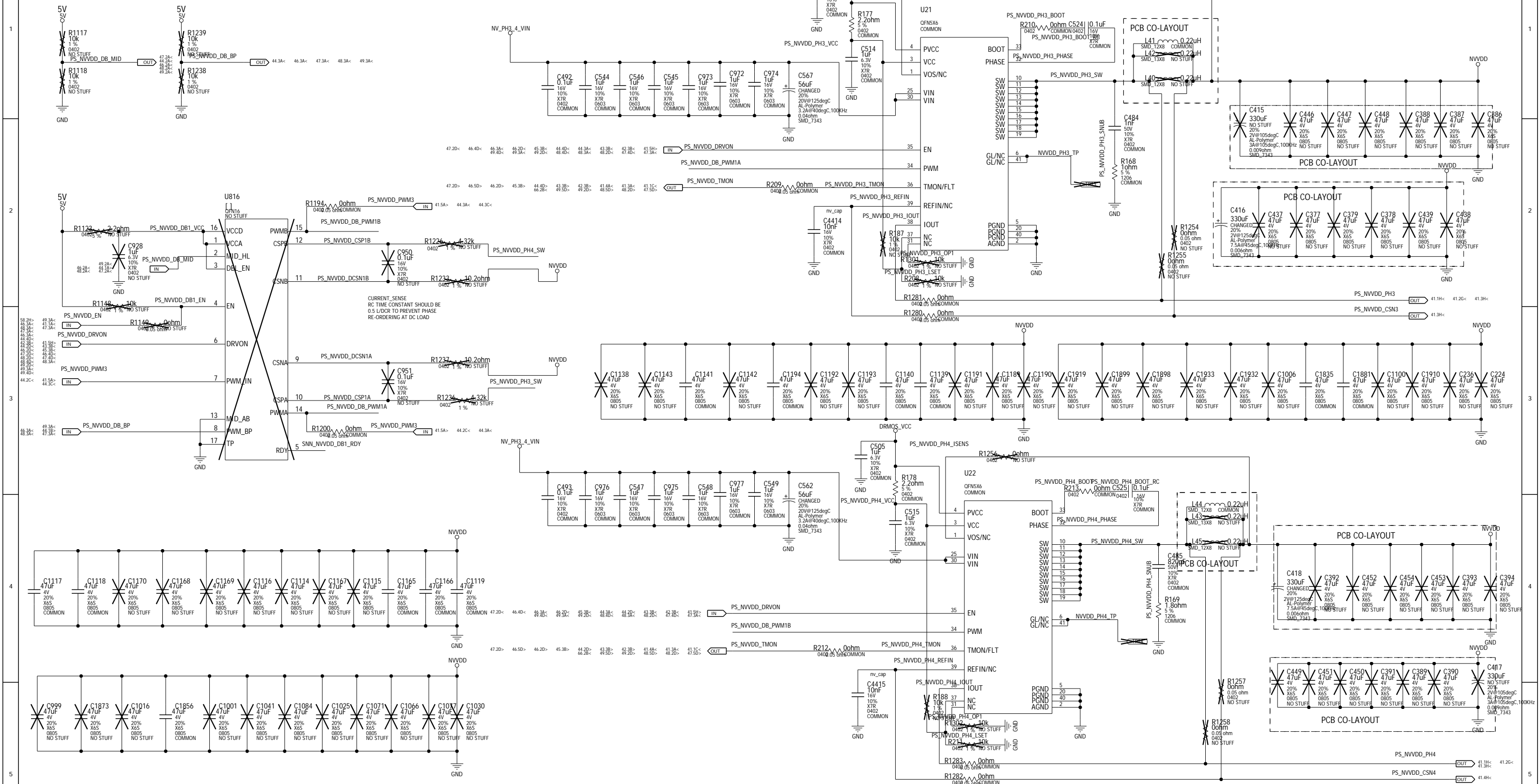
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PS: NVVDD Phase 2



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PS: NVVDD Phase 3, 4



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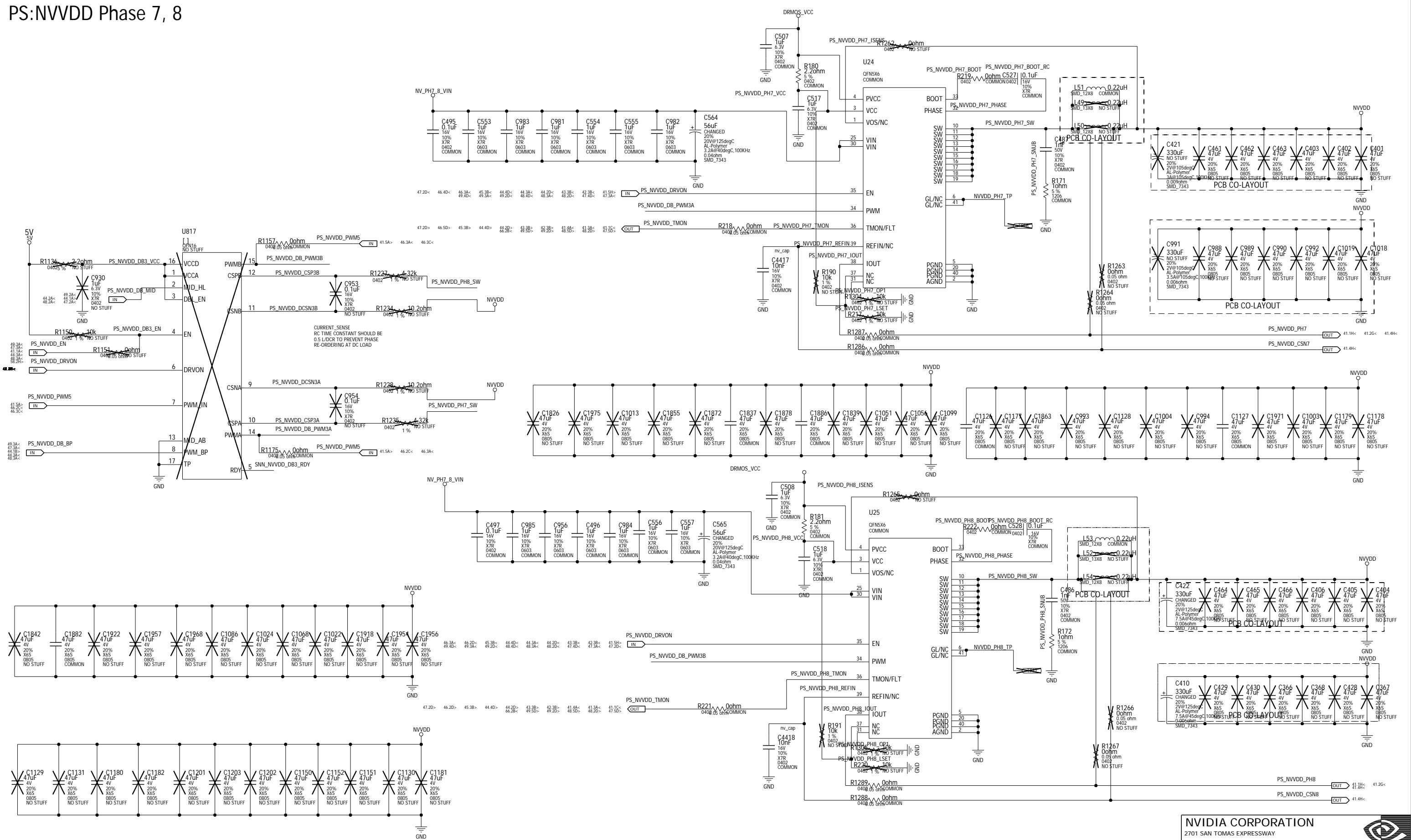
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PS:NVVDD Phase 7, 8

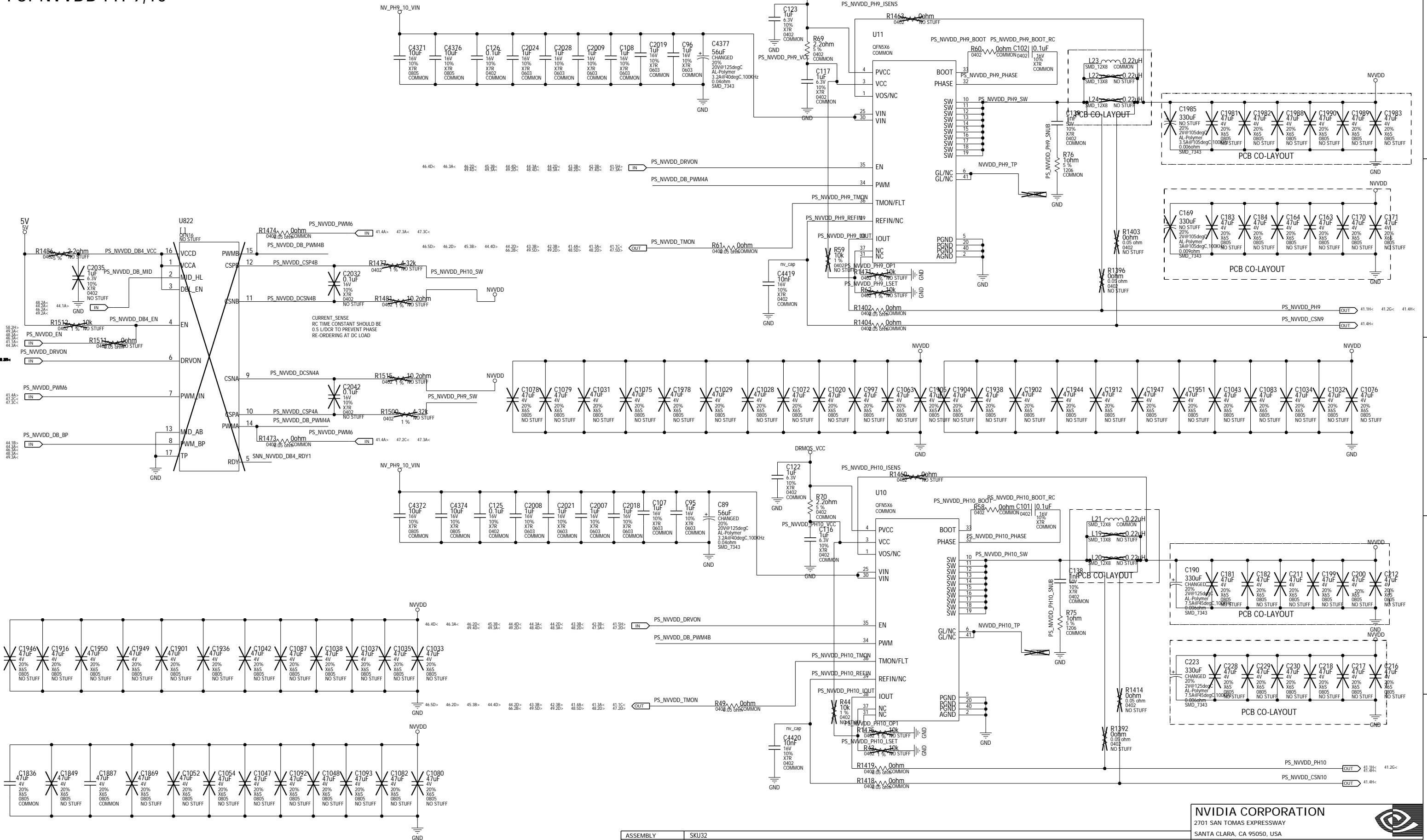


ASSEMBLY	SKU32
PAGE DETAIL	PS: NVVDD Phase 7, 8

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PS: NVVDD PH 9,10

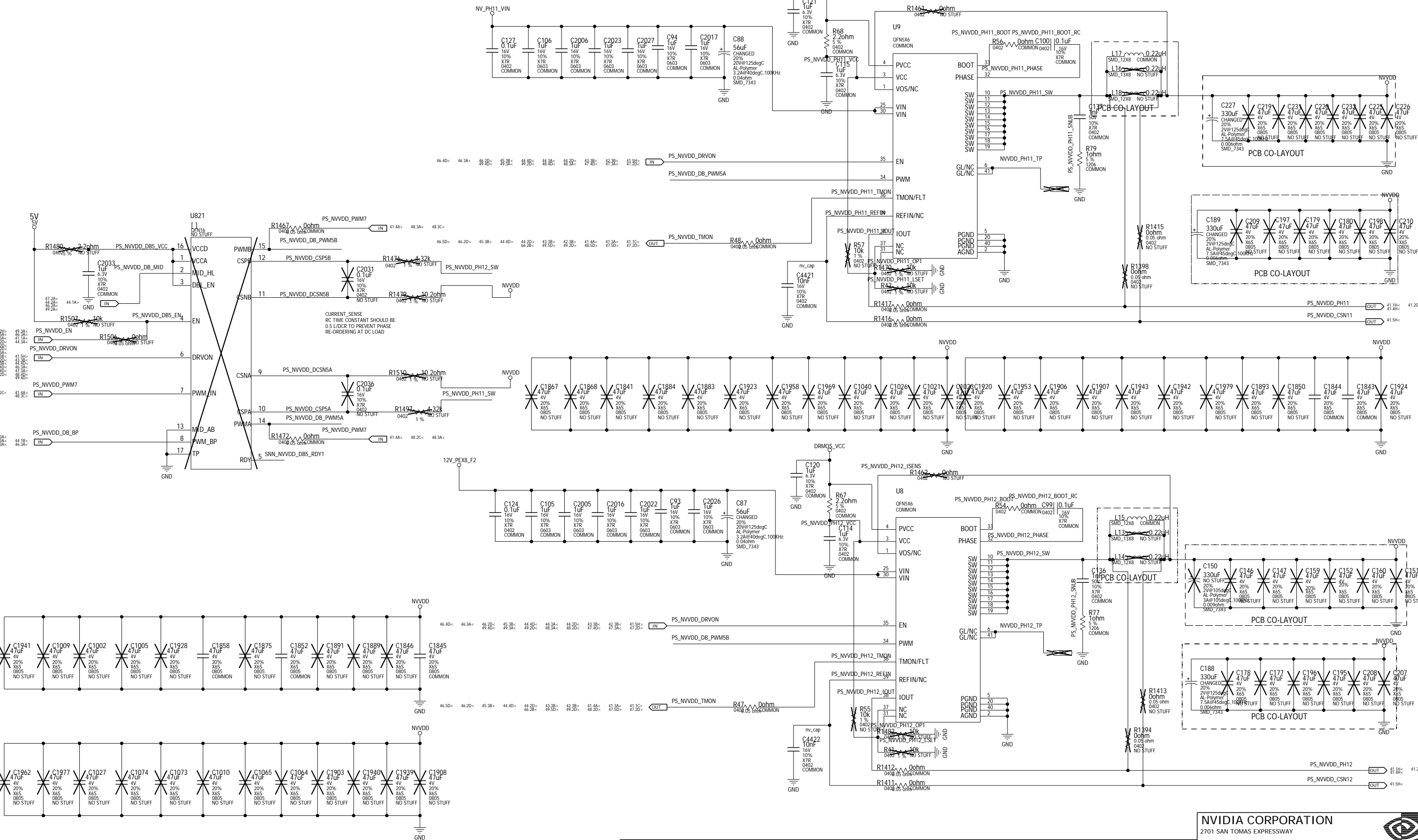


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ASSEMBLY	SKU32
PAGE DETAIL	PS: NVVDD Phase 9, 10

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PS: NVVDD PH 11,12



ASSEMBLY	SKU32
PAGE DETAIL	PS: NVVDD Phase 11, 12

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PS: NVVDD PH 13,14

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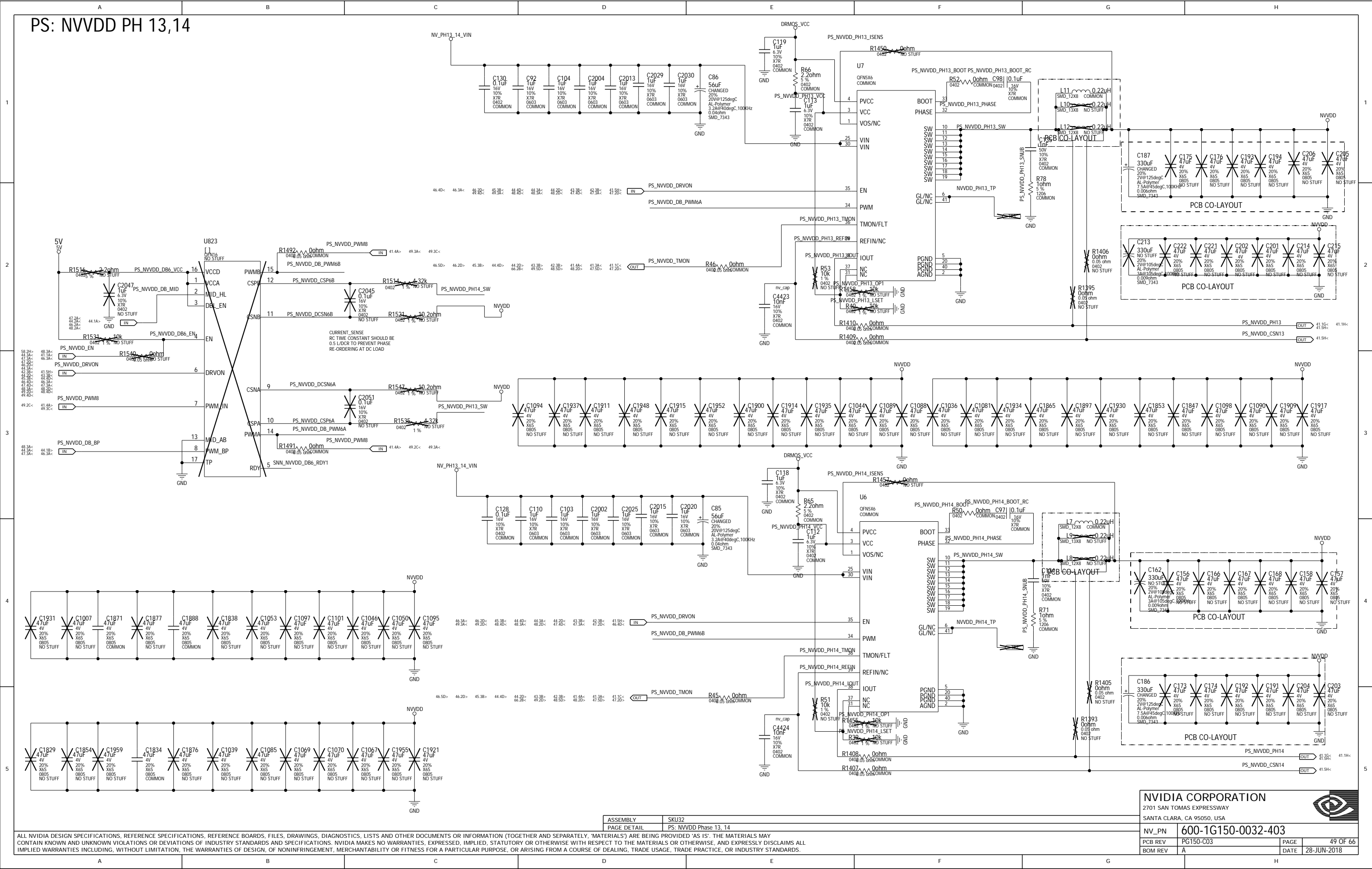
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ASSEMBLY	SKU32
PAGE DETAIL	PS: NVVDD Phase 13, 14

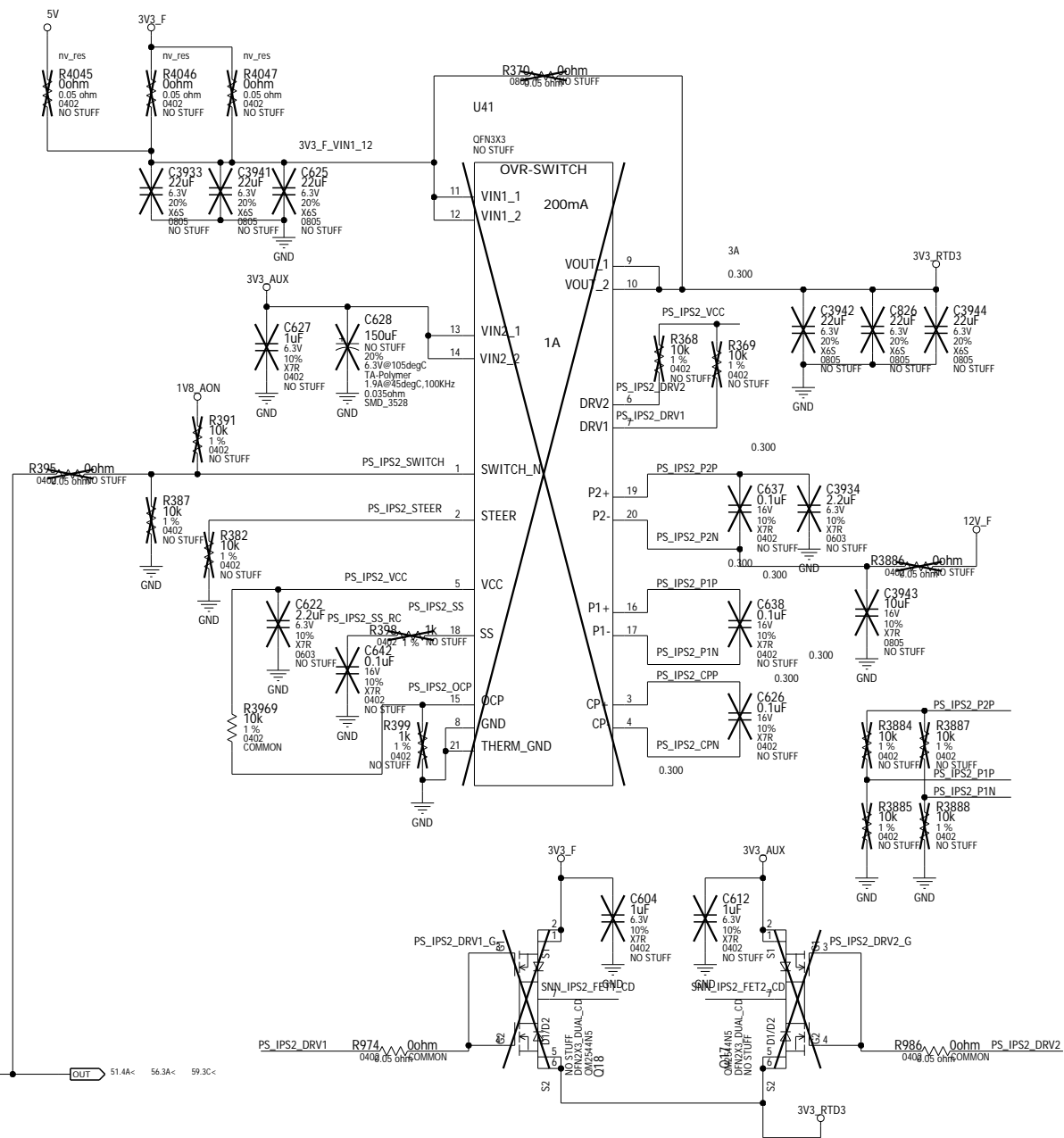
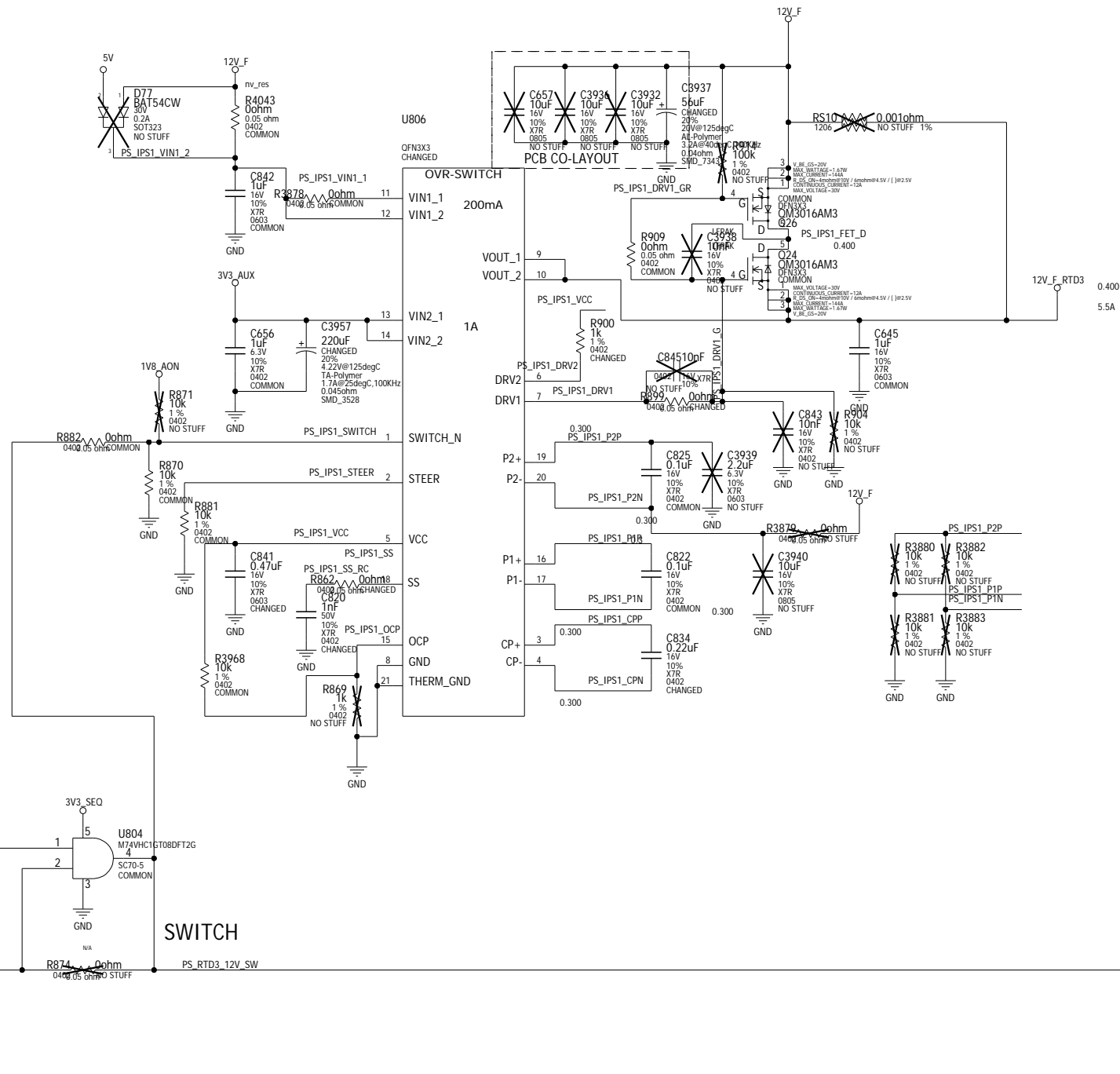
PS: INPUT SWITCH RTD3

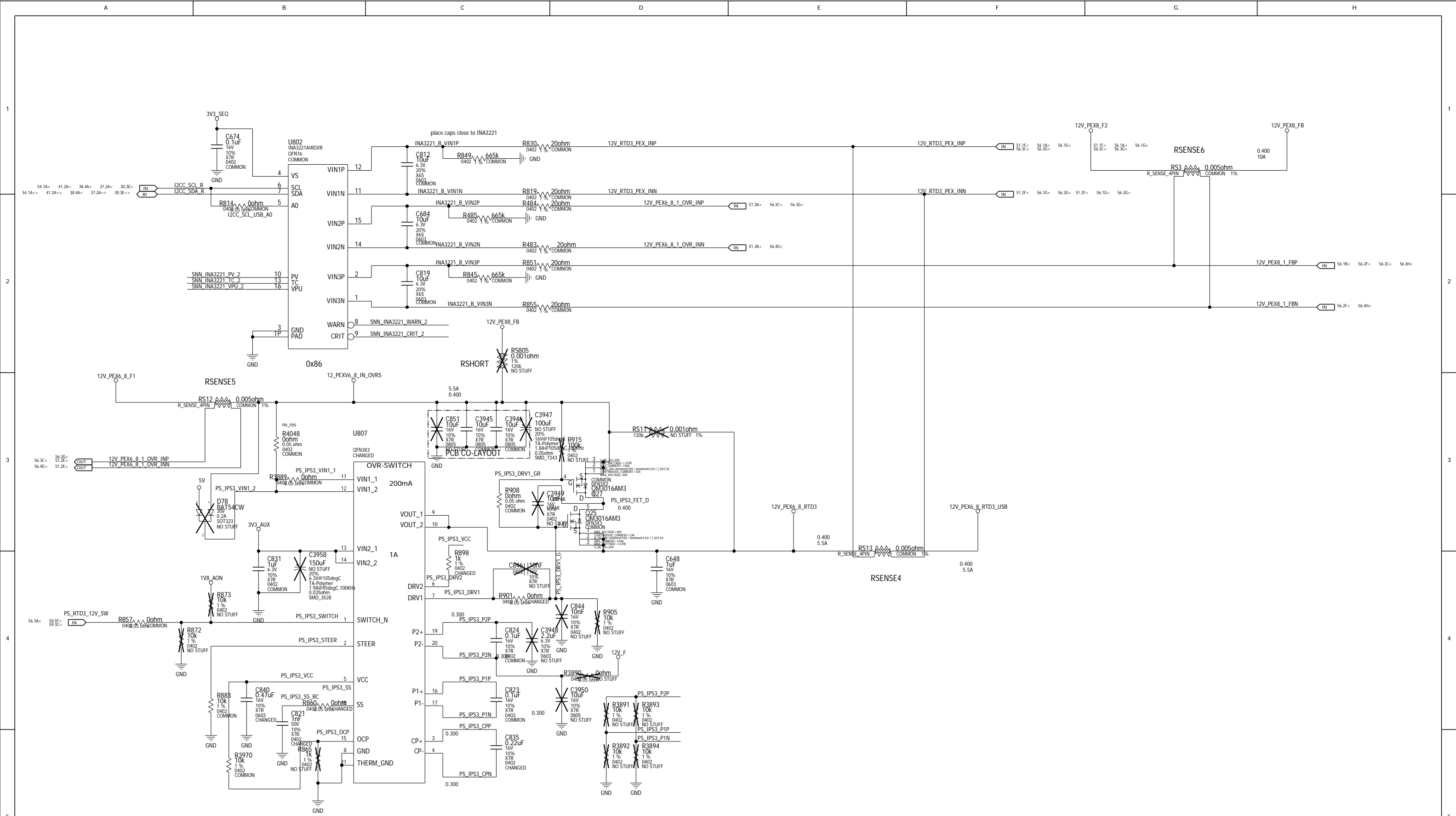
AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

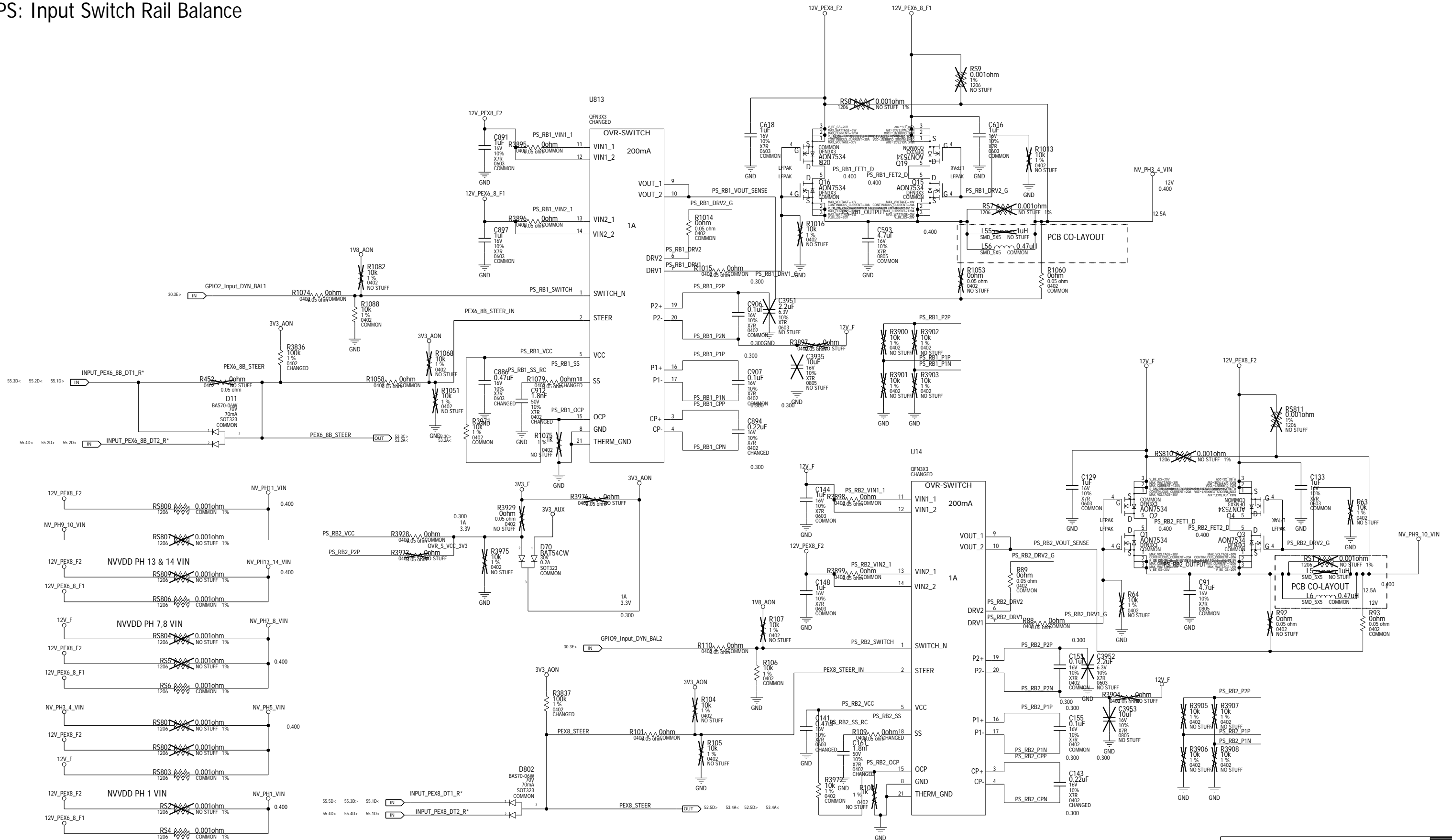
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A





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PS: Input Switch Rail Balance



ASSEMBLY	SKU32
PAGE DETAIL	PS: INPUT SWITCH RAIL BALANCE

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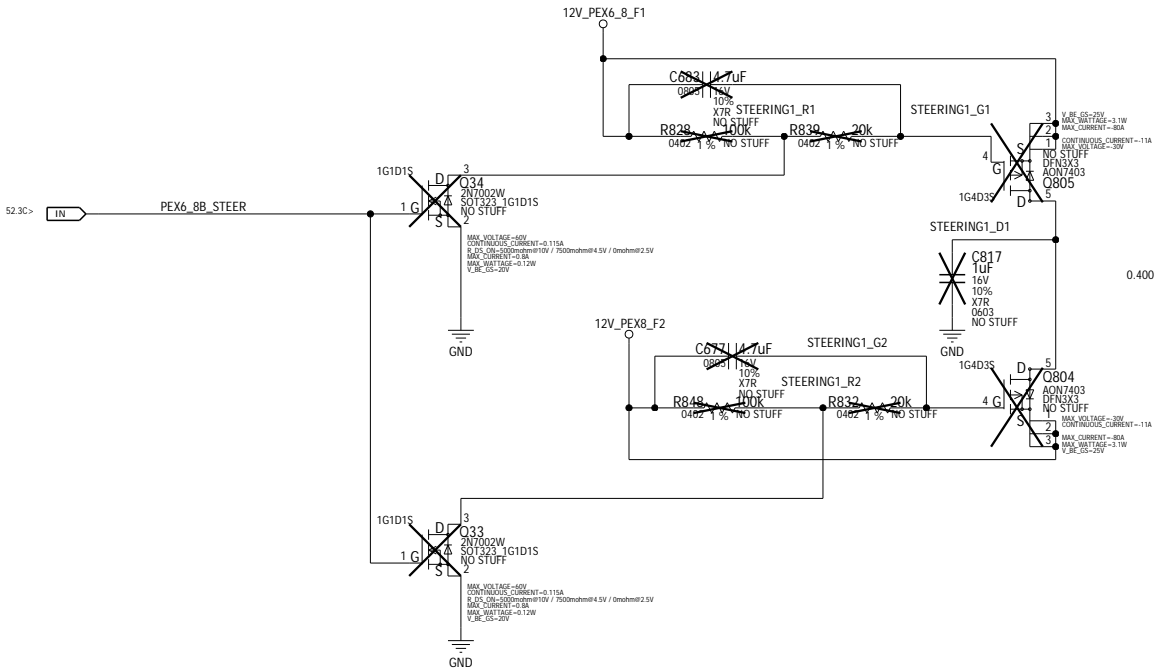
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NV_PN	600-1G150-0032-403
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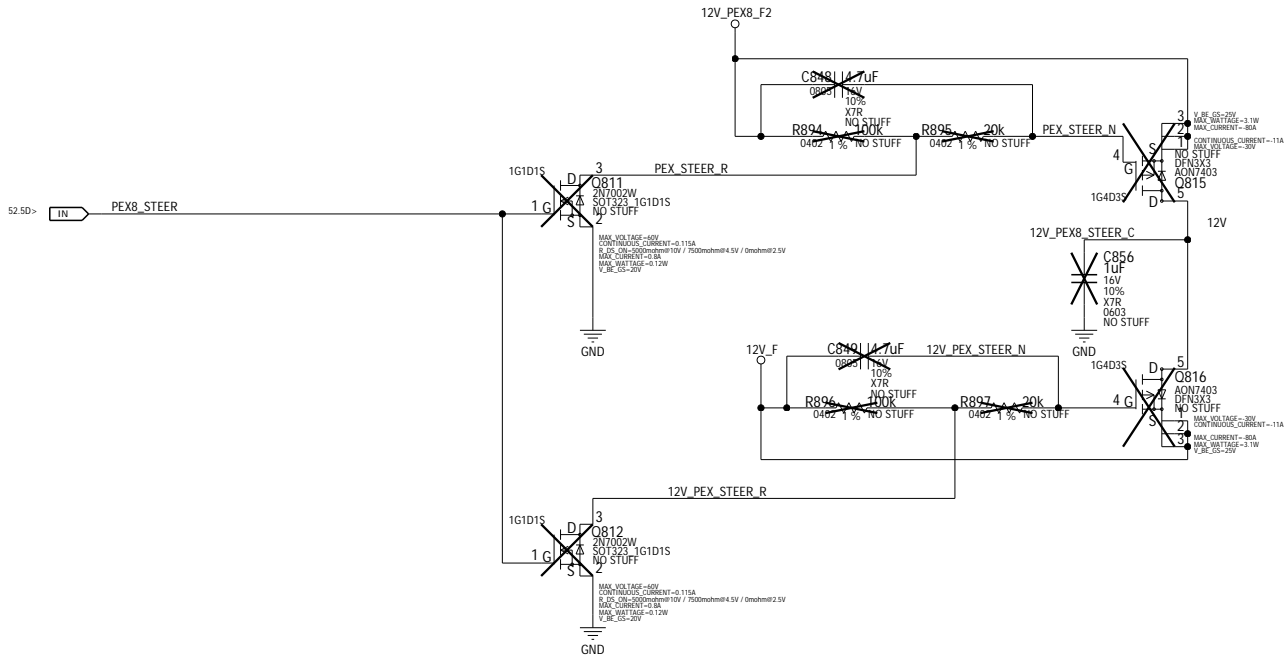
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12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



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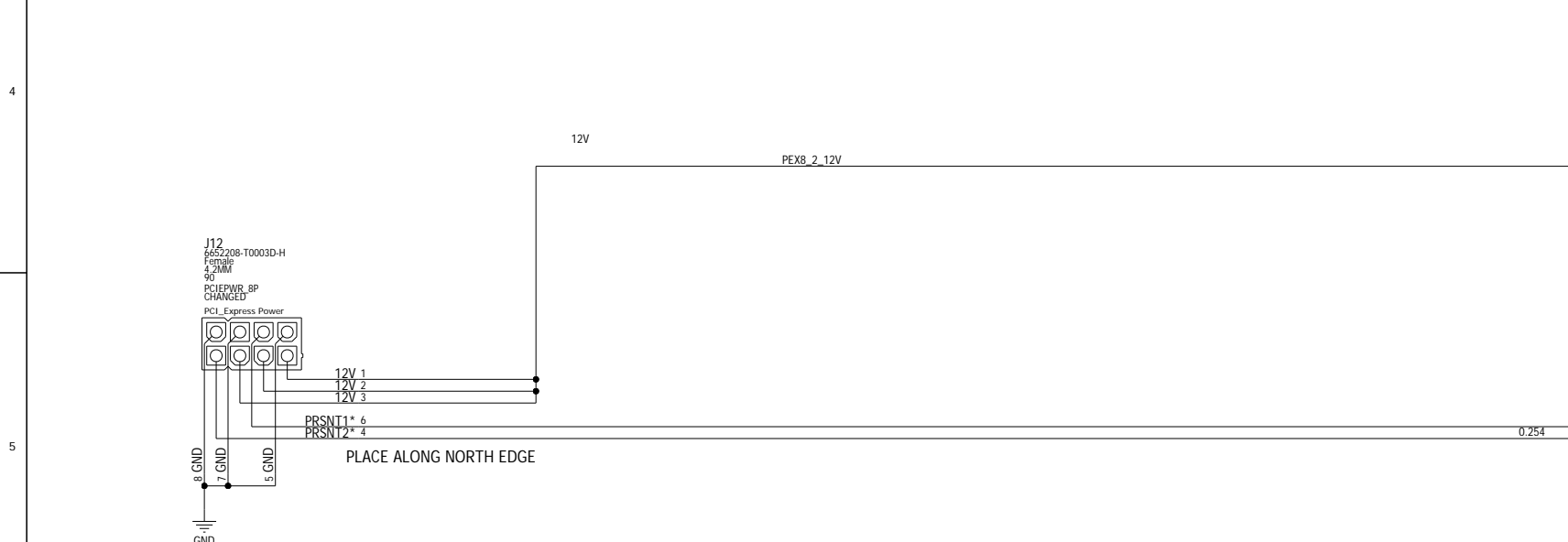
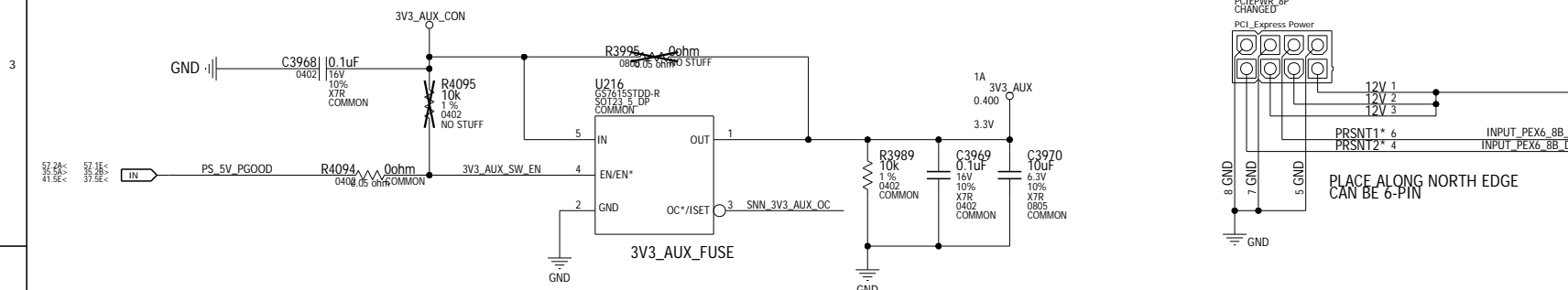
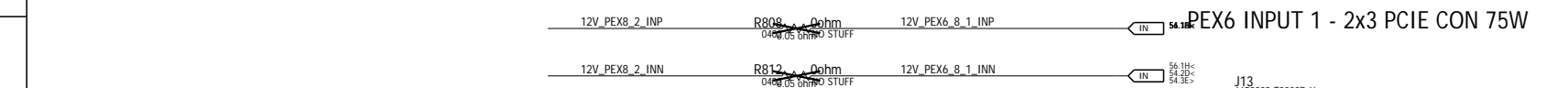
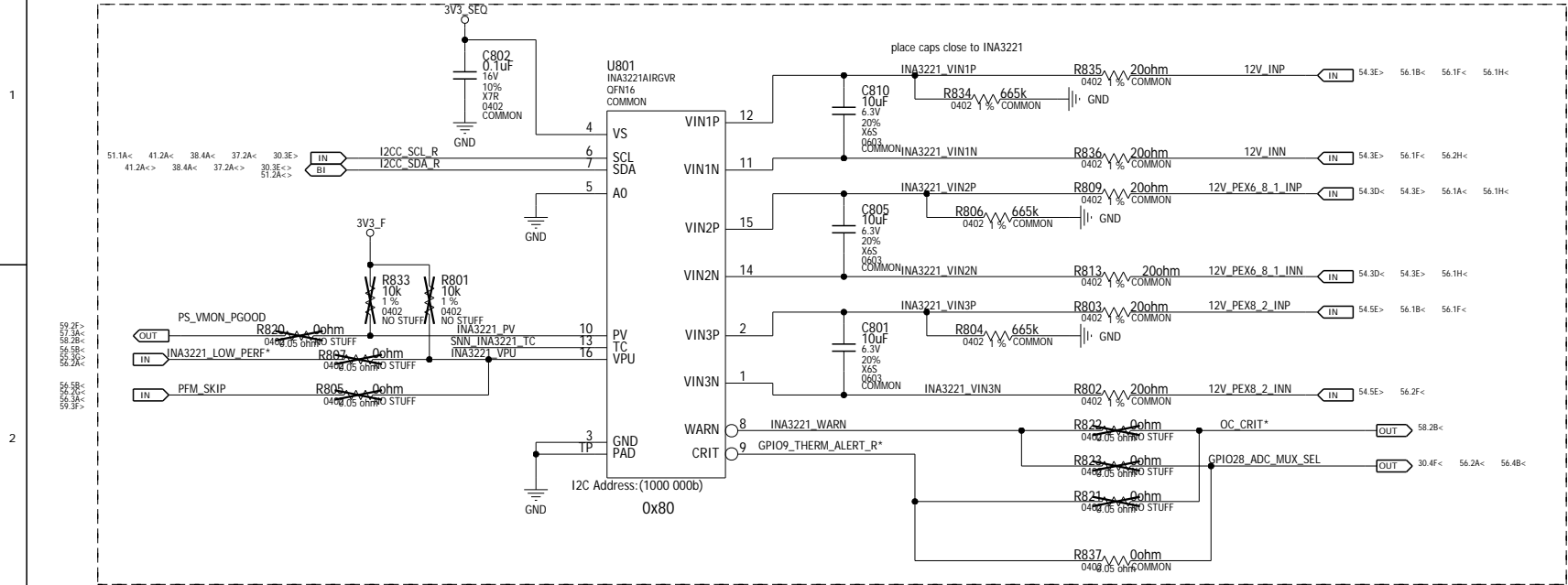


ASSEMBLY	SKU32
PAGE DETAIL	PS: DISCRETE STEERING

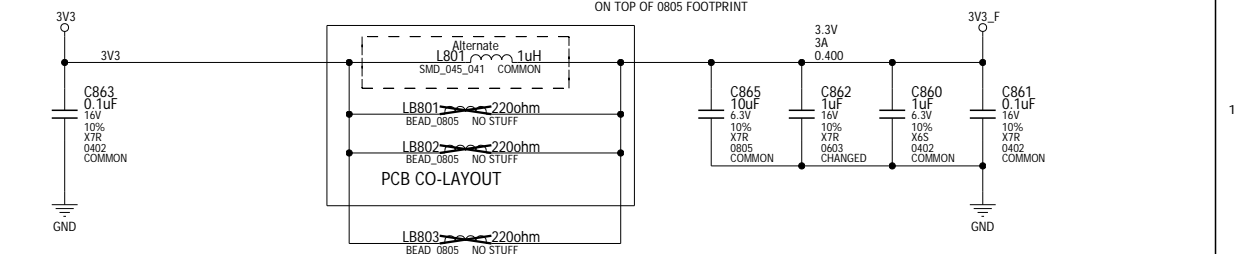
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BOM REV	A		

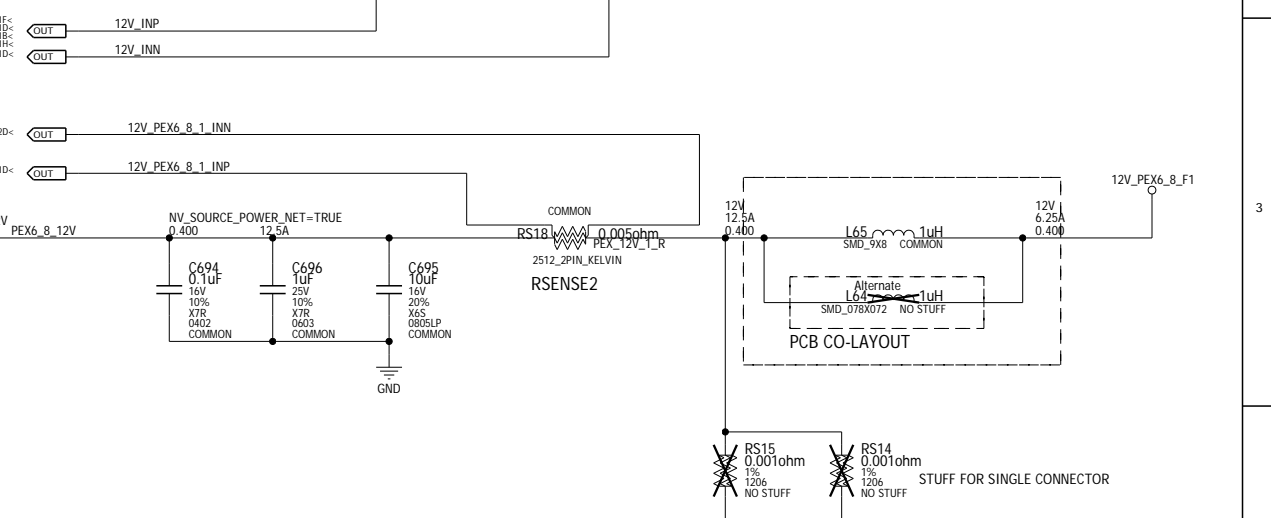
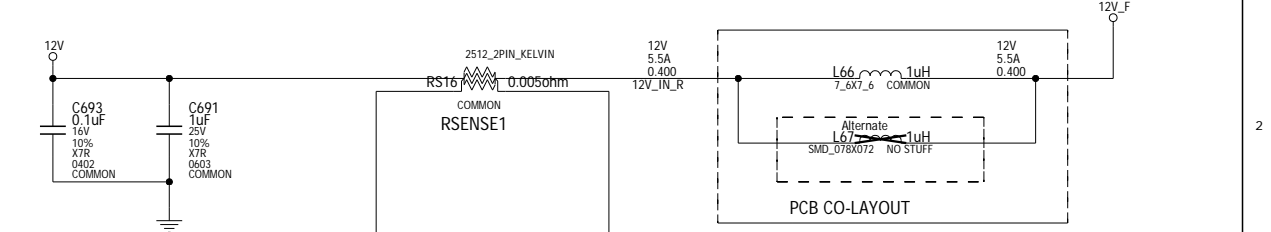
PS: Inputs, Filtering, and Monitoring



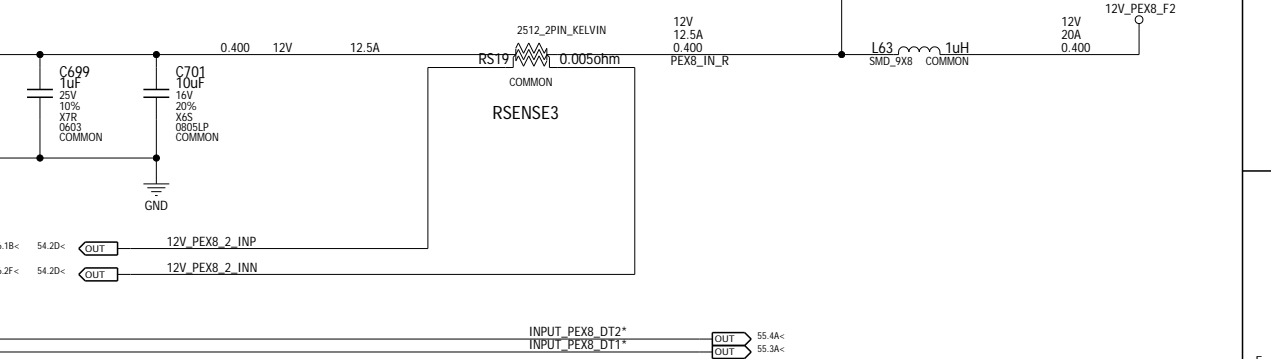
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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PS: 12V Current Steering & Hot Unplug Detect

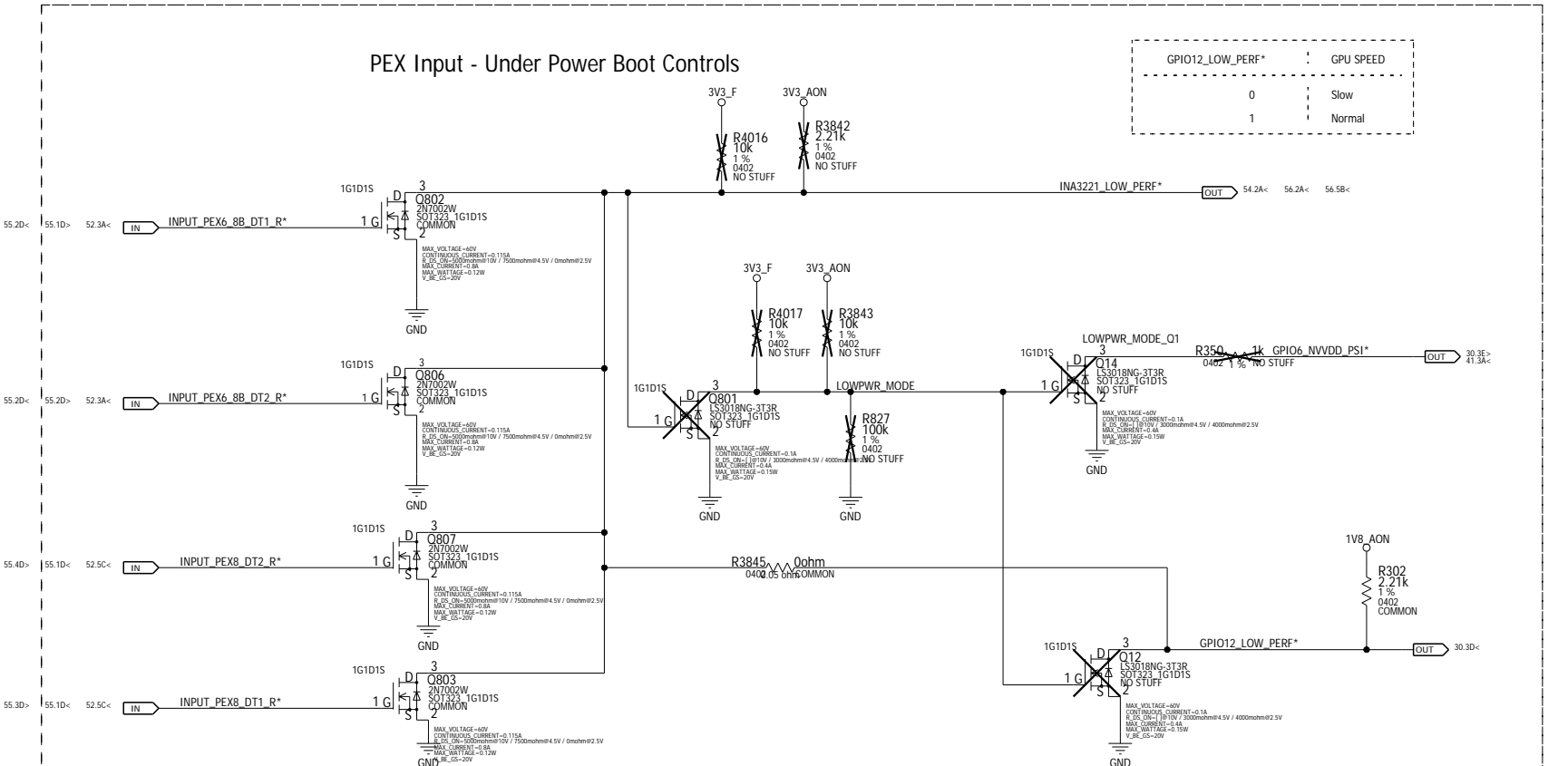
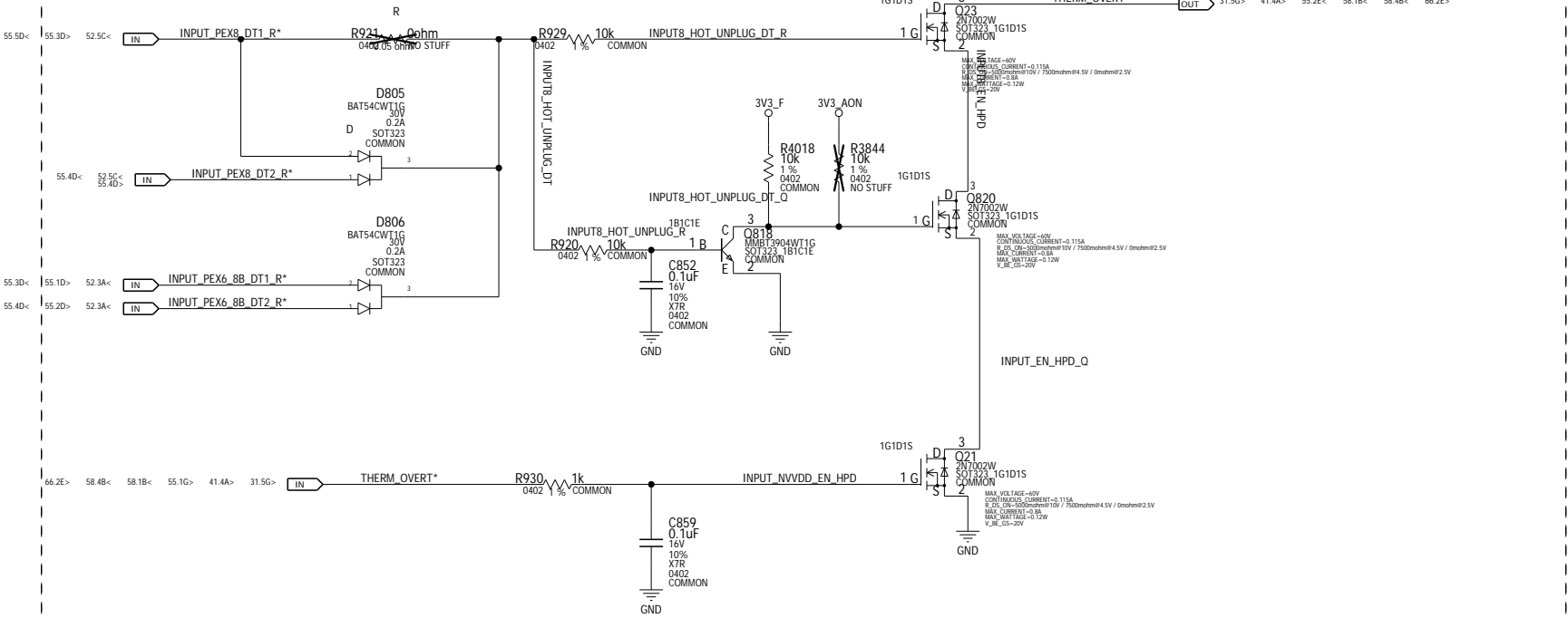
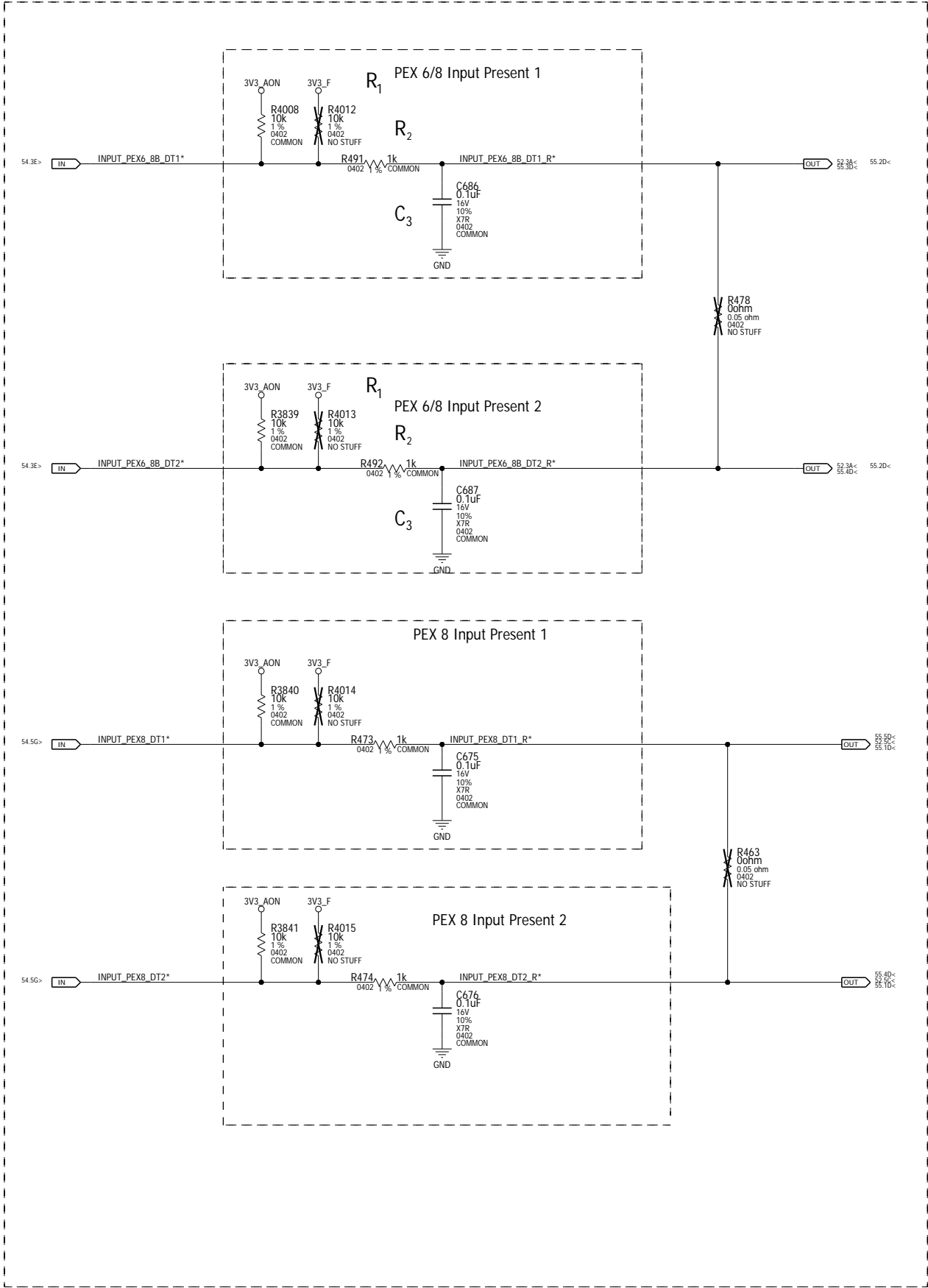
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A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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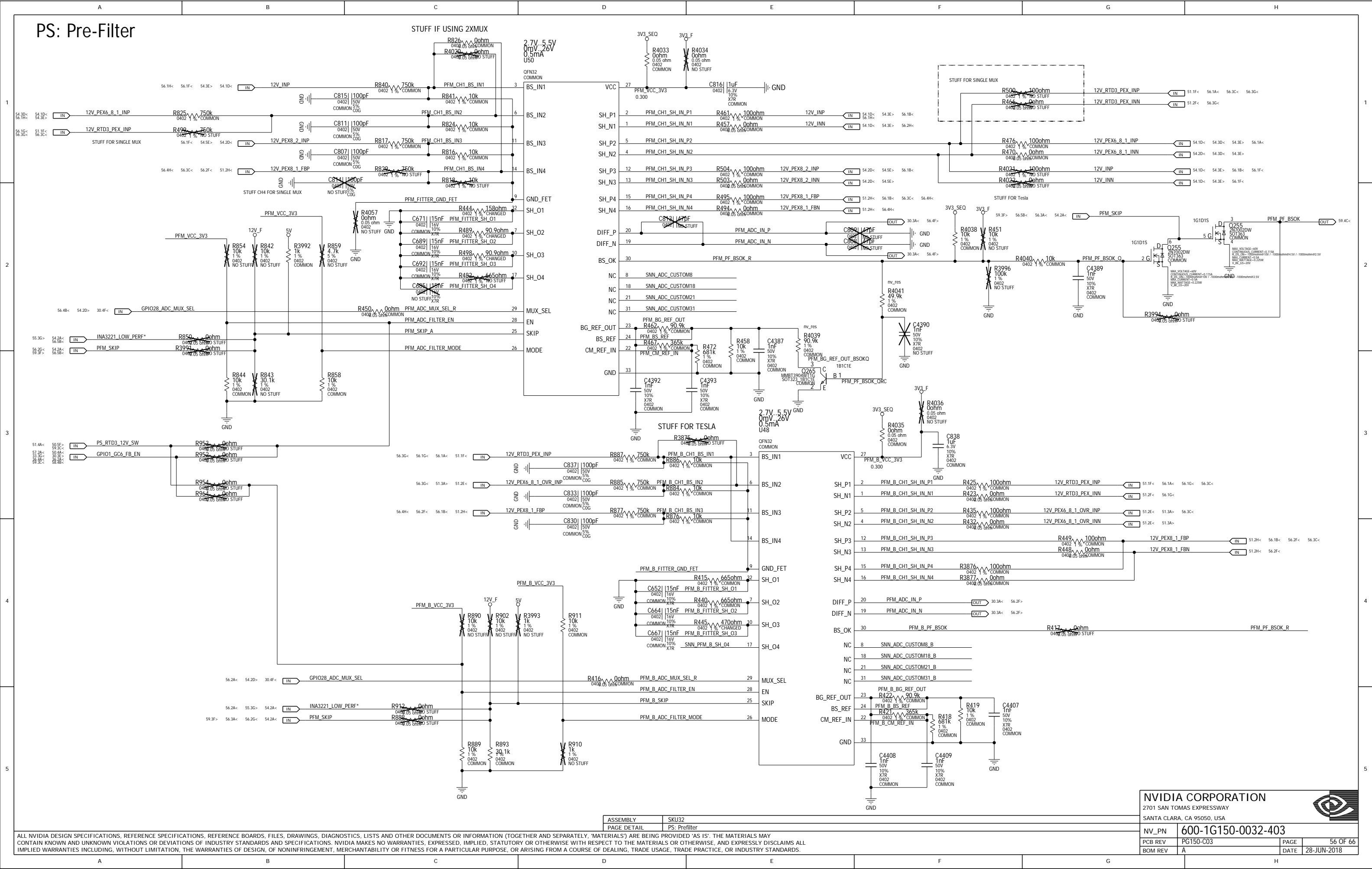
PCB REV PG150-C03

BOM REV A

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DATE 28-JUN-2018

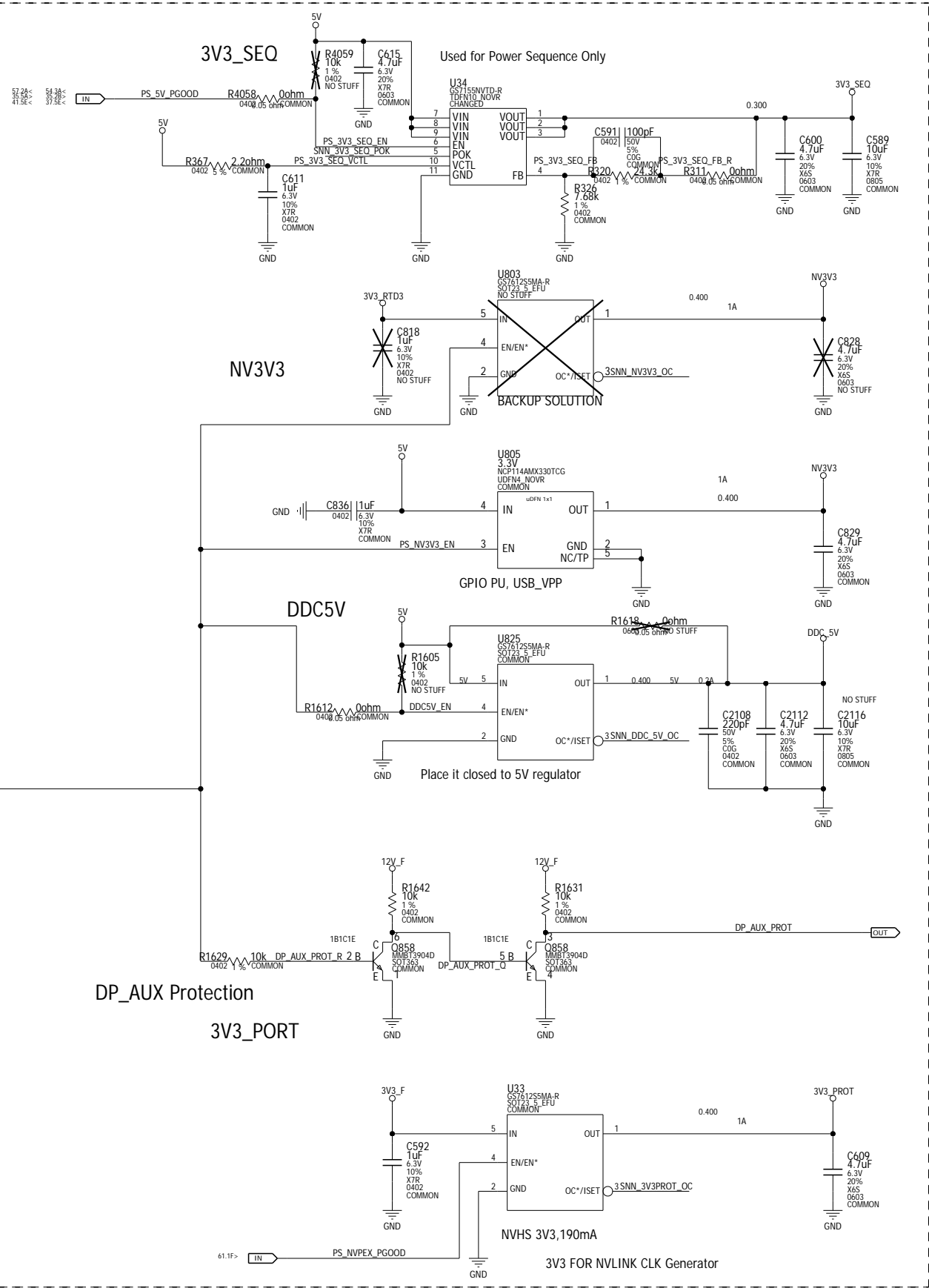
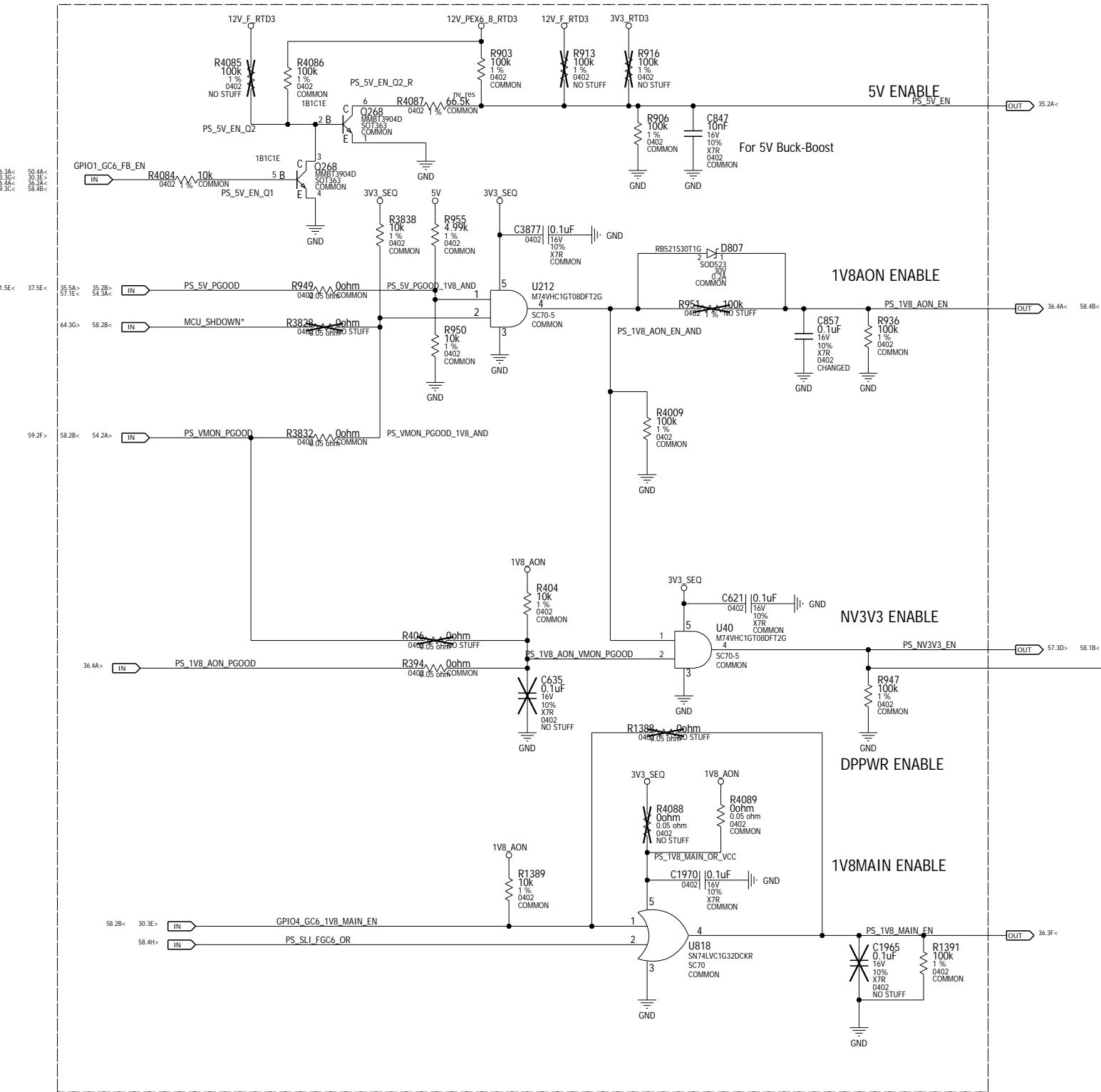
PS: Pre-Filter



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ASSEMBLY	SKU32
PAGE DETAIL	PS: Prefilter

SEQUENCE:5V,1V8,NV3V3 ENABLE



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PCB REV PG150-C03

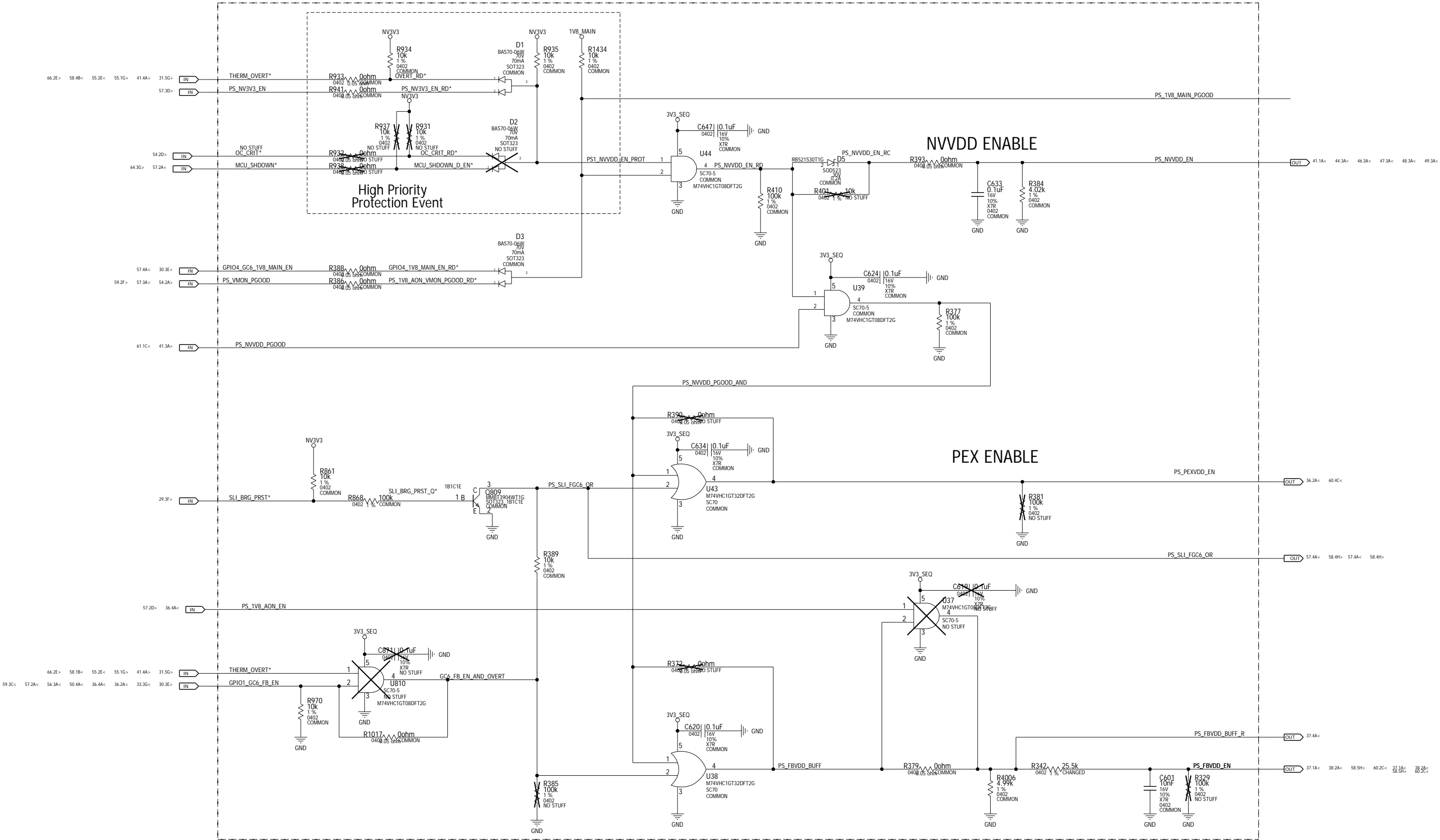
BOM REV A

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SEQUENCE:NV,PEX,FB ENABLE



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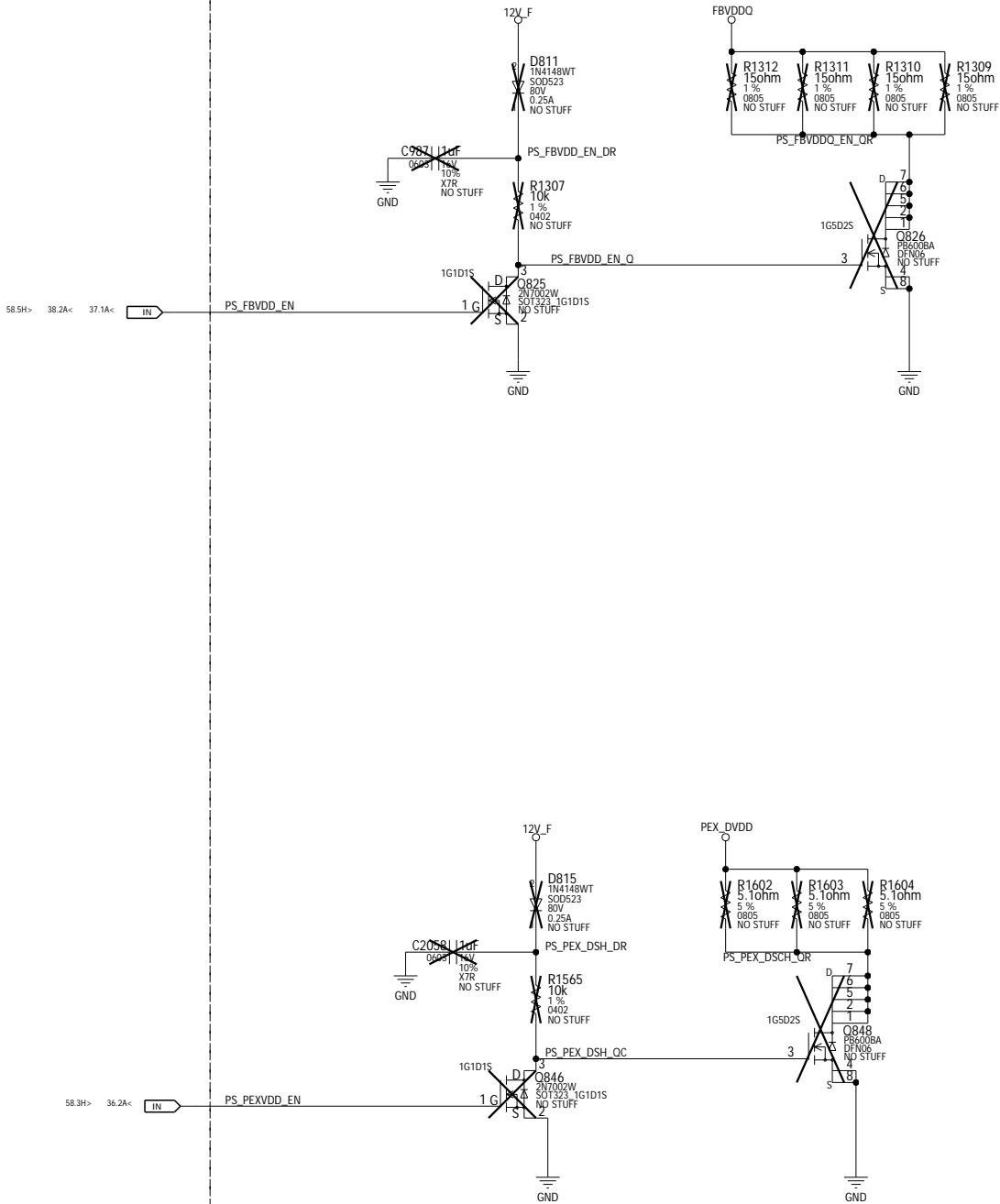
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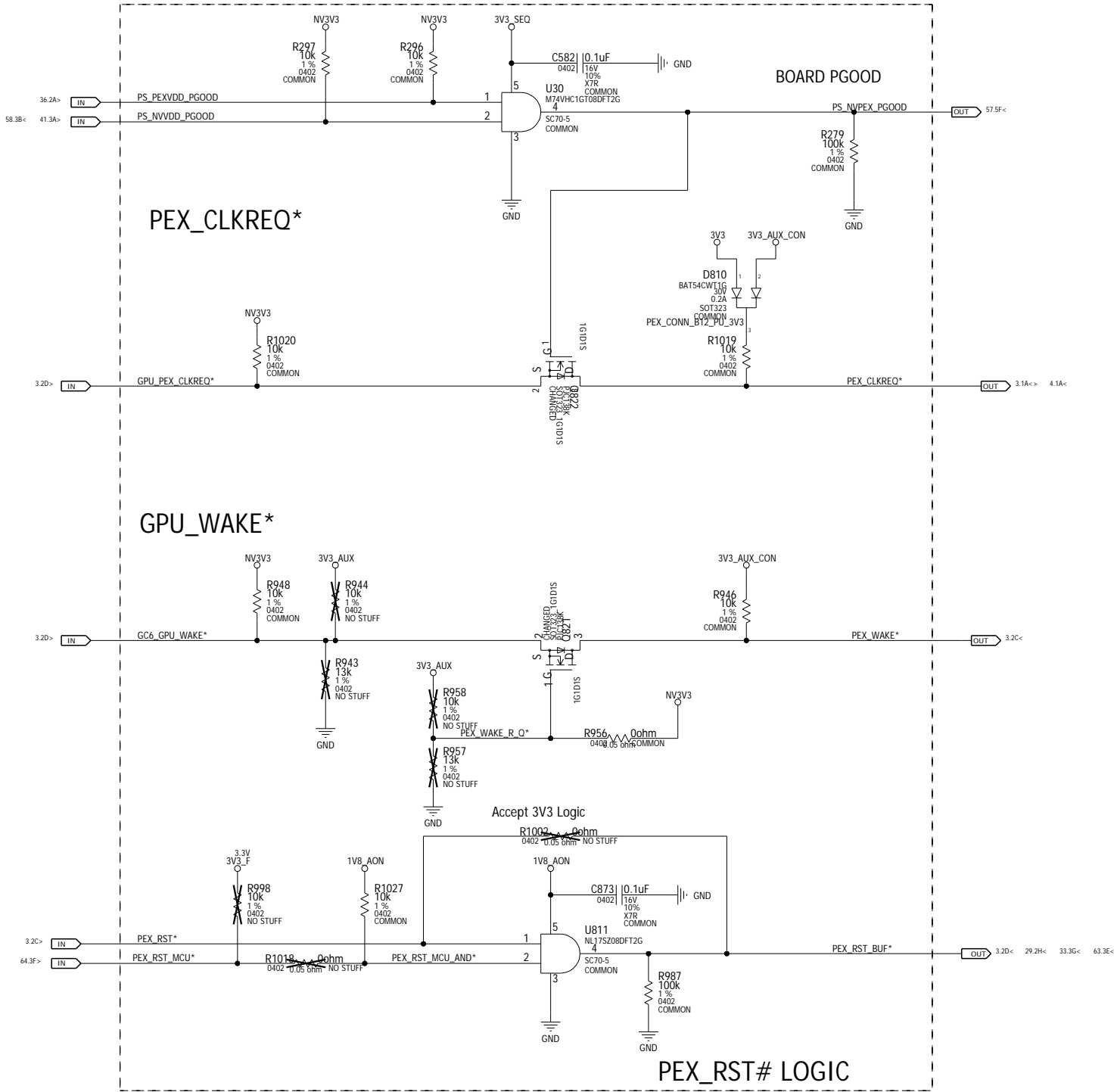
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SEQUENCE:Discharge



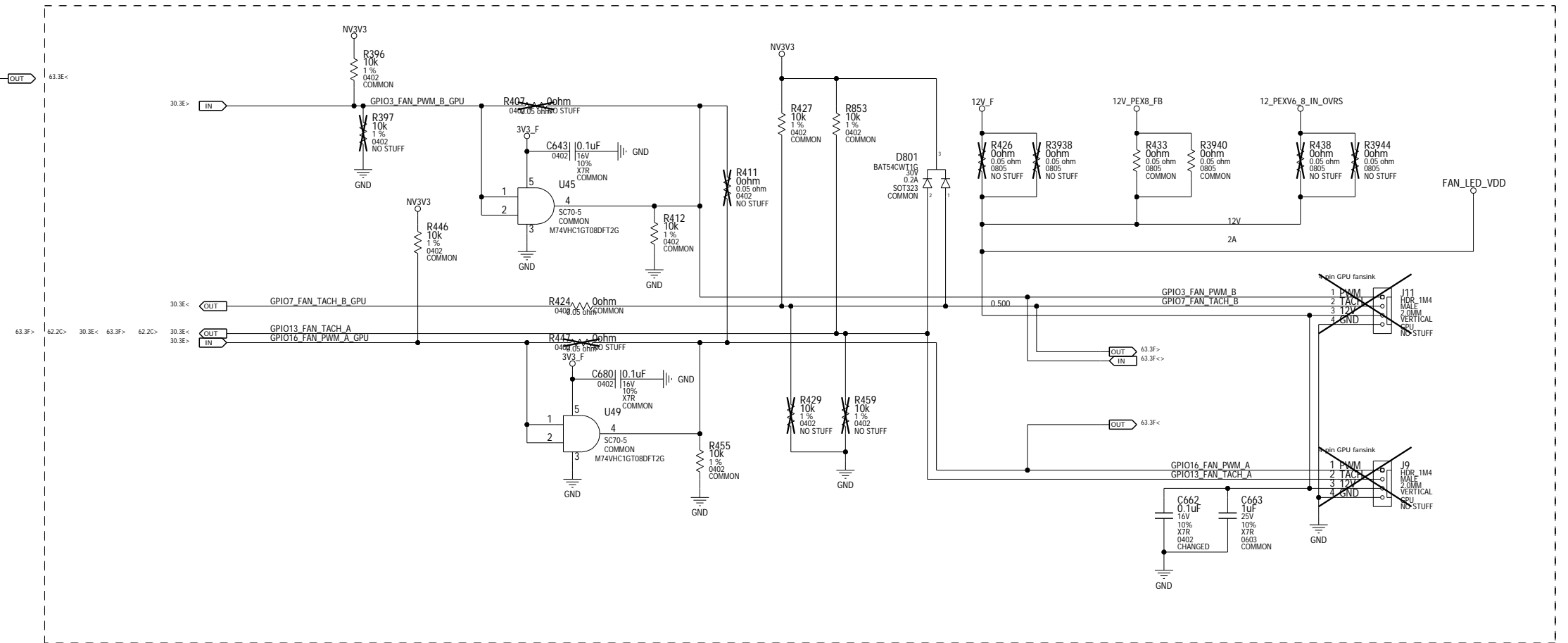
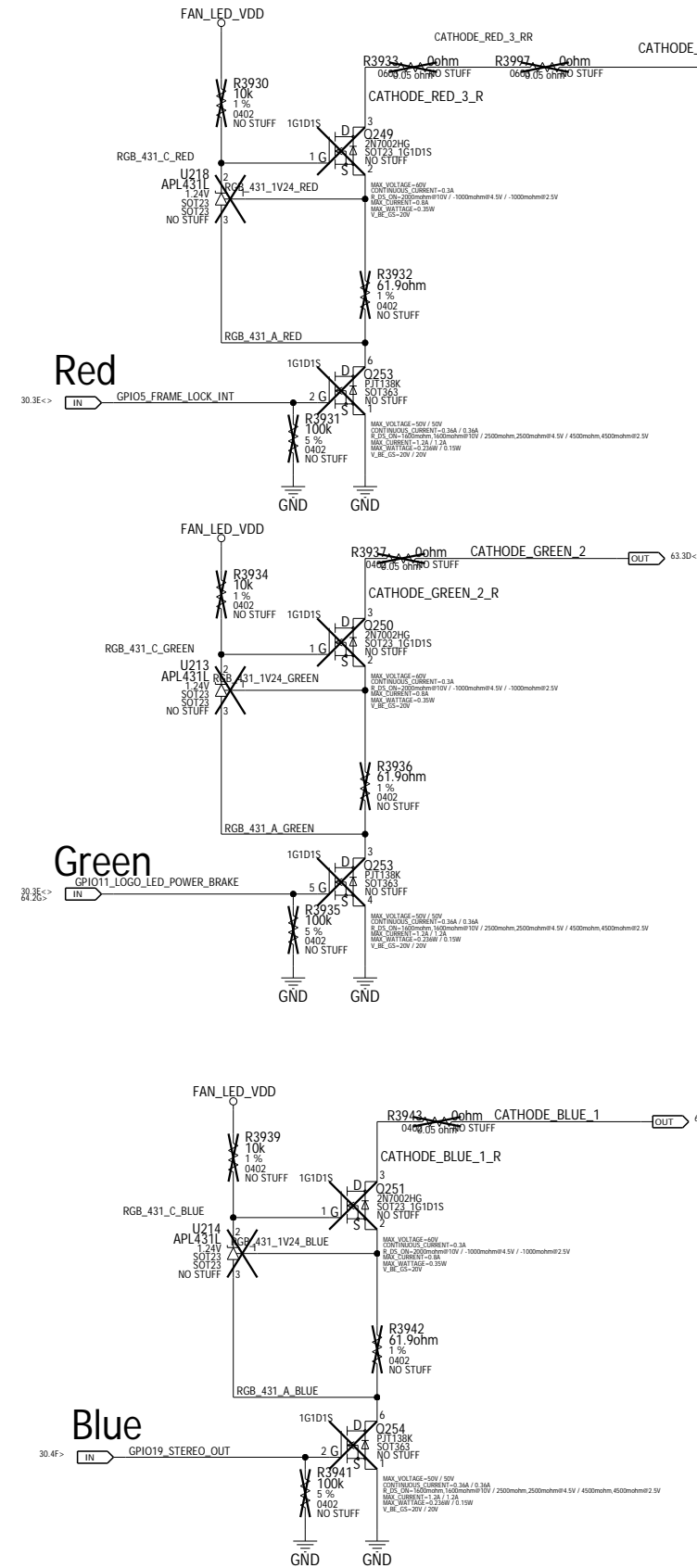
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SEQUENCE:MISC

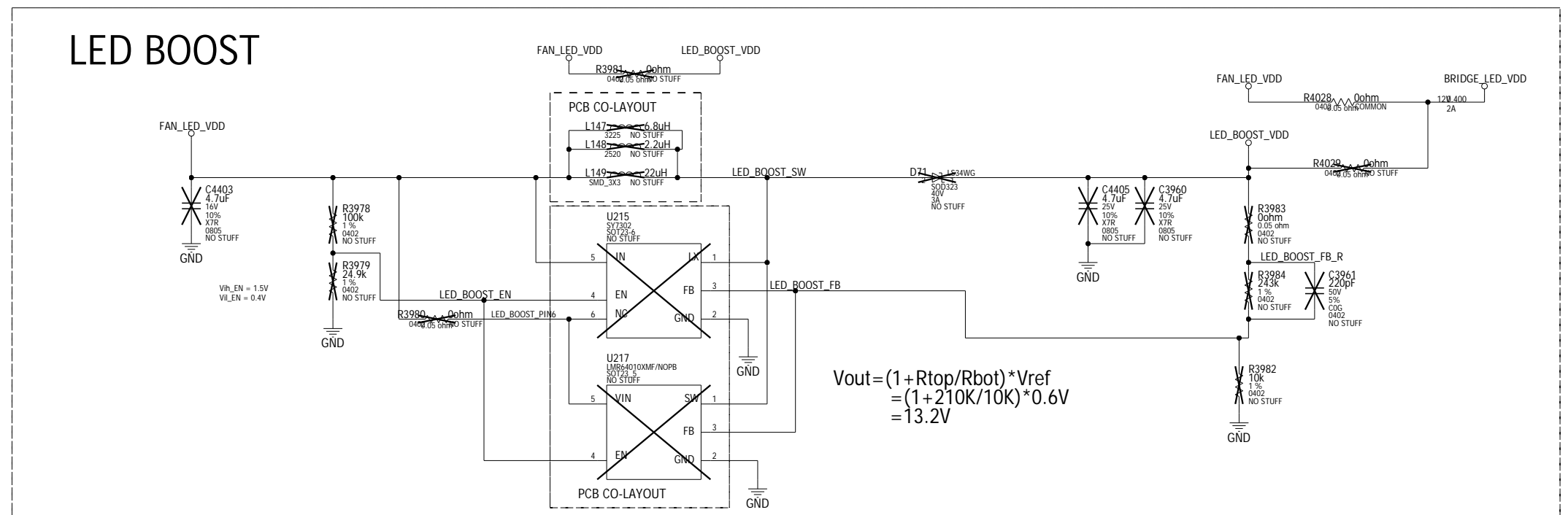


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MISC: FAN & LED1



LED BOOST



ASSEMBLY	SKU32
PAGE DETAIL	MISC: FAN & LED1

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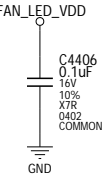
NV_PN	600-1G150-0032-403
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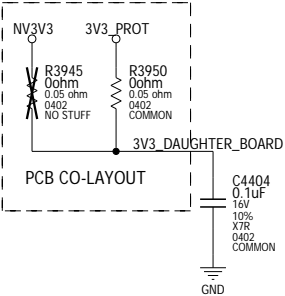


MISC: LED2

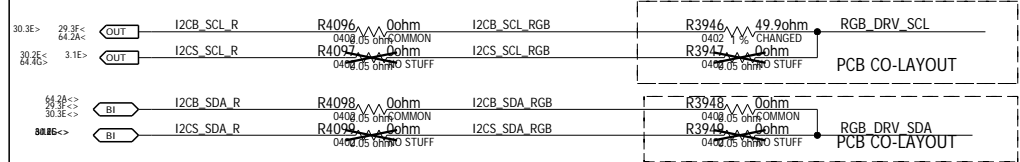
12V FROM FAN PAGE



PLACE CAPS CLOSE TO CONNECTOR

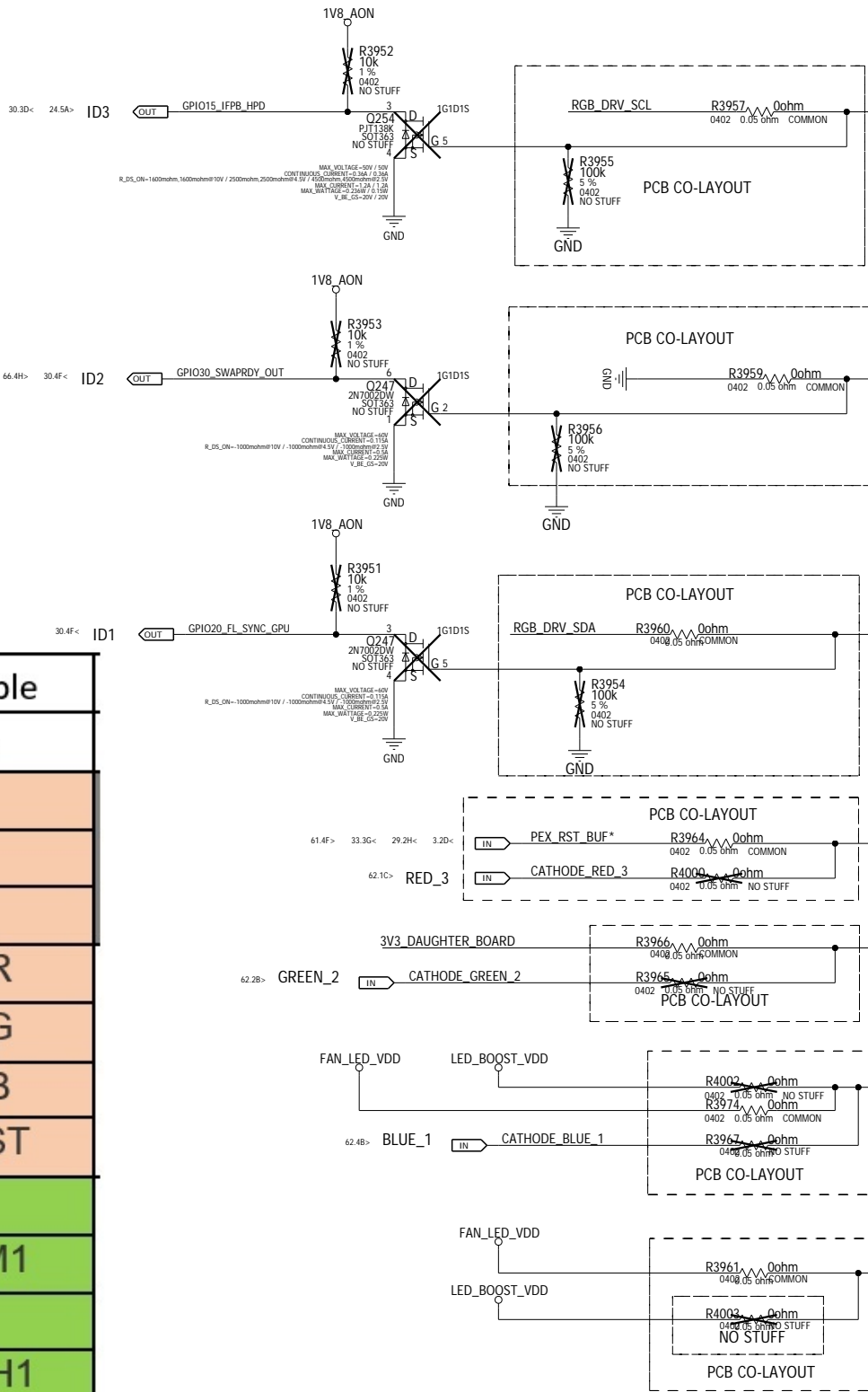


STUFF I2CB RESISTORS



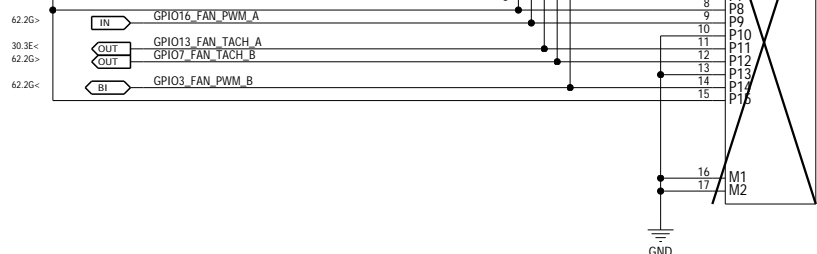
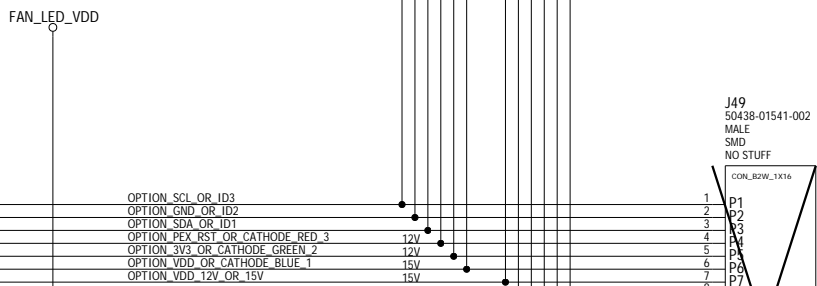
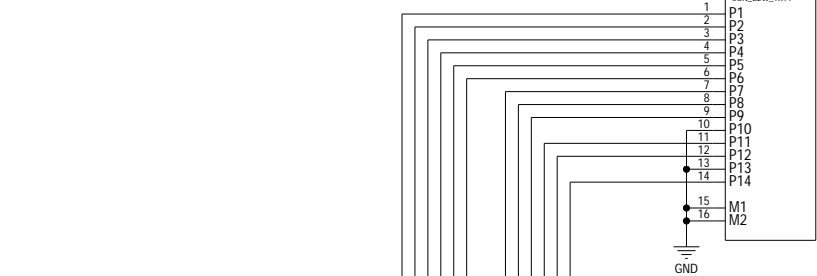
8-bit I2C Address of MCU on Daughter Board: 0x92

MCU Solution		For ONE ZONE RGB/cable	
PIN SEQ	Pin Name	PIN SEQ	Pin Name
1	I2C_SCL	1	ID3
2	GND	2	ID2
3	I2C_SDA	3	ID1
4	PEX_RST_BUF*	4	DRIVE3/R
5	NV3V3	5	DRIVE2/G
6	12V/BOOST	6	DRIVE1/B
7	12V	7	12V/BOOST
8	12V	8	12V
9	FAN_PWM1	9	FAN_PWM1
10	GND	10	GND
11	FAN_TACH1	11	FAN_TACH1
12	FAN_TACH2	12	FAN_TACH2
13	GND	13	GND
14	FAN_PWM2	14	FAN_PWM2
		15	12V



14-PIN STRAIGHT PRIMARY SOURCE -> 080-1586-000: ACES \$0.115
14-PIN STRAIGHT SECOND SOURCE -> 080-1600-000: WIESON \$0.2

FOR MCU SOLUTION



FOR ONE ZONE RGB SOLUTION

15-PIN STRAIGHT PRIMARY SOURCE -> 080-1617-000: ACES \$0.1165
15-PIN STRAIGHT SECOND SOURCE -> 080-1628-000: WIESON \$0.23

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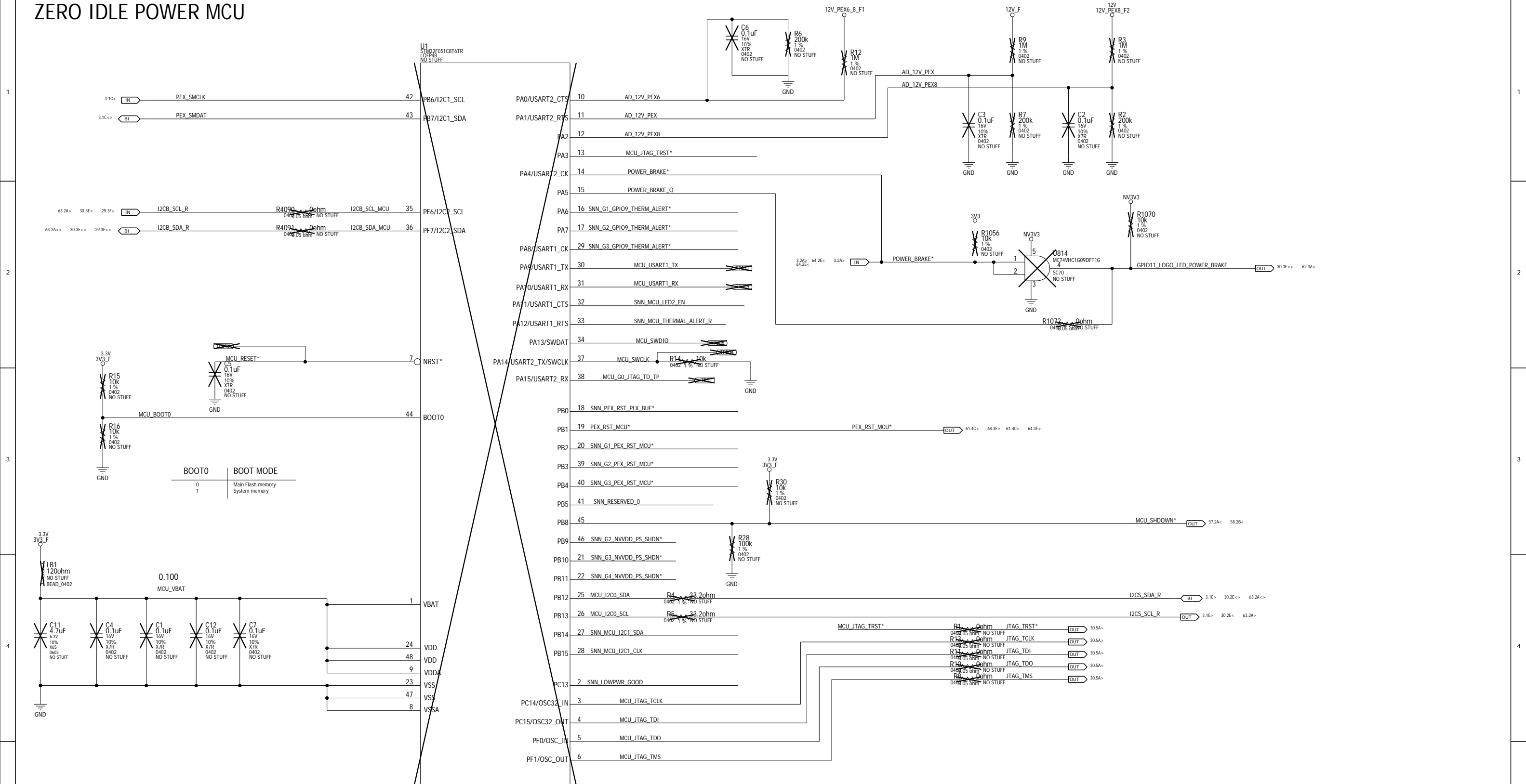


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ZERO IDLE POWER MCU



ASSEMBLY	SKU32
PAGE DETAIL	MCU ZERO POWER IDLE

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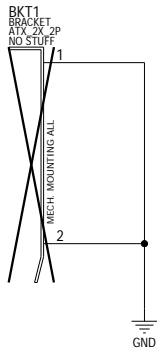
NV_PN	600-1G150-0032-403
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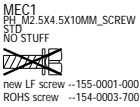


Mechanical: Bracket/Thermal Solution

Brackets:



Bracket Screw



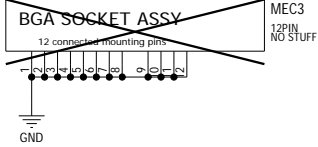
Back Cover



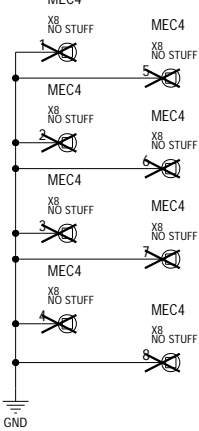
GPU Stiffner back side



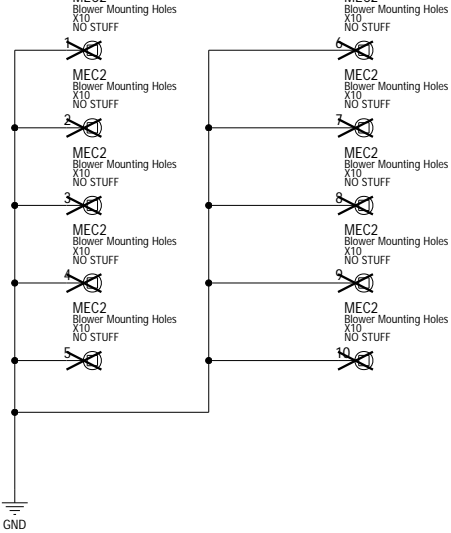
GPU Socket Symbol



GPU Mounting holes

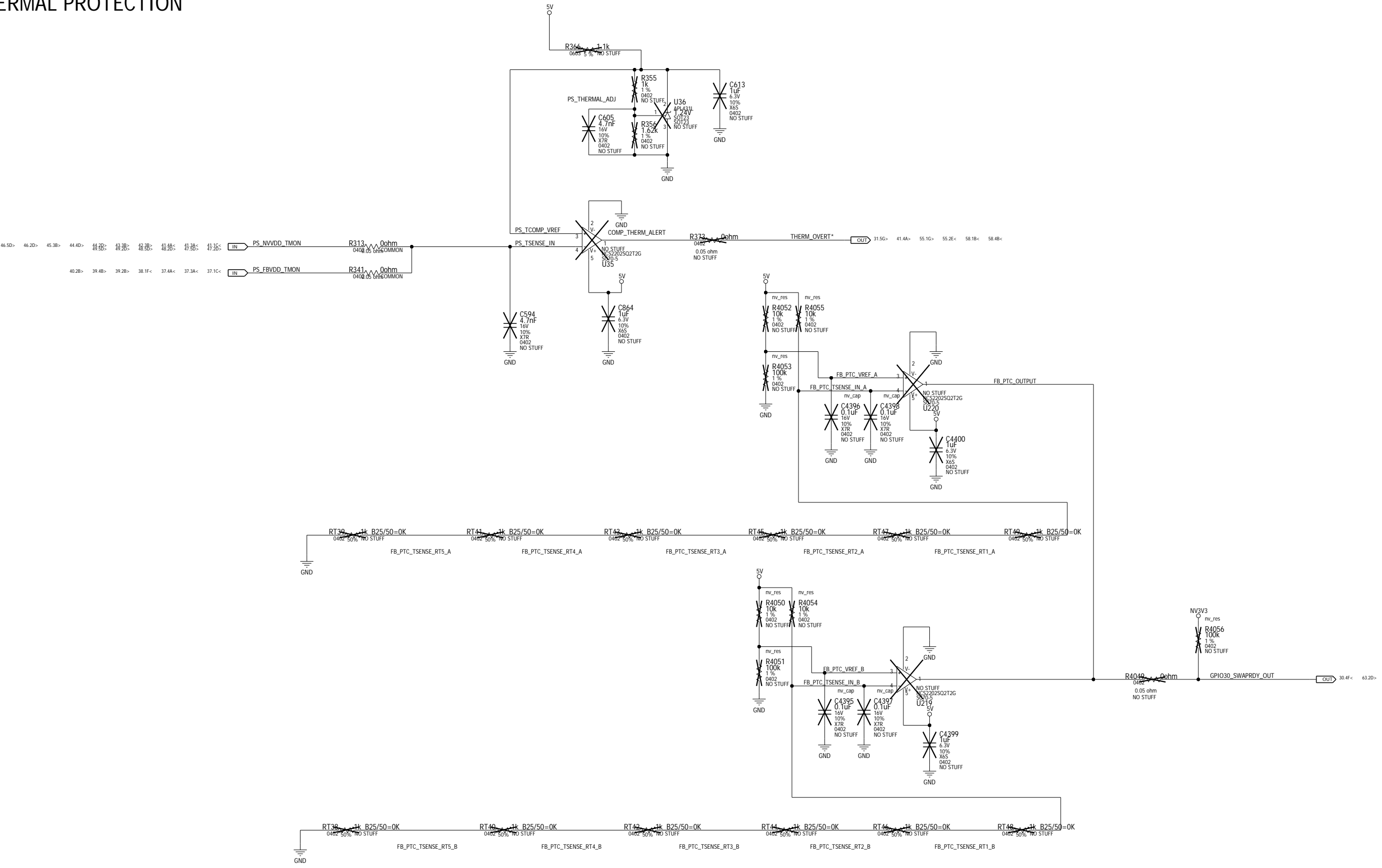


Mechanical Holes Symbol



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