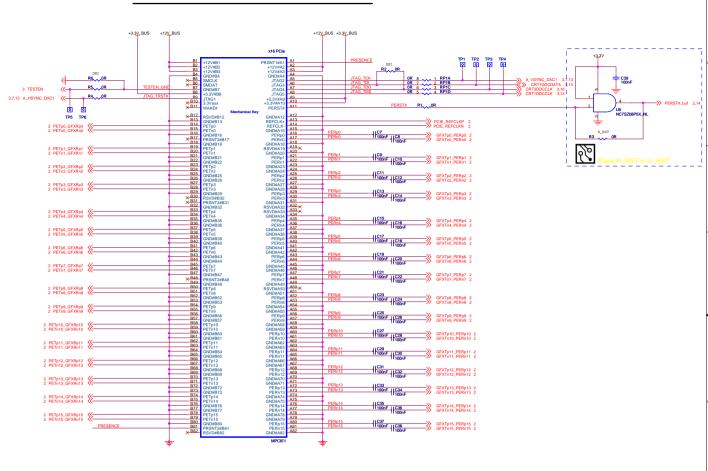
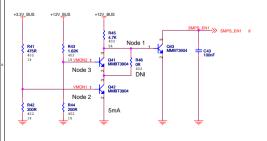


PCI-EXPRESS EDGE CONNECTOR





Power Sequence Circuit to ensure SMPS_EN is released after +12V_BUS and +3.3V_BUS are both in regulation. Pull-up may or may not be required on SMPS EN signal depending on SMPS design.

Node 1 When +12V ramps above min Vbe, SMPS_EN will be helt low

Node 2 When +3.3V gets close to regulation, one of the two

conditions of releasing SMPS_EN is active Target ~ 900mV when +3.3 at min regulation (worse case)

Typical trigger when +3.3V ramps above 2.2V (650mV)

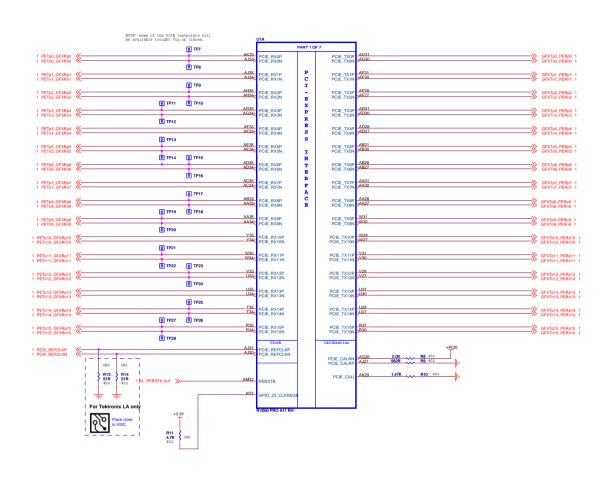
Node 3 When +12V gets close to regulation, one of the two conditions of releasing SMPS_EN is active

Target ~ 1.25V when +12 at min regulation (worse case)

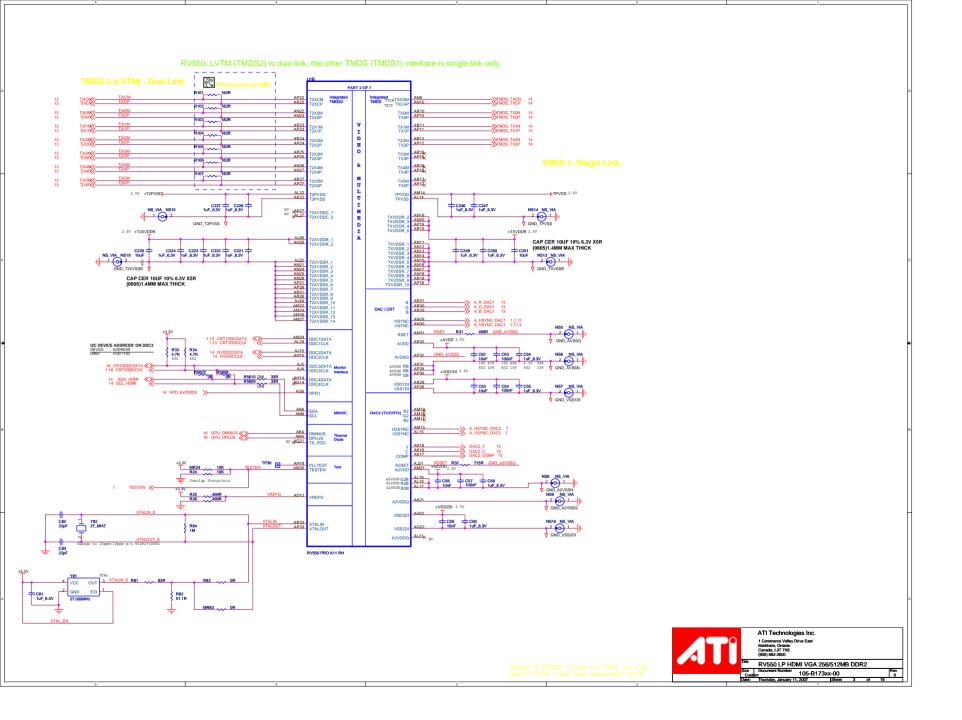
Typical trigger when +12V ramps above 10V (1.1V)

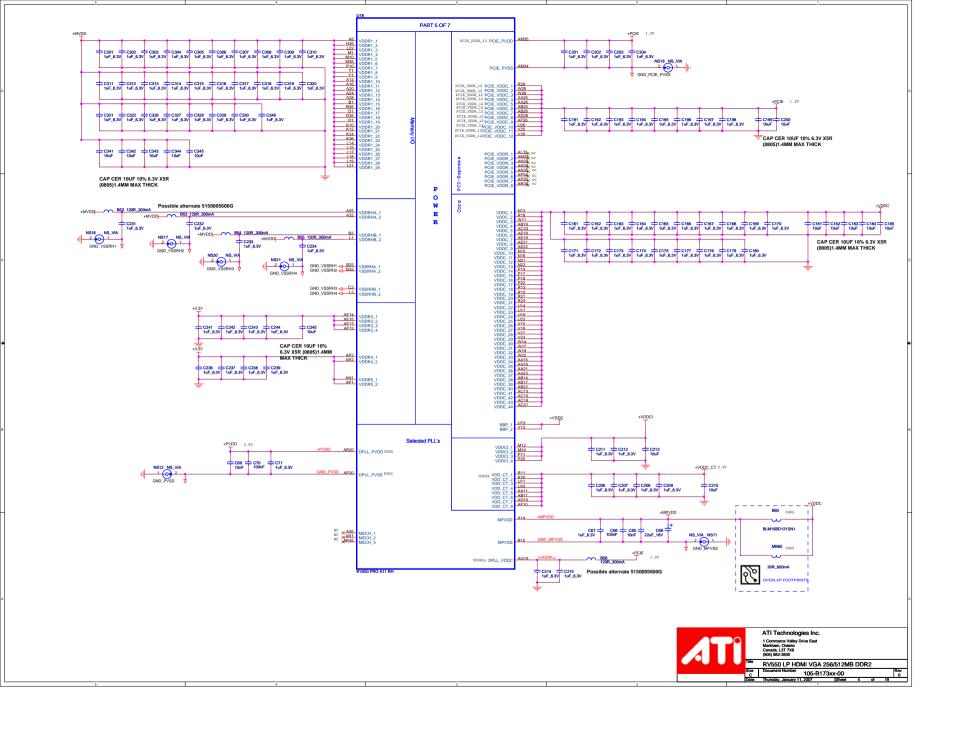


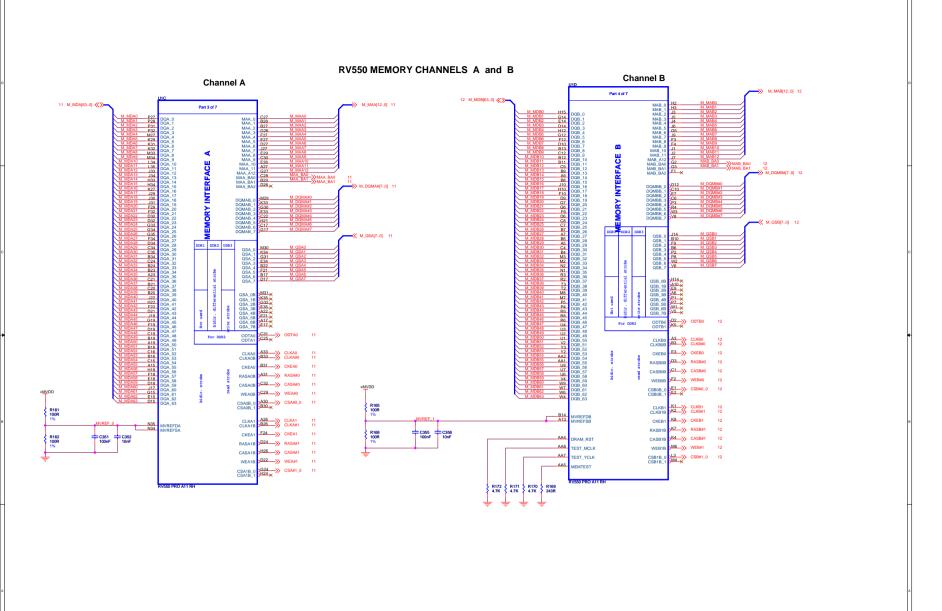




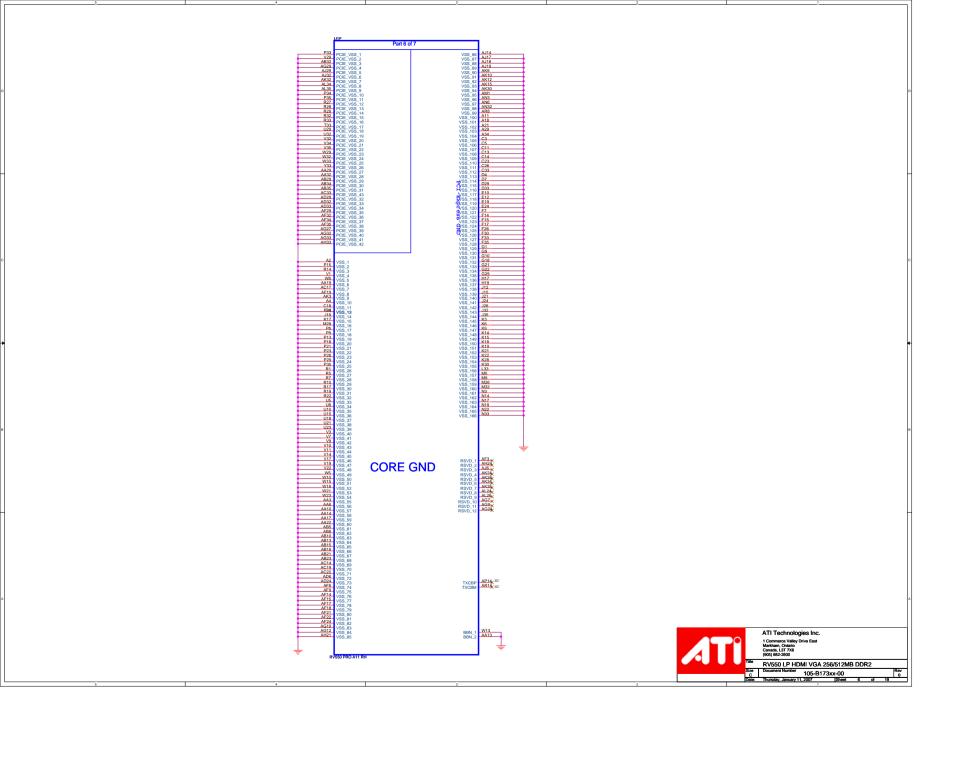


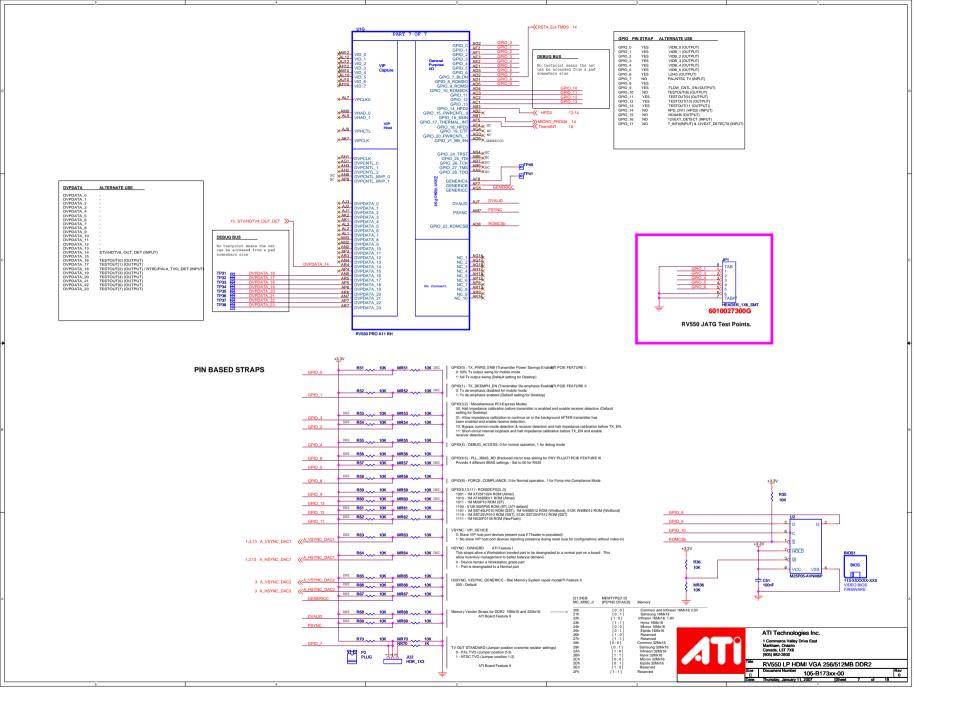


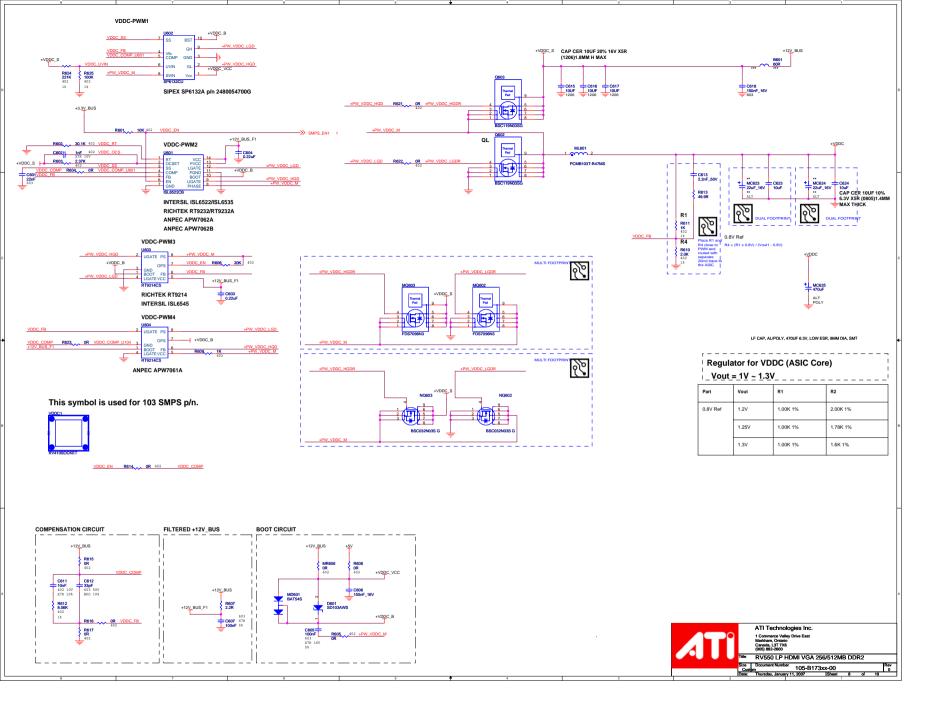


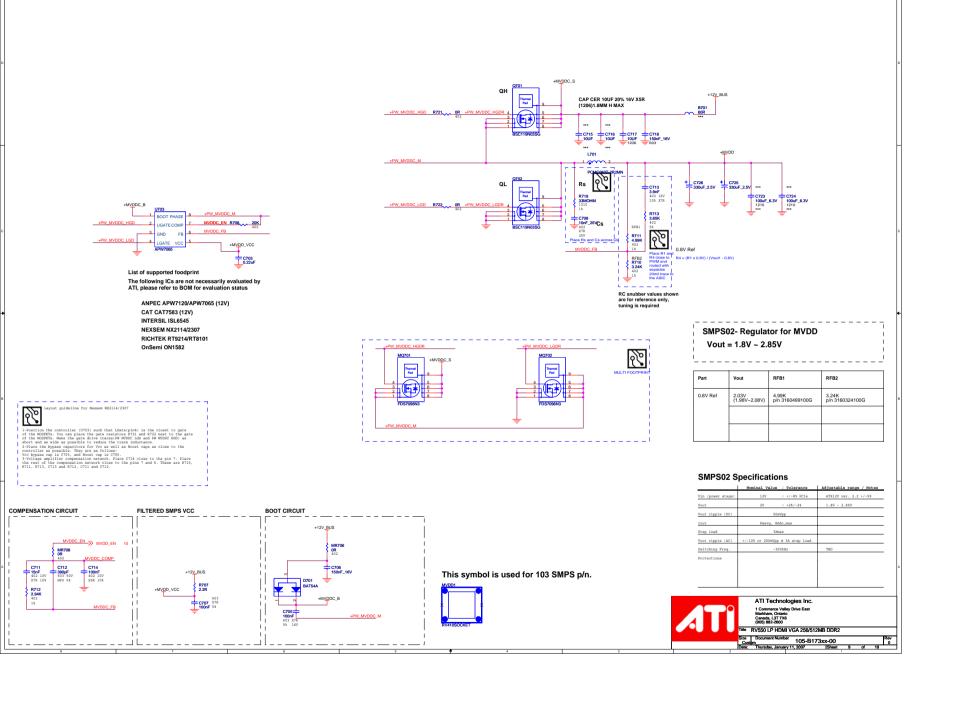


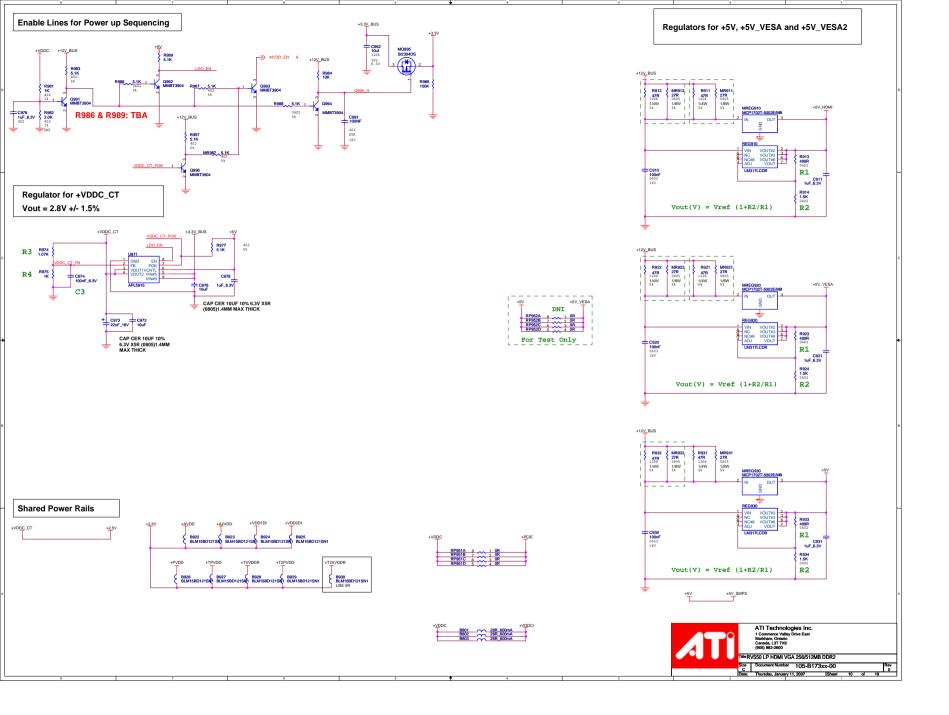


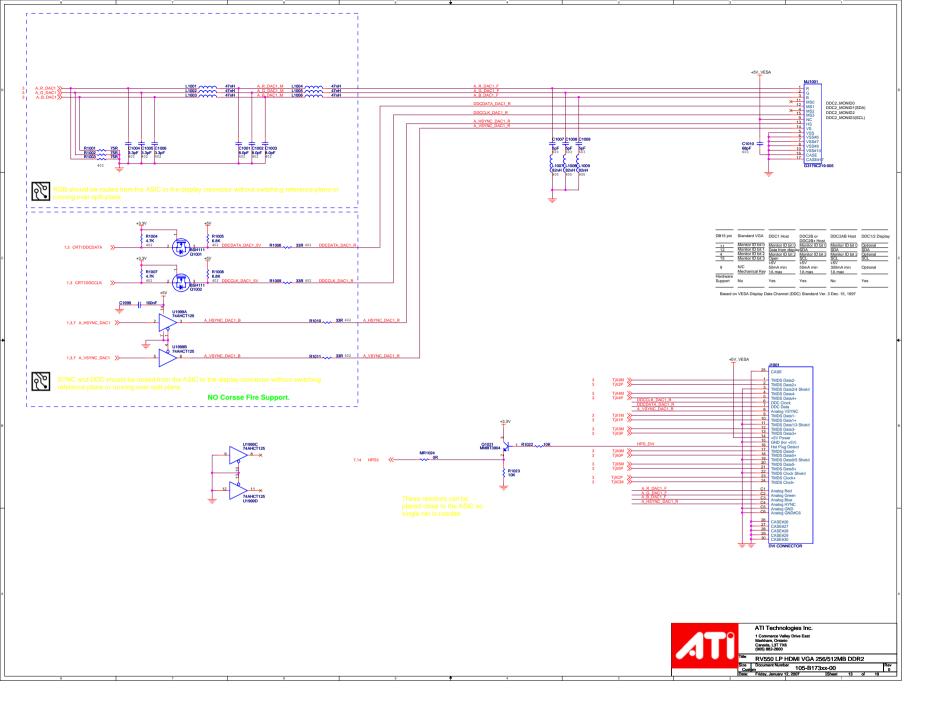


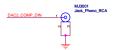


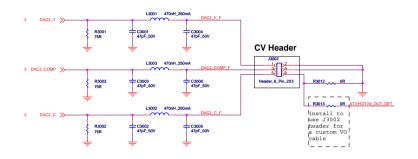


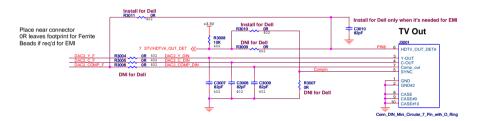








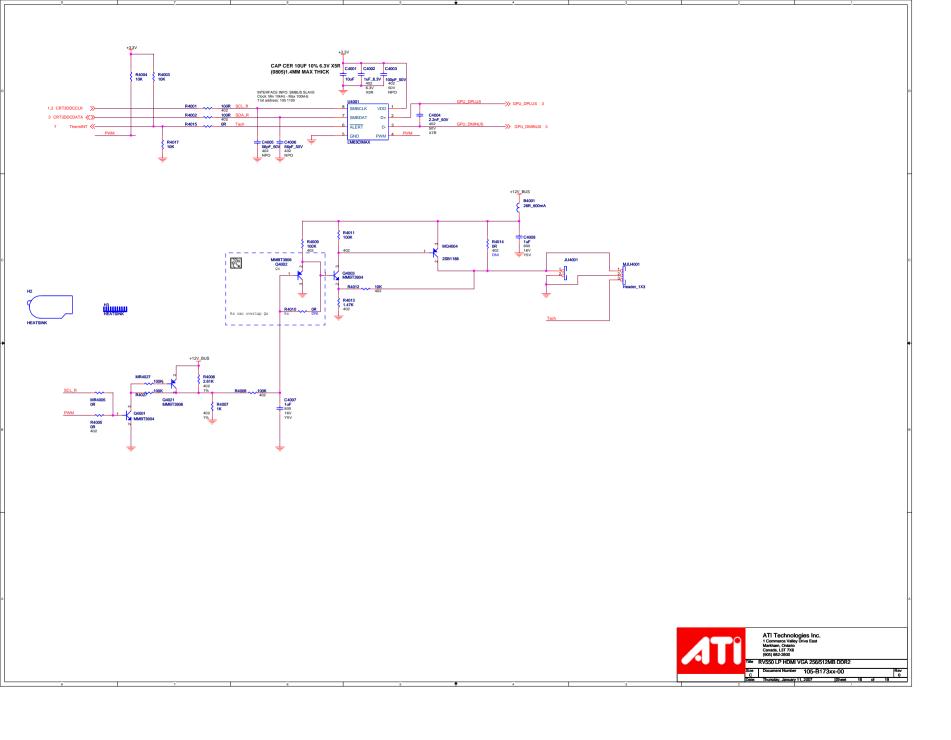


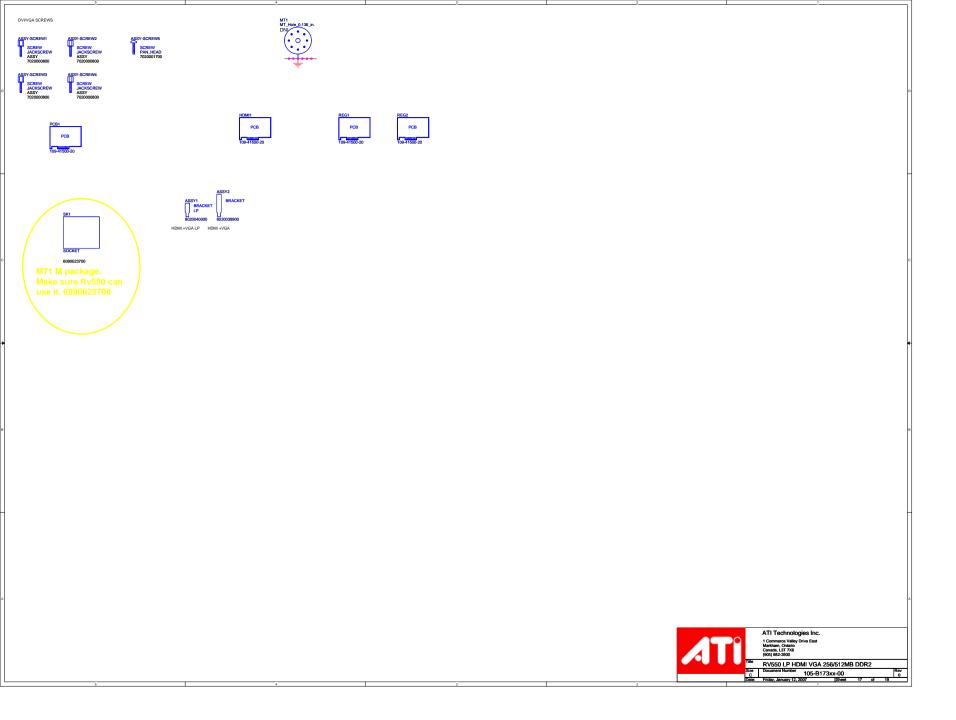


The 7-pin MiniDIN footprint allows one of the two MiniDINs:

- 7-pin Svideo/Composite MiniDIN P/N 6071001500G
- 4-pin Svideo MiniDIN P/N 6070001000G







	Name>	5	4 3	2	1		
			Title	Schematic No.	Date:		
			RV550 LP HDMI VGA 256/512MB DDR2	105-B173xx-00	Friday, January 12.	Friday, January 12, 2007	
		JU	REVISION HISTORY NOTE: This sche For Stuffin	matic represents the PCB, it does not represent any ng options (component values, DNI ,? please consuntat ATI representative to obtain latest BOM closes	specific SKU.	Rev 0	
Sch	РСВ	Date			it to the application desired.		
Rev	Rev						
01	A00	05-12-06	Initial release				
	-00	01-11-07	07 U1999 Floating pins 9,10,12,13 connected to GND ; R3012,R3013 added so J3002.6 can be connected to HDTV detect signal for future dongle/cable use				
		5	4 3	2	1	l .	

