

GA102 DT SKU P-BOARD

350W, FH Std PCB, 384b, GDDR6X x8

DP + DP + DP + HDMI/DP

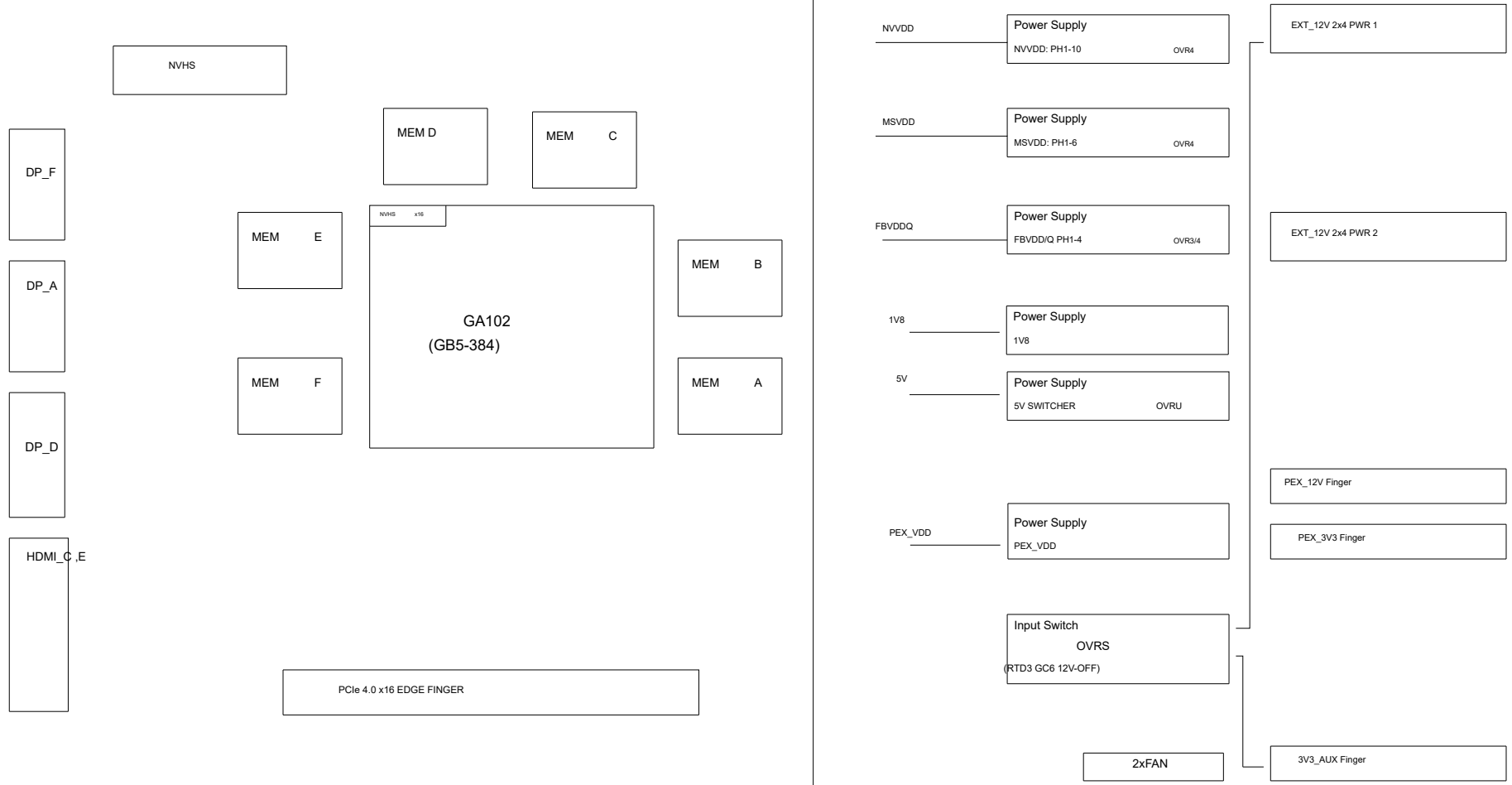
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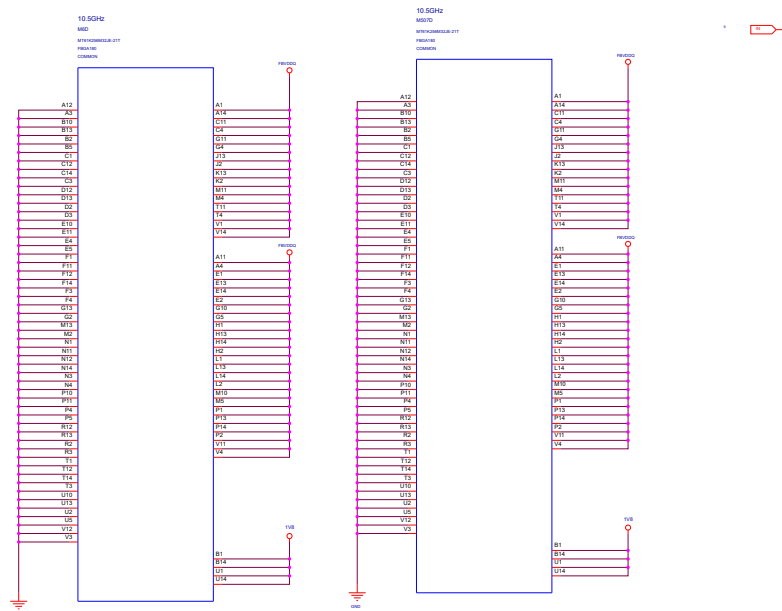
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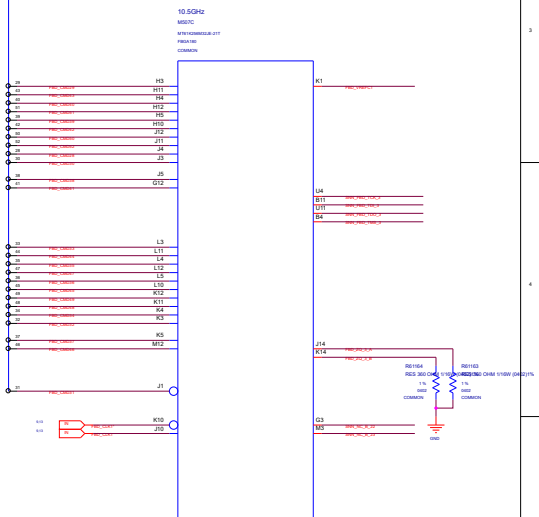
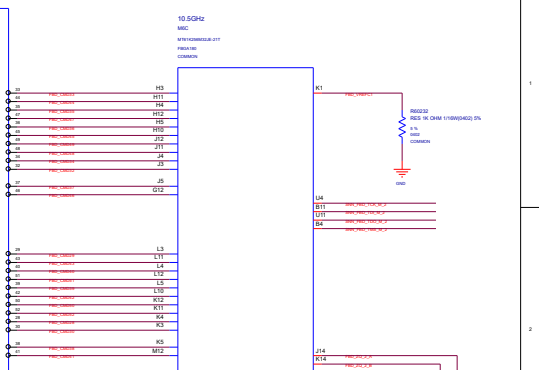
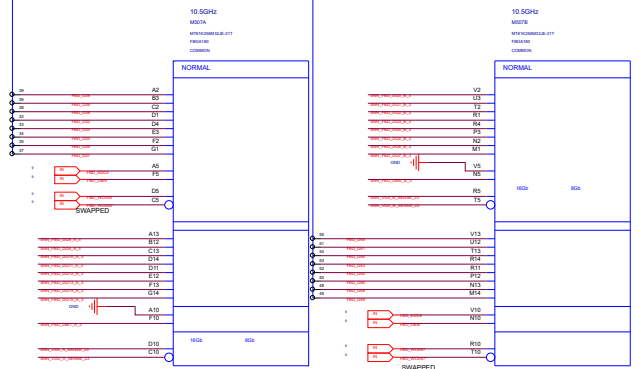
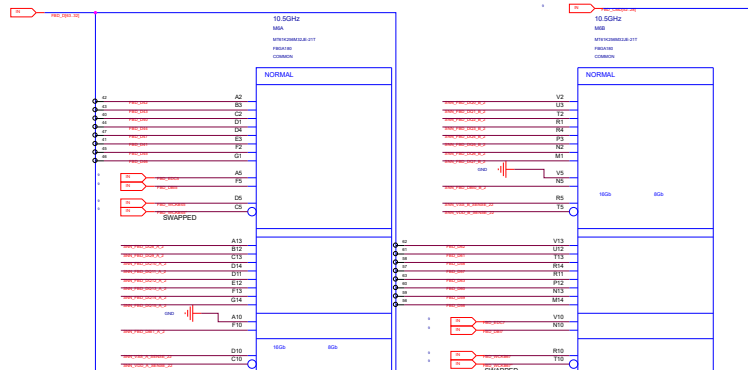
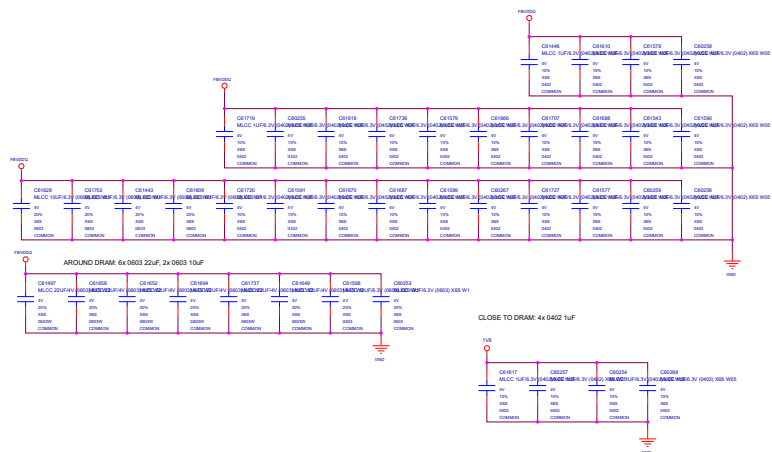
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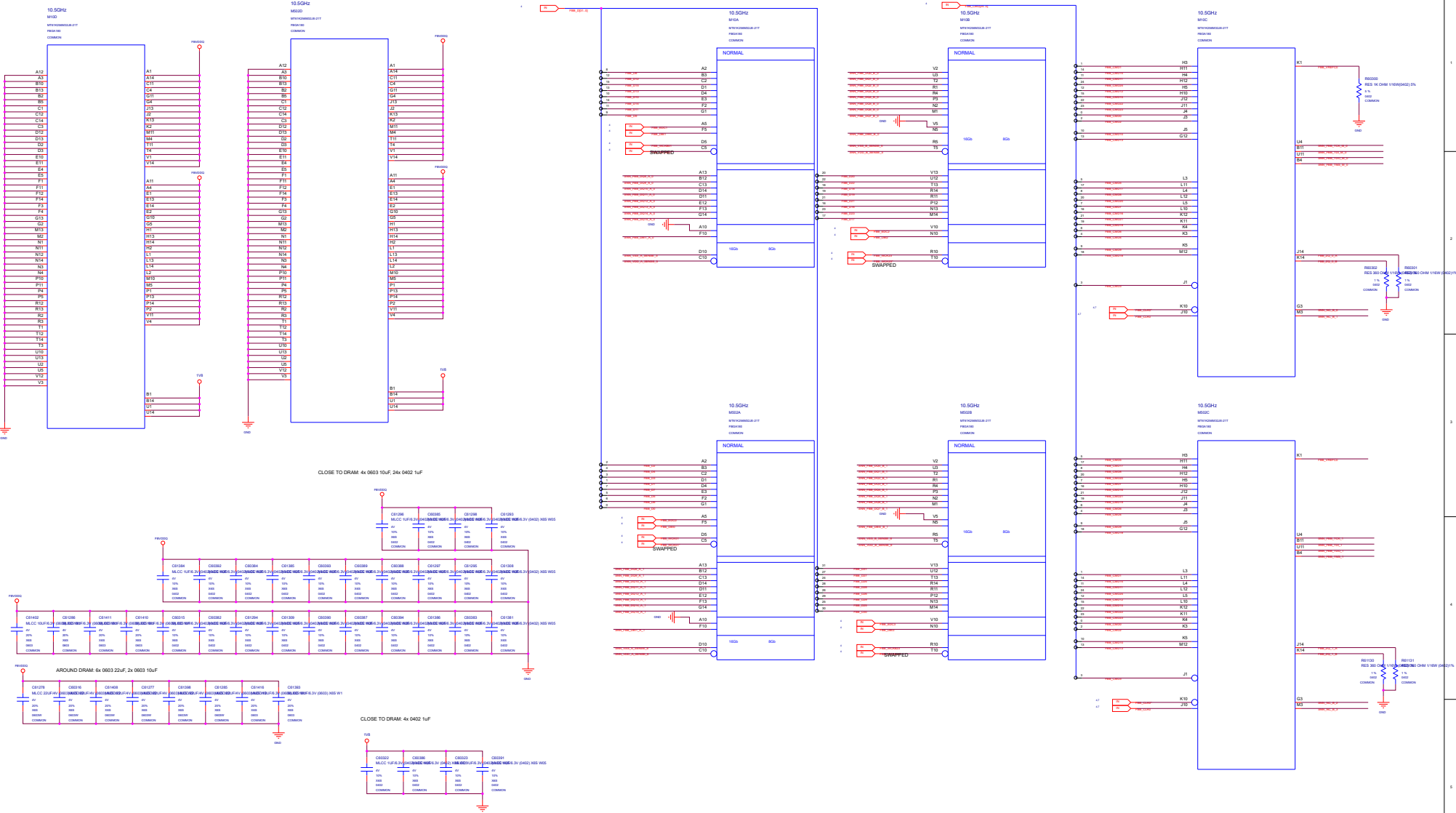
Block Diagram

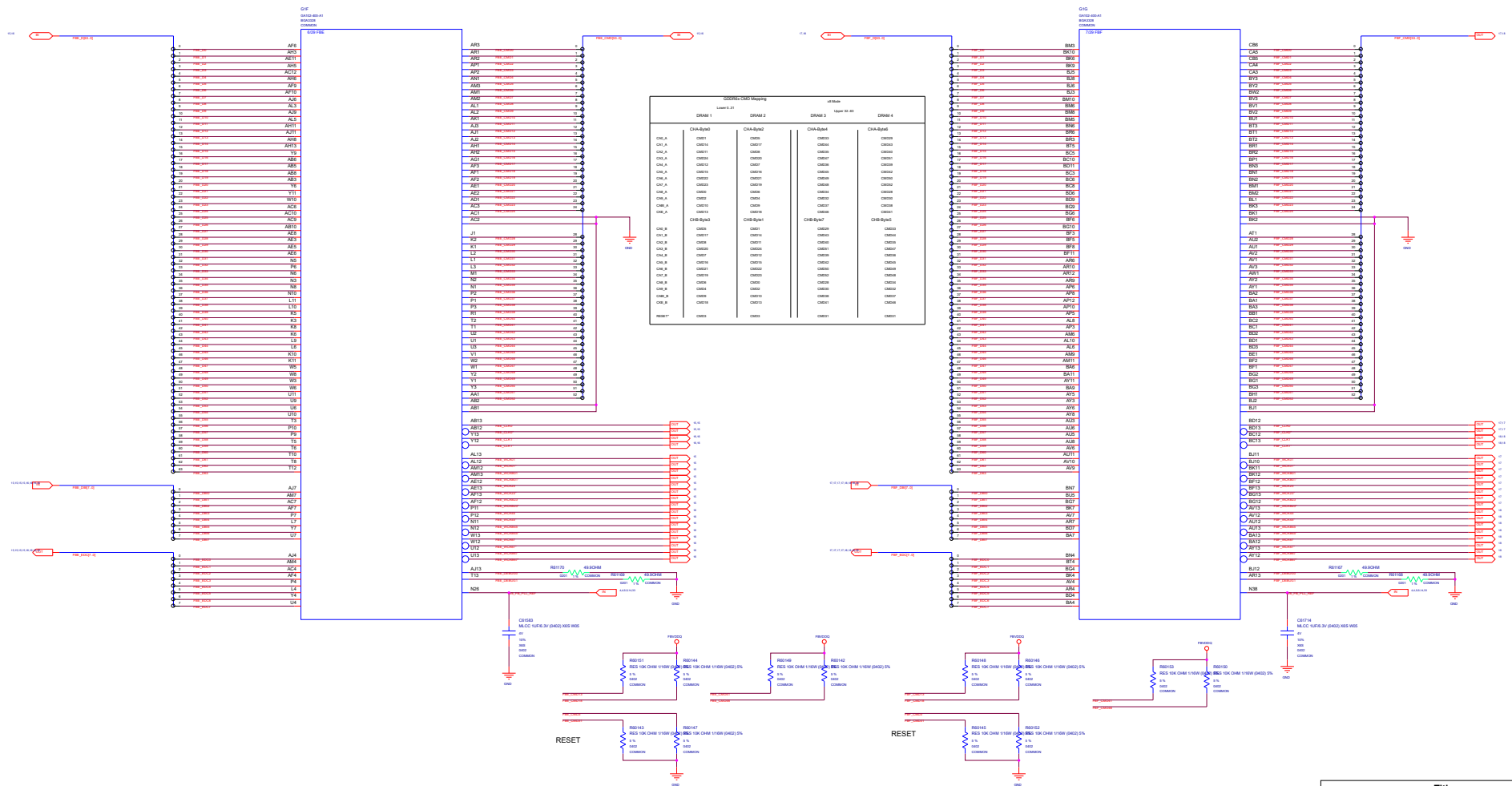


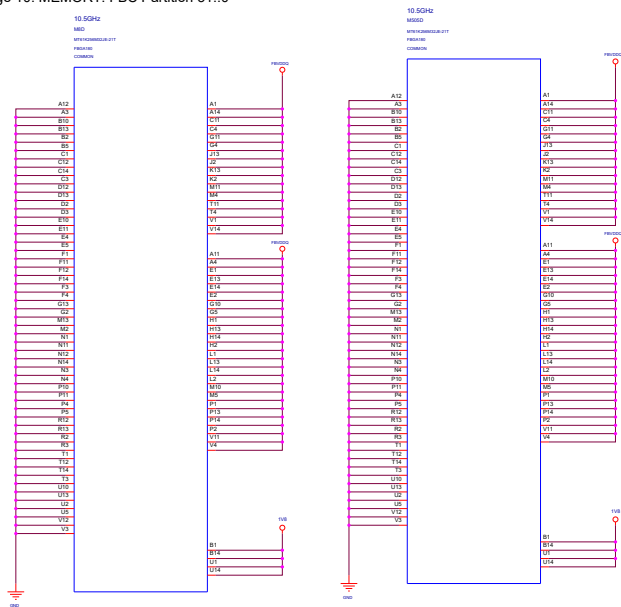


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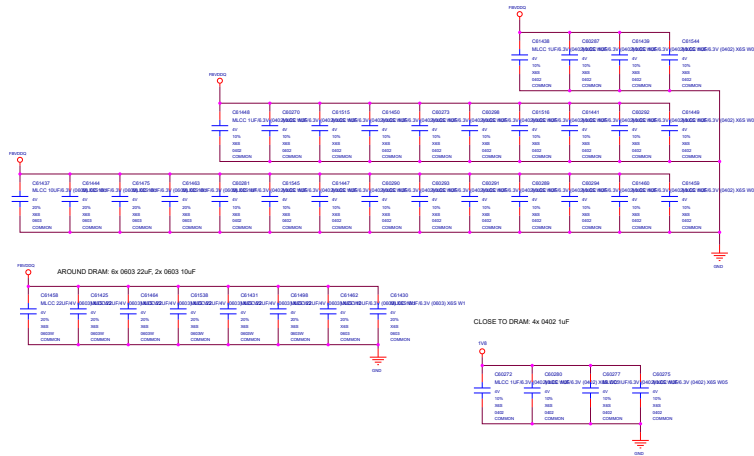




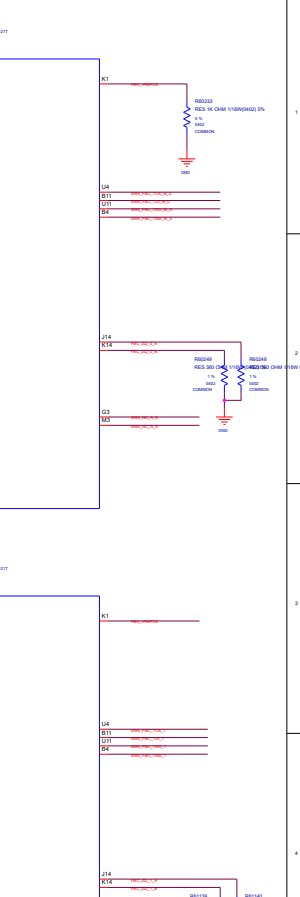
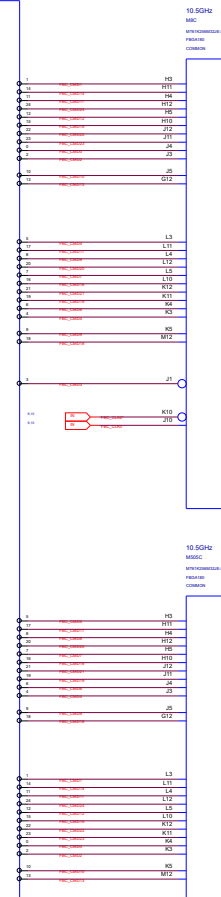
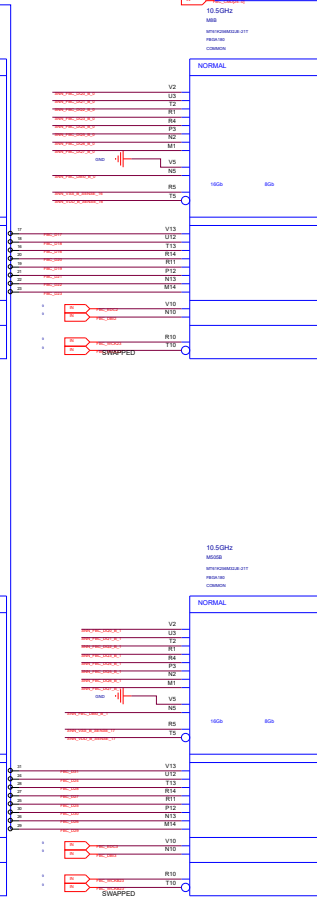
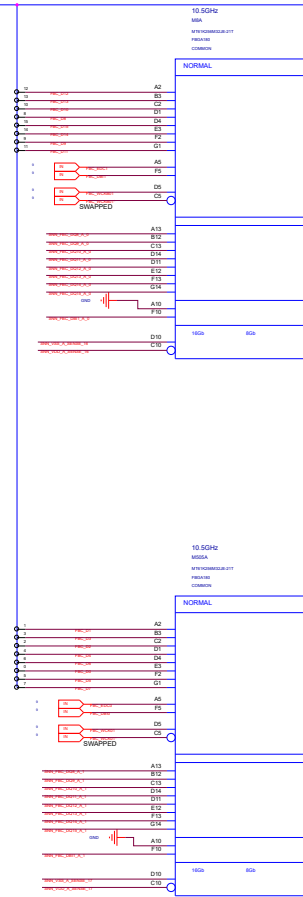


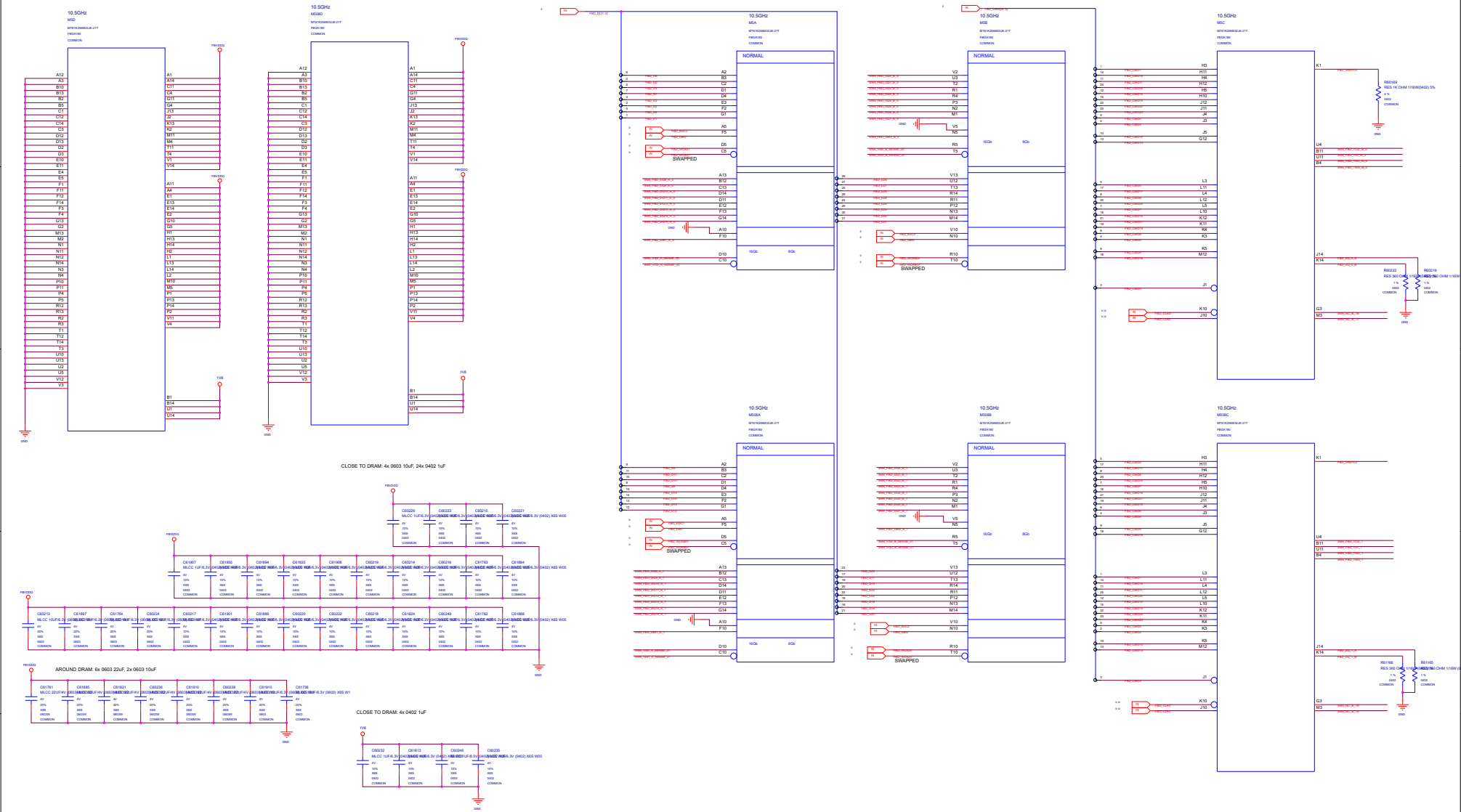


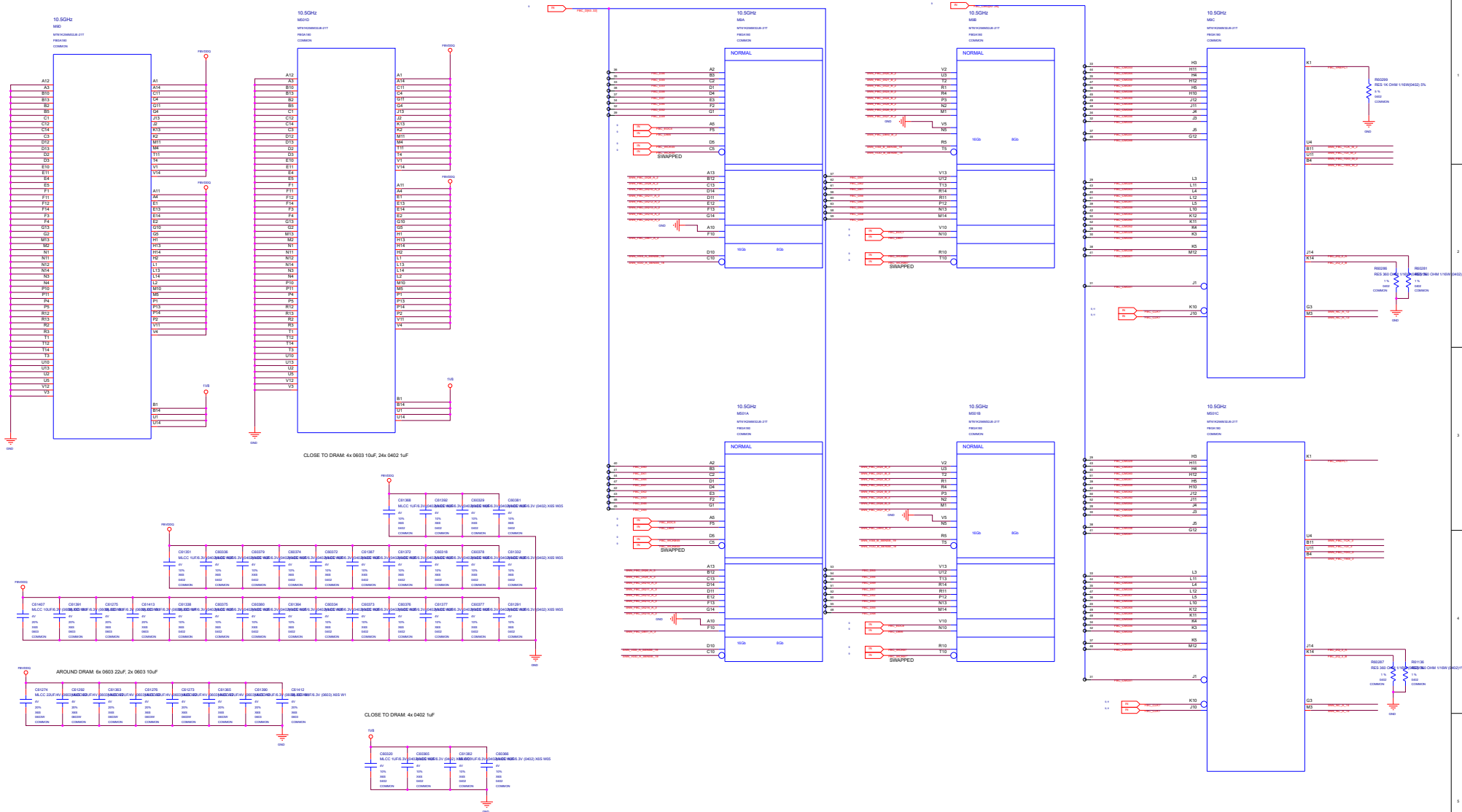
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CLOSE TO DRAM: 4x 0402 1uF

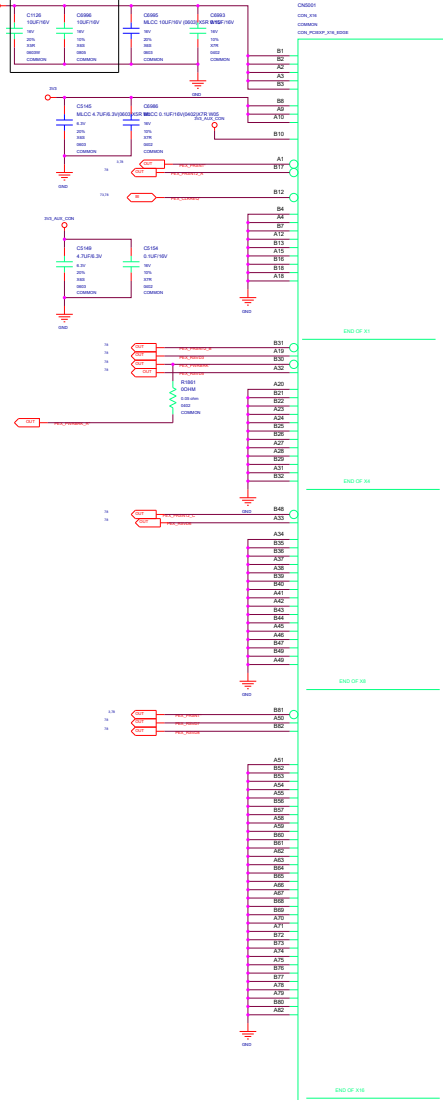




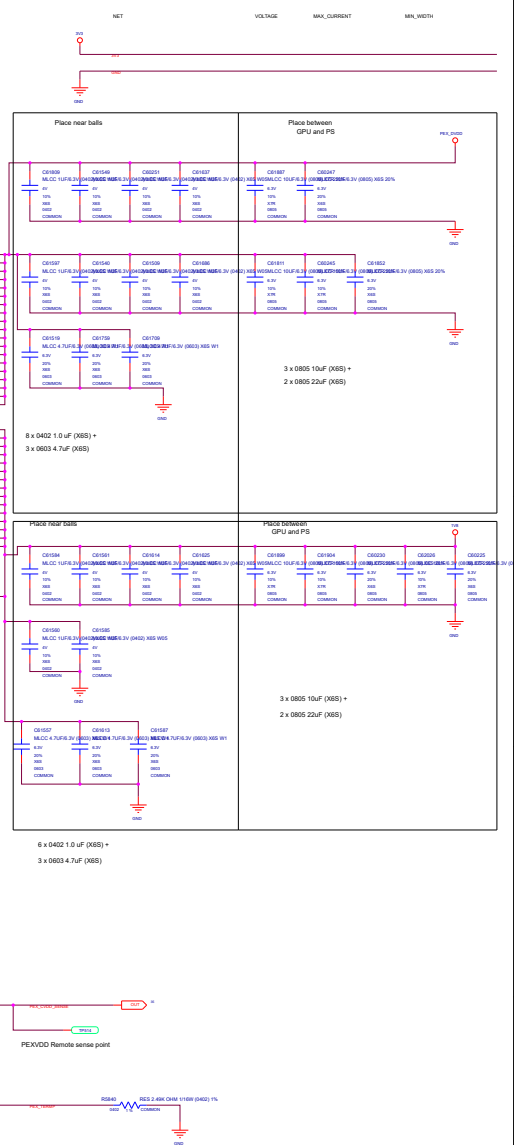
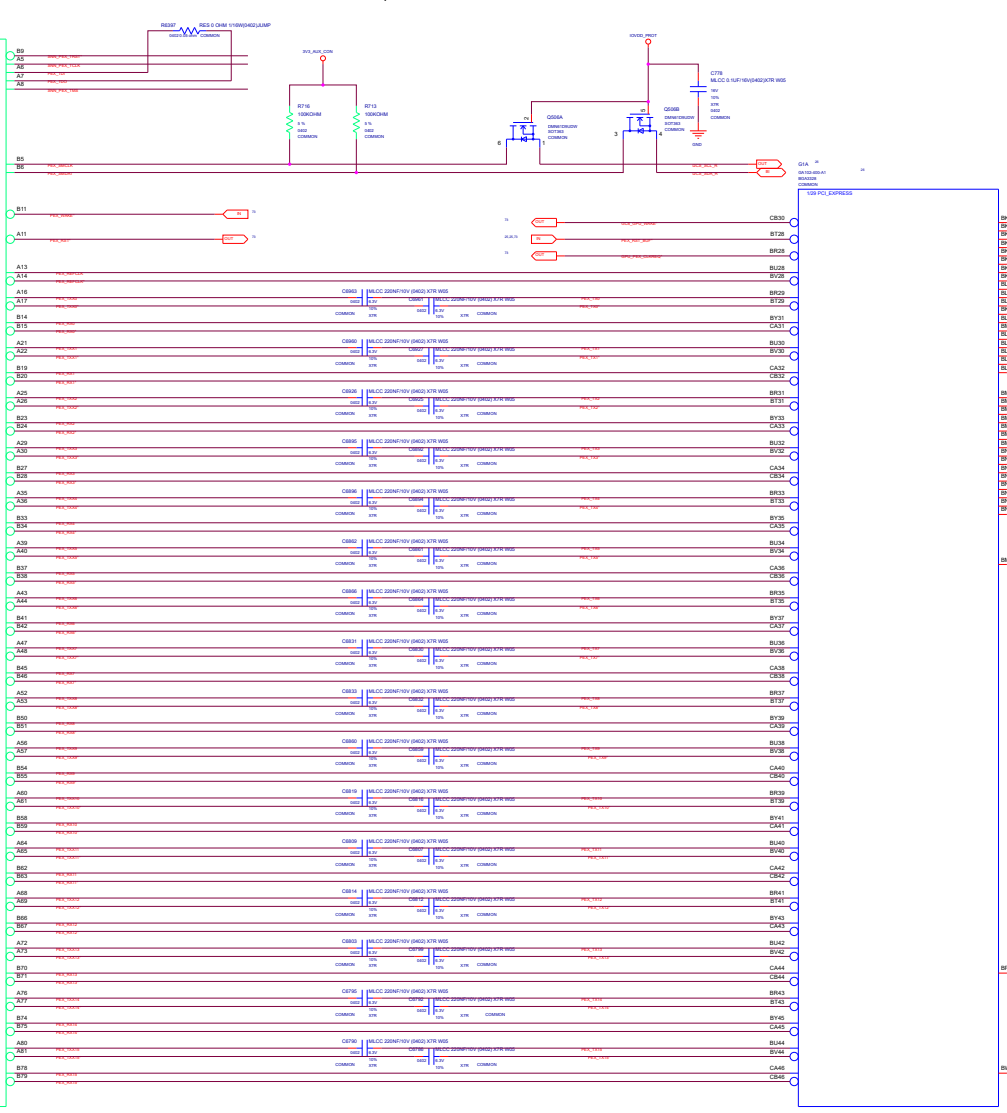


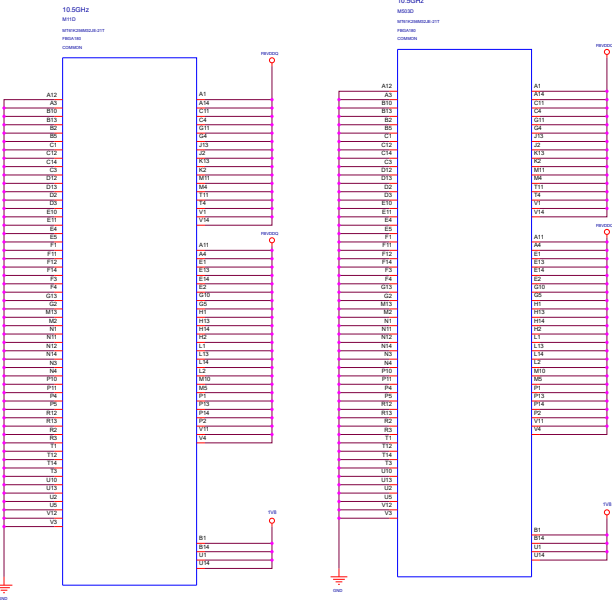


# PCB CO-LAYOUT

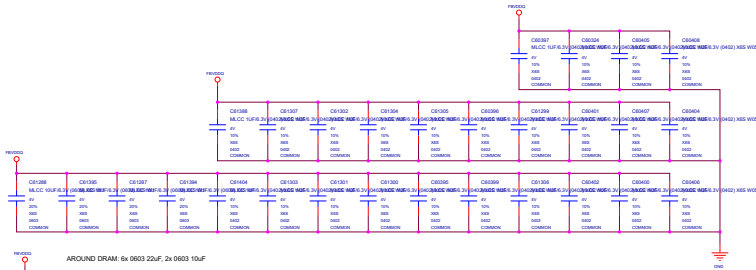


# PCI Express

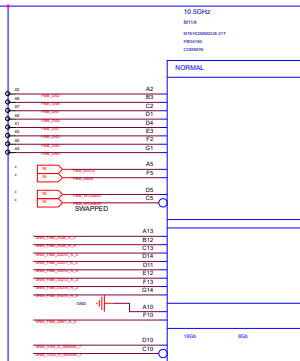
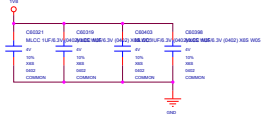




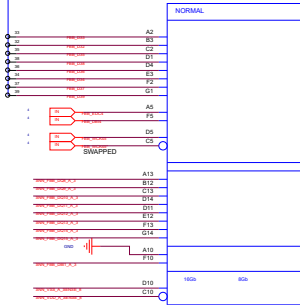
CLOSE TO DRAM: 4x 0603 10uF, 24x 0402 1uF



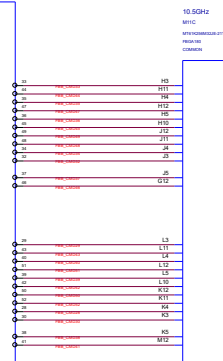
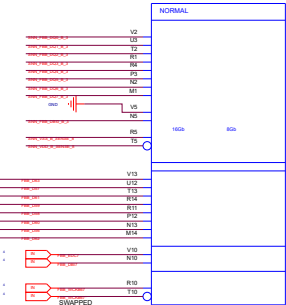
CLOSE TO DRAM: 4x 0402 1uF



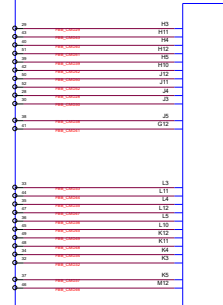
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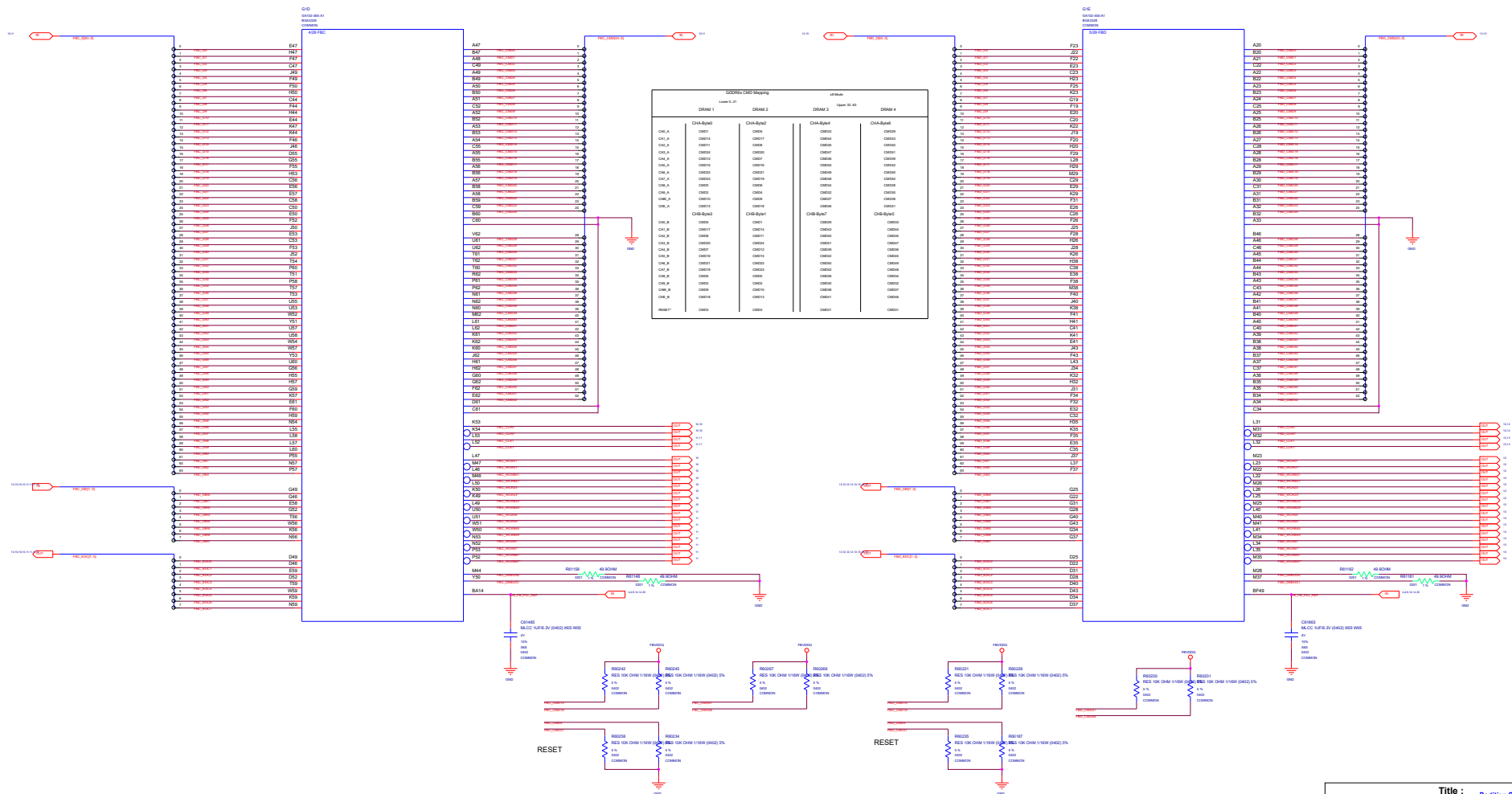


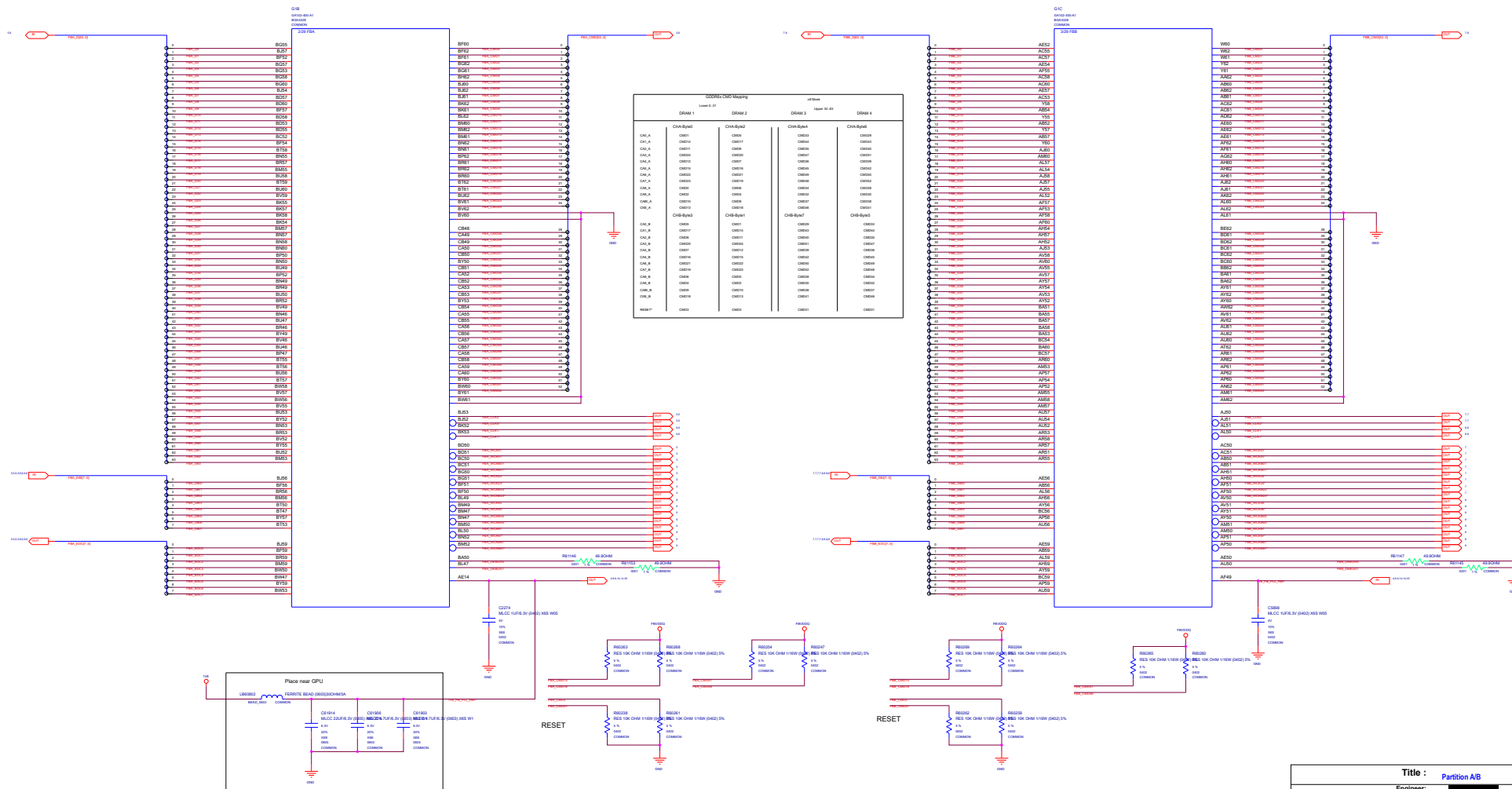
10.5GHz

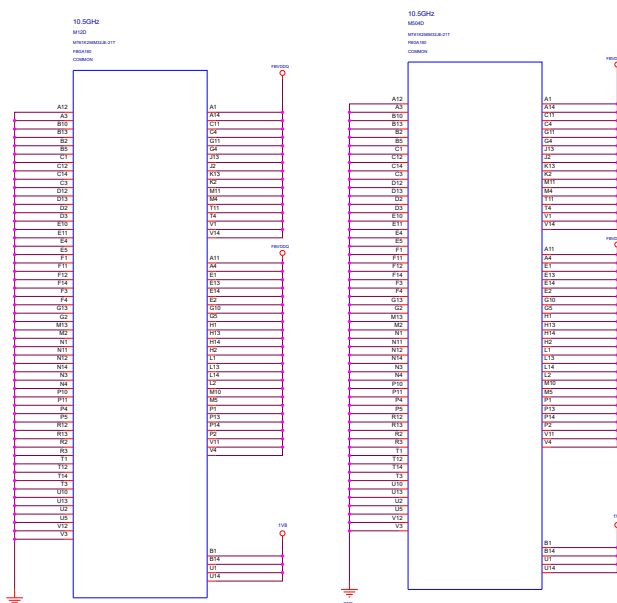


10.5GHz

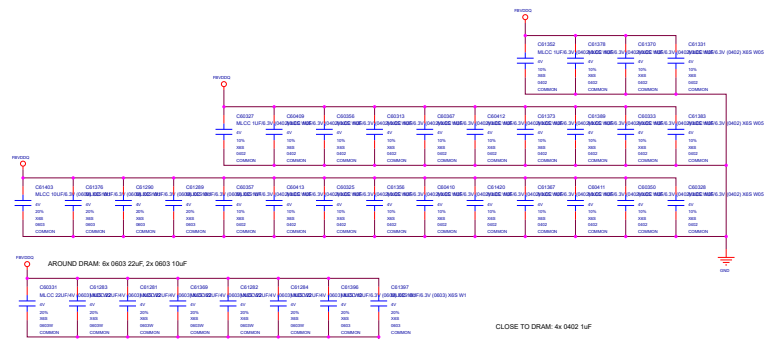




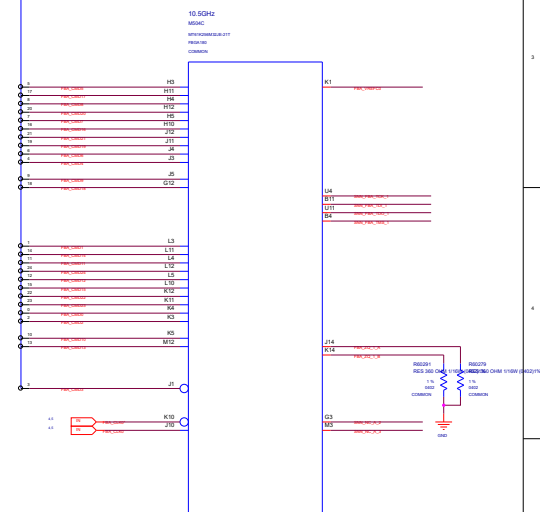
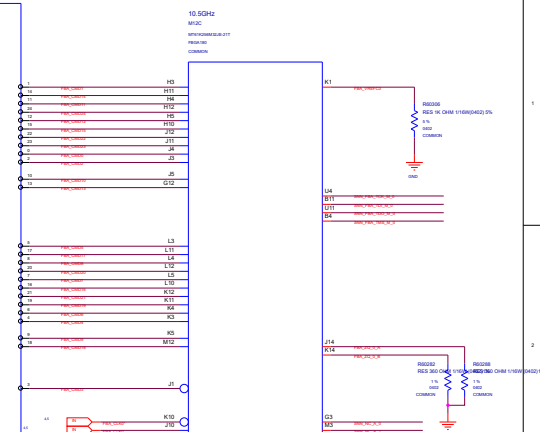
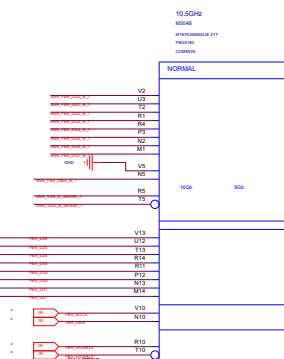
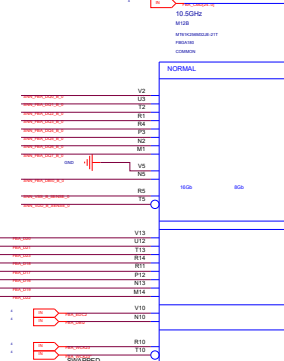
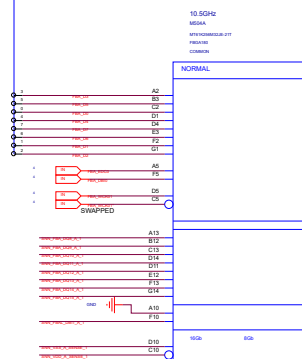
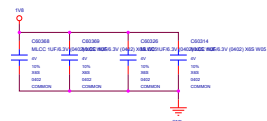


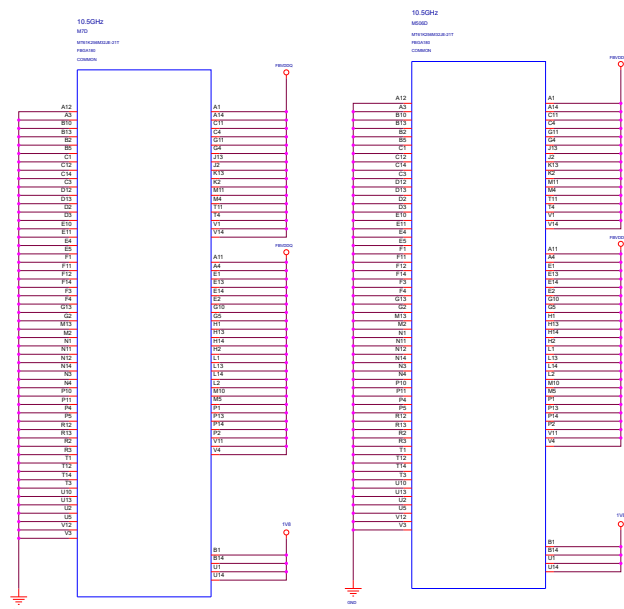


CLOSE TO DRAM: 4x 0603 10uF, 24x 0402 1uF

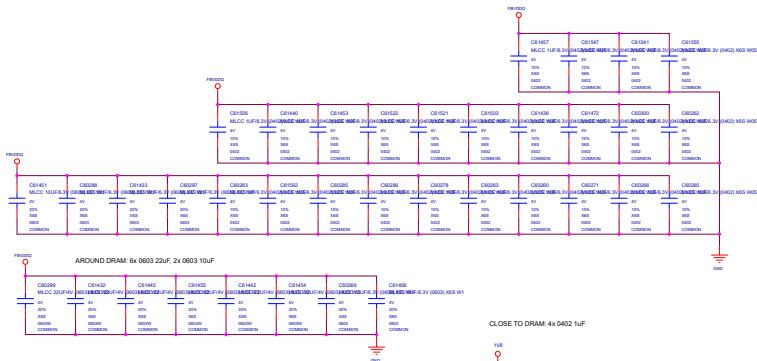


CLOSE TO DRAM: 4x 0402 1uF

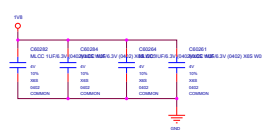


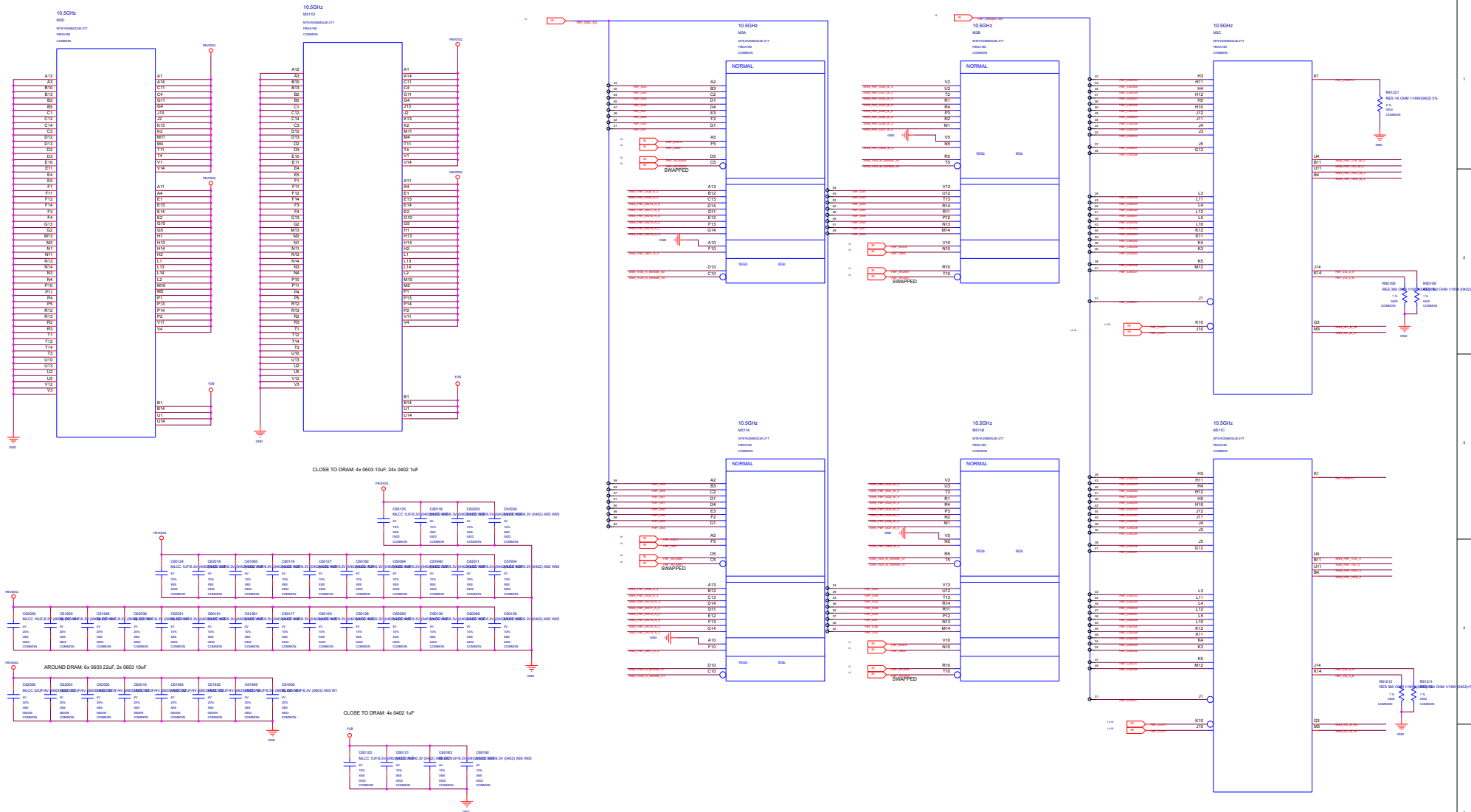


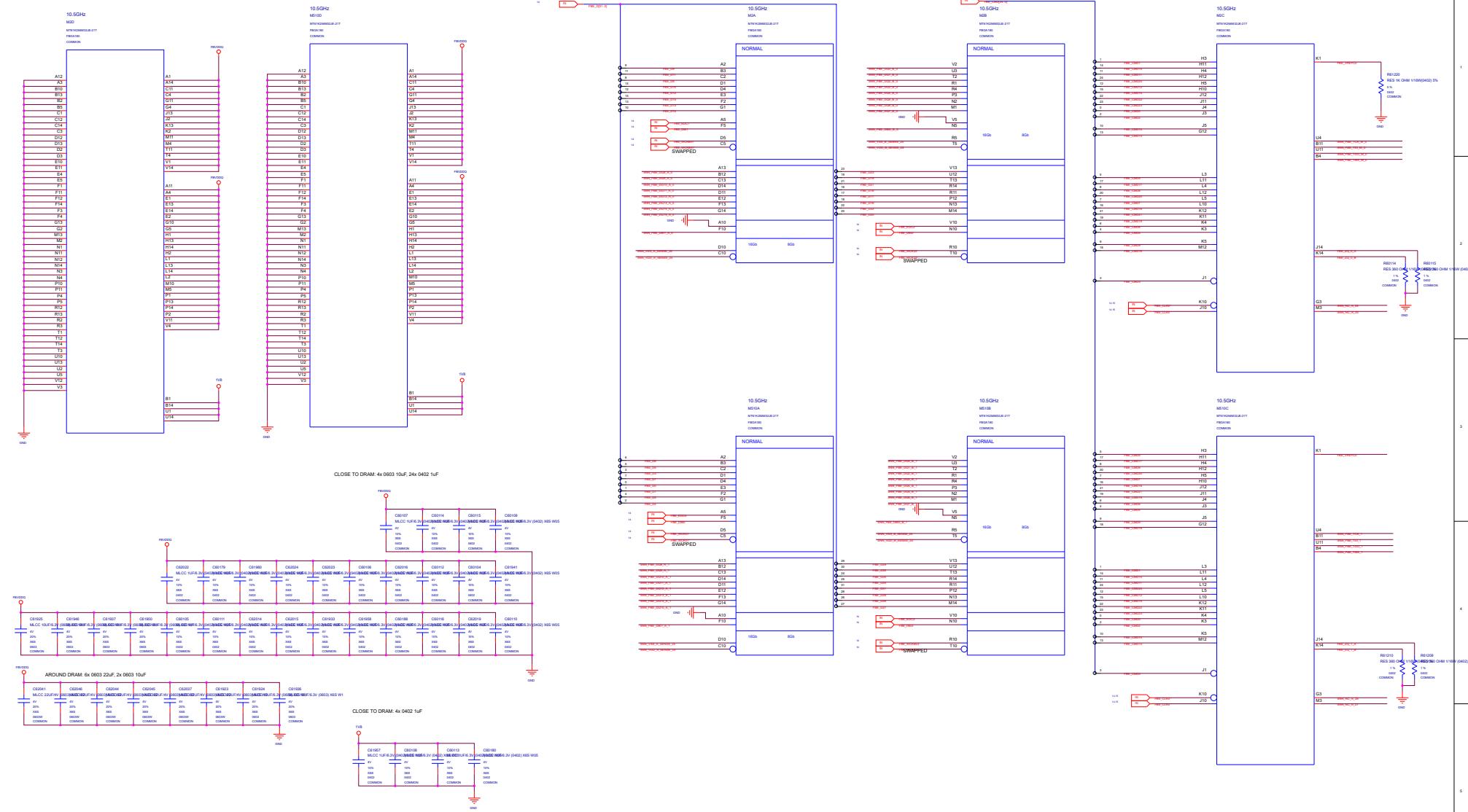
CLOSE TO DRAM: 4x 0603 10uF, 24x 0402 1uF



CLOSE TO DRAM: 4x 0402 1uF





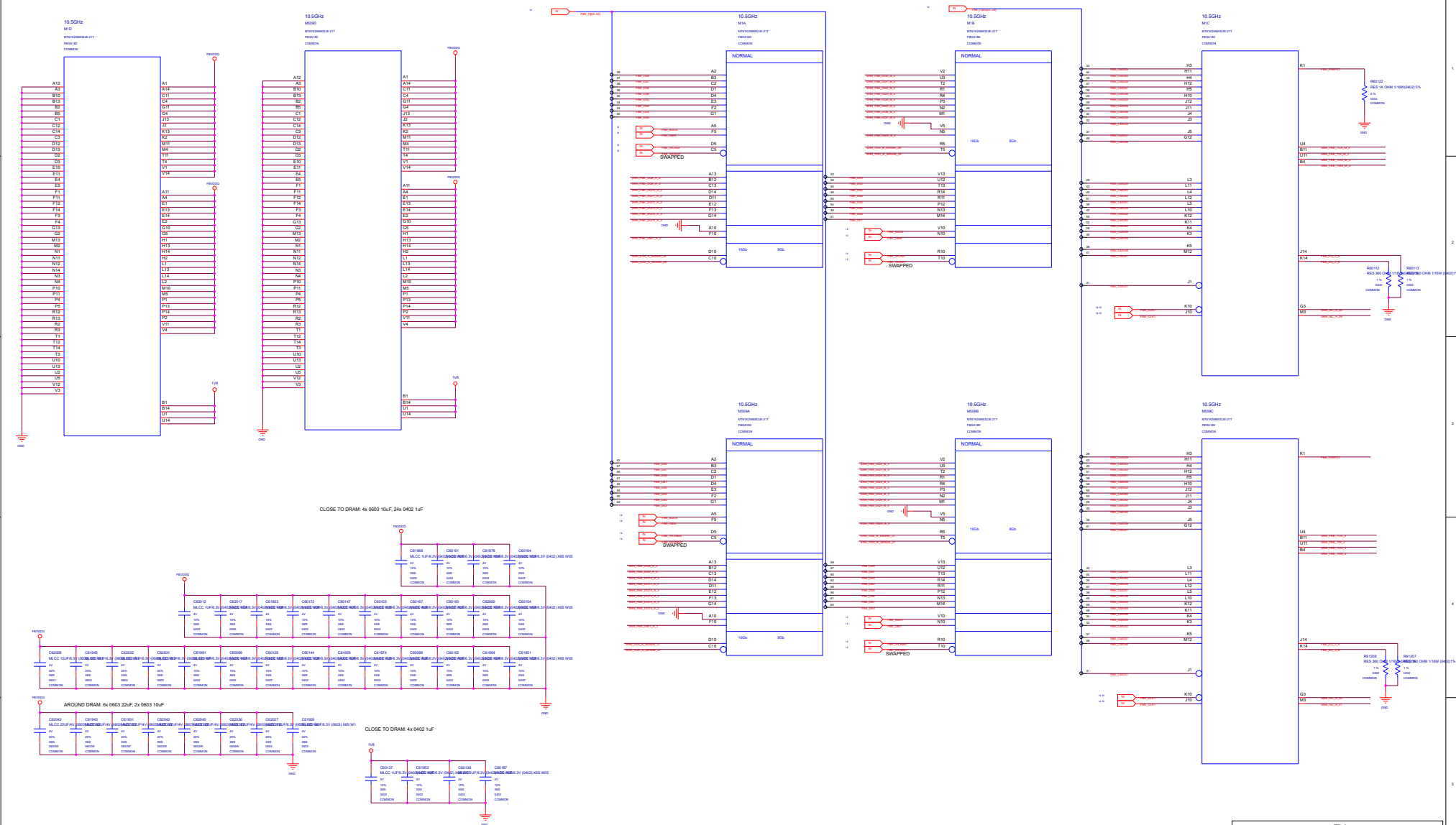


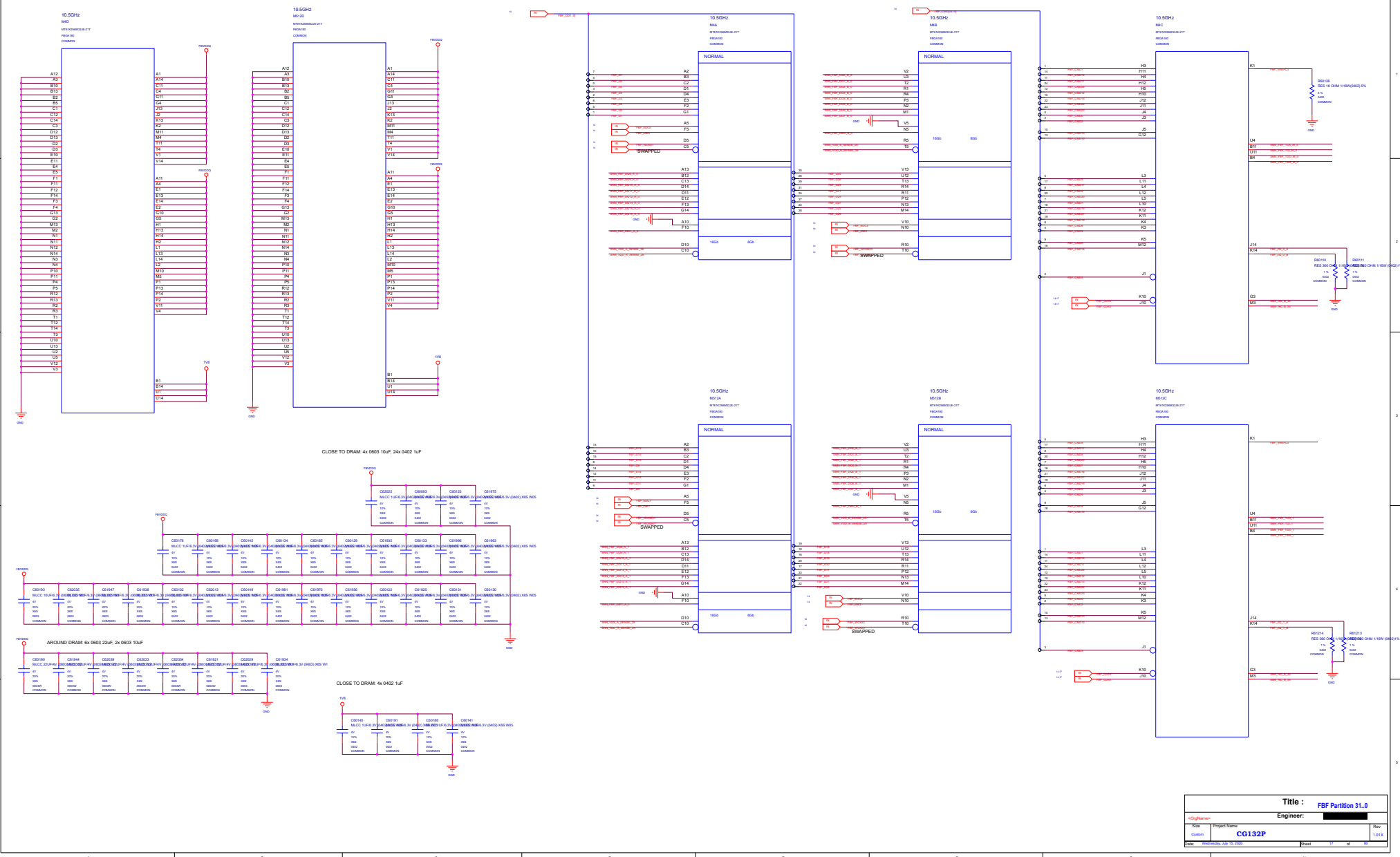


## NVVDD

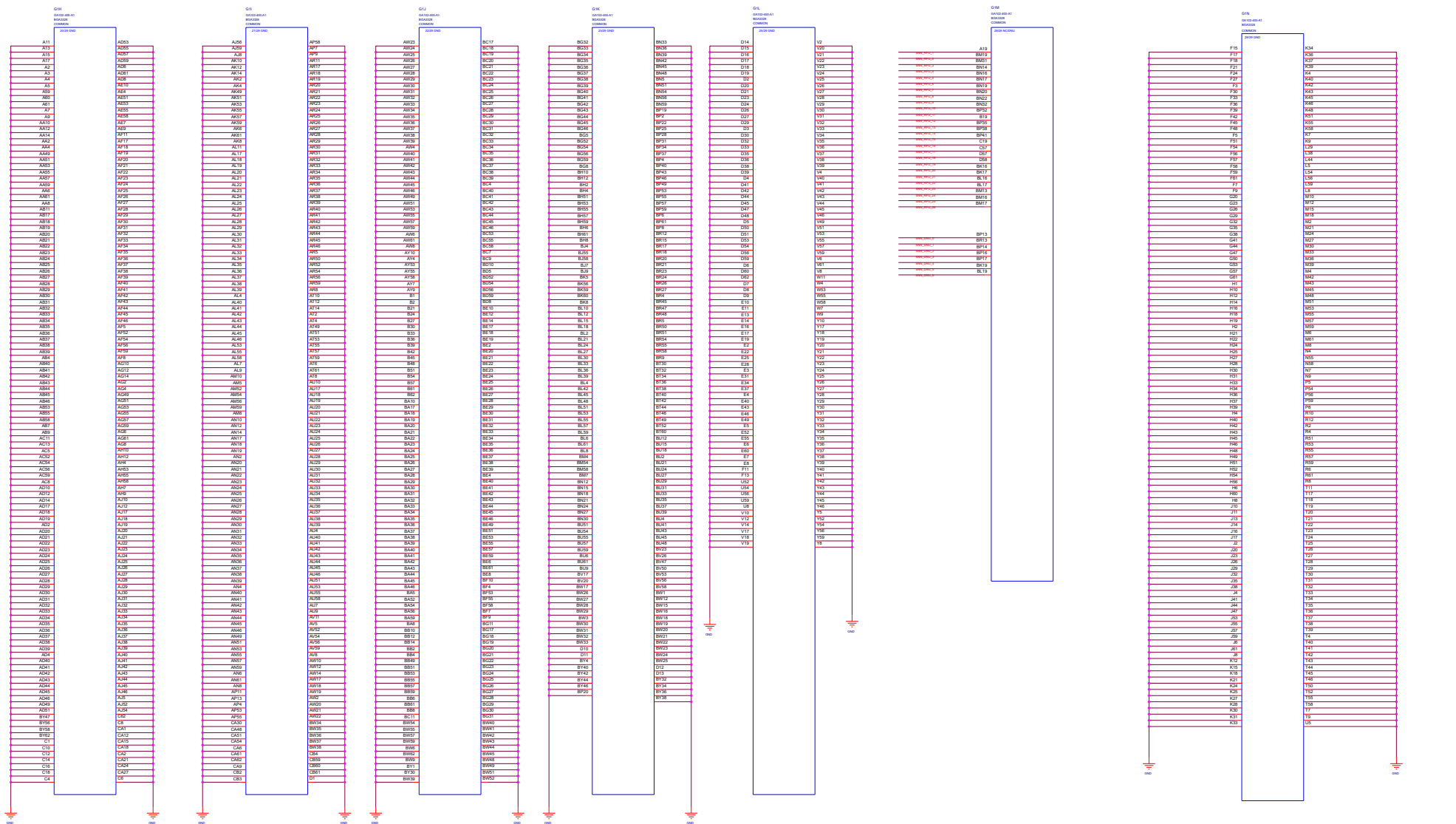
## UNDER GPU

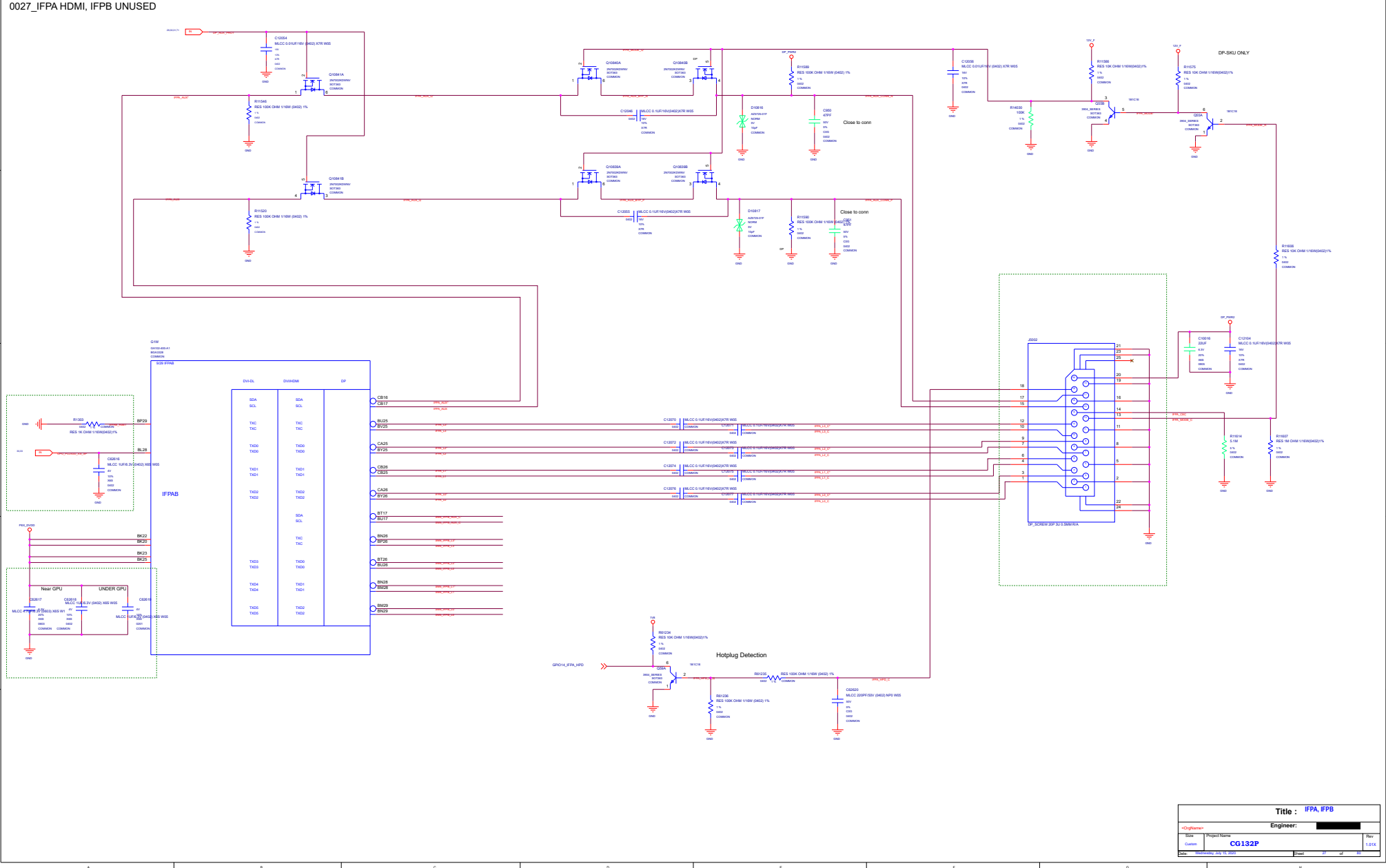




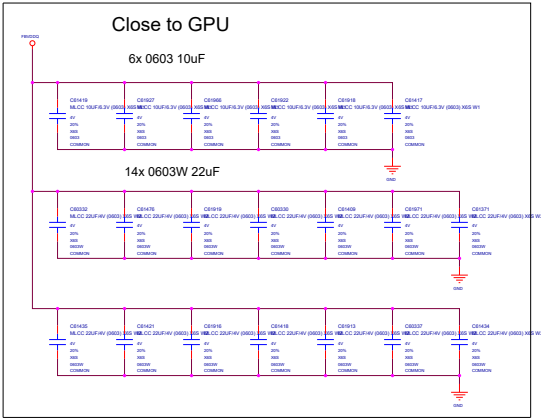
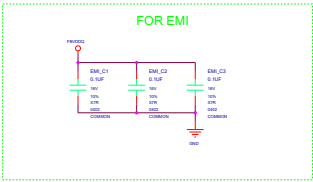
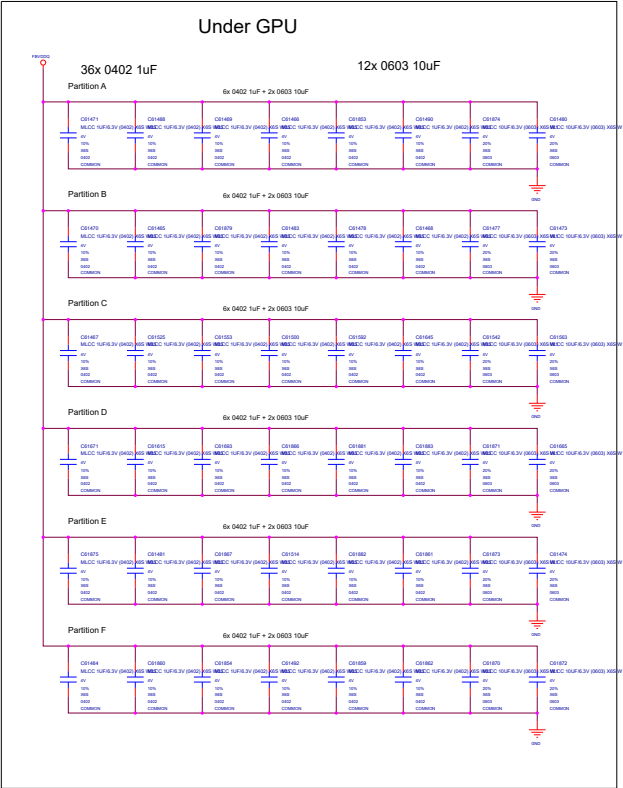


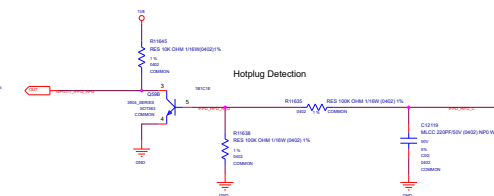
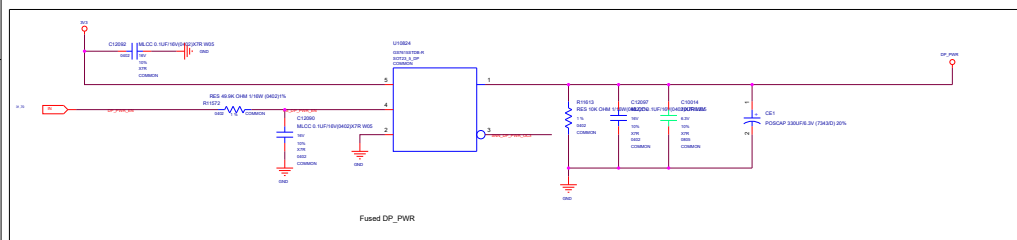
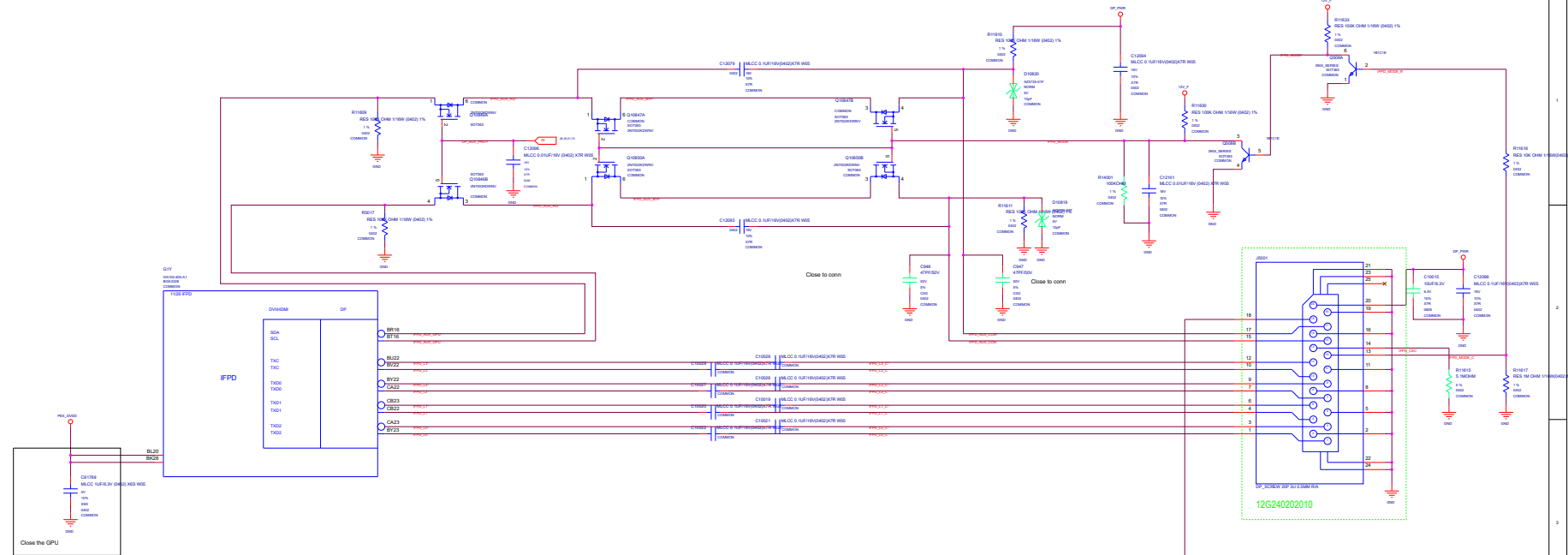
## GPU GND, RFUs &amp; RSVD





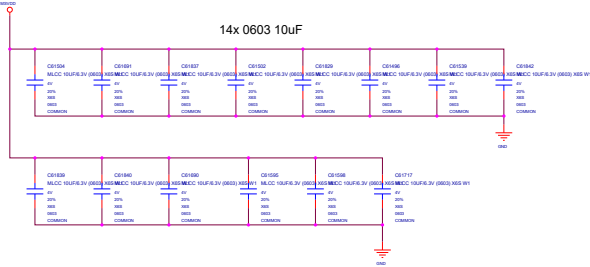
FBVDDQ



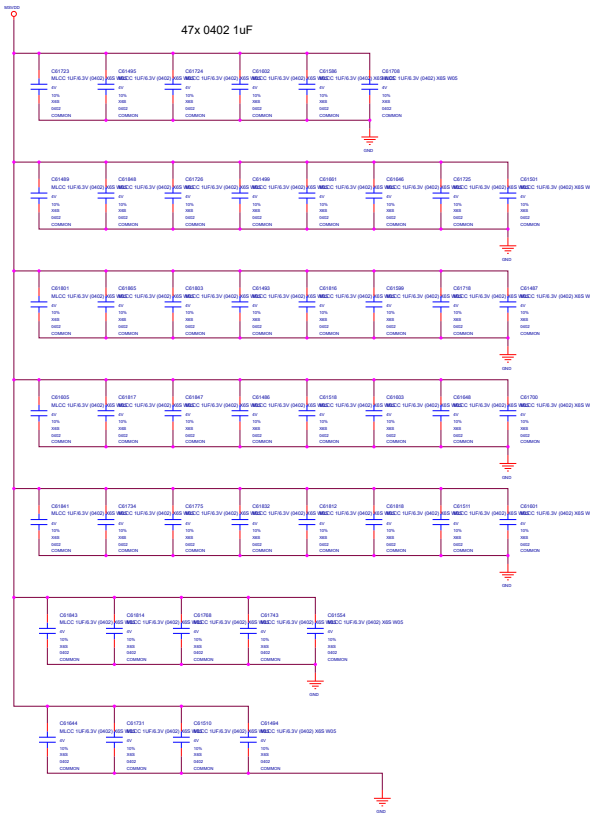


# UNDER GPU

## MSVDD



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

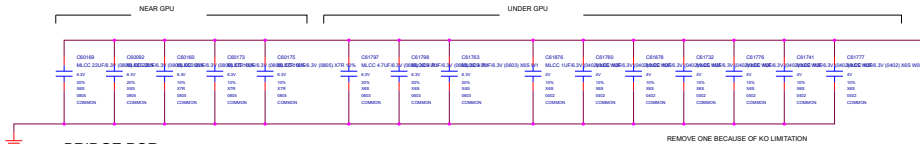




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Title :		BLANK
Engineer:		
Drawn	Project Name	
Checked	CG132P	
Date	Revised	By

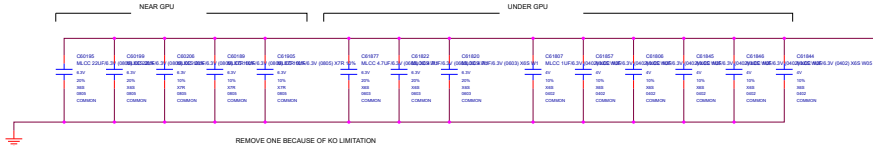
## NVHS Interface and FRAME LOCK



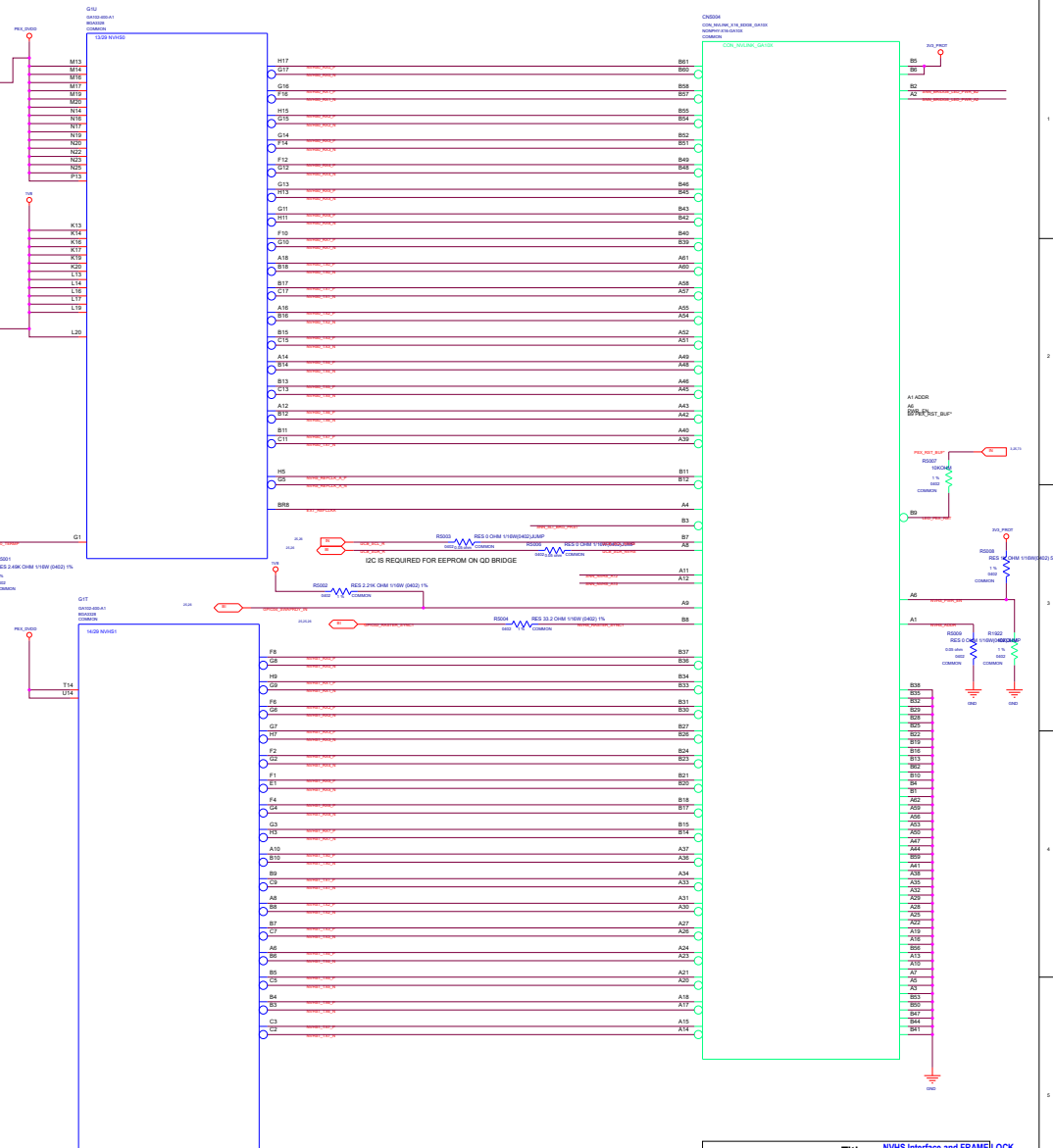
BRIDGE POR

LED -> NO

ID ROM ->YES

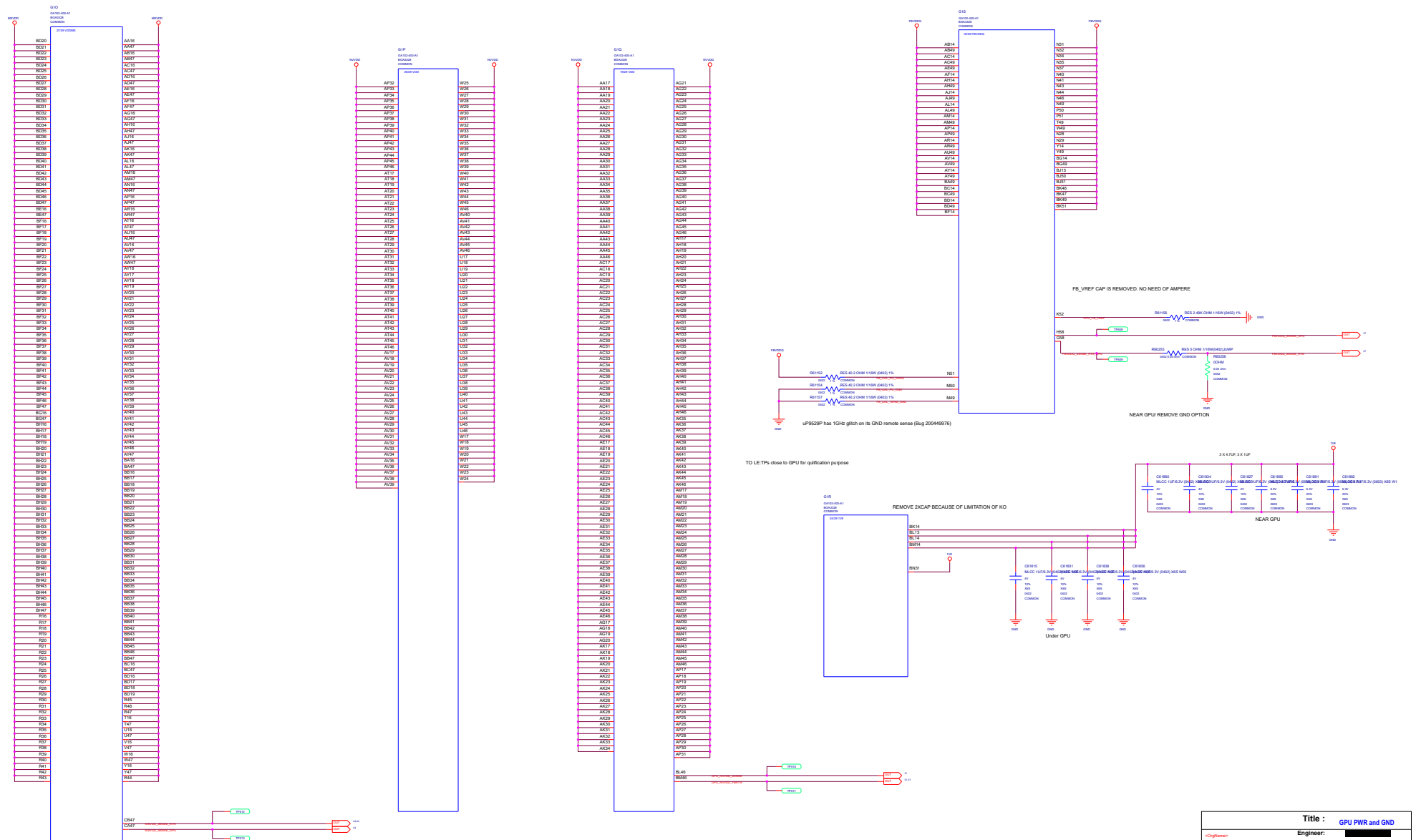


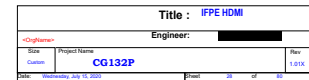
REMOVE ONE BECAUSE OF KO LIMITATION

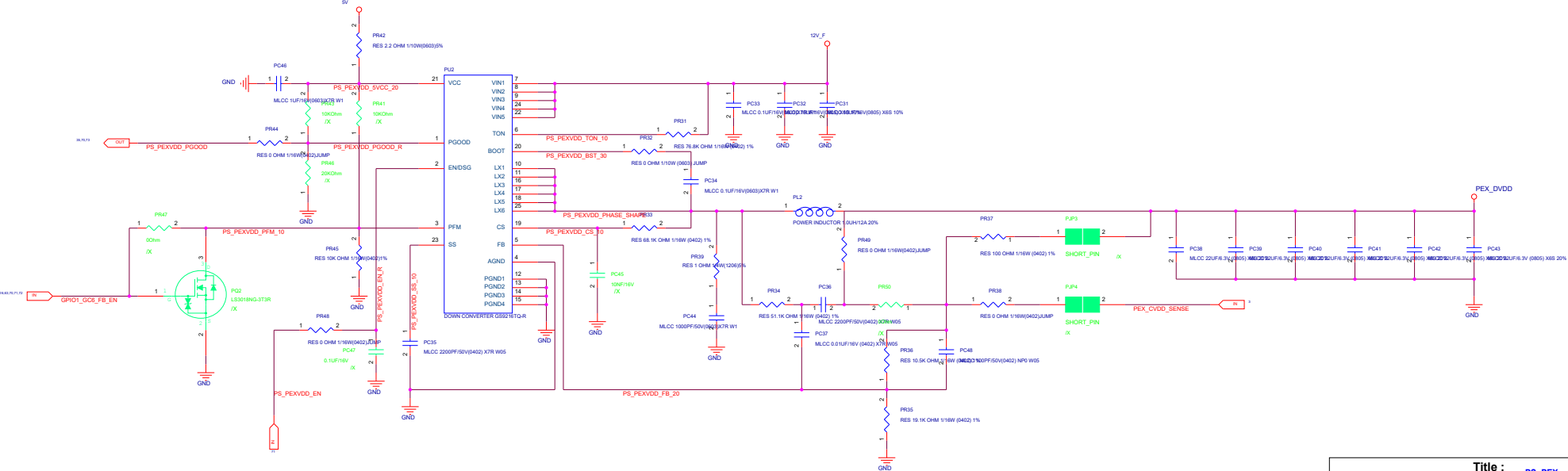


Remove FRAMELOCK

## GPU PWR and GND

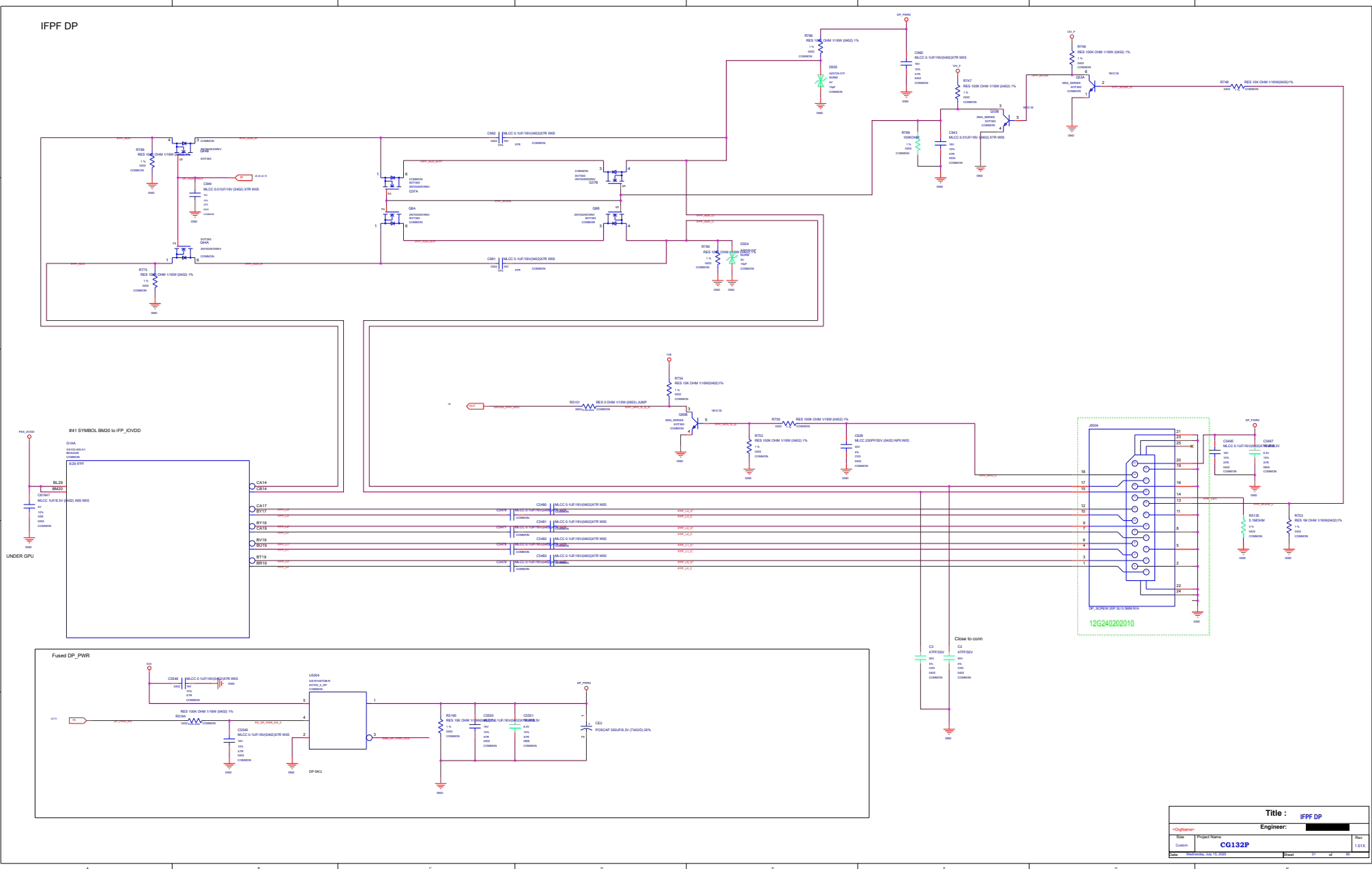


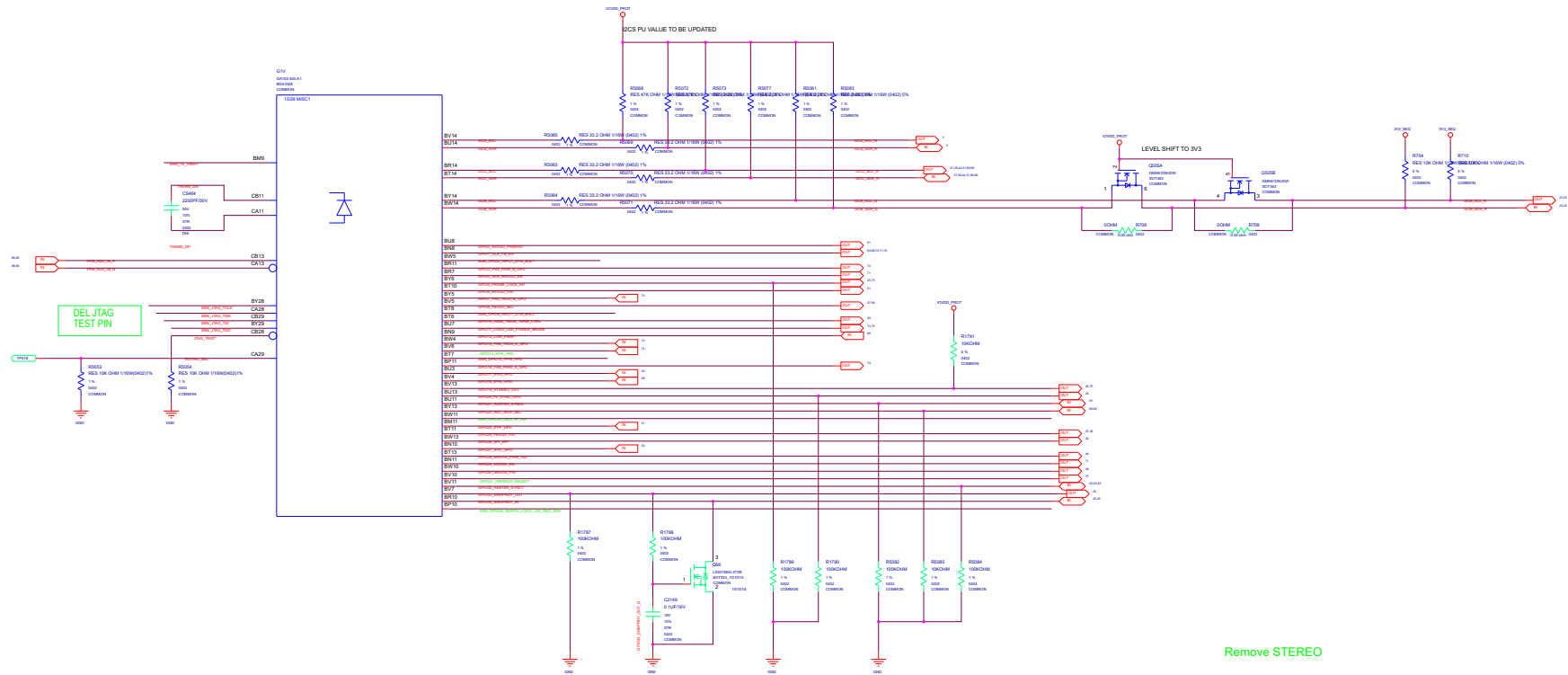




Title : <b>PS: PEX</b>		
Engineer: <span style="background-color: black; color: black;">XXXXXXXXXX</span>		
Size Custom	Project Name <b>CG132P</b>	Rev 1.01X
Date: Wednesday, July 15, 2020	Sheet 36	of 80

# IFPF DP





Remove STEREO



# MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	RAMCFG MICRON 8Gb 19Gbps
L	H	L	0001	RAMCFG TBD
H	L	L	0010	RAMCFG TBD
H	L	H	0011	RAMCFG TBD
H	L	H	0101	RAMCFG MICRON 8Gb 21Gbps

DEFAULT

H:High :Tied to 1.8V  
M:Middle:Tied to 0.9V  
L:Low :Tied to 0V

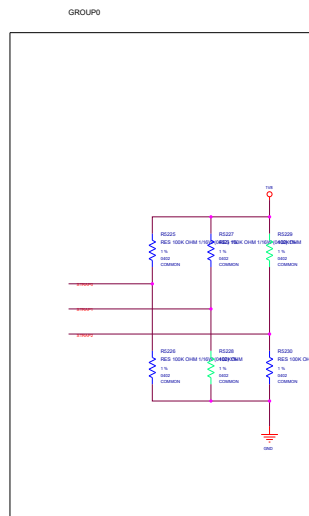
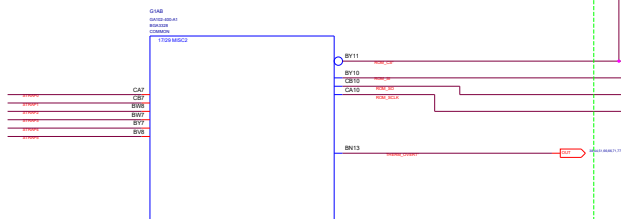
ROM_SO	ROM_S0	ROM_SCLK	SMARTFAN[2:0]_FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

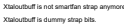
DEFAULT

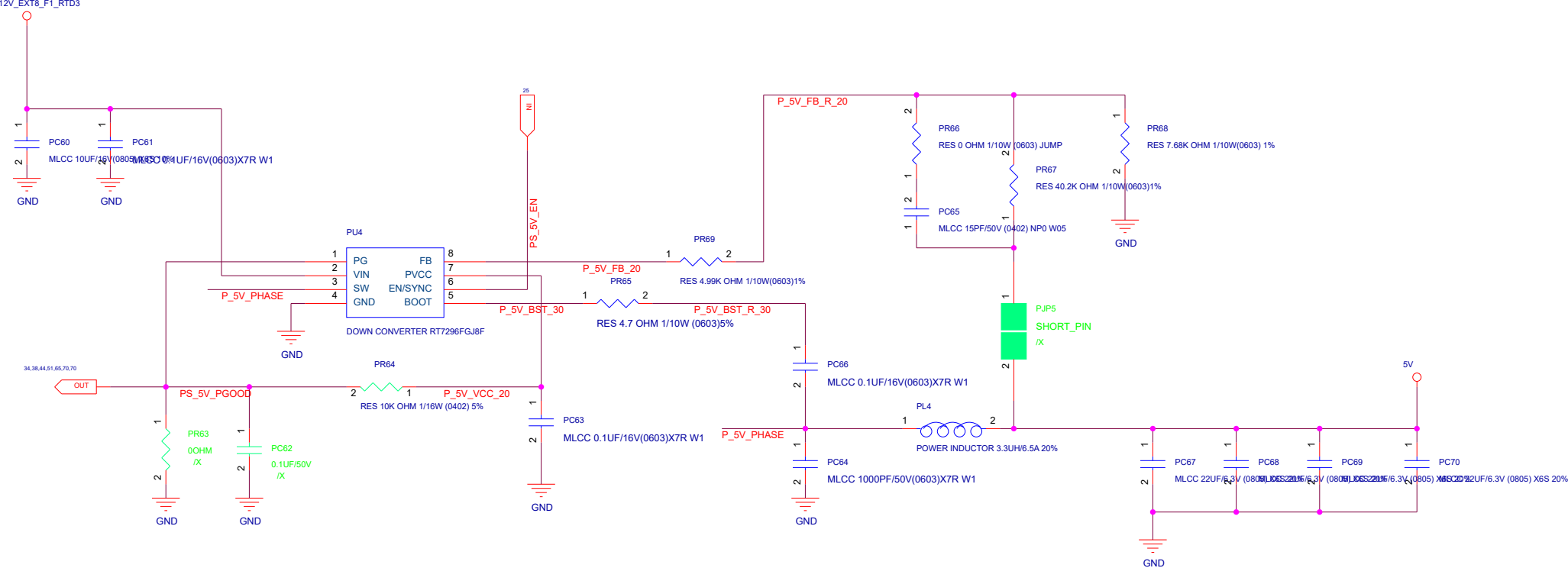
1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	H	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

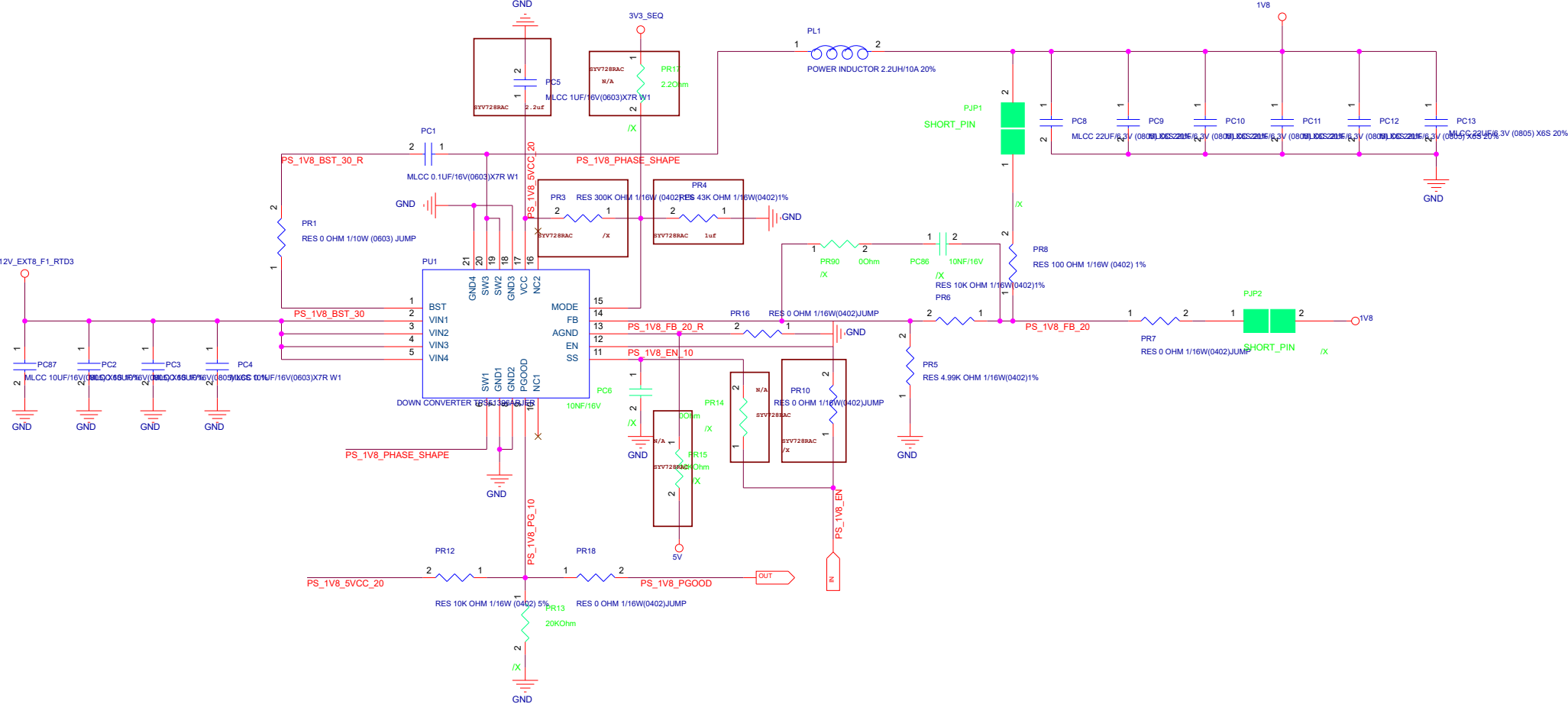




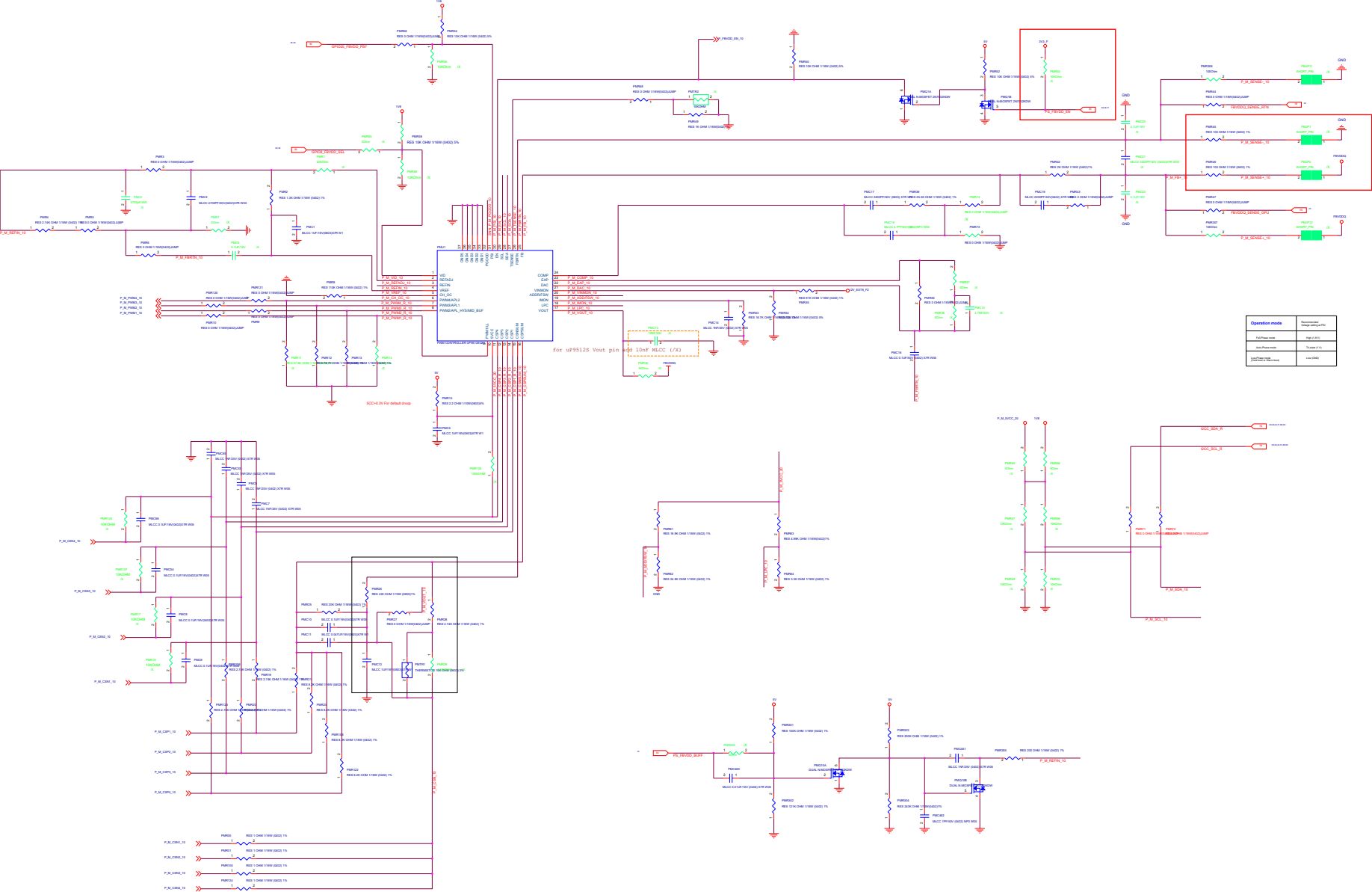


Title : PS: 5V		
Engineer: [REDACTED]		
<OrgName>		
Size	Project Name	Rev
A4	CG132P	1.01X
Date: Wednesday, July 15, 2020		Sheet 34 of 80

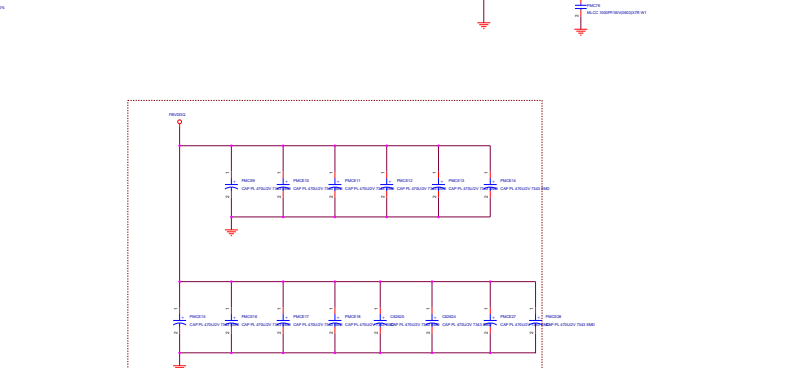
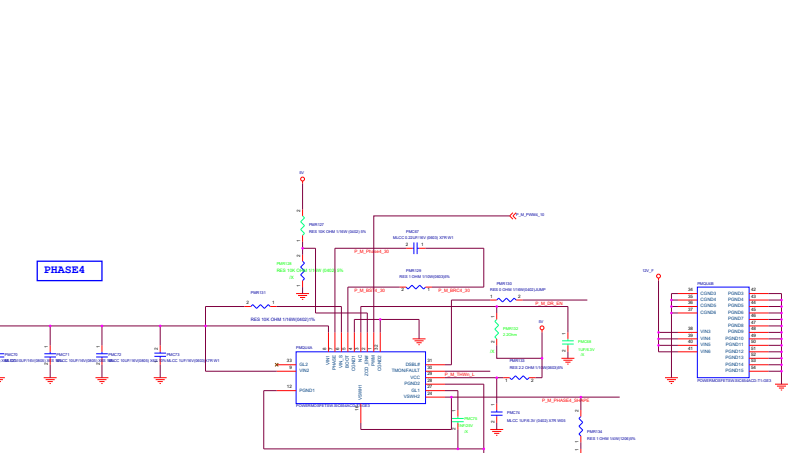
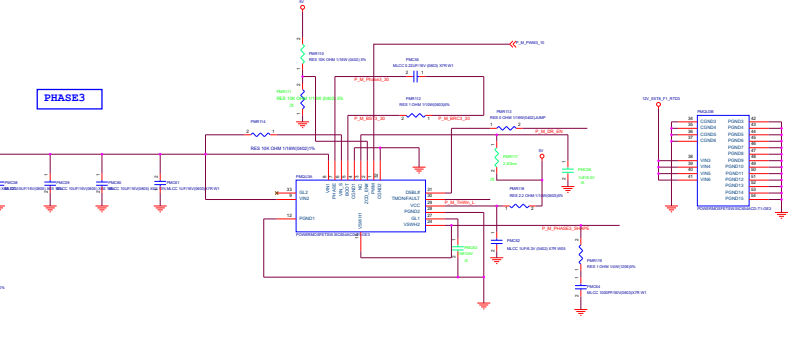




Title : PS: 1V8			
Engineer: [REDACTED]			
Size Custom	Project Name CG132P		Rev 1.01X
Date: Wednesday, July 15, 2020	Sheet	35	of 80



Operation mode	Measurement range (mV)
Auto mode	0.1V
Manual mode	0.1V
Auto mode	0.1V



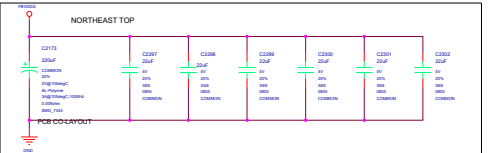
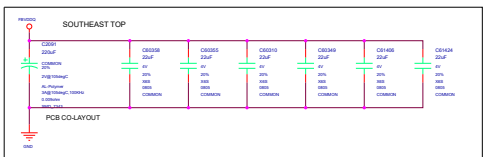
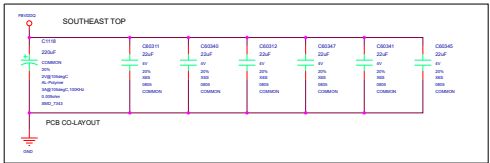
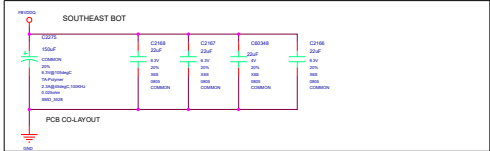
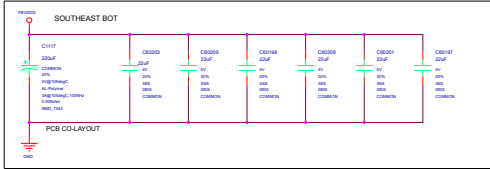
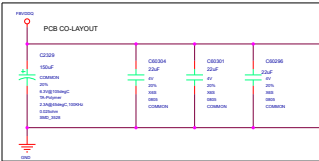
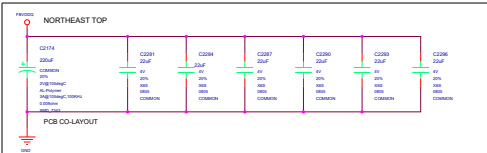
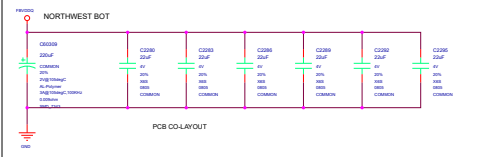
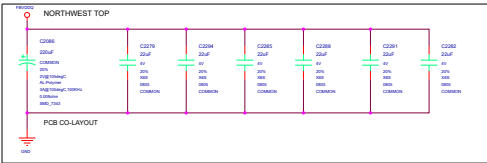
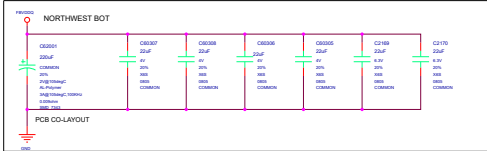
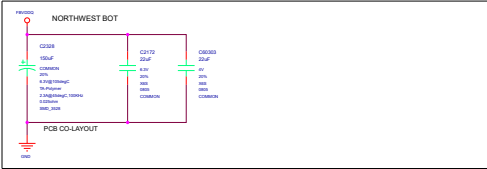
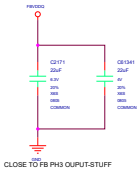
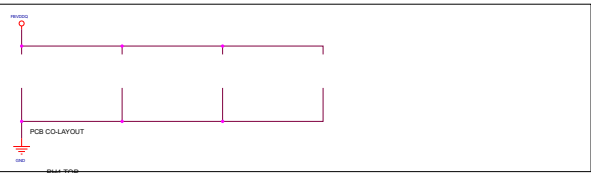
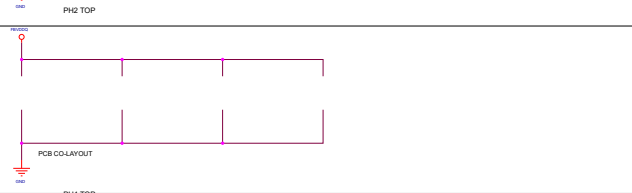
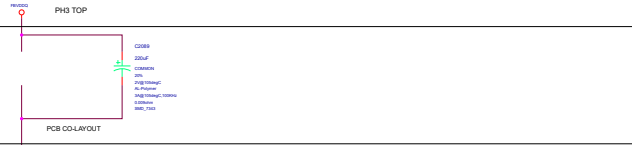
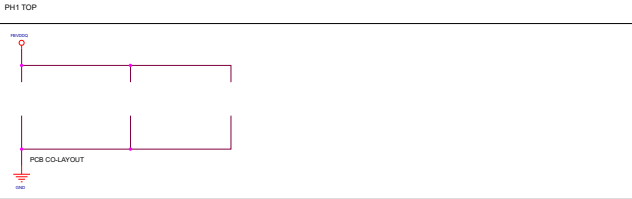
AND GATE LOGIC FOR P-BOARD			
GPI01	GPI023	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

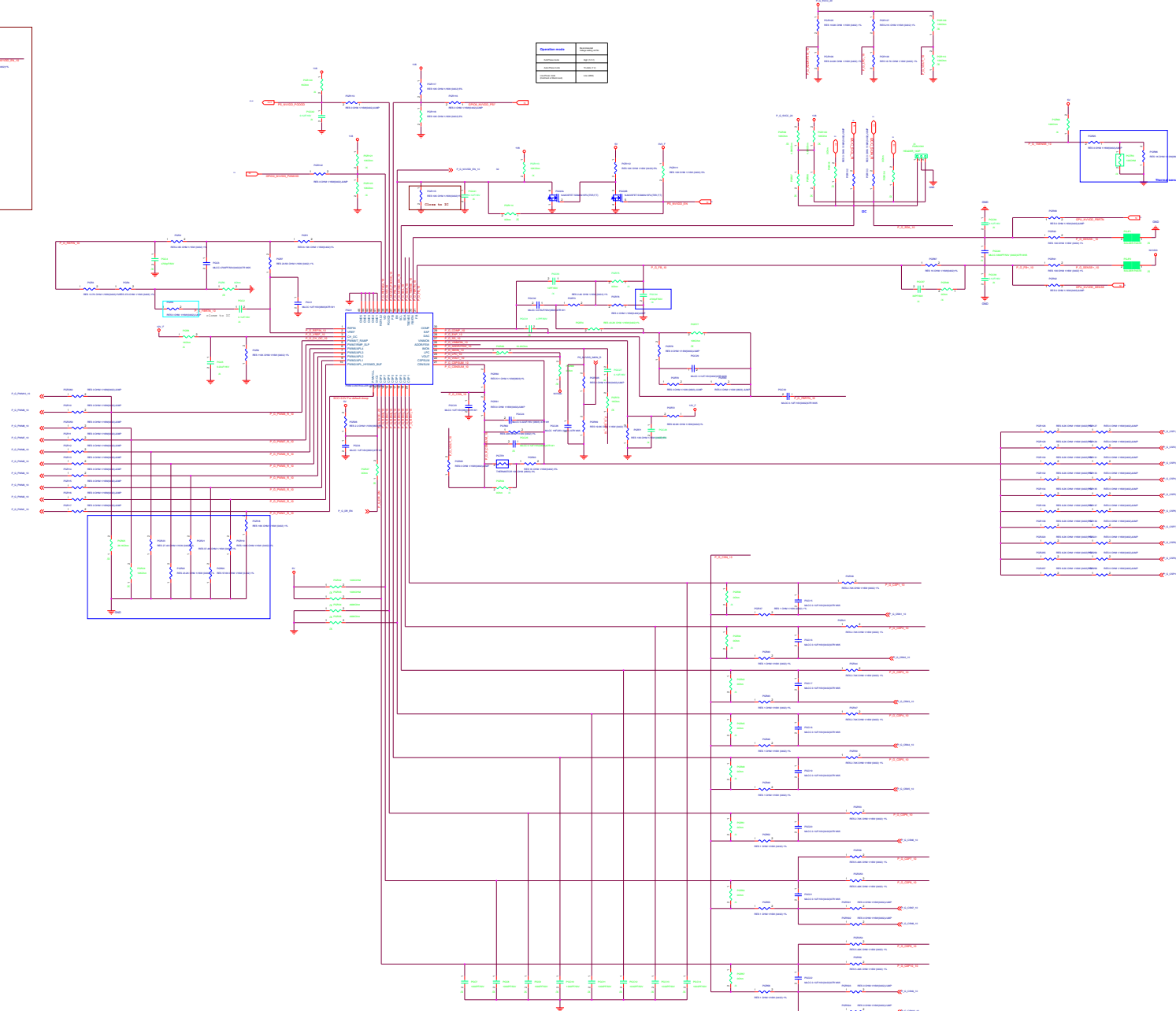
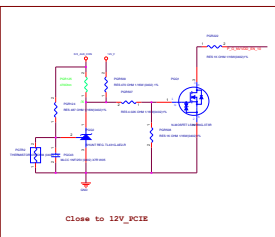


Remove RTD3 Switch Function



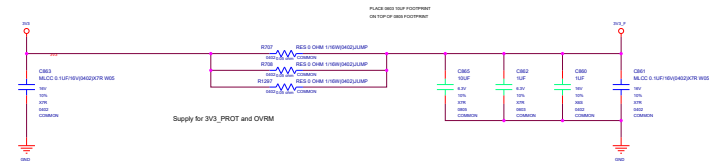
REFER TO PCB FOR BOM STUFFING



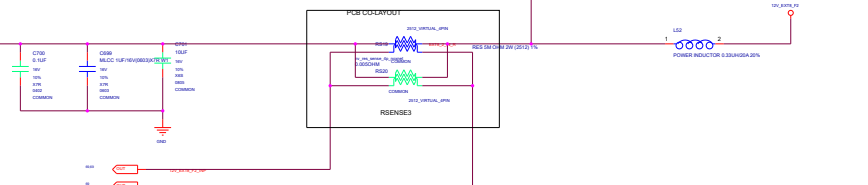
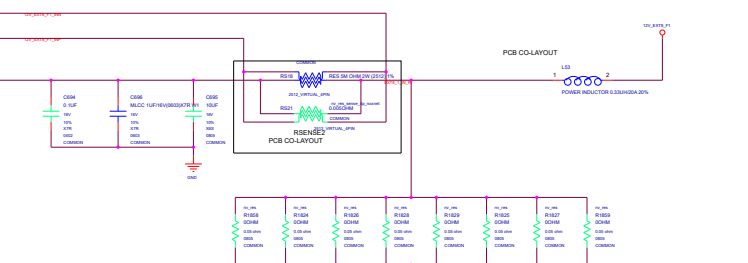
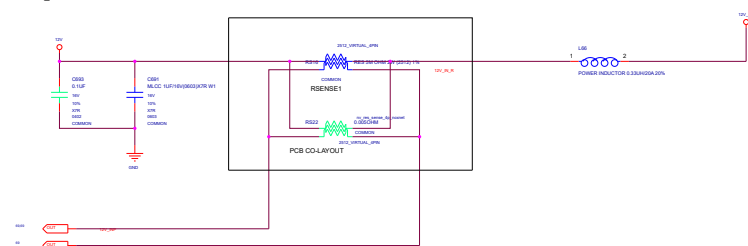


Remove 3V3\_AUX\_VUSE

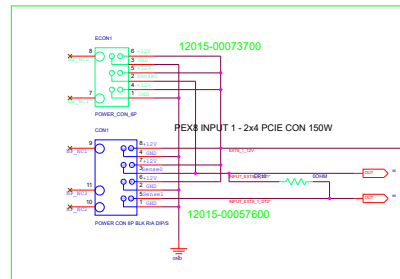
PEX 3V3 INPUT - 10W



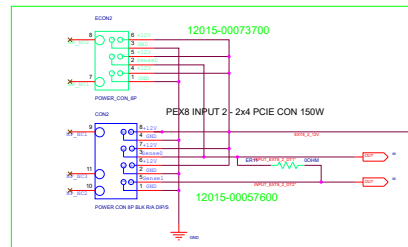
PEX\_12V INPUT - 66W

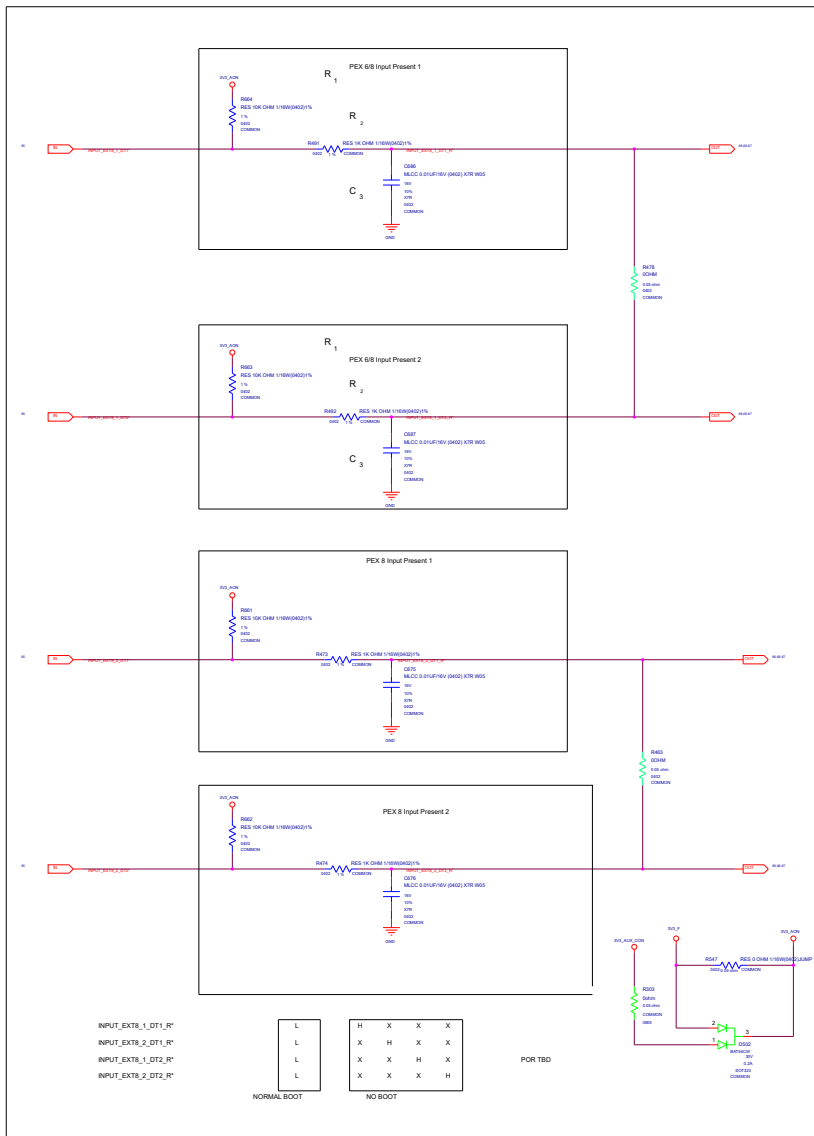


Reverse lock

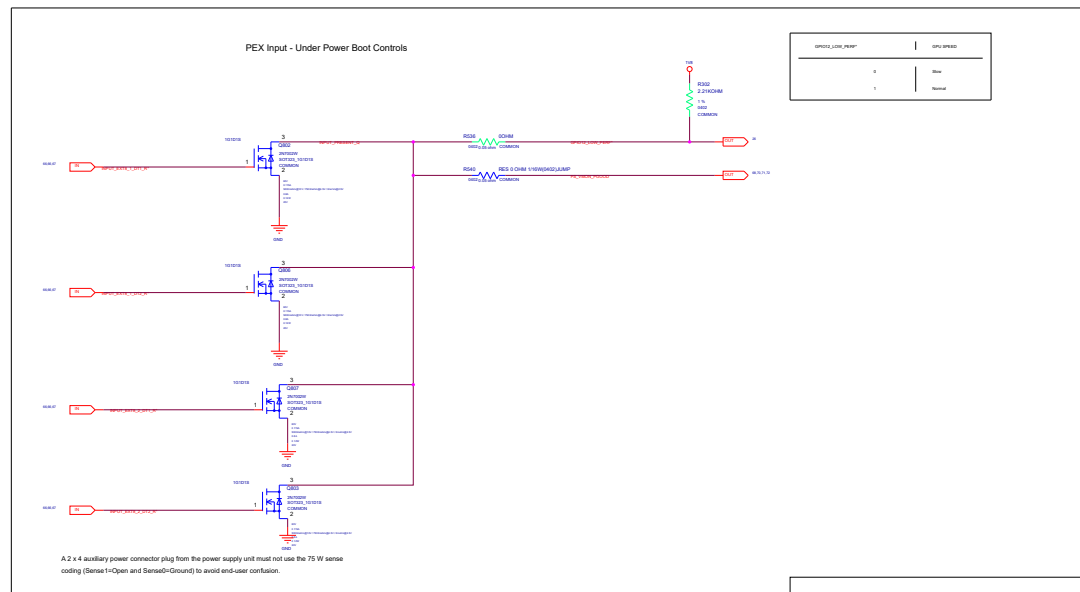


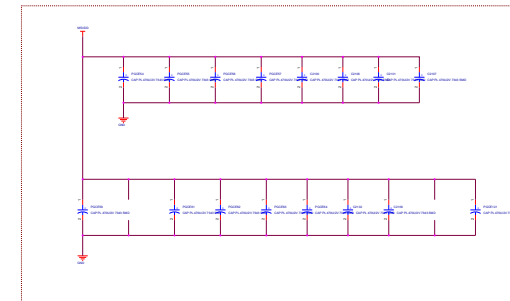
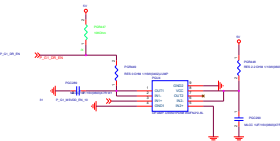
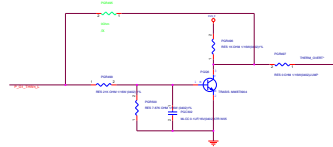
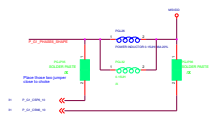
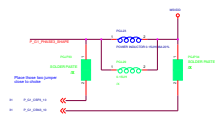
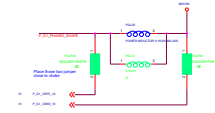
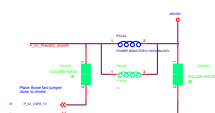
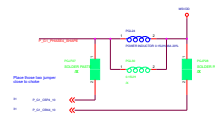
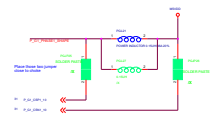
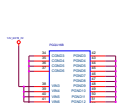
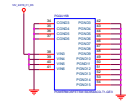
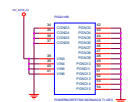
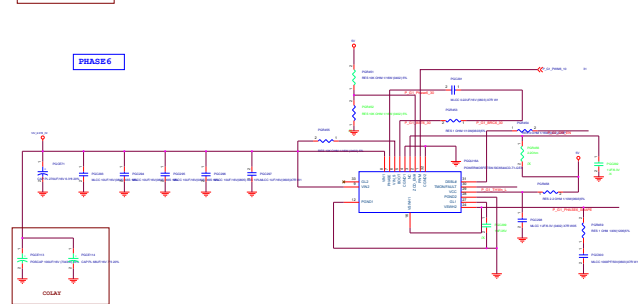
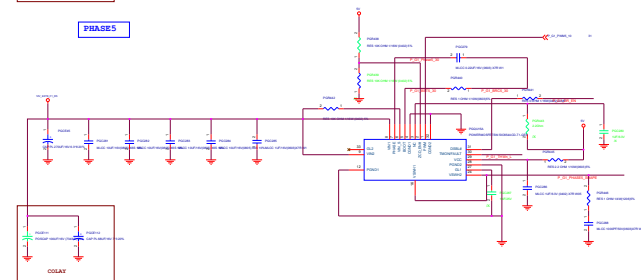
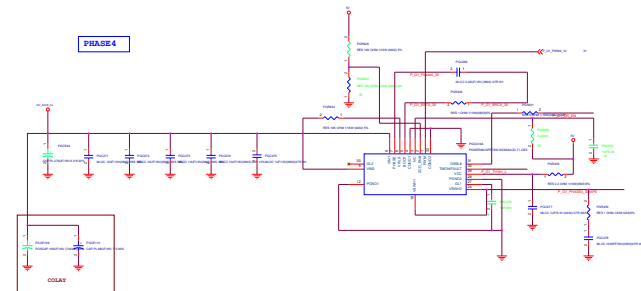
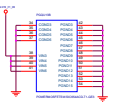
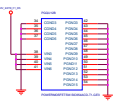
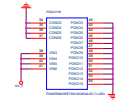
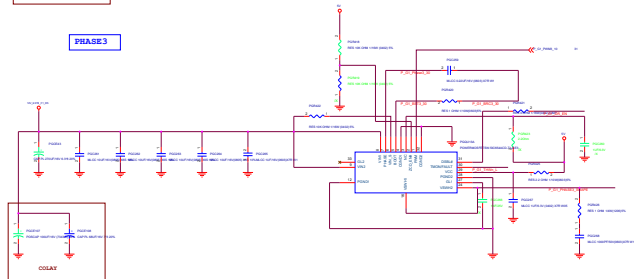
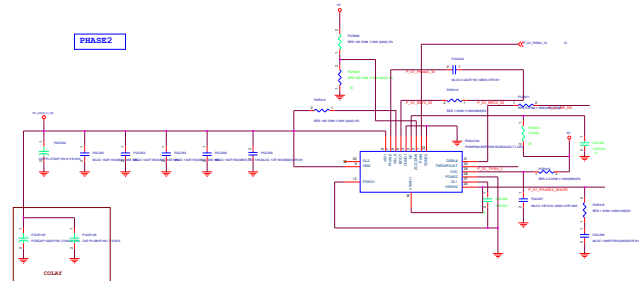
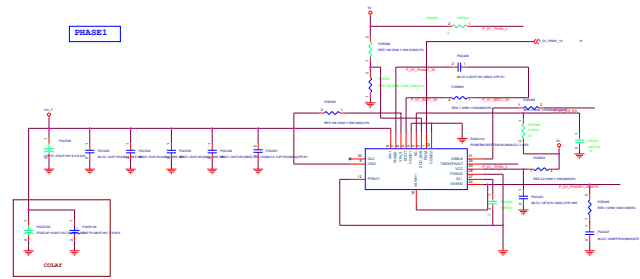
Reverse lock

Remove J24, J25, J26, J27  
MECH\_SPECIAL\_SOLDERING\_PIN\_LARGE-PG160



Remove Hot-Unplug Detect function

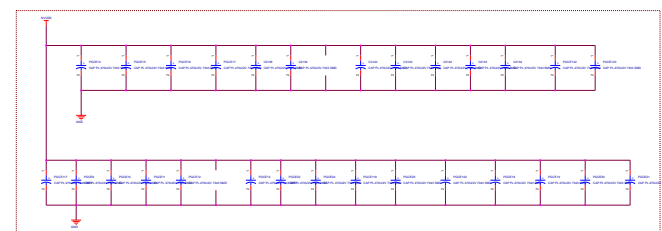
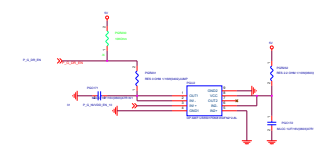
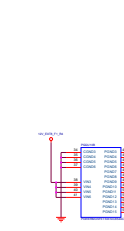
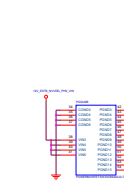
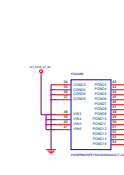
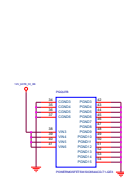
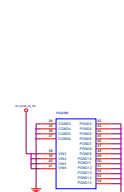
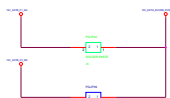
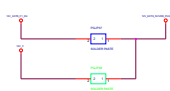
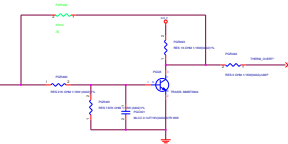
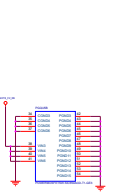
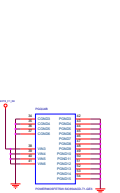
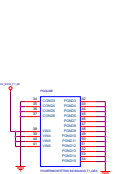
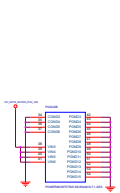
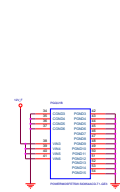




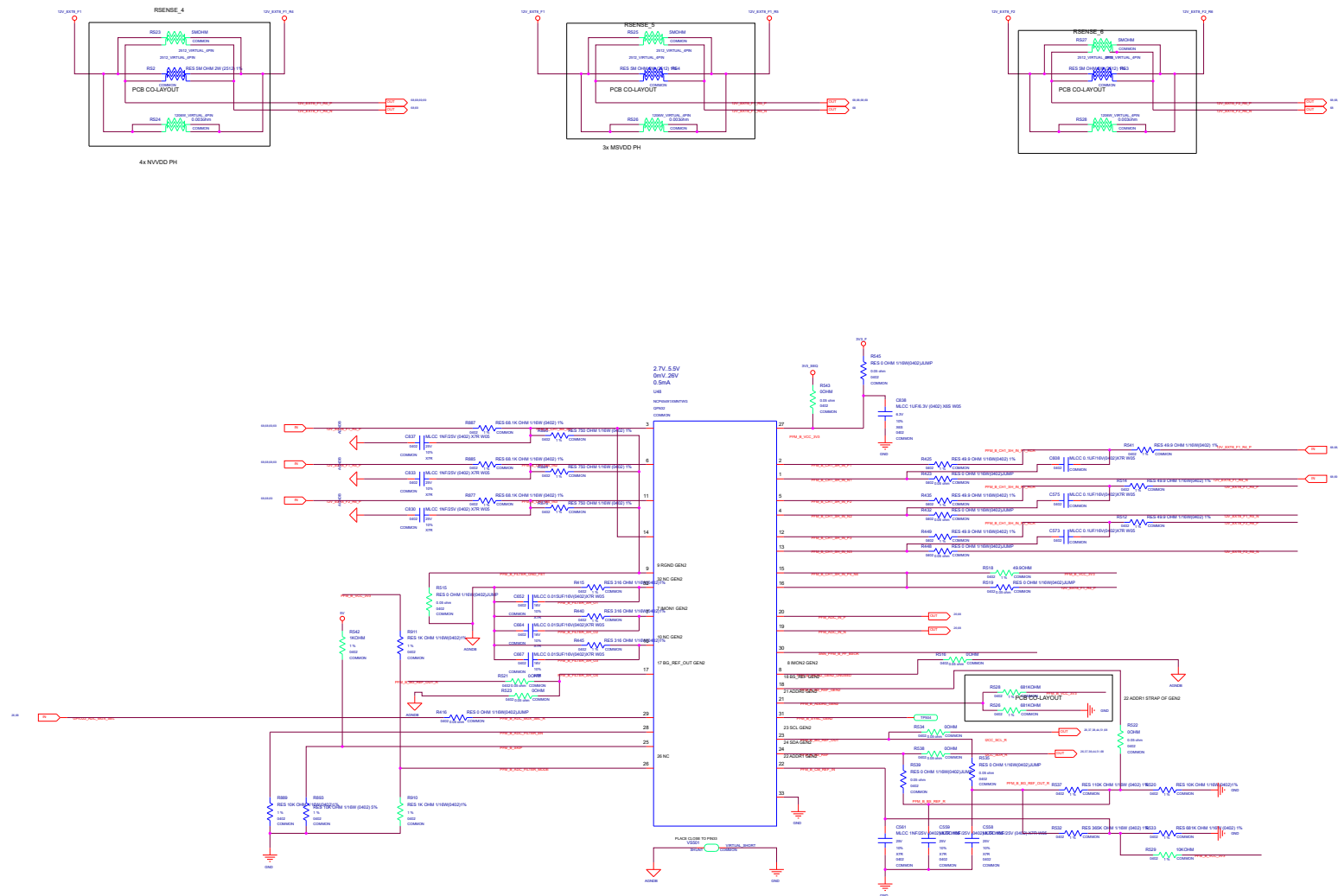
PS: Discrete Steering

Remove PS: Discrete Steering

Title : <b>Steering</b>	
Engineer: <span style="background-color: black; color: black;">XXXXXXXXXX</span>	
<div><div>Drawn</div><div>CG132P</div></div>	<div>Project Name</div> <div>CG132P</div>
<div>Scale</div> <div>1:1000</div>	
<div>Sheet</div> <div>1 of 1</div>	



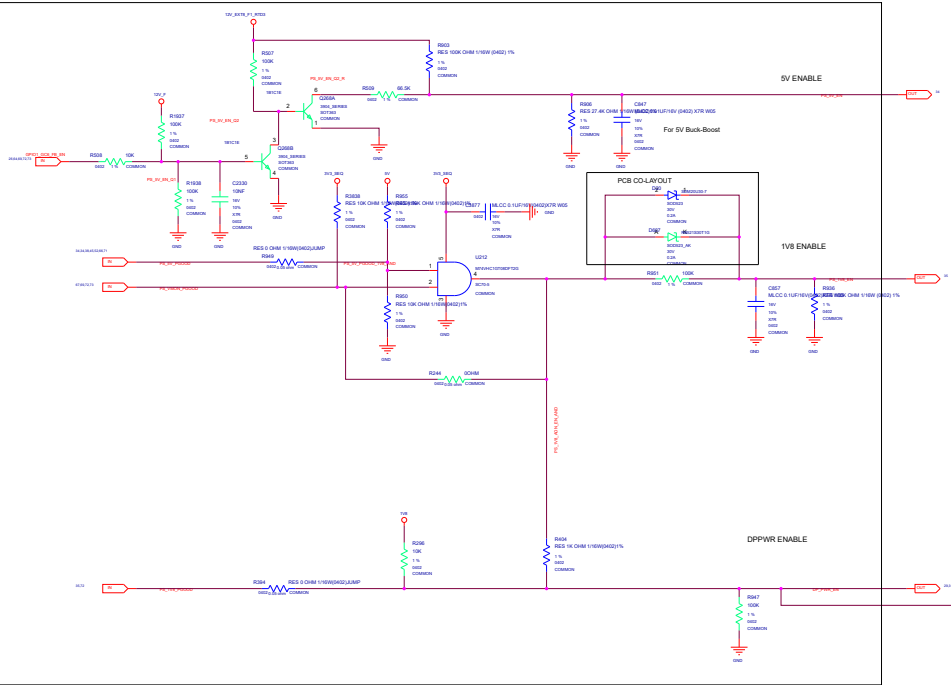
PS: Pre-Filter B

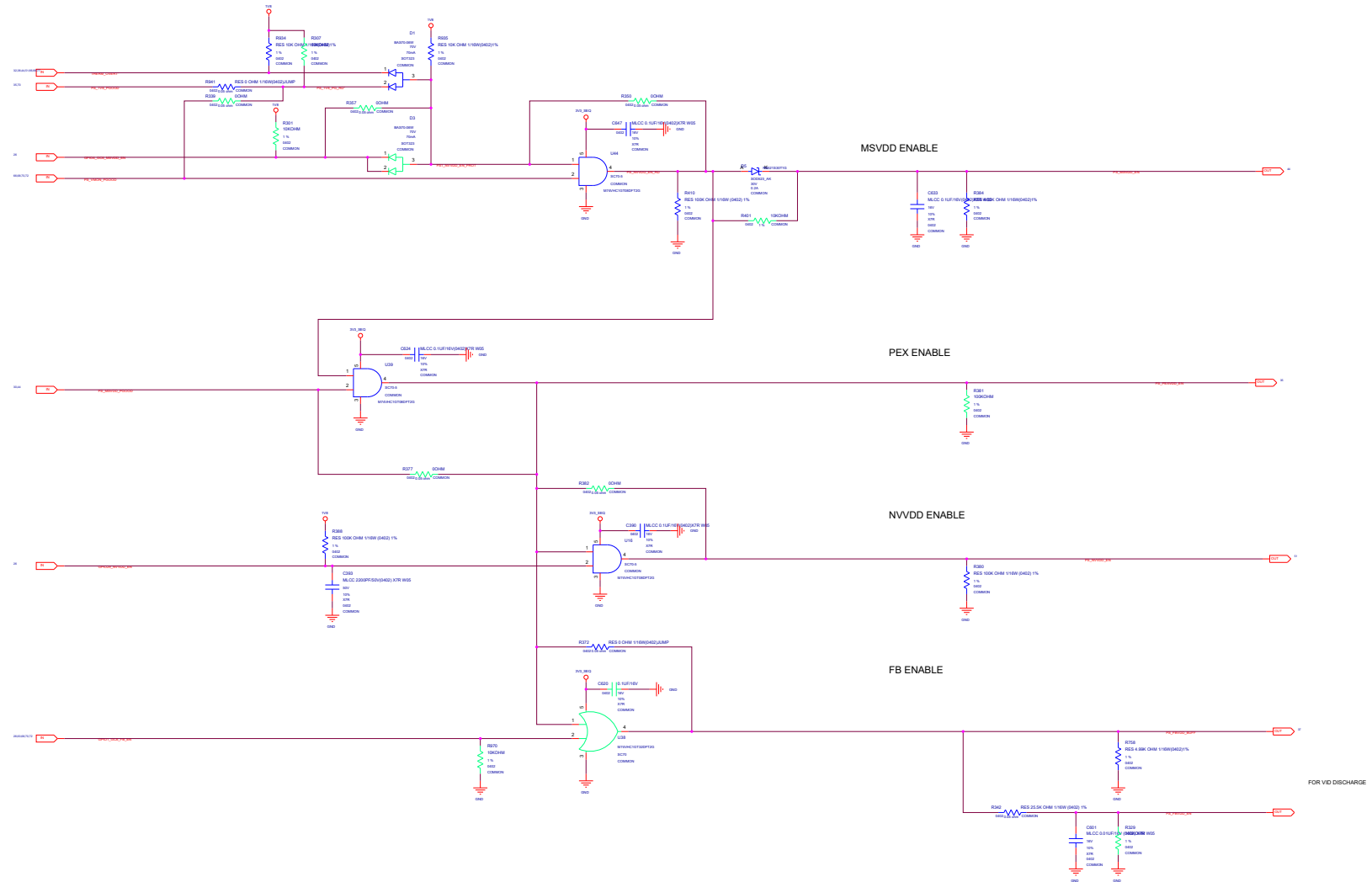


Title :		Pre-Filter B	
Engineer:		[REDACTED]	
Size Custom	Project Name <b>CG132P</b>	Rev 1.01X	
Date: Wednesday, July 15, 2020		Sheet	66 of 66

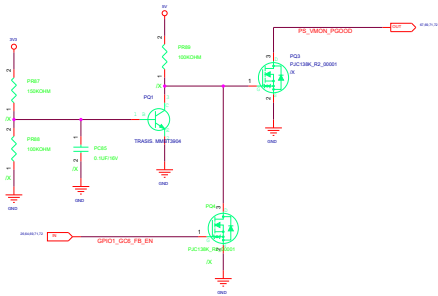


SEQUENCE:5V,1V8,3V3\_SEQ ENABLE





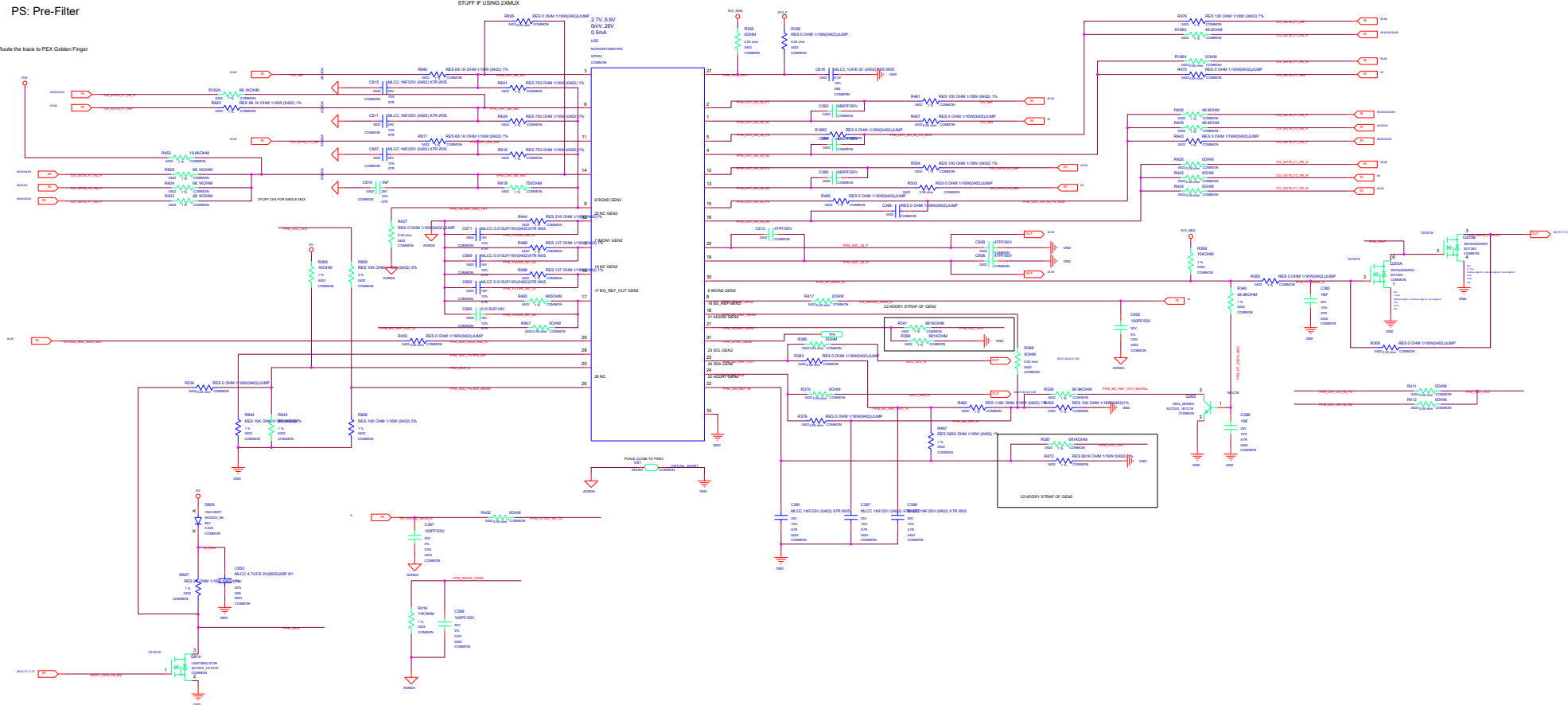
Sequence: 3V3 MONITOR

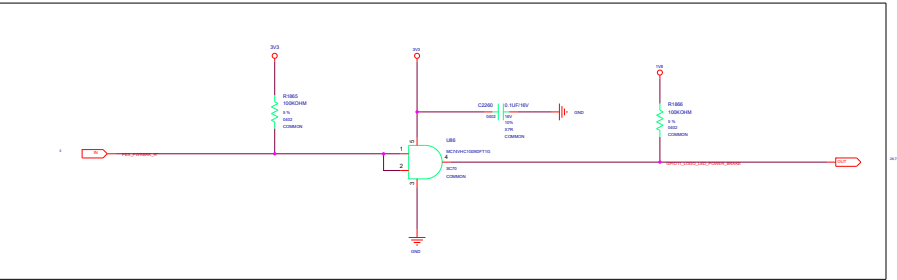
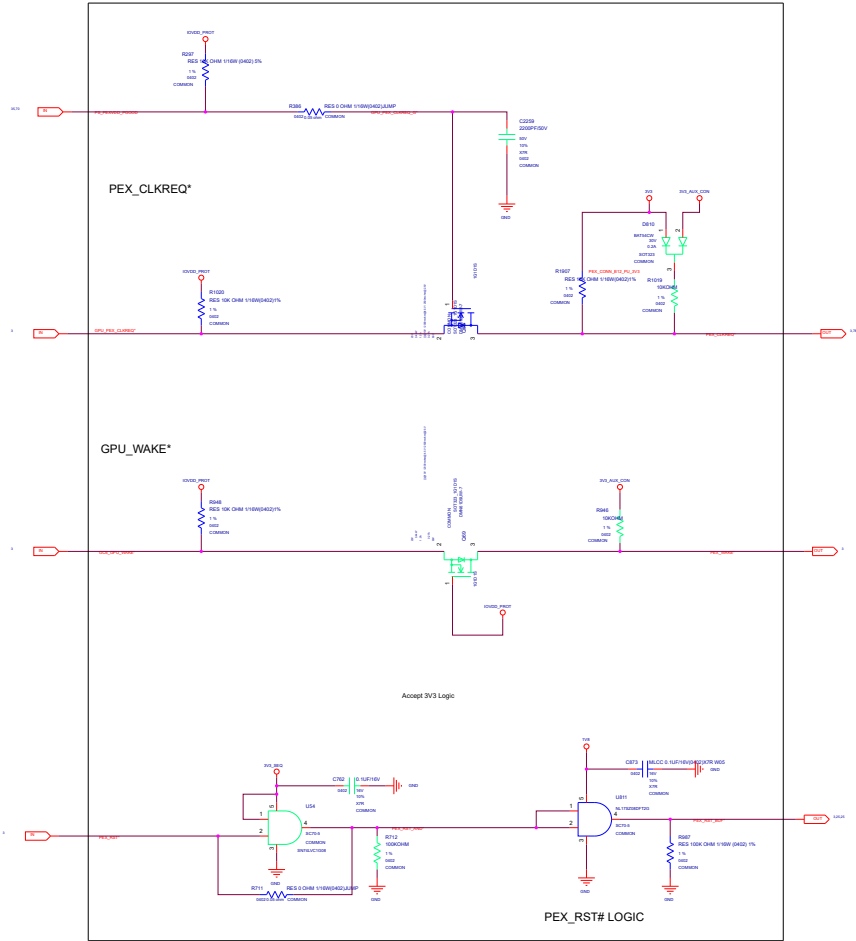


Title : 3V3 MONITOR	
Engineer: [REDACTED]	
<Original>	
Rev	Project Name
A	CG132P
Date: Wednesday, May 18, 2016	
Drawn	By
	10/11

PS: Pre-Filter

Route the trace to PEX Golden Finger



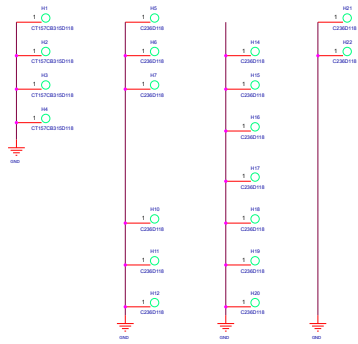


MISC: RGBW LED REF

Remove MISC: RGBW LED REF

Title :		MISC: RGBW LED REF	
Engineer:		[REDACTED]	
<div><div>&lt;Signature&gt;</div><div>Project Name</div></div>			
Date		CG132P	
Created		1.01X	
Date		2024/05/15 10:00	
Print		1/1	

Mechanical: Mounting holes



Title : Mounting holes			
Engineer: [Redacted]			
Size	Project Name	Rev	
CG132P		1.00X	
Date: Wednesday, 2025-10-22 10:20:00		Sheet	16 of 16

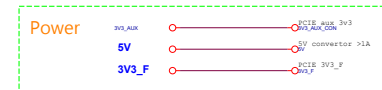
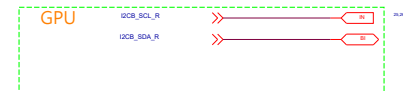
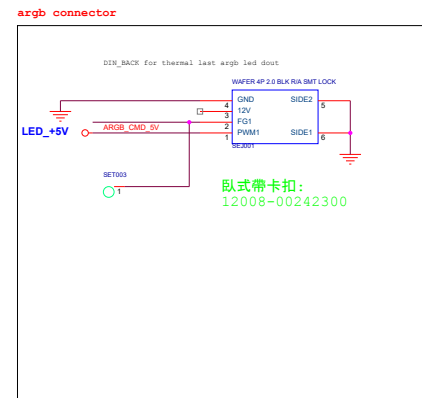
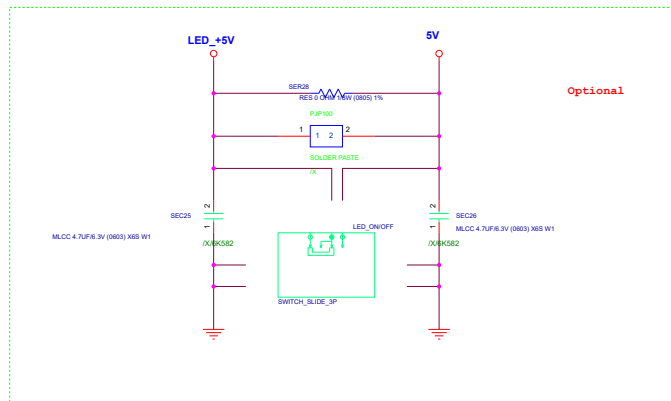
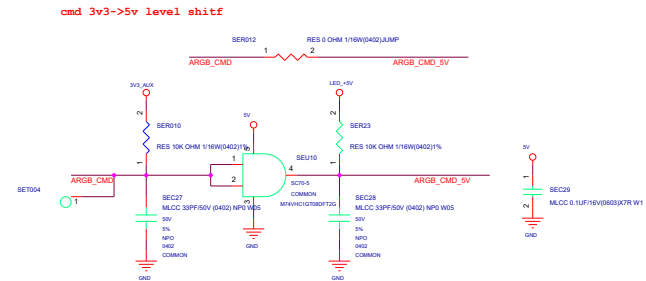
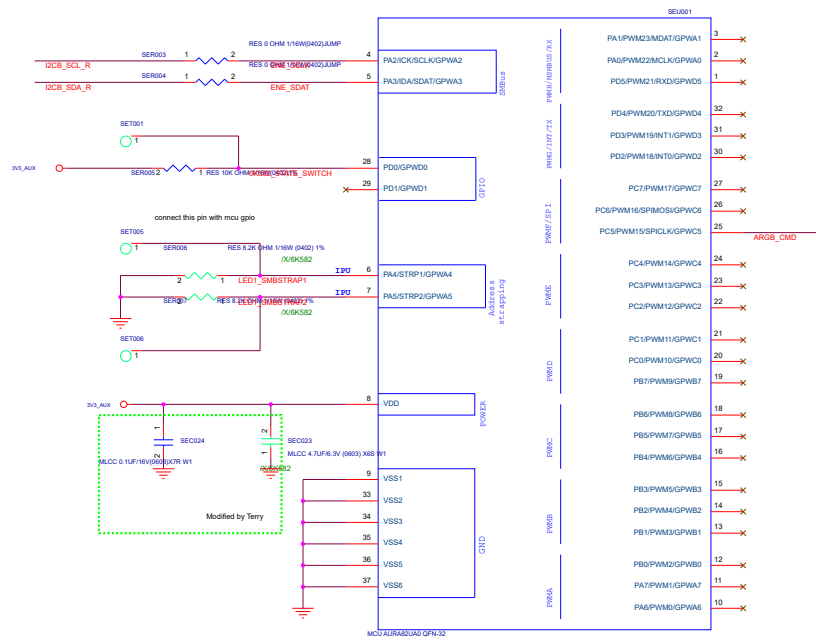
VR THERMAL PROTECTION

Title : VR THERMAL PROTECTION		
Engineer: [REDACTED]		
Scale	Project Name	Rev
CG132P		1.01X
Date: 2023-09-15 10:00:00		



PCI TERM





DEL 2-PIN LED HEADER FUNCTION

Tach1 & 3 switch (第一)

3 FAN 7-PIN HEADERS

立式带卡扣: 12008-00230300

