P1041-B01 GF104

GF104-300, 768MB/1536MB, GDDR5 192b 32M/64Mx32
DVI-I-DL, DVI-I-DL/DP, mHDMI

Table of Contents:

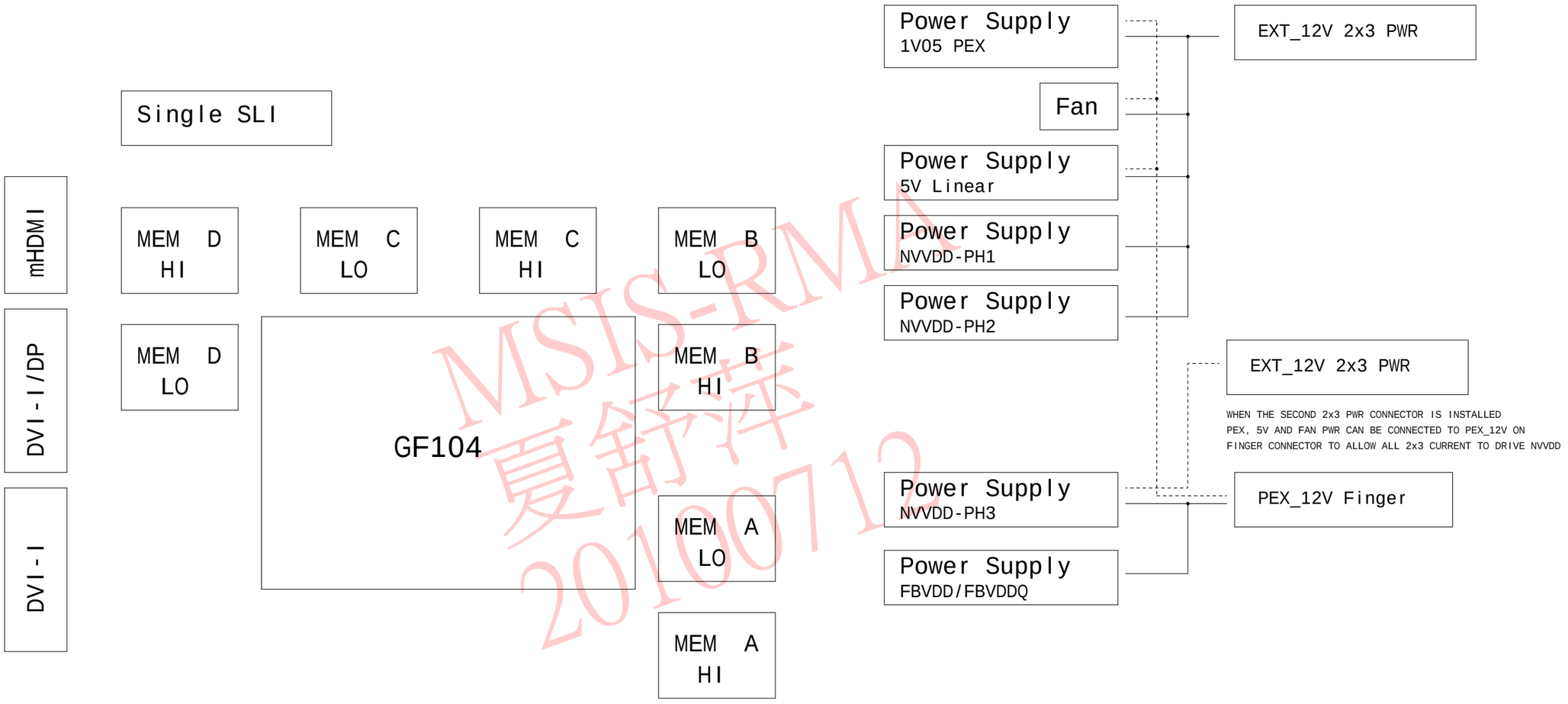
SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11041-BASE-000	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	600-11041-0000-300	P1041 GF104-300 768MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
2	SKU0010	600-11041-0010-300	P1041 GF104-350 1024MB GDDR5 32Mx32 DVI-I+DVI-I+mHDMI Frame Buffer
3	QS1	600-11041-0000-QS1	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	1 OF 34
BOM REV	A	DATE	12-MAY-2010

Page2: Block Diagram



ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	2 OF 34
BOM REV	A	DATE	12-MAY-2010

Page3: PCI Express

PEX NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR		
PEX_REFCLK	1	90DIFF	PEX_REFCLK	OUT	
PEX_REFCLK*	1	90DIFF	PEX_REFCLK	OUT	
PEX_TXX0	1	90DIFF	PEX_TXX0	OUT	
PEX_TXX0*	1	90DIFF	PEX_TXX0	OUT	
PEX_TXX1	1	90DIFF	PEX_TXX1	OUT	
PEX_TXX1*	1	90DIFF	PEX_TXX1	OUT	
PEX_TXX2	1	90DIFF	PEX_TXX2	OUT	
PEX_TXX2*	1	90DIFF	PEX_TXX2	OUT	
PEX_TXX3	1	90DIFF	PEX_TXX3	OUT	
PEX_TXX3*	1	90DIFF	PEX_TXX3	OUT	
PEX_TXX4	1	90DIFF	PEX_TXX4	OUT	
PEX_TXX4*	1	90DIFF	PEX_TXX4	OUT	
PEX_TXX5	1	90DIFF	PEX_TXX5	OUT	
PEX_TXX5*	1	90DIFF	PEX_TXX5	OUT	
PEX_TXX6	1	90DIFF	PEX_TXX6	OUT	
PEX_TXX6*	1	90DIFF	PEX_TXX6	OUT	
PEX_TXX7	1	90DIFF	PEX_TXX7	OUT	
PEX_TXX7*	1	90DIFF	PEX_TXX7	OUT	
PEX_TXX8	1	90DIFF	PEX_TXX8	OUT	
PEX_TXX8*	1	90DIFF	PEX_TXX8	OUT	
PEX_TXX9	1	90DIFF	PEX_TXX9	OUT	
PEX_TXX9*	1	90DIFF	PEX_TXX9	OUT	
PEX_TXX10	1	90DIFF	PEX_TXX10	OUT	
PEX_TXX10*	1	90DIFF	PEX_TXX10	OUT	
PEX_TXX11	1	90DIFF	PEX_TXX11	OUT	
PEX_TXX11*	1	90DIFF	PEX_TXX11	OUT	
PEX_TXX12	1	90DIFF	PEX_TXX12	OUT	
PEX_TXX12*	1	90DIFF	PEX_TXX12	OUT	
PEX_TXX13	1	90DIFF	PEX_TXX13	OUT	
PEX_TXX13*	1	90DIFF	PEX_TXX13	OUT	
PEX_TXX14	1	90DIFF	PEX_TXX14	OUT	
PEX_TXX14*	1	90DIFF	PEX_TXX14	OUT	
PEX_TXX15	1	90DIFF	PEX_TXX15	OUT	
PEX_TXX15*	1	90DIFF	PEX_TXX15	OUT	
PEX_RX0	1	90DIFF	PEX_RX0	OUT	
PEX_RX0*	1	90DIFF	PEX_RX0	OUT	
PEX_RX1	1	90DIFF	PEX_RX1	OUT	
PEX_RX1*	1	90DIFF	PEX_RX1	OUT	
PEX_RX2	1	90DIFF	PEX_RX2	OUT	
PEX_RX2*	1	90DIFF	PEX_RX2	OUT	
PEX_RX3	1	90DIFF	PEX_RX3	OUT	
PEX_RX3*	1	90DIFF	PEX_RX3	OUT	
PEX_RX4	1	90DIFF	PEX_RX4	OUT	
PEX_RX4*	1	90DIFF	PEX_RX4	OUT	
PEX_RX5	1	90DIFF	PEX_RX5	OUT	
PEX_RX5*	1	90DIFF	PEX_RX5	OUT	
PEX_RX6	1	90DIFF	PEX_RX6	OUT	
PEX_RX6*	1	90DIFF	PEX_RX6	OUT	
PEX_RX7	1	90DIFF	PEX_RX7	OUT	
PEX_RX7*	1	90DIFF	PEX_RX7	OUT	
PEX_RX8	1	90DIFF	PEX_RX8	OUT	
PEX_RX8*	1	90DIFF	PEX_RX8	OUT	
PEX_RX9	1	90DIFF	PEX_RX9	OUT	
PEX_RX9*	1	90DIFF	PEX_RX9	OUT	
PEX_RX10	1	90DIFF	PEX_RX10	OUT	
PEX_RX10*	1	90DIFF	PEX_RX10	OUT	
PEX_RX11	1	90DIFF	PEX_RX11	OUT	
PEX_RX11*	1	90DIFF	PEX_RX11	OUT	
PEX_RX12	1	90DIFF	PEX_RX12	OUT	
PEX_RX12*	1	90DIFF	PEX_RX12	OUT	
PEX_RX13	1	90DIFF	PEX_RX13	OUT	
PEX_RX13*	1	90DIFF	PEX_RX13	OUT	
PEX_RX14	1	90DIFF	PEX_RX14	OUT	
PEX_RX14*	1	90DIFF	PEX_RX14	OUT	
PEX_RX15	1	90DIFF	PEX_RX15	OUT	
PEX_RX15*	1	90DIFF	PEX_RX15	OUT	
PEX_TX0	1	90DIFF	PEX_TX0	OUT	
PEX_TX0*	1	90DIFF	PEX_TX0	OUT	
PEX_TX1	1	90DIFF	PEX_TX1	OUT	
PEX_TX1*	1	90DIFF	PEX_TX1	OUT	
PEX_TX2	1	90DIFF	PEX_TX2	OUT	
PEX_TX2*	1	90DIFF	PEX_TX2	OUT	
PEX_TX3	1	90DIFF	PEX_TX3	OUT	
PEX_TX3*	1	90DIFF	PEX_TX3	OUT	
PEX_TX4	1	90DIFF	PEX_TX4	OUT	
PEX_TX4*	1	90DIFF	PEX_TX4	OUT	
PEX_TX5	1	90DIFF	PEX_TX5	OUT	
PEX_TX5*	1	90DIFF	PEX_TX5	OUT	
PEX_TX6	1	90DIFF	PEX_TX6	OUT	
PEX_TX6*	1	90DIFF	PEX_TX6	OUT	
PEX_TX7	1	90DIFF	PEX_TX7	OUT	
PEX_TX7*	1	90DIFF	PEX_TX7	OUT	
PEX_TX8	1	90DIFF	PEX_TX8	OUT	
PEX_TX8*	1	90DIFF	PEX_TX8	OUT	
PEX_TX9	1	90DIFF	PEX_TX9	OUT	
PEX_TX9*	1	90DIFF	PEX_TX9	OUT	
PEX_TX10	1	90DIFF	PEX_TX10	OUT	
PEX_TX10*	1	90DIFF	PEX_TX10	OUT	
PEX_TX11	1	90DIFF	PEX_TX11	OUT	
PEX_TX11*	1	90DIFF	PEX_TX11	OUT	
PEX_TX12	1	90DIFF	PEX_TX12	OUT	
PEX_TX12*	1	90DIFF	PEX_TX12	OUT	
PEX_TX13	1	90DIFF	PEX_TX13	OUT	
PEX_TX13*	1	90DIFF	PEX_TX13	OUT	
PEX_TX14	1	90DIFF	PEX_TX14	OUT	
PEX_TX14*	1	90DIFF	PEX_TX14	OUT	
PEX_TX15	1	90DIFF	PEX_TX15	OUT	
PEX_TX15*	1	90DIFF	PEX_TX15	OUT	
PEX_PLL_CLK_OUT	1	90DIFF	PEX_PLL_CLK_OUT	OUT	
PEX_PLL_CLK_OUT*	1	90DIFF	PEX_PLL_CLK_OUT	OUT	
PEX_RST*	1	50OHM		OUT	3> 32<
PRSNT*				OUT	
PEX_TRST*				OUT	
PEX_TCLK				OUT	
PEX_TDI				OUT	
PEX_TDO				OUT	
PEX_TMS				OUT	
JTAG_TCLK				OUT	3< 25>
JTAG_TMS				OUT	3< 25>
JTAG_TDI				OUT	3< 25>
JTAG_TDO				OUT	3> 25<
JTAG_TRST*				OUT	3< 25>

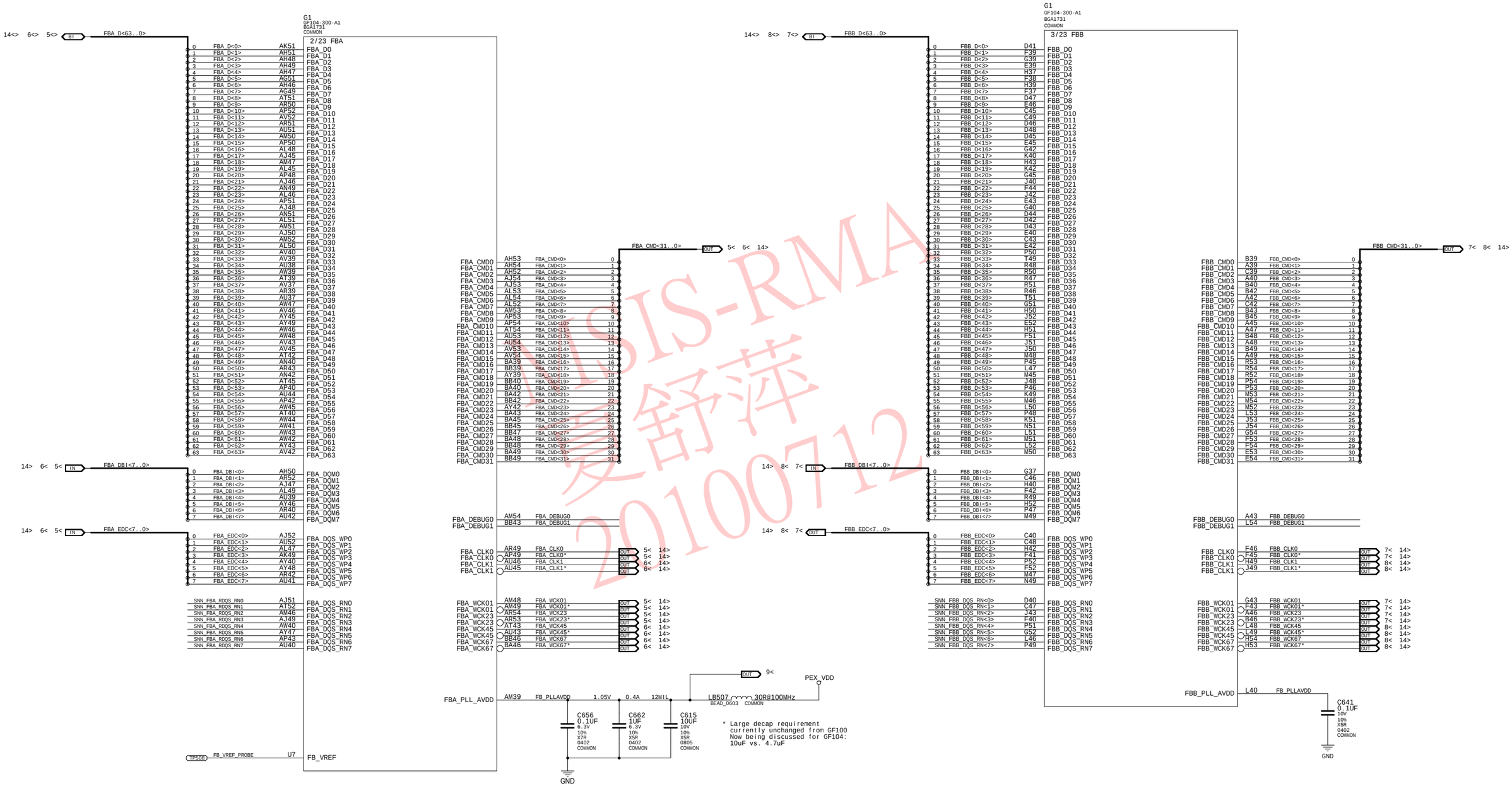
	NET		VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	NV_SOURCE_POWER_NET	12V	5.5A	24MIL
3V3	3V3	NV_SOURCE_POWER_NET	3.3V	3.0A	20MIL
GND	GND	NV_SOURCE_POWER_NET	0V	8.5A	16MIL
IN	PEX_PLLVDD		1.05V	0.16A	12MIL

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	3 OF 34
BOM REV	A	DATE	12-MAY-2010

Page4: GPU Partition A/B



ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

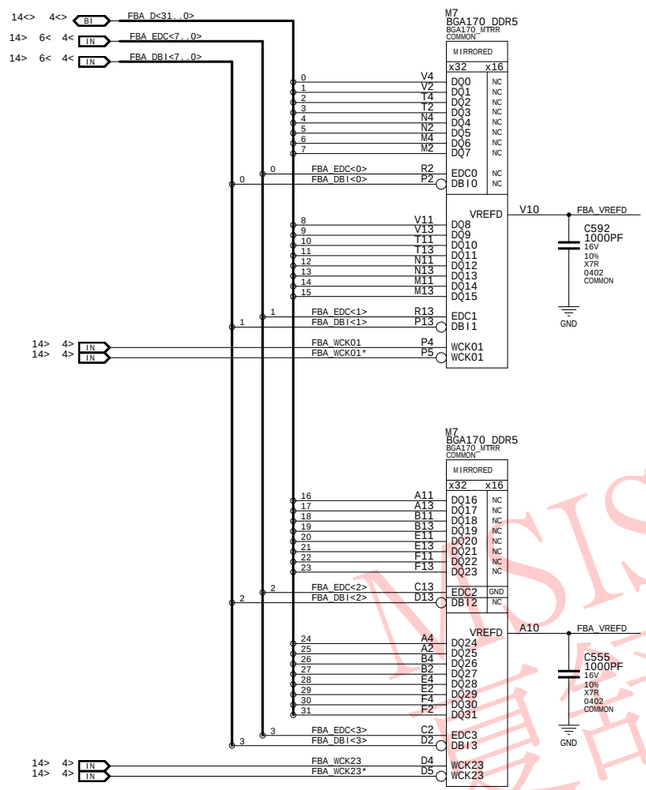
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

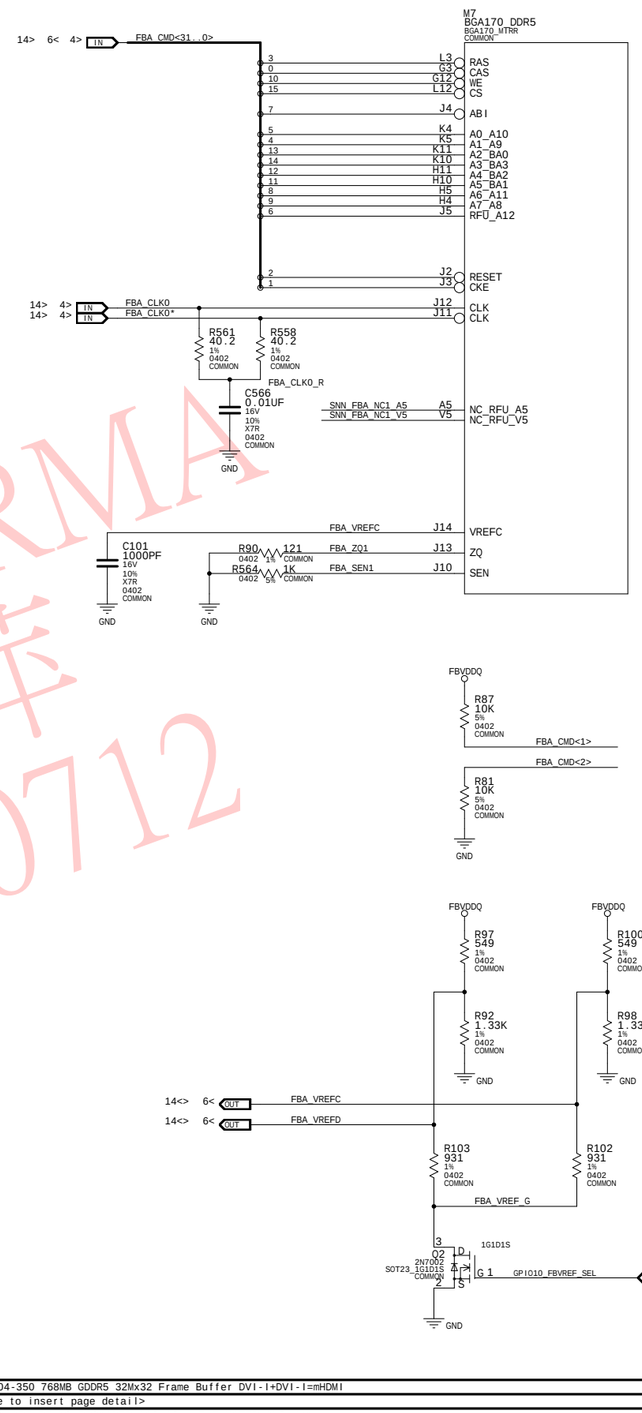
NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	4 OF 34
BOM REV	A	DATE	12-MAY-2010

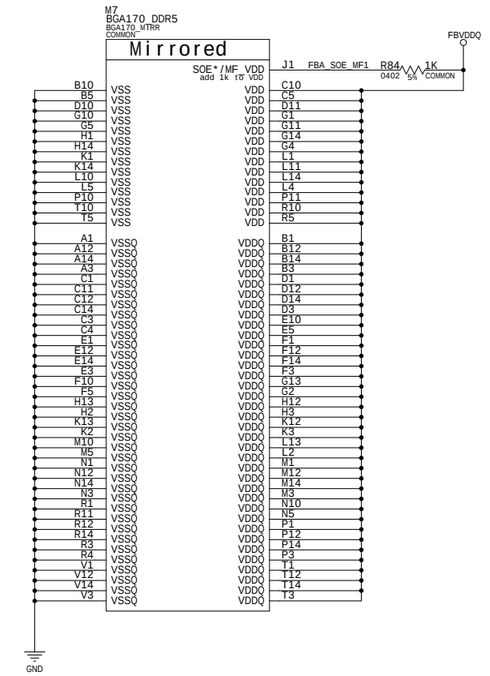
Page5: FBA Partition 31..0

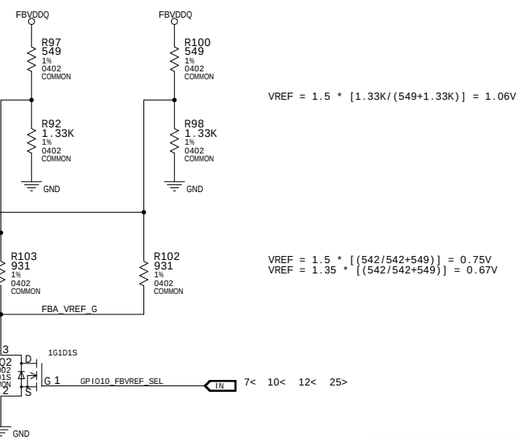
GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

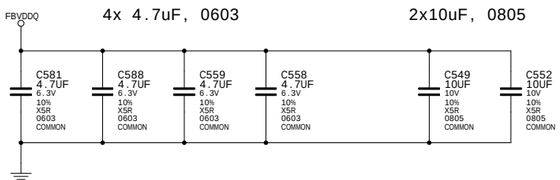
** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update

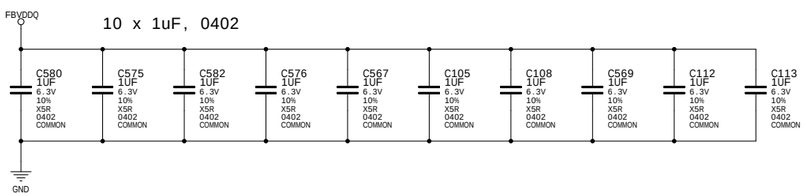












ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

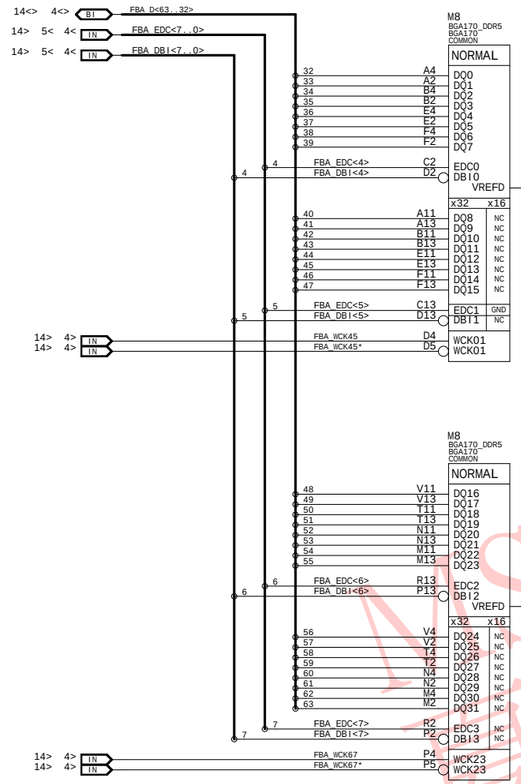
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

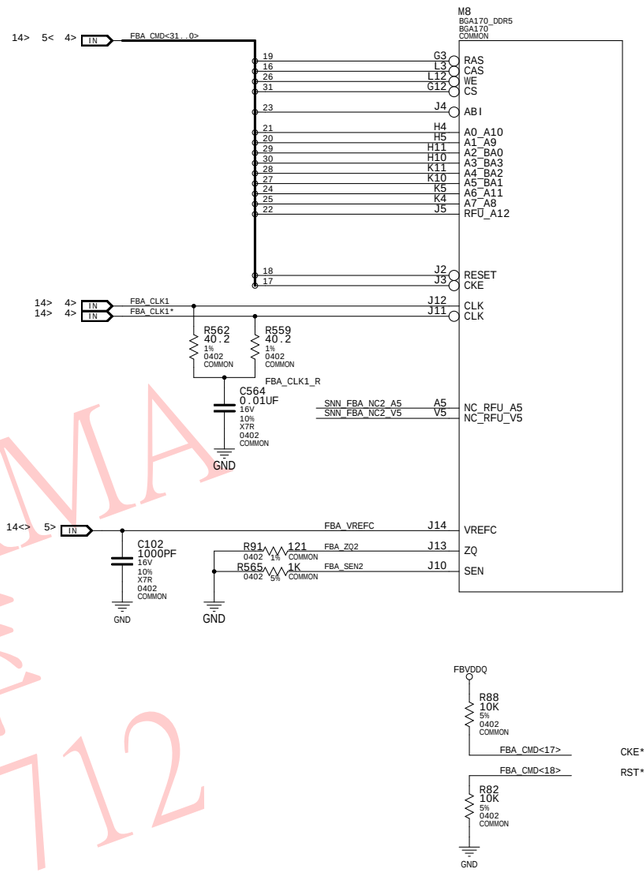
NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	5 OF 34
BOM REV	A	DATE	12-MAY-2010

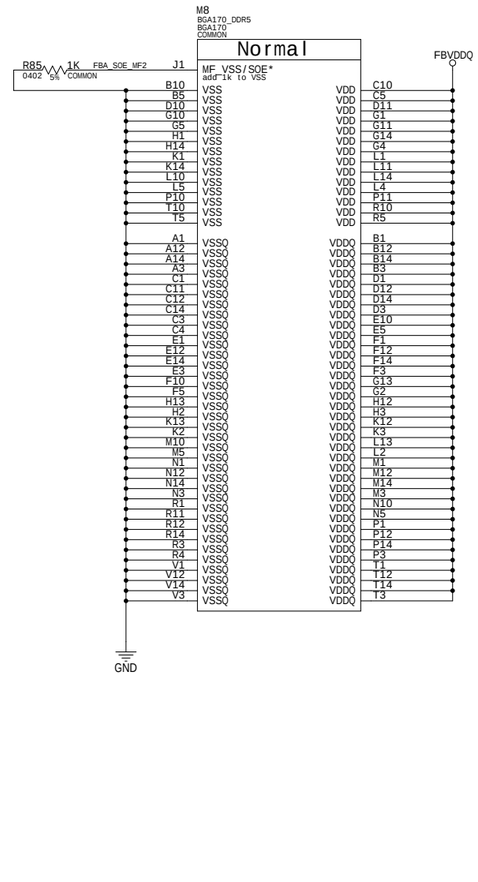
Page6: FBA Partition 63..32

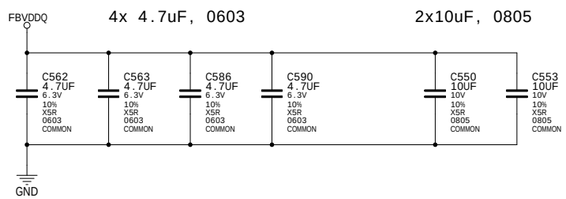
GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

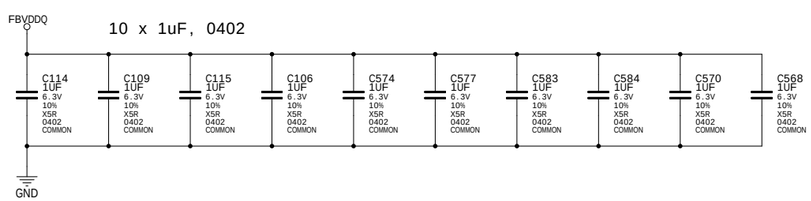
** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update











ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

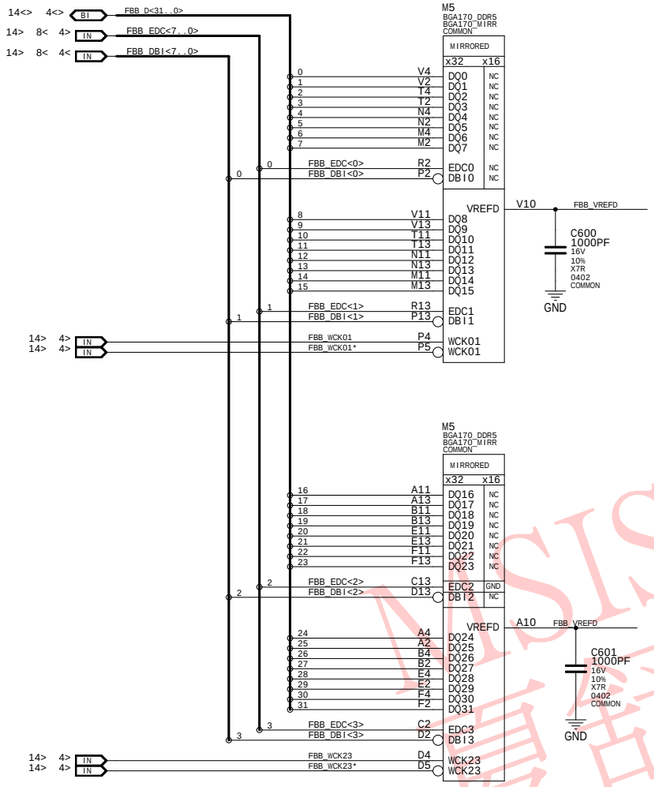
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

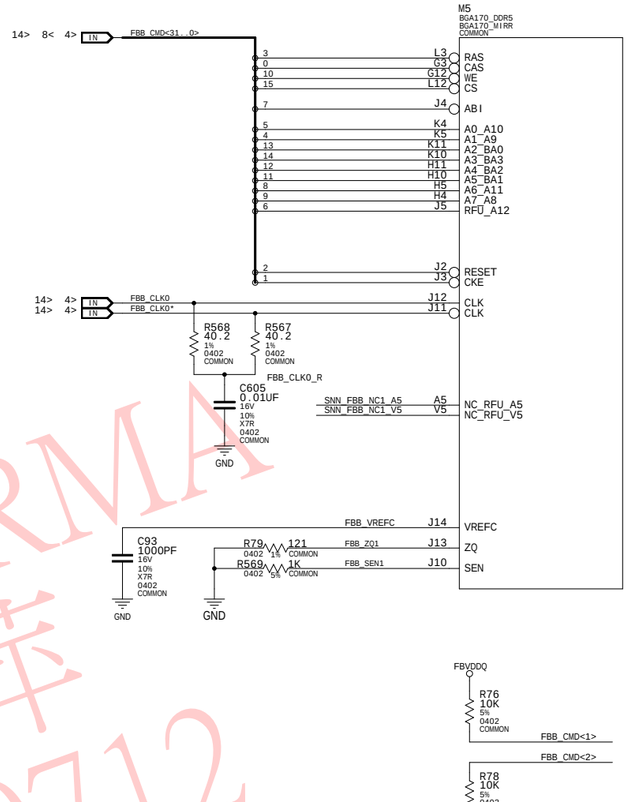
NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	6 OF 34
BOM REV	A	DATE	12-MAY-2010

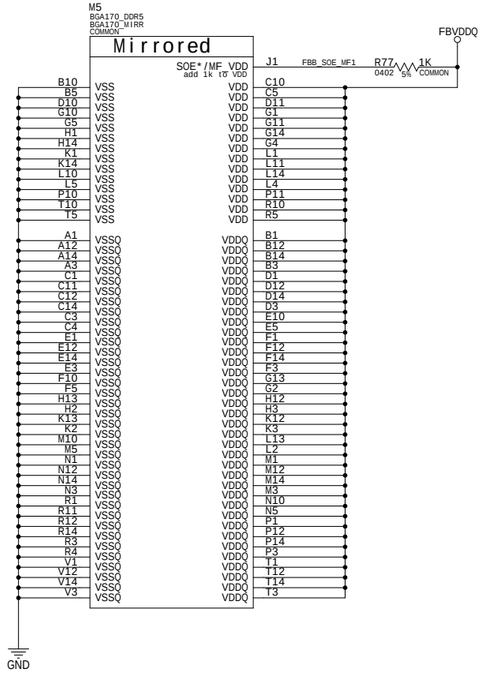
Page7: FBB Partition 31..0

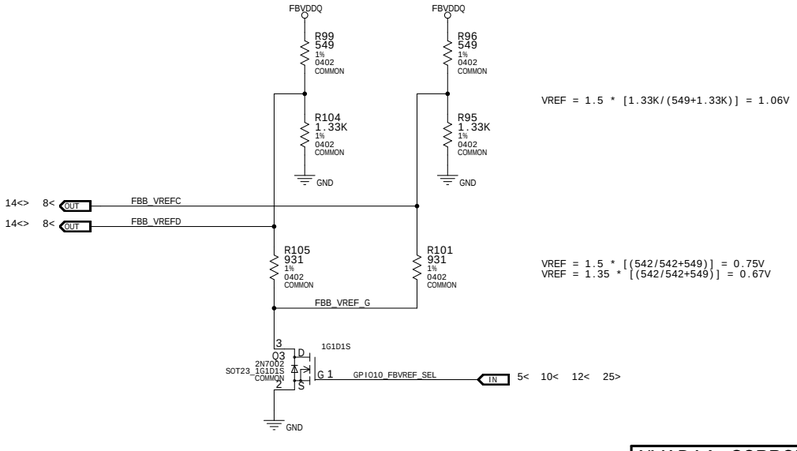
GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CA5*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CA5*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

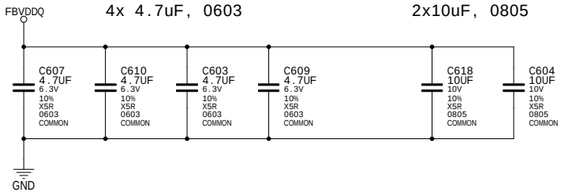
** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update

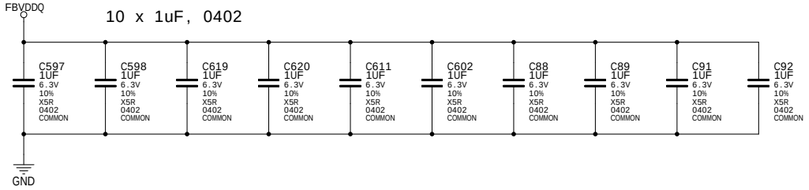












ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

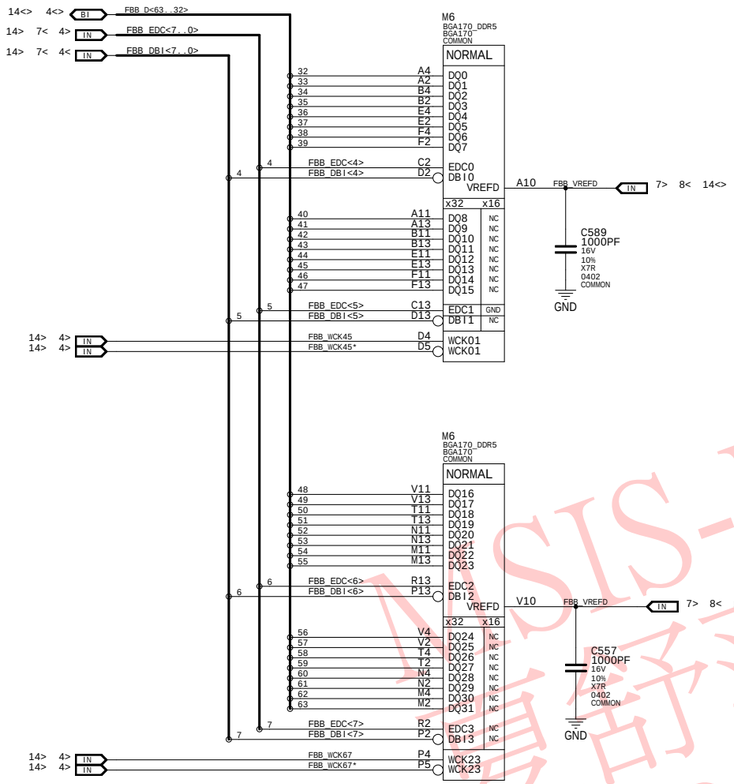
NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	7 OF 34
BOM REV	A	DATE	12-MAY-2010

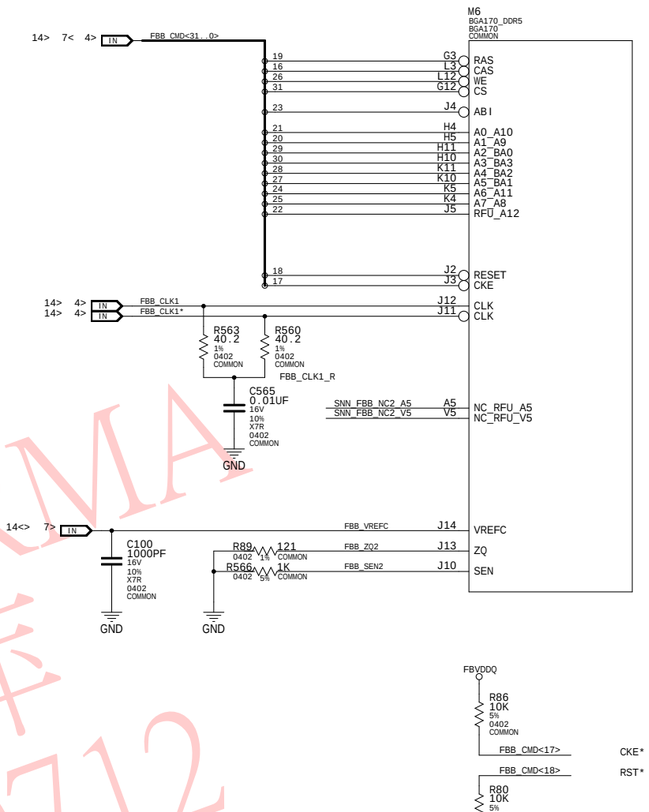
Page8: FBB Partition 63..32

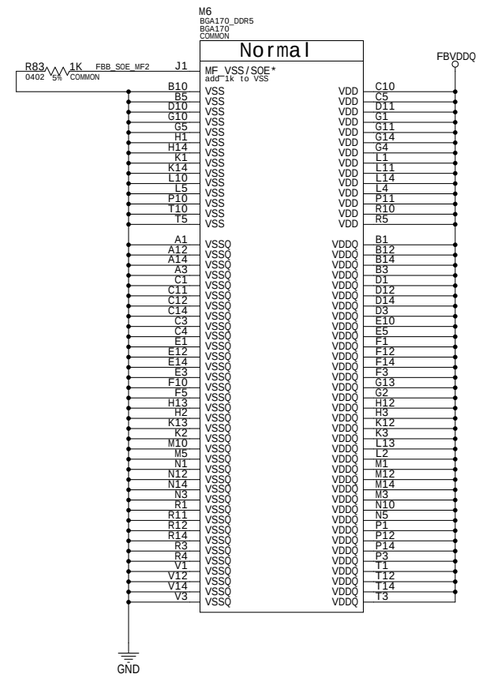
GDDR5 CMD Mapping

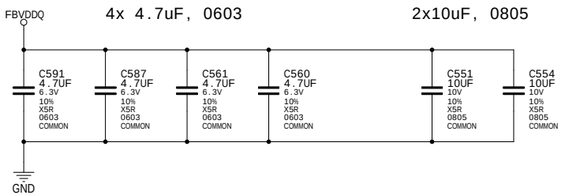
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

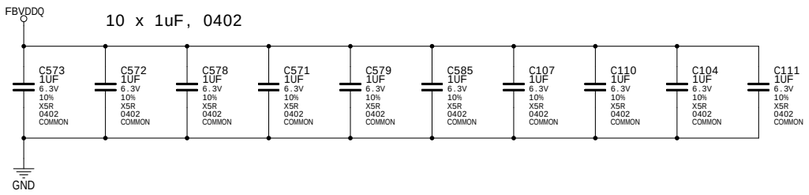
** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update











ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	8 OF 34
BOM REV	A	DATE	12-MAY-2010

Page9: GPU Partition C/D

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

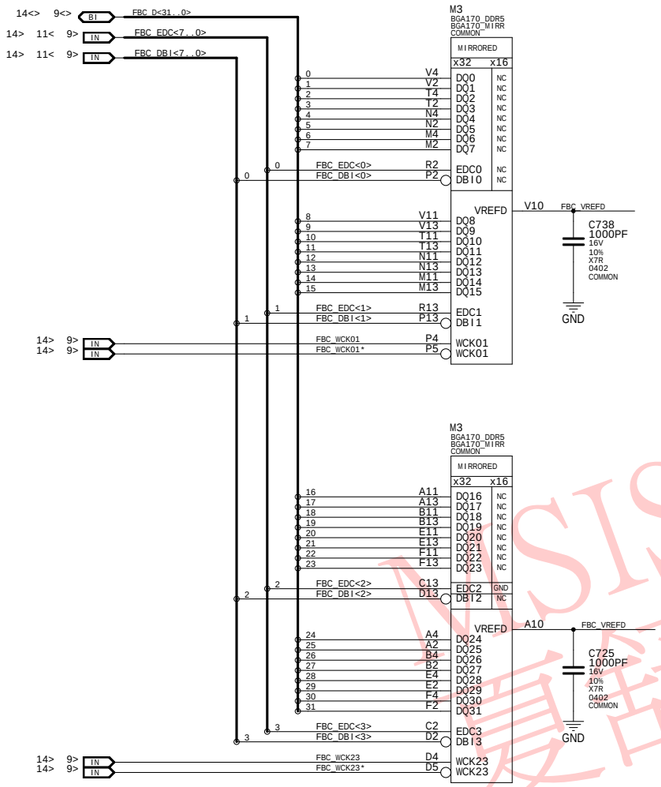
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

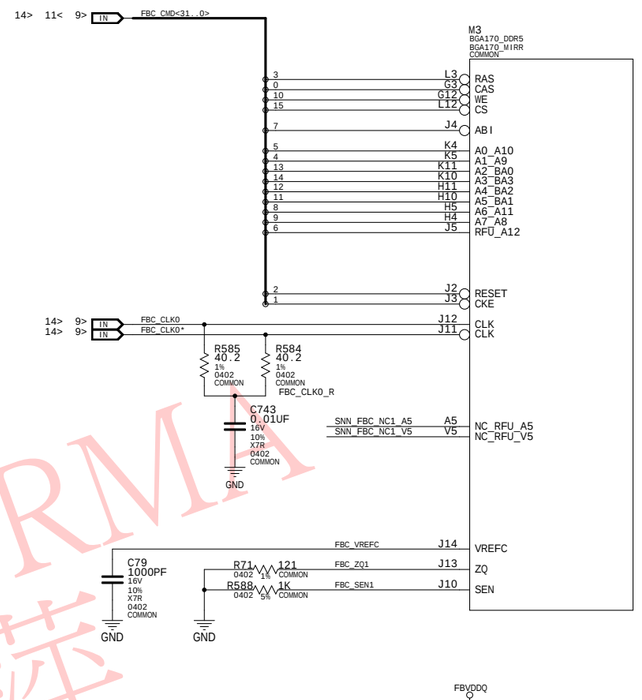
NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	9 OF 34
BOM REV	A	DATE	12-MAY-2010

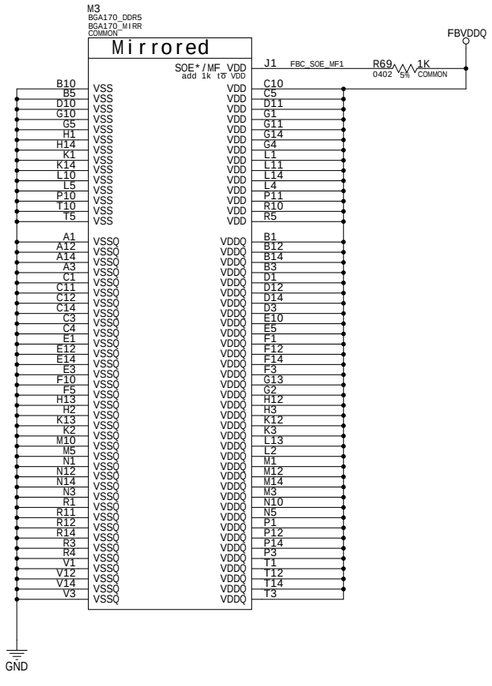
Page10: FBC Partition 31..0

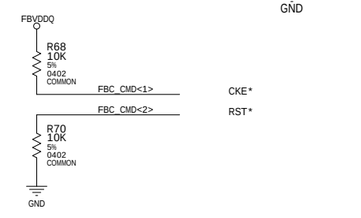
GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

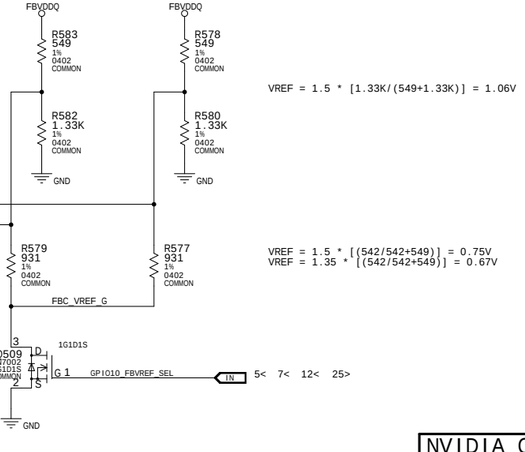
** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update

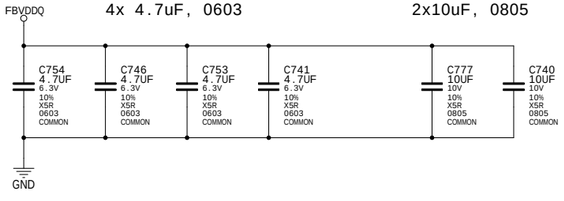


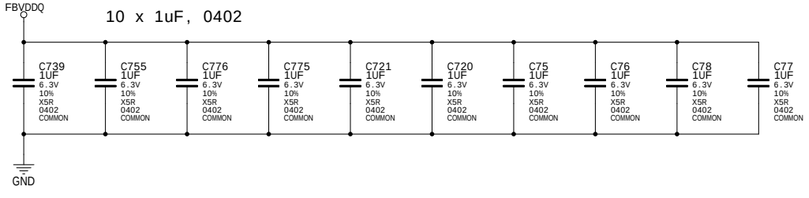












ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

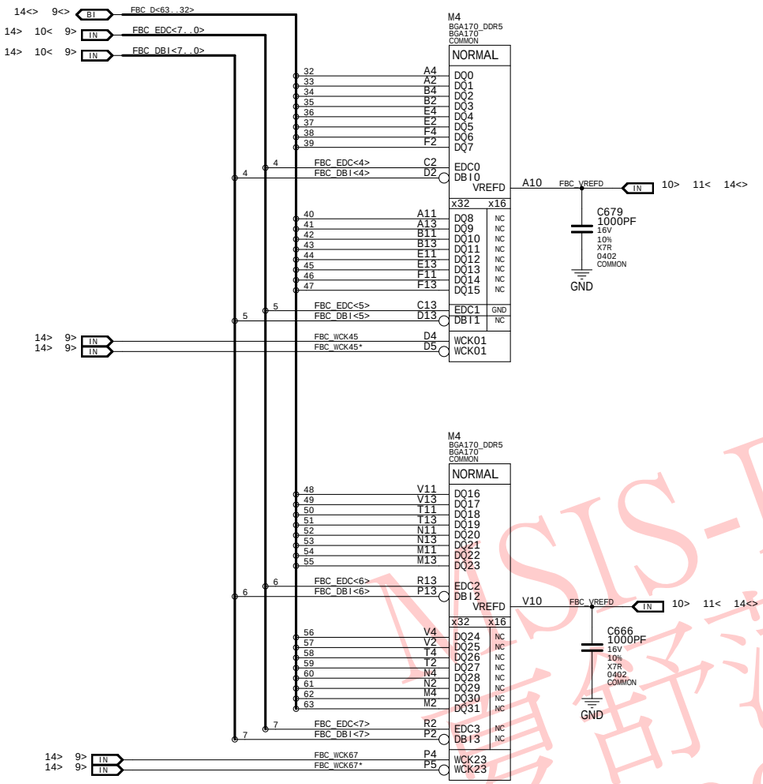
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

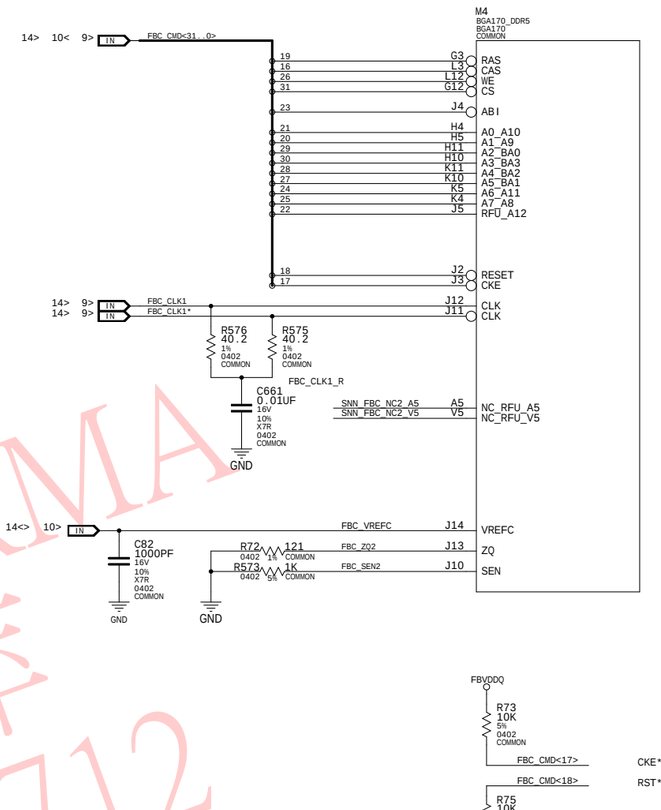
NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	10 OF 34
BOM REV	A	DATE	12-MAY-2010

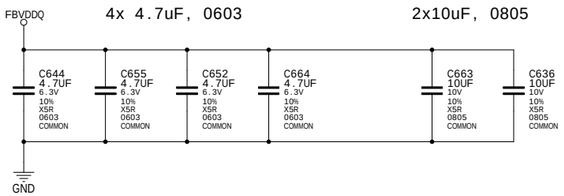
Page11: FBC Partition 63..32

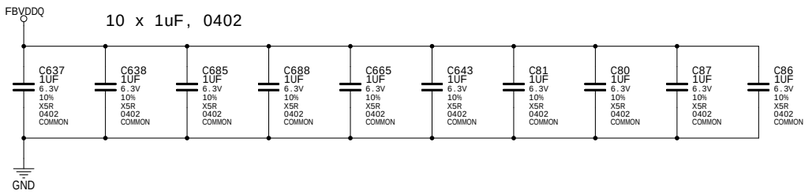
GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update









ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

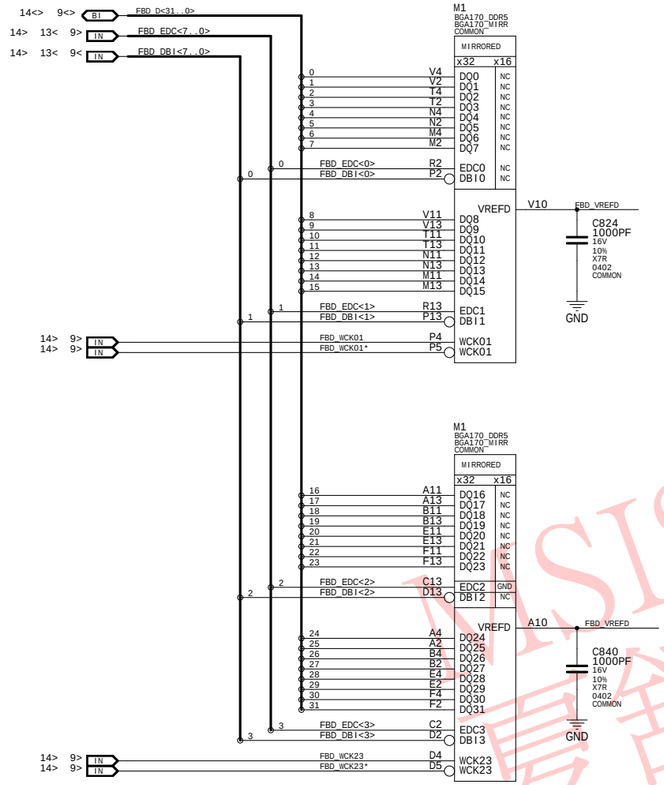
NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	11 OF 34
BOM REV	A	DATE	12-MAY-2010

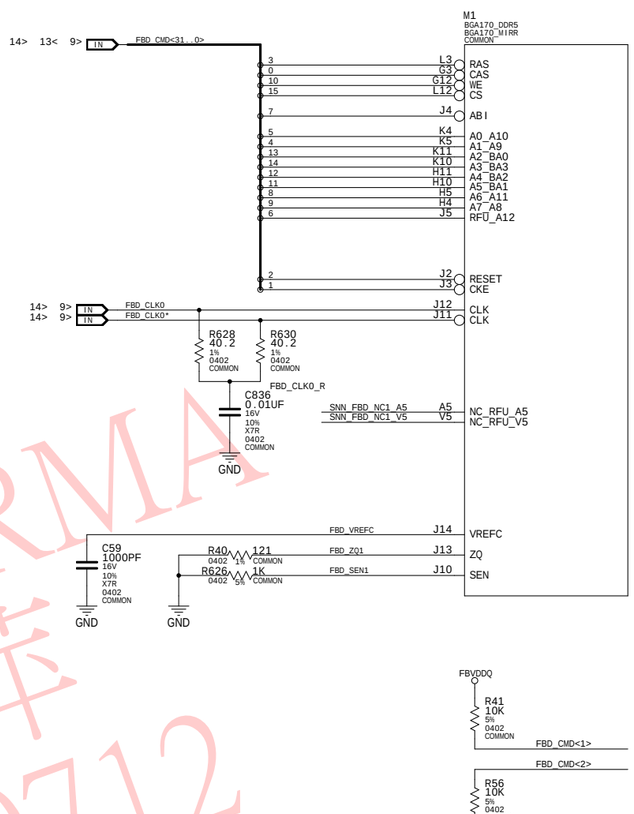
Page12: FBD Partition 31..0

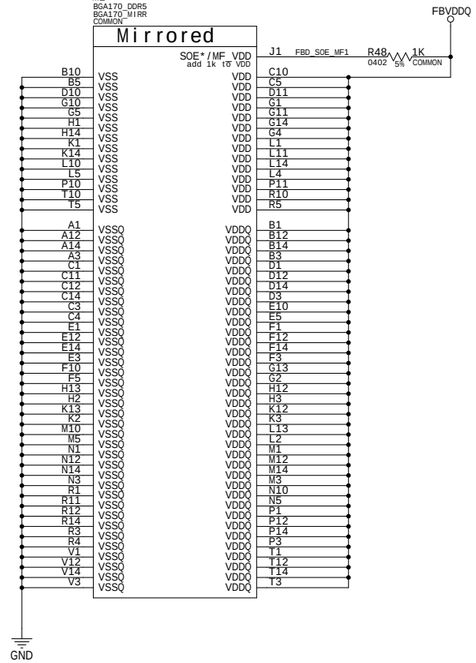
GDDR5 CMD Mapping

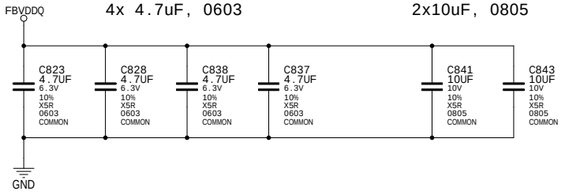
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

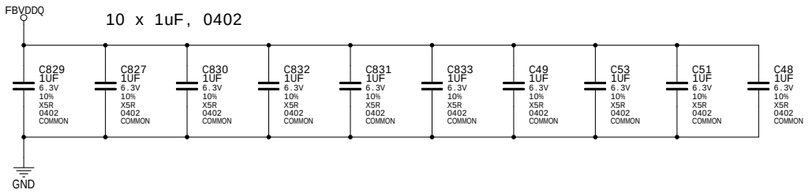
** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update

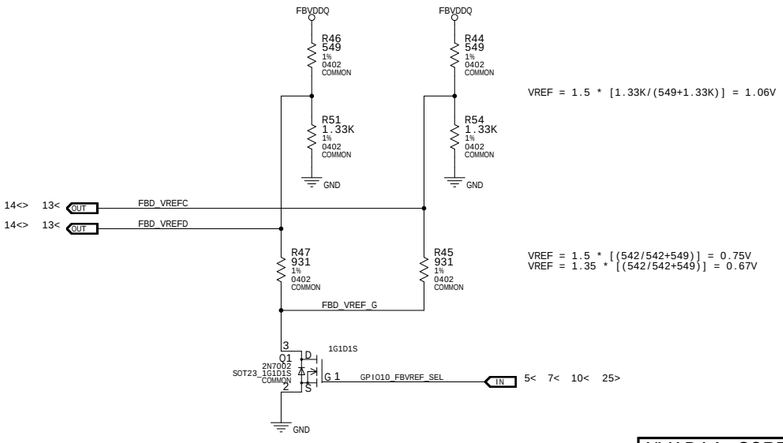












ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

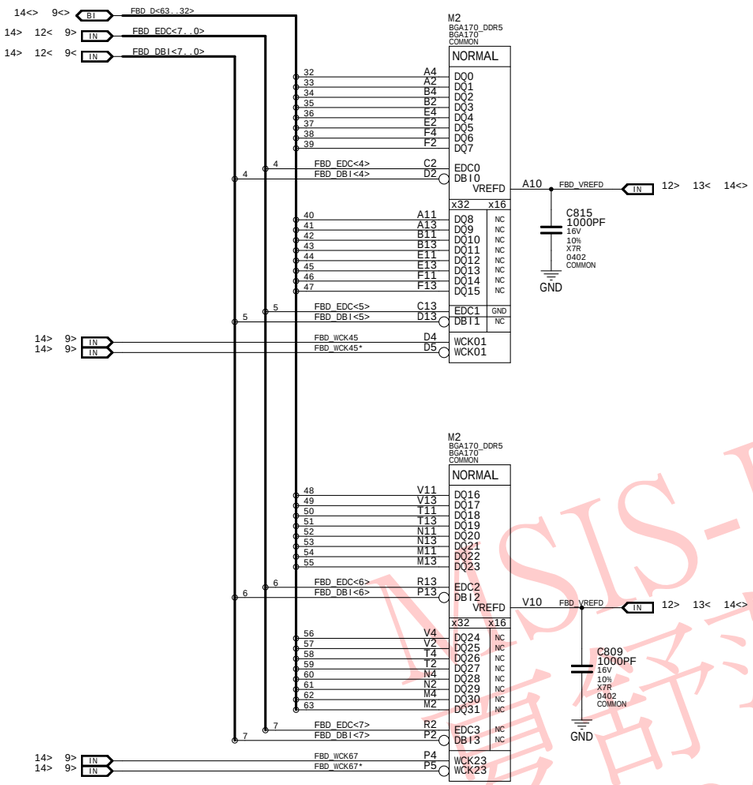
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

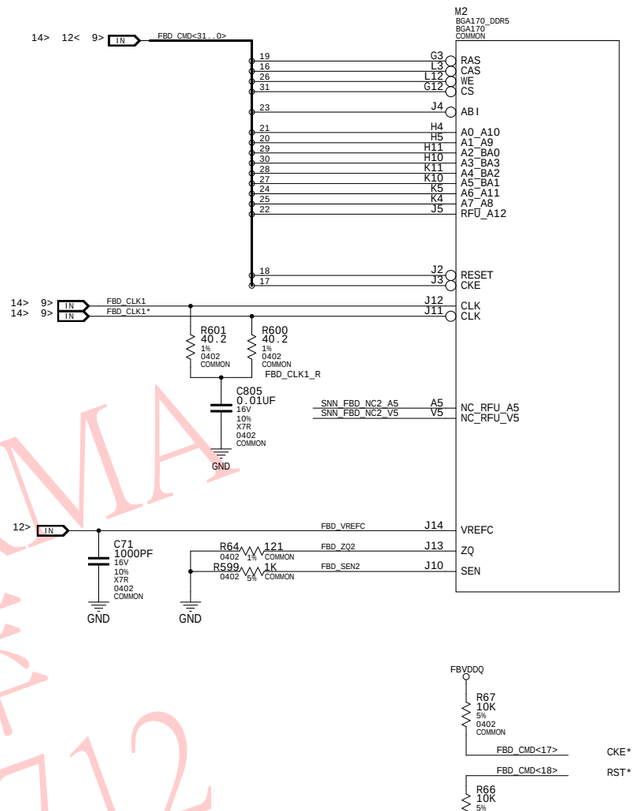
NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	12 OF 34
BOM REV	A	DATE	12-MAY-2010

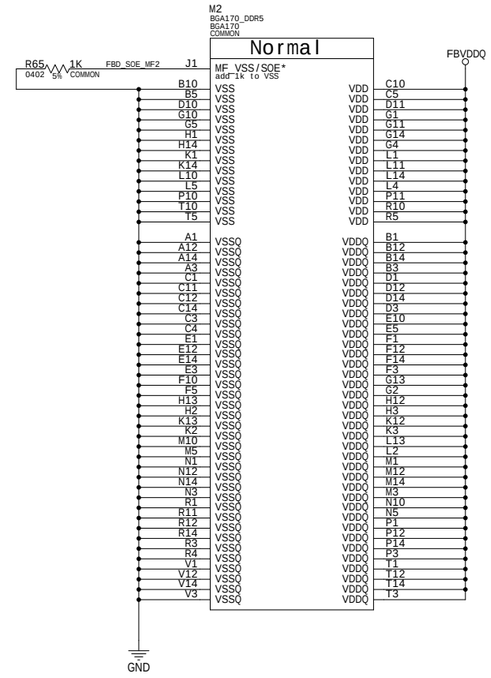
Page13: FBD Partition 63..32

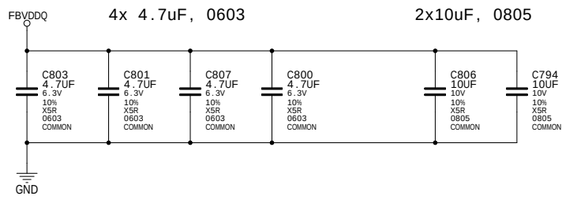
GDDR5 CMD Mapping		
CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

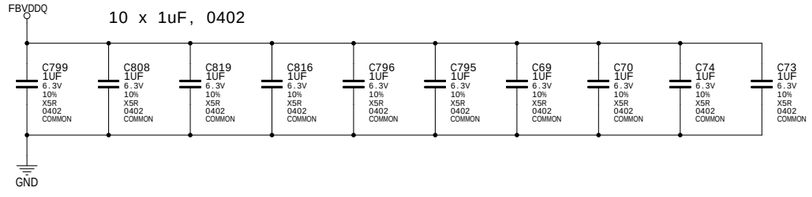
** Vref switching options:
- internal Vref should be POR for VrefD
- potential for update











ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	13 OF 34
BOM REV	A	DATE	12-MAY-2010

Page14: FB Net Properties

NET RULES for FrameBuffer A/B

Ref	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
5< 4>	OUT	FBA_CLK0	1	80DIFF	FBA_CLK0
5< 4>	OUT	FBA_CLK0*	1	80DIFF	FBA_CLK0
6< 4>	OUT	FBA_CLK1	1	80DIFF	FBA_CLK1
6< 4>	OUT	FBA_CLK1*	1	80DIFF	FBA_CLK1
7< 4>	OUT	FBB_WCK01	1	80DIFF	FBB_WCK01
7< 4>	OUT	FBB_WCK01*	1	80DIFF	FBB_WCK01
7< 4>	OUT	FBB_WCK23	1	80DIFF	FBB_WCK23
7< 4>	OUT	FBB_WCK23*	1	80DIFF	FBB_WCK23
8< 4>	OUT	FBB_WCK45	1	80DIFF	FBB_WCK45
8< 4>	OUT	FBB_WCK45*	1	80DIFF	FBB_WCK45
8< 4>	OUT	FBB_WCK67	1	80DIFF	FBB_WCK67
8< 4>	OUT	FBB_WCK67*	1	80DIFF	FBB_WCK67
6< 5< 4>	OUT	FBA_CMD<31..0>	1	45OHM	
6< 5< 4<	OUT	FBA_EDC<7..0>	1	45OHM	
6< 5< 4<	OUT	FBA_DBI<7..0>	1	45OHM	
6<> 5<> 4<>	BI	FBA_D<63..0>	1	45OHM	

Ref	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
7< 4>	OUT	FBB_CLK0	1	80DIFF	FBB_CLK0
7< 4>	OUT	FBB_CLK0*	1	80DIFF	FBB_CLK0
8< 4>	OUT	FBB_CLK1	1	80DIFF	FBB_CLK1
8< 4>	OUT	FBB_CLK1*	1	80DIFF	FBB_CLK1
5< 4>	OUT	FBA_WCK01	1	80DIFF	FBA_WCK01
5< 4>	OUT	FBA_WCK01*	1	80DIFF	FBA_WCK01
5< 4>	OUT	FBA_WCK23	1	80DIFF	FBA_WCK23
5< 4>	OUT	FBA_WCK23*	1	80DIFF	FBA_WCK23
6< 4>	OUT	FBA_WCK45	1	80DIFF	FBA_WCK45
6< 4>	OUT	FBA_WCK45*	1	80DIFF	FBA_WCK45
6< 4>	OUT	FBA_WCK67	1	80DIFF	FBA_WCK67
6< 4>	OUT	FBA_WCK67*	1	80DIFF	FBA_WCK67
8< 7< 4>	OUT	FBB_CMD<31..0>	1	45OHM	
8< 7< 4>	OUT	FBB_EDC<7..0>	1	45OHM	
8< 7< 4<	OUT	FBB_DBI<7..0>	1	45OHM	
8<> 7<> 4<>	BI	FBB_D<63..0>	1	45OHM	

Ref	Port	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
6< 5>	BI	FBA_VREFD	1.00V	0.02A	8MIL
6< 5>	BI	FBA_VREFC	1.00V	0.02A	8MIL
8< 7>	BI	FBB_VREFD	1.00V	0.02A	8MIL
8< 7>	BI	FBB_VREFC	1.00V	0.02A	8MIL

NET RULES for FrameBuffer C/D

Ref	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
10< 9>	OUT	FBC_CLK0	1	80DIFF	FBC_CLK0
10< 9>	OUT	FBC_CLK0*	1	80DIFF	FBC_CLK0
11< 9>	OUT	FBC_CLK1	1	80DIFF	FBC_CLK1
11< 9>	OUT	FBC_CLK1*	1	80DIFF	FBC_CLK1
10< 9>	OUT	FBC_WCK01	1	80DIFF	FBC_WCK01
10< 9>	OUT	FBC_WCK01*	1	80DIFF	FBC_WCK01
10< 9>	OUT	FBC_WCK23	1	80DIFF	FBC_WCK23
10< 9>	OUT	FBC_WCK23*	1	80DIFF	FBC_WCK23
11< 9>	OUT	FBC_WCK45	1	80DIFF	FBC_WCK45
11< 9>	OUT	FBC_WCK45*	1	80DIFF	FBC_WCK45
11< 9>	OUT	FBC_WCK67	1	80DIFF	FBC_WCK67
11< 9>	OUT	FBC_WCK67*	1	80DIFF	FBC_WCK67
11< 10< 9>	OUT	FBC_CMD<31..0>	1	45OHM	
11< 10< 9>	OUT	FBC_EDC<7..0>	1	45OHM	
11< 10< 9>	OUT	FBC_DBI<7..0>	1	45OHM	
10<> 9<> 11<>	BI	FBC_D<63..0>	1	45OHM	

Ref	Port	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
12< 9>	OUT	FBD_CLK0	1	80DIFF	FBD_CLK0
12< 9>	OUT	FBD_CLK0*	1	80DIFF	FBD_CLK0
13< 9>	OUT	FBD_CLK1	1	80DIFF	FBD_CLK1
13< 9>	OUT	FBD_CLK1*	1	80DIFF	FBD_CLK1
12< 9>	OUT	FBD_WCK01	1	80DIFF	FBD_WCK01
12< 9>	OUT	FBD_WCK01*	1	80DIFF	FBD_WCK01
12< 9>	OUT	FBD_WCK23	1	80DIFF	FBD_WCK23
12< 9>	OUT	FBD_WCK23*	1	80DIFF	FBD_WCK23
13< 9>	OUT	FBD_WCK45	1	80DIFF	FBD_WCK45
13< 9>	OUT	FBD_WCK45*	1	80DIFF	FBD_WCK45
13< 9>	OUT	FBD_WCK67	1	80DIFF	FBD_WCK67
13< 9>	OUT	FBD_WCK67*	1	80DIFF	FBD_WCK67
13< 12< 9>	OUT	FBD_CMD<31..0>	1	45OHM	
13< 12< 9>	OUT	FBD_EDC<7..0>	1	45OHM	
13< 12< 9<	OUT	FBD_DBI<7..0>	1	45OHM	
12<> 9<> 13<>	BI	FBD_D<63..0>	1	45OHM	

Ref	Port	NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
11< 10>	BI	FBC_VREFD	1.00V	0.02A	8MIL
11< 10>	BI	FBC_VREFC	1.00V	0.02A	8MIL
13< 12>	BI	FBD_VREFD	1.00V	0.02A	8MIL
13< 12>	BI	FBD_VREFC	1.00V	0.02A	8MIL

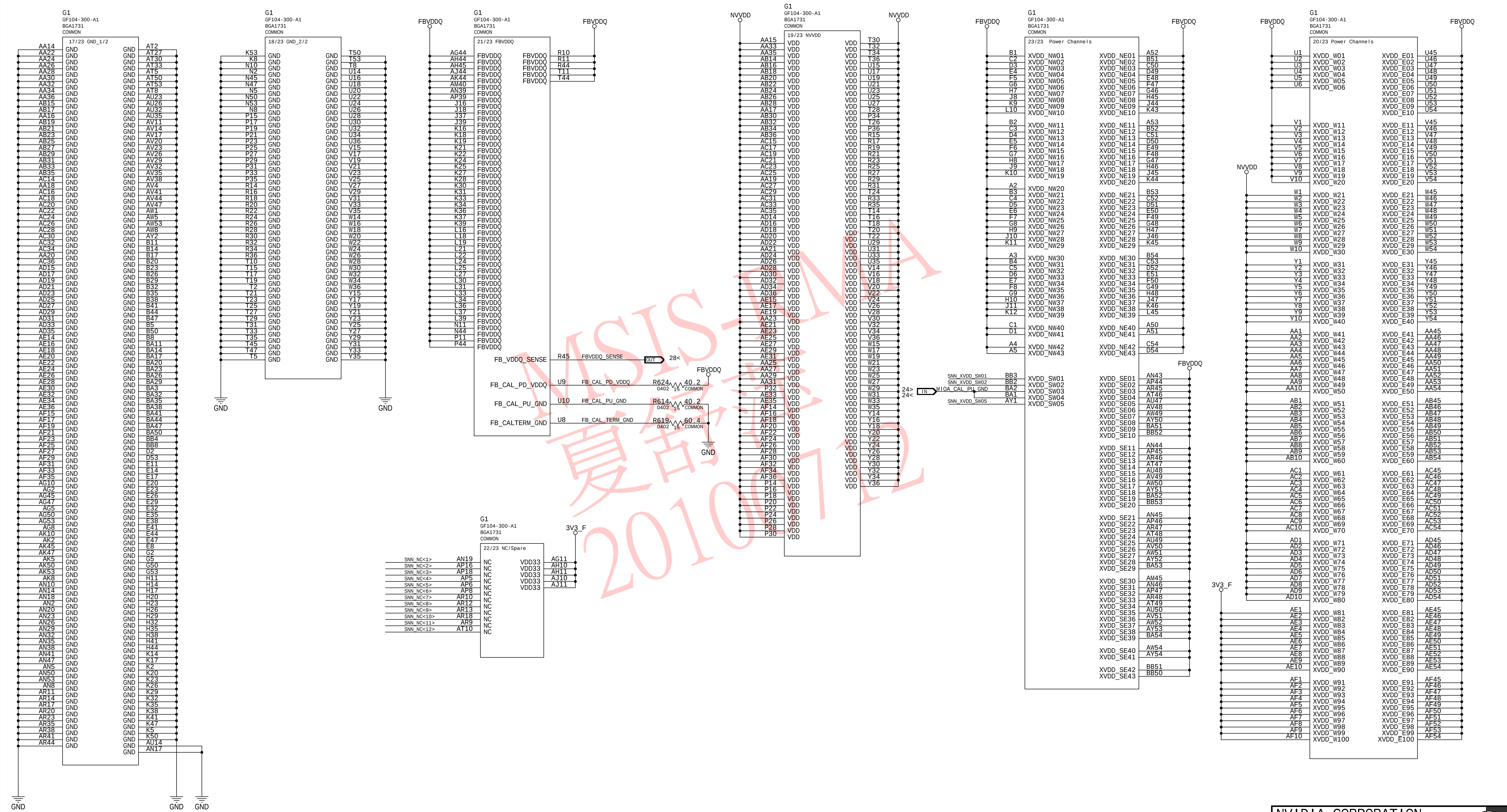
ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	14 OF 34
BOM REV	A	DATE	12-MAY-2010

Page15: GPU PWR and GND

** Power channels are configurable.
XVDD_* pins are not connected on the substrate.
Therefore, XVDD_* pins can be assigned as needed.

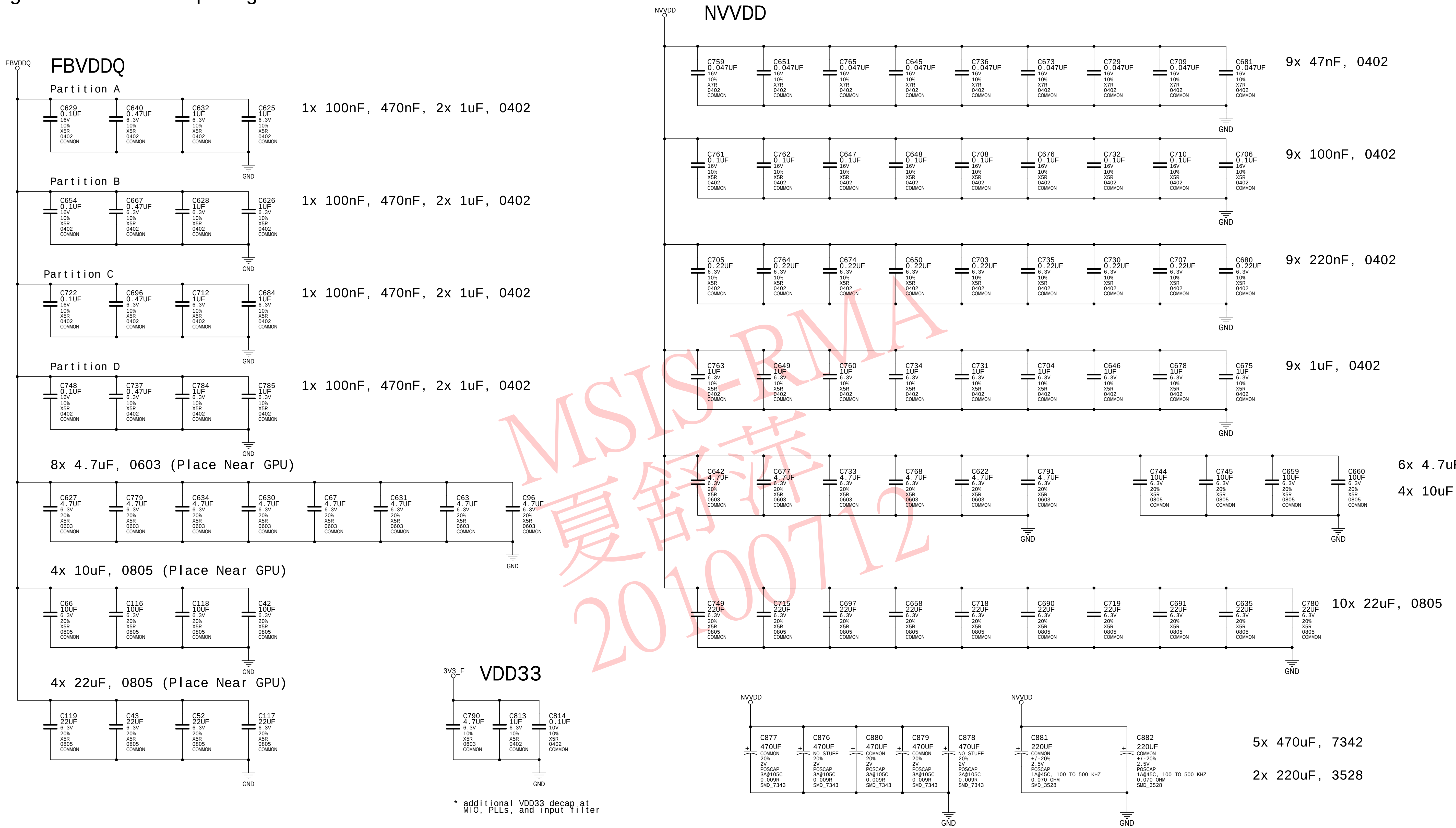


ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	15 OF 34
BOM REV	A	DATE	12-MAY-2010

Page16: GPU Decoupling



ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I+mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	16 OF 34
BOM REV	A	DATE	12-MAY-2010

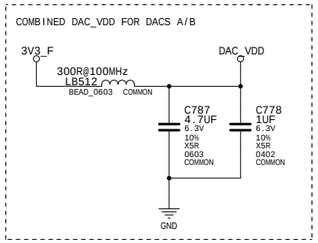
Page17: Blank

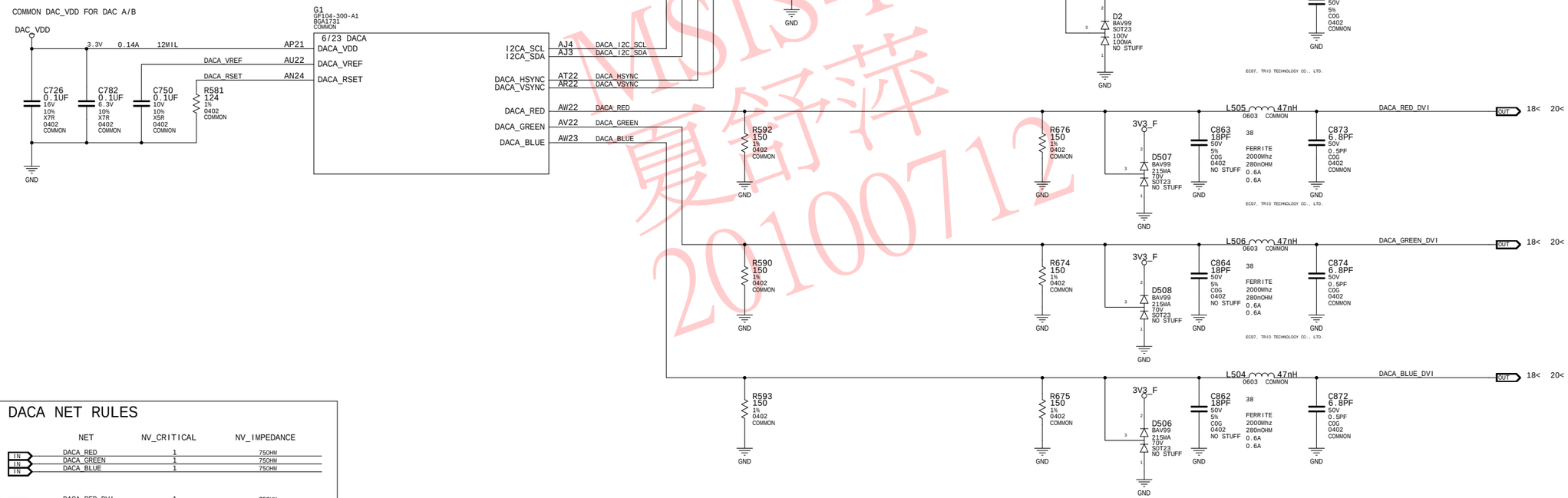
ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	17 OF 34
BOM REV	A	DATE	12-MAY-2010

Page18: DACA (South)





DACA NET RULES

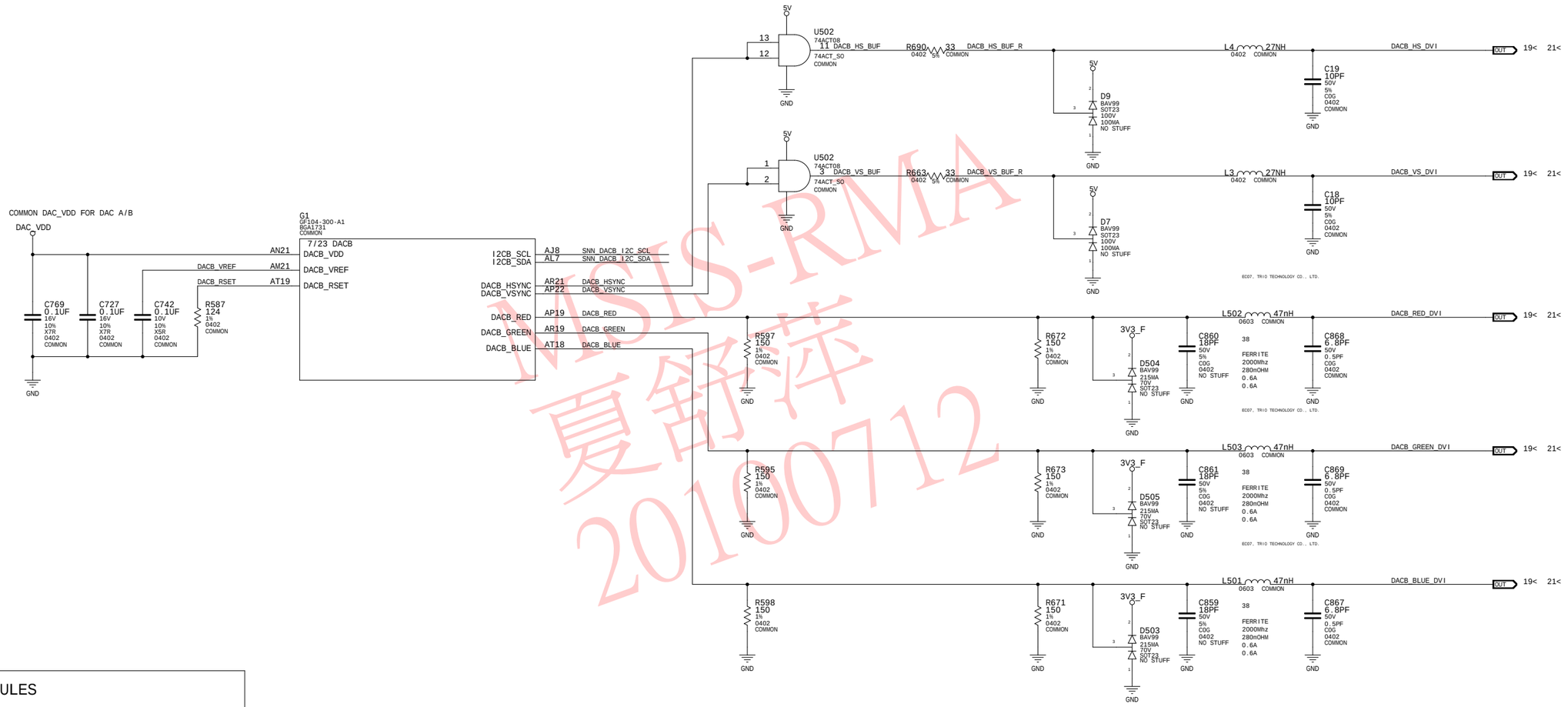
	NET	NV_CRITICAL	NV_IMPEDANCE
IN	DACA_RED	1	75OHM
IN	DACA_GREEN	1	75OHM
IN	DACA_BLUE	1	75OHM
20< 18> IN	DACA_RED_DVI	1	75OHM
20< 18> IN	DACA_GREEN_DVI	1	75OHM
20< 18> IN	DACA_BLUE_DVI	1	75OHM
IN	DACA_HSYNC	2	50OHM
IN	DACA_VSYNC	2	50OHM
IN	DACA_HS_BUF	2	50OHM
IN	DACA_VS_BUF	2	50OHM
IN	DACA_HS_BUF_R	2	50OHM
IN	DACA_VS_BUF_R	2	50OHM
20< 18> IN	DACA_HS_DVI	2	50OHM
20< 18> IN	DACA_VS_DVI	2	50OHM

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	18 OF 34
BOM REV	A	DATE	12-MAY-2010

Page19: DACB (Mid)



DACB NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE
IN	DACB_RED	1	75OHM
IN	DACB_GREEN	1	75OHM
IN	DACB_BLUE	1	75OHM
21< 19> IN	DACB_RED_DVI	1	75OHM
21< 19> IN	DACB_GREEN_DVI	1	75OHM
21< 19> IN	DACB_BLUE_DVI	1	75OHM
IN	DACB_HSYNC	2	50OHM
IN	DACB_VSYNC	2	50OHM
IN	DACB_HS_BUF	2	50OHM
IN	DACB_VS_BUF	2	50OHM
IN	DACB_HS_BUF_R	2	50OHM
IN	DACB_VS_BUF_R	2	50OHM
21< 19> IN	DACB_HS_DVI	2	50OHM
21< 19> IN	DACB_VS_DVI	2	50OHM

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	19 OF 34
BOM REV	A	DATE	12-MAY-2010

Page20: IFPAB DVI-I-DL (South)

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	20 OF 34
BOM REV	A	DATE	12-MAY-2010

Page21: IFPEF DVI-I-DL (Mid)

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

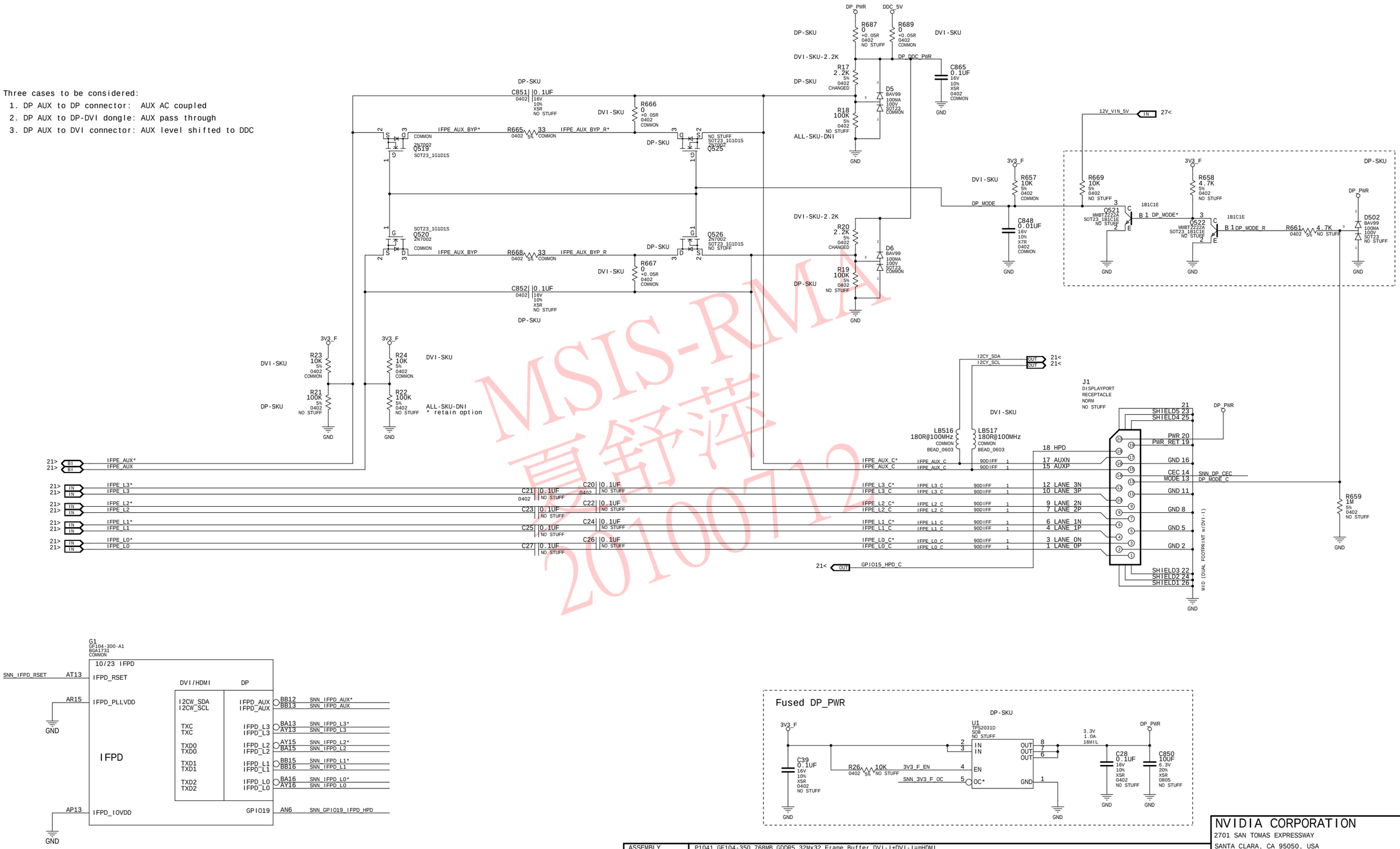
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	21 OF 34
BOM REV	A	DATE	12-MAY-2010

Page22: IFPEF DP (Mid)

Three cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through
3. DP AUX to DVI connector: AUX level shifted to DDC

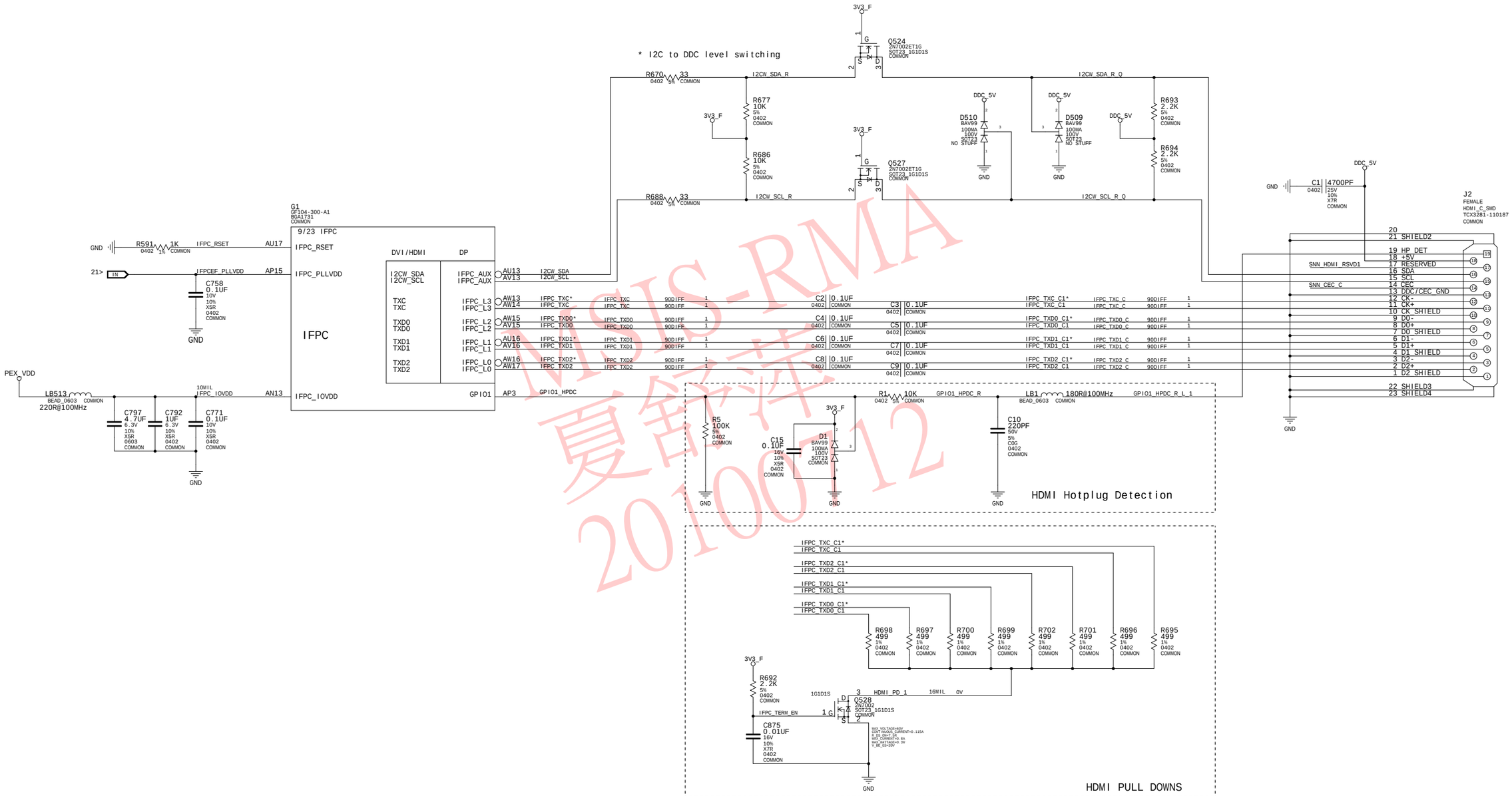


ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	22 OF 34
BOM REV	A	DATE	12-MAY-2010

Page23: IFPC mHDMI (North)

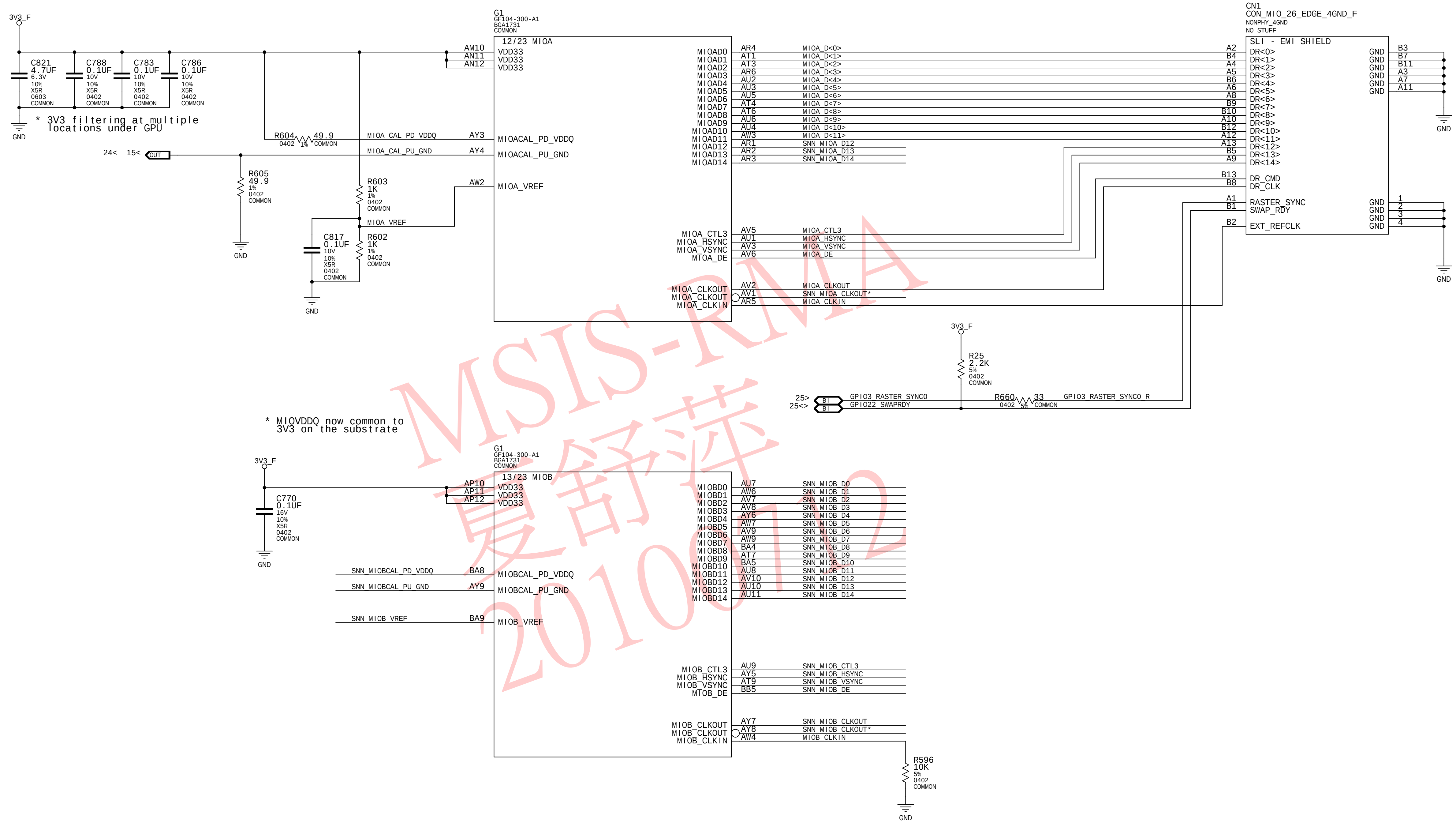


ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE_DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	23 OF 34
BOM REV	A	DATE	12-MAY-2010

Page24: Multi-use IO (MIO) Interface



MIO NET RULES

	NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IN	MIOA_D<11..0>	1	50OHM	
IN	MIOA_HSYNC	1	50OHM	
IN	MIOA_VSYNC	1	50OHM	
IN	MIOA_CTL3	1	50OHM	
IN	MIOA_DE	1	50OHM	
IN	MIOA_CLKOUT	1	50OHM	
IN	MIOA_CLKIN	1	50OHM	

24> 15<

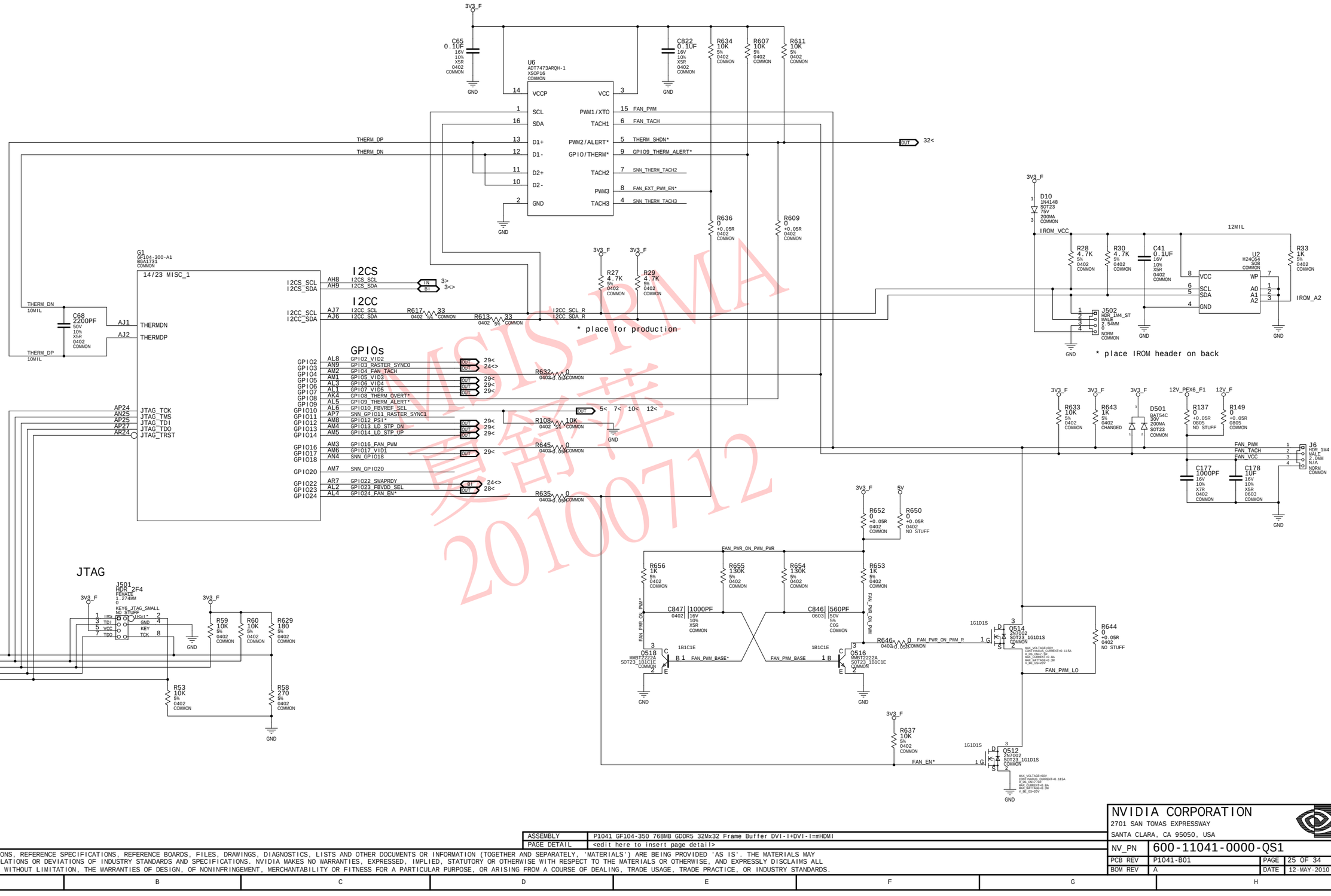
	NET	VOLTAGE	MIN_WIDTH
IN	MIOA_VREF	1.65V	6MIL
IN	MIOA_CAL_PD_VDDQ	3.3V	6MIL
IN	MIOA_CAL_PU_GND	0.0V	6MIL

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	24 OF 34
BOM REV	A	DATE	12-MAY-2010

Page25: Misc: Fan, Thermal, JTAG, GPIO



ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	25 OF 34
BOM REV	A	DATE	12-MAY-2010

Page26: Misc: ROM, HDCP, XTAL, Straps

STRAP0	USER_BIT [3..0]	0000:=> 5K PD
STRAP1	3GIO_PADCFG_LUT_ADR	0000 :=>5K PD 0000 Desktop
STRAP2	PCI_DEVID [3:0]	0010 For 0x0E22 :=> 15K PD 0100 For 0x0E24 :=> 25K PD
ROM_SI	RAMCFG[0]	32Mx32 256 bit Samsung for SKU 10 first memory 0011: PD 20K 32Mx32 256 bit Hynix for SKU 10 2'nd memory 0010: PD 15K
	RAMCFG[1]	
	RAMCFG[2]	32Mx32 192 bit Samsung for SKU 0 first memory 1011: PU 20K 32Mx32 192 bit Hynix for SKU 0 2'nd memory 1010: PU 15K
	RAMCFG[3]	
ROM_SO	VGA_DEVICE	1
	SMB_ALT_ADDR	0 — 10k PD
	FB[0]_BAR_SIZE	0
	XCLK_417	0
ROM_SCLK	PEX_PLL_EN_TERM100	1 ENABLED
	SLOT_CLK_CFG	1 ENABLE — 45K PD
	SUB_VENDOR	1 Dedicated BIOS
	PCI_DEVID_EXT	0 0xC

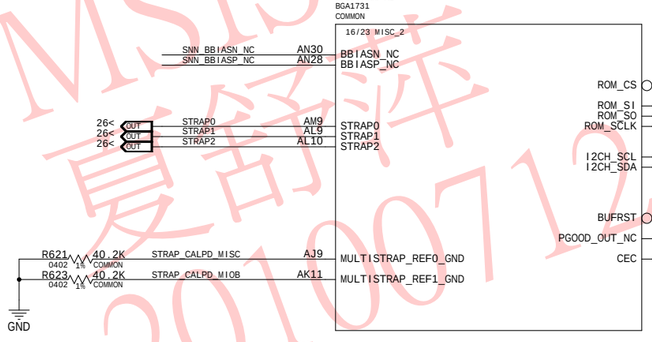
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

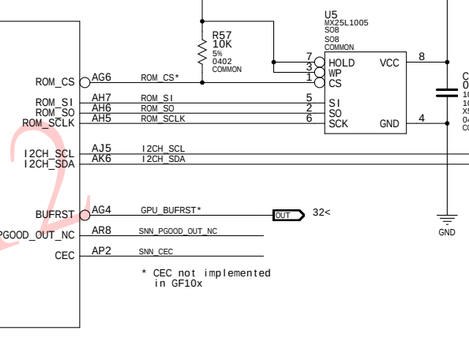
CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit	Qimonda
0010	32Mx32 256-bit	Hynix
0011	32Mx32 256-bit	Samsung
0100	Reserved	
0101	64Mx32 256-bit	Qimonda
0110	64Mx32 256-bit	Hynix
0111	64Mx32 256-bit	Samsung
1000	Reserved	
1001	32Mx32 192-bit	Qimonda
1010	32Mx32 192-bit	Hynix
1011	32Mx32 192-bit	Samsung
1100	Reserved	
1101	64Mx32 192-bit	Qimonda
1110	64Mx32 192-bit	Hynix
1111	64Mx32 192-bit	Samsung

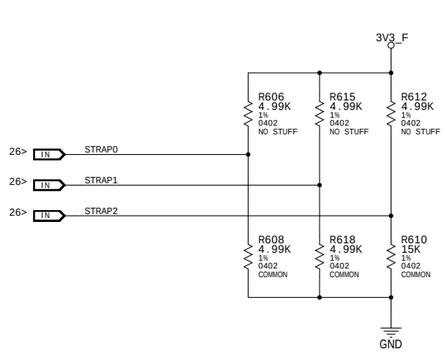
MISC NET RULES

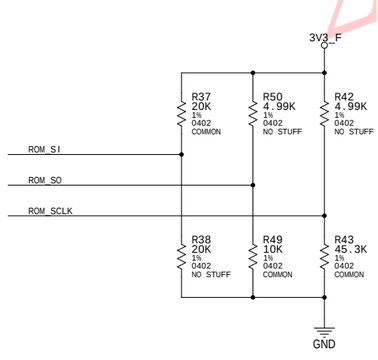
NET	NV_CRITICAL	NV_IMPEDANCE
XTALSSIN	1	50OHM
XTALIN	1	50OHM
XTALOUT	1	50OHM

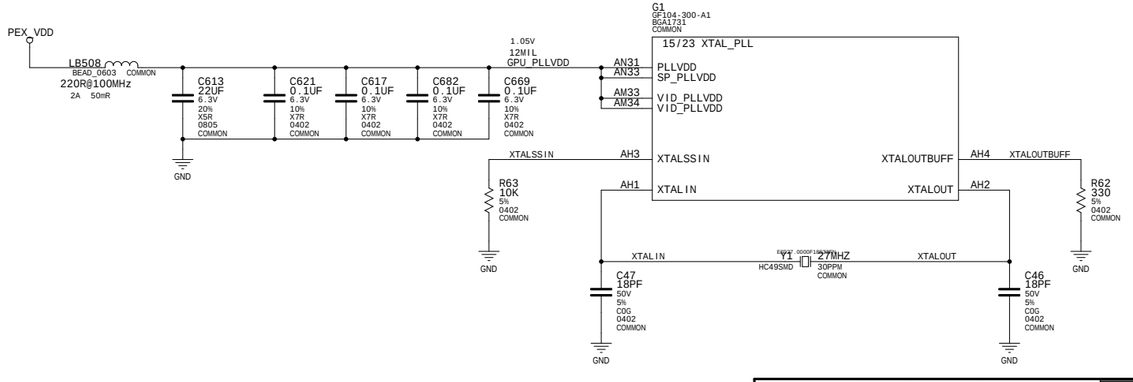
	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	40.2k 1% TO GND	NC
BINARY BRINGUP	NC	NC
MULTI-LEVEL	40.2k 1% TO GND	40.2k 1% TO GND









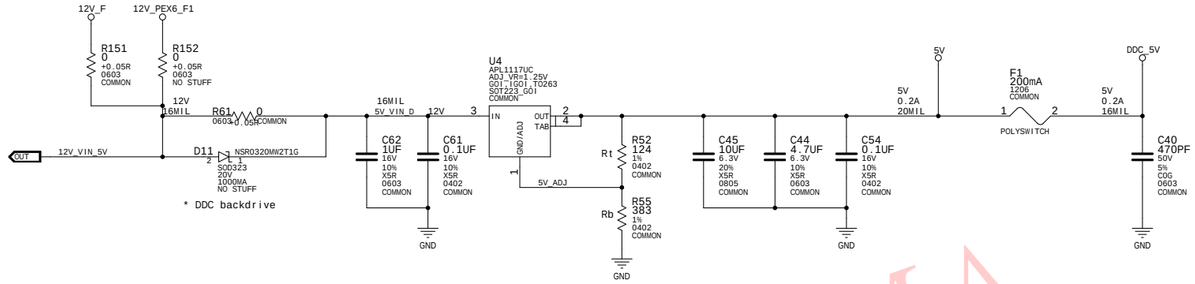


ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

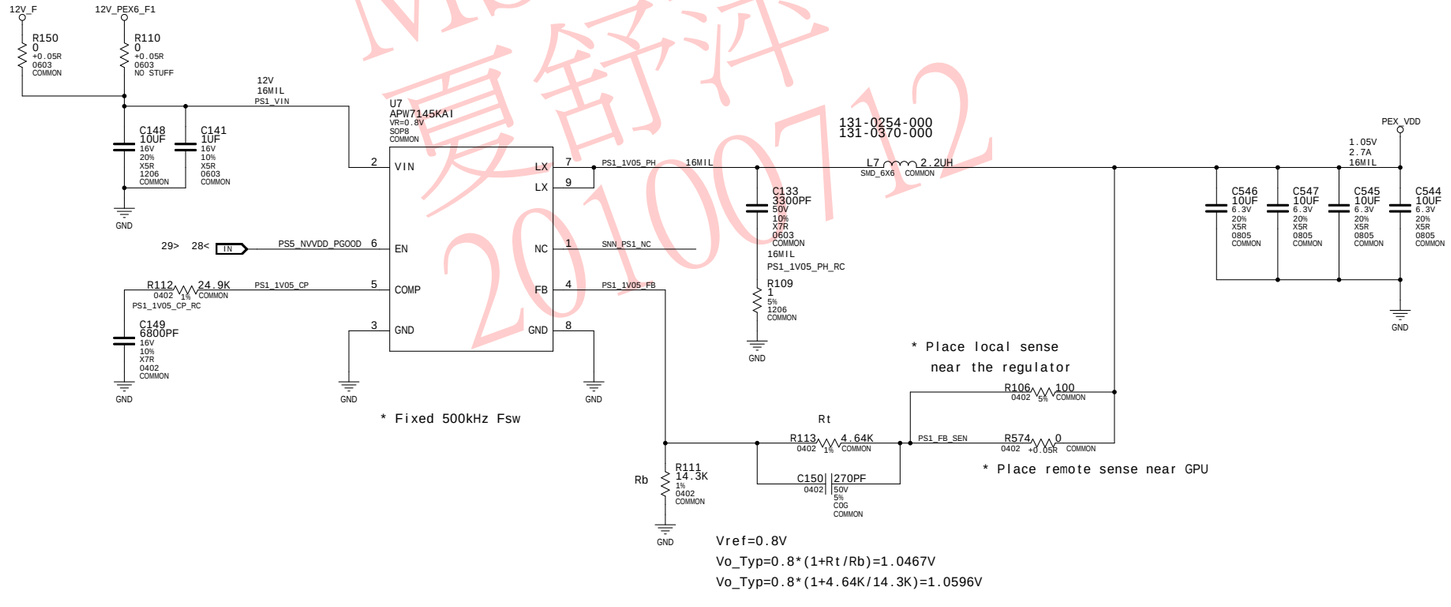
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	26 OF 34
BOM REV	A	DATE	12-MAY-2010

Page27: PS: 5V, PEX_VDD



Input ripple (Irms) = ~0.9A @ 2.7A



ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	27 OF 34
BOM REV	A	DATE	12-MAY-2010

Page28: PS: FBVDD/Q

Input ripple (Irms) = 8.8A @ 23A

12V_F

C514 0.47UF 16V 10% X7R 0603 COMMON

C515 1UF 16V 10% X5R 0603 COMMON

C155 10UF 16V 20% X5R 1206 COMMON

C154 10UF 16V 20% X5R 1206 COMMON

C156 270uF COMMON 20% 16V OCCAP 5.5A@105C 0.010R TH_D80P35

1nd: 041-0146-000
2nd: 042-0083-000

* place close to drain of Top FET

APW7165:315-0460-000
uP6101: 315-0462-000

U8 APW7165A VR=0.8V PSOP8 COMMON

R114 2.2 5% 0402 COMMON

C151 1UF 16V 10% X5R 0603 COMMON

12V_PS3_R 20MIL

VCC, BOOT, HDRV, PHASE, COMP/EN, GND, GND, LDRV, FB

R553 0 0402 0.05R COMMON — 20MIL PS3_FBVDDQ_UG_R

R552 2.2 0402 5% COMMON — 20MIL PS3_FBVDDQ_BOOT_RC — C527 0.1UF 16V 10% X5R COMMON

20MIL PS3_FBVDDQ_BOOT

20MIL PS3_FBVDDQ_UG

20MIL PS3_FBVDDQ_PHASE

R555 0 0402 0.05R COMMON — 20MIL PS3_FBVDDQ_LG

20MIL PS3_FBVDDQ_FB — 12MIL

Q6 NTMFS4945NT1G LFPAK COMMON

Q5 NTMFS4939NT1G LFPAK COMMON

C537 3300PF 50V 10% X7R 0402 COMMON

Q4 NTMFS4939NT1G LFPAK COMMON

131-0477-000

L6 0.6uH TH COMMON

C137 330PF 50V C0G 0603 NO STUFF

C129 2200PF 50V 10% X7R 0603 COMMON 20MIL PS3_FBVDDQ_RC

R107 1 5% 1206 COMMON

APW7165: 2200pF
uP6101BS8: 3300pF

APW7165: 1 ohm
uP6101BS8: 3.3 ohm

FBVDDQ

1.5V 25A 14MIL

C99 1UF 6.3V 10% X5R 0402 COMMON

C97 4.7UF 6.3V 10% X5R 0603 COMMON

C98 4.7UF 6.3V 10% X5R 0603 COMMON

C95 820uF COMMON 20% 2.5V OCCAP 5.0A@105C 0.007R TH_D63P25

C103 820uF COMMON 20% 2.5V OCCAP 5.0A@105C 0.007R TH_D63P25

1nd: 041-0147-000
2nd: 042-0087-000

APW7165: 100nF
uP6101BS8: 10nF

C521 0.5PF 50V 0.25PF C0G COMMON

R534 20K 0402 1% COMMON — PS3_CP — C520 0.1UF 16V 10% X5R COMMON

APW7165: 12.7K ohm
uP6101BS8: 12.7K ohm

APW7165: 15pF
uP6101BS8: 47pF

PS3_FS_DIS

Fixed 300kHz Fsw

Cap for shoot-through protection. Results in high/max OCP setpoint.

APW7165: 0 ohm
uP6101BS8: 22 ohm

APW7165: 6800pF
uP6101BS8: 6800pF

R545 0 0402 0.05R COMMON — 12MIL PS3_FBVDDQ_FB_RC — C526 6800PF 16V 10% X7R COMMON

R542 1.02K 0402 1% COMMON — PS3_FBVDDQ_VSEN 12MIL — R93 100 0402 5% COMMON

R94 0 0402 0.05R COMMON — FBVDDQ_SENSE — IN 15>

Rt

Vref=0.8V
Vo_Typ=0.8*(1+1.02/(1.47//5.76))=1.497V
Vo_Typ=0.8*(1+1.02/1.47)=1.355V

Rb

R551 4.32K 1% 0402 COMMON

R540 1.47K 1% 0402 COMMON

3V3_F

R554 10K 5% 0402 COMMON

R533 10K 5% 0402 COMMON

29> 27< IN PS5_NVVDD_PGOOD

32> IN 12V_PRSNT*

PS3_EN*

Q505 2N7002 SOT23_1G1D1S COMMON

Q506 2N7002 SOT23_1G1D1S COMMON

Q507 2N7002 SOT23_1G1D1S COMMON

C533 0.1UF 16V 10% X5R 0402 COMMON

gates PGOOD prior to NVVDD controller being enabled

R557 10K 5% 0402 COMMON

25> IN GPIO23_FBVDD_SEL — R556 1K 0402 5% COMMON — GPIO23_FBVDD_SEL_G

Q508 2N7002 SOT23_1G1D1S COMMON

PS3_FBVDDQ_FB_D

C548 0.01UF 16V 10% X7R 0402 COMMON

FBVDD/Q	GPIO23
1.35V	0
1.5V	1

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE_DETAIL	<edit here to insert page detail>

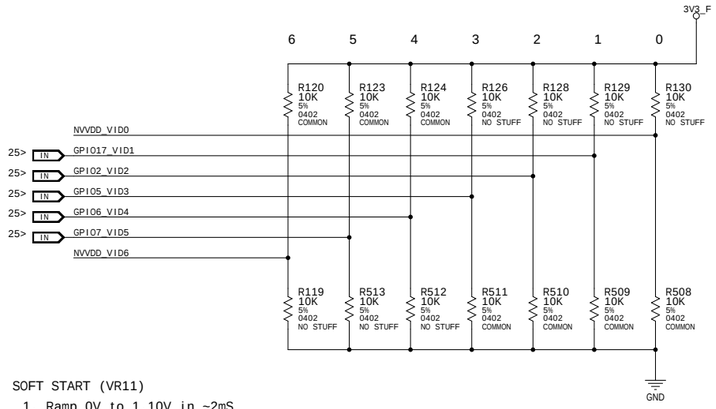
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	28 OF 34
BOM REV	A	DATE	12-MAY-2010

Page29: PS: NVVDD Controller

VID Table

GPIO7	GPIO6	GPIO5	GPIO2	GPIO17	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

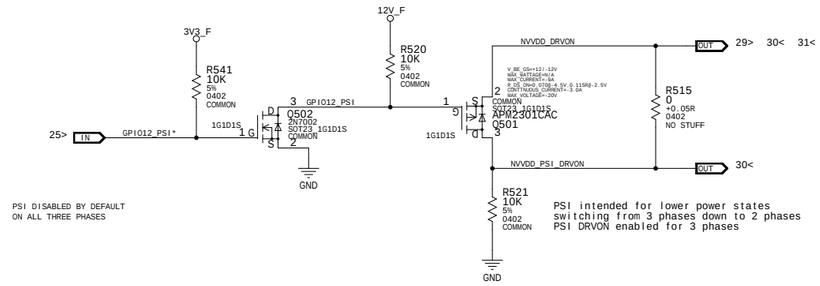


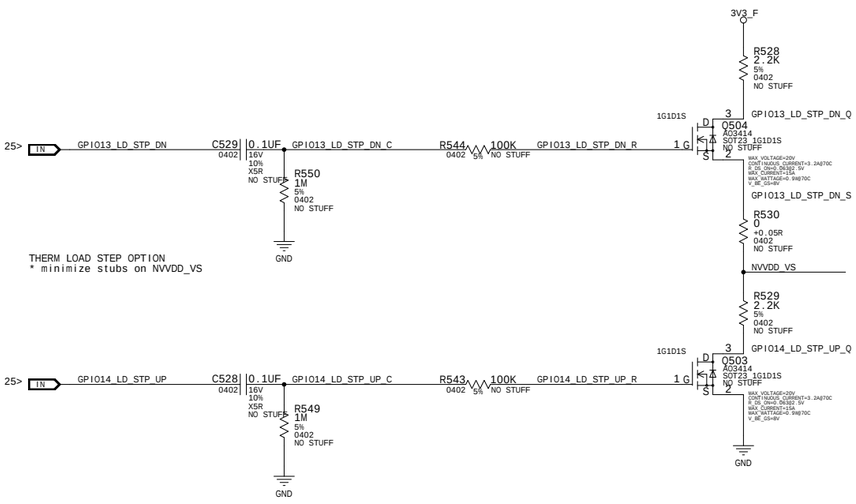
SOFT START (VR11)

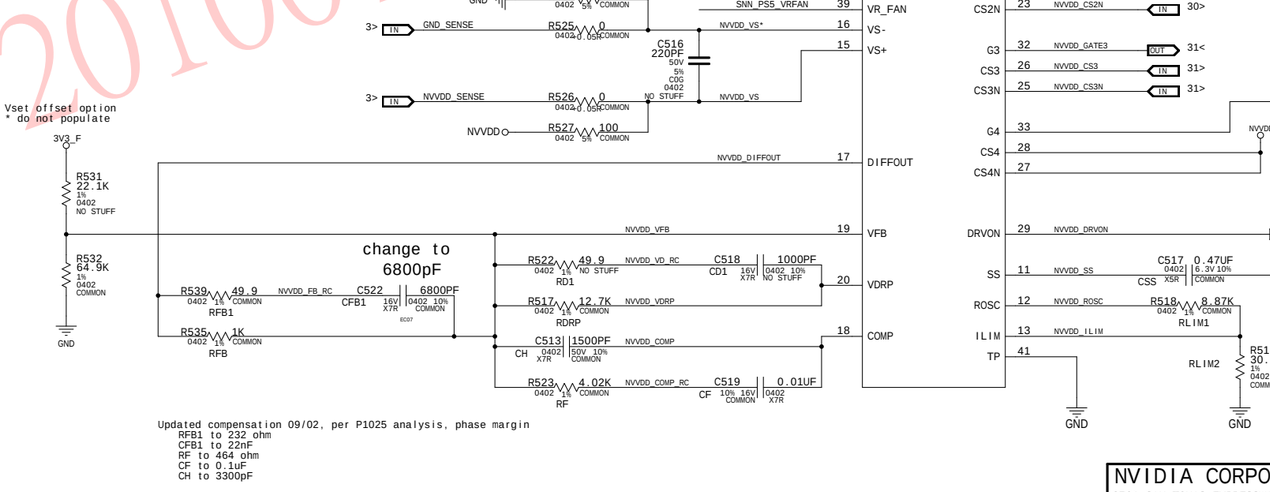
1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPIO tri-state
   VID[5:1]=11000 to set 0.9125V

P-STATE VOLTAGES

1. P0 at 1.05V
2. P8/P12 at 0.80V







Updated compensation 09/02, per P1025 analysis, phase margin
RFB1 to 232 ohm
CFB1 to 22nF
RF to 464 ohm
CF to 0.1uF
CH to 3300pF

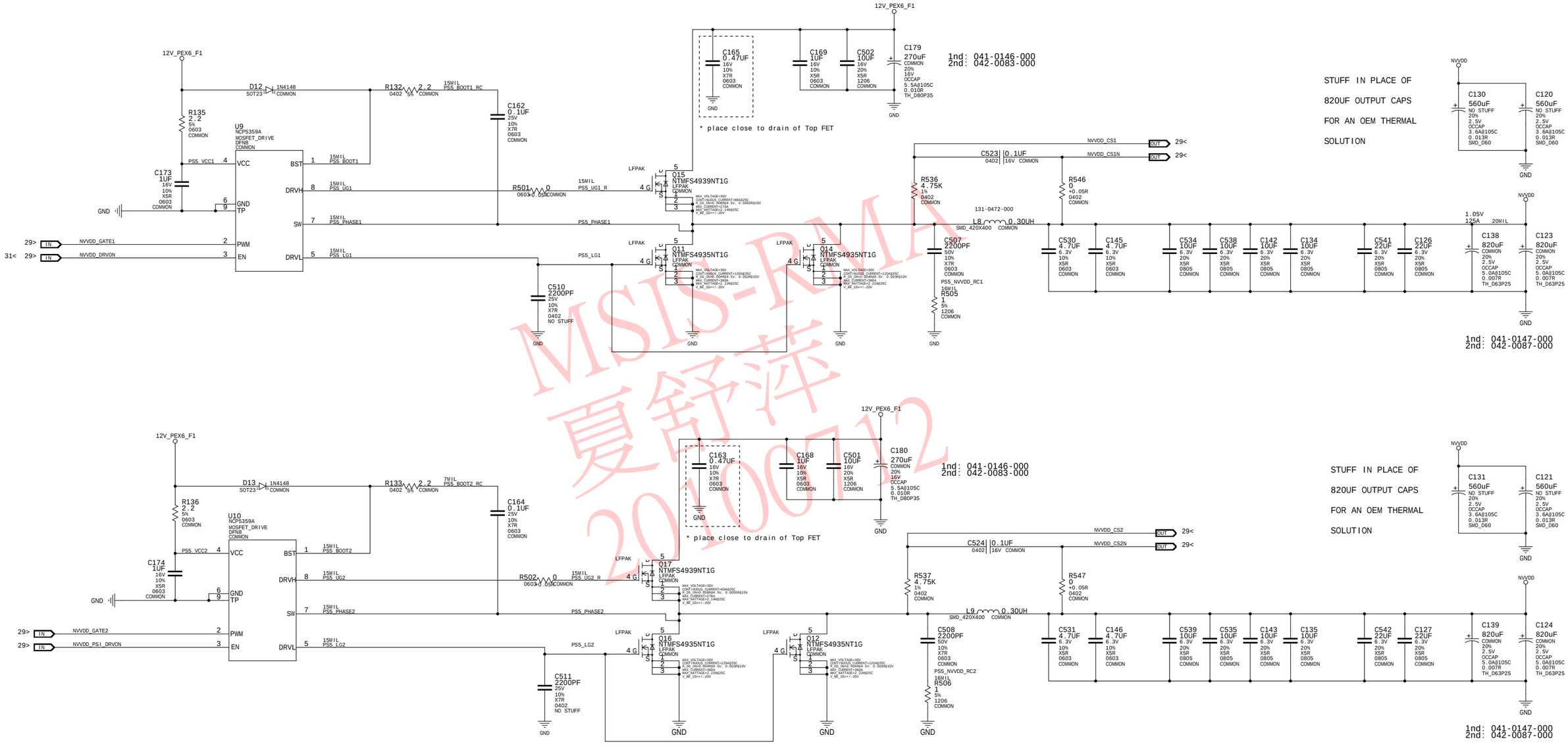
ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	29 OF 34
BOM REV	A	DATE	12-MAY-2010

Page30: PS: NVVDD Phase 1-2

Input ripple (Irms)/phase = 10.175A @ 90A
Irms shared across phase 1-2 input caps



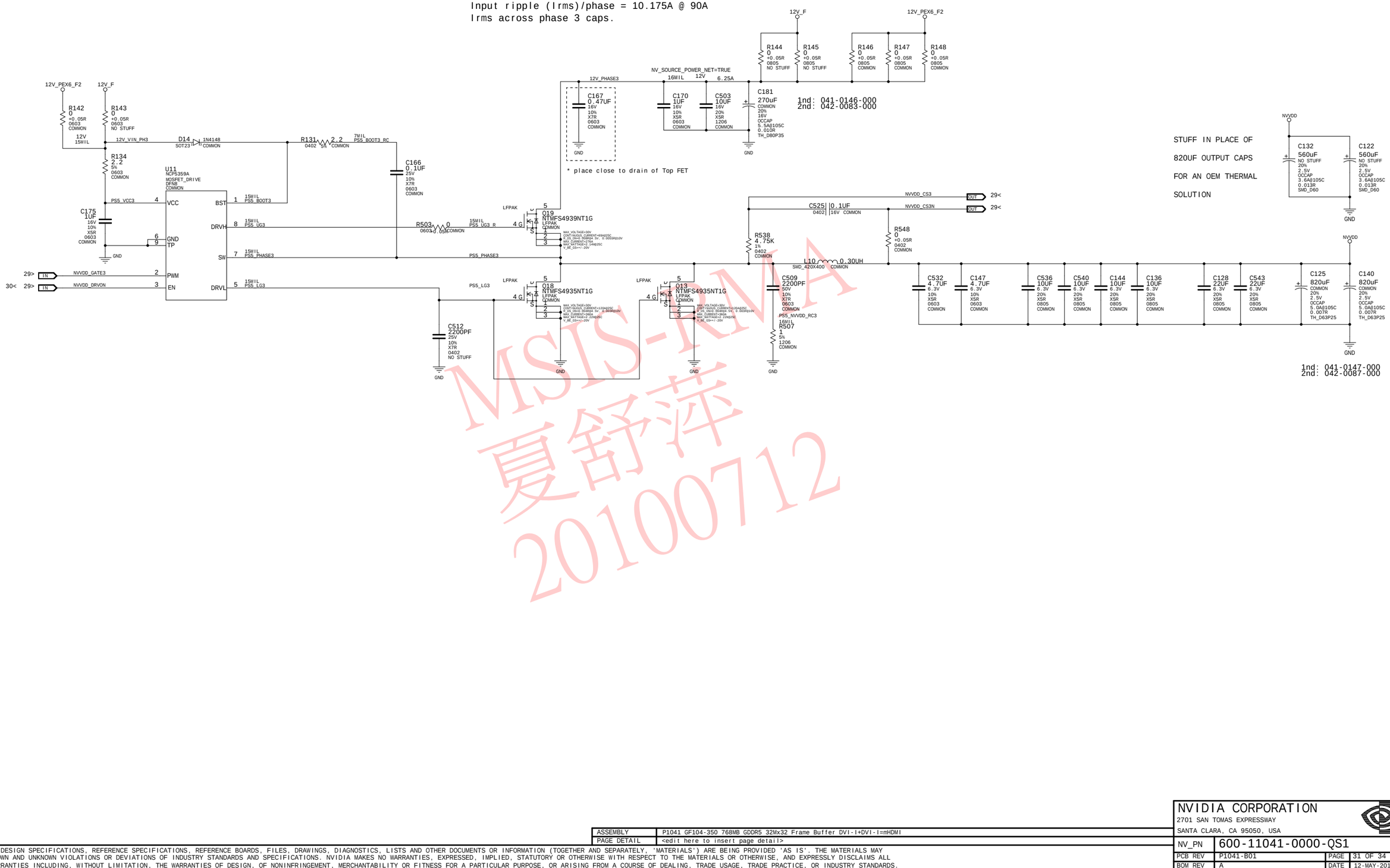
ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	30 OF 34
BOM REV	A	DATE	12-MAY-2010

Page31: PS: NVVDD Phase 3

Input ripple (Irms)/phase = 10.175A @ 90A
Irms across phase 3 caps.



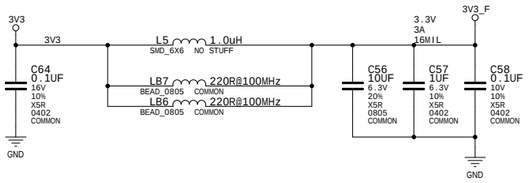
ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

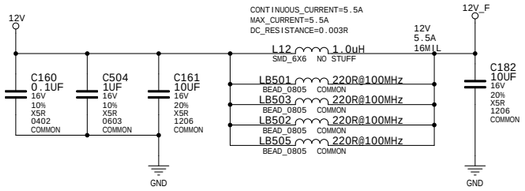
NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	31 OF 34
BOM REV	A	DATE	12-MAY-2010

Page32: PS: Inputs, Shutdown

PEX 3V3 INPUT - 10W



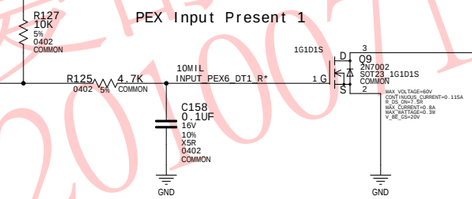
PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W

MUST BE ATTACHED AND POWERED TO START BOARD

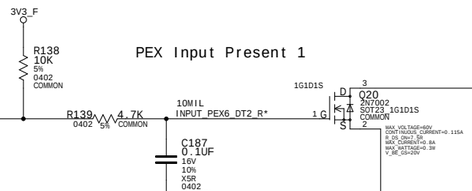
PEX Input Present 1



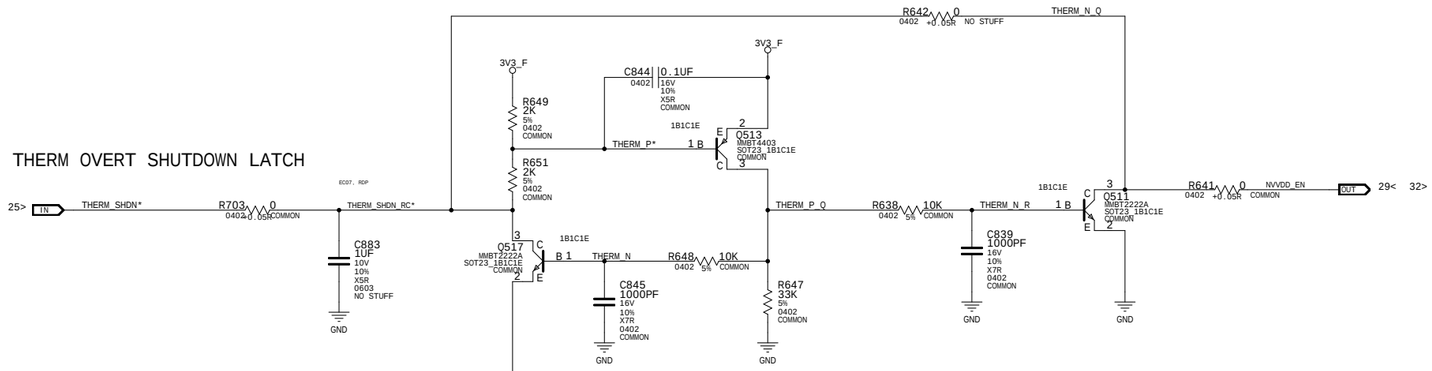
PEX6 INPUT 1 - 2x3 PCIE CON 75W

MUST BE ATTACHED AND POWERED TO START BOARD

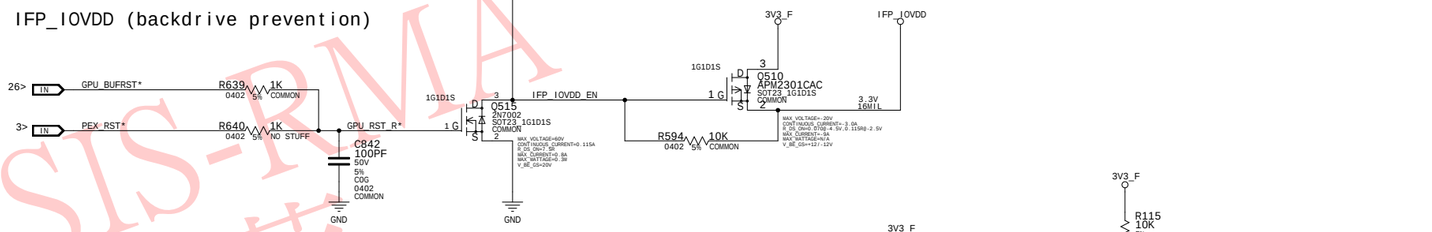
PEX Input Present 1

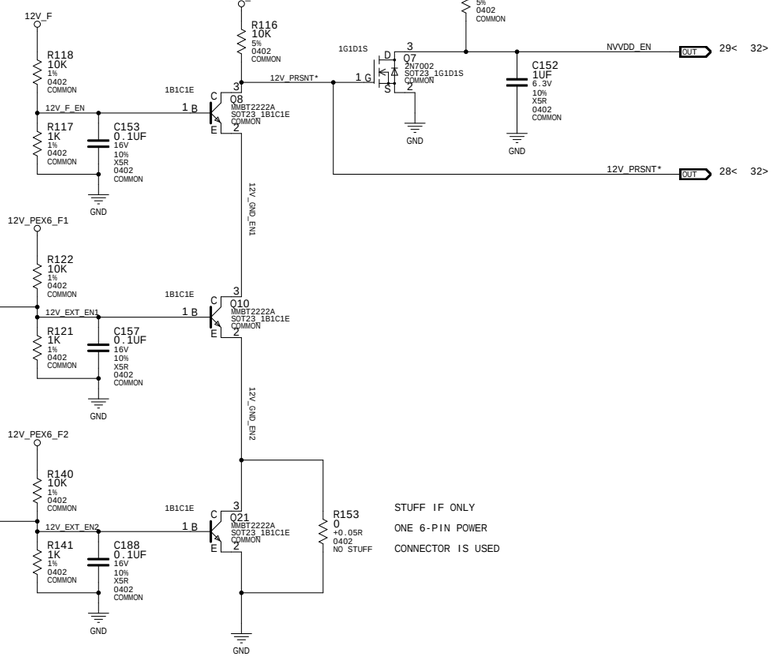


THERM OVERT SHUTDOWN LATCH



IFP_IOVDD (backdrive prevention)





ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

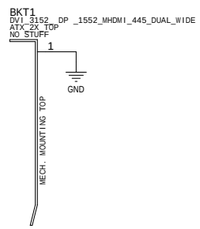
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	32 OF 34
BOM REV	A	DATE	12-MAY-2010

Page33: Mechanical: Bracket/Thermal Solution

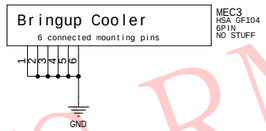
Brackets:

Bracket with DVI_DP_mHDMI : 151-10001-0355-071

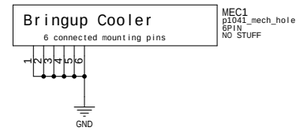


Bracket Screw

Cooler/GPU Stiffener



P1041 MOUNTING HOLE LOCATIONS



ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	33 OF 34
BOM REV	A	DATE	12-MAY-2010

Page34: Blank

ASSEMBLY	P1041 GF104-350 768MB GDDR5 32Mx32 Frame Buffer DVI-I+DVI-I=mHDMI
PAGE DETAIL	<edit here to insert page detail>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-11041-0000-QS1		
PCB REV	P1041-B01	PAGE	34 OF 34
BOM REV	A	DATE	12-MAY-2010